AUGUST 1980

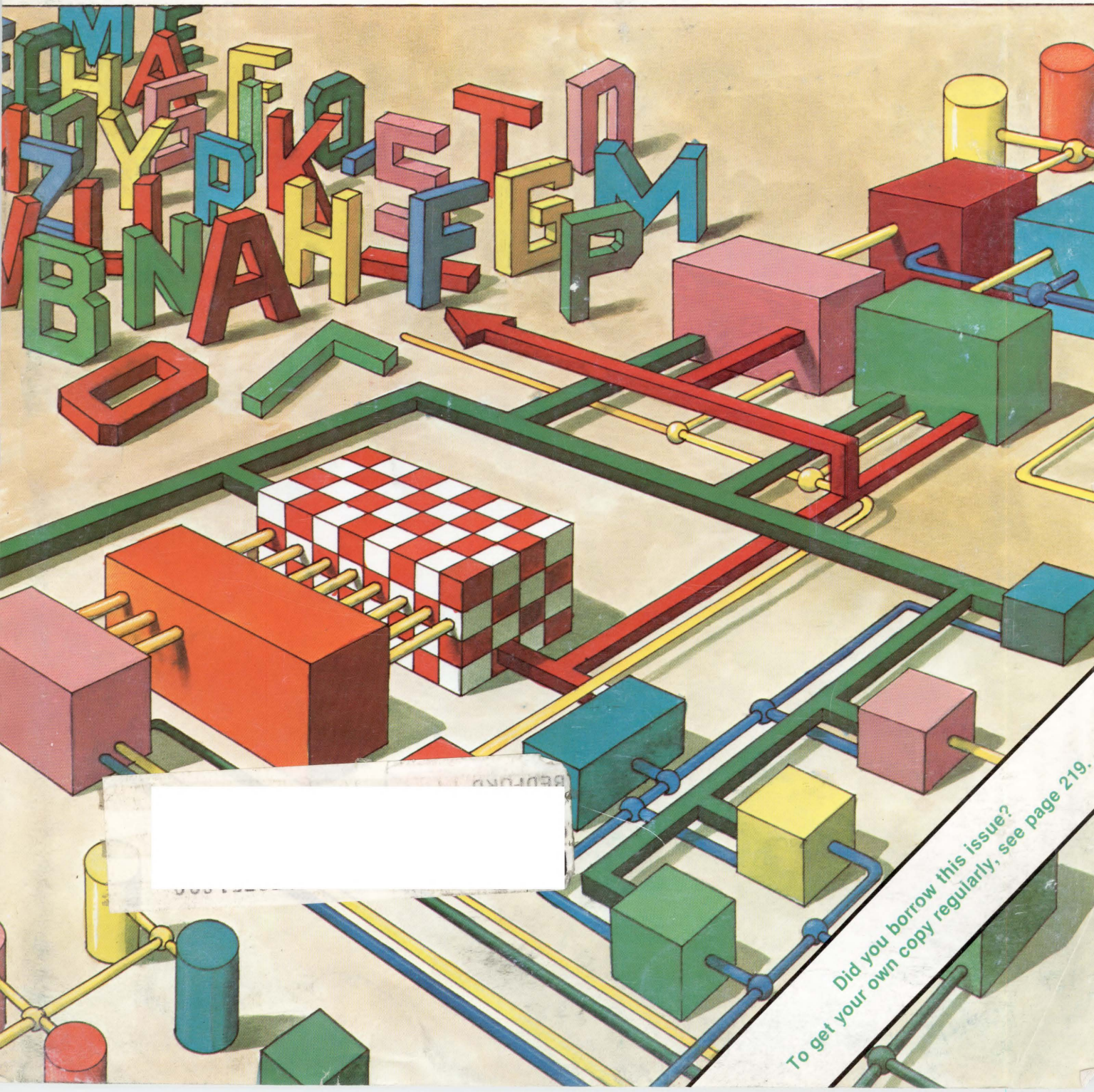
COMPUTER DESIGN

THE MAGAZINE OF COMPUTER-BASED SYSTEMS

WORD PROCESSING SYSTEM DESIGN FOR HIGH THROUGHPUT

MATRIX TECHNIQUE LEADS TO DIRECT ERROR CODE IMPLEMENTATION

INDEXED MEMORY MAPPING EXTENDS MICROPROCESSOR ADDRESS RANGE



How to cut the cost of Winchester backup.

Low cost head crash insurance.
Save up to 50% by using a data cartridge system.
With a transparent controller by Western Peripherals.

The controller makes the CPU think it's working with a half-inch tape drive.

Piggyback as many as eight ¼-inch, 3-M type cartridge drives – and dump nearly 140MB of data.

For low cost archival storage, backup storage or economical head crash insurance, count on data cartridge systems – with controllers from Western Peripherals.

☐ Yes! Please send complete information about low cost mass storage.

NAME TITLE

COMPANY ADDRESS

CITY STATE ZIP ( ) TELEPHONE

CPU Type: ☐ DEC LSI-11* ☐ PDP-11* ☐ Data General NOVA/Eclipse**

western peripherals

Division of Wespercorp
14321 Myford Road
Tustin, CA 92680 (714) 730-6250

*Trade name of Digital Equipment Corporation.** Trade name of Data General Corporation.

CIRCLE 1 ON INQUIRY CARD

New from Kennedy

Model 6809 Data Streamer™

Kennedy does it again. Data Streamer is ideal for Winchester disk drive backup where fast starting and stopping is not required. Designed to emulate the performance of the IBM 8809, Data Streamer has a wide range of features:

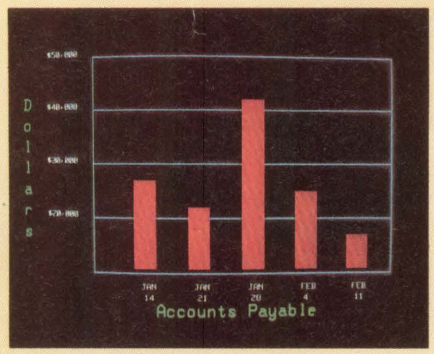
- Tape drive includes built-in industry standard formatter—it's a compact package.
- Contains only four moving parts—hence a much higher MTBF than normal tape drives.
- Streams (read/writes) at 100 ips or, in start/stop mode, 12.5 ips.
- Data Streamer can be mounted in three ways—vertically in rack, horizontally in drawer or horizontally in a low boy console.

Model 6809 has been designed and built with all the innovative features and reliability that Kennedy products are known for. Additionally, Model 6809 is much less expensive than traditional tape transport/formatter combinations. It's the ideal answer for large capacity disk drive backup.

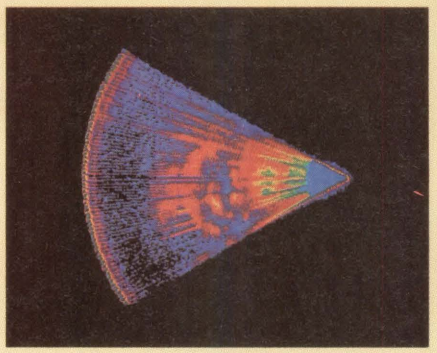
KENNEDY
Subsidiary, Magnetics & Electronics Inc.
1600 Shamrock Ave., Monrovia, CA. 91016
(213) 357-8831 TWX 910-585-3249

KENNEDY • QUALITY • COUNT ON IT

CIRCLE 2 ON INQUIRY CARD



Management Information Display



Ultrasonic heart sector scan

High-resolution display with alphanumerics

Get the professional color display that has BASIC/FORTRAN simplicity

LOW-PRICED, TOO

Here's a color display that has everything: professional-level resolution, enormous color range, easy software, NTSC conformance, and low price.

Basically, this new Cromemco Model SDI* is a two-board interface that plugs into any Cromemco computer.

The SDI then maps computer display memory content onto a convenient color monitor to give high-quality, high-resolution displays (756 H x 482 V pixels).

When we say the SDI results in a high-quality professional display, we mean **you can't get higher resolution than this system offers in an** NTSC-conforming display.

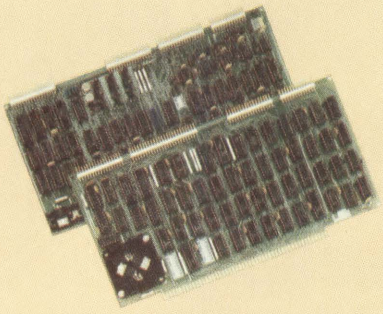
The resolution surpasses that of a color TV picture.

BASIC/FORTRAN programming

Besides its high resolution and low price, the new SDI lets you control with optional Cromemco software packages that use simple BASIC- and FORTRAN-like commands.

Pick any of 16 colors (from a 4096-color palette) with instructions like DEFCLR (c, R, G, B). Or obtain a circle of specified size, location, and color with XCIRC (x, y, r, c).

*U.S. Pat. No. 4121283



Model SDI High-Resolution Color Graphics Interface

HIGH RESOLUTION

The SDI's high resolution gives a professional-quality display that strictly meets NTSC requirements. You get 756 pixels on every visible line of the NTSC standard display of 482 image lines. Vertical line spacing is 1 pixel.

To achieve the high-quality display, a separate output signal is produced for each of the three component colors (red, green, blue). This yields a sharper image than is possible using an NTSC-composite video signal and color TV set. Full image quality is readily realized with our high-quality RGB Monitor or any conventional red/green/blue monitor common in TV work.

Model SDI plugs into Z-2H 11-megabyte hard disk computer or any Cromemco computer

DISPLAY MEMORY

Along with the SDI we also offer an optional fast and novel **two-port** memory that gives independent high-speed access to the computer memory. The two-port memory stores one full display, permitting fast computer operation even during display.

CONTACT YOUR REP NOW

The Model SDI has been used in scientific work, engineering, business, TV, color graphics, and other areas. It's a good example of how Cromemco keeps computers in the field up to date, since it turns any Cromemco computer into an up-to-date color display computer.

The SDI has still more features that you should be informed about. So contact your Cromemco representative now and see all that the SDI will do for you.

Cromemco
incorporated
280 BERNARDO AVE., MOUNTAIN VIEW, CA 94040 • (415) 964-7400
Tomorrow's computers today

CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN THE MAGAZINE OF COMPUTER-BASED SYSTEMS

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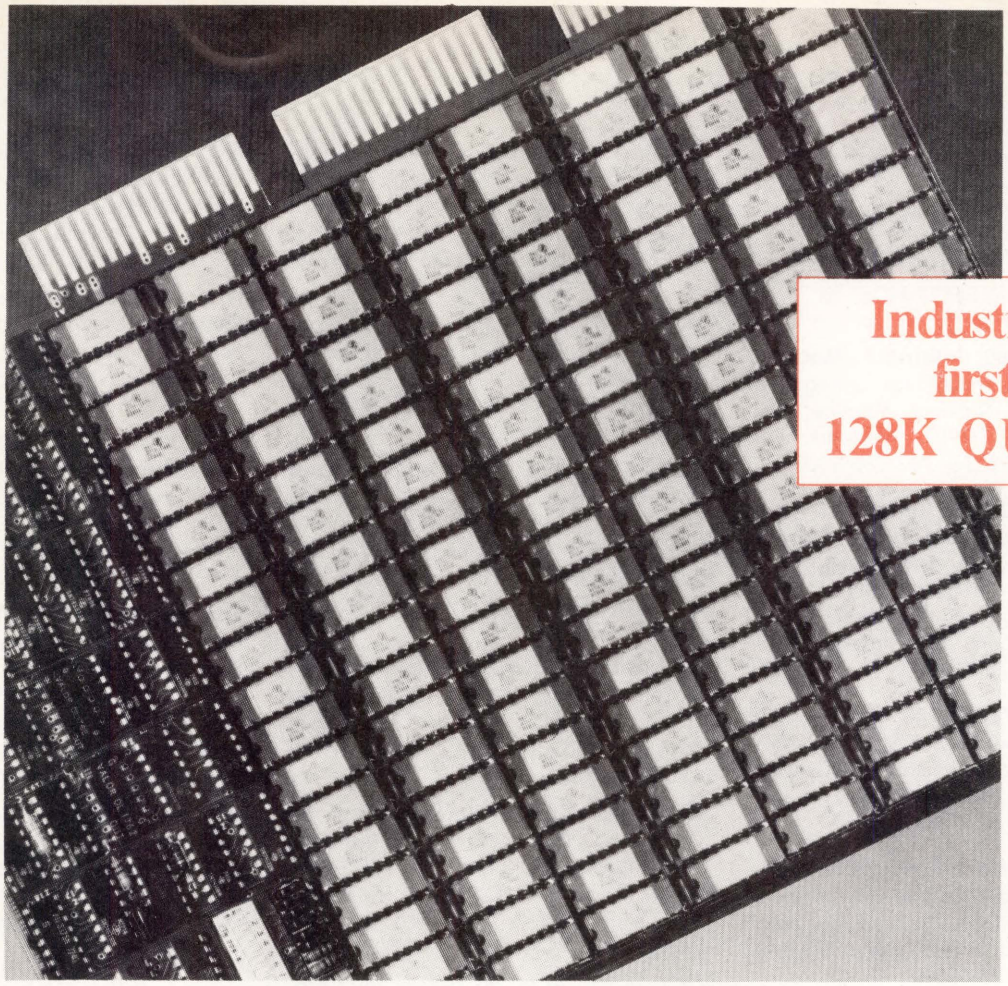

Industry's first 128K QUAD

128K x 18 FOR LSI-11/23®

Dataram Corporation, first to offer a 128K x 18 single-board PDP®-11 ADD-IN, has done it again.

This time with an incredible 128K x 18 semiconductor ADD-IN for DEC®'s LSI-11/23!

This industry first, the DR-113S, is packaged on a standard DEC 8½" x 10" quad board. But more than just being a "first," the DR-113S is also a "best," saving you not only space and money, but also greatly reducing overhead circuitry, optimizing MTBF, and minimizing power consumption. And the DR-113S is also available in 64K and 96K configurations.

From Dataram Corporation, the people who provide everything you need to make a big thing out of the LSI-11 —
• PDP-11/03L compatible chassis • 16K x 18 core ADD-IN • 32K x 18 semi ADD-IN (dual-size board) • BULK CORE and BULK SEMI Disk Emulation Systems • BULK MINI • Tape, Disk, and SMD controllers • and even DEC-manufactured LSI-11 and LSI-11/23 microcomputers and other accessories.

☐ Please tell me more about Dataram 128K x 18 memory for my LSI-11/23 microcomputer.

☐ Please send me information about your other LSI-11 compatible products.

☐ Please have a salesman contact me.

Name _____

Title _____ Phone _____

Company _____

Address _____

City _____ State ____ Zip _____

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CIRCLE 5 ON INQUIRY CARD

CALENDAR

CONFERENCES

SEPT 3-12—1980 Internat'l Machine Tool Show, McCormick Place, Chicago, Ill. INFORMATION: National Machine Tool Builders' Assoc, 7901 Westpark Dr, McLean, VA 22102. Tel: 703/893-2900

SEPT 16-18—FOC '80 (Internat'l Fiber Optics and Communications Exposition), Hyatt Regency Embarcadero, San Francisco, Calif. INFORMATION: Michael A. O'Bryant, Information Gatekeepers, Inc, 167 Corey Rd, Suite 111, Brookline, MA 02146. Tel: 617/739-2022

SEPT 16-18—WESCON/80, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

SEPT 18-21—Mid-Atlantic Computer Show, DC Armory/Starplex, Washington, DC. INFORMATION: National Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

SEPT 22-25—Software INFO (National Software Package Conf and Exposition), Hyatt Regency, Chicago, Ill. INFORMATION: Professional Exposition Management Co, Suite 545, 222 W Adams St, Chicago, IL 60606. Tel: 312/263-3131

SEPT 23-25—COMPCON Fall '80, Capital Hilton, Washington, DC. INFORMATION: COMPCON Fall '80, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

OCT 1-3—Fault Tolerant Computing Systems, Kyoto, Japan. INFORMATION: Prof John Meyer, Dept Elec and Computer Engineering, U of Michigan, Ann Arbor, MI 48109. Tel: 313/763-0037

OCT 1-3—Internat'l Conf on Circuits and Computers for Large Scale Systems, The Rye Town Hilton Inn, Port Chester, NY. INFORMATION: Dr NB Guy Rabbat, 32 Tor Rd, Wappingers Falls, NY 12590. Tel: 914/897-8126

OCT 6-9 AND OCT 14-17—8th World Computer Congress, Tokyo, Japan, and Melbourne, Australia. INFORMATION: AFIPS, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/243-4100

OCT 8-9—Connector Symposium, Benjamin Franklin Hotel, Philadelphia, Pa. INFORMATION: Jim Pletcher, Electronic Connector Study Group, Inc, PO Box 167, Fort Washington, PA 19034. Tel: 717/780-8857

OCT 13-15—Symposium on the Foundations of Computer Science, Sheraton Inn, Syracuse, NY. INFORMATION: Prof Ronald V. Book, Dept of Math and Comp Science, U of California, Santa Barbara, CA 93106. Tel: 805/961-2778, 2171

OCT 13-15—Internat'l Computer Conf: Hong Kong 1980, Hong Kong. INFORMATION: Dr Wellington C. P. Yu, IBM Corp, F02/61C, 5600 Cottle Rd, San Jose, CA 95193. Tel: 408/256-3426

OCT 14-16—Mini/Micro Computer Conf and Exposition, Civic Auditorium, San Francisco, Calif. INFORMATION: Robert D. Rankin, Mini/Micro Conference and Exposition, 32302 Camino Capistrano, Suite 202, San Juan Capistrano, CA 92675. Tel: 714/661-3301

OCT 16-19—Mid-West Computer Show, McCormick Place, Chicago, Ill. INFORMATION: National Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

OCT 20-23—CPEUG '80 (Meeting of the Computer Performance Evaluation Users Group), Orlando, Fla. INFORMATION: Theodore F. Gonter, U.S. General Accounting Office, 441 G St, NW, Rm 6118, Washington, DC 20548. Tel: 202/275-5410

OCT 26-29—ACM '80 (Assoc for Computing Machinery Nat'l Conf and Exhibition), Opryland Hotel, Nashville, Tenn. INFORMATION: Lucy Jean Johnson, Box 1980 Station B, Nashville, TN 37235. Tel: 615/322-2951

OCT 27-30—ICCC '80 (Internat'l Conf on Computer Communication), Peachtree Plaza Hotel, Atlanta, Ga. INFORMATION: ICCC '80 Executive Committee, PO Box 280, Basking Ridge, NJ 07920. Tel: 201/221-8800

OCT 28-30—Interface West, Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: Peter B. Young, The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

OCT 30-NOV 1—Nat'l Small Computer Show, New York Coliseum, New York, NY. INFORMATION: Ralph Ianuzzi, 110 Charlotte Place, Englewood Cliffs, NJ 07632. Tel: 201/569-8542

NOV 3-5—Conf on Computer Graphics in CAD/CAM Systems, MIT, Cambridge, Mass. INFORMATION: Prof David C. Gossard, Dept of Mechanical Engineering, Rm 3-445, Massachusetts Inst of Technology, 77 Massachusetts Ave, Cambridge, MA 02139. Tel: 617/253-4465

NOV 4-6—MIDCON/80, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

NOV 6-12—Electronica '80, Munich Fairgrounds, Munich, West Germany. INFORMATION: Franc D. Manzolillo, Rm 6015, U.S. Dept of Commerce, Washington, DC 20230. Tel: 202/377-2991

NOV 20-23—Northeast Computer Show, Hynes Auditorium/Prudential Ctr, Boston, Mass. INFORMATION: National Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

NOV 30-DEC 4—NTC '80 (National Telecommunications Conf), Shamrock Hilton Hotel, Houston, Tex. INFORMATION: John R. Howell, Houston Lighting and Power Co, PO Box 1700, Houston, TX 77001. Tel: 713/228-9211, X3351

DEC 2-5—CMG XI (11th Internat'l Conf of the Computer Measurement Group), Sheraton-Boston Hotel, Boston, Mass. INFORMATION: Judith G. Abilock, Price Waterhouse and Co, Office of Government Services, 1801 K St, NW, Washington, DC 20006. Tel: 202/296-0800

DEC 4—California Computer Show, Hyatt-Palo Alto, Palo Alto, Calif. INFORMATION: Norm De Nardi, Norm De Nardi Enterprises, 95 Main St, Los Altos, CA 94022. Tel: 415/941-8440

SEMINARS

OCT 20-21—Distributed Processing and Multiprocessing: Components and Applications; OCT 27-28—Data Communications; AND OCT 30-31—Microprocessors: Hardware, Software, and Applications, Worcester Polytechnic Inst, Worcester, Mass. INFORMATION: Ginny Bazarian, Office of Continuing Professional Education, Worcester Polytechnic Inst, Worcester, MA 01609. Tel: 617/753-1411, X517

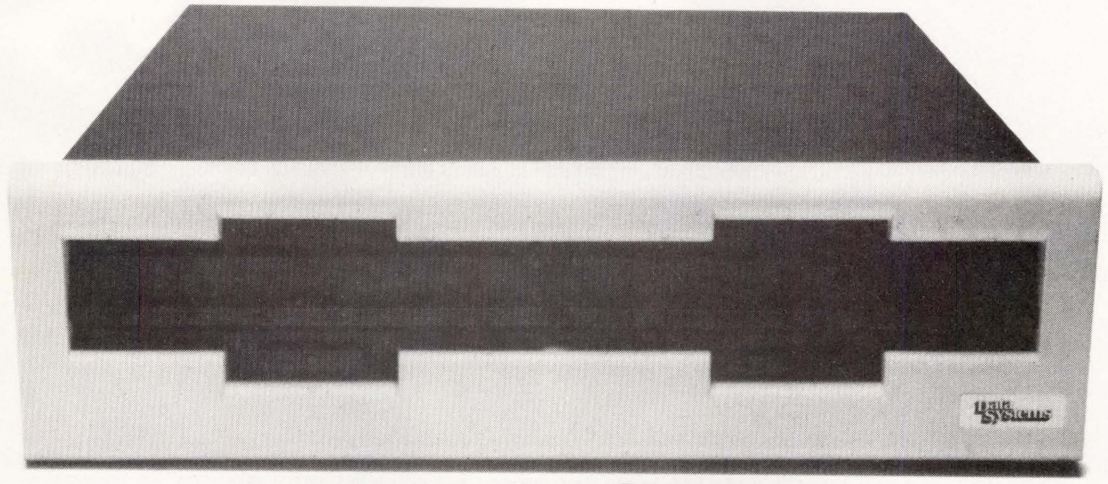
NOV 3-4—Workshop on Aerospace Applications of Microprocessors, Goddard Space Flight Ctr, Greenbelt, Md. INFORMATION: Robert J. Schwartz, McDonnel Douglas Astronautics Co, Box 516, St Louis, MO 63166

SHORT COURSES

OCT 7-10—Pascal Computer Programming, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106

OCT 27-29—Fundamentals of Data Communications, American Management Associations Headquarters, New York, NY. INFORMATION: American Management Assocs, 135 W 50th St, New York, NY 10020. Tel: 212/586-8100

THE DSD 440. TOTAL DEC® RX02 COMPATIBILITY,



AND MORE.

The DSD 440 is the only alternative to the DEC RX02 that's 100% software, hardware and media compatible with LSI-11, PDP®-11 and PDP-8 computers, including those with extended memory. It can be configured as an RX02 for DEC double density or IBM 3740 single density recording, or as an RX01 for backward operating system compatibility.

MORE

A 512-byte hardware bootstrap is built into all PDP-11 and LSI-11 interfaces. It loads system software automatically from either single or double density diskettes. Extensive self-testing is DIP-switch selectable with the "Hyperdiagnostics" that run without being connected to a computer. The low profile 5¼-inch DSD 440 features write protection and diskette formatting.

FASTER

The optimized DSD 440 microcode increases system throughput when using the RT-11 foreground/background monitor. In particular, the DSD 440 with an LSI-11 runs fill and empty buffer operations 20% faster than an RX02.

FOR LESS

The DSD 440 is the RX02 compatible flexible disk system that combines high performance and advanced features with fast delivery... at a lower price. For further information, call or write Data Systems Design today. A data sheet and price list will be forwarded to you immediately.

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CIRCLE 6 ON INQUIRY CARD

BIOMATION K100-D

Compare this general purpose logic analyzer with the currently accepted industry standard.

The K100-D wins over Hewlett-Packard's 1615A hands down!

Logic designers have made Gould's powerful Biomation K100-D our fastest selling logic analyzer

ever. You'll see why once you compare it to its nearest competitor, the 1615A from Hewlett-Packard.

Compare clocking speed.

With a 100 MHz clock rate, the K100-D gives you resolution to 10 ns—*five times better than the 1615A's.* Use the K100-D's latch mode to catch gliches as narrow as 4 ns. It gives you the most precise logic analysis for today's high speed minicomputer, mainframe and microprocessor systems. Best of all, you're already prepared for faster designs as they arrive.

Compare capacity.

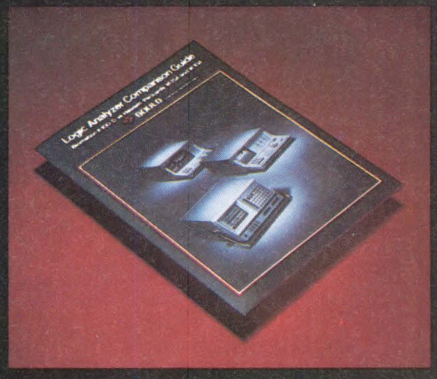
The K100-D's 1024 word memory is *four times as deep as the 1615A's.* This dramatically extends the length of data you can trap from your system at any one time. And that means faster, more accurate debugging. In addition, the K100-D's standard 16 channel format can be expanded to 32 channels for work on the new generation of 16-bit microprocessors.

Compare your productivity.

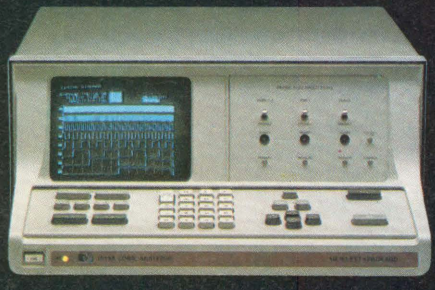
Finally, the K100-D makes designers more productive with convenience features superior to those of the 1615A. The K100-D has a larger keyboard, plus an interactive video display. Comprehensive status menu. Data domain readout in hexadecimal, octal, binary or ASCII. And the list goes on and on.

The final analysis.

To help you evaluate these two fine instruments before you buy, we've prepared a point-by-point *competitive comparison* of the two. If you're designing and debugging high-performance digital systems, you'll want to read this document carefully. To get your free copy, just use the reader service number or write Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.

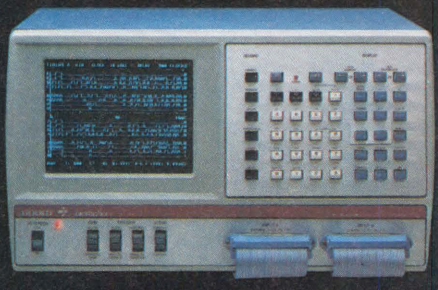


Hewlett-Packard 1615A
A very good logic analyzer



Speed: to 20 MHz
Resolution: 50 ns
Memory: 256 words
Channels: 8 timing & 16 data, or 24 data

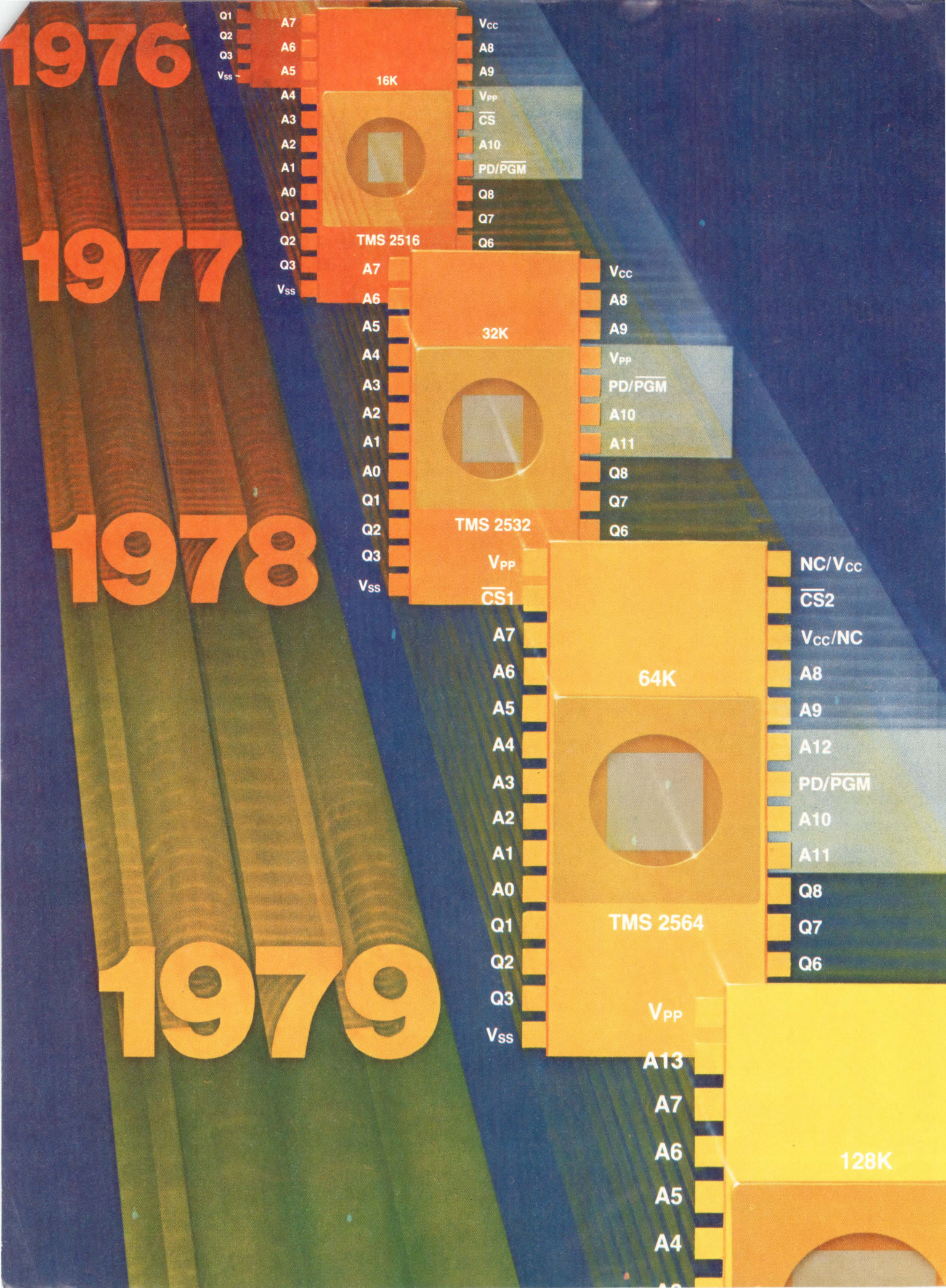
Biomation K100-D
The industry's finest logic analyzer



Speed: to 100 MHz
Resolution: 10 ns
Memory: 1024 words
Channels: 16 timing or 16 data, or 32 data

GOULD
An Electrical/Electronics Company

CIRCLE 7 ON INQUIRY CARD


1976
Q1
Q2
Q3
VSS
A7
A6
A5
A4
A3
A2
A1
A0
Q1
Q2
Q3
VSS
16K
TMS 2516
VCC
A8
A9
VPP
CS
A10
PD/PGM
Q8
Q7
Q6
1977
A7
A6
A5
A4
A3
A2
A1
A0
Q1
Q2
Q3
VSS
32K
TMS 2532
VCC
A8
A9
VPP
PD/PGM
A10
A11
Q8
Q7
Q6
1978
VPP
CS1
A7
A6
A5
A4
A3
A2
A1
A0
Q1
Q2
Q3
VSS
64K
TMS 2564
NC/VCC
CS2
VCC/NC
A8
A9
A12
PD/PGM
A10
A11
Q8
Q7
Q6
1979
VPP
A13
A7
A6
A5
A4
128K

64K EPROMs from Texas Instruments. Defining the future. Ready today.

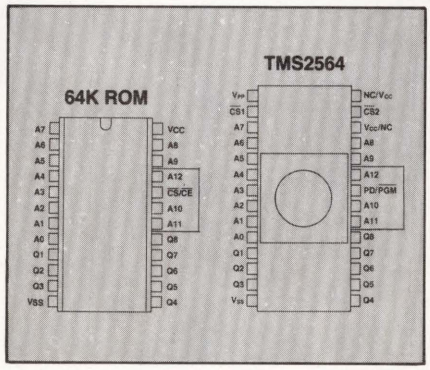
EPROMs regularly double in density — 128K devices are inevitable. By factoring TI's new 64K EPROM into your plans today, you can pave the way for these greater densities and minimize system redesign.

Because the new TMS2564 comes in a 600-mil, 28-pin, dual-in-line package. Plug compatible with that anticipated for the 128K EPROMs ... and ROMs. When the time comes to upgrade, you'll be able to substitute one for the other.

Outstanding compatibility

In the meantime, the TMS2564 EPROM allows you a great deal of latitude. For maximum compatibility with present devices, its JEDEC-approved pinout is derived from the industry-standard 24-pin 64K ROM supplied by eight sources.

On the new TMS2564, pins 26 and 28 are reserved for the 5-V supply. With a supply trace to pin 26, both 24- and 28-pin devices can be used with no jumpering. If you choose, you can even use smaller EPROMs without compatibility problems. And upgrading from the TMS2532 32K EPROM is a snap.



Low power

The TMS2564 offers you the lowest power per bit in the industry ... only 13 μW max active. A must for high reliability and low system operating costs.

Widest choice

Adding the TMS2564 to our fast-growing EPROM family gives you a choice unmatched in the marketplace. All members are available in 600-mil packages with industry-compatible pinouts. All share the reliable production-proven TI EPROM technology.

Here now

TI's TMS2564 has been in production since mid-1979. No need to wait — place your order today for the industry's first 64K EPROM, from the industry's first supplier of 16K and 32K EPROMs. Check your nearby TI sales office or authorized distributor. Or write Texas Instruments, P.O. Box 1443, M/S 6965, Houston, Texas 77001.

Fifty Years of Innovation

PACESETTING EPROMs FROM TI

Device	Description	Power Supply	Typical Power (0°C) Operating	Standby	Access Time
TMS2564	64K	5 V	400 mW	50 mW	450 ns
TMS25L32	32K	5 V	325 mW	50 mW	450 ns
TMS2532	32K	5 V	400 mW	50 mW	450 ns
TMS2516-35	16K	5 V	285 mW	50 mW	350 ns
TMS2516	16K	5 V	285 mW	50 mW	450 ns
TMS2508-25	8K	5 V	250 mW	50 mW	250 ns
TMS2508-30	8K	5 V	250 mW	50 mW	300 ns
TMS2716	16K	+12, ±5 V	315 mW	—	450 ns
TMS27L08	8K	+12, ±5 V	245 mW	—	450 ns
TMS2708	8K	+12, ±5 V	690 mW	—	450 ns
TMS2708-35	8K	+12, ±5 V	690 mW	—	350 ns

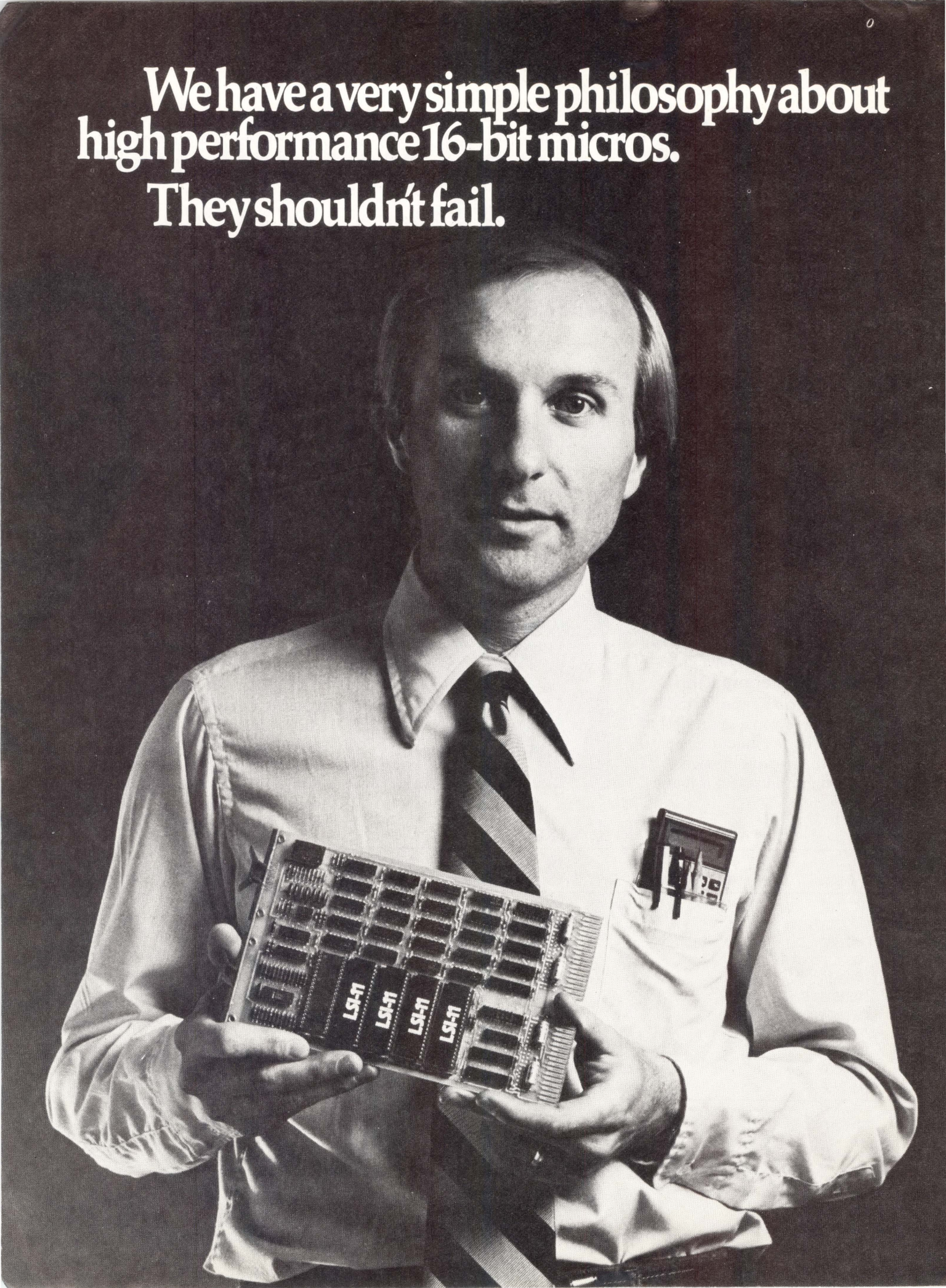
TEXAS INSTRUMENTS
INCORPORATED

85135A

CIRCLE 8 ON INQUIRY CARD

We have a very simple philosophy about high performance 16-bit micros.

They shouldn't fail.



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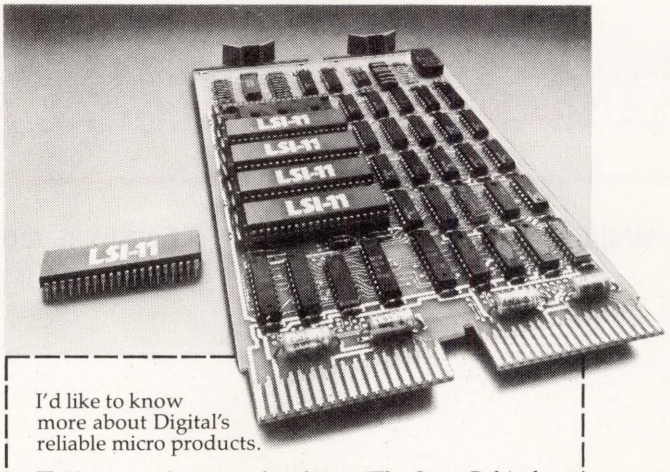

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CIRCLE 9 ON INQUIRY CARD

RF MODEM DESIGN FOR BROADBAND COAXIAL LOCAL AREA NETWORKS

D. G. Willard and P. E. Wagner

The MITRE Corporation
Bedford, MA 01730

Established community antenna television technology provides a highly reliable, inexpensive, broadband 2-way distribution network on which multimode communications can be readily implemented in a local area. When properly designed, the network furnishes common transmit and receive signal levels that are independent of both frequency and subscriber location. It also provides a very good signal to noise ratio and a low intermodulation characteristic.

Many community antenna television (CATV) network applications include some form of digital communication. Each class of digital subscriber equipment requires a radio frequency (rf) modem at the interface to the cable network. The modulated signal emitted by all such modems must be clean, ie, have no significant extraneous signals that might interfere with other signals in the spectrum. The modem must also produce a signal level sufficient to match the network. Each receiver section must selectively reject all frequencies except that of the desired signal and be sensitive enough to acquire and demodulate the signal.

Availability of all traffic to all subscribers is an inherent characteristic of CATV networks. The bus concept is, therefore, especially promising for local area digital communications. In some bus applications the modem must be carefully implemented to insure that the receiver does not "hear" its own transmitter directly and thus mask reception of transmissions being received from the network.

Two ways of implementing 2-way CATV distribution networks are either on a single cable using bandsplitting techniques, or on two separate cables, in effect employing space division. Differences between these two methods have little effect on the functional requirements of digital modems. Modems intended for single-cable networks must transmit and receive on a common cable connection at different frequencies. Those intended for 2-cable networks must transmit and receive on separate cable connections, generally on the same frequency. There is no other significant difference.

Classes of RF Modems

Two main classes of rf modems for CATV applications are those intended for point to point links replacing dual-pair wireline links, and those to be used in some form of multiple subscriber digital bus such as time division multiple access (TDMA), listen-while-talk, and polling.

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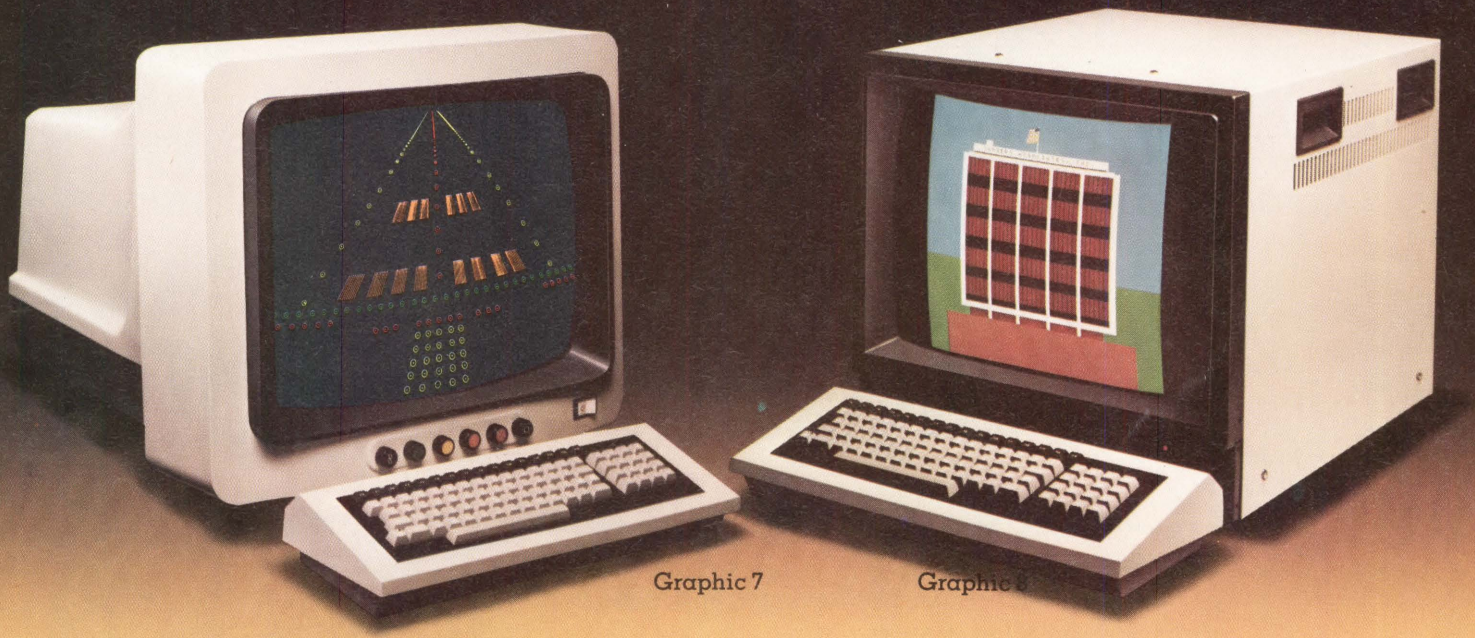

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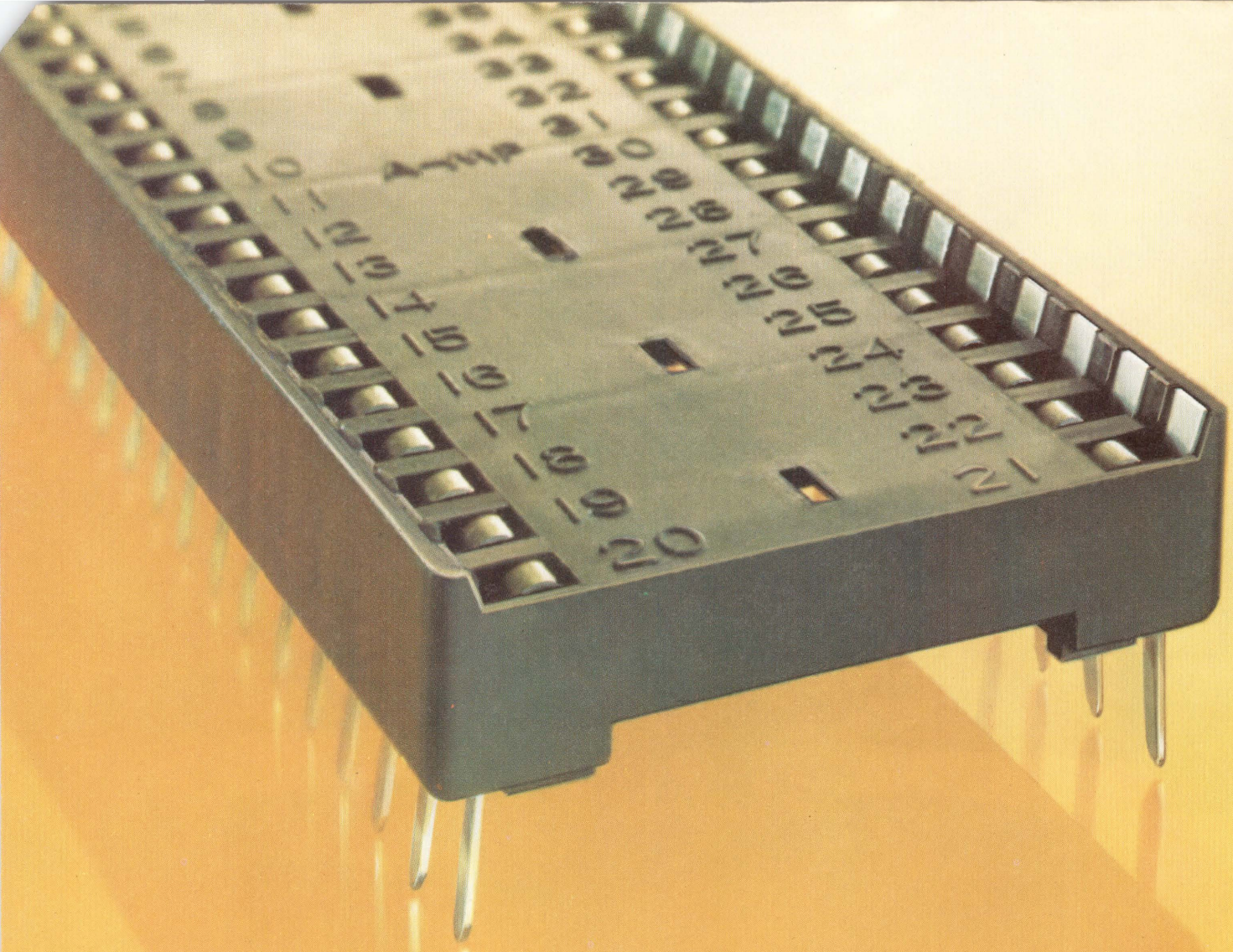

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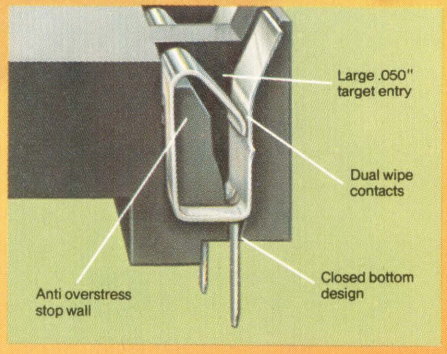

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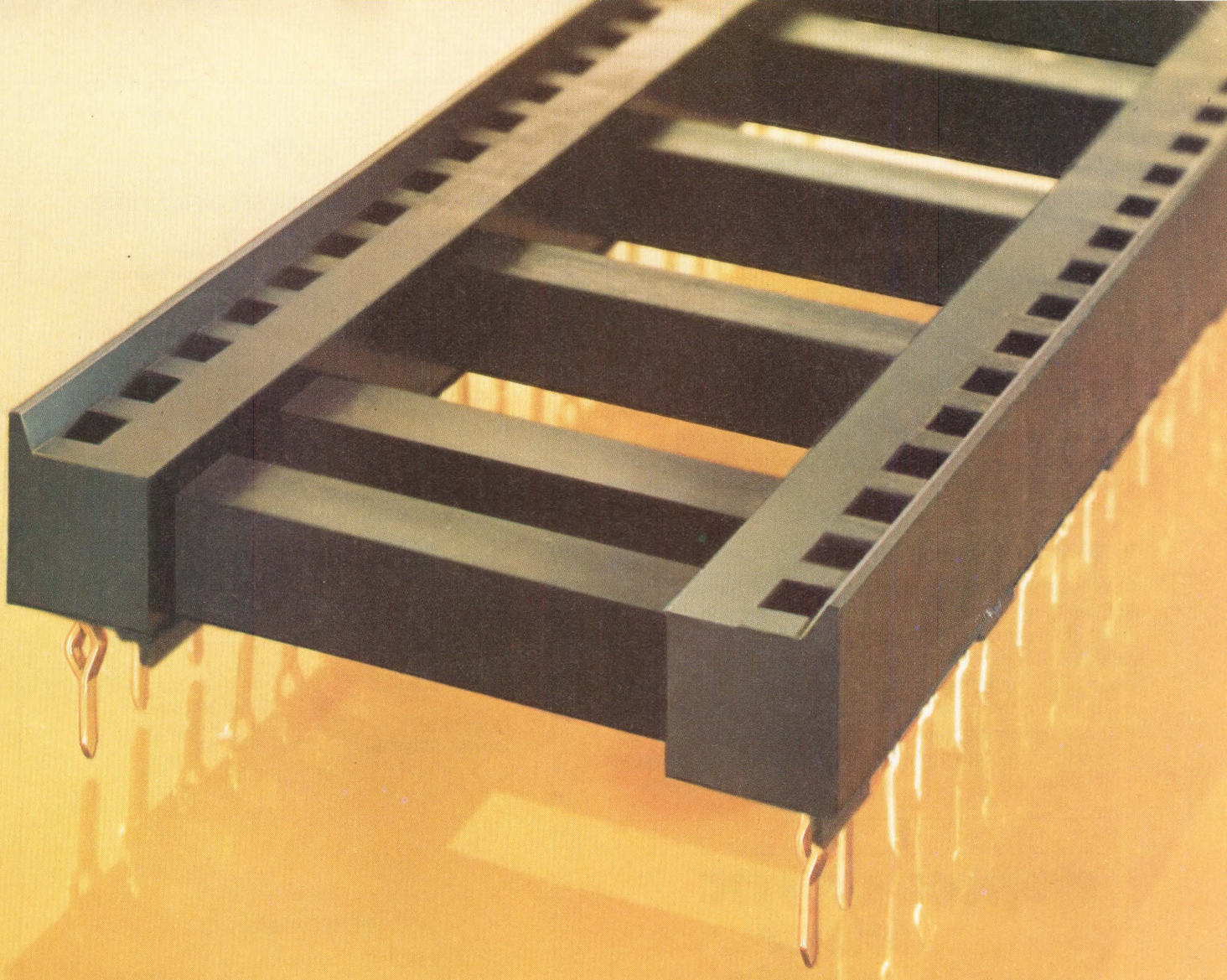

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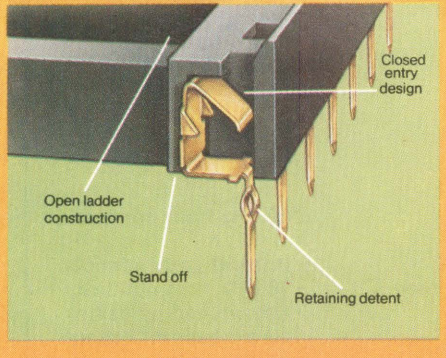

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Point to point modems are generally implemented to provide full-duplex service. They are used in cross-frequency matched pairs, where subscriber A transmits in frequency band 1 and receives in frequency band 2, while subscriber B transmits in band 2 and receives in band 1. Both rf carriers are on continuously, and signal acquisition time is not critical.

In contrast, a modem for a multiple subscriber bus must emit signals only during the subscriber's transmit time, and acquire other subscribers' signals rapidly in order to minimize the amount of overhead time associated with each transmission. Generally, bus modems for 2-cable systems are also required to transmit and receive on the same frequency band. In some bus applications they transmit and receive simultaneously, and therefore are required to provide sufficient isolation between transmitter and receiver to insure that the subscriber's own transmission is received only from the network.

RF Modem Constraints

Interface with the CATV network should be carried out in such a manner that the presence of the rf modems does not affect other signals that might be on the cable. Moderate wideband impedance matching must also be achieved. In single-cable networks modem impedances are normally isolated from the drop cable by a 3-dB rf combiner/splitter that connects the transmitter and receiver to the drop cable. Moderate excursions from the nominal 75-Ω design center

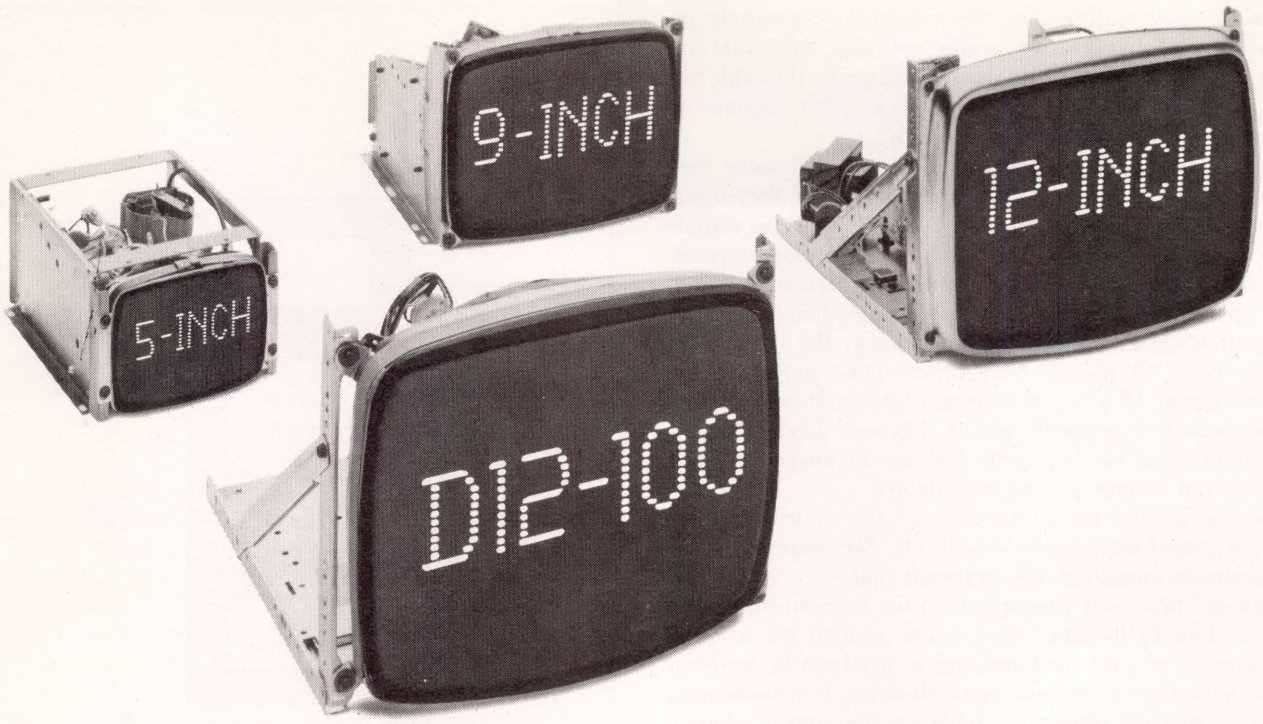
MODEM RF MODULE SPECIFICATIONS

Transmitter section	
Center frequency	50.0 MHz
Modulation	Phase-continuous fm
Deviation	1 MHz
Modulating data rate	1.5M bits/s max
Baseband interface	TTL (data and key)
Rf interface	75Ω (VSWR ⩽3:1 from 5 to 300 MHz)
Output level	60 dBmV (0 dBmV = 1 mV rms)
On/off ratio	100 dB
2nd harmonic	⩽– 60 dB below carrier level
All other harmonics and spurious	⩽– 70 dB below carrier level
Receiver section	
Center Frequency	50.0 MHz
Passband	2 MHz (– 6 dB points)
Demodulation	fm
Modulating data rate	1.5M bits/s max
TTL interface	Open collector (data and key)
Rf interface	75 Ω (VSWR ⩽ 3:1 from 5 to 300 MHz)
Input level	0 to 20 dBmV
Carrier detection	0 dBmV

PERFORMANCE

Transmitter section	
Deviation	± 2% of nominal
Center frequency	± 100 kHz from nominal. Center frequency is determined by adding numerical value of mark and space frequencies and dividing by two
Signal balance	± 1 dB difference between mark and space frequencies
Level	± 2 dB from nominal. Determined by measuring average of amplitudes of mark and space frequencies
Receiver section	
Filter center frequency	± 50 kHz from nominal
Filter bandwidth	± 200 kHz from nominal
Discriminator center frequency	± 20 kHz from nominal. Determined by using zero crossover voltage of discriminator response

The device(s) have met the above tolerances over a temperature range of 0 to 40 °C and voltage supply of 11.5 to 13.0 Vdc



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are sufficiently nullified by the splitter to cause only insignificant mismatches. In 2-cable networks, moderate impedance excursions are sufficiently isolated by the cable tap or signal splitters so that effects on other signals or subscribers are of a minor nature only.

Spurious transmit signals are to be avoided since they could cause interference with other services if they occur outside the signal band. Similarly, inband spurious signals can cause degradation in the recovered data. Bus transmitters must exhibit a good on/off ratio of emitted signal level. During transmit periods, when only one modem is emitting a signal while all others are on standby, the cumulative energy from all the off transmitters must not mask the desired signal. In a system having a large number of active subscribers, it is generally agreed that such leakage signals will combine as random noise because of unsynchronized carriers and diverse propagation delays.

The bus modem must interface with the control circuitry using standard logic levels, usually TTL. Six separate signals are generally employed: key (transmit enable, receive signal presence), data, and timing (clock) for both transmit and receive. Usually transmit clock is not used by the modulation process of CATV modems, and so need not be supplied to the modulator in most designs. However, it is convenient to have transmit timing available on the control modem cable connector to facilitate testing of the control circuit without the modem in place.

The modem receiver is generally required to derive receive timing and use it to reclock the recovered data for output. Data transitions may be used to phase a locally generated clock signal for this purpose. The alternative is to encode transmit clock with transmit data and recover the clock from the received signal. The major disadvantage of the latter approach is that it requires twice the signaling rate used to transmit data alone, and so requires an increase in signal bandwidth.

Cable Bus Modem Design

Specifications and performance data for an rf modem developed at MITRE Corp for CATV digital communications applications are shown in the Panel. A modem for cable-based buses consists of four major elements (Fig 1). The rf modulator accepts transmit data and key and generates an rf signal containing the transmit data information. The rf demodulator accepts the rf signal from the cable and recovers the transmitted data and the carrier presence information (receive key). Timing recovery circuitry develops a times-one clock signal from the recovered data and uses this signal to reclock the recovered data and key. The power sequencing circuitry insures that the modem generates no extraneous signals during power-up and power-down operations.

Components of the rf module are shown in Fig 2. The modulator consists of a phase-coherent frequency shift keying (FSK) oscillator, an active isolating buffer, and a passive low pass filter. Transmit data cause the oscillator to change frequency smoothly as a function of the data pattern. The transmit key stops the oscillator and shuts off the buffer. Because the oscillator signal itself is clean and narrow, contains only low level carrier frequency harmonics, and has no spurious frequencies, only a low pass filter is required to produce a clean output signal.

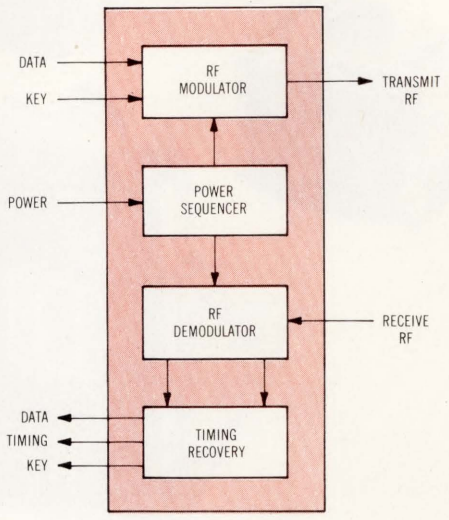


Fig 1 Major elements of CATV rf modem. Modulator develops transmit signal. Demodulator recovers data from cable signal. Timing circuit uses clock signal to reclock recovered data and key. Power sequencing circuitry prevents generation of extraneous signals

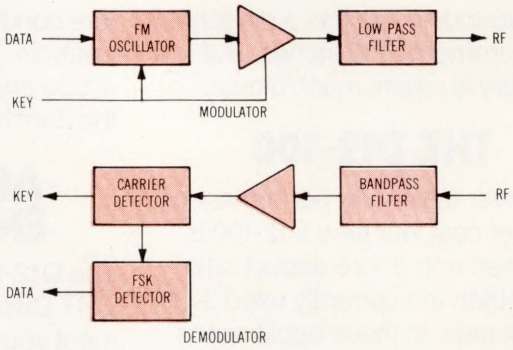
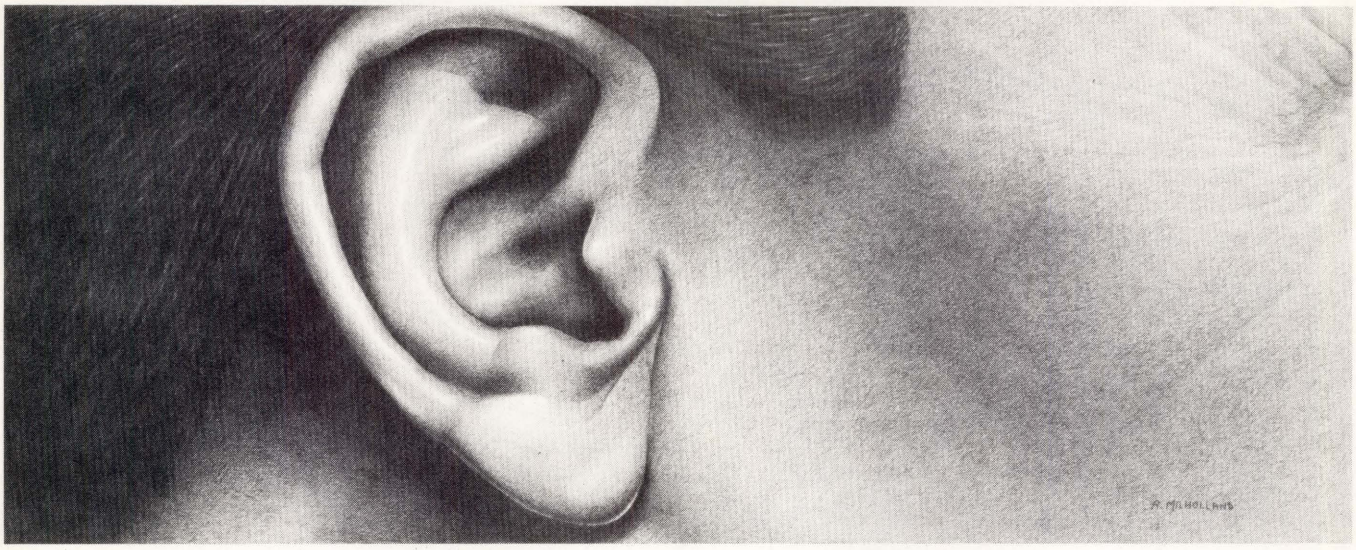


Fig 2 Components of rf module. Modulator contains phase-coherent FSK oscillator, active isolating buffer, and passive low pass filter. Demodulator has bandpass filter, rf amplifier, and fm and carrier detectors

Listen, listen, listen.



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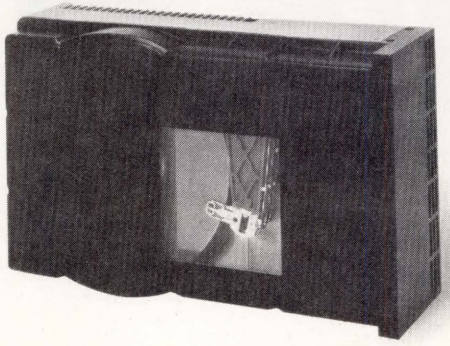

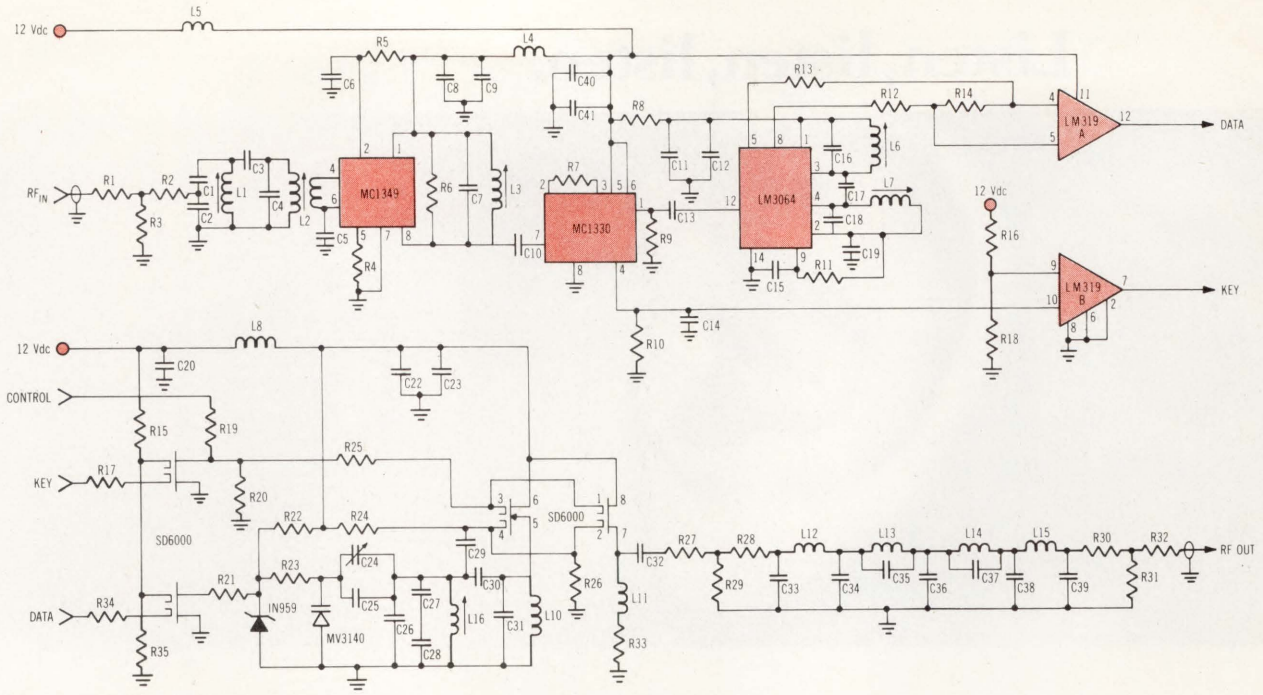

Fig 3 Schematic of rf module. Circuit is constructed of readily available components

The demodulator includes a bandpass filter, rf amplifier, and the frequency modulation (fm) and carrier detectors. The filter selects only the desired signal to be amplified. The fm detector produces a replica of the information used to modulate the rf carrier and is, therefore, the recovered data. The carrier detector generates an active level signal during carrier presence and is the recovered key.

A schematic diagram of the rf portions of a bus modem is shown in Fig 3. The MC1349 TV intermediate frequency (if) amplifier chip is used in the demodulator as an rf amplifier within a 3-pole bandpass filter. The filter is isolated from the cable by a 3-dB pad. Video detector chip MC1330 has a dual function of detecting carrier presence and providing additional amplitude-limited rf gain for the data detector. The LM3064 TV automatic frequency control (afc) discriminator chip provides a differential output as a function of the received signal. These levels are converted to TTL levels by one section of an LM319 voltage comparator and supplied as recovered data. The amplitude detector signal is also converted to transistor-transistor logic (TTL) by a second section of the LM319.

Transmit data and key are first buffered by elements of an SD6000 chip to convert to on-modem levels in the modulator. Since these levels directly affect the frequency deviation of the oscillator, buffering isolates the modulator from variations in external TTL voltages. The second SD6000 twin dual-gate MOSFET chip, usually used as an rf amplifier, is used here as an oscillator and buffer. A varactor is lightly coupled into the oscillator tank circuit, producing phase-continuous FSK modulation. The coupling capacitor is used as the deviation adjustment element to minimize the resistor-capacitor (RC) time constant. The transmit low pass filter has been designed for 60-MHz cutoff. This permits the transmit center frequency to be adjusted anywhere between 40 and 60 MHz by changing only the oscillator resonant circuit.

The modem as described will function properly at data rates up to 1.5M bits/s. Nominal receive signal strength is 0 dBmV (1 mV rms across 75 Ω). Nominal transmit level is 60 dBmV. An interior view of a completed modem is shown in Fig 4. The reader is encouraged to consider adapting this proven rf modem for CATV to his own applications.

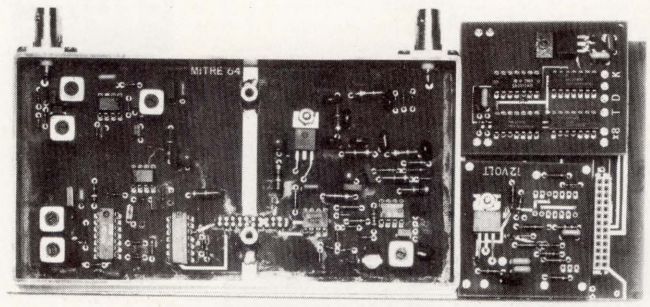

Fig 4 Modulator/demodulator with mother card. Latter includes power sequencing and receive timing recovery circuits. Modem is used for 50-MHz center frequency unslotted contention bus digital communication system at 1.152M bits/s

Editor's note: Interested readers may obtain a complete parts list for the modem diagrammed in Fig 3 by writing to: The Editor, *Computer Design*, 11 Goldsmith St, Littleton, MA 01460.

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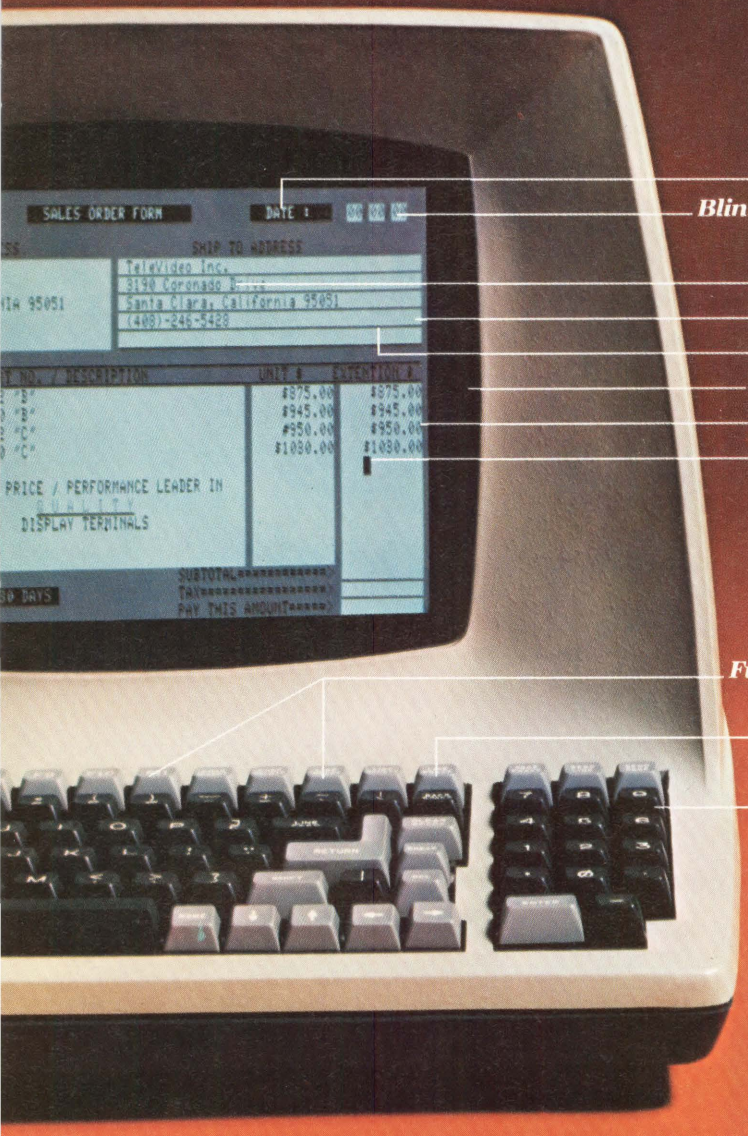

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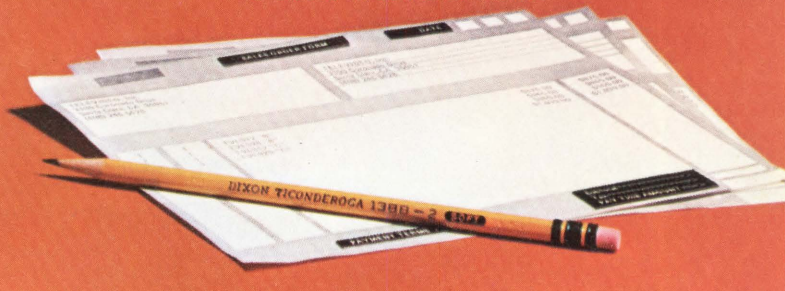

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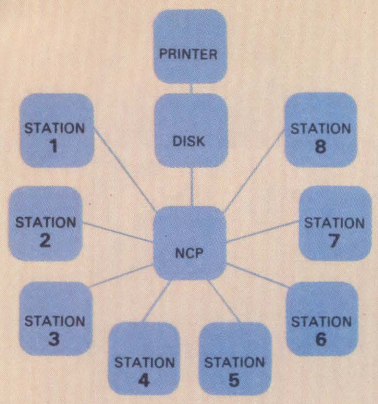

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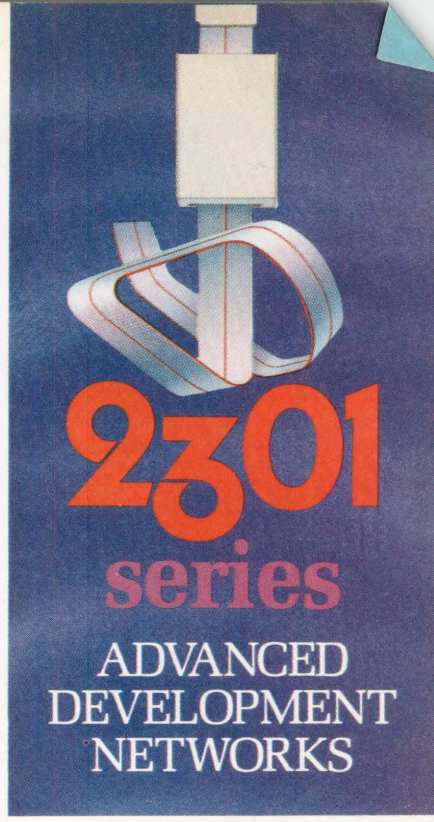

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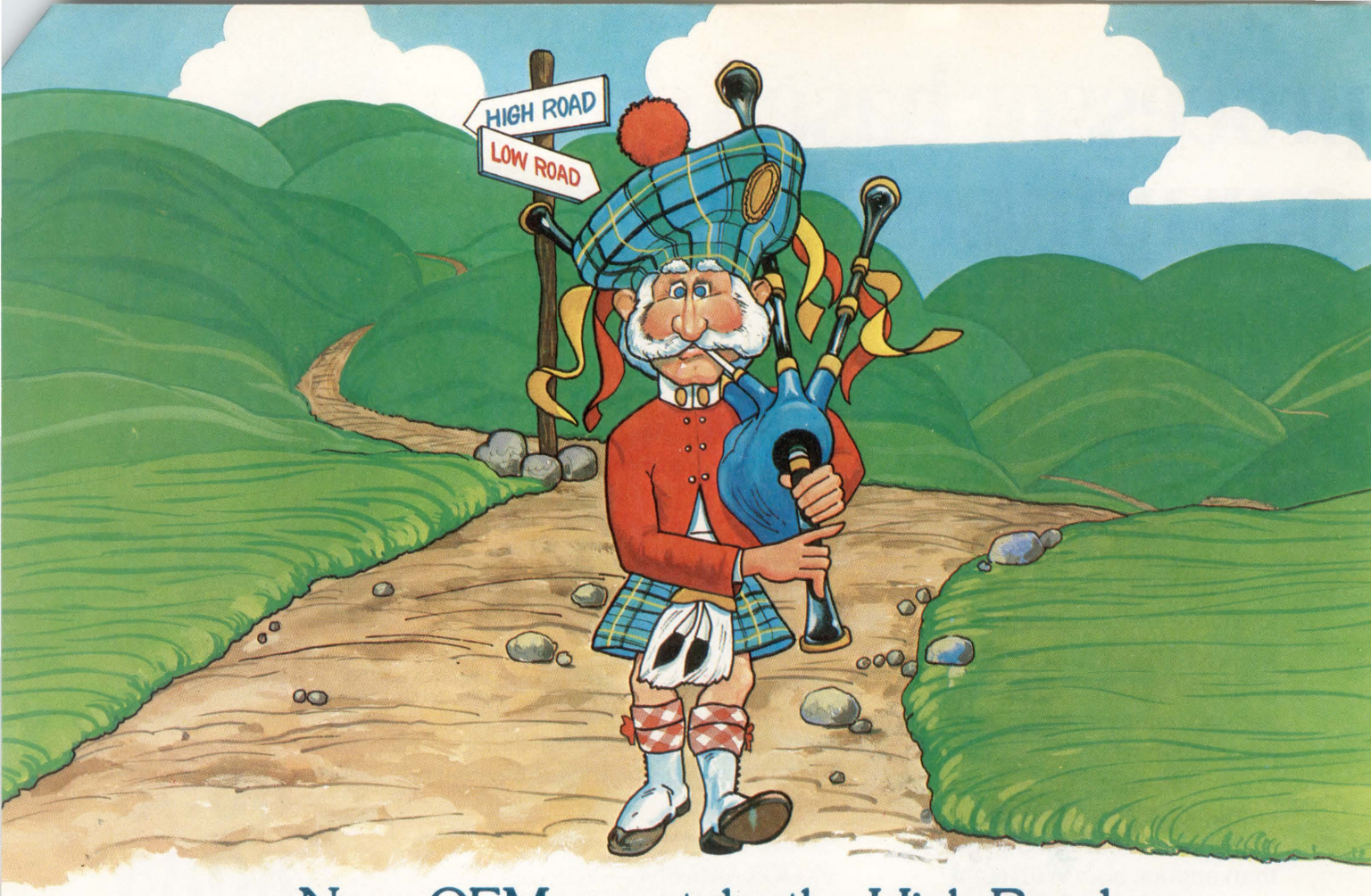
CIRCLE 16 ON INQUIRY CARD

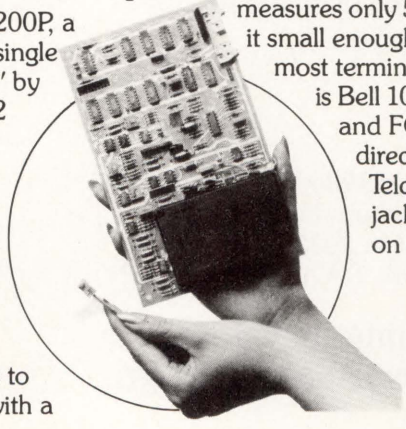


Now, OEMs can take the High Road or the Low Road with our Direct-Connect Modem Cards, small enough to mount inside Data Terminals.

As the auld Scottish tune suggests, Racal-Vadic now makes it easy for OEMs to take the high road (1200 bps) or the low road (300 bps), with low cost direct-connect "Modems-on-a-Card," small enough to mount inside CRT displays, teleprinters, POS devices, and other terminals and systems.

The High Road: 1200 bps

Meet the compact VS1200P, a complete modem on a single PC board measuring 5" by 8.35." That's a thrifty 42 square inches of space. It's fully compatible with Bell 202C and S modems. Only better, offering much more in performance, flexibility and test capability. It's registered for direct-connect, too. Connects to the switched network with a cable that plugs right into a Telco voice or data jack. Built-in 20 pin ribbon connector easily interfaces the VA1200P to your terminal. Price is right, too. Just $200 in quantities of 100.



The Low Road: 300 bps

The VS300P is a 300 bps full duplex, automatic originate/answer "Modem-on-a-Card." Like the VS1200P, it measures only 5" by 8.35," making it small enough to mount inside most terminals. The VS300P is Bell 103/113 compatible, and FCC Registered for direct connect via a Telco voice or data jack. Mounting holes on each corner make it a cinch to install. And the price would put a smile on the face of the thriftiest Scotsman. Just $200 in lots of 100.

Both Roads: The TI Story

Two of Texas Instruments new Silent 700* data terminals include Triple Modems custom made by Racal-Vadic. Although small enough to fit into TI's portable 17 pound terminal, this remarkable modem combines a Racal-Vadic VA3400, a Bell 212A, and a Bell 103. Imagine, a full originate/answer direct-connect modem with both 1200 bps full duplex and 300 bps full duplex in such a tiny package. And it can even be acoustically coupled.

We did it for TI, and we can do it for you. Phone or write today.

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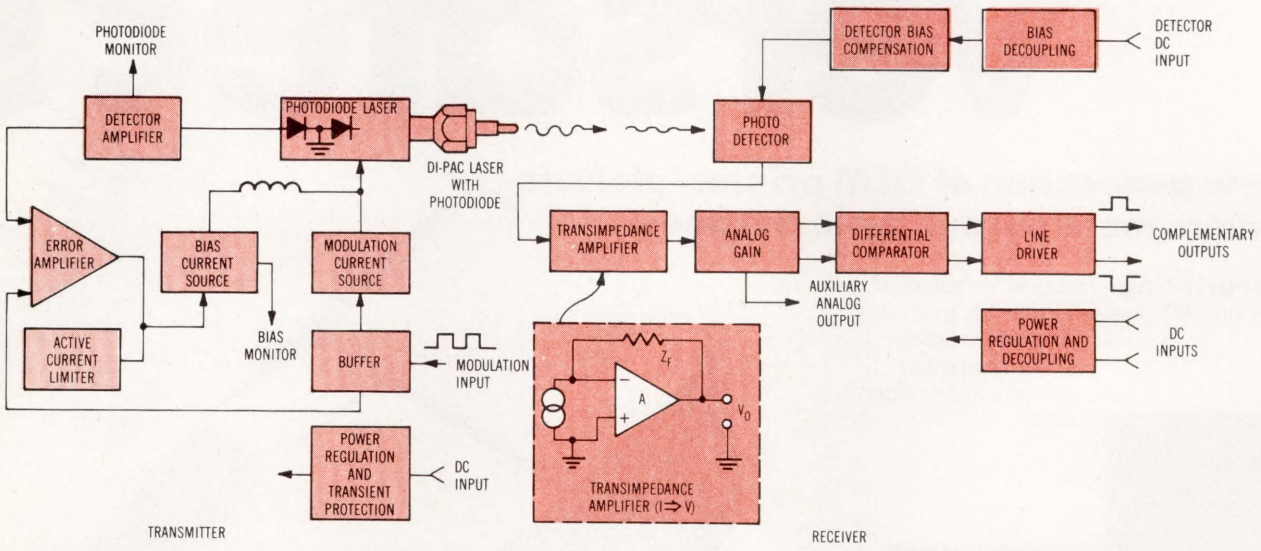
RACAL
The Electronics Group

CIRCLE 17 ON INQUIRY CARD

Transmitter/Receiver Sets Provide High Speed, Low Error Rate Data Over Long Fiber Optic Links



Combined block diagram of transmitter/receiver sets. Output signal from transmitter error amplifier automatically adjusts bias current to maintain constant laser baseline power. Auxiliary analog output in receiver provides for efficient clock recovery systems

Typical performance ratings of the 5100 series fiber optic transmitter and receiver modules include 0.1- to 150M-bit/s NRZ data rates and less than 10^{-9} bit error rate. Fiber optic link lengths, without repeaters, are up to 4 km using a PIN detector receiver, and up to 5 km with an APD receiver. These units are in standard production and are available from Optical Information Systems, 350 Executive Blvd, Elmsford, NY 10523. Transmission distances up to 12 km can be achieved at 50M bits/s, and longer distances if higher error rates can be tolerated.

Use of a laser rather than an LED light source is key to system performance. The transmitter is a feedback stabilized ECL compatible module usable to 275M bits/s NRZ. The company manufactured optical source is a double heterostructure AlGaAs diode laser chip mounted in a metal 14-pin DI-PAC™ DIP. More than 1-mW peak to peak modulated optical power is delivered to the end of an Amphenol 906 metal connector, which mates with a variety of commercially available fiber optic cables. An integral feedback photodiode detector mounted at the rear facet of the laser stabilizes laser output power. Rise and fall times are less than 1.5 ns; typical operating wavelength is 820 nm. Circuitry is on a low profile PC module that also contains transient protection and voltage regulation. Voltage requirements are ±12 to ±15 Vdc. Typical power consumption at ±12-Vdc operating power is 3.5 W.

The fully shielded wideband receiver modules are available with either a PIN or APD detector. Sensitivity of the PIN version at 150M bits/s is −21 dBm. Voltages required are ±12 to ±15 Vdc and 45 Vdc. Power consumption at ±12 Vdc is 2.2 W. The APD model sensitivity at 150M bits/s is −35 dBm; its voltage requirements are ±12 to ±15 Vdc and 300 Vdc. Typical power consumption at ±12 Vdc is 2.5 W. Full range temperature compensation stabilizes the gain of the APD receiver. Each receiver model has voltage regulation and detector bias decoupling. Complementary ECL outputs are provided at SMA connectors.

Both the transmitter and receiver are fabricated on 4.5 x 6.5 " (11.4 x 16.5-cm) PC cards that plug into standard 44-pin PC card connectors.

The 150M-bit/s data rate is compatible with the maximum required output rates of most data concentrating and formatting computers, whether multiplexed or not, used in interconnecting distributed computing or process control networks, as well as in telecommunications, satellite communications, and terrestrial microwave links. With fiber optics as the transmission medium, the error rate of the highest speed CPU to CPU, CPU to terminal, digitizer to CPU, or array processor/CPU/terminal/DMA link is immune to noise induced by EMI, atmospherics, ground loops, transients, and other electromagnetic or electrostatic disturbances.

Price for the transmitter/receiver pair with the PIN detector is $3250; with the APD detector, $3300. Delivery is stock to five weeks ARO.

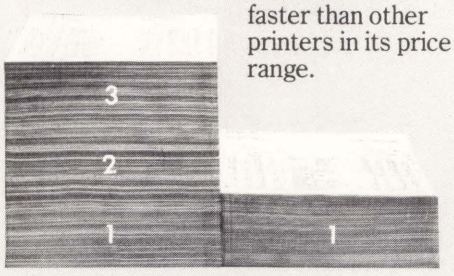
Circle 517 on Inquiry Card

(continued on page 31)

Output for Versatec's

A new generation of OEM printer/plotters delivers more output for less money.

Faster printing. The new Versatec V-80 prints 1000 lines per minute, more than three times faster than other printers in its price range.

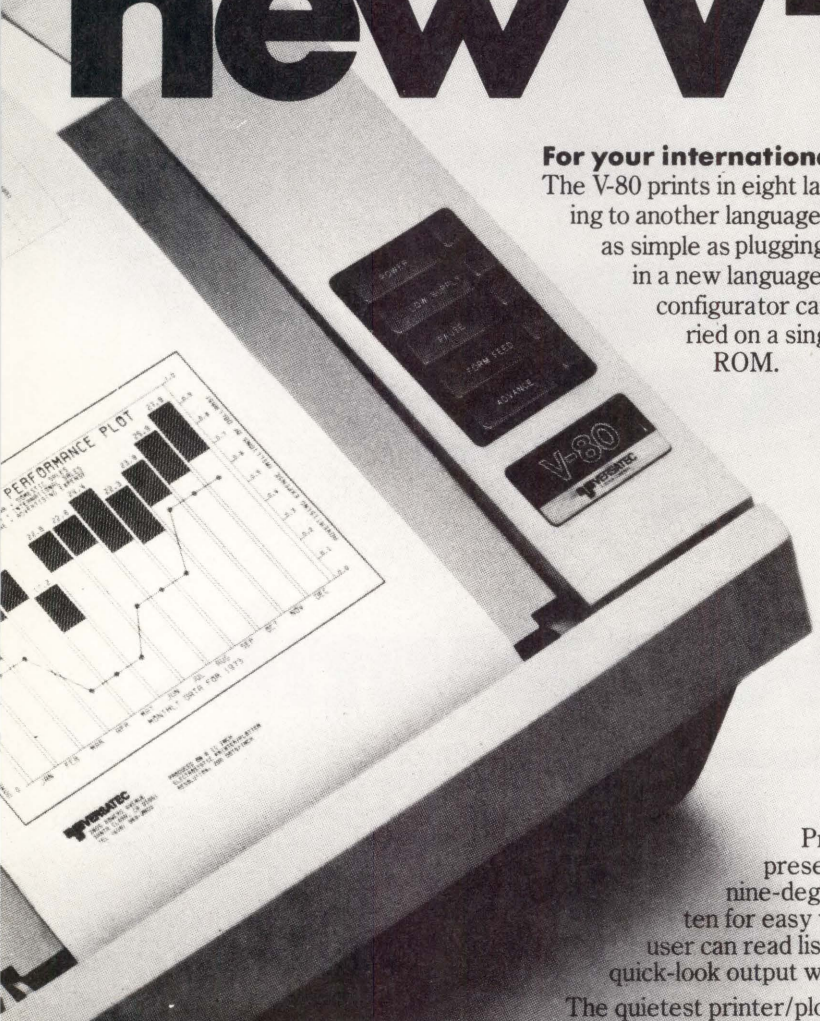


Graphics. The Versatec V-80 gives you better image quality than other printer/plotters. Get true high quality graphics with 200 dot per inch resolution. Plot an 11 by 8½-inch page in just seven seconds.

Hard copy from display. V-80, with an optional controller, makes quick, archival quality copies from storage tube displays or digital sources within twenty seconds.

Easy to integrate. Use V-80 with any popular computer. Styled to complement your computer-based system, the V-80 is suitable for any office or laboratory environment. The V-80 can be mounted directly into your system console, placed on a table, or be carried on its own optional utility stand. Weight is only 75 pounds.

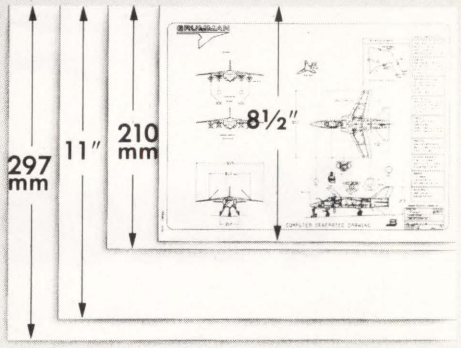
the 80's. new V-80.



For your international customers. The V-80 prints in eight languages. Changing to another language is as simple as plugging in a new language configurator carried on a single ROM.

The V-80 has been designed to meet both UL and VDE standards. Re-positioning one electrical plug adapts the printer/plotter to different voltage requirements.

Paper widths of standard 8½ and 11-inch *and* international A4 (210 millimeter "Portrait" and 297 millimeter "Landscape").



Easy to use. Printed output is presented on a nine-degree sloped platen for easy viewing. The user can read listings and other quick-look output without standing.

The quietest printer/plotter ever built, the V-80 makes no irritating clatter. Users can receive output even when talking on the telephone.

Changing toner is easier, faster and cleaner than changing typewriter ribbon. The disposable toner bottle inserts directly into the printer. No pouring. No mess. The toner is sealed away from hands and clothes.

Easy to maintain. Electrostatic writing is simple, because it's electronic rather than mechanical. Versatec has reduced mechanical part count to just 135, and that includes screws. Improvements in electronic design include microprocessor control, new LSI technology, and low power Schottky TTL logic. Fewer mechanical and electronic parts reduce spares requirements.

More profit. V-80 gives you better output specifications for less money. Excellent OEM margins assure more profit per system.

For more information, circle our readers' service number for the free brochure — "Output for the Eighties." To arrange a demonstration, call your local Versatec representative.

CIRCLE 18 ON INQUIRY CARD

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A XEROX COMPANY

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Telephone: (408) 988-2800
TWX: 910-338-0243

Versatec European Headquarters
27/35 London Road
Newbury, Berkshire, England
Telephone: (0635) 42421
Telex: 847259

Vincent van Dumb.

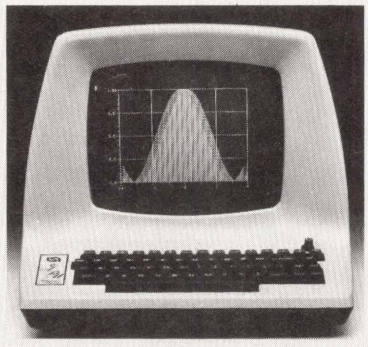
The Dumb Terminal® video display terminal has done it again.

For around $2000, you can have all the alphanumeric capabilities of the renowned ADM-3A Dumb Terminal, plus the full vector drawing and point plotting capabilities of a sophisticated graphics terminal. All in one neat package. That's less than half the cost of other comparably equipped graphics terminals.

The ADM-3A with Retro-Graphics™ gives you complete flexibility to develop bar charts, pie diagrams, histograms, even function plots. What's more, it's completely Tektronix® Plot 10™ software-compatible.

The package consists of an ADM-3A Dumb Terminal plus a single plug-in card engineered to fit neatly inside the ADM-3A without soldering, special tools, or a service call.

Retro-Graphics is a product of Digital Engineering, Inc., and is sold separately or installed in the ADM-3A by local Lear Siegler distributors. Contact the distributors listed below, any Lear Siegler sales office or Digital Engineering, Inc., 1775-C Tribute Road, Sacramento, CA 95815, 916/920-5600.



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LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

The Retro-Graphics-equipped Dumb Terminal. What does it mean to you?

Draw your own conclusions.

Lear Siegler, Inc./Data Products Division, 714 N. Brookhurst Street, Anaheim, CA 92803 800/854-3805. In California 714/774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices: • San Francisco 408/263-0506 • Los Angeles 213/454-9941 • Chicago 312/279-5250 • Houston 713/780-2585 • Philadelphia 215/245-1520 • New York 212/594-6762 • Boston 617/423-1510 • Washington, D.C. 301/459-1826 • England (04867) 80666.

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GPIB Bus Interface Reduced to a Few Chips

HMOS-II™ 8293 GPIB transceiver provides high current drive and interface required by the 1978 bus standard and replaces conventional bipolar TTL devices. Used with the company's GPIB component family 8291 talker/listener and 8292 controller, it provides a complete IEEE-488 interface that is a functional replacement for an entire board of electronics, according to Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. HMOS-II is a proprietary process for producing high performance MOS devices. The transceiver is the first application of this technology to a device that must provide high drive currents rather than high functional density. Using HMOS-II allows two transceivers with a total average power dissipation of 0.75 W to perform functions ordinarily requiring up to nine TTL bipolar devices dissipating up to 3.5 W.

Each transceiver chip contains nine line drivers and nine receivers. Each also has the bus line terminations required to meet the IEEE-488-1978 specifications. Receiver components needed to meet hysteresis (Schmitt-trigger) characteristics required by the standard and power-up and power-down protection are also built in.

Drivers can be configured as open collector or 3-state devices depending on programmed mode requirements. Each driver can sink 48 mA and can drive high capacitance loads at high speed. Propagation delays are less than 50 ns max. The transceiver operates from a single 5-Vdc power supply at typically 75- to 100-mA supply current. Bus power-down leakage current is 10 μA.

A pair of transceivers will directly connect the bus to a talker/listener, or to both a talker/listener and a controller for an economical bus control system. This flexibility is enabled by four programmable modes of the transceiver that reconfigure its internal circuitry so that it can function both in talker/listener and talker/listener/controller environments. Such interface systems have heretofore required up to 40 or more TTL bipolar devices, plus passive components such as resistor networks.

Circle 518 on Inquiry Card

(continued on page 32)

High Speed Network Designed For ATE Production-Test Environment

High speed intelligent 2291 GRnet™ data communications network is dedicated to the needs of the automatic test equipment (ATE) user. It is made up of three basic components: network interface module (NIM) that oversees the system's data communications functions; connecting hardware and cable; and data communications software. The system has been developed by GenRad Inc, 300 Baker Ave, Concord, MA 01742. The network provides a link to allow a GenRad 2290 multiuser programming station to communicate with any in-circuit or functional test system, or other programming station. All systems in the network can call for test files from central disc storage, eliminating the need for physical handling of discs and improving revision control of test programs. Programs can be loaded in less than a minute.

The Z80 based NIM interfaces the host system (2290) via a set of commonly mapped memory registers and transfers data to or from the host via direct memory access (DMA). NIMs are available for Digital Equipment Corp PDP-8A, -8E, -11/34, LSI-11/02, and -11/23 based test systems.

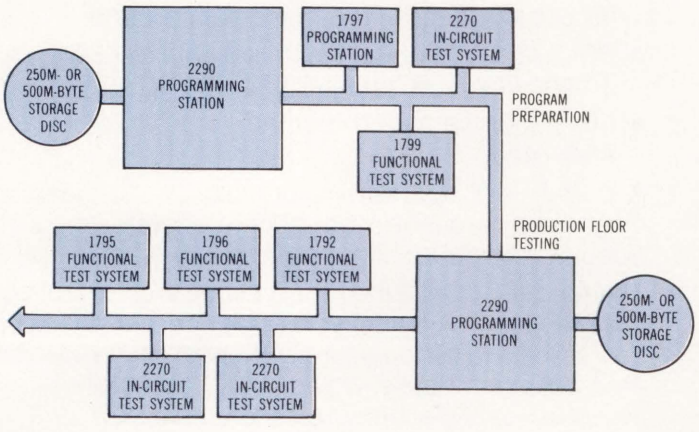
GRnet can drive a network up to 2000 ft (610 m) long. Transmission medium is a 93-Ω coaxial cable pair. In systems daisy-chained along the network, a single drop line is used for connection.

Software is virtually user-transparent and is invoked by means of keystroke commands from operator's keypads.

While raw data transfer rate can be up to 655k bits/s, typical throughput is approximately 40k bits/s. Up to four transfers can be executed simultaneously with minimal throughput degradation. Communications are managed by SDLC protocol, and use of cyclic redundancy check (CRC-16) assures data reliability, with errors corrected by retransmission. Data are transferred in packets, varying in size between 1k and 2k bytes.

The networking system can accommodate up to 64 systems on a single line. With a programming station functioning as host processor, all test systems have access to test files from central storage. Storage can be expanded to more than 500M bytes with the addition of two 250M-byte standalone disc drives. The programming station automatically sends requested test files directly to the production test system.

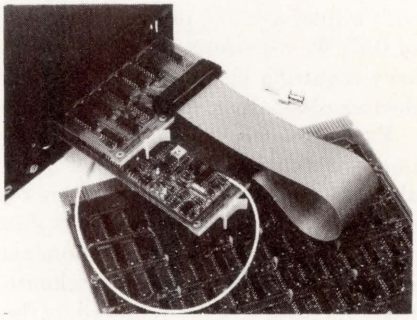
Circle 519 on Inquiry Card



ATE resource allocation using GRnet. System can typically transfer up to four 100k-byte files in about 20 s. Company says transfer of one such file would take 5 to 20 min at 9600-bit/s rate of other networks

Interface Provides 1M-Baud DMA Transfers Between PDP-11s

DMA block transfers between as many as 255 PDP-11 processors over a single coaxial cable at a 1M-baud rate are enabled by model 11-0016 Megalink Unibus™ compatible interface. Cable length depends upon type of coax used and can be up to 32,000 ft (9754 m). The interface, packaged on a standard 8.5 x 12″ (21.6 x 30.5-cm) quad-board that plugs directly into the PDP-11 backplane, is a product of Computrol Corp, 15 Ethan Allen Hwy, Ridgefield, CT 06877. The quad-board is cabled to a self-powered accessory module that holds the cable communications circuits, including a standard 1M-baud coaxial cable modem.



Model 11-0016 Megalink. Quad board is cabled to self-powered 3.62 x 13.25 x 11.56″ (9.2 x 33.7 x 29.4-cm) accessory module that contains cable communications circuitry

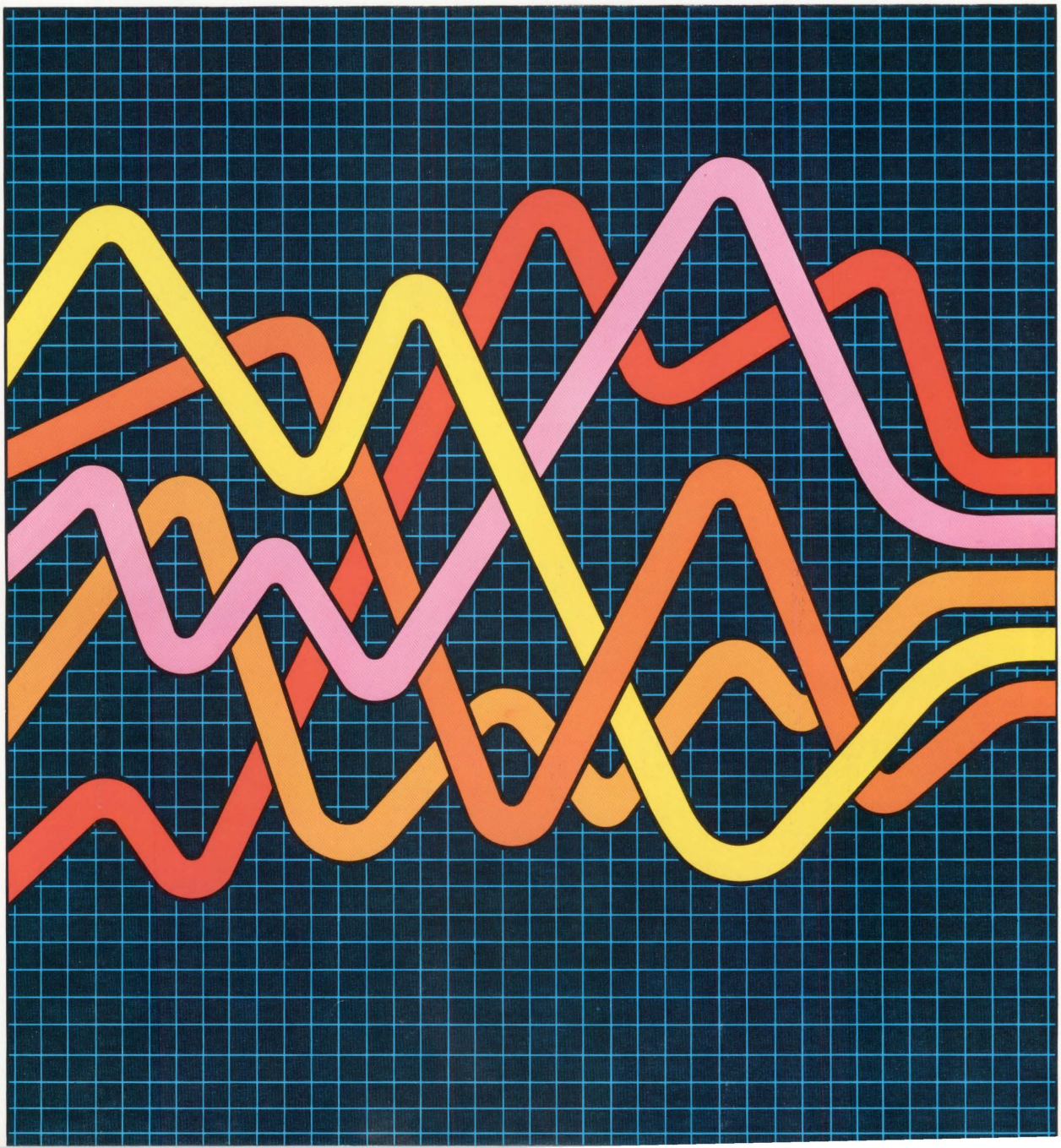
Wide dynamic range of the modem allows operation at any point on the coax without gain adjustments. Provision for carrier control enables single-cable half-duplex point to point and multidrop party line communications. SDLC protocol is implemented in hardware; protocol and control functions require no program intervention. CRC-16 error detection and recovery are provided by the protocol at primary and secondary stations. The computer can retransmit on error or request retransmission. Line connection is via a BNC T connector.

Since all the company's Megalink interfaces are compatible, local area coaxial networks of unlike processors such as PDP-11s, LSI-11s and iSBC/80s can be configured by using appropriate interface models.

Circle 520 on Inquiry Card

(continued on page 39)

What's the shortest distance between you and an intelligent data acquisition and control system?



The starting point: Our new A/D converters.

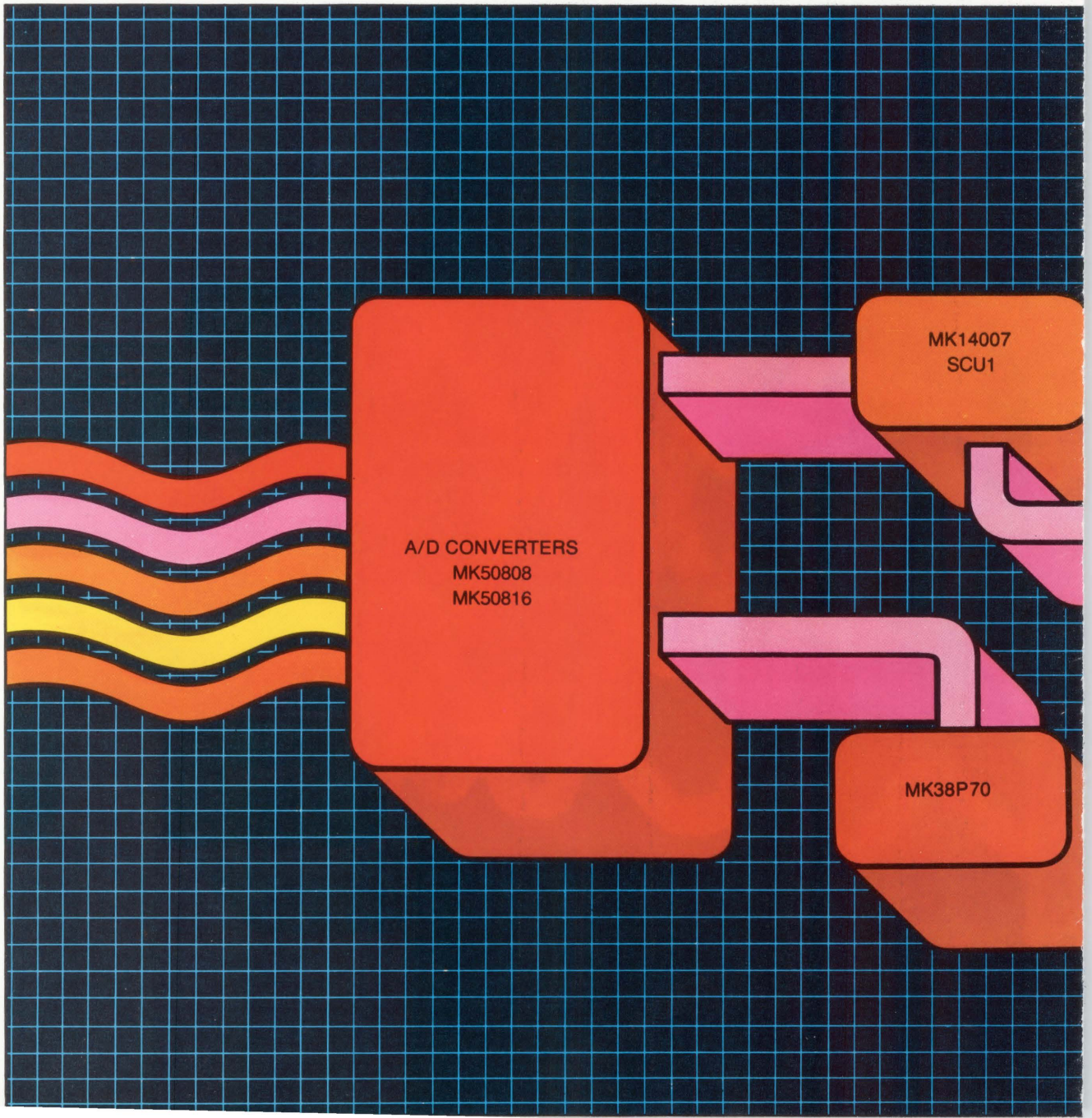
To convert the analog world to digital, use either of our new A/D converters. Both are CMOS devices requiring only a single +5 volt power supply. Power dissipation is a low 1.5mW typical.

The MK50808 is an 8-bit successive approximation A/D converter. This 28-pin device has microprocessor-compatible control logic and an 8-channel input analog multiplexer. The MK50816 A/D converter is a 40-pin circuit with the same logic as the MK50808, but features an expandable 16-channel analog multiplexer.

Both A/D converters use a series resistor ladder approach that guarantees monotonicity and no missing codes and allows both ratiometric and fixed-reference measurements. With these devices, external zero and full-scale adjustments are unnecessary and an absolute accuracy of ≤1LSB, including quantitizing error, is provided. Operating temperature range versions of 0° to +70°C or −40°C to +85°C are available.

Maximum conversion time for both converters is a fast 110 microseconds. They also feature latched TTL-compatible 3-state outputs with true bus-driving capability for direct interface to the host microprocessor. Conversion can be continuous or controlled, and either an external clock or the on-chip oscillator may be used.

Low power, minimal temperature dependence, and excellent long-term accuracy/repeatability make these



converters ideally suited for machine and industrial control applications.

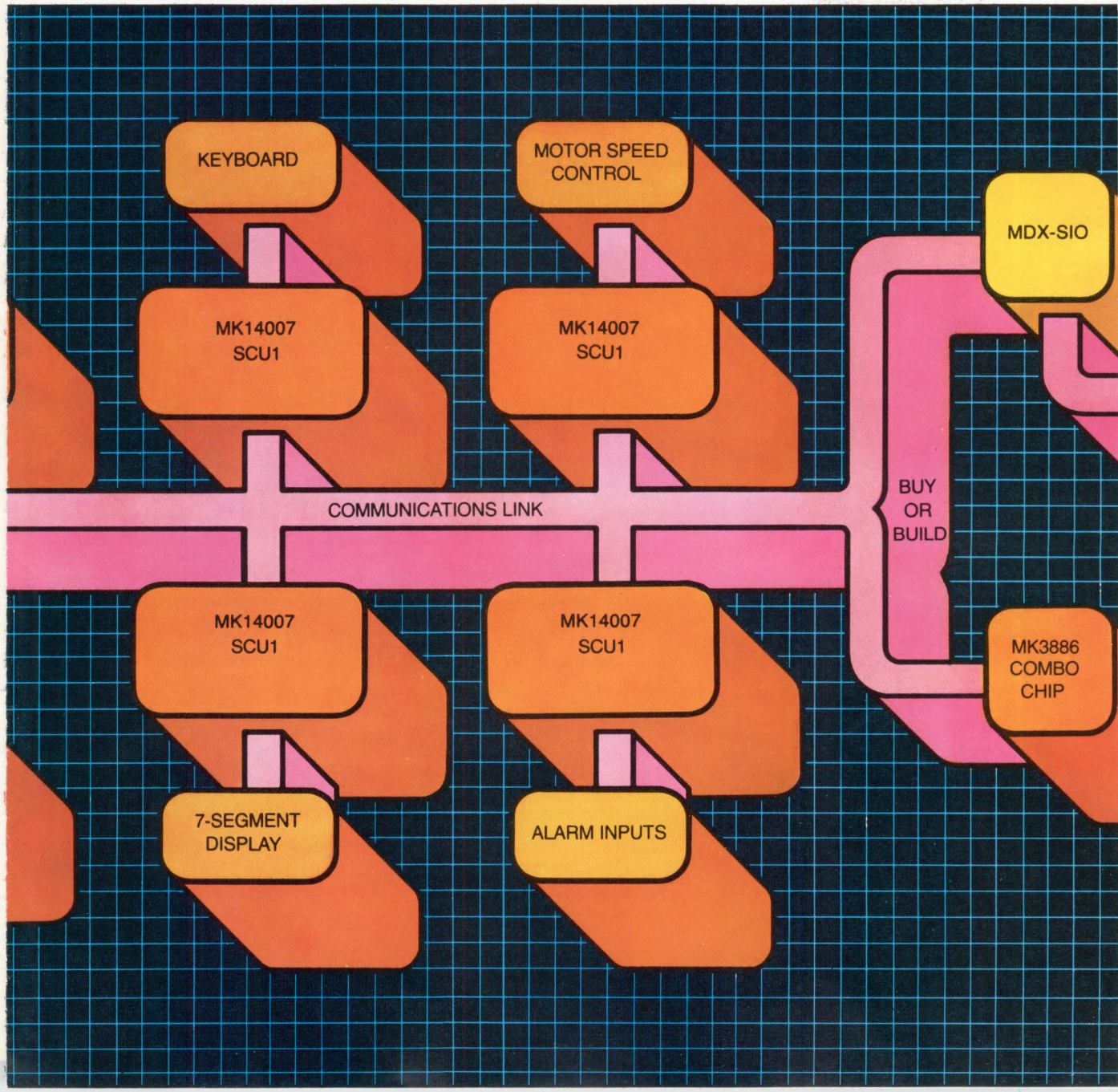
Make the connection with a new serial control unit.

Now that all the signals are digital, connect them to the new MK14007 SCU1™ serial control unit. Designed for both monitoring and control systems, this 40-pin circuit performs 19 pre-programmed I/O tasks received from a host computer via a half-duplex serial link. Commands include bit input and bit output; byte input and byte output; set, clear, and toggle selected pins; interface to A/D or D/A converters or to a 3½ digit digital panel meter (with data outputs); and monitor input pins for a specific bit pattern.

The SCU1 also provides for programmable remote I/O functions through its 16 I/O pins. The chip contains a complete communications processor capable of generating and receiving messages. Results of commands executed can be echoed back to the host computer.

You can use, and individually address, up to 255 SCUs in your network using only a single communications channel. Handshaking pins allow it to interface to the central controller over twisted pair lines, R.F. communications link, modems, or fiber optic cable. Plus error-resistant data link protocol. Power is a low 275mW (typ.), and the SCU1 requires only a single +5 volt power supply.

Low cost and easy implementation make the SCU1 an



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excellent choice for microprocessor-based, distributed processing systems where remote intelligence is required.

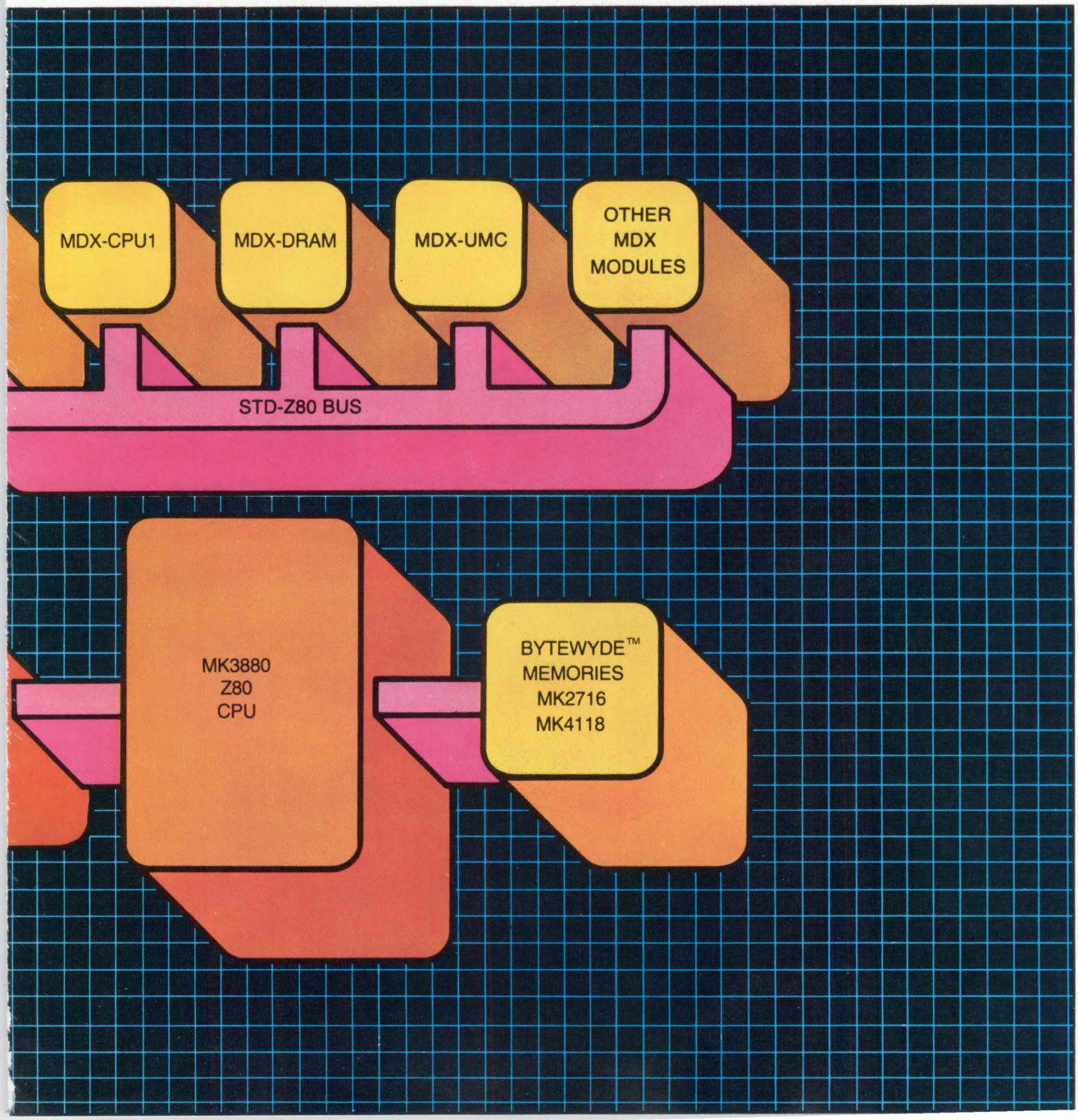
Cross the finish line with your choice of Z80-based controllers.

Next, run your communications link back to your control system. Build that control system one of two ways.

Buy the Mostek MD Series of STD-Z80 BUS expandable microcomputer boards. Based on the Z80 microprocessor, this compact board series has fully assembled, fully debugged and fully warranted hardware. Plus comprehensive software support highlighted by the Matrix™ development system.

Or, if it's cost-effective, design your own control system using our MK3880 family of Z80 microcomputers. Then configure a simple and upward compatible memory array with our family of BYTEWYDE memories.

Whatever way you go, all the components, including the A/D converters and the SCU1, are available now from your Mostek distributor.



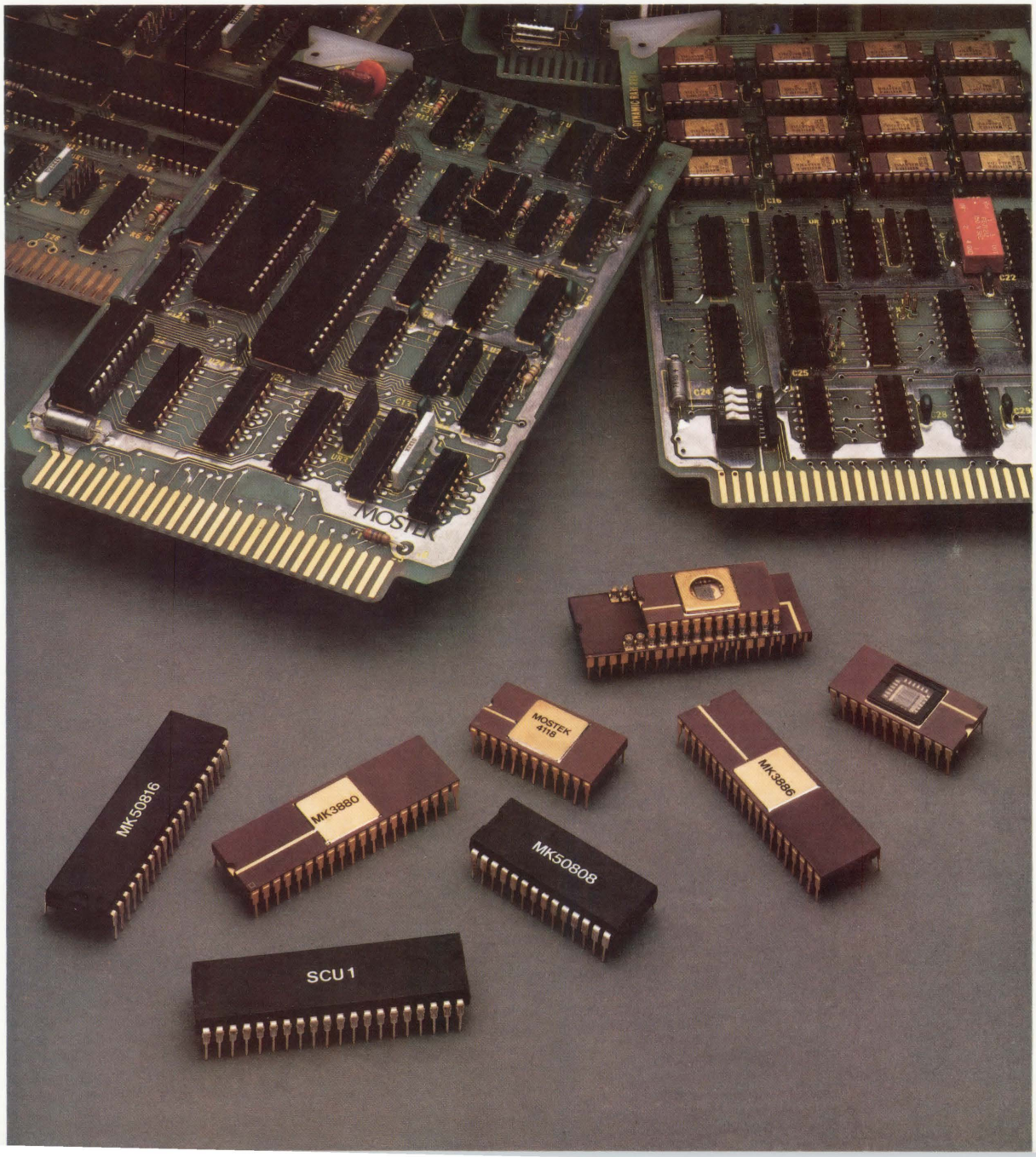
A complete line from a single-source: Mostek.

Now you only need one source to design intelligent, microprocessor-based real-time data acquisition and control systems. Mostek can supply you with all of it: A new line of A/D converters. Intelligent remote controllers. A choice of Z80*-based control systems to back it up. And, of course, complete development systems to speed up your design cycle.

To configure your system, start with any of our new A/D converters. Next, interface them to our microprocessors. For a stand-alone system, use the MK38P70 single-chip microcomputer with a piggyback EPROM. For larger systems, interface the A/D converter to our new serial control unit, SCU1. Then run your communications link back to your central processor. To build it, use our broad line of Z80 components and BYTEWYDE™ memories. Or choose from our MD Series™ microcomputer modules to quickly configure your system controller.

Now develop and debug the software with our Matrix™ Series of hardware and software microcomputer development systems. After this task is completed, use your Matrix system as a network controller if required. For multi-tasking operations, specify the MITE-80/BIOS™ software package to speed up implementation.

The result? Easy to design systems that are flexible, yet powerful.



Hardware, Software Products Implement Local Area Network

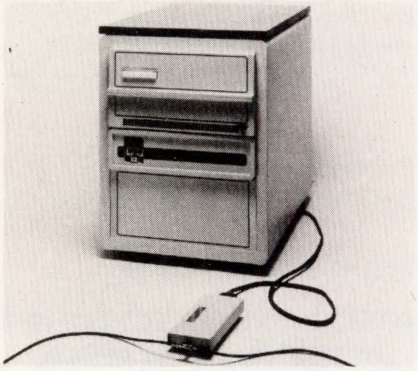
Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014, has announced three products that permit full implementation of Z-Net, an expandable local computer network for multiuser business and specialized data interconnect applications. This is phase two of a 3-part introduction of systems products that started with announcement of the MCZ-2 line of small business computers (*Computer Design*, July 1980, p 140). The third announcement, coming later this year, will introduce a multiprocessor feature for enlarging network capabilities.

SDS 2/01 shared data station is a 10M-byte cartridge disc subsystem that has a dedicated processor (Z80A and 64k bytes of memory) and shared data manager software. The station is packaged in a 30" (76.2-cm) high rack.

NST 2/01 network station transceiver is packaged in a 10.75 x 4.8 x 15" (27.3 x 12.2 x 3.8-cm) box for wall mounting. A 25-ft (7.6-m) cable is provided for connection to a small business computer or shared data station.

Network Protocol Software is a collection of layered software modules that facilitate communications across the network. The software runs on a computer or shared data station.

The Z-Net architecture concept is based on a single-channel packet-switched local computer network with fully distributed control. Both the small business computers and shared data stations can serve as nodes or stations in the network. Nodes are linked by a cable TV-type coaxial line, and each station is connected to the network through a transceiver unit and a passive BNC T connector. Stations may tap into or out of the network without affecting operation of any other station. System software allows these hardware elements to operate together as an integrated network.



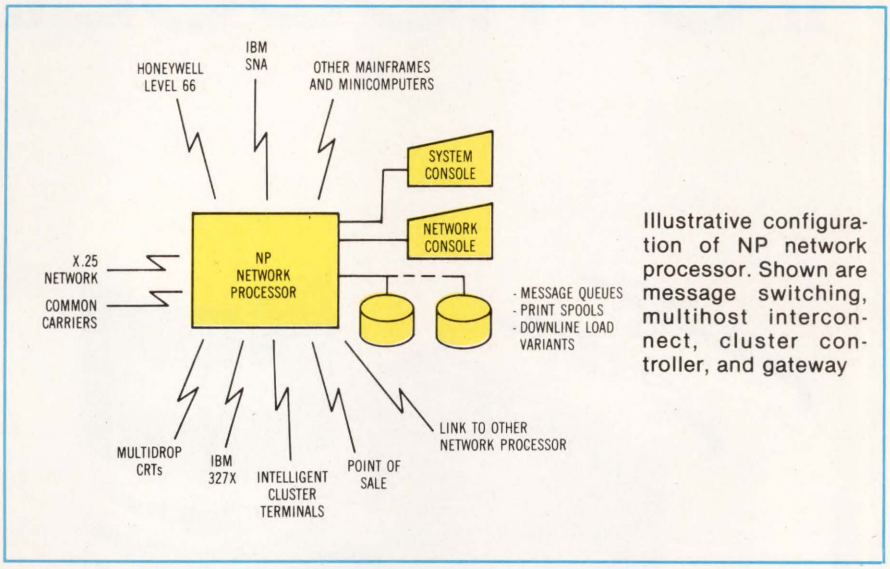
Z-Net local network elements. SDS 2/01 shared data station connected to coaxial link via T tap and NST 2/01 network station transceiver

Transmission facilities of Z-Net can support a network of up to 255 stations of either computer or shared data stations, which can be deployed along the network in any combination, at sites wherever needed, over a total cable length of 2 km. Transmission speed is up to 800k bits/s.

The shared data station provides a common data base for the small computer stations along the network. Each has a 10M-byte base storage capacity that can be expanded to 40M bytes in 10M-byte increments, each of which is half fixed, half removable cartridge. Shared data manager software within the data station is a hierarchical multiuser file system with record level locking and unlocking, and multiple volume capability across the full 40M-byte range.

Circle 521 on Inquiry Card

Variety of Configurations Handled by Network Processor



Illustrative configuration of NP network processor. Shown are message switching, multihost interconnect, cluster controller, and gateway

Network Processor NP, based on a Honeywell Level 6 minicomputer, can be configured to perform as a remote concentrator, cluster controller, message switch, and node of a centralized or distributed network. The processor also allows offloading multiple host communications and data processing functions.

The NP, developed by Advanced Computer Techniques Corp, 437 Madison Ave, New York, NY 10022, is based on Honeywell L6 hardware and GCOS software, using multiline communications processors (MCLPs) that handle up to 96 communication lines per processor. The system can support several hundred terminals and printers on multi-drop lines, BSC 2780/3780, and Bunker Ramo systems.

Product architecture permits use of L6 supported asynchronous, synchronous, polled, nonpolled, and packet protocols, including X.25, HDLC, VIP7X00, TTY, and PVE. HASP, HIS level 66 remote batch facility (RBF), and IBM 2780/3780 terminal utilities handle file transfer functions.

The processor provides message routing based on logical destination, station address, or message header. Local disc storage accommodates message transactions queuing. Online network reconfiguration capability allows for increased network availability. Other features include audit trail of operator modifications and journaling on disc of errors for offline network operations analysis.

Circle 522 on Inquiry Card

The new way to ease the pain of microprocessor interfacing.

CRYDOM BUFFERED I/O MODULES!

These are the new high performance interface switches for electrically clean, photo-isolated (4000V RMS min.), noise-free interfacing between CMOS or NMOS microprocessors or TTL and any other logic-based controllers and the associated devices in your new system.

The Crydom Touch.
Physically and electrically equivalent and pin compatible with older versions offered by other manufacturers, the new Crydom Series 6 Input/Output modules offer several advantages the others can't provide.

Higher Output Current.
All Crydom output modules can control loads up to 3.5 Amps @ 45°C as compared to 3 Amps (or less) for the others. A larger heat spreader, thinner case walls and optimum thermal conductivity encapsulating epoxy enable ours to dissipate heat faster and run cooler, permitting greater current handling capability.

Buffering: The big design advantage.
The others' output modules require special add-on, external buffering circuits to reduce the input drive requirements to a level suitable for microprocessor MOS devices. The Crydom Touch has eliminated this often painful exercise. Buffering is built into selected output modules to reduce your design time and production costs. And you'll end up with an uncluttered control assembly.

Better protection against circuit noise.
A hysteresis factor of 30% provides added protection by blocking out most transient signals. The others don't offer this feature.

A Broad Line.
There is a Crydom Series 6 model to match every AC and DC Input or Output module offered by the others, plus inverting and non-inverting buffered output modules they can't supply. Mounting boards for up to 24 modules are available. Send for our new catalog, and put the Crydom Touch into your new system!

Series 6 I/O Modules are available at competitive prices from Crydom Distributors everywhere!

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COMMUNICATION CHANNEL

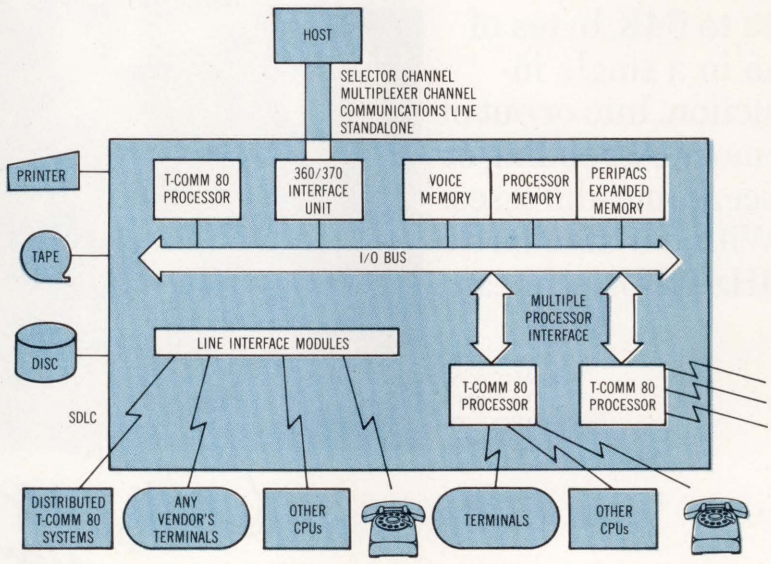
Networking Concept Provides Variety of Functions

A modular building block architecture enables networking concept T-COMM 80 to be configured as an intelligent node, frontend processor, or standalone transaction processing system for data communications, voice response, or multifunction networks. The entire line of products that comprise the concept features a common hardware and software technology, integrated to maximize system performance. The networking concept has been developed by Periphonics Corp, 75 Orville Dr, Bohemia, NY 11716. Its versatility derives from a range of micro and minicomputers (LSI-11, PDP-11/04, -11/23, and -11/34). Processing power can be increased by grouping multiple processor interfaces (MPIs) in a single system, and memory size can be augmented by using the PERIPACS^{R} extended memory management system.

A data communications network can be configured by choosing terminal and host computer interfaces available from a library of more than 40 such devices. A single network can handle any mix of terminals and hosts, and enables communication in multivendor networks. Intervention, processing, and programming support for network control and diagnostic and error correcting services are self contained and offloaded from host computers.

Communications control software supports such capabilities as communications with up to seven host processors from each network system via channel level or communications ports. Messages can be switched to different destinations without host processor intervention, and primary or alternate hosts for each terminal can be assigned to any network node.

Use of the company's VOICEPAC 2000^{R} adds voice response capability and provides a choice of voice output messages from a master vocabulary of more than 1200 recorded words and phrases. Dialogues are controlled by the networking system or the host. Data are entered using a telephone keypad in response to voice prompting. The multifunction network combines data communications and voice response within the same, or separate networking systems. □



T-COMM 80 system. Any mix of asynchronous, synchronous, or SDLC terminals plus voice response lines present common interface and access method to host. Multiple processor interface provides high speed channel level interface among processors. Multiprocessor configurations function as single system while providing load and task sharing among up to four processors

Circle 523 on Inquiry Card

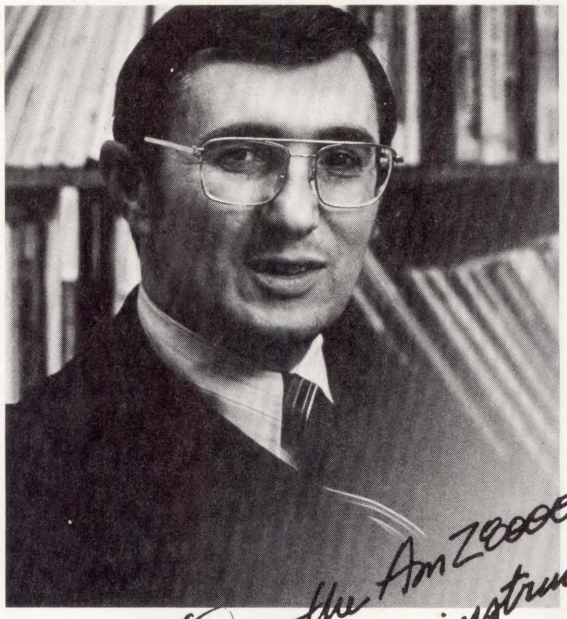
You're designing an intelligent CRT terminal and you're looking for the best 16-bit CPU for your application.

Congratulations. Your search is over.

"The AmZ8000 is better at handling strings of characters or data words."

The AmZ8000 has special block I/O instructions that allow you to move from 1 byte to 64K bytes of data in a single instruction. Into or out of memory. Ascending or descending addresses.

With our standard 4MHz CPUs, you can move a data item every 2.5 μsec. And you can interrupt the instruction to take care of other business.



Rick McCarthy
Manager,
Field Applications,
Engineering

Only the AmZ8000 offers string instructions for exceptionally efficient I/O.

"The AmZ8000 has a better development system."

Our System 8/8 was designed especially for the AmZ8000.

It comes with 64K bytes of RAM, dual double-density floppy disks, an optional cartridge disk and piles of software. It's Multibus* compatible. And it's even got an optional in-circuit emulator that runs in real time: 4MHz. No wait states.

"The AmZ8000 is better for intelligent CRT terminals."

"The AmZ8000 has a better macroassembler."

The MACRO8000 has powerful macro and conditional assembly capabilities. And it generates relocatable output for either of the AmZ8000 CPUs.

For even more efficient programming, we'll soon be offering C, a powerful system implementation language, as well as PASCAL.

"The AmZ8000 is better because our peripherals are better."

Advanced Micro Devices has a whole family of peripherals to go with the AmZ8000. For example, we've got DMA channel controllers and interrupt controllers and all kinds of high-speed, high-drive bipolar support circuits. We even have a powerful new linked-list CRT controller on the way.

And there's more: The AmZ8000's general-register architecture and efficient instruction set give you high throughput for sophisticated displays. The CPU directly addresses up to 8M bytes of memory. And we are still the only company that processes every part to the rigorous requirements of MIL-STD-883. For free.

If you're looking for a 16-bit CPU for your intelligent CRT terminal, look into the AmZ8000. It's available right now.

And it's the best 16-bit family for you.

*Multibus is a trademark of Intel Corp.

Advanced Micro Devices

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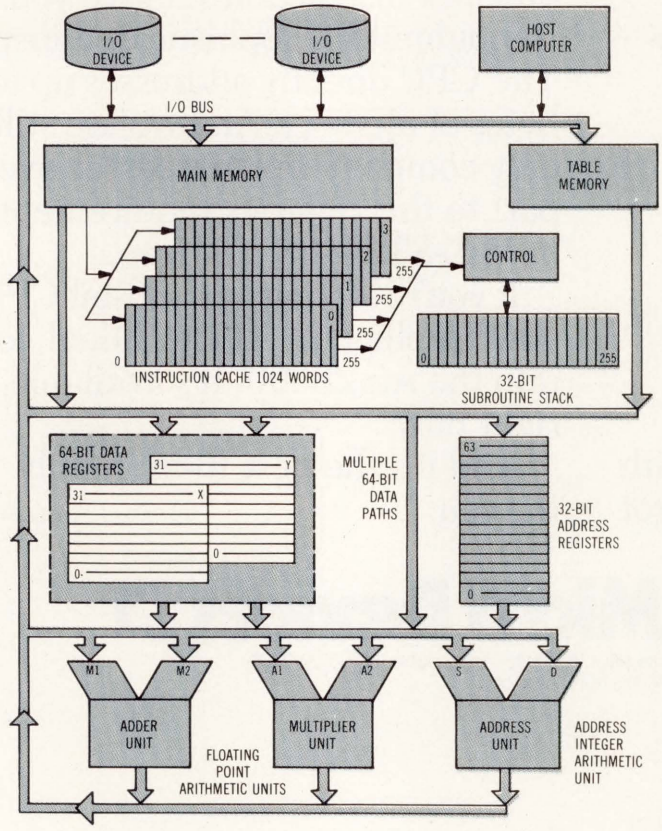
Right, from the start.

CIRCLE 22 ON INQUIRY CARD

TECHNOLOGY REVIEW

Attached Processor Handles Large Scale Scientific Computing Applications



Floating Point Systems' array processor FPS-164 combines 64-bit computation with large memory addressing. With host maintaining overall control, unit executes computationally intensive portion of application in parallel with host

High speed 64-bit computation and large memory addressing provided by the FPS-164 attached processor fill demands for access to large volumes of data and extended floating point precision. Attaching to a DEC VAX-11/780 or IBM 3033 or 4341 host processor, the high speed machine from Floating Point Systems, Inc, PO Box 23489, Portland, OR 97233, features internally synchronous operation of multiple independent parallel data paths, separate memories, and multiple pipelined arithmetic units.

The processor provides a maximum of 12M floating point operations/s, plus a concurrent maximum of 6M integer/address operations/s. Its precision exceeds 15 decimal digits through 64-bit floating point arithmetic. Main memory, based on 16k memory chips, expands to 1.5M 64-bit words (12M bytes). Large programs and associated data sets can reside in main memory which can expand to a maximum of 48M bytes. The 24-bit address allows direct addressing of 16M words. An instruction cache is interposed between main memory and the control element and serves as an instruction buffer. Four independent 256-word (64-bit) regions are filled from main memory. A 1k-word ROM contains the operating system and utility primitives.

Machine architecture features internally synchronous operation of multiple independent parallel data paths, separate memories, and multiple pipelined arithmetic units. Parallel organization allows array indexing, loop counting, and memory access functions to be performed simultaneously with arithmetic operations on the data. The 64-bit instruction word can control 10 or more simultaneous synchronous operations during any one instruction cycle.

Four separate banks of operating registers supply operands to arithmetic and logic units and store intermediate results from them. Each arithmetic element can produce one result per machine cycle (167 ns).

The I/O subsystem consists of a synchronous bus for transfer of programs, data, address, and control instructions between processor and external devices. This system contains I/O bus, I/O port, host interface, and I/O device adapters. Computational efficiency is achieved through the parallel nature of internal data paths. Separate 64-bit paths are provided to each of the two inputs to the floating point adder and multiplier pipelines, allowing data from any processor element to move to the arithmetic units in a single instruction cycle. In addition to the six dedicated arithmetic data paths, there is a seventh path connecting most functional elements of the processor. Because arithmetic elements can receive input from any of several sources, routines run at a high percentage of the available maximum rate.

Diagnostic and reliability features of the machine include a diagnostic microprocessor system which has a diagnostic bus connection to major system elements. This unit performs three levels of fault isolation: functional unit, board level, and diagnostic microprocessor and floppy disc faults. Confidence tests verify correct operation of hardware/software components by executing system subroutines from a normal host job.

Support for the system is provided by runtime system software, program development software, and application software. Executing on the host, development software includes a FORTRAN compiler, assembler, linker, interactive debugger, and interactive simulator.

Circle 420 on Inquiry Card

(continued on page 48)

ROLM's New ARTS Is A Fast Real-Time System. With WCS, It's Even Faster.

ROLM's Mil-Spec ECLIPSE® Computers now have a software/hardware combination that zeroes in on today's tough, real-time military applications.

The total package is fast, compact, and configurable. A real-time operating system designed for both time-critical and hostile environments.

ARTS (Advanced Real-Time System) expands the performance range of our Mil-Spec ECLIPSE line of computers by adding true real-time multiprogramming, multitasking capability. WCS (Writable Control Store) provides the additional hardware to access our microprogrammed processor and increase throughput for high-speed applications.

As a compatible subset to Data General's AOS (Advanced Operating System), ARTS is loaded with outstanding real-time features. It's configurable and

modular, providing memory support from 64KB to 2048KB. ARTS can be memory-only or disk-based, depending on the needs of the application. Other features include: high order language support, (FORTRAN 5, PL/I, DG/L™ system programming language), memory resident file structure, and efficient interprocess communications.

The optional hardware part of the package, WCS, maximizes the computing power of our Mil-Spec ECLIPSE processors. And at the same time, it minimizes the critical path execution time for high-speed functions or processes. In time-critical operations, specialized functions can be tailored precisely to the application.

ROLM's Mil-Spec ECLIPSE Computers with ARTS and WCS give military system designers the optimum system. It solves today's real-time problems... with tomorrow's technology.

That's Why We're #1 in Mil-Spec Computer Systems

ROLM MIL-SPEC Computers

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(408) 988-2900. TWX 910-338-7350.

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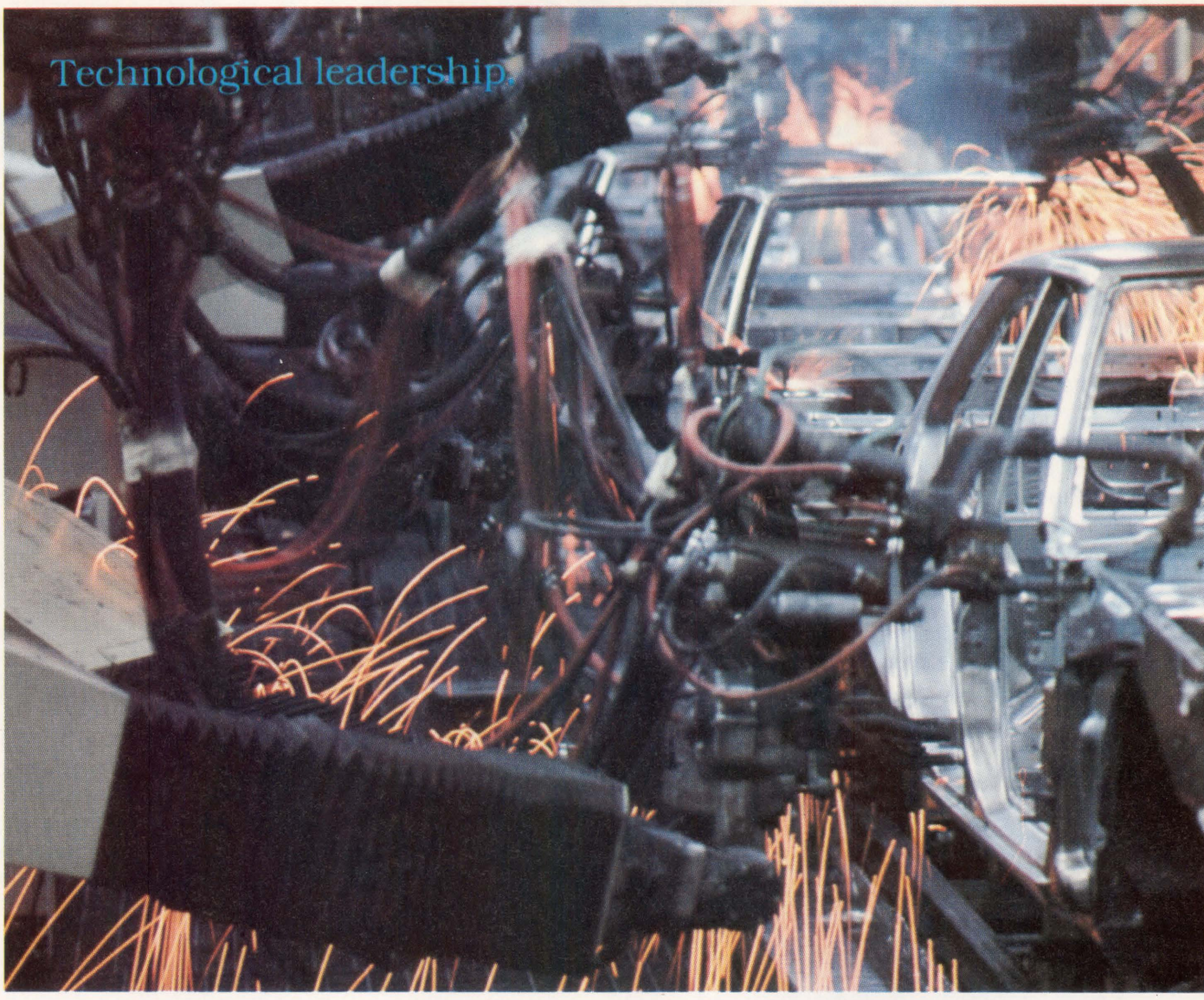


Drive directly off logic with the noise-immune I/O modules.

Motorola introduces the first, industry-standard family of Input/Output modules to connect right up to any logic system/MPU port/microcomputer without any external buffering or noise-immunity circuitry whatsoever.

Easy and versatile-to-use, the series incorporates all necessary components within itself to offer state-of-the-art capability and performance in the heavy industrial control area.

Besides buffering and noise-immunity, each module contains signal conditioning, isolation, logic interface, power handling and status indication when used in MS4-24 series boards.

High, 200 kΩ input impedance provides compatibility with microamp drive current levels of CMOS and NMOS devices. The ability to operate from a wide 3.3 to 26.5 V logic supply range means you can use the same modules with all logic families including bipolar. And, they're compatible with older, non-buffered, standard types.

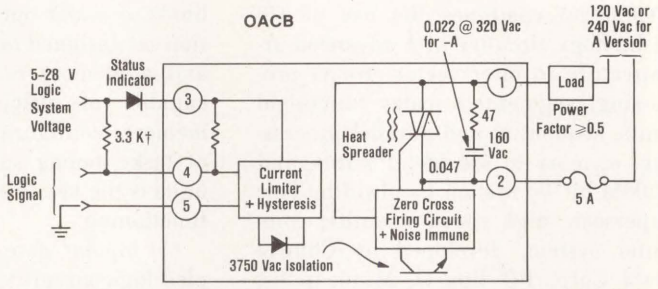
Once the I/O module gets the message from logic or MPU, it can control up to 3 A, 60 Vdc or 3 A, 240 Vac in the outside world to control fractional hp motors, small heaters, solenoids, lamps, contactors, timers, starter and relay coils.

All Motorola I/O modules utilize high-quality opto couplers tested to 7.5 kV peak. This ruggedness makes our units rated at 3,750 $V_{(RMS)}$ isolation, meeting European VDE and IEC demands as well as UL specs. They also meet IEEE noise-immunity spec 472-1974 (common mode) making them virtually impervious to high industrial noise problems.

ARNOLD ZANN, BLACKSTAR

Ability to withstand MIL shake, rattle and roll plus 100% testing attains the highest degree of integrity and user confidence.

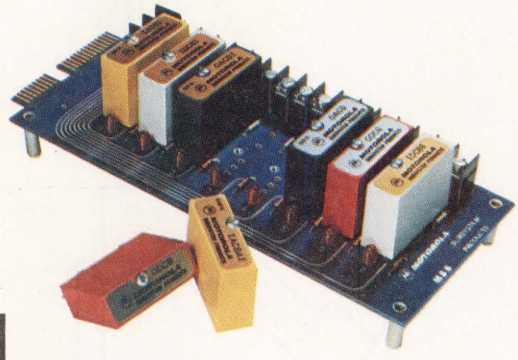
Using our 4 to 24 module, socketed mounting board, you can interface an entire system with standard minis like PDP-11, Supernova and Motorola and Intel micros . . . install them in standard NEMA enclosures . . . and remove or



†Resistor is pull-up for open-collector drive. Typical valueshown is supplied on standard MS (Mounting System) boards. For CMOS applications replace with 56 k.

Case Color	120 Vac Devices		240 Vac Devices		DC Devices	
	Standard	Noise Immune	Standard	Noise Immune	Standard	Noise Immune
Yellow	IACB	IACBI	IACBA	IACBAI		
White					IDCB	IDCBI
Black	OACB	OACBI	OACBA	OACBAI		
Red					ODCB	—

PDP-11 is a trademark of Digital Equipment Corporation.



first fully-buffered Even in places like this.

They're made well, too. Covered footprints prevent bowing of terminals and ensure dimensional consistency and positioning stability. Void-free, vibration- and moisture-resistant potting has withstood billions of hours of automotive environments. Single-cycle surge rating of 80 A provides 2 to 3 times the protection offered by some others. Base standoffs eliminate unit/board contact reducing component thermal stress and contaminant collection. Heat spreaders ensure even thermal gradients, efficient cooling and inherently higher performance at any temperature.

Conformal coating of PC boards raises reliability and breakdown voltage and absorbs shocks. UL-flame retardant resin will not track under the most demanding high-voltage/humidity conditions.

replace modules without disturbing wiring. You remain outside the card cage of most MPU structures with safety and convenience.

Contact Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036 for data. We're the place to come to for

Innovative systems through silicon.

MOTOROLA INC.

CIRCLE 24 ON INQUIRY CARD

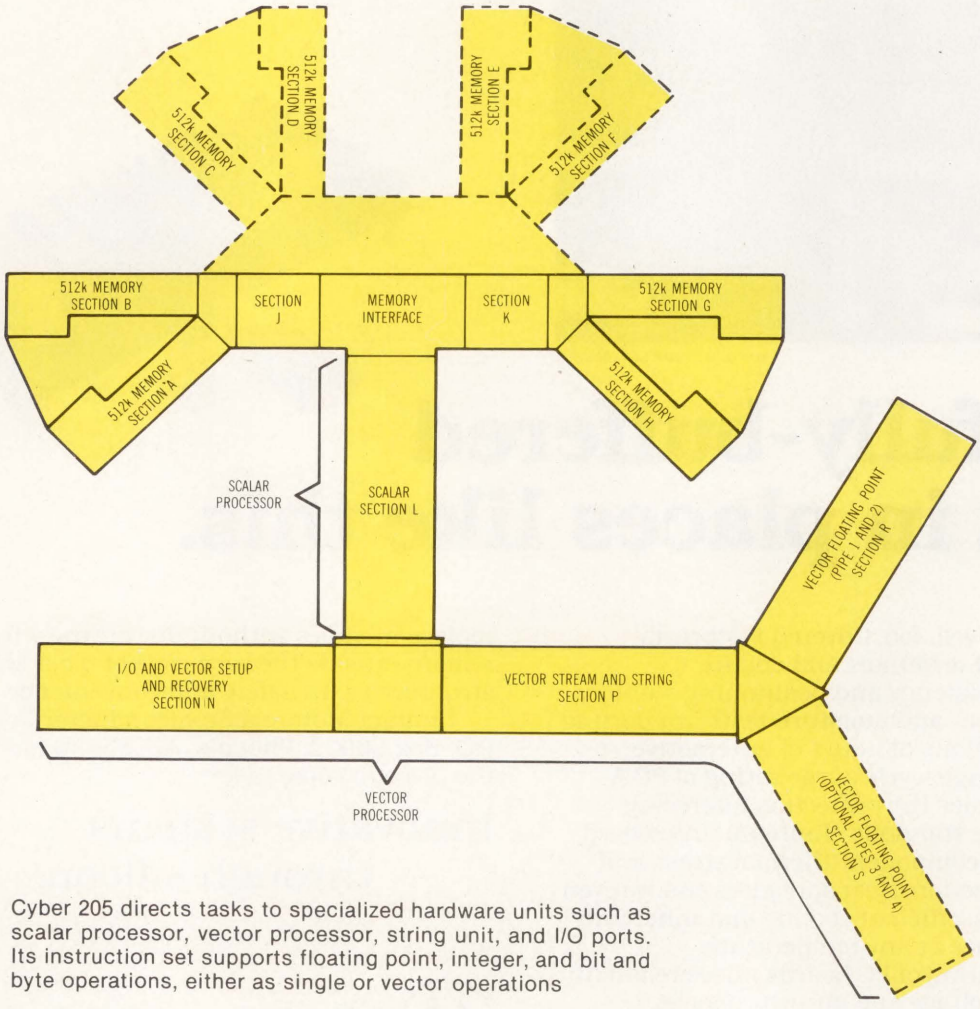
Supercomputer Incorporates Both Scalar and Vector Processors

CYBER 205 combines the use of LSI technology circuitry with advanced architecture to offer vector stream processing, segmented scalar functional units, sequential and parallel processing, memory to 4M 64-bit words, and 3200M-bit I/O system bandwidth. This superscale high speed scientific computer system, developed by Control Data Corp, PO Box O, Minneapolis, MN 55440, yields a performance factor of up to 4 to 1 more than its nearest competitor and matches the need for 3-dimensional processing of the volumes of data associated with petroleum exploration and structural analysis as well as that required for accurate 24-h weather forecasts.

Architecture of the system provides high performance scalar operations, vector processing extended beyond the limits of scalar operations, an instruction set designed for vector processing, and a memory management scheme capable of efficient use of large memory configurations. Distribution of tasks among specialized hardware units is the key to speed and economic functioning.

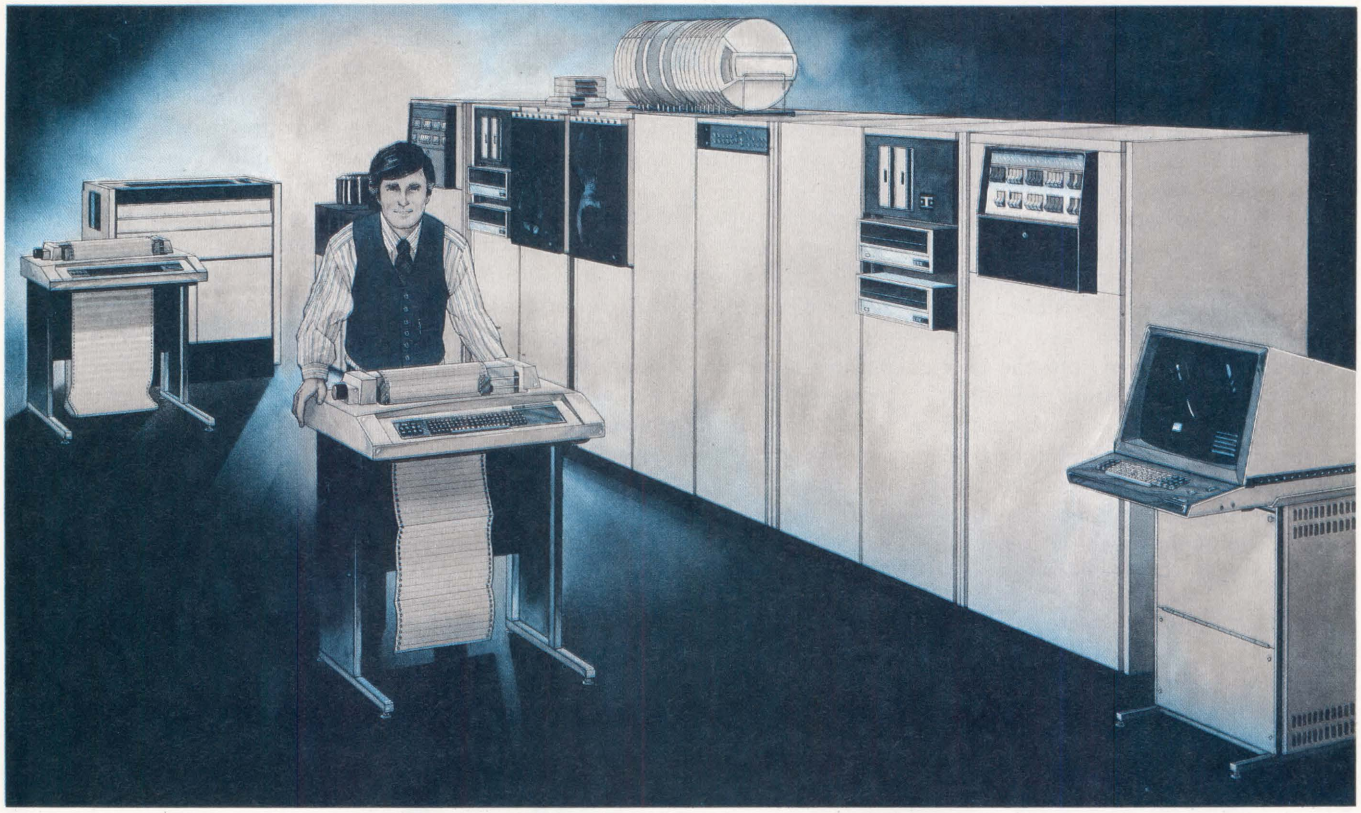
LSI bipolar gate array emitter coupled logic circuitry is used throughout the CPU. High density packaging (168 gates/chip) results in subnanosecond switching because of fast circuit switch time and reduced distance between switches. Only 29 different chip types are used in the CPU; each is a plug-in module that is easily replaceable. A direct heat transfer technique places a cold surface beneath each chip to assure low stable junction temperature, extending circuit life when compared with conventional air or edge cooling.

The single processor system executes instructions that are issued in conventional sequential fashion. Each instruction, however, is executed by parallel operations in either the scalar or vector unit. The scalar unit performs a single operation per instruction, which can be issued every clock cycle (20 ns) or up to 50M instructions/s. This unit decodes all



Cyber 205 directs tasks to specialized hardware units such as scalar processor, vector processor, string unit, and I/O ports. Its instruction set supports floating point, integer, and bit and byte operations, either as single or vector operations

Avco is THE systems house that can offer a turn-key, custom designed measurement and control system worldwide.



When you come to Avco, you're dealing with a single source supplier for computer-based measurement and control systems. From specification and design to installation and training, Avco professionals work with you to develop the optimum system built to your individual requirements.

Avco begins with application engineering. We study the problem and help you define the system requirements. We then select the hardware. Or we can manufacture any needed component in our 125,000 square foot Huntsville plant.

Component interface is an Avco specialty. Our engineers carefully integrate sensors, field panels and central stations to achieve a system that delivers trouble-free performance right from turn-up.

Software optimization is critical to the effectiveness of any measurement and control system. Avco programmers work with you to develop the software that will generate the exact data you need to get the job done.

Avco has designed, built, delivered, and installed some of the **most sophisticated distributed network systems** ever created, such as the world's largest and fastest real-time computer data acquisition network system and the world's largest machinery health monitoring system. Avco has also designed the world's largest industrial test system, utilizing over 100 computers in a four-level hierarchical network, for the leading U.S. manufacturer of diesel engines, and the world's largest energy management system designed to tri-service specifications.

But Avco also builds the best small systems — computer-based electrical power demand and load control systems, automated data acquisition systems and process control systems — all offering reliable performance at competitive prices.

All Avco systems are carefully tested for quality assurance and conformance to customer specification. We supervise the entire installation and start-up sequence. We even train your operators.

And Avco **field service** is always right at hand. Your investment is protected by our highly skilled technical service staff. We can be anywhere in the world whenever you need us.

Avco. The strength and assurance of a $2 billion corporation. The flexibility and technical support of a leader in system electronics. Find out why major corporations around the country are turning to us. Write or call today for more information. Telephone: (205) 837-6500.

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CIRCLE 25 ON INQUIRY CARD

instructions and directs vector instructions to proceed independently to the vector processor for execution. The unit operates with a 64-word instruction stack and a 256-word register file that allows rapid processing by minimizing accesses to memory.

The vector unit performs arithmetic operations on arrays or streams of data with a single instruction, using both 32- and 64-bit operands. Consisting of one, two, or four segmented pipelines, the vector processor performs portions of specific operations in steps. This segmentation allows a new set of operands to be moved into the first stage of the pipeline during each 20-ns clock cycle, providing a result rate of up to 200M (64-bit) operands/s. A triadic linkage instruction can be used to double this rate in some applications. When 64-bit precision is not required, use of 32-bit half-word produces twice as many vector results per clock cycle.

Central memory is comprised of up to 4M 64-bit words. A single level random access memory using 4k bipolar ECL circuits, central memory ranges to 32M bytes. Each 0.5M words contains 16 memory stacks arranged in 8 phased banks. Data transfers to and from the CPU occur at speeds up to 25.6G bits/s for each 1M-word memory increment. The system's virtual memory addressing technique uses hardware to map from the 2 x 10^{12} word/user address space to central memory.

Eight I/O ports each 32-bits wide are standard. Each can transfer up to 200M bits/s, providing capacity for incorporation of higher performance secondary storage devices as they become available. Memory bandwidth permits all 16 I/O ports to achieve maximum transfer rate concurrently while supporting maximum vector processing rates. One port is used by the maintenance control unit which handles error processing, online and offline diagnostics, and downloading of peripheral processors.

Circle 421 on Inquiry Card

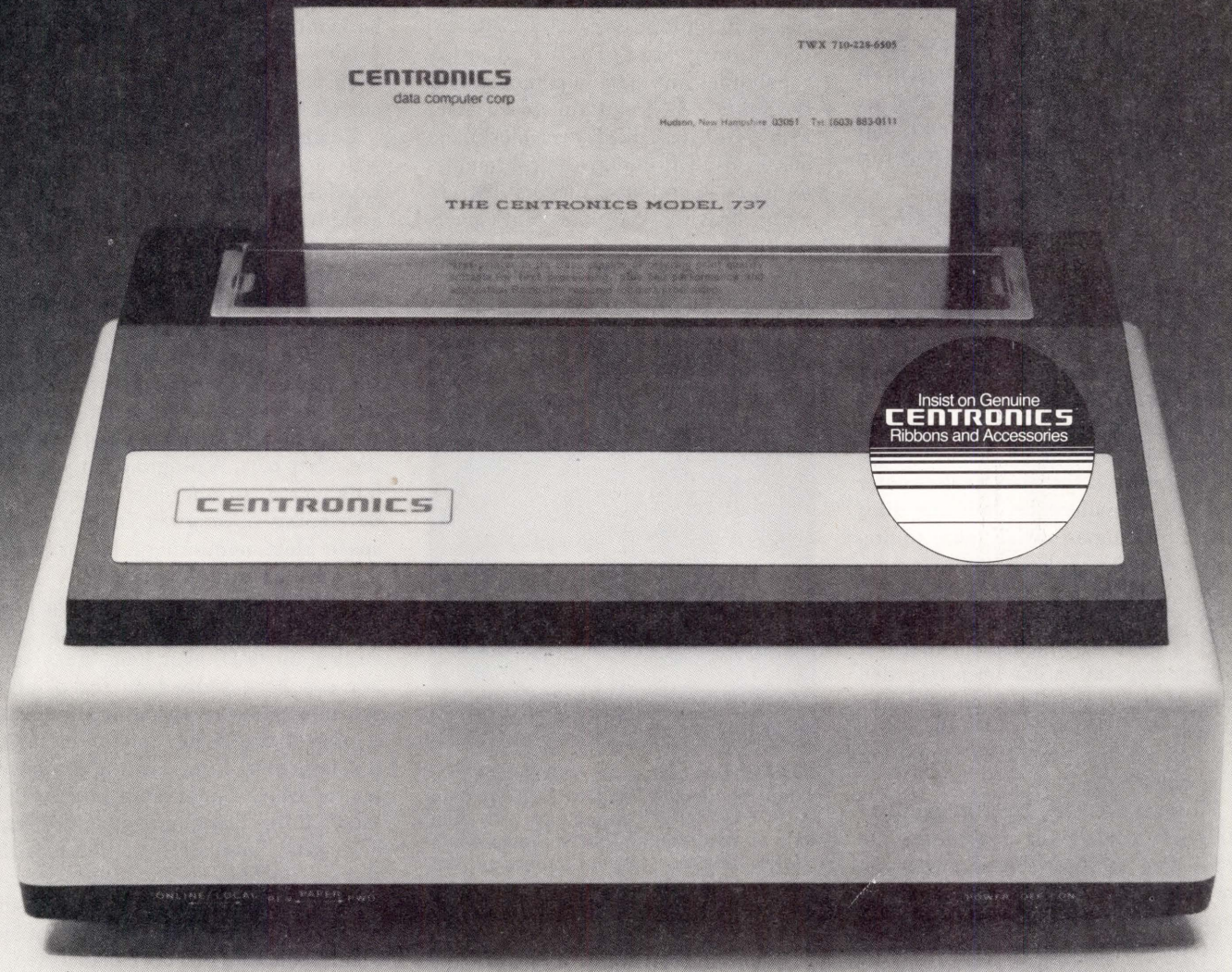
Paginated Glass Discs Being Developed for Digital Optical Recording

Increasing demand for information is stimulating research and development efforts on systems capable of recording massive amounts of data in a compact form. This in turn requires development of a recording medium capable of carrying this volume of information.

Developments in this field are underway at Philips Research Laboratories, Eindhoven, The Netherlands. While still in the experimental stage, a compact digital optical recorder using a semiconductor laser has been produced. This unit can write the equivalent of 0.5M pages of text on a disc the size of a long playing record and can retrieve any desired page within 0.25 s.

The necessary density of data on the recording surface requires that extreme accuracy be obtained in directing the fine beam of laser light onto the sensitive layer of the disc. To record, the 0.001-mm diameter beam of light flashes on and off, burning

CENTRONICS MODEL 737: The Advantage for Low Cost Word and Data Processing



The flexibility and print quality OEMs need is here now. The new Model 737 is the small business printer versatile and reliable enough to meet almost any systems requirement. It's the first low-cost printer to offer print quality suitable for text processing plus the performance and applications flexibility required for data processing and electronic mail. And this latest Centronics breakthrough is priced under $1000 in the U.S.A.

Outstanding Print Quality

Model 737 is the first small business printer to offer correspondence quality printing. 18 x 9 dot matrix provides high-quality characters with true descenders as well as underlining. Proportional spacing, the ability to justify right margins and serif typeface makes the 737 ideal for text processing applications. Standard business data processing spacing of 10 and 16.7 characters per inch are also resident in the 737, allowing for applications ranging from letters to aged accounts receivable reports. The steel platen assures crisp, clean print impression.

Unexpected Features

Leave it to Centronics to have some surprises in the new Model 737. You get the ability to print subscripts and superscripts. Especially attractive to OEMs requiring superior print appearance and/or chemical or mathematical applications. Centronics gives you its field proven 700 Series printhead, stepper motor paper drive, fewer moving parts, microprocessor electronics and high volume production to achieve reliability that you wouldn't expect in a compact, low-cost printer.

The 737 is quiet. An optional acoustic cover makes it ideal for office environments.

Pick Your Paper

Run letterhead paper for correspondence, roll paper for general information, or fan-fold paper for standard data processing (payroll, billing, inventory, etc.). You can, with the 3-way paper handling ability of the Model 737.

The Printer of the Future . . . Today

Never before has one printer offered such high quality, reliability, and applications flexibility at such low cost.

Another workhorse in the Centronics 700 Series is the 730, if you don't need the correspondence quality of the 737. Delivers 100 c.p.s. at even greater savings.

Why Wait?

The new Model 737 is now available for delivery. For more information: call (603) 883-0111, or contact any of our 15 U.S.A. or 9 international sales offices. Centronics Data Computer Corporation, Hudson, New Hampshire 03051.

All Centronics products are supported by the largest worldwide service network of any independent printer company.

CENTRONICS® PRINTERS
. . . the advantage

CIRCLE 27 ON INQUIRY CARD

microscopic pits in the sensitive layer to form coded data. The precision of the system demands that no dust or other impurity be present and that there be no unevenness in the sensitive layer.

Discs for use with the recorders are being manufactured on a laboratory scale and are made of two layers of tempered glass that is impermeable to moisture. These glass discs are placed on either side of a transparent pregrooved or paginated lacquer layer and a sensitive layer composed of a material based on the element tellurium. Two metal spacer rings, placed between the discs at the center and the circumference, hold the discs apart, creating a boxlike space to prevent oxidation of the sensitive layer.

The pregrooved layer is made by flowing a transparent lacquer over a casting mold in which the pattern of pits for pagination has been recorded and placing a glass disc onto it. The lacquer is hardened and adhered to the glass disc by the action of ultraviolet light.

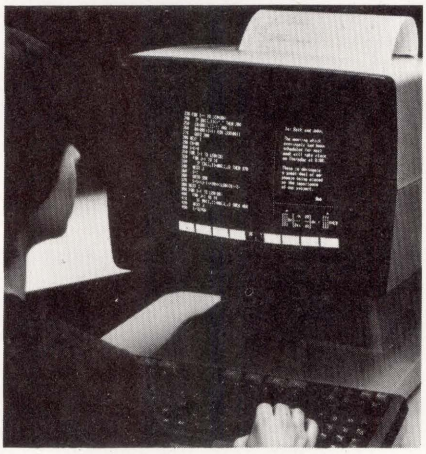
To form the even layer of sensitive material needed for recording, the glass disc is passed into a vacuum enclosure in which tellurium is vaporized and deposited on the disc in a very thin layer. The silver-colored tellurium reflects 60% of the laser light falling on it, allowing the prerecorded data to be read out as the differences in reflection between pits and flat surface.

Circle 422 on Inquiry Card

Data Entry Terminal Offers Multiwindow Display And Dual I/O Ports

HP2626A display station enables users to divide both display memory and display screen into as many as four independent work areas. Bringing together data entry and program development capabilities, the unit combines individual workspaces with dual data communications ports to permit users to display data from two different computers or from two different sessions on the same computer.

The teleprinter compatible terminal, developed by the Data Terminals Div of Hewlett-Packard Co, 19400 Homestead Rd, Cupertino, CA 95014, as the top of its "smart" line, uses the company's proprietary SOS CMOS LSI technology to provide display capabilities and data communications flexibility. A 16-bit microprocessor with 32k-bytes display memory and 80k bytes of firmware control handles terminal operations. Custom LSI circuits provide multiple workspace, multiple window, dual data communication port, and horizontal scrolling capabilities.



Multiwindow display of workspaces provided by Hewlett-Packard's 2626A data entry terminal in conjunction with dual data communication ports allows users to view data from two computers or from two separate sessions on same computer

Power and flexibility of the terminal are made easy to use by screen labeled function keys that allow forms to be created interactively and terminal configuration to be done using menu selection. User operation may be simplified by specifying operation through screen labeled user keys and providing audible cues. These capabilities may be applied to provide high performance data entry systems over low speed lines, to increase programming productivity, and to implement advanced office applications.

Lines for the four workspaces contained in the terminal can be set from 80 to 160 char, allowing 132-col reports and double-width pages to be handled as easily as single-width pages. Total length of workspaces can vary as long as the total line count is within the terminal's capacity.

Separate areas on the display screen (windows) view contents of memory workspaces. The screen may be divided into two vertical segments and as many as four horizontal segments; four windows may be on the screen at one time. Data may be scrolled both horizontally and vertically within a window to view all data within a workspace; size of the window may be changed via the keyboard.

Combination of workspaces, screen windows, and data communications capabilities offers the user data entry and program development advantages. A single window attached to multiple workspaces allows an operator keying data into one workspace to transmit data from another to the host computer. The terminal can be used to simultaneously receive and print data from one computer while an operator enters data to another computer via the other port. A programmer can use both ports to the same computer, developing a program in one workspace while monitoring a job or printing a listing with the other.

User definable soft keys may be programmed with a sequence of keystrokes up to 80 char long. Each soft key can be described on the display screen with a corresponding label consisting of two 8-char lines. Via these function keys, forms can be designed interactively. Capabilities within the sketch forms function include drawing horizontal and vertical lines with single-, double-, or bold line definitions. In addition, margin frame and data frame functions are included. Fields, edit, and display enhancements are also defined via the function keys.

An optional built-in thermal printer can reproduce dot for dot the display on the screen. It, therefore, can duplicate line drawings, math and special language symbols, and large characters. The printer has a compressed print mode that can copy 132-col lines on the 8.5″ (21.6-cm) wide paper. Expanded mode produces double-size characters.

A basic display station offers operation in block line, line modify, and character modes. Data communications capabilities handle hardwired, full duplex, half duplex, or multipoint asynchronous or synchronous operation. The unit connects to any TTY port using ASCII. Two RS-232 ports are standard; 20-mA current loop is optional. Data rates range from 110 to 9600 baud. List price is $3950; the optional printer adds $1150.

Circle 423 on Inquiry Card

(continued on page 56)

THE DATA I/O SYSTEM 19 PROGRAMMER: SAVES ENGINEERS TIME. SAVES DEVELOPMENT SYSTEM TIME.

Data I/O's System 19 Programmer frees your microprocessor development system for more important tasks. Here's an example:

An engineer is building six prototypes for a new microprocessor based product. If each unit has eight 2708 PROMs, it will take more than an hour to program those 48 PROMs—one at a time—on the development system.

That's time and money wasted.

Instead of tying up the development system to program PROMs, the engineer could simply down load the information into the System 19's RAM and free the development system for more creative tasks.

That's time and money saved.

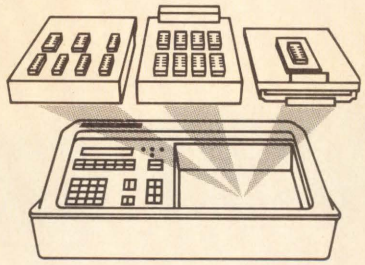
System 19 interfaces more easily with more development systems than any other programmer, and accommodates 16 bit microprocessor data too! System 19 is intelligent. It can communicate using RS232C or 20mA current loop with a variety of formats without the need for intermediaries like paper tape.

And Data I/O makes interfacing easy because we supply application notes explaining exactly how to do it.

System 19 can transmit and receive data formatted in: Binary, DEC Binary, ASCII-BNPF, ASCII-BFLF, ASCII-B10F, 5-level BNPF, Spectrum, ASCII-Hex, ASCII Octal, RCA Cosmac, Fairchild Fairbug, MOS Technology, Motorola Exorciser, Intel Intellec 8/MDS, Signetics Absolute Object and Tektronix Hexadecimal.

System 19 is a valuable editing tool. Instead of waiting for development system time to refine a program, an engineer can also edit the program using the System 19 keyboard.

The System 19 modular concept keeps it state of the art. The System 19 is designed around a standard mainframe and plug-in modules:



—UniPak: a single, seven socket module that programs more than 200 different bipolar and MOS PROMs and gives you design and purchasing freedom for evaluating new devices and developing second sources.

—Individual PROM Programming Paks: for generic PROM families.

—Individual Logic Programming Paks: for devices such as FPLAs and PALs.

—Gang Module: programs up to eight MOS devices at once.

Let us show you the future. The Data I/O System 19 is available now. To make arrangements for a demonstration or to get your free copy of this valuable 32-page book, circle reader service number or contact Data I/O, P.O. Box 308, Issaquah, WA 98027. Phone 206/455-3990 or TOLL FREE 800/426-9016.

DATA I/O

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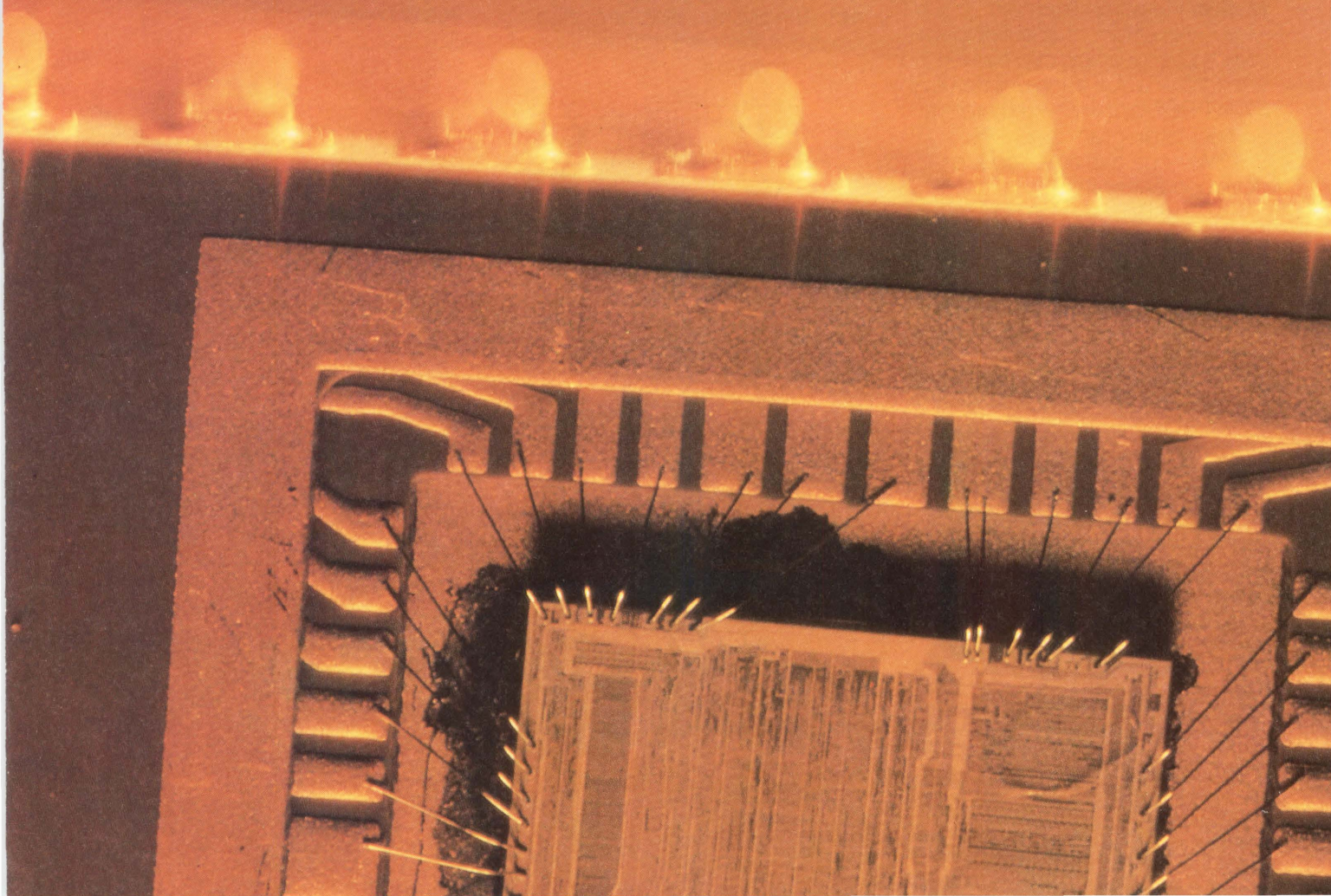
As your ideas race into the future, you need products to match your stride. Today Zilog offers you the most advanced family of microprocessor products made: components, support devices, software, development systems. All available in production quantities with worldwide support.

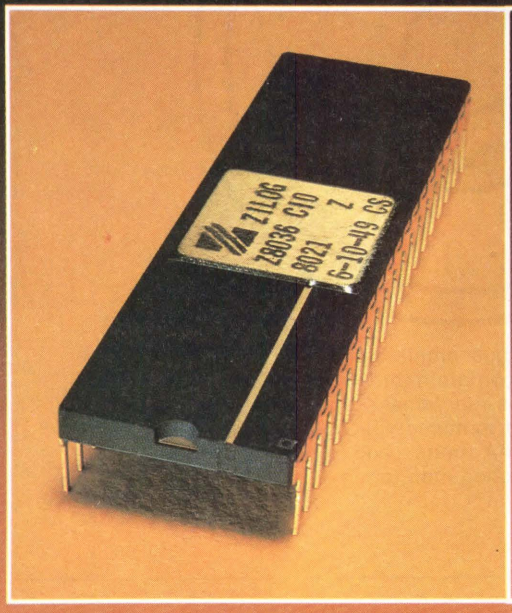
Elegant but soundly conservative scaled n-channel manufacturing processes combine with generation-ahead architecture to give Zilog products uncommon performance levels. The 8-bit Zilog Z80 revolutionized the microprocessor industry.

Today it's become the still more powerful Zilog Z80B. Its cousin, the Zilog Z8, packs an ingeniously flexible, complete 8-bit microcomputer onto a single chip. And, as you would expect, the incredible 16-bit Zilog Z8000 has set the microprocessor performance standards for the 1980's.

Give your imagination some of our hard, profitable facts to work with. Write: Zilog, Dept. E, 10460 Bubb Road, Cupertino, CA 95014. Or, call your nearby Zilog distributor.



THE POWER TO DESIGN THE MOST ADVANCED MICROPROCESSOR-BASED SYSTEMS IN THE WORLD. AT YOUR COMMAND TODAY. FROM ZILOG.



Meet the most versatile counter/timer and parallel I/O ever made. Zilog's Z8036 CIO.

Now there's an incredibly flexible way to time and count external events plus control and peripheral I/O interfaces in real time. It's Zilog's new Z8036 CIO. The Z8036 gives you: three fully programmable I/O ports with 20 I/O lines, four 16-bit counter/timers with four external access lines and three programmable output lines, pattern recognition logic, four handshake modes (2- and 3-line), and much more.

Zilog

An affiliate of EXXON ENTERPRISES INC.

CIRCLE 29 ON INQUIRY CARD

IBM Compatible Processors Based on Flexible Multibus Architecture

A modular multibus architecture forms the basis of QMX 6300 computer systems from Nanodata Computer Corp, One Computer Pk, Buffalo, NY 14203. Flexibility of the architecture allows the addition of modular components to meet user requirements through functional specialization. Modularity and microcode control ensure that peripherals and operating systems can be installed as necessary.

Fully compatible with IBM System/370 operating and application software, the QMX 6336 provides up to 1.3 times the internal performance of a 370/148. This performance level is achieved through the design concept, use of LSI technology, and microcode, all of which also contribute to the unit's price/performance ratio.

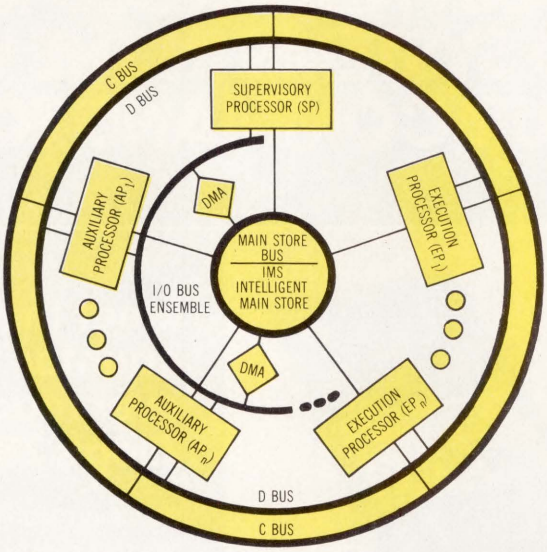
The design incorporates three independent types of processors: service, auxiliary, and execution. Each system has an independent service processor which monitors performance and runs diagnostics without increasing overhead for system operation or reducing performance. This processor is also capable of reconfiguring system resources to run under some types of failure conditions. Auxiliary processors provide system support, handle I/O processing, and perform special functions. Multiple auxiliary processors can be used to improve I/O response and performance in the event of intense I/O activity. The execution processor can emulate various instruction sets. Multiple identities can be executed simultaneously by adding one or more execution processors to the system. Modular addition of DMA controllers provides a high speed data transfer path to and from main memory. An auxiliary processor simultaneously sends control information to and receives information from these controllers via the I/O bus ensemble.

Composed of interchangeable modules, main memory has built-in hardware error correction. Addresses can be changed without altering physical memory. Main memory ranges in capacity from 1M to 4M bytes; a reloadable memory of up to 94k bytes stores microcode necessary for standard functions and optional features. Special function modules supply intelligent main memory with virtual memory control, memory protect, base registers, and data mapping.

The system's multiple bus structure allocates the main store bus to transfers to and from memory while functional processors are linked via the communication bus. The I/O bus ensemble provides multiple busing between auxiliary processors, DMA units, and device controllers. A diagnostic bus links components and functions only as a monitoring vehicle of the service processor.

The basic QMX 6336 consists of processor and display console. Memory capacities range from 1M to 4M bytes in 1M-byte increments; memory cycle time is 495 ns/8 bytes. Machine cycle time is 175 to 350 ns with simultaneous multiple instruction processing capability. The unit is equipped with one integrated byte multiplexer channel and two block multiplexer channels. Channel data rates of 50k bytes/s in byte mode and 2M bytes/s in block mode can be achieved on individual channels. Aggregate data rate is 8.05M bytes/s. Depending on configuration, system price will range from $163,000 to $212,000, without peripherals.

Circle 424 on Inquiry Card



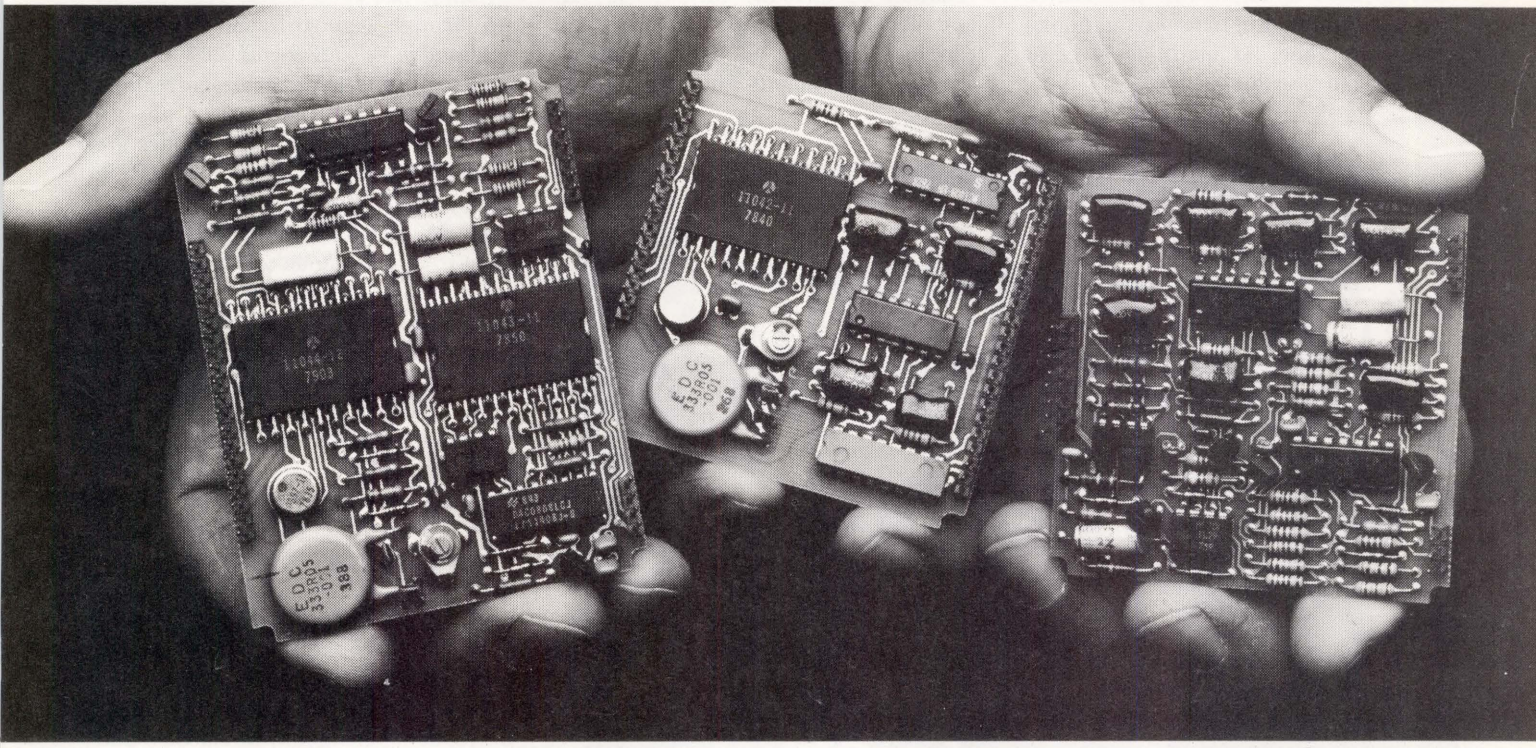
Based on modular multibus architecture, Nanodata's QMX 6300 series computers incorporate three separate processors. Communications bus links functional processors, while main store bus provides access to memory. I/O bus ensemble links auxiliary processors, DMA units, and device controllers; diagnostic bus offers function monitoring

Frequency Response Analyzer Offers Dynamic Testing in Laboratory/Field

Frequency response analyzer model 2540 is a complete keyboard interfaced, interactive CRT ATE system capable of dynamic analysis. For use standalone or linked to peripherals and larger systems the unit from Systron-Donner Corp, 2750 Systron Dr, Concord, CA 94518, works efficiently in field or laboratory environment.

The microprocessor controlled unit consists of a wideband high purity generator and two independent digital correlators. These elements are used to drive the system under test and to detect the response of the system at

R24. The first 2400 bps modular modem.



Rockwell's compact MOS-LSI modem gives new physical design freedom.

Micro Power

Rockwell's R24 Modem is the most compact 2400 bps MOS-LSI modem available today. Its small size and modularity give designers a whole new form factor flexibility. Requiring only 25 square inches of system area, the R24 is ideal for terminals and communications equipment.

The R24 provides functional flexibility also. Of its 3 modules, one is the transmitter, two the receiver. Terminal designers can offer transmit-only or receive-only options. And, the R24 is Bell 201 B/C and CCITT V.26 and V.26 bis compatible.

With its major functions in LSI circuits, the R24 is solid-state reliable and economical. It can be configured for operation on either leased lines or the general switched network. And, each low-profile module can be plugged into standard connectors or wave soldered onto system PC boards.

A new generation of modems from the company that's delivered more high-speed modems than anyone in the world. That's Rockwell Micropower!

For more information, contact Modem Marketing, Electronic Devices Division, Rockwell International, P.O. Box 3669, RC 55, Anaheim, California 92803. (714) 632-5535.

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...where science gets down to business

CIRCLE 30 ON INQUIRY CARD

any two points within the system. Commonly used dynamic test procedures are incorporated in firmware, minimizing setup time. As many as 120 test results can be stored.

With the analyzer, any transfer function of virtually any closed- or open-loop system, subsystem, or circuit can be measured. Its built-in microcomputer automates both measurement process and programming of dynamic test procedures. Tests are set up through keyboard control with the interactive 9″ (22.9-cm) CRT display providing guidance, error correction, or editing.

Two major measurement modes are accessible through the keyboard; in either, mode tests may be run once or may be repeated until interrupted. Spot frequency mode offers a choice of sinusoidal, triangular, or square waveforms over a 1-mHz to 10-kHz frequency range; all are digitally generated with 1024-steps/cycle resolution. Test results can be computed and expressed in cartesian, polar, or log-polar form with magnitudes in volts or decibels, absolute or relative.

In sweep frequency mode, a sequence of up to 120 discrete frequency measurements is performed over any specified frequency range. The unit may be keyboard programmed to sweep either up or down between selected limits. Logarithmic or linear frequency spacing may be selected and the internal microcomputer automatically computes test frequencies.

Built-in statistical facility enables display of the standard deviation of a set of readings. This allows the user to repeat a measurement until a statistical significance has been reached. Measurement can then proceed to the next test frequency, considerably reducing total test time. Statistical results are displayed adjacent to the relevant parameters in either spot or sweep frequency mode.

External peripheral devices are accessible via several interfaces. External CRT displays are driven through a rear panel video output; printers, computers, or memories are driven by an optional RS-232 or IEEE-488 interface rear panel output.

The analyzer uses full digital implementation to compute the direct Fourier transform. It operates over a 10^6 to 1 (120-dB) amplitude range, and provides ± 0.1 accuracy in magnitude, computing at 12 bits and allowing for worst case error to ensure 10-bit absolute accuracy and better than 0.1° accuracy in phase.

Circle 425 on Inquiry Card

Entry Level Computer Combines Virtual Storage With Flexibility

VS-50 is an entry level addition to the virtual storage family offered by Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851. In this system, low cost is combined with the functionality, versatility, and capabilities of the other members of the family.

A basic configuration consists of CPU with 128k-byte memory, internal fixed disc drive with 28k-byte storage capacity, workstation, and integral 1.2M-byte dual-sided, double-density diskette for program loading and media interchangeability. This configuration supports a maximum of six workstations and up to eight other peripherals and provides the ability to perform data processing, word processing, key entry, electronic mail, and telecommunications from a single workstation. The system can expand to 512k bytes of memory and can be enhanced to support 32 workstations, large capacity disc drives, multiple high speed printers, and other peripheral devices.

Introduced concurrently with the entry level computer system, the archiving workstation consists of workstation and single diskette drive. It supports a range of I/O operations and diskette formats. In addition to providing more functionality, the unit allows greater local control over dispersed data processing/word processing functions. When fully configured with multifunction diskette drive, the machine can handle archiving of word processing documents, data exchange with IBM 3741 type devices, storage and processing of VS/DP files, data file backup, and file interchange with other systems.

The key entry option is a software package that allows operators to key data through a workstation at machine speed. Using this option allows elimination of offline keypunches in many cases and will allow point of origin entry of orders, accounting, and operational data.

Circle 426 on Inquiry Card

Multiuser Computer Geared to Satisfy Business Processing Needs

Modularity is the key to the 8870/3 computer system's flexibility, allowing configuration to meet specific needs. In the machine, Nixdorf Computer Corp, 168 Middlesex Tpk, Burlington, MA 01803, has incorporated capability to handle 32 workstation peripherals and ability to transmit data between itself and other computer systems.

A logical enhancement of the workstation oriented 8870/1, it can function as an independent processing system or within a distributed network. Features of the system include 128k to 512k-byte main memory, 264M-byte disc storage capacity, 26M-, 39M-, or 52M-byte cartridge disc capacity, and 8-color graphics plotter. The CPU contains a 16-bit MOS LSI minicomputer with execution time of 700 ns. Programmable realtime clock and battery backed power fail/restart are standard.

Fully software compatible with the 8870/1, the unit supports the company's NIROS operating system as well as TAMOS operator control system. Operating systems provide facilities for performing byte manipulation, indirect addressing, multiregister arithmetic, base address relocation, page relocation, priority interrupts, and trap handling. Business BASIC provides 58 BASIC instructions and more than 300 functions.

Circle 427 on Inquiry Card

Single-Board Disc Controller Operates with PDP-11 VAX Computers

SC21 offers single-board convenience along with useful features and better performance. The large disc controller, for use with PDP-11 and VAX-11/780 systems, is a follow-on of the 2-board SC11 controller also produced by Emulex Corp, 2001 E Deere Ave, Santa Ana, CA 92705.

Among the features provided by the controller are the ability to interface up to four drives and to mix drives of different capacities and configurations on the same controller with no change to microcode. Bus delays have been reduced to where they are not a factor in system configuration.

An added feature, the adaptive DMA throttle allows the controller to measure the duration of pending NPR requests to ensure that other DMA requests are not locked out. This feature, combined with DMA burst length control, controlled deadband time between bursts, and 3-sector buffer, allows systems to operate without "data late" problems often encountered in complex configurations.

The controller, because of parts commonality and directly translated microcode with the SC11, is usable on all PDP-11 computers from the -11/04 up. It emulates all applicable DEC disc subsystems using any standard drive with standard SMD interface. Standard models are the SC21/A for a standard SMD, Winchester, and CMD type drives; /B for SMD and Winchester units in the 40M to 600M range; and /C for emulating an RK11 controller combined with RS06 or RK07 drives.

Circle 428 on Inquiry Card

32-Bit, Single-Slot CPU Provides Large Machine Features

Incorporating a single-slot integrated memory module and single-slot I/O processor, the 32-bit superminicomputer with single-slot CPU is packed in a compact 15" (38-cm) high chassis which mounts in a standard 19" (48-cm) rack. The unit, designed by Systems Engineering Labs, 6901 W Sunrise Blvd, Ft Lauderdale, FL 33313, provides compatibility with other Systems 32 machines via the Mapped Programming Executive (MPX-32).

Large machine features of the CPU include a 16M-byte mapped memory management system, instruction lookahead, and floating point arithmetic instructions. The memory module combines 256 bytes of ECC MOS memory with refresh logic and memory controller functions. The system can be expanded to 1M byte of directly addressable memory within the basic chassis. I/O processor module functions include 16-device controller subchannels, four external priority interrupts, interval timer, realtime clock, and operator's console interface.

By supporting up to 16M bytes of physical memory in a reduced hardware configuration, a memory resident version of the executive system (MPX/M) offers a cost-effective software approach to OEMs. Loaded from either magnetic tape or floppy disc, the software allows up to 20 programs to be executed concurrently.

Circle 429 on Inquiry Card

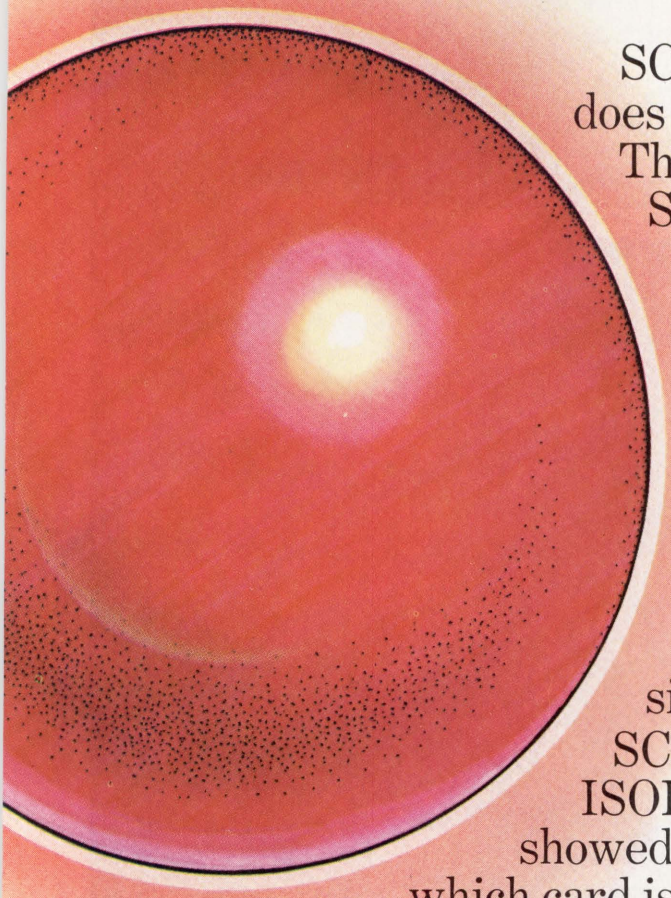
Advances in Solid State Circuits Subject of Conference

The IEEE International Solid State Circuits Conference, forum for presentation of advancements in solid state circuits, will take place from February 18 to 20, 1981, in New York City. Sponsors of the conference, the IEEE Solid State Circuits Council, New York section, and the University of Pennsylvania, are seeking papers for presentation.

Of particular interest are digital circuits, including logic and memory, design, fabrication, testing and systems aspects of LSI and VLSI; computers and peripherals; microprocessor circuits, architecture, and applications; and digital signal processing. Other areas of interest include analog devices, analog and signal processing, data acquisition, and telecommunications circuits; circuit design and testing; and optoelectronics.

Prospective authors should submit, before September 19, 30 copies of a 35-word abstract and a 300- to 500-word summary that describes significant theoretical and experimental results obtained. North American authors should send these to Lewis Winner, 301 Almeria, Box 343788, Coral Gables, FL 33134 (Tel: 305/446-8193). The European secretary is P. Jespers, Universite Catholique de Louvain, Place du Levant 3, B-1348 Louvain-La-Neuve, Belgium (Tel: 010/41.81.81-2564), and Asian papers should be directed to H. Ishikawa, Semiconductor Labs, Fujitsu Laboratories, Ltd, 1015 Kamikodanaka, Nakaharaku, Kawasaki, Japan (044/777-1111). Deadlines for European and Asian Papers are September 12 and September 5, respectively.

See SCOUT save.

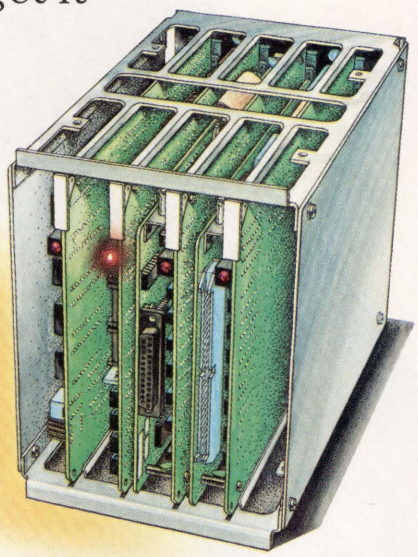


SCOUT™ has a red light. It does not mean what you think. The red light says one of SCOUT's boards does not feel well.

Will this make you sad because your minicomputer can't play anymore?

Will the expensive repairman take a long time to get it fixed?

No no, silly. Since SCOUT's ISOLITE™ showed you which card is bad, all you do is pull it out and put in a spare 6.25″ x 8.3″ card.



What fun! Now SCOUT can run and play again. And save you a lot of jack.

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Save on service costs. Save on system costs.

Save on 16-bit minicomputer performance. SCOUT starts at less than $1000 for a CPU, I/O, 32K Byte RAM and card cage.

Isn't saving fun?

Save SCOUT, save.

See SCOUT save.

Money. Time. And end user aggravation. Plus other ways to save in our how-to-save-on-maintenance primer, *A Plug for SCOUT.* Get your free copy with this coupon and a business card. Or, for immediate information call 714/833-8830, Ext. 455.

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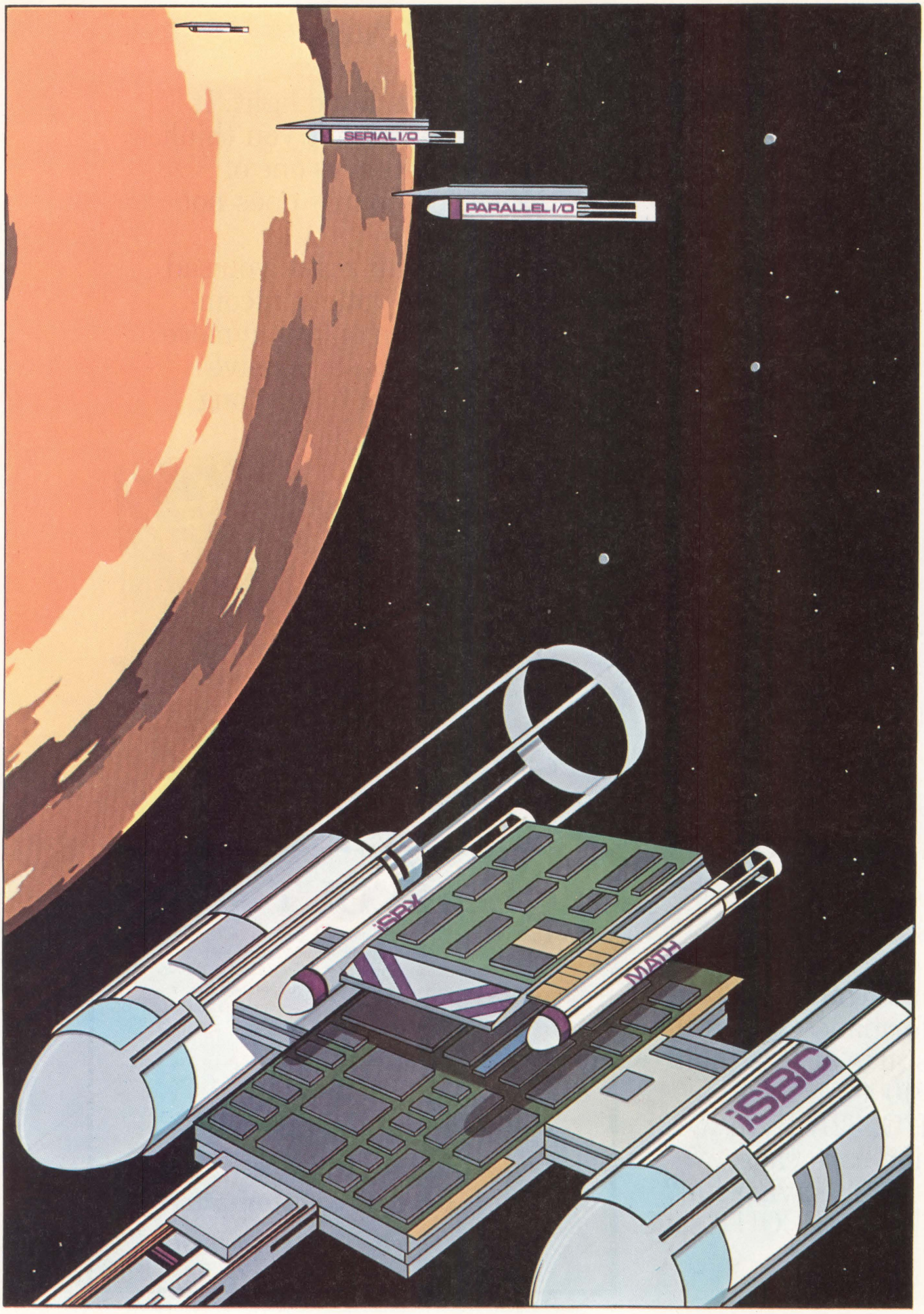
CIRCLE 33 ON INQUIRY CARD


SERIAL I/O
PARALLEL I/O
iSBX
MATH
iSBC

One Step Beyond the iSBC™ System

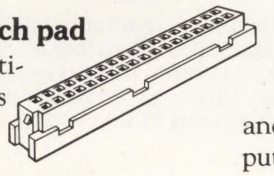
Introducing iSBX™ Multimodule™ boards. A whole new dimension in configuring single board computers.

Intel pioneered the concept of flexible microcomputer *system* design in 1976. That's when we began introducing iSBC™ systems, a family of single board computers. These are expandable via the Multibus™ interface, presently accepted as the industry standard for microcomputers.

Now Intel has extended this well-accepted concept to *board*-level design—with Multimodule™ boards and the iSBX™ bus. With this new line of plug-in modules, you can now expand iSBC systems simply and efficiently at the board level. Without making any demands on the system structure. And all at much lower cost than was previously possible.

Multimodules let you add special performance features today to your iSBC host board—features like high-speed math functions. And serial or parallel I/O. Soon you'll also be able to add Multimodules for D-to-A and A-to-D conversion, communications, and peripheral interfaces—and more. With these modules, you'll be able to precisely tailor hardware configurations to your application, and cut down critical development time.

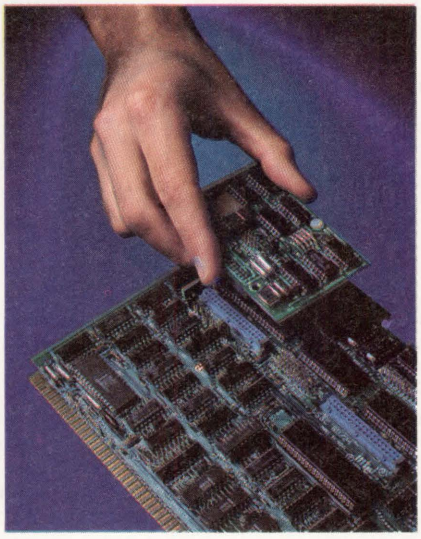
The iSBX™ launch pad



The key to Multimodule flexibility is the iSBX bus—the first physical/electrical interface for direct on-board expansion of iSBC systems. Available on all future Intel single board computers, the iSBX bus assures you of compatibility between iSBCs and the emerging Multimodule product line.

You can also count on improved system performance. Since Multimodules tie directly into the iSBC's internal bus, you get faster, more efficient memory access and I/O operation than is possible with full expansion boards.

For those who want to explore their own expansion module designs, Intel also offers iSBX 960-5™ connectors. These let you create custom Multimodule boards to meet your own unique requirements.



Two new iSBC™ command modules

Intel's new 8-bit iSBC 80/10B™ and iSBC 80/24™ single board computers are just the first of many iSBCs to offer iSBX Multimodule expansion capabilities. Both are improved, iSBX-compatible versions of popular single board computers.

Backed by life-support equipment

To support your implementation efforts, Intel provides an extensive set of hardware development tools. Such as the Intellec® system, with ICE™ in-circuit emulation. Or high-level programming languages like PL/M, BASIC, and FORTRAN. And the RMX/80™ real-time software.

A small step for microcomputers

Intel's new iSBX bus and family of Multimodules represent a small step for incremental design of micros. But a giant step toward making you and your iSBC system more productive. Available from Intel today are the first three Multimodules, and our two iSBX-compatible single board computers. The next step is up to you.

For more information, or to order, return this coupon or call your local Intel sales office/distributor. Or contact Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

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Please send information on:
☐ iSBX Multimodule package
☐ Configuration Guide
Other _____
☐ Please have a Sales Representative call.

Name _____

Title/Organization _____

Address _____

City/State/Zip _____

Phone _____

Mail to: Intel Corporation, 3065 Bowers Ave., Santa Clara, CA 95051. CD

CIRCLE 34 ON INQUIRY CARD

Belden's new fan cords help make ends meet.

Belden cooling fan cords help make ends meet financially... by helping cord ends mate faster and easier during production. That's because Belden cords offer the kind of high quality and superior product features that have made Belden a preferred supply source for over 75 years. Just look at these great features.

TWO COMPLETELY FINISHED ENDS while most others only offer a finished plug end.

NON PLUG ENDS ARE SLIT, STRIPPED, TWISTED, SOLDERED and ready for production when they're delivered to you.

PRICE IS COMPARABLE TO CORDS WITH ONLY A FINISHED PLUG END. That means you get all this added value at no extra cost.

PLUG ENDS ARE MADE AT A 45 DEGREE ANGLE to fit the contour of most cooling fans. This helps in both the design and installation phases of production.

TEMPERATURE TOLERANCE RATING OF 105 DEGREES C to provide longer, more dependable performance under tough conditions.

UL AND CSA APPROVED 18/2 SPT 1 with quotes available for 18/3 SPT 2.

FIVE STANDARD LENGTHS: 17902—2′, 17903—3′, 17904—4′, 17905—5′, 17906—6′.

For more information, contact Belden Corporation, Electronic Division, P.O. Box 1980, Richmond, Indiana 47374. Phone: 317-983-5200. Or call our Eastern Regional Sales Office at 617-872-7846 or Western Regional Sales Office at 714-833-7700.

BELDEN

Coming through...

with new ideas for moving electrical energy

8-1-0 A

CIRCLE 35 ON INQUIRY CARD

SOFTWARE

VAX Software Extensions Serve Realtime, Interactive, And Commercial Needs

Extensions to the VAX software set introduced by Digital Equipment Corp, Maynard, MA 01754, provide greater programming and execution efficiency and increase the system's application range. Included in the announcement are BASIC and COBOL compilers, a version of FORTRAN, CORAL 66 language support, an enhanced VAX/VMS operating system, and extended capabilities for data retrieval and forms generation.

The VAX/VMS virtual memory operating system supports up to 4M bytes of MA780 as well as 8M-bytes local memory, DR780 high speed interface, and added peripheral devices. In addition, it supplies an editor with keypad editing and automatic journaling, instructional aids, user message utility, system tuning and disc protection features, and encrypted passwords for security.

BASIC and COBOL compilers extend current standards and offer improved performance. Taking advantage of the large address space and instruction set, the compilers produce 32-bit object code. Utilities and functions of the VMS common language environment that can be accessed include symbolic debugger, runtime library of sharable routines, RMS file management system with multikey ISAM, and transparent access to DECnet communications software. COBOL incorporates features planned for the ANSI standard COBOL expected during 1981. The VAX implementation supports nine COBOL modules—nucleus, table handling, sequential, relative, and indexed I/O, segmentation, SORT/MERGE, library, and interprogram communication. The language processor can compile 3000 lines/min.

A superset of FORTRAN-77, the FORTRAN compiler can handle 2000 to 3000 lines/min. It provides access to RMS multikeyed ISAM files. BASIC has compilation speed of 3000 lines/min and execution speed of FORTRAN. CORAL 66 conforms to the UK official definition and allows block structuring of programs.

Extension of the Forms Management System to VAX systems allows users to interactively create and modify custom forms using standard languages. Instant validation of application data, scrolling for large forms, and a HELP facility are provided. In addition, a version of Datatrieve allows access to RMS, supports variable record lengths, and offers single inquiry access to multiple forms.

Circle 430 on Inquiry Card

Data Management Package Ensures Consistency of Distributed Data Base

ENCOMPASS provides total transaction processing and distributed database control in one package to ease the task of generating online applications programs. The distributed database management system, developed by Tandem Computers Inc, 19333 Vallco Pkwy, Cupertino, CA 95014, for use with its NonStop™ systems, ensures database consistency and recovery in a totally distributed environment.

Of interest to users of transaction oriented online systems, the system contains transaction logging and backout functions that guarantee integrity of data whether stored locally or in geographically dispersed sites within a network. Among the system's features are distributed audit trails, transaction backout over a dispersed data network, automatic dump of audit files, online backup, network wide transaction control facilities, and software utilities for recovery of dispersed data files in event of logic errors in an application program or of a total communication failure. In addition, it includes software for frontend control of

DILOG INTERFACES DEC 11*

10 intelligent hard disc and magnetic tape controllers offer LSI-11,* 11/2, 11/23, and PDP-11* single quad slot compatibility with up to 60% power saving.

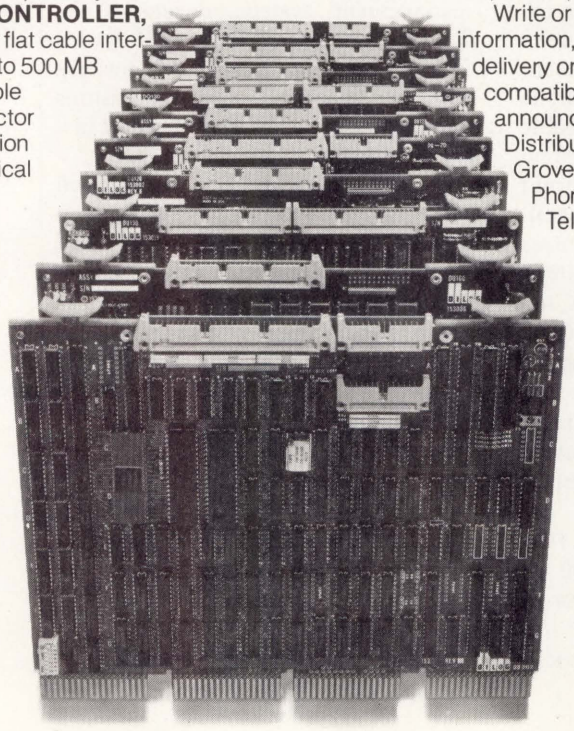
Only DILOG (Distributed Logic Corporation) exclusive automated design, common proprietary architecture and sophisticated bipolar μPs give you • all single board quad size products requiring no external power or chassis . . . just a cable to connect the drive . . . *you don't need anything else* • high reliability • automated self-test including data base protect feature and indicator. And at cost savings of 50% or more.

LSI-11 MAGNETIC TAPE CONTROLLER, Model DQ 120, interfaces 4 industry standard reel-to-reel drives • emulates TM11* • handles 7 and/or 9 track NRZI drives to 112.5 ips • selectable DEC or IBM byte order formatting • data error checking • RT-11/RSX-11* compatible • extended addressing to 128K words.

LSI-11 MAGNETIC TAPE COUPLER, Model DQ 130, interfaces dual density (NRZI/PE) formatted drives • emulates TM11 • handles up to eight 9 track 800/1600 bpi industry standard drives at speeds from 12.5 to 125 ips • "streamer" mode capability • software or switch selectable density • RT-11/RSX-11 software compatibility.

LSI-11 MASS STORAGE DISC CONTROLLER, Model DQ 200, interfaces any two SMD flat cable interface compatible hard disc drives for up to 500 MB on-line storage • mix or match compatible Winchester, SMD or CMD • variable sector size • automatic media flaw compensation with bad sector flagging • optimized logical to physical unit mapping • implements Winchester fixed head option.

NEW LSI-11 SHUGART SA4000 WINCHESTER DISC CONTROLLER, Model DQ 201, emulates DEC RK* • runs drivers under RT-11 and RSX-11M* systems • compatible with 14.5 MB SA4004 or 29 MB SA4008 drives • automatic media flaw compensation.



LSI-11 DISC CONTROLLER, Model DQ 100, interfaces 2.5, 5, 10 or 20 MB cartridge and fixed platter drives in combinations to 80 MB • RKV-11/RKO5* emulator • handles front load (2315) and/or top load (5440) drives • automatic power fail/power down media protection • RT-11/RSX-11 compatible.

NEW LSI-11 EMULATING MASS STORAGE CONTROLLER, Model DQ 202. Cost effective interface of two 8 and/or 14-inch Winchesters, SMD or CMD hard disc drives without changing controller . . . 8 to 300 MB capacity • RP emulator • automatic media flaw compensation.

PDP-11 MAGNETIC TAPE CONTROLLER, Model DU 120, emulates TM-11 and has same features as Model DQ 120 (LSI unit) • software compatible with RT-11, RSX-11, RSTS, IAS and MUMPS.

NEW PDP-11 MAGNETIC TAPE COUPLER, Model DU 130, offers features of Model DQ 130 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS software compatible.

PDP-11 DISC CONTROLLER, Model DU 100 includes features of Model DQ 100 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS compatible • emulates RK-11.

NEW PDP-11 EMULATING MASS STORAGE CONTROLLER, Model DU 202, offers same features as Model DQ 202 (LSI unit).

Write or call for detailed product performance information, OEM quantity pricing, stock to 30 day delivery or warranty data on these DEC 11 compatible products . . . or several soon to be announced new DILOG products.

Distributed Logic Corp., 12800-G Garden Grove Blvd., Garden Grove, CA 92643
Phone (714) 534-8950
Telex: 681399 DILOG GGVE

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DILOG

CIRCLE 37 ON INQUIRY CARD

All DILOG μP Products are Low Power, Quad Size

*Trademark Digital Equipment Corp.

SOFTWARE

multiple terminals, various line protocols, screen formatting and sequencing, data validation, transaction definition and application control, data dictionary, and query language and report writer.

Because the software performs terminal management, database control, and transaction logging and auditing as automatic system functions, programmer productivity is increased. Users can view each transaction as a whole even though geographically dispersed.

The system's transaction monitoring facility ensures a consistent data base by enabling the removal of incomplete or interrupted transactions from the distributed network. Backout of individual transactions is accomplished automatically at every node in a network through the use of distributed audit trails.

Licenses for the package are available at $31,500 plus an $8500 microcode charge. Release is scheduled for December.

Circle 431 on Inquiry Card

Automatic Programming System Eliminates Many Coding Tasks

FORCE (For Online Realtime Code Expansion) speeds the creation of application programs by freeing the programmer from time consuming coding tasks. The automatic programming system, introduced by Point 4 Data Corp, 2569 McCabe Way, Irvine, CA 92714, consists of a central database handler. It offers standardized messages, comments, and commands, continuity within the system and between systems, and freedom from coding aspects of the program.

From a description of the screen format, record layout, and data element that is fed into the database, executable code is generated. Creation of the database is independent of individual program modules. With FORCE all other modules in the system can be automatically recoded on demand. Generated code is free from syntactic and typographical errors, reducing system development time.

Operator/system interaction is improved by the system's self-explanatory instructions and error messages. Systems continuity provides standard field type, size range checks, and table for file lookups in every module, allowing programmers familiar with the structure to move within and between systems easily, as well as to maintain other programs written by others.

FORCE is available in four levels. Level 1 covers database maintenance, screen maintenance, screen macro expansion, database documentation, menu program generation, and system linkage module; level 2 covers data element maintenance, input macro expansion, and element and synonym documentation; level 3 offers file and record layout maintenance, disc I/O macro expansion, and file and record layout documentation; and level 4 provides program input maintenance, macro expansion modules, file maintenance code generation, and program documentation.

Running under the IRIS realtime operating system and using Business BASIC, the system rents for from $400 to $1050/mo. □

Circle 432 on Inquiry Card

Aircraft Cockpit Simulator Researches Collision Avoidance Systems

Bruce Morgenstern

ARINC Research Corporation
2551 Riva Road, Annapolis, MD 21401

A simulation test bed has been developed to determine the cockpit information requirements for an aircraft collision avoidance system so that pilots can evaluate alternative methods of displaying collision avoidance information in a realistic but safe environment. The test bed was designed around an existing Boeing 727 cockpit simulator equipped with a computer generated image system that projects a nighttime visual scene on the cockpit windshield. A simulation control computer and peripherals interfaced to the simulator provide a realistic air traffic control environment. Qualified pilots from commercial aviation and industry flew typical flight patterns in the simulated Los Angeles metropolitan area. During the flight, adverse situations involving other aircraft were generated, and pilots were asked to respond to these situations on the basis of information presented to them by one of three experimental collision avoidance displays.

Two computers were included, in addition to the GP-4* that was part of the existing cockpit simulator: a Digital Equipment Corp PDP-11/35 to produce a computer generated scene depicting the nighttime view from the forward windshield of the jet transport aircraft and project it onto the forward windows of the simulator, adding realism to the regular flight training program, and a PDP-11/34 to produce the air traffic control environment for the simulation test bed and to control simulation activities (Fig 1).

The simulation control computer collected flight results and stored these data on tape for subsequent analysis. Flight operation data collected by the computer were correlated with data from questionnaires filled out by participating pilots to determine the cockpit information requirements and used to prepare a final report on the experimental results.

The test bed is an interactive, distributed processing system that includes a simulated cockpit and its associated control computer; a computer generated image (CGI) display system; a simulation control computer; a control and monitoring station with associated communications; and three experimental collision avoidance displays. It was designed to permit evaluation of flight crew reactions to aircraft conflict and near conflict situations that could present a significant element of danger if conducted in actual aircraft. Use of a simulator makes experimental problem control and data collection much simpler than would be possible in an experiment using actual aircraft. In addition, simulation presents significant cost and time advantages over an experiment that might require several transport aircraft operating in controlled airspace under the precise conditions necessary for experimental work.

The cockpit module is mounted on a base that moves in three degrees of freedom to simulate the movement of an aircraft cockpit. A control panel located inside the cockpit module across from the flight engineer's station effects simulator control. During the simulation, this panel was used to control weather conditions, aircraft weight and balance, fuel and serviceable items, and aircraft initial position.

Image Display System

The landscape scene consists of light points that provide a full color representation of the evening landscape in a large metropolitan area, including the major airport serving the city. It is made up of more than 7000 lights out of a data base of 15,000. Similar data bases are available for the Denver, Los Angeles, and San Francisco metropolitan areas. These data bases are stored in the image display

*The GP-4 computer was developed by Singer-Link to control the aerodynamic simulation of the flight, by such parameters as attitude, degree of air turbulence, airspeed, and the like.

A whole world. Because our parent company, C. Itoh Co., Ltd. (pronounced "C. Eetoe") is a multinational organization with resources and subsidiaries located in every corner of the globe.

As C. Itoh Electronics, Inc., we're fortunate to be part of this international network. It lets us seek out quality materials and technologies wherever they can be found. And for a company that specializes in computer peripherals for the OEM, that's just as important as price or the capability to deliver.

Today, we're offering the latest designs in dot matrix and daisy wheel printers, card readers, CRT monitors, floppy disk drives, and a lot more.

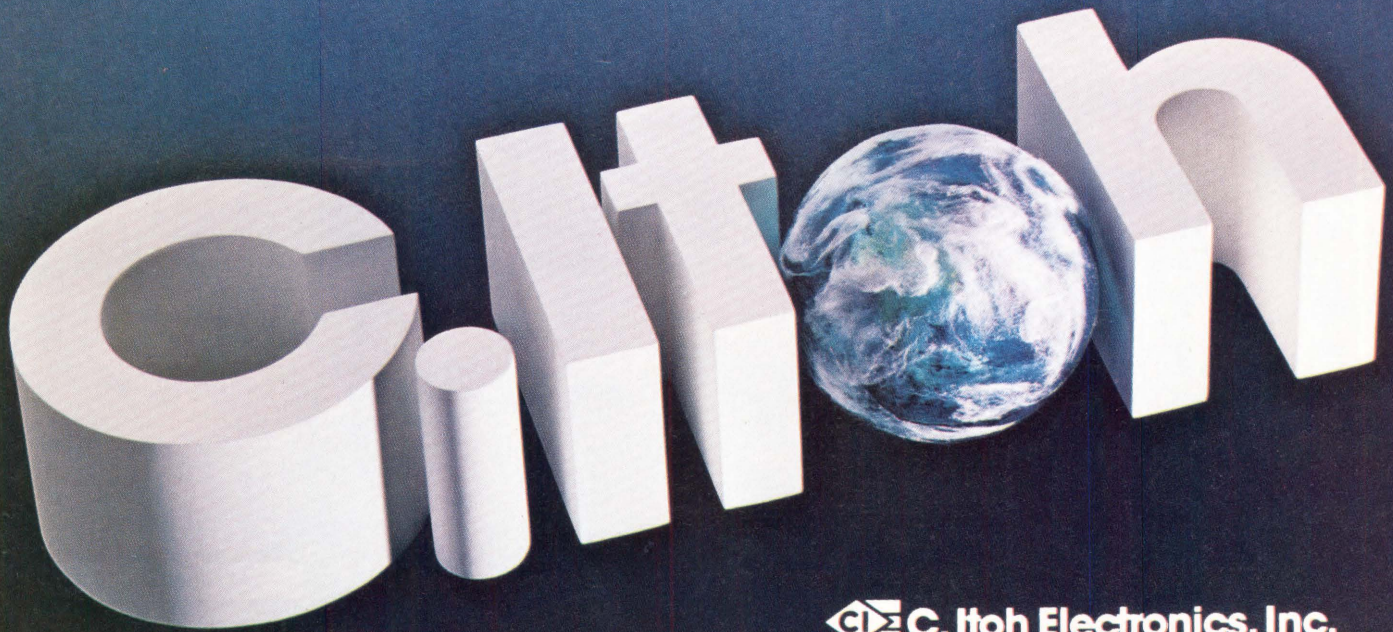
We're also seeing to it that our OEM customers get all the support they need. The engineering support to solve their system integration problems. Plus complete documentation and a service network that operates repair and refurbishment stations nationwide.

So when you deal with us, you can be sure you're doing business with people who are dedicated to the OEM. And a company whose parent organization has been around since 1858.

Our goal? To become the best OEM peripheral source in the country. Because with all our international connections, we haven't forgotten what our motto promises: One world of quality.

For information on our product lines for the OEM computer systems manufacturer, contact C. Itoh Electronics, Inc., 5301 Beethoven St., Los Angeles, CA 90066, Tel. (213) 390-7778; Midwestern Regional Office: 240 East Lake St., Suite 301-A, Addison, Illinois 60101, Tel. (312) 941-1310; Eastern Regional Office: 666 Third Avenue, New York, NY 10017; Tel. (212) 682-0420.

A world of quality.



C. Itoh Electronics, Inc.
One world of quality

CIRCLE 39 ON INQUIRY CARD

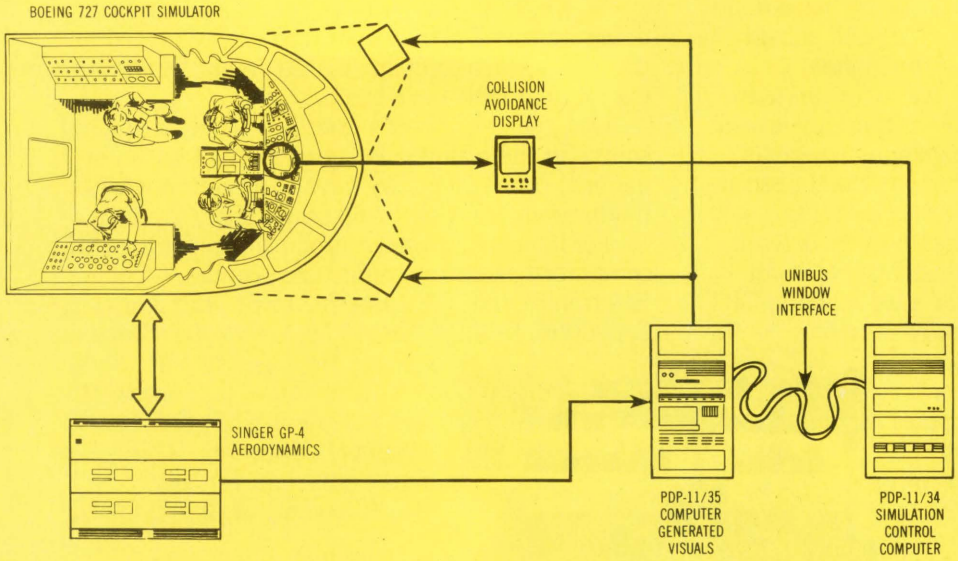
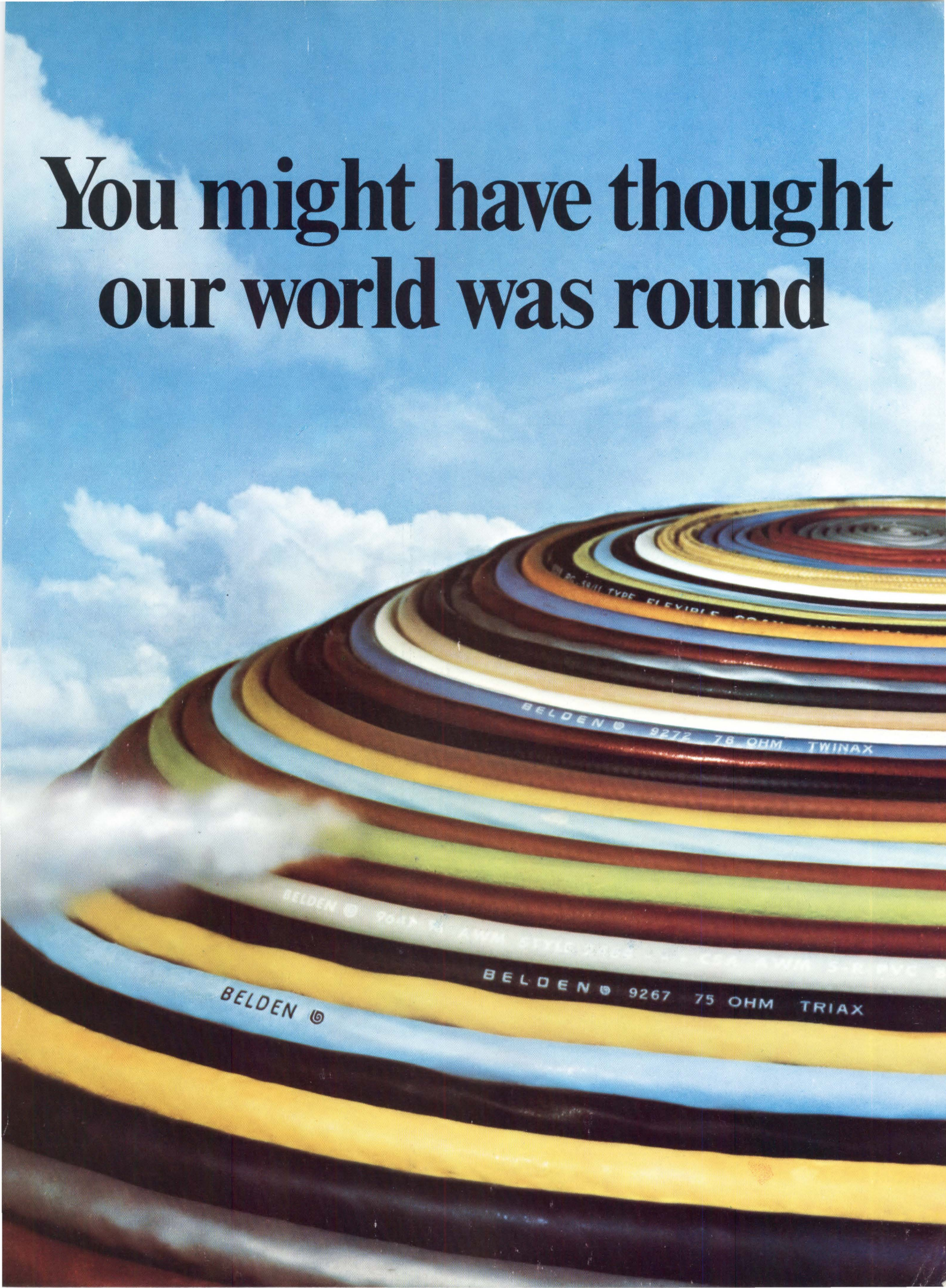


Fig 1 Diagram of aircraft collision avoidance simulator. PDP-11/34 and /35 computers were added to existing GP4 computer and aircraft cockpit simulator. By introducing adverse weather, turbulence, system malfunction, and potential collision situations, simulator aids in flight crew training and instrument evaluation

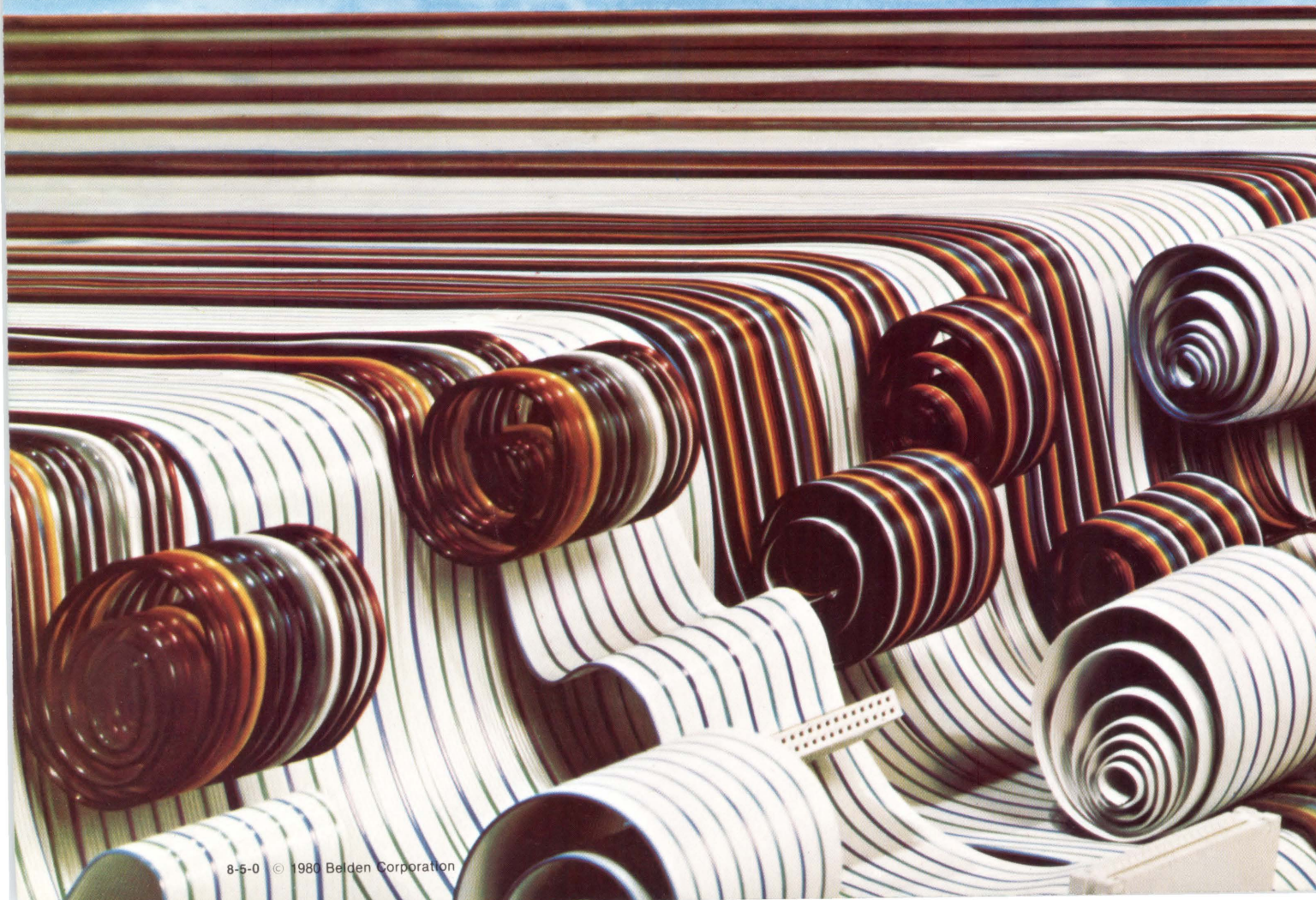
system computer as a file of 3-dimensional coordinates characterized as to color and intensity. The displayed lights fall into the forward field of view, which is approximately 45° right, 55° left, 30° up, and 60° down. An interface to the GP-4 computer supplies simulator position and attitude, which are updated 20 times/s. Additional controls simulate various conditions of visibility, ceiling height, cloud cover, and ground fog.

CGI system software was modified to simulate other aircraft in the visual scene. Each intruder aircraft appears as a

You might have thought our world was round



Think again.



BELDEN FLAT CABLE & CONNECTOR SYSTEMS

Sorry, Columbus. When it comes to cable, round is not always right. And we should know, we make both round and flat cable.

For mass terminations, Belden Flat Cable and Connector Systems offer substantial improvements in installation time, serviceability and cost effectiveness when compared to round cable. What's more, Belden Flat Cable is worlds away from other flat cable. With tough, flexible insulations; uniform centers; easier breakouts; and much more. It's the kind of quality that keeps total end costs down to earth.

We offer a wide range of custom and standard flat cables—.050″, .100″ and .156″ centers; laminated; bonded; jumper cables in bulk rolls or pre-stripped lengths; and our unique twisted pair cable, Vari-Twist.™

Vari-Twist is the only twisted pair cable which has both opposite direction lays—and varying length of lay—on each adjacent pair as a standard product.

Combine all our flat cable with dependable Belden connectors and accessories, and you have a complete flat cable and connector system. A complete system which is made even better by the full service and custom engineering capabilities you've come to expect from Belden.

Let us put our world of flat cable to work for you. You'll discover we beat the competition flat.

CIRCLE NUMBER 222 ON THE READER SERVICE CARD.

Belden takes the system approach

Quality Flat Cables

Belden makes flat cable for all types of applications. Among our flat cable capabilities:

• Round conductors, (solid, stranded, or unistrand) • Flat conductors (Mylar or Kapton insulation) • Bulk and precut, prestripped jumper cables • PVC solid or color-coded laminations • Cable assemblies made to specifications • Compatibility with all major makes of connectors • Passes VW-1 Vertical Flame Test

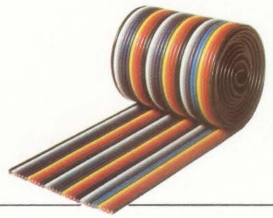
Compatible Connectors

Belden connectors provide fast, easy installation; reliable connections; and long service life. Among the features offered by all Belden connectors:

• −55°C to +105°C temperature range • 30V DC UL voltage ratings • Phosphor-bronze (gold-over-nickel plating) contact materials • Highly reliable U-contact (double action IDC) on all IDC connectors • Solvent-resistant glass-filled PBT housings • UL recognized 94V-O

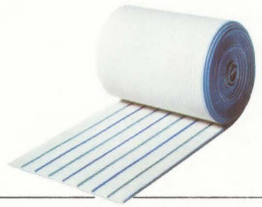
Bonded Flat Cable

• 10 to 30 conductors • 22, 24 and 26 AWG stranded • 80°C temperature rating • 300V voltage rating • UL style number 2697



Laminated Flat Cable

• .050" (1.27mm) spacing • 10 to 64 conductors, 28 AWG stranded • 105°C temperature rating • 300V voltage rating • UL style number 2651



Rainbow Flat Cable

• .050" (1.27mm) spacing • 10 to 64 conductors, 28 AWG stranded • 105°C temperature rating • 300V voltage rating • UL style number 2884

.100/.156 Flat Cable

• .100" (2.54mm) spacing, 2 to 28 conductors • .156" (3.96mm) spacing, 2 to 24 conductors • 22, 24, 26 and 28 AWG stranded (.100)/18, 22, 24 and 26 AWG stranded (.156) • Rated to 105°C & 300V

Vari-Twist™ Flat Cable

• .050" (1.27mm) spacing • 5 to 32 pairs • Adjacent pairs have opposite lays • Lay length varies with each adjacent pair • 105° C temperature rating • 300V voltage rating

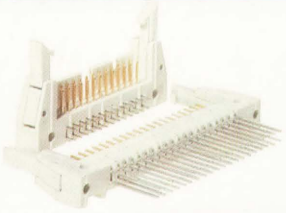
Write for our free Catalog

Belden Corporation, Electronic Division, P.O. Box 1980, Richmond, IN 47374. Phone: (317) 983-5200. Out west, call our regional sales office at (714) 833-7700. In the east, call our sales office at (617) 872-7846.

CIRCLE NUMBER 222 ON THE READER SERVICE CARD.

Headers

• .100" (2.54mm) grid contact/terminal spacing • Selective plating (gold-plated contact and solder-plated terminal) • Flex lock/eject hooks • Many diversifications (10 to 60 pins, wire-wrap/straight/right angle)

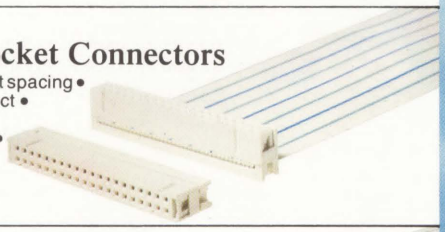


Socket Connectors

• .100" (2.54mm) contact spacing • Double-cantilever contact • Bottom-entry contact • Many diversifications (10 to 60 pins, closed-end/through-end) • Dual-beamed contacts • Polycarbonate strain relief

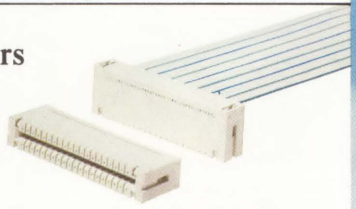
Low-profile Socket Connectors

• .100" (2.54mm) contact spacing • Double-cantilever contact • Bottom-entry contact • Dual-beamed contacts • Many diversifications (10 to 60 pins)



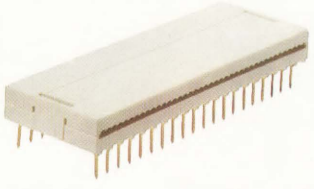
Card Edge Connectors

• .100" (2.54mm) contact spacing • Bifurcated contacts • Many diversifications (10 to 60 pins; with ears, half ears or without ears; and with or without strain relief)



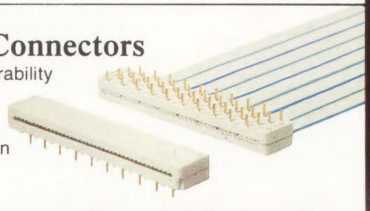
D.I.P. Connectors

• Plugs into IC sockets or can be soldered for permanent connections • Low-profile installation on PC board • Many diversifications (10 to 60 pins)



P.C.B. Transition Connectors

• Tinned pins for excellent solderability • For reliable permanent PC board connections • 1.6mm (1/16") standard thickness of PC board • 14, 16, 24 and 40 position connectors



BELDEN

Coming through...

with new ideas for moving electrical energy

Printed in USA

flashing red light and a flashing white light that seem to be spaced 60 ft (18 m) apart. Simulated aircraft, whose positions relative to the simulator place them within the forward viewing area, appear in the nighttime visual scene. Processing the red and white lights independently provides proper viewing perspective; in all other respects, the moving lights representing other aircraft are controlled in the same manner as the fixed ground lights.

Simulation Control Computer

Software for simulation control was developed in FORTRAN and assembly language under the RSX-11M multitasking environment that allows several executable modules, called tasks, to compete for the computer's resources simultaneously. Tasks can execute continuously, periodically, or on request. A predetermined priority scheme determines which task will execute at any particular time.

Simulation tasks can be described in terms of five major problem areas: parameter and variable initialization, the main loop, console operation, the simulator interface service routine, and the display drivers. Simulation parameters and variables, including collision avoidance parameters, aircraft maneuvering variables, aircraft state variables, display data buffers, and simulation state flags, all are stored in a shared global data region—a partitioned area of memory containing data or code that can be accessed by more than one task. The parameter and variable initialization task sets up the global data region at the beginning of each simulated flight.

The main loop task creates the air traffic control environment. This software includes traffic and intruder generation logic, simple radar and tracking algorithms, conflict detection and resolution logic, and an air traffic control display driver. Traffic generation logic, in turn, performs aircraft initialization, sets up an arbitrarily complex flight path, applies a simple aerodynamic model, and terminates the aircraft flight simulation at an appropriate time. Traffic flight plan data are stored in external files. These data consist of the aircraft initial state and a list of time-driven maneuvers that update the aircraft control variables—heading, speed, and altitude. These, in turn, are used to update aircraft position and velocity through a simple integration scheme. Updated data act as input to a tracking mechanism that introduces characteristic position reporting errors present in the air traffic control system.

The intruder logic initiates conflict situations between simulated intruder aircraft and the cockpit simulator. Conflict geometries are preprogrammed, and conflicts occur with limited intervention by the simulation test engineer. The test engineer can, however, control the intruder's speed and altitude to assist development of the conflict.

The FAA furnished collision avoidance logic consists of detection, resolution, and proximity warning indication mechanisms. Collision avoidance commands supplied as output inform the pilot of appropriate action required to avoid a collision, while traffic advisories provide the pilot with information about aircraft that are within his protected volume of airspace.

An air traffic control display was developed for use by an actual air traffic controller who assists in the experiment by providing appropriate clearances to the pilot in the simulator and increasing the realism of the simulation. A Tektronix 4006 storage tube graphics terminal creates the air traffic control display and supplies the air traffic controller with appropriate air routes, navigational aids, aircraft tracks, and a readout of the simulator's altitude (Fig 2). The display is redrawn whenever the simulator approaches the edge of the display area.

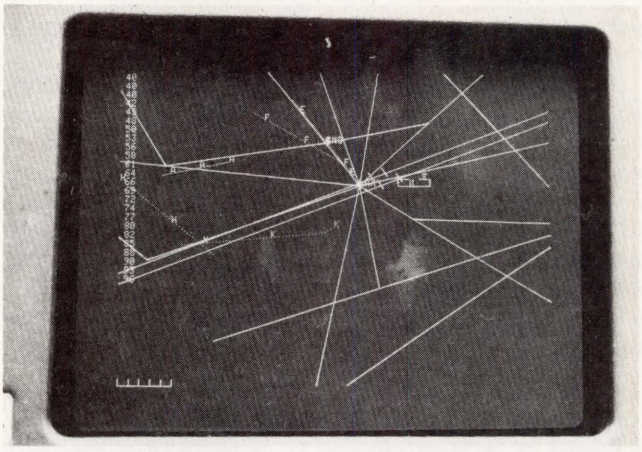


Fig 2 Simulated air traffic control display. Air traffic controller assists with experiments by providing clearances to pilot. Controller's display shows air routes, navigational aids, aircraft tracks, and cockpit simulator altitude. Display is redrawn when simulator approaches edge of screen

The console operating task supplies a means for the test engineer to interact with the simulation and obtain simulation status information. This is achieved by reading or modifying variables and flags in the shared global data region. To reduce interference with the simulation's realtime activities, the console operation task executes at a low priority and only when sufficient time is available.

Multiple Computer Interface

The simulation control computer and the CGI display computer communicate via a UNIBUS window, a high speed interbus channel. This window, selected as the fastest available interface between the two computers, allows one system to access addresses on a companion system's bus as though the addresses were on its own bus. This is achieved by translating requests to a designated part of the bus address space into requests on the companion bus. Since window hardware performs all synchronization internally, operation is completely transparent to operating software.

Window size can be set in binary increments from 512 to 32k words and is normally established directly above the last memory module in each machine. A window size of 512 words was chosen to minimize impact on the existing CGI display software. Since the simulation control computer has 64k words of memory, the window occupies byte addresses

400000 to 402000 octal. Once initialized, any access from the simulation control computer to a location in this range will be translated automatically to access the appropriate address in the companion system. Although either processor is capable of originating access through the window, only the simulation control computer is used for this purpose, further reducing the number of software changes required in the CGI system.

Establishing a common partition above the simulation control computer's physical memory simplifies program access to the bus window. Creating the partition after initial system loading bypasses the RSX-11M bootstrap diagnostics. Once created, a shared data region can be mapped to the partition, and access to the window becomes transparent to the programmer.

Initialization of the window is accomplished by setting transfer enable and write enable flags in the bus window control and status register. There is one set of registers for each processor with access limited to the assigned processor. In addition, the relocation address register assigned to the computer generated graphics system is set to specify the starting address of the window area. Interrupt on error conditions is disabled to eliminate the need for interrupt service routines; interface software implements all error handling.

Once initialized, the data transfers are very straightforward and transparent to the software. To access a data item that is offset 100 bytes from the start of the data area in the CGI computer, the address 400000 + 100 or 400100 is requested on the simulation control computer. Bus window hardware translates this request into the appropriate address in the CGI computer memory. A second bus request is next generated, this time in the CGI computer, and the transfer is completed.

The simulator interface service task performs data transfers every 1/20 s to update the nighttime visual scene. Data to be transferred include simulator position and attitude, and positions of those aircraft that could be represented as part of the visual scene—aircraft that are within visible range of the cockpit simulator. The interface service task runs at highest priority and executes as efficiently as possible to minimize impact on CGI computer processing, since data transfers tie up both of the computer busses. No noticeable degradation in the computer generated visual scene was apparent during the experiment.

Cockpit Displays

Test displays selected for use in the simulation reflect three distinct methods for presenting collision avoidance information to a flight crew. They include: modified instantaneous vertical speed indicator (IVSI); light emitting diode (LED) display; and, cathode ray tube (CRT) display. The modified IVSI is the only test display that integrates the collision avoidance function with preexisting cockpit instrumentation. Modifications to the standard instrument added illuminated red arrows for all positive collision avoidance commands (climb, descend, turn right, turn left), lighted yellow indicators for negative horizontal commands (don't turn right, don't turn left), and lighted yellow arc segments for commands that restrict the aircraft's rate of ascent or descent.

Combinations of LEDs make up the arrows and command bars on the display, and each arrow or command bar is tied back to a specific pin on the input jack. Since simple, inexpensive relays were not available for the PDP-11/34 computer, an interface box was developed to translate an asynchronous character stream into voltages on specific pins or sets of pins. The transmitted characters are actually coded bit sequences representing arrows or command bars required to form the desired command.

The LED display used in the simulation stands as the first application of this technology in an air transport aircraft cockpit (Fig 3). The device is a 3-color display that provides traffic advisory messages and collision avoidance commands. The display is capable of producing up to 40 characters or symbols arranged in four lines of ten characters each. The LED display, developed by Litton Aero Products, accepts asynchronous transmissions directly from the standard computer asynchronous interface. Forty-nine characters are transmitted. The first three and the last two characters frame the 40-char message. The remaining four characters provide color control for each line according to the type of message that is being displayed. Traffic advisories are displayed in green, negative and limit vertical commands in amber, and positive commands in red. The traffic advisories are abbreviated to form a 10-char message consisting of intruder bearing, range, heading, and altitude. For instance,

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"Tektronix' IGL software the first day. Its modularity current and future

Strathclyde University's Architecture and Building Aids Computer Unit (ABACUS) uses computer graphics to instantly appraise the consequences of building design decisions. Tektronix color graphics and Interactive Graphics Library (IGL) software are playing an increasingly crucial role.

Bill Gardner
Research Fellow, Architecture and Building Aids Computer Unit, Strathclyde University, Glasgow, Scotland

For ten years, ABACUS has utilized Tektronix graphics in displaying spatial, functional, environmental and economic effects of design alternatives. Their research has led to special design packages for school, hospital, air terminal and housing projects — including participatory programs in which the building users themselves help develop layout strategies.

Now ABACUS has literally added whole new dimensions to its pioneering efforts, with the adoption of the Tektronix 4027 Color Graphics Terminal and segments of the new Tektronix Plot 10 IGL.

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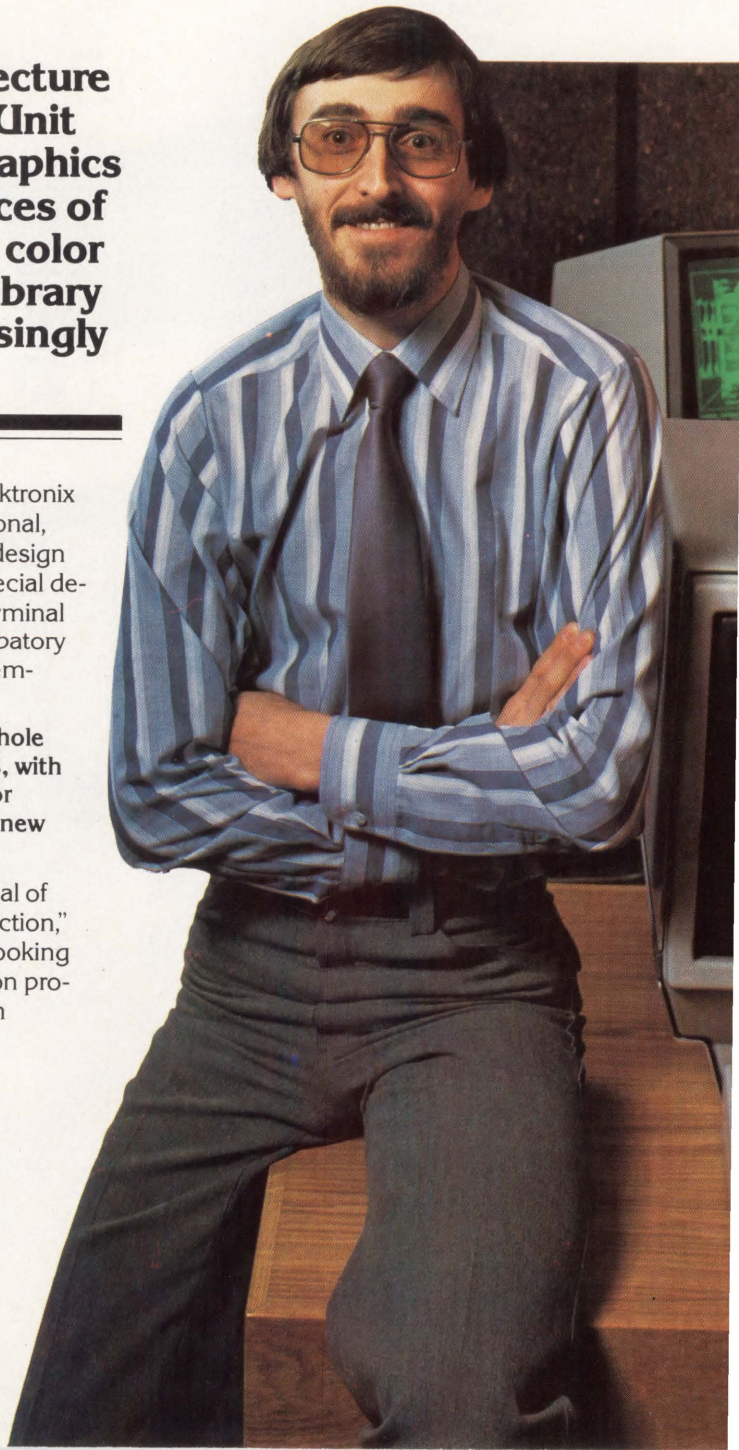

was up and running
can keep it running on all our devices."

Because IGL is completely device independent, ABACUS will be able to add new equipment, and even emulate color graphics on its monochrome terminals, without rewriting code. In addition, IGL's easy-to-read manuals and highly-acclaimed HLS color selection system have made working with shades and combinations of colors easier to learn and remember than ever before. HLS, too, will be a permanent point of reference no matter how the technology evolves.

"Simple yet powerful capabilities like these," says Gardner, "will let architects graphically design and integrate everything from carpets to working conditions, while keeping a firm grasp on capital and running costs."

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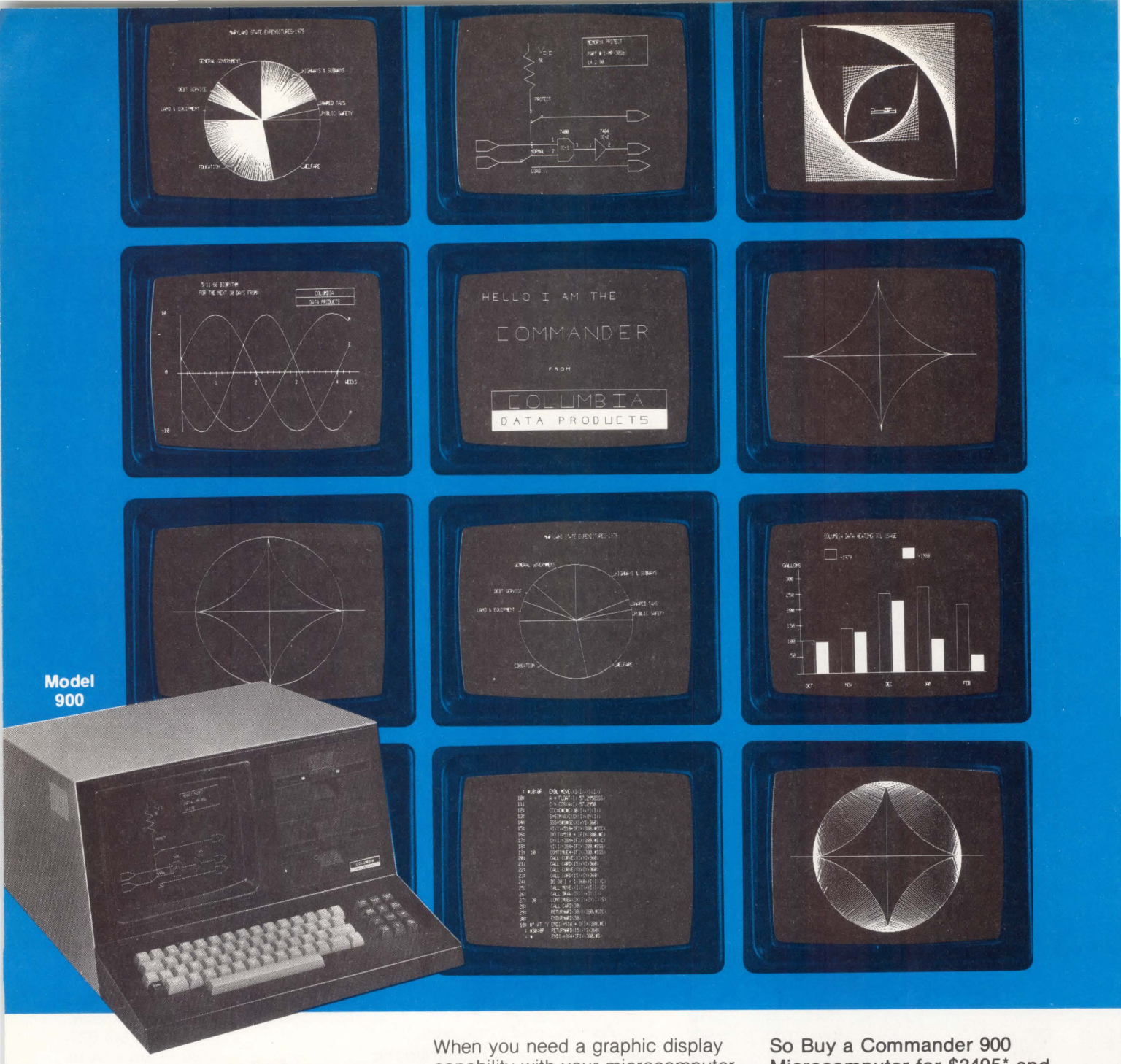

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CIRCLE 45 ON INQUIRY CARD

Fig 3 indicates traffic at 12 o'clock, 2 mi (3.7 km) away, southeast bound, at an altitude of 6100 ft (1.9 km). The pilot is told to descend to avoid the other aircraft.

The CRT display combines symbols and alphanumerics in a graphical presentation of the conflict situation. The display is heading oriented and centered on the aircraft to present the same view that the pilot would see when looking out of the cockpit window. A small aircraft symbol represents the cockpit simulator. A numerical data block positioned to the left of the aircraft symbol provides simulator altitude in hundreds of feet. The aircraft symbol is surrounded by range rings that correspond to ranges of 3 and 6 nautical miles (5.6 and 11 km). An aircraft that violates cockpit simulator airspace is symbolized by a ring of dots. Present and previous aircraft position is represented by a trail of dots that begins at the center of the aircraft symbol. To the right of the aircraft symbol is a numerical data block containing the aircraft altitude in hundreds of feet and the altitude trend. Commands are displayed in large alphanumeric characters at the bottom of the display area.

Fig 4 shows a typical conflict situation with the cockpit simulator aircraft at 8500 ft (2.6 km). An intruder is located at approximately 1 o'clock, less than 3 mi (5.6 km) away, heading directly across the simulator's path, and descending through 9000 ft (2.7 km). Collision avoidance logic instructs the pilot to descend to avoid the potential collision. Additional traffic appears at 11 o'clock, 5.5 mi (10.2 km) away, heading toward the simulator, and climbing through 7000 ft (2.1 km).

The CRT display is actually a converted television monitor with a customized tube that provides a large display area and uses a standard video input. A computer compatible interface card provides a composite video signal from a matrix array of on/off bits representing the dots in a 256 x 256 raster scan. The on/off bits are stored in a random access memory addressed through registers on the interface card. An X and Y address into the 256 x 256 array is established, and a third register indicates whether the dot is to be lighted or blanked. Illuminating and blanking the appropriate raster dots develops an arbitrarily complex picture. A software character generator provides simple alphanumerics and symbols.

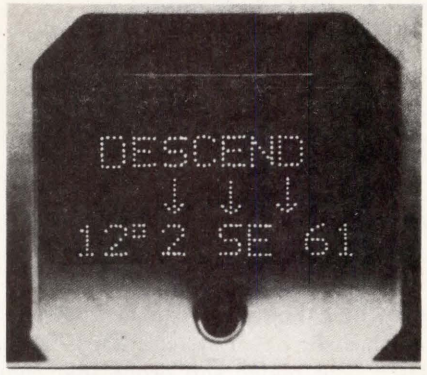


Fig 3 LED display. 3-color readout produces 4 lines of 10 characters each and stands as first application of this technology in an aircraft cockpit. Traffic advisories appear in green, negative and limit vertical commands in amber, and positive commands in red. Shown here is intruder at 12 o'clock, 2 mi away, southeast bound at 6100 ft

Fig 4 CRT display. Combining symbols and alphanumerics in a graphical presentation, display is heading oriented and centered on the aircraft to simulate pilot's view through windshield. Small aircraft symbol represents simulator. Solid ring shows intruder at 1 o'clock, less than 3 mi away heading toward simulator, and descending through 9000 ft. Ring of dots shows still another aircraft at 11 o'clock, 5.5 mi away, heading toward simulator and climbing through 7000 ft

Summary

Modern computer controlled simulators provide pilots with a degree of realism so close to that of the true flight environment that an entire pilot training program soon may be performed in cockpit simulators. By surrounding the pilot with familiar visual and aural cues, realism is maintained despite the abnormal frequency of near collision situations that develop during a typical simulated flight. Evaluation of collision avoidance issues using modern computer controlled simulators can be conducted safely and at a significantly lower cost than in an experiment requiring real aircraft.

The tests performed were successful in part because of the advantages available through simulation. The test bed incorporated an existing high fidelity cockpit simulator and nighttime visual display system. A general purpose minicomputer was selected as the simulation control computer to provide the desired and necessary flexibility in experiment design and control. The system interface was selected to provide the minimum impact possible on existing hardware and software, and the system software was designed to accommodate the realtime simulation environment. This approach provided a minimum cost, maximum return experiment.

DC & AS BRIEFS

System Monitors and Controls Crop Irrigation Channels

As many as 16 irrigation lines can be controlled by the ECH_20 microprocessor based system. Each line or "channel" includes a gold plated soil probe that continuously measures soil parameters. Data fed from the probes to the computer are evaluated by the computer, which then turns water pumps on or off depending on soil conditions.

Allowances are made for variations in temperature, sunlight, length of daylight, humidity, wind, and the moisture needs of various plants at different stages of growth. Once installed, practically no supervision or maintenance is required.

Developed by Fenlow Irrigation Ltd, 19 Baker St, Weybridge, Surrey, England, the multichannel system is modular in form. Each module is linked to four probes and up to four modules can be attached to the computer via 2-wire cable.

Soil moisture level is set into the computer for each channel. The computer scans all probes continuously until it selects a channel to be irrigated. Triggering an irrigation cycle for one channel locks out all other channels to prevent simultaneous irrigation of more than a single channel. When the soil moisture for one channel reaches its optimum value, the computer closes that line and selects the next channel to be irrigated. Automatic alarms alert the grower if excessively wet or dry conditions occur as a result of a faulty valve or a broken pipe.

Papers Invited for IECI '81

For the first time in its 7-year existence, the International Conference and Exhibit on Industrial Control and Instrumentation will be held in San Francisco (instead of Philadelphia). Again for the first time, it will take place in November rather than the usual March. However, the historical emphasis on applications of microprocessors in this field will continue.

IECI '81, sponsored by the Industrial Electronics & Control Instrumentation and the Computer Societies of the Institute of Electrical and Electronics Engineers, is planned to provide a medium for the exchange of information related to the overpowering importance of microprocessors in process control, instrumentation, and automation. Areas of interest listed in the Call for Papers include the technical aspects of designing, implementing, and testing small computer systems. Such systems might be used in manufacturing, process control, energy management, data acquisition, or a multitude of other areas. Equal emphasis is expected on software and hardware evaluations.

Abstracts of no more than 40 words, describing work not generally published or previously published, are due by Mar 1, 1981. For copies of the Call for Papers contact V. K. L. Huang, Bell Telephone Laboratories, Murray Hill, NJ 07974 (201/582-4630) or Robert A. Begun, FMC, 1185 Coleman Ave, Santa Clara, CA 95052 (408/289-3751). Suggestions and proposals for tutorial and special panel sessions should be sent by Apr 1, 1981 to General Chairmen J. D. Irwin and H. T. Nagle, Jr, Electrical Engineering Dept, Auburn University, Auburn, AL 36830 (205/826-4330).

Data Acquisition and Control Systems And Subsystems

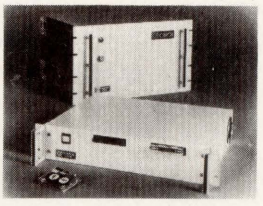
Scientific and Industrial Application Data Logger

Based on a PM 4000 compact data logger plus additional hardware and software, the PM 4001 universal data acquisition system handles up to 950 analog and/or digital inputs. IEC-625 instrument bus, parallel and serial interfaces, and the combined V24 (RS-232-C)/20-mA interface card are compatible.

The basic modular system, available from NV Philips' Gloeilampenfabrieken, Science and Industry Div, PO Box 523, 5600 AM Eindhoven, The Netherlands, holds 50 input channels while satellite units handle 100 channels each. Up to 100 m can be maintained between data acquisition unit and input devices. An output buffer allows stored data to be fed to a printer that operates at a slower rate.

Circle 440 on Inquiry Card

Mass Storage Option



As many as 64 A-D channels and/or 96 discrete signals can be monitored and data stored online with the dual-drive DEC Tape II (TU-58) cartridge subsystem for the Cinch industrial monitor and control system. Introduced by Control Logic, Inc, 9 Tech Circle, Natick, MA 01760, the optional subsystem has a capacity of 256k bytes/drive and is fully software supported by the resident, realtime, multitasking operating system. Program development is in BASIC.

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(continued on page 84)

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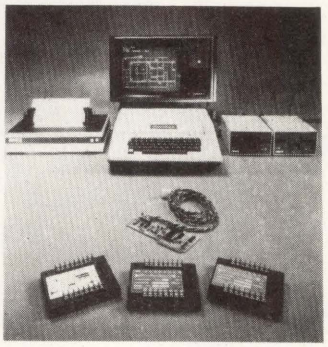

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Turnkey Computer Systems

A series of turnkey, computer based measurement and control systems introduced by Avco Electronics Div, 4807 Bradford Dr, Huntsville, AL 35805, include model 7001 for fire detection, security, and energy control in a single building; 7002 for process control, maintenance, and failure prediction; and 7003 for testing of engine performance, duration, development, production, and regulation. Model 7004 is for structural and materials testing with hydraulics control, 7005 is for remote and local equipment operation, and 7006 is for realtime analysis.

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Harsh Environment Microcomputer

An upgrade of the company's modular line, the 180+ microcomputer subsystems are intended for use in harsh industrial environments. Included are an EPROM-RAM module (1813+C) with up to 64k bytes of EPROM and 16k bytes of RAM, a bankswitched RAM module (1815+A) with up to 64k bytes, a digital output module (1828+A) for processing up to 64 outputs, a bidirectional TTL I/O module (1829+A) that processes up to 64 program selectable channels, and an analog I/O module (1850+C/1) with 16 single-ended channels.

Microcomputer modules, from Xycom, Inc, 750 N Maple Rd, Saline, MI 48176, are the 1862+B master-slave configuration containing Z80 microprocessor, up to 8k-byte RAM, up to 8k-byte EPROM-ROM, two independent serial ports, and arithmetic or floating point processor units; and the 1880+B with Z80 microprocessor, 1k-byte RAM, up to 8k-byte EPROM-ROM, serial ports, and processor unit.

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Graphic Programming System

Relay logic simplicity in the programming of microcomputers is claimed for the SPT-100 symbolic programming system. Introduced by Sibthorp Systems, Inc, 8050 Production Ave, Florence, KY 41042, the system supports Multibus and STD BUS microcomputers with the company's multitasking industrial control executive (MICE) software supplied in 16k of P/ROM. Programming is in a high level industrial graphic language (IGL).

The multitasking system has three modes: immediate for handling time relevant functions, deferred for nontime relevant functions, and interrupt for time or event critical functions. A terminal (see photo) contains monitor/debugger, editor, and compiler/decompiler software. A logic assist board, compatible with the specific microcomputer bus, processes logic operations and is claimed to reduce memory usage and speed system scan time by up to 800% over comparable software logic handlers.

Circle 445 on Inquiry Card

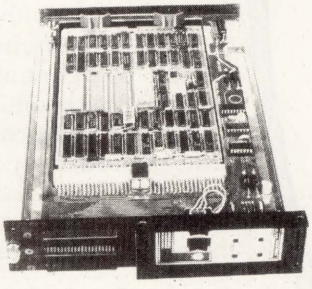
Hard Disc Option for Test Systems

Availability of a hard disc option made up of 10M-byte disc, controller, and operating system for its LM-80 and -25 process control test systems has been announced by Lomac Corp, 3052 Orchard Dr, San Jose, CA 95134. The disc is arranged into two 5M-byte platters, one fixed, the other removable for transferring programs to other systems and system backups. The controller will support up to four drives, for a total of 40M-byte storage capacity. Existing systems can be updated by a field installation.

Circle 446 on Inquiry Card

LSI-11/23 Based Controller For CAMAC Standard

The MIK-11 family of microprocessor based IEEE 583-1975 (CAMAC) standard controllers has been expanded to include the MIK-11/23. Available from Standard Engineering Corp, 44800 Industrial Dr, Fremont, CA 94538, the controller incorporates the DEC LSI-11/23 microprocessor, an asynchronous serial port that interfaces RS-232-C and 20-mA loop terminals, and a controller board for interfacing the processor to the CAMAC data bus. In addition to doubling the speed over the -11/2 predecessor, this unit addresses 128k words of resident memory (four times increase over the -11/2); supports RT-11, RSX-11M, and all DEC PDP-11 software; includes memory mapping I/O; has a 46-instruction floating point option; and supports floppy and hard disc drives. Several memory options are available.



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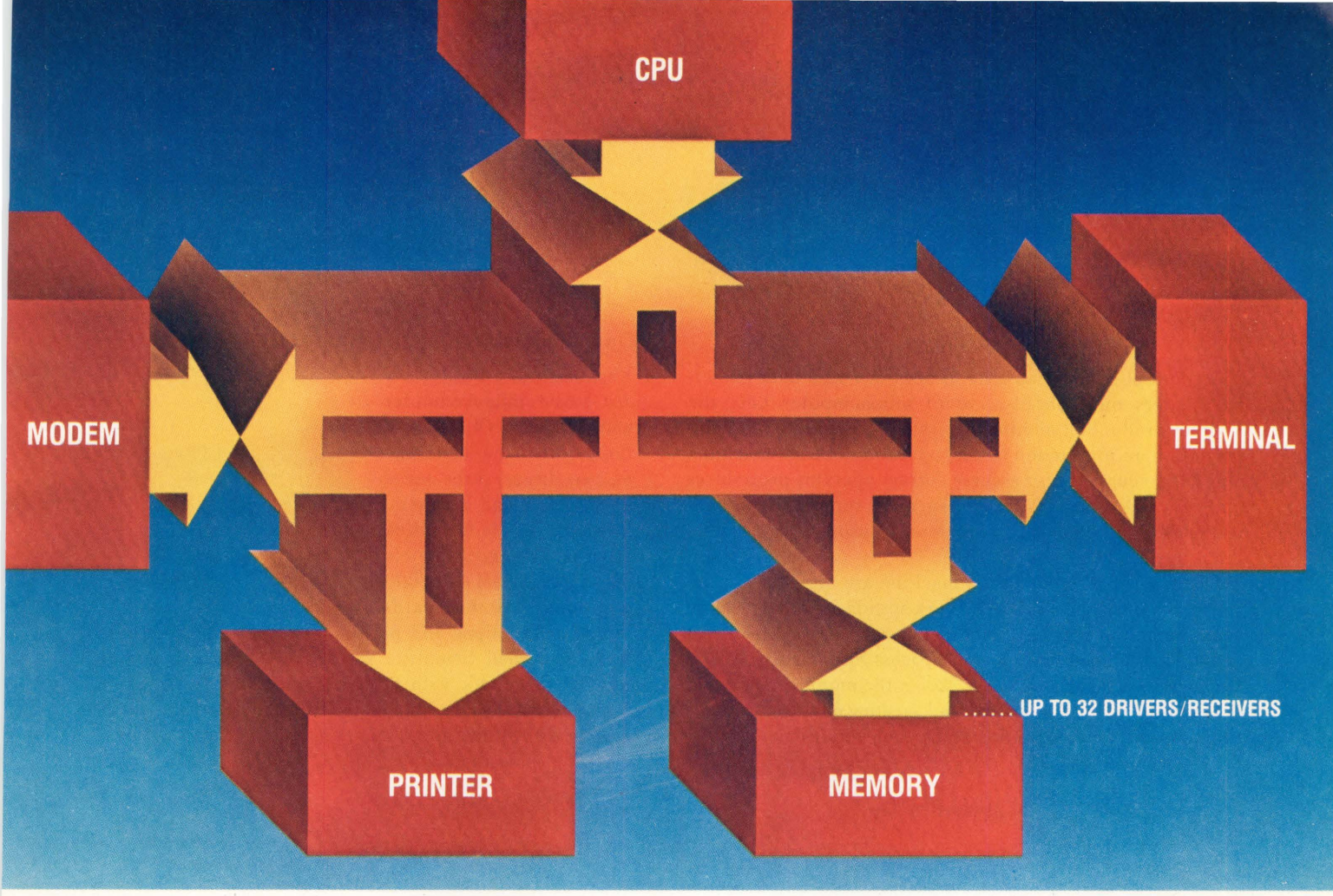

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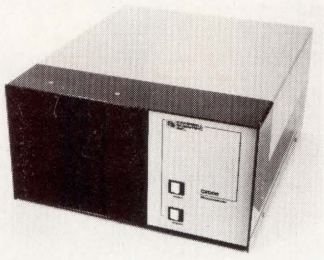
Status and alarms for each machine are displayed in the control center on a color CRT. Work station terminals enable communication between machine operators and the control center. Introduced by Logicon, Process Systems Div, 10398 Democracy Lane, Fairfax, VA 22030, the monitoring system is made up of both standard and custom modules, permitting a specific configuration to fit each requirement.

Circle 448 on Inquiry Card

Data Acquisition Microcomputer



Expansion of a basic C2000 Z80 based microcomputer with 48k of RAM, 600k of floppy disc mass storage on two drives, three serial RS-232 ports, and a cassette interface for CSI formatted tapes can bring the system up to 56k of RAM and eight additional STD BUS cards for other functions and peripherals. The system, available from Campbell Scientific Inc, PO Box 551, Logan, UT 84321, is available with CP/M disc operating system, Wordmaster text editor, extended BASIC interpreter, cassette read/write utilities, and ROM based memory test utilities. □

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Backed by Shugart experience. No matter which of our 14-inch fixed disk drives you choose, you're getting the competitive edge with the right capacity and the right price/performance. And you get great Shugart support, including a full range of technical services, product documentation, and design assistance. Proven technology, low cost, reliability, and delivery in the volume you need. That's what we're Headstrong about at Shugart.

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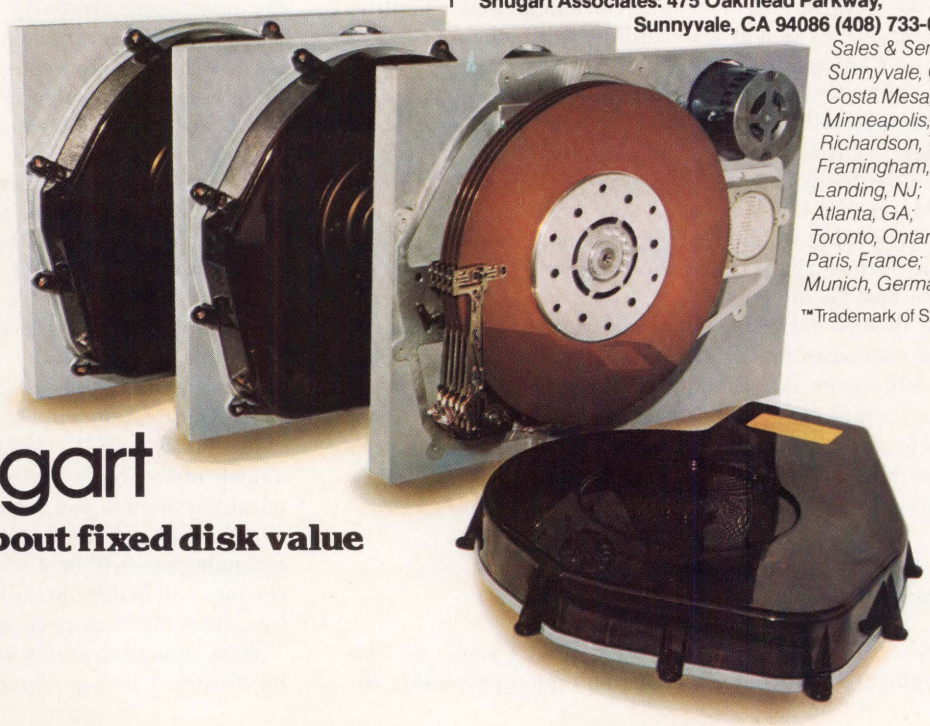

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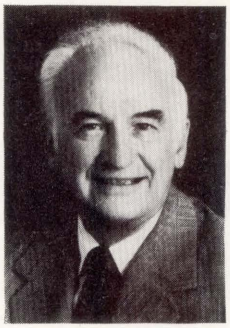
Wescon/80

Western Electronic Show and Convention
Anaheim Convention Center
Anaheim, CA
September 16, 17, 18, 1980

Allen R. Stubberud
Chairman of Professional
Program Committee



Simon Ramo
Keynote Speaker

For the first time in the 29 years that the Western Electronic Show and Convention has alternated between northern and southern California, WESCON/80 will be held in Anaheim. "Electronics, the Magic Kingdom" will be the theme of the largest WESCON in the past 20 years, as measured by the number of exhibitors and booths. All Professional Program sessions and technical and scientific presentations, as well as the exhibits, will be housed in the Anaheim Convention Center.

Although the conference officially begins on Tuesday, Sept 16, there will be a full day of preview activities on Monday, Sept 15. Among these will be the Keynote Luncheon at noon in the Disneyland Hotel's Grand Ballroom and the annual Marketing Conference, also at the Disneyland Hotel. Keynote Speaker will be Dr Simon Ramo, a founder of TRW Inc and former chairman of the President's Committee on Science and Technology.

As with most current technical electronic conferences, the largest concentration of sessions in the Professional Program will cover microcomputers and integrated circuits. Further emphasis will be on data communications, memories, and testing. Sessions will be organized this year in three blocks, starting at 9 am, noon, and 2 pm on each of the three days.

Professional Program

Advances in microprocessor technology, such as the development and introduction of 16-bit microprocessors, involve many factors. High level languages can be supported, virtual memory can be used, and system capabilities can be increased. Microprocessor sessions will include papers on these factors, as well as the programming of industrial microcomputers in BASIC, the effects of microcomputers and their abilities to increase the level of instrumentation, and the interfacing of analog functions to microcomputers for data acquisition applications. Still another session will discuss the pros and cons of single-board microcomputers: Is there any great value in putting CPU, memory, and I/O on one board—or would separate boards be simpler, cheaper, and equally effective?

Two sessions will involve home/personal computers, one from a technical angle, the other involving applications. Discussions will include the evolving of what was initially intended to be a device for the home market into an aid for small businesses. Further discussion will be on recent developments that make such computers more economical, powerful, and useful.

Integrated circuits will be approached from many directions. One session will cover the testing of complex LSI circuits—RAMs, codecs, bubble memories, gate arrays, and analog microprocessors—each of which has different electrical parameters and requires different test methods. Gate array LSI chips—including ECL, IIL, and I^3L technologies—will be discussed in a separate session. Other sessions will involve breadboarding, computer aided design, low power CMOS devices, and MOS analog circuits.

Data communications systems and basic components will be discussed in four separate sessions. One will cover Bell

compatible modems, multiplexing, and transmission methods; another will describe four specialized ICs—subscriber line interface circuits, monolithic PCM codecs, PCM switches, and signal processing chips. Fiber optic transmission systems, technology, performance parameters, component availability, and cost tradeoffs will be covered in a separate session.

Memory sessions will include ones on non-volatile memories, applications of bubble memory in harsh environments, and memory concepts for the '80s. Automatic testing will cover IEEE-STD-488 and commercial equipment as well as emerging test strategies for digital systems. Other sessions will discuss electronics packaging, power cells, multiplexed liquid crystal displays, computer terminals, and 16-bit microprocessor peripherals.

Exhibits

Several groupings have been organized in the Convention Center so that related exhibits will be together. The South Hall will contain mini- and microcomputers and EDP peripherals; production, packaging, and test equipment; and instrumentation and control systems. Components, microelectronics, and fiber/electro-optics will be in North Hall. Components, instrumentation, production, and packaging will be in the Arena. Exhibit hours will be 9 am to 6 pm Tuesday and Wednesday, and 9 am to 5 pm on Thursday.

Special Events

The annual Marketing Conference will be held on Monday at the Disneyland Hotel from 8:30 am to 5 pm. A $25 registration fee covers this conference, the Keynote Luncheon, exhibits, and Professional Program.

A special series of sessions for electronics industry purchasing executives will be held Tuesday, Wednesday, and Thursday mornings from 10 to 11:30 at the Inn-at-the-Park Hotel. Registration for this series is included in the basic WESCON registration.

The All-Industry Reception will be held at the Disneyland Hotel on Tuesday evening. Price per person of $15 includes hors d'oeuvres, soft drinks, entertainment, and two liquor and/or wine and beer beverages.

Registration

Advance registration, at $5, is available through WESCON, 999 N Sepulveda Blvd, Suite 410, El Segundo, CA 90245 (Tel: 213/772-2965). At-conference registration is $10. In addition, exhibitors have a number of courtesy registration cards for their special customers (at no charge to the person registering) and participating companies may order "gold cards" for their employees (at a $2 charge per person to the company). □

COMPCON FALL '80

Capital Hilton Hotel, Washington, DC
September 23-25, 1980

The 31st international conference of the IEEE Computer Society, COMPCON FALL '80, will be held at the Capital Hilton Hotel, Washington, DC, from Tuesday, Sept 23 to Thursday, Sept 25. "Distributed Computing," the conference theme, will cover a wide range of subjects in 40 sessions. As in past years, a series of pre-conference, extra charge tutorials will be held on Monday.

Technical Program

With the exception of Tuesday, there will be four groups of technical sessions each day: 9 to 10:30 am, 11 am to 12:30 pm, 2 to 3:30 pm, and 4 to 5:30 pm. Nearly every group will have four concurrent sessions. On Tuesday, the Plenary Session, from 9 to 10:30 am, will be the platform for presenting the IEEE 1980 Emanuel R. Piore Award to Lawrence Rabinter of Bell Laboratories and Ronald W. Schafer of the Georgia Institute of Technology.

Distributed computing, as indicated by the conference theme, will be involved throughout the technical session organization, including management issues, user interface, and human factors. Database software, environment, methodology, data flow, performance evaluation, and research directions will be covered, as will distributed operating systems, programming languages, and multicomputer architecture.

Communications and networks, closely tied to distributed processing, will be thoroughly discussed. Some of the sessions will involve network architecture for distributed computers, local computer networks, switching techniques, operating systems, testing, and applications.

Other subjects of interest will include VLSI chips and processor architectures. A panel debate on Tuesday evening from 7 until there are no more arguments to be presented will be on "The Cartesian Programmer vs The Hacker."

Pre-Conference Tutorials

Four special tutorials, each on a different area of technology, will be presented on Monday starting at 9 am. Registration can be either separate or as part of a package including the conference.

"An Overview of Distributed Processing" will include a general introduction to computer networks and define the areas of point of use systems, resource sharing networks, and multiple-processor systems. The presentation by Burt H. Liebowitz of International Computing Co will cover characteristics, benefits, and tradeoffs for each of the areas. Among the subjects will be computer technology in distributed systems, telecommunications for geographically distributed systems, and resource sharing networks.

In "Distributed System Design" Michael P. Mariani of TRW Inc and David F. Palmer of General Research Corp will offer a procedure for the orderly treatment of design decisions as well as techniques and computer aids used in procedural steps: analysis, partitioning, allocation, and synthesis. Examples will be based on realtime systems and multicomputer simulations.

Harvey A. Freeman of Sperry Univac will present an introductory level tutorial on "Local Computer Networks." Such systems are generally owned by a single organization, cover distances of a few miles, and use a communication subnetwork. Definition of local computer networks as well as design issues, potential problem solutions, and case studies will be covered.

"Computer Communications Technology in the 80s" will review what can be expected to be the prevalent technologies of the current decade. Included will be wideband digital transmission facilities, multiple-access schemes, ring switching, and public data networks. Wushow Chou of North Carolina State University will be in charge of this tutorial.

Registration

Fee schedule for COMPCON registration is as follows

	Advance Registration (Before Sept 12)		Late Registration (After Sept 12)	
	Member	Non-Member	Member	Non-Member
Conference Only or One Tutorial Only	$ 75	$ 95	$ 85	$105
Conference and One Tutorial	$150	$170	$160	$180

A student discount fee of $25 for the conference only is available to IEEE student members who are not employed full time. Tutorial registration fees include luncheon and notes. The conference fee covers one copy of the proceedings and two drink tickets for each of the COMPCON-hosted parties on Tuesday and Wednesday evenings. Further information is available from COMPCON FALL '80, PO Box 639, Silver Spring, MD 20901 (Tel: 301/589-3386).

TECHNICAL COURSES

Course 410 • a four-day course

Digital Image Processing

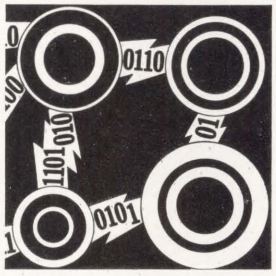
WASHINGTON, D.C.
September 16-19
SUNNYVALE
October 7-10
BOSTON
October 21-24
HOUSTON
October 28-31
ANAHEIM
December 9-12

This course covers state-of-the-art digital image processing techniques and available hardware/software options for both real-time and off-line image processing.

Topics covered include: ■ Acquisition ■ Quantization ■ Filtering ■ Enhancement ■ Compression ■ Coding ■ Feature Extraction ■ Equipment Selection ■ Remote Sensing, Image Recognition, Cartography, Facsimile and Military Applications.

Course 355 • a four-day course

Computer Network Design & Protocols



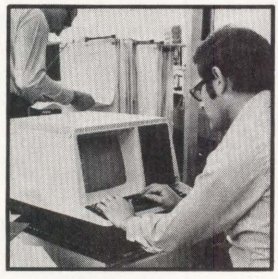
WASHINGTON, D.C.
September 16-19
SAN DIEGO
September 23-26
CHICAGO
October 14-17
BOSTON
October 28-31
SAN FRANCISCO
November 11-14

This course for design engineers and programmers emphasizes the practical aspects of network design, interfacing, protocols and packet switching.

Participants will learn how to: ■ Implement Network Communication Protocols ■ Utilize Packet and Message Switching Techniques ■ Evaluate Available Network Hardware and Software ■ Design and Build Local User Networks.

Course 340 • a four-day course

Microprocessor Software Engineering



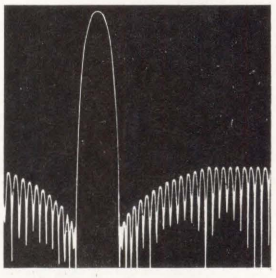
SAN DIEGO
September 16-19
WASHINGTON, D.C.
September 30-October 3
DALLAS
October 7-10
BOSTON
October 21-24
SUNNYVALE
November 18-21

This unique course develops and improves skills required to successfully manage real-time micro/minicomputer-based projects involving the design/integration of software and hardware.

Participants will learn how to: ■ Make Accurate Cost and Time Estimates ■ Increase Productivity Using Software Engineering Methods ■ Achieve Software Reliability and Portability ■ Insure Proper Software and Hardware Documentation ■ Stay Within Budget and On Schedule.

Course 412 • a four-day course

Digital Filters & Spectral Analysis



ANAHEIM
September 9-12
WASHINGTON, D.C.
September 23-26
HOUSTON
October 21-24
BOSTON
November 4-7
SAN DIEGO
November 18-21

This course provides attendees with the fundamentals of advanced digital signal processing techniques and state-of-the-art hardware/software components available for system implementation.

Topics include: ■ Mathematical Fundamentals ■ Fast Fourier Transform Algorithms ■ Finite Impulse and Recursive Filters ■ Spectral Estimation Techniques ■ General and Special Purpose LSI ■ Array Processors ■ Application Case Studies ■ Future Trends.

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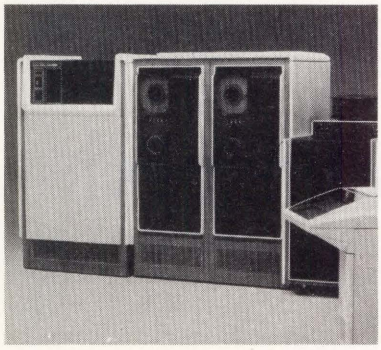
CIRCLE 51 ON INQUIRY CARD

WE SAW THE 32-BITS. AND

INDUSTRY'S RAISED 'EM.



INTRODUCING ECLIPSE® MV/8000, the fast new processor that gives you high throughput, high performance, and unmatched reliability, and the most compatible 32-bit computer system in the industry.

You need a 32-bit system that thinks fast. MV/8000's 36.4 MB/sec. memory bandwidth is two-to four-times faster than its nearest competitor. And it features a unique three-level I/O system using independent processors that drive high-speed busses and as many as 128 terminals.

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The Computer of the U.S. Olympic Sports Medicine Committee

CD 8 80

CIRCLE 52 ON INQUIRY CARD

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One board takes the place of four. In many SBC 80 based systems, the MSC 8009 can reduce the number of boards from four or more to only one. This hardware reduction helps lower system costs while increasing capability, throughput, and reliability.

Floppy disk interface. An on-board, single chip 1793™ floppy disk controller provides a soft-sector format that can be made IBM compatible. With proper options, up to eight 4 or 8 inch single or double density drives can be controlled.

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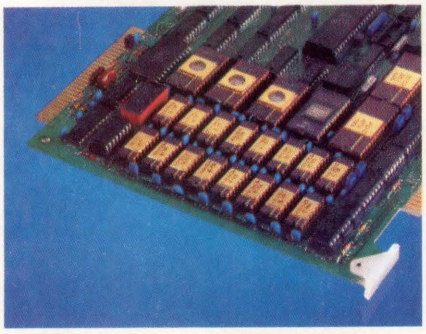

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Extensive memory capacity. The dual-ported memory can be configured with up to 32K bytes of dynamic RAM. The EPROM section is compatible with standard 1K, 2K, and 4K byte devices to a maximum of 16K bytes.

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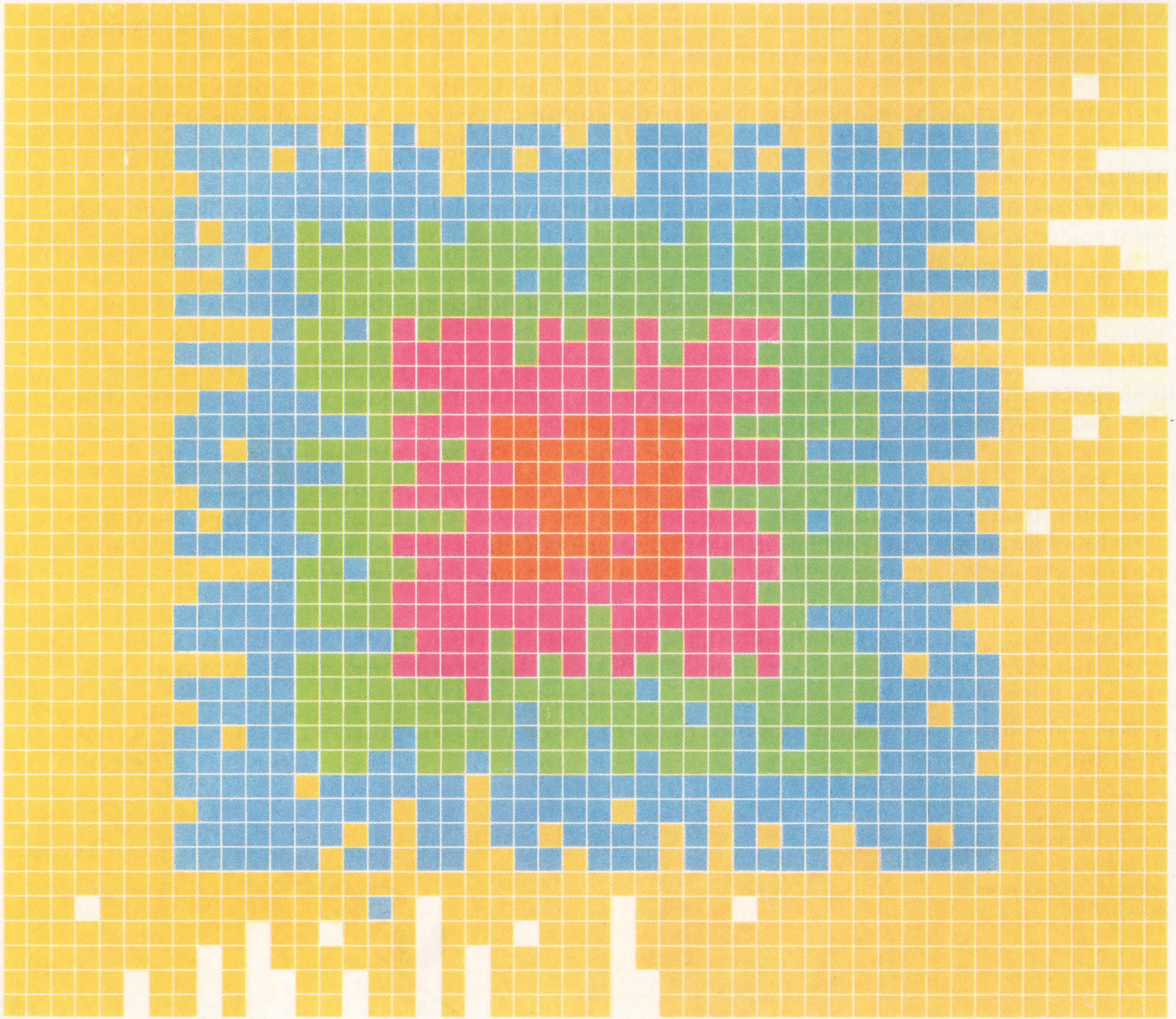

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WORD PROCESSING SYSTEM DESIGN FOR HIGH THROUGHPUT

Parallel microprocessors, fast DMA, and high speed communications multiplexer optimize throughput in a specialized application system, featuring an unusual bus design

Peter D. Cherry

Wordplex Corporation
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Modern word processing systems integrate computer and communications technologies to automate document typing, storage, transmission, retrieval, and hard copy generation. With the cost of producing an average business letter currently exceeding $6, and with the volume of documentation increasing steadily, these computerized word processing systems promise to ease typing tasks, enhance productivity, improve accuracy, and reduce costs.

Two types of word processing systems predominate: standalone systems for small volume applications, and multiterminal systems for large volume applications. Many such systems, however, merely adapt existing minicomputer equipment and software that are oriented to data processing. Systems designed specifically for multiterminal word processing supply fundamental requirements of bulk storage, high speed communication with terminals, and extensive text manipulation capability. They achieve the primary objective of efficient word processing without contending with boundary constraints imposed by utilizing an existing minicomputer product.

Word Processing Requirements

Word processing is essentially the manipulation of words and characters towards the generation of text onto paper. The critical functions of word processing are basic typing,

page layout, revision, and selective retyping; storage and retrieval of documents such as form letters, standard paragraphs, lists, or prototype reports and contracts; and fast generation of rough drafts and/or finished copy. In order to facilitate the rapid, accurate, and inexpensive completion of these functions, modern standalone word processing systems offer a microprocessor based central processing unit (CPU) for control; a video display terminal (VDT) for input and display of both text and commands; bulk online storage; a high speed character printer; and high speed communication channels.

Large, shared resource, multiterminal systems typically contain more than 12 individual VDTs, each connected to the powerful central processor and the large disc storage system. VDTs may be connected to the CPU either directly or through the telephone network and can update either local or remote files easily and rapidly. Large systems can also route messages, or electronic mail, from terminal to terminal directly or via the main CPU. The more sophisticated word processors have software and hardware, such as IBM 2741 or 2780 emulators, that communicate with large data processors and timesharing systems.

These large, shared resource systems are more efficient than standalone systems. They optimize usage of expensive shared resources, such as storage and hardcopy devices, while reducing the need for trained operators to handle storage media and output equipment. In addition, benefits accrue from the systems' ability to merge many discrete data bases, such as standalone system floppy discs, into a shared, bulk storage medium and from the software's ability to perform many of the filing, retrieval, distribution, and cross referencing tasks required to maintain a data base of finished documents.

Multiterminal word processing systems require many megabytes of disc storage, both for online file handling and for the offline file backup that guards against catastrophic system failure. These storage requirements necessitate use of at least two large, removable discs. Rapid disc access, with requisite fast direct memory access (DMA), is then a salient system design function that has a direct impact on system response time.

The importance of equipping a word processing system to produce large quantities of high quality printout is axiomatic. Commercially available daisywheel printers generate 45 to 55 char/s. However, much of the output consists of preliminary draft documents, for which a high speed line printer offering 200 to 900 lines/min may be adequate. The printers can be located remotely from terminals, but, more often, one printer is shared locally by a cluster of terminals.

CPU Design

The WPX/7 CPU supplies the high speed DMA transfers, considerable processor power, and dedicated communications input/output (I/O) processor specifically required for word processing. This CPU includes four Z80 microprocessors, up to six DMA channels, a disc controller, a microprocessor con-

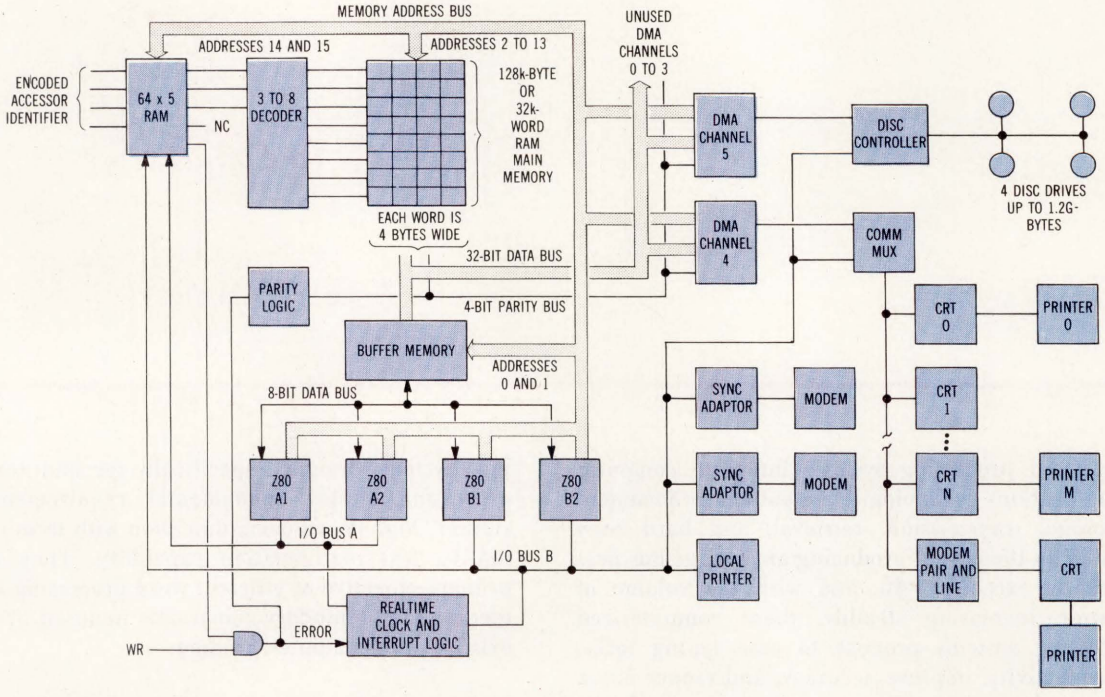

Fig 1 System block diagram. Data pass between main memory, buffer memory, and DMA channels on 32-bit data bus. Microprocessors access buffer memory via 8-bit data bus. 64 x 5 bit RAM allocates four memory pages to each accessor

trolled communications multiplexer, a potential for up to 256k bytes of memory, and a high speed buffer memory (Fig 1).

Of the four microprocessors integral to the CPU design, two (designated A1 and A2) perform application functions such as entering, changing, and manipulating text. One microprocessor (B1) controls DMA transfers, directs terminal I/O, and drives the hardcopy printers. The fourth microprocessor (B2) controls the overall system hardcopy output functions. This parallel division of word processing functions among the microprocessors enhances both speed and performance.

All of the microprocessors write directly to main memory, and all read data either from main memory or from high speed buffer memory. DMA channel controllers also transfer data directly to and from main memory. Dedicated DMA channels are allocated to the communications multiplexer and the disc controller. Additional DMA channels, each operating at up to 1.2M bytes/s, with a total, short term, peak load of 4.8M bytes/s distributed among the channels, are available to handle future expansion. The 32-bit memory data bus achieves this high data rate without significant effect on CPU operation.

Microprocessors

Because standard word processing characters are commonly handled as 8-bit data, 8-bit microprocessors such as the 8080 and the Z80 are particularly well suited to text manipulation. An earlier design of the WPX/7 CPU contained two 8080 microprocessors; by contrast, the four Z80s contained in the present design more than double the number of VDTs the system can support. The Z80 instructions are a superset of the 8080 instructions, and, in fact, the initial design software runs on the present design without modification.

The Z80 was chosen for its expanded instruction set. It defines about twice as many instructions as the 8080. For example, the Z80 has a fast block move capability that copies blocks of data up to 16k bytes in size, in only one instruction.

Input and Output

A shared resource word processing system CPU must have adequate capability to communicate with the VDTs and printers. The WPX/7 uses a high speed communications controller—the communications multiplexer—as its principal serial I/O mechanism. The multiplexer incorporates an Intel 3000, bit slice microprocessor with an 8-bit arithmetic unit and a 36-bit microinstruction word. It transfers memory data across a DMA channel to the communications channels. The multiplexer controls 24 full duplex, asynchronous communications channels at 9600 baud. Each channel can drive a VDT directly, through short haul modems at 9600 baud, or over the telephone network at lower data rates.

Although communications channels are designed to be driven by the multiplexer, they also can be controlled directly by the B1 and B2 microprocessors. This flexibility optimizes the I/O capability. The microprocessors perform short transfers, up to five or six bytes, while the multiplexer handles larger transfers.

Memory Organization

Main memory is organized into 32-bit words, rather than the 8-bit bytes handled by the microprocessors, to obtain a 1.2M bytes/s disc transfer rate and to allow concurrent operation of all four microprocessors. The DMA channels handle 4-byte transfers to and from main memory; however, at the beginning or end of a transfer, one, two, or three bytes may be written to complete the operation.

Main memory is addressed in eight pages of 16k bytes each (Fig 1). The 32-bit data bus connects to each page of memory. Six DMA channels access this bus directly, but microprocessors access the data bus only by way of the auxiliary buffer memory. The memory bus has 16 address lines for a 64k-byte addressing capability. Page select logic allocates any four pages from the total set of eight to each main memory accessor. Page allocation changes dynamically under program control. Any page can be designated read only for any specified accessor. Memory access is granted to the four microprocessors and six DMA channels on a fixed priority basis.

All transfers between the microprocessors and main memory are routed through the buffer memory, which serves two functions. It breaks the 32-bit memory data words into 8-bit bytes required by the microprocessors, and it holds all four data bytes read from main memory and

TABLE 1
Types and Combinations of Data Transfer*

DMA[1]	Refresh[2]	Main memory write[3]	Main memory read[4]	Buffer memory read[5]
1	0	0	0	2
0	1	0	0	2
0	0	1	0	2
0	0	0	1	1
0	0	0	0	2

1. DMA: (Main memory cycle)—Read or write. Uses 32-bit data bus only
2. Refresh: Cycle uses neither 8- nor 32-bit data bus, since no data transfer occurs
3. Main memory write: Initiated by a microprocessor. Uses both 8- and 32-bit data buses
4. Main memory read: Initiated by a microprocessor. Uses both 32- and 8-bit data buses
5. Buffer memory read: Initiated by a microprocessor. Uses 8-bit data bus only

*Permissible combinations of memory cycles in one 500-ns time slot

TABLE 2
Typical Memory Paging*

Main memory accessor	Physical page 0	1	2	3	4	5	6	7
B1 MPU	A[1]	-	B[2]	-	C	-	D	-
B2 MPU	A	B	C	-	-	D	-	-
A1 MPU	A	-	-	-	-	B	C	D
A2 MPU	-	B	A	-	D	-	C	-
DMA Channel 5	-	-	-	-	A	B	C	D
DMA Channel 4	-	A	D	C	-	B	-	-

1. A is memory page addressed by accessor as 0 to 16k – 1
2. B is 16k to 32k – 1, C is 32k to 48k – 1, and D is 48k to 64k – 1

*An example of memory page allocations for 6 accessors, where each is allocated 4 pages out of 8 available

makes them available to a microprocessor on demand without the need for an additional main memory access.

Main memory is refreshed in two stages, by addressing one row every 22 μs. About 18 μs after a refresh cycle, the refresh logic makes a low priority memory cycle request. If a memory cycle has not been granted, it generates a high priority refresh request 4 μs later. This technique not only ensures that memory is always refreshed at the correct rate, it also ensures that most memory refresh cycles occur in time periods that would otherwise be unused.

Buffer Memory

Buffer memory reduces the number of main memory accesses each microprocessor makes by serving as an auxiliary memory to relieve the load on the memory system. It can store 4 bytes for each microprocessor. When a microprocessor accesses any main memory board via buffer memory, the 4-byte word read from main memory is transferred into buffer memory. The microprocessor can use only one byte from this word, but there is a high probability that the next byte required by the microprocessor also will be contained within the 32-bit word held in buffer memory. The next time the microprocessor addresses main memory, buffer memory is automatically checked for the required byte. In practice, this byte is present in buffer memory better than half of the time. If it is not present, a main memory cycle is initiated.

Buffer memory is loaded only during instruction fetch operations; data fetch operations do not affect buffer memory contents. A microprocessor is forced to make a main memory cycle after it writes into the main memory a word that is currently duplicated in buffer memory. After eight consecutive buffer memory cycles the microprocessor is again forced to access main memory. These conventions make the presence of buffer memory completely transparent to programmers.

Data transfers to and from main memory always use the 32-bit data bus. Data transfers from buffer memory to the microprocessors use the 8-bit data bus and proceed concurrently with main memory transfers. When a DMA channel is using main memory, the microprocessors can be allocated two buffer memory cycles between them, as shown in Table 1. In one main memory cycle, a DMA channel can read or write four bytes of data from main memory and, in addition, allocate up to two buffer memory cycles. Thus, up to six bytes of data can be accessed during the 500-ns main memory cycle time.

Memory Paging

The 128k-byte memory is divided into eight 16k-byte pages. Each accessor has 16 address lines and is therefore allocated four pages. Table 2 presents a typical memory page allocation and, under program control, any or all allocations may be changed as needed. All memory accessors—the four microprocessors and six DMA channels—can acccess any memory location.

Microprocessor B1 performs the supervisory role of changing page allocations. It also controls the write protect logic used to prevent any particular accessor from modifying a particular page of main memory. Of the 16 memory address lines on each microprocessor, lines 14 and 15 select the particular page, or 16k-byte block. Lines 0 and 1 address buffer memory, and lines 2 through 13 select the word location within the page.

Page select logic determines the relationship between the eight physical pages in main memory and the four pages addressable by each accessor. A small, high speed, static random access memory (64 x 5 bits wide) has four locations allocated to each potential memory accessor. Each of these four locations defines, for one accessor, a page that has been assigned. Of the five bits per location, one controls the write protect logic and four define the assigned page. This provides a total addressing capability of 256k bytes, only half of which is implemented in the present system.

System Timing

The high memory bus utilization is achieved only by close attention to the overall system timing during all phases of system design. A 40-MHz crystal controlled oscillator drives a 10-stage Schottky logic Johnson counter. The counter outputs are decoded to produce the main timing signals used throughout the system. Fig 2 shows the most important of these. When any accessor requires a main memory access, it generates a request to the memory access logic. At the start of every 500-ns period, this logic examines the state of the various request lines and generates an acknowledge signal to the highest priority accessor. This gates the memory address onto the bus within 100 ns. The maximum delay within each accessor is two levels of logic before the address is set onto the bus.

Meanwhile, the memory access logic examines the requests for a buffer memory cycle and allocates a cycle to the

highest priority accessor. Because buffer memory consists of high speed registers, this entire cycle is completed within 175 ns, and the 8-bit memory bus is available when the main memory cycle is completed, 500 ns after it was initiated. If the main memory access is a read cycle initiated by a microprocessor, data are then set on the 8-bit data bus for 125 ns, completing a microprocessor main memory read cycle 625 ns after it was initiated. The last 125 ns of this cycle overlap the start of the next main memory cycle.

If the main memory access is not a microprocessor read cycle, a second buffer memory cycle can occur during the 125-ns time period A (Fig 2). During time period B, data may be written from a microprocessor to a set of latches connected to the 32-bit data bus. A memory cycle never uses the 8-bit data bus for more than 125 ns, and three different data bytes can pass across this bus in a 500-ns time period.

Each DMA channel can request a memory cycle approximately once every 3 μs. A microprocessor can access memory approximately once every 2 μs, of which, on the average, every other cycle will be a buffer memory cycle. Thus, microprocessors require a main memory cycle about once every 4 μs.

A system with two DMA channels will use, on the average, about 80% of the available main memory cycles and about 50% of the available buffer memory cycles. Naturally, short term peaks occur in the system loading. These do not affect system integrity because the low latency DMA channels have priority over the more tolerant microprocessors. In practice, efficiency of the lowest priority microprocessor exceeds 80% of the highest priority microprocessor efficiency.

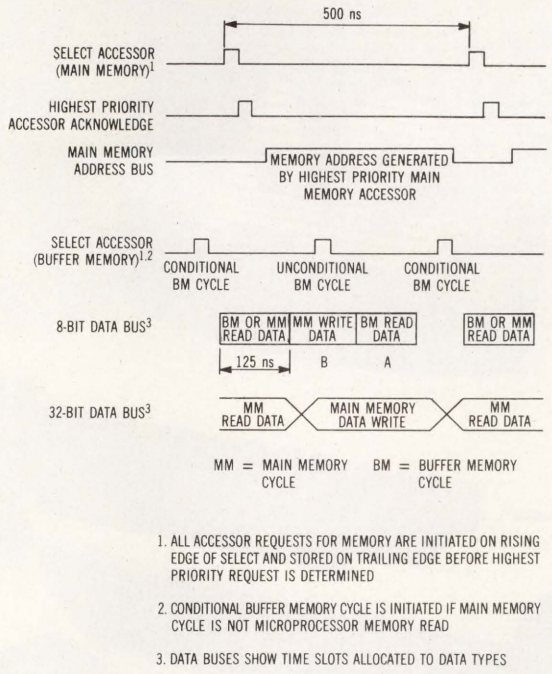

Fig 2 Memory timing diagram. Main memory has 500-ns cycle time, while 8-bit data bus runs at 125 ns. If main memory cycle is not microprocessor read request, additional buffer memory cycle can be granted

Summary

The problems in designing an economical, large scale, word processing system differ considerably from those of designing or enhancing a minicomputer system. Transforming existing minicomputer systems to serve word processing functions often results in limited and less than satisfactory performance. The WPX/7 system, designed specifically for word processing applications, achieves rapid DMA transfers between bulk storage and the CPU, as well as high speed communication between the CPU and the terminals, without impacting the considerable processor power required for shared resource word processing.

The WPX/7 system achieves reduction in the load to the memory system through the 32-bit memory data bus. The bus reduces the rate of data transfer, 1.2M bytes/s, from disc to memory system by fourfold, to one transfer every 3.3 μs. The WPX/7 system allows microprocessors to access the data bus by way of a 4-byte buffer memory, again reducing the load on the memory system as there is a high probability that one of the three unused bytes will be the one next required by the microprocessor.

Page select logic, allocation of tasks among microprocessors, and close attention to overall system timing complete application design requirements. The final design optimizes throughput in word processing applications by supplying data bandwidth in a way this specific application can best use. Thus, it achieves full benefit of resource sharing economies and far exceeds the limited performance obtained by enhancing a standard minicomputer product.

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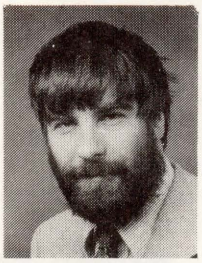

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MATRIX TECHNIQUE LEADS TO DIRECT ERROR CODE IMPLEMENTATION

A set of parity equations, expressed in matrix notation and configured in LSI, when solved, detects and corrects memory errors

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Advances in large scale integration technology have provided memory devices with speeds and densities not possible before. Moreover, memory is no longer just another component in a data processing system; it has matured to the point of being a unique subsystem with an architecture of its own. Poor performance results if care is not taken in memory design at both the component and the system levels.

Accuracy of the storage and retrieval process is an important aspect of memory system design. Many factors influence accuracy, including the nature of the storage medium itself, transmission line characteristics, and the overall electrical environment. For this reason, memory errors may be either intermittent (soft errors) or permanent (hard errors). Some errors seem to display both soft and hard properties, as in the case of those induced by alpha radiation in charge coupled device memories. Whatever the error source, data integrity must be ensured. Sometimes a technique as simple as retrying a memory access operation and comparing the new result with the old assures sufficient accuracy. Other applications require more sophisticated techniques. Algebraic coding theory provides one such means of guaranteeing data integrity; although not new, it has received a great deal of attention recently in view of the many new memory devices and memory configurations now available.

Error detecting and correcting codes generally are viewed as a direct consequence of the division algorithm. For every pair of polynomials d(x) and g(x), there is a unique pair of polynomials q(x) and r(x), such that

$$d(x) = q(x)g(x) + r(x)$$

with the degree of r(x) always less than the degree of g(x). A polynomial can be used to represent binary data by assigning each data bit as the coefficient of a power of the variable x. This method requires a division circuit, usually in the form of a linear feedback shift register, as part of the coding hardware. Depending on the time available to

perform the required shifting, parallelism may be introduced to increase speed, or memory timing may be arranged to allow for the necessary operations.

A parity check matrix provides the conceptual basis for an alternative to the division algorithm for error correcting codes. Composed of zeros and ones, a parity check matrix embodies a set of parity equations that must be satisfied whenever data are checked. Combinational logic can implement the equations, making speed a function only of delay time through the gates. Parallelism, or a byte oriented access technique, is preferred in this approach. Use of logic arrays or read only memory (ROM) achieves compactness and improves delay time. Further, such implementation lends itself to custom large scale integration (LSI) design.

The Hamming (15, 11) code will be used as an example to establish basic concepts. This code was chosen because it is long enough not to be trivial and yet short enough to allow enumeration of results. The Hamming code is presented as a set of equations. These are then formulated and examined in terms of vectors and matrices.

Parity Equations

Odd or even parity tells whether there is an odd or an even number of ones in the binary string. Sometimes, as a check, an extra bit may be added to enforce the desired parity. Expressing this concept in vector form for the 15-bit vector $(a_1, a_2, \ldots, a_{15})$ with odd parity gives

$$a_1 + a_2 + \ldots + a_{15} = 1$$

to indicate that the modulo 2 sum of bits in the string is odd, the condition for odd parity. This is most often implemented as a flipflop toggled by ones in the serial data.

Checking only certain bits for odd or even parity extends the concept a step further. The set of parity equations in Fig 1(a) reflects four such possibilities for a 15-bit binary string. Sums p_0, p_1, p_2, and p_3 can be visualized as forming a parity vector. All 0s, or even parity, is the desirable condition for this vector; hence, the vector 001001011100010 gives zero sums and satisfies the set of equations, as verified in Fig 1(b).

Next, suppose one bit, the tenth, is altered from a 1 to a 0. The new string, 001001011000010, yields a nonzero parity vector of value 1010_2 when applied to the four parity equations [Fig 1(c)]. It is no coincidence that this value not only flags the error but also identifies the erroneous bit. Altering the sixth bit instead of the tenth produces parity vector 0110_2. In fact, no matter which bit is in error, the parity vector reveals existence of the error and identifies the erroneous bit.

$$\begin{aligned}
a_1 + a_3 + a_5 + a_7 + a_9 + a_{11} + a_{13} + a_{15} &= p_0 \\
a_2 + a_3 + a_6 + a_7 + a_{10} + a_{11} + a_{14} + a_{15} &= p_1 \\
a_4 + a_5 + a_6 + a_7 + a_{12} + a_{13} + a_{14} + a_{15} &= p_2 \\
a_8 + a_9 + a_{10} + a_{11} + a_{12} + a_{13} + a_{14} + a_{15} &= p_3
\end{aligned}$$

(a)

$$\begin{aligned}
0 + 1 + 0 + 0 + 1 + 0 + 0 + 0 &= 0 \\
0 + 1 + 1 + 0 + 1 + 0 + 1 + 0 &= 0 \\
0 + 0 + 1 + 0 + 0 + 0 + 1 + 0 &= 0 \\
1 + 1 + 1 + 0 + 0 + 0 + 1 + 0 &= 0
\end{aligned}$$

(b)

$$\begin{aligned}
0 + 1 + 0 + 0 + 1 + 0 + 0 + 0 &= 0 = p_0 \\
0 + 1 + 1 + 0 + 0 + 0 + 1 + 0 &= 1 = p_1 \\
0 + 0 + 1 + 0 + 0 + 0 + 1 + 0 &= 0 = p_2 \\
1 + 1 + 0 + 0 + 0 + 0 + 1 + 0 &= 1 = p_3
\end{aligned}$$

(c)

Fig 1 Parity equations. In (a), linearly independent equations produce useful parity vector based on Hamming code for 15-bit string. Sample string 001001011100010 is verified in (b) to show that parity equations are satisfied. In (c), single-bit error at tenth bit produces parity vector that both flags error and locates its position

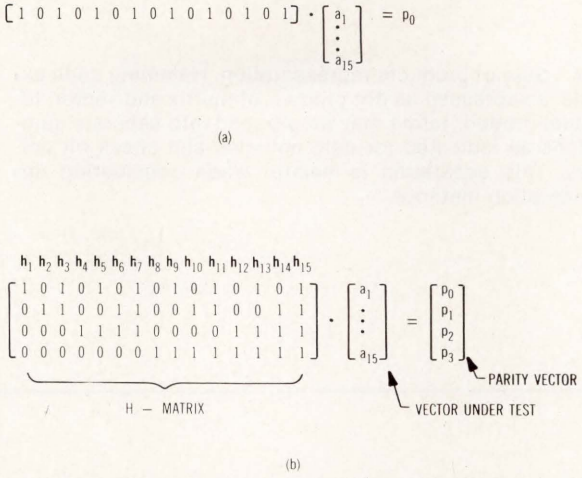

Fig 2 Dot product representation. First parity equation of Fig 1(a) is expressed as 15-element dot product in (a). It becomes first row of H-matrix, in (b), representing all four parity equations. Columns of H-matrix can be considered as vectors h_1 through h_{15}. Any 15-bit vector, **a**, applied to H-matrix, produces 4-bit parity vector, **p**. Parity vector can identify errors as well as correct them

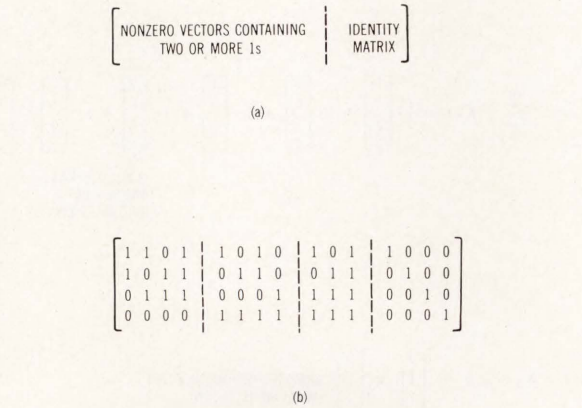

Fig 3 H-matrix standard column arrangement. H-matrix columns can be rearranged as required; however, any change affects the simple error locating mechanism of Fig 1. One standard rearrangement (a) groups column vectors to form identity matrix at end of array. In (b), specific parity equations from Fig 1 produce standard column arrangement shown when columns 1, 2, 4, and 8 are moved to end of array

A set of simultaneous equations such as those in Fig 1 suggests a matrix representation. The first of these four equations can be rewritten as a sum of products on all 15 bits

$$1 \cdot a_1 + 0 \cdot a_2 + 1 \cdot a_3 + 0 \cdot a_4 + \ldots + 0 \cdot a_{14} + 1 \cdot a_{15} = p_0$$

The dot product representation of Fig 2(a) is now apparent. When each of the remaining three equations is rewritten in this fashion, the matrix notation of Fig 2(b) can be used to represent the entire parity equation set. Here, the coefficient matrix is called the H-matrix, or check matrix, and provides the basis of the coding process. The data vector **a** is any vector under test, and the parity vector **p** is called the syndrome.

Encoding

Only fully encoded 15-bit vectors have been tested in this example so far. The actual coding problem begins with the data bits, then adds check bits to form code words that satisfy a set of parity check equations with a zero parity vector. Since each equation requires one check bit, the example uses 11 data bits and four check bits.

In the vector arrangement $a_1, a_2, \ldots, a_{15}$, there are no absolute positions for data and check bits. Considering four equations in 15 variables, the choice of data bit assignments determines 11 of those variables. The remaining four variables are check bits whose values are determined by solution of the simultaneous equations. The simplest choice assigns a_1, a_2, a_4, and a_8 as check bit positions because these bit locations occur only once. For the 11-bit information string $d_1, d_2, \ldots, d_{11}$ and the four check bits c_1, c_2, c_3, and c_4, the final code vector has a bit configuration of

$$c_1, c_2, d_1, c_3, d_2, d_3, d_4, c_4, d_5, d_6, d_7, d_8, d_9, d_{10}, d_{11}$$

If a different bit arrangement is desired, such as having check bits grouped together at one end of the data string, columns in the H-matrix can be permuted to rearrange variables in the parity equations. Fig 3(a) illustrates one way of writing check matrices. The identity matrix shown here is a square matrix of all 0s except for 1s on the main diagonal. Fig 3(b) shows the specific case of the Hamming code used in the earlier example.

Syndromes

The dot product of a recovered data vector and the check matrix, syndromes play a key role in any decoding scheme. In the H-matrix approach, their role is especially graphic. Matrix representations may be written as a linear combination of column vectors. Fig 4 applies this to the permuted example matrix. The last expression in this figure shows column summations separated into two groups acccording to multiplier type, whether data or check bit. Since this summation is a linear combination, any choice of columns is permissible for each group.

Code words are generated or checked by examining these linear combinations. For example, the encoding process can

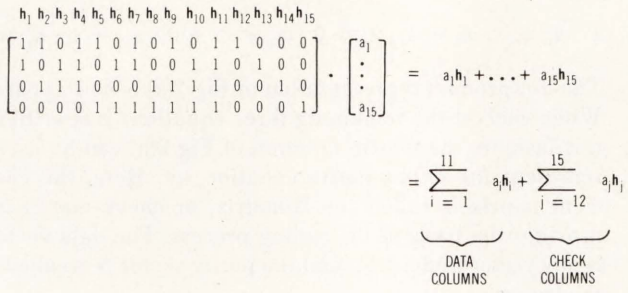

Fig 4 Sum of products representation. Hamming code example is expressed as dot product of matrix and vector. Individual product terms may be grouped into separate summations as indicated for data columns and check bit columns. This separation is helpful when considering implementation methods

be accomplished by forming the sum of the data columns and using this to determine the accompanying check bits directly. Since

$$\sum_{i=1}^{11} \mathbf{a}_i \mathbf{h}_i + \sum_{j=12}^{15} \mathbf{a}_j \mathbf{h}_j = 0$$

for all code words,

$$\sum_{i=1}^{11} \mathbf{a}_i \mathbf{h}_i = \sum_{j=12}^{15} \mathbf{a}_j \mathbf{h}_j = \mathbf{I} \cdot \mathbf{a}_i = (a_{12}, a_{13}, a_{14}, a_{15}) \qquad 12 \leqslant i \leqslant 15$$

These are the actual check bits. Had the columns of the H-matrix selected for the check locations not formed an identity matrix, the actual check bits would be found by simultaneous solution of the reduced equations.

Error Vectors

The problem of interpreting recovered data is best understood by visualizing error vectors. Briefly, an error vector is of the same length as the recovered vector with which it is associated and contains all zeros except in the erroneous bit locations. Any recovered vector, **r**, can be factored into the original code word plus some error vector, **e**. Then, the decoding process can be represented as

$$\mathbf{H} \cdot \mathbf{r} = \mathbf{H} \cdot (\mathbf{c} + \mathbf{e})$$

Now, all code words produce a zero dot product with **H** so that

$$\mathbf{H} \cdot \mathbf{r} = \mathbf{H} \cdot \mathbf{e}$$

This result indicates that statements about the properties of error correcting codes focus on an examination of error vectors. It also gives insight into the column selection nature of the decoding process. For instance, Fig 5 uses the example matrix in standard form and a code word that is recovered with an error in the tenth position. The check matrix is applied to both the received word and the error word in Figs 5(b) and 5(c). Both summations give the same result. Moreover, the error vector summation in Fig 5(c) reveals the

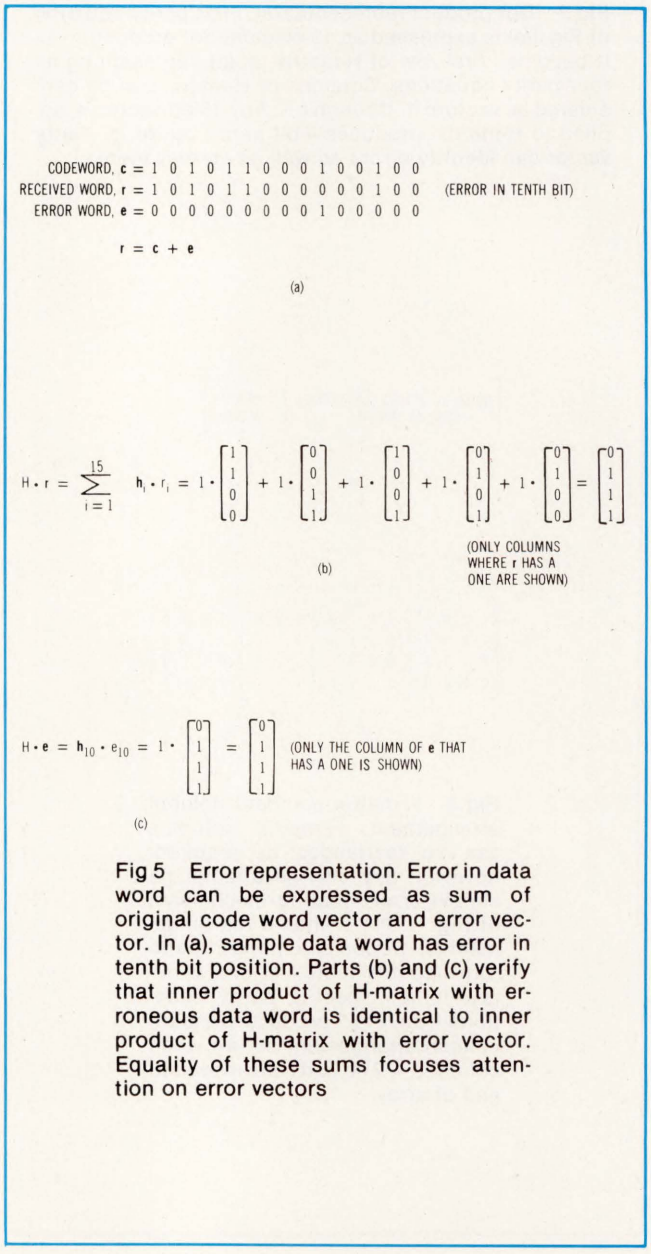

Fig 5 Error representation. Error in data word can be expressed as sum of original code word vector and error vector. In (a), sample data word has error in tenth bit position. Parts (b) and (c) verify that inner product of H-matrix with erroneous data word is identical to inner product of H-matrix with error vector. Equality of these sums focuses attention on error vectors

simple column selection technique that earlier located the erroneous bit.

On recovery of information, the syndrome is a sum of the columns of **H** at the erroneous locations. Where only one bit is in error, comparison of the syndrome with the columns of **H** points directly to the erroneous bit location. When multiple bits are in error, the analysis becomes more complex because summations of columns of **H** are involved.

Correction and Detection Properties

A valuable extension of this line of reasoning specifies the error correcting properties and deduces methods for improving them. For the example code, there are 15 distinct, nonzero syndromes that can indicate error conditions. Essentially, this means that 15 data encoding errors can be named accurately. All other errors will be mapped into this 15-element set. Specifically, all 15 possible single-bit errors can be located and corrected. However, if any multiple-bit errors occur during use of this code, their column sums will match one of the 15 single-bit sums and cause incorrect error recovery. Suppose the code is to be used as an error detector only, without error correction. In this case, the recovery circuit accepts only those words that have a zero syndrome. The false determinations will be those error patterns whose corresponding column sum is zero. An instance of this occurs in the example if the first three columns are in error. There are no instances of 2-bit error patterns that yield a zero syndrome. Therefore, this code offers double-error detection if it is not used for error correction. Enumeration of column combinations can be extended to determine error handling properties in response to three or more errors.

The picture of H-matrix methods just developed clarifies the tradeoffs involved in improving the performance of error detecting and correcting codes. If detection or correction properties are to improve, the ratio of column vectors available to syndromes resulting from error summations must increase. This can be achieved in two ways: more check bits can be added, adding more rows to **H** without adding more data, or the amount of data can be reduced for a given number of checks, reducing the columns of **H**.

Hamming codes are typically extended to single-error correcting, double-error detecting codes by adding a row of all ones to the H-matrix. The modified matrix has five check bits, allowing 31 nonzero syndromes. When it is used as a single-error correcting code, 15 of these combinations are spoken for. The added row enforces odd parity on the total word so that no combination of two columns can be 0 or equal to a column vector. Therefore, in addition to correcting single errors, this code will detect all 2-bit errors. It cannot correct double errors because there are too many double-bit error combinations to allow a unique syndrome for each. Deleting columns of the H-matrix achieves double-error correction with a Hamming code. For the example using four check bits, the number of data bits must be reduced from 11 to 1 before double-error correction can be performed.

There is opportunity to employ a great deal of sophisticated mathematics when specifying a matrix. Most codes can be described in matrix notation. A variety of valuable codes can be designed using the techniques discussed here

Vector and Matrix Representation

Coding theory attaches no significance to one end of the vector or the other in the numerical sense of high and low order positions; rather, it is the overall order or sequence of elements that matters. This ordering must be interpreted consistently.

Codes may be implemented in any prime modulus number system. Results are simplest and most convenient when the implementation number system is based on the prime number 2. As it can be verified that subtraction produces the same truth table as addition, in modulo 2 arithmetic, addition and subtraction are the same operation. Both correspond to the exclusive OR logic relationship.

Where one vector is a list of coefficients and the other is a list of variables, the dot product can be used as an alternate notation for algebraic expressions. For example, the equation

$$ax^2 + bx + c = 0$$

may be written as the product of two vectors:

$$(a, b, c) \cdot \begin{bmatrix} x^2 \\ x \\ 1 \end{bmatrix} = 0$$

Writing the list of variables as a column vector rather than a row vector is a matter of style that offers notational advantages when considering matrices.

A set of simultaneous equations can be expressed compactly as several rows of coefficient vectors applied in dot product form to a single variable vector, yielding a resultant vector. The equations below can be rewritten in matrix notation as shown.

$$6x + 3y + 2z = 12$$
$$3x + y = 6$$
$$4y + z = 7$$

or

$$\begin{matrix} \mathbf{c}_1 & \mathbf{c}_2 & \mathbf{c}_3 \end{matrix}$$
$$\begin{bmatrix} 6 & 3 & 2 \\ 3 & 1 & 0 \\ 0 & 4 & 1 \end{bmatrix} \cdot \begin{bmatrix} x \\ y \\ z \end{bmatrix} = \begin{bmatrix} 12 \\ 6 \\ 7 \end{bmatrix}$$

Solution of simultaneous equations such as these is usually discussed in terms of matrix methods. The solution is not important here; instead, it is the vector and matrix notation that matters. Elements of a vector usually are written in lower case letters. Vectors are denoted by a lower case letter in bold face or with an arrow above it. Matrices are indicated by upper case letters. Subscripting and superscripting are allowed when needed.

One additional way to visualize simultaneous equations is as the sum of products on column vectors. For the present set of equations, number the columns from left to right, and then the equations can be written as

$$x \begin{bmatrix} 6 \\ 3 \\ 0 \end{bmatrix} + y \begin{bmatrix} 3 \\ 1 \\ 4 \end{bmatrix} + z \begin{bmatrix} 2 \\ 0 \\ 1 \end{bmatrix} = \begin{bmatrix} 12 \\ 6 \\ 7 \end{bmatrix} = x\mathbf{c}_1 + y\mathbf{c}_2 + z\mathbf{c}_3$$

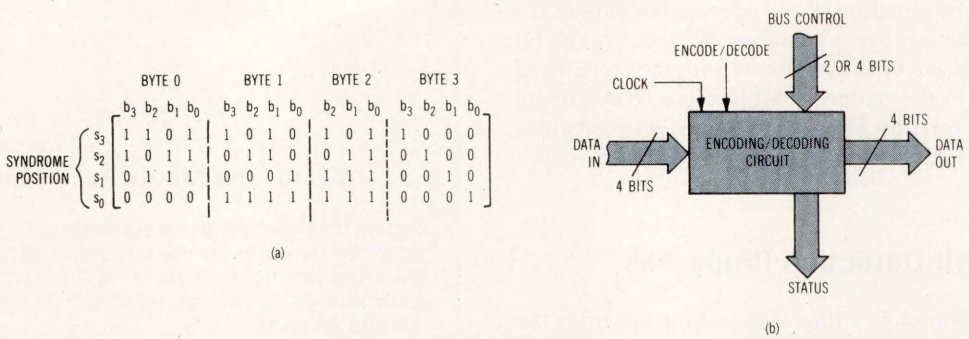

Fig 6 Sub-matrices based on 4-bit channel. In (a), matrix is partitioned with data bit assignments as shown. S_0 to S_3 indicate syndrome bit positions. Part (b) shows a general interface with signal descriptions that might implement this example

simply by modifying Hamming codes to fulfill a particular requirement. In general, a Hamming code for any word length $2^m - 1$ affords $2^m - m - 1$ data bit positions for single-error correction. Error correction capability can be increased at the expense of data locations.

Circuit Design

As is frequently the case in algebraic coding theory, the mathematics of error correction immediately suggest a hardware configuration. The typical application in a memory design involves a channel of some width less than the code word size. This channel width, called a byte, may be said to partition the matrix. Fig 6(a) illustrates the code from the ongoing example applied to a 4-bit byte. It does not matter that the code length (15 bits in this case) is not evenly divisible by the channel size. Unused bit positions are taken as zeros and can be designated as don't cares in device configuration. Fig 6(b) shows an encoding block interface providing data input and output ports, perhaps sharing the same bus, and control inputs that determine the encoding function and data activity. Status outputs may indicate correctability of any errors that exist or flag a

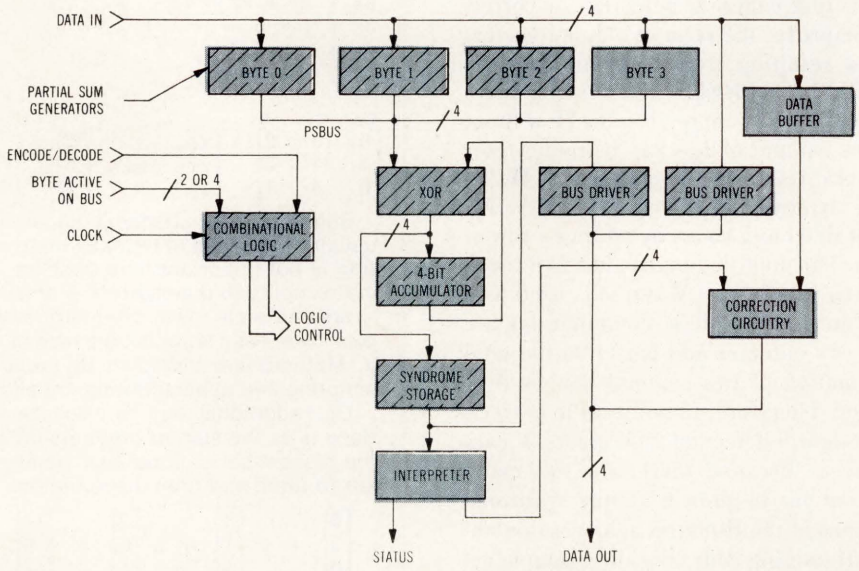

Fig 7 Circuit block diagram. Complete circuit applies example code to 4-bit data channel. Shaded areas are encoder components, also common to the decoder. Each block corresponds to a standard MSI logic package; entire diagram reflects LSI device. Components labeled $byte_0$ through $byte_2$ are 16 x 4 ROMs. Interpreter is 64 x 4 ROM

ROM Data for Standard Matrix Example

Encoding ROM Data													Interpreter ROM Data															
				Byte 0				Byte 1				Byte 2				Syndrome				Byte 0				Byte 1				Byte 2				Byte 3			
b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	A_5	A_4	A_3	A_2	0	0			0	1			1	0			1	1		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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0	0	1	0	0	1	1	0	1	1	0	1	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	1	1	1	0	0	0	1	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	0	1	0	1	0	0	1	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	0	1	0	1	0	0	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	1	0	1	1	0	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	0	0	1	1	0	0	1	0	0	1	N/A				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	1	0	0	1	0	1	0	1	0	N/A				1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	1	0	0	1	0	0	N/A				1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	1	0	0	0	1	1	1	N/A				1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	1	0	0	0	1	1	0	1	1	0	0	N/A				1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	1	1	1	1	N/A				1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	1	N/A				1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	0	0	0	1	0	N/A				1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

multiplicity of errors. The block, as developed here, suggests a single LSI function chip.

Fig 7 shows a circuit diagram whose component blocks can be either medium scale integration (MSI) devices or sections of some integrated design. The shaded portions indicate parts used during the encoding operation. In order to encode the 11 data bits, each byte appears on the input data lines and addresses the appropriate partial sum generator, a ROM that contains all possible column sums for the input data. In the case of bytes 0 and 1, there are 16 outcomes, and there are eight outcomes for byte 2. Simple combinational logic gates ROM outputs onto the PSBUS.

Outcomes for the example matrix are enumerated in the table, a listing of Fig 7's ROM content. Bits on the input data bus address each ROM. Bit weights are shown in the left column of the table and ROM outputs are indicated for each byte of input under the appropriate heading. Since an identity matrix determines the outcome for the third byte, its ROM may be replaced by a buffer/driver. The PSBUS loads one side of an exclusive OR whose other input is the accumulated summation. Adding successive partial sum ROMs to the existing summation produces a total sum of products, whether encoding or decoding. The parity byte summation during decoding reflects the only difference between these

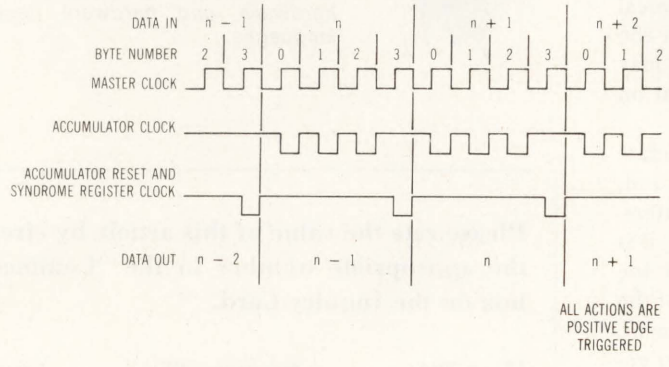

Fig 8 Circuit timing diagram. MSI logic implementation allows continuous data flow with error correction accomplished on the fly. Accumulator clock illustrates first three bytes of word being summed, with final summation being placed in storage register directly. Accumulator is cleared, during final byte addition, in preparation for first byte of next data word. Stored syndrome is available to interpreter as page address during processing of subsequent input word

two operations. In either case, the last accumulation is saved in the syndrome store so that the accumulator may be cleared in preparation for continuous data flow. While encoding, the input data may pass directly out through a driver. Then, when all three information bytes have been processed, the check bits may be placed on the output data lines. During decode, the input data can be stored for correction in a buffer. Convenient buffer configurations include stacks and parallel storage.

The syndrome exists in the storage register once four bytes have been received. Since there are only 16 possible interpretations of the syndrome, it, too, can be decoded using a ROM. Exact format of the interpreter will depend upon the buffering technique. Suppose a first in, first out stack is used so that continuous flow of data can be maintained. The correction circuit is a 4-input exclusive OR, and the interpreter is a 64 x 4 bit ROM (64 x 5 to add a status bit) that associates one correction byte with each of the four received data bytes. The table also shows the content of the interpreter ROM. The syndrome addresses one of 16 pages, and the bus byte count selects individual bytes. Note that no more than a single 1 appears in any row of the table, except for the row addressed by the zero syndrome. This isolated 1 locates the erroneous bit.

Timing for several words of the decoding operation is illustrated in Fig 8. The cycle actually begins in byte 3 of word $n-1$, when the accumulator is cleared. Three bytes are then clocked to the accumulator, followed by parity. The last summation is saved and the accumulator is cleared for the next word. The saved syndrome is a line address to the interpreter ROM whose outputs change with the byte count. Data move out of the buffer through an exclusive OR correction circuit that performs correction, if possible, using the interpreter bytes. The result may be placed directly on the data output lines.

Hardware Implementation

There are, perhaps, five general tasks that occur in any hardware implementation involving error correction. Various tasks are partial sum generation, syndrome accumulation, control, error correction, and syndrome interpretation. The storage buffering process is included with error correction, since there would be no need to save the data if correction were not performed. Partial sum generators are linked in size to the byte size of the channel. Typical sizes of eight or nine bits result in realistic ROM sizes of 256 or 512 words, respectively. Larger bus sizes, say 16 bits, may be broken into pieces and summed prior to placement on the PSBUS.

The accumulator must be large enough to accommodate the syndrome. That size is also the PSBUS size and, therefore, the ROM data size of the partial sum generators. Since the information columns of H may be rearranged, it is sometimes beneficial to arrange columns so that zeros line up in one row of a byte. This forces a zero on that line of the ROM, thereby narrowing the ROM output size requirement. There are numerous tricks and tradeoffs of this nature; unfortunately, discovery of most of these requires considerable insight into the matrix behavior.

Summary

Error detecting and correcting codes are typically implemented as a consequence of the polynomial division algorithm. An alternative viewpoint, the H-matrix perspective, suggests a matrix representation that is ideally suited to ROM based implementation. This approach is especially advantageous for use with relatively short blocks of data as, for example, when reading and writing random access memory.

Attention to the specific details of an ongoing example traced through complete development of the H-matrix perspective gives further insight into system behavior and potential design techniques. Overall, the procedure is essentially unclocked, very fast, and conducive to implementation as a single LSI device.

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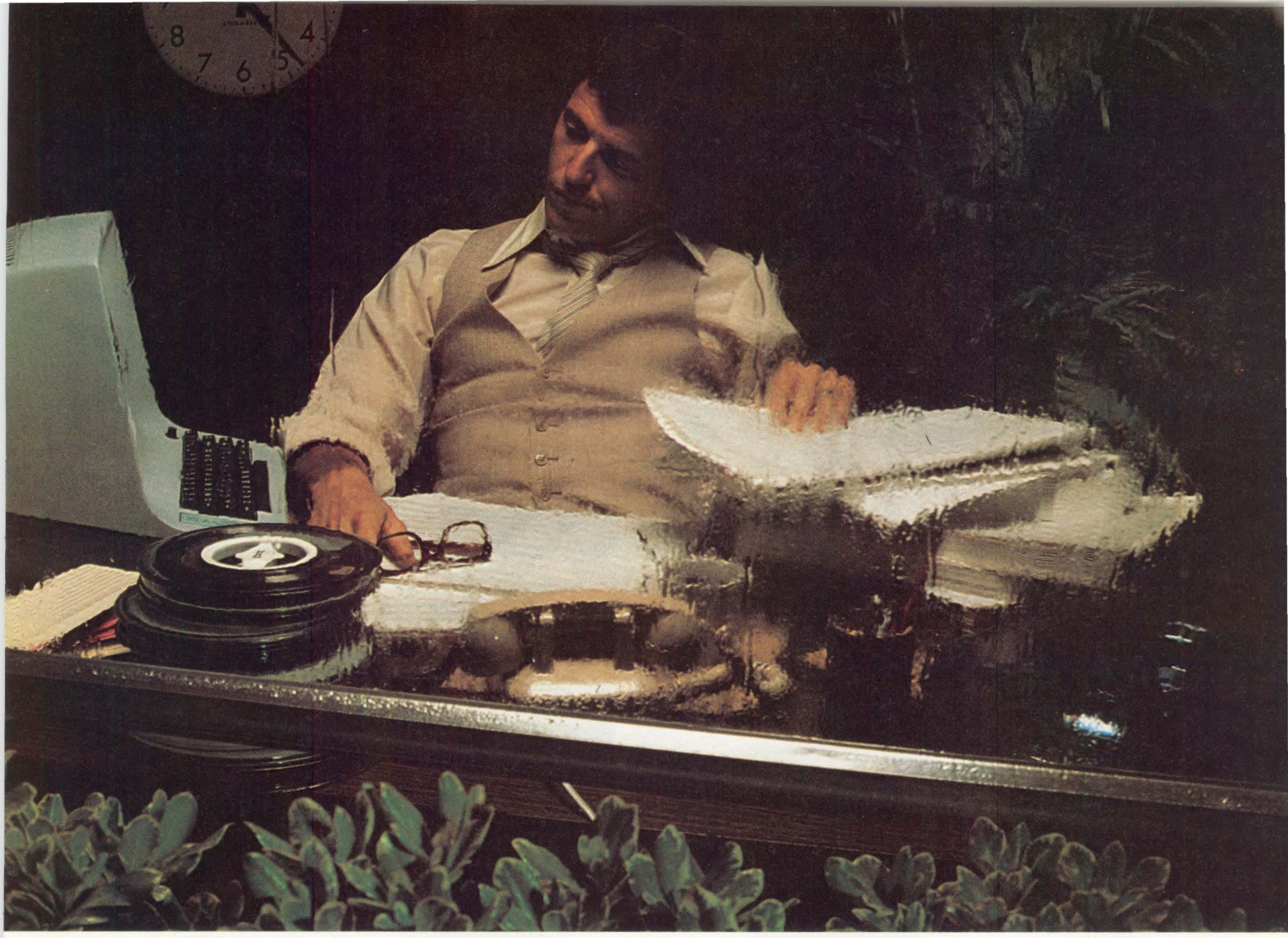

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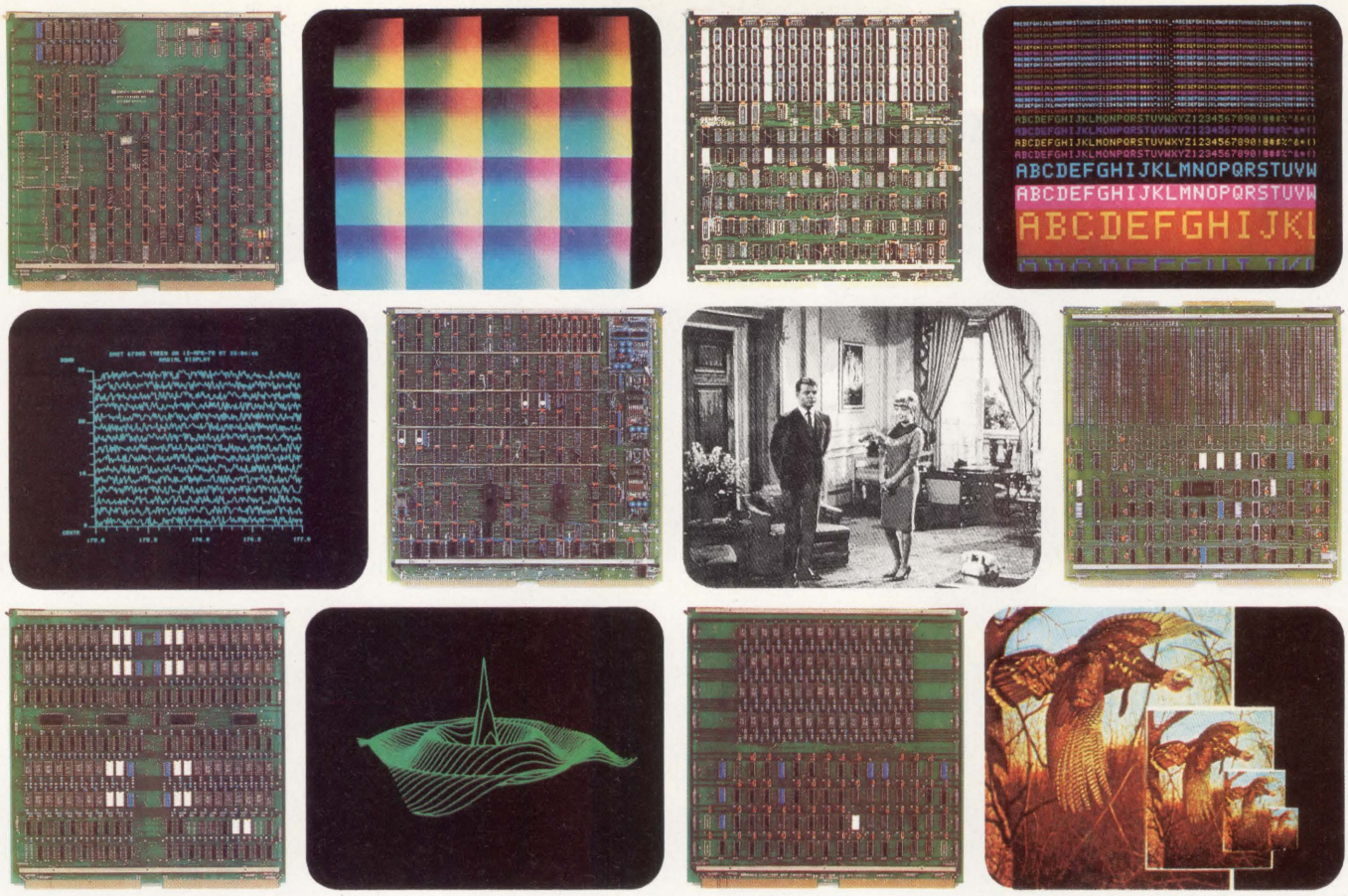

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INDEXED MAPPING EXTENDS MICROPROCESSOR ADDRESSING RANGE

Memory mapping unit functions as a memory system component but is accessed as an I/O device to increase program or data storage and allow dynamic allocation of variable size memory blocks with minimal overhead in multiprocessing applications

Ian LeMair

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5005 E McDowell Rd, Phoenix, AZ 85008

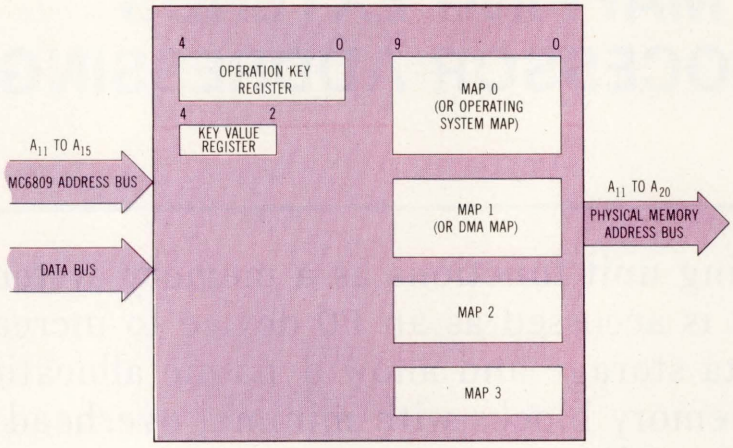
Dramatic declines in the price of memory, the increased use of high level languages, and the availability of high performance 8-bit microprocessors have resulted in application demands for expanded microprocessor system storage. The price of memory at nearly 0.02¢/bit and the price of 8-bit microprocessors under $15 when purchased in quantities, has increased interest in applying microprocessor based systems to minicomputer type tasks. Use of structured high level languages also makes adding new modules to programs an attractive and relatively easy way to augment or expand basic system capabilities. Yet, while the newer, high performance 8-bit microprocessors are capable of executing greater numbers of these complex tasks, they are restricted in their ability to store the requisite programs and data. The immediate need for more memory, coupled with the necessity for future program expandability, requires that random access memory based systems initially support large programs as well as offer the capability of adding still more memory storage as required.

Several 16-bit microprocessors have sufficient direct addressing range to support complex applications programmed in high level languages. Their chief problem is how to effectively manage the large memory space. However, 8-bit microprocessors, such as the MC6809, are limited to a 64k-byte addressing range. Therefore, problems arising from applications requiring more memory have no obvious or easy solutions, and expandability in memory intensive applications is limited severely, even though the microprocessor has sufficient computational power to support these applications.

The easiest way to extend microprocessor addressing range is by adding more address bits to the instructions; however, microprocessors have a limited number of pins available for this purpose. In addition, any functional change will drastically impact the instruction set and the architecture. Addresses are a form of data, and the largest data structures that 8-bit microprocessors can handle routinely are 16 bits in length. Adding more bits to the 16-bit address forces the microprocessor to support a data type foreign to its instruction set and architecture. For example, the addition of two address bits to a 16-bit address would mean that a processor could address 256k bytes of memory, but then it would have to operate on 18-bit data as well as load and store these alien quantities. This would have a major impact on the microprocessor architecture since it would completely change its characteristics.

Overlays

If a program with its associated data cannot fit within a microprocessor's total address space, more memory will not help unless the program can be broken up into overlays or segments. When an application exhausts available memory, a number of hardware and software alternatives would allow for memory expansion. A typical solution assigns an overlay area in memory space. Several tasks or other data can reside



LSI Device Achieves Indexed Mapping

A memory management unit using the indexed mapping technique described in the article will soon be available from Motorola Semiconductor to support the MC6809 microprocessor. This device, the MC6829, can extend the physical addressing range of the MC6809 from 64k bytes to 2M bytes organized as 1024 pages of memory, each page containing 2k bytes. Based on HMOS LSI technology, the MC6829 offers more features than the more general approach taken in the application example of indexed mapping.

The MC6829 contains four sets of mapping registers with 32 registers per set. For many applications each set of registers can be pictured as mapping a single task. This allows for fast context switching between tasks that the processor is performing. Up to eight of the MC6829s can be connected together, providing the capability of having 32 unique tasks mapped into physical memory, each task with up to 64k bytes of memory available. Each MC6829 has a 3-bit key value register which is programmable by the processor. At system initialization time a unique key value is written into each key value register in the system. This should guarantee that no two devices in a multiple MC6829 system are in conflict when mapping logical to physical addresses.

Memory can also be shared between tasks (in increments of 2k bytes) for parameter passing and common data and program areas. By having a large number of tasks premapped, each task can be ready to take control of the system, as soon as the task is enabled. Tasks are enabled by a method that is similar to bank switching. The operating system enables a task by enabling the register set associated with that task through the use of a 5-bit operate key written into the operate key register. The first three bits identify which MC6829 chips (up to eight) by comparison with the key value, while the next two bits identify which of the four maps in the selected chip to enable. A task switch is accomplished by modifying the operate key, which can be modified only while the processor is in MAP 0. In a system, MAP 0 is reserved as the map for the operating system and is always enabled in response to any exceptions to processing such as RESTART, hardware INTERRUPTS, and software INTERRUPTS. MAP 0 would contain the addresses of the memory management unit as an I/O device as well as all other I/O device addresses, the interrupt and restart vector addresses, service routines, and the operating system itself.

Another reserved map in the system is MAP 1, which is reserved for mapping DMA transfers and is automatically enabled whenever the MC6809 makes the bus available to a DMA transfer request, whether it is a cycle stealing or burst mode of operation. When the transfer is complete, the processor will continue to operate from the map it was in prior to the DMA request.

Although the MC6829 was designed to work specifically with the MC6809, it can, with the addition of external logic, work with other M6800 family processors. The figure is a block diagram of the MC6829.

in this area on a temporary basis. Data are brought in from mass storage, as required, under control of a supervisor program, and they may or may not be returned to mass storage, following use, depending on whether they were modified during execution. If the program or other data remains unchanged after execution, new data can be brought into the overlay area without first copying the original data back into mass storage.

This overlay method, although relatively simple to implement, has serious drawbacks for many applications. Relying on mass storage devices such as disc or tape to extend memory size incurs time penalties when loading the overlay area from mass storage and, possibly, when restoring modified data to the storage medium. Also, programs execute faster when they and their data reside in memory continuously. However, overall system performance suffers when the time required to load the overlay area from mass storage is added to program execution time. This problem can be amplified when a called task requests execution of another task and the second task overlays its caller, and then, when the second task finishes execution, the first task must be restored to memory and parameters must be returned to it. An example of this occurs during recursive subroutine execution. Generally, if all programs and data can be made to reside in memory, at least an order of magnitude improvement in execution time is feasible, depending upon

the application and the technique used. Another drawback to the overlay method is that as programs and data bases expand, there is an increase in the chance of multiple calls to mass storage for transfer of programs and data into and out of memory during execution since there may be insufficient room in the overlay area for both the programs and their data.

Segmentation

Segmentation is an alternative to overlaying that allows all programs and data to reside in and be executed from memory storage. The actual range of a microprocessor's instruction set, called its logical addressing range, is restricted to 16 address lines, a logical address range of 2^{16} or 64k bytes. In contrast, the memory's physical address range is determined by the number of lines carrying an address to the memory system. For example, a 1M-byte memory requires a 20-bit physical address implemented on 20 address lines. Effective address range extension requires a mechanism to translate the microprocessor logical address into a larger memory system physical address. Picture a black box placed between the microprocessor and the physical memory. The black box takes in 16 microprocessor address lines and generates some larger number of memory system address lines, allowing expansion of physical memory above 64k bytes in size. However, even though the physical address range is larger than the logical addressing range, the microprocessor is still restricted to one segment of memory at any one time, addressing only a range dictated by its logical addressing capability. Two of several methods for implementing the black box mechanism that increases the number of lines carrying an address to memory are discussed in following sections.

Bank Switching

Bank switching selects among alternate blocks of memory (Fig 1). Mainframes and minicomputers have used this technique for many years to extend addressing range. With this method, one bank of memory is enabled while all other banks remain disabled. A supervisor program enables and disables the various memory banks and, as additional system memory is required, the supervisor can be upgraded to handle additional memory banks. Concatenating a hardware bank selector to the logical address achieves translation between logical addresses and physical addresses. The logical address acts as a displacement within the bank of memory enabled by the bank selector hardware. In order to minimize some of the inherent problems associated with bank switching, a common supervisor program, which preempts a small part of logical address space, typically is carried from memory bank to memory bank. The common supervisor program allows communication among the various banks of memory and provides for common input/output (I/O) and interrupt service routines. It also makes possible the easy switching from memory bank to memory bank, since the supervisor can execute from and control programs running in all of the different memory banks.

Bank switching is an excellent and economical method for expanding the address range of a dedicated microprocessor with only a single user. It is also an excellent method for expanding systems with several users if the individual user memory allocations are assigned by the programmer and fixed in size for all users and programs. Drawbacks are evident in the granularity of the memory partition (64k bytes) and the inability of bank switching to support a large number of users or a large number of concurrent tasks residing in memory at the same time, particularly when the different user memory regions vary in size.

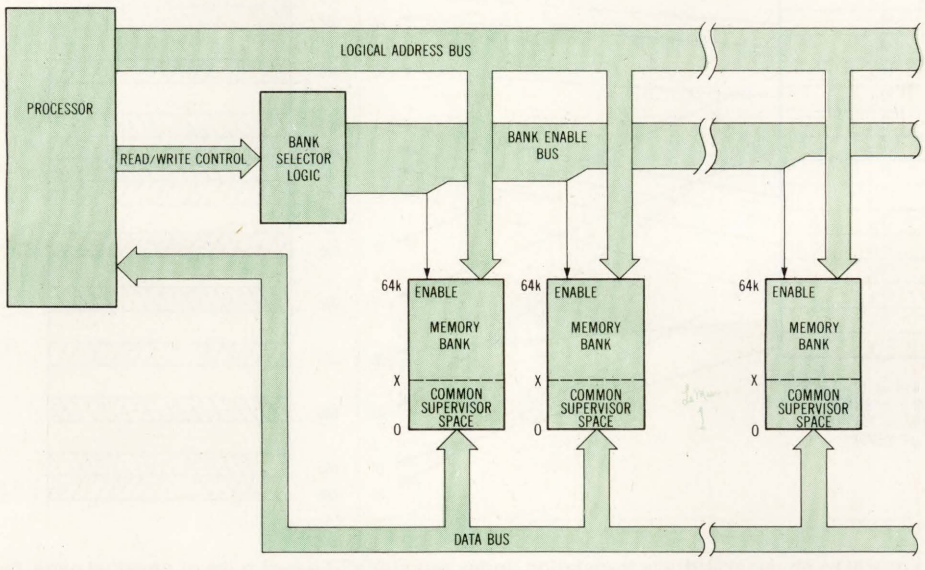


Fig 1 Bank switching. Bank selector logic enables one 64k-byte memory bank at a time. Concatenating bank selector content with microprocessor logical address produces memory system physical address. Identical supervisors occupy system area in each memory bank. Granularity is drawback, and ability to support concurrent tasks or multiple users is limited at best

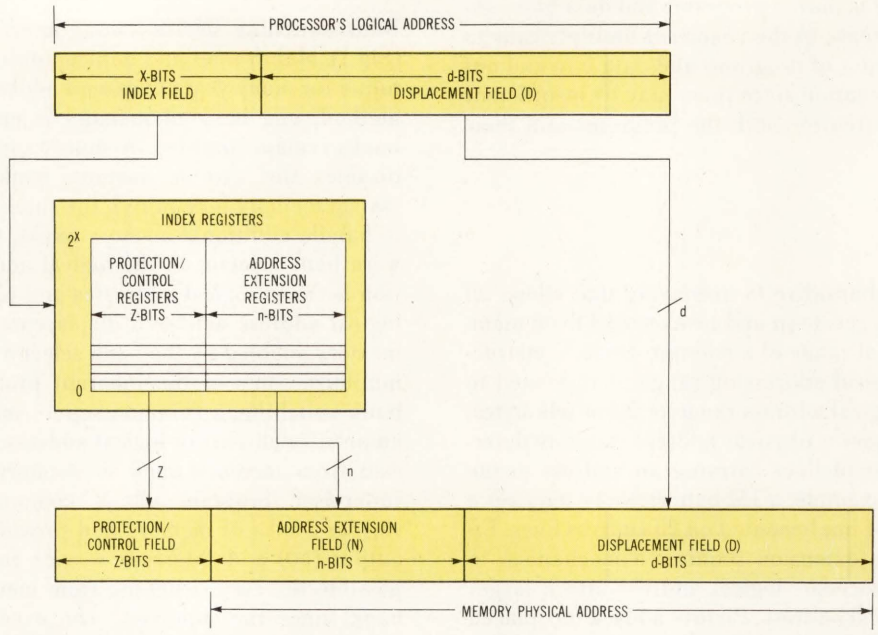


Fig 2 Indexed mapping. Use of index registers translates microprocessor logical address into potentially larger physical address. Logical address consists of index register field and displacement field. Concatenating content of designated index register with displacement field produces memory system physical address. Index register protection field offers control bits that can flag each segment, or page, as read only, read/write, execute only, and so on

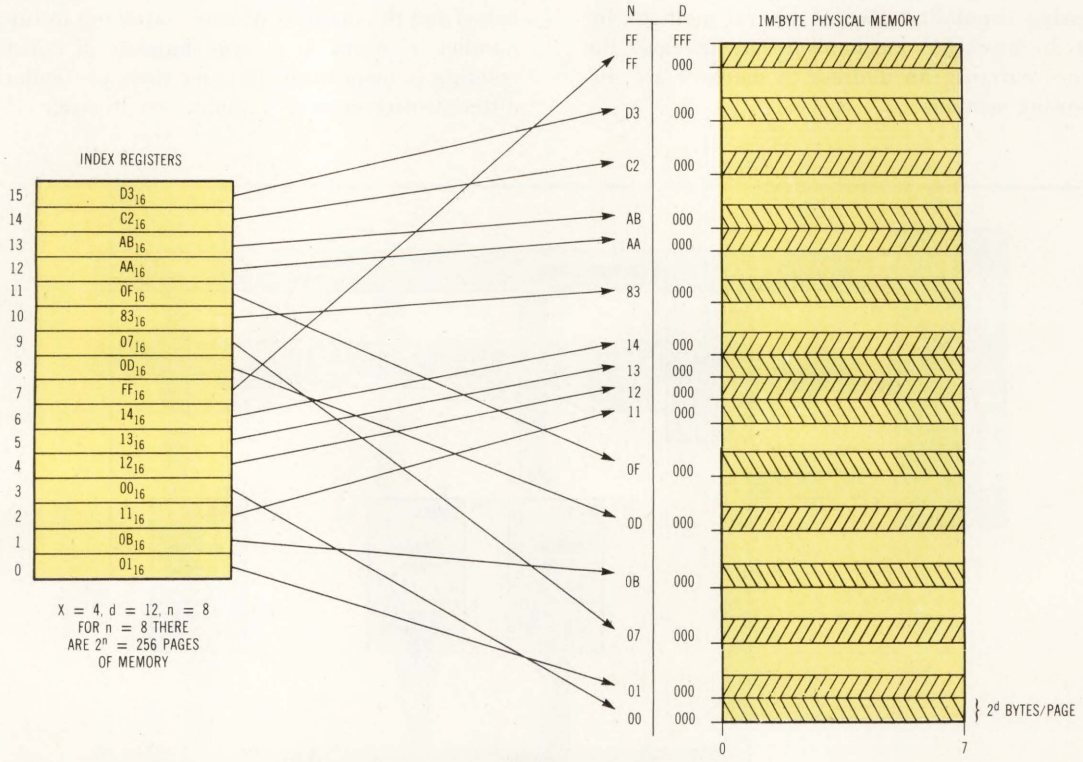


Fig 3 Logical to physical address translation. Index register addresses base of physical page. Normally, physical pages do not overlap but, as shown, pages mapped at any one time need not appear in sequence. Size of displacement field determines size of each page, in bytes. Size of index register field determines number of index registers and, therefore, maximum number of pages mapped concurrently. Product of these cannot exceed microprocessor logical addressing range

Indexed Mapping

Indexed mapping extends microprocessor address range by dividing the microprocessor logical address into two parts, a displacement field and an index field. The index field, reflecting the high order bits of the logical address, acts as an index into a high speed register file. Concatenating the content of the register selected by the index with the low order displacement field forms a physical address (Fig 2). This method also makes possible the addition of protection bits in the register file, restricting certain areas of memory, under program control, to read only access, no access, or execute only access. Even though indexed mapping does not require that a program and the program's associated data reside in a contiguous physical memory area or that these regions be assigned in sequential order, the microprocessor is still restricted to a range of addresses equal to its logical address range at any one time.

The number of bits in the displacement field determines the memory segment or page size. Typically, the pages do not overlap in memory (Fig 3). Apart from the displacement field, the number of bits remaining in the logical address determines the number of index registers. The number of bits in each of the index registers then determines the number of memory pages. To add more users or programs to an indexed memory system, new locations are added to the map table. When either a user or a program is enabled, the corresponding memory map values are loaded into the mapping hardware and the program is executed. Similar to bank switching systems, the supervisor, I/O routines, map tables, restart routines, and interrupt service routines are always active and always mapped to the same location regardless of which user or which program is active. This means that at least part of the supervisor program is carried with each executing portion of memory in a fixed portion of nonmappable memory.

Indexed mapping supports dynamic allocation of memory for tasks and users and is transparent to the user except for the supervisor's logical memory overhead. Multiple hardware memory maps can be established for users, tasks, and I/O operations. In addition, system programs can be shared among application tasks through shared pages of memory as long as the shared programs are reentrant. Couple these features with the protection field that can be incorporated into the addressing scheme and an extremely flexible means of memory expansion results. Use of bipolar large scale integration (LSI) parts currently available implements this type of memory system with minimal impact on overall system performance. The logical to physical address translation can be accomplished in less than 60 ns and, while this time might add to the overall memory access time, most microprocessors can hide the additional access time and show no effect on performance as a result. The application example using the MC6809 is a case in point.

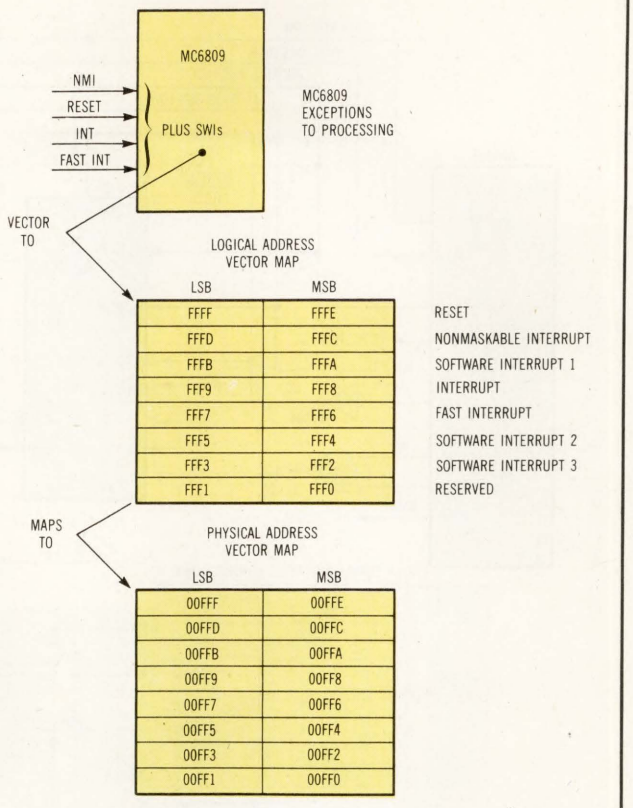


Fig 4 System exception processing. MC6809 responds to unusual conditions by trapping through memory locations FFF0 to FFFF. Indexed mapping unit translates these logical addresses to physical memory locations 00FF0 through 00FFF. System plan for handling exceptions is important first step for indexed mapping unit design

Application Example

The MC6809 demonstrates an indexed mapping application in which parameters are chosen to increase addressing range from a logical address space of 64k bytes to a physical addressing range of 1M bytes. Each 64k-byte memory page is made up of 16 segments or pages of 4k bytes each. Also, a 4-bit protection field assigns individual bits for write protection, illegal access indication, or other protection features. The AM29705 2-port random access memory (RAM) was selected to minimize impact on system performance and reduce the total logic requirements. Three such RAMs are required to make an index register array 12 bytes wide, allowing eight bytes for the page address and four bytes for the protection field. The two address ports allow writing directly to the registers or accessing them for output to either the address bus or the microprocessor data bus. The two output data ports with independent output controls allow additional flexibility in the overall system design. Permitting the processor to read back the data stored in the register file and making the second output port available with independent, 3-state controls eliminates the need for additional buffering and multiplexing.

For a detailed indexed mapping unit design, it is first necessary to understand the processor's response to unusual conditions, such as interrupts or reset, and to determine the system response to these conditions. This is an important consideration when implementing any plan for memory expansion. Fig 5 shows a system plan for the MC6809, which

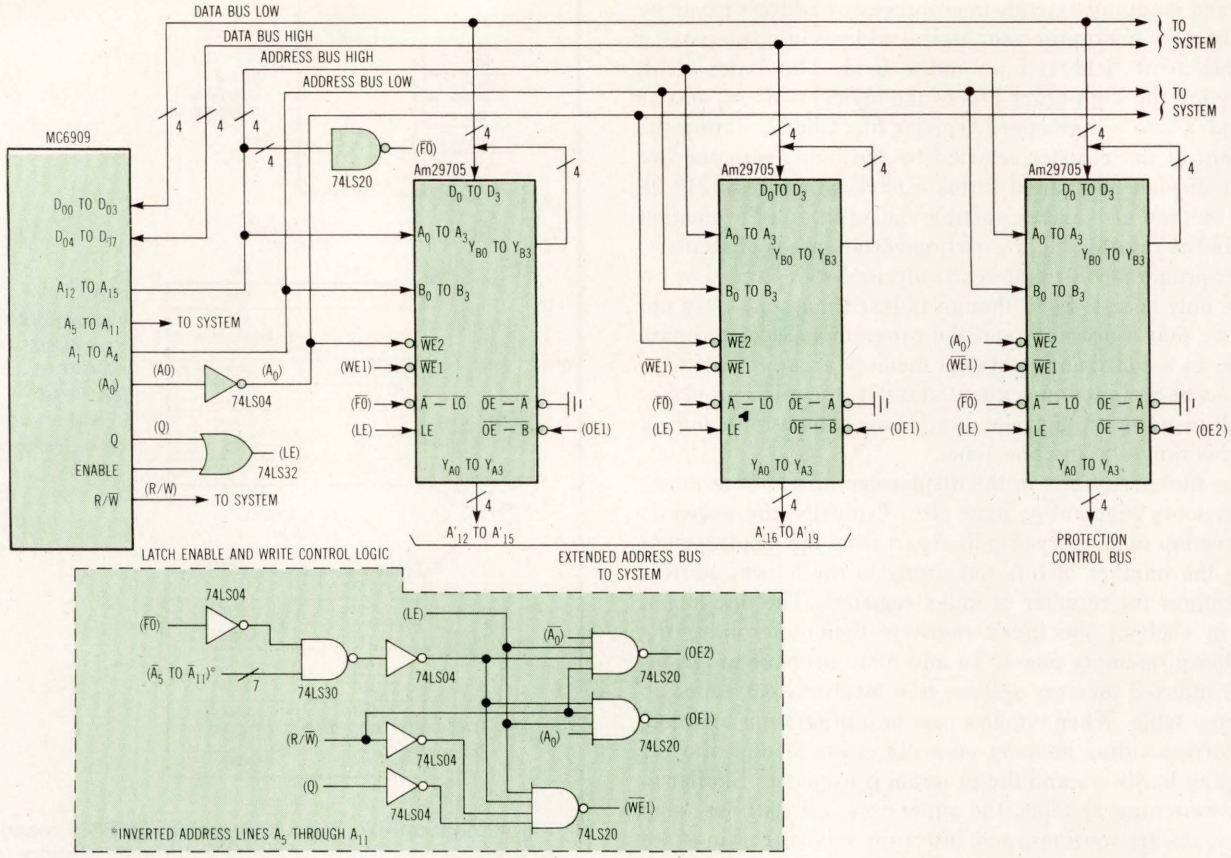


Fig 5 Circuit diagram for hardware implementation. Microprocessor address, data, clock, and read/write lines connect to three LSI bipolar components forming indexed mapping unit. Additional SSI TTL components decode control functions. Address and data buffers are omitted for clarity. YA outputs from AM29705 extend address or control bus, while YB outputs connect to data bus so that microprocessor can read mapping unit registers. Extended address and control bus outputs handle exception processing

responds to unusual conditions (NMI, SWI1, SWI2, SWI3, INTERRUPT, FAST INTERRUPT, and RESET) by trapping through a set of vectors located in reserved memory locations FFF0 through FFFF. This capability simplifies mapping the system and supervisor functions. The AM29705s have an output control on the A-data latch, $\overline{\text{A-LO}}$, which forces the output to zero. By decoding FXXX on the MC6809 address bus as the address of the 4k-byte page containing the system and supervisor functions and applying this decoding to $\overline{\text{A-LO}}$, these vectors map from FXXX in logical address space to 00XXX in physical memory. This allows mapping of all the exception vectors that alter the normal flow of processing as well as fixing in physical memory the addresses for all I/O devices, including the memory mapping unit.

Also fixed in physical memory are the interrupt service routines, shared memory locations for passing parameters between tasks, and additional mapping tables in the 4k-byte page of physical memory starting at location 00000. It is important to note here that other microprocessors respond differently to exceptions that occur during processing, and the vector mapping for exceptions must account for this difference when the system design is applied to other microprocessors. Even for microprocessors that trap to page zero for exception processing, additional mapping facilities must be provided to assure that the supervisor and other system functions also are mapped into page zero.

Fig 5 shows the mapping unit hardware implementation. Address and data buffers are omitted from the schematic for clarity, but careful design in a large system environment would mandate their use. The YA outputs of each AM29705 are used as the extended address or control bus, while the YB outputs are connected to the microprocessor data bus so that the content of the indexed mapping unit can be read by the microprocessor. Extended address and control bus outputs are forced to zero whenever A12 through A15 of the MC6809 address bus are equal to F. This maps the logical addresses FXXX to physical addresses 00XXX, fixing the system and supervisor functions in a 4k-byte segment of

physical memory starting at address 00000. A single, 4-input NAND gate used for this function is connected to $\overline{\text{A-LO}}$, the AM29705 input that forces all the YA outputs to zero. If system executive functions require a larger segment of supervisor memory, additional address decoding would reserve a second 4k-byte block of physical memory for this purpose. It would also reduce the number of mapping registers from 15 to 14.

The mapping unit functions as part of the memory system, but the processor communicates with it as though it were an I/O device. Each page mapping and protection register has its own unique address in the system page of memory. In this design, these addresses are physical memory addresses 0000 through 001F. Fig 6 shows how the protection and control registers are interleaved with the page mapping registers. The content of register F is a "don't care," here. It corresponds to logical address FXXX from the processor which forces the address bus to zero.

Because the indexed mapping unit is implemented as an I/O device, the B address port controls writing of data to each mapping unit register, along with Write Enable 1 and Write Enable 2 ($\overline{\text{WE1}}$ and $\overline{\text{WE2}}$). In addition, the MC6809 may read each mapping or protection register individually. The YB outputs of the AM29705s are normally in a high impedance state and under control of the B-address port, Output Enable B ($\overline{\text{OE-B}}$), and Latch Enable ($\overline{\text{LE}}$). In this design, because the read and write logical addresses (B-address port) of the mapping and protection registers were selected as F000 through F01F, each register can be accessed independently, allowing selective modification of an individual register's page address or protection level, without affecting the content of other mapping registers. Data are entered into the mapping unit via the processor data bus and the D0 through D3 inputs on the AM29705s. The clocking signals for the AM29705s are derived from the MC6809 clocking and control signals.

As a memory mapping unit, A12 through A15 of the MC6809 address bus connect to the A-address port input of the AM29705s and are used to address the mapping and protection registers in parallel. In addition, the YA outputs for the extended address bus are controlled by $\overline{\text{OE-A}}$ and $\overline{\text{LE}}$. The YA outputs and the YB outputs are in the transparent mode whenever Q-clock or enable clock from the MC6809 is active. This allows the address on the extended address bus to appear a maximum of 45 ns after $\overline{\text{LE}}$ goes active and the YA and YB (if enabled) outputs are latched at the removal of

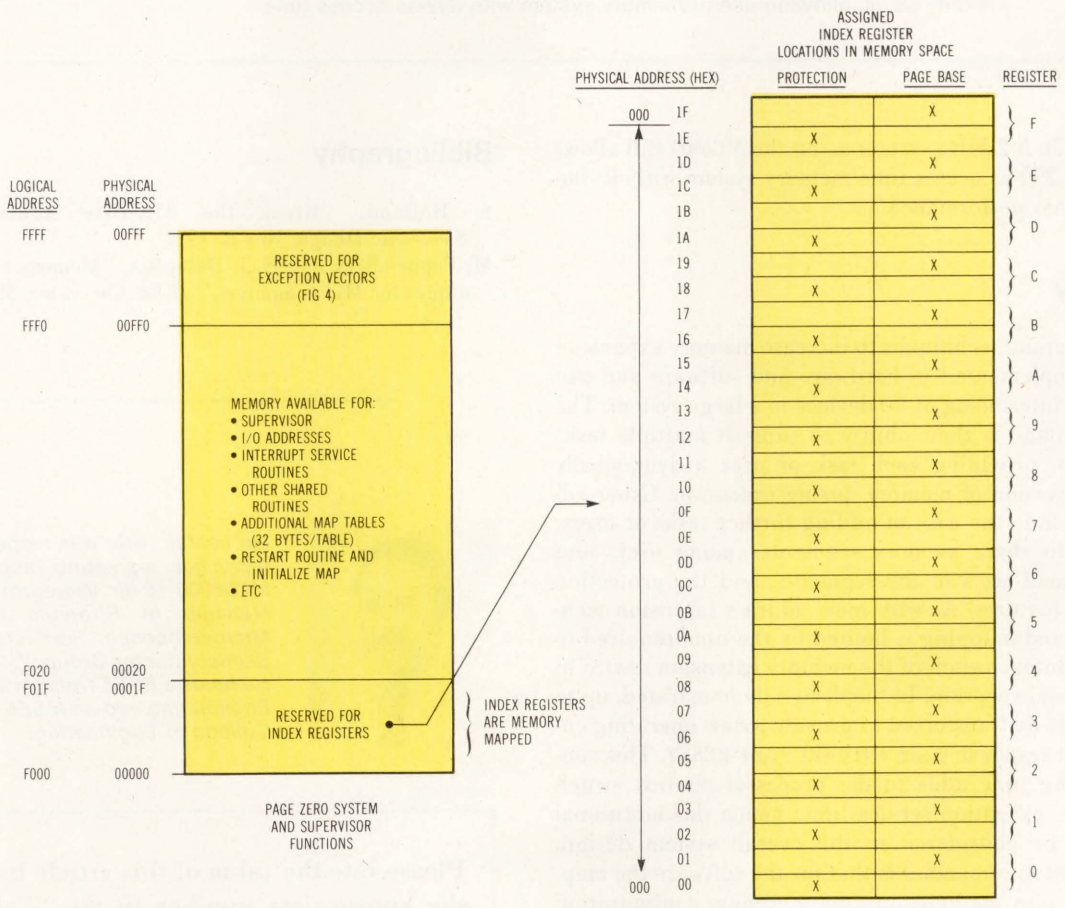


Fig 6 System functions. Physical memory system page zero contains exception processing vectors, supervisor, and executive routines, along with reserved space for mapping index registers as I/O devices. Each index register occupies two bytes supplying mapped page base address and page protection attribute bits

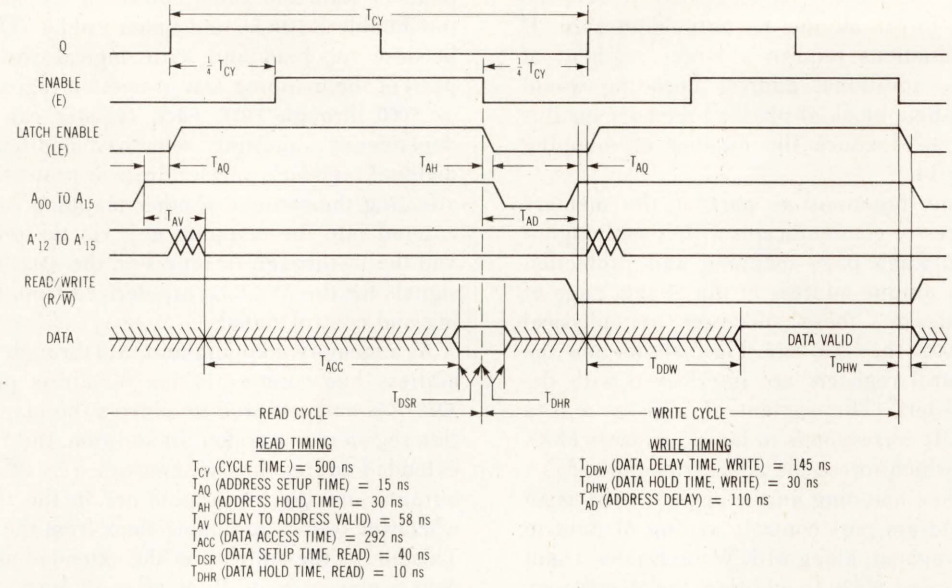


Fig 7 Timing diagram. A12 through A15 of MC6809 address bus connect to MC29705 A-address port inputs to address mapping and protection registers in parallel. YA and YB outputs are in transparent mode whenever Q or E is active. Address appears on extended address bus maximum of 45 ns after LE goes active, and YA or YB output is latched at removal of E. With 2 MHz MC6809, delay in converting logical address to physical address is only 58 ns, allowing use of memory system with 292-ns access time

enable (Fig 7). A 2-MHz system using the MC6809 still allows the use of a 290-ns access time memory system without impacting system performance.

Summary

Indexed mapping techniques to increase memory expansion are easily implemented in hardware and software and can simplify the interfacing of I/O devices to a large system. The major advantage is their ability to support multiple tasks and/or users, providing each task or user a dynamically allocatable portion of memory during execution. Other advantages include the ease of adding further tasks or users, the ability to share memory segments among users and tasks, the small sizes of the segments, and the protection and control features. As with most address extension techniques, indexed mapping is limited by the time required to perform a context switch of the memory extension device in response to an exception. In the design demonstrated, up to 30 bytes must be transferred to provide a new operating environment in response to an INTERRUPT or RESET. This context switching time adds to the processor context switch time and the exception service time; hence this additional delay must be considered in the overall system design. Another point to remember is that for the software the mapping facility must be built into the minimum configuration operating system to allow for future memory expansion. However, because of the availability of bipolar LSI parts and the capability of most microprocessors to hide additional access time, the indexed mapping system implements with minimal impact on system performance.

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Ian LeMair, who was responsible for the technical marketing support for the MC68000 16-bit Microprocessor, is now Manager of Strategic Marketing for Microcomponent Products for Motorola Semiconductor Group, World Marketing. He holds a BSEE from Newark College of Engineering and an MSEE from Midwest College of Engineering.

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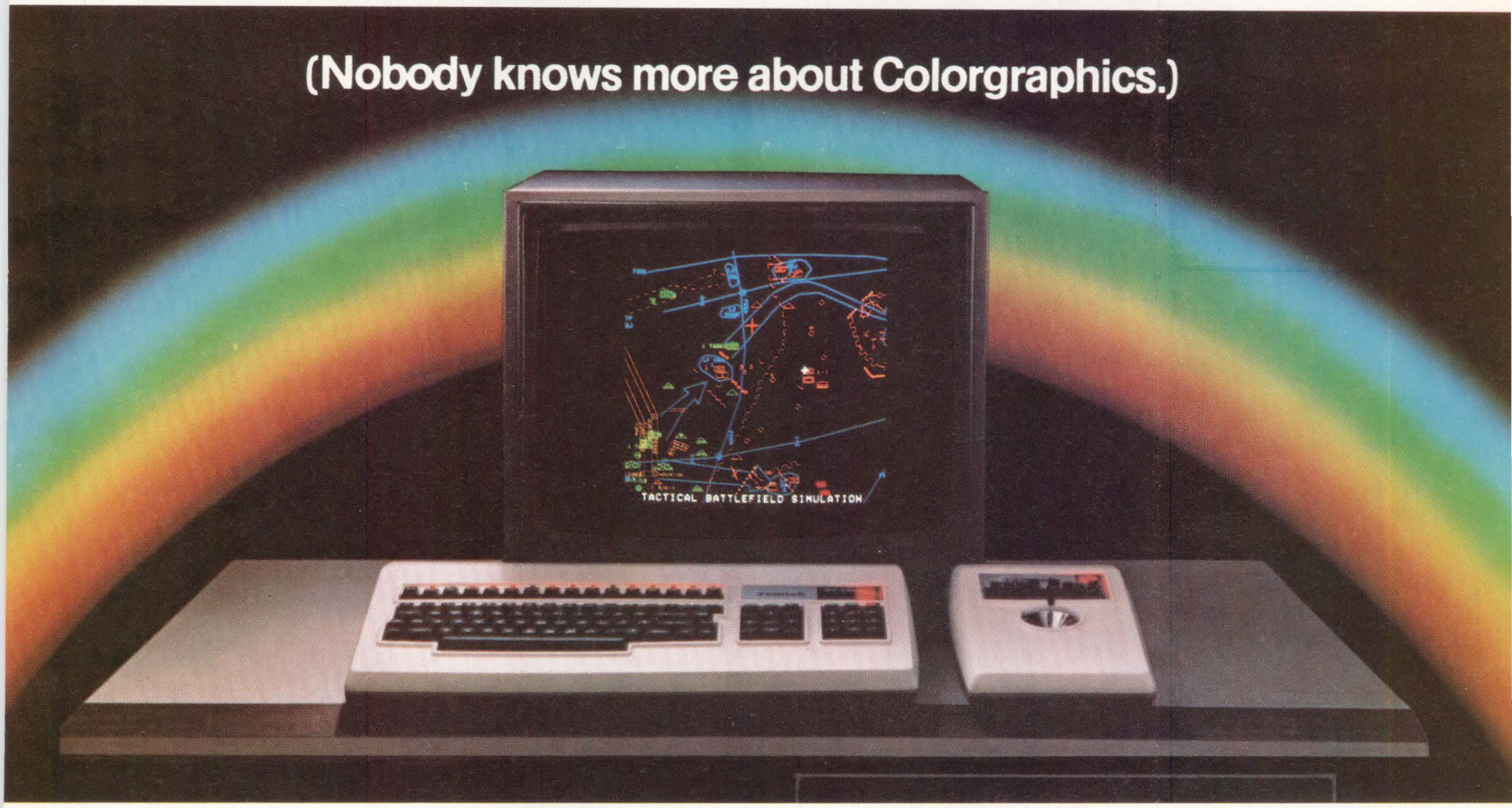

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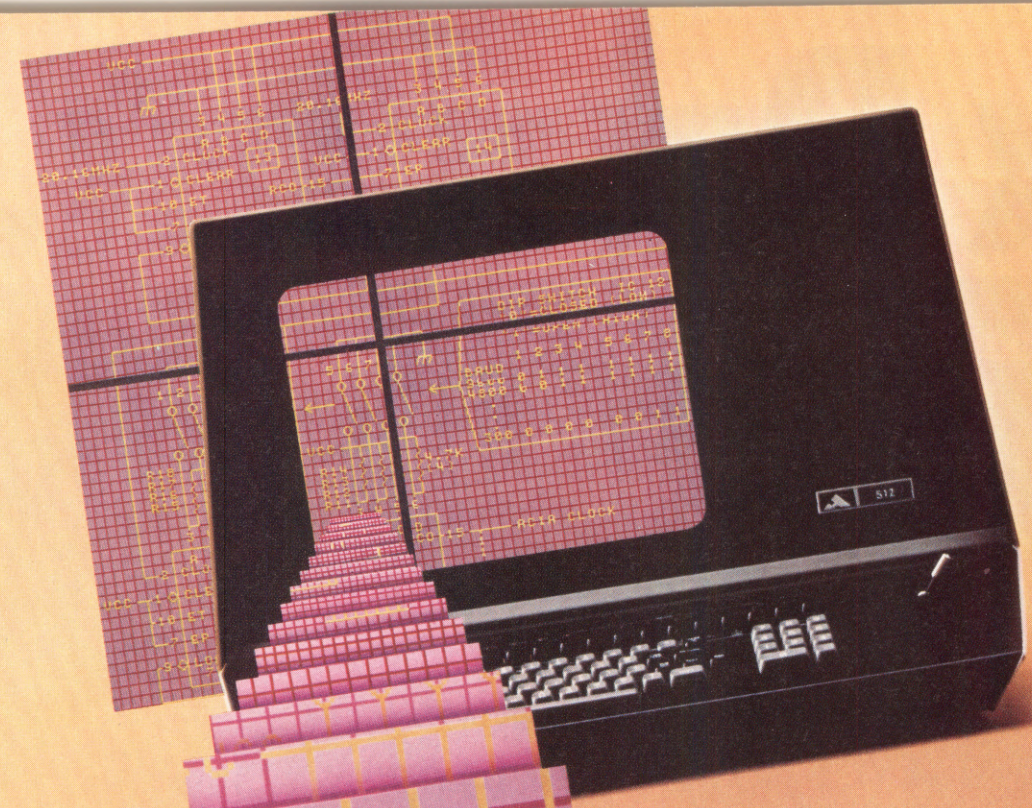

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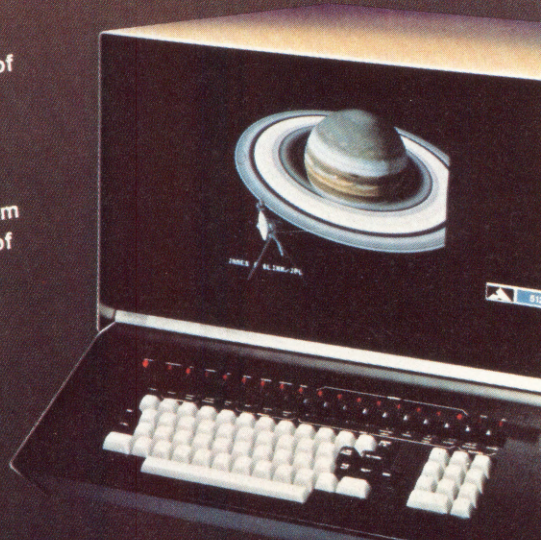

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DESIGN NOTE

A Diagnostic Module Design for the LSI-11/2 Microcomputer

Single-board circuit inserted into unused slot on microcomputer backplane displays bus cycles occurring during program steps, interrupt acknowledgment, or DMA sequences

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PO Box 500, Beaverton, OR 97077

As microcomputers have replaced minicomputers in many applications, one useful feature has been virtually eliminated. Digital Equipment Corporation's LSI-11/2 microcomputer does not provide the traditional programmer's console found on older PDP-11s, where lights and switches allowed the operator to monitor program execution on a cycle by cycle basis. This feature has been replaced by a console octal debug technique (ODT) firmware routine, which allows the operator to examine and alter memory or registers, or to execute single program instructions, using commands entered from a terminal.

Bus Monitor Augments Console

Although this soft front panel performs a majority of the functions previously handled by a hardware front panel, there are occasions when the designer of an LSI-11/2 hardware or software system may require more detailed information concerning Q-bus operation than is available with the console ODT firmware. The relatively simple Q-bus monitor (Fig 1) allows the operator to step through a program, one bus cycle at a time, examining bus addresses accessed and data transferred. In addition, the bus monitor displays data transfers that occur during an interrupt acknowledge or direct memory access (DMA) sequence. It thus augments the single step capability of the console ODT firmware, performing many of the functions previously provided by a front panel.

Since all but one of the signals required for bus monitor operation are obtained directly from any unused slot in the Q-bus, the bus monitor is easily installed and removed from equipment and should prove especially useful in servicing LSI-11/2 installations such as industrial controllers, where a terminal may not be available. The bus monitor also greatly increases the utility of a logic analyzer display by allowing the operator to examine timing waveforms associated with execution of individual program instructions, without the surrounding clutter of bus activity that accompanies single instruction execution under console ODT firmware.

Advantageous Use of LSI-11/2 Timing Requirements

The bus monitor circuit takes advantage of a specific timing requirement, which must be met by the processor and any other Q-bus master device. The circuit functions through this timing requirement to halt the LSI-11/2 during each bus transaction, and it does this without modifying the processor internal circuitry. Since the Q-bus is asynchronous, any bus master must be prepared to wait an indefinite length of time for the handshake signal

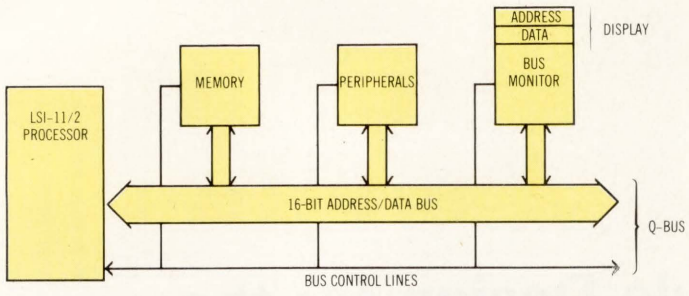

Fig 1 Bus monitor block diagram. Attaching bus monitor to LSI-11/2 Q-bus allows examination of bus activity in greater detail than processor console firmware affords

(BRPLY). BRPLY must be unasserted by the addressed peripheral or memory before the processor can complete the bus transaction by unasserting BSYNCH. Bus monitor activity during a typical LSI-11/2 instruction fetch is shown in Fig 2.

The bus monitor control logic (Fig 3) monitors the state of the BRPLY signal on the bus to detect a bus transaction. When this signal is asserted by some other device during a bus transaction, the bus monitor also asserts and holds BRPLY. Since the bus drivers for the BRPLY line are open collector drivers, the LSI-11/2 sees the wired OR of BRPLY as asserted by the addressed device and held asserted by the bus monitor. The LSI-11/2 is thus prevented from completing the bus transaction as long as the bus monitor holds BRPLY. Operation of a momentary contact switch, S1, causes the bus monitor to release BRPLY, allowing the LSI-11/2 to continue.

Utility of the bus monitor circuit as a debugging tool is increased by latching bus address and data information for readout on octal, 7-segment displays. In addition, six status LEDs indicate the type of bus transaction: read, write, write byte, instruction fetch, interrupt vector transfer, or DMA transfer.

Circuit Description

The bus monitor circuit is based on interaction with an LSI-11/2 microprocessor as bus master. Similar operation will be obtained when DMA devices and other bus masters are used. The single-cycle logic (Fig 3) operates with IC 1a initially cleared and its NOT Q output high. With mode switch S2 set for single cycle operation, NAND gate IC 2 has both inputs high, making pin 3 of open collector bus driver IC 3 high. When BRPLY is asserted by another device during a bus transaction, pin 2 of IC 3 also goes high, causing IC 3 to hold BRPLY asserted. This state is maintained until S1 is actuated. A low to high transition, debounced by gates IC 4a and IC 4b, then clocks D flipflop IC 1a. Since BRPLY is asserted, the D input to IC 1a is high and its NOT Q input goes low. Thus, pin 1 of IC 2 goes low, causing pin 3 of IC 3 to go low. This causes IC 3 to unassert BRPLY, allowing the microprocessor to continue execution. Once BRPLY is no longer asserted, flipflop IC 1a is cleared and the circuit is ready for the next bus transaction.

Mode switch S2 allows selection of a single-instruction mode as well as a single-cycle mode of operation. In single-instruction mode, the processor is halted only during instruction fetches. For this feature to function, processor signal SRUN must be provided. This signal is readily available on backplane pin AA1 of the LSI-11/2, but only at the slot containing the processor. Therefore, with DEC backplanes, SRUN must be connected from pin AA1 of the processor slot to pin AA1 of any backplane slot in which the bus monitor is installed.

With S2 set for single-instruction mode, pin 2 of IC 2 is connected to the Q output of D flipflop IC 1b. This flipflop is initially cleared, and thus pin 2 of IC 2 is low. This causes pin 3 of IC 3 to be low and prevents assertion of BRPLY by the bus monitor. Early in the execution of an instruction fetch bus cycle, the LSI-11/2 brings SRUN low and then high, clocking flipflop IC 1b to the set state. This causes pin 2 of IC 2 to go high, allowing pin 3 of IC 3 to go high. Thus, the bus monitor is ready to hold BRPLY, once it is asserted, and the processor is stopped during the fetch. When S1 is actuated, the bus transaction proceeds as in single-cycle mode and flipflop IC 1b is cleared until the

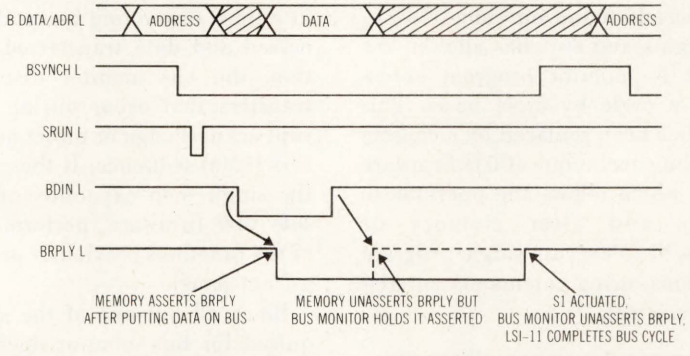

Fig 2 Typical LSI-11/2 fetch cycle waveforms. Bus monitor detects BRPLY and holds it asserted until momentary contact switch allows processor to continue

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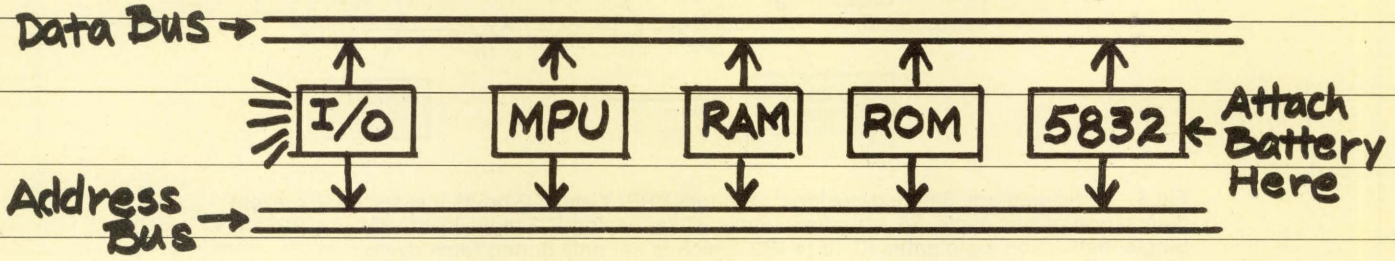

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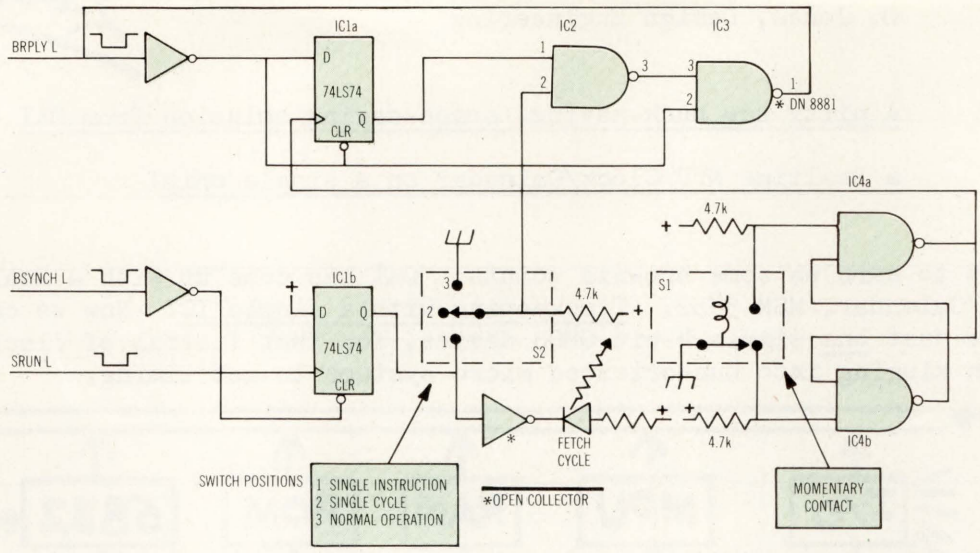

Fig 3 Logic diagram. Single cycle logic monitors BRPLY and IC3 holds it asserted to prevent completion of bus cycle. S1 actuation clocks IC 1a, driving IC3 input low to release BRPLY. Single instruction logic gates IC 1b to IC2, which is set only during fetch cycle.

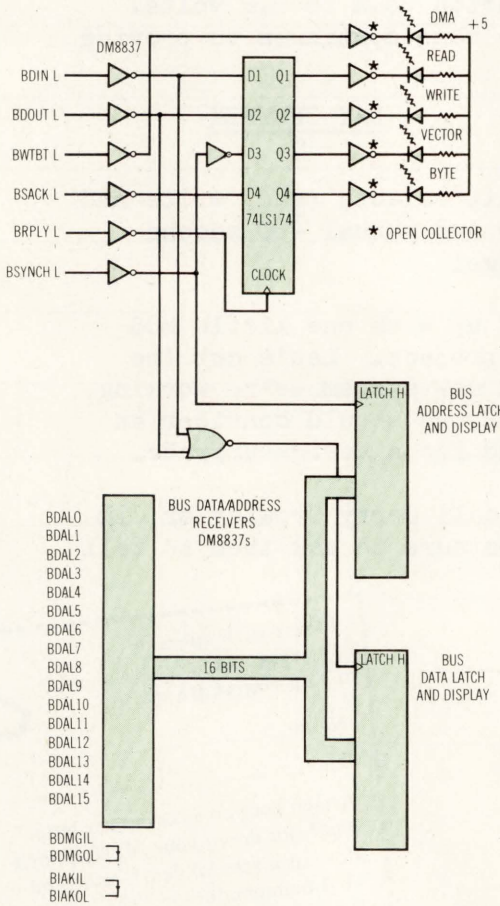

Fig 4 Address, data, and status display logic. Bus receivers buffer all signals to latches that hold data with logic 1 at clock input. Status indicators display selected bus control lines. Latches and display drivers are chosen to fulfill specific requirements

next instruction fetch. A third position of S2 grounds pin 2 of IC 2, disabling the bus monitor.

The address, data, and status displays (Fig 4) are quite straightforward. Bus receivers buffer the Q-bus signals before they are applied to display latches and drivers. Bus address information is latched on the assertion of BSYNCH, while bus data are latched on the assertion of BDIN or BDOUT. The bus monitor cannot be installed in some older LSI-11 systems that use a DMA refresh card because it will prevent proper memory refresh. Also, even though the bus monitor is useful in the initial debugging of hardware incorporating DMA, it does not allow proper operation of those DMA-type devices, such as disc drives, in which realtime data transfer must occur. □

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DESIGN NOTE

N-Channel Asynchronous Arbiter Resolves Resource Allocation Conflicts

Double function arbiter circuit reduces input and component requirements while solving conflicts in multiprocessor system service requests

Emil Petriu Polytechnic Institute
Bv Parvan 2, 1900 Timisoara, Romania

When two or more processors simultaneously require the use of a common resource in a multiprocessor system, conflicts usually occur, and an arbiter circuit is normally used to resolve them.[1] The arbiter must be an asynchronous circuit, and be able to react to requests occurring at any time. However, it cannot be a clocked sequential circuit, since the value of an input signal may change even when a clock pulse is present.

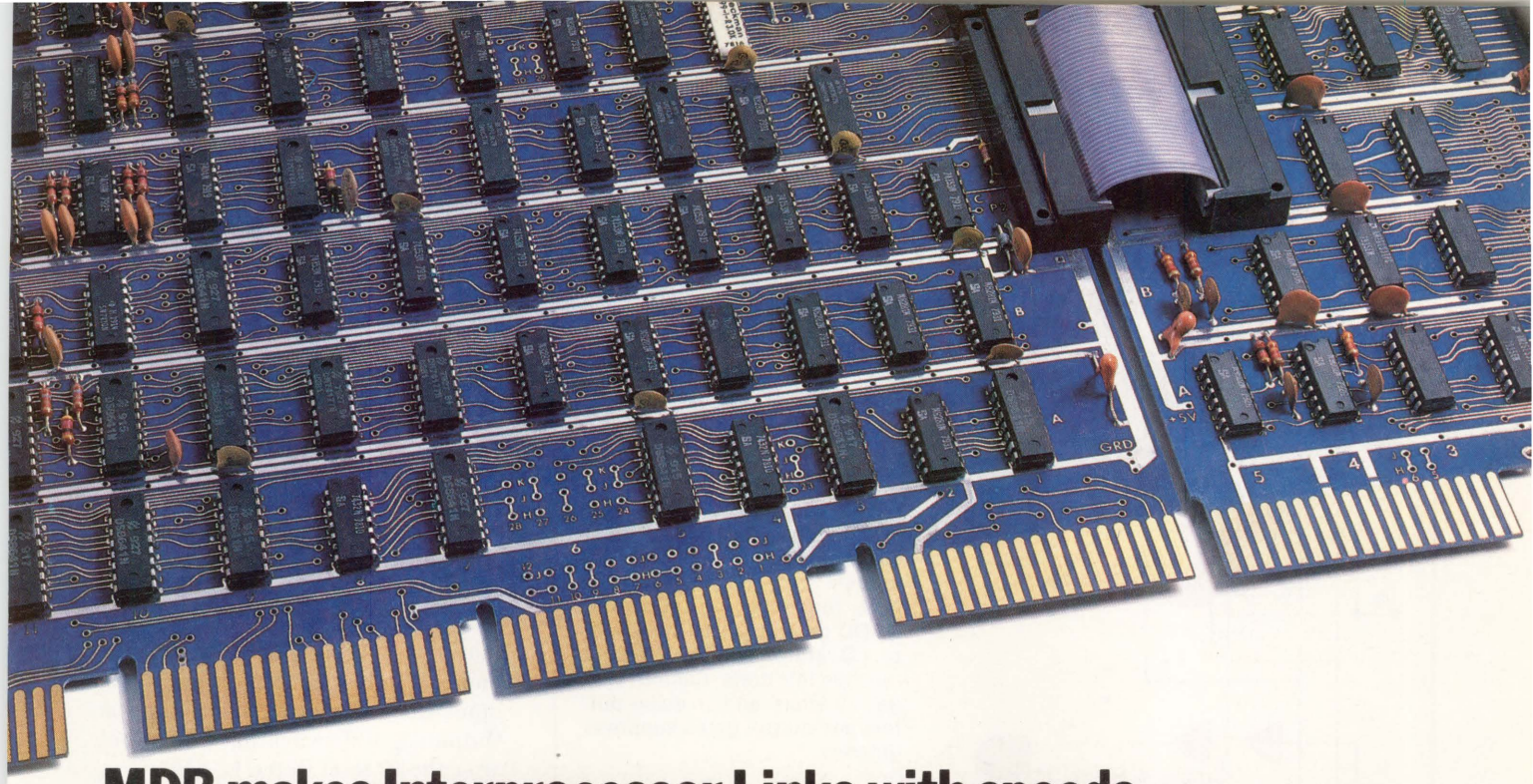
Heretofore two techniques generally have been used for implementing an n-channel arbiter. One,[2,3] a basic arbiter module, has a double function: as an arbiter for concurrent requests, and as a memory for acknowledge[2] or grant.[3] The module can process only two requests; however, by extending this approach, asynchronous n-channel structures can be implemented, connecting many basic arbiter modules.

In the second technique the memory and arbiter functions are performed by different circuits.[1,4,5,6,7] Clocked latches are usually used as memory circuits for request inputs and for output grants; otherwise, the presence of a clock pulse is a disadvantage. The arbiter function is performed by excluding-type circuits. Existence of a separate arbiter block permits a more convenient implementation of sophisticated priority rules.[1,4] The arbiter block may also be conceived as a programmable unit.[5,6]

A simple n-channel asynchronous arbiter circuit with a double function (arbiter and memory) can arbitrate n concurrent requests according to fixed priority rules. It should handle many current applications; and it can also be used as an asynchronous arbiter module for more than two channels, suitable for implementing large arbiter structures.

Asynchronous N-Channel Arbiter

The n-channel arbiter consists mainly of n NAND gates, each with n inputs Fig 1). A request signal R_K (K = 1,... n) is applied to an input of each NAND gate K. The output of each NAND gate $\overline{G}_K$ is applied as a feedback signal to an



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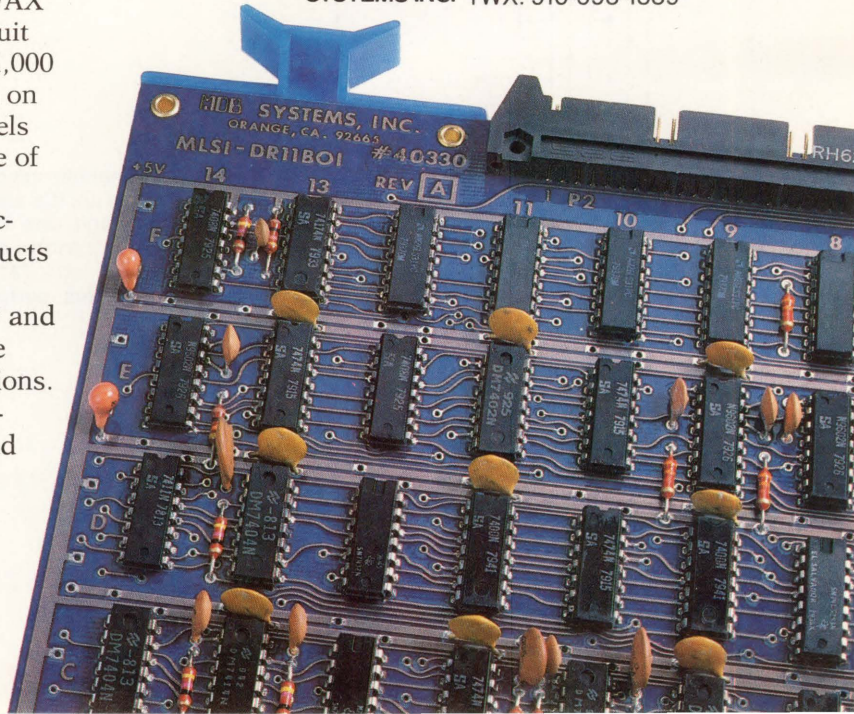

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Circle 61 for LSI-11, 62 for PDP-11, 63 for DG, 64 for PE, 65 for IBM.

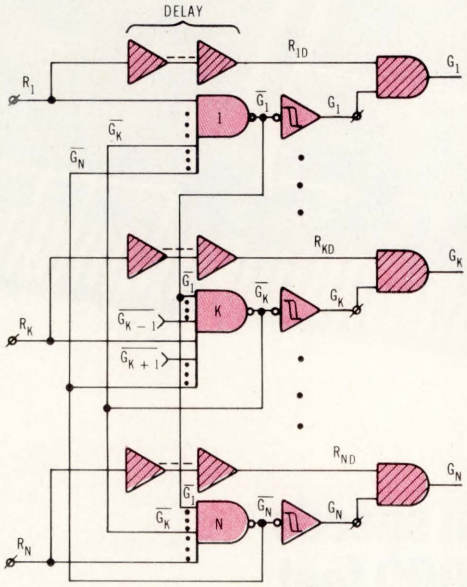

Fig 1 Generalized n-channel asynchronous arbiter. Circuit can arbitrate n concurrent R_K request signals. For concurrent requests, all activated NAND gates start to switch into LO state, but only fastest reaches this state. Schmitt trigger inverters and/or delay buffers and output gates suppress glitches

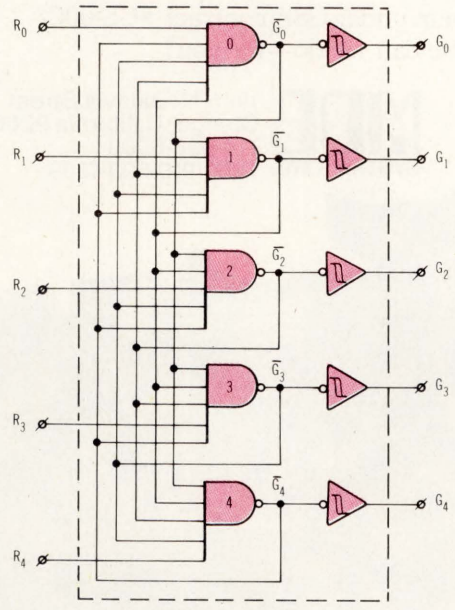

Fig 2 5-channel asynchronous arbiter. Only six ICs are required, five 7430s and one 7414. 7430 NAND gates perform arbiter and memory functions; 7414 Schmitt trigger inverters perform glitch suppression

input of all the other n − 1 gates. Schmitt-trigger inverters are used for glitch suppression. If glitches remain at the output of these inverters, they can be removed by performing an AND operation between output signal G_K and the delayed version R_{KD} of the request signal.

In the quiescent state, all request lines $R_1 - R_N$ are at LO level and consequently all outputs $G_1 - G_N$ are at HI level. If channel input K requests processor access, a HI signal is sent to input R_K. Thus with the K NAND gate inputs all at HI, its output G_K switches to LO. During the time that the HI level is applied to R_K, a LO level appears at output G_K. This LO level is applied to all the other NAND gates, maintaining their outputs at HI level, even if other input channel request signals appear. Output G_K will switch back to HI only after the HI level to the R_K input deactivates, thereby allowing another NAND gate to be switched to LO.

If several channel requests occur simultaneously, all corresponding NAND gates start to switch into LO, but only the fastest gate reaches this state. The output signal that first reaches threshold level V_T forces all the other gates to switch back to HI. However, glitches will appear at the output of those NAND gates that do not succeed in switching from HI. These glitches are suppressed by Schmitt trigger inverters.

As described, the circuit of Fig 1 can arbitrate several concurrent requests. Switching characteristics of the NAND gates determine the priority rule. The circuit includes a memory function; no other memory circuits are necessary for grant storage. By using standard 745133 TTL gates, asynchronous arbitration of up to 13 concurrent requests can be realized.

5-Channel Arbiter Configuration

Structure of a 5-channel arbiter (Fig 2) occurs as a particular case of the general structure presented in Fig 1 with N = 5; Fig 3 is the corresponding timing diagram for this circuit. The special case of five concurrent requests is analyzed.

Although not all the switching characteristics have been considered, Fig 3 emphasizes the hazard of glitches occurring in the first level of the logic circuit. The two distinct

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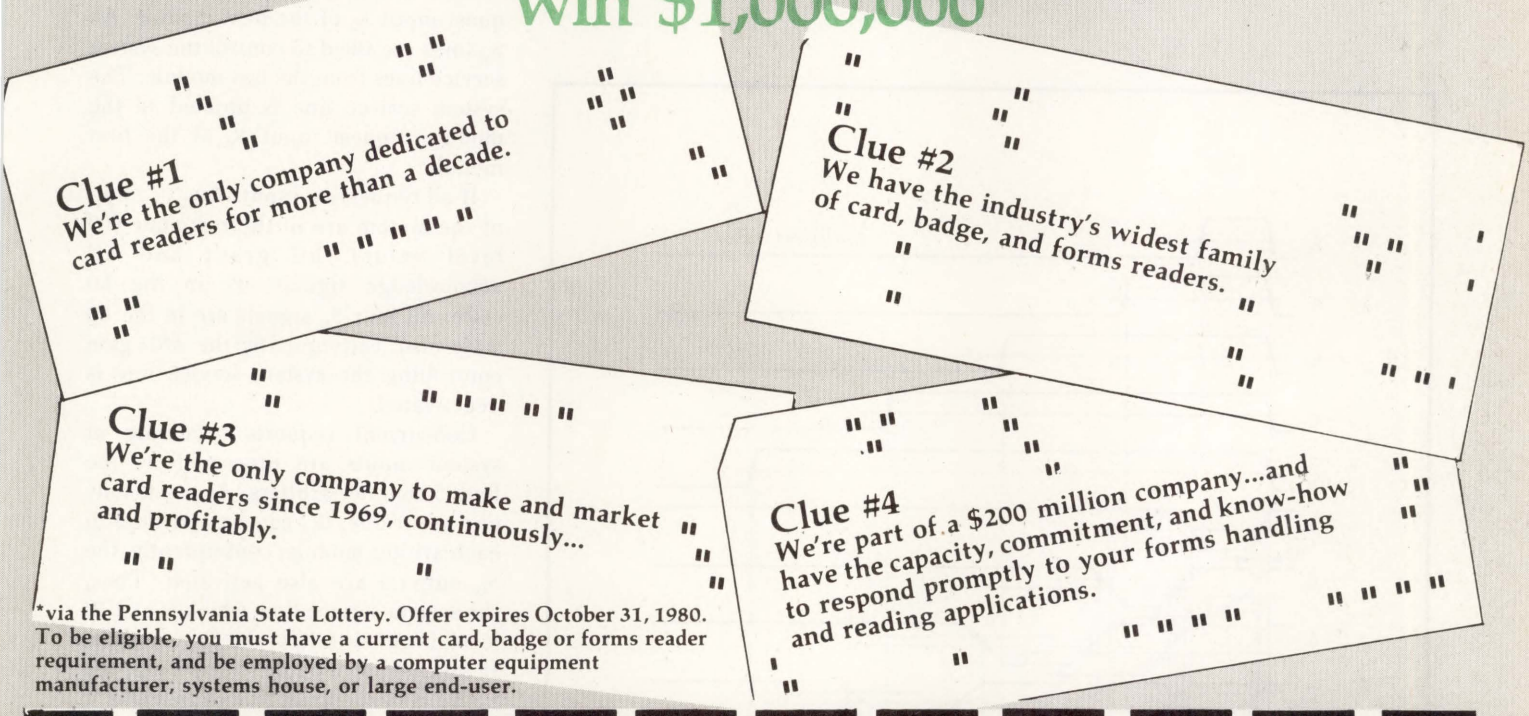

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threshold values for the Schmitt triggers determine the glitch suppression capabilities of these inverters.

The first NAND gate, having a $\overline{G}_0$ output, is considered to be the fastest; therefore, the R_0 input has the highest priority, followed in sequence by R_1, R_2, R_3, and R_4. A NAND gate begins to switch state when the input signal reaches threshold value V_T. It can be seen from Fig 3 that, if there are two or more concurrent requests, only one grant line is activated. Another grant line can be activated only when the previous grant line is deactivated. The request having the highest priority always releases the grant.

The 5-channel arbiter of Fig 2 needs only five 7430 ICs, using only five of the eight inputs to each NAND gate, and one 7414 IC.

Extended Multichannel Configurations

Using one request and one grant as module request and module grant, respectively, the 5-channel arbiter of Fig 2 can be used as a 4-channel arbiter module, and can be connected in extended multichannel configurations. For example, a 16-channel asynchronous arbiter structure can be realized by using four of these 4-channel arbiter modules (Fig 4).

Grant lines G_1, G_2, G_3, and G_4 coming from a 5-channel arbiter are gated by module-request line R_0, resulting in acknowledge signals A_1, A_2, A_3, and A_4. Grant lines of each module are ORed, resulting in a request service signal S_M. The module grant output G_0 of each module is connected to the module request input R_0 of the next module. All S_M lines are ORed to control the system service lines from the last module. The system service line is applied to the module request input R_0 of the first module.

If all requesting inputs $RQ_{11} \ldots RQ_{44}$ of the system are in the rest state (LO level value), all grant and all acknowledge signals are in the LO state. All four S_M signals are in the LO state also; consequently the AND gate controlling the system service line is deactivated.

Concurrent requests occurring at system inputs are processed by the four 5-channel arbiters. At most, only one grant line, G_K, can be activated in each arbiter module; consequently, the S_M outputs are also activated. Thus, the system service line, which is at a HI level, is gated to R_0 of the first module. If this arbiter module is servicing, the active system service line cannot award a grant to this module, but it does enable the output acknowledge gates of the module. Consequently, only the first module will present an active acknowledge output signal. All the other modules have a LO level signal at their R_0 inputs, which disables the acknowledge output gates.

When a higher priority module relinquishes the common resource, the system service line, enabled by the S_M of the waiting modules, gains the grant G_0 = HI in this module, enabling the acknowledge output gates of the adjacent module. Since the R_0 input has the highest priority in each module, a module that has relinquished the common resource cannot be serviced again until the previous module is in the waiting state. When G_0 of the last module reaches the HI level, the system service line is lowered and a LO level is propagated through the module

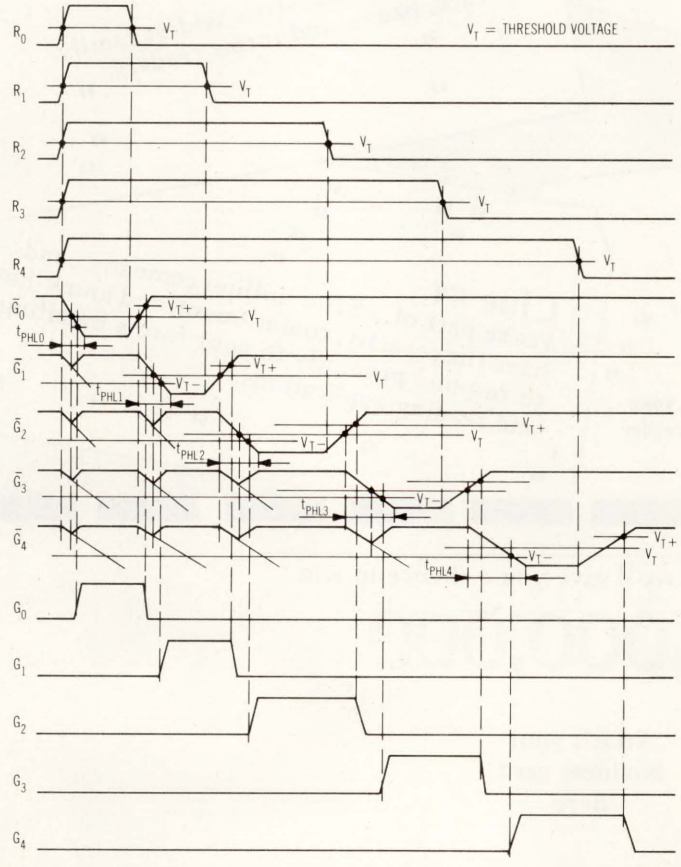

Fig 3 Timing diagram for 5-channel asynchronous arbiter. Priority order for request inputs in R_0 (highest) followed by R_1, R_2, R_3, and R_4 (lowest). Five NAND gates of arbiter have propagation delay times from HI to LO level output in increasing sequence: 8 ns $\leqslant t_{PHL0} < t_{PHL1} < t_{PHL2} < t_{PHL3} < t_{PHL4} \leqslant$ 15 ns. If there are two or more concurrent requests, only one grant line corresponding to the highest priority input is activated

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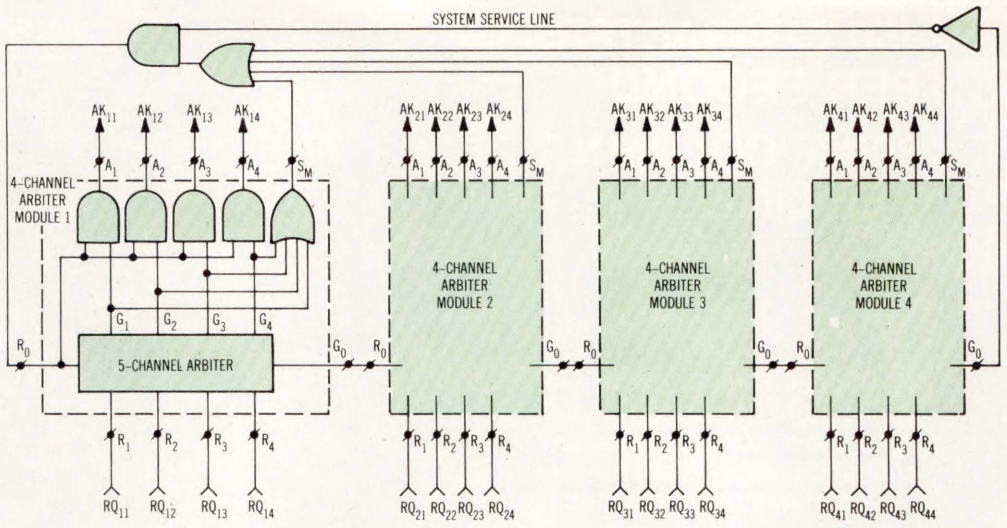

Fig 4 Extended multichannel configuration. It is obtained by using 5-channel arbiter as 4-channel module with R_0 serving as module request line and G_0 serving as module grant line. System service line is enabled by request service outputs S_M and propagated through module request/grant lines to first servicing module, enabling its acknowledge gates

request/module grant line, finally lowering the G_0 output of the last module. Only then can a new servicing cycle begin.

Conclusions

An n-channel asynchronous arbiter circuit for concurrent processors can be conceived as a module, and can be implemented in a larger arbiter structure. The 4-user arbiter module is useful in many current applications where no sophisticated priority rules are needed. In the Table this approach is compared with the well-known SN74278 4-bit cascadable priority register in accomplishing the same function. The proposed module can be contained in a 14-lead package.

Comparison of Arbiter Circuits

	SN 74278	4-Channel Module
Total Inputs	55	42
Total Gates Used	25	15
Number of External Leads	11	11
Remarks	Clocked; Expandable	Asynchronous; Expandable

Acknowledgments

This work was done during a specialization period under a UNESCO fellowship at the University of Technology of Delft, The Netherlands. The author is indebted to Prof B. P. Th. Veltman for the cooperation offered during this period, and also to Mr C. van Holten for his readiness to discuss relevant questions.

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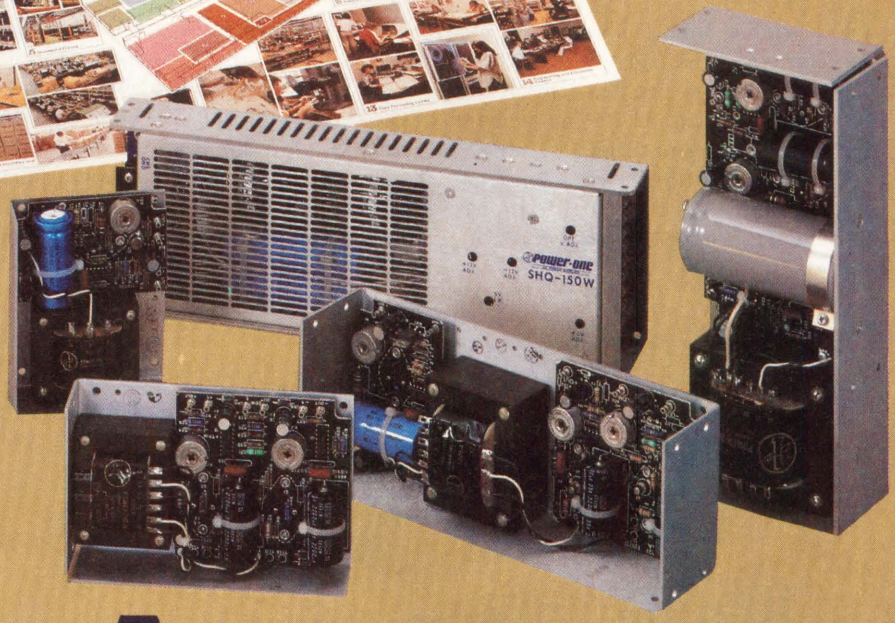

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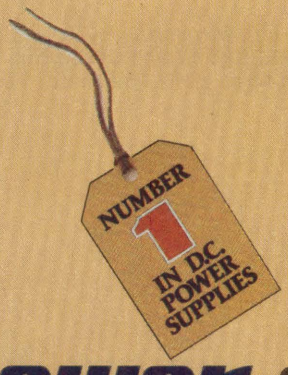

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TECH BRIEF

A Simple Tri-Stable Latch

Narrow negative going pulse, applied to latch, generates stable states of 1, −1, and 0

Dil Sukh Jain and V. L. Patil NRSA, Hyderabad, India

A tri-stable latch finds applications in Zeeman modulators and various scientific instruments. This circuit can also be used as an interfacing element between binary and ternary systems.

Fig 1 shows three transistor-transistor logic (TTL) control inputs (PRESET$^+$, PRESET$^-$, and CLEAR), which are used to obtain three stable states, 1, −1, and 0, corresponding to 5, −5, and 0 V, respectively, at output Q. The circuit consists of a dual J-K flipflop (SN7476), three 2-input AND gates (SN7408), and an operational amplifier (μ A741). Circuit operation is defined in the Excitation Table; important waveforms are shown in Fig 2.

The tri-stable latch performs as a TTL to bipolar signal converter when 50- to 100-ns narrow pulses, derived from the leading and trailing edges of the TTL signal, are applied to the PRESET$^+$ and PRESET$^-$ inputs, respectively.

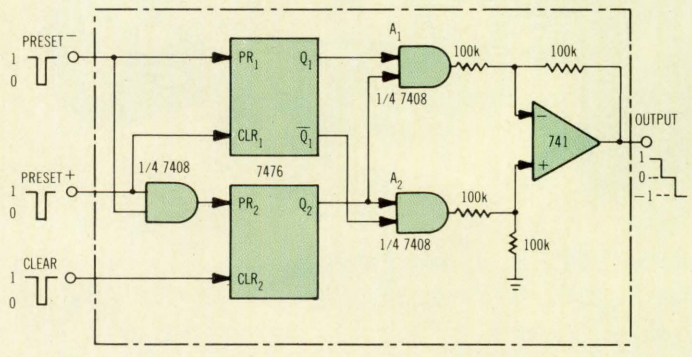

Fig 1 Tri-stable latch. Circuit generates stable states of 1, −1, and 0 when 50-ns negative going pulse is applied at PRESET$^+$, PRESET$^-$, and CLEAR inputs, respectively

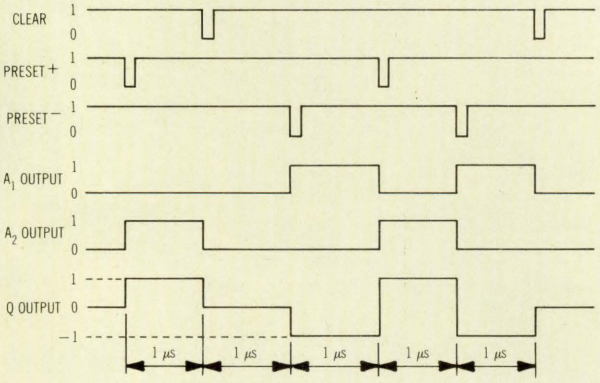

Fig 2 Important waveforms. 50- to 100-ns pulse trains at PRESET$^+$, PRESET$^-$, and CLEAR inputs, randomly derived from 1-MHz clock, generate 1-μs wide tri-stable output

Excitation Table

Inputs			Intermediate Outputs				Output
PRESET$^+$	PRESET$^-$	CLEAR	Q_1	Q_2	A_1	A_2	Q
NP	1	1	0	1	0	1	1
1	NP	1	1	1	1	0	−1
1	1	NP	x	0	0	0	0

NP = 50- to 100-ns negative pulse
x = Don't Care

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MICRO DATA STACK
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INTERFACING FUNDAMENTALS: CONDITIONAL I/O USING TWO MICROCOMPUTERS

Peter R. Rony Virginia Polytechnic Institute and State University
Blacksburg, VA 24061

Advantages and disadvantages of different types of input/output techniques can be best studied experimentally. Fig 1 provides a schematic diagram of a 2-microcomputer handshaking input/output system built upon a pair of 8080A based microcomputers and four interface chips. The heart of the interface circuit is a 74LS373 buffer/latch integrated circuit, which contains eight transparent D-type latches with 3-state outputs. Transparent latch means that while the enable is high, the output of each latch follows the data input. When the enable is low, the output is latched at the level of the data that were set up.[1] All eight latches are enabled simultaneously at pin 11, the latch enable (LE) input, and all eight 3-state buffers are also enabled simultaneously at pin 1, the output enable ($\overline{OE}$) input.

Input/output (I/O) device select pulses shown in Fig 1 are summarized in Table 1. Source $\overline{\text{OUT 05H}}$ pulse sets the semaphore, and acceptor $\overline{\text{OUT 06H}}$ resets the semaphore, which is a 7474 D-type edge-triggered flipflop with preset and clear. The preset and clear inputs to the 7474 are used, as depicted in a previous column.[2] Two $\overline{\text{IN 04H}}$ pulses input the semaphore output, Q, to the D0 position of the accumulator of the source and acceptor microcomputers. Once input to the accumulator, the D0 bit is rotated into the carry position and the logic state of the carry tested with either a JC or JNC instruction. Output from the source microcomputer is latched into the 74LS373 with the aid of the $\overline{\text{OUT 80H}}$ pulse, and data in the 74LS373 are input to the acceptor microcomputer with the aid of a $\overline{\text{IN 07H}}$ pulse.

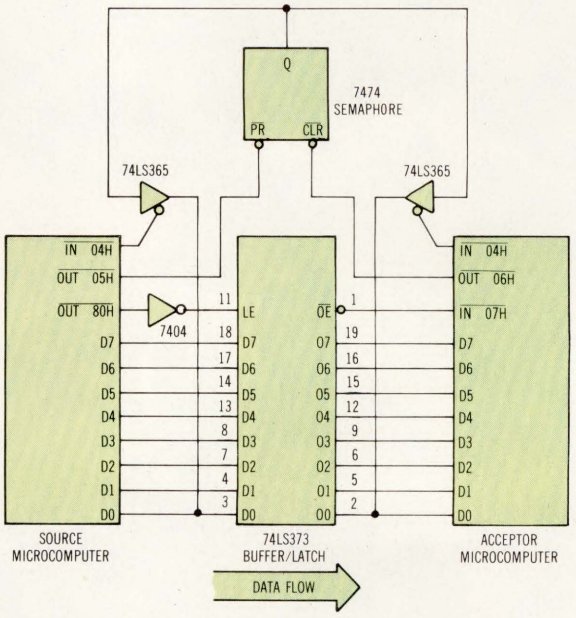

Fig 1 2-microcomputer conditional I/O circuit. Data flow is from left to right, from source microcomputer, through 74LS373 buffer/latch, to acceptor microcomputer

TABLE 1

Input and Output Device Select Pulses

	Source Microcomputer
$\overline{\text{IN 04H}}$	Inputs semaphore (flag) bit into source microcomputer
$\overline{\text{OUT 05H}}$	Sets semaphore (flag)
$\overline{\text{OUT 80H}}$	Outputs data from source microcomputer to 74LS373
	Acceptor Microcomputer
$\overline{\text{IN 04H}}$	Inputs semaphore (flag) bit into acceptor microcomputer
$\overline{\text{OUT 06H}}$	Resets semaphore (flag)
$\overline{\text{IN 07H}}$	Inputs data from 74LS373 buffer to acceptor microcomputer

It is possible, in principle, to eliminate the source $\overline{\text{OUT 05H}}$ and acceptor $\overline{\text{OUT 06H}}$ device select pulses, and replace them with $\overline{\text{OUT 80H}}$ and $\overline{\text{IN 07H}}$, respectively. Since the circuit in Fig 1 is designed for educational purposes, it is more useful to provide independent data I/O and semaphore set/reset capabilities.

Fig 2 provides flowcharts and 8080A assembly language listings for conditional I/O using a semaphore.[3] Programs for source and acceptor microcomputers both were started at memory location 0300H. The objective of the programs was to transfer 64 successive bytes from memory locations 0380H through 03BFH in the source microcomputer to memory locations 0380H through 03BFH in the acceptor microcomputer. Data stored in these locations were 00H, 01H, 02H, 03H, ... 3FH, which permitted ease of observation of the progress of data transfer. Data transfer from source to acceptor was monitored using a hexadecimal latch/display output port on each microcomputer. A successful transfer of 64 bytes was concluded by the appearance of the number 3FH on the hexadecimal latch/display output port on each microcomputer, and with one or both microcomputers in the halt state.

The data processing routine for the source microcomputer consisted of retrieving a single byte of data from a memory location, executing a time-delay routine, incrementing the memory pointer, and testing the memory pointer to see if any more data needed to be output. The data processing routine for the acceptor microcomputer consisted of storing input data into a memory location, executing a time-delay routine, incrementing the memory pointer, and testing the memory pointer to determine if memory was full. The source and acceptor microcomputers were identical, but the source had a clock frequency of approximately 0.75 MHz, while the acceptor microcomputer had a clock frequency of 1.17 MHz.

In the absence of a time-delay routine in either the source or acceptor programs, it was possible to transfer data from source memory to acceptor memory at a rate of 134 μs/byte. If both microcomputers were operated at 4 MHz, the data

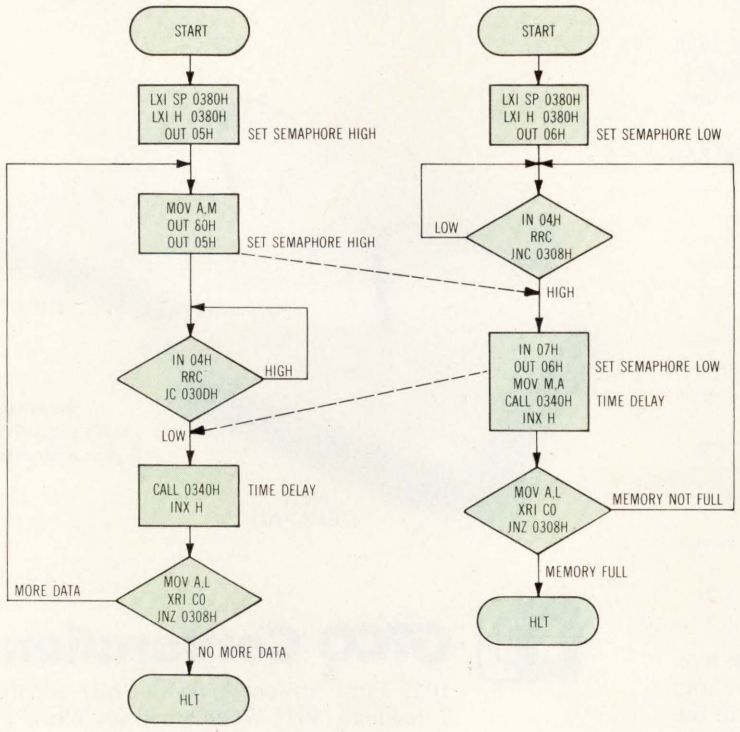

Fig 2 Flowcharts and assembly language programs. Source microcomputer program is on left, while acceptor microcomputer program is on right

TABLE 2

Modifications of Assembly Language Programs in Fig 2

Type of I/O Operation	Modifications Required
Conditional I/O with semaphore	Use source and acceptor programs as given
Conditional output with flag	Use source program as given. Eliminate first OUT 06H and IN 04H, RRC, and JC 0308H from acceptor program
Conditional input with flag	Use acceptor program as given. Eliminate first OUT 05H and IN 04H, RRC, and JC 030DH from source program
Unconditional I/O	Difficult to synchronize data transfer of 64 bytes from source memory to acceptor memory

transfer rate would be approximately 38 μs/byte. When a 6.131-ms delay was added to the acceptor program, with the source program running as fast as possible, the data transfer rate slowed to 6.235 ms/byte. Conversely, when a 9.506-ms delay was added to the source program, with the acceptor program running as fast as possible, the data transfer rate became 9.695 ms/byte. These results confirm the expectation that the longest time delay, whether in the source or acceptor programs, governs data transfer rate.

The semaphore in Fig 1 can be converted to a flag simply by deleting the flag-testing loop in either source or acceptor program; details are provided in Table 2. For conditional *output* with flag, a 6.131-ms delay in the acceptor program, with the source program running as fast as possible, produced a data transfer rate of 6.189 ms/byte. For conditional *input* with flag, a 9.530-ms delay in the source program, with the acceptor program running as fast as possible, provided a data transfer rate of 9.642 ms/byte.

Using a pair of microcomputers to demonstrate characteristics of conditional I/O techniques has advantages. Influences of time delays in source or acceptor can be explored simply by making software changes. As discussed, the longest time delay governs the data transfer rate. Software changes also can be made to determine the type of I/O operation performed, and whether a flag or semaphore is used.

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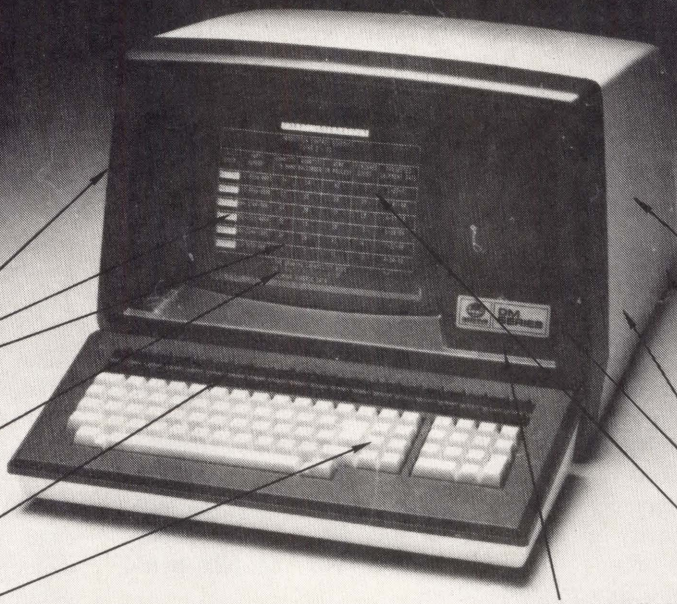

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STD-Z80 BUS Cards Permit Modular Configuration Of Motherboard Based Microcomputer System

A motherboard interconnection system, the STD-Z80 BUS system, permits an MD Series™ card to mount in any slot of a 6- to 14-slot card cage specifically designed for the cards. The 4.5 x 6.5″ (11.43 x 16.51-cm) cards from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006, provide a modular system construction concept by segregating functions to separate cards. All card connections to the bus are via 56-pin edge connectors. Connections from individual boards to peripherals are made through additional board mounted connectors. Power requirements vary, depending on individual boards, but a complete system requires 5, 12, and −12 Vdc.

Foundation of the STD-Z80 BUS based microcomputer system is an MDX-CPU1 CPU board designed around the 8-bit Z80 microprocessor, with 256 bytes of scratchpad static RAM and sockets for 4k bytes of EPROM. Offboard memory is expandable to a system capacity of 65k bytes. I/O addressing is via an onboard programmable timer, and four counter/timer channels are provided. The card's multilevel interrupt structure will accept vectored interrupts.

Designed for multi-protocol asynchronous or synchronous I/O use, the MDS-SIO serial I/O card can handle asynchronous, synchronous, and synchronous bit-oriented protocols. It can generate CRC-16 and CRC-CCITT (−0 and −1) codes, and can be programmed by the system CPU for any traditional asynchronous format. The card has two independent, full-duplex serial data channels, each of which has an independent baud rate generator (110 to 19,200 baud). I/O data are presented at the card's connectors at RS-232-C levels or as isolated 20-mA current loop signals.

All required controlling/formatting/interfacing logic between the STD-Z80 BUS and one to four floppy disc drives is provided by the MDX-FLP card. This card is compatible with any Shugart-compatible floppy disc drives, and will work with 5.25 or 8″ (13.34 or 20.32-cm) single- or double-sided, single-density drives.

An MDX-SC/D card serves as a system controller/diagnostics function to verify that other MD series modules are operational. Its five 24-pin sockets can contain up to 10k bytes of user supplied EPROM memory.

The MDX-MATH, a high speed mathematics card, performs 16- and 32-bit fixed point and 32-bit floating point trigonometric and mathematical operations. It is based on the AM9511 arithmetic processing unit.

Intended to function as a universal EPROM add-on card, the MDX-EPROM/UART is a fully buffered asynchronous I/O port. A full-duplex UART is included. Up to 10k bytes of user supplied EPROM memory can be accommodated.

An MDX-EPROM memory expansion card increases EPROM memory to 32k bytes, and three RAM cards, the MDX-DRAM8, 16, and 32, provide memory capacities of 8, 16, and 32k bytes, respectively.

MDX-A/A8 is an 8-bit A-D converter card designed to operate as a 16-channel single-ended device. It has provisions for further analog expansion and input to the card via its sample and hold circuitry. Full-scale analog input range is from 0 to 5 V. Operating specifications of the card include a conversion time of 138 μs, maximum, a total unadjusted error of less than ±½ LSB, and linearity error of less than ±½ LSB.

The MDX-PIO card provides a variety of ways to input and output data. It contains two MK3881 Z80-PIO components and four independent, oncard programmable, 8-bit I/O ports, each of which has two handshake data transfer control lines.

A low cost way to generate and debug Z80 programs on the STD-Z80 BUS itself is available through the use of the MDX-DEBUG card, which has 10k bytes of masked ROM containing DDT-80 and ASMB-80 firmware for the Z80. DDT-80 is the operating system for the card, and ASMB-80 is an assembler, loader, and text editor package.

The MDX-UMC universal memory card carries eight 24-pin sockets to accommodate EPROMs, RAMs, or ROMs. Users can configure the card to meet their particular systems' requirements.

A hardware single-step card, the MDX-SST, is designed to enhance hardware and software debug capabilities. Operating in conjunction with the CPU1 and DEBUG cards, the card generates and debugs Z80 programs on the bus system.

RAM memory expansion is provided by the MDX-SRAM4 and -SRAM8 cards. The SRAM4 has eight sockets, four of which contain the company's MK4118 static memories; the SRAM8 is populated totally with eight MK4118 RAMs (8k bytes, total).

Available as a prototyping kit which aids system development, the MDX-PROTO kit consists of an 8-slot card cage with motherboard, CPU card, memory card, program development/debug card, one blank wirewrap card, and a blank extender card. Also included are an RS-232 interface cable and a Teletype interface cable. Users can implement, program, debug, and evaluate an STD-Z80 based microcomputer system.

Software available for the MD Series includes FLP-80 DOS, the operating system software (editor, peripheral interchange package, Z80 relocatable assembler and linking locator, P/ROM programmer, and file manager), MITE-80/BIOS, a multiple independent task executive, and MEDEX-80. Used in conjunction with the operating system, MITE-80 provides for asynchronous event handling. It also provides the basic services required to manage the CPU's resources in a realtime environment. MEDEX is the foundation upon which users can add their systems' card configuration details. The resulting package identifies malfunctioning hardware to the card level.

Circle 465 on Inquiry Card

(continued on page 142)

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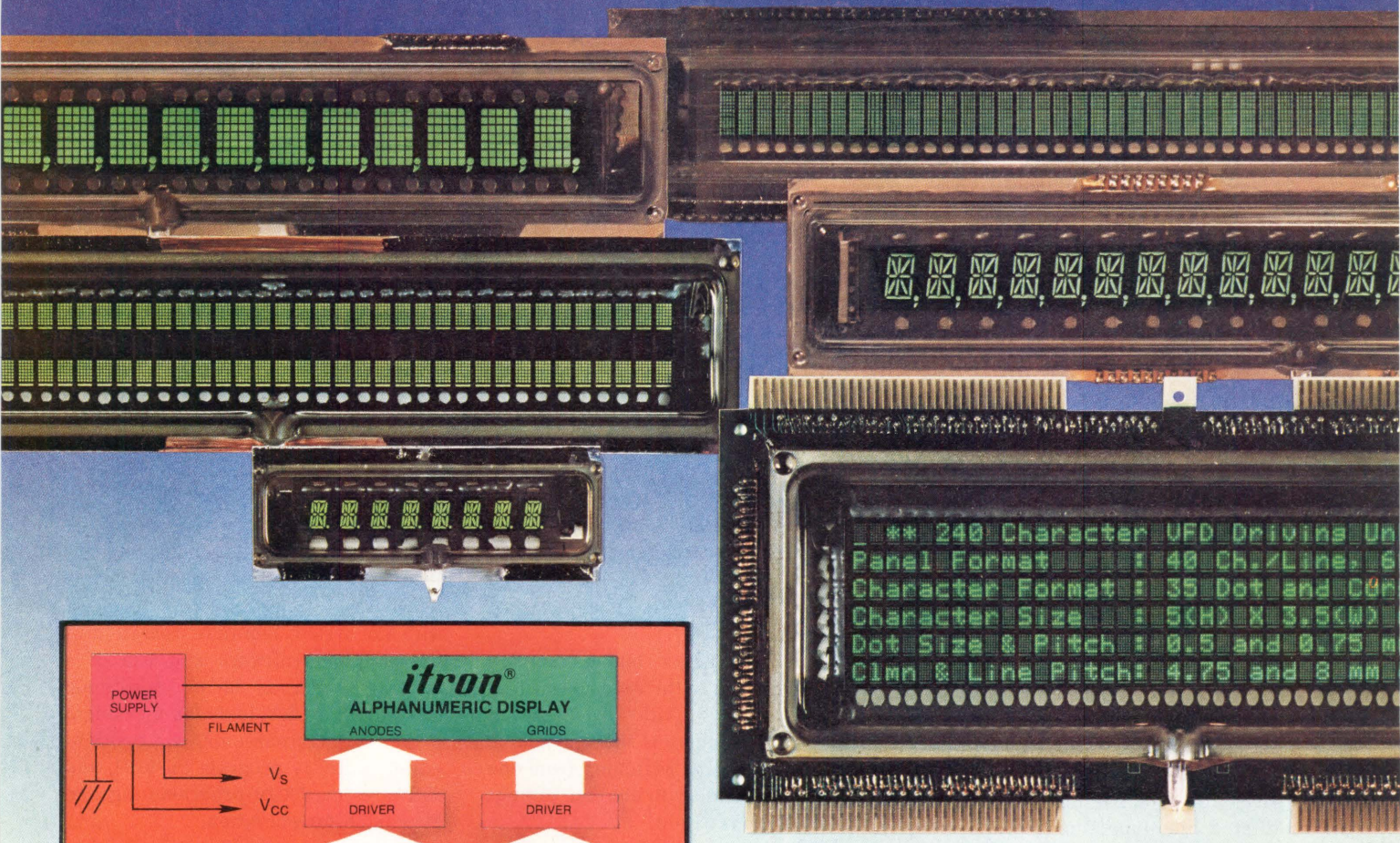

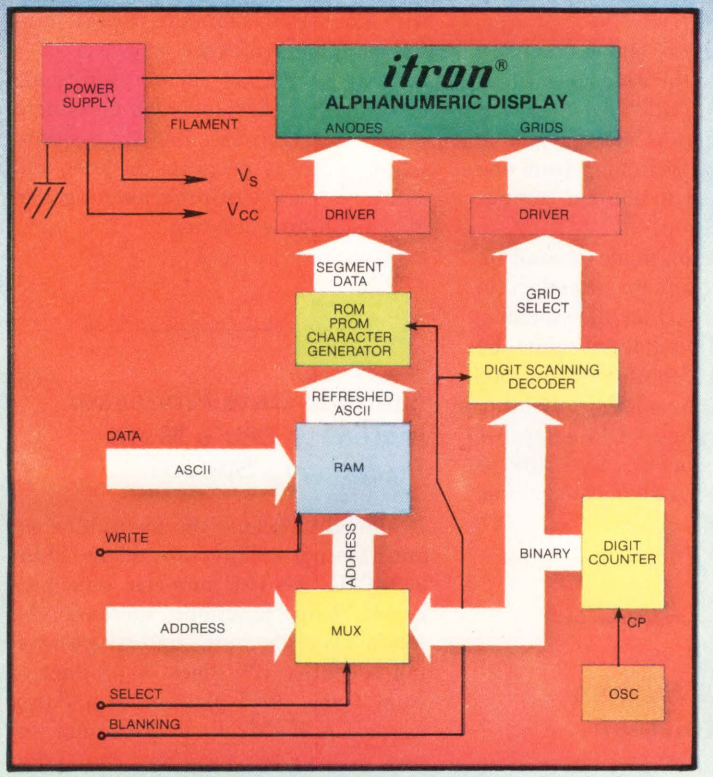

With itron's evolutionary 14-segment and dot matrix alphanumeric displays, your readout designs are sure to be frontrunners everytime. They're offered in a wide selection of character heights from 5 mm to 15 mm, and character counts that range from an 8-character 14-segment mini-package array, all the way up to the unique 240 character, 5 x 7 dot matrix (6 line x 40 characters/line) plug-in panel—and even 5 x 12 dot matrices for upper/lower case fonts.

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Microcomputer Features User Transparent Operating System

System hardware operation need be given no consideration by users because of a transparent operating system included with the Apple III microcomputer from Apple Computer, Inc, 10260 Bandley Dr, Cupertino, CA 95014. The company designed central processor features a superset of the 6502 instruction set, relocatable base page register and stack, and 128k-byte address range.

Intended for operation in expanded data manipulation and word processing, systems are available in two packages. Information Analyst includes 96k bytes of RAM, 5.25″ (13.34-cm) floppy disc drive, keyboard, two printer interfaces, and a 12″ (30-cm) black/white video monitor. The Word Processor package is identical, with the inclusion of a second disc drive. Options for the two systems include up to 32k bytes of additional RAM, additional 5.25″ (13.34-cm) disc drives (to a maximum of 4/system), either a Silentype™ or thermal type, letter quality printer, the use of a standard NTSC color video monitor, a RGB (red/green/blue) color monitor, or a standard television receiver, I/O cards for interfacing other peripheral devices, and a vinyl carrying case.

Composed of five parts—system call manager, file system, device module, event management interface, and memory manager—a sophisticated operating system (SOS) serves as a foundation for all other software development done on the system. Overlayed directly on system hardware, SOS interfaces to all system elements and isolates their operating details from the user.

Primary application interface to SOS is through the system call manager. The call manager receives and processes SOS calls from the applications running on the system, and the relevant information is collected and passed to the proper SOS module.

The file system is device independent. Every device or source of data in the system is given a file name and is placed in a hierarchy, which allows the system to perform read, write, and read/write operations with all devices or data sources. SOS acts as an interface to all elements of the system, and permits operation as either an interrupt driven or a polled system.

Data from different devices, eg, disc or keyboard, are handled by the device module. Both block- and character-oriented data may be manipulated by reading and writing exactly as much data as each device is capable of handling. Interrupts or polled events are associated with data arriving from an outside source by the event management interface.

Different devices are handled according to their type by the SOS device module. It handles blocks of data to and from block-oriented devices, such as disc drives, and it handles one character at a time when dealing with character oriented devices such as a keyboard. In effect, SOS is a device management interface, reading and writing exactly as much data as each device is capable of handling.

Memory manager makes memory use transparent to the user, permitting programs to be run anywhere in memory where there is space available and handling bank switching from one segment of memory to another without operator intervention.

Apple II emulation modes do not interface with SOS, but go directly into Apple III hardware. Once the system is in this emulation mode, it must be booted to go into another mode. SOS also permits each user's operating systems to be configured to a specific hardware arrangement, but SOS is preconfigured to handle most common peripheral devices.

Circle 466 on Inquiry Card

Development System Includes Full-Screen Editing Capability

Programming and design development for the 1802 CMOS microprocessor line may be accomplished using the CDP18S008 COSMAC Development System IV from RCA, Solid State Div, Box 3200, Somerville, NJ 08876. Featuring full-screen editing, the system includes integral CRT and keyboard, dual floppy drives, 28k bytes of RAM, CDOS disc file management operating system, resident and plug-in monitoring and debugging, built-in P/ROM programmer, and printer interface.

Full-screen editing provides instant verification of program development and changes. The keyboard has 72 keys which include all standard ASCII characters, plus 14 special function keys. Dedicated keys provide for often used functions; less used functions are provided for through use of a control key.

A 12″ (30-cm) CRT is filtered to minimize interference from ambient lighting. Display format is 80 characters on 24 lines. The integral data terminal with CRT display incorporates all system hardware except the floppy disc drive and Micromonitor debugging aid.

An additional 32k bytes of RAM may be added to the system to accommodate high level languages such as PLM 1800. Total RAM capacity is 60k bytes. The 28k bytes of RAM included with the system facilitate operation of the supplied software and use of a language such as BASIC. Additional software provided includes a resident level II macroassembler, resident editor, a utility program on ROM, and software for P/ROM programming and Micromonitor operation.

Circle 467 on Inquiry Card

Numeric Data Processor Increases CPU's Math Processing Speed

Designed to extend the instruction set and internal architecture of the 16-bit 8086 CPU, the 8087 numeric data processor chip functions increase the 8086's average mathematical processing speed by 100 times. A product of Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, the chip can use, intact, existing 8086 programs containing software floating point routines from the company's development software library.

The 8087 couples to the CPU chip, adds more than 120 instructions to the 8086/8088 instruction set, and is programmed in the same languages. Its instructions are added to the CPU's applications program, along with escape

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CIRCLE 74 ON INQUIRY CARD

(ESC) instructions. When the processor sees the ESC instruction in the instruction stream, the processor executes its instructions while the CPU executes other instructions.

8087 operation conforms to proposed IEEE standards for microcomputer floating point arithmetic, and includes all options, plus extensions and additional data types. All computations are performed on the processor in a temporary real 80-bit format, which provides the highest precision. Up to eight temporary real numbers are maintained in a stack of eight 80-bit registers and all computation centers on these registers. Conversion to and from six other standard data formats is automatic.

A 68-bit arithmetic logic unit (ALU) provides high speed and maximum precision for subtract, multiply, divide, square root, and remainder functions. The data path is also 68 bits wide, so operands can be moved quickly.

Circle 468 on Inquiry Card

Diagnostic Emulator Includes Logic State Analyzer Functions

In addition to emulation of 8080A, 8080A-1, 8085A, and 8085A-2 microprocessors, the EM-188 Diagnostic Emulator™ also provides logic state analyzer and automatic test functions. Both realtime and single-step emulation may be accomplished. An RS-232 interface is included which operates at up to 19.2k-baud rates. The emulator allows display and alteration of all microprocessor registers, memory locations, and I/O ports.

EM-188 Diagnostic Emulator for 8080/8085 based equipment. Transparent operation does not occupy target system memory or I/O space and functions as emulator and logic state analyzer

Regional and relational breakpoints and a 250-word x 32-bit trace memory provide debugging capabilities. Regional breakpoints set a breakpoint upon access to a group of preset, user-selected locations; relational breakpoints occur after either a memory read or write followed by a second memory read or write.

Automatic test functions include RAM data and/or address test and continuous address increment for signature analysis stimulus. P/ROMs may be copied via the front socket into target system memory, or target memory may be verified against the P/ROM inserted in the front panel.

Options from Applied Microsystems Corp, 11003 118th Pl NE, Kirkland, WA 98033, include 8k-byte RAM memory mapping in two 4k x 8-bit blocks and remote control software set implemented in ROM. The remote control software and disassembly software provide formatted ASCII output with instruction mnemonics to a video terminal or printer.

Circle 469 on Inquiry Card

Graphics Interface System Provides for Versatile Displays

Consisting of two circuit boards manufactured by Cromemco, Inc, 280 Bernardo Ave, Mountain View, CA 94043, the SDI graphics interface plugs directly into the S-100 bus of any of the company's microcomputer systems. The interface can display color or black/white images with up to 756 x 484-point resolution.

Four basic modes of operation may be employed using 12k or 48k bytes of memory. For use with the interface, the company has also developed 16k-and 48k-byte 2-port memory cards on which memory is accessed through a built-in connector on the cards. Depending on software, 75 to 100% CPU utilization can occur.

Direct memory access is used to display the contents of a display memory. Each pixel of the display may be mapped from one nibble or from one bit of the display memory. Bit or nibble mapped modes are software selectable, and one part of a picture may be displayed in one mode and another part in the other mode.

In the nibble mapped mode, any 16 of 4096 possible colors may be displayed in a single picture; in the bit mapped mode, any two of these colors may be displayed in a single picture. For the black/white nibble mapped mode, there can be 16 shades of grey. A bit mapped black/white picture yields strictly a black/white display.

Circle 470 on Inquiry Card

Realtime Emulator Employs Dual Bus Structure System

Realtime simulation for both segmented and non-segmented Z8000 processors is provided for the RTE™ 16/8050 realtime emulator. Utilizing two buses, one of which serves the development system processor for memory and I/O data paths while the other is dedicated to Z8000 emulation, the problem of bus contention between the system processor and emulator is eliminated.

A product of Advanced Micro Computers, 3340 Scott Blvd, Santa Clara, CA 95051, the emulator system may be coupled with the AmSYS™ 8/8012 or 8/8014 development system to increase hardware and software development capabilities.

Basic hardware configuration of the system includes emulator, realtime trace, breakpoint and control, and program memory boards. A 1M-byte user memory map can be specified anywhere within a 16M-byte address range and may be configured with emulation and user memory intermixed on any 1k boundary. The realtime trace buffer consists of 256 48-bit bytes and provides a record of bus activity surrounding specified events.

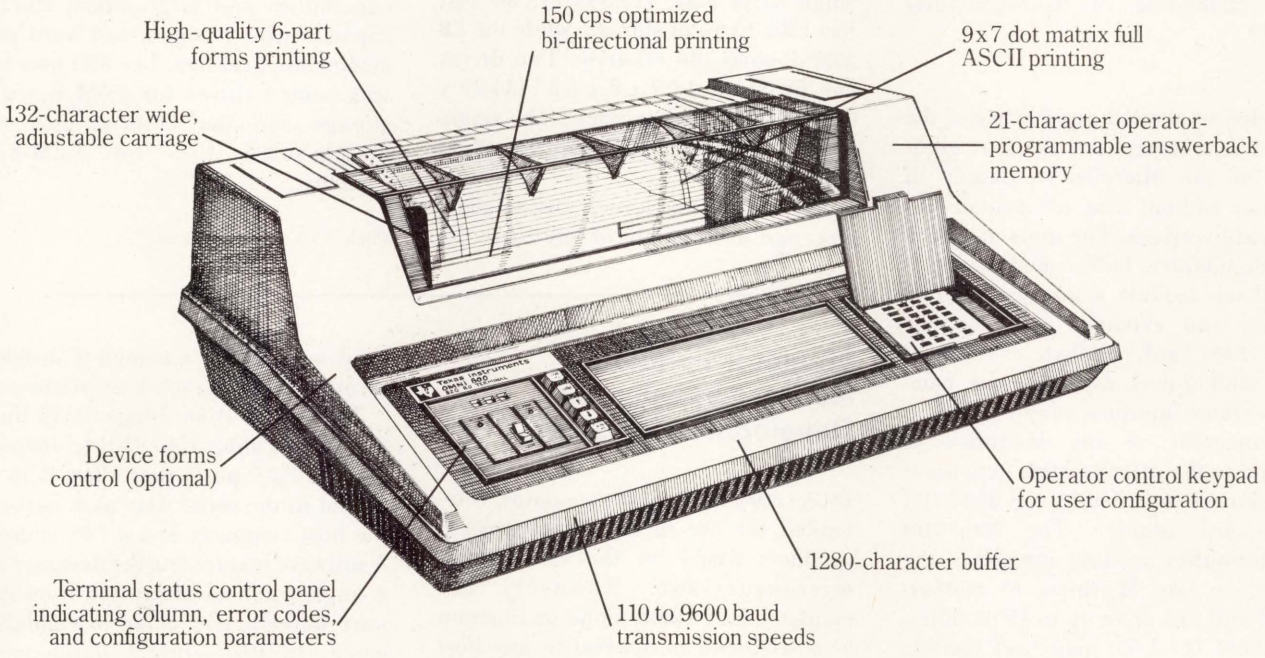
During an emulation, the CRT is divided into several windows, each of which displays specific information. Typically, one window displays Z8000 registers and status, another displays the system and normal stack, and a third window displays information as selected by the user.

Circle 471 on Inquiry Card

IMMEDIATE DELIVERY

The Associate Producer.

820 RO
Receive-Only Printer



The OMNI 800* Model 820 RO Printer has the same designed reliability as its associate, the 810 RO. With more standard features and options like expanded and compressed printing, the 820 RO offers greater flexibility for additional applications. And, should application needs change, the 820 RO is easily upgraded to a KSR model for a modest cost. The productive 820 RO Printer has all the quality and performance you associate with the OMNI 800 Family.

TI is dedicated to producing quality, innovative products like the Model 820 RO Printer. TI's hundreds of thousands of data terminals shipped worldwide are backed by the technology and reliability that come from 50 years of experience, and are supported by our worldwide organization of factory-trained sales and service representatives.

For more information on the 820 RO, contact the TI sales office nearest you or write Texas Instruments Incorporated, P.O. Box 1444, M/S 7784, Houston, Texas 77001, or phone (713) 937-2016. In Europe, write Texas Instruments Incorporated, M/S 74, B.P. 5, Villeneuve-Loubet, 06270, France.

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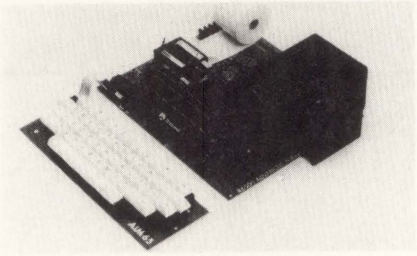
CIRCLE 75 ON INQUIRY CARD

Card Family Permits Modular Capabilities Increase for AIM 65



Modular add-ons mount on AIM 65 microcomputer to increase flexibility and capabilities of microcomputer system

Intended to expand capabilities of the AIM 65 microcomputer, the first eight units of the Microflex 65 family of modular add-ons also are available in Eurocard versions. The units include a module adapter, buffer module, 4-slot piggyback module stack, prototyping module and extender card, 8k-byte static RAM card, 16k-byte P/ROM/ROM card, and 2-port asynchronous communications interface adapter.

Connection of any Microflex 65 module to the AIM 65 system expansion connector is provided by the RM65-7101 single-card adapter. The RM65-7104 adapter-buffer module interfaces the AIM 65 to any Microflex 65 motherboard and can drive up to 15 modules. The RM65-7004 4-slot piggyback module stack (PMS) is the first available card cage and motherboard assembly in the family.

Power and return lines on the RM65-7201 design prototyping module are pre-routed and allow users to develop their own custom circuits. An RM65-7211 extender card is also available from Rockwell International, Electronic Devices Div, 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803.

Using R2114 devices arranged in two 4k-byte memory blocks, the RM65-3108 8k-byte static RAM module features include address assignment, write protect, and bank select and enable. The RM65-3216 16k-byte P/ROM/ROM module has eight 24-pin sockets, allowing installation of standard devices.

Two independent asynchronous serial I/O channels may be interfaced by the RM65-5451 ACIA module. Each may operate as a data terminal or a data set. Channel one provides RS-232-C and 20-mA current-loop interfaces, and channel two is an RS-232-C port.

Circle 472 on Inquiry Card

Compact Floppy Drives Provide Low Cost Disc Storage Availability

An intelligent controller interface provides for efficient use of the CBM 2030 series of disc storage devices. The single drive 5.25″ (13.34-cm) CBM 2031 has 130k bytes of storage, while the CB 2032 doubles the capacity. Two drives can fit in one 13.5 x 8 x 6.5″ (34.29 x 20.32 x 16.51-cm) cabinet. The single drive may be field upgraded to a dual drive version.

Said to have the lowest cost, smallest size, and least weight of any currently available drive, the 2030 series of drives from Commodore Business Machines, Inc, 3330 Scott Blvd, Santa Clara, CA 95051, are software compatible with the company's other drives.

Also available is the large capacity high performance 8″ (20-cm) CBM 8060 series, which provides software capabilities and large online storage capacities for business and word processing applications. The 8061 uses two single-sided drives for 1.6M bytes of storage and the CBM8062 uses two double-sided discs for 3.2M-byte capacity.

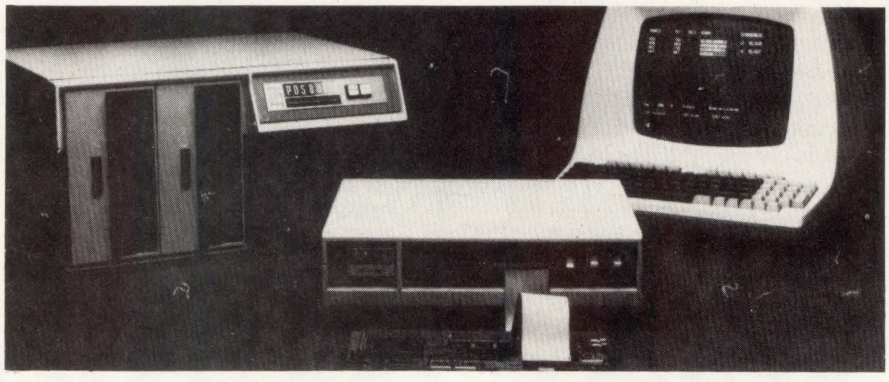
Circle 473 on Inquiry Card

Emulator Functions As Host-Independent Development System

ZSCAN 8000, an analyzer/emulator, is intended for use in developing system products based on the Z8000 16-bit microprocessor. However, the emulator may stand alone or function as a front-end peripheral to any host with an RS-232-C serial interface. Thus, users who have developed or are developing microprocessor based products on the PDS 8000 or other hosts need not acquire a complete development system for each host processor.

The system from Zilog, 10340 Bubb Rd, Cupertino, CA 95014, features dual RS-232-C ports that allow it to be placed in the serial data path between the host computer and a CRT console. A software feature lets the designer use a single command to switch from software development mode to emulation mode. In the software development mode, the system is logically transparent in the path between the CRT and host.

Circle 474 on Inquiry Card



Standalone emulator. Designed to operate with the PDS 8000 product development system, ZSCAN 8000 can also function with any host having an RS-232-C serial interface

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A programmable 16-line multiplexer that beats everything in its class*

PDP-11 users, we have another winner for you. This time it's DMAX/16™, our new programmable multiplexer for connecting your PDP-11 to 16 asynchronous serial communications lines. DMAX/16 makes the most of the 11's DMA capabilities to establish computer overhead at a level far below that of competitive units like the DJ11 and DZ11. It also offers software compatibility with the DH11... in one-fourth the space!

Now, for the first time, you don't need an expansion box or special back planes. DMAX/16 consists of two hex boards which install easily into standard SPC slots and connect to the current loop or EIA/RS-232 panel by separate flat-ribbon cable. As many as 16 units can be placed on a single PDP-11 for a total of up to 256 lines. A DMUX/16™ option allows modem control for 16 channels.

DMAX/16 provides complete program control of the lines, each of which operates with several individually programmable parameters, such as character length and number of stop bits. Parity generation and detection are odd, even or none. The operating mode is half duplex or full duplex. Fifteen software programmable baud rates: 0 to 9600 baud – plus 19,200 baud – and an external baud rate. Breaks may be generated or detected on each line and the unit can echo received characters without software intervention.

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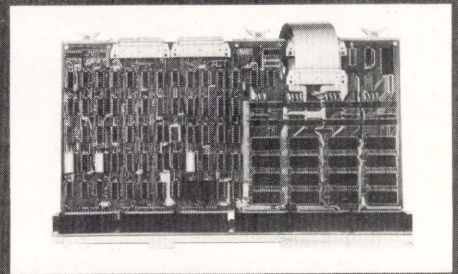

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CIRCLE 76 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

M6800 Compatible Chips Increase Systems Flexibility

Two single-chip microcomputers, a microprocessor, and an analog data acquisition unit (A-D converter) are compatible for use with the Motorola M6800 series of products. Available from Hitachi America, Ltd, 707 W Algonquin Rd, Arlington Heights, IL 60005, the HD6801 and HD6805 8-bit microcomputers contain CPU, ROM, RAM, and I/O ports on a single chip. The HD6809 microprocessor can handle 8- or 16-bit operations. The HD46508 A-D converter contains the necessary onboard peripheral circuits through which it can be connected directly to the company's HMCS6800 series family or to the Motorola M6800 series.

Offering 2k bytes of ROM, 128k bytes of RAM, 29 I/O lines, and a 16-bit timer, the HD6801 also includes an expanded 6800 instruction set, onchip serial communication interface, and 65k-byte memory expansion capability. The HD6805 offers 1.1k of ROM, 64 bytes of RAM, 20 I/O lines, and an 8-bit timer with 7-bit prescaler.

Enforced registers, along with two 16-bit index registers, two 16-bit indexable stack pointers, two 8-bit accumulators, direct addressing throughout memory map, and an expanded instruction set are provided in the HD6809 microprocessor. A total of 1464 instructions with unique addressing modes is available.

Circle 475 on Inquiry Card

Microcomputer System Operates as Text And Business Processor

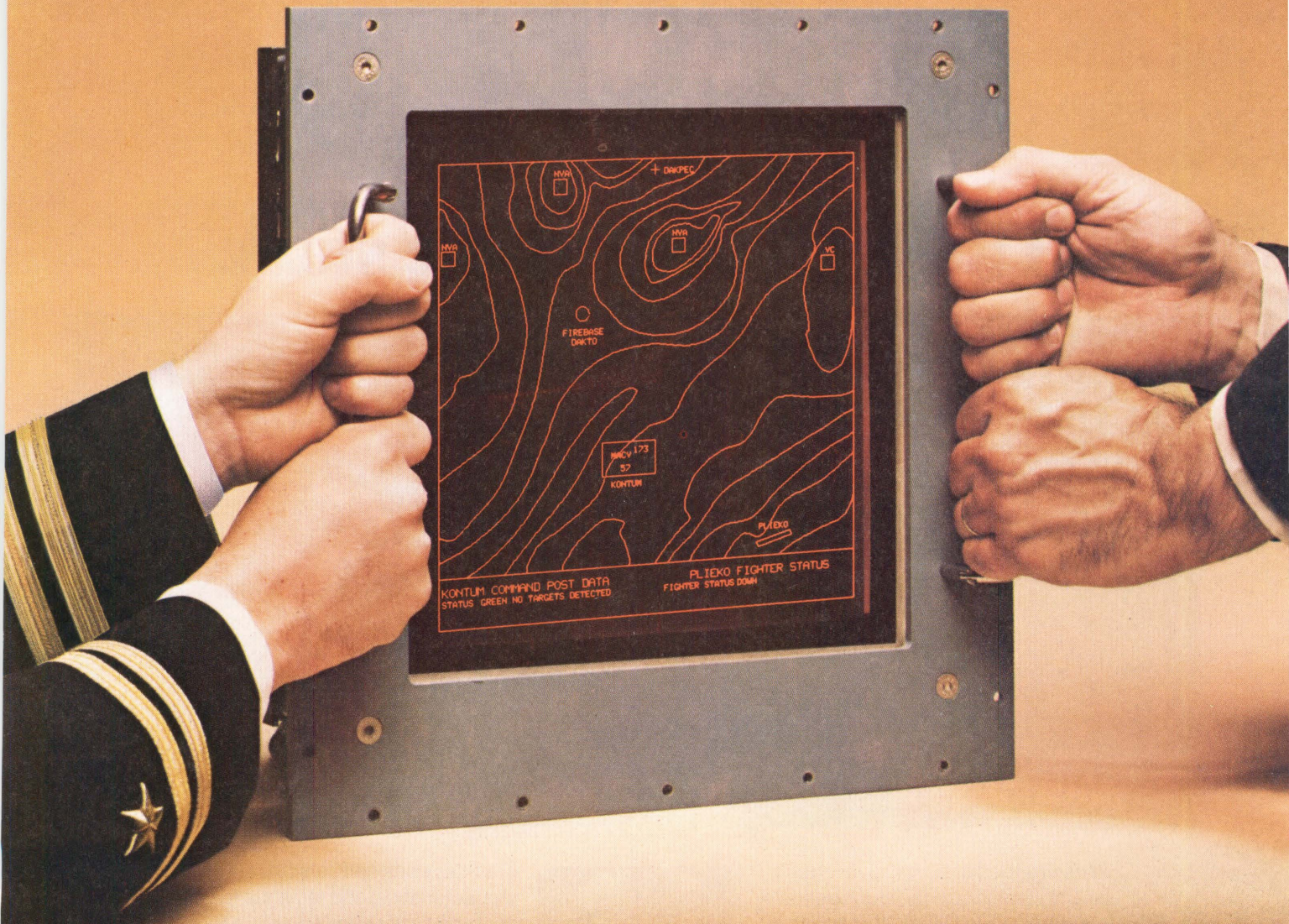
Offering multiple programming languages, communications protocols, text processing, and business application systems, the Astra 205 is intended to operate as a standalone small business system. Additional capabilities allow the system to operate as a member of an Astra Series network or to access IBM networks under 3780 or 3740 batch or asynchronous modes. The system uses a 16-bit microprocessor with 114 business EDP-oriented instructions and supports COBOL, BASIC, and a macroassembler.

Applications software includes a text processing program (Astra Write), sales order processing and analysis, inventory control, billing control, accounts receivable and payable, general ledger, and payroll packages.

Modular expansion features included in the system from NEC Information Systems, Inc, 5 Militia Dr, Lexington, MA 02173, permit a typical configuration of 128k bytes of main memory expandable to 256k, two 1.2M-byte, double-sided, double-density disc drives (expandable to four drives, total), and a 120 char/s matrix printer, with a Spinwriter printer option.

Circle 476 on Inquiry Card

Until today you couldn't get your hands on a plasma display without the terminal. Today you can.



Introducing Interstate's PDA 300 Plasma Head. Tough, bright, with more than 10,000 hours of service life.

Now you have the flexibility to design in a rugged, long-life plasma display in tough system environments with Interstate's flat-panel PDA 300 Display Head. It displays alphanumerics/graphics, and is TTL compatible for easy interface. Inherent memory eliminates display refresh, and the unit is totally digital with no analog circuits. It has a thin profile and is designed to help meet your system RFI/EMI requirements. Optional equipment includes a touch panel, variable brightness control, rack mount, and remote-mounted power supply.

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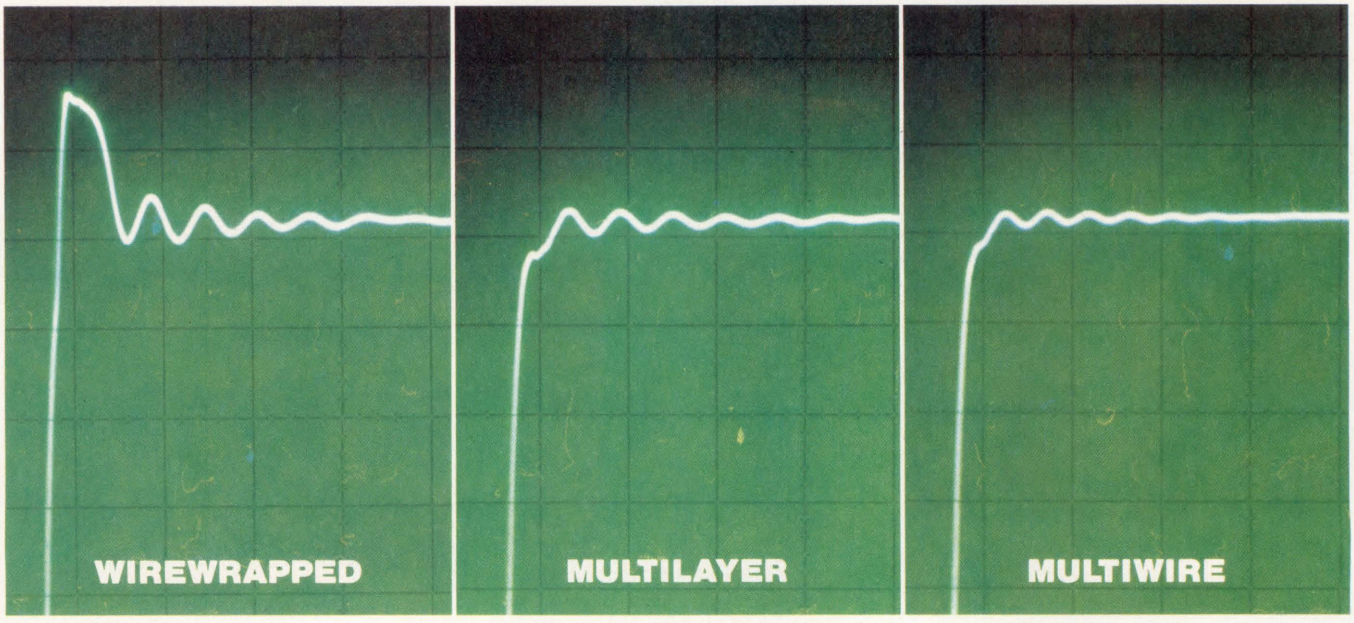

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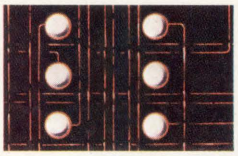

A typical example of the circuit density achievable with Multiwire circuit boards.

Multiwire, 31 Sea Cliff Avenue, Glen Cove, NY 11542. Phone (516) 448-1307

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CIRCLE 79 ON INQUIRY CARD

Multibus Compatible Modules Provide Interfacing Flexibility

Two general purpose bus foundation modules and a universal wirewrap module from MDB Systems, Inc, 1995 N Batavia St, Orange, CA 92665, permit a flexible interface between 8- or 16-bit Intel computers and user peripheral devices. Each general purpose bus foundation module contains basic Multibus logic elements, plus wirewrap positions for up to 38 IC devices. With wirewrap posts on the component side of the board, the modules fit a single slot in the computer chassis. Designer wired options permit multiple controller applications, address selection, and interrupt control and the modules have provision for three 50-pin ribbon cable connectors.

Up to 60 low-profile sockets, or ICs, in combination from 14- to 40-pin packages, may be contained on the universal wirewrap module. Wirewrap posts are on the component side of the board for 0.5" (1.27-cm) spacing in a single chassis slot. Three I/O positions are provided at the top of the module for use with 16- to 50-conductor ribbon cable edge connectors to external devices or modules.

Circle 477 on Inquiry Card

Desktop Unit Houses Complete Development System

Packaged as a standalone desktop system, the MC6809 based EXORset 30 software and hardware development system consists of a total of 48k bytes of RAM, provision for up to 24k bytes of ROM/P/ROM, with development and debug firmware, ASCII keyboard, dual mini-floppy disc drives, and CRT. Designed to facilitate software development for MC6809 systems, the system has two unfilled bus slots which can be used by users to interface Micromodules or compatible custom modules.

Two controller boards are used in the system from Motorola Semiconductor Products, Inc, PO Box 20912, Phoenix, AZ 85036. System timing and control functions are handled by a main control board, while disc drive tasks are executed by a second board. The main control board has three peripheral interface adapters, programmable timer for a realtime clock, and an RS-232-C port; 32k bytes of undedicated RAM are contained onboard.

EXORbug, the 4k-byte system monitor firmware handles system initialization, interrupts, command interpretation, and object program debugging. Compatibility with EXORciser's firmware allows any user program designed for the EXORciser also to run with the system.

Formats for the 9" (23-cm) CRT are 16 or 22 lines by 80 characters. Graphics capabilities are user selectable through keyboard or software control and provide a 320-column, 256-row dot pattern on which alphanumerics may be superimposed.

Resident disc drive firmware includes entry points for user insertable special disc handling routines. XDOS, the disc operating system, is compatible with MDOS, the EXORciser file manager.

Circle 478 on Inquiry Card

Prototyping Boards Offer Design and Breadboarding Versatility

Four Multibus™ compatible boards configured to meet specific design requirements comprise the Multicircuit prototyping family. All are designed to work with iSBC microcomputers in all modes of operation and contain a user defined power bus, which accepts bus distribution strips, three I/O connectors (26, 40, and 50 pins), a ground plane on the circuit side, and a solder mask. Connections for power, bus, interrupt, address, and data are defined on each board from Artec Electronics, Inc, 605 Old County Rd, San Carlos, CA 94070.

Configured in a 105 x 48, 0.1" (0.254-cm) grid array, the Multicircuit board can accept up to 130 16-pin wirewrap sockets. The Multipower board has a solder pad arrangement for dc-dc converters and a 6.75 x 12.0" (17 x 30-cm), 0.1" (0.254-cm) grid array which can contain a maximum of 120 16-pin wirewrap sockets. The Multipurpose Interface/Multipower board contains solder pads for dc-dc power and interface logic, with space for 90 16-pin wirewrap sockets.

Included on the Multipurpose Interface board are complete buffering and control logic arranged for 16-bit address and 8-bit data such that all 8-bit Multibus-compatible microcomputers may be interfaced. Address and data buses may be expanded to 20 and 16 bits, respectively. Switch-selectable 12-bit address decoding and buffered interrupts are available. Memory mapping or programmed I/O interfacing are also switch-selectable. Space for up to 95 16-pin wirewrap sockets is provided.

Circle 479 on Inquiry Card

SOFTWARE

Software Tools Provide for Efficient Systems Operation

First of three software introductions from Microsoft, 10800 NE Eighth, Ste 819, Bellevue, WA 98004, is a BASIC interpreter for the Z8000 CPU. Called BASIC-Z8000, the interpreter utilizes the Z8000 instruction set to provide what is claimed to be the fastest BASIC interpreter available. Increased execution speed is attributable to math functions design and instruction histogramming of non-math portions. The accuracy of internal calculations is in excess of eight digits for single precision and 18 digits for double precision. Double precision range of exponents is from −308 to 308.

MS-Pascal, the second software tool, is a true compiler, and includes optimizer and modular code generators for 8080, Z80, 8086, Z8000, and a pseudo machine. Adaptable to system programming, MS-Pascal is divided into four levels, metalanguage, standard, extended, and systems. Metalanguage $STANDARD enforces use of ISO standard only and includes conditional compilation and $INCLUDE, and $EXTEND and $SYSTEM.

Enhancements include expanded string support, UNITS and USES interfaces, a machine oriented WORD type, dynamic and conformant arrays, and attributes for variables and procedures. Low level escapes such as direct access to memory locations, call to assembly language subroutines, and a RETYPE function are also provided.

Version 4.0 of the company's COBOL-80 compiler for 8080, 8085, and Z80 includes full screen interactive ACCEPT/DISPLAY and SCREEN SECTION (compatible with Data General Interactive COBOL), CHAIN with argument passing, and segmentation to ANSI standard level 1. Additional features of the release are full COPY, trace-style

debugging, and ASCII, packed, and binary data formats. A portable source language permits translation for additional processors. Capable of supporting up to 8M bytes of files and providing sequential, line sequential, relative, and indexed file types, version 4.0 operates with CP/M, 1.3, 1.4, and 2.X, and is compatible with ISIS-II, IMDOS, CDOS, TEI's TDOS, and model II TRSDOS operating systems.

Circle 480 on Inquiry Card

High Level Language for North Star Executes Ten Times Faster than BASIC

A software system for the North Star computer provides an integrated disc based system which includes interactive FORTH compiler, an assembler for both 8080 and Z80, disc file system, and text editor. Both single- and double-density disc operating systems may be accommodated. Included is a partial source for text editor, utilities, and assembler. The system requires 24k bytes of memory.

Based on FORTH, and modeled after fig-FORTH (FORTH Interest Group, PO Box 1105, San Carlos, CA 94070), OmniFORTH, from Interactive Computer Systems, Inc, 6403 Dimarco Rd, Tampa, FL 33164, is a high level language whose program development time is reduced because continuous interaction allows immediate testing and debugging. The system is extensible, which allows defining new words to expand the applications possibilities. Applications written in high level definitions can be transported between computer systems because the system is compatible with standards developed by the FORTH International Standards Team. □

Circle 481 on Inquiry Card

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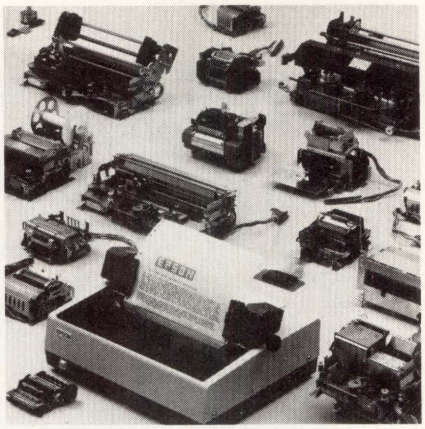

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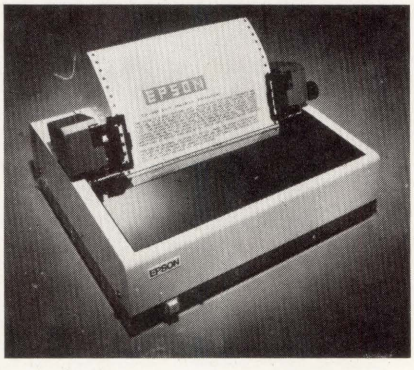

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DIGITAL SIGNAL PROCESSING SYSTEMS MOVE TO FLOATING POINT ARITHMETIC— PART 1: ADVANTAGES OF VLSI

Louis Schirm IV

TRW LSI Products
2525 E El Segundo Blvd, El Segundo, CA 90245

For the past decade, the vast majority of digital signal processing systems (Fig 1) have been based on fixed point arithmetic, which has been the fastest way to perform the necessary operations. Now, however, the designers of these systems are moving to floating point for the same reason that general purpose computer users have done so over the last few years: floating point provides a wider dynamic range for the same number of bits.

In digital signal processing (DSP) systems, the worst case application determines whether fixed or floating point processing is needed. Fixed point arithmetic is adequate for 1-dimension (1-D) signal processing that involves a small amount of calculation-induced word growth. Examples of 1-D processors are digital filters and fast Fourier transforms (FFTs), where 16 bits of fixed point precision are sufficient if the inputs are significantly less than 16 bits.

In multidimension processing, however, each additional dimension adds its own bit growth requirement above and beyond the input precision. Speech recognition, for example, might break down a 1-s duration sound input into a 2-dimensional array of coefficients and then compare that array with a library of known words. Although data precision does not grow appreciably in this case, the dynamic range requirement grows beyond the capabilities of reasonable fixed point hardware. For these reasons, most speech recognition research is currently done on large computers or array processors where floating point arithmetic is used to achieve 24 bits of precision in a 2^{280} dynamic range.

Fig 2 illustrates the dynamic range advantages of floating point over fixed point. As shown, a dynamic range of 10^{24} requires 80 bits in a fixed point system, whereas only 22 bits are necessary for a floating point system. These 22 bits are divided into 16 bits of mantissa and 6 bits of exponent.

Obviously, the resolution of the floating point system is not as good as the fixed point system for a given system word size, but in many cases this is not a problem. In speech

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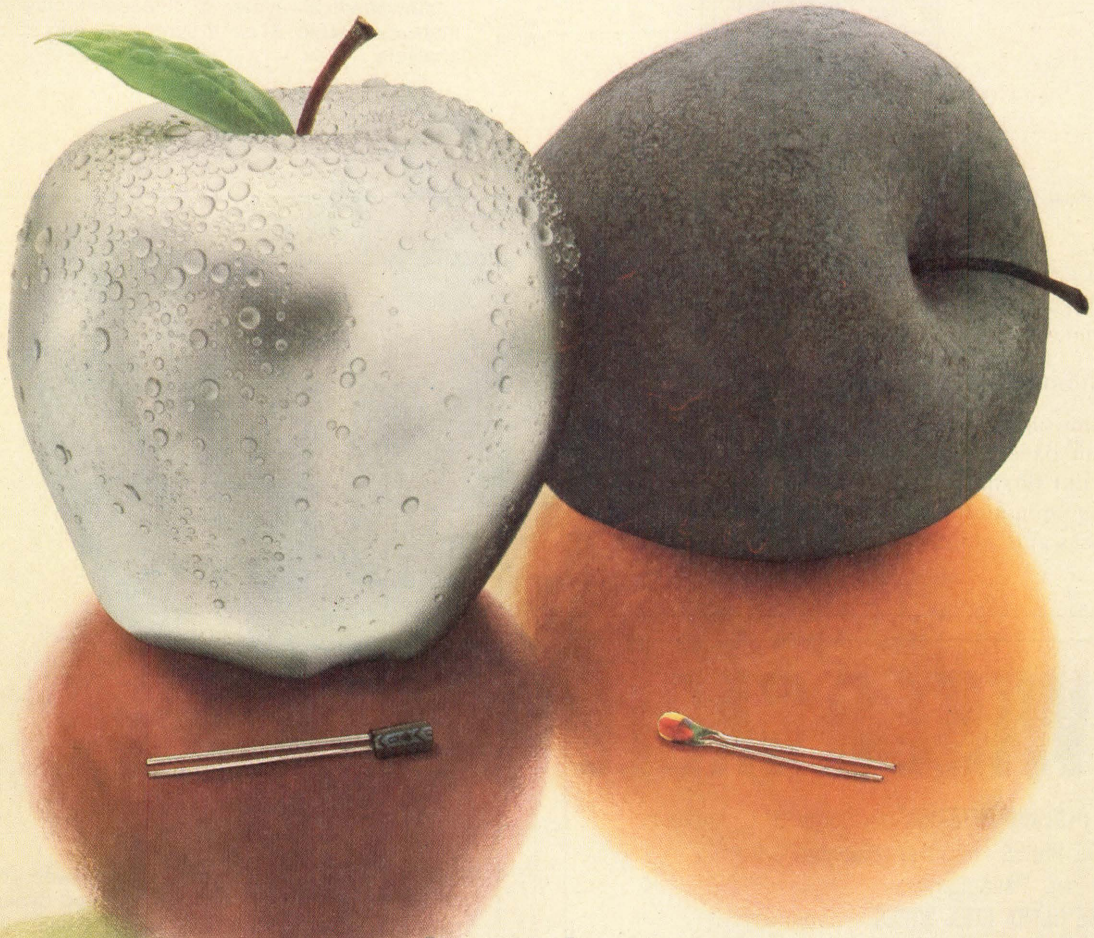

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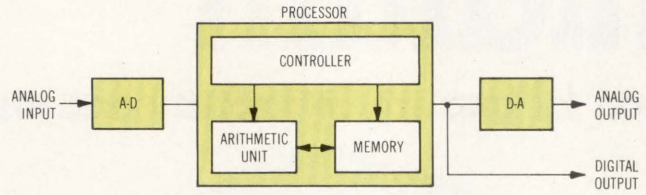

Fig 1 Typical digital signal processor (DSP). ADC and DAC interface digital processor to external analog environment, with both digital and analog outputs being used in some cases. DSP applications can be found in TV and other video processing, geophysical exploration, radar/sonar, medical systems, telecommunications, instrumentation, speech synthesis, and speech analysis

recognition and imaging systems, the advantages of broad dynamic range override the reduced resolution of floating point arithmetic.

Multiplication and Addition

Multiplication in floating point is only slightly more complex than in fixed point. Each requires a single multiply operation, but floating point requires an addition as well. The floating point multiplication consists of multiplying the two mantissas and adding the two exponents.

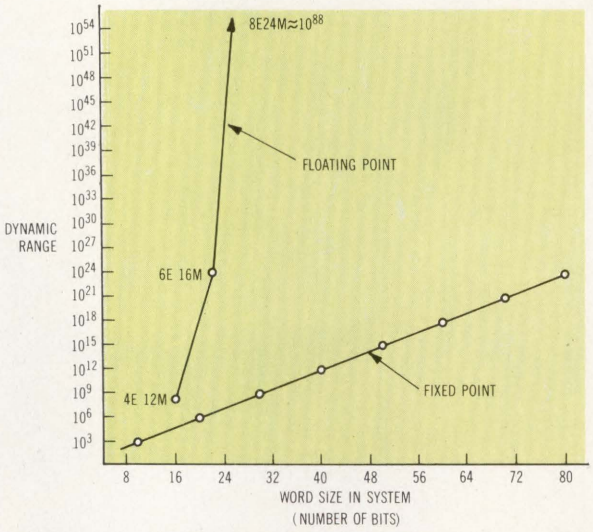

Fig 2 Dynamic range comparison between fixed point and floating point systems. As required dynamic range increases, advantage of floating point rises sharply

On the other hand, addition in floating point is much more complex than in fixed point. The reason for the greater complexity is the interrelationship between the exponent and mantissa in floating point addition. That is, the exponents of the two numbers must be examined before the addition is performed, in order to establish the proper numerical relationship between the two mantissas that are to be added. In floating point multiplication, there is no direct interrelationship between the mantissas and exponents, and each can be treated independently.

Another difference beween the floating point adder and multiplier is the availability of very large scale integration (VLSI) to simplify the design of these arithmetic functions. Floating point multiplication can be achieved with available multiplier VLSI and a few medium scale integration (MSI) chips. It is not yet possible to make extensive use of VLSI for high speed floating point addition, but such chips are under consideration.

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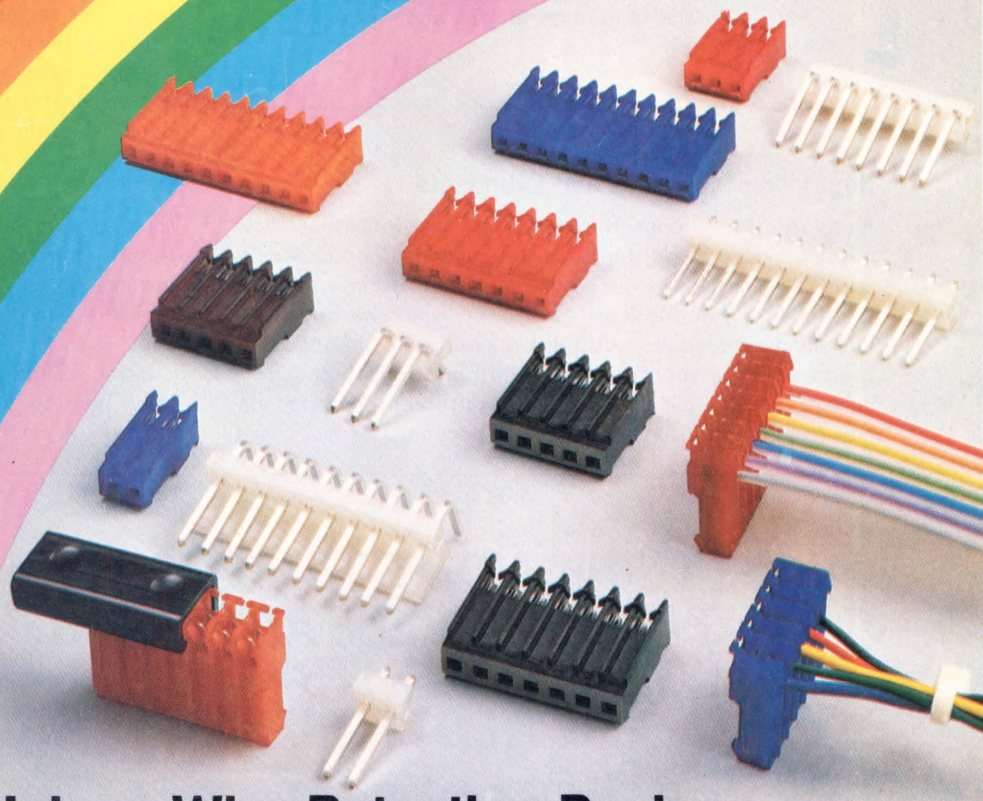

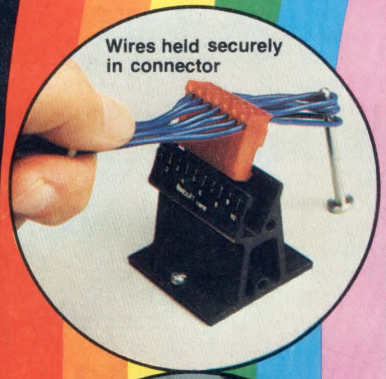

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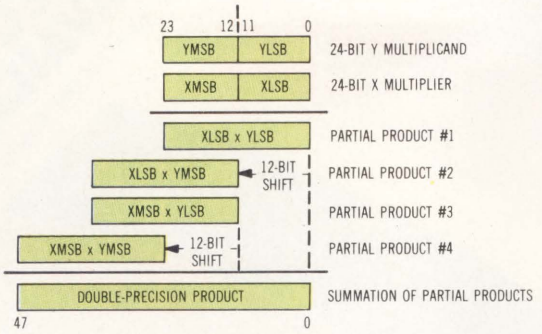


Fig 3 24- by 24-bit multiplication using 12- by 12-bit multiplier. Algorithm utilizes summation of partial products

Separating Mantissas and Exponents

Many of the present floating point multiplication techniques involve 32-bit words. In this case, the 8-bit exponent and 24-bit mantissa are first separated from both the multiplier and multiplicand. Then, the exponents are added and the mantissas are multiplied to obtain the floating point product. In one approach, the 24-bit multiplication can be accomplished using a 12- by 12-bit multiplier integrated circuit (IC) and additional control and accumulator ICs.

Fig 3 illustrates the 24-bit multiplication concept for a 12- by 12-bit multiplier. First, the 24-bit multiplier and multiplicand are separated into the most significant and least significant 12 bits. Then, 12-bit multiplication is performed on the XLSB and YLSB to obtain the first partial product. Next, the second and third partial products of the XLSB and YMSB and the XMSB and YLSB are obtained. These two partial products must be shifted 12 bits relative to the first partial product to maintain the proper relationship to partial product number one. The fourth partial product involves the XMSB and YMSB, which must be shifted an additional 12 bits. A 48-bit double-precision product is produced by summing the four partial products in succession.

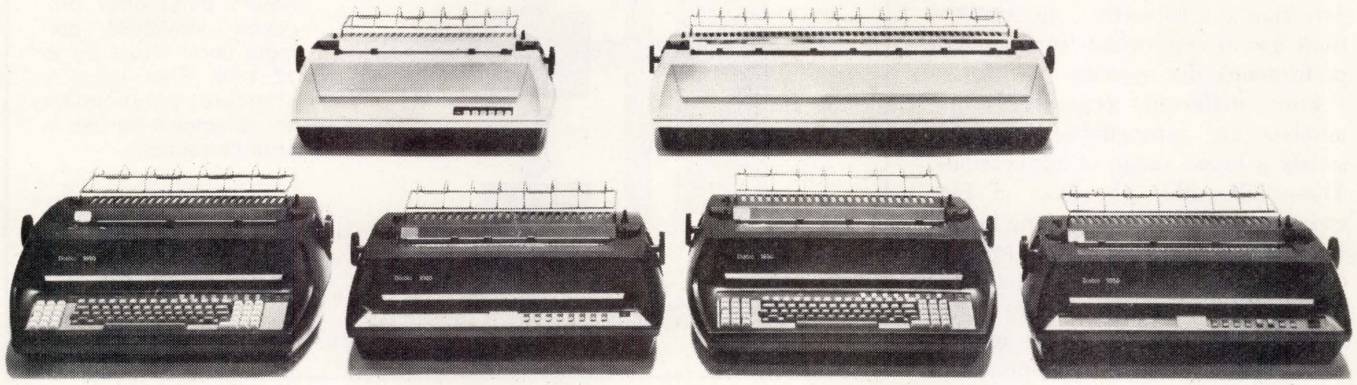
The final product may then be normalized to maintain the proper range for the mantissa, ie, between 0.5 and 1.0. This may involve changing the exponent to the next lower or higher value if any shifts occurred in the normalization. If desired, this result can be rounded to reduce truncation errors when the answer must be single precision.

Summary

Floating point arithmetic is beginning to see more use in digital signal processing systems. Multiplication can now be performed easily using an available 12- by 12-bit multiplier VLSI chip. VLSI to perform floating point addition is the next step.

In the second of this 3-part series, the hardware details of 32-bit floating point multiplication will be described. Part 3 will explain floating point addition.

The Workaholics.



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CIRCLE 88 ON INQUIRY CARD

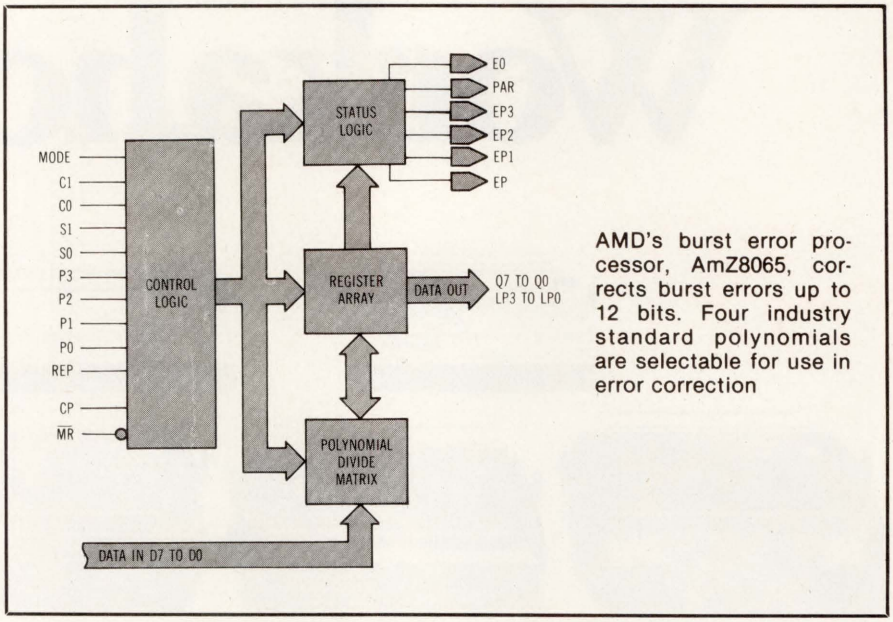
LSI Chip Detects 12-Bit Burst Errors

A general purpose burst-error processor (BEP) from Advanced Micro Devices, 901 Thompson Pl, Sunnyvale, CA 94086, can detect and allow correction of up to 12-bit burst errors in serial data streams moving at up to 20M bits/s. Operating as a peripheral interface circuit for serial or parallel detection and correction, the AmZ8065 finds use in applications such as high performance disc systems.

Four different generator polynomials are internally encoded to satisfy a broad range of applications. These fall within the class of Fire codes, multiple-error correcting binary codes for nonindependent errors, in common use by most disc manufacturers. The industry standard codes implemented in this chip include 48- and 56-bit polynomials popularized by IBM and 32- and 35-bit polynomials favored by the minicomputer industry. These four Fire codes cover over 80% of all applications for burst error processing.

In operation, the BEP divides the data stream by the selected polynomial and appends the resulting remainder, the check word, to the data stream. When this data stream is read out, the device again performs the data stream division, a remainder of zero indicating no errors. If the BEP detects an error, onchip facilities are used to extract the burst error pattern and its location in the data stream and to correct the error. The circuit can handle any number of bits in error, as long as the distance between the first and the last error is 12 or fewer bits. This is the "burst" error common to disc drives.

For greater flexibility, the chip provides two read modes, normal and high speed, which determine the correction methodology if an error is found. The normal or full period clock-around method is the present methodology used in industry because it requires less hardware to implement. This is an exhaustive algorithm providing a worst case correction time equal to the natural period of the Fire code selected: 42,987 clock periods for the 32-bit code, 94,185 for the 35-bit code, over 500k for the 56-bit code, and diverging virtually infinitely for the 48-bit code.



AMD's burst error processor, AmZ8065, corrects burst errors up to 12 bits. Four industry standard polynomials are selectable for use in error correction

Without losing any accuracy, the user can select the high speed correction method based on the Chinese Remainder Theorem. This method computes the error location and the correction needed. To illustrate its effectiveness, it lowers the worst case time for a correction using the 56-bit Fire code from over 500k clock periods to a maximum of 111. The 48-bit Fire code is not well suited to either methodology. Here, the BEP employs a reciprocal polynomial that lets the user approach the data stream from the check bits side. This reduces worst case correction time to the length of the data stream.

Write data are entered on the fly into the BEP, while blocks are written to the associated disc, and check bits are extracted following the last data byte. Read normal mode performs extraction of the error pattern and location while a read high speed mode allows direct division of data by the factors of the generator polynomial. A divide mode generates output check bits and validates data. Compute mode initiates a data correction process by locating and outputting the error pattern for correction.

The device achieves its 20M-bit/s data-rate handling capability by accepting data as serial bytes. This reduces the single-phase clock requirement to a manageable 2.5 MHz. Additional characteristics include operation from a single 5-V supply and packaging in a 40-pin DIP. The part will also be available as the general purpose Am9520 burst error processor.

Circle 501 on Inquiry Card

16k EEPROM Claimed As Industry First

An electrically erasable programmable read only memory having a 350-ns max access time is said to be the world's first 16k EEPROM. Offered by Hitachi America, Ltd, 707 W Algonquin Rd, Arlington Heights, IL 60005, the HN48016 utilizes N-channel silicon gate MNOS (metal nitride oxide semiconductor) process technology.

The manufacturer indicates that this memory outperforms existing P-channel aluminum gate EEPROMs whose limits have included a max memory capacity of 8k bits and a fastest max access time of 650 ns. This EEPROM is also favorably compared to

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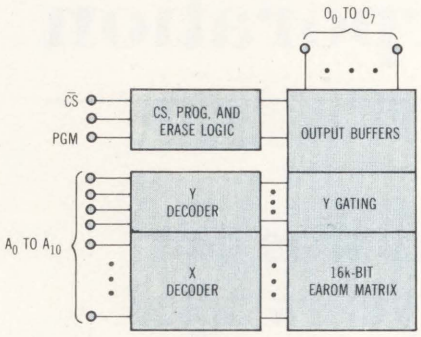


Electrically erasable programmable read only memory, HN48016, from Hitachi provides 350-ns max access time. Device is said to be first 16k EEPROM on market

standard versions of the 2716 family of UV-erasable 16k EPROMs whose max access time is 450 ns.

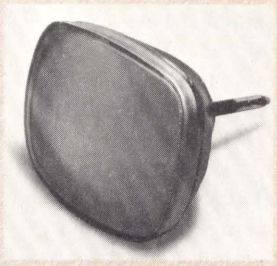
Compatibility with the 2716 family is a key attribute of the 24-pin, dual in-line device, which uses a single 5-V supply in the read mode, with 5- and 25-V supplies required during erasure or programming. Organized as 2048 x 8, the memory can accept up to 1000 programming and erasing cycles, retaining data for over 10 years at 85 °C.

Applications include control programs of microprocessors and terminal equipment, operating programs or calibration data storage in controllers or measuring equipment, and logging of a system's operating history. The memory also finds use in the online storage of data that must be preserved in the event of a power failure.

Inputs and outputs are TTL compatible during read, program, and erase modes, and 3-state outputs are also featured, providing an OR-tie capability. The device is fully static, requiring no clocks. Other characteristics include onchip address decode, power dissipation of 300 mW (max), typ access time of 250 ns, use of a 10-ms programming pulse, and total erasure of all bits in 1 s.

Absolute maximum ratings require that all input and output voltages relative to ground stay between −0.3 and 7 V and that supply voltage relative to ground stay between −0.3 and 28 V. Temperature must remain between 0 and 70 °C in operation and between −65 and 125 °C in storage.

Circle 502 on Inquiry Card



With Raytheon new Beam-Penetration Color CRT's. Designed specifically for computer color-graphic system applications, Raytheon Beam-Penetration Color CRT's offer better color resolution and better overall system performance than conventional color tubes and other beam penetration CRT's.

Available in 15″ to 25″ diagonal rectangular and 10″ to 23″ dia. round sizes, Raytheon Beam-Penetration Color CRT's feature the unique Raytheon patented split-anode design. And this means faster switching, constant focus voltage and good spot size for all colors.

Such tubes are just one example of Raytheon's wide choice of versatile, performance-proven CRT's that are available in a variety of electron-gun types and phosphors and in all shapes and sizes 3″ to 25″.

Color it right. Color it with Raytheon Beam-Penetration Color CRT's. For complete information, contact the Marketing Manager, Raytheon Company, Industrial Components Operation, 465 Centre St., Quincy, MA 02169. (617) 479-5300.

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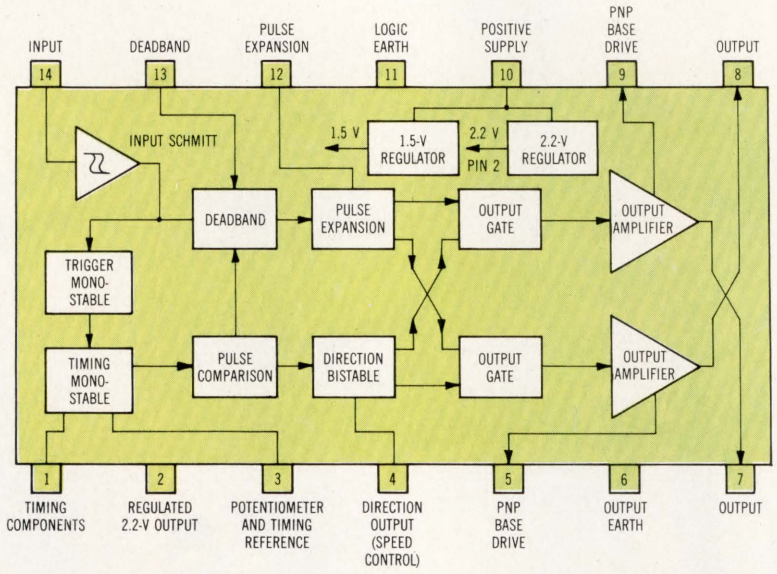
CIRCLE 91 ON INQUIRY CARD

IC Varies Pulse Widths To Control Servos



Precision servo integrated circuit, ZN419CE, from Ferranti Electric uses pulse width modulation in control applications. Chip governs remote machinery operation

Designed for pulse width position servomechanisms used in control applications, the ZN419CE is a monolithic integrated circuit, mounted in a 14-pin DIP. This chip from Ferranti Electric, Inc, 87 Modular Ave, Commack, NY 11725, controls the speed, direction, and position of remote machinery. The device utilizes time division multiplexing and requires few external components.

Features of the servocontroller include low power consumption—typically 7-mA quiescent current drain at a V_{cc} of 4.8 V—high current complementary output drive capability, Schmitt trigger input shaping, onchip precision voltage regulators, and reversing relay output for dc motor control. Balanced deadband control increases battery life by eliminating hunting around the quiescent position that is caused by servo inertia and overshoot.

In a typical radio control servo application, a control stick varies the pulse width of a timing circuit and many such pulses are time division multiplexed, typically modulating a 27-MHz transmitter. A receiver then decodes the transmitted signal and reconstitutes an independent train of pulses for each servo channel.

Maximum ratings require that supply voltage not exceed 6.5 V and that package dissipation remain ≤ 300 mW. Temperature must remain between -20 and 65 °C in operation and between -65 and 150 °C in storage.

Circle 503 on Inquiry Card

Speech Chip Includes Onboard FIFO

Designed for easy interface to a standard microprocessor having an 8-bit data bus, a speech synthesis processor with an onboard first in, first out buffer has been added to the family of Solid State Speech™ chips from Texas Instruments Inc, PO Box 1443, Houston, TX 77001. The TMS5200, currently used in the TI-99/4 home computer speech synthesizer peripheral, is suited for a wide variety of industrial and commercial applications.

This speech chip has the capability of accepting data from either the TMS6100 (a compatible 128k-bit ROM) or the onboard 128-bit FIFO buffer. The buffer allows the storage of speech data in P/ROMs, EPROMs, RAMs, or other random access storage media such as disc or bubble memories. Organized as 16-byte parallel in, serial out, the FIFO frees the CPU to tend to other tasks during the 50 ms that it takes for the speech chip to exhaust the data in the buffer.

Additional characteristics include TTL compatible I/O, ±5-V power supplies, and single-ended output drive that simplifies output connection. Onchip interface logic permits microprocessor access to non-speech data stored in the compatible ROM. Packaging is provided in a 28-pin plastic DIP.

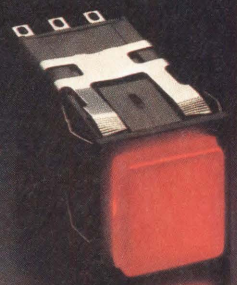
The device is manufactured using a P-channel metal oxide semiconductor (PMOS) process, also used in the recently announced TMS5100 speech chip. Speech encoding on these chips is achieved through pitch excited Linear Predictive Coding (LPC), a technique based on a linear equation that formulates a mathematical model of the human vocal tract and an ability to predict a speech sample based on previous ones.

Circle 504 on Inquiry Card

Sample and Hold Amplifier Contains JFET and Bipolar Op Amps

A monolithic sample and hold amplifier, the NE/SE5537, combines advantages of ion implanted JFETs and bipolar devices to obtain a typ 0.002% gain accuracy (with $R_L = 2$ kΩ), an acquisition time of 4 μs, and a droop rate of 0.5 mV/s for a 0.01-μF capacitor. This device from Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086, includes two operational amplifiers, which function as unity gain amplifiers (and, therefore, as a combined unity gain amplifier) in the sample mode. The first of these has bipolar input

The first LED pushbutton that's as bright as an incandescent, but doesn't burn out like one.



Our AML pushbuttons, indicators, paddles and rockers have a new light source.

A unique, dual chip LED.

Like other LED's, this one will last a long time (its half-life is 100,000 hours or more). It resists shock and vibration. It uses only half the current of an incandescent. It will save you money on repairs. And comes in red, yellow and green.

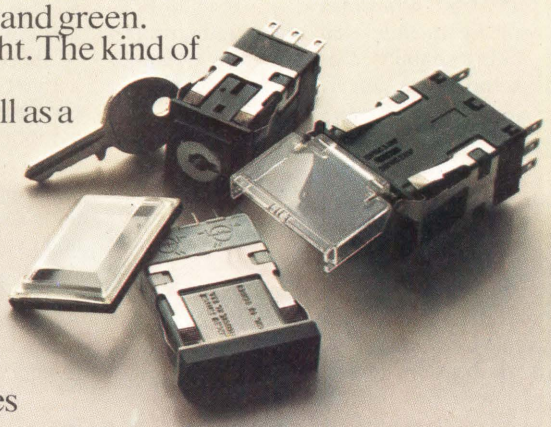
But unlike all other LED's, this one is very bright. The kind of brightness you'd expect from an incandescent.

And a special adapter makes it as easy to install as a standard T1¾ wedge base.

In addition to this one very 'bright' idea, we've made some other additions to the Advanced Manual Line. Like a keylock switch, a protective panel seal, and a switch guard.

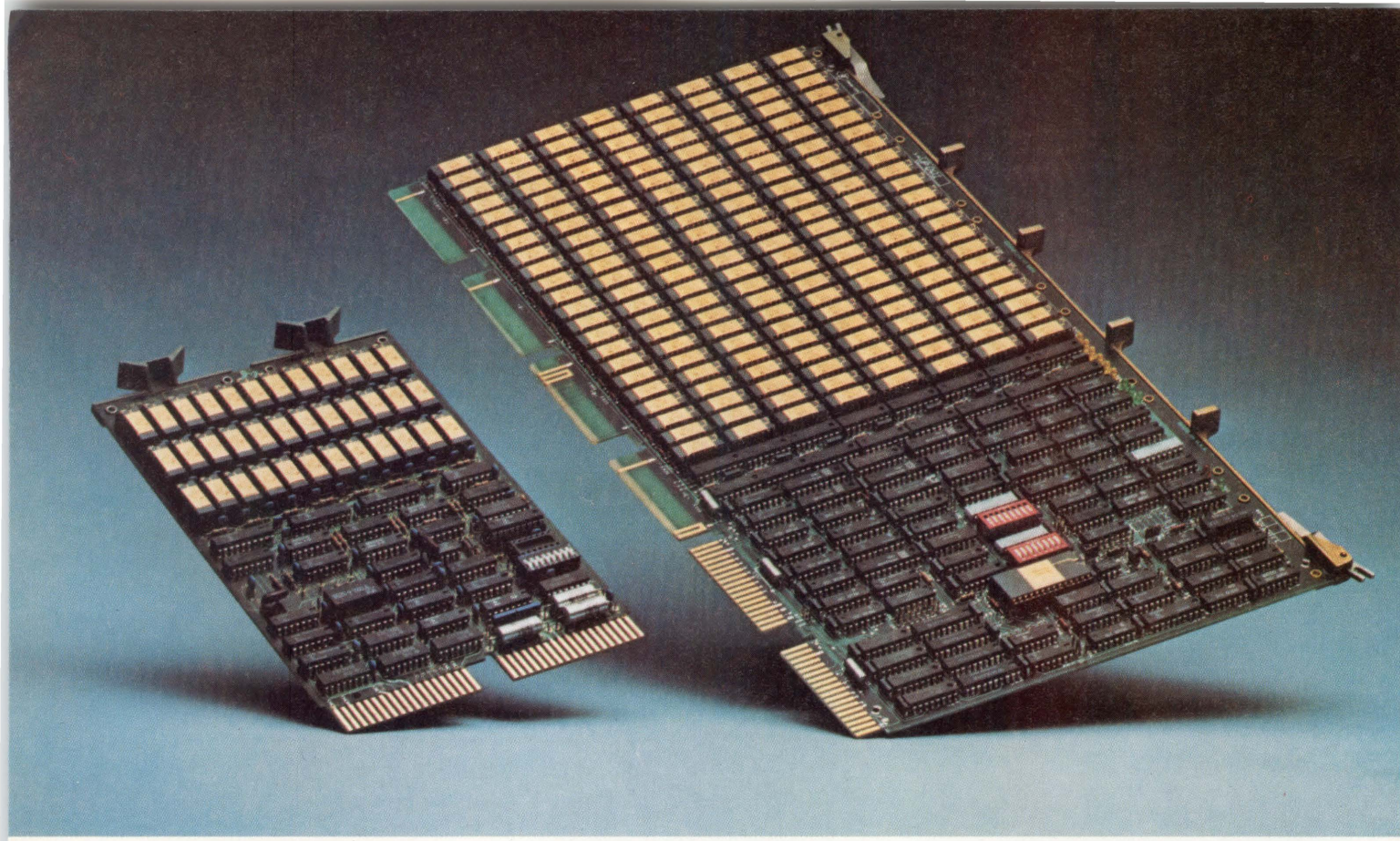
Not to mention a new solid state LED annunciator, with more room for legends.

For details about these and other bright ideas for control panels, and the locations of our sales offices and distributors around the world, write MICRO SWITCH, Freeport, Illinois 61032. Or call 815-235-6600.



MICRO SWITCH
a Honeywell Division

CIRCLE 92 ON INQUIRY CARD



More memory on board and a custom-design capability. Memory systems from Texas Instruments.

Quality. Reliability. Compatibility. And more memory on board than anybody else can offer. These are just a few of the many user benefits inherent in TI's new add-in memory modules.
Here's more:

TMM20000 modules

This high-speed module is fully compatible with the DEC PDP-11 family of UNIBUS† computers. It's the only available module that offers enhanced system reliability through error detection and correction (EDAC) on board.

High-density, 256K x 16 bits organization *plus* 6 bits for EDAC, make TI's new TMM20000 the densest add-in module ever. Operation from a single 5-V supply with low power consumption is another big plus.

Programmable options include modified or extended UNIBUS, I/O page size, control status register address location, and error status register. Twenty-two address lines allow for expansion to 2M words.

TMM10000 modules

Two versions. Both Q-BUS† and Q-BUS PLUS† compatible. Q-BUS for LSI-11/2. Q-BUS PLUS for the newly announced LSI-11/23. The TMM10000-01 with parity. TMM10000-02, without. Both modules use 5-V only technology storage devices for high performance and low power.

These add-in modules, organized 64K x 16 bit words, with an additional 2 bits for parity (01 only) are the densest available on a standard DEC "dual" board.

An optional feature allows extended addressing to 1 megabyte. Fast access and cycle times, too.

Basic storage unit

All TI-designed add-in memory systems employ a state-of-the-art 5-V memory technology. The basic storage unit makes possible such module features as increased board densities, lower power dissipation, improved performance and enhanced system reliability.

These same advantages will be available to users who require production of custom memory systems.

Custom capability

If you need custom memory systems in production quantities, be sure and talk to TI. We'll custom-design modules for specific applications with the same high quality, reliability and meticulous attention to cost-effectiveness that our standard modules offer.

For price and availability information, call your nearest field sales office or authorized TI distributor, or write to Texas Instruments Incorporated, P.O. Box 1443, M/S 6958, Houston, Texas 77001.

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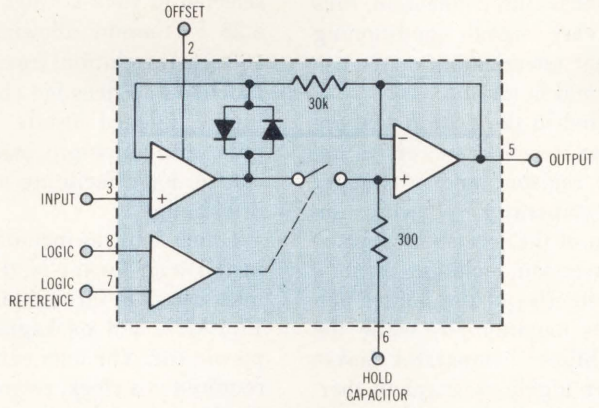
CIRCLE 93 ON INQUIRY CARD



Sample and hold amplifier, NE/SE5537 from Signetics, is implemented on single chip. Op amp at upper left of diagram uses bipolar input transistors; op amp at upper right uses JFET

transistors, which gives the system a low offset voltage. JFET input transistors in the second op amp are used to achieve low leakage current from the hold capacitor. Current mirrors are used, in a proprietary circuit design, to cancel leakage current.

The chip is pin for pin compatible with the LF398 from National Semiconductor Corp, and is said to offer five times better drive capability and one-half the leakage at approximately the same price. Logic inputs are fully differential and compatible with TTL, PMOS, or CMOS.

Most similar ICs drive down to 10 kΩ, whereas this circuit is rated to 2 kΩ. This is an advantage to designers because most ADC circuits are used with input impedances in the 5-kΩ vicinity. In addition to applications in A-D converters, the circuit finds uses in data acquisition systems, measurement circuits, filters, test systems, oscilloscopes, and computers.

Leakage current is 100 pA max, input impedance is 10^{10} Ω, and input offset voltage at 25 °C is typically 1 mV for the SE version and 2 mV for the NE, with corresponding max values at 3 and 7 mV. The unit operates from ±5- to ±18-V supplies with operating ambient temperature range −55 to 125 °C for the SE package and 0 to 70 °C for the NE. Absolute maximum ratings include a ±18-V limit on supply voltage and a 500-mW max power dissipation.

Circle 505 on Inquiry Card

Monolithic 8-Bit Data Acquisition System Offered at Low Cost

Implemented on a single chip in CMOS technology, the DAS-952R, an 8-bit data acquisition system, includes a 16-channel multiplexer, 8-bit successive approximation A-D converter, and microprocessor compatible control logic. This system from Datel-Intersil, 11 Cabot Blvd, Mansfield, MA 02048, is priced at $37.50 in quantities of 1 to 24, and is designed to interface easily with microprocessors for a wide range of control applications.

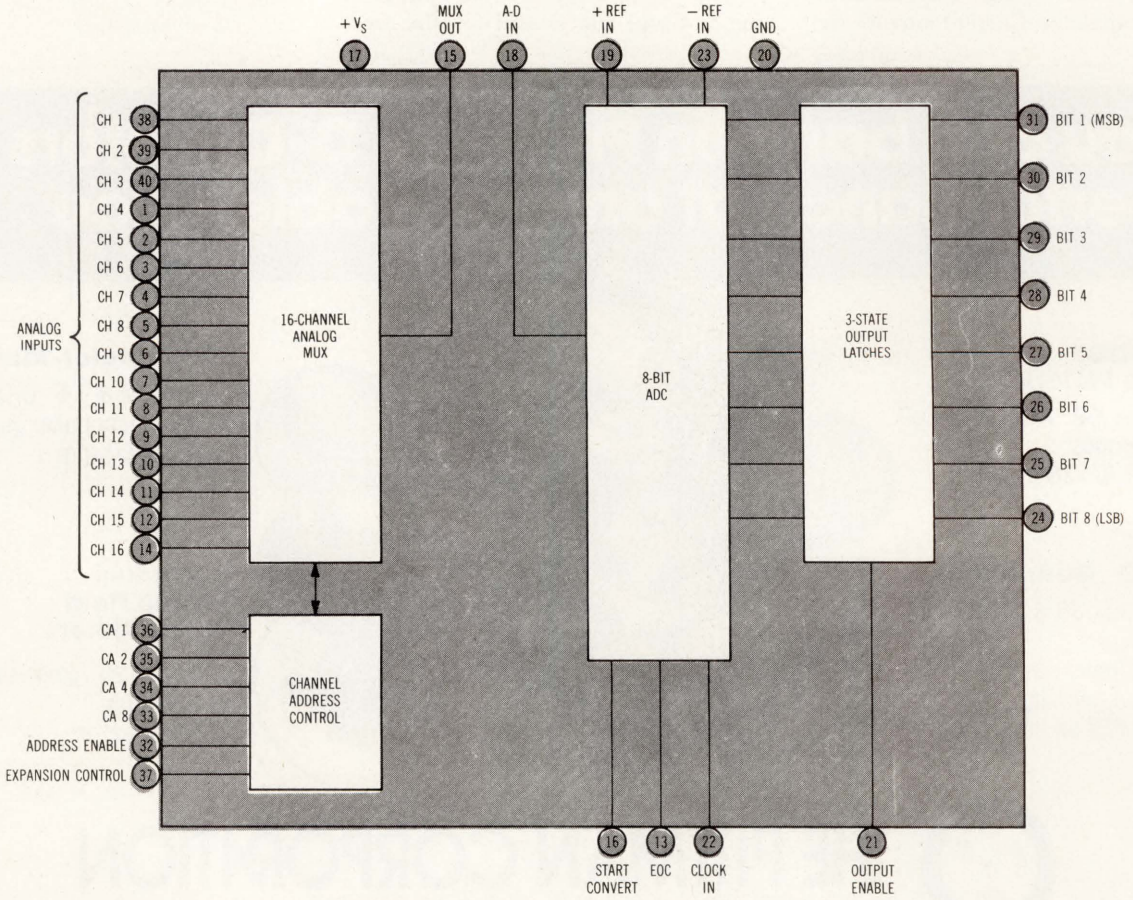
The input multiplexer allows random access to any one of 16 single-ended analog input channels and provides necessary logic for additional channel expansion. Connection of the multiplexer output to the converter input is by external pin connection, thus permitting easy signal conditioning such as sensor linearization or the use of a sample and hold.

Incorporated in the onchip ADC are a 256R ladder network, successive approximation register, and a chopper stabilized comparator, allowing implementation of the successive approximation conversion technique with a switching tree. Use of the ladder network ensures monotonicity while the chopper stabilizer comparator makes the converter highly resistant to thermal effects and long term drift.

Analog to digital conversions are performed on a ratiometric basis, the analog input signal level being digitally expressed as a fraction of the converter's full scale voltage range. Full-scale range for the system is determined by the voltage of the external reference source, which may be selected to yield a range from 0.512 to 5.25 V, thereby allowing selection of LSB size (resolution) from 2 to 20.5 mV. Latched and decoded channel address inputs, latched 3-state TTL data outputs, and microprocessor compatible control logic facilitate microprocessor interfacing.

Other features include a total unadjusted error for the system of $\pm\frac{1}{2}$ LSB max, a system throughput rate of up to 17.5 kHz, and packaging in a 40-pin plastic DIP. The only external circuitry required is a clock, reference, and connection to a power supply (5 V at 1 mA max).

Maximum ratings limit supply voltage V_s to 6.5 V and reference voltage to V_s + 0.1 V. Voltage at



DAS-952R from Datel-Intersil is 8-bit data acquisition system implemented on single chip. Circuit design emphasizes minimum of adjustments, with no full scale or zero adjustment required

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We'll get you going fast. If designing a fixed disk system with back-up is taking too long and costing too much, we can help—today. We'll get you started with Shugart 8 or 14-inch Winchester fixed disk drives, floppy drives for back-up—and a new series of the most versatile and intelligent controllers available. And if you need additional back-up capability, our controllers can handle 1/4-inch streaming tape cartridge drives, too.

The intelligent approach. Our new SA1400 intelligent controllers are so flexible and easy to interface that you can get your fixed disk system on-line in two or three days instead of weeks. SA1400 controllers feature the AMD 2900 series MPU along with ECC, sector interleaving, sector buffering, automatic copying, data separation, and on-board microdiagnostics. For greater flexibility, all SA1400's have the same Host I/O. The SA1400 offers more intelligence than most competitive controllers while relieving the CPU of more drive-related functions for faster data throughput.

The low cost solution. We've solved the cost problem, too. First you get the lowest cost per Megabyte fixed disk drives in the industry. Next, add a realistically priced intelligent controller and either a floppy drive or a 1/4-inch streaming tape drive. Back-up media costs are minimal and you only need a single power supply. And design costs are low because you get started faster. The Shugart solution. An intelligent approach to back-up that combines fast start-up with significant system savings. If this is what you've been waiting for, contact your nearest sales office today.

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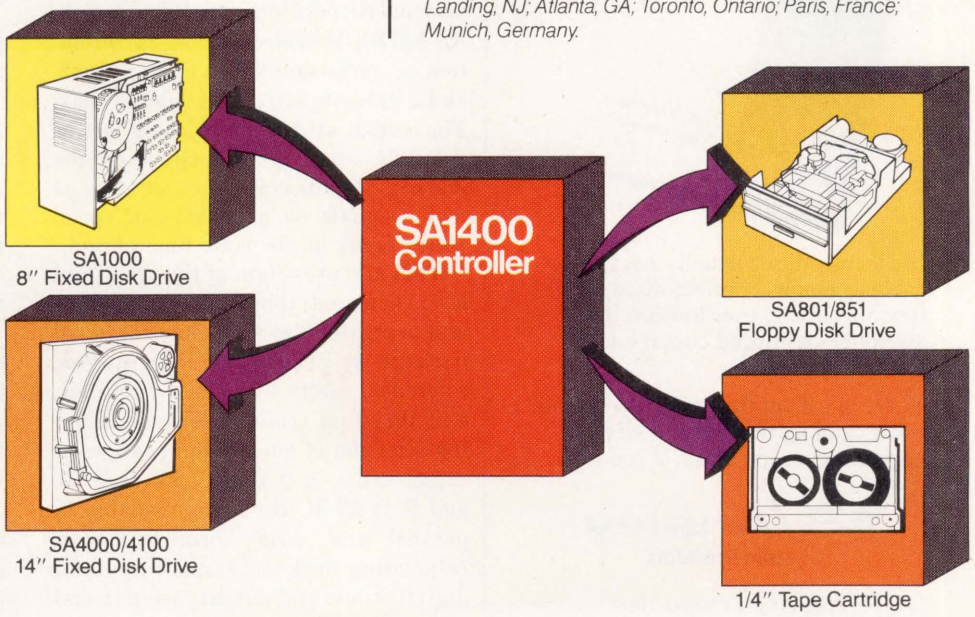

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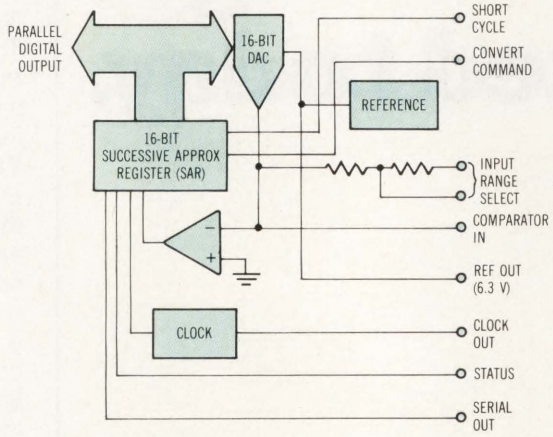
digital inputs must stay between −0.3 and 15 V, while voltage at all other pins is constrained to a range of −0.3 V and V_s + 0.3 V. Allowable temperature ranges are −25 to 85 °C in operation and −65 to 150 °C in storage.

Circle 506 on Inquiry Card

High Speed 16-Bit ADC Offers ±0.003% Linearity



Burr-Brown's 16-bit hybrid A-D converter, ADC71. Models have 13- and 14-bit accuracies

A hybrid, successive approximation, analog to digital converter announced by Burr-Brown Research Corp, International Airport Industrial Pk, Tucson, AZ 85734, provides 16 bits of resolution, a conversion speed of 50 μs max, and a linearity error of ±0.003% max. The ADC71, said to be twice as fast as the only comparable product on the market, permits conversion of twice as many signals or a conversion speed 100% faster in the same time period.

This ADC uses state of the art IC and laser trimmed thin film components and is provided in a 32-pin dual inline package. It is complete with internal reference, short cycling capabilities, and thin film scaling resistors, allowing selection of analog input ranges of ±2.5, ±5.0, ±10.0, 0 to 5.0, 0 to 10, and 0 to 20 V. Data are available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are DTL and TTL compatible.

The thin film resistors that govern accuracy and linearity of the converter are contained on a single chip and automatically laser trimmed before mounting on the product. As a result, final yield is high and price is kept low. The 13-bit accurate model (suffix JG) is priced at $159 in hundreds, the 14-bit accurate model (suffix KG) at $189.

This device's higher resolution is applicable in analytical instruments and clinical analyzers where accuracy rather than speed of measurement is the critical requirement. In automatic testing equipment applications, the available 14-bit accuracy permits testing of 10- and 12-bit parts.

The unit is complete with internal clock, comparator, and reference. It is contained in a proprietary alumina package optimized for thermal properties, the substrate of the 32-pin, triple-wide DIP forming the bottom of the device. Additional characteristics include power supply requirements of 5 and ±15 Vdc, an operating temperature range from 0 to 70 °C, and a package size of 1.76 x 1.16 x 0.23" (44.7 x 29.5 x 5.8 mm).

Circle 507 on Inquiry Card

(continued on page 174)

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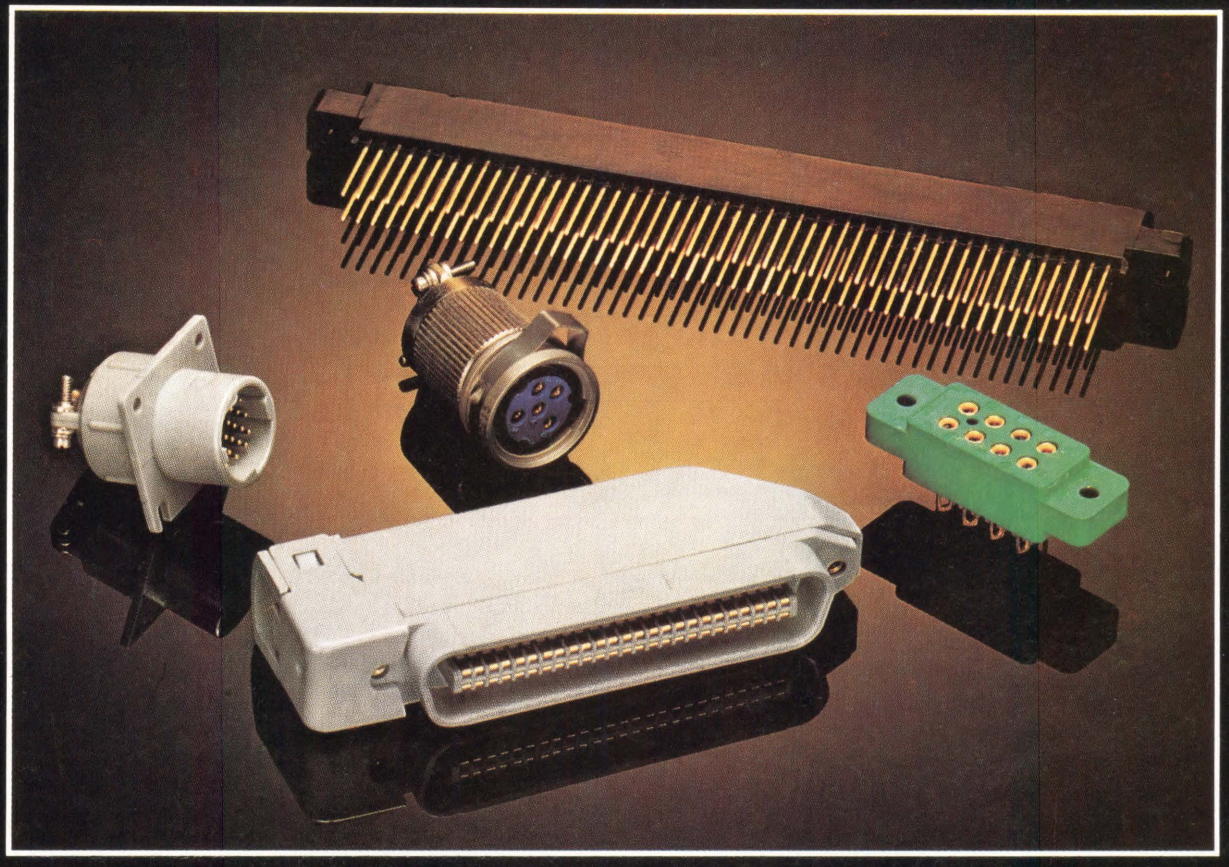

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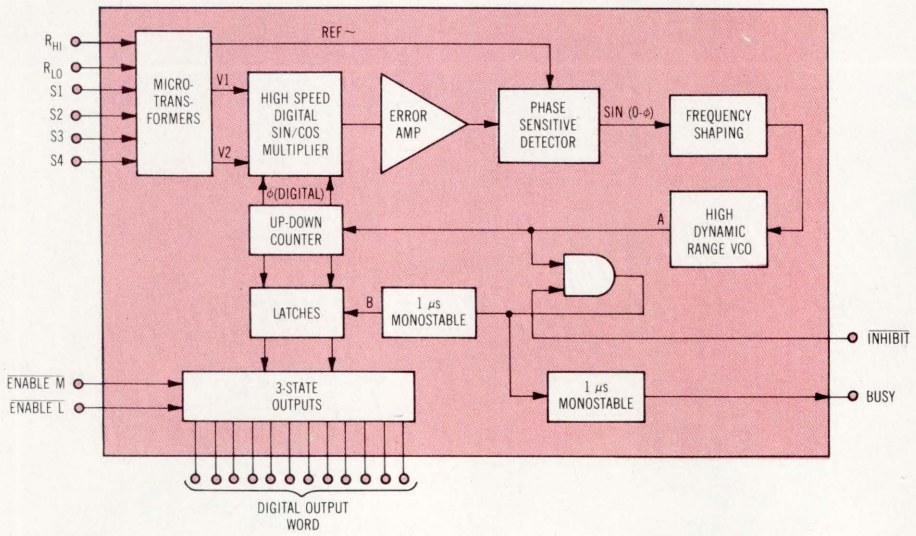
CIRCLE 97 ON INQUIRY CARD

12-Bit Hybrid S-D and R-D Converters Include Transformers



Functional diagram of SDC1741 S-D converter or SDC1742 R-D converter from Analog Devices. Isolation transformers are included in hybrid package

A synchro to digital converter, SDC1741, and a resolver to digital converter, SDC1742, from Analog Devices, Inc, Rt 1 Industrial Pk, Norwood, MA 02062, are said to be the first such devices in the industry to include isolation transformers in a hybrid package. The converters accept all standard synchro and resolver signals and provide a complete, pre-engineered synchro system for servomechanisms, robotics, and other applications where angles, position, or rotation are monitored and/or controlled.

Both 12-bit resolution devices feature 350 Vdc of isolation, continuous tracking (even during data transfer) of at least 18/s, 3-state latches with either parallel or 2-byte outputs controlled by separate $\overline{\text{ENABLE}}$ inputs, and packaging in a small hermetic metal DIP measuring 1.7 x 1.1 x 0.26" (44 x 29 x 6.6 mm). Accuracy is specified at ±10 arc-min ±1 LSB and ±3.2 arc-min ±1 LSB, max, respectively, over the operating temperature range of −55 to 125 °C. Outputs may be enabled at any time without interrupting the internal control loop, with valid data available within 3 μs max.

The isolation transformers, unique to hybrid devices, eliminate traditional user worries about balancing signal lines, noise spikes, and common mode voltages. These features are particularly important in avionic applications. The transformers are cubic in shape with edge length of 0.1" (2.54 mm).

Standard reference frequencies of 400 Hz and 2.6 kHz are available. The 400-Hz models operate with full accuracy over 360 Hz to 1 kHz, while the 2.6-kHz models operate with full accuracy over 2 to 3 kHz. Available reference voltages are 115 V, 26 V, or 11.8 V rms.

All converters receive pre-cap inspection, 24-h stabilization bake at 150 °C, temperature cycling from −65 to 150 °C, acceleration testing at 5000 g, fine leak testing, and operating burn-in at 125 °C for 24 hours. Full processing to MIL-STD-883, Method 5008, Class B is available. Circle 508 on Inquiry Card

Fast Version of Industry Standard 4k RAM Announced

A static 4096-bit random access memory, the MM2147-3, is a high speed version of the 2147. The newly announced memory from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, provides an address access time of 55 ns max. This device is based on a proprietary XMOS™ N-channel silicon gate technology that includes electron beam techniques for mask development and projection aligners in the production stages. Faster versions of the device are expected in the near future.

In its other parameters, the memory is equivalent to the standard product. Organized as 4k x 1, it requires no clocks or refresh, and all data are read out nondestructively, with the same polarity as the input data. In standby operation, current is reduced by 85%. The RAM utilizes a single 5-V supply, provides a tri-state® output for bus interface, and has TTL compatible I/O.

Introducing quality print at matrix speed. For only $1295.*

Until now, you could pay thousands for a slow, letter-quality character printer. Or hundreds for a dot matrix printer, giving up print quality for speed and price.

But that was before Paper Tiger™ 460 offered you a better choice.

The new Paper Tiger 460 is the first matrix printer with high-density dot matrix characters plus high speed. At a low price.

The secret? A unique nine-wire, staggered matrix head provides overlapping dots in both horizontal and vertical planes. The result is dense, high-quality characters you'll be proud to show off.

What's more, Paper Tiger 460 gives you a combination of features simply not available on any other printer, at any price. Like bi-directional, logic-seeking printing at speeds in excess of 150 cps. Microprocessor electronics, with field-installable character sets. Proportional spacing. Automatic text justification. DotPlot™ high resolution graphics option. RS232 and parallel interfaces. And more.

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performance printers ideally su
printer, the IDS 460, offers feat

Automatic proportional spacing
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Paper Tiger 460 Print Sample

But its most important feature is high reliability. The Paper Tiger 460 is designed to be tough and dependable. It has rugged, stepper-motor head and paper drives. A new 300-million-character ballistic-type print head. And its simple, chassis-mounted cartridge ribbon lasts up to four times longer than cassette or spool ribbons.

All this means that Paper Tiger 460 is perfect for word processing, data processing, or electronic mail. It's also perfect for anyone who requires the flexibility of a matrix printer but wants superior quality printing. Without trading off speed or price.

Get your paws on the Paper Tiger 460, and join the tens of thousands of satisfied Integral Data Systems users. Call us toll-free: 800-343-6412. (In Massachusetts, Alaska, and Hawaii, call (617) 237-7610.) Or, write for complete specifications. Integral Data Systems, 14 Tech Circle, Natick, Massachusetts 01760.

Paper Tiger 460

Integral Data Systems, Inc.

*Suggested single-unit, U.S. price. Generous OEM discounts available.

CIRCLE 98 ON INQUIRY CARD

Data Link Controller Offers Wide Variety Of Protocol Features

Designed for use with the S6800 and other 8-bit parallel microprocessors, the S6854 advanced data link controller performs communication link functions for the Advanced Data Communication Control Procedure (ADCCP), High-Level Data Link Control (HDLC), and Synchronous Data Link Control (SDLC) standards. Operating at a 1-MHz clock rate, this device from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, provides data transmission rates as high as 1.5M bits/s. An S68A54 version is also available, with a 1.5-MHz clock rate.

The controller operates as the data communications interface for primary and secondary transmitting stations in standalone, polling, and loop configurations. Among the functions it performs are automatic flag detection and synchronization; "zero" insertion and deletion; extendable address, control, and logical control field generation; variable word length (5-, 6-, 7-, or 8-bit) field provision; and automatic frame sequence generation and checking. It also detects and transmits an abort or idle control bit when the FIFO transmitter register is empty.

All inputs of the ADLC are high impedance and TTL compatible, and outputs are compatible with standard TTL. Interrupt Request (IRQ), however, is an open drain output, having no internal pull-up. I/O ports on the bidirectional data bus allow the data transfer between the chip and the system bus. The data bus drivers are 3-state devices that remain in the high impedance (off) state except when the microprocessor performs an ADLC read operation.

Absolute maximum ratings require that supply and input voltages stay between −0.3 and 7.0 V. Allowable temperature ranges for the 28-pin dual-inline device are 0 to 70 °C in operation and −55 to 150 °C in storage. □

Circle 509 on Inquiry Card

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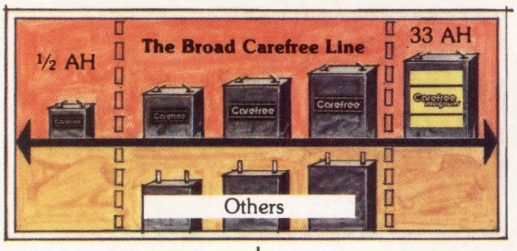
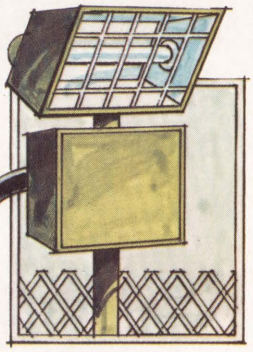
You really do have a broader choice.



When you need maintenance-free rechargeable batteries, you'll find the broadest range of sizes in the Carefree® line—models either *more* powerful or *less* powerful than those available from our competitors.

Our 6 Volt ½ Ampere Hour model—the world's smallest maintenance-free rechargeable—provides the same American-made dependability as our largest Carefree Magnum® models. These Magnum® batteries are noted in the industry for providing up to 20% more power in the same-size cases as conventional models.

More power—or less—than you'll find anywhere else. With about 30 standard sizes in between. Popular models like our 1, 5, and 8 Ampere Hour batteries. Or **unique**, special-purpose units.



All Carefree® rechargeables feature immobilized electrolyte technology. Guaranteed to deliver 100% capacity on first cycle, unlike gels. None of the memory problems of nickel cadmium. That's why Carefree® immobilized electrolyte technology is becoming the standard of the industry. Specify it in your next design.

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Company _____

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City/State/Zip _____

Area Code _____ Phone _____

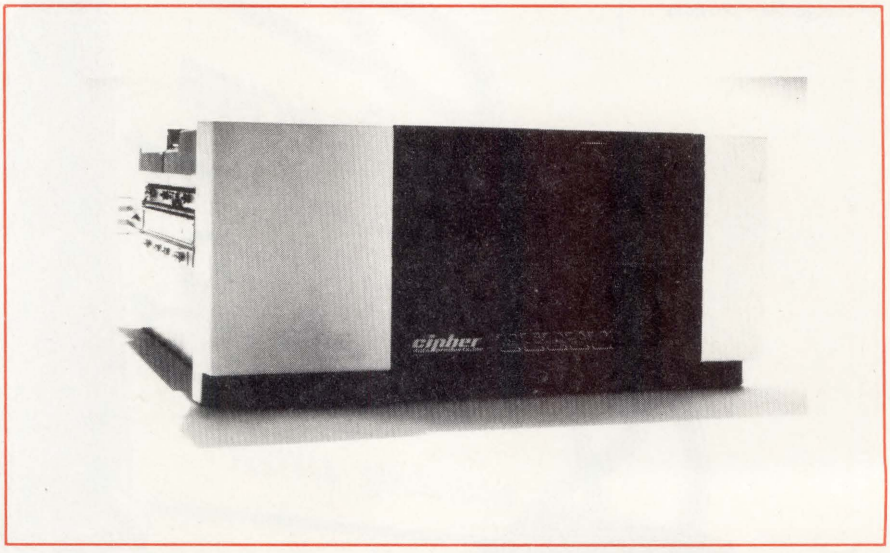
CIRCLE 100 ON INQUIRY CARD

PRODUCT FEATURE

Streaming Tape Drive Offers Doubled Packing Density

By combining a 3200-bit/in (1260/cm) packing density with an operating speed of 50 in (127 cm)/s, the Microstreamer 2 drive doubles the amount of data that can be stored on a standard reel of 0.5″ (1.27-cm) magnetic tape. Up to 92M bytes of unformatted data can be stored on an ordinary 10.5″ (26.7-cm) reel of tape, recorded at a transfer rate of 160k bytes/s.

Operating speeds of 25 and 100 in/s (64 and 254 cm/s), standard on Cipher Data Products' older unit, are retained in this model for operation with the 1600-bit/in (630/cm) ANSI and IBM packing density. The high density model enables an entire 200M-byte Winchester disc to be backed up in less than 25 min, including rewind time, and it can be used, in its 25-in (64-cm)/s operating mode, as a traditional tape drive.



Features and Capabilities

All operating features of the original Microstreamer are provided. The drive will accept 7, 8.5, and 10.5″ (17.8-, 21.6-, and 26.7-cm) reels of tape and uses the phase encoded (PE) recording format. Data are written in nine tracks. Interrecord gaps necessary for the ANSI format are inserted automatically.

Demonstrable hard error rates are better than 1 in 10^{10}. Effectively that is as little as 1 nonrecoverable read error in 200 or more 10.5″ (26.7-cm) reels of tape. Error correction circuitry compensates for the complete loss of one track or for as much as a 10% speed variation. Multiple channel dropout, format, speed, and other system hard errors will be detected and an error signal given.

Data access and repositioning times for the double-capacity tape drive are, respectively, 30 and 120 ms at 25 in (64 cm)/s, 210 and 630 ms at 100 in (254 cm)/s, and 120 and 350 ms at 50 in (127 cm)/s. Choice of recording density is selected from the unit's control panel.

Specifications

Physical dimensions are 8.75″ H x 17″ W x 22″ D (22.2 x 43.2 x 55.9 cm). Weight is 50 lb (22.7 kg). The unit fits a standard EIA rack. Power requirements are 100, 120, 220, or 240 Vac +10 −15%, 48 to 61 Hz, 250 W max. Environmental ranges are 2 to 37.8 °C operating temperature, 15 to 95% noncondensing relative humidity, and 0 to 10,000 ft (3048 m) altitude.

Price and Delivery

In OEM quantities, the Microstreamer 2 is priced at $2350 each. Shipments will begin in December of this year with production quantity shipments during the first calendar quarter of 1981. Cipher Data Products, Inc, 10225 Willow Creek Rd, San Diego, CA 92131. Tel: 714/578-9100.

For additional information circle 199 on inquiry card.

WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60/S4 STANDS ALONE.

Magnavox combines the superior display and control features of the plasma-panel-based Orion-60 terminals with the powerful S4 Micro-Computer System.

The result is a stand alone graphics system that allows you the freedom to develop a wide variety of graphics application and development programs—while maintaining complete control over program storage, program-generated data, library routines and other facilities.

The Orion-60 display terminal offers full graphics with floppy-disc storage, as well as optional rear-projection functions. It lets you create your own displays and enter data by simply touching the screen with your finger. So you can program your own character sets and generate vectors of any length to absolute coordinates. And because the Orion-60 is plasma-based, you'll get bright, high-contrast images free of jitter or distortion.

The S4 Micro-Computer has system software with development capabilities that are as good or better than those found in many larger computer systems.

Features include CP/M* 8080 system utilities, Fortran with 32K RAM, and a full range of graphic utility routines including window, zoom, sub-image movement and rotation. The Orion-60/S4.

For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 South Coliseum Boulevard, Fort Wayne, Indiana 46803, (219) 482-4411.

Magnavox
DISPLAY SYSTEMS

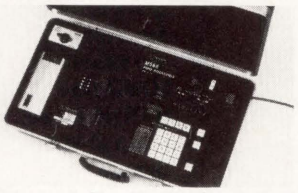
**CP/M is a trademark of Digital Research.*

CIRCLE 102 ON INQUIRY CARD

PRODUCTS

Universal P/ROM Programmer Handles Devices up to 64k x 16 Bits

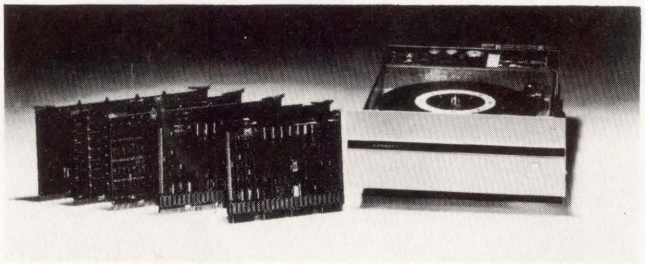
Designed to meet the changing needs of P/ROM technology, the M980 universal P/ROM programmer control unit can blank check or verify a 2716 P/ROM (2k x 8 bit), for example, in 5 s. Human engineered to prevent mistakes, the unit uses a combination of audio prompter and lights to lead the operator through the programming process, flagging errors, and signaling program end. The battery backed built-in RAM buffer retains stored data up to 7 days without external power. Quality performance is assured by self-testing of keyboard, display, and buffer memory, as well as UL listing and error coding. No calibration is required.



All of the company's generic, dedicated, and gang personality modules are accepted. Using these plug-in modules, more than 450 different devices can be programmed. Operators can program from the keyboard, directly from another device, or from peripheral equipment via buffer memory. Built-in software and expanded 8-digit hexadecimal display will accommodate devices up to 64k x 16 bits. Operations include checksum, blank check, duplicate, verify, read, and program. Manufacturing mode permits single-button P/ROM duplicating. Among the buffer editing features are fill buffer, invert buffer, nibble swap, insert, and delete. Weighing less than 22 lb (9.9 kg) with personality module installed, the unit is housed in an attache carrying case. Std programmer is available with 4k x 8-bit CMOS RAM buffer; it is also available with 8k x 8-bit or 16k x 8-bit RAM buffer. Keyboard selectable interfaces include RS-232-C, paper tape reader, parallel I/O, and TTY. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

Circle 202 on Inquiry Card

Plug Compatible Winchester Drives Reduce Cost of Mass Memory for PDP-11

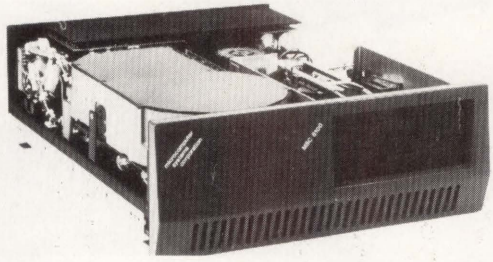


Microprocessor controlled Winchester disc systems supply 10.4M- or 32.2M-bytes formatted, mass memory for DEC's PDP-11 minicomputers and LSI microcomputers at about 40% the cost of similar capacity DEC drives. System consists of microprocessor based controller/interface, cables, and either model 5300-14 or -42 Winchester drive. KSC11 and KSC01 controllers emulate DEC disc controllers and operate with PDP-11/04 to -11/60 minicomputers and LSI-11, -11/2, and -11/23 microcomputers, respectively. They are software transparent to RT-11, RSTS-E, and RSX-11M operating systems and are plug compatible with Unibus or Q-bus. Only two card positions in the mainframe are required.

KSC11 controllers support up to 4 drives for a total of 128.8M bytes; KSC01 controllers handle 2 drives giving up to 64.4M bytes. Onboard slide switches select base and vector addresses. Systems provide DMA transfers with a full 128k-word bus address range. A 2048-byte high speed RAM provides a 3-sector buffer, permitting contiguous sector reads, eliminating sector interface schemes and allowing operation at a low bus priority without affecting data transfer rate performance. Both controllers perform a 16-bit cyclic redundancy check on header information and a 32-bit error detection and correction code on the field. Onboard firmware provides automatic self test and operator assisted diagnostics supported by error display LEDs. Discs have a recording density of 6000 bits/in (2362/cm) and track density of 300 tracks/in (118/cm). There are 700 data tracks/surface; head flying height is 19 to 21 μin (0.48 to 0.53 μm); and data transfer rate is 8 MHz. Single track positioning time is 10 ms with avg positioning time of 45 ms. **Kennedy Co,** 1600 S Shamrock Ave, Monrovia, CA 91016.

Circle 200 on Inquiry Card

Hard Disc Mass Storage Combined with Floppy Disc Backup in Single System

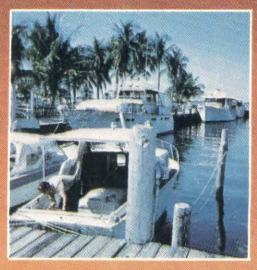


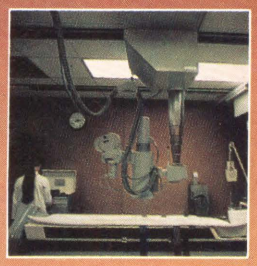
Disc storage system combines hard disc mass storage with flexible disc backup to provide an economical means of expanding the online storage capacity of most small computers, while retaining the media transportability of floppy discs. MSC-8100 is a self-contained data storage system that incorporates intelligent controller/formatter with a universal IEEE-488 bus protocol for easy integration into host systems, a high density Winchester technology drive using 8″ (20-cm) fixed discs for capacities to 19.1M bytes, and a backup flexible disc drive with capacity for 1.6M bytes/disc.

The 7″ (17.8-cm) high system mounts in a std 19″ (48-cm) rack. Use of a single controller and a single power supply reduces the size and cost and increases system reliability. Single, high level intelligent bus interface simplifies system design and integration. The system's integrated controller adapts to virtually any minicomputer or microcomputer system.

The MSC-8100 (IEEE-488) and -8110 (LSI-11) can accommodate up to three 8″ (20-cm) sealed Winchester type platters with a total capacity of 19.1M bytes unformatted, or formatted to 15M bytes. The other drive accepts double-sided, double-density flexible diskettes with a capacity of 1.6M bytes formatted, or 1.2M bytes in IBM format. The hard disc drive's avg access time is less than 30 ms. All disc formatting, control, and management functions are provided by the integrated controller. A bipolar LSI design, the controller provides operating and maintainability features that include a full sector data buffer, error detection and correction, error recovery including automatic retry, automatic position verification, automatic seek to alternate track, parallel or serial interrupt, relative sector addressing, programmable sector interleaving, and implied seeks. **Microcomputer Systems Corp,** 432 Lakeside Dr, Sunnyvale, CA 94086.

Circle 201 on Inquiry Card





Protect expensive electronic circuitry.

Now you can protect your circuit with the switch that turns it on.

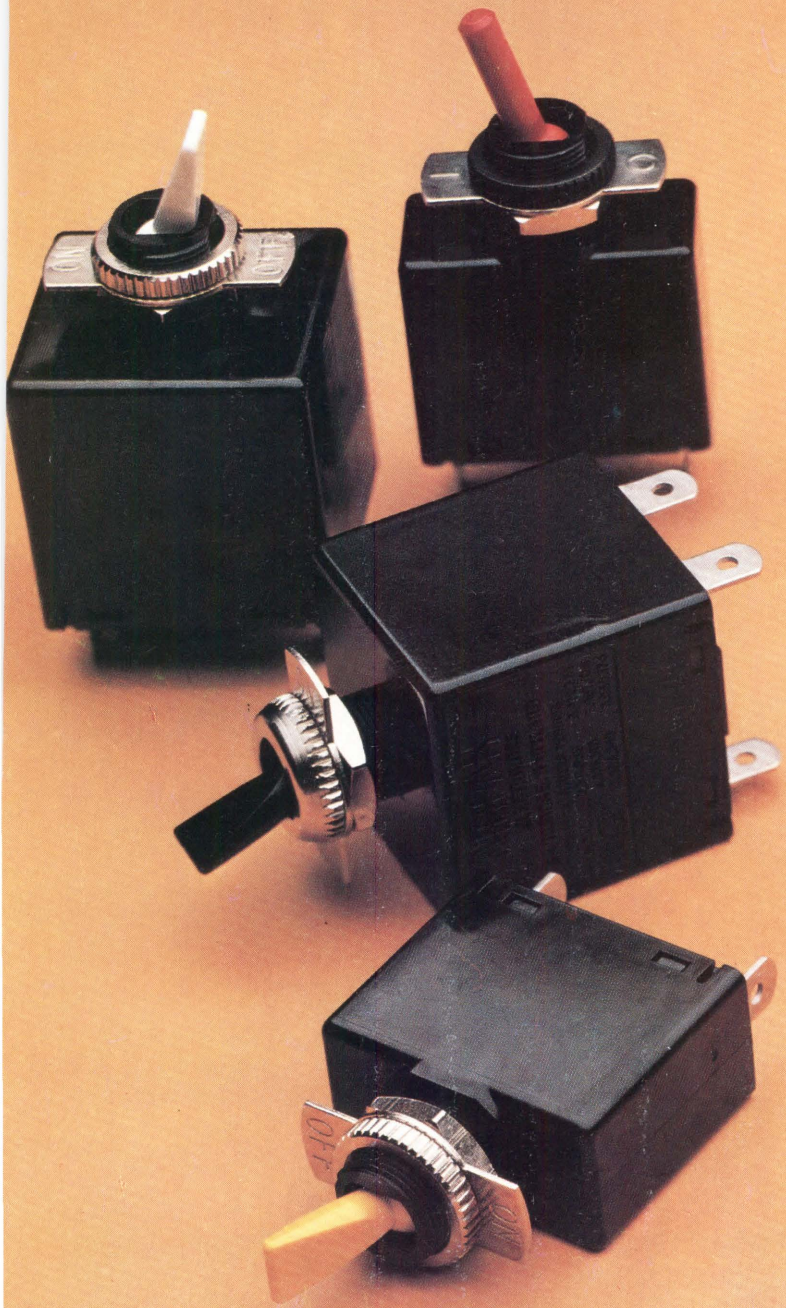
The new AIRPAX SNAPAK® circuit breakers look and operate like switches, but their performance doesn't stop there. They are also snap-acting magnetic circuit breakers that can protect your product and its components from damaging power surges and faults.

For products that never had circuit protection before, the SNAPAK breakers are a great idea—they feature easy, single-hole mounting, they're available in a wide range of delay characteristics and current ratings, plus they come in a choice of baton or paddle handles in six attractive colors.

For products that previously used fuses and thermal devices, they're a better alternative—they eliminate extra stocking and assembly of multiple components, they save space and they reduce product wiring requirements.

You can order SNAPAK circuit breakers in SPST and DPST configurations (they're the only snap-action DPST circuit breakers around). There are shunt and relay versions available. And you can choose from a complete selection of mounting hardware to match your product's panel aesthetics.

All the facts about AIRPAX SNAPAK circuit breakers are contained in our new brochure. To get your free copy, contact us at: AIRPAX, Cambridge Division, Woods Road, Cambridge, MD 21613. Telephone: (301) 228-4600. Or circle our reader service number.



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CIRCLE NUMBER 103 FOR IMMEDIATE NEED
CIRCLE NUMBER 104 FOR REFERENCE ONLY

For years, manufacturers of computers, processors and other electronic equipment have improvised all too freely when running interconnecting cables *outside* cabinets. The results have been cumbersome, unattractive, often costly and sometimes hazardous.

Brand-Rex, long a leading supplier of Tape Cable® for internal use, now has the answer for external applications. A line of UL-listed jacketed Tape Cable. With shielding or without, it's made to fit a full range of temperatures and voltages up to 105°C and 600 volts. Now, interconnections can be efficient, economical, hazard-free, often even invisible.

Get complete information about Brand-Rex jacketed or shielded-and-jacketed flat cable. Write to Brand-Rex Company, Electronic and Industrial Cable Division, Willimantic, CT 06226. Or call 203/423-7771.

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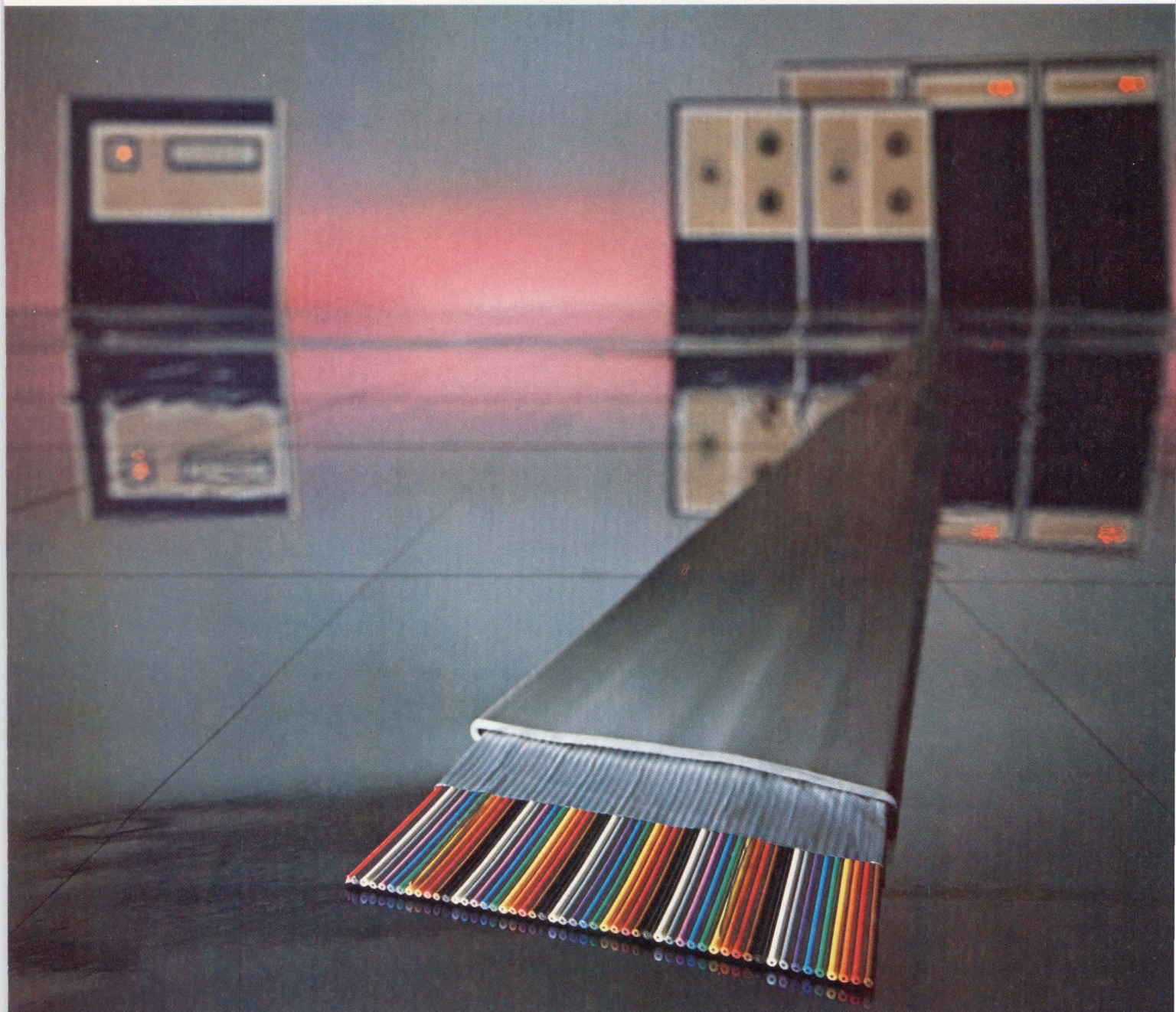
THE SAFEST CONNECTION BETWEEN TWO POINTS IS NOW A FLAT LINE.

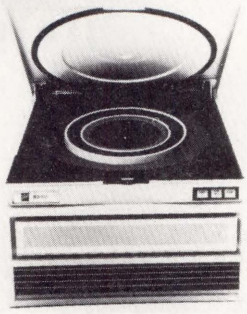


STATE-OF-THE-ART-SOLUTIONS

CIRCLE 105 ON INQUIRY CARD

PRODUCTS

160M-BYTE RACK MOUNTABLE DISC DRIVE



A self-contained random access mass storage unit storing 160M bytes on a removable disc pack, BD-160 has 5 read/write surfaces, each carrying 1645 tracks, and capacity for a total of 164.2 x 10^6 bytes. Each track carries 20,160 bytes or 161,280 bits (including header and gaps). Track density is 768 tracks/in (302/cm). Recording method is MFM, bit serial. A closed loop head positioner servo system receives positioning information from tracks prerecorded on one dedicated disc surface. Max access times avg 30 ms; between two adjacent tracks, 5 ms; and across max tracks (0 to 1645), 55 ms. Latency time is 16.7 ms. Data transfer rate is 9.68 x 10^6 bits/s at std rotational speed of 3600 r/min. Start and stop times are 20 s. **Ball Computer Products,** 860 E Arques Ave, Sunnyvale, CA 94086.

Circle 203 on Inquiry Card

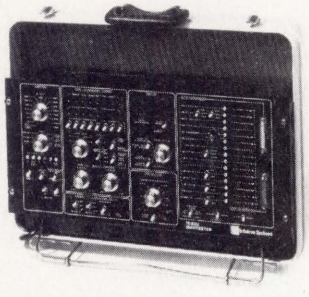
64 x 64-PIXEL IMAGE DIGITIZER

Type 611 allows a host computer access to 64 x 64 pixel gray scale view of virtually any visual scene. TTL compatible interface and low power requirements permit direct connection to I/O structure of most mini and microcomputers without additional controllers. Standard C-mount enables customizing of optical characteristics. Silicon sensor has a response curve with peak sensitivity in the near-IR region which allows IR illumination for applications where visible lighting is undesirable. Host computer controls all digitizer functions. Variations of integration time (exposure) permit electronic adjustment of sensitivity by host. Fast (f/1.6) lens focuses from 0.2 m to infinity. **Periphicon,** PO Box 324, Beaverton, OR 97005.

Circle 204 on Inquiry Card

MODEM/MULTIPLEXER TESTER

Portable TE620 Infotester test set speeds fault isolation and measures performance in any data communications network. It will verify proper operation of synchronous and asynchronous modems and time division, frequency division, and statistical multiplexers. Using various test modes, it precisely measures, counts, and clearly displays bit, char, and block error rates, distortion and overspeed variations, request to send/clear to send turnaround times, and other performance parameters. The RS-232 compatible unit generates test data at switch selectable speeds from 50 to 19,200 bits/s in a choice of 6 formats. Char may be transmitted one at a time, in a continuous stream, or in bursts. **Infotron Systems Corp,** Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003.



Circle 205 on Inquiry Card

More guts. Better value. From NCR for OEMs.

New High Value 0226 Thermal Printer
We've packed over 10 years of thermal printer experience into this new, quiet, lightweight 80 column unit. The result is a machine with advanced design features and solid NCR reliability, that *actually costs less* than competitive models. Compare us with other printers. You'll find we're a better value.

Unique 5x8 Dot Matrix — gives you a true lower case, easier reading.

Low Print Head Replacement Costs — save almost half the price of most.

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You can buy "mechanism only" — or get complete RO or KSR cabinet units.

For delivery information, prices, or literature, please contact us at NCR Engineering and Manufacturing, OEM Marketing, P.O. Box 627, Ithaca, New York 14850, (607) 273-6066.

NCR

CIRCLE 108 ON INQUIRY CARD

PRODUCTS

DISC CONTROLLER FOR COMBINED FLOPPY/WINCHESTER SYSTEMS

SA1400 incorporates functional intelligence onboard to relieve host computers of many std disc control functions. Onboard data separator logic is capable of controlling up to 4 disc drives and works with any combination of SA1000 8″ (20-cm) or SA4000 14″ (36-cm) Winchester and SA800/850 8″ floppy disc drives. In the case of 8″ drives, this arrangement eases retrofit of existing floppy based systems with Winchester discs and simplifies the combined Winchester with floppy backup concept. Based on a high performance bit-slice microprocessor, the controller uses advanced firmware design concepts to provide onboard controller functions and optimize CPU operation. Functions include automatic copy, sector interleaving, error correction code, and microdiagnostics. **Shugart Associates,** 435 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 206 on Inquiry Card

BISYNC REMOTE CONTROLLER FOR PRINTER/PLOTTER

Emulating IBM 3780 data communications terminals, model 440-20 provides remote electrostatic plotting and printing with any of the company's printer/plotters. Using Versaplot™ software on the host computer, input data is processed and compressed, then transmitted over data communication lines in compressed raster format to the controller. The controller decompresses raster data and controls plotting or printing. An exclusive plot compression algorithm reduces data communications time by as much as 30 to 1 over the ordered vector compression technique. The controller carries its own data link trace facilities and self-test diagnostics. Synchronous serial RS-232-C data is input at rates from 2400 through 19.2k bits/s. **Versatec, a Xerox Co,** 2805 Bowers Ave, Santa Clara, CA 95051.

Circle 207 on Inquiry Card

DISC CONTROLLERS

Lotus 700 is an economical high performance SCM/CMD compatible moving head disc storage interface designed for use with the company's minicomputers. A single-board design using low power Schottky and MSI logic, it has provisions for all necessary connections. Interfacing up to 4 disc storage modules at transfer rates to 1.209M bytes/s, it supports mixtures of drives. Model 701 provides 10M-byte interface capabilities. Using only 1 card slot and totally transparent to the IRIS operating system, it can control up to 4 10M-byte drives and accommodates either multisurface single-platter, or cartridge type single- or multiplatter drives at 1500 or 2400 r/min. Features include automatic seek as part of read/write, overlapped seek operation, complete data error checking, and choice of formats. **Point 4 Data Corp,** 2659 McCabe Way, Irvine, CA 92714.

Circle 208 on Inquiry Card

In OEM modem cards UDS technology deals a full deck

Universal Data Systems' justly deserved reputation in OEM modem cards has been built on one fact — technical superiority lets us deal from a full deck. We've proved our leadership by delivering well over 200,000 OEM modems!

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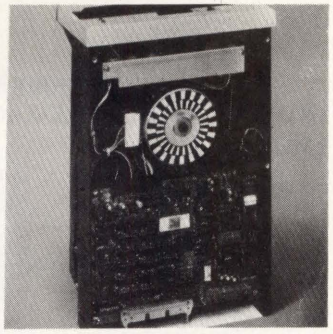
CIRCLE 111 ON INQUIRY CARD

Created by Dayner/Hall, Inc., Winter Park, Florida

PRODUCTS

FLOPPY DISC DRIVES



FDD-403A and -403B use LSI architecture and a simplified spindle drive mechanism featuring a direct drive dc motor to achieve MTBF of >80,000 h. A VFO circuit in the A version permits separation of MFM or FM data; the same function is done externally in the B version. Up to 3 B models can be connected to and controlled by an A unit through daisy chain interface lines. Both drives offer storage capacity of 985k bytes in an IBM 26-sector format. With recording density of 6816 bits/in (2683/cm) and data transfer rate of 500k bits/s, units accept MFM recording methods. Using IBM Diskette II or equivalent they record on 154 tracks, offer track to track access times of 3 ms, settling times of 35 ms, and head loading times of 50 ms. **Hitachi America, Ltd,** 100 California St, San Francisco, CA 94111.

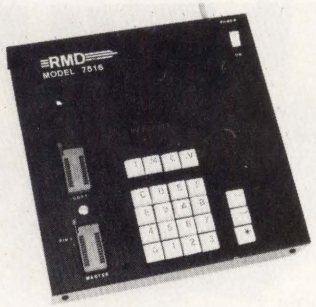
Circle 209 on Inquiry Card

POWERFUL MIDRANGE MINICOMPUTER

Large system features of the PDP-11/34 include max memory of 1M bytes, integral 8k-byte cache memory, microprocessor controlled programmer's console, and provision for optional floating point and commercial instruction set processors. The general purpose minicomputer is available in std system configurations or as separate CPU. CPU features include a min 256k bytes of ECC MOS semiconductor memory, 2 serial line units, microprocessor controlled ASCII interface, 8k-byte cache memory, and power supply. System configurations comprise the CPU, dual TU58 DECtape II drives, DECwriter III terminal, and choice of mass storage devices. Operating systems include RSX-11M, RSX-11M-PLUS, and version 7 of RSTS/E multiuser, multitasking operating system. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 210 on Inquiry Card

EPROM PROGRAMMER

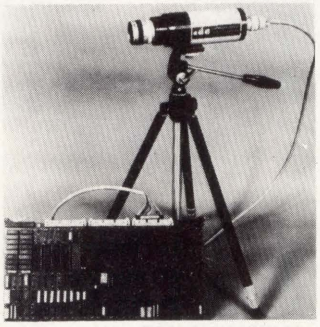


Model 7516 programs industry std 2716 and TMS 2508 EPROMs (1k- and 2k-byte, single-voltage type). It is suitable for users who require additional programming facilities but wish to avoid the cost of multiple universal P/ROM programmers. Standard features of the unit are separate protected master and copy sockets, RS-232-C serial interface with keyboard selectable baud rate, 2k-byte editing RAM with microprocessor control, and data entry and command keyboard with an 8-char alphanumeric display. Editing features allow user to read, correct, and verify data before committing them to P/ROM. Data can be merged from multiple P/ROMs, compared, and checksum computed. **RMD, Inc,** PO Box 206, Bristol, PA 19007.

Circle 211 on Inquiry Card

COMPUTERIZED VIDEO DATA ACQUISITION SYSTEM

Designed as a complete solid state video system for PDP-11s in process control, instrumentation, and engineering applications, basic MIP-3/V contains a high speed microcomputer controlled input processor board, 16k-word dual-port memory board, and 128/128 x 8-bit/pixel solid state camera, equipped with a 25-mm f/1.4 lens and 25-ft (7.6-m) cable. System inputs up to 30 frames/s, enabling user to acquire data continuously or perform real-time processing, such as integration. Basic system buffers up to 2 complete frames and is expandable to 8 frames of data. Dual-port memory enables PDP-11 Unibus to be optimized for controlling other system peripherals. Video system operates on 5 V at 6 A drawn from the PDP-11. **Computer Design & Applications, Inc,** 377 Elliot St, Newton, MA 02164.



Circle 212 on Inquiry Card

WINCHESTER DISC DRIVE WITH INTEGRAL CARTRIDGE BACKUP

DFR-900 series drives incorporate 3330-11 technology for the removable cartridge media and Winchester technology for the fixed module to give the user high performance with proven backup capability. Winchester and cartridge drives share a common integral power supply, microprocessor control logic, air filters, and controls—all housed in a single unit that mounts in std 19″ (48-cm) rack. Both cartridge and fixed media are served by independent head positioners that provide 16M bytes of removable storage plus 16M, 48M, or 80M bytes of fixed capacity. Fixed storage module can be removed in field and replaced with higher capacity module to meet increased storage requirements. **Ampex Corp, Memory Products Div,** 200 N Nash Rd, El Segundo, CA 90245.

Circle 213 on Inquiry Card

COMPUSTAR™

INTERTEC'S NEW $2500 MULTI-USER SMALL BUSINESS COMPUTER

At last, there's a multi-user microcomputer system designed and built the way it should be. The CompuStar™. Our new, low-cost "shared-disk" multi-user system with mainframe performance.

Unlike any other system, our new CompuStar offers what we believe to be the most practical approach to almost any multi-user application. Data entry. Distributed processing. Small business. Scientific. Whatever! And never before has such powerful performance been available at such modest cost. Here's how we did it . . .

The system architecture of the CompuStar is based on four types of video display terminals, each of which can be connected into an auxiliary hard disk storage system. Up to 255 terminals can be connected into a single network! Each terminal (called a Video Processing Unit) contains its own microprocessor and 64K of dynamic RAM. The result? Lightning fast program execution! Even when all users are on-line performing different tasks! A special "multiplexor" in the CompuStar Disk Storage System ties all external users together to "share" the system's disk resources. So, no single user ever need wait on another. An exciting concept . . . with some awesome application possibilities!

CompuStar™ user stations can be configured in almost as many ways as you can imagine. The wide variety of terminals offered gives you the flexibility and versatility you've always wanted (but never had) in a multi-user system. The CompuStar Model 10 is a programmable, intelligent terminal with 64K of RAM. It's a real workhorse if your requirement is a data entry or inquiry/response application. And if your terminal needs are more sophisticated, select either the CompuStar Model 20, 30 or 40. Each can be used as either a standalone workstation or tied into a multi-user network. The Model 20 incorporates all of the features of the Model 10 with the addition of two, double-density mini-floppies built right in. And it boasts over 350,000 bytes of local, off-line user storage. The Model 30 also features a dual drive system but offers over 700,000 bytes of disk storage. And, the Model 40 boasts nearly 1½ million bytes of dual disk storage. But no matter which model you select, you'll enjoy unparalleled versatility in configuring your multi-user network.

Add as many terminals as you like - at prices starting at less than $2500. Now that's truly incredible!

No matter what your application, the CompuStar can handle it! Three disk storage options are available. A tabletop 10 megabyte 8" winchester-type drive complete with power supply and our special controller and multiplexor costs just $3995. Or, if your disk storage needs are more demanding, select either a 32 or 96 megabyte Control Data CMD drive with a 16 megabyte removable, top loading cartridge. Plus, there's no fuss in getting a CompuStar system up and running. Just plug in a Video Processing Unit and you're ready to go . . . with up to 254 more terminals in the network by simply connecting them together in a "daisy-chain" fashion. CompuStar's special parallel interface allows for system cable lengths of up to one mile . . . with data transfer rates of 1.6 million BPS!

Software costs are low, too. CompuStar's disk operating system is the industry standard CP/M*. With an impressive array of application software already available and several communication packages offered, the CompuStar can tackle even your most difficult programming tasks.

Compare for yourself. Of all the microcomputer-based multi-user systems available today, we know of only one which offers exactly what you need and should expect. Exceptional value and upward growth capability. The CompuStar™. A true price and performance leader!

INTERTEC DATA SYSTEMS®

2300 Broad River Rd. Columbia, SC 29210
(803) 798-9100 TWX: 810-666-2115

*Registered trademark of Digital Research, Inc.

CIRCLE 115 ON INQUIRY CARD

PRODUCTS

HIGH CAPACITY 0.25″ CARTRIDGE TAPE SYSTEM

GPIB (IEEE-488) 0.25″ (0.64-cm) cartridge mag tape system 4000A has a formatted data capacity of more than 24M bytes and 20k-byte/s avg data throughput. Recording is on DC300 type data cartridges with either 300 or 450 ft (91.4 or 137.2 cm) of mag tape. Recording is compatible with current and proposed ANSI stds. System has integral 4k-byte data buffer, optionally expandable to 16k bytes, controlled by a dedicated Z80A microprocessor. **Dylon Corp,** 3670 Ruffin Rd, San Diego, CA 92123.

Circle 217 on Inquiry Card

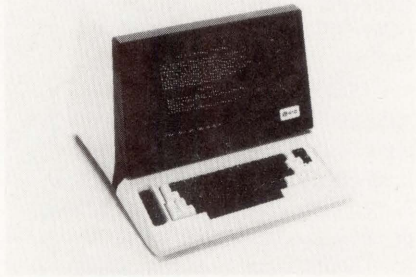
LOW PROFILE INTELLIGENT DISKETTE SYSTEM

A slim line system that provides up to 3.2M bytes of data in a 5.25″ (12.7-cm) high space, the 48 Subsystem incorporates RFS 4810 master drive with an onboard microprocessor based controller/formatter, min electronics RFS 4820 slave drive controlled by electronics of the 4810, dc power supply, and enclosure. Dual-head drive provides 1.6M bytes of unformatted data/drive in double-density encoding. Formats include IBM compatible 26-, 15-, or 8-sector/track, expanded capacity, or double-density 46-sector/track. **Ex-Cell-O Corp, Remex Div,** 1733 Alton St, Irvine, CA 92713.

Circle 218 on Inquiry Card.

CRT TERMINAL

Featuring complete editing and char highlighting capabilities, the VC410 CRT terminal is compatible with Teletype Corp CRT terminals. Included are split screen, with windows for host response, and terminal status display. The terminal provides a 1920-char display, buffered line edit mode, char/line insert and delete, and direct X-Y cursor addressing. **Volker-Craig, Ltd,** 266 Marsland Dr, Waterloo, Ontario N2J 3Z1, Canada.



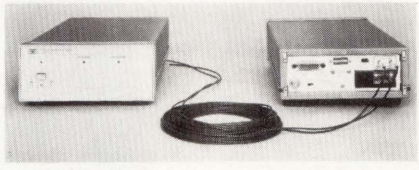
Circle 219 on Inquiry Card.

LINE PRINTER CONTROLLER

Controller DLP-3300 for Series/1 minicomputer emulates the IBM 4973 attachment. It operates in any single I/O slot of the Series/1 or 4959 I/O expansion unit and is compatible with IBM's RPS, EDX, and CPX OS. It features self test and selectable addressing to any of the 128 address locations supported by IBM software. The 9 x 7″ (23 x 17.8-cm) single-board unit is designed with bipolar MSI and LSI logic. Data transfer rate is 1.6M bytes/s, with cycle time of 170 ns. Power requirement is 5 V at 3.0 A. **Datasystems Corp,** 8716 Production Ave, San Diego, CA 92121.

Circle 220 on Inquiry Card

INTERFACE BUS EXTENDER



HP-IB extender HP 37203A serializes HP-IB information and transmits it over coax cable or fiber optic link to a remote (up to 1-km) extender unit that reconverts serial data to parallel HP-IB format. Transfer rate is up to 50k bytes/s. Extenders are transparent to HP-IB operation and support full range of procedures including pass control and a form of parallel control. Single-error correction/detection algorithm identifies and corrects transmission errors. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 221 on Inquiry Card

Of course our Floppys aren't cheap.

Quality never is.

It's no use trying to hide the fact: Maxell Floppy Disks give you the finest quality you can buy no matter how much you spend. And more and more of you are agreeing that your data is worth our perfection.

Our floppys work better with your drive.

Naturally, our floppys conform to ISO and IBM specifications. More important, they have also been approved by major OEMs, the people who recommend only those few floppys they are certain will work best with their hardware. So although we obviously don't know which drive system you are using, it makes no difference. Maxell Floppy Disks are so good they actually work better with *any* drive.

What it all means for you.

Yes, you can pay less for some other floppys. But lost data is a terrible price to pay when quality is what you want. And Maxell Floppy Disks help you profit in the very parameters you use this medium for: storing more data with virtually no down-time.

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So when you have to depend on full data retrieval, a few cents can make a big difference. Depend on Maxell Floppy Disks. They can really save you.

Maxell offers the full range of Floppy Disks from standard 8-inch to 5¼-inch plus Data Cassettes. *Dealer inquiries invited.*

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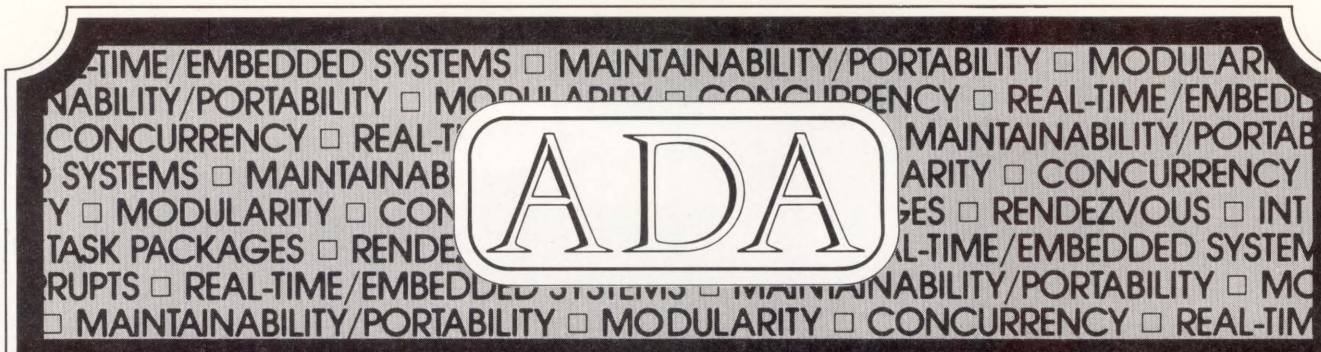

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Course 335 • a four-day course

Programming in ADA

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Course Benefits

This course provides a comprehensive introduction to the ADA language, its structure, features and support environment. Topics covered include:

- **ADA Language Features: Data Typing, Procedures, Packages, Tasks, Exception Handling**
- **ADA Modules, Information Hiding and Compilation Units**
- **Concurrent Processing Using ADA's Multi-Tasking Capabilities**
- **Real-Time Interrupt Handling and External I/O Interfaces**
- **Portability and the ADA Program Support Environment**
- **Structured Programming and Structured Design Using ADA**
- **Host/Target Considerations for Embedded Systems**

ADA is a modern programming language which has been developed over the last several years at the initiative of the U.S. Department of Defense, in cooperation with the U.K., French and German Defense Ministries and with extensive contributions from industry and universities worldwide. The language is specifically aimed at improving software reliability, portability and maintainability while significantly reducing system life cycle costs. ADA is designed for implementations ranging from large, complex systems to embedded, real-time applications. **ADA is expected to become the dominant language of the 1980's and 90's.**

WHO SHOULD ATTEND:

This course is designed for programmers, systems analysts, software engineers, program and project managers who will need to use the ADA programming language. The course will be equally useful for those involved with aerospace and defense industry software systems — due to language standardization — and for all personnel involved in the planning, design and implementation of advanced industrial/scientific software products.

COURSE FEE: $795.00

Course fee includes **Complete Course Materials**, luncheons and coffee breaks.

Course Author

MR. DAVID T. MOORE

Mr. Moore is a member of the ADA Implementation Group, and has been an active participant in the ADA Test and Evaluation Phase. His responsibilities at Systems Consultants include the management of software conversion projects and the development of ADA implementations. Mr. Moore has designed and implemented real-time systems on hardware ranging from large main-frames to 8080/6800 microprocessors, employing languages ranging from FORTRAN and PASCAL to PL/M and assembly language. His current activities include the design of embedded, multi-microprocessor configurations using the ADA language.

About the Course Sponsor

ICS specializes in technical education. Over the last six years, we have implemented practical, cost-effective training programs for large corporate and government clients throughout North America and Europe. Our clients include **ESTEC, General Electric, Hughes Aircraft Co., IBM, JPL, L. M. Ericsson, MBB, NASA, NUSC, Philips, RDAC, U.S. Army** and many others.

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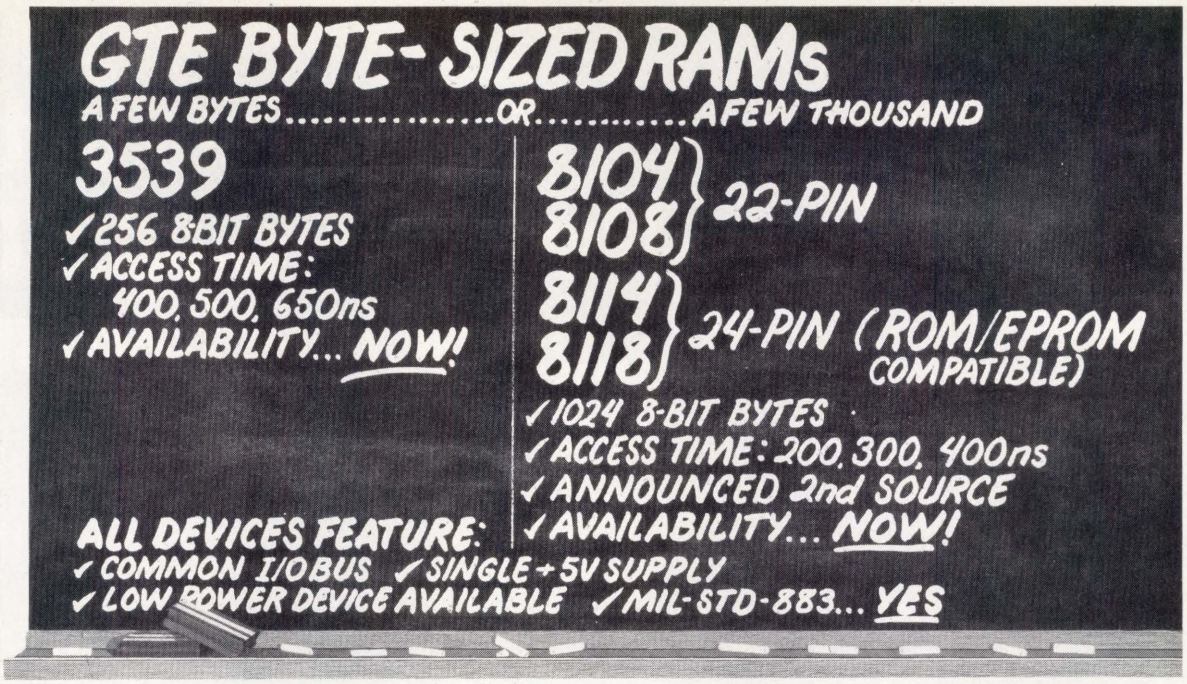
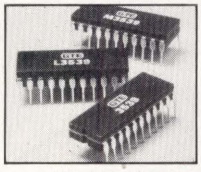
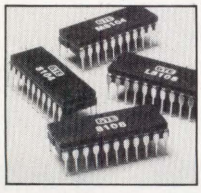


GTE Has Byte-Sized Memory to Match Your Needs



A Few Bytes...

If your system needs just a few bytes of memory, take a good hard look at our 3539. For small memory designs, it's ideal. It's organized as 256 8-bit bytes ...a 2048 bit Static RAM packaged in a standard 22-pin DIP. You have a choice of access times... and what's more, it's available in a low power configuration, or you can select a military version that meets MIL-STD-883 requirements. The time-proven, highly reliable 3539 is a natural upgrade for small memory applications using 2111's and 2112's...and you'll like the byte oriented I/O structure.



or a Few Thousand

On the other hand, if you need a larger memory, consider our 8K family. GTE offers the most complete line of 8K Static RAMs in the industry. They all provide 1024 8-bit bytes, with a common I/O bus for ease of design. You have a choice of access times as low as 200 nanoseconds. For those special applications, our low power units may be the answer... or perhaps an 8K military device that meets MIL-STD-883 requirements... and, all are immediately available.

GTE 8K Static RAMs offer the design engineer many advantages... including higher performance, lower system cost, significant power savings... and the convenience of an 8-bit bus I/O structure. And furthermore, GTE's 8K's are the only Static RAMs with an announced second source.

So... if you need a few bytes, or a few thousand, GTE Microcircuits is the company with the *experience*, the *history*, and the *product variety* to match your memory needs.

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CIRCLE 119 ON INQUIRY CARD

Check 'em out! New Burroughs OEM print mechanisms and heads.

You'll find every feature you've been looking for: speed, performance, price and reliability.

That's right. For the first time ever, Burroughs offers to OEM's our line of dependable, low-cost, dot matrix print heads and printer mechanisms. The print head options include 90, 120 or 180 cps operation with 7 or 9 pin configuration. Print mechanisms available with 132 print positions and print speeds to 90 cps.

Add Burroughs dependability to your product. For the name of your nearest OEM representative, write or call **Burroughs OEM Marketing,** Burroughs Place, Detroit, MI 48232, (313) 972-8031. In Europe, Langwood House, High Street, Rickmansworth, Hertfordshire, England. Telephone: 09237-70545.

Burroughs

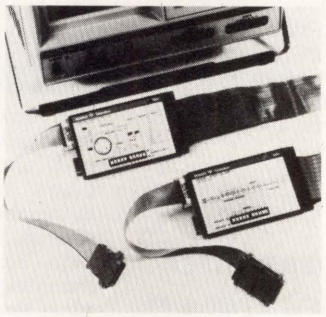
Circle 120 for General Information

Circle 121 for Detailed Specifications

PRODUCTS

LOGIC ANALYZER ACCESSORY PODS

Enabling users of K100-D logic analyzer to see all primary digital signals associated with serial data communications channels, the K100-D/RS-232 serial data analyzer consists of basic analyzer and accessory pod—a communications channel monitoring subsystem contained in a pod with cables that attach to RS-232 or CCITT V.24 communications port and to 8 optional signal sources. Built around 2 UARTs, it can analyze a full-duplex transmit/receive channel. For IEEE-488 GPIB users, the K100-D/488 GPIB analyzer adapter provides digital analysis facilities, including the flexibility to correlate data flows with other complex functions in the system or device under test. Switches on the pod allow capture of signals on 3 handshake lines and 5 bus management lines or selection of any 8 TTL level signals. **Gould Inc, Biomation Div,** 4800 Old Ironsides Dr, Santa Clara, CA 95050.



Circle 214 on Inquiry Card

DIGITIZING TABLET WITH HANDPRINT RECOGNITION CAPABILITY

Recognizing handprinted input, accepting drawings or sketches, and producing automatic solutions from handprinted mathematical problems, unit will also accept input through Teletype compatible touch table, series of calculations through a calculator touch table, or coded entry to computer programs or security systems through a user selectable touch table key area. Shaped like a desk blotter and only 4 mm thick, digitizing tablet accepts std business size paper placed horizontally or vertically. With a special pen, shapes and char may be drawn, digitized, and stored in an online or offline computer. Char entered through the tablet are converted to ASCII code for transmission to host via RS-232-C/V.24 interface at rates to 9600 baud. **Image Data Products, Ltd,** 1-4 Portland Sq, Bristol BS2 8RR, England.

Circle 215 on Inquiry Card

VARIABLE TRACTOR FEED TELEPRINTER

Tabletop model 43 BSR (buffered send/receive) features tractor feed capable of handling business forms ranging from 3 to 12″ (7.6 to 30.5 cm) in width and up to 22″ (55.8 cm) long. In addition to horizontal/vertical tabulation and top of form, controls are provided for horizontal and vertical alignment of data on preprinted forms. The unit is equipped with 16k of buffer for sending, receiving, and editing. Data can be prepared offline, edited for accuracy, and then sent at speeds up to 180 char/s. Features also include simultaneous online send/receive capability with offline data preparation, automatic answer (unattended operation), and a menu of 30 keyboard selectable options. **Teletype Corp,** 5555 Touhy Ave, Skokie, IL 60077.

Circle 216 on Inquiry Card

PRODUCTS

VT100 COMPATIBLE CRT TERMINAL

VIT 100 is plug compatible to the DEC VT100[R] and other 132-col CRTs. Std display format is 24 lines x 80 or 132 col. Detachable typewriter style keyboard has numeric/function keypad. 12″ (30.5-cm) diag CRT screen displays selectable single- and double-width/height char size and reverse char. Split screen, fixed and settable tabs, and dual-speed scroll are also std. Terminal uses EIA std interface and an RS-232 serial printer port. **C. Itoh Electronics, Inc,** 5301 Beethoven St, Los Angeles, CA 90066.
Circle 223 on Inquiry Card

LOW PROFILE FLOPPY DISC DRIVE

Doubling storage capacity of word processors and small computers by allowing 2 drives to be installed in the space of 1, disc drives are 2.125″ (5.39 cm) high. Other dimensions are 12.5″ (31.8 cm) long and 8.5″ (21.6 cm) wide. Model 82 provides dual heads for reading/writing on both sides of the disc; model 81 has one head for single-side operation. Storage capacity is 800k bytes for the single-head model and 1600k bytes for the dual. **Micro Peripherals, Inc,** 9754 Deering Ave, Chatsworth, CA 91311.
Circle 224 on Inquiry Card

MULTICOLOR PRINTER/PLOTTER

COLORPLOT 100[TM] produces high quality color plotting and printing at line printer speeds. A proprietary 3-zone ribbon and impact dot matrix printing technology are used to produce multicolor print on std computer paper at an avg cost of $0.25/copy. No operator assistance is required to make copies up to 13.2″ (33.5-cm) wide and any length. Resolution is 100 dots/in (39/cm), plotting both horizontally and vertically. Precision dot placement anywhere on the form provides contiguous plots. **Trilog, Inc,** 17391 Murphy Ave, Irvine, CA 92714.
Circle 225 on Inquiry Card

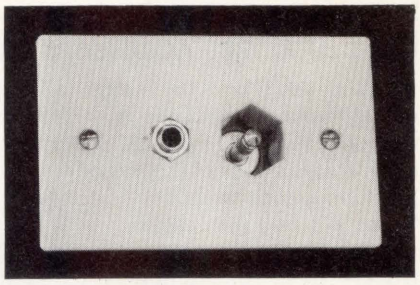
1200-BIT/s MODEM

Full-duplex operation at 1200 bits/s is provided over dial-up and 2-wire lines, asynchronous or synchronous, with the MT212D modem. Available in both stand-alone and rackmount configurations, the unit provides originating and automatic answering capability. Voice-to-data transferring is accomplished on the chassis; no special RTC exclusion key phones and adapters are needed. **Multi-Tech Systems, Inc,** 82 Second Ave SE, New Brighton, MN 55112.
Circle 226 on Inquiry Card

SINGLE-BOARD BUBBLE MEMORY SYSTEMS

Including controller and all electronics, RMS family includes 4 modules with 32k- through 256k-byte capacity systems. Interfacing with AIM 65 microcomputer, System 65 development system, and Motorola Exorciser[TM] and Micro-module[TM] series allows immediate evaluation of bubble memory. Each 6 x 9.75″ (15.2 x 24.76-cm) module uses a 100-kHz field rate and is electrically compatible with the 6500 and 6800 bus. **Bubble Memory Products, Electronic Devices Div, Rockwell International,** PO Box 3669, Anaheim, CA 92803.
Circle 227 on Inquiry Card

TERMINAL PLUG-IN BOX FOR 3600 SYSTEMS



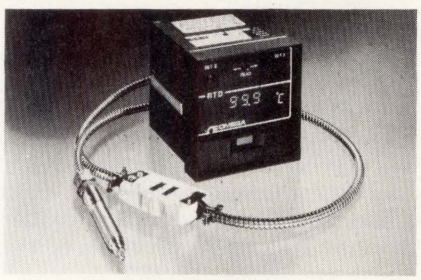
Port Box provides a secure hardwired receptacle for IBM 3600 System connection, and replaces subloop jacks and plugs. Data communication loop is automatically reinstated when an individual terminal is removed. Molded in high density polystyrene, the unit's mounting holes match those of std electrical terminal boxes. Contact surfaces are nickel, with 1.27-μm hard gold plating. **Datatec Products, Inc,** 45 Smith St, Englewood, NJ 07631.
Circle 228 on Inquiry Card

EXPANDED CAPABILITY OPERATING SYSTEM

Release 2.0 of GCOS 6 MOD 400 operating system includes advanced COBOL and FORTRAN compilers, distributed data entry at up to 24 terminals, and menu driven display formatting and control. Also included is a transaction control language which permits concurrent transactional executions by multiple users. Designed for use with the company's Level 6 computers, a programmable Facility 3271 permits IBM host interaction. **Honeywell Information Systems,** 200 Smith St, Waltham, MA 02154.
Circle 229 on Inquiry Card

DIGITAL CONTROLLERS

Series 4200 RTD digital controllers utilize a linearizing technique to provide accuracies up to 10 times greater than other 1% meter controllers. 3-wire lead compensation permits sensors to be up to 1000 ft (304.8 m) from the controller. Available in both 1.0 and 0.1° options, with single or dual setpoints, std features include proportional bands, manual reset, and LED readout. **Omega Engineering, Inc,** 1 Omega Dr, Stamford, CT 06907.



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BRAIN CELLS.

They're Gates Energy Cells. And they're limited only by your imagination.

Our cells offer hundreds of recharges, greater than 8 years life in float applications, and have superior storage life.

That's why dozens of manufacturers have chosen Gates Energy Cells to power their products safely and reliably.

Our Cells are now available in our basic 2V sizes, ranging from 2.5 to 25Ah, for dozens of battery configurations.

Learn more about the cells imaginative engineers are using to make great products even better.

Write: Gates Energy Products, Inc., 1050 South Broadway, P.O. Box 5887, Denver, CO 80217. Phone (303) 744-4806.

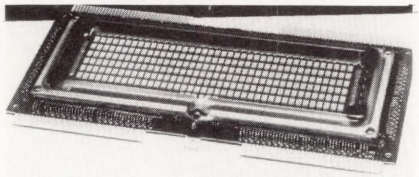
GATES ENERGY

Circle our number on the reader service card.

CIRCLE 125 ON INQUIRY CARD

PRODUCTS

240-CHAR FLUORESCENT DISPLAY PANELS



DC40066A displays 240 alphanumeric char in six of 40-char lines. Completely prewired to card edge connectors for plug-in installation, the display uses a combination of thick/thin film substrate (anode) fabrication and conventional processing. Each char consists of 35 bright fluorescent emission dots, in a 5 x 7 dot arrangement. A cursor is positioned under each char. Char measure 3.5 mm wide and 5.0 mm high. **Noritake Electronics, Inc,** 22410 Hawthorne Blvd, Torrance, CA 90505.

Circle 231 on Inquiry Card

DATA COMMUNICATIONS SURGE PROTECTOR

COMGUARD[R] provides virtually unconditional overvoltage protection to remote terminal or minicomputer and the associated modem. It wraps around all cable inputs entering the data station. Normal data signals and 110/220-V power supply can pass through the unit, but any combination of steady state or transient overvoltages are limited to a safe level. Switching transients and other emi are attenuated by 40 dB. A patented circuit stops high energy electromagnetic pulses or 20k-A direct lightning hit. **Kapusi Laboratories,** 2121 S El Camino Real, San Mateo, CA 94403.

Circle 232 on Inquiry Card

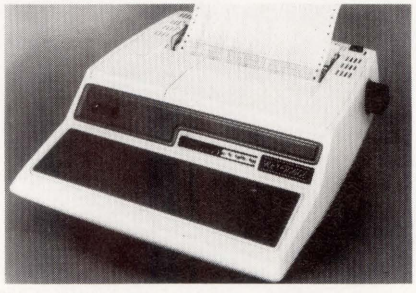
BRIDGE RECTIFIERS WITH INTEGRALLY MOLDED HEAT SINKS

Measuring 1.125 x 1.125 x 0.4″ (2.86 x 2.86 x 1.01 cm), the bridge rectifier products provide a thermal resistance, junctions to case, of 1 °C/W, due to the integrally molded heat sinks. Ratings for the epoxy cased units are FPI40 series—40 A, 1 kV PRV; MPI40—40 A, 400 A surge; MPI50—50 A, 800 V PRV; UPI50—50 A, 1000 V surge, at up to 600 V PRV. **Electronic Devices, Inc,** 21 Gray Oaks Ave, Yonkers, NY 10710.

Circle 233 on Inquiry Card

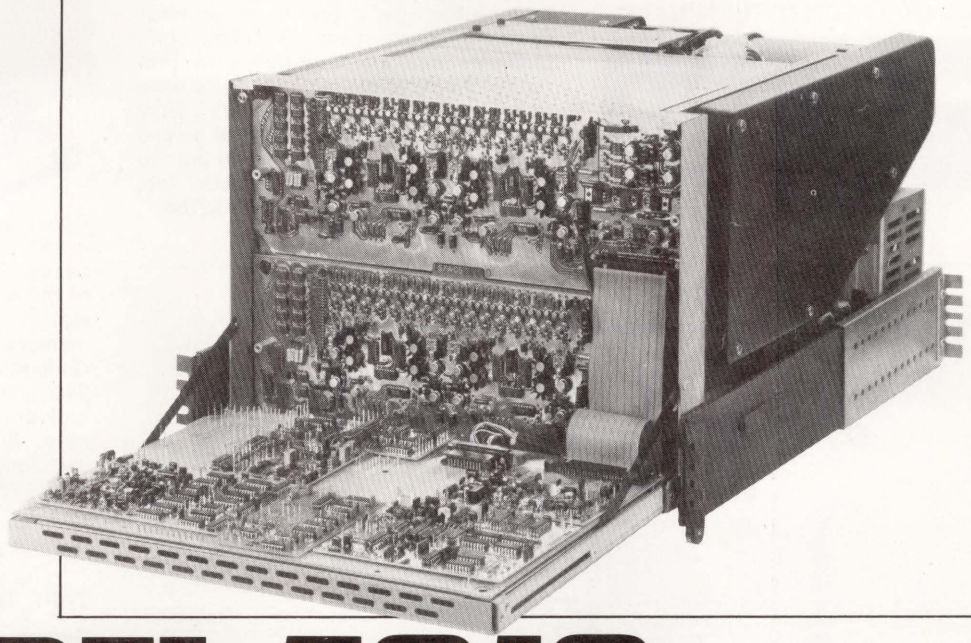
96-COLUMN RO PRINTER

Bidirectional printing is featured in the Century Z80 based printer. Utilizing the Burroughs PM 100 series printer mechanism, the device is fully logic seeking and includes RS-232, V.24 20-mA current loop, and Centronics compatible interfaces. 96-char ASCII set with descenders at speeds of up to 9600 baud, 132-char line, and a 3k-char FIFO buffer are std. **Weyfringe, Ltd,** Longbeck Rd, Marske, Redcar, Cleveland TS11 6HQ, England.



Circle 234 on Inquiry Card

RELIABILITY: 28,000 hr. MTBF.
ECONOMY: .035 cents per bit.



VRC MODEL 4016 MEMORY

CAPACITY . . .	37.9 million bits
BIT RATE	4.33 MHz
ACCESS TIME	8.5 m/sec.
DIMENSIONS	Height – 12¼" (31.2 cm.)
	Width – 17½" (44.5 cm.)
	Depth – 22" (55.9 cm.)
MEAN TIME TO REPAIR . .	Less than 1 hr.

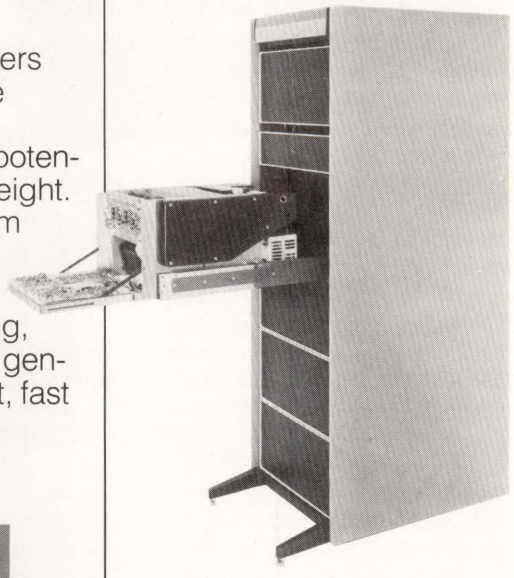
When it comes to speed, reliability and low cost, systems users in 25 countries in every continent of the world depend on the VRC 4016 head-per-track memory.

It features a fail-safe actuation system that eliminates the potential of media damage and data loss. It's compact and lightweight. All electronics, drive components and head retraction system are mounted outside the drum, making service simple and eliminating risk of contamination.

Applications are endless. Telecom and message switching, process control of all kinds, geophysical exploration, power generation, news editing, typesetting. Wherever low cost-per-bit, fast access and high data storage capacity are required.

For proven reliability, worldwide support, field service and predictable high quality, you can rely on VRC.

Write or call for complete details on the Model 4016 head-per-track memory...a simple, rugged, compact unit to improve the reliability of your system.



Vermont Research
CORPORATION

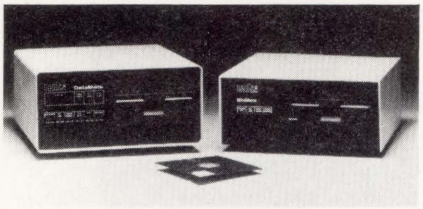
Precision Park
North Springfield, Vermont 05150
Tel. (802) 886-2256, TWX: 710-363-6533
FAX (802) 886-2682

Vermont Research, Ltd.
Cleeve Rd.
Leatherhead, Surrey, England
Tel. Leatherhead 76221
Telex: 23280
FAX Leatherhead 76834

CIRCLE 127 ON INQUIRY CARD

PRODUCTS

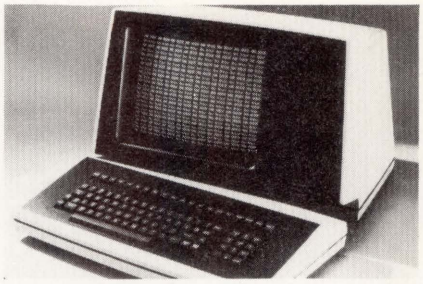
RS-232 MINI-FLOPPY TERMINALS



Store and edit DataMate II and MiniMate II terminals provide 163k storage capacity. Units store up to 1280 addressable records of 128 char; 328k capacity is optional. DataMate adds editing capability to nonintelligent terminals without special program discs; MiniMate complements intelligent terminals by providing char edit mode. Both units have store and forward capabilities. They communicate in batch or line at a time mode at switch selectable rates from 110 to 9600 baud. **Western Telematic, Inc,** 2435 S Anne St, Santa Ana, CA 92704.

Circle 235 on Inquiry Card

ANSI COMPATIBLE CRT TERMINAL



Designed to provide maximum flexibility in an off-the-shelf product, the Ambassador CRT terminal implements most of the ANSI X3.64, 1979 std. Display format is selectable, 18 to 60 lines, and memory capability is 60 lines of 80 char. Consisting of a 15″ (38-cm) display and 94-key detached keyboard, the system includes 12 programmable function keys. **Ann Arbor Terminals, Inc,** 6175 Jackson Rd, Ann Arbor, MI 48103.

Circle 236 on Inquiry Card

TAPE TRANSPORT FORMATTERS

Generation of inter-record gaps, positioning of heads within gaps, and control of data density on TDX series tape transports is provided by model TF-800, -160, and -816 formatters. For use with dual-gap heads for read checking while writing at 75″ (190 cm)/s, the units are constructed on single PCBs and have provision for mounting on the host drive. Up to 8 daisy-chained drives may be controlled. **TDX Peripherals, Div of GAW Control Corp,** 150 New York Ave, Halesite, NY 11743.

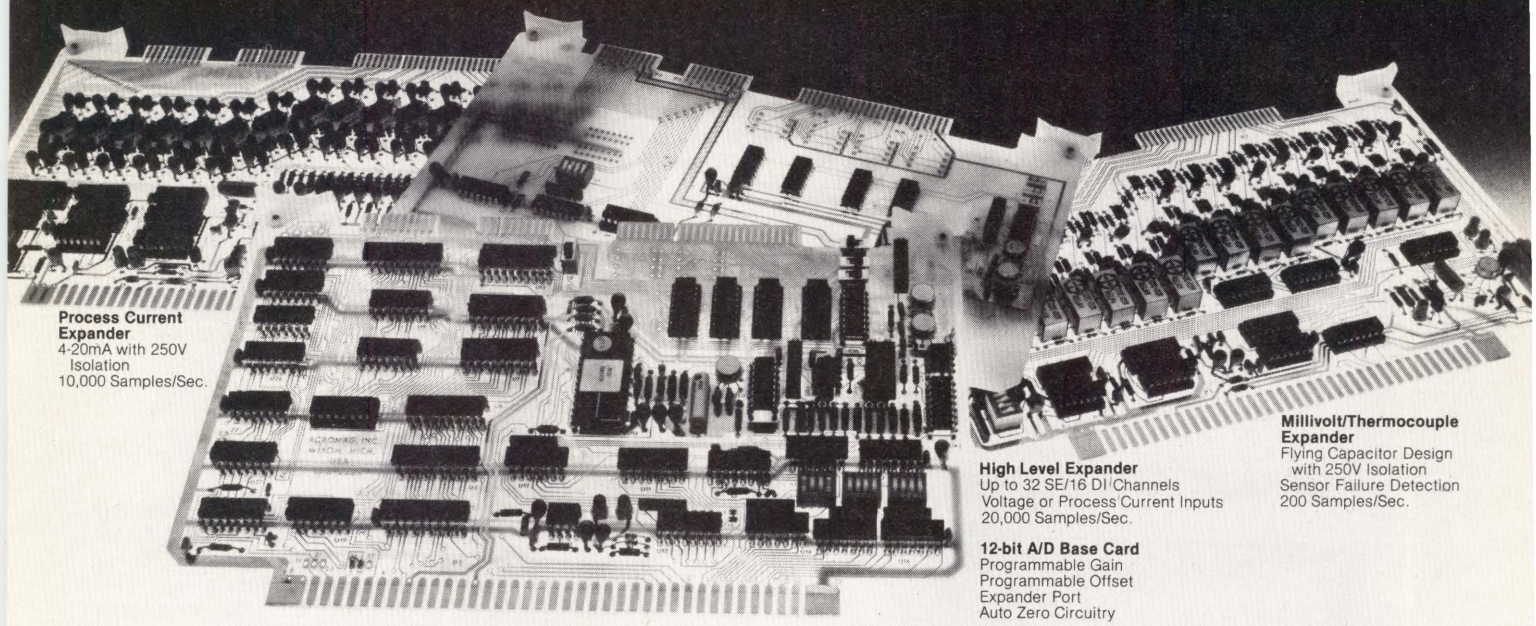
Circle 237 on Inquiry Card

STATISTICAL MULTIPLEXER FOR MULTIPOINT NETWORKS

Microprocessor controlled SNP-1100 features a multipoint capability that allows users to poll a number of remote sites along a single transmission line. The unit will double throughput and quadruple bandwidth of FDM multiplexers. Features include ARQ error control and downline loading that permits changes in remote site operation to be made from central location. Completely transparent to terminals, CPUs, and software, the multiplexer installs without changes in existing systems. **Prentice Corp,** 266 Caspian Dr, Sunnyvale, CA 94086.

Circle 238 on Inquiry Card

New! For Motorola EXORciser users.*



Process Current Expander
4-20mA with 250V Isolation
10,000 Samples/Sec.

High Level Expander
Up to 32 SE/16 DI Channels
Voltage or Process Current Inputs
20,000 Samples/Sec.

12-bit A/D Base Card
Programmable Gain
Programmable Offset
Expander Port
Auto Zero Circuitry

Millivolt/Thermocouple Expander
Flying Capacitor Design with 250V Isolation
Sensor Failure Detection
200 Samples/Sec.

Marries your micro to real world analog signals.

Here's the easy way to get your micro to accept industrial analog signals: Acromag's new Series 6800 Industrial Data Acquisition A/D Subsystem. It's compatible with the Motorola EXORciser bus and real world signals. Even in the presence of ground loops.

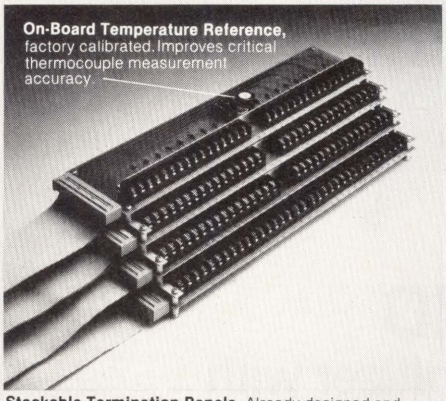
Our exclusive programmable offset feature gives resolution approaching that of a 14-bit system, with the speed and economy of a 12-bit.

Expands to 256 input channels (voltage, thermocouple and 4-20mA inputs) with only one base card.

Accepts any thermocouple input directly.

Thermocouple temperature reference on field wiring panel makes system independent of thermocouple type.

Auto zero feature improves accuracy over 0-70°C operating range.



Stackable Termination Panels. Already designed and built. So you don't have to do it. Industrial screw terminals provide practical solution to field wiring. Stacking feature saves space, simplifies later field expansion.

Powerful programming capabilities. Memory-mapped I/O with Auto Scan (and more).

Thermocouple linearization routines and software drivers available for fast system implementation.

The Series 6800 system's cards are electrically and mechanically compatible with the EXORciser bus. Just plug them in.

The 6810 base card includes a high speed 12-bit converter, programmable offset, programmable gain, external trigger and EXORciser bus interface/control logic.

Voltage, thermocouple and 4-20mA inputs are routed to appropriate expander cards where primary input filtering and signal conditioning take place. Expander cards may be mixed and matched for specific applications and do not present a bus load to the system.

For further details, call your local Acromag rep. Or write for Series 6800 packet. We'll also include a copy of our framable "Murphy's Laws of Instrumentation"...from the people who beat these laws with over 20 years of analog signal conditioning experience. Acromag, 30765 Wixom Road, Wixom, MI 48096. Ph: (313) 624-1541.

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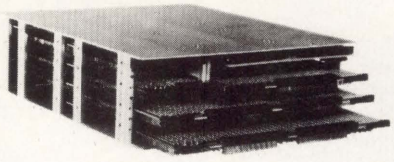
ACROMAG®

*TM of Motorola, Inc.

CIRCLE 129 ON INQUIRY CARD

PRODUCTS

HORIZONTAL CARD RACK



Three different size wirewrap panels or PCBs can be mixed in the same Mixer family of racks. The optional data bus backplane eliminates need for wirewrapping common signals; the I/O bus backplane has a 72-pin I/O connector associated with each 108-pin wirewrap connector. Wirewrap panel maximum size is 15.85 x 14.90″ (40.26 x 37.85 cm). Side plates permit cabinet and benchtop mounting. **Mupac Corp,** 646 Summer St, Brockton, MA 02402.

Circle 239 on Inquiry Card

DISC CONTROLLER

Compatible with CDC Storage, Cartridge, and Mini Module Drives, model 3000 controller can interface from 1 to 4 drives. The 1-board NOVA compatible embedded device features 1-command transfers of up to 32k words. Also included are R/W operations that are continuous across head and cylinder boundaries, transparent seeks, single command formatting, and internal diagnostics. **Mini-Computer Systems, Inc, Peripheral Products Div,** 399 Fairview Pk Dr, Elmsford, NY 10523.

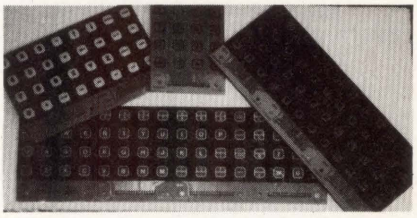
Circle 240 on Inquiry Card

IMPROVED TEST GENERATION SOFTWARE

Intended to accommodate future testing requirements, version 5.1 of LASAR features 3-state implementation in all LASAR modules, permitting test patterns consistent with bus-structured LSI/VLSI boards. Fault diagnostics are now consistent with 3-state operation. Program capacity range is for more than 8000 board level nodes and 512 input and 512 output nodes. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111.

Circle 241 on Inquiry Card

SWITCH PANELS



Designed to expand from 16 to 64 keys in 16-key increments, MOD-44 switch panels include tactile technology. Each side of each switch has a pin to provide for user coding; the pins are on 0.1″ (0.254-cm) centers for connector interface. Options include snap dome switch PC card, graphic overlay, rubber boot, and keycap assemblies. Contact rating is 24 Vdc at 10 mA, resistive. **KB Denver, Inc,** PO Box 119, Frederick, CO 80530.

Circle 242 on Inquiry Card

PC BOARD TESTER

High speed 3PX680 tests fully assembled PC boards including microprocessors, memories, and oscillators at full board operating speeds. This capability allows full testing at one station with one test, eliminates need to remove components from board, and reduces total test time. Fully compatible with existing 3PX500 and 600 series logic tester test programs, the unit's high speed test patterns dynamically test PCBs containing LSI and VLSI devices. **Three Phoenix Co,** 21639 N 14th Ave, Phoenix, AZ 85027.

Circle 243 on Inquiry Card

Advance Announcement...

Tutorial Week 80

Chairman: David Stomberg, CSC Arrangements: Roberta J. Kerr, CSC
Chairman, Tutorial Week West Standing Committee: Joseph P. Fernandez, IBM Corp.
Chairman, IEEE-CS Professional Development Committee: Stanley Winkler, IBM Corp.

A solid week of tutorials in 3 tracks • December 15-19, 1980

Attendance limited to 100 per tutorial. Advance registration only: deadline — November 14, 1980.

MONDAY, 12/15	TUESDAY, 12/16	WEDNESDAY, 12/17	THURSDAY, 12/18	FRIDAY, 12/19
① **VLSI from a User's Perspective** Rex Rice	② **Design of Microprocessor Systems** John H. Carson	③ **Microprocessor Interfacing** G. Jack Lipovski	④ **Microcomputer Control System Programming** (with hands-on experiments) Lance Leventhal	⑤ **Microcomputer System Software & Languages** Belton E. Allen
⑥ **A Pragmatic View of Distributed Processing Systems** Kenneth J. Thurber	⑦ **Distributed Processor Communication Architecture** Kenneth J. Thurber	⑧ **Local Computer Networks** Harvey Freeman	⑨ **Distributed System Design** David F. Palmer Michael P. Mariani	⑩ **Distributed Data Base Systems** Carl Kagan
⑪ **Software Management I** Donald J. Reifer	⑫ **Software Management II** Donald J. Reifer	⑬ **Software Requirements Analysis & Specification** Peter Freeman Anthony I. Wasserman	⑭ **Software Design Techniques** Peter Freeman Anthony I. Wasserman	⑮ **Software Systematic Construction** Peter Freeman Anthony I. Wasserman

Plus a special 3-part course for novices (Half-day sessions)

⑯ **An Intelligent Spouse's Guide to Computers** Part I, Part II, Part III — Ware Myers

Hotel Del Coronado San Diego, California

Attendance limited to 100. Register NOW!

Select up to one tutorial per individual per day.

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Includes bound tutorial text and luncheon.
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HOTEL ACCOMMODATIONS:

Reserve your room at the Hotel Del Coronado now. Write to:

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Attn.: IEEE Tutorial Week

RATES: Single or Double: $36.75
Lanai: $63.75; Parlor Suite: $101.25

Mail to: Tutorial Week 80, Box 639, Silver Spring, MD 20901

☐ I am interested in the following tutorials (Please circle numbers):
1 2 3 4 5 6 7 8 9 10 11 & 12 13 14 15 16
Please mail me the complete program announcement.

☐ I want to register right now. Enclosed is $_____ to reserve space at the following tutorials (Circle numbers as appropriate):
1 2 3 4 5 6 7 8 9 10 11 & 12 13 14 15 16

☐ Check enclosed ☐ VISA/Bank Americard ☐ Master Charge

Card #_____ Exp. Date_____ Signature_____

Name_____ IEEE or IEEE-CS Membership No._____

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City/State/Zip_____

IEEE COMPUTER SOCIETY

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC

PRODUCTS

4-CHANNEL, 9600-BIT/s MODEM

Conforming to CCITT recommendation V.29 and V.27 bis/ter, the 9629 LSI data modem can be optioned for 4-channel multiport capability. It features automatic equalization, displays BER count and contains local and remote loopback features. In V.29 mode, the modem operates through a combination of amplitude and phase modulation; in the V.27 bis/ter mode, it operates through phase shift keying (PSK). **Penril Corp,** 5520 Randolph Rd, Rockville, MD 20852.

Circle 260 on Inquiry Card

DESKTOP COLOR GRAPHICS TERMINAL

Available in semi-graphic (character oriented) or full graphic (point addressable overlay) models, CDT-7001 includes 13″ (33-cm) CRT, keyboard, and keypad. Half- or full-duplex communications at 110 to 9.6k baud is possible in asynchronous or block transfer modes. Up to 64 user defined characters are provided for. Onboard firmware supports line of peripherals. **The Telecrafters Corp,** 999 Pieffers Ln, Harrisburg, PA 17109.

Circle 261 on Inquiry Card

POWER FAILURE MONITOR

Two detectors, one to sense ac input voltage and the other to sense power supply input voltage comprise the PM-1 power failure monitor. The monitor provides a TTL 0 signal if the power supply voltage drops below an adjustable threshold voltage or if the ac input voltage is below its minimum rated value, supplying 5-ms advance warning of a pending output drop. A TTL 1 signals that the input voltage is within rated limits and the main output is above its threshold value. **Deltron Inc,** Wissahickon Ave, North Wales, PA 19454.

Circle 262 on Inquiry Card

LED TERMINAL MODULE

Each module consists of 3 matched, 7-segment digits and 34 matched indicators. 28 indicators state patterns, and 6 show appliance functions. The module includes a memory to recall and produce programmed functions, and a glass panel with an array of touch sensitive control switches to enable the indicated preprogrammed function. Individual 10 x 10-mil LED matched die are mounted on the PC board. **Opcoa, Div of IDS Inc,** 330 Talmadge Rd, Edison, NJ 08817.

Circle 263 on Inquiry Card

BUMPLESS TRANSFER DAC

ISO-DAC™ converts 10-bit digital word to an isolated 4- to 20-mA signal, providing computer bus interface, bumpless transfer, and galvanic isolation. Max common mode voltage of the DAC1423 is specified at ±1500 Vdc, continuous, ±1000 V at 60 Hz. Transient protection meets IEEE 472-1974, and common mode rejection is 103 dB at 60 Hz and 250 Ω. Monotonicity is guaranteed from 0 to 70 °C with integral and differential nonlinearities of ± ½ LSB. **Analog Devices, Inc,** Rte 1 Industrial Pk, Norwood, MA 02062.

Circle 264 on Inquiry Card

MULTICHANNEL ANALYZER

The series 40 offers up to 8192 channels with $2^{20}-1$ counts/channel and a 100-MHz, 8192-channel ADC with either a 300-kHz (std) or optional 20-MHz MCS. A 9″ (23-cm) raster scan CRT provides both linear and log data modes plus alphanumeric text area and multiple ROI. Std features include peak net area, fractional stripping, and energy calibration. Built in terminal interface handles TTY, EIA, and cassette I/O. **Canberra Industries, Inc,** 45 Gracey Ave, Meridan, CT 06450.

Circle 265 on Inquiry Card

SMALL TAPE CARTRIDGE DRIVE

MicroDrive/OEM series tape drives offer up to 1.344M bytes of data storage in mechanism only or minimum electronics only board configurations. Measuring 3.63 x 3 x 2.63″ (9.22 x 7.62 x 6.68 cm), the minimum electronics only board provides a switching power amplifier to drive the motor, digital interface, write amplifier, and read preamp. Only the circuitry required to interface the transport mechanism is included on the mechanism only board. **Moya Corp,** 6319 Desoto Ave, Unit K, Woodland Hills, CA 91367.

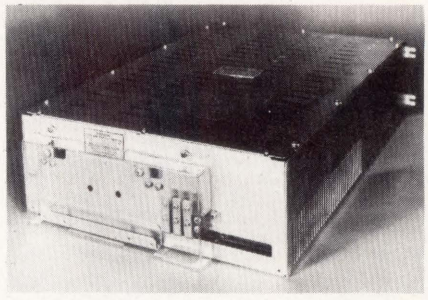
Circle 266 on Inquiry Card

FIBER OPTIC DATA LINK

HLT-10/HLR-10 consists of a single-fiber optical cable, terminated at both ends, which plugs into 856 x 490 x 490-mil hybrid transmitter and receiver modules. The modules can be plugged directly into a PC board. The data link offers a bandwidth from 10k to 10M bits/s and a dynamic range of 30 dB. The transmitter contains GaAs LED that transmits up to 2 km over single-fiber cable without repeaters. Peak emission wavelength of the LED is 820 nm. **Galite, Inc,** 2 Tower Dr, Wallingford, CT 06492.

Circle 267 on Inquiry Card

BATTERY BACKUP UNIT



Battery backup unit bridges power line disturbances such as voltage spikes, oscillatory power decays, and undervoltages. The single-board unit will support the CPU and memory of ECLIPSE® minicomputers for 2 min. Advanced Operating System (AOS) software has been enhanced to provide ECLIPSE battery backup system users with an orderly processing shutdown when an ac power failure occurs. The unit is air cooled and is rechargeable, requiring no separate ac power. **Data General Corp,** Rte 9, Westboro, MA 01581.

Circle 268 on Inquiry Card

The Universal™ Intelligent Controller and the 5 Little Plugs

Five plug sets is all it takes for simultaneous, multi-device storage control. DML's Universal™ Intelligent Controller makes it possible.

- S-100 Bus, with CP/M* support
- Plug adaptable device support
- Control of up to 8 storage devices: 4 fixed disks, 4 floppy or tape cartridge drives
- IEEE DMA or port transfer

Call or write for full information. Data Management Labs, 2148 Bering Drive, San Jose, CA 95131 (408) 946-9424.

*CP/M is a trademark of Digital Research

DML

DATA MANAGEMENT LABS

CIRCLE 131 ON INQUIRY CARD

FIBER OPTIC LINK TEST SET

A fiber optic link test set, model 650A, features interchangeable plug-in modules which accept a variety of connectors, sources, and detectors. A high power LED emitter couples light into the link under test through a front panel connector at a −30-dBm level. The device's range is 2 to −80 dBm, with an absolute receive light level accurate to ±1 dB. Also included are rechargeable batteries and charger. **Bowmar/ALI, Inc,** 531 Main St, Acton, MA 01720.

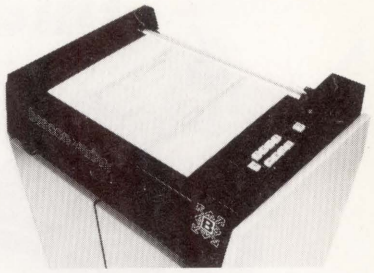
Circle 244 on Inquiry Card

μC CONTROLLED MODEMS

BIZCOMP™ 1030 and 1031 Intelligent Modems™ combine low error rate modems with ACU and BIZ-080 microcomputers into FCC registered units having auto answer, auto dial, and auto repeat features. Code multiplexed design allows modem control via same terminal used for data communications. Model 1031 also has command selectable pulse or tone dialing, plus self test. Both models have auto baud feature, with 5 data rates covering 110 to 300 baud. **Business Computer Corp,** PO Box 7498, Menlo Park, CA 94025.

Circle 245 on Inquiry Card

ELECTROSTATIC PRINTER/PLOTTER



Model 9222Q 22″ (55.9-cm) electrostatic printer/plotter incorporates Quadrascan® writing head with 4 offset rows of styli. Each printed dot overlaps adjacent dots by approx 50% for uniformity and blackness of solid areas. Print speed is to 560 lines/min and plot speed 1.5 in (3.8 cm)/s. Features include dynamic toning, automatic supply level monitoring and concentrate add, and integral paper takeup. Std model has char generator with 2 software selectable char sizes. **Benson-Varian, Inc,** 385 Ravendale Dr, Mountain View, CA 94043.

Circle 246 on Inquiry Card

RIPPLE REGULATOR

Up to 12 Vdc at 4 A may be provided at efficiencies of 85% or more by the WM14-40/S12/4000/U dc-dc converter. Input to the converter is 24 Vdc (14- to 40-Vdc range) at 25 kHz. Included are overvoltage protection, short circuit current limiting, and remote sensing with protection against disconnection. Output may be adjusted with an external trimpot over a ±10% range. **Stevens-Arnold, Inc,** 7 Elkins St, South Boston, MA 02127.

Circle 247 on Inquiry Card

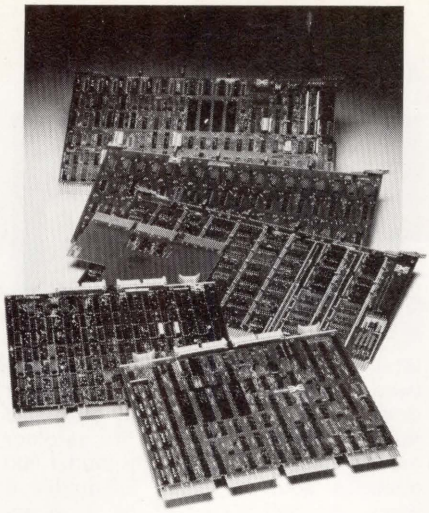
MASS-TERMINATED CARD EDGE CONNECTOR

Single-sided 0.062″ (0.157 cm) thick PCBs with circuit pads on 0.156″ (0.396-cm) centers may be mass terminated to discrete wire or ribbon cable (AWG 26 through 18) with MTA card edge connectors. Available in 3, 6, 9, 12, 15, 18, and 20 through 24 positions, with locking and keying plugs, covers, and optional snap-in contacts, the device is made of natural color 94 V-O rated thermoplastic. **AMP, Inc,** Harrisburg, PA 17105.

Circle 248 on Inquiry Card

We're the company building a business by building the industry's preferred stock of software-transparent, microprogrammed controllers for DEC cpu's.

Now we're broadening our offerings for mag tape users



Our two new tape controllers give us the industry's broadest line of software transparent controllers for LSI-11, PDP-11 and PDP-11/70 users.

For all you mag tape users. New stock offering in DEC.

even further. Two new controllers that make it easy to climb aboard the LSI-11 Qbus and PDP-11/70 Cache bus. And a brand new discount schedule, the most aggressive in the industry.

You're probably familiar with our TC11 controller, introduced at last year's NCC. It's the proven dual-density controller that puts virtually any tape transport on the PDP-11 Unibus.

Now we put you on the LSI-11 Qbus, too, with our new TC01. It's the first and only fully-embedded dual-density controller for use with LSI-11, 11/2 and 11/23 cpu's.

It's fully compatible with DEC's TU10/TM11 tape subsystems. And it gives you the option of NRZ or PE format at all speeds up to 75 ips.

We've got a new offering for 6250 bpi tape users, too. Our TC70 controller puts you on DEC's PDP-11/70 Cache bus to meet your high density GCR storage needs. It functionally emulates the TWU45/TWU77 tape subsystems from DEC.

Fact of the matter, it makes no difference which DEC series 11 cpu you're using, or what storage device. We support 59 different drives. Including 14-inch Winchester and SMD class disks. And we're adding more all the time.

You might say we're bullish on DEC. Ask your peripheral salesman. Chances are he'll tell you we're blue chip. After all, we make his job that much easier.

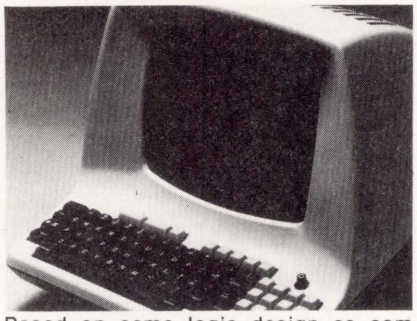
And ask us about our new discount schedule. And for your copy of our Buyer's Guide. Call or write today. Emulex Corporation, 2001 East Deere Avenue, Santa Ana, CA 92705. (714) 557-7580.

EMULEX

CIRCLE 133 ON INQUIRY CARD

PRODUCTS

DUMB CRT DISPLAY TERMINAL



Based on same logic design as company's ADM-3A Dumb Terminal^{R}, model ADM-3A+ includes additional features to speed operations. Some of these are built-in 0 to 9 numeric keypad, period, comma, tab, minus, and return, plus cursor control keys for single stroke up, down, left, right, and home. Caps-lock key and full u/lc char display with 2-dot descenders are std. Program mode key permits writing into display memory and displaying all control codes in addition to ASCII 96-char set. **Lear Siegler, Inc, Data Products Div,** 714 N Brookhurst St, Anaheim, CA 92803.

Circle 249 on Inquiry Card

FULL KEY TRAVEL 1-PIECE MODULAR KEYBOARD

Only 3 parts are used for each switch assembly in 58- or 64-key alphanumeric and optional 16- or 20-key side arrays. Contact reliability exceeds 10M cycles, switch operating force is 60 g, and switch assemblies may be wave or hand soldered to the PCB. Contact rating is 12 Vdc, 0.5 W max, with 1-mΩ max contact resistance. Keytops can be of stepped or sloped configuration. **Mechanical Enterprises, Inc,** 7 Park Ctr, Sterling, VA 22170.

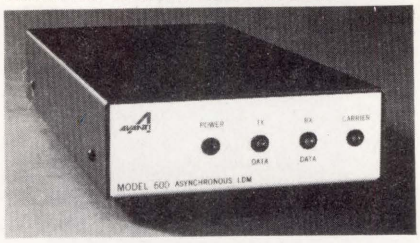
Circle 250 on Inquiry Card

CRT TERMINAL WITH FULL SCREEN EDITING

Containing an 80-char x 24-line display, plus integral full ASCII keyboard and 14 function keys, the CDP18S040 CRT terminal includes an RS-232-C interface, 300- to 19.2k-baud selectable rates, and full screen editing capability. Based on the CDP1802 microprocessor, the unit's totally CMOS circuitry provides for cursor positioning, 2-speed auto repeat cursor movement, overtype, char or line insertion/deletion, and scrolling. **RCA Solid State Div,** Box 3200, Somerville, NJ 08876.

Circle 251 on Inquiry Card

ASYNCHRONOUS LIMITED DISTANCE MODEM



Intended to transmit digital data between asynchronous terminals and/or computers operating over unloaded telephone company loops or customer owned metallic circuits, the model 600 operates point to point, full-duplex 4 wires, or half-duplex 2 or 4 wires. Available in desktop or rackmount modules, the device functions at up to 9600 bits/s with RS-232-C interface. **Avanti Communications Corp,** Aquidneck Industrial Pk, Newport, RI 02840.

Circle 252 on Inquiry Card

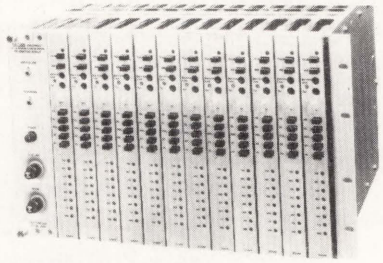
80- AND 250-CHAR/s MATRIX PRINTERS

P80 is a low cost, 80-char/s matrix printer which features true char descenders, underlining, bidirectional logic seeking, processing of single-sheet or continuous forms, and self-testing routines. P250 uses a 7 x 9 char pattern with 9 x 9 pattern optional, and has true char descenders and underlining capabilities. In addition, it is bidirectional logic seeking and is capable of operating asynchronously at transfer speeds from 50 to 19,200 baud. **Pertec Computer Corp, Peripherals Div,** 12910 Culver Blvd, Los Angeles, CA 90066.

Circle 253 on Inquiry Card

1200-BIT/s FULL-DUPLEX RACKMOUNT MODEM

Operating at a 300- or 1200-bit/s rate, the 212AR full-duplex modem offers port security, direct connect switched network operation, Bell compatibility, integral diagnostics, and a service line option for telephone line access. The rackmount microprocessor based device can be used with rotary or touch dial types of systems for manual call origination and manual or auto answering. **General DataComm Industries, Inc,** 1 Kennedy Ave, Danbury, CT 06810.



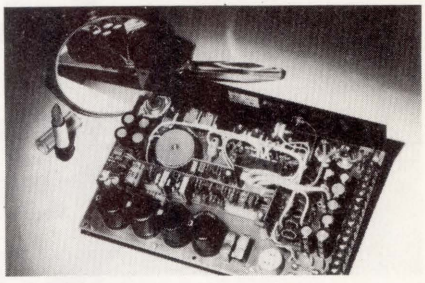
Circle 254 on Inquiry Card

FONT AND COMMUNICATIONS OPTIONS FOR LINE PRINTER

Host defined font option for the T-3000 300-line/min printer allows loading different char fonts downstream from computer or other host while printer is in operation. Another 128-char set can be added to std stored char set without affecting printer speed. Buffered asynchronous communications adapter, available in 3 different protocols, allows 300-line/min printing of transmitted data online at 4800 baud. Data transfer to the T-3000 is bit serial char asynchronous via RS-232 or 20/60-mA current loop interface. **Mannesman Tally,** 8301 S 180th St, Kent, WA 98031.

Circle 255 on Inquiry Card

6-OUTPUT OPEN FRAME SWITCHING POWER SUPPLIES



300-W SCB306 units provide 6 separate regulated outputs of 5 V at 20 A, 12, 15, −12, −15, and 24 V at 4 A. Line regulation is 0.2% max. Load regulation is 0.3% max on the 5-V output, and 5% on the ±12-, ±15-, and 24-V outputs. ±15-V outputs have isolated ground returns. Input voltage is either 115 or 230 Vac (−20%, +10%) at 47 to 440 Hz. 2.5 x 11.75 x 7.6″ (6.4 x 29.8 x 19.3-cm) units mount on either of 2 surfaces. Convection cooling is used. **KEC Electronics, Inc,** 19300 S Vermont Ave, Gardena, CA 90248.

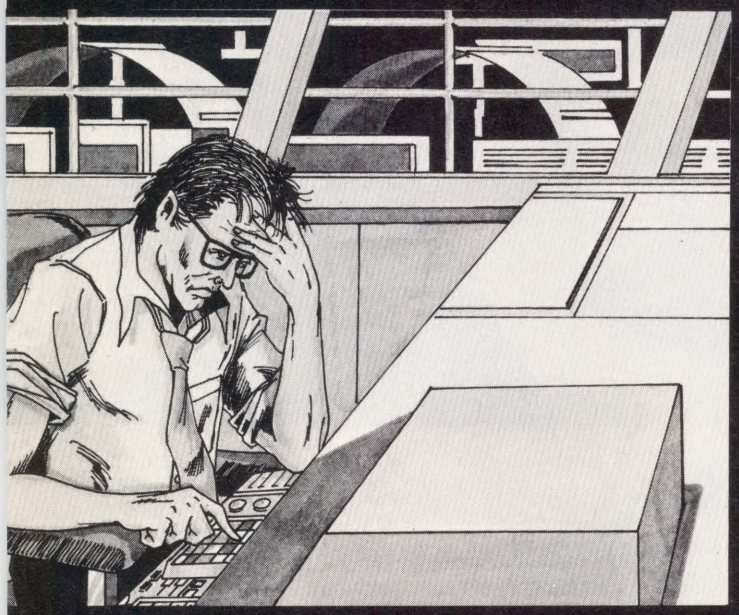
Circle 256 on Inquiry Card

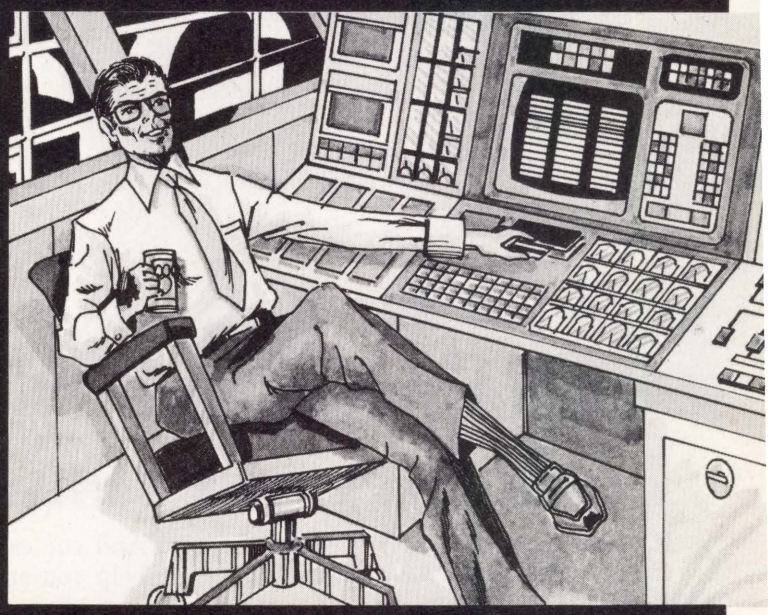
9600-BIT/s MODEM WITH BUILT-IN CONCENTRATOR

Micro8000 modem series features built-in concentrator and automatic retransmission on error. Automatic adaptive equalizers compensate for line problems. Unit operates at 4800 or 9600 bits/s on unconditioned leased lines. 2, 4, 8, or 12 asynchronous data terminals can share error free transmission on line without changes to existing hardware or software. No asynchronous to synchronous converters are required. Microprocessor design with MOS/LSI implementation results in compact unit. **Micom Systems, Inc,** 9551 Irondale Ave, Chatsworth, CA 91311.

Circle 257 on Inquiry Card

Put an end to program reloading.



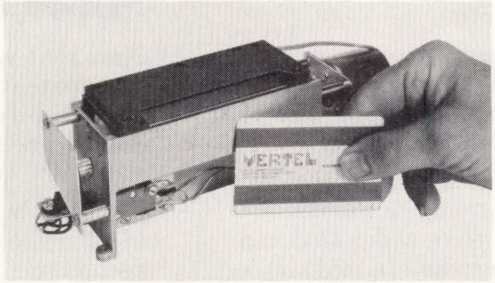


Set it up once . . . and forget it with the KILOBYTE CARD™ READER / WRITER.

With the Vertel KB-31 System, there is no longer any need to manually enter the same program more than once. Simply enter the program into the system, as you normally would, then let the system record the program on our KILOBYTE CARD with our KB-31 Microloader; when you are ready to re-use that program simply insert the KILOBYTE CARD into the KB-31 and your program will be loaded automatically into your system.

Designed for microprocessor based systems, this rugged, low cost*, field-proven performer is ideally suited for everything from intelligent terminals and instrumentation to machine tool controls and test equipment.

*As little as $192 in OEM quantities.



The 4-stripe magnetic KILOBYTE CARD can record up to 1,088 eight-bit bytes and with the microloader, it is the ideal peripheral for parameter loading, field program modifications, and user activated diagnostics.

To learn how the KILOBYTE system can benefit your operations, call or write today for details on our free, thirty-day trial offer.

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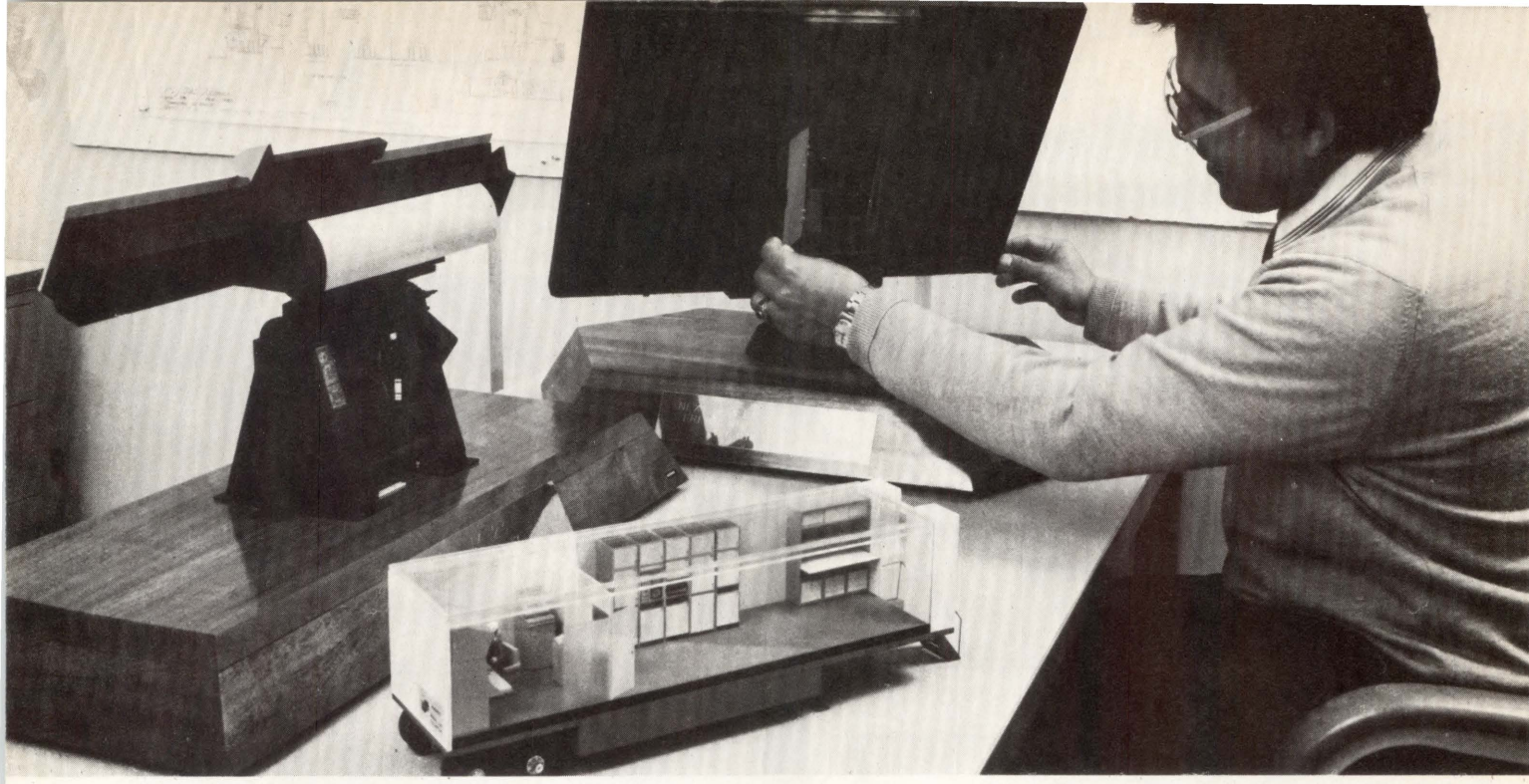

Look over our resume.

If you want to start at the state of the art, and move ahead from there—

Better make sure the place you go to work in the Eighties has a record of reaching beyond the ordinary.

We have.

Join us, and you'll be welcome to use everything we know.

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Our company has a 4½ billion dollar backlog—more than 1,500 high-technology projects. Many of the most challenging are here, at Hughes Ground Systems in Southern California's easy living Orange County.

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Now that you've read a couple of our credentials, please send us your own resume. Tell us what you've been doing lately, and what you'd like to be doing soon.

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The PM3500 100MHz 16 Channel Logic Analyzer

- Performs state and timing analysis both synchronously and asynchronously.
- Choose binary, hex, octal, mapping, or timing display.
- 505 X 16 bits memory format, or two 249 X 16 bit active memories in compare mode.
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- External triggering through separate input.
- Triggering can be delayed up to 9999 clock pulses, which can be set to walk or run through the data stream.
- Data input 5:1 probe tips matched for 100MHz operation and can be grouped or used singly.

The PM3540 10MHz Logic Analyzer and Real-Time Scope

- Accepts 16 channels of input data.
- Checks software and hardware together.
- Choose binary, hex, or octal coding.
- 64 X 16 bits active memory, plus separate 64 X 16 bit compare memory.
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- Digital delay of up to 9999 clock pulses.
- "Store Trig" provides quick and convenient paging both upstream and downstream.
- Microproccessor- equipped for display and basic logic analyzer functions plus comprehensive self-testing.

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LITERATURE

Switches, Keyboards, Relays, and Hardware

Catalog with photos and drawings details each product group dimensionally and electrically and provides specs, switch selector chart, and switch and solid state relay engineering information. **Grayhill, Inc,** La Grange, Ill.
Circle 300 on Inquiry Card

Thermocouple Termination Modules

Bulletin illustrates and lists features of OM101 10-channel precision isothermal thermometer and OM102 10-channel thermocouple scanner, and details performance of the latter. **Omega Engineering, Inc,** Stamford, Conn.
Circle 301 on Inquiry Card

Capacitors and Resistors

Catalog describing 13 capacitor series, 2 resistor series, and 10 designer's kits includes chart with cross-reference to major manufacturers for making direct replacements. **Capar Components Corp,** Melville, NY.
Circle 302 on Inquiry Card

Prototyping Parts

Devices included in 52-p selection guide range from components to board level products. **Priority One Electronics,** Sepulveda, Calif.
Circle 303 on Inquiry Card

Socket Assemblies and Headers

Dimensional drawings, photos, specs, part number codes, and lists of features are supplied by brochure detailing SGF/SGH series mass termination systems. **Augat Inc,** Attleboro, Mass.
Circle 304 on Inquiry Card

Microprocessor Elements

ICs and support system for RCA 1800 COSMAC family, data for RAMs, ROMs, and I/O devices, diagrams, and cross-reference to other manufacturers' devices are found in product guide MPG-180C. **RCA Solid State Div,** Box 3200, Somerville, NJ 08876

Power Sources

Wall chart presents ac-dc power supplies and dc-dc converters, with lists of input and output voltages and package size, and gives features and specs of offline switchers. **Semiconductor Circuits, Inc,** Haverhill, Mass.
Circle 305 on Inquiry Card

Miniature Encoders

Information kit comprises Microseries data sheets giving technical descriptions of absolute optical shaft angle encoders and bulletins discussing applications and optical equipment. **Itek Measurement Systems Div,** Newton, Mass.
Circle 306 on Inquiry Card

Fiber Optics

Published quarterly, "FiberTopics" covers products, applications, technological advances, and activities in the telephone, broadcasting, CATV, military, and data communications markets. **Valtec Corp,** West Boylston, Mass.
Circle 307 on Inquiry Card

Multipoint Polling System

Brochure introducing Micro 900 multidrop concentrator discusses applications, installation, troubleshooting, and features of five models, and provides specs plus drawing of typical configuration. **Micom Systems, Inc,** Chatsworth, Calif.
Circle 308 on Inquiry Card

Plastic Display/Readout Panels

List of features, description, information on choice of panel substrates, color selection, and surface treatments, plus discussion of options are found in brochure together with photos. **Panelgraphic Corp,** West Caldwell, NJ.
Circle 309 on Inquiry Card

Switching Power Supplies

Detailed in brochure with photos, drawings, and tables are specs on ac-dc and dc-dc models, from 10 to 300 W, in single-, dual-, and triple-output designs. **Kepco, Inc,** Flushing, NY.
Circle 310 on Inquiry Card

Picture Digitizer and Display

With photos, flow and block diagrams, and tables, handbook on EyeCom II describes black and white as well as pseudocolor and true color displays, graphics and alphanumerics overlays, calibration, and software. **Spatial Data Systems, Inc,** Goleta, Calif. Circle 311 on Inquiry Card

Zero Insertion Force Rectangular Connectors

Illustrated catalog lists standard data on DL Series and presents plugs and receptacles, accessories, applications, graphs of temperature/current ratings, shell dimensions, panel cutouts, contacts, tooling, and assembly information. **ITT Cannon Electric,** Santa Ana, Calif.
Circle 312 on Inquiry Card

Data Communications and Transmission Test Equipment

Described and illustrated in catalog are 500-series for testing transmission line parameters, 700-series for general transmission line measurements, 800-series for data system analysis, and 4200 Network System. **Halcyon, Inc,** San Jose, Calif.
Circle 313 on Inquiry Card

Interactive Memory Board Tester And Memory Test System

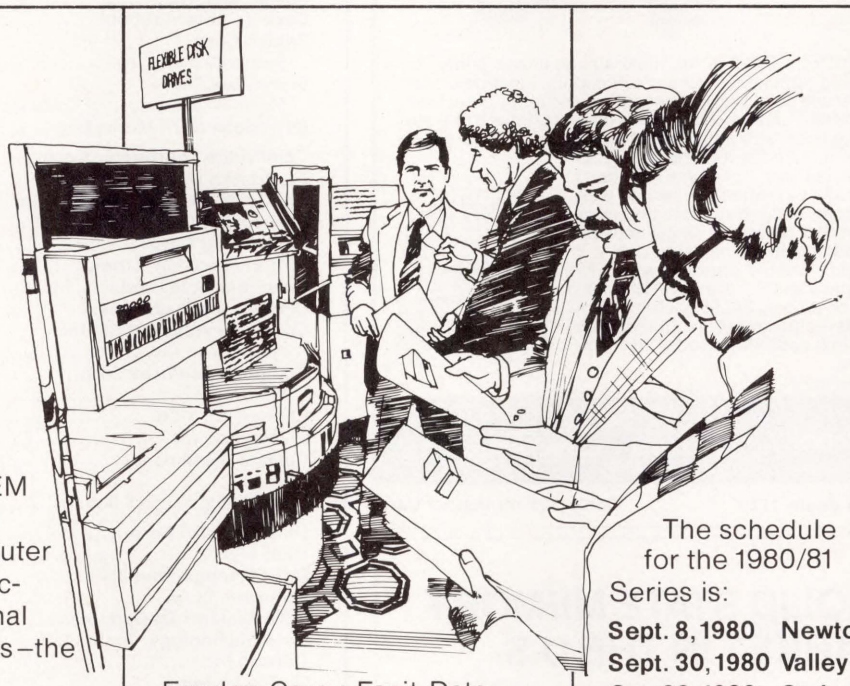
One of two brochures presents applications, production highlights, block diagram, and specs for Macrodata MD-207/11 tester; other includes features, software, interfacing, and block diagram for M-1 test system. **Eaton Corp,** Cleveland, Ohio.
Circle 314 on Inquiry Card

Statistical Multiplexers and Network Processors

Presenting features of Integrated Network Architecture (INA) and System 355 Master Network Processor, booklet also contains application and network diagrams plus chart showing INA component compatibility. **Digital Communications Associates, Inc,** Norcross, Ga.
Circle 315 on Inquiry Card

OEM America Meets

At The Invitational Computer Conferences



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