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COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

FEBRUARY 1981

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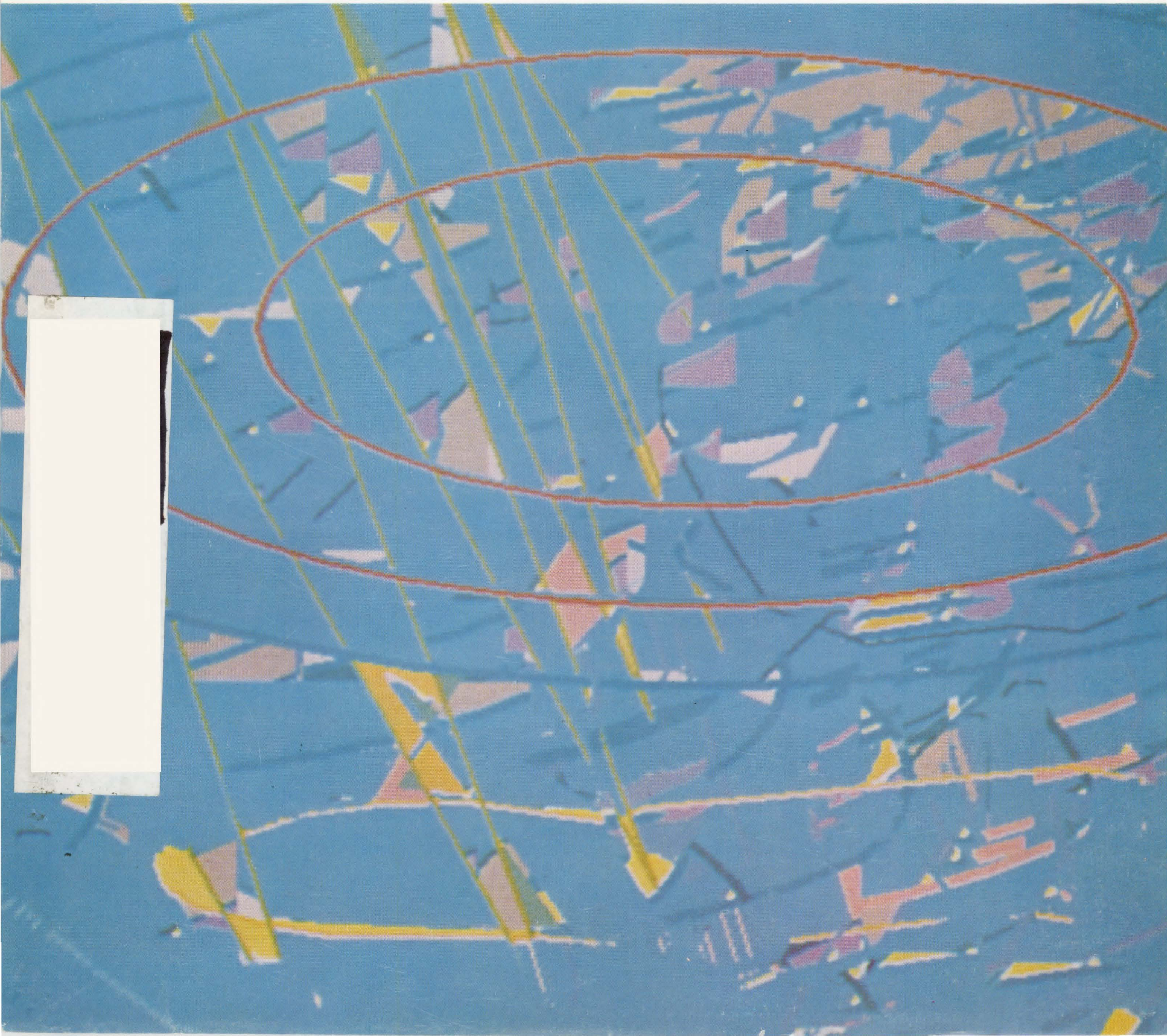

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CIRCLE 130 ON INQUIRY CARD

COMPUTER DESIGN® THE MAGAZINE OF COMPUTER BASED SYSTEMS

VOLUME 20, NUMBER 2

FEBRUARY 1981

DEPARTMENTS

Cover by Darcy Gerbarg
Created at the Computer Graphics Research Laboratory of the New York Institute of Technology

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FEATURES

CONFERENCE

VBPA ABP

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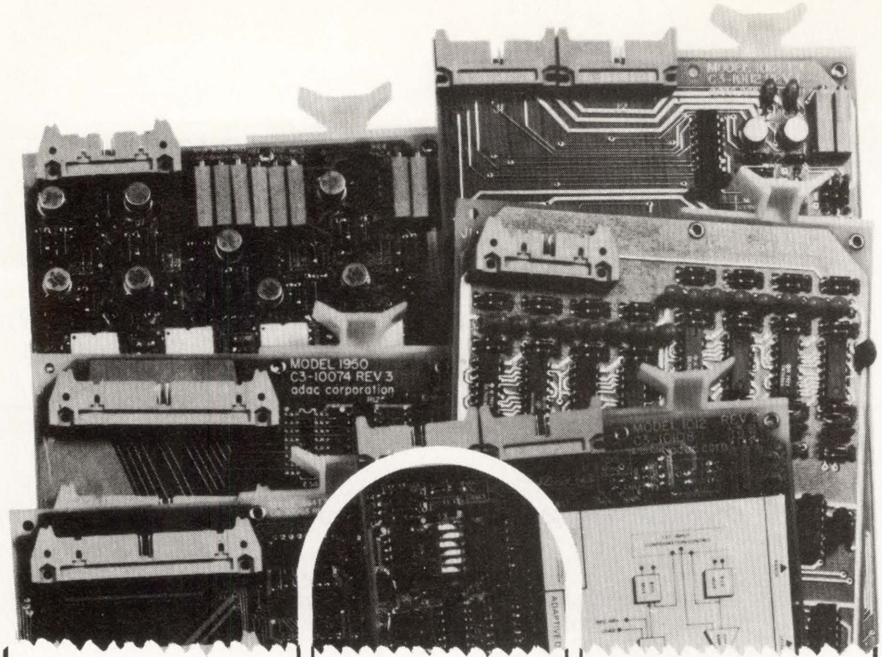
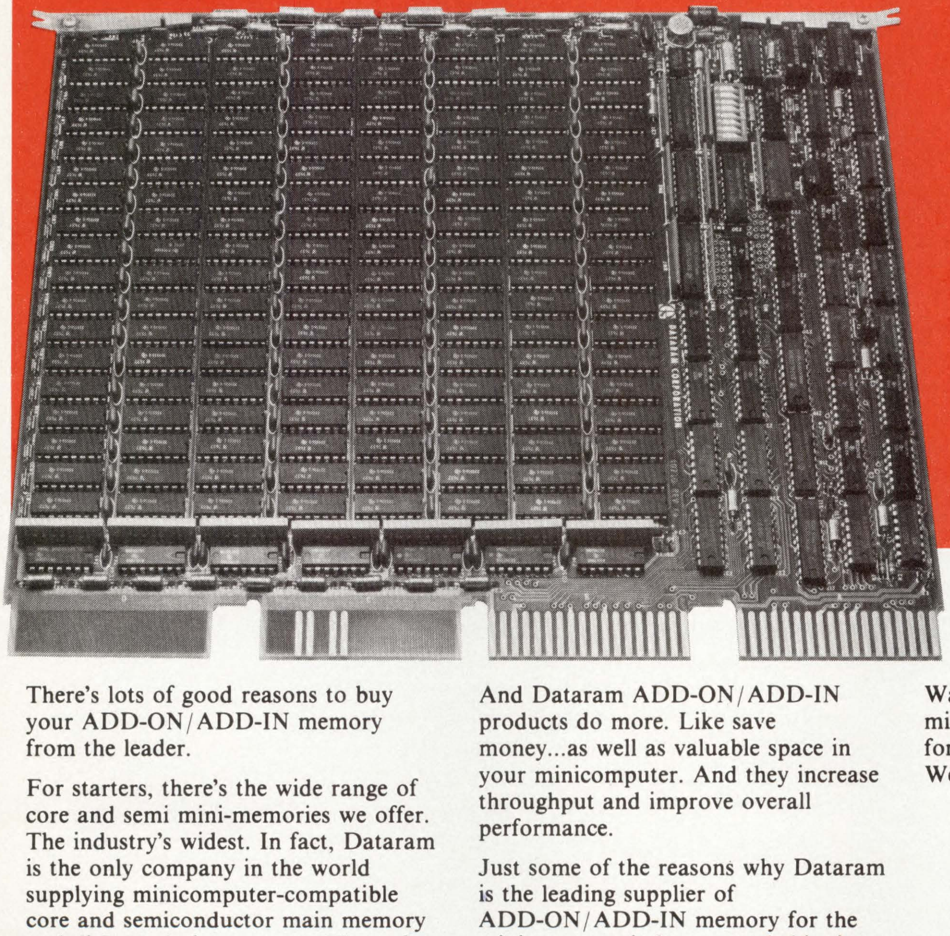

MODEL 1950
C3-10074 REV 3
adac corporation

ADD-ON ADD-IN

MEMORY...FROM THE LEADER



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CIRCLE 4 ON INQUIRY CARD

Compare our data and time domain logic analyzer with the industry's leading data-domain-only unit.

For complete analysis, the K100-D outperforms H-P's 1610B!

Before you settle for the Hewlett-Packard 1610B data domain analyzer, compare it with the general purpose Biomation K100-D, our fastest-selling logic analyzer ever.

Compare depth of information.

A data domain (software) analyzer—even a unit as sophisticated as the H-P 1610B—simply does not give you all the information you need for debugging your mainframe, mini- and microprocessor-based systems. During the critical system-integration stage of a development cycle, a problem that looks like a software failure may turn out to be a not-too-obvious hardware malfunction. The K100-D's data/timing capability lets you analyze software/hardware relationships and find the problem, wherever it originates. You can display up to 16 channels of critical timing information about race conditions and phase relationships between signals.

So vital is this timing information to complete problem analysis that industry trends indicate logic analyzers of the future will have both data and timing analysis capabilities—like the K100-D has today!

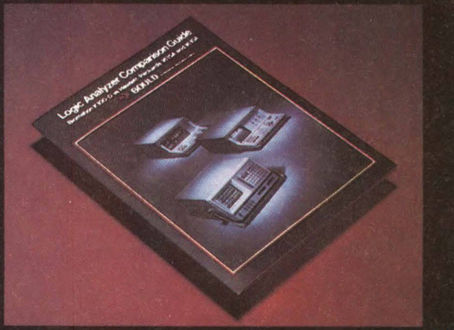
Compare data domain range.

The high-speed K100-D gives you data domain capability to 70 MHz—as compared with the 1610B's 10 MHz rate—for use with faster multiplexed microprocessors, computers, and ECL bit-slice processors. At 12 to 70 MHz, the K100-D gives you 16 channels of data display, with 1024 words of memory.

Operating at 0 to 10 MHz, both units give you 32 channels of data domain information. But the K100-D's memory is 8 times as deep as the 1610B's—512 words versus 64. The 1610B's 7 levels of triggering exceed the needs of most users, and those who do need this capability can generally get it from their development system. With the K100-D, you don't sacrifice vital timing information for data domain capabilities you don't need.

The final analysis.

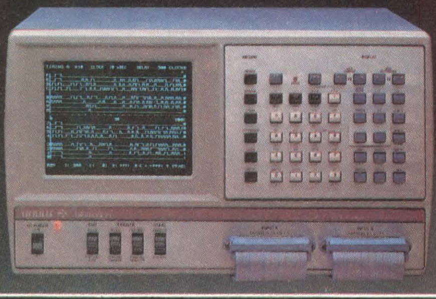
To help you evaluate your needs before you buy, we've prepared a point-by-point competitive comparison of the Biomation K100-D and the H-P 1610B. (Incidentally, it also shows how the K100-D beats H-P's general purpose 1615A hands down.) To get your free copy, just use the reader service number or write Gould Inc., Instrument Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.



Hewlett-Packard 1610B
A sophisticated data-domain-only logic analyzer

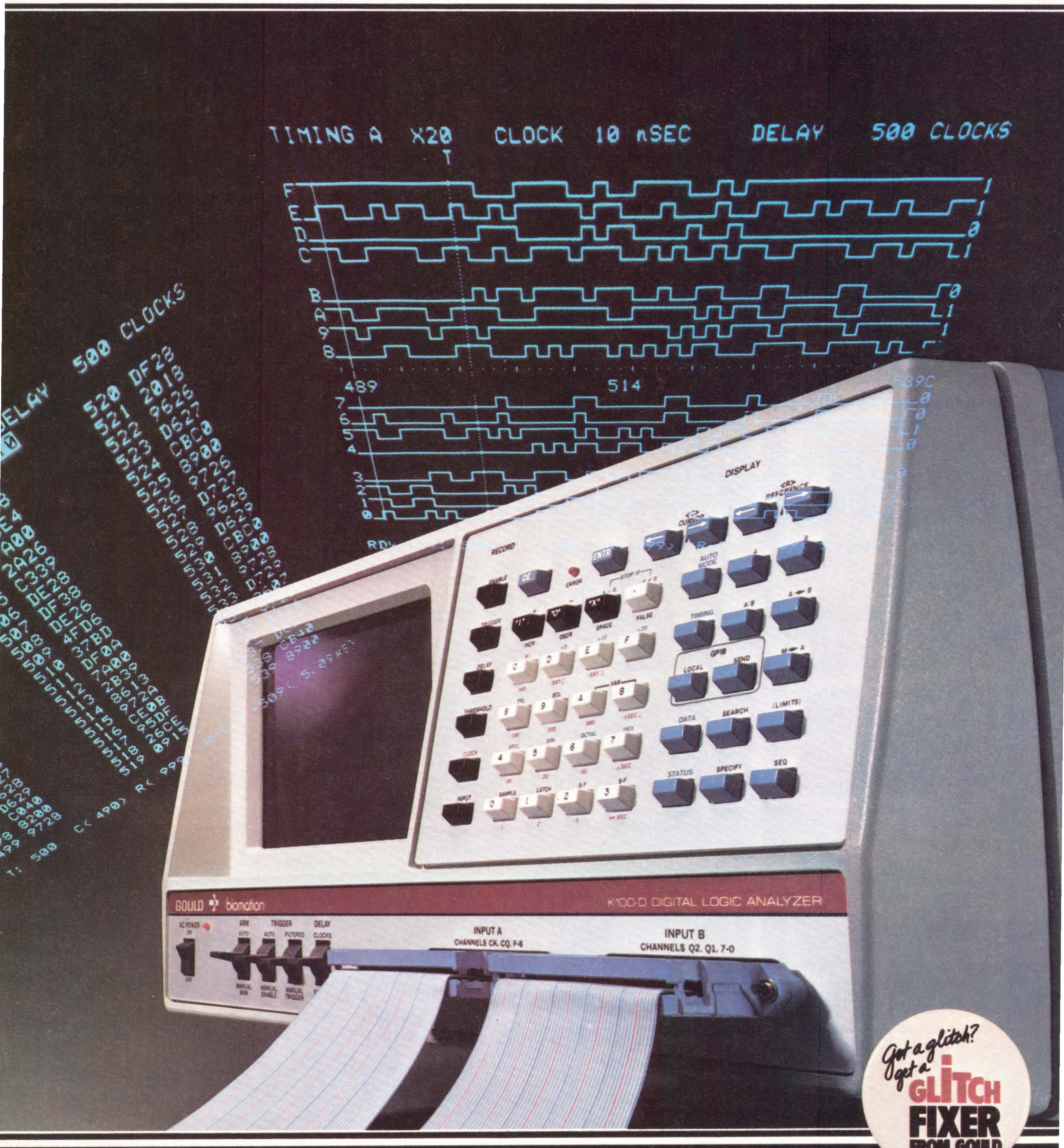
Analysis: Software
Speed: to 10 MHz
Channels: 32 data
Memory: 64 words

Biomation K100-D
The industry's finest data/timing logic analyzer



Analysis: Software & Hardware
Speed: to 70 MHz data domain
to 100 MHz time domain
Channels: 32 data to 12 MHz,
16 data to 70 MHz,
16 timing to 100 MHz
Memory: 1024 words @ 16 channels
512 words @ 32 channels

BIOMATION K100-D



GOULD

An Electrical/Electronics Company

CIRCLE 5 ON INQUIRY CARD

CALENDAR

CONFERENCES

MAR 3 AND MAR 5—Invitational Computer Conf, Dallas Marriott, Dallas, Tex, AND Adams Mark Hotel, Houston, Tex. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

MAR 11-13—Business & Computer Sales Expo '81, AND New York Business Show, Madison Sq Garden, New York, NY. INFORMATION: George Pachter, Produx 2000, Inc, PO Box 2000, Bala Cynwyd, PA 19004. Tel: 215/457-2300

MAR 12—California Computer Shows, Inn-at-the-Park, Anaheim, Calif. INFORMATION: Norm De Nardi, 95 Main St, Los Altos, CA 94022. Tel: 415/941-8440

MAR 16-18—Industrial and Control Applications of Microprocessors, IECI '81, Sheraton Hotel, Philadelphia, Pa. INFORMATION: H. Troy Nagle, Dept of Electrical Engineering, Auburn U, Auburn, AL 36830

MAR 23-25—Office Automation Conf, Albert Thomas Convention Ctr, Houston, Tex. INFORMATION: Kate Frye, Office Automation Conf, PO Box 9659, Arlington, VA 22209, Tel: 703/558-3617

MAR 23-26—Internat'l Conf on Digital Communications, Congress Bldg, Internat'l Fair of Genoa, Genoa, Italy. INFORMATION: Manager, Rome Branch of Administrative Office, 5th ICDSC, Telespazio SPA, Corso D'Italia 43, 00198 Rome, Italy

MAR 24-26—FOC '81 EAST, Internat'l Fiber Optics and Communications Expo, Hyatt Regency, Cambridge, Mass. INFORMATION: Ellen M. Bond, Information Gatekeepers, Inc, 167 Corey Rd, Brookline, MA 02146. Tel: 617/739-2022

MAR 24-27—Printemps Informatique, Palais des Congres, Paris, France. INFORMATION: Kallman Assocs, 30 Journal Sq, Jersey City, NJ 07306. Tel: 201/653-3304

MAR 30 AND APR 1—IEEE Internat'l Conf on Acoustics, Speech, and Signal Processing, Sheraton-Atlanta Hotel, Atlanta, Ga. INFORMATION: Ronald W. Schafer, Dept of Electrical Engineering, Georgia Inst of Tech, Atlanta, GA 30332. Tel: 404/894-2917

APR 1-3—Internat'l Conf on Distributed Computing Systems, Paris, France. INFORMATION: E. Gelinbe, Univ de Paris-Sud, LBI Batlment 490, 91405 Orsay Cedex, France

APR 3-5—West Coast Computer Faire, Civic Auditorium, San Francisco, Calif. INFORMATION: Computer Faire, 333 Swett Rd, Woodside, CA 94062. Tel: 415/851-7075

APR 6-8—Internat'l Sym on Computer Message Systems, Chateau Laurier Hotel, Ottawa, Canada. INFORMATION: IFIP TC-6 Sym '81, Bell-Northern Research Ltd, Dept 3D20, PO Box 3511, Sta C, Ottawa K1Y 4H7, Canada

APR 7-9—Electro, Coliseum and Sheraton Ctr, New York, NY. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

APR 7-9—Internat'l Reliability Physics Sym, Sheraton-Twin Towers, Orlando, Fla. INFORMATION: John Edwards, Gen'l Chm, American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051. Tel: 408/246-0330

APR 7-9—Survival and Growth of the Engineering Industries through Integration of CAD/CAM Technology, Carlton Hotel, Cannes, France. INFORMATION: Rhonda Gerganess, Computer Aided Manufacturing International, Inc, 611 Ryan Plaza Dr, Suite 1107, Arlington, TX 76011. Tel: 817/265-5328

APR 23—California Computer Shows, Hyatt-Palo Alto, Palo Alto, Calif. INFORMATION: Norm De Nardi, 95 Main St, Los Altos, CA 94022. Tel: 415/941-8440

APR 26-30—Comunicaciones Expo '81, Coconut Grove Exhibition Center, Miami, Fla. INFORMATION: Gloria Gomez-Mena de Marina, Marketing and Promotion Div, City of Miami, Office of Trade and Commerce Dev, 100 N Biscayne Blvd, Suite 901, Miami, FL 33132 Tel: 305/579-3320

APR 27-29—IOOC '81 (Internat'l Conf on Integrated Optics and Optical Fiber Communication), Hyatt Regency, San Francisco, Calif. INFORMATION: Barbara Hicks, Optical Society of America, 1816 Jefferson Place, NW, Washington, DC 20036. Tel: 202/223-8130

APR 27-30—National Design Engineering Show & ASME Conf, McCormick Pl, Chicago, Ill. INFORMATION: Banner & Greif, Ltd, 110 E 42nd St, New York, NY 10017. Tel: 212/687-7730

APR 28-30—Internat'l Telecommunications Forum, Concorde Lafayette Hotel, Paris, France. INFORMATION: Dusty Rhodes, Arthur D. Little Decision Resources, Acorn Park, Cambridge, MA 02140. Tel: 617/267-3456

APR 28-MAY 1—Society for Information Display Internat'l Sym, Grand Hyatt Hotel, New York, NY. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193/4 (1 to 5 pm)

MAY 4-7—NCC (National Computer Conf), McCormick Place, Chicago, Ill. INFORMATION: Gerard Chiffriller, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/558-3600

May 12-14—Internat'l Sym on Computer Architecture, Minneapolis, Minn. INFORMATION: Harry Hayman, Computer Architecture, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAY 19-21—INTELEC '81 (Internat'l Telecommunications Energy Conf), Royal Lancaster Hotel, London, England. INFORMATION: INTELEC '81 Secretariat, The Inst of Electrical Engineers, Savoy Pl, London WC2R OBL, England

JUNE 10-12—CONPAR '81 (Conf on Analysing Problem-Classes and Programming for Parallel Computing), Nurnberg, West Germany. INFORMATION: Wolfgang Handler, Immd, Universitat Erlangen-Nurnberg, Martensstrasse 3, D-8520 Erlangen, West Germany

SEMINARS

MAR 23-25—Error Correcting and Detecting Codes, Boston, Mass. INFORMATION: Hellman Assocs, 299 California Ave, Palo Alto, CA 94306. Tel: 415/328-4091

MAR-APR—Data Communications: An Introduction to Concepts and Systems; Advanced Concepts and Systems; AND Effective Network Design; AND Systems Analysis and Design: Concepts and Effective Practice AND Advanced Techniques, various dates and locations. INFORMATION: Datapro Research Corp, 1805 Underwood Blvd, Delran, NJ 08075. Tel: 609/764-0100

Announcements intended for publication in this department of *Computer Design* must be received at least two months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.

INTRODUCING

the DSD 880.

A DEC®-compatible disk system combining eight-inch Winchester and flexible disks.

For DEC users who need more capacity and performance than a dual RX02, the DSD 880 now offers a more cost effective alternative than a dual RL01.

- significantly lower initial and total life-cycle costs
- the reliability of a Winchester, with 7.5 Mbytes, emulating RL01
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- valuable saving in rack space (5¼" vs. 21" for dual RL01)
- unique "hyperdiagnostics" enabling fast and easy troubleshooting to the modular level
- built-in bootstrap eliminating the need for an expensive DEC bootstrap board and saving a backplane slot
- one half-quad backplane slot vs. two quad boards for the RLV11
- versatile interface card for easy integration with any LSI-11 backplane, unlike DEC's RLV11 interface that needs a special backplane and cannot be used with the VT 103 terminal

Compare for yourself and see why nothing compares to the DSD 880.

Data Systems

The Intelligent Alternative to DEC Disk Systems

To get more information on the DSD 880, call or write:

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TWX: 910-338-0249

Western Region Sales:
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Santa Clara, CA 95050
Tel: (408) 727-3163
TWX: 910-338-0249

Eastern Region Sales:
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Norwood, MA 02062
Tel: (617) 769-7620
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International Sales:

Australia: Melbourne (03) 543-2077, Sydney (02) 848-8533; Canada (416) 625-1907; Denmark 01/83 34 00; Finland 90/88 50 11; France 03/956 81 42; Israel 03/298783; Italy 02/4047648; Japan: Osaka (06)323-1707, Tokyo (03)345-1411; Netherlands 020/45 87 55; New Zealand 4/693-008; Norway 02/78 94 60; Sweden 08/38 03 70; Switzerland 01/730 48 48; United Kingdom 01/207-1717; West Germany and Austria (089) 1204-0.

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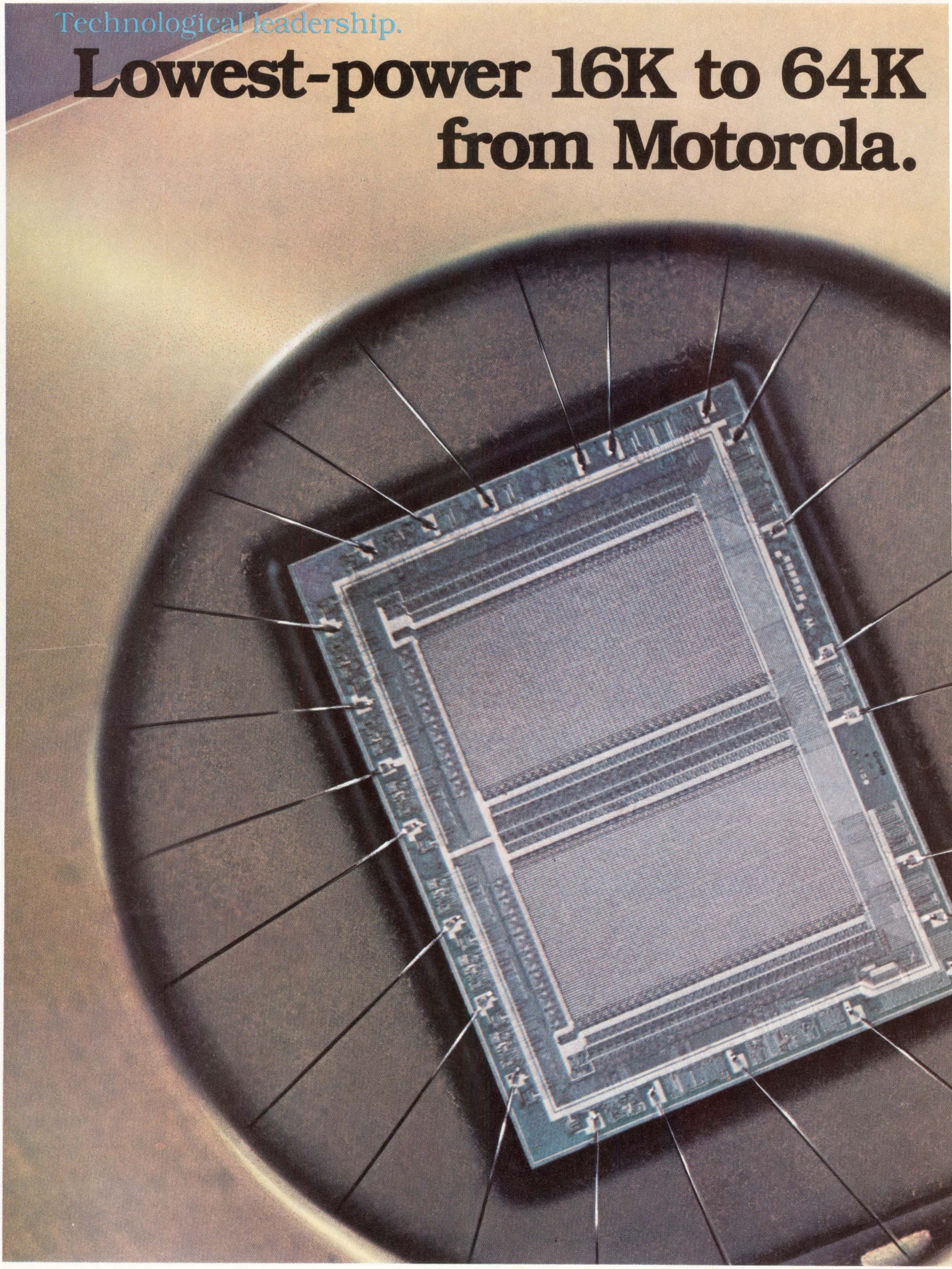
CIRCLE 8 ON INQUIRY CARD

Technological leadership.

Lowest-power 16K to 64K from Motorola.



5 V EPROMs Immediately available.

You'll find the ultra low-power 5 V EPROMs you're looking for in Motorola's comprehensive, quality-built 16K to 64K EPROM family.

That includes the MCM68764 and MCM68L764, far and away the lowest-power 5 V 64Ks available. The family also includes our MCM68766 and MCM68766-35 for those who need a 5V 64K with an extra-fast output-enable access time.

They're all available in volume from Motorola now.

These Motorola 5 V EPROMs are pin-compatible with the 8K through 64K industry-standard mask-programmable ROMs, right down to using the same 24-pin packaging. Even the 64Ks are "plug-in" replacements for the 24-pin industry-standard ROMs, as well as for smaller 5 V EPROMs. The 16K, 32K, and 64K EPROMs from Motorola all have JEDEC-approved standard pinouts.

Added attractions such as on-chip overvoltage protection circuitry help put these 5 V EPROMs in a class by themselves. The higher-performance versions are all ±10% supply devices.

Data retention in these EPROMs is superior, consistent with the high quality of product Motorola has been noted for since the 1950s. By superior data retention, we're talking about a failure rate of only 0.001% per 1000 hours.

The MCM68766 EPROM offers all the features and performance of Motorola's original ultra low-power 64Ks except power down. It has the same access time from address and an even faster 150 ns maximum output enable access time.

Order Motorola 5 V EPROMs now from your local Motorola sales office or authorized distributor. For additional information, use the coupon or write to Motorola Semiconductor Products Inc., Technical Information Center, P.O. Box 20912, Phoenix, AZ 85036.

Motorola's Comprehensive 5 V EPROM Family

Motorola Part Number	Access Time – ns	Max Active Current – mA	Max Standby Current – mA	5 V Supply Tolerance – %
16K EPROMs				
MCM2716	450	100	25	± 5
MCM27L16*	450	50	10	± 5
MCM2716-35	350	100	25	±10
MCM27L16-35*	350	50	10	±10
32K EPROMs				
MCM2532	450	100	25	± 5
MCM25L32*	450	50	10	± 5
MCM2532-35*	350	100	25	±10
MCM25L32-35*	350	50	10	±10
64K EPROMs				
MCM68764*	450	120	25	± 5
MCM68L764*	450	60	15	± 5
MCM68766	450(150[1])	160	–	± 5
MCM68766-35	350(150[1])	160	–	±10

*Lowest power in the industry [1]Access time from output enable

Industry-standard ROMs, 64K dynamic RAMs, fast static RAMs, and these leading 5 V EPROMs all point to one thing. Motorola has the MOS memories you need for

Innovative systems through silicon.

MOTOROLA INC.

TO: Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

Please send me information on 5 V EPROMs

80 CD 2/81

Name ____________________

Title ____________________ Tel.: (   ) ____________

Company ____________________

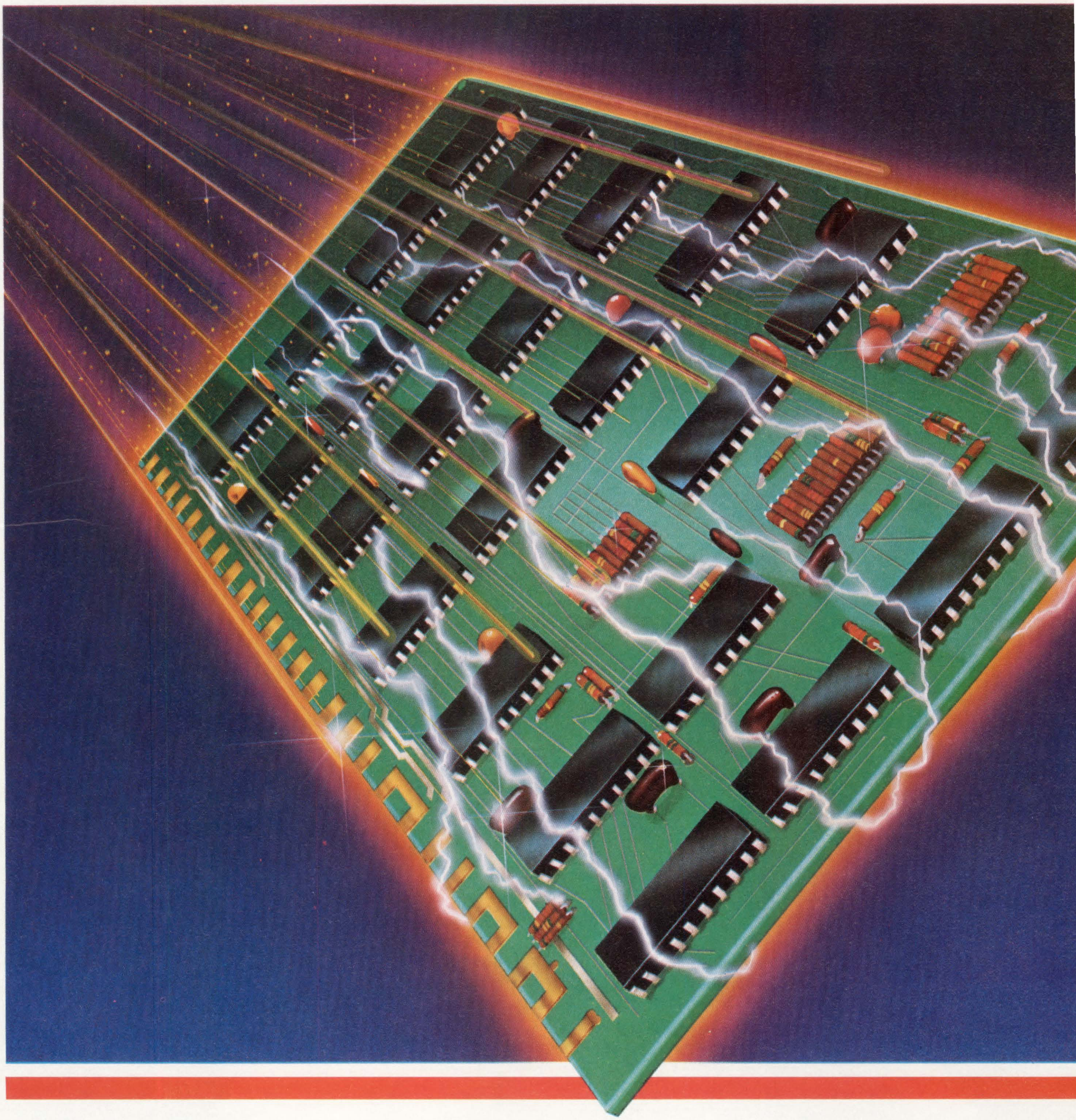
Address ____________________

City ____________________

State ____________________ ZIP ____________

FAIRCHILD

A Schlumberger Company



More of the fastest circuits

For high-speed and low-power requirements, nothing comes close to our FAST registers and multiplexers.

You've already heard about the exceptional performances of Fairchild's FAST latches, flip-flops and counters. Now, here are a few FAST facts on some of our other fine devices that you can use to upgrade your logic systems.

REGISTERS

74F194 4-Bit Universal Shift Register

Shift Frequency . . 150 MHz typ
Clock-to-Output Delay . . . . 4.0 ns typ
ICC . . . . 33 mA typ

The 74F194 is 50% faster than Schottky and requires 65% less power. It's currently available in a plastic or ceramic package. And we have three octal shift registers planned for the near future: the 74F299, 74F322 and 74F323.

MULTIPLEXERS

Data-to-Output Delay

74F153
Dual 4-input. . . . 5.0 ns typ
74F253
Dual 4-input with 3-state outputs . . . . 4.4 ns typ
74157
Quad 2-input . . . 4.5 ns typ
74F257
Quad 2-input with 3-state outputs . . . . 4.0 ns typ
74F158
Quad input with inverted outputs . . . . 2.9 ns typ

Select-to-Output Delay

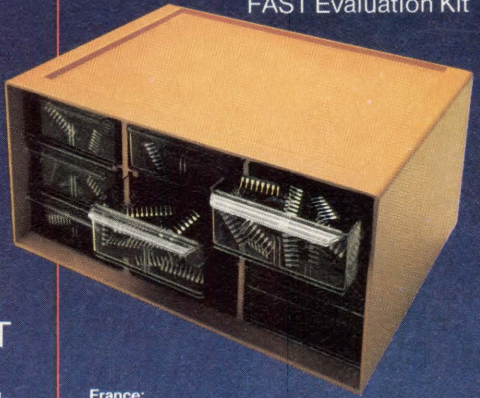
74F352/353
inverted versions of the 74F153/253. .6.3 ns typ

Our multiplexers are 30% faster than Schottky and require 70% less power.

Our total FAST offering.
There is a total of 30 FAST parts available now in production quantities, with additional functions coming soon. So you can upgrade your standard Schottky system or design a new system today, with Fairchild's high-speed, low-power, improved-density devices.

Make a thorough examination.
To check our parts out further, order our evaluation kit that contains 14 different 74F Series devices. A total of 72 parts. Contact your nearest Fairchild sales office or distributor for our kit or information about our product delivery dates. Or call or write FAST, Fairchild Semiconductor Products Group, P.O. Box 880A, Mountain View, CA 94042. Tel: (415) 962-FAST. TWX: 910-379-6435.

FAST Evaluation Kit



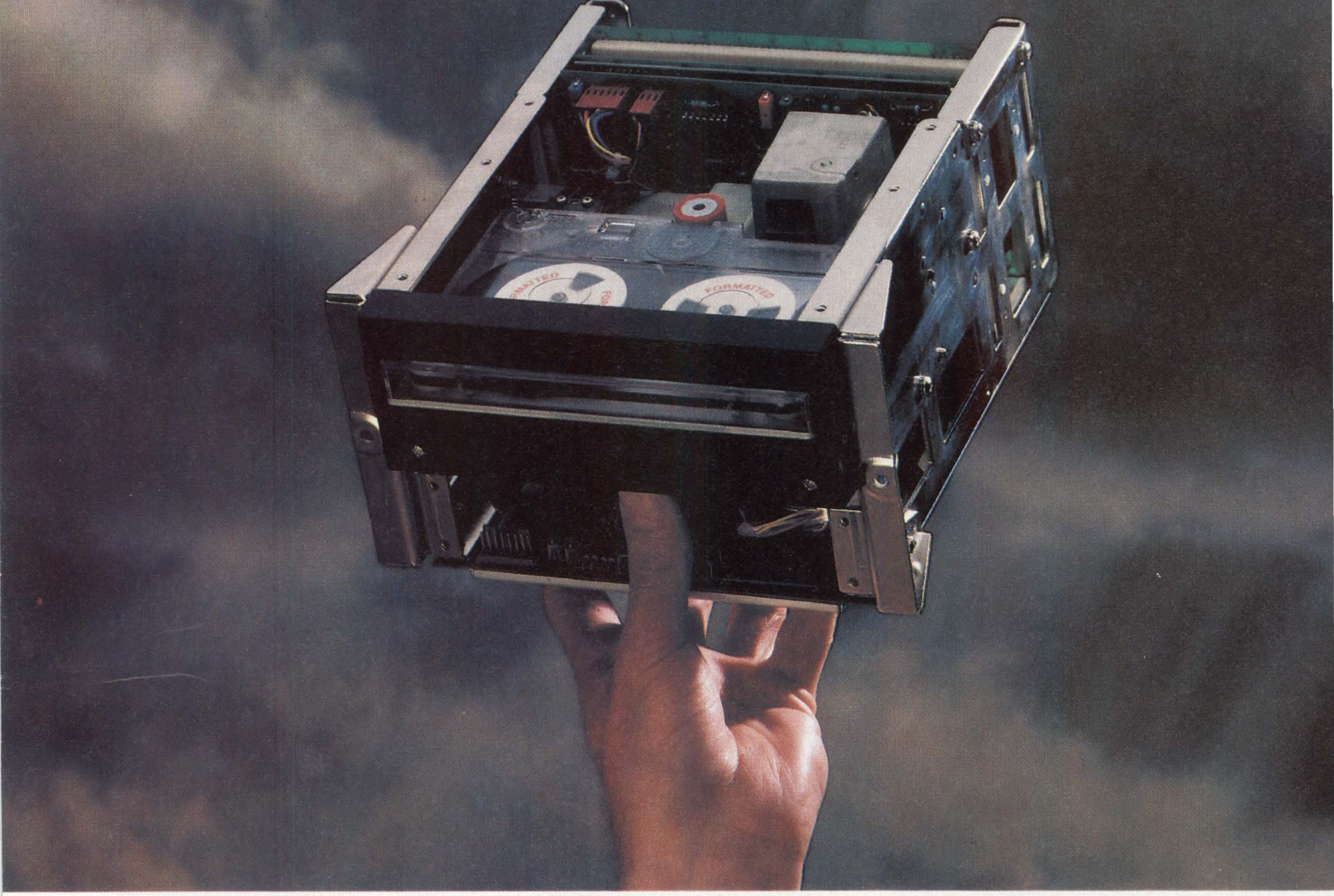
France: Fairchild Camera & Instrument S.A., 121 Ave. d'Italie, 75013 Paris. Tel: 331 584 55 66. Telex: 0042 200614. **Italy:** Fairchild Semiconduttori S.P.A., Viale Corsica 7, 20133 Milano. Tel: 02 296001-5. Telex: 843-330522. **Germany:** Fairchild Camera & Instrument (Deutschland) GmbH, 8046 Garching Hochbruck, Daimlerstr. 15, Munchen. Tel: 089 320031. Telex: 52 4831 fair d. **England:** Fairchild Camera & Instrument (UK) Ltd., 230 High St., Potters Bar, Hertfordshire EN6 5 BU. Tel: 0707 51111. Telex: 262835. **Sweden:** Fairchild Semiconductor AB, Svartengsgatan 6, S-11620 Stockholm. Tel: 8-449255. Telex: 17759. **Japan:** Fairchild Japan Corporation, Pola Bldg., 1-15-21 Shibuya, Shibuya-Ku, Tokyo 150. Tel: 03 400 8351. Telex: 2424173 (TFCTYO J). **Hong Kong:** Fairchild Semiconductor (HK) Ltd., 135 Hoi Bun Road, Kwun Tong, Kowloon. Tel: 3-440233. Telex: HX73531.

Fairchild Camera and Instrument Corp.

across the board.

CIRCLE 11 ON INQUIRY CARD

Never Before Has A Back-up System Been As Intelligent As The System It's Backing Up.

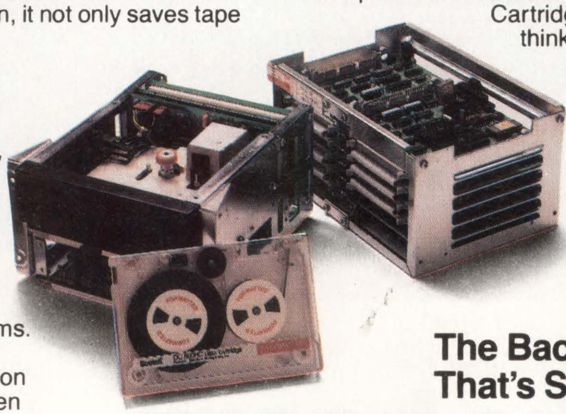


This is 3M's HCD-75 High Capacity Data Cartridge Drive. And the reason it's as intelligent as a computer is because it thinks like one.

You see, unlike other back-up systems, the HCD-75 is interfaced directly with the primary system by means of sophisticated, microprocessor electronics. When the host computer has data to feed, the HCD-75 starts automatically. When the host computer stops, it does too. And since the HCD-75 also positions to any location, it not only saves tape cost, but retrieval time as well.

Of course, the use of microprocessors allows the HCD-75 to perform a number of other time-saving functions, too. Like block replacement, so you can easily correct errors or change files which need updating. And fast random access, which makes it useful both as an I-O device or as a storage unit for low-usage files. All of which relieves the host computer from difficult timing and formatting problems.

What's more, the HCD-75 features state-of-the-art error detection and correction capabilities. Even when the system is off-line, self-test diagnostic routines monitor its performance. And, combined with each of its $32.50 high-capacity cartridges, the HCD-75 provides a full 67 megabytes of formatted user information (144 mbytes unformatted). So costly operator interventions are sharply reduced.



If you're looking for a reliable, cost-effective solution to the problem of disk back-up, the HCD-75 High Capacity Data Cartridge Drive is the system you should be thinking about.

Not only has a lot of thinking gone into it. But a lot of thinking comes out of it, too.

For more information, check the listing on the next page for the representative nearest you. Or write: Data Products Division/3M, Bldg. 223-5E/3M Center, St. Paul, MN 55144.

The Back-up System That's Suddenly Way Out Front.

LETTERS TO THE EDITOR

To the Editor:

While reading the Tech Note "Making PL/M Programs More Understandable" (by Douglas L. Abbott) in your Nov 1980 issue, I discovered what I believe to be a serious error.

On page 176, the author states, "DO UNTIL is identical to DO WHILE NOT." This is generally not true. The difference between DO UNTIL and DO WHILE involves the position of the test for condition.

A DO WHILE block tests for condition, executes the block (if true), and repeats. A DO UNTIL block executes the block, tests for condition, and repeats (if true). Analyzing these tests one can see that a DO WHILE block may never execute, whereas a DO UNTIL block will always execute at least once. It is clear that the DO UNTIL and DO WHILE structures *are* different; they may *not* be arbitrarily exchanged.

I hope that some means exists to rectify what could be a costly misdirection for many PL/M users.

John M. Pantone
National CSS, Inc
Wilton, Conn

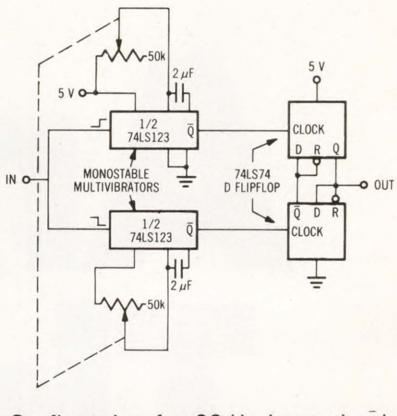
To the Editor:

The digital phase shifter presented by Mr Perry in the Nov 1980 *Computer Design* (p 199) has a couple of design flaws in the method for producing a phase shift replica of a digital input. Since the JK flipflop is negative-edge triggered only when an output of one monostable multivibrator falls while the other monostable output is zero, there will be a problem when the outputs of the monostables overlap. In this case the JK flipflop will sense only the trailing edge of just one of the multivibrators. Thus, it will constantly clock in the same value to the output of the JK flop.

Another possible problem occurs from the fact that the J or K input of the flop is in transition during the triggering of the flipflop. If the delay in the NOR gates is significant, or if the clocking threshold of the flipflop is at a low level, J and K could be settled at the low level by the time the flop is clocked. This would cause the Q output of the flop to remain at the low level.

A better and simpler design would be to have the outputs of the monostables clock separate flipflops as shown. A positive pulse at the top monostable input will cause a high state to be clocked to the Q output of the top D flipflop after a delay determined by the monostable. When the input pulse falls, the bottom monostable will trigger and clock a low state to the Q output of the bottom D flipflop after the same delay time and reset the Q output of the top flipflop, thus producing a delayed replica of the input.

Gordon H. Rettke
Teledyne Brown Engineering
Huntsville, Ala



Configuration for 20-Hz input signal. Positive phase shifts may be varied from 33 to 180° while negative phase shifts may be varied from −36 to −180° with R and C values shown

Letters to the Editor should be addressed:

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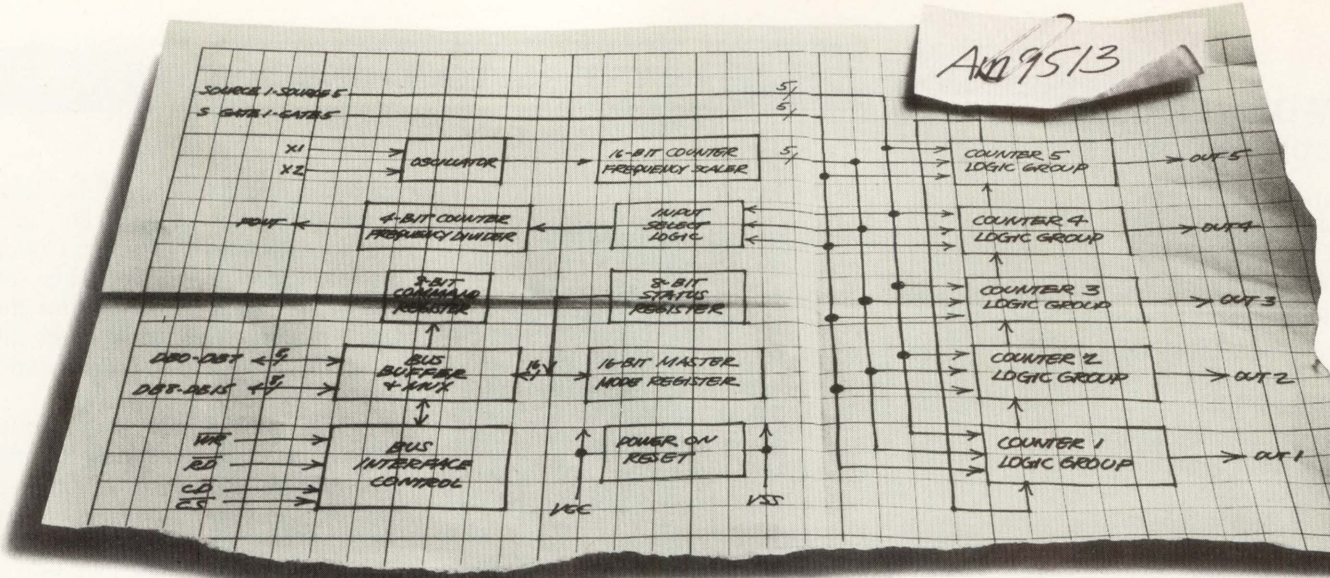

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Local Area Networks Overview—Part 1: Definitions and Attributes

J. Michael Kryskow
Gould Modicon, Haverhill St, Andover, MA 01810

C. Kenneth Miller
Concord Data Systems, Inc,
430 Marrett Rd, Lexington, MA 02173

Local area networking has been much in the news lately, with many companies and vendors scrambling for a place on the bandwagon. The recent combined efforts of Digital Equipment Corp, Intel, Xerox, and the IEEE to propose standards for local networks have been widely publicized. This overview presents a background on what a local area network is, how the concept came into being, current activities, and a prognosis for the future.

Until just recently a local area network was described as a communications network that covered a limited geographical area. The definition of "limited" is still a subject for debate. An early reference on the subject[1] defined a local network as one covering distances of 0.1 to 10 km with data rates of 0.1 to 10M bits/s. These numbers are arbitrary. In fact, the boundary between the high end of a local area network and the low end of a large topology network may be determined more by the data rate and organization of the network than by its geographical coverage.

Primary Attributes

Networks following the "local" definition are generally characterized by inexpensive transmission media and modems, high data rates, a high degree of interconnection between devices on the network with every node having the potential of communicating with every other node via the "link" protocol, and higher layer protocols similar to the International Standards Organization (ISO) Open System Interconnection (OSI) standards activities.

Although not a part of the definition of a local area network, a general characteristic is that such networks require no central node or processor. In fact, as the cost of computing power has continued to decrease, the trend to distributed processing has been the driving force in the development of local networks.

Another key attribute of local network structures is that every user generally listens to every transmission, whether addressed to him or not. Therefore there is a requirement to establish links between compatible nodes. This is the task of the link protocol. In addition, link protocol flow procedures must be created to provide the ability to define certain links as either allowable, or as under some form of restriction due to operational parameters or the state of the links. There may also be a requirement to be able to create new links dynamically across the network without manual intervention.

Some of the attributes of local area networks, such as high data rates and the ability of all system users to listen to all transmissions on the medium, have stimulated interest in extending the local area network concept to applications that cover wider geographical areas. Typically, these applications are for the future, and include "wired cities," large industrial complexes, oil and gas pipelines, and satellite communications. These potential areas differ from strictly local applications in that the transmission media and associated modems may be significantly more costly. However, these costs are generally less than those for data transmission over the telephone network. Also, the media in strictly local applications are usually privately owned by the users, whereas community antenna television (CATV) channels, satellites, and other broadband media would usually not be owned by the application users.

History of Local Area Networks

Research in these networks began in the early 1970s, spurred by increasing requirements for resource sharing in multiple processor environments. In many cases these requirements first appeared in universities or research laboratories; one such case is the OCTOPUS network at Lawrence Livermore Labs.[2] In the same time frame, research was being carried on in packet networks, and these have greatly influenced the evolution of the local area network concept. Ethernet, the first bus contention technology, appeared in the mid-1970s. It borrowed many of the techniques and characteristics of the ALOHA network,[3] a packet radio network developed at the University of Hawaii. Since then, networks using a number of topologies and protocols have been developed.[4] Currently, ambitious attempts are being made by the IEEE and other standards bodies to standardize on local network topologies, protocols, and modulation techniques while leaving room for future growth.

(continued on page 26)

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Local Area Network Technology Today: Media and Modulation Techniques

Traditionally, the voice telephone system has been the data transmission medium. Modems are required to convert digital data to an analog form suitable for transmission over the telephone network. This medium is characterized by being relatively inexpensive, and by the ability to cover great distances at data rates limited to 9600 bits/s or less. The standard medium in local area networks is completely opposite. It is inexpensive, and spans short distances at data rates as high as 10M bits/s.

In most local network applications up to now, twisted pair and coaxial cable have been the most commonly used transmission media. Coaxial cable of the type used in the CATV industry is probably the most popular because of its low cost and low losses at high frequencies. For example, RG-6 CATV cable typically costs less than $0.10/ft ($0.33/m) and has losses of 5.5 dB/1k ft (18.3 dB/km) at 10 MHz. Fiber optic cable has also been considered as a medium because of its high bandwidth and excellent isolation properties. However, at the present time it is generally more costly, more difficult to attach multiple devices to, and less reliable. For these reasons fiber optic cable has not been used to any great extent to date.

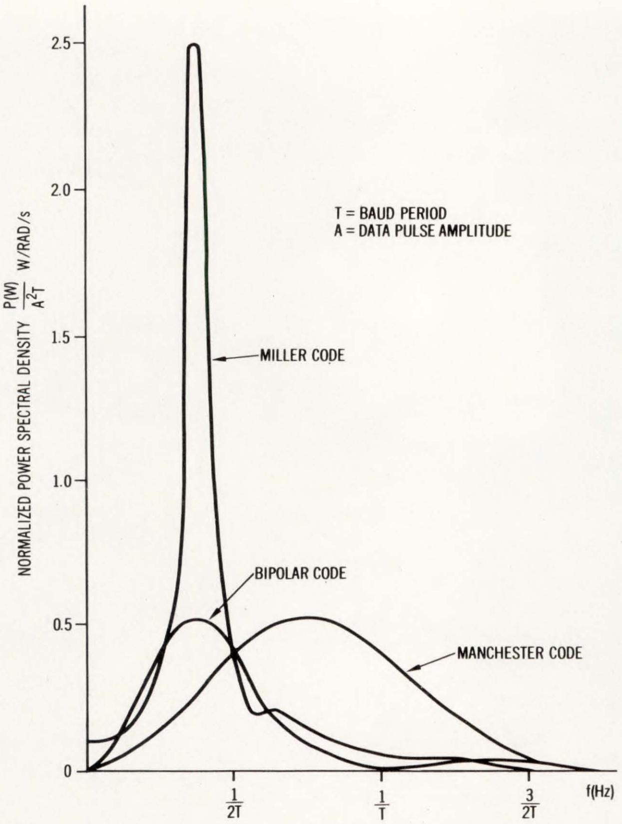

Fig 1 Code spectral occupancy. Bipolar, Miller, and Manchester characteristics are shown and random input data assumed

Modems used in cable systems can be relatively unsophisticated and hence inexpensive. The modems employed in limited bandwidth telephone line data transmission are often costly and complex, incorporating automatic equalization in order to pack as high a data rate as possible over one line to minimize line costs. In most cases the high cost of the modem, however, is offset by savings in line costs. In local area networks based on the coaxial cable medium, abundant inexpensive bandwidth allows the modem to be simple, economical, and have a high data rate. Baseband modulation techniques used for local area networks have no requirement for modulation on a carrier as do telephone line transmissions.

The most commonly used baseband modulation techniques are bipolar and its variants, Miller (delay) modulation, and Manchester (diphase) and its variants. Bipolar is a ternary code in the partial response family[5] and is currently used in the Bell system for T-carrier transmission at 1.544M bits/s or higher. Miller coding[6] is a binary code that has good spectral efficiency and has been used for baseband signaling over telephone company metallic pairs and for tape recording. Manchester coding[6] is a binary code commonly used because clocking information is present at each bit and implementation is simple. However, Manchester has the worst spectral efficiency of the three techniques (Fig 1). Because of the simplicity of its implementation, however, Manchester or one of its variants will likely emerge as the standard modulation technique for local cable applications.

Other cable media such as CATV distribution systems can be used to form a bus structured local area network. Costs involved in modems and medium, however, fall between those of a simple coaxial system and those of a telephone facility.

A CATV system operates under some constraints. It has a 5- to 300-MHz bandwidth. Available equipment is inherently unidirectional and is frequency divided into forward (>150 MHz) and backward (<150 MHz) channel groupings to allow bidirectional communications. The system requires a "head end" remodulator for converting frequency channels from one group to another, eg, to convert receive frequencies below 150 MHz to corresponding transmit frequencies above 150 MHz. The system uses rf modems operating in the two frequency bands. Commercially available rf modems with 19.2k-bit/s data rates use differential phase shift keying (DPSK) or frequency shift keying (FSK) modulation techniques and operate within a 100-kHz spectrum. Modems available for speeds above 1M bits/s typically use quadriphase shift keying (QPSK) or FSK modulation and operate within a 6-MHz spectrum. Currently, up to 1000 19.2k-bit/s or six 1M-bit/s channels, or some combination thereof, can exist on one cable system. Since the CATV system relies on a central head end remodulator

(continued on page 28)

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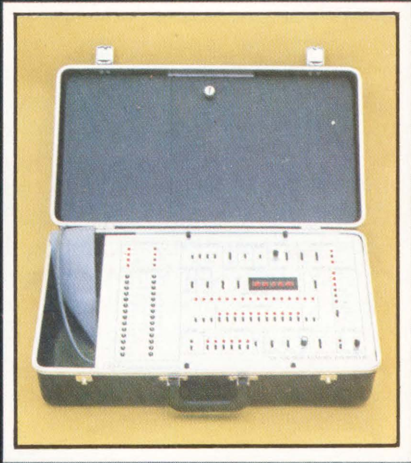

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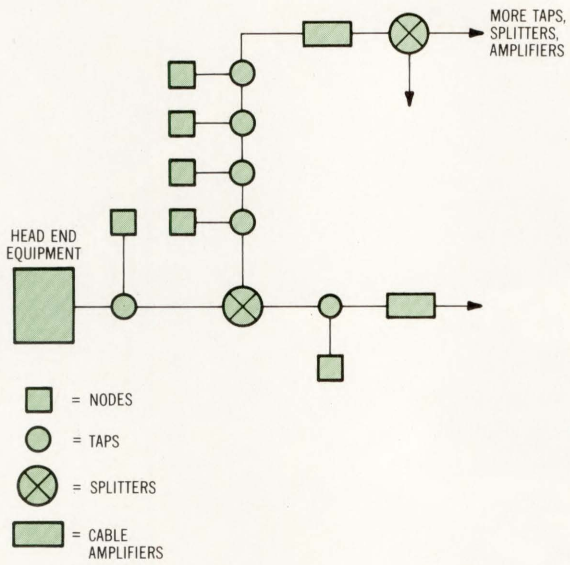

Fig 2 CATV topology. CATV systems are becoming popular for local data distribution because of excess "free" bandwidth where they also carry video and voice signals

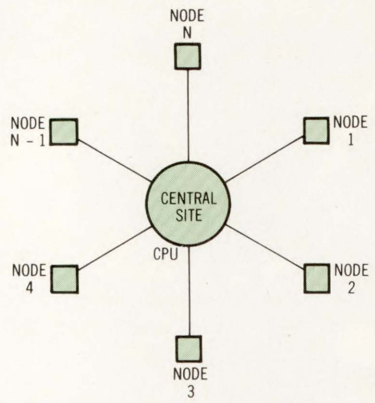

Fig 3 Star topology. Historically, most common data network topology, not decentralized

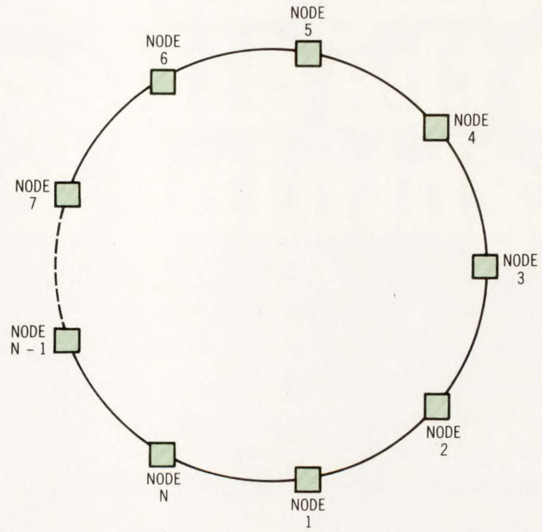

Fig 4 Ring topology. Failure at single node can bring network down unless some form of bypass is provided

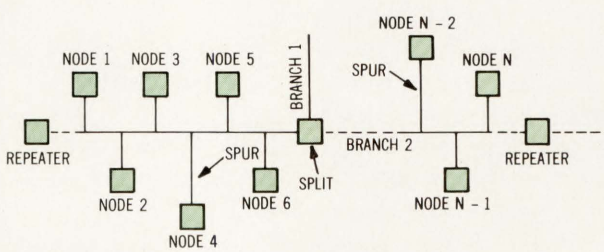

Fig 5 Bus topology. Ability to insert splitters and create spurs facilitates network reconfiguration

and needs a more complex modem, the increased expense makes it difficult to justify this medium for simple data distribution. However, if video and voice channels are also required, this medium becomes much more attractive. A typical CATV system topology is shown in Fig 2.

Leading Network Topologies and Access Methods

Although some early topologies such as in OCTOPUS were in a star configuration (Fig 3), most local area networks have evolved into either ring or bus configurations. Both are distributed decentralized topologies with distributed decentralized access techniques.

Ring Topology and Access Techniques—In the ring topology (Fig 4), messages are passed unidirectionally from node to node through some form of repeater until they reach their destination. No routing decisions are needed. Usually data are demodulated, buffered, and remodulated at each node on the ring.

Various flow control and access strategies have been used or proposed for inserting and removing messages from ring networks.[4] In the control token concept, a unique control token is passed around the ring. Any node may remove the token, insert a message, and append the token. Usually, the node is responsible for removing or "stripping" the message it inserted as it comes back around the ring.

(continued on page 32)

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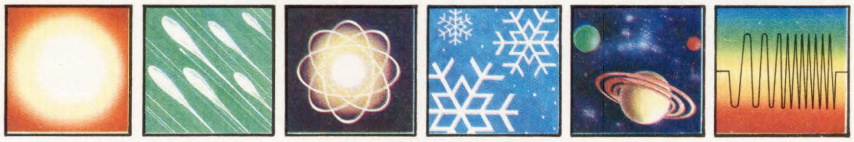

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With the message slot concept, sequences of bits sufficient to hold full messages are continually sent around the ring and may be full or empty. When any node receives an empty slot, it may mark it full and place a message in it. This strategy is generally not decentralized; an administration node is needed to initiate the slot pattern.

Register or buffer insertion is a third access strategy for ring networks. Here the message to be transmitted is loaded into a FIFO buffer. When the channel becomes idle or if the end of a message is detectable the loop is broken, the buffer is inserted, and the new message is sent onto the loop. Any incoming messages are shifted through the FIFO buffer until the original message returns, at which time the buffer is removed from the loop. At any node the node buffer must be removed before that node may transmit again. Various other criteria for deciding when to add or remove the buffer have been proposed.

Bus Topology and Access Techniques—A general bus topology is shown in Fig 5. All nodes have their receivers attached to the bus. Under normal conditions only the sending node's transmitter is attached to the bus and all nodes receive all messages essentially simultaneously, within the constraints of the propagation delay of the medium. As in ring networks, no routing decisions are needed.

The access strategy for inserting messages in bus networks may be either an asynchronous form of contention or self-synchronizing as in the ring topology (token passing). When contention is used as an access control mechanism two or more nodes may attempt to transmit at the same time, in which case a collision occurs. During the collision, the two or more messages become garbled and lost. The access control strategy usually requires that nodes be able to detect the possibility of a collision, wait (back off) for a random time so that there is a high probability that a collision will not reoccur, and then retransmit the message. Binary exponential backoff is a widely accepted strategy that uses an exponentially increasing slot selection based on the number of collisions detected. An improvement on this scheme, called carrier sense multiple access/collision detection (CSMA/CD), requires the node to listen before transmitting. Thus, if the medium is occupied with a signal, there will be no attempt to transmit. This is the strategy used in Ethernet. A problem in CSMA/CD is that collision detection can be difficult when there is a large difference in energy level between the transmit and receive signals. Various strategies have been proposed to overcome this limitation.

Synchronous techniques for access to a bus topology are similar to those used in a ring system. The most common are token access schemes. In a ring the token is present at only one user at a time and is passed through the devices on the ring. In bus topologies all users receive the transmitted signal "simultaneously" (with due respect to the worst case propagation delay of the bus). A token may pass from station to station in a logically predetermined manner, with the owner of the token having the sole right to communicate. In its simplest form each user must know who may send him messages (who gives him the token) and to whom he may send messages (to whom he next gives the token), ie, the exact logical equivalent to the ring topology.

Whether or not to distribute the function of building the token is a general problem in both ring and bus topologies. Mechanisms to have a distributed processing system tolerate errors or failures in the token list are also needed. Several techniques have been developed and are already in use in Japan and Europe.

Comparison of Ring and Bus Topologies

It is important to remember that ring and bus systems were developed for distributed processing applications where it is undesirable that the whole system could go down due to the failure of any single component. Therefore it is essential to look at both topologies from a reliability standpoint. Reliability has several aspects: performance in the presence of noise or other error producing conditions; performance in the presence of hard failures at the various nodes; or, provision for maximum performance in widely varying topologies.

As both ring and bus synchronous access methods require that control be sent around the network in the form of tokens or message slots, these schemes are inherently more vulnerable to errors than a bus using contention access. An access control message may be destroyed or mistaken, requiring a node to recreate a lost token or delete a duplicate. This is difficult to implement in a completely decentralized distributed system.

In a bus topology with contention access, errors could be mistakenly interpreted as collisions, causing system algorithm errors and leading to prolonged station access delay. Even if errors and collisions can be separated, the transmitting node doesn't know if the message was correctly received or garbled. A retransmission must be requested by the receiving node, or a link or virtual circuit timer must be implemented in order to detect the absence of a response in a reasonable time.

There are other distinguishing differences between bus token and contention schemes. In a token system errors are errors regardless of the distance and topology. In a contention system it is extremely difficult, if not impossible, to separate errors and collisions at large distances. A token system can accommodate priority schemes, while CSMA/CD systems, as currently defined, have no sense of priority.

Ring networks require active repeaters at each node either to regenerate the message transmitting on the ring or to remove an old message and insert a new one (or none). A failure at any one node could cause the whole network to go down. To solve this problem, relays are commonly used at each node to bypass a failure. There must be a means of detecting a repeater failure in order to determine when to activate the bypass relay. Also, in the worst case, two adjacent nodes may fail and be bypassed, tripling the normal transmission distance requirements. Thus, reliability considerations in the ring limit the maximum geographic scope of the network. In the case of open or shorted cables, the whole network can go down without the possibility of bypass.

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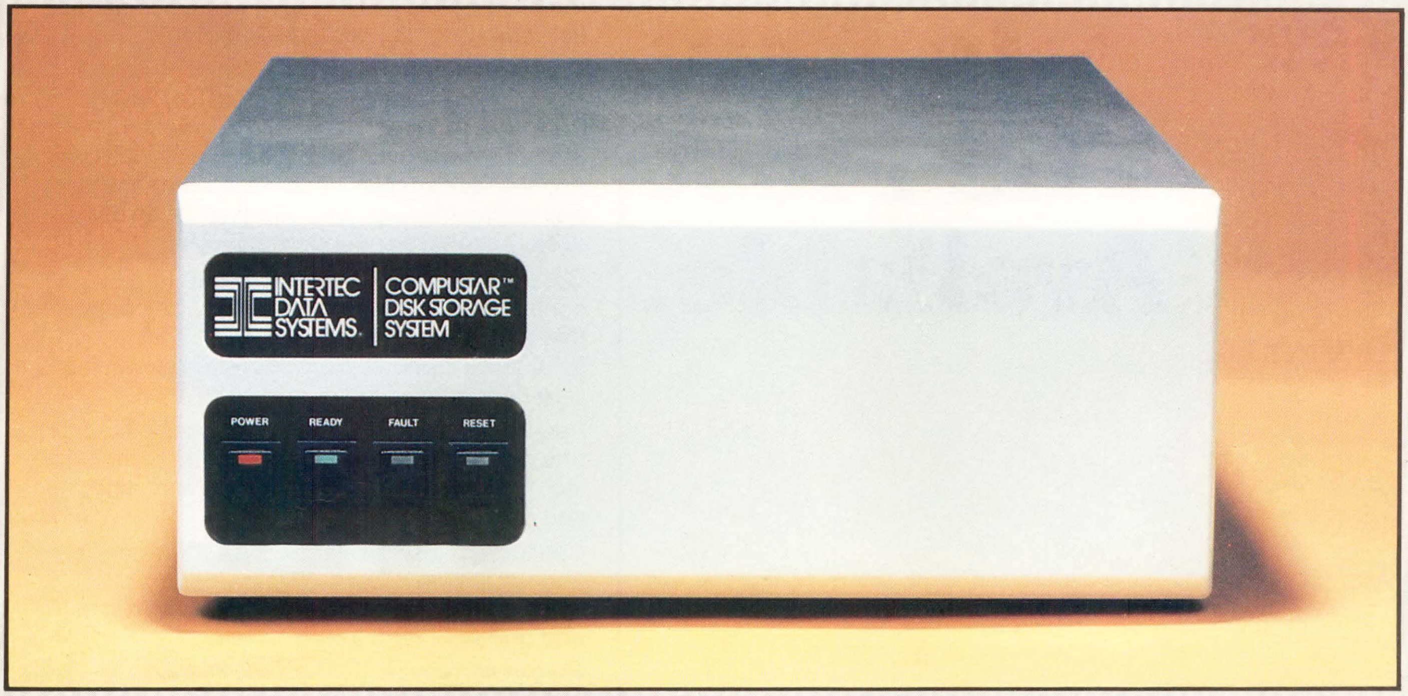

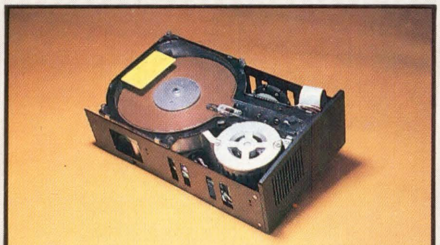
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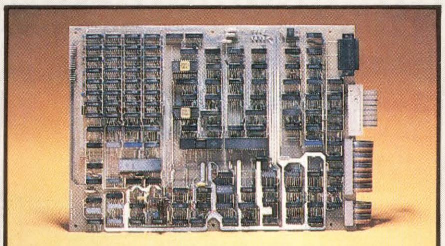
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CIRCLE 19 ON INQUIRY CARD

Bus networks do not normally require repeaters and so do not have as severe a reliability problem. Node failures must be such that the transmitter at each node is off and the receiver does not load down the medium. A transmitter getting stuck ON completely disables the network; some systems use watchdog timers to automatically shut off transmitters whose ON time is greater than normal. There is no limitation on transmission distances in bus networks due to reliability considerations since no active repeaters are required, and the maximum bus length is equal to the maximum transmission distance of the modems used.

Open or shorted cables in bus topologies split the network, but each segment can function if operation is possible without a termination at one end. However, in the higher data rate systems a shorted or open cable would probably cause the system to be severely degraded, if not inoperable.

Transmission Distance Limitations

In the ring topology, to allow for failure of any one node without bringing the network down, the distance limitation between nodes is determined by the worst case failure, generally assumed to be two segments in tandem. Thus, distance capability is strictly a function of media quality and modem performance. Since there are economic constraints on both, practical cost/performance tradeoffs dictate the ultimate result. In the case of rings, the maximum transmission distance is usually halved to determine the maximum node to node distance allowed.

In bus topologies when the medium is coaxial cable, each node may be in fact a spur, requiring a splitter where the spur attaches to the main bus. Splitters inherently have insertion loss, both in the direction of the spur and in the direction of the main bus (Fig 4). This loss reduces the distance capability of the system and makes the application of active splitters (transceivers) attractive in some cases. Also, if an Ethernet-like collision detection protocol is used, the maximum allowable receive signal level variation is typically less than 15 dB, greatly limiting the maximum end to end distance allowed. Additionally a large number of taps may have adverse effects on the impedance matching of the cable medium when operating at high data rates, causing further distance limitations. This factor has been instrumental in causing active taps to be used by the DEC/Intel/Xerox combine[7] for the new Ethernet system, that operates at 10M bits/s.

Physical Network Interface

In the ring topology the medium is broken at each node with one side connected to the receiver and the other to the transmitter. Adding nodes requires the inconvenience of physically cutting the cable. Ring networks are not easily reconfigurable without laying new cable or other media. The alternative is to install cable with many extra splices or junctions between nodes to accommodate later additions. However, this will increase cable losses and further reduce the maximum allowable separation.

On the other hand, bus networks do not require the node to be directly on the bus; it can be attached via a spur. Also, assuming a coaxial cable bus, the actual tap into the main bus has been accomplished by physically boring through the shield to connect a probe to the inner conductor. With this method it is unnecessary to break the cable. However, such connections may deteriorate with time, especially when operating at the higher data rates. Even if the bus must be broken to allow the insertion of a splitter, the ability to have spurs allows flexibility in reconfiguring the bus network.

Mixed Media and Access to Other Networks

When it is desirable to access other networks, either long haul or other local networks, access may be complicated by differing media, data rates, and/or protocols. These problems can be overcome by switches or gateways. These may be regenerative repeaters in the simplest form, or switches with buffers, or gateways with buffering and protocol conversion. In most instances local area network developments and standards rely on the higher level communication protocols such as the ISO Open Systems Interconnection[8] structure to implement network to network transfer.

Acknowledgment

The authors wish to thank Mr William D. Northam for his review and comments in the preparation of this article.

Next month's article will discuss the activities of various groups in attempting to develop local area network standards.

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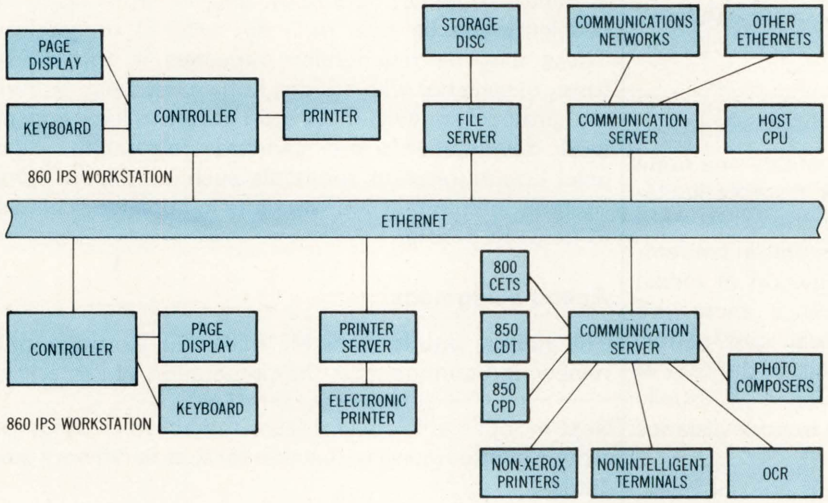
Business Information System Integrates Office Equipment Into Single Network



8000 Network System elements. All are connected to Ethernet local area network cable to link different types of office equipment into single integrated network

Designed for use with the Ethernet local area network (*Computer Design*, Mar 1980, p 42) 8000 network system (NS) includes an electronic file server that can store up to 10k pages of information, a print server comprising a compact electronic laser printer, and several communications servers that allow different types of office equipment, including competitive devices, to be linked into a single integrated network. The system, recently announced by Xerox Corp, Office Products Div, 1341 W Mockingbird Lane, Dallas, TX 75247, will use the company's 860 information processing system as the initial workstation.

The file server is the central point on the Ethernet for receiving, storing, and forwarding electronic mail. Three models are available, with capacities of 10M, 29M, or 50M bytes, respectively, allowing storage of approximately 1k, 4.5k, or 10k text pages. Each model includes a processor, floppy disc storage, and keyboard/display terminal. Analogous to a filing cabinet, the file server provides levels of storage like the file drawer, folder, and document categories of a conventional office filing system. The workstation operator can request a file drawer catalog that lists the file drawers on the workstation display. New files can be set up and identified, documents retrieved and displayed, and file contents changed or deleted. When a document is transferred from workstation floppy to file server hard disc, its name is added to the file catalog. For electronic mail storage and distribution, a post office catalog lists all mailbox names and also levels for mail folders and individual documents. The file server may also store various types of programs as well as conventional documents.

The system print server consists of a high speed control processor, floppy and hard disc storage, keyboard/display terminal, and the printer unit. In the latter device a laser scans digital fonts and creates images that are xerographically printed at a rate of 12 pp/min, equivalent to about 3k words/min of average double-spaced text. In normal operation, documents sent to the printer through Ethernet are stored on disc and printed in the order received.

Models 872 and 873 communications servers provide external interface to remote workstations, terminals, and host computers for communication with the Ethernet network. Model 872 provides for four, and 873 for eight outside connections. Data rates are up to 9600 bits/s. In conjunction with the other system servers, the communication servers allow communication with such company products as the 860 information processing system, and those from other manufacturers using TTY or IBM 2770, 2780, or 3270 protocols.

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Ideal for new 10-bit DAC designs as well as old AD7520 sockets, the AD7533 is flexible enough to interface to TTL or CMOS, operate on a +5V to +15V power supply, and provide binary scaling for reference inputs of either positive or negative polarity. You can even use it with AC references.

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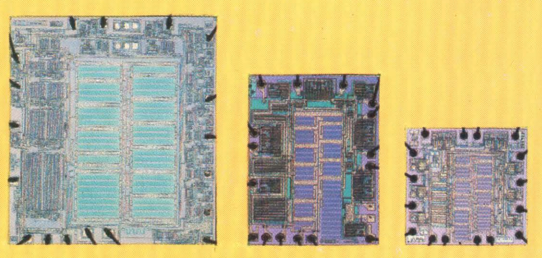
The AD7533 is a full four-quadrant multiplying DAC manufactured using our improved, smaller geometry, thin-film-on silicon CMOS wafer fabrication process. This means lower output capacitance for higher speed. It also means we can now guarantee ±0.05% (±½ LSB) linearity referred to the endpoints. And since the AD7533 is latch-up proof, no protection Schottky diodes are required on the outputs.

THE SMALLEST CHIP SIZE MEANS THE LOWEST PRICE.

By scaling the FET and resistor geometries, we were able to make our new AD7533 chip significantly smaller than our old AD7520. And our old AD7520 chip was already smaller than the competition's. The smaller the chip, the higher the yield; the higher the yield, the lower the price.



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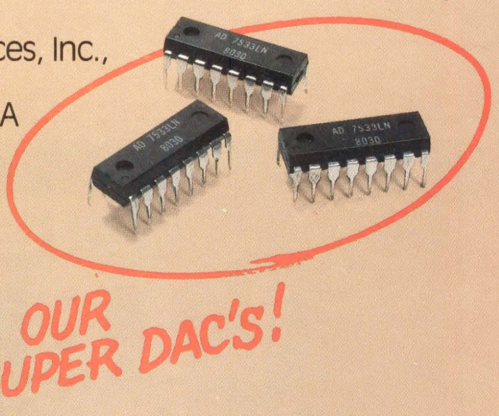

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CIRCLE 22 ON INQUIRY CARD

Wideband Fiber Optic Receivers Operate at 0.1M to 50M Bits/s

Fiber optic receivers series ORX5000 come in two versions, having either PIN or APD detectors, and can operate at 50M bits/s (NRZ) with a BER of 10^{-9} or better. Sensitivity is -27 dBm for the PIN module, and -41 dBm for the APD. The receivers have been developed by Optical Information Systems, 350 Executive Blvd, Elmsford, NY 10523.

Voltage requirements for the PIN versions are ± 10 to ± 15 Vdc and 45 Vdc, and for the APD unit ± 10 to ± 15 Vdc and 300 Vdc. Both fully shielded receivers have onboard voltage regulation, line filters, bias decoupling, and auxiliary analog output, useful in implementing clock recovery circuitry.

The modules plug into standard 44-pin edge-connected PC cards. Optical input is through an Amphenol 906 connector and standard level Schottky TTL output is available at the edge connector.

Circle 322 on Inquiry Card

60- and 240-Channel Units Expand Family of Intelligent Multiplexers

The data concentration exchange (DCX) family of intelligent multiplexers from Rixon Inc, 2120 Industrial Pkwy, Silver Spring, MD 20904, has been augmented by two units. DCX836 point to point statistical multiplexer provides compacted error free transmission of up to 60 asynchronous channels with 144.2k-bit/s aggregate rate over a single composite 19.2k-bit/s link. Network multiplexer DCX840 offers the same transmission characteristics but handles up to 240 asynchronous channels over as many as 12 composite links. Aggregate data rates are input, 500k, and output, 230.4k bits/s.

The network multiplexer provides centralized control and fault isolation functions using a mapping and test panel that allows network maps or configurations to be created and rapidly modified. Two different network maps can be stored and interchanged by a few keystrokes to change from daytime to nighttime operation. In the event of a fault, each network node can be accessed and the multiplexer's test microprocessor instructed to enter a test routine to determine whether the fault is in the line, multiplexer, or modem. DDD backup can be used if the node cannot be accessed through the network.

Both models are upwardly compatible and offer unrestricted intermix of speeds and codes, error free transmission, flyback buffering, automatic baud rate detection, and terminal flow control. Both are available in standalone or rack-mount configurations.

Circle 323 on Inquiry Card

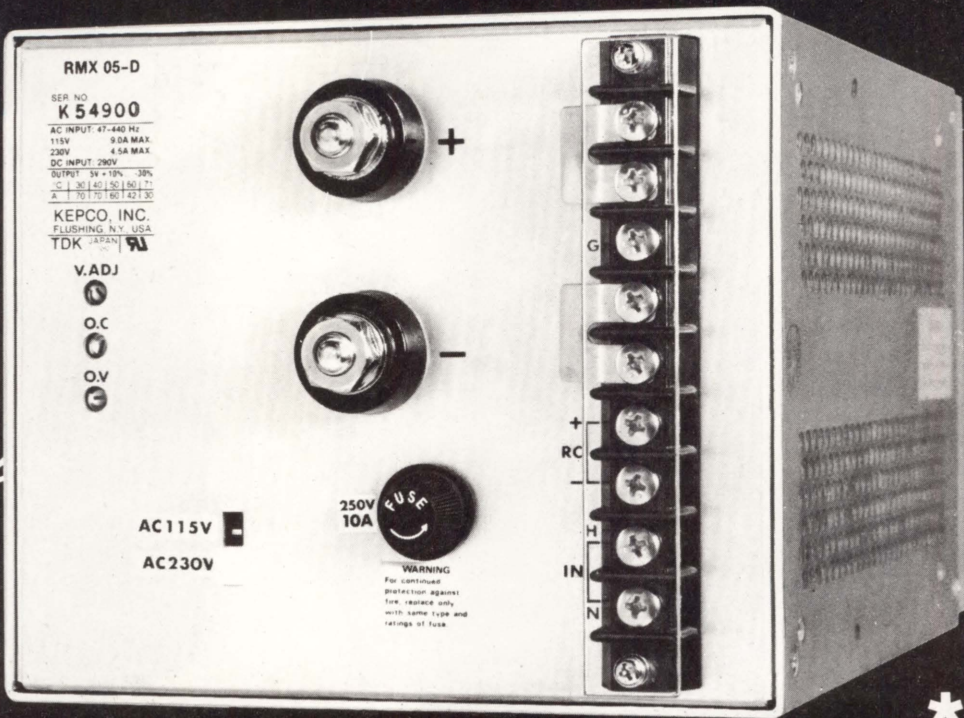
µ-Law Codec Has Transmit, Receive Filters On Single Chip

Said to be the first silicon single chip per channel codec in the world, CMOS S3505 combines encoder, decoder, and input/output filters. It was developed by American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051.

The device meets or exceeds AT&T D3 and CCITT G.711 and G.733 specifications. It handles serial data rates from 64k to 2.1M bits/s at a nominal 8-kHz sampling rate. A switched capacitor circuit design supplies 80-dB separation between transmit and receive filter sections to suppress crosstalk. Anti-aliasing prevents distortion from affecting transmit filters. Idle channel noise is 14 to 17 dBrnCO. Absence of both transmit and receive strobes causes automatic power shutdown.

Circle 324 on Inquiry Card

you gotta read the label



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. . . this symbol means that these fine Kepco/TDK Switching Power Supplies have been submitted to the inspection of Underwriters Laboratory, have been tested, have passed and are listed! They have also been certified by CSA, the Canadian Standards Association.

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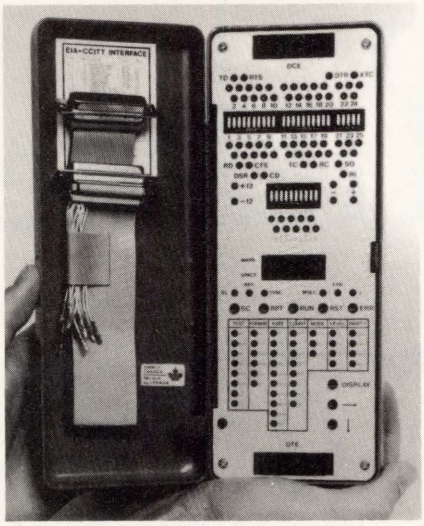
CIRCLE 24 ON INQUIRY CARD

Handheld Test Set Analyzes Total Data Network Performance



Portable SUPERTEST set. Complete RS-232-C interface breakout box allows cross-patching and signal interconnection in addition to normal monitoring functions. In monitor mode, device is transparent to interface

Portable microprocessor based test set SUPERTEST can diagnose faulty network elements and also analyze total data network performance. A programmable cursor feature enables over 100k internal configurations. The device, developed by Navtel Ltd, 8481 Keele St, Unit 12A, Concord, Ontario L4K 1B1, Canada, may also be configured for DTE or DCE simulation.

Eight messages, including MARK, SPACE, alternate MARK-SPACE, Fox, and 63-, 511-, 2047-, and 4095-bit pseudorandom word patterns, can be transmitted. Nine speeds cover the popular range from 75 to 19.2k bits/s, and an OPT position may be user specified to 200, 134.5, 600, 1800, or 56k bits/s. Transmission can be synchronous or asynchronous, with programmable number of start and stop bits, 5-, 6-, 7-, or 8-bit character levels, and odd, even, mark, or no parity.

The test set can perform BERT/BLERT analysis; errors are counted, displayed, and can also be inserted in bits or blocks up to 999 with overflow indication. Block test lengths may be selected from 1 to 10^6 blocks plus continuous. TON or TOFF modes allow signal acknowledgment delay measurement. TON mode measures time delay between RTS spacing of any other signal on the interface, while TOFF measures delay between RTS marking and the subsequent marking of any selected signal on the interface. A repeat feature allows dynamic testing and fault isolation of such modem functions as automatic equalization, receive clock synchronization, receive carrier recovery, agc circuit performance, and initial recovery of received data.

The self-contained unit includes an interface cable and a set of breakout patch cords, and weighs less than 1 kg. It is powered by internal nicad batteries or from the ac recharger supplied with the set. A display defeat switch extends battery life on long test runs.

Circle 325 on Inquiry Card

X.25 Network Front End Package for PDP-11s Supports 32 Terminals

A microprocessor based front end package allows PDP-11 users to interface with packet-switched networks that conform to CCITT recommendation X.25. IF-11/X.25 package, from Associated Computer Consultants, 228 E Cota St, Santa Barbara, CA 93101, supports X.25 protocol levels 1, 2, and 3, and has been certified for use on Tymnet and Telenet in the U.S. with forthcoming use on Datapac in Canada and PSS in the U.K.

The complete package plugs into two hex slots in the PDP-11 backplane. It transfers most of the X.25 processing load from the PDP-11 to the front end. The multichannel driver (MCD) and its microprocessor counterpart multichannel executive (MCX) make the package appear as a peripheral device controller with 66 multiple device units. These units, however, are really logic channels, two of which are reserved for supervisory link control functions. The remaining 64 channels are paired and provide up to 32 dynamically mapped full-duplex virtual circuits.

While the front end package performs all three levels of X.25 functions, it does not serve end to end requirements. For this, users may either provide their own PDP-11 user software or adopt the company's User Mode X.29 software package. This package resides entirely in the PDP-11 and conforms to CCITT recommendation X.29. When used in conjunction with the front end package, the software allows up to 32 independent user terminals to access the network simultaneously, and the entire X.25 network becomes transparent. Version 3.2 of the RSX-11M operating system is required in this instance.

Circle 326 on Inquiry Card

LSI Modem Modules for Data Communications Operate at 300 and 1200 Baud

Multicapability modems operating at 0 to 1200 baud are implemented with custom LSI chips into single 2.25 x 2.75" (5.6 x 7-cm) modules that can be mounted on PC boards or any flat surface inside most computers or terminals. They can be used as building blocks for communication on a variety of networks at various baud rates.

Seven functional modules have been announced by Novation Inc, 18664 Oxnard St, Tarzana, CA 91356. They can be mounted singly or in any combination to provide the following range of capabilities: 300-baud Bell 103 compatible or CCITT V.21 compatible unit with full- or half-duplex, answer and originate, and self-test; a 1200-baud module with 2-wire half-duplex and 4-wire full-duplex capability; a dual 1200/300-baud 103/102 compatible module; a viewdata module offering CCITT V.23 compatibility with 1200-baud receive mode and 75-baud reverse channel; a "deaf" modem module providing interface with the deaf TTY network as well as 103 answer/originate; and a phone line interface (PLI) featuring auto or manual answer, pulse dialing control, multitiming functions, and line busy with solid state holding functions. The PLI is registered for direct connection to the telephone network.

The modules are enclosed in a plastic case and can be secured after mounting by a hold-down strap or snap-on clips anchored to the circuit board.

Circle 327 on Inquiry Card

CIRCLE 26 ON INQUIRY CARD


JAPAN 082 S
HM6147P-3
JAPAN 044 S
HM6147P
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CC BRIEFS

Low Speed Coupler Modem Offers Increased Data Throughput—Acoustic coupler and direct-connect modem AJ 347 provides 0-to 450-bit/s data rates as opposed to the 300-bit/s couplers conventionally used in low speed applications. It operates full-duplex asynchronous and is fully Bell 103/113 compatible. The unit, from Anderson Jacobson, Inc, 521 Charcot Ave, San Jose, CA 95131, can originate and manually or automatically answer calls. It can be interfaced to any RS-232 or 20-mA TTY terminal and communicate over ordinary telephone or 2-wire leased lines. Quartz crystal control of the unit's transmitter provides for long term accuracy.
Circle 328 on Inquiry Card

Device Substitutes for Modems and Data Sets—Economical and space saving ME 922 dual-active modem eliminator permits direct interconnection of two business machines at EIA levels. The module incorporates two independent channels, usable for either synchronous or asynchronous applications. It generates and accepts data, timing, and control signals to emulate, though flexible strap option, the action for a pair of modems. The eliminator, a product of Gandalf Data, Inc, 1019 S Noel, Wheeling, IL 60090, operates within the limits of EIA RS-232-C and CCITT V.24. An internal crystal clock is included for synchronous applications, as are carrier and data status indicators for each channel.
Circle 329 on Inquiry Card

Multimodems Operate Over Any VF Circuit—Four-channel 2400-bit/s modem configuration GDCS 1050 operates over any VF circuit within the parameters of a CCITT data VF channel, including a tandem LOS microwave/FDM channel. The four-modem configuration has been introduced by General DataComm Systems Inc, 100 Parkway Drive S, Hauppauge, NY 11787, the military/government subsidiary of General DataComm Industries, Inc of Danbury, Conn. Each of the four modems has integral test capability for fault detection in the modem card, input equipment, or VF channel, and each has its own power supply. The four channels require less than 75 W input power. The modems are mounted in a 19" (48-cm) rack configuration with a front panel space of 11.125 x 5.25 x 9.5" (28.3 x 13.3 x 14 cm) available for insertion of ancillary functional circuitry.
Circle 330 on Inquiry Card

Network Processor Supports 125 Ports—System 355 network processor, designed for use in medium to large private networks, allows asynchronous terminals to access any host computer anywhere in the network. It also can support up to 125 ports, of which 62 can be high speed synchronous trunk links. Features include port contention, unlimited routing, X.25 support, and extensive network management tools. The processor, from Digital Communications Associates, Inc, 135 Technology Park, Norcross, GA 30092, can be used in point to point statistical, multipoint, and full-function multinode multiplexing applications.
Circle 331 on Inquiry Card

Device Converts RS-232 Interface to Current Loop—Available in self-powered standalone or in rack mountable multicircuit versions, universal RS-232 to current loop data converter has been developed by Dataprobe Inc, 110 W Palisades Blvd, Palisades Park, NJ 07650. It features half- or full-duplex operation, internal or external current loop supply, 20- or 60-mA operation, selectable RS-232 control signals, and LED indicators for receive and transmit signals. Send/receive leads on the RS-232 side of the interface are switchable to allow the device to be connected to either a terminal or modem.
Circle 332 on Inquiry Card

Modem Operates at 300 and 1200 Bits/s—FCC-registered MT212A is Bell 212A compatible and operates full-duplex over dial-up lines at both 300 and 1200 bits/s. Asynchronous or synchronous operation is selectable in the 1200-bit/s mode. The modem, from Multi-Tech Systems, Inc, 83 Second Ave SE, New Brighton, MN 55112, is available in both standalone and rackmount versions. Originate and automatic answer capabilities are provided. A push-button switch on the modem chassis transfers voice to data; 502 exclusion-key phones and adapters are not required. In originating applications, the telephone set can be connected directly to the modem, which can be connected to the phone line via either RJ11C, RJ11W, or RJ45S modular connectors.
Circle 333 on Inquiry Card □

Things are bigger in Texas.

But bigger doesn't necessarily mean better. Take printers, for instance. The 310 Ballistic™ Printer from Lear Siegler doesn't have a price tag nearly as big as the Texas Instruments 820. And though we're not the big guys in the printer field, we can offer you big enough reasons to buy our 310 Ballistic Printer. And that's a matter of no small importance.

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You can see for yourself. Right down the line. When placed up against the big competition, the 310 Ballistic Printer comes out ahead.

First off, at 180 cps and with space/blank compression, you get higher throughput for higher volume data flow.

You also get a nine-wire head with a 9 high by 7 wide dot matrix. Which gives you true lower case descenders plus underlining.

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THE 310 BALLISTIC PRINTER FITS RIGHT IN.

Our printer is totally compatible with all Lear Siegler terminals or with any RS-232C interface. It fits anyplace you have a CRT terminal or small business minicomputer system.

Feature	LSI 310	TI 820RO
Speed	180 cps	150 cps
Dot Matrix	9-wire head (9 hi x 7 wide)	7-wire head (7 hi x 9 wide)
Lower Case	Standard, with descenders and underlining	Standard, but no descenders or underlining
Buffer	512 expands to 2048	Fixed 1280
Space/Blank Compression	Yes	No
Interfaces	Serial and parallel	Serial only (parallel not available)
Current Loop	Standard	Optional
Forms Control	14 settings standard	Optional
Elongated character sets	Standard	Optional
Price	Base Price $2045 Expanded buffer 100 Price as shown $2145	Base Price $1995 Options 310 Price as shown $2305

The 310 Ballistic Printer is capable of satisfying low-speed day-to-day requirements and is economical enough to handle those high-speed tab runs, too. With the patented Ballistic printhead and 100% duty cycle, no job is too difficult.

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CIRCLE 29 ON INQUIRY CARD

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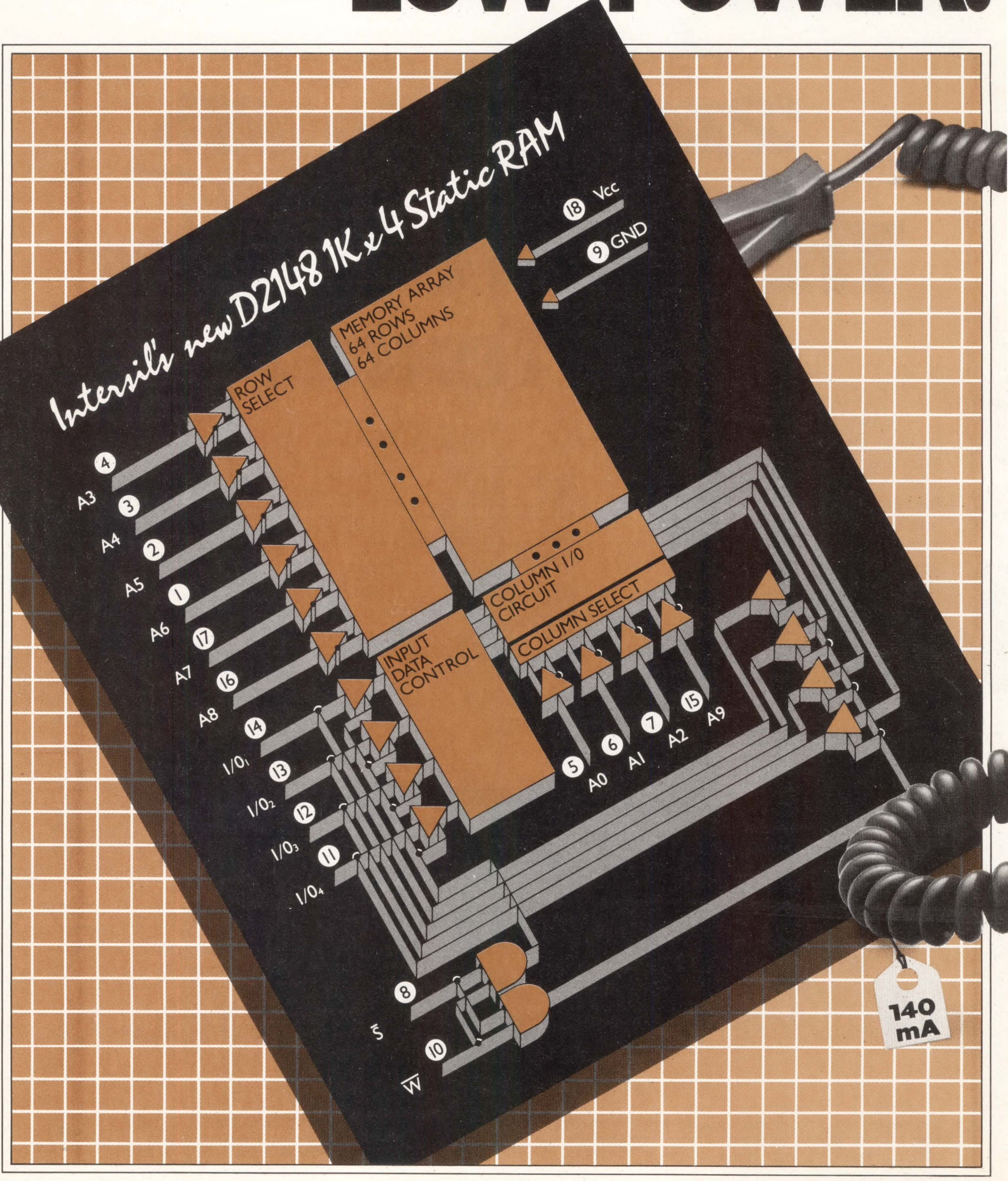

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Yes, it's the industry standard. Yes, it has multiple-source availability.

Yes, it's pin-for-pin compatible with other 2148s and 2114s.

But Intersil offers it in low-power. With 140mA active current and 30mA standby. Which is a full 20% under the competition's standard part. And even lower power versions are available for special applications.

For high-speed applications.

Finally there's an industry standard 1Kx4 static RAM to go with high-speed microprocessors. Or into cache or scratchpad memory. Or high-speed main memory. Or real-time-access data storage systems.

Intersil's Fast 4K RAMs

	Access Time	Operating Power
D2148 (1Kx4)	70ns	140mA
D2148-3 (1Kx4)	55ns	140mA
D2147 (4Kx1)	70ns	160mA
D2147L (4Kx1)	70ns	140mA
D2147-3 (4Kx1)	55ns	180mA

Intersil's new 2148s have all the speed you need: a 70ns standard part plus a 55ns high-speed version.

1Kx4 or 4Kx1—take your choice.

Either way you want it, Intersil has RAMs for you. And since our single-layer poly HMOS is producing speeds competitive with bipolar, we're continuing to expand the family. Right now there are plenty of fast Intersil memories to choose from. In the near future, there'll be even more.

Delivery: now.

Yes, we're very competitive on price. And as for delivery, it's immediate. Off the shelf. Which is pretty hard to beat.

So if you're in the market for a fast, low-power 1Kx4—wait no longer. Get a sample by calling your local Intersil sales office. Or by writing them on your company letterhead. To get literature, just send in the coupon. Then start designing faster memories.

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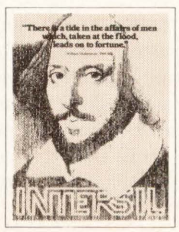
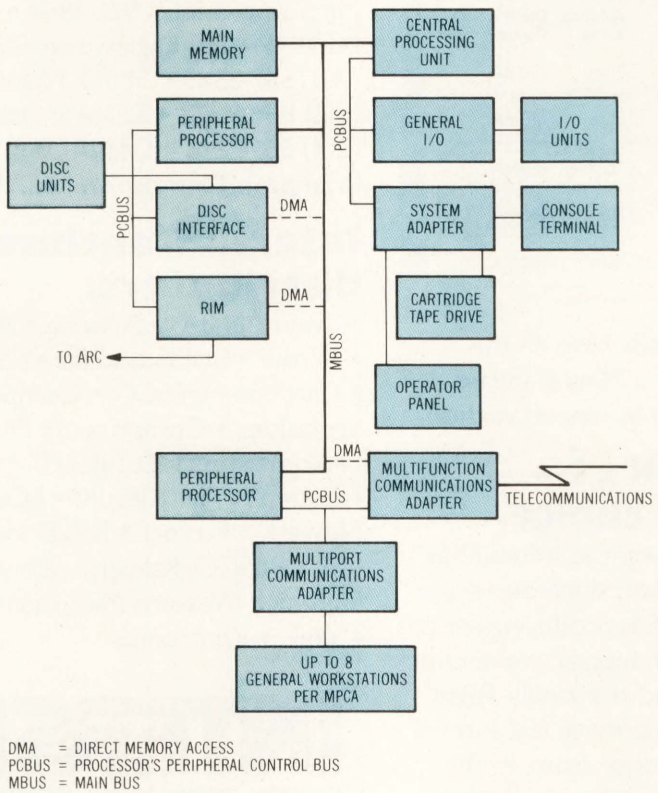


☐ Also, please send me one of your Shakespeare posters from your "famous quotations" ad series.

Multiprocessor Architecture Extends Resource Sharing Within Network



For use as standalone, data resource, or applications processor, Datapoint's 8800 incorporates multiprocessor architecture. Central processor and main memory are supported by peripheral processors all linked by high speed internal bus and DMA channel

A 16-bit multiprocessor machine with up to 1M bytes of memory, the 8800 runs under the RMS (Resource Management System) operating software to give users a shared resource operating approach to resource allocation. Introduced by Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, the combination is geared to provide economical incremental growth without constant reprogramming, and to allow efficient control of peripheral devices by giving users complete software control over configuration and reconfiguration of the network.

System architecture consists of a 16-bit central processor and main memory supported by peripheral processors all linked by a high speed internal bus and direct memory access. This architecture allows the peripheral processors, with separate processing power and up to 64k bytes of independent memory, to relieve the CPU of the task of controlling peripheral devices.

The 8800 is designed to be configured to fit specific user needs. The chassis has 20 circuit board slots. The basic operating configuration requires three slots for memory, three for the central processor, and two for interfacing. The other 12 are available for memory expansion boards, a disc controller, multiport communication adapters for workstation interfacing, multifunction telecommunication adapters, peripheral processors, or RIM communication adapters used to interface to ARC networks. The two system interface boards include an interface module to attach the control terminal and a Datapoint "5500" standard external I/O adapter used to attach printers and tape drives to the system.

The computer can be used as a standalone processor, designated an 8860. In this case it can support a local network of "nonintelligent" terminals (which will execute multiple languages and functions), a disc storage unit, and other peripheral devices.

If used as a data resource processor, designated an 8840, it can, in addition to other tasks, support a minimum of 202M bytes of online disc storage, 67M bytes of which would be on a removable disc, facilitating the production of file "backups." Disc capacity can be expanded with an additional six drives of 135M bytes each, bringing the total to over 1G bytes of online storage. While operating as a data resource processor, the system can additionally perform concurrent tasks such as communications and print spooling.

As an applications processor, designated an 8830, the computer comes

(continued on page 56)

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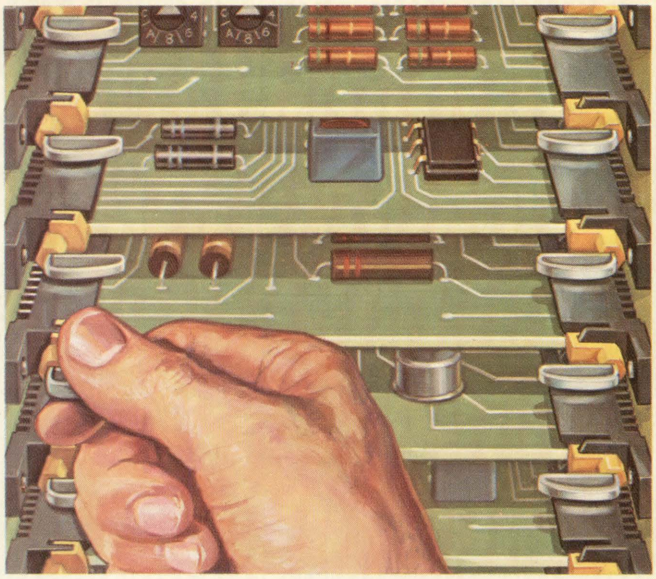

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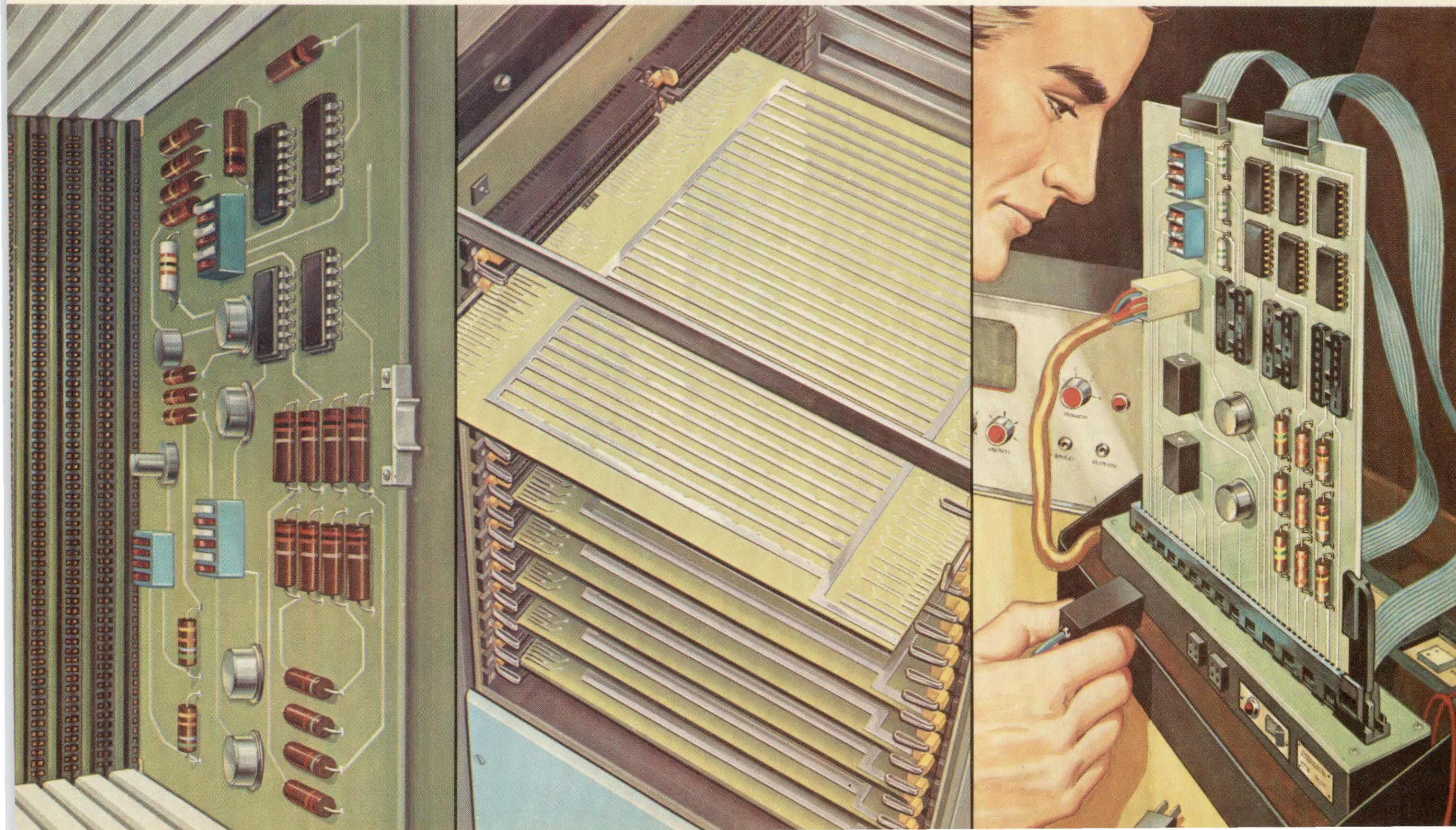
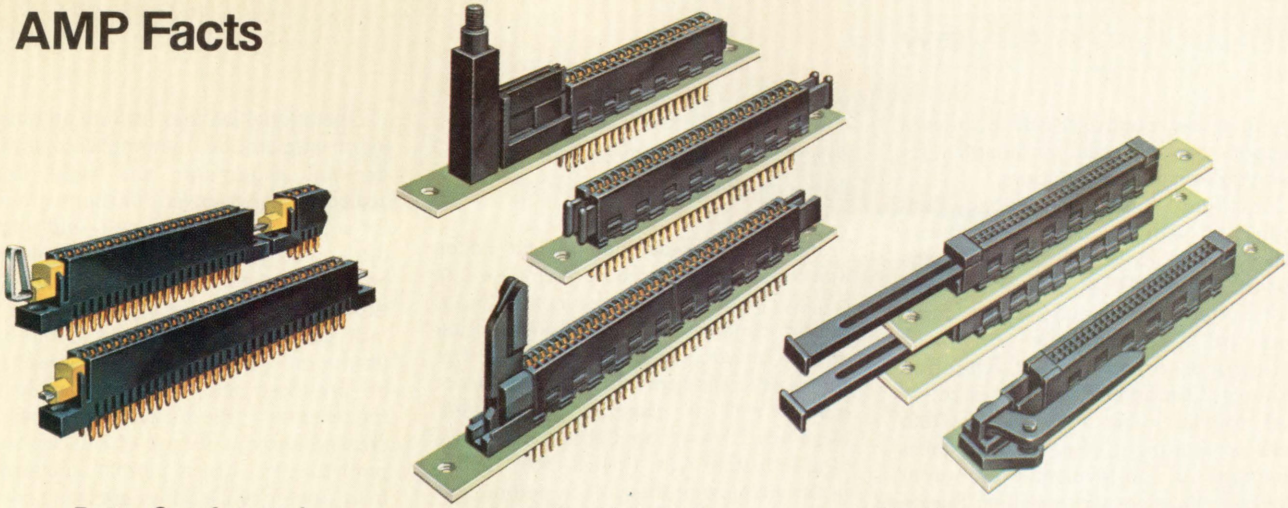
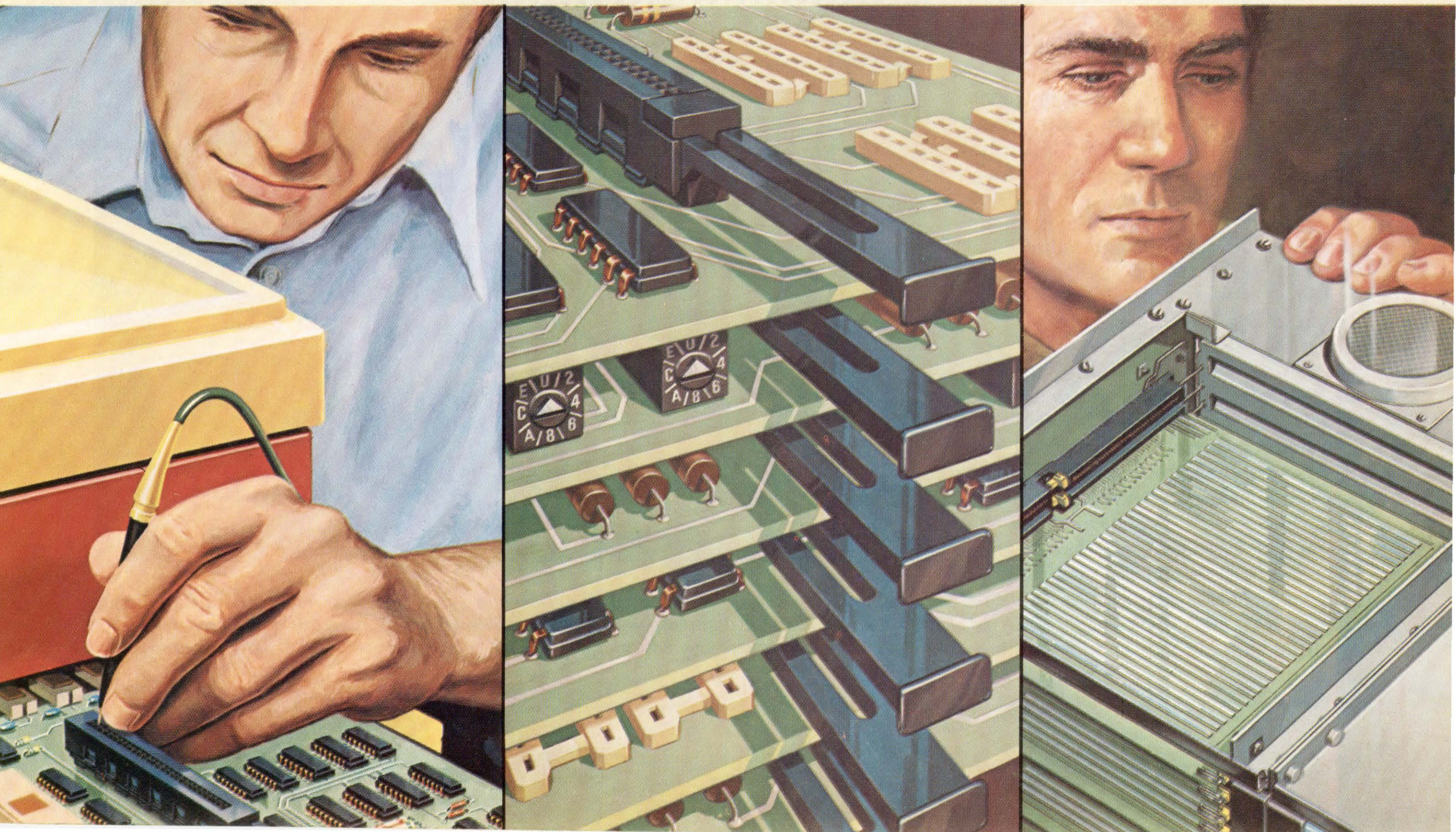






without a disc controller but includes a multiport communications adapter for operating multiple workstations.

Combining resource management capabilities with a range of software utilities and multiple high level language support, the RMS™ (Resource Management System™) operating system functions in a standalone or in a multiprocessor ARC™ (Attached Resource Computer™) environment (a local coaxial cable network). Within either environment, the software takes advantage of all available computer resources, locating and assigning the required processing power, memory, and peripherals needed to complete a particular computing task. In addition, it offers multitasking capabilities, disc data compression, large disc files, fast program loading, and a virtually unlimited number of file names on a single disc.

With the software, every workstation can perform every function supported by the software, whether data processing, word processing, or other function. Regardless of the processing need (memory, languages, storage), RMS manages the allocation of resources from whatever is available within the equipment configuration.

In an ARC environment, users can share available resources without being concerned about complex programming tasks to control those resources. Extra computing power can be added simply by attaching more resources to the network. A network user can configure the system to meet specific needs, and the resources of the network can be shared at all appropriate levels.

Processors and peripherals operating under RMS/ARC software can coexist within a network operating under DOS/ARC software. Most high level language applications written under DOS require only minor modifications to run under RMS software. Simultaneous operation of the two operating systems facilitates conversion of programs and files from one to another. In an ARC environment, unconverted programs and files can be used, even while the rest of the processors are operating under RMS software.

In practice, there is no limit to the size of a disc file under the software. Files can be as large as the storage capacity of the drive being used. Limitations on the number of file names per disc volume have also been essentially eliminated.

In its initital release, RMS supports COBOL, DATABUS[R] high level business-oriented language, and Assembler language.

Circle 350 on Inquiry Card

Standalone Visual Text Processing System Meets Entry Level Needs

Wangwriter is a standalone text editor that consists of three components—a CRT display, an independent keyboard, and a printer console with minidiskette drive and accompanying electronics—and that serves as a replacement for standard electric as well as electronic typewriters. Developed by Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851, as an element of their office automation strategy, it provides as standard many features available as options on other systems.

The display is a standard 12" (30-cm) diagonal CRT unit that shows 24 lines of 80 chars. Horizontal scrolling allows text lines of up to 158 chars.

The compact, floor standing printer console houses a bidirectional 20-char/s daisywheel printer with semiautomatic paper feed and eject control, a dual-sided, double-density minidiskette drive, and all accompanying electronics. Minidiskettes are 5.25" (13.34 cm) square with the capacity to store approximately 60 pages or 240k char each.

Operational features include automatic word wraparound, automatic centering, decimal alignment, and right hand justification. Advanced functions provide for super move, super copy, and a type through mode that permits information to be typed at the printer and displayed simultaneously on the screen.

A glossary feature allows commonly used words, phrases, and paragraphs to be prestored and retrieved rapidly for repeated use. Productivity is further increased through the use of a background print function which permits documents to be printed while others are being edited or created through the keyboard.

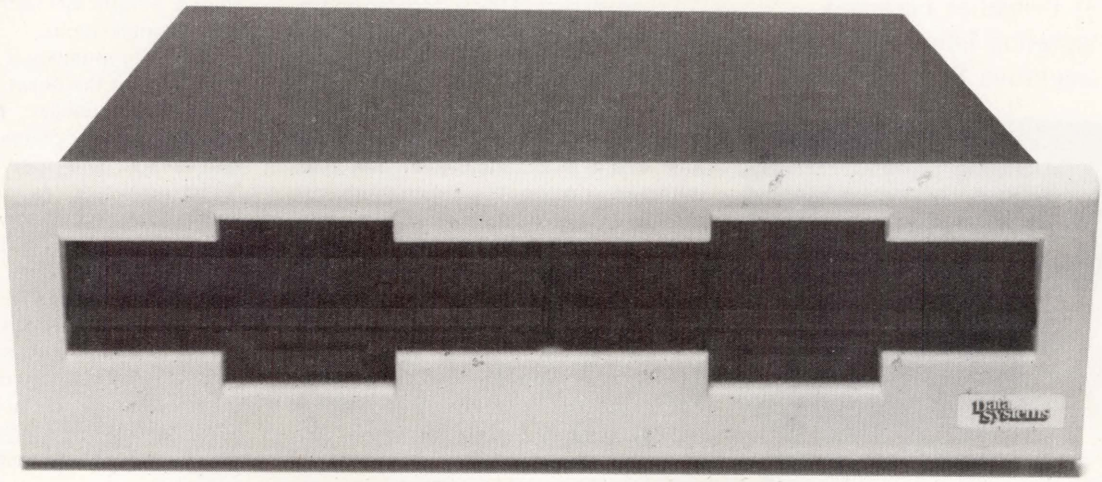
Introduced concurrently, the related Minidiskette Workstation serves as a peripheral to the company's office information system (OIS). This unit provides media compatibility with the minidiskettes, allowing the Wangwriter to transfer information to and from the OIS, and functions as a standard 64k OIS workstation.

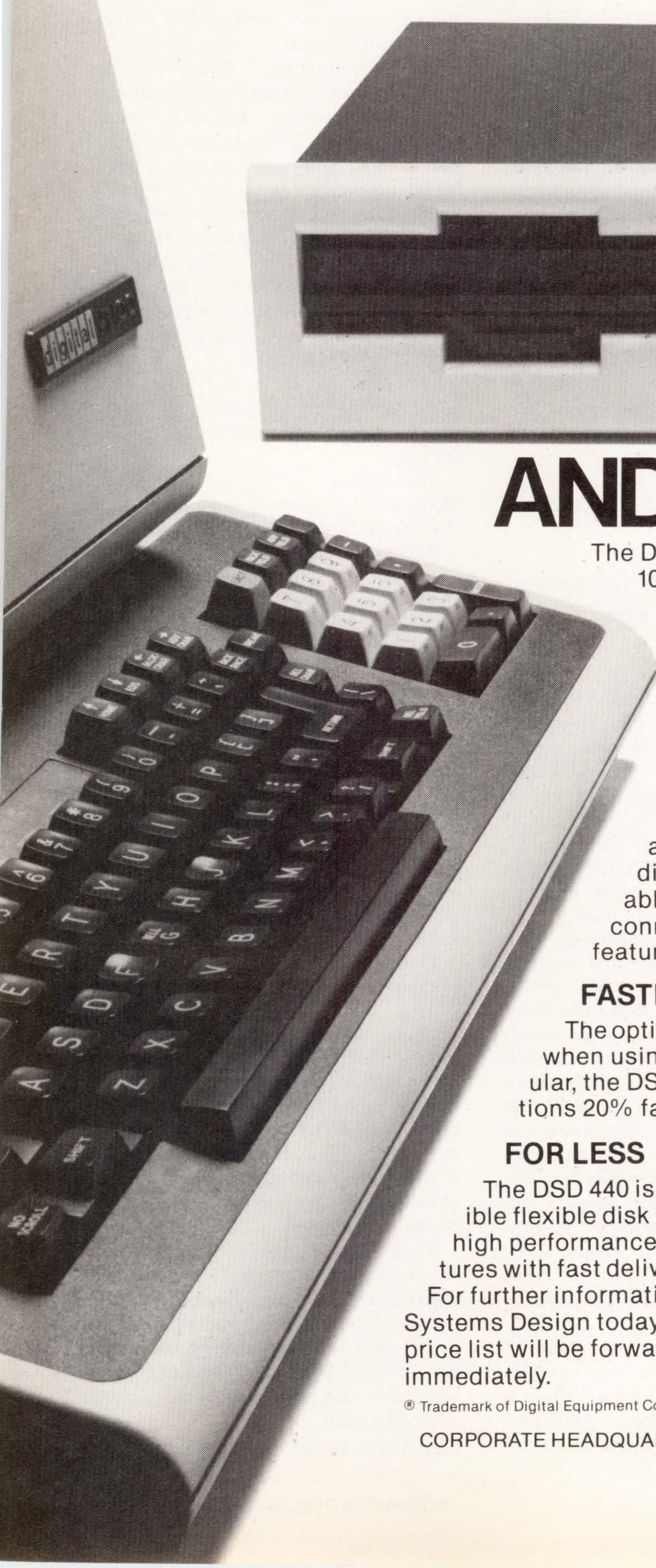
Price of the workstation, keyboard, printer console, and software is $7500. The minidiskette workstation will be available in May for $6200.

Circle 351 on Inquiry Card

Standalone Wangwriter includes 24- by 80-line video display screen, separate keyboard, and printer console complete with electronics and diskette memory. Providing storage on 5.25" minidiskettes, unit features editing and printing capabilities of larger systems

THE DSD 440. TOTAL DEC® RX02 COMPATIBILITY,





AND MORE.

The DSD 440 is the only alternative to the DEC RX02 that's 100% software, hardware and media compatible with LSI-11, PDP®-11 and PDP-8 computers, including those with extended memory. It can be configured as an RX02 for DEC double density or IBM 3740 single density recording, or as an RX01 for backward operating system compatibility.

MORE

A 512-byte hardware bootstrap is built into all PDP-11 and LSI-11 interfaces. It loads system software automatically from either single or double density diskettes. Extensive self-testing is DIP-switch selectable with the "Hyperdiagnostics" that run without being connected to a computer. The low profile 5¼-inch DSD 440 features write protection and diskette formatting.

FASTER

The optimized DSD 440 microcode increases system throughput when using the RT-11 foreground/background monitor. In particular, the DSD 440 with an LSI-11 runs fill and empty buffer operations 20% faster than an RX02.

FOR LESS

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CIRCLE 32 ON INQUIRY CARD

Modular Computer Packaged For Integration Into Instrumentation Systems

Designed for dedicated test, measurement, and instrument control applications, Hewlett-Packard's 9915A supplies heart of desktop HP-85 in rackmountable package that runs programs developed on desktop unit

The modular HP 9915A computer contains CPU, memory, operating system, and I/O parts of an HP-85 desktop computer in a rack mountable box packaged for integration into instrument systems. Running programs developed on the HP-85, the system offers the low system development cost of a desktop computer and the low unit cost of a board computer. It is being aimed by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, at dedicated test, measurement, and control applications.

Programs for the system are developed through the HP-85. With a program development ROM and an I/O ROM installed, the -85 becomes a development station featuring an interactive BASIC language operating system. With its interactive editing and debugging aids, it can also serve as a 9915 emulator for in-system software debugging.

When completed, system software is transferred to the 9915A via EPROM or magnetic tape. The unit accepts up to 32k bytes of EPROM-stored information. With an optional tape unit the system can exchange programs and data with data cartridges that contain approximately 200k bytes of programs or data.

Eight front panel LEDs and eight software definable special function keys provide an economical operator interface. Interfaces and I/O drivers facilitate connection of various CRT displays, keypads, typewriter keyboards, or custom control panels and keyboards.

I/O capabilities of the system include interrupt, bit manipulation, high speed transfer, software control of interface configuration, and easy data formatting. I/O drivers are built in. The standard unit comes with 16k bytes of user accessible RAM which is expandable to 32k bytes with an optional plug-in memory module. The operating system, contained in 48k bytes of ROM, expands through additional optional ROMs to provide matrix math, plotter/printer control, and mass storage control.

Price of the modular computer is \$1675; the cartridge tape unit adds \$425, and the operator interface \$350. OEM discounts are available.

Circle 352 on Inquiry Card

Network of Dedicated Computers Offers Data Sharing Plus Interactiveness

Domain, a network of dedicated computers, offers both the functionality of timeshared systems and the performance and interactive levels of dedicated systems. Specific features of the system developed by Apollo Computer Inc, 5 Executive Park Dr, North Billerica, MA 01862, are a 32-bit VLSI CPU dedicated to each user, a high resolution bit map display that permits each user to run multiple programs simultaneously, and network level modularity that supplies high performance levels, wide growth potential, and system reliability and maintainability. The network is a high speed, coaxially-connected communications system that joins all nodes such that each user can access both his own and other users' data with comparable speed and functionality. Node to node communications occur at a 10M bit/s transfer rate. Nodes connected to the network are dedicated, powerful computer systems designed to support a single user. Physically, each node consists of a display monitor, a keyboard, and an electronics enclosure.

While there are several basic nodes on the network with which to build complex applications, the Computational Node is the backbone of the system. Additional nodes include the Peripheral Node for shared peripherals such as line printers and magnetic tapes.

The Computational Node provides each user on the network with dedicated computing capability, access to system resources, and optional local dedicated disc storage. This node has both multiple 32-bit processors as well as a separate floating point processor. It also has a fully associated virtual memory mapping system which provides 24-bit virtual address and translates to a 22-bit physical address. In effect, each user process has access to a multi-megabyte program and data space supported by a physical memory of up to 1M bytes (the minimum is 256k bytes), allowing each user to solve very large problems on his own dedicated system.

File storage of the Computational Node can be either a local fixed media Winchester disc providing a minimum of 33M bytes, or a partition on a remote disc accessible over the entire network. Since storage provided on all nodes on the network is viewed as a uniform, very large, distributed file system, access to remote files is comparable to access to local files.

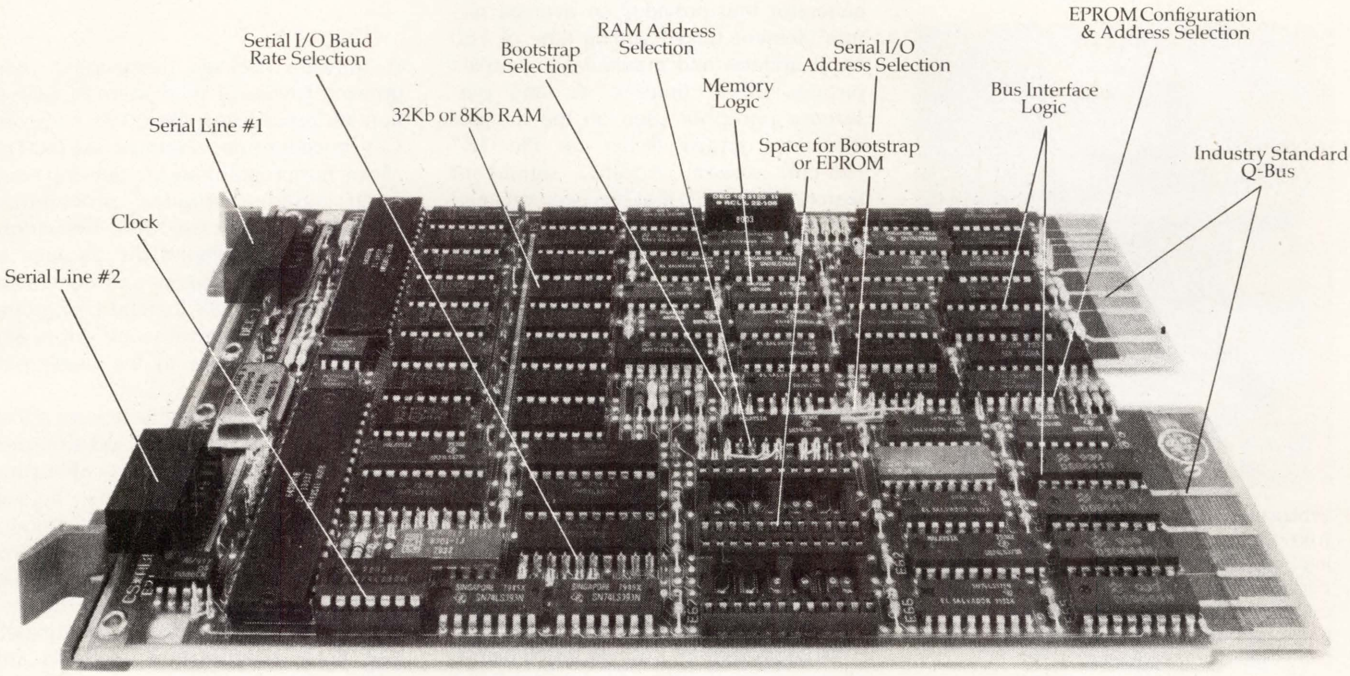
Interactiveness extends to the system's integrated bit map display capability. The display system supports multiple windows into different processes; these windows can be presented side by side or overlaid in whole or part. The display manager allows any window to be brought into full screen view instantly, and windowing allows the operating system to support multiple command environments simultaneously.

Operating software is based on a kernel optimized to service a single user as compared with traditional timesharing systems designed to maximize local machine efficiency. In addition to simple command level interaction the system provides user interfaces to menu selections, function keep, and graphics pointing devices. The command environment is a full programming language that includes multiple program execution by stream connections.

Typical prices for a Computational Node with 256k-byte main memory, bit-map display, keyboard, three serial ports, network interface, and operating system is \$24,000. A mass storage expansion consisting of 33M-byte Winchester fixed disc, and 1M-byte removable diskette adds \$10,000.

Circle 353 on Inquiry Card

Everything but the kitchen sink.



Digital's MXV11 will change your ideas about micro packaging.

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Yet it has so much capability, all you have to do is combine it with one of Digital's LSI-11 processors (also 5.2" x 8.9"), and you have a complete, low-cost microcomputer ready to handle a whole range of applications. From instrument control to intelligent terminals.

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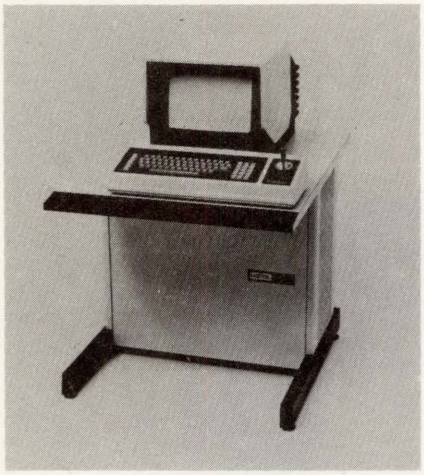
CIRCLE 33 ON INQUIRY CARD

Color Graphics Workstation Provides Line Drawing In Low Price Configuration



Whizzard 6250 color graphics workstation from Megatek offers CAD/CAM line drawing capabilities in low priced terminal configuration. Each unit consists of 13" color monitor and graphics processor packaged with keyboard and joystick control in desk style cabinet

A color graphics workstation that provides dynamic line drawing capabilities at a low price for use in distributed CAD/CAM applications, the WHIZZARD 6250 consists of a 13" (33-cm) color raster monitor packaged with a keyboard and joystick control in a desk-style cabinet. Its 14-slot chassis includes a graphics processor, vector memory, RS-232 serial asynchronous interface, and room for option modules.

Megatek Corp, 3931 Sorrento Valley Blvd, San Diego, CA 92121, designed this RS-232 configuration to provide the high technology graphics features of the larger WHIZZARD 7250 color raster system (see *Computer Design*, May 1980, p 155) in a smaller unit that costs only half as much. "The size and expansion capabilities of the 6250 have been limited intentionally so that the cost can be maintained at an affordable level for use by more people," explained Peter J. Shaw, Megatek's vice president and director of marketing. "This means that it has a smaller chassis, monitor, and power supply; offers only eight colors with no color lookup table; and cannot be expanded to use hardware modules for clip, rotate, and scale transformations. Other than these exceptions, the two systems are essentially the same."

The unit incorporates the 7250's proprietary high speed digital vector generator that provides an average picture element (pixel) writing time of 160 ns. It updates and manipulates complex pictures 20-30 times/s. A long persistence phosphor used on the monitor eliminates screen flicker on the 13" (33-cm) screen. Another significant feature of the 7250 that has been retained is the 4096 x 4096 virtual vector space, which provides a high level of detail in realtime steps from 512 x 512 through 4096 x 4096. To the user, this provides a standard capability of displaying the entire 4096 x 4096 area on the screen or zooming in on some smaller viewport, such as 2048 x 2048, 1024 x 1024, or 512 x 512, according to Shaw. "This zoom feature is a true scaling, rather than the pixel replication available on other raster systems. Scaling causes more and more information to be displayed, allowing the user to see more and more of the details contained within the 4096 x 4096 virtual display space."

Write protection of individual bit planes allows realtime data to be displayed simultaneously with static overlays. Double-buffered bit planes also permit erasure of overlapping or intersecting lines in a drawing without causing breaks in the lines that remain in other planes on the screen.

Use of a powerful bit slice architecture microprocessor and the WAND 6200 software package provides a high level of intelligence in the remote terminal, reducing communications traffic with the host computer. A subset of the WAND 7200 software system, WAND 6200 is written entirely in ANSI FORTRAN, following CORE guidelines established by ACM SIGGRAPH. It provides support for all output functions, including segment and memory management control, display processor control, display and segment attribute control, and error generation control. Since it is completely compatible with WAND 7200, all programs written for use on the 6250 will be compatible with programs written for larger systems, including both vector refresh and color raster types.

The system is priced at $17,500. Deliveries are scheduled to begin in March 1981.

Circle 354 on Inquiry Card

Procedure Development Software Allows Oscilloscope Calibration To Be Computerized

A software package designed to meet growing pressures to modernize calibration lab procedures, the CG 551AP Scope Cal Procedure development aid (SCPDA) allows nonprogrammers to develop computer aided calibration procedures. Tektronix Inc, PO Box 500, Beaverton, OR 97077, developed the package to govern operator actions and generation of calibration signals thereby taking over measurement of oscilloscope errors and making comparisons to the user's permissible standards.

The package allows a technician skilled in calibration techniques to develop procedures that reflect his calibration philosophy. The result is a step by step procedure that will guide an operator through the most involved calibrations, eliminating the possibility of a critical step being overlooked. In addition, throughput is increased approximately four times over manual methods and easily analyzed management data are collected.

Designed for use with the CG 551AP, a microprocessor based oscilloscope calibration generator that is fully programmable, the software forms an integral part of a system using GPIB (General Purpose Interface Bus, IEEE 488). Although the CG 551AP Programmable Calibration Generator can be used manually, it will typically form part of a system that will include a controller (such as the Tektronix 4052 Graphics Computing Controller) for program development and execution, and may include a hardcopy printer or a line printer for automatic documentation. The SCPDA software is written in 4050 BASIC. The software assumes that the operator is not familiar with programming, and takes advantage of two simplified approaches to incorporate the calibrator's knowledge. The first is a series of questions that appear on the controller's CRT. The calibrator's answers to these questions form the foundation for the software that will eventually run the system. The second approach is the "LEARN" mode, which allows the calibrator to set function and ranges using

(continued on page 64)

You're looking at a raster graphic* generated by the best family of high-speed, high-resolution processors, monitors, and peripherals available. *Dollar-for-dollar,* they'll outperform *any* systems you can buy.

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LEXIDATA CORPORATION

*Photo of actual CRT display.

RASTER DISPLAYS...FOR THOSE WHO DEMAND PERFORMANCE

CIRCLE 34 ON INQUIRY CARD

16 bits of information

1. Self-contained and upward compatible. The 8550 Microcomputer Development Lab is the single-user member of the new 8500 Modular MDL Series, which also includes the 8560 multi-user system and the 8540 Advanced Integration Unit for the host computer environment. The 8550 is a complete microcomputer design tool, covering both software development and integration into the prototype. The 8550 can also be used as a station on Tek's forthcoming 8560 multi-user system.

2. Real-Time Emulation. Takes the concept of emulation to a new performance level. Advanced circuitry eliminates the need for wait states during program execution and debugging. The emulator processor now functions in real-time, with its operation totally transparent to the user.

3. Multi-Vendor Chip Support. The 8550 MDL supports 26 chips in all. The broadest support available anywhere, covering a wide range of vendors. With microcomputers as well as microprocessors. The ultimate in design flexibility.

on the new 8550 MDL.

4. 16-bit Support. You'll be able to choose from an entire new generation of 16-bit processors. Tektronix has the high performance tools to make it possible. Assembler support is available now for the 16-bit chips listed below. The TMS 9900 and SBP 9900 are fully supported with emulation today. Real-Time Emulation and Pascal support will be available in stages for the 68000, Z8000 and 8086 beginning the third quarter of 1981.

68000	**TMS 9900**
Z8000	**SBP 9900**
8086	

5. 16-bit Trigger Trace Analysis. Gives you highly sophisticated triggering ability for selective snapshots of full-speed code execution on the prototype bus. Up to four data acquisition triggers can be combined in a wide variety of ways. Bus cycle resolution to 8 MHz.

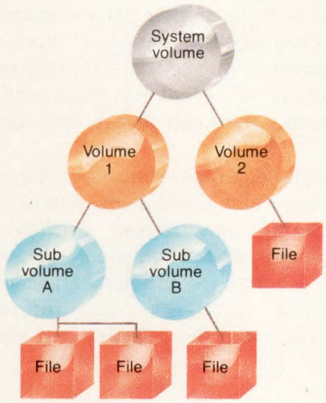
6. 8-bit Support. Besides the most up-to-date microprocessor coverage, you can also take advantage of extensive 8-bit microcomputer support. All 8-bit chip support includes real-time emulation.

6800	**8048**	**3870**
6802	**8039**	**3872**
6808	**8039-6**	**3874**
Z80A	**8035**	**3876**
8080A	**8021**	**F8**
8085A	**8022**	**1802**
8049	**8041A**	**6500/1**

7. 8-bit Real-Time Analysis. An optional Real-Time Prototype Analyzer lets you extract both bus and hardware logic at full operating speeds. You capture 48-bit words for storage in a 128-word memory. Two triggers for precise data acquisition.

8. Split-Bus Architecture. The 8550 uses one processor and bus for system operation, and another for real-time emulation. This architecture assures that the emulator processor is denied access to system memory, preventing the possibility of a system crash during prototype program execution.

9. Tree-Like File Structure. Combines ease of use, rapid access and in-depth organization. Allows files to be arranged in a predetermined hierarchy that best supports your current situation. A flexible tool that supports filing situations from very simple to extremely complex.



10. Advanced CRT-Oriented Editor. Gives you the quickest path possible to perform many editing operations. Lets you use screen-oriented editing as well as line-oriented editing. Up and down scrolling capabilities give you a total window on all of your code.

11. Macro Assembly. The most powerful assembler software available today in a development system. Lets you employ user-defined constructs and library resources. A conditional assembly feature allows sophisticated user manipulation of code at assembly time.

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front panel controls and to have these entries automatically transferred to the controller for use in forming the program.

All information acquired during this process is automatically converted into a simpler program format that will govern the system's operation. These procedures can then be used by less skilled personnel to test and calibrate oscilloscopes.

Besides governing operator actions and generation of calibration signals, software takes over much of the measurement of oscilloscope error and all comparisons to the user's permissible standards by accepting data from the CG 551AP or the controller keyboard. Measuring accuracy is improved through extremely low noise content, which makes measurements at low levels (40 μV) practical; rise time, aberrations, and long-term flatness performance; an updating of the traditional timing marker method of timing oscilloscope sweeps; and the addition of "slewed edge" approach, which keeps pace with the fast sweep speeds used to test digital circuitry (0.2 ns/div).

Circle 355 on Inquiry Card

Conferences Issue Call for Papers Covering Computers and Connectors

Areas of practical importance within the broad scope of the art and science of computer usage will be covered during the Annual Conference of the Association for Computing Machinery, to be held Nov 9-11, 1981, in Los Angeles, Calif. The program committee is soliciting tutorials, proposals for panel discussions, and short technical papers or surveys for presentation with special emphasis on innovations or recent advances and the connection between theory and applications.

Suggested topics include operating, database, and distributed systems: programming languages; artifical intelligence; software engineering; privacy and security; computer architecture; graphics networks, computers in aerospace and the military; and simulation.

Authors should submit four copies of their work; proposals for special sessions or tutorials should contain sufficient details to explain the presentation. Deadline for submission is Mar 7, 1981. ACM '81—Call for Papers, Village Station, PO Box 24059, Los Angeles, CA 90024.

To be held by the Electronic Connector Study Group, Nov 11-12, 1981, at the Franklin Plaza, Philadelphia, Pa, the Annual Electronic Connector Symposium will cover significant advances in the field. Papers are invited in the areas of printed wiring applications, data and documentation requirements, military and space applications and packaging, flexible and flat cable circuitry, fiber optics, and test methods and evaluation. Also of interest are rf and emi applications, materials, finishes, and platings, standardization and reliability, IC packaging, backplane interconnection wiring, and termination and connector techniques.

Deadline for 200-word abstracts is Mar 20. Send to Papers Chairman, 14th Annual Connector Symposium, PO Box 167, Fort Washington, PA 19034.

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CIRCLE 36 ON INQUIRY CARD

Small Computer Family Includes 32-Bit Multiprocessor Superminicomputers

DPS 6, a family of 10 models covering a range from entry level to supermini class machines, responds to the changes being made in the way computers are used. Announced by Honeywell Information Systems, 200 Smith St, Waltham, MA 02154, the family includes 16- and 32-bit models based on the advanced technologies and bus architecture of the existing Level 6 line. The company also addressed the office automation area with the introduction of a word processing application facility and communicating shared resource systems running under the GCOS 6 operating system.

With performance levels that begin at about twice that of the Level 6 Model 23 and reach to approximately three times that of the Model 57, all models have a file commercial instruction set. Systems are targeted at data processing, transaction processing, office, and network applications, and are packaged to fit them while offering growth and expansion flexibility.

Based on the Level 6 architecture, the family's machine level instruction set is identical to that of recent large Level 6 models. Three processors are used in the series. In the 6/30 the processor occupies just one board slot yet offers a traditional minicomputer instruction set, as well as a full COBOL oriented set claimed to be better than that of most mainframes. Supplied are decimal arithmetic that supports normal COBOL data types directly in hardware, binary-decimal conversion, and character string editing, as well as functions such as searching an array of character strings for match or mismatch on a given substring. In addition, the processor includes a memory management unit with segmentation, relocation on a segment to segment basis, and four-ring protection structure.

In the DPS 6/48, an optional floating point processor can be added. This unit's processor introduces a second slave processor board to handle the commercial instruction set more effectively. Cache memory, added in 6/70 systems improves performance significantly. Top of the line 6/90 models, however, switch to a 32-bit processor while retaining software compatibility with 16-bit members of the family.

This processor adds a full set of 32-bit functions to those provided by the Level 6 Model 57 without altering existing functions or introducing emulation modes or registers. Instruction set, register structure, and memory and I/O busing, as well as internal CPU implementation, are all designed to allow smaller systems to be upgraded and to provide greatly increased throughput. 32-bit registers are added without altering the 16-bit general registers and address registers.

The Megabus structure of previous processors has been extended to double its throughput—from 6.5M to 13M bytes/s. Compatibility with existing units allows any 16-bit controller to be plugged into the 32-bit bus without the need for adapters, multiple buses, or duplicate controller lines.

Performance is attained by the structure's three pipelined processors. The central processor obtains the instructions, develops addresses, and executes short traditional binary instructions. Acting as slaves, the other two processors pick up and execute commercial and scientific instructions, respectively, leaving the central processor free to fetch the next instruction and begin processing it. With this structure, basic instructions are executed in a fraction of a microsecond.

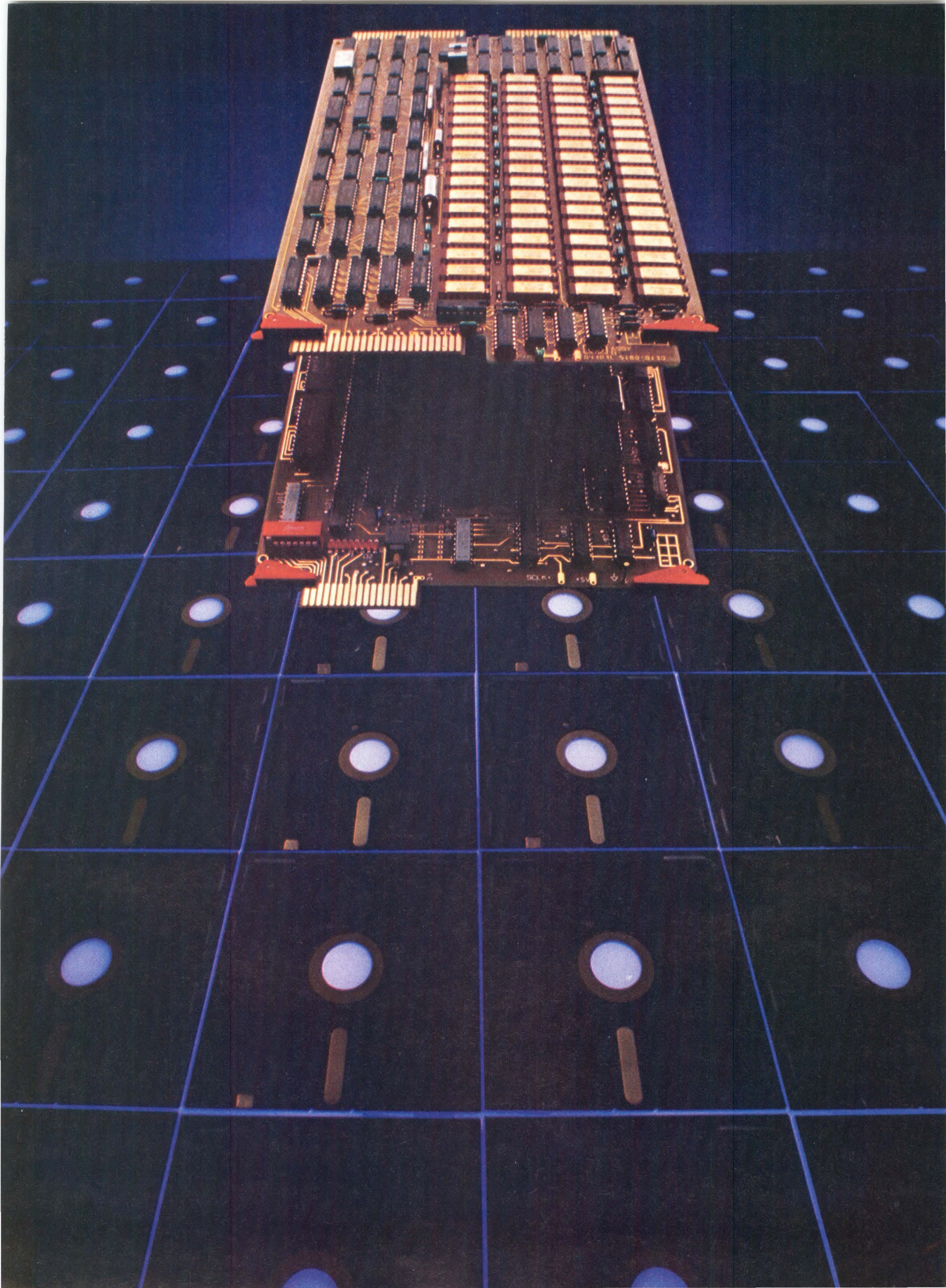
At the low end of the DPS 6 family are the DPS 6/30, /32, and /34, which are 5-slot megabus units in 30" (76-cm) cabinets. Main memory sizes range from 128k to 256k bytes. Also in this group is the DPS 6/38, which has a 10-slot megabus and a maximum memory capacity of 768k bytes. In typical configurations, prices range from \$28,800 to \$75,000.

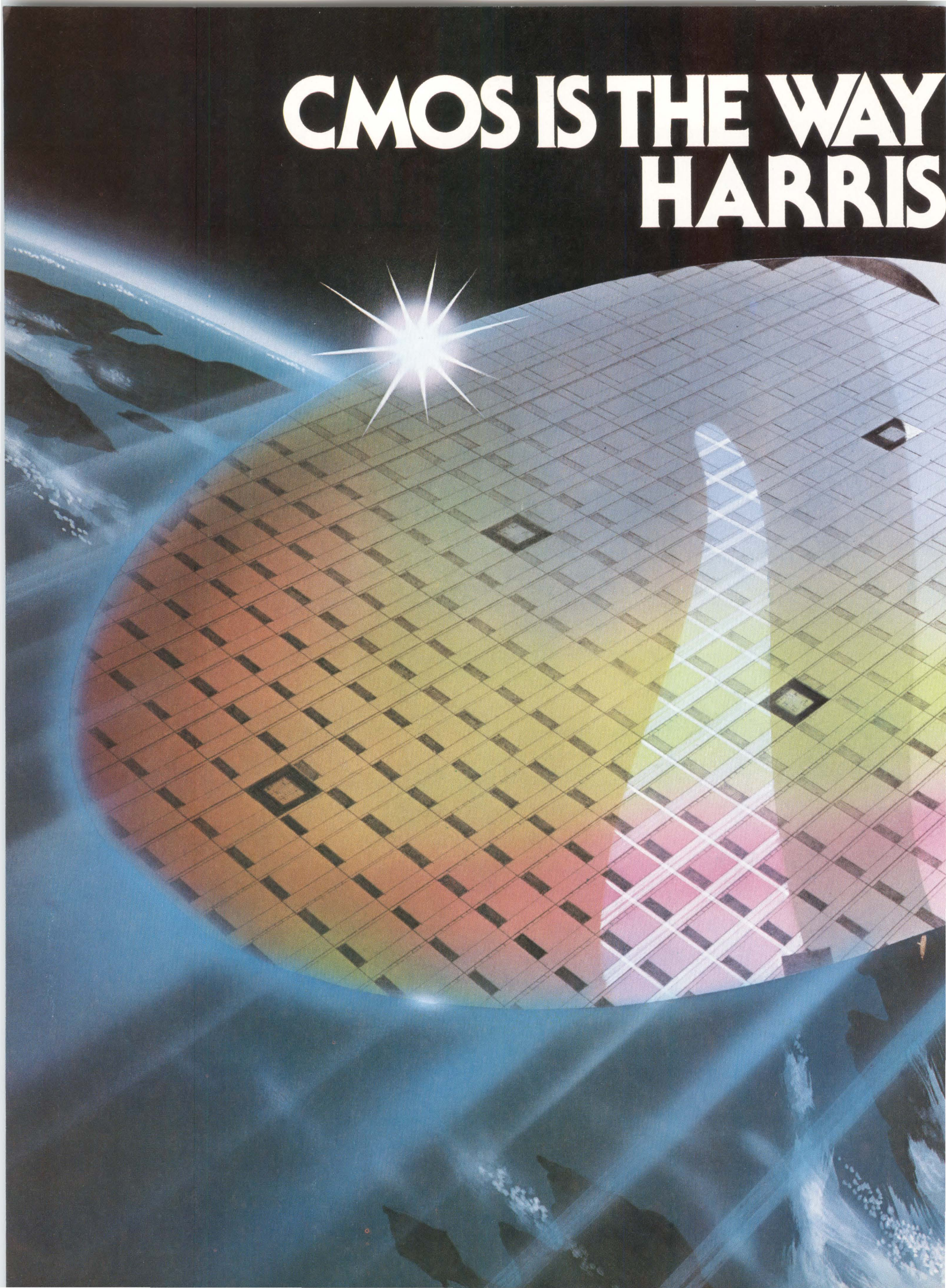
In the mid-range are DPS 6/48, /54, /74, and /76, all 16-bit machines that are field upgradable to 32-bit systems. The /48 and /54 come with a 20-slot, 32-bit expandable Megabus and a 60" (152-cm) cabinet. The 6/48 can accommodate up to 32 communications lines and offers a performance level 30 to 100% higher than the Level 6 Model 33, substantially more memory capacity, and wider configurability. The 6/54 handles up to 40 communications lines and in COBOL-oriented environments is 20 to 100% faster than a Level 6 Model 43. Both systems have a memory capacity of up to 1M bytes.

The 6/74 comes with a 20-slot Megabus, accommodates 40 communications lines, has a maximum memory of 1M bytes, and offers up to 1G bytes of mass storage. The 6/76 comes with 30-slot Megabus, accommodates 64 communications lines, has a maximum memory of 2M bytes, and offers up to 2G bytes of mass storage. Both have 60" (152-cm) cabinets and incorporate a fast cache memory. All four upgradable models are available with an optional scientific instruction processor in addition to the standard commercial instruction processor. Typical systems are priced from \$50,000 to approximately \$200,000. The DPS 6/54 has 30 to 50% more processing power than the Level 6 Model 43; 6/74 and 6/76 are each 30 to 100% faster than the Level 6 Models 43 and 47, respectively.

In the 32-bit category, the 20-slot 6/92 with the 32-bit megabus chassis, CPU, cache, commercial and scientific instruction processors, 1M-byte memory (64k chips), 64 communications lines, 2 disc drives, console, and 600-line/min printer is priced at \$223,400. The DPS 6/96 with 40-slot, 32-bit megabus chassis, cache, CIP and SIP, 4M bytes of 64k chip memory, 112 communications lines, 4 disc drives, console, 900-line/min printer, 2 tape drives, and card reader sells for \$461,800. 16-bit models will be available in the first quarter of 1981, and 32-bit models in the fourth quarter.

Office automation products include a word processing applications facility called Word Processing 6, which runs on DPS 6 and Level 6 small computers under the MOD 200 and MOD 400 executives of the GCOS 6 operating system, plus two models of a DPS 6-based Administrative System with up to 4 and 16 workstations, respectively. The application facility and the administrative system both provide text editing and revision, storage and retrieval of boilerplate text for inclusion in any document, multi-indexed document filing and retrieval, merging of standard and variable text from different documents, formatting, prevention of unauthorized access, and a document distribution capability for sending and receiving documents between business locations. Circle 356 on Inquiry Card

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Enhanced IBM Compatible Disc Controller Emphasizes Data Availability

A disc storage control unit for use with IBM and plug compatible mainframe computers, the 38304 provides two independent paths—called storage directors—for transfer of data and file positioning commands between processor channels and disc storage units. In making the announcement Control Data Corp, Box 0, Minneapolis, MN 55440, concurrently revealed plans for future IBM compatible disc drive and controller products which include a series equivalent to the 3880 control unit and associated discs such as the 3380 drive.

Design of the controller emphasizes data availability as well as capacity and performance, while reducing space, power, and cooling requirements. This unit provides the capability of two IBM 3830 controllers but occupies one-third the space, and uses one-fifth the power.

Each storage director of the controller operates independently, can be serviced individually, and includes its own power supply that is capable of operating both directors automatically if the other supply fails. The controller can be attached to block multiplexer channels of IBM 4300 series groups 1 and 2, 303X, and /370 series processors. Each storage director can access up to four processor channels with the addition of optional 2- and 4-channel switches.

In a 4-channel configuration, an individual storage director can control up to four strings of drives—a maximum of 32 actuators—to provide a total capacity per director of more than 20G bytes of data. Disc drives that can be attached include the 317M- and 635M-byte 33501 and 33502; the 100- and 200M-byte 33301 and 33302; and equivalent IBM 3350, 3333 and 3330 drives. A combination of 38304 storage controller and the 33502 disc unit will provide performance and capacity that are equivalent to that of an IBM 3350 subsystem, yet will use only half the power and take half the space.

Circle 357 on Inquiry Card

Japanese Language Information Processor Handles 9000 Ideographs

A Japanese language information processing system adds full Japanese language processing capabilities to an existing alphanumeric-Katakana based system. Announced by its joint developers NCR Corp, Dayton, OH 45479, and its subsidiary, NCR Japan, Ltd, the system is called JAPAN (for Japanese Advanced Processing Architecture by NCR). This announcement was coupled with introduction of I-8290 family of computer systems that support both conventional alphanumeric-Katakana processing and the JAPAN software.

A minimum system, capable of handling approximately 3600 different ideographs, can be expanded as required up to a maximum system accommodating approximately 9000 different characters. Existing I-8200 users can upgrade by adding JAPAN software, Japanese language video display, and Japanese character printer to their current configuration. Display units and printers located at remote sites in a processing network can interchange data with a Japanese language processor over standard communications lines.

Circle 358 on Inquiry Card

Processor Family Doubles Power of Predecessors

Models 5860 and 5880, single- and dual-processor units in the 580 family use air cooled LSI technology, advanced microcode techniques, and an additional class of firmware called macrocode. The 580 series comprises the most powerful units produced by Amdahl Corp, 1250 E Arques Ave, Sunnyvale, CA 94086.

Series 580 model 5860, a uniprocessor configuration, provides twice the processing power of the 470 V/8, and represents a compatible evolutionary extension to the 470 series. Built using air cooled LSI technology, it allows up to 32M bytes of main storage and 34 I/O channels, and occupies about 40% less space than 470 configurations. The system is supported by MVS/SP, VM/SP, and ACP operating systems, and can be field upgraded to a 5880.

Model 5880, a complete dual-processor complex, offers 36 channels and 32M bytes of main storage. Supported by MVS/SP and VM/SP, this tightly coupled configuration offers 3.4 to 3.6 times the performance of a 470 V/8.

Circle 359 on Inquiry Card

Options Extend Source and Measurement Range Of Discrete Test Systems

Options extend the source and measurement range of T300 family discrete test systems to permit testing of high power and low current devices. Introduced by Teradyne, Inc, 183 Essex St, Boston, MA 02111, the options are M181 Low Current Instrument, M195 Thyristor Test Adapter, and M160 Multiplexed Current Source.

The low current instrument performs leakage measurements on FETs down to 100 fA with 10-fA resolution. The system addresses the severe problem of heat transfer encountered when measuring in the 10^{-15} A range. Two independently programmable voltage supplies, an ammeter for measuring from 200 μA to 100 mA, and data bit storage for two multiplexed test stations are also provided.

Optimized for testing SCRs and triacs, the M195 meets requirements for thyristor testing by providing accurate, clean test pulses, preventing false triggering due to dv/dt, and allowing variable test time for holding current testing. The option's three independently programmable bidirectional power supplies are accurate to 1%. Test times are software controlled. A current supply up to 5 A can be provided for 100 μs to 10 ms, allowing I_H testing of 50 to 400 Hz devices.

Requirements for testing high power devices are met by the M160 multiplexed current source. The unit can provide 160 A of collector current and 50 A of base current at up to 12 V, and can perform breakdown tests at 800 V and 1.5 A.

Circle 360 on Inquiry Card

Low Cost System Uses Data Streaming to Search Large Data Bases

Associated File Processor, a special purpose hardware system, retrieves text and document information from large data bases. Operating standalone or as a subsystem to a large computer, the system from Datafusion Corp, 5115 Douglas Fir Rd, Calabasas, CA 91302, provides effective character matching at 9G bytes/s.

Replacing elaborate software systems running on large mainframes, the AFP uses data streaming handled by the AXP-100 associated crosspoint processor, firmware and user software, PDP-11 processor, user frontend system, and conventional disc units. It scans contents of the database disc at a rate of 1.2M bytes/s with 8k bytes of parallel query term memory.

The data base is maintained on disc systems accessible by both AFP hardware and the CPU. Documents may be stored as completely full text or may be partially or fully formatted. Queries are generated online and may be input from several CRT displays simultaneously. A natural language query can be formatted from a few key words or more efficiently using Boolean expression forms.

Outstanding queries are collected, key phrases and terms extracted and loaded into memory by the AFP, before it starts the search. During a search, the CPU is free for other chores since its bus is disconnected from the search disc.

Retrieval and review of documents is performed on user demand, and can occur either during or after a search. Documents of interest may be saved in a user's personal file for later review, output to other devices, or made into reports for hardcopy review.

Five configurations of the system range from model AXP-100 with AFP and disc controller, firmware, and user software for $39,000 to an AXP-300T16, which includes AFP, PDP-11, disc and controller, magnetic tape unit, line printer, 16 CRT terminals, and workstation concentrator, priced at $179,000.

Circle 361 on Inquiry Card

Entry Level Computers Provide English Language For User Programming

A user programmed computer DAVID functions as a standalone computer or as an intelligent terminal in a system of up to 20 users. Featuring 1.25M bytes of floppy disc storage and a choice of printers, the system's built-in logic effectively performs storage, retrieval, and processing on data.

Logical Machine Corp, 1294 Hammerwood Ave, Sunnyvale, CA 94086, has provided the machine with capability to operate in most spoken languages, including French, German, Italian, Portuguese, and Spanish, as well as English. Most standard programming chores have been eliminated, allowing users to concentrate on applications. The system's English language requires significantly fewer instructions and shorter programs than BASIC or COBOL, achieving greater programmer productivity.

The system provides 1.25M bytes of floppy disc storage, 64k bytes of memory, and a choice of printers. Up to 20 of the units can be attached to a larger central storage file unit, which arbitrates use of files and records for each. In this configuration each DAVID operates as a standalone computer while utilizing the larger system's filing resources.

Circle 362 on Inquiry Card


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CIRCLE 39 ON INQUIRY CARD

SOFTWARE

Database Machine Solves Problem of Resource Saturation

A backend database system that organizes data within a computer to suit specific needs makes accessing and updating far easier. Offered as a solution to the problem of resource saturation by Software AG of North America, Inc, Reston International Ctr, 11800 Sunrise Valley Dr, Reston, VA 22091, the machine provides a means of offloading a database management system freeing up to 60% of the mainframe's time to perform other tasks.

Basically a mainframe computer that attaches to a host computer through a special communications system, the machine incorporates a special processor which serves to contain the system itself. The externally supported processor (ESP) mainframe is compatible with IBM /360, /370, and 4300 series processors, and provides their functions. The database machine (DBM) communicates with the host computer through a special channel to channel communications system (CTCS). The DBM contains the database management software ADABAS, while the host computer executes the applications programs.

The ESP processor combines extensive microcoded instruction capability with fast executing ECL hardware that supports a machine cycle speed of 50 ns, and offers processing speed of 0.75M instructions/s. It uses a common microprogrammed, bus driven architecture that allows simple field upgrading of CPU, memory, and I/O channels via printed circuit board changes. The mainframe contains 2M bytes of main memory, one byte-multiplexer channel, and two block multiplexer channels, and provides an integrated channel to channel adapter.

Designed to facilitate the transmission of commands, data, and status information between the host computer and the backend machine, the CTCS communications system consists of a user machine communications module residing with the host computer and data base machine communications module in the backend processor. These modules are joined by a high speed channel to channel link which facilitates increased database performance.

ADABAS offers a simple data base design. It is an inverted list, multithreaded system that facilitates a relational hierarchical or network view of the data. Functions are distributed between the two computers. The nucleus resides with the DBM, where all updates, finds, adds, deletes, and disc management take place. Applications programs, which reside with the host, call ADABAS through the communications interface module and are translated for transmission to the data base machine through the CTCS.

The DBM can function in different configurations depending on needs of the environment. A number of host machines can communicate with one DBM, or a number of DBMs can communicate with one or more hosts. Host mainframe may be any IBM /360, /370, 303X, 4300, or plug compatible unit under OS or MVS operating system. DBM runs under VS1. ADABAS requires about 256k resident memory in the DBM. Channel to channel software requires less than 20k in each mainframe.

Circle 363 on Inquiry Card

Standardized Color Graphics Software System for Process Control Applications

Color Graphics System (CGS) can be used to create, modify, and display color images related to a range of industrial process and electric utility plant operating parameters. Introduced by Scientific Systems Services, Inc, 1135 John Rodes Blvd, Melbourne, Fl 32901, the software interfaces with Aydin 5215 display generator and color monitors plus either Modcomp, PDP-11, or Sel 32 computers. Since it is written in FORTRAN IV, it is easily convertible to other computers that have a FORTRAN compiler and file I/O capabilities.

The system enables users to keep informed about various plant conditions at a number of remote locations. Flow lines of electricity or fluids, or other diagrams of systems or processers can be drawn and displayed. Operators can create, modify, delete, and save images from the main color monitor. Images can be displayed on any monitor connected to the system.

Dynamic display capability allows certain conditions or point values to alter the image so that it can be detected easily. Open and closed valves can be different colors and alarm conditions can be shown by blinking signals.

Circle 364 on Inquiry Card

Flexible Software Speeds Development of Factory Data Collection Systems

An enhanced version of Transactor definition language (TDL) software incorporates years of programming experience into an easy to use English method of programming without coding sheets, key punching, or prior programming experience. The flexible TDL software system from General Automation, Inc, 1055 S East St, Anaheim, CA 92803, permits fast low cost configuration of factory data collection terminals to meet individual requirements and supports a total system consisting of the company's processors and Transactor data collection terminals.

The software is tutorial and interactive. A user simply answers a series of questions that appear on a CRT screen. During configuration of the transaction network, functions, formats, prompts, error messages, and other features can be defined for each terminal in the system.

The package includes software to support a load sharing redundant processor configuration, which offers maximum data collection reliability and system uptime. It is capable of interfacing to applications currently written in FORTRAN or COBOL, and of handling existing 80-col punched cards.

Circle 365 on Inquiry Card

CAD Software Runs Engineering Analyses on Superminicomputers

A CAD package running on Harris Corp's 500 and 800 supermini systems under the Vulcan operating system performs engineering analyses cost effectively. ANSYS software, developed by Swanson Analysis Systems, Inc, PO Box 65, Houston, PA 15342, cuts the cost of data preparation and review of results.

The finite element CAD package enables engineers to solve a variety of problems in structural analysis, heat transfer, thermal fluid flow, thermoelectricity, and wave motion analysis. Using the interactive package, engineers can graphically review data as they are input and modified, guaranteeing that the model and boundary conditions are accurately defined before the job is processed. Interactive graphics available with the system simplify the review of results and are more informative than conventional printouts.

Circle 366 on Inquiry Card

High cost wrap/pin boards made OBSOLETE

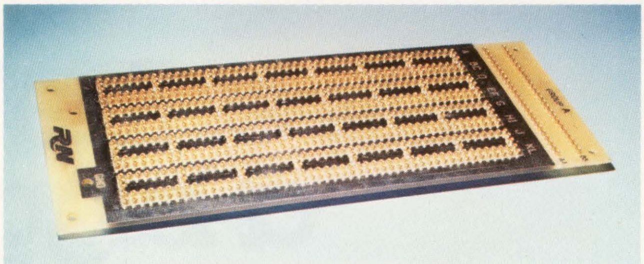
Save money, save time! Wire your boards faster, easier than ever before —with the RN QUICK/CONNECT point-to-point IDC wiring system.

Here is a wiring system that does what wrap/pin does—but does it faster, easier. The wire is simply pushed into the "Quick/Connect" tine which pierces the insulation (IDC) making a gas-tight connection between wire and terminal. "Daisy chain" wiring is accomplished with no break in the wire, no insulation stripping.

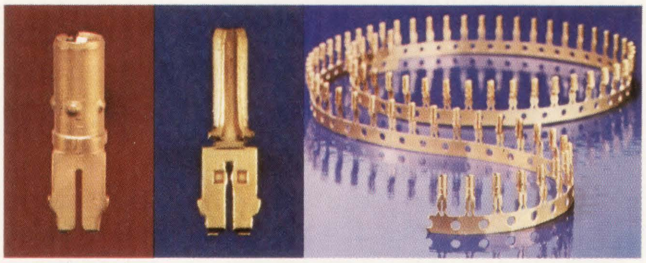
You'll never willingly use wrap/pin for boards again. Consider these advantages:

1. **High speed wiring simplicity**—You connect just **one** wire per connection. There is **no time-consuming insulation stripping** as needed with wrap/pin.
2. **Fast, easy wiring changes**—Repair or modify boards by simply removing the individual wires and quickly re-wiring. Field wiring modifications are simple and fast.
3. **Meets highest reliability standards**—Durable four-finger BeCu contacts and fully heat treated IDC tines insure gas-tight performance.
4. **High density low profile boards**—The "Q/C" board profile is only 0.235″ compared to the 0.703″ wrap/pin board. "Quick/Connect" boards go right into production racks.
5. **Wiring machines available**—The semi-automatic wiring machines now in use can be readily modified for the "Q/C" system. Also, semi-automatic "Q/C" machines are available.

This is not just a "dream" system. A major electronics firm is currently using the "Quick/Connect" system on a regular basis.

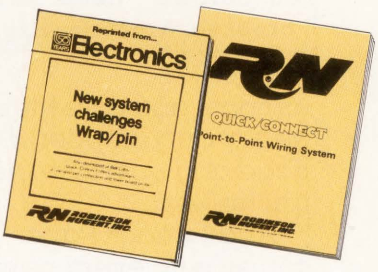


"Quick/Connect" socket boards, ready for wiring, are available in several standard configurations or can be developed to meet customer specifications.



Socket Terminal Sockets and terminals supplied on strips for easy board insertion.

Write or call today for full details on this new point-to-point wiring system that will obsolete wrap/pin boards. The time and money savings are truly phenomenal!



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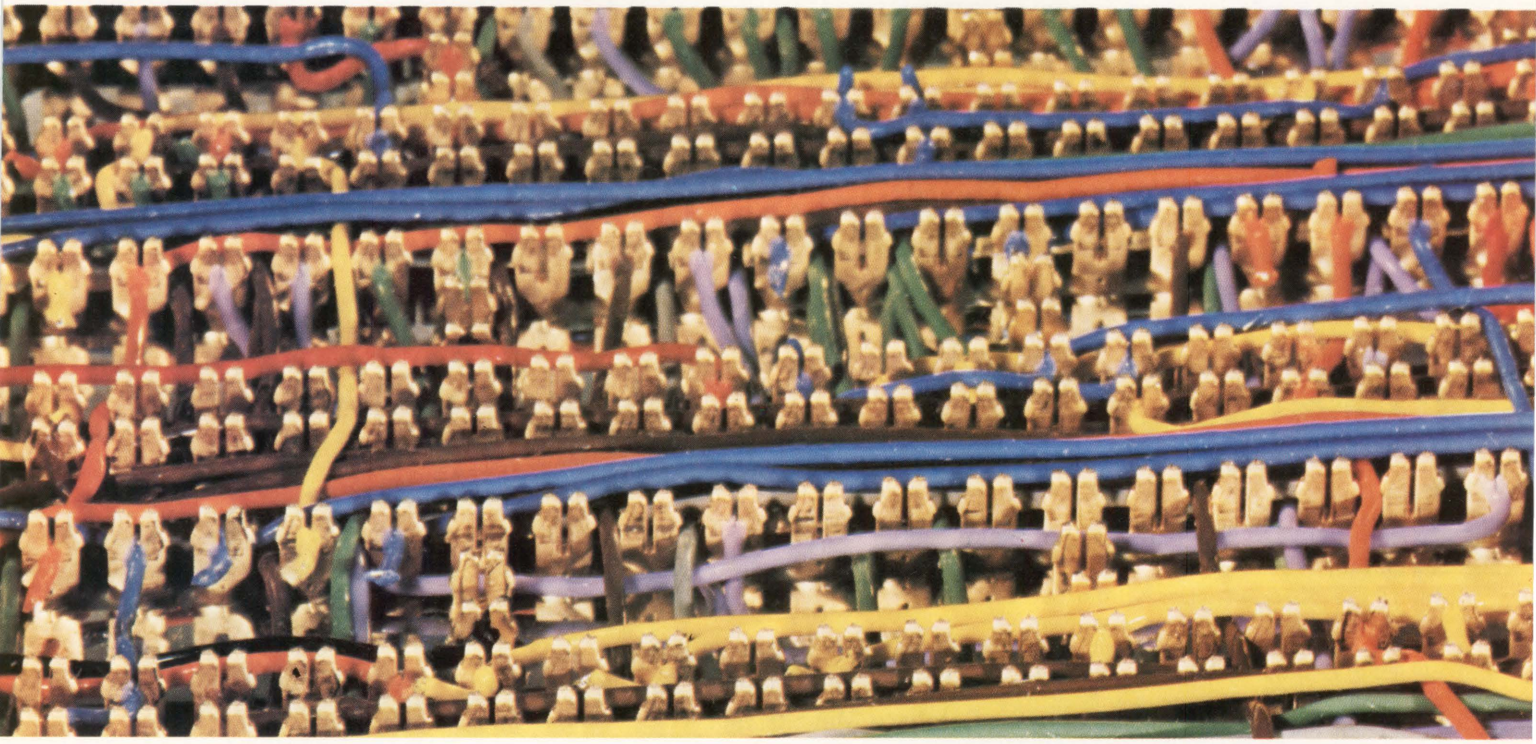

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SOFTWARE

Software Development Tool For PDP-11 Eases Programming Tasks

Central Software allows users to perform system development and maintenance functions interactively from a video terminal. Previously available only to IBM/CICS users, a version specifically designed for PDP-11 users has been released by Planning Research Corp, 1764 Old Meadow Lane, McLean, VA 22102.

The package includes up to eight levels of security controls, screen formatting, automatic edits, a database manager, and programmer/user aids such as online application programming, debugging, diagnostic aids, and message switching. By eliminating many of the redundant coding tasks usually associated with application programming, it allows programmers to concentrate on the quality of their realtime transaction processing logic.

Circle 367 on Inquiry Card

Terminal Application Processing System Makes Computers Easier to Use

An advanced version of terminal application processing system (TAPS) for 50-series systems increases productivity by simplifying operation and offers several levels of security. Available from Prime Computer, Inc, Prime Park, Natick, MA 01760, Prime/TAPS allows any application system to be moved to IBM or other equipment, making the system useful in distributed data processing.

The package consists of three basic modules: communication interface, program manager, and data manager. With the system, software applications can be developed faster than usual because the system performs many functions such as screen handling and file retrievals. Complete interactive business applications can be implemented without a single line of written code.

Circle 368 on Inquiry Card

Realtime Native Code Pascal Has Multitasking Extensions

Pascal compiler not only has extensions for realtime and multitasking operations but can communicate with modules written in other languages. Designed by Computer Automation, Inc, 2181 Dupont Dr, Irvine, CA 92713, for its Naked Mini 4 series of minicomputers, the compiler produces fast running native machine code that executes under both OS4 and RTX4 operating systems.

NM4 Pascal is defined as a superset of the proposed ISO draft specification for Pascal, and maximizes portability of existing Pascal applications to the company's processors. The compiler supports compilation and linkage of separate program modules written in Pascal, Assembler, or one of the other NM4 structured languages.

The compiler executes under OS4 on either NM4/10, 4/30, or 4/90 with 128k bytes of memory, rotating memory, terminal device, and line printer. Execution of the runtime can be under OS4 or RTX4.

Circle 369 on Inquiry Card

FORTRAN Version Extends Language's Power And Efficiency

Released by ADP Network Services, Inc, 175 Jackson Plaza, Ann Arbor, MI 48106, FORTRAN version combines features of previous FORTRAN versions with those of recent releases from DEC and adds features that enhance problem solving capabilities. More efficient than older versions, the package provides savings of up to 50% on some operations.

Among the features provided are dynamic arrays with an arbitrary number of dimensions for all data types; STRING data type with complete string handling capabilities, including concatenation, substring selection, and automatic conversion routine; and extended character set. Expanded free format source input statements, any number of subscripts on arrays, array bounds which may be negative or zero, and symbolic names for constants are also provided, as are compiler macro definitions. The compiler is able to read data written in any of the company's other programming languages, and offers comprehensive error checking and diagnostics, global optimization, and enhanced sequential and random access I/O capabilities.

Circle 370 on Inquiry Card

System Development Software Enhanced to Support Database Management

Application system development software Genasys Release 3.07 supports DBMS as well as the IBM 3800 laser based page printer. Available from Genasys International, Inc, 17 E 45th St, New York, NY 10017, the software automates major segments of application development from initial design through source code generation and final documentation. It helps analyst and user compile, review, and revise a design manual that becomes the basis for automatic generation of COBOL or PL/I source code. Final system documentation is generated automatically to support maintenance of the system once it has been implemented.

The release extends the maximum size of an overall database definition and expands support of the use of segment search arguments under IBM's information management system. Other changes allow ISAM type and sequential files to have records located in the file definition area instead of in working storage. Another enhancement enables the user to set any CICS attribute byte to any value desired.

Under the system, IBM's 3800 printer can be designated as the device on which the design manual is printed as well as the output device for reports from the system under development. The software runs on IBM compatible mainframes but produces source code that can be compiled and run on a variety of computer systems. Online design support under the Specifier package requires CICs.

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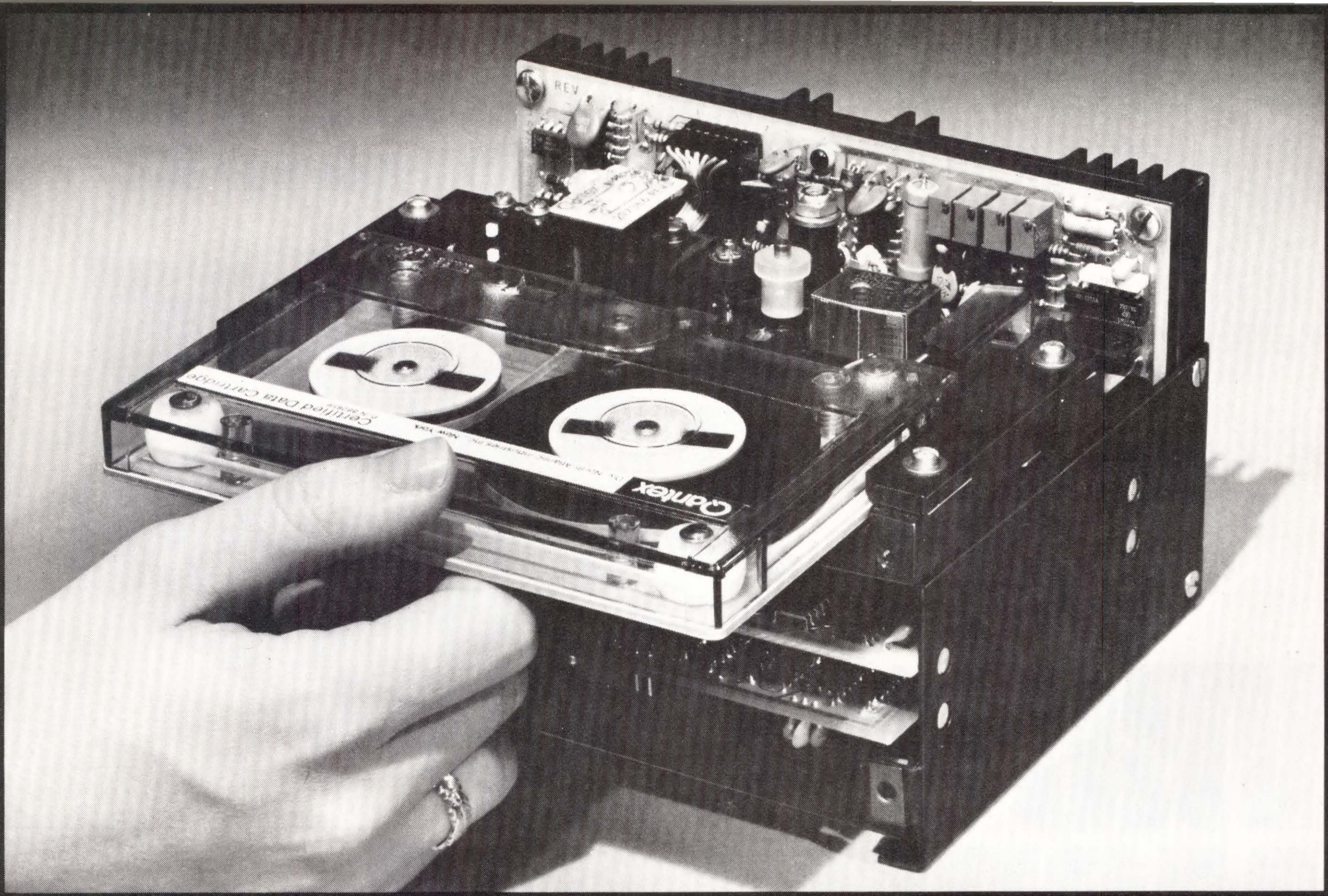
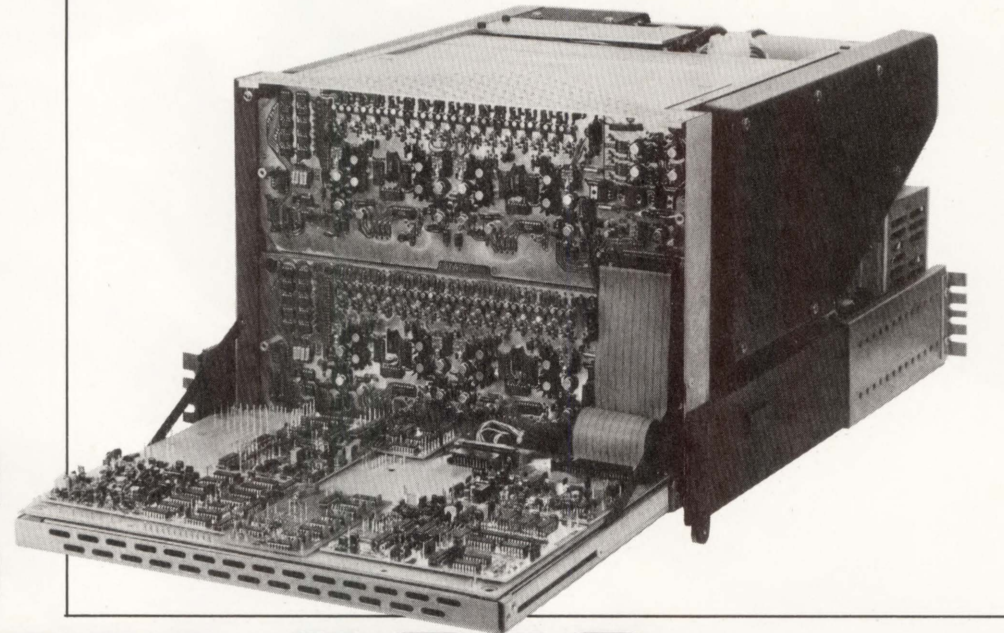
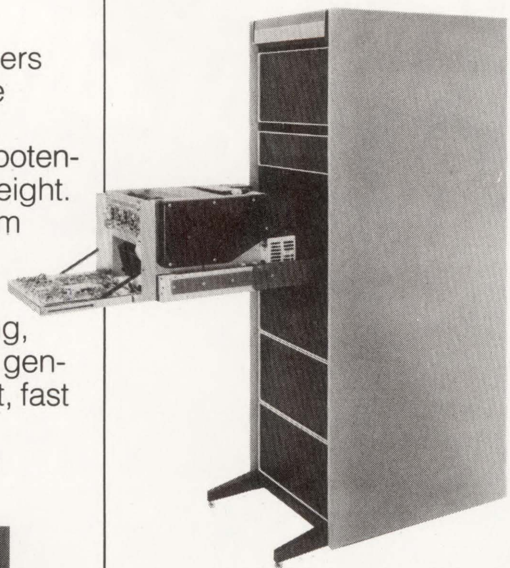


RELIABILITY: 28,000 hr. MTBF.
ECONOMY: .035 cents per bit.



VRC MODEL 4016 MEMORY

CAPACITY . . .	37.9 million bits
BIT RATE	4.33 MHz
ACCESS TIME	8.5 m/sec.
DIMENSIONS	Height – 12¼″ (31.2 cm.)
	Width – 17½″ (44.5 cm.)
	Depth – 22″ (55.9 cm.)
MEAN TIME TO REPAIR . .	Less than 1 hr.



When it comes to speed, reliability and low cost, systems users in 25 countries in every continent of the world depend on the VRC 4016 head-per-track memory.

It features a fail-safe actuation system that eliminates the potential of media damage and data loss. It's compact and lightweight. All electronics, drive components and head retraction system are mounted outside the drum, making service simple and eliminating risk of contamination.

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Automated System Combines Technologies for Production of Aircraft Structural Assemblies

A prototype robot assembly operation being conducted by Northrop Aircraft Corp, 3901 W Broadway, Hawthorne, CA 90250, under USAF auspices, will lead to automated processing of advanced composites for aircraft structural assemblies. Named the Integrated Flexible Automation Center (IFAC), this operation is currently in a semi-automated stage but is nearing full automation. The advanced composite operated upon in this work cell is pre-impregnated graphite, which, when laminated, attains a stiffness and strength approximately three times that of aluminum, at half the density.

Two earlier phases have been completed. First, each of the separate elements of the system was tested. Then, a semi-automated version of the system was put into operation. The current, or third, phase is directed toward full automation.

Borrowed Technology

In working with the pre-impregnated graphite fabric, the system utilizes techniques and instruments that originated in the garment industry. The fabric cutting is performed by Gerber System 91, provided by Gerber Garment Technology Inc, PO Box 664, S Windsor, CT 06074. This system, as utilized in IFAC, includes a modular cutting table consisting of four tabletops, 6 ft (1.8 m) wide and 10 ft (3 m) long, forming a tabletop 40 ft (12 m) in length.

The system also includes a high speed reciprocating needle-knife, oriented perpendicular to the tabletop and driven by a computer-directed positioning system that provides 3° of translational and 1° of rotational control. Programs entered into the system's dedicated minicomputer establish the set of ply shapes (menu) that are to be cut. The knife rides on a mobile gantry that travels on rails mounted on the table sides.

A second element from the garment industry, a material dispensing unit (MDU), operates in conjunction with the System 91. Furnished by Cutting Room Appliances, 201 W John St, Hicksville, NY 11801, the MDU rides on the Gerber rails, automatically unrolling fabric onto the cutting table. At the end of its excursion, it cuts off the unrolled sheet with the simple action of a cutting blade that follows a straight line path perpendicular to the longitudinal axis of the table. The MDU then returns to its home location at the head of the table, and the table area is ready for the reciprocating knife.

In the IFAC environment, the cutting table has been specially modified. The three tabletops at the foot of the table, where the plies are to be cut, have surfaces consisting of thick polypropylene bristles, approximately 0.125" (0.3 cm) in diameter. This bristle surface enables the reciprocating knife to cut through the fabric without damaging (or being damaged by) the tabletop. The tip of the blade merely bends the tip of the bristles out of the way.

Furthermore, these three tabletops are removable. After being raised by lifting devices, they are captured by carriages traveling on an overhead monorail system and taken to workstations, where the layups they contain are operated upon in preparation for subsequent curing, bonding, and lamination. Integration of these fabric machines and the monorail transport and the other workstations constitutes the semiautomatic system that now exists, as well as the fully automatic system under development.

System Overview

Eight elements make up the system (Fig 1), with a ninth to be added later. Four of these elements, the System 91, the MDU, the table lifting devices, and the monorail system, have already been described. Other elements in the system are a T^3 transfer robot, from Cincinnati Milicron, 4701 Marburst Ave, Cincinnati, OH 45209, a scrap remover, a video camera system for inspection, and a central minicomputer. The element to be added is a rotating platform (analogous to a "lazy Susan") that can reorient a tabletop when the need arises.

Operating under semi-automated or fully automated control as described in the following sections, the system functions as follows. The MDU lays out the fabric, and the reciprocating knife cuts it into preprogrammed plies. After the table lifters raise the tabletops and the carriages of the monorail system pick them up, the next stop in the monorail system is the transfer robot station. The robot, modified to use differential air pressures to pick up selected plies, transfers the plies from the tabletop to the surface of a curing/bonding fixture. After leaving the robot station, the carriage docks in the scrap remover, where surplus bits of pre-impregnated graphite (prepreg) are removed. Video inspection is carried out by cameras, operating in the vicinities of the various workstations to monitor material dispensing and cutting operations, menu configurations, and scrap removal. The inspection system, designated as automated inspection evaluation system (AIES), provides an online realtime quality assurance capability for the cell.

Since the reach of the robot arm does not extend to the far edge of a tabletop, some potentially advantageous menu configurations could not be handled by the present system. For this reason, the table rotating station is to be added. After a tabletop has initially left the robot station, it could be taken to this additional location in order to be

(continued on page 88)

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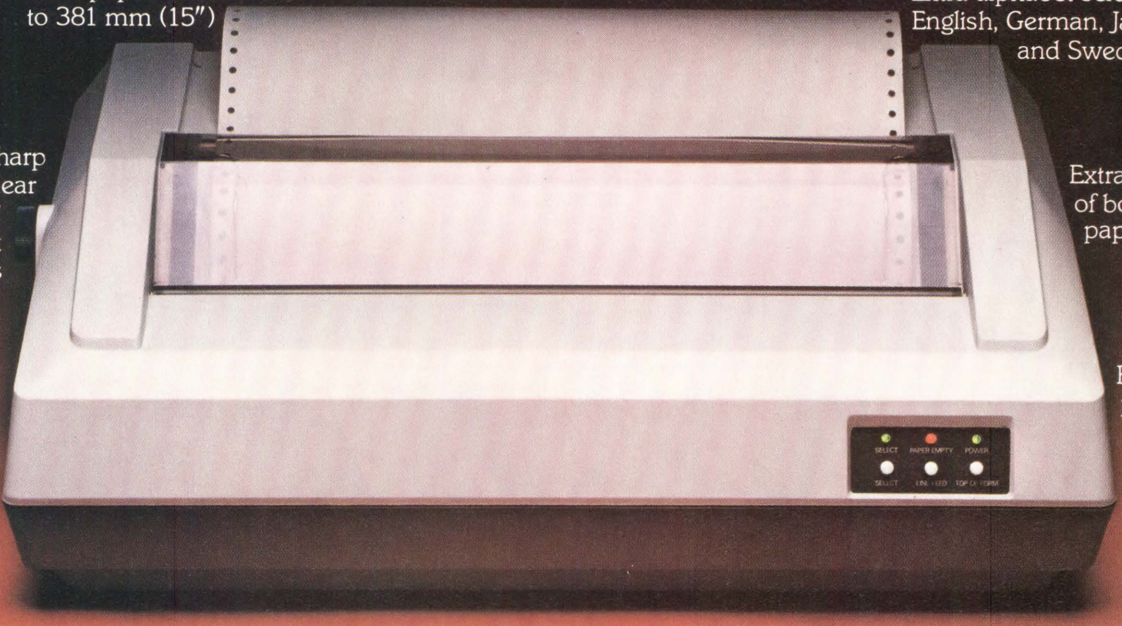

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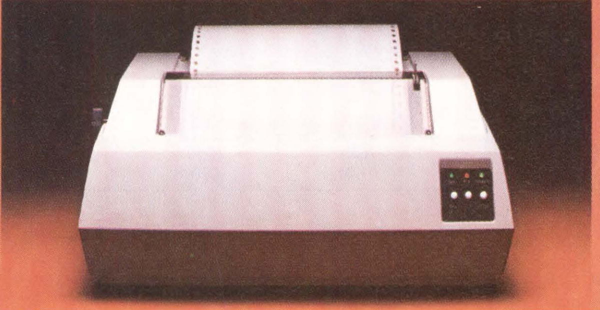

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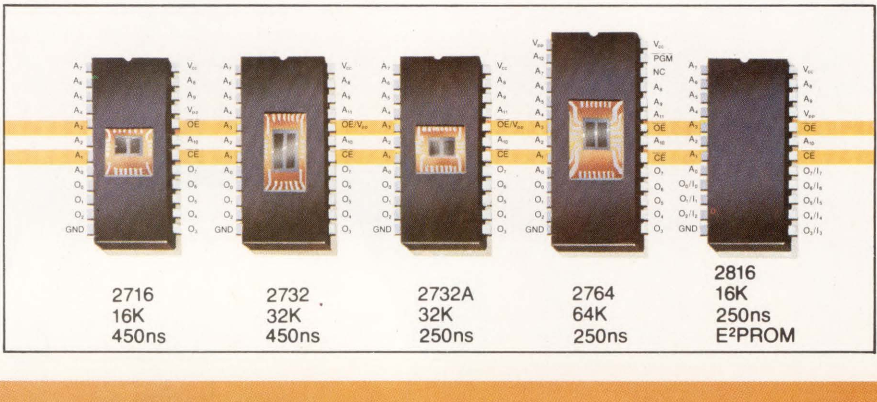

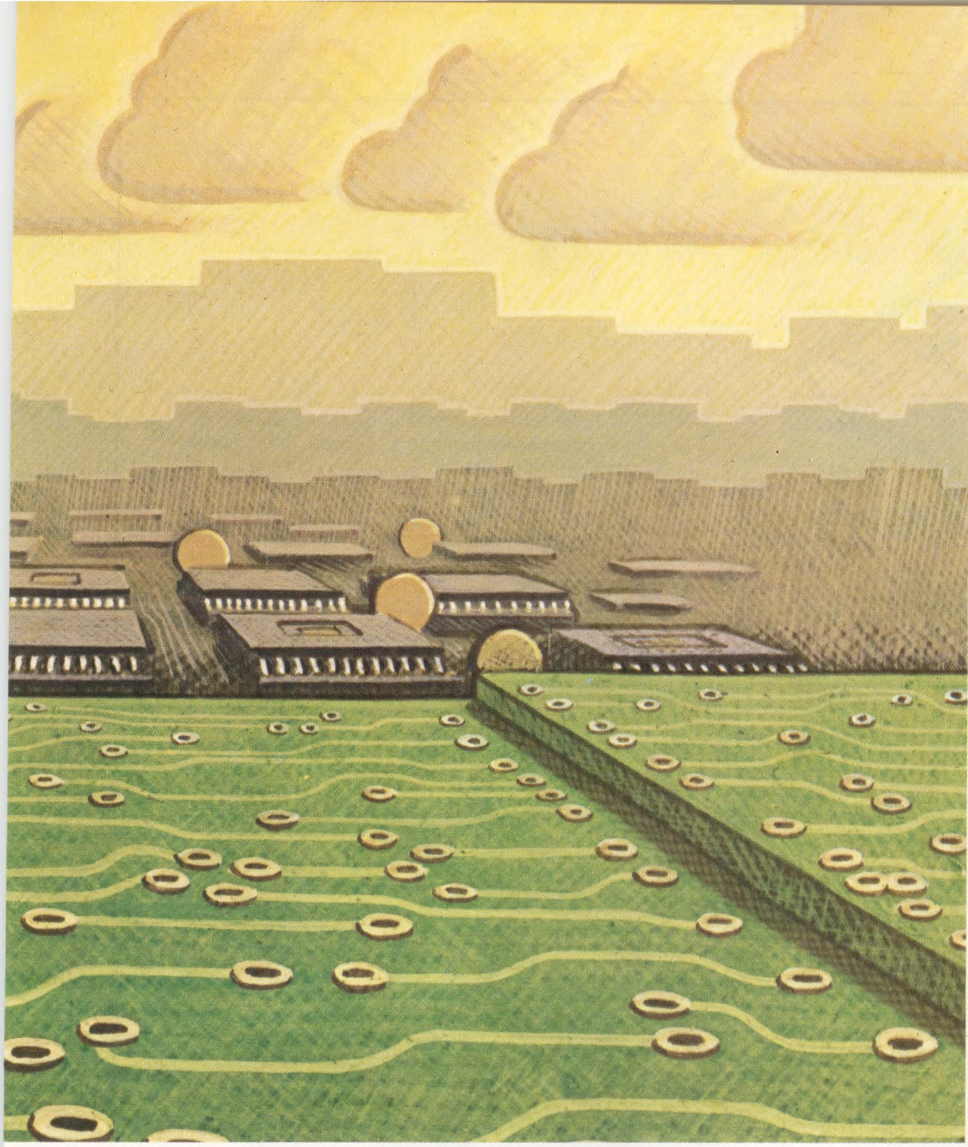

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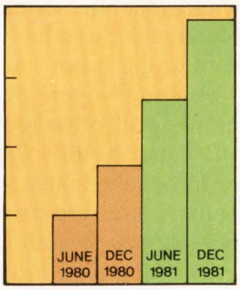

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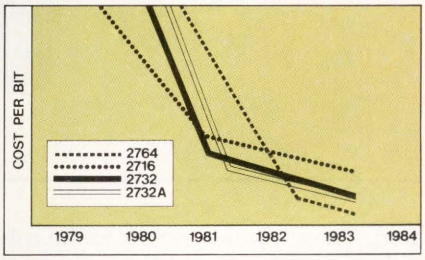

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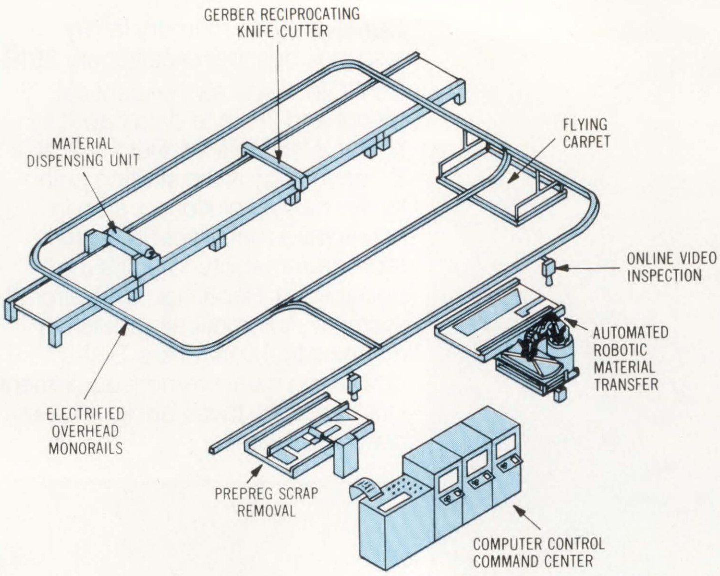

Fig 1 Artist's conception of IFAC. Carriages designated as flying carpets transport detachable tabletops to series of workstations

rotated. Then it would return to the robot station to present the formerly unreachable plies to the robot.

Semi-Automated Operation

In the present operating mode, the central computer in the IFAC cell is a Raytheon 704 minicomputer, whose sole function is to govern and monitor the ply-selecting operations of the robot. The robot operates under divided control, since its lifting and transporting operations are governed by the dedicated minicomputer provided by the manufacturer of the robot.

Selection of plies by the robot is accomplished through the use of the differential air pressure system that has been added. Six flexible air ducts lead from blowers to a head affixed to the terminal end of the robot arm (Fig 2). There are two plenum chambers in the head, one maintained at positive and the other at negative pressure relative to the atmosphere. Selection of one or more specified plies from a nest of several plies requires that the head present a negative air pressure to the selected plies and a positive pressure to those plies that are not yet selected.

A matrix of valves in the 250-lb (114-kg) head presents either positive or negative pressure to each of 145 perforated sectors, measuring 4 in^2 (26 cm^2), on the face of the head. The central computer monitors all valve positions and presents (on a CRT display) the locus of all valves that are pulling vacuum. It also controls a panel of LEDs, corresponding to the valve matrix, with *on* indicating negative pressure, *off* indicating positive pressure, and *blinking* indicating a diagnostic.

The robot's dedicated minicomputer is programmed to transfer each ply to its correct location on the tool bed. When a layup on the tool bed has been completed, it is carted into another (not yet automated) part of the plant, where curing, bonding, and laminating are performed. Meanwhile, another tool bed is moved into position adjacent to the robot station.

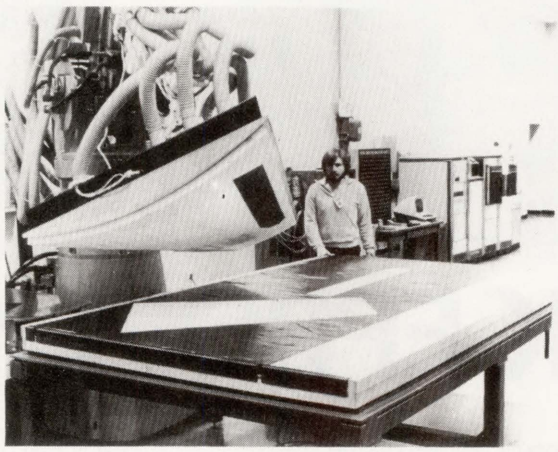

Fig 2 Cincinnati Milicron T^3 robot. Modification allows selective pickup of fabric plies. Vacuum draws selected plies to head, while positive air pressure prevents acquisition of plies not yet selected. Black strip on face of head is ply that robot has acquired

A system operator, working at a console, initiates and monitors all other aspects of the operation. He orders the MDU to begin dispensing material, orders the reciprocating knife to cut according to its preprogrammed pattern, and orders all events related to the movements of tabletops to and from various workstations.

The operator monitors the visual displays, including the CRT and LED panel relating to valve settings. He also

(continued on page 90)

monitors a display that is part of the AIES that presents the visual field seen by whichever of the system's cameras has been selected at the console.

Three cameras are located at the robot station. Before entering this station, each carriage is stopped for inspection by an overhead camera to establish that the menu of plies is correctly configured with regard to the assortment of shapes and their locations. When the operator has verified the correct menu, he allows the tabletop to be placed on the robot work table.

As the robot arm transports the selected ply toward the tool bed, it is stopped in midswing. During the pause, a second camera, located in a casing on the floor, photographs the ply arrangement on the head to allow the operator to verify that the menu has not been perturbed during selection. A third camera subsequently provides a view of the menu as placed on the tool bed for a final verification.

An additional camera is located near the scrap remover, which consists of a docking framework equipped with a brush arm. This brush arm is maintained in a cocked position to avoid interference with the approaching carriage. When the carriage docks, it activates a microswitch that lowers the arm so that its brush engages the bristles of the tabletop. The operator then commands the carriage to exit from the scrap remover, and the exit motion automatically sweeps the tabletop. A second microswitch is activated by the carriage's departure from the dock, and this resets the brush arm into the cocked position.

At this point, the carriage is halted under the nearby camera, and the operator can verify that no scraps are present. If scraps are present, the carriage is commanded to reenter the scrap remover.

Fully Automated Operation

Virtually all of these control and monitoring operations are to be brought under control of a new minicomputer that is to replace the existing central computer. This minicomputer is the SEL 32/77 from Systems Engineering Laboratories, 6901 W Sunrise Blvd, Fort Lauderdale, FL 33313, offering 256k bytes of RAM, and peripherals that include an 8M-byte disc drive, a magnetic tape drive, a band printer, and a card reader. Among the functions carried out by the computer will be video to digital conversion of all camera information. This computer will readily interface with a wide spectrum of mainframe computers if it is found advantageous to tie it into a data base or general plantwide operation.

The fully automated system will incorporate an additional camera mounted on a gantry that will ride on the rails of the Gerber table just behind the MDU. Utilizing a wide angle mirror to view the entire 5-ft (1.5-m) width of

(continued on page 92)

the fabric, this camera will scan the fabric as it is dispensed, in order to locate defects. A microprocessor, located on the MDU, will notify the central computer of the location of any significant defect, and the central computer will instruct the Gerber knife minicomputer to adjust its cutting program to avoid the defective area. This microprocessor will also inform the central computer as soon as it clears each section of table during its travel back to its home location at the head of the table, so that the reciprocating knife gantry can be ordered to work without the hazard of a collision between these two moving elements. Similarly, the reciprocating knife minicomputer will notify the central computer when it has joined the MDU at the head of the table. This will free the space above the table for the passage of the carriages along the monorail system, to return empty tabletops or collect full ones.

When a tabletop containing a menu is ready to be picked up (as indicated by the completion of cutting and the return home of the reciprocating knife), the central computer will direct the table lifting devices to raise that tabletop to a height governed (as is also true in the semi-automated mode) by preset microswitches. An approaching carriage will generally be in motion toward this tabletop before the latter has reached its fully raised position. However, the tabletop will be at the raised position when the carriage arrives, and the carriage will automatically collect it on flanges that (again, as in the semi-automated mode) will slide under the side edges of the tabletop.

Consisting of 230 linear ft (69 m) of electrified track, the monorail system is configured as a large loop subdivided into two subloops and a sidespur (Fig 3). In the fully automated system, the monorail will contain a monorail communication system (MOCS), enabling the central computer to know the locations of all carriages, to send commands to each carriage, and to operate railroad-type switches at branch points of the monorail. This will enable the system to shunt a carriage off into a standby position on a sidetrack if the rail or station immediately ahead is occupied by another carriage.

At the robot transfer station, the central computer will again perform video to digital conversion in order to process the camera data. As one example of the speeding up that will result from the full automation, the robot will pause for only 1/60 s in order to let the upward looking camera verify the menu that it is transporting. The video to digital conversion will be facilitated, at all camera locations, by the contrast specifically provided between the white polypropylene bristles of the tabletop and the black fabric.

Control of the robot will be quite similar to its present definition, with transport motions governed by the dedicated minicomputer and valve status governed and monitored by the central minicomputer. The same downward-looking camera that verifies the menu on the tabletop (prior to robot acquisition of selected plies) will also provide the central computer with verification that the plies have been removed and that the robot head is away, before a signal is sent through the MOCS ordering the carriage to retrieve the tabletop for transport to the scrap remover.

At the scrap removal station, the process will be facilitated by signals from the station's microswitches to the central computer. A signal from one microswitch will inform the computer that the carriage has docked and that the brush arm is lowered. The computer will respond by ordering the carriage to vacate the dock, and then the second microswitch, as it returns the brush arm to its

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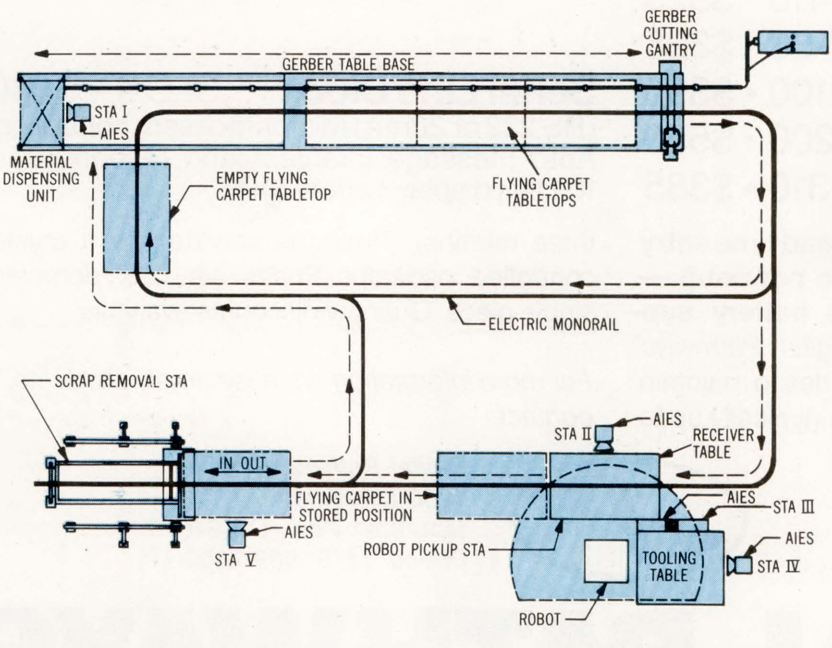

Fig 3 Diagram of IFAC. Design of monorail system enables switching of flying carpet carriages onto alternate paths to avoid traffic problems. Operations are monitored by AIES visual feedback system

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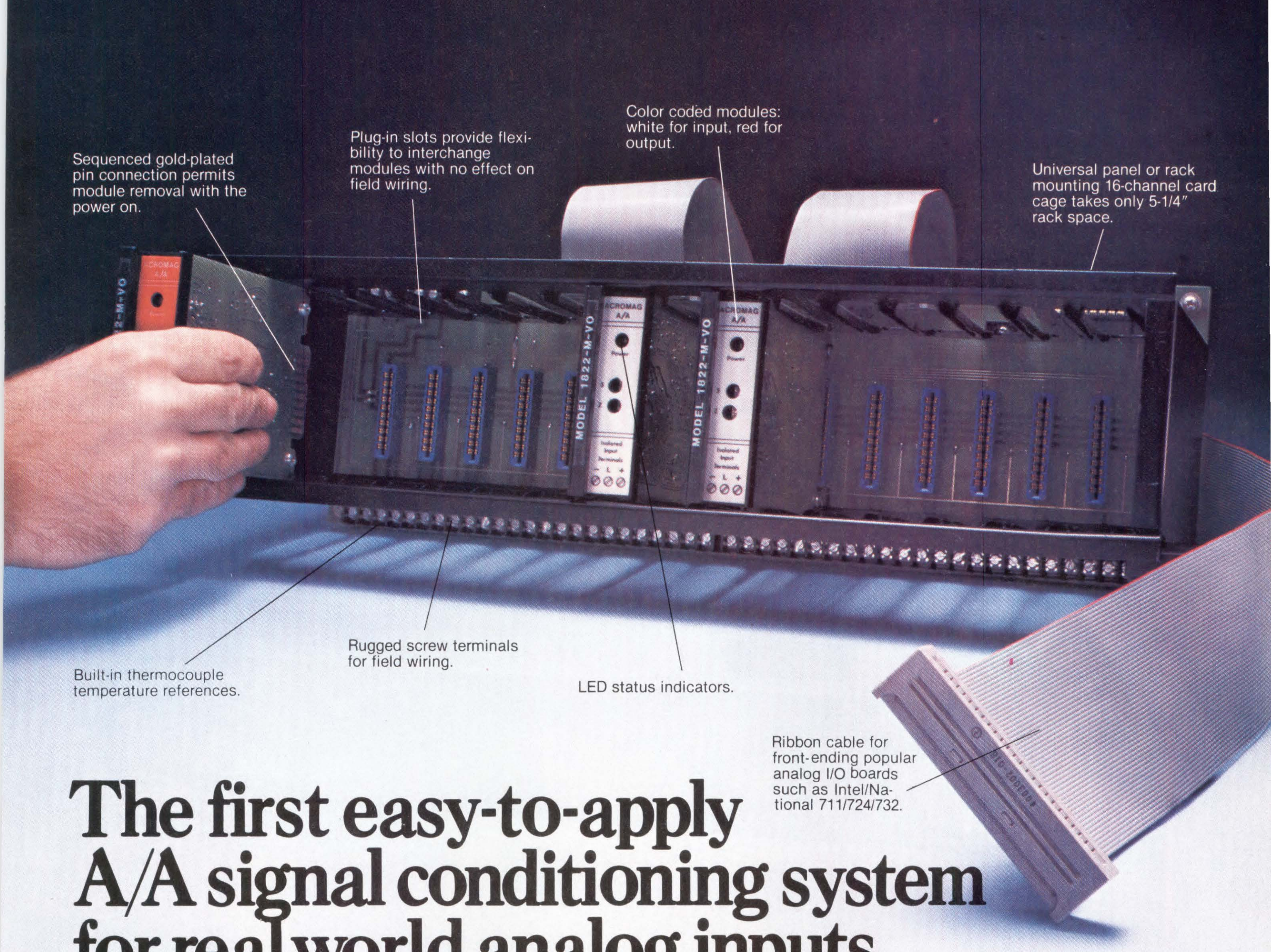

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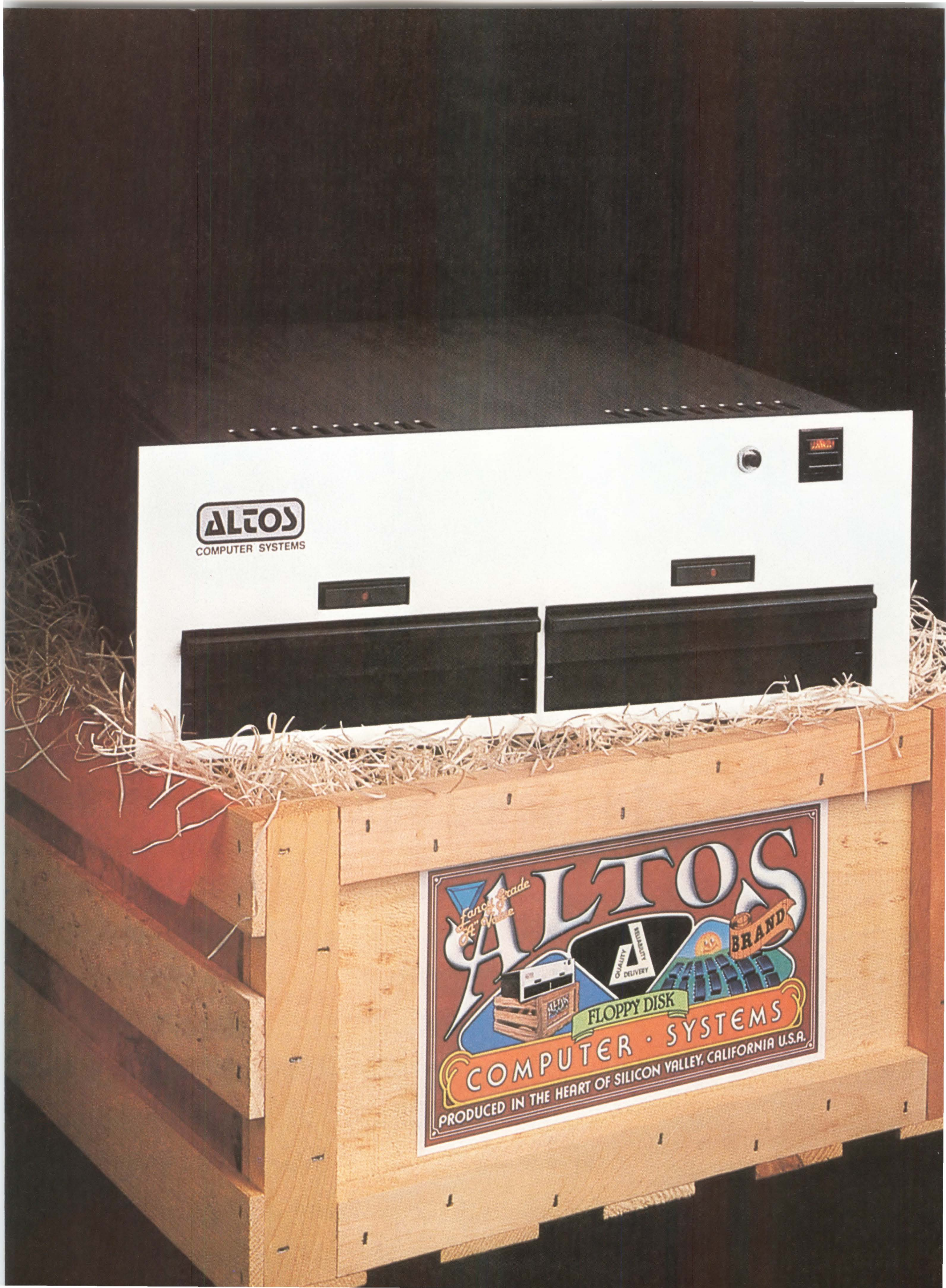
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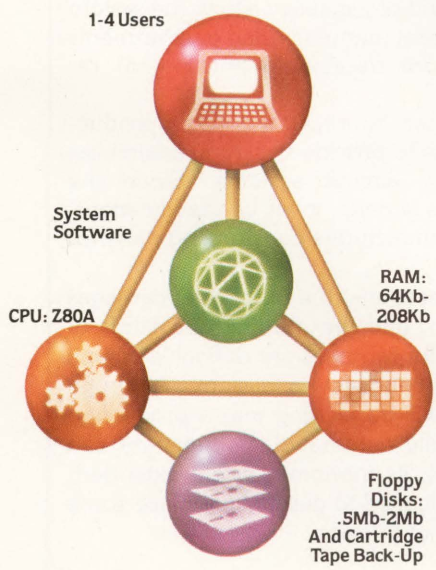

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cocked position, will validate the completion of this action.

If the AIES, sensing the field of view of the next camera, indicates the persistence of scrap on the tabletop, the central computer (emulating the function previously performed by the operator) will order the carriage back into the scrap remover. After a preprogrammed number of unsuccessful transitions (perhaps three) through the scrap remover, the system will signal to the operator, requesting intervention.

Once the scrap removal has been successfully accomplished, the central computer (having verified that the path is clear of both gantries) will send the clean tabletop back to a location above a vacated section of the cutting table. The table lifting devices will rise to support the tabletop, the carriage will disengage and move away, and the table lifters will descend to position the tabletop on the table, ready for the MDU to pass over it, dispensing another sheet of fabric.

Summary

Manufacturing of structural assemblies through use of advanced composites has been under way for some time now in various aircraft plants. However, IFAC represents a change in this production process by moving in the direction of full automation. This prototype system has not yet been integrated into the production process but is being used to demonstrate the feasibility of the approach, as well as to prepare for actual implementation on a production basis. Upon conclusion of phase three of the program, the system will be tested through the fully automated production of 40 horizontal stabilizers. After the successful completion of this test, it is anticipated that the automated work cell could be fully integrated into the plant's production of advanced composite parts.

Flexibility has been an important factor throughout the development of this system. One of numerous examples is the operation of the table lifting devices, whose excursion height is variable, as a function of microswitch positioning, rather than being fixed at the maximum extension of the lifters. This kind of variability allows the system to be configured to different manufacturing environments and to varying (and not necessarily anticipated) requirements.

IFAC, when verified, can be integrated into a production manufacturing mode to provide structural assemblies for today's and future aircraft systems. Since the automated technology is generic, it will be readily adaptable to use by other manufacturers constructing parts for different vehicles.

The number of table sections, the number of carriages on the monorail system, and the number and kinds of workstations visited by the carriages are definable by any manufacturer implementing such a system. Although IFAC, as defined now, will be feeding into a production area that is itself not fully automated, its functions can potentially be expanded, its monorail system extended, and its workstations multiplied to gradually replace some (or all) of the facilities that it feeds.

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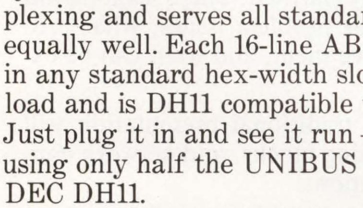

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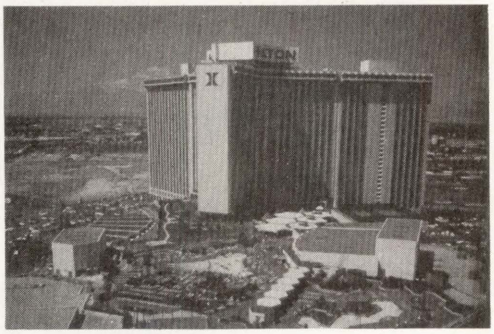


Las Vegas Convention Center
Las Vegas, Nevada
March 30 - April 2, 1981

INTERFACE '81, the ninth annual conference and exposition devoted to data communications, distributed data processing, and networking, will feature a 56-session technical program including 10 Special Focus half-day seminars. Regular sessions, 90 to 120 min each, will be organized in 15 subject groups such as Information Productivity, Network Productivity Strategies, Data Communications Interfaces and Standards, Network Control Solutions, and Peripheral Trends, as well as the conference's traditional "Datacomm School." Special Focus seminar topics will include Distributed Data Processing Futures, Network Security, Satellite Strategies, Fiber Optics Link to the Future, Local Network Developments, SBS and Its Alternatives, SNA '81 Update, Office Systems Planning, A View Toward Business Graphics, and Technology for Tomorrow.

Program committee chairmen will include Max Beere, vice president, ICS Group, Inc; Ralph Berglund, senior partner, Berglund & Smith, Consultants; A. A. (Tony) Carlson, manager-data networks, U.S. Senate Computer Center; Richard L. Deal, president, Richard L. Deal & Assoc; Dixon Doll, president, DMW Group; Leonard Elfenbein, president, Telecom Systems Group; Howard Frank, president, Network Analysis Corp; and Gil Held, chief-data communications, U.S. Office of Personnel Management. Nearly 100 additional speakers will round out the panels for both regular and Special Focus sessions.

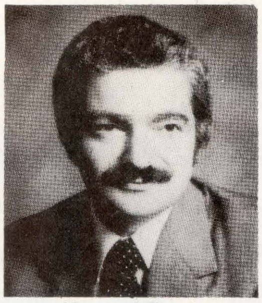
Technical Program Regular Sessions

All regular sessions on the conference program will be presented in the following groups, with particular stress on the conference theme areas. Conference management states that because "such functions as the acquisition, processing, storage, retrieval, and communications of information blend into each other in increasingly complex systems,... INTERFACE '81 will encompass additional areas of information resource management, including office automation."

Information Productivity: Convergence is Key—This group of sessions will relate information productivity to corporate growth and define the requirements that must

Program Committee Chairmen

Ralph Berglund



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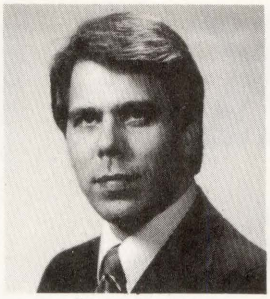

A. A. Carlson

Dixon Doll

Richard L. Deal

be understood prior to planning. It will also cover the integration of solutions into information resource management and the criteria to be considered before making decisions.

Integrating Information Resources—Changes in information processing and communications procedures offer potential for improving the handling of data. Speakers will alert attendees to the integration movement and discuss the issues involved.

Issues of the Information Industry—The merging of computers and communications and the resulting confusion and turmoil in Congress, Federal agencies, and the Courts still are not fully clarified. These sessions will update attendees on major problem issues, what progress is being made to solve them, and what can be expected in the near future.

Datacomm School—This traditional presentation will cover fundamentals, building blocks, and network concepts for data communications.

Network Productivity Strategies—Understanding the approaches to network architecture is a requisite to the design and functioning of productive networks. Adding either new features or new applications can result in degraded service if the approaches are not clear.

Datacomm Interfaces and Standards—In these sessions, the speakers will explain how to get more out of

(continued on page 100)

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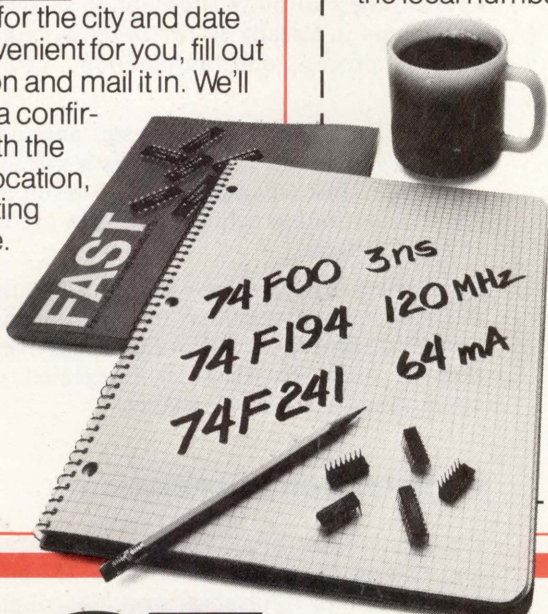

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modems and multiplexers and discuss port contention alternatives.

Public Networks: A Bridge to the Future—Speakers will update information on extended network services and will identify the impact that home information services will have on the industry.

Network Control Solutions—Current structural network architectures may include local, distributed, and private to public nets, but all require full network control. New systems and networks being introduced will solve many existing problems.

International Networking—Although many multinational companies would like to arrange networks that encompass all the countries in which they have branches, such international networks bring out new challenges. Idiosyncracies and differences in regulations are major problems for datacomm professionals, and some regulatory issues have blocked progress.

The Emerging Integrated Office; Word Processing: An Integral Function; Mainframe in Transition; and *Data Base Developments*—Panelists will discuss each of these subjects in detail, pointing out technological advances, new issues of interest, and methods of using the techniques to advantage.

Peripheral Trends—All datacomm environments (whether network, automated office, or information transfer) have always been dependent on peripherals. This dependency is growing rather than abating, and persons in the field must be aware of the latest developments.

Digital Communications Impact—This group of sessions will cover progress in digital communications, digital pathways now available, and preparation for a digital future.

Focus Sessions

Speakers at each of the half-day focus sessions will discuss current technology, expected advances, and potential value of updating existing systems. In particular, they will identify areas that should be of concern to the system designer.

Distributed Data Processing Futures—As with all advances in technology, DDP retains the potential for creating as well as solving problems. Progress has been made in avoiding the difficulties inherent in the implementation of DDP and in implementing strategies for hardware/software interaction.

Network Security—Whether a network ranges around the world or is limited to a single building, maintaining the integrity of confidential or proprietary data on that network is a must. Such security can be attained through a variety of technological and management approaches.

Satellite Strategies—Advances in both technology and application of satellite data transmission are not always used to full advantage. Incomplete understanding of how accelerated services of satellites and ground stations can benefit networks can cause many users to fall behind.

Fiber Optics Link to the Future—The first communications application for fiber optics, which involved only carrying voice, has become relatively minor of value. Semiconductor laser and LED beams now carry data in both extensive high speed and local transmission networks. In addition, designers now incorporate fiber optics technology in modems, multiplexers, switches, controllers, and peripherals.

Local Network Developments—Whether limited to one building, part of a building, or several buildings, local networks are vital concerns in maintaining the high speed digital links required for office automation/information systems. Short haul modems, fiber optics, and other products simplify the problems met by designers of local networks and bring about measurable cost savings.

Technology for Tomorrow—Many of the major problems that now exist in the design of data communication systems will likely be solved soon through further integration of digital technology. Knowing what is likely to be available within the design period of a system is an absolute must for the designer of that system.

SBS and Its Alternatives—Although satellite business systems have seemingly won over AT&T's advanced communications systems (ACS) network and the Xerox XTEN network for large user organizations, there is a question whether SBS is practical for smaller amounts of data traffic. In particular, broadening the service to include voice traffic results in the need for more knowledge about SBS for both large and small users.

The View toward Business Graphics—Because of the ease and speed of recognizing and interpreting information viewed on a color CRT display as opposed to reading through reams of computer printouts, executives are pressing for more use of such graphics. Interest in these displays is becoming as avid for business systems as it already is for other systems such as industrial process and automation, and information display.

SNA '81: An Update—IBM's recent announcements may have an impact on that company's system network architecture. Just what changes will result and the trends for the continuing evolution of SNA are of importance to all SNA users.

Office Systems Planning—Piecemeal automation of office systems may create as many problems as it solves. System designers should evaluate the overall organization in order to view an integrated office before attempting to make any changes.

Registration Information

Registration fee for all four days of conference sessions and exhibit floor admission is $125, and 1-day conference/exhibit floor admission, $65. Exhibits-only admission, for those who want to visit the over 200 companies with displays, is $10. For futher information contact The Interface Group, 160 Speen St, Framingham, MA 01701. (Tel: 800/225-4620 from outside Massachusetts and 879-4502 from within that state.)

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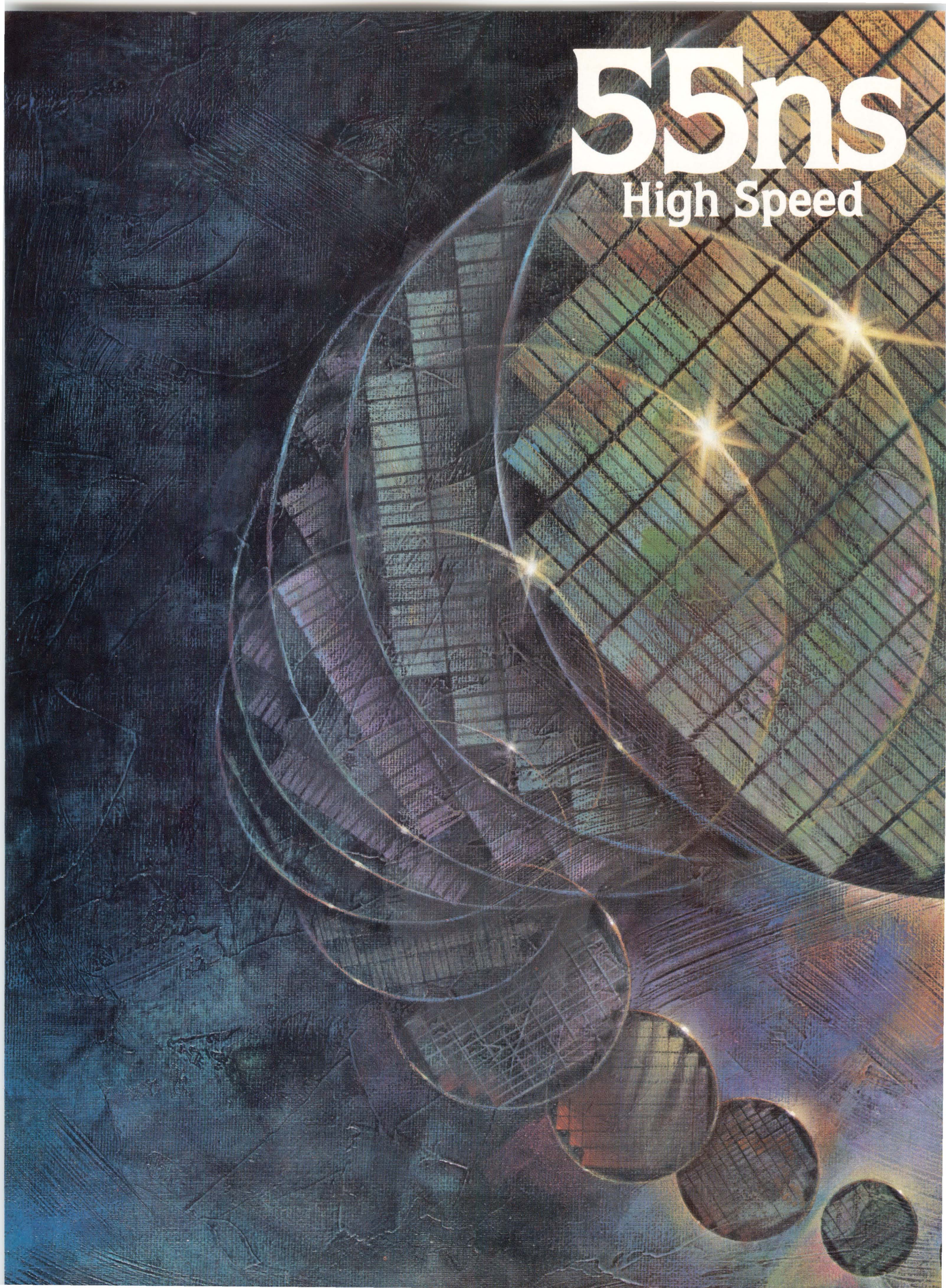
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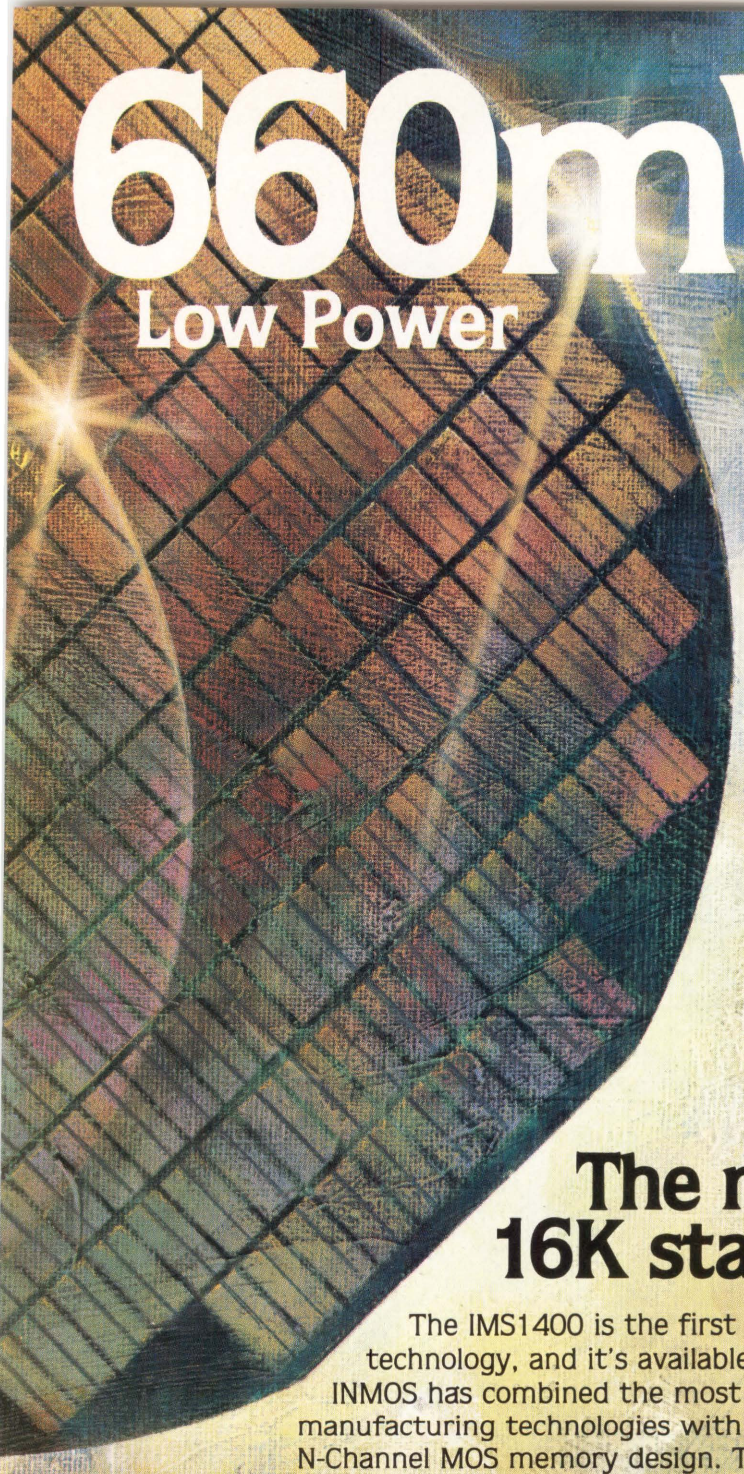

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I/O SUBSYSTEM USES IDLE CPU RESOURCES

Integrating channel functions into a small system CPU eliminates need for a separate special purpose I/O subsystem processor

Paul Hain IBM Deutschland GmbH
Schönaicher Str 220, 7030 Böblingen, Federal Republic of Germany

Data transfers to and from input/output devices and input/output command handling require powerful computing during short intervals. In small systems supporting only a few input/output devices, this computational power is needed only a small part of the time. An economical system implementation services input/output devices by using as many functional components of the central processing unit as possible, thereby integrating input/output channel functions into the central processing unit. Although different input/output devices require various physical interfaces, the system architecture uses only one logical interface to access all devices. Therefore, an economical system implementation also services the various physical interfaces by using as many common resources as possible. The design of the IBM 4331-1 processor illustrates channel services that are integrated from these viewpoints.

Dedicated on request to channel related microprogram routines, the central processing unit provides hardware for the transfer of input/output (I/O) data to and from main storage. Special processor functions and hardware components simplify and accelerate channel tasks. These include hardware data transfer support, special microinstructions, an addressing mechanism for fast access to control information, and an internal interrupt system for fast microprogram swaps. An integrated channel bus serves as the common medium used by all I/O devices to transfer data to and from main storage and exchange information with the microprogram. I/O adapters connect the integrated channel bus to various interfaces: a standard channel interface for attachment of I/O devices via control units, a direct controller interface for direct attachment of disc and tape units, and a programmable interface for universal controller subsystems or telecommunication attachments.

I/O Subsystem Tasks

A data processing system can be viewed as consisting of three logical parts: a main storage, an instruction processing unit (IPU), and an I/O subsystem. The I/O subsystem can be further divided into one or more I/O channels, control units, and I/O devices (Fig 1). The IPU obtains programmed instructions and data from main storage, and returns the results produced during processing to main storage. The I/O subsystem helps to keep the IPU fully occupied by transferring programs and data between main storage and such I/O devices as discs,

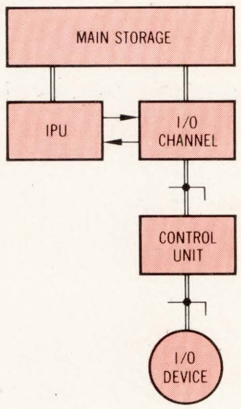

Fig 1 System block diagram. Data processing system consists of instruction processing unit and I/O subsystem, both connected to main storage. I/O subsystem moves programs and data into storage. IPU executes programs and requests transmission of results from storage to I/O device

tapes, printers, or terminals. Channels perform the actual data transfer by executing channel control programs that are kept in main storage as chains of channel control words (CCWs). Control units individually adapt standard device interfaces, according to specific I/O device requirements, to achieve communication between the channels and the I/O devices.

Communication between the IPU and a channel is carried out by I/O interrupts and I/O instructions that the IPU executes in series with data processing instructions (Fig 2). When a Start I/O (SIO) instruction arrives in the IPU instruction stream, the IPU gives control to the channel, passing it a device address and a pointer to the channel control program (the channel address word, or CAW). IPU instruction execution then resumes while the channel concurrently uses control units to communicate with the designated I/O device and to transfer data to or from main storage. Upon completion of the I/O operation, the channel interrupts the IPU instruction stream to return status information.

Throughput considerations require the IPU to execute a certain number of instructions within each given time period. Because execution time varies among instructions, performance is measured in millions of instructions per second (MIPS) using a long-term average that assumes a typical mix of operations. Within any time period, the number of I/O instructions and CCWs to be handled, and the number of bytes to be transferred by the I/O subsystem, can be derived from the MIPS rate of the IPU and certain characteristics of the task being performed. However, both the time available for the channel to handle a single CCW (the channel turnaround time in Fig 2) and the time to transfer a byte of data depend on physical characteristics of the I/O device and its control unit.

In a modern general purpose computer, most channel activity involves disc storage devices whose data rate largely determines I/O subsystem performance requirements. For example, on a small processor such as the 4331-1, about 250 CCW/s must be handled, and about 100k bytes/s must be transferred, depending on the MIPS rate and assuming a typical job. This leaves, on the average, 4000 μs available for one CCW and 10 μs available for one data byte. However, a disc drive with a 40-μs gap between data fields and a 1M-byte/s data rate requires CCW handling (for chaining in a gap) within 20 μs and data byte transfer within 1 μs. In view of the multiple I/O devices running on different channels at the same time, the I/O subsystem must perform hundreds or thousands of times faster than would be expected from average throughput figures.

I/O Subsystem Implementation

Several implementation schemes can achieve the required I/O subsystem performance. One method is to install one or more dedicated channel processors that realize the advantages of modularity and increased data capacity. However, because each channel processor must be able to accomplish its task within about 1% of

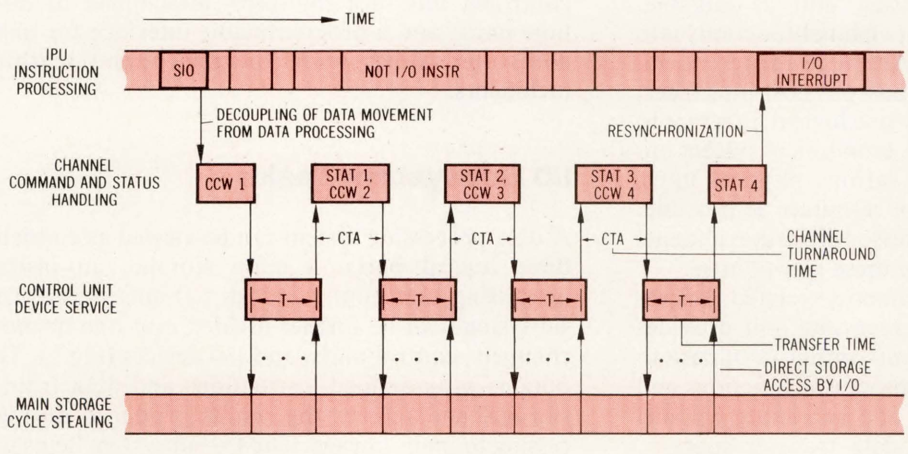

Fig 2 I/O device service diagram. Initiated by SIO instruction, I/O handling is decoupled from instruction stream to proceed in parallel, at rate determined by device speed and channel turnaround time, until interrupt signals that operation is finished and resynchronizes device service with instruction processing

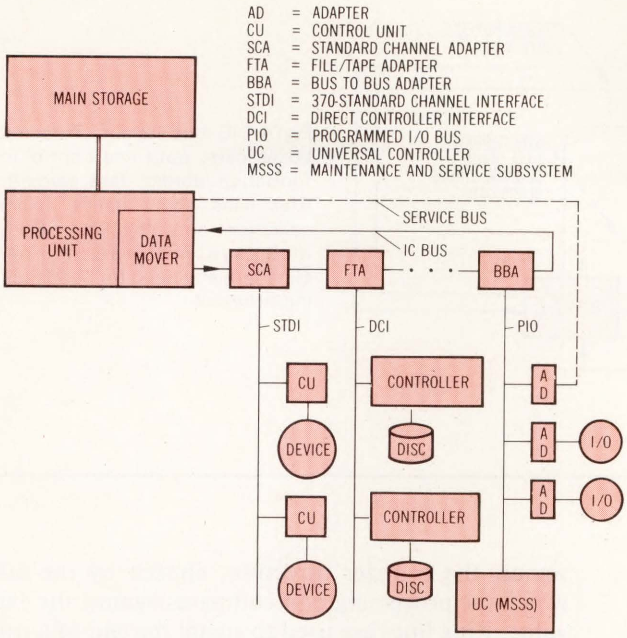

Fig 3 I/O device hierarchy. Common IC bus connects processing unit and main storage to various I/O adapters. These, in turn, service I/O devices through control units (standard interface), controllers (direct control interface), or I/O subsystem (programmed I/O bus)

the available time, this approach increases the amount of idle hardware. An alternative method extends the channel processor capability by incorporating control unit functions to achieve an I/O processor that attaches to I/O devices directly. This technique sacrifices the advantage of standardized interfaces for connecting I/O devices and their controllers. Yet another solution integrates the channel tasks into the IPU. This single-processor solution leads to the best use of existing hardware, but it requires extended IPU capabilities because IPU hardware and microinstruction sets, designed to execute machine instructions, usually will not suffice to perform I/O channel tasks. Nonetheless, this last approach, that of the integrated channel, was selected for the 4331-1 processor I/O subsystem (Fig 3).

Channel Bus

A general purpose computer must accept various numbers and types of I/O interfaces. Physical considerations (eg, packaging and I/O pin limitations) make it impossible to provide all types of interfaces directly on the processor; therefore, in the 4331-1, the integrated channel bus (IC bus) serves as a common path for transferring data and control information between the processor and individual adapters. Different I/O configurations are realized by attaching various adapters to the IC bus.

Physically, the IC bus is built up of ring buses and star lines. Starting and ending at the processing unit, the two ring buses provide a 2-byte data path and a 2-bit control path for up to six adapters (Fig 4). Individual adapters can exchange signals with the processing unit on the star lines. The processing unit and the adapters receive pulses from a common clock; therefore, a connection between the processing unit and an adapter can be established by simple synchronization pulses and does not require a handshaking procedure. Apart from the ring buses and star lines, three additional lines provide these synchronization pulses.

One central dispatching mechanism distributes bus time among the processor and the adapters. Bus capabilities and the dispatching algorithm must be matched to the expected load and the realtime response requirements. At first glance, it might seem economical to adjust bus capability according to average load for good utilization. Unfortunately, however, service requests occur at random; therefore, bus waiting time appears as soon as requests arise faster than they can be serviced. When higher utilization leads to a higher probability of waiting for the bus, response deteriorates and buffers are required for those mechanical I/O devices whose service requests cannot be postponed. Furthermore, the IC bus must service varied requests. Adapters require transfer of variable quantities of data to or from main storage at variable rates. The processor, however, requires single-byte transfers for its status monitoring and control operations. Although buffers could be used in adapters to overcome bus waiting time restrictions, high bus utilization would require large buffers, and an efficient bus transfer mechanism would retain an established connection until the buffer had been emptied of data. This approach makes the bus unsuitable for single-byte sense and control operations in response to asynchronous events that demand fast processor response.

A consequence of poor bus service, data overrun would occur if the bus system failed to accept or deliver data within the time period prescribed by an I/O device. Program overrun would occur if the processing unit failed to meet the realtime requirements of a device when accepting status information or supplying a command. Overrun situations can be corrected on different

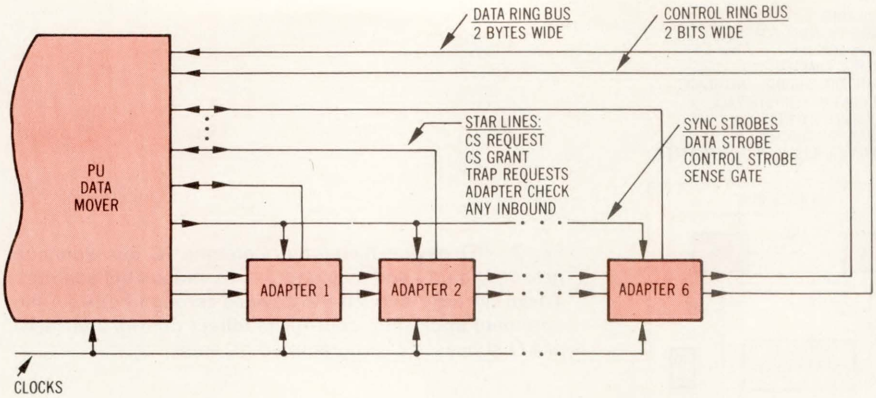

Fig 4 IC bus layout. Two ring buses carry data and control information during data transfer. Star lines allow direct device selection and checking. Common synchronization lines eliminate any need for handshaking protocol

levels, at varying expense, by the microprogram, the operating system, or the operator. Of course, system performance depends on the choice of recovery method.

Combining fast realtime response with an effective data transfer mechanism, the chosen dispatching algorithm provides a good compromise between efficiency and responsiveness. Data transfer granularity achieves fast response without introducing idle hardware by performing data transfers in small slices and implementing a priority scheme that gives preference to those requests needing fastest response. In contrast to first in, first out servicing, the dispatching algorithm gives the processor priority over adapters, and it services requests from adapters according to their data rates and buffer sizes. Priority decisions overlap the previous data transfer cycle, permitting back to back transfers on the bus and avoiding loss of speed. A compact physical interface between the processor, main storage, and adapters compensates for the extra hardware devoted to bus control.

Data Transfer

Microprogram preparation for data transfer between an adapter and main storage initializes command, flag, address, and count information in the processor and in the adapter. A data transfer cycle is requested by an adapter as soon as data or space for data becomes available. Then, an 800-ns time slot allows four bytes to be exchanged. If the adapter keeps its transfer request active, another time slot will be allotted, provided that no higher priority request is pending.

The adapter asserts a cycle steal request (CS REQUEST in Fig 4) to initiate a transfer operation, and the processing unit services the request by using CS GRANT to select the adapter and DATA STROBE to synchronize the transfer cycle. Because the bus is two bytes wide, two consecutive 400-ns cycles complete the transfer. The processing unit tests ADAPTER CHECK and ANY INBOUND lines during every cycle. ADAPTER CHECK signals data errors, such as parity checks, and selection errors, such as double select or unrequested select. ANY INBOUND signals the transfer direction, chosen by the adapter, which the processing unit compares against the expected value. Ring lines are used to signal the end of a transfer: the CCW count exhausted or an error, if transferring out to the adapter; a device termination, with up to four bytes of valid data transferred, if transferring in to the processing unit.

Sense and Control

Processing unit microinstructions request a control or sense operation directly via the IC bus. Using one data bus byte to address both the adapter and a register in the adapter while the other byte carries control or sense data, these operations need only one bus cycle. A CONTROL STROBE signal triggers control and sense operations, and the SENSE GATE level determines the transfer direction. Although sense and control operations can establish communication between the processing unit and an I/O adapter, the large amount of processing time required to poll adapters for asynchronous requests is a serious disadvantage. Therefore, a trap mechanism allows adapters to interrupt the processing unit on the microprogram level.

Seven trap levels are available. One or two TRAP REQUEST lines per adapter connect to the trap control according to their priority. Vector traps, produced by the trap mechanism, force unique addresses, which point to the first microinstruction of the trap routine, into the control storage address register (CSAR). A current trap indication, set when a trap request is accepted, determines whether a subsequent trap request will take priority over the current trap. During a trap, the microprogram saves the next microinstruction address and processing unit status of the interrupted program. The first microinstruction of every trap routine is a branch and link (BAL) that saves return information in a local storage register. After servicing the adapter, which drops its trap request during service routine execution, a LEAVE microinstruction resumes the interrupted program by means of saved link information and resets the current trap indication. Thus, the trap mechanism allows fast response and high flexibility when servicing requests of different priorities without devoting hardware to extra save registers.

Use of Local Storage

Data processing systems usually require simultaneous operation of several I/O devices that a single processor machine must handle in sequence. One shared microprogram can be used reentrantly for this service if the operands it requires are identically formatted and indirectly addressed. Then, I/O device service can be interrupted at any point in the program, the same program can service a different I/O device, and the interrupted service operation can be resumed without loss of control. Identically formatted operands are guaranteed for all I/O devices attached to identical adapters that have similar control blocks in the processing unit. These control blocks, called unit control words (UCWs), hold information about the channel control program (ie, the chain of CCWs) and the device (eg, status). UCWs reside in the data local storage (DLS) assigned to the I/O device (Fig 5).

A UCW provides space for eight words, and the DLS has space reserved for 32 UCWs. The processing unit allows indirect addressing of DLS operands; however, existing addressing modes and local store address registers (LSARs) do not fit the UCW format. Therefore, indirect addressing of UCWs in the DLS requires a special addressing mode and a dedicated I/O address register (IOAR). When a microinstruction operand requires the special indirect addressing mode, five bits of the IOAR select a UCW, and three bits of the operand field select a word in the UCW. In addition, three IOAR bits select an I/O adapter in the case of BUS SENSE and BUS CONTROL microinstructions that communicate with adapters.

A BAL microinstruction automatically saves the IOAR, and a LEAVE microinstruction restores it. Thus, setting the IOAR at the beginning of an I/O trap routine associates a UCW and a particular adapter with the common microcode routine. For a byte multiplexer channel, UCW selection depends on the device address. Then, because the number of UCWs is smaller than that of possible device addresses, a folding technique achieves UCW selection. Hardware supports a mapping algorithm that associates several device addresses with the same UCW, and a special CONTROL microinstruction sets the UCW pointer in the IOAR from the device address.

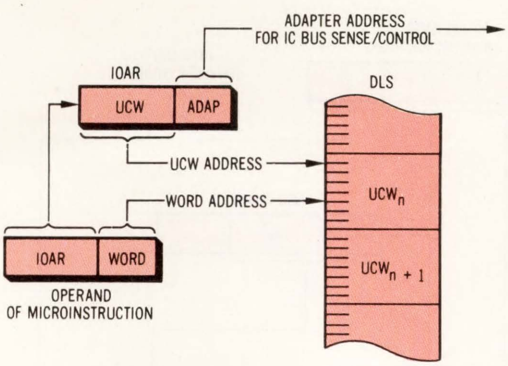

Fig 5 Access to local data storage. Special indirect addressing mode allows reentrant microprogram to service several devices concurrently. When accessing UCW in DLS, operand supplies 3-bit word offset, which is concatenated with five bits of IOAR pointing to UCW. Three IOAR bits may select adapter

Address Translation

CCW addresses provided by the CAW and TIC commands, (ie, transfer in channel, channel program jump), as well as data addresses contained in the CCWs and indirect data address lists (IDALs), are virtual addresses that must be translated into physical addresses using the main storage directory (MSD). Translation is time consuming because the MSD is too large to be held in the hardware for fast access. The IPU can minimize address translation overhead by using a directory lookahead table (DLAT), implemented in hardware, that contains up to 32 translated addresses. The localized behavior of program and data fields guarantees a high probability that the next address requiring translation will be one of the 32 different addresses most recently translated and saved in the DLAT. Failing this, an incidental miss requires address translation from the MSD but has little impact on average performance.

The channel program requires a different address handling mechanism for two reasons. Many new addresses require explicit translation during command chaining, at precisely the time fast response is required. Also, several channel programs with independent storage address ranges might be multiplexed, causing common DLAT usage to disturb the localized address behavior and produce many DLAT misses during channel service. A special microinstruction meets this need for fast MSD translation. Accepting a virtual address as its operand, the TRANSLATE microinstruction builds the MSD entry address, fetches the real page frame address, and concatenates it with the low order bits of the virtual address to form the true address (Fig 6). In addition, TRANSLATE may update the virtual address to the beginning of the next page to prepare for the next translation.

True addresses are stored in the UCWs rather than in a special channel DLAT. Each UCW supplies space for two such translated data addresses; one can be prepared by the microprogram while the other is being used for data transfer, a mechanism that provides continuous data transfer over several page frames.

Data Mover

Controlling the flow of data between the I/O adapters and main storage, the data mover has three basic parts.

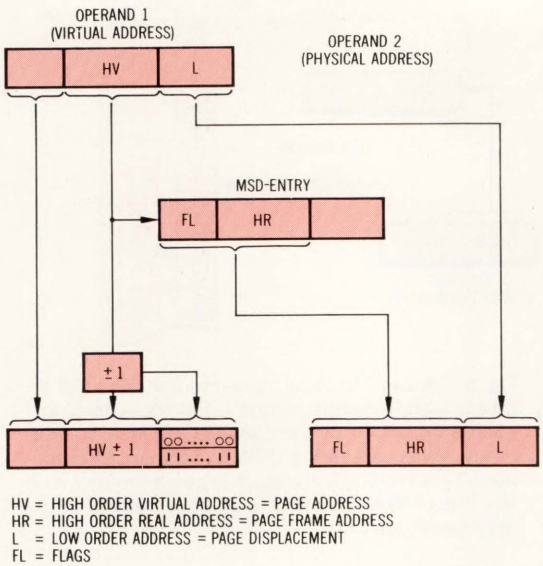

Fig 6 Channel program address translation. Special microinstruction reduces virtual address translation overhead during command chaining when speed is critical. Accepting virtual address, it builds MSD entry address, fetches real page frame address, and thus forms true address

The transfer control picks up adapter requests for data transfer and, supported by the processing unit, handles control blocks stored in the DLS. It also triggers IC bus and main storage operations. The IC bus control provides for transfer of information between adapters and the processing unit via the IC bus. The main storage control supervises transfers between the processing unit and main storage. Fig 7 shows these units together with part of the data flow involved in data transfer operations.

Cycle Stealing

Any data transfer is triggered by an I/O adapter raising CS REQUEST. Requiring processing unit support, the cycle steal request suspends execution of the microinstruction stream and forces a special operation code in the processing unit. During execution of the pseudo-operation code, two UCW words are read from DLS, updated, and returned. The processing unit also handles data addresses and byte counts in its arithmetic and logic unit, while the transfer control inspects and updates two control bytes containing additional, detailed information about the operation to be performed. A pointer establishes connection to the proper UCW. Because adapter service is multiplexed and all adapters could be set up for transfer simultaneously, transfer control hardware stores a different pointer for each adapter.

During UCW handling, the transfer control has all information necessary to trigger the bus control and the main storage control in the correct sequence according to the direction of transfer. Serving as intermediate data storage, a register on the IC bus and main storage interface decouples the two transfer sections and allows IC bus operation to overlap main storage operation. The use of processing unit data flow mechanisms during the data transfer operation eliminates considerable hardware that would be required for working storage and for an arithmetic unit. It degrades processing unit performance by an average of less than two percent.

Pipelining

Three parts of the system are involved in transferring data between main storage and an I/O adapter: the processing unit that reads control information out of DLS, updates it, and restores it; the main storage and its controller that fetch or store data according to the command and the address; and the IC bus that receives and sends data from and to the specified I/O adapter. These

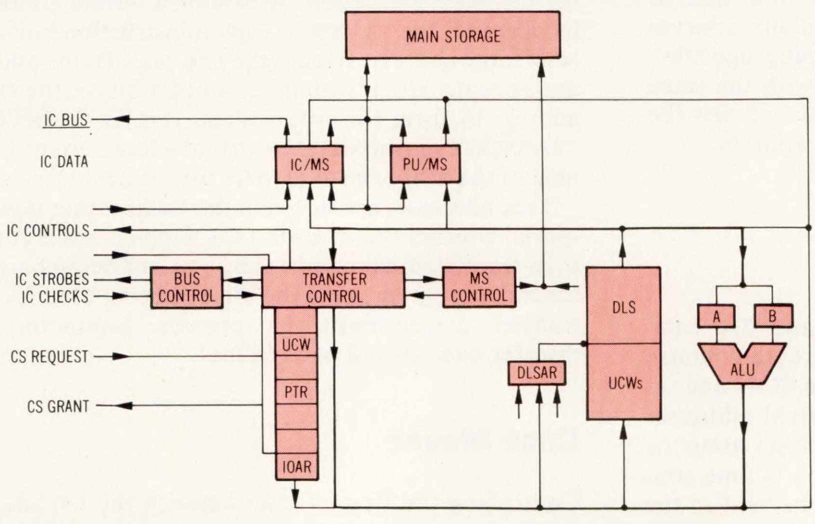

Fig 7 Data mover block diagram. Using address pointer from transfer control, processing unit delivers parts of UCW from its DLS for transfer control inspection and update. UCW address and count fields are updated in processor's arithmetic and logic unit. IC bus control logic handles data transfer between processor and adapter. Main storage control handles flow between processing unit and storage

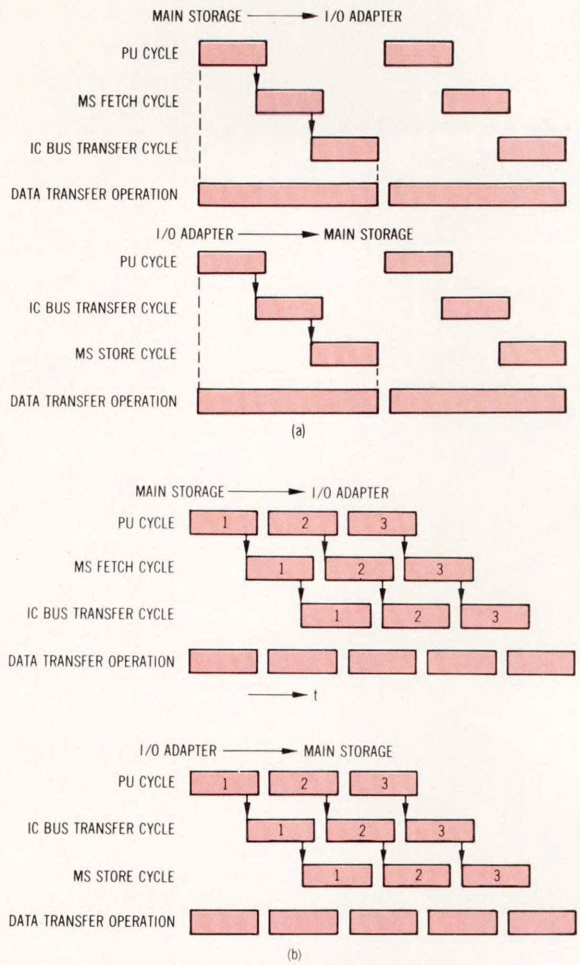

Fig 8 Enhancement through pipelining. Without overlap, in (a), duration of transfer operation is sum of processing unit cycle, main storage cycle, and IC bus cycle. In (b), pipelining independent operations by staggering processing unit, main storage, and IC bus cycles gives threefold improvement in throughput

three parts are not used at the same time, however. The processor service cycle starts the transfer operation and analyzes the transfer direction. If data are to be transferred from the main storage to an adapter, it triggers a main storage fetch cycle that makes data available to the IC bus in the interface register. Then, an IC bus cycle transfers the data to the adapter. When transferring from an adapter to main storage, the IC bus cycle and the main storage cycle are reversed in sequence. Fig 8(a) shows these data transfer timing characteristics and indicates where the processing unit must wait for operations to complete before beginning a new operation.

To reduce processing unit idle time, the IC bus and the main storage control work independently of each other and of the processing unit. Each controller receives a request and a command code from, and provides status information to, its partners. Each can execute an operation with independent timing, when all necessary resources are available, so that the processing unit can resume its instruction stream while the IC bus and main storage execute requests initiated earlier. Thus, up to three operations can be overlapped [Fig 8(b)]. Because the processing unit, main storage, and IC bus are each busy for about the same amount of time, pipelining decreases the impact of data transfers on the processing unit and also improves the data rate by a factor of three.

Summary

In contrast to certain microprocessors, which address I/O device registers as memory locations, general purpose computers use separate address spaces for main storage and I/O devices. Thus, during execution, the processing unit must exchange data with only one physical interface connected to a fast, random access device—the main storage. I/O instructions that transfer data between main storage and other physical devices are effectively decoupled from the instruction stream, and the tasks performed by an instruction processor become very different from I/O subsystem tasks.

Instruction processor design can be optimized for high average performance; however, the diverse physical characteristics of I/O devices that may exist in a multitude of configurations, along with the need for fast realtime response, challenge designers to implement efficient I/O handling without introducing I/O subsystem hardware that will remain idle most of the time. Although large systems can afford special purpose processors that are dedicated to I/O tasks, a more economical alternative addresses performance tradeoffs in a single-processor system. By modifying the instruction processor, the design retains well-balanced computational ability and adds I/O power with the flexibility to service a wide range of system configurations.

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About the Author:

Paul Hain, an advisory design engineer at IBM, is working on I/O subsystems, channels, and I/O attachments and subsystems for small general purpose processors. Before joining IBM, he was involved in the design of electronically controlled exchanges. He received his Dipl-Ing from the Aachen Technical University.

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REDUCING ROUNDOFF ERRORS IN MICROPROCESSOR BASED CALCULATIONS

Analysis technique identifies sequence of operations that produces least error during expression evaluation, reducing the need for extended precision arithmetic

Henry A. Davis

American Microsystems, Incorporated
3800 Homestead Rd, Santa Clara, CA 95051

Errors are inevitable when dealing with a finite representation of a real number, such as the binary representation used in computers. These errors can never be eliminated, but they can be controlled and their effects estimated. As microprocessors are applied to more mathematical and scientific problems, quantizing and roundoff errors become serious obstacles to successful implementations because the obvious remedy of multiple-precision arithmetic imposes too large a penalty in terms of program size, data storage requirements, and execution time. In many cases, analysis based on a simple model of error propagation directs systematic reordering of the sequence of operations during expression evaluation to ensure sufficient accuracy without the need for multiple-precision arithmetic.

Pure integer mathematics is exact for addition, multiplication, and subtraction; however, its accuracy for division is limited by the remainder. This limitation, coupled with the lack of dynamic range inherent in fixed bit length integers, leads to the use of various types of floating point number representations. Problems in scientific programming generally require the benefits of floating point arithmetic. Examples of such applications are signal processing, least-mean-square algorithms, and iterative programming techniques used in linear programming applications.

Theory

Floating point formats typically represent real numbers by supplying a 1-bit sign, an n-bit exponent, and a t-bit mantissa. The mantissa is said to be normalized if its high order bit is a 1; otherwise it is unnormalized. It represents a number between 0 and 1, usually expressed as its integer cell number on a uniform graduation of this interval into 2^{t-1} equal cells. The exponent represents the signed integer power (usually of base 2) to which the mantissa must be raised to yield the real value. Thus, normalization is performed by shifting the mantissa left and decrementing the exponent once for each shift until a 1 appears in the mantissa high order bit.

Denormalization, the reverse process, is performed on one of two operands to give both operands the same exponent. Once this is achieved, addition and subtraction may be performed by adding or subtracting the mantissas, carrying forward the common exponent, and normalizing the result. Multiplication and division, which do not require denormalization, are performed by forming the product or quotient of mantissas, adding or subtracting the exponents, and again normalizing the result. Addition and subtraction introduce error when bits are shifted right off the low order end of one operand mantissa during denormalization.

Multiplication and division introduce error when the 2t-bit product of mantissas is normalized to produce a t-bit result mantissa. Both error sources reflect overflow of the integer mantissa.

Thus, because the floating point mantissa is represented by a binary integer, the same errors encountered during integer arithmetic also appear in floating point arithmetic. In general, three sources of error can be identified: initial, roundoff, and truncation. Initial error is caused by input sensor inaccuracy and sometimes can be the major system error, but this type of error cannot be corrected because it is not systematic. That is, in general, random error cannot be removed without significant signal processing. Initial error is most often reduced by using better sensors.

Roundoff error results from using a finite set of binary integers to represent an infinitely fine graduation over a range of real numbers. If the floating point representation is normalized, roundoff error cannot exceed half the magnitude of the least significant bit value. Usually, this error appears in every number stored in a computer. Since two consecutive mantissa values span an infinity of real numbers, only the largest and smallest of which are represented precisely, roundoff error can be assumed in the floating point representations of all numbers.

Truncation error occurs when an infinite series is computed by evaluating a finite or truncated series. For example, the sine function is almost always represented by some portion of the Taylor series in a computer. If the Taylor series expansion stops after the first seven terms, eight significant decimal digits result. In this instance, the sum of all subsequent Taylor series terms reflects the truncation error. Since the series converges, the absolute error cannot exceed the magnitude of the eighth term.

Quantization errors due to word size limitations result from the inexact binary representation for most numbers. For example, consider a real number X; then, the absolute error introduced by using this value is $X - \overline{X}$, where $\overline{X}$ is the normalized value of X with associated quantization error. For convenience, the error term in X is shown as $e_X = X - \overline{X}$. An addition operation involving X gives

$$\begin{aligned} X + Y &= (\overline{X} + e_X) + (\overline{Y} + e_Y) \\ &= (\overline{X} + \overline{Y}) + (e_X + e_Y) \end{aligned} \tag{1}$$

Similarly, subtraction yields

$$\begin{aligned} X - Y &= (\overline{X} + e_X) - (\overline{Y} + e_Y) \\ &= (\overline{X} - \overline{Y}) + (e_X - e_Y) \end{aligned} \tag{2}$$

Subtraction brings to light an interesting problem. When two numbers of nearly identical magnitude are subtracted, the magnitude of the error term may approach and even exceed the magnitude of the difference. This phenomenon, known as cancellation, can cause erroneous results that differ from the correct result by orders of magnitude.

Multiplication is slightly more complicated, with an error term involving sums of cross products

$$\begin{aligned} XY &= (\overline{X} + e_X)(\overline{Y} + e_Y) \\ &= \overline{X}\,\overline{Y} + \overline{X}e_Y + \overline{Y}e_X + e_Xe_Y \end{aligned}$$

Because the product of errors, e_Xe_Y, is extremely small in relation to the other terms, drop that insignificant term to obtain

$$XY \cong (\overline{X}\,\overline{Y}) + (\overline{X}e_Y + \overline{Y}e_X) \tag{3}$$

Division is represented by

$$\begin{aligned} \frac{X}{Y} &= \frac{\overline{X} + e_X}{\overline{Y} + e_Y} \\ &= \frac{\frac{1}{\overline{Y}}(\overline{X} + e_X)}{1 + \frac{e_Y}{\overline{Y}}} \\ &= \left(\frac{\overline{X}}{\overline{Y}} + \frac{e_X}{\overline{Y}}\right)\left(\frac{1}{1 + \frac{e_Y}{\overline{Y}}}\right)\left(\frac{1 - \frac{e_Y}{\overline{Y}}}{1 - \frac{e_Y}{\overline{Y}}}\right) \\ &= \left(\frac{\overline{X}}{\overline{Y}} + \frac{e_X}{\overline{Y}}\right)\left(\frac{1 - \frac{e_Y}{\overline{Y}}}{1 - \left(\frac{e_Y}{\overline{Y}}\right)^2}\right) \end{aligned}$$

Because e_Y is very small in relation to $\overline{Y}$, consider the number resulting from the division of e_Y by $\overline{Y}$ to be nearly zero, and disregard the square of this quotient to obtain

$$\begin{aligned} \frac{X}{Y} &\cong \left(\frac{\overline{X}}{\overline{Y}} + \frac{e_X}{\overline{Y}}\right)\left(1 - \frac{e_Y}{\overline{Y}}\right) \\ &\cong \frac{\overline{X}}{\overline{Y}} + \frac{e_X}{\overline{Y}} - \frac{\overline{X}e_Y}{\overline{Y}^2} - \frac{e_Xe_Y}{\overline{Y}^2} \end{aligned}$$

The final term in this equation may be dropped for the same reason to give

$$\frac{X}{Y} \cong \left(\frac{\overline{X}}{\overline{Y}}\right) + \left(\frac{e_X}{\overline{Y}} - \frac{\overline{X}e_Y}{\overline{Y}^2}\right) \tag{4}$$

Since division is similar to subtraction in many theoretical senses, particular attention should be paid to possible problems. Examination of Eq (4) shows that the error may be very large when the denominator of this equation, which depends only on the divisor, is small in relation to the numerator of the equation, which depends only on the dividend. This type of error sensitivity results from ill-conditioned operand terms under division and has important ramifications because, no matter how well roundoff and truncation are controlled, initial error sensitivity in the ill-conditioned dividend and divisor may render the final quotient useless.

Absolute error expressions are not really appropriate for roundoff error analysis; instead, it is the relative error propagation that matters. The relative error carried through a computation by any term, X, is

$$\frac{X - \bar{X}}{\bar{X}} = \frac{e_X}{\bar{X}}$$

Absolute error expressions derived earlier can be rewritten as relative error expressions to give

$$\frac{e_X + e_Y}{\bar{X} + \bar{Y}} = \left(\frac{\bar{X}}{\bar{X} + \bar{Y}}\right)\left(\frac{e_X}{\bar{X}}\right) + \left(\frac{\bar{Y}}{\bar{X} + \bar{Y}}\right)\left(\frac{e_Y}{\bar{Y}}\right) \tag{5}$$

$$\frac{e_X - e_Y}{\bar{X} - \bar{Y}} = \left(\frac{\bar{X}}{\bar{X} - \bar{Y}}\right)\left(\frac{e_X}{\bar{X}}\right) - \left(\frac{\bar{Y}}{\bar{X} - \bar{Y}}\right)\left(\frac{e_Y}{\bar{Y}}\right) \tag{6}$$

$$\frac{\bar{X}e_Y + \bar{Y}e_X}{\bar{X}\bar{Y}} = \frac{e_X}{\bar{X}} + \frac{e_Y}{\bar{Y}} \tag{7}$$

$$\frac{\left(\frac{e_X}{\bar{Y}} - \frac{\bar{X}e_Y}{\bar{Y}^2}\right)}{\frac{\bar{X}}{\bar{Y}}} = \frac{e_X}{\bar{X}} - \frac{e_Y}{\bar{Y}} \tag{8}$$

Application

These equations can be used to reduce computational error by considering a tree representation of binary operations (Fig 1) derived directly from Eqs (5), (6), (7), and (8). The amount of relative error added at each node is the sum of the relative error of each branch in the tree. Branch error, in turn, is the product of the branch coefficient (relative roundoff error) and the error of the previous node (relative quantization error). Basic tree structures corresponding to the four arithmetic operations are combined to build a tree representation for any arithmetic expression. The tree representation expresses the total error propagated by expression evaluation. For example, the typical computation Y = A + B + C + D shows how the sequence in which operations are performed can affect error propagation (Fig 2). The total error at node 1 is

$$\left(\frac{\bar{A}}{\bar{A} + \bar{B}}\right)\left(\frac{e_A}{\bar{A}}\right) + \left(\frac{\bar{B}}{\bar{A} + \bar{B}}\right)\left(\frac{e_B}{\bar{B}}\right) + r_1 = \frac{e_A + e_B}{\bar{A} + \bar{B}} + r_1$$

where r_1 is the roundoff error. Node 2 has a total error of

$$\left(\frac{\bar{A} + \bar{B}}{\bar{A} + \bar{B} + \bar{C}}\right)\left(\frac{e_A + e_B}{\bar{A} + \bar{B}} + r_1\right) + \left(\frac{\bar{C}}{\bar{A} + \bar{B} + \bar{C}}\right)\left(\frac{e_C}{\bar{C}}\right) + r_2$$

and the total evaluation error at node 3 is

$$\frac{\bar{A} + \bar{B} + \bar{C}}{\bar{A} + \bar{B} + \bar{C} + \bar{D}}\left[\frac{e_A + e_B + e_C + (\bar{A} + \bar{B})r_1 + (\bar{A} + \bar{B} + \bar{C})r_2}{\bar{A} + \bar{B} + \bar{C}}\right] + \left(\frac{\bar{D}}{\bar{A} + \bar{B} + \bar{C} + \bar{D}}\right)\left(\frac{e_D}{\bar{D}}\right) + r_3$$

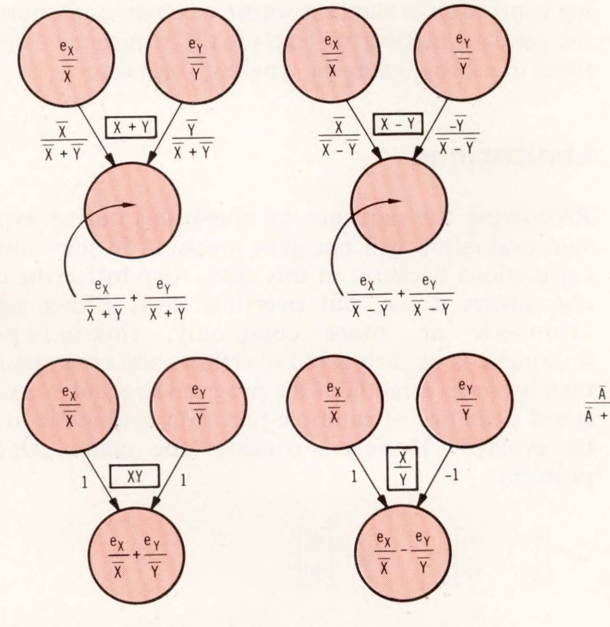

Fig 1 Tree structured model of binary operations. Branch error is product of node error and branch coefficient. Sum of branch errors is total error propagated through each basic operation. Tree structures—derived from Eqs (5), (6), (7), and (8)—combine to reflect sequence of operations during expression evaluation

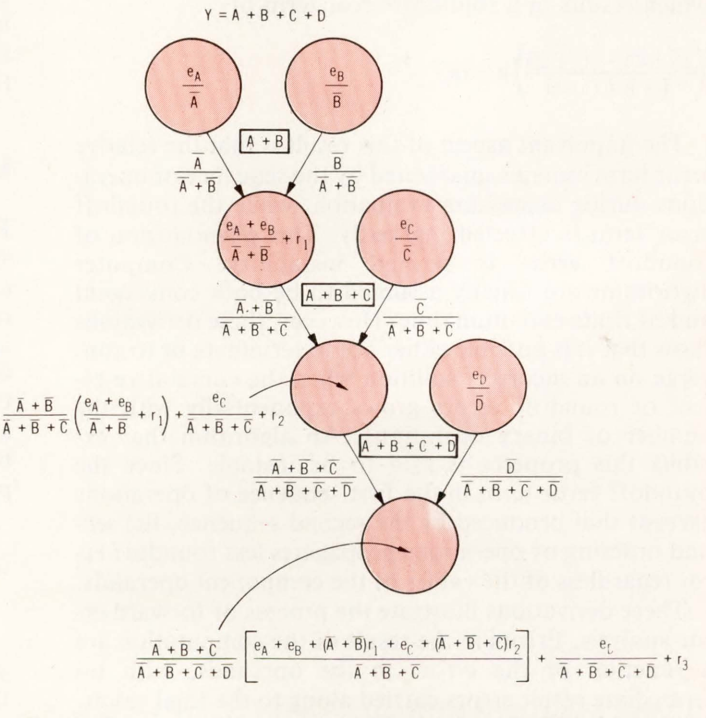

Fig 2 Conventional sequence of operations. Unbalanced tree represents strict left-to-right evaluation of Y = A + B + C + D. Propagated error, evaluated at each node, leads to overall error term at final node

If we denote by R the maximum of r_1, r_2, and r_3, then

$$\frac{e_Y}{\bar{Y}} \le \frac{e_A + e_B + e_C + e_D}{\bar{A} + \bar{B} + \bar{C} + \bar{D}} + \frac{(\bar{A} + \bar{B})R + (\bar{A} + \bar{B} + \bar{C})R + (\bar{A} + \bar{B} + \bar{C} + \bar{D})R}{\bar{A} + \bar{B} + \bar{C} + \bar{D}}$$

Finally, the roundoff error term is

$$\left(\frac{3\bar{A} + 3\bar{B} + 2\bar{C} + \bar{D}}{\bar{A} + \bar{B} + \bar{C} + \bar{D}}\right)R$$

Adding explicit parentheses alters the order of expression evaluation and produces the branch coefficients shown in Fig 3. Here, the error at node 1 is

$$\frac{e_A + e_B}{\bar{A} + \bar{B}} + r_1$$

as when the expression was evaluated previously. However, using this new sequence of operations, the error at node 2 is now

$$\frac{e_C + e_D}{\bar{C} + \bar{D}} + r_2$$

The total error at node 3 becomes

$$\frac{\bar{A} + \bar{B}}{\bar{A} + \bar{B} + \bar{C} + \bar{D}}\left(\frac{e_A + e_B}{\bar{A} + \bar{B}} + r_1\right) + \frac{\bar{C} + \bar{D}}{\bar{A} + \bar{B} + \bar{C} + \bar{D}}\left(\frac{e_C + e_D}{\bar{C} + \bar{D}} + r_2\right) + r_3$$

Again, replacing each of r_1, r_2, and r_3 by their maximum, R, yields

$$\frac{e_Y}{\bar{Y}} \le \frac{e_A + e_B + e_C + e_D}{\bar{A} + \bar{B} + \bar{C} + \bar{D}} + \frac{(\bar{A} + \bar{B})R + (\bar{C} + \bar{D})R + (\bar{A} + \bar{B} + \bar{C} + \bar{D})R}{\bar{A} + \bar{B} + \bar{C} + \bar{D}}$$

which results in a roundoff error term of

$$\left(\frac{2\bar{A} + 2\bar{B} + 2\bar{C} + 2\bar{D}}{\bar{A} + \bar{B} + \bar{C} + \bar{D}}\right)R = 2R$$

The important aspect of this result is that the relative error term remains unaffected by the sequence of operations during expression evaluation, while the roundoff error term is affected markedly. This phenomenon of roundoff error is termed instability. Computer algorithms are usually assumed to be both convergent and of finite execution time. However, these derivations show that it is possible either not to terminate or to converge on an incorrect solution when the cumulative effect of roundoff errors grows exponentially with the number of binary operations. An algorithm that exhibits this property is said to be instable. Since the roundoff error term in the first sequence of operations exceeds that produced by the second sequence, the second ordering of operations propagates less roundoff error regardless of the values of the component operands.

These derivations illustrate the process of forward error analysis. Errors in the result of the computation are a function of the errors in the operands, with intermediate result errors carried along to the final result. By means of this analysis technique, conservative bounds on the magnitude of error can be computed from the absolute values of each term in Eqs (5), (6), (7), and (8).

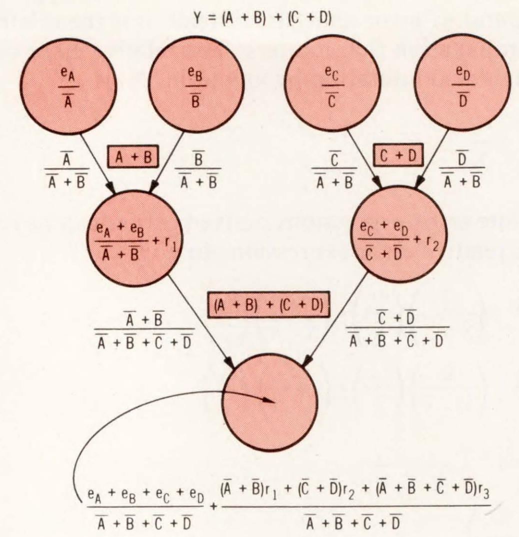

Fig 3 Altered sequence of operations. Balanced tree with fewer levels represents evaluation of Y = (A + B) + (C + D). Sequence of operations propagates less error than strict left-to-right evaluation

The total error propagated through a tree is much easier to determine than Figs 2 and 3 might indicate because, in practice, actual numeric values can be assigned to the subscripted error terms (based on the implementation system mantissa size) and the uppercase operand terms (based on maximum and minimum expected values). Further, this example illustrates an important general result: the sequence of operations during expression evaluation whose tree representation has the smallest number of levels is the sequence of operations that propagates the smallest total error.

Limitations

Reordering the sequence of operations during expression evaluation will not gain precision in pure integer calculations because, in this case, roundoff error does not always occur, but overflow may. Either scaled arithmetic or, more commonly, floating point arithmetic is used to avoid overflow, and error analysis then becomes essential if the program size and execution speed penalties of multiple-precision arithmetic are to be avoided. However, consider the matrix algebra problem

$$A = \begin{bmatrix} 41 & 40 \\ 40 & 39 \end{bmatrix} \qquad b = \begin{bmatrix} 81 \\ 79 \end{bmatrix}$$

whose exact solution is $X_1 = X_2 = 1$. Now, assume that there was some small error in b so that the real b is

$$b = \begin{bmatrix} 80.99 \\ 79.01 \end{bmatrix}$$

$$X'_1 = 1.79, \quad X'_2 = 0.19$$

Thus, relative errors of about 1.25×10^{-4} in the right-hand side of the equation resulted in relative errors of about 4.3 in X_1 and X_2. Such systems are said to be ill-conditioned. For the most part, ordinary matrices do not behave in this way. Unfortunately, least-squares problems that occur in electrical engineering, and particularly in signal processing, are typically ill-conditioned. Rewriting the previous example in general form gives

$$A = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \quad b = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} \quad X = \begin{bmatrix} X_1 \\ X_2 \end{bmatrix}$$

$$b_1 = b + e \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} + \begin{bmatrix} e_1 \\ e_2 \end{bmatrix}$$

$$AX = b \qquad AX' = b'$$

Therefore,

$$A^{-1} = \frac{1}{\det(A)} \begin{bmatrix} a_{22} & -a_{12} \\ -a_{21} & a_{11} \end{bmatrix}$$

Rewriting this to account for errors in X and b gives

$$X' = A^{-1} b'$$

or, using e as the error matrix associated with $b' = b + e$,

$$= A^{-1}(b + e)$$

Distributing A^{-1} over b + e yields

$$= A^{-1} b + A^{-1} e$$

Then, since $X = A^{-1}b$, substitution gives

$$= X + A^{-1} e$$

Subtracting the ideal representation of X from both sides permits expressing the right-hand side in determinant form.

This last equation shows that small changes in E_1 and E_2 can result in large errors if any of the factors $A_{ij}/\det(A)$

$$X' - X = A^{-1} e$$

$$= \frac{1}{\det(A)} \begin{bmatrix} a_{22} & a_{12} \\ -a_{21} & a_{11} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \end{bmatrix}$$

$$= \begin{bmatrix} \frac{a_{22}}{\det(A)} E_1 & -\frac{a_{12}}{\det(A)} E_2 \\ -\frac{a_{21}}{\det(A)} E_1 & \frac{a_{11}}{\det(A)} E_2 \end{bmatrix}$$

is very large. The clincher in this analysis is that these factors are precisely the elements of A^{-1} that scaling will not help.

Summary

Errors cannot be avoided when computations are performed using floating point arithmetic. Extended or multiple-precision computations reduce arithmetic error but incur a large penalty in terms of program size, data storage requirements, and execution speed. By paying careful attention to the order in which an expression is evaluated, it is sometimes possible to gain adequate precision to forestall the use of multiple-precision arithmetic.

A tree structured model of arithmetic expression evaluation represents the relationships that were derived for error propagation. Using this model to perform a boundary analysis identifies the sequence of operations that propagates the least error. It also gives confidence in the correctness of results under various conditions. Roundoff instability, cancellation, and algorithm instability are key factors in final error magnitude, all of which can be controlled under certain conditions.

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About the Author:

Henry A. Davis is manager of systems engineering at American Microsystems, Inc. He has worked on development systems, logic boards, digital signal processing with microprocessors, artificial intelligence, pattern recognition, and high level languages for microprocessors. His education includes undergraduate work at Furnam University and graduate work in computer science at New Mexico Institute of Mining and Technology.

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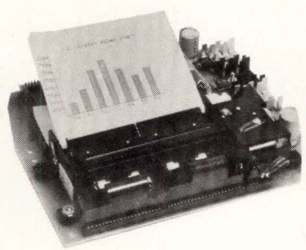

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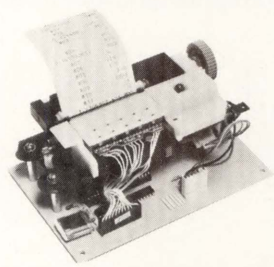

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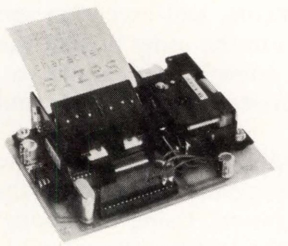

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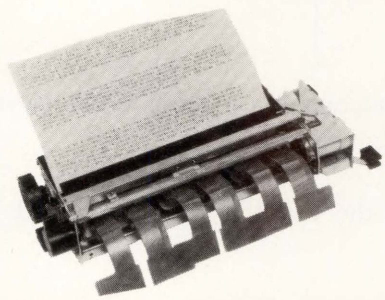

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DISTRIBUTED COMMUNICATION ARCHITECTURE FORMS FRAMEWORK FOR NETWORK DESIGN

Dissimilar computer systems interact freely by using a data communication architecture that defines basic concepts and capabilities to build a highly structured framework for network planning and design

Michael L. Timmons
Sperry Univac
17900 Von Karman Ave, Irvine, CA 92714

In order to understand modern distributed data processing, it is necessary to briefly review the advent of this phenomenon. Distributed data processing arrived upon the user scene, not because of spontaneous generation of a certain kind of processing capability, but rather as a series of logically discrete organizational development processes phased in over a period of time. The advent of the true minicomputer in the mid-1960s created opportunities for economical placement of computers into locations and application environments never before thought possible. Users could implement various kinds of functionality at low cost wherever appropriate within an organization. As a result of the capability to locate computers near their users, a period of decentralization rapidly followed. This decentralization often left organizations with various kinds of systems from several different vendors dispersed among many sites.

Management demand for centralized control and, to a lesser extent, the need for minicomputer access to the centralized corporate data base exerted pressure to connect the various minicomputer systems to the corporate central computer. Networks that resulted from this recentralization pressure were the first distributed data processing systems. When successful, recentralization was a long, difficult, and often expensive process whereby minicomputer systems were connected to the central systems using whatever data communication protocols were available. In many cases, adequate protocols were not available and had to be provided by special development efforts, often without benefit of communication access methods. Application programs in the resulting networks were often heavily embedded with data management and control information required by the specific protocols. Any change in the basic configuration of these user networks generally required program changes at many levels.

Organizations using minicomputer distributed data processing in this period experienced mixed results from their networks, which offered little in the way of configuration flexibility, management convenience, or ease of use. However, the networks did provide the key to better performance of operations necessary to support the organization. Specifically, it was the structuring of distributed data processing systems in a way natural to the needs of organizations that improved performance, reduced costs, and increased reliability.

Problems that grew out of the early distributed data processing experience did not involve proving the concept, which had succeeded in demonstrating ways of freeing users for the most part from the rigid demands of batch oriented processing in a structured system. Rather, the concerns dealt with means for developing new generations of distributed data processing systems that could exploit and expand upon the benefits that accrued from the first age of minicomputer distributed data processing while avoiding the trauma associated with its implementation.

Distributed Communication Architecture

Specifically designed to provide a systematic means of implementing data communication systems and distributed data processing systems, distributed communication architecture (DCA) is not a product, but is instead a highly structured framework for network design and planning. It defines the concepts, logical structures, and functional capabilities of all components that make up a communication network. DCA establishes a set of rules and guidelines that specify how logical structures are mapped to host processors, network processors, cluster controllers, and terminals.

The primary objective of DCA is to define a structure within which any given set of computing systems, whether homogenous or not, can be interconnected to form a harmonious and freely interacting processing environment. In defining such a processing environment, it is necessary to identify a part of each computing system as belonging to a single logical entity that has complete responsibility for handling all interaction among the computing systems. The first of the major DCA structural components, this logical entity is termed the communication system (Fig 1). The remainder of the environment within each computing system is concerned with processing data for various applications on behalf of users. It is termed the application system environment and is the second major DCA component.

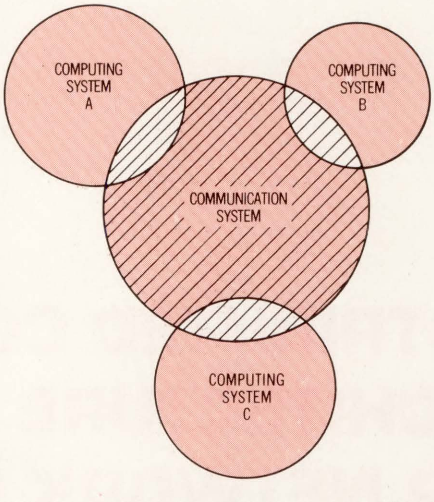

Fig 1 DCA environment. Comprising that portion of each computer system devoted to network interaction, communication system is logical entity with complete responsibility for flow of data among computer systems. Remainder of each computer system is called its application system environment

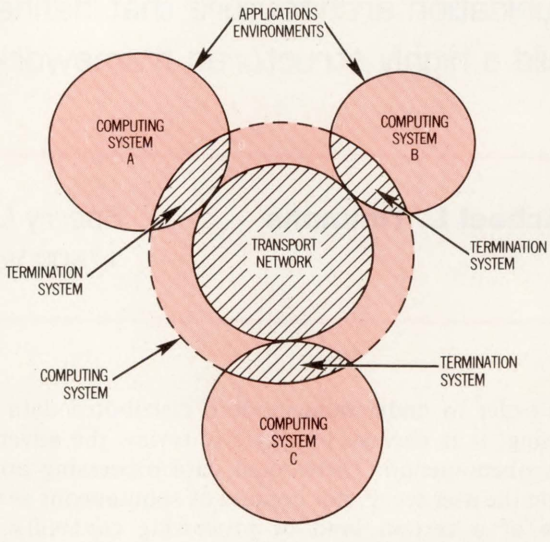

Fig 2 Communication system components. One local termination system interfaces with each application system environment. Remainder of communication system, called transport network, moves information from one physical location to another by linking paired termination systems

Communication System Components

Within the communication system, a further subdivision distinguishes those functions related only to the job of moving information from one physical location to another from those functions concerned with the application system environment interface. An architecturally defined component called the transport network moves information between interface regions—called termination systems—and therefore between computing systems (Fig 2). The transport network portion of the communication system consists of one or more control components interconnected by a transmission facility, which is the physical link connecting the network processors and into which the transport network control components have been mapped.

Functioning as a bridge between the application system environment and the transport network, the termination system provides a number of logical ports into the network through which communication system users can establish logical connections, called sessions, with other communication system users. These logical port sessions are bidirectional logical paths through the communication system, across which termination systems send data. Thus, as its name implies, the function of the transport network is to transport or convey units of information (called port data units) between paired termination systems.

The transport network control component is a portion of the transport network. Each transport network control unit provides a logical service facility for its portion of the information path between paired termination systems. Architectural layers into which each transport network control component can be partitioned are data unit control (DUC), route control (RTC), and trunk control (TC). DUC is responsible for managing the logical interface between a termination system and the transport network. RTC determines the transport network route, or path, a network data unit should travel in order to reach its paired DUC. TC controls the flow of network data units between transport network control components. Each TC regulates trunks, defined as the logical paths between two transport network control components. Trunk control selects the proper trunk protocol or subarchitectural interface to be used in transporting each network employed in transporting individual network data units to the paired TC, providing a flow control mechanism between the two TCs.

Application System Environment

Application systems are logical entities that reside outside the DCA communication system. DCA recognizes their existence, since they are the sources and destinations of data passing through the communication system. It further defines a logical structure inside the application system consisting of two logical elements called communication system users and end users. The communication system user supports the DCA interface between an application system and the communication system. The application system gains access to the communication system through the local termination system. Communication system users provide control and addressing structure for end users. End users, as the name implies, are the actual operators of the network. Application programs, terminal devices, and even terminal operators are all classed as end users under DCA.

Management Services

DCA defines a logical structure of layered protocols and interfaces to maintain the flow of information between paired communication system users across the communication system. This information flow comprises a session; major components and elements of DCA related to session activity include the communication system users, termination systems, and the transport network.

Control functions needed to initiate and terminate sessions, as well as services to monitor and maintain session activity, are all associated with the components and elements that support sessions. Collectively called management services, these control functions identify the full range of services required to support DCS session activity and are distributed among two types of complementary logical components. Application management services support communication system users and a termination system. Existing in the form of a communication system user in every termination environment, an application management component controls the attachment of communication system users to the communication system. Network management services support the transport network and are distributed such that the full range of services need not exist in all—or any—of the individual network nodes.

To establish a session between two communication system users, the combined session services of both application management services and network management services are required. Application management services on each end of the session path establish the connection between communication system users and the communication system. Network management services complement the application management services by establishing a path through the transport network connecting the two termination systems.

Each application management system is external to the communication system and is unique to its own management environment, considering such factors as the number of communication system users, their internal addressing mechanisms, and their resource handling requirements. Each application management service must also be closely tied to its termination system because its responsibilities include assigning and tailoring the logical port facilities to the communication system user.

The Second Age of Minicomputer Distributed Data Processing

The second age of minicomputer distributed data processing was launched by introduction of the DCA system on the V77-800 general purpose minicomputer. The V77 implementation follows the guidelines for network design postulated under DCA. Its actual software is based on the Vortex operating system, which evolved over many years.

Trunk protocol, or subarchitectural interface (SAI), handles data transmission across the trunk to a data communication processor or other V77 system. The trunk protocol is defined externally to DCA (hence the term "subarchitectural interface") to afford the flexibility of DCA systems implementing a variety of intercorporate protocols as required by users. The universal data line control (UDLC) protocol is the primary SAI; however, several other alternatives are offered including one using the CCITT X.25 high level data link control (HDLC) protocol for communicating with public data networks.

UDLC is a high level, bit oriented communication line procedure offered as a function of DCA. Although not a new standard or procedure in its own right, it encompasses all presently known variations of advanced data communication control procedure (ADCCP), HDLC, and synchronous data link control (SDLC). Providing for a variety of configurations such as point to point, multipoint, and switched or unswitched communication links, its design allows for efficient transmission over land, sea, and satellite paths. Several UDLC links can be active at any given time. UDLC is applicable to interactive, transaction, and batch mode transmissions. Moreover, it supports multimode transmissions among dissimilar terminals on the same circuit at speeds of up to 56k bits/s.

DCA Communication System

As implemented under V77, the DCA communication system consists of the combined termination system (TS) and transport network (TN). When data are received from the DCA network, they are first examined by the TS/TN interface, where the message header is checked for possible error conditions and the logical port is extracted from the header. When sending data to the DCA network, the TS/TN interface inserts a header in front of outbound data units. A logical port multiplexer segments user data blocks into network data packets prior to transmission across the DCA network. It also reassembles data packets received from the network, controls network data flow, and achieves the interface to various communication system users.

End users, which are V77 application or utility programs, are able to open, access, and close system resources such as other application programs, utilities, or files. When required resources are not in the same processor, a session with the appropriate processor is established using the session control interface capabilities of the V77 communication system users, PRONTO or GRAM. Session control regulates the establishment and use of communication paths between the communication system users. Incoming data contain session control headers that identify the end user for whom data are destined. For outgoing data, the session control header is generated and inserted.

The V77 transaction processing monitor, PRONTO, provides a convenient means of routing transactions from external sources, such as terminals or other computer systems, to V77 tasks written in any of the high level languages that are supported. PRONTO implements a number of convenient functions that isolate programs from the administrative issues normally required in network oriented systems. These include security validation at both terminal log on and task execution times; transaction logging for recovery, tuning, or auditing purposes; transaction routing to local V77 tasks scheduled by the Vortex operating system, remote computers, or other V77 terminals; pre- and post-processing of transaction data according to the user application; and terminal or trunk control transparency to application programs.

For applications other than PRONTO, the global resource access manager (GRAM) offers a means for users to obtain standard communication system functions. Tasks that interface through GRAM can access locally attached terminals, conduct system sessions with other end users located anywhere within the DCA network, and acquire or release files. Itself a language of commands, GRAM permits user control of resources, transmission of data to or from sources, reception of resource status information, and other related functions. It provides a complete set of standardized commands that can be used by COBOL, FORTRAN, or other languages to access local or remote resources.

Every communication processor must provide network control functions that allow users to monitor and regulate those resources for which the architecture is directly responsible. Under V77, these services include the network console processor management, error handling, session establishment, and related functions. It would be undesirable from an operational viewpoint if every V77 system required a network console staffed by a trained operator. Instead, V77 routes all network administrator traffic to one network console which controls a number of remote facilities.

The device attach family handles communication with attached terminals. Support is structured in a line protocol handler (LPH) and a real to virtual (RTV) adapter. The RTV adapter handles conversion between data and control formats demanded by the terminal and the DCA network. The terminal protocol handler function is called a terminal access module (TAM) and executes under the control of the TAM executive. The TAM interfaces with the data communications hardware via the V77 telecommunications access method, VTAM.

V77 software offers the capability to interface non-DCA systems by emulating the various terminal protocols, using TAMs specific to each protocol. The device attach facility shown in Fig 3 is a general example of this capability. Of course, non-DCA elements, by their very nature, cannot enjoy the full features of DCA such as

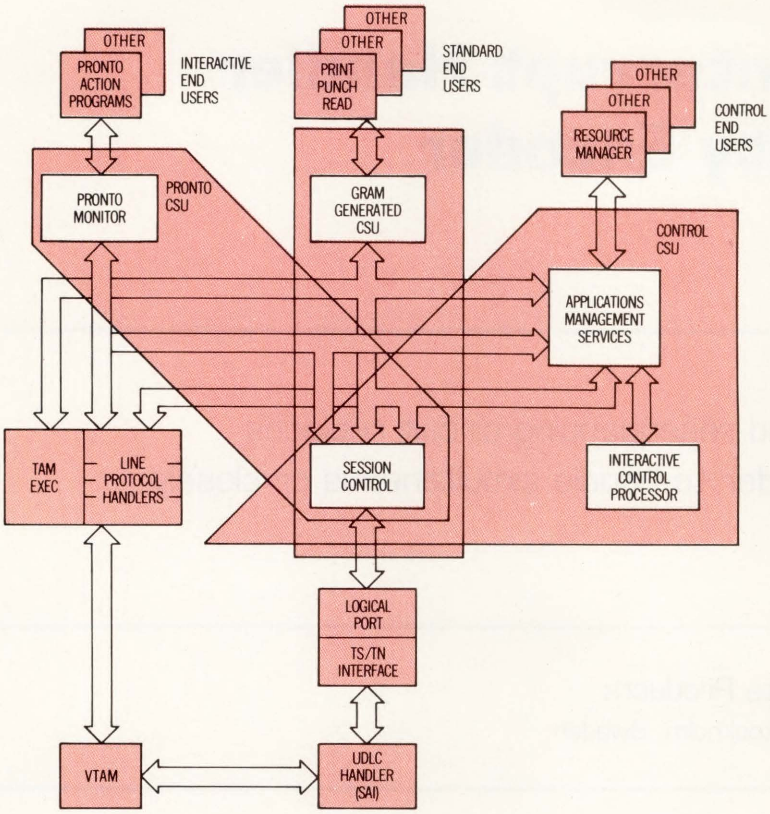

Fig 3 Elements of V77 DCA system. Transaction processing monitor routes transactions from external sources and provides end users with communication system user functions. Global resource access manager is alternative means of supplying communication system user (CSU) functions

application management services and control facilities. However, these elements can interact with application programs that may themselves be either interactive or standard DCA end users. In this way, non-DCA elements gain access to DCA structured networks.

The Future of Distributed Data Processing

Minicomputer distributed data processing will experience rapid advancement directed at the ease of use in network oriented systems by operators whose skills are oriented toward applications expertise rather than network design experience. The next age of minicomputer distributed data processing will see vendor product lines that provide features to make them appear homogeneous from top to bottom. Among these features will be distributed transaction processing, distributed file transfer, distributed program development, job distribution, distributed database management, and other distributed functions. Using these, operators will be able to improve productivity to levels only imagined a few years ago.

Currently the national sales manager for distributed data processing and network implementation at Sperry Univac Minicomputer Operations, Michael L. Timmons is a graduate of Eastern Illinois University and holds a BS in mathematics. His background includes implementation of military network processing, corporate network switching, and point of sale network systems.

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n-Dimensional Interrupt Handler Replaces Priority Encoder

Realtime interrupt queuing and resequencing circuit replaces microprocessor priority encoder to handle simultaneous or closely spaced events

Kalman Rozsa

Facit Data Products
105 45 Stockholm, Sweden

Despite their increasing speed when events occur in a realtime environment, the microprocessors' interrupt handling capability is sometimes insufficient. Events occur with varying frequency and, although the average time between them may be relatively long, a burst of closely spaced interrupts can challenge system capabilities. As frequency increases, overhead begins to limit system performance. A burst of events in realtime applications can require significantly higher performance than the average processing load. When confronted with this, designers should always investigate a pure software solution. Often, a well-designed interrupt management mechanism will provide a flexible, low cost solution to the problem of handling closely spaced interrupts.

When several events occur almost simultaneously, today's microprocessor has a predefined interrupt priority that determines which event will be processed first. Many have a number of so-called restart instructions. Once enabled onto the data bus during an interrupt acknowledge cycle, a restart instruction acts as a subroutine call to a particular address, up to eight of which can be used in the 8080, 8085, and Z80 (interrupt mode 0) microprocessors.

Outside the microprocessor, hardware allows the highest priority interrupt to generate its corresponding restart code. In most cases, a priority encoder assigns a 3-bit code to a pending interrupt (Fig 1). When combined with certain static bit values, the priority code becomes a restart code. The priority encoder notifies the microprocessor that an interrupt is pending. Then, upon completing the current instruction, the microprocessor issues an interrupt acknowledge signal to indicate that the interrupt has been accepted and gates the restart code onto the data bus. The source of the interrupt must recognize the interrupt acknowledge signal and deactivate its interrupt request to allow processing of the next event.

The event priority concept raises two problems because it is a 1-dimensional interrupt handling mechanism. It cannot handle a second or subsequent interrupt that occurs before a pending interrupt has been acknowledged by the processsor. Also, it requires a means of maintaining and perhaps resequencing the interrupt queue if multiple interrupts are queued for service in chronological order.

A 2-dimensional interrupt handling mechanism, the interrupt processing unit (IPU) addresses these problems by replacing the priority encoder in Fig 1 with a first in, first out interrupt queuing and resequencing scheme that allows event priority to affect the output sequence. Whereas 1-dimensional interrupt handling requires only combinatorial logic, a 2-dimensional

(continued on page 128)

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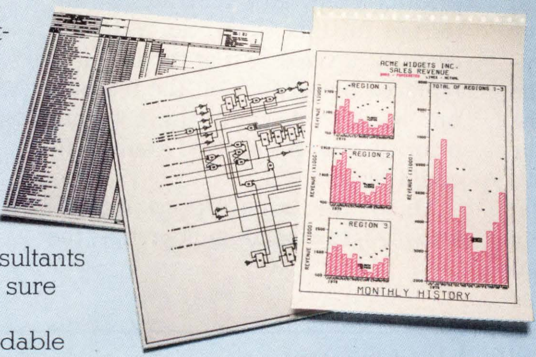

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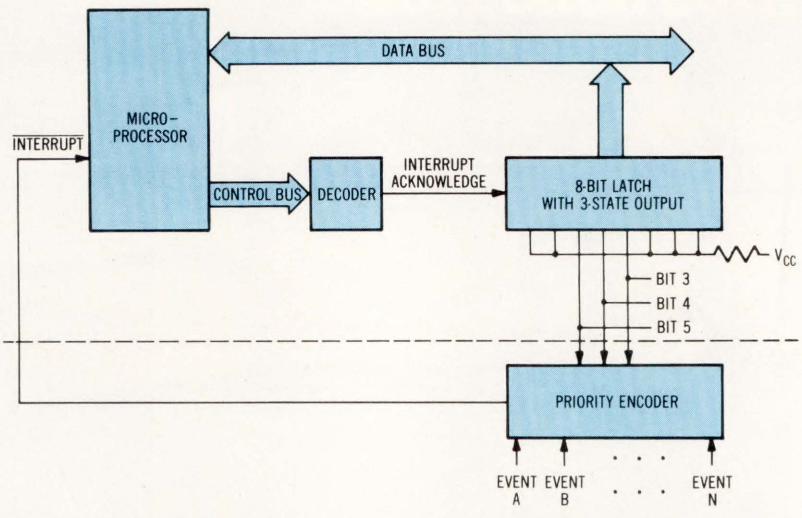

Fig 1 One-dimensional interrupt handling. Assigned by priority encoder to pending interrupt, this 3-bit priority code is combined with certain constant bit values to generate restart instruction

scheme must include some sort of memory storage. Attached to the microprocessor data bus by means of an 8-bit latch, the IPU responds to events at virtually any frequency and generates interrupts at a controlled rate appropriate for the microprocessor. Thus, it adapts the true realtime event frequency to the processor response time, and achieves a controlled, flexible, situation dependent priority among events. It smooths out the high frequency bursts of multiple realtime interrupts, maintains and redefines event priority, monitors the overall interrupt environment, and notifies the microprocessor of abnormal situations.

In Fig 2, two different events, A and B, enter the IPU in a random sequence. Within the IPU, these events are placed in a queue from which they emerge as interrupt requests generated in a reordered, well-defined sequence. For simplicity, this explanation first assumes that event A always has the highest priority; no B event will be presented as IPU output while an A event remains stored in the IPU. The microprocessor receives interrupts from the IPU at a frequency limited only by its interrupt handling capability. However, IPU characteristics now determine the interrupt sequence. In Fig 2's simple example, the IPU selects the highest priority event and generates an interrupt for that event. So, although event B_1 arrived first at the IPU, it is replaced by event A_1 at the IPU output because A events have higher priority and A_1 arrived before B_1 could be serviced.

Once the microprocessor acknowledges a pending interrupt, the IPU removes it from the queue and issues the next interrupt. The length of the interrupt queue increases as events enter the IPU and decreases as interrupts generated by the IPU are acknowledged by the microprocessor. The state diagram in Fig 3 illustrates basic IPU operation. Up to three A events and three B events can be handled using the 4 x 4 cell matrix shown, and all possible combinations are allowed. An address pointer indicates the current IPU state by addressing one of the cells in the state diagram. As events enter the IPU, the pointer moves downward for B events, to the right for A events, and diagonally downward to the right for a simultaneous combination of one A event with one B event [Fig 3(a)]. As IPU generated interrupts are acknowledged, the pointer moves left to remove an A event from the queue. It moves upward to remove a B event, provided that it addresses a cell in the leftmost column, indicating that no A events remain in the queue [Fig 3(b)].

To implement the 2-event IPU, a storage device is partitioned into sufficient cells to handle the maximum queue sizes. Assuming two events with queues that may differ in length, the number of cells required in IPU storage is the product of one more than the maximum queue sizes. A pointer references
(continued on page 130)

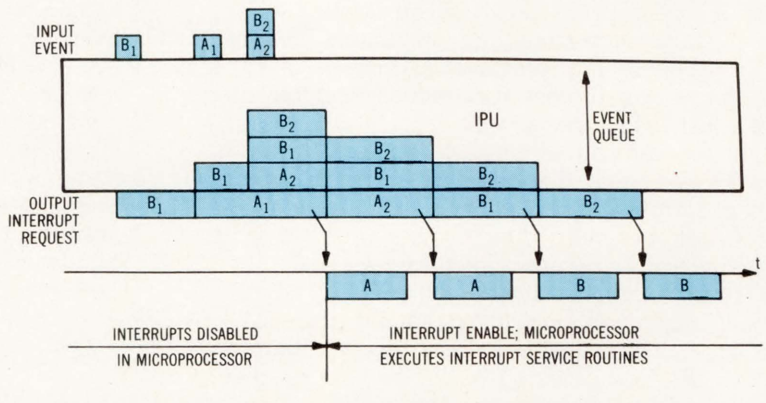

Fig 2 Two-dimensional interrupt handling. Random sequence of input events can include simultaneous events. IPU queues multiple events, resequences event queue, and presents as output well-defined sequence of properly spaced interrupt requests. Once microprocessor acknowledges interrupt, IPU removes event from queue and requests interrupt for next event

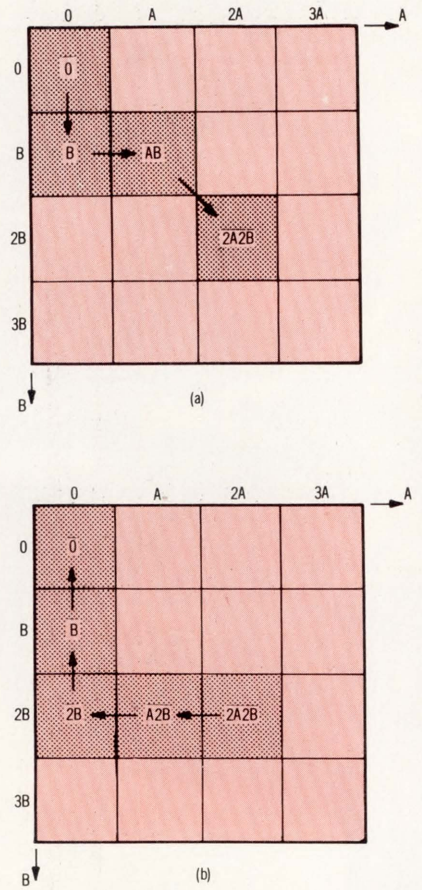

Fig 3 State diagram of basic IPU operation. Pointer designates IPU state by addressing storage cell. In (a), input events change IPU state by moving pointer downward for B events, to right for A events, and diagonally downward to right for simultaneous A and B events. In (b), interrupt acknowledge removes events from queue by moving pointer to left, as A event interrupts are acknowledged, then upward, as B events are acknowledged

one cell within the array; the position or address of the referenced cell then indicates how many A events and how many B events remain to be serviced. Event input and output operations manipulate the pointer; entering events move the pointer downward or to the right (or both); and, an interrupt acknowledge moves it upward or to the left.

Made up of several memory locations, each cell in IPU storage supplies an appropriate restart code that generates the restart instruction, and the address of the next cell to be addressed by the pointer that follows an interrupt acknowledge. Using the procedure diagrammed in Fig 4, a truth table can be constructed to determine IPU storage location values. Fig 4(a) shows possible paths that the pointer can take from a generalized storage cell outside the leftmost column. Beginning in cell 11 (hexadecimal) of the 8- x 4-cell storage matrix that shows one A event and two B events waiting to be accepted by the microprocessor, six possible paths reflect the eight possible combinations on the three input lines (event A, event B, and interrupt acknowledge).

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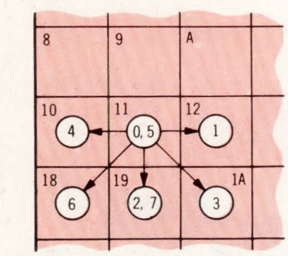
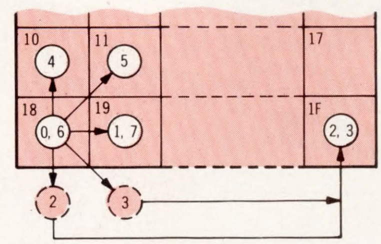


INTERRUPT ACKNOWLEDGE ←	EVENT B ↓	EVENT A →	RESULT	EXPLANATION
0	0	0	0	NO CHANGE
0	0	1	→	GO TO CELL 12
0	1	0	↓	GO TO CELL 19
0	1	1	→↓	GO TO CELL 1A
1	0	0	←	GO TO CELL 10
1	0	1	←→	NO CHANGE
1	1	0	←↓	GO TO CELL 18
1	1	1	←↓→	GO TO CELL 19



INTERRUPT ACKNOWLEDGE ↑	EVENT B ↓	EVENT A →	RESULT	EXPLANATION
0	0	0	0	NO CHANGE
0	0	1	→	GO TO CELL 19
0	1	0	↓	OVERFLOW, GO TO CELL 1F
0	1	1	→↓	OVERFLOW, GO TO CELL 1F
1	0	0	↑	GO TO CELL 10
1	0	1	↑→	GO TO CELL 11
1	1	0	↑↓	NO CHANGE
1	1	1	↑→↓	GO TO CELL 19

Fig 4 IPU truth table. Portions of 8- x 4-cell matrix show cell addresses in hexadecimal. In (a), current state (outside leftmost column) permits six possible future states, depending on three input parameters that can assume eight possible values. In (b), current state within leftmost column also permits six possible pointer changes, two of which here fall outside cell matrix and therefore reflect event queue overflow

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Fig 4(b) shows possible pointer modifications when the pointer addresses a storage cell in the leftmost column. Here, the pointer addresses cell 18, indicating that three B events and no A events are waiting to be accepted. As before, each of the eight possible input combinations generates one of six possible pointer changes. However, because cell 18 corresponds to the maximum number of B events, two of the possible input combinations direct the pointer to cells that are not implemented. This event overflow situation can be detected by reserving one storage cell (cell 1F in this figure) and directing all states that fall outside the storage cell matrix into the reserved cell. The event overflow interrupt defined in the overflow cell should generate a unique, high priority restart code that informs the microprocessor of the overflow condition and directs remedial action.

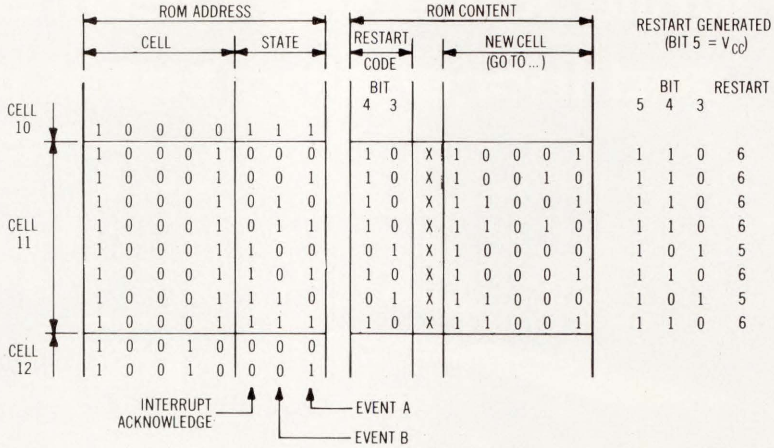

Fig 5 IPU storage data. ROM is partitioned into 8-byte cells. Five most significant bits of cell address correspond to cell number in Fig 4. Three least significant address bits correspond to three input lines. For each combination of current state and input value, ROM data supplies appropriate restart code and new cell number to be loaded into pointer

Fig 5 shows how the storage cell matrix might be implemented in hardware. A read only memory (ROM) of sufficient size is partitioned into cells according to the maximum queue sizes. Every cell contains eight memory locations in this example. Then, to realize the situation shown in Fig 4, the ROM requires 32 cells of 8 positions each, or 256 locations. For each ROM location, the five most significant bits of its address designate its cell number, and the three least significant address bits correspond to the three input variables. Data contained in ROM locations give the appropriate restart code and the new pointer value for each combination of cell number and input values.

Basic IPU hardware incorporates the storage device and the pointer latch (Fig 6). IPU inputs should be synchronized and formed with the circuit shown in Fig 6(a). This converts the rising edge of the input pulse (event X) into a pulse of well-defined length that is synchronized to the clock (INTERRUPT x). If a ROM with suitable access time is used, the IPU clock can be the central clock for the microprocessor. A single OR gate sets the INTERRUPT flipflop if any of the restart bits is set [Fig 6(b)]. The initial reset forces the pointer to start from the empty queue position, cell 0 in the storage cell matrix.

The IPU approach is not limited to only two events, nor is it restricted to a fixed priority interrupt handling mechanism. An IPU for three or more events can be implemented by selecting a suitable ROM and allocating a multidimensional matrix of storage cells [Fig 6(c)]. Alternative priority schemes are achieved by simply changing pointer address values in ROM. Several useful interrupt handling schemes are quite easy to implement. For example, when the IPU contains a combination of multiple A and B events, an event pacing scheme could generate alternating A-B-A-B interrupts. Particular combinations of pending events could issue particular restart codes or, perhaps, no restart code at all. Only every second or third event might generate an interrupt. Also, the IPU could distinguish between positive and negative events (eg, clockwise or counterclockwise rotation) and send interrupts to the microprocessor accordingly; then, closely spaced events migh cancel each other out under certain circumstances, and the IPU would eliminate all microprocessor overhead involved in processing self-canceling pairs of events. Finally, an event management scheme can handle multiple events very effectively by replacing a series of individual interrupts with a single interrupt, keyed to the particular combination of events, that will be interpreted by the microprocessor. A sufficiently large ROM could hold two or more such alternative priority schemes, from which microprocessor software could make a selection by using the SELECT signal in Fig 6(c).

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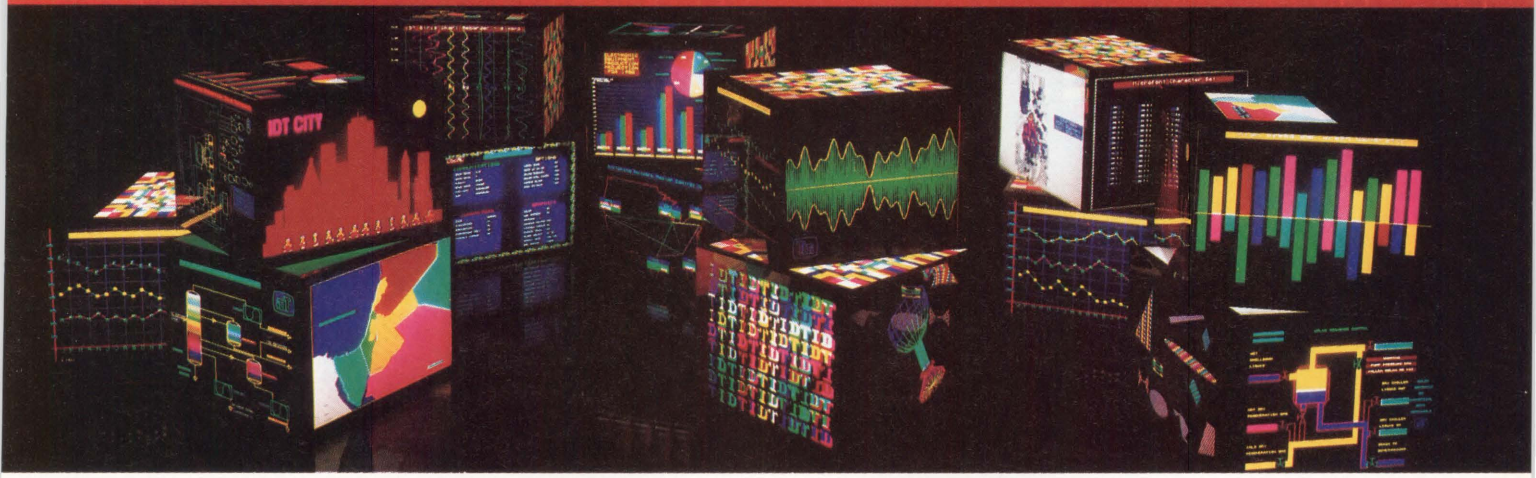

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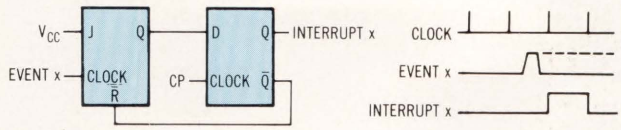
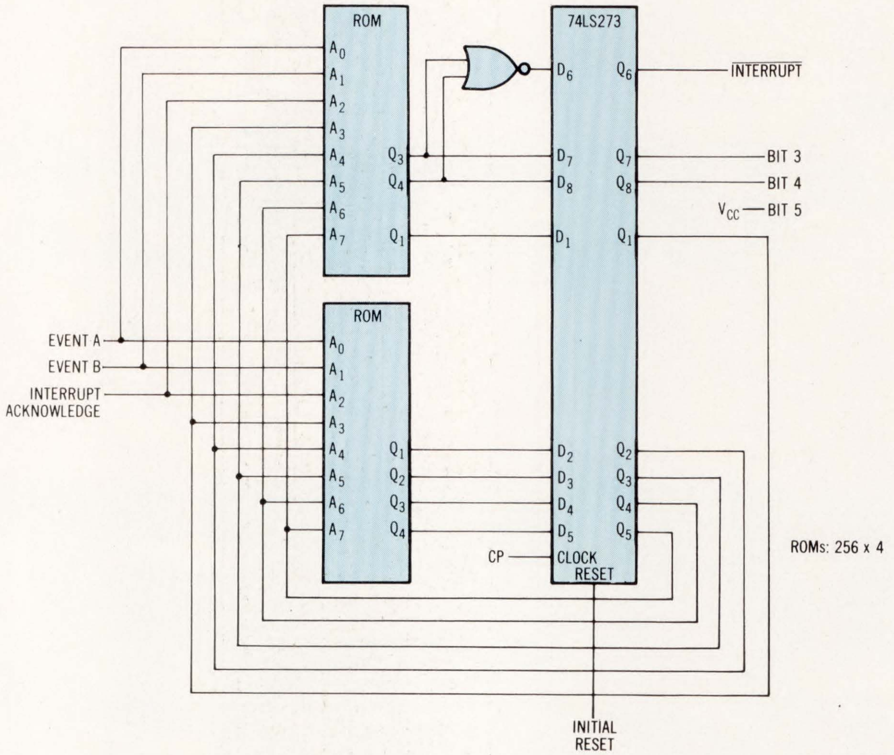
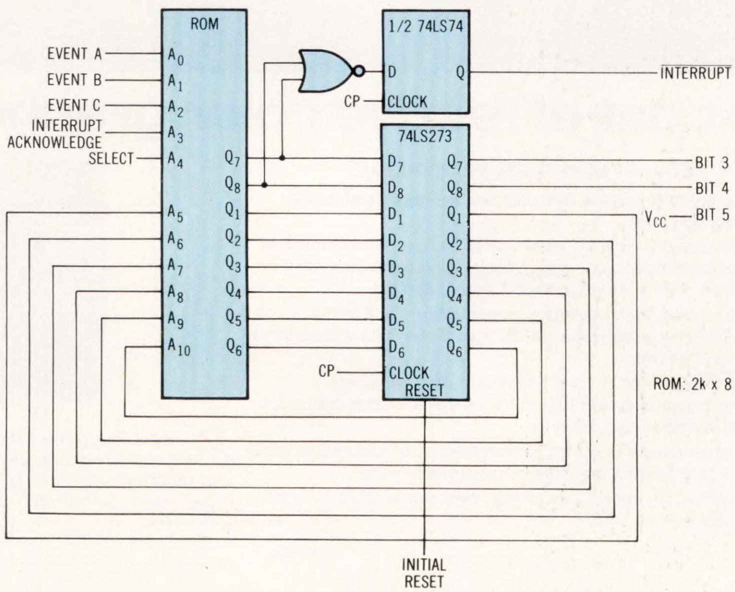


(a)



(b)

Fig 6 Hardware implementation. Basic circuit incorporates storage device and pointer latch. Inputs should be synchronized and formed using circuit shown in (a). In (b), 256- x 4-bit ROMs implement 2-event IPU from Figs 2 to 4. Extension to three events establishes 3-dimensional cell matrix using 2k- x 8-bit ROM as shown in (c). For three queues of four events each, this size ROM holds two complete 3-dimensional cell matrices, one of which can be selected by software



(c)

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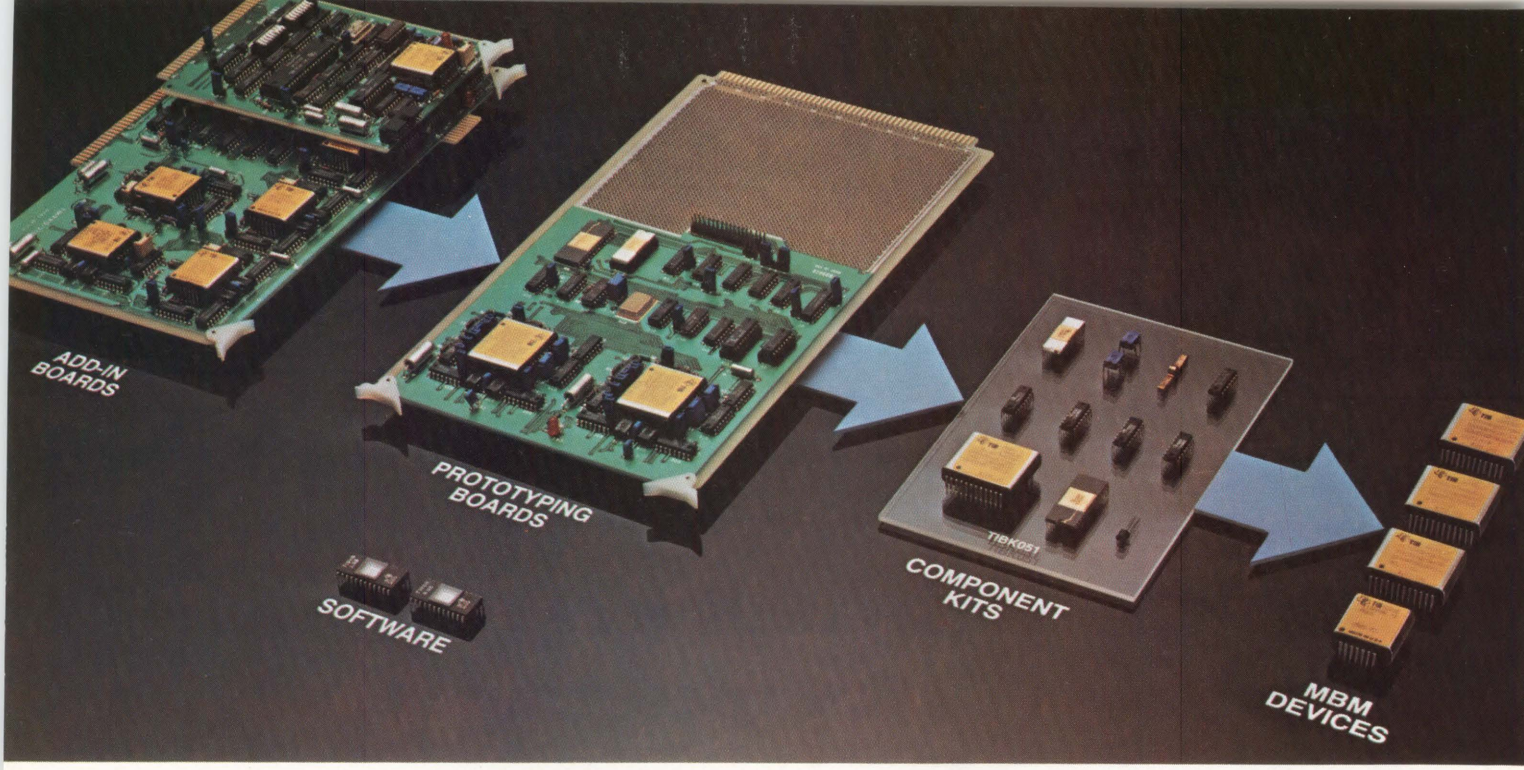

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As data processing systems become more complex, the equipment used to maintain and diagnose these systems has to, by necessity, keep pace. Concurrently, requirements for reliability and fast, efficient service are magnified. Traditionally, service has been provided by expanding field engineering staffs, developing more sophisticated test equipment, and intensifying field staff training in the hardware and software technology of these more complex products.

To meet this magnification of needs in a slightly different fashion, a detached diagnostic terminal, STC 3910, consisting of a Z80 microprocessor, a 5″ (13-cm) full ASCII keyboard, floppy disc, and 16 bytes of random access memory (RAM), was developed. This portable, offline, intelligent device is used locally and remotely to maintain and/or diagnose a variety of peripheral subsystems. Utilizing advanced microelectronics for efficient and effective diagnostics and ease in programming on any subsystem, the design allows for adaptation to a variety of applications including data collection and transfer, limited logic analysis, and microcode development and writing.

Basically, the device detects and isolates failures on a subsystem through its microprocessor, eliminating the need to tie up valuable central processing unit (CPU) time. Such diagnostic tests as functional and reliability checks, artificial stress testing, and fault isolation are run at a reduced cost. With appropriate microcode, additional tests for other equipment can also be programmed onto cards and inserted into spare card slots.

To function remotely, the device is connected to a standard RS-232 interface that operates an acoustic coupler. Data are then transmitted via telephone lines to a remote location for further interpretation, allowing more rapid diagnosis and repair. Remote diagnosis enables the field engineer to determine exactly what is wrong with a peripheral, and what is needed to repair it, before going to the installation. This results in a reduction

(continued on page 138)

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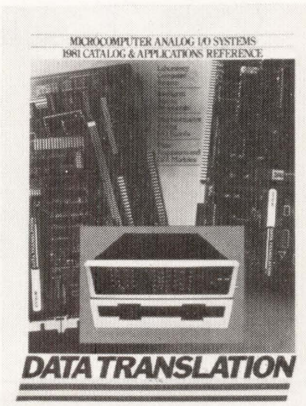

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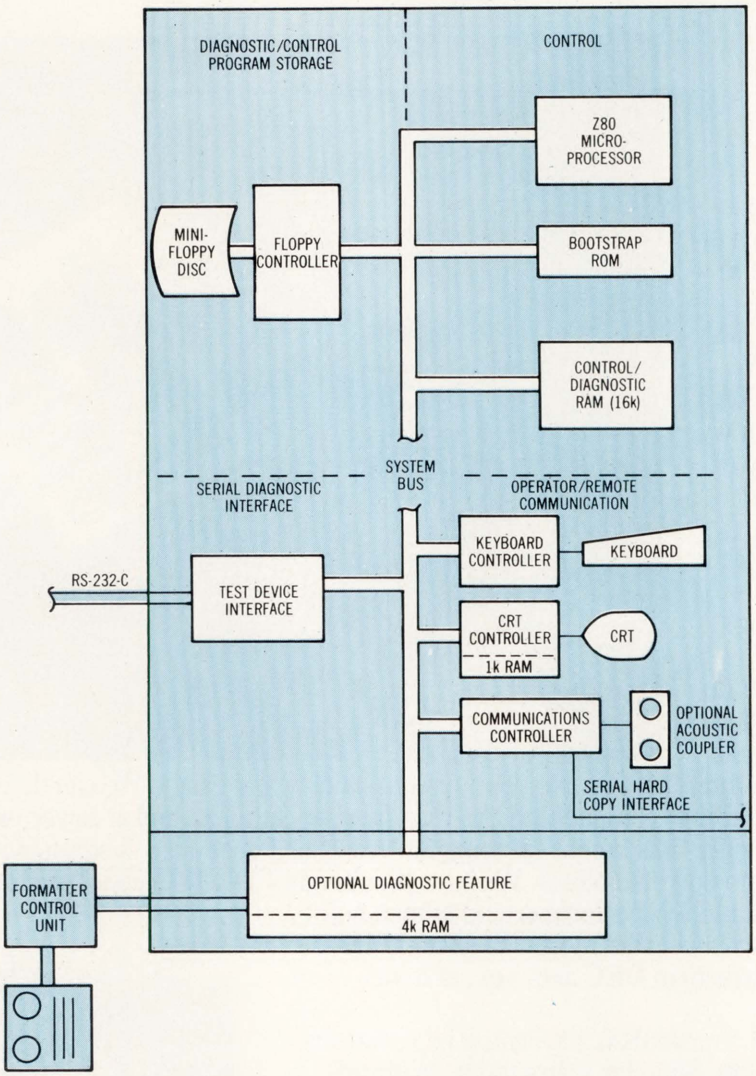

Fig 1 Detached diagnostic device block diagram. Four separate sections provide control, storage, serial diagnostic interface, and communications capability

in time spent and in trips between installations and field offices. Because it weighs less than 40 lb (18 kg) and runs off standard wall current, the device is portable to almost any location.

When the device is not in use, the acoustic coupler can be unplugged and a printer attached to the same port. Although it comes with cathode ray tube (CRT) screen, the device also can print out a permanent record of diagnostic tests and results that serves to document maintenance and repair activities.

Hardware Design

Fig 1 shows the diagnostic monitor divided into four sections: control, program storage, serial diagnostic interface (SDI), and operator/remote communication (COMM). The control and program storage are on one circuit card while the SDI and the COMM are contained on a second card with two extra slots in the card cage to permit options.

The Z80, which runs at 4 MHz, was chosen because of its large instruction set that includes bit test, set, and reset; its various interrupt modes; its automatic refresh of dynamic RAM; and its two index registers. To take advantage of the bit test instructions, the input/output (I/O) responds to memory addresses rather than I/O addresses (memory mapped I/O). Any loss of memory address space is offset by the increase in speed.

The CRT was chosen because it displays 16 lines of 64 characters each, yet is lightweight and small, and uses 12-V dc. Interface to the display provides direct access to the CRT refresh memory from both the Z80 and the CRT controller and allows CRT refresh without stealing cycles from the Z80.

Since the refresh memory is directly accessible from the Z80, scrolling is done in software, allowing splitting of the screen into scrolled and unscrolled (fixed) areas. The fixed areas of the screen are used to display data that change rapidly, such as status bits; and because the data location is fixed, information can be easily read, even as it changes. For additional display, four light emitting diodes (LEDs) on the processor circuit board serve as indicators for the wake-up diagnostics.

The full alphanumeric ASCII keyboard with two special function keys, machine reset and nonmaskable interrupt, was chosen because of the flexibility it gives for future applications and because it is an off-the-shelf item. Its controller is an 8-bit I/O port. Designed to use a 5.25" (13.34-cm) mini-floppy drive, with an associated single- and double-density controller, the diagnostic monitor uses both formats, under software control.

Wake-up diagnostics that run on power-on or machine reset, a bootstrap program, and more extensive tests for RAM and the floppy drive are contained in the device's 1k-byte programmable read only memory (P/ROM). A more complete set of diagnostics can be run from the mini-floppy after proper operation of the mini-floppy and memory

(continued pn page 140)

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CIRCLE 67 ON INQUIRY CARD

are verified. The 16 bytes of dynamic RAM, to be used by the functional program, were chosen primarily because of their low cost, a cost decreased further with the automatic refresh capability of the Z80.

Two serial interfaces are provided, the SDI to connect to the device being tested and the COMM to provide remote diagnostic capability and to connect to the acoustic coupler through an external connector on the top of the device. Both interfaces have either RS-232 or 20-mA current loop capability.

In the COMM connector, data transmit and receive, carrier detect, and a signal to select originate or answer mode in the acoustic coupler are implemented. In the SDI connector, transmit and receive data, dataset ready, data terminal ready, and receive clock are implemented. The 20-mA current loop in the SDI interface can be either active or passive (as selected by jumpers on the logic card), but the COMM interface has an active loop only. When data are being transmitted through either interface, they are sent through both RS-232 and current loop; when data are being received, either RS-232 or current loop must be selected under software control. The transmission rate is programmable from 110 to 9600 bits/s and can be sent independently for each interface, both of which use universal synchronous/asynchronous receiver/transmitter (USART) chips.

Software Design

STC 3910 software, divided into P/ROM resident firmware and the internal diagnostics, resides on floppy disc. Firmware in P/ROM is accessed either by power-on or by using the reset or interrupt keys. The P/ROM contains a set of wake-up diagnostics, which runs automatically on machine power-on; the programming necessary to execute a set of debug commands; and several in-depth diagnostics for the device.

At power-on or keyboard entry of reset, the Z80 is initialized to address the P/ROM and to start the execution of its firmware. The four LEDs located on the processor circuit board light up and stay on for 2 s. During these 2 s, further execution of the power-on/reset sequence is cancelled by typing the interrupt key, thus generating a nonmaskable interrupt and allowing reset without destroying the contents of memory. After 2 s, the P/ROM begins executing a set of functional diagnostics. As each test begins, it displays a unique pattern in the LED. If any test fails, it automatically loops and is identified by the code in the LED. This allows malfunctions to be diagnosed without depending on the proper operation of the CRT.

The first diagnostic, a P/ROM checksum test, reads the full P/ROM and verifies the sum of the data contained in all P/ROM memory locations. The processor test then checks all Z80 functions, none of which involve reading or writing RAM since RAM has not been tested yet. Once basic processor operation is confirmed, the RAM test writes and verifies all locations in dynamic RAM. The floppy drive controller test then checks the data, and sector and track registers in the floppy controller; the CRT test verifies the CRT refresh RAM, initializes the CRT, and displays the full character set. Using specially designed circuitry that loops the write path to the read path, the communications test then verifies operation of COMM USART. If the test is successful, basic functions are verified and the command mode is entered. Any wake-up diagnostic can be run once or run in loop mode on request.

P/ROM command mode provides various debug operations and a bootstrap loader which loads the first track from a mini-floppy disc. A bootstrap load can also be performed through the COMM USART, providing diagnostic capability without depending on proper operation of the floppy disc drive. P/ROM firmware provides access to a memory address register, allowing the selection of a specific address, examination of the contents of that memory location, changing of the contents, and stepping forward through memory from that address. Another P/ROM command performs a jump to the address selected by the address register. If the nonmaskable interrupt key is typed during execution of any program, the program counter is displayed in the address register and control passes to the command mode portion of the P/ROM firmware. There is a command available to clear the CRT screen and reset the stack pointer.

In addition to the bring-up diagnostics and debug capabilities, the P/ROM provides interrupt vectoring and two in-depth diagnostics. When an I/O interrupt occurs, the Z80 jumps to a fixed address in P/ROM. That address contains a vector to dynamic RAM, where software routines poll all I/O devices to determine which device generated the interrupt. Running only upon request, the in-depth diagnostics contained in P/ROM consist of a floppy read test, which reads a specially written track on the floppy disc and verifies each byte of data, and a memory test, which writes and verifies a "walking 1s" pattern through dynamic RAM.

Internal diagnostics are a set of routines on floppy disc that perform functional and fault isolation testing. The floppy resident processor test is divided in two sections. One section tests all internal processor functions, such as register transfers and jumps, and any other function that does not reference memory; the other tests all instructions that read and write memory and is subdivided into a test of normal read and write instructions and a test of those instructions that cause memory cycles to be executed in uninterrupted succession, eg, INC HL, which causes a read followed by a write. After these tests are complete, processor interrupts are tested.

Additionally, several utility programs are contained on the disc, offering convenience and a monitor program to control the operation of the diagnostics and utility programs. The monitor is loaded with the P/ROM bootstrap, and each test is selected by name and has options, such as printing the test title or looping the test.

(continued on page 142)

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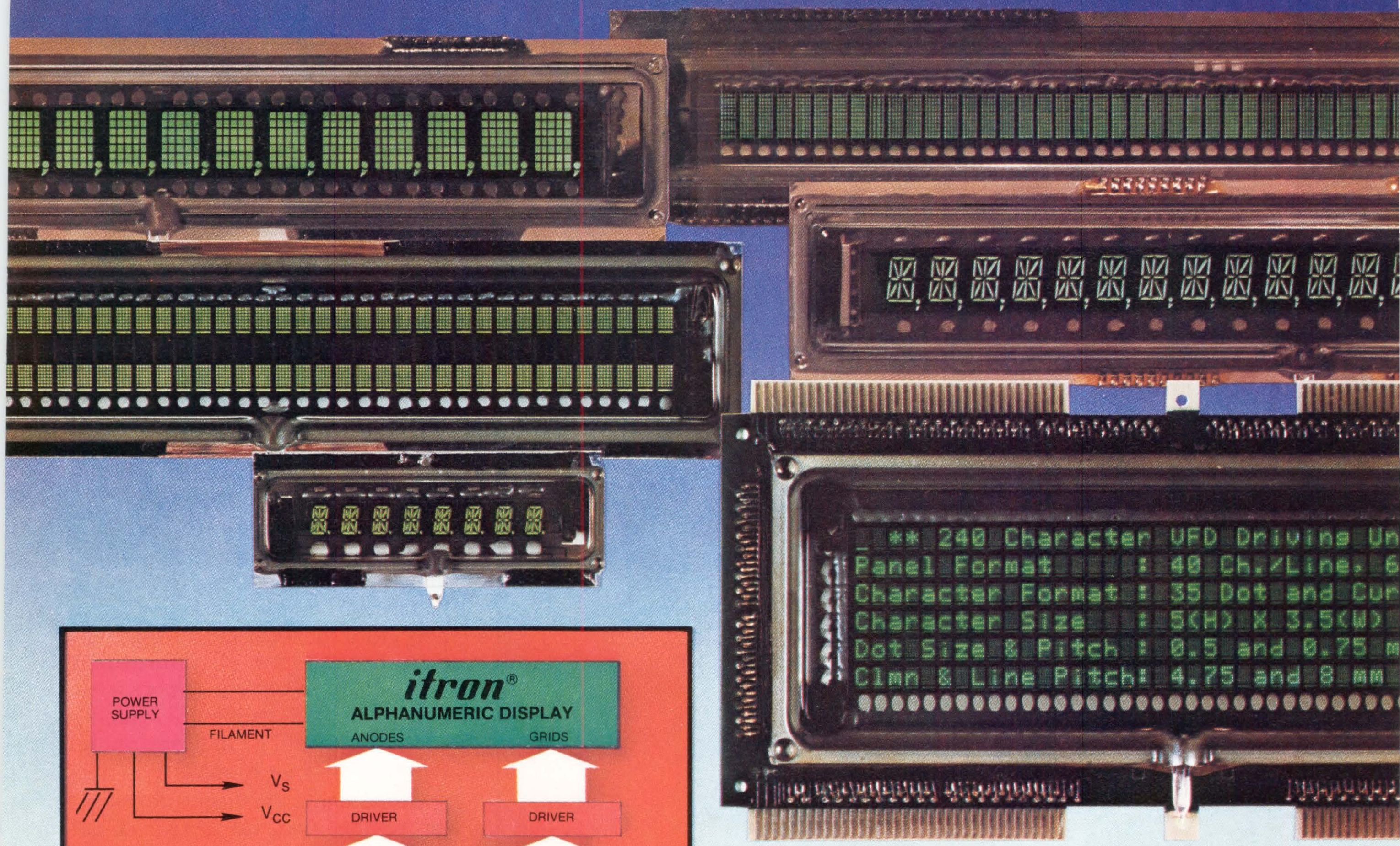

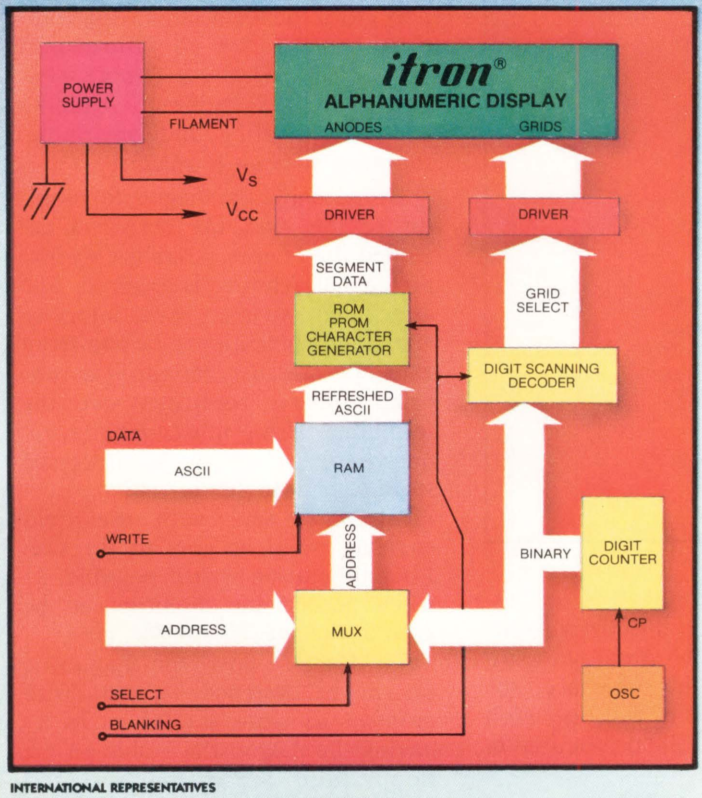

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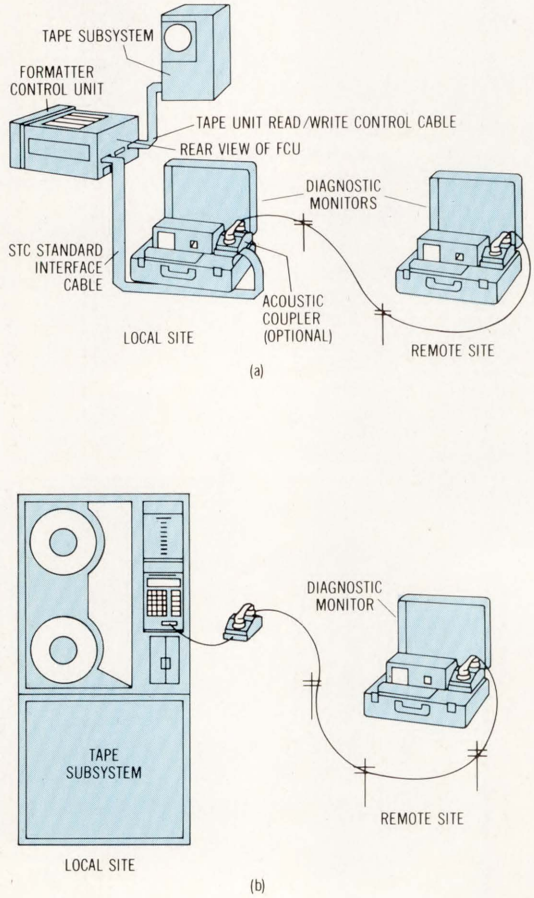

Fig 2 Remote operation. Remote console capability allows control over all diagnostics and monitor functions from a remote location using acoustic coupler (a). With tape subsystem in (b), extended remote capability requires no local diagnostic monitor connection

Diagnostic Test Packages

Currently, the monitor is used to test the STC 1900 and 4500 tape subsystems, with different methods of attachment and different goals for each. [See Figs 2(a) and (b).]

Attachment to the 1900 subsystem is done by inserting a special interface card into a spare slot in the monitor and then attaching it to the standard interface of the 1930 or 1935 formatter control unit (FCU). This card contains a 4-byte high speed RAM buffer and the circuitry necessary to attach it directly to the high speed, parallel data, standard interface. With this interface, the tape can be tested at full operation speed with any of the drives used in the subsystem.

The 1900 tape subsystem diagnostic package is coded in a special high level diagnostic language that is interpreted by the monitor and provides intimate stimulation and examination of the hardware while improving efficiency of the code and reducing memory requirements. It is defined to be independent and unrelated to the machine language of the monitor. Fault isolation, artificial stressing, functional, and reliability tests are performed on the formatter and the attached tape drives. The diagnostic monitor also provides remote console capability that permits control of all the diagnostic and monitor functions from a remote location using the acoustic coupler.

All functions available to the local field engineer are available at the remote location, including sending messages between the two locations and running all or any of the diagnostics using any options. Also, special diagnostic programs can be written from either location. It takes about 5% more time to run the diagnostic package if the remote option is used since the transmission rate over the telephone is at approximately 30 characters/s. The remote feature can also be used for display only, with the local site having complete control, but all information being displayed at the remote location. This is valuable for training and demonstrating, and for troubleshooting difficult problems.

By attaching the diagnostic monitor to the 4500, the designers extended the remote capability so that no local attachment is required. The attachment is via an RS-232 interface enabling diagnostics to be run from a locally attached monitor or run, using modems, completely over the telephone. Using this capability, requests for service can be processed from a remote center and replacement parts sent with the field engineer when he goes to the site. Local operation is still possible, so when needed the monitor can be used at the site.

To decrease cost, the diagnostic system is designed to run with modems as slow as 300 bits/s by having the diagnostics reside on the floppy disc inside the 4500 and having the error messages reside on the disc inside the monitor, so that only an error code and a few modifier bytes have to be transmitted between the two devices. If there is no monitor at the site, the diagnostic package can be run in a

(continued on page 144)

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The SM-810-002 is the second in a series of dot matrix display systems. Its field of 20 half-inch characters provides outstanding viewability as a result of 75fL typical brightness and a 130° viewing angle. Like its predecessor, the 40 character SM-810-001, it is microcomputer controlled. It can be used in process control, instrumentation applications, business equipment and a variety of terminal, as well as other OEM designs, including point-of-sale equipment, industrial controls and computer peripherals.

Interfacing is greatly simplified because the display system incorporates an 8 bit bidirectional parallel data bus — a design that can be used with either a parallel ASCII keyboard or an outboard microprocessor. In either case, the unit can generate a continuous display or accommodate updating of real time data from either an operator monitored process or an instrument.

All of the operational features of the SM-810-002 are the same as those of the 001; however, the larger characters of the 002 appear brighter and, of course, can be read from greater distances.

Both display systems have the ability to blink a field that includes 96 standard ASCII symbols and the degree sign, plus the Greek letter "Mu." In addition, the SM-810-002 accommodates left-to-right data entry. Mounted on a compact PC board, it incorporates a custom masked μC with 1K of ROM. Powered by a single 5V supply, the SM-810-002 dissipates only 8.75W (typ).

The microcomputer's built-in intelligence simplifies the setup of special messages: An operator can completely blank, and then unblank, the display to generate a message immediately; or, can scroll a message from right-to-left. A self-test feature is also included.

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CIRCLE 70 ON INQUIRY CARD

go/no-go mode from a small panel located inside the drive. Additionally, software can be patched over the phone line.

Wake-up diagnostics that run at power-on and perform a functional test prior to the subsystem coming on line to the CPU, online diagnostics that run at the same time the customer is using the tape subsystem, and offline diagnostics that run only when the customer is not using the tape subsystem make up the 4500 diagnostic package. Online and offline diagnostics are further divided into level 1 tests that perform functional testing and are used to select the proper fault isolation test(s) to run, and level 2 tests that perform fault isolation to the card level.

Wake-up tests are used to check out the tape subsystem as thoroughly as possible in 30 to 60 s without moving tape, while the online tests share the processor of the 4500 with the functional program so that they can run while the subsystem is being used for normal operation. The tests usually require that one tape drive of the subsystem be offline, but the others may be used for normal operation. If the system cannot be fully tested with online diagnostis, the entire subsystem can be taken offline and the offline diagnostics run for complete isolation.

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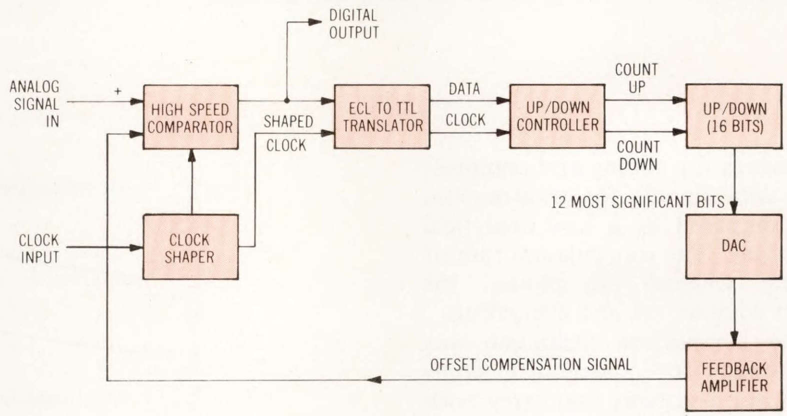
Offset Compensation for A-D Converters

Digital feedback circuit eliminates offset in the analog input and offset introduced by the A-D converter

An analog to digital converter (ADC) eliminates dc offset in the final digitized signal as well as in the analog input by using digital feedback for compensation. Because the circuit does not require capacitor or transformer coupling of the analog input, its frequency response is not limited by the frequency characteristics of such components. It is useful in data processing applications in which analog format data are entered at high rates—for example supermarket and department store point-of-sale data input systems.

In the digital feedback circuit, an up/down counter integrates the ADC output (see the Figure). Counter output is fed back to the ADC input through a digital to analog converter (DAC) and an amplifier. The feedback signal cancels the dc offset when, on the average, the A-D output has an equal number of plus ones and minus ones. The feedback circuit not only compensates for offset but measures it as well, since the digital value stored in the up/down counter is linearly proportional to the offset.

In one version of the converter, the high speed comparator and clock shaper are composed of fast emitter-coupled logic (ECL) ICs. The up/down controller and up/down counter use moderate speed TTL IC, which are adequate for a 40-MHz clock rate (a translator interposed between the high speed comparator and the up/down controller converts current and voltage levels to make the two types of logic compatible). If ECL circuits were used exclusively, a clock rate of 100 MHz could be accommodated.



A-D converter. Consisting of ECL clock shaper and high speed comparator circuits, it has dc restoration that is generated largely by TTL circuits. Digital output is integrated by up/down counter, and resultant is reconverted to analog form as offset compensation signal

The high speed up/down controller handles the serial input bits in pairs. It sends an up clock pulse to the up/down counter if both bits are plus one, a down clock pulse if both bits are minus one, and no clock pulse if the two bits are different. In effect, the up/down controller acts as an additional counter stage, reducing the clock rate to the up/down counter by a factor of 2. The controller also keeps the 16-bit up/down counter from overflowing, if the offset is too large, by inhibiting counting for minimum and maximum values of the counter.

The 12 most significant bits of the up/down counter go to the DAC. Feedback amplifier output, which is applied to the negative input of the high speed comparator, is equal to the input offset voltage plus any offset introduced in the ADC.

Note

This work was done by Stanley S. Brokl and William J. Hurd of Caltech, Pasadena, Calif, for NASA's Jet Propulsion Laboratory.

Comparing Data Transmission Systems

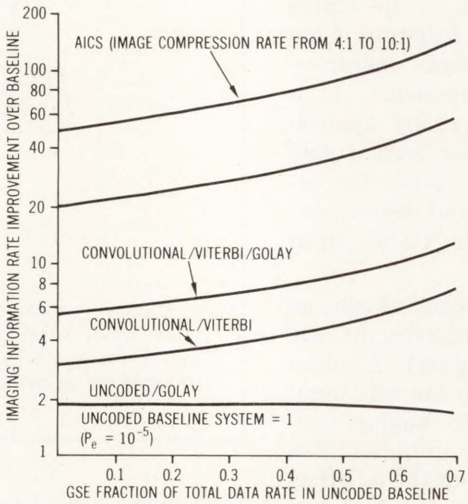
The transmission rates of schemes for transmitting image and scientific data are graphed for easy comparison

Schemes for coding and compressing data signals for transmission are compared by a new analytical technique. The transmission rate of several schemes are plotted for direct comparison and evaluation.

The comparison technique was developed for spacecraft communication systems that carry both image data and general science and engineering (GSE) data signals. Usually, GSE data demand much lower error rates than image data. By using the new comparison method, it is possible to select an efficient transmission scheme, while ensuring that the error rate requirements of all data are satisfied.

In the analysis, it is assumed that the GSE transmission rate is fixed and that this rate is the same for all systems being compared. One system is selected as a reference or baseline by fixing an allowed probability of error. Its maximum information transmission rate is determined by fixing an allowed probability of error and considering such factors as its power and antenna capabilities.

The image data transmission rate for the baseline (the difference between the total information rate and the GSE rate) is then compared with calculated image data rates for the other systems. The others can have higher or lower rates depending on how much better or how poorly they protect against transmission errors. Equations for evaluating the transmission rates of the coding schemes are solved, using basic algebra, and plotted as a function of the fractional GSE rate for the baseline.



An uncoded channel is the baseline in the figure; it is compared with: Golay compression/uncoded transmission; convolutional coding/Viterbi decoding; convolutional/Viterbi/Golay transmission; and advanced imaging communication system (AICS), which uses a combination of several compression, coding, and decoding algorithms. Alternatively, any one of these systems could be the baseline, and the others can be compared with it.

Note

This work was done by Robert F. Rice of Caltech for NASA's Jet Propulsion Laboratory.

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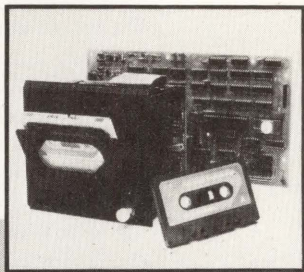

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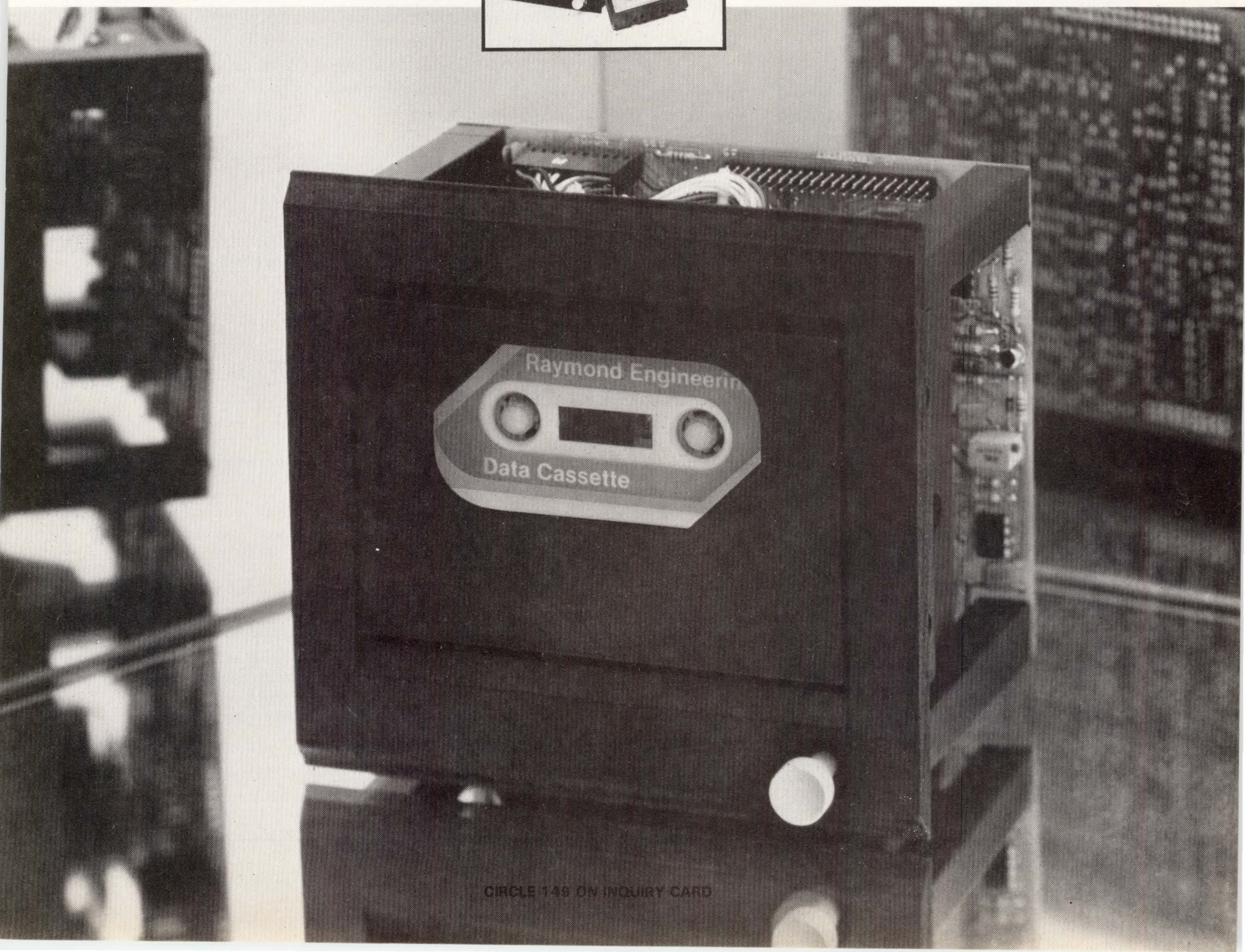

CIRCLE 149 ON INQUIRY CARD

Programming the 8086—Part 3: Procedures and Parameters

Stanley Mazor

Intel Corporation
1350 Bordeaux Dr, Sunnyvale, CA 94086

Features incorporated in the 8086's symbolic assembly language include register oriented instructions and various addressing modes, which were dealt with in the two previous issues. This discussion of parameter passing between PL/M and symbolic assembly language subroutines concludes the series.

Architecture of the 8086 incorporates substantial improvements over the 8080 for passing parameters to subroutines as required by modern high level languages. Subroutines—*procedures* in 8086 terminology—can reduce the amount of program memory needed for repetitive software functions such as mathematical expression evaluation, table lookup, and input/output formatting. Whether written by programmers or provided in a standard subroutine library, procedures greatly extend the functional capabilities of any programming language.

Procedures can be written in a high level language, such as PL/M or Pascal, or, for maximum performance, in assembly language. Assembly language procedures can be called within PL/M language programs; however, mixing two languages requires a standard protocol for passing shared data. Data sent to a procedure are called *arguments* or parameters to distinguish them from results returned by the procedure. Protocols for passing arguments and returning results reflect both underlying hardware characteristics and overriding PL/M-86 constraints.

Passing Arguments to Procedures

Traditionally, arguments are passed to procedures by placing them in specific memory locations or on the stack before calling the procedure. PL/M-86 programs pass all arguments to subroutines on the stack. Any procedure written for use with a PL/M-86 program must be able to find its arguments on the stack, remove them from the stack, and leave results (if any) in the accumulator. A PL/M program statement to call a square root subroutine with the number 4 as an argument might be coded as X = SQRT(4). Here, parameter "4" is pushed onto the stack before the square root subroutine is called. Equivalent assembly language code generated by the PL/M-86 compiler for this statement might be

```
(1)     PUSH     FOUR      ; stack argument
(2)     CALL     SQRT      ; invoke procedure
(3)     MOV      X, AX     ; assign result
```

The SQRT procedure, invoked in step (2), expects to find its argument value on the stack, and leaves its result in the accumulator.

Procedures written in any 8086 compiler language obey this protocol. However, assembly language programmers must follow the rules explicitly. Steps (1) and (2) use the stack and the stack pointer (SP) register. The PUSH instruction first decrements the SP register to point to the next free word in the stack memory area, and then copies the specified memory data word into the new top of stack (TOS) position in memory. The SP always points to the current TOS (Fig 1). Since each memory word occupies two bytes and the SP contains a byte address, it is actually decremented by two. *(continued on page 150)*

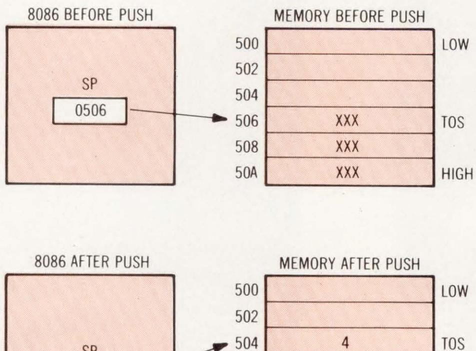

Fig 1 8086 stack manipulation. PUSH instruction enters data onto stack by first subtracting two from SP value, then writing data at new TOS addressed by SP. PUSH instruction operates on registers or memory words

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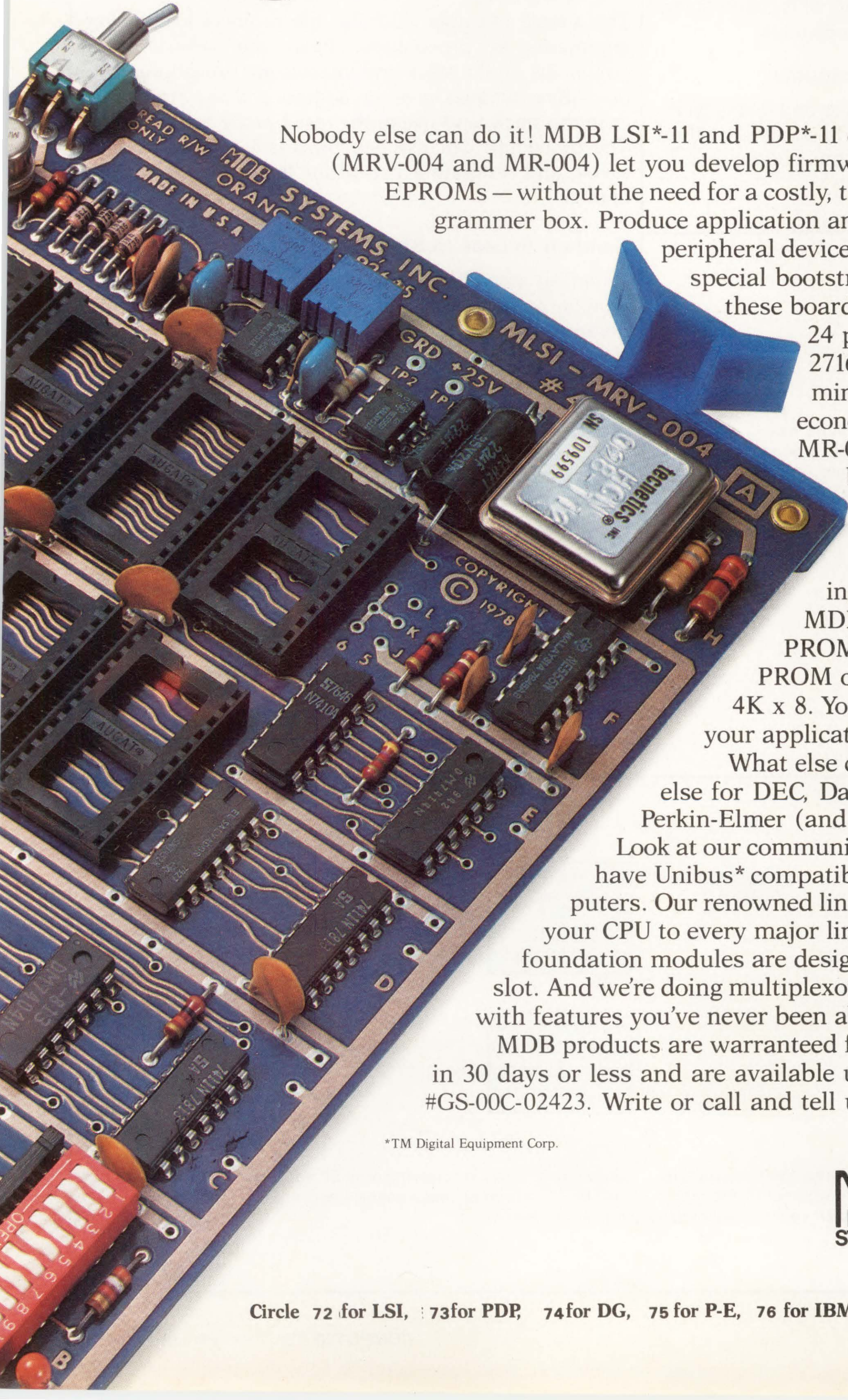

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The processor's CALL instruction uses the stack to save the return address—the point in the calling program at which execution will resume after completion of the procedure. CALL instructions automatically push the address of the next sequential instruction onto the stack and then jump to the designated procedure, as shown in Fig 2. Here, the address of the instruction following the CALL, location 0326, is saved on the stack as part of the mechanism for calling procedure SQRT. Assembly language programmers must observe this stack status when writing compiler compatible procedures.

Accessing Arguments within Procedures

The square root procedure must access and delete its incoming argument and its return address. One method would be to POP both values into registers by means of

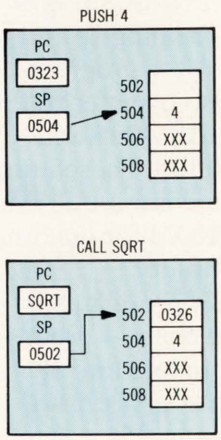


Fig 2 Procedure calling. Before invoking SQRT procedure, caller must PUSH its argument onto stack. Then, CALL instruction pushes address of next sequential instruction onto stack as return address and branches to SQRT procedure

```
SQRT:   POP BX          ; pop return address
        POP AX          ; pop argument
                        ; perform calculation
          •
          •
          •
        MOV AX, RSLT    ; load result
        JMP BX          ; return to caller
```

This simple example illustrates the protocol for passing arguments to procedures. First, the caller places arguments on the stack and invokes the procedure. The procedure removes its return address and any arguments from the stack, and places the result in the accumulator. The procedure can use any processor register without saving and restoring it except for the base pointer (BP) register.

Random Access to Stack Data

When an assembly language procedure requires many arguments, it may be more convenient to keep these parameters on the stack and access them as needed instead of transferring them all into memory. The BP register is designed for this purpose and serves as a base register for the stack segment. In contrast, all other base registers automatically reference the data segment.

The stack segment shown in Fig 3(a) contains eight arguments designated P1, P2, ..., P8, all pushed onto the stack by a caller. Since this procedure will use the BP register to access its arguments, it must first save the BP content on the stack as shown in Fig 3(b). Copying the SP into the BP establishes the proper base pointer value. Now, every parameter on the stack can be accessed by designating an appropriate offset from the base address in the BP [Fig 3(c)]. For example, argument P3 can be accessed as the 14th byte beyond the BP value, using

```
ADD  CX, [BP] + 14
```

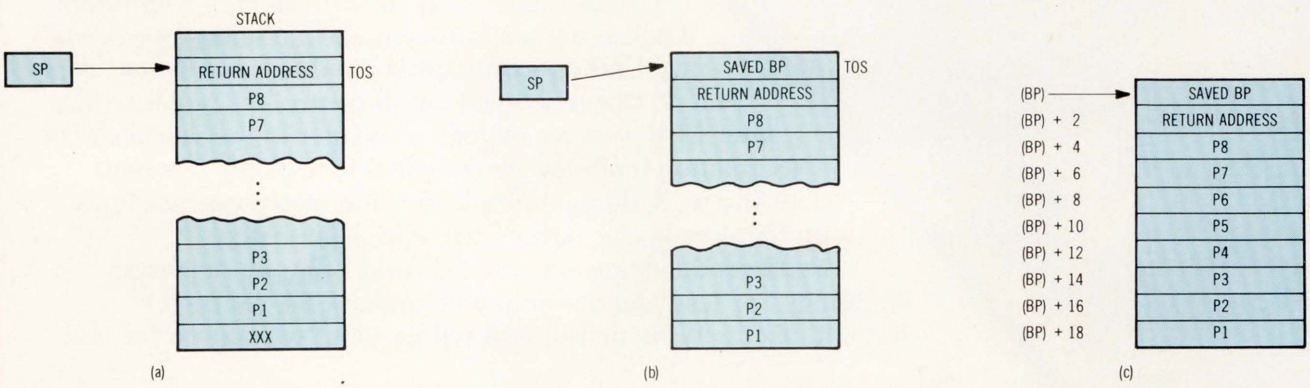


Fig 3 Accessing arguments within procedures. When procedure is invoked, stack segment (a) contains eight arguments and return address at TOS. In (b), procedure first saves BP value by pushing it onto stack. Then, by copying new SP value into BP, procedure can use BP offsets to access variables as shown in (c) without removing them from stack

Because the actual displacement (14) occupies only one byte of program memory, this instruction is relatively economical. With a 1-byte offset, about 60 parameters can be allocated on the stack and accessed in random sequence using the BP displacement method. Additional parameters would require a less economical 2-byte offset.

The 8086 assembler provides a natural extension to the equate (EQU) declarative. Using the equate statement, equivalent names can be declared for stack variables. For example, after declaring

```
P1    EQU    [BP]  +  18
P2    EQU    [BP]  +  16
       •
       •
       •
P8    EQU    [BP]  +   4
```

P1, P2, ..., P8 can be used as symbolic variable names. Then, the typical program statement

```
ADD  CX, [BP] + 4
```

would appear in the more mnemonic form, ADD CX, P8.

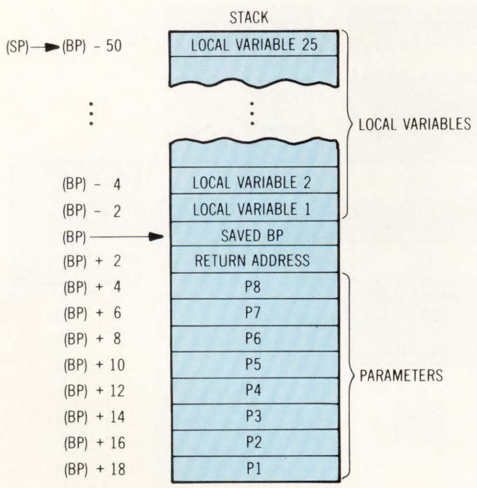


Fig 4 Local variable storage. Starting with initial stack configuration shown in Fig 3(c), procedure allocates storage for 25 local variables by adding 50 to SP. Then, local variables can be accessed by designating negative displacement to BP, and arguments can be accessed by designating positive displacement to BP

Local Variables

Procedures that need temporary memory to store intermediate results can allocate space within the stack by operating directly on the SP. For example, the instruction SUB SP, 50 moves the stack pointer downward and allocates 50 bytes of storage within the stack for use by the procedure. This storage is accessed by supplying a negative offset relative to the BP. Again, a 1-byte offset within the instruction will access any of these temporary storage locations, called local variables. As shown in Fig 4, local variable access involves a negative BP displacement or offset, and argument access involves a positive BP displacement. Allocating all variables in the stack when the procedure is entered helps in programming interruptible and reentrant routines.

PL/M Protocol

To achieve PL/M compatibility, an assembly language procedure must also restore the old value into the BP register and remove all local variables and arguments from the stack. BP addresses the stack location containing its original value; therefore, only a MOV and POP instruction are required to restore the BP and the SP.

```
PROCX:   PUSH   BP       ; save base pointer
         MOV    BP, SP   ; mark stack base
         SUB    SP, 50   ; allocate local variables
          •
          •
          •
EXIT:    MOV    SP, BP   ; reset SP
         POP    BP       ; restore original BP
         RET    N        ; delete N parameter bytes
```

A novel combination, the return and add immediate instruction, is used to delete the stack data. This instruction fetches the return address from the TOS and advances the SP by N bytes to remove procedure parameters from the stack.

Summary

Assembly language programmers who follow the compiler's protocol for passing parameters to procedures can easily combine compiler statements and assembly language subroutines. Programs can access subroutine arguments directly from the stack, by using the BP register. Temporary storage space within the stack can be allocated and deleted using simple operations on the stack pointer register. Storage of arguments and local variables on the stack makes it possible to implement reentrant or recursive procedures under modern high level languages.

Microprocessor Development System Expanded to Support Eight Users

Development capability for up to eight simultaneous users is provided by the EXORmacs multi-user microprocessor development system. Added to the basic EXORmacs system (see *Computer Design*, Apr 1980, pp 171-173), which supports both 16- and anticipated 32-bit microprocessor designs, hardware components include hard discs, a universal disc controller, and a multichannel communications module.

Basic hardware components of the system, available from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, include EXORmacs 15-slot chassis, MC68000 MPU/MMU module, DEbug module, two 128k-byte dynamic RAMs, and universal disc controller.

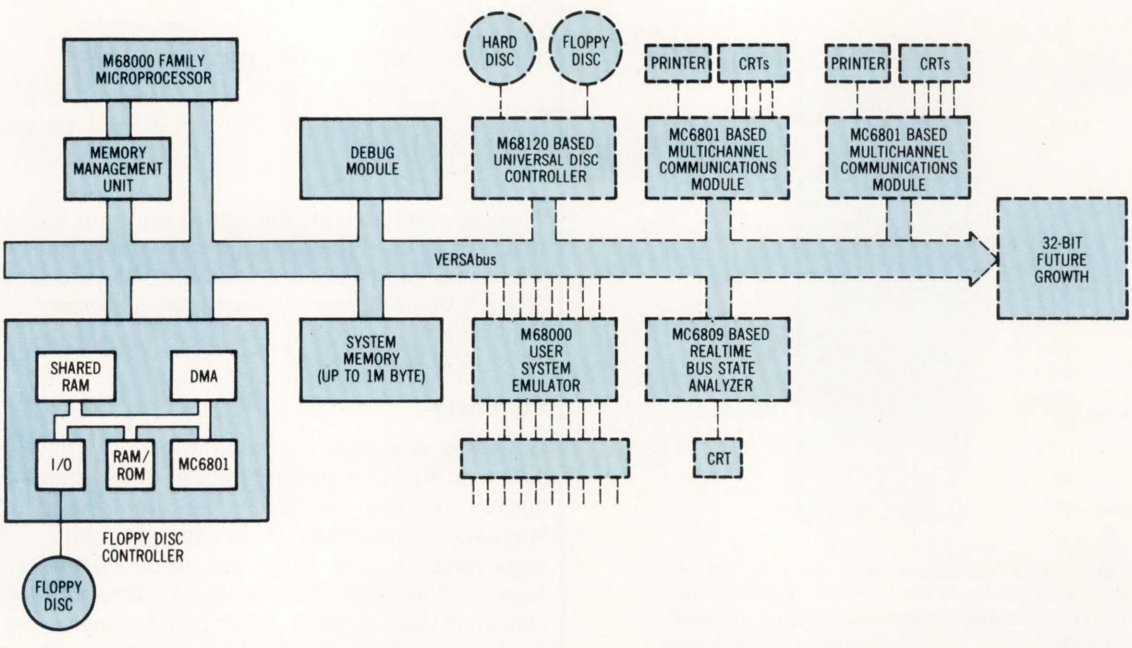
Software includes the VERSAdos multitasking operating system, CRT editor, structured assembler, linkage editor, PASCAL compiler, and symbolic DEbug.

Providing 32M-bytes capacity for centralized mass storage, the hard disc drive combines fixed and removable storage. An optional 96M-byte drive unit is also available; two units may be connected to provide a total hard disc storage capacity of 192M bytes with a transfer rate of 1.25M bytes/s. An MC68120 microcomputer intelligent peripheral controller handles requests from the system, and provides self-contained module diagnostics. This multiprocessing technique offers increased system performance, resulting in efficient utilization of multiple users' time.

A multichannel communications module (MCCM) provides I/O interface among multiple users through four serial RS-232 ports and a printer port shared by the four users. Individual baud rate generators within the communications module allow each user to program his terminal. Each module supports four EXORterm 155 display consoles that provide editing and debugging capabilities for EXORmacs. Additional MCCMs and memories meet the expanded requirements of multi-user development.

600 lines/min can be printed by the optional high speed line printer. Features include a 96-char set with 132-column, upper- and lowercase capability, and built-in diagnostics.

Circle 401 on Inquiry Card



Microprocessor development system. Motorola's basic EXORmacs (within solid lines) expands to provide increased performance and development capability for up to eight simultaneous users. (Dotted areas show multi-user and support expansion system.)

Process Control Computer Integrates Digital/Analog I/O on Single Board

Based on the iAPX 88/10 processor, the iSBC 88/40 measurement and control computer from Intel Corp, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123, provides a high level of digital and analog integration on a single board. The board, designed for industrial and laboratory applications such as realtime process control, production monitoring, supervisory control, and data acquisition, can update process loops up to three times faster than boards using other 8-bit processors.

The speed and power of the iAPX 88/10 (formerly Intel 8088) processor supply the ability to concurrently process and update 16 control loops in 200 ms, using a traditional proportional integral derivative control algorithm. It also provides 8-bit data bus capability, 1M-byte address, 16-bit internal registers, and hardware multiply/divide, and uses about 20% less code when programs are written in high level languages.

Memory capability includes 4k bytes of RAM, expandable to 8k bytes, and including 1k byte of dual-port RAM. Four 28-pin sockets, expandable onboard to 8 sockets, allow up to 32k bytes of EPROM, expandable to 64k bytes. These sockets also support the company's 2816 E^2PROMs, allowing onboard programming of up to 4k bytes of data. An onboard dc-dc converter allows modification of memory for changing data or programs that must be kept in nonvolatile memory.

A programmable, 20-kHz analog input subsystem provides 32 single-ended or 16 differential inputs, and features 12-bit resolution. Programmable gains of 1, 5, 50, and 250, and a programmable offset for high accuracy readings (within 0.05%), are provided. Twenty-four programmable parallel I/O lines read setpoints or output digital signals to peripherals.

To expand system capabilities while retaining the single-board form factor, up to three iSBX Multimodule boards can be added. These include concurrently announced multichannel analog I/O units. iSBX 311 analog input and iSBX 328 analog output Multimodule boards can be added to the computer by the iSBX expansion bus protocol and connectors. As many as three units can be used on a single board. The input module provides eight differential or 16 single-ended inputs. Signal inputs can range from 20 mV to 5 V; inputs can be either 0 to 5 V unipolar, or −5 to 5 V bipolar with jumper selection. Analog/digital conversion resolution is 12 bits; accuracy can be adjusted to 11 bits at 0 to 60 °C. The 50-ns ADC and simple programming interface allow up to 17,000 12-bit samples/s to be stored in system memory. Inputs can be conditioned with noise filters, resistor dividers, or current loop to voltage conversion resistors.

Eight output channels per unit are provided by the analog output unit. The user can independently jumper any output channel for 0 to 5-V unipolar voltage output, −5 to 5-V bipolar voltage output, or 4 to 20-mA current loop output. The output unit also provides 12-bit conversion resolution and 11-bit accuracy.

Users can screw-terminate field wiring to the iCS 910 signal conditioning and termination panel, and connect the outputs to the panel with flat ribbon cable. For closed loop control applications, the input and output units can be combined on the measurement and control computer for a high performance, high point count, and larger numbers of control loops. A typical 16-loop mix of 24 analog inputs and 16 analog outputs can be controlled by the computer using three multimode boards.

Three programmable 16-bit counter timers are featured by the board, which can function as a standalone system, a multimaster among other computers, or an intelligent slave analog preprocessor in a larger Multibus supervisory control system. Hardware support will include iSBC multimode memory expansion and numeric data processor boards, memory, I/O, and controller boards, signal conditioning boards, and an iCS industrial control systems chassis.

Circle 402 on Inquiry Card

Standalone Microcomputers Are Fully Expandable Into Network Systems

MCZ 2/19 and -2/49 are high power, floppy disc, standalone microcomputer systems. The 2/19 is a modular desktop system based on the 4-MHz Z80 MPU, featuring 64k bytes of RAM, 2.4M bytes of floppy disc storage, and a power supply that can support up to four boards. The -2/49 includes all the features of the -2/19, adding a fully functional 1920-char CRT terminal, RIO Version 3 operating system, and either COBOL runtime interpreter or BASIC. MCZ 2/49-2 is identical to the -2/49-1 except for a functionally increased, 1920-char CRT terminal. These basic systems, available from Zilog, 10340 Bubb Rd, Cupertino, CA 95014, are fully upgradable with extensive expansion options.

Operating systems, high level languages, relocating assembler and linker, and learning aids facilitate program development. RIO Version 3 operating system support software includes printer drivers, a sort merge package, and a text editor. Optional RIO/CP multitasking/concurrent processing operating system provides increased processor efficiency and usability. A relocating assembler and linker provides macro processing, as well as generation and linking of relocatable and absolute object code modules. The linker automatically produces ready to run files. A symbolic debugger provides assembly level debugging. Learning aids such as HELP and ERROR functions are provided.

Expansion capabilities available for these systems include 2.4M bytes of additional floppy disc storage using sectored, industry compatible format, and double-sided, double-density drives. The intelligent floppy disc system has a dedicated microprocessor and buffer memory. Random access file structure provides fast record retrieval and updating. A 4-line, programmable serial interface allows the implementation of ASYNC and the IBM 2780/3780 workstation facility. Optional serial and I/O capabilities include four additional RS-232-C ports that can support any serial drive. A field upgrade kit allows attachment to the Z-NET local computer network, including the RIO/CP operating system, NST 2/01 network station transceiver, network protocol software, and the SDS 2/01 shared data station, for distributed multi-user, multiprocessor, shared file expansion.

String manipulation, 2-dimensional array, subroutine calls, and 13-digit BCD capability are provided by the company's BASIC. The level 1 COBOL runtime interpreter is compatible with ANSI 74 level 1, offers the index sequential address method to simplify record retrieval and updating, and also contains some features of level 2; the ANSI X3.23 1974 level 2 COBOL compiler and/or runtime interpreter is available as an option. COBOL/MT allows one to five terminals concurrent access to the same COBOL application program. The company's PLZ family of application and systems programming languages is also available.

Circle 403 on Inquiry Card

Storage System Combines Winchester and Floppy Discs

8.9M bytes of fixed 8″ (20-cm) Winchester storage and 1M byte of double-sided floppy disc storage for DEC's LSI-11 are provided by the FWTO1172 "Flinchester" system. The double-sided floppy disc used in the unit, developed by Scientific Micro Systems, Inc, 777 E Middlefield Rd, Mountain View, CA 94043, provides over 40% faster average access time and eight times the system throughput of DEC's single-head RX02 floppy disc drives. The system includes disc drives, controller, interface, power, and cabling in a 5.25″ (13.33-cm) rack or tabletop enclosure. A PDP-11 version is also available.

Compatible with standard DEC operating systems RT-11 and RSX-11M, as well as PDP-11, the system recognizes standard DEC RX01, RX02, and IBM 2/2D formats for data I/O. Average access to 8.9M bytes of storage is 70 ms with data transfer rates greater than 500 bytes/s. Floppy discs require less than 60 s to transfer 1.2M bytes of data to or from the Winchester disc.

A proprietary controller interfaces the LSI-11 Q-bus and up to two floppy and two 8″ (20-cm) Winchester discs, using compatible and extended modes of operation. Compatible mode provides complete DEC RX02 hardware, software, and media compatibility. Extended mode increases system throughput with high performance DMA interface operations. Data blocks of up to 65k bytes can be transferred, without interruption, in a single command; the controller automatically steps to successive tracks or cylinders. Each device is independently addressed by the same SMS RT-11 or RSX-11M handler.

Test and diagnostic support features include a resident controller self-test that automatically performs basic CPU, memory, controller, and drive tests after each power-up or bootstrap operation. Additional tests can be executed via software slected maintenance commands or onboard switches. An installation and test diskette automatically boots a standalone program which provides a terminal to operator interface. A menu driven display with operator selection allows testing, drive alignment, copying, formatting, scanning, and Winchester backup and load functions. LEDs indicate basic system malfunction via an error code display.

Circle 404 on Inquiry Card

Peripheral Boards Offer Improved Capabilities, Compact Packaging

Four computer peripheral boards, including a combination analog and digital interface, a video interface, a RAM/EPROM memory board, and an I/O CMOS memory board, make it easier for OEMs and technical end users to design microcomputers into their applications. From Data General, Rte 9, Westboro, MA 01581, the boards are compatible with the company's microNOVA board computer line as well as the MP/100 and MP/200 microcomputers.

Model 4335-S, the analog and digital I/O interface board, is designed for data acquisition and process control applications. OEM instruments can be combined with this board and either the MBC/2 or MBC/3 in a 2-board, intelligent system that has the capabilities of a full NOVA computer with an MP/OS operating system using FORTRAN or Pascal. The digital I/O section, user programmed I/O control, has 16 input and output lines with handshaking signals. The analog input port provides four single-ended channels, and four onboard test channels that measure analog signals to a 10-bit resolution. One channel of analog output is also provided.

Giving direct control over formatting information, model 4337-S video interface generates alphanumerics on a video monitor, and is an interface to an ASCII keyboard. Features include upper- and lowercase characters, 5 x 7 dot matrix, and a 7 x 10 character block. Two versions of the RAM/EPROM memory board, models 8688 and 8689, are available, providing 8k bytes of RAM and 32k bytes of EPROM, and 32k bytes of RAM and 32k bytes of EPROM, respectively.

Rechargeable batteries mounted on the I/O CMOS memory board supply power to the storage array for up to 30 days after power is turned off. The board contains up to 16k of nonvolatile memory that is accessed either by the data channel, for page transfers, or programmed I/O, for single-word transfers. Applications include collecting data at remote sites, changing data in table driven applications, and use in keyed security systems.

Circle 405 on Inquiry Card

STD-BUS Compatible 8-Channel, 8-Bit DAC Operates at 4 MHz

A high speed, 8-channel, 8-bit digital to analog converter, the ST4305, is designed for microprocessor based data conversion applications, and will operate with any processor in STD- or PC44-BUS environments. The converter measures 4.5 x 6.5″ (11.4 x 16.5 cm), and offers 2.3-μs settling time and $\pm 0.1\%$ FSR relative accuracy. Available from Applied Micro Technology, PO Box 3042, Tucson, AZ 85702, the converter operates at any speed up to and including 4 MHz. Operating temperature range is 0 to 55 °C.

All eight channels are latched, and the card is configurable for either a current or voltage mode. In the current mode, current source may be provided either onboard or offboard. In the voltage mode, output range is 0 to 10 V unipolar, or −5 to 5 V bipolar. Each channel is independently configurable. Each output channel has an operational amplifier for buffering, and a transistor for current mode operations; both amplifier and transistor can be removed when not required by the application. The converter is also available in a 4-channel version.

Other features include onboard switches that allow the user to select I/O addresses between 00_H and FF_H. Selectable power source voltages can be provided either by the microsystem or an external supply. Voltage requirements are 12 V at 110 mA, −12 V at 130 mA, and 5 V at 90 mA.

Circle 406 on Inquiry Card

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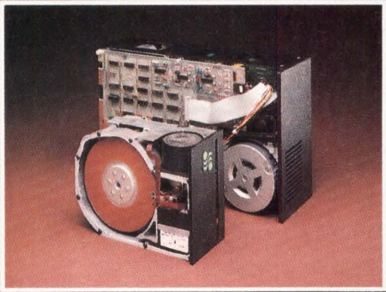
A better choice than eight-inch Winchester.

Our drive is smaller, more cost-effective and easier to back up. Some eight-inch Winchester drives require AC power. This complicates system integration and produces extra heat that can mean additional cooling. We use only 22 watts.



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20% more capacity for less money.

Try our micro-Winchester with your floppy-based system.

Our drive has the same track capacity as your double density 8-inch floppy. This means minimal software conversion. You'll find it easier to trade up users, because they can use the same data base.

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Like the minifloppy, the micro-Winchester has dimensions of 5¾" by 3¼" by 8." It uses the same voltages (+12 and +5) and requires no AC power. Give your customers almost 15 times the capacity of a double-sided minifloppy at less than three times the cost.

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CIRCLE 80 ON INQUIRY CARD

MICRO DATA STACK

2-MHz Dynamic RAMs Available for 6800 and 6809 Microprocessors

16k, 32k, 48k, or 64k bytes of dynamic RAM are available in the MM-6800D memory module for Motorola's 6800 and 6809 microprocessors. Designed for 2-MHz operation, the module is compatible with Motorola's EXORciser I and II, and Rockwell's System 65, and is available from Micro Memory Inc, 9434 Irondale Ave, Chatsworth, CA 91311. Features include even parity with jumper-selectable output to NMI, parity error, or the dynamic system bus (DSB); switch-selectable hidden refresh or cycle stealing; and write protect control in 8k increments up to 64k. Series II DSB provides page enable, parity error, and extended memory management.

Cycle time is 450 ns; access time is 220 ns from memory clock. 16-bit random access addressing and 8-bit bidirectional data in/out with 3-state output are provided. Connectors are dual 43-pin on 0.156" (0.396-cm) centers. The module measures 5.75 x 9.75" (14.60 x 24.76 cm), requires 5 V ±5% and 12 V ±5%, and has an operating temperature range of 0 to 60 °C.

Circle 407 on Inquiry Card

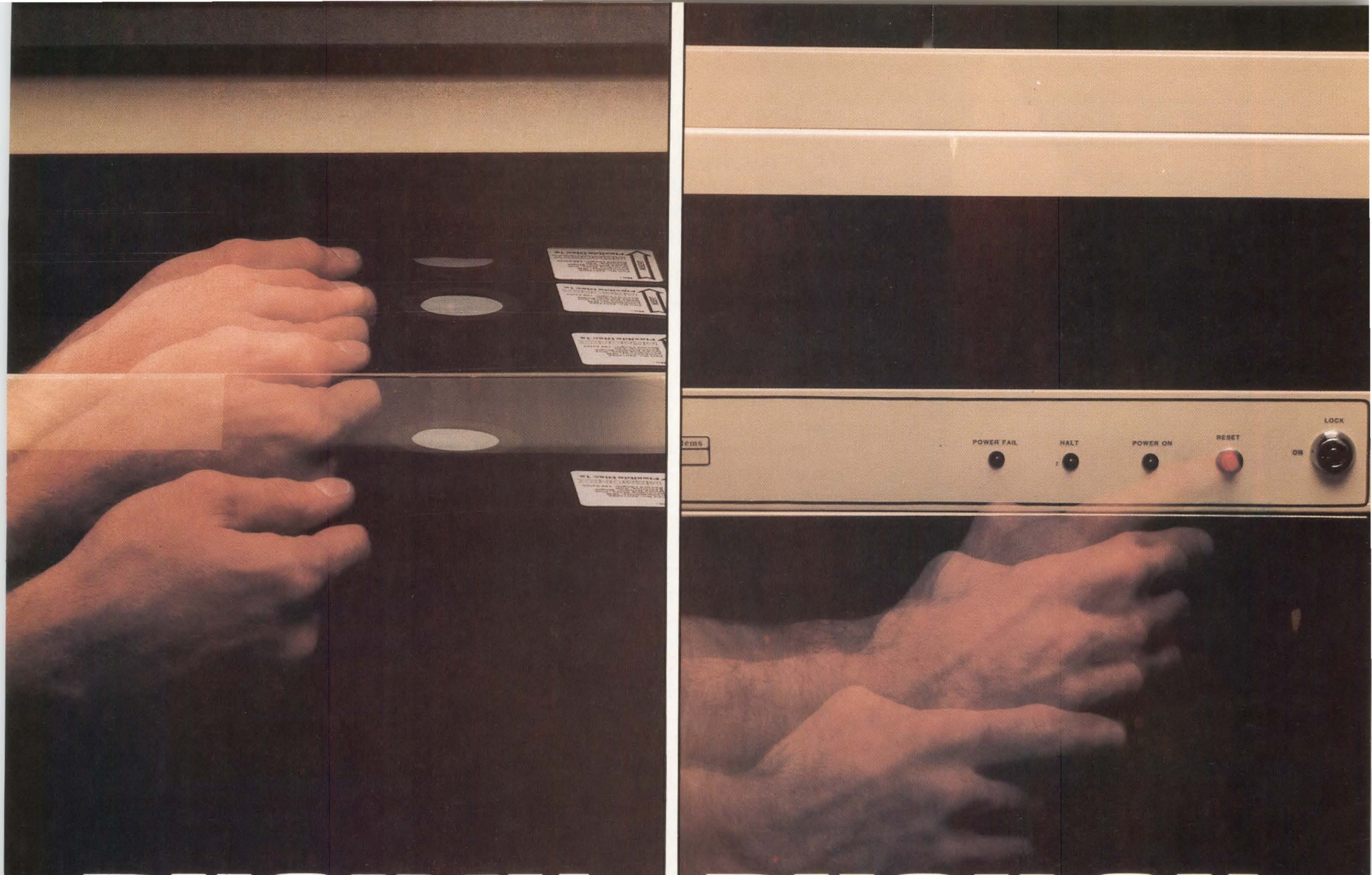
16-bit CPU Board Is Compatible with S-100 Proposed Bus Standard

C-86, a 16-bit central processor board that uses the 8086 microprocessor, is compatible with the proposed IEEE-696 S-100 bus standard. Used for single- and multiprocessor applications, the board features an onboard local bus that contains 2k x 16 bits of P/ROM, an RS-232-C serial I/O port, a software programmable timer, and an expansion connector. Available from Piiceon, Inc, 2350 Bering Dr, San Jose, CA 95131, the board operates at 5 MHz in standard configuration, and at 8 MHz in an optional C-86-A version.

Several features of the proposed bus standard are incorporated in the board. Up to 16 bus masters (1 permanent and 15 temporary) can operate on a single bus, passing control from one to another. When multiple requests are made, the bus is controlled by the master that the system designer has determined to have the highest priority. When the bus transaction is completed, the master with the next highest priority controls the bus; if no temporary master has priority, control returns to the permanent master. The board can be jumpered to serve as either a permanent or a temporary master, and a precise timing scheme allows error free transition from one bus master to another. Up to 1M bytes of switch-selectable memory can be directly addressed with the standard's 16M-byte address space. Increased processor throughput is achieved by use of 16-bit data paths.

Full compatibility with the company's SUPERMEM ECC error checking and correcting dynamic RAM board and V-100 video controller board, and other bus compatible products, is provided. High level languages and operating systems software are available.

Circle 408 on Inquiry Card



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The systems are available with CP/M or MP/M operating systems. For real-time or multiuser applications, the CCS OASIS real-time multitasking operating system supports re-entrant programs and relocatable code modules, with facilities for task-to-task communication, file protection, time-of-day bookkeeping, spooling, task overlay, dynamic memory management, ISAM file structures and device-independent I/O. CCS OASIS includes debug, text editing, linkage, and file sort utilities; the system supports a host of existing languages, applications, and utilities from a range of vendors.

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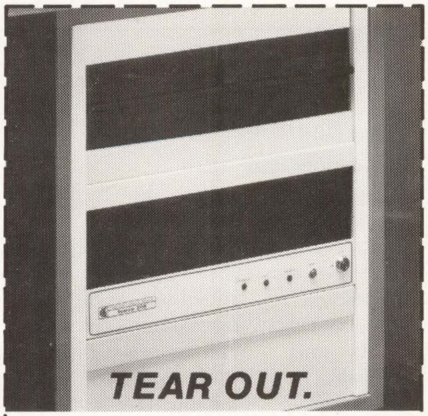

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CIRCLE 82 ON INQUIRY CARD

Plug-In Matrix Printer Provides Hard Copy for Intellec Systems

The MDP-125 printer plugs directly into all Intellec microcomputer development system models, and provides low cost hardcopy output with no special hardware or software. A product of EMC Corp, 385 Elliot St, Newton, MA 02164, the 125-char/s printer is designed for high reliability operation during long duty cycles.

Features include bidirectional operation for maximized throughput, front or bottom loading forms tractor feed mechanism, long life Mobius loop ribbon cartridge, self-testing firmware, and sound deadening. The 125-char/s, 9 x 9-dot matrix printer produces the 96-char ASCII character set with upper- and lowercase characters plus underlining on an original and five copies. An automatic on/off control allows activation directly from the Intellec console.

Circle 409 on Inquiry Card

Desktop Microcomputer Available for Single- and Multi-User Systems

Micro 210, a desktop microcomputer from Data Terminals and Communications, 590 Division St, Campbell, CA 95088, functions as a single- or multi-user system. Using an 8085A-2 microprocessor, the system features 64k bytes of RAM, 2k bytes of phantom ROM, and four RS-232 asynchronous interface ports. Two BASF 5.25″ (13.33-cm), single-sided, 40-track, floppy disc drives provide up to 300k bytes of online storage. DMA method allows an average random access time of 270 ms to be achieved. Expansion boxes allow the addition of up to four mini-floppy or two 6M-byte Winchester disc drives.

Up to four operators can simultaneously access the system, using asynchronous data terminals, interfaced via EIA RS-232 connectors on the rear panel. A fifth data port option uses DB-25-2 type connectors. Each of the four ports is compatible with Bell 103/113 and 212, and provides software programmable baud rates from 110 to 9600, variable duplex and parity modes, and terminal/modem selectors.

Optional software packages for use in conjunction with single- and multi-user operating systems include extended BASIC interpreter, BASIC sort, 8085 assembler, and word processing. Word processing includes text editor, letter writer, names file maintenance program, and document processor. Other optional system software packages are MK II, IV, and X, and MUBBS, and CP/M. The system is loaded from disc into RAM upon power-up or reset.

Hardware options include a controller required for Winchester disc drives, and drive expansion boxes containing the power supply unit required for additional floppy and/or fixed disc drives. All additional drives must be housed in these boxes. The operating temperature range is −40 to 10 °C, and power requirements are 115 V at ±10%, 60 Hz, with 230 V ±10%, 50 Hz optional. The system measures 14.6 x 12.5 x 6.5″ (36.4 x 31.3 x 14.2 cm), and weighs 19.7 lb (9.0 kg).

Circle 410 on Inquiry Card

Tape Controller/Formatter Is Compatible with TU10/TM11 Subsystems

Complete compatibility with DEC TU10/TM11 tape subsystems is provided by the 1521, a fully embedded, dual-density, tape controller/formatter for the LSI-11, -11/2, and -11/23 microcomputers. Available from Datum Inc, 1363 S State College Blvd, Anaheim, CA 92806, the unit can control up to four drives with maximum cable length of 50 ft (1500 cm).

The controller/formatter plugs into a standard Q-bus backplane or system unit, and executes all existing DEC PDP-11 system and diagnostic software for the tape subsystem. It can be used with any industry standard reel to reel magnetic tape transport operating at speeds up to 75 in (190 cm)/s.

Recording, in either NRZ format at 200 to 800 bits/in (79 to 315/cm) or PE format at 1600 bits/in (630/cm), is switch-selectable. Data packing options are provided for either DEC or IBM format. Timing is generated by a crystal clock, and all specifications are met over a wide voltage and clock range. Conservative derating is made on all components, and environmental ranges exceed those of all commercial LSI-11 host computers and applicable industry magnetic tape transports. The system makes full 16-bit word NPR data transfers and checks for parity errors on all memory read operations.

Circle 411 on Inquiry Card

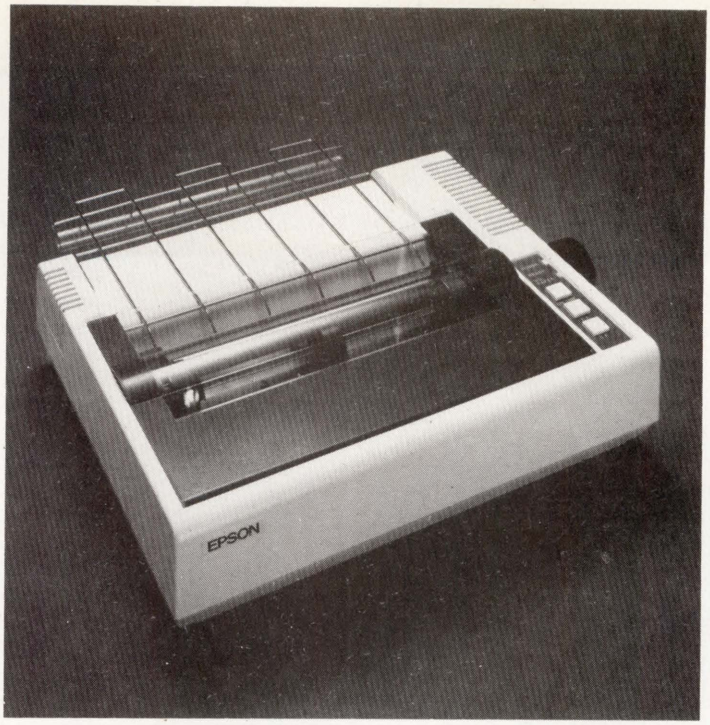
STD-BUS Based Development System for Control Applications

A microprocessor development system for use in applying the STD-BUS to control system and other OEM applications, the Link allows a choice between 6809 or 6800 CPU cards and TSC's FLEX or Microware's OS-9 operating systems. A product of Matrix Corp, 1717 Saunders, Raleigh, NC 27603, the system uses a dual-memory map architecture to provide freedom in target system debugging without complex emulation hardware.

Dual 8″ (20-cm) floppy drives with single/dual-density controller, debug logic, 48k bytes of RAM, printer spooler controller, CPU card, and a 16-slot quiet motherboard are included. Hardware features include complete chassis/enclosure assemblies supplied in a mobile rack. A complete video terminal will be available with graphics capabilities and internal provision for a standard card cage to support OEM needs.

Circle 412 on Inquiry Card

The MX-80. It not only does everything, it does everything well.



Epson.

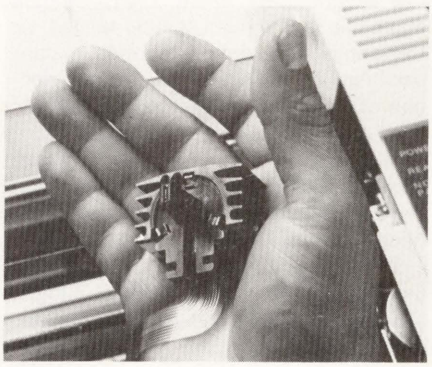
This is the new Epson MX-80 dot matrix printer. It does just about everything you could ask a printer to do. Quickly. Quietly. Reliably. In fact, for OEM installations, the MX-80 may be the single best, all-round printer you can buy. But that's not the best reason to buy it.

The MX-80 prints bidirectionally at 80 CPS in a user-defined choice of 40, 80, 66 or 132 columns. And if that's not fast enough, its logical seeking function minimizes print head travel time. The MX-80 prints 96 ASCII, 64 graphic and eight international characters with a tack-sharp 9x9 matrix. For a long time. Epson printers are known for reliability and the MX-80 is no exception. But that's not the best reason to buy it either.

The print head has a life expectancy of up to 100×10^6 characters, and when it wears out, just throw it away. A new one costs less than $30 and the only tool you need to change it is attached to the end of your arm. The MX-80 is compact, weighs only 12 lbs., and the whole unit, including the two stepper motors controlling carriage and paper feeding functions, is precisely controlled by an internal microprocessor. But even that isn't why you should specify the MX-80.

The best reason is this: because Epson makes more printers than anyone else in the world, we can afford to sell each one for a little less. So you can get one Epson MX-80 Printer for less than $650. And more than one for even less than that.

That's what we call a small price to pay for a printer that does everything well.



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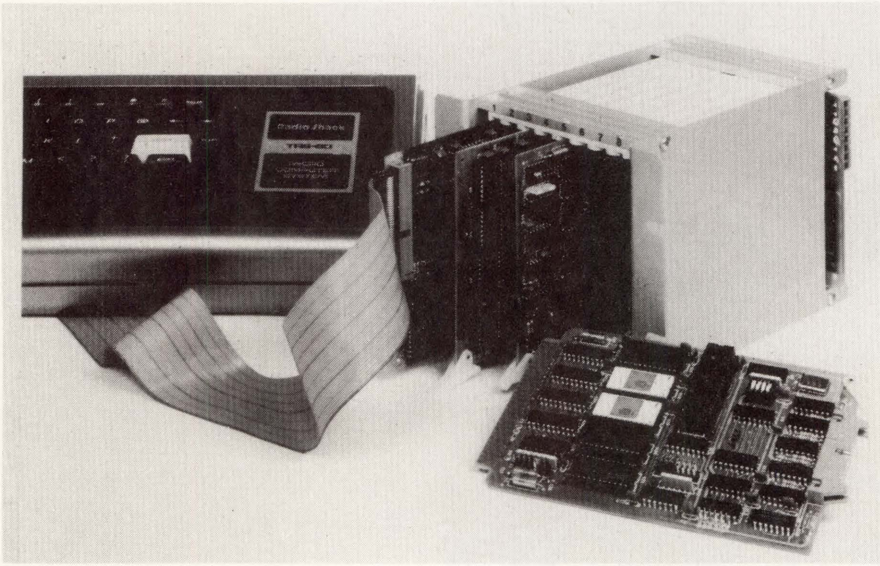
CIRCLE 83 ON INQUIRY CARD

STD BUS I/O Cards Emulate TRS-80 for Software Compatibility



STD-BUS I/O cards. Offered by Xitex, cards emulate keyboard, cassette, and video functions of Radio Shack TRS-80

Keyboard cassette, master video timing, and video cards exactly emulate functions of the Radio Shack TRS-80. The series of STD BUS I/O cards, manufactured by Xitex Corp, 9861 Chartwell Dr, Dallas, TX 75243, used in conjunction with existing Z80 CPU and RAM cards, can run level I, II, and III BASIC in ROM or EPROM, and execute model I-III software.

While retaining functional compatibility with cassette, and video designs, the cards incorporate improvements. These include a cassette interface with built-in AGC, lowercase characters with descenders, external video sync provisions, and multiple-display capability. Complete compatibility with any unit providing parallel ASCII data and strobe is provided by the keyboard interface card, allowing the user to select the keyboard that best suits a particular application.

Circle 413 on Inquiry Card

Printer Interface Makes Apple II Compatible with Centronics Type Printers

Model 7728 printer interface gives Apple II users compatibility with printers using Centronics type parallel interfaces. Included in the interface from California Computer Systems, 250 Caribbean Dr, Sunnyvale, CA 94086, are an 8-bit data output bus, four status inputs, data strobe and acknowledge handshake signals, and a printer reset signal.

An onboard 256-byte ROM provides driver firmware and controls ASCII character output to the printer, such as the Integral Data Paper Tiger, Okidata Microline 80, Microtek MT-80P, MPI-88T, or Centronics. The driver responds to standard Apple II printer commands for selection of command characters, characters/line, auto feed, and video echo. Standard ROMs can be replaced by RAMs, allowing users to develop their own drivers. A ROM/RAM jumper makes the necessary logic changes.

The interface may reside in any Apple II peripheral slot 1 to 7. Arbitration logic, including jumper-selectable IRQ generation, supports the interrupt daisy chain. DMA daisy chain passthrough is also provided.

Circle 414 on Inquiry Card

Low Power NMOS RAM Board Offers Fast Access, Cycle Time

NS23L, a 64k-byte dynamic NMOS RAM board, offers onboard parity generation, parity check circuits, internal or optional external refresh functions, battery backup provisions, and expanded address space operation. A product of National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, the board is compatible with LSI-11, -11/2, and -11/23, and PDP-11/03, and provides fast access and cycle speeds, low power levels, and increased processor throughput capability.

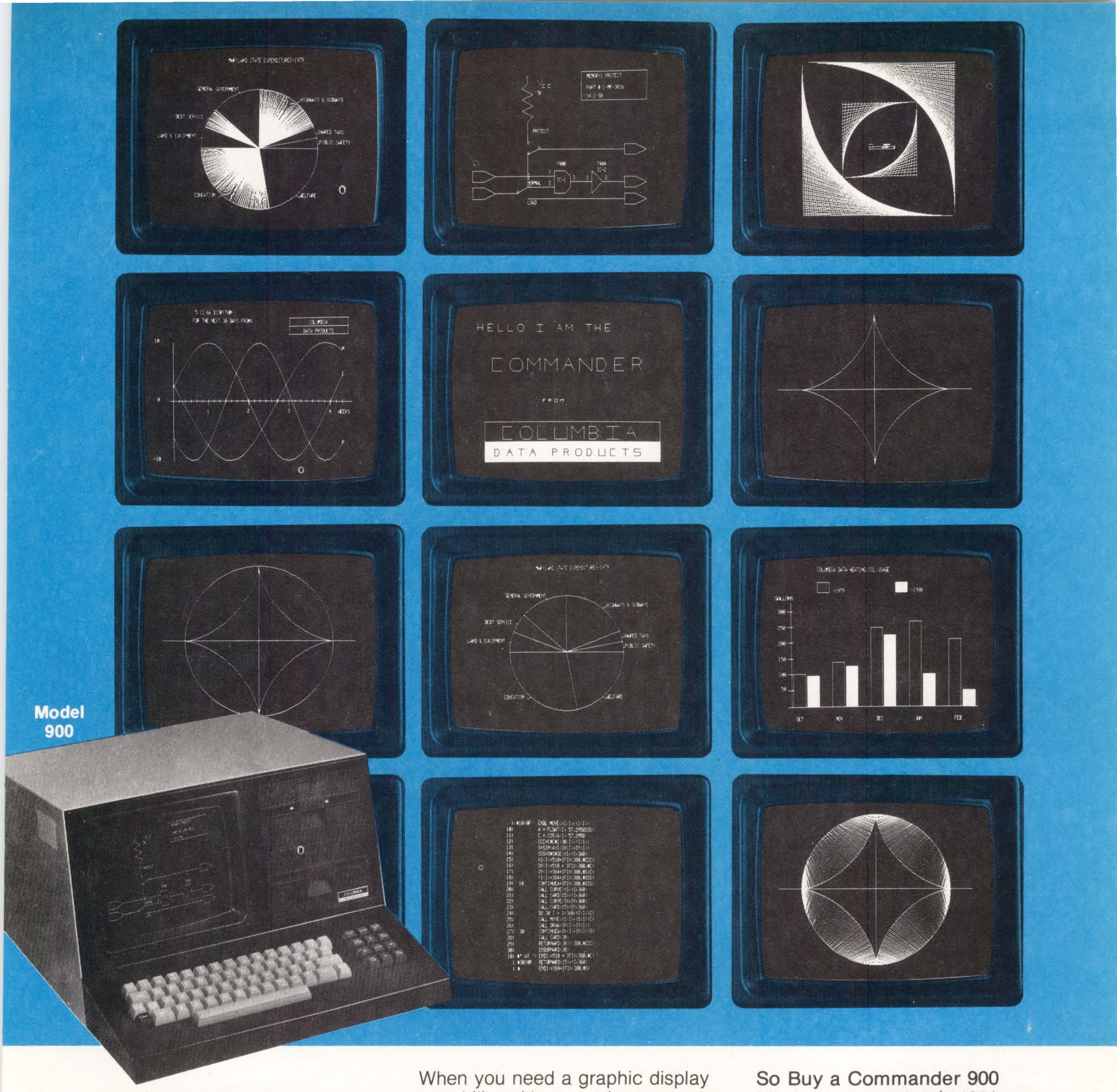
Read, write, and read/modify/write access times are 190 ns, 90 ns, and 700 ns, respectively; read, write, and read/modify/write cycle times are 490 ns, 390 ns, and 1000 ns. Standard configuration is 32k x 18 bits; optional versions are 32k x 16 bits without parity, and depopulated versions are 16k x 18 bits or 16k x 16 bits. Operating power requirements are 1.5 A at 5 V, and 0.4 A at 12 V. Segmented power planes cut standby power requirements to 0.775 A at 5 V, and 0.11 A at 12 V. All ICs are preconditioned, and all RAMs are socketed to aid ease of removal and installation.

I/O Panel Allows Interconnection between Multibus Backplanes

An input/output panel, a Multibus compatible interconnector, allows easy interconnection between Multibus backplanes or between Multibus backplanes and other equipment. The panel, available from Mupac Corp, 646 Summer St, Brockton, MA 02402, is a PC board with an 86-pin connector that mates directly to the edge connector on the backplane. The connector is bused to a 72-pin plug that has grounding between critical signal paths. This plug is connected to a 72-conductor flat cable assembly that can come straight or at right angles off the panel.

In order to interconnect power and ground between equipment, heavy gauge cabling can be plugged into two 6-pin connectors that are mounted and connected to power and ground. 72-conductor flat cable assemblies for interconnection between equipment are supplied in any length, with receptacle(s) at one or both ends.

Circle 415 on Inquiry Card



Our Micro-computer Doesn't Need a Separate Graphics Terminal...

It's Built In

When you need a graphic display capability with your microcomputer . . . don't buy a separate terminal . . . select our Model 900 Commander with the self-contained vector and point plotting features of a sophisticated graphics terminal.

You can display bar charts, pie charts, histograms and complex point to point plots. You can even output displays originally intended for a Tektronix 4010 with our Tektronix® terminal emulator. And because Commander has an independent processor controlling the display, graphics can be handled without interrupting primary computing tasks.

CIRCLE 84 ON INQUIRY CARD

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Computer Systems Division
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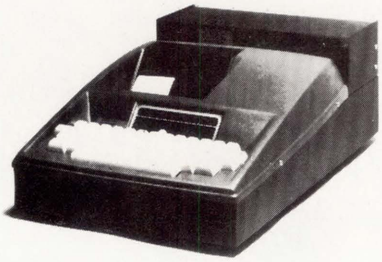
*Dual, independent Z80A Processors, 96K RAM, dual floppy drives, and 512x256 resolution vector graphics on a 9 inch CRT in quantity 100 to qualified OEMs. I/O includes 4 RS-232 ports, 4 parallel ports and RS-170 composite video.

System Preserves Memory Up to One Month After Power Loss



The MMC-65 Maxi-Micro computer is a solid state system for data acquisition, storage, and industrial control; the complete unit, with full-size keyboard, 20-character display, thermal printer, and extensive I/O capability, is housed in a desktop size cabinet. From duTec Inc, 4801 James McDivitt Rd, Jackson, MI 49204, the system preserves memory contents after power loss for at least one month; a power fail monitor permits 1k bytes of program execution before the system ceases operation.

Up to 56k bytes of RAM or ROM, 24k of which may be RAM, can be included. I/O capabilities consist of six serial RS-232/current loop ports, one serial current loop only port, two cassette recorder interfaces, 32 fully programmable I/O lines, and six I/O control lines.

Installed system firmware includes 8k Microsoft BASIC. Other firmware includes an 8k monitor/editor, and a 4k symbolic 2-pass assembler. BASIC callable serial I/O communications firmware, optically coupled industrial I/O control modules, and multichannel analog input hardware are available as options.

Circle 416 on Inquiry Card

Plug-In Processor Board Increases Apple II Power and Versatility

The Mill, a plug-in processor board, installs into any Apple II peripheral slot to provide users with a Motorola 6809E processor that operates concurrently with the unit's existing 6502. The board, designed by Stellation Two, PO Box 2342, Santa Barbara, CA 93120, facilitates realtime data aquisition, stack type languages such as Forth and Pascal; and concurrent programming tasks. Users can run existing 6502 programs or use software developed for the 6800 processor; the assembler will compile 6800 instructions into 6809 object code.

Since the added processor is hardware compatible with the Apple's existing processor, external circuitry is kept to a minimum. In operation, both processors run concurrently and perform internal operations independently. The 6809 acts as bus master during the 6502's bus accesses, commanding 80% of available bus time. However, the 6502 can acquire the bus for time critical I/O operations. Large programs show performance improvements of two to three times, resulting from use of the 6809. These are gained by the processor's direct manipulation of 16-bit quantities through its 16-bit registers.

Features of the board include multiprogramming operations, directly addressable stacks, and position independence of code. An operating system such as the Microware OS9 can be employed to operate the computer in the multiprogramming mode. A more efficient instruction set and 16-bit, rather than 8-bit, addresses and integers allow faster operations of routines such as graphics and large computations.

Circle 417 on Inquiry Card

Floppy Disc System Increases Storage And Flexibility

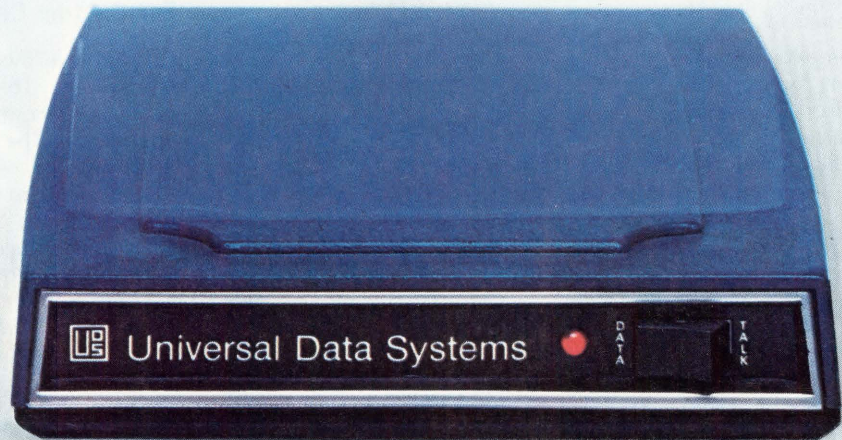
Storage capacity of 2M bytes is provided by the Z-47, an 8" (20-cm), dual-sided, dual-density, floppy disc system designed for use with the Z-89 microcomputer system. Available from Zenith Data Systems, 1000 Milwaukee Ave, Glenview, IL 60025, the system allows both operating system and program discs to be run simultaneously, providing more efficient data access and greater flexibility for a variety of applications.

Up to 2.5M bytes of data and program storage are provided by the system when used with the microcomputer's built-in 5.25" (13.33-cm) disc drive, increasing data capacity up to 24 times. Data can be easily transferred between 8" (20-cm) and built-in 5.25" (13.33-cm) discs at any time. Average data access time is cut from 348 ms to 191 ms.

A special interface board and 40-conductor flat cable attach the disc drive to the Z-89(FA) models. Z-89-48 and Z-89(CA) models must first be fitted with the Z-89-6 and Z-89-7 upgrade kits. Software capabilities, including CP/M and HDOS operating systems and the company's program software, are designed for the 8" (20-cm) disc format in addition to the 5.25" (13.33-cm) built-in system.

Circle 418 on Inquiry Card

Ask About
Our Newest LP Modem...
The ANSWER is AUTOMATIC



The UDS 103LP has ☐ Automatic answering capability ☐ Switch-selectable originate/answer ☐ FCC direct-connect certification ☐ Phone-fitting form factor ☐ No need for AC power

Another innovation in line-powered modems — the 103J-LP auto-answer — is now available from UDS. A TALK/DATA switch allows you to use your desk phone for data communications or ordinary conversation. Data rates up to 300 bps are accommodated with no AC power connection.

The new modem joins the originate only 103, switch-selectable originate/answer 103 and Model 202 LP units previously announced.

For technical details and surprisingly low prices, contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone 205/837-8100; Telex 810-726-2100.

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CIRCLE 85 ON INQUIRY CARD

Created by Dayner/Hall, Inc., Winter Park, Florida

Floppy Controller Is Compatible with LSI-11 Series CPUs

One or two dual-density single- or double-sided floppy disc drives are supported by the SCD-RXV21 floppy controller for the LSI-11, -11/2, and -11/23. Available from Sigma Sales, Inc, 6505 Serrano, Anaheim Hills, Calif, the single dual-wide board replaces DEC's RXV21 control logic, and is software compatible with DEC operating systems and RX02 diagnostics.

Features include onboard formatting capability, which permits writing sector heads, checking written headers, and writing the data field in user selected density. An onboard, jumper selectable, transparent firmware bootstrap that automatically boots double-density diskettes provides jumper selectable 4-level interrupt priorities compatible with LSI-11/2 or -11/23. Power fail detect protects media during loss of power. Write precompensation reduces bit shift for greater data integrity, and write current control is provided for tracks greater than 43.

The controller is compatible with RX01/RX02 media, IBM 3740 format, and Shugart interface. It is also pin to pin, signal, and power compatible with Q-bus backplanes that support LSI-11 series CPUs and associated devices.

Circle 419 on Inquiry Card

Isolated Input Boards Expand Multibus Compatible Analog Input Systems

The DT1748-EX family of isolated input expander boards is intended to expand the channel capacity of Multibus compatible, single-board, analog interface systems. The boards, available from Data Translation, 4 Strathmore Rd, Natick, MA 01760, pass microvolt level input signals, while withstanding common mode voltage input levels to ± 250 V.

Additional isolated differential input channels are provided for the DT1748, DT1759, and DT3755 systems. The DT1748 is a 12-bit, low level/wide range, isolated analog input system containing up to 12 isolated differential input channels; the DT1759 combines a 4-channel low level/wide range, isolated analog input system with a 2-channel, nonisolated analog output system; the DT3755 intelligent analog peripheral includes a 4-channel, low level/wide range, isolated analog input system, an 8085A CPU, 16k bytes of dual-port RAM, EPROM storage, and serial I/O port.

The expander boards feature 8-, 16-, and 24-channel differential input models in which each channel uses a reed relay/flying capacitor design for high isolation and low level signal handling capability. Each is mounted on a single Multibus compatible board for immediate plug-in operation and can operate from 5 Vdc derived from the Multibus backplane. Operating temperature is 0 to 70 °C; safe storage temperature is − 25 to 85 °C. All models measure 6.75 x 12 x 0.375" (17.14 x 30 x 0.952 cm), directly fitting any Multibus backplane.

Circle 420 on Inquiry Card

8" Floppy Subsystem Offered in Integrated Hardware/Software Package

An 8" (20-cm) floppy subsystem for North Star users is offered in a fully integrated software/hardware package from John D. Owens Associates Inc, 12 Schubert St, Staten Island, NY 10305, that allows transfer of files from 5.25" (13.33-cm) media to 8" (20-cm) media, and vice versa. System hardware includes a Tarbell double-density controller, dual Shugart 800R drives, power supply, cabinet, fan, and all necessary cabling, and requires simple plug-in installation. The DMA-DOS software interface is a high speed, single-user, CP/M compatible 8080/Z80 disc operating system, produced by Dynamic Microprocessor Associates. The package provides auxiliary storage, and operates in single or double density on 8" (20-cm) media in an IBM compatible format.

DMA-DOS utilities and 20 basic system commands provide extensive control over processing activity. The system is easily configurable for a variety of I/O systems, and will support floppy or hard disc files of up to 4.2M bytes. Each file can be declared write protected, system wide, or invisible to the directory. Up to 16 user/project passwords allow each user to access only his own or system wide files. One master user may access any file. Up to six print files can be queued to a background print task for printing while system control is maintained by the user. When at the command level, the console input stream can be assigned to a saved file; all program requests for console input will be directed to the file until an EOF is detected or an abort sequence initiated. The software system is also available separate from the hardware/software package.

Circle 421 on Inquiry Card

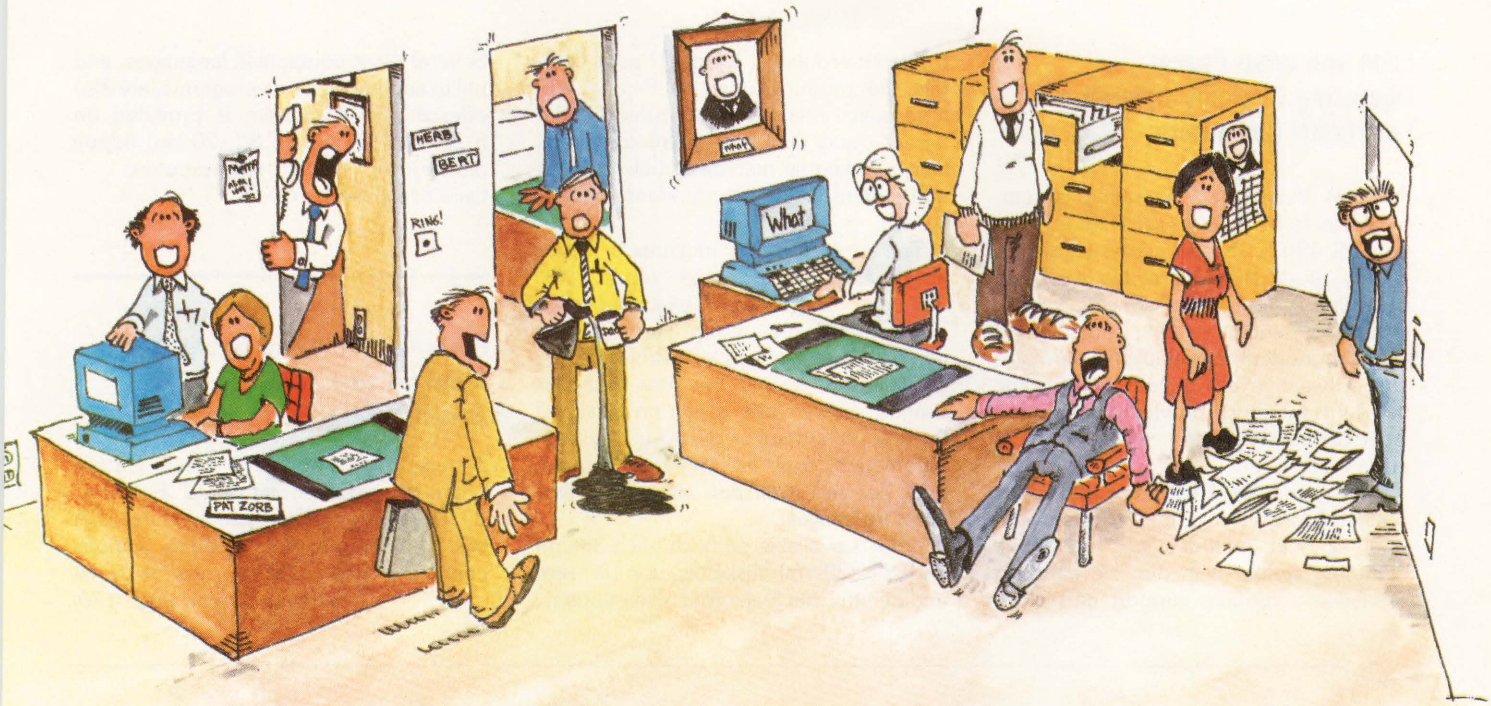
Single-Board Computer Provides Breadboarding Areas For Custom Circuitry

Custom 86 allows the user to develop a customized, 16-bit single-board computer, using components that best fit the application. The single-board computer uses a 5- or 8-MHz 8086 CPU, and is IEEE 796 standard bus compatible. A product of Microbar Systems Inc, 1120 San Antonio Rd, Palo Alto, CA 94303, the board has two breadboarding areas where circuitry can be added for a specific application. After the addition of specialized circuitry, the manufacturer can produce a custom board to be used in an OEM volume market. The system allows the flexibility of a CPU board designed from scratch to be combined with the shorter design cycle provided by a standard board product.

Fully buffered 20-bit address and 16-bit data bus lines are brough out to wirewrap stakes in order to allow custom memory capability. For I/O functions or other circuitry, the connections for the microcomputer's control lines, chip-select lines, and some prototyping interconnections are all brought out to the prototyping area. The breadboard area will accept any standard 0.3 or 0.6" (0.7 or 1.5-cm) socket. The CPU area accepts 2 user-installed 50-pin flat ribbon cable connectors for interfacing other devices or boards.

Circle 422 on Inquiry Card

A SOLUTION TO SOFTWARE DEVELOPMENT PROBLEMS?



FUTURESOFT Has The Only Complete Solution: Debug, Analyze, Verify.

FUTURESOFT'S software emulators are a new concept in develoment tools for the software engineer. They have been designed to help reduce debugging time, increase debugging proficiency, analyze software performance and identify percent of program tested. In short, to provide you with the complete solution to your software development problems.

DEBUG – The **FUTURESOFT** software emulator has eight breakpoints, each of which can have eight nested conditions to provide detection of the most complicated software faults. In addition, the last 255 instructions executed are always saved in the TRACE buffer; or you may opt to save TRACES for jump instructions only.

ANALYZE – The **FUTURESOFT** software emulator automatically times program execution so that you may quickly determine which part of a program is taking the most time, or whether an interrupt routine can handle the required rate of interrupts. You simply specify a set of regions, and the software emulator will keep track of the executed cycles in each region.

VERIFY – The **FUTURESOFT** software emulator automatically monitors program execution and provides you with two levels of information which aid in thorough testing and verification of software. First, it tells you the percentage of instructions in the program which have been executed. Secondly, it tells you the percentage of possible execution paths the program has taken. For the first time, a meaningful number may be used to specify the degree to which software has been verified.

Seeing is believing, and we believe that once you see how effective our emulators are, you too will become a believer. **FUTURESOFT** — the *only* complete software development solution. Just complete and return the coupon for details.

Oh boy, am I interested! Please send me more information on:

☐ 6800 Emulator ☐ 8048 Emulator
☐ 6801 Emulator ☐ 8051 Emulator
☐ 6805 Emulator ☐ GR 2300 DIAGNOSTICS Package

My development system is a ______________________

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Company ______________ Phone ______________
Address ______________________
City, State, Zip ______________________

FUTURESOFT

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Canoga Park, California 91304 (213) 704-5808

CP/M and UCSD Pascal Operating Systems Offered For Heath Computers

A CP/M Version 2.2 operating system, available from Heath Co, Benton Harbor, MI 49022, allows access to a wide variety of CP/M based software. Three operating system modules are included: BIOS, BDOS, and CCP. BIOS, implemented as a disc resident relocatable file, contains all hardware level I/O code. CCP is the transient monitor, providing command level communications between the user and CP/M.

Configured for Heath Computers by Softech Microsystems, the P-System with UCSD Pascal includes an interactive operating system with disc file handling capabilities, runtime support and block I/O service routines, a 1-pass Pascal compiler that produces universal P-code, and a compact interpreter that runs P-code. Screen- and character-oriented editors, filer, conditional macroassembler, linker, and system library are standard with the system.

The CP/M package includes a 2-pass absolute assembler, text editor, 8080 debugger with traced execution and disassembly, file dump, and system generation and relocation. Programs are provided to display file sizes and disc usages, set file class, assign physical and logical devices, display system parameters, copy files between devices, and convert internal HEX files into memory images.

CP/M is available on 5.25" (13.33-cm) and 8" (20-cm) diskettes, for H8, H89, and Zenith Data System's Z-89 computers. Several CP/M compatible languages, and utility and applications programs, are also offered. The P-System is provided on 5.25" (13.33-cm) or 8" (20-cm) floppy discs for the H8 and Z-89 computers.

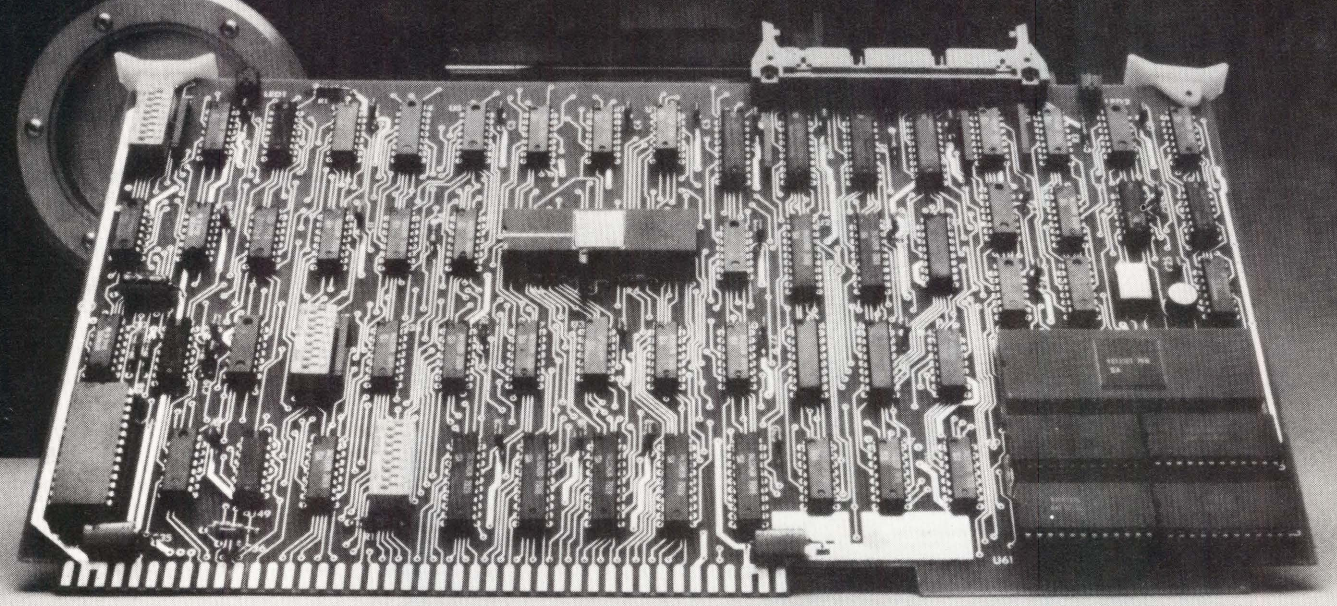
Circle 423 on Inquiry Card

Portable Operating System Allows Users to Move Among 16-bit Processors

A transportable operating system (TROS), offered by Corporate Data Sciences, 3910 Freedom Cir, Santa Clara, CA 95050, automatically handles various configurations, allowing users of 16-bit

(continued on page 170)

The little guys have done it again.



PRESENTING THE FIRST ANSI WINCHESTER DISK CONTROLLER FOR MULTIBUS.™ AVAILABLE TODAY. FROM INTERPHASE.

The WDC 2880 is an Intelligent Controller for up to 8 ANSI X3T9.3 compatible Winchester drives. It gives your MULTIBUS system true performance.

Hardware ECC, Automatic Error Recovery, Sector Interleaving, Bad Track Mapping, and Overlapped Seeks mean High Performance on the Disk side.

Maximum speed DMA, 8 and 16 bit data transfers, both Absolute and Relative 20-bit addressing modes mean High Performance on the MULTIBUS side.

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Drivers for many standard Operating Systems available now.

You've come to expect high quality innovations first from Interphase. The most talented Intelligent Disk Controller specialists in the country. And the WDC 2880 is no exception. It is elegant, well designed, affordable and available off the shelf.

But that's not all. We give you full support to help you integrate it into your system. So why wait for someone else? Call or write us today.

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CIRCLE 88 ON INQUIRY CARD

microprocessors and minicomputers to move from system to system without converting their applications software. The system incorporates device independent I/O, and the message based organization facilitates expansion and networking.

An editor, command line interpreter, and BASIC interpreter are features of the system, which allows realtime multiprogramming with a large number of users and tasks. Sequential, random, and indexed file organizations are supported and may be maintained on floppy and/or hard discs.

Motorola 6800, Intel 8086, National 16000, and Zilog Z8000 16-bit processors, and DEC PDP-11 and VAX-11/780, Data General ECLISPE MV8000, and Interdata 8/32 minicomputers can use this system in realtime applications such as information management, networking, distributed data processing, process control, business analysis, and engineering, scientific, and medical inquiry and development systems. Additional versions for other 16-bit microprocessors, and for Pascal, ADA, FORTRAN, and COBOL compilers, and a data management system, are planned for late this year.

Circle 424 on Inquiry Card

Cross Assembler Transforms Various Computers Into Development Systems

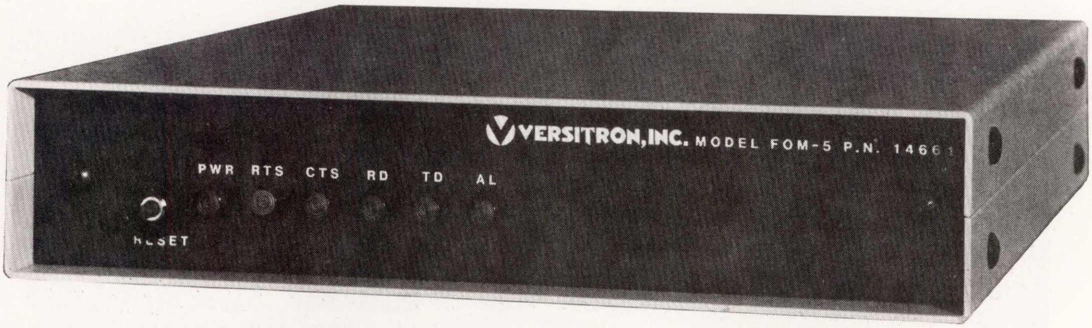
Programs for Zilog Z80 microprocessors are generated by various minicomputers using the Z80 cross assembler software package. Available from Millenium Systems, Inc, 19050 Pruneridge Ave, Cupertino, CA 95014, the package, when combined with a MicroSystem Emulator, transforms the computer into a complete development system. It can also be used with FASTPROBE test generator software to create functional test programs for production test and field service of Z80 based systems.

The package includes a MACRO assembler for translating source programs into relocatable object modules, a linking loader to connect relocatable object modules into a single program for execution and debugging, and a formatter that arranges the linked program into a form that can be transferred to the emulator, analyzer, or designer for execution. The downloader performs the actual transmission of the formatted program. The package is written in ANSI standard FORTRAN IV to ease maintenance, modification, and installation. Source code is provided on floppy disc or magnetic tape for compilation on the host system.

Systems and configurations specifically supported by the cross assembler include DEC's PDP-11 and LSI-11 with either an RT-11 or RSX-11 operating system, Data General's NOVA 1200 or ECLIPSE with either RDOS or AOS, HP 1000 or 3000, and TI 990/10. The assembler may be installed on any host computer that includes a FORTRAN IV compiler, supports a data word length of at least 16 bits and a disc or magnetic tape facility, and provides at least 20k words of RAM.

Circle 425 on Inquiry Card

fiber optic modem for local data distribution



multiplexes control signals along with the data

Fiber optic modems are ideally suited for many local data distribution applications since they offer several inherent advantages over conventional hard-wired systems. These include immunity from rf and magnetic signals, increased bandwidth, and a significant improvement in the security of the data link.

Versitron's FOM-5 fiber optic modem (one of a family of fiber optic modems) not only provides the basic advantage of fiber optics, but also offers several unique system operating features that makes it ideal for local data distribution applications.

Multiplexes Control Signals — Three separate control signals in each direction are multiplexed with the data over the fiber optic link. This provides a fully interactive handshaking sequence with the FOM-5 functioning as a truly transparent device at both ends of the link.

Increased Throughput and Range — The FOM-5 operates full duplex over a fiber optic cable pair at synchronous rates of 50 or 56 kbps and asynchronous rates up to 14 kbps; with an operating range of 1 kilometer.

Intrusion Alarm — The receive circuitry continuously monitors the receive data for the presence of the multiplexer sync signal generated by the remote unit. Loss of this signal will cause an audible alarm condition and block further data transmission at both local and the remote modems. After verifying that the link is still secure, the system may be reset from either the local or remote unit.

Plug-In Compatibility — The FOM-5 has DSU/V35 or RS-232/MIL-188 interfaces. Precut and terminated fiber optic cables are also available from Versitron.

Versitron, Inc. installed its first fiber optic link utilizing a multiplexed data technique in the early 1960's. Since that time we have sold over 19,000 fiber optic links covering a wide variety of requirements for military and commercial applications.

VERSITRON

Versitron, Inc. 6310 Chillum Place N.W. Washington, D.C. 20011 (202) 882-8464

CIRCLE 90 ON INQUIRY CARD

DS BRIEFS

Development System Available for 6800/6809 μProcessors — Scoutsystem development systems for 6800/6809 microprocessors, from Smoke Signal Broadcasting, 31336 Via Colinas, Westlake Village, CA 91362, provide up to 64k bytes of RAM and 2M bytes of disc storage. System includes Hunter shortcut debug package, uses standard Motorola assembler directives, and provides MDOS conversion package, text editor, text processor, EPROM programmer, and memory diagnostics.
Circle 435 on Inquiry Card

Software Provides Interactive Forms Capability for μComputers — Screen Interaction Module (SIM), from Solid State Technology, Inc, 160 New Boston St, Woburn, MA 01801, allows programmers to create forms for operators to fill in the blanks using series 8100 computers. It also permits full editing, such as insertion, deletion, and movable character, words, lines, and cursor, providing reduced development time and memory requirements for program execution. COBOL, FORTRAN, BASIC, and MACRO 85 (assembler) languages are offered with the module.
Circle 436 on Inquiry Card

Multiplier/Accumulator Board Uses Sophisticated Arithmetic Processor — SBC bus compatible multiplier/accumulator board facilitates the use of sophisticated arithmetic procedures such as matched filtering and fast Fourier transforms. Available from Adaptronics, Inc, 1750 Old Meadow Rd, McLean, VA 22102, it provides add, subtract, multiply, and accumulate operations, on normal or sign extended (8- to 32-bit) data; functions can be performed in 2's complement, fractional, or integer notation. Data and control bytes are memory mapped for speed and ease of use.
Circle 437 on Inquiry Card

Industrial FORTRAN Added to Development Software Language — Industrial FORTRAN 77, available from Xycom, Inc, 750 N Maple Rd, Saline, MI 48176, is fully integrated and compatible with industrial Pascal, and runs on all the company's development hardware configurations. It can perform industrial multitasking and process I/O, be burned into EPROM, and be downloaded to target/remote control or source data acquisition equipment.
Circle 438 on Inquiry Card

Economy Processor Board Provides for Memory and I/O Expansion — Four 28-pin sockets for EPROM/RAM and three SBX module positions for I/O expansion are provided by the ZX-80/05, a high performance 8085A-2 processor board. Available from Zendex Corp, 6680 Sierra Lane, Dublin, CA 94566, the board is 100% software transparent to code generated for the Intel SBC-80/05, and uses the Mostek byte-wide memory socket concept for RAM/ROM mixing.
Circle 439 on Inquiry Card

Power Supply Available for AIM 65 Systems — AIM-Mate power supply, from Forethought Products, 87070 Dukhobar Rd, Eugene, OR 97402, powers a complete system, including AIM-65, Memory-Mate, Video-Mate, and Floppy-Mate boards. The unit is slim enough to fit into many custom enclosures and includes short circuit and overvoltage protection.
Circle 440 on Inquiry Card

Hard Disc Controllers Support Multiple Drives — Multiple 8 or 14" (20 or 36-cm) drives with SMD or ANSI standard interfaces are supported by the DC100 series hard disc controllers for the LSI-11 bus. The controllers, from Alcyon Corp, 8474 Commerce Ave, San Diego, CA 92121, are software compatible with standard DEC operating systems and data reliability diagnostics, and feature a proprietary multiprocessor architecture utilizing bipolar array logic.
Circle 441 on Inquiry Card

Software Displays 21 Colors on Apple II — MICRO-PAINTER software, from Datasoft, Inc, 16606 Schoenborn St, Sepulveda, CA 91343, employs high resolution graphics to "paint" pictures in 21 different colors on the Apple II. The program is written in both BASIC and machine language, and includes a magnification feature for dot by dot and inverse coloring; pictures can be saved, or displayed either unpainted or in any combination of colors. Pictures can be repainted at any time.
Circle 442 on Inquiry Card

High Density Dot Matrix Printer Offered for Word Processing Applications — A proportionally spaced, high density dot matrix printer, the Line Printer IV, from Tandy Corp/Radio Shack, 1800 One Tandy Ctr, Fort Worth, TX 76102, produces 80 or 132 upper- or lowercase characters per 8" (20-cm) line for word processing applications. Special characters offered include the grave accent, braces, back slash, and caret. True underlining, subscripts, superscripts, fixed or proportional print, enlarged characters, boldface, and forward or reverse line feeds are also provided.
Circle 443 on Inquiry Card

128k-Byte MOS Memory Available for LSI-11 μComputers — Fast, add-in MOS memory for the DEC LSI-11 family features onboard refresh, parity, and provision for battery backup. Available from Cambex Corp, 360 Second Ave, Waltham, MA 02154, the board is double the density of standard DEC memory with up to 128k bytes of RAM on a single, dual-height card. It is available also in 32k-, 64k-, and 96k-byte configurations.
Circle 444 on Inquiry Card

Single-Board μComputer Serves Range of Functions — QCB-9 microcomputer card, based on the 6809 8-bit microprocessor, features onboard floppy disc controller, RS-232-C serial communications interface, two 8-bit parallel ports, up to 24k bytes of EPROM or 6k bytes of RAM, flexible I/O and memory addressing, S-100 bus structure, and power regulation. A product of Logical Devices, Inc, 1525 NE 26th St, Fort Lauderdale, FL 33305, the board performs functions ranging from word processing and software/hardware development to industrial control.
Circle 445 on Inquiry Card

Controller Supports Cartridge Tape Drive — DZ-80 Piggy Back Tape Controller/software package links a Data Electronics Funnel or equivalent cartridge tape drive to any Z80 based system, and permits Winchester disc backup. The controller, manufactured by Alloy Engineering Co, Inc, 85 Speen St, Framingham, MA 01701, is plug compatible with the Z-80 and provides an interface via 16 I/O ports to the CPU.
Circle 446 on Inquiry Card

Extended Disc Storage Achieved with Double Tracking Feature — Gnat Computers, Inc, 7895 Convoy Ct, Bldg 6, San Diego, CA 92111, offers 1.6M bytes of additional online disc storage for the desktop System 10 microcomputer. Extended storage is achieved by the addition of a double tracking feature to the double-sided, double-density, 5.25" (13.33-cm) disc drives. The additional disc space is sufficient to operate accounting software, including accounts receivable, accounts payable, payroll, and general ledger.
Circle 447 on Inquiry Card

Counter/Timer Board Handles up to 4 Digital Signal Sources — ZT 7399, a STD BUS compatible BCD counter/timer board, provides two independent 4-digit BCD counters that can be controlled by either a Z80 or 8085 CPU. A 4-input digital multiplexer is supplied on the front end of each counter; four separate digital signal sources may be counted under computer control. The board is available from Ziatech Corp, 2410 Broad St, San Luis Obispo, CA 93401.
Circle 448 on Inquiry Card

MICRO DATA STACK

DS BRIEFS

Alphanumeric Video Display Board Provides 1920 Positions—A Multibus compatible, alphanumeric memory mapped video display board, model VR-109A, available from Datacube, Inc, 670 Main St, Reading, MA 01867, generates 12 or 24 lines of 40 or 80 characters each under software control. Each character position provides regular or reverse video, underline, half-intensity, and blink display attributes usable in any combination, and limited graphics capability; an input port is provided for an external keyboard operating in an interrupt or polled mode.
Circle 426 on Inquiry Card

Board Expands System RAM Capability—32k to 128k dynamic RAM board, available from Central Data Corp, 713 Edgebrook Dr, Champaign, IL 61820, allows the user to add 32k, 64k, 96k, or 128k of dynamic RAM to an existing system. Parity checking is standard and will generate an interrupt if any single-bit memory error occurs.
Circle 427 on Inquiry Card

Microcomputer System Features Dual-Floppies with Status Panels—Model 6100 is an expandable Z80A based microcomputer system incorporating a pair of floppy disc drives, with six status indicators each, that verify major functions while aiding operation, programming, and debugging. Available from Innotronics Corp, Brooks Rd, Lincoln, MA 01773, the system is compatible with the CP/M operating system, IBM 3740 single-density format, IBM 2D double-density format, S-100 bus, and RS-232-C.
Circle 428 on Inquiry Card

RM/COBOL Available Under CP/M—RM/COBOL for the OEM market is available for custom installation under the OEM's operating system or general purpose operating systems such as OASIS, CP/M, or UNIX. Providing language level and features necessary for real world application development, the software is offered to OEMs under a fully paid, unlimited volume license or a per copy royalty license, from Ryan-McFarland Corp, 609 Deep Valley Dr, Palos Verdes, CA 90274.
Circle 429 on Inquiry Card

Small Business Computer Provides 64k of RAM—Available from Ai Electronics Corp, 2-28-16 Shimomaruko, Ohta-ku, Tokyo 146, Japan, ABC-26 provides 64k bytes of RAM, and peripheral support allows up to 1M byte of RAM extension. The system also contains 280A processor, floating point hardware, separate keyboard, 12" (30.5-cm) CRT, and dual 8" (20-cm) floppy drives. Three powerful operating systems and a variety of high level languages are available.
Circle 430 on Inquiry Card

Diskette Controller Eliminates Need for Full Size SBC Board—ZBX-218 controls up to four double-sided, double-density, 8" (20-cm) diskette drives, eliminating the need for a full size SBC-board diskette controller. The controller, complete with clock, data separator, and PLL circuitry, is available from Zendex Corp, 6398 Dougherty Rd, Dublin, CA 94566.
Circle 431 on Inquiry Card

8-W Supply Powers Microcomputers—PS-80 power supply from Miller Technology, 16930 Sheldon Rd, Los Gatos, CA 95030, can be card edge mounted or attached by standoffs to the M-80 microcomputer and can supply at least two fully stuffed M-80 boards. A standard slo-blo fuse is mounted on the board in fuse clips, reducing external wiring.
Circle 432 on Inquiry Card

CP/M2 Available for C3 Computers—CP/M2, for Ohio Scientific's C3 computers, compensates automatically for 2-or 4-MHz operation and is compatible with the original CP/M disc format; software and data on current CP/M discs can be retained. The system, available from Lifeboat Associates, 1651 Third Ave, New York, NY 10028, operates only with the Z80 processor, and includes a CP/M disc to disc copy routine, a memory test program, and I/O drivers.
Circle 433 on Inquiry Card

Z80 Based Microcomputer Provides Multiuser Capability—C8001MU, a 5-user, Z80 based microcomputer system combining 8" (20-cm) Winchester disc drives and tape cartridge drives in a desktop enclosure, is available from Onyx Systems, Inc, 73 E Trimble Rd, San Jose, CA 95131. The system is fully compatible with all application programs currently available with the C8001; software includes MOASIS, multiuser BASIC, and COBOL. □
Circle 434 on Inquiry Card

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  - Pre-Programmed/User-Programmable
  - Async/Byte Sync/Bit Sync
  - IBM Bisync (3270, 2780, 3780)
  - IEEE 488-78 (GPIB)
  - 4 Channels/Module
  - DMA
- Level Converters
  - RS-232/RS-422/RS-423/20 mA
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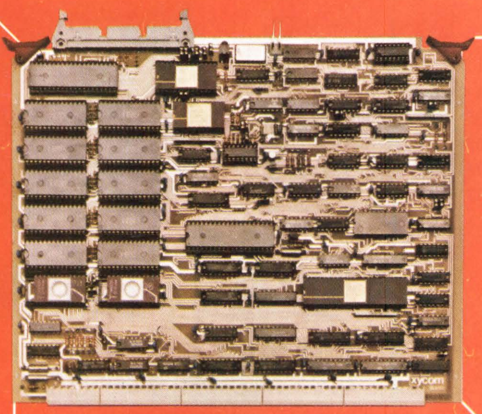


CIRCLE 92 ON INQUIRY CARD

Microprocessors Run at Minicomputer Floating Point Levels

Pete Heller
Intel Corporation
2625 Walsh Ave, Santa Clara, CA 95051

Almost since the first microprocessor was introduced, the microcomputer industry has recognized the need for inexpensive numerical computing. Many applications, such as small business systems, scientific or engineering processors, process control devices, industrial robotics, and instrumentation, require timely and precise numerical processing—but at reasonable cost. Although minicomputers can meet the technical need, they are prohibitively expensive for these applications. Now, however, many microprocessor systems can provide the necessary low cost numerical processing, including floating point operations.

Examples of Floating Point Microprocessor Products

To meet the need for low cost floating point capability in these small systems, Intel in 1977 introduced the FPAL library of floating point software routines which run on the 8080 and 8085 microprocessors. FPAL provided the function required but not the performance level called for by these applications. However, products introduced since then have been designed to address the need for higher performance floating point computational capability.

The iSBC 310, a single-board computer introduced in 1978 and based on Intel's 3000 series of bit-slice processors, provided about ten times the performance of FPAL. Then, in 1979, two 8-bit peripheral devices were introduced for use in 8080 or 8085 class designs. One of these, the 8231, executes, in hardware, many floating point functions for arithmetic, trigonometry, and exponentiation. The other, the 8232, provides only floating point add, subtract, multiply, and divide. Both deliver approximately the same level of performance as the iSBC-310, but are simpler to use and are more cost effective.

Following the introduction of the iAPX 86/10 (8086 CPU) 16-bit microprocessor, the company has developed a 2-chip configuration to provide special support for high performance numerics processing. That configuration, consisting of an 8086 CPU and an 8087 CPU extension (NPX), forms the iAPX 86/20 floating point numeric data processor. In addition, the iAPX 88/20, an 8088 CPU with an 8087 math processor extension, is available. (Figs 1 and 2.)

Both of these floating point numeric data processors perform high speed calculations on 32-, 64-, and 80-bit floating point numbers, 16-, 32-, and 64-bit integers, and 18-digit binary coded decimal numbers. The 86/20 has a full complement of arithmetic, logical, and processor control instructions for both the general CPU and the floating point numeric extension. Also included are instructions that execute trigonometric, logarithmic, and exponential functions, load special constants (π, $\sqrt{2}$), and control accuracy, eg, rounding.

Compared with other microcomputer numeric processing alternatives, the 86/20 is faster by a factor of up to

(continued on page 178)

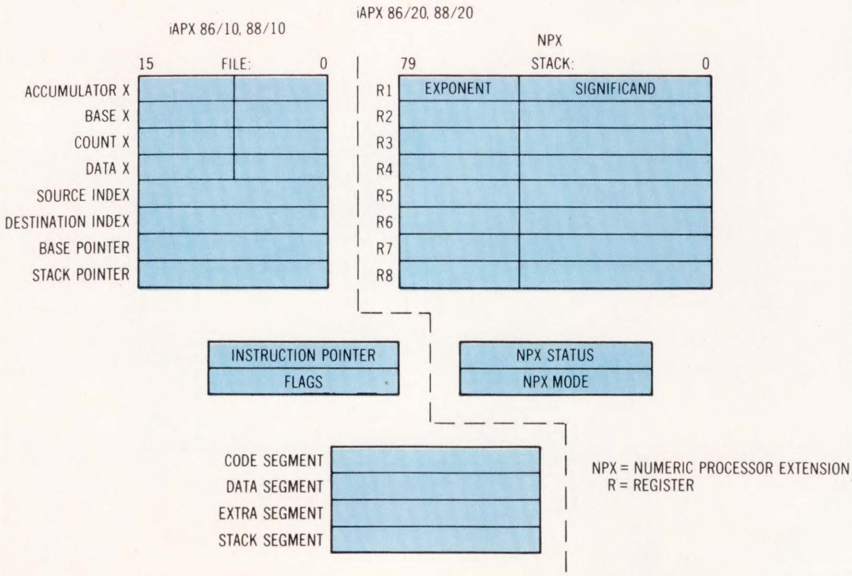


Fig 1 Floating point numeric processor expands architecture of iAPX 86/10 (shown to left of dotted line). Eight 80-bit registers, two operations status registers, and math processing instructions are added

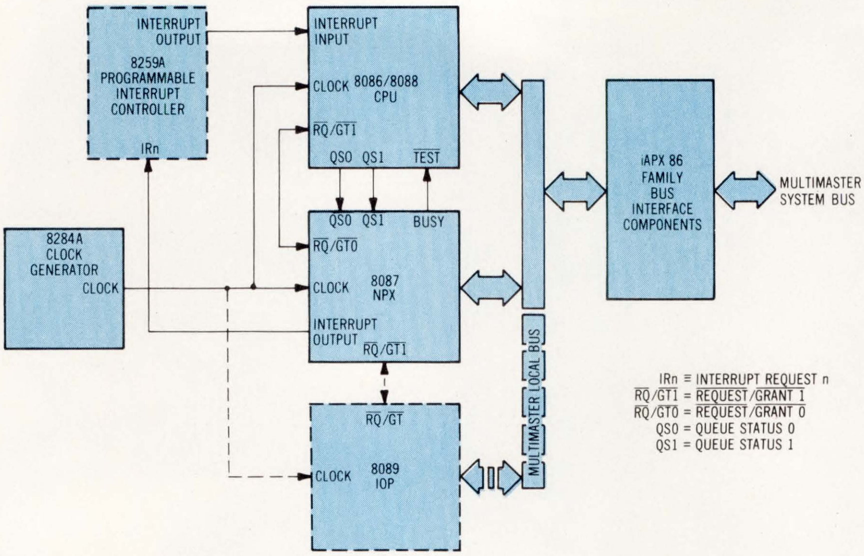


Fig 2 8087, from Intel, is connected in parallel with 8086 or 8088. It reads same instruction stream as 8086 or 8088, recognizes those instructions it is to operate on, then begins processing. This improves performance over system where math processor acts as "peripheral" chip and is addressed by CPU as memory location

ten. Most dramatic is a comparison with a microprocessor executing numeric algorithms in software. In this case, the 86/20 is often 100 times faster. The device runs at approximately 75% of the throughput of a PDP-11/34 minicomputer with floating point hardware. From a performance standpoint designers can now use a microsized product and obtain minicomputer levels of capability. (See the Table.)

Designing in a floating point numeric data processor is no more difficult than designing in a general purpose microprocessor. The floating point instructions are part of the applications programming language repertoire and are the same whether execution takes place in software or hardware. Thus, a system originally configured to handle math processing using the 8087 software emulator can be quickly converted to a hardware environment without affecting the applications source code.

Concern for rounding errors is practically eliminated because the 86/20, using 80-bit registers, delivers up to 19 decimal digits of floating point precision. The 86/20, like FPAL, the iSBC 310, and the 8232, complies with all the provisions of the proposed IEEE floating point standard. The value of the standard is that regardless of which machine or processor is doing the mathematical calculations, the results will be repeatable and reliable if those calculations conform to the standard. Even more important, the results will be identical.

Conclusions

Floating point numeric processors represent a breakthrough for microcomputers. The performance, range, and accuracy of microcomputers is high enough to be a practical alternative to more expensive and larger systems. Applications such as standalone graphic terminals, high speed industrial control systems, robot systems, and high speed/high accuracy data acquisition systems can now be built using smaller, less expensive microcomputer technology.

iAPX 86/20 Performance Comparisons

Throughput Speed Comparison*

Processor	Relative Throughput Speed (86/20 = 1)
iAPX 86/10 Emulation	0.01
Intel 8232	0.1
DEC LSI-11/23**	0.1
iAPX 86/20	1.0
DEC PDP-11/34**	1.33
DEC VAX 11/780	7.0

Instruction Speed Comparison (μs)

Floating Point Instruction	86/20	PDP-11/34**	LSI-11/23**	8232	86/10
32-bit Multiply	18	16	80	50	1,600
64-bit Multiply	27	26	193	437	2,100
Square Root	36	—	—	—	19,600

* Based on Whetstone standard floating point benchmark.
**With floating point unit.

Intelligent Peripheral Controller Designed for Distributed Processing and Multitasking Applications

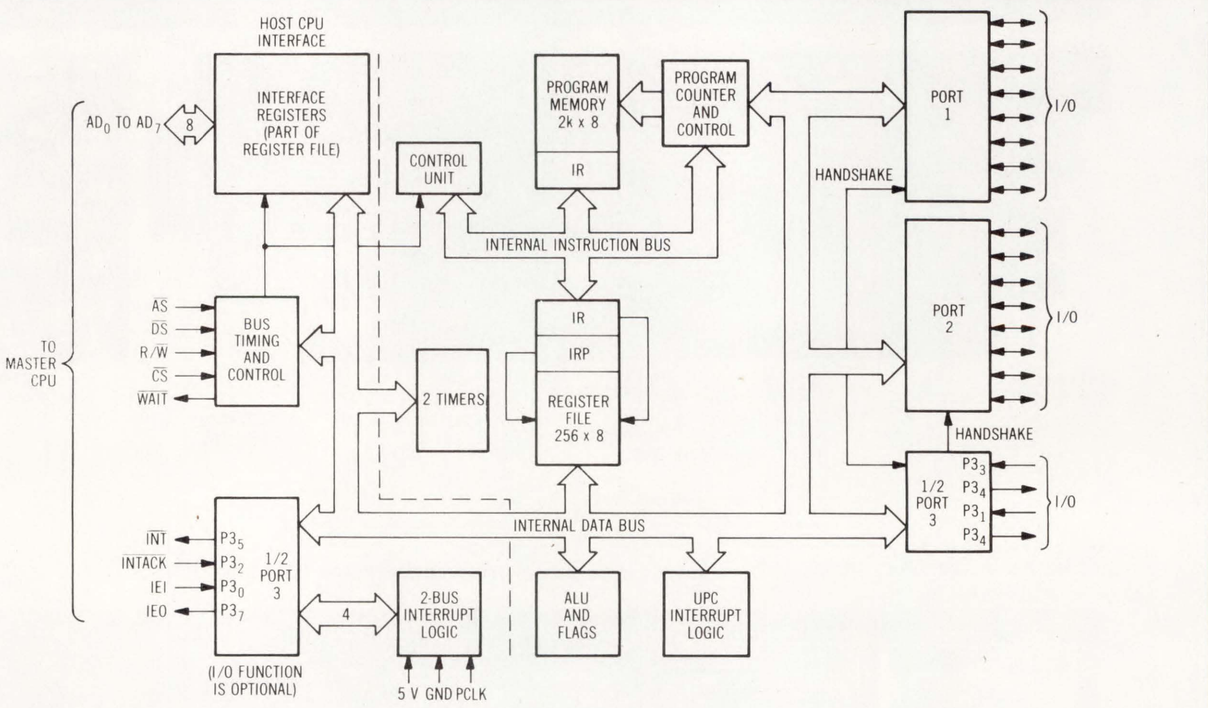
Based on the architecture and instruction set of the Z8 single-chip microcomputer, a universal peripheral controller (UPC) assumes tasks traditionally performed by host processors, such as arithmetic, translation and formatting of data, and control of I/O devices. From Zilog, 10340 Bubb Rd, Cupertino, CA 95014, the Z-UPC features 2k bytes of internal program ROM, a 256-byte register file, 3 programmable 8-bit I/O ports, 2 counter/timers, and 6 levels of internal prioritized interrupts.

Z-UPC's internal register file contains 234 general purpose registers, 19 status and control registers, and 3 I/O port registers. The internal register file containing I/O port and control registers is accessed by the Z-UPC program and indirectly by its associated master CPU. This architecture results in both byte and programming efficiency because UPC instructions can operate directly on I/O data without moving it to and from an accumulator. Such a structure allows the user to allocate as many general purpose registers as the application requires for data buffers between the CPU and peripheral devices. All general purpose registers can be used as address pointers, index registers, data buffers, or stack space.

The register file is logically divided into 16 groups of 16 working registers each. A register pointer is used in conjunction with short format instructions, resulting in tight, fast code, and easy task switching.

Twenty-four of the UPC's 40 pins can be dedicated to I/O functions. Grouped logically into three 8-line ports, these can be programmed in various I/O combinations with or without handshake. Two programmable 8-bit hardware counter/timers, each with a 6-bit prescaler, relieve the UPC software of handling realtime counting and timing problems. Both counter/timers are independent of program execution.

To cover a range of system peripheral device control needs, the UPC is offered in four versions other than its standard configuration, including: a 64-pin development version, Z8091, with external interface for up to 4k bytes of ROM; a 64-pin version, Z8092, with external interface for up to 4k bytes of RAM which can be downloaded from the master CPU; a 40-pin protopack version, Z8093, with a socket for up to 2k bytes of ROM; and, a 40-pin protopack RAM version, Z8094, with a socket for up to 2k bytes of RAM which can also be downloaded from the master CPU. Circle 461 on Inquiry Card



AD$_0$ TO AD$_7$ = ADDRESS/DATA LINES
$\overline{\text{AS}}$ = ADDRESS STROBE
$\overline{\text{DS}}$ = DATA STROBE
R/$\overline{\text{W}}$ = READ/WRITE (INPUT)
$\overline{\text{CS}}$ = CHIP SELECT
RP = REGISTER POINT
IRP = INTERRUPT PRIORITY
P3$_1$ TO P3$_7$ = I/O PORT LINES
$\overline{\text{INTACK}}$ = INTERRUPT ACKNOWLEDGE
PCLK = CLOCK (INPUT)
IEI = INTERRUPT ENABLE INPUT
IEO = INTERRUPT ENABLE OUTPUT
UPC = UNIVERSAL PERIPHERAL CONTROLLER

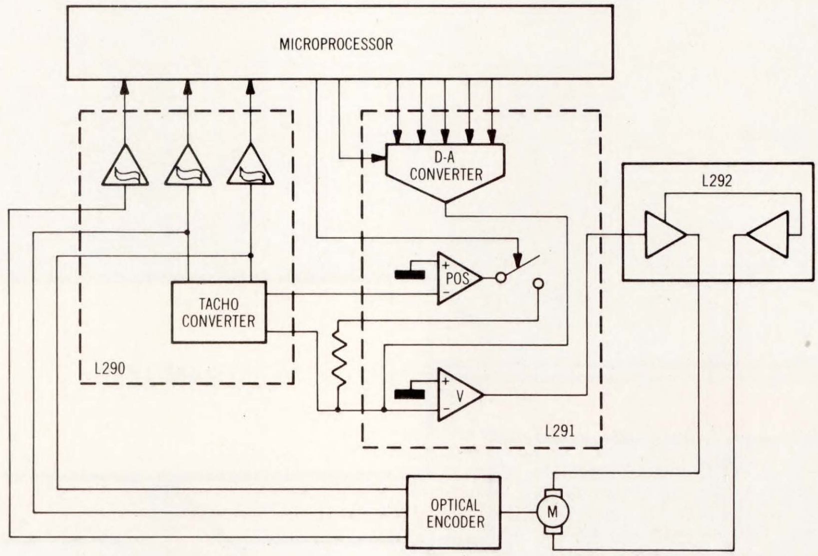
Functional block diagram of Zilog's Z-UPC. Communication between master CPU and register file is accomplished via one group of 19 interface registers addressed directly by CPU and UPC or via block transfer. Access by CPU is controlled by UPC to allow independence between CPU and UPC software

3-Chip Positioning System Is Microprocessor Controlled

The L290/1/2 positioning system, from SGS-Ates Semiconductor Co, 240 Bear Hill Rd, Waltham, MA 02154, is a complete dc motor positioning system that can be directly controlled by a microprocessor. Two servo modes are used. Initially, velocity control takes the motor towards the target position, but as this point is approached, the system switches to position control to stop the motor in the desired position. Motors can be driven directly at up to 70 W. A typical application is carriage daisy wheel position control in typewriters.

L290, the tachometer chip, processes three rate and position signals from an optical encoder and provides a reference voltage for the DAC to ensure that the overall system characteristics remain constant in spite of input variation, temperature changes, and device aging. A system error amplifier, a position amplifier, and the direction/mode switches controlled by the microprocessor are implemented in the L291 DAC and position amplifier. Both chips are packaged in 16-lead plastic DIPs. The L292 switch mode driver IC handles up to 2 A at 36 V using a protected H-bridge output. Different motor characteristics are accommodated by an externally programmed current feedback loop. Additional L292s are easily synchronized and two logic enable inputs are provided. The device is packaged in a 15-lead MULTIWATT package.

Speed commands for the system originate in the microprocessor. It is continuously updated on the motor position by means of pulses from the L290 tachometer chip, which in turn gets its information from the optical encoder. From this basic input, the microprocessor computes a 5-bit control word that sets the system speed dependent on the distance to travel. When the motor is stopped and the microprocessor orders it to a new position, the system operates initially in an open loop configuration as there is no feedback from the tachometer generator. Therefore maximum current is fed to the motor. As maximum speed is reached, the tachometer chip output backs off the processor signal, thus reducing accelerating torque. The motor continues to run at top speed but under closed loop control.



Block diagram of SGS-Ates's 3-chip microprocessor controlled positioning system. L290, tachometer converter, integrates tacho voltage generator, reference voltage generator, and position pulse generator functions. L291, DAC and position amplifier, integrate 5-bit DAC, error and position amplifier functions. L292 is switch mode driver

As the target position is approached, the microprocessor lowers the value of the speed demand word; this reduces the voltage at the main summing point, in effect braking the motor. The braking is applied progressively until the motor is running at minimum speed. At that time, the microprocessor orders a switch to the position mode, and within 3 to 4 ms the L291 drives the motor to a null position, where it is held by electronic detenting.

Circle 462 on Inquiry Card

GaAs IC, ALU, and RAM Recently Fabricated

A highlight of the 1980 IEEE Gallium Arsenide Integrated Circuit Symposium was a report by F. S. Lee and co-workers from Rockwell International that the company had fabricated a GaAs IC. The Rockwell LSI circuit, an 8 x 8 multiplier, contains 1008 equivalent gates fabricated from approximately 6000 transistors and diodes. High logic gate density (2×10^4 to $10^5/cm^2$) is achieved by use of a planar process which employs projection optical lithography and selective multiple ion implantation to provide 1-μm MESFETs and Schottky diodes.

K. Suyama reported on details of an ALU fabricated by Fujitsu Laboratories using 2-μm design rules and planar ion implantation techniques. The propagation delay time is 190 ps with 12-mW power dissipation for a ring oscillator test circuit positioned on the chip near the ALU.

GaAs static RAM designs, with a basic memory size of 57 x 40 μm, were reported by D. K. Kinell, of Lockheed Microelectronics Center. This small size is suitable for 4k-bit static RAMs with a chip size of 5 x 3.5 mm. Data were presented showing cell read and write operation with a 0.4 output signal for a 1.3-V total power supply voltage.

Circle 463 on Inquiry Card

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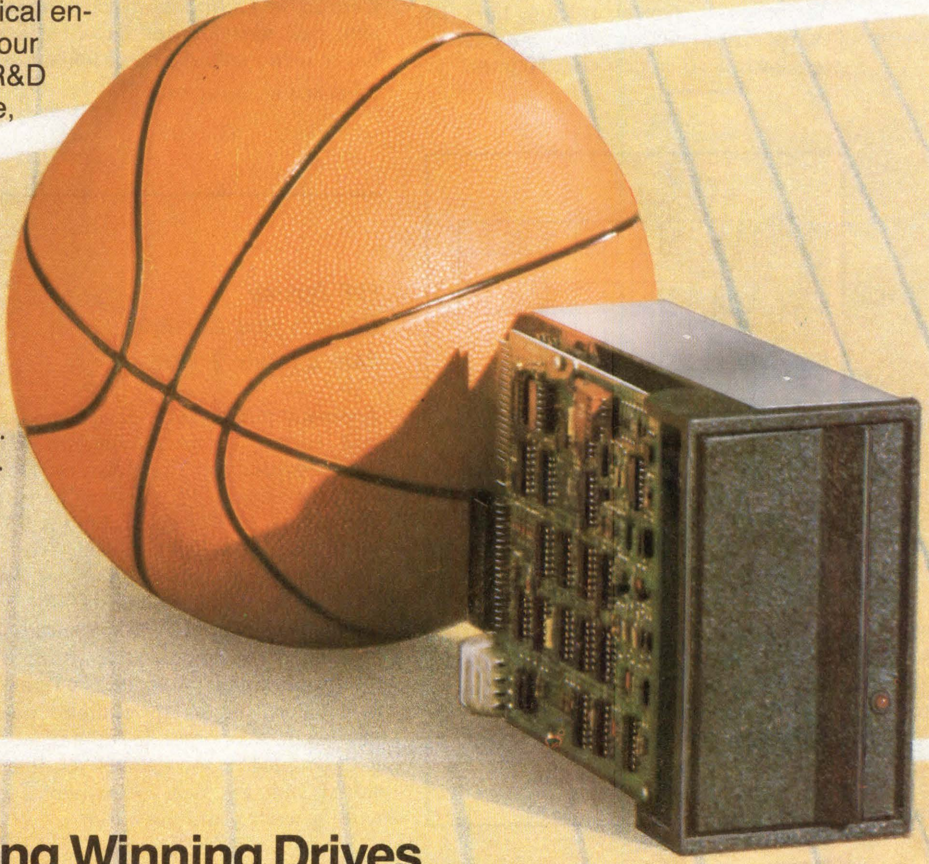


Siemens: Engineering Winning Drives.

CIRCLE 97 ON INQUIRY CARD

Family of Converters And Op Amps Are Specified Over −55 to 200 °C

Designed for data acquisition and control systems as well as instumentation applications, an ADC, DAC, and general purpose op amp can operate over −55 to 200 °C. The family of integrated circuit components was recently announced by Burr-Brown, Internat'l Airport Industrial Pk, Tucson, AZ 85734. A fast slewing op amp with a −55 to 175 °C range was introduced simultaneously.

The general purpose, 12-bit successive approximation ADC is designated ADC10HT and offers 50 μs, maximum conversion time, no missing codes over temperature, and is 5 V CMOS and TTL compatible. Utilizing laser trimmed, thin film components, the ADC is equipped with an internal clock and voltage reference. Internal scaling resistors are provided for bipolar input voltage ranges of 5 and 10 V and a unipolar input voltage range of 0 to 10 V; a pin for serial output data is provided. The device is packaged in a dual-width, 28-pin, ceramic DIP.

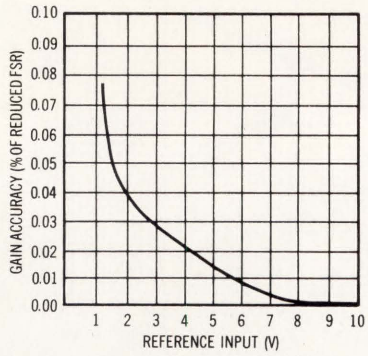
DAC10HT is a general purpose, 12-bit DAC. It is monotonic over temperature and offers a typical settling time of 200 ns. Other performance parameters are a low max gain drift of ±10 ppm/°C and a ±3 ppm/°C max linearity drift over temperature. Special design concepts minimize output glitches. The package is a ceramic 24-pin DIP.

The wideband operational amplifier, designated OPA11HT, is a general purpose device with an input bias current of 30 nA and a typical input offset voltage coefficient of ±5 μV/°C. Typical bandwidth is 12 MHz. Applications include high speed pulse amplifiers, general purpose gain blocks, audio amplifiers, high frequency active filters, and photodiode amplifiers. In addition to its high temperature capability the op amp offers significant advantages in high gain, wide bandwidth, low bias current, high output current, and high common mode rejection. The device is internally compensated for stability at all gains.

OPA12HT is a fast slewing op amp designed for use in circuits requiring fast transient response while operating over temperatures from −55 to 175 °C. Typical specifications are a slew rate of 120 V/μs (80 V/μs, minimum), a settling time of 200 ns, and a gain bandwidth product of 20 MHz. The device is internally compensated to allow fast slewing and wide bandwidths for gains of 3 or more. Applications include very high speed pulse amplifiers, comparators, fast followers, and DACs.

Both op amps are mounted in TO-99 packages with standard 741-type pinouts. In accordance with MIL-STD-883, method 5004, class B, the company screens 100% of both devices with a 200 °C burn-in. Destructive and nondestructive boarding wire pull tests are conducted in accordance with method 2011 of MIL-STD-883.

Circle 464 on Inquiry Card



Gain accuracy vs reference voltage of DAC10HT from Burr-Brown. Output is product of reference input and digital input values. Reference may be ac signal from 0 to 10 V. For highest accuracy the input reference voltage should be as high as possible

EDC Device Detects and Corrects RAM System Errors

A general purpose EDC device can detect and correct errors in random access memory systems. The detection time of the LSI device is 34 ns, worst case, and 25 ns, typical. Correction time is 63 ns, worst case, and 40 ns, typical.

Am2960 EDC, from American Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 95086, will work with any processor, can handle data words from 8- to 64-bits wide, and may be operated in multiple modes to optimize performance or economy. In operation, the EDC generates a set of check bits that are stored with the data bits when a data word is written into memory.

On a read from memory the EDC examines both the data and check bits to determine if the data and check bits are correct, and if they have a single-bit error that can be corrected or a multiple-bit error. If an error is detected, flag outputs go active and may be used to interrupt the processor to stretch the memory cycle. For single-bit errors, the EDC will automatically correct the data which may then be rewritten into memory and sent on to the processor.

The EDC can cut field maintenance costs in two ways. First, since it corrects all single-bit hard errors, a bad RAM will not cause a system crash. The bad RAM can then be replaced at the next regularly scheduled maintenance session. Second, the EDC makes available the error syndromes that indicated which bit is in error. These syndromes can be logged and later examined to determine RAMs that exhibit increasing intermittent error patterns. A preventive maintenance program could then replace these RAMs before they permanently fail.

The Am2960 EDC comes in a 48-pin DIP and requires a single 5-V supply. It will also be available as the Am28160 which is optimized for AmZ8000 designs. Military temperature range parts are also available.

Circle 465 on Inquiry Card

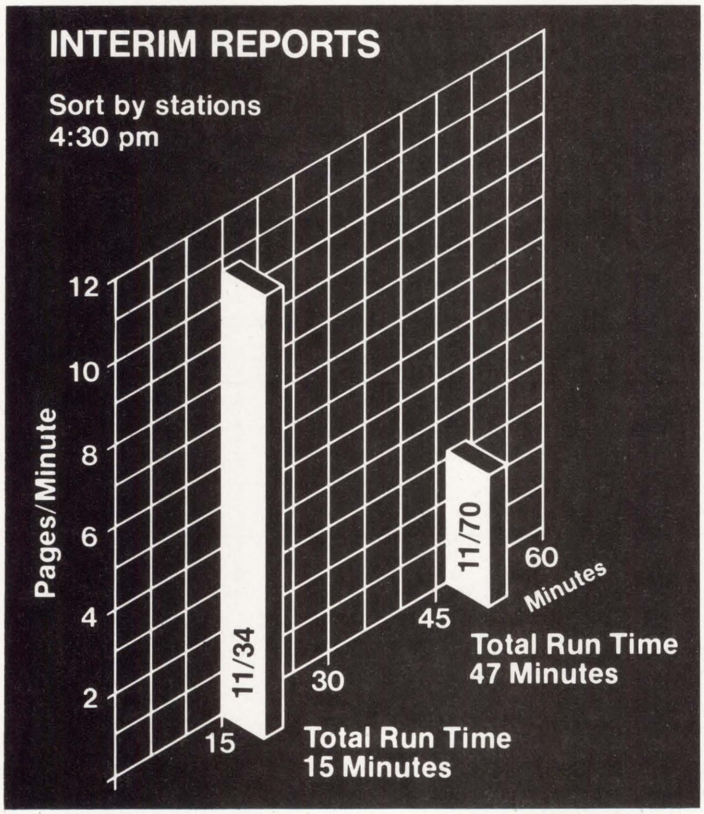
VHSIC Complexity Chip Processed

An initial wafer run of a bipolar very high speed integrated circuit (VHSIC) demonstration chip was completed by Honeywell Inc, Solid State Electronics Center, Honeywell Plaza, Minneapolis, MN 55408. This run indicates that the Department of Defense VHSIC Phase I speed and density goals are feasible. The chip was designed by engineers at the company's Systems and Research Center. Less than 0.6-ns gate delay on the high speed logic family and less than 2 ns on the high density logic family were attained. The latter family is capable of 74,000 gates/cm².

The VHSIC complexity bipolar chip is 5 x 6 mm and contains about 7000 gates; 5000 gates are in a gate array and the balance in a programmable logic array, register stack, and 16-bit shift register latch. Utilizing 1.25 μm feature sizes the chip has a functional throughput greater than the Phase I VHSIC requirement of 5 x 10^{11} gate Hz/cm². The ability to fabricate this chip and get parts of it working represents the first step toward processing up to 10 x 10 mm die sizes using wafer stepping technology.

Circle 466 on Inquiry Card

AMPEX MAKES PDP 11/34 OUTPERFORM PDP 11/70.



That's what happened at San Francisco General Hospital Medical Center. With the addition of Ampex Megastore, processing time was reduced to more than 1/3 the time previously required.

Ed Wong, Manager of Data Processing, was running 4,000 patient tests every day, seven days a week. And he needed help.

Ampex Megastore has been in use over one year for Ed Wong, seven days a week, 24 hours a day, without failure. According to Ed, "We put a lot of time and study into our selection of Megastore, so naturally we're very pleased with the results. Our line printer is now running at maximum rate, 600 LPM. Before it was less than half that. During peak load periods, we have experienced no wait time with our 26 terminals."

Dr. Myron Pollycove, M.D., Director, Clinical Laboratory, added, "We had considerable delays in processing information on the CRT screen, in some cases up to one minute. When you consider the number of inquiries from doctors, that kind of response time is just too slow. Of course, that was before we installed Ampex's Megastore."

With non-volatile storage of from ½ megabytes to 4 megabytes. It's made of core. And it's fast. 3 microseconds, max. And there's no latency. Megastore is transparent to minicomputer software, and requires no program changes. Additionally, it's high reliability improves system uptime and availability.

Megastore. The higher performance alternative to fixed head disks on PDP-11 minis that provides exceptional throughput and reliability.

For more information about how you can put Megastore to work performing for your system, call Cal Goshi at 213/640-0150. Or write him at Ampex Memory Products, 200 N. Nash Street, El Segundo, CA 90245. Ed Wong did.

AMPEX

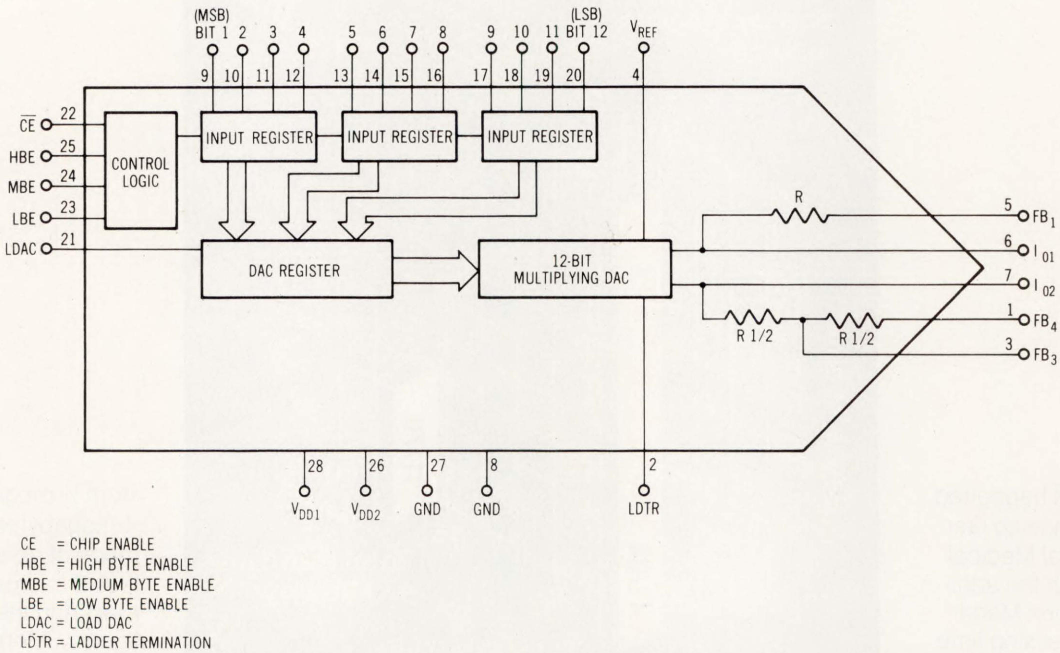
MAKES THE DIFFERENCE.

Double Input Registers on Monolithic 12-Bit DAC Facilitate Bus Addressing

A monolithic 12-bit multiplying DAC with internal, 2-stage input registers for easy interfacing with microprocessor data and address buses was recently announced by Hybrid Systems Corp, Crosby Drive, Bedford Research Pk, Bedford, MA 01730. For extra flexibility, the 12 data inputs are organized into three independent addressable 4-bit input registers. Thus, the HS3120 can be connected to either a 4-, 8-, or 16-bit data bus. A 12-bit parallel DAC register is in series to the input registers for holding the DAC data and the DAC output while the input registers are updated. A separate LDAC command input transfers the input data to the DAC register and the conversion circuitry. All controls are level triggered to allow static and dynamic operation.

The DAC is a single-chip CMOS circuit with a resistor ladder network designed without laser trimming. A total of five output lines are provided to allow unipolar and bipolar output connection with a minimum of external components. The linearity of the HS3120-2 is 0.01% and 0.05% for the HS3120-0. Monotonicity of the HS3120-2 is guaranteed over the entire operating temperature range. Commercial versions will operate from 0 to 70 °C and military versions, processed according to MIL-STD-883 Class B, will operate from −55 to 125 °C. The DAC is packaged in a 20-pin ceramic or plastic DIP.

Circle 467 on Inquiry Card



Functional diagram of HS3120 double-buffered 12-bit DAC from Hybrid Systems. Input registers are sectioned into 3 individually addressable segments of 4 bits each

Two Single-Supply N-Channel JFET Op Amps Offered

Two JFET-input operational amplifier integrated circuits designed for single-power supply low level input signal applications have been announced by Texas Instruments, PO Box 225012, Dallas, TX 75265. Developed by the company in 1980, the INFET process combines N-channel JFETs with bipolar devices on the same chip. Designated TL091 and TL092, the op amps are considered suitable for use with high impedance signal sources such as single-power supply, automotive, telecommunications, and instrumentation systems in which an input signal is near or at ground level (0.5 V or less).

Utilizing the company's NFET technology (patent pending), the TL091 single-op amp and TL092 dual-op amp are functionally identical. Both op amps are identical in function to the TL094 quadruple-op amp announced previously.

With a high input impedance of $10^{12}\ \Omega$, the devices also feature low distortion class A-B outputs. With an input common mode range that includes ground, or V_{CC-}, the devices can be used in applications with input signal levels as low as ground, or V_{CC-}. The band width of the devices is 1 MHz. Slew rate is 1 V/s. Offset current is a low 50 pA, typical. Input bias is 100 pA.

The devices operate with a wide range of supply voltages from either a single- or dual-power supply. With a single-supply, they can operate over a range from 3 to 36 V. They can also operate with a dual supply, provided the difference between the two supplies is 3 to 36 V. Output voltage is from V_{CC-} to V_{CC+} minus 1.5 V.

Circle 468 on Inquiry Card

DILOG INTERFACES DEC 11*...

10 intelligent hard disc and magnetic tape controllers offer LSI-11,* 11/2, 11/23, and PDP-11* single quad slot compatibility with up to 60% power saving.

Only DILOG (Distributed Logic Corporation) exclusive automated design, common proprietary architecture and sophisticated bipolar μPs give you • all single board quad size products requiring no external power or chassis . . . just a cable to connect the drive . . . *you don't need anything else* • high reliability • automated self-test including data base protect feature and indicator. And at cost savings of 50% or more.

LSI-11 MAGNETIC TAPE CONTROLLER, Model DQ 120, interfaces 4 industry standard reel-to-reel drives • emulates TM11* • handles 7 and/or 9 track NRZI drives to 112.5 ips • selectable DEC or IBM byte order formatting • data error checking • RT-11/RSX-11* compatible • extended addressing to 128K words.

LSI-11 MAGNETIC TAPE COUPLER, Model DQ 130, interfaces dual density (NRZI/PE) formatted drives • emulates TM11 • handles up to eight 9 track 800/1600 bpi industry standard drives at speeds from 12.5 to 125 ips • "streamer" mode capability • software or switch selectable density • RT-11/RSX-11 software compatibility.

LSI-11 MASS STORAGE DISC CONTROLLER, Model DQ 200, interfaces any two SMD flat cable interface compatible hard disc drives for up to 500 MB on-line storage • mix or match compatible Winchester, SMD or CMD • variable sector size • automatic media flaw compensation with bad sector flagging • optimized logical to physical unit mapping • implements Winchester fixed head option.

LSI-11 SHUGART SA4000 WINCHESTER DISC CONTROLLER, Model DQ 201, emulates DEC RK* • runs drivers under RT-11 and RSX-11M* systems • compatible with 14.5 MB SA4004 or 29 MB SA4008 drives • automatic media flaw compensation.

LSI-11 DISC CONTROLLER, Model DQ 100, interfaces 2.5, 5, 10 or 20 MB cartridge and fixed platter drives in combinations to 80 MB • RKV-11/RKO5* emulator • handles front load (2315) and/or top load (5440) drives • automatic power fail/power down media protection • RT-11/RSX-11 compatible.

LSI-11 EMULATING MASS STORAGE CONTROLLER, Model DQ 202. Cost effective interface of two 8 and/or 14-inch Winchesters, SMD or CMD hard disc drives without changing controller . . . 8 to 300 MB capacity • RP emulator • automatic media flaw compensation.

PDP-11 MAGNETIC TAPE CONTROLLER, Model DU 120, emulates TM-11 and has same features as Model DQ 120 (LSI unit) • software compatible with RT-11, RSX-11, RSTS, IAS and MUMPS.

PDP-11 MAGNETIC TAPE COUPLER, Model DU 130, offers features of Model DQ 130 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS software compatible.

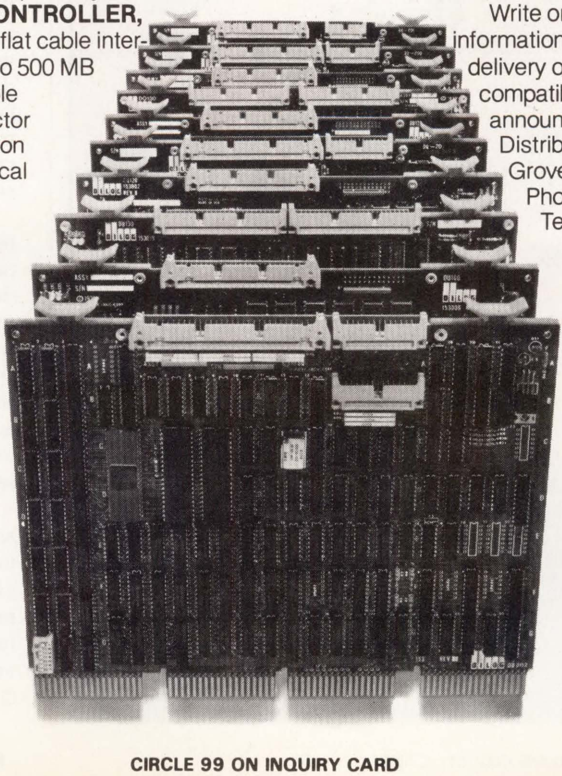
PDP-11 DISC CONTROLLER, Model DU 100 includes features of Model DQ 100 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS compatible • emulates RK-11.

PDP-11 EMULATING MASS STORAGE CONTROLLER, Model DU 202, offers same features as Model DQ 202 (LSI unit).

Write or call for detailed product performance information, OEM quantity pricing, stock to 30 day delivery or warranty data on these DEC 11 compatible products . . . or several soon to be announced new DILOG products.

Distributed Logic Corp., 12800-G Garden Grove Blvd., Garden Grove, CA 92643
Phone (714) 534-8950
Telex: 681399 DILOG GGVE

DISTRIBUTED LOGIC CORP.
DILOG



All DILOG μP Products are Low Power, Quad Size

*Trademark Digital Equipment Corp.

CIRCLE 99 ON INQUIRY CARD

High Speeds Attained In Schottky Bipolar P/ROM Series

Using a TiW technique, Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086, has developed a series of Schottky 1k and 2k bipolar P/ROMs that are claimed to be among the fastest available. They are part of a family of high performance generic P/ROMs that will include Schottky(s) and lower power Schottky (LS) devices. Fabricated with a $PlSi_2$ process, the devices are capable of high speeds over commercial and military operating temperature ranges.

Pin compatible with industry standard NiCr Schottky P/ROMs, these 16-pin high performance TiW Schottky P/ROMs use a programming technique that does not require a separate programming pin as in standard P/ROM fuses. The TiW P/ROMs store logical lows and are programmed to the high state. Special onchip circuitry and extra fuses provide for preprogramming testing to ensure high programming yields and high reliability.

Available in 256- x 4-bit (1k) and 512- x 4-bit (2k) configurations, the high speed Schottky bipolar P/ROMs feature PNP inputs for low input current, full Schottky clamping, and 3-state or open collector outputs. The devices are said to consume the same power (0.65 W) as NiCr fused P/ROMs, but are faster. They are specified at 45 ns commercial and 55 ns military.

High switching speeds make the bipolar P/ROMs suitable for applications such as minicomputers where there is a requirement for realtime signal processing. The company claims that the P/ROMs are fast enough to be used as programmable logic elements in some applications. Other applications include microprogram control storage, microprocessor program storage, lookup tables, character generators, and code converters.

The 1k P/ROM bears the designation 63S140/1 for the commercial device and 53S140/1 for the military version. Commercial 2k P/ROMs are designated 63S240/1 and military devices, 53S240/1.

Circle 469 on Inquiry Card

Linear Array Includes More Than 800 Components

Designated the MOM monochip, a 2.5 x 3.8 mm linear array from Interdesign Inc, 1255 Reamwood Ave, Sunnyvale, CA 94026, includes more than 800 linear components. The linear array operates up to 20 V and has 28 bonding pads. It enables designers to reduce large scale discrete, MSI, or hybrid circuitry to a single linear integrated circuit resulting in lower productions cost, a real estate savings, increased reliability, and improved product security.

In addition to the components traditionally available on the company's linear arrays, the chip has several useful new devices including: four vertical PNPs for use in grounded collector configurations with either input or output stages; four special geometry (low wide band noise) NPN transistors for use in input stages of audio, rf, and instrumentation circuitry; and, five resistor pockets for designs with several power supply voltages.

A kit is available from the company to assist in IC design. Components of the kit include: process technology, component characteristics, breadboard parts, predesigned linear components or digital functional overlays, layout techniques, and test techniques.

Circle 470 on Inquiry Card

64k ROM Is Mask Programmable

A mask programmable 64k ROM was recently announced by Electronic Arrays Inc, 550 East Middlefield Rd, Mountain View, CA 94043. Designated EA8364, the device is organized 8192 words x 8 bits and fabricated with MOS N-channel silicon gate ion-implanted technology and is suitable anywhere a microprocessor is used. The completely static memory operates from a single 5-V power supply with a 10% supply tolerance. Access time is a maximum of 450 ns.

Fully TTL compatible, the product contains a programmable chip select input and 3-state outputs which allow memory expansion to 16,384 words x 8 bits without the use of any external logic. All inputs are protected against static charge.

The ROM is available in molded and ceramic 24-pin dual-inline packages. It is pin compatible with 2716, 2732, and 2564 EPROMs. A single EA8364 can replace four 2716s, two 2732s, or one 2564 EPROM.

Circle 471 on Inquiry Card

Optocoupled Isolator Designed for Isolated Digital Coupling

Designed to provide foolproof operation in applications where isolated digital coupling is required, an optocoupled isolator with Schmitt trigger output was recently announced by General Electric Co, 101 Merritt 7, Norwalk, CT 06856. Compatible with common microprocessor and logic families, H11 utilizes an innovative IC detector design to provide data rates up to 1 MHz.

Device utilizes the company's liquid phase epitaxial GaAs infrared emitting diode and proprietary 6-pin DIP optocoupler construction to provide reliability and longevity. H11L offers isolated I/O capabilities for microprocessors, intermixed logic systems, and interface buses, as well as the ability to handle current loop sensing, power line monitoring, switching power supply control, process control sensor inputs, and pulse restorer circuitry.

Circle 472 on Inquiry Card

LSI Design Service Developed to Speed Turnaround and Reduce Costs

A comprehensive approach to designing and building custom integrated circuits is now offered by Plessey Semiconductors, 1641 Kaiser Ave, Irvine, CA 92714. This service is said to reduce development costs and shorten turnaround time over conventional methods. Developed after two years of internal use, MICROCELL combines a library of NMOS circuit fabrication techniques and advanced CAD capabilities.

Much of the cost and time savings accrue from the use of the library of circuit cells. Using this modular approach eliminates many handpacking procedures required to lay out full custom ICs, since the stored data base of IC layouts is optimized to achieve minimum silicon area. The design service provides the designer with chip complexities up to 1500 gate equivalents, 18-week (and less) turnaround from logic diagrams to prototypes, total design costs from $30,000 to $50,000, and chip areas usually only 10% larger than those achieved by traditional design methods.

More than 30 catalog and custom parts using the design service have been completed by the company and nearly a dozen IC designs are now in progress. The design service library has 22 different cell types, including fundamental NAND and NOR gates, D-flops, I/O buffers, latches, clock drivers, and shift bits. I/O interfaces are compatible with TTL and CMOS logic.

The maximum clock speed at which a MICROCELL circuit can operate depends on the design layout. Unloaded D-flops will toggle at least to 8 MHz. A heavily loaded signal path may limit local operating frequency to 1 MHz. Capacity loading is the limiting factor on circuit speed and is determined by the layout choices of the IC designer. Average gate delays under moderate loading conditions are less than 50 ns, which allows the total circuit system to almost always operate at 2 MHz or faster.

Circle 473 on Inquiry Card

Two High Speed P/ROMs Available

Two high speed bipolar fuse programmable ROMs, a 16k- and an 8k-bit chip, were recently announced by Supertek Inc, 1225 Bordeaux Dr, Sunnyvale, CA 94086.

SM82S190/191-1 is a 16k P/ROM, organized 2048 x 8 with a 35-ns typical access time, 50 ns maximum. The full military version, MM82S190/191-1 is specified to 60 ns. SM82S180/181-1 is an 8k P/ROM organized as 1024 x 8. This device has a typical address access time of 30 ns, 45 ns maximum. Its military version, MM82S180/181-1, has a maximum access time of 55 ns.

Both products are packaged in 24-pin ceramic packages. They are pin for pin compatible with the industry standard, can be programmed by commercially available programmers, and have open collector or 3-state output options.

Circle 474 on Inquiry Card

Z-80 Monitor Implemented in Single EPROM

A recently announced Z-80 monitor allows operators to display, substitute, or fill memory, perform hexadecimal arithmetic, establish two program breakpoints, set and examine registers, assign I/O devices, and input and output from or to an I/O port. Built-in scanning enables the monitor to quickly review the remaining memory capacity and properly set its stack so that the EPROM monitor does not have to be replaced or reprogrammed as users add or subtract RAM memory.

An industry standard I/O vector jump table is included with the new SSM Z-80 monitor from SSM Microcomputer Products, 2190 Paragon Dr, San Jose, CA 95131. Documentation and software listings are provided, and the monitor is compatible with any SSM interface board, video board, or CB2 microcomputer board.

Circle 475 on Inquiry Card

High Speed Parity Generator/Checker Designed for Digital Systems

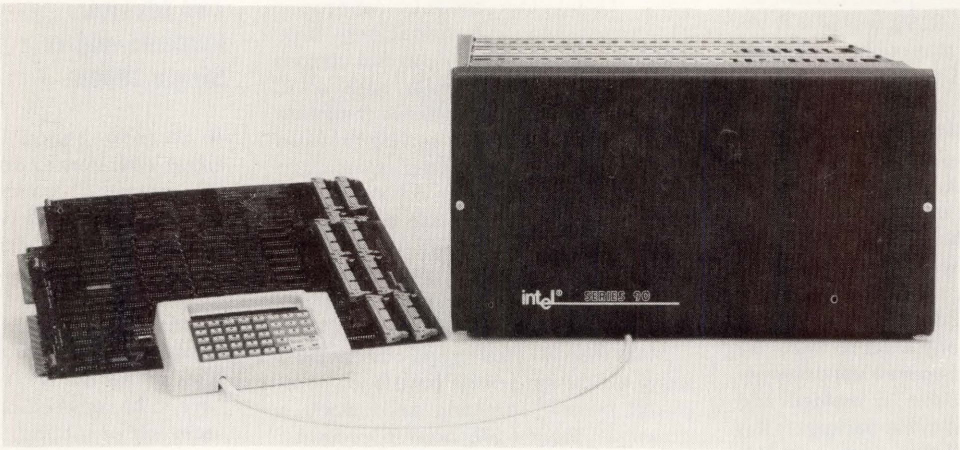
Designed for use in the data path of high performance digital systems, a high speed parity generator/checker is pin for pin compatible with Texas Instruments' 74S280. It has a 9-bit word length and the flexibility needed to carry parity bits in an 8- or 16-bit system.

The device is equipped with control inputs to permit operation with even or odd parity without external logic to simplify system controls. Other key features of the 74S280, from Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086, are its ability to be easily cascaded to n-bits using a ladder network, and its high speed operation. □

Circle 476 on Inquiry Card

PRODUCT FEATURE

Intelligent Memory System Extends System Availability through Fault Tolerant Mechanism



Uninterrupted availability, memory tasking, ECC as well as soft-error scrubbing, onboard diagnostics, and error reporting are offered by Intel's Series 90/iQX memory system. In addition, the 8086 based enhancement to the Series 90 family supplies an integral unit that monitors, reports, and margins up to four power supplies. The module also serves as a communications controller that links the system through a modem to a remote diagnostic site. A handheld maintenance terminal, available as an option, allows operator communication with the system's onboard diagnostics through a set of simple instructions.

Functional Description

Providing up to 16M bytes of memory with cycle times ranging from 250 to 800 ns, depending on the memory module used, the system consists of a Series 90 (see ***Computer Design***, Aug 1979, pp 74, 78) vertical or horizontal mount memory system. The iQX module, located between the user and the BXP™ bus, provides the memory system's intelligence features, such as fault tolerance, diagnostics, and memory tasking. The integral power supply monitor automatically issues a warning if an out of tolerance voltage is detected in any of four power supplies.

The memory system operates in an asynchronous, noninterleaved mode on bidirectional lines performing basic operating cycles—read, write, byte write, read-modify-write, and swap. Refresh operations are user programmed and can be either burst, distributed, or distributed burst. Word widths up to 80 bits plus eight ECC bits can be accommodated.

Error correction circuitry corrects single-bit errors and detects double-bit errors. Soft-error scrubbing circuitry monitors the error detection circuits for single-bit errors. If the errors are transient, it corrects and restores them; if hard errors are found however, they are handled by the memory reallocation mechanism, which automatically redirects memory selection from failed locations to spare memory.

Tasking software resident in the intelligent controller module allows it to perform operations on itself or on data within the memory system. To accomplish this, the message driven interface uses a mailbox protocol. A section of memory set aside for iQX/host communication, the mailbox is used to exchange control information. The host places commands and parameters in the mailbox and activates an alert signal; the module reads the mailbox, executes the command, stores resulting data in the mailbox, and sends a task complete signal. This relieves the host of chores such as moving blocks of memory, filling parts of memory with constants, setting and resetting memory protect, or executing diagnostic programs and reporting results.

The maintenance terminal is a handheld unit which provides a 40-key alphanumeric keyboard for operator communication with the system. A 12-char LED display provides readout of error counts and locations logged during system operation. Approximately 30 commands are available to the operator for use in running onboard diagnostic programs.

System diagnostics can be initiated by the terminal in either on- or offline modes of the host. Onboard diagnostics permit system troubleshooting to be performed without using host time or special test routines on the host.

Specifications

Two chassis configurations are available: a horizontal mount chassis includes up to four memory modules, dc power supplies, and blower assembly; and a vertical mount chassis includes up to 16 memory modules and dc power supplies, but requires a separate blower assembly. System 90/iQX offers up to 16M bytes of high performance dynamic RAM in 128k-, 256k-, 0.5M-, or 1M-byte increments; System 91 provides 16M bytes of high density dynamic RAM in 1M-byte increments, while System 92 supplies up to 4M bytes of static RAM in 32k-, 64k-, 128k-, or 256-byte increments. System 90 has cycle/access times of 650, 500, or 420 ns; System 91 operates at 650 or 800 ns; and System 92 at 250, 290, or 400 ns.

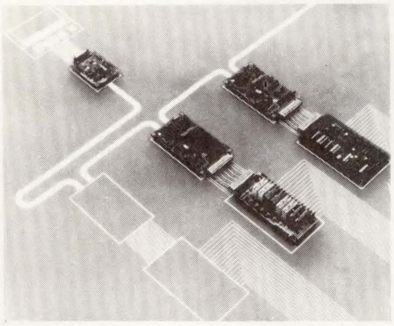
Price and Delivery

Single-unit price for a typical Series 90 with 4M bytes of dynamic RAM with cycle time of 550 ns and intelligent module is approximately $76,610. In a high density VMS chassis configuration with 1024k by 64-bit (8M bytes) of static RAM, the iQX will cost $142,770. OEM discounts are available. Deliveries are 60 to 90 days ARO. Intel Corp, Memory Systems Operation, 1302 N Mathilda Ave, Sunnyvale, CA 94086. Tel: 408/734-8102.

For additional information circle 199 on inquiry card.

Remote Input/Output System Reduces Installed System Costs

RIOS™, a remote I/O system, links almost any mix of remote electrical motors, process and environmental controls, analog signals, alarm and security monitors, and other data and control points at a lower cost than conventional distributed data systems. Employing microprocessor based modules, the system operates either under control of individual remote stations using ROM stored programs, with the RIOS controller issuing all supervisory commands, or under control of a user supplied computer.



Each microprocessor based remote station can accommodate 16 I/O lines. With the maximum 127 stations, more than 2000 data or control points can be monitored. Communication with remote stations is via a bit-serial party line cable using standard asynchronous 11-bit format, at a rate of 9600 baud. Only 3 elements are needed to build a system: a controller/driver, twisted pair cable, and addressable remote interface adapters (RIAs). These microprocessor based adapters serve as station building modules and convert serial cable messages into parallel data for interfacing with ADCs or DACs or with I/O modules which interface with ac and dc power and signal systems. Each RIA contains a 2k-byte ROM to store user defined instructions.

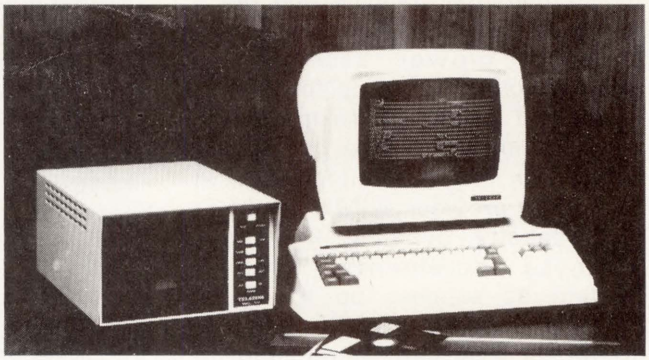
Architecture of the system provides for a manual interface adapter (MIA), a feature not usually found in remote I/O systems. Coupled to a RIOS controller board, the MIA provides manual control or backup through user supplied manual switches and status lights. **Crydom Div, International Rectifier,** 1521 E Grand Ave, El Segundo, CA 90245.

Circle 200 on Inquiry Card

Video Display System Provides Forms Creation and Data Entry Capability

Replacing printed forms with video displayed forms and miniature storage diskettes, Teleform consists of ASCII video terminal, Teledisk, and optional printer. Terminal keyboard is similar to that of an office typewriter with the addition of special keys dedicated to the forms system. Each 5.25" (13.33-cm) diskette stores the displayed form and data entered into the form. For hardcopy printout of the form and data or just data on a preprinted form, a printer may be optionally connected. Most serial printers with speeds from 10 to 960 char/s are acceptable.

Intended for use either as a standalone unit or with a host computer system, the system has an editing terminal with capability of inserting and deleting characters or lines. Screen capacity is 1920 char; storage is provided for 529 char. The block mode terminal is capable of transmitting lines, messages, or full pages of text. A communications port on the terminal provides interface to the computer. The disc unit includes a port for printer interface; this port allows use of line control and baud rate independent of I/O band. **Teleray Div, Research Inc,** PO Box 24064, Minneapolis, MN 55424.



Circle 201 on Inquiry Card

Low Cost CRT Models Offer Block Mode/Editing and Numeric/Cursor Pad

Models 550S and 550E offer editing capabilities and numeric/cursor pad, respectively, in the low cost Bantam CRT family. The microprocessor based 550S provides three modes optimized for conversational timesharing, transaction processing, and text manipulation or software development, and extensive features to suit each.

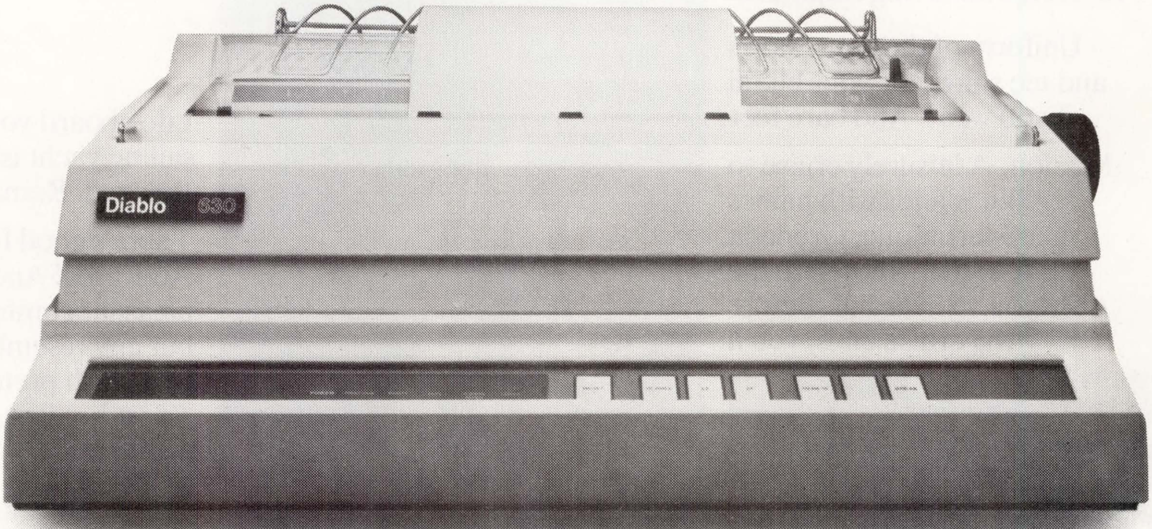
Standard unit has an 83-key keyboard that includes multifunction numeric pad and 4 programmable function keys. An ASCII serial printer port is provided, as well as XON/XOFF host control over terminal block transmissions and field attributes. The 24-line screen acts as a movable window into 48 lines of 80 characters stored in memory; an optional second page of fully scrolling memory can be called automatically in transaction processing mode.

Model 550E, driven by an LSI chip and 19 ICs, offers a dedicated keypad for numeric entry and cursor movement. The unit's 12" (30-cm) diagonal screen comes standard with P4 (white) phosphor; green or amber are optional. It displays 24 lines of 80 characters using a 7 x 10 matrix. Character sets include U.S., U.K., Danish/Norwegian, French, German, Spanish, and Swedish. An RS-232-C/CCITT-V.24 communications interface is standard; 20-mA current loop implemented in an external adapter is optional.

To connect a printer, the terminal offers an optional wye type printer port and control switch. The port drives most ASCII serial printers. **Perkin-Elmer, Terminals Div,** 360 Rte 206, Flanders, NJ 07836.

Circle 202 on Inquiry Card

If you want a choice in print wheels, there's only one choice in printers.



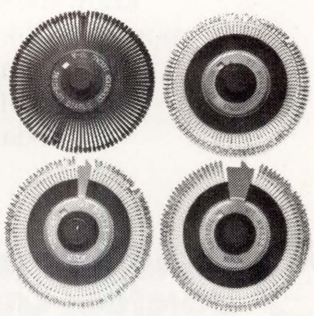
The Diablo 630.

It's the only one that lets your customers use either metal or plastic print wheels. Which means they can choose the print wheel that's just right for the job.

The 630 works as well with a 96-character plastic daisy print wheel as it does with an 88-, 92-, or 96-character metal daisy print wheel. In over 100 different type styles.

Every 630 has a fully strappable power supply. It's as easy to use in Paris, Kentucky as it is in Paris, France. So you only need to stock one printer for international and domestic markets.

It has fewer moving parts than competitive printers, which makes it more reliable. And it offers unsurpassed print quality. Compatibility with Diablo supplies. And bi-directional printing capability.



The 630 is the only printer in the world that uses both metal and plastic wheels.

Once your customers hear they can change their print wheels, they're going to be changing their printers.

To Diablo 630 printers.

Diablo Systems

XEROX

GET A CLEAR HONEST IMAGE THE HITACHI WAY!

Computer data and graphic displays never looked better, brighter, sharper.

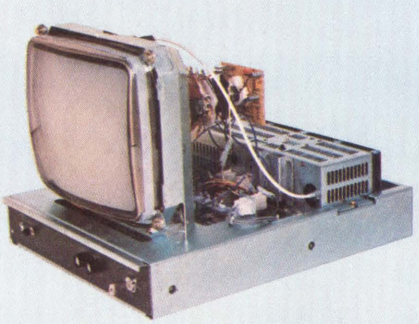
New Hitachi high resolution in-line RGB color monitors utilize wide video bandwidth and a 0.31 mm spacing between triad pairs. The result? A trio-dot density **twice that of conventional monitors!**

Look at these advanced features

Adjustment-free convergence, single PCB configuration, video amplifier bandwidth from 50 Hz to 25 MHz. Flexible frequencies range from 15 to 18 KHz horizontal and 50 to 60 Hz vertical. Monitors provide high contrast and brightness from black matrix and 85% light transmission tubes. Can any other maker match these advantages?

Variety of Screens

You can select from a wide choice of screens to meet your specific application needs: Normal phosphor; long persistence phosphor to virtually eliminate flickering, or medium resolution versions for most ambient light situations.



Unsurpassed performance

Long time convergence stability is assured due to self convergent in-line guns and **single PCB reliability.** Operator controls include power on/off, degauss, brightness, contrast.

Call or write for more information.

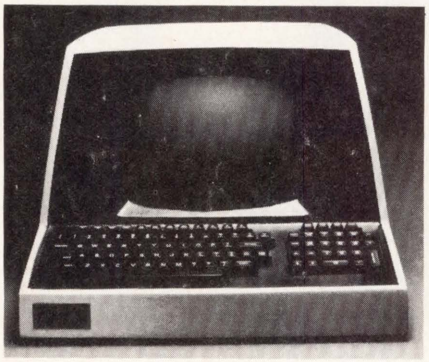
Hitachi America, Ltd. 100 California Street, San Francisco, Calif. 94111 Tel: (415) 981-7871

Crown Electronics, Tualatin, OR (503) 638-7561; **Quadrep, Inc.,** San Jose, CA (408) 946-4000; **Bestronics, Inc.,** Culver City, CA (213) 870-9191, Irvine, CA (714) 979-9910, San Diego, CA (714) 452-5500; **Comstrand, Inc.,** Minneapolis, MN (612) 788-9234; **Sumer, Inc.,** Rolling Meadows, IL (312) 991-8500, Brookfield, WI (414) 784-6641; **Bear Marketing,** Richfield, OH (216) 659-3131; **Robert Electronic Sales,** Catonsville, MD (301) 788-2380, Lansdale, PA (215) 855-3962, Richmond, VA (804) 276-3979; **Technology Sales, Inc.,** Lexington, MA (617) 862-1306.

CIRCLE 105 ON INQUIRY CARD

DATA TERMINALS

SMART CRT TERMINAL



IQ 135 features 14 user programmable function keys that increase operator efficiency by giving the operator a choice of 14 separate functions with a single keystroke. Users can custom fit the unit to specific requirements using programmable transmission delimiters, print delimiters, keyboard repeat rate, and lead in code; adjustable right hand margin; and programmable blink rate. A range of built-in edit commands requires no additional user programming. Other features include easy to use transmission and print commands, data rates from 110 to 19,200 baud, tab and clear functions, video functions for operator convenience, and cursor control. Absolute cursor positioning enables the operator to position the cursor anywhere on the screen by keying in the X and Y coordinates. **Soroc Technology, Inc,** 165 Freedom Ave, Anaheim, CA 92801.
Circle 203 on Inquiry Card

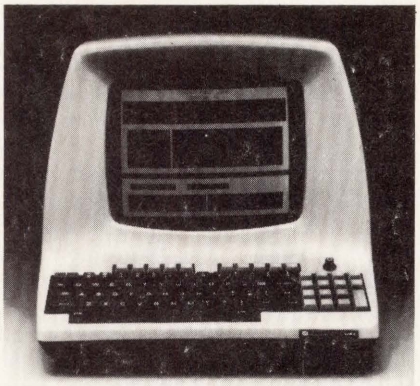
PORTABLE DATA ENTRY TERMINAL

Alphanumeric display, with English language prompts for numerical data entry applications, is provided by user programmable MSI/88e terminal. Compatible with the company's portable terminal accessories, including wand scanners, and terminal communications protocols, including full 2-way communications and downline loading of programs, terminal provides 16-digit, 14-segment LED display. A realtime clock is available as an option. **MSI Data Corp,** 340 Fischer Ave, Costa Mesa, CA 92626.
Circle 204 on Inquiry Card

USER PROGRAMMABLE INTELLIGENT TERMINAL

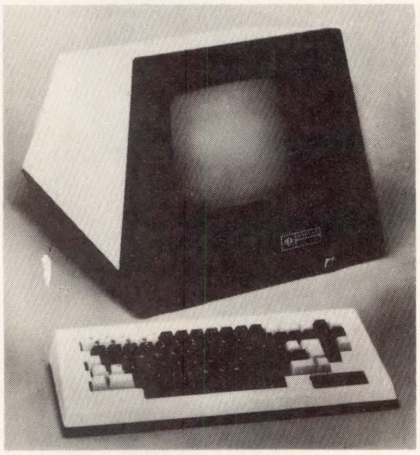
Display 8 single-board, LSI technology, Z-80A based CRT terminal is designed for use as a smart inquiry/response device or as a user programmable terminal in a distributed processing network. Numerous memory configurations are provided. The 12" (30.5-cm) CRT displays 25 lines of 80 chars. 128-char display character set and 96-position detachable keyboard are std. Two serial I/O ports allow communications via various protocols or interface to such peripherals as printers, floppy discs, OCR, or badge readers. S100 bus adapter is available. **Computek, Inc,** 63 Second Ave, Burlington, MA 01803.
Circle 205 on Inquiry Card

CONVERSATIONAL VIDEO DISPLAY TERMINAL



The ADM-5 Dumb Terminal console provides visual attributes—reverse video, reduced intensity, and reverse video/reduced intensity—limited editing capabilities, and a gated extension port for selective transmission of data from terminal to serial RS-232-C peripheral device. Editing capabilities enable operator to erase to end of line or to end of page, providing operator convenience for high volume data entry operations by eliminating trailing characters and lines. Characters are displayed as a 5 x 9 dot matrix in a 7 x 10 field. The unit has a 12" (30-cm) diagonal display screen and teletypewriter keyboard. Up to 1920 char can be displayed in 80-char by 24-line format. Terminal operates asynchronously in half- or full-duplex modes at any of 11 data rates from 75 to 19.2k bits/s. **Lear Siegler, Inc, Data Products Div,** 714 N Brookhurst St, Anaheim, CA 92803.
Circle 206 on Inquiry Card

VIDEO DISPLAY TERMINALS



Series 630 Data Screen[R] incorporates features that make it more adaptable to human interface requirements. Detached keyboard as a typewriter layout with 79 keys, typamatic (autorepeating) after 0.75 s, and 6 function keys capable of generating 16 2-char code sequences. The 12" (30-cm) diagonal screen has a P4 phosphor nonglare (antireflect) display. It displays 25 lines of 80 characters formed in a 6 x 8 dot matrix (in an 8 x 10 field): P31 type, green nonglare (antireflect) display, and PC 124 type, yellow nonglare (antireflect) display are also available. Switch-selectable features include 8 data transfer rates from 110 through 9600 baud. **TEC, Inc**, 2727 N Fairview Ave, Tucson, AZ 85705.

Circle 207 on Inquiry Card

DATA TERMINAL OPTIONS

Wand type bar code reader reads CODE 39, 2 out of 5, and UPC/EAN for input to terminal. Magnetic stripe reader allows terminal to accept ANSI and ISO magnetic badges. Auxiliary IEEE-488 (HP-IB) interface connects up to 14 peripherals and operates at 110 to 9600 baud. RS-232-C/CCITT V.24 port has 16-line, 32-char capacity. Extended display capabilities offer page having 16 lines of 32 char, and large character page for visibility from a distance. **Hewlett-Packard Co**, 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 208 on Inquiry Card

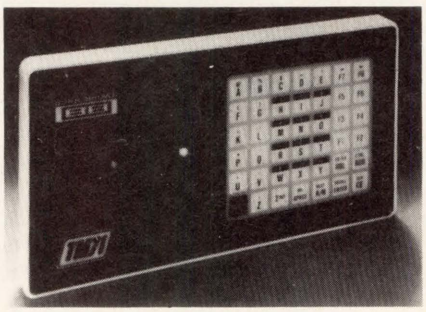
PORTABLE CRT TERMINALS

Portable data terminals Ambassador III and IV incorporate 7" (17.8-cm) diag CRT screens with 24-line by 80-char displays using ASCII 128-char set. Mosel III has integral 300-baud acoustic coupler; model IV has 80-col electric discharge 2-line/s printer. Both work in page and character mode and transmit in 7- or 8-level code at selectable rates from 110 to 9600 baud. Units weigh less than 20 lb (9.1 kg) and fit easily under airline seat. **Telcon Industries, Inc**, 1401 NW 69th St, Fort Lauderdale, FL 33309.

Circle 209 on Inquiry Card

ALPHANUMERIC DATA ENTRY TERMINAL

TM71, with full alphanumeric capability, offers simplified man/machine interface for applications where communications are distributed and complex, but limited in size, and in harsh operating environments. The compact, waterproof 8.5 x 4.5 x 0.6" (21.6 x 11.4 x 1.5 cm) unit has a 42-key keyboard and permits entry of messages up to 80 char long. A 16-char LED display, with scroll left/scroll right keyboard controls, permits review and editing of data entered before transmission. In edit mode, operators can backspace and advance cursor position and insert and delete characters. Two 80-char buffers are provided for keyboard generated data and two 80-char buffers available for CPU generated messages. Display features include CPU control of flashing, scrolling, or blanking. **Burr-Brown, Industrial Systems Products Div**, PO Box 11400, Tucson, AZ 85734.



Circle 210 on Inquiry Card

80/132-COL CRT TERMINAL

With video and editing functions including regional smooth scrolling, split screen, and double-high/double-wide characters, the DT80/3 offers features of DEC's VT100, but is designed for use in nonDEC operating system environments. The 80/132-col terminal also emulates 4 low cost terminals, allowing users to upgrade without investing in new software. The terminal allows users to select either 80- or 132-col display. Attached to the terminal by a coiled cable, the keyboard can be positioned up to 6' (1.8 m) away. Keyboard can be electronically disabled and the screen can be read one character at a time. Host computer has use of field tab. The unit interfaces with host computer via std EIA RS-232-C/CCITT V.24 or optional 20-mA current loop interface. **Datamedia Corp**, 7401 Central Hwy, Pennsauken, NJ 08110.

Circle 211 on Inquiry Card

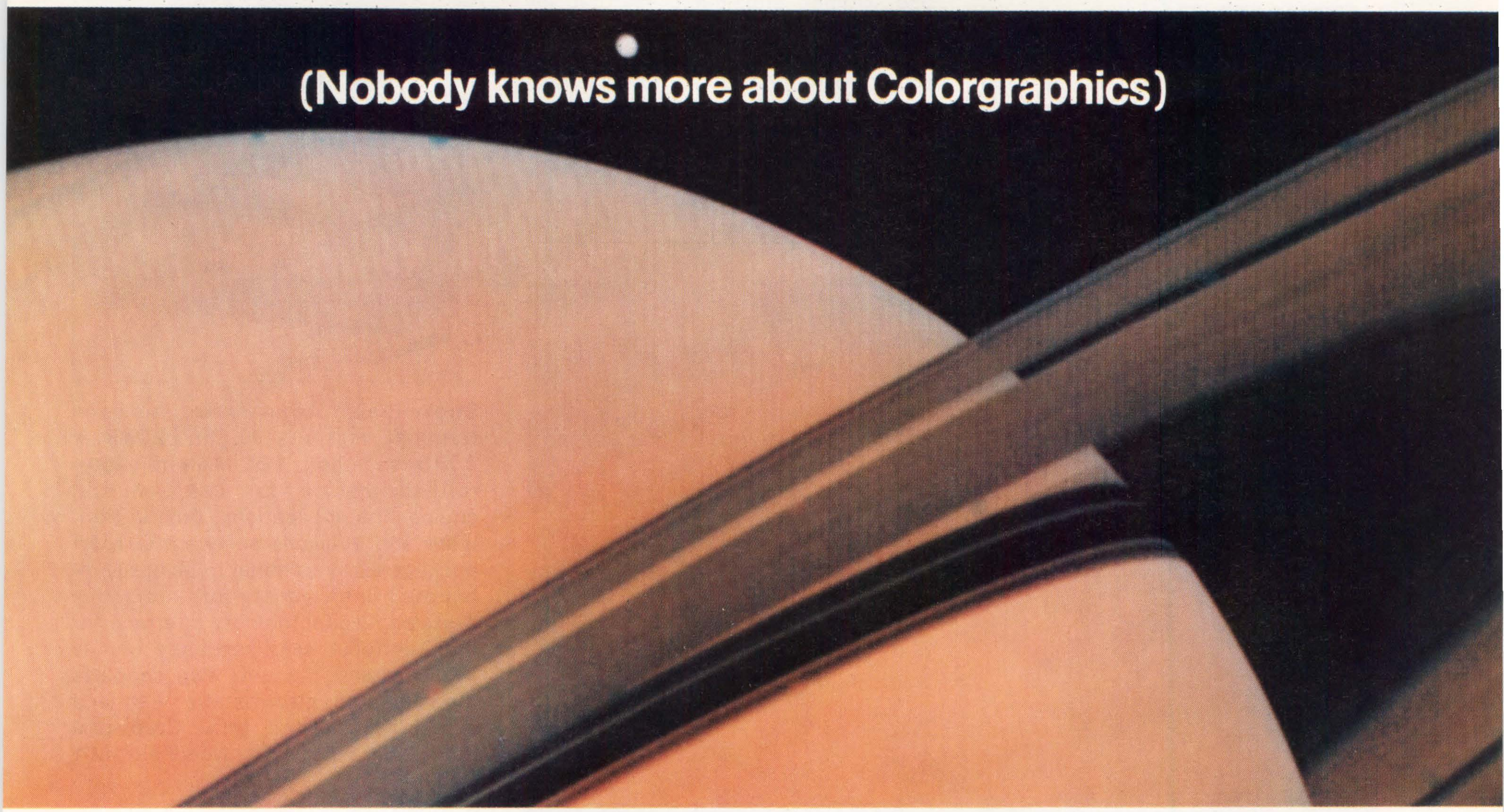
COLOR GRAPHICS TERMINAL

Intelligent 5217CT character graphic color terminal consists of keyboard/display controller and 13" (33-cm) dia high resolution inline gun RGB monitor. It can produce 256 alphanumeric and special graphic symbols. The device can be used as a remote terminal and color display generator, or can optionally be configured as a standalone terminal. When used with optional floppy disc controller and DOS software it can function as standalone programmable microcomputer system with color display. **Aydin Controls**, 414 Commerce Dr, Fort Washington, PA 19034.

Circle 212 on Inquiry Card

Ask Ramtek.

(Nobody knows more about Colorgraphics)



Get the most out of your computer graphics with a monitor from Ramtek.

Choose the right monitor for you from our complete line of more than forty models—13 to 25 inches, color or monochrome, cabinet or rackmount.

The 800 Series: Highest resolution ever in a raster CRT. Ramtek's 800 Series color and monochrome monitors bring the advantages of raster scan to even the most sophisticated display system. Sold exclusively by Ramtek, these monitors address a 1280 X 1024 picture element (pixel) matrix.

The 700 Series: High performance at a lower price. For users who don't require 1000-line resolution, Ramtek has the 700 Series with 640 X 512 addressable pixels. The Model 714 uses the latest in-line color gun technology to achieve cost-effective color displays.

From the company that pioneered raster color graphics. Our monitors display the same high quality and performance that have made Ramtek the world's largest independent manufacturer of raster scan computer graphics and imaging systems. From our most sophisticated 9400 Series to the 6212 interactive terminal, Ramtek has lead the way with colorgraphic systems for CAD/CAM, process control, management information, medical imaging, command and control and computer simulation.

Why a high performance monitor? Computer graphics users are demanding more resolution, color and performance. To find out how to compare the difference in high-performance monitors, write on your company's letterhead to Ramtek, 2211 Lawson Lane, Santa Clara, CA 95050 and request "High Performance Monitors for Computer Graphics and Imaging." It's Issue Number 4 of Ramtek's "USE OUR EXPERIENCE" series.

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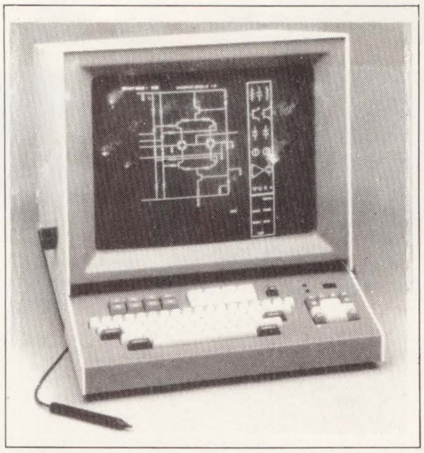
CIRCLE 107 ON INQUIRY CARD

SYSTEM/34 AND /38 COMPATIBLE CRT DISPLAY

CRT display station 3751-11 is plug compatible with IBM System/34 and /38. It has a 24-line by 80-char display with a 25th line for expanded error message and cursor position display. Moveable typewriter-style keyboard includes a field convertible numeric pad. Human engineered features include adjustable keyboard clicker/alarm, document holder, tiltable screen, palm rest, and automatic dimming. **Decision Data Computer Corp**, 100 Witmer Rd, Horsham, PA 19044.

Circle 257 on Inquiry Card

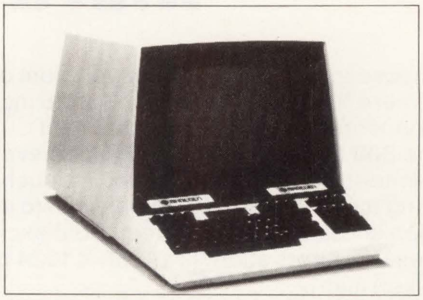
INTERACTIVE INTELLIGENT GRAPHICS TERMINAL



Stroke-drawn DYNAGRAPHIC series II terminal features bright, 2048 x 2048 resolution, 19" (48-cm) vector refresh display for CAD/CAM and engineering applications. Built-in firmware and available software support package allow terminal to be easily integrated into variety of interactive systems. Digital memory interface for the Tektronix 4631 hardcopy unit is available and the unit also supports the Versatec electrostatic V-80 and compatible plotters. **IMLAC Corp, OEM Marketing**, 150 A St, Needham, MA 02194.

Circle 258 on Inquiry Card

DEC COMPATIBLE INTELLIGENT TERMINAL



BT-100, a high resolution, 12" (30-cm) CRT with attached keyboard, features complete DEC VT-100 emulation, video package, and printer port. Double-size, dual-density, and reverse video characters; user selectable 80/132-char/line; split screen and smooth scrolling; blinking and underlining; composite video output; fixed and settable tabs; line drawing and graphics characters; and full-duplex, asynchronous communications line are also provided. Transmission speeds are up to 19,200 baud. **The Braegen Corp**, 3340 E La Palma Ave, Anaheim, CA 92806.

Circle 259 on Inquiry Card

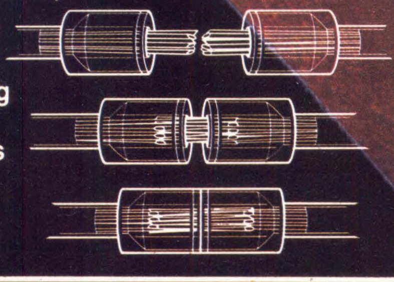
The state-of-the-art in PC design...

Bendix Low Mating Force Brush Connectors

Low mating force, bristle brush connectors by Bendix! They've advanced PC design to a new state-of-the-art!

A connector that's *dependable* (stable contact resistance), *durable* (up to 20,000 mates/unmates), *flexible* (20 - 400 contacts per connector), and *smooth* (mating force reduced by 70 - 90%)!

The brush "wiping" action of gold-plated wire bristles, meshing at highly redundant contact sites, creates multiple electrical paths, and intimate, gas-tight connection.



A masterpiece of simplicity. Available in a broad variety of connector/termination formats.

- compatible with High Speed Digital Switching
- greater board effectiveness by allowing more circuits per board
- stable electrical performance
- less need for exterior board supports
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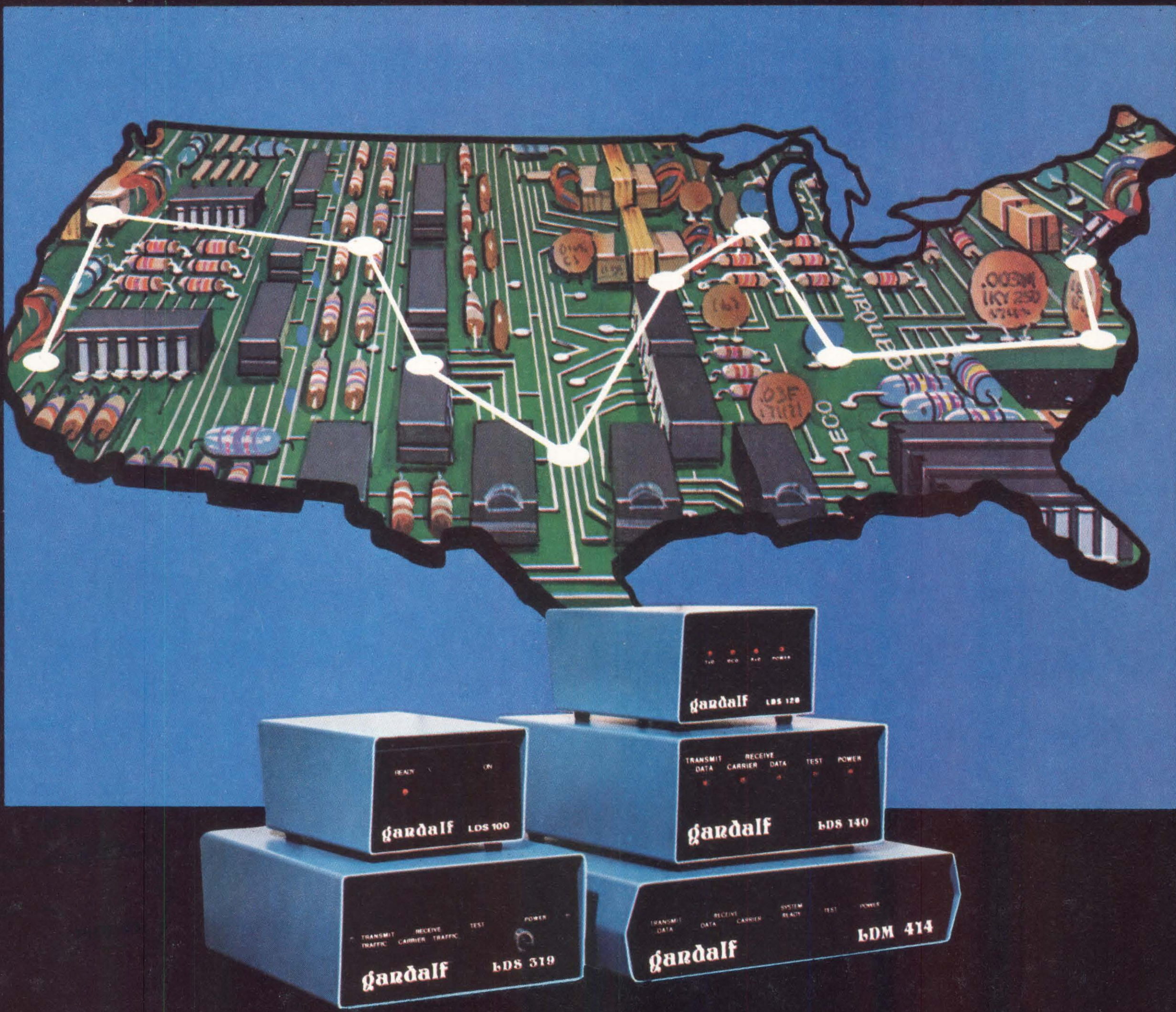
That's the "broad brush" picture on our brush connectors. Get all the fine details in our new brochure, *LOW MATING FORCE.* Call 607 563-5302, or write The Bendix Corporation, Electrical Components Division, Sidney, New York 13838.

We speak connectors. Bendix

CIRCLE 109 ON INQUIRY CARD

It's Gandalf Country!



gandalf "bridges the gap" in cross country communications

Whatever your communication needs, 200 feet or 2000 miles, Gandalf has a modem to *"bridge the gap"*. Gandalf engineers a broad line of data communication equipment, with synchronous and asynchronous transmissions. Their common characteristic is quality . . . uncompromising quality . . . insuring you of continuous, on-line reliability and cost effective performance.

The asynchronous line (LDS 100, LDS 120, LDS 140, LDS 319, and LDM 414 pictured) include short to limited distance units, with speeds up to 9600 bps. This complete line has won nationwide acceptance averaging 87,000 hours MTBF. Rack mounted or stand alone versions are available and are easy to install. Gandalf data sets conform to A.T. & T. pub. 41004 and 43401. Interface meets EIA RS232C and CCITT V.24 requirements.

It's Gandalf Country

In relatively a few short years, Gandalf has become one of the most highly regarded growth companies in data communications.

We have the technology for efficiency of operation, backed by unparalleled service, assuring you of better communications and increased profits.

Let a Gandalf trained sales representative give you more detailed information on how to *"bridge the gap"* in your specific application.

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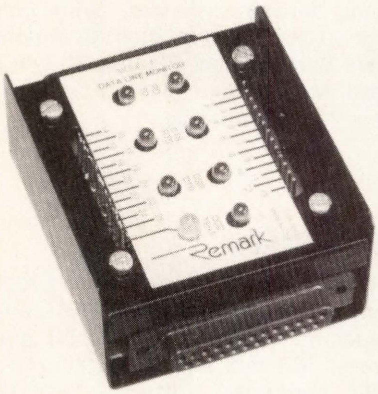
Gandalf Data Communications Ltd., Gandalf Plaza, 9 Slack Road, Ottawa, Ontario, Canada K2G 0B7 Tel: (613) 225-0565
Gandalf Digital Communications Ltd., 4 Cranford Court, Hardwick Grange, Warrington, Cheshire, England Tel: 09-2581-7755

CIRCLE 110 ON INQUIRY CARD

DATA COMMUNICATIONS

LINE POWERED DATA LINK MONITOR



Model 41 monitor can determine if analyzed signal is MARK (-3 to -25 V), SPACE (3 to 25 V), or invalid (between 3 and -3 V)) by incorporating current limiting circuitry and a bipolar LED in TEST position. Red insignals above 3 V, green those below -3 V, and OFF indicates an invalid signal. Seven dedicated LEDs display TD, RD, RTS, CTS, DSR, DCD, and DTR. Housed in a 3 x 2.5 x 1.5" (7.6 x 6.4 x 3.8-cm) aluminum case, device derives its power from signals under test. **Remark International**, 4 Sycamore Dr, Woodbury, NY 11797.

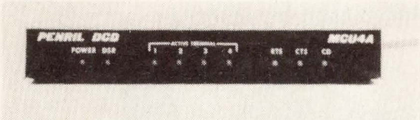
Circle 213 on Inquiry Card

MULTIFUNCTION MODEM MODULES

Mounting singly or in any combination on PCBs or any flat surface in computers or terminals, 7 modules implemented with LSI chips include 300-baud modem, CCITT 300-baud modem, phone line interface, 1200-baud module, view data module, 1200- or 300-baud selectable module, and deaf modem module. Modules can communicate with a variety of networks. Plastic container provides protection during installation or replacement. **Novation, Inc**, 18644 Oxnard St, Tarzana, CA 91356.

Circle 214 on Inquiry Card

4-CHANNEL MODEM CONTENTION UNIT



Useful in systems where terminals are colocated, operated in contention, and where simultaneous transmission of data to or from one or more terminals is not required, MCU-4A channel contention unit replaces costly MUXs and split stream modems. It allows a single modem to be shared by up to four colocated terminals on a first come, first served basis, and can be used with all company or equivalent modems in private line or dial networks. Tandem connection enables one modem to service 7, 10, 13, etc, terminals. **Penril Corp, Data Communications Div,** 5520 Randolph Rd, Rockville, MD 20852

Circle 215 on Inquiry Card

MICROCOMPUTER CONTROLLED MODEM

Models 1030 and 1031 offer capabilities increased over those of ordinary modems. 1030 combines low error rate modem with automatic calling unit (ACU) and custom BIZ-080 microcomputer into a compact FCC registered unit with auto-answer, auto-dial, and auto-repeat dial features. Code multiplexed design allows intelligent modem control using the same terminal as that for data communication. For computer sites, code multiplexing also enables communications software to be written in high level languages such as BASIC or COBOL, speeding development time. Interfacing to RS-232 equipped computers, terminals, and word processors requires only a 3-wire data cable. Command selectable dial pulse or tone dialing, and self-test are added by the 1031. Tone dialing capability adapts it for use as a CPT-TWX network interface. Both models feature automatic baud rate acquisition and communications rates of 110, 134.5, 150, 200, or 300 baud. **Bizcomp Corp**, PO Box 7498, Menlo Park, CA 94025.

Circle 216 on Inquiry Card

MEMORIES

UNIVERSAL P/ROM PROGRAMMING MODULE

PM2000-2 Multi Module, for use with PPX and PP17 universal programmer mainframes, enables users to program over 300 individual P/ROM types. Selection of bipolar P/ROM, EPROM, CMOS P/ROM, or EEPROM is achieved by means of thumbswitch on the module and 6 separate socket adapter modules, which allow the use of dual-master, slave sockets to eliminate accidental reprogramming of master devices. The unit provides an Empty Check to verify correct erasure of UV, and can be used with the PP17 P/ROM production copier without need for keyboard entry. Separate socket adapters provide master device protection, longer module life, and greater reliability. **Stag Systems Inc**, Palo Alto Industrial Pk, 1120 San Antonio Rd, Palo Alto, CA 94303.

Circle 217 on Inquiry Card

5.25" FLOPPY DISC CONTROLLER

For use with FD-50 series drives, IBM sector format compatible FC-50 controller accommodates single- or double-sided drives, and can read, write, and format single- or double-density discs. Up to 4 drives can be connected in daisy chain configuration. Features include direct mounting to drive frame, LSI microprocessor technology, and DMA or program control transfer of data. **TEAC Corp of America**, 7733 Telegraph Rd, Montebello, CA 90640.

Circle 218 on Inquiry Card

CARTRIDGE DISC BACKUP SYSTEM

CDBS software package, developed for Data General's family of microNOVA, NOVA, and ECLIPSE processors using either 10M- or 20M-byte cartridge disc subsystems, ensures integrity of system's disc resident data base. It eliminates common problems associated with backing up cartridge discs containing fixed and removable platters. The CDBS package is available on 800-bit/in (315-bit/cm) tape or single-density diskettes, with complete user documentation. **Concentric Data Systems Inc**, PO Box 363, Harvard, MA 01451.

Circle 219 on Inquiry Card

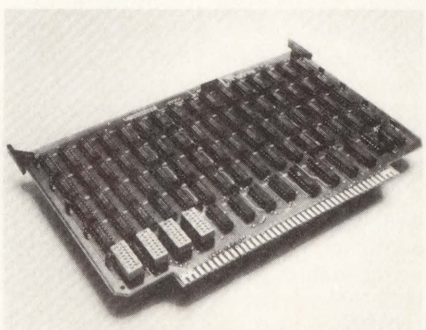
ADD-IN MEMORY

Add-in memory for the VAX-11/780™ computer, SM256 has 256k-byte capacity organized as 32,768 quad words (64 bits plus 8 bits ECC). It is fully hardware, software, and ECC compatible with the DEC M8210™ module and is optionally available with sockets for the memory ICs. Installation is simple plug-in, with no configuration requirements. **Shell Computer Systems, Inc**, PO Box 36, Waban, MA 02168.

Circle 220 on Inquiry Card

32k STATIC RAM MODULE

9629 is configured as four 8k-byte blocks, each of which can be selected by an onboard switch to operate at any 8k boundary. 6800/6809 compatible module operates from a 5-Vdc supply, and requires approx 2.0 A. Maximum access time is 450 ns; version 9629A provides max access time of 200 ns. Partially populated versions of the modules that permit system memory expansion are available for use in smaller systems. **Creative Micro Systems**, 11642-8 Knott St, Garden Grove, CA 92641.



Circle 221 on Inquiry Card

TELEX GCR: STANDS OUT...AND FITS IN.

Outstanding field-proven subsystems to fit your high-performance needs.

TELEX GCR Tape Subsystems *stand out* as the most proven, high performance rack-mountable GCR units available today. Field proven in demanding seismic operation. Compatibility proven in IBM plug-compatible applications. Versatility proven in superminicomputer environments.

Enhance your high performance computing system with high performance peripherals. Select the TELEX 6200 family. Available in 6253 (6250/1600/800 bpi), 6250 (6250/1600 bpi) and 6240 (1600/800 bpi) tape drives and tri-density 6850 formatters. Tape speeds of 50, 75 and 125-IPS available.

TELEX GCR subsystems *fit in* with your high performance computer system. Already interfaced to sixteen different CPU's. TELEX Engineering assisted with these interface developments to provide reliable operation and customized features. And we stand ready to assist you in making TELEX subsystems fit into your computer system.

With more than 2,000 units shipped — a majority for high-speed 125-IPS operation and a large number with tri-density capability — TELEX GCR offers field maturity, versatility, and integratability.

For more information, contact the nearest TELEX OEM Sales Office listed below or phone our OEM Marketing Department in Tulsa at (918) 627-1111.

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CIRCLE 113 ON INQUIRY CARD

Smart screen size: 15"

15-inch display heads the Executive 80™ list of smart ergonomic features.

When you look at the business end of a terminal, you expect to see a clear, crisp display. That's exactly what you'll see on the Executive 80™ standard 15-inch display. Executive 80 gives you a viewing area that's 25% larger than the competition's 12-inch screens — at no extra cost. Since a larger screen is easier to read, you can expect increased throughput, fewer errors, and greater comfort for your operators.

Hazeltine's attention to ergonomic detail doesn't stop with the larger screen. You can order the tiltable screen with detached keyboard for greater operator convenience. And the *Enhanced Video Option* features smooth scroll, selectable double-size characters, and switching between 80- or 132-column format from the keyboard.

Put Executive 80's big screen to the test. You'll agree it's the smart way to look at data.

Call today and we'll send you additional literature and pricing information. Call toll-free (800) 645-5300 — in New York State call collect (212) 752-3377.

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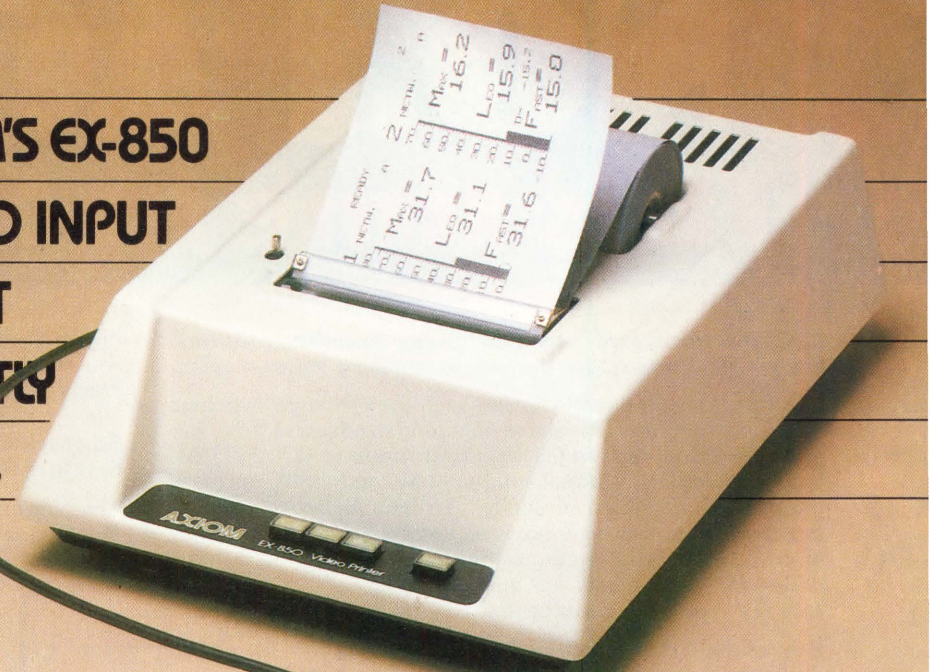
CIRCLE 114 ON INQUIRY CARD

JUST CONNECT AXIOM'S EX-850 PRINTER TO THE VIDEO INPUT OF VIRTUALLY ANY CRT DISPLAY AND INSTANTLY PRINT WHAT YOU SEE.



The Video Un-Interface

Imagine, instant hard copy of anything displayed on the CRT of your graphics terminal, video monitor or TV set... with absolutely no hardware or software interface.

And we mean anything — complex graphics, alphanumerics in any size or font, foreign symbols and hieroglyphics — whatever is on the screen.

That's because this amazingly simple printer operates from the composite video input of the CRT display. Just connect two wires and start printing.

IBM, Tektronix... You Name It

Nowhere will you find a printer that does what the $1495 EX-850 does. For example, it provides hard copy for many Tektronix graphic terminals at about 1/4 the cost of competitive printers. And the EX-850 plugs directly into the coax connector on IBM's 3270. You name it, the EX-850 will print it.

For Banks, Insurance Companies, and Others — The Electronic Notebook

The compact EX-850 is the ideal companion for CRT terminals in banks, insurance companies and a multitude of other businesses. It provides low cost hard copy at a teller's window, an executive's desk, or on the production line floor. At $1495 (less in quantity) you can afford to equip every terminal with an EX-850 VideoPrinter.

A Complete Graphics Printer

No stripped-down model, the EX-850 is a complete stand-alone printer including case, power supply, video printer controller, low paper detector, bell and paper roll holder. Maintenance is minimal, too. The printhead is self-adjusting and there are no inky ribbons to change. And every Axiom printer is backed by our nationwide distribution and service centers in the USA and 18 foreign countries.

AXIOM

AXIOM CORPORATION

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CIRCLE 115 ON INQUIRY CARD

NO.1 AGAIN

This time in Switchers

Long the recognized leader in quality open-frame linears, Power-One is now setting the pace in switching power supplies.

Our fast growing line of efficient high-performance switchers offer a combination of features not found in others at these low prices. Features such as fully regulated outputs, 115/230 VAC input capabilities, superior hold-up time, and totally enclosed packaging for enhanced safety. Additionally, these models incorporate many other innovative ideas that set our switchers apart... while reflecting the same simplicity of design that has kept our open-frame linears the most cost-effective in the industry.

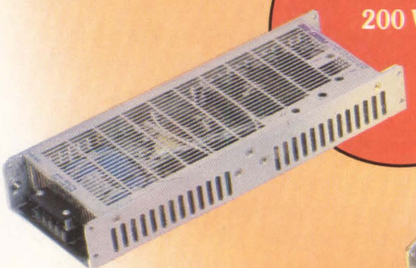
Best of all, Power-One switchers are 100% American built by Power-One personnel, at Power-One facilities, and under tough Power-One quality control standards. Adding up to total dependability at typical Power-One low prices.

So check us out. See why we're leading the way again. This time in switchers.

Send for our new '81 Catalog. Better yet, contact your local Power-One representative for immediate action.

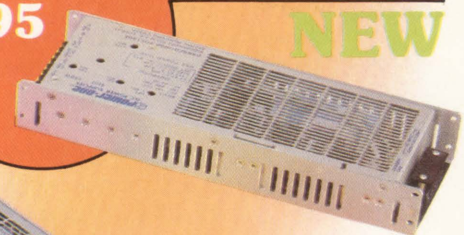
VOLTS	AMPS	MODEL
5V	40A	SK5-40
12V	16.8A	SK12-16.8
15V	13.4A	SK15-13.4
24V	8.4A	SK24-8.4
28V	7.2A	SK28-7.2
SIZE: 2"H X 4.88" W X 13"L		

$250
200 WATTS



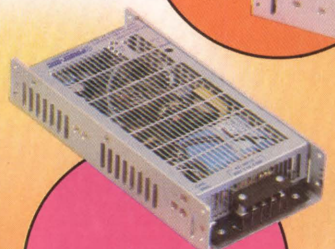
OUTPUT	VOLTS	AMPS
#1	5V	20A
#2	12V	5A
#3	−12V	3A
#4	5V, 12V, 15V, or 24V. USER SELECTABLE	3.5A
SIZE: 2"H X 4.88"W X 14"L		
MAX OUTPUT POWER: 150 WATTS CONTINUOUS, SUM OF ALL OUTPUTS		
150 WATTS - 4 OUTPUTS THE UNIVERSAL SHQ-150W		

$295 NEW



$115
50 WATTS

VOLTS	AMPS	MODEL
5V	10A	SD5-10
12V	4.2A	SD12-4.2
15V	3.4A	SD15-3.4
24V	2.1A	SD24-2.1
28V	1.8A	SD28-1.8
SIZE: 2"H X 4.88"W X 6.25"L		

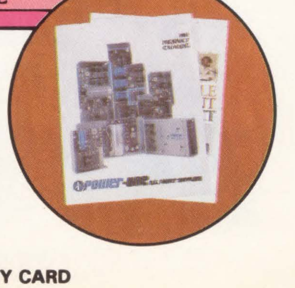


$170
100 WATTS

VOLTS	AMPS	MODEL
5V	20A	SF5-20
12V	8.4A	SF12-8.4
15V	6.7A	SF15-6.7
24V	4.2A	SF24-4.2
28V	3.6A	SF28-3.6
SIZE: 2"H X 4.88"W X 10"L		

FREE! NEW 1981 CATALOG AND POWER-ONE TOUR GUIDE.

SEE EEM OR GOLDBOOK FOR OUR COMPLETE PRODUCT LISTING AND LOCATION OF YOUR NEAREST POWER-ONE REPRESENTATIVE.



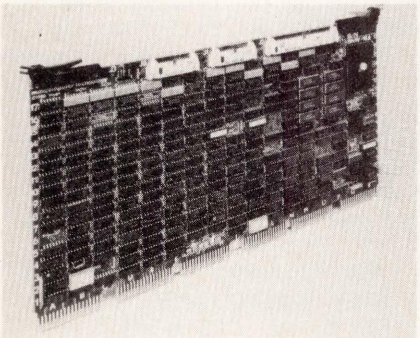
POWER-ONE D.C. POWER SUPPLIES

POWER-ONE INC. • POWER ONE DRIVE • CAMARILLO, CA 93010
PHONE: (805) 484-2806 • (805) 987-3891 • TWX: 910-336-1297

CIRCLE 116 ON INQUIRY CARD

MEMORIES

UNIBUS COMPATIBLE DISC CONTROLLER



SMV15 single-board SMD controller DEC VAX-11/780 and PDP-11 Unibus series features 32-bit data error and header error control and supports any 1 or 2 SMD interface compatible drives. Jumper selectable DMA throttle rate optimizes system throughput, bipolar architecture implements most controller functions in firmware, and sector interleaving factor permits efficient disc and bus utilization. Board plugs directly into any SPC slot and is media compatible with SMC11 disc drive. **MiniComputer Technology**, 2470 Embarcadero Way, Palo Alto, CA 94303.

Circle 222 on Inquiry Card

PERKIN-ELMER EMULATING DISC CONTROLLER

SPECTRA 14 emulates MSM-80 and MSM-300 disc subsystems while attaching up to four 80M- or 300M-byte compatible drives, and is completely compatible with full range of Perkin-Elmer 16- and 32-bit minicomputers. Dual bipolar microprocessor design controls both CPU channel and disc interfaces simultaneously. Onboard self test microdiagnostics and 32-bit error correction code assure reliability, and 1.5k-byte RAM buffering eliminates "data late" errors and achieves optimum speed between disc and selector channel. **Spectra Logic Corp**, 2316 Walsh Ave, Santa Clara, CA 95051.

Circle 223 on Inquiry Card

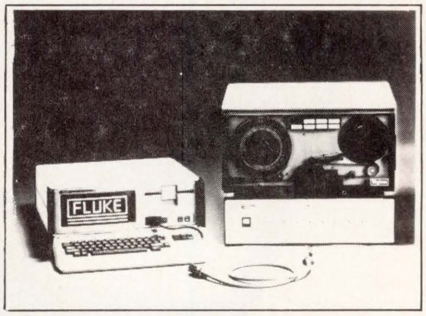
EPROM-ERASING UV CABINETS

Spectroline[R] PC-4400 erases up to 288, and PC-2200 up to 144 EPROM chips at one time in as little as 6 min. Cabinets also accept PCBs and 4" (10.2-cm) dia silicon wafers for erasure without need for removal. Both units have ultrahigh intensity ozone-free grid lamps having peak irradiance of 16k uW/cm² typ at chip level. Specular reflectors provide uniform UV distribution. Housings shield user from hazardous radiation, and safety interlock prevents premature operation. 60-min timer is included for automatic shutoff. **Spectronics Corp**, 956 Brush Hollow Rd, PO Box 483, Westbury, NY 11590.

Circle 224 on Inquiry Card

IEEE-488 TAPE SYSTEMS

Available in 10.5, 8.5, and 7" (26.6-, 21.5-, and 17-cm) reel sizes, and in 800- or 1600-bit/in (315 or 630/cm) or dual-density models, models 2001 and 9001 0.5" (1.27-cm) tape systems provide transfer rates over 100k bytes/s and transport speeds of 25 to 75" (63 to 190 cm)/s. Self-test feature checks RAM and ROM on power-up; signature analysis identifies failed components. Code conversion between ASCII and EBCDIC is optional. **Dylon Corp**, 3670 Ruffin Rd, San Diego, CA 92123.



Circle 225 on Inquiry Card

CIRCLE 117 ON INQUIRY CARD

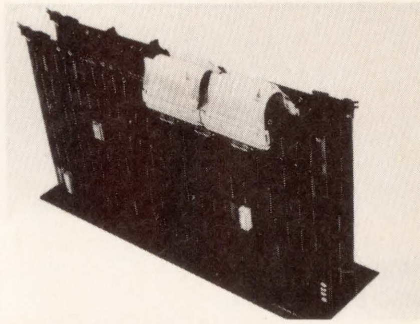
COMPUTERS AND COMPUTER SYSTEMS

COMPUTER GRAPHICS SUBSYSTEM

Subsystem provides G150 microprocessor video display terminal, G100 graphics options board, and G160 computer printer. Terminal features upper/lowercase characters, 12 x 10 char resolution, 24 x 80 char display, 12" (30-cm) screen, and 14-key numeric pad. Graphics board features Tektronix 4010/4012 graphics format and 4012 Alpha Mode, and 512 x 520 resolution. Printer speed is 32 dot rows/s, 560 dots/row. Line length is 560 dots/7.2" (18.2-cm) line on an 8.5" (21.5-cm) page. **MQI Computer Products**, 18381 Bandilier Cir, Fountain Valley, CA 92708.

Circle 260 on Inquiry Card

ARRAY PROCESSOR FOR PDP-11



MSP-3X block floating point array processor, on two standard hex 8.4 x 15.7" (21.3 x 39.9-cm) boards that plug directly into the SPC slots of the host, is said to perform a variety of signal analysis functions at 20 to 50 times the speed of the PDP-11 alone. Connected to host by DMA interface, processor uses 24-bit mantissa and 8-bit exponent, and includes 4k x 24-bit high speed data memory and onboard memory table of trigonometric values. It represents one load on the UNIBUS™. Required 52.5-W power is supplied by the host. **Computer Design & Applications Inc**, 377 Elliot St, Newton, MA 02164.

Circle 261 on Inquiry Card

MODULAR INTERACTIVE DISPLAY SYSTEM

Consisting of four basic modular components designed for use individually or as a total system, alphanumeric display may be linked with multiple displays to provide message transmission networks and silent paging systems. All programmable display and interface functions may be controlled from keyboard through use of ASCII control codes. Modules include alphanumeric display, capacitive keyboard, power supply, and housing. Alphanumeric display (W416-1053 or W420-1053) is a self-contained 14-segment single-line display. Complete microprocessor controlled circuitry includes drivers, character generator, and refresh memory, and provides all std functions. Switch selectable features include full- or half-duplex, and 8 baud rates from 110 to 9600. The solid-state capacitive keyboard has 66 ASCII encoded keys plus functions for other keys with relegendable tops. The system power supply delivers 12 V at 1 A and −12 V at 50 mA to display system. It operates from normal 120-Vac, 60-Hz, 0.25-A line voltage. **Cherry Electrical Products Corp**, 3600 Sunset Ave, Waukegan, IL 60085.

Circle 262 on Inquiry Card

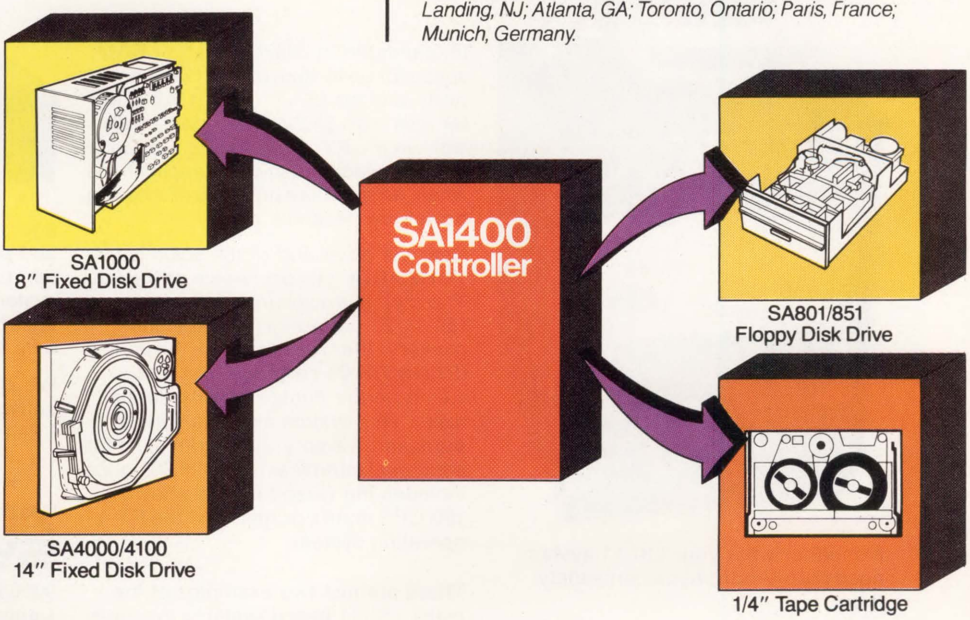
Shugart's fixed disk back-up solution. You can get started today.

We'll get you going fast. If designing a fixed disk system with back-up is taking too long and costing too much, we can help—today. We'll get you started with Shugart 8 or 14-inch Winchester fixed disk drives, floppy drives for back-up—and a new series of the most versatile and intelligent controllers available. And if you need additional back-up capability, our controllers can handle 1/4-inch streaming tape cartridge drives, too.

The intelligent approach. Our new SA1400 intelligent controllers are so flexible and easy to interface that you can get your fixed disk system on-line in two or three days instead of weeks. SA1400 controllers feature the AMD 2900 series MPU along with ECC, sector interleaving, sector buffering, automatic copying, data separation, and on-board microdiagnostics. For greater flexibility, all SA1400's have the same Host I/O. The SA1400 offers more intelligence than most competitive controllers while relieving the CPU of more drive-related functions for faster data throughput.

The low cost solution. We've solved the cost problem, too. First you get the lowest cost per Megabyte fixed disk drives in the industry. Next, add a realistically priced intelligent controller and either a floppy drive or a 1/4-inch streaming tape drive. Back-up media costs are minimal and you only need a single power supply. And design costs are low because you get started faster. The Shugart solution. An intelligent approach to back-up that combines fast start-up with significant system savings. If this is what you've been waiting for, contact your nearest sales office today.

Shugart Associates: 475 Oakmead Parkway, Sunnyvale, CA 94086 (408) 733-0100. *Sales & Service: Sunnyvale, CA; Costa Mesa, CA; Minneapolis, MN; Richardson, TX; Framingham, MA; Landing, NJ; Atlanta, GA; Toronto, Ontario; Paris, France; Munich, Germany.*

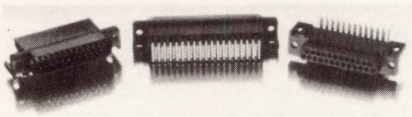


Shugart

Headstrong about mass storage value.

PACKAGING AND INTERCONNECTION

MULTITERMINAL CONNECTOR



Series 6850 subminiature D-pin and socket connectors install directly over the PC trace pattern, and do not require additional insulation. Connector is available in 9-, 25-, and 37-contact configurations, and contacts are gold-plated and preloaded with posts bent to a 90° angle. Recommended board hole size is 0.042" (1.19-mm) diameter, and max board thickness is 0.093" (2.36 mm). Current rating is 1 A with dielectric withstanding voltage at 1,000 V. Op temp range is −55 to 140 °C. **Stanford Applied Engineering, Inc,** 340 Martin Ave, Santa Clara, CA 95050.

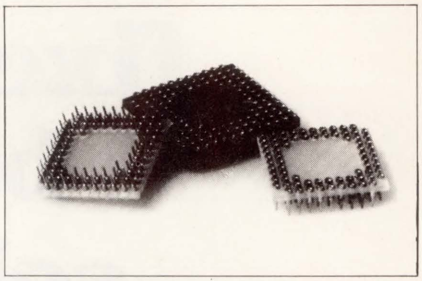
Circle 226 on Inquiry Card

2-PIECE PCB CONNECTORS

Series of economical dip solder and crimp type connectors developed for reliable board to board, cable to cable, or cable to board interconnects in a stress environment provides a broad selection of single row miniature connectors with 2.5-mm contact spacing. Some series elements have securing latches. Dip solder types are intended for direct coupling of PCBs and achieve high density in small space. Automatic crimp termination and semiautomatic equipment are available for all series. **TRW Cinch Connectors,** 1501 Morse Ave, Elk Grove Village, IL 60007.

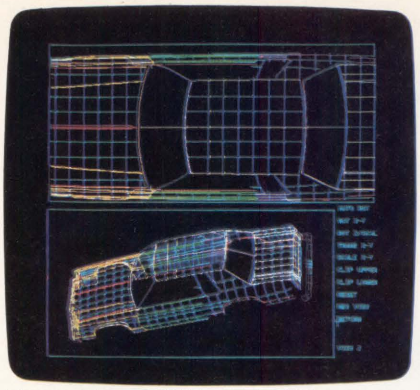
Circle 227 on Inquiry Card

PLANAR GATE ARRAY SOCKETS

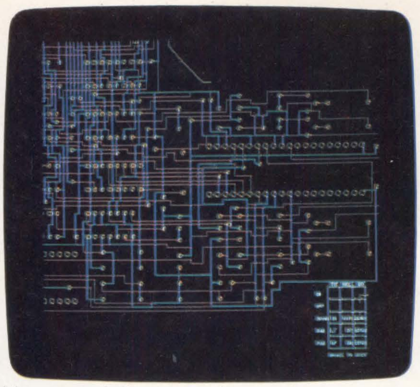


Family of pin-pak (patent pending) sockets for use in interconnecting planar gate array and similar plug-in IC packages features specially designed machine contacts to provide lower extraction and insertion forces to accommodate these multipin arrays with pins on 0.100" (2.5-mm) grid. Each contact is enclosed in bottom machined sleeve to prevent solder wicking or flux contamination. Sockets for 64-, 72-, and 120-pin packages are available, other sizes on request. **Augat Inc,** 33 Perry Ave, PO Box 779, Attleboro, MA 02703.

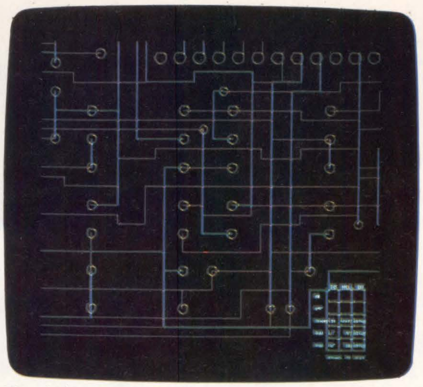
Circle 228 on Inquiry Card



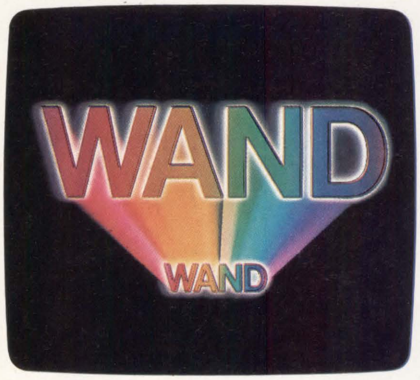
Megatek's new Whizzard 6250 raster system makes advanced computer graphics more economical than ever.



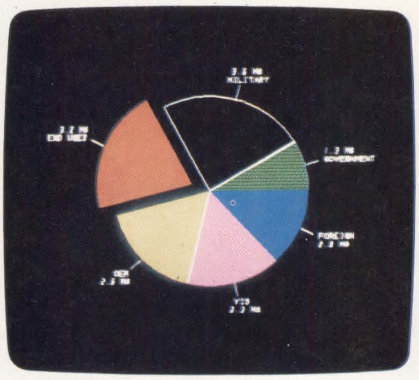
You can define your image in a 4096 x 4096 virtual space, with up to eight colors.



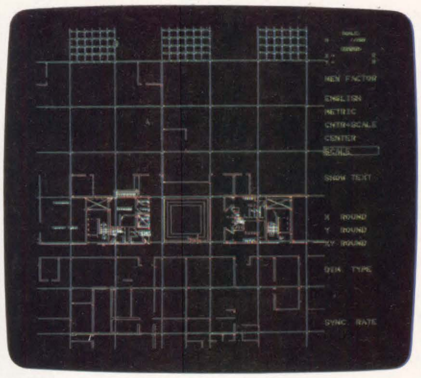
Real-time dynamics enable you to pan throughout this space, then zoom in with true scaling for added detail.



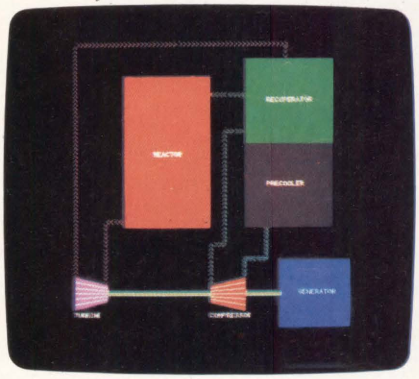
And our new system introduces you to low-cost, FORTRAN-based WAND software.



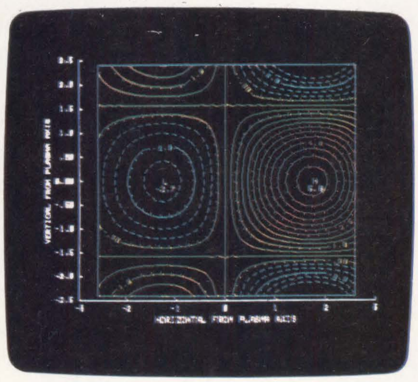
The Whizzard 6250 harnesses the power of Megatek technology for your business applications . . .



. . . for new flexibility in architecture and drafting . . .



. . . for an added dimension in process control . . .



. . . and wherever a visual presentation makes data easier to understand.

So imagine yourself at the Whizzard 6250 keyboard. Computer creativity has never been so affordable.

Imagine . . . all this technology for far less than you imagined.

At Megatek, we strive to set the standards for technology in computer graphics. Now we've set a new standard for value, too. Introducing our new Whizzard 6250 system.

It gives you graphics power you would expect from Megatek. For far less than ever before. You get the drama of full raster color. High resolution. Sophisticated dynamics implemented in hardware. Local vector memory. Double buffered bit planes. And the performance of advanced digital vector generation. Plus an RS-232 interface, standard.

The 6250 has its own version of easy to use WAND software. It's upward compatible to WAND 7200, software for our family of advanced systems and terminals.

MEGATEK

MEGATEK CORPORATION

The new Whizzard 6250 is the perfect starter system for end-users. OEM configurations are available too. Imagine all the possibilities. Better yet, write for all the facts. Megatek Corporation, 3931 Sorrento Valley Blvd., San Diego, CA 92121. 714/455-5590. TWX 910-337-1270. Megatek International/Europe 11 Woudstraat, 4031 JA Ingen, The Netherlands. Telephone: 31 3443-2800. TWX 70619.

CIRCLE 121 ON INQUIRY CARD

First compare quality. Then compare cost.

Morrow Designs' 10 megabyte hard disk system: $3,695.

MORE MEMORY. LESS MONEY.

Compare Morrow Designs' DISCUS™ M26™ hard disk systems to any system available for S-100 or Cromemco machines. First, compare features. Then, compare cost per megabyte. The M26 works out to under $200 a megabyte. And the M10 is about half the cost of competing systems.

COMPLETE SUBSYSTEMS.

Both the M10 (8"), and the M26 (14"), are delivered complete with disk controller, cables, fan, power supply, cabinet and CP/M® operating system. It's your choice: 10 Mb 8" at $3,695 or 26 Mb 14" at $4,995. That's single unit. Quantity prices are available.

BUILD TO FOUR DRIVES.

104 Megabytes with the M26. 40+ megabytes with the M10. Formatted. Additional drives: M26: $4,495. M10: $3,195. Quantity discounts available.

S-100, CROMEMCO AND NORTH STAR*.

The M26 and M10 are sealed-media hard disk drives. Both S-100 controllers incorporate intelligence to supervise all data transfers through four I/O ports (command, 2 status and data). Transfers between drives and controllers are transparent to the CPU. The controller can also generate interrupts at the completion of each command ...materially increasing system throughput. Sectors are individually write-protectable for multi-use environments. North Star or Cromemco? Call Micro Mike's, Amarillo, TX, (806) 372-3633 for the software package that allows the M26 and M10 to run on North Star DOS. MICAH of Sausalito, CA, (415) 332-4443, offers a CP/M expanded to full Cromemco CDOS compatibility.

Morrow Designs' 26 megabyte hard disk system: $4,995.

AND NOW, MULT-I/O.™

Mult-I/O is an I/O controller that allows multi-terminal and multi-purpose use of S-100 and Cromemco computers. Three serial and two parallel output ports. Real time clock. Fully programmable interrupt controller. Designed with daisy-wheel printers in mind. Price: $299 (kit), $349 assembled and tested.

MAKE HARD COMPARISONS.

You'll find that Morrow Designs' hard disk systems offer the best price/performance ratios available for S-100, Cromemco and North Star computers. See the M26 and M10 hard disk subsystems at your computer dealer. Or, write Morrow Designs. Need information fast? Call us at (415) 524-2101.

Look to Morrow for answers.

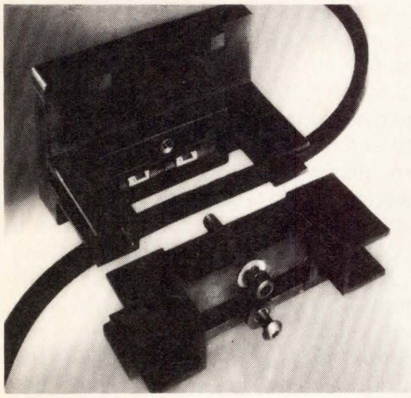
MORROW DESIGNS

5221 Central Avenue
Richmond, CA 94804

*CP/M is a trademark of Digital Research Corp.
*Cromemco is a trademark of Cromemco, Inc.
*North Star is a trademark of North Star Computers, Inc.

PACKAGING AND INTERCONNECTION

ACTIVE COAXIAL DATA HIGHWAY TAP



Making an electrical and mechanical tap connection to coaxial cable without cutting the cable or otherwise interrupting service of a coaxial data highway system, the Active Coaxial Tap connects both 50- and 75-Ω cables. Center conductor of the cable is captivated between a pair of insulated metal probes. One probe is fixed and the other is spring-loaded, ensuring a residual stored-energy connection for long term stability. Both probes are sharp enough to pierce the cable unassisted, so that a minimal amount of metal enters the cable to avoid excessive insertion losses. Capacitive loading is less than 3 pF. Two sets of ground prongs pierce the cable jacket and deform to crimp the cable braid between the two pairs of compliant prongs in each set. **AMP Inc**, Harrisburg, PA 17105.

Circle 229 on Inquiry Card

FIBER OPTIC ACTIVE COMPONENT RECEPTACLE

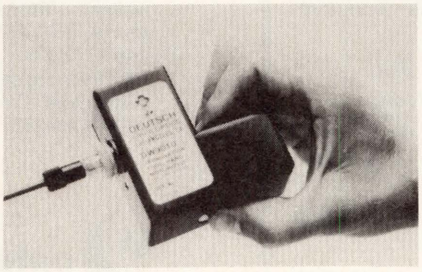
Fiber optic active component (FOAC) receptacle 905 series interconnects SMA-type connectors with different styles of FOAC devices, including Motorola STRAIGHTSHOOTER™ emitters and detectors and United Detector Technology UDT® FO-02-200 detectors. Typ insertion loss when mated with 905 and 906 series fiber optic connectors is 1.25 dB. Less than 0.300″

(7.6-mm) high, device meets standard 0.500″ (12.7-mm) computer board spacing requirements. Components include FOAC receptacle, emi/rfi shield, and lockwasher and nut for bulkhead mounting. **Amphenol North America Div**, 2122 York Rd, Oak Brook, IL 60521.

Circle 234 on Inquiry Card

FIELD TERMINABLE FIBER OPTIC BOX CONNECTOR

For all Corning, Valtec, and ITT graded 50- to 100-μm core fibers, "Terminus" consists of DW 4600 series plug, DW 4400 coupling nut, DW 4500 receptacle, coupling threads, and square flange for mounting on flat surface. Spring loaded tip holds and protects fiber end when connector is unmated, and permits fiber end to automatically align into optical lens system of connector plug when connector is inserted into receptable. Insertion loss is less than −1.0 dB in repeated use. **Deutsch Fiber Optics Div**, 7001 W Imperial Hwy, Los Angeles, CA 90045.



Circle 235 on Inquiry Card

PRINTERS/PLOTTERS

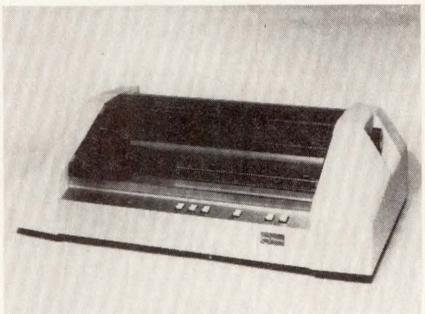
DAISYWHEEL TELEPRINTER TERMINAL

Model 833 provides programmable keyboard, nonvolatile memory, bidirectional printing with combined horizontal and vertical motion and space compression, 128-char ASCII character set, 2k-byte internal buffer expandable by 32k bytes, 3-way buffer overflow protection, and test and diagnostic systems covering all terminal functions. Terminal operates at selectable rates of 110, 150, 300, or 450 bits/s, and std print speed is 45 chars/s. Optional 600 or 1200 bit/s rates, and text enhancements are available. **Anderson Jacobson, Inc,** 521 Charcot Ave, San Jose, CA 95131.

Circle 263 on Inquiry Card

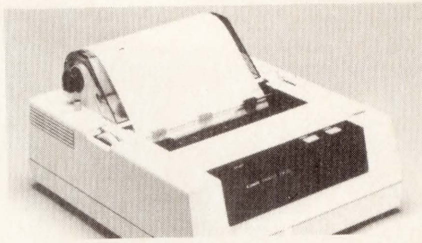
SERIAL DOT MATRIX PRINTER TERMINAL

Desktop PM-LC11 provides bidirectional printing of 10, 12, or 13.3 chars/in, with either 6 or 8 lines/in (2 or 3/cm) vertical spacing, 600-char FIFO buffer storage, underlining, double-width characters, graphics mode, and full ASCII character set. Printer incorporates pushbutton self-test, and external operator panel provides for selection of power on/off, on/off line, vertical alignment, feed, form feed, and top of form. Terminal accepts parallel, RS-232, or current loop interface. **Plessey Peripheral Systems,** 17466 Daimler, Irvine, CA 92714.



Circle 264 on Inquiry Card

THERMAL/IMPACT RECEIVE ONLY PRINTERS



Providing vertical and horizontal movement with printing speeds of 80 chars/s, PW-80 is a bidirectional wire dot matrix impact printer and the PT-80 is a quiet thermal printer. Both are capable of graph plotting, provide the full 128-char ASCII set (as well as 32 semigraphic characters and special symbols), are capable of both std and half-pitch size characters, and provide 80- or 160-col line lengths. Interfaces are EIA RS-232-C (V.24) or 8-bit parallel. Character sizes are 2.04 x 2.94 mm std (5 x 8 dots) and 1.20 x 2.20 mm (3 x 6 dots) half-pitch on the PW-80, 1.99 x 2.82 mm and 1.15 x 2.10 mm on the PT-80. **Canon USA, Inc, Systems Div,** One Canon Plaza, Lake Success, NY 11042.

Circle 265 on Inquiry Card

CIRCLE 124 ON INQUIRY CARD

CIRCLE 125 ON INQUIRY CARD

WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60/S4 STANDS ALONE.

Magnavox combines the superior display and control features of the plasma-panel-based Orion-60 terminals with the powerful S4 Micro-Computer System.

The result is a stand alone graphics system that allows you the freedom to develop a wide variety of graphics application and development programs—while maintaining complete control over program storage, program-generated data, library routines and other facilities.

The Orion-60 display terminal offers full graphics with floppy-disc storage, as well as optional rear-projection functions. It lets you create your own displays and enter data by simply touching the screen with your finger. So you can program your own character sets and generate vectors of any length to absolute coordinates. And because the Orion-60 is plasma-based, you'll get bright, high-contrast images free of jitter or distortion.

The S4 Micro-Computer has system software with development capabilities that are as good or better than those found in many larger computer systems.

Features include CP/M* 8080 system utilities, Fortran with 32K RAM, and a full range of graphic utility routines including window, zoom, sub-image movement and rotation.

The Orion-60/S4.

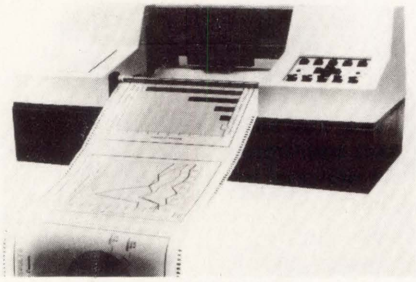
For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 South Coliseum Boulevard, Fort Wayne, Indiana 46803, (219) 482-4411.

Magnavox
DISPLAY SYSTEMS

**CP/M is a trademark of Digital Research.*

CIRCLE 126 ON INQUIRY CARD

HIGH SPEED PLOTTER



Model 1453SX, a 12" (30-cm) 4-pen digital drum plotter, is a desktop unit with the high speed and fine resolution of 36" (91-cm) units. It offers max speeds of 15" (38-cm)/s axially; 21" (53-cm)/s diagonally with 0.001" (0.0254-mm) resolution. Designed for use with continuous feed paper for unattended multiple-plot operation, the plotter is equipped with either RS-232 or IEEE-488 interface for connection to a variety of computers and terminals using either a direct communications port or modem connection. An integral, microcomputer based controller provides rapid, cost-effective throughput by shifting a significant portion of the processing from the host CPU to the controller. Communications line errors are detected and corrected automatically by block retransmission. **Nicolet Zeta Corp**, 2300 Stanwell Dr, Concord, CA 94520.

Circle 230 on Inquiry Card

PRINTER/PLOTTER INTERFACE FOR LSI-11 BASED SYSTEM

Model 125 single-board interface allows DEC PDP-11 or LSI-11 systems to use any of the company's electrostatic plotter or printer/plotter, I/O multiplexer, hardcopy controller, or vector to raster converter, and supports all printer/plotter functions. Package includes RT-11 print/plot driver, software, 4' (122-cm) flat cable, and 20' (609-cm) extension cable, and provides printing speeds to 1000 lines/min and plotting speeds to 34 ft² (3 m²)/min. Printer/plotter can be located up to 54' (16.5 m) from computer. **Versatec**, 2805 Bowers Ave, Santa Clara, CA 95051.

Circle 231 on Inquiry Card

DEC COMPATIBLE PRINTER CONTROLLERS

Controllers include a 15' (4.5-m) cable and connector for the printer, and provide a self-test capability that sends a 96-char ASCII test pattern to the printer. 12-position DIP switches allow status, data, and vector registers to be addressed in any available I/O space in the host computer. Controller can be used with serial and line printers at speeds from 160 chars/s to 300 lines/min, fit into the DEC UNIBUS without hardware or software modification, and are compatible with all DEC operating systems. **Mannesmann Tally**, 8301 S 180th, Kent, WA 98031.

Circle 232 on Inquiry Card

132-COL DOT MATRIX PRINTER

Producing correspondence quality overlapping dot matrix characters, model 560 prints bidirectionally at speeds up to 150 char/s and is about half the size and weight of most competitive 132-col machines. In addition to standard proportional character spacing, automatic text justification, variable character sizes and advanced forms control functions, this addition to the Paper Tiger family offers a raster graphics printing option. The unit prints a full 132 char/line at 10 pitch, with other pitches giving up to 220 col on std 15" (38-cm) paper. A 9-wire ballistic printhead uses 2 staggered rows of print needles to create vertically overlapping dots in a single pass of the printhead. The printhead is driven bidirectionally under microprocessor control by a stepper motor drive mechanism with true logic seeking look-a-head capability and high speed slew from the end of one line to the beginning of the next. **Integral Data Systems, Inc**, 14 Tech Circle, Natick, MA 01760.

Circle 233 on Inquiry Card

300-LINE/MIN MATRIX PRINTER

Tabletop printer for small business systems and distributed data processing is useful where requirements call for high throughput with minimum of operator involvement. Three subsystems are offered: model 4355, with programmed I/O controller; 4356 with data channel controller; and 4354 with serial I/O interface. Both 4355 and 4356 run on NOVA and ECLIPSE systems; 4354 can also be used with microNOVA computers. The printers use a 14-wire dual-column printhead that combines the speed and long life of a multiple head with the flexibility of a single head. Expected life is 300M char. Line printing speed ranges from 125 to 300 lines/min, depending on characters per line. A std ASCII 96-char set is printed in a 7 x 7 half-dot matrix. **Data General Corp**, Rte 9, Westboro, MA 01581.

Circle 236 on Inquiry Card

SCREEN TO HARDCOPY PRINTER

Model 1300 screen printer attaches to 1377 display station terminal, allowing users to obtain hard copy directly from screen without central processor or terminal controller intervention. 7 x 7 dot matrix characters are printed in 80-char lines at 100 chars/s. Printer accommodates cut sheets, fan fold, or rolled paper, and can produce original plus two copies on cut sheets or fanfold paper. It measures 4.9 x 11 x 14.5" (12.4 x 28 x 36.8 cm), and weighs 10 lb (4.5 kg). **Memorex Corp**, San Tomas at Central Expy, Santa Clara, CA 95052.

Circle 237 on Inquiry Card

DAISY WHEEL PRINTERS

Three daisy wheel printers have been introduced to the U.S. OEM market. DY 211 is a 20-char/s unit with 13" (33-cm) platen. DY 311 medium speed unit achieves 32-char/s avg and 39 char/s peak speeds and has a 15" (38-cm) platen and RS-232-C interface. High performance DY 811 is similar to DY 311 but with printing speeds of 65 char/s avg and 80 char/s peak. All models have four printing pitches, 1k-byte buffer, parallel interface and ribbon cartridge. **Olivetti Peripheral Equipment SpA**, 525 Executive Blvd, Elmsford, NY 10523.

Circle 266 on Inquiry Card

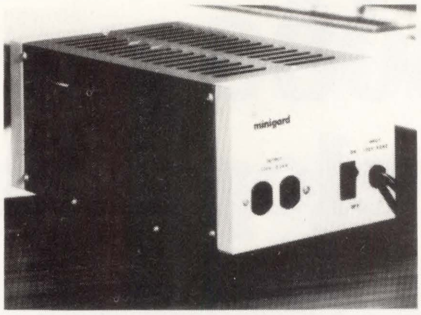
POWER SOURCES AND REGULATORS

DUAL-OUTPUT MODULAR DC POWER SUPPLIES

Thirteen models available in 200 series supplies have outputs of ±5, ±12, or ±15 Vdc and output currents from ±50 to ±500 mA. Input is 105 to 125 Vac at 50 to 440 Hz. Output voltage accuracy is ±1%, line regulation ±0.05% and load regulation ±0.1%. Other specifications include 1-mV rms ripple and noise, 50 μs transient recovery time, and 1500 Vac breakdown voltage. Supplies are encapsulated in phenolic cases having 4-40 threaded inserts and solderable pins for PCB mounting. **Power General,** 152 Will Drive, Canton, MA 02021. 02021.

Circle 238 on Inquiry Card

SMALL COMPUTER VOLTAGE REGULATOR

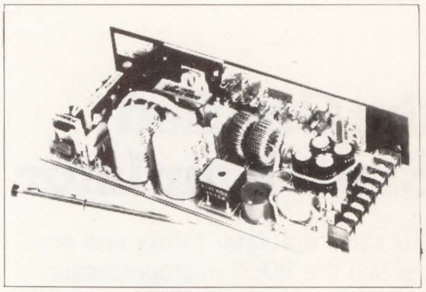


Voltage regulating ferroresonant transformer Minigard™ series comes in portable plug-in versions in sizes up to 2 kVA, and in hardwire models from 300 VA to 11 kVA. The transformers provide instantaneous regulation for constant voltage output, isolation, 120-dB normal noise level attenuation, 60-dB common mode noise rejection, brownout protection, and silent operation. The series was designed for computer and minicomputer systems, POS equipment, terminals, and word processors. **Litton Industries, Jefferson Electric Div**, 840 25th Ave, Bellwood, IL 60104.

Circle 239 on Inquiry Card

SINGLE-OUTPUT 100-W OPEN FRAME SWITCHERS

115- and 230-V inputs, brownout protection, and an MTBF of greater than 50,000 h are provided by 9 SCA models having outputs from 5 to 48 V at 100 W. Input frequencies are 47 to 440 Hz. Line and load regulation are 0.2% max and 0.3% max, respectively. Overvoltage protection at 120 to 140% of the nominal is provided, and noise and ripple are 50 mV pk to pk max for 5-V models and 100 mV for others. Op temp range is 0 to 70 °C, and dimensions are 4 x 9.5 x 2.5" (10 x 24.1 x 6.3 cm). **KEC Electronics, Inc,** 19300 S Vermont Ave, Gardena, CA 90248.



Circle 240 on Inquiry Card

Microcontrol Mastery with Signetics 8X300

Compact floppy disk controller handles multiple drives and formats.

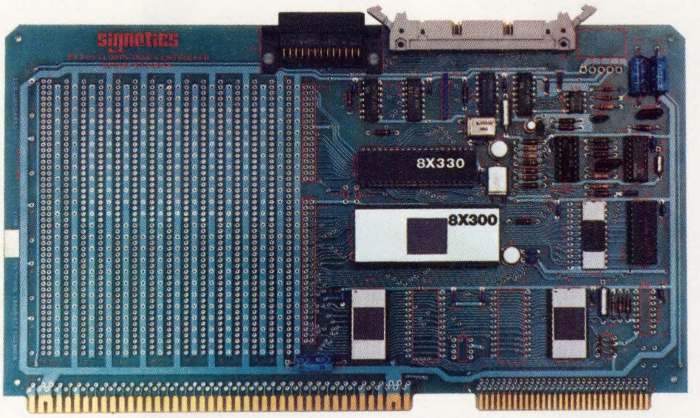
How one design met several goals in firmware.

Today's floppy disk controllers need more than high-performance interface capability. That's why the goals for this design were to maximize flexibility and minimize board space. With performance for tomorrow's needs.

This design—a programmable, intelligent I/O controller built around the 8X300 microcontroller and the 8X330, a new floppy disk controller chip—achieves these goals.

Flexibility is achieved because this FDC can handle multiple disk drives in any combination of single/double density on 5¼ or 8 inch media. With either standard or non-standard track formats.

The on-board 8X300 microcontroller minimizes host overhead by implementing user-defined macro commands. Designed-in flexibility also allows error correction within IBM-compatible formats. And, bipolar performance meets next generation drive requirements with 1 megabyte/second data transfer rates.



Compact Floppy Disk Controller occupies less than half of a standard 7"x12" PCB. The complete controller, based on Signetics' 8X330/8X300, consists of only 10 chips and a host interface.

The 8X330 is the first floppy disk controller chip to integrate the PLL data separator and write precompensation. Result: board space is minimized. An entire double-sided, double-density, dual drive disk controller with RS232 interface requires less than 30 square inches.

Greater flexibility, smaller size, and lower cost. All made possible by the 8X300 microcontroller and the new 8X330 floppy disk controller from Signetics. Find out how you can put Signetics' Microcontrol Mastery to work in your system. Write us today. Or call any Signetics sales or distributor office. *Signetics Corporation, 811 E. Arques Ave., P.O. Box 409, Sunnyvale, CA 94086. (408) 739-7700.*

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To: Signetics Publication Services MS27, 811 E. Arques Ave., P.O. Box 409, Sunnyvale CA 94086

☐ Please send technical information on the 8X300 and 8X330.

☐ I need a more detailed explanation. Please have a Bipolar LSI specialist contact me today at:

( )__________ ext.______

Name__________ Title__________

Company__________ Division__________

Address__________ MS______

City__________ State______ Zip______

CD 281

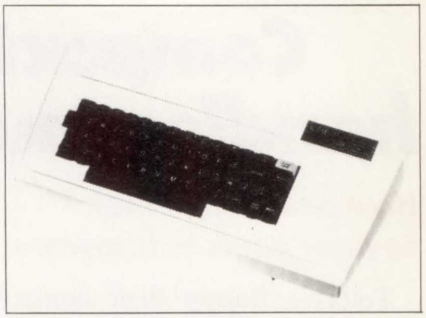
SUBASSEMBLIES AND CIRCUIT COMPONENTS

VANEAXIAL FANS

A larger range of vaneaxial fans for ac and dc operation, the Maxiax^{TM} line is offered in flow ratings from 275 to 825 ft^3/min (7.8 to 23.4 m^3/min). Fans require minimum loads and reduce heat generation. Any number of frequencies and voltages can be furnished in ac models to suit customer requirements. Maxiax Invertafan^R has integrally mounted inverter to convert available 28-Vdc or other dc voltages to the ac input required to drive the motor. **EG&G Rotron, Custom Div,** Woodstock, NY 12498.

Circle 241 on Inquiry Card

KEYBOARD TERMINAL MODULES



KTM-3 provides full ASCII keyboard, composite video for user supplied CRT monitor, and power supply. In 40- and 80-char display width, KTM-3 and -3/80, respectively, versions represent the low cost approach of splitting up the terminal into the keyboard/digital electronics and using a standard CRT monitor. Units consist of 58-key keyboard that generates the full 128 ASCII set of upper/lowercase alphanumerics using an 8 x 10 field size matrix. Video control is provided for scrolling, full-cursor control, and absolute, as well as relative, cursor positioning. Clearing can be achieved to end-of-line or end-of-screen. Even, odd, or no parity with 1 or 2 stop bits is provided. Framing and parity errors are displayed. Switch-selectable baud rates range from 100 to 19.2k. **Synertek Systems Corp,** 150 S Wolfe Rd, Sunnyvale, CA 94086.

Circle 242 on Inquiry Card

INPUT/OUTPUT INTERFACE MODULES

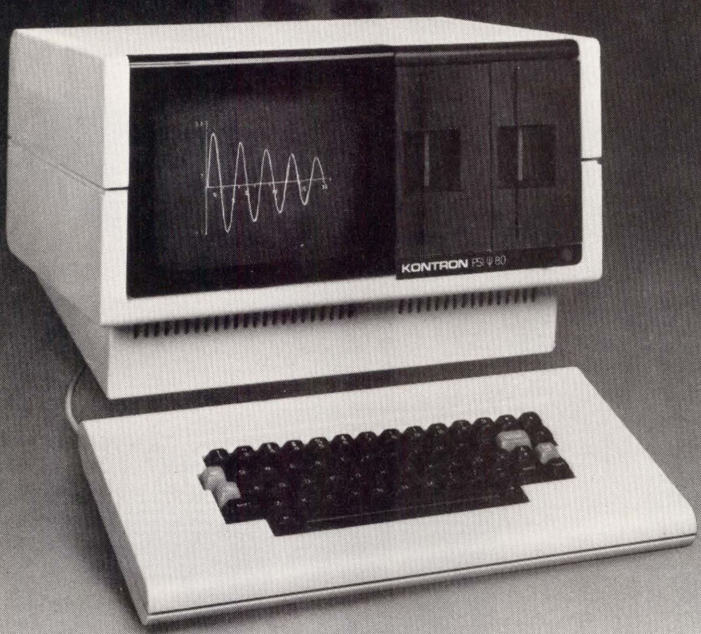
Having footprints of 0.68 in^2 (4.38 cm^2) and volumes of 0.68 in^3 (11.14 cm^3) modules can achieve one-third greater stacking densities and one-fourth less height than previous versions. A break-away screw mount tab incorporated into the housings can be removed when not required, allowing mounting flexibility. Tops of the cases are clean, permitting users to use their own identification markings. Side areas are used for markings, schematic pin layout diagrams, and I/O ratings along with trademark and model designations. Inputs to outputs are photocoupled to provide up to 2500 Vrms isolation. Zero voltage ac switching minimizes emi noise generation. Ac output units have built-in snubber suppression network for high dv/dt and transient voltage protection. **Guardian California,** 4030 W Spencer St, Torrance, CA 90503.

Circle 243 on Inquiry Card

This is Kontron's PSI80 Series Intelligent Computer/Controller

NEW

COMPUTER/
CONTROLLERS:



Introducing . . .
Kontron's PSI80 Series Intelligent Computer/Controller System. The new PSI80 system is designed to control most processes via IEEE 488 bus, RS 232 and parallel interfaces. Additionally, the PSI80 can be easily adapted to any analog or digital source for process control through standard ECB computer boards on a modular basis. Standard features include:

- 32/64 KByte RAM
- Single/dual minifloppies, 144 KBytes each
- Two RS 232 interfaces (synchronous and asynchronous)
- Parallel I/O, Centronics compatible
- 19-inch rack mount capability
- Full graphic video display with an extra 16 KByte video RAM, upper and lower case with extenders on 25 lines at 80 characters
- 9-inch monitor
- Detachable keyboard

Plus . . .
The PSI80 is fully expandable via Kontron's unique card cage design which accepts six Kontron ECB cards for these user-specified functions:

- CMOS RAM (ECB V)
- IEEE 488 (ECB B)
- High-speed arithmetics (ECB A)
- Analog I/O (AN-μP80)
- Digital I/O (ECB I)
- Real time clock (month, date, etc.)
- Subprocessor modules for multiprocessor applications (Z80-EML/SP)

Get complete details and the name of a Kontron sales and service organization near you.

Write or call
Kontron Electronic Inc.
630 Price Ave.
Redwood City, CA 94063

COMPUTER/CONTROLLERS:

For data on Kontron® Computer/Controllers, Digital Multimeters, Counters, PROM Programmers, Logic Analyzer and Printers, call (800) 227-8834. In California call (415) 361-1012.

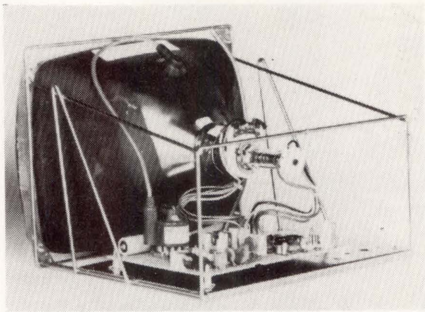
Circle for Literature 130.
Circle for Demo 132.

OPERATIONAL AND BUFFER AMPLIFIERS

ADLH0032 op amp and ADLH0033 buffer amp offer guaranteed offset voltage drifts of ±50 and ±100 μV/°C max, respectively. Op amp features small signal (−3 dB) bandwidth of 70 MHz; 500 V/μs typ, 350 V/μs min; and differential FET input stage with 10^{12}-Ω input impedance and bias currents of ±100 pA max (G grade) and ±200 pA max (CG grade). Unity gain buffer amp features slew rate of 1500 V/μs typ, 1000 V/μs min; ±100 mA output current rating; operation from 0 to 30 or −30 V single or ±5 to ±20 V dual power supply; and 10^{11}-Ω input impedance. CG grades operate over −25 to 85 °C and G grades over −55 to 125 °C. **Computer Labs Div, Analog Devices, Inc**, 505 Edwardia Dr, Greensboro, NC 27409.

Circle 244 on Inquiry Card

ALPHANUMERIC CRT DISPLAY

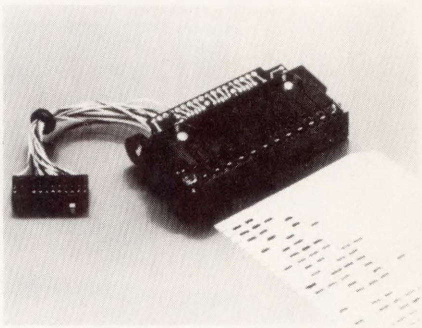


Options available with BC-series 12" (30-cm) display include specified line rates to 19,400 Hz, use of either 20 or 25" (51- or 64-cm) spherical radius CRTs, various phosphors or contrast enhanced screens (25" radius version only), several frame tilt configurations, and ac power supplies. BC-100 models have std horizontal line rate of 15,750 Hz; BC-200 has nominal 18,400-Hz rate plus internal horizontal oscillator and centering control. Both models are available for either 12 Vdc or 15 Vdc power supplies. **Ball Electronic Display Div**, PO Box 43376, St Paul, MN 55164.

Circle 245 on Inquiry Card

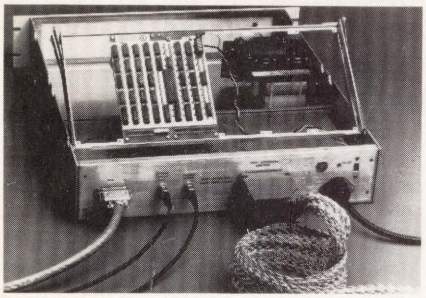
CARD READER SENSOR HEAD

Designed for reading punched or marked 80-col cards, opto sensor head 121 uses individual visible LEDs and silicon phototransistors for each of 12 read positions, and will read marks or punches interchangeably. Pen and pencil marks of many densities and colors can be handled. 12 TTL-level parallel outputs are op amp driven with shaped trigger waveforms. Self-biasing channels require no adjustments. Mechanical isolation and signal control eliminate crosstalk. **HEI, Inc**, Jonathan Industrial Ctr, Chaska, MN 55318.



Circle 246 on Inquiry Card

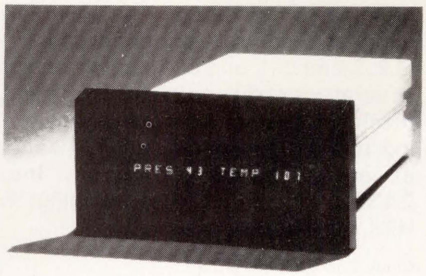
GPIB/IEEE-488 INTERFACE MODULE



Available as integrated plug-in module or self-contained, low profile, rack-mount chassis, GPIB interface for data acquisition systems allows interconnection of analog data acquisition to display devices and compatible lab instruments using a single bus. Functions implemented include service request, talker and listener functions, all DAS operation modes, device command message format, multimode DAS conversion trigger, device trigger, parallel roll, selectable device address, definable data format, data overrun flag, and device clear. **Phoenix Data, Inc,** 3384 W Osborn Rd, Phoenix, AZ 85017.

Circle 247 on Inquiry Card

INTELLIGENT PANEL METER



SPM-100 combines 16 channels of analog input, 12-bit plus sign ADC, user programmable microprocessor, 16-char alphanumeric display, serial communications interface, and industry standard digital I/O option in a convenient panel meter configuration. Its onboard 8748 single-chip microcomputer can be used for scaling, linearization, averaging, units conversion, and limits detection, adapting the unit to applications requiring several inputs to be arithmetically processed into a composite result for display. The 16-char 17-segment alphanumeric display provides capability for annotated data presentation. Software controlled communications interface provides one serial input and one or two serial output ports compatible with current loop, RS-422, RS-423, or RS-232 interfaces. **Elec-Tek, Inc,** 10653 Chester Rd, Cincinnati, OH 45215.

Circle 248 on Inquiry Card

LIGHTED PUSHBUTTON POWER SWITCHES

Available in incandescent and neon versions, series 05-7 switches are offered in momentary or maintained action. Rectagular snap-in panel mounting requires 0.75 x 1.141" (19- x 29-mm) cutout. All switches have quick-disconnect terminals and choice of variety of colored lens caps. Neon switches include lamp with 33k-Ω 0.25-W resistor for 125-V version, and 100k-Ω resistor for the 250-V model. Incandescent switches accept T-1¾ flange base lamps. **Licon, Div Illinois Tool Works, Inc,** 6615 W Irving Park Rd, Chicago, IL 60634.

Circle 249 on Inquiry Card

PRODUCTS

DATA ACQUISITION AND CONTROL

DEDICATED CNC MACHINE CONTROL

Specifically designed for dedicated high production machine tools, Mach 3 MicroCam system is a microcomputer based machine-mounted control unit. The single-board device measures 15 x 17 x 1.75" (38 x 43.2 x 4.4 cm) and provides base control for up to 8 axes of closed loop servo control. It is compatible with both dc and hydraulic servo control systems. Independent portable programmer MicroPort houses programming and control functions and 5" (12.7-cm) CRT, and can support one or several control units at different machines. Programming and monitoring functions need not be duplicated at each machine. **Omicron, Inc,** 24320 Indoplex Circle, Farmington Hills, MI 48018.

Circle 250 on Inquiry Card

INCREMENTAL SHAFT POSITION ENCODER

Solid state shaft encoding and GaAs illumination sources, resolution up to 4096 counts/turn, and TTL compatible outputs are provided by model 81. Std units can provide 2 channels of up to 1024 cycles/revolution. Encoder is available in uni- or bidirectional incremental code models with or without zero index marker pulses, and operates with 5, 12, 15, or 24 V. Dia is 1.5" (3.8 cm), height is 1.10" (2.79 cm). **Litton Systems Inc, Encoder Div,** 20745 Nordhoff St, Chatsworth, CA 91311.

Circle 251 on Inquiry Card

DATA ACQUISITION AND DISPLAY SYSTEM

Designed to monitor and improve power plant performance, data acquisition and display system can be used as integrated data system responsive to requirements of NUREG-0696, process data logger, online performance monitor, computerized device for special purpose tests and analyses, or display via simulator linkup of critical plant parameters. Based on microprocessor technology, the system provides data acquisition for up to 576 single-ended analog or digital input combinations. Data are displayed via RS-232-C ports at up to five independent locations. A total system includes programming for display routines plus capability for users to modify high level programs onsite. The system logs data on tape, maintaining 12 h of stored information. Display peripherals include CRT interface to permit data display on control CRT, b/w or color graphic CRT, or line printer, or to be transmitted over telephone line via a modem. Hard copy printout is available for CRT displays. **Babcock & Wilcox, Nuclear Power Generation Div,** PO Box 1260, Lynchburg, VA 24505.

Circle 252 on Inquiry Card

DATA ACQUISITION SYSTEM

Combined with multiprocessor computer and interactive CRT terminal, PD2064 system can scan 496 inputs, of which 32 can be BCD or counter/timer types. Each terminal can control two PD2064 scanner systems and uses standard RS-232-C signal paths and ASCII codes. Optional switched network mode allows central site control of remotely located scanner systems. Scanner accepts mV, V, thermocouple, thermistor, RTD, and BCD inputs. Computer is factory programmed in English language prompting messages. **Esterline Angus Instrument Corp**, PO Box 24000, Indianapolis, IN 46224.

Circle 253 on Inquiry Card

INTELLIGENT SERIAL TO PARALLEL INTERFACE

SL-6100 facilitates interconnection of such parallel output devices as scales, computers, multiple relay contacts, and BCD output instruments with an RS-232-C serial port. Firmware covers a large number of parallel device types and is configured by onboard jumpers for baud rate, stop bits, and parity check, and by ASCII-coded messages for all other functions. Up to four independent blocks of 16 TTL level I/O lines each are available. Serial port handles speeds from 75 to 9600 baud. **Syslog Inc**, 4996 Place de la Savane, Suite 4, Montreal, Quebec H4P 1Z8, Canada.

Circle 254 on Inquiry Card

DATA ACQUISITION MODULE

ZAD7600 includes 16-channel multiplexer, 12-bit ADC, programmable (2 to 1000) gain amplifier, and sample and hold circuit, and accepts 16 single-ended or 8 differential analog inputs from ±10 mV to ±5 V, and bandwidths of 400 kHz at ±5 V to 10 kHz at ±10 mV. Module will resolve 12 bits with differential linearity of ± ½ LSB and no missing codes; linearity is ±0.012% of full scale. High level signals are converted at 100 kHz, and lower level signals at up to 30 kHz. Modular housing measures 4.6 x 4.6 x 0.4" (11.6 x 11.6 x 1.01 cm). **Zeltex Inc**, 940 Detroit Ave, Concord, CA 94518.

Circle 255 on Inquiry Card

MODULAR HIGH SPEED DATA LOGGER

8212/n, available in 4-, 8-, 16-, or 32-channel packages, digitizes input signals at a variable rate up to 100 kHz, with 12-bit resolution and ½-LSB relative accuracy. Simultaneous sampling (within 5 ns) is allowed. Unit operates in single and continuous modes. Full scale signal range is bipolar ±5 V, 0 to −10 V, or 0 to 10 V. Data are read by computer or stored locally in fast buffer memory. Interfaces are GPIB, RS-232-C, or CAMAC. **LeCroy Research Systems of California**, 1806 Embarcadero Rd, Palo Alto, CA 94303.

Circle 256 on Inquiry Card

LITERATURE

Micro-Winchester Disc Drive

Four-color brochure describes features of 510™ 5.25" unit and tabulates backup alternatives for small Winchester drives. **Irwin International,** Ann Arbor, Mich.
Circle 300 on Inquiry Card

16-Bit Computer

Pamphlet explains architecture for MK-16 and supplies description of basic instruction formats, synopsis of use of Pascal, FORTRAN, or both, and block diagram. **Mikros Systems Corp,** Albany, NY. Circle 301 on Inquiry Card

Add-On Memory

Specs and application notes describing use of add-on memory systems, interfacing, and communication between existing and add-on memory is furnished in application note. **Digital Data Systems, Inc,** Plantation, Fla.
Circle 302 on Inquiry Card

Edgeboard Connectors

Data sheets illustrate and describe series M and S selectively plated edgeboard connectors, featuring dimensional diagrams and electrical, material, and mechanical specs. **Stanford Applied Engineering, Inc,** Santa Clara, Calif. Circle 303 on Inquiry Card

Magnetic Circuit Breakers

"Slide Rule" selector gives comparative data on breaker configurations, ratings, voltages, number of poles, and handle and terminal styles. **AIRPAX/North American Philips Controls Corp,** Cambridge, Md.
Circle 304 on Inquiry Card

Switches and Multiplexers

Catalog lists data and provides functional diagrams and performance graphs for dielectric isolated and non-dielectric isolated monolithic DMOS multiplexers and monolithic CMOS switches. **Micro Power Systems, Inc,** Santa Clara, Calif.
Circle 305 on Inquiry Card

Full-Travel Membrane Keyboard

Illustrated brochure describes design, construction, and operation of keyboard, listing mechanical, electrical, and environmental specs as well as specs for optimal electronics package. **Oak Technology Inc, Switch Div,** Crystal Lake, Ill.
Circle 306 on Inquiry Card

Edge Connectors

Data sheet lists features and constituent materials of CARDCON™ and supplies environmental and electrical specs as well as photo. **TRW Cinch Connectors,** Elk Grove Village, Ill.
Circle 307 on Inquiry Card

Digital Signal Generation

Applications guide describes word generation, timing simulation, bit slice microprocessor controlled data, and timing/generator tester, including pulse, word, and timing generation diagrams. **Interface Technology,** San Dimas, Calif. Circle 308 on Inquiry Card

Interface Protection

Found in brochure detailing devices for signal/data/telephone lines are general specs, survey of various modules, applications diagrams, design example, and mounting information. **MCG Electronics Inc,** Deer Park, NY.
Circle 309 on Inquiry Card

Universal Probes and Test Lead Sets

Pamphlet contains photos, descriptions, and specs of models including oscilloscope, high voltage and rf demodulator probes, as well as test lead sets; also listed are options and accessories. **Test Probes, Inc,** La Jolla, Calif. Circle 310 on Inquiry Card

Custom Power Supplies

Included in brochure are facility photos, design approach techniques, and summaries of engineering, test, manufacturing, and quality assurance functions. **National Power Technology,** Anaheim, Calif.
Circle 311 on Inquiry Card

Educational Programs and Test Instruments

Instruction programs in electronics, microprocessors, and computer programming are detailed in catalog also featuring descriptions and specs on available test instruments. **Heath Co,** Benton Harbor, Mich.
Circle 312 on Inquiry Card

Educational Computer

Brochure describes state of art RC-1 standalone computer system featuring sophisticated graphics, USE language, Z80 microprocessor, CRT with self-contained bit mapped memory, and editing capabilities. **Regency Systems,** Champaign, Ill.
Circle 313 on Inquiry Card

Video Equipment

250-page directory lists and profiles companies manufacturing video hardware and software or providing services for home applications. Single copies available for $25 (prepaid) from **Savvy Management, Inc,** Suite 800, 80 4th Ave, New York, NY 10003. Circle 314 on Inquiry Card

Wideband Multiplexer

Brochure presents photos and specs of Micro750 multiplexer; also included are configuration, network control, and applications block diagrams. **Micom Systems, Inc,** Chatsworth, Calif. Circle 315 on Inquiry Card

Fiber Optic Cables

Features, applications, thermal specs of jacket materials, and optical and mechanical specs for Galite® 6050, 5050, and 5020 are covered by illustrated data sheets. **Galite, Inc,** Wallingford, Conn.
Circle 316 on Inquiry Card

Uninterruptible Power Source

Brochure details operating characteristics, I/O electrical specs, mechanical and physical features, dimensional drawings, and suggested applications for the portable, plug-in Mini UPS. **Sola Electric,** Elk Grove Village, Ill. Circle 317 on Inquiry Card

Universal P/ROM Programmer

Brochure on M980 features cross-reference table of over 500 MOS, bipolar FPLAs, and PALs, correlates devices programmable on M980 with specific personality modules, and includes diagrams and charts. **Pro-Log Corp**, Monterey, Calif.

Circle 318 on Inquiry Card

Selector Switches

Illustrated catalog contains information on thumbwheel, leverwheel, and pushwheel switches, including engineering drawings and specs on 23 different types. **Cherry Electrical Products Corp**, Waukegan, Ill.

Circle 319 on Inquiry Card

Miniature Motion Systems

Including specs, performance curves, part numbers, and selector guide, catalog describes precision miniature dc and ac motors and gearmotors, fans and blowers, and pumps. **TRW Globe Motors**, Dayton, Ohio.

Circle 320 on Inquiry Card

High Speed FFT Processor Design

Application note explains differences between DFT and FFT and details DAU design with timing and block diagrams. **TRW LSI Products**, El Segundo, Calif.

Circle 294 on Inquiry Card

Electronic Components

Highlighting fixed resistors, resistor networks, and panel and trimming potentiometers, catalog includes specs, information on features and applications, diagrams, tables, and illustrations. **Allen-Bradley Co**, Milwaukee, Wis.

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IC Pluggable Packaging Assemblies And Accessories

Catalog includes photos and dimensional diagrams, and covers wide range of interconnection products and capabilities. **Garry Manufacturing Co**, New Brunswick, NJ

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Standard Line Connectors

Catalog includes applications, contact arrangements, electrical and mechanical data, materials and finishes, dimensions, and performance test results for std units for commercial, industrial, military, and aerospace use. **ITT Cannon Electric**, Santa Ana, Calif.

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Power Supplies

Featuring assemblies for test equipment and military ground support, catalog describes std switching and linear power supplies. **Lambda Electronics**, Melville, NY.

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Minicomputers

Describing hardware and software features, specifications, advantages, and reliability features, brochure presents VAX-11/780 and -11/750. **Digital Equipment Corp**, Northboro, Mass.

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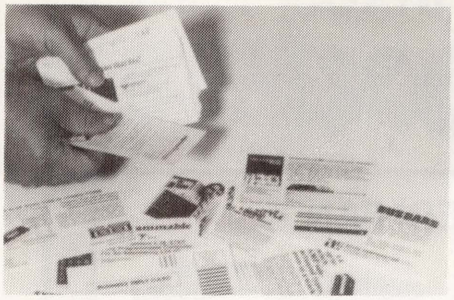

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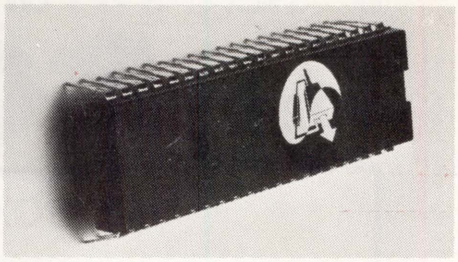

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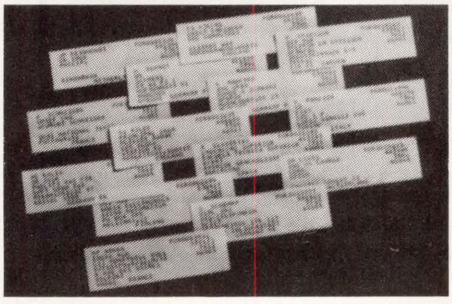

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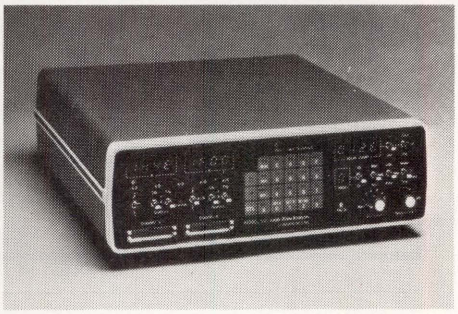

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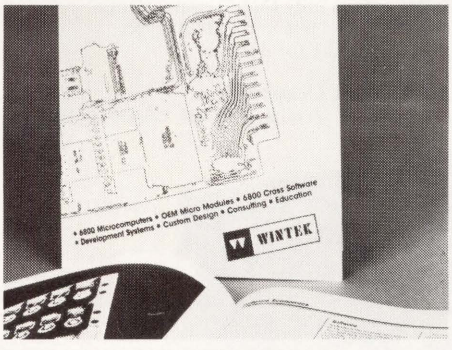

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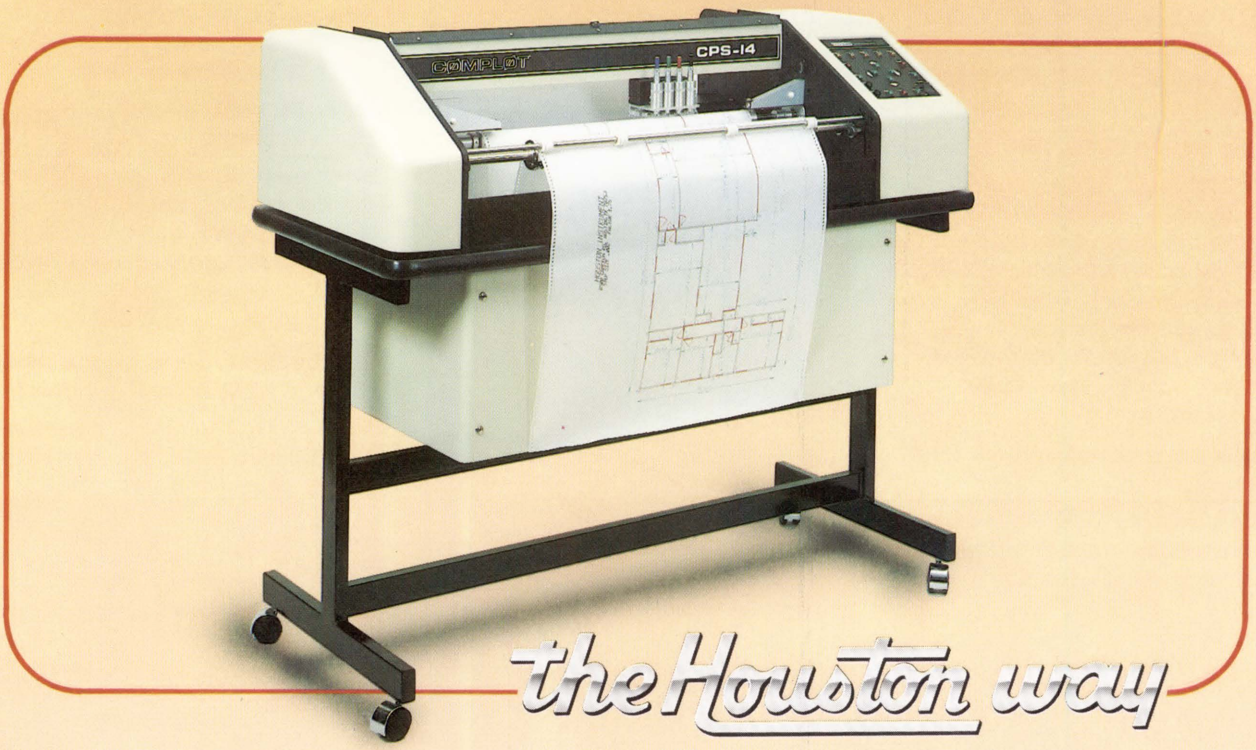

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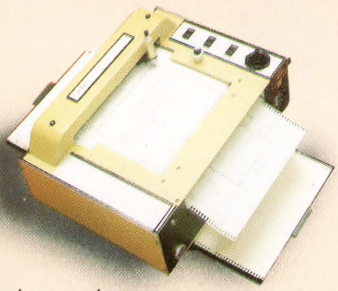

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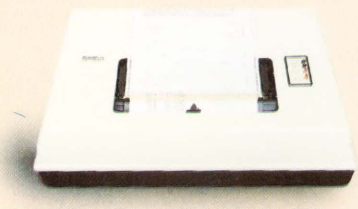

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