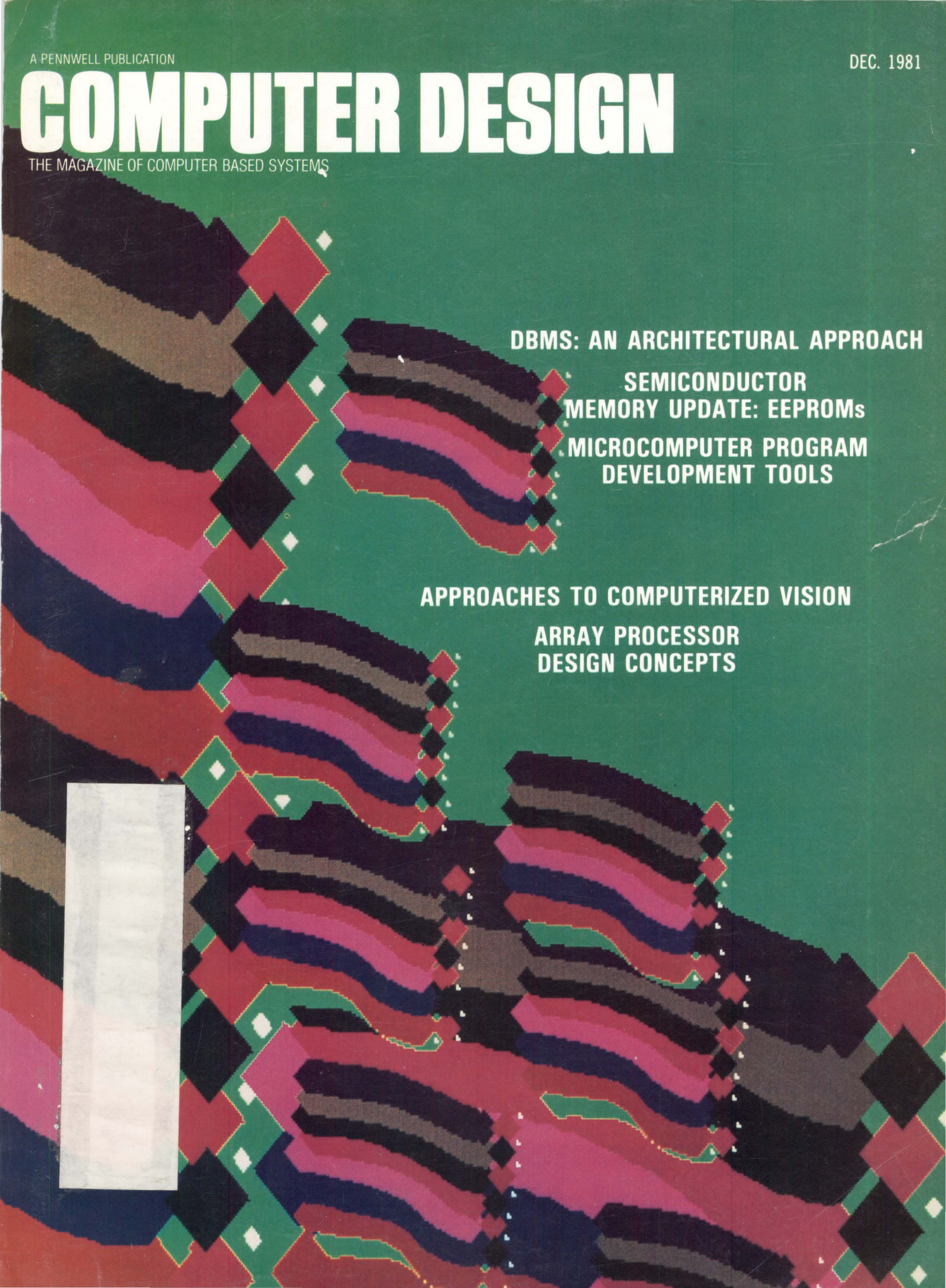
A PENNWELL PUBLICATION

DEC. 1981

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS



DBMS: AN ARCHITECTURAL APPROACH

SEMICONDUCTOR MEMORY UPDATE: EEPROMs

MICROCOMPUTER PROGRAM DEVELOPMENT TOOLS

APPROACHES TO COMPUTERIZED VISION

ARRAY PROCESSOR DESIGN CONCEPTS

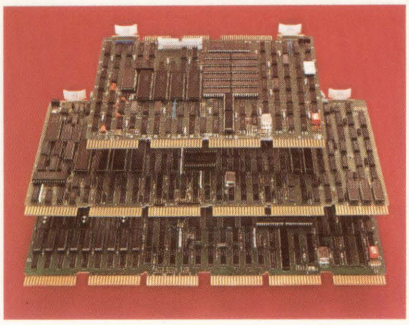
Family pride.

Now there's an advanced technology family of single board controllers for DEC* computers from Western Peripherals—the number one name in controllers.

The TC-131 (for PDP-11s*) is the first TM-11 emulating controller to combine PE and NRZ on one standard hex board. It lets you mix 9-track, PE, NRZ or dual density tape units in any combination up to 125 ips. A 64 byte data buffer allows installation at any point on the unibus without consideration of NPR priority.

The TC-151 single board NRZI tape controller interfaces any industry-standard drive to the LSI-11.* Add a dual width Phase Encode Board for the same performance as the TC-131.

The DC-231 accommodates up to four SMD disc drives of 40 to 600 mb each with RMO2 emulation. Its four sector (2048 bytes) data buffer makes "data-late" errors a thing of the past. The advanced technology "micro-engine" allows a complete track to be written on a single drive revolution. A measurable performance advantage for your PDP-11.



All three controllers are software compatible. All have self test. All are backed by one of the best factory service organizations in the business. And all can be delivered in 30 days.

For more information, call or write today: Western Peripherals Division, Wespercorp, 14321 Myford Road, Tustin, CA 92680, U.S.A. (714) 730-6250. TWX: 910 595-1775. CABLE: WESPER

Number 1 in controllers for DEC and Data General computers.

western peripherals™
Division of WESPERCORP

*Trade name of Digital Equipment Corporation.

CIRCLE 1 ON INQUIRY CARD

We'll back up our disks— and anyone else's.

That's right. Ask any other supplier of peripheral products for system backup, and you'll find that some can supply a disk, some can supply a cartridge recorder, others a streaming transport. But none can supply the choice which Kennedy can offer.

Kennedy is the only company that can offer an SMD compatible, 8" 40 MByte disk drive (Model 7300) and an 80 MByte 14" Winchester disk drive (Model 5380). To back them up, Kennedy has a ¼" cartridge recorder (Model 6450), and Model 6809, ½" Data Streamer Tape Transport.

Kennedy was the first to utilize the ¼" 3M cartridge for disk backup; Kennedy was the pioneer in Winchester disk technology, and was a leader in developing a low cost streaming tape drive.

All of these products were conceived and designed to meet the need for reliable, low cost backup — for our systems or for any other system.

Kennedy has always backed its products. That's why we're No. 1. Call or write us about your problem.

We won't back off.

KENNEDY
Subsidiary, Magnetics & Electronics Inc.
1600 Shamrock Ave., Monrovia, CA. 91016
(213) 357-8831 TELEX 472-0116 KENNEDY
TWX 910-585-3249

KENNEDY INTERNATIONAL INC.
U.K. and Scandinavia
McGraw-Hill House
Shoppenhangers Road
Maidenhead
Berkshire SL6 2QL England
Tel: (0628) 73939
Telex: (851) 847871 KEN UKS G

KENNEDY INTERNATIONAL
Koningin Elisabethplein, 8
B-2700 Sint-Niklaas
Belgium
Tel: (031) 771962
Telex: 71870 KEN CO

KENNEDY • QUALITY • COUNT ON IT

CIRCLE 2 ON INQUIRY CARD

New Cromemco System One shown with our high-capability terminal and printer.

A new small computer that won't limit you tomorrow

Here's a low-priced computer that won't run out of memory capacity or expandability halfway through your project.

Typically, computer usage tends to grow, requiring more capability, more memory, more storage. Without a lot of capability and expandability, your computer can be obsolete from the start.

The new System One is a real building-block machine. It has capability and expandability by the carload.

Look at these features:

- **Z80-A processor**
- **64K of RAM**
- **780K of disk storage**
- **CRT and printer interfaces**
- **Eight S-100 card slots, allowing expansion with**
  - **— color graphics**
  - **— additional memory**
  - **— additional interfaces for telecommunications, data acquisition, etc.**
- **Small size**

GENEROUS DISK STORAGE

The 780K of disk storage in the System One Model CS-1 is much greater than what is typically available in small computers. But here, too, you have a choice since a second version, Model CS-1H, has a 5'' Winchester drive that gives you **5 megabytes** of disk storage.

MULTI-USER, MULTI-TASKING CAPABILITY

Believe it or not, this new computer even offers multi-user capability when used with our advanced CROMIX* operating system option. Not only does this outstanding O/S support multiple users on this computer but does so with powerful features like multiple directories, file protection and record level lock. CROMIX lets you run multiple jobs as well.

In addition to our highly-acclaimed CROMIX, there is our CDOS*. This is an enhanced CP/M† type system designed for single-user applications. CP/M and a wealth of CP/M-compatible software are also available for the new System One through third-party vendors.

COLOR GRAPHICS/WORD PROCESSING

This small computer even gives you the option of outstanding high-resolution color graphics with our Model SDI interface and two-port RAM cards.

Then there's our tremendously wide range of Cromemco software including packages for word processing, business, and much more, all usable with the new System One.

ANTI-OBSOLESCENCE/LOW-PRICED

As you can see, the new One offers you a lot of performance. It's obviously designed with anti-obsolescence in mind.

What's more, it's priced at only $3,995. That's considerably less than many machines with much less capability. And it's not that much more than many machines that have little or nothing in the way of expandability.

Physically, the One is small — 7'' high. And it's all-metal in construction. It's only 14⅛'' wide, ideal for desk top use. A rack mount option is also available.

CONTACT YOUR REP NOW

Get all the details on this important building-block computer. Get in touch with your Cromemco rep now. He'll show you how the new System One can grow with your task.

*CROMIX and CDOS are trademarks of Cromemco Inc.
†CP/M is a trademark of Digital Research

Cromemco™
incorporated
280 BERNARDO AVE., MOUNTAIN VIEW, CA 94040 • (415) 964-7400
Tomorrow's computers today

CIRCLE 3 ON INQUIRY CARD

UP FRONT

EMI test service facility

Chomerics, Inc of Woburn, Mass, has established Radiation Test Services, a facility to perform emi measurements applicable to FCC Docket 20780 regulations as well as to VDE standards. Devices are tested for pass/fail emi radiation analysis. Equipment and test methods are said to replicate those used by the FCC at its Equipment Authorization Laboratory in Laurel, Md.

4M-bit memory chip to be developed

While other companies are delivering 16k- and 64k-bit memory chips—and developing 256k devices—a Texas company claims to be developing a 4M-bit chip that it hopes to license to manufacturers for 1984 product introduction. Condesin, Inc, which will relocate to a facility at 10131 Bubb Rd in Cupertino, Calif, some time after the first of the year, will develop the chip under contract to Ebram, Ltd, a California research and development limited partnership.

Condesin's technology includes patents and patents-pending of Dr Alton O. Christensen, Sr, who was the first to integrate MOS random access memory through patents now owned by Shell Oil Co. Dr Christensen will direct the memory development for Ebram, and says the chip will consist of an 8 x 8 array of 64k-bit storage pages. Each page will be 10 x 10 mils in size and the full 4M-bit chip will be 100 x 164 mils, including control circuitry. Electron beam technology will be used in the read/write circuitry. However, chips will be manufactured by normal photolithographic methods.

Hopper award winner announced

Given annually in recognition of major computing achievements made by individuals under 30 years of age, the 1981 Grace Murray Hopper Award was presented by the Assoc for Computing Machinery to Daniel S. Bricklin, chairman of the board of Software Arts, Inc, and co-creator of the VisiCalc® software package. The award, named for U.S. Navy Captain and computer pioneer Grace Murray Hopper, includes a cash award of $1000, donated by Sperry Univac.

Computer program mimics human reasoning skills

AURA—automated reasoning assistant—is a general purpose program that appears to mimic some reasoning skills of the human mind. According to the scientific development team from the Dept of Energy's Argonne National Laboratory and Northern Illinois Univ, AURA eliminates the need for a scientist to understand complex programming when solving a new problem. The scientist only needs to explain a problem in terms that AURA can understand. AURA interacts with the scientist, who then suggests paths of inquiry for AURA to investigate. AURA does not solve the problem; however, it does produce information that points out directions for further study.

The Japanese come Forth

Quasar, a division of Matsushita Electronic, was seen at COMDEX sporting a handheld 6502 based microcomputer system that features a Forth-like programming language (SNAP), as well as a Micro-Soft™ BASIC. The operating system is said to utilize virtual memory addressing techniques and is written in SNAP.

UP FRONT

Data communications network service announced

Based on receipt of FCC approval, the American Telephone and Telegraph Co is planning to form a separate subsidiary on or before June 1, 1982, for the future provision of enhanced communications services and customer premises equipment. The subsidiary's first offering—by January 1, 1983—would be Advanced Communications Service, an enhanced, shared data communications network service. This service would provide communications processing and storage capabilities, manage data communications networks, and transport data, and is designed to provide increased compatibility among many different terminals and computers, integration of diverse networks, and access to multiple business applications and data bases from a single terminal.

Memory products manufacturer sold

Perkin-Elmer Corp, manufacturer of OEM disk and tape drives, has agreed in principle to sell its Garden Grove, Calif, Memory Products Div to Cipher Data Products, Inc. The agreement includes acquisition of inventories, land, building, equipment, leaseholds, patents, and sales contracts. Cipher expects to retain most former Perkin-Elmer employees. The transaction is subject to further definition of the agreement and approval by the boards of directors of both companies.

Pretriggers

Control & automation Redac Interactive Graphics, Inc, now a division of Racal Electronics Ltd, offers to the U.S. market a broad range of CAD/CAM equipment—from entry level to complex multiterminal systems.

Communications Controller boards from Interlan, Inc, interface DEC UNIBUS and Q-bus systems to the Ethernet local area network.

Microprocessors/ microcomputers Swelling the stream of products out of Digital Equipment Corp in recent months is a 16-bit single-board computer with a compact form factor. Tagged the Falcon SBC-11/21, the board is based on the T-11 chip, a 40-pin MPU that executes the PDP-11 instruction set and is supported by the MicroPower/Pascal software development package.

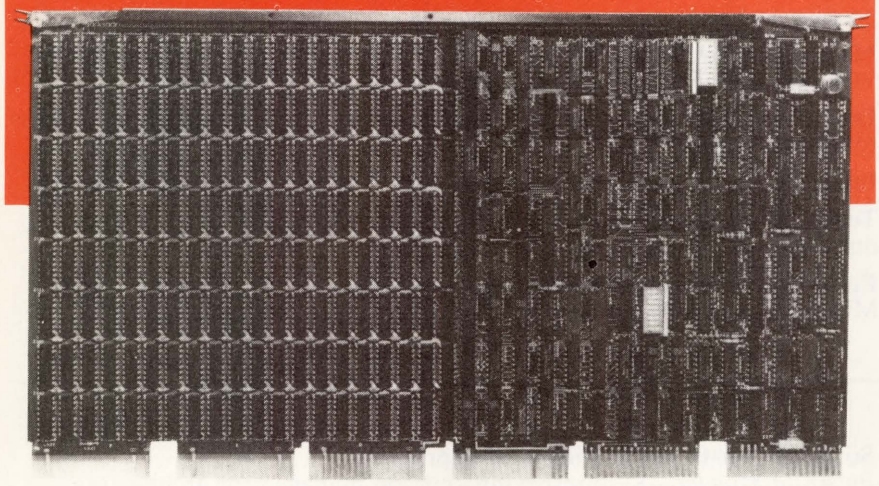
Software Nortek, Inc, has announced the immediate availability of SPICE, a stack oriented, procedural interactive computing environment that combines an operating system, high level programming language, assembler, file system, and multitasking executive. SPICE is designed specifically for systems integration and controller applications utilizing the new DEC Falcon single-board computer. The Forth-like language is also available on the DEC PDP-11 family, Zilog Z80 and Z8000, Motorola 6809, and TI 9900.

Peripherals Serving single-user graphics design needs, the Hewlett-Packard 1360 graphics system supplies a graphics data base and high level software library for creating specialized graphics applications. Supporting plotters, digitizers, printers, and mass storage devices, the Pascal language system eliminates the need to develop interface code for individual devices.

Computers A fault-tolerant 32-bit computer system from Stratus Computer, Inc, takes advantage of the low cost and high performance of current hardware to reduce the cost of continuous processing. By performing failure detection and recovery in hardware, and using high speed checking logic resident on each board, the system eliminates the burden of unproductive processing overhead common in nonstop systems.

Postmaster: CHANGE OF ADDRESS—FORM 3579 to be sent to Computer Design, Circulation Dept, PO Box 593, Littleton, MA 01460. (USPS 127-340)

DEC®-COMPATIBLE SEMI ADD-INS



FROM THE LEADER

Look to the leader — Dataram — for your DEC-compatible semiconductor add-in memory. Offering not only the broadest, most complete line of semi add-ins, but the most capable...no matter what your yardstick. Compatibility, throughput, cost, power efficiency, size...no matter how you measure capability, Dataram DEC-compatible semi add-ins are the clear leader.

A leadership position earned by improving on DEC's price and delivery...and then adding features available from no one else in the industry.

The chart provides a glimpse at the industry-pacesetting family of DEC-compatible semi add-ins. Circle the reader service number below or, better yet, call us today at 609-799-0071, and we'll give you a close-up look at the products that have made us the leader.

DEC Mini	Dataram Add-In	Board Size	Maximum Capacity
LSI-11®	DR-115S	dual	64 KB
LSI-11	DR-215S	dual	256 KB
LSI-11	DR-113S	quad	256 KB
LSI-11	DR-213S	quad	1.0 MB
PDP®-11	DR-114S	hex	256 KB
PDP-11	DR-114SP	hex	256 KB
PDP-11	DR-214SP	hex	1.0 MB
PDP-11	DR-144S	hex	256 KB
PDP-11	DR-244S	hex	4.0 MB
VAX®-11/750 PDP-11/70	DR-175S	hex	256 KB
VAX-11/780	DR-178S	extended hex	512 KB
DECSYSTEM 2020®	DR-120S	extended hex	512 KB
PDP-8/A	DR-118S	quint	128 K x 12

DEC, DECSYSTEM 2020, PDP and VAX are registered trademarks of Digital Equipment Corporation.

Dataram also provides core add-ins, core and semiconductor add-ons, memory system units, memory management, and a wide range of memory-related accessories for DEC users.

DATARAM CORPORATION

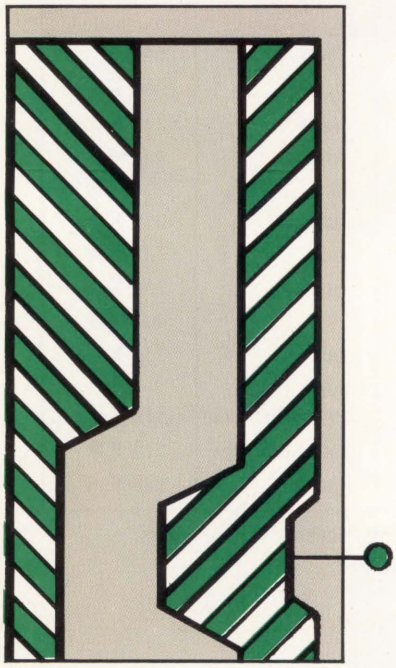
Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

COMPUTER DESIGN®

System technology

112 *A raster scan color graphics display terminal supports 2-D transforms and up to four bit planes of display memory*

System design



137 *MNOS structure, the more mature EEPROM technology, is electrically equivalent to three MOS transistors connected in series, but with common gate*

Vol 20, No 12
Dec 1981

This month's cover by Larry Gartel, entitled "Database architecture," was generated using a Digital Effects VP-3 and D-48 color printer

System components

Departments

Designers' Preference Survey*

*Appearing in Domestic issues only.

Editorial reviewers for this issue:

Albert H. Ashley
Thomas Crawford
John F. Wakerly

GOULD BIOMATION K100-D

7 reasons why the K100-D is now the world's best-selling logic analyzer.

How the general-purpose K100-D beat out H-P to become #1.

Not so long ago, Hewlett-Packard logic analyzers were the industry standard. We asked digital designers to compare the K100-D with H-P's popular 1610B and 1615A logic analyzers before making any buying decision.

In head-to-head comparison, the K100-D came out looking so good, it's now the best-selling logic analyzer in the world. Here's why:

1. It's easy to systematize.

For automated troubleshooting and production ATE, the K100-D features a fully-programmable GPIB interface.

To help you support a wide variety of bus-oriented systems, there are standard high-performance probes, specialized probing accessories and detailed application notes available on all the popular microprocessor systems currently in use.

2. It's concise.

The K100-D monitors 16 channels in time domain, 32 in data domain, so you can probe enough points to pin down problems at their source.

3. It's fast.

A 100 MHz clock rate resolves signals to 10 nanoseconds. The front end is also sensitive enough to capture glitches as narrow as 4 ns.

4. It's deep.

1024 words deep in memory—for faster, more accurate debugging. The K100-D extends the length of data you can trap from your system at any one time.

5. It's clear.

The K100-D has a large keyboard and interactive video display, a comprehensive status menu, highly useful time domain display, and data domain readout in user-specifiable hexadecimal, octal, binary or ASCII.

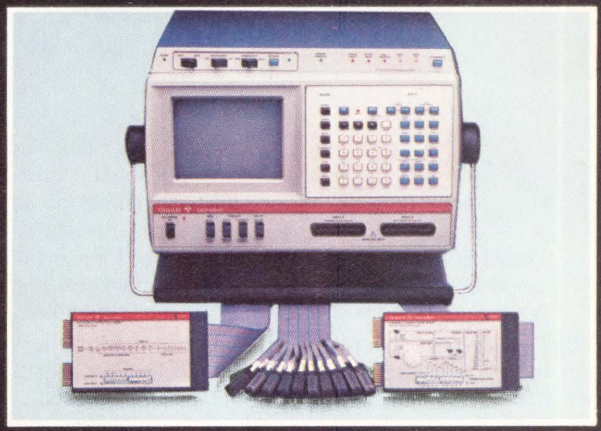
6. It has remote diagnostics.

A new T-12 communications interface option lets your field troubleshooters share their system observations with the best engineers back at headquarters. Remote diagnostics provide faster debugging and save a lot of time and travel for your most valuable people.

7. It's well supported.

You get full applications support from the experts in logic analysis.

For a free copy of our "Logic Analyzer Comparison Guide," request card for microprocessor system application notes, and T-12 Communicator information, just circle the appropriate reader service numbers. Or contact Gould, Inc., Instruments Division, Santa Clara Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050, phone (408) 988-6800.

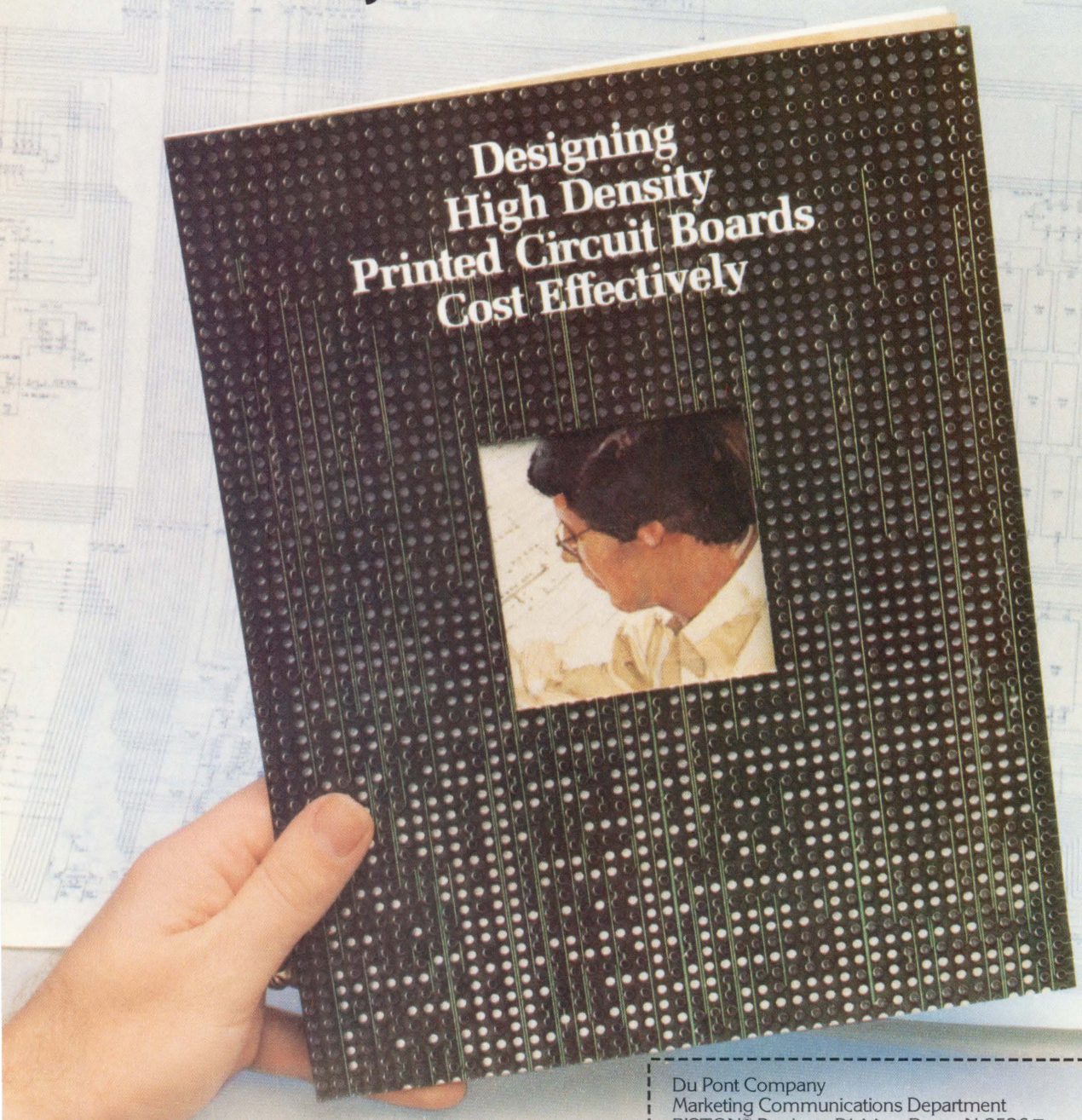


The T-12 "top hat" for the K100-D provides logic analyzer remote diagnostic capability. Other options include the GPIB Analyzer and RS232 Serial Data Analyzer.

Circle 5 for Comparison Guide
Circle 6 for App. Note request form
Circle 7 for T-12 communicator data

GOULD
Electronics & Electrical Products

Write for this important booklet. It could be your most cost-effective idea today.



This 16-page Du Pont publication explores in depth many of today's high-density printed circuit board design challenges, including:

• Reducing circuit size • Placing more circuits in the board area • Standardizing the board for modular application • Developing more effective conductor routing and more economical production techniques

What's more, you get plenty of solutions . . . from the manufacturers of RISTON® Photopolymer Dry Film Resist and VACREL™ Dry Film Solder Mask. New components . . . new materials . . . cost effective results—they're all here. For your copy, fill out and mail the coupon.

Du Pont Company
Marketing Communications Department
RISTON® Products Division, Room N-2526 F
Wilmington, DE 19898

Please send me a copy of "Designing High Density Printed Circuit Boards Cost Effectively."

Name _____ Title _____

Company _____ Phone _____

Address _____

City _____ State _____ Zip _____

Type of boards being designed _____

For use in _____

VISIT THE DU PONT BOOTH
AT NEPCON WEST, ANAHEIM, CA,
FEBRUARY 23–25, 1982.

An electronics company.

DU PONT
REG. U.S. PAT. & TM. OFF.

CIRCLE 13 ON INQUIRY CARD

WATCHING THE JAPAN WATCHERS

The media these days seem to be deeply concerned about losing the "next war" to our allies—the Japanese. The hue and cry is, Adopt Japanese management methods; train American employees to be more like their Japanese counterparts.

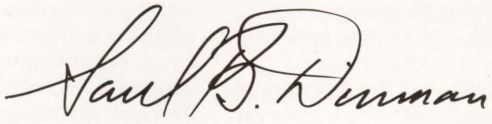
A paranoia is sweeping upper level management and the business, or "B," schools: Copy Japanese corporate and organizational techniques; impose them on U.S. industry. The pervasive attitude is a product of hysteria. After all, the great American automobile industry is about to become a dinosaur; we lost our manufacturing edge in radios, television sets, vacuum tubes, and cameras; the awesome Silicon Valley fortress has a breach in its outer wall. If you believe the bulk of what you read, the solution is simple: Adopt the Japanese way. It works for them; ergo, it should work for us.

But is it really that simple, or have I missed something? Or, have the originators of all those ideas missed something? Anyone who has ever attempted to negotiate an OEM contract with a Japanese executive discovers very quickly that something is radically different about the Japanese personality. The Japanese, the Germans, the French, and the English, as well as we Americans, are all products of our respective cultures. We possess attitudes, morals, and personalities that have been molded—in some cases, over millennia, not mere centuries.

Before the B schools start cranking out a new wave of samurai managers to deal with our industry, they should take a hard look at something in the electronics industry that is unique to the United States. Our industry was built mainly by forcing the frontiers of technology and the limits of people. The bulk of electronic innovations has come from us, and even if it was only our economy that allowed that to happen, it happened uniquely nonetheless. The spirit of entrepreneurship in the United States is duplicated nowhere else in the world. Where else can two people in a garage float a start-up investment with an idea and go on to become a Digital or an Apple? Where else do a handful of people work day and night, seven days a week, against the impossible odds of undercapitalization, established competition, and a skeptical market, and come out winners?

The question is not what Japanese managers do to achieve their results, but rather what happens to a U.S. company when it leaves its embryonic stage and becomes an established corporate entity. Where did the mind-set of the founders and the first wave of employees go when the professional managers came in? Why did the need to produce large volumes at low cost cause a "sweatshop" mentality to prevail? Where did the close personal ties that existed in the originating team of a business go when that team became a department? Why do employees eventually develop "9 to 5" and job hopping mentalities even though they are working on concepts that offer the same mental stimulus that drove the founders of a business to success?

Perhaps the answers to all of these questions lie a lot closer to the B schools than they would care to admit. Perhaps it's related to the case study method that attempts to treat businesses as mathematical formulas, without any terms in the equation for people as individuals. Or, perhaps it's related to time and motion studies, in which people's inputs are reduced to elementary equations with no terms for John's depression or Mary's temporary trauma. If anything is to be learned from our Japanese brothers, I hope it's the attitude that human beings need human contact, nurturing, and stroking; that "saving face" is a lot more than a cultural quirk—it's a concept of human relations that transcends and eliminates corporate politics; that bottom line management is all well and good, but when one of the expenses is people—as opposed to people's salaries—the bottom line is bound to suffer.



Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—July
"Low Cost Alternative to Hamming Codes Corrects Memory Errors"
Lee Edwards, NCR Corporation

This article will now compete with other monthly winning articles for the 1981 Windjammer cruise award.

TEK DAS 9100 DIGITAL ANALYSIS SYSTEM

Tektronix introduces 132 state of the art logic analyzers, in one.

A new concept in logic analysis.

Now you can have a single logic analysis system that is both configurable and upgradable. All with unprecedented performance and flexibility.

It's the DAS 9100. A single mainframe that houses up to six card modules. With acquisition speeds up to 660 MHz, timing resolution down to an unprecedented 1.5 ns, data widths up to 104 channels and synchronous or asynchronous operations.

And for the first time, you can combine *pattern generation with data aquisition*. Pattern generation provides stimulus data widths up to 80 channels and speeds up to 25 MHz.

Need I/O capability? There's an option that adds RS-232, GPIB and hard copy interface. And another for a built-in magnetic tape drive system.

Select your own width and speed combination, for data acquisition.

DAS 9100 gives you four different data acquisition modules to use as building blocks. Each has its own data width and maximum speed: 32 channels at 25 MHz; 8 channels at 100 MHz with glitch memory; 4 channels at 330 MHz or two channels at 660 MHz. Modules can be combined to give you the performance you need.

Need high speed performance? One module can track your system clock (synchronously) at speeds up to 330 MHz or provide asynchronous sampling to 660 MHz. The eight channel module provides *both* synchronous and asynchronous sampling at 100 MHz. And the 32 channel module can be used to arm the trigger on those with higher acquisition rates.

To obtain the data width and speed your application calls for, simply select the appropriate combination of modules and add on later as your needs change.

To back it all up, there's powerful triggering, programmable reference memory and multiple clocks. Plus glitch triggering, with a separate glitch memory for

unambiguous glitch detection and our unique, new "arms mode" allows timing correlation between synchronous and asynchronous data.

DAS 9100 integrates the power of pattern generation with data acquisition.

At last, you can have a tool that covers your digital system debugging needs. By combining pattern generation and data acquisition modules, you can stimulate your prototype while simultaneously analyzing its operation. Allowing you to enter a whole new dimension of design analysis and verification.

Pattern generation capability is built around a 16 channel, 25 MHz module. Through additional expansion modules, you can raise the total to 80 channels while maintaining full system speed. The pattern generator allows interaction with the prototype through data strobe outputs and external control inputs, including an interrupt line. The generated pattern can even be changed based on the data acquired by the logic analyzer.

The DAS 9100 lets you start debugging hardware even before your software is available. Pattern generation makes it all possible.

With plenty of room for mainframe options to fit your application.

A powerful I/O option adds RS-232, GPIB and hard copy interace for full remote programmability. A built-in magnetic tape drive using DC-100 cartridges is also available, so you can save whole or partial instrument setups for recall. Pattern generation routines and reference memory data also can be stored.

DAS 9100 easy-to-use keyboard and menus tie it all together.

Operation of your DAS 9100 is simple and straightforward. Selectable menus help you set up trigger conditions, select data formats, and define voltage thresholds. You can even define your own mnemonics to fit the data under test.

How does it all go together?

In whatever combination your application calls for, or choose one of these pre-configured packages from Tektronix:

The DAS 9101. 16-channels of data aquisition at 100 MHz.

The DAS 9102. 32-channels of data aqusistion at 25 MHz plus 16-channels of pattern generation.

The DAS 9103. 32-channels of data aquisition at 25 MHz plus 8 more channels at 100 MHz. And 16-channels of pattern generation.

The DAS 9104. 80-channels of data aquisition, with 64-channels at 25 MHz and 16-channels at 100 MHz. Plus a 16-channel pattern generator with a built-in DC-100 magnetic tape drive.

Backed by Tektronix support.

You get a world-wide service organization, extensive documentation and applications assistance.

Contact your Tek Sales Engineer for more information. Or call us toll-free. 1-800-547-6711, in the U.S. In Oregon, 1-800-452-6773.

For further information, contact:

U.S.A., Asia, Australia, Central & South America, Japan Tektronix, Inc., P.O. Box 4828, Portland, OR 97208, Phone: 800 547-6711, Oregon only 800 452-6773, Telex: 910-467-8708, Cable: TEKTRONIX

Europe, Africa, Middle East Tektronix International, Inc., European Marketing Centre, Postbox 827, 1180 AV Amstelveen, The Netherlands, Telex: 18312

Canada, Tektronix Canada Inc., P.O. Box 6500, Barrie, Ontario L4M 4V3, Phone: 705 737-2700

FLEXIBLE SOLUTIONS
FOR A FUTURE OF CHANGE

The One. Digital Analysis System.

Tektronix
COMMITTED TO EXCELLENCE

Circle 8 for Literature
Circle 9 for Sales Contact

COMPUTER DESIGN

Publishing Staff
Publisher
Ronald W. Evans

Editorial
Editor in Chief
Saul B. Dinman
Managing Editor
Sydney F. Shapiro
Technical Editor
Christopher J. Brown
Senior Editors
Peg Killmon
James W. Hughes
Associate Editor
Colleen G. da Silva
Senior Copy Editor
Debra M. Highberger
Copy Editors
Jun U. Smith
Mary Therese Cipar
Editorial Assistant
Colleen Feeney
Editorial Adviser
Rex Rice
Western Editorial Staff
540 Weddell Drive, Suite #8
Sunnyvale, CA 94086 Tel. (408) 745-0715
Managing Editor
Tom Williams
Senior Editor
Doug Eidsmore

Circulation
Circulation Director
Robert P. Dromgoole

Production
Production Manager
Linda M. Wright
Asst. Production Manager
Lou Ann Sawyer
Graphics Coordinator
Debbie Brady
Design Consultant
Ken Silvia Design Group
Technical Art
Concepts Unlimited

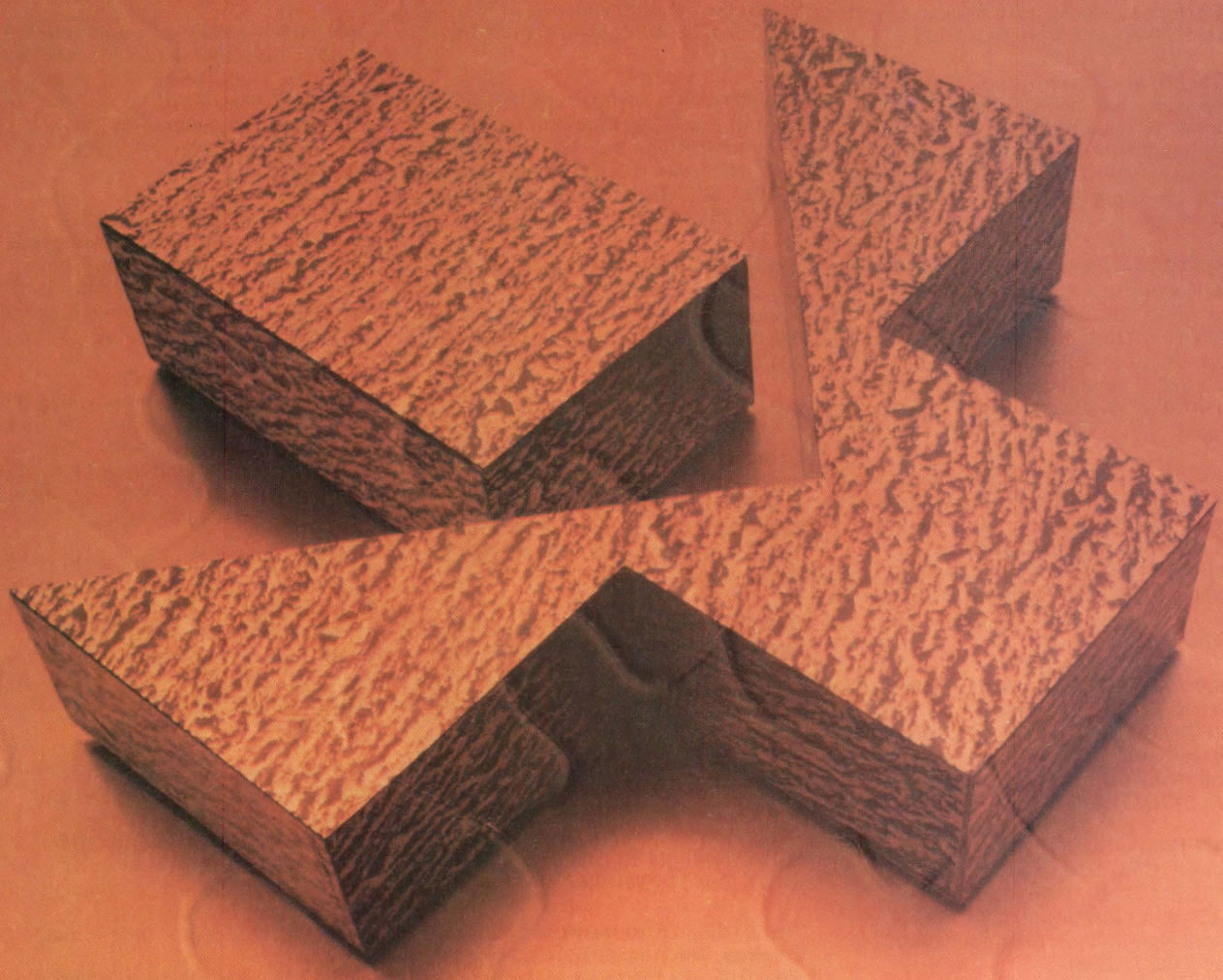
Marketing
Director of Marketing
Gene Pritchard
Marketing Services/P.R. Manager
Linda G. Clark
Promotion Manager
Tom Hodges
Advertising Coordinators
Cherie Crosby
Sally H. Bowers

Financial
Controller
David C. Ciommo

Computer System
Director
Wayne Newman
Data Services Manager
Wanda Holt
Data Services Assistant
Sue Bowker

Editorial & Executive Offices
11 Goldsmith St, Littleton, MA 01460 Tel. (617) 486-8944/(617) 646-7872
Editorial manuscripts should be addressed to Editor, Computer Design, 11 Goldsmith St., Littleton, MA 01460. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."

All the pieces are in place.



Our computers set the pace.

We've become an integral part of the Gould electronics and electrical family and changed our name to Gould Inc., S.E.L. Computer Systems Division. Everything's in place and it fits perfectly.

While you won't be seeing the name SYSTEMS, our dedication to high-performance, real-time computation hasn't changed. You'll see our new face, but not any difference in operating philosophy. In fact, as one of the key elements in Gould's building block strategy for high-technology electronics markets, our growth and our impact will be even greater. Being Gould S.E.L. will increase our capabilities and strengthen our leadership position in the 32-bit minicomputer marketplace.

Our continuing efforts, coupled with the additional expertise and resources available, allow us to serve you even better than before. By advancing present products. Accepting new challenges. Reaching new markets. You can look for realistic, sustained growth. Growth that reaffirms our commitments to you.

Check out our new identity. All the pieces are now in place. And, Gould S.E.L. is the right place to go for all your computational needs.

Gould Inc., S.E.L. Computer Systems Division,
6901 West Sunrise Boulevard,
Fort Lauderdale, Florida 33313. 1-305-587-2900.

GOULD

Electronics & Electrical Products

CIRCLE 12 ON INQUIRY CARD

CALENDAR

CONFERENCES

JAN 3-8—Annual Meeting of AAAS, Washington, DC. INFORMATION: American Assoc for the Advancement of Science (AAAS), 1515 Massachusetts Ave NW, Washington, DC 20005

JAN 11-13—Western Conf and Expo, Anaheim, Calif. INFORMATION: Col Richard G. Deem, Armed Forces Communications and Electronics Assoc (AFCEA), Skyline One, Suite 300, 5205 Leesburg Pike, Falls Church, VA 22041

JAN 12-14—Communications Networks Conf and Expo, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: Bill Leitch, CW Conf Mgmt Group, 375 Cochituate Rd, PO Box 880, Framingham, MA 01701. Tel: 617/879-0700; 800/225-4698 (outside Mass)

JAN 14 AND FEB 10—Invitational Computer Confs, South Coast Plaza Hotel, Orange County, Calif; and Pier 66 Hotel, Ft Lauderdale, Fla. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

JAN 18-21—ATE Seminar/Exhibit, Pasadena Ctr, Pasadena, Calif. INFORMATION: Elaine Bull, Promotion Coordinator, ATE Seminar/Exhibit, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JAN 19-21—SOUTHCON, Orange County Conv Ctr, Orlando, Fla. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

JAN 20-22—Texas Computer Show, Dallas Conv Ctr, Dallas, Tex. INFORMATION: Catherine Manor, Texas Computer Show, PO Box 214035, Dallas, TX 75221. Tel: 214/761-9108

FEB 10-12—Internat'l Solid State Circuits Conf, Hilton Hotel, San Francisco, Calif. INFORMATION: L. Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 21-23—Non-impact Printing Technologies Data Base Access Meeting, Sheraton Fisherman's Wharf, San Francisco, Calif. INFORMATION: Linda M. Tempero, Advanced Technology Resources Corp, 6256 Pleasant Valley Rd, El Dorado, CA 95623. Tel: 916/626-4104

FEB 22-25—COMPCON Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAR 22-25—Interface '82 Nat'l Conf and Expo for Data Communications/ DDP/Networking, Dallas Conv Ctr, Dallas, Tex. INFORMATION: The Interface Group, PO Box 927, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

MAR 30-APR 1—INFOCOM '82, Joint Conf of the IEEE Computer and Communications Society, Las Vegas, Nev. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

APR 21-28—Hanover Fair, Hanover, West Germany. INFORMATION: Hanover Fairs Information Ctr, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044; 800/526-5978 (outside NJ)

SEMINARS

Datapro Seminars, various U.S. cities and dates. INFORMATION: Joseph F. Menendez, Mgr, Seminar and Conf Operation, Datapro Research Corp, 1805 Underwood Blvd, Delran, NJ 08075. Tel: 609/764-0100

Digital Seminars, various U.S. cities and dates. INFORMATION: Educational Services, Digital Equipment Corp, U.S. Marketing Group BU/E55, 12 Crosby Dr, Bedford, MA 01730. Tel: 617/276-4111

Data Communications for Minicomputer Users, various U.S. cities and dates. INFORMATION: Seminar Administrator, Micom Systems, Inc, 20151 Nordhoff St, Chatsworth, CA 91311. Tel: 213/998-8844

JAN 21-22—Local Network Equipment Seminar, The Adams Hilton, Phoenix, Ariz. INFORMATION: Architecture Technology Corp, PO Box 24344, MN 55424. Tel: 612/935-2035

MAR 9-11—Internat'l Zurich Seminar on Digital Communications, Swiss Federal Institute of Technology, Zurich, Switzerland. INFORMATION: Secretariat 82 IZS, Miss M. Frey, EAE, Siemens-Albis AG, CH-8047 Zurich, Switzerland. Tel: +41-1-247 51 20

SHORT COURSES

Courses for Developers and Users of Computer Systems, various U.S. cities and dates. INFORMATION: American Management Assocs, Information Systems & Technology Div, 135 W 50th St, New York, NY 10020. Tel: 212/586-8100

Hellman Assocs Tutorial Courses, various U.S. cities and dates. INFORMATION: Hellman Assocs, 299 S California Ave, Palo Alto, CA 94306. Tel: 415/328-4091

IEEE Continuing Education Courses, various U.S. cities and dates. INFORMATION: Continuing Education Dept, IEEE Service Ctr, 445 Hoes Ln, Piscataway, NJ 08854. Tel: 201/981-0060

JAN 11-13—Design of Fault Tolerant (Highly Reliable) Microprocessor Based Systems, The Frederic Ctr, Madison, Wisc. INFORMATION: Avi Vaidya, U of Wisconsin-Extension, Rm 741, 432 N Lake St, Madison, WI 53706. Tel: 608/262-8592

JAN 11-15—Applied Interactive Computer Graphics, U of Tennessee Space Institute, Tullahoma, Tenn. INFORMATION: Jules Bernard, U of Tennessee Space Institute, Tullahoma, TN 37388. Tel: 615/455-0631

JAN 19-22—Peripheral Array Processors for Signal Processing & Simulation, Sheraton National Hotel, Washington, DC. INFORMATION: Continuing Education Institute, 10889 Wilshire Blvd, Suite 1030, Los Angeles, CA 90024. Tel: 213/824-9545

JAN 26-29, MAR 9-12, and APR 20-23—VIO-Voice Input/Output for Computers, Washington, DC; Los Angeles, Calif; and Boston, Mass. INFORMATION: Ruth Dordick, Integrated Computer Systems, 3304 Pico Blvd, PO Box 5339, Santa Monica, CA 90405. Tel: 213/ 450-2060

FEB 16-19—Intelligent Robots: The Integration of Microcomputer and Robotic Technology, George Washington U, Washington, DC. INFORMATION: Director, Cont Engineering Ed, George Washington U, Washington, DC 20052. Tel: 202/676-6106; 800/424-9773 (outside DC)

FEB 17-19—Practical CAD/CAM Considerations (Concept Through Operation), U of Calif, Los Angeles, Calif. INFORMATION: Sylvan H. Chasen, Univ Extension, Cont Ed in Engineering and Mathematics, 6266 Boelter Hall, UCLA, Los Angeles, CA 90024. Tel: 213/825-1047

FEB 25-27 and MAR 1-3—Digital Electronics for Instrumentation; and Microcomputer Interfacing Design and Programming, Virginia Polytechnic Inst and State U, Blacksburg, Va. INFORMATION: Dr Linda Leffel, CEC, Virginia Polytechnic Inst and State U, Blacksburg, VA 24061. Tel: 703/961-4848

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance.

A FULL SPECTRUM OF CHOICES IN DEC-COMPATIBLE DISK STORAGE:

And now a new 32.2-Mb Winchester/Floppy System

DATA SYSTEMS DESIGN

More disk storage choices than you get from DEC.

disk cartridge drives plus bootstrap card, and you'd pay about twice the cost of one DSD 880. Plus, you'd give up the high reliability of the DSD 880's winchester technology—a state-of-the-art choice DEC doesn't even offer LSI-11 and PDP-11 users. And you'd have three ungainly boxes over 30 inches high—as compared with the DSD 880's compact 5¼-inch panel height, which saves you rack space and cabinetry costs and allows use in space-critical applications.

Whether you choose the 32.2, 21.8 or 8.8 megabyte winchester/floppy system, your disk system is more cost-effective than any comparable DEC disk drive or combination.

The hardware bootstrap is built right into the interface so you don't have to pay extra for a separate board.

The DSD 880 interfaces require 70% less backplane space than equivalent DEC configurations.

And the HyperDiagnostic™ panel simplifies troubleshooting for cost-effective remote diagnosis.

Fully compatible three ways.

The DSD 880 is hardware-compatible. It integrates with any DEC LSI-11 or PDP-11 computer-based system. Combine the DSD 880 with a VT103 containing an LSI-11/23 and you've got a complete, powerful table-top microcomputer with up to 32.2 megabytes of storage.

Software compatibility is no problem either. You can use your RT-11 or RSX-11 operating systems with RL01 or RL02 (winchester) and RX02 (floppy) handlers. With no modifications at all. And the DSD 880 runs all applicable DEC diagnostics and utilities.

It's media-compatible, too. DSD floppies can use either DEC double-density or IBM single-density formats.

With its higher capacities, smaller size, lower cost and more, the DSD 880 gives your DEC computer-based system the disk storage it deserves.

DEC designs great CPUs. Data Systems Design gives you disk storage to match.

For CPU quality, you can't beat DEC's LSI-11 and PDP®-11. But their disk storage doesn't always measure up. At Data Systems Design, data storage is our *only* concern. That's why our DEC®-compatible disk systems are more reliable, less expensive, more compact and easier to maintain than the disk systems you get from DEC.

And you get more choices of systems, too, so you can pick the exact features your product application requires.

DSD 880 gives you more megabytes per buck for your PDP-11 and LSI-11.

With the addition of a new DSD 880 version, you now have three choices in winchester disk storage: 31.2, 20.8 or 7.8 megabytes. Each with a choice of 0.5 single- or 1-megabyte double-sided floppy backup. More capacity for less cost-per-megabyte than any comparable DEC alternative.

To match the capacity of the DSD 880's 31.2-megabyte winchester disk, for example, you'd need three DEC RL02

A choice of 4 floppy systems.

Pick the features you need. Data Systems Design gives you more choices in DEC-compatible floppy disk systems, too.

Each of the four floppy systems is packaged in a low-profile 5¼-inch chassis. All offer built-in hardware bootstrap and complete DEC RX02 compatibility, plus a choice of domestic or international configurations, and complete documentation for easy system integration.

DSD 480 provides double-sided floppy storage for your LSI-11 or PDP-11.

For twice the capacity of DEC's RX02, choose the DSD 480. An optional EXCHNG™ software program lets the DSD 480 transfer files between IBM- and DEC-generated diskettes.

DSD 470 gives you low-cost double-sided floppy storage for your LSI-11.

The DSD 470 is software compatible and can be configured for single- or double-sided diskettes. And its single-board controller/interface* has far fewer parts than separate boards for better space utilization and improved reliability.

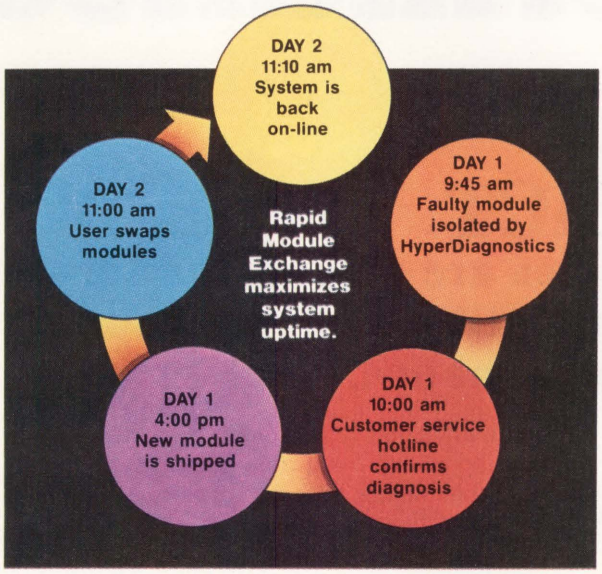
Choose DSD 440 for single-sided floppy storage with your LSI-11 or PDP-11.

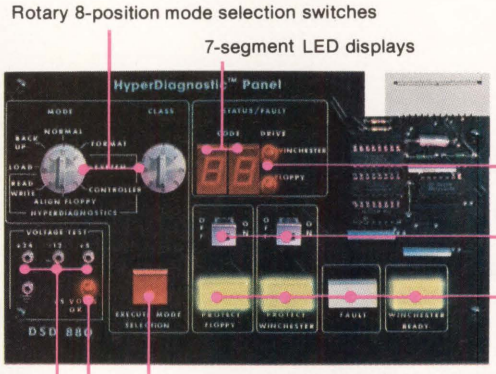
The DSD 440 is RX01 and RX02 software-compatible. It can transfer data 20% faster than DEC's RX02, and features built-in self-diagnostics for easy servicing.

Choose DSD 430 for lowest entry cost with your LSI-11.

With 2 single-sided floppy drives, the DSD 430 gives you full RX02 compatibility and complete LSI-11/23 four-level interrupt support.

More reliable performance and easier maintenance.





DSD 880 HyperDiagnostic™ Panel

A revolutionary concept in uptime: Remote diagnosis ends costly service calls.

The true measure of a system is its ability to perform. Day after day, reading and writing data on demand. Data Systems Design units outlast any other disk system on the market. But even the most rugged system has an occasional problem. And that's when Data Systems Design really shines.

You know the usual service scenario. There's a problem, so you call the service rep. And wait for a return call. Then you wait for someone to show up. And every minute is costing money, in addition to the high cost of the service contract itself.

Data Systems Design ends all that with the service system that will soon be the industry standard: remote diagnosis.

HyperDiagnostics,™ standard on the DSD 440, 480 and 880, allow the user to test, exercise and debug without a CPU or a service call. Easy-to-use controls activate microprogrammed routines, and LED indicators designate fault status. On the 430 and 470, ODT-driven self-diagnostics and software diagnostics assist in troubleshooting.

A call to our service hotline gets instant back-up and confirmation of the diagnosis.† Our service records show that over 20% of the problems are fixed over the phone, with no service needed.

When a faulty module is isolated, **Rapid Module Exchange**™ gets the user back on-line faster than a service call. Thanks to our system's modular design, the user simply swaps modules after consultation with a hotline advisor. We usually ship out a new module the same day a failure is diagnosed in a specially-designed reusable carton for easy return of the original module.

For less than half the cost of a DEC service contract, our **HyperService**™ option extends warranty protection for one year beyond the standard 90 days and covers factory repairs and Rapid Module Exchange Service.

At Data Systems Design, we have carefully considered every step in the process to make service as easy and cost-effective as possible.

Get the disk storage you deserve for your DEC-based system.

For full technical details, write Data Systems Design, Inc., 2241 Lundy Avenue, San Jose, CA 95131, or call the sales office nearest you.

United States: Western Region (408) 727-3163; Eastern Region (617) 769-7620.

International: Australia: Melbourne 03/543-2077, Sydney 02/848-8533; Canada 416/625-1907; Denmark 01/83 34 00; Finland 90/88 50 11; France 03/956 81 42; Israel 03/298783; Italy 02/4047648; Japan 06/323-1707; Netherlands 020/45 87 55; New Zealand 4/693-008; Norway 02/78 94 60; Sweden 08/38 03 70; Switzerland 01/730 48 48; United Kingdom 01/207-1717; West Germany and Austria 089/1204-0.

*This controller/interface is also available separately as the DSD 4140.

†Although these services are available within the U.S.A. only, comparable service is available through our international distributors.

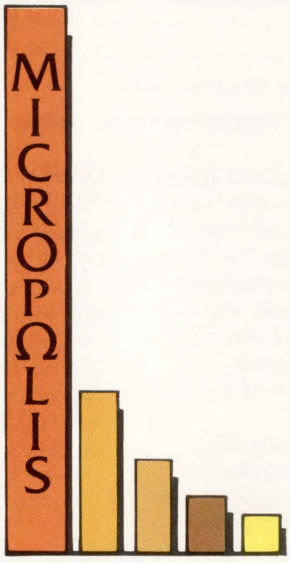
Circle 101 for DSD 880 information.
Circle 102 for DSD 480 information.
Circle 103 for DSD 470 information.
Circle 104 for DSD 440 information.
Circle 105 for DSD 430 information.

Data Systems

Some plain high performance

FACT: We've delivered more 45 Mbyte 8" Winchesters than all the competitors put together.

A 50,000 square foot plant with the finest clean rooms money can buy is totally dedicated to producing high capacity, high performance drives. Plant capacity exceeds 2000 drives monthly. Availability questions about high capacity, high performance 8" Winchesters are a thing of the past. The only question left is - how many would you like – and when.



COMPETITORS

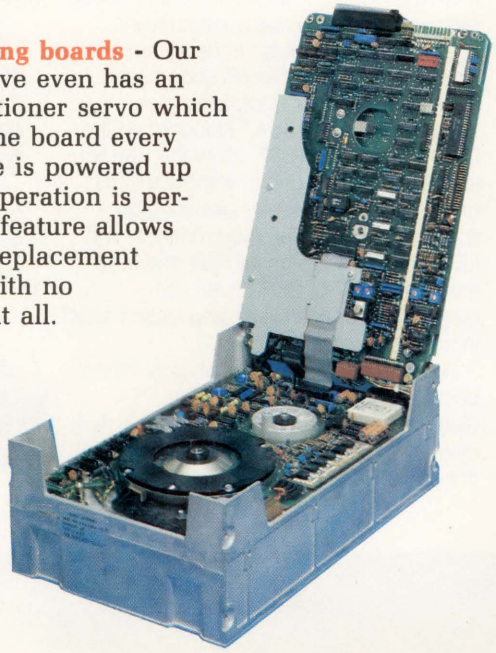
FACT: Micropolis drives are engineered for reliability, stability and performance.

We pay close attention to the clean area, but there's more. Designed in are features which make ours the most reliable, stable high performance 8" Winchester on the market.

• **Quartz locked direct drive motor** - A unique Quartz crystal speed control circuit holds rotational accuracy to better than 0.5%, which allows 5% more data on the drive. The high efficiency brushless dc motor eliminates two main shortcomings of line voltage induction motor/belt drives - excessive power and heat, and double inventorying for 50/60 Hz requirements.

• **Fail-safe braking mechanism** - Micropolis doesn't agree with those who feel it's good engineering to let the head slow the disk by friction. Instead, we extend the life of our disks by including a spring loaded brake that stops the motor in seconds.

• **Self-adjusting boards** - Our intelligent drive even has an adaptive positioner servo which recalibrates the board every time the drive is powered up or a restore operation is performed. This feature allows quick board replacement in the field with no adjustments at all.



FACT: Critical components start out only in the clean room.

Recording heads, platters and voice coil positioner start out in the clean room and are never exposed to contaminated air. They're completely sealed in the lower half of the drive with pure air circulated through a 0.3 micron life-time filter. All active components are kept out of this sealed area, resulting in a clean area MTBF of 25,000 hours. Some manufacturers include active components in the sealed area, creating nightmares for field service.

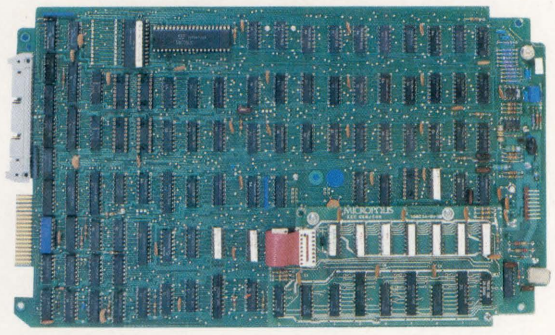
facts about 8-inch Winchesters

• **Truly balanced positioner** - A balanced rotary voice coil mechanism combines with a closed loop servo to continuously monitor head position, removing the danger of off-track writing inherent in stepping motor systems. Also, drives using non-rotary voice coils or stepper positioners are vulnerable to even very low levels of shock and vibration.

• **Latches and locks hold head in place** - Heads always land in the non-data area and are latched in a safe position even when the drive is moved from desk to desk. A special lock protects against higher shocks during shipping and is unlocked manually for installation.

FACT: Micropolis' optional Intelligent Controller can save you time and money.

Why spend valuable development time and money designing a controller from scratch when we've already done it for you. Our Intelligent Controller board fits inside the drive, gives you 922 Kbyte data transfer rate, sophisticated EPM data separation, up to 1 Kbyte of buffering and 5 bits of error correction.



Even with all of this, the controller costs less than $400 in OEM quantities. As a further economy, each master drive with Intelligent Controller can handle up to three additional slave drives. Drive interfaces are also available for SMD, ANSI and SA 1000.

FACT: Militarized computers use our drive.

Thanks to our inherent reliability, customers such as Rolm Computer and Miltope Corporation buy Micropolis drives for their militarized computer systems. Solid, rugged construction means long life and low maintenance costs in your less hostile environment.

FACT: On the horizon, 90 and 180 Mbyte 8" Winchesters.

We're at 45Mbytes and climbing. We plan to introduce three more 8" models by the end of 1982 with storage capacities of 60Mbyte, 90Mybte and 180Mbyte. The new models will help maintain our leadership position in the high capacity, high performance over-30Mbyte market.

If a solidly engineered high performance 8" Winchester plays a role in your design plans, phone or write for more "plain facts".

MICROPOLIS™

21329 Nordhoff Street
Chatsworth, CA 91311
(213) 709-3300 • Telex 651486

Growth positions available for talented people.

OUR CMOS EPROM WE'VE GOT YOUR

COLLECTION: SIZE AND PRICE.

TREND-SETTING EPROMS.

Intersil is the CMOS EPROM trend-setter. First in 4K, and now in 8K too. Adding to our lead in the fashionable technology for the '80s.

Whether you're in program development or volume production, try on our 8K IM6657/58 (2048×4 and 1024×8, respectively) for size. They're compatible with the CMOS ROMs you're now using, including our IM6316 16K ROM, and with our IM6653/54 4K CMOS EPROMs.

LOW ACTIVE OPERATING POWER.

When it comes to low current requirements, our EPROMs are a cut above the rest. Only 100μA standby, and active current that decreases with lower operating frequencies. So battery life can increase 100-fold in your low-power applications.

FASHIONABLY FAST.

Our EPROMs meet and surpass NMOS EPROM speeds, while adding the CMOS advantages of low power, increased reliability, and lower system cost. At 5V, access time is a 1MHz-compatible 450ns. And if you need speed at higher system voltages, our 10V "A" version gives you a 300ns access.

WE'VE GOT YOUR STYLE.

Choose our industrial line, with a temperature range of −40°C to +85°C. Or we can tailor your order to military specifications. With 883B processing and full temperature range of −55°C to +125°C.

EASY TO PROGRAM.

All our CMOS EPROMs can be programmed by any standard EPROM programmer with the proper personality module. Or, you can get a dedicated 6920 CMOS EPROM programmer from us. After all, we're the leader in CMOS EPROMs.

AVAILABLE NOW. OFF THE RACK.

The new 8K CMOS EPROM dramatically expands Intersil's EPROM production. Both 4K and 8K CMOS EPROMs are in stock. Call or write for our EPROM data sheets and a delivery quotation. Whatever your CMOS ROM or EPROM needs, chances are we've got your size.

INTERSIL FRANCHISED DISTRIBUTORS:

Advent (IN, IA) • Alliance • Anthem • Arrow • Bell Industries • Cadence • Cardinal • CESCO • Component Specialties • Components Plus • Diplomat (FL, MD, NJ, UT) • Harvey (upstate NY) • Kierulff • LCOMP • Newark • Parrott • R.A.E. Ind. Elect. Ltd. • RESCO/Raleigh • Schweber • Summit • Western Microtechnology • Wyle • Zentronics

INTERSIL SALES OFFICES:

CALIFORNIA: Sunnyvale (408) 744-0618 • COLORADO: Aurora (303) 750-7004 • FLORIDA: Hollywood (305) 920-2442 • ILLINOIS: Hinsdale (312) 986-5303 • MASSACHUSETTS: Lexington (617) 861-6220 • MINNESOTA: Minneapolis (612) 925-1844 • NEW JERSEY: Englewood Cliffs (201) 567-5585 • TEXAS: Dallas (214) 369-6916 • CANADA: Brampton, Ontario (416) 457-1014

INTERSIL

DIGITAL PRODUCTS—MEMORY
10710 N. Tantau Avenue
Cupertino, CA 95014
Tel: (408) 996-5000
TWX: 910-338-0171

Dear Intersil:

_____ Dress me in style. Rush me data sheets on your _____ IM 6653/54 4K EPROMs
_____ IM 6657/58 8K EPROMs.

My annual EPROM usage is approx. _____ units.
My EPROM application is _____.

Name _____

Company _____

Address _____

City/State/Zip _____

Phone _____

☐ Please send me a free Shakespeare poster from your "Famous Quotations" ad series.

CD1281

Modular remote data acquisition and control system has twisted pair wiring

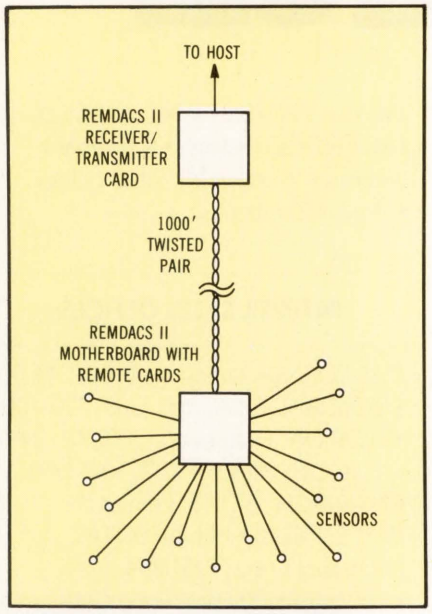


Fig 1 REMDACS II configuration. Remote analog cards include position potentiometers, transducers, thermocouples, and semiconductor temperature probes. Digital cards include pressure switches, switch closures, circuit breakers, solenoids, and contactors. Twisted pair reduces installation costs

Modular remote data acquisition and control system with twisted pair wiring, REMDACS II™ uses preprogrammed microcomputer controlled cards located near a signal source or control point. Remote analog, digital, and digital-peripheral cards are linked to a control receiver/transmitter card through a single twisted pair of wires. The receiver/transmitter provides serial digital current loop communications with the remote cards. Four cards provide the host computer interface: RS-232-C, STD-BUS, Multibus, and a general purpose data bus card. A simple system diagram is shown in Fig 1.

The remote card family offers options for specific analog sensing or digital functions. Analog cards measure voltage, current, temperature, or 4- to 20-mA current loop signals. Accommodating most common sensors, the remotes handle transducers, potentiometers, resistance-temperature devices, semiconductor temperature sensors, strain gauges, bridges, thermocouples, and transmitters. Onboard circuits perform scaling, signal conditioning, multiplexing of up to 16 channels, and 12-bit A-D conversion.

Digital remote cards supply up to 36 I/O signals per station. One remote card interfaces directly with low level TTL signals or with compatible peripheral cards for monitoring contact closures, sensing power levels, setting alarm limits, or controlling ac power and heavier loads.

A series of compatible motherboards configured specifically for installation of analog and digital cards supports the remote cards. Each remote card is compatible with the REMDACS II motherboard termination system (RMBTS). The motherboards are two modular interconnect systems; the analog motherboard is available in one through four slots, and the digital motherboard is available in two through five slots. Both motherboards are compatible, allowing expansion to 256 remote stations per twisted pair or receiver/transmitter. Edge connectors and card guides are provided for seating the cards, while 3-terminal Weidmuller barrier connectors are provided for direct interface with external signals. Ribbon connectors are available for interface between cards. In addition, electrical and mechanical connectors allow interconnects between multiple analog or digital motherboards. All connectors are UL and CSA approved.

REMDACS II is transparent to the central processor, which sees the system as a data source or control device. The receiver/transmitter card handles all communications with up to 256 remote stations and supplies data to the host computer via a parallel bus or through an RS-232-C interface.

Upon command from the host, the receiver/transmitter formats the message, inserts communication bits, and polls the remote stations. Moreover, the receiver/transmitter decodes the remote's response, removes communication bits, and prepares the data for the host. Both remote cards and the receiver/transmitter cards automatically error-check messages transmitted between them. Receiver/transmitter station is shown in Fig 2.

Several digital peripheral cards are available, and more will be available soon. The present cards are 8-channel electromechanical relays and 8-channel solid state relays with LED status indication, 4-channel electromechanical relays and 4-channel solid state relays with switch override and LED status, and an 8-channel active logic input card for ac or dc voltage detection from 5 V to 230 V rms. A universal breadboard card is also available for dedicated customer applications.

Both the analog and digital remote stations come standard with a 24 Vac input, making them compatible with UL requirements. If the 2500 V station to station isolation is not required and a dc power supply system is preferable, the remote stations are available with an 8 to 20 Vdc input. **Intersil Inc**, 10710 N Tantau Ave, Cupertino, CA 95014.

Circle 240 on Inquiry Card

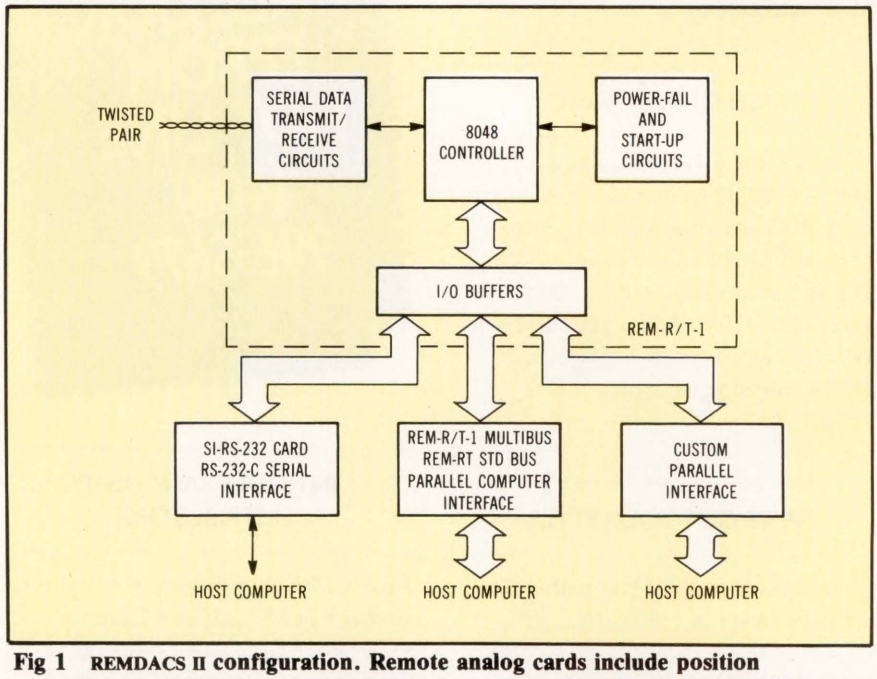
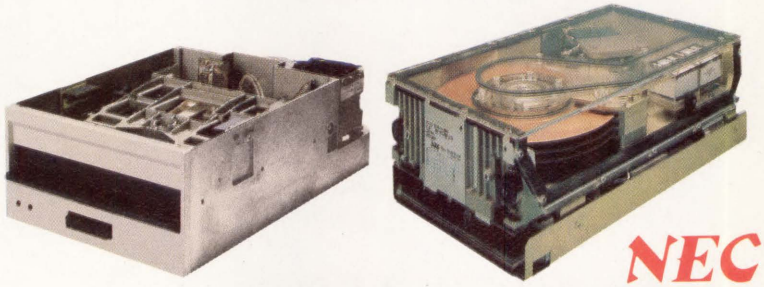


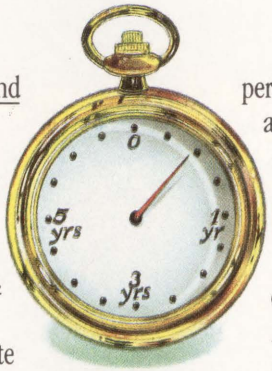
Fig 1 REMDACS II configuration. Remote analog cards include position potentiometers, transducers, thermocouples, and semiconductor temperature probes. Digital cards include pressure switches, switch closures, circuit breakers, solenoids, and contactors. Twisted pair reduces installation costs

Fatten your profits with NEC disks.



NEC

NEC Information Systems, Inc.



Our Soft-Touch 8-inch diskette drive has a mean time between failure of 15,000 hours. That's nearly 5 years of normal use.

They're less expensive going in, and that's only the beginning.

Our disks also give you extra margins which no competitive products can touch. Here's how.

Built-in quality plumps up profits.

Take our NEC Soft-Touch™ dual-sided double-density 8-inch diskette drive. It gives you a media life of more than six million passes, nearly double that offered by other suppliers. The entire drive has a field-proven mean time between failure (MTBF) of 15,000 hours, nearly twice the industry average.

NEC technologically reduced the parts in our high-performance 8-inch Winchesters. As a result, we eliminated the need for periodic maintenance, extended MTBF to more than 12,000 hours (about five years of normal operation), and cut mean time to repair (MTTR) to 30 minutes.

Our 14-inch, 317 mega-byte high-performance Winchester has a field-proven 10,000-hour MTBF and an MTTR of only one hour. Plus, it offers optional off-line microprocessor-diagnostic capability.

All of this translates to the kind of value you take to the bank.

Our 15 years of disk-building experience pays off.

We know disks, we know how to build them, and we know how to keep them running. As a result, we've got features in our disks that give you, and your customers, years of hassle-free service.

As a first step to fattening your profits...

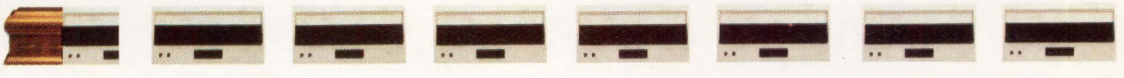
Send for information on NEC disks, or call your nearest NEC sales office.

NEC Information Systems, Inc.
5 Militia Drive, Lexington, MA 02173

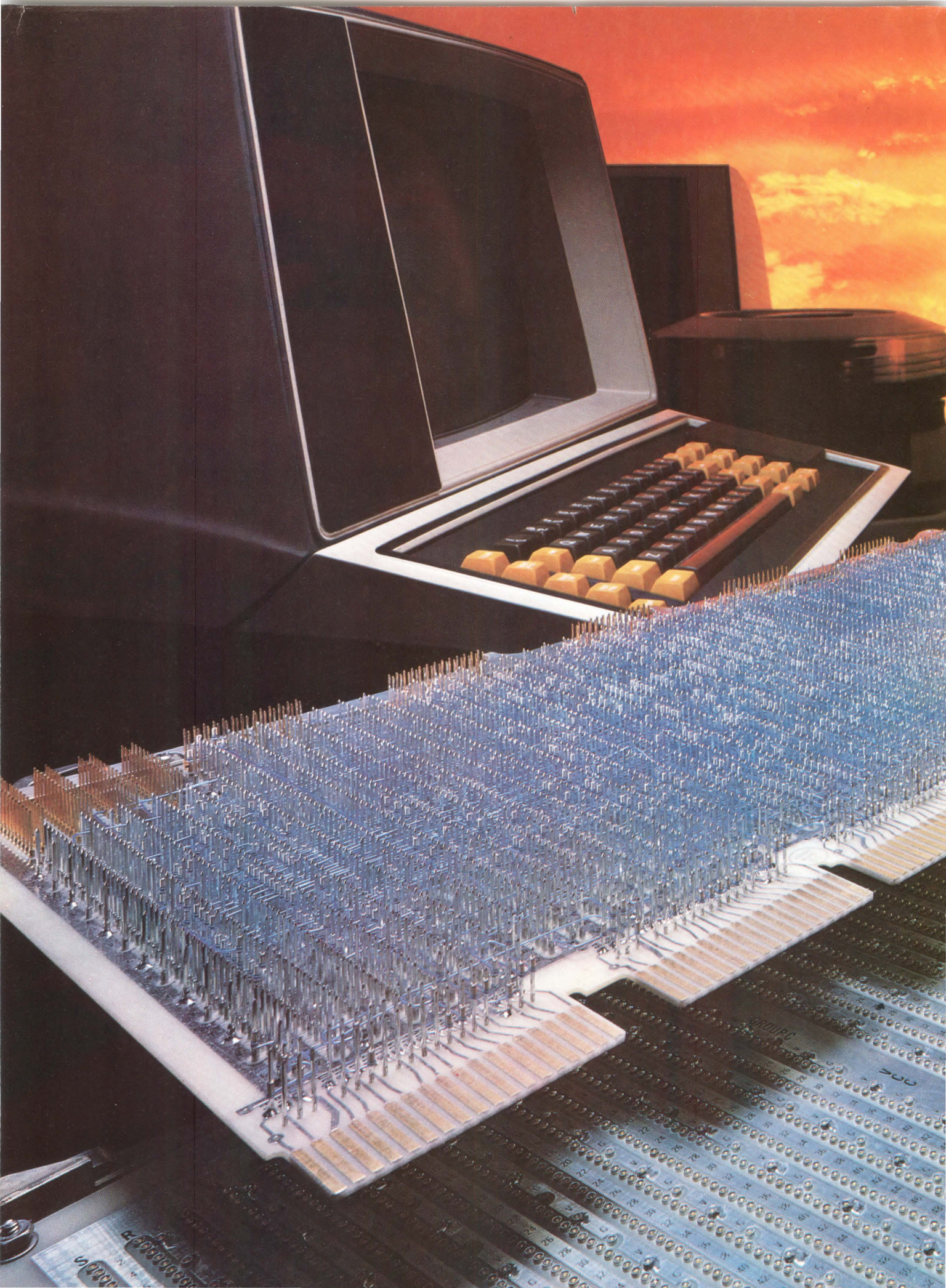
Because we manufacture almost every part in all our disks, we can assure the high tolerance engineering, rigid quality control in selection of raw materials, and attention to production details that guarantee you years of trouble-free operation.

Our significantly better diskette drive DOA rate reduces test and inspection time, saving you hundreds of dollars.

NEC Soft-Touch™ DOA rate: practically nil.



Other diskettes' DOA rate: as much as 10%.



The many interfaces of Augat.

Augat Wire Wrap* interface panels make it easy to connect with all the big names in the minicomputer industry. Digital Equipment Corporation, Data General, Intel, Motorola, Prolog, Zilog, Texas Instruments and all the rest.

Your panel source. Our inventory of chassis and bus compatible IC pluggable panels includes patterned boards and boards with columns which accept IC's of all sizes. There's one to match the specifications of virtually any minicomputer on the market. When you need a custom panel, Augat engineers are ready to help.

Save time and money. All Augat interface panels give you the flexibility of wire wrap. They get your design to the market faster for a head start on sales and profits. Logic and wiring changes are quick and inexpensive at any design stage—even in the field.

High reliability, density. What's more, the heat dissipation of wire wrap posts keeps IC surfaces cooler for longer chip life and greater reliability. The high planar density of panels typically offsets pin extension providing greater volume density.

Custom wiring. All our panels can be wired quickly and accurately at facilities in Attleboro, MA; Houston, TX; and Van Nuys, CA. Send us your logic diagram. We do the rest.

Free Interface Panel Brochure. For details on the fastest, easiest way to interface the minicomputer industry, ask your Augat representative or distributor for a copy of our new brochure. Or write Augat Interconnection Systems Division, 40 Perry Avenue, P.O. Box 779, Attleboro, MA 02703. Tel: 617-222-2202. TWX: 710.391.0644. Or Augat Datatex, 10935 South Wilcrest Drive, Houston, Texas 77099. TWX: 910.881.2486.

AUGAT® **Augat applies for your job.**

*Registered trademark of Gardner Denver Company

CIRCLE 15 ON INQUIRY CARD

Make the most of your host with the lowest cost development tool available.

It's called RADIUS*. By using one with a host computer (any host †), you can develop Z80 and 3870 applications for a lot less than ever before. In fact, at $2995, plus an emulation module, RADIUS is the most inexpensive microprocessor/ microcomputer development station available. Yet it's fast, powerful and reliable.

Why? Because RADIUS lets you take full advantage of the host's speed and power to develop the application software. Once completed, the software is downloaded to the RADIUS (using a link-error-tolerant protocol). Then, using only the RADIUS with the appropriate emulation module, you can perform the full range of real-time, in-circuit emulation and debug needed for hardware development and software integration.

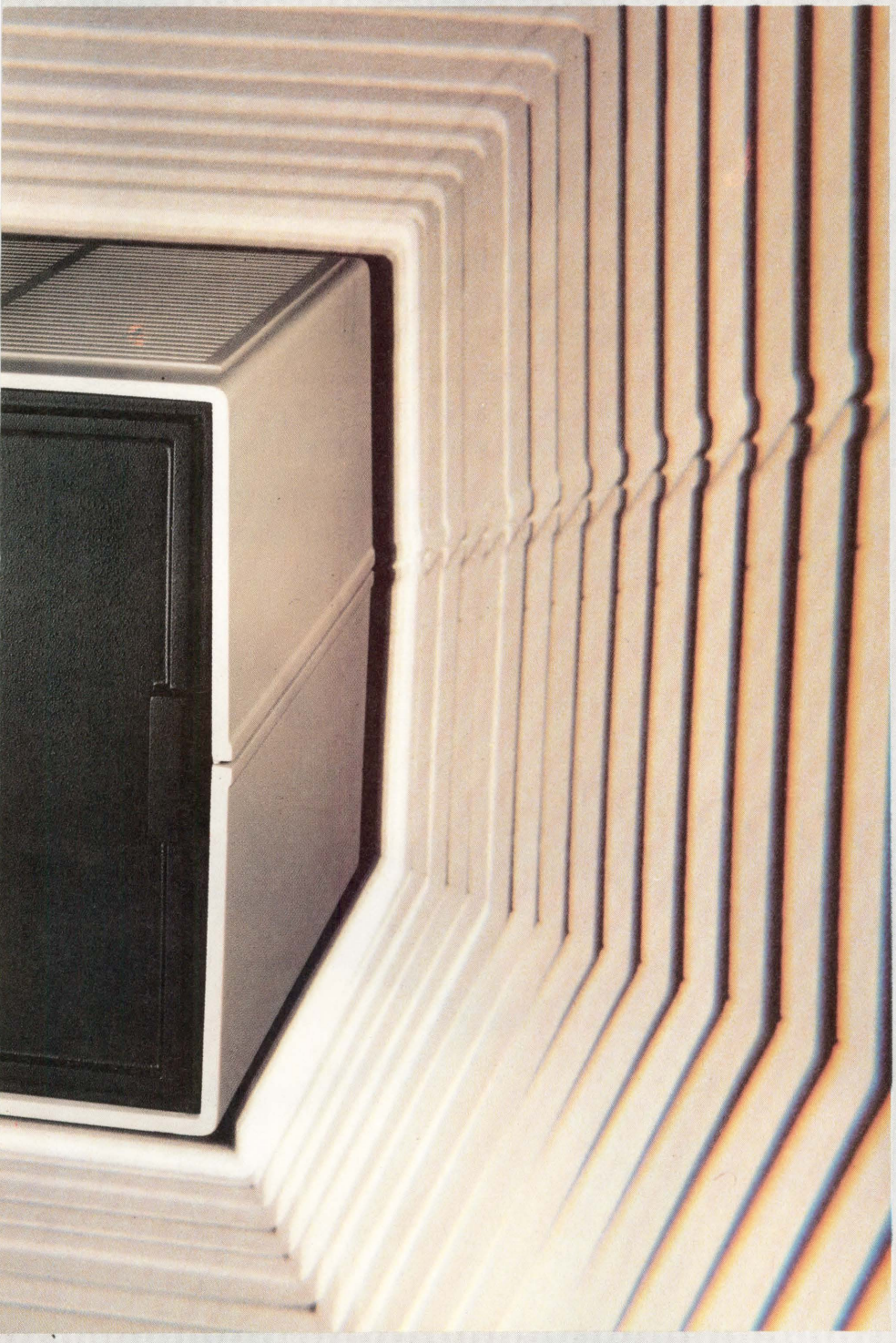
A very friendly user interface makes it all possible. Local or remote (with a MODEM) emulation capability makes it very practical as well. Because at the price we're offering RADIUS, the idea of multiple development stations is more affordable than ever.

In a multi-user environment, for example, you can connect several RADIUS units to an appropriate host and operate them simultaneously to perform entirely separate jobs. This configuration also supports the development of multiple microprocessors and microcomputers.

A SMART WAY TO DEVELOP PLANS FOR THE FUTURE.

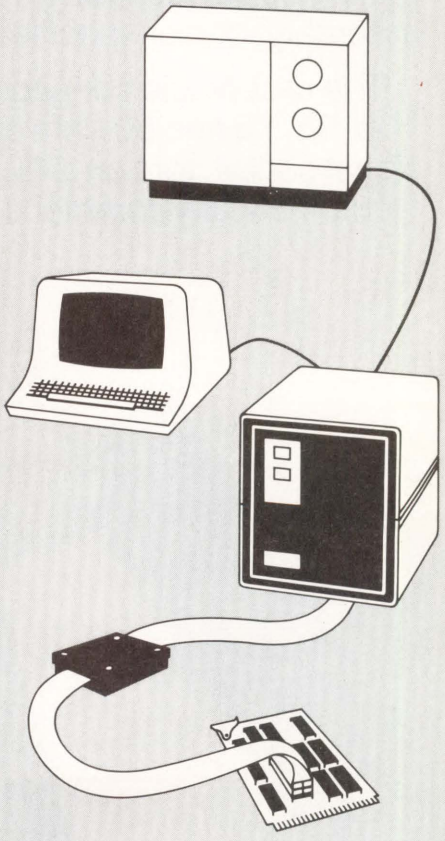
In addition to Z80 and 3870 emulation capability, RADIUS will also accept the forthcoming emulation module for the MK68000, our new

UNITED TECHNOLOGIES MOSTEK



16-bit microprocessor. So no matter which way you're going or plan to go, 8-bit or 16-bit, RADIUS can help you get there. For less.

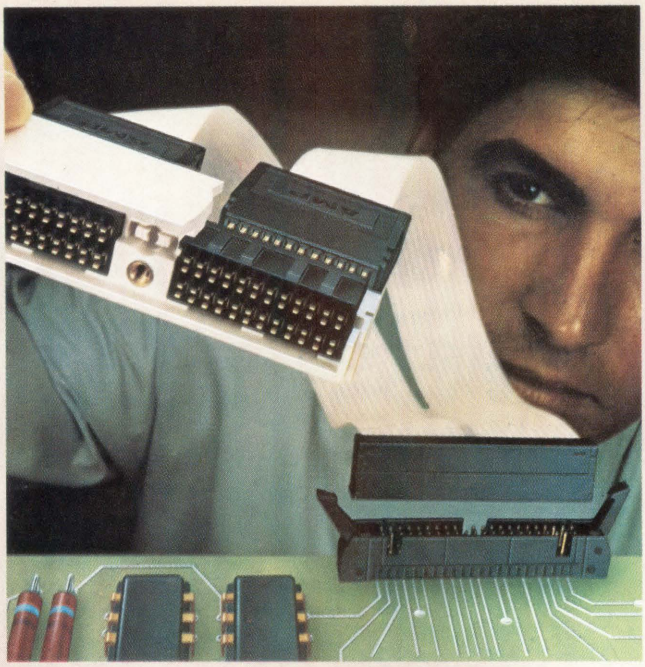
Find out more by contacting Mostek, 1215 West Crosby Road, Carrollton, Texas 75006 (214) 323-1801. In Europe, contact Mostek International at (32)(02) 762.18.80. In the Far East, Mostek Japan KK (03) 404-7261.



*RADIUS is a trademark of Mostek Corporation

†Handshake software packages available for DEC, PDP-11 and VAX. More will be available soon. For others, Mostek will provide source code and compatibility conversion instructions. (DEC, PDP-11 and VAX are trademarks of Digital Equipment Corporation).

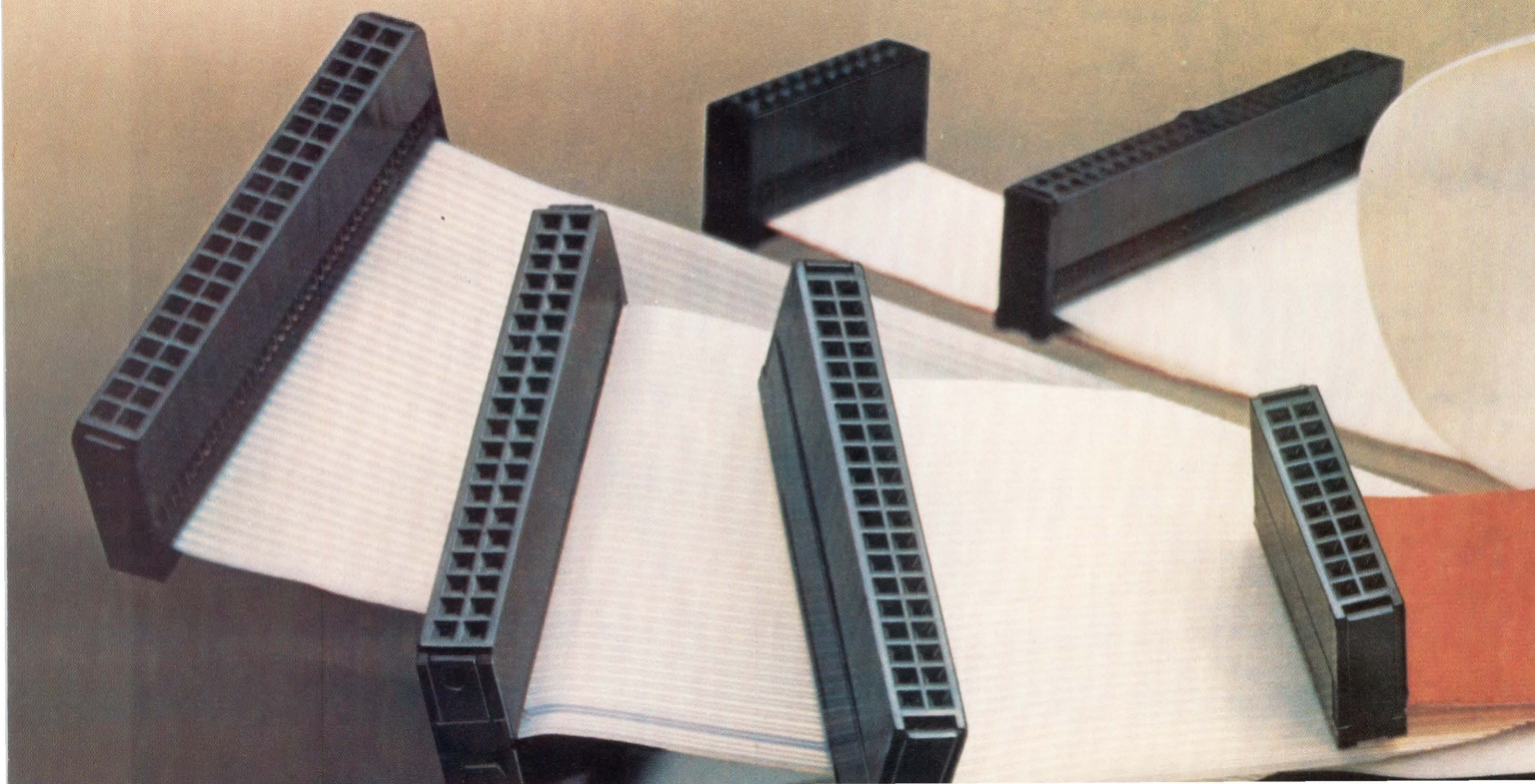
The first solderless transmission cable assembly protects your signals, and your costs.



The unique AMP connector mass terminates transmission cable far faster than soldering—and solderless design means you eliminate high cost, high-temperature cable. You can even forget tooling costs because we supply the assembly to your specifications.

The receptacle connector handles 100, 95, 75 and 50 ohm cables with signal conductors on .050" centers. It automatically commons the grounds to your specified pin out. It physically separates and electrically isolates grounds from signal conductors. What's more, pinfield and SLT types are available, and all come in your specified length, and with your specified cable.

To get the crosstalk—and the cost—out, specify AMP transmission assemblies.



AMP Facts

Typical Mechanical/Electrical/ Environmental Properties

Mechanical

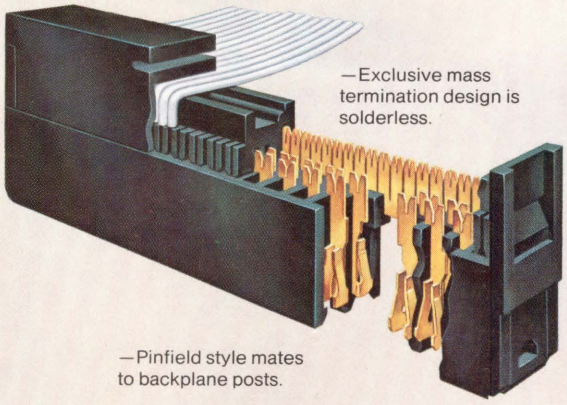
Mating Force	8 oz. max./contact
Unmating Force	1½ oz. min./contact
Mating and Unmating	200 cycles
Vibration	15 G's, 10-2000 Hz
Physical Shock	100 G's, 6 millisec.

Electrical

Current	1.0 ampere max./contact
Contact Resistance	25 milliohms max.
Insulation Resistance	5000 megohms min.
Dielectric Withstanding Voltage	500 volts RMS (sea level)

Environmental

Temperature	−65°C to 105°C
Thermal Shock	5 cycles: −65°C to 105°C
Moisture Resistance	10 days, 25°C to 65°C, 80-98% R.H.
Salt Spray	5% solution, 48 hours
Industrial Gas	10% SO_2, 24 hours



—Exclusive mass termination design is solderless.

—Pinfield style mates to backplane posts.

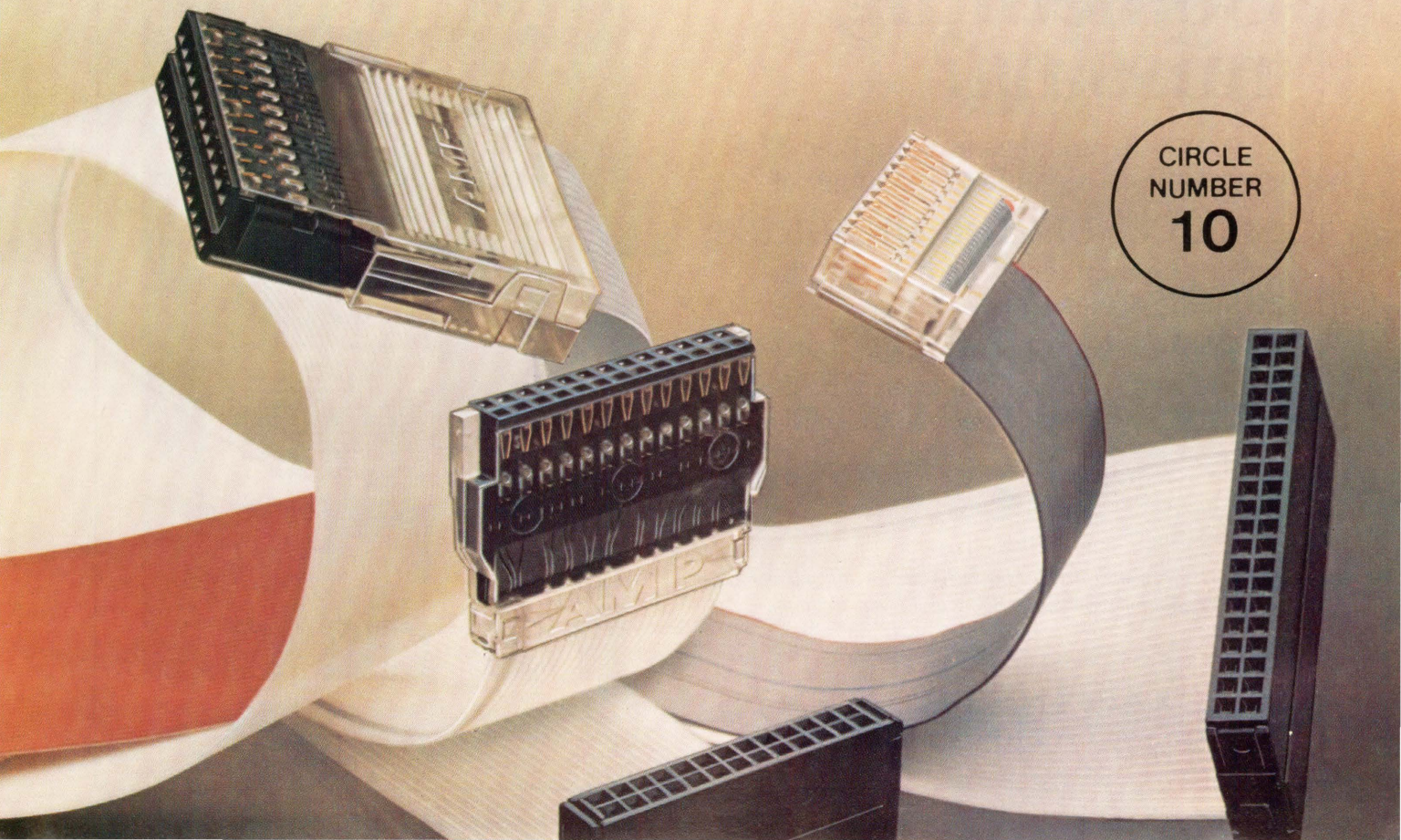
—24 position SLT style for .125″ x .250″ interface.

—.100″ x .100″ receptacle, in 20, 26, 40 or 50 positions.

For more information, call the AMP Transmission Cable Assembly Information Desk at (717) 780-8400.

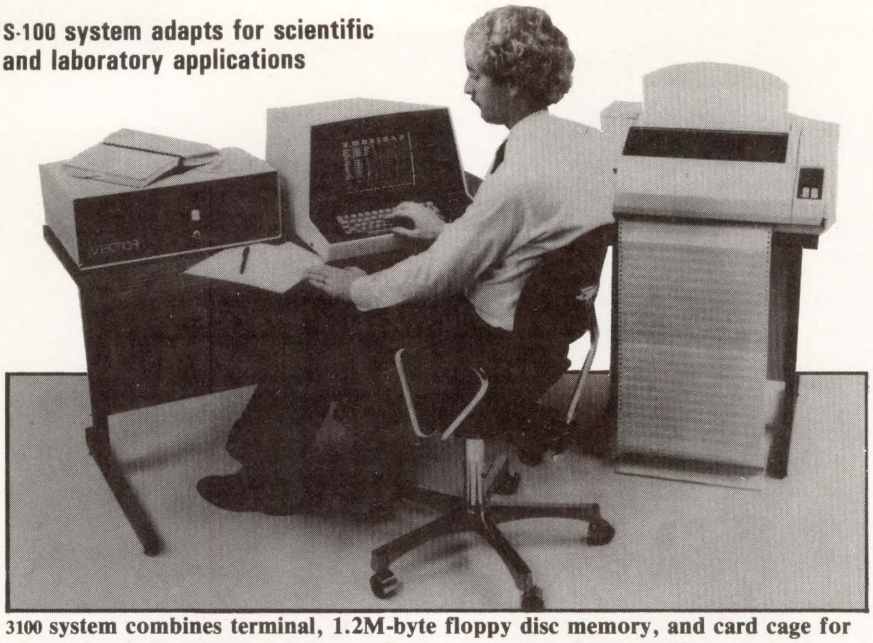
AMP Incorporated, Harrisburg, PA 17105.

AMP means productivity.



CIRCLE NUMBER 10

S-100 system adapts for scientific and laboratory applications



3100 system combines terminal, 1.2M-byte floppy disc memory, and card cage for up to 18 S-100 interface modules to allow user to assemble versatile systems for variety of electronic, chemical, physical, optical, and other research and development projects

Two versions of an S-100 based technical computer system are designed specifically for industrial and scientific applications such as automating laboratory experiments and procedures. The Vector 2 series by Vector Graphic consists of a Z80 processor and terminal with memory and I/O boards in an 18-slot card cage with heavy duty power supply and a choice of disc storage configurations. The 3100 contains two 600k 5.25″ (13.34-cm) floppy disc drives for 1.2M bytes of storage, and the 3105 contains one 5.25″ (13.34-cm) Winchester disc with 5M bytes of storage and a single 630k-byte floppy disc.

In addition to the wide variety of S-100 cards available for scientific and instrumentation applications, Vector Graphic is offering six boards of its own for such applications: a fast scan video digitizer; a high resolution graphic module; a 12-channel D-A converter and a multichannel A-D converter; a clock/calendar; and a board with P/ROM and RAM. Machine language software support modules are also available for each of the boards.

Additional software targeted for use with this series includes an extended BASIC, which allows system output to an X-Y plotter and which also has routines to plot data on a dot matrix printer. This version of Microsoft BASIC 80 also allows users to load assembly language programs directly into memory. In addition, a series of cross assemblers for most popular 8-bit microprocessors is available for program development.

The base price for the Vector 2 3100 system is $5795; the 3105 is priced at $8495. **Vector Graphic, Inc**, 500 N Ventu Park Rd, Thousand Oaks, CA 91320.
Circle 241 on Inquiry Card

MEMORIES

from Texas Instruments

Read-and-File Guide to TI Semiconductor Memories

Here are the densities and performance features — the advanced technologies — that will help you design the best possible, most cost-effective systems.

A broad choice in both MOS and bipolar: DRAMs. EPROMs. ROMs. SRAMs. PROMs. All from Texas Instruments. All of proven quality and reliability.

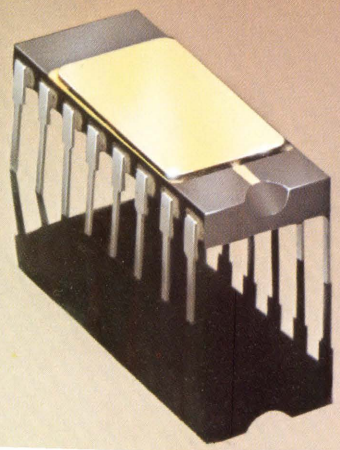
Included are the industry's first 32K and 64K EPROMs. The fastest of the fast statics. The widest selection in PROMs. And a pacesetting 64K DRAM.

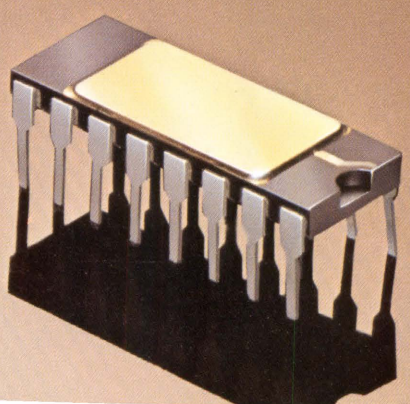
Read and file this convenient guide. It's worth a lot of mileage in helping you save time and money.

DRAMs

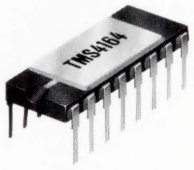
from Texas Instruments

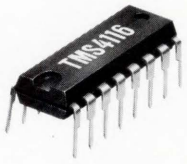
PART NO.	ORGANIZATION	ACCESS	CYCLE	MAX. POWER		PACKAGE
				OPER.	STBY.	
TMS4116-15	16K × 1	150 ns	375 ns	462 mW	20 mW	NL-Plastic
TMS4116-20	16K × 1	200 ns	375 ns	462 mW	20 mW	NL-Plastic
TMS4116-25	16K × 1	250 ns	410 ns	425 mW	20 mW	NL-Plastic
TMS4164-15	64K × 1	150 ns	280 ns	200 mW	27 mW	NL-Plastic JDL-Sidebraze
TMS4164-20	64K × 1	200 ns	350 ns	200 mW	27 mW	NL-Plastic JDL-Sidebraze
TMS4164-25	64K × 1	250 ns	410 ns	200 mW	27 mW	NL-Plastic JDL-Sidebraze





Major performance improvements at lower costs





Readily available, TI's new TMS4164 64K DRAM brings higher system performance at lower overall system cost to your new designs and upgrades.

Best speed/power combination — In all the world, only the new TMS4164-15 offers 150-ns access time and 280-ns cycle time coupled with the lowest power dissipation for such a device. Only 140 mW typical — a 50% reduction compared to 16Ks.

And, our 200- and 250-ns versions have even lower typical power dissipations — 125 and 105 mW — ideal for small systems demanding low active power.

Faster cycle times also mean refresh overhead is reduced from 2.4% to 1.8%.

"Elegant" chip design — In addition to lowering power requirements, TI's unique epitaxial silicon technology virtually eliminates the effects of substrate noise and dramatically increases operating margins. And, this innovative design also results in a 64K chip that's the smallest in production.

Overall economies — Having 64K bits in a single package substantially boosts system capability and reduces system costs.

Compared to four 16Ks, the single 300-mil, 16-pin package saves board space and eases layout. As does the single +5-V power supply — normally you would need three.

System operating margins are improved. As is reliability. Interconnects and system test are reduced. As are cooling requirements.

The TMS4164 is in distributor stocks ready for off-the-shelf delivery. It is supported down-the-line by knowledgeable, accessible field sales engineers in TI's 50 sales offices across the nation. Help, whenever you need it, is only a phone call away.

TI's TMS4164. It gives you the best possible performance improvement obtainable today at an extremely cost-effective price.

Coming soon:

- An even faster TMS4164
- A new 64K especially for microprocessor systems
- A controller to simplify DRAM design

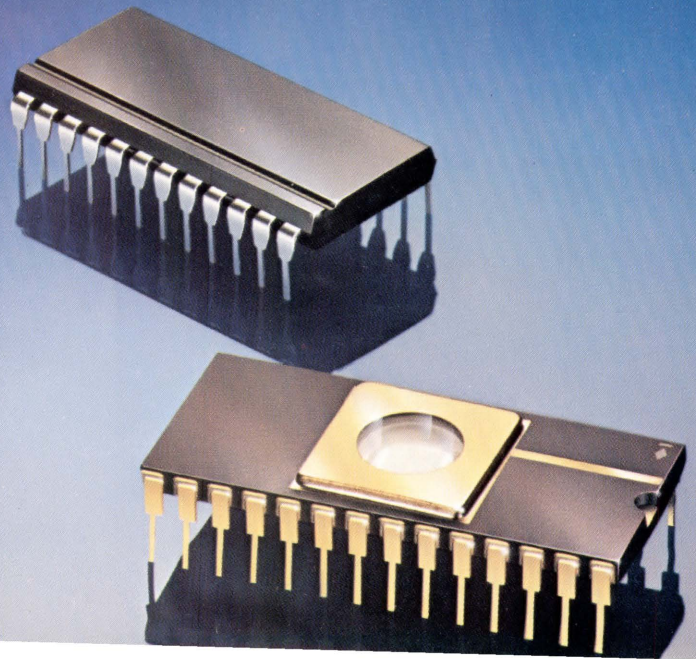
Leadership 16K DRAM — For designs where larger memory capacity is not required, TI continues to offer the low-cost TMS4116 16K device. The popular choice for present high-volume applications, the TMS4116 offers outstanding — and thoroughly proven — quality, performance, and reliability. The result of five years of production experience, the TMS4116 represents TI's on-going commitment to MOS memories.

EPROMs

from Texas Instruments

PART NO.	ORGANIZATION	ACCESS		MAX. POWER		PACKAGE
		FROM ADDR.	FROM C/S	OPER.	STBY.	
TMS2708-35	1K × 8 3 power supplies	350 ns	120 ns	800 mW	—	JL-Ceramic JDL-Sidebraze
TMS2708-45	1K × 8 3 power supplies	450 ns	120 ns	800 mW	—	JL-Ceramic JDL-Sidebraze
TMS27L08-45	1K × 8 3 power supplies	450 ns	120 ns	580 mW	—	JL-Ceramic JDL-Sidebraze
TMS2716-30	2K × 8 3 power supplies	300 ns	120 ns	720 mW	—	JL-Ceramic JDL-Sidebraze
TMS2716-45	2K × 8 3 power supplies	450 ns	120 ns	720 mW	—	JL-Ceramic JDL-Sidebraze
TMS2516-25	2K × 8	250 ns	120 ns	525 mW	131 mW	JL-Ceramic JDL-Sidebraze
TMS2516-35	2K × 8	350 ns	120 ns	525 mW	131 mW	JL-Ceramic JDL-Sidebraze
TMS2516-45	2K × 8	450 ns	120 ns	525 mW	131 mW	JL-Ceramic JDL-Sidebraze
TMS2532-30	4K × 8	300 ns	—	840 mW	131 mW	JL-Ceramic JDL-Sidebraze
TMS2532-35	4K × 8	350 ns	—	840 mW	131 mW	JL-Ceramic JDL-Sidebraze
TMS2532-45	4K × 8	450 ns	—	840 mW	131 mW	JL-Ceramic JDL-Sidebraze
TMS25L32-45	4K × 8	450 ns	—	500 mW	131 mW	JL-Ceramic JDL-Sidebraze
TMS2564-45	8K × 8	450 ns	120 ns	840 mW	158 mW	JDL-Sidebraze

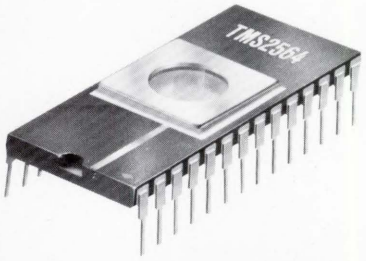
ROMS						
TMS4732	4K × 8	300 ns	120 ns	440 mW	110 mW	JL-Ceramic NL-Plastic
TMS4764	8K × 8	300 ns	120 ns	440 mW	110 mW	JL-Ceramic NL-Plastic



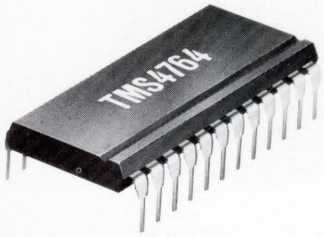
The broad choice for optimum system performance

From the workhorse 16K to the industry's first 64K, TI offers 5-V, fully-static EPROMs to fit your every design need. With high performance, and access times as fast as 250 ns. For today's new systems and upgrades. Preparing for what is to come.

Use TI's TMS2500 family for program and fixed parameter storage during system development and prototyping where you need to change data quickly and easily. Check out their cost effectiveness for use in initial production when you are in a hurry to get to the marketplace.



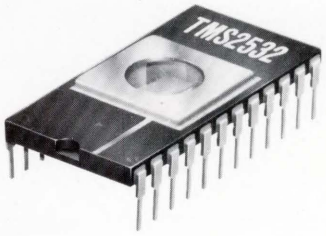
Maximum compatibility — The pinouts for TI EPROMs are derived from popular industry-standard ROMs so that all members of the family are plug-compatible with each other. And will be with those that are on the way. Which makes upgrading a simple design task, and prolongs product life.



Easy programming — You avoid mask charges by programming TI EPROMs yourself using widely available programmers and a single TTL-level pulse. You program in any order — individually, in blocks, at random. Erasing is only a matter of ultra-violet.

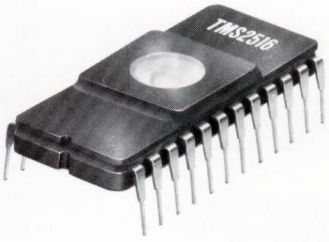
The result is that whatever EPROM type you choose, it can be used for many different programs. You lower inventory costs and eliminate write-off costs when programs need updating.

From TI, you have the choice and the performances to achieve optimum system performance. At especially attractive prices. With prompt delivery from distributor stocks.



Coming soon:

- A new EPROM family with very fast access times
- A high-density 128K EPROM for tomorrow's systems



Economical, high-density ROMs — When your programming will not change or need to be updated, using large-capacity ROMs in large numbers can achieve the lowest cost of any semiconductor memory. TI offers two high-density ROMs tailored for the job — the 32K TMS4732 and the 64K TMS4764.

Both are high performance memories with low power dissipations, typically less than 400 mW. Maximum access and minimum cycle times are 300 ns. They are fully static — no clocks — and require only a single 5-V power supply. Reliability is enhanced by the use of N-channel silicon gate technology during fabrication, and all outputs are TTL compatible.

These ROMs are plug-compatible with TI's 32K and 64K EPROMs. After you have defined your programming using TI EPROMs with their inherent savings, you can switch to TI ROMs for the economies of volume production. A system designed with appropriate memory addressing can utilize TI's 32K or 64K EPROMs or TI's 32K or 64K ROMs on the same printed circuit boards in the same 24- or 28-pin sockets.

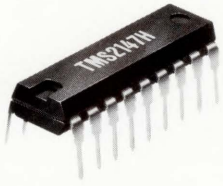
SRAMs from Texas Instruments

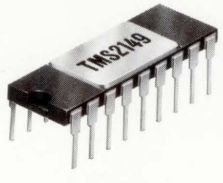
PART NO.	ORGANIZATION	ACCESS		MAX. POWER		PACKAGE
		FROM ADDR.	FROM C/S	OPER.	STBY.	
TMS2114-15	1K × 4	150 ns	70 ns	330 mW	120 mW	NL-Plastic
TMS2114-20	1K × 4	200 ns	85 ns	330 mW	120 mW	NL-Plastic
TMS2114-25	1K × 4	250 ns	100 ns	330 mW	120 mW	NL-Plastic
TMS2114-45	1K × 4	450 ns	120 ns	330 mW	120 mW	NL-Plastic
TMS2114L-15	1K × 4	150 ns	70 ns	248 mW	72 mW	NL-Plastic
TMS2114L-20	1K × 4	200 ns	85 ns	248 mW	72 mW	NL-Plastic
TMS2114L-25	1K × 4	250 ns	100 ns	248 mW	72 mW	NL-Plastic
TMS2114L-45	1K × 4	450 ns	120 ns	248 mW	72 mW	NL-Plastic
TMS4044-12	4K × 1	120 ns	70 ns	303 mW	108 mW	NL-Plastic
TMS4044-20	4K × 1	200 ns	70 ns	303 mW	108 mW	NL-Plastic
TMS4044-25	4K × 1	250 ns	70 ns	303 mW	108 mW	NL-Plastic
TMS4044-45	4K × 1	450 ns	100 ns	303 mW	108 mW	NL-Plastic
TMS40L44-12	4K × 1	120 ns	70 ns	220 mW	60 mW	NL-Plastic
TMS40L44-20	4K × 1	200 ns	70 ns	220 mW	60 mW	NL-Plastic
TMS40L44-25	4K × 1	250 ns	70 ns	220 mW	60 mW	NL-Plastic
TMS40L44-45	4K × 1	450 ns	100 ns	220 mW	60 mW	NL-Plastic
TMS2147H-3	4K × 1	35 ns	35 ns	660 mW	165 mW	NL-Plastic JL-Ceramic
TMS2147H-4	4K × 1	45 ns	45 ns	660 mW	165 mW	NL-Plastic JL-Ceramic
TMS2147H-5	4K × 1	55 ns	55 ns	660 mW	165 mW	NL-Plastic JL-Ceramic
TMS2147H-7	4K × 1	70 ns	70 ns	660 mW	165 mW	NL-Plastic JL-Ceramic
TMS2149-3	1K × 4	35 ns	15 ns	660 mW	—	NL-Plastic JL-Ceramic
TMS2149-4	1K × 4	45 ns	20 ns	660 mW	—	NL-Plastic JL-Ceramic
TMS2149-5	1K × 4	55 ns	25 ns	660 mW	—	NL-Plastic JL-Ceramic
TMS2149-7	1K × 4	70 ns	30 ns	660 mW	—	NL-Plastic JL-Ceramic

Speed demons and other performance leaders

Where speed is the top priority in storing variable data, TI's fast SRAMs win hands down. Two new memories from TI — TMS2147H and TMS2149 — offer an access time from address of a scant 35 ns. Access time from chip select can be a lightning-fast 15 ns. Yet maximum operating power is only 660 mW.

They are just the ticket for use in cache, control store, and high-speed buffer applications.





High performance TMS2147H — Organized 4K × 1, this new SRAM offers access times from address or chip select of 35, 45, 55, and 70 ns, and has a chip select, power down feature. Maximum operating power is 660 mW, with standby power at 165 mW.

High performance TMS2149 — This new SRAM is organized 1K × 4, and has an access time from chip select as fast as 15 ns. Allowing you to take full advantage of system decoding delays and get the performance you expect. Access time from address is 35, 45, 55, and 70 ns.

Because of TI's low power, both memories come in space-saving 18-pin, 300-mil ceramic and plastic packages. And, both are ready for delivery now.

If your system calls for slower speeds but you still want high performance, check our new 4K TMS4044 and TMS2114 static RAMs. The 4K × 1 and 1K × 4 offer 120 ns and 150 ns access times respectively, with maximum operating power only 220 mW and 248 mW on the low-power versions. Both represent a dependable, reliable solution to simplify your microprocessor system design.

Coming soon:

- A new 2K × 8 static RAM with 120 ns access times
- A high-density, high-performance 16K × 1 static RAM
- A MOS memory subsystem for cache memory design

PROMs from Texas Instruments

PART NO.	SIZE	ORGANIZATION	TYPICAL ADDRESS ACCESS TIME	TYPICAL POWER DISSIPATION
TBP18S030 TBP18SA030	256 Bits 256 Bits	32W × 8B	25 ns	400 mW
TBP24S10 TBP24SA10	1K Bits 1K Bits	256W × 4B	35 ns	375 mW
TBP28L22 TBP28LA22	2K Bits 2K Bits	256W × 8B	45 ns	375 mW
TBP28S42 TBP28SA42	4K Bits 4K Bits	512W × 8B	35 ns	500 mW
TBP28S46 TBP28SA46	4K Bits 4K Bits	512W × 8B	35 ns	500 mW
TBP24S41 TBP24SA41	4K Bits 4K Bits	1024W × 4B	40 ns	475 mW
TBP28S86-60 TBP28SA86-60	8K Bits 8K Bits	1024W × 8B	35 ns	625 mW
TBP28S86 TBP28SA86	8K Bits 8K Bits	1024W × 8B	45 ns	625 mW
TBP28L86	8K Bits	1024W × 8B	65 ns	275 mW
TBP24S81-55 TBP24SA81-55	8K Bits 8K Bits	2048W × 4B	35 ns	625 mW
TBP24S81 TBP24SA81	8K Bits 8K Bits	2048W × 4B	45 ns	625 mW
TBP28S166-55 TBP28S166	16K Bits 16K Bits	2048W × 8B 2048W × 8B	35 ns 45 ns	675 mW 675 mW

A = OPEN COLLECTOR; L = LOW POWER

Top performers across the board

Name your design needs in bipolar PROMs. Fill them quickly from the industry's broadest choice. At Texas Instruments.

Low densities to high — Your choice ranges from a 256-bit PROM — often needed but difficult to find — to a new high-performance 16K device. You can choose from by-4 and by-8 organizations. With maximum address access times as much as 20 ns faster than data sheet specifications thanks to speed screening.

Better heat dissipation — Many TI PROMs in plastic packages now incorporate advanced copper-clad stainless steel leadframes which improve thermal characteristics by 20% to 25%. Result: Lower operating temperatures in the circuit which boost product reliability.

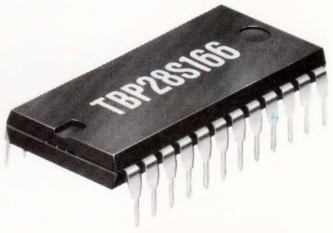
Convenient programming — TI's PROMs eliminate many programming problems and reduce programming costs. A single specification programs all members from 1K through 16K, using any of the popular programmers on the market. Or for no fallout whatever, you can have TI program, symbolize, and ship your PROMs to you (200-piece minimum order per program per scheduled delivery).

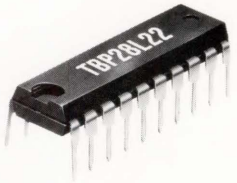
Space-saving packages — You can order many TI PROMs in 300-mil wide packages that save 50% in board space. The 600-mil package is also available — both widths in plastic or ceramic.

More advantages — All TI PROMs incorporate titanium-tungsten fuse lengths. All have low current PNP inputs to permit easy interfacing with MOS and bipolar microprocessors. All are Schottky-clamped for the best speed/power combinations.

Coming soon:

- Registered PROMs ideally suited for microprogrammed pipeline systems





Read and file this guide. As a quick reference to TI's broad selection of semiconductor memories, it can quickly put you on the right track to solutions for design problems.

For more detailed information on any of TI's semiconductor memories, call your authorized TI distributor.

TI Distributors

ALABAMA: Huntsville, Hall-Mark (205) 837-8700.

ARIZONA: Phoenix, Kierulff (602) 243-4101; R.V. Weatherford (602) 272-7144; **Tempe,** Marshall (602) 968-6181; **Tucson,** Kierulff (602) 624-9986.

CALIFORNIA: Anaheim, R.V. Weatherford (714) 634-9600; **Buena Park,** RPS (213) 744-0355; **Canoga Park,** Marshall (213) 999-5001; **Chatsworth,** JACO (213) 998-2200; **El Monte,** Marshall (213) 686-0141; **Glendale,** R.V. Weatherford (213) 849-3451; **Goleta,** RPS (805) 964-6823; **Irvine,** JACO (714) 540-5600; Marshall (714) 556-6400; **Los Angeles,** Kierulff (213) 725-0325; **Newport Beach,** Arrow; **Northridge,** Arrow (213) 701-7500; **Palo Alto,** Kierulff (415) 968-6292; **Pomona,** R.V. Weatherford (714) 623-1261; **San Diego,** Arrow (714) 565-4800; Kierulff (714) 278-2112; Marshall (714) 578-9600; R.V. Weatherford (714) 695-1700; **Santa Barbara,** R.V. Weatherford (805) 465-8551; **Santa Clara,** United Components (408) 496-6900; **Sunnyvale,** Arrow (408) 745-6600; Marshall (408) 732-1100; Time (408) 734-9888; United Components (408) 496-6900; **Torrance,** Time (213) 320-0880; **Tustin,** Kierulff (714) 731-5711.

COLORADO: Denver, Arrow (303) 758-2100; Diplomat (303) 740-8300; Kierulff (303) 371-6500; **Englewood,** R.V. Weatherford (303) 428-6900.

CONNECTICUT: Orange, Milgray (203) 795-0714; **Wallingford,** Arrow (203) 265-7741; Marshall (203) 265-3822; Kierulff (203) 265-1115.

FLORIDA: Clearwater, Diplomat (813) 443-4514; **Ft. Lauderdale,** Arrow (305) 973-8502; Diplomat (305) 971-7160; Hall-Mark (305) 971-9280; **Orlando,** Hall-Mark (305) 855-4020; **Palm Bay,** Arrow (305) 725-1480; Diplomat (305) 725-4520; **St. Petersburg,** Kierulff (813) 576-1966; **Winter Park,** Milgray (305) 647-5747.

GEORGIA: Norcross, Arrow (404) 449-8252; Hall-Mark (404) 447-8000; Marshall (404) 923-5750.

ILLINOIS: Bensonville, Diplomat (312) 595-1000; Hall-Mark (312) 860-3800; **Elk Grove Village,** Kierulff (312) 640-0200; **Chicago,** Newark (312) 638-4411; **Schaumburg,** Arrow (312) 893-9420.

INDIANA: Ft. Wayne, Graham (219) 423-3422; **Indianapolis,** Graham (317) 634-8202; Arrow (317) 243-9353.

IOWA: Cedar Rapids, Arrow (319) 395-7230; Deeco (319) 365-7551.

KANSAS: Lenexa, Component Specialties (913) 492-3555; **Shawnee Mission,** Hall-Mark (913) 888-4747; **Wichita,** LCOMP (316) 265-9507.

MARYLAND: Baltimore, Arrow (202) 737-1700, (301) 247-5200; Hall-Mark (301) 796-9300; **Columbia,** Diplomat (301) 995-1226; **Rockville,** Milgray (301) 468-6400.

MASSACHUSETTS: Billerica, Kierulff (617) 667-8331; **Burlington,** Marshall (617) 272-8200; **Holliston,** Diplomat (617) 429-4120; **Woburn,** Arrow (617) 933-8130; Time (617) 935-8080.

MICHIGAN: Ann Arbor, Arrow (313) 971-8200; **Oak Park,** Newark (313) 967-0600; **Farmington,** Diplomat (313) 477-3200; **Grand Rapids,** Newark (616) 241-6681.

MINNESOTA: Bloomington, Hall-Mark (612) 854-3223; **Edina,** Arrow (612) 830-1800; Kierulff (612) 941-7500; **Minneapolis,** Diplomat (612) 788-8601.

MISSOURI: Earth City, Hall-Mark (314) 291-5350; **Kansas City,** LCOMP (816) 221-2400; **St. Louis,** Arrow (314) 567-6888; LCOMP (314) 291-6200; Kierulff (314) 739-0855.

NEW HAMPSHIRE: Manchester, Arrow (603) 668-6968.

NEW JERSEY: Camden, General Radio Supply (609) 964-8560; **Cherry Hill,** Hall-Mark (609) 424-0880; **Clifton,** JACO (201) 778-4722; Marshall (201) 340-1900; **Fairfield,** Kierulff (201) 575-6750; **Marlton,** Milgray (609) 424-1300; **Moorestown,** Arrow (609) 235-1900; **Saddlebrook,** Arrow (201) 797-5800; **Totowa,** Diplomat (201) 785-1830.

NEW MEXICO: Albuquerque, Arrow (505) 243-4566; International Electronics (505) 345-8127; United Components (505) 345-9981.

NEW YORK: Endwell, Marshall (607) 754-1570; **Freeport,** Milgray (516) 546-5600, N.J. (800) 645-3986; **Hauppauge,** Arrow (516) 231-1000; JACO (516) 273-5500; **Liverpool,** Arrow (315) 652-1000; Diplomat (315) 652-5000; **Melville,** Diplomat (516) 454-6400; **Rochester,** Arrow (716) 275-0300; Rochester Radio Supply (716) 454-7800; Marshall (716) 235-7620; **Ronkonkoma,** QPL (516) 467-1200.

NORTH CAROLINA: Greensboro, Kierulff (919) 852-6261; **Raleigh,** Arrow (919) 876-3132; Hall-Mark (919) 832-4465; **Winston-Salem,** Arrow (919) 725-8711.

OHIO: Beachwood, Kierulff (216) 587-6558; **Centerville,** Arrow (513) 435-5563; **Cincinnati,** Graham (513) 732-1661; **Columbus,** Hall-Mark (614) 846-1882; **Dayton,** ESCO (513) 226-1133; Marshall (513) 236-8088; **Highland Heights,** Hall-Mark (216) 473-2907; **Solon,** Arrow (216) 248-3990.

OKLAHOMA: Tulsa, Component Specialties (918) 664-2820; Hall-Mark (918) 835-8458; Kierulff (918) 252-7537.

OREGON: Beaverton, Almac Stroum (503) 641-9070; **Portland,** Kierulff (503) 641-9150.

PENNSYLVANIA: Pittsburgh, Arrow (412) 856-7000.

TEXAS: Austin, Component Specialties (512) 837-8922; Hall-Mark (512) 258-8848; Harrison Equipment (512) 458-3555; Kierulff (512) 835-2090; **Dallas,** Component Specialties (214) 357-6511; Hall-Mark (214) 341-1147; International Electronics (214) 233-9323; Kierulff (214) 343-2400; **El Paso,** International Electronics (915) 778-9761; **Houston,** Component Specialties (713) 771-7237; Hall-Mark (713) 781-6100; Harrison Equipment (713) 652-4700; Kierulff (713) 530-7030.

UTAH: Salt Lake City, Diplomat (801) 486-4134; Kierulff (801) 973-6913.

WASHINGTON: Redmond, United Components (206) 643-7444; **Seattle,** Almac/Stroum (206) 643-9992; Kierulff (206) 575-4420; **Tukwila,** Arrow (206) 575-0907.

WISCONSIN: Oak Creek, Arrow (414) 764-6600; Hall-Mark (414) 761-3000; **Waukesha,** Kierulff (414) 784-8160.

CANADA: Calgary, Cam Gard Supply (403) 287-0520; Future (403) 259-6408; Varah (403) 230-1235; **Downsview,** CESCO (416) 661-0220; **Edmonton,** Cam Gard Supply (403) 426-1805; **Halifax,** Cam Gard Supply (902) 454-8581; **Hamilton,** Varah (416) 561-9311; **Kamloops,** Cam Gard Supply (604) 372-3338; **Moncton,** Cam Gard Supply (506) 855-2200; **Montreal,** CESCO (514) 735-5511; Future (514) 694-7710; **Ottawa,** CESCO (613) 729-5118; Future (613) 820-8313; **Quebec City,** CESCO (418) 687-4231; **Regina,** Cam Gard Supply (306) 525-1317; **Saskatoon,** Cam Gard Supply (306) 652-6424; **Toronto,** Future (416) 663-5563; **Vancouver,** Cam Gard Supply (604) 291-1441; Future (604) 438-5545; Varah (604) 873-3211; **Winnipeg,** Cam Gard Supply (204) 786-8481; Varah (204) 633-6190. AF

Outside the United States and Canada:

Argentina 748-1141; Australia (02) 887-1122; Belgie/Belgique (02) 720.80.00; Brasil 518423; Deutschland 08161/801; France (3) 946 97 12; Italia (0748) 69034; Japan 03-498-2111; Mexico 567-9200; Nederland 020-473391; Schweiz/Suisse 01 740 22 20; Sverige (08) 23.54.80; United Kingdom (0234) 223000

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

TEXAS INSTRUMENTS
INCORPORATED

Printed in U.S.A.

SCG678
83966

Operating system kernel has realtime response

Machines that have available a C language compiler can now run a realtime operating system kernel to create a portable environment. Known as Operating System/Real Time (OS/RT), the kernel is provided in C source code and needs only a small section of machine language code (250 to 500 bytes) to enable it to talk to a given system. OS/RT uses a "compatibility based" design that allows the programmer to think in terms of named processes without having to remember machine specific details.

User programs can refer to resource names rather than to control block addresses. OS/RT supports five types of resources—operating system entities that can be dynamically created and destroyed. Since resources are all referred to by names (ASCII strings), the programmer can create a process without knowing how the system handles resource allocation.

Five types of resources are processes, executable code that competes for CPU control; memory, a section of memory allocated by the system and accessible to a process; events, generated or anticipated by processes and used for process synchronization; interprocess communication, channels over which processes communicate in packets of data; and interrupt, a signal to the OS that an external event has occurred.

Since the system allocates resources, there are no fixed system tables or table sizes in OS/RT. A process can act as a "parent" process and start up multiple "child" processes. The parent can then pass other resources to its "children," giving them access rights to resources. Thus child processes can share data and resources via their parent.

This structured parent/child hierarchy prevents deadlocked situations since resources can be shared by resource name while the parent process also has control over which resources child processes can access. Thus the system requires the programmer to structure named applications hierarchically to reduce uncertainty about resource allocation or possible deadlocks.

For multifunction environments, OS/RT offers realtime response capabilities for time-crucial applications. OS/RT can handle interrupts or pass control to an interrupt handling process (resource); and in systems with built-in clocks, it can support interrupt time-outs. The user can define a time frame within which an interrupt is expected to occur. If the interrupt does not occur within this period, OS/RT alerts the user.

OS/RT allows the user to configure a custom environment and is designed to require a minimal fixed amount of RAM. The user can decide how much RAM the applications programs require and can dynamically create the needed resources at runtime. Software resources necessary, such as peripheral drivers, would be written as part of the application and not as an integral part of the operating system. OS/RT then arbitrates between these processes and other named resources they require.

OS/RT can maintain separate spaces for system and user data; and because it requires so little data to run, OS/RT can be placed easily in ROM. This separation of user programs also helps to protect system control block structures.

The system is supplied in C source code, with complete programmer documentation and model machine language interfaces for a variety of processors. These interfaces are intended for popular machines, and also as instructional examples for programmers who wish to implement OS/RT on other computers. It is priced at $8000 for an unlimited binary license. **The Destek Group**, 1923 Landings Dr, Mountain View, CA 94043.

Circle 242 on Inquiry Card

Two OS processors implemented by coupling firmware OS with μPs

An operating system kernel, single-chip 80130 implemented in firmware, when coupled with a standard 8086 or 8088, becomes the basis for a realtime, high performance multitasking and multiprogramming OS for OEM products. The OS processors are designated iAPX 86/30™ for the 8086 and 80130 2-chip set, and iAPX 88/30™ for the 8088 and 80130. The 80130 connects directly to the local bus of either processor and self-detects with the processor in tandem.

The iAPX 86/30 and 88/30 extend the base 8086 and 8088 architecture by providing 35 OS instructions (primitives) in hardware, to implement an OS kernel. The primitives form a compact instruction set which can serve as an OS for simple products, as a base for the company's iRMX™ 86 realtime multitasking OS, or as a base for a custom OS. The primitives create, manipulate, and delete five new system data types to add interrupt handling, message passing, task synchronization, and memory

(continued on page 42)

management facilities to iAPX 86 and iAPX 88 systems. This structure is similar to mainframe and mincomputer software architecture.

The five new system data types are jobs, tasks, segments, mailboxes, and regions:

- Job data support multiprogramming, allowing several different applications to run on a single OS processor and maximizing hardware utilization.
- Tasks are basic units used to create, delete, and control execution of instructions in realtime multitasking systems. There are two techniques in multitasking systems that decide task sequencing. Time slicing is used in time-sharing systems to run tasks on a first-come, first-served basis. Preemptive priority based scheduling compares assigned priorities of tasks waiting to run and processes the most important tasks first. OS processors support the latter technique.

Logic and interrupt level primitives, rather than a polled method of event processing, is used to map external interrupts at any of eight levels directly into 255 different task priorities. Interrupts can set and reset interrupt levels, based on task priority, to any level. The number of interrupts is expandable to 57 by adding external 8259A interrupt controllers. An interrupt handler method is used with time critical interrupts or for simple interrupt processing. The interrupt task method is used where more processing work needs to be done, still allowing interrupts to be recognized.

- Segment data are used for memory management. OS processors support a dynamic allocation technique that permits jobs to share memory, as well as reallocates memory as job requirements change during system operation. Primitives create and delete segments up to 64k bytes long, in units of 16-byte paragraphs, anywhere in the CPU's 1M-byte address space.
- Mailbox data permit communication and synchronization between tasks. Such interaction is required whenever one task must pass data or event information to another task for processing to continue.
- Region data prevent one task from seizing control of a shared resource while another task is modifying its contents. This technique, called "mutual exclusion," ensures correct processing by making tasks wait until certain processing is finished.

In addition to the 16k-byte OS kernel control store, the 80130 contains a programmable interrupt controller, an OS timer, a delay timer, a baud rate generator, and support logic. The programmable interrupt controller performs all functions of the company's 8259A, and accepts direct requests at any of 8 interrupt pins. Each input can be set for edge- or level-sensitive operation, and also can be cascaded through an external 8259A operating as a slave.

The hardware described occupies a 16-byte block of addresses in the processor's 64k-byte I/O space. A system based on one of the two OS processors requires a total of 2.5k bytes of system RAM—1k byte for CPU interrupt vectors and 1.5k bytes for storage of system variables, data structures, and stacks. The user provides this RAM anywhere in system

(continued on page 48)

COMBINATION PLATTER FOR DEC SYSTEM USERS.

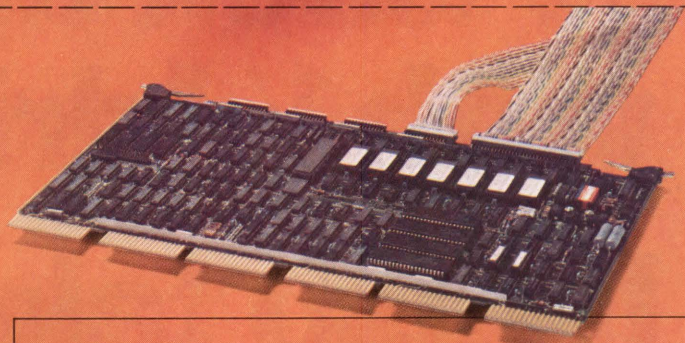
AED's new single-board controller mixes SMDs and Winchesters.

Chinese cuisine is probably the most eclectic in the world. The blending of carefully prepared foods with exotic herbs and spices is a centuries-old art developed to perfection by the Chinese and relished the world over.

DEC users will also relish the added system flexibility obtained with our new STORM 25™ controller board. It allows you to mix 80 and 300 megabyte storage module drives and SMD-compatible Winchesters in any combination you please. Up to four drives can be accommodated by this single-slot, HEX board controller. And there's no compatibility problem, because STORM 25's on-board firmware emulates the RM02 and RM05 disk systems, and is transparent to DEC's operating system and diagnostics. Media may be interchanged, too, because STORM 25's pack format is identical to that of the RM02 and RM03 (80 MB), or RM05 (300 MB).

Another tasty feature is STORM 25's external Writeable Control Store (WCS) capability. This allows the OEM or system user to functionally replace firmware control store memory. The STORM 25 hardware also provides a unique self-test capability that automatically tests all major functions of the controller 'in system'.

Unique configuration flexibility. Cost-effective multi-disk control. Plus easier field maintenance. STORM 25 is definitely a controller for disk connoisseurs. Call or Telex our Marketing Department today for the sales office nearest you. 30-day delivery. Advanced Electronics Design, Inc., 440 Potrero Ave., Sunnyvale, CA 94086. Phone 408-733-3555. Telex 357-498.

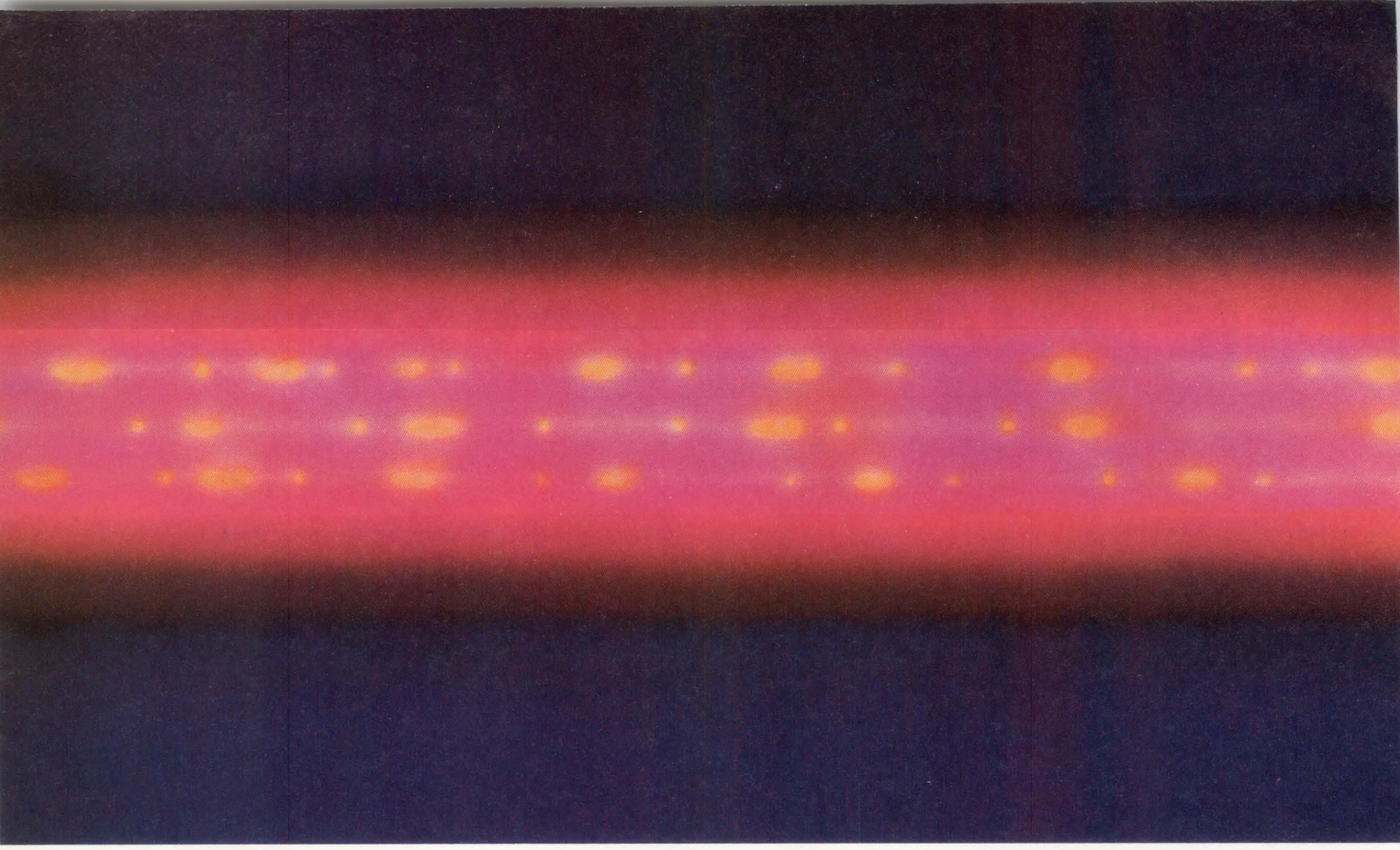


If normal bingo response time is too slow for your needs, please attach your business card to this coupon and mail today! Or call **(800) 824-7888.** From California call **(800) 852-7777.** Ask for operator 604.

ATTACH CARD HERE

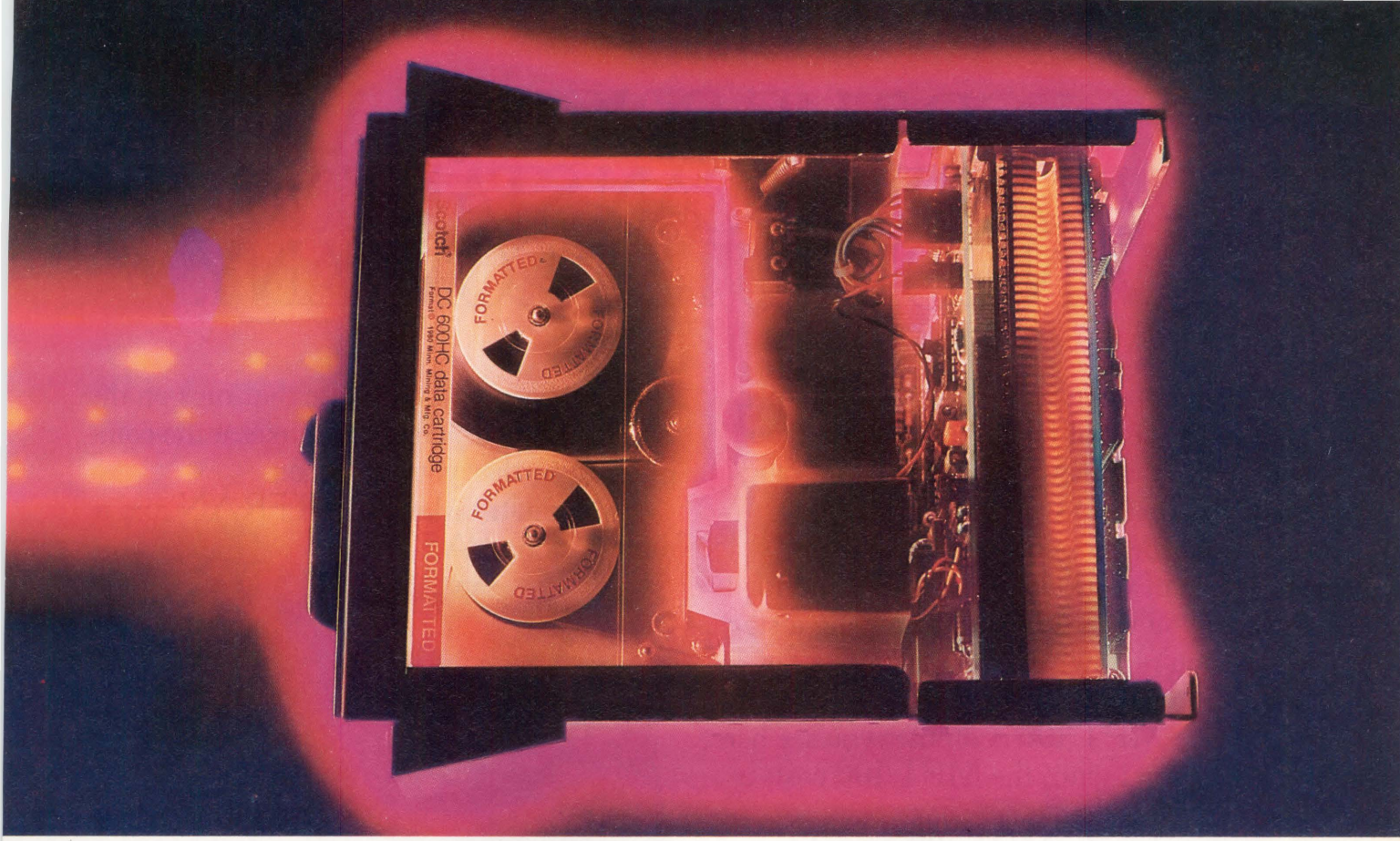
Advanced Electronics Design, Inc.
440 Potrero Ave., Sunnyvale, CA 94086. Phone 408-733-3555. Telex 357-498.

CIRCLE 20 ON INQUIRY CARD



It takes real nerve to compare our ¼" back-up system with ½" drives.

It also takes 67 megabytes.



HCD-75: so much for so little.

Presenting the only ¼" cartridge back-up system that'll go head to head with ½-inchers in the critical 30-70 Mbyte range.

The reason is simple. The 3M Brand HCD-75 Data Cartridge Drive System gives you 67 Mbyte per cartridge formatted. No other cartridge drive gives you so much capacity.

There's nothing medium about the medium, either. Each Scotch® DC 600HC cartridge is pre-recorded with permanent forward/reverse-reading block keys. They give you block-addressable storage. You get compact recording on all 16 tracks, with a density of 10,000 frpi, without rewinds.

The HCD-75 system, including drive and controller, is about one-fifth the size of a ½" tape drive. You don't have to put back-up and I/O plans on the back burner because of size constraints.

Interchange for the better.

Cartridges interchange quickly and easily. Tape-to-head alignment is ensured by a special sub-routine. It automatically aligns the read-write head and stepper motor controller to the tape edge each and every time the operator puts a cartridge in the system.

There's brain to this back-up, too. First, all its functions are handled through its controller. And second, there's minimal host involvement, so host time can be freed up for more critical functions.

All the reliability without high cost.

You can run one HCD-75 drive off the controller, or two, or three, or four. You still get all the reliability of the high-priced drives. The HCD-75 runs self-test routines to ensure proper operation. It gives you sophisticated error messages when faults are detected.

Advanced error-detection/correction routines keep working to deliver extremely low error rates. The micro-processor controls the drive functions; so potentiometer adjustments are a thing of the past.

Back-ups to go.

The total system—drive, controller, pre-formatted Scotch DC 600HC cartridges—is available to OEMs now. One at a time, or in evaluation quantities, you can take delivery on this reasonable, reliable, truly high-capacity alternative to ½" drives.

As close as your phone.

In fact, if you have been holding off on a back-up decision—or even if you haven't—make us put our back-up where our mouth is.

Call toll-free 800-328-1300. (In Minnesota, call collect: 612-736-9625.) Ask for the Data Recording Products Division. We'll give you the name of the 3M HCD-75 representative in your area. He's just waiting for the chance to show off his latest, greatest back-up.

Or write us at Building 223-5N, 3M Center, St. Paul, MN 55144.

3M hears you...

3M

CIRCLE 21 ON INQUIRY CARD

FOR THE PRICE OF A NEW CAR, YOU CAN START YOUR OWN COMPUTER COMPANY.

Skim through almost any newspaper and you'll see that for around $7,000 you can buy a basic new car. Perfect for going back and forth to work.

But for those of you who harbor ambitions of working for yourself, and for those of you who dream of becoming a star where you're now working, there is a far more prudent investment.

The MPT/100 computer you see here.

To start with, the MPT/100 costs a good deal less than a new car.

Besides, the MPT/100 can take you a good deal further.

Inside the MPT/100 you'll find a 16 bit microNOVA® computer. 64K bytes of memory. 80 column by 24 line screen. Full keyboard with numeric pad. 716 KB of on-line storage on 358 KB mini-diskettes.

Out back you'll find an I/O bus that accepts the standard microNOVA peripherals, including Data General Winchester-type disks. As well as your own interfaces. Two synchronous/asynchronous communications ports, programmable to 19.2K baud.

And a host of features many desktop computers don't even have as options.

Which is a lot of computer to find in a desktop computer that doesn't take up the whole desk.

As impressive as the hardware may be, it's the systems software that runs on the MPT/100 computer that makes it the computer to further your ambitions.

A multi-tasking FORTRAN and a multi-tasking PASCAL

that executes at assembly language speeds. An ANSI-compatible BASIC that lets you quickly write large programs that take up a small amount of space. A full range of user-friendly aids like a Command Line Interpreter, a Menu Editor, and a Debugger. And MP/OS, one of the most advanced operating systems in the industry.

With software like that, you can be out making a name for yourself while everybody else is trying to figure out how you did it.

You can take your big ideas anywhere in the world. Because the MPT/100 comes with the same worldwide support we give every Data General computer.

And when you start to carry a lot of weight in your industry, you can migrate all your software, all your peripherals, and everything you've learned. Because we've gone out of our way to make Data General computers get along with each other.

The point we're driving at is that this computer can help you do what a lot of other companies have done with other Data General computers.

Like Finnigan of Sunnyvale, California, one of the world's leading suppliers of Mass Spectrometers. They came to Data General partly because they had to write software elaborate enough to identify the fingerprints of over 30,000 chemicals. Partly because of our worldwide service. And partly because they didn't have to wait a year to get our computers.

Of course buying an MPT/100 may mean driving your present car a while longer. But look at it this way. A few years from now, maybe you'll be driving any car you jolly well please.

For more information about the MPT/100 computer, call your local Data General office, your Data General manufacturers representative, or one of the distributors listed below. Or write us at MS C-228, 4400 Computer Drive, Westboro, MA 01580.

Data General
We take care of our own.

MPT/100 computers are available for delivery from SCHWEBER, HALLMARK, KIERULFF, ALMAC/STROUM and R.A.E. in Canada.
microNOVA is a registered trademark of Data General Corporation.

memory. Applications are seen in such diverse multitasking areas as industrial control systems with complex I/O requirements, multifunction small business and personal computers, PABX equipment, multiuser/multidisc file servers, and transaction processing systems such as those used for electronic funds transfer.

The iAPX 86/30 and 88/30 are MULTIBUS™ compatible. Like the 8086 and 8088, the 80130 is fabricated with HMOS, the company's patented, metal oxide semiconductor process technology. The OS product is packaged in a 40-pin cerDIP. **Intel Corp**, 2625 Walsh Ave, Santa Clara, CA 95051.

Circle 243 on Inquiry Card

OS provides interface to CP/M based software

A software operating system, M/OS-80 provides a standard interface between CP/M™ or SD Series™ based user software and the MDX Series™ board level microcomputer products. The system is designed to run on Z80 based microcomputers using FLP-80DOS programs. The system is sold on a floppy disc which is bootable on any 32k, 48k, or 64k Mostek disc system.

Each file can be expanded well beyond the 256k CP/M limit to over 65M bytes. Random file accessing techniques, file protection attribute bytes, direct access to a system clock, and interrupt handling—features not often found on CP/M systems—are included on the recently announced OS. The system also includes over 14 utility programs not offered by CP/M. One such program activates the System Spooler, which acts like a separate task to print files while another task is simultaneously processed. The OS is shipped in three configurations to support several combinations of Mostek board level products. Four memory configurations for each of these systems provide 12 OS versions.

As a diskette only, the software is priced at $199. The diskette with bootstrap P/ROMs is $249. Unlimited reproduction rights are available for $1995. **Mostek Corp**, 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 244 on Inquiry Card

COMPUTERS

Maintenance processor in easy to use large computer system enables both local and remote diagnostics

Although both hardware and software offer sophisticated capabilities compared to previously announced 32-bit computer systems according to Microdata Corp officials, the SEQUEL™ system is "the first fast, powerful large system that's as easy to use as a small system." It is not intended to be a number cruncher for scientific applications; rather, it is described as an advanced information processor aimed at the commercial market—for people who are not computer professionals. One specific use might likely be in a standalone special purpose interactive application such as manufacturing control where process automation can now be handled on the plant floor.

One design objective when SEQUEL (then code-named "Sequoia") was being developed as the big brother to the

(continued on page 52)

MARINER DEPLOYED...

...expanding to eight Satellite Processors at down-to-earth cost!

Make MICROMATION's MARINER your entry-level system. System expansion is easy and inexpensive; plug in another Satellite processor card, connect a terminal, and you have multiprocessor, multitasking lift-off!

Each user has his own processor and 64K bytes of dynamic RAM, keeping MARINER performance up under loads that make single-processor systems sag. A separate 4-MHz Master processor and memory hold costs down by managing the sharing of MARINER's built-in 22M-byte Winchester disk drive, 8-inch floppy disk and 1/4-inch streaming tape drive.

There's nothing nebulous about MARINER's flexibility. Operate with CP/M, MP/M, or the new, high-speed DBOS (CP/M compatible) and you'll have a galaxy of software available for applications.

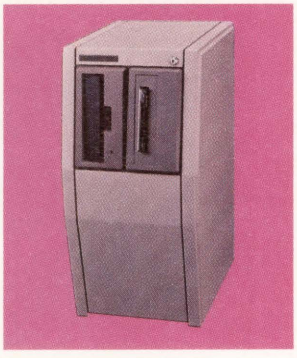
Program satellites with BASIC, COBOL, or FORTRAN, use them for word processing, general accounting, any of a multitude of tasks, each with complete independence.

And MARINER's M/LINK modem communicates at 2400 baud on standard voice-grade phone lines, using SDLC, BI-SYNC, or X.25. Sounds universal? MARINER is.

MARINER's attractive, freestanding cabinet houses the Master and up to eight Satellite processors. And it's only 14″ x 20″ x 29″ in size, so it fits in beautifully, quietly, anywhere!

Get a world of additional information about MARINER now by calling your MICROMATION dealer. If you need help in locating the dealer nearest you, or if you would like to hear about our special support program for systems integrators and OEM manufacturers, call MICROMATION now!

1620 Montgomery Street, San Francisco, CA 94111, 415/398-0289 TLX: 172457



The background to the MARINER system is a photograph of the Lagoon Nebula, which can be seen with the aid of binoculars in the constellation Sagittarius.

MICROMATION

CIRCLE 24 ON INQUIRY CARD

Now you can get a terminal as easy to use as a VT100 no matter what kind of terminal you need.

Up until now if you wanted VT100 quality in anything other than a VT100, you had two choices: Do without, or settle for something less.

Now Digital's created a family of VT100 terminals. All of them as easy to use as a VT100 because they're all made with the same high regard for people and the way they work.

The new VT125 business graphics terminal, for instance.

Affordable graphics for business and engineering.

It gives you what you'd expect in terms of durability and ease of use from a VT100. But what makes it an ideal graphics terminal is our new graphics instruction set called ReGIS (Remote Graphics Instruction Set).

With just a few simple lines of programming language, even an average programmer can run VT125 graphics off of your present minicomputer.

Then, with simple but powerful ReGIS commands, any operator can call up data and put it into graphic form with very little demand on the CPU.

The VT125 also writes text as well as it draws pictures, so what graphics fail to express, words can.

You can buy the VT125 as a complete terminal package. Or you can buy it as an option for the VT100 you already own.

Either way, it'll work like a charm on any system supporting ASCII terminals. As will any other terminal in the VT100 family.

This next one, for instance.

The economical VT101.

It can display 80 or 132 columns of data with smooth scroll. You can select double-height and double-width characters. And you can personalize it right from the keyboard . . . so you'll feel comfortable working with it.

But because the VT101 was designed with a little less power and option space than the VT100, it costs less.

Thus it's perfect for people who want a terminal as easy to use as a VT100 but not as powerful or expandable.

The VT101, we think, fills a very practical niche between too much terminal and not enough.

But suppose you need even more features to start out with?

The VT131. A new, fully optioned terminal.

You get advanced video features to make an operator's life easier and more productive. The VT131 also comes with a printer port, five full and half duplex protocols and full modem control.

With the VT131 you can select block mode or character operation from the keyboard.

All of these features are designed in a terminal package that, like the VT101, has less option space and power than a VT100.

Thus the VT131 also represents an affordable choice in terminals.

Then, of course, there's the VT100 itself.

Some have called it the "perfect" terminal.

Perfect for OEMs developing demanding applications. Perfect for people who'll want its power and space for additional options later on.

There are options now that'll turn a VT100 into a personal computer for the office, or into a business graphics terminal. Easily and affordably.

Many have called the VT100 the best video terminal ever made.

Imagine what they'll say about a whole family of them.

Hard copies from your terminals?

For printed copies, you can choose from the DECprinter III for exceptional throughput or the versatile DECwriter IV if your applications include graphics. One is probably perfect for you. Your Digital terminals dealer can help you decide.

To buy your terminals, see your local Digital terminals dealer or sales representative today or contact: **Digital Equipment Corporation,** Terminals Product Group, MR2-2/M67, One Iron Way, Marlboro, MA 01752. Telephone toll-free 800-225-9378 (outside the continental U.S. or in Massachusetts call 617-467-7068) between 8:30am and 5:00pm Eastern time. In Europe: Digital Equipment Corporation International, 12 Av. des Morgines, CH-1213 Petit-Lancy/Geneva. In Canada: Digital Equipment of Canada, Ltd.

digital

We change the way people work.

company's REALTY® series of small computers was to enable execution of machine instructions at least 8 times faster than REALITY. Benchmarks to date indicate that some applications run 50 times faster, and others, which require high levels of disc activity, run just barely 2 times faster. On the average, and again dependent on application mix, the company claims performance up to 10 times faster than that of small business systems. To meet another objective, that of enabling many more users to operate the machine, system designers increased processor bandwidth. Now as many as 127 interactive terminals can be operated simultaneously.

Basic processor technology is based on 2901 bit slice architecture with numerous Z80 type microprocessors as special task controllers. Storage capacity of the system is up to 2M bytes of main memory (16k chips) and 1G byte of disc capacity. Special function independent processors handle I/O and local and remote diagnostics, with single-bit architecture, intelligent controllers functioning through a DMA multiplexer, and 16 DMA channels. An I/O processor interfaces with disc controllers and communications controllers through the data bus. In addition, according to Microdata senior scientist Richard Vahlstrom, a diagnostic maintenance processor (DMP) enables remote control of the CPU and also serves as a local controller. One CRT terminal acts as an interface to the DMP, performing all initialization and setup of the system.

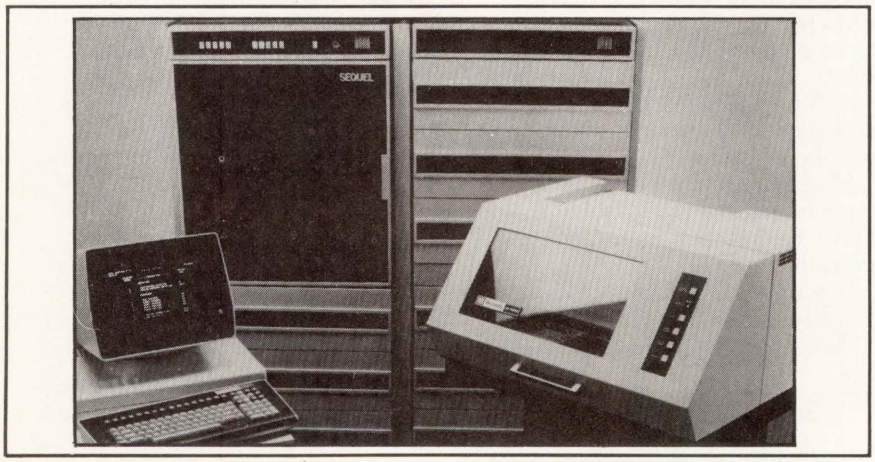
The company, it is said, has made an effort to include more diagnostics in this machine than it had in the past—firmware and software level diagnostic capabilities built into SEQUEL are much improved compared with earlier, similar products. For example, using modems and a telephone line, software on a system located in New York can be debugged to the PCB level remotely from the home office in California.

To obtain the necessary high power of the CPU, a separate processor, running independent from the CPU, fetches, parses, and places instructions into proper locations. It runs with a simple program and sets up all software instructions used by the CPU. Microdata software engineer Terry Johnson has stated that whereas instruction decoding on previous computers required as much as 40% of the CPU's time, the separate processor reduces that time to about 5% by decoding in parallel to the CPU. He also stressed that a significant difference between SEQUEL and other 32-bit systems is its software architecture, which allows users to share data without being aware that they are sharing.

SEQUEL hardware is designed to handle frames, each consisting of 512 bytes of data, that could be either in main memory or on disc. Firmware automatically brings data into memory whenever they are accessed. When a software instruction is executed, hardware determines the location of referenced data. If in main memory, there is immediate access.

Standard program languages include DATA/BASIC and English®, a database language that permits programmers to enter commonly used words rather than codes to generate reports. An additional option, ALL™ (application language liberator), is claimed to reduce development, testing, and debugging time, virtually eliminating programming. ALL is not designed to replace analysts responsible for system design, but it does save

(continued on page 56)



32-bit SEQUEL large business system. Features include up to 2M bytes main memory and 1G-byte disc capacity. System supports simultaneous access by up to 127 users via CRT terminals. Ease of use is augmented by ALL, an application development tool that virtually eliminates programming

The most complete line of Interface Products for PDP*-11, LSI-11 and VAX* Computers with features you can't get anywhere else

For DEC users... MDB makes the difference!

You *can* have it all! Along with the benefits of your DEC computer, you can get interface products that significantly extend the capability, flexibility and economy of DEC systems. MDB makes more DEC system boards than any independent manufacturer—some with plain vanilla compatibility; others with plain incredible performance boosting features. For example—

- Line printer controllers for every major line printer, with complete self-testing capability and optional RS-422 "long lines."
- Peripheral device controllers for card readers, X-Y plotters, electrostatic printer/plotters and paper tape readers/punches.
- DZ11 compatible multiplexors for LSI-11 and PDP-11 users; some combine RS-232 and current loop or RS-422 with a single board.
- High speed synchronous serial interfaces; one DUP-11 compatible model has all bit and byte protocols even for LSI plus X.25 capability.
- Inter processor links between Unibus computers or between Unibus and Q-bus.
- System modules including DMA modules with RS-422, general purpose parallel and digital I/O interfaces, an IEEE 488 bus controller and a programmable real time clock.
- PROM memory modules, some with an on-board PROM programmer.
- General purpose interface and bus foundation modules.
- LSI-11 based subsystems and systems with capabilities like TU-58 cartridge storage and memory management.
- LSI-11 system boxes with 22-bit addressing and switching power supplies.

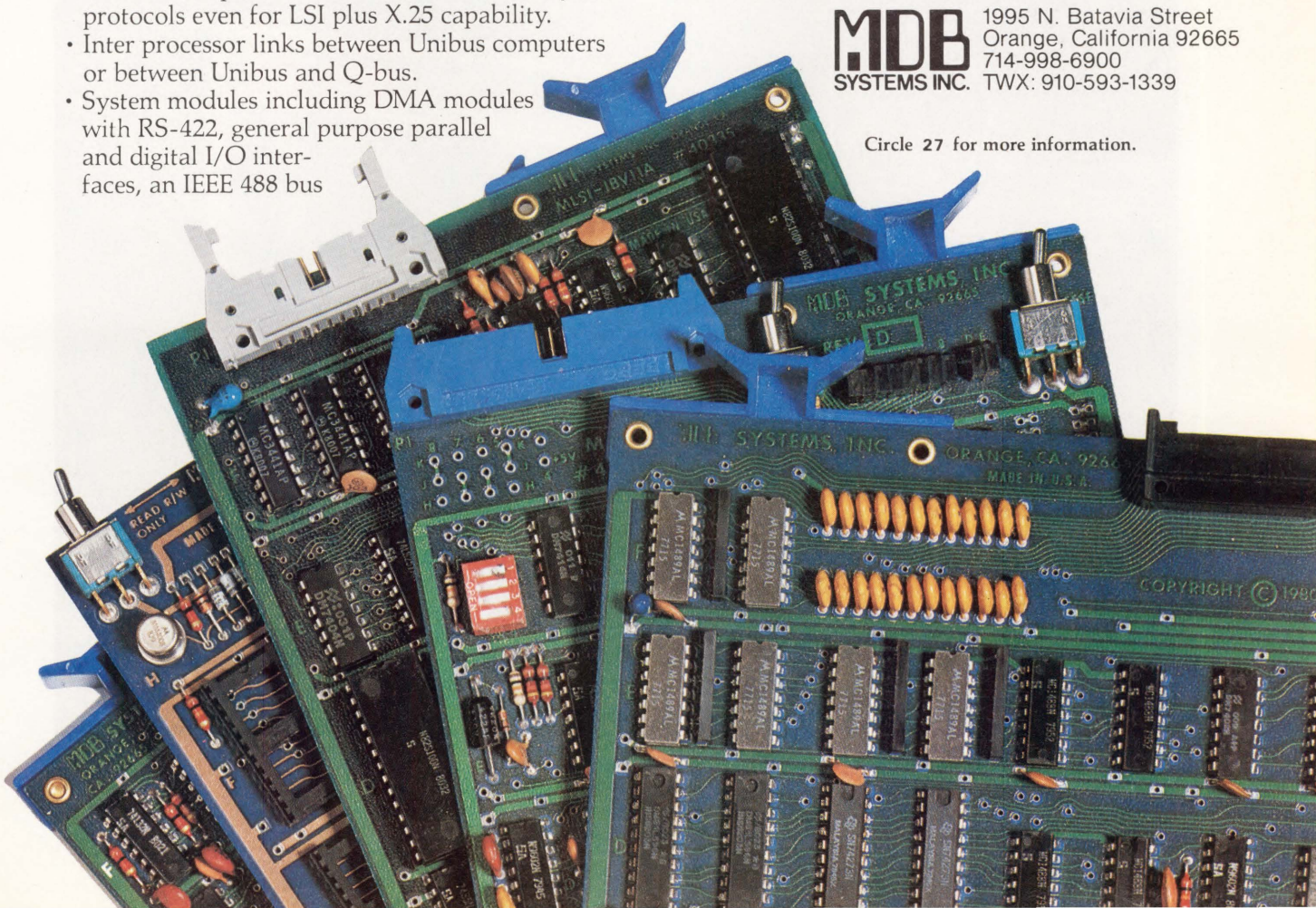
In addition to the DEC compatible products, MDB also manufactures comparable interfaces for Data General, Perkin-Elmer, Intel and IBM Series/1 computers. All MDB products are available under GSA contract #GS-00C-02851.

Give your DEC system *all* the benefits. Discover the difference MDB interface products can make.

*Trademark Digital Equipment Corp.

MDB SYSTEMS INC.
1995 N. Batavia Street
Orange, California 92665
714-998-6900
TWX: 910-593-1339

Circle 27 for more information.



Shown from top to bottom: CM 16/DS2 Multiprocessor System; CMT 68000 CPU; CM 16/DS2 Storage Subsystem.

CMS Series 16

The Complete Family Of 68000 Systems And Products.

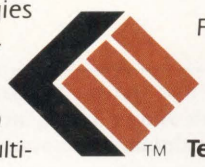
CM Technologies presents a complete family of Multibus*-compatible computer products and systems based on the Motorola 68000. From our CMT 68000 16-bit single board computer to the CMS Series 16 Multiprocessor Systems, you can choose the state-of-the-art solution to increase your system performance and reduce development time and risks.

The CMT 68000 CPU board provides system designers with a high-performance 68000-based single board computer including 64K of dual ported RAM. The CMT 68000 CPU is also available set in an industry-standard 19" chassis, 9-slot Multibus card cage with serial I/O ports and power supply. Either way, you get the most powerful 16-bit microprocessor available today in the popular Multibus standard which will help speed your product to market.

For software development, CM Technologies offers a range of options. Using the CMS 16/DS1, software may be developed on any DEC** PDP-11** and the finished program downloaded to and debugged on the CMT 68000 CPU. The top of the line is the CMS 16/DS2 Multiprocessor System, a powerful CP/M‡ based computer system with dual processors, which functions as a stand alone, real-time development system. A Z80† CPU functions as an I/O controller or a bus master to run CP/M application software. A CMT 68000 CPU runs the main program and is the execution vehicle for developing custom applications. For storage, the CMS 16/DS2 provides a built-in 11 Megabyte Winchester drive and a dual-sided, double-density floppy disk.

When you add it all up, CM Technologies delivers the family of state-of-the-art products you need for product development. Best of all, they're available now, so you can start designing today.

*Multibus is a registered trademark of Intel Corporation. **DEC and PDP are registered trademarks of Digital Equipment Corporation. ‡CP/M is a registered trademark of Digital Research, Inc. †Z80 is a registered trademark of Zilog, Inc.



For more information, call or write:

CM Technologies
525 University Avenue
Palo Alto, CA 94301 415/326-9150
Telex: 334417 Cable: CHIMINGCO

time by eliminating the need to develop documentations. Every application is developed and documented the same way, and therefore can be easily changed. ALL is self-documenting—upon completion of the application, the operator's instructions and application specifications are automatically printed out.

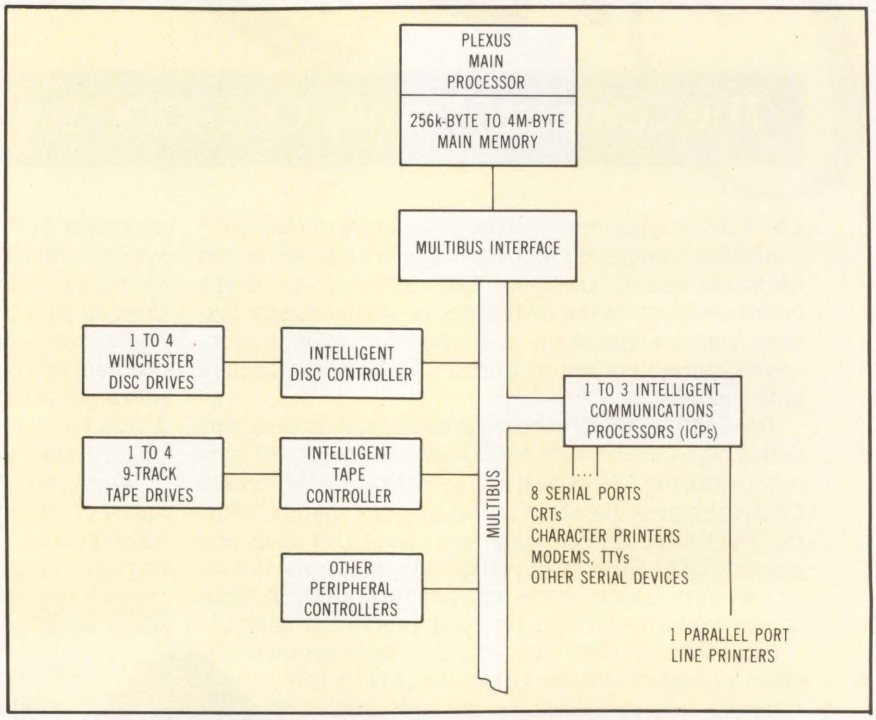
In essence, according to Gerald Fleming, vice president of corporate marketing, SEQUEL is a "super REALITY" that runs much faster and offers both improved performance and larger memory. The design target of being an easy system to use was given equal importance by the company and has been met.

A basic SEQUEL system—including four CRT terminals, 1M byte of main memory, 256M bytes of disc memory, one magnetic tape drive, and one 300-line/min printer—is priced at $155,500. ALL is available optionally for a one-time licensing fee of $22,700. **Microdata Corp**, 17481 Red Hill Ave, Irvine, CA 92714.

—Sydney F. Shapiro, Managing Editor

Circle 245 on Inquiry Card

Compatible base architecture to optimize UNIX operating system



Plexus P/40 system. Industry standard hardware with extensive use of DMA channels allows intelligent controllers to offload tasks from main processors, while maintaining response time for up to 24 terminals

Specifically designed to run the UNIX operating system, Plexus P/40 computer utilizes a compatible base architecture concept to optimize the characteristics of UNIX. Plexus accomplishes this and also maintains flexibility and expansion paths for the OEM by using a distributed processing architecture that allows offloading of specialized tasks to separate processors and the standard MULTIBUS™. Thus every controller has its own processor, and different capabilities can be easily added by plugging in MULTIBUS cards that are available for a wide variety of functions.

In addition to taking advantage of UNIX multiprogramming and multi-user capabilities, the P/40 hardware design relieves some constraints imposed by a timeshared operating system. Since UNIX is memory and disc intensive, a DMA channel between disc and main memory, with a bandwidth of 3M bytes/s speeds disc transfers and overlays. A memory manager handles memory mapping and transfers between main memory and the peripheral controllers. Since UNIX is not a realtime operating system, its handling of interrupts is impaired; however, this situation is improved by multiple processors and intelligent controllers.

Memory consists of increments of 256k bytes using high speed 16k dynamic

(continued on page 59)

ROMs

MOS STATIC ROMs (+5 Volts)

Character Generators[3]

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × (7 × 5)	MCM6670P	350	18
128 × (7 × 5)	MCM6674P	350	18
128 × (9 × 7)	MCM66700P	350	24
128 × (9 × 7)	MCM66710P	350	24
128 × (9 × 7)	MCM66714P	350	24
128 × (9 × 7)	MCM66720P	350	24
128 × (9 × 7)	MCM66730P	350	24
128 × (9 × 7)	MCM66734P	350	24
128 × (9 × 7)	MCM66740P	350	24
128 × (9 × 7)	MCM66750P	350	24
128 × (9 × 7)	MCM66760P	350	24
128 × (9 × 7)	MCM66770P	350	24
128 × (9 × 7)	MCM66780P	350	24
128 × (9 × 7)	MCM66790P	350	24

Binary ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
1024 × 8	MCM68A308P	350	24
1024 × 8	MCM68A308P7[4]	350	24
1024 × 8	MCM68B308P	250	24
2048 × 8	MCM68A316AP	350	24
2048 × 8	MCM68A316EP	350	24
2048 × 8	MCM68A316EP91[4]	350	24
4096 × 8	MCM68A332P	350	24
4096 × 8	MCM68A332P2[4]	350	24
8192 × 8	MCM68A364P	350	24
8192 × 8	MCM68A364P3[4]	350	24
8192 × 8	MCM68B364P	250	24
8192 × 8	MCM68365P25	250	24
8192 × 8	MCM68365P35	350	24
8192 × 8	MCM68366P25	250	24
8192 × 8	MCM68366P35	350	24

CMOS ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256 × 4	MCM14524	1200	16
2048 × 8	MCM65516P43	430	18
2048 × 8	MCM65516P43M[4]	430	18
2048 × 8	MCM65516P55	550	18

[3]Character generators include shifted and unshifted characters, ASCII alphanumeric control, math, Japanese, British, German, European and French symbols.

[4]Standard Patterns for MOS ROMs:
MCM68A308P7 – MC6800 MIKbug/MINIbug ROM
MCM68A316EP91 – Universal Code Converter and Character Generator
MCM68A332P2 – Sine/Cosine Look-Up Table
MCM68A364P3 – Log/Antilog Look-Up Table
MCM65516P43M – MC146805 Monitor Program

PROMs

ECL PROMs

Organization	Part Number	Access Time (ns max)	No. of Pins
32 × 8	MCM10139	20	16
256 × 4	MCM10149	25	16

TTL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
512 × 8	MCM7641*	70	3-State	24
1024 × 4	MCM7643	70	3-State	18
1024 × 8	MCM7681	70	3-State	24
2048 × 4	MCM7685	70	3-State	18
2048 × 4	MCM7689	–	3-State with Registers	20
2048 × 8	MCM76161*	80	3-State	24

Not all package options are listed.

Operating temperature ranges:
MOS – 0°C to 70°C
ECL – Consult individual data sheets
TTL – Military –55°C to +125°C, Commercial 0°C to 70°C

MOTOROLA MEMORIES

Motorola has developed a very broad range of reliable MOS and bipolar memories for virtually any digital data processing system application. And for those whose requirements go beyond individual components, Motorola also supplies Memory Systems and Micromodules.

New Motorola memories are being introduced continually. **This selector guide lists all those available as of December 1981.** For later releases, additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

Data sheets may be obtained from your in-plant VSMF Data Center, distributors, Motorola sales office or by writing to:

Literature Distribution Center
Motorola Semiconductor Products Inc.
P.O. Box 20912
Phoenix, AZ 85036.

MOTOROLA MEMORIES Selector Guide

RAMs
ROMs
PROMs
EPROMs
EEPROMs

December 1981

MOTOROLA

MOTOROLA

RAMs

MOS DYNAMIC RAMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
4096 × 1	MCM4027AC-2	150	+12, ±5 V	16
4096 × 1	MCM4027AC-3	200	+12, ±5 V	16
4096 × 1	MCM4027AC-4	250	+12, ±5 V	16
16384 × 1	MCM4116BP15	150	+12, ±5 V	16
16384 × 1	MCM4116BP20	200	+12, ±5 V	16
16384 × 1	MCM4116BP25	250	+12, ±5 V	16
16384 × 1	MCM4517P10	100	+5 V	16
16384 × 1	MCM4517P12	120	+5 V	16
16384 × 1	MCM4517P15	150	+5 V	16
16384 × 1	MCM4517P20	200	+5 V	16
32768 × 1	MCM6632L15[1]	150	+5 V	16
32768 × 1	MCM6632L20[1]	200	+5 V	16
32768 × 1	MCM6632L25[1]	250	+5 V	16
32768 × 1	MCM6633L15	150	+5 V	16
32768 × 1	MCM6633L20	200	+5 V	16
32768 × 1	MCM6633L25	250	+5 V	16
65536 × 1	MCM6664AL12[1]*	120	+5 V	16
65536 × 1	MCM6664L15[1]	150	+5 V	16
65536 × 1	MCM6664AL15[1]*	150	+5 V	16
65536 × 1	MCM6664L20[1]	200	+5 V	16
65536 × 1	MCM6664L25[1]	250	+5 V	16
65536 × 1	MCM6665AL12*	120	+5 V	16
65536 × 1	MCM6665L15	150	+5 V	16
65536 × 1	MCM6665AL15*	150	+5 V	16
65536 × 1	MCM6665L20	200	+5 V	16
65536 × 1	MCM6665L25	250	+5 V	16

TTL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
256 × 4	MCM93422	45	3-State	22
256 × 4	MCM93L422*	60	3-State	22
256 × 9	MCM93478*	60	3-State With Latches	22
256 × 9	MCM93479*	45	3-State	22
1024 × 1	MCM93415	45	Open Collector	16
1024 × 1	MCM93425	45	3-State	16

*To be introduced.

[1]Motorola's innovative pin #1 refresh

[2]All MOS memory outputs are three-state except the open collector MCM2115A series.

MOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × 8	MCM6810	450	24
128 × 8	MCM68A10	360	24
128 × 8	MCM68B10	250	24
1024 × 4	MCM2114P20	200	18
1024 × 4	MCM2114P25	250	18
1024 × 4	MCM2114P30	300	18
1024 × 4	MCM2114P45	450	18
1024 × 4	MCM21L14P20	200	18
1024 × 4	MCM21L14P25	250	18
1024 × 4	MCM21L14P30	300	18
1024 × 4	MCM21L14P45	450	18
1024 × 1	MCM2115AC45[2]	45	16
1024 × 1	MCM2115AC55[2]	55	16
1024 × 1	MCM2115AC70[2]	70	16
1024 × 1	MCM21L15AC45[2]	45	16
1024 × 1	MCM21L15AC70[2]	70	16
1024 × 1	MCM2125AC45	45	16
1024 × 1	MCM2125AC55	55	16
1024 × 1	MCM2125AC70	70	16
1024 × 1	MCM21L25AC45	45	16
1024 × 1	MCM21L25AC70	70	16
4096 × 1	MCM6641P20	200	18
4096 × 1	MCM6641P25	250	18
4096 × 1	MCM6641P30	300	18
4096 × 1	MCM6641P45	450	18
4096 × 1	MCM66L41P20	200	18
4096 × 1	MCM66L41P25	250	18
4096 × 1	MCM66L41P30	300	18
4096 × 1	MCM66L41P45	450	18
4096 × 1	MCM2147C55	55	18
4096 × 1	MCM2147C70	70	18
4096 × 1	MCM2147C85	85	18

CMOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256 × 4	MCM5101P65	650	22
256 × 4	MCM5101P80	800	22
256 × 4	MCM51L01P45	450	22
256 × 4	MCM51L01P65	650	22

ECL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	No. of Pins
8 × 2	MCM10143	15	24
256 × 1	MCM10144	26	16
16 × 4	MCM10145	15	16
1024 × 1	MCM10146	29	16
1024 × 1	MCM10146A*	10	16
128 × 1	MCM10147	15	16
64 × 1	MCM10148	15	16
256 × 1	MCM10152	15	16
256 × 4	MCM10422*	15	24
4096 × 1	MCM10470*	35	18
1024 × 4	MCM10474*	25	24

EPROMs

MOS EPROMs

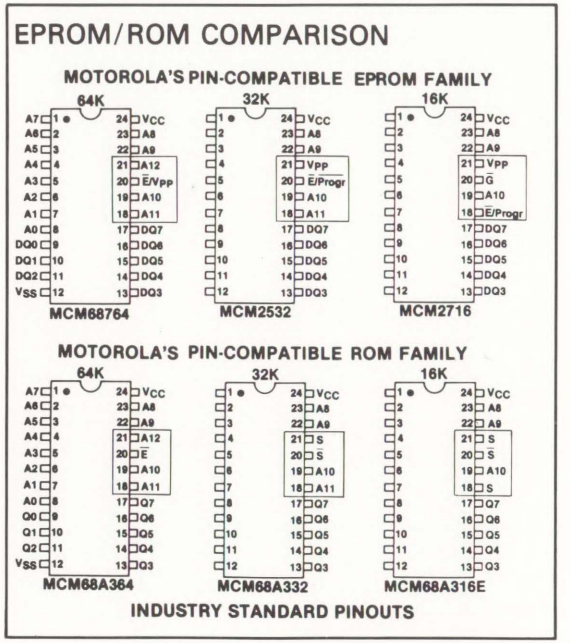
Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
1,024 × 8	MCM2708C	450	+12, ±5 V	24
1024 × 8	MCM27A08C	300	+12, ±5 V	24
2048 × 8	TMS2716C	450	+12, ±5 V	24
2048 × 8	TMS27A16C	300	+12, ±5 V	24
2048 × 8	MCM2716C	450	+5 V	24
2048 × 8	MCM2716C35	350	+5 V	24
4096 × 8	MCM2532C	450	+5 V	24
8192 × 8	MCM68764L	450	+5 V	24
8192 × 8	MCM68766L	450	+5 V	24
8192 × 8	MCM68766L35	350	+5 V	24

EEPROMs

MOS EEPROMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
16 × 16	MCM2801P	10 μs	+5 V	14
32 × 32	MCM2802P*	15 μs	+5 V	14

EPROM/ROM COMPARISON



RAMs, expandable to 4M bytes. Organized as 22-bit words with 16 bits for data and 6 error correcting bits per word, memory performs single-bit error detection and correction, and double-bit error detection. Cycle time, with error detection and correction, is 600 ns.

The multiple processor architecture of the P/40 allows it to accept up to 8 processors, including the main or job processor; intelligent communications processors (ICPs) which handle serial communications; disc and tape controllers; and additional intelligent controllers selected by the user. Giving controllers local processing and memory greatly reduces the number of interrupts the job processor is called upon to handle, and potentially increases the number of interrupt levels in the system to several thousand. (See illustration.)

Based on the 16-bit Z-8000, the main processor includes a floating point processor that can perform single precision (32-bit) or double precision (64-bit) arithmetic functions. A battery operated realtime clock remains operational even when the system is powered down and gives the processor continuous time and date information. This feature, along with firmware power-up and self-test programs, allows a user to start up the system with a single switch.

System is designed to optimize UNIX operating system developed by Bell Laboratories. Typical 8-user Plexus P/40 has 512k bytes main memory, 72M bytes disc storage, 8-channel ICP, and 9-track tape unit

The intelligent communications processor, ICP, is designed to offload serial I/O tasks from the job processor. The ICP's onboard Z-8000 controls serial communications with eight RS-232 channels at 19.2k baud, performs buffering, and handles data transfers between the ICP and main memory. In addition to serial ports, the ICP has one parallel Centronics type port and nine DMA channels, each associated with a communications port. Data transfers between the ICP and main memory take place via the DMA channels.

Communication between the ICP and main processor takes place via command and status blocks located in main memory, which are controlled by the ICP's processor. The ICP can address 64k bytes, the lower 48k (16k are P/ROM) on its local board, and the upper 16k mapped into main memory by the system's memory manager. Plexus P/40 can handle up to three ICPs for a total of 24 users.

Other intelligent controllers supplied with the basic system include a disc controller, a storage module drive (SMD) type handling up to four 145M-byte Winchester drives; and a tape controller likewise handling up to four tape drives. The disc controller can detect an erroneous data burst up to 32 bits in length and correct a burst up to 11 bits long. It uses a 32-bit error code that it appends to each sector ID or data field when that field is written to disc. The 0.5″ (1.3 cm), 9-track 1600-bit/in tape subsystem can operate in streaming mode and back up 46M bytes in 4.8 min, or in conventional mode compatible with ANSI/IBM for exchanging data among computers. (See photo.)

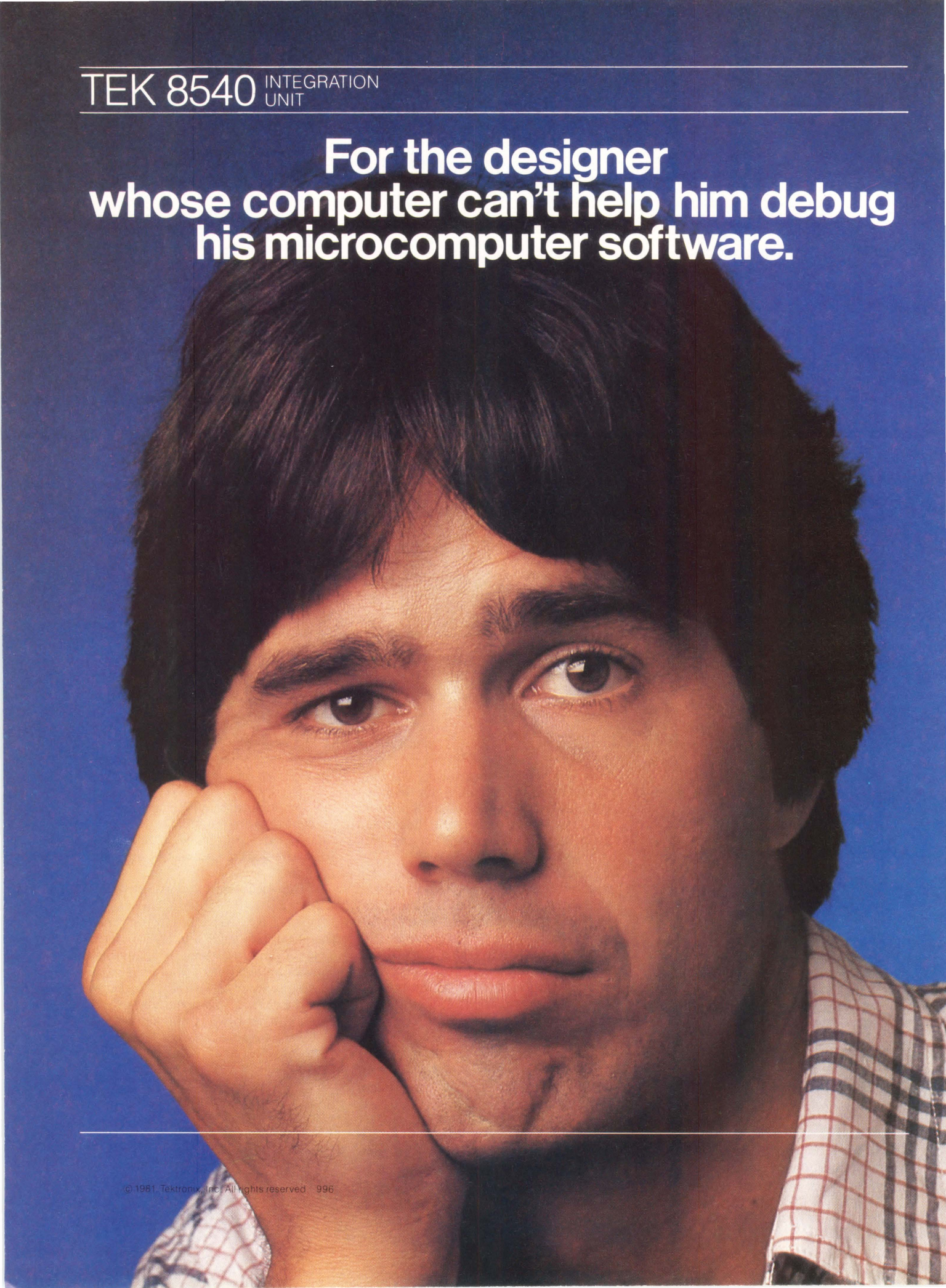
Plexus deliberately chose Bell Labs UNIX Version 7 operating system, licensed from Western Electric, rather than license or write a UNIX-like system. The rationale was that programs that would run under UNIX would most likely run under systems similar to UNIX, but that the reverse was not necessarily the case. Also provided is a C compiler and a Z-8000 assembler. **Plexus Computers**, 2230 Martin Ave, Santa Clara, CA 95050.

—Thomas Williams
West Coast Managing Editor

Circle 246 on Inquiry Card

TEK 8540 INTEGRATION UNIT

For the designer whose computer can't help him debug his microcomputer software.



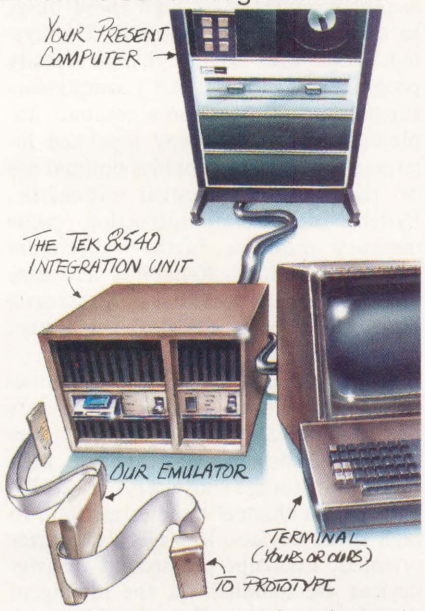
Tek announces the 8540 Integration Unit.

When designing with microcomputers, your resident host computer can be a powerful ally in the fight against impossible design schedules.

But, ultimately, it only gets half the job done.

Even though it gives you everything you need for fast, accurate code development, you still have to install and debug your developed code in the prototype hardware. A process that often consumes half your total design time.

Enter the 8540 Integration Unit.

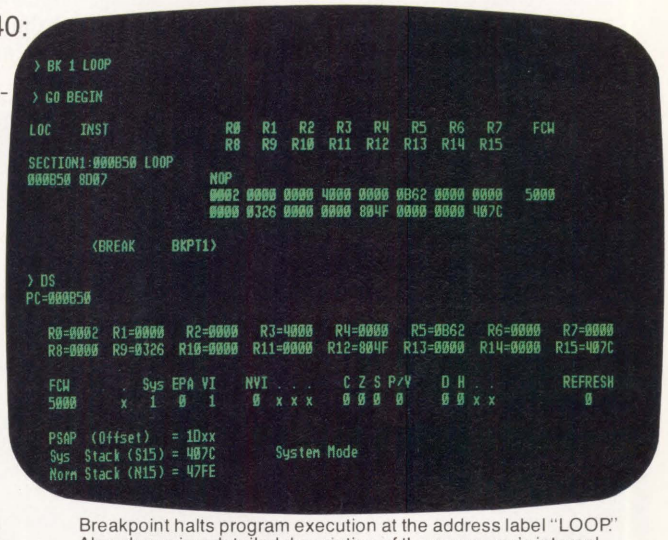


When it comes to hardware/software integration, Tektronix has the answer. The 8540 Integration Unit. It interfaces easily with almost any host computer using ASCII terminal communications. And, once connected, its high-performance emulators and debug software handle the entire integration process.

All with an unmatched range of chip support.

Your host & the 8540: A synergistic team.

The 8540's sophisticated interface features make the most out of your host's processing power. Like the ability to download symbolic debug tables along with object code to the 8540. Or permanently store your specialized, host-oriented debug commands aboard the 8540 as either key words or command strings.



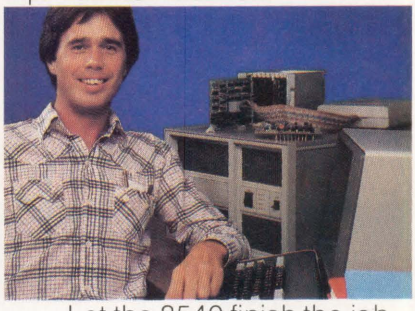
Breakpoint halts program execution at the address label "LOOP." Also shown is a detailed description of the processor's internal status at the breakpoint.

To retain any terminal-oriented command structures you've developed, the same terminal can be used for direct communication with either the 8540 or the host system. There's even a local printer interface on the 8540 so its printing operations won't burden the host.

A Trigger Trace Analyzer for real-time prototype monitoring.

In many applications, the timing of code execution becomes critical. To fully support real-time debugging, the 8540 includes an optional Trigger Trace Analyzer. It has four trigger channels ready to track down even the remotest sections of code execution.

You can do things like identify all non-ASCII writes to an I/O port. Or count the number of calls to a specific subroutine. Or measure the elapsed time of an interrupt handler routine.



Let the 8540 finish the job your computer started.

Contact your nearest Tektronix field office about buying or renting the 8540.

Chips The 8540 I.U. Supports:	
16-bit	8-bit
Z8001 Z8002 8086 68000	6809 6800 6808 6802 Z80A 8080A 8085A 8049 8088 8048 8039 8039-A 8035 8021 8022 8041A

U.S.A., Asia, Australia, Central & South America, Japan Tektronix, Inc., P.O. Box 4828, Portland, OR 97208. Phone: 800 547-6711, Oregon only 800 452-6773. Telex: 910-467-8708. Cable: TEKTRONIX

Europe, Africa, Middle East Tektronix International, Inc., European Marketing Centre, Postbox 827, 1180 AV Amstelveen, The Netherlands, Telex: 18312

Canada, Tektronix Canada Inc., P.O. Box 6500, Barrie, Ontario L4M 4V3, Phone: 705 737-2700

Tektronix®
COMMITTED TO EXCELLENCE

Circle 31 for Literature
Circle 32 for Sales Contact

Midsize 32-bit computer lowers cost of virtual memory addressability

A midsize 32-bit machine, the ECLIPSE MV/6000™ complements Data General's larger MV/8000™ by offering the same virtual storage addressability at a lower price. Available with up to 2M bytes of main memory and ability to handle up to 2.5G bytes of online mass storage, the machine can operate up to 64 user terminals simultaneously.

The 32-bit system, packaged compactly in a rackmounted chassis, is designed for users who need the large memory addressability of a virtual storage implementation but also require less power than the larger MV/8000. The system efficiently manages its address space of up to 4G bytes for each user within a physical memory that ranges between 1M and 2M bytes. User programs of up to 2G bytes are supported. Management of large logical address space is handled by the virtual memory management system integrated into AOS/VS.

Compatibility with the entire ECLIPSE family contributes to high performance and ease of use. Because MV/6000 architecture is an extension of the 16-bit ECLIPSE design, instructions for 32-bit functions coexist with 16-bit instructions. Users can operate or develop programs for 16-bit systems while operating and developing programs for 32-bit computers without losing efficiency.

Special hardware components incorporated in the system improve program execution and accelerate operating system functions. Several special function processors allocate resources, offloading the central processor. These processors are interconnected by high speed buses to deliver high performance. The system's CPU uses advanced high density program array logic (PAL®) components for high performance in a compact implementation. The 4-way pipelined instruction processor provides optimal use of the system's central processor. System cache and instruction cache memory modules further accelerate system operations. Reliability and easy maintenance are provided by an integral diagnostic processor, called the system control processor.

MV/6000 incorporates a 3-level independent I/O facility. A 16.16M-byte/s burst multiplexer channel (BMC) handles direct memory access through high speed disc storage subsystems. A 2.27M byte/s data channel handles medium to high speed devices; low speed character oriented, interrupt per second transfer devices are handled via the intelligent asynchronous controllers (IACs).

An extensive set of both hardware and software products allows expansion. Peripheral support includes disc drives ranging from 12.5M-byte Winchester to 277M-byte removable subsystems; 800- and 1600-bit/in magnetic tape drives; line printers with speeds of 300 to 900 lines/min; and several synchronous and asynchronous communications controllers.

The system operates under 32-bit AOS/VS, an intelligent, multiprogramming software system that controls concurrent timesharing, batch, and online operations for both 16- and 32-bit processes. It constantly monitors all processes, automatically adapting the system to both user priorities and

(continued on page 66)

Are you a systems house or minicomputer OEM?

We're MICOM, and we can help you make more money.

We specialize in *data communications for minicomputer users.* Our products are meant for *your customers,* to allow the "dumb" terminals they use with minicomputer systems to operate properly over telephone lines—error-free and at lower cost.

We want to help you too, by making it easy for you to sell turnkey systems with data communications. When faced with a remote terminal application, or a sale involving data communications, many OEM's choose to ignore the communications components. This not only costs them *the profit they could make,* but also makes their bids less attractive to customers looking for a single source of supply. And it drives up the overall system price without adding to profits.

Let the telephone company handle the data communications? Sure, and let your customer pay a fortune in telephone charges—while keeping him from running his terminals as fast as he'd like. To add insult to injury, occasional phone line "glitches" will drive his CRT's crazy—and you, not the phone company, will be the first to hear about it.

At MICOM, we build smart little boxes that keep glitches from having any effect. Our products provide error control for dumb terminals and allow several of them to share one telephone line. More than 30,000 of our data concentrators and error controllers are already in service, installed by their users as painlessly as plugging in a terminal. (With some of those customers supporting four 2400 bps CRT's on a single 2400 bps line, no wonder these products are so easy to sell.)

MICOM is helping systems houses and OEM's concentrate on profits. We'll give you the training you need, the OEM discounts you expect, plus the service and support you demand from any good supplier. We'll also give you the technical tips you'd otherwise have to learn the hard way.

Call or send today for our free booklet "Data Communications for Minicomputer Users." It could put you in a whole new add-on business.

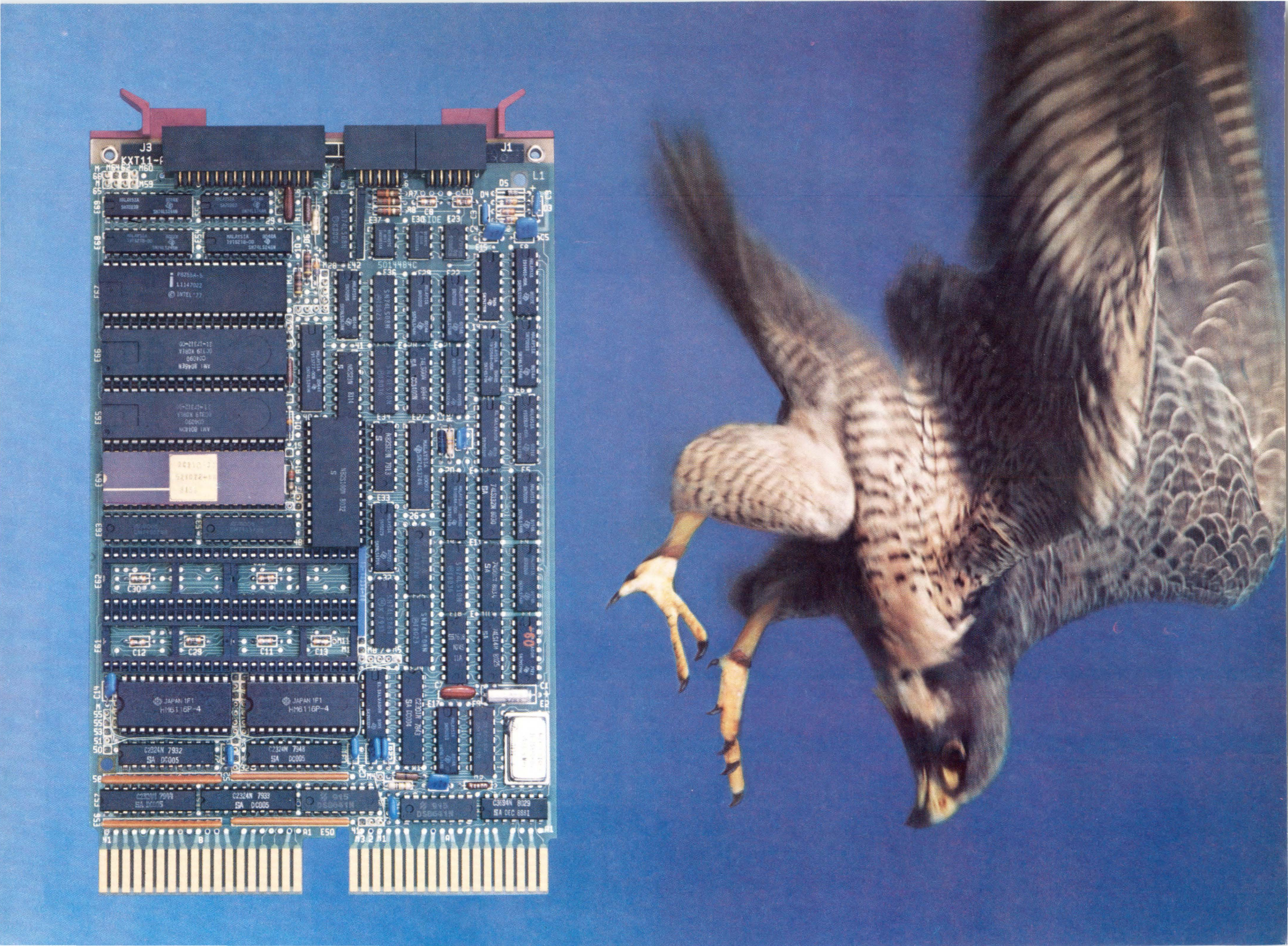
MICOM® MicroComputers for DataCommunications™

MICOM SYSTEMS, INC. • 20151 Nordhoff Street • Chatsworth, CA 91311 • Telephone (213) 882-6890 • TWX 910/494-4910
Regional Sales and Service • Eastern: Woodbridge, NJ (201) 750-1120 • Central: St. Louis, MO (314) 576-7626
Regional Sales Offices • Atlanta, GA (404) 435-2999 • Boston, MA (617) 235-8870 • Dallas, TX (214) 258-0774
MICOM-BORER LTD. • Bel Court • 15 Cradock Road • Reading, Berkshire RG20JT, England • (0734) 866801 • Telex 847135

Available now from these stocking reps...

AK: Anchorage (907) 276-5616/Juneau (907) 789-3310 ● **AL:** (800) 327-6600 ● **AR:** (214) 620-1551 ● **AZ:** (602) 994-5400 ● **CA:** Anaheim (714) 635-7600/Lodi (209) 334-1961 San Diego (714) 565-1557/Santa Clara (408) 727-6491 ● **CO:** (303) 777-8070 ● **CT:** (203) 226-4281 ● **DE:** (609) 779-0200 ● **FL:** (800) 432-4480 ● **GA:** (800) 327-6600 ● **HI:** (808) 523-8881 ● **IA:** (402) 895-5850 ● **ID:** (801) 466-6522 ● **IL:** (312) 255-4820 ● **IN:** (317) 846-2591 ● **KS:** (816) 252-3700 ● **KY:** (317) 846-2591 ● **LA:** (800) 327-6600 **MA:** (617) 235-5520 ● **MD:** (703) 241-7803 ● **ME:** (617) 235-5520 ● **MI:** (313) 588-2300 ● **MN:** (612) 425-4455 ● **MO:** Independence (816) 252-3700/St. Louis (314) 721-0401 **MS:** (800) 327-6600 ● **MT:** (801) 466-6522 ● **NC:** (800) 327-6600 ● **ND:** (612) 425-4455 ● **NE:** (402) 895-5850 ● **NH:** (617) 235-5520 ● **NJ:** North (212) 687-2455 South (609) 779-0200 ● **NM:** Albuquerque (505) 292-1212/Las Cruces (505) 524-9693 ● **NV:** (714) 635-7600 ● **NY:** East Aurora (716) 655-4322/Loudenville (518) 459-5891 New York City (212) 687-2455/Rochester (716) 442-5631 ● **OH:** Cleveland (216) 267-0445/Dayton (513) 434-7500 ● **OK:** (214) 620-1551 ● **OR:** (503) 224-3145 ● **PA:** East (609) 779-0200/West (412) 892-2953 ● **RI:** (203) 226-4281 ● **SC:** (800) 327-6600 ● **SD:** (612) 425-4425 ● **TN:** (800) 327-6600 ● **TX:** Dallas (214) 620-1551/Houston (713) 862-6685 ● **UT:** (801) 466-6522 ● **VA:** (703) 241-7803 ● **VT:** (617) 235-5520 ● **WA:** (206) 364-8830 ● **WI:** (414) 784-9379 ● **WV:** East (301) 261-4344/West (412) 892-2953 ● **WY:** (303) 777-8070 ● **Washington, DC:** (703) 241-7803 ● **Guam:** (671) 646-7280 ● **Puerto Rico:** (809) 723-9689

CIRCLE 34 ON INQUIRY CARD



Digital's new 16-bit Falcon. Fierce competition for 8-bit SBC's.

You don't have to sacrifice size or affordability anymore to step up to 16-bit performance for your ROM-based application. Because now you can buy Digital's new ultra-small 16-bit Falcon for just $521.*

Never has so much microcomputer been packaged in so little space. At just 8.5" x 5.2", Falcon is by far the smallest 16-bit SBC on the market—smaller, even, than most 8-bit SBC's.

Yet astonishingly, the tiny Falcon is a full-power LSI-11, executing the same proven PDP-11 instruction set that has made our micros the world sales leader.

On one board, the SBC-11/21 Falcon packs 4Kb RAM, sockets for up to 32Kb PROM or additional RAM, 2 serial I/O lines, 24 lines of parallel I/O, and 50, 60 or 800 Hz Line Time Clock. And Falcon's LSI-11 Bus Interface lets you use other I/O interfaces from Digital's large family of I/O modules.

However you measure performance—power, functionality or size—Falcon is fierce competition for 8-bit SBC's.

For complete details, fill out the coupon or contact the Hamilton/Avnet, Harvey Electronics, Pioneer/Standard, Pioneer/Washington or Wyle distributor near you.

Or simply call toll-free (800) 225-9222 and ask us to send Falcon Information Package #0-190. In MA, HI, AK and Canada call (617) 568-5707.

*In quantities of 100. Single unit price is $790. Domestic U.S. prices only.

Please rush your Falcon Application Information Package to me at once. My application is:

☐ Laboratory/Scientific
☐ Data Communications
☐ Industrial Controls (please specify)_____

_____

☐ Other (please specify)_____

Name_____

Title_____

Company_____

Street_____

City_____

State_____ Zip_____ Tel. (____) _____

Digital Equipment Corporation
Microcomputer Products Group, HL2-2/E10,
77 Reed Rd., Hudson, MA 01749.

0-12-1
Dec-C-190

digital

We change the way people work.

CIRCLE 35 ON INQUIRY CARD

ongoing activities for highly efficient use of system resources.

Communications products for the system include X.25 based XODIAC™ network management software, IBM SNA compatible DG/SNA software, RJE80 (2780/3780), HASP II, and RCX70 (3270). The system, coupled with DG/SNA operates as an IBM 3274 and 3276 terminal in an SNA network. Both can operate concurrently in the system.

Application development programming languages include ANSI '74 COBOL, RPG II, ANSI BASIC, APL, FORTRAN 5, ANS FORTRAN 77, PL/I, DG/L™ and Macro Assembler. Data management software includes INFOS® II file management software, CODASYL based DG/DBMS; INFOS II and DG/DBMS also incorporate query capabilities designed to help nonprogrammers. TPMS transaction processing management software and interactive data entry/access (IDEA) software are also available.

A small system configuration consisting of CPU with 1M-byte main memory, 1600-bit/in tape drive, 73M-byte disc subsystem, system display console, 16 display terminals, asynchronous controller, 300-line/min printer, and AOS/VS software lists for $172,000. A large configuration with 2M-byte memory, 800/1600-bit/in tape drive, two 147M-byte discs, 40 terminals, 3 asynchronous controllers, 600-line/min printer, and AOS/VS sells for $293,200. **Data General Corp, Information Systems Div**, 4400 Computer Dr, Westboro, MA 01580.

Circle 247 on Inquiry Card

Medium scale computers shrink through use of CML circuits

Medium scale DPS 7 systems use the same architecture, interface concepts, and operating systems as the Level 64/DPS, but have twice their performance. This power, in a package one-third the size, is attained through use of micropackaged current mode logic circuits in both central processor and I/O processors.

High density current mode logic (CML) reduces power dissipation and electrical consumption and lowers propagation time per gate. A CML gate has only two transistors while ECL requires four; this difference alone cuts the required power in half. In addition, since CML operates on a 3.3-V supply voltage rather than ECL's 5.2 V, required power is cut by another one-third. CML circuits, when mounted in a micropackage, require less additional power for lines offchip (ie, signal transfer to other chips) than do ECL. Because CML requires less power than ECL, transistor density can be increased since heating is reduced. Lower power consumption also allows chips to be more closely spaced, reducing signal delay and improving overall circuit speed.

Micropackaging reduces the length of electrical connections between circuit chips and the substrate, and between the chips themselves. With micropackaging 60 to 100 chips can be mounted on a single substrate in close proximity; so power needed to drive the signal among the chips is hardly greater then power needed to operate the chips themselves. In the DPS 7, each substrate is 5-cm square and 1-mm thick, and can receive 36 chips. Nine substrates mount on a PCB supplying up to 15,000 logic functions—7 times that of Level 64 boards. CML and micropackaging used together provide a speed of 1-ns/gate delay and use about 3 mW of power/gate.

Central system of the DPS 7 is divided into three types of processors—central, peripheral, and network—each with arithmetic/logic unit, read/write memory, and ROM. Executed by central or peripheral processors, firmware based microprograms provide basic machine functions or support software. Among the functions performed are virtual memory management, error correction, program synchronization, task management, and execution of diagnostics.

A second level of decentralization occurs in the CPU itself. Seven subunits within the CPU communicate with one another over a high speed bus. These subunits independently execute microinstructions from ROM, with up to five units operating simultaneously.

Peripheral processors include mass storage, magnetic tape, and unit record processors. All are microprogrammed and include ROM, RAM, and ALU, thereby offloading the CPU of all device handling responsibilities, including error detection and correction.

DATANET 8 frontend network processors offload the central processor of line, protocol, terminal, network handling, and administration. Attached to the central system via a standard 1.25M-byte/s I/O channel, the processor transfers data to and from its host and serves for communication across private and public networks under Distributed Systems Architecture (DSA).

Decentralization permits peripheral and network processors to work simultaneously with the central processor. Each processor attaches to the CPU via a dedicated high speed (1.25M-byte/s) multiplexer channel, resulting in data transfer to and from the central main memory at up to 10M bytes/s. This leaves the central processor free to execute system and user programs and, more important, control access to the system by multiple local and remote end users.

The GCOS 64 operating system supports batch, transaction, and distributed processing, and interactive timesharing, all within an integrated environment. Operating system features COBOL, FORTRAN, RPG, BASIC, and query language processors; TDS/64, a high performance transaction processing system; and I-D-S-II, a CODASYL compatible database management system.

Program and data segments are protected on several levels. Data segments, for example, have protection bits that prevent execution as instructions; code segments are protected similarly against write modification. Attempts to access a location outside a program's address space result in an exception report and halt. Ring protection in a 4-class hierarchy provides a 4-level system of privilege. Each procedure or code segment in the system has a minimum and maximum execute ring number assigned to specify who may call the procedure.

System family consists of four models. An entry level 7/35 with 1M-byte memory, 600M-byte mass storage, 900-line/min printer, and 4 synchronous lines sells for $279,877. The 7/45 supports up to 143 communications lines, and can have 4M bytes of memory, 10G bytes of mass storage, 8 tape drives, and 5 unit record devices. Model 7/55 offers 4M bytes of memory, 15G-byte mass storage, 16 tape drives, 10 unit record devices, and 143 communications lines. The top of the line DPS 7/65 supports 4M bytes of memory, 20.8G-byte mass storage, 16 tape drives, 10 unit record devices, and 271 lines. Configured with 3M-byte memory, 4.2G-byte disc storage, two 900-line/min printers, 8 tapes, 500-card/min reader, and DATANET 8 frontend processor with 16 lines, this unit sells for $920,382. **Honeywell Inc**, 200 Smith St, Waltham, MA 02154.

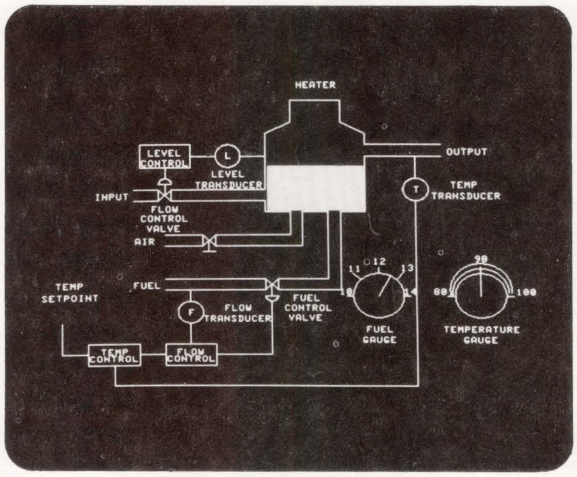
Circle 248 on Inquiry Card

There's already $50 million in software behind the HP 1000 L-Series microsystem.

What we just added makes it look even better.

Low-cost, high-performance graphics.

At only $10,800, Hewlett-Packard's Model 5 microsystem now includes an integrated HP 2623 graphics terminal (with built-in graphics printer) and our powerful Graphics/1000-II software. So you can picture your more demanding applications without the expense of add-on graphics.



Easy does it.

Graphics/1000-II uses straightforward, high-level graphics commands that let you concentrate on getting to the solution—without writing time-consuming subroutines. And, the device-independent software allows you to develop your applications without worrying about which peripherals will be used. This reduces development time *and* maintenance costs.

Big software. Small package.

The Model 5 is built around our popular two-board, ½ megabyte L-Series microcomputer. But don't let the system's small size fool you. You get a powerful, real-time, multiprogramming, multi-user operating system. And you can choose from among any of four languages for developing your programs—Assembly, Pascal, FORTRAN 4x or BASIC. There's also our advanced HP DSN networking software and our award-winning IMAGE data base management system. All of these packages are upwardly compatible throughout the entire HP 1000 line.

Matching the system to the job.

The L-Series graphics microsystem is completely modular, so you can configure a system that precisely matches your applications. Hard discs and other peripherals (including a wide range of graphics devices) can be plugged in directly. And if there's ever a problem, you won't have to worry about multiple vendors. The entire system is backed by HP's full range of customer services, provided from 170 offices around the world.

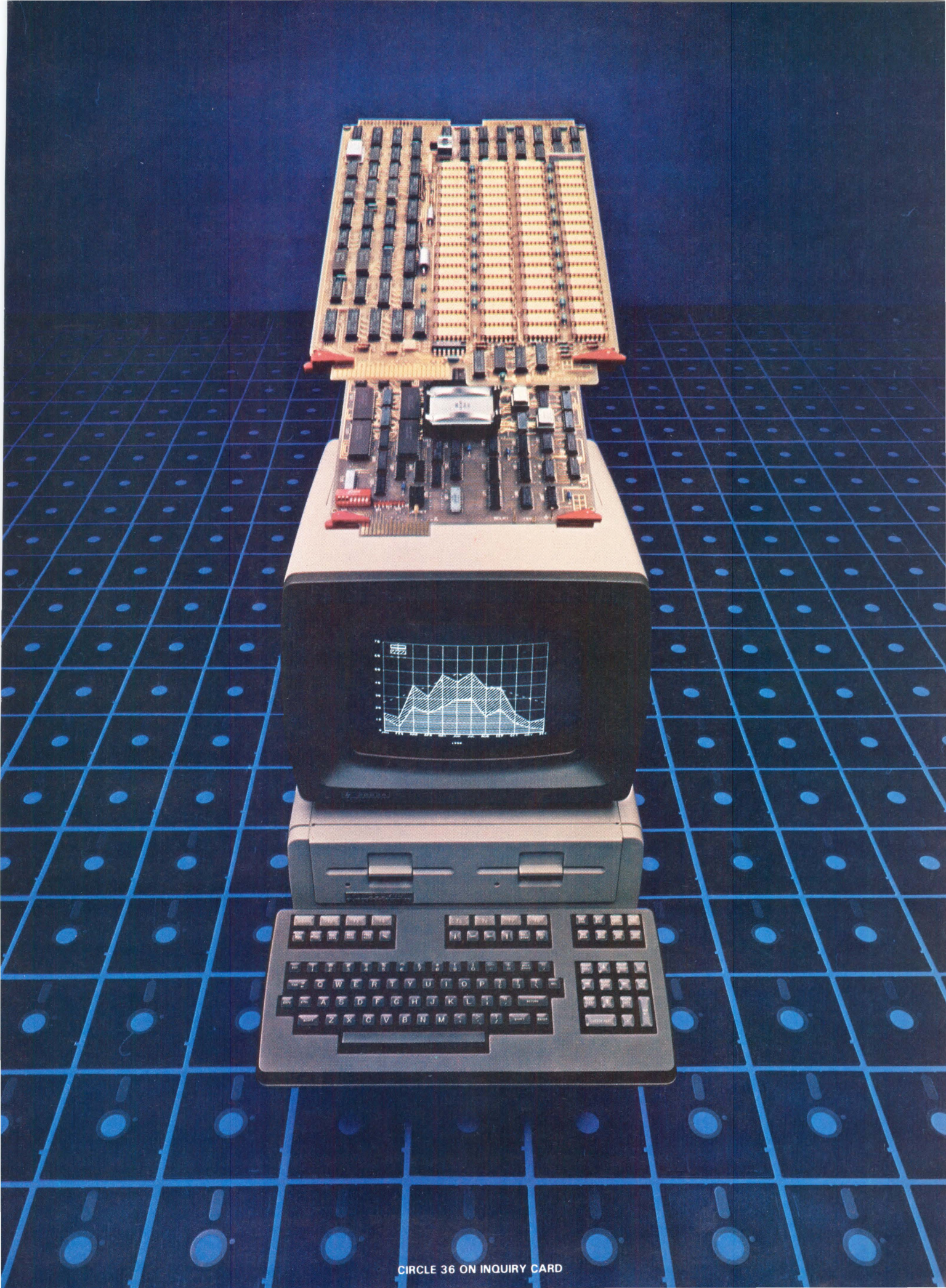
To get the complete picture on this new graphics microsystem, contact your local HP sales office listed in the White Pages. We'll be glad to arrange a hands-on demonstration. Or, write for more information to Hewlett-Packard, Attn: Joe Schoendorf, Dept. 12117, 11000 Wolfe Rd., Cupertino, CA 95014.

When performance must be measured by results.

HEWLETT PACKARD

Prices U.S.A. list, OEM quantities of 100.

22105
HPDS160



CIRCLE 36 ON INQUIRY CARD

OUR MEDIA IS OUR MESSAGE.

Over the past seven years we've earned a name for ourselves by making the best magnetic media in the business. Precision magnetic media — Diskettes, Mini Diskettes, Diagnostic Diskettes, Rigid Discs, Disc Packs, and Disc Cartridges — all certified to be 100% error free both on-track **and** between the tracks.

Now we're making it easier for you to buy the best. Just dial Dysan direct TOLL FREE at 800/538-8150 or 408/988-3472 (in California) or contact your local Dysan office.

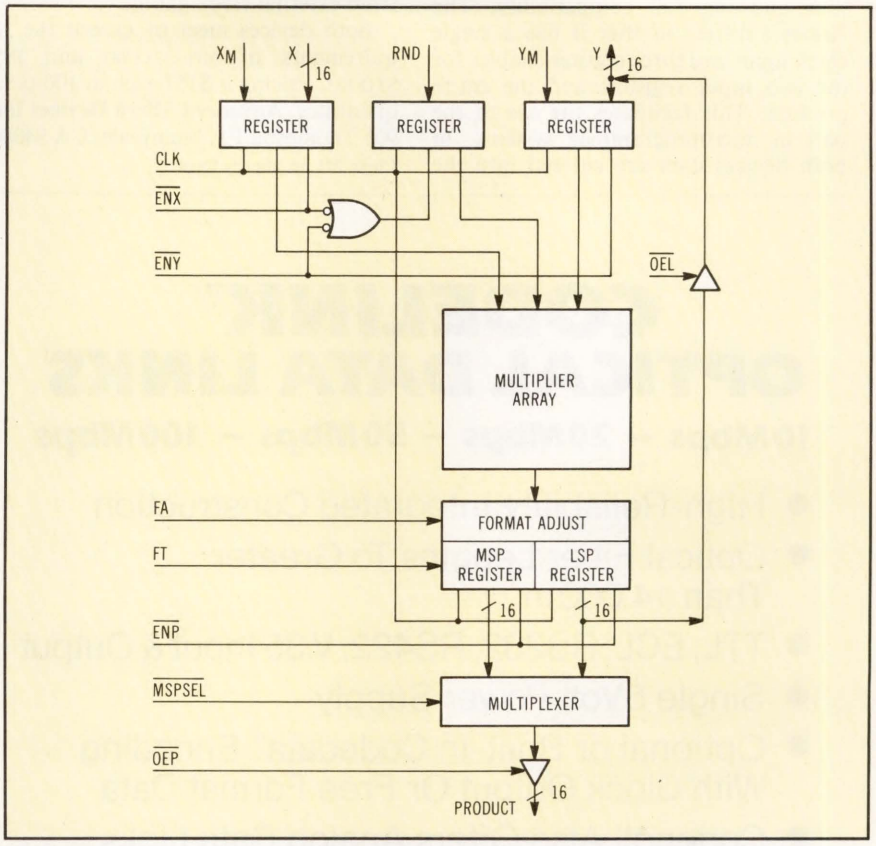
Precision magnetic media from Dysan.

Our media says it all.

dysan Dysan® CORPORATION
5440 Patrick Henry Drive
Santa Clara, CA 95050
408/988-3472
TLX: 171551 DYSAN SNTA

CIRCLE 37 ON INQUIRY CARD

Bipolar 16-bit parallel multipliers produce 32-bit product in 80 ns



Single clock input (CLK) and three register enables (ENX, ENY, and ENP) for two input registers and entire product facilitate use of Advanced Micro Devices' 16 x 16-bit parallel multiplier Am29517 in microprogrammed systems

First components in the Am29500 digital signal processing family of circuits, Am29516 and Am29517 are 16-bit parallel multipliers that use an unclocked combinatorial array to produce a 32-bit product in no more than 80 ns over the full military temperature range. The 64-pin devices provide a 40-ns typical multiply time.

A plug-in replacement for TRW's MPY16HJ, the Am29516 is fabricated using the IMOX™ (oxide isolated) process, and is 2.5 times as fast as the part it replaces. The Am29517, a proprietary device, is optimized for microprogrammed system applications. Both devices feature internal ECL circuitry for high speed. In addition, they have TTL compatible I/O ports for interface flexibility and require only a single 5-V power source for operation.

The high speed parallel 16 x 16-bit multipliers provide 17-bit input registers for X and Y operands and their associated mode controls X_M and Y_M. These mode controls are used to specify the operands as 2's complement or unsigned numbers.

A format adjust control (FA) at the output of the multiplier array allows the user to select either a full 32-bit product or a left shifted 31-bit product suitable for 2's complement only. Two 16-bit output registers hold the most and least significant halves of the product (MSP and LSP) as defined by the format adjust control. For asynchronous output, these registers may be made transparent by taking the feedthrough control (FT) high. A round control (RND) allows the MSP to be rounded. This control is registered, and is entered whenever either input register is clocked.

The two halves of the product may be routed to a 16-bit 3-state output port via a multiplexer. This allows the user to obtain a full 32-bit product consisting of both least and most significant halves at a single output port. This is particularly advantageous for use in expansion schemes where a large multiplier array is being designed to handle long word-width multiplications. In addition, the LSP is connected to the Y input port through a separate 3-state buffer.

In the Am29516, the X, Y, MSP, and LSP registers have independent clocks. The output multiplexer control uses a

(continued on page 72)

pin which is a supply ground in the TRW MPY16HJ. When this control is low, the device functions like the TRW device, thus allowing full compatibility. The Am29517 differs in that it has a single clock input and three register enables for the two input registers and the entire product. This facilitates the use of the part in microprogrammed systems. In both devices data are entered into the registers on the positive edge of the clock. The single clock approach eliminates clock delay and skew, which result from external clock gating.

Both devices meet or exceed the requirements of MIL-STD-883 and INT-STD-123. Pricing is $157 each in 100-piece quantities. **Advanced Micro Devices Inc**, 901 Thompson P1, Sunnyvale, CA 94086.

Circle 271 on Inquiry Card

30-channel, 128-channel transmitters and receiver ICs designed for remote infrared applications

A 30-channel and 128-channel infrared transmitters and a companion receiver device from Texas Instruments Inc are designed for applications in which infrared light beam transmissions are used for remote control.

The 30-channel device, SN76881, generates and transmits an 8-bit code at 40.9 kHz carrier frequency. Operated from a simple matrix keyboard with up to 30 keys, the part transmits a minimum of two codes with each key press. Typical operating current for the device is 6 mA at 10 V. Other features include automatic power-up with debounce control, an open collector output stage capable of sinking up to 50 mA, and a standby mode that requires 5 mA (typ).

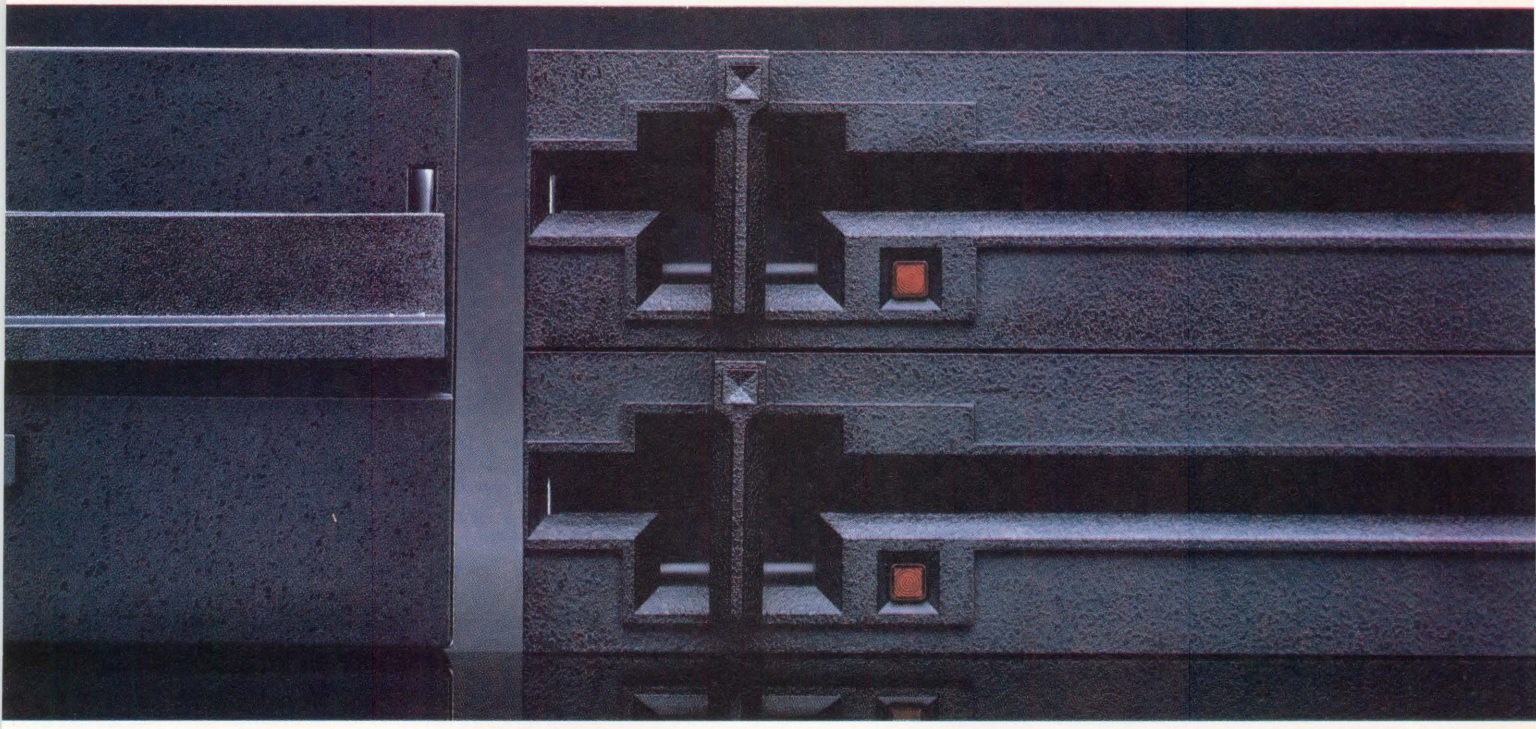
SN76882, the 128-channel transmitter, can operate as a 64-, 64 + 64-, or 32 + 32 + 32 + 32-channel device. A keyboard matrix of up to 8 x 8 keys can be accommodated. Other characteristics are the same as those of the SN76881.

Receiver/detector SN76832A replaces a number of standard ICs and other components required for the reception and processing of a modulated infrared light beam. An onchip transimpedance preamplifier, differential amplifier, and demodulator are included in the device. The combined voltage gain of the two amplifiers is over 80 dB, resulting in a 95-dB dynamic range for detecting nA infrared signals. A high-impedance input stage allows direct interface with an infrared detector, such as the TIL100. A gated-output stage, with an external-enable control, allows the receiver to share a data bus. It also has an open collector output that allows it to interface directly with microprocessors.

Since the SN76832A outputs data in the same binary format as the SN76881 and SN76882 transmitters, the microprocessor can decode data from the SN76832A without the need for external circuitry. **Texas Instruments Inc**, PO Box 202129, Dallas, TX 75220.

Circle 249 on Inquiry Card

Introducing 3.2 Mb capacity in a 1.6 Mb space.



Presenting the half-size 8" ThinLine™ Floppy that lets you double your capacity without increasing your cabinet size.

We're proud to announce the 8" floppy disk drive that brings unheard-of capacity to traditional single-drive systems—the TM-800.

Since it's exactly half the height and weight of a standard 8" floppy, you can stack two ThinLine floppys where one standard used to go. That doubles your capacity from 1.6Mb to 3.2 Mb without increasing cabinet size, weight, or power requirements. And the TM-800 is priced less than a standard floppy.

The TM-800 ThinLine family is built with quiet, efficient brushless DC motors which eliminate the need for voltage changes for overseas use (as required with AC motors in traditional 8" drives).

Our TM-848-1 reads and writes .8 Mb (double density, IBM unformatted) on one side of the disk. And our TM-848-2 provides 1.6 Mb (1.2 formatted) by using both sides of the disk.

Both models feature our proprietary high-resolution manganese-zinc read/write heads. They have 30%-40% higher performance than ferrite and minimize diskette wear. What's more, despite the fact that other manufacturers talk about bringing out products like the 8" ThinLine, Tandon is the only place to get one.

Because no one else has our capacity for turning the unheard-of into a reality.

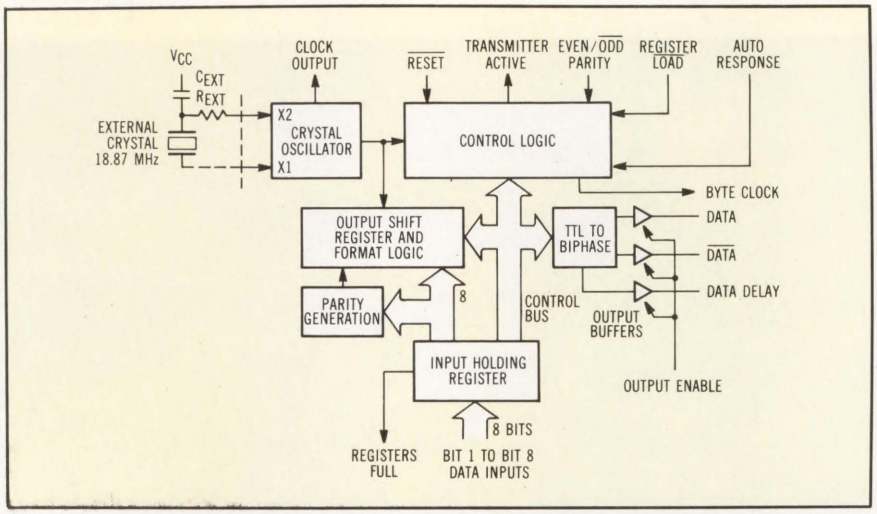
Tandon. 20320 Prairie, Chatsworth, CA 91311, (213) 993-6644. Regional Sales Offices: Wakefield, MA (617) 245-4482; Plano, TX (214) 423-6260; Addison, IL (312) 530-7401; Newport Beach, CA (714) 675-2928; Sunnyvale, CA (408) 745-6303; Frankfurt, West Germany (0611) 392081-85 TWX 411547.

CIRCLE 39 ON INQUIRY CARD

Tandon

The most successful disk drive company you never heard of.

Data transmission ICs provide 3.5M bit/s data rate



Block diagram of DP8342 transmitter/encoder. Transmitter/encoder contains crystal oscillator. Input is crystal with frequency eight times data rate. Clock output is provided to drive DP8343 receiver/decoder clock input and other system components at oscillator frequency. Oscillator drives control logic and output shift register/format logic blocks

Two recently released digital interface ICs provide a data bit rate of up to 3.5M bits/s with 8-bit data words. National Semiconductor Corp's DP8342, a transmitter/encoder, and DP8343, a receiver/decoder, can be used with coaxial, twisted pair, fiber optic, magnetic, infrared, rf, ultrasonic, and audio and current carrying media. The DP8342/43 2-chip set enables the use of high speed serial data buses rather than more costly parallel buses. In addition, the devices enhance data integrity and allow transmission over long lines, eg, 5000' (1524 m) of coaxial. A digital phase locked loop adjusts the receive window, promoting the recovery of data over variations in frequency.

DP8342 generates a 5-bit starting sequence, 3-bit code violation, followed by a sync bit and 8-bit data byte plus a parity bit. Termination of the transmission is signaled by a 3-bit ending code. Block diagram is shown in the Figure.

Recognizing biphase serial data sent from the transmitter chip, the DP8343 receiver converts them into eight bits of parallel data. Separation of transmitter and receiver allows the addition of receivers at one end of the line without adding more transmitters and also allows flexible data bus organization. **National Semiconductor Corp**, 2900 Semiconductor Dr, Santa Clara, CA 95051.

MICROPROCESSORS/ MICROCOMPUTERS

OEM microcomputer system integrates VLSI hardware and software standards

Among the many problems facing the OEM in an era of rapidly advancing VLSI technology and changing market requirements is how to handle system development and production in time for the optimum market opportunity. System components such as microcomputer boards, chassis, power supplies, peripherals, operating systems, languages, and utilities are commonly acquired from different vendors and integrated into a system or product. By the time this process is completed, the optimum market opportunity has often passed. Intel attempts to solve this problem with system 86/330, its first integrated OEM microcomputer system. It provides an accelerated route to the achievement of VLSI systems.

Aimed at the sophisticated technology OEM marketplace, the system uses industry standard boards, discs, and software. By adding an RS-232 compatible terminal, the user can begin to write applications software at once without using up significant setup, integration,

(continued on page 79)

THIS IS A 14" SCREEN

THIS IS 80 CHARACTERS PER LINE

THIS IS 132 CHARACTERS PER LINE

THIS IS DOUBLE WIDE

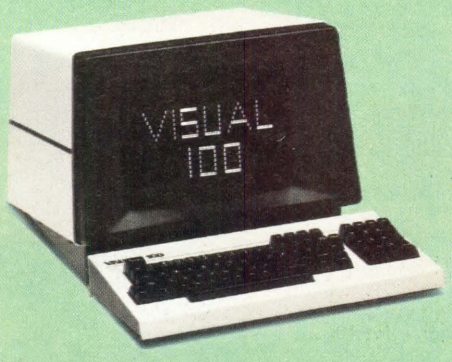
THIS IS DOUBLE HIGH DOUBLE WIDE

Actual character size.

The advantages of VISUAL'S 14" screen are easy to see.

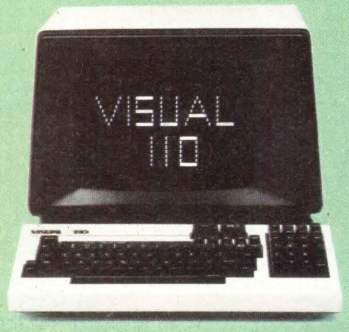
It's tough to read 132 columns of data on a 12" screen. And the terminals with 15" screens are terribly bulky and expensive. We have a better way. A 14" diagonal screen that displays 132 columns in big, crisp characters that measure a full 33% larger than on a 12" screen. And they're available in either green or white display.

So if you want a big screen in a compact terminal at an economical price, call or write us today.



VISUAL 100 – DEC VT100® Compatible Plus

- Non-glare, tiltable screen
- Detached solid state keyboard, n-key rollover
- CRT saver feature
- Serial buffered printer interface option



VISUAL 110 – Data General Dasher™ Compatible Plus

- 80 or 132 columns
- Smooth scrolling of data
- Double high, double wide characters
- Horizontal split screen
- Non-volatile RAM set-up mode

VISUAL 400 – Top of the line... All Capabilities of the Visual 100 Plus

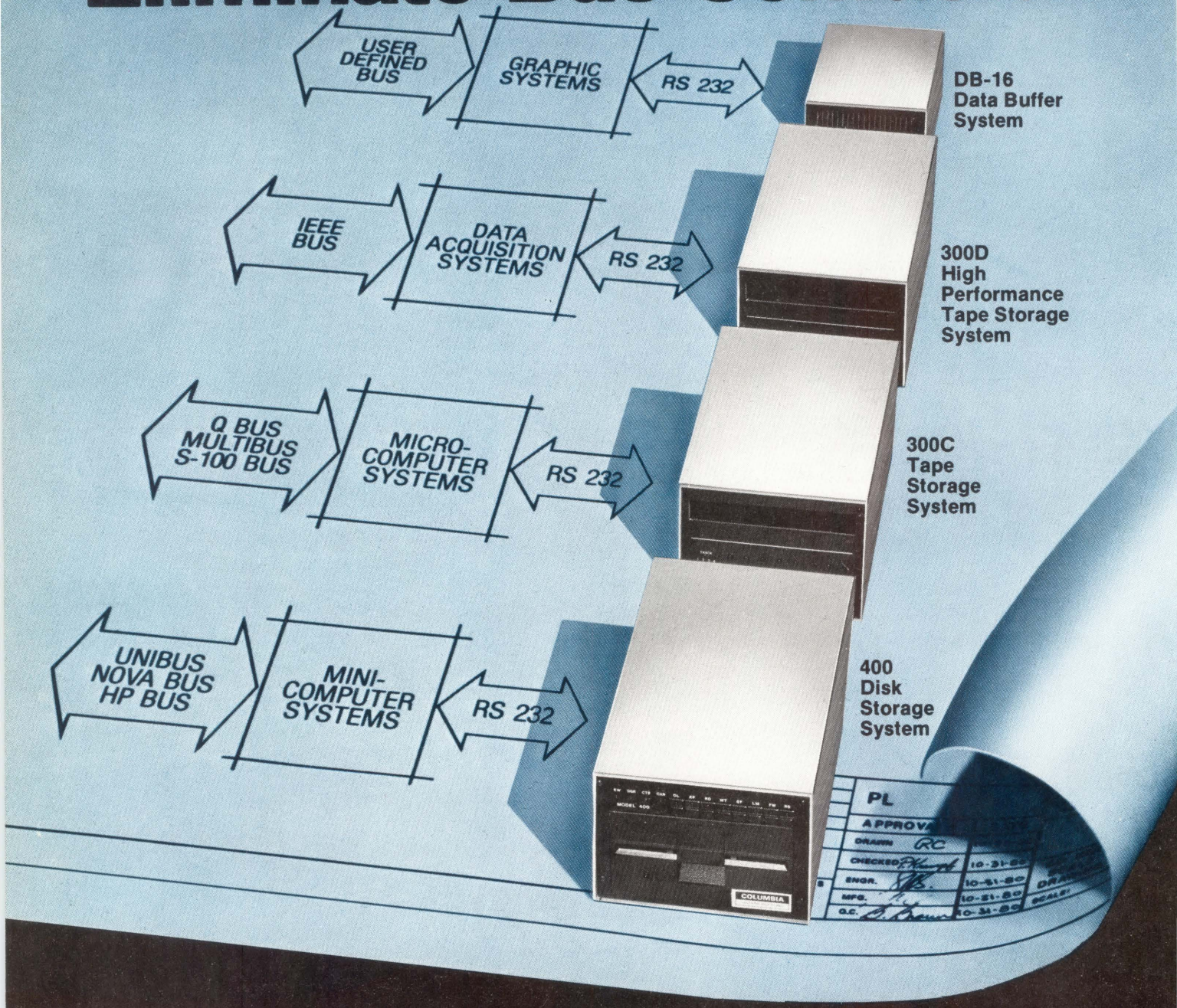
- Flexible block mode transmission parameters
- 2 or 4 optional pages of memory; flip page or scroll
- Programmable non-volatile function keys
- 8 resident national character sets & line drawing

VISUAL See for yourself

Visual Technology Incorporated
540 Main Street, Tewksbury, MA 01876
Telephone (617) 851-5000. Telex 951-539

CIRCLE 41 ON INQUIRY CARD

Our RS-232 Peripherals Eliminate Bus Confusion



Forget about compatibility with the Multibus, Q bus, S-100 bus, Unibus or the host of others. Most systems have an RS-232 data port. So select an RS-232 compatible peripheral from Columbia Data Products and leave the bus confusion to others.

System compatibility isn't all you get with CDP peripherals. You also get microprocessor intelligence in our floppy disk, cartridge tape or RAM based storage systems.

That intelligence gives you remote control and failsafe operation for data acquisition applications ...comprehensive editing for data entry, graphics and data processing applications...file management and telephone data logging for data communications applications.

And Columbia Data peripherals also deliver performance. Dual port data transfer rates can be up to 19.2K baud, with storage capacity of 5.15 Mbytes on tape, 180 Kbytes on disk and 32 Kbytes in RAM. The buffered input and output ports can be set at different baud rates to match system requirements and constraints...or achieve data rate conversions.

With intelligent tape and disk systems priced under $1400 and semi-conductor storage under $700 in OEM quantity, you get that compatibility and performance at the right price.

COLUMBIA
DATA PRODUCTS, INC.

Columbia Data Products, Inc.
8990 Route 108
Columbia, Maryland 21045
(301) 992-3400

CIRCLE 42 ON INQUIRY CARD

Our Commander Computer Now Works Three Times As Hard

Not only does Columbia Data Products' Commander Computer give you the largest I/O complement in the industry, we now give you multi-tasking capability to play with.

And by *multi-tasking*, we mean simultaneous execution of several software processes — like performing data entry operations while supporting on-line data communications...or developing software while batch printing...or running a business package while updating your data base...or performing concurrent peripheral operations in an industrial environment.

In fact, we could go even farther. By utilizing the Commander 964+ dual processor architecture, graphic terminal emulation software or even custom user modules, like "Space Commanders" depicted above, can be downloaded to the terminal system processor, while the host Z-80A — 128K processor system under the MP/M II operating system can support independent multi-user, multi-tasking operations.

Other standard features of the Commander 964+ include 512 x 256 graphics display, dual Z-80A processors, 128K RAM host system, 32K RAM terminal, four RS-232 ports, four parallel ports, RS-170 composite video, four channels of programmable counter/timer, 800K bytes disk storage, and CP/M® and MP/M® II operating systems. Optional features include APU, DMA, IEEE bus controller and expandable disk capacity.

Think about it...resource sharing at its best, from Columbia Data Products.

Contact us for more information.

COLUMBIA

DATA PRODUCTS, INC.

Home Office:
8990 Route 108
Columbia, MD 21045
Telephone 301-992-3400
TWX 710-862-1891

West Coast:
3901 MacArthur Blvd.
Suite 211
Newport Beach, CA 92663
Telephone 714-752-5245
Telex 692 310

Europe:
P.O. Box 1118
4050 Moenchengladbach 1
West Germany
Telephone 021-61-33159
Telex 852 452

® Trademark of Digital Research

CIRCLE 43 ON INQUIRY CARD

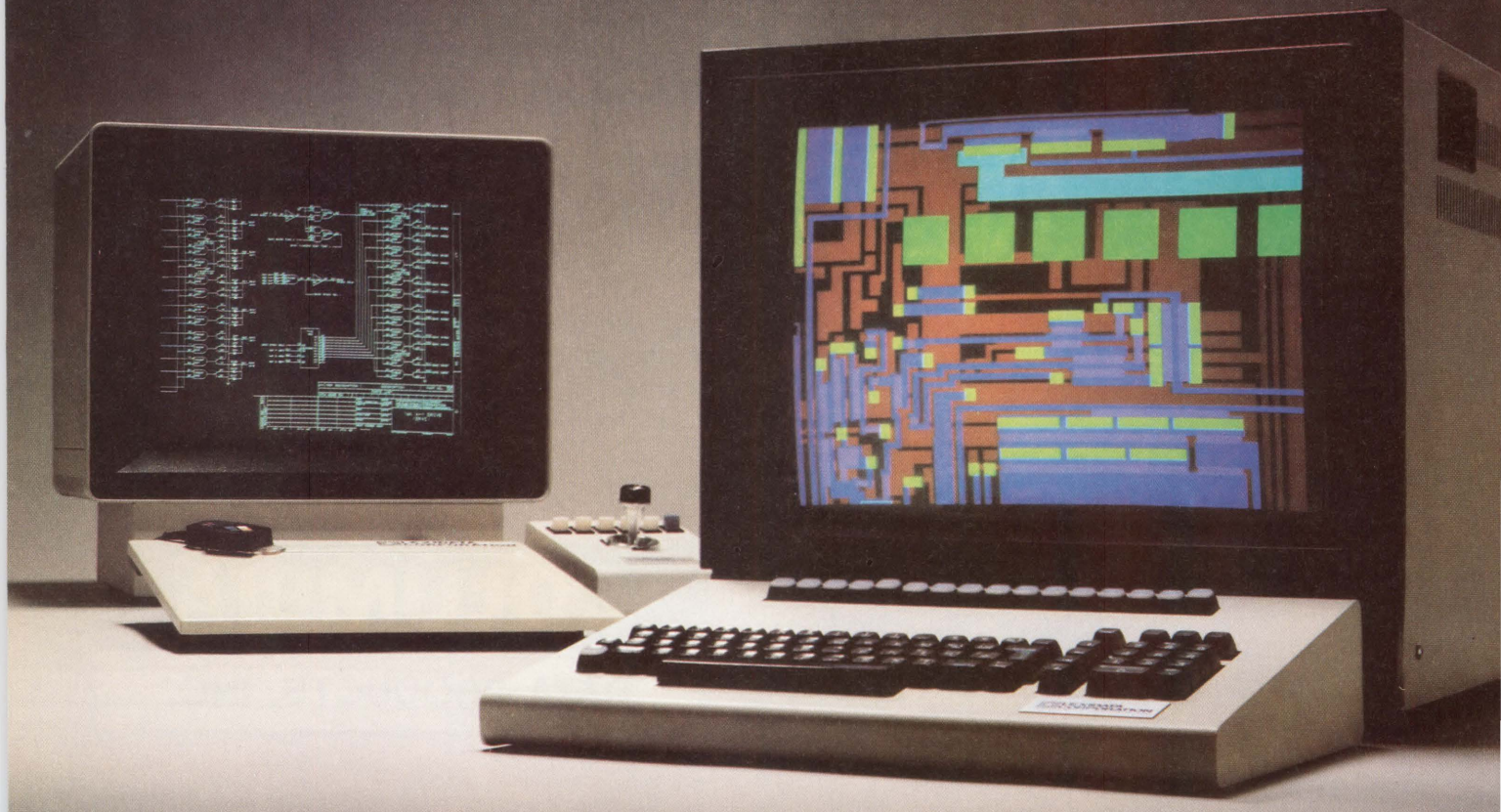
The Lexidata System 3400 Display Processor and full line of interactive peripheral devices are designed specifically for OEMs and sophisticated end-users. The System 3400, rapidly becoming the leader, with over 1,000 units shipped to date, possesses the product characteristics required by this demanding customer group.

- System 3400 *performance* is truly outstanding. Only the System 3400 offers 1280x1024 resolution at 60Hz non-interlaced black-and-white and grayscale capability, or 880x704 resolution at 60Hz non-interlaced color. Our programmable lookup tables are the industry standard of performance. Double buffered memories or multiple lookup tables with bank switchable memories and processor features, such as pan/zoom and 4K WCS, are available.
- System 3400 *quality* satisfies the requirements of Fortune 500 companies, the leading CAD/CAM systems vendors and military and government contractors. We continue to focus on quality because we believe that quality and cost effectiveness are closely related.
- System 3400 *flexibility* ensures a configuration to meet the exact requirements of each customer. The System 3400 offers a complete range of OEM configurations, starting from $7,540, including monitor.
- System 3400 *software* provides a high-level language user-interface to execute graphics and imaging functions. The powerful subroutine library streamlines application software development and facilitates user interaction.
- System 3400 *cost effectiveness* enables even price-sensitive OEMs to configure a highly competitive product. You will be able to maximize your value-added contribution and optimize your overall system performance.

For more details, call (617) 663-8550 or write to us at 755 Middlesex Turnpike, Billerica, MA 01865. TWX 710-347-1574.

LEXIDATA CORPORATION

LEXIDATA



RASTER DISPLAYS...
FOR THOSE WHO DEMAND PERFORMANCE.

CIRCLE 44 ON INQUIRY CARD

and testing time. A Centronics compatible printer can be added for hard copy. The system is said to offer three times the user memory, four times the numeric processing performance, and 50% more mass storage than a comparably priced minicomputer based system.

Based on the latest VLSI technology, system 86/330 contains a 16-bit iAPX 86/20 coprocessor set: the iSBC 86/12A and the IEEE floating point standard iSBC 337 for general purpose and numeric computation. It is the first system to incorporate VLSI 8087 and 8089 coprocessors.

An 8″ (20-cm) Winchester disc furnishes 35M-byte storage; access time is 50 ms, and data transfer rate is 6M bits/s. An 8″ 1M-byte double-sided/double-density floppy drive handles data/program storage, file transfer, and backup. It has 90-ms access time and data transfer rate of 0.25M bits/s. A 320k-byte high speed RAM is provided for execution of multiple jobs. Additional hardware includes an RS-232-C serial port, parallel printer port, intelligent 8089 based disc controllers, and two additional MULTIBUS system slots.

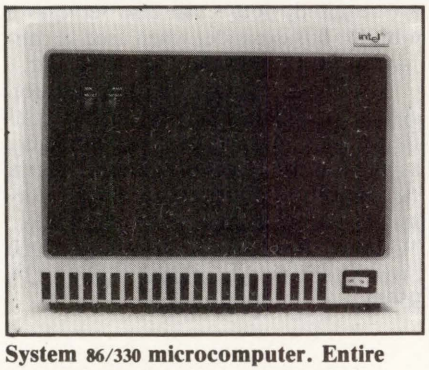
System software, designed with VLSI in mind, is built around the iRMX 86 realtime multitasking operating system. This system forms the basis for both the development system environment and the execution system that results. Operating languages include Pascal-86, FORTRAN-86, PL/M-86, and Assembler-86. The company's universal development interface (UDI) supports third party supplied industry standard languages including BASIC, COBOL, and C. This range of languages is available for program development and for access to a wide range of microapplication software.

System 86/330 used the proposed IEEE-796 MULTIBUS standard as its system architecture. It supports standards such as GPIB (IEEE-488) for instrumentation I/O, RS-232, -422, and -449 communications standards, Ethernet, and others. The MULTIBUS system bus multiprocessor architecture allows easy expansion of processing and intelligent I/O devices. If the system's iSBC 86/12A processor is nearing capacity, up to two more MULTIBUS based processor boards can be added for additional processing power. More than 50 MULTIBUS system boards are available for a broad range of expansion possibilities. Modular standard products permit flexible decomposition of the system to board-level products for custom configurations.

Priced for OEMs at $19,000 (U.S.) each in quantities of 10, the complete system package includes hardware, preconfigured and configurable iRMX software, and documentation. Initial deliveries are scheduled for January 1982. **Intel Corp,** 5200 NE Elam Young Pkwy, Hillsboro, OR 97123.

—Jim Hughes, Senior Editor

Circle 250 on Inquiry Card



System 86/330 microcomputer. Entire system including disc peripherals is contained in single 21 x 16 x 12″ (53 x 41 x 30-cm) cabinet that can be desktop or rackmounted. Package meets UL, FCC, VDE, and CSA safety and emi/rfi specifications

Designed as programming aid piggyback 8-bit microcomputer accepts EPROMS

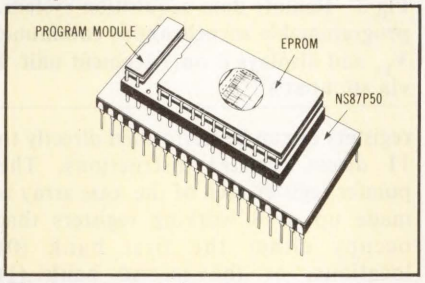


Fig 1 NS87P50 microcomputer piggyback package. Microcomputer contains EPROM socket, program module interface, system timing, control logic, RAM, and 27 I/O lines

An 8-bit microcomputer, designated NS87P50, has been developed as a programming aid for 8048, 8049, and 8050 CPUs. The device is housed in a 40-pin DIP with a plug-in adapter that accepts a 24-pin 2758A, 2716, or 2732 EPROM. A program module, when installed, is used to select the INS8048 or 8049; when the program module is not installed, the INS8050 is automatically selected. The piggyback structure is shown in Fig 1.

Designed to overcome the limitations of single-chip microcomputers with onboard EPROM, the part also emulates large program memory designs—other EPROM based designs seldom exceed 1k byte of ROM. Also, in most devices an EPROM part cannot be operated simultaneously with the ROM based part. Other designs can require 2k to 4k of ROM (program memory) and more than the 64 bytes of RAM (data memory) available on EPROM versions. NS87P50, on the other hand, provides up to 4k bytes of ROM and 256 bytes of RAM. The program memory consists of 1024, 2048, or 4096 8-bit bytes of P/ROM.

Resident RAM data memory is arranged by the program module (Fig 2). RAM addressing is implemented indirectly via either of two 8-bit RAM pointer

(continued on page 80)

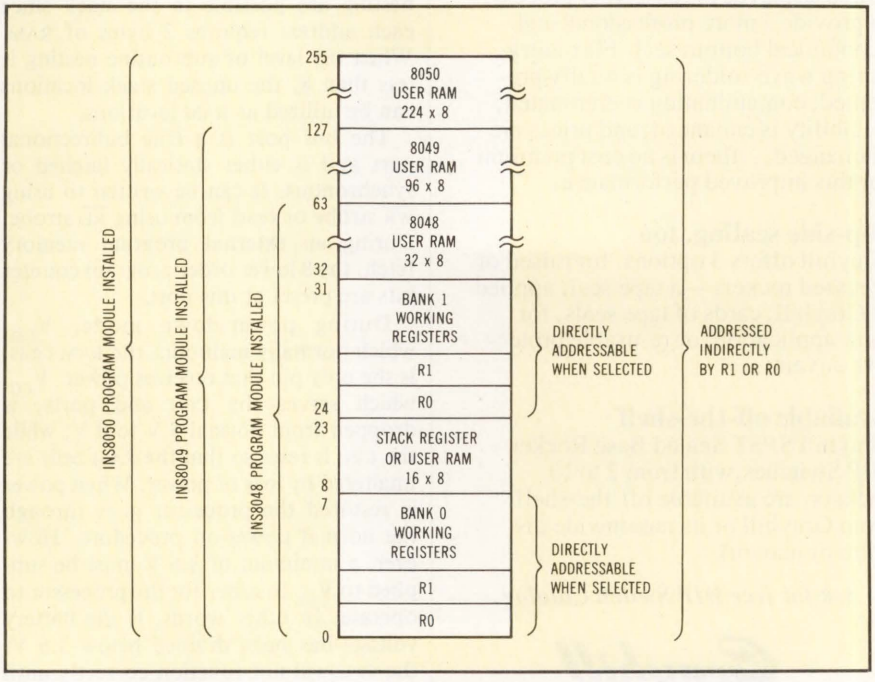


Fig 2 RAM data memory. RAM capacity depends on processor type. RAM addressing is indirectly implemented with R0 and R1 pointer registers. Pointer registers are first two RAM locations

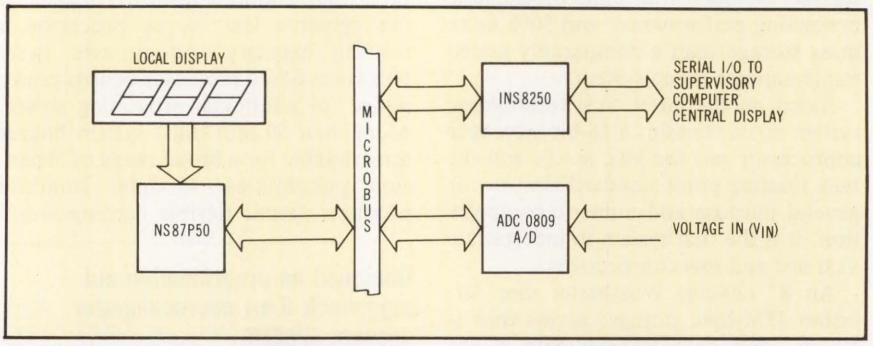


Fig 3 Remote data acquisition system. INS87P50 application with INS8250 programmable asynchronous communication system. CMOS ADC receives data at V_{IN} and displays it on 7-segment unit. Data are transferred from ADC to INS8049 via MICROBUS™

registers or can be performed directly to 11 direct register instructions. The pointer register area of the RAM array is made up of 8 working registers that occupy either the first bank (0) locations, or the second bank (1) locations. The second bank of working registers is selected by using the register bank switch instruction. If this bank is not used for working registers, it can be employed as user RAM.

An 8-level stack after bank 0 occupies RAM address locations 8 to 23, which are addressed indirectly through R0, R1, or the 3-bit stack pointer. The stack pointer keeps track of the return address and pushes each return address down into the stack. Eight levels of subroutine nesting are possible in the stack since each address requires 2 bytes of RAM. When the level of subroutine nesting is less than 8, the unused stack locations can be utilized as RAM locations.

The bus port is a true bidirectional port and is either statically latched or synchronous. It can be written to using $\overline{WR}$ strobe or read from using $\overline{RD}$ strobe. During an external program memory fetch, the 8 lower order program counter bits are preset at this port.

During power-down mode, V_{DD}, which normally maintains the RAM cells, is the only pin that receives power. V_{CC}, which serves the CPU and ports, is dropped from normal 5 V to 0 V, while the CPU is reset so that the RAM cells are unaltered by loss of power. When power is restored the processor goes through the normal power-on procedure. However, a minimum of 3.6 V must be supplied to V_{DD} in order for the processor to operate. In other words, if the battery voltage has been drained below 3.6 V, the CPU will not function correctly until the battery is recharged.

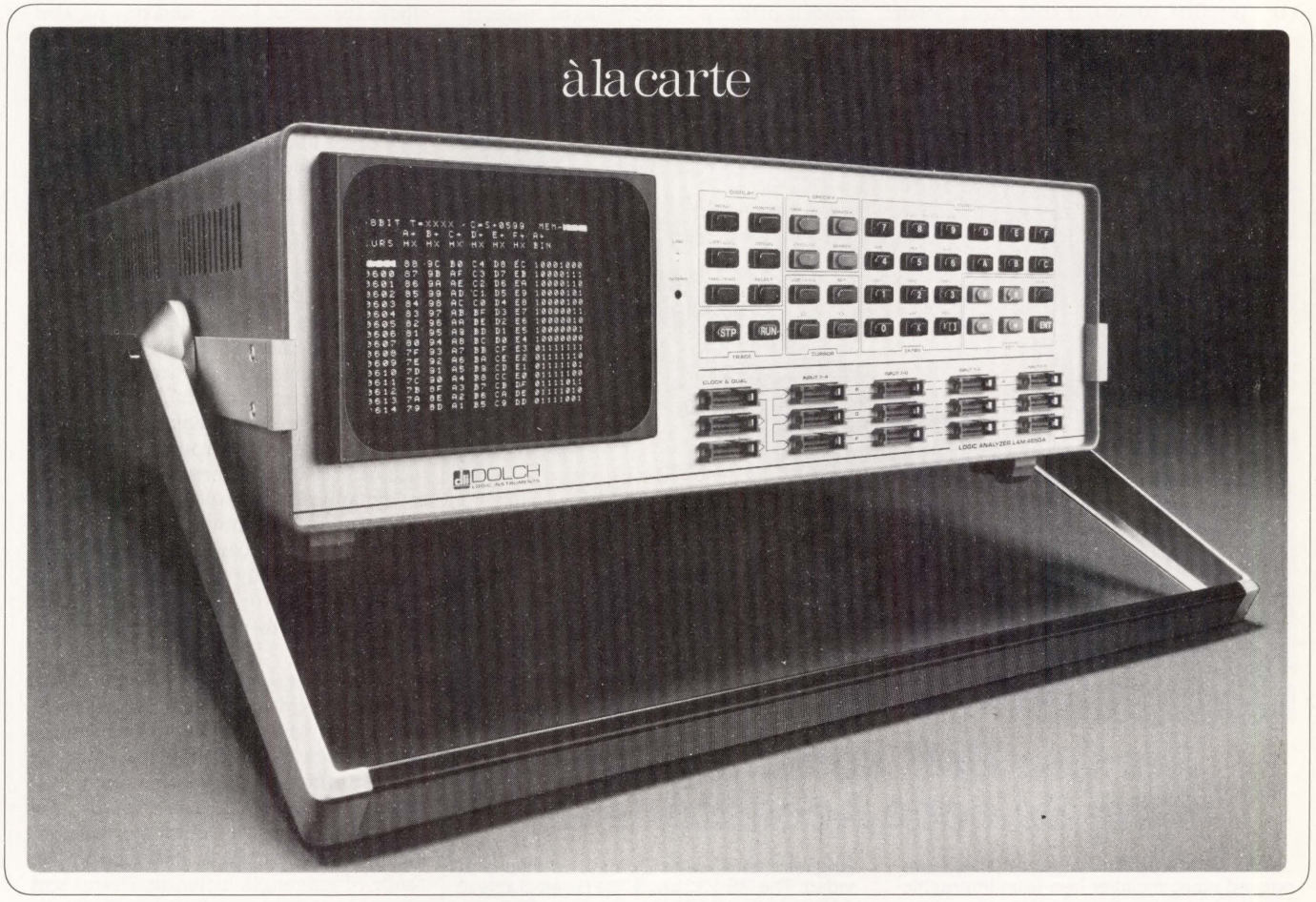
Program memory (P/ROM) can contain program instructions, program data, or P/ROM addressing data. Using standard UV erasable P/ROMs to emulate a future single-chip system makes program development straightforward. P/ROM addressing, up to a maximum of 4k, is accomplished by a 12-bit program counter (PC). When emulating the INS8048 and INS8049, the NS87P50 will automatically address external memory when the boundary of their internal memories, 1k and 2k respectively, is surpassed. The binary value of the address selects one of the 8-bit bytes contained in P/ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential binary count value.

Twenty-seven I/O lines are organized as three 8-bit ports plus three test inputs. The three ports can be used as inputs, outputs, or bidirectional ports. Ports 1 and 2 differ from port 3 (bus port) in that they are quasi-bidirectional. Ports 1 and 2 can be used as input and output while being statically latched. If more I/O lines are required, port 2 can also serve as a 4-bit I/O bus expander when used in conjunction with the INS8243 I/O expander.

A typical remote data acquisition system is shown in Fig 3. In this configuration, an INS8250 programmable asynchronous communication system can receive commands or update information from a supervisory computer. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Dolch.

advanced logic analysis



48 to 96 Channels, 300 MHz, plus Mnemonics

Order up your parameters. Dolch's LAM 4850A logic analyzer makes it easy with a new key — Monitor. Monitor gives you status information and comments on menu setups, and can be called up at any time to interpret each parameter, its range, and its interaction with the current setup. And, you can store your setups for three months without power, eliminating the need to reprogram.

Zero in fast. The LAM 4850A disassembles your code into Mnemonics and gives you the channels you need to trace data, address, port and control lines. And for future needs, you can expand to 64, or even 96, channels.

Hook up fast, too. Dolch personality probes clip right over your CPU chips so you don't waste time connecting dozens of individual hooks. And the probe takes care of clock, timing and signal interfacing — no need to worry about signal conditions.

300 MHz sampling across 16 channels. A revolutionary option gives you the ultimate in sampling resolution — 3.3 ns — to help you solve the toughest timing and phase related problems. A unique memory overlay configuration provides simultaneous dual asynchronous recording across 16 channels without compromising any of the LAM 4850A features.

Don't settle for less than Dolch. The basic LAM 4850A is truly a universal logic analyzer system with 50 MHz sampling rate, 1000 bits per channel source and reference memories, and sophisticated sequential trigger and multilevel clocking.

For details on the Dolch LAM 4850A, or any of our other troubleshooting tools, write: Dolch Logic Instruments, Inc., 230 Devcon Drive, San Jose, CA 95112. Or call toll free: (800) 538-7506; in California call (408) 998-5730.

DOLCH
LOGIC INSTRUMENTS

Circle 46 for Demonstration

Circle 139 for More Information

68000 based microcomputer runs UNIX compatible operating system

The Universe 68, billed as a 32-bit "supermicro," is built around the Motorola 68000 microprocessor and runs UNOS, a UNIX compatible operating system. According to Charles River Data Systems' president, Richard Shapiro, it is "the first computer that gives system designers the functionality and flexibility of 32-bit architecture and the economy inherent in microprocessor technology." It "leapfrogs the 16-bit minicomputers, which are still stuck with the addressing limitations of their architecture."

The 32-bit architecture of the multi-user, multiprocessing system provides a 16M-byte addressing capability. Initial models offer up to 6M bytes of memory and support for as many as 34 users. The UNOS operating system takes advantage of the ease of use and file management functions that make UNIX effective as a program development system, while providing additional features.

Based on the Motorola 68000 microprocessor, the central processor contains memory management unit, system clock, two serial ports, and one parallel port. The processor has 32-bit data and address registers, and its logical and arithmetic operators manipulate 32-bit values. It uses a 24-bit program counter. Memory is made up of 128k-byte boards to a total 6M-byte maximum storage capacity (16M-byte maximum addressing capability). It is packaged in a 7-slot 7″ (18-cm) high or 15-slot 12″ (30-cm) high rackmountable or desktop unit. A 30-A power supply is provided in the 7-slot chassis; 80-A in the 15-slot unit. Disc subsystems include an 8M-byte 8″ (20-cm) Winchester with floppy disc and an 80M-byte cartridge (65M-byte fixed/15M-byte removable) drive.

UNIX features incorporated in UNOS include file management facilities such as dynamically grown files, device independence, and mountable files. Ease of use features include hierarchical file structures, I/O redirection, and pipes; a simple method for allowing the output of one process to be the input for a second process.

Among the extensions to UNIX that have been built into UNOS are an event count scheme for process synchronization, which is essential for realtime transaction-oriented applications. Interactive debugging, a screen editor, and support for extensive database management are also provided. UNOS supports a range of languages including Pascal and BASIC, as well as FORTRAN and C. While UNOS is not a Bell licensed version of UNIX, applications that run under UNIX will also run under UNOS, usually requiring only a simple recompilation.

The Universe 68/10 system, including two serial ports and one parallel port, 256k bytes of main memory, 8M-byte Winchester disc, and floppy disc backup, is priced at $18,500 in single units. The larger 68/80, with greater expansion capacity and an 80M-byte cartridge disc, sells for $38,500. Base price for a single UNOS operating system license is $3000. A board set configuration, including central processor, basic interface, and 256k bytes of memory sells for $6850. OEM discounts of up to 35% on hardware and as much as 98% on software are available. **Charles River Data Systems, Inc,** 4 Tech Circle, Natick, MA 01760.

Circle 251 on Inquiry Card

Dear Ma:
For remote user or central computer site, Racal-Vadic offers the broadest line of low and medium speed modems.

PACKAGING

Near Right: Low profile, low cost, low heat "50" series. Includes displays, diagnostics and voice/data switch.

Far Right: VA1616 Multiple Data Set. 16 channel chassis houses up to 16 intermixed modems and automatic dialers in 7-inch high chassis. Includes displays, diagnostics and redundant power supplies.

MODEMS FOR THE REMOTE TERMINAL USER

"50" Series

MODEMS FOR THE CENTRAL COMPUTER SITE

VA1616

300 bps Full Duplex Bell 103/113 Compatible

VA103 — World's first voice/data phone with modem circuitry built inside standard rotary or tone telephone. Direct connect.

VA355 — Direct connect originate/answer 300 bps FDX modem. Switched network and 2-wire leased line in single package. **Replaces** Bell 103A2/F/J, 108, 113A/B/C.

VA315 — Direct connect auto originate/answer 300 bps FDX modem. Operates with Racal-Vadic VA811 Singleline/Multiline Automatic Calling Unit. **Replaces** Bell 103A/E/J and 113A/B/C/D.

VA317 — Direct connect answer only 300 bps FDX switched network/2-wire leased line modem. **Replaces** Bell 113B/D.

1200 bps Half Duplex Bell 202 Compatible

VA1250/55 — Direct connect switched network 1200 bps half duplex modem (with or without reverse channel). **Replaces** Bell 202C/E/S. Leased line models available to replace Bell 202D/T.

VA1230/40 — 2/4-wire leased line 1200 bps half duplex (with or without reverse channel). **Replaces** Bell 202D/T. VA1230 is 1800 bps version.

VA1244/45 — Direct connect switched network 1200 bps half duplex (with or without reverse channel). Operates with Racal-Vadic VA811 Singleline/Multiline Automatic Calling Unit. **Replaces** Bell 202C/S.

1200 bps Full Duplex Bell 212A/103 and Racal-Vadic VA3400 Compatible

VA3413/12 — Full duplex dual acoustic coupler (VA3413). Operates at 1200 and 0-300 bps. Bell 103/113 and Racal-Vadic VA3400 compatible. VA3412 operates at 1200 bps FDX (VA3400) mode.

VA3450 — Direct connect switched network originate/answer triple modem. 1200 and 0-300 bps FDX operation (VA3400, Bell 212A and 103 modes). 2-wire leased line model available.

VA3467 — Direct connect switched network answer only triple modem. 1200 and 0-300 bps FDX operation. (VA3400, Bell 212A and 103 modes.)

VA3480 — Direct connect auto originate/answer triple modem. 1200 and 0-300 bps FDX. (VA3400, Bell 212A and 103 modes.) Operates with VA811 Singleline/Multiline Automatic Calling Unit. **Replaces** Bell 103A/E/J, 113A/B/C/D and 212A.

2400 bps Half Duplex Bell 201 Compatible

VA2450 — Direct connect switched network 2400 bps half duplex modem (with or without 75/150 bps auxiliary channel). **Replaces** Bell 201B/C. 2/4-wire leased line models available.

VA2440/45 — Direct connect switched network 2400 bps half duplex (with or without 75/150 bps auxiliary channel). **Replaces** Bell 201B/C. Operates with VA811 Singleline/Multiline Automatic Calling Unit. 2/4-wire leased line models available.

Available from these stocking reps...

Alabama: (800) 327-6600 • **Alaska:** (907) 344-1141 • **Arizona:** (602) 947-7841 • **California:** S.F. (408) 727-6491, L.A. (714) 635-7600, S.D. (714) 565-1557 • **Colorado:** (303) 779-3600 **Connecticut:** (203) 265-0215 • **District of Columbia:** (301) 649-6000 • **Florida:** Fort Lauderdale (800) 432-4480, Orlando (305) 423-7615, St. Petersburg (800) 432-4480 • **Georgia:** (800) 327-6600 • **Illinois:** (312) 255-4820 • **Indiana:** (317) 846-2591 • **Kansas:** (913) 362-2366 • **Maryland:** (301) 649-6000 • **Massachusetts:** (617) 245-8900 • **Michigan:** (313) 973-1133 • **Minnesota:** (612) 944-3515 • **Mississippi:** (800) 821-3742 • **Missouri:** (800) 422-4591 • **New Jersey:** North (201) 445-5210, South (609) 779-0200 • **New Mexico:** (505) 299-7658 • **New York:** Binghamton (607) 785-9947, N.Y.C. (212) 695-4269, Rochester (716) 473-5720, Syracuse (315) 437-6666 • **North Carolina:** (800) 327-6600 • **Ohio:** Cleveland (216) 333-8375. Dayton (513) 859-3040 • **Oregon:** (503) 224-3145 • **Pennsylvania:** East (609) 779-0200, West (412) 681-8609 • **South Carolina:** (800) 327-6600 • **Tennessee:** (800) 327-6600 • **Texas:** Austin (512) 451-0217, Dallas (214) 231-2573, Houston (713) 688-9971 • **Utah:** (801) 262-3000 • **Virginia:** (301) 649-6000 **Washington:** (206) 364-8830 • **Wisconsin:** (414) 784-9379 • **Canada:** Calgary (403) 243-2202, Montreal (514) 849-9491, Toronto (416) 675-7500, Vancouver (604) 681-8136

Free Short Form Catalog. Better send for yours today, Ma!

Your independent thinking son,

Alexander Graham Jr.

Member IDCMA

Racal-Vadic

RACAL The Electronics Group

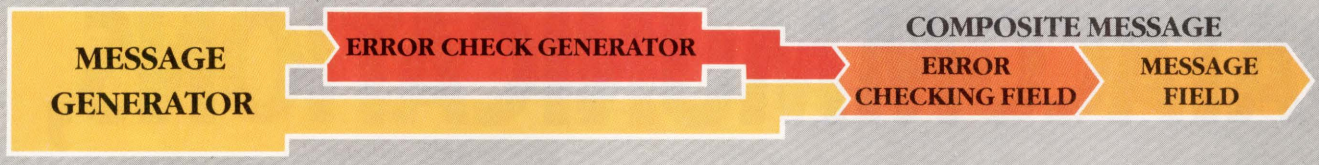
222 Caspian Drive
Sunnyvale, CA 94086
Tel: (408) 744-0810 • TWX: 910-339-9297

Racal-Vadic Regional Offices: West: (408) 744-0810 • **East:** (301) 459-7430 **Central:** (312) 932-9268 • **Northeast:** (617) 245-8790 • **Southwest:** (817) 277-2246

CIRCLE 49 ON INQUIRY CARD

Motorola is the alternate source for these Signetics datacomm circuits.

erfect, you wouldn't need error detection. uits."



Noise, interference and crosstalk can cause random errors in any datacomm system. That's why we designed our 2653, 2661 and 2652 datacomm circuits with special error-control features.

These features make it easier—and less expensive—to implement error control. They also make our circuits extremely versatile. So you can choose the error-control technique that best fits your application.

"It may be the most important job protocols do."

All protocols apply statistical methods to increase the probability of error-free data transfers. These techniques generate special check bits which are added to the end of each message. And monitored by the receiver. When errors are detected, the message is re-sent.

The accuracy—and cost—of error detection depends on the sophistication of the technique you select. These are three of the most popular:

Vertical Redundancy Check. This is the simplest check system. It adds a single parity bit to each character to make the total number of logic "1" bits either odd or even. For example, in an 8-bit code, 7 bits are data and one is the parity.

Longitudinal Redundancy Check. When using LRC, a special Block Check Character is sent at the end of each message or data block. The LRC is obtained by computing parity from corresponding bits of the message characters. The receiver generates its own BCC and compares it to the one that's sent. If they don't match, the message is incorrect.

Cyclic Redundancy Check. This is a more sophisticated system of block checking. CRC divides the data stream with a complex polynomial to obtain the Block Check Character. As with LRC, this character is compared to the BCC generated by the receiver.

In addition to checking for data errors, protocols have other techniques for detecting sequence errors. These include alternating acknowledgements and block sequencing. You'll find them—along with VRC, LRC and CRC—discussed in depth in Signetics' Datacomm Information Kit #4.

"Our circuits have all the error-control features you need."

Our 2653 Polynomial Generator/Checker, 2661 Programmable Communications Interface and 2652 Multi-Protocol Communications Controller are fully equipped to handle error-control for all of today's character-and bit-oriented protocols.

For example, the 2653 supports LRC and CRC checking as well as parity generation and checking. It also operates in parallel mode for easy interfacing to any receiver/transmitter chip. And it performs special character recognition for BISYNC.

By itself, the 2661 supports parity checking and can be combined with the 2653 to handle CRC checking, too. The 2652 implements CRC checking internally for all bit-oriented protocols and many character-oriented protocols.

In addition, both the 2661 and 2652 have special operational modes to help maintain system integrity.

For complete information on our circuits and protocol error-control, send in the coupon for the Signetics Datacomm Information Kit #4. Or call (408) 746-2136 for immediate assistance.

We'll help you get as close as you can to a perfect system.

Signetics

Data Comm Information Kit #4

I want to know more about protocol error-control. Please send me the Signetics Datacomm Kit #4.

Name _____

Title _____

Company _____

Division _____

Address _____

City _____

State _____ Zip _____

Mail to: Signetics Publications Services, MS 1227, P.O. Box 409, 811 E. Arques Ave., Sunnyvale CA 94086

CD12/81

This is the fourth ad in a special datacomm series.

signetics

a subsidiary of U.S. Philips Corporation

IF YOU HAVE ANYTHING TO DO WITH DATACOMMUNICATIONS,

COMMUNICATE.

THE INTERFACE GROUP
P.O. Box 927, 160 Speen Street, Framingham, MA 01701

You're right, Interface '82 is the place I have to be on March 22-25, 1982.

I've marked my calendar. Now send me information.

Name _____

Company _____

Address _____

City_____ State_____ Zip_____

INTERFACE '82 IS YOUR ONE CHANCE OF THE YEAR TO FIND OUT WHAT'S HAPPENING IN DATACOMM.

The whole world of data communications comes together at Interface '82. This is the 10th anniversary for this leading datacomm event and, this year more than ever, Interface will prove to be the single most important event for the industry. Now, co-sponsored by McGraw Hill's BUSINESS WEEK and DATA COMMUNICATIONS magazines, Interface '82 will be not only bigger, but broader. The expanded emphasis will now offer broadened coverage of the world of information networks and office automation. You'll find more exhibits of the latest equipment developments. With over 250 "hands-on" displays in 1000 booths. Plus outstanding conference sessions presented by more than 150 leading international datacomm experts guaranteed to put you right at the leading edge of today's technology.

☐ The Place: Dallas Convention Center. The dates: March 22-25, 1982. Make your plans now to be there. Send in the coupon, and we'll send you updated information on Interface '82.

THE INTERFACE GROUP
Conference & Exposition Management
Producers of
INTERFACE FEDERAL DP EXPO COMDEX
COMDEX SPRING THE COMPUTER SHOWCASE EXPOS

P O Box 927, 160 Speen Street,
Framingham, MA 01701 • 617-879-4502
Outside Massachusetts, 800-225-4620

NOW CO-SPONSORED BY BUSINESS WEEK AND DATA COMMUNICATIONS

TDK and ELPAC Have Combined Their Power Conversion Technology . . .

. . . To Provide the American Market with the Best Value Per Watt In DC/DC Converters

That's right . . . TDK and Elpac have combined their engineering and electronic expertise to expand their availability of DC-DC converters by over 200%. Elpac's nationwide distribution network now makes it possible for you to obtain the best value per watt in DC-DC converters from .2 to 10 watts.

When additional on-board power distribution becomes a necessity, consider the economy of Elpac/TDK converters. DC-DC converters' wide ranging technical specifications allow inputs from 3.5 to 24 volts, single and dual outputs from 5 to 28 volts. Power levels of .2, .25, .3, 1.5, 6, and 10 watts. Solves application problems from battery backup circuits. For technical or applications assistance, contact our Applications Specialist.

Take advantage of the cost-effective versatility that DC-DC converters provide for all your on-board conversions without reconfiguring your main power supply. Exceptional reliability and stability, high MTBF, provide superior performance at an affordable price (as low as $4.00). But, of course, that's part of the Elpac tradition.

For catalog and application charts on Elpac/TDK DC-DC converter line, or for information on Elpac's full line of Brute Force, Switcher, Series Pass and Linear power supplies, call or write today! **(714) 979-4440**

ANOTHER UGLY™
Where Beauty is in the Performance

ELPAC POWER SYSTEMS/TDK®

3131 S. Standard Avenue • (714) 979-4440
Santa Ana, CA 92705 TWX 910-595-1513

CIRCLE 51 ON INQUIRY CARD


S85
S373
S85
S86
AS885

The next generation:

TI's Advanced Schottky magnitude comparator.

One single device—TI's new SN54/74AS885—is now all you need to compare two parallel 8-bit binary words. You would need four standard Schottky parts to equal the functional capability of the AS885. The saving is obvious. The performance outstanding. With TI's Advanced Schottky technology, the next generation of TTL logic is here today.

Speedy and small

The AS885 is more than twice as fast as the standard Schottky arrrangement. Typical propagation delay is only 12 ns vs 28 ns (see table).

Contained in a 24-pin, 300-mil package, the AS885 occupies just 0.4 sq. in. of board space instead of 1.0 sq. in. This compact design includes an octal on-chip latch to store one 8-bit input data word.

Savings with the new Advanced Schottky

	SN54AS885 SN74AS885	Standard STTL Configuration	Your Savings
Packages	1	4	3 packages
Package Area	0.4 sq. in.	1.0 sq. in.	0.6 sq. in.
Pins	24	66	42 pins
Performance (t_{pd})	12 ns	28 ns	16 ns
Power	650 mW	1500 mW	850 mW

As for power, consumption is substantially reduced—650 mW compared to 1500 mW.

The AS885 performs a binary 2's complement magnitude comparison of two 8-bit numbers. With a choice of logical or arithmetic routines built right into your system. And, they can be cascaded to any length.

Advanced technology

The new AS885 is the newest member of the growing Advanced Schottky (AS) Series from Texas Instruments.

As the historical leader in Schottky technology, TI has constantly refined the process until, across the line, the AS Series sets new performance standards. Featuring a typical 1.5-ns SSI gate delay and higher-density MSI, the Series is—typically—twice as fast as the original Schottky family.

In addition, there's an Advanced Low-Power Schottky (ALS) Series that's more than two times faster than today's popular 74LS family—at half the power.

And both the AS and ALS devices can be designed-in as simply as you do with TI's popular Low-Power Schottky (54/74LS) and Schottky (74/54S) TTL series.

Figure the savings

Ideal for high-speed processors and microprocessor/microcomputer-based systems, the AS885 produces real bottom-line results. Fewer components, reduced power consumption, greater performance—they add up to savings in design time, board space, production and operating costs.

Initial quantities of the AS885 are available now. Check with your local authorized TI distributor or TI field sales office.

For more information on TI's Advanced Schottky magnitude comparator, simply fill out and return the coupon today.

Check one: CD4

☐ Please send me more information on your new Advanced Schottky AS885.

☐ You've convinced me. Send me a sample.

Name _____

Title _____

Company _____

Address _____

City _____ State _____ Zip _____

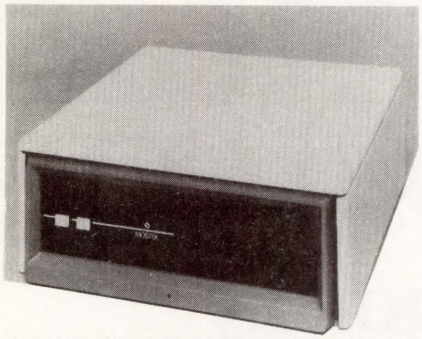
Texas Instruments
P. O. Box 202129
Dallas, Texas 75220

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

TEXAS INSTRUMENTS
INCORPORATED

84114

STD-Bus based computer system can be tailored by user



A series of STD-Bus based computers can be configured by the user to tailor a system using multisourced hardware and software components based on the STD-Bus. This integrated system allows users to select packaging and disc storage components that most closely fulfill select requirements. The Matrix OEM series is Z80 based and comes with or without 8″ (20-cm) floppy disc drives.

Matrix 010 is equipped with a 10-slot card cage, power supply, and fan, allowing it to be used as a nondisc based unit. A single 8″ or 2 low profile 8″ floppy discs can be added. The user then designs in the appropriate 4.5 x 6.5″ (11.4 x 16.5-cm) STD-Bus cards. The Matrix 100 has a single 5.25″ (13.34-cm) single-sided, double-density floppy disc-drive.

Both models are available in rack-mount or tabletop versions with a low profile box measuring 7.8 x 19.0 x 22.5″ (19.8 x 48.3 x 57.1 cm) (010) and 8.3 x 21.0 x 22.5″ (21.0 x 53.3 x 57.2 cm) (100). Power supply is rated at 5 V at 15 A, 12 V at 0.5 A, −12 V at 0.25 A, and 24 V at 3.4 A. The units require standard 115/230 Vac at either 50 or 60 Hz. Future family members will include more disc storage capacity and a 5.25″ (13.34-cm) Winchester disc.

The products are system components aimed at OEMs and system integrators. They provide a level of integration over and above board level by integrating boards, power supplies, storage, and card cages into a box.

The computer package includes a foam front bezel with quick release ball studs so it can be removed for access to the disc drive. The disc drive is mounted in a horizontal plane for low profile appearance and to conserve panel height in rack mount. An adjustable door provides access to the 10-slot card cage. The drive may be removed from front or top for ease of maintenance. **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.

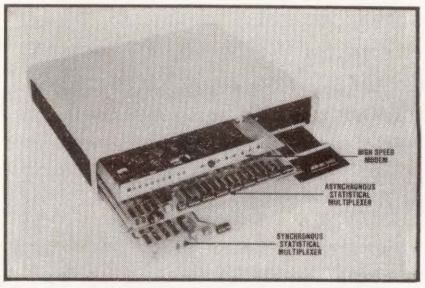
Circle 252 on Inquiry Card

DATA COMMUNICATIONS

Compact data concentrator links remote terminals to minicomputers

A complete, self-contained data concentrator system for linking clusters of remote terminals to minicomputers in point to point communications, the E/SERIES family incorporates three functions in a single package. Units consist of a 4-, 8-, 12-, or 16-channel asynchronous statistical multiplexer/concentrator, optional modem, and optional synchronous statistical multiplexer, all combined in a desktop cabinet.

The system eliminates the need for discrete external communication units and their associated cabling. A minicomputer interface option that allows the series to tie directly to the minicomputer bus further reduces interface and cable costs. The system is designed for users of small to medium sized minicomputers with remote asynchronous terminals.



E/SERIES incorporates three functions. Asynchronous statistical multiplexer, optional modem, and optional synchronous multiplexer channel are contained in single cabinet measuring 3.5 x 17 x 14″ (9 x 43 x 36 cm) and weighing 26 lb (12 kg). Access to each module and to programming switches is via hinged front panel

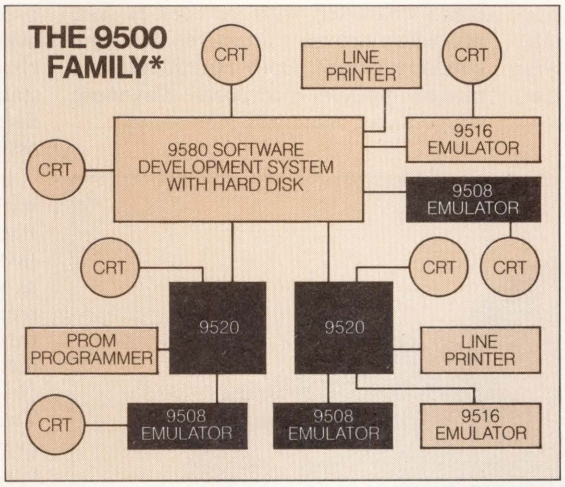
Speed/data code and traffic flow control for each asynchronous channel are independently switch selectable. Each channel can handle up to a 9600-bit/s data rate with a maximum aggregate input of 76.8k bits/s for 8-channel, and 38.4k bits/s for 4-channel versions, respectively. The single synchronous

(continued on page 92)

In-circuit emulation just came unbundled.

Do-it-yourself ICE.™ Start small. Think big. With the Millennium 9508 MicroSystem Emulator and a CRT, you can add a total hardware/software development and integration station to your mini or dedicated development system. Using a single RS-232 port. Or, double your equipment's productivity by using the 9508 stand-alone as a debug instrument.

Real time emulation. With speeds up to 11MHz. So, choose your μP or μC. The 9508 provides full speed emulation for the Z80A, 8085A, 6801, 6803, 6809, 8048, 8049, 8041, 8021 and 8035. With more on the way. But you don't have to buy them all. You simply buy the emulator boards you need. As you need them.



Complete cross-software. If we emulate it, we support it with complete cross macroassemblers. Simple as that. Emulation and cross-software from a single source. Debugged by Millennium.

Mappable memory. The 9508 has up to 16K of high speed memory, mappable on 1K boundaries. Program changes can be made with a line by line assembler. Thus, full memory, register and I/O can be examined and modified, quickly. And, emulation memory can be mapped anywhere in the target μP's address space. So, you can develop a system without a complete hardware prototype. In fact, software debug can begin without hardware.

Real time trace. Capture 128 events in the trace buffer. In real time. Then, display in disassembled form for quick debugging. The 9508 lets you qualify the entered events ten different ways dramatically improving the "Trace Debug Window" into your target system.

Choose your mode. External or internal emulation. Real time emulation step-by-step. Hardware development, software development or hardware/software integration. The 9508 was designed to help you analyze and correct system problems. Efficiently.

Easy to work with. Start with a straightforward command set. Just 25 commands, all of which are functionally relevant. With the command set, you can examine or change any memory location or processor register. Other special commands can help you fill or relocate large portions of memory. And four available hardware and software breakpoints speed your system design.

Systems your way. The 9508 stand-alone emulator is just the first step on the road to a multi-user, multi-tasking microprocessor development system (see diagram above). With a price/performance ratio that is melting the competition's ICE. But what else would you expect from the people who invented unbundled in-circuit emulation.

More information? Call us. Write us. Or, circle one of the Reader Service Numbers below. We'll come running.

MILLENNIUM

Call for information or demonstration

(800) 538-9320 Toll Free

(800) 662-9231 in California

Millennium Systems Inc., 19050 Pruneridge Ave., Cupertino, CA 95014

Millennium Systems is a subsidiary of American Microsystems, Inc.

*Products shaded in black are immediately available.

ICE is a trademark of Intel Corporation.

For information circle reader service number 55

For demonstration circle reader service number 54

data link operates at a maximum rate of 9600 bits/s.

Automatic down-line loading allows individual channel parameters to be set from the master system without operator intervention at the remote end. Down-line loading will not affect data flow on other channels. High peak traffic loads are supported by a 16k-byte buffer. Data flow from computer or terminal is automatically stopped when the buffer is nearly full. Moreover, the user can select out of band or inband traffic control independently for each channel.

Data link control is synchronous X.25 level 2. A 16-bit cyclic redundancy check (CRC) character with go-back-N ARQ procedure provides error-free data link communications. Both multiplexer and modem modules incorporate diagnostic circuits and automatic self-test features.

Designed to incorporate 2400-, 4800-, or 9600-bit/s modems, the series can also operate with conventional free standing external modems. Communications interfaces are standard RS-232-C/CCITT V.24/V.28, with RS-422 or RS-423 available on special order. The synchronous channel option provides statistical multiplexing of synchronous data through dynamic bandwidth assignment.

E/SERIES is designed for interfacing with Digital Equipment, Hewlett-Packard, Data General, Perkin-Elmer, IBM, and similar minicomputers, as well as with frontend processors. The multiplexer/concentrator series is being sold through a worldwide network of distributors. Unit prices are $1650 (4-channel) and $2250 (8-channel). Twelve- and 16-channel versions will be available soon. **Timeplex, Inc,** One Communications Plaza, Rochelle Park, NJ 07662.

—Jim Hughes, Senior Editor

Circle 253 on Inquiry Card

Second generation PCM line filter provides high performance at lower power

Follow-on to the 2912 single-chip monolithic line filter (*Computer Design*, Jan 1979, pp 22-27) for digital telephone systems using pulse code modulation (PCM), the 2912A PCM transmit/receive filter requires less power and offers significantly improved noise performance compared to its predecessor. The device exceeds requirements of AT&T® D3/D4 and CCITT G712 transmission specifications, and also exceeds specifications for digital switching systems used in class 5 central offices.

The second generation chip incorporates many design improvements over the earlier version. By reducing the amount of powered circuitry to a single buffer (powerdown buffer), standby power is reduced from 55 mW to about 0.4 mW. Powerdown buffer maintains the chip in a condition required for rapid power-up into active state.

Active power is reduced from 210 mW to 50 mW, and from 280 mW to 80 mW (without and with power amplification, respectively). This is done by eliminating the class AB output stages of 15 op amps used to drive the filter/capacitor arrays. A technique called "zero-insertion" requires that the amplifiers drive only capacitors instead of both resistive and capacitive loads.

Typical noise rejection for the −5-V supply (V_{BB}) is 45 dB at 1 kHz and 40 dB at 20 kHz. Rejection for the 5-V supply

(continued on page 94)

In OEM modem cards UDS technology deals a full deck

Universal Data Systems' justly deserved reputation in OEM modem cards has been built on one fact — technical superiority lets us deal from a full deck. We've proved our leadership by delivering well over 200,000 OEM modems!

103/113s, 202s, 12 • 12s, 201s, 208s, and the new 9600 bps units are all available in OEM card configuration. UDS has cards for dedicated line applications and cards for dial-up use via a DAA. FCC-certified cards for direct connection to the dial-up network are also available.

If you need OEM modem cards, ask UDS to deal you a hand! (Incidentally, we play the multi-channel rack-mount and free-standing modem games too.) For details, phone your UDS representative or contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone: 205/837-8100.

"Confidence in Communications"

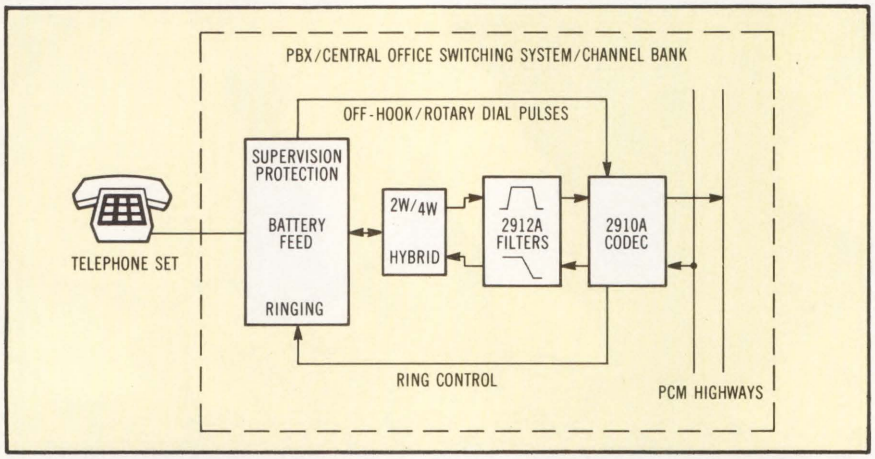
Universal Data Systems

Member IDCMA

DISTRICT OFFICES: **Summit,** NJ, 201/522-0025 • **Blue Bell,** PA, 215/643-2336 • **Atlanta,** 404/998-2715 • **Chicago,** 312/441-7450 • **Columbus,** OH, 614/846-7478 • **Dallas,** 214/385-0426 • **Englewood,** CO, 303/694-6043 • **Santa Ana,** 714/972-4619 • **Sunnyvale,** 408/738-0433 • **Boston,** 617/875-8868.

Created by Dayner/Hall, Inc., Winter Park, FL

CIRCLE 57 ON INQUIRY CARD



Typical line termination. Filter will be used in most applications with Intel's 2910A μLaw or 2911A A Law codecs. Filter and codec furnish 2-chip interface between PCM highways of digital telephone systems and voice telephone lines

(V_{CC}) is also much higher than with the earlier version. High rejection extends to 50 kHz for both supplies. Typical C-message noise, referenced to the codec, is 5 dBrnc0 (receive) and 7 dBrnc0 (transmit). A high pass filter replaces the 50/60-Hz notch filter used in the 2912, effectively rejecting all noise from dc to voiceband. Typical performance is 23 dB at 60 Hz, 28 dB at 50 Hz, and 58 dB at 16 Hz. Common-mode input rejection is 75 dB.

In other respects the new device uses the same switched capacitor and 2-layer polysilicon gate n-channel technology used in the previous version. The chip embodies two fifth-order bandpass filters, smoothing filter, sin x/x correction filter, 600-Ω line driver, op amps, and complementary circuitry. It samples the voice band at 128-kHz internal clock rate in the high pass section and at 255 kHz for other sections.

The device is a universal replacement for the two types of 2912 filters now needed to meet worldwide needs in such applications as channel banks, PBX and central office switching systems, and remote concentrators. It is packaged in a standard 16-pin cerDIP and is available now at $15.60 (U.S.) in quantities of 100. 2910A and 2911A PCM codecs are priced at $15 in 100 quantities. **Intel Corp**, 5000 W Williams Field Rd, Chandler, AZ 85224.

Circle 254 on Inquiry Card

We Fit In Practically Anywhere... Including Your Budget!

The VRC® 6064 Moving Head Memory is rugged enough to withstand the environmental stress of an industrial site, the shock and vibration of a mobile installation, and the sharpened pencil of the accountant. At less than 1/3 the cost of a fixed head memory device, the 6064 provides 16 moving heads to access 131K bytes per cylinder—10.2 megabytes of data. More important, the 6064 offers constant storage density. Each track is the same length, with the same density. Track switch time within a cylinder is only 20 microseconds with no re-seek or additional settling time required. The result is high data throughput equal to that of fixed head drives at a fraction of the cost. All in a compact, durable package.

Compare the rigidity of drum memory with disk. And consider that the heads, actuator and media are mounted within an elastomer suspension system. A dedicated servo system provides accurate and reliable positioning of the heads. These design features provide shock and vibration protection, in adverse environments, for all critical components. Maintenance is simplified, with all electronics and test points outside the media enclosure to eliminate contamination problems. No AC power is required. The drive is brushless DC. Every feature is built-in to enhance performance and reliability.

For more information, call or write: Vermont Research Corporation, Precision Park, North Springfield, VT 05150. Tel: 802/886-2256. TWX: 710-363-6533.

In Europe call or write:
Vermont Research Ltd.
Cleeve Road, Leatherhead,
Surrey, England
Tel: Leatherhead 76221
TLX: 23280

- 10.2 megabytes formatted 5.1 MWords
- 16 moving heads
- Rugged construction

VRC

VERMONT RESEARCH CORP.
VERMONT RESEARCH LTD.

Building Products That Build Reputations.

CIRCLE 59 ON INQUIRY CARD

Q-bus controller handles both Winchesters and floppy backup

Operating systems, along with device driver programs that they invoke, are designed for the CPU manufacturers' peripherals. Although cost and performance improvements can be achieved by mating peripherals from other sources with the processors, operating systems may not support foreign devices. A controller that causes these devices to emulate the manufacturers' devices required for the operating software, however, solves the problem and supplies more options to the user.

The WDC11, a family of multifunction Q-bus controllers developed by Andromeda Systems Inc, serves this function. Contained on a single dual-width card, the controller plugs directly into the Q-bus backplane. Through its bipolar microcontroller and ROM firmware, it can cause independent Winchester and floppy discs to emulate various DEC devices. The controller actually serves three functions at once: with Winchester discs it emulates DEC's RK05 and RL01/2 hard discs, and with floppy discs it emulates the RX02 floppy unit. In addition, it provides an onboard ROM boot for system initialization.

Logical organization of the controller is based on the 8X300 bipolar control chip, which provides the speed needed to handle the high data rates inherent to Winchester drives. Data transfer to the host computer is via DMA, with 18 address bits implemented for direct addressing of 256k bits of CPU memory space. Four additional address bits are provided to handle the anticipated DEC support of a 22-bit address field. Changeover to emulate one or another of the DEC devices is accomplished by simply plugging in the appropriate ROM chip containing the control firmware to drive the 8X300.

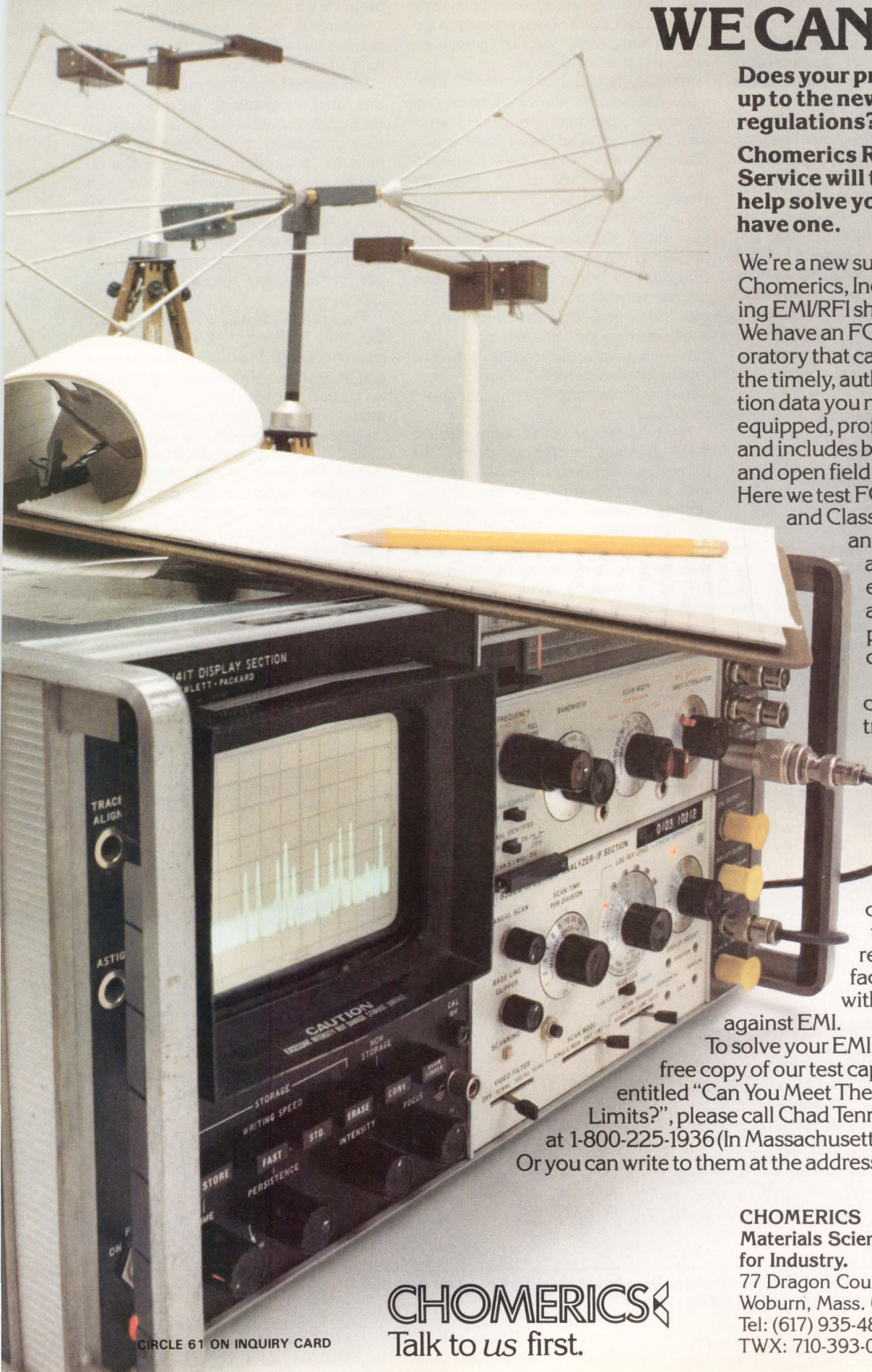
The hard disc controller section of the board is used to interface 8″ or 5.25″ (20- or 13.34-cm) Winchester disc drives to the LSI-11 bus. It can be specified to emulate the RK05, RL01/2, or RP02/3 controllers. The choice depends on data storage capacity of the drives that are used. RK05 emulation is appropriate for 2.5M to 20M bytes; RL01/2 emulation covers the 5M- to 40M-byte range; and RP02/3 is good from 20M to 160M bytes. All versions are software compatible with DEC operating systems using RK, DK, DL, or DP handlers. Each Winchester drive may contain up to eight logical units, depending on capacity. Formatting of individual logical units is supported by the WDC11.

The floppy disc controller section is used to interface 8″ or 5.25″ (20- or 13.34-cm) floppy drives to the bus. This section emulates the RX02/3 double-density floppy disc system, and is software compatible with operating systems using the DY handler. In addition, 8″ diskettes are media compatible with RX01, RX02/3, and Andromeda single-density floppy diskettes for interface purposes. Double-headed disc drives are supported and two logical units are accessible, for total capacity of over 2M bytes. Formatting of both headers and data is supported in both single and double density.

The bootstrap ROM automatically boots either hard or floppy disc, logical unit 0, on power-up or system reset. Any logical unit may be manually bootstrapped by entering the device specification on the console terminal.

(continued on page 98)

IT'S YOUR MOVE:
WE CAN HELP



Does your product measure up to the new FCC EMI regulations?

Chomerics Radiation Test Service will test, tell you and help solve your problem if you have one.

We're a new subsidiary service of Chomerics, Inc., the world's leading EMI/RFI shielding specialist. We have an FCC-replicated test laboratory that can provide you with the timely, authoritative verification data you need. Our lab is fully equipped, professionally staffed and includes both indoor, 3 meter and open field, 10 meter test sites. Here we test FCC-identified Class A and Class B products, business and personal computers and their peripherals, electronic typewriters and other microprocessor devices for compliance.

Failure to comply can delay product introduction so we'll recommend the most cost-effective solution to prevent excessive radiation. Chomerics brings to this process 20 years of high technology materials research and manufacturing experience with products to shield against EMI.

To solve your EMI problem, or for a free copy of our test capability brochure, entitled "Can You Meet The New FCC EMI Limits?", please call Chad Tennant or Tony Genova at 1-800-225-1936 (In Massachusetts, call 1-800-842-1134). Or you can write to them at the address below.

CHOMERICS
Materials Science and Engineering for Industry.
77 Dragon Court
Woburn, Mass. 01888
Tel: (617) 935-4850
TWX: 710-393-0173

CHOMERICS
Talk to *us* first.

CIRCLE 61 ON INQUIRY CARD

Depending on the device performing the emulation, a simple adapter or personality board may be required to accommodate connector pinouts and interface variations. These plug into the device proper and are contained entirely within its envelope. No personality card is needed for a configuration consisting of WDC11 and a single 5.25″ Winchester. Any combination of four Winchester or floppy drives may be controlled.

Among the devices currently supported are the Quantum Q2000 and Shugart Associates' SA1000 8″ Winchesters, Computer Memories' CM5000, and Seagate Technology's ST506 5.25″ Winchesters; and Shugart SA800, SA850, and Tandon TM100-4 floppies or equivalents. **Andromeda Systems Inc**, 9000 Eton Ave, Canoga Park, CA 91304.

—Peg Killmon, Senior Editor

Circle 255 on Inquiry Card

Two CMOS devices interface ARINC and Manchester buses

High performance CMOS bus interface circuit, HS-3282, is designed to meet ARINC 429-1 specifications, while dielectrically isolated bipolar differential line driver, HS-3182, complies with ARINC 429-4 requirements. Manufactured by Harris Semiconductor, the HS-3182 interfaces with the HS-3282 and a Manchester bus. Applications for the parts are seen in airborne commercial aircraft computers and navigation equipment.

HS-3282, the ARINC 429 bus interface circuit, also meets the requirements of similar encoded item multiplexed serial data protocols. The device consists of a transmitter and two receivers that operate at a frequency of 10 times the receiver data rate, which can be the same as, or different from, the transmitter data rate. Although the two receivers operate at the same frequency, they are functionally independent and each receives serial data asynchronously. The transmitter section consists primarily of a FIFO memory, which holds eight ARINC data words for serial transmission. The timing circuit correctly separates each ARINC word as required by the ARINC specification.

Even though the specification calls for a 32-bit word, including parity, the HS-3282 can be programmed to operate with a word length of 25 bits. The incoming receiver data word parity is checked, and a parity status is stored in the receiver latch and then output during the first word. Depending upon the status of a control signal, the parity generator will generate either odd or even parity. A logic 0 will cause odd parity to be generated and input to the output data stream. Conversely, a logic 1 will result in the generation of even parity that will be input to the output data stream.

An external TTL clock input allows the bus interface circuit to operate at data rates from 0- to 1M bit/s. To ensure no data ambiguity, the TTL external clock must be 10 times the data rate. The interface circuit is guaranteed to support 1M-bit/s data rates of ARINC specification 429-1 over both the voltage (±10%) and full military temperature range. It interfaces with TTL, CMOS, or NMOS support circuitry, and uses a standard 5-V supply.

Fig 1 is a block diagram of the device. The chip grew out of the company's custom digital and linear development and ruggedized processing capabilities. As a result, the chip has both analog and digital functions. For example, the two receivers are differential op amps.

Fig 2 shows the device interface timing control for receiving and transmitting. The timing sequence for loading the transmitter FIFO memory is shown in timing interval A. A transmitter ready (TX/R) flag signals the user that the transmitter memory is empty. The user then enables the transmitter data, a 16-bit word, on the data bus and strobes

(continued on page 100)

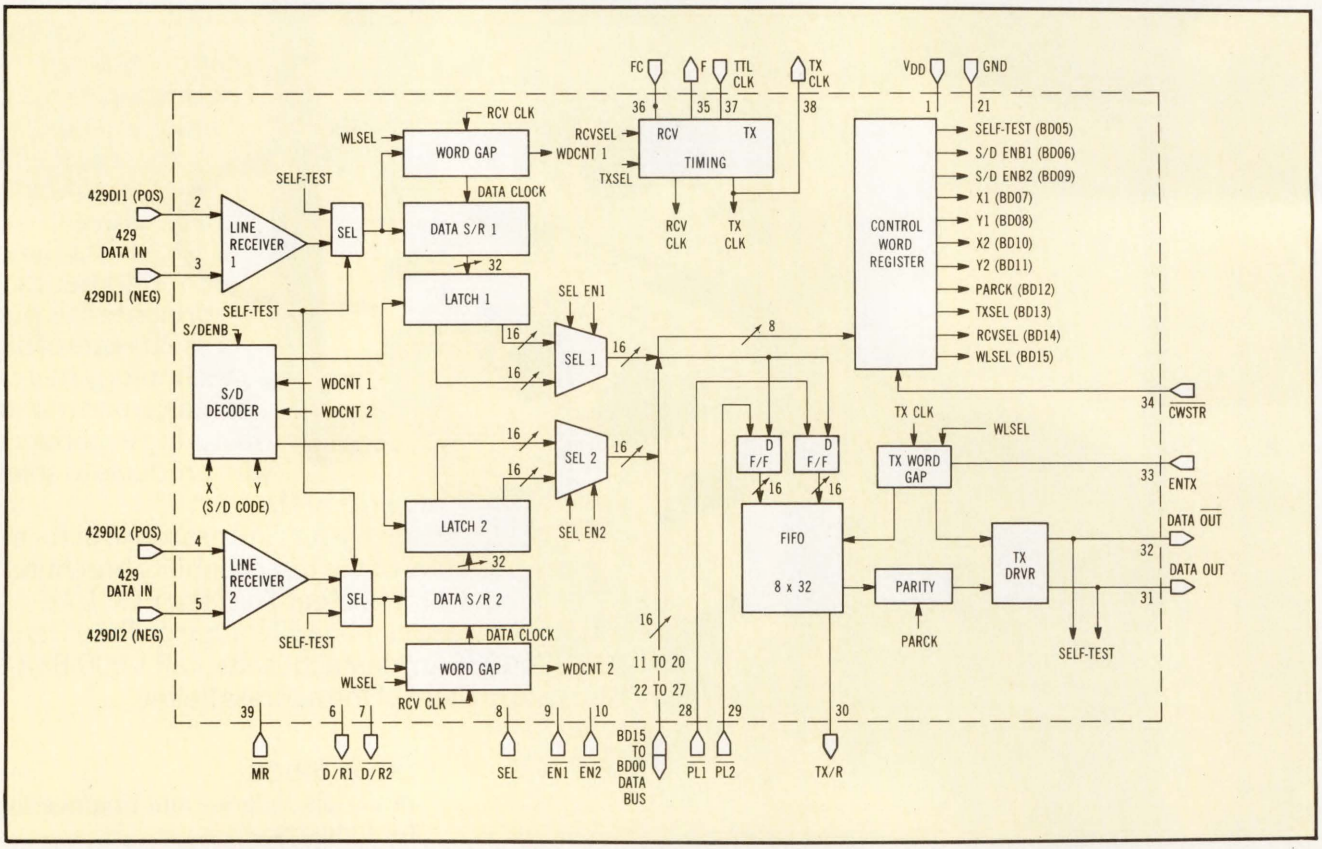


Fig 1 ARINC 429 interface device block diagram. Data bus is shared between receiver and transmitter. Bus control must be shared synchronously

IMAGE PROCESSING, KENTUCKY COAL AND YOU.

"The DeAnza IP6400 is an ideal tool for georeferencing LANDSAT data and for classifying the digital image into distinct land cover categories."

So says Peter Croswell of Kentucky's Land Unsuitable for Mining Program. Linked to a PRIME 750* minicomputer, the IP6400 Image Array Processor is used by Croswell to display, integrate and manipulate a variety of geo-based files as Kentucky attempts to achieve a delicate balance between surface coal mining and the fragile environment.

The Ideal Image Processing Tools for Your Application

The IP6400, one of our more powerful image array processors, provides features ideal for a variety of applications—

• Up to four 512 x 512 line x 8 bit image memories • Arithmetic computations in one frame time • High resolution color, monochrome or pseudo-color • Independent zoom and scroll with each memory controller

Whether your application is LANDSAT processing or non-destructive testing. Biomedical image enhancement or process control synthesis. Movie-mode animation or three dimensional computer graphics . . . DeAnza can provide the image processors and display systems, a basic software library and the experience to meet your image processing needs.

Which DeAnza System is Right for You?

Let's explore the possibilities.

Your application may call for the large memory and state-of-the-art performance of our powerful Image Array Processors. Or perhaps the more modest capabilities of our Image Display Systems. Or the stand-alone convenience of our Visual Display/Computer System.

Call Today for Answers.

But to provide the best answer, we'd like the opportunity to analyze your application and the system sophistication you require.

Call or write today, tell us what you need, and we'll go to work for you.

* PRIME 750 is a trademark of Prime Computer.

DeAnza Systems

The Leader in Image Processing

118 Charcot Avenue, San Jose, CA 95131.
(408) 263-7155 TWX (910) 338-7656
Regional Offices and Distributors Worldwide

LANDSAT imagery of Kentucky Coal Mining Terrain.

CIRCLE 62 ON INQUIRY CARD

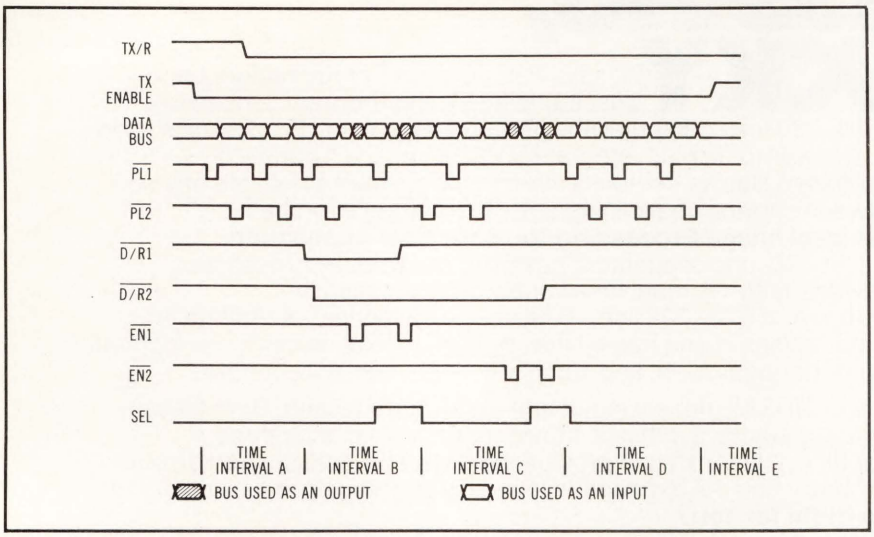


Fig 2 Typical interface timing sequence of HS-3282

the transmitter with a parallel load signal. The second part of the 32-bit word is similarly loaded into the transmitter with $\overline{PL2}$, which also initiates data transfer to stack. While the user is loading the transmitter, he does not have to service the receiver even if the receiver flags the user with the signal $\overline{D/R1}$ that valid received data are ready to be fetched. This is shown by the timing interval B. If the user decides to obtain the received data before the transmitter is completely loaded, he sets the two parallel load signals ($\overline{PL1}$ and $\overline{PL2}$) at a logic 1 state, and strobe $\overline{EN1}$ while the signal SEL is at a logic 0 state. Fifty ns after the negative edge of $\overline{EN1}$, the receiver data become valid on the data bus. At the positive edge of $\overline{EN1}$, the user should toggle the signal SEL to ready the receiver with the second 16-bit word.

During the time period in which the user fetches the receiver words, he can load the transmitter in between the two enable pulses ($\overline{EN1}$). This is shown by the timing interval B. Receiver 2 is serviced similarly, and is illustrated by timing interval C. Timing interval D shows the rest of the transmitter loading sequence and the beginning of the transmission by switching the signal TX enable to a logic 1 state. Timing interval E is the time it takes to transmit all data from the FIFO memory, either 288 bit times or 232 bit times.

HS-3182 directly interfaces with the ARINC bus interface circuit and can drive a shielded 2-line data bus. Fig 3 is an ARINC driver circuit block diagram. Two external capacitors can be used to adjust rise and fall times and the output differential range via the voltage reference input. The device can operate at a data rate of up to 100k bits and is available in a 16-lead DIP. Both parts satisfy mil spec requirements. **Harris Semiconductor, Programs Div**, PO Box 883, Melbourne, FL 32901. Circle 256 on Inquiry Card

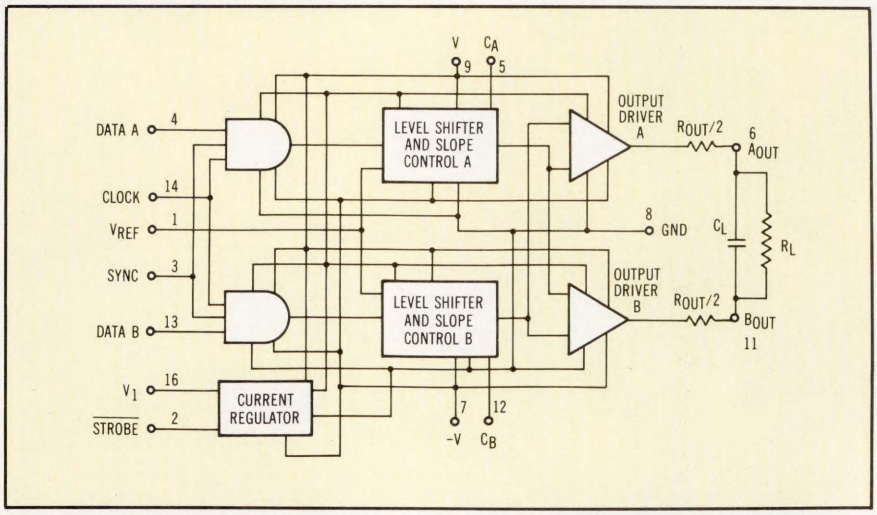


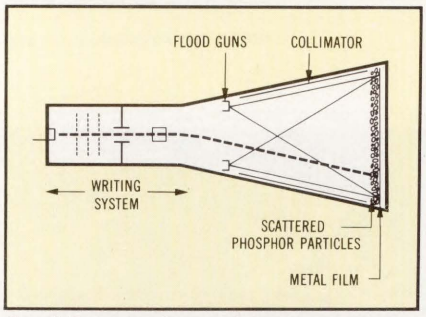
Fig 3 HS-3182 ARINC 429-4 driver circuit. Device interfaces with HS-3282 and drives 2-line data bus

TEST & MEASUREMENT

50-MHz oscilloscopes offer 2-mV sensitivity on dual-trace vertical inputs

A family of 50-MHz bandwidth oscilloscopes, Philips' PM3215, PM3217, and PM3219 have 2-mV sensitivity on dual-trace vertical inputs and offer outstanding price/performance ratios. PM3215, a single-time base instrument; PM3217, a dual-time base unit; and PM3219, a dual-time base unit with storage, all offer excellent trigger facilities including auto trigger level detection. Display possibilities include alternate time base, Z modulation, and X-Y displays.

Tube design of the PM3219 ensures maximum light output in either storage or nonstorage modes. A special magnesium oxide storage layer allows high intensities with no burn-in problem. Developed by Philips' Electronics Components Div, a burn resistant secondary emission insulator enables the scope to provide maximum light output in both storage and nonstorage modes. The development is expected to substantially cut the number of CRT burn-in related repairs caused by user error.



Special magnesium oxide storage layer on tube of PM3219 allows maximum light output in both storage and nonstorage modes with no burn-in

Performance of the CRT (see diagram) is made possible by substituting a magnesium oxide based layer for the more conventional magnesium fluoride on the storage mesh. While magnesium fluoride provides slightly higher initial writing speeds, it ages rapidly and is prone to irreversible burn-in markings if a high intensity beam stays on the screen too long. The magnesium oxide layer is harder chemically and lasts longer. An after-image may persist for a short time but will fade, leaving the screen "clean" after 24 hours. Other features of the tube include a quick start ensured by fast heating cathodes in both writing and flood guns. Warm-up is compressed into a 5-s time frame, and an improved collimation system guarantees a full display

(continued on page 102)

MANY PEOPLE THINK OF PENRIL AS THE BELL COMPATIBLE MODEM COMPANY

MAYBE that's because our 300/1200 is FCC registered and a Bell licensed replacement for the 212A...with over 10,000 in field use. Or maybe it's because our exclusive 2-chip switched capacitor filter replaces 22 filter chips in the Bell 212A version. It might even be our broad range of Bell compatible modems and accessories that satisfy Bell equivalent applications.

THEY'RE right. Penril is the Bell compatible modem company. But we're also a broad line data communications company. Our line of modems includes short haul, high speed and even centrally controlled diagnostic versions. Our centralized network controllers keep your data moving. And our statistical multiplexer makes your network more efficient.

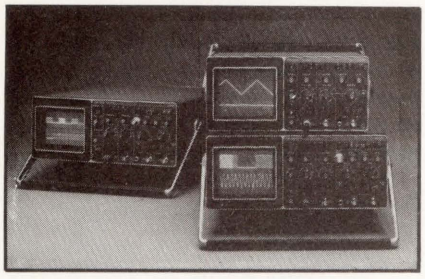
Now that you know we're the Bell compatible modem company...and a lot more...call us on the Penril Data Communications Hot Line (301) 881-8151.

Penril
Data Communications Division
5520 Randolph Road
Rockville, Maryland 20852
(301) 881-8151

CIRCLE 63 ON INQUIRY CARD

over the entire screen with no diminution of light output at the edges.

The unit has been designed to provide comprehensive, cost-effective storage of single-shot transients, low frequency phenomena, and other signals. It combines sophisticated facilities, such as babysit mode and auto erase, with its 50-MHz specification. Combining the dual advantages of variable persistence and variable storage allows, for example, low frequency signals to be displayed without flicker and also gives clear displays of fast pulses with low repetition rates.



50-MHz scope family from Philips covers range from single-time base to dual-time base with storage. All offer trigger facilities including auto trigger level detection

Variable persistence is obtained simply by using the instrument's memory and write pushbuttons. This effectively adds a tail to a slow moving signal, giving a continuous flicker-free display. The persistence control allows timing of this tail to be adjusted between 0.5 s and 1.0 min. Used to accentuate a changing signal trend, the persistence time is set so that the old trace fades away just as the new trace is written.

Variable storage is obtained by switching from write to read. At the instant of switching, the display on the screen is stored by the oscilloscope. Adjustable storage time allows signals to be retained and viewed for 1 min at maximum brightness, or 1 h at minimum brightness.

If the persistence control is set to the maximum, there is up to 1 min in which the occurrence of a transient can be noted and the display stored. Auto store or babysit mode can be used to capture transients by monitoring a normally static line unattended for up to 24 h. Any transient on the line is captured, but not displayed until required.

Auto erase allows the view time to be set between 1 and 10 s. In this way, a signal or part of a signal that repeats itself within this time span can be seen continuously on the screen. High external triggering sensitivity ensures stable triggering on TTL levels when 10:1 attenuator probes are used. Loss of time caused by readjusting the trigger level when the duty cycle changes is prevented by dc trigger coupling. The variable trigger holdoff time avoids double writing problems while retaining sweep calibration. Separate source triggering for both time bases is another feature. When both A/B buttons are pressed, composite triggering is obtained. This trigger mode gives a stable display of two signals that are unrelated in time, phase, or frequency.

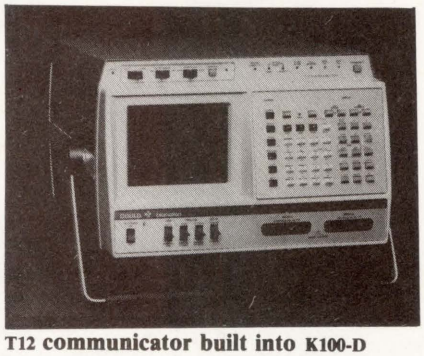
The single-time base PM3215 is available for $1175; the PM3217 with dual-base delayed sweep costs $1495. The PM3219 storage scope with no-burn CRT is priced at $4195. **Philips Test & Measuring Instruments, Inc**, 85 McKee Dr, Mahwah, NJ 07430.

Circle 257 on Inquiry Card

Logic analyzer incorporates communications for remote programmed diagnostics

Designed to allow factory engineers to perform remote fault diagnosis on field-installed computers or other digital products, the T12 communicator allows two logic analyzers to exchange data over a nondata-certified dial-up telephone line. Built by the Biomation Operation of Gould Inc's Instrument Div, the T12 incorporates a 1200-bit/s half-duplex modem, which preconditions signals before sending them out over the telephone line; and a microprocessor based controller, which manages communication between an internal modem and the GPIB interface of the logic analyzer. The T12 system is built into a Gould Biomation K100-D logic analyzer which, in addition to hardware timing analysis, is also able to trace the dynamic execution of software.

Four operating modes—automatic self-test, a built-in voice transmission capability, an auto answer mode, and an error detection/retransmission protocol—are supported by the T12. Thus, a factory engineer can instruct people at the remote site where to attach their analyzer's probes to the system under test.



T12 communicator built into K100-D logic analyzer. Combination allows transmission of programmed test parameters to similar remote unit connected to system under test. Results can then be transmitted back to factory engineer for evaluation

Performed during power-up and repeated automatically at regular intervals, self-tests check indicator LEDs, switches, and GPIB lines, and also check for errors in any of the three 4k-byte P/ROMs and three 256-byte RAMs that make up the T12's memory.

In addition to providing send and receive modes for data communication, the T12 allows the user to program and set up test parameters on the analyzer and transmit them to the remote unit. The user can then record the tests and send and display the recorded data on the instrument, where he can further manipulate, reformat, and compare it, to develop a diagnosis.

To facilitate error detection, data are transmitted between two T12s in blocks of up to 519 bytes each. Eight of these bytes are reserved for cyclic redundancy checks and synchronization, to signal start and stop of data. The remaining 511 bytes are used for transmitting the data. A "record complete" indicator on the T12s at both ends of the link acknowledges successful transmission, reception, and verification of a data block.

Voice communication is permitted over the same telephone line, and is signaled on the receiving end by a flashing LED and beeper tone. If data transmission is in progress, the alert signal is delayed until the current block has been successfully transmitted. When the automatic answering switch is activated, incoming calls are answered and the remote operator can transmit commands and data without any intervention at the remote site. **Gould Inc, Biomation Div**, 4600 Old Ironsides Dr, Santa Clara, CA 95050.

Circle 258 on Inquiry Card

Programmable pulse generator includes dual-channel and summing options

Designed for automatic test equipment (ATE) and bench applications, the model 2021 programmable pulse generator provides an output pulse range frequency of 10 Hz to 50 MHz, ± 20-V outputs (single channel), and transition times from 5 ns. Characteristics of the instrument family include the automatic calibration of frequency and voltage levels, delay, and width; an IEEE 488

(continued on page 104)

UNTIL NOW, LOCAL AREA NETWORKS WEREN'T REALLY A FACT. EVEN IN FANTASY.

Local area networking is an idea whose time has come. Almost. Massive investments of time and talent have created the concept – and the cable – to connect the network's stations. But so far only lip service has been paid to the interconnection of incompatible devices.

Some companies seem to believe the problem will eventually solve itself. Others feel that by ignoring it, it may go away. Still other companies, motivated largely by self-interest, have set out to create proprietary networking systems.

AT INTERLAN, WE'VE CHANGED ALL THAT.

Interlan is a new company that believes local area networking is not just desirable, it's inevitable.

That's why we have produced the hardware and software technology needed to connect almost any make of computer to today's networks. And we're already developing the equipment to make full use of tomorrow's networks.

For OEM's, Interlan means that compatibility – and more value – can be built directly into products, simply and inexpensively.

For end users, Interlan means greatly increased computing and data communications capabilities without greatly increased budgets.

DEDICATED TO SOLVING LOCAL AREA NETWORKING PROBLEMS.

At Interlan, we see the growth of networking as a tremendous business opportunity. But we also see it as our responsibility to turn tomorrow's ideas into hardworking realities. And we will.

To find out how Interlan can make local area networking a reality for you today, call or write.

INTERLAN

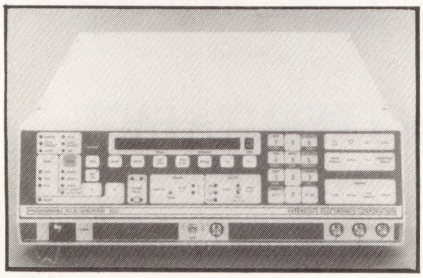
WE MAKE NETWORKS WORK.

160 Turnpike Road, Chelmsford, MA 01824
617-256-5888 (TWX) 95-1909

CIRCLE 64 ON INQUIRY CARD

interface; and user friendly controls and displays. Manufactured by Interstate Electronics, the 2021D has dual channels while the 2021DS has dual channels plus a summing capability.

Up to 10 store/recall messages or complete settings for a pulse signal can be stored (eg, waveform, voltage output, and pulse modes). Stored settings can be quickly displayed and reactivated. In addition, the dual output option provides a second output channel with independently programmable voltage levels, output impedance, waveform, delay width, duty cycle, and transition times. The second channel output shares a common repetition rate, burst count and mode, with the first channel.



For applications requiring a burst of high energy pulses, such as laser based systems, or when a series of stepped-output pulses are needed, the 2021DS summing option combines both outputs of a dual-channel 2021D to provide up to a ± 40-V peak to peak pulse. The VMOS output amplifier provides output immunity to short circuits and open circuit faults, even under high energy summing conditions. **Interstate Electronics Corp, Signal Source Operations**, 1001 E Ball Rd, PO Box 3117, Anaheim, CA 92803.

Circle 259 on Inquiry Card

In-circuit tester family expanded to accept high pin-count boards

Systems 2271 and 2272 have been added to GenRad's 227X family of in-circuit board testers. The 2271 can accommodate up to 960 nodes, while boards with as many as 3584 pins can be handled by the 2272. Concurrently with this introduction, the company announced release 7 of its Automated Test Generation (ATG) software and also the availability of the 2294 multi-user programming station.

The two new test systems have evolved from the earlier 2270 480-pin capacity system. All are designed to test a wide range of board sizes and complexities; and either analog, digital, or hybrid device technologies. Such features of the 2270 as parallel stimulus/response architecture, local driver/sensor memory, ATG software, and complete ac and dc

227X circuit board test system family. 2272 (foreground), 2271 (background right), and 2270 (background left) share same basic system architecture and can use same test programs. Fixtures are upward compatible between systems

(continued on page 106)

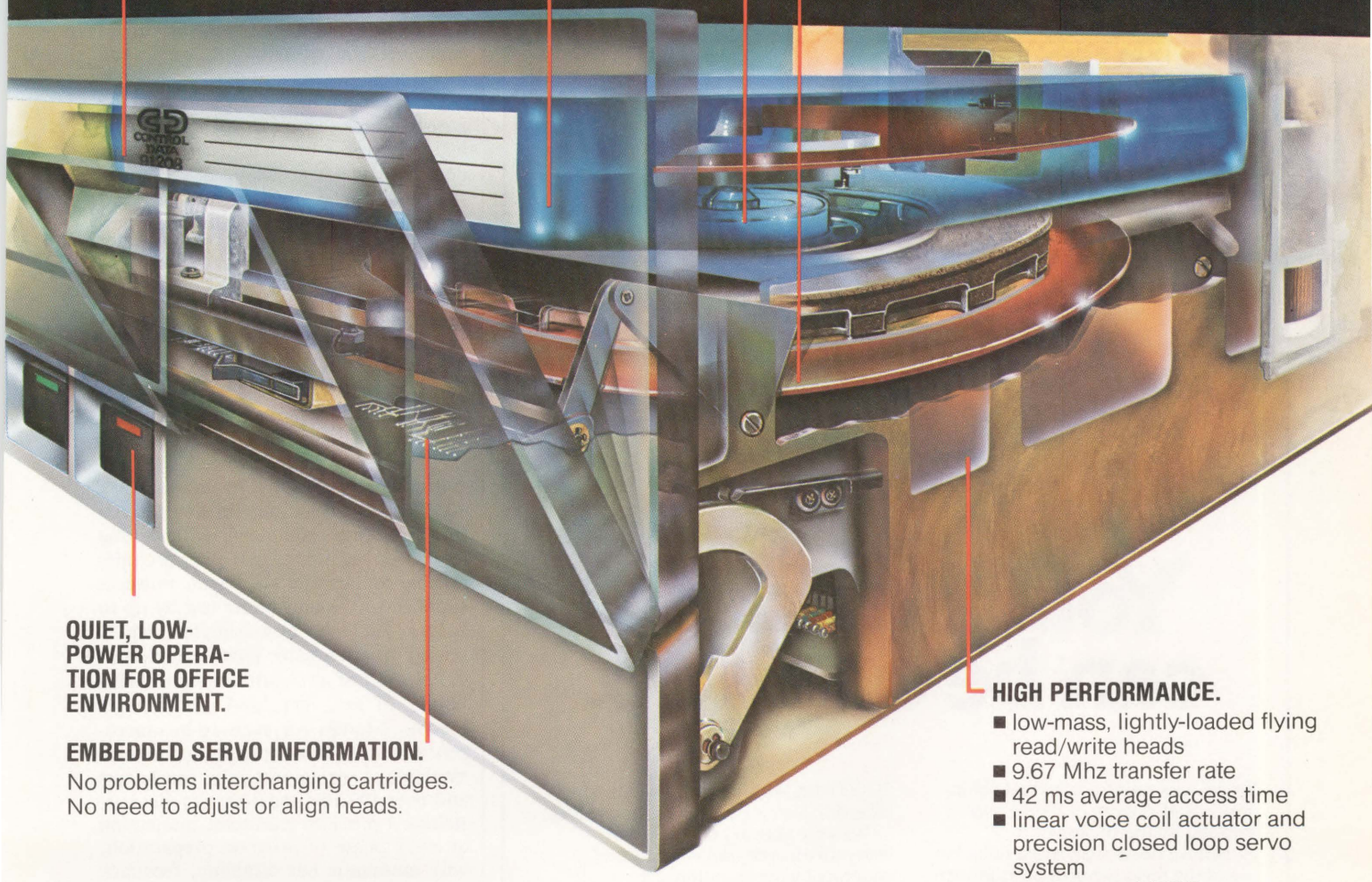
The LARK™

SOLVES BACK-UP AND OFF-LINE STORAGE PROBLEMS. Besides 8 Mbytes of *fixed* storage, Lark gives you 8 Mbytes of *removable* storage—per cartridge. Simplifies back-up and gives users both flexibility and growth capacity.

EQUIPPED WITH SMD INTERFACE. The 9455 Lark includes power and I/O module. And it's equipped with an SMD interface so you can use a common controller for the Lark and many other drives. But the 9454 Lark uses host power, and includes a new Micro Family Interface should you want to design your own controller.

COMPACT SIZE AND PACKAGING FLEXIBILITY. You can design smaller, more efficient systems. The Lark is the width of a floppy disc drive. In fact, you can mount two units horizontally or three vertically in a standard 19-inch rack.

EXCEPTIONAL RELIABILITY. Since the Lark is totally sealed during operation, no external air is forced across either the fixed module or cartridge disk surfaces.



QUIET, LOW-POWER OPERATION FOR OFFICE ENVIRONMENT.

EMBEDDED SERVO INFORMATION.
No problems interchanging cartridges. No need to adjust or align heads.

HIGH PERFORMANCE.
- low-mass, lightly-loaded flying read/write heads
- 9.67 Mhz transfer rate
- 42 ms average access time
- linear voice coil actuator and precision closed loop servo system
- 7500 hours MTBF

Now—an 8 inch drive with REMOVABLE MEDIA

For more information write:
OEM Product Sales, HQN08J
Control Data Corporation
P.O. Box 0, Minneapolis, MN 55440

CONTROL DATA

Addressing society's major unmet needs as profitable business opportunities

CIRCLE 66 ON INQUIRY CARD

instrumentation are retained in the new systems.

The testers' 14-bit instrumentation provides high accuracy for analog measurements. A quadrature reactance bridge enables combined phase and magnitude measurements to differentiate between parallel-wired components. Each pin has programmable access to both system and external IEEE instruments by way of a 4-line instrument switching matrix.

For digital testing, each point has a driver/sensor backed by local memory. This eliminates the need to repeatedly scan a single sensor for each output. Local driver/sensor memory provides constant and controllable timing for testing sequential devices. Placing a sensor at each point also enables automatic verification that the stimulus level for each test step is correct. Dual programmable positive/negative logic levels enable testing of ECL, TTL, MOS, and mixed logic boards and devices.

Costs per pin have been held down by a system architecture called "multiplexing." Since the in-circuit test technique does not require access to all system instrumentation at any time during the test procedure, multiplexing allows the new high pin-count systems to share instrumentation across groups of pins.

System 2272 can handle the densest PCB configuration and is particularly applicable to: high device-count ECL boards; bus-structured VLSI based CPU, memory, and I/O boards; and mass storage, communications, peripheral, and other typically hybrid boards. It accommodates three standard fixture sizes: 15 x 18″ (38 x 46 cm), 22 x 30″ (56 x 76 cm), and 30 x 30″ (76 x 76 cm). A vacuum actuated fixture interface combined with spring loaded power and signal pins provides reliable contact and alignment. Power is supplied to the unit under test by up to four 17-A/35-A current-limited remote sensed programmable power supplies.

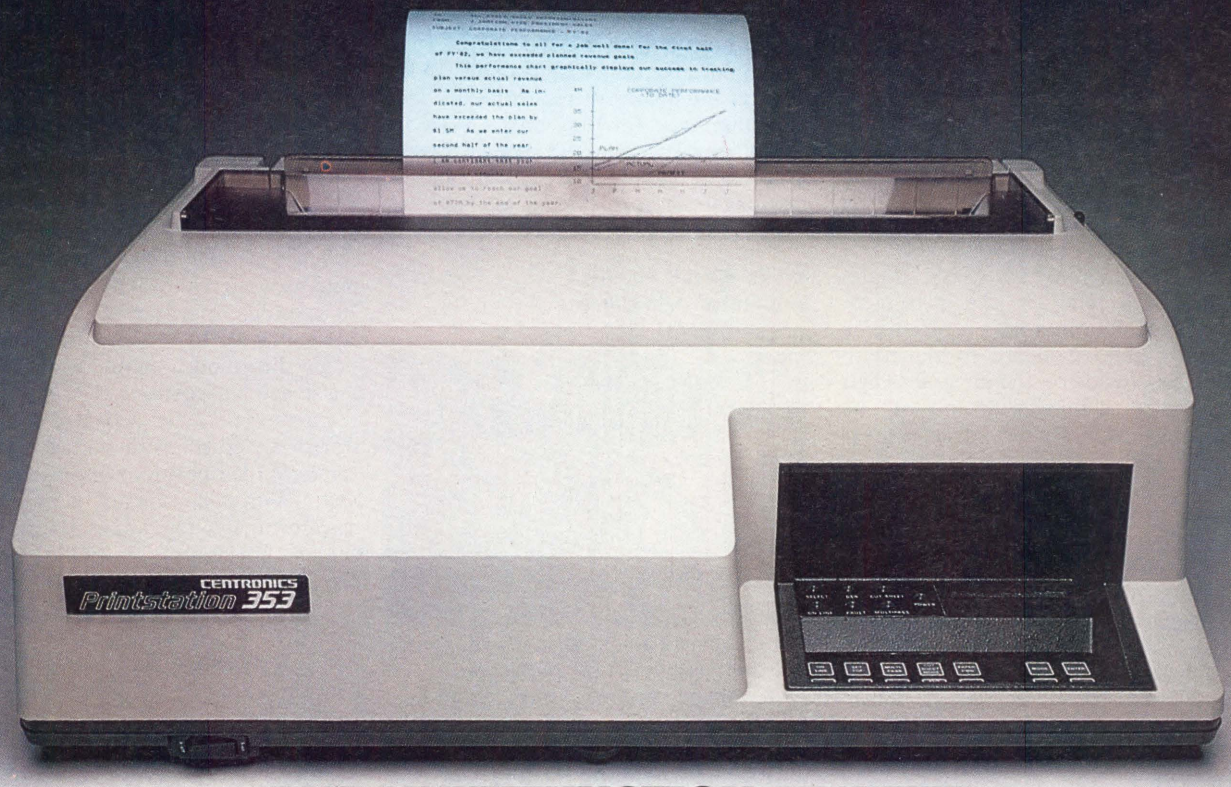
Release 7 of ATG software expands the library of ECL, TTL, and CMOS device models. Models for such 16-bit microprocessors as the 68000, Z8000, and 8086 are available as are support chips for the 8086 and over 100 10k and 100k ECL devices. Release 7 provides maximum automation at every phase of program preparation, with automatic bus disabling, feedback squelch, and wiring compensation.

Multi-user programming station 2294 is offered for users with larger programming needs. Based on the DEC PDP-11/44, it provides simultaneous full ATG support for up to eight programmers. Multiple 227X systems can also be configured with the 2294 acting as central controller of the GRnet™ network. This network provides central file storage and downloading of test data at rates said to be up to 40 times faster than standard data networks.

Prices for the 2271 and 2272 in usable configurations start at $150,000 and $180,000 respectively. Prices for the 2294 programming station start at $90,000. **GenRad, Inc, Board Test Div,** 300 Baker Ave, Concord, MA 01742.

Circle 260 on Inquiry Card

THE PRINTSTATION 350. ITS BEAUTY IS MORE THAN SKIN DEEP.



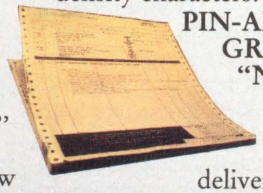
THE MULTIFUNCTION PRINTER WITH UNMATCHED PAPER HANDLING CAPABILITY.

If all you look at is the handsome, office-styled cover you'll miss the real beauty of its functionality, its revolutionary paper handling design and its list of standard features that even competitors' "options" lists can't match.

Centronics' new Printstation 350 is truly the "one-printer solution to the complete range of data processing, business processing, and word processing printing needs".

SEMI-AUTOMATIC PAPER HANDLING... FAN-FOLD, MULTI-PART FORMS, AND CUT SHEET loaded instantly and switched rapidly. In fact the Printstation 350 can be loaded with cut sheets faster and easier than a typewriter.

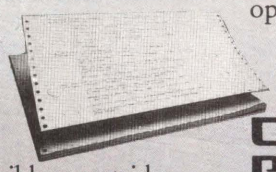
LETTER QUALITY PRINTING, a word processor's dream...using multipass technique for high resolution, high density characters.



PIN-ADDRESSABLE GRAPHICS PLUS "NO-WASTE" DEMAND DOCUMENT REMOVAL deliver true business processing capabilities.

HIGH SPEED "DRAFT" MODE with standard 200 CPS bi-directional logic-seeking feature for data processing operation.

ECONOMY-MINDED, OPERATOR-ORIENTED SERVICE FEATURES. Self-diagnostics are standard. So is the operator-replaceable printhead and the truly "clean hands" snap-in ribbon cartridge.



FAMOUS CENTRONICS BACK-UP. 12 years and 400,000 printers-worth of experience backed up with a world-wide network of factory service locations.

So don't judge a printer by its cover especially when it's one of the Printstation 350 family. Because underneath there's a unique collection of capabilities, mechanical architecture, and electronics that provide a level of versatility we call PRINTSTATION PROCESSING. But if beauty is in the eye of the beholder, you should behold the Printstation 350 in operation. For more information or a demonstration, contact us today.

CENTRONICS® PRINTSTATIONS

Centronics Data Computer Corp., Hudson, New Hampshire 03051
603-883-0111

CIRCLE 68 ON INQUIRY CARD

Portable digital test lab combines six essential functions

An all-in-one portable digital lab, unveiled by the B&K-Precision group of Dynascan Corp, combines functions of signature analyzer, logic analyzer, autoranging frequency counter, autoranging ac and dc digital voltmeters, and autoranging digital ohmmeter. This combination, when combined with a portable scope, allows the LA-1000 System Analyzer to rival capabilities of an average engineering bench.

Operating as a 20-MHz, single-channel logic analyzer, the instrument can present data in both state and time domains. State data are formatted in hexadecimal code on the integral 4-digit LED display. Timing diagrams of one channel by 16 bits can be displayed externally on most conventional oscilloscopes. For convenience, clock pulses and a cursor are also displayed on the scope display. Memory permits storage of 16 words, with 16 bits per word, in 256-bit deep memory. The word number is indicated on an LED readout.

Signature analysis capability makes it possible for semiskilled technicians to troubleshoot microprocessor based products to the component level. When signature analysis is used in association with other test capabilities, field engineers can solve complex problems, thereby avoiding the need to send a board to a central repair depot for testing and possible repair.

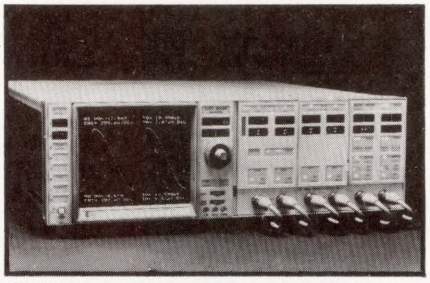
When analyzing a product designed for signature analysis, a circuit is traced until observed signatures fail to match those on the product's schematic diagram. With its data probe connected to a circuit node, the analyzer transforms the sensed bit stream into a unique 4-digit modified hexadecimal display. When a component with a correct input signature and incorrect output signature is reached, the problem has been isolated.

Eliminating the need for a separate DVOM, the instrument has a built-in microcomputer controlled meter. Its autoranging circuitry displays ac and dc voltage and resistance on an integral 3½-digit display. Microcomputer control offers fast, simple operation. The user selects the function desired and interfaces to a circuit under test; the DVOM's computer automatically selects the range, providing maximum resolution. Accuracy is to 0.1% dc and best ac accuracy is 0.5%. Resistances can be measured to within ±0.3%. All functions are overload protected.

Autoranging frequency measurement to 25 MHz allows clock and rf measurements to be made. Frequencies are displayed on a 6-digit LED readout and may be autoranged or measured with fixed resolution in the 1-s mode. Frequency counter input is through the data probe input of the SP-1.

The portable unit weighs under 14 lb (6.4 kg) and is constructed with extruded aluminum case for ruggedness. Price is $1745. **B&K-Precision, Dynascan Corp,** 6460 W Cortland St, Chicago, IL 60635.
Circle 261 on Inquiry Card

Scope option supplies automatic time domain measurements



Digital waveform storage. Installed on 1980 oscilloscope, Hewlett-Packard's 19860A digital waveform storage option supplies completely automatic time domain measurements. Using microprocessor within the scope, it acquires, stores, and displays signals, and can then output parameters to computer

Programmable waveform acquisition and digital storage are obtained by adding the model 19860A digital waveform storage option to the model 1980 oscilloscope measurement system. This combination, devised by Hewlett-Packard Co, supplies completely automatic time domain measurements, reducing measurement time and improving reliability by eliminating operator involvement.

Using the microprocessor within the scope system to control digitizing, scaling, and input/output, the storage option adds performance and provides versatility. The combination can automatically acquire, store, and display a signal and then output its parameters to a computer. It can also accept waveform data from a computer and display waveforms on its CRT.

The option adds a high bandwidth (narrow aperture) sample and hold circuit, a 10-bit A-D converter, data storage and display memory, display DACs, and control logic to the basic 1980 oscilloscope. When installed, it becomes an integral part of the scope in hardware integration, operation, and functions performed.

Data are acquired using both single-shot and repetitive sampling techniques. In repetitive mode, a signal is sampled at different times on successive sweeps by a narrow aperture sample and hold circuit. An A-D conversion is made and data are loaded into memory. Repetitive sampling at sweep speeds from 999 μs/div to 5 ns/div allows signals to 100 MHz to be captured with time resolution as low as 100 ps between data points. At sweep speeds slower than 1 ms/div, the instrument automatically switches to single shot mode. Minimum time between data points is greater than 20 μs as determined by the maximum of 501 points for 10 horizontal divisions. In single shot mode, sampling starts when the signal is triggered.

Cursors may be activated on each stored waveform with voltage or time values of their positions displayed on the CRT. With one cursor active on a waveform, a voltage value relative to the center horizontal graticule line is displayed, and a time value representing the time from the start of main sweep to the cursor position is displayed. With two cursors active, time and voltage between the cursor positions are displayed. Cursor position may also be read or set by a computer.

Measurement efficiency is increased by automating time domain measurements. The measurement system has continuous calibration in both horizontal and vertical axes. Coupled with continuous calibration is the ability to automatically select the number of acquired data points for the best relationship between signal resolution and acquisition time for each measurement.

To further reduce total test time, data transfer over HP-IB can be selected in either ASCII or binary format. In ASCII, 6 bytes/data point are transferred; in binary, only 2 bytes/point. This allows optimum choice between transfer and computation time.

Where operator interaction is desired, automatic operation improves efficiency by eliminating operator setup time and possible errors. A computer can send reference waveforms to the digitizer, set up front panel controls for each test, and write text on the CRT to direct an operator through a test or adjustment procedure. Without a computer, the instrument can be used as a traditional oscilloscope. Frequently used front panel setups can be saved in eight local registers and recalled to reduce measurement time.

A plot/sequence feature ROM for use with the unit, model 19811A offers a way of obtaining records of waveforms and

(continued on page 110)

MITSUBISHI SETS NEW STANDARDS FOR DISK DRIVES

It's harder today to specify the drive your system may need than it may have been only a year ago. Why?

So many manufacturers have marketed the "perfect" drive. More models and styles. But somewhere along the way something was lost. In many instances, the disk drive became just *another* mechanical assembly.

What makes a MITSUBISHI Disk Drive different? The operating efficiency, reliability, and cost-performance ratios are never taken for granted in a Mitsubishi Disk Drive, or any other high-technology product that carries with it the Mitsubishi tradition of quality and integrity. These are the standards OEM's have waited for.

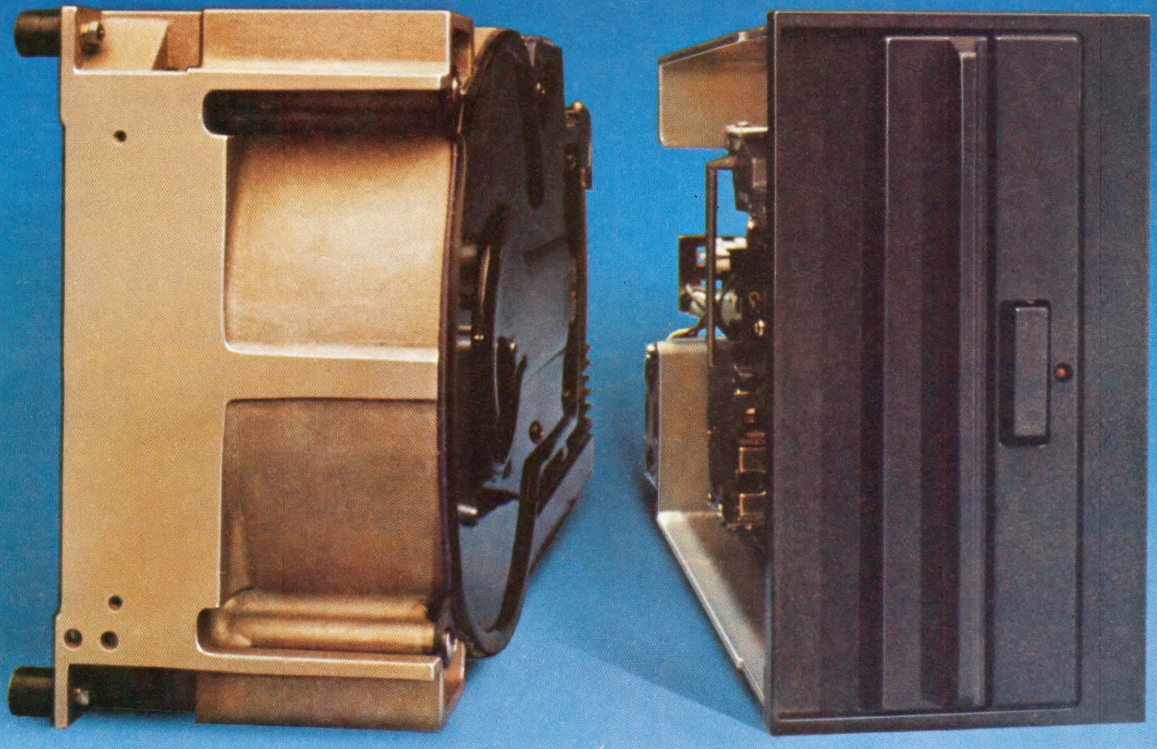
For example, the M2894 8″ Double-sided, Double-density Flexible Disk Drive: filled with more than interface compatibility and interchangeability with a Shugart SA85OR. Or, Mitsubishi M2860 Series 8″ Fixed Disk Drives with 21.73 or 50.71 MB capacity. Again interface compatible with SMD, Shugart and ANSI.

In each, Mitsubishi innovations abound. On the M2894, carefully engineered positioning of the stepper motor to prevent media damage or disk expansion, and SOFTOUCH,™ a proprietary head-loading design that minimizes media wear. And, on the M2860 Winchester drive, high stability, anti-vibration design is inherent. A Mitsubishi LSI- microprocessor based system performs RAS functions equal to a 14-inch unit. Together, mechanics and electronics join for maximum operation reliability.

NEW 5¼″ MODELS

Now, ready for OEM consideration, are Mitsubishi's new 5¼″ Mini-Flexible Drives. And, there are three new 5¼″ Fixed Disk Drives from 3.3 to 10 Mbytes, too. How will these new Mini-Drives fit? Perfect interchangeability!

Call your nearest Mitsubishi Computer Peripherals Representative or write for complete specifications and technical manuals. Whatever the size of your application, let our standards join yours on the bottom line issue . . . Reliability.



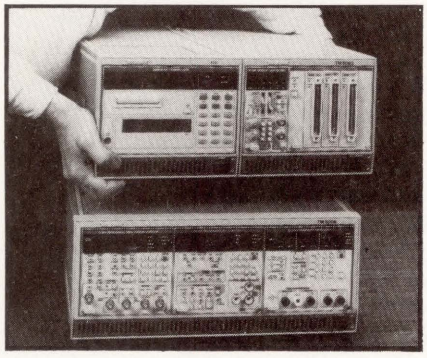
MITSUBISHI ELECTRONICS

MITSUBISHI ELECTRONICS AMERICA, INC.
COMPUTER PERIPHERALS DIVISION
2200 West Artesia Blvd., Compton, CA 90220 (213) 979-6055
Eastern U.S. (617) 938-1220

making repetitive measurements with or without a computer. This ROM contains a plot program that transfers stored waveform information directly to a listen-only plotter. A sequence program stores sequences of front panel keystrokes that can be implemented by pressing a key on any of the HP 10080 series probes. Productivity is improved by programming repetitious measurements, eliminating setup errors, and reducing test time. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 262 on Inquiry Card

Modular system automates testing of IEEE 488 instruments



Compact IEEE 488 test and measurement instruments. Designed to simplify system integration and software tasks, TM 5000 series instruments operate with 16-bit microprocessor based computer/controller optimized for test and measurement instrumentation control. Series includes counters, function generators, digital multimeters, and power supplies

Carrying the modular concept of instrumentation introduced with the TM 5000 series into its second generation, these IEEE 488 bus compatible instruments were designed from the ground up to simplify system integration and software tasks. In the system, Tektronix, Inc, incorporated an instrument oriented controller at the system level to overcome differences in command structures that are encountered when integrating IEEE 488 compatible instruments. Modular TM 5000 fully programmable IEEE 488 instruments, switching and control devices, and controller simplify system integration, software development, and daily operating tasks, and speed operation through the use of standard codes and formats, a high level command structure, and advanced diagnostics.

All instruments are microprocessor based and fully IEEE 488 compatible. Every front panel capability—even features like ac-dc coupling and trigger level on counters or external trigger slope selection on the function generator—is fully programmable via the IEEE 488 bus. Common to all of these instruments, and unique to the series, is the ability to read the bus address setting from any instrument's display by pressing a button on the unit's front panel. In addition, all instruments, when powered-up, go through an extensive self-test and diagnostic routine to check the condition of ROM, RAM, I/O, and functionality of other blocks.

Both physically and electrically optimized for test and measurement systems, the 4041 controller uses the 16-bit Motorola 68000 microprocessor with up to 160k of RAM, and provides up to four I/O ports (both IEEE 488 and RS-232), built-in tape cassette drive, alphanumeric display, thermal printer, and soft keys. The controller features enhanced BASIC language, eight character variables, named subroutine capability, line names, several data types, bus management commands, high speed DMA, and I/O optimization. It is available in either an execute only version, where users cannot access the program, or in a program development version for flexible programming use. In package size and styling, it fits with the instruments and can be joined to the 3-compartment mainframe for rack-mounting as a single unit.

The FG 5010 20-MHz function generator was designed to function as audio oscillator, rf generator, pulse generator, stepped sweep generator, ramp generator, signal regenerator, and low current power supply. Providing stimulus via sine, square, pulse, triangle, and ramps with amplitude or frequency modulation, it is optimized for superior waveform capability, especially in trigger, gate, counted burst, or phase lock modes. Output amplitude is programmable from 20 mV to 20 V peak to peak from 50 and offset from 0 to 7.5 V. It uses an error correction circuit to maintain frequency accuracy within 0.1%. A 350-MHz programmable counter/timer, the DC 5010 features high resolution and autotriggering for adaptation to different signals. Trigger level can be set automatically or to an absolute voltage level. Functions include rise/fall time, width, and several totalizing modes.

A probe compensation function and built-in test signal provide users with a means of compensating the high input impedance probe to the counter without disassembling the instrument. A null feature removes any time differential mismatch, resulting in display of true time interval at the end of the probe tips.

Digital multimeter DM 5010 features true rms ac capabilities and extensive math power for local processing before shipping final information over the bus. In addition to measuring dc voltage, true rms ac voltage (ac or dc coupled), and resistance, it includes a diode test function that forces a 1-mA current and measures the resulting voltage drop. A basic 0.015% dc accuracy 4½-digit instrument, it can also deliver 26 readings/s with 3½-digit resolution. Math capabilities include a null feature to zero out lead resistance in ohms measurements or provide a quasi-differential voltage measurement capability.

Designed to furnish commonly used positive, negative, and logic supply voltages from a single unit, the PS 5010 triple power supply provides programmable 0 to 32 and 0 to −32-V floating supply with 4.5 to 5.5-V logic supply. It continuously monitors all three supplies and can report to the controller if any goes from voltage to current limiting.

All instruments are modules designed to plug into either the full width TM 5006 (6-wide) or half width TM 5003 (3-wide) power mainframes. Both mainframes supply all operating power each instrument or module requires, as well as the IEEE 488 bus interface. Mainframes lock together for stacking or hand carrying and fit into a standard industrial rack. Users can mix TM 5000 programmable instruments and existing TM 500 non-programmable instruments in the same mainframe.

Estimated U.S. base price of several modules are FG 5010, $5200; DC 5010, $3600; DC 5009, $2200; and DM 5010, $1995. The triple power supply is priced at $2500, the TM 5006 mainframe at $950, and the 4041 controller at $4995. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

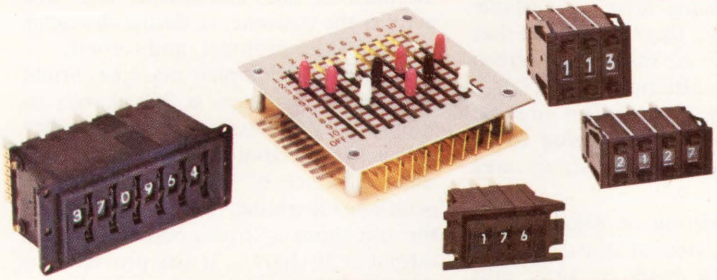
Circle 263 on Inquiry Card

Take your pick from this CHERRY crop of fine products:

PRECISION SWITCHES

Whatever you make . . . you can make it better with a Cherry switch. Cherry snap-action switches are designed with a unique coil spring mechanism for longer mechanical life. Vast choice of sizes, operating forces, mountings, termination and actuators with electrical ratings from 1 through 25 amps. Gold crosspoint contact switches for low energy circuits, too.

Phone: 312/689-7700
. . . or circle reader service number 000



SELECTOR SWITCHES

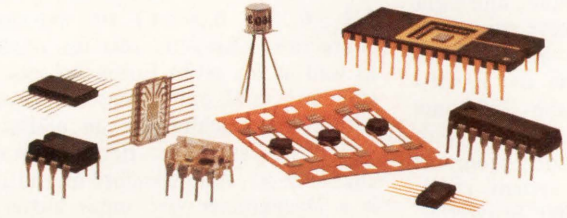
When you need a switch to count . . . count on Cherry. For thumbwheel, leverwheel and pushwheel switches in a full range of alphanumeric readouts and output codes. Full range of sizes, too. And, for matrix selector switches with up to 2784 crosspoints . . . standard and stocked.

Phone: 312/689-7701
. . . or circle reader service number 000

KEYBOARDS & KEYBOARD SWITCHES

Solid state . . . hard contact . . . or membrane? Cherry provides a broad range of custom designed keyboards in your choice of "any of the above" technologies. Plus, numerous standard keyboards available off-the-shelf . . . including the versatile, modifiable 67-key PRO. Many keycap colors, shapes, sizes and legends to choose from. Keyboard switches, too.

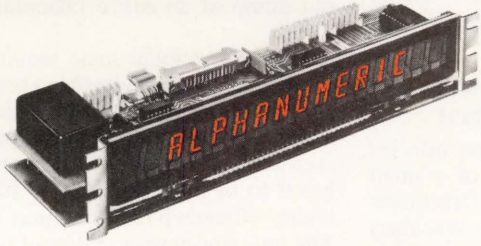
Phone: 312/689-7612
. . . or circle reader service number 000



INTEGRATED CIRCUITS

Need a custom bipolar IC? Take your pick of linear or I^2L digital . . . or a combination of both on the same chip. Cherry designed tooling or your own. Semi-custom and standard ICs, too.

Phone: 401/885-3600
. . . or circle reader service number 000



DISPLAY PRODUCTS

A 16 character alphanumeric display system with microprocessor controlled circuitry for less than $90.00 in production quantities is only one of Cherry's cost-effective applications of gas discharge display technology. Also offered are numeric and alphanumeric display panels and systems for virtually any application.

Phone: 312/689-7731
. . . or circle reader service number 000

Call Cherry...or your Cherry Distributor

CHERRY®

CHERRY ELECTRICAL PRODUCTS CORP.
3614 Sunset Avenue, Waukegan, IL 60085 • TWX 910/235-1572

Worldwide affiliates and phone numbers: Cherry Semiconductor Corp., East Greenwich, RI, U.S.A., 401-885-3600 • Cherry Mikroschalter GmbH, Auerbach, Germany, 09 643 181 • Cherry Electrical Products Ltd., Harpenden (Herts) England, (05827) 63100 • Cherco Brasil Industria E. Comercio Ltda., Sao Paulo, Brazil, 55 (011) 246-4343 • Hirose Cherry Precision Co., Ltd., Kawasaki, Japan, 044 933 3511

CIRCLE 70 ON INQUIRY CARD

Color raster display joins graphics terminal family

A 19″ (48-cm) raster scan color display terminal that supports local picture segments, 2-D transforms, zoom and pan, and up to 4 bit planes of display memory has been added to the Tektronix 4110 series. The 4113 uses a 60-Hz noninterlaced scan to eliminate flicker, even for displays with large areas of a single color. In addition, the 3 standard bit planes allow use of 8 colors simultaneously. An optional 4th plane increases this number to 16.

The 4113 maintains compatibility with the rest of the 4110 family, including the 4112 monochrome raster display and the 4114 high resolution storage tube system. Image data can be stored in a 4096 x 4096 addressable display space and displayed on the screen as 640 x 480 pixels. The display's zoom feature does not use the pixel representation method in which lines become thicker as the image is zoomed in. Rather, the user can zoom and pan the actual data in display memory through the 640 x 480 window.

Minimizing traffic with the host is of primary concern. Sustained communication rates of 9600 bits/s are utilized; alternately, the user can select independent receiving and transmitting rates via the RS-232-C interface. A block mode option permits error detection and automatic retransmission of data blocks. Moreover, host and terminal can flag each other when to start and stop transmission to avoid overflowing the input queues.

Local intelligence features of the 4113, which include local mass storage with 2 double-density 8″ (20-cm) diskettes, allow a great deal of graphics data to be manipulated independent of the host computer. To communicate with the host while working with the display data, the user may define a dialog area on the screen and an associated buffer in memory. The dialog area is scrollable with the terminal's thumbwheels so that the user may define a fairly small screen area for communications and associate it with a relatively large buffer area in memory. This allows the dialog to be reviewed without excessive screen area clutter.

Memory, consisting of 88k bytes of ROM and 32k bytes of RAM, can be expanded to 800k bytes of RAM, thus providing ample storage room for local picture segments. These picture segments can be manipulated, scaled, rotated, and redrawn at any time by recalling them from memory. Frequently used segments, such as titles and symbols, can also be stored on disc and dynamically loaded into memory when needed.

The 4113 is also designed to work with a number of peripherals, such as graphics input tablets, printers, and plotters. An optional serial interface provides three additional RS-232-C ports. Software supports background spooling and offline plotting functions, and eight programmable function keys allow user definable functions to be tailored to individual applications. The 4113 is software compatible with the Tektronix PLOT 10 graphics software and with existing 4010/4012 applications programs using terminal control system (TCS). **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

—Tom Williams
West Coast Managing Editor

Circle 264 on Inquiry Card

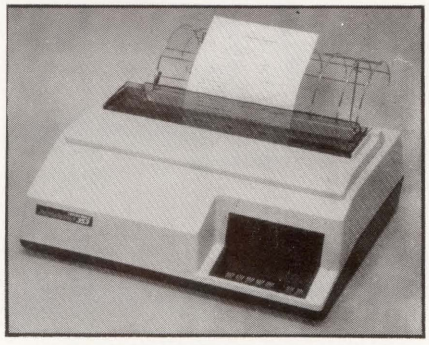
Midrange printers produce both draft and report quality output

Midrange printstation 350 series printers handle all the output needs of a small business computer. Features Centronics has incorporated within the machines should guarantee their acceptance in an office environment.

Printstation units are designed as universal machines, incorporating fanfold, cut sheet, and demand document paper handling systems as standard items. Their power system operates from 50 and 60 Hz, 110 and 220 V, meeting both domestic and foreign requirements. Each machine supplies both RS-232-C serial and Centronics parallel interfaces for further versatility.

The three models initiating the series are the 352, a single-mode draft quality unit; the 353, a dual-mode unit that provides both draft and correspondence quality output; and a bus standard unit that is designed to serve as a building block for value added OEMs. Consisting of cover, power supply, printhead mechanism, and electronics, this unit permits the customer to define character set, interface, protocol, and format.

Model 352, a complete machine, prints single-pass characters at 200 chars/s to supply data processing or draft quality copies. The dual-mode model 353 offers users a choice of single- or multipass printing. Operating in multipass mode, the unit supplies correspondence quality output at 50 chars/s. It also provides pin addressable graphics.



Users of either unit can choose 10-, 12-, 13.2-, 15-, or 16.5-chars/in (4, 5, 5.2, 6, or 6.5/cm) or expanded characters. Character sets for USASCII, as well as for seven European sets, are standard on all units. Space is provided within the machine for an additional 96-character user programmable character set. Also standard on the units is a 2k-character FIFO input buffer. A 4000-character buffer in the multipass model provides sufficient storage to permit dump of an entire 132-column CRT screen.

The bidirectional logic seeking print mechanism uses an improved printhead. Incorporating redesigned pole piece and armature, the 9-wire head exhibits more standard characteristics, permitting heads to be interchanged and supplying higher efficiency than previous models. The operator-changeable head prints on a 7 x 8 matrix using 8 pins; the ninth pin is reserved for underlining, ensuring that the underline is distinct from descenders on the characters.

Adhering to the "one printer solution" concept, the machines satisfy the needs of data processing with draft quality, business processing and forms

(continued on page 114)

Up front graphics backed by up front support.

In the computer graphics industry, back-up product support is too important to leave as a back-up thought. So CalComp puts the most comprehensive product support package available in front of all CalComp products.

Including the CalComp Vistagraphic display terminal systems. Each Vistagraphic display — six models for your CAD/CAM needs — is covered by the CalComp exclusive one-year warranty on parts and labor.

Call CalComp early in your planning to provide timely product information and advice to help you increase productivity. And with the largest team of systems analysts, sales consultants and field engineers, we'll put your system on-line fast and keep it operating at top condition.

Vistagraphic power backed by system flexibility.

Vistagraphic display systems easily handle CAD/CAM tasks, as well as seismic studies, mapping, process control and simulation. Special graphics requirements such as multiple station operation and distributed graphics are managed economically with the Vistagraphic's high performance terminal controller.

For maximum system flexibility, Vistagraphic Series 1000 systems with stroke refresh technology and raster Vistagraphic Series 3000 systems are software compatible. Plus, both series can provide color for better presentation.

Get full graphic support now.

Look to CalComp Vistagraphic display terminal systems for the kind of comprehensive graphics — and up front support you need now. Contact your nearest sales consultant today.

CALCOMP
A Sanders Graphics Company
SANDERS

California Computer Products, Inc., 2411 W. La Palma Avenue, Anaheim, California 92801 • (714) 821-2011

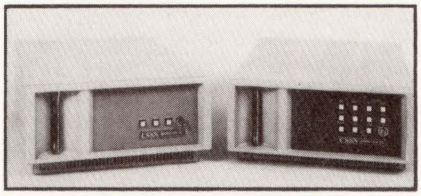
CIRCLE 71 ON INQUIRY CARD

handling capability, and word processing with the high quality matrix print. The unit's paper handling system allows the use of both continuous fanfold and single-cut sheets. Waste on continuous forms is eliminated by the ability to consistently tear off the form 1″ (2.5 cm) below the last printed line. The single-sheet feed mechanism guarantees accurate loading of cut sheets up to 14″ (36 cm) by simply inserting the sheet and letting the machine do the rest. Adjustable tractors accommodate fanfold forms up to 15″ (38 cm) wide. Front panel controls handle mode selection, form and line feed, line spacing, character pitch, and other format choices. Communications occur at 16 rates between 50 and 19,200 baud, using XON/XOFF, reverse channel, and DTR protocols. **Centronics Data Computer Corp,** One Wall St, Hudson, NH 03051.

—Peg Killmon, Senior Editor

Circle 265 on Inquiry Card

Database machines separate database and processing functions



Dispatch 10 database machine (left) is intended to be delivered preprogrammed to user. Dispatch 20 (right) adds all software necessary to develop custom file management applications and can be used to program model 10

An architectural approach to database technology claims to break through database cost barriers and permit database technology to be treated as a separate system function. Dispatch™ series database machines take advantage of microprocessor and disc technology advances to combine database processing and management into a single function unit. The unit attaches to most minicomputer or mainframes through a communications routine on the host.

During the past decade and a half, more and more data files and programs have exceeded the capabilities of small computers. This has left the user with two alternatives—moving up to more sophisticated hardware and software, or custom-designing file management for each application. Both options are costly and time-consuming, and require repetition of efforts each time a group of files is created. Another seemingly viable alternative has been to separate the database function from the processing function to create a separate database machine (DBM). Although this solution offered the benefits of few changes in the host configuration and minimal drain on host resources, until now it has been considered too expensive for OEMs and small systems integrators.

In its simplest form, Dispatch can be viewed as an intelligent disc machine. It receives a data request from the host for the storage/retrieval of a data item in some logical order within the data base. In the case of a query, for example, rather than present the host with each data item until the correct position is found, it performs the logic and returns only the requested information to the host. An integral cartridge tape drive backup capability saves each data base using the BackUp™ tape utility. As an option, the recovery/transaction log copies each transaction to the tape as it is made.

(continued on page 116)

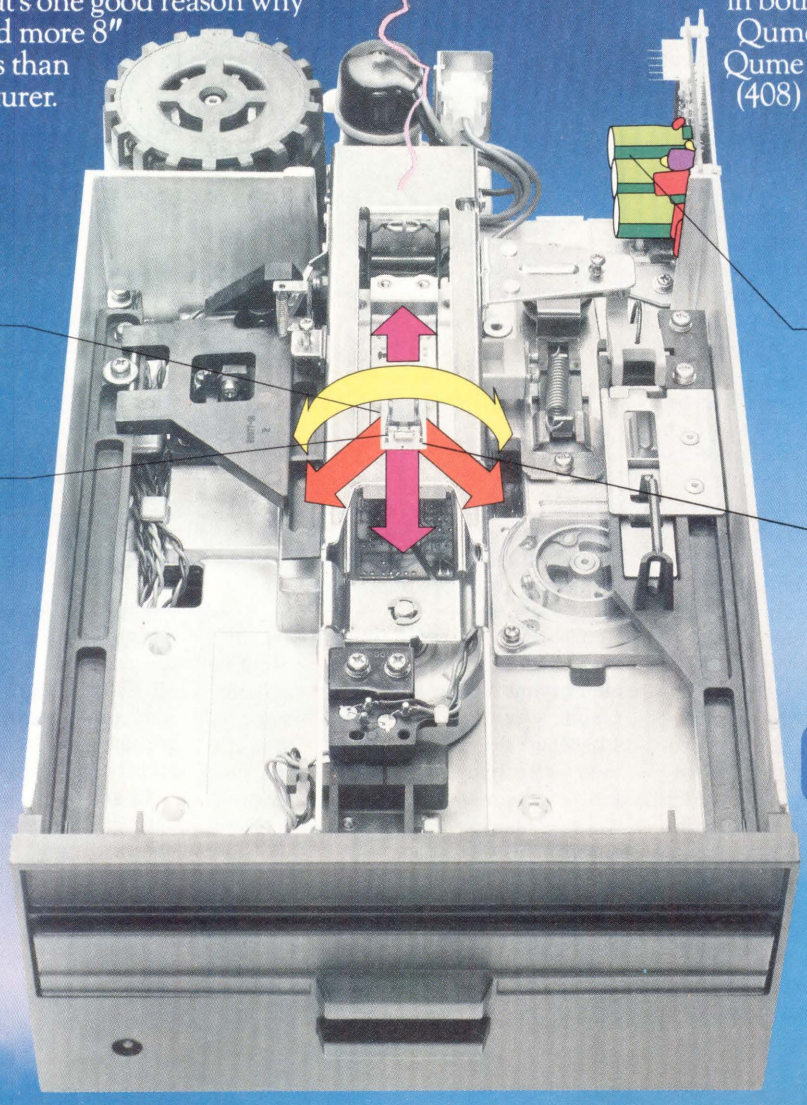
QUME

AC

For standard AC floppy drive applications, nothing beats QumeTrak 842. Our exclusive TriGimbal™ design heads glide smoothly over the disk surface for the gentlest media ride in the business. That's one good reason why QUME has installed more 8" double-sided drives than any other manufacturer.

DC

For special battery-backup or overseas installations, you get the same smooth media treatment from the QumeTrak 842DC drive. For more information about the gentlest, most reliable floppy disk drives in both AC and DC, call or write Qume Product Marketing, Qume Drive, San Jose, CA 95131. (408) 942-4000



ROLL, PITCH and YAW: TriGimbal head rotates on three axes for smooth ride.

TAP TEST: Qume beats industry standard 100,000 impacts to 25,000 impacts.

TWO VOLTAGES: +12 and +5 volts DC. No negative voltage required.

CONTINUOUS CONTACT TEST: Qume beats industry standard 10 million passes to 3 million passes.

Qume®
A Subsidiary of ITT

CIRCLE 73 ON INQUIRY CARD

The system allows the systems integrator to configure the right database machine for the application. As the amount of data to be managed grows, the disc cache facility can be increased to speed access. Additional processors can be added without changing the structure of the data base as the number of directly connected hosts or users increases. More storage capacity can also be added.

When configuring remote database machines, communications to the host can be handled by a task processor running a high level data communications protocol. This means that a group of users can locally use and maintain a data base and still have data available to a host at a remote location.

Of the available systems, the Dispatch 10 is intended to be delivered preprogrammed by an OEM systems house. This system incorporates a Z80 processor with S-100 bus architecture, 64k-byte RAM, 10M-byte disc with 13.4M-byte tape cartridge backup, two serial ports (host/diagnostics), standard switch console, and RS-232-C serial interface. Software for this, and all other models, provides a FAST™ operating system (CP/M compatible), a CODASYL database package, communications package, packet protocol, and STP microdiagnostics package. Options include a data recovery package and recovery transaction log (RTL).

Providing all software necessary to develop custom applications, the Dispatch 20 can be used to program the model 10. It includes a 24M-byte disc plus a parallel port, as well as two serial ports and a full system console. An assembler, program editor, linking loader, and debugger are added to the basic software package. FORTRAN or COBOL serve as standard host/development languages; PL/1 and C are available as options. Recovery transaction log and data recovery package become standard parts of the software system. A query/report writer is offered as an option.

The Dispatch 30 upgrades database support with a memory mapping processor and incorporates the software of the model 20. Standard hardware on this system includes a 45M-byte disc and 128k-byte RAM. However, the Z80 processor includes memory mapping capability made possible by Stretch 1000™, a combination of proprietary hardware and systems software. Using this, the system provides data access that is 5 times faster than that of the smaller systems. In addition, four serial ports and one parallel port are provided. This system expands to 1M-byte RAM and supports up to 16 disc drives.

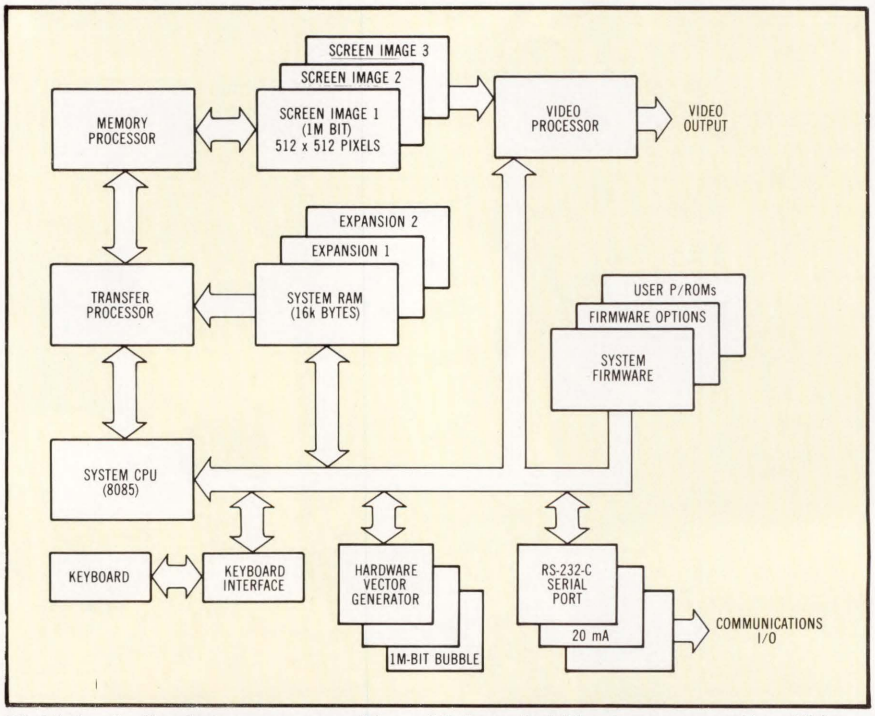
Providing a multiprocessor operating system with access to a data base through several processors, Dispatch 50 permits more than one host to access one or more data bases. Hardware for this system includes two task processors, each containing a Z80, and each with 64k-byte RAM and a serial port. Up to 16 task processors and 16 drives can be added, and system memory expands to 2M-byte RAM.

Proprietary software allows the Dispatch 100 to act as a standalone system as well as a backend host connected database machine. In a 4-station cluster, for example, hardware includes a database management processor, four task processors, four terminals with high speed dot matrix printers, plus an operational terminal. Functions can be used on a mix and match basis to yield considerable flexibility. This system offers a 45M-byte disc and 384k-byte RAM that expands to 2M bytes. Software for this machine provides a query/report writer as standard.

Dispatch 10, 20, and 30 are currently available at prices ranging from $9995 to $23,850. Dispatch 50 and 100 are scheduled for delivery in January at single-system prices of $27,995 and $41,195. **Computer Service Systems Network Inc,** 582 E St, Boston, MA 02210.

Circle 266 on Inquiry Card

Bubble memory mass storage fits graphics terminal to rugged uses



Multiple pipelined processors combine with large bubble storage capacity within Industrial Data Terminal's 220 terminal to rapidly execute functions on a single command from the host computer

Replacing the traditional floppy disc mass storage devices with a bubble memory module adapts the IDT 2200 color graphics terminal to use in airborne and seagoing environments. This allows the high performance provided by the ruggedized color graphics display terminal to be applied in additional applications requiring large capacity and long-term, maintenance-free operation.

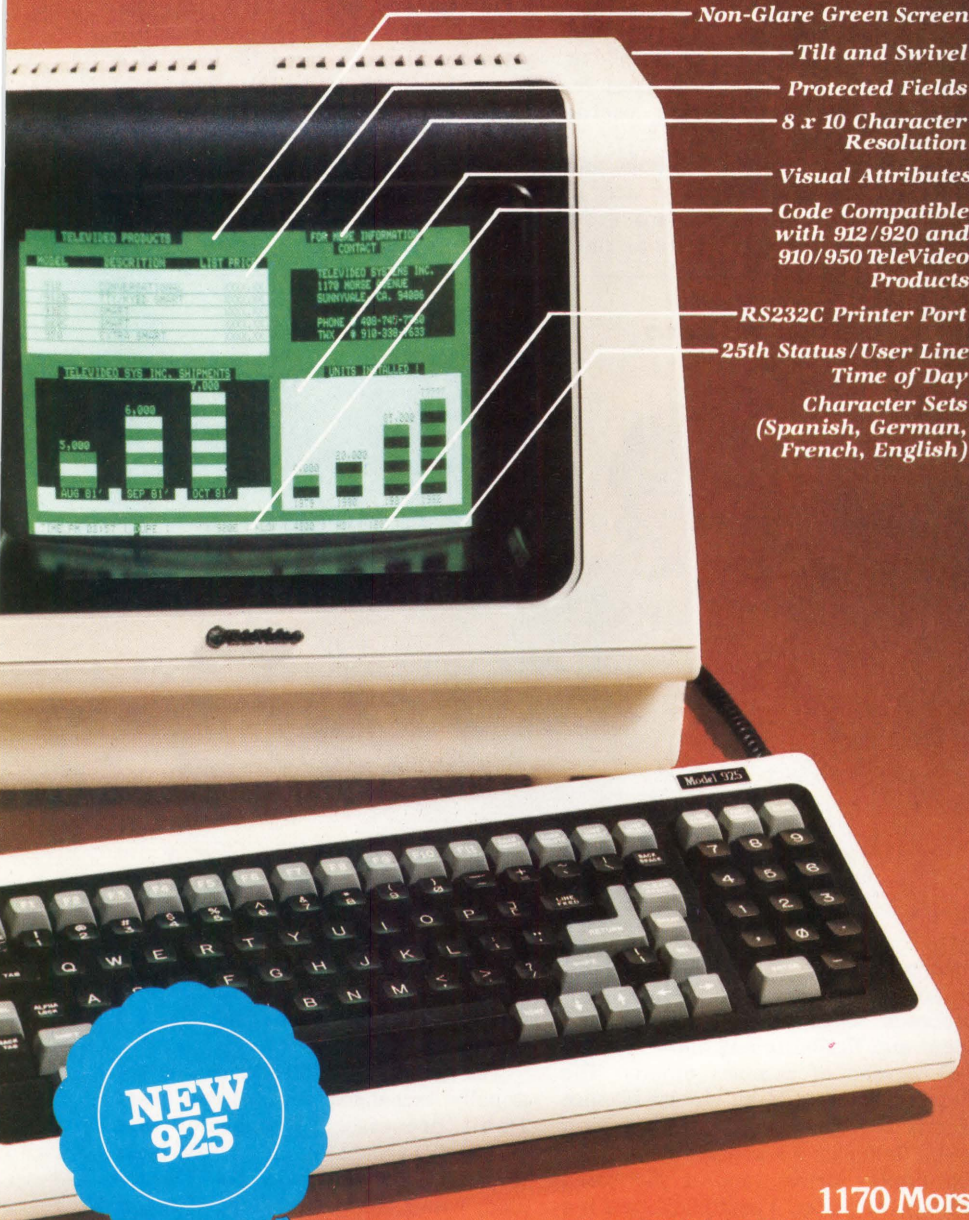
The bubble storage system is based on an Intel 7110 magnetic bubble memory chip, capable of storing 1M bit of data, and support chips that provide memory control and timing functions. Solid state design and low component count make the compact system more reliable than electromechanical devices or other semiconductor memories. Maintenance consists of exchanging modules when and if repairs are indicated.

In addition, the device expands product specifications in operating temperature range, air pressure, humidity, air quality, and shock and vibration. Because the device is completely nonvolatile, no battery backup is required to protect data when power is lost or the unit is switched off.

(continued on page 118)

The Performance Leader....

Model 925



Now you can have it all with TeleVideo's new 925. Code compatible with our 910 and 950 terminals, the 925, with its 6502 microprocessor-based control board can emulate our 912/920 models while operating at speeds up to 19.2K baud. This allows you to grow within the TeleVideo family of terminals, from the conversational to the smart.

The 925, a modular designed unit that uses the same power supply, monitor, and keyboard as the rest of TeleVideo's family, has built-in *proven* reliability and quality from beginning to end. TeleVideo's P31 non-glare, tiltable, green screen and detached selectric style keyboard make the 925 a comfortable, low stress terminal to use.

They offer you options; we give you standard features like RS232 printer port, X-on/X-off control, 22 function keys, user line, 25th status line with setup mode, local duplex edit modes, and many more.

Nationwide service is available from General Electric Company Instrumentation and Communication Equipment Service Centers.

Contact TeleVideo today for information on the Performance Leader, the 925!

NEW 925

TeleVideo®

TeleVideo Systems, Inc.

1170 Morse Avenue, Sunnyvale, CA 94086
408/745-7760; 800/538-8725 (toll-free outside California)

The Value Leaders

CALIFORNIA Santa Ana (714) 557-6095 • Sunnyvale (408) 745-7760 • MASSACHUSETTS Boston (617) 668-6891
NEW YORK/NEW JERSEY Morris Plains (201) 267-8805 • TEXAS Dallas (214) 980-9978
ILLINOIS Bloomingdale (312) 351-9350 • GEORGIA Atlanta (404) 255-9338
EUROPE London 44-9905-6464

CIRCLE 74 ON INQUIRY CARD

Used in the 2200, the memory allows permanent displays to be retained within the terminal and ensures data integrity even in the harshest environment. Bubble memory unburdens the host computer of memory requirements and dramatically reduces transfer time to the terminal. With its 1M-bit capacity, it allows an entire library of pictures and subpictures to be built and stored within the terminal. Moreover, its speed provides rapid reliable display.

For high performance graphics, the terminal itself supplies 512 x 512 individually addressable pixels and displays 85 characters on 51 lines. In addition, the unit has eight standard colors, provides two character cursors and a graphics cursor, and has built-in diagnostics. The unit's proprietary features are made even more effective by the provision for compatibility with PLOT 10 software; a hardware vector generator that draws vectors 10 times faster than before; and a front access design that permits easy maintenance and supplies room for three full-color display memory planes.

A highly reliable, rugged design has led to the unit's acceptance in the steel industry. It is currently undergoing stress and vibration tests to verify its claims to provide long life and low maintenance in industrial environments.

A pipelined hierarchical multiprocessing architecture allows high speed dot writing and macroprogramming manipulation. Intelligence permits programming using simple high-level ASCII commands and macro commands. The terminal's building block approach combines multiple bit slice and high speed Schottkey processors with flexible and expandable memory to provide users the opportunity to select firmware and hardware options to meet specific requirements.

The architecture makes provisions for user defined graphics figures and subpictures with embedded color and location information to be stored within the terminal. They are executed rapidly in response to a single command from the host, relieving the host of having to keep track of the details involved in picture drawing and updating.

MACROGRAPHICS™—user defined freeform graphics that can be stored in RAM or P/ROM—give the user the ability to create any figure, any size, with or without embedded color, and to rotate or provide mirror images, all under terminal control. RAMPICS™ are file programs stored in RAM within the terminal that create or execute complete pictures with a single command; BUBBLEPICS™ use the bubble device's greater storage capacity for creation of complex displays with simple programming. These include animation when combined with MACROGRAPHICS.

The unit is also capable of generating absolute solid vectors and relative solid vectors, and providing a bar graph generator that produces solid or patterned bar graphs. Optional functions include programmable patterned vectors, complex polygon fills, programmable area color change, patterned fills, high speed image dump by pixel, solid or patterned circles, 8-pen strip chart recording, and a hardware vector generator.

Screen images, special symbols, and control functions are transmitted in ASCII format over the standard RS-232 serial interface. Communications rates are selectable up to 19.2k baud. Options include parallel ASCII I/O, binary communication, PLOT 10 compatibility, and 20-mA current loop.

Consisting of video generator, 19″ (48-cm) color graphics monitor, and multifunction keyboard, the system is available as a packaged desktop cabinet, 19″ rackmount, or OEM unit. Base price for the 2200 terminal is $11,495. A 1M-bit bubble module sells for $3500; 2M bits cost $4900. The hardware vector generator increases speed 10 times, at a cost of $1250. **Industrial Data Terminals Corp,** 173 Heatherdown Dr, Westerville, OH 43081.

—Peg Killmon, Senior Editor

Circle 267 on Inquiry Card

Graphics system combines high speed display processors with CP/M controller

Incorporated in the IMI-500 advanced graphics display system, is a multiprocessor scheme designed to increase speed and flexibility and allow realtime 3-D viewing of complex objects. The system includes a 24-bit bipolar bit slice display processor, which incorporates a 24-bit floating point processor, a bipolar LSI display driver, and a Z80 based display controller. The display itself is a 21″ (53-cm) calligraphic stroke type with a resolution of 4096 x 4096 points.

The Z80 display controller with 60k bytes of memory is used for handling communications with the host computer, accepting input from the keyboard, and running the CP/M operating system to control local mass storage. In addition, the controller reduces incoming graphics commands and accepts floating point data and FORTRAN real numbers for later processing by the display computer. Communication with the host is via an RS-232 serial link or a DMA interface.

The Z80 display controller can be optionally exchanged for an 8086 based 16-bit processor. Winchester disc storage is available in either 10M bytes (8″, 20 cm) or 26M bytes (14″, 36 cm) along with 2.4M bytes of floppy storage. A graphics editor and various high level languages can be added, including a FORTRAN compiler, a text processor, and a PL/1 compiler with overlays.

The 24-bit floating point processor allows the IMI-500 to directly accept floating point numbers in its input data stream. The display processor, from its 128k-byte memory, pipelines data to the floating point processor. Floating point

(continued on page 120)

7.3 to 83 Megabytes

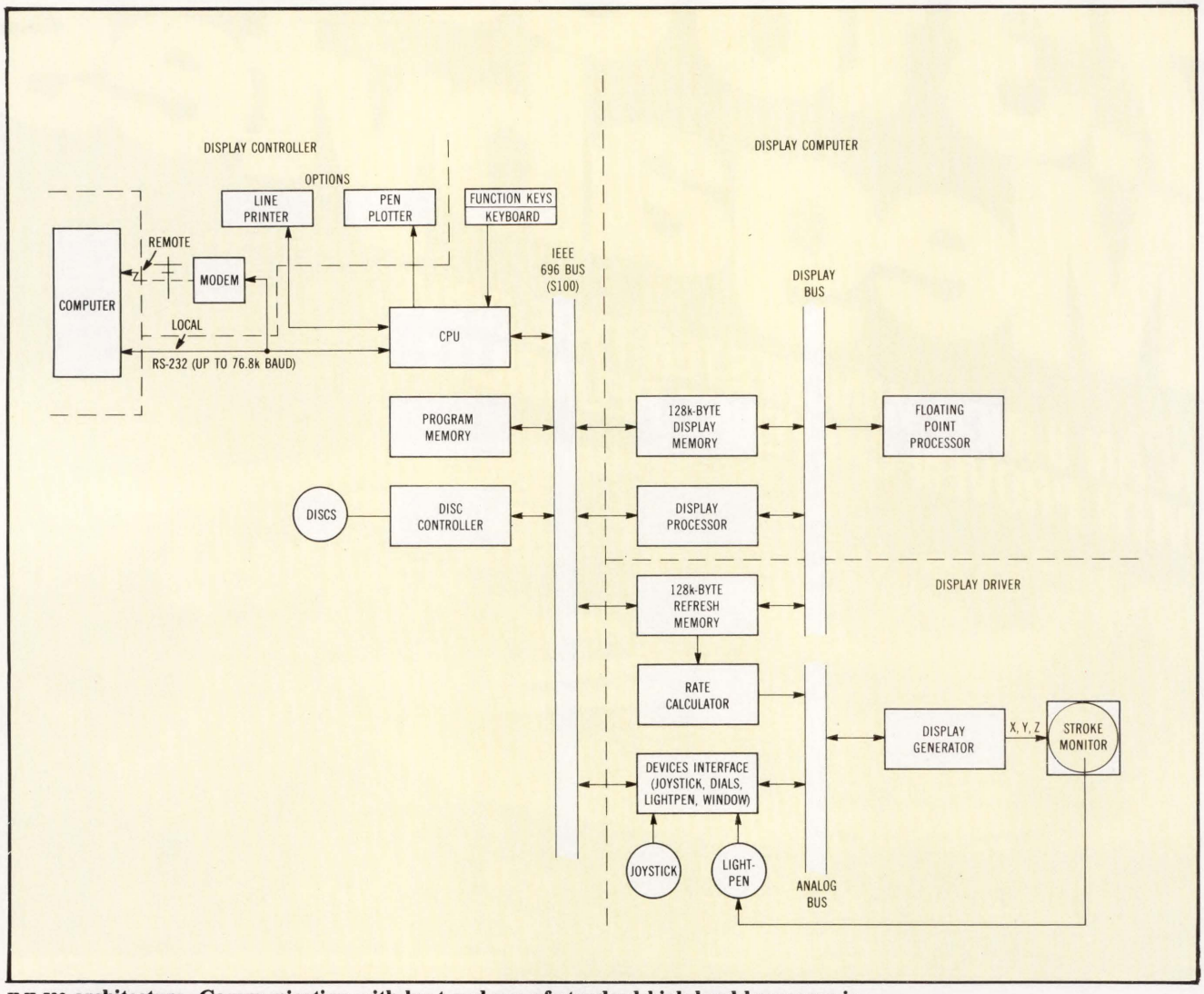
IN AN 8-INCH WINCHESTER-TYPE DRIVE WITH PROVEN CHEYENNE RELIABILITY

- ANSI, SMD and FLOPPY interfaces.
- Capacities of 7.3, 22, 36.7, 52 and 83 megabytes.
- Closed loop track following positioning system with rotary voice coil positioner.
- Daisy chain control with option for up to 8 drives.
- Microprocessor-based modular electronics package; can be remotely operated.
- Built-in self-diagnostic program.
- Patented sealed air system.

Making it more reliable
...every bit!

SL INDUSTRIES
21040 Victory Blvd.
Woodland Hills, Calif. 91367 / Phone: (213) 884-7300 / TWX: 910-494-2696

CIRCLE 75 ON INQUIRY CARD



IMI-500 architecture. Communication with host and use of standard high level languages is provided by Z80, CP/M based display controller. Bit slice display processor and floating point processor handle very high speed processing of display vector algorithms

data are converted to integer format after the display algorithms have been computed. Thus, the display processor can perform smooth rotation about any axis, scaling, clipping, and zooming; can vary perspective; and can support multiple viewports.

The 32-bit display driver, which also has 128k bytes of memory at its disposal, can refresh 32,000, 0.2″ (0.5-cm) vectors or 5000 characters at a rate of 36 frames/s. Refresh function is kept independent of any graphics updating performed by the display processor. The system gives a full ASCII character set and will support 154 user defined symbols or characters at any given time. Character size is continously variable as is the scaling of the display itself. **Interactive Machines Inc**, 2500B Townsgate Rd, Westlake Village, CA 91361.

Circle 268 on Inquiry Card

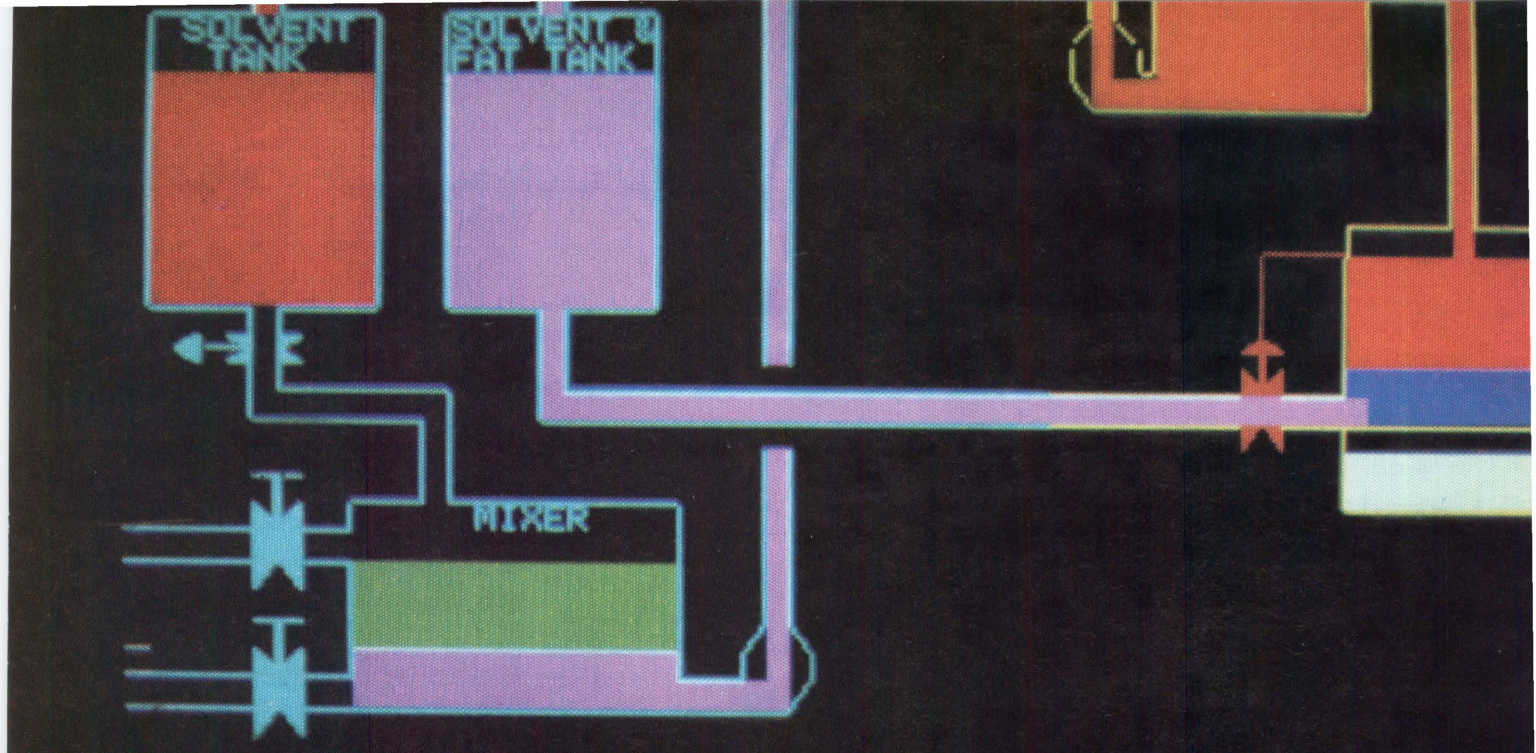
Magnetographics technology serves as basis for low noise desktop printer

A document printer designed for use in shared resource word processing and distributed data processing applications, PXL-6 is compatible with all word processing systems and can print 6 pages/min. The low cost printing system, described by AM International as a breakthrough in office automation technology, features automatic paper and envelope handling, printing flexibility with four typestyles online, and easy quiet operation.

While the majority of current document generators are laser based devices, the PXL-6 uses patented magnetographics technology—a nonimpact toned magnetic image transfer process. This technology enables the printer to achieve significantly higher output speeds, higher reliability, and executive print quality over a wide environmental range. The compact desktop unit operates at a decibel level significantly below that of current daisy wheel printers.

In magnetographic printing technology, the latent image is formed by creating magnetic flux reversals in a magnetic tape or drum, rather than by charging patterns on a dielectric surface. The image is then toned with a magnetic single-component toner. Both toner and application method are similar to those of small electrostatic copiers. Transfer may be done either by pressure or electrostatically. After transfer, both magnetographic and electrostatic image receptors must be cleaned, and the latent image erased prior to re-imaging.

(continued on page 122)



The Intelligent Systems' guarantee:

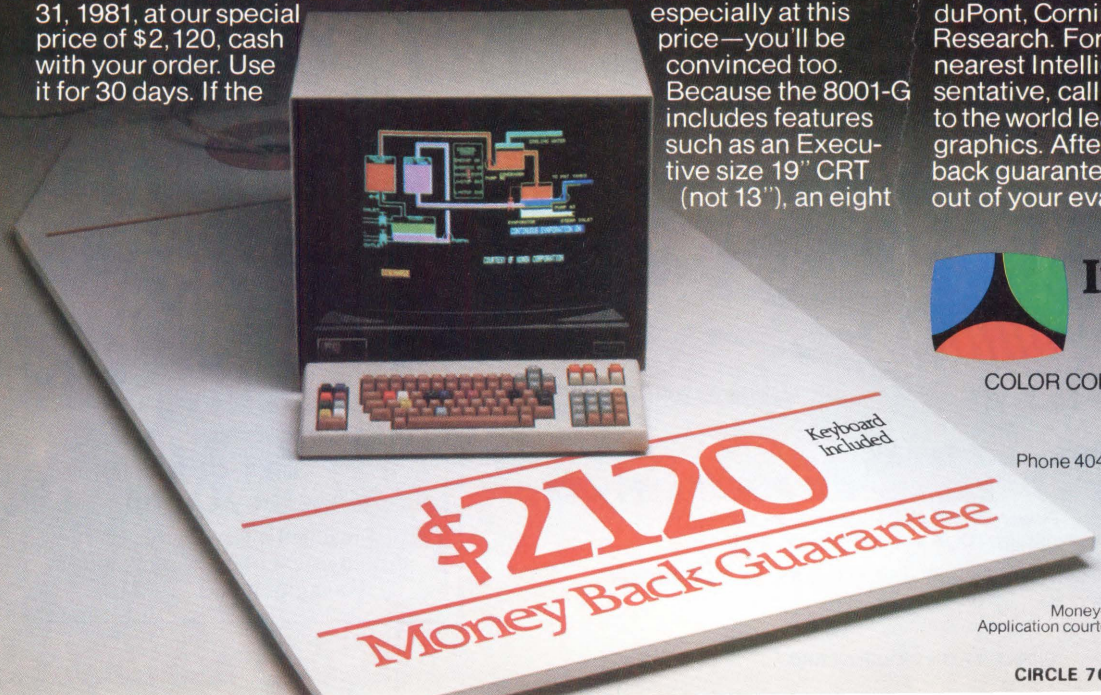
If you don't like it, we'll buy it back.

Leave it to Intelligent Systems to come up with an offer like this. After all, we were the first firm to deliver over 20,000 color graphics desktop computers and display terminals. *Now, we're the first to deliver a factory-direct, money-back guarantee!* And the 8001-G color graphics terminal we are offering is the standard in the process control industry.

Here's how it works: Buy a single-evaluation unit before December 31, 1981, at our special price of $2,120, cash with your order. Use it for 30 days. If the performance, reliability and quality of this unit does not convince you this is the very best value in color graphics terminals, simply return it. And we'll return the purchase price of the unit. It's that simple. If you wish to return the unit, your only cost will be transportation charges to and from Norcross, Georgia.

However, we're convinced you'll keep it. Because once you see the difference that color can make—especially at this price—you'll be convinced too. Because the 8001-G includes features such as an Executive size 19" CRT (not 13"), an eight foreground color, eight background color display... 160 x 192 graphics ... 128 standard characters... 80 characters per line by 48 line format... and an ASCII, 101-key keyboard. Plus, every terminal can easily and inexpensively be upgraded to a full-featured desktop computer!

So, it's sound business to make Intelligent Systems your low-cost one-stop source for color graphics. You'll be joining companies like Johnson Controls, Taylor Instruments, Leeds & Northrup, E.I. duPont, Corning Glass and Chevron Research. For the name of your nearest Intelligent Systems representative, call 800-241-9699. Talk to the world leader in low-cost color graphics. After all, with a money-back guarantee, we take the risk out of your evaluation!



Intelligent Systems

COLOR COMMUNICATES BETTER

225 Technology Park/Atlanta
Norcross, Georgia 30092
Phone 404/449-5961· TWX 810-766-1581

U.S. domestic price.
Unretouched photos of screens.
Money-back offer expires 12/31/81.
Application courtesy of the Xomox Corporation.

CIRCLE 76 ON INQUIRY CARD

In this printer, the write head is made of an etched bimetal foil that uses current confinement in a single conductor to define the write zone. This structure uses high currents, causing heating that is minimized by using very short current pulses. Design simplicity enables use of a very high yield photolithographic fabrication process similar to that used for PC boards. The PXL-6 prints at 240 spots/in (94/cm), but substantially higher density is possible using the process.

While the magnetic tape imaging member has a superficial resemblance to conventional magnetic recording tape, it is a multilayer structure designed to optimize toner holding forces. The imaging tape is a 0.56″ (1.42-cm) wide continuous loop having a circumference of about 30″ (76 cm). In operation, the tape accelerates to a constant speed for the magnetic writing and toning steps. When the toned image is positioned under the paper, the belt is stopped momentarily and brought into physical contact with the paper. A high voltage pulse transfers toner to the paper. The tape is then separated from the paper, again accelerated to a constant speed, cleaned, and magnetically re-initialized. Two impressions of 2 lines each are printed for each belt circumference.

With the exception of the write head and the transfer system, subsystems of the unit are extensions of xerographic technology, modified for a small width imaging member. The toner applicator is based on conventional magnetic brush designs. Its small width and open geometry allow the magnetic field configuration to be tailored to achieve high density images with very low background, giving high toner usage efficiency.

The transfer system is a combination pressure electrostatic system that achieves high transfer efficiency, accommodates a range of papers over a wide environmental range, and permits high quality printing on envelopes.

In addition, the printer is expected to be substantially more reliable than laser scanning systems based on small xerographic copiers. The magnetographic write head has no moving parts and no dirt-sensitive optical components. Humidity and temperature have virtually no effect on the writing process, and the imaging tape is less prone to mechanical damage than a photoreceptor.

The printer has four interchangeable electronic cartridges online. Moreover, the operator can introduce bold, slant, or double-size characters into a document to provide 24 different type fonts at any time. In addition to standard type styles, the unit accommodates variable size fonts from 6 to 24 point, logos, and special graphics characters.

Basic systems are priced at $5000 each in OEM quantities. Type fonts are available for $75 each. **AM International,** Prudential Plaza, 130 E Randolph St, Chicago, IL 60601.

Circle 269 on Inquiry Card

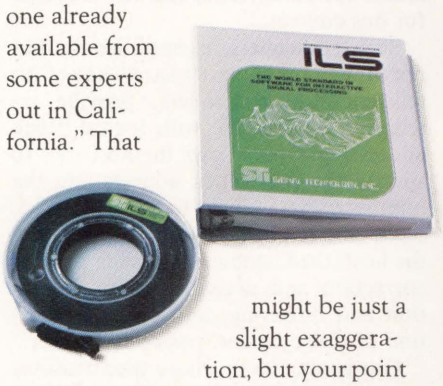
WHY YOU SHOULDN'T WRITE YOUR OWN SIGNAL PROCESSING SOFTWARE.

BY A.H. "STEEN" GRAY, Jr., Ph.D.
Vice President, Signal Technology, Inc.

I've been in this business long enough to know that some things never change. The "make or buy" quandary as it applies to software is a good example. "We've got some expensive programmers; let them earn their keep." How many times have you heard that when you've suggested buying a program package that seems perfectly tailored to your application?

HOW TO ANSWER

If your line of work is signal processing, the answer should be reasonably simple. Just say, "It would take us ten years and a bundle of money to come up with a package as good as the one already available from some experts out in California." That

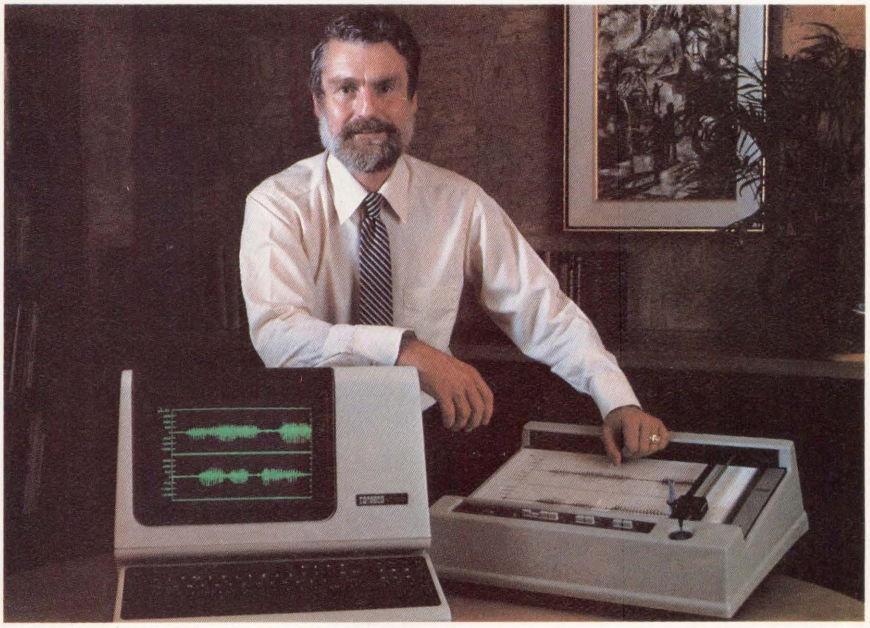


might be just a slight exaggeration, but your point would be well taken. You see, we do have the last word in interactive signal processing software. It's called ILS, and with over 200 installations worldwide, it is often referred to (and not just by us) as the "world standard."

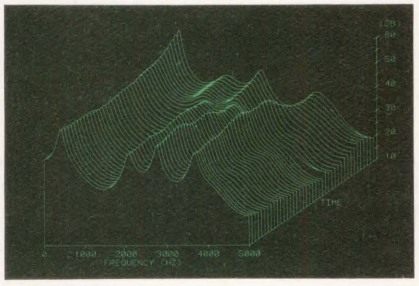
WHAT ILS IS

ILS is a highly modular set of FORTRAN programs that make up a sophisticated interactive software system with standard file structures, documentation and ongoing support. To date, it is performing with excellent results in a wide variety of industries and technologies, including: **speech—noise and vibration—acoustics—biology—medicine—simulation—digital filtering—sonar—radar—seismic—** and some we aren't being told about.

Many of our users also find DACS, our Data Acquisition and Conversion Software, and APAS, our Array Processor Application Software, of great value in their applications.



WHAT COMES OUT



With any compatible computer system and the appropriate terminals, ILS will give you: **pattern analysis—digital filtering—signal editing—3-D displays—modeling—correlation—convolution—spectral density—signal displays—coherence—** and maybe even a picture of your Aunt Sally, if that's what you want.

THE POINT IS

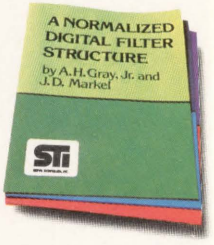
The important thing is, ILS is available *now*. It has been proven in a multitude of applications around the world. And it can cost you a lot less in time and money to buy it from us rather than developing a comparable package yourself.

FREE DEMO

If you have a compatible graphics terminal and modem, we can arrange to give you an on-line demonstration of ILS. Simply call (toll free) and ask for our ILS marketing representative at (800) 235-5787. We also have a video tape that illustrates many of the features of ILS and its capabilities. We'll be happy to send it to you.

IF YOU'RE STILL WITH US

If you've read this far, you probably have some kind of interest in signal processing. I'd be delighted to send you a reprint of the series of three articles on digital filtering that I co-authored with John Markel. Write to me at the address below.



STI SIGNAL TECHNOLOGY, INC.

15 West De La Guerra Street, Santa Barbara, CA 93101
California (805) 963-1552 • **Outside California Call Toll Free (800) 235-5787**
TWX 910-334-3471—SIGNAL TEC SNC

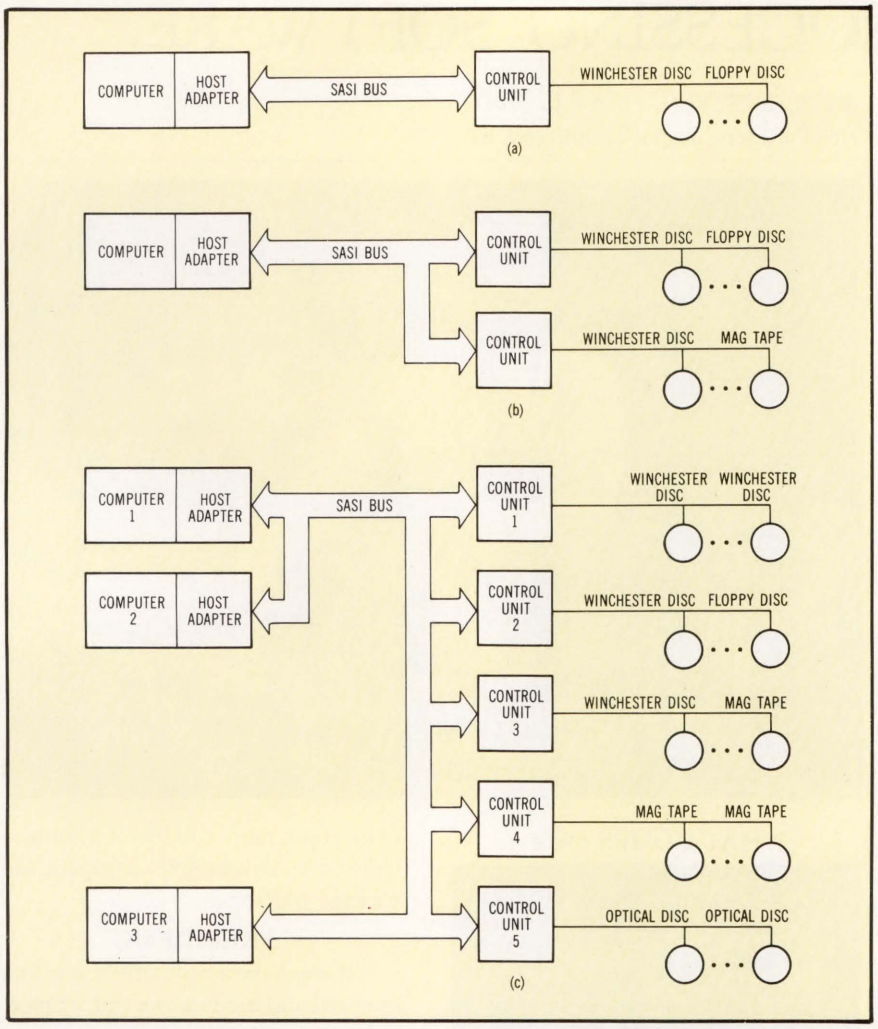


Fig 1 Sample SASI configurations. SASI bus supports up to 8 devices. Devices can be any combination of host CPUs and/or intelligent controllers. In (a), simple system is shown; in (b), basic 2-control unit system; and in (c), complex system

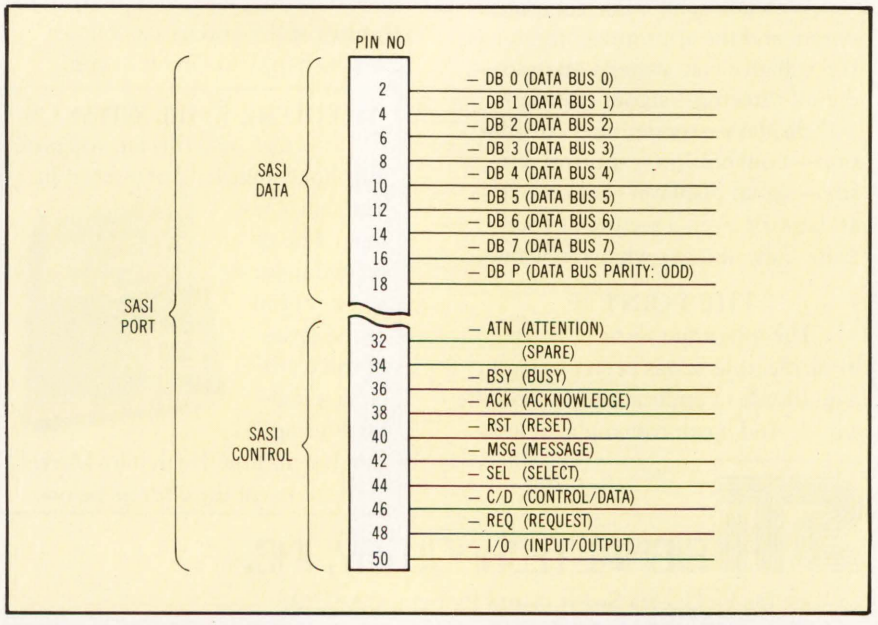


Fig 2 Control lines on SASI bus. CPU sends and requests data blocks over these lines via intelligent device controller

Standard interface for intelligent controllers eases integration effort

A system interface, designed to eliminate separate controller design efforts each time a new storage peripheral is integrated into a system, also reduces the need for altering software drivers and host adapters. The Shugart Associates Systems Interface (SASI) enables designers to mix, upgrade, and interchange memory peripherals without affecting the CPU, the operating system, or the application program. SASI consists of standardized connectors and cable between an intelligent controller and a host bus adapter.

Essentially a peripheral bus that assumes a certain amount of intelligence in the controller, SASI allows up to eight host CPUs and controllers to be interconnected. In addition, it provides data lines and a set of control lines that can be used by the host to communicate with the controller to perform searches, locate key parameters, and self-arbitrate for bus control.

Such controllers, exemplified by but not limited to Shugart's SA1400 line of intelligent disc controllers, provide intelligent architecture with logical block addressing. This allows the host CPU to specify the first block address and the number of data blocks to be transferred; seeks are implied. The controller, not the host, then handles tasks such as error correction and detection, data separation and buffering, and physical selection of disc cylinder, track, and sector.

One goal of SASI, whose specifications are being placed in the public domain, is the development of a standard set of custom LSI chips for controllers. This will allow price/performance improvements, as well as incorporate the controller into the form factor of the peripheral device.

Because its intelligence is located in the controller, SASI encourages the use of relatively high level host commands. More transparent to the user, high level commands can also be interpreted by the controller, which performs the particular logical and physical functions required by a specific device. It is, in effect, both establishing a discipline of things to do and initiating an internal Shugart standard.

This level of standardization eases integration of dissimilar devices. SASI permits buffered bidirectional data transfers between fast and slow floppy disc drives, while also providing an interface between relatively slow microprocessors and future high speed disc and optical storage systems. **Shugart Associates,** 475 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 270 on Inquiry Card

TOMORROW'S TAPE TRANSPORT IS HERE TODAY

Introducing DATUM's New "Gemini" Multifunction Tape Transport

TWO FUNCTIONS — ONE DRIVE

Until now, data processing managers have been forced to make a choice between a tape drive that performs transaction processing effectively or one that will load and unload disk files at a rapid rate. Now, for the first time in the industry, DATUM offers you a single transport uniquely matched to both functions...the DMF-1000 Gemini.

For day-to-day transactions, the Gemini operates as an industry-standard, 45-ips drive. For disk backup, streaming mode can be selected by software command. Transfer rates are monitored, and if data fails to keep pace at 125-ips streaming speed, the drive automatically reverts to 45-ips to provide optimum efficiency.

A TECHNOLOGICAL FIRST

The DATUM DMF-1000 Gemini is a major breakthrough in the evolution of magnetic tape transports. The result of an extensive two-year development program, the Gemini is the ideal solution for those users requiring both 45-ips transaction processing and high-speed disk file backup. DATUM's Gemini eliminates the need for compromise by meeting the demands of two different operating environments with a single entity. Gemini...tomorrow's tape transport...is here today.

datum inc
Storage Systems Division
1363 S. State College Blvd. Anaheim, California 92806
TEL: (714) 533-6333
TWX: (910) 592-1289, TELEX: 68-5579

CIRCLE 79 ON INQUIRY CARD

THE CLOSER YOU LOOK
at the MSC 8009 Microcomputer

For Multibus® Compatibility

The more you will be impressed by the balance of technology and standardization achieved with this Z-80A® based, Multibus compatible, single board computer. The MSC 8009's capability starts with the high speed, 4Mhz. Z80A microprocessor that offers more than 80 additional instructions over the 8080 or 8085 CPUs. Second, an on board Floppy Disc Controller for up to four disc drives is standard. Third, a unique memory management technique allows full utilization of up to 96K bytes of on-board RAM/EPROM. And, finally, all peripheral I/O interfaces normally required for most microcomputer system applications are included on the MSC 8009. For those who need complex transcendental arithmetic processing, an optional on board APU is available to add credibility to our claim that the MSC 8009 is the finest 8-bit microcomputer available today.

Superior Design

The superiority of the MSC 8009 design permits system configurations with a significantly reduced number of boards. Thus, many systems may only require a single MSC 8009 for all computer functions. The same system currently may require four or more boards to provide the same capability. In addition, a fully configured MSC 8009 requires only a single standard Multibus card slot. Full capacity configurations using many of the newest 8085 based boards, because of their "piggyback" configuration, require two board slots per microcomputer. An MSC 8009 based system will require fewer card slots and less power while providing higher reliability at an overall lower cost.

Application

The MSC 8009 Microcomputer provides the computational power, memory capacity, floppy disk controller and peripheral interfaces typically required in "high-end" microcomputer systems. It is ideally suited for floppy disk based, interactive systems running under CP/M®. Because it is CP/M compatible, users can select from a wide range of off-the-shelf systems and applications software packages when configuring a new system. The MSC 8009 configured with an appropriate software package can be the heart of a range of systems from software development stations to word processing systems, to office management systems. When used in conjunction with other MSC 8009 microcomputers, MSC 8901 memory management modules and MP/M or CP/Net, entire multi-user, multi-tasking networks are possible. These applications can be "performance optimized" by the use of multiple processors. No matter what your application is, the versatility and power of the MSC 8009 makes it a welcome addition to the Engineering Laboratory, an office environment or on the production floor.

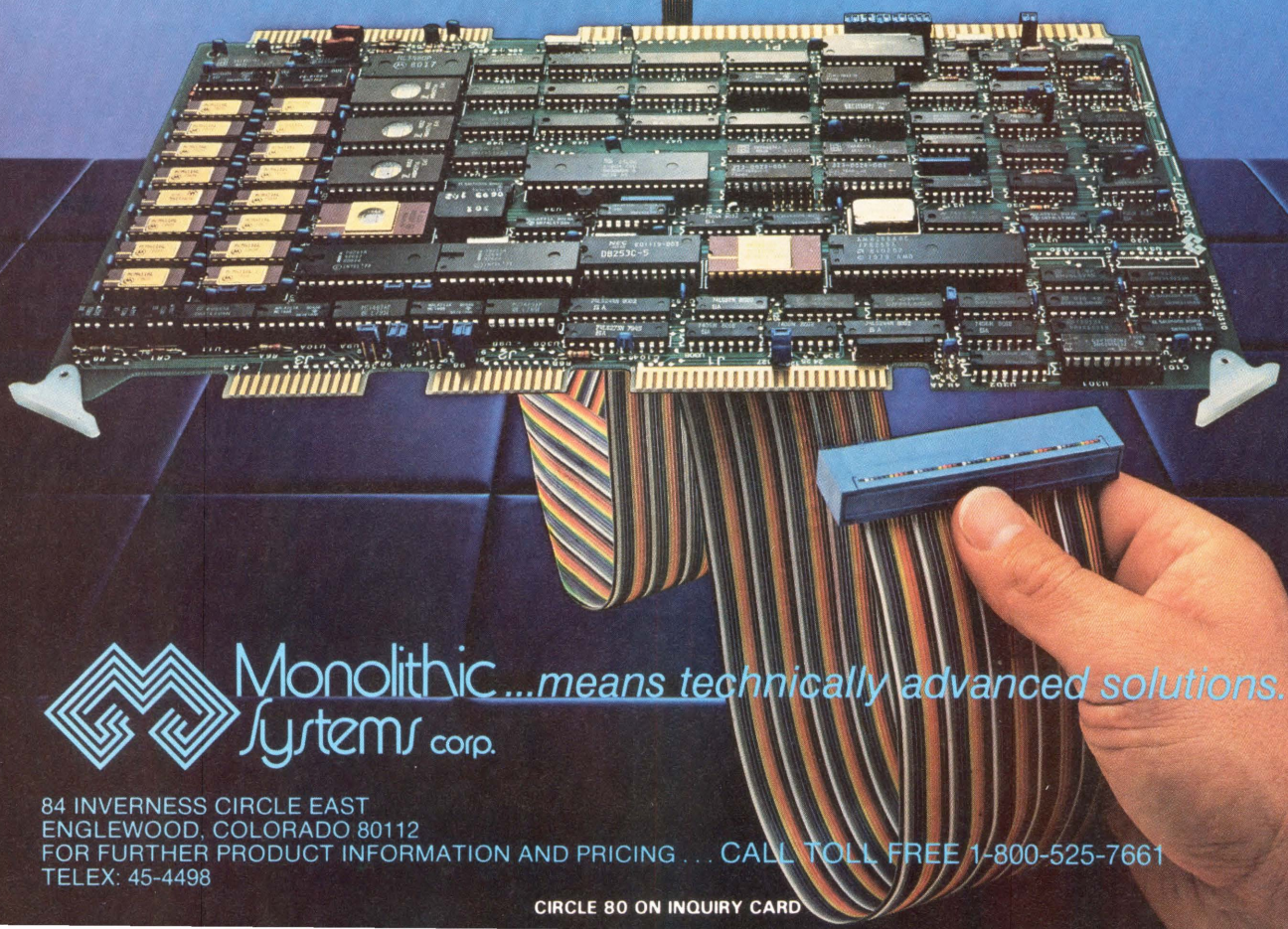
Software Support

Software support for the MSC 8009 microcomputer is provided by the MSC 8800 family of software development systems. These are among the industry's most cost/performance optimized systems. All MSC 8800 series development stations are complete systems including a MSC 8009 computer with 64K bytes of RAM, a floppy disk controller and peripheral interfaces. Mass storage is provided by two 8" double density disk drives. A CRT terminal and line printer are standard on all systems. Higher speed systems are available with multiprocessing capability. For highest performance, a multiprocessor based system is available with a semiconductor disk emulator. CP/M 2.2 with a universal BIOS that allows formatting and transfer of data between mixed drives is standard on all MSC 8800 series systems. Both assembly language and high level languages, including Basic and Pascal are available.

Features

- ☐ Multibus (IEEE 796) Compatible
- ☐ 4 Mhz. Z80A Microprocessor
- ☐ On board Floppy Disk Controller
- ☐ 32K Bytes Dynamic Ram
  Expandable to 64K Bytes on board Ram
- ☐ Socketed for up to 32K Bytes EPROM
- ☐ User defined RAM, ROM and I/O addressing
- ☐ Two RS232C Serial I/O PORTS
- ☐ Eight Prioritized and Vectored Interrupts
- ☐ One Non Maskable Interrupt
- ☐ Three 16 bit Programmable Counter/Timers
- ☐ Optional on board APU Provisions

Multibus® is a registered trademark of Intel Corp.
Z80A® is a registered trademark of Zilog Inc.
CP/M 2.2® is a registered trademark of Digital Research.



Monolithic Systems corp. ...means technically advanced solutions.

84 INVERNESS CIRCLE EAST
ENGLEWOOD, COLORADO 80112
FOR FURTHER PRODUCT INFORMATION AND PRICING . . . CALL TOLL FREE 1-800-525-7661
TELEX: 45-4498

CIRCLE 80 ON INQUIRY CARD

DBMS: AN ARCHITECTURAL APPROACH

Responsive information management architecture supports tools flexible enough to solve user needs and allow necessary growth

by Anita Moeder

Information is a corporate resource—but an important and expensive one. As companies grow in complexity and become more physically dispersed, the control and dissemination of information become critical. Moreover, advances in productivity are closely linked to how effectively information is managed at all levels of the organization. As information needs grow rapidly, so does the large backlog of work.

An information management architecture is a design concept that integrates software elements for the three user environments typical of most organizations (Fig 1). The first is a structured user environment in which the user provides a staff or service function. In this environment, experienced data processing professionals are responsible for coordinating and controlling corporate information. They use traditional data processing tools to develop and maintain high payback applications.

In the second of the three, the *ad hoc* environment, part of the line organization, less sophisticated data processing professionals develop and maintain large numbers of transient applications. Here, decision support systems that access corporate data are the key. Higher level tools are needed to speed up development and facilitate the maintenance of applications.

The third environment involves individuals—the end users—who are not data processing professionals. Because of ever changing information needs, they cannot rely on programmers to provide information in a timely manner. End users, who require information quickly to fulfill their decision support roles, need to access corporate data in ways that cannot be predefined.

Depending on the size and complexity of the organization, these three environments, which are not necessarily hierarchical, can be scattered throughout the corporate structure. Productivity must be improved at all levels, creating a challenge to build an architecture of information management products that supports a range of tools flexible enough to solve a wide variety of user needs and that will also provide for additional tools and growth. The integration of these products will facilitate information flow and control within the organization, whether in a local or distributed environment.

An information management architecture comprises many components. It must be built on a reliable hardware system with the capacity to handle large numbers of user requests efficiently. A powerful and flexible operating system that complements the hardware must be the cornerstone of all software used in the architectural approach. Miscellaneous utilities should include sort/merge packages; text and word processors; mail facilities; library utilities; and data copy, load and unload programs. These operating system elements should be designed to facilitate all users' jobs. They could be standalone or incorporated into other tools so as to be transparent to the user.

Network software should provide the means by which data resources maintained at remote sites are brought into an information management system. Companies that generate data at more than one site may use a corporate communications network to update some data bases at a corporate data center. It may be better to distribute other data bases among sites closer to where data are entered. With network software, the information management architecture could permit distributed

Anita Moeder is a product manager at Digital Equipment Corp, 8 Continental Blvd, Merrimack, NH 03054. Ms Moeder has worked in data processing for over ten years, in the areas of classic corporate data processing, financial accounting, transaction processing, and decision support systems. She has a BS degree in computer science from Boston University.

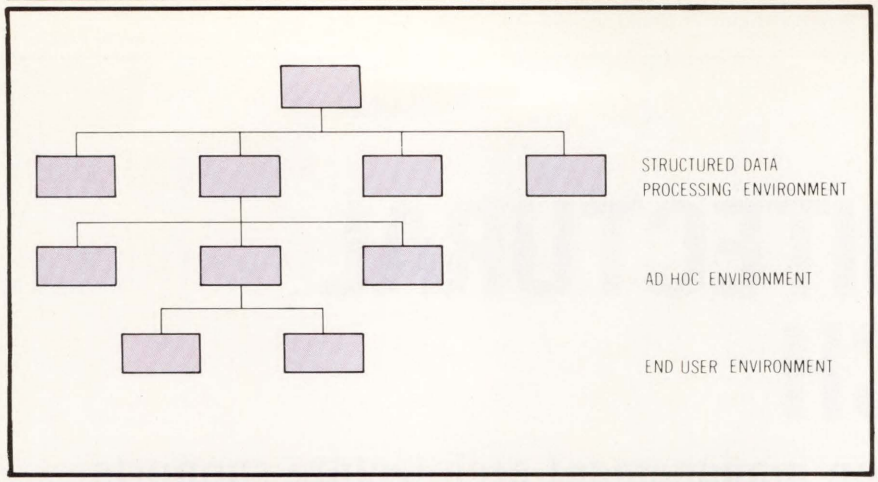


Fig 1 Organizational hierarchy. Three user environments typify most organizations. Size and complexity of organization determine these environments, which need timely and accurate information flow

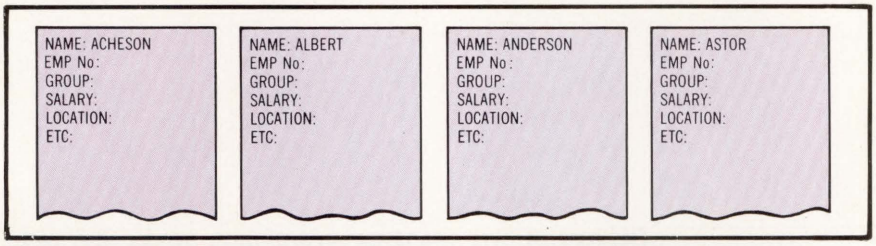


Fig 2 Employee file. Collection of data records is interrelated and known in some way to users

data access without changing the manner in which users access data.

Software that control the physical access to data must be available. These products understand how the data are physically stored and how data must be accessed or updated in response to requests from other software. The three most important data structures are file management systems, CODASYL (Conference on Data System Languages) data bases, and relational data bases.

File management

A file (Fig 2) is a collection of data records, interrelated in a way known to users. A file management system has no idea how the records in any file are interrelated, or related to records in other files. Therefore, an application program that makes use of such records must itself include statements to retrieve the right records from the right files before making calculations and producing reports. Other application programs that draw on data in these records—even the same exact data—must do likewise.

The three types of disc file organization are: sequential, keyed, and relative. In a sequential file, each record is accessed by retrieving, in succession, all records that physically precede it. In Fig 3(a), the record on Anderson can only be accessed after retrieving the Acheson and Albert records.

In a relative file each record is identified by its position relative to the beginning of the file and can be randomly retrieved by specifying its relative record number. In Fig 3(b), the Anderson record is then retrieved by specifying record number three.

A record is retrieved in a keyed file on the basis of the contents of a specified field in the record, called a primary key field. If this key field is employee name, then the user would specify Anderson in order to retrieve record number three. However, the user cannot later switch to make employee number the primary key because the key field must remain what it is initially assigned for the life of an indexed file.

In an indexed file, data records can be arranged either in a random physical order or in a specific order that may not always be relevant to users. A separate index is maintained in order by key contents, and each entry in the index refers to a relative record number in the data file. In Fig 4, the index lists employee names alphabetically; if the user selects "Albert," the index points to record number 5 in the relative data file.

A useful function of an indexed file is sequential access to data records in whatever sequence is defined by the index, which is entirely different from sequential access, where there is no index. For this reason, indexed files are usually referred to as indexed sequential files or indexed sequential access method (ISAM) files. Single key ISAM files are files in which there is only one key field. This organization can be extended to a multiple key ISAM file, in which there are separate indexes for the primary and secondary fields in the record. A user can thus retrieve a record by knowing its value in any key field.

CODASYL data bases

Data base management systems provide a more powerful, flexible method of handling data resources than file management systems. In file management, an application program itself must define the data structure and data needed for its specific task. Changes in data structure, therefore, also require changes in application programs. In addition, data definitions in different programs are likely to be subjective, that is, specifically

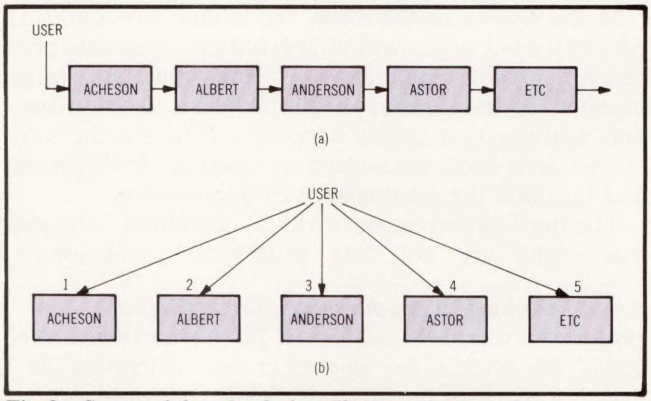


Fig 3 Sequential and relative file organization. In sequential file organization (a), each record is accessed by successively retrieving all preceding records. In relative file organization (b), each record is identified by its position relative to beginning of file and can be randomly retrieved

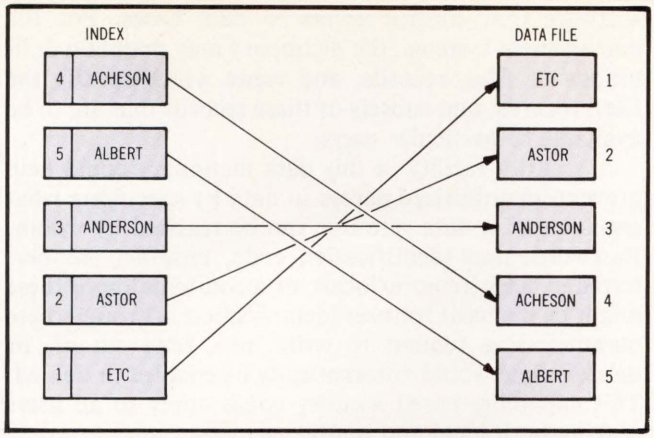


Fig 4 Single-key ISAM file. Whatever physical sequence of data file, access sequence is defined by index

oriented to the concerns of each program. A database management system, on the other hand, isolates data structure definitions and data from application programs. Accordingly, changes in data structure can be made without necessarily changing the application programs.

Definitions of data and structure in a data base are concentrated in an independent computer-readable file—the schema. The portions of the data base that are to be accessible to particular application programs are described in subschemas. Also independent of the programs, a subschema converts the objective data definitions in the schema into subjective definitions appropriate to an individual program. In addition, it can

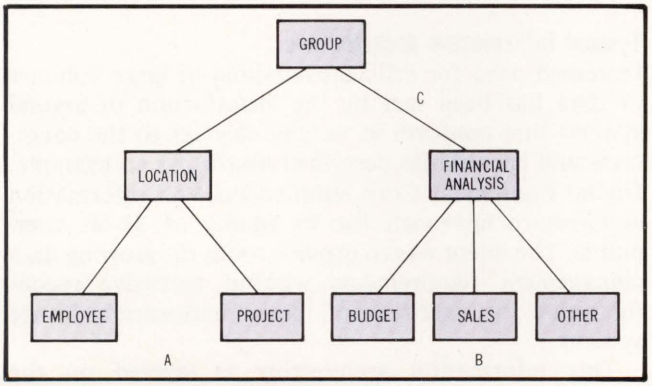


Fig 5 Tree or hierarchical structure. Structure is restrictive because once branch is taken, there is no way of reaching other records without first returning upward

also group fields in a record in a convenient arrangement for that program. For example, the employee file in Fig 2 might have been assembled by a subschema from data fields not associated that way in the actual data base.

The three types of classic database structures are tree or hierarchical, network, and relational. In a tree or hierarchical structure (Fig 5), each record type can branch down to one or more record types, each of which may, in turn, branch down to one or more, and so on. Once a branch is taken, there is no way to reach the records on another branch without returning upward and taking another path. The structure also restricts hierarchical relationships. For example, record types A and B in Fig 5 cannot be defined as subordinate to record type C in the schema.

The network is a more flexible form of database structure (Fig 6) in which any record can be related to any other record without restriction. Even greater flexibility was provided in a network structure when CODASYL introduced the set as the basic building block from which all database relationships can grow. (While all CODASYL data bases are networks, not all networks are CODASYL structures.) A set, the only form of data organization that can be defined in a CODASYL system, consists of three record types—owner, member, and connector—for additional flexibility.

In Fig 7, the supplier record is the owner, the parts record the member, and the supplier/parts record the connector, which defines the relationship between the other two record types. The connector permits records to be retrieved for all parts (members) made by a specified supplier (owner). Conversely, it points to all suppliers (now members) that make a specified part (now the owner).

The principal attribute of the CODASYL system set concept is that each set may be defined without regard to what kinds of sets already have been or will be defined in the future. In contrast to the hierarchical and network structures in Figs 5 and 6, there can be no illegal relationships between record types and the actual database structure is not important.

Relational data bases

The main characteristic of a relational data base is that the data appear to be structured in tabular form. The rows in a table correspond to records and the columns correspond to fields within records. Hierarchical and network structures can be flattened to appear relational, as has been done in Fig 8. In a relational system, it does not matter if the internal format of a relational data base is actually a hierarchy or a network, as long as the end user sees those data in rows and columns form.

A true relational database structure has distinctive features: each table contains only one record type; each record has a fixed number of specific fields; each record is unique and duplicates are not permitted; and new tables can be produced by matching field values in two existing tables.

The three ways in which relational data structure tables can be manipulated are selection, projection, and join. A selection operation creates a subset of all records in a table by applying a selection criterion to one or

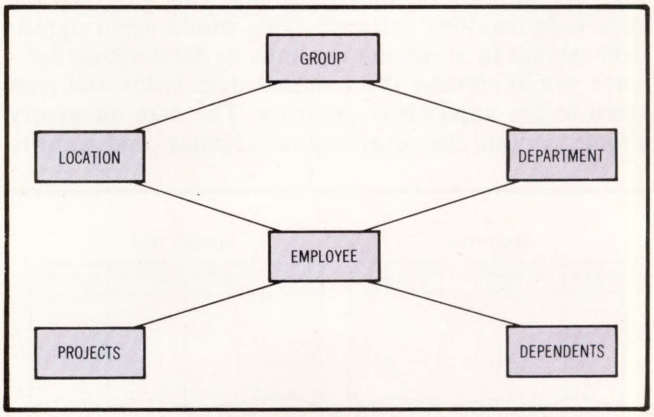


Fig 6 Network database structure. Any one record type can be related to any other record in whatever arrangement is needed to support information management system

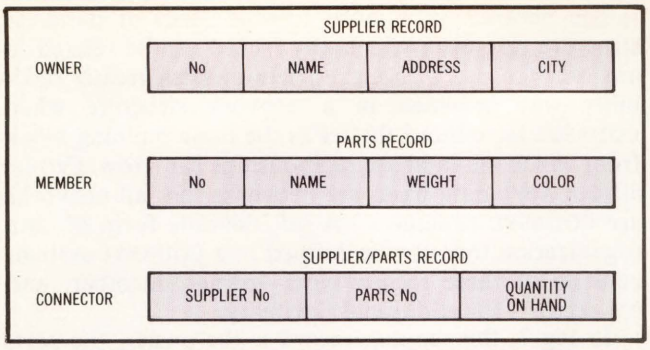


Fig 7 Flexible CODASYL set. Introduced as basic building block in network database structure, set does away with illegal relationships between record types

more fields. A selection might be made in table B of Fig 8, for example, by creating another table containing only those rows—group, address, and phone number—for which a specific location is given in the location column. In projection, only certain columns in a table are retained to produce a new table with fewer columns; table B can be projected without the telephone number column. A join combines two tables on the basis of common values in one column of each table. For instance, tables A and B can be joined via the group column to give the group name, manager, location, address, and telephone number on one table. The step-by-step process of joining can be very slow, resulting in a poor response time. All true relational database management systems should therefore include sophisticated means of optimizing table manipulation in the retrieval process.

Application languages

The application languages, additional information management architecture components, provide programming tools that are available under the computer's operating system. These languages, used by the company's data processing staff and often by some end users to write a variety of programs, usually require access to the company's data resources. However, a language designed primarily for computation may not be capable of efficiently accessing data resources. In addition, no matter how capable the language is, it may not be cost effective for the programmer to write the necessary retrieval algorithms.

Significant to an information management architecture are application languages that can interface the data base handling software. This would mean significant savings in programming time, as the database software would retrieve the required data fields and pass them to the application program. The data dictionary should contain the schemas, subschemas, and security

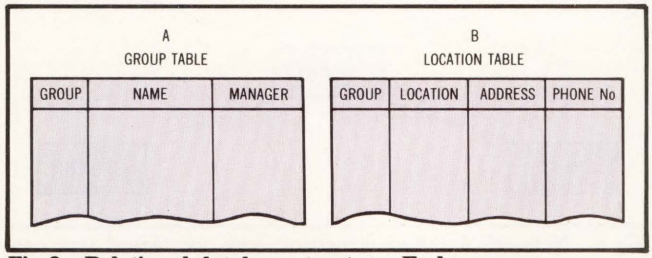


Fig 8 Relational database structure. End user can manipulate tables by selection, projection, or join

software that control access to data bases. For file management systems, the dictionary may maintain definitions of files, records, and views which specify the files, records, and subsets of these records that are to be available to particular users.

A security facility in this data dictionary could help prevent unauthorized access to data by specifying what segments of a data resource can be reached by whom. Password, user identification code, terminal number, terminal class (remote/local), or a combination of these might be the basis for user identification. Through these parameters, a request to write into, read out of, or delete a field would automatically be enabled or denied. This capability-based security could apply to all users making both local and remote requests.

Software tools that provide interactive interfaces between user and computer must be available. When making a request for information, the user should not be concerned with how data are stored, accessed, or controlled. To enter information, the user should be presented with a format with which he/she is comfortable. Four software tools are most common to the user. *Forms management* retrieves and modifies information organized in a display format on the video screen. Complex forms should be generated without detailed instructions by using predefined formatting algorithms. *Query language* creates, retrieves, sorts, and updates data. *Report writer* produces summary and detail reports, titles, headings, footnotes, group totals, and report totals. Users may or may not be given full capability. Lastly, *graphics* creates pie charts, plots, histograms, and other forms of graphical data.

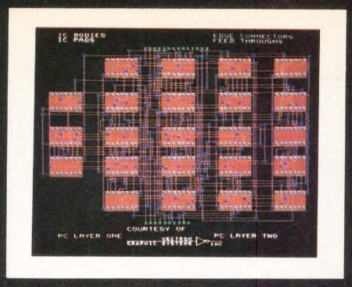
Typical information architecture

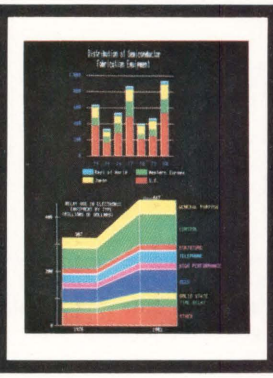
Increased need for efficient handling of large volumes of data has been met by the introduction of several systems that conform in varying degrees to the conditions and capabilities described above. As an example, Digital Equipment Corp adopted the VAX information architecture approach for its family of 32-bit computers. The intent was to provide room for growing data management requirements without extensive reconfiguration or sacrifice of basic hardware/software systems.

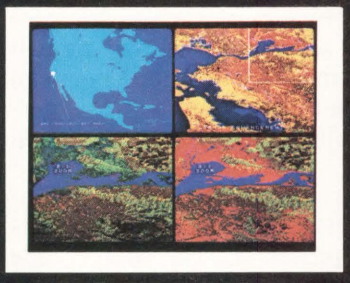
This information architecture is layered on the VAX/VMS operating system, which can handle a large range of tasks, languages, and hardware configurations. A wide variety of languages—including BASIC, BLISS, COBOL, FORTRAN, Pascal, and PL/1—are supported.

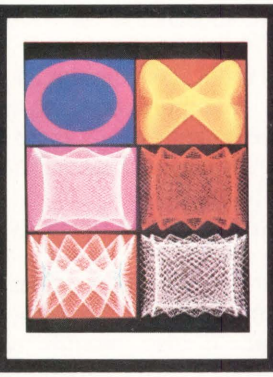
RMS (record management services), the file management system, provides general purpose file handling capabilities for all of the languages, as well as for DATATRIEVE. Its extensive data storage retrieval and modification facilities offer flexibility for a variety of applications. Sequential, relative, and multikeyed indexed files are supported, in addition to record access modes such as sequential, keyed sequential, random dynamic, and relative record access. Depending on the support provided by different languages, a program can use approximate generic and duplicate key access. RMS files can be concurrently accessed by multiple programs.

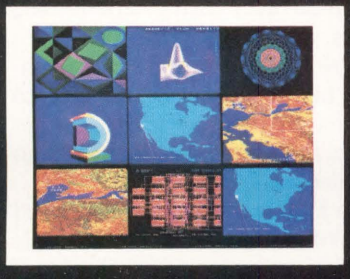
FMS (forms management system) provides a video screen management capability for the programming languages and DATATRIEVE. It can be used for fill-in-the-blank type input, in which validation checks are











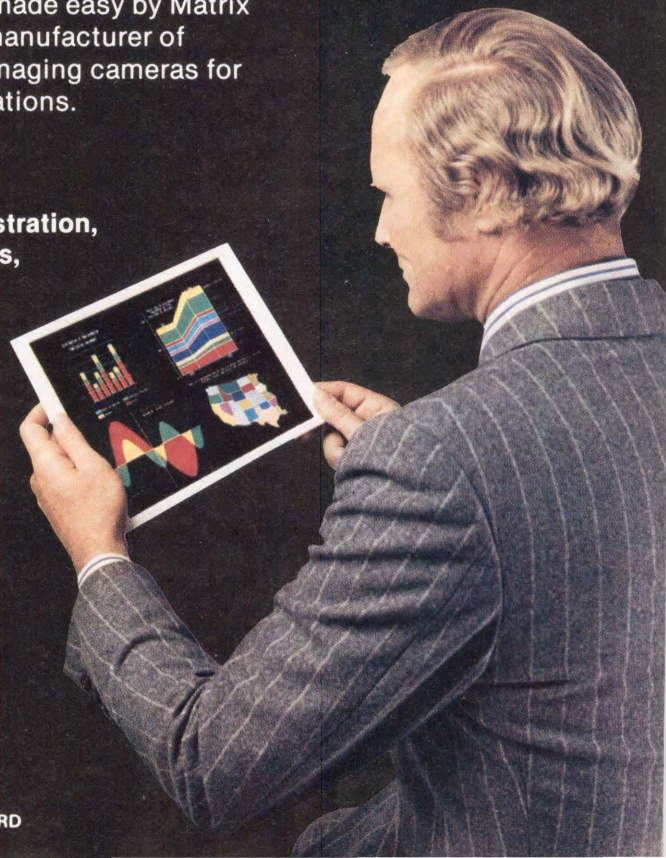
Color Graphics Hard Copy... Made Easy

The Matrix Color Graphic Camera System converts the output of any raster scan computer color terminal into brilliant, high resolution photographic hard copy. Both line and continuous tone images can be made with accurate, bright, saturated colors.

Our system does what no other instrument can do — it produces instant, on-the-spot results with Polaroid® 8 x 10 film, 8 x 10 color transparencies for backlit displays and overhead projection, 35mm color slides, 60 image color microfiche, and 16mm/35mm color animation films. All with one camera system. It also allows recording of multiple image formats. Related and sequential images can be recorded in orderly arrays, on a single sheet of 8 x 10 instant print film. The resultant ease of comparison and analysis is unmatched. The system is also fully modular and field upgradable. . . you purchase only the capability that you need now.

Microprocessor based electronics provide many automation, self-calibration, self-diagnosis and remote control functions. Color graphics hard copy made easy by Matrix Instruments, the leading manufacturer of precision electro-optical imaging cameras for diagnostic medical applications.

For more information, film samples, or a demonstration, contact Matrix Instruments, 230 Pegasus Avenue, Northvale, New Jersey 07647. Telephone (201) 767-1750 Or call toll-free: (800) 526-0274.



 # MATRIX INSTRUMENTS

Overhead Projection Transparency

Slide

Hard copy shown reduced from original 8″ x 10″, slide, and microfiche films.
Multiple images recorded on a single sheet of film.
"Polaroid" is a registered trademark of the Polaroid Corporation.

CIRCLE 81 ON INQUIRY CARD

performed as the information is entered. Screen forms can also be used to format video output displays and are defined interactively. Having one video screen management facility improves programmer productivity by reducing training time and by using the same form definition with DATATRIEVE and the programming languages. Because a consistent interface is seen—the screen form is the same—the end user becomes more productive.

CDD (common data dictionary) is a central repository for metadata (ie, data about data) and is the hub of this information architecture. It ties the components together by making possible use of a single set of data descriptions as a common resource. One logical dictionary per system is provided by CDD, which adds security on top of that provided by VMS. CDD also allows application languages and DATATRIEVE to share stored subschema definitions. CDD has one integrated directory that is an index to both the DATATRIEVE and the DBMS (data base management system) data definitions it contains. This directory is organized as an n-level hierarchy with a structure closely resembling that of the VAX/VMS system directory.

For DATATRIEVE, the CDD stores record format descriptions and domain definitions for RMS files and database structures, both local and remote. The CDD also contains DATATRIEVE procedures, tables, and views with extensions that allow location of files to be known, which in turn permits remote access without end user intervention. Another extension provides information on whether or not screen forms are to be used with specific definitions.

For DBMS, the CDD stores database data descriptions on three levels—schema, subschema, and storage schema. These definitions are used by DBMS to build database structures, and by languages to compile application programs. The schema, the master data definition for a database, contains all record, data item, and interrecord relationship definitions. One schema exists per data base. The subschema definitions, application program views of the data, are used by the language compilers to produce data definition source code in the compilation process. A storage schema is used to map the actual database data to particular storage media areas.

DBMS is a CODASYL-compliant DBMS based on the March 1981 working document of the ANSI (American National Standards Institute) Data Definition Language Committee. It automatically controls data integrity in a multi-user environment and, using automatic record level locking, provides full concurrent access and update capabilities. DBMS allows multiple data bases to be online at the same time.

Many applications do not warrant a full scale design effort involving subschemas and a storage schema. To accommodate these situations, DBMS provides an automatic default subschema and default storage schema generating facility. DBMS also allows addition of fields, records, and certain kinds of set relationships without the need to unload and reload the data base.

DBMS includes DBQ (data base query), a data manipulation tool that can be used interactively. DBQ lets the programmer interactively retrieve, update, and store any database record. It executes COBOL-like data manipulation commands and automatically generates

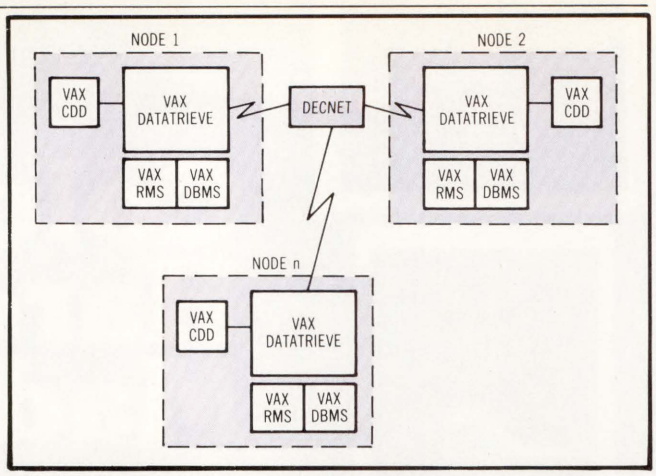


Fig 9 Transparent access to data. DATATRIEVE provides users with transparent access to data at remote nodes linked by DECnet communications software and equipped with DATATRIEVE

displays of easy-to-follow schematic diagrams that illustrate access paths. Data manipulation operations can be tested against actual data structures, which is particularly useful when checking out application program changes.

All DBMS definitions are stored in CDD. For application development, application program source code is compiled by a language processor. The source code must reference a particular subschema previously defined.

For FORTRAN and COBOL, data access commands are compiled in DBMS database manipulation language (DML). For the other acceptable languages, database access is performed by using DBQ statements that are interpreted by the DBQ utility at runtime.

DATATRIEVE can also be used to access DBMS structures. It gives very high level data access to data and eases user access to information. The user states in English commands what information is wanted; DATATRIEVE manages the rest. It also provides distributed access, a callable interface, forms capabilities, graphics, query capabilities, and a report writer.

High level access. DATATRIEVE, with one set of commands, provides a single high level user interface to traditional files and DBMS data structures. When an application is either added to the system or changed, no retraining or relearning is necessary.

The user is provided with a logical view of data stored in DBMS or RMS files, making it possible for a single statement to retrieve a set of records with a single request. With DATATRIEVE relational join capability, related records of different types may be linked dynamically. Users do not have to determine in advance the records they want to link. The access facility is capable of making these associations while in process by using a relational join.

DATATRIEVE is callable from user application programs with calls that use the same English-like syntax as interactive DATATRIEVE. Therefore, programmers can concentrate on coding the procedural part of the application and call DATATRIEVE to supply a high level, conditional, value based, data access.

Distributed data access. The information architecture works with DECnet-VAX to provide a distributed data access facility for users to access remote data in the same

We've got the VT100™ market seeing red,

and blue, and yellow...

Introducing the VT100-code compatible Colorscan 10 for just $3,195. It's the first affordable display terminal with the dramatic high-resolution color that businesses need.

The new Colorscan 10 features eight independently selected foreground/background colors (red, green, blue, yellow, cyan, magenta, black and white) crisply displayed in both 80- and 132-column formats. You also get a 128-character set, plus 128 special graphic symbols.

The Colorscan boasts state-of-the-art ergonomics too. You get a tiltable screen, high resolution display, and detachable keyboard with separate numeric pad.

Inside, the Colorscan is packed with performance. Like smooth or jump scrolling and split screen/regional scroll. Double-high/wide and double-wide characters. Keyboard selected set-up parameters, self testing, even a CRT saver. All standard.

If your business needs more effective financial and sales graphs, charts, histograms, or drawings in 80- or 132-column formats, ask about the Colorscan 10.

It covers the whole spectrum of business applications.

Write or call the smarter terminal maker: (609) 665-5400. Datamedia Corp., 7401 Central Highway, Pennsauken, NJ 08109.

Colorscan 10

Make me see colors. Please:

☐ Send complete product information.

☐ Have your representative call.

Return to: Datamedia Corporation, 7401 Central Highway, Pennsauken, N.J. 08109. (609)665-5400.

Name _____

Company _____

Address _____

City _____

State _____ Zip _____

Phone _____

DATAMEDIA

From the smarter terminal maker.

VT100 is a registered trademark of Digital Equipment Corporation.

CIRCLE 82 ON INQUIRY CARD

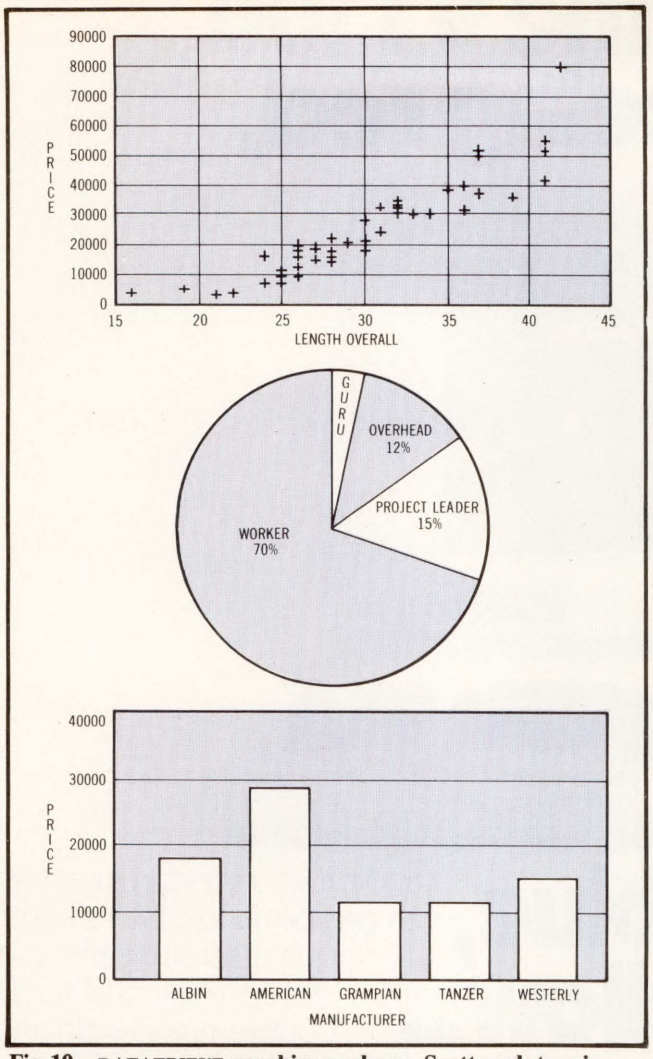


Fig 10 DATATRIEVE graphics package. Scatter plots, pie charts, and bar graphs created in displays or hard copy by DATATRIEVE, in conjuction with VT125 graphics terminal and LA34-VA printer

way as data stored locally. Because the CDD stores the remote data location, the user need not know where the information is stored. When the query request is executed, DATATRIEVE uses DECnet-VAX to forward the request to the appropriate node (Fig 9). The request response is then returned over the line and presented to the user just as if the data had been stored locally.

This operation is extremely efficient. Only the records that satisfy a query are returned over the transmission line, and since the data description is maintained with the data, the complex problems normally associated with distributed data management are minimized.

Query and report writing. DATATRIEVE commands are English words, not confusing acronyms. DATATRIEVE supports nonprocedural queries where the user can tell the system what information he wants to see without having to tell the system how to get it. However, interactive DATATRIEVE is not just a query and report writing facility. It has full update capabilities enabling a full range of information management functions at a high level to be performed. Entire standalone applications can be implemented from scratch, without any previous computer experience, with DATATRIEVE.

The DATATRIEVE report writer helps display data in easy-to-read format. A report may be displayed on a terminal, printed on a hardcopy device, or stored in an RMS file for display or printing at a later time.

The DATATRIEVE print statement can also be used to produce simple reports. The print statement does not provide all the formatting and statistical capabilities of the report writer, but the output contains the same options of immediate display on a terminal, hardcopy, or storage in an RMS file. In addition, guide mode is a special self-teaching feature for novice users. With this mode set, the user gets multiple-choice prompts at each decision point.

Information architecture provides a range of software tasks, with substantial productivity gains, to meet the users' needs.

DATATRIEVE also includes a utility called ADT, the application design tool. ADT simplifies the process of defining RMS files, which means it is not necessary for DATATRIEVE users to know or understand programming in order to create and use data files.

Graphics. The DATATRIEVE graphics package enables data summaries to be displayed on black and white and multicolored charts. With the plot statement, data can be displayed in several formats, such as: 1- and 2-variable pie charts; single-, multi-, and stacked-bar charts; 2-dimensional line graphs of 1 to 7 functions; 2-dimensional scatter plots; and histogram (Fig 10).

For video display of the plots, a VT125 video terminal using the Regis graphics language is necessary. The VT125 must be connected to a color monitor to display full color output. Hardcopy can also be generated using the LA34-VA matrix printer.

Summary

The information architecture provides a framework of interacting products. The user can select the most appropriate combination, with assurance that future growth is provided for within the framework of the information architecture. Moreover, the software investment of the past remains protected and extensible.

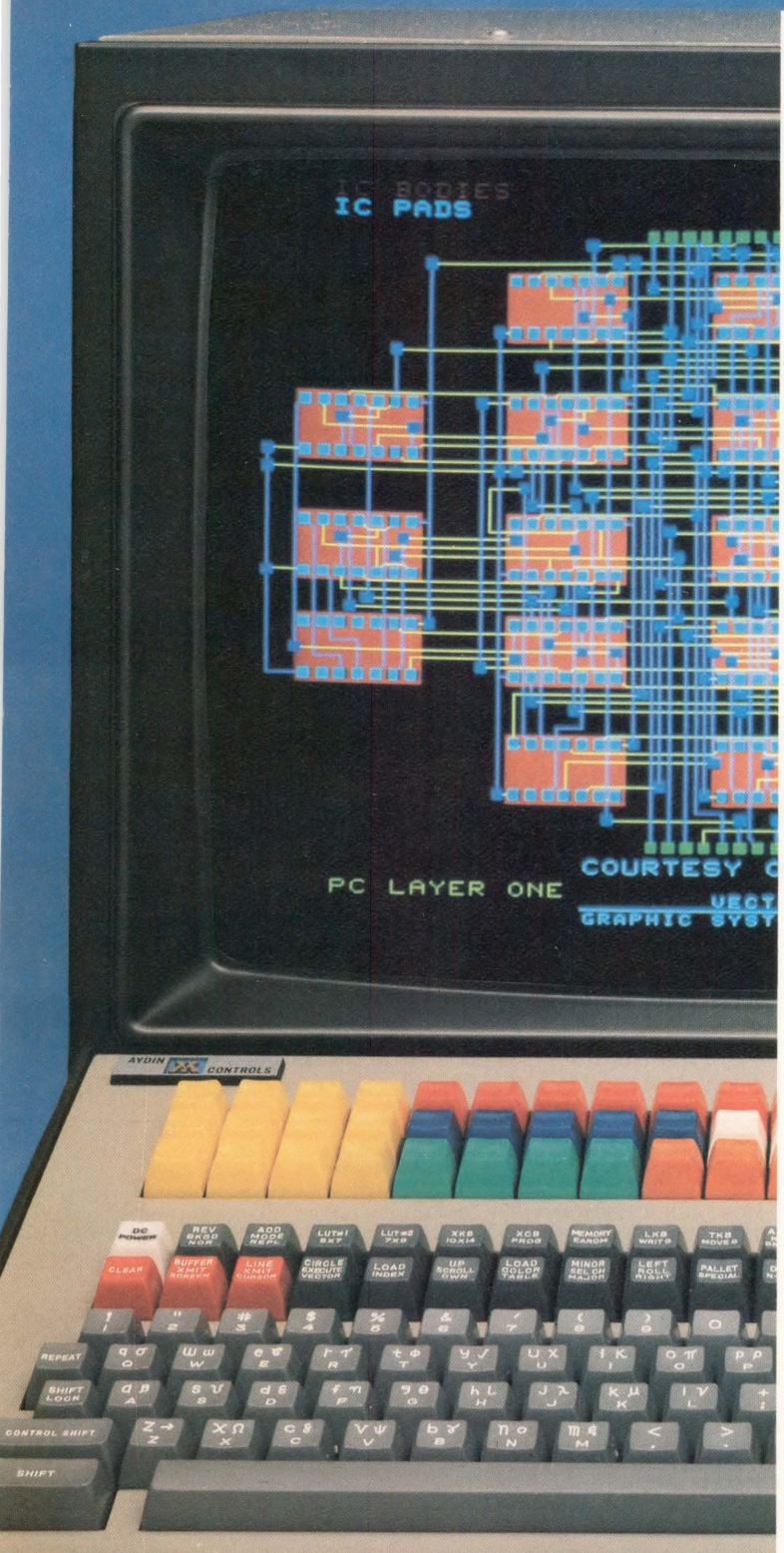
Information architecture provides a range of software tasks, with substantial productivity gains, to meet the users' needs. Key to this is the architecture—designed as an integrated product set to optimize information flow and control within a centralized or distributed environment.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 701 *Average 702* *Low 703*

Quickens Your Draw

Aydin user-oriented, full-color graphic systems let you tackle complex design and processing projects quickly and easily.



Aydin 5216 high-resolution multiprocessor-based color graphic systems lead the industry in fulfilling the needs of intricate process control CAD/CAM, simulation, C³I, image processing and many other sophisticated applications.

Versatility is the result of the Aydin growing family of hardware and 2D, 3D, imaging and CORE software modules. The 5216 gives you both the flexibility and programmability to design and implement your ideas efficiently and economically; a true man-machine interface. For example, AYGRAF instruction sets provide both standalone and distributed processing capabilities to support 2D graphics in a standardized manner. The 3D system, which supports standalone and host-driven applications, is designed to give the user the full benefit of sophisticated graphics, all with interactive control that doesn't burden the host computer.

Aydin modular design also means that you can customize the 5216 to your strictest requirements, easily expand memories, add storage and utilize various user-programmable lookup tables. In addition, a host of interactive devices are available, including joysticks, trackballs, graphic tablets, touch panels and lighted or non-lighted function keys.

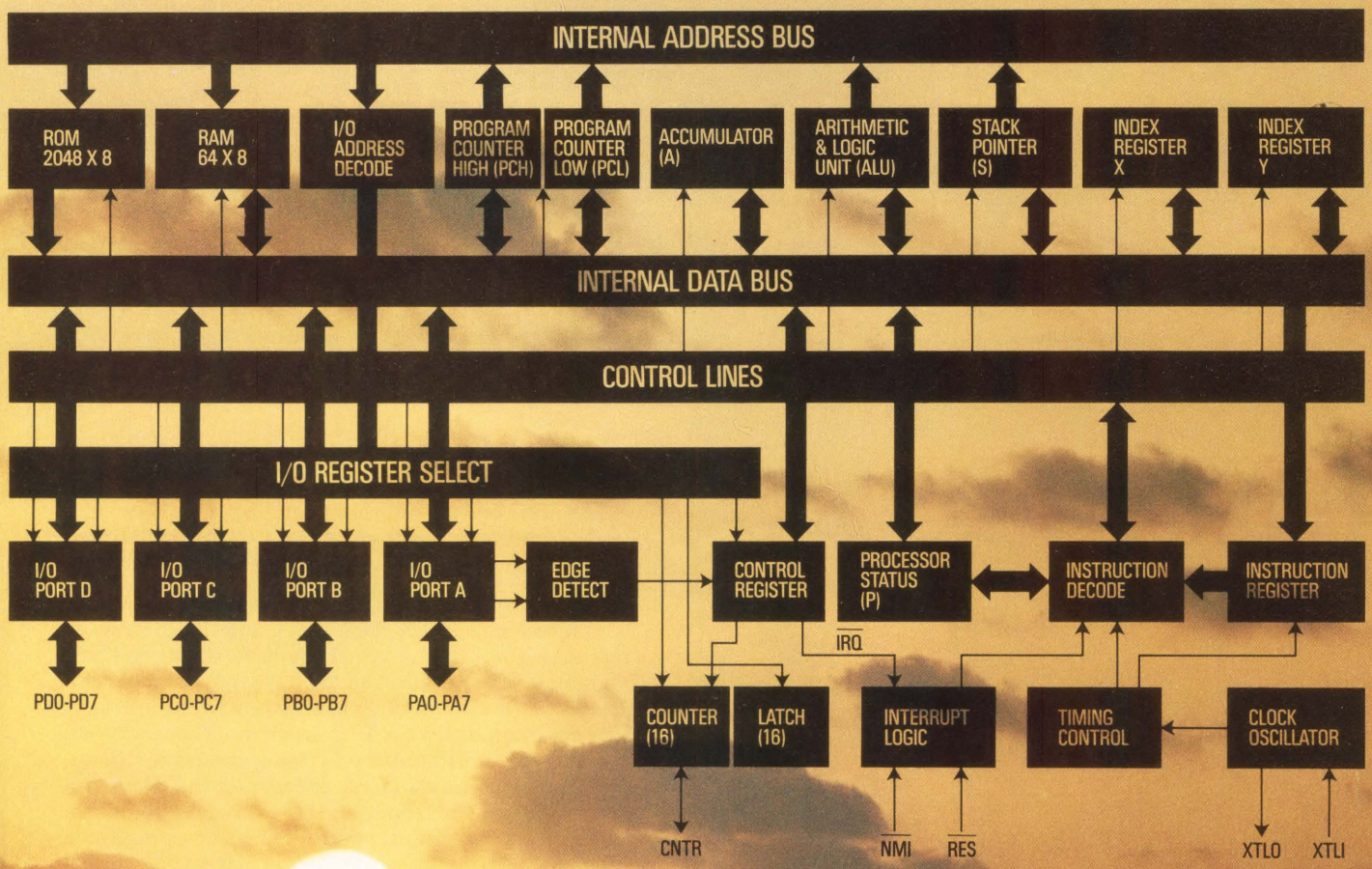
It all adds up to a user-oriented 5216 color system that is a reliable, flexible and economical solution to your graphics and image processing needs. Quicken your draw with Aydin, the industry leader in high-resolution, intelligent color graphics. For more information, contact Aydin Controls, 414 Commerce Drive, Fort Washington, PA 19034. Tel.: 215-542-7800. (TWX: 510-661-0518.)

Leadership Features:

• High-performance multiprocessor bus architecture • Pixel or graphic DMA block mode data transfer (800 nanoseconds per 16-bit pixel) • Multiple pixels per word • Wide selection of display formats up to 1024 x 1024 x 16 • Video processing through lookup table RAM at bit rates to over 40mHz • High-speed hardware vector and character generation • Four sizes of alpha characters • High-speed hardware math • Both parallel and serial peripheral interfaces available • User programmable • 16-Bit microprocessor.

AYDIN CONTROLS

CIRCLE 83 ON INQUIRY CARD



The 6500/1 One-Chip Micro. First, look what it's got. Then, look what it costs.

$10.50 at 1,000. And there's more good news. No masking charge for the on-board 2K x 8 programmable ROM. And, the MOS 6500/1 is available in either 1MHz or 2MHz versions.

Here's what you get. A microcomputer on a chip. The 8-bit NMOS 6502 CPU, software compatible with your existing 6502 programs. Four I/O ports (32 bi-directional lines). One bi-directional counter line. On-board clock. 2048 x 8 ROM. 64 x 8 static RAM. Your choice of a 1MHz or a 2MHz internal clock. 16-bit programmable counter/latch with four modes. +5V supply. And more. All, on a 40-pin DIP. Plastic or ceramic.

Good old 6502. Simple to program. Familiar. Which means you write software in weeks. Instead of months. And, the 6500/1 is the microcomputer on a chip with software compatibility with its host CPU.

Prototyping? Simple. Build your prototype system with PROMs before committing to mask-programmed production. Our 64-pin prototyping part, the 6500/1E emulator includes all 6500/1 interface lines and brings all internal memory address, data and control lines off-chip. There's even a 40-pin configuration in piggy-back EPROM.

Delivery now. 1MHz or 2MHz. Take your pick. Develop your system, provide us with final ROM masking program and we'll have your 6500/1 μC's back to you in five weeks. And yes, there are second sources.

More information? Call us. Or, mail us the coupon below. We'll have data sheets on the way to you. Pronto.

commodore
SEMICONDUCTOR GROUP

MOS TECHNOLOGY
950 Rittenhouse Rd.
Norristown, PA 19403
(215) 666-7950

Frontier Manufacturing Inc.
2955 N. Airway Ave.
Costa Mesa, CA 92626
(714) 979-6300

Optoelectronics, Inc.
4350 Beltwood Parkway So.
Dallas, TX 75234
(214) 387-0006

Eastern Regional Office
950 Rittenhouse Rd.
Norristown, PA 19403
(800) 345-6386 Toll Free
TWX 5106604168

Western Regional Office
3330 Scott Blvd.
Santa Clara, CA 95050
(408) 727-1130

Central Regional Office
4350 Beltwood Parkway So.
Dallas, TX 75234
(214) 387-0006
TLX 730-969

Gentlemen. Please send me complete information on the MOS 6500/1 computer on a chip. ☐ Include data on your line of 6500 support chips.

Name _____

Address _____

City _____ State _____ Zip _____

CIRCLE 84 ON INQUIRY CARD

SEMICONDUCTOR MEMORY UPDATE: EEPROMs

Electrically erasable programmable ROMs, combining the best features of both ultraviolet erasable and electrically alterable types, are likely to be the real impetus of the future

by Eugene R. Hnatek

Ever since the microprocessor was introduced, the amount of memory accompanying the system has been increasing dramatically. Semiconductor manufacturers are responding by concentrating on the development of memories with increased storage density, performance (speed and power), and flexibility, and on the nonvolatility, ease of use, and interchangeability of memory device types. As such there exist many competing technologies and memory types for design sockets, ie, more than one way (or one type of memory that can be used) to effect a viable system design. Microprocessors and dynamic random access memories that are currently available and forthcoming (ie, the leading edge products) are expanding the capabilities of the processing technology that developed during the 1970s. Many manufacturers are "phasing in" more sophisticated mask generation and testing equipment, to be ready for the next generation of devices.

The scaling down needed for very large scale integration requires the fabrication of submicron devices in production quantities. Substantial development work is required to solve problems of accurate alignment and exposure of circuit patterns, the etching process and metallization, and the formation of reliable interconnections of submicron widths. Techniques that employ submicron patterning with direct writing electron beams and X-ray lithography are under investigation. Concurrently, many manufacturers are scaling down existing parts with improved processes that cut silicon chip sizes, and then passing on the savings to their customers.

Competition among semiconductor manufacturers intensifies in proportion to the size and importance of the market. Rapid technological change and significant price reductions, which characterize the semiconductor industry, do not necessarily lower production costs. U.S. semiconductor firms have been joined recently by foreign competitors eager to establish a foothold in the market. The Japanese have entered the memory market with a sense of determination and dedication that is seen as part of a strategy to win a commanding share of the world computer market. This has heavily impacted U.S. manufacturers and has changed the lineup of frontrunners in several crucial product areas. As a result, all U.S. memory manufacturers have had to refine their strategies and pay more attention to quality control—for the good of all users.

Since the previous update on semiconductor memory[1] was published, a myriad of product developments and innovations has taken place, making it a monumental task just to keep abreast of the daily changes in the memory marketplace. Bewildered by a barrage of product announcements, which include some product retractions as well, design engineers are finding it difficult to choose the memory best suited to their applications. By building on the earlier update and focusing on the developments that have occurred since then (early 1980), this discussion seeks to ease the designer's task of choosing a memory type or part for a particular application. Some of the key developments that have taken place or have been under way since that time are listed (not in order of

Eugene Hnatek is vice president and general manager of Viking Laboratories, 440 Bernardo Ave, Mountain View, CA 94043. Prior to this, he held management positions at several other companies in the semiconductor industry. An authority on ICs, Mr Hnatek has published six books and more than 100 articles on the subject. He received BSEE and MSEE degrees from Bradley University.

The scope of Mr Hnatek's discussion precludes its publication in a single article—or even two. Full coverage requires a book, which is now under way. In the interim, one chapter of that book, a discussion of EEPROMs and EAROMs, is presented here; next month *Computer Design* will publish a second chapter, which examines dynamic RAMs and Japanese DRAM reliability.

Recent product developments

- 16k DRAMs* achieved commodity (high volume) status.
  - —They experienced severe price erosion as competition increased.
  - —Japanese suppliers captured 40% of the market.
- 64k DRAM finally began its production cycle.
- 256k DRAM entered the development/prototype stage.
- 16k UVEPROM achieved commodity status and experienced severe price erosion as competition increased.
- 32k UVEPROM began its production cycle.
- 64k UVEPROM began its preproduction cycle.
- 128k UVEPROM was introduced.
- 16k and 32k EEPROMs were introduced and began their preproduction cycle.
- 16k bipolar P/ROM achieved full production status.
- 32k and 64k bipolar P/ROMs were introduced and began their preproduction cycles.
- 64k ROM achieved production status.
- 128k ROM was announced and became available in sample quantities.
- 256k and 512k bytewide MOS ROMs are under development.
- 256k, 512k, and 1M-bit MOS ROMs were introduced by Japanese suppliers for Kanji character generation.
- 4k SRAM achieved full production status in both NMOS and CMOS technologies.
- Bytewide 16k SRAMs were introduced in both NMOS and CMOS technologies.
- 64k SRAMs were under development.
- CMOS UVEPROMs were introduced on a preproduction basis.
- 4k ECL RAMs achieved production status.
- Three major magnetic bubble memory suppliers—Rockwell, Texas Instruments, and National—dropped out of the market.
- CMOS became a viable and competing LSI/VLSI technology and is competing with NMOS.

DRAM— dynamic random access memory
UVEPROM—ultraviolet erasable programmable read only memory
EEPROM— electrically erasable programmable read only memory
P/ROM— programmable read only memory
ROM— read only memory
MOS— metal oxide semiconductor
SRAM— static random access memory
NMOS— n-channel metal oxide semiconductor
CMOS— complementary metal oxide semiconductor
ECL— emitter coupled logic
RAM— random access memory

*Acronyms used in this list are defined separately at the end.

importance) in the Panel, "Recent product developments."

EEPROMs

Electrically erasable programmable read only memories (EEPROMs) offer many advantages. They allow either bulk erasure or erasure and programming of individual bytes while in the printed circuit board socket. They also allow realtime program changes, have reasonable speed for reading data, and are programmed more easily and quickly than ultraviolet erasable programmable read only memories (UVEPROMs), using a low 20-V supply (40 s for 2k EEPROM vs 1800 s for UVEPROM). EEPROMs are easy to test and are nonvolatile. Most important, they are encased in inexpensive packages. At present, they cost eight to ten times more than comparable density UVEPROMs. However, as more sockets come on board and production increases, prices should come down to a level competitive with UVEPROMs.

Because of this programming flexibility and potentially low cost, UVEPROMs will supersede electrically programmable read only memories (EPROMs) within the next three to four years. 1981 saw the widespread availability of reasonable density [16k-bit (2048 x 8)] electrically erasable memories. Intel and Hitachi have already announced 16k devices based on different technologies, and a new Santa Clara company, Weitek, just introduced a 4k x 8 EEPROM. Hitachi is using the complex silicon nitride (MNOS, ie, metal nitride oxide semiconductor) n-channel technology, while Intel has opted for its proven floating gate tunneling n-channel metal oxide semiconductor (NMOS) technology. Hughes, meanwhile, is offering 4k and 8k EEPROMs based on complementary metal oxide semiconductor (CMOS) technology. In addition, Motorola, National Semiconductor, Mostek, General Instrument (GI), and others are preparing to join the foray.

Technologies. EEPROMs have evolved from two different technologies. The more mature technology, MNOS, is unlike today's dominant semiconductor technologies, bipolar and metal oxide semiconductor (MOS). The newer technology, on the other hand, is similar to the floating gate MOS technology used in UVEPROMs. MNOS technology, invented by National Cash Register (NCR) in the early seventies, has been generally rejected as a high volume technology primarily because of manufacturing difficulties. However, GI and Japanese manufacturers have mastered the technology and support it. Floating gate MOS (also known as FAMOS) was developed in the mid-seventies by Intel and was quickly accepted as the technology for UVEPROMs. Within the last two years, FAMOS has been refined into an electrically erasable technology and has found a number of supporters, mostly in the United States.

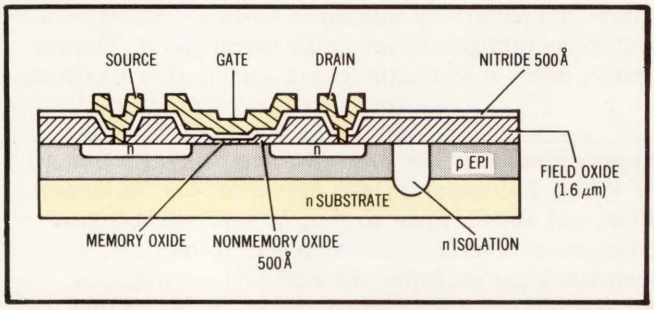


Fig 1 Cross section of n-channel MNOS transistor. Charges tunnel through charge storage layer (nitride) and thin gate oxide. Most of today's devices use a p channel

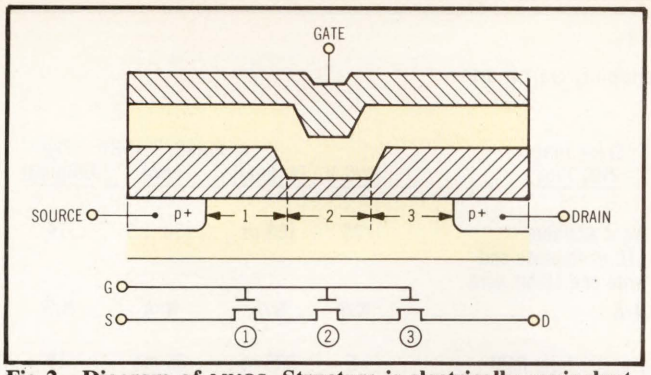


Fig 2 Diagram of MNOS. Structure is electrically equivalent to three MOS transistors connected in series, but with common gate. Transistor 2 controls overall characteristics

Nonvolatility requires charge to be stored, and the two technologies differ in their charge storage mechanisms. MNOS captures charge at trap sites within a nitride layer, while FAMOS stores charge on a polysilicon gate floating in or surrounded by a sea of silicon dioxide. Both technologies rely on a tunneling mechanism to move the charge from the substrate to the storage region. Fig 1 shows the cross section of a typical MNOS transistor. Because of the extremely thin oxide under the gate, one MNOS transistor can be modeled as three MOS transistors connected in series but with the gates in parallel (Fig 2). The central transistor—the one with the thin gate oxide (Fig 2)—is the storage transistor and influences the overall characteristics of the device.

In the erased mode, the nitride layer under the central transistor is charged negatively by applying a 25-V signal to the gate, relative to the substrate. This causes electrons from the substrate to tunnel through the thin oxide of the central transistor (but not through the thicker oxides of the peripheral transistors) and become trapped in the nitride. The central transistor then turns on because the trapped electrons induce a p channel in the substrate, and it stays on even after the erasing voltage is removed since the electrons are trapped. The threshold voltage of the composite (V_E) is therefore the threshold voltage of the peripheral field effect transistors.

Writing is the inverse of erasing. A large negative voltage applied to the common gate induces a positive trapped charge and, therefore, a negative shift in the threshold voltage of the central transistor. Since turning on the central transistor requires a more negative voltage than is required to turn on the peripheral transistors, the threshold voltage of the composite structure in the written state (V_W) is equal to the threshold voltage of the central transistor. This means that the state of the MNOS transistor (whether written or erased) can be detected by examining voltages V_W and V_E.

The storage cell of an MNOS EEPROM consists of an MNOS storage transistor and a detector, the detector often being another MOS field effect transistor. Such a 2-transistor cell sacrifices packing density but improves data retention (over a single-transistor cell) because it detects the difference between V_W and V_E, rather than their absolute values, which may change in time. Hitachi was the first to offer an n-channel MNOS EEPROM, the HN48016. GI is also switching from p-channel to n-channel MNOS technology.

Floating gate EEPROMs, unlike MNOS devices, which trap charge in a nitride layer under the gate, store charge on the gate itself. This requires the gate to be isolated from both the substrate and the control voltage supply lines. Isolation from the substrate is achieved by surrounding the gate with silicon dioxide. Control voltages are coupled capacitively via a second layer—Intel uses polysilicon and Hughes uses a metal. Fig 3(a) and (b) show cross-sectional views of the Intel and Hughes parts, respectively. Both parts rely on Fowler-Nordheim tunneling to move the charge to be stored from the substrate to the gate. As in MNOS, the gate oxide is locally thinned to aid in tunneling. But unlike MNOS, whose oxide thickness must be less than 100 Å, both Intel's and Hughes's floating gate devices use oxide about 200 Å thick. UVEPROMs do not rely on direct tunneling. Instead they use avalanche injection to put charge onto the floating gate.

Besides the difference in control-line material (Intel uses polysilicon and Hughes uses an aluminum nitride sandwich), there are differences in construction. Intel uses a regular p substrate for its NMOS cells, while Hughes starts with an n substrate and sinks a large p well into it for the entire memory array. Hughes makes p-channel devices (needed for the CMOS peripherals) directly in the n substrate. Another difference is in the location of the thin-oxide tunneling path. Intel's thin oxide is situated directly over a drain, a heavily doped n+ region. Hughes locates the tunneling path directly over the p-well channel region. This has important implications. Intel can erase a cell by grounding the control line and connecting the drain to a positive supply. Electrons stored in the gate then jump the gap to the drain. This procedure can essentially be followed a cell at a time. In contrast, since Hughes's tunnel path is over the channel region, erasure (or removal of stored electrons from the gate) can be carried out only by raising the potential of the entire p well. Unfortunately, this means that all cells are erased simultaneously.

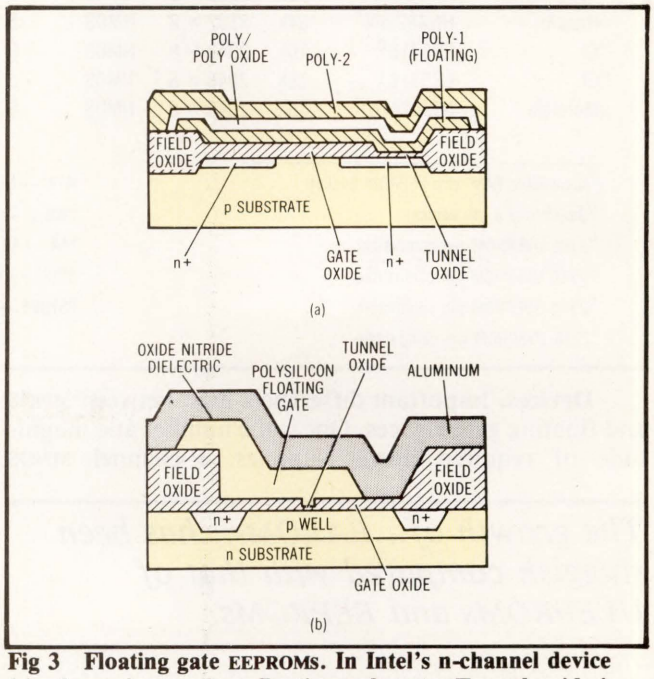


Fig 3 Floating gate EEPROMs. In Intel's n-channel device (a), charge is stored on floating poly-gate. Tunnel oxide is located over n+ drain region. Hughes's device (b) also stores charge on floating poly-gate, but tunnel oxide is situated over channel region. Location of this oxide affects erasability

TABLE 1

Selected EEPROM Availability Summary

Manufacturer	Part No	Density	Org	Technology	Power Supply (V)	Erase Time/ PWG Time	PWG V	TAA(max)	PDISS/PSTDBY (mW)	Pkg DIP(pins)
Motorola	MCM2801	256	16 × 16	NMOS	5	Word alterable 110 ns to erase and write one 16-bit word	25	168 µs	150/1.5	14
Panasonic	MN1218	272	16 × 16	NMOS	±5, -28	N/A	N/A	N/A	N/A	N/A
Xicor[a]	X2210	256	64 × 4	NMOS	5	Transfer from RAM to EEPROM 5 ms	5	300 ns	35 mA	18
	X2212	1k	256 × 4	NMOS	5	" "	5	300 ns	50 mA	18
	X2201	1k	1024 × 1	NMOS	5	" "	5	250 ns	275	18
SGS-ATE[b]	M120	1k	256 × 4	CMOS	5		20	450 ns	300 read 400 modified	18
GI	AR5304[a]	4k	512 × 8	NMOS	5	Transfer from RAM to EEPROM	N/A	300 ns	N/A	24
NCR	NCR4485[a]	4k	512 × 8	MNOS	5	Transfer from RAM to EEPROM	±22	250 ns 450 ns	600 600	28
Hughes	HNVM3004	4k	512 × 8	CMOS	5	Bulk alterable; byte erasure = 100 µs; programming = 100 µs/byte; entire array erase and rewrite = >0.1 s.	17	600 ns	10 mW/50 µW	24
Hughes	HNVM3008	8k	1024 × 8	CMOS	5	Bulk alterable; byte erasure = 100 µs; programming = 100 µs/byte; entire array erase and rewrite = 0.1 s.	17	600 ns	10 mW/50 µW	24
Harris	HM6808[c]	8k	1024 × 8	CMOS	5			350 ns	50mW/500 µW	24
Hitachi	HN48016[d]	16k	2048 × 8	NMOS	5	Byte and bulk erasable; programming = 10 ms/byte; erase time = 1 s all bits	25	350 ns	300	24
Intel	I2816[d]/2815	16k	2048 × 8	NMOS	5	Bulk erasure: Erase/write time = 10 ms/ bit; any of 2k bytes can be erased and rewritten in 20 ms	21	450/ 250, 350ns	600/ 300	24
National	NMC2816[d]	16k	2048 × 8	NMOS	5			350 ns	450/125	24
Hitachi	HN482764[e]	64k	8192 × 8	NMOS	5			N/A	N/A	28
GI	ER5716[d]	16k	2048 × 8	NMOS	5	Word/bulk	25	300	N/A	24
GI	ER5816[f]	16k	2048 × 8	NMOS	5	Word/bulk	25	300	N/A	24
Motorola	MCM2816[d]	16k	2048 × 8	NMOS	5	Erase and rewrite time = 50 ms	N/A	350, 450 ns	N/A	24

[a] Nonvolatile RAM with EEPROM backup
[b] Developing a 4k version
[c] 2708 UVEPROM pin compatible
[d] 2716 UVEPROM pin compatible
[e] 2764 UVEPROM pin compatible
[f] 2816 UVEPROM pin compatible

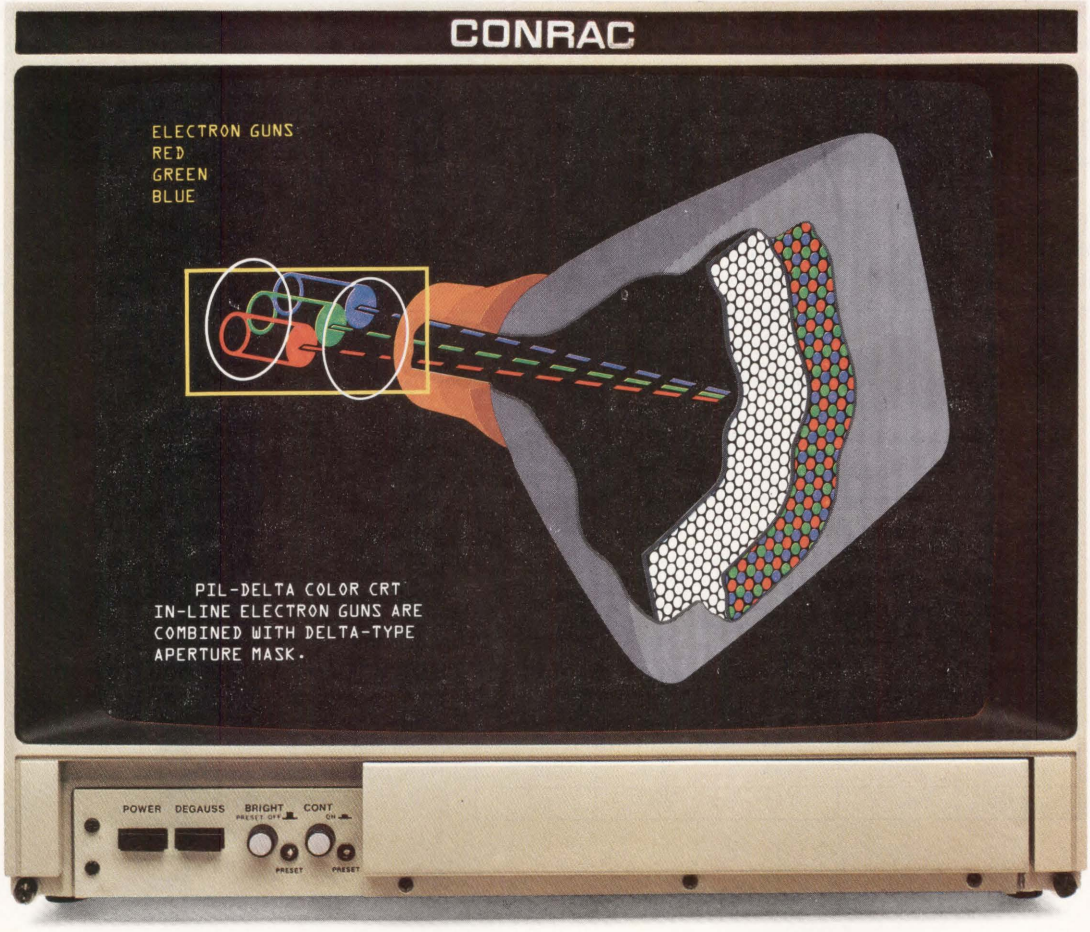
N/A — Not available
PWG V — Programming voltage
TAA — Address access time
PDISS — Operating power dissipation
PSTDBY — Standby power dissipation

Devices. Important differences exist between MNOS and floating gate devices. One is the number and magnitude of required power supplies. P-channel MNOS devices require three power supplies (5, −4, and −24 V, for example); the Hitachi n-channel MNOS EEPROM requires only two supplies—5 V for reading and 25 V for programming and erasing. Floating gate devices also use only two voltages, 5 V for read and a higher voltage for program/erase. In general, this higher voltage is lower than the programming voltage for MNOS devices. Intel uses 20 V and Hughes needs 17 V, for example.

The growth of...EAROMs...has been sluggish compared with that of UVEPROMs and EEPROMs.

In terms of speed, floating gate devices are superior to p-channel MNOS devices but are on a par with n-channel MNOS. Older p-channel MNOS devices, at best, took a microsecond or so to read, but their n-channel versions take less than half that time. Hitachi's 16k device, for example, can be read in 250 ns (max). Both floating gate

HIGH RESOLUTION WITHOUT COSTLY RE-CONVERGENCE. ANOTHER AMERICAN FIRST.



CONRAC

Conrac's precision in-line gun eliminates color re-convergence—the most expensive monitor maintenance procedure.

A lot of monitors can deliver beautiful high resolution pictures. But in conventional delta-gun construction, the color beams can drift out of convergence. In high resolution color graphics, that can give you an illegible image. A skilled technician must be called in to re-converge the monitor.

Of all the leading monitors today, only the new Conrac 7200 can give you a high resolution picture without these costly re-convergence problems. That's because Conrac teamed its high resolution circuitry with a precision in-line gun tube.

Precision in-line guns are, simply, more stable than delta guns. That one difference makes a big difference to you and your customers. You reduce your cost of product support, and your customer gets a product that lives up to its promise.

High resolution color. No convergence problems. It's the Conrac 7200 Series.

Find out more about all the new Conrac monitors. And ask us for details on price and delivery.

Conrac Division
Conrac Corporation
600 North Rimsdale Avenue
Covina, CA 91722
Telephone (213) 966-3511
Telex: 67-0437

Conrac Elektron, GmbH
Postfach 60m Industriestrasse 18
D 6992 Weikersheim
Federal Republic of Germany
Telefon 0 79 34/70 71
Telex: 07 4231 elecon

CIRCLE 85 ON INQUIRY CARD

and MNOS memories must go through an erase cycle before they can be programmed. All MNOS devices except Hitachi's can be byte- or block-erased. Among the floating gates, Intel's part can be byte-erased, but the Hughes part can only be block-erased.

Table 1 summarizes the EEPROMs currently available in both MNOS and CMOS technologies. Also included in this table are the Xicor series of NOVRAMs® (nonvolatile random access memories), static RAMs that are overlaid bit for bit with EEPROM backup and that combine the speed of static RAMs with the nonvolatility of EEPROMs. This family of devices allows virtually any kind of microprocessor based system to electrically alter nonvolatile data without the need for high programming voltage, ultraviolet light source, or unsocketing—a single 5-V supply will both erase and rewrite system firmware from a single word to an entire program. (These devices are discussed in References 1 and 2.)

In the future, EEPROMs and EAROMs (electrically alterable read only memories), as well as other memories, will include some intelligent features: built-in timing for their own erase and write operations and for alerting the microprocessor that erase.and write operations are complete; address and data latching; and the like. High density 4k x 8 and 8k x 8 EEPROMs with enhanced performance features (speed and power) will develop at a frantic pace, using both NMOS and CMOS technologies.

Pinout standardization

Pinout standards similar to those that have existed for years for bipolar programmable read only memories (P/ROMs) are being developed for UVEPROMs, read only memories (ROMs), bytewide static RAMs, and EEPROMs, and for interchangeability between these functional circuit components, in order to aid design engineers as their system memory requirements vary. Table 2 shows the Mostek pinout interchangeability approach as an example.

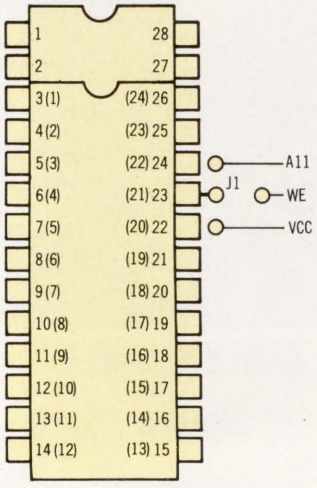
EAROMs

The growth of electrically alterable ROMs (EAROMs) has been sluggish compared with that of UVEPROMs and

TABLE 2

Mostek's Bytewide Static Memory Family

Memory Type	Part Number	Capacity	Package	Jumper J1
ROM	MK34000	2k × 8	24-pin	NC
ROM	MK37000	8k × 8	28-pin	A11
ROM	MK38000	32k × 8	28-pin	A11
RAM	MK4802	2k × 8	24-pin	WE
RAM		4k × 8	28-pin	A11
RAM	MK4118A 4801A	1k × 8	24-pin	WE
UVEPROM	MK2716	2k × 8	24-pin	VCC
UVEPROM	MK2764	8k × 8	28-pin	A11



4118A 4801A	4802	34000	2716	4k × 8	37000	38000	2764	2764	38000	37000	4k × 8	2716	34000	4802	4118A 4801A
				NC	NC	A14	NC	VCC	VCC	VCC	VCC				
				NC	A12	A12	A12	NC	NC	NC	WE				
A7	A7	A7	A7	A7	A7	A7	A7	NC	A13	NC	NC	VCC	VCC	VCC	VCC
A6	A6	A6	A6	A6	A6	A6	A6	A8	A8	A8	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	A5	A5	A5	A9	A9	A9	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	A4	A4	A4	A11	A11	A11	A11	VPP	NC	WE	WE
A3	A3	A3	A3	A3	A3	A3	A3	OE VPP	OE	OE	OE	OE	OE	OE	OE
A2	A2	A2	A2	A2	A2	A2	A2	A10	A0	A10	A0	A10	A10	A10	NC
A1	A1	A1	A1	A1	A1	A1	A1	CE	CE	CE	CE	CE	CE	CE	CE
A0	A0	A0	A0	A0	A0	A0	A0	D7	D7	D7	D7	D7	D7	D7	D7
D0	D0	D0	D0	D0	D0	D0	D0	D6	D6	D6	D6	D6	D6	D6	D6
D1	D1	D1	D1	D1	D1	D1	D1	D5	D5	D5	D5	D5	D5	D5	D5
D2	D2	D2	D2	D2	D2	D2	D2	D4	D4	D4	D4	D4	D4	D4	D4
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	D3	D3	D3	D3	D3	D3	D3	D3

Parentheses indicate pin number of 24-pin packages
24-pin devices are lower justified in pins 3 through 26 of 28-pin socket

MORROW DESIGNS

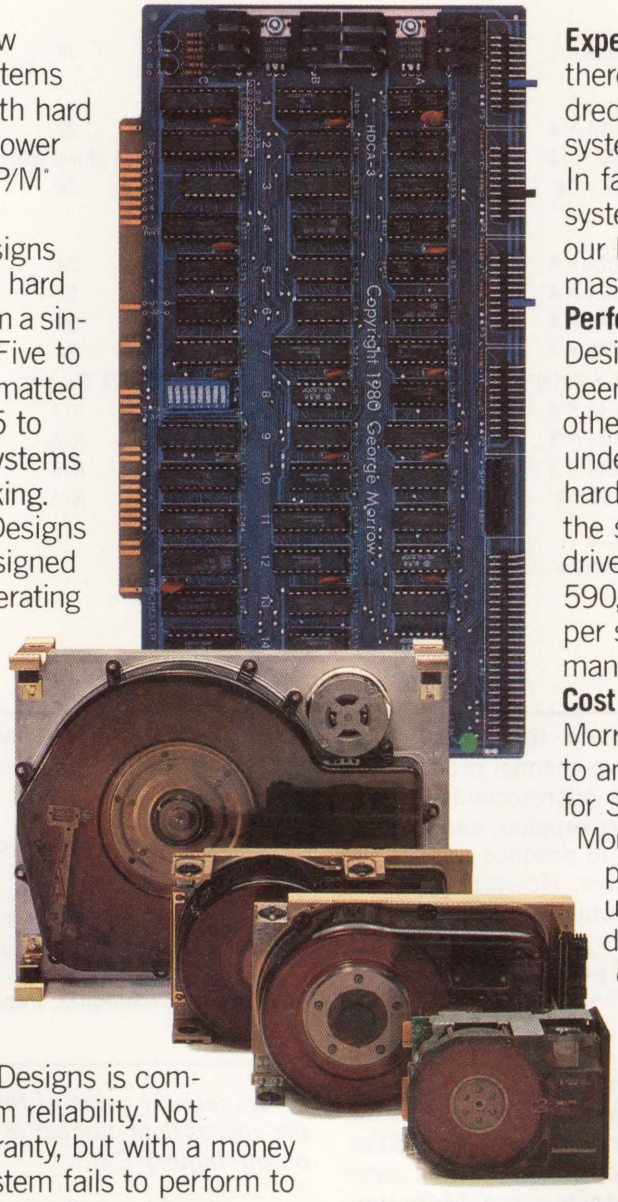
Now, Complete 5¼" System 5 Mbytes $2,495

Leading edge technology in hard disk systems.

Complete systems. Morrow Designs hard disk subsystems are delivered complete with hard disk, controller, cabinet, power supply, fan, cables and CP/M* 2.2 operating system.

Widest range. Morrow Designs offers the widest range of hard disk systems available from a single supplier. 5¼", 8", 14". Five to over 100 megabytes of formatted hard disk storage. $2,995 to $17,980. Cost effective systems that work. And keep working.

S-100 and more. Morrow Designs hard disk systems are designed for use with the CP/M operating system. Available software packages allow our systems to run on any IEEE696/S-100 Standard system with no hardware modification. Plus, Cromemco,*** North Star,** Vector Graphics, Godbout, Dynabyte, Exidy,**** IMSAI, Micromation, Processor Technology and California Computer Systems.



Reliable systems. Morrow Designs is committed to hard disk system reliability. Not simply with a 90-day warranty, but with a money back guarantee. If our system fails to perform to specification, send it back. We'll send back your money.

Experience. As of April, 1981, there were over fifteen hundred Morrow Designs hard disk systems successfully installed. In fact, over 200 independent systems integrators now use our hard disks to solve their mass storage problems.

Performance answers. Morrow Designs hard disk systems have been benchmarked against all other systems. None is faster under CP/M. Morrow Designs hard disks operate at 10 times the speed of a floppy disk drive. Transfer rates range from 590,000 bytes to 900,000 bytes per second. That kind of performance can become addictive.

Cost effective answers. Compare Morrow prices and performance to anything presently available for S-100 systems. You'll find Morrow's price/megabyte/performance ratio to be unmatched. Leadership in disk systems technology earned us leadership in price/performance. And that may have earned us a call from you. Circle the Reader Service Number for our full line data sheets. Can't wait? Call us at (415) 524-2101. And yes, OEM quantity prices are available. **LOOK TO MORROW FOR ANSWERS.**

MORROW DESIGNS

5221 Central Avenue, Richmond, CA 94804
(415) 524-2101

*CP/M is a trademark of Digital Research.
**Northstar is a trademark of North Star Computers, Inc.
***Cromemco is a trademark of Cromemco, Inc.
****Exidy is a trademark of Exidy Corporation.

CIRCLE 86 ON INQUIRY CARD

TABLE 3

Commercially Available EAROMS (MNOS)

Manufacturer	Part No	Organization	Max Access Time	Alterability	Pkg DIP (pins)	Power Supply (V)	Max PDISS (mW)
Toshiba	TMM142P	256 × 4	1.5 μs	RAM with EAROM Storage	18	5 - 15	800
GI	ER1711	256 × 4	900 ns	RAM with EAROM Storage	22	5, -12	650
Nitron	NC7033	21 × 16	10 μs first bit (serial data)	Word	8	10	28 (typ)
Nitron	NC7055	64 × 8	4 μs	Word	22	5, -28	400
GI	ER2055	64 × 8	2 - 4 μs	Word (6-bit binary addressing)	22	5, -28	500
Nitron	NC7051	1024 × 1	4 μs (serial data)	Word (5-bit parallel binary)	28	5, -28	400
Nitron	NC7451	1024 × 4	900 ns	Word	22	5, -12	450
GI	ER1400	100 × 14	833 μs (serial)	Word	14 (drives MOS)	-35	300
GI	ER2050/51	32 × 16	1 - 2 μs	Word (5-bit parallel binary)	28	5, -28	500
GI	ER2401/02[b]	1024 × 4	2 μs	Chip	24	±5, -14	300
GI	ER3400[c]	1024 × 4	900 ns	Word/bulk	22	5, -12, -30	450
Nitron	NC7810	2048 × 4	1.4 μs	Chip	24	±5, -24	250
GI	ER2810	2048 × 4	1.6 μs	Chip	24	5, 24	300
GI	ER4201[a]	128 × 8 (1k)	450 ns	Word/bulk	24 TTL comp	5, 24	400
NCR	NCR2811	2048 × 4	N/A	N/A	N/A	N/A	N/A
NCR	NCR2161	2048 × 8	N/A	Byte	N/A	N/A	N/A
NCR	NCR2168	2048 × 8	N/A	Block	N/A	N/A	N/A
NCR	NCR1734	256 × 8	N/A	N/A	N/A	N/A	N/A

[a] Automatic erase/write command for microprocessor control

[b] 2402 has output data strobe

[c] CE used as clock

EEPROMs. The reasons for it are the difficulty of working with the silicon nitride p-channel process, the inherently slow access times—in microseconds, the requirement for dual polarity power supplies, and the failure of several sources of supply to produce a sufficient number of different memory sizes. However, GI—one of the pioneers of EAROM technology—is switching the n-channel technology to obtain devices with shorter read times but retaining its metal gate approach. Table 3 summarizes currently available EAROM products.

Conclusion

Within the next year, the 64k UVEPROM will shift from preproduction to full production status. This places the viability of the 32k UVEPROM in serious question, since both the 32k and 64k were introduced about the same time and thus have the same learning curve. More suppliers can be expected to announce 128k (16k x 8) UVEPROMs as a follow-up to Texas Instruments' TMS 2528. Also, within the next two years, UVEPROMs with "double byte wide," or x16 output, configurations to support the 16-bit microprocessor can be anticipated. However, the real impetus of the future, based on user acceptance and ease of use, will be the EEPROM, at the expense of the high volume UVEPROM and EAROM—combining the best features of each.

References

1. E. R. Hnatek, "Semiconductor Memory Update," *Computer Design*, "Part 1: ROMs," Dec 1979, pp 67-77; "Part 2: RAMs," Jan 1980, pp 119-131; "Part 3: High Density Technologies," Feb 1980, pp 147-159
2. J. Drori et al, "A Single 5-V Supply Nonvolatile Static RAM," 1981 IEEE ISSCC Digest of Papers, Session 12: Memory Techniques, Paper 12.1

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 704 *Average 705* *Low 706*

Brilliance, Intelligence and Economy in One High Resolution Terminal.

RAISE YOUR GRAPHICS STANDARD!

Price/performance you couldn't get before in a high resolution raster terminal no matter how far up you climbed—it's yours in the Genisco G-1000.

The G-1000 high resolution (1024 x 792) desk top terminal offers extraordinary brilliance and contrast with full raster erasability, *plus* the intelligence of a Z-8001 microprocessor and 16K each of RAM and PROM. The price is less than $9,000 in OEM quantities.

What you get for your money is the industry's only true raster replacement for the Tektronix 4014-1 terminal (plug to plug and software compatible) and a no-end-in-sight expandable, fully programmable tool for CAD/CAM, plot previewing, mapping and many other present and future applications.

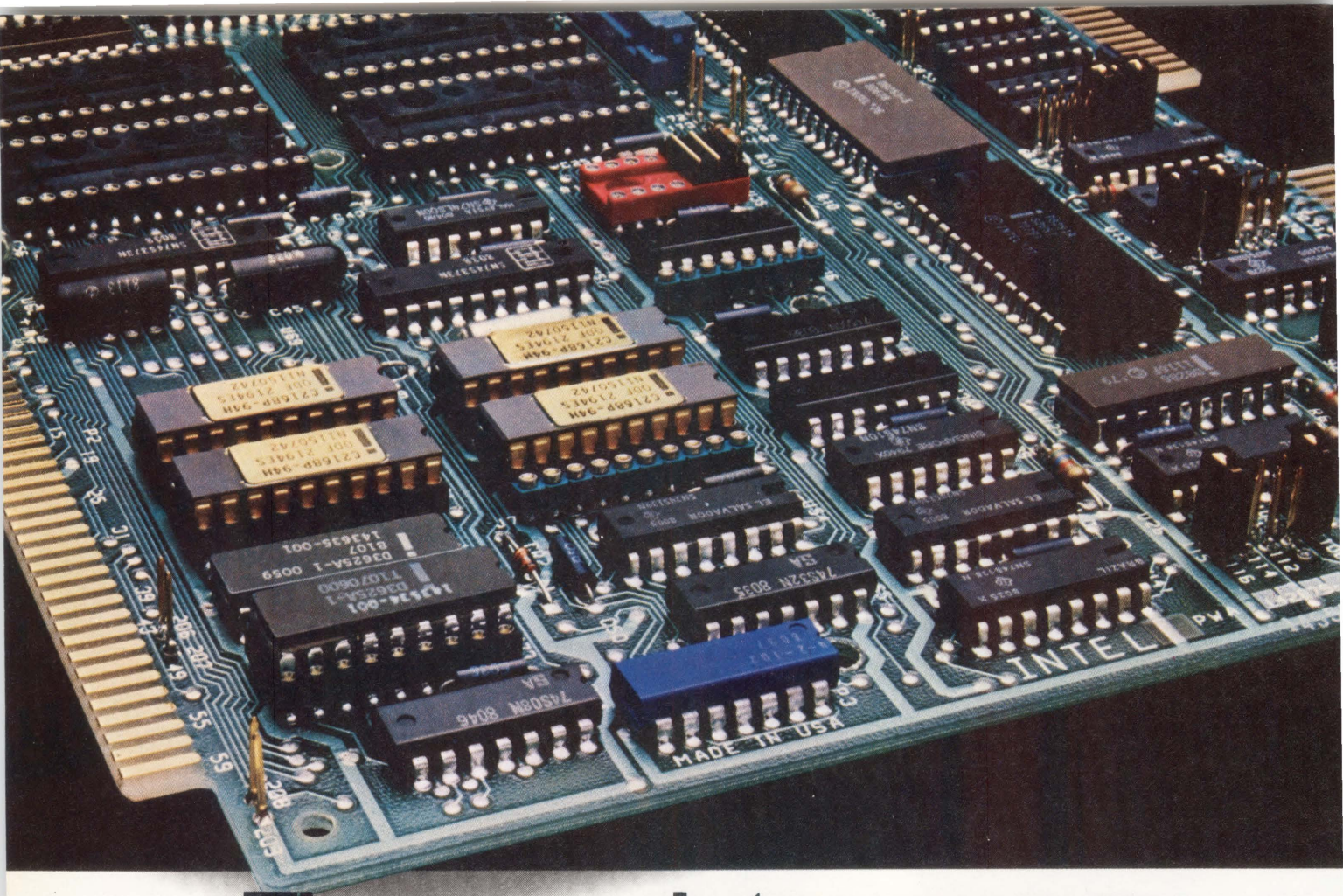
Expand your G-1000 capability with an optional alphanumeric overlay and memory to 512K bytes RAM and 32K PROM for distributed processing applications. Attach a graph tablet and/or one of several hard copy devices.

No matter how you look at it, it comes out on top.

Raise your graphics standard. Call or write for a G-1000 brochure to Genisco Computers Corporation, 3545 Cadillac Avenue, Costa Mesa, CA 92626, (714) 556-4916.

Genisco
GENISCO COMPUTERS CORPORATION

CIRCLE 87 ON INQUIRY CARD



There are only two reasons to use our new 16-bit microcomputer. Money and power.

Let's assume you've already realized the advantages of designing a system with an OEM microcomputer board. Like faster design cycles. Lower production costs. And faster time to market.

That's great. Now you're down to two basic choices. You can buy a ten-year old minicomputer architecture in pieces. Cheap.

Or you can go VLSI all the way. With a much newer, much more powerful microcomputer architecture. And fortunately, we've made this second choice a lot easier to afford.

Because we're introducing our new iSBC™ 86/05 board. Which only costs $1,195 in quantities of 100 or more. And gives you four times the Whetstone power of a low-end minicomputer. Or up to 20 times more when you add our iSBC 337 Numeric Data Processor. In fact, this solution gives you 110,000 Whetstones, which rivals the performance of mid-range minicomputers. And makes this the fastest numeric microcomputer in the world.

And since this is the only board with our 8/16 bit iSBX™ Multimodule connectors, you can add more processing power, digital or analog I/O processing, and even floppy disks or bubbles. At about half the cost you're used to. With our Multimodules, you can add EPROMs and E²PROMs, too. And thanks to our iSBC Multibus® architecture (IEEE P796), when your application calls for multiprocessing, you're not locked into a uniprocessor solution.

You won't exactly feel limited by the software, either. Because the iSBC 86/05 board is software compatible with our industry standard iSBC 86/12A board. Which means it works with our iRMX™ 88 executive and our iRMX 86 operating system, both of which we designed to handle real time multitasking applications. Even better, because of our modular software structure, you can customize and extend both of these packages to fit your particular application perfectly, whether it's in process control, or business data processing.

So look at the speed. The power. The range of features and options. Put all that together and you're looking at a whole new price/performance standard. Which should give you two very nice things to count on.

More money. And more power.

Get in touch with us now and we'll tell you more. Write Intel, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call us at (408) 987-8080.

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L. A. Varah, Wyle Distribution Group, Zentronics.

intel® delivers solutions

CIRCLE 88 ON INQUIRY CARD

MICROCOMPUTER PROGRAM DEVELOPMENT TOOLS

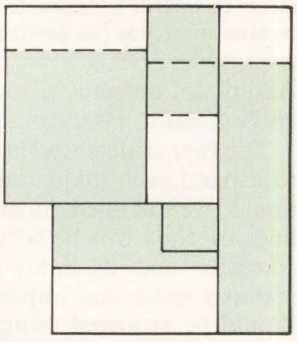
Using an integrated system concept, program development can be carried out on target systems that respond in real time with existing system characteristics

by Robert Harp

Trends toward developing microcomputer software by emulation on large program driven host computers or on multitarget systems lead to hardware that is more complex and costly than the target system hardware. Emulation can also mask the more subtle characteristics of the target system, especially those in real time. An integrated approach to program development replaces emulation on an alien host machine with a set of software tools that creates a host system environment on the target system. Since the hardware and operating systems are the same for host and target, actual correspondence between the two is accomplished. A powerful memory mapped program editor and a real-time debugger complete this set of tools.

When program development is carried out on a host system, all host system characteristics, notably for real time, exist and will respond to the programs as if they were the final product contained within the host machine. A prerequisite of such an integrated development system is to have the single-board computer be the same as in the target system. The target system is then a subset of the host—the development system. If additional functions are needed, they can be plugged into the host (target) system bus.

Robert S. Harp is co-founder, chairman of the board and vice president, engineering, of Vector Graphic, Inc, 500 North Ventu Park Rd, Thousand Oaks, CA 91320. A graduate of the Massachusetts Institute of Technology, he also holds a PhD degree in electrical engineering from Stanford University. Mr Harp holds several electronics patents and received the L. A. Hyland patent award in 1977. He is the author of over 30 papers on subjects that include plasmas, microwave circuits and theory, diagnostics, and millimeter waves.



A program developed and debugged on an integrated system will have virtually eliminated faults and control problems when it is transferred to the target machine. Since actual target hardware is used in program development, including peripherals and input/output (I/O) devices, most problems surface during development rather than in the field. Support features resident in an integrated system, such as the editor and debugger, can be used to simplify problem identification, analysis, and correction. Fig 1 illustrates a typical hardware configuration for an integrated software development system.

Development cycle

The first step in a program development cycle is to define the flow and operation of a desired program on the target machine. Using an inverted pyramid approach, several iterations of program development are flowcharted, each in successively greater detail. (See Fig 2.) Notes relating to special conditions, possible breakpoints for status monitoring, and potential trouble areas should be placed near the flowchart blocks. Flowcharts are then derived that allow the programmer to identify tasks that can be defined by a manageable group of instructions, including subroutines.

Following task definition, the program designer should know the scope of the target system and be able to set forth in block diagram required elements that show signal flows, peripherals, and lists of major software subroutines to be called. A rough cut at memory size is now possible. It is important to track product cost through the development cycle to ensure that cost objectives will be met for the final product.

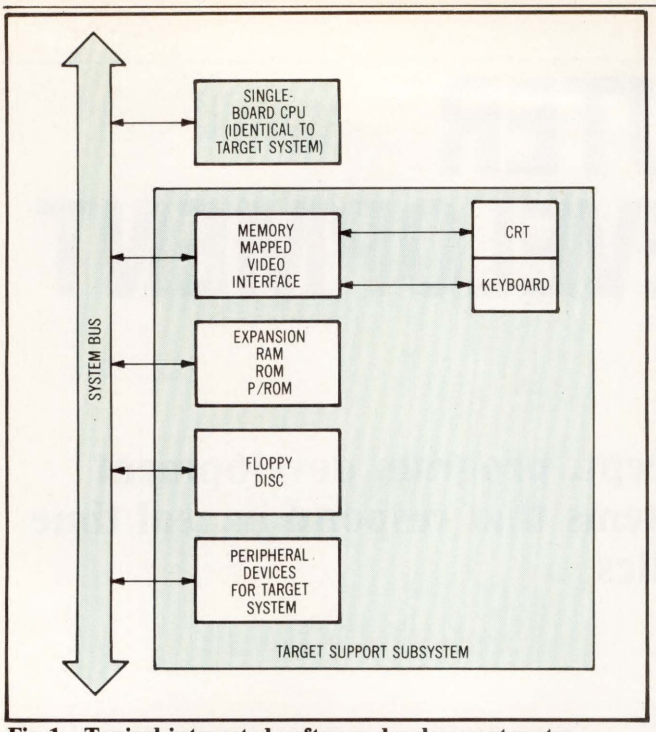


Fig 1 Typical integrated software development system. Components are usually housed in desktop computer. Easy access to boards is desirable especially if target system will involve numerous I/O devices

Additional objectives, such as package size and power and execution rate, can also be tested at this point.

The first critical step in the detailed program design is to expand each major task definition block into additional, well-defined function blocks for which specific lines of code can be written. Often a combination of compiler and assembly language is useful to save memory space and improve execution speed. Subtasks should be arranged using actual modules of the target system (both hardware and software) in every element of the host system. This will ensure that the host system is really the target system, maximizing payoff for the integrated approach.

Combining high level languages that have common relocatable formats, such as FORTRAN, BASIC, or Pascal, creates segments in different languages that can be linked to form an efficient program. Segments involving arithmetic (particularly floating point), scientific functions, or parsing of input strings are most efficiently written in FORTRAN or BASIC. Segments that deal with special peripherals, such as analog to digital converters, or video displays, are most efficiently handled in assembly language for speed of execution. A linking loader used to tie all elements together is now necessary.

Coding is a basic level of program development. It is essential to include comments within the code that will save retrieval time later in the process, especially if the program is maintained by persons other than the designer. A text editor, as part of the integrated approach, allows the designer to write and verify subtasks independently—to search and replace, globally modify statements, and perform tasks analogous to word processing. Coding is an iterative task within an integrated system, but the ability of the editor to handle "cut and paste" mechanics can help to eliminate the potential for errors. The advantage of the editor in the integrated approach is its ability to run on the host (target) system. This provides rapid turnaround between editing and testing of program parts under development, since it is unnecessary to continuously switch between host and target systems.

Assemblers and compilers

After the program is written, it will be assembled or compiled, depending on whether software was developed in an assembly or a high level language. An assembler operates on the text created by the editor and generates an object code file, usually in either absolute machine language form or hexadecimal format, which contains additional information allowing each small block of data to be loaded at a specific address. It creates a listing file that can be output either to a printer or directly to the screen.

The assembler also can generate output in a relocatable format. In addition to interpreting program mnemonics and labels in accordance with the microprocessor instruction set, an assembler responds to directives that give it additional information. For example, the source file can be set to generate a form feed in the listing file; or certain parameters can be set to given values, either locally or globally.

More advanced assemblers accept macro commands, which are defined in a flexible manner, so that a particular name appearing in the program source code and accompanied with optional parameters will be encoded in a specific manner when the assembler generates its output. This feature allows the programmer to incorporate in object code program segments referred to in a shorthand manner. Macro commands also allow an assembler to run on one machine and

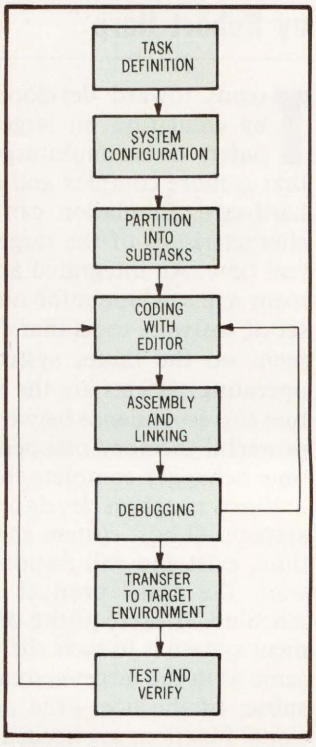


Fig 2 Software development cycle. Coding portion of cycle is usually most time consuming and could be further subdivided into several distinct tasks such as design, use of library routines, library maintenance, etc. Most coding for small applications is in assembly language; however, high level languages such as C, PL/1, or BASIC may be preferrable for some applications

generate code for a different type of microprocessor.

Compilers operate on source code written in a high level language, generating assembly language source to produce actual machine code. After the program is compiled, modules are generally required to link the program together, forming a runtime package. This runtime package often contains floating point arithmetic routines, string handling routines, and disc I/O routines to be accessed by the compiled linker program. The linker accepts program modules in a relocatable format, combining them in a file and adjusting the address references within each segment to correspond to their relative position within the entire program. Address bytes must be adjusted both for local references and references to external modules. The resulting compiled program is then written on the disc and executed by returning to the operating system.

Assemblers and compilers are important software development tools, although actual operational interaction with either is considerably less than with an editor or a debugger.

Debugging. In theory, when coding is complete, the program should work; but debugging is usually an ongoing part of the process. An integrated system gives availability of a full software tool set, including editor, assembler, compilers, and debugger, all running on the host (target) system to eliminate continual downloading of host to target for testing and debugging, thereby greatly aiding work flow. The ideal debugger simulates the target system, and can be made to single step through the sequence of instructions and show on the terminal screen the system state, register contents, flag status, and the like. Using the debugger, the system designer can analyze the program, find and correct problems with the editor, then assemble, compile, or link, and repeat the sequence with the debugger.

Since the peripheral and I/O devices intended for the target system respond during the debugging phase, the designer can quickly modify an integrated system, eliminating the need to read a memory dump for construction. Once the program is debugged and run on the host (target), it can be transferred to the target machine. This is done by burning a programmable read only memory (P/ROM), writing an erasable programmable read only memory (EPROM), or loading a floppy disc. To guarantee similar hardware environments, the verification process must be repeated for the prototype target equipment.

Memory mapped program editors

Editors were originally developed to work on slow speed, line-at-a-time devices. The physical constraints of such devices resulted in single-line editor designs. The slow rate of data assembly and limited display scope can make it difficult for the programmer to visualize the text that is being manipulated. However, program editors designed for self-contained development systems can rapidly manipulate text on screen by using a memory mapped video display, thus allowing the programmer to immediately see the effect of any changes. While not required for an integrated software development approach, the memory mapped editor further enhances the integrated approach.

A memory mapped editor, such as SCOPE™ by Vector Graphic, utilizes text manipulation techniques developed for word processing systems along with conventional program editor features. A principal difference between a program editor and a word processor is character orientation. Most programs are written so that a single line of text stands alone, while correspondence text has freer form, with sentences or phrases of arbitrary and widely varying length.

Formatting. A memory mapped editor loads a disc file segment into a buffer memory and displays a portion of this on the terminal screen. In memory and on disc, text is maintained in compacted form with multiple spaces replaced by a tab character. The beginning of one line immediately follows the end of a previous line. When text is displayed on screen, tab characters are expanded into a preset number of spaces, and individual lines of code occupy individual lines on the display. Text is viewed by scrolling the image on screen through the memory text buffer on a line-by-line or page by page basis; thus the entire text can be viewed rapidly to find the portion that needs modification.

A highlighted cursor moved on screen with arrow keys changes, inserts, or deletes text; changes appear instantly on screen and are reflected in the memory buffer. With instant display modifications, the programmer need not wait for slow, sequential, character-by-character construction of the display. Techniques for working with a memory mapped editor can be learned easily and make editing a program less cumbersome.

Memory mapped editors automatically provide line numbers that can be toggled on or off with a simple keystroke. These line numbers are totally separate from program line numbers and do not affect each other. Line numbers are also useful for moving portions of text from one position to another with a single command.

Global search and replace editing permits replacement of any character string with another arbitrary string. However, this replacement can be limited by either line number range and/or column range within the editor to prevent inadvertent replacement of mnemonic string sequences in a comment statement. The programmer can also control whether this replacement is done at each occurrence or not, skipping over a particular occurrence, if desired. Lowercase characters can be folded into uppercase, and wildcard characters can be included in the search string.

File manipulation. Another feature of the memory mapped editor is its flexibility to build a program from disc resident library files. Program developers tend to utilize familiar routines, and it is advantageous to be

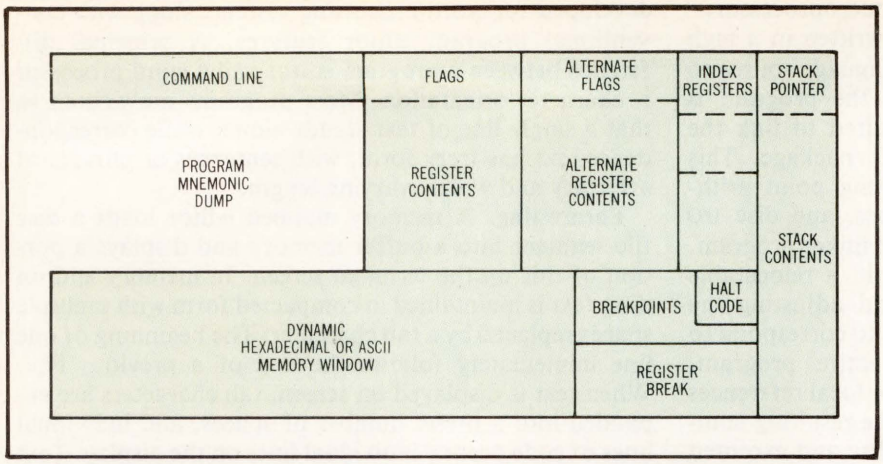


Fig 3 Debugger video display. Various areas of screen change dynamically with execution (simulation) of every machine instruction. Without complete refresh of screen, simulation speed is about 8 times slower than normal

able to weave such routines into the fabric of a new program by calling portions of library files for insertion in the program text being created.

Interlocks are editor commands organized to make it difficult for the programmer to accidentally lose the file. In addition, command organization preserves the original file as a backup, so that the original file can be deleted only by deliberate effort on the part of the operator.

Source files are often too large to be stored entirely in memory. The editor treats the source file on disc as a virtual memory, editing a portion of the file to fit in the system memory. For larger sources, the program pages through the text on disc, treating the disc as virtual memory.

When the editor is exited, the original file is preserved on disc and renamed as a backup file. Temporary files that were automatically created to store portions of text removed from the memory text buffer are modified, and then linked with present contents of the memory text buffer, along with any portions of the original file that were not modified. A new file is created on disc and given the name of the original file. Upon exiting the system, there are two files on disc—a newly edited file, given the name of the old file, and the original text, which is now a backup file.

Some print files generated by assemblers tend to have lines longer than the normal 80-column screen, but they can also be handled by the editor. By displaying the first 80 columns on screen and allowing the entire text to scroll sideways instead of up and down, the programmer can view portions of text that extend off screen. Memory mapped editors can handle line lengths of up to 250 characters.

Simulators

A debugging program that operates as a true simulator, and which can also operate in real time, is a key element of an integrated system. In this simulator, the instructions to be executed are fetched from host (target) memory and placed in a random access memory (RAM) location. The central processing unit (CPU) registers are then loaded from temporary storage locations and the instruction is executed. Modified contents of registers are then updated on screen and saved in temporary registers, and the program counter is then used to fetch the next instruction (see Fig 3). This type of program debugger allows program execution through system memory. Keyboard and video display can be utilized by the program in a normal fashion with displays either single-stepped or executed in several different speeds and refresh modes.

There are two operational modes of the simulator—execution and command. Execution is the actual running of object code, while commands tell the simulator what to do. Both aid the debugging process. To interrupt execution mode, a symbol is typed on the keyboard, causing the simulator to halt and enter command mode. Twenty independent commands can be typed onto the command line, and the program can then proceed in execution mode. An immediate execution command caused by any hexadecimal code entered from the keyboard and executed as instructions, permits some internal states of the CPU to be set, such as flags and interrupt status. A direct execution command is also provided for program execution without any simulation. All control over the program normally used for program segments that must operate in real time is lost in this mode.

With screen update activity, the simulator runs at a lower speed than normal program execution. Speed decrease varies from approximately 100 to 1 for full-screen refresh, to about 8 to 1 for minimum refresh. In many cases, slow execution speed is an advantage while observing program operation, particularly text editing programs that manipulate characters on screen rapidly. In a slower mode, a program designer can see exact manipulation and can often track bugs immediately. The use of a keyboard to halt program execution, without altering its use by the program being simulated, is a challenging aspect of the debugger program.

Summary

With an integrated system approach to microcomputer development, it is possible to offload many mechanical aspects of a task. The key to an integrated approach is the availability of an editor and realtime debugger that run on a host machine, and operate in such a mode that the machine, and programmer, actually think they are the target system.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 707 *Average 708* *Low 709*

Meet the SLC-II. It's the perfect fit for any computer that yearns to be more intelligent. SLC-II is the **robotic communicator** you've been dreaming about for years. It's actually a microcomputer, with synthesized voice, and an autodial/auto-answer 300 bps modem. Its vocabulary is well over 300 words. And what it can't say, it'll spell out in English.

Our clever little SLC-II can easily be tailored to give your computer extra productivity and efficiency—without disrupting existing hardware or software. This intelligent communications controller can intercept messages from your computer, and then take specific, independent action—from giving a wakeup call to hollering for the fire department.

SLC-II isn't just another "voice box" or a monitor that merely records events. It's a robotronic marvel capable of acting on commands. And the exciting possibilities of how it's used are limited only by your imagination.

Think about giving your computer creation a voice in its future. The SLC-II. For more information, simply contact us today at: Digital Pathways, 1060 East Meadow Circle, Palo Alto, CA 94303, Telephone: (415) 493-5544. TWX: 910-379-5034.

DIGITAL PATHWAYS

SLC-II. TAILOR IT TO MAKE YOUR COMPUTER A LOT SMARTER.

THE SLC-II. IT TALKS TO SIMPLY EVERYBODY.

United States: (415) 493-5544 • Canada: (403) 286-2744 • England: 403 813 813
Germany: (089) 60 60 71-72 Telex: 5216290 isio d • Switzerland: 022/310587 Telex: 289191

Synertek's 2K x 8 Static RAM... Not Just Another Jelly Bean.

For today's demanding microprocessor-based systems, you don't need another jelly bean. You need the most advanced 16K static RAM available anywhere.

Introducing Synertek's family of 2Kx8 static RAMs. With important system design features. The SY2128 offers Automatic Power Down for significant system level power savings. And for systems where speed is critical, the SY2129 offers a fast Chip Select Access of 50nsec (max.).

Mix and Match. With JEDEC approved 24-pin pinouts, both allow you to make the switch between RAMs, ROMs, EPROMs, and E^2PROMs as your needs dictate. With minimal board changes.

Process Plus. You also get the cost benefit of our advanced process technology. We manufacture the SY2128/SY2129 family with our state-of-the-art double-poly process – where we add a second layer of polysilicon to our advanced HMOS process – so that densities are increased dramatically.

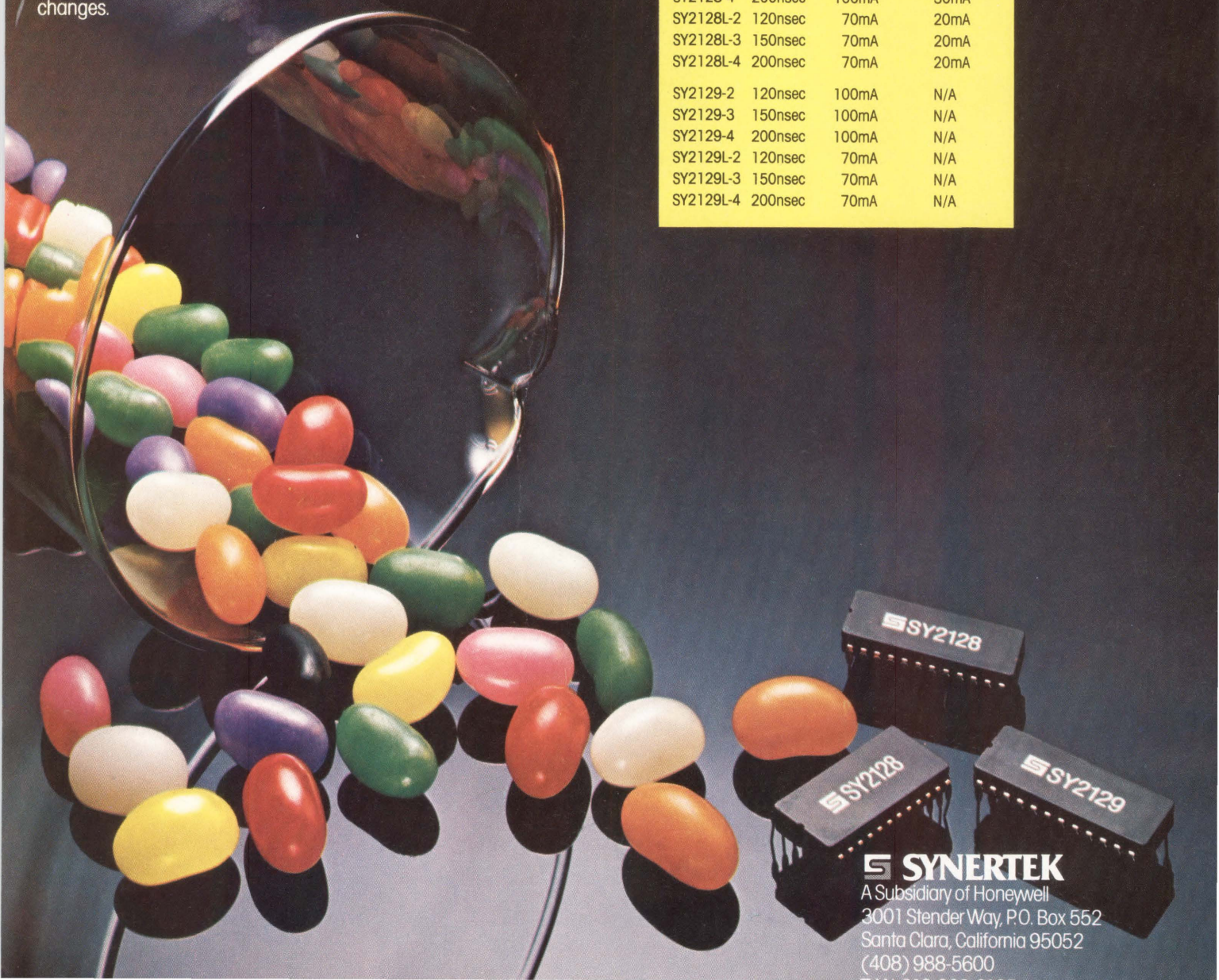
Together, and individually, our 16K static RAMs offer you choice and flexibility to make the perfect match with your micro-based system design needs.

Call on the company that makes it in MOS technology. Call Memory Product Marketing direct at (408) 988-5611. Or contact your nearest Synertek sales representative or distributor.

Synertek is a major MOS supplier of high volume products with advanced technologies and techniques behind everything we make. Static RAMs. ROMs. Custom circuits. Single-chip microcomputers. 6500 microprocessors and peripherals. Systems.

SY2128/SY2129

Part Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)
SY2128-2	120nsec	100mA	30mA
SY2128-3	150nsec	100mA	30mA
SY2128-4	200nsec	100mA	30mA
SY2128L-2	120nsec	70mA	20mA
SY2128L-3	150nsec	70mA	20mA
SY2128L-4	200nsec	70mA	20mA
SY2129-2	120nsec	100mA	N/A
SY2129-3	150nsec	100mA	N/A
SY2129-4	200nsec	100mA	N/A
SY2129L-2	120nsec	70mA	N/A
SY2129L-3	150nsec	70mA	N/A
SY2129L-4	200nsec	70mA	N/A



SYNERTEK
A Subsidiary of Honeywell
3001 Stender Way, P.O. Box 552
Santa Clara, California 95052
(408) 988-5600

APPROACHES TO COMPUTERIZED VISION

Large expenditures of both time and money have failed to produce one all-encompassing technique to perform pattern identification. However, existing techniques offer capabilities that can be applied to today's requirements.

by William Holderby

How to imbue the computer with a rudimentary form of intelligent sight is the fundamental problem facing designers of pattern or object recognition systems. Human vision is an analog function that reacts to colors, light intensity, and motion with a high degree of accuracy. The eyes send the brain a constant stream of data that describe visual scenes in great detail. Information is continuously updated, and constitutes a quantity of data far in excess of the information necessary merely to understand or identify the perceived images.

Digital pattern recognition is the technique of digitizing images and identifying the resulting binary pattern as it would be perceived in analog form. Such procedures require that objects or patterns, once identified, be stored as standards and compared with new images. However, digitized patterns lose some of the information that would be perceivable in analog form. Hence, digitization methods must be able to discriminate the pivotal qualities that distinguish one image from another. For example, the ability to distinguish between two flowers depends on the distinct physical structure of the flowers. One procedure could distinguish between a daisy and a rose; but if color were the only distinguishing visual characteristic, an entirely different technique would be necessary to distinguish between two roses.

Certain industrial applications require only a limited form of sight, and can be implemented by computers that perform pattern recognition. Computer applications for pattern recognition do not require the quantity or the quality of imagery that the human eye provides. In fact, for many industrial applications such detail and quantity prohibit the storage, identification, and functional retention of images.

The results that any optical recognition technique can achieve depend strictly upon the questions the procedure must answer. The type of pattern recognition employed must correspond to the pattern's physical peculiarities and emphasize the necessary areas of distinction. Requirements other than physical pattern differences can dictate method. Physical parameters, such as movement, ambient lighting, and orientation, affect the type of recognition system that would be most effective and reliable for a particular application.

There probably will never be only one technique, but available methods can meet many of today's requirements. Brief descriptions of several microprocessor based systems now used in industry will be followed by a detailed description of one approach to pattern recognition. Each technique discussed is ideally suited to a specific set of applications.

Attribute measurement

An attribute measurement system calculates specific qualities associated with known object images. Attributes can be geometric patterns, area, length of perimeter, or length of straight lines. Such systems analyze a given scene for known images with predefined attributes. Attributes are constructed from previously scanned objects and can be rotated to match an object at any given orientation. This technique can be applied with minimal preparation. However, orienting and matching consume significant processing time, and are used more efficiently in applications permitting standardized orientations. Attribute measurement is effective in parts segregating or sorting; parts counting; flaw detection; and recognition decisions 7, 8, 9, and 10. (For this and subsequent such references, refer to the Panel, "Typical recognition decisions.")

William S. Holderby is vice president of engineering at Autech Data Systems, 1301 W Copans Rd, Pompano Beach, FL 35064. Before that, he was president of Distributed Intelligence, Inc, and senior design leader at Modular Computer Systems. He has also worked as a senior engineer at Planning Research Corp and Harris Corp. Mr Holderby earned a BS in engineering at Florida Technological University, Orlando, Fla.

Color filtering

A color filtering system identifies patterns with a series of colored filters. Objects are scanned for symbols or colors, then identified by the system. Applying multicolored illumination to objects being scanned adds another dimension to the identification. Colored filters make it possible to recognize specially treated decals and allow the system to add or subtract color information for flaw identification. Certain flaw configurations can be discriminated because they respond differently to various wavelengths of light. This system has minimal hardware costs. Applications suit specially prepared objects, and include parts sorting; flaw detection; parts counting; and recognition decisions 1, 2, 3, 4, and 9.

Thickness or diameter identification

The thickness or diameter identification technique discriminates an object by its physical dimensions. Measurements of thickness or diameter, either combined or separate, are compared to profile templates. Comparison images are matched or rejected based on how well a given profile fits. This system can be used when physical tolerances are readily identifiable and in applications involving quality control. Actual dimensions can be obtained from noncontact systems, such as the Autech 2000 laser thickness or diameter system. In many applications, image identification is not required, but verification of proper construction is important. Applications include physical product specifications for quality control; process control based on product toleranicing; parts counting; flaw detection; material waste control; and recognition decisions 1, 5, 8, 9, and 10.

Grid counting

The grid counting system performs a single function: to count the number of discrete parts that pass over a calibrated, backlit grid. The system identifies and counts an object by sensing when light completely surrounds the object's profile as it passes through the system. Calibrated grids provide a frame of reference for determining the relative size of an object. Grids also enable the system to maintain a frame of reference for determining when more than one object is present in the scene. Grid counting systems also answer recognition decision 9.

Typical recognition decisions

1. Does an image match a single standard?
2. Does an image not match a single standard?
3. Does an image match one of a matrix of standards?
4. Does an image not match one of a matrix of standards?
5. What is the quantity of difference existing between an image and a particular standard?
6. What is the profile of differences/comparisons between an image and a set of standard images?
7. Does an image exhibit a specific attribute or set of attributes: ie, straight lines, areas, or shapes?
8. Does an image display certain features: ie, holes, dimensions, or thicknesses?
9. Does a particular image match the preceding scanned image?
10. Is an image similar to or different from a set of profile standard images based on length, width, height, color, or distinct reflective pattern?

Basic terms

Image or pattern—a scanned binary data set in some N x M array dimension of an object or scene.

Object—a physical entity, such as a resistor, screw, or complex assembly, that has length, height, width, and area dimensions. Objects can be backlit to produce a profile pattern, as in Fig A. Another approach, shown in Fig B, generates a reflected pattern by casting light onto the surface.

Scene—an image that contains more than one object. A scene may be a cluster of objects, even if only one object within the scene is to be examined.

Recognition—the identification of an object to a desired degree, based on the image it produces.

Edge detection—has two meanings that depend on the context in which the term is used. Operational edge detection tells the system hardware where to start creating an image or scan. In pattern identification, edge detection determines the physical edges of an object in a scene.

Template match—a direct object pattern match to a standard pattern on a point-by-point basis. Template technique results in a sum of differences, and normally does not provide for rotation or skewed orientation. The name derives from a manual recognition technique in which a perforated template is used to analyze photographic scenes.

Spatial regions

The spatial regions technique statistically assigns regions in a decision space that correspond to the image of a particular pattern or object. Each region is defined by the results of a specific set of tests performed on the image, which are summed and oriented. The resulting magnitude and angle become vector quantities for the image's position in the decision space. Image position must relate to the magnitude and angle of similar, previously quantified, objects grouped in space. Vector matching results in image recognition. The spatial regions technique uses and assigns values to object attributes in a manner similar to that of the attribute method. Orientation of sample images and image rotation are compensated for in the magnitude calculations. Applications for the spatial regions method include parts sorting; recognition of writing symbols; extension of recognition from object evaluation to document sorting; and recognition decisions 1, 2, 3, 4, 7, 9, and 10.

Bit-for-bit match

The bit-for-bit match is a digital template-matching technique that compares a scanned image with a single, previously stored, master image. Number of matches is compared to an operator defined deviation threshold, and a reject or accept light illuminates to indicate

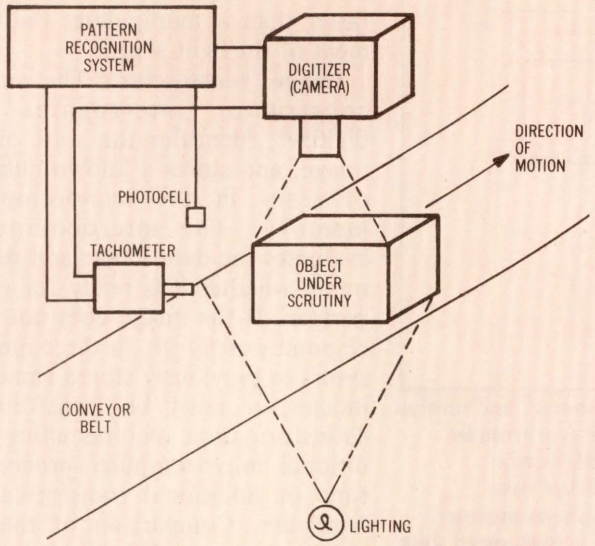


Fig A Profile analysis system. Pattern recognition system scans conveyor driven object. Object is illuminated from below to provide the system with backlit profile. Profile is scanned synchronously with movement of conveyor belt; tachometer provides synchronizing pulses. Photocell determines level of illumination and camera threshold is varied to maintain parameter consistency

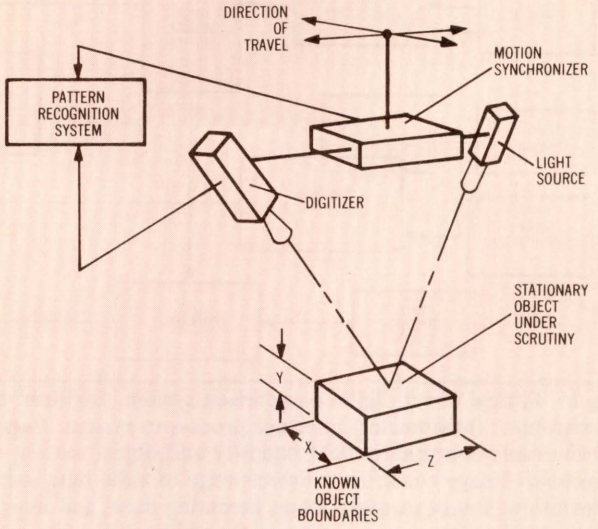


Fig B Reflective image analysis system. Object is arranged within known boundaries and image analysis system established in known position above object. Reflected light from object onto digitizer creates pattern. Digitizer can create image from single snapshot or scan entire object by movable support, coordinated by motion synchronizer

whether the matches are less or greater than this threshold. The bit-for-bit match presents a one-dimensional comparison that meets application requirements for testing repetitious images. However, the system cannot average or weight various portions of an image. By necessity, these systems are simple, expedient tools designed for pass/fail applications, and do not offer complex adaptations. Bit-for-bit matching can be applied to parts sorting; tolerance testing for quality control; parts counting; flaw detection; and recognition decisions 1, 2, 5, and 9.

Direct digital comparison

Direct digital comparison tests an image or scene against a standard set of images or scenes. Decisions made from a set of digital comparisons have to meet many industrial applications. This technique reduces images or scenes to the binary, or 2-dimensional, level: black and white. Thus, any set of pattern recognition requirements applying direct digital comparison must be based on information in a pattern, object, profile, or scene that can be discerned in 2 binary dimensions, as opposed to 64 gray levels or 16 colors.

For direct digital comparison, speed is defined as repetition in periods of less than one second. Granularity of an image determines how well the recognition system can identify patterns. Size of the incoming data matrix comprising a single image is directly proportional to the time it requires to process the image data. Decision complexity also affects system speed. If a system must evaluate an image against 10 standard images, it will function much faster than it will if it must evaluate the image against 100 standard images. Such time differentials constitute the "decision cost."

Image gathering. Digitizer, light source, and motion synchronizer (ie, tachometer) are the image gathering components of the direct digital comparison system shown in Fig 1, and form the interface to the physical process. Since the system must maintain a functional consistency of repeatability, data collected from the physical interface must be toleranced tightly. The digitizer portion can take several forms. A vidicon camera can be used, but vidicons require additional circuitry and periodic adjustment. Vidicons also provide more information than most applications need. Extraneous data must then be sorted out as the data are input, or stored for a reference sort. Either approach incurs additional expense and complications. When great detail is required, however, the vidicon provides the most data at the least expense.

The solid state digitizing camera converts video input into binary output. The charge-coupled device (CCD) array of the camera charges in proportion to the intensity of the incoming light striking the array, and is a function of both the light source and the scanning speed required for a given frame of data. Therefore, if either the light intensity or the linear speed changes, the data vary accordingly and affect system reliability. Variations are stored as analog voltages. Solid state digitizing cameras are available in different configurations, as a matrix array up to 1024 x 1024 pixels per camera, or in linear arrays from 64 x 1 pixels per camera.

Internal circuitry scans CCD matrices and converts individual pixel charges to binary data. The resulting image data are interfaced to the system as a stream of serial or parallel binary data bits. The limited scan speed of CCDs restricts the range of applications for various camera arrays. Because of its finite scan requirement,

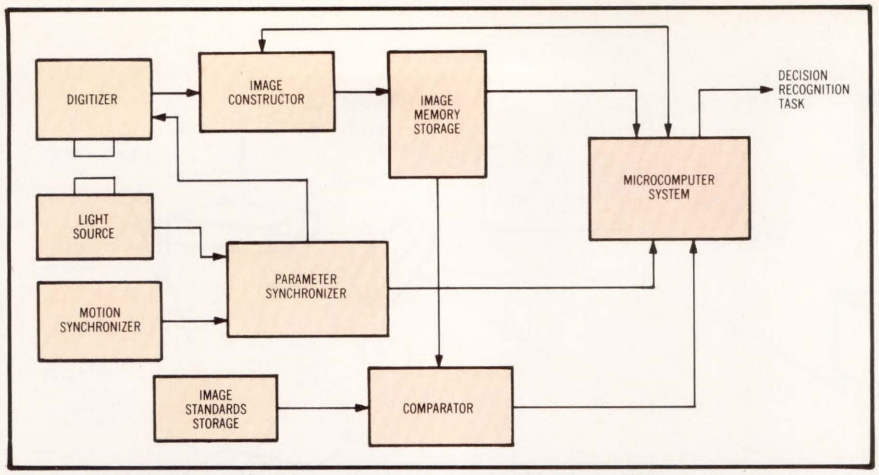


Fig 1 Typical direct digital comparison system. Digitizer, light source, and motion synchronizer (tachometer) interface process to system. Parameter synchronizer continuously coordinates light intensity and object motion with digitizer's threshold. Image constructor detects edge of valid data and identifies data orientation. Image memory stores incoming data, and image standards memory stores previously-constructed bases for comparison. Comparator is high speed data base that quantifies similarity between incoming data and standard bases. Microcomputer system directs operation of peripherals and judges comparison results

CCD matrix speed is inversely proportional to its array size. As a result, the CCD matrix response time under changing conditions, such as motion, ambient lighting, or reflective lighting variations, is finite. Although manipulation of binary thresholds or camera f-stops can provide some enhancements, these are only fine adjustments to specific requirements. The CCD array configuration must be selected carefully for a particular application. Four key questions determine the selection of the CCD array: Is the object to be scanned moving or stationary? If moving, what is the object's linear velocity? Can a tachometer synchronize the motion to the camera? How much pattern detail does the application require—ie, how much area does each pixel of the array cover?

Determining matrix size is fundamental, since the faster an object moves while being scanned by an array, the more smear or image degradation results from matrix scan time requirements. The N x M array is useful for stationary or very slowly moving applications, because it freezes the associated images. For rapidly moving objects, the 1 x N linear array, coupled with a motion synchronizer, can freeze a series of line images. When combined, the series constitutes a frame whose size is commensurate with the application requirements. Exact definition of movement in the array depends upon the scanning frequency of the camera chosen for a particular application; the associated device specifications also influence movement definition.

Parameter synchronizer. The basic relationship between light and speed requires that light intensity increase or decrease in proportion to speed. However, this is not achievable consistently with most light sources, such as incoherent filament generated light, which takes a finite time to heat or cool the filament to provide a respective increase or decrease in illumination. Any delay results in a lagging intensity level. One way to compensate for this lag is to vary the point at which the digitizing camera sets the threshold level of the analog CCD charge, at one or zero. The function of the parameter synchronizer is to manipulate the camera threshold, which is a direct current level, at a rate much faster than it manipulates the filament of the light source.

Image constructor. The image constructor interrogates the digitizer, identifies the start of an image, and stores a known number of scans in the microcomputer memory. The microcomputer evaluates the data image and determines whether it is ready for comparison. If the image does not correspond exactly (ie, in three dimensions) to previously stored standard images, it must be transformed. Transformation requires either additional microcomputer processing time or additional transformation hardware. Comparison of the incoming image and standard images forms the criteria for the system's "goodness of fit" decision.

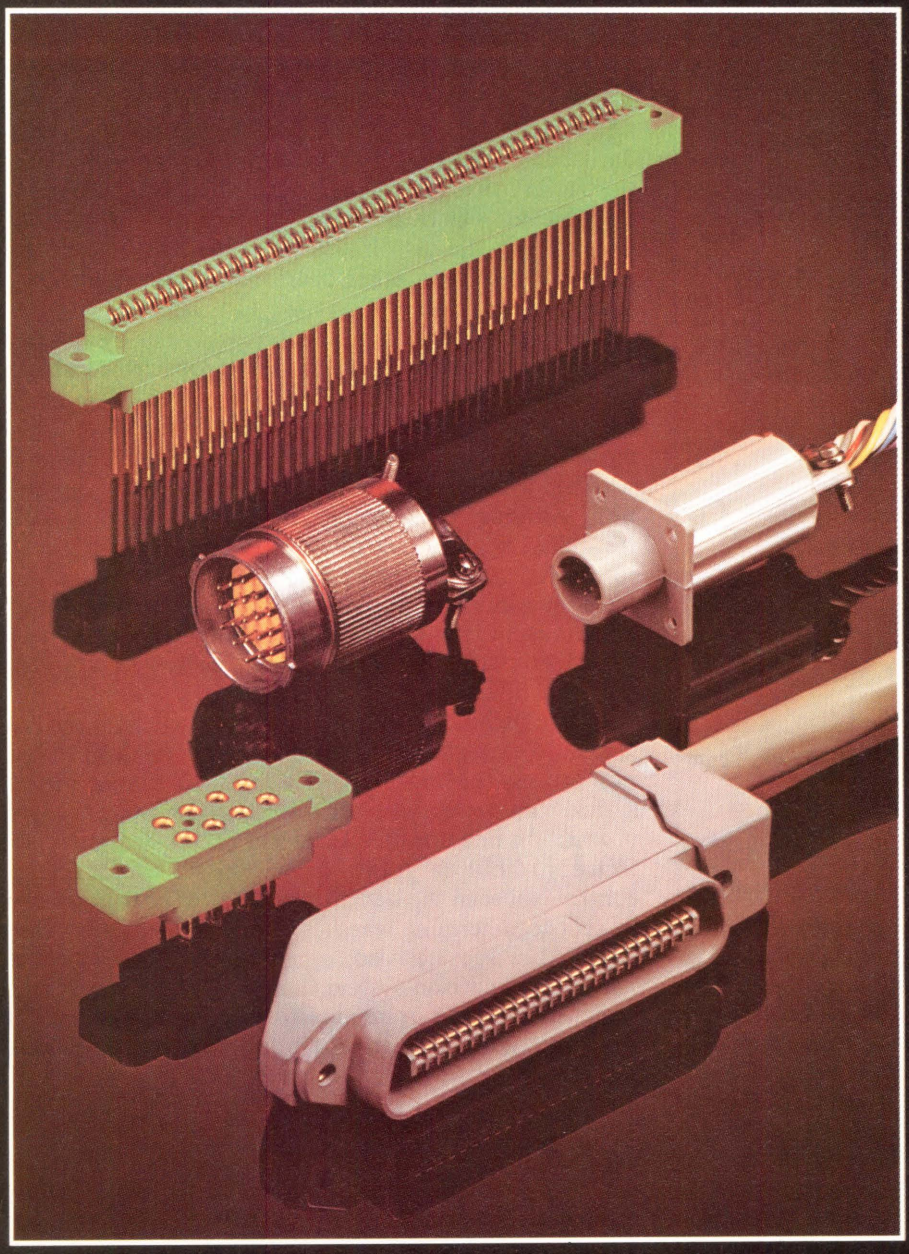
Image standards storage. Standards storage contains statistically averaged profiles for each image; profiles are constructed from a number of similar image frames previously scanned by the system. Two separate sections, the *average standard* and the *mask standard*, constitute image standards storage.

Scanning multiple images is an averaging process, which tests each bit to determine its repeatability over the image frames the system samples. Each data bit in average standards must occur in more than 50% of the scanned images of the same object. To be in mask standard, the bits must be found in 80% to 100% of these images. Bits that exhibit a high frequency of repetition constitute a weighted mask of required bits, with which a sample image must comply in order to be identified. Orientation masks can be designed into the mask standard to determine whether an image is skewed and by what angle.

Bit orientation in various mask standards corresponds to bit orientation in companion average standards. Therefore, if an image corresponds most to a mask standard and exhibits a 10° skew, then the comparison for final identification will be with an image in average standards that is also skewed at 10°. Another way to correct for skewed orientation is to determine a gradient vector that transforms the image through either transformation hardware or microcomputer software. The identification process incorporates both the mask standard image and the average standard image in a 2-dimensional approach. Goodness of fit is determined by a summed exclusive NOR comparison of the sample image with the standard bases. (See the Panel, "Recognition equations.")

Microcomputer system. The microcomputer is controlled by an 8-bit microprocessor that performs direct memory access data transfers to and from memory and the various peripheral facilities. In this system, the microprocessor directs the various steps of the recognition process and evaluates the resulting comparisons. The microprocessor must also be programmed to create

Our secret? Do a few things very, very well.



We've grown to where we are by making our connectors just a little bit better than the next guy. Price is important, but when it comes to a little-cheaper vs. a little-better, you know which wins. That's been our growth plan. And it has proved to be as totally dependable as our connectors.

VIKING
CONNECTORS

21001 Nordhoff Street | Chatsworth, CA 91311, U.S.A.
(213) 341-4330 | TWX 910-494-2094

CIRCLE 91 ON INQUIRY CARD

the standard data bases for a particular application. Programmed adaptability, the "learning mode," permits the system to operate in a wide range of applications and to respond to variations within the context of a specific application. Used to scan multiple images, the microprocessor creates a mask standard image and an average standard image from the profile of the bit array that each standard image comprises. This profile is determined by the number of times each bit repeats during the run of several similar images. This number must exceed 50% for a particular bit to be included in the average standard base and must exceed 80% to be included in the mask standard base. Including a bit in both bases doubles its relative weight when individual base versus image comparisons are summed. Weighting individual bits can be extended to three and four times by factoring additional standard bases into the goodness of fit equations. This allows an additional dimension for specifying special and required features in a given image. Base comparison summaries of the individual standards can be separated to permit a multilayered decision process that can reject an incoming image before it is compared to all standards. This saves time and reduces the decision cost.

Image sampling. Including a particular bit in any base depends on how many times it is found in similar patterns. The number of samples that provides these patterns is a major factor in the generation of a particular base or set of bases. A set of sample images evaluated must represent the entire population of possible images. To meet this requirement, two separate properties of a given image type, image pattern complexity and interpattern separation, must be evaluated.

Image pattern complexity is the minimum matrix size required to uniquely depict a given pattern for purposes of consistent recognition. In practice, the "recognizable pattern" of an object may only be a portion of that object. *Interpattern separation* measures the uniqueness of a given image pattern against similar images. Interpattern separation is basic to the goodness of fit decision. In "Recognition equations," Eq (3) shows that acceptance is based on whether an image's goodness of fit is greater than a statistically defined threshold; this threshold is inversely proportional to the interpattern separation. The greater the separation, the lower the threshold, and vice versa. The lower the interpattern separation, the more time and effort must be expended to solve pattern complexity.

In a given set of similar, but not equal, patterns, the distribution of each pattern will exhibit a specific mean and variation derived from comparisons against a standard base. The greater this variation, the greater the probability that inter-image separation will diminish to a point at which it cannot be recognized reliably. Overlapping the distribution of some images over images that belong in other distributions can result in incorrect recognition.

The goal of direct digital comparison, or of any pattern recognition system, is to identify processed images consistently. Percent of reliability required by an application, weighed against the reliability that a certain pattern recognition system can provide, will determine whether a process is feasible for a particular application. Although certain applications require over 90% reliability, pattern distributions often vary sufficiently to preclude that level of reliability. Pattern recognition techniques must be chosen carefully, since in many applications an image rejected as unknown because of insufficient data is as difficult to resolve as a wrong identification.

Direct digital comparison can be used as a sorting system to segregate selected components from a production process for rerouting. (See Fig 2.) A similar sorting system can verify whether all components on a given production line are the same, and detect dissimilar objects for rerouting. A profile analysis system for quality control can scan the backlit profile of a particular component to determine whether it is within specific tolerances. (See Fig 3.) Also, a self-learning, or adaptive, pattern comparison system that identifies changes in a monitored scene can be applied to security systems for detecting intrusion. In addition, direct digital comparison performs recognition decisions 1, 2, 3, 4, 5, 6, and 8.

Recognition equations

$$T_x = \sum_{i=o}^{N}\sum_{j=o}^{M} \left[(S_{Mij} \oplus I_{ij}) + (S_{Aij} \oplus I_{ij})\right] \quad (1)$$

where

T_x = total agreements between standard x and test image I
S_{Mij} = mask standard image (N x M matrix)
S_{Aij} = average standard image (N x M matrix)
I_{ij} = test image (N x M matrix)

$$G_F = \text{maximum } \{t_0, t_1 \ldots t_n\} \quad (2)$$

where

G_F = goodness of fit, maximum of set T_x

$$R = G_F - E \quad (3)$$

$$\begin{cases}\text{Accept} & R \geq 0\\ \text{Reject} & R < 0\end{cases}$$

where

R = acceptance (test condition of image as recognized)
G_F = goodness of fit [Eq (2)]
E = statistically defined reliability threshold

Conclusion

Advances in computerized pattern recognition directly influence the technology behind robotics, mechanized quality control, parts sorting, and document sorting. Designing computers that can identify, categorize, and make decisions based on visual entry to automated equipment will significantly improve automation in factories. Computerized pattern recognition technology can lead to closer quality control of manufactured parts and increased facilities productivity.

Advances in charge-coupled device cameras and microprocessors are making the systems described here economically feasible. Decreased memory cost per bit and increased density allow memory intensive pattern manipulation techniques. These trends are continuing

Panasonic CRT's— not just another pretty face.

When you can pack information on your screen to the furthest edge, and see it clearly under most lighting conditions, that's not just another CRT in your display terminal. It's probably a Panasonic. And it spells up-front advantages from any point of view.

Good looking for viewers.

In color and monochrome tubes alike, get sharp, clear focusing corner-to-corner and center-to-edge, thanks to a precision beam spot size and the Panasonic electron gun.

Panasonic high resolution color display tubes provide color photograph-quality pictures with twice the resolution of our conventional tubes.

You get the world's highest dot density (5x as many dots per unit area as conventional color CRT's), so you can use smaller characters and fit more data on the same size screen. You also get the high brightness and contrast of the Panasonic black matrix background.

An OEM competitive edge.

Whether you build monitors, terminals or entire computer systems, a Panasonic CRT can be a key factor in your competitive strategy. Choose from five color tube screen sizes, from 5″ to 25″, and eight monochrome sizes from 1½″ to 15″, plus special phosphors in both monochrome and color. Our wide selection is your design advantage. Our Direct Etch screen, an option available on most models, ensures non-glare viewing and contrast enhancement while saving you the cost of a separate faceplate. Our consistent quality and features are your selling points. And our reliable delivery and stock of the most popular sizes, models and options are all the back-up you need.

So whether you're buying or building a CRT display, look for something more than just another pretty face. Look for the best in CRT's: Panasonic. Panasonic Company, Electronics Components Division/Electron Tube Marketing, One Panasonic Way, Secaucus, NJ 07094; (201) 348-5275.

Direct Etch

Polished

Panasonic®
just slightly ahead of our time

CIRCLE 92 ON INQUIRY CARD

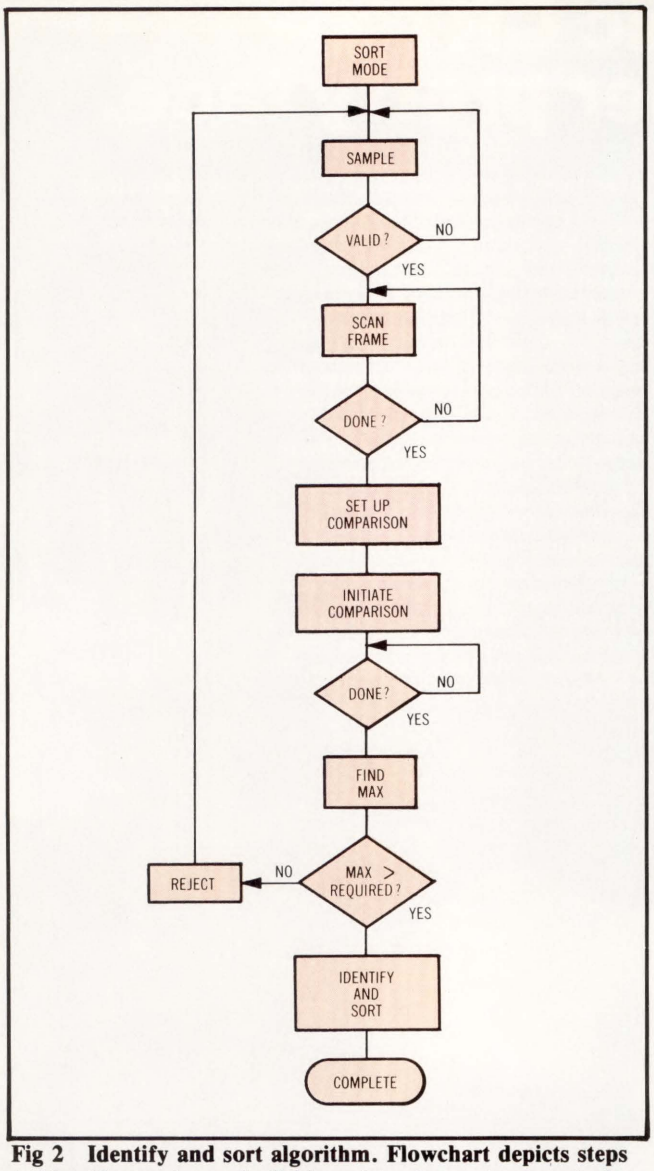


Fig 2 Identify and sort algorithm. Flowchart depicts steps to identify one image in field, and to change transport of object based on this decision. Comparison results are tested against predetermined threshold that determines reliability of decision

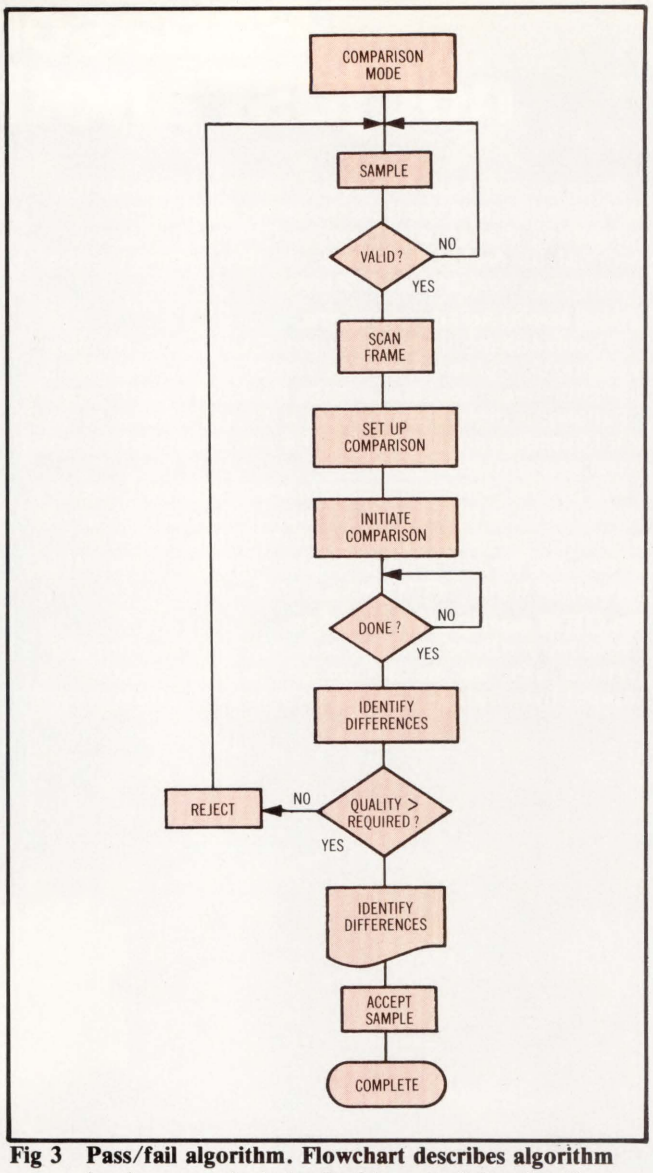


Fig 3 Pass/fail algorithm. Flowchart describes algorithm comparing image against standard base to determine if image matches standard. If number of matches exceeds threshold, image and associated objects are accepted. If image is less than threshold, object is rejected

and it is conceivable that techniques too costly today will one day be feasible. This is especially true for pattern identification involving gray levels or various color hues. The major problem with gray level technique, as opposed to digital matching, is that each operation requires numeric computation. Application times for gray level computation are in minutes, as opposed to fractions of a second for digital approaches. Holography and ultrasonic generated imagery have also advanced, but these approaches to pattern recognition may require years of research before they become useful for a wide range of applications.

Bibliography

G. J. Agin, "Computer Vision Systems for Industrial Inspection and Assembly," *Computer*, May 1980, pp 11-20

M. L. Baird, "Future Directions of Industrial Applications of Pattern Recognition," *Proceedings of Fourth International Joint Conference of Pattern Recognition*, Kyoto, Japan, 1978

D. Casasent, "Optical Pattern Recognition," *Electro-Optical System Design*, March 1981, pp 39-47

D. Casasent, "Pattern Recognition: A Review," *Spectrum*, March 1981, pp 28-33

D. H. Huhel and T. N. Wiesel, "Brain Mechanisms of Vision," *Scientific American*, vol 241, Sept 1979, pp 150-162

J. G. Jarvis, "Visual Inspection Automation," *Computer*, May 1980, pp 32-38

Y. Masahiko and S. Tsuji, "Industrial Computer Vision in Japan," *Computer*, May 1980, pp 50-63

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 710 *Average 711* *Low 712*

CSPI Array Processors bring speed to scientific and engineering computation

CSPI's MAP™ FAMILY IS DESIGNED FOR SPEED. Our 32- and 64-bit floating point array processors enhance the computational speed of 16- and 32-bit minicomputers by 10 to 200 times. MAP gives FAST results through parallel processing which permits arithmetic operations to proceed at peak speed while I/O data is rushing through. MAP maintains 12 MFLOPS of arithmetic with up to 18 megabytes per second of concurrent I/O. Arithmetic and I/O proceed at peak rates while the host minicomputer stays free for other activity. MAP's unique multiprocessor architecture supports up to 8 of our standard analog and digital peripheral device interfaces. The results — real time processing for your most demanding requirements.

MAP SPEEDS YOUR RESULTS BY SIMPLIFYING YOUR JOB. An easy to use FORTRAN library of more than 200 signal processing, math, I/O, and support functions is available. A cross-assembler and simulator support the development of special functions you may wish to add.

IN OVER 500 INSTALLATIONS WORLDWIDE, MAP's ARE DELIVERING FAST RESULTS — Find out how you can benefit from the MAP alternative — send for your free Array Processor guidebooks for details on applications, architectural considerations, specifications, and software support.

CSPI
THE ARRAY PROCESSORS

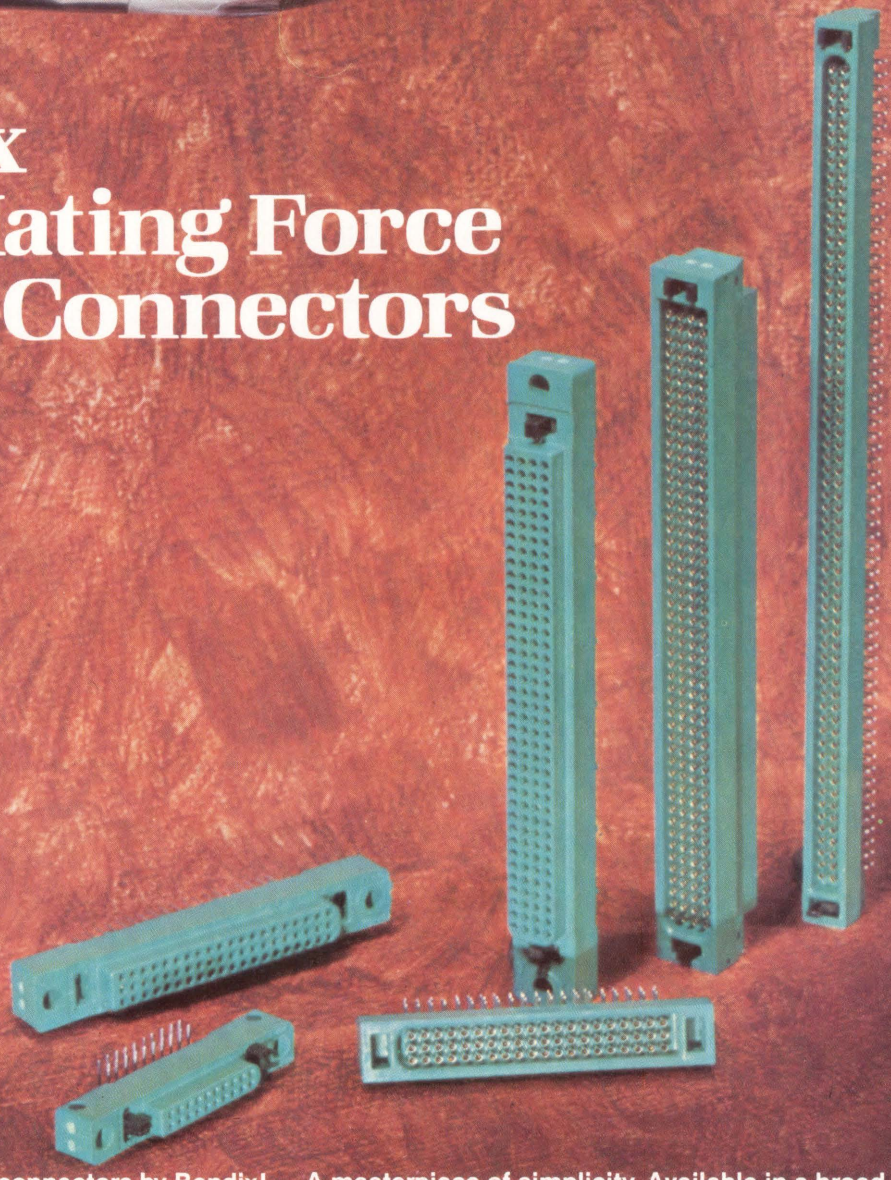
40 Linnell Circle, Billerica, Massachusetts 01821 • 617/272-6020 • TWX: 710-347-0176

WORLDWIDE SALES OFFICES: Cedar Rapids, Chicago, Cleveland, Dallas, Dayton, Denver, Detroit, Ft. Pierce, Houston, Indianapolis, Kansas City, Milwaukee, Minneapolis, New York City, Philadelphia, Pittsburgh, Redondo Beach, Rochester, Scottsdale, St. Louis, Downsview, Montreal, Ottawa, Vancouver, Amsterdam, Frankfurt, Geneva, London, Madras, Milan, Paris, Stockholm, Sydney, Tel Aviv, Tokyo, Wellington.

CIRCLE 93 ON INQUIRY CARD

The state-of-the-art in PC design...

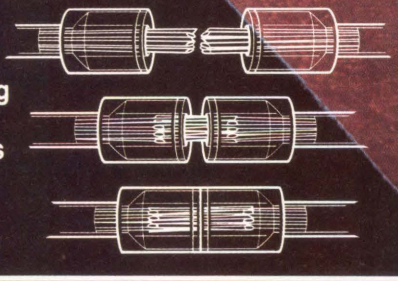
Bendix Low Mating Force Brush Connectors



Low mating force, bristle brush connectors by Bendix! They've advanced PC design to a new state-of-the-art!

A connector that's *dependable* (stable contact resistance), *durable* (up to 20,000 mates/unmates), *flexible* (20 - 400 contacts per connector), and *smooth* (mating force reduced by 70 - 90%)!

The brush "wiping" action of gold-plated wire bristles, meshing at highly redundant contact sites, creates multiple electrical paths, and intimate, gas-tight connection.



A masterpiece of simplicity. Available in a broad variety of connector/termination formats.

- compatible with High Speed Digital Switching
- greater board effectiveness by allowing more circuits per board
- stable electrical performance
- less need for exterior board supports
- no need for secondary activation procedures, typically required for zero-insertion force connection

That's the "broad brush" picture on our brush connectors. Get all the fine details in our new brochure, *LOW MATING FORCE*. Call 607 563-5302, or write The Bendix Corporation, Electrical Components Division, Sidney, New York 13838.

We speak connectors.

Bendix

CIRCLE 94 ON INQUIRY CARD

ARRAY PROCESSOR DESIGN CONCEPTS

Modularized array processor approach requires reexamination of system level design requirements: architecture, programmability, and interfacing

by Peter Alexander

Array processors are becoming popular arithmetic peripherals, as high speed computational tools for minicomputers in both realtime and scientific applications. The recent proliferation of these devices and trends leading to more complex, modularized, systems make timely a discussion of system level design issues.

Although array processors are programmable, they are not general purpose in the same way that minicomputers and mainframes are. The principal distinction is one of serial versus parallel operational modes. Most minicomputers work in a step-by-step, serial fashion, fetching data from memory, operating on the data, and sending results to memory after the manipulations have been completed. Array processors, on the other hand, rely heavily on parallelism to enhance throughput and computations. Assuming that data to be processed are organized in memory in a block or array of known size, fetching and storing operations can be set up to overlap the actual arithmetic or logic operations. With this hardware structure, many elementary data routing and processing functions can be implemented concurrently, improving speed by 10 to 100 times over typical minicomputers.

The drawback is that the data must conform to a preferred vector or array structure for optimum performance. When array processors are used indiscriminately, particularly with scalar (nonarray) data, mediocre performance often results. Thus, the array processor is best suited for applications characterized by highly repetitive arithmetic functions performed on large blocks of data.

Powerful, large-word size mainframe computers and supercomputers have made high data rate processing feasible, but these systems are not economical for laboratory environments or data acquisition and reduction applications. Similarly, although minicomputers are economical, they are technically unsatisfactory because of their limited computing speed and smaller fixed-point formats. An appealing compromise is a minicomputer for general purpose computation that is attached to a peripheral array processor for repetitive, computationally-intensive tasks.

Functional characteristics of array processors

The array processor is usually subservient to a host computer. (See Fig 1.) Since the array processor is a programmable unit, it needs program development tools of its own, and these are normally integrated with the host software utilities to ensure easy use and maintenance. For example, array processor manufacturers invariably supply cross assemblers written in FORTRAN to allow execution on the host processor.

Host data transfers. With very few exceptions, data flow to the array processor is through a direct memory access (DMA) port to the host data memory. Memory cycles are "stolen" from the host's central processing unit (CPU) when the host does not require access to the memory. Cycles are also taken by demand whenever conflicts occur, thereby forcing the CPU to wait. Once initiated, transactions take place between the host and array processor, or vice versa, without explicit reference to the current program being executed in the host. Host software overheads incurred in setting up the data transfer make a block transfer, rather than a single-word transfer, more efficient. Most array processor designs today provide cycle stealing "transparency" to the

Peter Alexander is vice president, Computer Products Div, CNR, Inc, 220 Reservoir St, Needham, MA 02194. A graduate of the Massachusetts Institute of Technology, Dr Alexander has been involved in the research and development of digital signal processing applications, realtime dynamic system simulation and implementation, and the analysis of communications systems. He is currently responsible for the development of new array processor products at CNR.

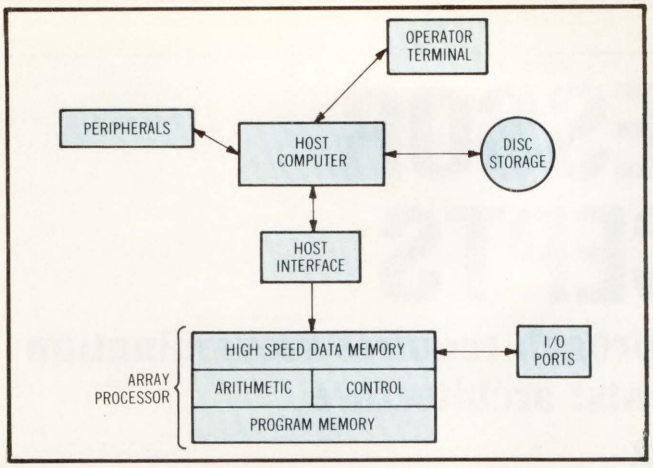


Fig 1 Functional characteristics of array processor. Host provides peripheral support, including standard I/O interfaces and utility software, as well as access to existing compilers, loaders, file managers, etc, in program development. For some applications, relatively low performance/low cost microcomputers can suffice as host

array processor as well. Array processor arithmetic and control operations can proceed in parallel with data movement into and out of the array processor data memory. This memory is addressable by two separate pieces of hardware, the host interface and the array processor's arithmetic unit.

Although a DMA interface is fairly easy to establish, in many instances transfer rates are limited to about 1M byte/s. If data must be supplied by the host and results returned to it, the array processor's arithmetic throughput capacity may outstrip transfer capacity and create an input/output (I/O) bottleneck. This is particularly true of machines that must receive command and control blocks through the same channel.

Other configurations are possible. The host can be as insignificant as a microcomputer with a pushbutton console panel in place of a terminal, and read only memory for storage of both the array processor and its own programs. Such dedicated processor configurations rely on direct data input through the array processor's I/O ports, and often lack program development support. A substantive development configuration, however, can adequately provide program development support. After debugging at such a facility, programs are burned into the host's or the array processor's read only memory.

Block processing. The objective is to enhance the system's arithmetic performance using the array processor peripheral. Samples are brought in from the host memory or from the array processor's peripherals and processed by the program loaded into the array processor. Although array processors are occasionally configured to input and process one sample at a time, most applications require that a complete block of data be input. This is partly to amortize I/O setup overheads, but also to accommodate block oriented algorithms such as the fast Fourier transform (FFT) and matrix operations. Furthermore, the number of basic arithmetic steps may differ from sample to sample, so that working on one block at a time allows loading fluctuations to be smoothed out.

Double-buffered I/O. If memory cost is not critical, some segments of the high speed data memory shown in Fig 1 can store incoming samples, while others hold data from an earlier block transfer. Such organization is characteristic of realtime signal processing applications when block-structured operations can usually be overlapped with input and output.

Data flow in an array processor is double buffered on both input and output sides of the arithmetic unit. (See Fig 2.) The input device first writes into array processor data memory via DMA transfers, using the space designated as input buffer 1 (IN1). These transfers are clocked at a rate determined by the external device rather than by the processor. Meanwhile, the arithmetic unit consumes previously input data stored in the second input buffer (IN2). Similarly, results produced for output to another device (eg, a display) are placed in output buffer 2 (OUT2), while a previously computed block is concurrently transferred from data memory under the control of the device itself.

Eventually, it becomes time to switch buffers so that input is to IN2 and output is from OUT2. The arithmetic unit then has autonomous use of the remaining two buffers, IN1 and OUT1. Timing for the buffer swap is controlled by the input process. A clock associated with the input device is counted down by the interface in the buffer-filling operation. When a block word count reaches zero, buffer base addresses are modified in the

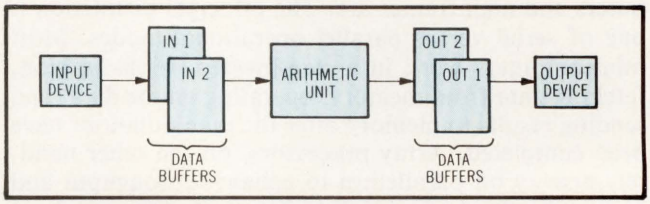


Fig 2 Double buffering of array processor's arithmetic unit. Buffers, defined as storage segments in array processor data memory, are switched logically between I/O devices and arithmetic unit. This isolation allows arithmetic unit to execute block arithmetic procedures

interface address generation mechanism and a flag set for the arithmetic unit.

Two design requirements ensure continuous processing without loss of samples: the interface address switch must occur within one sample time; and arithmetic processing carried out on a data block within the machine must be completed in less time than it takes to input a completely new block. When the second condition is met, the array processor waits a short time for the input device to complete its task.

Array processor DMA overhead. Typically, the I/O port gains access to the host system's memory on the array processor cycle that follows its request for access. (See Fig 3.) It has higher priority for memory reads and writes than the arithmetic unit. The array processor program may or may not require a transfer between the

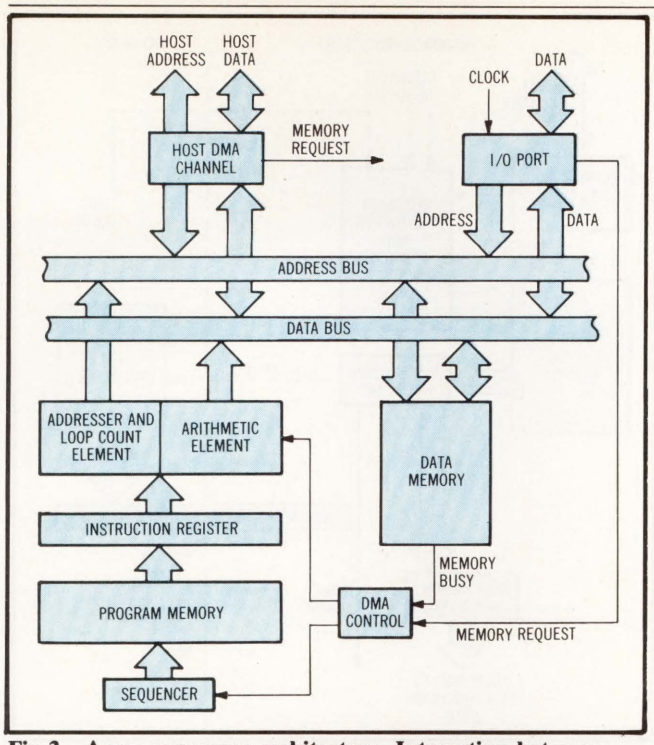


Fig 3 Array processor architecture. Interaction between array processor and I/O device illustrates DMA overhead for array processor. Timing of external device is almost always asynchronous with array processor clock, and special hardware provisions must accommodate timing differences. Memory is shared resource. Data are transferred via one or more I/O ports at rate determined by hardware (eg, host bus speed), software, or generation process itself

arithmetic unit and memory on this forthcoming cycle. If the DMA control circuit design allows, a word transfer from an external device into or out of memory can take place without affecting normal operation of the array processor, provided that there is no memory access conflict with the arithmetic unit. However, it is likely that granting a DMA request will force the array processor's clock to stop for at least one cycle, and possibly for two. In any case, array processor programs are generally memory intensive; most FFT and matrix routines need exclusive use of memory to run at full speed, and consume more memory cycles than arithmetic cycles during each processing step. Consequently, I/O devices conflict with arithmetic elements whenever a DMA request is made. In most cases, this problem is not severe; it simply extends the execution time of the algorithm.

Modular multiprocessing

For many computations, the number of operations per sample point or the data throughput rate is so high that multiple array processors become cost effective. Apart from the inevitable cost/speed tradeoffs, crucial architectural decisions in the design of an array processor are organization of the memory storage hierarchy, including register, data memory, bulk random access memory (RAM), host memory, and disc file access mechanisms; type and precision of arithmetic operations, such as fixed point, block floating point, or full floating point; software development, for example, arithmetic element instruction sets, pipelining within these elements, stack facilities for subroutine calls, and data paths interconnecting the basic elements; and system level concerns, including DMA and flag communication principles, as well as program loading, debugging, and processor control.

Careful data memory organization is important to array processor design. Arithmetic elements in an array processor can access data memory via the bus structure. Two sets of address lines must connect to the data memory to support this dual-port operation. Within the arithmetic section, a program memory usually contains several microcoded fields in each word, and a sequencer controls generation of the next program memory address. The sequencer handles address stack functions (eg, in subroutine calls) and conditional branching of the program sequence.

The array processor is best suited for applications characterized by highly repetitive arithmetic functions performed on large blocks of data.

Fields emanating from the program memory instruction register affect various processor elements individually, such as addressers for generation of data memory addresses, loading of operands into multipliers and adders, and incrementing loop counters. When the speed of the arithmetic section is insufficient for an application, little advantage is gained simply by adding arithmetic elements; access to data memory quickly becomes bottlenecked and limits the overall computational speed.

Architecture of the multiple array processing system described here can provide progressively increasing

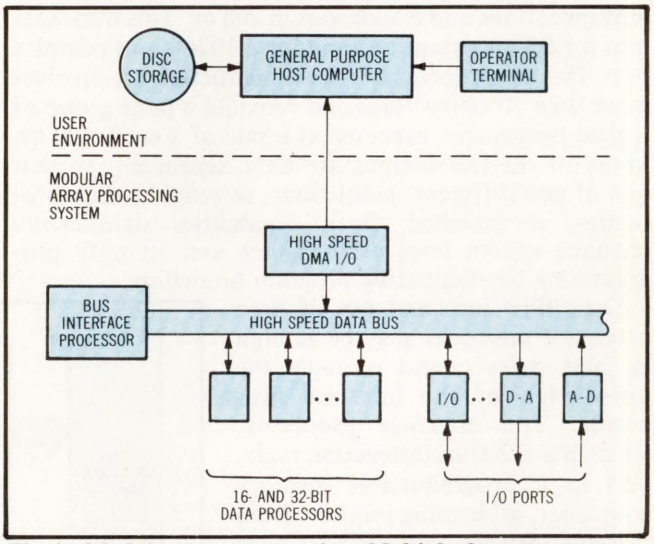


Fig 4 Modular array processing. Multiple data processors, connected by high speed bus, augment system's arithmetic power, while interface processor controls bus structures and I/O ports

arithmetic computational speeds while avoiding excessive I/O burdens. It is based on a modular processor concept that represents a viable hardware partition when ultrahigh processing speeds must be achieved. This scheme, called the modular array processing system (MARS), illustrates problems that can confront a set of cooperative processors in an array processing system—particularly with regard to I/O and interprocessor communication. Issues and conclusions presented here are universally applicable for configurations of this nature.

A programmable family of array processor modules, the MARS is intended for high speed realtime signal processing applications that require exceptional arithmetic throughput. The building blocks can be used in a variety of configurations tailored to a broad class of application types, involving either 32-bit or 16-bit arithmetic. Key aspects of this design are related to a fairly simple partitioning of the system hardware. Each modular arithmetic processor contains its own data memory and program memory. Also, modular, interrupt driven programmable bus controllers provide efficient arbitration of data transfer conflicts.

Component processors include data processors and interface processors, along with various interfaces to the outside world for interaction with a host minicomputer or additional digital and analog devices. Multiple data processors augment the arithmetic power of the system, while additional interface processors control bus structures and asynchronous I/O ports. Fig 4 shows a simple configuration consisting of one interface processor and several data processors.

The data processor is the arithmetic element in this family, and is available in a 32-bit version that carries out a single 32-bit multiplication and addition in 200 ns. An alternative choice performs 16-bit multiplications and additions on paired 16-bit data, and is capable of 4 multiplications and 6 additions in 200 ns. This translates into a 1.05-ms execution time for a 1024-point complex FFT. The data processor's total instruction set involves more than 50 instructions and provides a large group of logical operations, executed at a rate of 2 every 100 ns. Many of the instructions are data dependent, so that one of two different instructions, selected by data properties, is executed. Such capabilities significantly enhance system level performance and simplify programming by eliminating program branching.

Data flow into and out of data processor memories may be as high as 20M bytes/s, and is under the jurisdiction of the interface processor. The interface processor, which has a 200-ns instruction cycle, acts as a programmable memory controller, arbitrating requests from different devices on a cycle-by-cycle basis. Eight virtual channels can be set up for programmed or DMA transfer of data into and out of data processor memories, including, for example, transfers between two data processors. A set of read/write control lines in the interface processor handles device handshaking at the

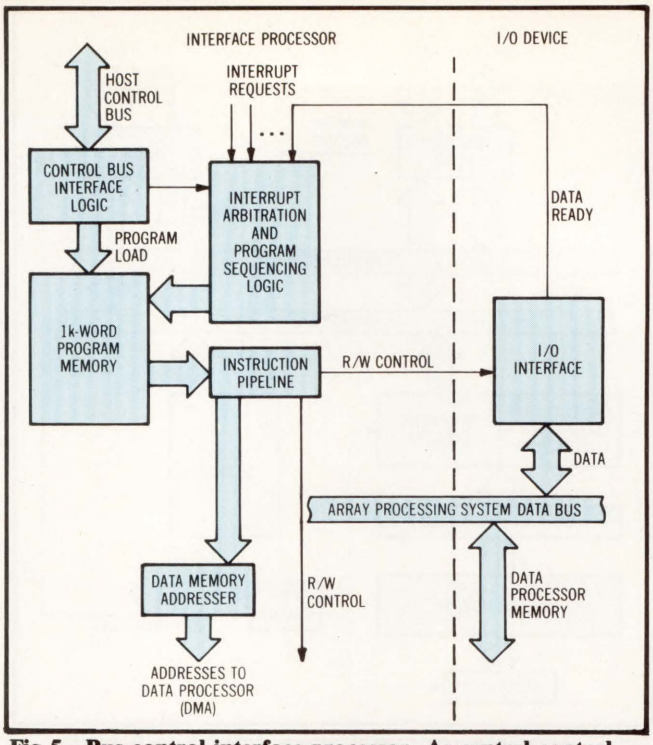


Fig 5 Bus control interface processor. As central control for system data flow, interface processor acts as memory controller that arbitrates requests from different devices on cycle-by-cycle basis. Read/write (R/W) control lines handle device handshaking at 200-ns cycle level

200-ns cycle level. (See Fig 5.) Using literal instruction fields under program control, the interface processor can select one of eight devices to be the data bus source. For write operations, an 8-bit instruction field can be programmed to give simultaneous transfers to eight different destinations.

In essence, the interface processor acts as the central control point for data flow in the system. For I/O processing of asynchronous devices, incoming blocks of data are passed to one or more data processors, if necessary in an interleaved fashion, according to the interrupts generated by requesting devices. Because only the data processors participating in a given word transfer are subjected to DMA cycle stealing, the I/O overhead is not as severe as it would be in a totally synchronized system.

Using data from the control bus, the interface processor supervises data processor program loading or loads

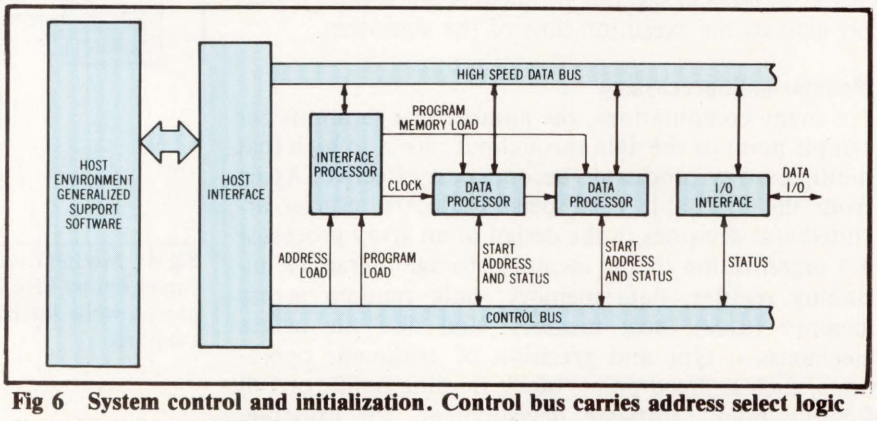


Fig 6 System control and initialization. Control bus carries address select logic (from host) for individual data processors, which extract parameters such as start address. Interface processor interprets host commands, loads its own service routine address file, or supervises data processor program loading

GET A CLEAR HONEST IMAGE THE HITACHI WAY!

Computer data and graphic displays never looked better, brighter, sharper.

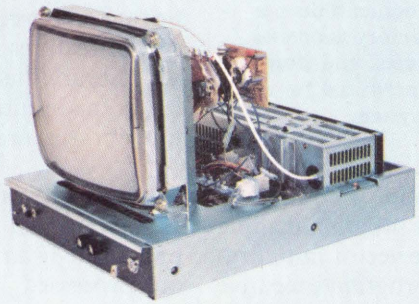
New Hitachi high resolution in-line RGB color monitors utilize wide video bandwidth and a 0.31 mm spacing between triad pairs. The result? A trio-dot density **twice that of conventional monitors!**

Look at these advanced features

Adjustment-free convergence, single PCB configuration, video amplifier bandwidth from 50 Hz to 25 MHz. Flexible frequencies range from 15 to 18 KHz horizontal and 50 to 60 Hz vertical. Monitors provide high contrast and brightness from black matrix and 85% light transmission tubes. Can any other maker match these advantages?

Variety of Screens

You can select from a wide choice of screens to meet your specific application needs: Normal phosphor; long persistence phosphor to virtually eliminate flickering, or medium resolution versions for most ambient light situations.



Unsurpassed performance

Long time convergence stability is assured due to self convergent in-line guns and **single PCB reliability.** Operator controls include power on/off, degauss, brightness, contrast.

Call or write for more information.

Hitachi America, Ltd.

100 California Street, San Francisco, Calif. 94111 Tel: (415) 981-7871
New Jersey Office: 6 Pearl Court, Allendale, N.J. 07401 Tel: (201) 825-8000

CIRCLE 95 ON INQUIRY CARD

its own service routine address file and interprets host commands. (See Fig 6.) Interface processor clock control commands can, for example, be employed to selectively clock the complete system.

Program loading and control

To specify I/O data transfer and control protocol with the host computer, the precise interaction between an applications program (user) and the array processor hardware must be considered in a realtime system environment. Array processors are inherently fast, and performance must not be compromised by excessive overhead at runtime. In essence, the burden must be placed on initialization preprocessing routines and, if necessary, on relatively inefficient use of program memory to minimize runtime linking and binding operations. For instance, some software systems load executable array processor code modules from a skeleton FORTRAN subroutine when that particular function is called. Others store a library of code modules in the array processor and dynamically link the code to the relevant data arrays during a task run. However, for each of these options the overhead burden that results for every function call is typically 1 to 5 ms. To reduce overhead, an array processor program can be built as an image file with the help of preprocessing utilities, in much the same way that object modules are linked together to create a load module for a minicomputer.

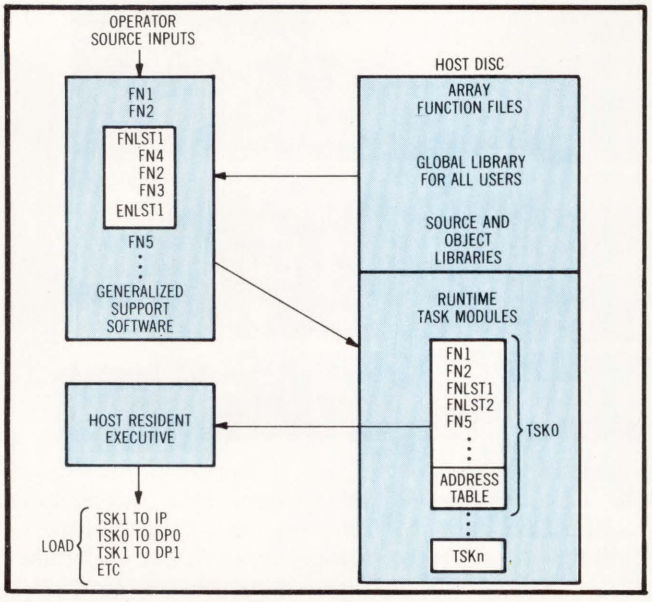


Fig 7 Preprocessor linking operations. Modular array processing system's preprocessor accepts specifications for lists of array functions to be executed (denoted FNLSTn) and individual array functions to be called. Program units are "linked" together in terms of program memory addresses, "bound" with tables of data buffer attributes, and stored permanently on disc. One load module is produced for each data processor and interface processor in system

System initialization, which includes program loading and interface processor service routine vector initialization, is handled by the host resident program executive support package. This program is written mostly in FORTRAN for portability between host computer systems. It maintains the integrity of a modular array processor configuration and acts as coordinator of user/processor system requests for processor driver services during this and runtime operations. After an offline program preparation stage, the user runs an application program in the host, and subsequent control and data transactions with the system are made via executive support. Typically, service requests will be for initialization, I/O, or array function execution calls.

Offline program development can be provided by generalized support software. A load module is generated for each data processor/interface processor, consisting of all runtime array function modules required, as well as any concatenated function list chains. Each entry in these runtime files may be accessed by a FORTRAN subroutine call in an arbitrary fashion. Since this normally takes several milliseconds from a host FORTRAN program, realtime applications are supported instead by user calls to modules consisting of linked function lists. (See Fig 7.)

For many computations, the number of operations per sample point or the data throughput rate is so high that multiple array processors become cost effective.

To clarify the reasons for the approach outlined, consider the two other popular approaches for program loading and access in array processing systems. In one, individual FORTRAN subroutines have the corresponding array processor code buried in an internal data statement. When called, the executive is consulted; if the code is not already in the array processor, it is extracted from the data statement and loaded into array processor program memory. Although slow, this is satisfactory for a single target processor. With the system described in this article, maximum program memory storage requirements can reach 128k bytes. In the worst case, this level of storage would be needed in the host data specifications for temporary storage of code. Discs supply the proper storage for modular array processor programs, so that one data processor can be loaded at a time.

The second scheme for array processor program organization and use requires initialization of array processor memory with a permanent, complete library that all users access. Unfortunately, this method consumes excessive amounts of memory. As the repertoire of standard routines grows, the fixed library approach becomes increasingly unsatisfactory. Middle ground can be found between these two strategies by recognizing the special features of a multiprocessor situation. A permanent library, held on disc, can be selectively accessed at load time in much the same way that scientific subroutine libraries are used in standard computer systems.

Realtime software design

In many signal processing situations, after data are input through an array processor's direct I/O port, they are processed by the array processor and eventually transferred to a host computer. In these instances, timing is determined in the array processor, rather than in the host program, so that provision must be made for synchronization of the user's host program with block transfers of data. This class of transfers will be referred

High-quality graphics. Built-in hard copy. Under $5000.

It's hard enough to imagine getting sophisticated graphics at such a low price—let alone getting an integrated printer to go with it. But then again, you've never seen anything like the HP 2623 graphics terminal.

The display's the thing.

The HP 2623 gives you more than just an extremely sharp screen image. With its advanced graphics features, you can shade different areas of a chart or graph with different patterns, or even draw entire pictures in a matter of seconds.

You can vary the size of the text, rotate it, or make it italic—in any of seven languages. And with a variety of software packages available (including PLOT 10 from Tektronix), you get a remarkable degree of flexibility in such a low-cost terminal.

The 2623 has two independent memories—for graphics and alphanumerics—so you can talk to your computer without disturbing your graphics display. And if you need hard copy, the thermal printer can dump it out in less than 40 seconds.*

Seeing is believing.

The HP 2623 works with computers from most major manufacturers. But no matter what system you use it with, HP's worldwide service organization can provide you with the advice, documentation and support you need.

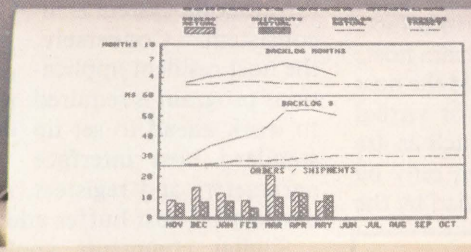
If you'd like to see an eye-opening demonstration, contact your local HP sales office listed in the White Pages. Or just return the coupon.

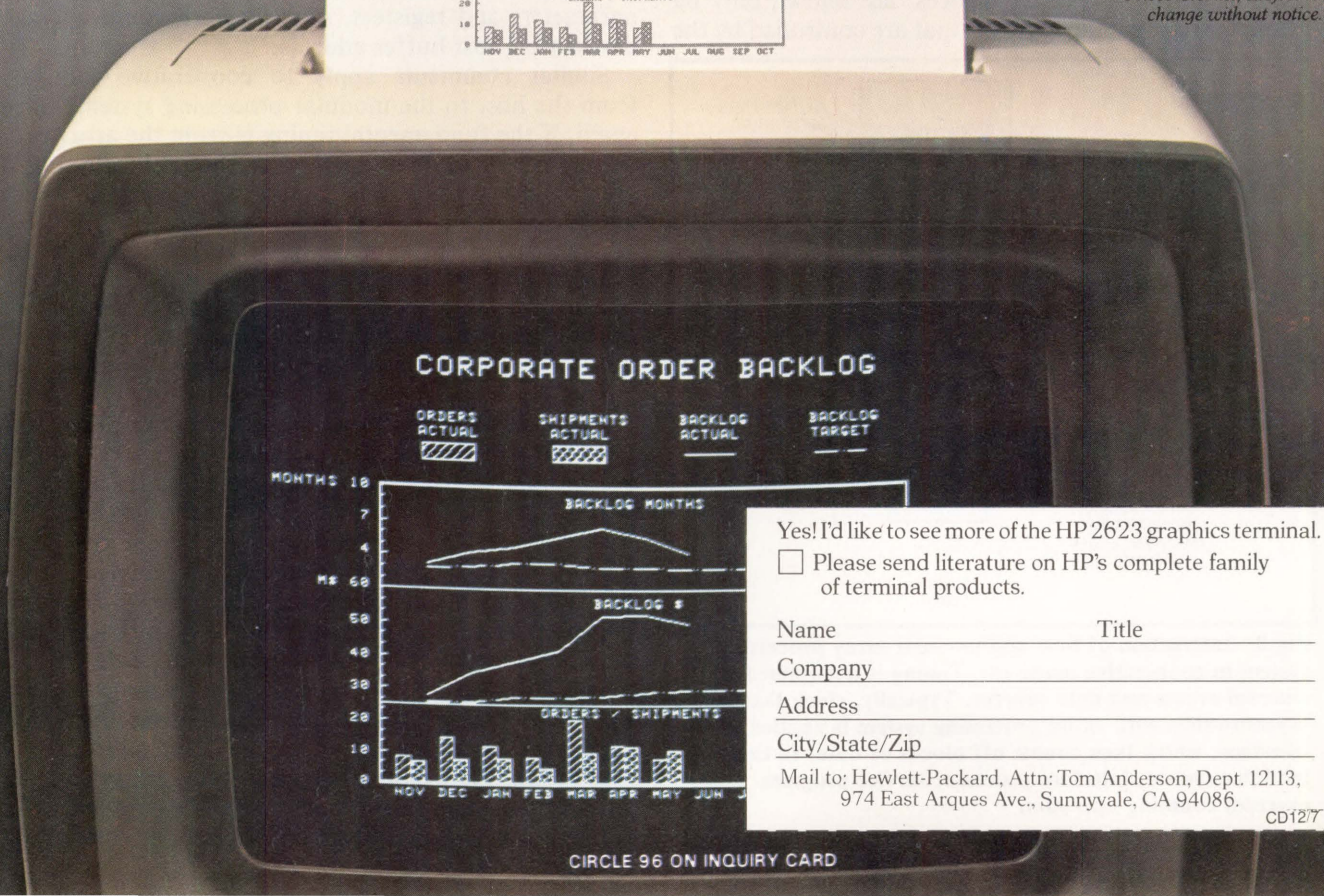
*The HP 2623 is available without hard copy for $3750.

When performance must be measured by results.

HEWLETT PACKARD

Prices U.S. list, subject to change without notice.





Yes! I'd like to see more of the HP 2623 graphics terminal.

☐ Please send literature on HP's complete family of terminal products.

Name Title

Company

Address

City/State/Zip

Mail to: Hewlett-Packard, Attn: Tom Anderson, Dept. 12113, 974 East Arques Ave., Sunnyvale, CA 94086.

CD12/7

CIRCLE 96 ON INQUIRY CARD

to as *cooperative mode I/O.* The second class of transfers comprises *host-initiated I/O.* Unilateral action by the host computer typically occurs during initialization phases of program execution or during debugging of applications programs, when the transfer request is initiated in the host computer. In both cases, the data transfer to a modular array processing system is accomplished by a cooperative effort between the host DMA interface and an interface processor program resident in the array processor. The DMA interface handles the storage of data within the host computer, while the interface processor program manages the data transfer from its side of the interface.

Cooperative data transfers. In broad terms, Fig 8 shows an external device transferring data to the modular array processing system. Following a series of data manipulation operations, the array processor is obliged, through the program structure, to make a block transfer to the host, perhaps for storage on disc or operator inspection at a display. Since internal programs will contain embedded directives to initiate I/O to the host, it is natural to think of the array processor peripheral as the synchronizing element in the I/O sub-

Array processors are inherently fast, and performance must not be compromised by excessive overhead at runtime.

system. For simplicity, however, the approach described here uses host control and setup of the host interface. There are several reasons for this decision. Certain hosts and host operating systems virtually dictate that the host control and prime the interface. In mapped or virtual memory systems, physical buffer addresses, such as are required by DMA transfer devices, are known only by reference to mapping registers that are controlled by the

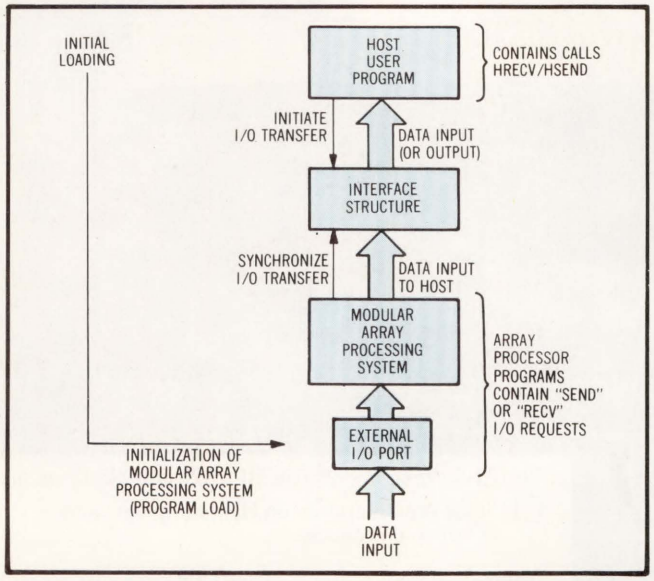


Fig 8 Interaction of host and modular array processing system in cooperative mode I/O. Timing is determined by external events and data sources. Typically, clock that is asynchronous with entire processing system is applied to interface, which then counts off blocks of data. In this modular system, interface processor service program executes counting operation

operating system. Overhead involved in accessing this information should be a burden placed on the host computer rather than on the array processor, where performance constraints are normally tighter. Potential host program relocation caused by swapping to peripheral storage or by shifting within main memory can be accommodated more easily. Simplified driver and interface protocols result, and these are desirable to avoid problems with new host operating system releases.

In terms of Fig 8, then, cooperative I/O, or synchronous I/O, requires that the host resident program and the programs for the modular array processing system be implicitly coordinated regarding the matching sequence of buffers for a given transfer. The interface processor, acting as the DMA device on the array processor side, does not explicitly communicate the identity of the next host buffer. It acts as a slave to the interface using program embedded address and block size information for buffers in the modular array processors. An error condition results if the transfer direction and/or block size between the host and the modular system is inconsistent. Conversely, the host resident applications program is required to work ahead to set up standard host interface parameters and registers, such as word count and the destination host buffer address.

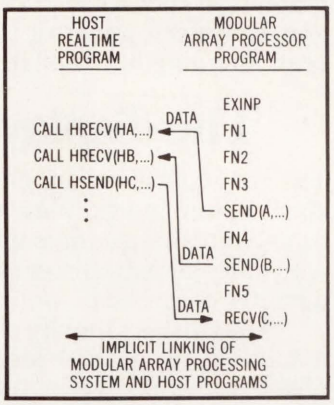


Fig 9 Implicit coordination of buffer transfers between host and modular array processing system. For event driven I/O, FORTRAN calls on host side and function statements on array processing program side link programs

Similar comments apply to cooperative transfers from the host to the modular processing system. Once again, if the fundamental timing is from the array processing system or its external ports, the applications programs resident there must contain I/O requests that are one-for-one with the host program requests. (See Fig 9.) A necessary restriction on program structure is the avoidance of runtime buffer selection based, for example, on data conditions (eg, data compression applications). Appending buffer identification information to the transmitted data block usually avoids this type of problem.

Host-initiated unilateral data transfers. The host program can initiate transfers without the cooperation or synchronization of a data processing program executing in the array processor. Even in this case, however, the cooperation of the interface processor is required, since it is the controlling element for any data movement inside the array processor over the high speed data bus. This class of data transfer is most likely to occur at the beginning or end of an application, when data parameters are loaded into data memory or final results read into the host computer. However, there may be situations when these transactions occur in the middle of an application. For example, the host may wish to monitor certain parameter values on an aperiodic schedule or in

Systems Houses can rely on NORTH STAR

We make your applications work like a dream.

Whatever you're dreaming up, we can help turn it into reality. To successfully bring your vertical market application system to market, you need cost effective, reliable hardware, and state-of-the-art software development tools. North Star offers our own proprietary development systems as well as CP/M. Our new "Application Development System" (ADS) lets you create your own software packages for a wide variety of applications. ADS provides you with a powerful set of programming tools for creating business applications and is based on the popular language "C." You can build from existing, proven software (word processing, data base management and accounting) by integrating your software with our standard business applications.

Systems Houses receive our full support including extensive documentation, programming seminars led by experienced business application programmers, a telephone hot-line for your programmers, software bulletins and development hardware discounts.

To make your dreams come true, and for more information, please write North Star Computers, Inc., ATTN: OEM Sales Dept., 14440 Catalina Street, San Leandro, CA 94577. Phone (415) 357-8500. TWX/Telex (910) 366-7001.

For more information on North Star's Application Development System, clip this coupon.

NAME

COMPANY

ADDRESS

CITY STATE

ZIP PHONE

CD 1281

FOLLOW THE STAR NorthStar™

CIRCLE 97 ON INQUIRY CARD

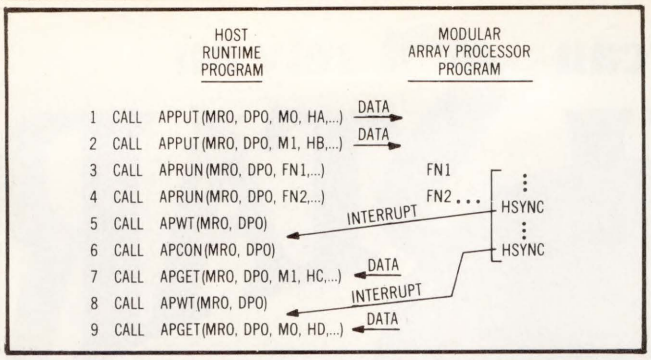


Fig 10 Explicit coordination of data transfers between host and modular array processing system. Possible sequence of program steps using host-initiated unilateral I/O is shown. Steps 1 and 2 transfer two buffers of data from host to modular array system. Then, in step 3, program segment FN1 is started in modular system 0 in data processor 0. When this segment completes, segment FN2 is begun. In step 4, FN2 contains host synchronization call that suspends data processor program and also generates interrupt to host computer. At step 5, host pauses until interrupt occurs. Then, step 6 causes FN2 to continue execution; while in parallel at step 7, data buffer is read back into host. At step 8, host waits for FN2 to complete, then final results at step 9 are read into host

response to an operator's directive. A second example is a control message transmission from the host to the modular system to cause a different computation to take place without losing processing synchronization with the data. A third example is the debugging of applications programs when it is desirable to examine data memory.

Since the time at which these transactions occur is not predictable, the interface processor service routines concerned with host I/O must check at the beginning of every transaction for the type of transfer about to be made. If a host-initiated unilateral transfer is indicated, a subroutine call is sent to a common service program located in a fixed area of interface processor program memory as part of the standard software package. This routine completes the I/O transaction and then returns to the calling procedure. The program must then loop back to the original test so that synchronization is maintained for cooperative data transfers. Such testing of I/O type is automatically generated when the standard modular array I/O service routines are used. Furthermore, the bootstrap dispatch program used to initialize all interface processor service routines contains the same test; thus, even if no host service requests are embedded in the user program, the capability to perform data transfers to and from the host computer exists.

For the interface processor program servicing these unilateral requests to direct the correct amount of data to or from the proper data processor memory cells, the host must transfer this information to the interface processor program before the transfer is initiated. Control bus commands accomplish this by loading the appropriate parameters into interface processor program memory in the area of memory reserved for host unilateral transfers.

If synchronization by the host with data processor programs is desirable (for example, to ensure that a computation is complete before reading answers), the data processor must execute a call to the resident host synchronizing signal routine stored in data processor location 0. This routine interrupts the host to signal the occurrence of the synchronizing event. After waiting for this event, the host program commands the data processor to resume and perform the desired I/O operation. Fig 10 illustrates a possible sequence of program steps using this type of I/O.

Array processor arithmetic and control operations can proceed in parallel with data movement into and out of the array processor data memory.

Conclusions

Conceptually, the array processor can be treated as a black box with three fundamental divisions: architecture, software, and interfacing. Architecture determines instruction set capabilities, in addition to arithmetic type, speed, and precision; software emphasizes program development as a tradeoff with runtime efficiency or total system performance; and interfacing connects equipment to the array processor, to some extent involving both architecture and software.

Essentially, array processors are complex devices. In many instances, the hardware and software within the array processor are more elaborate and complicated than the host processor they serve. This is a natural consequence of their role, which is to provide better arithmetic and I/O performance than the host by several orders of magnitude.

A second layer of complexity arises from the increasing sophistication of host computer memory structures and supporting operating systems. Strictly a peripheral, the array processor must work through normal operating system control and data transfer channels; this leads to an increased overhead burden for the user and additional complications for the designer. Today, substantial resources are being devoted toward the objective of simplified interfacing and easier access via higher level languages within a host program.

Bibliography

P. Alexander, "Enhanced Computation for Industrial R&D," *Industrial R&D*, Feb 1980, pp 152-156; and May 1980, pp 111-114

P. Alexander, "Giant Computers in Small Packages," *Machine Design*, Aug 1979, pp 87-92

J. Allen, "Computer Architecture for Signal Processing," *Proceedings of the IEEE*, vol 63, no 4, Apr 1975, pp 624-633

S. P. Hufnagel, "Comparison of Selected Array Processor Architectures," *Computer Design*, Mar 1979, pp 151-158

E. W. Kozdrowicki and D. Theis, "Second Generation of Vector Supercomputers," *Computer*, Nov 1980, pp 71-83

R. Norin and T. Pettibone, "Programming Array Processors," *Mini-Micro Systems*, Aug 1979, pp 59-71

R. Sugarman, "Superpower Computers," *IEEE Spectrum*, Apr 1980, pp 28-34

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 713 *Average 714* *Low 715*

Free ECC for your LSI-11/23*.

DEC now offers LSI-11/23 without requiring you to buy their memory boards!

The choice is yours. You can buy regular memories, **or for the same price or less** you can have error checking and correction (ECC). That's ECC for free. Check our 100 quantity price: $992 for a full 256K byte system.

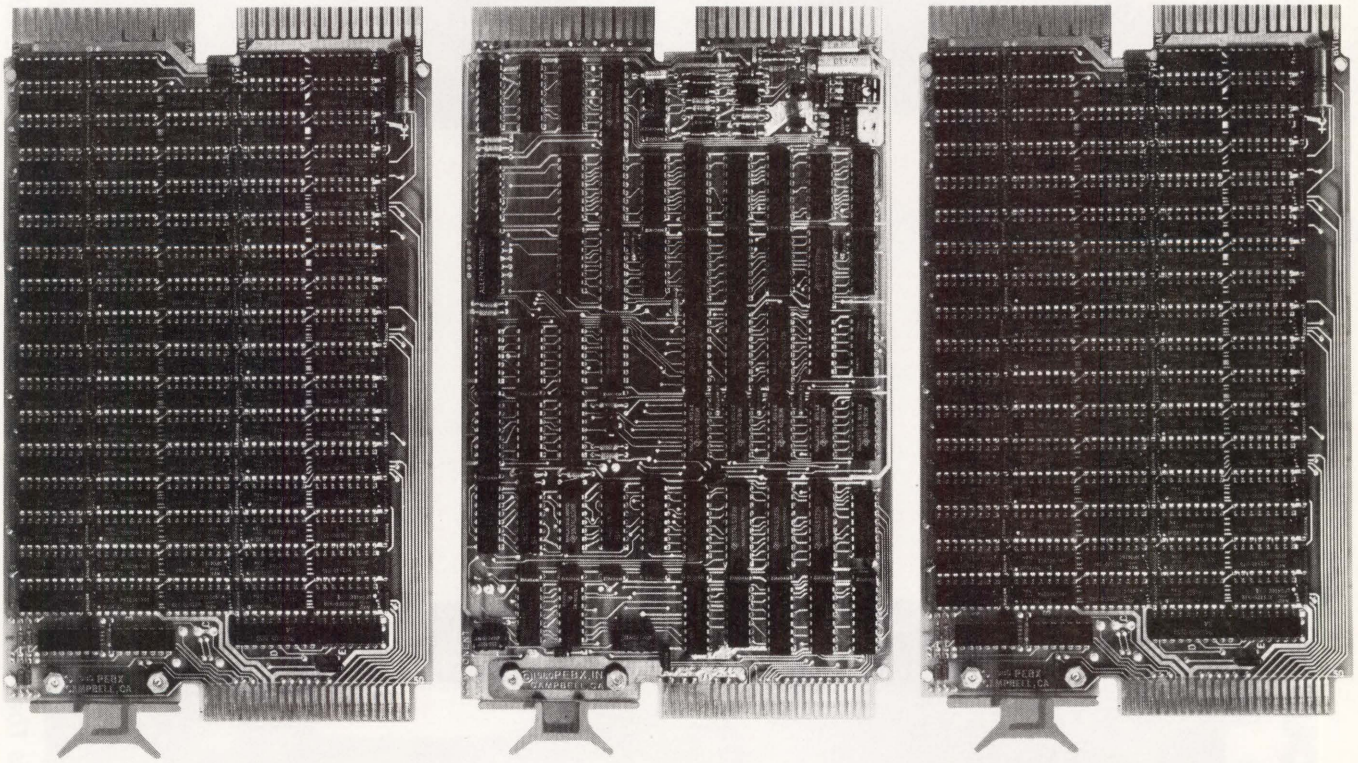
If you're an OEM, and you don't want to worry about loss of customer confidence or costly service calls, our error-correcting memories are for you. It's the best LSI-11 compatible memory system on the market. And we've got the data to prove it. We've more than 3000 ECC systems now installed in computers all over the U.S. and Europe.

PEBX is the first to protect your LSI-11 system from failing RAMs and random alpha particle crashes. Our easy-to-read LED display on the controller board can point out any failing RAM, while your full system continues to run error-free. And we've also made protection from power outages as easy as hooking up two battery wires.

Ordering's as easy as ECC, too. Simply call PEBX toll-free at 800/538-3112, or in California call 408/866-7838 for all the details about our LSI-11 compatible memory systems with **free ECC.**

PEBX

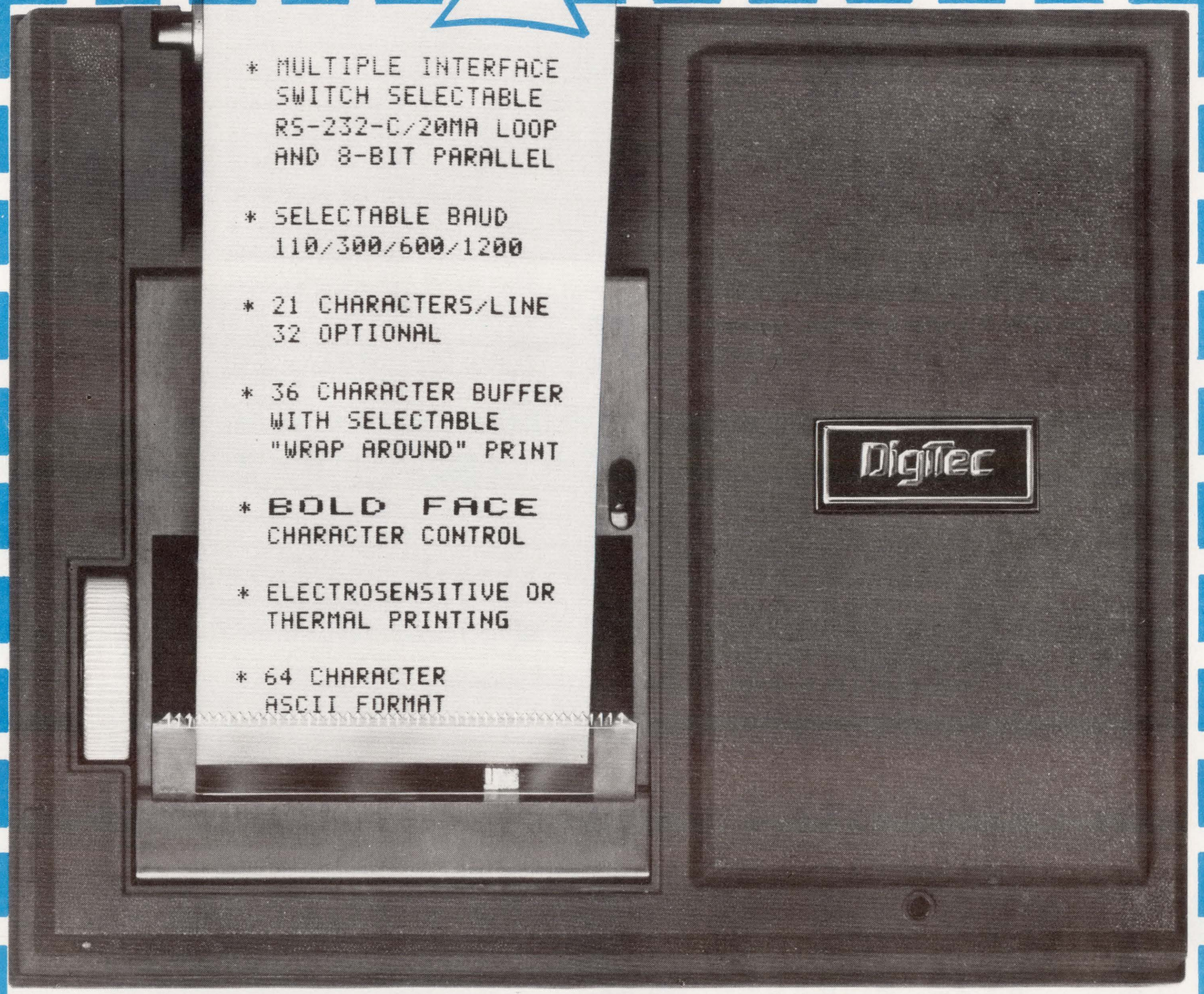
501 Vandell Way
Campbell, CA 95008
(408) 866-7838



*LSI-11/23 is a trademark of Digital Equipment Corporation.

CIRCLE 98 ON INQUIRY CARD

If your printer can't fit in this space and you're paying more than $299,* you're using the wrong printer.



This Is The Actual Size of DigiTec's New Low Cost Model 6430/6470 Printers 7.38"W x 3.08"H x 6.12"D, WT 3½ LBS.

DigiTec.
NON-IMPACT PRINTERS

We've opened a whole new world of printer applications to both the OEM and end user.

A built-in one chip microprocessor provides the simplest possible multiple interfacing. Just plug into the standard EIA connector.

You read first line-up . . . just like a book, its electric writing is quiet enough to use in a library . . . it's designer-styled to look good in any environment, . . . and

Who Else But DigiTec Warrants Their Printers For 1 Full Year.

$299.*

in 100 quantities
$399. List

DigiTec.

UNITED SYSTEMS CORPORATION

918 Woodley Road, Dayton, Ohio 45403
(513) 254-6251, TWX (810) 459-1728

ARBITER HANDLES SHARED RESOURCES FOR MULTIPROCESSOR

A priority rotation scheme used by a system arbiter allows multiple synchronous processors to share bus and resources

by Nicholas E. Scordalakes

A multiprocessing system configures more than one processor in an architecture that allows interprocessor cooperation in the execution of a common task. Most common multiprocessing architectures allow the processors to share a set of resources, such as memory and input/output. Increased system performance is possible because the processors simultaneously execute different portions of a target task; and increased system reliability results from modularity and module/data path redundancy. One failed module may decrease system performance, but will not necessarily cause a system failure. Fig 1 depicts a suggested architecture of a synchronous multiprocessor system, with n processors (P_1 through P_n), and k shared resources (R_1 through R_k).

In the suggested architecture of Fig 1, the processors transmit information to the shared resources over the shared, unidirectional DATA SEND bus. Since all shared resources have equal, fixed access times, data returned on the DATA RETURN bus will follow the order in which the shared resources were addressed. Arbitrating among the processors for the use of the DATA SEND bus is sufficient; after a fixed time interval following the address of a resource, the requesting processors can read returned data off the DATA RETURN bus.

Nicholas E. Scordalakes is a project engineer with Technology Marketing, Inc, 17862 Fitch St, Irvine, CA 92714. Mr Scordalakes has a BSEE from Cleveland State University, Cleveland, Ohio, and an MSEE from the University of Southern California, Los Angeles, Calif, which he received under the Hughes Masters Fellowship program.

Used to identify the availability status of each resource, the BUSY bus consists of k busy lines, one for each resource. The system arbiter receives n request lines, one from each processor, and provides n priority grant lines, one for each processor. A processor that must access a shared resource examines the busy line state of that resource. If the resource is indicated as available, it generates a request to the system arbiter, which then examines the state of all request lines and assigns DATA SEND bus access rights to one of the requesting processors by activating the corresponding priority grant line.

The arbitration scheme defines the order in which the system arbiter assigns priority rights to requesting processors.

The arbitration cycle is designated as the time required by the system arbiter to resolve priority rights among contending processors for DATA SEND bus access. This cycle determines the data transfer rate on the bus

transfer rate = (1/T) transfers/s

where T is the arbitration cycle expressed in seconds.

The arbitration scheme defines the order in which the system arbiter assigns priority rights to requesting processors. Employed by the system arbiter, this scheme is based on priority rotation. For example, if processor j is given the highest priority in the current arbitration cycle, then processor j + 1 will be given highest priority in the following arbitration cycle. The request/grant lines from the n system processors are configured to a closed loop daisy chain configuration. If the highest priority processor does not have a request, priority is

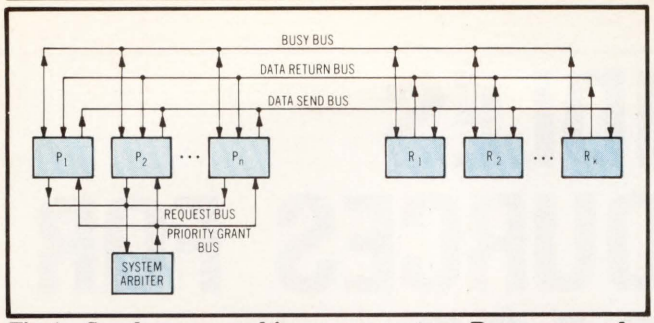


Fig 1 Synchronous multiprocessor system. Processors and shared resources operate synchronously with common clock. Here, n processors (P_1 through P_n) share k resources (R_1 through R_k)

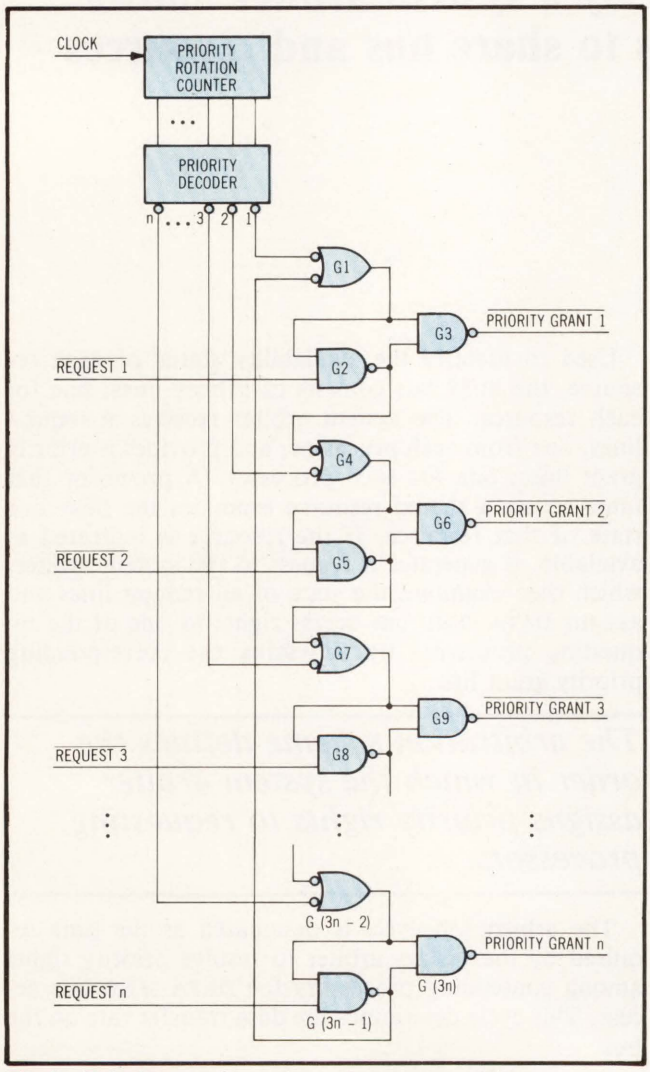


Fig 2 Priority rotation scheme for system arbiter implementation. During each arbitration cycle, when one or more request lines are active, system arbiter receives request line from each processor and activates one out of n priority grant lines

then passed to the next processor in the priority chain.

Fig 2 depicts the hardware implementation of the system arbiter. The priority rotation counter is configured to generate n distinct states. These states are decoded by the priority decoder, which defines the highest priority processor. The number of bits, k, required by the priority rotation counter is given by the inequality

$$(k - 1) < \log_2 n \leqslant k$$

Consider an arbitration cycle during which processor 1 is given the highest priority. Output 1 of the priority decoder will be active, causing the output of NAND gate G1 to be at its logical 1 state. If processor 1 has a request, then input request 1 will be at a logical 0, and the output of G2 will be at a logical 1. Since both inputs to G3 are at a logical 1, the output of G3 will be at a logical 0, and priority will be granted to processor 1. If processor 1 did not have a request, the output of G2 would be at a logical 0, and priority would be passed to the next device in line.

The arbitration cycle time T of a system arbiter for n processors is given by

$$T = tC + tD + tP + tS + (2n)tG$$

where:

tC = priority rotation counter delay
tD = priority decoder delay
tP = PRIORITY GRANT bus delay
tS = PRIORITY GRANT setup time
tG = NAND gate delay
n = number of processors

Arbiter signal timing of three simultaneous requests for three different resources is shown in Fig 3. During time period T1, all three processors arbitrate for the DATA SEND bus. Processor 1 has the highest priority and therefore is granted the bus during period T2. To prevent other processors from attempting to access that resource, processor 1 activates the busy line for resource 1 during period T2. The busy line is kept active as long as needed by either the requesting processor or the addressed resource. During period T2, processors 2 and 3 arbitrate for the bus. Processor 2 is granted the bus during period T3, as it has the highest priority. During period T4, processor 3 is granted the bus.

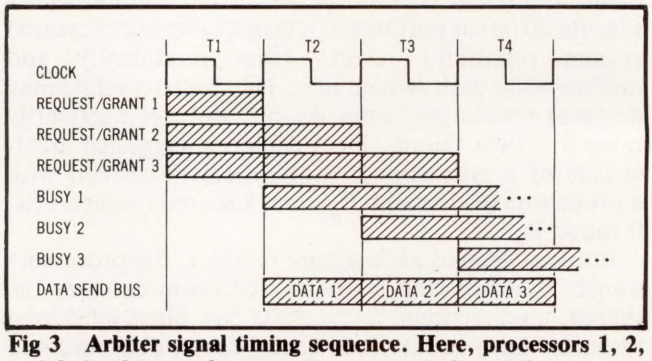


Fig 3 Arbiter signal timing sequence. Here, processors 1, 2, and 3 simultaneously request resources 1, 2, and 3

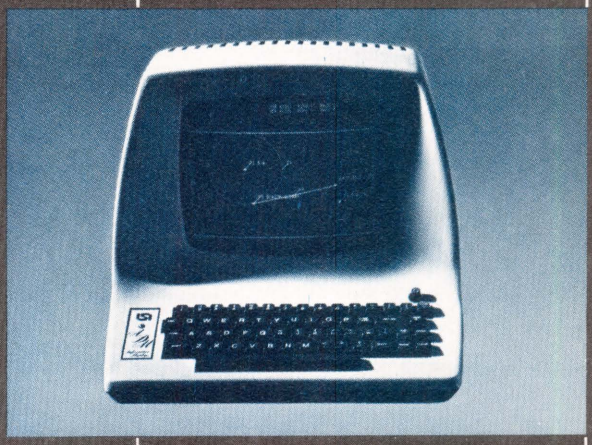
Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 716 *Average 717* *Low 718*

Plug-in Fiber Optic Modem Expands Capabilities of OEM Units

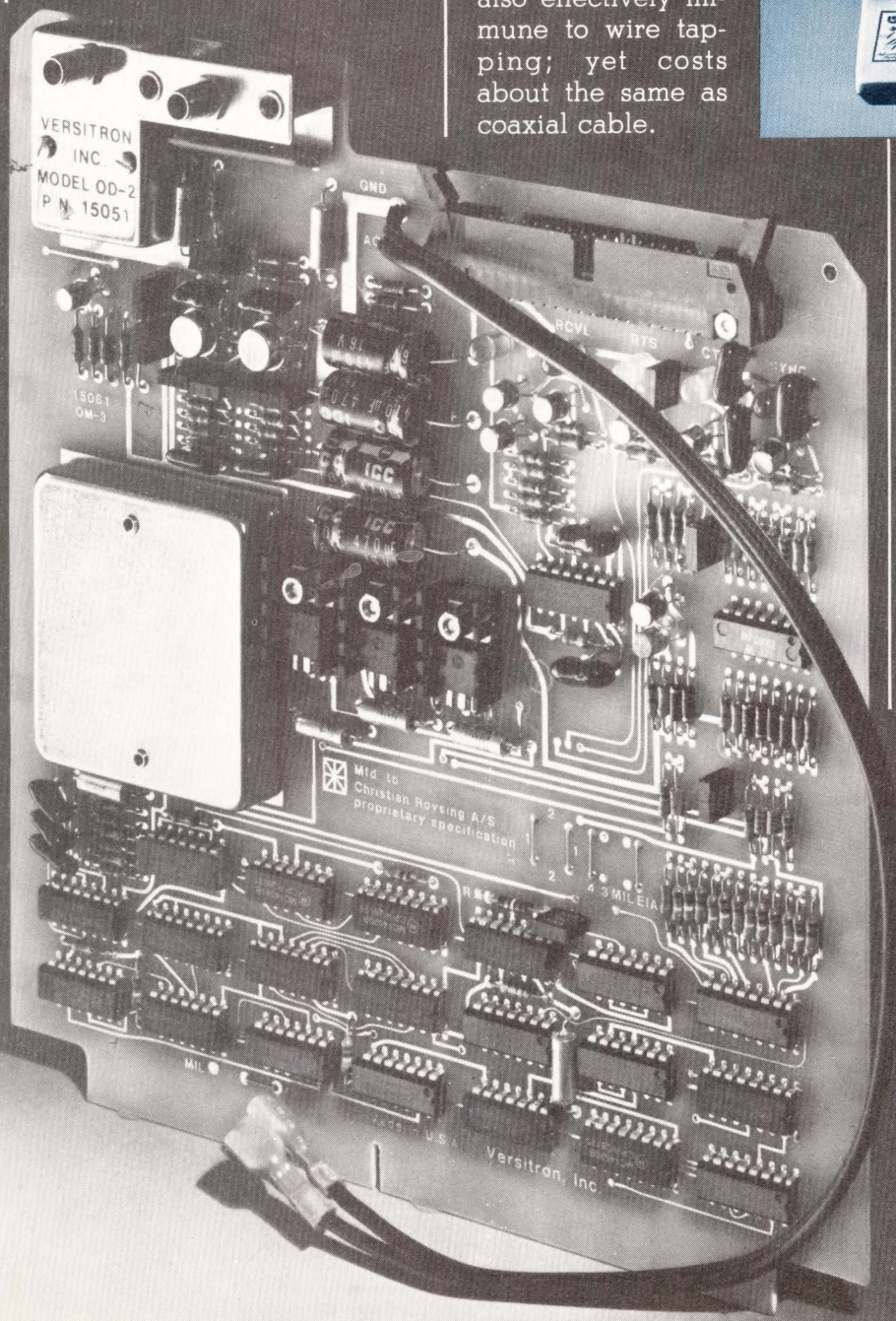
Equipment manufacturers can now integrate a powerful, new Fiber Optic Modem directly into their equipment; resulting in a device that will provide exceptional data throughput performance in any local distribution environment.

The Case for Fiber Optics: The use of fiber optics for local data distribution assures that your end product will perform as it was designed to; regardless of the environment in which it is used. Unlike conventional wire cables, optic cables are totally unaffected by rfi, adjacent noisy cables, or heavy duty electrical equipment. A big plus is that it is also effectively immune to wire tapping; yet costs about the same as coaxial cable.



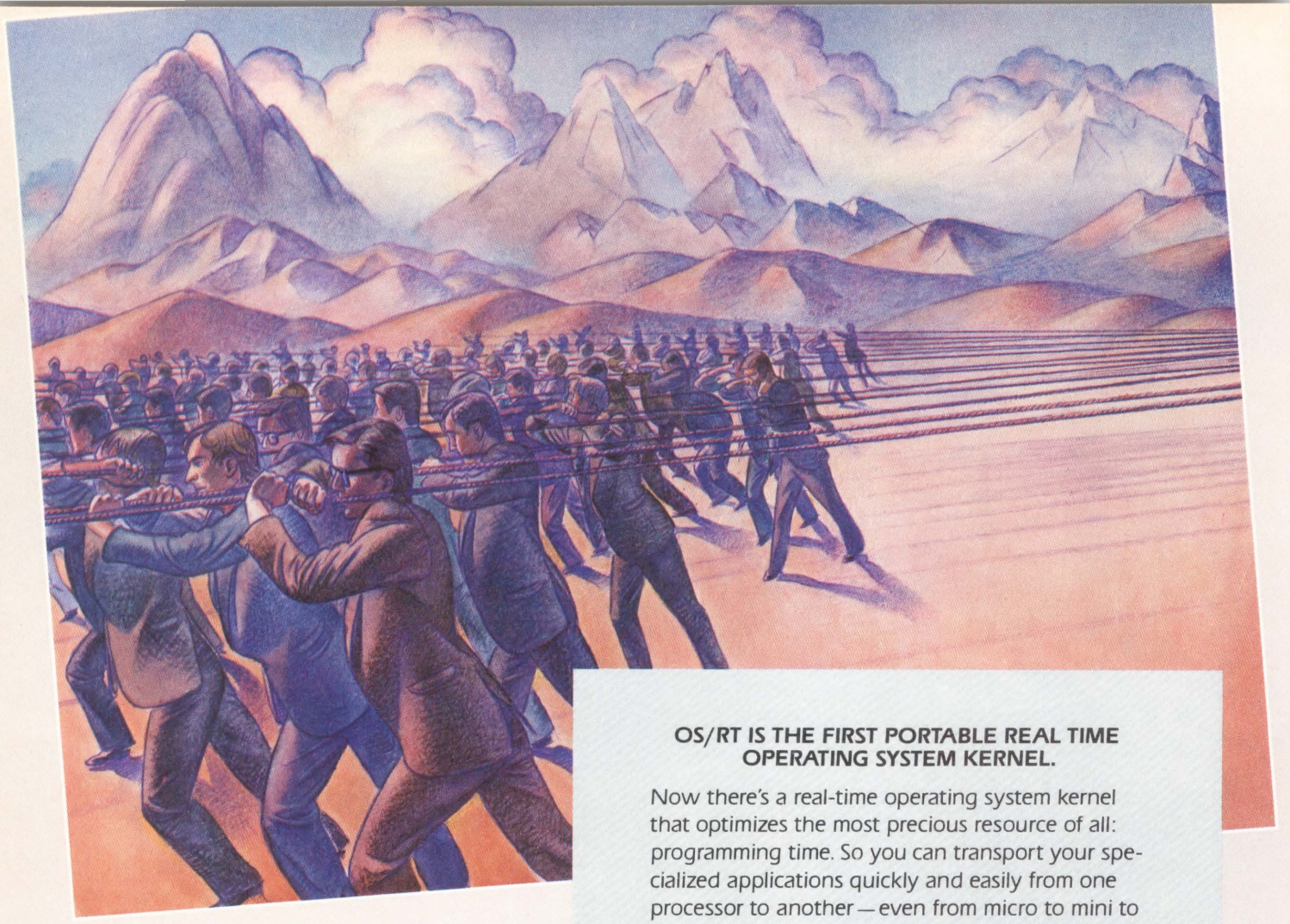
The Reasons for Using Versitron: In addition to the inherent advantages of fiber optics, Versitron's OM series of plug-in modems offers an impressive list of performance specifications. These include: operating range up to two kilometers (6500 feet), synchronous or asynchronous operation at data rates up to 38.4 KBPS, true EIA handshaking (three separate control signals in each direction are multiplexed along with the data), and an optional alarm circuit that will shut down all traffic if the cable is tampered with.

For details on how our optical modem can help you to significantly improve the marketability of your end product, give us a call at (202) 882-8464; or write Versitron, Inc., 6310 Chillum Place, N.W., Washington, D.C. 20011



VERSITRON, INC.

CIRCLE 100 ON INQUIRY CARD



INTRODUCING LABOR-SAVING SOFTWARE.

OS/RT IS THE FIRST PORTABLE REAL TIME OPERATING SYSTEM KERNEL.

Now there's a real-time operating system kernel that optimizes the most precious resource of all: programming time. So you can transport your specialized applications quickly and easily from one processor to another—even from micro to mini to mainframe. And devote your resources to developing new applications. Not reprogramming old ones.

OS/RT is ideal for electronic mail and message-switching applications. Not to mention process control, instrumentation, communications control and simulation systems. That's because OS/RT is written in "C." One of the most memory-efficient, code-conservative high level languages ever.

OS/RT is highly customizable. It includes all the functions you'd expect, including dynamic creation and destruction of resources, controlled resource sharing, and asynchronous event support. And with a very small amount of processor-dependent code, your applications are quickly generated on any computer that supports a "C" compiler.

OS/RT is budget-efficient, too. It is available in source code form with the rights for unlimited binary license basis, for only $8,000.

Call DESTEK toll-free at 800-227-9725 for complete details on OS/RT. We're the company developing state-of-the-art software and networking products to make your computing hardware more productive.

The DESTEK Group, 1923 Landings Drive, Mountain View, California 94043

DESTEK

WE BUILD ACCESS TO PRODUCTIVITY.

CIRCLE 141 ON INQUIRY CARD

INTERFACING CMOS DEVICES WITH OTHER LOGIC FAMILIES

Incompatibility of CMOS devices with other logic families can be overcome by considering input specifications

by Jonathan D. Luckey

Systems that mix different logic families often cause problems because of incompatibilities between various kinds of logic. With complementary metal oxide semiconductors, as opposed to most other logics which use transistors as the only active element, the incompatibility is often a result of their symmetrical push-pull internal structure. Using one type of active element can introduce an asymmetry into the logic level definitions, causing them to crowd one of the power supply lines. The symmetry of complementary metal oxide semiconductors causes logic thresholds to center around the midpoint between the supply lines. Incompatibility between logic types can occur because of differences in the arrangement of the logic thresholds.

Families and definitions

The most common logic families are transistor-transistor logic (TTL), complementary metal oxide semiconductor (CMOS), n-channel MOS (NMOS), p-channel MOS (PMOS), high performance MOS (HMOS), diode-transistor logic (DTL), resistor-transistor logic (RTL), and emitter coupled logic (ECL). DTL and RTL are all but obsolete. Because ECL is used in very high speed applications, it will rarely be found in the same system as CMOS. This discussion will therefore cover the interfacing of CMOS digital circuits to the remaining logic families. CMOS here usually refers to that running on a 5-V power supply. Exceptions are references to 10-V or ±5-V CMOS.

In defining logic levels, the voltage range is usually divided into three zones. One zone is called logic high, and is often designated as true. It includes all voltages above the logic high input threshold V_{IH}. The complementary zone is logic low, and includes all voltages below the logic low input threshold V_{IL}. Between V_{IH} and V_{IL} is a forbidden zone where the logic value is undefined. The worst-case output logic levels for the various types of logics are defined somewhere in the middle of the two corresponding logic level input zones. When noise is added to the signal, it does not cause the voltage level to cross a logic threshold. These output logic levels are designated V_{OH} for voltage output high, and V_{OL} for voltage output low. The minimum difference between V_{IL} and V_{OL} or between V_{OH} and V_{IH} is called the noise margin, since this is the maximum amplitude of additive noise the system can tolerate. These abbreviations are defined as follows:

V_{IL}	Maximum input voltage defining a logic low
V_{IH}	Minimum input voltage defining a logic high
V_{OL}	Worst-case (maximum) output voltage for a logic low
V_{OH}	Worst-case (minimum) output voltage for a logic high
Noise margin	Limit of the amplitude of noise that can be added to a worst-case system, equal to minimum $[(V_{IL} - V_{OL}), (V_{OH} - V_{IH})]$

Incompatibilities and limitations

In standard CMOS logic (such as the 74CXX series), the symmetrical structure of the p- and n-type metal oxide semiconductor field effect transistors (MOSFETs) provides logic thresholds that are centered around the midpoint between the power supply rails. This allows for wide logic level input zones and correspondingly high noise margins, but also makes it hard to interface the standard CMOS parts with other logic families. In Harris CMOS parts, the ratio between the complementary transistors in the input buffers was designed so that the logic thresholds group closer to the lower supply rail, similar

Jonathan Luckey is a CMOS applications engineer for Harris Semiconductor, PO Box 883, Melbourne, FL 32901. Prior to joining Harris, he worked as a systems programmer for Imlac Corp, and as an independent software consultant. He holds a BSEE degree in mathematics from Carnegie-Mellon University.

to the TTL family. This trades off a fraction of the noise margin toward TTL compatibility, but since the CMOS outputs swing from rail to rail, the degradation in performance is negligible.

As an example, a specification for a typical Harris CMOS part (in this case, the HD-6402-9 CMOS universal asynchronous receiver transmitter) follows. The operating temperature range is −40 °C to 85 °C. The operating voltage (V_{CC}) is assumed to be 5 V ± 10%. The parameters given are absolute worst case for the product. Typical parameter values are much better.

V_{IL} 20% V_{CC} = 1 V at V_{CC} = 5 V
V_{IH} 70% V_{CC} = 3.5 V at V_{CC} = 5 V
V_{OL} 0.45 V at I_{OL} = 2 mA
V_{OH} 2.4 V at I_{OH} = −0.2 mA

What may seem strange is that V_{OH} is less than V_{IH}, which gives a negative noise margin, meaning that V_{OH} is in the forbidden zone. V_{OH} would appear to fall in the forbidden zone, which would imply a negative noise margin. However, this is an illusion because V_{OH} is specified as sourcing a current of 0.2 mA, to drive a possible leakage current when interfacing to TTL. When connected to a CMOS input, this leakage current will be practically zero, allowing the output voltage to swing up to the rail, well above V_{IH}. Also worth noting is that V_{OL} is 0.45 V, which is 0.05 V above the TTL V_{OL}. This 0.45-V V_{OL} value is still well within the V_{IL} limit for TTL, but the noise margin is reduced 50 mV from that of a TTL only system: 350 mV as opposed to 400 mV.

The specifications for CMOS inputs require closer examination. The worst-case V_{IH} for the part is 3.5 V. The worst-case V_{OH} for TTL is 2.4 V, which would not appear to work. But when TTL is driving a load with a high dc impedance, such as with CMOS, the V_{OH} is typically above 3.5 V. The Harris CMOS inputs which are specified as $V_{IH} = V_{CC} - 2$ V work even better with TTL. In almost all applications, the CMOS inputs can be driven by TTL outputs with no problems; however, to guarantee 100% compatibility, the techniques described later should be used.

Fanout, the number of inputs that any one output can drive, is another limiting factor in logic design. It is limited because the impedance of the inputs is not infinite, and the impedance of the outputs is not zero. The limiting impedance can be either resistive or capacitive. In saturated logic families, such as TTL, either or both of the logic levels might require a dc current flow between input and output. Other logic families, including CMOS, have an almost infinite input resistance as a result of using MOSFET inputs, but still have capacitance. The charging time of the capacitance limits the speed of the system. The fanout depends on the frequency at which the system is required to operate.

General techniques

Two basic techniques exist for interfacing two different types of logic: passive and active. The passive technique connects the outputs of the driving device to the supply rails with resistors. These resistors are called pull-ups when connected to the upper supply rail, and pull-downs when connected to the lower supply rail. Pull-up/downs are used in two ways. In their simplest mode they merely increase current source/sink capability, but to do this they must be tied to an extra power supply that is lower than the low logic supply or higher than the high logic supply. In the other mode, which is more commonly used, the output voltage swing is brought closer to the rails. This mode takes advantage of the fact that most outputs do not supply current to the power supply rail nearest to the logic level output voltage. For example, a TTL output pulled up to the upper rail will have an output swing of nearly rail to rail. This is because the output does not sink current when it is high. Therefore the current through the pull-up resistor and the voltage across the resistor are both zero, and the output voltage is equal to the rail voltage. A disadvantage of this method is that when the output is near the opposite rail current will be flowing through the resistor. The output must be able to supply this current as well as provide the other inputs with the currents they require. The passive method will be discussed for particular cases. The active technique uses either buffer gates or simple transistor circuits to translate between logic level definitions. Buffers can be specially designed for this purpose, or they can be standard logic gates, which are empirically known to work as an interface between both logics.

Interfacing between TTL, HMOS, and CMOS

HMOS, a recent version of NMOS, has been designed to be TTL compatible, and can therefore be treated like TTL. The typical TTL circuit has a V_{IL} of 0.8 V and V_{IH} of 2 V. Its V_{OL} is 0.2 V and V_{OH} is 2.4 V. The current flow between an input and an output is small during a logic high state, but during a logic low state, the output must sink 1.6 mA for each input it is driving. A Harris CMOS output is specified to drive one standard TTL, or two lower power Schottky TTL (LS/TTL) inputs. If the output is specified as being capable of sinking 2 mA at V_{OL}, then it can also drive one input of either high power TTL (HTTL) or Schottky TTL (STTL).

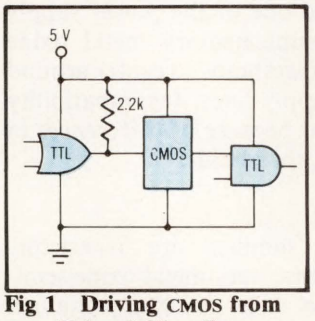


Fig 1 Driving CMOS from TTL. Using 2.2k pull-up resistor ensures sufficient V_{OH} from TTL output. Method brings V_{OH} to approximately 5 V and provides ample noise margin

Driving CMOS from TTL requires a different approach. The worst-case V_{IH} for a Harris CMOS input is usually specified as either 70% V_{CC} or V_{CC} −2 V. At a supply voltage of 5 V the former works out to 3.5 V, the latter to 3 V. The typical V_{IH} is usually 2 V, the same as a TTL input, but this is not guaranteed. The standard method of guaranteeing a sufficient V_{OH} from the TTL output is to use a pull-up resistor (Fig 1).

CMOS and exotic power supplied systems

CMOS must sometimes be interfaced to a logic system running on an exotic power scheme, such as CMOS running at 10 V or on split 5, −5 supplies, or PMOS running on 5, −12 supplies. Pull-up/down resistors are not recommended in this case because of the danger of

applying a voltage outside the operating range to the input, which could forward bias a static protection diode, with undesirable results. The standard solution is to use a buffer with a static protection circuit designed to allow use with pull-up/downs, or to use a simple resistor transistor circuit to translate between the systems. To translate from a high to a low level supplied system, a 74C901 or 74C902 device can be used. To translate from a low to a high level, an open collector (OC) type circuit can be used as a buffer with a pull-up to the higher supply. The resistor must be large enough so that the output can sink enough current to drive the output to the lower rail (a 10k resistor usually serves). Any of the TTL OC circuits will serve if the 5-V CMOS will drive them. The CMOS equivalents to the TTL OC circuits are open drain types, such as the 74C906 (Fig 2). Interfacing to logic where a voltage swing can go negative, such as in PMOS or in split supply CMOS, also presents the risk of forward biasing a protection diode. A 74C907 with a pull-down resistor on the output allows an interface from a CMOS system to a split supply system. 74C903 or 74C904 buffers allow an interface from split supply logic to CMOS (Fig 3). A buffer from CMOS to a split supply logic can also be made from one p-channel MOSFET. The open source of the p-channel FET is tied to the negative supply with a pull-down to the negative supply and then used as an output. This provides the necessary voltage swing for the split supply logic inputs (Fig 4).

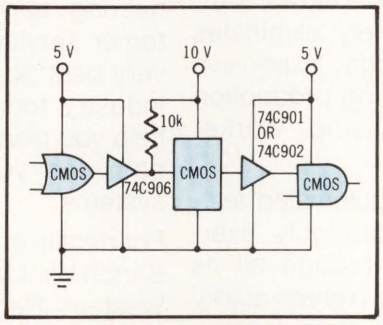


Fig 2 CMOS to 10-V CMOS interface. 10k resistor is used to pull up to higher supply. Open collector circuit is used as buffer. 74CXX circuits are low frequency logic family. Long propagation delays may degrade system performance

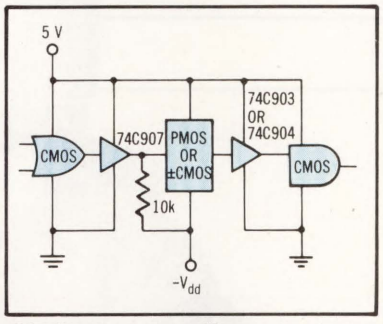


Fig 3. CMOS to split powered logic. 74C907 with pull-down resistor provides interface from CMOS to split supply system. 74C903 or 74C904 allows interface from split supply logic to CMOS

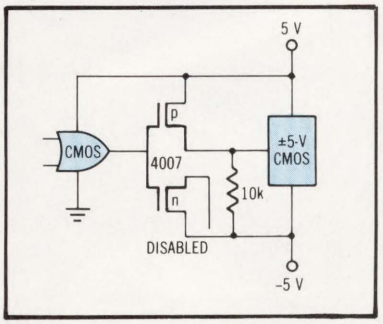


Fig 4 CMOS to split supply logic buffer. Buffer is p-channel MOSFET such as 4007 CMOS integrated circuit

Other considerations

When using the methods just described, factors beyond the ability to function must be considered. Discrete resistors may be used as pull-ups, but this complicates board assembly. The use of resistor networks permits 15 pull-ups to occupy one 16-pin dual inline package socket, but may complicate printed circuit board layout by crowding traces, which results in crosstalk. Noise margins may be different from the family standard at the interface; this may have an effect on the system. The effect of pull-up/downs on power requirements must be taken into account.

Transistor interface circuits may be cheaper than integrated circuit buffers, but device parameters may require various support components (eg, different resistors for different g_m values in FETs). The combination of different circuits should be regarded as a system, not just a collection of circuits.

Summary

When designing systems using mixed logic families, output logic levels must fall within the input logic zones, leaving a sufficient noise margin. If not, suitable conversion circuits must be used at the interface. Outputs must provide sufficient current to drive the impedances of the inputs. Logic level conversion circuits must not generate voltages outside the allowable operating limits of the CMOS devices.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 719 *Average 720* *Low 721*

"As OEMs discover the advantages of Quantum 8-inch Winchester drives, the demand grows daily. In Manufacturing, we're prepared to meet high-volume OEM commitments."

A very manufacturable disk drive.

Quantum's 10, 20, 30 and 40-megabyte Q2000 disk drives were designed to be built in high volume at low cost.

Working as a team, Quantum design and manufacturing engineers created a drive that gives you better performance than the industry-standard 8-inch Winchester, yet can be manufactured with simple, low-cost parts and fast, efficient production methods.

Low-cost, high-volume production.

To meet your low-cost, high-volume delivery requirements, we designed our manufacturing process as carefully as we designed the drive itself.

Our unique conveyorized "clean-air tunnel" combines the best of proven techniques for Winchester drive assembly. The drive is assembled on a conveyor line, so production is more efficient than with independent assembly stations. And the laminar-flow clean-air tunnel completely eliminates the need for a large, expensive "clean room," cutting production costs and increasing worker efficiency.

Specially-designed automated testing equipment thoroughly exercises each drive through all its functions, to assure highest quality while keeping labor costs down.

Every manufacturing operation is planned for easy, smooth expansion to meet growing OEM requirements.

In short, we're geared for low-cost, high-volume production of quality disk drives that we're proud to deliver to you.

Get to know Quantum now.

From manufacturing and engineering to marketing and customer service, Quantum has the very best people in the disk drive industry today. People who can help you plan an affordable growth path for your small computer systems.

For details on Quantum's low-cost 8-inch Winchester drives, call our Western Region Sales Office at (408) 262-1100, or our Eastern Region Sales Office at (603) 893-2672. Quantum Corporation, 1804 McCarthy Blvd., Milpitas, CA 95035.

QUANTUM ***Driving down the cost of quality.***

CIRCLE 143 ON INQUIRY CARD

A BUILDING BLOCK I/O PROCESSOR SUBSYSTEM

High speed networks can be handled, without tying up the CPU, through an intelligent I/O processing subsystem formed of Z-Bus family components

by Steven A. Sharp

Problems of providing input/output at a rate high enough to handle high speed networks without tying up the central processing unit are commonly solved by using a direct memory access controller. Another solution is to construct an input/output processing subsystem from standard building blocks. Savings in development costs, combined with performance attained, make this approach an attractive alternative to a direct memory access controller.

Z-BUS family components can be put together to create a subsystem that handles input/output (I/O) processing in the absence of a direct memory access (DMA) controller. This subsystem can be used either with a larger Z8000™ system or with another common microprocessor. The I/O processor subsystem takes the form of a satellite processor with a high speed data link that can handle the I/O chores without overburdening the main central processing unit (CPU). Design of the subsystem (Fig 1) can be examined in three stages: basic CPU/memory kernel; CPU kernel plus I/O; and CPU kernel, I/O, plus high speed first in, first out (FIFO) interface to the host system.

CPU/ROM/RAM kernel

A basic kernel to which various peripherals will be added to obtain the functions needed for I/O processing and data transfer, this stage consists of a Z8002 CPU, two Z6132 quasi-static random access memories (RAMs), and two 2716 erasable programmable read only memories (EPROMs). Duplicate memory elements are needed—one for the high byte and one for the low byte—because of the way in which words and long words are addressed in the CPU. This configuration provides 4k bytes of firmware storage, expandable in 4k increments, and 8k bytes of RAM, expandable in 8k increments.

The RAMs were chosen because of their high density (4k x 8 per package) and their quasi-static design, which makes refresh transparent to the user. Except for chip select decoding circuitry, they attach directly to the Z-BUS with no additional circuitry. The EPROMs were chosen because they are widely available, industry standard devices that can be programmed with a variety of commonly available development tools.

CPU kernel plus serial and/or parallel I/O

Adding several peripheral devices to the CPU kernel provides the ability to perform I/O functions. Logical choices are the Z8036 counter/parallel I/O unit (Z-CIO) and the Z8030 serial communications controller (Z-SCC). Both are directly Z-BUS compatible and attach to the CPU with minimum effort. They require only chip select decoding in addition to the standard bus signals already available from the CPU. To provide priority resolution, they are also designed to work the CPU's interrupt priority daisy chain. (See Fig 2.)

Three 16-bit counters, two of which can be chained together to form a 32-bit counter, are contained in the I/O unit. In addition, it has two 8-bit parallel I/O ports and one 4-bit port that provides handshaking signals if desired.

The communications controller has two independent, full-duplex channels that may operate from 0 to 1M bits/s in asynchronous, synchronous, or synchronous data link control/high level data link control (SDLC/HDLC) modes, available with nonreturn to zero (NRZ), nonreturn to zero inverted (NRZI), or frequency modulation (fm) data encoding. Moreover, each channel has its own crystal oscillator, baud rate generator, and digital phase locked loop for clock recovery.

It is possible to add as many of these serial and/or parallel I/O devices as are needed to produce a sub-

Steven A. Sharp is a product marketing engineer at Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014. Prior to joining Zilog, he was a hardware and software design engineer at GenRad, Inc. Mr Sharp has a BSEE degree from Cornell University.

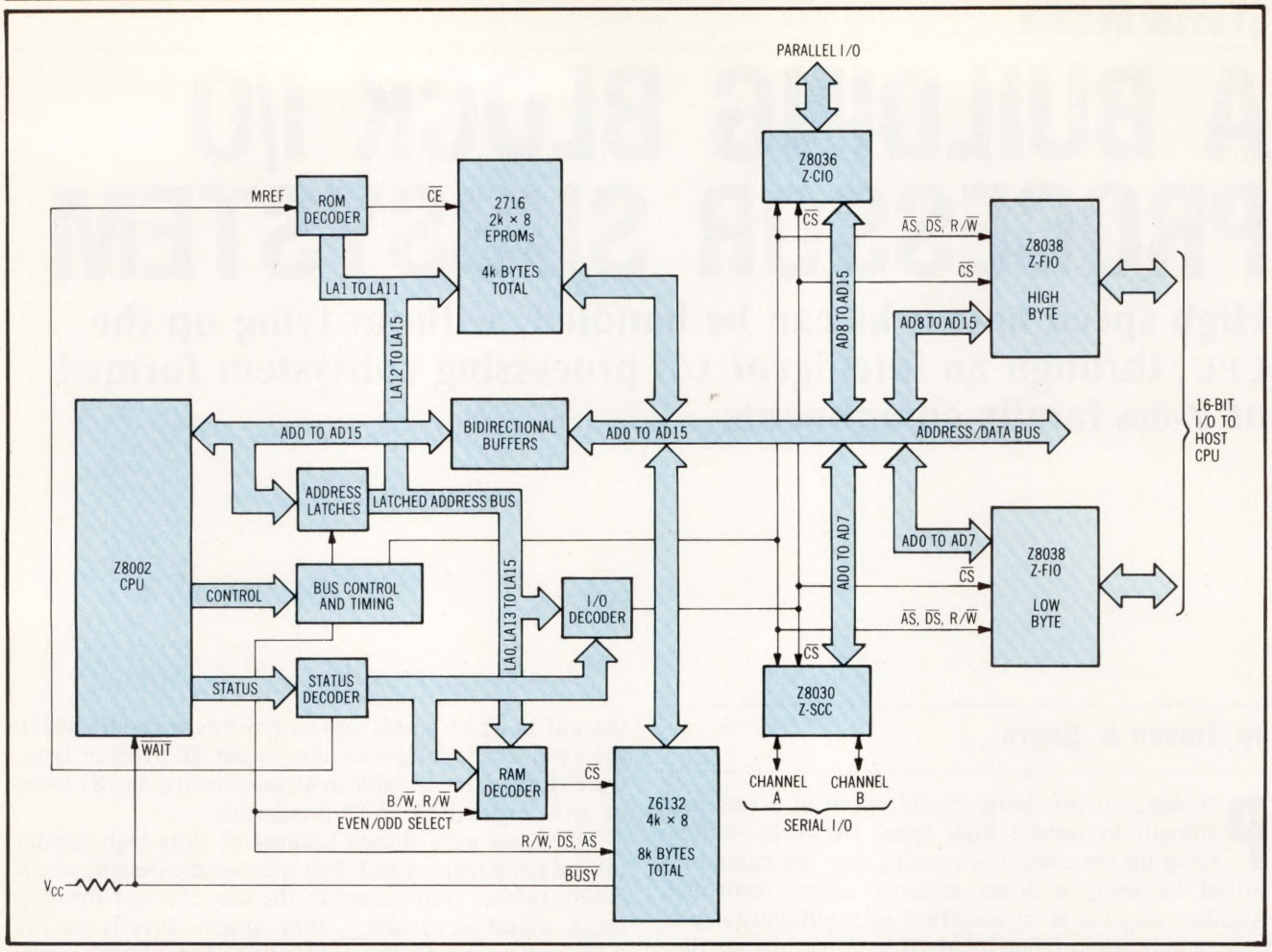


Fig 1 IOP subsystem. Put together using Z-BUS compatible components, subsystem takes form of satellite processor with high speed data link that handles I/O tasks to offload main CPU. CPU, two RAMs, and two EPROMs form basic kernel; parallel I/O unit and serial communications controller add ability to handle I/O; and data transfer to host occurs through FIFO interface

system capable of handling I/O functions. However, only the high speed data link need be added to provide I/O processing for a host system.

CPU kernel, I/O, and FIFO interface to host CPU

The small system already developed is capable of performing I/O and computational functions. Transferring data to a host CPU is accomplished by adding the Z8038 Z-FIO interface unit.

A 128 x 8 FIFO buffer, the Z-FIO expands to 16 bits in width using two interface units, one in Z-BUS high byte mode, and the other in low byte mode. Depth can be expanded to 256 bits by using two interface units back to back in each byte path. For this application, however, a depth of 128 was considered adequate (and more desirable) because of the reduced parts count.

The dedicated "mailbox" register with interrupt capability provides CPU to CPU communication independent of the FIFO buffer, and allows a variety of protocols to be implemented. Because the host CPU side of the interface units can be programmed as a Z-BUS interface or as a general microprocessor interface, the subsystem can be used with either the Z8000 or with another common microprocessor. Under programmed I/O control, a Z8000 can transfer data words to or from a pair of Z8038s at 750k bytes/s which is within the range provided by most DMA controllers. In addition, the necessary software is easier to design because transfers occur under program control, without the need for bus requests and arbitration. The result is an I/O processor (IOP) subsystem with several readily apparent performance benefits.

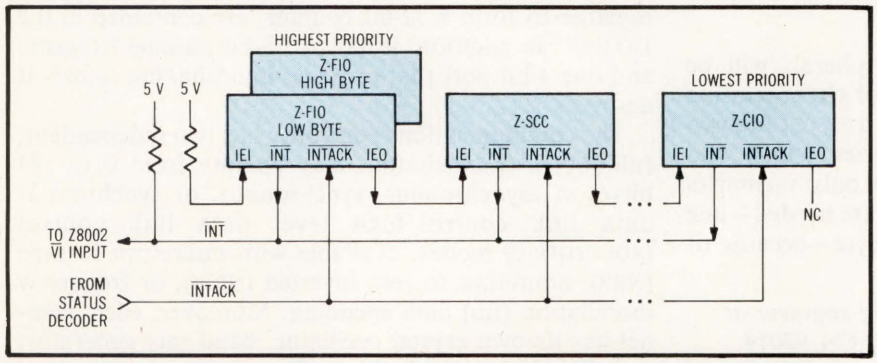


Fig 2 IOP interrupt control logic. Designed to work with CPU's interrupt priority daisy chain, counter/parallel I/O unit and communications controller require only chip select decoding to provide priority resolution

Resolving priority conflicts and collecting data, the IOP takes on the burden of processing interrupts

from various I/O devices. It can format data (doing byte packing if desired), recognize error conditions, and then send data to the host over the high speed interface unit link.

Structure of the IOP creates a modularity of I/O function, leading to programs that are easier to write, debug, and understand. "Variable record length" I/O is readily supported because of the ease with which the two CPUs can communicate through the mailbox register of the interface unit. The Z8038s are set up with port 1 sides connected to the IOP, so that the IOP controls the direction of data transfers. An appropriate message protocol provides the host CPU with handshaking enabling it to know when to send or receive data. The interface unit's interrupt logic can be used advantageously to detect the presence of a mailbox message or a change in data direction.

As an example of the kind of software involved, consider how the Z8002 sends a 128-word block of data to the Z-FIOs. This code assumes that the two Z-FIOs are addressed so that they respond to the same I/O addresses, one on the high byte of the address/data bus and the other on the low byte. It also assumes that they are set up to transfer data from the IOP to the main CPU at the time this code is executed.

```
LD R1, FIODATREG        !Load I/O address
                         of FIO data buffer
                         register !
LDA R2, DATABUFFER      !Load address of
                         RAM buffer !
LD R3, #128             !Load number of
                         words to
                         transfer !
OTIR @R1, @R2, R3       !Send block of
                         data !
```

Software tasks in the IOP include system initialization, I/O device initialization, I/O device service routines, data processing routines, and data transfer routines. System initialization involves all tasks necessary to start the system running, such as initializing the system stack pointer and setting up the processor status area so that interrupts may be processed. I/O device initialization involves setting up all of the I/O devices for the proper operating modes (ie, synchronous vs asynchronous in a Z-SCC), loading interrupt vectors into the I/O devices, and other device-related programming such as setting baud rate generators and pattern recognition logic.

I/O device service routines are those sections of code that are activated when an interrupt is received from an

The dedicated "mailbox" register with interrupt capability provides CPU to CPU communication independent of the FIFO buffer...

I/O device. One type of action performed in such a routine is to get a character from a serial I/O channel and put that character into a local buffer. Another example is to get a message byte from the Z-FIO mailbox register and dispatch control to the correct processing routine, based on the action requested by the main CPU.

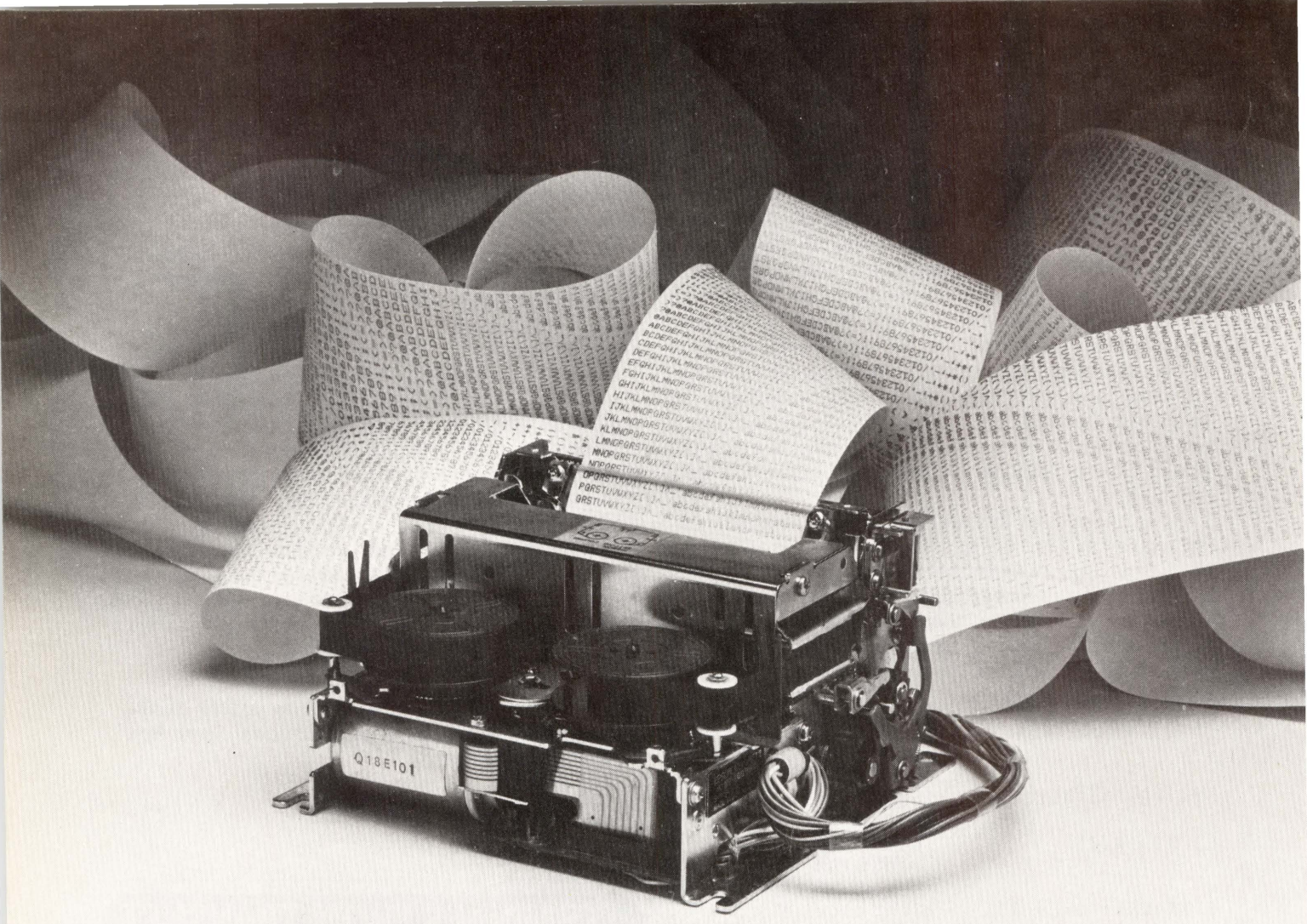
Data processing routines perform any necessary processing on the data being sent or received from the various I/O devices. This processing depends on the protocol set up between the host CPU and the IOP. Data transfer routines perform the actual transfer of data between the IOP and the host CPU. Primarily, this involves transfer of data to or from the Z-FIO and a local data buffer. In order to maintain modularity in programming, any necessary processing would be performed by either the appropriate I/O service routine or the data processing routines.

Conclusion

Constructed using simple Z-BUS building blocks, this I/O processing system provides high throughput, flexible configuration, and ease of programming. All development tools used to develop the Z8000 system hardware and software are also useful in developing the IOP hardware and software. This "economy" of development, a factor often ignored, should be carefully considered before deciding to design with another processing element. Savings in development costs, combined with high performance and easy system design, make the subsystem an attractive alternative to DMA in solving system I/O problems.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 722 *Average 723* *Low 724*



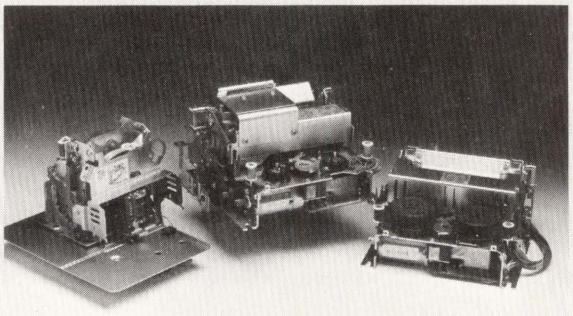
OUTRUNS THE COMPETITION.

The print head on a C. Itoh 500 series dot matrix printer prints out over 100,000,000 characters in its lifetime. That's a lot of cash register receipts. A lot of journal entries. It's one reason why C. Itoh printers are among the most reliable in the industry. And the most popular.

Of course, every series 500 printer is also long on features. Each is bi-directional. Each prints a fast 152 CPS. But best of all, there's one just right for your application. Our Model 512, for example, is the perfect journal printer with 40-column printout for a variety of applications. The Model 522, on the other hand, gives you two-stage 18-column journal/18-column receipt printing complete with logo stamp and automatic paper cutter for cash register applications. For efficient flat bed ticket or slip printing, the Model 542 40-column unit is the one to buy.

C. Itoh Series 200 printers are equally impressive. Compact and rugged, each requires just 24VDC and prints 5x7, 7x7 or 9x7 matrices at 2.4 LPS from a reliable 7-wire print head. They're the OEM's choice for cash registers, home computers, data loggers, electronic calculators and general peripherals. Choose the Model 210 roll-fed printer with 26-35 column capacity. Or the sprocket-fed Model 210S with 22-30 columns. You get 2-color printing either way. For dual-roll applications, the Model 220 records receipt and journal entries and features auto-stamp and independent high-speed line feed. And for multi-ply slip document applications, there's the Model 240 featuring an adjustable document stop gate.

So if you're looking for a little printer with a lasting impression, contact C. Itoh Electronics, Inc., 5301 Beethoven St., Los Angeles, CA 90066; Tel. (213) 306-6700. New York office: 666 Third Ave., New York, NY 10017; Tel. (212) 682-0420.



C. ITOH ELECTRONICS, INC.

One World of Quality

CIRCLE 145 ON INQUIRY CARD

ERROR CORRECTION THE HARD WAY

A double complement correct cycle in an ECC system forms a sophisticated double-bit error correction and management system

by Bob Nelson

The use of parity, the most common error detection method, can be expanded from simple error detection in data words to the correction of single-bit errors by means of a double complement correct cycle. The double complement method can also be used to advantage in combination with error checking and correction systems to detect and correct hard and soft combinations of double-bit errors, provided no more than one of such errors is soft. In addition, this technique points the way to more sophisticated double-bit error correction and error management systems.

A parity bit is assigned a value of 1 or 0 on the basis of the number of 1s in the data word. The value of the parity bit depends on whether the parity system chosen is odd or even. Thus, in an odd parity system, the sum of the 1s in the data word and the parity bit will always be odd, whereas in an even parity system, the sum of the 1s in the data word and the parity bit will always be even (Fig 1). All examples in this discussion, except for those in Fig 1, use odd parity. A single parity bit can be used to detect a single-bit error occurring during a memory read cycle, and the technique can be expanded to provide even further error handling.

Data Word	Parity	Number of 1s	System
10001010	1	4	even
10001010	0	3	odd
01101001	1	5	odd

Fig 1 Odd and even parity. Value of parity bit is generated to satisfy chosen parity system (even or odd) so that sum of all 1s, including parity bit, will conform to even or odd parity system

Parity error detection and correction

During a memory write, the parity bit which is created as a result of the data is written to the memory along with the data word for storage. When a read cycle occurs, parity generation is again performed on the data word, creating a new parity bit, which is then compared with the original parity bit read from memory. If a difference exists between the two parity bits, an error has occurred. Although this error cannot be located with the information given, and may have occurred in any bit location in the data word or even in the parity bit, if it is a hard error, its location can be determined through the use of additional memory cycles.

If an error is detected during a memory read cycle, a simple procedure called the double complement method will determine if the error is hard, and, if so, correct it. The method includes a routine during which the suspect data and parity bit are complemented and presented to the same location in memory for a write cycle. Following the write, a read cycle is performed, and if the error is a hard error, the memory will repeat it by providing the data with the error bit complemented again. After a second complement, the data will be correct. At the end of such a correct cycle the memory contains the complemented data, and one additional write cycle must be performed to restore the data in memory (Fig 2).

During a double complement correct cycle involving a data word containing an even number of bit locations, the parity test is performed after the second read and before the second complement. If the error is hard, a parity error will once again be detected following the second read. If the error is soft, a parity error will not result following the second read. For data words containing an odd number of bit locations, parity testing

1st write	11010011	0	original data
1st read	11010111	0	PE (parity error)
D→$\overline{D}$	00101000	1	data are complemented
2nd write	00101000	1	complemented data
2nd read	00101100	1	PE (parity error)
$\overline{D}$→D	11010011	0	data are complemented

↑ hard error location

Fig 2 Hard error correction with parity. Single parity bit can be used to correct single-bit hard error with double complement method. On each memory read, original parity bit is read and new parity check is done on bits in data word. New parity bit is then compared with that read for validity

Bob Nelson is responsible for digital systems applications and new product definition at National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. His engineering career began at the Burroughs Corp, where he worked on semiconductor memory systems and system interface design for large mainframe computers. Mr Nelson completed his basic engineering studies at Citrus College, Azusa, Calif, following undergraduate work at Pasadena City College.

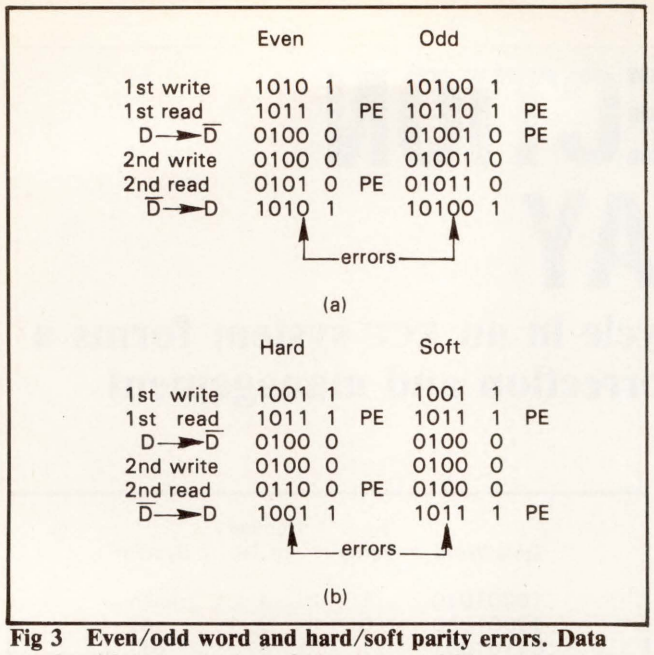


Fig 3 Even/odd word and hard/soft parity errors. Data words with even number of bits do not yield parity error on second read (a), nor soft error (b). Hard error, however, will be corrected

must be performed at different times during the correct cycle. In both cases, a double complement correct cycle can determine the type of error and, if it is hard, correct it (Fig 3).

If the bit in error is hard, the double complement correct can also be used to determine the bit's location in the data word. To do this, the data word and parity must be stored in a register when an error is detected. At the conclusion of the hard error correcting cycle, the location of the failing bit is determined by comparing the correct data with the contents of the register (Fig 4).

Thus, the use of a single parity bit not only makes it possible to deduce the error type, but also to locate and correct hard errors. This technique is useful for low cost terminal and word processing systems since, where retry is acceptable, the small amount of additional hardware

...the double complement method...also points the way to more sophisticated double-bit error correction and error management systems.

required can often eliminate the cost of an unscheduled service call. If a hard error can be detected, a double complement correct cycle will correct it, and the technique combined with an error checking and correction (ECC) system can also provide extended error correction capability when hard errors are involved.

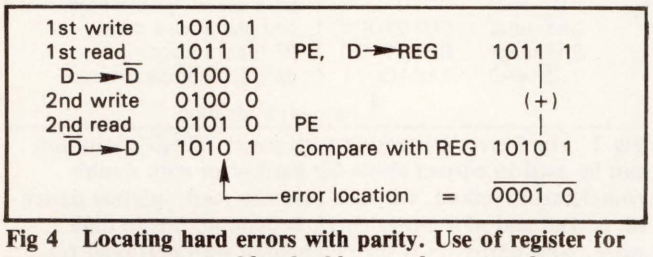


Fig 4 Locating hard errors with parity. Use of register for temporary storage enables double complement cycle to locate single hard error

ECC and double complement

The double complement method in combination with an ECC system can correct additional errors, both hard and soft. The ECC system under discussion here uses the code implemented by National Semiconductor in the DP8400 ECC device (Fig 5) to perform 1-bit error correction and 2-bit error detection. In an ECC system for 16-bit data words, such as the one discussed here, six parity bits are generated. Each of the parity bits is assigned a value as a function of the sum of the 1s in a unique combination of selected bits in the data word. Partial word parity bits in an ECC system are referred to as check bits. For simplicity, odd parity will be used in the examples, although in most ECC systems, including those implemented with the DP8400, a combination of odd and even parity is used to improve memory diagnostic capabilities.

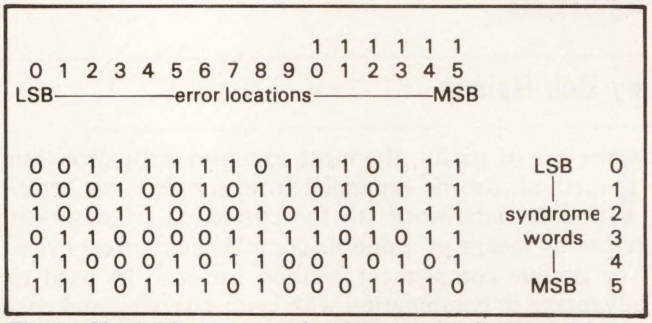


Fig 5 Check bit generator for data words. Code used is that implemented in National Semiconductor's DP8400 ECC device

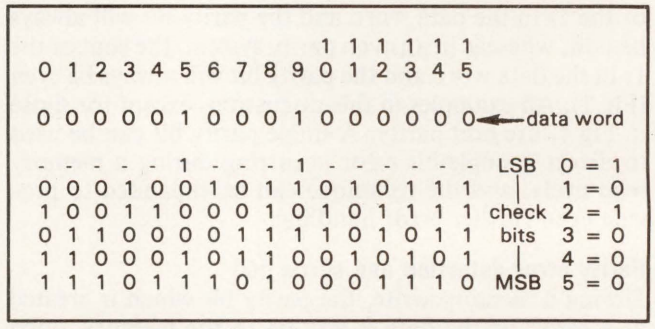


Fig 6 Error check bits are generated by presenting the data word to ECC code matrix and noting corresponding 1s. In first row, bits 5 and 9 correspond with 1s in matrix. Thus, to maintain odd parity LSB of check bits is set to 1

An ECC code forms a matrix (Fig 6) to which a data word can be presented for the generation of check bits. Given a data word, such as 0000010001000000, and the uppermost horizontal row of the matrix in Fig 7, check bit 0 is to be assigned a value based on the sum of corresponding 1s in that row and the data word. Using odd parity, the corresponding 1s in locations 5 and 9 dictate

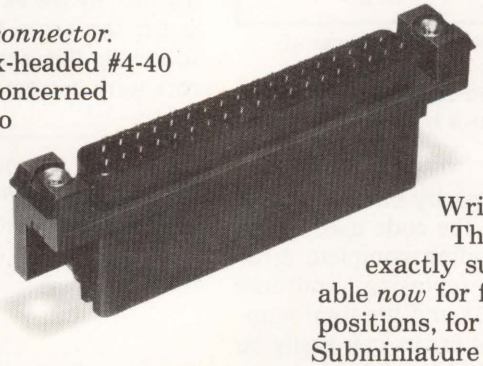
CABLE VISIONARY

New Holmberg D Sub accepts both RS 232 and RS 449 cable assemblies.

Holmberg Electronics announces the first D Subminiature Right Angle Female mounting system with a "built-in" future.

It's our new *Style J universal connector.* Featuring molded-in latch *and* hex-headed #4-40 threaded insert. So you're never concerned about the type of cable assembly to be plugged into your equipment. Because Style J accepts *both* industry standards — RS 232 and RS 449.

In fact, Holmberg offers a whole family of mounting styles to make mounting fast and easy. They eliminate loose washers and nuts. So there's nothing to inventory or fumble with ...no pre-assembly on the line. Your in-place costs drop dramatically as production efficiency climbs!



The wide variety of styles lets you select the most convenient and cost-effective option, using off-the-shelf components. Every Holmberg D Sub receptacle is built to the highest quality standards. With rugged dependability. Extra economy. And innovative features that enhance solderability, contact retention and reliable performance. Write for free specification data today. Then choose the mounting styles that exactly suit your applications. They're available *now* for fast delivery — in 9, 15, 25 or 37 pin positions, for positive mating with *all* makes of D Subminiature male connectors.

Holmberg Interconnects — they get into your system!

HOLMBERG ELECTRONICS

The Board Interconnect Professionals

Asheville Highway
Inman, South Carolina 29349
(803) 472-2821

17071 Murphy Avenue
Irvine, California 92714
(714) 556-2930

CIRCLE 106 ON INQUIRY CARD

Write	0000010001000000	000101	
Read	0000010001010000	000101	error in 11
Generate	0000010001010000	010110	new check bits
XOR check bits		010011	syndrome bits

Fig 7 Generating syndromes for locating error. Syndrome word is result of exclusive OR (XOR) of error check bits. No-error condition would result in syndrome word of all 0s

a value of 1 for the parity bit. For check bit 1, the selected location of correspondence is 9 only. Check bit 1 is assigned a value of 0 for odd parity. The complete set of check bits for this particular word is 000101 (05 HEX).

After check bit generation, the data and check bits go to the memory. During the read a new set of check bits are generated and compared against the check bits read from memory. The results of this check bit compare, an exclusive OR (XOR) function, are the syndromes (Fig 7). The single error indicating syndrome word is unique and is interpreted by the syndrome decoder to indicate the column in the matrix corresponding to the error location. The matrix or code is therefore a check bit generator for data, but a syndrome generator for error locations.

The...method in combination with an ECC system can correct additional errors, both hard and soft.

	5 9		
1st write	0000000000000000	110011	original data
1st read	0000010001000000	110011	2 errors
D→D	1111101110111111	001100	complement
2nd write	1111101110111111	001100	
2nd read	1111101111111111	001100	hard error fixed
D→D	0000010000000000	110011	complement
		000010	new check bits
		110001	syndromes for bit 5

Fig 8 Correction of hard and soft errors. In the case of data word with one hard and one soft error, double complement method has corrected hard error and determined existence of soft error, which is then located by syndrome word and can be corrected

The check bits, or partial word parity bits, generated by modified Hamming codes and the code used in the DP8400, are also capable of providing complete error reporting. Since the single error reporting syndrome words contain an odd number of 1s and the total number of 1s is greater than one, 2-bit errors can easily be distinguished from a 1-bit or detectable triple-bit error. The DP8400 monolithic ECC device performs this error determination by counting the number of 1s in the error indicating syndrome words. When no error exists, the syndrome word contains no 1s, and when a single check is in error, a single 1 is present in the syndrome word. When an odd number of data bits are in error, the number of 1s in the syndrome word is odd and greater than 1 (3 or 5 in this example); if an even number of bits are in error, the syndrome word contains an even number of 1s greater than 0 (2, 4, or 6).

An ECC system implemented with the DP8400 can, at minimum, detect 100% of 2-bit errors; all of these errors are correctable if no more than one of them is soft. The device has complement write and read modes to allow the double complement correct technique to be used with no additional hardware, and other ECC devices can be used with additional components to implement the function.

In Fig 8, a soft error exists in location 5 and a hard error in location 9. During a memory read, the generated

The matrix or code is...a check bit generator for data, but a syndrome generator for error locations.

syndromes are the XOR of the single error that indicates syndrome words representing the error locations. 110001 (+) 001011 = 111010 [31 (+) 0B = 3A HEX]. Since a double error is indicated—an even number of 1s in the syndrome word—the data and check bits are complemented and placed in the output registers for presentation to the memory. After the memory write and subsequent read, the new data are complemented and stored in the data input latch. The error in location 5 remains in the data. A new set of check bits is generated from the data in the data input latch and compared with that in the check bit input latch, producing the syndrome word 110001 (31 HEX), which corrects the remaining error.

A detected double-bit error followed by a double complement correct cycle is properly reported as to initial error type. If the detected errors were both soft, for example, no change would occur in the data or check bit, and the ECC device error flags would again report a double-bit error. If, after the second read and complement, the error flags still report a single-bit error, the hard error (of a hard and soft combination) has been corrected and only the soft error remains. Of course, the single remaining error will be corrected in the normal manner by the ECC device. In the case of a double hard error, the error flags will report a no-error condition following the second read cycle, indicating that both errors were corrected and that the data are valid.

This is the first of a 3-part series. The second part, "Simplification of 2-Bit Error Correction," will appear in next month's special report on memory system design.

New LM-4. The 40-Channel Logic Monitor you hold in your hand.

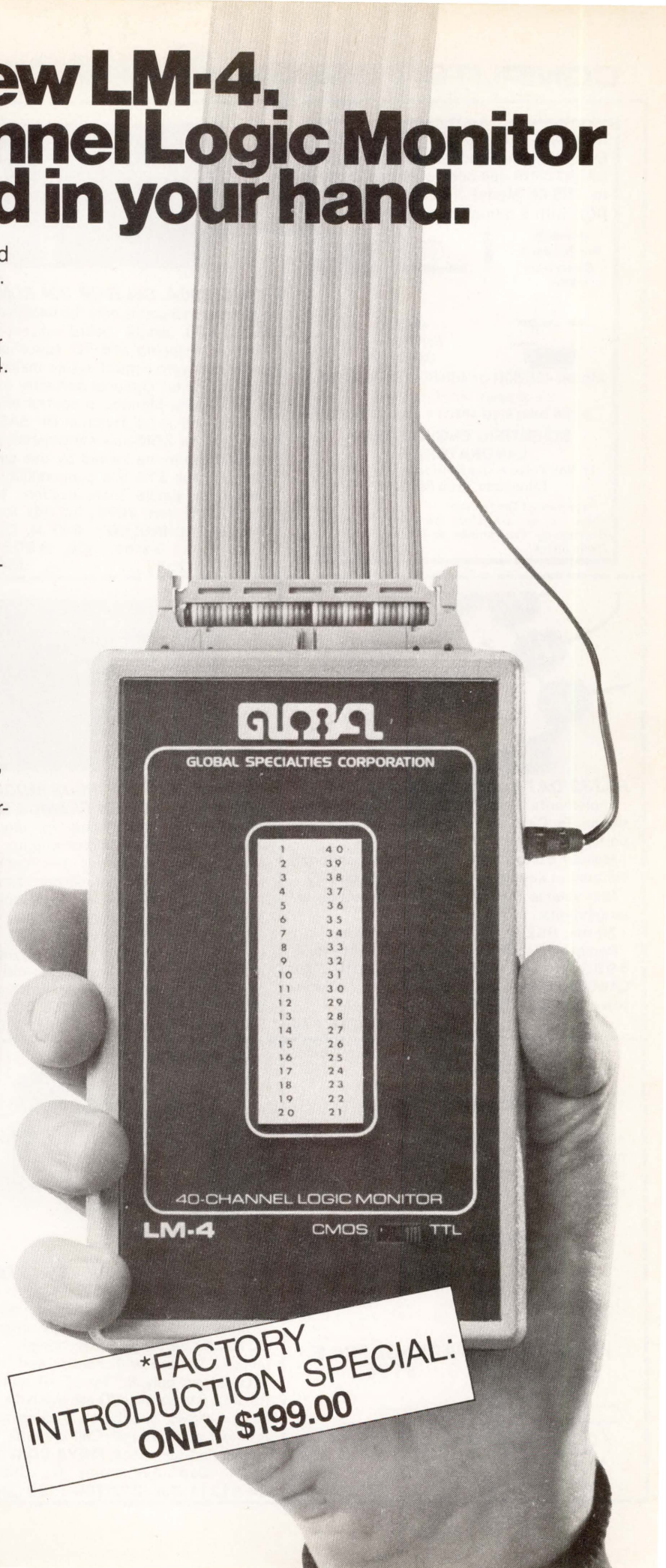
Now, there's a unique new way to speed and simplify your work with complex digital circuits. By simultaneously monitoring up to 40 points in a logic system with a compact, easy-to-use instrument that's faster than a scope and safer than a voltmeter. It's our new multi-family LM-4. At our factory introductory price of $199.00*, one of the best buys in logic today!

Simply slip its 40-pin IC test clip over your CMOS or TTL ROM, RAM, microprocessor or MSI/LSI chip and instantly see the logic state of each pin on a big, easy-to-read liquid crystal display.

But that's only the beginning. You can wire the LM-4 into a computer bus; fit it with two 16-pin test clips or sockets for comparing known good and questionable ICs; use it as a clip-on display for micros, minis and other computers during design, setup, testing, troubleshooting ...there's no limit to the ways LM-4 can save you time and money!

Measuring just 5.9 × 3.2 × 1.2″, the pocket-sized LM-4 comes with a 24″ 40-conductor ribbon cable terminated in a 40-pin IC test clip, plus instructions/applications manual and high-impact carrying case. (An optional Universal Cable Kit is also available for special interfacing requirements, priced at $75.00†)

So whatever the job—in design, production or service—simplify your testing with the power of 40-channel monitoring: Order your LM-4 today.



Call toll-free **1-800-243-6077**
8:30 AM–5 PM EST, Mon–Fri

GLOBAL SPECIALTIES CORPORATION

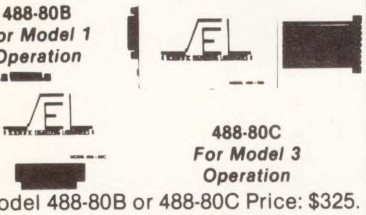
*FACTORY INTRODUCTION SPECIAL: **ONLY $199.00**

70 Fulton Terr., New Haven, CT 06509 (203) 624-3103, TWX 710-465-1227.
OTHER OFFICES: San Francisco (415) 648-0611, TWX 910-372-7992,
Europe: Phone Saffron-Walden 0799-21682, TLX 817477,
Canada: Len Finkler Ltd., Downsview, Ontario.

†U.S. Resale only; price, specifications subject to change without notice.

CIRCLE 107 ON INQUIRY CARD

IEEE-488 TO TRS-80* INTERFACE
Everything needed to add *powerful* BASIC GPIB-488 controller capability to TRS-80 Model 1 or 3, Level 2 or DOS with a minimum of 16K.

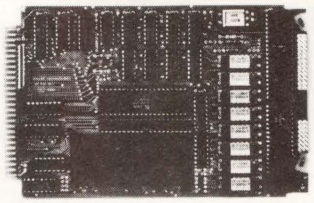


Model 488-80B or 488-80C Price: $325.
+ shipping, insurance & tax
WHEN ORDERING SPECIFY DISK OR TAPE

SCIENTIFIC ENGINEERING LABORATORIES
11 Neil Drive • Old Bethpage, NY 11804
Telephone: (516) 694-3205

**Trademark of Tandy Corp.*
There is no affiliation between Scientific Engineering Laboratories and Tandy Corp. or Radio Shack.

CIRCLE 475



4 MHZ Z80A, 64k RAM, 32k ROM, 32 I/O bits and serial port is only the beginning for the MCPU-800 single board microcomputer. Memory mapping and I/O space expansion under software control assure maximum system flexibility. Optional software includes a hard working Monitor, a control oriented 2k BASIC, and a full function 8k BASIC. Both Basics allow ROM-able statements. Many applications may be served by this card alone, although full STD bus compatibility is maintained for simple customization. 16k RAM MCPU-800 from $675, full 64k for $1175. **MILLER TECHNOLOGY**, 647 N. Santa Cruz Ave, Los Gatos, CA 95030. Tel: (408)395-2032. **CIRCLE 478**

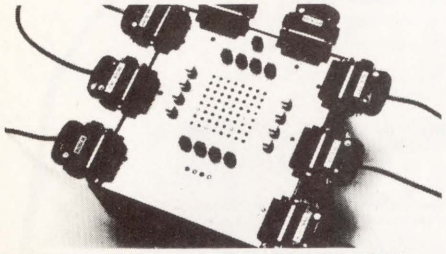
PRESENTING:

System Showcase

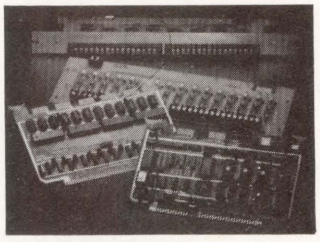
Your product could be represented here next month . . .

Call Maureen Sebastian
(617) 486-8944
Toll Free
(800) 225-0556

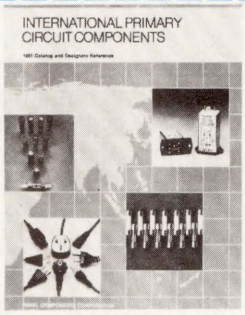
CIRCLE 481



RS232 DATA SWITCHING MATRIX
· Implements every possible connection between Tx Data and Rcvd Data for eight I/O ports.
· Manual Control and connection monitoring via built in key array and 8 x 8 LED display.
· Non-volatile memory for 16 connection arrangements.
· 20 ma, RS232, or TTL may be mixed.
· Remote selection via parallel TTL interface.
$995 (1-4, USA only), **DIGITAL LABORATORIES**,600 Pleasant St., Watertown, MA 02172. (617)924-1680.
CIRCLE 476



MICROBLOX™ EXORBUS MODULES FOR EASY SYSTEM FABRICATION
Modules have I/O pinouts for direct ribbon cable connections. Microcomputer has 6801 MCU, up to 13.1k of EPROM/ROM/RAM, 2 RS232C/20 ma ports, parallel port, timer, debug monitor. 80-line TTL I/O has 4 PIA's Industrial I/O has optical, relay isolation. Also available: 32-line I/O for interfacing Opto-22 mounting boards; 65k EPROM/ROM/RAM board; 4 port RS232C/20ma comm. module. EPROM programmer; card cages; support software. **MRC SYSTEMS**, 7320 Ashcroft, S-302 Houston, TX 77081. Tel: (713)771-7511 **Circle 479**



International Primary Circuit Components 1981 Catalog and Designers Reference — New 64-page catalog and design reference contains detailed descriptions of primary circuit components with international and North American product safety approvals. Fuses, fuseholders, primary circuit connectors, voltage selectors, RFI filters, and international cords and cordsets are covered. Each product section is preceeded with a description of applicable international standards and requirements. Suggested guidelines for specifying each component type are also included. **PANEL COMPONENTS CORP**, PO Box 6626, Santa Rosa, CA 95406. Tel: (707)523-0600.
Circle 482

Multi-Tasking Kernel

• Real-Time • Small (as little as 100 bytes) • Source Assembly • 8085, Z-80, 6502, 6800, & 6809 • Easy to Use • Fully Documented and Tested

Performance Statistics

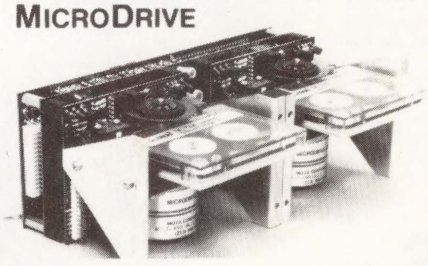
	8085	Z-80	6502	6800	6809	
Minimum Code Space	128	101	95	84	59	Bytes
Task Switch Time	179	197	129	133	85	usec.
Clock Frequency	2.0	1.0	1.0	1.0	1.0	MHz

To order write: **PACKAGE PRICE $195**

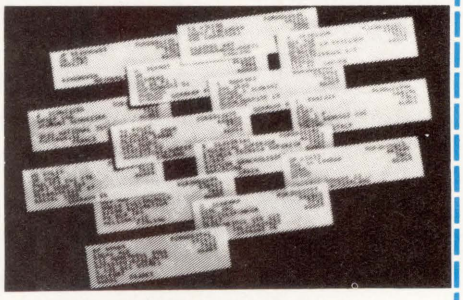
US Software
5470 N.W. Innisbrook Place
Portland, Oregon 97229 USA
(503) 645-5043

CIRCLE 477

MICRODRIVE



MicroDrive (TM)
TAPE CARTRIDGE DRIVE SYSTEMS DESIGNED FOR OEM'S
Rugged, all metal, patented main plate assures precise head to tape interface for DC100A cartridge interchange. Compact units (2 Drives) with control and formatting circuits use only 8" by 3" of panel space. RS-232 and parallel I/O are available. Modular design allows distributed packaging in tight terminal applications. Call or write for OEM pricing and full specs. **MOYA CORPORATION** 9001 Oso Ave, Unit B, Chatsworth, CA.91311. Tel: (213)700-1200 **CIRCLE 480**



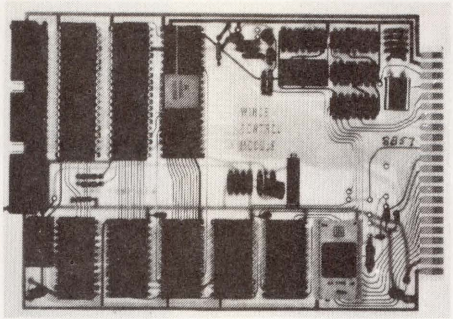
MATRIXED DIRECT MAIL LIST
The most Precise, most Versatile, Cross-Matrixed list of Computer Based Systems Designers ever offered for bulk or custom selection. You can rent the entire list, or pinpoint the exact engineers you want to reach. NEW 48-HOUR EXPRESS PROCESSING.
For details, contact Maureen Sebastian at **COMPUTER DESIGN**, 11 Goldsmith St., Littleton, MA 01460. Tel: (800)225-0556 In Mass: (617)486-8944 **CIRCLE 483**

GRAY SCALE PRINTER

Remarkable gray scale resolution! Great detail! The CEC® 912 Gray Scale Printer offers 16 true gray scale steps. 200 picture elements per inch, hor. & vert. (or 40,000 per sq. in.)! High speed printouts on inexpensive paper. Archival quality. Unaffected by ambient conditions. Call Cliff Haber, (213) 796-9381 Ext. 2575.

BELL & HOWELL CEC DIV. 360 Sierra Madre Villa, Pasadena, CA 91109.

CIRCLE 484



$73.80* SINGLE BOARD COMPUTER

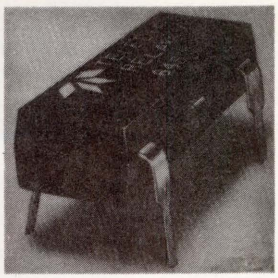
6800 MPU, serial I/O, parallel I/O, RAM, EROM, 44-pin 4½" x 6½" PCB.

EXPANSION MODULES

RAM, ROM, CMOS RAM/battery, analog I/O, serial I/O, parallel I/O, counter/timer, 488 GPIB, EROM programmer, power fail detect/power on reset. *100 piece price, model MCL11.

WINTEK CORP., 1801 South Street, Lafayette, IN 47904; 317-742-8428.

CIRCLE 487

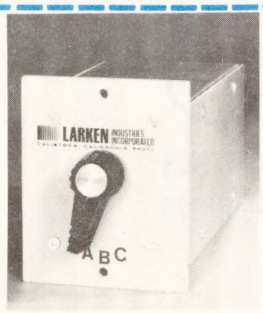


LOW EMI AC DIP RELAY

Teledyne's 645 meets FCC and VDE stds. Features 3.8 to 32V input and TTL logic compatibility, up to 1 amp switching at 250VRMS, back to back SCR output, low leakage current of 1mA RMS, 2500VRMS optical isolation, low insertion factor of ±1.5V, high noise immunity, and virtually no switching transients. $6.35 ea for 5000 pcs.

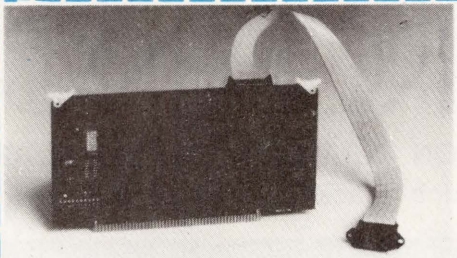
TELEDYNE RELAYS SS DIV, 12525 Daphne Ave, Hawthorne, CA 90250. Tel: (213) 777-0077.

Circle 490



LARKEN EIA RS-232 SWITCHES

The LARKEN RS-232 Switches provide instant switching of the EIA RS-232 interface circuits. All 24 active leads of the interface are switched, and the ground pin is hardwired through. These switches allow data circuit reconfiguration to meet normal operational requirements or to bypass failed equipments and circuits. Six switches can be mounted on 19" rack mountable rails. **LARKEN INDUSTRIES INC.**, PO Box 465, Calistoga, CA 94515. Tel: (707)942-5404. **Circle 485**

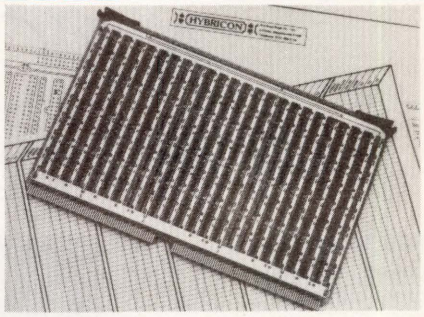


S-100 TO IEEE-488 INTERFACE

THE P&T-488 INTERFACE BOARD lets your S-100 computer be a talker, listener, or controller on the IEEE-488 instrumentation bus. Software packages allowing high level language access to the 488 bus are available for CP/M, CDOS, North Star DOS/BASIC, as well as for direct assembly language programming. Price of the P&T-488, assembled and tested with one of the software packages, is $450.

PICKLES & TROUT, Box 1206, Goleta, CA 93116 (805) 967-9563.

CIRCLE 488



VERSABUS™ COMPATIBLE PACKAGING

The 4-68000-VHF series are available fully or custom pinned, using Socket-Sert™. Unique VHF configuration, with continuous ground plane has been independently listed at clock rates up to 250 MHz. Hybricon manufactures card frames, multilayer backplanes and controlled impedance extender cards for Versabus™ and general purpose applications.

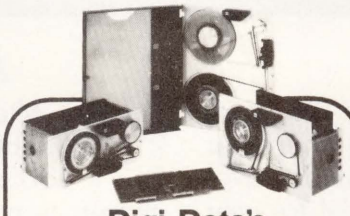
HYBRICON CORPORATION, 410 Great Road, Littleton, MA 01460. Tel: (617) 486-3174.

Circle 491

LOW COST POSTCARD MAILINGS

Here's a way for your company to test new product acceptance, offer catalogs, find new applications, or support ongoing product lines. Computer Design's POSTAL MAILERS go to our 70,000 domestic subscribers 4 times each year. Rates start at $895 per card and go down with frequency. Next closing December 21, 1981.

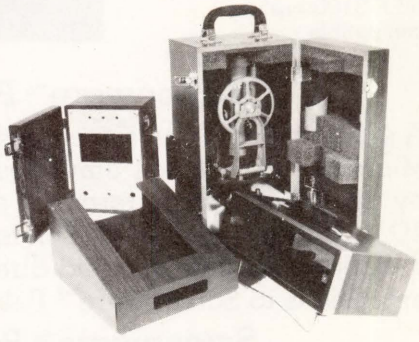
Contact Maureen Sebastian, **COMPUTER DESIGN**, 11 Goldsmith St. Littleton, MA 01460. (617)486-8944. **CIRCLE 486**



Digi-Data's reel-to-reel tape drives are compatible with DEC, DG and HP minicomputers... at up to 50% less cost.

CONTACT: DIGI-DATA CORPORATION
8580 Dorsey Run Rd.
Jessup, MD 20794
(301) 498-0200

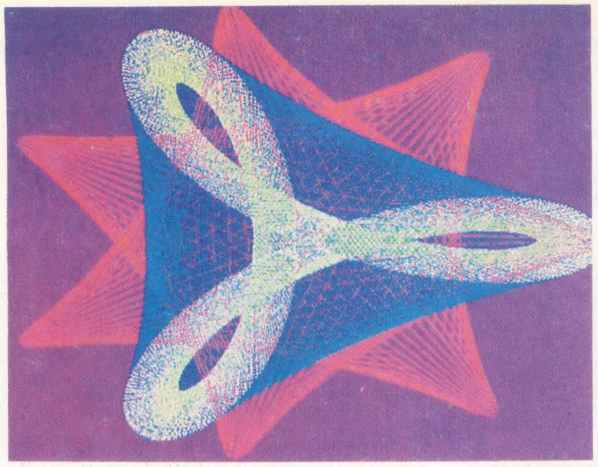
CIRCLE 489

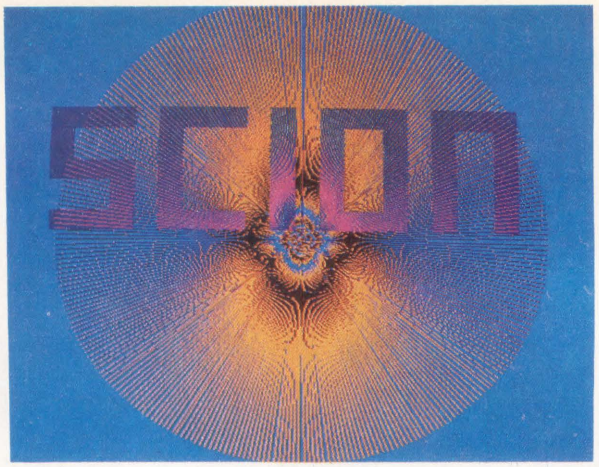


CASES • CABINETS • ENCLOSURES IN STOCK AND CUSTOM BUILT

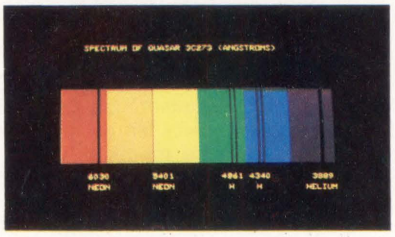
Formica® laminated construction for strength and durability. Stock line comprises more than 800 SIZES ranging up to 12¼" x 19" x 16". We custom-build, in any quantity, to meet exact requirements. **W.A. MILLER CO, INC**, 275 Mingo Loop, Oquossoc, MAINE 04964. Tel: (207)864-3344

Circle 492





"...stands well above other S-100 graphics displays in its price and performance range."
BYTE, Product Review



"...better monochromatic ...display...."
ELECTRONIC DESIGN, 1981 Technology Forecast

MICROANGELO

HIGH RESOLUTION GRAPHICS SINGLE BOARD COMPUTER

512 x 480 resolution black and white **and** vivid color displays

RS-170 composite or direct drive output

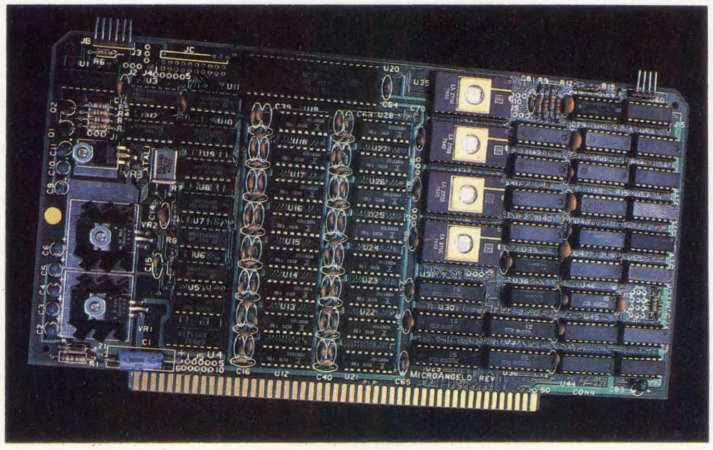
Local or external sync generation

4 Mhz Z80 microprocessor

60 hertz real-time clock

8 level interrupt tie-in

IEEE S100 bus compatible



Light pen interface

Time multiplexed refresh

4K resident Screenware™ Pak I operating system

32K RAM isolated from host address space

High speed communications over parallel bus ports

Screenware™ Pak I

A 4K byte operating system resident in PROM on MicroAngelo™. Pak I emulates an 85 character by 40 line graphics terminal and provides over 40 graphics commands. Provisions exist for user defined character sets and directly callable user extensions to Screenware™ Pak I.

Screenware™ Pak II

An optional software superset of Pak I which adds circle generation, polygon flood, programmable split screen for separate graphics and terminal I/O, relative coordinates, faster vector and character plotting, a macro facility, full UCSD Pascal compatibility, and more.

And now...COLOR!!

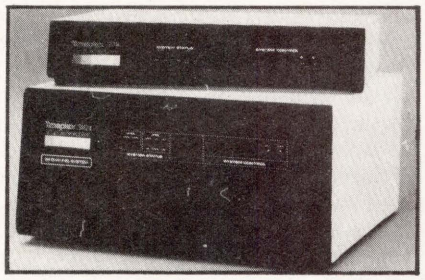
The new MicroAngelo™ Palette board treats from 2 to 8 MicroAngelos as "bit planes" at a full 512 x 480 resolution. Up to 256 colors may be chosen from 16.8 million through the programmable color lookup table. Overlays, bit plane precedence, fade-in, fade-out, gray levels, blinking bit plane, and a highly visual color editor are standard.

SCION

12310 Pinecrest Road • Reston, VA 22091 • (703) 476-6100 • TWX: 710-833-0684

CIRCLE 108 ON INQUIRY CARD

Statistical multiplexer/data concentrators support networks with up to 144 ports



SM8, SM24, and SM48 members of Switching Microplexer family support 8, 24, and 48 ports, respectively. Units can be mixed in any combination to form 1-, 2-, or 3-node networks with up to 144 ports. Designed for distributed data switching, the family provides flexibility in network configuration, including local and remote port contention and data PABX. Each port is user programmable to be either dedicated or switched. Virtually any combination of dedicated and switched ports is possible within a network.

Switched ports operate in either port contention or port selection mode. In the contention mode, ports can be partitioned into contention groups and any local or remote port can be programmed to contend for a group. The system automatically attempts to connect a calling port to its preselected contention group, starting with the lowest numbered channel in that group. If a connection cannot be made at that time, the system sends a message to the requesting terminal and continues trying at 10-s intervals. The port selection mode allows a port to automatically or manually call another port or contention group through an interactive sequence.

Dedicated connections between ports can be set up using the "electronic patch panel" feature, accessed via the supervisory port. Std synchronous protocols such as bisynchronous and SDLC are supported using dedicated connections. Single quantity prices for the multiplexer/data concentrators start at $2800. **Timeplex, Inc,** One Communications Plaza, Rochelle Park, NJ 07662.

Circle 280 on Inquiry Card

Modem integrates voice and data output

ADAS VIII voice/data modem enables any computer to place or receive telephone calls, bidirectionally transfer data at 300 baud, "speak" in unlimited vocabulary of synthesized voice, and receive Touch-Tone™ information from distant telephones for control or data retrieval. When interfaced to a host computer, the modem can perform std originate/answer modem functions. Connected by a self-contained FCC approved telephone coupler circuit to a std telephone line, the device can also deliver any vocal message, via telephone, to any telephone in the world.

An RS-232 interface connects the interactive system to the host computer; instructions to the modem, status indications, and modem data can be communicated through this link. Once programmed by the host computer, the modem can be commanded to place or receive telephone calls, either in a voice or data mode. Calls can be local, long distance, or PBX-originated. In the voice mode, the device produces unlimited, continuous speech, synthesized immediately from a phoneme library.

The system can be called from any telephone by dialing its designated telephone number; the modem notifies the host computer to answer the incoming call. When online with a distant telephone, the device will respond to Touch-Tone commands from a long distance caller, or signals from a distant modem.

A fail-safe feature instantly provides a backup system in the event of power failure. If 110-V power flow is lost for more than 15 s, the modem automatically goes into an alarm mode, reporting the problem to a preprogrammed telephone number so that immediate repairs can be made. **Butler National Corp,** 8246 Nieman Rd, Lenexa, KS 66214.

Circle 281 on Inquiry Card

Multiplexer allows simultaneous connection of synchronous and asynchronous lines

CS11/V multiplexer connects up to 32 synchronous and asynchronous line devices to a single controller board housed within the CPU backplane of DEC PDP-11 computers. Additional lines can be connected by adding another controller card to the CPU and line adapter cards to external distribution panels. The multiplexer includes all of the capabilities of the DEC DV11 system, plus higher line handling speeds and better throughput, in a smaller package.

Synchronous and asynchronous line interfaces can be mixed in sets of 8 lines, each operating either synchronously or asynchronously. The multiplexer uses a single hex-size circuit board for a CC11/V communications controller, connected by a 34-conductor ribbon cable to one or two 16-line CP11/V distribution panels. Each panel contains an integral power supply and one or two CA11/V line adapters. Adapters include data and modem interface circuitry plus UART type circuits that supply serial to parallel and parallel to serial conversions. The UARTs also contain a baud rate generator that provides all commonly used data rates, plus 19,200 baud, for a total composite data rate of up to 50,000 chars/s on a single controller.

The multiplexer is software transparent to the DH11 and executes std DECZJ192 diagnostics kits. It is supported under the DECNET-IAS and DECNET-RSX operating systems. A basic configuration, including 1 controller and 1 distribution panel with an adapter for 8 communications lines, is priced at $4925. **Emulex Corp,** 2001 E Deere Ave, Santa Ana, CA 92705.

Circle 282 on Inquiry Card

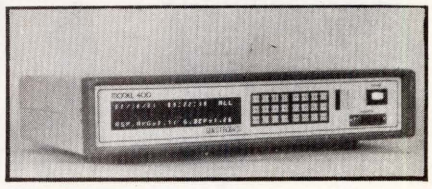
Communication control unit

Model 6270 allows ASCII CRTs to access IBM host systems using 3270 binary synchronous communications protocol. Compatible with IBM 3271/74/76 control units, attached 3277/78 display stations, and 3284/86 printers, the device runs with existing IBM 3270 applications without modifications. Unit can be configured with up to 16 access ports. Up to 2 ports can be defined for synchronous communication, with the remaining access ports available for asynchronous device attachment. **Carterfone Communications Corp,** 111 W Mockingbird Ln, Suite 1400, Dallas, TX 75247.

Circle 283 on Inquiry Card

Data communications monitor

Model 400 evaluates and prints reports dealing with data communications links and terminal response time; these data are provided on the front panel alphanumeric display or in a complete formatted report that can be routed to any std line printer. Device operates in 4 basic modes: the ALL STATIONS mode captures all transactions on the line, the CLUSTER mode examines all devices attached to a cluster, the DEVICE mode examines one particular device on the cluster, and the TRANSACTION BY ID mode keeps track of the number of transactions by ID characters. **Questronics, Inc,** 3565 SW Temple, Salt Lake City, Utah 84115.



Circle 284 on Inquiry Card

Communications Multiplexer

Model 6732 enables a locally attached IBM 3274 controller to conduct half-duplex communications with up to 32 remote 3278 or 3279 CRT terminals and 3287 printers on a single channel of a Videodata broadband coaxial cable network. The unit interfaces directly with the IBM 3274 terminal controller, multiplexing the 32 separate data signals into a single data stream for transmission over the cable. Multiplexer, including power supply, mounts in a std 19″ (48-cm) equipment rack and operates at 2.36M bits/s. **Interactive Systems/3M,** PO Box 33600, St Paul, MN 55133. Circle 285 on Inquiry Card

Position switching and port sharing units

Units allow several computers to share a common device or one computer to use several devices on one CPU port. GRS 232-S8AD has 4 positions and connects 4 devices to a common I/O device; GRS 232-S8AE has 5 positions and connects 5 devices to a common I/O device; and GRS 232-S8AF has 6 positions and connects 6 devices to a common I/O device. All 3 units also switch the basic 8 lines of the RS-232 interface. Options include monitoring and a rackmountable enclosure. **Giltronix, Inc,** 450 San Antonio Ave, Palo Alto, CA 94306.
Circle 286 on Inquiry Card

Rackmount integral auto dial modem

212 PLUS (model MD212-4) incorporates the auto dialer features of the 212 PLUS standalone unit in a 6 x 14″ (15- x 36-cm) rackmount card that occupies a single slot in the company's std 19″ (48-cm) rack enclosure. Integral auto dialer offers microprocessor controlled dialing from either computer or terminal equipment; no telephone is required. The FCC approved device is functionally compatible with Bell std 212A modems at both 1200 and 300 bits/s, both originate and auto answer. Features include instant redialing, dial forever commands that permit automatic redialing of a number until a connection is completed, and network addressing capability. **Ven-Tel, Inc,** 2390 Walsh Ave, Santa Clara, CA 95051. Circle 287 on Inquiry Card

X.25 network interface multiplexer

Machine independent PIN 9102 provides access to the X.25 packet switched networks for computer systems with asynchronous ports. Interactive terminals connected anywhere on the network communicate with the host computers(s) via logic channels that are demultiplexed by the unit. Device can be configured as an 8-channel standalone version or in increments up to 16 channels/rackmount configuration. On the synchronous link, it operates at speeds up to 19.2k bits/s. Channel related features include user selectable DCE/DTE interface and 5- to 8-level codes accepted with 1, 1.5, and 2 stop bits (even, odd, or no parity). Multiplexer is certified for TELENET (USA), PSS (U.K.), and DATAPAC (Canada) networks. **Gandalf Data Inc,** 1019 S Noel, Wheeling, IL 60090.
Circle 288 on Inquiry Card

Local network for small terminal systems

Data Loop Exchange (DLX) 10 ties data terminals, word processing workstations, personal computers, or a mix of these devices into a local area network for interconnection or communication with a common computer. Twisted pair loop wiring eases installation and eliminates the expense of modems and telephone lines. System gives up to 10 terminals within a 0.5-mi (0.8-km) radius access to 3 computer ports. It is capable of an asynchronous aggregate rate of 153,600 bits/s and a synchronous rate of 614,000 bits/s. Station data rate for asynchronous communication is up to 9600 bits/s and up to 19,200 bits/s for synchronous communication. **Electrosound Systems, Inc,** Phoenix Business Pk, 2917 N 35th Ave, Phoenix, AZ 85017. Circle 289 on Inquiry Card

Intelligent interface provides synchronous communications link

Microprocessor based, standalone INTERCON 100 links DEC VAX computers, PDP-11s with RSX-11M, and microcomputers running CP/M, Control Data Corp host mainframes; and IBM host mainframes via either dedicated or dial-up lines. It provides data rates up to 9600 bits/s, self-contained protocols, asynchronous/synchronous data conversion, and self-test capability. The unit is based on an Intel 8085A processor, with communications controlled by four 8251A USARTS, that operates under a P/ROM based monitor and controls all protocol functions, code conversion, and modem management. Power-up automatically

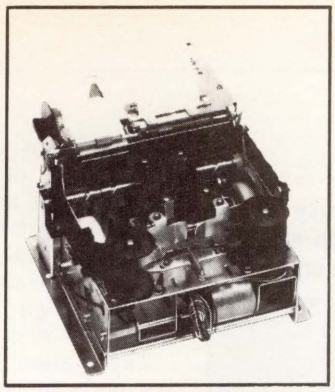
(continued on page 198)

WESTREX

DOT MATRIX PRINTERS

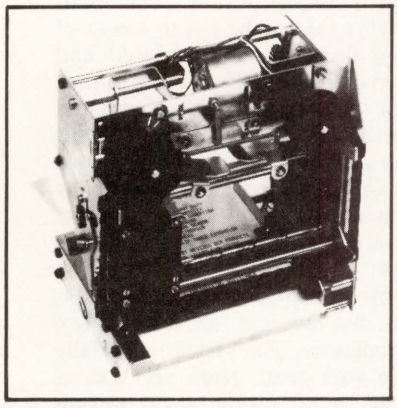
800 SERIES

INTRODUCING OUR NEW FAMILY OF COMPACTS



MODEL 820
SPLIT PLATEN PRINTER

- Various Platen Splits
- Five Line Validation
- Paper-Supply and Take Up
- Logo Printing
- Automatic Receipt Cutter

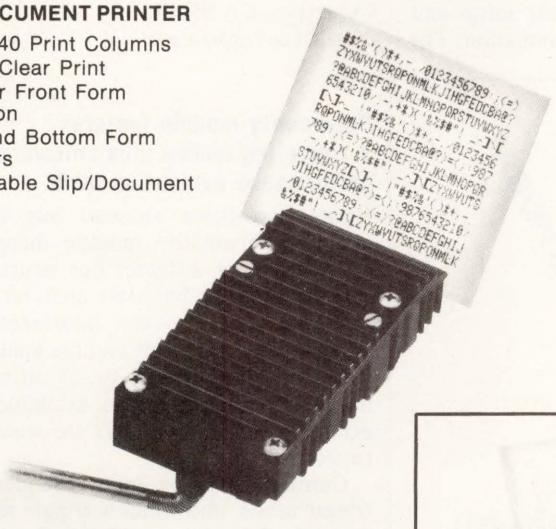


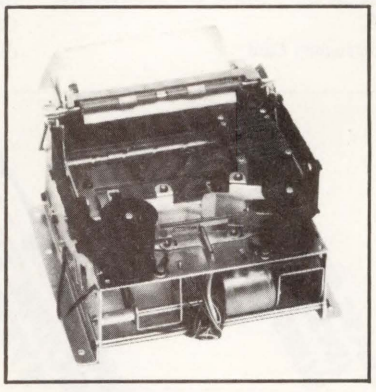
WESTREX 800 Series of alphanumeric bi-directional printers include split platen printers, flat bed slip/document printers and 51 to 96 column journal printers in a variety of standard models to suit a wide spectrum of OEM applications. All WESTREX 800 Series printers utilize the same simple, reliable drive system, head position sensors, ribbon transport mechanism and other quality tested components for maximum cost effectiveness.

Basic models illustrated on this page are obtainable with various options to suit your application needs. Data sheets with technical specifications for each of these products are available upon request.

MODEL 840
SLIP/DOCUMENT PRINTER

- Up to 40 Print Columns
- Large Clear Print
- Side or Front Form Insertion
- Top and Bottom Form Sensors
- Adjustable Slip/Document Stop





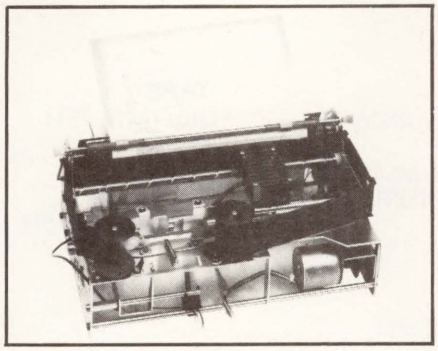
MODEL 850
JOURNAL PRINTER

- 51 Print Columns
- Integral Paper Supply Holder
- Easy Top Paper Insertion
- Document Validation Capability

AT THE HEAD, THEY'RE CLASS!

MODEL 801
LOW PROFILE, LOW WEIGHT, PRINT HEAD

- 7 Needle Vertical Array
- Low Power Consumption
- 100% Duty Cycle
- 100 Million Character Life



MODEL 880
JOURNAL PRINTER

- Up to 96 Characters Per Line @ 12 CPI
- Bi-Directional Printing
- Standard & Graphic Feed
- 576 Print Dots Per Line

For full details, write or call us

Litton **WESTREX OEM PRODUCTS**

1140 Bloomfield, West Caldwell, N.J. 07006 (201) 227-7290
IN FRANCE — WESTREX OEM PRODUCTS, 103-107 Rue de Tocqueville, 75017, Paris, France 01-766-32-70
IN SWEDEN — WESTREX OEM PRODUCTS, Box 3503, S-17203 Sundbyberg, Sweden 46/8+981100

CIRCLE 111 ON INQUIRY CARD

boots the system from P/ROM and sets up communications to the mini- or microcomputer.

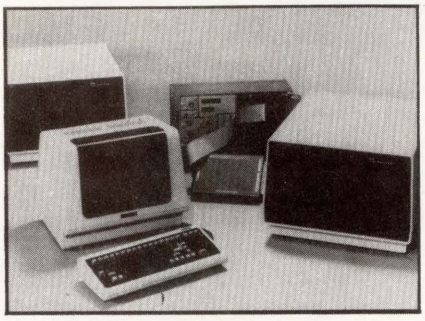
The interface has capacity for up to 4 switch-selectable 2716 P/ROM resident protocols: Control Data 200UT, IBM 3780, IBM 2780, and modified IBM 2780. A front panel switch allows protocol selection. With CDC 200UT protocol, the interface allows communications with CDC mainframes running either Scope-Intercom, NOS, or NOS-BE. Communication can be in either ASCII or BCD with appropriate code conversion made in the interface. With 3780 or 2780 protocol, the user can communicate with a variety of mainframes, terminals, or emulators using either ASCII or EBCDIC.

A lighted pushbutton reset switch and a lighted nonmaskable interrupt switch that doubles as a hard error indicator are mounted on the front panel. The rear panel contains power cord, 2-A fuse holder, and four 25-pin DB25 RS-232-C connectors. Price for the interface with 1 protocol is $3995; additional protocols are $1000 each. **Intercon Research Corp,** 2603 Artie St SW, Suite 14, Huntsville, AL 35805.

Circle 290 on Inquiry Card

DEVELOPMENT SYSTEMS

Integration and debug station provides realtime emulation of 8- and 16-bit microprocessors



Modular 9516 microsystem integration station offers realtime in-circuit emulation, software and hardware analysis, and softkey and menu-driven human interface to ease debugging of microprocessor based systems. System features totally transparent realtime operation implemented in a dual bus structure for realtime control and monitoring. Dual bus allows access to the logic trace analyzer for setup and display without stopping emulation. The emulator runs continuously, avoiding user refresh or DMA problems. The system's 24-bit address, 16 bits of status, and 25-bit externals have an expansion capability for 32 bits of address and 32 bits of data to support future 32-bit processors. High speed static memory operates at 90 ns.

The station supports 2 emulator systems in the same enclosure or with an add-on enclosure. Each in-circuit emulator is coupled with 4 global event lines linking the emulators, to a max of 4. Trace displays are correlated and presented on a line by line basis and each emulator requires only a debug card and the slave emulator. Current 8-bit emulators are supported via a universal adapter card that translates the system's bus structure into the bus structure of the company's 9508 microsystem emulator.

Support is provided for 8085A, Z80A, 8021, 8041, 8048, 8049, 8050, 6801, 6803, and 6809 microprocessors. The system is initially available with Z8001, Z8002, and 8086 in min and max mode. **Millennium Systems, Inc,** 19050 Pruneridge Ave, Cupertino, CA 95014.

Circle 291 on Inquiry Card

Personality module features 3 triggering modes plus software performance evaluation mode

M68BSA1 realtime MC68000 bus state analyzer personality module increases the number of different bus structures that the realtime bus state analyzer can monitor. The module interfaces to selected MC68000 signals and the analyzer stores data that appear on 63 different lines. Six of these lines are available for external connection and 57 are prewired to MC68000 lines.

Continuous trace mode, sequential trigger mode, and window trigger mode facilitate the gathering of data from the MC68000. In the continuous mode, the analyzer continually stores information until a fault is encountered or the system is halted. At this point, the analyzer's 63- x 128-line memory contains the MC68000 activity for the past 128 transactions. In the sequential triggering mode, a series of events are specified in sequence. Once the events occur in the specified order, the analyzer can start or stop storing data. Lastly, window triggering allows the designer to detect unplanned branches into or out of a specified range of memory addresses in which normal program execution would occur.

Software evaluation is provided through the analyzer's capability to

(continued on page 200)

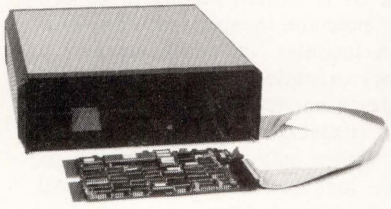
When You Need . . .

WINCHESTER DISK SYSTEMS

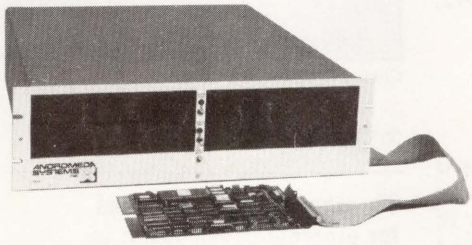
FOR THE Q-BUS

ADD-ON SUBSYSTEMS

MWDS

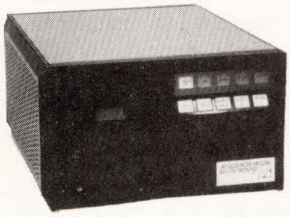


WDS



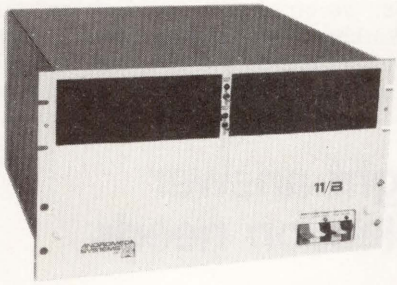
RPX60

5-1/4″ DISKS



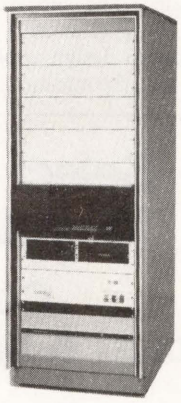
11/M-W

8″ DISKS



11/B-W

14″ DISKS



11/B-WTS

FULL TURNKEY COMPUTER SYSTEMS

. . . think of Andromeda

Andromeda Systems, Inc. offers the Q-Bus user a wide selection of Winchester disk based mass storage systems. Both add-on subsystems and full turnkey computer systems are available. Current storage capacities range from 2.5mb to 160mb. The Winchester disk controllers emulate DEC RK-05, RL-01/02, and RP-02/03 devices for compatibility with existing operating systems. Winchester disks in 5¼″, 8″ and 14″ formats are used to obtain the best possible performance in a variety of package sizes.

Back-up is to floppy disk or streaming magnetic tape. The 5¼″ and 8″ systems may be specified with an intregral floppy disk drive; these systems use the Andromeda WDC11 controller that includes an RX-02 emulating floppy disk controller on the same dual-width card. Also available for backup is a separate, high performance, non-emulating floppy disk controller, the DFDC11/DMDC11. This proprietary controller offers 25 to 61 percent more storage along with a data transfer rate 2.25 times faster than the RX-02.

We offer a complete line of Q-Bus based systems and other LSI-11 related products. For details, contact:

ANDROMEDA SYSTEMS INC.

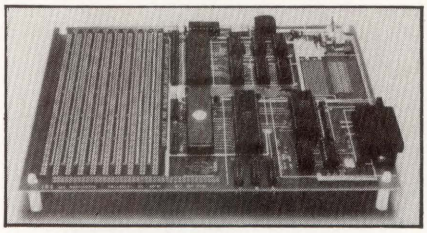
9000 Eton Ave.
Canoga Park, Calif. 91304
Phone: 213/709-7600
TWX: (910) 494-1248

monitor the relative frequency of memory accesses within an operator specified memory address range. This data can then be displayed in a histogram format, allowing a visual representation of those addresses occupying the program's time. The EXORterm™ 155 display console is used by the operator to communicate with the analyzer, with menu-type manipulation of the system parameters. Personality module, including cabling, chip probe, and documentation, is priced at $1500 in quantities of 1 to 5. (A control module is required as well.) **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.

Circle 292 on Inquiry Card

Programming/design subsystem

Based on a 5-MHz Intel 8088, IDC-8 is fully assembled and tested, and includes monitor software in an 8755 I/O ROM, 1k of static RAM, 256 bytes of I/O RAM, and an 8251 based CRT interface. The I/O ROM and I/O RAM have a total of 38 parallel I/O lines. The subsystem also contains over 18 in² (116 cm²) of wirewrap area for special design applications, card expansions, the addition of peripheral support circuitry, and the addition of CPU memory. It requires 5 V at 1 A and communicates to the user via an RS-232 terminal. Software developed on the subsystem is compatible with other 8088 based computers, including IBM's personal computer. Single-unit price is $399. **Intelligent Devices Corp,** One Cameron Pl, Wellesley, MA 02181.



Circle 293 on Inquiry Card

SOFTWARE

Timesharing OS is designed for program development in multi-user environments

A std version of the UNIX™ timesharing OS, seventh edition, Edition VII Workbench provides up to 128 users with a basic OS (I/O, file, and terminal handling), high level computer languages, text processing, electronic mail, graphics capabilities, and computer aided instruction. It also includes the Source Code Control System facilities of PWB/UNIX, an integrated set of commands designed to aid software development and control changes to source code and text files. This system provides facilities for storing, updating, and retrieving all versions of source code modules or documentations. Built-in program management facilities allow software developers to recreate previous program versions and to maintain and manage current versions.

The OS is written mainly in C, providing machine independent control of system facilities, including memory to memory operations. The language also includes a variety of data types and a macro processor for parameterized code. Other languages offered by the system include FORTRAN '77, Pascal, YACC, RATFOR, and CAL.

Compatible with C and supporting utilities at the object code level, the system's ANSI std FORTRAN '77 compiler includes optional subscript range checking and detection of uninitialized variables, and handles all arithmetic widths. For documentation requirements, the system offers full preparation and formatting software. Electronic mail is provided between terminal users. A large library of application software packages developed under UNIX is also available.

Available for the company's family of 32-bit MEGAMINI® computers, the OS is priced at $30,000, including documentation and 90-day warranty. **Perkin-Elmer Corp, Data Systems Group,** 2 Crescent Pl, Oceanport, NJ 07757.

Circle 294 on Inquiry Card

Software package allows formation of communications network

NETCOMM™ software package permits a Troubleshooter 800™ in-circuit test system to function as a terminal with virtually any mainframe computer. The package can link the test system to a CPU via an RS-232-C serial port. In this mode, the test system emulates a terminal and can function as an I/O device. Test programs, datalog data, and input lists can be uploaded and downloaded to the host computer from the test system, with no disruption of production testing.

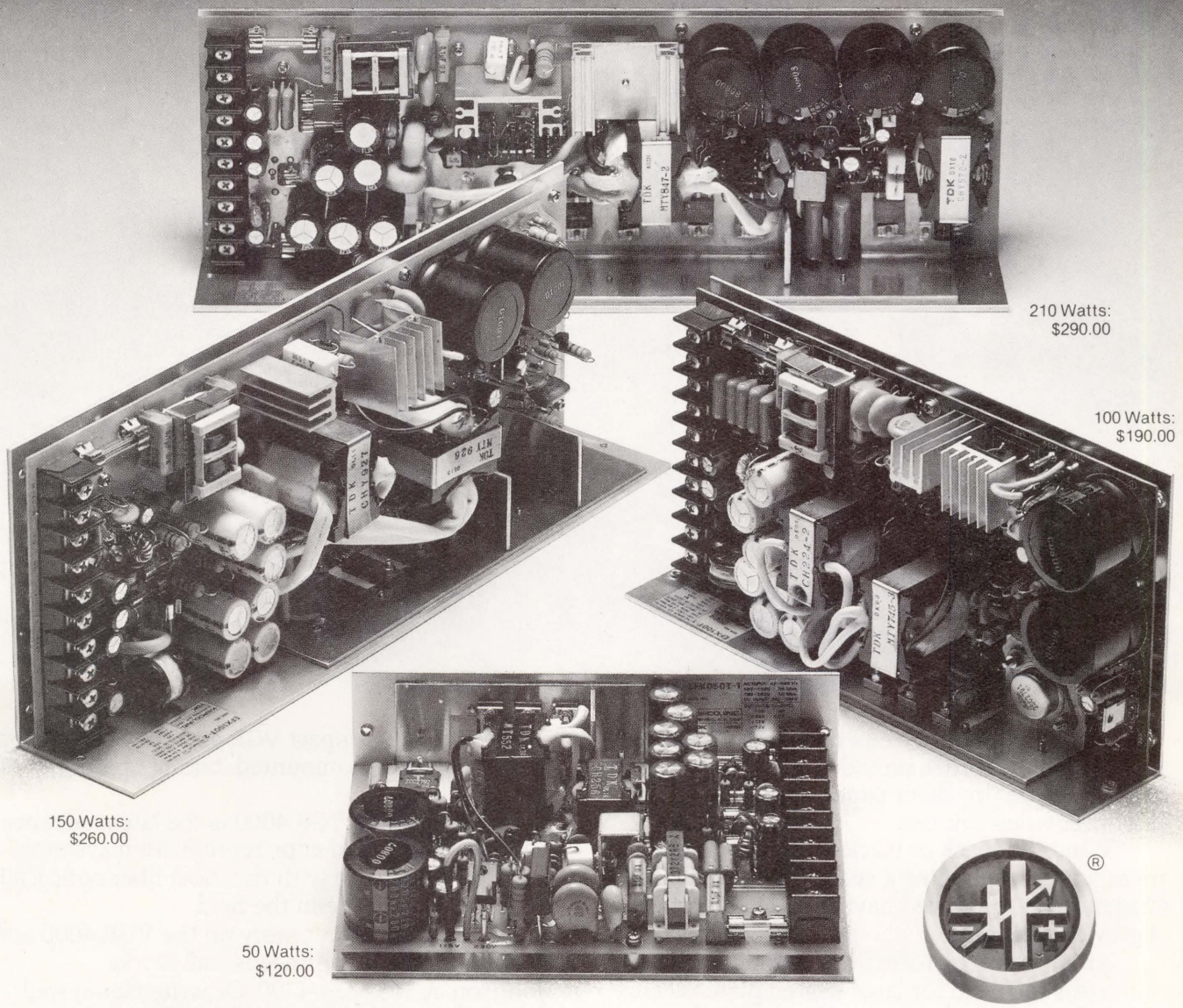
With the company's model 110 development station serving as the host CPU, the software enhancement can be used to form a communications network between the model 110, the Troubleshooter 800, and the Troubleshooter 900, without interfering with test functions.

(continued on page 206)

HIGH QUALITY

open frame SWITCHING POWER SUPPLIES

... at a very attractive price



210 Watts:
$290.00

100 Watts:
$190.00

150 Watts:
$260.00

50 Watts:
$120.00

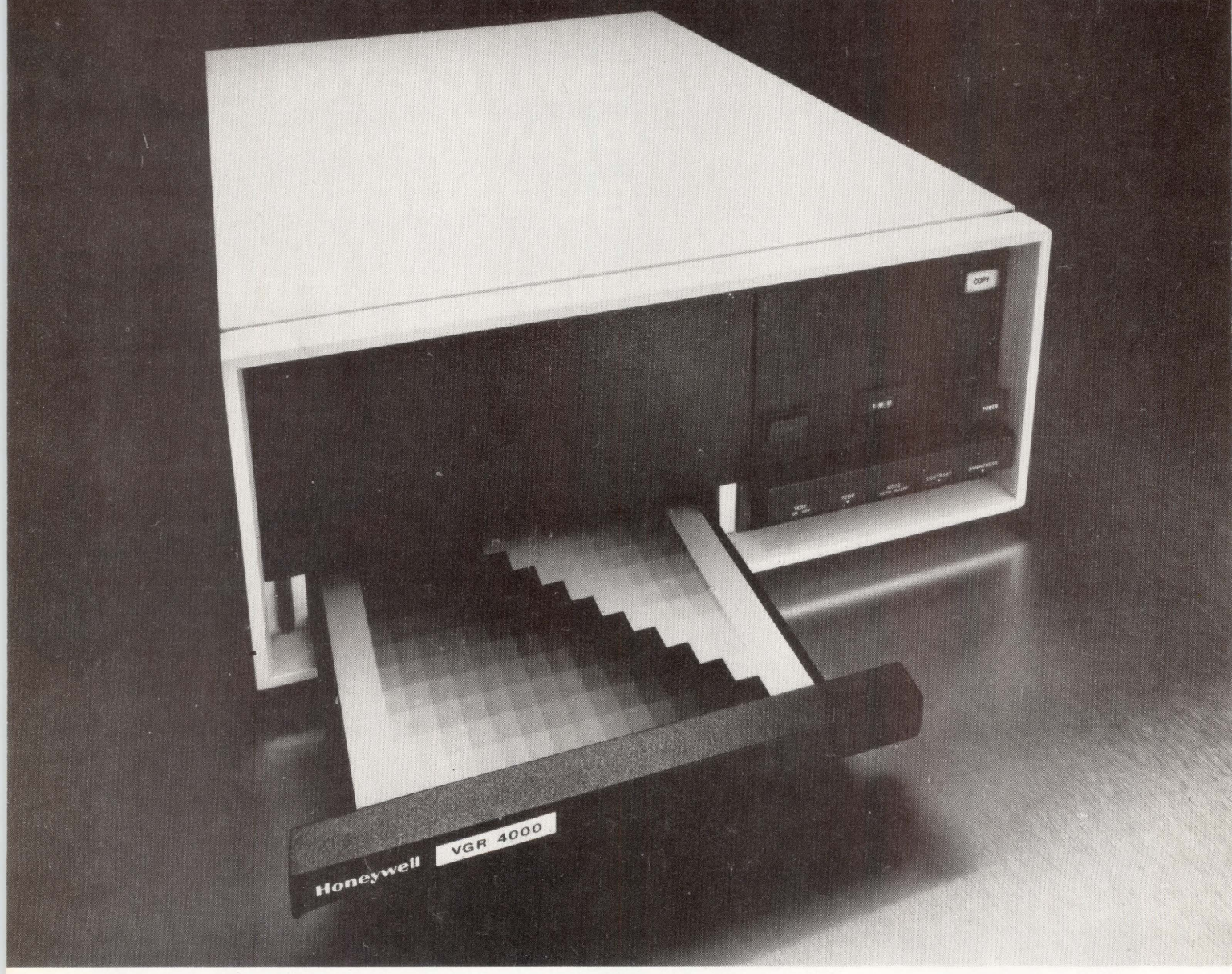
Single board, multiple-output, open frame switch-mode power supplies offer you high efficiency, well regulated power at a very attractive price.
The listed prices are for single unit quantities. Please contact us for quantity pricing and a demonstration.

KEPCO® For complete specifications, write Dept. DBF-79

KEPCO, INC. • 131-38 SANFORD AVENUE • FLUSHING, N.Y., 11352 U.S.A • (212) 461-7000 • TWX -710-582-2631 • CABLE: KEPCOPOWER NEWYORK

CIRCLE 115 ON INQUIRY CARD

THE LATEST ADVANCE IN VIDEO GRAPHIC HARD COPY RECORDING FROM HONEYWELL



VGR 4000, Honeywell's new and advanced video graphic recorder, provides fast, crisp, 8½ x 11" hard copies on dry silver paper from most CRT's and other video sources.

White-on-black or black-on-white images are as simple as flipping a switch. With options, images can be produced having up to 16 shades of grey or even more.

An innovative processing technique eliminates the need for large heated platens. This allows the recorder to run cool, consuming very little energy.

The VGR 4000 is the only recorder on the market available with a self-contained test-pattern generator providing a choice of formats for proper copy verification.

Rugged, yet cleanly designed for easy operation, the compact VGR 4000 can be used on a desk top or rack-mounted, taking up only 7" of front panel space.

Honeywell's VGR 4000 is the latest advance in video-input hard-copy reproduction systems, built by the people with the most fiber-optic CRT recorder experience in the field.

To get the whole story on the VGR 4000 and how it can meet your needs, call Durke Johnson at 303/773-4700. Or write Honeywell Test Instruments Division, Box 5227, Denver, Colorado 80217.

WE'LL SHOW YOU A BETTER WAY.

Honeywell

HON-6-631

CIRCLE 116 ON INQUIRY CARD

MORE BANG FOREVER

Forever is a long time and that's what Qantex Printers are designed to do, print for a long time. The new Qantex Impact Printers are perfect for applications where crisp copy is needed fast, reliably and at a modest cost.

The new feature packed Model 6010 incorporates a 2K or a 4K message buffer capable of accepting up to two full CRT screens of data. . . Switch selectable forms length from 3 to 22 inches in .5 inch increments. . . Switch selectable vertical tabbing, 4 or 6 lines. . . Horizontal tabs at columns 1, 9, 17, 25, etc. . . Adjustable tractors accept paper sizes from 3 to 15 inches, front or bottom feed. . . Multiple communications protocols accomodate parallel or up to 19,200 baud serial interfaces supporting RS-232, X-ON, X-OFF or current loop. . .

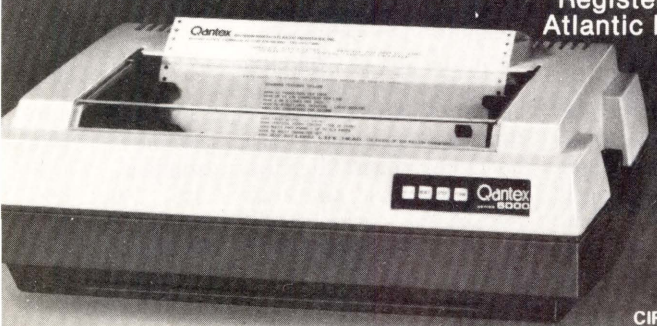
Other advanced features included at no additional cost include a sleek human factors engineered enclosure incorporating a low noise sound cover. . . Exceptionally high reliability resulting from simple mechanical and electronic design. . . 500 million character print head. . . High quality original plus up to five sharp copies. . . Beautiful 96 character set stored in the microprocessor in a 9 x 9 dot matrix. . . True lower case descenders and underlining. . . Bi-directional logic seeking. . . Built-in self test 150 characters per second. . . 80/136 columns per line. . . Available now!

For more information about the new Model 6010 contact your local distributor!

THE NEW MODEL 6010

Qantex*
Division of North Atlantic
60 Plant Avenue
Hauppauge, NY 11788
(800) 645-5292 (516) 582-6060
TWX (510) 227-9660

*Registered Trademark of North Atlantic Industries, Inc.



DISTRIBUTOR INQUIRIES WELCOME!

ARIZONA	
The Phoenix Group Inc.	(602) 967-1421
ARKANSAS	
Harvey Electronics	(501) 224-0899
CALIFORNIA	
Basic Systems Corp.	(213) 673-4300
Basic Systems Corp.	(714) 268-8000
Basic Systems Corp.	(408) 727-1800
ILLINOIS	
Electro Tech Marketing	(312) 588-4535
Engineered Sales	(312) 832-8425
LOUISIANA	
Micro Computer of New Orleans	(504) 885-5883
MARYLAND	(800) 645-5292
MASSACHUSETTS	
S & S Electronics, Inc.	(617) 458-4100
MINNESOTA	
Vikeland Sales	(612) 645-4647
MISSOURI	
ESC Sales & Leasing	(314) 997-1515
NEW YORK	
Daily Business Products, Inc.	(516) 543-6100 (800) 645-5556 (212) 594-8065
Straitline Marketing Inc.	(212) 445-4225
Synchro Sound Enterprises	(516) 484-1852
Washington Electric Co.	(212) 226-2121 (800) 221-5416
PENNSYLVANIA	
QED Electronics	(215) 674-9600
TEXAS	
Datanet Inc.	(214) 669-1758
VIRGINIA	
Nine Associates, Inc.	(703) 273-1803
AUSTRALIA	
Mitsui Computer Systems	02-9299921
CANADA	
Computer Markets	416-445-1978
DENMARK	
T.M.S. System i/S	(45) 02-840784
ENGLAND	
Northamber Limited	(44) 372-67646
FRANCE	
Gepsi	(33) 1-554-9742
GERMANY	
Technitron	49 (89) 692-4141
HONG KONG	
Hong Kong Equipment	3-444216-8
Computerworld Ltd.	5-440033
ITALY	
Eltron	39 (30) 55026
NETHERLANDS	
Compudata Benelux B.V.	31-73-422045
PORTUGAL	
Decada Equipamentos de Electronica Lda	351-19-558609
REPUBLIC OF CHINA	
Microcontrol Corp.	(02) 703-1842
SINGAPORE	
General Engineers Assoc. Pte. Ltd.	2729412
SPAIN	
2i Ingeniera Informatica	204-2099
VENEZUELA	
Sysgen Data	02-719455

CIRCLE 117 ON INQUIRY CARD

The network system provides a work-in-process management system with statistical quality control, and centralized test program storage and retrieval, without tying up production test time. The package also permits realtime process monitoring.

The software provides a choice of 8 data transfer options, ranging from 110 to 9600 baud. There are 3 options of 6, 7, or 8 bits/char. A std feature on all Troubleshooter 800 systems manufactured after July 22, 1981, the package is available free of charge to all current users of Troubleshooter 800 systems through the company's regional sales offices. **Zehntel, Inc,** 2625 Shadelands Dr, Walnut Creek, CA 94598.

Circle 295 on Inquiry Card

CAD software

SUPER SPICE, developed for computer aided design of analog and digital ICs, offers enhancements to the original SPICE program. Features include free format input, full editing capability, interactive graphics display, multilevel modeling capability, simple and elaborate models, subcircuit modeling, analysis with temperature dependency, and component values that can depend upon other components or on any branch voltage or current. The program is written in FORTRAN; core size is 1M byte. **COMSAT General Corp,** 950 L'Enfant Plaza SW, Washington, DC 20024.

Circle 296 on Inquiry Card

Enhanced ROSS/V operating system

Enhancements to ROSS/V software package include additional terminal handling capabilities such as support for RSTS/E's binary input mode, echo control mode, multiterminal I/O, and I/O escape sequence handling. Other enhancements include support for reading and writing DOS and ANSI file structured mag tapes and for specification of tape density and parity; support for "sys calls" not previously handled, including assigning and deassigning of devices, zeroing a mag tape, and setting terminal characteristics; and support for RSTS/E pseudo keyboards. **Evans Griffiths & Hart, Inc,** 55 Waltham, St, Lexington, MA 02173.

Circle 297 on Inquiry Card

Pascal compiler

Version 4.0 Pascal/Z™ includes overlays and the SWAT™ (SoftWare Analysis Tool) interactive debugger. SWAT aids in the isolation and correction of program faults generated by the compiler and software package. Overlay capability permits programmers to develop programs that are larger than the memory size of the computer. Using the LINK/Z linker/loader supplied with the package, routines are called and swapped into memory specifically allocated for overlays, while the main program remains resident in another portion. The package is provided in CP/M compatible format. **Ithaca Intersystems, Inc,** 1650 Hanshaw Rd, Ithaca, NY 14850.

Circle 298 on Inquiry Card

Interprocessor Communications Software

IPL-11 version 2.0 enables files to be transferred over either a telephone line or direct line using std terminal I/O ports. It operates between any 2 PDP-11/LSI-11/VAX-11 computers. Version 2.0 enhancements include a facility to run the package under the control of an indirect command file, enabling groups of files to be transferred at the execution of a single command. A remote activation facility enables the user to transfer files to or from a remote RSX-11M computer without requiring an operator at the remote computer. **Xoren Computing Ltd,** 28 Maddox St, London W1R 9PF, England.

Circle 299 on Inquiry Card

Realtime OS kernel

Written in C, OS/RT is highly portable and machine independent, requiring only a small machine dependent interface. The system is easily contained in ROM and supports 5 different resource types: memory, processes, events, interprocess communication, and interrupts. Designed for ease of program interface, the system features dynamic creation and destruction of resources, requires no fixed system tables, provides for optional separation of system and user data spaces, permits asynchronous event operation, and provides for controlled sharing of resources as well as deadlock prevention. **The DESTEK Group,** 1923 Landings Dr, Mountain View, CA 94043.

Circle 300 on Inquiry Card

Process control language

Designed for the 990E microcomputer system, language enables users with no formal knowledge of computer programming to program control applications. The equivalent of a relay ladder diagram can be generated without translating it into Boolean form; system displays the ladder on the development terminal as it is constructed. The completed ladder network can be programmed into EPROMs or P/ROMs and runs without additional support software. Language has 3 modes: command, edit, and process. Command mode controls the sequence of operations necessary to construct the ladder network; edit mode enters the desired elements into the network; and process mode compiles the input network, executes the scan after compilation, and performs a logical results evaluation of each scan. **Tau Zero, Inc,** 805 Business Pkwy, Richardson, TX 75081.

Circle 301 on Inquiry Card

68000 cross assembler

Full 68000 assembler accepts all std Motorola instruction mnemonics with the exception of certain "suffix variations" to some root mnemonics. All expressions are evaluated to a full 32 bits before any required truncation. Numerous directives or options permit page formatting, titles, subtitles, listing control, object code output control, sorted symbol table listing, line numbering, auto field formatting, warnings, command line parameters, inclusion of separate source files, and setting of even word boundaries. The assembler also supports conditional assembly and macros. Object code is output in Motorola S1/S2/S8/S9 records of ASCII hexadecimal data. Assembler executes on a 6809 microprocessor and is available for the FLEX™ or UniFLEX™ operating system. **Technical Systems Consultants, Inc,** PO Box 2570, West Lafayette, IN 47906.

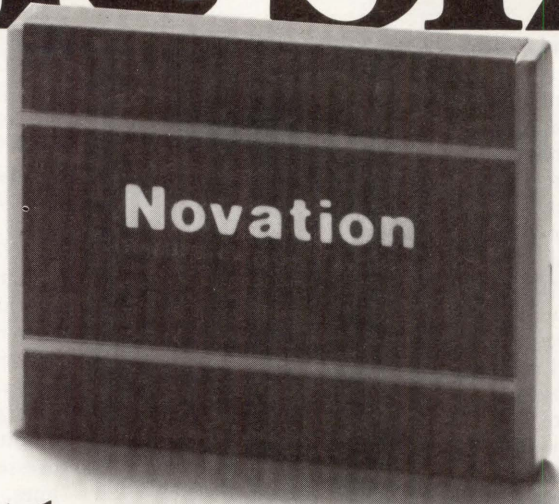
Circle 302 on Inquiry Card

Terminal management software system

TMS/I software system permits an IBM Series/1 computer running under the EDX operating system to operate as a data collection station for a network of the company's remote portable data entry terminals. Information is entered into the self-contained, battery powered terminals at remote sources and is transmitted over switched telephone networks to a 2741 protocol converter that transfers the data in useable form to the computer. This data can be directly processed or collected on the Series/1 and transmitted in batch to a larger host computer for processing. The system supports 2-way communications between terminals and computer. Up to 8 communication lines can operate simultaneously in 3 basic computer operating modes: attended, unattended, and auto dial. **MSI Data Corp,** 340 Fischer Ave, Costa Mesa, CA 92626.

Circle 303 on Inquiry Card

Life Size.



Save ⅓ the space with Novation's LSI Modem Modules.

Our LSI Modem Modules have only 11 parts, not 100, and just like that, you suddenly have a lot more design elbow room in all of the important ways.

First, space. No matter what you're used to, expect our modem to take up at least ⅓ less space.

Everything else is better, too. Performance is better. Reliability is better. Even the price is better; you'll save 10% or more.

All functions.

The modules are all the same size, but in that small package a variety of functions are available. For example: The Bell 103 or 202 series, CCITT V. 21 & V. 23—and more, including an FCC certified Phone Line Interface that eliminates the need for FCC certification of your system.

And if that doesn't cover everything you need, we can custom design a module to fit your specific application.

System Design.

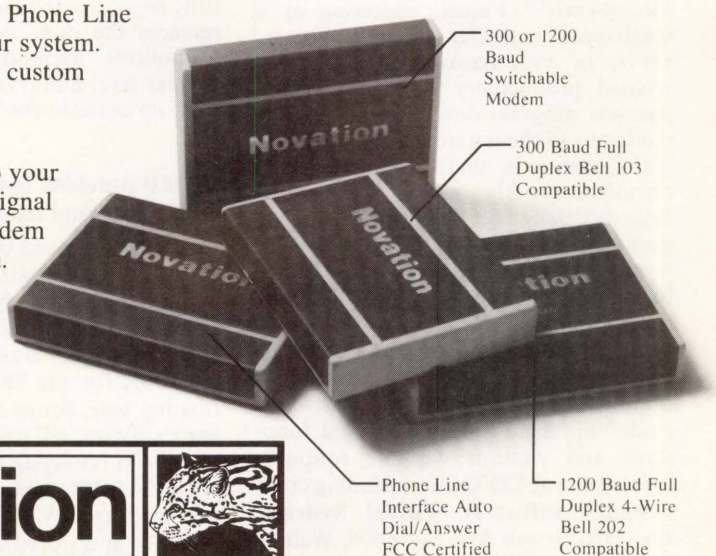
What's the best way to design one of our modules into your system? We'll show you. Just send us the pin-outs, interface signal description and form factor or dimensions of your current modem card. We'll take it from there and get a schematic back to you.

Tell us how many modules you'll need and we'll also give you a price.

The system design is free.

So, too, are any additional details. Write us. Or if you'd like some help right now, just call us or your nearest Novation representative.

2¾" x 2⅛" x ½"
That's all there is to it.



Toll free: (800) 423-5410
In California: (213) 996-5060

Novation

18664 Oxnard Street, Tarzana, CA 91356

Full-function BASIC interpreter for 68000 microcomputer

Designed for use with SP/68000™ and MSP/68000™ operating systems, interpreter is consistent with the syntax of common 8-bit BASICs, allowing most programs to be transported unchanged to a 16-bit 68000. It supports 32-bit integers, long and short floating point, and strings, in addition to all of the common mathematical and string functions. Features include cursor oriented EDIT command, PRINT-USING statement, full file support including random and sequential files, simple linkage to assembly language routines, dynamic string management with a full complement of string functions, and access to system functions without leaving BASIC. It also features program directed error trapping and tracing commands to simplify user debugging. **Hemenway Corp,** 101 Tremont St, Boston, MA 02108.

Circle 304 on Inquiry Card

Pascal software package

Program development system package for HP 9835 and 9845 desktop computers provides Pascal and assembly languages plus an OS, and resides on a tape cartridge and flexible disc. Min required user memory is 128k bytes for the 9835 system, and 187k bytes for the 9845. An assembly language execution ROM, a mass storage ROM, and a disc drive are required; and an internal or external printer is recommended for hardcopy output. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 305 on Inquiry Card

Pascal cross compiler

Microbench™ Pascal, operating as a single-pass compiler on DEC PDP-11, LSI-11, or VAX hardware, permits increased productivity while minimizing 8086/8088 program development time. It conforms to the ISO std Pascal language, with extensions that include external compilations, the ability to link to assembly language subprograms, support of single- and double-precision integers, support of underscore as a letter in identifiers, and the ability to conditionally compile program assertions to facilitate debugging. Average compilation rate is 200 lines/min, including optimizer and code generator phases. Included are a std library of Pascal functions and runtime support routines. Prices start at $3500 (not including cross assembly software). **Virtual Systems, Inc,** 1500 Newell Ave, Suite 406, Walnut Creek, CA 94596.

Circle 306 on Inquiry Card

INTEGRATED CIRCUITS

High density hard array logic circuits replace small and medium scale TTL components

HMSI™ bipolar circuits replace std TTL components at the ratio of 2 to 1 and offer additional features not provided by the TTL family. The series is composed of 7 devices: an 8-bit counter, 10-bit counter, 8-bit shift register, 8-bit multimode register, 16 to 1 multiplexer, dual 8 to 1 multiplexer, and quad 4 to 1 multiplexer. All are housed in 24-pin ceramic 0.3″ (0.8-cm) wide SKINNYDIP™ packages to increase space savings and design flexibility.

SN54/74LS461 8-bit counter is similar to the Texas Instruments SN54/74LS161, but replaces it 2 to 1. The device has 3-state outputs with 24-mA sinking current for bus driving. The 10-bit counter SN54/74LS491 handles the 9- or 10-bit resolution required for vertical and horizontal coordinates of video displays. It will also count either up or down.

Byte-wide expandable SN54/74LS498 8-bit shift register provides parallel to serial as well as serial to parallel data conversions. It has structured pinout and 3-state outputs with 24-mA sinking current for bus driving. SN54/74LS380 multimode register combines the features of the SN54/74LS374, SN54/74LS377, and SN54/74LS273 from Texas Instruments, plus the added features of "load complement" and "preset" that allow inverted data operations.

The 16 to 1 multiplexer (SN54/74LS450) is a 1 to 1 replacement for the SN54/74LS150, while the dual 8 to 1 multiplexer (SN54/74LS451) corresponds to the single SN54/74LS151, but replaces it 2 to 1. SN54/74LS453 quad 4 to 1 multiplexer replaces the dual SN54/74LS153 2 to 1. **Monolithic Memories, Inc,** 1165 E Arques Ave, Sunnyvale, CA 94086.

Circle 307 on Inquiry Card

EEPROM provides in-circuit alterability and nonvolatility

A low cost version of the byte-erasable 2816 EEPROM, the 2815 16k-bit EEPROM is organized as 2k x 8 bits with a std read-access time of 250 ns max, and requires 50 ms to write or erase a byte (compared to 10 ms for the 2816). The chip is a floating gate device that uses the company's Flotox cell structure and Fowler-Nordheim tunneling to store, write, and erase data. Pin compatible with the 2816 and with 2716 UV erasable EPROMs, the device retains stored data for 10 years. It is fully static and never requires refreshing, regardless of read frequency.

Application of a 21-V pulse for 50 ms erases any byte or the chip's entire contents. The same procedure is used to write new data into the chip's 2048 storage locations, 1 byte at a time. Any storage location can be altered up to 10,000 times. A single-byte program change can be made 20 times faster than on a bulk-erase part; any of the chip's 2k bytes can be erased and rewritten in 100 ms.

Rated for operation from 0 to 70 °C, the low power chip draws 120 mA of current from a single 5-V supply when active, and 60 mA in standby mode. Separate chip-enable and output-enable pins permit 2-line control of the chip, eliminating contention between addresses and data on multiplexed bus lines. Available in a 24-pin DIP, the chip has pinout that conforms to the JEDEC std for high density, byte-wide memories used in microcomputer systems. The U.S. price of the std (250-ns) chip is $26.50 each in 10,000-piece quantities. Also available are 350- and 450-ns versions. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 308 on Inquiry Card

High speed data drivers

Models 310H and 10910H, packaged in 24-pin DIPs, have output signals that range over ±15 V (30 V pk-pk) and ±10 V (20 V pk-pk), respectively. For the 310H, data repetition rates of up to 20 MHz are possible, depending on amplitude, with pulse widths as narrow as 20 ns; for the 10910H, data repetition rates to 100 MHz, depending on amplitude, with 5-ns pulse widths are attainable. Rise and fall transition times are 12 ns for the 310H at 30 V pk-pk and 2 ns for the 10910H at 10 V pk-pk. **Versatile Integrated Modules,** 1283-A Mountain View-Alviso Rd, Sunnyvale, CA 94086.

Circle 309 on Inquiry Card

Programmable digital timer circuit

Slow operate, slow release, intervals, and flashings from 6 μs to infinity can be programmed with the LS7210 monolithic, ion-implanted PMOS circuit. Delay duration is a function of the frequency and a weighting factor programmable from 1 to 31. With an internal oscillator, delays of 36 days are possible; longer delays can be obtained using an external clock or by cascading 2 or more circuits. Features include power-on reset, internal pullups on inputs, and CMOS type noise immunity on all inputs. **LSI Computer Systems, Inc,** 1235 Walt Whitman Rd, Melville, NY 11747.

Circle 310 on Inquiry Card

When you're down to the wire™:

Nobody can support you with mass termination products like Spectra-Strip can.

We make more variations of flat cable than any one: laminated, extruded and bonded, grey and color coded. Jacketed cable for inter-cabinet runs. Ground plane cable to reduce cross-talk. Even a twisted-pair flat cable that can be mass-terminated, so you get the performance you want and the lower costs you need.

Our connectors are more of the same: high quality, high performance and low prices. Choose from a range of pin headers and receptacles, DIP plugs and sockets, PCB transitions, and card edge connectors built to the relevant portions of MIL-C-83503 and MIL-C-21097. And IDC D-Subminiature connectors with metal shells (fully intermateable and intermountable with any of the other real D-Sub's).

We can also lower your capital investment, inventory and labor overhead. Let us prepare your jumpers for up to 20% less than you're paying now. Call your nearest Spectra-Strip value-added distributor for economical, fully-tested flat cable and IDC connector assemblies. Or call Garden Grove for custom assemblies that combine flat cable with the other kinds of interconnects you need. Whatever your applications, if you're down to the wire on price, performance or delivery, there's one simple solution:

Spectra-Strip, 7100 Lampson Ave., Garden Grove, CA 92642, telephone (714) 892-3361 and 720 Sherman Ave., Hamden, CT 06514, telephone (203) 281-3200.

In Europe, Spectra-Strip Ltd., Romsey, Hampshire, England, telephone (0794) 517575.

Call now for the name of your nearest distributor.

SPECTRA-STRIP

An ALLIED Company

4k nonvolatile RAM

NCR 4485 contains duplicate planes of static RAM cells and nonvolatile storage cells. Data stored in static cells are transferred to the nonvolatile cells, and thus retained, whenever system power is interrupted. Device has a byte-wide (512 x 8) organization. In RAM mode, it is fully static, with TTL compatible inputs and outputs, and requires a single 5-V power supply. Worst-case power dissipation is 600 mW, and worst-case access time is 450 ns. For nonvolatile erase and store operations, −22 V and 22 V are required, but less than 20 μA of current are drawn. The device is available in a std 28-pin plastic or ceramic package. The upper 24 pins comply with the JEDEC std of byte-wide memories, and the lower 4 pins are used for nonvolatile operations. **NCR Corp, Microelectronics Div,** 1700 S Patterson Blvd, Dayton, OH 45479.

Circle 311 on Inquiry Card

Semicustom bipolar gate arrays

Q-700 quick chip bipolar gate array series is 74LS and 74S TTL compatible as well as ECL 10k compatible. Device is available with 250, 500, or 1000 gate arrays and features 0.9-ns/gate typ speed (gate within a function cell); simultaneous TTL and ECL operation; ECL/TTL translation onchip; up to 76 inputs; macro logic function library, computer-aided simulation and circuit routing; and military or commercial op temp ranges. Series offers high complexity at sub-ns propagation delay speeds, permitting higher subsystem performance by reducing on/offchip transitions. **Applied Micro Circuits Corp,** 10626 Bandley Dr, Cupertino, CA 95014.

Circle 312 on Inquiry Card

DATA CONVERSION

D-A converter incorporates pin programmable logic functions for system and process control

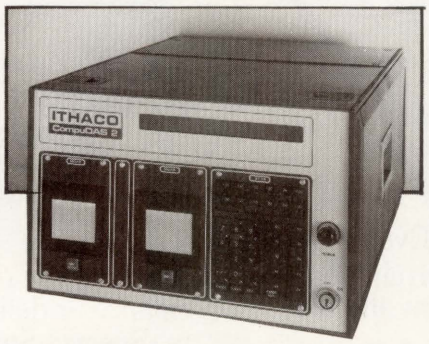
Monolithic, 10-bit, CMOS AD7527 DAC contains microprocessor compatible input registers, 3-state drivers, an up/down counter, and the necessary control logic for data readback, data increment/decrement operations, and either left- or right-justified data formats. Double-buffered input data latches allow 10 bits of data to be loaded in 2 operations from 8-bit buses and in 1 operation from 16-bit buses. DAC output updating can be immediate or deferred. Three-state data bus drivers allow the contents of the DAC register to be read back over whatever bus is in use.

The up/down counter increments or decrements the DAC register. Either an onchip oscillator or an external clock can determine count rate. Activated by 2 control inputs, this capability allows continued control of a process in the event of computer failure. Two equal and matched resistors are included for developing a 4- to 20-mA output. The override feature can select 1 of 3 codes for zero-, half-, or full-scale output for system initialization and calibration or, in process control applications, to provide 3 commonly used valve settings.

Relative accuracy is guaranteed at ±1 LSB max for KN, BD, and TD grades and at ±½ LSB max for LN, CD, and UD grades. Max gain error is guaranteed at ±10 LSBs for KN, BD, and TD grades, ± 5 LSBs for LN, CD, and UD grades, and ±1 LSB for G grades. Multiplying feedthrough error is 2 mV max. Housed in a 28-pin plastic or ceramic DIP, the device is available with 3 op temp ranges: 0 to 70, −25 to 85, and −55 to 125 °C. It is also available in chip form and in leadless chip carriers for hybrid applications. **Analog Devices,** Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062.

Circle 313 on Inquiry Card

Data acquisition and control system



Based on a 5-MHz Z80B microprocessor, CompuDAS 2 has true multi-user capability, allowing multiple independent programs or tests to run simultaneously; and complete multitasking capabilities, allowing each user to create and implement multiple tasks within his program. System supports over 300k bytes of user available dynamic RAM and up to 80k bytes of user available ROM or EPROM space. It is programmed in DABIL™, the company's version of ANSI std BASIC, with English-like commands for analog and digital inputs and outputs and with variable names of up to 160 char in length. Two RS-232-C compatible ports are std; 3 additional ports are optional. These ports support independently programmable baud rates from 50 to 19,200 baud. Bulk storage can be provided with single or dual microcassette units, a 4-track digital cartridge recorder, or a 9-track, 0.5″ (1.27-cm) mag tape drive. **ITHACO, Inc,** 735 W Clinton St, Ithaca, NY 14850.

Circle 314 on Inquiry Card

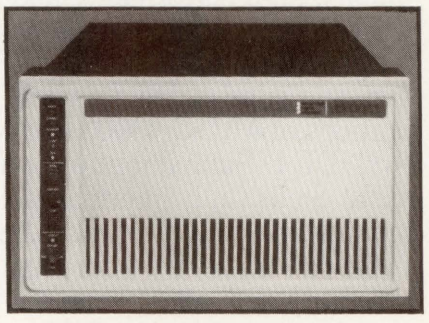
COMPUTERS

Minicomputer features 100-ns arithmetic instruction execution time

NOVA-compatible MiniMate™ minicomputer features 200-ns load and store time plus memory access time of 55 ns to a capacity of 128k bytes. DMA transfer time is 800 ns, with a slow speed channel slot-selectable on the backplane. Backplane features priority encoding to ease configuration changes. Eight of the 9 slots are free, providing increased system flexibility.

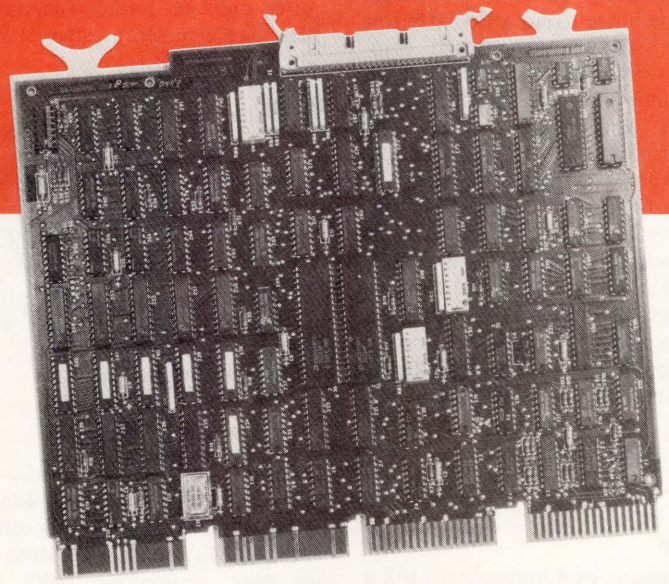
Features include execution/DMA overlap (processor is slowed by 25% during memory access); virtual front panel; switch convenience outlet on rear; modular, field replaceable power supply that includes all fans; and software compatibility with a variety of operating languages including IRIS, RDOS, BLIS/COBOL, VMOS, and others. An onboard battery backup system maintains memory for 3 days even if the board is removed from the computer.

As a board-only computer, the system plugs into any foreign chassis and requires 5 V of power. In its own 10.5 x 19 x 19″ (26.7- x 48- x 48-cm) chassis, the system includes CPU, memory, and power supply. The complete system, with 64k of memory, is priced at $7875; with 128k of memory, price is $9975. The system is also available with the MiniMeg™ solid state memory system that functions as a cache to store and retrieve frequently used data. **Integrated Digital Products,** 3156 E La Palma Ave, Unit A, Anaheim, CA 92806.



Circle 315 on Inquiry Card

DEC®-COMPATIBLE PERIPHERAL CONTROLLERS



Dataram Corporation offers the industry's widest range of DEC-compatible peripheral controllers — from comparatively simple NRZI tape controllers to complex 300 MB storage module drive (SMD) controllers.

An impressive array of state-of-the-art controllers, all built around high-speed bipolar microprocessors. All software compatible with the host LSI-11®, PDP®-11, or VAX® minicomputer...and all available now.

And Dataram's controllers are designed to save you money, and, more importantly, space — our controllers typically occupy half the space required for the comparable controller from DEC. Doing it with a level of performance that makes any member of this family worth looking at.

The chart shows our current family of peripheral controllers, growing every day. If you don't see the controller you need, we're probably working on it right now. Call us and discuss your requirements.

CONTROLLER	DESCRIPTION	COMPATIBILITY
C03	Cartridge disk controller	RK05
C33	Cartridge disk controller	RK05
T03	NRZI mag tape controller	TM11/TU10
T04/N	NRZI mag tape controller	TM11/TU10
T04/D	Dual density mag tape controller	TM11/TU10
T34/N	NRZI mag tape controller	TM11/TU10
T34/D	Dual density mag tape controller	TM11/TU10
T36	Dual density mag tape controller	TM11/TU10
S03/A	80MB/300MB SMD controller	RM02/RM05
S03/A1	160MB SMD controller	RM02
S03/B	80MB/300MB SMD controller	RK07
S03/C	200MB/300MB SMD controller	RP06
S03/D	96MB CMD controller	RK06
S33/A	80 MB/300 MB SMD controller	RM02/RM05
S33/A1	80 MB/160 MB SMD controller	RM02
S33/B	80 MB/300 MB SMD controller	RK07
S33/C	200 MB/300 MB SMD controller	RP06
S33/D	96 MB CMD controller	RK06

Products printed in red are LSI-11 Bus compatible.

Products printed in black are UNIBUS® compatible for PDP-11 and/or VAX minicomputers.

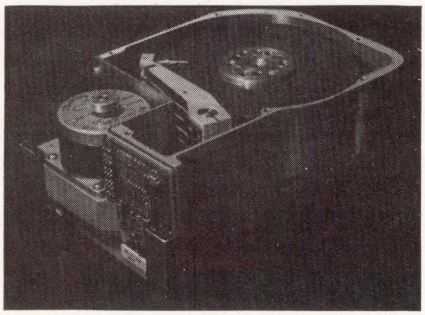
DEC, LSI-11, PDP, UNIBUS and VAX are registered trademarks of Digital Equipment Corporation.

DATARAM CORPORATION

Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

Canada: Ahearn & Soper Ltd., 416-245-4848 • **Denmark:** Technitron ApS, 02 96 98 22 • **Finland:** Systek OY, (80) 73 72 33 • **France:** YREL, (03) 956 81 42 • **Hungary/Poland/Rumania:** Unitronex Corporation, WARSAW 39 6218 • **Italy:** ESE s.r.l., 02/607 3626 • **Netherlands:** Technitron b.v., (020) 45 87 55 • **Sweden:** M. Stenhardt AB, (08) 739 00 50 • **Switzerland:** ADCOMP AG, 01/730 48 48 • **United Kingdom:** Sintrom Ellinor Ltd., (0734) 85464 • **West Germany:** O.E.M.-Elektronik GmbH, 07 11-79 80 47 • **Yugoslavia:** Institut "Jozef Stefan", 263-261 • **Australia/New Zealand:** Anderson Digital Equipment, (03) 544-3444 • **India:** Infosystems Private Limited, 79281 • **Israel:** Minix Computers & Systems Ltd., 03-298783 • **Japan:** Matsushita Electric Trading Co., Ltd., 06 (282) 5111 • **Taiwan:** Rabbit Associates, Ltd., 7219573-5 • **Hong Kong:** Automated Systems (HK) Ltd., 5-630256-9 • **Malaysia:** Automated Systems (M) Sdn Bhd., 773777 • **Indonesia:** P. T. Daya ASL, 584306 • **Singapore:** Automated Systems (PTE) Ltd., 2354133

5.25″ Winchester drives provide up to 16M bytes of storage



RO 100 series consists of four 5.25″ (13.34-cm) Winchester disc drives. Model RO 104 is a 4-platter device offering 16M bytes of unformatted storage (12.58M bytes when formatted in the std soft-sectored 256 bytes/sector format). High capacity is achieved using both sides of the disc, and recording at 8100 bits/in (3189/cm) and 10,417 bytes/track, with 384 tracks/disc. RO 102 and RO 103 have 2 and 3 platters, respectively, providing 8M and 12M bytes of unformatted storage. RO 101 is a single-platter drive with an unformatted capacity of 4M bytes.

Drives use the Winchester sealed chamber principle, but with 2 interconnected chambers, 1 containing the discs and the other the drive linkage mechanisms. Chambers are connected by a passage that permits the circulation of air between them, maintaining a high degree of thermal equilibrium between the discs and the actuator. Head/track misregistration due to temp difference is less than 1 μm throughout the temp range.

A microprocessor on the control board handles head positioning and power-up sequencing and monitors 10 potential fault conditions. A preamplifier board is positioned close to the heads to reduce noise and rfi. Dc motor speed is controlled to within 0.1%. Average access time is 85 ms, achieved using the microprocessor to buffer incoming step pulses and to select and implement the appropriate speed and damping algorithms. Data transfer rate is 5M bits/s, with a disc rotational speed of 3600 r/min.

There are no electrical or mechanical adjustments on the drive, and no preventive maintenance is required. Series is compatible with industry standards for electrical interface, power requirements, and drive size. Electrical interface is compatible with industry std controllers. Drives run from 5- and 12-V supplies and measure 8 x 5.75 x 3.25″ (20 x 14.61 x 8.26 cm). **Rodime Ltd**, 12-14 Edison House, Fullerton Rd, Glenrothes, Fife, KY7 5QR, Scotland.

Circle 316 on Inquiry Card

128k-byte bubble memory board

A fully integrated magnetic bubble memory module, iSBX-251, contains all support and control circuitry for interfacing with microprocessor based, single-board computers. The 128k-byte (1M-bit) bubble Multimodule board is software supported in iRMX-86 and iRMX-88 operating systems. Its simple design contributes to a particularly low entry cost. The iSBX-251 board communicates with the iSBC single-board host computer board via the built-in SBX bus. This arrangement frees the MULTIBUS for other traffic while the host iSBC board accesses the bubble memory. Interfacing firmware is already onboard the iSBC boards. Data access time for the memory board is 48 ms. Data can be transferred at the rate of 12.5k bytes/s in either direct memory access, interrupt, or polled modes. The board is priced at $1200 for quantities of 100. **Intel Corp**, 1302 N Mathilda Ave, Sunnyvale, CA 94086.

Circle 317 on Inquiry Card

128k-DRAM

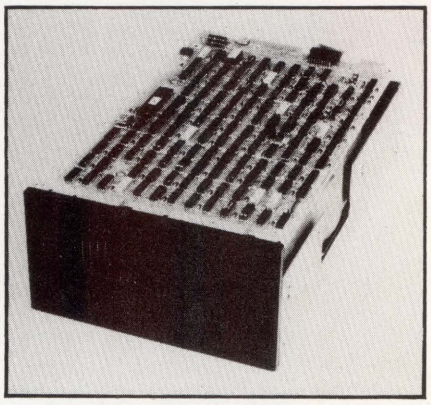
EDH-4816 consists of 8 industry std 16k x 1 RAMs in chip carriers mounted on a 32-pin single inline package. The device is available as 16k x 8 or 128k x 1 and requires only 0.66 in^2 (4.26 cm^2) of board space. Access time is 200 ns and cycle time is 375 ns. All supply voltages are decoupled with ±10% tolerance. Power required is 3.8 W max active and 160 mW standby. Price is $59 each in quantities of 100. **Electronic Designs, Inc**, 230 Eliot St, Ashland, MA 01721.

Circle 318 on Inquiry Card

8″ Winchester disc drives combine high capacity, fast access time, and ease of integration

SA1100 series consists of 20.3M-byte, 2-platter SA1104 and 33.9M-byte, 3-platter SA1106 Winchester disc drives. The series uses the FASTRAK™ closed-loop servo positioning system to offer 35-ms avg access time with recording densities of 500 tracks/in (197/cm). Position information is prerecorded on the underside of the bottom platter; under the control of a single-chip microprocessor, the servo head reads the servo information and positions the actuator over the correct cylinder. High positioning precision is achieved as the servo head is directly coupled to the data heads by the actuator assembly.

Track to track access time is 10 ms; max access time is 70 ms. Transfer rate is 4.34M bits/s. Automatic head retraction on loss of power to a dedicated head landing/shipping zone, plus shipping locks and spindle and head-arm parking restraints provide max data protection during power-off conditions. An all metal head and disc enclosure reduces the potential for emi and optimizes head transfer and dissipation. Series features a brushless dc spindle motor and requires only 24- and 5-Vdc power supplies. Ambient temp range is 50 to 115 °F (10 to 46 °C).



The series provides upgradability to SA1000 series users with only minor software modifications; the 2 drive families are plug compatible, with identical package size, mounting specifications, track capacity, and data rate. In addition, the drives are command bus compatible with SA801/851 series 8″ (20-cm) floppy disc drives, aiding integration with backup and I/O peripherals using SA1400 controllers. **Shugart Associates**, 475 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 319 on Inquiry Card

Dynamic memory system

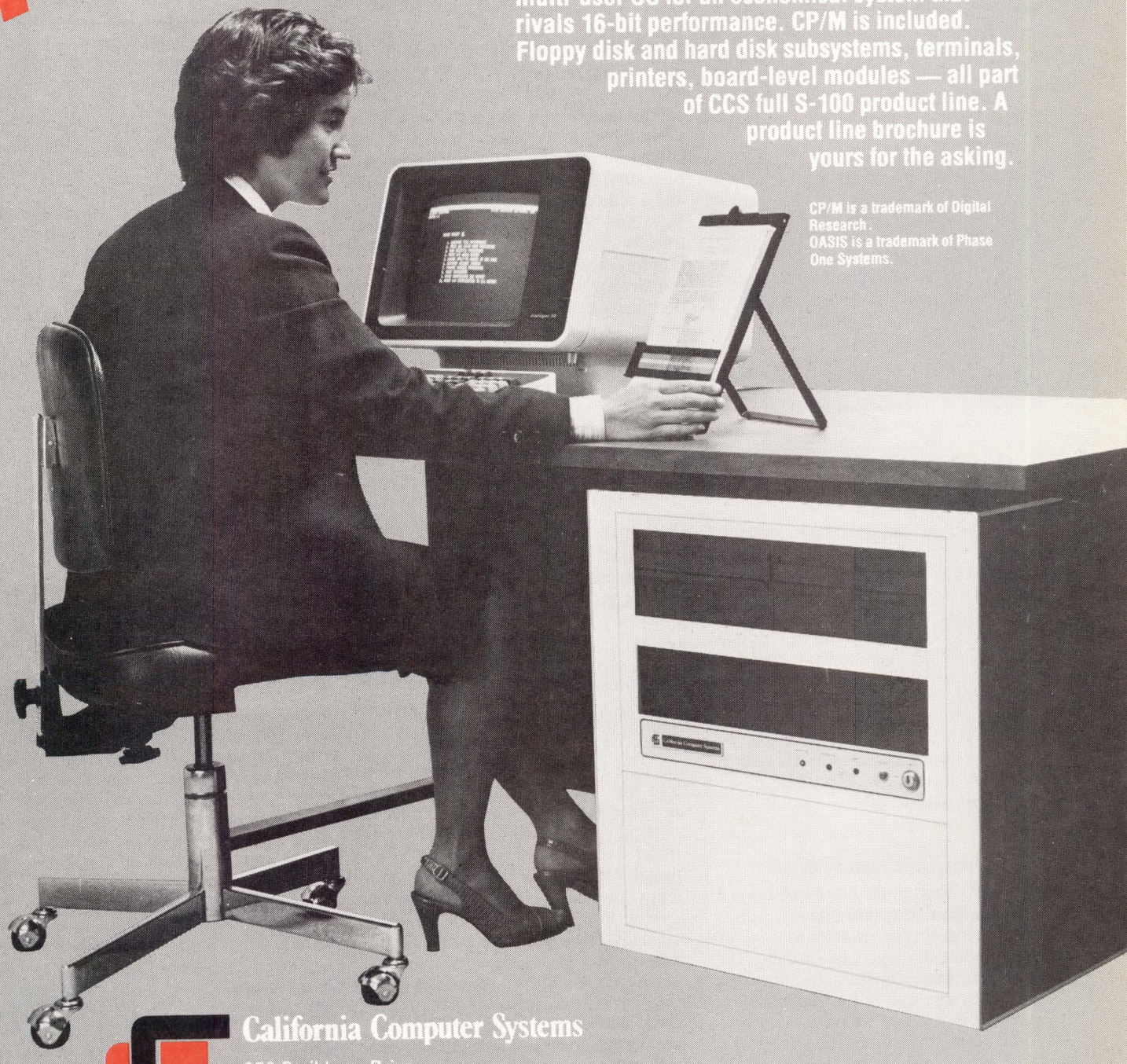
Designed for operation with the Motorola EXORcisor™ I or II and Rockwell system 65, CI-6800-2 is available in 16k-, 32k-, 48k-, or 64k-byte configurations. The board plugs directly into existing EXORcisor connectors and allows max processor throughput with the use of hidden refresh control logic onboard. Data access time is 225 ns, and cycle time is 400 ns, allowing the unit to operate as a static RAM at clock rates in excess of 1.5 MHz. Onboard memory select is available in 4k increments up to 64k words of memory on either the VUA or VXA control inputs. Memory has onboard even parity with output jumper selectable to the system bus as a parity error or nonmaskable interrupt. Complete board power consumption is less than 7 W. **Chrislin Industries, Inc, Computer Products Div**, 31352 Via Colinas, #102, Westlake Village, CA 91361.

Circle 320 on Inquiry Card

SYSTEMS KICKER.

Reliability, price, and a performance kicker that leaves other 8-bit systems far behind: Real-time hardware vectored interrupts and the OASIS multi-user OS for an economical system that rivals 16-bit performance. CP/M is included. Floppy disk and hard disk subsystems, terminals, printers, board-level modules — all part of CCS full S-100 product line. A product line brochure is yours for the asking.

CP/M is a trademark of Digital Research.
OASIS is a trademark of Phase One Systems.



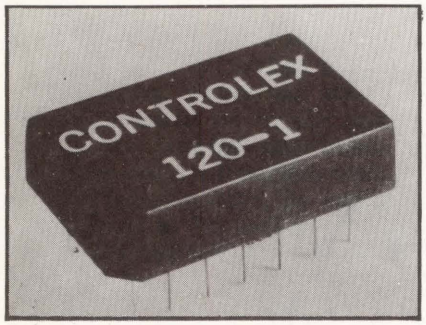
California Computer Systems
250 Caribbean Drive
Sunnyvale, California 94086
(408) 734-5811
Telex 171959 CCS SUVL

MAKING MINIS OUT OF MICROS.

CIRCLE 121 ON INQUIRY CARD

Tiny core memory modules

Designed for nonvolatile storage of critical microprocessor data, model 120 is a 4-bit array that stores a status word upon power shutdown or loss, and retains it for an infinite time. The device operates with 5-V power and uses low cost common TTL logic chips as support circuits. Data are loaded sequentially in 4 cycles and retained indefinitely on shutdown. On bring-up, data are sequentially loaded back through the I/O port to return the status word. The device is packaged in a 14-pin DIP and is available as either a core module only or with supporting circuitry mounted on a 1 x 2″ (2.54- x 5.08-cm) PCB ready to plug into the host system. Basic price is $6.90 each in OEM quantities. **Controlex Corp,** 16005 Sherman Way, Van Nuys, CA 91406.



Circle 321 on Inquiry Card

Ruggedized digital recorder

Model 4000-400 and -500 series systems apply commercial ruggedizing techniques to mil-type applications. Recording media is a Phillips cassette with optional data capacity of 500k to 5M bytes/tape. Interface options include RS-232 to 19.2k baud, 8-bit parallel, IEEE-488, and plug compatibility with Centronics, Printronix, or Dataproducts printers. Power required is 115/230 Vac, 50 or 60 Hz, or dc to ac inverter 150 W. **Saylor Electronics International,** 1408 E Katella Ave, Anaheim, CA 92805.

Circle 322 on Inquiry Card

9-track magnetic tape subsystem

Designed for use with DPS 6 and Level 6 small computers, subsystem supports both 1600-bit/in (630/cm) PE or 6250-bit/in (2461/cm) GCR formats. The basic subsystem consists of a magnetic tape controller and one 9-track primary magnetic tape drive; 3 tape drives can be added to the subsystem for a total of 4 tape units. Std tape speed is 125″ (318 cm)/s, for a max throughput capability of 780,000 bytes/s. Features include internal data buffering, automatic tape threading or cartridge load, vacuum assisted tape cleaning, reading or writing on one tape unit simultaneously with rewinding or unloading on other units, rewind and unload of a 2400′ (732-m) reel in 1 min, power hub, and power window. A full set of operator controls and indicators monitors major subsystem functions, while a test and maintenance program aids in fault isolation and equipment maintenance. **Honeywell Inc,** 200 Smith St, Waltham, MA 02154.

Circle 323 on Inquiry Card

Winchester/floppy storage system

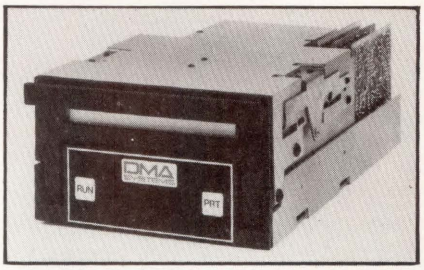
FWT series offers 8.9M-, 17.8M-, 26.7M-, or 35.6M-byte, 8″ (20-cm) Winchester disc storage plus a 1M-byte, IBM compatible double-sided floppy. Plug compatible interfaces are available for DEC PDP-11 and LSI-11, Intel MULTIBUS, and a general purpose byte parallel interface. For Winchester disc storage, max transfer rate of 543k bytes/s is possible. Floppy diskettes require less than 60 s to transfer 1.2M bytes of data to or from the Winchester disc. Disc drives, formatter, power supply, and cabling are contained in a low profile 5.25″ (13.34-cm) rack or tabletop enclosure. Extensive test and diagnostic features are included in each system. Prices start at $6200. **Scientific Micro Systems, Inc,** 777 E Middlefield Rd, Mountain View, CA 94043.

Circle 324 on Inquiry Card

Disc drive provides both fixed and removable file storage

MICRO-MAGNUM™ 5/5 disc drive is composed of two 5.25″ (13.34-cm) discs: an internal, nonremovable component; and a removable, portable data cartridge. Each drive has a storage capacity of 5M bytes of formatted data, for a system total of 10M bytes (13.5M bytes unformatted). Avg data access time is 40 ms, and data transfer rate is 5 MHz. Both fixed and removable disc compartments are self-sealing to protect against outside contaminants entering and affecting critical recording areas. Drive has a frontal form factor identical to mini-floppy disc dimensions, and mounts directly into housings and cabinetry originally designed for mini-floppy discs.

Featuring an all dc power design to meet worldwide requirements, the system is microprocessor controlled for high performance and reliability. It provides quiet operation for office environments, wide temp/altitude envelopes, shock-mounted design, 8000-h power-on reliability, and a total disc copy time of under 90 s. The system can be vertically or horizontally mounted and requires no read/write head alignment or preventive maintenance.

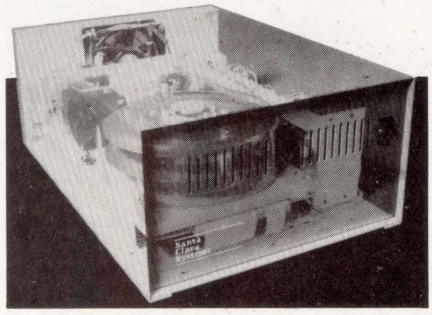


A 5.25″ (13.34-cm) oxide disc that is clamped to a hub and housed in a lightweight plastic enclosure comprises the system's data cartridge. Both cartridge and receiver mechanism have been designed to prevent improper media insertion. The disc and hub are constrained to prevent inadvertent contact with interior portions of the cartridge housing. Prerecorded embedded servo information on the disc surface facilitates cartridge interchange between systems. The fixed/removable disc drive is priced at $1275; the data cartridge is priced at $45 each in OEM quantities. **DMA Systems,** 325 Chapala St, Santa Barbara, CA 93101.

Circle 325 on Inquiry Card

Winchester/floppy disc drive subsystem

Model SCS-10/F interfaces to Apple II, TRS-80 I, II, and III, S-100 microcomputers, MULTIBUS, LSI-11, and Motorola 6800. It permits the use of most existing disc operating systems, allowing std 8″ (20-cm) CP/M floppy discs to operate with Apple II machines and 3.3 Apple DOS with 1.1 Pascal. The subsystem includes an Apple II, Microsoft CP/M, or std 8″ (20-cm) diskette, plus the ability to run Apple DOS 3.3 and Pascal 1.1. Error correction coding provides media error correction that is transparent to the host system. Storage capacities range from 10M to 120M bytes. Disc drive daisy chaining is permitted for higher storage levels. **Santa Clara Systems, Inc,** 560 Division St, Campbell, CA 95008.



Circle 326 on Inquiry Card

From concept...to prototype...to production. Faster. With Multiwire® circuit boards.

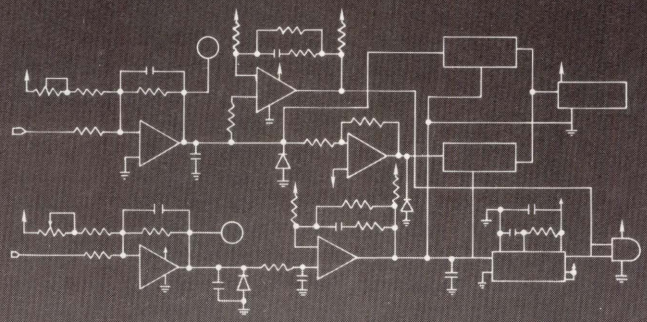
Just give us a net list and board layout. You'll get a computer-generated design, prototypes, and delivery of production boards in a fraction of the time you would expect.

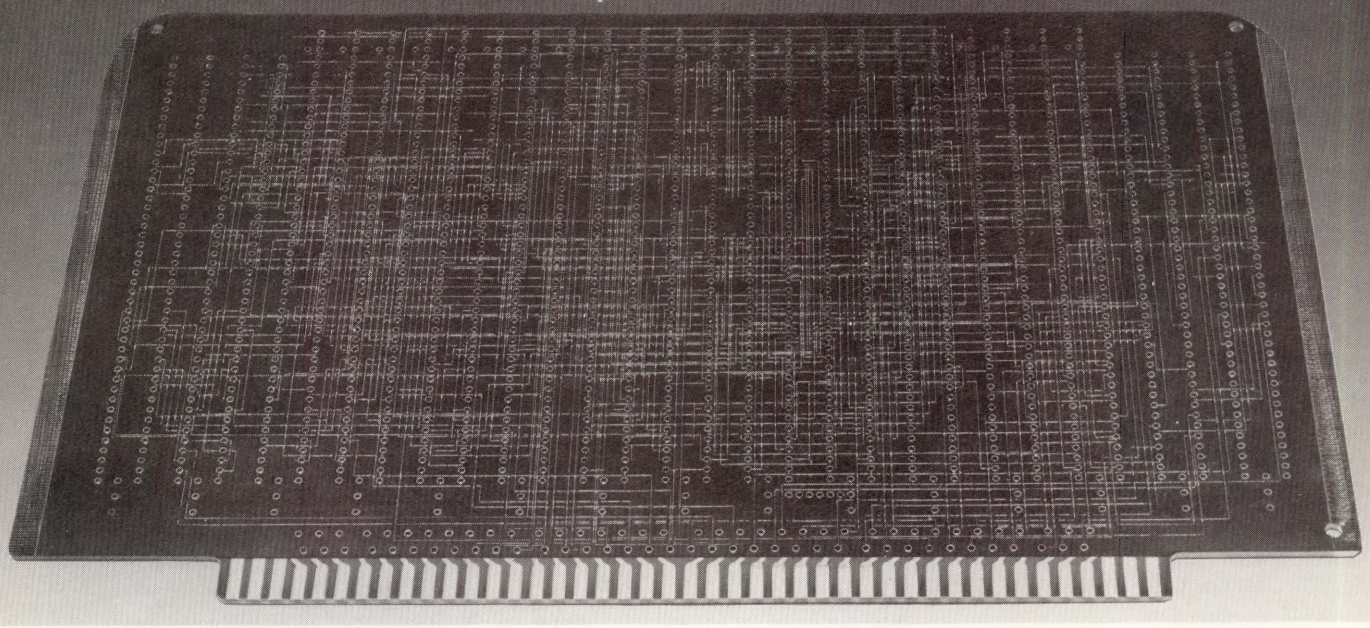
The Multiwire process is simply *faster* than multilayer . . . all the way from board design through manufacture to function. Especially working with high density interconnects.

A Multiwire circuit board is a pattern of insulated wires bonded to an epoxy glass substrate by a high-speed CNC machine, and terminated by plated through holes. It offers greater control of electrical characteristics, improved reliability, higher density, and fast changes for component updates and ECO's.

Multiwire is new. And different. And it has been proved in demanding applications by over 200 of the world's leading electronic manufacturers.

Call today. Tell us your specs. Let *us* tell *you* exactly how Multiwire can get your product to market first.





Licenses to design and manufacture Multiwire circuit boards are available from PCK Technology Division, Kollmorgen Corporation, 322 S. Service Rd. Melville, NY 11747 (516) 454-4442

Call your nearest Multiwire producer for full details
(or circle appropriate Reader Service No.)

I-CON Industries
1103 So. Airport Drive
Euless, Texas 46039
(817) 267-4466
Dallas/Ft. Worth
(817) 283-5361
Houston
(713) 733-7033
Orlando, FL
(305) 422-2272
Circle 122 on
Inquiry Card

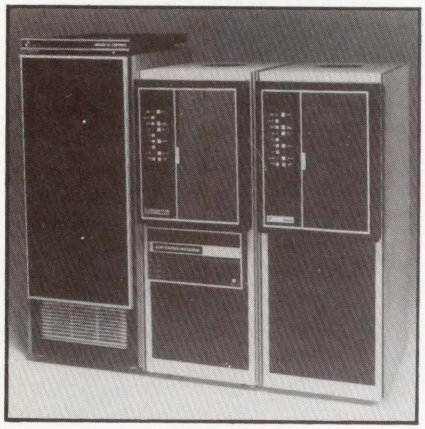
Circuitech, Inc.
1108 Pollack Avenue
Asbury Park, NJ 07712
(201) 493-4102
TWX 710 723-4620
Circle 123 on
Inquiry Card

Space Circuits, Ltd.
605 Kumpf Ave.
Waterloo, Ontario
Canada N2J 4A4
(519) 886-6670
TWX: 069-55326
Circle 124 on
Inquiry Card

MULTIWIRE®

Military tape subsystem

Group 30 military tape subsystem for AN/UYK series military computers includes tape drives and 5042 control processor, and incorporates a 256k-byte buffer and interface for AN/UYK computers. Both 75″ and 125″ (191- and 318-cm)/s models are offered, each permitting 800-, 1600-, and 6250-bit/in (315, 630, and 2461/cm) mode operation. Data transfer rate is 781k bits/s, on 0.5″ (1.27-cm) 9-track tape. Up to 4 channel interfaces can be accommodated through a single 5042 control processor. **Amperif Corp,** 21345 Lassen St, Chatsworth, CA 91311.



Circle 327 on Inquiry Card

High density memory expansion module

GMS6521, with a capacity of up to 65,536 x 8 bits of EPROM/PROM/ROM, is jumper selectable to accept Intel 2758, 2716, or 2732; or Texas Instruments 2508, 2516, or 2532 EPROMs with 1k, 2k, or 4k bytes/device. Requiring only 5-Vdc power, the 6 x 9.75″ (15 x 24.77-cm) module offers overvoltage and reverse polarity protection and is fully compatible with the Motorola EXORciser and Rockwell SYSTEM 65 and AIM 65 motherboards. **General Micro Systems, Inc,** 1320 Chaffey Ct, Ontario, CA 91762.

Circle 328 on Inquiry Card

16k static RAM card for STD BUS

STD-0016 high speed, low power memory card provides 2 modes of extended addressing capabilities. An 8-bit extended address register and selection decoder allows for user selected bank switching of 16k blocks of memory, or a program controlled 8-bit address extension for software implementation of a 24-bit address bus. Using 24-bit addressing, max memory expansion is limited only by backplane slots or 16M bytes.

The card is available in 2 versions: STD-0016 high speed (150-ns), fully populated, 16k card; and STD-0016-U without the 2114 RAM populated. Features include 16k x 8 jumper addressable static RAM, /MEMEX line for phantom feature or overlay, low power consumption, single 5-V power source, DMA capability, and optional memory diagnostic program for 8080 CPUs. Card measures 4.5 x 6.5″ (11.4 x 16.5 cm) and operates over 0 to 50 °C. **Crosspoint Systems, Inc,** PO Box 5267, Eugene, OR 97405.

Circle 329 on Inquiry Card

8″ Winchester disc drives

Scorpio family drives are available in 2 versions: model 48 with 49.7M bytes, and model 80 with 82.9M bytes of unformatted capacity and 20,160 bytes/track over 823 cylinders. Using a linear voice coil actuator in a closed-loop servo system, both versions offer avg access time of 30 ms, data transfer rate of 1.2M bytes/s, and avg latency of 8.3 ms. All critical recording components are enclosed in an environmentally sealed module to ensure long-tem reliability and data integrity. Drives provide SMD interface and require only dc power to operate. **Ampex Corp, Memory Products Div,** 200 N Nash St, El Segundo, CA 90245.

Circle 330 on Inquiry Card

EPROM programmer module

Contained on a single card that inserts into a std 4.5″ (11.4-cm) wide nest, module is designed to program the 2708 (1k x 8) EPROM and does not require a special software development system. Programs are first developed in RAM or CMOS read/write memory, and then transferred under software control to EPROM in 1k increments. Module pulses each EPROM chip 100 times/byte, with programmed information read back for verification after each pulse. Total programming time for chip burn-in is 1 min 40 s for each 1k byte of memory. A zero insertion force socket ensures reliable chip insertion and extraction. **Giddings & Lewis, Inc,** 142 Doty St, PO Box 590, Fond du Lac, WI 54935.

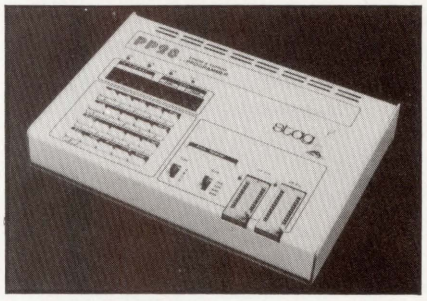
Circle 331 on Inquiry Card

5.25″ Winchester drive for personal computers

Using the Seagate Technology ST 506 drive, the David subsystem provides 5M bytes of formatted storage in a 4.75 x 5.9 x 11.25″ (12.07- x 15.0- x 28.58-cm) enclosure. The subsystem features 32-bit polynomial, 11-bit burst ECC, automatic flaw mapping and tracking, and write precompensation, and is available with host adapters for Apple and S-100 computers. Adapters will be available for the TRS-80 and Xerox personal computers in the future. Subsystem is priced at $3195, including a 90-day parts and labor warranty. **Konan Corp,** 1448 N 27th Ave, Phoenix AZ 85001.

Circle 332 on Inquiry Card

EPROM programmer

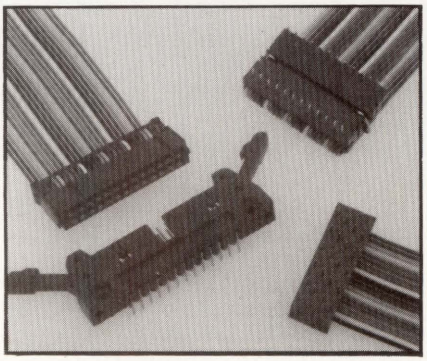


Self-contained PP28 offers a Z80 CPU, 128k bytes of RAM, 24- and 28-pin sockets, integral dc power supply, and an RS-232-C serial interface. It can be loaded from an MDS at up to 9600 baud using Intellec, Motorola, Tek-Hex, Future Data, and other std formats. Features include self-test capability, continuous short circuit and over current device monitoring, and a dual function data entry and editing keyboard. Checksum and cyclic redundancy checks are performed for complete programming integrity. **Stag Microsystems Inc,** 1120 San Antonio Rd, Palo Alto, CA 94303.

Circle 333 on Inquiry Card

INTERCONNECTION & PACKAGING

Insulation displacement connectors

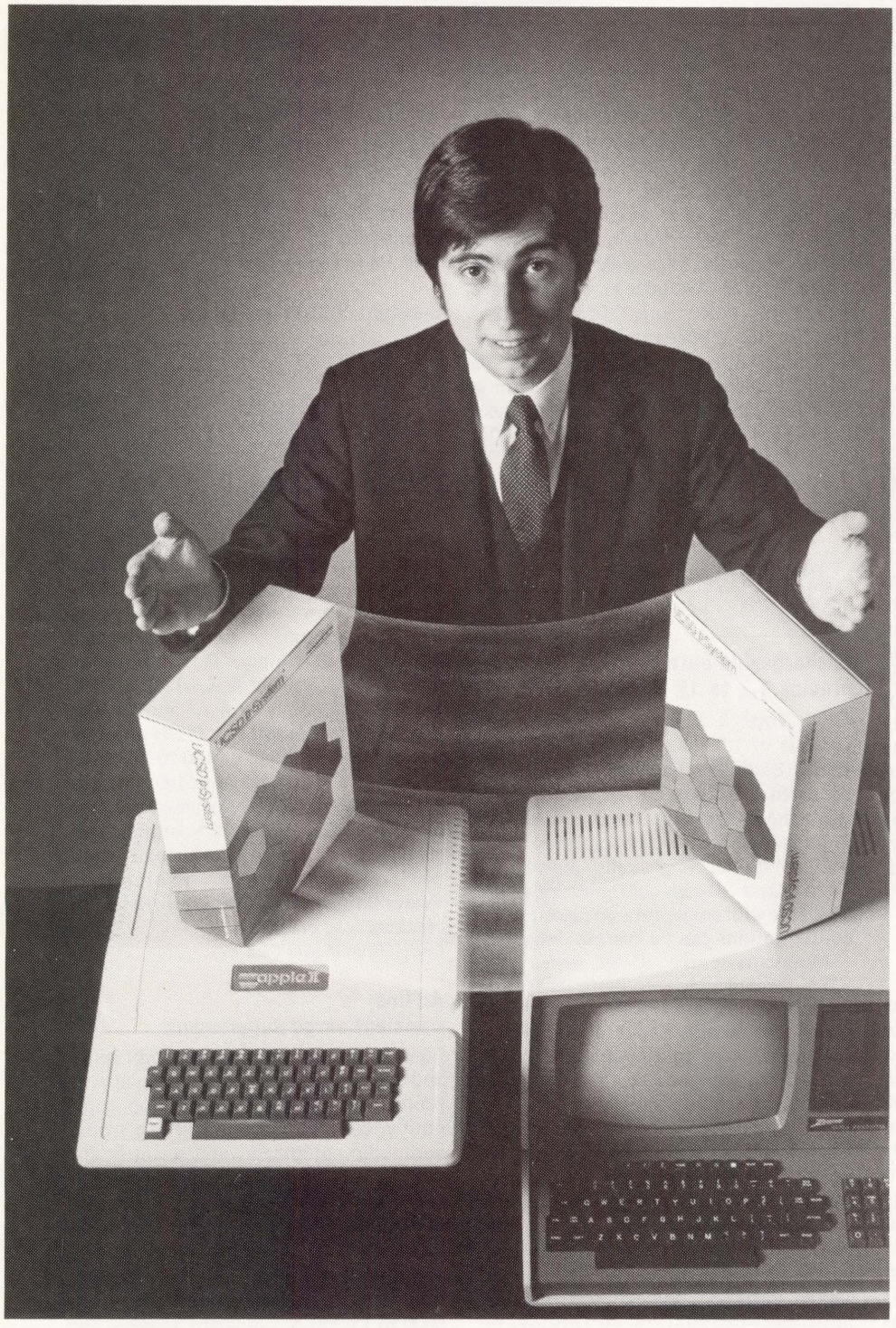


CWR-210 socket connectors are available in 10-, 20-, 26-, 34-, 40-, and 50-pin configurations with bare 725 alloy contacts, as well as tin or gold plated phosphor bronze contacts per MIL-C-83503/7. An insulated metal strain relief cover provides strain relief and protection from forces applied to the cable. CWN-300 series

(continued on page 218)

"WITH THE UCSD p-SYSTEM,™ WE CAN WRITE ONE APPLICATION THAT GOES FROM APPLE TO ZENITH."

HARRY BLAKESLEE, President, Denver Software



Our business is bigger and better than ever.

A lot of the credit for that goes to the UCSD p-System software from SofTech Microsystems. It's given us ten times the market we used to have.

We can write a single, sophisticated applications program with the UCSD p-System—like our financial management package—and it just keeps on running. On Apple, Commodore, Ohio Scientific, Texas Instruments, Zenith, and more. That's the real beauty of the UCSD p-System. Any program you write for one microcomputer runs on others, both today and tomorrow. You protect your software investment, without restricting your hardware options.

And with the UCSD p-System,you can use the language of your choice—UCSD Pascal,™ FORTRAN-77, BASIC, or assembly language. All are backed by SofTech Microsystems, a leading system software company who's been around for over a decade, who knows how to develop professional quality software, and who's committed to delivering it.

Get a head start on tomorrow. With the microcomputer software that goes from "A" to "Z." Distribution licensing and single copies available. Write or call for details, so you can start going places, too.

SOFTECH MICROSYSTEMS
A SUBSIDIARY OF SOFTECH

For the software that's going places.

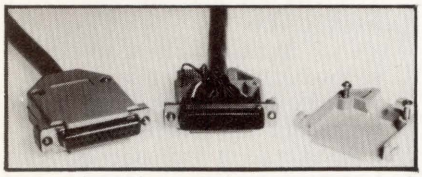
9494 Black Mountain Road, San Diego, CA 92126. (714) 578-6105
TWX: 910-335-1594

UCSD p-System and UCSD Pascal are trademarks of the Regents of the University of California.

header connectors are offered in std pin configurations matching the socket connectors, with bare 725 alloy contacts; phosphor bronze contacts with gold plating to meet MIL-C-83503/20 and /21 requirements are available. CWR-130 series DIP connectors are available in 14-, 16-, 24-, or 40-pin configurations with bare 725 alloy contacts, as well as tin or gold plated phosphor bronze contacts per MIL-C-83503/6 requirements. Strain relief is available as required. CWR-142 series PCB connectors are available in std sizes from 10 to 50 contacts. Optional strain relief and closed-end design are available, with gold plated phosphor bronze or bare 725 alloy contacts, in addition to the tin plated MIL-C-83503/23 version. **CW Industries,** 130 James Way, Southampton, PA 18966.

Circle 334 on Inquiry Card

D-subminiature connectors



M-D series crimp version connectors offer size 20 stamped and formed contacts that can be machine installed on wire sizes 28 through 20 AWG. Plug and receptacle housings are available in all std sizes. Insulator material is glass-filled nylon and UL rated 94 V-0; insulator design provides integral retaining fingers, eliminating the need for spring clips on each contact. Rear release retention system eases contact removal. Series is designed for applications requiring high density packaging. **Contact Electronics, Inc,** 30 Plymouth St, Fairfield, NJ 07006.

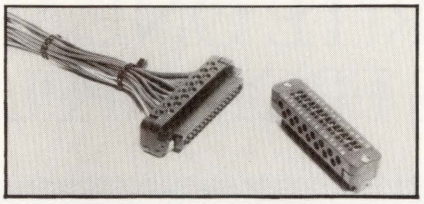
Circle 335 on Inquiry Card

Card frame and power supply

Z-Frame houses up to 16 variable speed Z9600C modems; edge connectors provide power and signals. Each modem card slot can operate independently and is connected to external devices via RS-232 and line connectors attached to the motherboard. Downed lines do not affect the operation of other modems in the frame. The family of asynchronous modems is designed for short haul operation of up to 10 mi (16 km) at speeds up to 9600 bits/s. The unit is a std 19″ (48-cm) frame, 5.25″ (13.34 cm) high. Power is 110 V/60 Hz with optional 220 V/50 Hz. **Madzar Corp,** 37490 Glenmoor Dr, Fremont, CA 94536.

Circle 336 on Inquiry Card

PCB panel mounted I/O connectors



ElectroCon series connectors permit discrete wire connections to PCBs with inline 0.156″ (0.396-cm) wire lead alignment. Included are single- and double-sided electrical and isothermal types with rear entry, and double-sided electrical and isothermal types with side entry. Available with 12 to 44 circuits, connectors accept stripped, untinned wires from 14 to 26 AWG (rear entry), and from 12 to 26 AWG (side entry). They are suited for PCBs from 0.054 to 0.071″ (0.137- to 0.180-cm) thick and are available with alphanumeric legends to identify wire contacts. Typ price for a 30-circuit, side entry, isothermal connector is $16.80 each, in quantities of 5000. **Precision Connector Designs, Inc,** 5 Lowell Ave, Winchester, MA 01890.

Circle 337 on Inquiry Card

POWER SOURCES & PROTECTION

Rechargeable batteries provide 1.2 to 12 V power

Gold Top® II high temp battery line consists of 1.2-V C_s cells and ½D- and D-size batteries. The ½D and C_s cells are rated at 2.2 and 1.2 Ah, respectively, while the D-size cell is rated at 4 Ah. All 3 units operate at temperatures from −20 to 70 °C. Single cells, plus 2-, 3-, 4-, 5-, and 10-cell configurations, are available with solder tabs or packs; other configurations can be custom designed.

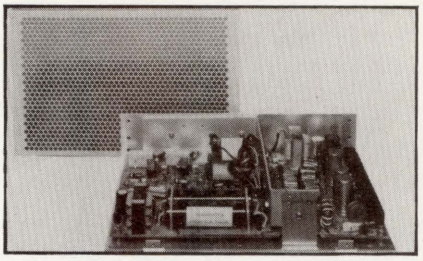
Maintenance free, 10-Ah, sealed lead, 2.0-V rechargeable SPIO batteries feature spirally wound construction of thin lead plates that permits a high discharge rate (up to 100 A of continuous, and 200 A of pulsed, operation). The batteries operate at temperatures from −20 to 60 °C and have a low discharge rate. They can be stored after full charge for up to 2 yrs at room temp and then be recharged with a constant potential or a constant current charger. To increase voltage or capacity, batteries can be connected in series or parallel. A keyed center insulator post protects against improper installation or accidental shorting.

Quick Fire™ rechargeable 12-V batteries feature low internal resistance (30 m at 20 °C) and high discharge currents (110 A pulsed or 60 A continuous). They have a low self-discharge rate and can be charged from either constant potential or constant current chargers. Op temp is −20 to 60 °C. Packaged in a rugged injection molded plastic case, batteries weigh 5.2 lb (2.34 kg). Mounting holes in the case eliminate the need for bracketing and molded-in terminal designations reduce the risk of accidental shorting.

All batteries feature maintenance-free sealed construction, allowing them to be mounted in any position and incorporated in devices containing sensitive electronic circuits. **General Electric Co, Battery Business Dept,** PO Box 992, Gainesville, FL 32602.

Circle 338 on Inquiry Card

6-output 300-W switcher



ESQ-300 series open frame switching regulated power supply provides up to 300 W of continuous output power in a semiregulated supply. Dc outputs are 5 V at 20 A, 12 V at 4 A, -12 V at 4 A, 15 V at 4 A, -15 V at 4 A, and 24 V at 4 A. Line regulation is ±0.2% at an input of 90 to 132 Vac or 180 to 264 Vac, 47 to 440 Hz. Std features include 25-kHz switching rate; overvoltage protection on the primary 5-V output; soft start, short circuit, overload, and positive brownout protection. **Power/Mate Corp,** 514 South River St, Hackensack, NJ 07601.

Circle 339 on Inquiry Card

Ac line transient surge suppressors

Four suppressor models instantly sense and suppress high voltage transients to protect microcomputers, desktop computing calculators, sensitive electronic and audio equipment, and scientific instruments. Two of these units operate in series with the ac line, while two operate in parallel. All four respond to transients in less than 25 ns. Transient energy absorption ranges from 50 to 200 J, and pk transient current protection varies from 6000 to 15,000 A. Units are designed for 120-Vac, 15-A lines and are priced from $24.95. **PMC Industries, Inc,** 1043 Santa Florencia, Solana Beach, CA 92075.

Circle 340 on Inquiry Card

Quality and delivery are two good reasons to choose Panasonic CRT data displays...

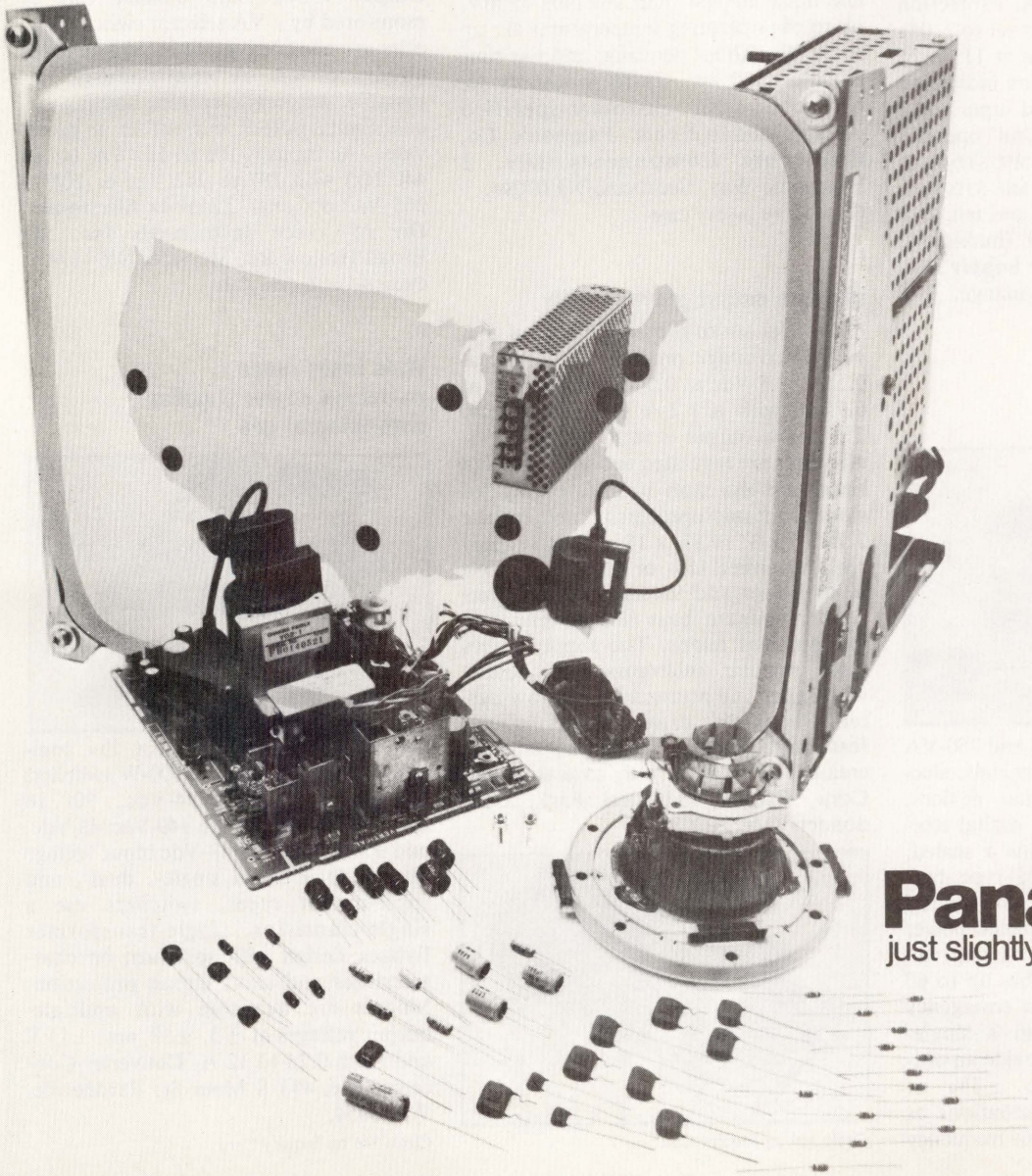
The point is, there are a lot of good reasons to choose Panasonic CRT data display modules. Like a full line of models to choose from. Quality that's built in. Delivery when promised. And a super service program that will put you in "seventh heaven".

Seven factory servicenters in the U.S. are ready to serve you – either at our facilities or on your site. Component parts for our complete line are available from our Secaucus, N.J. parts depot. And our U.S. Applications and Design Lab is fully equipped to help you with applications, design, testing, troubleshooting and problem solving.

The complete Panasonic line of CRT Data Displays includes high resolution color modules for fine line graphics. A 600-line vertical page reader. And a wide variety of other top-quality color and monochrome CRT chassis assemblies, to give you far-ranging design flexibility.

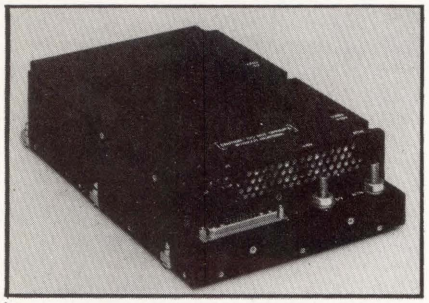
Need any more reasons to choose Panasonic? Then call one of our Application Engineers – he's got plenty more to convince you. Or write for additional data: Panasonic Company, Data Display Dept., Industrial Sales Division, One Panasonic Way, Secaucus, NJ 07094; phone (201) 348-5385.

7 servicenters make 7 more.



Panasonic®
just slightly ahead of our time

Military power supply



SP7911 has 4-W/in³ (0.244/cm³) capacity and complies with MIL-E-16400. Output voltage is 5.25 V (adjustable ±5%) at 100 A and 15 V (adjustable ±5%) at 14 A. Regulation is ±0.3% for all combinations of line and load. Output ripple is 70 mV pk-pk. Efficiency is 75% min with a load variation of 10% to full load. Input voltage range is 95 to 130 Vrms, 47 to 440 Hz, 30 A. Protection features include overcurrent set to 110% of max output, overvoltage at 115% of max output, overtemperature indication for optional shutdown, and input surge current limit of 15 A. Unit operates from 0 to 65 °C and meets MIL-STD-810C, method 514 (vibration); MIL-STD-810C, method 516, proc I (shock); and MIL-STD-810C, method 507, proc IV (humidity). **CEAG Electric Corp, Power Supply Div,** 1324 Motor Pkwy, Hauppauge, NY 11787.

Circle 341 on Inquiry Card

Portable, plug-in UPS

Mini UPS is available in 400- and 750-VA models for use with pos terminals, electronic lab monitors and test devices, microcomputers, and other digital electronics devices, and contains a sealed, maintenance free, lead-acid type battery. In blackout situations, both models provide up to 20 min of regulated power at full load from battery backup; an auxiliary battery pack supplies up to 60 min of additional regulated emergency power. Units operate from a single-phase 115-Vac input and provide an output voltage regulated to ±3% of nominal through input fluctuations as great as 10% to −20%. Input frequency fluctuations of up to ±10% of nominal (60 Hz) are regulated at output to ±0.5 Hz (one-half cycle). The device also attenuates electrical noise and limits output harmonic distortion to less than 5% total Vrms. **Sola Electric, a Unit of General Signal,** 1717 Busse Rd, Elk Grove Village, IL 60007.

Circle 342 on Inquiry Card

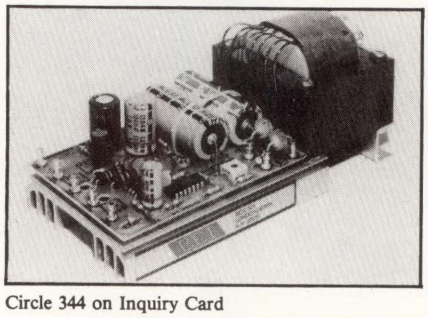
200-W switching power supplies

Lightweight MG series supplies measure 15 x 2.56 x 5.12″ (38 x 6.5 x 13 cm) and feature 75% efficiency, wide input line variations (15 to −26%), modular construction, overvoltage and short circuit protection, 50-kHz operation, and 40-A inrush current. Dropout (or holdup) time is over 20 ms; differential ripple and noise are less than 1% plus 75 mV, pk to pk; operating temperatures are up to 50 °C without derating; and rise time is within 100 ms. Up to 6 outputs are provided with customer-specified voltages and currents. **Panasonic Co, Electronic Components Div,** 1 Panasonic Way, Secaucus, NJ 07094.

Circle 343 on Inquiry Card

Multiple output power supply

CEI model MP400 provides 5 Vdc at 5 A with overvoltage protection, 12 Vdc at 0.5 A, −5 Vdc at 0.5 A, and 24 Vdc at 0.75 A with a 1.2-A surge capability. The 5-Vdc output is regulated to 0.1%; all others are regulated to 5%. Noise and ripple are less than 10 mV. Fitting std slope front microprocessor cabinets, the 3.75 x 7 x 3″ (9.53- x 18- x 8-cm) supply requires either 115- or 230-Vac ±10% input power and incorporates an oversized aluminum heat sink to maintain low ambient temps. The supply drives most popular microprocessor boards with small line printers and/or low current floppy disc drives. Model MP400P, featuring onboard connectors and increased outputs, is also available. **CEI Corp,** Grenier Industrial Park, Londonderry, NH 03053.



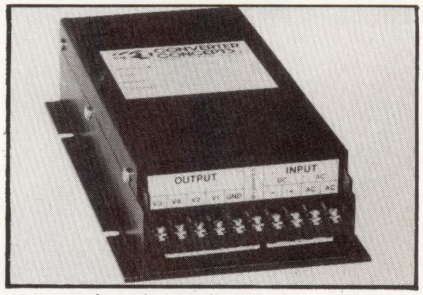
Circle 344 on Inquiry Card

Power supplies

LQ series supplies use monolithic, multifunction voltage regulators with built in onchip temp regulation to provide 0.005% regulation, 150-μV rms ripple, and 0.005%/°C temp coefficient. The 5-yr guaranteed supplies are available in 5 models with voltages of 0 to 120 V and current ratings up to 14 A. All units are convection cooled and require no fans or blowers. Digital meter readout is std. Output voltage and current can be monitored by a VA selector switch. Supplies are completely protected and short circuit proof. A continuously adjustable, automatic current limiting circuit limits output current to a preset value. Ac input is 105 to 132 Vac (47 to 440 Hz) with 187 to 242 Vac or 205 to 265 Vac optional. **Lambda Electronics, Div of Veeco Instruments Inc,** 515 Broad Hollow Rd, Melville, NY 11747.

Circle 345 on Inquiry Card

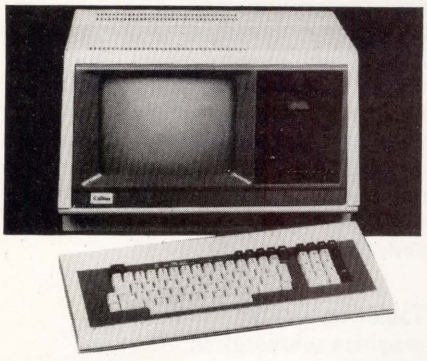
Wide input range switching power supplies with integral UPS



UPS option is available for the company's 25-, 50-, 75-, and 100-W switchers in 90- to 140-Vac/24-Vdc, 90- to 250-Vac/24-Vdc, 90- to 140-Vac/48-Vdc, and 90- to 250-Vac/48-Vdc input voltage ranges. Offered in single-, dual-, and triple-output types, switchers use a single-transistor, single-transformer flyback design with soft turn on characteristics and short circuit protection. Models are available with multiple-output voltages of ±5, ±12, and ±15 V and from 0.25 to 12 A. **Converter Concepts, Inc,** 435 S Main St, Pardeeville, WI 53954.

Circle 346 on Inquiry Card

MULTIBUS compatible integrated workstation



Model CD100M offers a 5.25″ (13.34-cm), 5M-byte Seagate Technology Winchester disc; a 604k-byte, 96-track/in (38/cm) Tandon minifloppy disc; Z80A CPU; 64k-byte dynamic memory; and CP/M operating system. Housed in a single desktop cabinet, the system features 25-line x 80-char display with variable split screen capability and scrolling areas in both partitions, 7 x 12 individual char matrix for high resolution, ANSI command capability, full editing capability, and 6 individual char attributes with invisible control commands for customized display presentations. Communication is via an RS-232-C interface at 9600 baud. **Callan Data Systems, Inc,** 2637 Townsgate Rd, Westlake Village, CA 91361.

Circle 347 on Inquiry Card

Generic PC board adds graphics capability to many alphanumeric terminals

A generic package designed to convert alphanumeric displays into terminals with graphic functions while retaining all of their original functions, model RG1000 consists of a PC board, complete with controlling microprocessor and RAM. It allows users to emulate the Tektronix 4010 series including creation of simple point plots to curves and complex mapping. Depending on the resolution of the host terminal, resolutions of 640 x 240, 720 x 272, or 800 x 300 are offered. A retrofitted terminal is also compatible with ISSCO's DISSPLA and TELLAGRAF and Tektronix' PLOT 10 software systems. Other features include fill, selective erase, enhanced text mode, and an interactive cross-hair cursor. Also, the system is designed with two graphics bit planes which allow multiple intensity levels or multiple graphics pages. An optional lightpen allows the direct transmission of X-Y coordinates. **Digital Engineering, Inc,** 630 Bercut Dr, Sacramento, CA 95814.

Circle 348 on Inquiry Card

Non-expandable video terminals

VT101 entry level terminal provides basic VT100 functions such as keyboard-command parametric setups, plus local echo for use with computer systems that have no ability to echo back a character from the host. VT102 offers all VT101 functions plus an advanced video option and printer port as std features. The video option provides 24 lines of 132-col display, 4 char attributes (blink, bold, video reverse, and underline), and provisions for user installable char sets. Terminal also has true half- and full-duplex communications capabilities. VT131 offers all features of the VT102, plus local editing capabilities, and adds features for computer systems employing asynchronous block mode transmission. When used on the company's computer systems that do not employ block mode transmission, VT131 can be set to operate with a VT102. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 349 on Inquiry Card

300- and 600-line/min impact printers

Offered for the PTS-2000 intelligent terminal system, printers produce 132-col printouts on single- through 6-part forms. Each printer uses a 9 x 9 dot char matrix to overlap dots both vertically and horizontally, producing solid appearing chars that are OCR readable. They provide both ASCII and EBCDIC char sets (full 96-char sets of upper/lowercase chars with true descenders). Printers measure 16.5 x 30 x 24″ (41.9- x 76- x 61-cm) and weigh 185 lb (84 kg). An acoustic cabinet reduces noise to less than 60 dbA. **Raytheon Data Systems Co,** 1415 Boston-Providence Tpk, Norwood, MA 02062.

Circle 350 on Inquiry Card

Handheld 2-way data entry terminal

Data Prompter™ DP 2002 enters, stores, and transmits product, service, and resource information from any location. Without a modem or external coupler, alphanumeric data can be sent and received via telephone, radio, microwave, or satellite between any 2 locations, to and from a central data base or an existing computer system, and from one data terminal to another within the same system. Terminals require minimal training to operate and are programmed to prompt data entry and to monitor entries for errors. **Pinetree Systems, Inc,** 734 Greenview Dr, Grand Prairie, TX 75050.

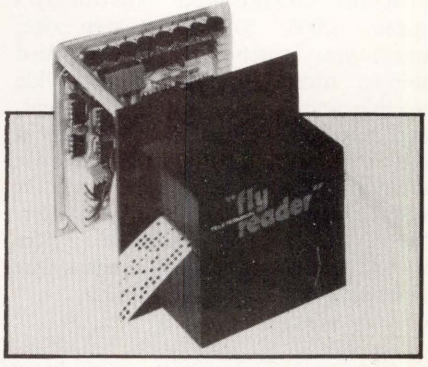
Circle 351 on Inquiry Card

Dot matrix graphic printer

VIC 1515 prints any of the alphanumeric and graphic symbols common to the VIC 20 personal computer at 30 char/s, allowing VIC 20 users to create hard copy for forms, program listings, mailing labels, charts, graphs, etc. Enhancements allow the printer to produce extra-wide and reversed (negative) characters as well. Single quantity price is $395. **Commodore Business Machines, Inc, Computer Systems Div,** 681 Moore Rd, King of Prussia, PA 19406.

Circle 352 on Inquiry Card

300-char/s paper tape reader



Fly Reader III bidirectional tape reader handles any 8-level, 1″ (2.54-cm) tape per ANSI X3.18, EIARS-227, or ECMA 10 standards. Any tape material, including mylar, paper, or oiled paper with transmissivity up to 60%, can be read without adjustment. Unit requires a single 5-V, 2-A power supply and employs a stepper motor tape drive and precision fiber optic light distribution system. It is available with or without an electronics board which provides a TTL interface along with motor control and output data conditioning. **Teleterminal Corp,** 390 Portsmouth Ave, Greenland, NH 03840.

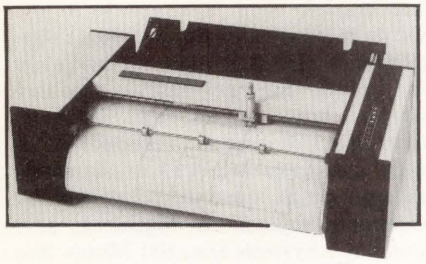
Circle 353 on Inquiry Card

Smart ASCII video display terminal

D2100 features molded plastic case, high resolution 12″ (30-cm) monitor, 24-line x 80-char display format, and optional tilt and swivel base. Typewriter-style keyboard with integral numeric keypad is std; optional layouts are available to meet specific requirements. Terminal is configured with RS-232 communications and printer interfaces with data transmitted asynchronously at up to 9600 bits/s (TTY block mode). Terminal software supports data entry and editing, including typewriter-style tabbing, forms creation, and data insertion/deletion on a char by char or line basis. **Delta Data Systems Corp,** 2595 Metropolitan Dr, Trevose, PA 19047.

Circle 354 on Inquiry Card

22″ plotter



Available in 3 intelligence configurations with 5 different interface capabilities, CPS-30 interfaces with most computers. Features include 400″ (1016-cm)/s speed, 0.005″ (0.013-cm) step size, touch-type switches, fully dampened stepper motors designed to provide reliable and quiet 8-vector movement, and rugged construction for use in adverse conditions. Plotter also allows the user to change or upgrade computer systems without replacing the plotter. Metric versions are available. Prices start at $6400. **Houston Instrument,** One Houston Sq, Austin, TX 78753.

Circle 355 on Inquiry Card

Microprocessor based, intelligent daisywheel printer features drop-in plastic printwheels

Model 620 desktop printer, operating at print speeds of up to 25 chars/s, offers drop-in plastic printwheels with automatic ribbon and printwheel positioning sensors. Printer also features a long life ribbon cartridge system designed to remain in place during printwheel changes, a 512-char buffer, correspondence quality output, and a stepper motor design that provides subscript, superscript, and bidirectional printing capabilities. It incorporates 5 modular assemblies designed to enhance diagnostic procedures and repair routines: printer mechanism, control panel, power supply, 2-bolt cover design that facilitates access to the printer's internal components, and a PCB that contains two 8-bit microprocessors.

Drop-in printwheels reduce the amount of operator training required for printer operation. Printwheel alignment is achieved by an intelligent encoding system that electronically positions the wheel after it has been inserted loosely into an envelope-like opening; there are no notches, hubs, or alignment requirements. The system notifies users if they attempt to use a proportionally spaced printwheel for an output task requiring a 15-pitch printwheel; at the same time, the system adjusts its printing method to match the ribbon being used. Up to 132 chars can be printed horizontally in a single column using 10-pitch printwheels.

Available in both U.S. and European configurations, the printer operates at or below the 66-dBA range and meets safety standards of UL, CSA, and VDE 0730. It also meets VDE 0804 and 0871, and FCC Class B requirements. **Diablo Systems Inc, a Xerox Co,** 24500 Industrial Blvd, Hayward, CA 94545.

Circle 356 on Inquiry Card

High speed color copier for computer graphics

ACT-1 creates plain paper copies of color images displayed on computer graphics terminals. Unit uses an ink jet printing technique to produce multicolor images on paper in less than 2 min for an 8.5 x 11″ (21.6 x 28-cm) print. It can print copies up to 12.5″ (31.8-cm) wide by any desired length. No special training is required for operation. Copier is priced at $9000. **Advanced Color Technology, Inc,** 187 Billerica Rd, Chelmsford, MA 01824.

Circle 357 on Inquiry Card

30-char/s letter quality printer

Microprocessor controlled model 9611, connected to any of the company's processors with a serial interface, functions as a local printer in either a standalone configuration or as part of the Attached Resource Computer (ARC) local network system. It also functions as a terminal printer when connected to the company's 8200 video workstation. Line width and spacing, form length, and print pitch are user specifiable. Power required is 120 Vac at 50 or 60 Hz. The printer is priced at $3990. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284.

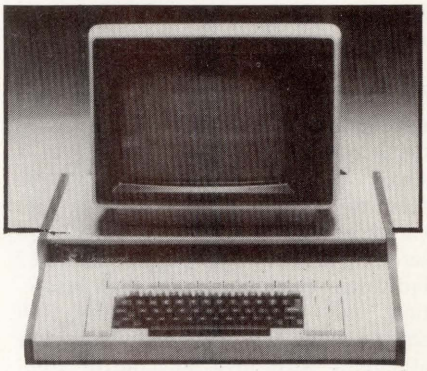
Circle 358 on Inquiry Card

Color graphic display systems

Raster 640 and 320 full-featured desktop terminals offer high resolution raster scan and pixel addressable color graphics. The systems communicate with host computers via a std RS-232-C interface and offer resolutions of 640 x 256 and 320 x 256 pixels, respectively. A std parallel ASCII printer interface is supplied along with an RS-170 interface for RGB video monitor or hardcopy device. Three refresh memory planes permit simultaneous display of up to 8 colors for foreground and 8 colors for background. Software allows user to draw lines, vectors, circles, and rectangles, and up to 256 user defined symbols can be stored in P/ROMs. Additional interface, color monitors, interactive devices, and software packages are optional. **Phoenix Computer Systems, Inc,** 119 Board Rd, Lafayette, LA 70505.

Circle 359 on Inquiry Card

Tablet option for graphics workstation



Designed for the CC-80 graphics workstation, cursor control tablet permits the operator to switch cursor control back and forth from the tablet to the joystick or thumbwheels already provided on the console. Packaged on a portable, wedge shaped board, the tablet can be located anywhere on the work table. Simulated keys are activated with the stylus as if the operator had depressed a key on the actual keyboard. An 11 x 11″ (28- x 28-cm) work area is located below the silkscreened area that contains menu function keyboard. **Auto-trol Technology Corp,** 12500 N Washington St, Denver, CO 80233.

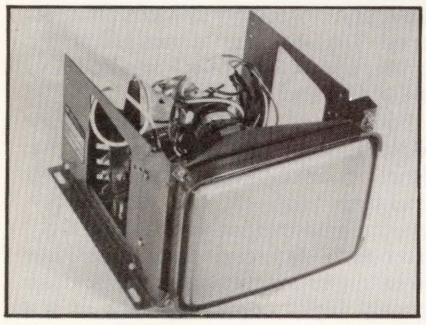
Circle 360 on Inquiry Card

Desktop digitizer

Bit Pad 10 features CRT cursor position control, graphic command menu input, and free sketch input. Intended for use with small business or personal computers, or where large surface tablets are not required, the device provides increased operator comfort in applications where long periods of time are spent digitizing. It offers an 11″ (28-cm) sq active surface; height is 0.49″ (1.24 cm) at the front and 2.78″ (7.06 cm) at the rear, with an 8° slope. RS-232, IEEE, and 8-bit parallel interfaces permit the unit to transmit digitized data directly into data processing system. **Summagraphics Corp,** 35 Brentwood Ave, Fairfield, CT 06430.

Circle 361 on Inquiry Card

CRT data displays



BHD-700 series monitors have optimized corner focus, resolution, bandwidth, and geometric characteristics. All deflection and video processing electronics are located on a single plug-in PCB, and all circuit boards are pin for pin compatible with std data display video input connectors. CRT alignment, centering, tilt angle, and mounting points meet current industry standards. Series is designed for std TTL level input, and handles composite video input signals with added circuit module. Displays are available in several configurations, including a std chassis version and kit form, or built to custom specifications. Options include a separate power supply, selected horizontal scan frequency (15,750 to 21,000 Hz), and several phosphor types. **Dotronix, Inc,** 160 First St SE, New Brighton, MN 55112. Circle 362 on Inquiry Card

20-col alphanumeric thermal printer

Model MAP-20P features a 96-char print set, print rate of 2 lines/s, internal self-test program of all chars and printing modes, and complete microprocessor electronics and ac power supply. It accepts 8-bit TTL parallel input data at rates up to 2000 chars/s. Included in the standalone package are programmable controls for text or lister printing, and normal or extended char size. Unit measures 4.5 x 2.8 x 7.0″ (11.4 x 1.1 x 17.8 cm) and weighs 4.2 lb (1.9 kg). Single-unit price is $625. **Memodyne Corp,** 220 Reservoir St, Needham Heights, MA 02194.

Circle 363 on Inquiry Card

136-col enhancement for 80-col data terminals

TXP 136 enhancement upgrades any std 80-col TI 743 or 745 into a 136-col data terminal, providing 70% more data in the same space. A full 5 x 7 matrix is used in both operating modes, providing char densities of 10 and 18 chars/in (4 and 7/cm). The unit requires only replacement of socketed microprocessor with a small PCB and changing the motor pulley and cable. It is approved by Texas Instruments for installation in TI 743 and 745 data terminals, without affecting the warranty of the Silent 700® terminal. Nationwide field service support is provided by Texas Instruments. The enhancement is available in tested kit form for $375, or installed in the user's TI 743 or 745 for $495. **Texprint, Inc,** 8 Blanchard Rd, Burlington, MA 01803.

Circle 364 on Inquiry Card

INTERFACE

64-bit, jumper programmable, digital I/O card

Model 1664ATTL operates as an I/O interface to DEC LSI-11 series computers and has 8 registers that can be jumper programmed to operate as input ports, output ports, or mixed I/O ports. When programmed to operate as an input, the associated port will accept data from digital devices such as voltmeters, bit switches, and keyboards; programmed as an output, the associated port will drive devices such as printers and CRTs. Once the program jumpers are configured, the 8 independently controlled 8-bit registers operate directly under software program control. All output latches can be set, or reset, upon power-up initialization. Latching registers provide high noise immunity against logic level changes. The ½ quad size board plugs directly into the LSI-11 backplane and derives its power from the host computer's 5-V logic supply. **ADAC Corp,** 70 Tower Office Pk, Woburn, MA 01801.

Circle 365 on Inquiry Card

Enhanced programmable communications interface device

SY2661 dedicated peripheral controller performs synchronous and asynchronous protocols simultaneously. Offered in a 28-pin ceramic or plastic DIP, it operates from a single 5-V power supply, has TTL compatible inputs and outputs, and is available in 3 baud rate ranges. Model SY2661-1 conforms to European specs, while model SY2661-2 incorporates a new domestic design. Model SY2661-3 is a direct replacement for the Signetics 2651. The devices are designed for applications in network and frontend processors, computers and computer links, intelligent terminals, peripherals, and bisync adapters. **Synertek,** 3001 Stender Way, Santa Clara, CA 95051.

Circle 366 on Inquiry Card

IEEE 488 bus controller/computer system

Based on a 4-layer, single-board GPIB controller that features 2 independent GPIB ports, each with a bus transfer rate in excess of 14k bytes/s, model 48 includes an RS-232 serial port, 2 parallel data ports, and a built-in 12″ (30-cm) CRT with a full 80- x 24-char display. Up to 132 col of hard copy are provided by an optional impact dot matrix printer. System contains 64k bytes of internal memory; an additional 350k bytes of mass storage is supplied by a 5.25″ (13.34-cm) floppy disc drive. The controller contains Z80 and 8085 microprocessors and is supplied with the CP/M operating system, text editor, assembler, and debug software. **Systel Computers, Inc,** 538 Oakmead Pkwy, Sunnyvale, CA 94086. Circle 367 on Inquiry Card

DEC compatible controller for 5.25″ mini-floppy disc drives

DSD 4120 emulates DEC RX02 subsystems, making high capacity 5.25″ (13.34-cm) drives appear to the computer as single-sided 8″ (20-cm) floppy drives. It executes unmodified DEC RX02 software and is totally compatible with DEC RT-11 V3B, RT-11 V4, and RSX-11M operating systems. Packaged on a single dual-wide card, the controller supports up to two 5.25″ mini-floppy disc drives providing 1.2M bytes of formatted storage capacity. Shugart Associates' SA460 and Tandon's T-100-4 drives are also supported. An on-board 6-MHz bit slice processor controls the disc drives and all data transfer functions. **Data Systems Design, Inc,** 2241 Lundy Ave, San Jose, CA 95131.

Circle 368 on Inquiry Card

Programmable controller offered for small relay replacement applications

Solid state Micro-84 allows users to control small machine operations requiring 4 to 60 relays. The device has a free formatted multinode programming format, with programming in relay symbology. In addition to relay functions, it provides internal timers; counters; and arithmetic, drum, and sequencer functions. The controller can be programmed using the P190 multifamily CRT programming panel or the company's handheld/tabletop LCD programming panel.

Features include search functions, disable/enable force functions, user-defined keys, supervisory functions for start/stop, load/dump memory, clear memory, error code display, arithmetic capability for value addition and subtraction, and full register capacity. EAROM addresses up to 64 I/O points, any combination in groups of 8. The device's program pack consists of removable EAROM storage media that can be used for program loading and storage, recipe storage, and similar operations.

Element reference numbers and network and data status are accessible on the programming panel. Power flow direction is indicated as well. User oriented status keys ease the programming process. I/O modules are available for 115- and 220-Vac, and 24-Vdc signals. Inputs are optically isolated, have load side indicators, and accommodate 2- to 14-AWG wires. Typ scan time is 25 to 40 ms. Op temp is 0 to 60 °C. The basic controller (without programmer and removable memory pack) is priced at $500. **Gould Inc, Modicon Div,** 1280 E Big Beaver Rd, Suite B, Troy, MI 48084.

Circle 369 on Inquiry Card

User programmable process control and monitoring system

MBL-500 digital sensor indicator/controller features programmable engineering units and RS-232-C/20-mA communications capability. Providing excitation from 0 to 25 V and accepting most sensor inputs directly, including strain gage (load cell), the microcomputer based system performs a variety of tasks from standalone measure/command jobs to distributed intelligence, process control functions. Features include user programmable scaling factors and limit alarms, interval timer, 24-h clock, optional event counter, and 5-digit LED display with floating decimal. Programmable data are entered through the serial I/O port or optional local keyboard. System measures 5.5 x 2.5 x 6.75″ (14.0 x 6.4 x 17.15 cm) and is priced from $495. **M.B. Laboratories, Inc,** 50 Moraine St, Belmont, MA 02178.

Circle 370 on Inquiry Card

MICROPROCESSORS/ MICROCOMPUTERS

Bipolar, 16-bit microprocessor is offered for military and high performance applications

SBP9989 second generation IIL microprocessor has a throughput more than twice that of the first generation SBP9900A. Fabricated using military std processing (MIL-STD-833B, method 5004, 100%), the device operates over a temp range of −55 to 125 °C; it will operate in radioactive environments and use virtually any power supply capable of supplying the desired current at injector voltage. Features include a 4.4-MHz clock rate (single-phase, 50% duty cycle) and the ability to directly access up to 132k bytes of memory. Used with the SN54LS610 memory mapper peripheral chip, the processor can directly access up to 16M bytes of memory.

The processor incorporates the company's memory to memory architecture, providing 4.5-μs context switching and a virtually unlimited number of registers. Interrupt and I/O handling capabilities include 16 prioritized hardware interrupts and 16 software interrupts, plus serial I/O via the communications register unit. Parallel I/O is handled via a 16-bit data and address bus.

Four new instructions have been added to the first generation SBP9900A: signed multiply, signed divide, load workspace pointer, and load status register. Improved microcoding and the processor's fast clock rate enable the processor to execute instructions at extremely high speed; operating at 4.4 MHz, the ALU performs a 16-bit signed multiply to obtain a 32-bit signed product in 7.3μs.

Power required is 400 mA (±5%) and typ power dissipation is 500 mW. Device is provided in a std 64-pin DIP and is priced at $489.70 each in 100-piece quantities. **Texas Instruments Inc,** PO Box 202129, Dallas, TX 75220.

Circle 371 on Inquiry Card

Personal computer uses TV for display and tape cassette recorder for program storage

Based on a 4-chip design, the portable ZX81 personal computer measures 6 x 6.5 x 1.5″ (15 x 16.5 x 3.8 cm), weighs 12 oz (340 g), and utilizes a std home TV for display and any conventional home cassette recorder for program storage. The system provides all the important features of the ZX80 computer, including single-stroke key word entry, edit facilities, automatic syntax checking of every statement line, and a 24-line x 32-char display. A master chip replaces 18 chips in the ZX80 and adds new cir-

cuitry. New features include the ability to operate in 2 software selectable modes, fast and normal; fast is four times the speed of normal. In the normal mode, the computer will both compute and display simultaneously, allowing continously moving, flicker-free graphics.

(continued on page 225)

A 40-key, touch sensitive membrane provides the equivalent of 91 keys using function mode and single-press key word system. Graphics mode enables an additional 20 graphics and 54 inverse video characters to be entered directly from the keyboard. The graphics display can also be divided into 64 x 44 pixels, each of which can be blacked in using PLOT and whited out using UNPLOT under program control.

An 8k BASIC ROM allows the system to operate in decimal arithmetic with full scientific functions. Numbers are stored in 5 bytes in floating point binary form, providing a range of $\pm 3 \times 10^{-39}$ to $\pm 7 \times 10^{38}$, accurate to 9.5 decimal digits. The computer features full log, trig, and their inverse functions, and handles multidimensional numerical and string arrays. A comprehensive, 164-p instruction manual is provided with the system and includes a course in BASIC programming. The computer is priced at $149.95; it is available in kit form for $99.95. **Sinclair Research Ltd,** 2 Sinclair Plaza, Nashua, NH 03061.

Circle 372 on Inquiry Card

Expandable microcomputer system

Pronto 2818, contained in a 26 x 18 x 20″ (66- x 46- x 51-cm) cabinet, is suited for deskside use as a basic single station with 1M byte of storage. System can also be expanded to a multistation system with hard disc storage in excess of 50M bytes. It holds up to two 8″ (20-cm) floppy disc drives plus one 8″ rigid disc drive; or one 8″ floppy disc, one 8″ rigid disc, and streamer tape backup. The system's CVT type flexible power supply accommodates changing input and output voltage requirements, std 110/220 Vac, 50/60 Hz. Its IEEE std motherboard accommodates up to 18 PC cards and features gold plated card edge connections. The unit also includes a double-pole circuit breaker, a dual ac convenience outlet mounted on the rear of the cabinet, a double-bit on/off key switch, and a power-on indicator and reset. **Para Dynamics Corp,** 7740 E Redfield Rd, Scottsdale, AZ 85260.

Circle 373 on Inquiry Card

Single-board, Z80A based microcomputer features dynamic memory controller chip

MLZ-92A features the Texas Instruments TMS-4500 dynamic memory controller chip that combines DRAM timing, refresh counter, and address multiplexing functions on a single 40-pin device. The chip connects directly to the CPU address bus and is supplied with an 8-MHz clock signal. CPU provides the Z80 instruction set and vectored interrupt capability. An onboard jumper allows system clock frequency to be reduced to 2 MHz for system debugging.

Two ROM sockets accommodate Intel 2716, 2732 or 2764 EPROMs. The onboard 64k DRAM has a parity bit for error detection and runs at full processor speeds with no wait states. Onboard programmable DMA offers Z80 compatible I/O and memory data transfers, multimode operation, and memory to memory, memory to port, port to memory, and port to port transfers.

The microcomputer is compatible with the expanded 20-bit MULTIBUS. A programmable address mapping RAM puts memory map under software control, allowing full use of the 20-bit address space on the bus. A bus mapping feature defines the address block that the board occupies on the MULTIBUS. Onboard I/O devices can be moved to different I/O base address or turned off completely under software control.

Four serial ports support both synchronous and asynchronous communication and are supplied with dual baud rate generator and crystal. Baud rates are selectable from 50 to 19.2k baud. Two ports can be configured for RS-232 or RS-422. Four independent counter/timer channels and power-on jump are also included. Options include APU, floppy disc drive, Winchester interface, streamer tape/Centronics compatible parallel port, DIP switches, and LEDs. Single unit, with 64k of RAM, is priced at $2789. **Heurikon Corp,** 3001 Latham Dr, Madison, WI 53713.

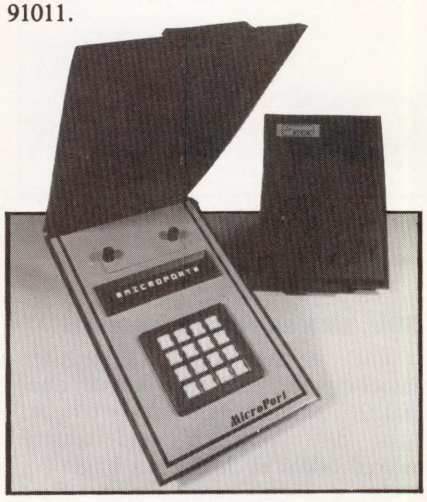
Circle 374 on Inquiry Card

Handheld CMOS microcomputer system offers flexibility, adaptability

Microport handheld CMOS microcomputer system utilizes the NSC-800 CPU with an 8080, 8085, and Z80 compatible instruction set; a companion NSC-810 provides 2 counter-timer channels and 14 available parallel I/O ports. Two I/O ports are wired to transistors for bidirectional serial I/O. RAM and ROM are organized around 3 memory sockets. The system is provided with a 2k monitor and 2k CMOS RAM in two 24-pin sockets. A 28-pin socket provides program memory space; ROM size of up to 8k (2764) can be used in this position. This memory is located in a zero insertion force socket behind a removable access door on the front panel. A separate board area is provided for system expansion and interface circuitry; it accommodates board sizes up to 4.1 x 3.6″ (10.4 x 9.1 cm).

A 12-digit alphanumeric display has an onboard 60-s timer circuit for power save blanking. Char height is 0.11″ (0.28 cm) std, or 0.16″ (0.41 cm) optional. The 16-position keyboard has removable keycaps, allowing the keyboard to be tailored to specific applications. Case size is 1.5 x 5 x 7.7″ (3.8 x 13 x 19.6 cm). On the front panel is a small area available for special controls; on the rear, a switch and connector area provide external access.

A debug and utility monitor aids in implementation of the user's software. Routines include execute program, memory change, register examine, breakpoints, keyboard scan, and serial memory download/upload. The system runs with 6 AA cells. Avg continuous usage life is 24 to 36 h. **MDE Electronics,** 4726 Daleridge Rd, La Canada, CA 91011.



Circle 375 on Inquiry Card

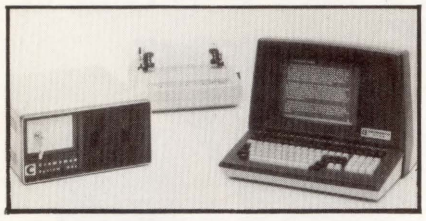
High speed, 16-bit microprocessor

A 10-MHz version of the Z8000™, Z8000B is offered in segmented and nonsegmented versions. The 48-pin segmented Z8001B allows the user to address up to 32M bytes of memory for highly memory-intensive applications and systems requiring very high throughput. Used with the company's Z8010 memory management unit, it offers a memory addressing range of up to 48M bytes. The 40-pin nonsegmented Z8002B has a 256k-byte memory addressing range and is suited to less memory intensive applications. **Zilog, Inc,** 10340 Bubb Rd, Cupertino, CA 95014.

Circle 376 on Inquiry Card

Desktop microcomputer

Designed for single- or multi-user applications, System One includes a Z80A based CPU, 64k of RAM, printer interface, and dual quad-capacity 5″ (13-cm) floppy disc drives that offer 780k bytes of storage capacity. An 8-slot card cage provides room for expansion, allowing the system to be configured for specific requirements by adding memory and I/O cards. The computer provides system diagnostics and operates with user-selectable 110/220-V, 50/60-Hz power. In addition to business oriented, end user software, available software includes Structured BASIC, FORTRAN, COBOL, C, RATFOR, and LISP; a choice of operating systems is provided, including the company's CROMIX™ multi-user, multitasking operating system. System is priced at $3995. **Cromemco, Inc,** 280 Bernardo Ave, Mountain View, CA 94043.



Circle 377 on Inquiry Card

4-MHz, Z80A based microcomputer

Episode, a standalone, single-user microcomputer, provides 64k RAM, dual serial I/O, parallel Centronics interface, floppy disc controller, and battery powered calendar clock on a single 6 x 8″ (15- x 20-cm) card. System offers storage capacities of up to 1.6M bytes on dual 5.25″ (13.34-cm) floppy disc drives and is designed to interface with a variety of peripherals. Features include curly phone cord connections to the console and printer, fully internal diagnostic test circuitry, and modem interface. Base price of $2550 includes CP/M operating system and Supervyz software system. **Epic Computer Corp,** 7542 Trade St, San Diego, CA 92121.

Circle 378 on Inquiry Card

Single-board microcomputer

DSZ-80 features a 4-MHz Z80 CPU and provides an 80 x 25 CRT controller, Centronics printer interface, keyboard interface, and an asynchronous/synchronous RS-232 communications channel onboard. Memory array consists of 64k bytes of dynamic RAM and 2k bytes of 2716, or 4k bytes of 2732 bootstrap P/ROM. A 2k-byte global memory is provided for interprocessor communication in a distributed multiprocessor system architecture. Memory address space is 1M byte. The system is fully compatible with MP/M and CP/M 2.2. **Dynamic Structured Systems,** 8 Murray Dr, Westbury, NY 11590.

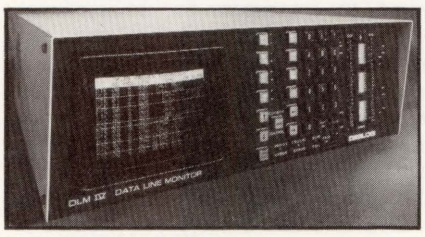
Circle 379 on Inquiry Card

TEST & MEASUREMENT

Interactive data line monitor offers X.25 frame and packet level analysis

DLM IV data line monitor facilitates quick fault analysis on private, dial, and packet switched lines. It features X.25 HDLC and X.25 BSC to level 3, menu guided setup, 1024-char output buffer, counters and timers, bit protocol orientation, match under mask, start/stop trap on bit/byte, 12k-byte data storage, 9 codes std plus 1 optional, EIA breakout box, built-in 511 BERT, clear text and hexadecimal printer output, and binary breakout of any char on the 16- x 32-char CRT display screen. Other features include a hexadecimal keypad, cursor and control keys, error and status indicators, external video connector, and mass storage interfaces. Menu parameters and output buffers can be saved during power-down by nonvolatile EEPROM.

Weighing only 17.0 lb (7.7 kg), the monitor is equipped with a dust cover and traveling handle; a bracket is available for rackmounting in a std 19″ (48-cm) frame for technical control applications. The companion MSU III dual-floppy diskette mass storage unit provides unattended line monitoring, data recording, or operator training. A factory installed conversion package is available for $1220 that adds X.25 and other DLM IV diagnostic features to an active model DLM III. **Digilog Inc, Network Control Div,** Babylon Rd, Horsham, PA 19044.



Circle 380 on Inquiry Card

Test equipment aids development and testing of MIL-STD-1553 multiplex hardware and systems

Members of multiplex test equipment line are designed for use with multiplex hardware and systems conforming to MIL-STD-1553 A/B. The bus controller/monitor dual-function test instrument functions as a bus controller for design, development, and final testing of remote terminals, or as a device for monitoring data buses during system integration. The multi-terminal simulator develops and tests bus controllers and bus control software. Both have dual standby redundant data buses and provide for either direct coupled or transformer coupled connection to data buses. Units control the amplitude of transmitted words from 0 to 20 V pk-pk. They can be operated manually or under control of a general purpose computer via a high speed parallel interface, allowing for automated testing or dynamic simulations.

As a bus controller, the bus controller/monitor formats commands and data for transmission on data buses per MIL-STD-1553 protocol. As a bus monitor, the unit compares traffic on the data buses with a trigger word. When a word with positive sync on the selected data bus matches the trigger word, the device takes a 256-word snapshot of data bus traffic. Validity checks are made and stored with each of the 256 words. Up to 32 remote terminals can be simulated by the multi-terminal simulator to develop and test bus controllers and bus control software. Validity checks verify parity, Manchester coding, and data sync timing. Both units require 115 Vac at 1 A (50 to 400 Hz). Op temp is 10 to 35 °C. **Test Systems, Inc,** 217 W Palmaire, Phoenix, AZ 85021.

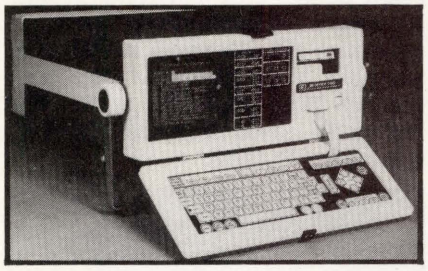
Circle 381 on Inquiry Card

Data analyzer/recorder aids data communications diagnostics

Interview® 3900 data communications analyzer and selective data recorder monitors serial data and provides protocol diagnostics, network performance measurements, and traffic analysis. Up to 100 tests can be stored on a single tape; tests are entered by menu selection. The system automatically translates all codes to ASCII; data and test program used can be printed out on any ASCII printer. All data, protocol characters, and hexadecimals are printed for a permanent record.

(continued on page 227)

Prompt messages notify the operator when an event has occurred and suggest appropriate responses. Messages are composed by the user to meet specific requirements. International interface standards, such as V.35, X.21, and V.24, in addition to loop current MIL-STD-188C and RS-232, are built in. External adapters are available for RS-449 and Bell 303. Character sequence detection, required for 75% of diagnostic and performance measurements, is directly entered from the code converted full ASCII keyboard. Up to 16 separate strings can be entered in a test. Simultaneous search of online data for 8 strings of 16 chars is accomplished at speeds of up to 9.6k bits/s.



Recording of 72k bits/s is accomplished with an optional 1M-bit solid state memory board. Data can be selectively transferred onto permanent storage magnetic tape that holds up to 600,000 chars for further analysis. A conversion kit is available to upgrade the company's Interview 3500 to the 3900. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.

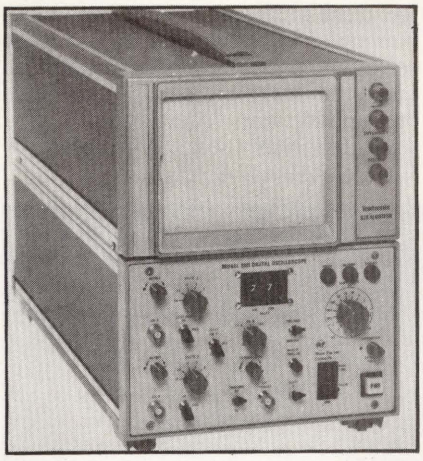
Circle 382 on Inquiry Card

Multifunction data communications tester

Designed for field service use, Hawk 4020 performs interactive troubleshooting and passive monitoring of serial data associated with the EIA RS-232-C digital interface. Data traffic is displayed on a 1-line, 20-char alphanumeric readout. Interactive and monitoring functions are configured from a menu selection format that displays the various system parameters. The device can passively monitor and trap online data, perform a bit or block error rate test, and simulate both data terminal and data communications equipment to interactively communicate with both local and remote network components. It can also be configured to transmit or reply to polling messages, generate or check CRC, and measure either RTS/CTS or RTS/DCD delays. **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02865.

Circle 383 on Inquiry Card

Digital storage oscilloscope



PR 8101 features dual-mode capability, functioning as an analog oscilloscope in realtime mode and providing for single-sweep storage in the stored mode. Std features include 20-MHz sample rate, 10-MHz bandwidth, 8-bit resolution, 4k memory (expandable to 8k), dual-channel, pre- and post-trigger data capture, cursor control, and IEEE-488 interface. Optional interfaces allow flexibility for automated signal processing. The oscilloscope is priced at $5400. **Micro-Pro, Inc,** Advance Lane, Colmar, PA 18915.

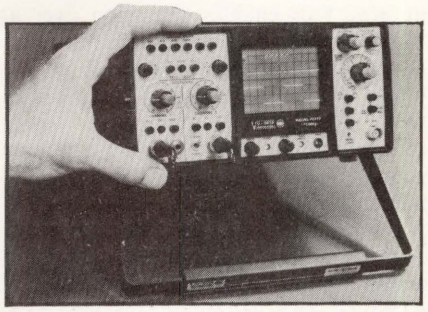
Circle 384 on Inquiry Card

Handler for EPROM programming and testing

Automated G101 Gang EPROM handler interfaces to multisocket programmers/testers. Designed for simultaneous production testing and programming of 16 EPROMs, it also can be used to verify preprogrammed parts. Mechanical throughput is said to be as high as 7200 devices/h, but will be lowered by device dependent test and program times. The handler is constructed with two independent loading rails, each with LED displayed status conditions, including IN TRAY EMPTY, TEST SITE FAILURE, OUTPUT HOLDING TRAY JAM, and OUTPUT SORT TUBE JAM/FULL. A test site release button allows jammed parts to drop through to a sort tube; parts are visible and accessible at all times. Once programming is completed, parts drop automatically for sorting. There is a 1-s delay before the next series of parts starts loading into the test sites. One operator can operate 4 handlers at a time. **Advant Corp,** 696 Trimble Rd, San Jose, CA 95131.

Circle 385 on Inquiry Card

Portable oscilloscope



Model PS975 75-MHz miniscope weighs 13.75 lb (6.19 kg) and has a volume of less than 550 in^3 (9013 cm^3). Features include dc to 75-MHz bandwidth, 2-ns sweep resolution, 5-mV/div sensitivity, less than 5-ns rise time, delay line, and X-Y capability. Fully floating CRT is enclosed in μmetal shield, cushioned by layers of foam rubber to absorb shock if instrument is dropped. **Vu-data Corp,** 7170 Convoy Ct, San Diego, CA 92111.

Circle 386 on Inquiry Card

SYSTEM ELEMENTS

Monolithic, bipolar op amps

3500/MIL series op amps offer input offset voltage of ± 5 V max, output voltage of ± 10 V min, output current of ± 10 mA, and bias current of ± 30 nA max. Model 3500R/MIL offers 100% screening, PDA verified to less than 10%, and groups A and B testing performed on each inspection lot. Model 3500R/883B has the same electrical specs as the /MIL device over -55 to 125 °C. Class B screening is performed 100%. Model 3500U/883B features premium specs from -25 to 85 °C and has specs from -55 to 125 °C. All units are hermetically sealed in a TO-99 package. **Burr-Brown,** International Airport Industrial Pk, Tucson, AZ 85734.

Circle 387 on Inquiry Card

Fiber optic transmitter, receiver, and evaluation kit

Designed for TTL compatible data transmission via optical fibers, the FOT-108B transmitter provides data rates of up to 20M bits/s NRZ while the FOR-100B receiver handles rates up to 5M bits/s NRZ. The transmitter emits light at 820 nm from a 500-μm port that can couple over 100 μW into a 400-μm fiber and couple over 20 μW into a 200-μm fiber at an op current of 70 mA. Optical rise time is 15 ns. The receiver uses a pin photodiode and a wideband transimpe-

(continued on page 228)

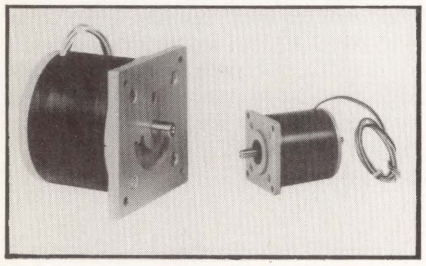
dance amp ac coupled to a comparator that provides TTL and CMOS compatible output. This enables operation over a 45-dB dynamic range and also sensitivity of 100 nW at 400k bits/s or 2 μW at 5M bits/s, both at a bit error rate of less than 10^{-10}. Both transmitter and receiver operate from a single 5-V power supply and are packaged in a 14-pin metal case DIP.

An evaluation kit for these devices, EZLINK™ includes the receiver and transmitter plus 10 m of Dupont PIFAX™ S-120 type 30 plastic-clad silica 200-μm core fiber assembled with bayonet connectors. The kit also includes assembled boards. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Circle 388 on Inquiry Card

Hybrid stepper motors

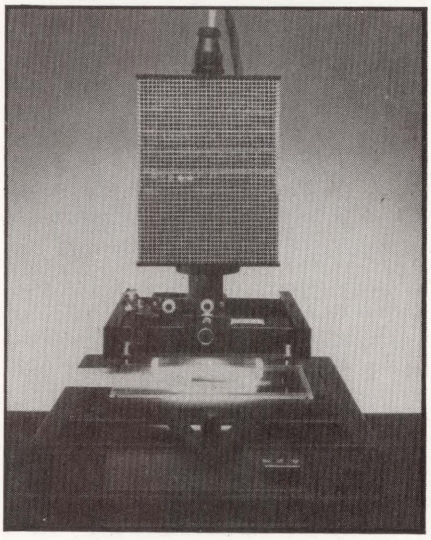
Size 15 stepper motor steps in 1.875° increments and provides fast damping and accurate control required for lower speed machines, along with high torque to inertia and torque to volume ratios. These characteristics make it suitable for printwheel applications in daisywheel printers. Size 23 steps in 1.8° increments with a nominal accuracy of ±5%; higher accuracy is available. It provides 90 oz-in (0.63 N • m) of dynamic torque and a min slew rate of up to 10,000 pulses/s. Very low noise makes the unit suited for disc drive positioning, carriage and paper feed drive, and tape head positioning applications; it can also be used in machine tool applications. **Clifton Precision,** PO Box 160, Murphy, NC 28906.



Circle 389 on Inquiry Card

Solid state electronic camera

Designed for image processing, CAD/CAM, and computer or communications graphics, model C321 camera has resolution at the image plane (35 mm) of 4.5M pixels in a 1720 x 2592 format. Pixels are output from the camera at a 2-MHz rate, each consisting of 8 parallel bits representing 256 levels of gray. Any 35-mm lens can be used with the camera; with a commercially available 35-mm lens, imaging an 8.5 x 11″ (21.6- x 28-cm) page gives a resolution in the object plane of 200 dots/in (79/cm). An illumination compensator option that calibrates the system for lens anomalies and nonlinearity in lighting is available for applications requiring true gray scale. **Datacopy Corp,** 1070 E Meadow Cir, Palo Alto, CA 94303.



Circle 390 on Inquiry Card

Coded miniature rotary switches

Switches offer choice of BCD or BCD-complement coded outputs and are rated to make and break 125 mA at 30 Vdc, resistive load for 25,000 cycles of operation. Contact resistance is 20 mΩ initially and 300 mΩ max after life, insulation resistance is 50,000 MΩ initially and 10,000 MΩ after life, and voltage breakdown is 500 Vac between mutually insulated parts. Switch dimensions are approx 0.5″ (1.27 cm) in diameter and 0.44″ (1.11 cm) behind the panel. Units are available with PC terminals that extend from the rear of the switch, and are priced at $8.50 each in quantities of 100. **Grayhill, Inc,** 561 Hillgrove Ave, La Grange, IL 60525.

Circle 391 on Inquiry Card

Subminiature slide switch

Model 625 is a 3-position, 3-pole switch with 2 poles being off-on-on and off-on-off and the third pole a normally open momentary action pushbutton that makes contact only when pushed in positions 2 and 3. The switch features a max dimension of 0.625″ (1.588 cm), long life construction (typ in excess of 150,000 cycles), nickel silver frame with phenolic housing, and precious metal contacts providing low contact resistance. It is available with terminals either "straight through" or angled at 90° to the plane of the switch body. **Wilbrecht Electronics, Inc,** 240 Plato Blvd, St Paul, MN 55107.

Circle 392 on Inquiry Card

Tactile feel keyboards

Provided with membrane style panel surfaces, including graphics and capabilities of rear lighted or front panel LED signaling, the TACTIFLEX keyboard features a dome switch contact that allows high density circuitry to remain uninterrupted. Nom switch actuation pressures of 8 or 16 oz (224 or 448) g) are available. Spill proof and puncture resistant surfaces are completely sealed to guard against dust and contaminants. Keyboard is capable of contact resistances from 1 to 10 Ω at 0.5 to 5 mA, 5 Vdc, and is available with gold, silver, or nickel circuitry. **Bowmar Instrument Corp,** 4640 126th Ave N, Clearwater, FL 33520.

Circle 393 on Inquiry Card

EMI PROTECTION

RFI power line filters

Series F1400, designed for switching power supply noise attenuation, features a high peak current design to provide high insertion loss at min leakage current. Filters meet VDE and SEV requirements and have a dual current rating of 3 A/115 V for U.S. and 1.5 A/250 V for Europe. Line frequency is 50/60 Hz, and max leakage current, each line to ground, is 0.40 mA at 250 Vac, 50 Hz. Filters are available with wire leads or quick connect terminations. **Curtis Industries, Inc,** 8000 W Tower Ave, Milwaukee, WI 53223.

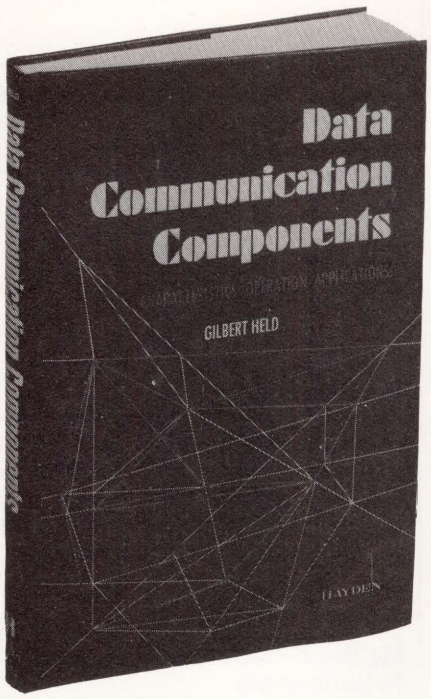
Circle 394 on Inquiry Card

Designer's Bookcase

DATA COMMUNICATION COMPONENTS: Characteristics, Operation, Applications by *Gilbert Held.*

A comprehensive guide to the utilization of over 25 distinct components in data communications networks. Explains basic characteristics of each component, how they operate, and the economics and cost-benefits tradeoffs one should consider prior to their incorporation into a network.

Hayden Book Company, Inc., 280 pages, 6 x 9, 5.26-3, $19.50 Circle 455 on Inquiry Card

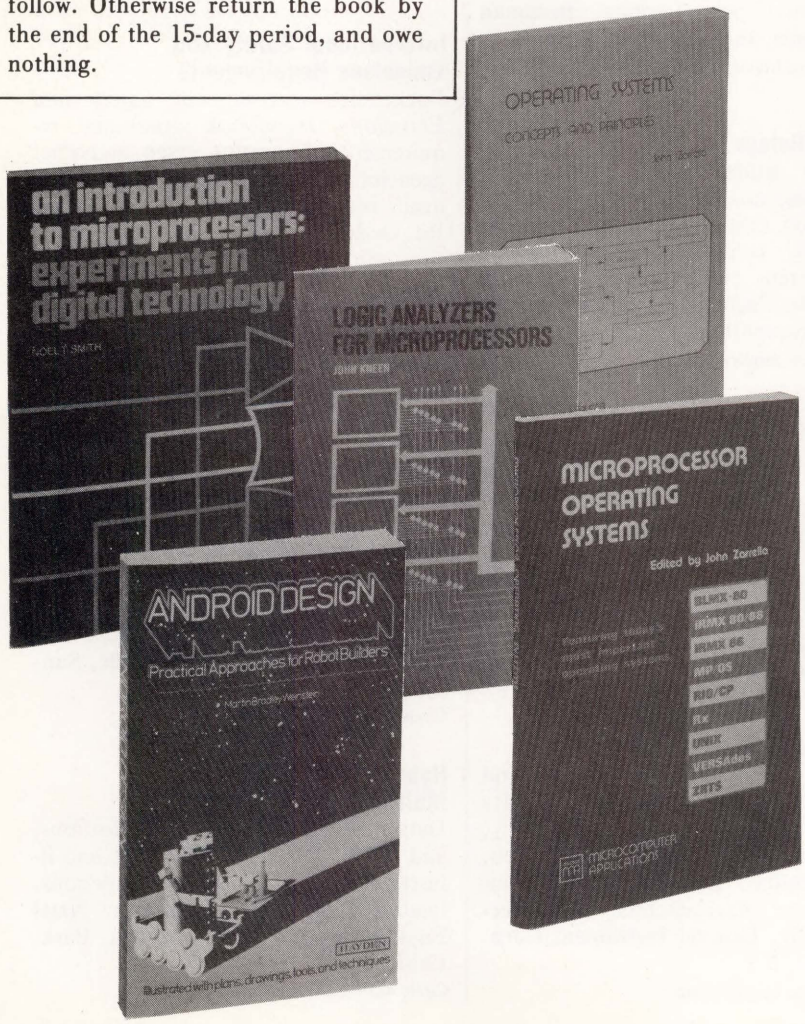


HOW TO ORDER:

15-DAY FREE EXAMINATION

Simply circle the appropriate number(s) on the Reader Inquiry Card at the back of this magazine.

Your book will be sent to you for your **15-day free trial.** If you are satisfied, keep the book and an invoice will follow. Otherwise return the book by the end of the 15-day period, and owe nothing.



OPERATING SYSTEMS: CONCEPTS AND PRINCIPLES by *John Zarrella.*

Used by Intel, Zilog, and Harris for software training. The most important component of system software is the operating system. This book provides an introduction to current operating systems technology. Operating systems concepts, capabilities, and terminology are explained.

Microcomputer Applications, 152 pages, 5½ x 8½, 1979, $8.95 Circle 456 on Inquiry Card

MICROPROCESSOR OPERATING SYSTEMS Edited by *John Zarrella*

Designed for microprocessor system users and anyone who must select, evaluate, or design operating systems to support applications software, this book contains descriptions of the most important systems currently available. Each chapter is written by an industry leader involved in the development or implementation of the operating system. This wealth of user-oriented technical detail makes it easy for you to compare systems. The BLMX-80, iRMX 80/88, iRMX 86, MP/OS, RIO/CP, Rx, UNIX, VERSAdos, and ZRTS Operating Systems are described.

Microcomputer Applications, 166 pages, 6 x 9, 1981, $11.95 Circle 457 on Inquiry Card

LOGIC ANALYZERS FOR MICROPROCESSORS by *John Kneen*

The most up-to-date information available on diagnostic test equipment for digital system troubleshooting. Describes the current second-generation set of logic analyzers for bus analysis problems on a bus-by-bus basis, with inclusions of cross-bus event correlation and data trace linked and nested loop algorithms.

Hayden Book Company, Inc., 128 pages, 6 x 9, 0953-4, $9.80 Circle 458 on Inquiry Card

AN INTRODUCTION TO MICROPROCESSORS: Experiments in Digital Technology by *Noel T. Smith*

A "learn-by-doing" guide to the use of integrated circuits provides a foundation for the understanding of the underlying hardware actions of programming statements. Emphasis is placed on how digital circuitry compares with analog circuitry. Experiments provide clear understanding and encourages the reader to construct electronic projects using integrated circuits.

Hayden Book Company, Inc., 184 pages, 8½ x 11, 0867-8, $10.95 Circle 459 on Inquiry Card

ANDROID DESIGN: Practical Approaches for Robot Builders by *Martin Weinstein.*

A comprehensive look at the tools, materials and techniques necessary for designing an android. Examines what an android is, what you can expect it to do, and how this will translate into the design requirements. Also looks at both usual and unusual hardware and software, and mechanics and mechanisms.

Hayden Book Company, Inc., 256 pages, 6 x 9, 5192-1, $11.95 Circle 460 on Inquiry Card

Breadboard System
Bulletin that details Scotchflex breadboard kit depicts components, step-by-step assembly and connection, and insulation-displacement solderless connection system, and lists optional microprocessor boards. **3M**, St Paul, Minn. Circle 404 on Inquiry Card

Miniature and Subminiature Switches
Photos, drawings, and specs are included in catalog that features Mini Mike, module series, Tapit, Mr Clean II, and TO-5 switches, and illuminated and non-illuminated rocker and paddle switches. **Chicago Switch Inc**, Chicago, Ill.
Circle 405 on Inquiry Card

Computer Systems
Illustrated brochure on MOD 3100 discusses design, hardware, software, graphics displays, POL*3 programming language, and architecture. **Taylor Instrument Co, Div of Sybron Corp**, Rochester, NY.
Circle 406 on Inquiry Card

Connectors
Catalog comprises photos, dimensional drawings, specs, and information on design and construction of IDC flat cable and D-subminiature connectors, box connectors and headers, and transistor sockets. **Eby Co**, Philadelphia, Pa.
Circle 407 on Inquiry Card

Sonic Digitizer
Technical bulletin presents description, specs, menu features, and output formats of GrafBar model GP-7 digitizer. **Science Accessories Corp**, Southport, Conn. Circle 408 on Inquiry Card

Fixed Precision Wirewound Resistors
Found in 7-p brochure are description, application, specs, and engineering data for ultra high, high precision, precision positive TCR, precision power, and standard style resistors. **Precision Resistor Co, Inc**, Hillside, NJ.
Circle 409 on Inquiry Card

Flexible Circuits
Design and manufacturing advantages of flexible circuit interconnects are explained in brochure that provides design and specification guidance. **Buckbee-Mears Co**, Nashua, NH.
Circle 410 on Inquiry Card

Electronic Components
Selector guides, application notes, technical data, tables, charts, and drawings are supplied by 206-p catalog that describes fixed resistors, resistor networks, panel and trimming potentiometers, and adjustable attenuators. **Allen-Bradley Co**, Milwaukee, Wis.
Circle 411 on Inquiry Card

Data Communications for Minicomputers
Brochure includes descriptions and photos of data and multidrop concentrators, programmable communications controllers, port selectors, and combination multiplexer/modems. **Micom Systems, Inc**, Chatsworth, Calif.
Circle 412 on Inquiry Card

Multiturn Precision Potentiometers
Illustrated brochure on Helipot® line gives specs for 7/8 x 3/4″ wirewound and hybrid models, and data on environmental ruggedness, standard resistance values, and power rating. **Beckman Instruments, Inc**, Fullerton, Calif.
Circle 413 on Inquiry Card

Control Relays
Selection guide, photos, schematics, wiring diagrams, and specs are provided by catalog that describes low profile, miniature, mechanical and magnetic latch, current sensitive, power, and solid state units. **Eagle Signal Industrial Controls**, Davenport, Iowa.
Circle 414 on Inquiry Card

Motors and Gearmotors
Bulletin provides performance ratings, features, characteristics, performance illustrations, and dimensional drawings of ac subfractional electric motors, gearmotors, gear reducers, variable speed controls, and base mounting adapters. **Robbins & Myers, Inc, Electric Motor Div**, Springfield, Ohio.
Circle 415 on Inquiry Card

LSI Microcircuits
Featured in catalog are specs and descriptions of ROM, electrically alterable, nonvolatile memory, microcomputer, speech synthesis, video, tuning, audio, control, and telecommunications microcircuits. **Microelectronics Div, General Instrument Corp**, Hicksville, NY.
Circle 416 on Inquiry Card

Lighted Pushbutton Switches and Indicators
Detailed in catalog are cross-reference charts, specs, photos, and schematics for Optolite and Presslite switches and incandescent, neon, and LED indicators. **Oak Switch Systems, Inc**, Crystal Lake, Ill.
Circle 417 on Inquiry Card

High Density Digital Cartridge Tape Drive
General description, options available, specs, and photo are found on data sheet that discusses series 3400 drive called Funnel. **Data Electronics, Inc**, San Diego, Calif.
Circle 418 on Inquiry Card

RS-232 to IEEE 488 Bus Controller
Illustrated brochure discusses remote computer system, typical application, operation, commands, and specs for model 4885A. **ICS Electronics**, San Jose, Calif.
Circle 419 on Inquiry Card

International Safety and Emissions Requirements
Pocket-size *International Safety and Emissions Handbook* combines requirements of FCC, VDE, CISPR, and other agencies. Request on company letterhead from **ACDC Electronics**, 401 Jones Rd, Oceanside, CA 92054.

Peripherals for Microcomputers
Catalog presents model numbers and descriptions of hard disc, mirror backup, and constellation network systems, demo kits, Apple software, accessories, and manuals. **Corvus Systems**, San Jose, Calif.
Circle 421 on Inquiry Card

Data Communications
Handbook covers telephone systems; telecommunications networks; network peripherals, modes, and protocols; and network diagnostics. **Racal-Vadic**, Sunnyvale, Calif.
Circle 422 on Inquiry Card

Hybrid 4-Quadrant Multiplying Sin/Cos DAC
Data sheet listing features, applications, and specs of HDSC 2016 explains and illustrates operation, self-test functions, loading, and pin designations. **Natel Engineering Co, Inc**, Canoga Park, Calif.
Circle 423 on Inquiry Card

OWNERSHIP STATEMENT
Statement of the Ownership, Management
Etc. of
COMPUTER DESIGN
September 30, 1981

(This statement is published in compliance with the Act of October 23, 1962).
Published monthly, at Littleton, MA.
Publisher: Ronald W. Evans
Editor: Saul B. Dinman
Managing Editor: Sydney F. Shapiro

The Owner is: Computer Design Publishing Co, 11 Goldsmith St, Littleton, MA, subsidiary of PennWell Publishing Company, 1421 S. Sheridan, Tulsa, Oklahoma.

Stockholders holding 1 percent or more of total amount of stock of PennWell Publishing Co.: Estate of Helen B. Lauinger, Tulsa, Okla.; P.C. Lauinger, Tulsa, Okla; Edward P. Boyle, Oil City, Pa. Known stockholders, mortgages and other security holders holding 1 percent or more of the total amount of bonds, mortgages or other securities: None.

The average number of copies of the publication during the twelve months preceding the date shown above is: Printed—90,693; paid subscriptions by mail—1,228, total paid subscriptions—1,228; free distribution including samples, by mail, carrier or other means—87,983; total distribution—89,211; office use, left over, unaccounted, spoiled after printing—1,494; total above—90,693. Actual number of copies of single issue published closest to filing date; Printed—92,092; paid subscriptions by mail—1,258; total paid circulation—1,258; free distribution, including samples, by mail, carrier or other means—89,197; total distribution—90,455; office use, left over, unaccounted or spoiled after printing—1,637; total above—92,092.

I certify that the above statements made by me are correct and complete.

Ronald W. Evans
Publisher

AD INDEX

AD INDEX

CD* SALES OFFICES

Home Office
Director of Marketing
Gene Pritchard
Direct Marketing Sales Mgr
Maureen Sebastian
Classified Advertising Mgr
John G. French
11 Goldsmith St.
Littleton, MA 01460
(617) 486-8944

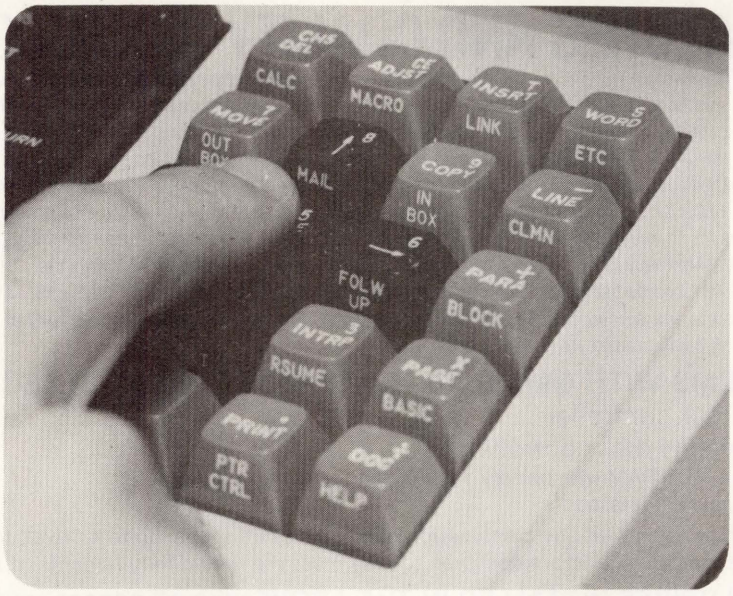
New England and Upstate New York
Regional Sales Manager
Carol E. Fountain
11 Goldsmith St.
Littleton, MA 01460
(617) 486-8944

Middle Atlantic States, Long Island and Southeastern States
Dick Busch, Inc.
Richard V. Busch
6 Douglass Dr., R.D. #4
Princeton, N.J. 08540
(201) 329-2424

Midwestern States and Colorado
Berry Conner Associates
Berry Conner, Jr.
88 West Schiller St.
Suite 2208
Chicago, IL 60610
(312) 266-0008

Western States and Texas
Buckley/Boris Assoc., Inc.
Terry Buckley
Tom Boris
John Sabo
22136 Clarendon St.
Woodland Hills, CA 91367
(213) 999-5721
(714) 957-2552
Terry Buckley
Barbara Arnold
P.O. Box 278
Campbell, CA 95009
(408) 866-8735
(213) 999-5721

Today, executives push buttons, too.



Learn about your evolving office at

THE THIRD ANNUAL

OFFICE AUTOMATION CONFERENCE

Moscone Center • San Francisco • April 5-7, 1982

Everyone is affected by office automation. Directly or indirectly. The dramatic changes it carries with it touch all our lives. For some of us, how we manage these changes may even shape our professional futures.

That's why we urge you to attend the one conference that can provide you with the latest information about and insights into this exciting-but-sometimes-scary concept. We'll accomplish this through a program of technical sessions spotlighting featured speakers. Through a series of innovative industry-related workshops. Through an exhibit floor packed with displays by some 200 companies.

If you're uncertain about any aspect of office automation, don't push the panic button! Instead, fill out and mail this coupon. Learn in more detail about the conference whose theme focuses on "The Human Connection." On you.

Sponsored by the American Federation of Information Processing Societies, Inc.

NAME_____ TITLE_____

COMPANY_____

ADDRESS_____

CITY_____ STATE_____ ZIP_____

Mail to:
AFIPS
1982 O A C
P.O. Box 9659
Arlington, VA. 22209

c **"THE INTERNATIONAL CONFERENCE FOR DECISION MAKERS"**

JUDGE THE REST, THEN BUY THE BEST

Only GIMIX offers you **SOFTWARE SWITCHING** between **MICROWARE's OS-9** and **TSC's FLEX**. Plus you get the power of the GMXBUG system monitor with its advanced debugging utility, and memory manipulation routines. A wide variety of languages and other software is available for these two predominant 6809 Disk Operating Systems.

You can order a system to meet your needs, or select from the 6809 Systems featured below.

JUDGE THE FEATURES AND QUALITY OF GIMIX 6809 SYSTEMS

GIMIX' CLASSY CHASSIS™ is a heavyweight aluminum mainframe cabinet with back panel cutouts to conveniently connect your terminals, printers, drives, monitors, etc. A 3 position keyswitch lets you lock out the reset switch. The power supply features a ferro-resonant constant voltage transformer that supplies 8V at 30 amps, +15V at 5 amps, and −15V at 5 amps to insure against problems caused by adverse power input conditions. It supplies power for all the boards in a fully loaded system plus two 5 ¼'' drives (yes! even a Winchester) that can be installed in the cabinet. The Mother board has fifteen 50 pin and eight 30 pin slots to give you the most room for expansion of any SS50 system available. 11 standard baud rates from 75 to 38.4K are provided and the I/O section has its own extended addressing to permit the maximum memory address space to be used. The 2 Mhz 6809 CPU card has both a time of day clock with battery back-up and a 6840 programmable timer. It also contains 1K RAM, 4 PROM/ROM/RAM sockets, and provides for an optional 9511A or 9512 Arithmetic Processor. The RAM boards use high speed, low power STATIC memory that is fully compatible with any DMA technique. STATIC RAM requires no refresh timing, no wait states or clock stretching, and allows fast, reliable operation. The system includes a 2 port RS232 serial interface and cables. All GIMIX boards use gold plated bus connectors and are fully socketed. GIMIX designs, manufactures, and tests in-house its complete line of products. All boards are twice tested, and burned in electrically to insure reliability and freedom from infant mortality of component parts. All systems are assembled and then retested as a system after being configured to your specific order.

56KB 2MHZ 6809 SYSTEMS WITH GMXBUX/FLEX/OS-9 SOFTWARE SELECTABLE

With #58 single density disk controller **$2988.59**
With #68 DMA double density disk controller **$3248.49**
to substitute Non-volatile CMOS RAM with battery back-up, add 300.00
for 50 Hz export power supply models, add 30.00

Either controller can be used with any combination of 5'' and/or 8'' drives, up to 4 drives total, have data recovery circuits (data separators), and are designed to fully meet the timing requirements of the controller I.C.s.

5 ¼'' DRIVES INSTALLED IN THE ABOVE with all necessary cables

	SINGLE DENSITY		DOUBLE DENSITY		
	Formatted	Unformatted	Formatted	Unformatted	
40 track (48TPI) single sided	199,680	250,000	341,424	500,000	2 for **$700.00**
40 track (48TPI) double sided	399,360	500,000	718,848	1,000,000	2 for **900.00**
80 track (96TPI) single	404,480	500,000	728,064	1,000,000	2 for **900.00**
80 track (96TPI) double	808,960	1,000,000	1,456,128	2,000,000	2 for **1300.00**

Chart shows total capacity in Bytes for 2 drives.

Contact GIMIX for price and availability of 8'' floppy disk drives and cabinets; and 5'' and 8'' Winchester hard disk system.

128KB 2Mhz 6809 DMA Systems for use with TSC's UNIFLEX or MICROWARES's OS-9 Level 2

(Software and drives not included) **$3798.39**
to substitute 128KB CMOS RAM with battery back-up, add 600.00
for each additional 64KB NMOS STATIC RAM board, add 639.67
for each additional 64KB CMOS STATIC RAM board, add 988.64
for 50 Hz export power supply, add 30.00

NOTE: *UNIFLEX can not be used with 5'' minifloppy drives.*

GIMIX has a wide variety of RAM, ROM, Serial and Parallel I/O, Video, Graphics, and other SS50 bus cards that can be added now or in the future. Phone or write for more complete information and brochure.

THE SUN NEVER SETS ON GIMIX USERS

GIMIX Systems are found on every continent, except Antarctica. (Any users there? If so, please contact GIMIX so we can change this.) A representative group of GIMIX users includes: **Government Research and Scientific Organizations** in Australia, Canada, U.K., and in the U.S.; NASA, Oak Ridge, White Plains, Fermilab, Argonne, Scripps, Sloan Kettering, Los Alamos National Labs, AURA. **Universities:** Carleton, Waterloo, Royal Military College, in Canada; Trier in Germany; and in the U.S.; Stanford, SUNY, Harvard, UCSD, Mississippi, Georgia Tech. **Industrial users** in Hong Kong, Malaysia, South Africa, Germany, Sweden, and in the U.S.; GTE, Becton Dickinson, American Hoechst, Monsanto, Allied, Honeywell, Perkin Elmer, Johnson Controls, Associated Press, Aydin, Newkirk Electric, Revere Sugar, HI-G/AMS Controls, Chevron. **Computer mainframe and peripheral manufacturers,** IBM, OKI, Computer Peripherals Inc., Qume, Floating Point Systems. **Software houses;** Microware, T.S.C., Lucidata, Norpak, Talbot, Stylo Systems, AAA, HHH, Frank Hogg Labs, Epstein Associates, Softwest, Dynasoft, Research Resources U.K., Microworks, Analog Systems, Computerized Business Systems.

TO ORDER BY MAIL

SEND CHECK OR MONEY ORDER OR USE YOUR VISA OR MASTER CHARGE. Please allow 3 weeks for personal checks to clear.

U.S. orders add $5 handling if order is under $200.00. Foreign orders add $10 handling if order is under $200.00.

Foreign orders over $200.00 will be shipped via Emery Air Freight COLLECT, and we will charge no handling. All orders must be prepaid in U.S. funds. Please note that foreign checks have been taking about 8 weeks for collection so we would advise wiring money, or checks drawn on a bank account in the U.S.. Our bank is the Continental Illinois National Bank of Chicago, account #73-32033 Visa or Master Charge also accepted.

GIMIX INC. reserves the right to change pricing and product specifications at any time without further notice.

FLEX AND Uniflex are trademarks of Technical Systems Consultants Inc. OS-9 is a trademark of Microware Inc. See their ads for other **GIMIX** compatible software

GIMIX Systems are chosen by the Pros because of quality, reliability and features.

GIMIX INC.

The Company that delivers
Quality Electronic products since 1975.

1337 WEST 37th PLACE, CHICAGO, IL 60609
(312) 927-5510 • TWX 910-221-4055

CIRCLE 135 ON INQUIRY CARD

CØMPLØT® SERIES 7000 DIGITIZERS HAVE MORE . . .

the Houston way

What a combination in a standard digitizer

. . . Up to 200 coordinate pairs per second digitizing rate in 8 switch selectable rates . . . ±0.005″ accuracy right up to the edge of the active area. . . . Resolution as fine as .001″ (.005″ and .010″ also switch selectable).

There is more yet. Only Houston Instrument's Series 7000 digitizers feature an extra dedicated menu area, in a complete border around the active area. No need to buy a separate menu pad. The Series 7000 digitizers are all translucent (at no extra charge) which makes them ideal for backlighting. Thoughtfully placed stylus/cursor connectors on each side allow both left and right-handed operators to perform comfortably.

There are 40 user set configuration controls available which enable you to tailor the Series 7000 digitizer to your specific applications. For CAD or other interactive applications, functions can be down loaded by the host computer. Point, stream, switch stream and incremental modes, fixed or relocatable origin — of course.

There's a Series 7000 digitizer size especially for you — active areas of 12″x12″, 17″x24″, 36″x48″ and 42″x60″. And you won't have to worry about demagnetization or biasing — EVER.

Power tilt stands (with or without backlighting) are available for maximum flexibility and operator comfort.

If all this sounds fantastic, we agree. And with prices starting at $2,950*, we're convinced that the Series 7000 digitizers offer the ultimate in speed, accuracy and resolution.

Let us show you the Houston way. Call or write Houston Instrument, 8500 Cameron Road, Austin, Texas 78753.(512) 835-0900. For descriptive literature, outside Texas, call toll free, 1-800-531-5205. For technical information ask for operator #6.

houston instrument
GRAPHICS DIVISION OF
BAUSCH & LOMB

* U.S. suggested retail price. OEM prices available.
® Registered trademark of Houston Instrument.
• Tested for FCC rules and regulations, Class A.

Circle 136 for Literature
Circle 137 to Have a Representative Call

Pro-Log M980 Programmer: Best for development.

Interfaces directly with your development system.

For developing new products that use programmable devices, save valuable time by downloading programs directly to the Pro-Log M980 programmer. The M980 interfaces with popular development systems, as well as with computers and modems, paper-tape readers and TTYs.

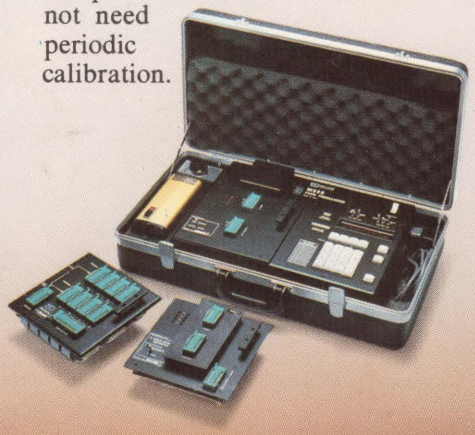
Twenty data formats are key-selectable on the M980. The RS232C baud rate is also selectable—from 50 to 9600. And the addresses can be offset during downloading and uploading.

Ready for over 450 programmable devices.

With the powerful M980 control unit and our vendor-approved personality modules, you can program, copy, test and edit most MOS and bipolar PROMs and logic devices. And you're ready for new devices as they come along . . . including devices as large as 64K × 16 bits.

No calibration required.

Because our programming voltages and timing are generated using proven designs and precision components, the M980 does not need periodic calibration. So you don't need expensive calibrating equipment and trained personnel, and you don't lose the use of your programmer every 90 days.



Find out more.

Pro-Log has provided programming leadership since 1973. Over 9,000 programmers and 20,000 personality modules are now performing reliably worldwide.

For full details, send for our 32-page M980 brochure. Or better yet, ask for a free demonstration.

Write or call Pro-Log Corporation, 2411 Garden Road, Monterey, CA 93940, phone (408) 372-4593.

PRO-LOG CORPORATION

CIRCLE 138 ON INQUIRY CARD