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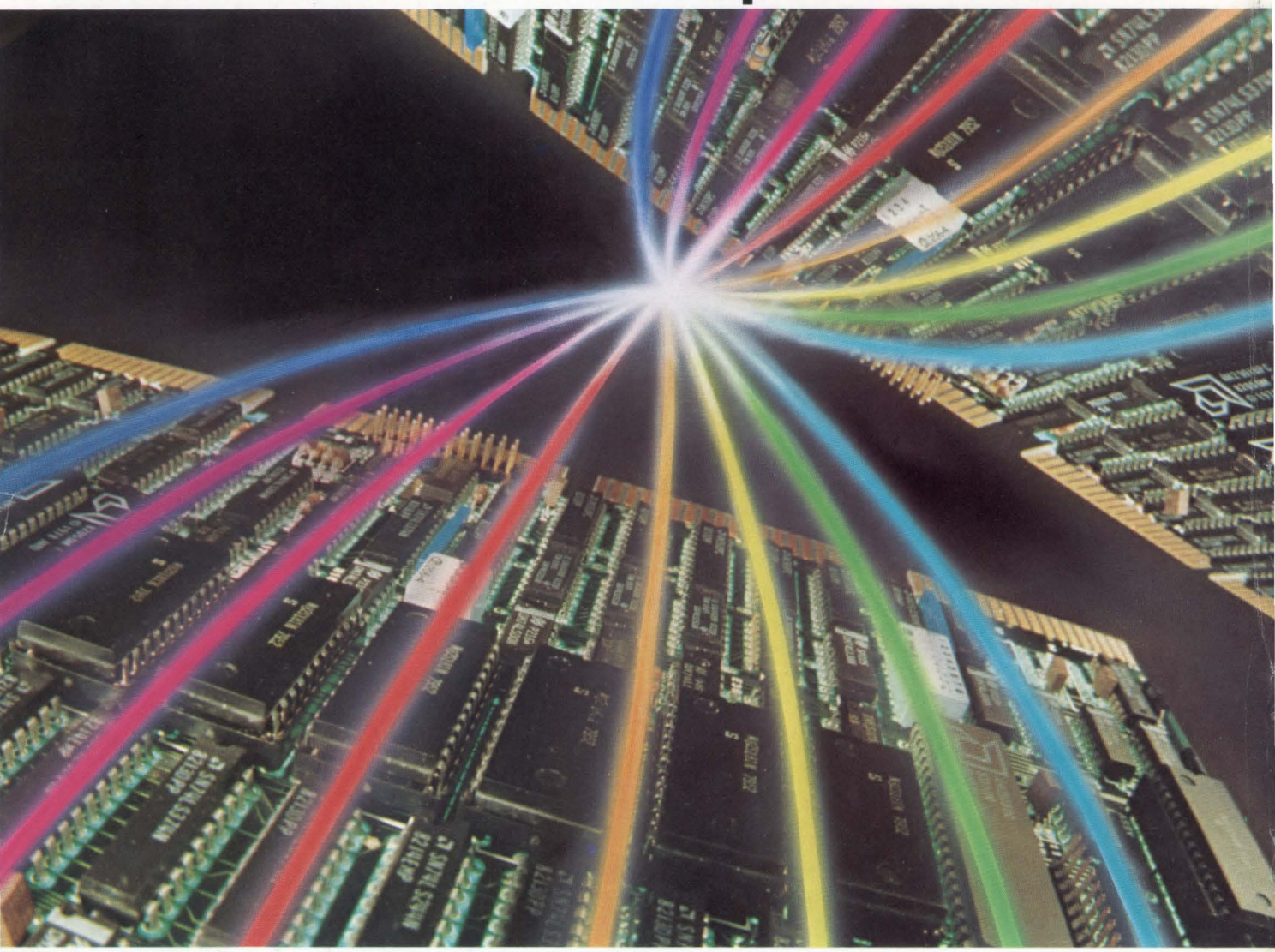
JUNE 198

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

SPECIAL REPORT: SEMICONDUCTOR MEMORIES

From out of the West...Tape Dimension III



Brings a new dimension to Unibus efficiency for $1983.

Tape Dimension III is the only buffered tri-density (GCR/PE/NRZI) TS-11™-emulating controller on the market. The combination of its unique asynchronous handshake design and 64K byte buffer enables it to take full advantage of bus speeds without the risk of causing data late conditions in other bus transfer operations. It makes Tape Dimension III particularly adaptable to systems with high speed disk drives.

And more. The 64K byte buffer provides total immunity to data late conditions, even at high-speed data rates on a highly populated peripheral bus. In fact, Tape Dimension III actually has greater capability than the TS-11!

Tape Dimension III is completely software-transparent to the VAX™ and PDP-11™ Unibus environment including diagnostics in VMS.

The Tape Dimension III controller supports up to four dual density (Pertec compatible) drives or four tri-density (STC or TELEX type) drives. It is a single embedded hex PC board that fits into any standard SPC slot.

This new dimension in tape transfer dramatically reduces the ratio of protocol to information data. And dramatically increases the efficiency of Unibus utilization. Find out how much it can improve your system throughput. Call or write today for complete information and the name of your nearest distributor (limited quantities) or regional sales representative (OEM quantities).

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CIRCLE 1

You've concluded that you need the performance and capacity that only an 8 inch Winchester drive can provide. Which one should you buy?
There are 109 different models available.
Of this 109, only 39 are 8 inch floppy form-factor compatible.
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And of this 109, only 17 offer true SMD compatibility.
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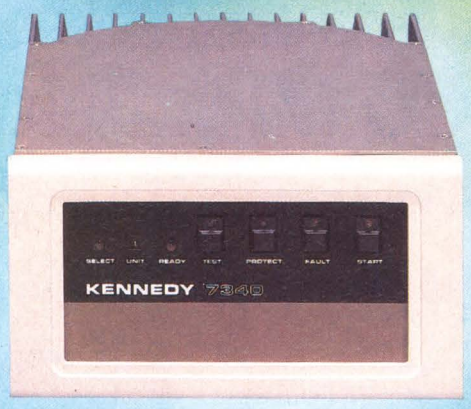

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- Available 30-45 days ARO
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CIRCLE 2

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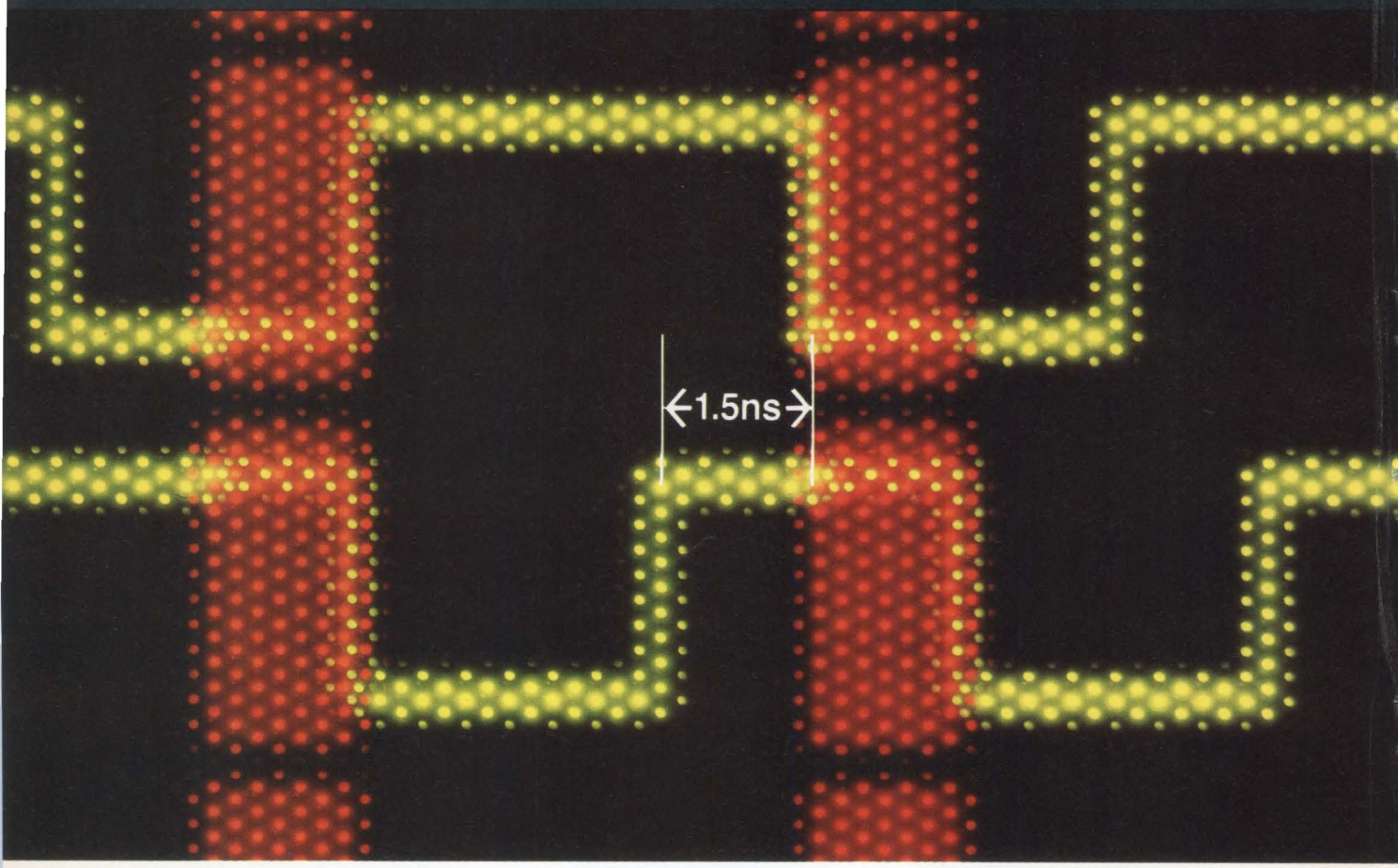
FOR A FUTURE OF CHANGE



At 660 MHz, Tektronix' Color DAS is the fastest logic analyzer ever.

660 MHz.

A fleeting 1.5 ns between sample intervals. No other logic analyzer even comes close.

Transform glitches from ghosts into definable, displayed data. Resolve individual byte transfers on a mainframe data bus. Whatever your application, the Color DAS's new 91A04 Data Acquisition Card redefines the meaning of high-speed logic measurement.

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It's all part of the power you'll find only in Tektronix' Color DAS, which also includes the industry's first color-coded display, data widths to 104 channels, pattern generation and microprocessor software design support.

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UP FRONT

Memories from the last (?) Anaheim NCC

Attendance at NCC '83, whether or not it met the predicted 120,000 to 130,000 figures, was notably heavy—in most of the exhibit areas. Although temperatures in the Pavilion (better known as "The Tent") were said to have reached nearly 115 °F, exhibitors in other areas of the Convention Center and at the Disneyland Hotel found crowds of people to view their products. However, because of the problems with exhibit facilities and local hotel space, reports indicate that in future years NCC will alternate between Las Vegas and Chicago, beginning in 1984 in Las Vegas. Those cities are considered to be the only ones with adequate space for this conference.

Notable in the drive (pardon the pun) to offer small disk drives with greater storage capacities was a family of 5¼" minifloppies from Amlyn Corp. For example, the model 1560 drive provides up to 3.3M bytes of unformatted capacity using double-sided recording.

This year, Control Data announced its Cricket 3½" Winchester disk drive, offering 6.38M bytes of unformatted data storage. This drive uses thin film read/write heads (similar to those in the company's larger disk drives) and nickel-cobalt plated recording media. Custom LSI chips handle servo functions and read chain control.

Although not yet incorporated in any manufacturer's available drives, 5¼" diskette media introduced by the Spin Physics unit of Eastman Kodak are said to be capable of storing up to 10M bytes using vertical recording technology. The media use isotropic cobalt-doped magnetic particles (0.2 μm long) to support both vertical and horizontal magnetization.

Weighing less than 11 lb and operating from either a rechargeable built-in battery or ac power, the PC-5000 is Sharp Electronics' introduction to the portable computer market. It can be used either standalone or coupled to a host computer and is based on an 8088 microprocessor. The portable computer contains 128K bytes of RAM (expandable to 256K) as well as 128K bytes of bubble memory storage and 128K bytes of ROM in cartridge.

Scotsman III, introduced by Racal-Vadic, compresses data at a 2 to 1 ratio. It can compress a 192k-bit data stream, transmit it over a 9600-bps line, and reconstruct it back to 19.2k bits. Four 9600 bisync or two full-duplex 9600 lines can be compressed and transmitted over a single line. The unit is compatible with async, bisync, X.25, SDLC, and HDLC protocols.

Multiple communication lines can be connected to one or more VAX, PDP-11, DECsystem 10, and System 20 computers with the Attach system announced by Able Computer. It allows up to 128 terminal lines to be connected via a single composite cable.

A keyboardless color executive terminal was shown by Santa Barbara Development Laboratories at an off-NCC site. This terminal features touch screen data access and voice control of data entry and editing functions. By touching one of several screen images, the user can access information in less than 1 s. Described by the designers as "user transparent," the system can be used for many phases of communications, information presentation, and office automation. Product introduction is scheduled for late this year.

A generic version of the Unix operating system carrying Western Electric's blessing (and certification) will soon be available for use with three popular 16-bit microprocessors. In a mutually beneficial collaborative agreement, Western Electric has entered into "software development arrangements" with Motorola, Intel, and National Semiconductor for the 68000, iAPX 286, and 16032 processors, respectively.

UP FRONT

Pretriggers

Distributed processing architecture that promises to optimize performance is based on use of a minicomputer for resource allocation and multiple 16-bit microprocessors for task processing. SyFAnet, offered by Computer Automation's Commercial Systems Div, is linked by a broadband network in a proprietary CSMA/CA transmission scheme.

Attributes of both per-line switched PBXs and packet-switched LANs are blended in a distributed communication system from CXC Corp. The Rose system supports from 192 to 50k subscribers with multiple processing nodes and variable bandwidth allocation from 64k to 33M bps.

Integration of data with digitized voice is accomplished by Sydis using a multiprocessor system connected through a LAN. VoiceStation employs several 68000s as application servers, file servers, or voice processors for both switching voice messages over the same system and performing voice digitization and recording. Thus, voice messages can be stored and edited as data files and appended to documents such as word processing files.

Clearer viewing of complex 3-D wireframe images is possible by removing hidden lines and polygon backfaces. In one case, recent software enhancements to the Anvil 4000 mechanical CAD/CAM system from Manufacturing Consultants and Services focus on the mathematical model. In another case, enhancements to the Template® graphics software tools from Megatek emphasize image processing. Both efforts have the same visual effect.

A very high resolution color display system that combines liquid crystal and CRT technologies was described by Tektronix engineers at the recent Society for Information Display conference. Color can now be added to displays without degrading resolution, making the system feasible for use on small instruments.

Simultaneous logic design and physical layout are accomplished on a design workstation introduced by Valid Logic. SCALDstar combines monochrome and color CRT displays, with design parameters available to both. When the cursor on the logic diagram is placed at a particular location, the layout display cursor moves to the corresponding circuit elements.

A self-contained 16-bit "mobile" microcomputer that weighs 9 lb and can operate up to 8 h on its rechargeable batteries was shown by Gavilan Computer at the spring Comdex conference. User interface is via an integrated touch panel that moves a pointer on the screen to the file or item desired. Price for a basic system will be under $4000.

Microcomputer interface to major mainframes is accomplished by Tab Products on its System 800 and 1600 desktop computers through combined bisync and async transmission capabilities. This eliminates the need for dumb terminals and frontend controllers.

Ruggedized data and program storage systems for portable, mobile, remote, and difficult environments, introduced by Targa Electronics Systems, are designed around removable bubble memory cartridges. Present cartridges contain 256K bytes, but the company foresees 1M byte in future cartridges.

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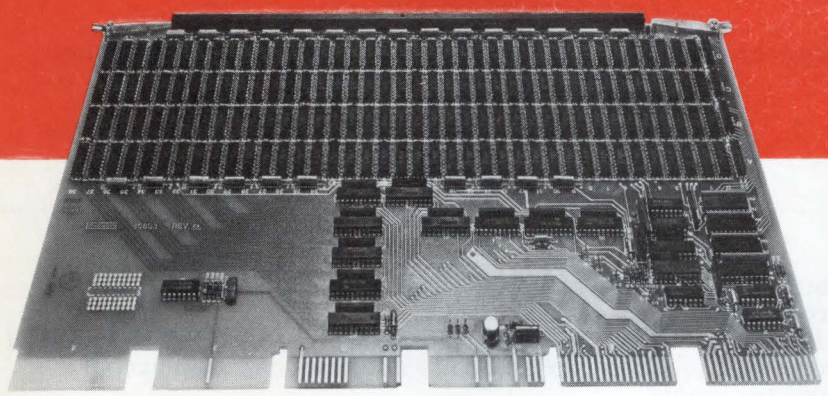

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PDP-11	DR-214	hex	1.0 MB
PDP-11	DR-144	hex	256 KB
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VAX-11/780	DR-178	extended hex	512 KB
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DECSYSTEM 2020®	DR-120	extended hex	256 KB

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Dataram also provides core ADD-INs, core and semiconductor ADD-ONs, memory system units, memory management, and a wide range of memory-related accessories for DEC users.

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CIRCLE 5

COMPUTER DESIGN®

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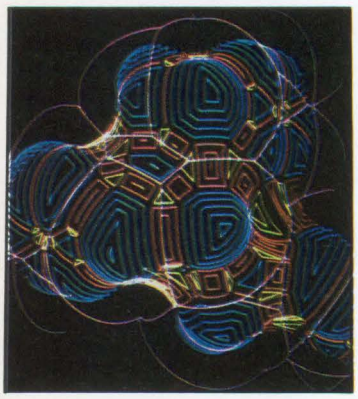
SIGGRAPH'83



78 Sophisticated computer graphics and interactive techniques are becoming indispensable in applications ranging from CAD/CAE and robotics to image synthesis and office automation. At its 10th annual conference next month, ACM's Special Interest Group on Computer Graphics will size up the scope of graphics technology today and forecast what is shaping up for tomorrow.

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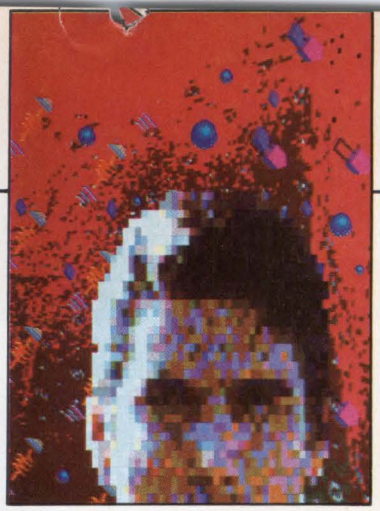
June 1983



This month's cover was created by Mark Lindquist on the Digital Effects Video Palette III.

Special report on semiconductor memories

149 New technologies and approaches to memory have surfaced in the last few years. This month's "Design Frontier" report examines some of these developments. The staff report explores the directions being taken by nonvolatile memory development. Two other articles deal with particular memory devices—one with a FIFO buffer and the other with a new EEPROM. Another report deals with a virtual memory management chip.

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Editorial reviewers for parts of this issue:

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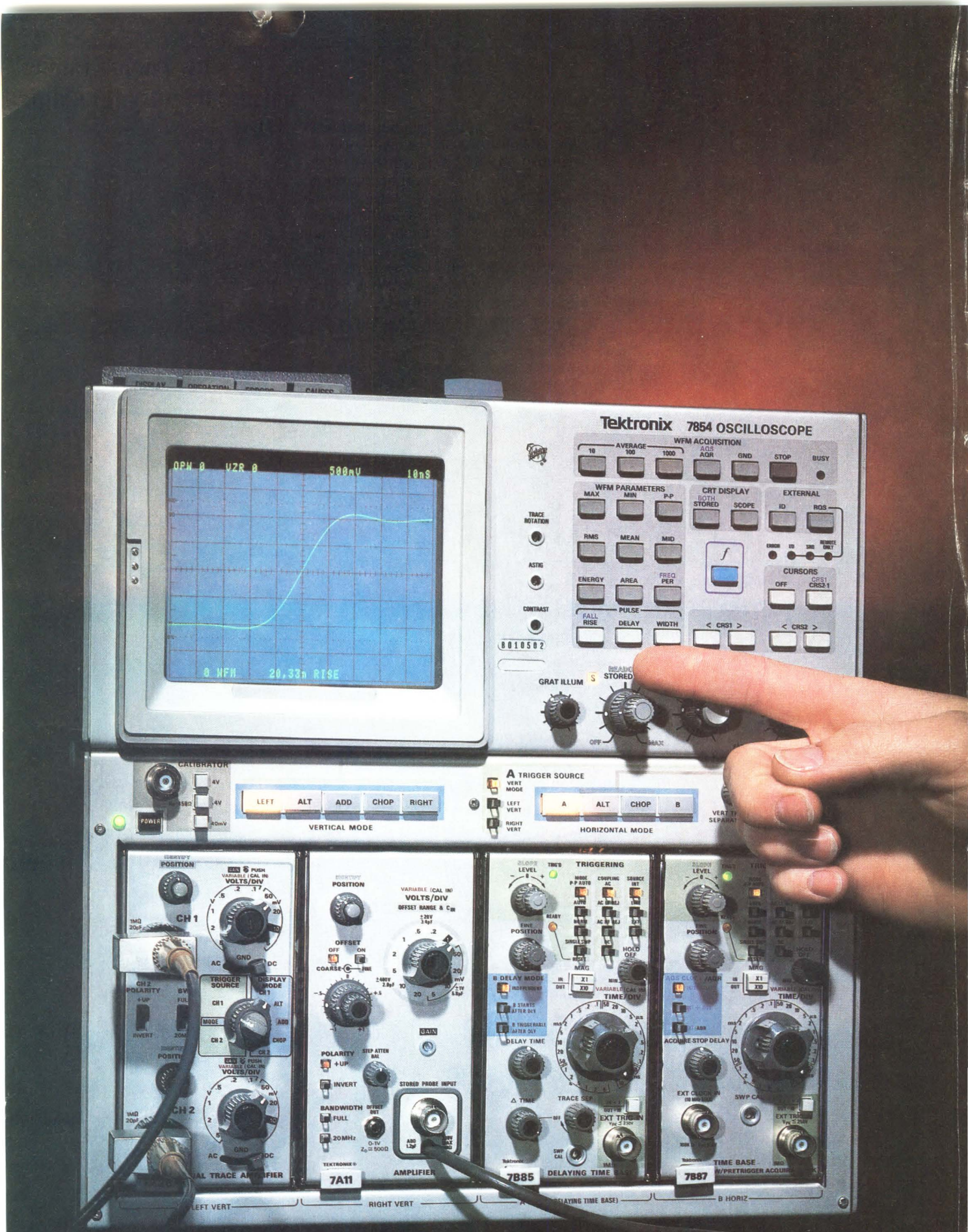
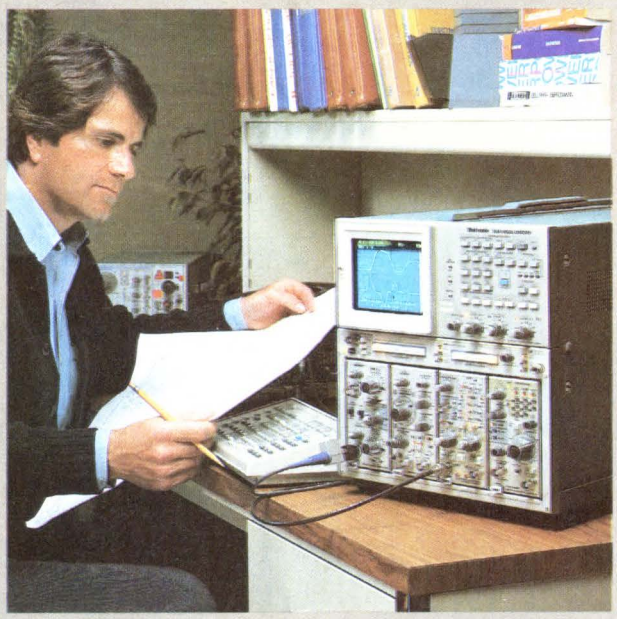


Precise answers instantly: now waveform measurements are automatic!

Now you can cut from minutes to seconds the time it takes to perform most common waveform measurements. By automatically performing all routine measurement tasks, the Tek 7854 minimizes errors and gives you more time for more productive activity.

Touch a front panel key and the 7854 digitizes repetitive signals up to 400 MHz. Stores them. Measures them. And displays the answer. For any rise time measurement, for example, you need only press two keys—AQR and RISE—to consistently obtain a precise, repeatable answer on-screen. There is no painstaking set-up, no decision-making, no mental calculation required.

Time savings and risk reduction are even more dramatic in more complex tasks, such as calculating the area under a power curve or determining instantaneous power from current and voltage waveforms... both the work of a few seconds on the 7854.



You can develop your own measurement routines using the companion waveform calculator. You can make virtually any sequence of procedures automatic, then leave operation to lesser skilled operators and technicians. You can even connect the 7854 to host computers and mass storage via the standard IEEE-488 interface bus.

More than 30 plug-ins let you reconfigure capabilities at will. Like all Tek 7000 Series scopes, the 7854 keeps expanding in value. Add high-sensitivity differential amplifiers. Comparators. Counters. Spectrum analyzers. Or sampling plug-ins that let you digitize repetitive signals up to 14 GHz. At any time, you can add new performance at a fraction of the cost of a monolithic instrument.

Allow yourself more time for creative problem-solving. In this era of hand-held calculators, it's about time you let the 7854 begin making your life simpler and your time more productive. Call your Tektronix Sales Engineer today!

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CIRCLE 8

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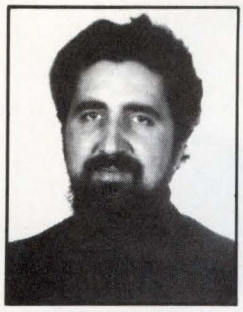
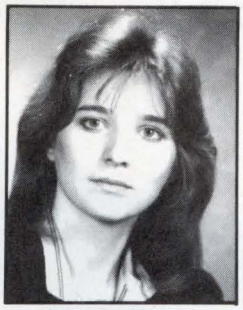


Nicolas Mokhoff



Malinda Banash

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Lauren A. Stickler

In the increasingly complex computer product marketplace, the need for discriminating magazine editors is growing. Designers and integrators are demanding concentrated editorial coverage of their specialties as well as timely reports on emerging technologies and applications.

Few technical publications can continue to do the job effectively without improving their editorial staffs' technical expertise. New sister publications such as *Telecommunication Products + Technology*, coupled with extra issues of *Computer Design* on automation & control and office system design, underscore the need to continuously upgrade and expand our staff. Our stringent hiring requirements ensure that you will be served by editors of the highest caliber. To meet your system design needs, *Computer Design* has always been written by designers and integrators for designers and integrators.

That is why, at this time, we are very pleased to introduce a new senior editor who has been in the trenches with you. Nicolas Mokhoff, both design engineer and accomplished writer, is heading up our new field office in New York City. From there, he will be in constant contact with companies in the North Atlantic states and through the Southeast into the Midwest. Joining Nicolas on our editorial staff is another engineering graduate, Malinda Banash. Malinda is a member of the IEEE Computer Society and the Society of Women Engineers. As assistant editor, she will be responsible for technical support of the editorial staff here in Littleton.

We are also very pleased to announce that two fine journalists who carry impressive publishing credentials are joining the copy-editing staff. Leslie Ann Wheeler and Lauren A. Stickler will assume the important task of maintaining the standards and editorial quality of our magazine.

Good people . . . people who share your interests . . . are playing an important role in keeping you up to date with all the advances within the computer based system design market. If you get a chance, drop them a line or call them with some important industry news or applications.

Ronald W. Evans
Publisher

Finally, a single source for multi-processo designed for OEMs and systems integrator Now that's intelligent.

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Intelligent Systems introduces the Datavue multi-processor, multi-user computer system.

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Advanced systems architecture delivers stand-alone performance. For advanced applications—decision support systems, office automation, management productivity, and even process control—Datavue provides a simple computing environment with a dedicated computer for each user (or control application).

Up to eight computer cards can be inserted in the Datavue system which resource shares mass storage and common I/O. Each user gets a full microcomputer with a Z80A, 64Kb RAM, and CP/M* 2.2. As a result, all users get stand-alone performance with the economies of a multi-user shared resource system.

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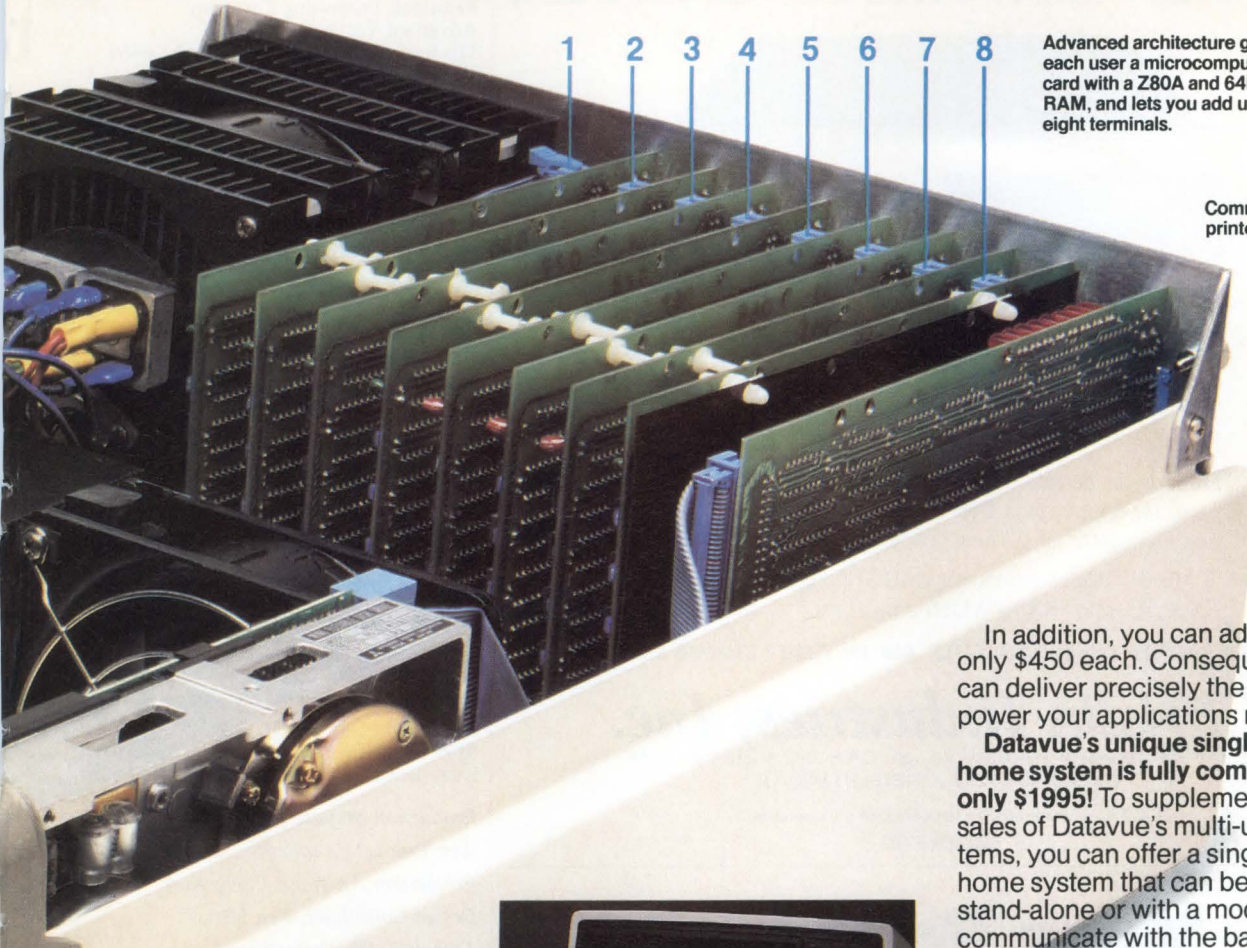
Add intelligent terminals to meet your customers' needs. Since 1973, Intelligent Systems has been a world leader in designing and manufacturing color graphics terminals. Now, you can profit from our expertise with: The Intecolor 2405, the indus-

ulti-user computer systems



Advanced architecture gives each user a microcomputer card with a Z80A and 64Kb RAM, and lets you add up to eight terminals.

Common Centronics printer port.

In addition, you can add users for only $450 each. Consequently, you can deliver precisely the computing power your applications need.

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That's Datavue multi-processor, multi-user systems. That's Intelligent Systems.

More information. Datavue is shipping now. OEM contract discounts are available. And a limited number of dealerships are open. For details, contact Marketing Communications at 404/449-5961, TWX 810 766 1581.

DATAVUE™ 132C

try standard ANSI color terminal; only $1295. The unique Datavue 132-column monochrome terminal for spreadsheet applications; only $1795. And the Intecolor 8301R, an advanced, dot-addressable, color graphics terminal; only $3995.

Since you contract with a single vendor, you can mix and match terminals and get excellent product discounts—increasing your profit margins.

Intecolor 8301

Datavue price/performance wins, especially with heavy compute requirements. For example, a four-user system with a full microcomputer for each user is only $7045—or *only $1762 a user!* This four-user system includes:

- 4 microcomputers, each with a Z80A, 64Kb RAM, 4Kb EPROM, and 2 RS232-C ports
- 12Mb 5¼" Winchester hard disk and a 1Mb floppy for back-up
- Shared resource management card for mass storage
- Centronics parallel printer port which all users can access
- CP/M 2.2 operating system, compatible with the world's largest library of off-the-shelf software.

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*CP/M is a registered trademark of Digital Research, Inc.

CIRCLE 9

COMPUTER DESIGN

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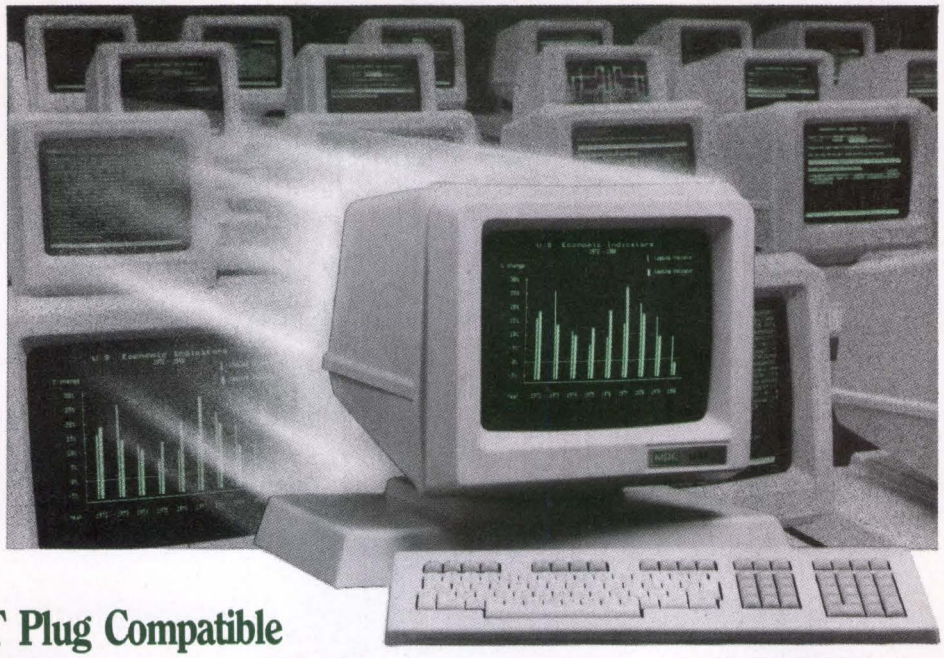
CIRCLE 12

MPC Puts the Big Picture in Graphic Detail



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Not only does the 1200/1250 Series deliver superior emulation of the DEC VT models, but they offer the extras you've been looking for . . . like an ergonomic design with video and screen enhancements. Any way you view it, the heavily featured MPC 1200/1250 Series gives you the DEC™ VT alternatives worth looking into!

Available Now!!!

Why wait through long factory lead times? Your local MPC distributor can deliver your MPC 1200/1250 DEC™ VT plug compatibles, loaded with extras, from stock today.

A worldwide distribution network provides sales and service for the MPC family of sophisticated CRT terminals. Call (703) 430-1800 for the name of your nearest distributor.

You'll See Built-in Extras at no Extra Cost!

MPC's 1200/1250 Series brings you the costly options of other terminals as standard features. Take a closer look at the extras in MPC's new generation of engineering excellence:

- **Superior Monochrome Graphics.** Color Optional; 1250 Model
- **640 x 480 Readable bit map**
- **24 Programmable Function Keys,** plus programmable numeric keypad, store up to 36 individual function sequences in NVR.
- **Eight pages of Video Memory**
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- **40, 80 or 132 Columns,** user selectable
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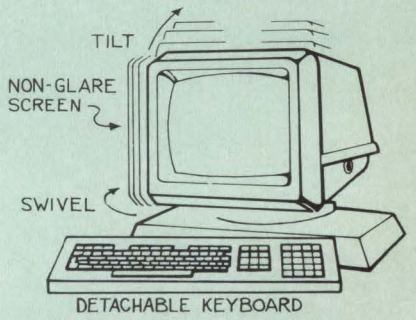
- **Enhanced Scrolling:** Jump, smooth, and bi-directional
- **Selectable Video Attributes** and adjustable brightness controlled from keyboard
- **Two RS-232 Ports**—bidirectional and independently controlled
- **14" Non-Glare Screen**
- **Detachable Keyboard** meets European DIN specs.
- **Soft Set-Up Plus Host Configurable**
- **UL Listed, FCC & CSA Approved**



Ergonomics: All MPC terminals offer an enlarged non-glare screen and adjust to individual preference by rotating 60° in either direction or by tilting up to 15°. The low profile, detachable keyboard meets new European DIN specifications.

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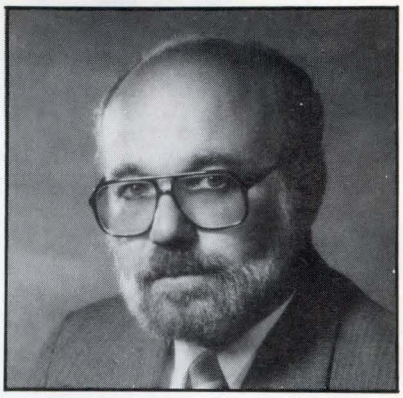
CIRCLE 13

RALLY 'ROUND THE ECONOMY

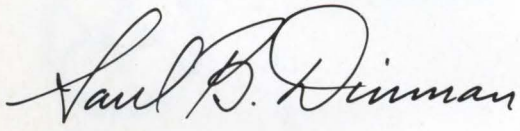


Some 18 months ago, the Reagan Administration initiated Project Exodus to stem the flow of American technology into the Soviet Union. This project, and its attendant Controlled Commodities List (CCL) that the U.S. Department of Defense maintains as a classified document, has been a thorn in the side of many high tech manufacturers. Not only are the CCL's contents unavailable to the average industrial or commercial system manufacturer, but the enforcement of Project Exodus—dependent upon the interpretations of as many as five separate government agencies—has proven to be capricious at best.

Most of our industrial and commercial computer system manufacturers rely on exporting 30% to 50% of their business to Europe. As the United States climbs out of the recession, Europe will not be far behind, requiring more U.S. exports. This export business will be vital to the next U.S. boom period. However, Project Exodus has the potential to seriously hamper this plan, and even to finish off some of the smaller recession-starved companies eagerly awaiting the coming boom.

Originally, Project Exodus was implemented as a panic measure and is valid only through the summer; it will come up for renewal in the fall. Since its inception, there has been vigorous debate between high tech "have" and "have not" states. The high tech state legislators have argued with Congress to clean up the bill's provisions; they have also spent a great deal of time helping some of the smaller manufacturers fight the bill's fluctuating provisions regarding company exports. Legislators from non-high tech states have argued that though the Soviet Bloc is behind us for the moment, we should not indirectly provide them with our technology through some of our European trading partners who do not object to doing business with the Soviets. These same legislators, however, argue that the Soviets are now technologically ahead of us and that, in order to catch up, we must again embark on a technological spending binge like we did in the Sputnik days. A question that defies logic is, If the Secrecy Act's provisions prevent most manufacturers from finding out the CCL's contents, why don't they also prevent truly classified technology from leaving this country?

As the debate over Project Exodus' renewal warms up—it is already becoming hot in many of the high tech states—it would behoove all of us to make our voices heard by our congressional representatives. We should demand at least sensible provisions for the enforcement of such a bill, if not seek defeating the measure on the grounds that normal secrecy provisions should be sufficient to protect us from technology leaks. If our voices are not heard, the fallout predicted because of overcrowding in the marketplace may just come sooner than we expected—and for an entirely different reason.



Saul B. Dinman
Editor in Chief

A reminder to those of you who have not responded to the readership study in Computer Design*'s Automation & Control Premier Edition: please turn to p 174 of that issue, answer the questions on the Reader Inquiry Card on p 181, and get it back to us. We need your valuable feedback to help us plan next year's editorial calendar. Thank you.*

Best Technical Article of the Month—November
"Understanding the High Speed Digital Logic Signal"
Malcolm Davidson, Heaviside Industries, Ltd

This article will now compete with other monthly winning articles for the 1982 editorial excellence award.

Nice try,

Well, Motorola's still trying to get the 68000 System together.

Unfortunately, it's not only too late. It's too slow.

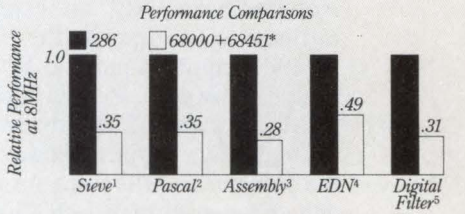
THE 68000 WAS FAST. BUT THE iAPX286 IS A WHOLE LOT FASTER.

The new 286 is three times faster than the 68000. Even our extremely cost-effective 186, which integrates 20 LSI devices into one chip, outperforms it. (Sorry, Motorola.)

And you can forget what Motorola's been saying about memory. The 286 not only addresses 16 Megabytes of physical memory, it addresses 1 Gigabyte per user of virtual memory.

Unlike the 68000, the 286 even has the memory management, the protection, and the operating system interface functions built on to the chip itself. So you get software protection and software-in-silicon with no external components to drain the juice out of your CPU.

But there's a lot more to the iAPX86 family than performance.



*Performance adjusted to reflect indicated system configuration. Details available from AMD. [1]"A High Level Language Benchmark," Byte, Sept., 1981. [2]"A Performance Evaluation of the Intel iAPX 432," Computer Architecture News, June, 1982. [3]"16 Bit Microprocessor Benchmark Report," Intel Corporation, 1981. [4]"16 Bit Microprocessor Benchmarks," EDN, Sept., 1981. [5]"Digital Filter Implementation on 16 Bit Microprocessors," IEEE Micro, Feb., 1981.

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THE WORLD'S FIRST PARTNERCHIP.™

The Partnerchip gives you two responsible domestic sources:

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(Motorola has their second sources spread out from here to Tokyo. Not one comes close to offering you the entire product line.)

Together, we have more peripherals on the shelf than any other 16-bit family.

And since we've signed an agreement to exchange parts, masks and R&D, we'll be delivering a lot more than promises over the next 10 years.

So if you want the system that'll keep you way out in front, climb aboard the Partnerchip.

It's a lot better than what Motorola's peddling.

The iAPX86 People.

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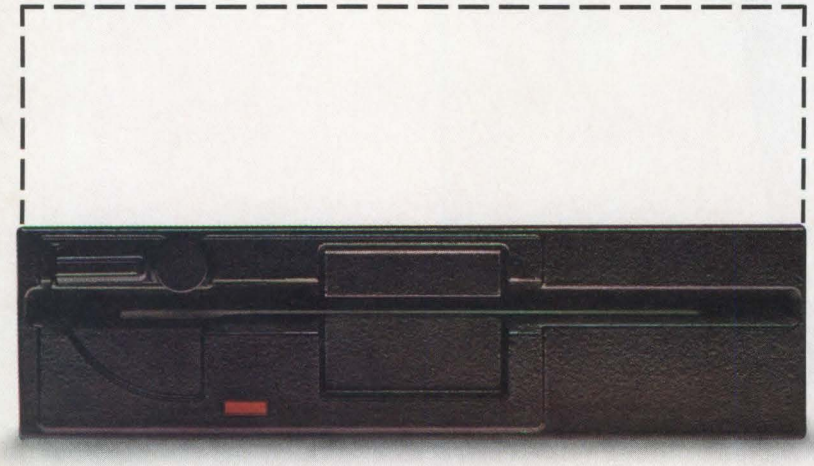
CIRCLE 14

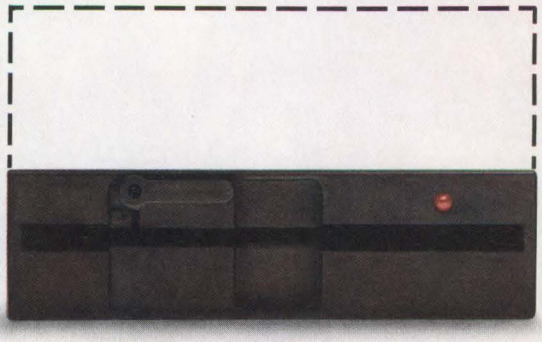
SHUGART DRIVES.

1/2 OFF.

SA810



SA455



No, it's not a sale.

It's just a way of telling the world that Shugart now has a whole line of half-height floppy disk drives.

Half of which are our new 5.25" Minifloppies. Or, if you will, mini Minifloppies.

The SA455/465 double-sided drives.

Both offer improved performance and reliability over conventional minis. And more design flexibility, because of a technology that demands only half as much space.

So you can create smaller, more competitive systems. Or build more storage capacity into existing designs by putting two drives in the space of one.

Moreover, both the 48tpi SA455 and 96tpi SA465 are compatible with their relatives, the industry standard SA400/405 and SA410/460. So there's no need for a major revamping of hardware or software.

And once they're in place, you'll find they use 45% less power than ordinary 5.25" drives. While delivering snappier access times (in the case of the SA465, 3 msec track-to-track). And even better reliability—an impressive 10,000-hour MTBF. A 25% improvement over most full-height drives.

Then there's the other half of the story. Our new 8" half-heights, the SA810 single-sided and SA860 double-sided floppies.

They too give you more performance and reliability out of a lot less hardware.

They too eliminate major redesign. Since the controller interface, mounting holes and internationally recognized DC power supply requirements are fully compatible with the industry standard SA801 and SA851 8" drives.

The SA810/860 are also the only half-heights offering true electrical compatibility with the existing user base of over 4 million 8" disk drives.

And all our half-height drives feature rapid-start direct drive DC motors for better reliability, speed control and longer media life than any other floppy disk drive.

Of course, Shugart still offers the industry's most complete line of full-height floppy and Winchester drives. Plus an extra-economical 2/3-height Minifloppy,™ the entry level SA200.

And our newest small wonder, the SA300 3.5" microfloppy.

All backed by the largest and most experienced engineering, sales and service organizations in the business.

Which is our way of giving you more.

Even if it's only half as much.

For more information, contact Shugart Corporation, 475 Oakmead Parkway, Sunnyvale, CA 94086, 408/733-0100 (Hamilton/Avnet, authorized distributor).

Shugart

Right from the start.

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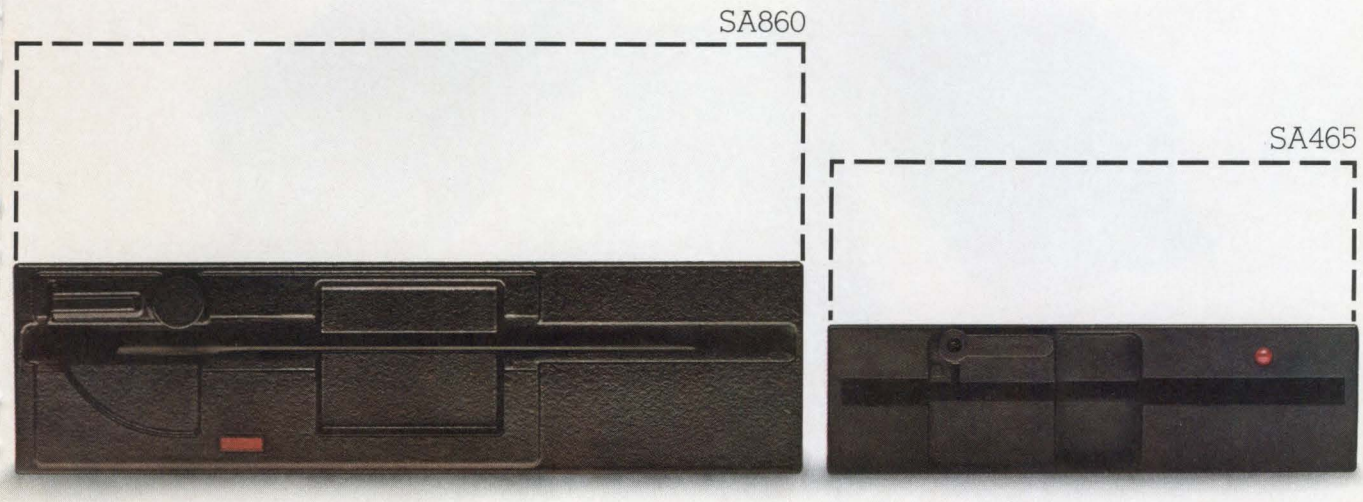

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FAMILY PLANNING.

Family planning. It's the way to get flexibility in E^2 designs. And it's why SeeQ's "B" family of latched E^2ROM makes it practical to plan today's memory needs around a technology that's growing up fast.

For starters, the 52B13 (16K), 52B23 (32K), and 52B33 (64K) all offer fast 1 msec write times, 200 ns access times, and standard JEDEC bytewide pinouts. So expanding from 16K to 64K is a simple upgrade. Not a complex redesign. And with onboard latches (another "B" family standard), E^2 designs are easy to implement as well as alter.

$6, $15, $40—all in the family.

At SeeQ, we use the most advanced technology to make E^2 more cost-effective. It's a family tradition.

Last year, our oxynitride process produced the world's first 16K 5V E^2ROM—eliminating all need for expensive high voltage circuits.

Today, our new 2 micron dry plasma process makes our 64K 52B33 the right solution for all high-performance 16- and 32-bit microprocessor systems.

And this unique combination of technology and market demand will make our E^2 competitive with older nonvolatile technologies in half the usual time.

That's why by December you'll be able to get your hands on production quantities (25,000 units minimum) of our 64K 52B33 for only $40. Or our 32K for $15. Or our 16K E^2 for just $6.* Check that against EPROM prices. And check the coupon for a way to put our "B" family E^2 to work at December's prices right now.

And feel free to ask us for whatever else you need. Just call (408) 942-1990. Say you're a friend of the family.

I want to put SeeQ's "B" family E^2ROM to work in a design today. Send me the parts indicated. My check, made out to SeeQ Technology, is enclosed.
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(Limit one of each density per person) __ My check is enclosed, but I have an idea for E^2 that can't wait. Please have a sales representative call me at (_____) _____. The best time to call is _____.

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Orders accepted with this coupon (or photocopy) only. Limit one part of each density per person, plastic packages.

seeQ

*Effective for orders on or after December 1, 1983, in quantities of 25,000 or more, plastic packages.

LETTERS TO THE EDITOR

Plugging in poses problems

Designing computers presents a problem that appears to have been ignored by writers, designers, and manufacturers. This problem has continued for the 20 years I have been involved with evaluations and installations. Within clusters of equipment, each component needing power is uniquely powered, requiring a separate power receptacle for each device.

Few manufacturers or suppliers configure centralized, fused power for their particular sets of equipment in total. Some do not have common plugs within their configurations. A 4-plex should be able to configure a small expandable system of CPU, disk, printer, and modem, except that the modem could have a power converter and possibly a channel alignment device. The converter's construction usually denies access to at least one other outlet; in addition, the channel device is uniquely powered—hence, you're short two outlets. Want to add more peripherals? Each will take at least one additional outlet.

Looking behind some of today's "PCs" and "workstation" configurations, you will find a jungle of power cords, power strips, I/O cables, and a back wall of 2- to 10-horsepower outlets. Most buildings today were not designed to support the recent burst of PCs and terminals. In fact, try to convince a non-computer oriented electrical engineer of your requirements for power and cable routes. Lots of luck! Few, if any, buildings will be torn down and rebuilt to support the computer world. However, some are being built or modified to fit the need.

In my opinion, the logical, easiest, and best solution to this aggravation is to have a fused power block on a central unit—with the possible addition of integral isolation transformers. At the very least, it sure would be nice to have a standards group evaluate this very definite problem.

Carl D. Ricketts
Boeing Computer Services
PO Box 24346, MS 6R-02,
Seattle, WA 98124

Ethernet eluded

I read with interest your article on local area networks ("Untangling Local Area Networks," Richard Parker and Sydney F. Shapiro, Mar 1983, p 159). I was disappointed, however, to note that there was no reference at all to Ethernet products that are available from Digital Equipment Corp.

DEC is the only computer vendor today that can provide customers with a complete system level networking solution based on Ethernet technology. In May 1982, we announced an entire family of Ethernet products, with product availability to be specified over the next three years. Our initial Ethernet hardware and software products went into field test in Oct 1982 and we began delivery in May 1983. We intend to make available additional Ethernet products that will provide the capability to connect all of our CPU families (from Professional 300 personal computers through VAX and DEC20 mainframe computers) to Ethernet with appropriate software.

Today's products offer system implementers the same datagram-level service on Ethernet hardware that is available from other vendors. At the same time, however, it is also possible to use our company's DECnet hardware and networking software to construct an Ethernet network with system level capabilities.

The DEC Ethernet products are available with DECnet networking software. With this combination of hardware and software functions, it is possible to copy files, send electronic mail, create and access distributed database management systems and Datatrieve files, access remote directories, and log onto other systems.

Additionally, the capabilities of a local area network Ethernet are integrated with our wide area networking services, making Ethernet a segment of a much larger network. Today, inside DEC, several Ethernets operate as parts of the DEC engineering network that consists of over 200 computers in locations from California to England.

Ethernet functions offered from DEC are also integrated with SNA and X.25 gateway capabilities. This allows an Ethernet user to access corporate data bases through an SNA gateway or send messages across X.25 public packet-switched nets.

Thomas D. Rarich
Digital Equipment Corp
1925 Andover St
Tewksbury, MA 01876

Unfortunately, the parts played by both DEC and Intel in the development of Ethernet were not adequately emphasized in this article. Although both were mentioned, possibly further discussions would have made the article more replete.

The Alps Advantage in 5¼" floppy disk drives:

Miniaturized for less space, more storage capacity. Since 1948, miniaturization has always been an important part of The Alps Advantage. In our 5¼" floppy disk drives, the advantage is immediately apparent: you can double (or quadruple) your storage capacity in the same space! And it's all done without any sacrifice of design or performance features:

Brushless DC motor. Models available with standard brush motor, or new brushless DC motor with 10,000 hours life rating and higher operating reliability without brush noise.

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High speed access time. Choice of 5 or 12 millisec. track-to-track access time, achieved by the use of a unique steel belt head carriage design.

Up to 500 Kbytes storage capacity. Single or double side, single or double density models. 48 TPI track density. Head load time 35 millisec. FM (single density) or MFM (double density) recording method.

Automatic disk eject. Media removal is fast, smooth and easy.

Simple design, high reliability. High precision ultra-thin stepper motor is combined with a unique hub collet configuration in a simple, reliable design for improved accuracy in head positioning and media clamp centering.

Improved disk life. A ceramic based magnetic head protects the media from excess wear and provides increased accuracy of data readout.

World-wide acceptance. Many thousands of Series 2000 drives have been delivered to OEM manufacturers throughout the world. You can easily learn what they already know about The Alps Advantage–just write or call today.

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OUR SMALLEST ACHIEVEMENT IS THE INDUSTRY'S BIGGEST SUCCESS.

The Tandon 8" and 3½" Floppy Company is the world's largest producer of 8" ThinLine™ drives.

And now we're ramping up for high volume production of single and double-sided 3½" drives.

When we introduced the half-height 8" floppy drive, we expected system designers to go wild over it.

You did. Some of you stacked two of our drives to double system storage to as much as 3.2MB without increasing system size. Others took advantage of our small achievement to reduce system size instead.

Whatever you've done with our ThinLines, we want to thank you for having the confidence in them to give us an overwhelming lead in the half-height 8" market.

Now we're using our experience in making drives small to make them even smaller. Our new 3½" drives are now in production in four versions. 500K byte single-sided and 1MB double-sided Tandon interface models. And Sony interface-compatible drives of the same capacities.

We plan on becoming the world's leader in 3½" the same way we became the world's leader in half-height 8." By focusing our energies on building more drives, better, at a lower cost than anyone else.

Like all Tandon companies, we start with a high degree of vertical integration. And an aggressive commitment to R&D no one can match.

We've also established ourselves in a brand-new facility with all the latest manufacturing and test equipment. So we can triple our current leading monthly production rate while ramping up to meet the burgeoning 3½" market.

Just because we've become a success by thinking small doesn't mean our plans are modest.

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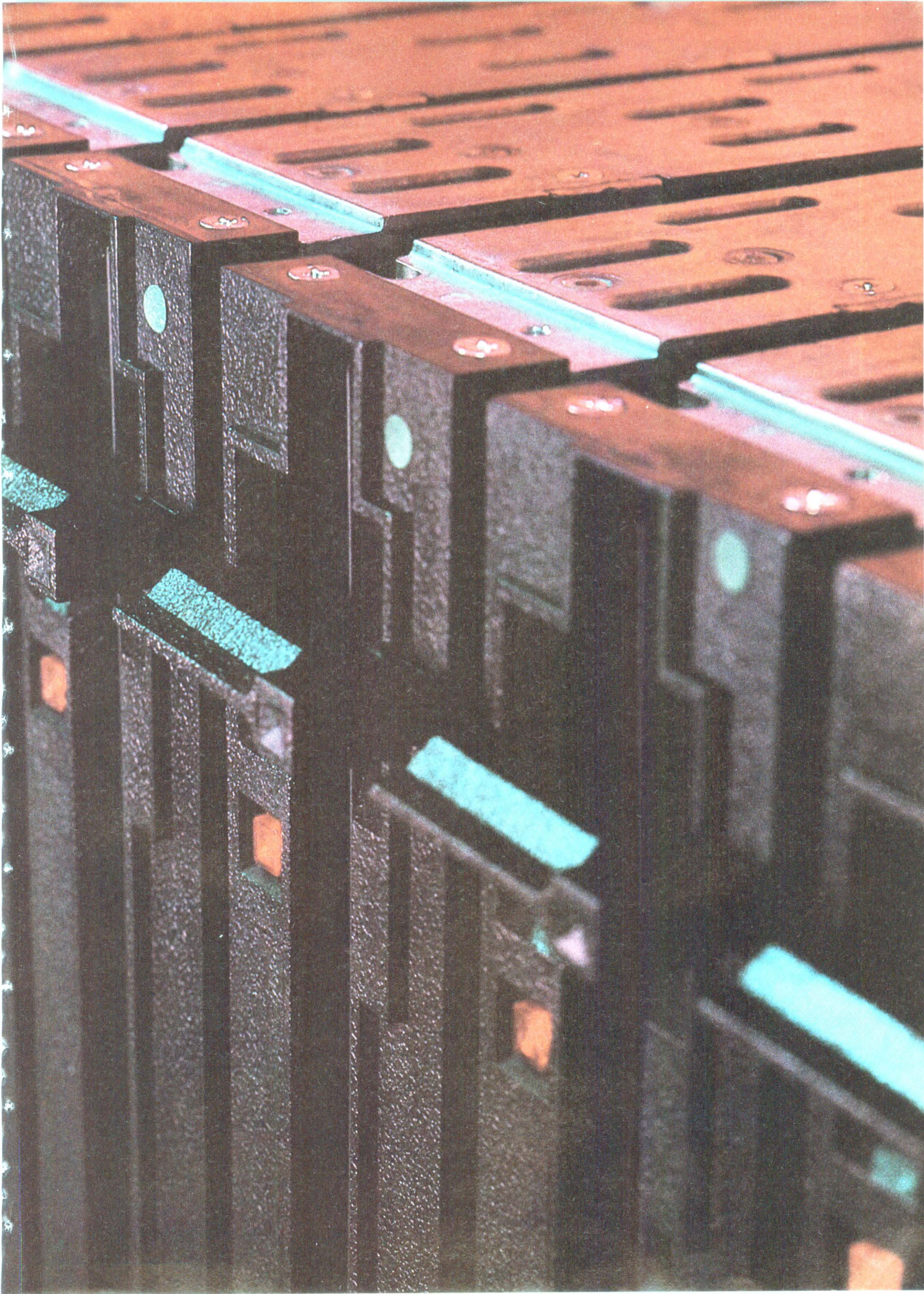


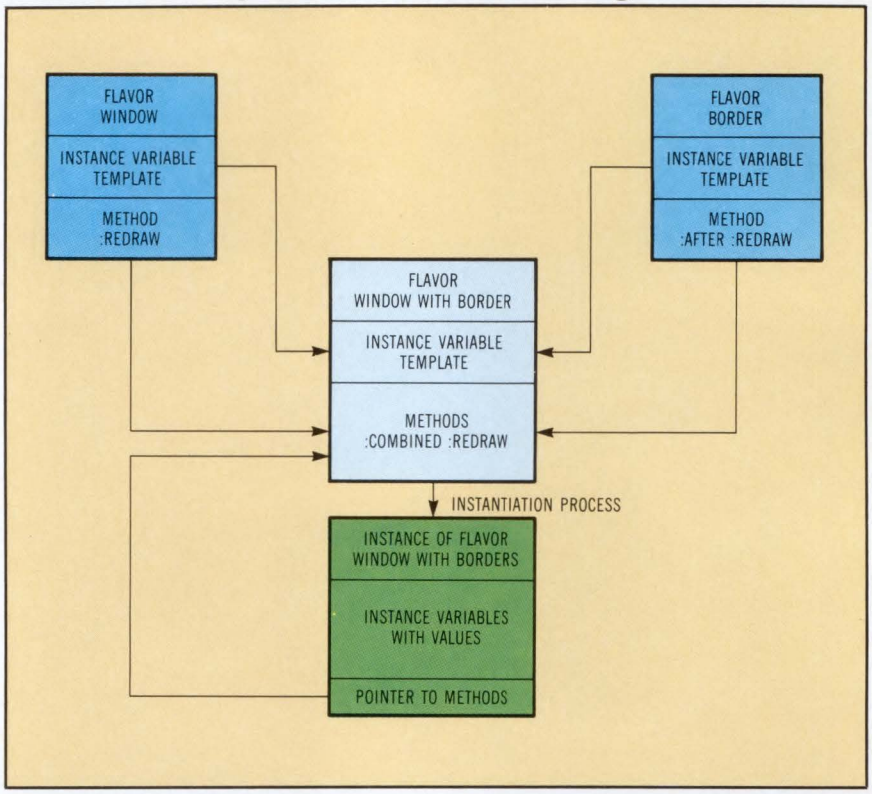
Programming language adds flexibility for artificial intelligence

For systems that manage large data bases with complex control logic, such as expert systems or other phases of artificial intelligence, Symbolics, Inc has integrated attributes of Flavors into its Zetalisp compiler. Flavors is an object-oriented programming language used on the company's 3600 computer system (see *Computer Design*, May 1983, p 280). The Flavors system allows designers to bind operations and data structures together and to construct well-defined message paths for user interfaces.

In general, the point of object-oriented programming is to construct new data types by defining the data structures associated with the type as well as defining generic operations valid for those data. Specific instances of these types are then created. Each instance maintains local state information and uses the defined operations to interact with the user. Thus, data and procedures are encapsulated as objects of the new data type. This method shields users from the actual implementation and permits programs to be easily developed and maintained.

In this implementation of the Flavor system, flavors are the abstract data types and methods are the generic operators. Objects are flavor instances that are manipulated with messages requesting specific operations. Instance variables hold local state information for a flavor instance. Applications are implemented by first defining the flavors in one part of the program and then creating flavor instances in another.

New flavors can inherit methods and instance variables from existing flavors, or they can explicitly define unique methods and instance variables. In either case, designers explicitly declare the relationships among flavors. For example, certain flavors can be specified in order to define others. An inherited method can be executed conditionally, depending on the flavor declarations. Method definitions of new flavors can override, augment, and otherwise change the methods of existing flavors.



Using Symbolics' Flavors system, designers can blend the attributes of many data types through a process called instantiation. Here, the flavor types "window" and "border" combine to form a new flavor, "window with borders."

The Flavor system bases its type and method dependencies on a graph structure (multiple parents) that allows arbitrarily complex flavors to be created while still retaining modularity and ease of maintenance. After flavors are defined, flavor instances are allocated and used with a constructor function. Flavor definitions can contain the local variables' initial values. In many cases, initial values can also be declared in the call to the constructor. The system provides accessor methods for instance variables whose values are externally available to the instance. It also provides mutator methods for instance variables that can be changed by other parts of the program.

Once flavor instances are created, they either receive messages that pass arguments to local variables or they request procedure results. In fact, operations are implemented as function calls that accept arguments.

An example of how the Flavors system works is shown in Zetalisp's user defined condition system. The condition system detects exceptional events that occur during program execution and provides a means to respond to those events with user supplied code. Each standard class of events (eg, errors such as dividing by zero) has a corresponding flavor called a condition.

Reporting an event occurrence creates a condition object that is an instance of that flavor. These instance variables contain further information about the event, such as the condition's various parameters. A signaling mechanism then searches for a user supplied code that assumes control. This handler accesses the instance variables for that condition object. The handler can

(continued on page 30)

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CIRCLE 19

Programming language

(continued from page 28)

either continue execution (perhaps after repairing a piece of code), or retry the operation at a specified point earlier in the program.

Designers can either specify conditions that are very specific to a particular set of circumstances or others that are more general. Also, they can choose the level of response to conditions according to a particular application's needs.

Custom user interfaces are also implemented with windowing techniques based on the Flavors system. Designers mix their defined flavors with other flavors contained in the window library. Each window is a Zetalisp object and an instance of some flavor (momentary, multiple choice, or multiple menus). To manipulate a window, a program sends it messages. These messages can alter the appearance and shape of that window, control cursor position, and perform I/O operations. Windows also understand many graphics operations that handle drawing points, lines, and regular polygons. The user supplied flavors control or modify the predefined flavors' behavior to suit the specific application. **Symbolics, Inc**, 257 Vassar St, Cambridge, MA 02139.

Circle 240

Setting sail against the software pirates

Picture this: an antiseptic, $10,000, state of the art desktop microcomputer. Now, imagine it plastered with all manner of odd-sized authorization stickers so that it looks like the cab door of an interstate tractor trailer rig. Sound farfetched? Not so. This version of "computing 1984" is exactly what is envisioned by Whitesmiths, Ltd, the Concord, Mass software house specializing in C-related products.

The stickers are there to prevent software piracy. They authorize an individual computer to run a specific copy of a program. In a stratagem that depends equally on users finking on their fellows, customers defacing their expensive hardware, and the establishment of legal precedents covering "licensing under copyright," Whitesmiths hopes to find a safe harbor from software pirates.

"For every legitimate copy of most popular software packages, between 4 and 10 pirated copies are in circulation," claims Bill Plauger, Whitesmiths' swashbuckling president. He adds that, as a result of this piracy, software developers are losing up to 50% of their rightful earnings. According to Plauger, this situation is threatening the economic health of many software producers.

(continued on page 32)

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CIRCLE 21

Software piracy

(continued from page 30)

Plauger feels that the standard solutions—end-user licenses and patents—are ineffective deterrents to piracy. The former are cumbersome and expensive to execute, the latter of questionable legal validity. So, what to do?

For Whitesmiths, the solution is licensing under copyright. In theory, this tactic relies on existing copyright laws, as amended in 1980 to cover computer programs. These amended laws protect the form or expression of ideas (in programming languages or binary code) rather than the underlying logic or algorithms. It is Whitesmiths' opinion that the amended copyright laws are stringent enough to facilitate the prosecution of commercial pirates—those who copy for a profit. For the time being, disk duping user groups and computer science students are safe.

By extending, or licensing copyrights to OEMs and end users, the rather limited rights of pure copyright are expanded. This expansion allows users to make and retain limited copies of programs on magnetic media. For instance, users may make one authorized copy of a program for storage within a specific computer, and archival copies for private use. The catch, however, is that a specific computer is authorized to run each program.

Thus, a user cannot buy a copy of Whitesmiths' UNIX-like operating system, Idris, and lend it to a friend. Nor can a user, in good conscience, copy a Whitesmiths program onto several mass storage units attached to different computers. Software can be bought and sold with hardware, however, and OEMs need not report such transfers. This last aspect of the plan greatly simplifies the OEMs' life.

The instrument of Whitesmiths' plan is the authorization seal (see Photo). This intricately drawn seal is sold with the software and must be promptly affixed to the machine on which the software will, forever after, run. The detailed and difficult to counterfeit seal carries two series of numbers, one of which identifies the product. The other series of numbers identifies the program that the machine to which the seal is affixed is authorized to run. In this case, a Whitesmiths cross compiler is running under RSX-11 with a POS-11 target.

The Whitesmiths seal, celebrating copyright from the age of calligraphy to computers, is designed to be difficult to duplicate.

The key to this software protection scheme—enforcement—seems also to be its Achilles' heel. The burden of guilt falls most upon users, for it is they who must bring violators to Whitesmiths' attention. In the *laissez faire* world that is microcomputing, it is questionable whether or not users can be imbued with so high a sense of duty. Part of the reason is that software producers have not, to date, been successful in convincing users that a $1200 floppy disk is really 10 times as valuable as a $120 floppy disk, and therefore worthy of protection.

In any case, Plauger is optimistic about the cooperation he will receive from his customers: "We are . . . so convinced that everyone else is as concerned about piracy as we are that we are asking everyone to participate." Plauger adds, "If our software is running on a computer that does not display an authorization seal, that software is probably not an authorized copy. I urge you to report such incidents to me." Plauger claims that he will vigorously enforce his ownership rights in court and exhorts other software producers to follow his lead by adopting a similar authorization seal.

Whitesmiths' attorney, Henry Dane, is more circumspect in his appraisal of the authorization seal program. He did not speculate on the likelihood of user cooperation, but he did emphasize that, in his opinion, the company is on firm legal ground where software copyright laws are concerned. Though unable to cite any recent legal precedents or litigation relating favorably to licensing under copyright, Dane has no doubt that Whitesmiths will get a sympathetic hearing in court if, and when, the time comes.

Though confident about cooperation, Company President Plauger is slightly less assured where legal

(continued on page 34)

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CIRCLE 22

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SYSTEM TECHNOLOGY/ SOFTWARE

Software piracy

(continued from page 32)

matters are involved. At a recent press conference, he said, "We know that we are taking some chances by pioneering this concept . . . [but] our attorneys assure us that we are in a good position. They say that you can recognize pioneers by the arrows in their backsides. I sure hope I dodge most of the arrows."

Whether on firm ground or pioneering, the Whitesmiths strategy for combatting software piracy is interesting on several counts. First, it illustrates the gravity of piracy, a problem that has even penetrated the highly specialized environs of Whitesmiths' market.

Second, this strategy demands customer accountability unheard of in any other buyer/seller relationship. Third, if it is to be viewed as anything more than an elaborate ruse, the antipiracy program will require considerable financial resources to support ongoing litigations.

In a practical sense, Whitesmiths' approach is most likely to serve as a deterrent to, rather than an ironclad prohibition of, commercial piracy. As Atari has shown in the microcomputer game arena, the best defense against piracy may actually be a boisterous offense. As the folks at Whitesmiths set sail to meet the software pirates, the first legal broadsides have yet to be fired.

—Chris Brown, Technical Editor

COMPUTERS

Supermini doubles performance

Highly pipelined parallel architecture, Advanced Schottky TTL, fast static RAMs in dedicated caches, and hardware design innovations including a "board-slice" floating point processor and separate address generator are key features of Data General's latest bid in the mainframe-class superminicomputer arena. While doubling the performance of its earlier high end MV/8000, the company has cut cycle time in the Eclipse® MV/10000 from 220 to 140 ns.

The 32-bit virtual memory machine gleans 2.5M-Whetstone/s single-precision and 1.9M-Whetstone/s double-precision performance for up to 192 users. This is backed by 16M-byte main memory, 18.5G-byte online storage, 4G-byte virtual address space, and 2G-byte program size. Cross development of AOS/RT32 realtime and AOS/VS virtual storage operating systems accommodates CAE and technical timesharing as well as real-time computational applications.

A bipolar bit-slice microsequencer directly accesses the writable control store every 140 ns. As an option, the control store expands from 4K to 8K words (425K to 850K bits), reserving 4K words for the computer's instruction set and 4K words for user-programmable microcode. Within the loadable store, field groups are assigned to control specific processing subsystems. This permits many hardware resources to be managed simultaneously with reduced microsequencing overhead.

A single-board integer processor performs the system's main arithmetic and logic functions, including 16- and 32-bit integer arithmetic, number shifting, and data translation/validation. It has a fixed-point ALU; 2-port, 32-bit register file; and 256-register scratchpad memory. The single-board processor executes macroinstructions like add, load, and store in one 140-ns cycle, offloading logic functions to other processing subsystems if necessary.

Under direct control of the microsequencer, the floating point processor operates synchronously with the integer processor, performing integer multiply/divide operations to offload that processor if directed. Two identical boards compose the floating point unit, which divides the execution task by using one

(continued on page 39)

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	Unit	Double Density
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Media		
Record Surfaces	2	
Tracks	80	
Recording		
Max Recording Density	Bpi	8946
Track Density	Tpi	100
Transfer Rate	bits/sec	250K
Access Time		
Average Access Time	msec	55
Track to Track	msec	3
Setting Time	msec	15
Average Latency Time	msec	100
Motor Start Time	sec	0.7 (min)
Disk Speed	rpm	300
Reliability		
Error Rates		
Soft Error		10^{-9}
Hard Error		10^{-12}
Seek Error		10^{-6}
Media	3-inch Cartridge	
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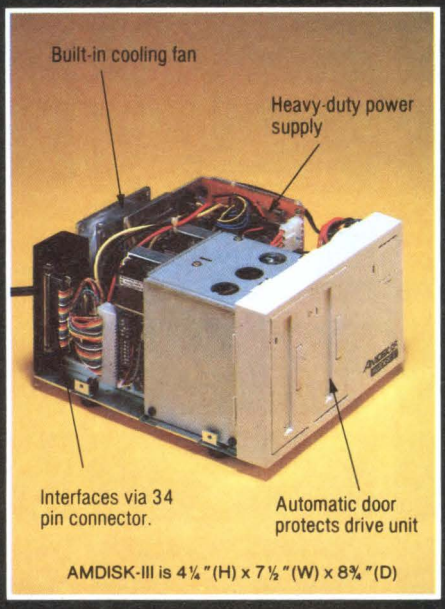
External Interface

Connector: 34-pin (Shugart)

Pin No.	Signal	Pin No.	Signal
2	Unused	20	Step
4	In use (option)	22	Write data
6	Drive select 3	24	Write gate
8	Index	26	Track 00
10	Drive select 0	28	Write protect
12	Drive select 1	30	Read data
14	Drive select 2	32	Unused
16	Motor on	34	Ready
18	Direction	1-33	Ground

NOTE: Single head per drive



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CIRCLE 24

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	IMS2620-12	120ns	190ns
	IMS2620-15	150ns	240ns
64K x 1	IMS2600-10	100ns	160ns
	IMS2600-12	120ns	190ns
	IMS2600-15	150ns	230ns

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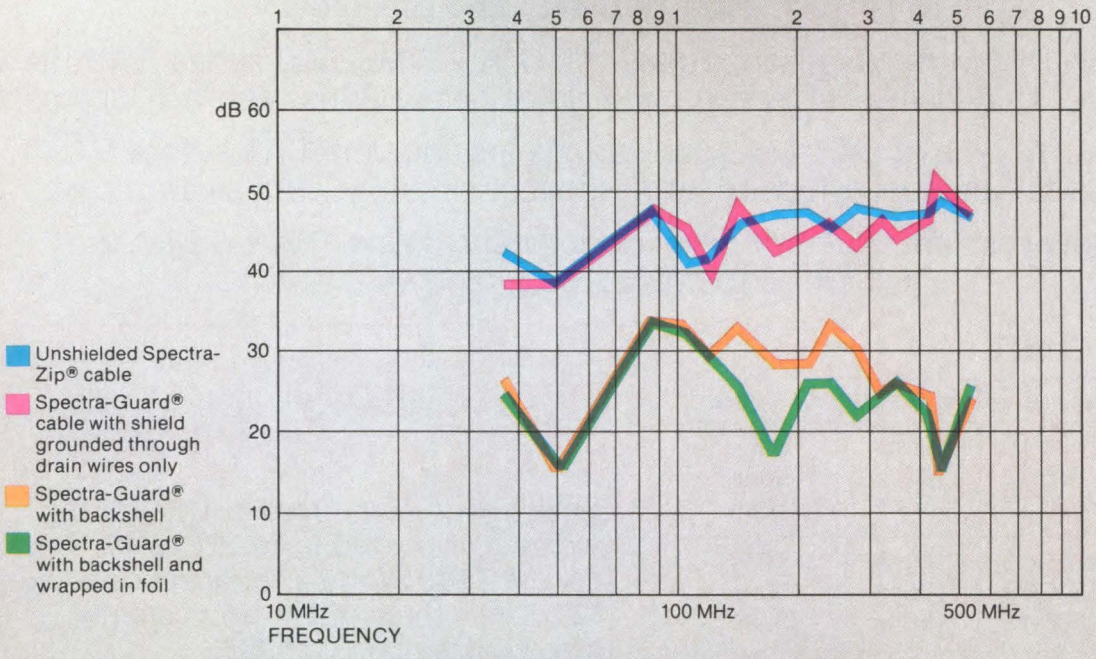

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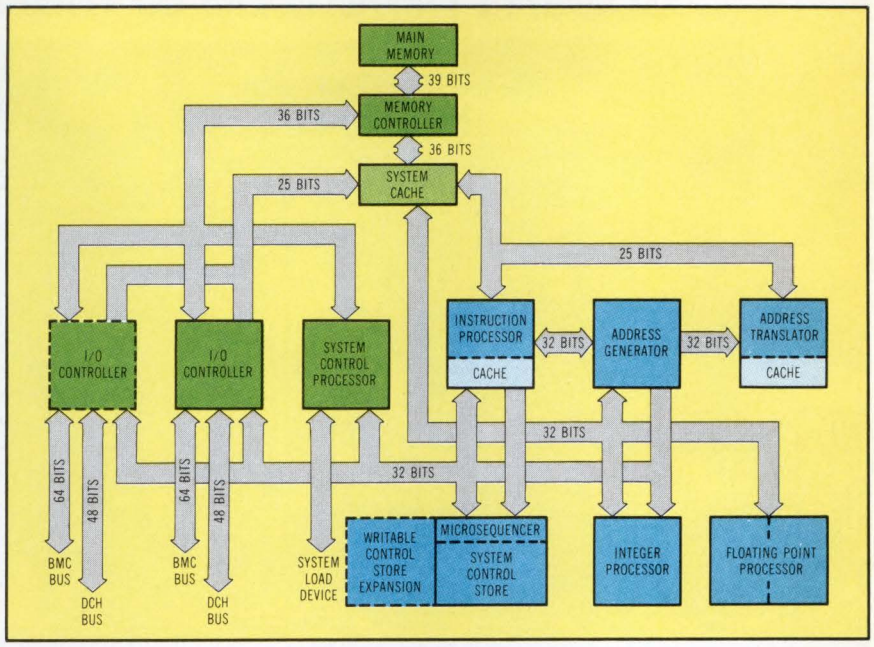
CIRCLE 26

Mainframe-class supermini

(continued from page 34)



Dedicated pipelines, caches, and buses allow Data General's Eclipse MV/10000 subsystems to operate concurrently with minimal contention. Microcode has been extended from 80 to 104 bits to take advantage of expanded system organization and provide better control of parallel operation.

board for single-precision (32-bit) and both boards for double-precision (64-bit) operations. Parallel design dedicates separate hardware ALUs for mantissa, sign, exponent, and multiply/divide functions. Accuracy is improved through 72-bit wide data paths that allocate 56 bits to the mantissa and 8 bits to the exponent, with 8 guard bits.

Four pipeline levels in the instruction processor provide for concurrent fetch, decode, and execution of macroinstructions. Each instruction sequence is carried through the pipeline in various stages of completion, with one exiting every 140 ns. The directly mapped instruction cache acts as a 4K-byte, lookahead/lookbehind buffer for the instruction stream, fetching 32 bits every 70 ns. Lookahead buffering prefetches and stores instructions from the system cache before they are executed—to improve performance in sequential instruction streams. Lookbehind buffering retains instructions after they have been decoded, reducing execution time for program loops.

A dedicated address generator creates logical addresses from the instruction stream and converts them to physical memory addresses. It operates concurrently with other processing subsystems so that operand fetches can overlap instruction execution. Moreover, the address generator contains its own 32-bit ALU and register file that is accessible to the instruction processor. This register file supports a fifth pipeline level that allows macroinstructions to reference a logical memory address within one 140-ns cycle. Under microprogram control, the address generator will perform 32-bit arithmetic to offload the integer processor.

In virtual memory applications under AOS/VS, the 70-ns address translator is a hardware accelerator for the demand paging function. Operating in conjunction with the instruction processor and address generator, the unit translates logical addresses sent from the address generator into physical addresses. A high speed 4K cache contains a lookup table that stores 14 bits of recently translated addresses for up to 1024 individual pages in physical memory. Furthermore, these 14 bits

(continued on page 45)

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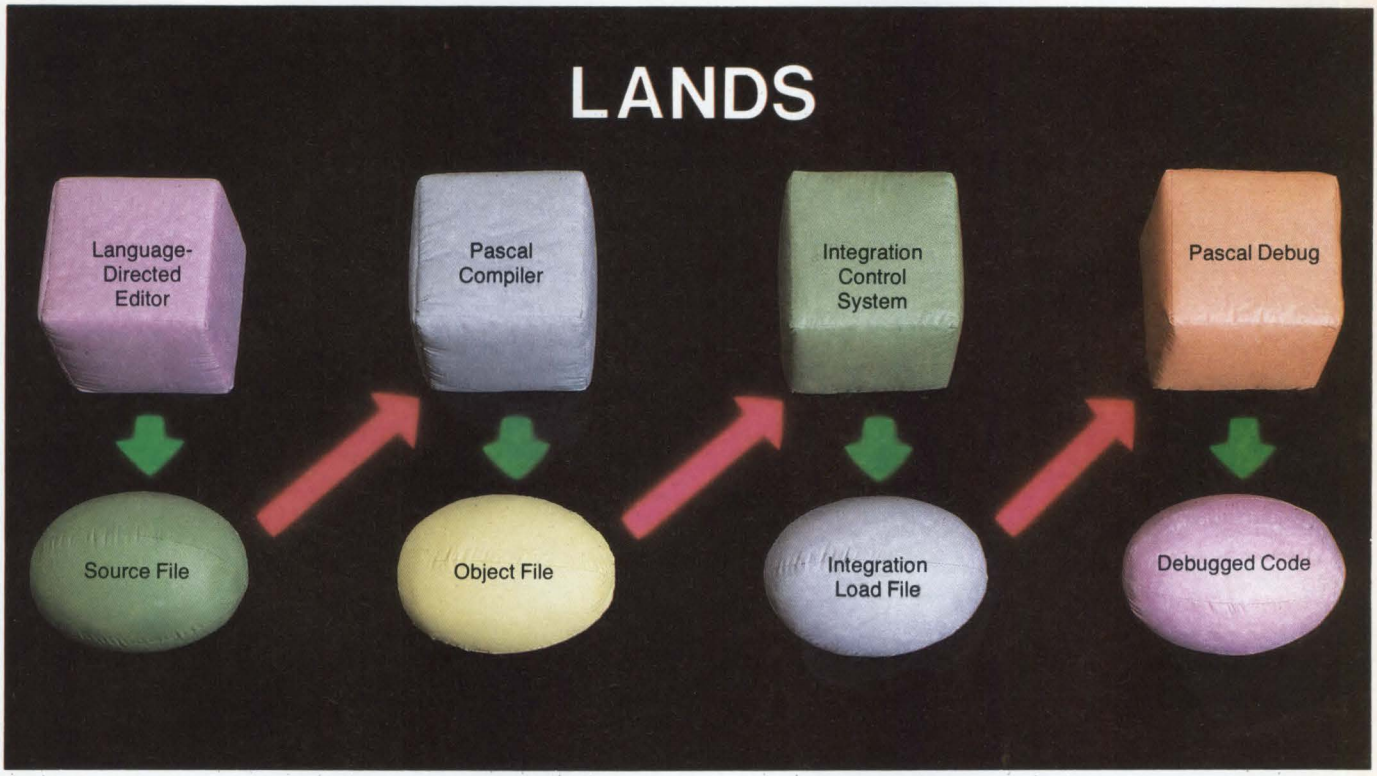

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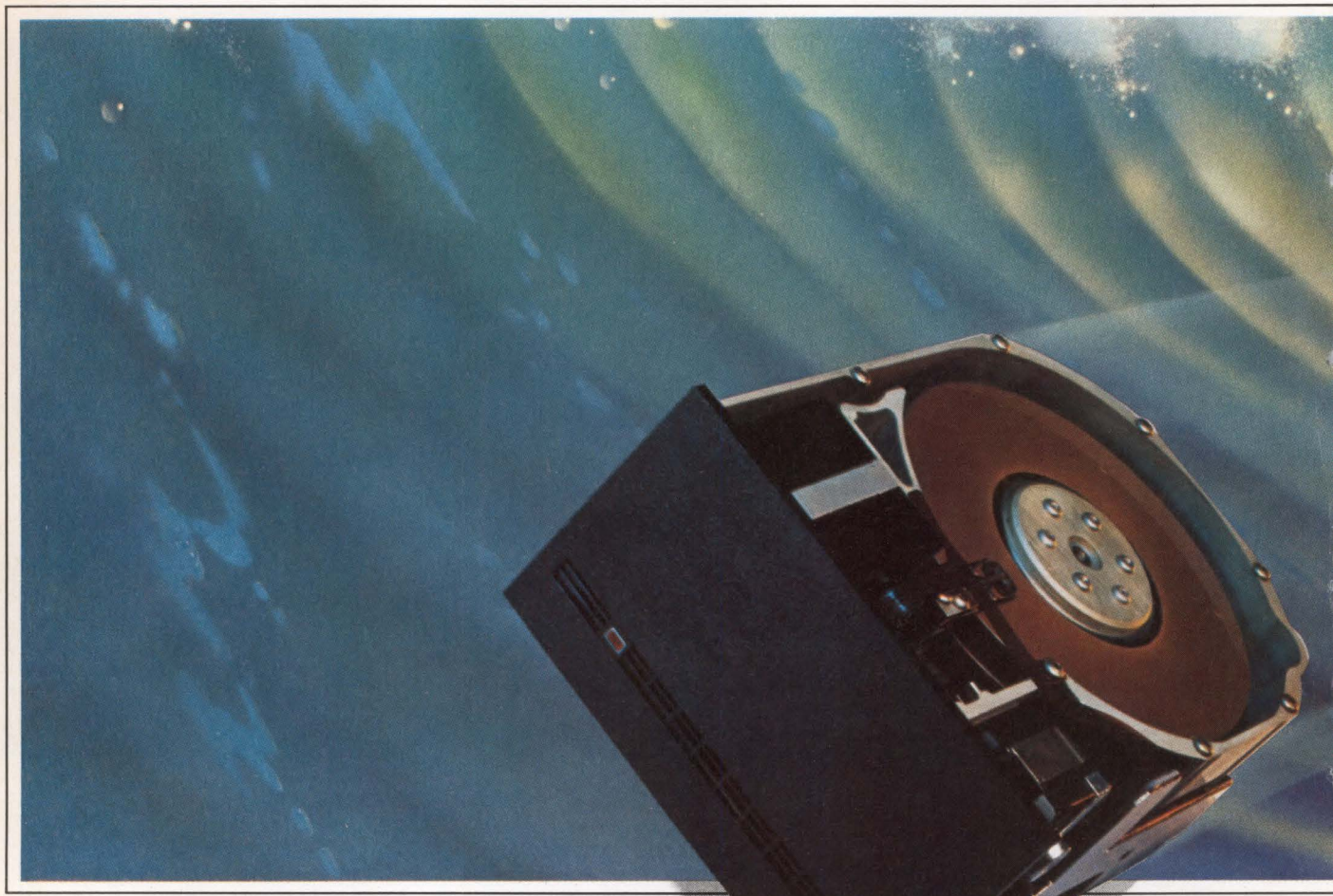

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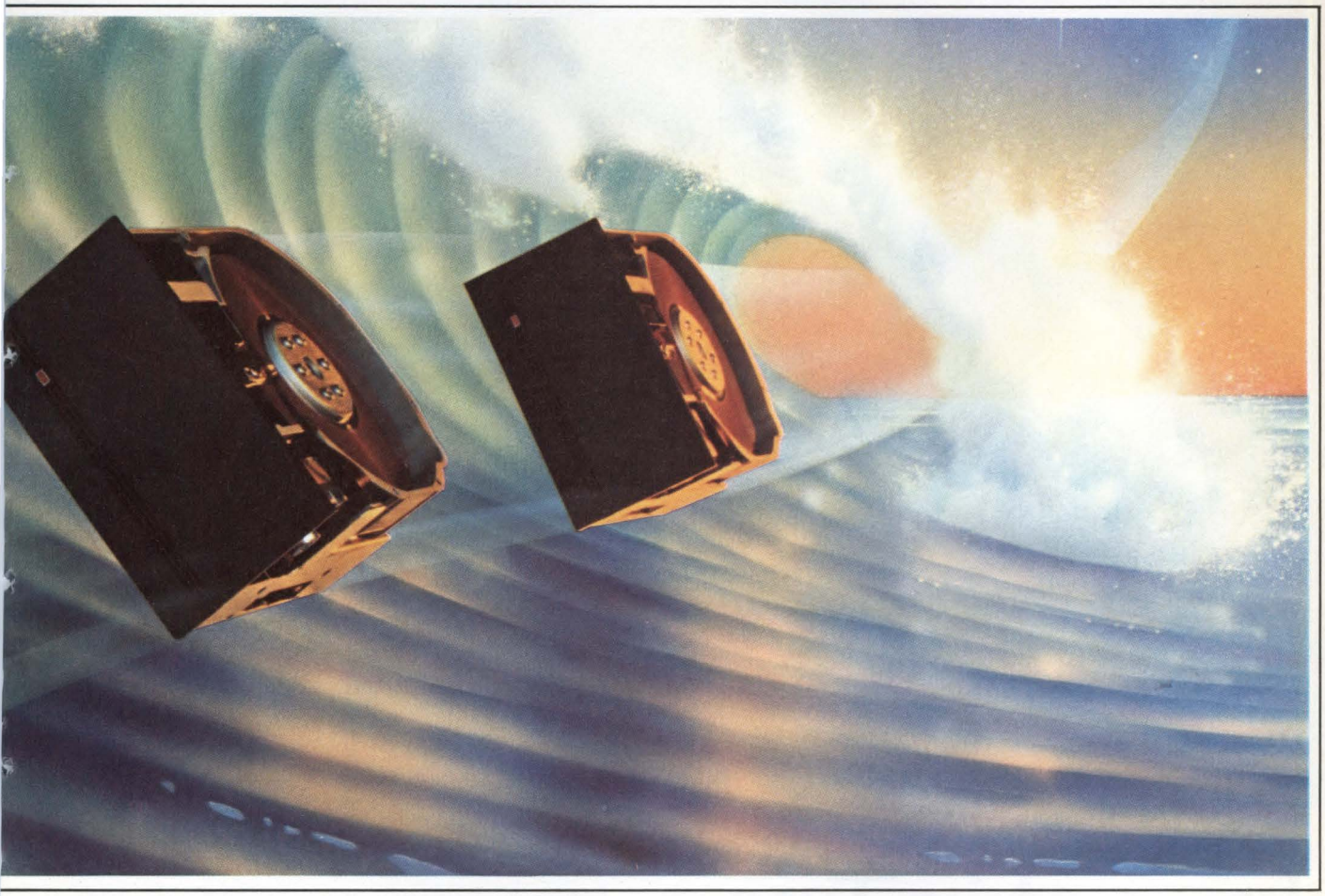

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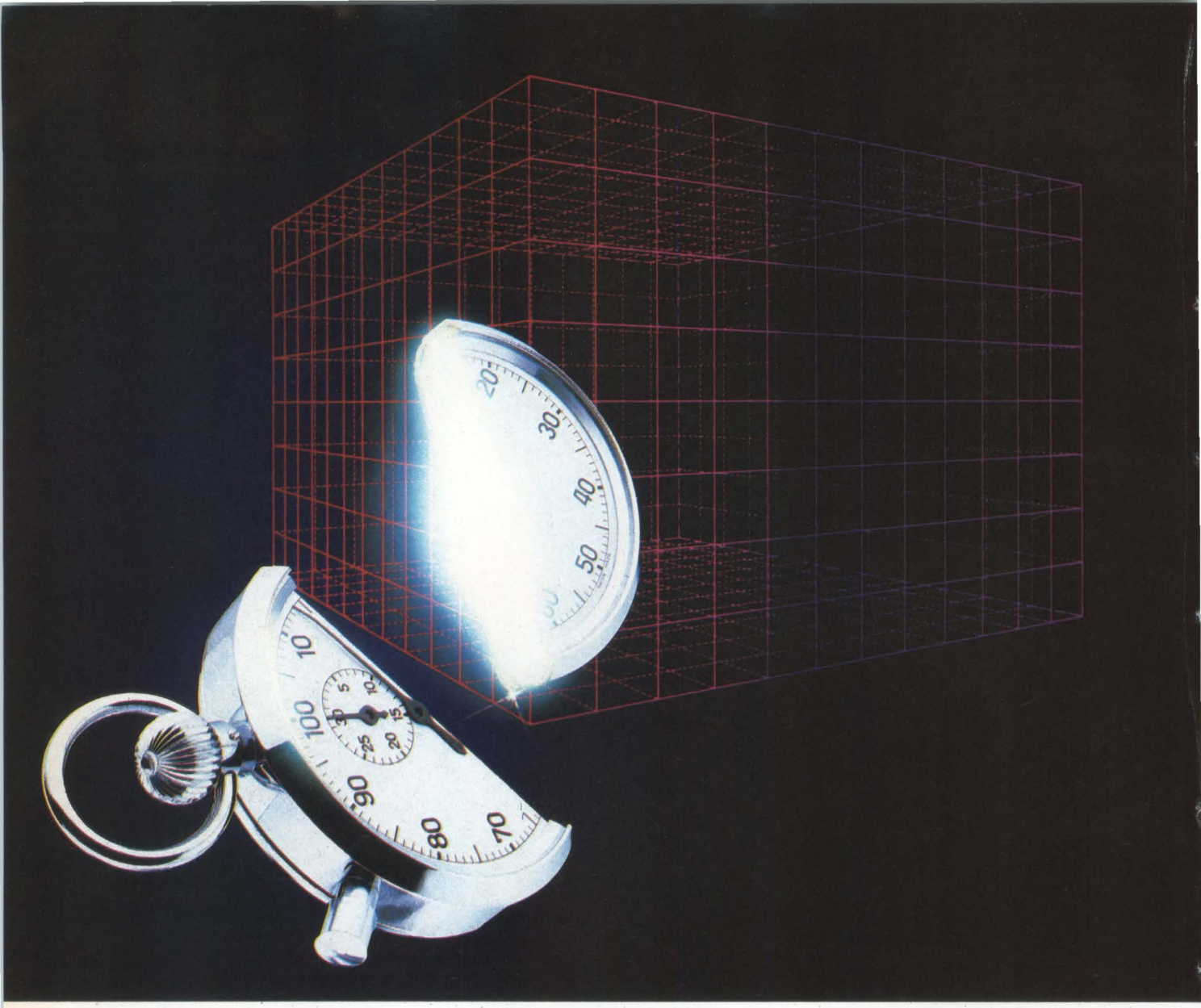
CIRCLE 29



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CIRCLE 31

Mainframe-class supermini

(continued from page 39)

are concatenated into full physical addresses. When a program requests a page, the address translator checks for the location of that page in the cache; a "hit" obviates the address regeneration step.

Moreover, address translator logic controls access to all programs, data, and files via hardware. This imposes an 8-level security structure upon the system's 4G-byte address space. Each ring corresponds to one of the eight segments maintained by the AOS/VS operating system for demand-paged virtual memory management. Rings are prioritized, and higher privileged rings assigned to critical system processes such as operating system or memory and file management software. Application programs and user data usually reside in outer, lower privileged rings. Communication between rings is allowed only after the system confirms proper accessibility, according to a hardware implemented hierarchy.

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Circle 241

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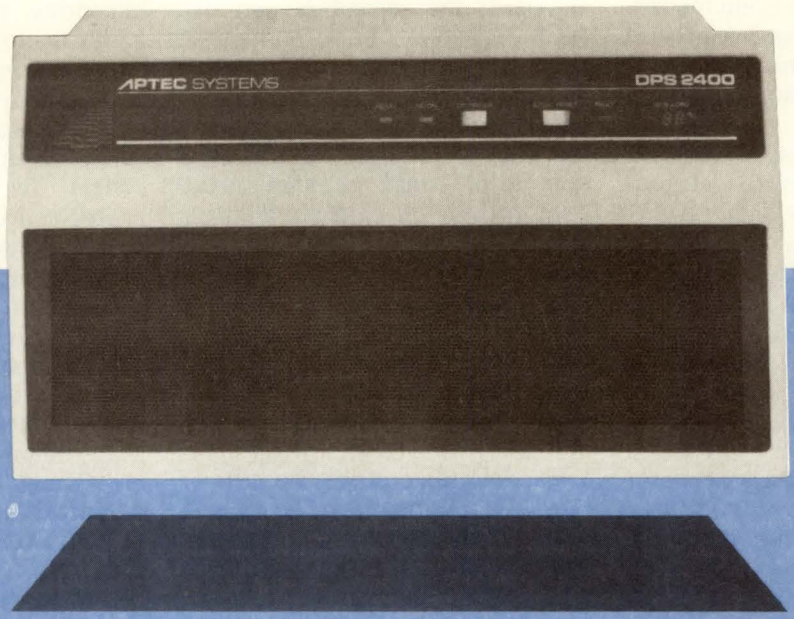

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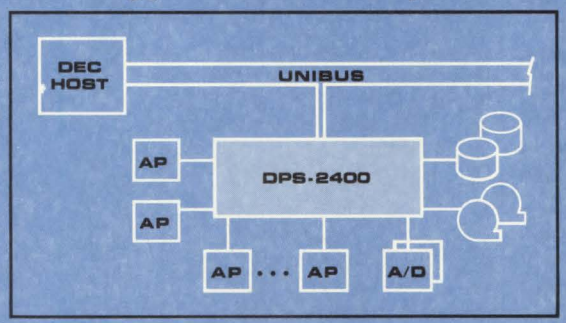

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CIRCLE 33

Advances make CMOS serious VLSI contender

Major advances in CMOS are leading this technology toward dominance in increasing application areas, especially those that demand low power consumption and portable operation. In fact, engineers are no longer speculating about whether or not CMOS will become predominant but rather about which CMOS technology will win out—or, indeed, whether an industry standard CMOS technology will emerge.

In addition to the low power consumption for which it is well known, CMOS, in aiming for greater densities, also must address reliability, high data bandwidth, and increased speed issues. Intel Corp has announced its CHMOS-D III process technology, which addresses all four issues. Although it has not announced any specific product, the company has demonstrated this technology in the form of a 70-ns 64K DRAM.

Using an HMOS-like silicon substrate, CHMOS uses a P-channel memory cell embedded in an N-well biased at V_{DD} potential. Soft errors induced by alpha particles are partially prevented because the N-well array acts as an effective minority carrier barrier.

Soft error resistance is further improved due to CHMOS' ability to create much thinner storage gate oxides than before, which increases the capacitance of any size memory cell. The greater the capacitance, the larger the charge that can be stored; hence, it becomes less likely that the charge disturbance caused by an errant alpha particle will cause an error.

Intel reports that by using CHMOS it has achieved gate oxide thicknesses of under 150 Å—down from 1200 Å—and an average gate capacitance of about 145 femtofarads using a 250-Å gate oxide thickness. Gate capacitance in Intel's 2164A HMOS 64K DRAM is 85 femtofarads.

Significant improvements in power consumption have also been reported. Intel claims that operating current is about one-half that of the HMOS 64K DRAM, or 28 mA at a 135-ns cycle time. Standby current at 5 μA amounts to about one-fifth that of the HMOS product.

Power consumption improvements have also resulted in faster speeds, with 70-ns access time and 130-ns cycle time, representing a 40-ns improvement over the HMOS product. In addition to the improved cycle speeds, CHMOS D-III allows faster methods of accessing stored data to be used. Two methods of data access, called ripplemode and static column mode, allow a 25M-bps data bandwidth. This bandwidth strongly qualifies the high density CMOS RAM for applications that demand both high density and high bandwidth.

Implementation in CMOS has also allowed simpler peripheral circuitry design because of reduced switching noise. CMOS requires only 14 clock generators as opposed to 40 for a comparable NMOS chip; overall, it requires about 500 fewer peripheral transistors. This not only reduces cost, but simplifies the task of adding static circuits on the chip. Indeed, adding these static circuits makes possible the high bandwidth ripplemode previously mentioned.

Ripplemode is essentially a form of high speed page mode that allows random access to all bits in a row. The user supplies one row address strobe and a new column address. The presence of flowthrough latches implemented as static logic on the address inputs allows a lookahead function before the column address strobe goes low. This allows an access time of 40 to 45 ns.

The potential applications for high speed, high density CMOS are spurring efforts by other manufacturers, notably Japanese ones. Mitsubishi has reported power consumption improvements in an N-well CMOS 64K RAM using a divided

(continued on page 48)

CMOS advances

(continued from page 47)

word line technique to improve both the word delay and the column current. In the 64K RAM, the cell array as well as the word line is divided into eight 1K blocks. The word lines are arranged so that current flows only in a selected block, thus reducing overall power consumption. Mitsubishi reports a one-eighth reduction in column current. Address access time of 50 ns has also been reported.

With the prospect that CMOS may well become a dominant VLSI technology, some observers predict that there will be a variety of CMOS technologies responding to differing speed, power, noise, and radiation requirements, as well as process compatibility and analog capability requirements. N-well CMOS, however, appears to be gaining popularity, especially in the memory area, because of its speed and its ability to avoid latchup problems when used at scales below 2 microns. An even greater prospect is to go beyond single-crystal substrates to epitaxial wafers. The latter are particularly attractive because of their relative immunity to latchup at short channel lengths, while silicon-on-insulator (SOI) options become less attractive due to high cost.

With higher densities becoming possible, the problems of interconnection and wiring must be addressed. These issues bring multiple layer metal and silicide techniques to the fore and renew the interest in SOI structures. CMOS is clearly emerging as a viable VLSI technology for the future. However, the process technology options and trade-offs now available within CMOS make it a rich field for innovation and variety even before agreement is reached on a set of industry standards. **Intel Corp**, 2625 Walsh Ave, Santa Clara, CA 95051.

Circle 242

MEMORY SYSTEMS

QIC no guarantee for compatibility

Proposed standards for quarter-inch tape cartridge drives are intended to help establish that medium as the likely choice to back up rigid disk drives. Yet, many members of the Working Group for Quarter-Inch Cartridge (QIC) Drive Compatibility admit that the adoption of the QIC-02 interface and QIC-24 format specifications will not guarantee total compatibility between streaming drives and controllers.

ANSI and the European Computer Manufacturers Association (ECMA) currently have both proposals under consideration. There are, however, specific concerns that will, no doubt, be the focus of future ANSI and ECMA discussions.

For example, a total of three command sets are defined in the QIC-02 interface proposal. Yet only one set will be required for all controllers and drives. Also, magnetic specifications in the QIC-24 format proposal leave considerable latitude for different drive implementations. Idiosyncrasies among these drives (eg, unique erasing schemes) can inhibit the ability to exchange cartridges.

Unquestionably, more work is needed before these standards are adopted. Meanwhile, system designers should keep one phrase in mind: "let the buyer beware."

According to QIC group coordinator Ray Freeman, of Freeman Associates (Santa Barbara, Calif), multiple command sets in the QIC-02 proposal (standard, optional, and vendor-unique) balance the need for an industry accepted device protocol with the desire to maintain design flexibility. In this sense, the proposed interface provides for upward compatibility. To comply with the proposed interface, drives and controllers need only execute the standard commands.

Basic functions needed for streaming image backup of rigid disk drives are implemented in the standard commands. These functions consist of read and write data blocks and file marks, initialize and erase the cartridge, and transfer status byte information. Streaming commands from Archive Corp (Costa Mesa, Calif) and Cipher Data Products (San Diego, Calif) interfaces serve as a basis for these standard QIC-02 commands.

On the other hand, optional commands are intended to increase the functionality of the tape drives and offer a measure of product differentiation among vendors. Such commands can either enhance streaming operations (eg, READ N FILE MARKS) or emulate start/stop drives (READ REVERSE). Optional commands can only be executed if a drive supports them. Otherwise, the drive traps them and sets an error flag.

Vendor-unique commands are simply reserved opcodes in the specifications. Each drive manufacturer is free to use them for proprietary commands, but these commands will be trapped as well if not supported on any given drive.

Through upward compatibility, each vendor can implement all optional commands (a total of 23), a subset, or none at all. Specific implementation of each optional command is also left to each vendor. The QIC-02 proposal only defines the name of the command, the command's opcode, and the desired results. For example, the READ EXTENDED STATUS 1 command specifies the contents of the extended status register for only a portion of the 6 bytes used. Tandberg Data, Inc (Orange, Calif) chooses to use some of these undefined bytes for saving extra information such as the most significant bits of the last file mark. These bits are ignored if the command is issued to another vendor's drive.

As a step toward minimizing the confusion over which optional

(continued on page 54)

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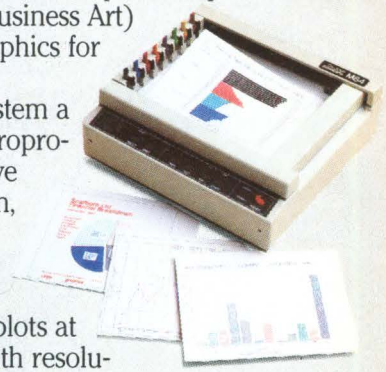

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CIRCLE 35

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CIRCLE 36

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QIC compatibility

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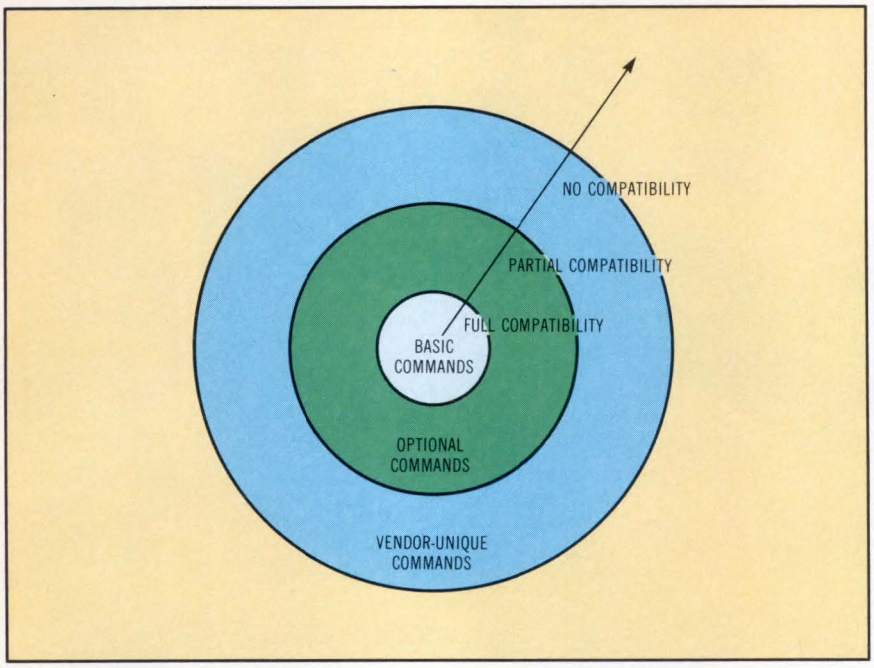

Viewed as a layered shell, compatibility among QIC-02 drives becomes easier to discern. Basic commands offer full compatibility, with vendor-unique commands offering no compatibility.

commands will be supported, several vendors have chosen the same commands to augment the standard set. Archive, Cipher Data Products, and Tandberg Data, as well as Wangtek (Culver City, Calif), claim they will support those commands that enhance streaming operations. The WRITE WITHOUT UNDERRUNS command allows the tape drive to continue streaming even if data from the host are momentarily interrupted. Redundant data are written until new information is sent. The READ N FILE MARKS and WRITE N FILE MARKS help reduce the number of commands the host issues. SEEK EOD (end of data) provides a means to get past the last record and continue streaming. As multiple vendors augment the standard commands with these optional commands, a *de facto* standard emerges.

Otherwise, vendors are following no real pattern in implementing optional commands. Both Archive and Cipher Data Products will support a self-test instruction, but will use proprietary diagnostics. Tandberg Data will support all optional commands, while Data Electronics will not implement any. Designers should, therefore, carefully match application requirements with the capabilities of the standard and optional command sets. Multiple sources may be required for drives that implement desired optional commands.

Tape controllers face a similar dilemma. All QIC-02 controllers must support the standard command set, but have the flexibility to support a portion or all of the optional set. Key to this is the involvement of the controller in translating host system commands into drive commands.

For firmware based controllers, such as the Gypsy from ADES (Pomona, Calif), implementing all or part of the optional set requires considerable modification of the microcode responsible for interpreting system calls. Also, the variety of ways that optional commands are implemented on different drives places an enormous burden on the controller to keep track of possible differences. The company has bypassed these concerns by only supporting the standard commands.

Yet, if the interpretation of system calls is handled in software, modifications can easily be made as host computers and tape drives change. This is the approach taken by Systech (San Diego, Calif) to support Multibus systems running under UNIX. Host software drivers for the company's STC-4400 contain the necessary code (written in C) to implement all optional commands. Constants are set to select specific commands implemented on any given drive. The company currently supports Archive, Cipher Data Products, and Tandberg Data drives.

Media compatibility raises fewer issues than those posed for the physical interface. The QIC-24 format specifications define both the physical layout of tracks and blocks and the magnetic characteristics associated with reading and writing to tape. A second level of compatibility for data exchange overcomes a liability of floppy disk drives. While media and interface standards exist, floppy disk drives suffer from a lack of uniform standards.

Compatibility becomes an issue when vendors implement the magnetic specifications on their drives in unique ways. These magnetic techniques address the method of tape erasure, and background noise. They also permit reading at reduced track density (QIC-24 specifies both four and nine tracks).

For example, Mike Newton, engineering manager with Data Electronics (San Diego, Calif), says that reading a 4-track cartridge with a 9-track head can cause problems because of the different signal amplitudes needed. Background noise can also hamper reading tapes made on different drives due to varying erasure techniques. According to Newton, half-inch tape drives encounter problems even with the IBM 9-track format. Competing drives may be compatible with IBM drives, but not with each other.

Without the frames of reference available with half-inch tape drives, Wangtek Engineering Manager Jerry Fuchs says that it will be interesting to see which vendor will make changes when one drive cannot read a cartridge made on another. Newton believes that a spirit of informal cooperation among vendors will iron out differences.

(continued on page 56)

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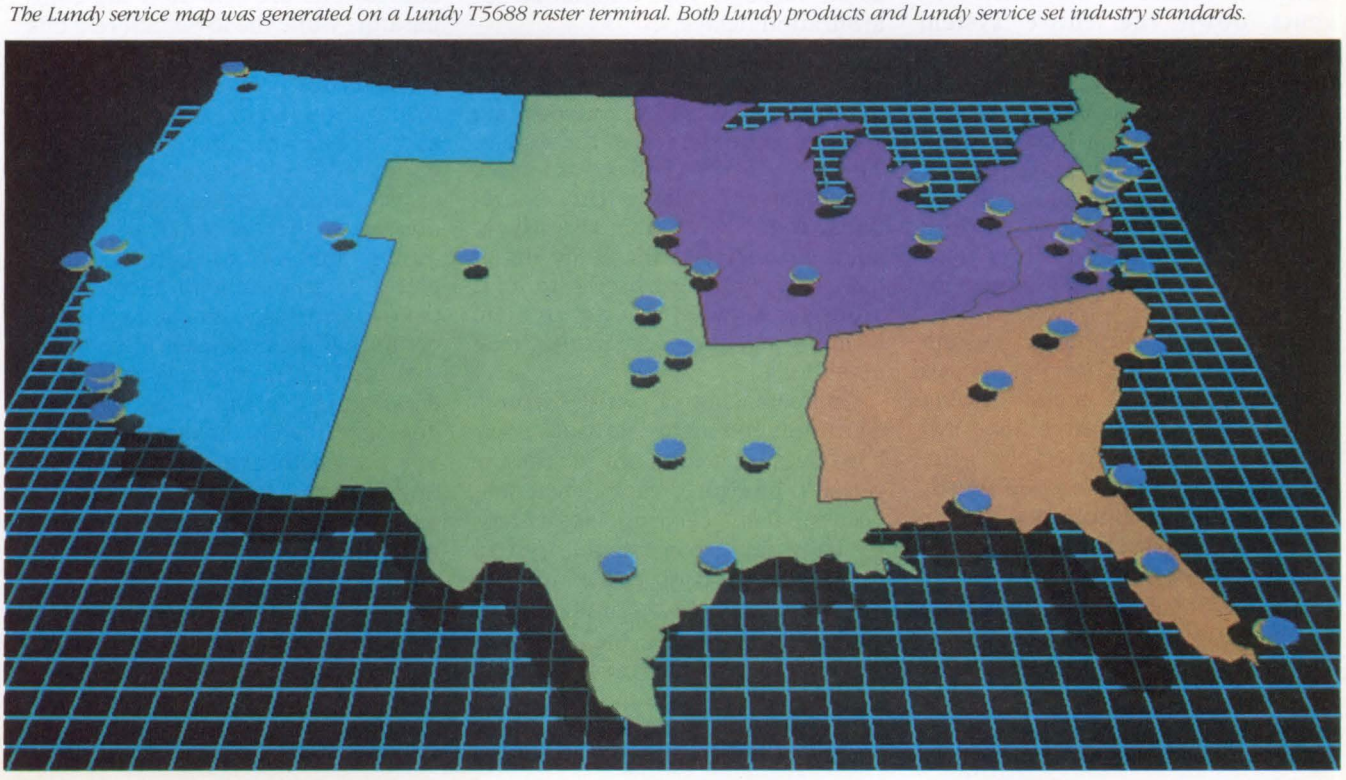

CIRCLE 38

QIC compatibility

(continued from page 54)

It should be emphasized that the QIC-02 and QIC-24 proposals complement each other, but do not require each other for implementation. The QIC-02 interface can support existing formats from Archive, Cipher Data Products, Data Electronics, and Tandberg Data. The QIC-24 format can be used with separate interfaces from Control Data (Minneapolis, Minn), Kennedy Co, (Monrovia, Calif), and 3M (St. Paul, Minn) as well. However, neither standard has allowed room for such developments as 3M's drive that uses a 600' (183-m) cartridge with 16 tracks. New standards will be needed as such developments gain industry acceptance.

—Joseph Aseo, Field Editor

Onboard cache memory speeds up transfers

Tying main memory with its own high speed cache, the High Density Memory with Cache (HDMC) memory board from Systems Group accelerates data transfers in Multibus systems. The 2K x 16-bit static RAM array (35-ns access time) handles about 85% of the read operations, with the slower 256K x 22-bit dynamic RAM array (200 ns) used to store seldom accessed data. Data are transferred on a byte or word (16-bit) basis.

Using a modular cache configuration also overcomes problems associated with fixed-size caches in conventional systems. In these systems, performance typically degrades as large amounts of main memory are added. Perhaps more critical, a hardware failure in the cache RAM shuts down the entire system because such memory is typically located with the CPU.

In contrast, the HDMC expands the size of the cache RAM as main memory is added. This ensures that system cache performance is maintained. Fatal system errors do not occur since hardware failures on a memory board have no direct impact on the CPU.

Designed to minimize system overhead, the memory board uses address and data latches during write operations to free the processor. The remainder of the write operation is handled onboard, enabling the processor to supervise other system tasks. Furthermore, no wait states are imposed on the processor for precharging the dynamic RAMs between write operations. This task is also handled onboard as part of the write cycle.

Data transfers are further reduced for Multibus systems if designers take advantage of the board's dual-ported architecture. An onboard bus (plus bus) can be used to support separate processors on each board. Use of the Multibus could then be limited to interprocessor communications. Bus arbitration logic is included to handle competing requests from either bus on a first-come, first-served basis. Requests occurring while the internal bus is active must wait. As a result, redundant multiprocessor architectures can be realized without resorting to custom hardware.

If applications only require a single bus, the bus arbitration logic can be defeated and data transfers accelerated even further. Read access times are reduced from 70 to 20 ns through the elimination of arbitration delays.

The modular cache does not require software drivers to maintain it. In fact, cache operations are transparent to the rest of the system. The CPU merely issues read/write commands. During write operations, data are written directly to main memory and the cache simultaneously. Onboard hardware logic arbitrates between accesses to main memory and the cache during read operations.

Implementing a write-through algorithm eliminates software overhead because it does not require the cache to be cleared each time a miss occurs. The clearing algorithms typically cause considerable system overhead in RAM-intensive applications implemented on multiple port systems, according to the company. Assuming that the most recently written data are the most accessed simplifies cache updates so that they merely write over old data as misses occur. Seldom accessed data still reside in main memory. The cache is kept current because the first read request after a write operation always guarantees a miss.

Complementing the write-through algorithm is a cache tag scheme similar to the scheme found on systems from Texas Instruments (Dallas, Tex) and Charles River Data Systems (Natick, Mass). Main memory is now organized into 128 pages, each the same size as the cache memory. The upper address bits (A12 to A20) uniquely identify each page. The lower address bits (A0 to A10) describe locations within each 2K x 16-bit boundary. When a 22-bit address is passed during a read operation, the upper address bits are sent to a tag comparator, while the lower address bits are used to determine the location in cache memory. While data are being read out on the data bus, the upper address bits are compared with the upper address bits stored in the cache address tag RAM. The addresses in the tag RAM are stored during the write operation that places data in the main memory. If the two addresses match, a cache hit occurs and the cycle ends after 70 ns.

A cache miss occurs when the address stored in the cache tag RAM does not match the upper address bits passed during the read operation. Control logic then initiates a data transfer from main memory. Both the cache RAM and its tag RAM are updated simultaneously by writing over those locations where the miss occurs. The total time required to handle a cache miss is 430 ns. Besides handling cache and dynamic RAM, the control logic

(continued on page 58)

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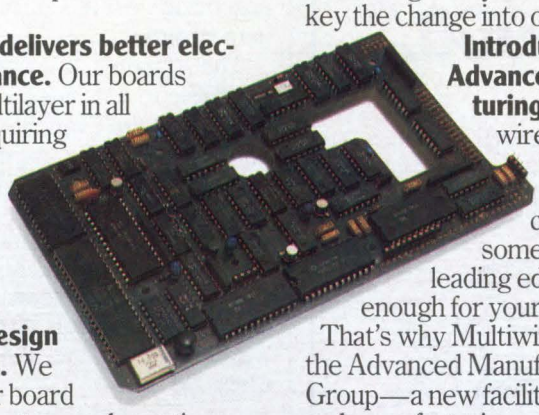

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Onboard cache memory

(continued from page 56)

generates support timing for the dynamic RAMs and also generates the acknowledge to the requesting bus.

The memory board ensures high data reliability by featuring a hardware error detection and correction unit. This unit generates 6 syndrome bits for each 16-bit data word written into main memory (dynamic RAMs are 22 bits wide). During read operations, the error correction code (ECC) logic corrects single-bit errors and flags double-bit errors as the syndrome bits are decoded. Initialization logic fills the dynamic RAMs with valid ECC information before the first read access on power-up, and inhibits access until the operation is finished. Initialization allows the board to be used without modifying system software and gives the system the benefit of power monitoring.

Since the cache handles most read operations, dynamic RAM refresh can occur simultaneously with them. The refresh operations are postponed if a read access to dynamic RAM is needed. However, processor wait states are imposed if a read access occurs while a refresh operation is in progress.

The dynamic RAM arrays are expandable to 2M bytes when 256K-bit RAM chips are available. Addressing and control logic were designed with this expansion in mind by providing a 22-bit address space. Information on the HDMC's price and availability is obtainable upon request. **Systems Group, a div of Measurement Systems and Controls,** 1601 Orangewood Ave, Orange, CA 92668.
Circle 243

July Preview—
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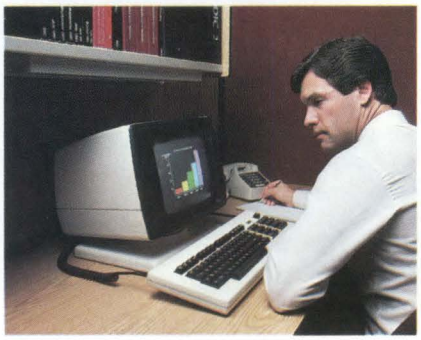

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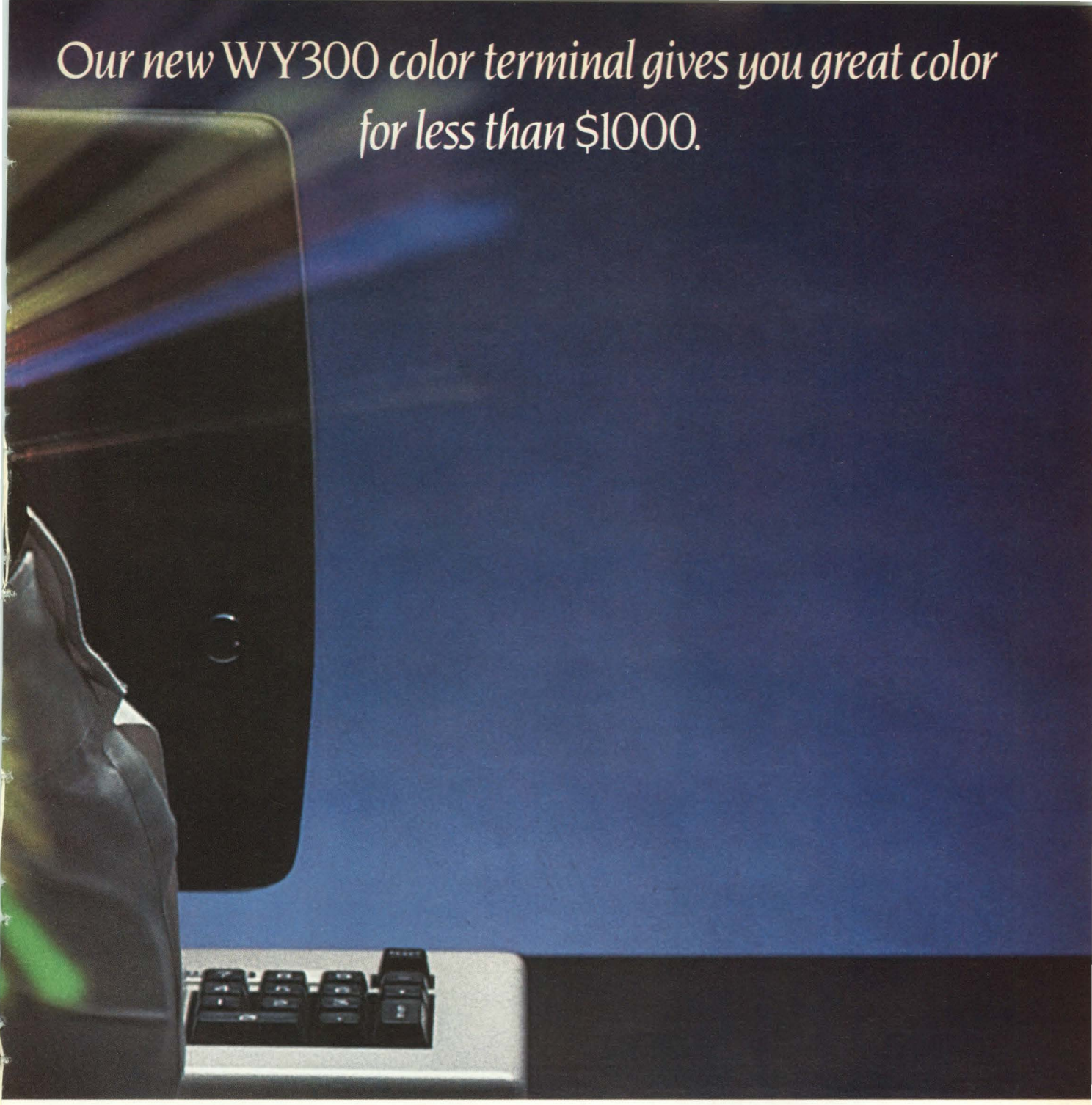

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CIRCLE 43

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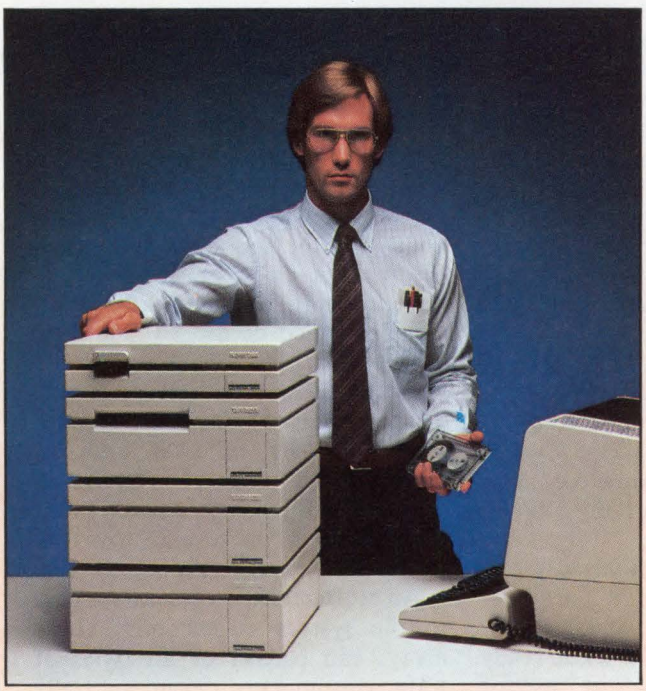

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DATA SYSTEMS DESIGN

CIRCLE 44

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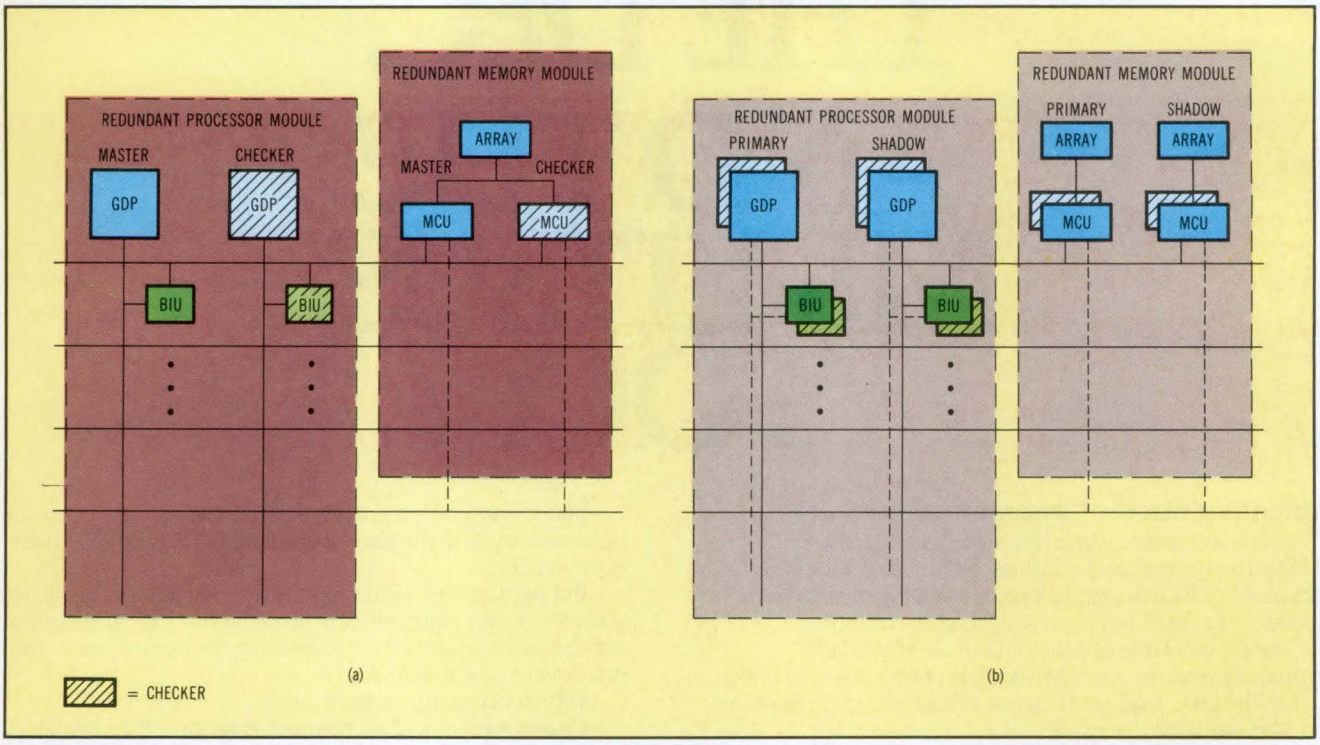
Components make systems fault tolerant



Fault tolerance requires duplication of processors, interconnections, and memory arrays. Intel's FRC configuration (a), which preserves computation results while halting processing, uses two complete sets of system elements. QMR (b), which provides automatic transparent error detection and correction, requires four complete sets.

Two added components in Intel's Micromainframe family—the iAPX 43204 bus interface unit (BIU) and the iAPX 43205 memory control unit (MCU)—provide the switching and interface circuitry needed to build fault-tolerant multiprocessor systems. The units combine to replace entire boards of discrete components that are normally needed to detect failures and must switch to a redundant processor, bus, or memory. All fault detection and recovery functions are transparent to the application software.

System configurations can range from partial fault tolerance with functional redundancy checking (FRC) to complete fault tolerance with quad modular redundancy (QMR).

An FRC system consists of a master general data processor (GDP), which handles normal processing; a redundant "checker" GDP, which runs parallel to the master and can take over processing at any time; two or more BIUs, which connect to GDP's local bus to parallel, redundant system master buses; and two MCUs per memory array, which check each other, correct errors, and connect to the system master bus. Each GDP consists of a 43201 instruction decode unit, a 43202 microexecution unit, and a 43203 interface processor that maintains communication with I/O subsystems.

A second set of hardware components ensures that no single hardware failure will corrupt the results of a single computation. System software still must disable the faulty component and restart the system, however.

A QMR system is essentially two FRC systems running in parallel—each GDP, BIU, MCU, and memory array has a "shadow" backup ready to take over instantly in case of trouble. Fault detection and a disabled, failed GDP or memory array are transparent to both application and system software, although the system software is notified after the recovery is complete that a failure has occurred.

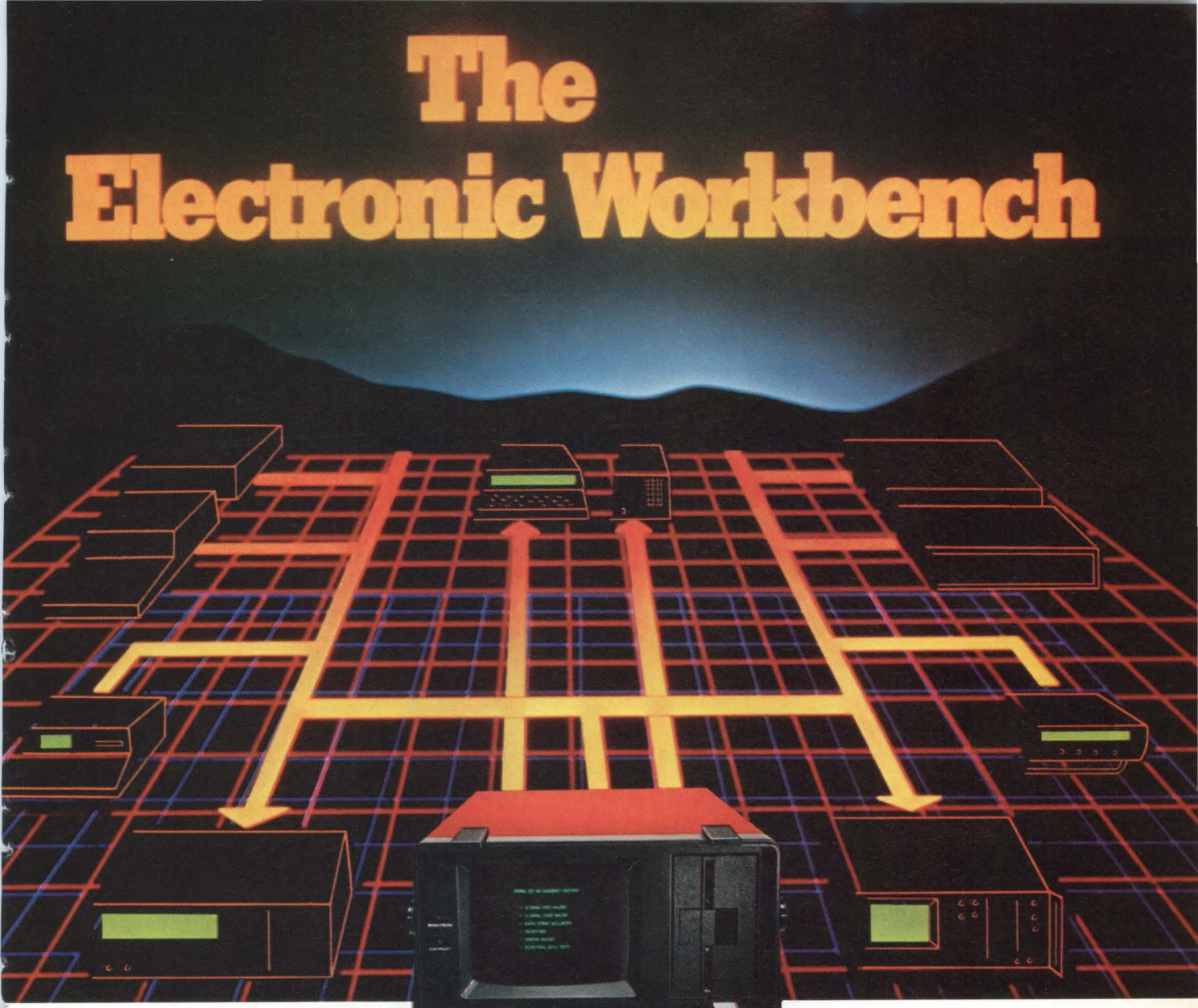
The FRC configuration requires twice the number of GDPs and control circuits as a minimum functional iAPX 432 system does, while the QMR configuration requires four times the number of GDPs. Both redundant systems depend on the functions provided by the BIU and MCU devices.

A BIU is a switch that accepts access requests from the GDP and, based on the physical address, decides which memory or buses will be used. BIUs also arbitrate bus contention among the several GDPs that can be part of a system.

An MCU interfaces memory arrays to the system master bus. These arrays can consist of all types of RAM components, even partially failed ones. The MCU treats memory as 32 data bits, 7 bits of error correcting code, and 1 spare bit. It

(continued on page 66)

The Electronic Workbench



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CIRCLE 45

Fault-tolerant systems

(continued from page 64)

automatically refreshes dynamic RAM arrays and scrubs single-bit errors as a background task. Further, only a modest amount of external logic is required to interface the MCU to the storage array RAMs.

The iAPX 432 is designed for large scale realtime control and transaction processing systems. Both the BIU and the MCU will be generally available the second half of this year. In quantities of 100, the BIU is priced at $262.50 and the MCU at $497.50. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 244

DATA COMMUNICATIONS

Data and voice share wire

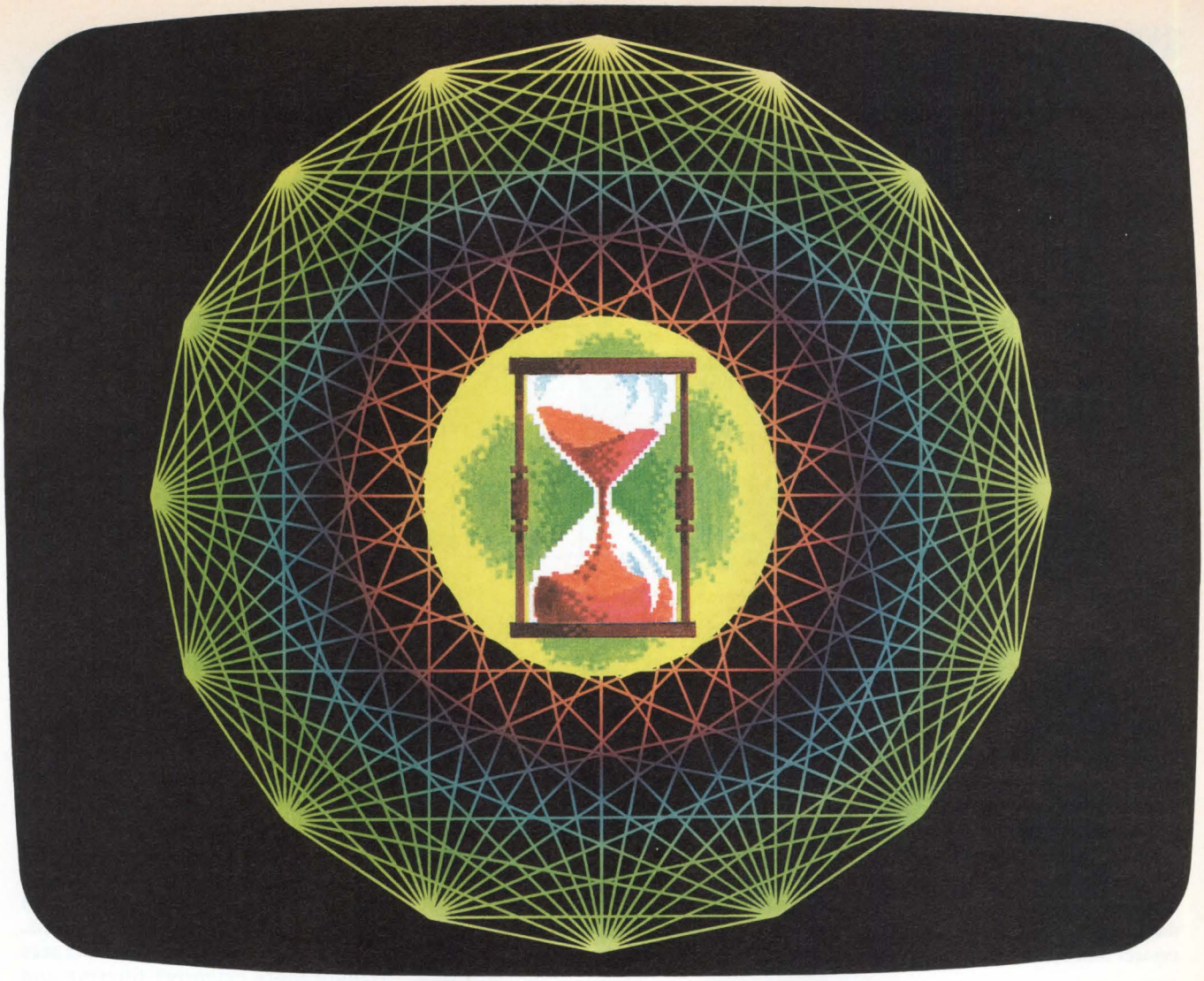
Reducing the need to rewire buildings, data-over-voice multiplexing schemes piggyback data atop voice on existing twisted-pair telephone wire. These techniques offer an alternative to local area networks that depend on costly coaxial cable as well as digital voice/data private branch exchanges (PBXs).

Data-over-voice techniques are well suited for large facilities such as college campuses and high-rise office buildings needing to upgrade their data handling capabilities. Typically, these sites already have an extensive investment in PBXs and voice-grade telephone lines. Such facilities would have difficulty installing coaxial cable to handle local area networks, such as Ethernet, because of cost and duct capacity. Likewise, voice/data PBXs that digitize voice may not be economically feasible if present voice-only PBXs can be modified to handle data via data-over-voice multiplexing.

Several products are now available to meet these needs. Micom Systems, Inc (Chatsworth, Calif) and Teltone Corp (Kirkland, Wash) address the need for intrabuilding communications with carrier systems capable of handling data rates up to 19.2k bps at a range approaching one mile. Interbuilding communications for a total distance approaching three miles is handled with the Line Miser system from Gandalf Data, Inc (Wheeling, Ill). Distances exceeding three miles are handled with the narrowband model 6860 Speech Plus system from RFL Industries, Inc (Boonton, NJ).

All of these systems use frequency division multiplexing to create data channels on top of (or within) the voice band that extends from 0 Hz to 4 kHz. Like Micom's Instalink460, these systems all exploit the minimal signal losses and fairly wide bandwidth of twisted-pair wire. According to Micom, signal losses increase linearly with frequency to nearly

(continued on page 68)



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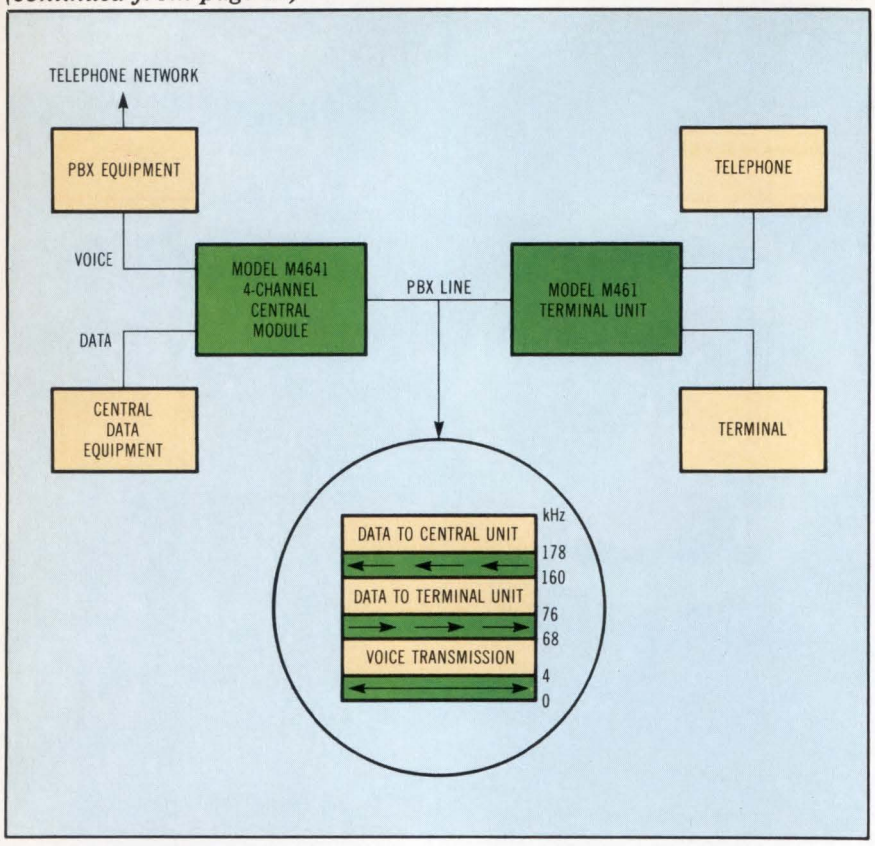
CIRCLE 47

Data-over-voice

(continued from page 66)



The Instalink461 terminal unit uses short haul modem techniques to create two data channels above the voice frequency for full-duplex transmission. An M4641 central unit splits off the data signals so that voice signals can be routed to the PBX.

1 MHz. This provides a comfortable margin for the 200-kHz bandwidth used with the Instalink460. Extraneous noise, such as channel crosstalk, is minimized because twisted-pair wire acts as a balanced carrier. The only noise encountered comes primarily from other data channels operating at the same frequencies.

The Micom system transmits data from a terminal to the computer between 160 and 178 kHz and receives data from the computer between 68 and 76 kHz. With phase-coherent frequency shift keying schemes, asynchronous full-duplex transmissions up to 19.2k bps are achieved. Teltone's DCS-2 carrier system (*Computer Design*, May 1982, p 68) implements its data channels at much lower frequencies. Remote station units transmit data between 36 and 40 kHz, and receive data between 72 and 80 kHz. As a result, full-duplex asynchronous transmissions are reduced to 9600 bps. The Teltone and Micom systems both claim an operating range of 5000 cable-feet from terminal to PBX wire center or computer center.

Using 24-gauge wire typically found between central offices and customer sites, Gandalf Data extends the range of its carrier scheme to almost 18,000 cable-feet. Asynchronous or synchronous full-duplex transmissions occur at 9600 bps. The Line Miser transmits data from the remote terminal between 48 and 36 kHz, with data received between 84 and 96 kHz. According to a Teltone engineer, Malcolm Klug, these longer distances are possible due to lower attenuation with the thicker 24-gauge wire. Both the Teltone and Micom systems are geared to handle the thinner 26-gauge wire usually found in PBX-to-telephone systems.

However, all of these systems terminate at the voice PBX in the same manner. A central unit removes the data from the line prior to arrival at the PBX or outside telephone system. In fact, telephone lines usually terminate at a large distribution frame rather than at the switchboard itself. At this point, voice and data signals separate through frequency splitting and voice lines reconnect to the PBX side of the distribution frame. Data lines are routed either directly to computer ports, to a data PBX to gain access to multiple host computers, or to a high speed multiplexer for transport to a remote site.

Due to the separation of voice and data transmissions, normal telephone and PBX operations (eg, ringing and dialing) do not hinder the data carrier system. Although ringing and hook transients cross into the data frequencies, extensive filtering reduces signal levels well below these systems' signal-to-noise thresholds (eg, −55 dB for the Line Miser). Klug notes that most noise problems occur when strong signals going from the terminal to the host encroach on weaker signals going from the host to the terminal.

Thus, the operating frequencies selected to implement the data channels must temper the transmission speeds and distances traveled. Higher speeds and longer distances require more extensive filtering and signal extraction schemes, according to Klug. Distances exceeding 18,000 cable-feet are impossible to implement with wideband techniques. Such is the case because, in order to improve voice quality, telephone companies place inductance coils on the lines.

Narrowband techniques operating within the voice range overcome this barrier. The RFL Speech Plus carrier system shifts the voice band upward from 1.2 to 2.35 kHz to between 2.15 to 3.4 kHz. The voice band from 300 to 830 Hz remains unchanged. Voice compression creates a single 600-Hz data channel (830 to 2150 Hz) that allows 1200-bps half-duplex asynchronous transmissions. Previous implementations only allowed 600-bps transmissions.

Apart from narrowband multiplexing, the Speech Plus system operates like the others. Data signals split off from the voice line for routing to a computer, data

(continued on page 70)

IBM Compatible 3200 bpi Tape...the new standard for high capacity disk backup.

CacheTape™ Improves System Performance—with 92 MB of Winchester Backup.

3200 bpi—A New Tape Standard

With the announcement by many computer manufacturers of the availability of 1600/3200 bpi tape drives, the primary requirement (a large user base) for standardization exists. Why 3200 bpi? The choices in tape density until now have been 1600 bpi tape (46 MB) or expensive 6250 bpi tape (180 MB). The new choice is 3200 bpi tape with 92 MB capacity at a low incremental price ($375) to the standard 1600 bpi tape drive. Substantially less expensive than 6250 bpi with better performance in most applications, Cipher's CacheTape also offers the added benefit of standardization.

Start/Stop Performance

CacheTape provides superior performance versus tension arm, vacuum column, 100/25 ips streaming, and 50 ips 6250 bpi (GCR) tape drives. As an example, the following benchmark comparison provides typical performance data for a file-oriented backup application:

	Benchmark Time*
Streaming Tape (variable speed, 1600 bpi)	.23 min.
Vacuum Column (125 ips, 1600 bpi)	.7 min.
CacheTape Model 891 (1600 bpi)	**.7 min.**
50 ips 6250 bpi (GCR)	6.4 min. (calculated)
CacheTape Model 891 (3200 bpi)	**.5.9 min.**

*Benchmark measured on a DEC PDP-11/34 under RSTS™ for available tape drives.

**OEM Quantities

RSTS is a registered trademark of Digital Equipment Corporation.

UNIX is a trademark of Bell Laboratories.

For higher capacity disk backup, 3200 bpi density offers 184 MB of disk backup with only one reel change.

CacheTape offers field-proven streaming mechanics, fully automatic loading and threading, and compact package size...and still performs disk backup and transactional applications as well. CacheTape is the total solution to your tape drive needs.

Call or write for a free benchmark brochure that explains the performance advantages and how to calculate in advance the benefits of CacheTape.

Tape Adapter Compatibility

CacheTape easily interfaces and operates with industry-standard tape adapters. CacheTape is completely interface compatible with existing couplers for products from DEC, DG, and TI, and couplers for Multibus, S-100, and other popular mini- and microcomputers. Take advantage of CacheTape's easy integration features and increase your system performance while eliminating extra time and expense from your budget. With CacheTape, you can use your current controller investment wisely and effectively... plug in CacheTape for immediate benefits.

Software Transparent

Cipher's CacheTape products are completely software transparent with current vacuum column or tension arm start/stop tape software. CacheTape provides start/stop tape performance for tape applications such as file-oriented disk backup, transactional journaling, tape sort/merge, and data acquisition. Utilization of a cache memory in the tape drive means that CacheTape can provide higher performance than existing tension arm or vacuum column tape drives at much less cost. Just plug CacheTape into your system now...and benefit from total software compatibility.

Up to 40% Less Cost

CacheTape Model 891 (with 1600 bpi)	**$3420****
CacheTape Model 891 (with 1600/3200 bpi)	**$3795****
versus 125 ips vacuum column	**$6100**
versus 50 ips 6250 bpi (GCR)	**$7000** (estimated)

UNIX Friendly

UNIX™—the emerging operating system of the 80s—now has with CacheTape an easily integrated, low cost, standard tape drive with superior performance. Do other alternatives make sense anymore... particularly if software development time and resources are scarce?

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Telex: 521-4094

Data-over-voice

(continued from page 68)

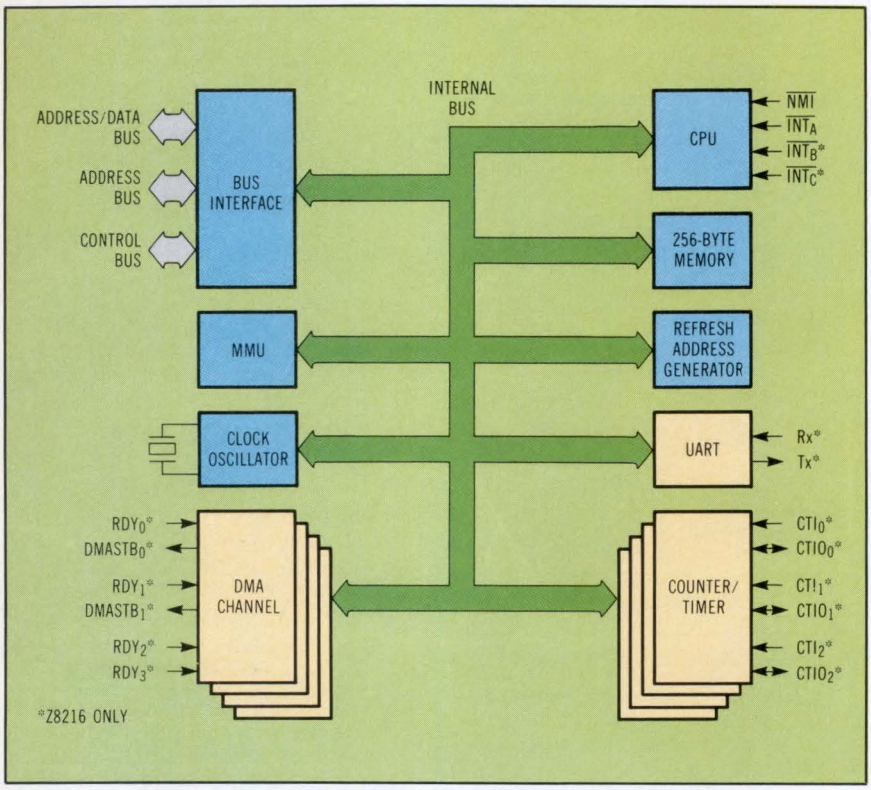
multiplexer, or data PBX. To aid in normal PBX operations, the control signals on the voice line are retained.

System designers considering data-over-voice implementations should evaluate the different products' advantages and disadvantages. For instance, the total cable distance traveled must be balanced against required transmission speeds and overall cost. Configuration and pricing information are available from the manufacturers.

—Joseph Aseo, Field Editor

MICROPROCESSORS/MICROCOMPUTERS

Z80 code expands into large systems



The Z8216, a full-feature member of the Z800 family, incorporates four DMA channels, four counter/timers, and 24 bits of address space with memory management. The CPU is fully compatible with the Z80 instruction set and supports additional instructions.

An 8-bit Z80 compatible microprocessor with onchip memory management and peripherals expands Z80 code into the world of higher performance systems. Zilog's Z800 can address 16M bytes of memory and execute code at 1M to 5M instructions/s depending on the data bus width. The microprocessor supports all documented Z80 opcodes and runs all Z80 programs with the proviso that existing timing loops may have to be adjusted to accommodate the Z800's faster execution speed. The system provides Z80 software a migration path into higher performance systems using the latest 16-bit peripherals. It also includes large address spaces and enhanced microprocessor capabilities for advanced designs.

Actually, the processor comprises a family of four chips: the Z8108 and Z8208 support 8- and 16-bit nonmultiplexed bus peripherals, respectively, and the Z8116 and Z8216 support Z-Bus multiplexed 16-bit peripherals that are also used with the Z8000. The family is further divided into two package sizes—a 40-pin (Z8108 and Z8116) and a 64-pin (Z8208 and Z8216).

Both 40-pin packages are limited to 19 bits of address space and do not support the onchip peripheral. The 64-pin versions support all 24 bits of address and onchip peripherals including one onchip UART, three counter/timers, one timer, dynamic memory refresh circuitry, and four DMA channels.

An onchip memory management unit (MMU) divides the 64K-byte logical address space manipulated by Z80 programs into pages. It then maps these pages into the Z800's larger physical address space. Depending on whether or not the Z800's program/data separation is enabled, these pages are either 8k or 4k bytes in length. Using this technique, 16-bit logical addresses are translated into 24-bit physical addresses for the Z8208 and Z8216, or into 19-bit physical addresses for the Z8108 and Z8116.

Memory management techniques used by the Z800 allow system and user modes of operation and also the separation of programs and data. Address translation, which can be done in both system and user modes, can also be done so that instruction references are separated from data references. This separation allows programs up to 64K bytes long to manipulate up to 64K bytes of data without operating system intervention.

Including different types of commonly used peripherals onchip reduces system cost and design complexity. In addition to the peripherals mentioned, all family members contain an onchip oscillator/clock generator and programmable refresh circuitry for dynamic memories. All onchip peripherals lie in standard Z80 I/O address space and can be accessed by Z80 I/O instructions. In addition, some of the

(continued on page 72)

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CIRCLE 49

Z80 code expands

(continued from page 70)

devices can be linked internally to increase their capabilities and speed throughput.

All Z800 family members use a superset of the Z80 register set. Among the additional registers is a user stack pointer that, with the system stack pointer, supports the dual mode of operation. Two bus timing registers are also included: the bus timing and control register and the bus timing and initialization register. These registers aid in programming wait states for memories of differing speeds and for operations such as daisy chain timing. An added I/O page register expands the I/O address space. It consists of 8 bits that are added to the 16 bits normally output for Z80 I/O operations. These extra bits allow pages of I/O addresses to be generated in a manner analogous to memory page addressing.

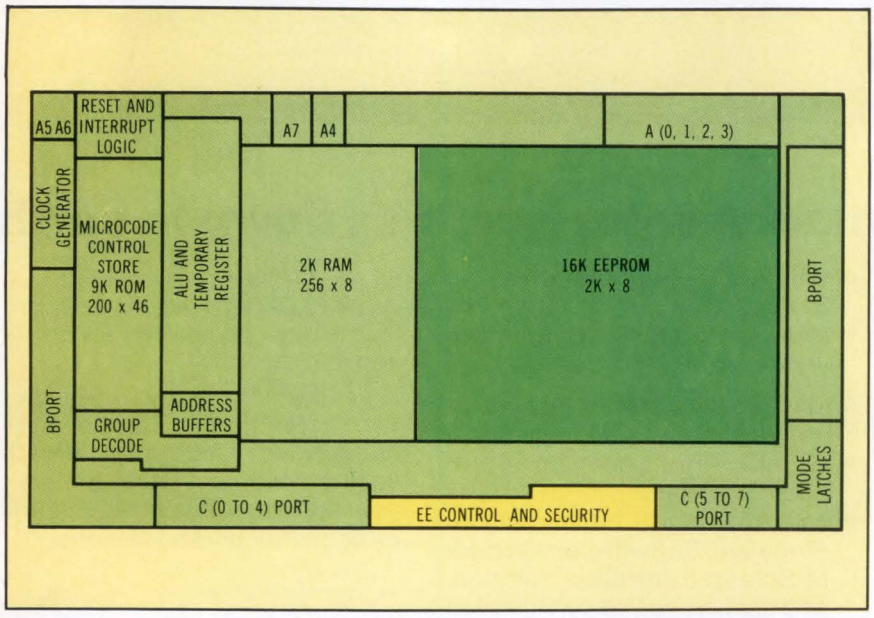
In addition to Z80 interrupt modes 0, 1, and 2, a new mode, 3, is a service interrupt mode intended to handle interrupts and traps. Mode 3 looks at an interrupt/trap vector table to find a new program status value table. These values consist of a new program counter value and a new master status register value in the case of a trap or nonvectored interrupt. For vectored interrupts, the old program counter and master status register are saved and a vector is read from the interrupting device. This method allows complete nesting of interrupts as the state of the previous interrupt enable is saved on the stack.

A number of trap conditions are internally defined in hardware for system protection; normally, software cannot disable them. These conditions include extended instruction traps, which signal attempts at extended instructions when the extended processing architecture is disabled; division exception trap to prevent division by zero; and a system call trap to provide orderly transition between system and user mode. These and other traps enable the designer and user to easily detect conditions that may adversely affect code execution or system operation.

Finally, in order to allow multiple processors to use the bus, the Z800 family supports a global/local bus option and an external bus arbiter to resolve bus contention. **Zilog Corp**, 1315 Dell Ave, Campbell, CA 95008.

Circle 245

Embedded EEPROM is reprogrammed in-circuit



The Seeq 72720 self-adaptive microcomputer addresses applications requiring remote programming ability. These applications include robotics, learning machines, laboratory instruments, and maintenance diagnostic equipment. This microcomputer is also designed for applications requiring nonvolatile memory that can be erased and programmed without removal from the system.

One of the advantages of embedding nonvolatile electrically erasable read only memory (EEPROM) onboard single-chip microcomputers is that the EEPROM can be erased and reprogrammed without removal from the system. Although not frequently valuable because the reprogramming procedure is still slow, this feature will become much more important as procedure time diminishes. The first such devices will result from an agreement between Seeq Technology, Inc, and Texas Instruments to apply Seeq's EEPROM technology to TI's TMS7000 family of 8-bit single-chip microcomputers.

Under the terms of the agreement, Seeq will develop versions of the TMS7000 using a 2K x 8-bit 5-V only EEPROM in place of TI's standard ROM. Several different family members will be produced with the integrated EEPROM, providing a range of capabilities. Seeq will then make available the resulting integrated microcomputer packages to TI starting in 1984. The first part to be produced, a 72720 self-adaptive microcomputer, is targeted for applications that require remote programming ability.

Functionally and electrically interchangeable with the TMS7020, the Seeq 72720 includes an additional program instruction that allows the device to program and alter its own nonvolatile EEPROM. It also has an additional 128 bytes of internal RAM for a total of 256 bytes. Additional registers and control logic forbid external access to the internal program memory after the stored program has been verified and execution has begun.

(continued on page 74)

VISUAL 300/330.

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Both the VISUAL 300 and VISUAL 330 combine VISUAL ergonomic elegance with excellent emulation capability.

For example, the VISUAL 300 complies to the ANSI X3.64 standard and is protocol-compatible with DEC VT100/VT52® terminals. And the VISUAL 330 emulates the DEC VT52, Lear Siegler ADM-3A,™ Data General D200, and Hazeltine 1500.

Nothing compares to these VISUAL terminals when it comes to ergonomics. They are designed in lightweight plastic and can easily be swiveled and tilted for maximum operator comfort. A "menu-style" set-up mode eliminates all cumbersome switches. Other human design features include:

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The versatile VISUAL 300 and 330 offer a package of standard features unmatched by any terminal in their class:

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All this at surprisingly low prices. Call for details on the VISUAL 300 and 330—the flexible terminals.

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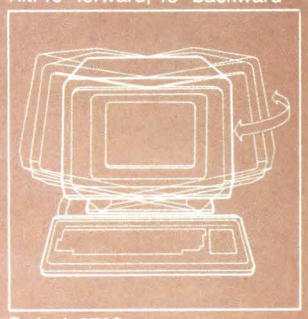

Swivel: 270°

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CIRCLE 50

Embedded EEPROM

(continued from page 72)

Information can be written into the 72720's program memory by having the CPU execute a single PRG instruction or by applying external address, data, and control signals, as in standard EEPROMs. The CPU's PRG instruction uses the TMS7000's indirect addressing mode to load data from the accumulator into the address pointed to by a register pair. Under CPU control, a byte of memory can be programmed in 13 ms, which allows the 72720 to be remotely programmed via a serial link at rates greater than 600 baud. This is accomplished without data buffering.

Security is implemented by a 1-bit control register in the processor's I/O address space. When this bit is set, which can only be done by the CPU, the onchip inhibit logic will block data transfer from the EEPROM to the external data bus. Only an externally generated block erase, which also erases the EEPROM's entire contents, can reset (clear) the inhibit bit. Thus, the user can be assured that proprietary program code cannot be read once the system is activated.

Remote and self-adapting programming abilities will allow designers to build systems whose software can be altered to suit an application's requirements without human intervention. Such products can also be designed to modify the programs or data in their own memories as circumstances dictate.

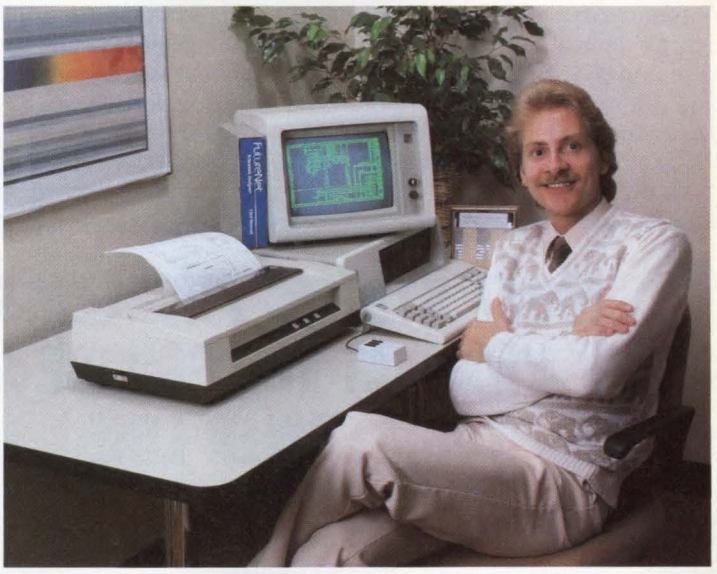
With appropriate software, remote servicing, such as uploading stored data and downloading new programs or parameters, can be done by telephone. Maintenance diagnostic monitors can be installed in equipment located in remote areas, with the 72720 tracing and recording operational sequences up to and including failures.

By itself, the Seeq 72720 is not particularly impressive in terms of speed or capabilities—equivalent performance could be obtained by using an EEPROM and a conventional microprocessor. However, when the principle behind the 72720 is applied to other architecture, significant gains in both speed and functionality can be expected. Using CMOS technology, for instance, will significantly decrease power consumption. Two-micron design rules, along with optimized microcode and chip layout, will also heighten performance.

With a tenfold speed increase that is possible with improvements in the EEPROM portion of the microcomputer, the devices will be very useful in applications such as voice technology. Realtime adaptive filtering, fast Fourier transforms, and pattern recognition will be both possible and cost effective. **Seeq Technology, Inc**, 1849 Fortune Dr, San Jose, CA 95131.

Circle 246

THE AGONY & THE ECSTASY



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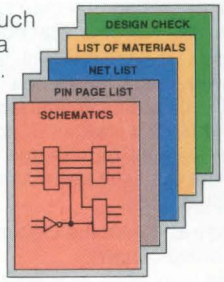

DASH-1 does much more than create a perfect schematic. With your design data captured automatically on disk, essential documents — Net Lists, Lists of Materials, Design Check Reports — can be produced at will. Think of the hours of drudgery you'll save by eliminating these time-consuming, error-prone tasks. Plus, you'll have peace of mind knowing that DASH-1 will locate many common design errors before they reach the hardware stage.

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CIRCLE 52

Chips gain speed and flexibility

A family of high speed digital processing chips with a 200-ns cycle time and a 5M-instruction/s execution time has been announced by Texas Instruments. One member of the family, the TMS320, is presently being sampled for applications such as image processing, speech recognition and synthesis, and instrumentation control.

While this device is especially fast—its 60-member instruction set consists primarily of single-cycle and single-word instructions—it has been optimized for control and computation and not for use as a general purpose CPU. Also, its onboard RAM is adequate for 64-point fast Fourier transform implementations. The company intends this chip as a replacement for multichip bit-slice devices available now.

Based on a modified Harvard architecture (separate data and program memories), the chip allows transfer between the two memory areas. In this way, constants can be stored in program memory and program branches can be taken on the basis of data computations. Data memory consists of 144 16-bit words of onchip static RAM.

A fast arithmetic logic unit (ALU) on the chip can multiply two 16-bit signed 2's complement numbers in 200 ns to form a 32-bit product. Although the ALU maintains all operands internally as 32-bit numbers, input and output are 16 bit. A single-cycle 0- to 16-bit barrel shifter and the ability to use offchip RAM or ROM further increase device flexibility.

First versions of the chip use different methods of storing programs: the TMS320M10 microcomputer version has 3K bytes of masked ROM onboard, while the TMS32010 microprocessor version can use up to 8K bytes of external memory. The SMJ32010 is a MIL-STD-883B version of the microprocessor.

The chip family is fabricated using silicon gate NMOS and 2.7-micron design rules. It operates from single 5-V power supplies, typically dissipates 950 mW, and is provided in standard 40-pin plastic or ceramic DIPs.

Samples are now being provided, and production quantities will be available soon. In 100-piece quantities, devices are $120 in ceramic packages and $105 in plastic. The military version price is $577.43 in 100-piece quantities. **Texas Instruments, Semiconductor Group,** PO Box 401560, Dallas, TX 75240.
Circle 247

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But it won't overpower your budget. Buy only what you need. Tower 1632 will arrive from the factory tailored for any application from one to sixteen users.

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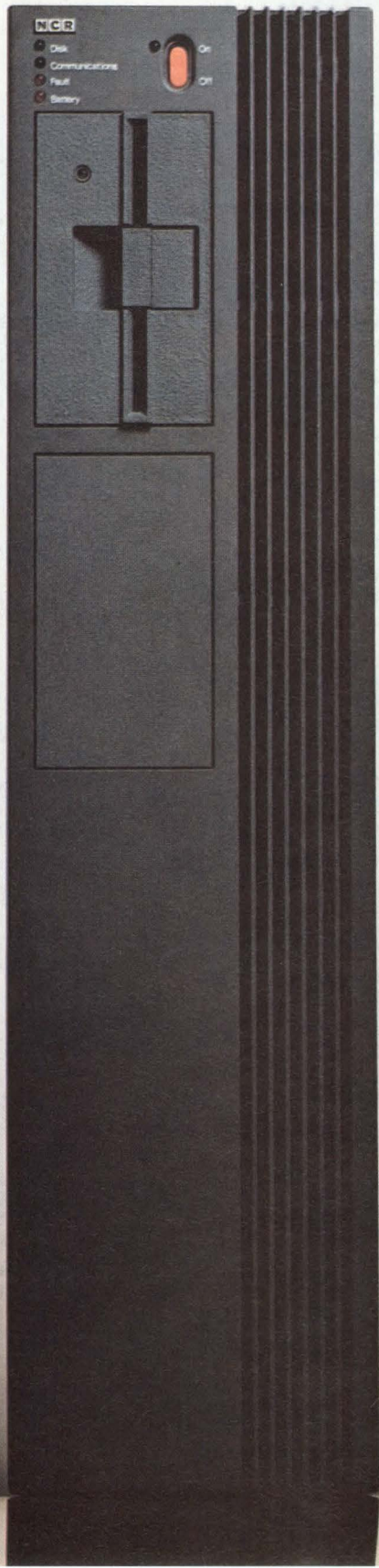

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CIRCLE 54

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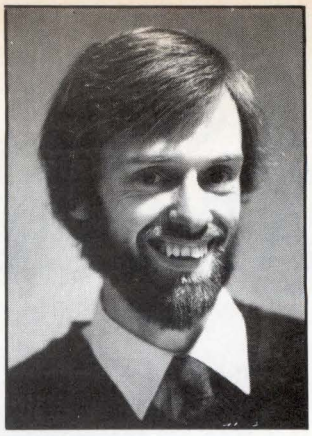
SIGGRAPH'83

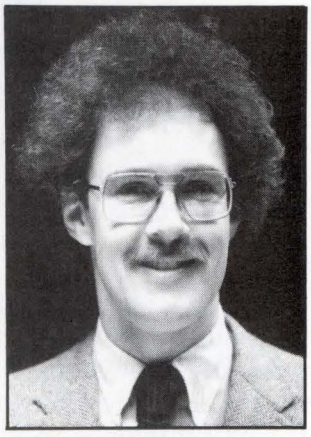
Conference on Computer Graphics and Interactive Techniques

Cobo Hall, Detroit, Michigan
July 25 to 29, 1983



Peter Tanner
Technical Program Chair

Kellogg S. Booth
Conference Cochair



John C. Beatty
Conference Cochair

Drawing from a growing repertoire of computer graphics installations, SIGGRAPH '83 exhibitors and Technical Program speakers are expected to plumb every aspect of computer graphics design. An exhibitor forum adjacent to exhibition areas will host product expositions on hardware trends, CAD/CAM/CAE, and future applications. Strong showings are expected in the fields of engineering workstations; refresh vector, raster, and storage tube display systems; graphical input; image processing; film/paper hardcopy equipment; and software support.

The 10th annual conference is sponsored by the Association for Computing Machinery's Special Interest Group on Computer Graphics in cooperation with the Engineering Society of Detroit, IEEE Technical Committee on Computer Graphics, and Eurographics.

Formal presentations at SIGGRAPH are broken up into two groups: tutorial/seminar courses during the first two days of the conference, and Technical Program panels/paper presentations over the remaining three days. Technical Program sessions likely to interest *Computer Design* readers are listed on the following pages.

Locations for the full-day tutorial/seminar courses are being scheduled concurrently at Cobo Hall, Westin Hotel, Veterans Memorial Building, and the Engineering Society of Detroit. One 2-day tutorial will introduce both graphics application software development and the Graphical Kernel System (GKS) being developed by ANSI and ISO. Session 6, which is geared to software engineers who plan to use GKS, will examine practical applications of the standard as well as the problem of converting existing applications to GKS.

Distributed Graphics Systems (Session 21 on Tuesday) will discuss how to provide integrated graphics capabilities through a network of processors, computers, and data facilities. Lecturers will explain how to design fairly independent functional modules for allocation in a distributed network.

Monday's Session 11 will introduce general issues and future trends in CAD/CAM/CAE, before exhibiting vendors in companion Session 12 give technical descriptions of their CAD systems the next day. Alternately, scheduling Session 13 for Monday will open up the tutorial on solid modeling for mechanical CAD/CAM/CAE applications. Starting with basic principles, representations/algorithms, applications, and systems, the meeting will proceed to examine recent research as well as a contemporary solid modeler. Advanced topics will be pursued Tuesday during Session 14, when speakers will delve into oct-tree representations, Boolean operations, finite element meshes generation, and robot simulation.

Other promising options include Monday's Session 16, during which the role of interactive graphics in VLSI design and the use of VLSI in computer graphics systems will be considered.

Throughout the conference, a juried art show will display computer-generated sculpture, drawings, prints, and murals. Video and film works will be shown with frame buffer and interactive installations. In addition, film and video programs on Tuesday and Wednesday nights will screen sophisticated scientific, artistic, and commercial motion graphics.

For registration information, contact
ACM SIGGRAPH '83, PO Box 72045, Chicago, IL 60690.
Tel: 312/644-6610

(continued on page 80)

Black and white facts about color graphics.

Fact 1.
Software development is expensive.

Raster Technologies' Model One graphics systems feature software tools that speed application development. Like an integrated local debugger. Command stream translator. Local command execution. A complete HELP facility. And truly easy to use macro programming. These unmatched software tools save you time and money.

Fact 2.
Software redevelopment is even more expensive.

With Raster Technologies' fully compatible Model One family, you can take advantage of the latest hardware without any software rewrites. This means an easy upgrade to a more powerful product while still using the same graphic commands, program development tools and host library. So the application developed for the best hardware today can run on the best hardware tomorrow. Without modification.

Fact 3.
Performance is a lot more than good specs.

Graphics performance goes beyond pixel and vector timing specs. It is the ability to display a complex picture without having to wait. Provide instantaneous interaction between an application program and its user. And efficiently communicate with a host computer. The kind of total graphics performance you should measure before you buy.

Fact 4.
Graphics applications demand flexibility.

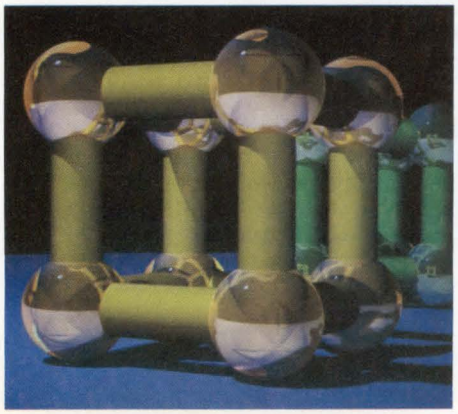
The Model One family from Raster Technologies offers maximum flexibility at the lowest cost. Because it lets the user select the combinations of display resolution, color and refresh rates that are right for that particular application. Factors that are different for every application.

Fact 5.
Graphics technology is moving fast.

Raster Technologies is dedicated to one business: graphics. All our development efforts focus on advancing graphics technologies. With the latest microcircuitry. The newest and fastest microprocessors. The most advanced display list architectures. And the most innovative pipelined multiple processor designs. All to advance graphics capabilities compatibly. And keep today's customers with us tomorrow.

Fact 6.
You should benchmark the Model One.

The Model One/25 features vivid full color imaging performance with 512 x 512 resolution. The Model One/40 features ultra high 1024 x 1024 resolution. The Model One/60 features 100% flicker-free 60 Hz non-interlaced display with 768 x 576 resolution. All support our Advanced Graphics Application Development Firmware and powerful display list package. Put the Model One family to the test.



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See Us at Booth #1832 at NCGA

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CIRCLE 55

(continued from page 78)

Technical Program Excerpts

Image Generation I
Wed 9 to 10:30 am, Cobo Arena

Chair: E. Catmull, Lucasfilm

"Pyramidal Parametrics"
L. Williams, New York Institute of Technology

"Lighting Controls for Synthetic Images"
D. R. Warn, General Motors Research Labs

"Artificial Texturing: An Aid to Surface Visualization"
D. Schweitzer, University of Utah

Computer Graphics in Higher Education
Wed 9 to 10:30 am, Cobo Hall A

Chair: J. D. Foley, George Washington University

Panelists: A. Bork, University of California, Irvine; M. Brown, Digital Productions; R. King, Sheridan College; A. van Dam, Brown University; and M. Wozny, Rensselaer Polytechnic Institute

Courtesy: Monique Nahas and Hervé Huitric, Paris, France, and SIGGRAPH '83.

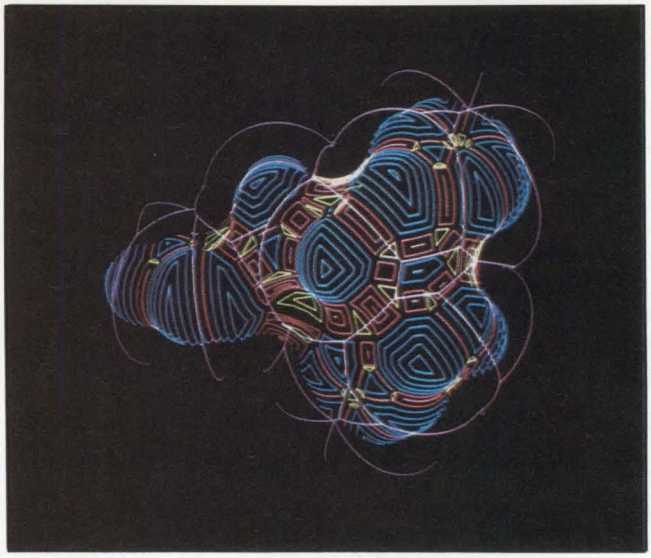
User Interface
Wed 10:45 am to 12:15 pm, Cobo Arena

Chair: D. Bergeron, University of New Hampshire

"Towards a Comprehensive User Interface Management System"
W. Buxton, M. R. Lamb, D. Sherman, and K. C. Smith, University of Toronto

"Syngraph: An Automatic Interaction Generator"
D. R. Olson, Jr and E. P. Dempsey, Arizona State University

"A Graphics Editor for Benesh Movement Notation"
B. Singh, Schlumberger-Doll Research; and J. C. Beatty, K. S. Booth, and R. Ryman, University of Waterloo



Courtesy: Michael Connolly, Scripps Clinic and Research Foundation, and SIGGRAPH '83.

Advances in New Display Technology
Wed 10:45 am to 12:15 pm, Cobo Hall A

Chair: S. Sherr, Westland Electronics

Panelists: I. Chang, IBM Corp; T. Maloney, PanelVision; P. Pleshko, IBM Corp; E. Schlam, Eradcom; and P. Seats, Thomas Electronics

Raster Algorithms
Wed 3:45 to 5:30 pm, Cobo Arena

Chair: A. Fournier, University of Toronto

"Near-Realtime Shaded Display of Rigid Objects"
H. Fuchs, G. D. Abram, and E. D. Grant, University of North Carolina, Chapel Hill

"A Scan-Line Hidden Surface Removal Procedure for Constructive Solid Geometry"
P. R. Atherton, General Electric Co

"Ray Tracing Algebraic Surfaces"
P. Hanrahan, University of Wisconsin, Madison

"Ray Tracing Fractal Surfaces"
J. T. Kajiya, California Institute of Technology

Technical Implications of Proposed Graphics Standards
Wed 3:45 to 5:45 pm, Cobo Hall A

Chair: D. Straayer, Tektronix Inc

Panelists: P. Bono, Athena Systems; R. Ehlers, Evans & Sutherland Computer Corp; G. Enderle, Karlsruhe Nuclear Research Centre; T. Reed, Los Alamos National Lab; D. Shuey, McDonnell Douglas Automation; M. Skall, National Bureau of Standards; E. Sonderegger, SIGGRAPH; and T. Wright, ISSCO

(continued on page 82)

*Technical Program sessions are subject to last-minute changes.

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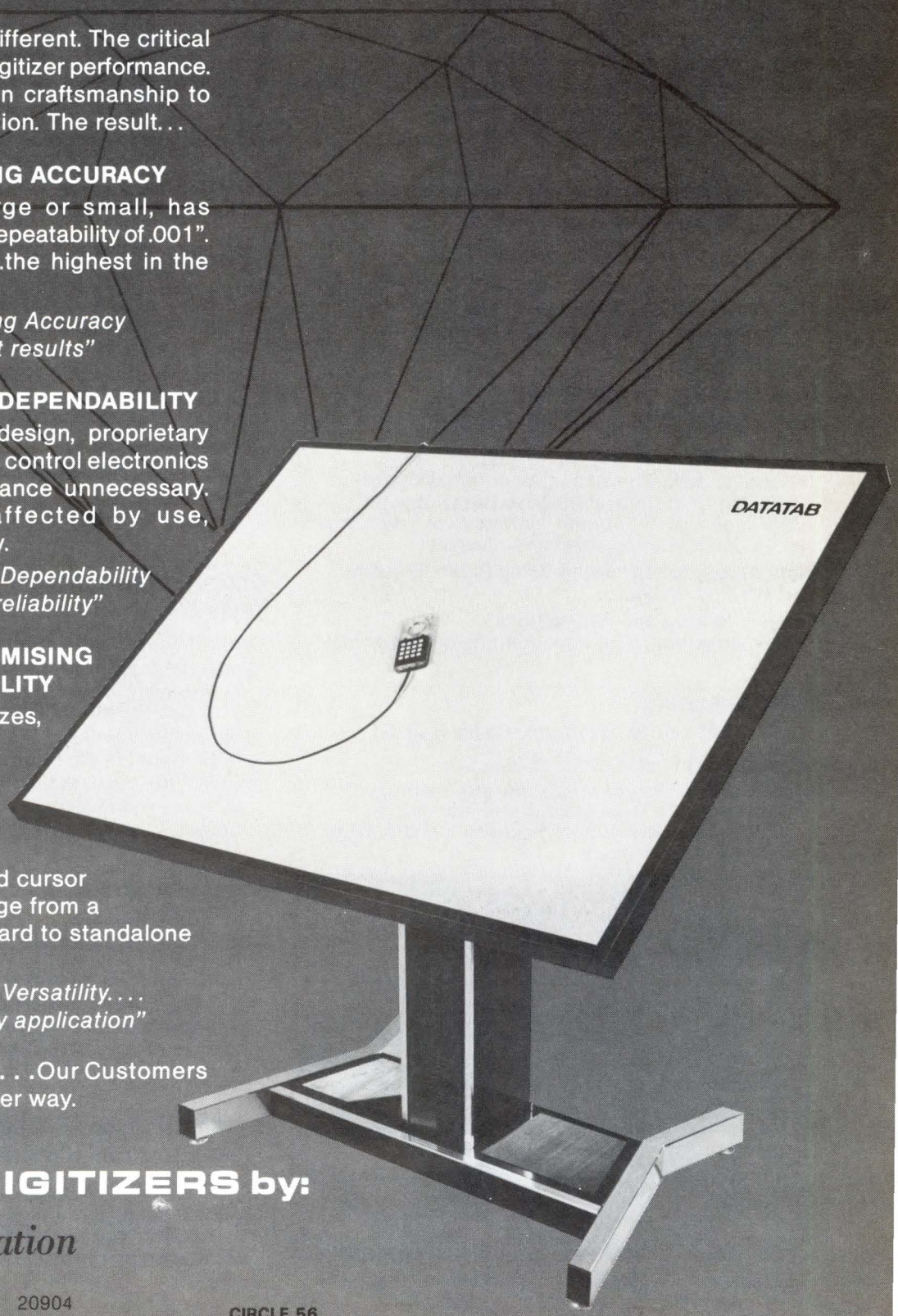

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CIRCLE 56

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(continued from page 80)

Applications

Thurs 9 to 10:30 am, Cobo Arena

Chair: H. Freeman, Rensselaer Polytechnic Institute

"Computer Graphic Modeling of American Sign Language"
J. Loomis, H. Poizner, U. Bellugi, and A. Blakemore, The Salk Institute of Biological Studies; and J. Hollerbach, Massachusetts Institute of Technology

"Incense: A System for Displaying Data Structures"
B. A. Myers, Xerox Palo Alto Research Center

"Graphical Style—Towards High Quality Illustrations"
R. J. Beach, University of Waterloo; and M. Stone, Xerox Palo Alto Research Center

The Simulation of Natural Phenomena

Thurs 9 to 10:30 am, Cobo Hall A

Chair: C. A. Csuri, Ohio State University

Panelists: J. Blinn, Jet Propulsion Lab; J. Gomez, Ohio State University; N. Max, Lawrence Livermore National Lab; and W. Reeves, Lucasfilm

Anti-Aliasing Techniques

Thurs 10:45 am to 12:15 pm, Cobo Arena

Chair: J. Clark, Stanford University

"A Parallel Scan Conversion Algorithm with Anti-Aliasing for a General-Purpose Ultracomputer"
E. Fiume and A. Fournier, University of Toronto; and L. Rudolph, Carnegie-Mellon University

"Anti-Aliased Line Drawing Using Brush Extrusion"
T. Whitted, Bell Labs

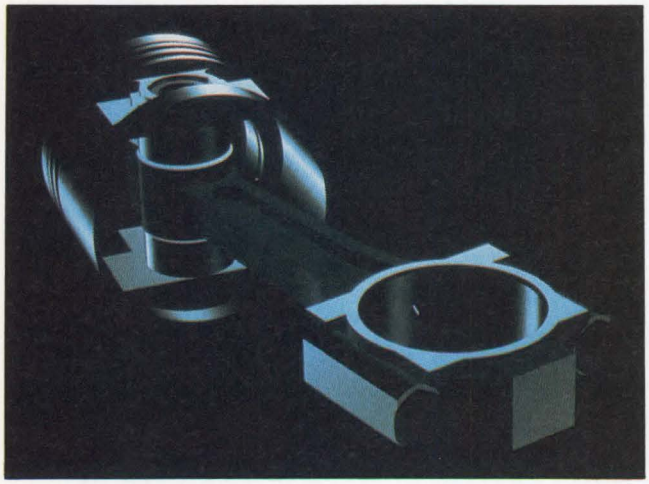
"Edge Inference and Applications"
J. Bloomenthal, New York Institute of Technology

Solid Modeling

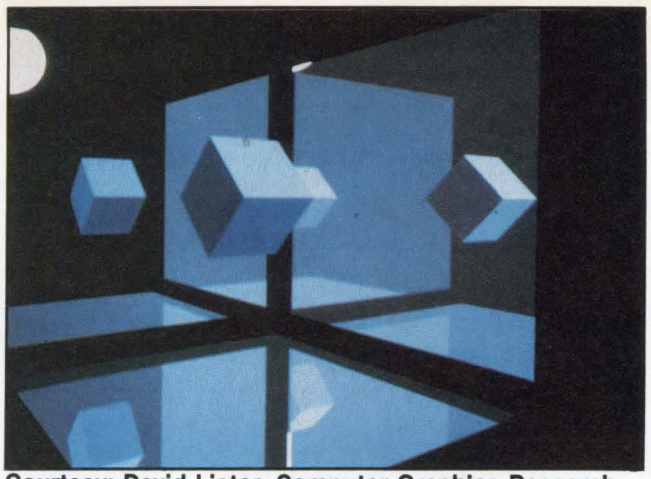
Thurs 10:45 am to 12:15 pm, Cobo Hall A

Chair: R. N. Goldman, Control Data Corp

Panelists: D. Gossard, Massachusetts Institute of Technology; R. Riesenfeld, University of Utah; H. Voelcker, University of Rochester; and T. Woo, University of Michigan



Courtesy: Ford Motor Co and SIGGRAPH '83.



Courtesy: David Lister, Computer Graphics Research Group, Ohio State University, and SIGGRAPH '83.

Systems and Standards

Thurs 2 to 3:30 pm, Cobo Arena

Chair: R. Hopgood, Rutherford-Appleton Research Labs

"A Device-Independent Network Graphics System"
D. U. Cahn and A. C. Yen, Lawrence Berkeley Lab

"A Core Graphics Environment for Teletext Simulations"
D. F. Dixon, RCA/David Sarnoff Research Center

"Minimal GKS"
R. W. Simons, Sandia National Labs

Shape Representation

Thurs 3:45 to 5:15 pm, Cobo Arena

Chair: R. Riesenfeld, University of Utah

"Local Control of Bias and Tension in Beta-Splines"
B. A. Barsky, University of California, Berkeley; and J. C. Beatty, University of Waterloo

"Topologically Reliable Display of Algebraic Curves"
D. S. Arnon, Purdue University

"Curve-Fitting with Piecewise Parametric Cubics"
M. Plass and M. Stone, Xerox Palo Alto Research Center

Industrial Strategies of Japanese Computer Manufacturers

Thurs 3:45 to 5:45 pm, Cobo Hall A

Chair: T. Kunii, University of Tokyo

Panelists: T. Ikedo, Seillac Company Ltd; K. Ishimura, Yamaha Research Institute; K. Iwata, Graphica Computer Corp; K. Naito, Daini Seikosha; and S. Saimi, Japan Radio Corp

Geometric Input Techniques

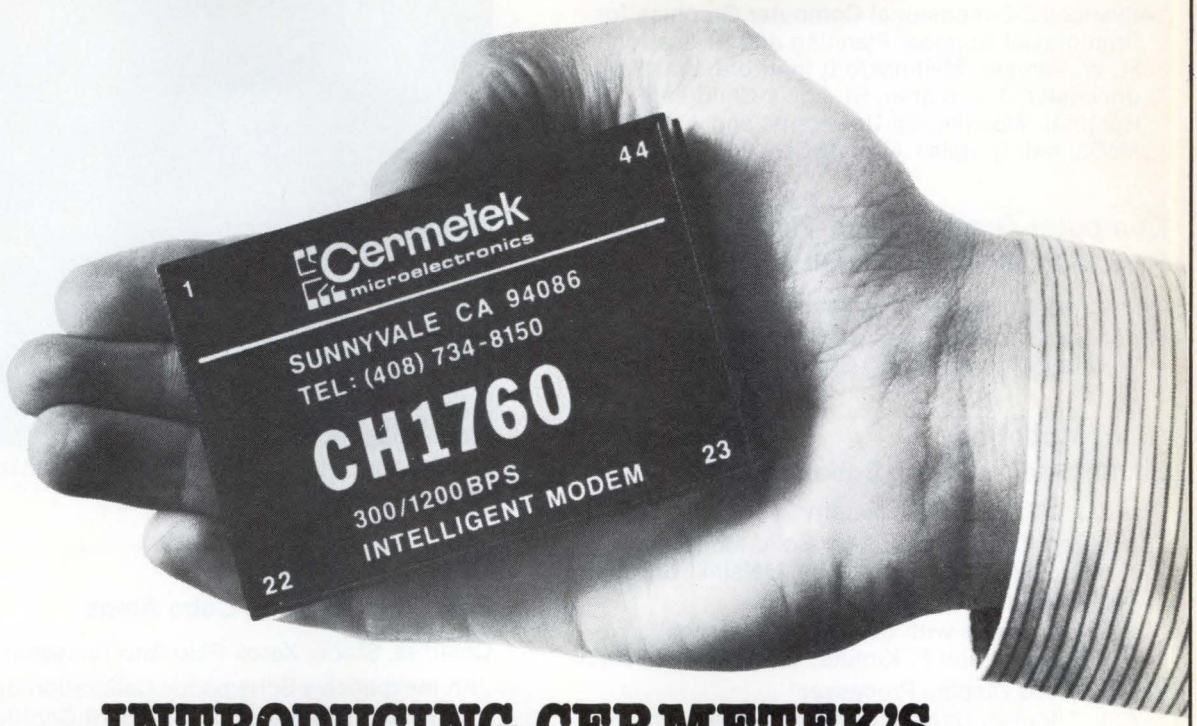
Fri 8:30 to 10 am, Cobo Arena

Chair: I. Carlbom, Schlumberger-Doll Research

"Solid Model Input through Orthographic Views"
H. Sakurai, Nissan Motor Co; and D. G. Gossard, Massachusetts Institute of Technology

(continued on page 84)

FROM THE SIZE OF THIS PAGE TO THE SIZE OF YOUR PALM.



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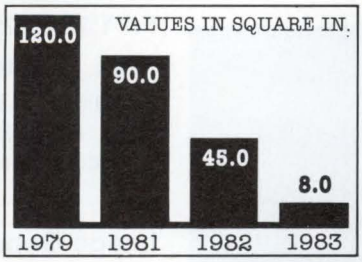

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(continued from page 82)

"Spatial Input/Display Correspondence in a Stereoscopic Computer Graphic Workstation"
C. Schmandt, Massachusetts Institute of Technology

"Advanced 3-Dimensional Computer Graphics for Craniofacial Surgical Planning and Evaluation"
M. W. Vannier, Mallinckrodt Institute, Washington University; J. L. Marsh, St. Louis Children's Hospital, Washington University; and J. O. Warren, McDonnell Douglas Aircraft Co

Computer Graphics and Visual Designers

Fri 8:30 to 10 am, Cobo Hall A

Chair: A. Marcus, Aaron Marcus and Assocs

Panelists: D. Coates, Design Consultant; and W. Mitchell, CAD Design Group

Solid Modeling

Fri 10:15 to 11:45 am, Cobo Arena

Chair: J. Dill, Cornell University

"Localized Set Operations for Solid Modeling"
M. Mantyla and M. Tamminen, Helsinki University of Technology

"Design of Solids with Free-Form Surfaces"
H. Chiyokura and F. Kimura, University of Tokyo

"High Speed Display Processor"
A. L. Thomas, University of Durham

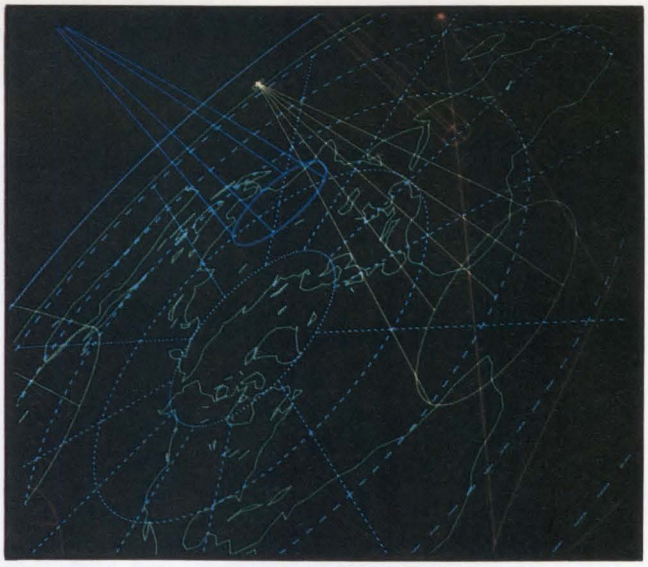
Artists Interfacing with Technology: Basic Concepts of Digital Creation

Fri 10:15 to 11:45 am, Cobo Hall A

Chair: F. Dietrich, West Coast University

Panelists: L. Cuba, Independent Artist; D. Gerbarg, New York University; A. Lippman, Massachusetts Institute of Technology; and D. Sandin, University of Illinois, Chicago

Courtesy: Maria Mezzina, Columbia University, and SIGGRAPH '83.



Courtesy: Patrick C. Orum, Martin Marietta Aerospace, and SIGGRAPH '83.

Raster Techniques

Fri 1:15 to 2:45 pm, Cobo Arena

Chair: M. Stone, Xerox Palo Alto Research Center

"An Inexpensive Scheme for Calibration of a Color Monitor in Terms of CIE Standard Coordinates"
W. Cowan, National Research Council of Canada

"Interactive Image Query System Using Progressive Transmission"
F. S. Hill, Jr, University of Massachusetts; S. Walker, Jr, University of Maine; and F. Gao, Beijin Normal University

"Graphics in Overlapping Bit-Map Layers"
R. Pike, Bell Labs

Solid Modeling: A User Perspective

Fri 1:15 to 2:45 pm, Cobo Hall A

Chair: F. W. Bliss, Ford Motor Co

Panelists: C. Machover, Machover Assocs; M. Smith, Bendix Corp; and C. Vogel, General Motors Corp

Image Generation II

Fri 3 to 4:30 pm, Cobo Arena

Chair: T. Whitted, Bell Labs

"Particle Systems—A Technique for Modeling a Class of Fuzzy Objects"
W. T. Reeves, Lucasfilm

"Temporal Anti-Aliasing in Computer Generated Animation"
J. Korein and N. Badler, University of Pennsylvania

"Modeling Motion Blur in Computer Generated Images"
M. Potmesil, Bell Labs; and I. Chakravarty, Schlumberger-Doll Research □

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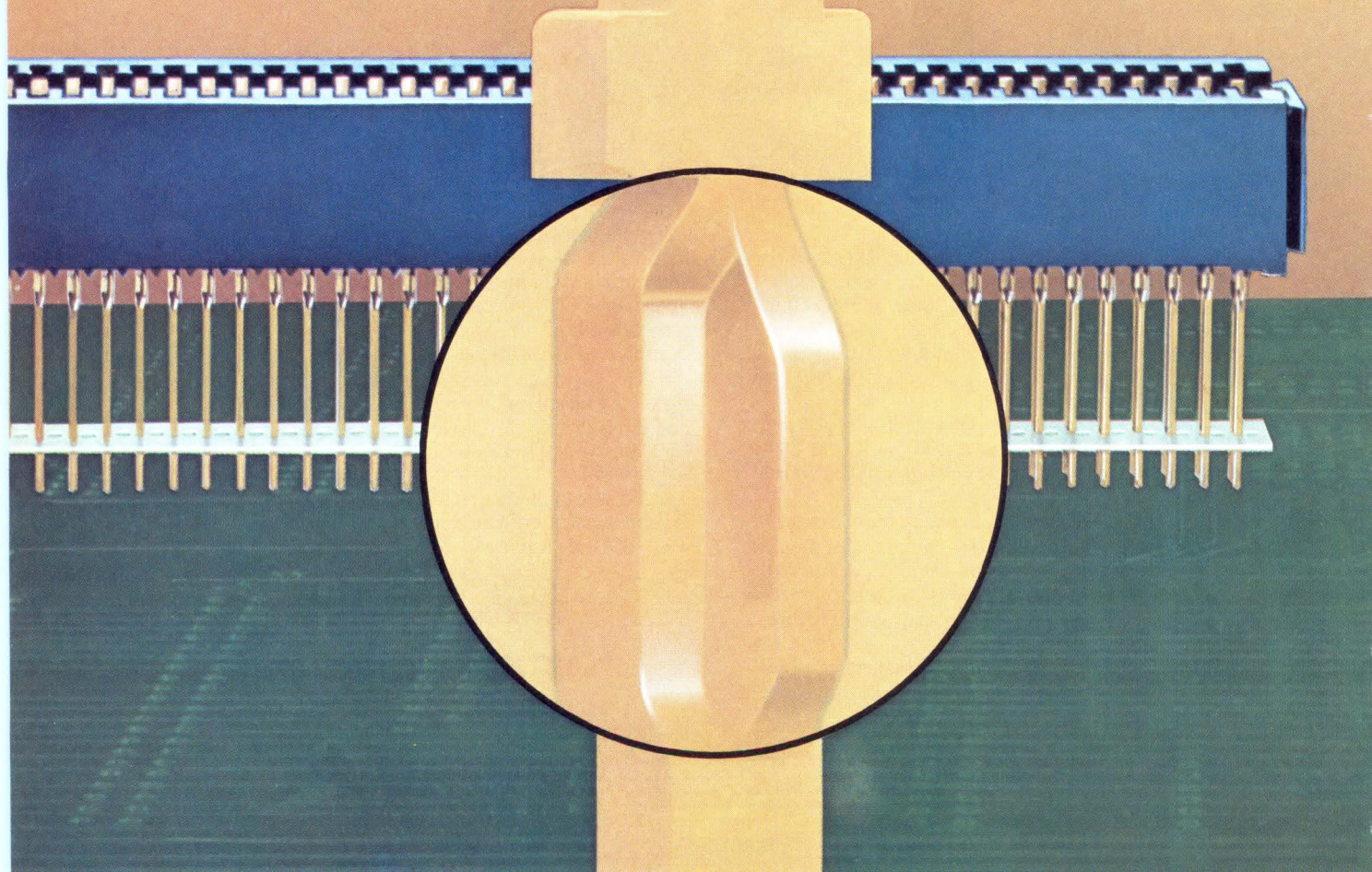
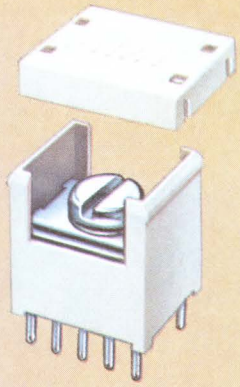


AMP Facts



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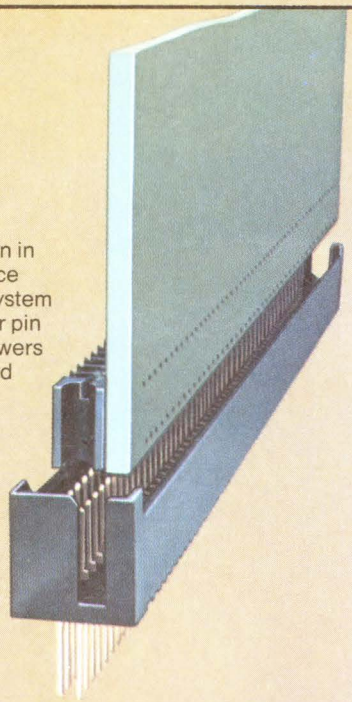

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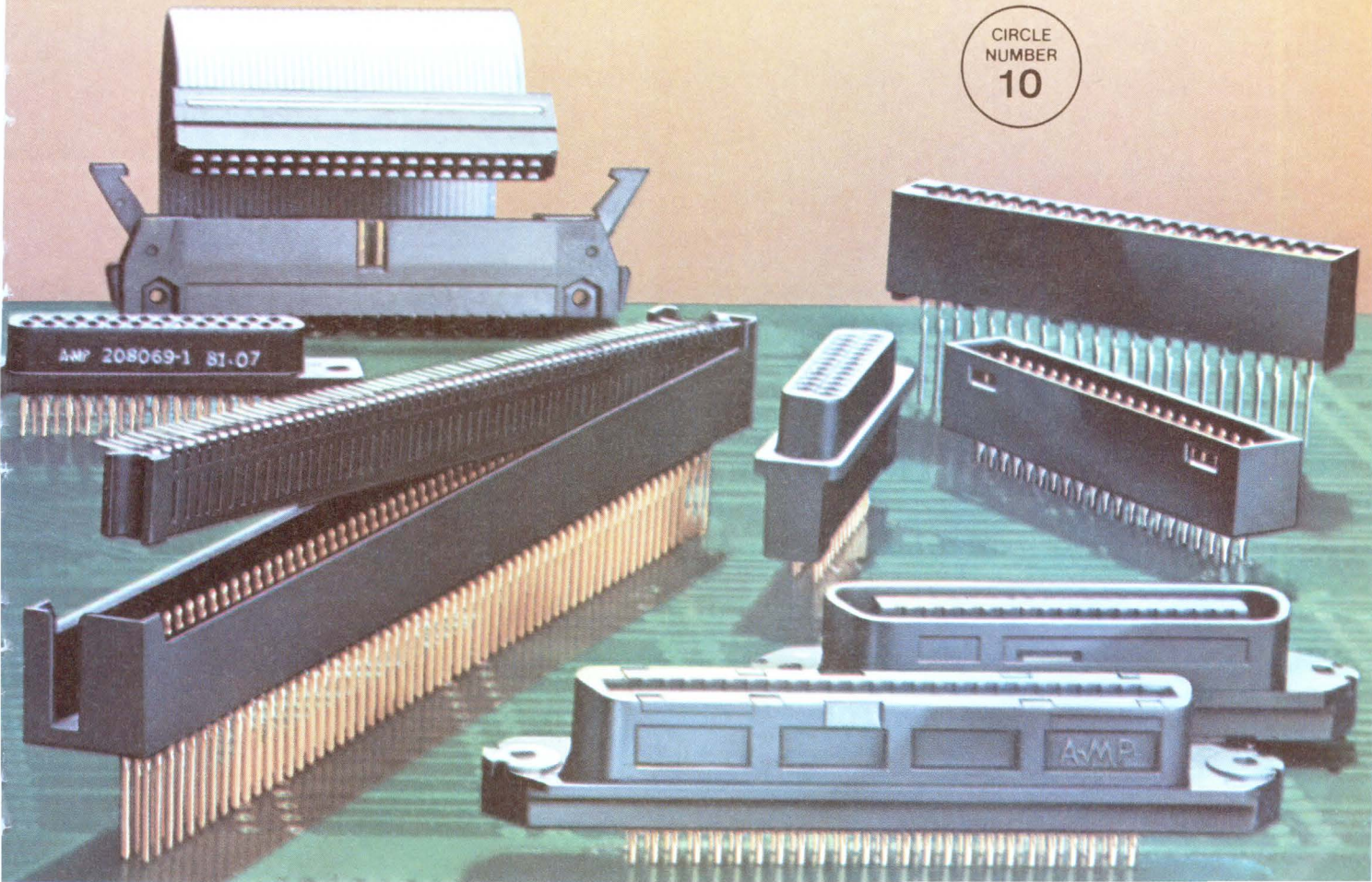

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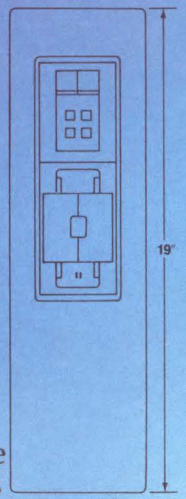

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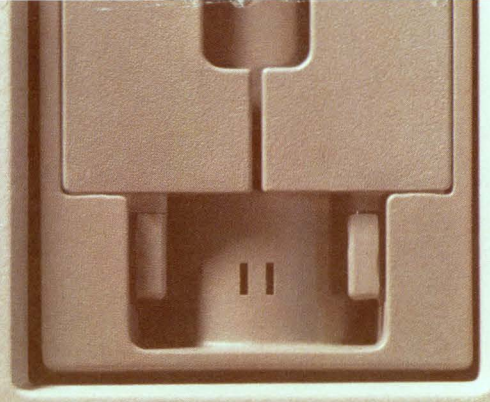

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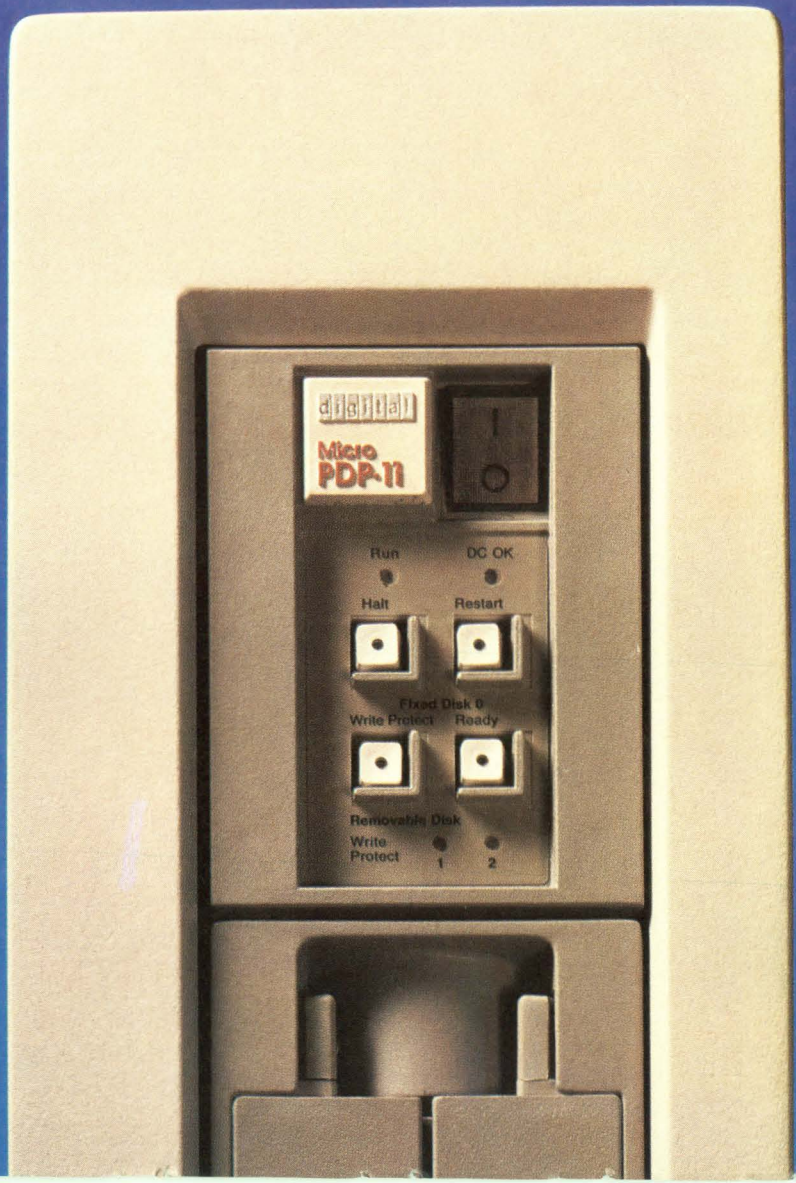

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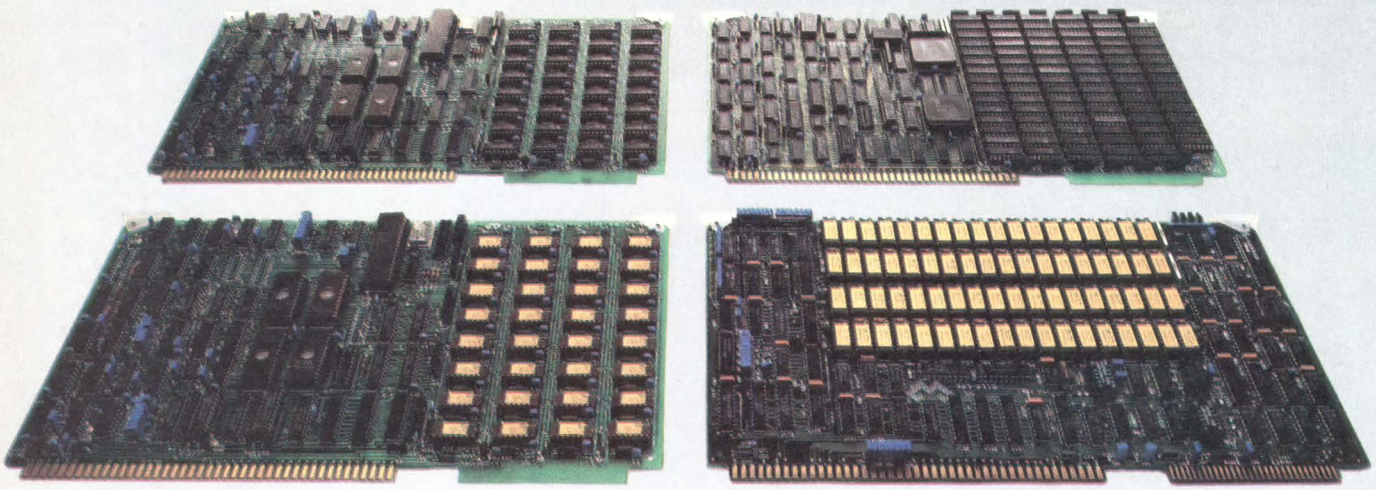

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CIRCLE 59

MANAGING YIELDS BY YIELDING MANAGEMENT TO COMPUTERS

Productivity receives a boost when the precepts of modern data processing are applied to information management in the automated factory.

by Ronald D. Barker

One of the ironies of modern computer technology is that its creators—the engineers—are often the last to reap its benefits. Only recently, computer based tools like computer aided design/computer aided manufacturing and information management systems have made inroads into the design labs of America. For a profession that hastily abandons the slide rule for the electronic calculator, this spotty application of computer technology is, indeed, enigmatic.

Impinging realities of modern economics are changing this situation, however. The push for increased productivity, as exemplified by factory automation, is providing an avenue for the introduction of computer based tools into many facets of manufacturing and design. Unfortunately, much automation is taking place haltingly and haphazardly. As a result, factories are ending up with a diverse mix of tools, systems, and functions that are incompatible and isolated. This being the case, it is often impossible to integrate these elements into a factory-wide information system.

One starting point from which to attack this integration problem is yield management. In addition, the architecture of a system designed to manage yield can also be applied to any highly technical manufacturing environment. The concepts implicit in such architectures are central to factory-wide integration of computer based information management.

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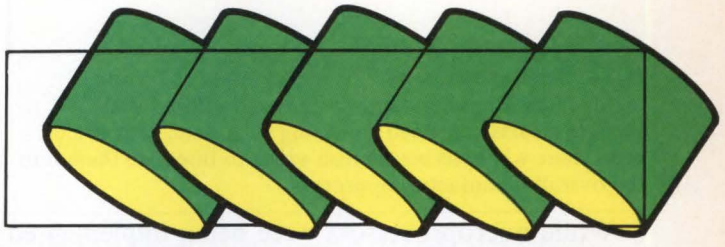

Yield management is defined as the collection and analysis of data, and the presentation of information that enables engineering and production staffs to understand and manage elements that comprise yield within their environment. When, where, and how data are collected and used to effectively manage yield are key issues in the design of such a system. The decisions made during the automation process lay the groundwork for yield management development.

The microprocessor problem

Availability of inexpensive microprocessors has dramatically increased the range of potential applications for computer based automation in manufacturing. However, to fully tap the increased yield potential of these applications, a change must occur in the decision process of what gets automated, and how. Isolated, standalone applications are no longer sufficient. To maximize productivity, systems must be implemented that integrate manufacturing data into a factory-wide information system. This data can then be used to model and manage manufacturing process yields. Yield is defined as the ratio of products passing final test to all products manufactured. Fig 1 points out the inherent isolation and inadequacy of standalone applications. In such situations, correlating manufacturing-step data into the larger world of the factory is extremely difficult.

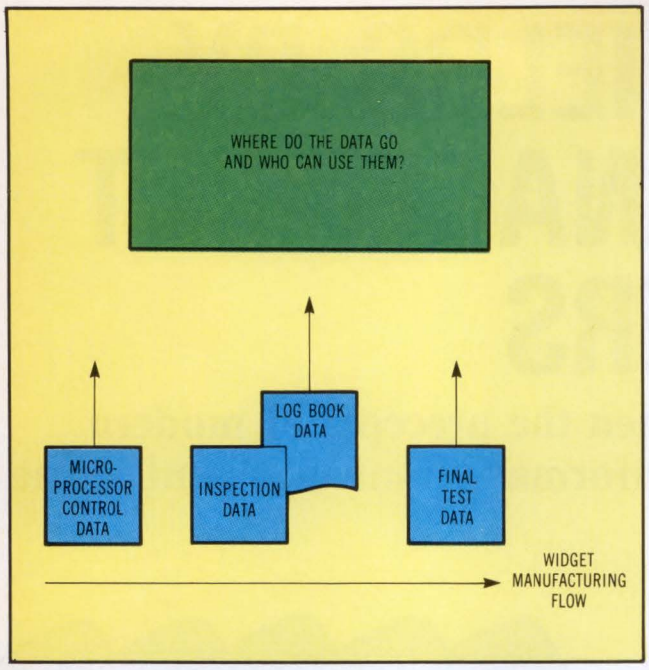

Fig 1 The isolated nature of present data collection methods used in manufacturing provides little benefit. Despite efforts expended collecting such data, they are of little value when no mechanism exists to integrate them into the overall manufacturing process.

While microprocessors were being implemented for manufacturing applications, a different evolution was occurring in the administrative applications of computers in the factory. Typical applications included payroll, billing, and inventory. The administrative environment became characterized by large data processing centers, big mainframe computers, and integrated data bases.

Administrative applications require integrated data bases since orders have a direct relationship to many aspects of the manufacturing exercise including: billing, inventory, and what goes into the salesman's paycheck. The relationship between raw material quality, defect density, process control conditions, and final test results is not as well-defined. However, according to Castrucci et al,[1] it is possible to develop a yield model for semiconductor processes that describes yield as a function of process parameter values. The concept, of course, can be applied to other highly technical manufacturing processes, given the ability to collect, integrate, and present the relevant information.

Key to determining applicability of the yield management concept is the ability to detect defects that lower yields. Once detected, these defects can be related to specific process steps, and then fed back as process corrections based on the defect analysis. For example, in a multiple-step manufacturing operation, defect detection is accomplished by an inspection for quality levels or misprocessing. A measurement for conformance to specifications or a functional test can also be performed. Ideally, the data collected in each detection mode can be analyzed to determine probable cause of the defects. To increase yield, corrections can then be fed back to the process steps that introduced the defects. This closed loop process is illustrated in Fig 2. A problem arises, however, due to the separate evolutions of automation and data processing. Automation processing is distributed; mainframe data processing is centralized. As a result, these opposite ends of the application spectrum must be the starting point for developing an integrated yield management system.

Yield management system

Four steps are required to develop and implement a yield management system. First, yield must be defined. Yield usually means different things to different people in the factory. Exactly how yield is defined is not as important as the consistency with which the definition is observed. Everyone who participates in managing the factory yield, from process step operator to plant manager, must embrace the same definition of yield. In its simplest sense, yield is defined as the ratio of products passing final test to all products manufactured.

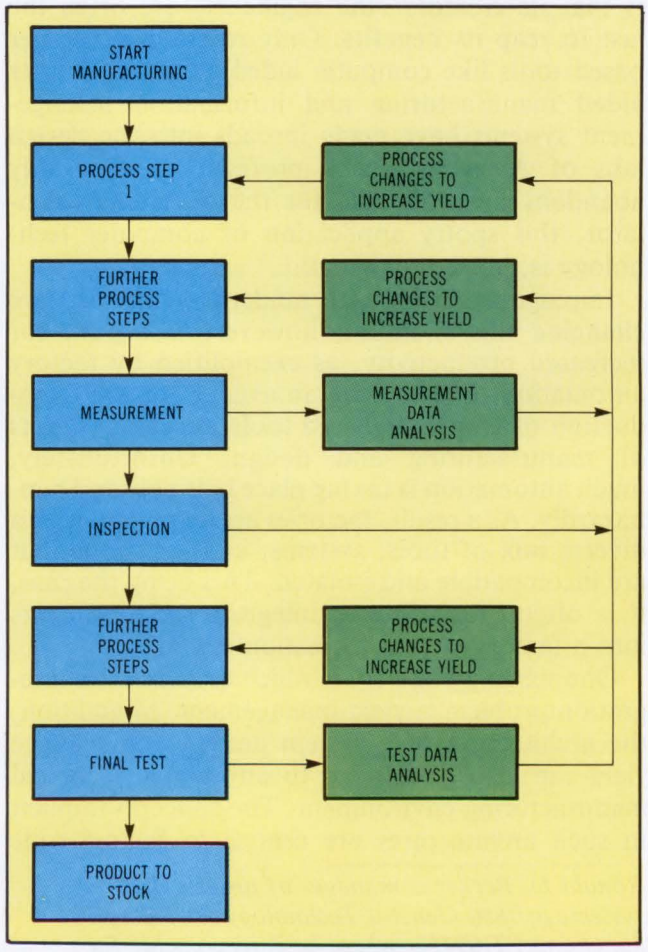

Fig 2 A manufacturing process that provides for feedback improves productivity and yield. Establishing data gathering and feedback loops enables operators to gain control of product flow and process efficiency.

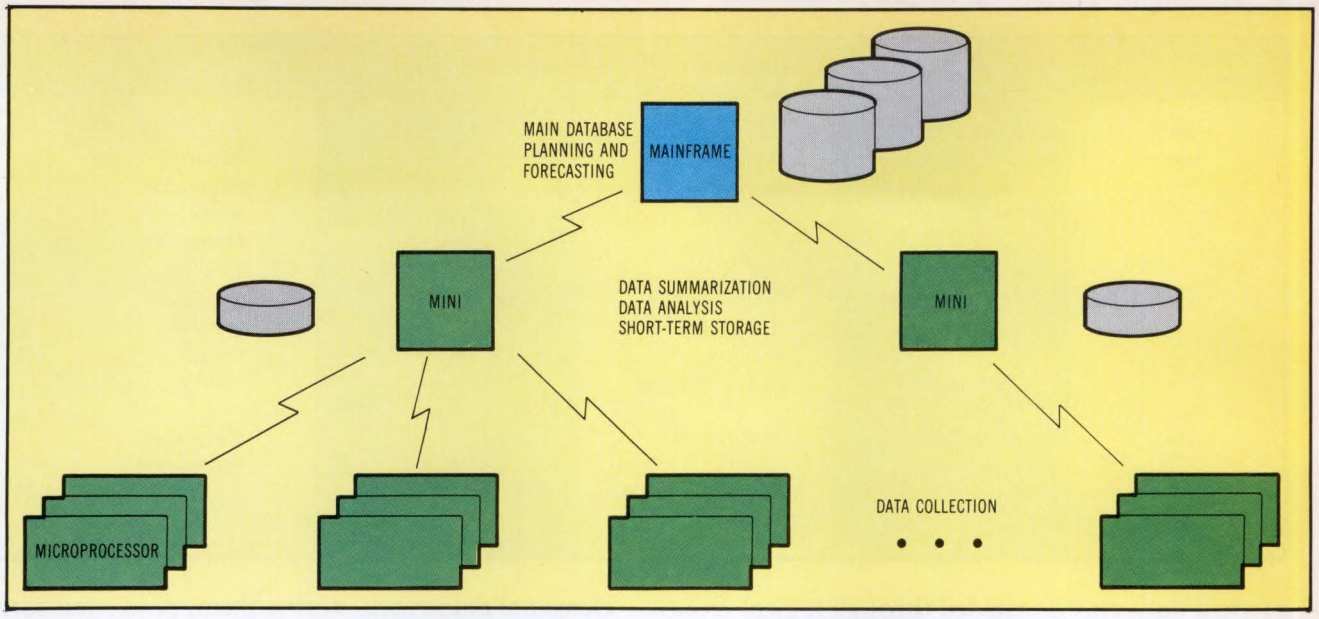

Fig 3 In a typical yield management system, the system itself represents the hierarchical nature of the tasks and data. Low level data collection leads upward to data analysis and storage. Eventually, insights gleaned from analysis of stored data aid in modeling and forecasting.

Once yield is defined, the second step in implementing a yield management system is to isolate the elements that affect factory yield. Here, many questions need to be raised. For example, what are the known yield detractors (eg, breakage, misprocessing, or loss)? Are there invisible yield detractors such as a reprocess cycle where a product may languish forever? Are there yield bonuses, such as last month's reprocessed products appearing this month as extras? What are the suspected but unconfirmed yield detractors? The entire manufacturing process, in successive layers of detail, needs to be examined to establish measurement tools and targets.

The third step provides the financial base from which to judge the affordability of the hardware and software to be installed. After examining the yield elements determined in step two, decisions need to be made on the potential productivity gains resulting from increased yields. In other words, practical yield objectives need to be set. These are not black and white decisions. Rather, they involve many facets of a manufacturing operation and require the full involvement of the engineering, systems, and financial staffs. For example, a 1% yield loss during the first few manufacturing steps may be acceptable due to the investment required to correct it. A 1% yield loss in the final manufacturing steps may be unacceptable because of the added value to the product as it nears completion. Therefore, significant investment to correct this loss may be warranted. Also, the amount of hardware and software necessary to encompass large segments of the manufacturing process, or identify major process interactions as yield detractors, may be prohibitively expensive. In this case, system implementation may be deferred. It is thus important to decide which elements should be attacked first. This decision should be predicated upon the potential productivity increase due to improved yield, and reasonable yield increase objectives.

Gathering the required tools is the final step. Tools are more than hardware, software, data analysis, and reports. In fact, one essential tool is the organizational structure itself. Manufacturing control and engineering personnel must be organized in such a way that management responsibility coincides with the defined yield elements. All personnel must understand the yield objectives defined in step three, as well as their measurements. A clear definition of objectives helps to implement a successful yield management system.

Yielding to the hierarchy

System architecture is, in actuality, a mirror of all data collected in the factory. Several characteristics of the architecture become apparent when defining the yield management process. The foremost is its hierarchical nature. Fig 3 illustrates a typical yield management system architecture.

The hierarchical nature of the data determines the product mix and the volume that is manufactured. A high level of this hierarchy may be cost objectives. Those help determine manufacturing volume and mix, and are generated by sales forecasts. Sales eventually translate into orders and manufacturing schedules, a more immediate and intermediate level of manufacturing control data. At a low hierarchical level is machine control data.

Yield data are in a similar hierarchy. At the highest level are relationships across product lines and many manufacturing steps. Intermediary levels

Yield Management System Task Assignments				
Level	Functions Provided	Data Analysis	Data Storage	Data Presentation
High	Product planning Correlate business functions to yield functions	Trend analysis Correlation analysis	Long-term statistical summaries	Reports Interactive query Interactive planning
Intermediate	Correlation across set of lower levels Monitor for known yield detractors	Status reports Correlation analysis Failure analysis	Short-term, across many elements	Statistical analysis Online inquiry
Low	Data collection Microprocessor interface	Pass/fail edit criteria Go/no-go decision criteria	None	Collection verification

of yield data may be yielded through logical groupings of manufacturing steps. Low levels may be measurements of component quality or conformance to specification.

What seems to be required, then, is a system architecture that mirrors and complements this data structure. A hierarchical architecture with levels of functions, data analysis, data presentation, and data storage allows interaction with the system that is consistent with established ways of viewing the information.

When examining system interactions, data acquisition (the lowest level of the architectural hierarchy) provides a good example.

Data acquisition at a process step level is an isolated function. It might involve a material quality measure or an inspection result. In either case, it does not require interaction with data collected at other steps. Thus, the lowest level of the architecture is characterized by limited scope of function, elementary analysis, limited data presentation, and no data storage. Luckily, these characteristics describe the distributed computer automation already in existence in the factory. This primitive level of automation can serve as the basis for building a factory-wide information management system.

An intermediate level of the hierarchy consolidates the data from the low level collection systems into the first elements of an information system. The intermediate level, which recognizes correlations among results collected from several low level segments, provides functions to manage those correlations. Initially Stapper,[2] and later Melan et al,[3] demonstrated the techniques of using correlation analysis among yield elements to feedback process corrections. For example, if the first microprocessing steps have been isolated as a yield element, the intermediate level for the architecture would be assigned the tasks of collecting the elemental data types, storing them, producing correlation analyses, and presenting information that spans several process steps.

At a high level of the architecture, functions relating business parameters to yield can be found. Issues to be resolved by these functions are what happens to yield when volume and mix change, and the rate of yield learning. These functions naturally merge the business applications of the existing data processing center into the new functions of yield management. Data stored at this level span the factory and must be kept for a long time to establish trends. The information presented here depicts yield as a function of the entire factory environment. This layer of the architecture coincides with, and enhances, existing data processing operations.

Thus, it is apparent that this layered, hierarchical architecture bridges the gap between the distributed, automated base and the centralized, data processing base from which a yield management system began. The Table, "Yield Management System Task Assignments," summarizes the functions, presentations, and storage of data in the system architecture.

Implementation issues—getting it to work

A distributed base is a starting point to implement a yield management system. Layers of function are added to this base until the existing data processing center is reached. Key technical issues need to be resolved and key business factors determined if a yield management system is going to grow into a complete implementation.

Three key technical issues arise immediately: database structures, data communications methods, and application development methods. Database strategy must revolve around implementation, maintenance, and enforcement of a factory-wide data dictionary. This requires collecting and correlating hundreds of different data elements from

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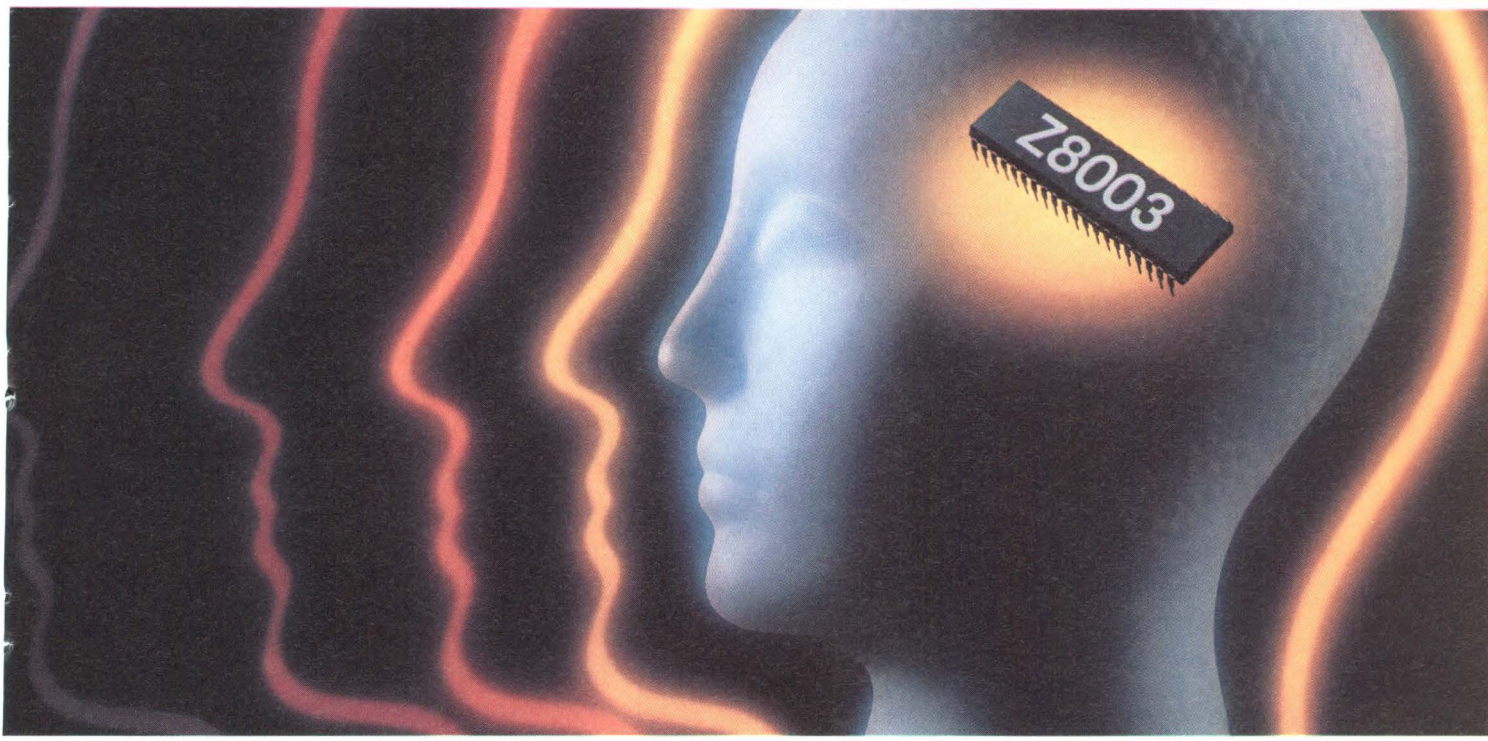

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Time and cost are key business factors in implementing yield management.

diverse areas of the factory for extended periods of time. This activity has a low likelihood of success without centralized data control. The database management system chosen must, of course, be able to work with the dictionary. Further, it must be diverse enough to handle the layered storage depicted in the architecture, from small amounts of data with few correlations to large amounts with many, complex correlations. Also, a consistent interface to the application programmer must be maintained.

Data communication methods must provide consistent communication among system layers from microprocessor to mini, to small mainframe, to large mainframe. Each layer of the architecture filters out detail and passes on a higher level of information. The lowest level of the hierarchy provides for local attachment of terminals.

Undoubtedly, layered architecture will be implemented on several different types of computers. Ideally, a language should be chosen for application development that spans micro, mini, and mainframe boundaries, and provides maximum flexibility in applying the programming resources.

As in any system implementation, time and cost are key business factors in implementing yield management. The implementation schedule and cost depend on the technical maturity of the programming and engineering staffs. Organizational maturity of the management staff, complexity of the manufacturing operation, and economics of yield productivity also play a role in system implementation.

Merging engineering measurements into the hierarchical structure, and attempting to correlate the results, requires broad-based technical experience. In addition, the management team must be flexible enough to reorganize when necessary to reflect yield element definition. They must also be mature enough to accept a new set of objectives and measurements as well as a new organizational hierarchy if that is deemed necessary. The intransience of the human element should not be underestimated.

Moreover, manufacturing complexity will slow the implementation process. More products, manufacturing steps, and complex flows result in additional data collection points and correlation among yield elements. Consequently, more time is required to understand the relationships and provide data collection hardware.

The growth path from the distributed-centralized starting point to a mature yield management system is evolutionary. From isolated yield elements, consolidation occurs in one section of the next higher layer of the architecture. Implementation proceeds apace with technical and organizational learning. The rate and extent of implementation depend on the economics involved. In general, yield-increase targets generate higher productivity. Picking the right targets and the correct elemental yield points that should be initially attacked is a combined business and technical decision.

As experience and technical maturity are gained, more extensive parts of the architecture can be implemented. Accelerated investment in such a system may be based on a commitment to climb a yield learning curve more quickly. An important business factor to consider is that the first steps in establishing both the architecture and the viability of the concept are relatively inexpensive. Using the existing factory automation base, and adding a small hardware and software investment to it, creates a new way to manage the information generated.

Due to the inexpensive microprocessor, it is economically feasible to use computer resources to help manage yield in the automated factory. The described architecture for a yield management system is a generalization of the system that is boosting factory productivity at the IBM semiconductor plant in Essex Junction, Vermont. Its hierarchical nature mirrors the data required to manage yield, and its implementation evolved from a distributed automation and centralized data processing base.

The time and money invested in a yield management system must be entirely consistent with demonstrable productivity gains. With a mature yield management computer system, however, yield becomes a more manageable element of factory productivity.

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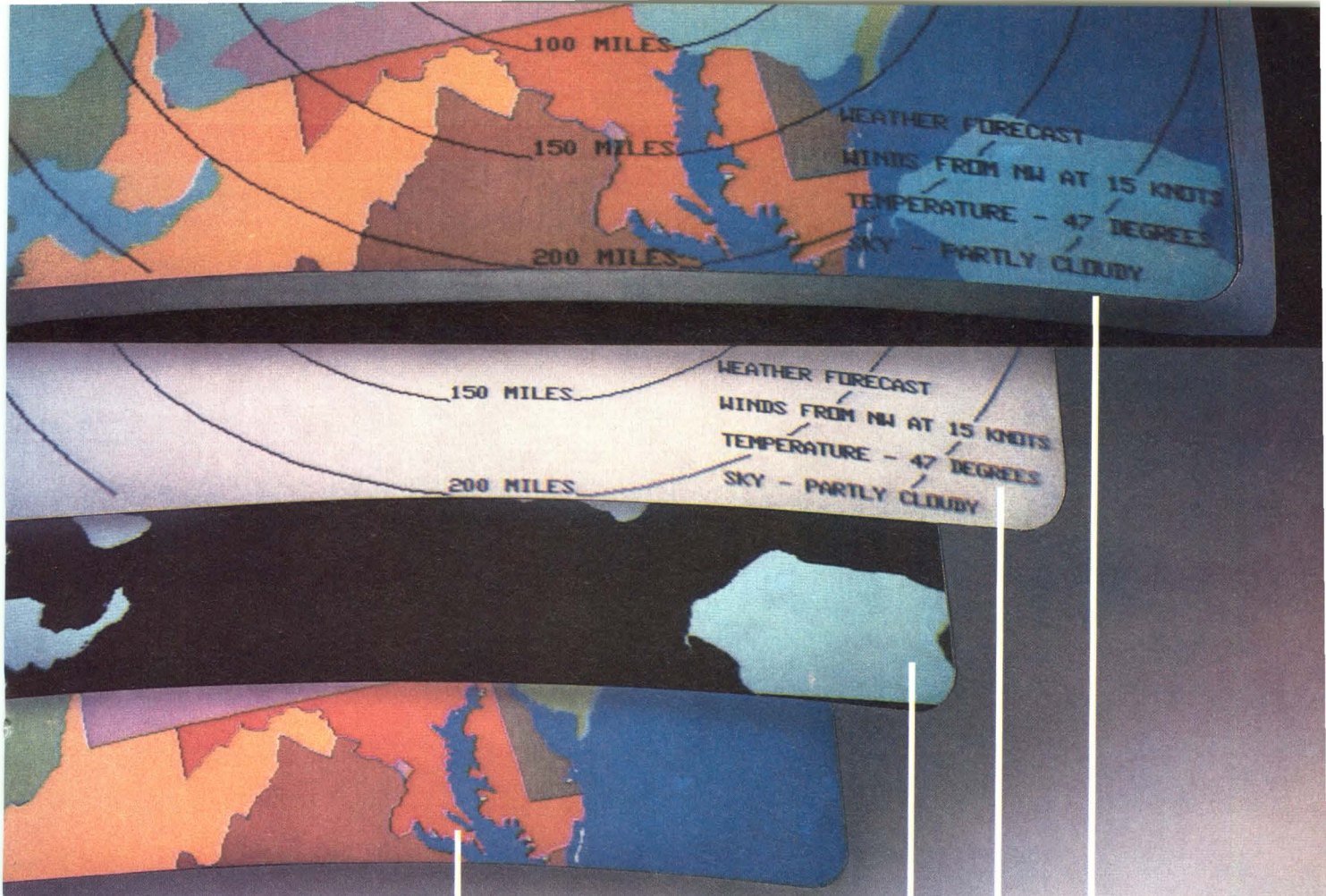

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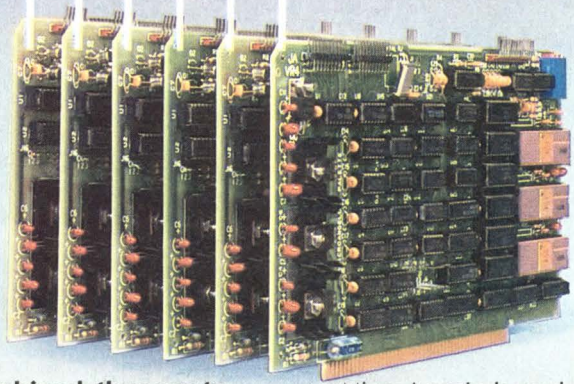

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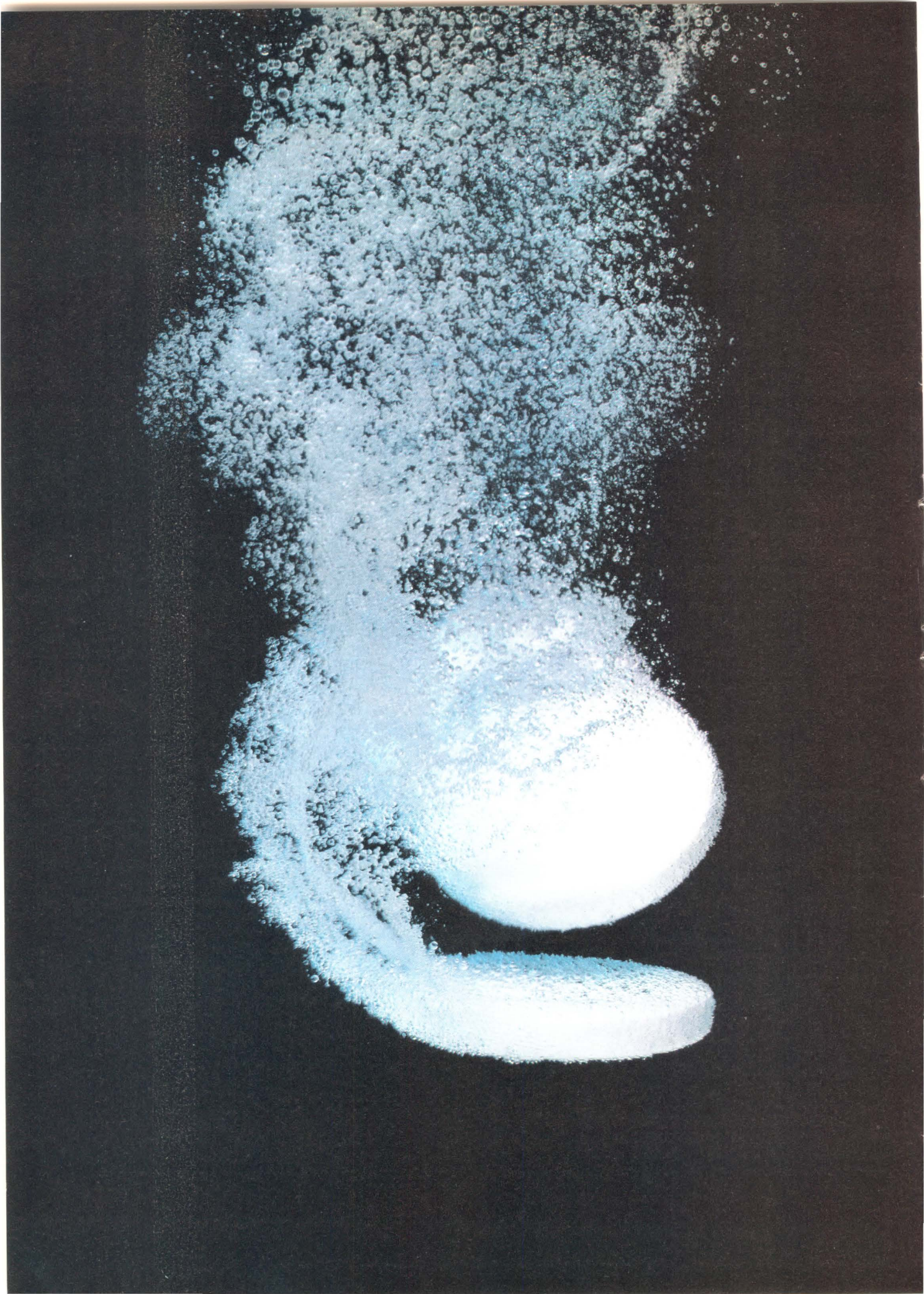

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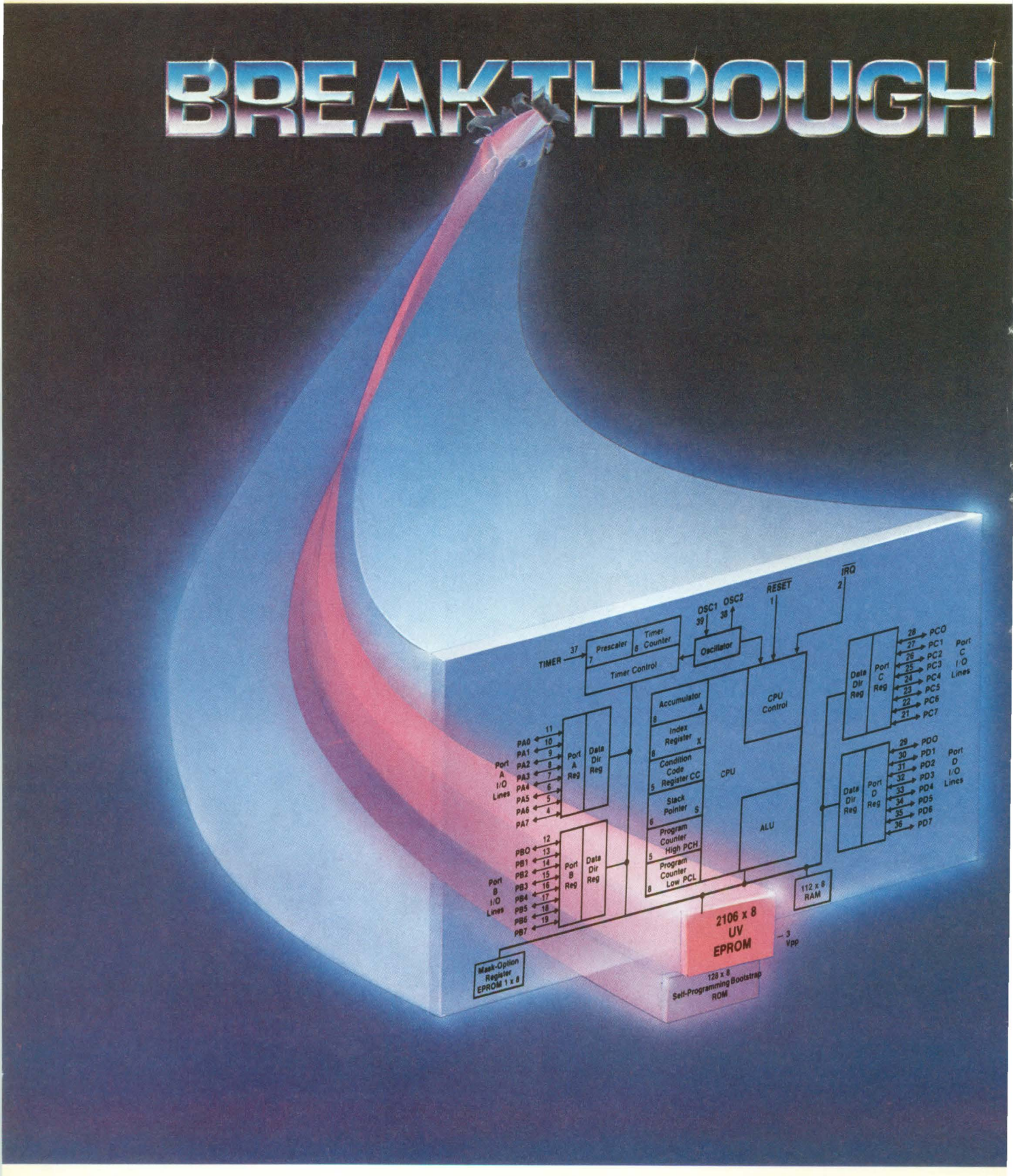

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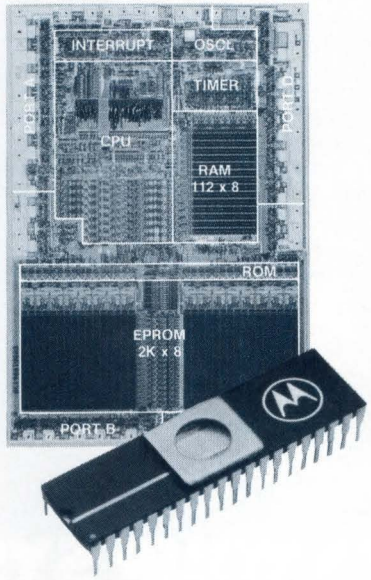

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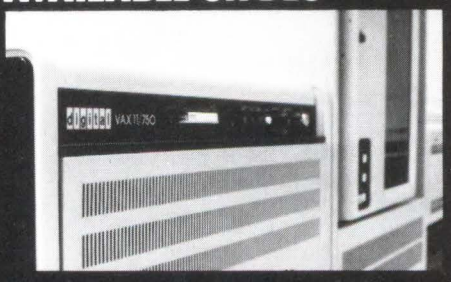

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by Robert C. Sanford

Microprocessors have come a long way in just 10 years, and predictably, many features and functions have been added to them during that time. The most recent entries sport features designed specifically for multiprocessing and memory management. Yet, most microprocessors have followed the architectural precedents laid down by the 8008. As a result, today's processors suffer from several serious limitations.

First, the microprocessor units (MPUs) are Von Neumann structures centered around memory. The central element, however, should be the arithmetic logic unit (ALU), since it alone permits computation. Second, buses are multiplexed both internally and externally for direction and sometimes functions such as address and data. The chief reason for external multiplexing is that MPUs are pin limited; this is because MPU manufacturers will not use larger packages. Third, because data are handled in ASCII, all MPUs are based on a *de facto* 8-bit byte. (An 8-bit byte allows only 256 different instructions of all types, but even 16-bit MPUs do not offer enough different instructions.) In addition, most

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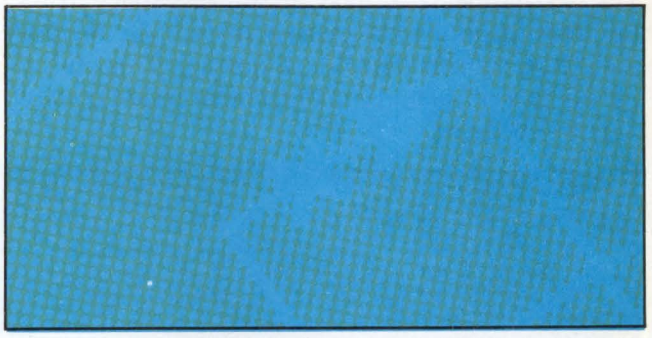

MPUs use a general register bank instead of dedicated registers. These banks are often random access memories (RAMs) because regular, orthogonal layouts use less silicon.

Consider the following as well: basic address space, 16K, requires 2 bytes (1 word for a 16-bit MPU) for addressing. Expansion or segmentation requires at least 1 more byte. Newer MPUs with more complex instructions require more than 1 byte for some instructions, plus an address. This complicates programming and, as a result, some desirable or useful functions are unavailable. Finally, more emphasis is placed on how much read only memory (ROM), RAM, and input/output (I/O) are squeezed onto a chip than on what functions are available.

Perfectly viable computers have been produced using 4, 8, 12, 16, 18, 19, 21, 24, 32, 48, 56, and 64 bits as a word length. Before ASCII, most word lengths were multiples of 6 bits because most data were in IBM 6-bit code. Now, MPUs are based on multiples of 8 bits. This need not be the case, however. Nontraditional designs have many advantages.

Breaking with tradition

A first break with tradition is choosing a 12-bit byte. This design uses only 48 pins of a 64-pin package. The 12-bit byte is ideal for the popular 12-bit digital to analog and analog to digital converters. Twelve bits also allow up to 4K different instructions. In such a scheme, 4K of memory can be directly accessed.

By treating this 4K of basic memory as a page, all MPU memory reference instructions can work over it with just 1 address byte. As shown in Fig 1, the first bit in each instruction determines whether an address uses 1 byte (direct) or 2 bytes (extended) addressing. A 1-byte direct address provides a full 4K MPU. To gain direct access to 16M bytes, change that 1 bit in any memory reference instruction and use 2 address bytes.

For direct addressing, the most significant address byte goes out as all zeros. Two-byte addresses are used when the bit is set for extended addressing. Using special instructions PGE (page) and NPG (no page) permits the use of only 1 address byte. PGE locks up the most significant byte so that any following instructions require only 1 address byte. The MPU appears to have an address space of 4K, but that page can be placed in any 4K memory area. NPG returns the MPU to normal. This places a useful part of memory management inside the MPU where it belongs.

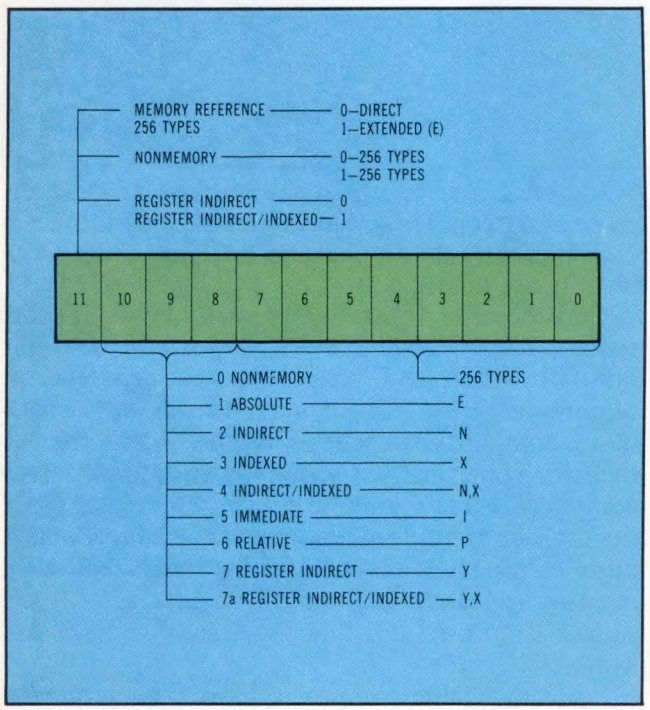

Fig 1 Architecture supporting 12-bit words greatly facilitates instruction and addressing operations. By flagging specific word bits with addressing parameters, single- and double-word, and direct and indirect addressing modes can be supported. A 12-bit format provides 4000 instructions and addresses up to 16M bytes.

The next 3 bits offer eight choices, six of which are addressing modes for memory reference instructions. The other two choices provide register indirect addressing and nonmemory instructions. The remaining 8 bits offer 256 different instruction types. In addition to direct or extended memory addressing, that first bit allows two types of register indirect addressing and doubles the 256 nonmemory types. In total, there are 512 nonmemory, 512 register indirect, 1536 direct address, and another 1536 extended address instructions possible.

Complementary metal oxide semiconductor (CMOS) memories, both RAM and erasable programmable read only memory in N x 1 and N x 4 configurations, are ideal for 12-bit schemes. These structures keep the data inputs and outputs separate. Beyond 4 bits wide, memories multiplex inputs and outputs. Even though there are many byte-wide (8-bit) CMOS memories available, some studies of future memory use indicate that the two traditional structures will find continued use in large memories.

A second break with tradition is prohibiting both internal and external bus multiplexing (Fig 2). This means there are no 2-way buses and no sharing of data and addresses on MPU pins. Since a bus can only pass information in one direction at a time, multiplexing for direction or function only slows down an MPU. Data enter from the outside on one data bus to either memory register M or instruction register I and exit to the outside on a separate data bus that features 3-state drivers. The 24-bit address bus, which also has 3-state drivers, is not shared with data.

The MPU's row of registers has an input side and an output side. A single letter identifies each register as required by the assembly mnemonic code. At the left is register M, which accepts memory output whenever it is not functioning as an instruction byte. At the top of Fig 2, there are two buses feeding the ALU at the far right. Note that all paths funnel through the ALU since it is the one element that lets the MPU compute. Data on one bus can only be added or passed through by the ALU. On the other bus, data can be added, subtracted, passed, or inverted (complemented). Logic functions AND, OR, and XOR use both buses while other instructions use one or both buses.

When Xs are located near buses and register inputs, they represent CMOS transmission gates. All the gates feeding a particular bus form a multiplexer. This, however, does not add multiplexing to the MPU because data are only going one way. In CMOS, such a multiplexer is conventionally made from transmission gates instead of logic gates. This is done because the transmission gates are simpler to work with, much faster, and can also be used for analog signals.

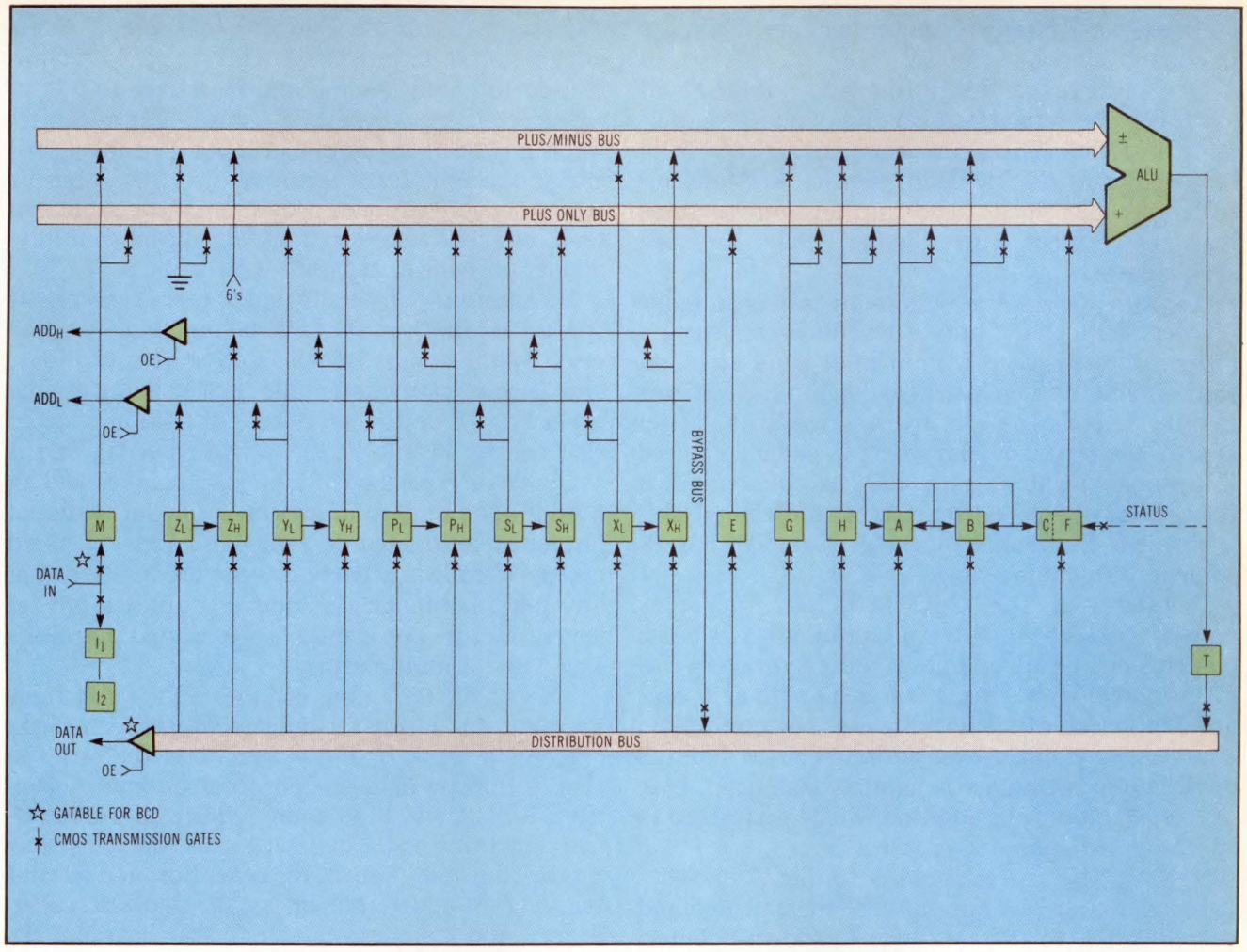

Fig 2 In the proposed 12-bit architecture, bus multiplexing is avoided in order to improve performance. All data paths funnel through the ALU via two special function buses. A high performance ALU is essential in such a scheme.

An architecture rich in registers

In the 12-bit MPU, data from any register must pass through the ALU; that is why a high speed ALU is so important. Every instruction causes a transfer from one or two registers through the ALU to some other register, which can be one of the two sources. The bypass bus in Fig 2 is only used during some swaps and for some addresses in special instructions.

Register M holds memory outputs and feeds both sides of the ALU so that the ALU sees memory as just another register. An instruction can use M as easily as any other register. Arithmetic or logic functions called out by the instruction can occur on a transfer to or from memory just as easily as between registers. This fosters many new types of instructions.

Remember that in a mainframe, mini, or MPU computer, a register is a place to store data or an address. If it is expected to count—to be incremented or decremented—the register's contents must be passed through an ALU or separate incrementer/decrementer and then back to the register. This ties up other hardware and takes time. The 12-bit MPU uses true hardware counters. They can count faster, and count while the ALU is doing other things. Register E is a down counter while P, S, X, Y, and Z are all 2-byte up/down counters because they deal with addresses.

If data in a conventional computer are to be shifted right or left they must go from a register, through some shifting device, and back to the register. In MPUs, the shifter has usually been a set of gates to shift left 1 bit, pass through data unchanged, or shift right 1 bit, sometimes as part of the ALU. Another scheme uses a hardware shift register somewhere in the data path. This register can provide multibyte shifts.

Accumulators A and B can be used separately or together as double-width accumulator D. Since shifting is an accumulator function, A and B are true hardware shift registers. Data can be shifted in the register while the ALU is occupied. Rotate and shift instructions can control A alone (short shifts) or both registers as D (long shifts).

The memory register, program counter, and accumulators are designated M, P, A, and B. Transparent register T stores temporary results from the ALU and is unavailable to the programmer. It is

useful during outputs to slower memory. Flags are in condition code register F.

Free registers G and H, forming part of the 12-bit MPU, provide scratchpad capability and programming flexibility. These can be used either separately or together as double-width register K. Many instructions manipulate data into and out of these registers. Except for shifting, they are full accumulators.

Another powerful programming tool is an index register. With traditional or true index registers, a direct address is read from memory and an offset value stored in the register is added to the contents in order to create an effective address. If the offset is zero, the program goes where the address stored in memory dictates. With some exceptions, MPUs depend heavily on register indirect addressing. This is inverted traditional indexing. Not many MPUs offer traditional indexing.

Register X in the 12-bit MPU is a true index register. It feeds the ALU plus/minus bus so that its contents can be added to any address register or to memory register M. Register X deals with addresses and reaches all of memory. It is a 2-byte up/down counter. Any single byte address can be indexed anywhere in memory. If the most significant byte of X is zero, only one addition will be performed to speed up throughput.

Register S is the stack pointer for the 12-bit MPU. It handles addresses and must be incremented and decremented, so it is a 2-byte up/down counter. Various instructions allow S to be used for program purposes.

Address pointers are also extremely useful. Providing traditional indirect addressing—not register indirect—allows any memory location to be used as a pointer. Register Z is used to hold indirect addresses. In addition, address register Y is used for register indirect addressing. Address register Y is another 2-byte up/down counter.

Register Y can also move data memory to memory. In this case, Z holds the destination address and Y holds the source address. Since both are counters, clocking them lets the programmer go through a block of addresses. A simple protocol when using instruction MFM (memory from memory) allows single or block transfers. Since Y can be manipulated with several instructions, it can be an indirect addressing register for programmers who prefer that mode.

Counter E keeps track of how many blocks of data are transferred. Since blocks can be up to 4K bytes long, an entire page can be transferred. Counter E is also a true down counter. It can be directly loaded with a number instead of requiring a complement. The letter E does not stand for anything in particular but can be considered as enter count. If E's contents are zero, instruction CNT (count) loads the following byte into E. If it is not zero, CNT decrements E. This single instruction is used for both loading and counting. A flag in register F is set whenever E is not zero and reset when E is zero. A jump instruction permits a program to sample for a zero count so that E can be used as a conventional programmable counter up to 4K bits. It is also used internally during multiply, divide, normalize, and shift instructions.

Flag register F differs from the other registers. It consists of flipflops that can be individually set or reset by the results of ALU and shift operations, and various instructions. Bits C, S, V, and Z are the usual flags found in MPUs in a condition code or flag register (Table 1). Bit F is a true flag and is available on a package pin as both an input and an output. The only requirement is that the external line must be treated as a bus and kept tri-stated except when it is actively driven. It can be read at any time. Although this does multiplex a pin, at least two more pins would be needed to control the flag without multiplexing.

This 12-bit MPU now includes all the functions necessary for a truly versatile microprocessor. Data registers A, B, G, H, and M feed both ALU buses so that arithmetic or logic can occur on any instruction. Registers E, F, P, and S require only straight-through transfers. They feed only the plus only bus. Meanwhile, X feeds the other bus, and its contents can be added to memory and addresses. Registers T and Z are unavailable to the programmer.

Another register the programmer cannot use is instruction register I. It accepts memory outputs during instruction fetches and consists of two levels of transparent registers that create a 2-stage fetch pipeline. An instruction from memory falls through immediately to I_2 where it feeds the decoding and control hardware. If the decoded

TABLE 1

Bits in Flag Register

Bit	Assignment
F	Flag flipflop (available on a pin)
C	Carry bit
S	Sign bit
V	Overflow (signed arithmetic)
Z	Zero
E	Counter E contains a count
B	BCD mode
I	Interrupt enable
H_1	Half-carry (low-order decade)
H_2	Half-carry (middle decade)
P	Page mode
A	ASCII pack mode

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instruction does not require a memory access, the MPU fetches the next instruction, which stops in I_1 until the present instruction is completed.

On the ALU input buses (Fig 2), either or both buses can be fed from ground during certain instructions, as in other MPUs. An input to the plus/minus bus is marked "6's." When adding or subtracting packed binary coded decimal (BCD) numbers with a binary adder, some answers will be wrong. Most MPUs have a decimal correction instruction that adds six units to each BCD decade (10 units) where a carry-out occurs. This carry-out is usually called H and appears as a half-carry flag in the condition code or flag register. Since the 12-bit byte holds three BCD decades, two flags are available, designated H_1 and H_2. Feeding the 6's to the plus/minus bus makes it easy to correct for subtraction as well as addition.

Dealing with BCD

A large amount of data moving to and from memory is in BCD but buried within ASCII characters. Whether an MPU uses an 8- or a 12-bit byte, only the 4 least significant bits (LSBs) are of interest for BCD. A byte must be brought in, masked, and packed before BCD arithmetic can be performed. Special added instructions RRH (right rotate Hex) and LRH (left rotate Hex) rotate accumulator A 4 bits at a time to aid in packing and unpacking BCD decades, but do not change the need for masking.

In Fig 2, the star alongside the input to M and another above the data output drivers represent a special function that instruction BCD enables and BIN (binary) disables. When BCD is active, all but the 4 LSBs of data memory or I/O are gated to prevent any data from getting to M. The inputs to M are clamped to zero. ASCII BCD characters are masked on the way in.

By using instruction AOM (A ORed with memory), the BCD decade in M is ORed with A on the way into A. An RRH instruction then rotates the decade to the 4 most significant bits (MSBs) of A. Packing three BCD decades is thus much faster than the conventional MPU way.

The other star above the data output drivers indicates that during BCD conditions all but the 4 LSBs are gated and the driver output is a true ASCII character. A binary three (0011) is gated out of the middle decade to form the ASCII character and the 4 MSBs are gated out as zeros. Unpacking reverses the packing scheme by using MFA (memory from A), and by LRH rotating the decades the opposite way. Instead of the usual masking and merging steps required by most MPUs, this method translates ASCII to packed BCD and back again to ASCII with I/O gates and versatile instructions.

Bit F can also be controlled with the program. It can be set and reset directly. Jump instructions allow sampling for program decisions. In addition, bit F is the MSB of register F. If the contents of register F are transferred to A, the bit F appears in A in the sign-bit position and can be manipulated by all the instructions dealing with the sign. This flag is intended for control of or by external hardware. It can be used to provide a serial I/O capability.

Flag bit E indicates the contents of counter E. It is set whenever E contains a count and reset when E is zero. Jump instructions allow bit sampling to use counter E as a conventional counter. Bit B simply indicates that the MPU is in the BCD mode. It is set by BCD and reset by BIN.

When bit I is set, all interrupts are accepted. When it is reset, NMI is still accepted but IRQ and INT are disabled. Bits H_1 and H_2 are decade carry-outs from the ALU and are used internally for decimal correction.

Bit P indicates the page mode. When P is set, the most significant byte of an address is locked to its present value, and all extended 2-byte addresses are held to one 4K address space determined by the locked upper byte. Here, E is programmed for extended addressing. One address byte is used. If the lowest 4K space (zero page) is desired, program for direct and again use 1 address byte. This permits the programmer to move between the zero page and any other page. Full control without paging is retained using normal direct and extended addressing.

Bit A (for ASCII) is set by instructions PCK (pack), UPK (unpack), and reset by NPK (no pack). To overcome the inefficiency of a 12-bit byte for ASCII characters, PCK and two start addresses (they can be on different pages) are programmed to set up a memory to memory transfer with special conditions. Three ASCII inputs are packed into 2 bytes inside the MPU and stored in memory as 2 bytes instead of 3. Either address can, of course, be an I/O function. Programming UPK and 2 addresses does the opposite; each of 2 inputs is unpacked and stored in memory as 3 ASCII bytes. Instruction NPK returns the MPU to normal from either mode. Programs containing long strings of ASCII characters to be stored or unloaded can use this pack mode macro.

Providing lines for adequate control

Table 2 shows the control functions in a 64-pin package. As in all modern MPUs, two leads are provided for a crystal to control an internal oscillator. One of these lines can also be used as an input for an external clock. This signal is divided down sufficiently to provide all the internal MPU timing signals.

Reset involves clearing registers E, F, and P. Register E is cleared to get a zero count to agree with its flag bit in register F. Clearing F allows the MPU to escape from all special conditions and to inhibit interrupts. Register P is cleared so that it contains address zero, which is the usual restart vector where the starting address of a program is placed.

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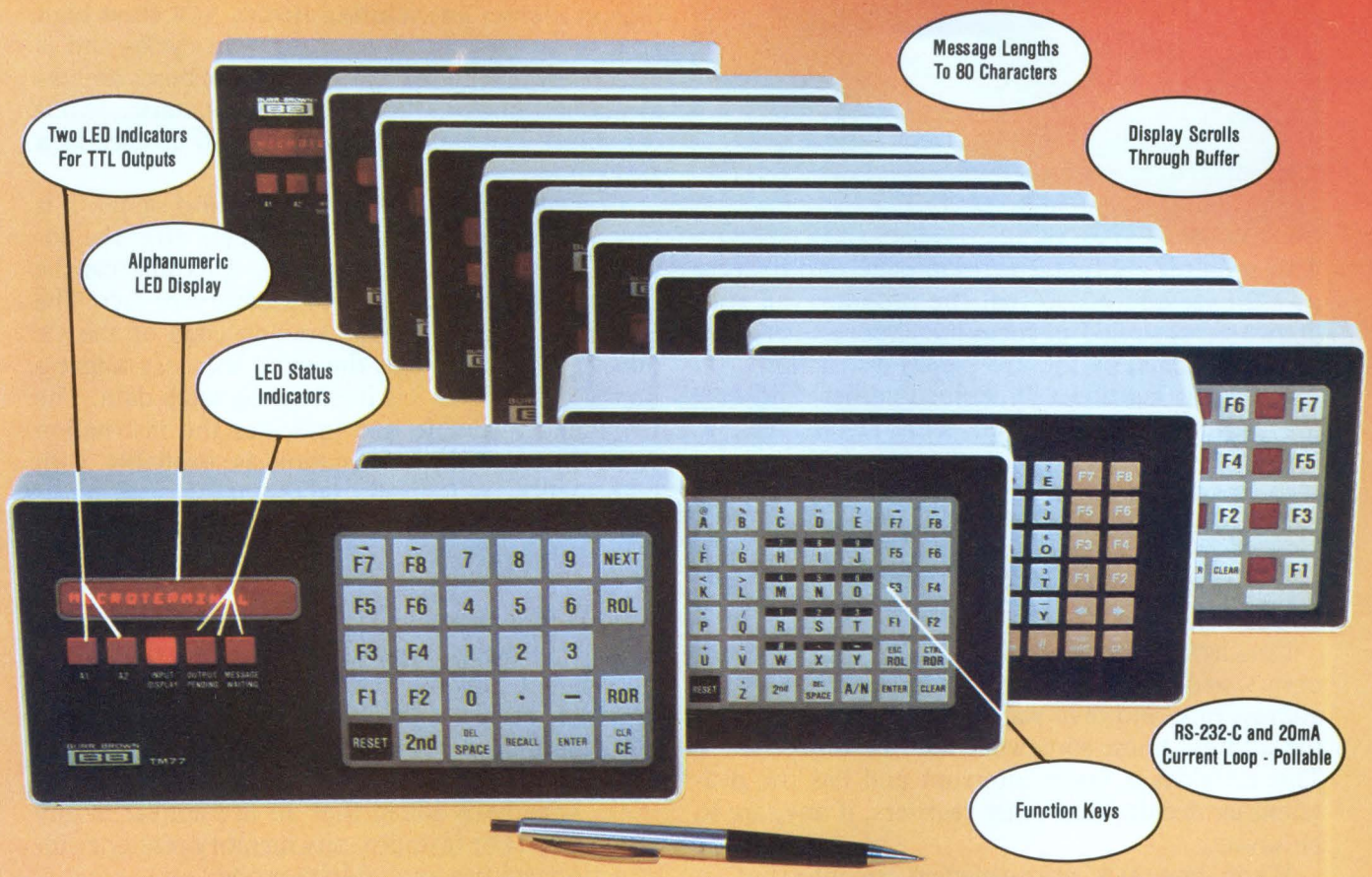

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TABLE 2

Buses and Control Lines

Data bus in (12 lines)	F (external flag line)
Data bus out (12 lines)	NMI (nonmaskable interrupt)
Address bus out (24 lines)	IRQ (6800-type interrupt)
V_{DD}	INT (addressable interrupt)
Ground	ACK (acknowledge)
X-in (crystal or clock in)	DMA (bus request)
X-out (crystal)	HOLD (adds wait cycles)
CL (clock out)	ENA (enable address latches)
RESET (clear E, F, P)	FETCH (fetch cycle)
R/$\overline{W}$ (data bus direction)	

This requires the first 2 bytes in page zero to serve as a 2-byte address so that the program can start anywhere specified in memory. Address zero can also be reached by the RES (reset) instruction.

External flag line F (described earlier) and R/$\overline{W}$ are used for data direction. This 12-bit MPU has three interrupt lines. NMI and IRQ are 6800-type interrupts that automatically save all registers (15 bytes) before acknowledging the interrupt and vectoring to the interrupt routines. The only difference is that NMI cannot be inhibited by flag bit I as IRQ can; they also use different vectors.

Line INT is a different type of interrupt. It stores only F and P before acknowledging, tri-states the address bus, and then waits for a 24-bit address on the address lines, somewhat like the 8080 scheme. This provides a faster interrupt and lets the programmer decide what other registers, if any, are to be saved.

When line ACK acknowledges an interrupt, it goes high during the first instruction fetch after automatically saving registers. If the interrupt is INT, ACK can be used to gate a 24-bit address onto the address bus, and point to the start of the interrupt program. This same line acknowledges direct memory access (DMA) and hold inputs. During a DMA request, ACK remains high as long as the buses are tri-stated for external signals, and acts as a BA (bus available) line. During HOLD, ACK stays high as long as the MPU is inserting wait cycles and is effectively in a halted state. Thus, the buses are unavailable. Since CMOS is completely static, HOLD can insert wait cycles indefinitely and be used as a HALT line.

The line marked ENA carries a hybrid signal. It is timed so that the leading edge occurs after the address lines have been stabilized. This line can be used to latch addresses into memory or I/O. The trailing edge matches the trailing edge of the CL (clock) line much like the valid memory address line of a 6800. This lets it externally latch data. The remaining available line indicates the instruction fetch cycle. This information is available with many MPUs. It is useful in timing external hardware such as memory management circuitry and code disassemblers.

What is in a mnemonic?

In general, the mnemonic code follows some simple rules based on this hardware concept and allows hundreds of instructions in a fairly regular set. The most common abbreviations are used for the exceptions. Some functions and programming tricks have been added that do not appear in any other MPU. For instance, any memory reference instruction can use any address mode.

Each instruction mnemonic consists of three letters. Table 3 defines each letter. Each register is

TABLE 3

Mnemonics Instruction Letter Assignments

First Letter		Middle Letter		Last Letter	
A	Main accumulator	A	AND (logical)/ Arithmetic shift	A	Main accumulator
B	Aux accumulator	C	Complement (2's)/Carry flag	B	Aux accumulator
C	Carry flag	E	Counter E flag	C	Carry flag
D	Double accumulator	F	From/Flag flipflop	D	Double accumulator
E	Counter E flag	G	Goes	F	Flag register
F	Flag register	I	Inverted from	G	Free register
G	Free register	L	Less (minus)/ Logical shift	H	Free register/Hex (rotate 4 bits)
H	Free register	N	(When) not	K	Double free register
J	Jump	O	OR (logical)	M	Memory
K	Double free register	P	Plus	P	Program counter
L	Left shift (rotate)	R	Rotate	S	Stack pointer/ Sign flag
M	Memory	S	Swapped with/ Sign flag	U	Unity (value of one)
P	Program counter	V	Overflow flag	X	Index register
R	Right shift (rotate)	W	When	Y	Indirect register
S	Stack pointer/ Sign flag	X	Exclusive-OR (logical)	Z	Zero
V	Overflow flag				
X	Index register				
Y	Indirect register				

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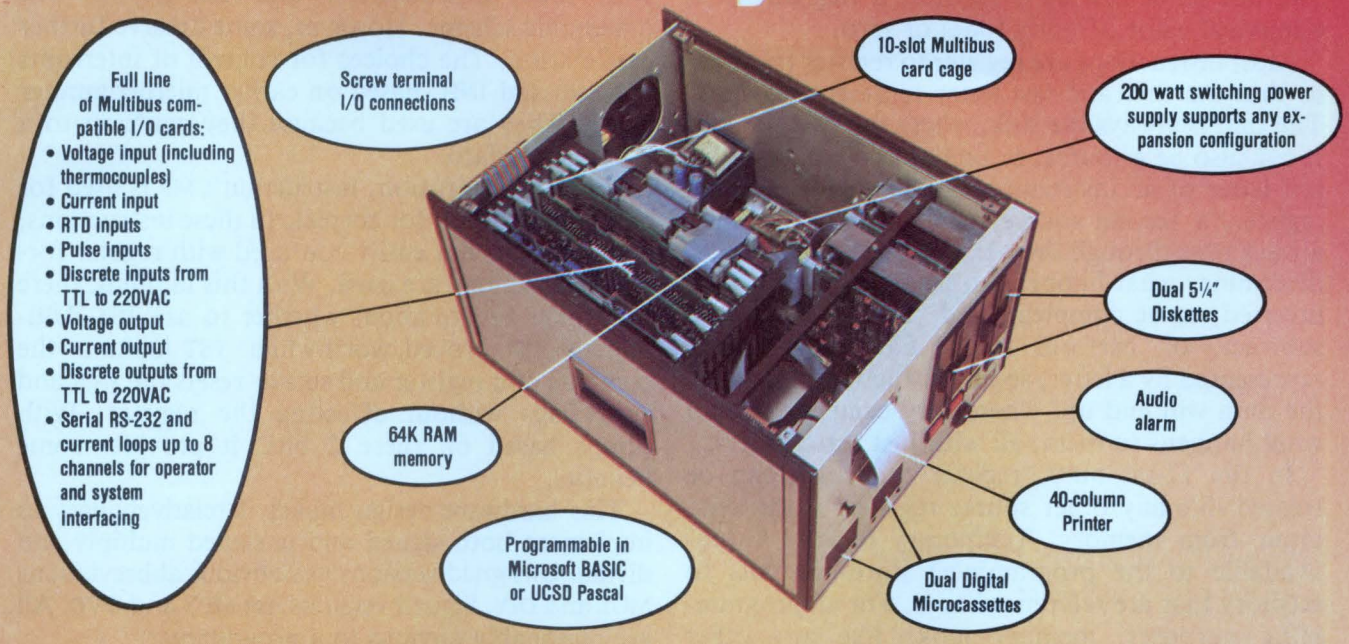

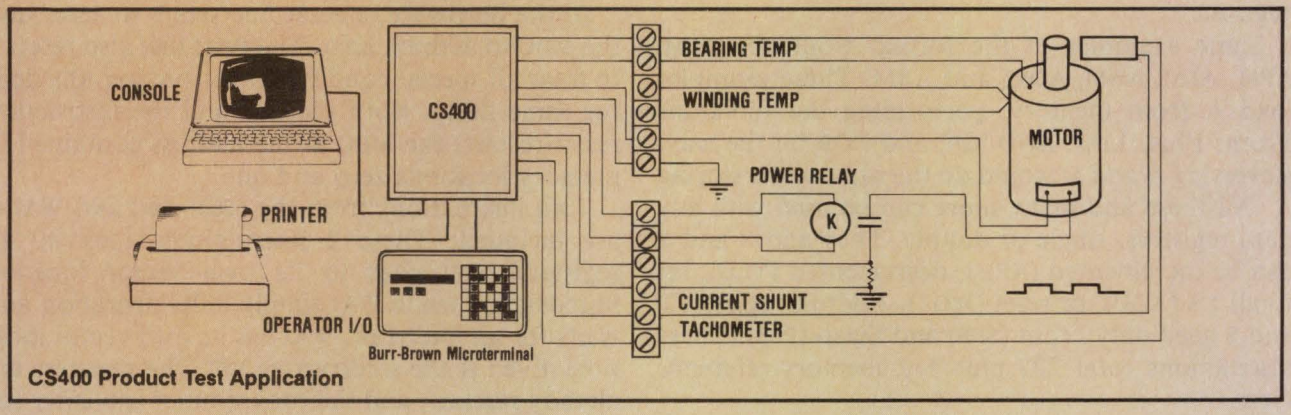

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CIRCLE 64

identified by a single letter. The first letter in an instruction can stand for a register, a shift direction, a flag bit, or a jump. The middle letter can be an ALU function, a type of shift, or a jump condition. The last letter can be a register, a flag bit, or a numerical value of unity (one) or zero.

Most instructions are register to register transfers so that the first and last letter represent registers. The first is always the sink, where the data end up. It can also be a source, or one of two sources. The last letter of an instruction can either be the same register, a second source, or a value. Data must always pass through the ALU, and the middle letter determines what happens to it. Data can pass, be inverted, or be complemented. The ALU can add, subtract, or perform logic. Each function is represented by a letter, so an instruction tells where the data will end up, where they came from, and what happens to them, all with just three letters.

In the 12-bit MPU, register M, which can be treated like any other source register, stores data input from memory. Temporary register T (unavailable to the programmer) stores outputs to memory that are referenced as M. For all programming purposes, memory looks like any other register.

Some examples of the format would be AFM, APM, ALM, AAM, AOM, and AXM. These examples load A from memory, performing the functions From, Plus, Less, AND, OR, and XOR on the way. Reversing A and M would do the same while storing A. All these and many more can be used with any data registers, single or double. They and X and Y can be incremented (XPU), decremented (YLU), set to all 1's (AGU), or reset (MGZ). Address registers P and S need only From (SFP) and Swap (PSS). These instructions total 202 plus 112 memory-reference types.

The mnemonic code is set up similarly for other types of instructions. Hardware shift registers shift directly in A or D. The first letter of a shift instruction tells which way to shift—left or right. The middle letter tells what kind of shift—arithmetic, logic, or rotate. The last letter tells the size of the shift—either A alone or A and B together as accumulator D. There are 12 shift instructions.

The term jump is used instead of branch because, unlike most MPU branches, none of the jumps are restricted in either addressing mode or memory location. In the mnemonic code, an instruction is a jump if the first letter is a J. The middle letter defines the flag bit or jump condition, and the last letter tells whether the bit is set or reset. Since jumps are dependent on the state of the flag bits, instructions are needed to manipulate those bits. Flag bit E can be reset; this clears both the flag and counter E that it represents. It is possible to set or reset external flag bit F and also set and reset overflow bit V. The primary concerns are carry-bit C and sign-bit S. These can be set, reset, inverted, transferred, and swapped. There are 12 conditional jumps and 16 bit manipulation instructions.

Table 4 contains all special instructions, along with their explanations, that do not fit the mnemonic scheme. However, some deserve further explanation. The choices for control of interrupts are ENB and INH, based on earlier microcomputer usage. They are used because they conform to a 3-letter standard.

To avoid confusion, instruction CMP is used for compare and COR for correct. In these instructions, abbreviations not easily confused with regular format instructions are used. With this in mind, there was some debate about whether to use TST. Ultimately, TST proved worthwhile. TST looks at the contents of a register and sets or resets the sign and zero flags without affecting the register. With jumps based on these 2 bits, it provides some benefits.

This hardware design makes it relatively easy to implement both signed and unsigned multiply and divide. Unsigned versions use obvious abbreviations MUL and DIV. Signed versions use MPY and DVD. All are reasonably obvious to a programmer.

In the hardware, a reset line sets P to zero, and the MPU to address zero. The reset line also resets F to clear all special conditions. Instruction RES does the same thing. Both the line and the instruction reset (restart) the MPU at the address contained in memory locations zero and one.

Two instructions from the 6800—SWI and WAI—are included. These 2 instructions stack all 15 registers. SWI goes to its own vector location immediately while WAI simply halts operation and waits for an interrupt. WAI has its own vector location. Even if the interrupt is INT, the registers are already stacked, and the programmer can enter the interrupt program immediately, without worrying about saving registers. Return from any type of interrupt is RTI.

There might be some unfamiliar instructions in Table 4 (eg, CNT, which was explained earlier). In general, floating point instructions are not suitable for this MPU, but some users may want floating point capabilities. To make that easier, instructions NMZ and NRM are included. Instruction NMZ causes accumulator A or D, whichever is selected, to shift left until the sign bit differs from its right-hand neighbor and then to stop. The accumulator holds the normalized number and sign while counter E holds the exponent, or number of shifts. Instruction NRM reverses this action, shifting right until counter E holds zero and extending the sign. Writing a floating point routine should be quite simple.

Input from memory or I/O goes to register M. On the way, some gates are put on the upper 8 bits. These bits are used by instructions BCD and PCK.

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TABLE 4

Special Instructions for 12-bit Processor

Mnemonics	Definition
BCD	Memory input accepts only lowest 4 bits; outputs BCD or Hex in true ASCII format
BIN	Binary mode; returns to normal from BCD mode
CMP r	Compare register; subtracts register from accumulator A but does not change A
CNT	Count; if flag bit E is set, decrements counter E; if flag bit E is reset, inserts following byte as contents of counter E
COR r	Correct register; uses flag bits H_1 and H_2 for decimal correction of packed BCD
DIV	Unsigned 24-/12-bit division
DVD	Signed 24-/12-bit division
ENB	Enable interrupt; sets flag bit I
HLT	Halt MPU operation; waits for interrupt or reset
INH	Inhibit interrupt; resets flag bit I
JMP	Unconditional jump to effective address
JSR	Jump to subroutine at effective address
LRH	Left rotate Hex
MPY	Signed 12- by 12-bit multiply
MUL	Unsigned 12- by 12-bit multiply
NMZ r	Normalize register A or D; shifts left until sign differs from next bit; counter E holds exponent
NOP	No operation; increments program counter
NPG	No page; returns to normal from page mode
NPK	No pack; returns to normal from pack mode
NRM r	Normal; reverses normalize procedure
PCK	Pack mode; masks inputs and packs 3 ASCII characters into register D, then outputs 2 packed bytes
PGE	Page; locks upper byte of program counter P and address register Z so that extended addresses require only 1 byte
PSH r	Push register onto stack; advances stack pointer S
POP r	Pop top of stack to register; decrements stack pointer S
RES	Reset MPU to address zero; same as reset line
RRH	Right rotate Hex
RTI	Return from interrupt
RTS	Return from subroutine
SWI	Software interrupt; stacks all registers and vectors through SWI address
TST r	Test register; sets flags S or Z as tested; no effect on register
UPK	Unpack; inputs 2 bytes to register D, then outputs 3 ASCII characters
WAI	Wait for interrupt; stacks all registers and halts until interrupt or reset occurs

Outputs to memory or I/O are on a separate bus, with 3-state drivers. Another eight gates are included in these drivers. When programming BCD, the input gates hold off data on the upper 8 bits and insert zeros on those bits into register M. An ASCII BCD character is masked so that M stores only the 4 BCD bits.

Various instructions unpack the three BCD decades and output them one at a time to get ASCII BCD back. On the way, the gates in the output drivers turn the pure BCD back into ASCII BCD. To get back to normal inputs and outputs, program BIN and all the gates open. With BCD, the programmer must do the packing and unpacking. If a great deal of BCD arithmetic is used in a particular program, the function can go into a subroutine.

Extended addressing is indicated by an E after a memory reference instruction, followed by 2 address bytes. If PGE is programmed, the upper byte of program counter P and address register Z are locked. If a 1-byte direct address is used, it will still go into the first 4K or zero page. If E is programmed, 1 address byte can still be used, and the address will be in the 4K page indicated by the locked upper byte P or Z.

It is possible to jump around in memory by using 1- and 2-byte addressing or, by using PGE with only 1-byte addressing. To change any page but the zero page, program NPG, insert a new 2-byte address, then PGE again. This could even be put into an assembler as a pseudo instruction; program EA for extended address instead of E and the assembler takes care of inserting the new page number. NPG allows the MPU to escape from the page mode.

MFM allows the transfer of single bytes or strings of bytes between locations in memory or between memory and I/O. A simple protocol programs MFM, source address, CNT, number of bytes, and sink address. Since transferring only 1 byte would be cumbersome, the assembler could recognize a letter (eg, Z for zero) following MFM. Then, only MFM and two addresses are needed. Since this 12-bit MPU allows any addressing mode for any memory reference instruction, either or both of the addresses can be direct, extended, paged, indirect, or indexed. A block of memory can therefore be transferred from one page to another very easily.

Addressing modes provide flexibility

There are many addressing modes available in the 12-bit architecture. If E is not programmed after an instruction, it will be a 1-byte absolute address (direct). With E, the instruction needs 2 bytes. Indirect is selected by N after the instruction or after the E. This is a true indirect where the address in memory contains the effective address of the instruction instead of data. Indexed instructions are indicated by X. With this type of indexing, a 1-byte address can be put anywhere in memory. By using

indirect, a pointer in memory can point to a table. By adding N,X after an instruction, it goes indirectly through the pointer and the index steps it through the table.

Another useful addressing mode is program counter relative (P). In most MPUs, this mode is usually used for branches and is often unavailable to the programmer. An offset value is stored in memory and added to the program counter to form an effective address.

Most MPUs include immediate addressing. It is useful if the data are not changed during the program. The term immediate is used because the data follows immediately after the instruction, in place of an address. In earlier use, it replaced the address in a fixed length word.

The next two modes do not require a memory reference because the address is in register Y. Addressing register Y can be used like H and L registers in an 8080 or Z80. In the 6800 and others, this is called an index register and is indicated by X. Actually, however, it is an indirect addressing register like H and L, only it can also add an offset value stored in memory to the register's contents. This forms an effective address. It is the reverse of true indexing. This mode is indicated as Y,X (register indirect, indexed).

An MPU built to these hardware guidelines from modern silicon gate CMOS can have greater throughput and outperform all existing CMOS MPUs. It will also give most N-channel metal oxide semiconductor MPUs a run for their money. Decoding and control for such an MPU should be relatively simple because the bit structure of instructions lends itself to simple decoding. The hardware should be equally simple to control.

In total, there are 260 nonmemory and 2310 memory reference instructions, including all memory modes. Undoubtedly, users will think of others that have been left out.

These innovative concepts for MPU design can be used to overcome the limitations of present MPUs. Although the concepts and techniques can be used in a 16-bit MPU, more pins are required. The input and output buses could be combined, but larger chip carriers are the right answer. An ALU in Schottky transistor-transistor logic (TTL) can be made very fast, so such an MPU could be built in TTL if desired. Remember, however, that any attempt to save silicon by changing any of the concepts is bound to slow down performance, limit capabilities, or both. In any case, the 12-bit concept is worthy of serious consideration.

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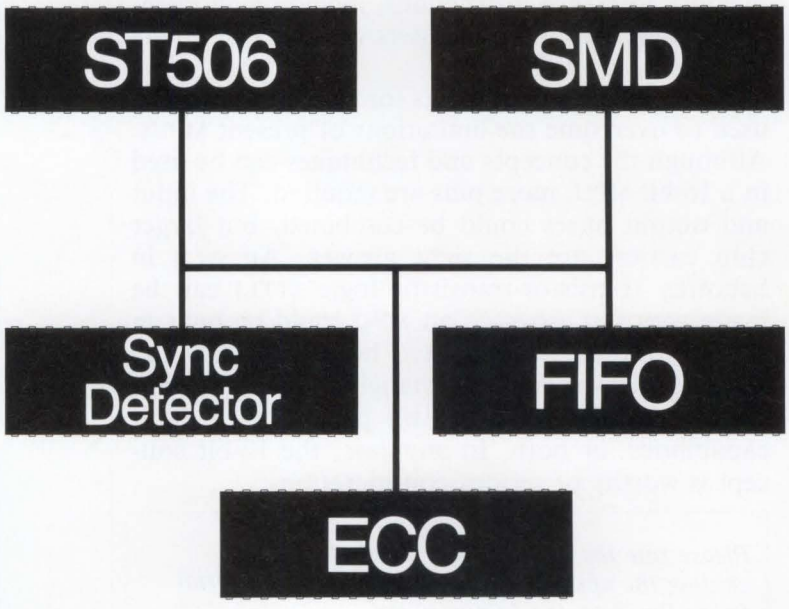

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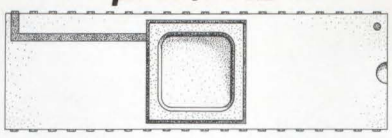

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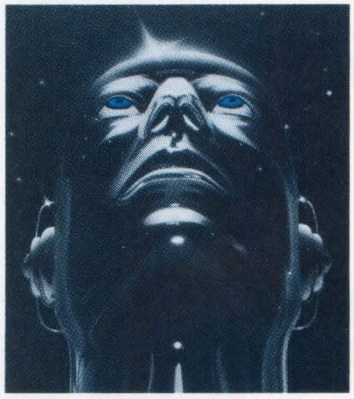

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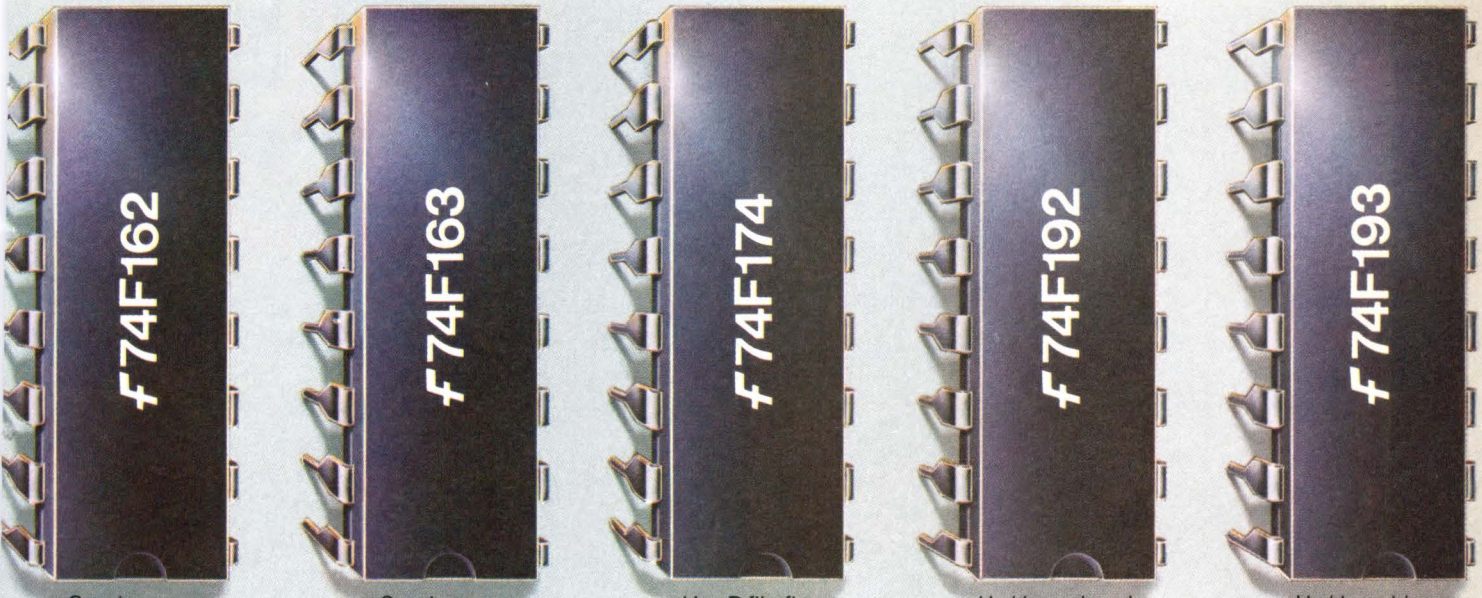

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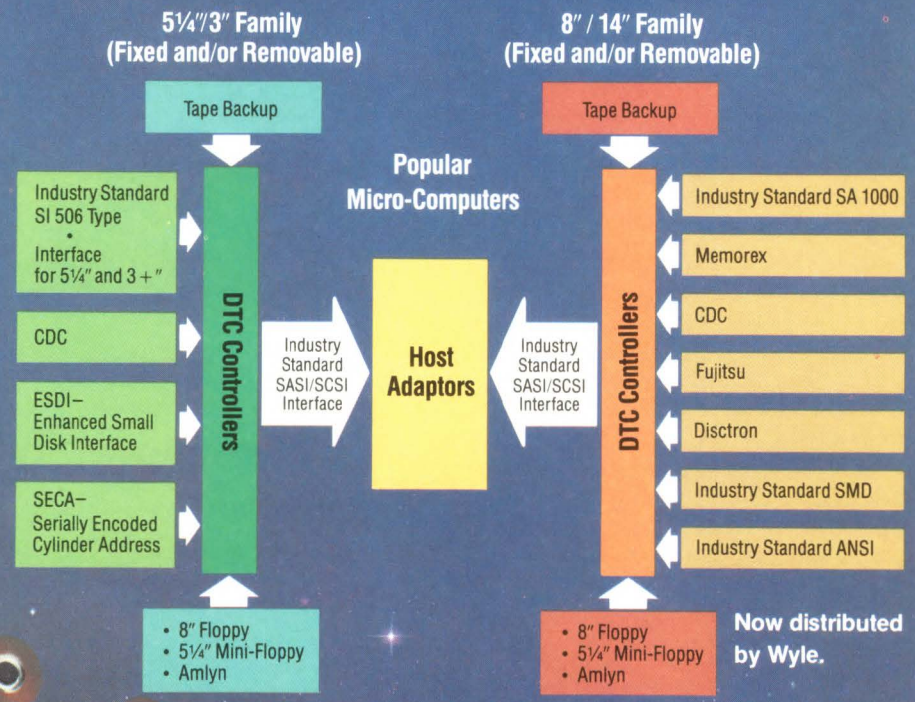

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CIRCLE 69

ADVANCED DATA ACQUISITION AIDS THE HANDICAPPED

Computer based acquisition and analysis tools are providing pathologists and researchers with insight into the mysteries of the spoken word.

by Andrew Davis and Ari Berman

Speech—it is not only one of the most complicated stimuli that humans perceive, its generation is one of the most skilled activities people engage in. Thus, it is not surprising that ear, brain, or vocal system injuries can have devastating impacts on human functions. Although prosthetic devices and special training are available to help some of the hearing and speech impaired, help is often unavailable for many of the more severely impaired. Consequently, there is a continuing need to better understand speech perception and production in order to find new ways to prevent or treat speech and hearing handicaps.

Andrew Davis is marketing director at Data Translation, Inc, 100 Locke Dr, Marlboro, MA 01752, where he is responsible for all marketing functions. Prior to joining Data Translation, he served as a product manager with Data General Corp. Mr Davis holds both a BS and an MS from Cornell University, and an MBA from Harvard University.

Ari Berman is a senior software engineer at Data Translation, Inc, where he is responsible for laboratory software systems. Prior to joining Data Translation, he worked for Data General Corp. Mr Berman holds a BS in computer science and artificial intelligence from the University of Massachusetts, Amherst.

Enter the computer

Speech research is technically intensive and, by necessity, interdisciplinary. Several social, psychological, and biological factors are involved. An adequate understanding of speech mechanisms requires input from linguists, psychologists, ear-nose-throat physicians, neurologists, speech therapists, and audiologists. In addition, speech research requires expertise in technical areas such as acoustics, mechanics, electronics, and, lately, computer hardware and software.

Historically, limitations in these technical areas have most impeded progress. Studies of speech perception require precise control over the time and frequency properties of sounds. The speech signal must be systematically dissected and then recreated in various ways to examine each acoustic component's contributions. In addition, since speech production involves a complex interaction of acoustic, physiological, and mechanical processes, its study necessitates sophisticated measurement of muscle movements and an ability to synthesize speech gestures.

Technically, both these tasks are extremely difficult to perform. The earliest speech studies used tape, wire, or disk recordings, signal generators, analog filters, mixers, and switches to measure, manipulate, or synthesize speech. Unfortunately, even though people hear speech as a series of discrete elements called phonemes, it really consists of spectrally varying cues that overlap in time. For this reason, a simple filter cannot extract a single

varying cue, and an analog recording cannot be cut into segments corresponding to phonemes. Neither can speech production be cut into segments corresponding to phonemes, nor can it be studied by examining a simple linear combination of movements or vocal tract shapes.

However, the advent of computer based recording, editing, and synthesizing promises great advances. Computers allow scientists to digitally record natural speech signals and gestures. In addition, computers can perform the high speed calculations required to spectrally analyze signals or synthesize dynamic speech events. All this can be done while maintaining precise control over temporal and spectral details.

Unfortunately, using a computer in these contexts presents several problems. Unlike analog analysis, computer processing involves manipulation of discrete digital values stored in memory or on a mass storage device. This raises several design issues. For one, what are the memory and storage requirements for recording or synthesizing speech signals? Also, what digitization rates are appropriate and possible? And finally, how are hardware and software to be optimized for speech research?

In part, the amount of storage required depends upon the duration of the signal to be analyzed. The smallest speech segments that carry linguistic information are from 20 to 100 ms long. However, these segments ordinarily occur in the context of syllables or words that are up to 1 s long. This fact plays an important role in perception because overall speech segments contain temporally distributed, redundant information that increases speech intelligibility in noisy or distorted environments. This redundancy is particularly important to the hearing impaired, whose auditory systems add distortion. Thus, the study of speech segments in their natural environment requires digital samples at least 250 to 1000 ms long.

Two additional factors dictate durations longer than this, however. Since speech events occur rapidly, it is often necessary to record a signal window two or three times as large as the target event. An optimal window seems to be about 2.5 s wide. The second factor influencing duration is whether individual speech segments called suprasegmentals are to be studied.

Suprasegmentals are signal characteristics conveyed during relatively long sequences of smaller segments. They include the sentence intonation and amplitude contours and are typified by the difference between the utterance "You know why!" and "You know why?" Suprasegmentals also reveal emotional or psychological information. An increase in speech rate might signify heightened speaker anxiety. The study of suprasegmentals is particularly important for developing speaker-recognition systems. Analysis of suprasegmental features requires digitalization of utterances over a wide range of sample periods, from tens of seconds to minutes. The storage limitations of older computer systems demanded that suprasegmentals be studied by breaking large utterances into smaller, more manageable segments — a very tedious process. Today, the direct-to-disk system of storage greatly increases the efficiency and the flexibility of such analysis.

A powerful tool used in modern speech research is Data Translation's DT4136 LAB-DATAX acquisition system. This unit provides high speed continuous data flow to microcomputer memory and/or disk storage. Based on a 16-bit computer, it includes the company's specialized analog to digital (A-D) interface with its unique random access memory (RAM) channel file multiplexer, a digital to analog (D-A) interface, and a realtime programmable clock (Fig 1). Together with the package of FORTRAN callable subroutines, the system provides up to 250k-sample/s throughput to memory or 100k-sample/s throughput to disk without the loss of any interbuffer data points. The high disk throughput can be sustained until 36M bytes of disk storage have been filled. Hence, speech signals can be recorded for time periods well over 1 min.

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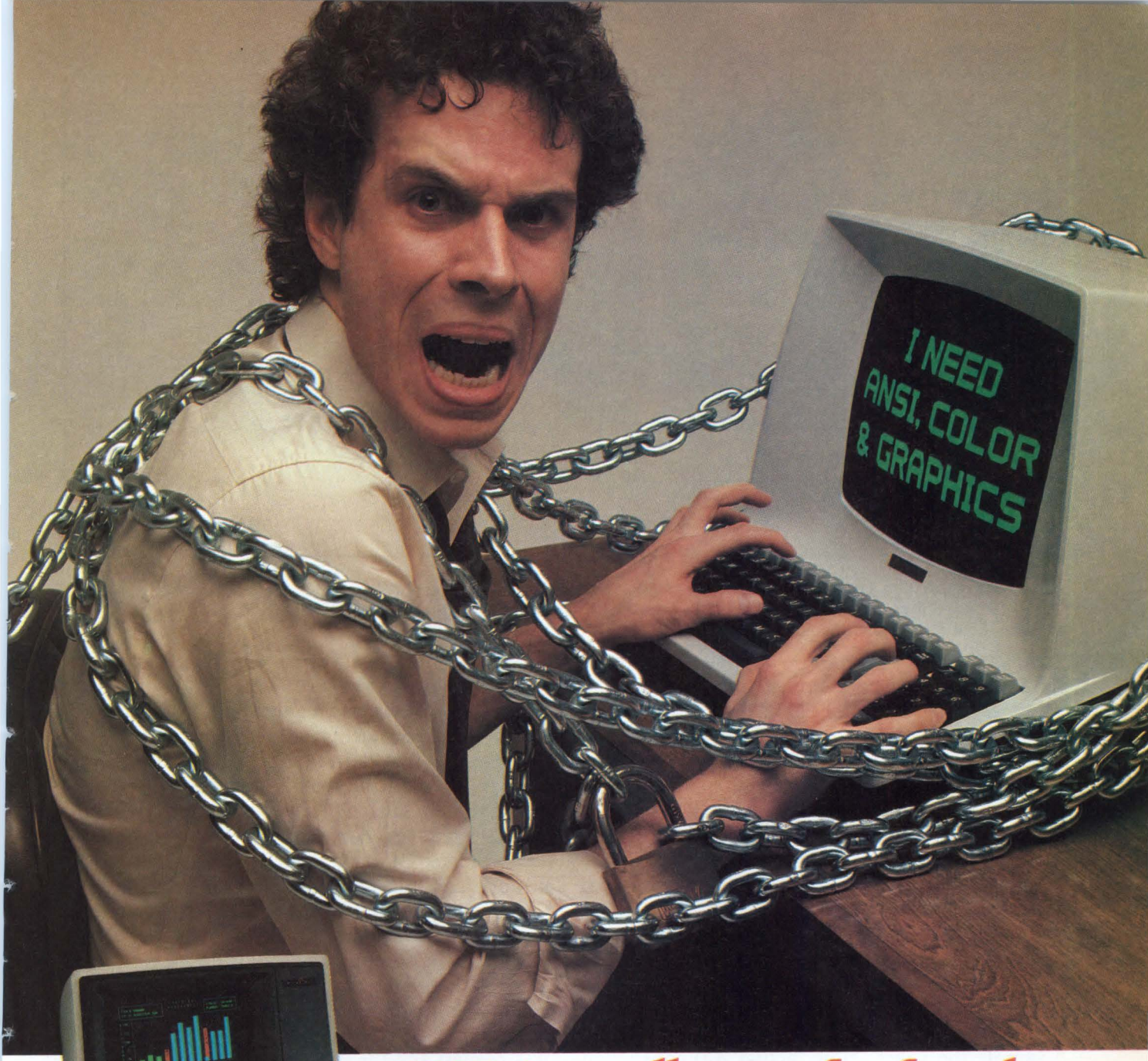
Gathering data from an experiment or real world process with a microcomputer or minicomputer based data acquisition system has been traditionally limited to either slow data rates or small numbers of data points. These limits result from hardware and software constraints imposed by 16-bit architectures, instruction execution times, software designs, operating system overhead, and throughput-to-disk limitations. These limits arise not only when one signal must be sampled at a high rate, say 50 kHz, but also in seemingly modest multichannel situations. For example, sampling 16



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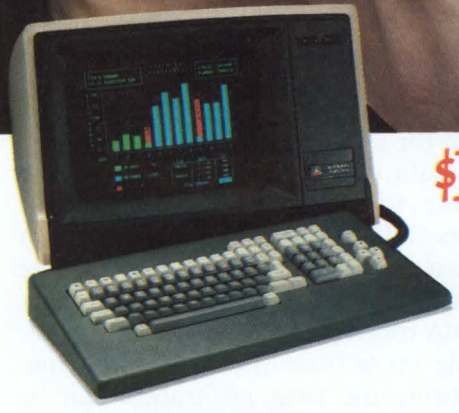

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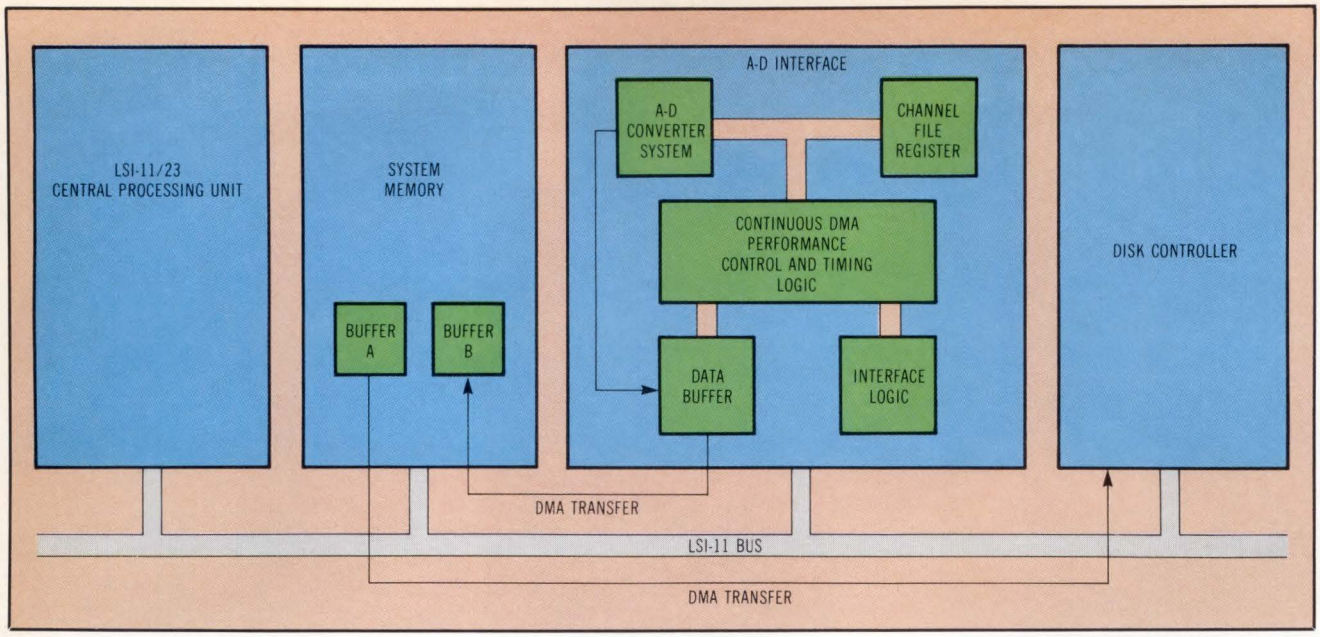

Fig 1 Data acquisition system elements include the LSI-11/23 processor, A-D converters and interfaces, and RAM channel file multiplexer. Several channels can be sampled at optimized individual rates. Maximum system throughput approaches 250k samples/s.

channels at 2 kHz per channel for 2 s requires a system level A-D rate of 32 kHz and the storage of 64k samples.

When A-D converters operate below 20k samples/s, the central processor can be called upon to directly manipulate the A-D interface, using programmed input/output data transfers. However, when acquisition rates of greater than 20 kHz are required, the A-D board must move the data to memory using direct memory access (DMA) I/O.

Usually, when an analog input signal is measured, a multiplexer is directed to switch to the specific channel. A sample-and-hold circuit is fed by the multiplexer's output. When the multiplexer has settled, the sample-and-hold circuit is allowed to sample the value. Now, actual A-D conversion can begin. The A-D trigger first switches the sample-and-hold to hold and then starts a successive approximation A-D conversion. Once the conversion is complete, an interface board makes a DMA request. When the A-D interface becomes bus master, data are transferred to memory. This process is repeated until a buffer of data has been acquired.

Once a buffer in memory is filled, its data must be written into a disk file while the A-D converter transfers data to a second buffer. When the second buffer is full, it will also be sent to the disk while the A-D converter again fills the first buffer. This mode of operation is called double buffering.

Memory buffer data can be moved into a disk file at very high rates. Unfortunately, the data can be transferred only when the disk's read/write head has been correctly positioned and an appropriate storage area on the disk surface has come under this head. The time required for each of these events to occur is highly variable. Therefore, each data buffer must be large enough to hold data until the previous data buffer has been written to the disk, or until the disk is ready to accept data from the new buffer. The entire data acquisition process resembles a series of pipelines: data conversion, transfer of data from the A-D interface to memory, and transfer of data from memory to disk.

The first pipeline is the A-D subsystem, which is capable of converting 250k samples/s. The second pipeline is the computer bus and the A-D interface board. When data are ready to be transferred to memory, the interface requests bus control. Because the DMA latency (ie, the time between the DMA request and the DMA grant) can be more than 4 μs, the analog data word is moved from the A-D converter module to an onboard data buffer. Therefore, a second A-D conversion can begin almost immediately after the first is complete. The A-D interface will perform either single-word or double-word DMA transfers.

By transferring more than one word at a time, the time lost during the DMA arbitration can be averaged over more than one data transfer. The decision to transfer a single word, or a pair of words, is left to the very last moment. By waiting, the probability of performing a double transfer is maximized. A double-word transfer allows the onboard DMA to "catch up" when a DMA latency is unusually long.

Disk drive, the third pipeline, introduces a DMA latency factor far greater than that of other components. Adequate-sized data buffers are required to overcome the up to 40-ms delays encountered in

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CIRCLE 71

transferring data to disk. The CPLIB software package utilizes a pair of data buffers, each of which is 8192 bytes long.

Despite careful integration of hardware and software, the maximum continuous throughput to disk of conventional systems is limited to approximately 10k samples/s. The switching process of conventional A-D interfaces imposes this limit. When a conventional A-D interface has finished filling a buffer, it stops acquiring analog data and issues an interrupt to the processor, which then requires from 20 to 100 μs to respond.

When the processor finally begins to execute the interrupt service routine, it must load the A-D interface with the information necessary to restart the acquisition process. Typically, this information includes the new buffer address, the number of samples to acquire, and an A-D control word. This restart process takes approximately 50 μs for an LSI-11. During both the interrupt latency period and the interface restart period, a conventional A-D cannot acquire data.

Speech is a highly skilled action and, as such, involves the simultaneous activation of many muscles.

The consequences of the A-D's not being active for a variable period of time are twofold. First, while the A-D is shut off, it cannot receive trigger pulses from the device, such as a programmable clock, which controls the sampling rate. Therefore, the minimum clock period (the intersample interval) must be larger than the maximum period during which the A-D is inactive. Otherwise, some requests for samples (clock ticks) will be ignored (thus, samples will be lost). Obviously, if no points are to be lost, the worst-case A-D restart condition must determine the maximum sampling rate. With careful design, the restart time can be held to 100 μs, so the maximum sampling rate is 10k samples/s.

Second, while the clock is inactive it cannot sense trigger pulses that may be sent to it. Thus, the clock cannot inform the software that it has missed a data point. For this reason, any attempt to drive the A-D at a speed higher than 10k samples results in the undetected loss of one or more data points. These lost data points cumulatively degrade the time-domain analog data being acquired and, in certain situations, render the data invalid.

Careful design for higher throughput

With its specialized analog I/O hardware and software and its Winchester disk optimized for data throughput, the DT4136 system provides a larger data buffer (98,048 samples) than did previously available laboratory data acquisition systems, as well as higher throughput rates to memory. But, a major breakthrough is the system level integration. With wrap-around buffer management, this allows continuous throughput to disk at 100k samples/s.

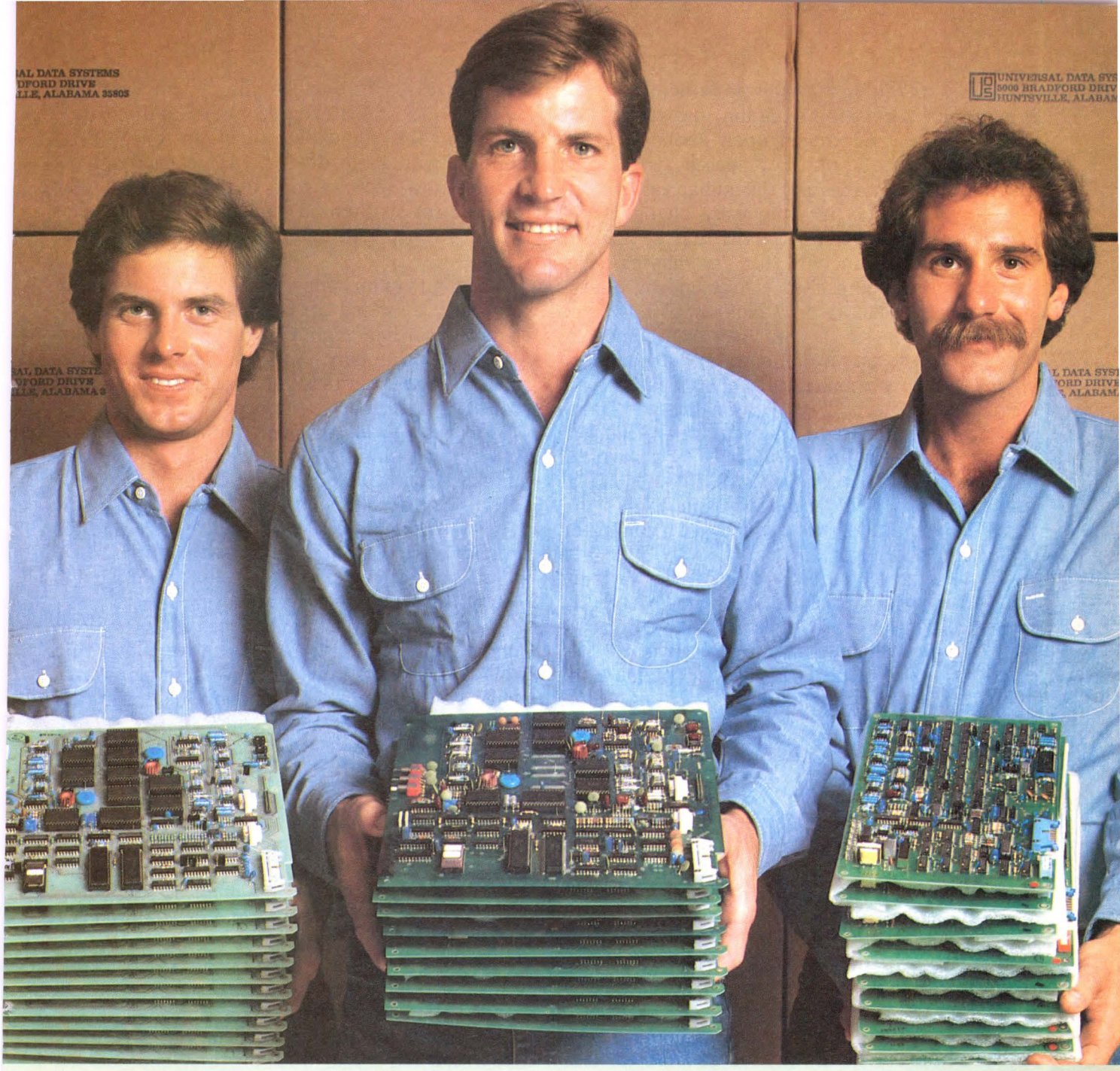
This system achieves high performance by the introduction of innovative hardware and software techniques for data acquisition interfaces. The hardware architecture, which supports 250k-sample/s throughput, multiple triggering and sampling schemes, and a RAM channel/gain list file for user programmable gain and multiplexing, is based on a threaded buffer interrupt handling system.

Such an approach allows the DMA hardware onboard the A-D interface (also the D-A interface) to chain between buffers without stopping the data acquisition process. An interrupt is generated when a buffer is nearly full, rather than when it is actually full. However, unlike conventional hardware approaches for data acquisition, the A-D interface in this system does not stop when it issues an interrupt. Instead, it continues to fill buffer A.

Meanwhile, an interrupt service routine performs the functions necessary to have the system begin filling buffer B. While buffer B is filling, the software determines how much additional data were put into buffer A, after the initial interrupt. Via bookkeeping, additional data are redirected into buffer B. In addition, while buffer B is filling, buffer A's contents are being sent to disk. When it is nearly full, buffer B will likewise generate an interrupt service request and the process will repeat. This A-B-A-B buffer scheme provides continuous, no data-gap data acquisition up to the limits of available disk storage.

To support these continuous data transfers, the software package comprises a library of routines designed to be linked to a user's FORTRAN application program under the RT-11 operating system. Combining several techniques makes continuous data acquisition possible. Drivers are system resident, that is, they are really RT-11 device handlers rather than device drivers linked to the user's application program. Hence, I/O requests can be handled as RT-11 system requests. This ensures that the drivers are resident even if a user's program fails. Although this makes the CPLIB drivers more complex to design, it provides for smaller and faster interrupt service requests.

Another unusual aspect of this software is that the drivers dequeue an I/O request as soon as the I/O starts, rather than after it ends. This approach allows the I/O drivers to prepare for the next I/O request while the first is still running. Completing all possible calculations in the initiation (startup) section of the device handler minimizes interrupt service routine execution time. Dequeuing also gives the software time to manage the threaded buffer bookkeeping tasks.



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CIRCLE 72

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Measuring speech mechanisms accurately

In any data acquisition situation, the appropriate sampling rate is dependent upon frequency range and desired resolution. For speech, vocal tract acoustic characteristics and the human ear's resolving power define the frequency requirements. Speech production can be modeled as an acoustic filter transfer function for a varying-cross-sectional-area tube excited at one end by a noise source (eg, the larynx or Adam's apple). The excitation source is a roughly trapezoidal or triangular wave with a rich harmonic structure extending to approximately 10 kHz. Fundamental frequencies of around 100 Hz for men and 200 to 300 Hz for women and children are typical. The vocal tract above the larynx acts as a series of dynamic filters that shape the harmonics of the fundamental to yield an output signal. This signal varies in amplitude and frequency depending on changes in cavity size.

Larynx vibration is only one of the ways the vocal tract can be excited. In whispered speech, air is pushed past an open larynx, creating a broadband hiss that is then shaped by the tract. Hiss excitation can also be produced at other points along the vocal tract by constricting air flow. This occurs for sounds such as the s in see or the j in justice. Suddenly releasing air pressure to create a burst of noise, as with the k in key, is another instance of localized sound production. Hisses, constriction noises, and bursts all can have meaningful frequency components above 10 kHz.

The diversity of speech research problems and approaches requires that each laboratory develop much of its own software.

Taken together, these acoustic components of speech require a bandwidth of at least 10 kHz. Often a bandwidth as large as 15 or 20 kHz is necessary to contain speech data. Bandwidth requirements are further complicated during digital signal playback analysis. Here, signals must not only be recreated at precisely the same rates at which they were recorded, but they must be mixed accurately to create stereo reproduction. Several experimental applications require simultaneous playback of two signals—for instance, to study the effect of one sound upon the intelligibility of another. This dual channel playback not only doubles signal storage requirements but also increases the required bandwidth by 20 to 40 kHz.

Bandwidth directly determines the digitizing rate required. The widest bandwidth (BW) for a particular rate (R) is known as the Nyquist frequency and has the value BW = R/2. For example, an acoustic bandwidth of 15 kHz requires a rate of at least 30 kHz. Fortunately, the system described here provides stable external timing and maximal true rates (input and output) of up to 250 kHz. Coupled with large data storage capacity, these features allow speech signals of long duration to be recorded (or synthesized) and played back one or two at a time, with natural fidelity and accurate timing.

Although multichannel audio recording is not frequently required in speech research, multichannel recording of audio plus other analog information is commonly required. This need arises when the coordination of the vocal tract activities producing speech are examined.

Speech is a highly skilled action and, as such, involves the simultaneous activation of many muscles. Control problems are common in many speech disorders ranging from stuttering, to the overly nasal sound of deaf persons' speech, to the complex misarticulations found with injuries to the muscle control centers in the brain. Investigating these disorders, as well as normal speech mechanics, involves the simultaneous monitoring of muscle activity, articulator movement, and acoustic output. A typical application might examine larynx activity, jaw movement, lip muscle activity, nasal air flow, and acoustic output (Fig 2). Differences in the relative timing and degree of these variables subtly distinguish the sounds of the letters m, n, b, and p. A deaf person's speech is often characterized by abnormal nasal air flow during pronunciation of m or p. This produces what sounds like n or b. Using multichannel monitoring, the nature of the incorrect control of nasal air flow can be studied and new approaches to speech therapy suggested.

Not surprisingly, this sort of multichannel recording presents technical problems. Principal among them is the differing data rates required for each channel. The audio recording, as previously noted, can require digitization rates approaching 30 to 40 kHz. Muscle electrical activity, detected by fine wire electrodes fastened to the skin, requires data rates of only 100 Hz or so. Air flow as measured with a thermistor, larynx vibration as measured with a sensitive accelerometer, and jaw movement as measured with a strain gauge demand even lower sampling rates. Most A-D systems allow for multiplexed multichannel recording. Unfortunately, many of these systems also require that all channels be sampled at the rate of the highest data rate channel. A multichannel measurement, as shown in Fig 2, requires rates in excess of 150 kHz. With this method, nonaudio channels are grossly oversampled, and valuable data storage is squandered.

The LAB-DATAX system is designed to eliminate this problem by using random channel addressing. Here, the appropriate choice of an overall

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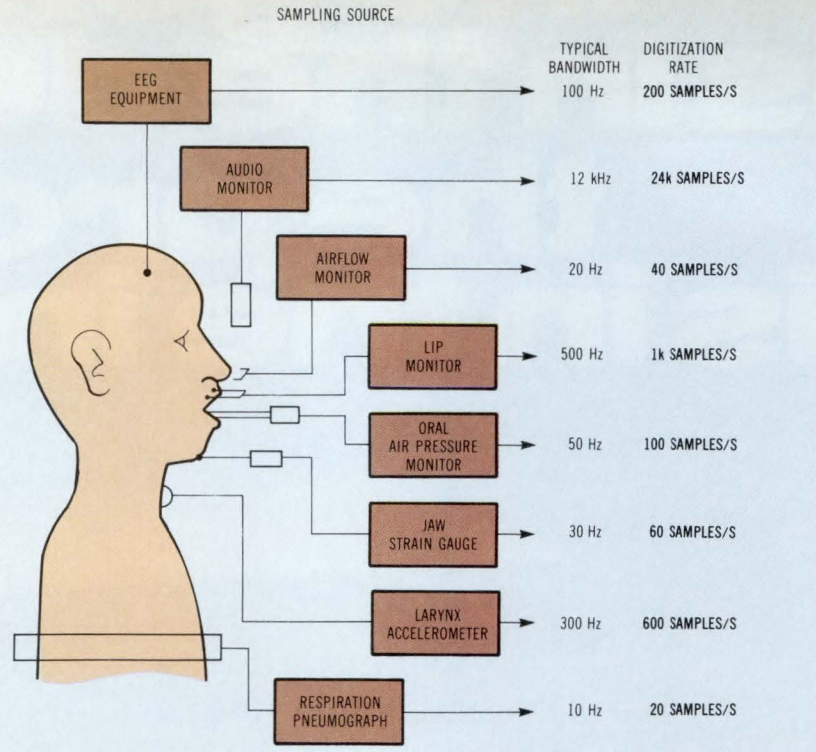

Fig 2 Shown here is a typical multichannel data acquisition situation encountered in speech research. Data relating to muscle movements, sound production, and cavity constriction are simultaneously gathered from several channels and recorded on disk. Data can then be displayed, compared, and recombined to ascertain where speech related problems lie.

sampling rate, in conjunction with a channel-addressing scheme, allows the audio channel to be sampled more frequently than other channels. Now, each channel can be digitized at a rate closer to optimum.

This performance is achieved by the use of a RAM channel file implemented on the A-D (and D-A) interfaces. The multiplexer channel file is an on-board 1024-byte RAM, which is divided into four 256-byte pages. The LSI-11 processor has read/write access to the RAM so that it can store (and read) the channel numbers to be input or output in any desired sampling order. Each entry in the channel list file on the A-D interface includes 6 bits for channel number information and 2 bits for gain determination. On the D-A interface, the RAM includes 6 bits for channel number and 2 bits for a deferred trigger mode.

Access to the channel list from both the processor and the A-D or D-A converters is controlled by a set of pointers that allow the user to set the board to scan, within a 256-byte page, only as much of the channel list as is required during an operation. The channel address pointer automatically increments after each conversion until it matches the final address pointer. It automatically resets to the value held in the start address pointer at this time.

RAM channel list file flexibility includes three conversion schemes, each of which can be controlled by software or external triggers. With the single-channel approach, each trigger causes one element in the channel list to be converted. With the channel-scan approach, each trigger causes the entire list from start address pointer to final address pointer to be converted. With the burst mode, each trigger causes a preset number of conversions (specified by a word count register) to be performed, regardless of how many times the channel list must be scanned. None of these conversion schemes require processor intervention and they can be performed at the full speed of the A-D or D-A interface.

Editing acquired data

Digitized speech information is rarely studied in its raw form. Analysis usually requires averaging input root mean square amplitudes or relative decibel levels. In addition, experimental interest may focus on one of two input segments. The desired segment must be extracted from its context for further examination. Although some automatic signal processing schemes have been developed for such analyses, most experimental approaches require an interactive mode in which the scientist reviews recorded data and marks events of interest. Such editing is virtually impossible in the absence of a computer-controlled signal display. Some applications use a cathode ray tube to plot stored data. Other more crude systems use a storage oscilloscope to display successive segments of data. By repeated searches of the data stream, the scientist can isolate and mark segments for analysis or excision.

LAB-DATAX offers an alternative to these options. The high speed D-A system is designed to dump digitized data in a dynamic, point-plot mode

using a standard, X-Y display, laboratory oscilloscope. A few simple software commands scroll up to eight channels of stored data, from memory or disk, across the screen. Labeling of channels, sample number, and instantaneous amplitudes are automatically provided. The display software, directly accessible by user-written FORTRAN programs, provides listings of marked segments for further analysis. In addition to providing relatively inexpensive signal editing, the display option maximizes use of the unique signal storage and D-A conversion system modes.

The diversity of speech research problems and approaches requires that each laboratory develop much of its own software. Unfortunately, as advances in technology extend signal processing possibilities, increasing technical complexity makes programming difficult. For instance, the DEC 11/23 system provides for both virtual memory addressing beyond the 16-bit word limitation and for non-central processing unit DMA bus control. Using virtual memory greatly increases the amount of storage available, and the device-driven DMA also increases signal throughput. Use of these and other sophisticated features requires a programmer intimately familiar with both the hardware and machine language. Sadly, few laboratories can afford this kind of support personnel.

A distinct advantage of the LAB-DATAX system is its application-oriented software. All subroutines in the DTLIB and CPLIB packages are designed for easy incorporation into user-developed FORTRAN programs. Since the packages are authored by software professionals familiar with the demands of speech data acquisition, subroutines fully exploit the advanced technical features of both the DEC 11/23 and the data acquisition hardware.

Joining powerful computing and data acquisition hardware with accessible, yet effective software helps to meet the rigorous demands of speech related data acquisition. The result of this technical commingling is most gratifying. When technology serves humanity in such profound and therapeutic ways, it is at its most noble.

Acknowledgments

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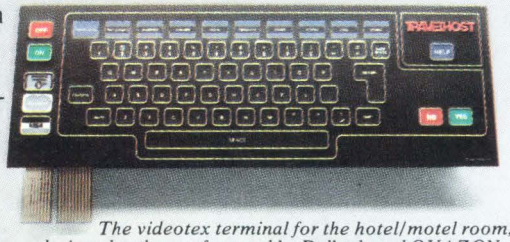

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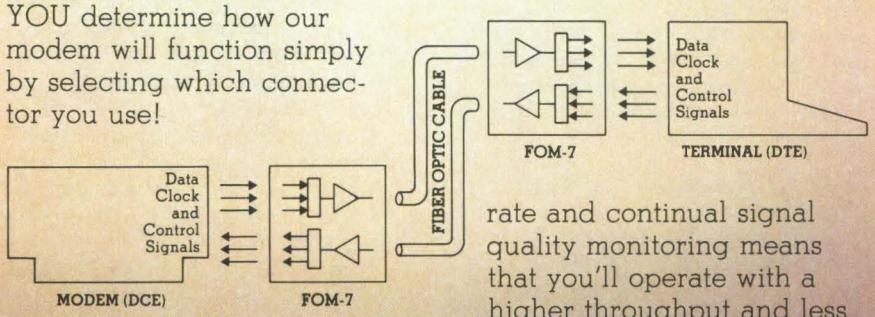

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GENERATING HUFFMAN CODES

Time and space are saved when alphanumeric data are compressed and represented by these efficient encoding schemes.

by George Grosskopf, Jr

Modern computers store and transmit vast amounts of data. As the requirements for storage and transmission increase, the physical limitations of the computer system become evident. One way to partially overcome these limitations is by using Huffman encoding techniques to compress data. Huffman encoding produces optimum, variable length codes that represent a finite number of characters. These characters can be alphabetic, numeric, or alphanumeric. In fact, Huffman encoding methods can be used with ASCII characters. Here, the ASCII 7-bit word used to represent up to 128 alphanumeric characters can be compressed to allow additional data to be stored or to reduce the time required to transmit the data.

When using Huffman encoding with ASCII characters, shorter Huffman codes are assigned to characters that frequently occur. Longer codes are assigned to characters that are less frequent. This assignment can be depicted as

$$P(1) \geq P(2) \geq P(3) \geq \ldots P(N-1) \geq P(N)$$

George Grosskopf, Jr is currently the engineering manager at Litton Systems Inc, AMECOM Div, 300 Kennedy Dr, Hauppauge, NY 11787. Mr Grosskopf is responsible for the digital design engineering on all projects, and the design of a digital facsimile.

where P(1) is the probability of character 1, P(2) is the probability of character 2, and so on. N is equal to the number of characters to be coded. The assignments for the length of the codes must be

$$L(1) \leq L(2) \leq L(3) \leq \ldots L(N-1) = L(N)$$

where L(1) is the length of the most probable code, P(1); and L(2) is the length of the next most probable code, P(2), etc. Though it is possible that codes for characters with the same probability of occurrence can differ in length, interchanging these codes will not affect the total number of bits required to store or transmit a message.

Some restrictions on the Huffman code of characters do exist. For instance, no two coded characters can be represented by identical code words. Also, codes are constructed in such a way that shorter codes will not appear, bit by bit, as the first part of a longer code. Two coded characters, with a code length of L(N), have codes that are the same except for the last bit in the codes. Finally, each possible sequence of L(N) − 1 bits must be used either as a code or one of its prefixes must be used as a code.

Generating Huffman code

Huffman codes are generated from tables. Table 1, a Huffman code reduction table, illustrates the steps required to generate typical Huffman codes. The first step required in generating Huffman codes is to list probability values, or reduction

TABLE 1

Huffman Code Reductions

Char	Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10
									→0.55	→0.99
								→0.44	0.44	
							→0.28	0.28		
0	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.27		
						→0.24	0.24			
					→0.20	0.20	0.20			
4	0.16	0.16	0.16	0.16	0.16	0.16				
3	0.12	0.12	0.12	0.12	0.12	0.12				
			→0.12	0.12	0.12					
				→0.12	0.12					
2	0.10	0.10	0.10	0.10						
9	0.10	0.10	0.10	0.10						
1	0.06	0.06	0.06							
5	0.06	0.06	0.06							
6	0.06	0.06								
8	0.04	→0.06								
7	0.02									
	①	①			⓪		⓪		①	Huffman Code

codes, of the set of characters to be compressed. These values were calculated from the list of phone numbers in Table 2. The list of probability values appears in column 1 of Table 1. The column is organized with the most probable character at the top, and the least probable character at the bottom.

It is mandatory that the two least probable characters have codes of equal length, and that two coded characters, with a code length of L(N), have codes that are alike except for the last bit. To allow for these restrictions, the bottom two reduction codes must be combined. This combination is referred to as an auxiliary character.

To accommodate the final restriction on codes, that each possible sequence of L(N) – 1 bits must be used either as a code or one of its prefixes must be used as a code, a new column must be created (column 2). This column contains all the reduction codes that were not previously combined, plus the new auxiliary character. In creating this column, the auxiliary character will be handled and referred

TABLE 2

Encoded Bit Requirements

Phone Number	Number of Bits for ASCII Codes	Number of Bits for Huffman Codes	Number of Bits for Binary Codes
423-2000	49	18	28
699-1054	49	23	28
853-9494	49	24	28
486-0100	49	22	28
233-6530	49	23	28
792-4400	49	21	28
243-1000	49	19	28
TOTAL	343	150	196

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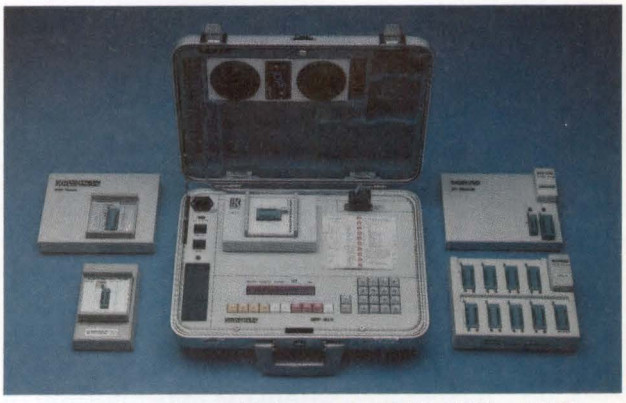

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TABLE 3

Huffman Codes for Numeric Characters

Characters	Huffman Codes
0	01
1	1010
2	110
3	001
4	000
5	1011
6	1000
7	10011
8	10010
9	111
	MSB LSB

to as another reduction code. The column must be rearranged by order of probability and will also contain one less reduction code.

Once again, the bottom two reduction codes are combined to form a new auxiliary code. A third column is now formed using all the reduction codes that were not combined in column 2 and the new auxiliary code. This procedure is repeated until a column with only one reduction code results. (See column 10 of Table 1.)

Now, Huffman codes can be generated from the reduction table. A bit is defined in a Huffman code if the reduction code or the auxiliary character of the character to be coded is contained within a bracket. If the reduction code or the auxiliary character is located in the upper portion of the bracket, then a bit in the Huffman code is defined to be 0. This bit is defined to be a 1 if the reduction code or the auxiliary character is located in the lower portion of the bracket.

For example, the shaded area of Table 1 highlights the generation of the Huffman code for the character 7. Column 1 shows the reduction code for the character 7 contained within the lower portion of the bracket; therefore, a bit in the Huffman code is defined to be a 1. Column 2 shows an auxiliary character for character 7 contained within the lower portion of the bracket; thus, the next bit in the Huffman code is also defined to be a 1.

Columns 3 and 4 do not contain combinations of the auxiliary characters for the character 7; therefore, these two columns do not define a bit in the Huffman code for the character 7. (Note that columns 3 and 4 do contain combinations of the auxiliary characters for the characters 1, 5 and 9, 2, respectively.) Another auxiliary character for the character 7 is contained within the upper portion of the bracket in column 5; thus, the next bit in the Huffman code is defined to be a 0. This procedure is continued until all auxiliary characters contained within brackets are employed to define the Huffman code for the character being coded.

Table 3 illustrates the Huffman codes generated with the aid of the Huffman code reduction table. The right column is a tabulation of the Huffman bit patterns used to represent the characters in the left column. Using ASCII codes to represent the phone numbers of Table 2, the number of bits required by a computer to store or transmit this information is 343. Applying the Huffman codes of Table 3 to the problem, the total number of bits required to represent the same information is reduced to a mere 150. This represents a savings of approximately 50% in the number of bits required to store or transmit this data. More importantly, the same computer system can double the amount of phone numbers it stores, or halve the time required to transmit them.

Obviously, ASCII codes are not the optimum set of codes employed to represent the phone numbers used in Table 2. If 4-bit binary codes are employed to represent these phone numbers, the number of bits required to store or transmit them would only be 196. Employing Huffman codes instead of the binary codes to represent the phone numbers means a savings of approximately 30% in the number of bits required to represent them.

Wide-ranging Huffman code application

Huffman encoding can be employed in facsimile equipment, digital television, and word processors. In word processors, Huffman encoding can increase storage capacity at no extra cost.

Huffman encoding need not be limited to just characters either. It can also be used to generate codes for common combinations of characters, known as digraphs, as well as commonly used words such as and, is, the, or the mnemonics in an assembler. Although these combinations might not be the most probable, they could offer additional compression. Computers and dedicated word processors also store additional control characters to control printer and disk formats. These control characters can be encoded, removing the conflict between these special control characters and the variable-length codes generated by Huffman encoding. In short, Huffman encoding techniques can provide many advantages to systems where storage is at a premium or data transmission rates must be maintained on existing hardware.

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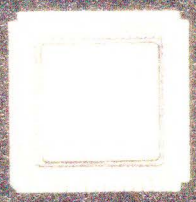

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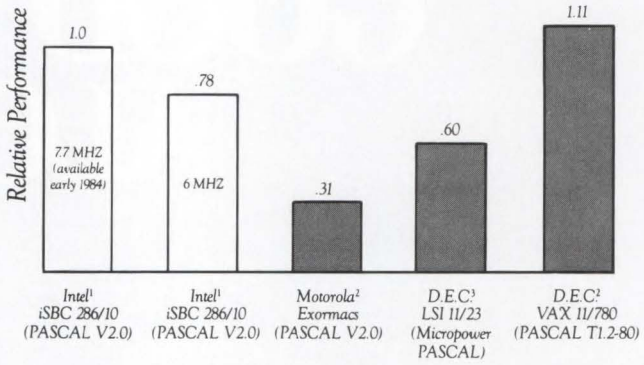

[1]*Based on Eratosthenes Sieve Benchmark in PASCAL. Details available from Intel's "Eratosthenes Sieve Prime Number Benchmark on the ISBC 286/10 Board," literature order number 210984.* [2]*"Eratosthenes Revisited," BYTE. Jan., 1983.* [3]*"A System/Architecture Approach to Microcomputer Benchmarking." Digital Equipment Corporation. Sept., 1982.*

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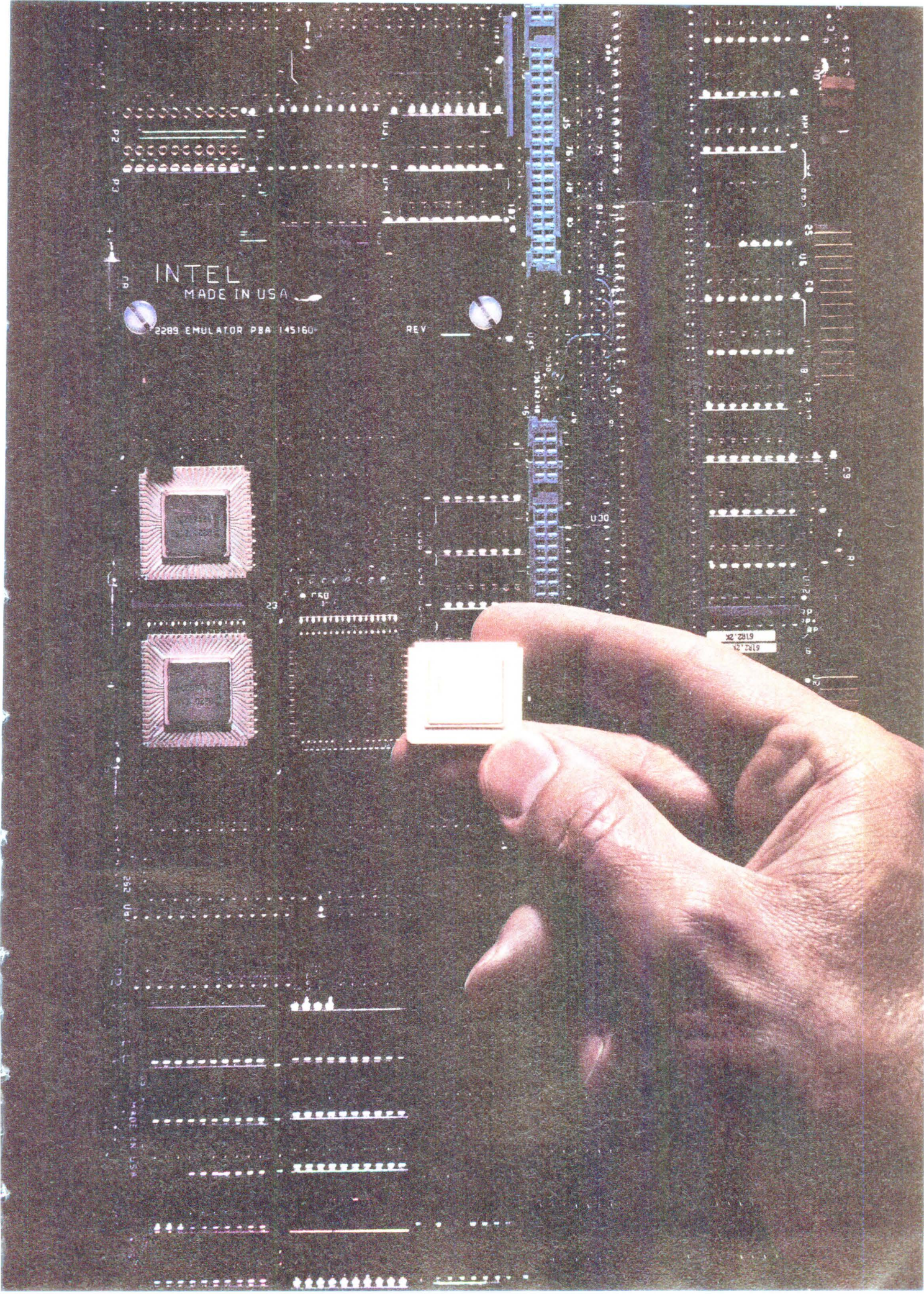
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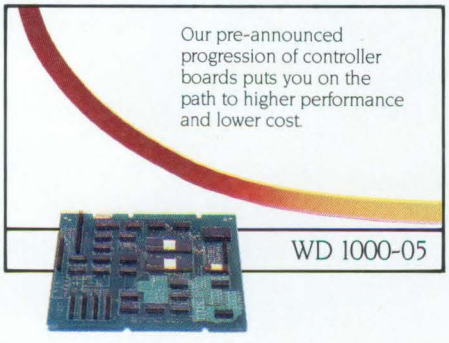

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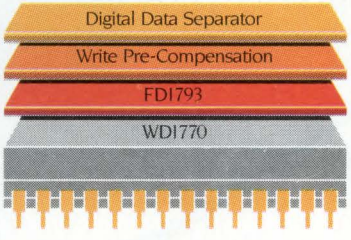

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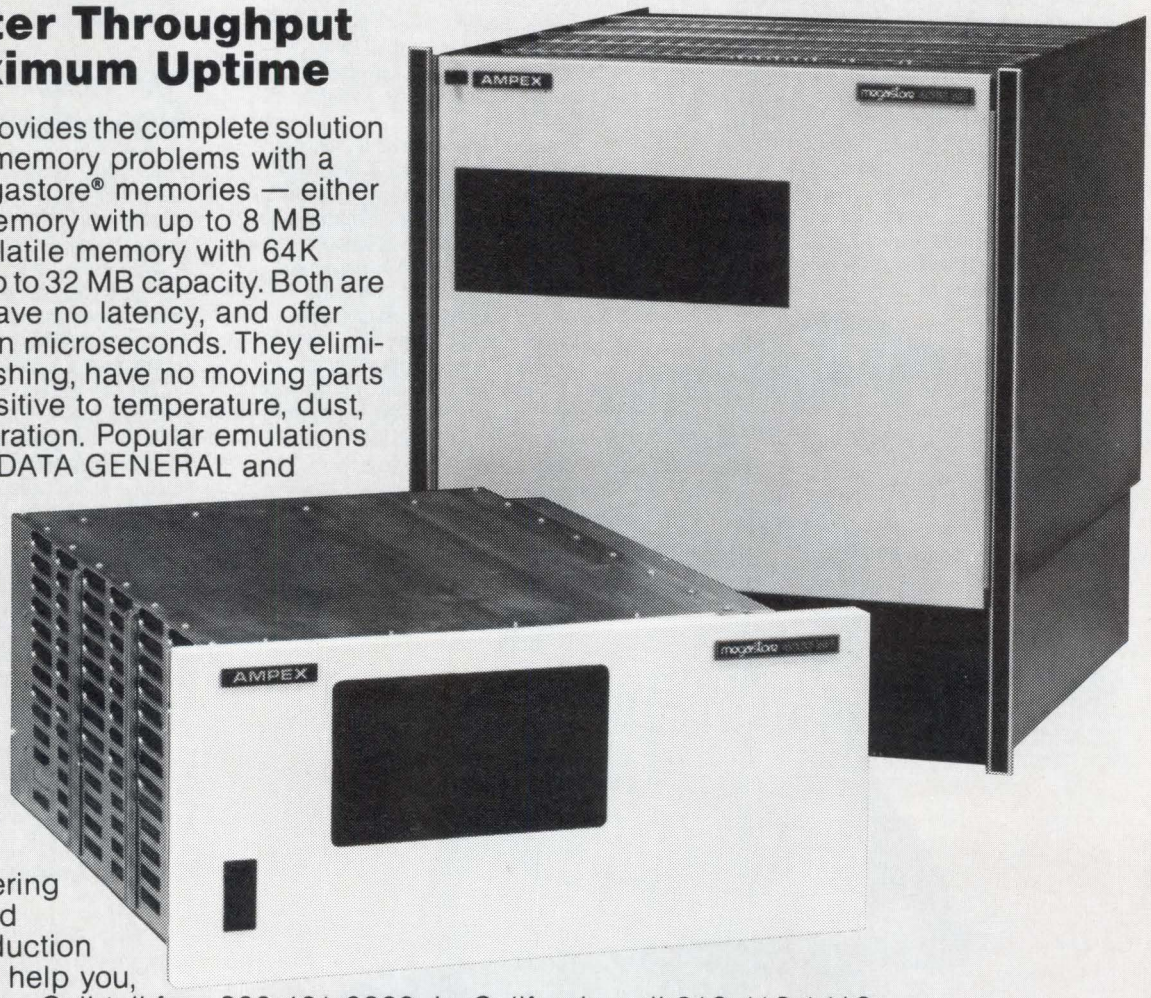

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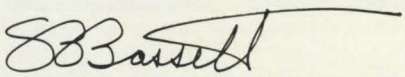
The new 16- and 32-bit CPU chips are putting sophisticated operating systems and large number-crunching programs on microcomputers. Despite the spectacular rise in RAM capacity (and drop in price), continuously keeping all this software in memory is impractical and undesirable. The rise of multi-user systems makes memory space increasingly valuable. Virtual memory management has been available in mainframe software for years and is now migrating to microcomputers—in silicon. A number of manufacturers are producing memory management units to go with their powerful CPUs.

Parkinson's Law states that a work load increases to fill its time and space allocations. Computer applications are no exception, but for one difference—if they work too fast, the peripherals they control cannot keep up. Using memory to put a buffer between a fast processor and a more leisurely peripheral is nothing new, but more capable devices like FIFO buffers are taking over the job from RAM and leaving the CPU free for computing.

Keeping data accessible when the power is off once involved many trade-offs. While tapes and disks are cheap and spacious, they are also slow. Batteries and uninterruptible power supplies are expensive and not always reliable, and ultraviolet erasable PROMs are slow to program and erase. With the advent of electrically erasable PROMs (EEPROMs) in the last three years, however, there is an alternative. With prices that are following the traditional semiconductor learning curve, these EEPROMs will be much more common in the years to come.



Sam Bassett
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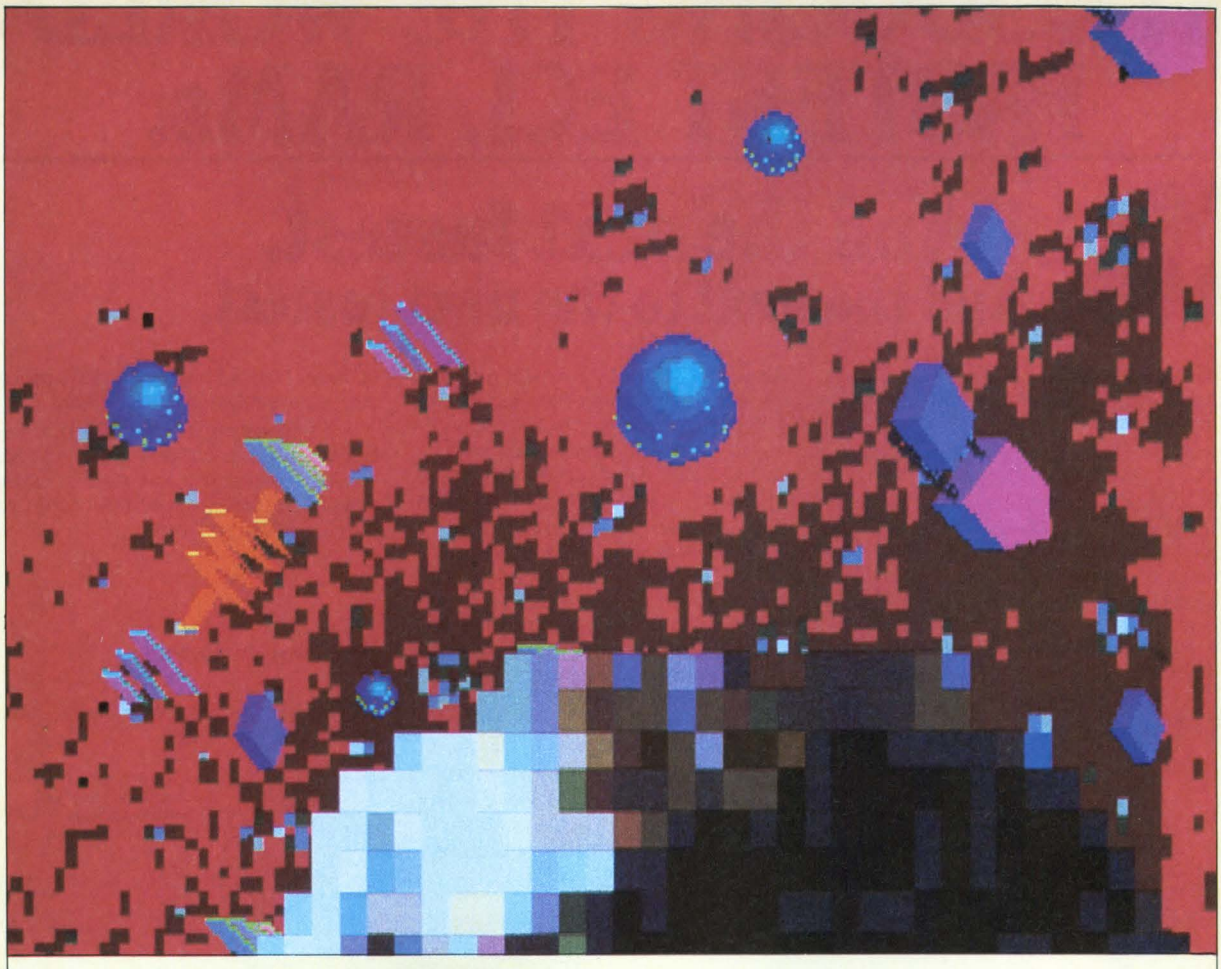
CIRCLE 82



Special report on semiconductor memories

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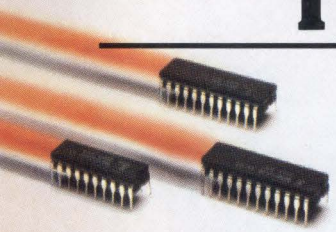

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CIRCLE 83

NONVOLATILE CHIP MENU GROWS TO SUIT VARIOUS APPLICATIONS

Matching devices and applications is not as simple as it used to be. New technologies and increased capacity in nonvolatile memories give designers wide freedom of choice.

by Rob Mortonson, Contributing Editor, and Sam Bassett, Field Editor

Designers trying to match their application requirements to available solid state, nonvolatile memories will find a greater choice of varieties and vendors. From read only and programmable read only memories to the frequent read/write NOVRAM, manufacturers are offering devices to meet the present needs of an array of applications.

Inevitably, there is some overlapping of functions between devices as well as occasional jousting for sockets. Nevertheless, each nonvolatile device type has an application area all its own. What have been changing are the characteristics of those exclusive areas. For example, the minimum volumes for read only memories (ROMs) and maximum volumes for erasable programmable ROMs (EPROMs) are continuing to rise.

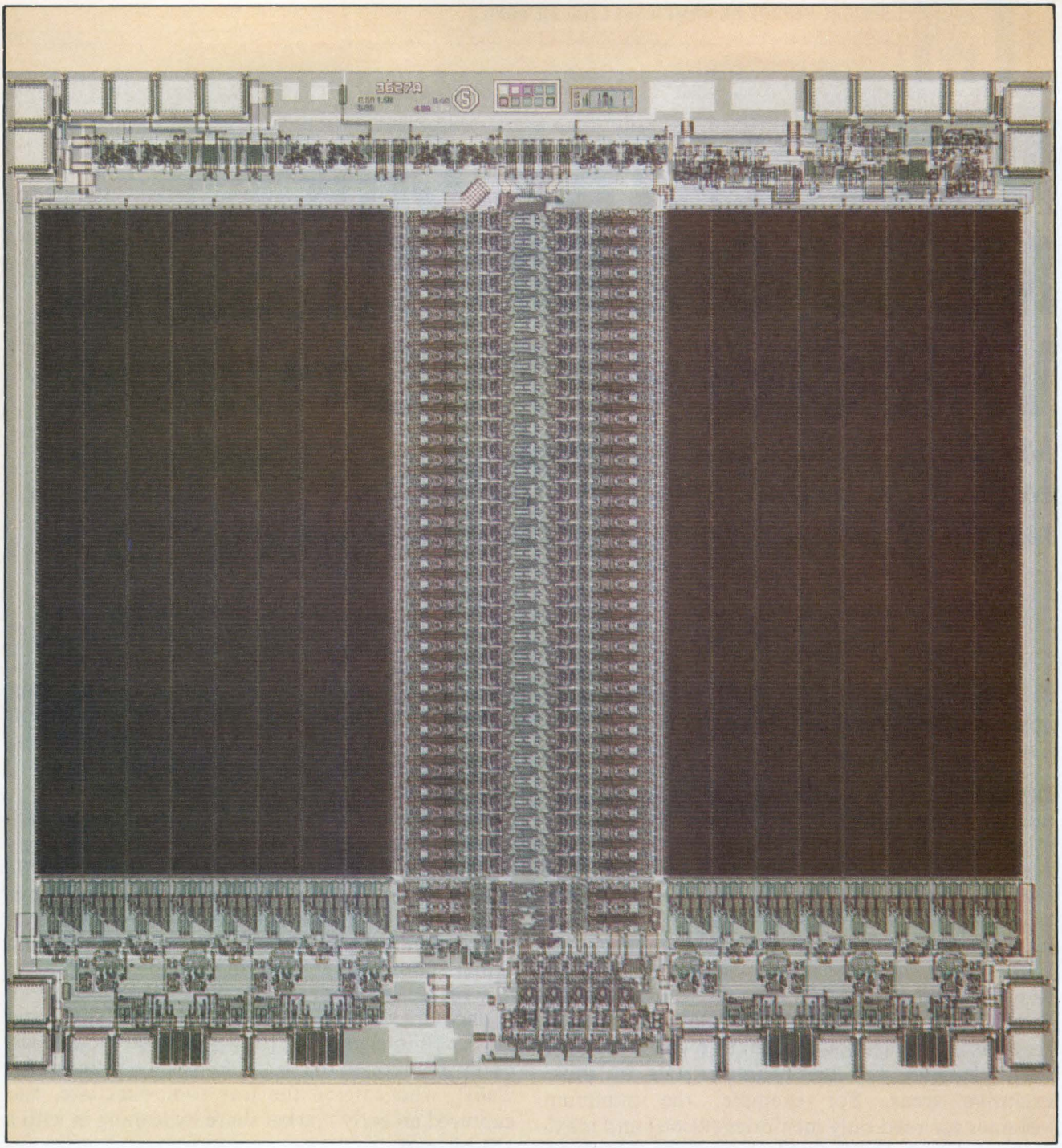
Simple economics has kept electrically erasable PROMs (EEPROMs) from breathing too heavily down the neck of EPROMs. There appears to be a 2 to 2.5 premium factor in their relative price per bit which, of course, favors EPROMs. Nevertheless, where in-system reprogramming is critical to an application, EEPROM has either carved out a unique socket opportunity or eliminated EPROM from consideration.

The very high price per bit premium for nonvolatile random access memories, or NOVRAMs, keeps them from threatening voltaile RAM devices supported by battery backup. This application, however, appears to be the primary one for these components. So far, the use of these components has been confined to applications where battery backup is unacceptable or where the amount of storage is critical yet small.

Although not a semiconductor technology, bubble memories are solid state and packaged in a way that makes them alternatives to other nonvolatile chips for certain applications. After a clamorous beginning with many vendors announcing impending design efforts, the bubble went through a rather severe shakeout during which such notables as Texas Instruments (Dallas, Tex), National Semiconductor Corp (Santa Clara, Calif), and Rockwell International (Newport Beach, Calif) virtually abandoned the technology. Intel (Sunnyvale, Calif), who entered the fray somewhat late, had captured an early market share by leaping in with a 1M-bit part.

Today, the domestic bubble market is served by Intel and Motorola (Austin, Tex). A recent agreement between the two giants has Motorola in lockstep with Intel on technology and packaging. Fujitsu Microelectronics, Inc (Santa Clara, Calif) and Hitachi America, Ltd (San Jose, Calif) are also mounting a bubble effort. Unlike Intel and Motorola, who appear to be playing a component-level strategy, the two Japanese manufacturers have concentrated so far on bubble boards and cassettes.

Originally, bubbles were used for mass storage-like functions in harsh environments. Their inherent



With the peripheral control circuitry implemented in CMOS, Signetics' 64K EPROMs are both fast and economical on power. These products are the first fruits of Signetics' highly automated Albuquerque fabrication plant.

immunity to shock, heat, and contaminants made them the only alternative in areas that would have proven catastrophic for rotating mass storage systems. However, a new niche has appeared for these high density memories. More computer manufacturers are putting them in portable computers as a form of working storage—that is, a selective group of records and files gleaned from a master storage system and carried along with the portable computer. Systems from Grid Systems Corp (Mountain View, Calif) and Teleram Communications Corp (White Plains, NY) have already proven the efficacy of this procedure. Fujitsu has recently announced a personal computer—the BC—that uses bubble cassettes for the same purpose.

In each of these six nonvolatile product areas—ROMs, PROMs, EPROMs, EEPROMs, NOVRAMs, and bubbles—manufacturers have announced new products. Some products feature higher capacity, faster speeds, or more flexibility through onchip functions. Some are the result of technological innovations. Others are combinations of several of these

characteristics. The trends in these six areas are important to consider because they will affect design decisions and selection criteria of devices in future products.

ROMs: bigger, cheaper, faster

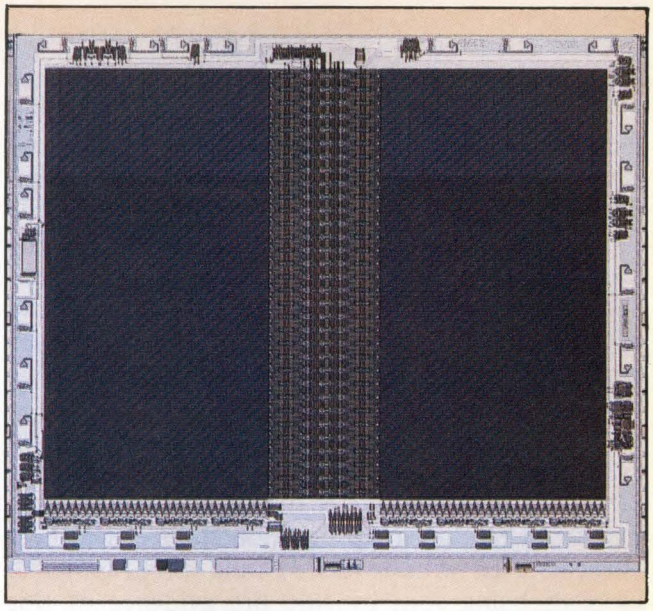
There are quite a few 256K ROMs available now, but NEC's (Natick, Mass) Electronic Arrays have a 1M-bit complementary metal oxide semiconductor (CMOS) ROM. These devices can accommodate twice the number of bits that are directly addressable by most 8-bit microprocessors. However, access time is a slow 5 μs. Thus, for most of today's ROM applications, the current crop of 256K chips have the leading edge. The fastest appear to be Synertek's (Santa Clara, Calif) 200-ns version of its SY23256 and Signetics' (Sunnyvale, Calif) 23256A, operating at the same speed.

Others start at 250 ns, and all companies offer slower, cheaper versions for applications that are more cost- than speed-sensitive. Synertek is working on a CMOS 64K chip and Motorola is reputed to be developing a 256K device. Speeds and power dissipations for these devices are not yet definite. Synertek makes a smaller, faster ROM family—the SY3316—with 80-ns access times and a latched ROM version aimed at use in pipelined bit-slice architectures, according to Chris Peterson, strategic marketing manager for Synertek's memory products.

Technologically speaking, most ROMs are still built using N-channel technology in the matrix or NOR configuration. Manufacturers create a fabrication mask from the data tapes given them by customers. Where the bit should be a logic one, nothing is done to create an active device and the voltage level remains high at the output. Conversely, a logic zero is implemented by creating a thin oxide active device that is in an "on" state when selected and shows an output zero voltage level. The mask determines the locations of these active devices in accordance with the tape's program data.

CMOS ROMs are also being developed. Here, one uses p-channel and N-channel device pairs to form simple logic gates for the peripheral decode circuitry. Only during transitions from one state to another is appreciable current drawn. Thus, a CMOS device consumes less power than an equivalent N-channel only type.

Without question, the largest market for ROMs continues to be in game modules or TV game cartridge applications. The game's program is stored indelibly in ROM, which is packaged in a plastic container with an edge connector. Inserted into a microprocessor based game, the ROM program determines such things as screen format, scoring, and sound effects. The actual game dynamics are the result of the processor sampling the game controller position, firing button, and image position



Synertek's SY23256 256K ROM represents the most advanced technology in commercially available ROMs. The 32K x 8 memory offers 200-ns access speeds.

data, which are dynamically written and read in RAM chips contained within the game system itself.

The second largest application area is in program memory for general purpose microprocessor based systems. With capacities topping 256K, ROMs can store whole language compilers and operating system software. For systems such as word processors that are used primarily for one application but can also be used for others, a ROM can be used to store the word processor application and operating software. Thus, users do not have to load a diskette each time the system is powered-up. For other applications, the ROM could be deselected and an appropriate program could then be loaded into RAM from diskette.

ROMs promise to continue being the lowest cost read only memory; the trade-offs are masking charges and lead times. Lead times can be as short as 3 weeks for prototypes, but 8 to 12 weeks appear to be the norm for production quantities.

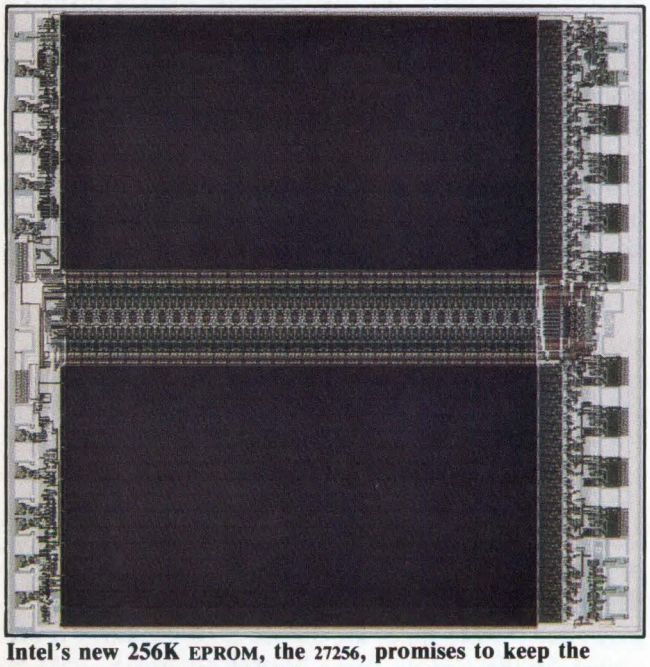
Mask charges are the tooling costs passed on to the customer; they are one way for ROM manufacturers to ensure adequate volumes and margins. At certain minimum volumes (usually negotiable), these charges tend to disappear. These charges also tend to shift lower volume orders to other alternatives such as EPROMs. Most ROM makers balk at requests to quote prices. The standard response is, "It depends on quantity and delivery expectations." Mostek (Carrollton, Tex) volunteered that the price per bit for its 256K device in 100 quantities is about $0.004. How one chooses to use a ROM is critical in taking advantage of its inherently low cost. If the program to be stored is subject to change even once, ROM may not be the most economical approach.

EPROMs: fewer users care about the "E"

More and more designers are putting EPROMs into sockets once reserved for ROMs. The reason is simple: their once-high premium has melted away. Coupled with EPROM's user programmable abilities and increasing capacities and speeds, the more favorable EPROM prices have had a significant effect on the memory's application niche. Originally, the erasable feature made them attractive for very low volume and prototype development because they were easily modified and could be purchased in low volumes without a mask charge penalty.

Today, it appears that most EPROMs are used in ROM applications that are too low in volume for ROM or that require faster turnaround. In essence, like the ROM, they are programmed once and never altered. The windowless, 1-time programmable EPROMs being sold by NEC are evidence of this fact. By putting the EPROMs in plastic rather than ceramic packages, and by programming them once, they really become MOS PROMs. The advantages are lower cost compared with EPROMs and faster turnaround than with ROMs.

It is interesting how quickly the EPROM manufacturers have scrambled after the ROM market. In the past, it was not unusual to have a 2-year gap between a ROM introduction and that of a comparably large EPROM. Today that gap has narrowed to less than a year. In fact, Intel's 27256, a 256K EPROM, was introduced only about six months after the 256K ROMs were.



Intel's new 256K EPROM, the 27256, promises to keep the flames of competition high between ROMs and EPROMs. Its introduction occurred only six months after the announcements of 256K ROMs. The new chip's die is 15% smaller than the 27128, 128K EPROM's die. The chips are being selected for access speeds between 450 and 200 ns.

A lot has happened since Dov Frohman-Bentchkowsky developed the floating-gate avalanche-injection MOS transistor (FAMOS) and with it the erasable PROM technology (see Panel, "Floating gates: the common link"). In addition to Intel's 256K device, there are several 128K chips in or soon to be in circulation from Seeq Technology (San Jose, Calif), Intel, Mitsubishi Electronics America, Inc (Sunnyvale, Calif), Toshiba America, Inc (Tustin, Calif), Hitachi, Fujitsu, and Oki Semiconductor (Santa Clara, Calif).

The bulk of the EPROM business is in the 64K area. The industry standard 2764 is available in a variety of speeds and power consumptions. The majority of devices offer speeds from 450 ns down to 200 ns. Typically, I_{CC} specifications are 135 to 150 mA. NEC claims the low power NMOS prize with a 64K part that consumes only 80 mA.

For really low power 64K applications, Fujitsu announced a CMOS part with 40-mA active and 1.1-mA standby current ratings. Signetics is reportedly working on 64K and 128K CMOS EPROMs at its new, highly automated, Albuquerque fabrication plant. Rumor has it that the parts will be 30-mA devices with less than 100-ns access times. National Semiconductor has already staked its claim in the CMOS EPROM territory. The company offers a 16K and a 32K part. Both parts offer 53-mW active power (about 11-mA I_{CC}) and 5.3-mW standby. The 32K NMC 27C32 has a 350-ns version, and both parts come in 450-, 550-, and 650-ns versions. National Semiconductor is planning to sample a 256K CMOS part by year's end.

Device scaling allows rapid capacity and speed increases. Intel's 256K has cell sizes of only 36 square microns compared to 108 for its 2764. With the variety of EPROMs in N-channel MOS (NMOS) and CMOS, plus capacities from 16K to 256K, it would seem likely that EPROMs will push even harder against ROMs in many applications. Interestingly, the EPROM memory market is still dominated by U.S. manufacturers, unlike the volatile memory market where Japan has garnered major shares in the higher capacities. Domestic manufacturers enjoy a 56% share of the 32K EPROM market and about a 95% share of the 64K market, according to Dataquest (Cupertino, Calif), a respected market analysis firm.

EEPROMs: the benefit of in-system programming

The close relationship between EEPROMs and EPROMs is apparent as soon as one looks at a diagram of the cell structure (see Panel). The floating-gate tunnel oxide structure (called FLOTOX by Intel) permits writing and erasing by having electrons move through potential barriers onto the

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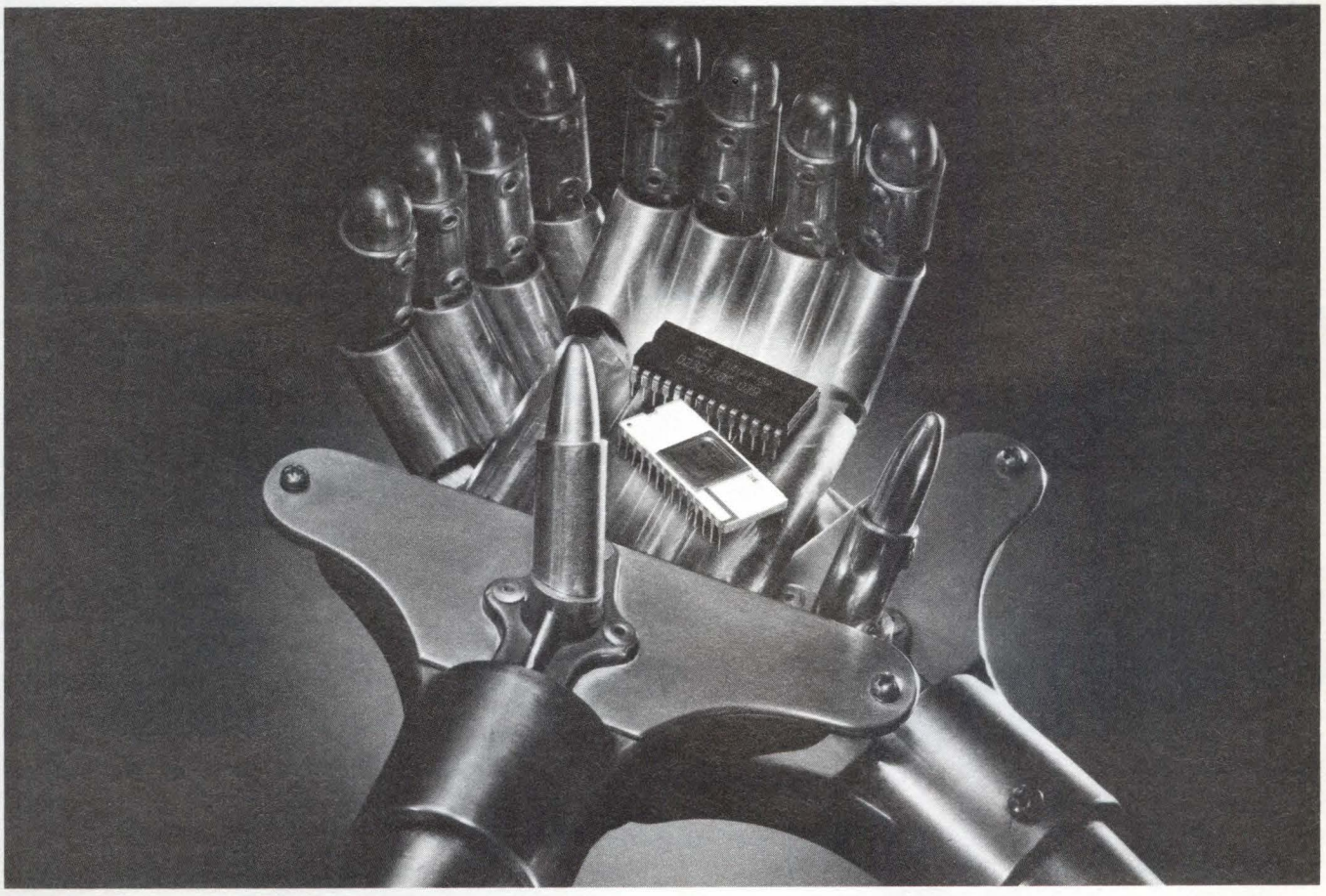


CIRCLE 84

Floating gates: the common link

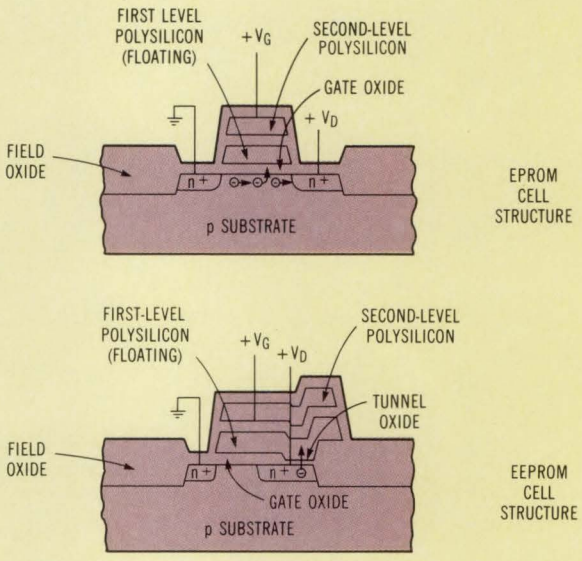
EPROMs and certain EEPROMs have a lot in common. In 1971, Dov Frohman-Bentchkowsky developed the floating-gate avalanche-injection MOS transistor (see Figure). This transistor has the gate surrounded completely by a silicon-dioxide insulator and injects high energy electrons into it from either gate or source. The electron energy levels are created by elevated electric fields in the channel, enabling the electrons to jump the energy barrier posed by the silicon/silicon dioxide junction between the substrate and the gate dielectric.

Once the electrons penetrate the gate oxide, they are drawn by electrostatic attraction to the floating gate, which has been capacitively coupled with a positive bias on the gate above it. Once sufficient electrons are collected on the floating gate and the threshold voltage is elevated to the point where the device channel conducts, that cell is "programmed."

To erase the cell, the floating gate's electrons must be subjected to collisions with high energy ultraviolet photons. As the electrons absorb energy from these collisions, they can traverse the barrier and make their way back to the substrate.

The floating-gate tunnel oxide EEPROM process uses a similar floating-gate structure. However, a thin tunnel oxide is created that allows electrons to tunnel in accordance with the Fowler-Nordheim tunneling mechanism. Again, these electrons are collected on the floating gate and, ultimately, conduction is induced in the channel. To erase this cell, the drain is held positive while the gate is grounded, thereby reversing the tunneling process and removing the electrons from the floating gate.

Because of the thin oxide (less than 200 Å thick), there are two factors involved in EEPROMs: endurance, or the number of times the cell can be programmed and erased, and retention, or the length of time that the number of electrons remains high enough to ensure adequate threshold potential.



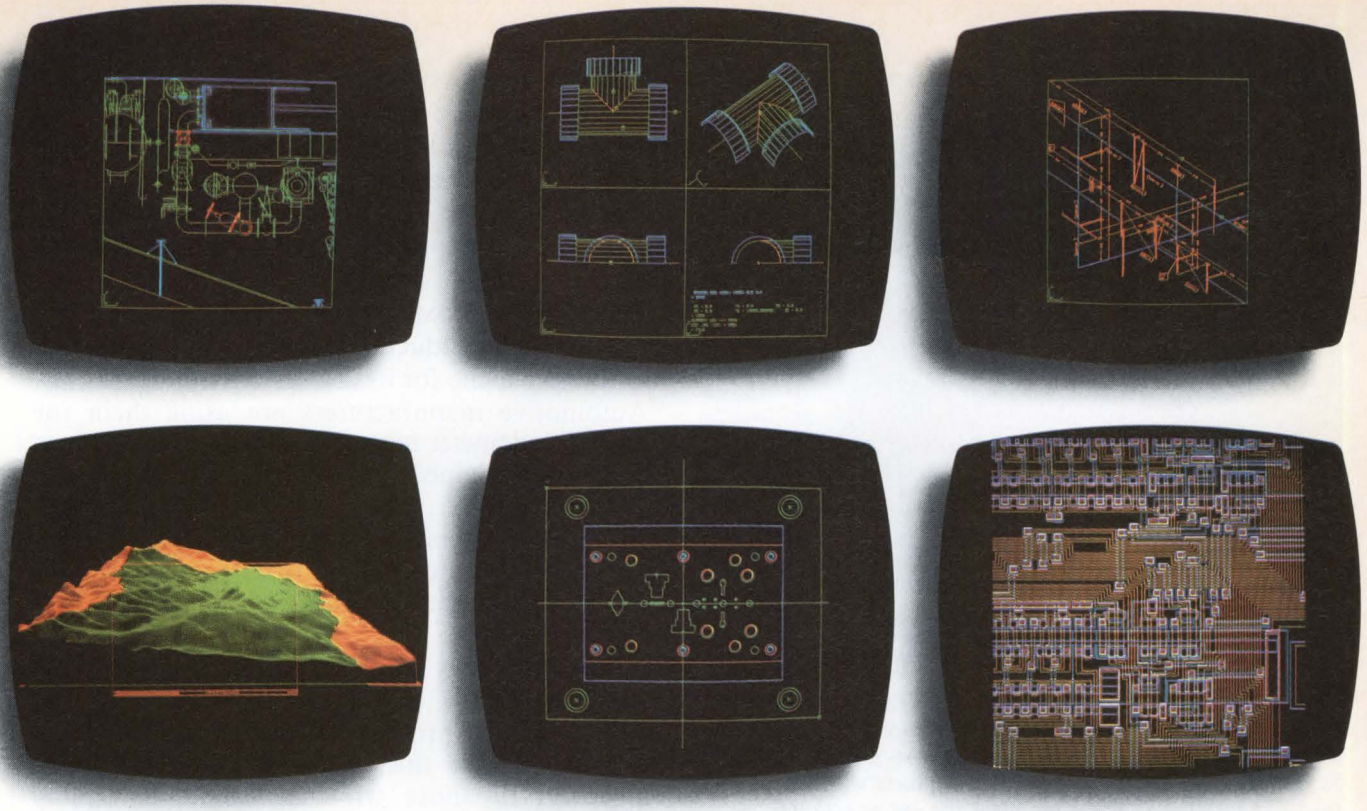
Most EEPROMs exhibit about 10-year retentivity. Testing indicates that it is possible to achieve that retention level even at temperatures above 125°C. As for endurance, most devices can undergo from 10k to 1M program/erase cycles without threshold voltages varying beyond tolerance limits.

floating gate, much as it is done with EPROMs. The major difference between the two methods is that both erasing, which is normally done by ultraviolet light, and writing can be done electrically as with EPROMs. This method makes it practical to program and erase the EEPROM without removing it from its socket.

The older EEPROM technology, metal nitride oxide semiconductor (MNOS), traps electrons at the oxide junction. Proponents of this technology point to the success of new parts using an N-channel version called silicon nitride oxide semiconductor (SNOS). Inmos (Colorado Springs, Colo) is one company that has produced a 64K device using this technology. Those who favor FLOTOX say that MNOS and its derivatives are not as scalable. For the time being, certainly, both technologies are thriving.

EEPROMs appear to be at the same evolutionary point as were early EPROMs. That is, the technology has been accepted but the architectural details and product features still need to be settled on. At the 64K level, indications are that Intel and National Semiconductor will follow Xicor, Inc (Milpitas, Calif) and offer products that are largely compatible with other memories. These will be self-timed, 5-V only devices with onchip latches; they can be connected to a conventional memory bus without creating havoc due to unfamiliar waveform timing requirements, according to Richard Orlando, product marketing manager at Xicor.

In fact, Xicor has already announced its 64K, as has Hitachi. National Semiconductor is rumored to be moving faster than expected, and may be bypassing its NMC 98C32 32K CMOS product by



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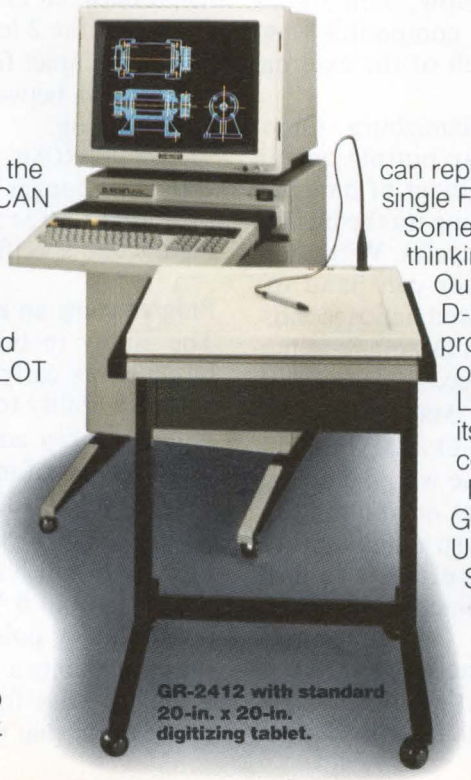

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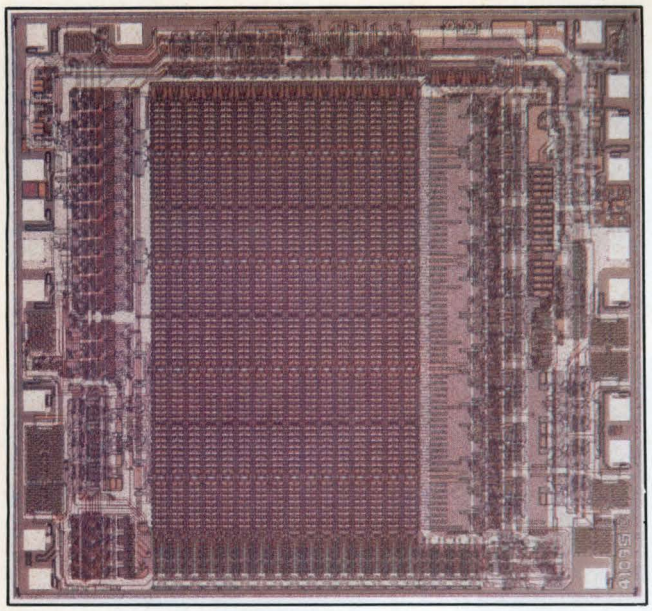

Synertek's 256 x 8 EEPROM represents a different trend for these products. Whereas many manufacturers are pushing to higher capacities with conventional EPROM- and ROM-like EEPROMs, some are making smaller products with I/O port-like interfaces. These are ideal for use as external memories, since single-chip microcomputers interface more easily with them than with conventional memories.

announcing a 64K product instead. As with other CMOS memories, the cell array is done using N-channel floating gate but the peripheral circuitry is done in CMOS, according to Drew Osterman, the company's MOS memory marketing manager.

The first 16K EEPROM was Intel's 2816. It required both higher voltage and external wave shaping for programming and erasing. Its look-alikes, too, required external support. Now, with Intel's 2817A, National Semiconductor's compatible NMC 9817, and other compatibles, much of the external circuitry has been put onchip.

Larger devices, like NCR's (Miamisburg, Ohio) 32K 52832 and Inmos' IMS 3630, are putting onchip latches on the die so that several bytes of data can be shifted in quickly without holding up the bus for the typical 10-ms write and erase cycles. With these onchip latches, the microprocessor can hand off the data to the chip in a few hundred nanoseconds, freeing the bus to do other things. Dramatic reductions in programming time are accomplished with this method. For example, in the IMS 3630, it could take 83 s to fully program a 64K EEPROM, but with the chip's 64 bytes of registers, the whole chip can be programmed in only 128 cycles or about 1.2 s, according to Fred Jones, Inmos' strategic marketing manager for memories. "The effect is to have our 3630 behave much like an edge-activated RAM," Jones said.

Whereas some EEPROM manufacturers are keeping one step behind the capacities of EPROMs, others are opting to produce smaller parts. General Instruments (Hicksville, NY) makes the ER5901, a byte-wide 128- x 8-bit device, and also a 16 x 16 serial device. The first device finds much use as a DIP-switch replacement in terminals and other systems, and the serial device finds use as a memory device in stereo receiver and TV receiver electronic tuning, according to Mort Kalet, the company's EEPROM product marketing manager. National Semiconductor is another company that has found a niche for its 256- and 1K-bit EEPROMs. "Automotive manufacturers are using them for electronic odometer memories," marketing manager Osterman explained. Interest in National Semiconductor's 8-pin, mini-DIP EEPROMs for automotive odometers is growing domestically as well as overseas, according to Osterman. NCR is another vendor that produces and markets a 16 x 16 serial EEPROM.

Seeq Technology announced a family of EEPROMs that includes a 16K, a 32K, and a 64K part that Ken Kwong, memory products marketing manager, says will be available this year. Kwong is the most outspoken of those who see EEPROMs rapidly pushing EPROMs to the wall in terms of price. "The major cost factors are die size and testing," Kwong explained. Testing costs for EEPROMs could fall below those for EPROMs because of the more favorable write and erase speeds. Kwong claimed that Seeq's use of innovative metal line plasma etching has helped to scale EPROMs down from the more typical 10 microns to 6 microns. As a result, said Kwong, Seeq is producing 64K dies that are actually smaller than 64K EPROM dies.

Others are more reluctant to prophesy a major collision between EPROMs and EEPROMs. The consensus is that the 2 to 2.5 price premium per bit is likely to remain intact for a while longer, ensuring that the competition between the two remains more frictional than head-on.

Like EPROMs, EEPROMs are being read with 200-ns or longer cycles. One notable exception is Motorola's MCM 2832, which has a 150-ns maximum read access specification.

Programming: an issue with EPROM and EEPROM

The ability to both program and erase an EPROM hastened its early popularity. This quality, coupled with the ability to perform these tasks in-system, is EEPROM's key advantage. However, manufacturers of both types of memory are concerned with shortening the time it takes to program their devices.

Intel described a method for programming EPROMs in which a 1-ms pulse is applied while the V_{CC} level is held to 6 V. (Traditionally, a nominal 50-ms programming pulse is used for each cell.) As soon as the cell exhibits a one-to-zero transition, it is hit with a longer pulse four times the total of the sum of pulses up to that point. Thus, if the transition occurs

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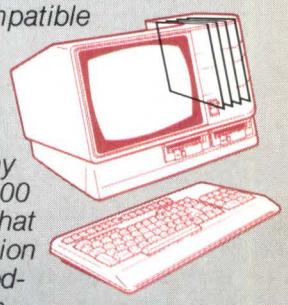

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CIRCLE 86

after two pulses, another pulse 8 ms long is used and the cell is adequately programmed in about 10 instead of 50 ms.

The scheme allows up to 15 pulses before the cell is declared faulty. Thus, cell programming could take as long as 60 ms. However, according to Intel's Don Knowlton, 5- or 10-ms programming is much more the norm. Called "intelligent programming algorithm," the process can be used on any manufacturer's EPROMs. PROM programmer manufacturers Data I/O Corp (Issaquah, Wash) and Pro-Log Corp (Monterey, Calif) are incorporating such algorithms in their systems' hardware and software.

Other methods for speeding up programming are gang programming of two or more EPROMs and special chip control lines that allow several cells to be tested at once. Many manufacturers are adopting such innovative techniques to speed up EPROM testing in order to better control production costs.

Bipolar PROMs cannot be beaten for applications requiring speed.

As already mentioned, many of the newer EEPROM products have onchip latches. These latches permit several bytes of data to be loaded quickly into the latches, then to be written internally to the EEPROM array, which is isolated from further bus activity. In addition, NCR and Inmos permit the actual voltage thresholds to be determined both during manufacture and later while the parts are in a system. From those data, storage retentivity can be calculated and, if necessary, the device can be quickly reprogrammed to avoid potential loss of data at some later time.

Another EEPROM feature that could increase programming speed is a bulk chip erase function. There is some difference of opinion, however, in the practicality of that function. Xicor's Orlando feels that some users see chip erase as a threat. "Some found out early that depending on how they socketed their EEPROMs, they could accidentally erase the first byte on power-up," Orlando explained. "The prospect of wiping out the whole chip's memory by mistake is even more intimidating." Hence, chip erase is not a feature on Xicor's X2864A.

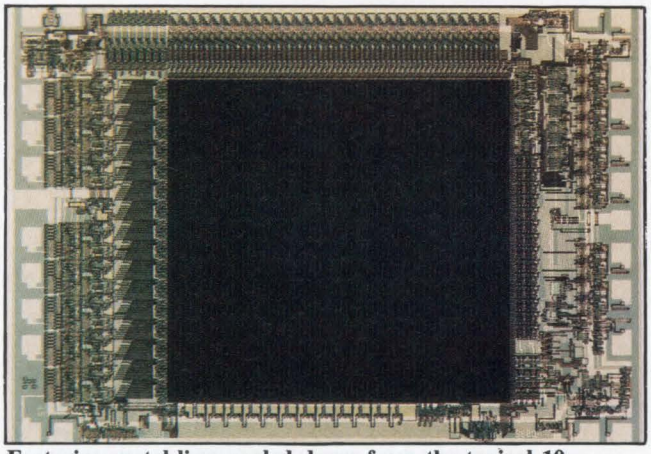
RAM chips, the proverbial scratchpads of a computer, are rapid read/write memories and are used for very temporary storage of interim data. However, when the power goes down, unless the RAMs are backed up by batteries, the chips develop amnesia and the data go away. Elaborate approaches to quickly dumping RAM storage to disk upon sensing a drop in supply voltage have been tried, but the fear of losing important data from volatile memories still looms large in the hearts and minds of computer users.

CMOS RAMs with battery backup are a simple way to ensure against such data losses. However, for remote systems in facilities where personnel cannot visit very often to check on the batteries' health, the risks increase. Enter the NOVRAM, typically a static RAM with an EEPROM shadow. In most cases, the chip behaves like a static RAM, but upon power-down, it stores its data in EEPROM. If NOVRAMs were priced only slightly higher than RAMs and batteries, one would expect a wholesale shift to NOVRAMs for such applications. However, right now, NOVRAMs are expensive. One reason is that they encompass a fairly recent technology. Another reason is that the one-for-one memory redundancy is a glutton for silicon die area.

Xicor established the NOVRAM concept with its 4-bit wide family, including the X2210 and X2212, 64 x 4 and 256 x 4 chips, respectively. It has since developed 8-bit wide 1K, 2K, and 4K parts, the 2001, 2002, and 2004. NCR has mirrored the Xicor line with its own 4- and 8-bit products fabricated in SNOS and NMOS. Except for the prefix 5, the part numbers are identical (eg, 52210, 52212, and so on). NCR also makes a 128 x 4 52211, a chip that Xicor does not make.

General Instruments has announced its 4K ER5304, but the product appears to be on the back burner since the company's attention is mainly focused on its EEPROM products. Intel, too, will join the select club of NOVRAM makers when it introduces its own 4K device. Intel's part, like those of NCR, is reputed to have automatic power-up recall. This feature provides automatic copying of the EEPROM data to the RAM upon power-up.

As battery-backed-up RAMs are serving applications, NOVRAMs are also being used (like some EEPROMs) for DIP switch replacement in terminals and other peripheral systems. Xicor also makes a 16 x 16 serial device, the X2444, which it says is a



Featuring metal lines scaled down from the typical 10 microns to only 6 microns, Seeq Technology's 52B13 16K EEPROM enjoys a die size comparable to similar capacity EPROMs. This EEPROM is said to actually have a smaller die than the company's own 64K EPROM.

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fine companion for single-chip microcomputers. Unlike microprocessors that are designed for external memory interface, single-chip devices deal with the outside world through ports. According to Xicor's Orlando, a serial device like the 2444 is a good fit with the port interface architecture. He feels that using a separate microcomputer chip plus a small NOVRAM is a far better solution than making a monolithic single-chip with onboard EEPROM as Seeq Technology is doing. Said Orlando, "It's a lot cheaper to use a $2 single chip and a $2 NOVRAM than to pay $30 for a monolithic." One can see how Xicor prices its serial device.

Bubbles were once touted as the be-all and end-all of memory technology.

As for other devices, the 100-piece price quotes for NCR's line are $5.50, $8, and $12 in ascending order of capacity for its 4-bit wide parts; and $16, $28, and $61 for the byte-wides. The premium for NOVRAM is glaring when one considers paying $61 for a 1K part!

As long as the preferred device continues to be a 6-transistor static RAM cell coupled one-for-one with either floating-gate or SNOS EEPROM cells, price reductions due to smaller dies will be slow in coming and not very dramatic. However, in a recent International Electronic Devices Meeting (IEDM) paper, Mostek's D. Guterman suggests using a single transistor dynamic RAM cell tied to a small EEPROM cell made using a vertically integrated triple-polysilicon process. The end result is a 1.5-mil^2 cell. This method could lead to future higher density, lower cost NOVRAMs.

Bipolar PROMs: the niche still exists

Remember bipolar PROMs? They are still around and cannot be beaten for applications requiring speed. The biggest, the Fujitsu 7143, is just 64K, but read access is a rapid 55 ns. This PROM was built using diffused eutectic aluminum vertical fuses. Unlike the surface-level, horizontal fusible links in other PROMs, these links are subsurface. According to Allen Hu, product marketing manager for bipolar PROMs, fusing the links will not rupture the passivation layers.

Signetics is now announcing a 32K 80-ns part using its nichrome fuse technology. However, Signetics' Geoff Dyer said that faster parts are in the works. He explains that these parts will obtain the higher speed by switching from junction isolation to oxide isolation with a technology called avalanche-induced migration (AIM). Signetics is expected to announce a 16K with speeds down to 30 ns or better. And, by November, it expects to have a 32K in the new technology with twice the speed of the current one.

Harris (Melbourne, Fla) is another 64K PROM vendor, but the main business still seems to be with 16Ks and 32Ks. National Semiconductor's DM87S321 is a 55-ns 32K device; Monolithic Memories (Sunnyvale, Calif) makes one specified at 50 ns. These devices obviously do not compete with 200-ns EPROMs for sockets. In fact, the largest application continues to be in program and control store, particularly in bit-slice processor based systems.

System pipelining is an approach in which a processor overlaps operational cycles. For example, the processor may be fetching the next instruction while it accesses the preceding data and executes the instruction before that one. Some manufacturers, National Semiconductor for one, are putting registers in their PROMs to support such pipelined architectures. In essence, the data in the first location are latched in the register while the PROM is already setting up the next data word.

Monolithic Memories, which has been steadfastly committed to bipolar technology with PROMs as a major part of its business, is not rushing to a 64K part. When asked why, Dan Medler, product marketing manager, answered that demand for that part has not become widespread. He sees the part as attractive primarily to the military at this time. Fujitsu's Allen Hu confirmed that view by estimating that more than 50% of his company's 64K business is for military applications.

Bubbles: still floating, not bursting

Bubbles are an interesting technology. They have been included in this article because, like the others, they are solid state, nonvolatile memories. Unlike other memories, they do not use semiconductors. Instead, they are a magnetic technology most similar in concept to Core memory. Core, like the vacuum tube, has largely been displaced by semiconductor memories, but the bubble continues to control certain application areas.

Historically, bubble technology was pioneered at Bell Laboratories (Short Hills, NJ). Early proponents of the concept were Texas Instruments and Rockwell. A bit later, National Semiconductor announced a research and development effort aimed at producing bubble products. One of the last domestic manufacturers to try its hand at bubbles was Intel. But Intel entered tumultuously by starting at the 1M-bit level and truly leapfrogging its competitors.

For users, bubbles were an enigma. Engineers versed in 5-V square wave pulses were now faced with triangle current pulses and strange timings. Those manufacturers who offered a bubble chip and left the interface and control details to the

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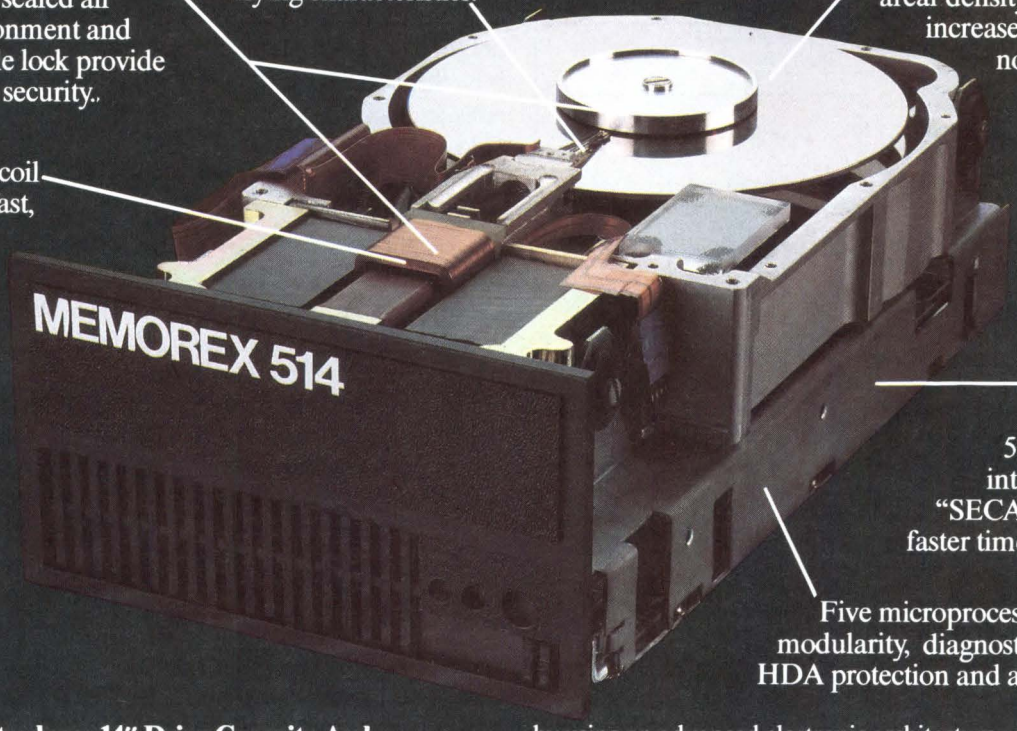

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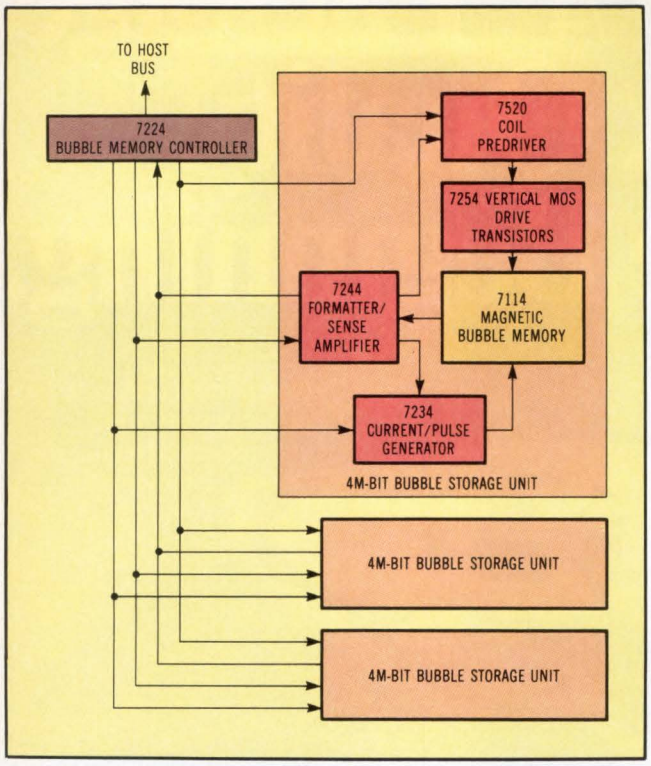

It takes only five support chips to interface a microprocessor to Intel's 4M-bit bubble memory. The host bus is tied to the 7224 bubble memory controller and the host treats the entire subsystem as a typical I/O subsystem. All pulse shaping and timing is handled by the support integrated circuits.

designer found a largely unresponsive audience. Perhaps, thorough planning, hindsight, or both led Intel to announce its bubble chip with an array of support components that would simplify a designer's interface problem. In effect, the control complexity was designed into the support chips, leaving designers with a fairly straightforward peripheral-like interface.

In their early days, bubbles were touted as the be-all and end-all of memory technology. Visionaries saw bubbles cutting a swath through the likes of RAMs, ROMs, PROMs, and even disks. More sober outlooks had bubbles gaining a foothold in harsh environment system applications, increasing their share according to price and speed factors. Bubbles have, in fact, gained that foothold. They are used for storing operation programs for automated machinery and numerical control machines. Another demand just beginning to emerge is what some call "working storage," a kind of briefcase of the future. With a large market forecast for small, battery-operated portable computer workstations, bubbles offer a means to travel with much file storage in a relatively small volume.

A typical scenario has a user downloading from a data base the portions of files that he or she might need while traveling or while away from company headquarters. Of course, tape cassettes or flexible disks can be used for that purpose, too. However, bubbles are faster than both cassettes and disks and are very portable. As the number of portable systems grows, bubble use in portable applications will probably grow commensurately.

As for vendors, the original list of participants has dwindled considerably. Rockwell, Texas Instruments, Mitel Semiconductor (San Diego), and National Semiconductor have all moved on to other things, citing a variety of reasons for their respective decisions. Domestically, Intel and Motorola continue to build and sell bubble memories. Hitachi and Fujitsu make up the Asian vendor list.

Today's largest bubble is the Intel 7114, a 4M-bit device. Its architecture is very similar to that of the original 1M-bit 7110, but the number of its quads has doubled to eight and the number of bubble sites in each loop has also doubled to bring a fourfold capacity increase.

Intel is using X-ray lithography to achieve its submicron widths, but continues to use a 50-kHz field rotation rate. In addition to Intel's 1M-bit bubble, Fujitsu and Hitachi are also believed to be sampling their own 1M-bit parts. They, however, use a 100-kHz field rotation frequency and their parts, at 13 to 15 ms, operate faster than Intel's at 40 ms. The trade-off is that the Japanese-made products are not specified to the same upper temperature limits as the Intel parts are. Intel will guarantee operation at 70 °C, whereas Hitachi guarantees it at 60 °C and Fujitsu at 50 °C.

Motorola and Intel recently agreed to a second-sourcing arrangement whereby they will use the same technology and architecture plus compatible packaging. Both will probably continue to stress Intel's component-level strategy. In contrast, Fujitsu and Hitachi have emphasized a board-level and cassette-level marketing posture. They both offer bubble board products at the 1M-bit level that include the necessary support circuitry. Interestingly, both Fujitsu and Hitachi use far more support chips for their bubbles than do Intel and Motorola. Price competition is warming up, but with so few players, no one appears ready to sacrifice profits. Current prices on the street are about $200 to $300 per megabit in OEM quantity.

With the present state of the bubble market, the vendor list should remain stable. In the face of rapidly increasing markets such as that of working storage, others may again venture into bubble manufacturing. It is a safe bet that bubble prices will not fall dramatically—but fall they will.

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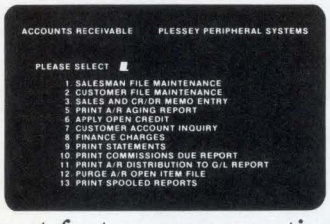

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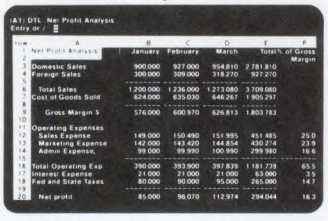

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CIRCLE 90

VIRTUAL MEMORY MANAGEMENT EXPANDS MICROPROCESSORS

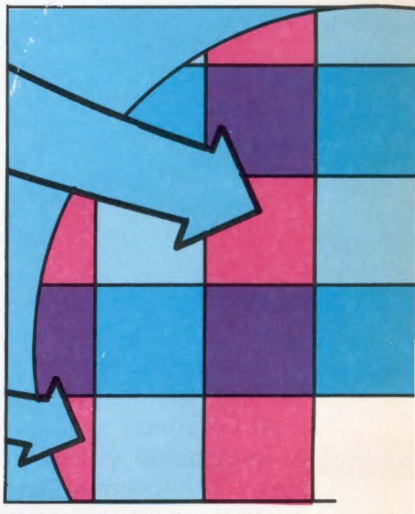
A memory management unit combines demand page swapping with onchip cache for a 124-bit virtual address space.

by Gary Martin

Virtual memory systems offer an appealing solution to the problem of limited memory capacity in microprocessors. Whereas the 64K-byte address space of a decade ago may have been adequate for applications of that time, today's multi-user, multiprogram environment requires a much larger address space than ever before.

There are several ways of designing a computer system that will handle the memory capacity needed in a large address space environment. The approach used by many mainframe manufacturers—to ship a full complement of physical memory with each system—does give the user enough memory to service the total address space potential of the host central processing unit (CPU), but it is very expensive.

The virtual memory approach is to divide the total memory into two parts: main memory directly accessed by the CPU, and peripheral memory (eg, disk) that complements main memory in providing the total address space. If designed correctly, this virtual memory is completely transparent to both programmer and user, who have the illusion of possessing more main memory than actually exists. A very sophisticated virtual memory system also offers user and memory protection, and a certain amount of debugging capability. What has made virtual memory systems so appealing, however, is that when properly designed, they offer an inexpensive way of obtaining large amounts of address space because of their use of low cost peripheral memory.



How virtual memory works

All of today's 8-bit devices are limited to a 64K-byte address range. With the advent of the 16-bit microprocessor, the user's address range expanded somewhat, with one manufacturer offering 1M-byte and others 24-bit (16M-byte) address ranges. With the introduction of National Semiconductor's NS16000 family, the available address range was extended to a full 16M-byte address space, but the new CPU can operate many times faster because it was designed with 32-bit registers, arithmetic logic units, and internal data paths.

Gary Martin is a systems development engineer for National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, where he is involved in technical marketing. Mr Martin holds a BS in computer science from The College of William and Mary, Williamsburg, VA.

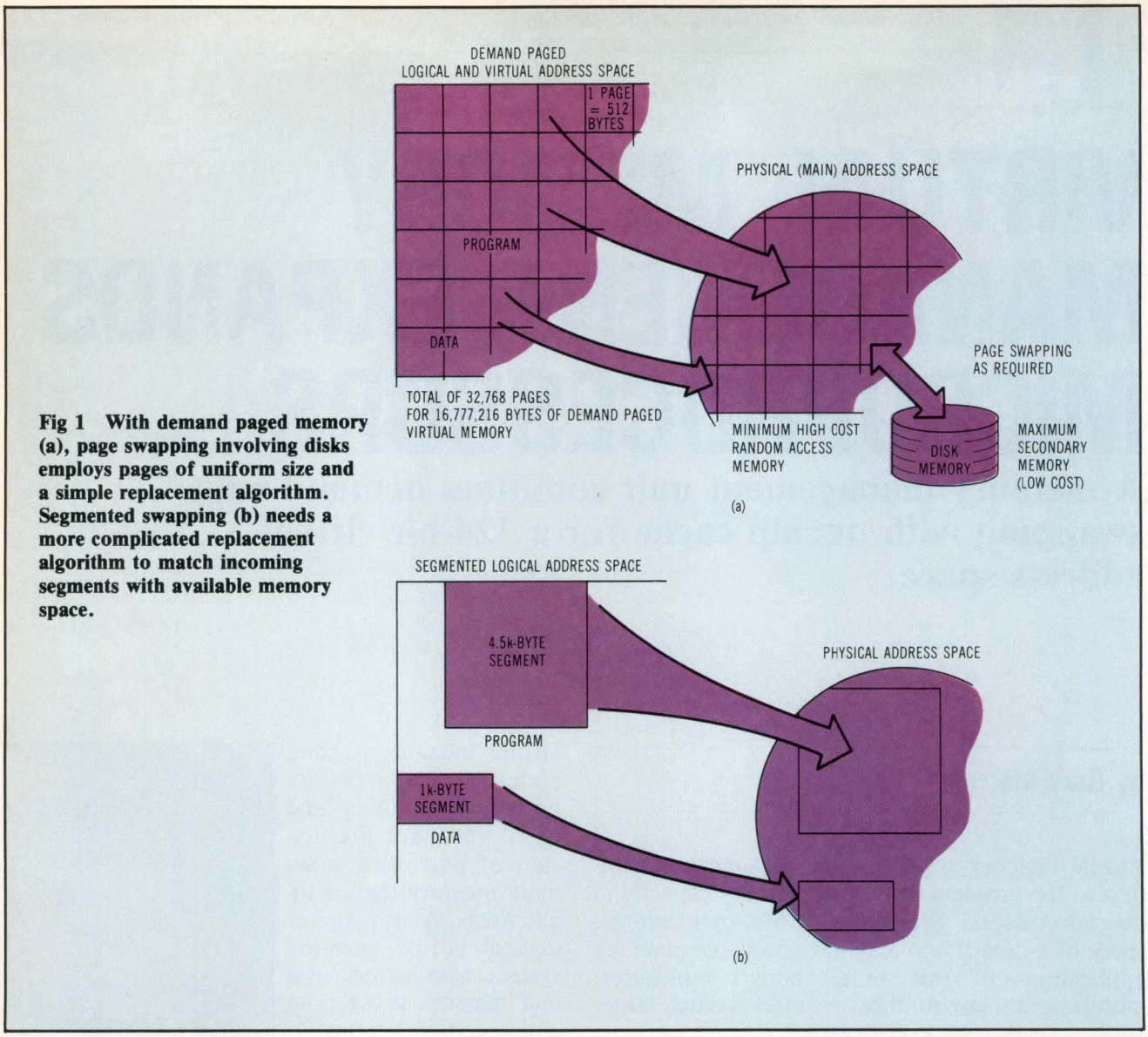


Fig 1 With demand paged memory (a), page swapping involving disks employs pages of uniform size and a simple replacement algorithm. Segmented swapping (b) needs a more complicated replacement algorithm to match incoming segments with available memory space.

For a large address space to be beneficial and still stay within the competitive price range of a small computer system, computer designers hope to implement virtual memory that, in essence, allows the original equipment manufacturer to combine primary storage (main memory) with secondary memory—such as disk—in such a way that memory management functions appear transparent to the user. In this way, extremely large operating system software and application programs can be used without the user having to worry about the system's hardware limitations.

In a virtual memory computer, the user's program only references virtual addresses, which are translated to physical addresses. Virtual addresses reside either in main memory, in which case the program continues normally, or in disk memory. If the referenced address is on disk, a user's program is suspended. A special system routine is called up that swaps the disk location with an unused main memory location. Once this routine is completed, the user's program is resumed. For maximum efficiency, locations that are likely to be referenced next are brought from disk into main memory at the same time.

Segmentation versus demand paging

The two predominant types of virtual memory used today are segmentation and demand paging (Fig 1). Demand paging—the basis of the company's NS16082 memory management unit (MMU)—is far more efficient and faster than the segmentation approach.

Segmentation divides the address space into a number of segments of varying length, each corresponding to specific programs or data. Segmentation's limitations emerge when attempting to allocate the main or disk memory resources. The minimum unit that can be swapped when using segmentation is the segment itself. This means that a segment must reside entirely in physical (main) memory or disk, and that there must be a contiguous hole large enough in main memory

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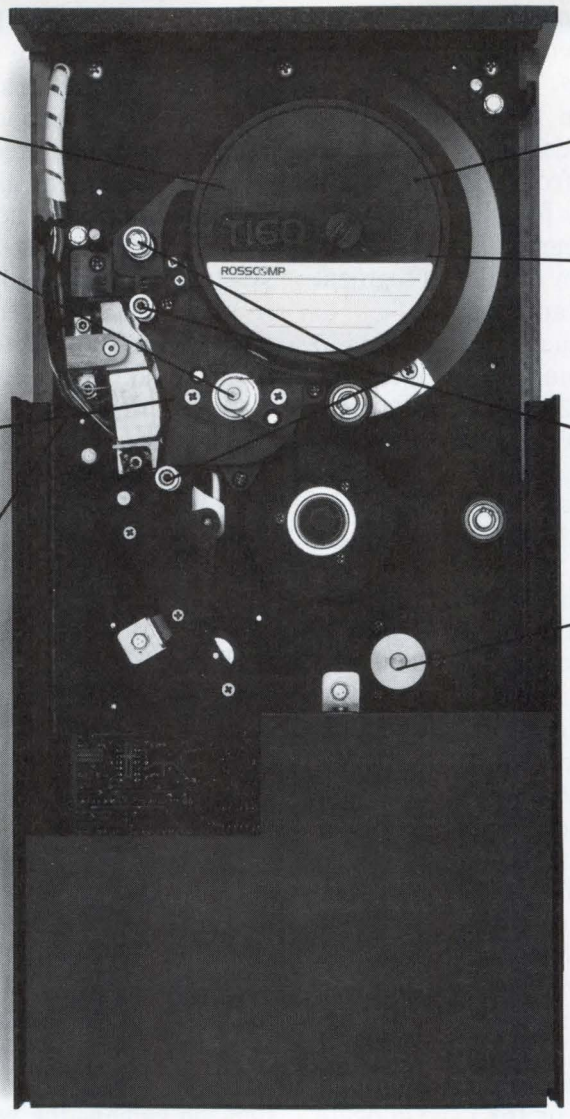

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whenever a segment is swapped in. If a large segment of data—about 100k bytes—has to be swapped out of main memory to make room for another segment that the program needs to continue, all 100k bytes must go, not just some. This not only ties up the system and local bus for the direct memory access transfer, but it demands higher disk drive transfer rates.

Other problems arise if, in the middle of an instruction, the program finds that the data it needs must first be swapped from disk into main memory. If there is no facility for abort and retry instructions, then all data segments must be in memory simultaneously. If they are not, a segment fault is detected and the program stops.

This is the primary reason such systems demand large amounts of main memory. Consider, for example, a program that is 20k bytes long with data tables of 100k bytes. Therefore, the minimum amount of main memory required each time that the program is loaded for execution is 120k bytes. Not many systems can afford that kind of main memory for several tasks.

Another major problem with some segmentation schemes involves the small number of segments that can be active at the same time and the granularity of protection. For instance, one manufacturer's MMU allows 32-segment descriptors to reside onboard for high speed translation. This may seem like enough for most applications, but it is not. Each task alone consumes one descriptor for its program and another for its data. More typical programs take up to four or five descriptors. For this reason, an average system can allow only a few tasks to be active at a time. Segment descriptors must be loaded before, and remain for the duration of, the program segment's execution.

As an additional handicap, segment descriptors can only identify memory spaces that are multiples of a power of two (eg, 2K, 4K, or 16K). To allocate the right number of bytes for a particular segment, extra descriptors must be used, thereby consuming an already expanding descriptor space.

If, as is many times the case, more bytes are assigned to a data structure than are needed, the excess bytes become wasted space. This process is known as internal fragmentation. If a program is 1500 bytes long, for example, and 2K bytes are allocated for it, 500 bytes or 25% of the space is wasted; either segment descriptors are added to gain resolution (at the cost of scarce descriptor space) or memory is lost through internal fragmentation. Either alternative is unacceptable.

Segmented systems exhibit another often debilitating problem called external fragmentation. Since various-sized segments are used, it is necessary to find a proper-sized hole to place them in before swapping. External fragmentation results when the holes between segments are too small to accommodate an incoming segment. When this occurs, the operating system must decide whether to take out a segment large enough to create the required space or to crunch existing segments to make enough room. The first option is usually the one chosen because few computer architectures allow the dynamic relocation of programs and data required by the second. Fragmentation occurs with both primary and secondary storage.

The replacement algorithm assumes the role of determining which segment to swap out. In segmented systems, this decision has a great impact on system performance. If a small segment is removed, it may not create enough space; hence, several segments may have to go at once. If a large segment is taken out, much time is wasted on the transfer, throughput is diminished, and performance once again suffers. As an additional complication, if a large segment is swapped out, the space can become fragmented by smaller segments. When an attempt is made to swap the original segment back in, the hole no longer exists.

As can be seen, the optimum replacement strategy for segmentation is important. Not only is the probability of referencing a given segment difficult to predict, but the penalty for making a wrong decision is high. In addition, the operating system overhead for replacement algorithms and swapping has adverse effects on overall performance.

In recent years, the advantages of demand-paged virtual memory have caused some large computer makers to abandon the segmentation approach entirely. For example, following IBM's lead in its System/370 of the 1970s, Digital Equipment Corp has designed demand paging into its VAX-11 series, as has Data General in its MV8000 minicomputers.

Demand paging—the way to go

Demand paging systems solve all of the problems experienced by the segmentation approach to virtual memories. Demand paging divides both the virtual address space and main memory into equal-sized segments, called pages. The most obvious advantage of this method is that, because all pages are of equal size, pages can be swapped without leaving unusable fragmented spaces. In addition, it is not necessary to swap in all of a program's pages at once, just the page or pages required to carry out the immediate routine. This greatly reduces the time spent in swapping, since, as in the case of the NS16000, pages are only 512 bytes long. As a result, operating system overhead and performance improve tremendously.

Since there is absolutely no external fragmentation problem, the penalty for making a wrong prediction on a page swap is also greatly reduced.

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PM-DCV06A	RK06	CDC Phoenix CMD Drive or Ampex DFR9xx Series (32, 64, or 96MB ea.)	Min: 28MB (2 logical RK06) Max: 8 logical RK06; up to 2 physical drives
PM-DCV02A	RM02	80MB CDC 9762 SMD/80 CDC 9730-80 MMD/ 160MB CDC 9730-160 MMD	Min: 67MB (1 logical RM02) Max: 2 physical drives/4 logical RM02 (268MB total)
	RM05	300MB CDC 9766 SMD/600MB CDC 9775 FMD/ (also any CDC-compatible SMD interface)	Min: 256MB (1 logical RM05) Max: 2 physical drives/4 logical RM05 (1024MB total)
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Floppy:			
PM-XC21	RX02	Shugart/NEC/Qume. Single or double density	512KB per drive (x2)
PM-XC31	RX03	Shugart/NEC/Qume. Double-sided/double-density	1024KB per drive (x2)
Disc Cartridge:			
PM-DC06A	RK06	CDC Phoenix CMD Drive or Ampex DFR932 Series (32, 64, or 96MB ea.)	Min: 28MB (2 logical RK06) Max: 8 logical RK06 with up to 4 physical drives
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PM-DC02A	RM02	80MB CDC 9762 SMD/80MB CDC 9730-80 MMD/ 160MB CDC 9730-160MMD	Min: 67MB (1 logical RM02) Max: 268MB (4 logical RM02)
	RM05	300MB CDC 9766 SMD/600MB CDC 9775 FMD/ (also any CDC-compatible SMD interface)	Min: 256MB (1 logical RM05) Max: 1024MB (4 logical RM05)
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VAX			
SMD (Removable) MMD (Fixed):			
PM-DCG03	RM03/ RM05/ RM80	80MB CDC 9762 SMD/160MB CDC 9730-160 MMD (2 logical RM03 or 1 logical RM80)/300MB CDC 9766 SMD (1 logical RM05)/ 474MB Fujitsu M2351 (3 logical RM80)/600MB CDC 9775 FMD (2 logical RM05)/(also any CDC-compatible, SMD interface)	Min: 67MB (1 logical RM03) Max: 2048MB (8 logical RM05) Supports up to 4 physical or 8 logical drives

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The replacement algorithms concentrate on which page must be replaced rather than which segment. Hence, many programs can have pages in main memory simultaneously, and share memory with pages that have been most recently used. This reduces the frequency of page swapping.

The NS16000 also fully supports abort and retry instructions. Any memory reference—whether for instructions or data—can be terminated in mid-cycle. When this happens, the microprocessor saves the state of its operations to allow an instruction retry. An instruction retry occurs after the page containing the instruction or data is swapped into main memory. This means that both program and data pages can be swapped in dynamically (on demand). The implication, of course, is that a greater number of processes can reside in far less physical memory than is possible with segmentation.

In addition, this system allows a great variety of protection codes on each page. The MMU can be programmed to prohibit any combination of read or write references, depending on the task at hand. Protection can also be differentiated between supervisor and user modes.

Debugging has been designed as a function of the NS16082 MMU. The reason for this design is that it is in an excellent position to monitor program behavior because it resides on the address and data buses (Fig 2). Debugging is provided by the breakpoint and program-flow registers. Breakpoint registers can be programmed to monitor the address bus for any read, write, or execute reference. Program-flow registers record the addresses of consecutive, nonsequential program fetches and can be used to reconstruct the most recent two branches in the instruction flow.

Because of the nature of virtual memory, two sets of translation tables can be used within the system. This dual address space mode allows independent mapping of computer tasks and acts primarily to secure the operating system from destruction. This feature can be used to run several operating systems on one machine and to simply keep user tasks and the kernel physically separated. Thus, the operating system never loses control of the machine.

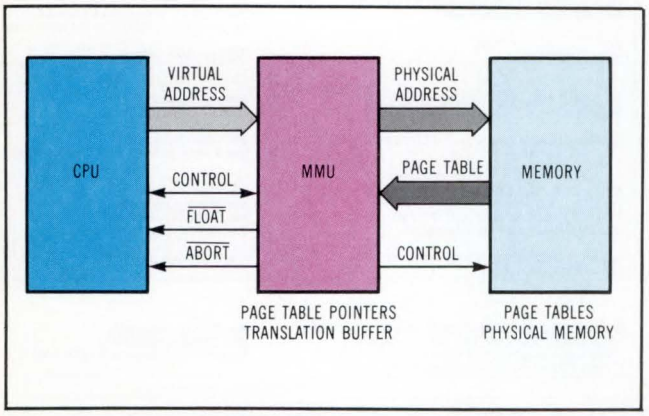

Fig 2 With the MMU conceptual interface, the MMU resides on both address and data buses; its internal registers can monitor program flow and implement dual address spaces.

Dynamic address translation

To reduce the number of NS16000 CPU and MMU pins (there are 48 for each), both units share the same multiplexed address/data bus. During the time the MMU needs to access memory translation tables, the MMU can assume full control of the bus.

The address space itself is divided into 32,768 fixed pages of 512 bytes each (Fig 3), as opposed to 64K bytes for some other microprocessing systems using segmentation schemes. This enables the NS16000 to transfer data in and out of memory quickly and uniformly.

The MMU keeps track of the logical and virtual addresses requested by the CPU. To do this, it uses page and pointer tables that are stored in main memory. These tables, which surprisingly do not require large amounts of memory, contain pointers indicating where to go in physical memory. An entire 16M bytes of virtual memory will use only one 1024-byte page table with 256 pointer tables of 512 bytes each, for a total of 132,096 bytes devoted to address mapping.

Although dynamic address translation looks complicated, it is quite simple to understand. For example, to keep track of a byte of data referenced by a logical or virtual address, but actually stored in a physical address, the MMU uses the 8 most significant bits of the 24-bit virtual address to locate 1 of the 256 (32-bit) entries of the page table. The MMU knows where the page table is kept in main memory through one of its two page table registers.

The contents of this page table entry (PTE), in turn, point to the start of 1 of 256 different pointer tables, each of which contains 128 (32-bit) entries. Once the pointer table has been located, the 7 next significant bits of the virtual address locate one of the entries, which contains the actual page number of the memory location. Once the physical address of the page containing the data has been located, the MMU translates the location (offset) of the data within the page directly from the 9 least significant bits of the virtual address.

A look at some of the details of a PTE will illustrate just how much usable information is included (Fig 3). In addition to the 16 bits devoted to the page frame number (the high order 16 bits of a physical page address), there is a valid (V) bit that, when set, indicates that the corresponding page is resident in physical memory. When the V bit is

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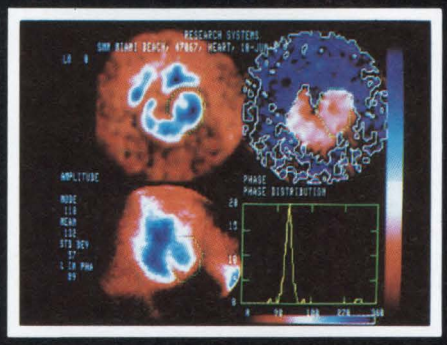

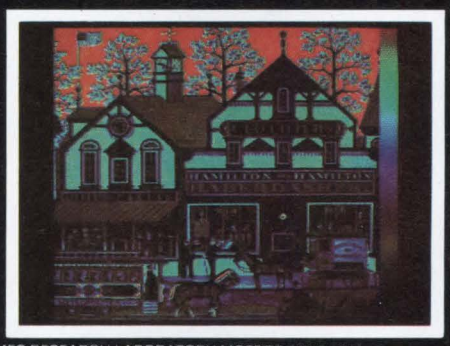

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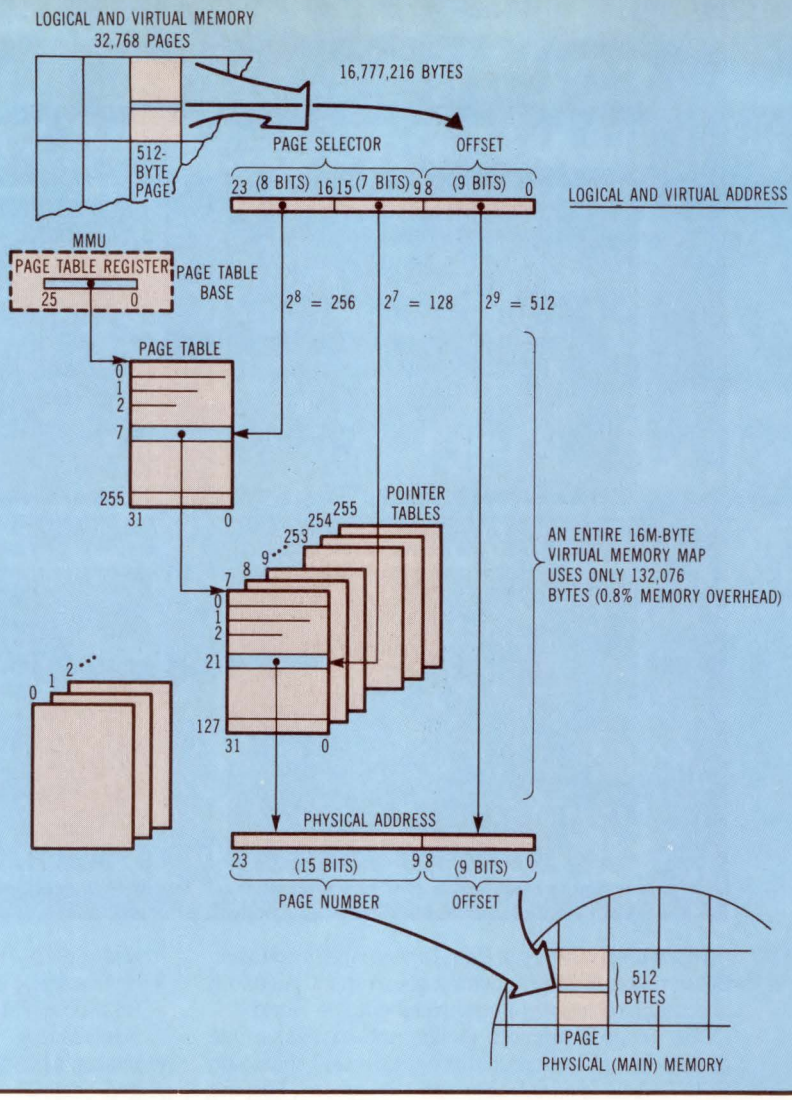

Fig 3 Any of 16,777,216 bytes of dynamic address translation of the NS16000 family can be located in physical memory by just selecting a PTE (8 bits), which references a pointer table (7 bits), which in turn points to the 512-byte page in physical memory. The byte location referenced within that page corresponds to the offset in the original logical address. Shaded areas indicate memory areas available for PTE expansion in larger systems.

cleared, any attempted reference to the page will cause the MMU to abort the reference. This, of course, is followed by location of the page on disk and a page swapping algorithm. The PTE also contains 2 protection level bits that control user access to pages. Divided between user and supervisor modes, these 2 bits can allow read-only, full-access, or no-access levels of accessibility.

Finally, a modified (M) bit indicates when the page mapped has been modified and whether a page needs to be written to mass storage when it is de-allocated from physical memory. A referenced (R) bit indicates when a page has been referenced. It is tested and cleared periodically by the operating system in order to compile frequency of reference statistics for each page currently in memory. This information is then used to determine the least frequently used pages when swapping in new pages from main memory. It is interesting to observe that the availability of unused portions of the PTE (shaded sections of Fig 3) permits the future expansion of the MMU to include both greater mapping space and conditional references.

Onchip cache

When a virtual (logical) address is passed from the CPU to the MMU, the MMU first attempts to match it with a special associative cache contained on the chip. This cache contains the 32 most recently accessed virtual addresses (15 bits) as well as their translated physical addresses (16 bits).

If the address requested by the CPU matches 1 of the 32 cache entries, the CPU is allowed access to the physical address immediately. This virtual to physical address translation takes only one clock cycle. Since the associative cache memory located directly on the CPU contains 32 of a possible 512 page address entries, it is easy to see how a logical to physical address translation happens so fast (Fig 4). Each cache entry contains not only the physical address of the information sought, but an associated protection level encoded in 2 bits. If the requested address is not present in the cache, however, the MMU must fetch both page and pointer table entries from memory before address translation can be performed. This can take up to 30 clock cycles.

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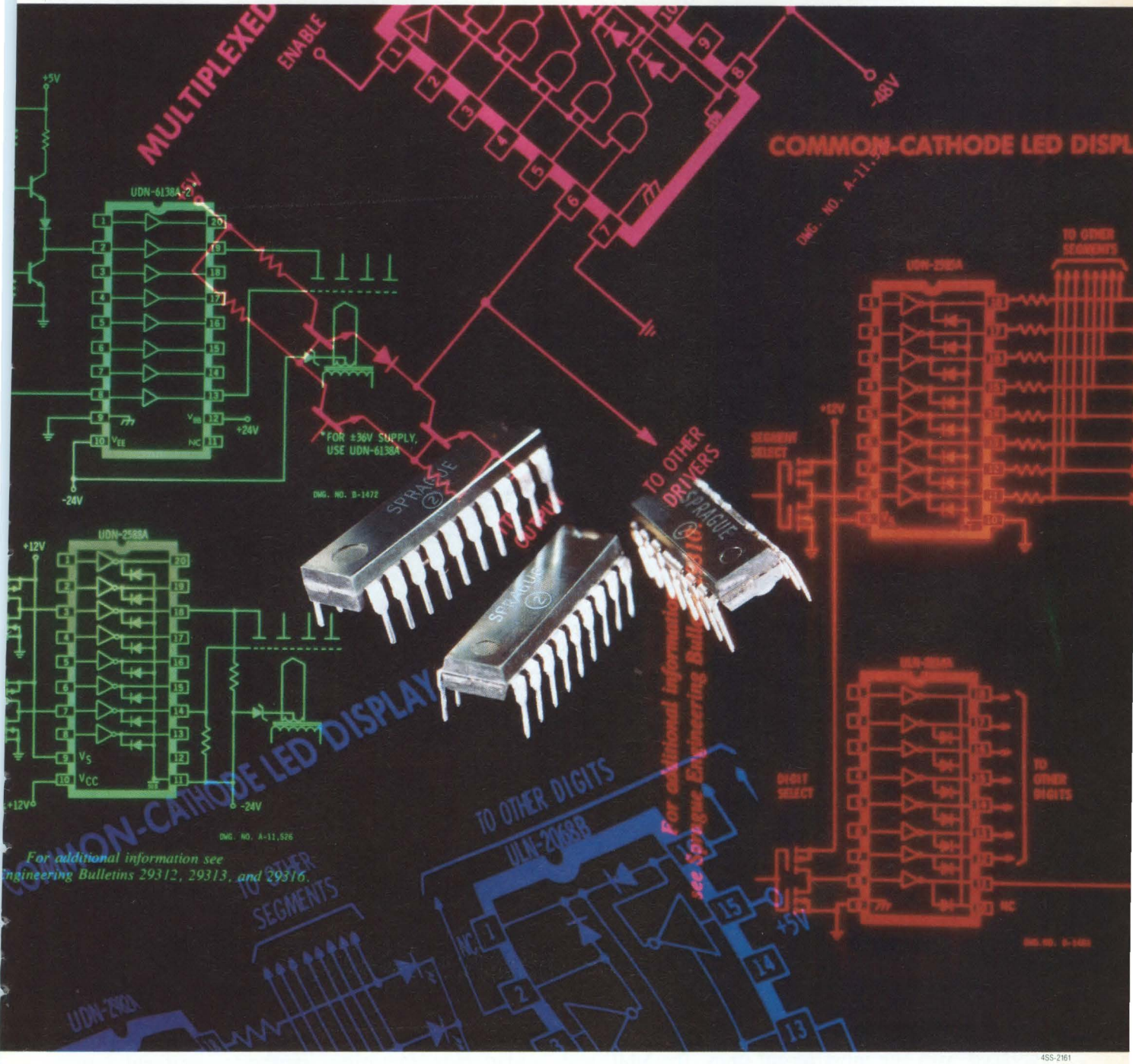

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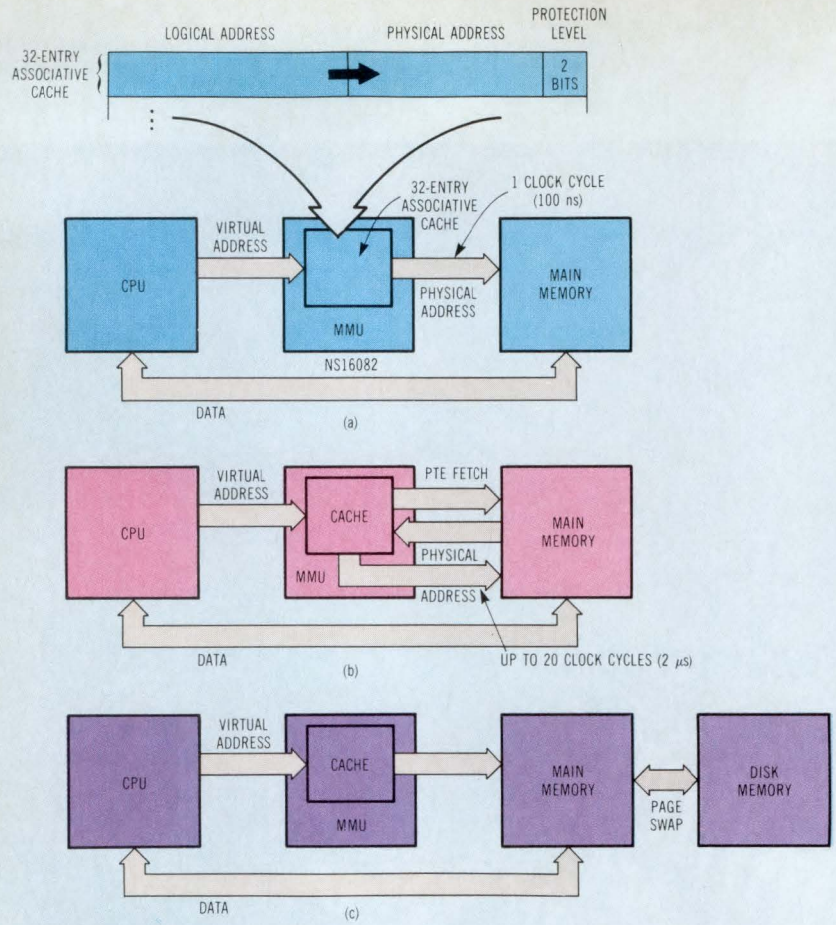

Fig 4 For an onchip cache, the PTE is resident in main memory (a), and data addressing takes only one clock cycle (100 ns). If the page is in main memory but not in the cache, a PTE must be fetched from main memory (b) using about 20 clock cycles. If the page must be swapped in from disk (c), an additional swap from main memory into cache must follow.

Although transparent to the user, the MMU associative cache has proven to be a powerful tool for hastening processing speeds. It has been calculated that a CPU entry will be present in the cache about 97% of the time. Such a hit ratio means that 97% of all references will take only one clock cycle.

If the next instruction address is not contained in the cache, the MMU must obtain the required entry address directly from the physical memory page table. In order to do this, the MMU floats the CPU bus by activating its Not Float (NFLT) signal, which turns over bus control to the MMU. The MMU, following a replacement algorithm already programmed in the hardware and transparent to the user, also updates the associative cache with this latest entry. Although the replacement algorithm causes the least recently used mappings to be replaced with the most recent ones, the MMU will fill an empty spot that appears in the cache before replacing an item in the cache.

It normally requires up to 20 clock cycles or 2 μs to fetch the PTE from main memory. Then, whether the page containing the required information is resident in main memory or on disk is determined. If it is in main memory, the CPU is released to access the data. If the page is resident on disk, however, the page must be swapped into main memory before the data are available for CPU access.

The benefits of the described memory page swapping methods are many. Moreover, with the advent of low cost disk memory storage, NS16032 CPU and NS16082 MMU users now have, with the virtual memory system, the cost advantages of a computer that has a minimal amount of expensive main memory. This system also has the large memory space formerly associated only with large mainframe computer systems. In fact, this system not only provides a less expensive way of obtaining large memory address, but an easier way of implementing it. Typical applications include intelligent terminals, workstations, business and personal computers, integrated office systems, graphics, telecommunications, and industrial and process control. Other applications include high performance games, computer aided design/computer aided manufacturing, synthesis, artificial intelligence systems, and radiation-hardened/high speed military systems.

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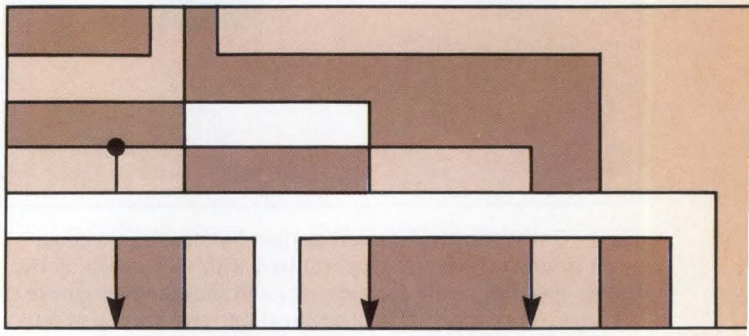
FIFO—THE GLUE HOLDING SYSTEMS TOGETHER

Dual-port, high density FIFOs are playing a greater role in interconnection. The latest generation offers HCMOS compatibility as well as onboard SRAM and independent access.

by Ching-Lin Jiang and Michael Bolan



Primarily because of the introduction of the microprocessor, computing power costs are now so low that the connections can cost more than the computers themselves. To lower these costs and to simplify rate buffer applications, first in, first outs are often used as connecting tools. But, they have been relegated to low bit density, they have expansion difficulties, and they do not have the advantages of high performance complementary metal oxide semiconductors, all of which impair their usefulness as connecting tools.

There are, however, a number of dual-port memories that are configurable with Mostek's BiPORT™ cell. One such compatible memory is the MK4501 first in, first out (FIFO), which will also carry an MK68000 family designation, MK68345. Its development is significant in that it makes possible innovative applications for memories as connector devices, particularly because it provides improved methods for interconnecting systems.

Most system designers are familiar with the use of memories as video buffers, disk buffers, and printer buffers. Historically, static random access memories (SRAMs) have been used to implement the buffer function. These examples, however, are all dual port in nature, and the use of a single RAM to implement them significantly increases system design complexity. It is now possible to configure dual-port memories in a variety of ways to meet specific application needs.

Ching-Lin Jiang is a senior design engineer at United Technologies/Mostek, 1215 W Crosby Rd, Carrollton, TX 75006, where he is responsible for the BiPORT memory designs. Mr Jiang holds a BSEE from National Taiwan University, an MSEE from the California Institute of Technology, and a PhD from the California Institute of Technology.

Michael Bolan is currently a product definition manager at United Technologies/Mostek, where he is responsible for the BiPORT memory designs. He is interested in nonvolatile memory and computer architecture. Mr Bolan holds a BSEE from the University of Cincinnati.

Interconnect problems and approaches

Today's system designers face a bewildering number of interconnect problems. Transporting data across a time boundary and providing the necessary elasticity (buffering) for different data rates are the two

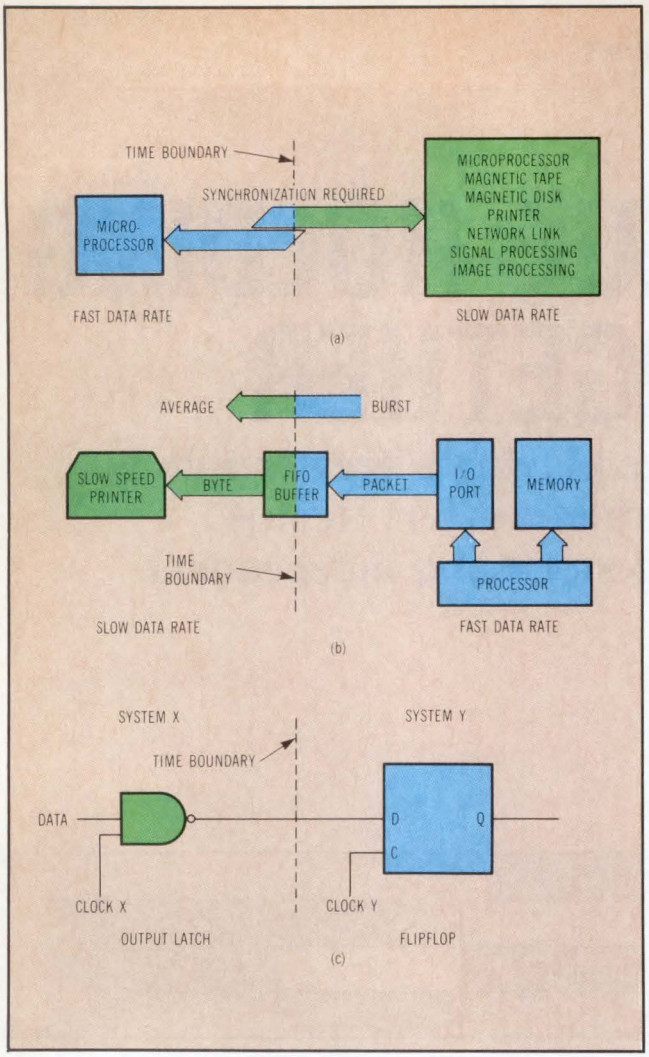


Fig 1 Transporting data across time boundaries, in some applications (a), can be synchronized with a common clock, but as speed disparity increases (b) and independent clocks are used, the danger of synchronization error increases (c). Buffer size is directly influenced by the disparity of data rates.

most common and most difficult. To transport data across a time boundary requires synchronization [Fig 1(a)]. In a simple system, a common clock allows a straightforward solution. As a system becomes more complex, a common clock is no longer possible—for example, a computer transmitting data at full speed (1M bps) interfaced to a serial printer that receives data at 1200 bps [Fig 1(b)].

Assume two systems (X and Y) with independent clocks, where X needs to pass data to Y. Most engineers are familiar with clocking data into a D flipflop [Fig 1(c)]. Because the relationship between clock X and clock Y is asynchronous, the possibility exists that data at the D input to system Y's flipflop will arrive at exactly the same time that C receives a clock pulse. In this case, the time required for Q to reach a stable state is indeterminate. This is often referred to as a meta-stable state or synchronization error.[1, 2]

Avoiding this problem is fundamental to reliable system operation. Arbitration minimizes, but does not eliminate, the possibility of synchronization error. The essence of this technique is to narrow the time window of sensitivity—ie, speed up the clocks—until the probability of timing collisions is insignificant in a given application. The window of sensitivity is equal to the few nanoseconds of setup time, plus the hold time. If the clock rate is very slow—one or fewer events per hour—the possibility of a problem becomes extremely remote. However, as the clock rate is increased, the problem becomes more acute. In practical circuit design, parameters such as high transistor gain, short propagation delay, and multiple strobes can narrow the window. Even when careful attention is given to circuit design, circuit performance verification can be so difficult as to limit the usefulness of this technique.

Handshaking is another common method of transporting data across a time boundary. Data transfers are constrained to follow a strict protocol of request, acknowledge, and transmit. The biggest disadvantage is the hardware overhead needed to generate the handshake signals and the time needed for synchronization. When used in computer systems, this approach often results in substantial software overhead, with correspondingly slower execution times.

Another technique involves the use of a dual-port memory. An essential requirement is that the hardware be able to support simultaneous writes in Port X while Port Y is reading. The development of such a memory cell in high performance complementary metal oxide semiconductors (HCMOSs) is important because it can also help simplify subsystem interconnection.

The Table shows the variations possible for a dual-port memory. Although the BiPORT cell allows asynchronous reads and writes in either port

Port Variations

Port X	Port Y
Write only	Write only
Read only	Read only
Read/write	Read/write
Sequential	Sequential
Random	Random
Serial	Serial
Parallel	Parallel
Synchronous	Synchronous
Asynchronous	Asynchronous

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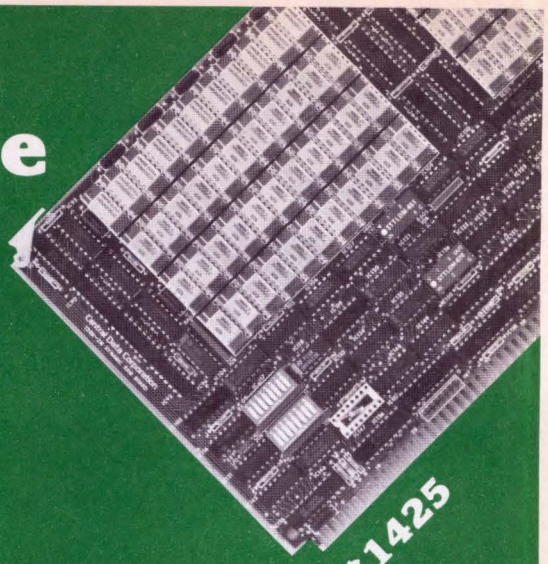

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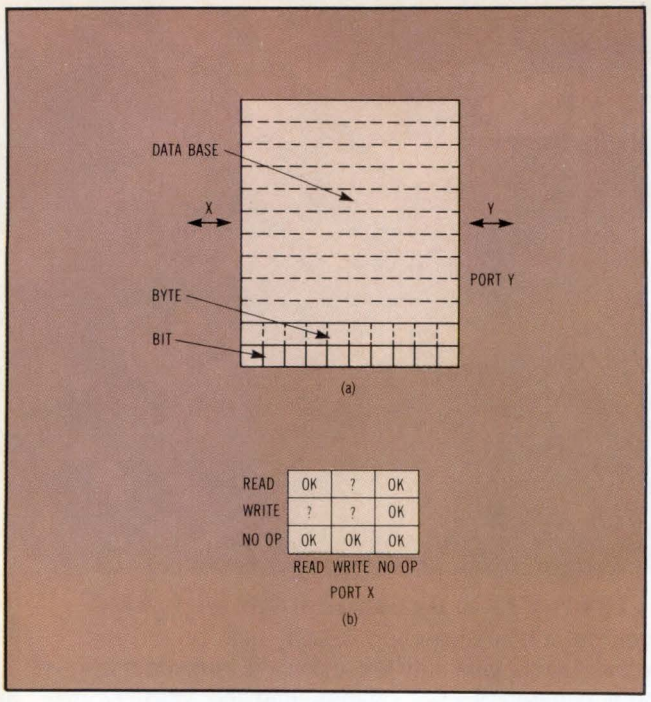

Fig 2 Because bits are usually part of a larger unit (a)—a byte or a data set—the integrity of the data can be jeopardized if a simultaneous write or a simultaneous read/write is attempted (b).

on the same cell, data bits in a system are normally interdependent. Sets of bits make up a byte, sets of bytes make up a data base [Fig 2(a)]. Often these set relationships must be preserved. Fig 2(b) shows the conditions under which the integrity of the set is in jeopardy. Because bits are normally not independent entities, but have a set relationship, a more significant accomplishment is moving a set of data bits (a byte or word) across a time boundary while maintaining its integrity. One implementation in the BiPORT series is a device following FIFO rules. This device allows simultaneous writes and reads, but not at the same location, thereby maintaining integrity of the set. A FIFO can therefore be used to avoid synchronization problems.

Data rate disparity between the sending and receiving subsystem is another difficulty that system designers face. To overcome this, data must be allowed to accumulate or to be buffered. The SRAMs that have been used for this purpose have two distinct drawbacks: the circuitry needed to generate address information and a need for the overhead circuitry to create separate input and output ports. The buffer space required is a function of the rate disparity: the greater the disparity, the larger the buffer must be. The MK4501's main application is as a rate buffer capable of absorbing and sourcing data being transmitted at different clock rates, such as interfacing fast processors to slow peripherals.

Because rate buffer applications are often concerned with overflow and underflow conditions, FIFO full and empty flags are provided to prevent such conditions. Ideally, a FIFO should be large enough that full and empty flags are rarely generated, so that the direct attention of the sender and receiver is not needed, and data transfer can proceed automatically. If the sender or receiver must spend much time dealing with overflow and underflow, little time is left for more important tasks. When interruptions for full and empty flags reach an extreme, the subsystem begins to thrash, allowing no time for useful work. For this reason, the low bit density of previously available FIFOs has limited their usefulness.

Architecture and bipolar circuit limitations also restrained earlier FIFO approaches. The most popular devices resemble shift registers in which data are dumped in one end and fall out the other, after propagating through the entire depth of storage. A consequence of this approach is a rather long fall-through delay, which exhibits itself as a delay between the time data are written and the time data can be read. As the FIFO depth increases, this delay also increases, making expansion awkward.

Bipolar devices are inherently larger than the equivalent complementary metal oxide semiconductor (CMOS) devices, permitting fewer gates on a chip of a given size, and requiring significantly more power to operate. For this reason, FIFOs have been available only at low bit density and high power dissipation.

A high density monolithic FIFO

The MK4501 is the highest density monolithic FIFO available. The package pinout is given in Fig 3 with pin functions and performance characteristics listed in the accompanying key. This pinout is designed to serve many generations of higher density FIFOs. A key feature of this memory, its 8-element BiPORT

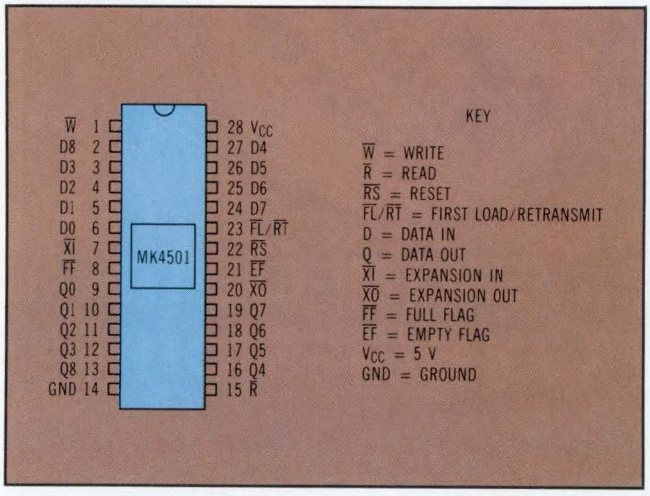

Fig 3 In the MK4501 monolithic FIFO, two sets of nine pins are labeled D0–D8 for data in and Q0–Q8 for data out. Because bytes are accessed sequentially by separate read and write pointers, there is no need for address lines; the $\overline{RS}$ line puts everything into a known state.

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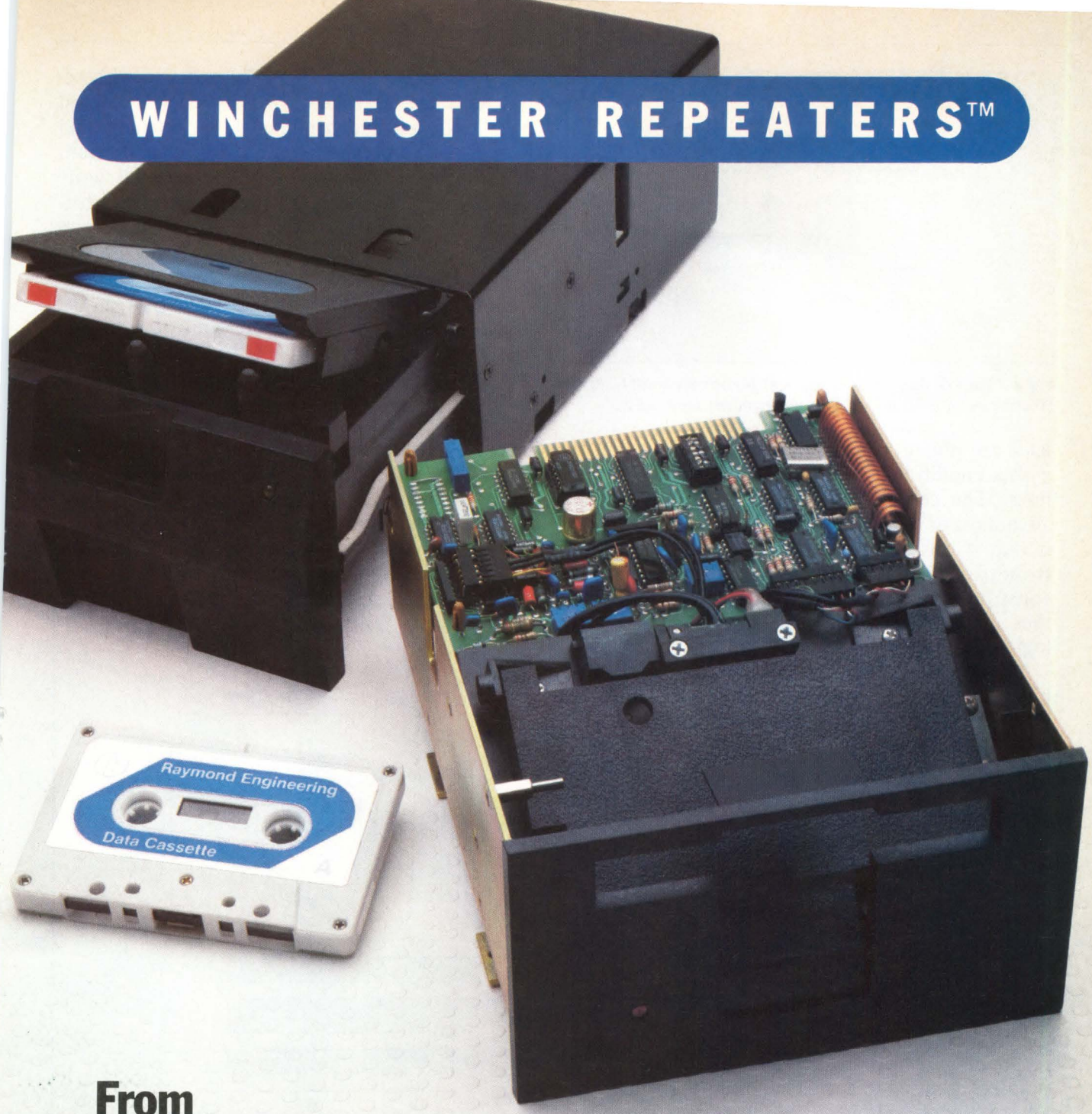

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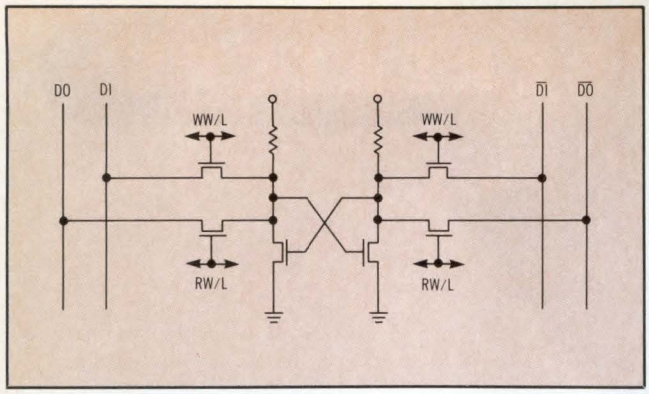

Fig 4 The cell area of the 8-element BiPORT RAM cell is 40 x 50 microns or 3.2 mil^2 with an independent read/write.

RAM cell (Fig 4), consists of a SRAM cell augmented with an additional set of access transistors and bit lines. The cell size is 40 μm x 50 μm. A clear advantage of a memory array formed by these cells is that it can be read and written independently, from two separate ports. An efficient FIFO can be constructed using this dual-port array supported by the appropriate addressing schemes and status logic circuitry.

The 512 x 9 FIFO memory chip consists of four building blocks [Fig 5(a)]. The memory function block includes the matrix, the read/write control logic, and the location pointers. The flag generation block uses counters and comparators to create empty and full status flags. The expansion logic block provides the input and output control signals to expand the depth of the FIFO, while the reset block generates commands to reset all FIFO operations.

The memory matrix is organized into 128 rows and 72 columns, split into two halves, made up of dual-port RAM cells. Read pointers address the 128 read word lines that are in the center of the chip. Two identical sets of write pointers are placed at the right and left sides of the matrix for the corresponding 128 write word lines. Two 4-bit column pointers are used to access the bit lines for the read and write operations. The pointers consists of CMOS shift registers.

The MK4501 operation depicted in Fig 5(b) uses two independent pointer rings to address the BiPORT memory array. Using shift registers only in the pointer rings and BiPORT RAM cells as storage elements provides efficient usage of silicon real estate, resulting in very high density monolithic FIFOs.

To begin MK4501 operation, a reset command is sent into the device by drawing the $\overline{RS}$ input low. During the reset, both the internal read and write pointers are set to zero (W_0, R_0), and an empty flag is internally generated to inhibit any read functions.

This FIFO initiates a write cycle on the falling edge of the write enable control input ($\overline{W}$) provided that the full flag ($\overline{FF}$) is not set. Data setup and hold time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data are stored sequentially and independent of any ongoing read operations. To prevent a data overflow condition, the $\overline{FF}$ will go low whenever the internal write pointer catches up with the read pointer, and further write operations will be inhibited. Upon completion of a valid read operation, the $\overline{FF}$ will go high and a valid write can begin.

Similarly, the device initiates a read cycle on the falling edge of the read enable control input ($\overline{R}$) provided that the empty flag ($\overline{EF}$) is not set. In the read mode, it provides fast access to data from 9 of 4608 locations in the static storage array. The data are accessed on a FIFO basis independent of any ongoing write operations. After $\overline{R}$ goes high, the data outputs will return to a high impedance condition until the next read operation. In the event that all data have been read from the FIFO, the $\overline{EF}$ will go low and further read operations will be inhibited: the data outputs will remain in high

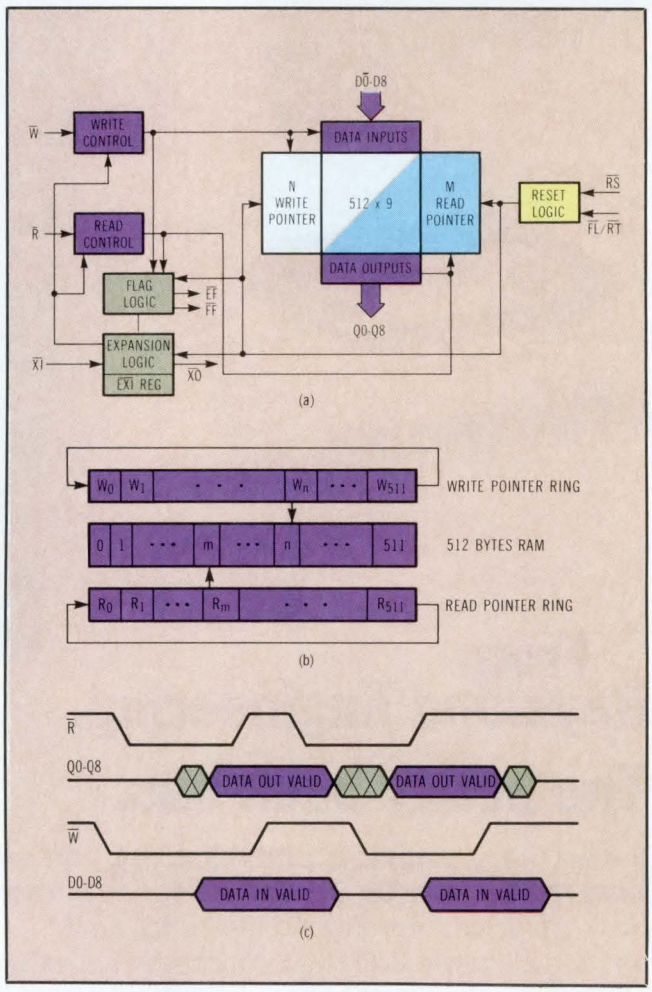

Fig 5 In the 512 x 9 FIFO memory chip (a), the read control advances the read pointer and accesses the data output, while the write control independently increments the write pointer and connects to the data input (b). The write operations are inhibited when chip timing is such that the write pointer catches up with the read pointer, preventing buffer overflow (c).

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impedance. Upon completion of a valid write operation, the $\overline{EF}$ will go high, and a valid read can begin. The maximum latency can be just one cycle time. Fig 5(c) shows the timing diagrams of the previously described read/write operations.

This FIFO's word width can be expanded beyond 9 bits simply by connecting the corresponding input control signals of multiple devices. Any one device can detect status flags ($\overline{EF}$ and $\overline{FF}$). Fig 6(a) demonstrates a method of implementing an 18-bit byte width by using two MK4501s. Any byte width can be attained by adding devices.

The basic pointer ring architecture shown in Fig 5(b) provides an easy means to expand the FIFO depth to greater than 512 bytes. Basically, the rings of the individual devices can be externally connected through the expansion in ($\overline{XI}$) and expansion out ($\overline{XO}$) signals to form an arbitrarily large ring of pointers in a multiple-device FIFO system. Fig 6(b) demonstrates depth expansion using three MK4501s. Any depth can be attained by adding more devices. This FIFO operates in the depth expansion configuration when certain conditions are met.

The first device must be designated by grounding its first load control input ($\overline{FL}$), and all other devices must have $\overline{FL}$ in the high state. The expansion out ($\overline{XO}$) pin of each device must be tied to the expansion in ($\overline{XI}$) pin of the next device. External logic is needed to generate a composite full flag and empty flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s—ie, all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$ [Fig 6(b)].

One additional feature of this device is the retransmit capability for systems having data writes less than 512 bytes between resets. The FIFO can be made to retransmit data when the retransmit enable control input ($\overline{RT}$) is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. $\overline{R}$ and $\overline{W}$ must be inactive during retransmit. It should be emphasized that this retransmit feature is not compatible with the depth expansion previously described where the same pin is used to designate the first active device in a ring of FIFOs.

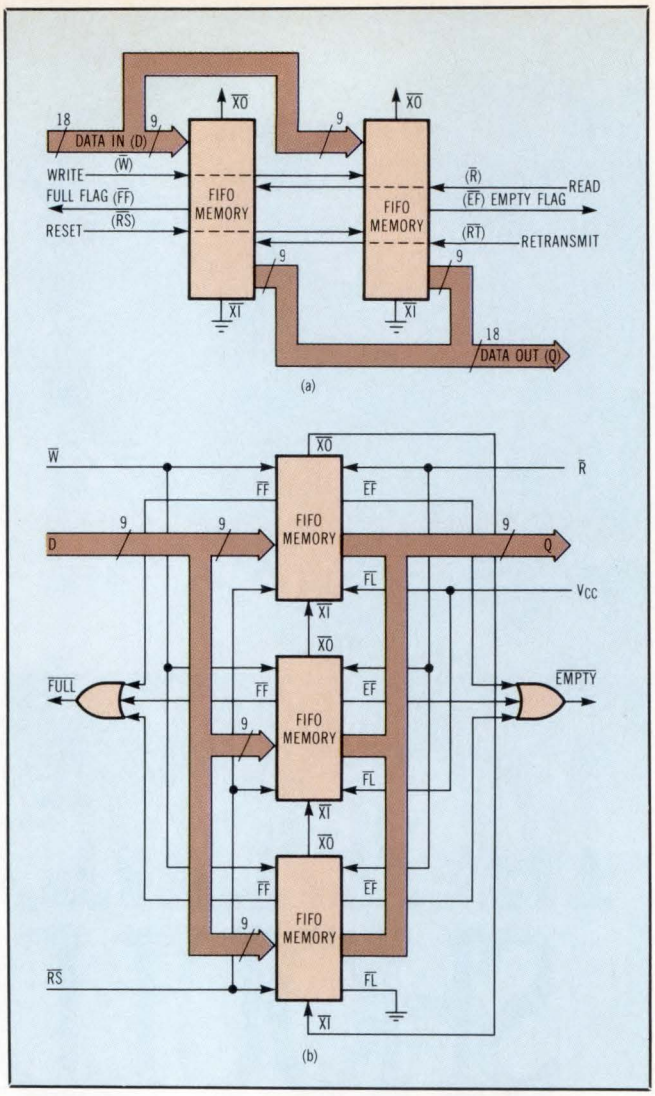

Fig 6 Width expansion of the 512 x 18 FIFO memory (a) is a straightforward matter of connecting the respective read and write pointer rings by means of XO and XI signals. Depth expansion (b) to 1536 x 9 format requires chaining three chips or more together.

FIFO solves rate buffering problems

An application of the MK4501 to the Harris Corp's Mind™ series of distributed data processing systems is a good example of how to solve rate buffering problems. This application involves connecting a disk controller to a memory system through a direct memory access (DMA) controller. If the data rate coming from the DMA controller can exceed disk capability, the data rate from the disk controller can vary by ± 2%.

Using several MK4501s for rate buffer memory eliminates timing problems and smooths the data transfer. This application involves a 16-bit data bus. As a result, two FIFOs are required to implement the data bus. (The parity bits are not required in this application.) The data bus must also be bidirectional, and because this FIFO is designed to pass data in only one direction, a total of four is required to meet the bidirectional need.

Moreover, the application requires that entire sectors be read or written at a time. Because a sector length is 128 bytes, the 512-byte depth of the MK4501s is more than adequate to meet the requirement. If a read-from-disk operation is desired, the processor gives the disk controller the appropriate commands. The disk controller responds by writing data to the read-data FIFOs. After the first byte in a sector has been written, the empty flag goes to the inactive state ($\overline{EF}$ = VOH), which signals the DMA circuitry to start reading data. Data are continuously transferred from the disk through the DMA to memory until the processor terminates transfer from the disk controller. The DMA can

move data faster than the disk controller can, but the full flag of the read data FIFO is connected to the interrupt network of the processor, should an error or overrun condition occur.

If a write-to-disk operation is desired, the processor circuitry gives the DMA the appropriate commands. The full flag from the write-data FIFOs is used to tell the DMA that the FIFOs are not full and data transmission can occur ($\overline{FF} = VOH$). The DMA will then write data to the FIFO buffers in an attempt to completely fill them. When the buffers are full, the full flag changes state ($\overline{FF} = VOL$), terminating the DMA request. The MK4501 will then generate a full flag prior to completing the last write cycle that causes the buffers to be full. This gives the DMA time to recognize that the DMA request has been terminated prior to doing another write cycle. Transfer from the FIFO to the disk is accomplished by the disk controller under the direction of the processor.

Software is designed so that an underrun condition, FIFO empty, should not occur. However, the empty flag of the write-data FIFO is connected to the interrupt network of the processor, should an error or underrun condition occur. The $\overline{R}$ and $\overline{W}$ signals are generated by the appropriate control device (disk controller and DMA) and conditioned with timing signals. Only a minimum of interface logic is required to use the MK4501. The tri-state buffers of the FIFO allow direct connection to the processor and disk controller bus, eliminating the need for multiple bus transceivers.

Future products using the BiPORT cell will also encompass shared storage for tightly coupled processors. More advanced rate buffers are also under development to further increase FIFO bit density and performance.

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2. T. J. Chaney and C. E. Molnar, "Anomalous Behavior of Synchronizer and Arbiter Circuits," *IEEE Transactions on Computers,* Apr 1973, p 421.

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NO WAITING— EEPROM AT WORK

In addition to allowing TTL level *in situ* programming, today's EEPROMs write and erase without delaying their host microprocessor.

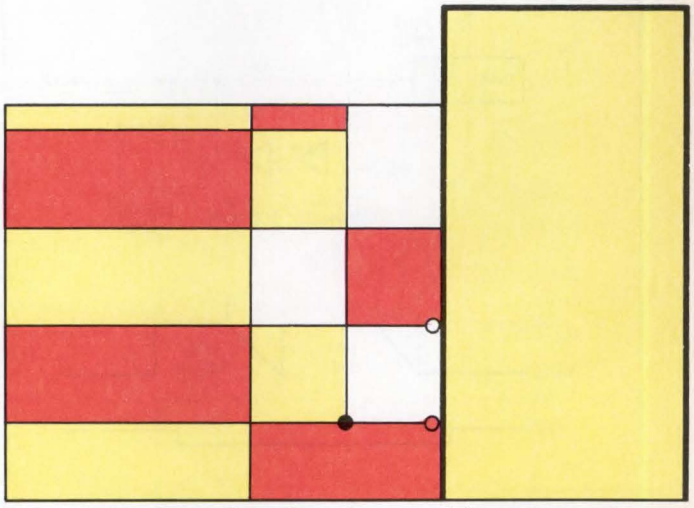
by Kendall W. Pope

As control, monitoring, and portable or remote data gathering applications become commonplace, the designers of such systems often find themselves between a rock and a hard place. At issue is memory. The choice facing designers has traditionally been whether to use random access memory or read only memory for storing small amounts of program code and data.

Random access memory (RAM) is attractive because it makes the inevitable debugging and altering of programs infinitely easier. Its main drawback, however, is its susceptibility to the loss of information during a power failure. Although battery systems alleviate this problem, the solution is a real-estate and cost-intensive one.

Read only memory (ROM), on the other hand, is immune to the volatile frailties of RAM and requires no external power or refresh mechanism. Unfortunately, the very nonvolatility that makes ROM attractive also limits its flexibility in many applications. Code resident in ROM (including programmable ROM and ultraviolet erasable programmable ROM) is difficult to alter. At the very least, chips must be removed from circuits, erased, reprogrammed, and then reinstalled. This is a time-consuming, cumbersome and—in some applications—an impossible procedure.

Kendall W. Pope is an applications engineer at Synertek, 3001 Stender Way, Santa Clara, CA 95051, where he is responsible for all memory products. He holds a BSEE from California Polytechnic State University at San Luis Obispo.



It seems, then, that there is a need for a nonvolatile memory chip that can be programmed and reprogrammed *in situ*. Such a chip must also allow programming to take place quickly (in 1 s) to be of any practical value. Other desirable features might include the ability to reprogram individual words stored within the chip as well as an architecture that facilitates easy interfacing with other circuit components.

Enter the latest generation of electrically erasable programmable ROMs (EEPROMs). The basic cell of the EEPROM is a floating gate transistor (Fig 1) in which the threshold voltage can be changed by the application or removal of a charge on the floating gate. The EEPROM is constructed from a number of these cells by completely surrounding each polysilicon floating gate with a silicon dioxide layer. Because less than 10% of a charge placed on the floating gate leaks away in 10 years, EEPROMs provide nonvolatility. The EEPROM uses a thin oxide layer to pass electrons to and from the floating gate, thus facilitating cell programming.

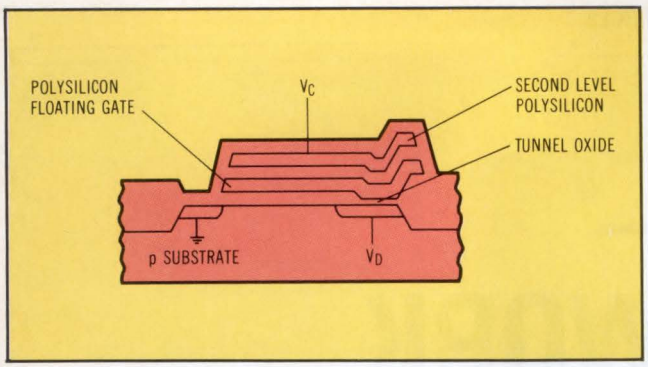


Fig 1 The floating gate transistor memory cell threshold voltage responds to a charge placed on the floating gate. The cell is fully static, yet it can be reprogrammed if a charge is applied sufficient to initiate Fowler-Nordheim tunneling through the dielectric layer (tunnel oxide).

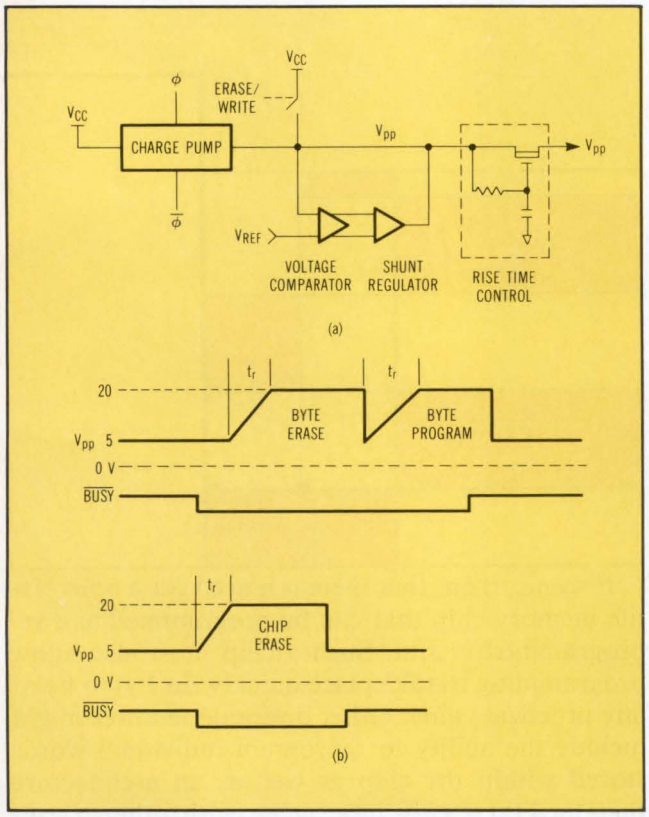


Fig 2 Erase/write voltage is generated from TTL levels onchip (a) and limited by shunt regulators. The 20-Vdc pulse waveforms (b) that result are more than adequate to write to and clear memory cells.

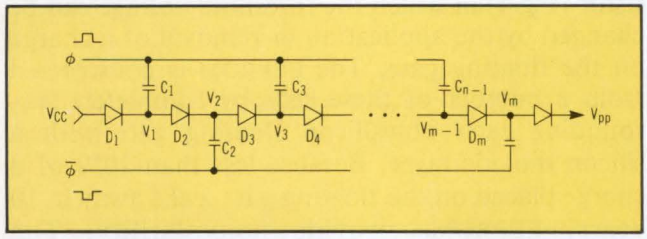


Fig 3 An onchip charge pump circuit uses a succession of capacitors and diodes to raise TTL-input voltage levels to a value sufficient for EEPROM programming.

An EEPROM's physical mechanism of programming is known as Fowler-Nordheim tunneling. This occurs when an electrical field is applied across a thin silicon dioxide insulator. As the electric field approaches 10 MV/cm, electrons penetrate the silicon dioxide layer and tunneling begins.

The tunneling mechanism is bidirectional, thus allowing each gate to be charged as well as discharged. If the insulator is less than 200 Å thick, programming levels of approximately 20 Vdc are possible. In this case, an onchip charge pump is used to generate voltage levels adequate for programming from 5-Vdc sources. The onchip charge pump eliminates the need for externally generated, high voltage programming pulses and associated pulse-shaping circuitry.

A charge pump is a relatively straightforward circuit and works as follows. The erase/write voltage V_{pp} is generated internally and limited by a shunt regulator. This mechanism appears in Fig 2(a). An additional shunt is used to clamp V_{pp} to V_{CC} when the cell is not erasing or writing. This clamp is released once for each individual erase or program operation, producing a V_{pp} pulse that swings between 5 and 20 Vdc [Fig 2(b)]. The leading edge of this pulse is ramped by a rise time control circuit in order to prevent damage to the memory transistor's tunnel dielectric.

The voltage multiplier, or charge pump, depicted in Fig 3 operates in a manner similar to the technique used to raise a metal oxide semiconductor transistor's gate voltage above the supply level. Coupling capacitors C_1 to C_{n-1} are driven by internally generated clocks (ϕ,$\overline{\phi}$) and pump packets of charge along the diode chain D_1 to D_m. Because the nodes between diodes are not discharged, the average potential (V_1 to V_m) increases progressively from input to output along the diode chain. In the configuration depicted in Fig 3, the voltage that results at the output of the diode chain is more than sufficient for EEPROM cell programming.

The combination of Fowler-Nordheim tunneling and an onchip charge pump allows 20-Vdc programming levels to be generated from 5-Vdc supplies. As a result, a compact package of nonvolatile, yet easily alterable, memory can be fabricated.

Extending EEPROM capability

A producer of EEPROM devices, Synertek uses charge pump techniques in its SY2801A memory chip. This fully static chip allows TTL level programming to take place in 10 ms and is packaged in standard 16-pin, dual-inline format. Unfortunately, for many applications, this chip's 20-ms erase/write cycle is too slow. In these situations, it is often necessary to latch incoming data with

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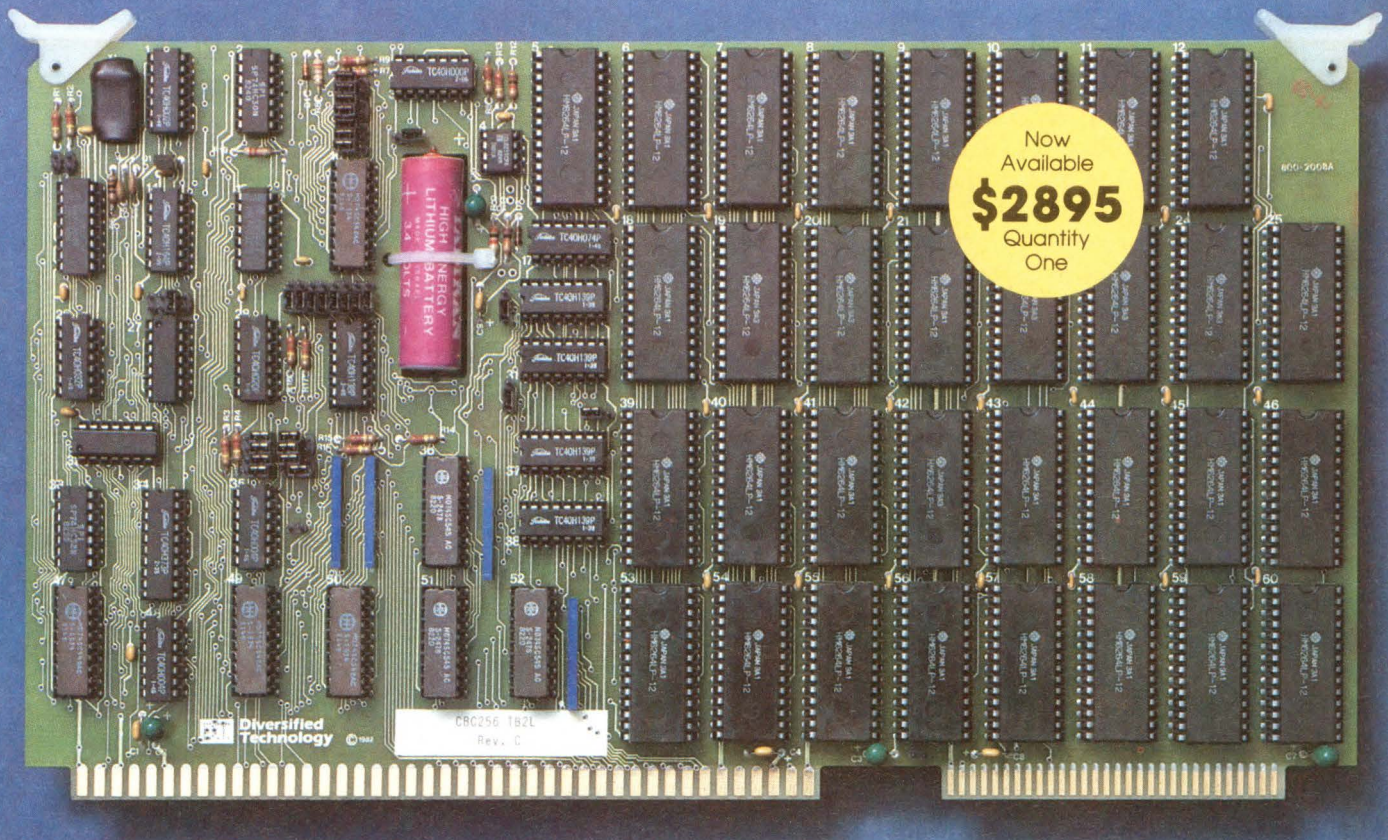

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Operating Currents	3.0A, 1.4A (max.)	100mA (max.)
Cycle Time	48 milliseconds avg.	500 nanoseconds typ.
Card Slots Required	2	1
Operating Temperature	0°-55°C	0°-70°C

ADDITIONAL FEATURES OF DTI'S CBC 256 INCLUDE:

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CIRCLE 102

external circuitry. This latching complicates interfacing EEPROMs with the rest of the circuit elements and often requires more circuit board real estate than can be justified.

To alleviate these problems, the company developed the SY2802E chip (Fig 4). This EEPROM incorporates all the onchip logic necessary to allow it to function as a 256- x 8-bit nonvolatile memory register file. Featuring a general purpose, bus-oriented interface, this chip is well suited for use with most microprocessors. Included in its architecture are an 8-bit data latch, a status register, and timing and control circuitry. Because of the chip's data latch circuitry, a microprocessor does not have to wait for it to complete an erase/write cycle. In fact, the processor can go about its business without regard for any EEPROM activity.

Essentially, the chip serves as a small lookup table for a microprocessor. Its main focus is actually not software storage, but rather, the storage of data such as calibration constants. Thus, the main problems that the SY2802E addresses are in timing and control areas. Because the chip has a full set of onboard control logic—plus control signals for the microprocessor to work with—it does not need a traditional architecture of its own. As a result, the device looks like an input/output (I/O) location rather than an area of memory, resulting in several benefits when the chip is used with I/O oriented microcomputers.

To interface externally, the SY2802E ties into a data bus and data port. All operations can be port oriented and internally controlled. No longer is the designer limited to a $\overline{\text{BUSY}}$ signal coming from an EEPROM. Now, because access to a status register is available, processors that cannot be interrupted can be used. In addition to a 3-state bidirectional 8-bit data port, this EEPROM has conventional chip select ($\overline{\text{CS}}$), register select (RS), read/write (R/$\overline{\text{W}}$), and strobe (STRB) inputs. For external wait state or

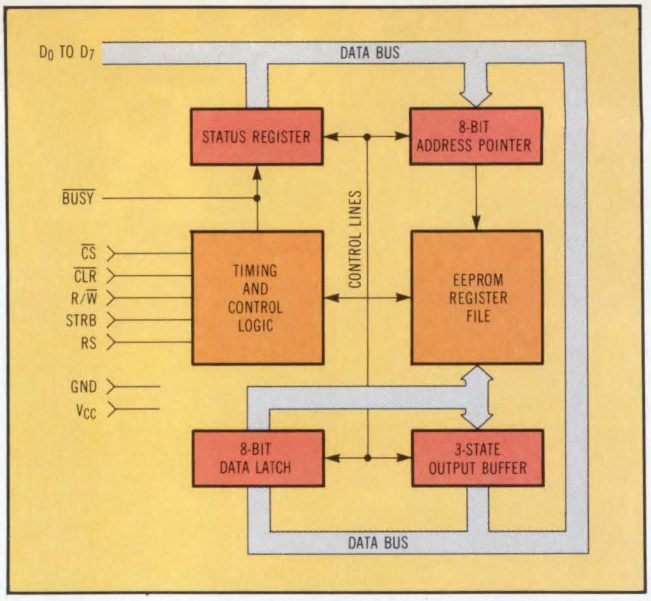

Fig 4 This EEPROM block diagram reveals the key to improved memory performance. Including a data latch and status register enables the chip to operate without causing processor delays or requiring external timing or control.

polling operation, a chip clear/store ($\overline{\text{CLR}}$) cycle status flag—$\overline{\text{BUSY}}$—is available.

The SY2802E also has seven modes of operation. (See the Table.) The reading mode requires two cycles. First, the address is loaded into the 8-bit address pointer, and, second, the data from the selected location are read. Both the address and data are transmitted through the same 8-bit port, and 8-bit address data are relevant only to internal locations.

The writing mode also requires two cycles. As with the read cycle, the address pointer is loaded first. Then, by loading the data input register, the byte erase/write operation is initiated. Therefore, during the byte erase/write operation, the microprocessor is free to perform other tasks. Both the $\overline{\text{BUSY}}$ bit and bit 7 of the status register are set

Operational Modes

Mode	Pin $\overline{\text{CS}}$ (12)	R/$\overline{\text{W}}$ (16)	RS (15)	STRB (13)	$\overline{\text{BUSY}}$ (14)	$\overline{\text{CLR}}$ (11)	Data Input/ Output (0 to 7)
Read Register File	0	1	0	X	1	X	Data Out
Read Status Register	0	1	1	X	X	X	Data Out
Write Address Pointer	0	0	0	↗	1	1	Data In
Write Data in Latch	0	0	1	↗	⊓	1	Data In
Deselected	1	X	X	X	X	X	High Z
Write Inhibited	0	0	X	↗	0	1	X
Block Clear	0	1	1	↗	⊓	0	High Z

X = Don't Care
↗ = Positive Transition
⊓ = Negative Pulse

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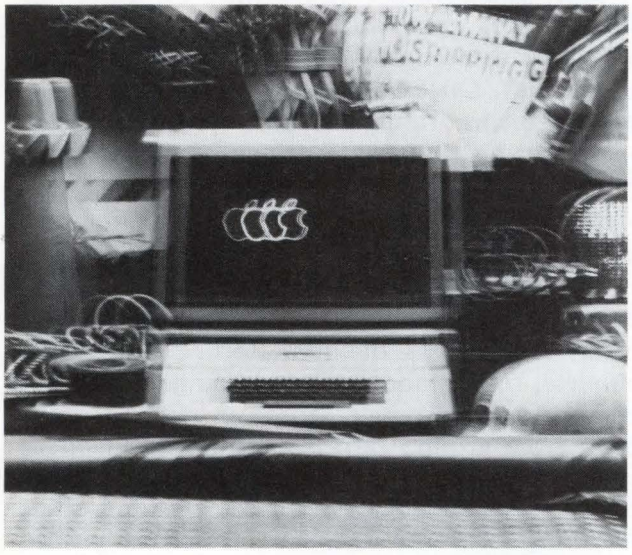
—Daniel R. Obed, CEO
MPC Peripherals Corp.
San Diego, California



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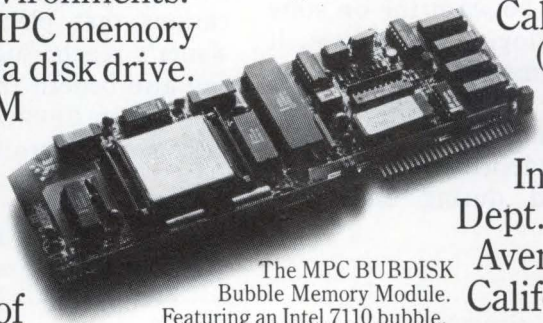

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CIRCLE 103

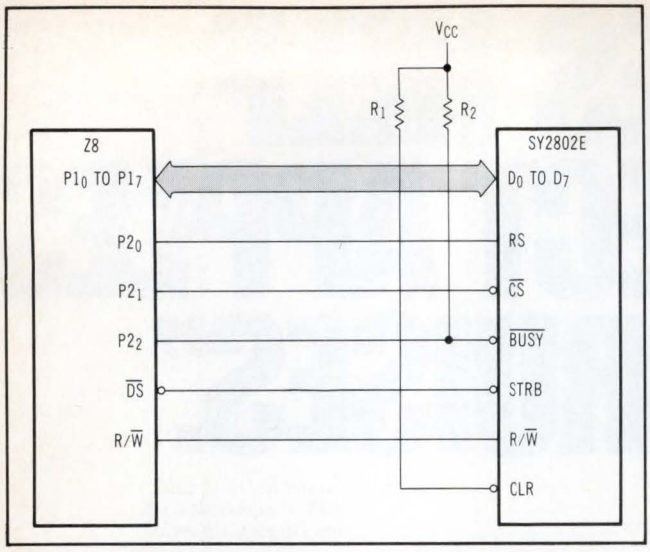

Fig 5 In this microcontroller configuration, Port 1 ($P1_0$ to $P1_7$) is byte configured as an 8-bit data I/O port and handles address and data. Port 2 ($P2_0$ to $P2_2$) is bit configured and handles register select (RS), chip select ($\overline{CS}$), and $\overline{BUSY}$ signals.

during the erase/write operation. During this operation, only the status register is accessible. Depending on the circumstances, the microprocessor can interact in one of the following methods:

- Processor is held in wait states until $\overline{BUSY}$ inactive
- Processor is in a tight program loop using status register read and branch on minus (bit 7)
- Processor works on other tasks, periodically polling the status register (bit 7)
- Processor uses the trailing edge of the $\overline{BUSY}$ signal to activate an edge triggered interrupt

In addition, the SY2802E can be block cleared to all zeros. As with data store, the clear cycle need only be initiated. All the timing is controlled internally, and $\overline{BUSY}$ and status (bit 7) become active. Again, during the clear cycle, only the status register is available.

One of the most distinguishing characteristics of EEPROMs is that the number of erase/write cycles is limited. As the voltage level between the on state (logic 1) and the off state (logic 0) decreases, it becomes hard for the sense amplifiers to recognize which state is represented. Synertek designs its EEPROMs to meet a minimum of 1×10^4 endurance cycles. Endurance is word independent, and adjacent words are unaffected during endurance cycling.

Using EEPROMs effectively

The SY2802E can be used in situations where the system's memory addressing space is used up. This is often the case in systems using a Z8 processor or the like. Here, all memory addressing space is usually quickly filled. Because the company's EEPROM acts and looks like a peripheral to the processor, no memory address space is needed (Fig 5). The address and data are passed from the microprocessor to the EEPROM as two consecutive 8-bit data transfers. Address is contained in the first, data in the second.

A more sophisticated application for this EEPROM is possible in data collection and manipulation settings. In surveying, for example, maps and charts are made from readings often taken under severe conditions. Generally, 128 readings are taken over a 2-acre site. To enable mapping, a computer based device must have the means to measure distance by focus as well as by angle of tilt. These values along with rotation allow a map to be drawn.

By sampling location information, a microprocessor based unit can calculate angle, distance, and rotation in seconds. To make this function fully automatic, a nonvolatile EEPROM, configured as a register file, can be used to store the readings. Once the data are safely stored, the field unit incorporating EEPROMs can be connected to a base unit that has a printer. A typographic printout can then be quickly generated.

In a hypothetical sequence of operation, the start button (reset) is pushed. Then, the lens is focused (or an autofocus lens is used). While the rotation is being stored, the microprocessor reads the distance sensor. As soon as the first storage sequence is complete, the distance is stored. While distance is being stored, the angle sensor is read, and the height from ground zero is calculated. When the distance storage is complete, the height is stored. As soon as the height is stored, the unit shuts everything off until the start (reset) is pushed again.

Because this 256 x 8 EEPROM can store 256 (8-bit) words, it is ideal for this application. This chip provides designers with an alternative to the standard RAM versus ROM choice. The chip's nonvolatility, ease and speed of programming, and in-circuit programmability make it perfect for use in any portable data gathering device. In addition, applications that place components beyond the designer's reach, such as military or space systems, can also benefit from the remote programmability of modern EEPROMs. It seems likely that as portable systems proliferate, so will the EEPROM.

Acknowledgments

The author would like to thank Bob Salter and John Turner for their contributions to this article.

THE WINCHESTER BACKUP SYSTEM

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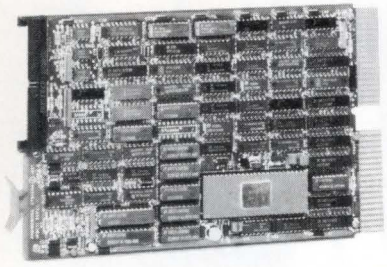
CIRCLE 104

GET THE POWER YOUR Q-BUS SYSTEM WAS DESIGNED TO GIVE

It's Plug-In Simple with Remarkable DEC-Compatible Technology from Andromeda Systems



The WDC11 Triple Function Compatible Controller: Its Power is Amazing Versatility

Interfaces with 8- and 5¼-inch Winchester and floppy disk drives, and includes an intelligent bootstrap ROM. This LSI-11 compatible Controller emulates these standard DEC devices: RK-05, RL-01/2, RP-02, RX02.

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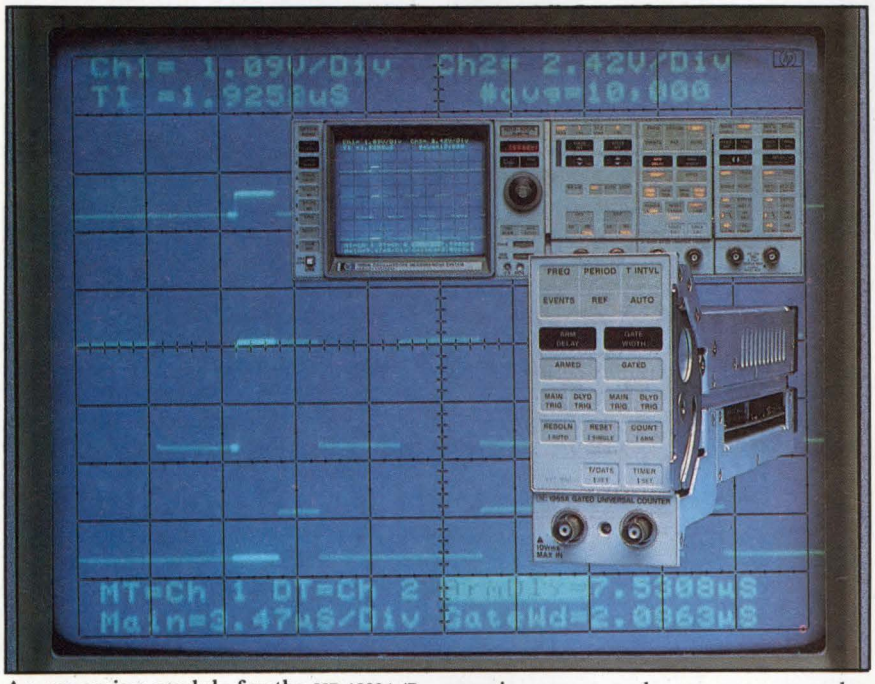
CIRCLE 105

Integral universal counter/timer upgrades oscilloscope



An expansion module for the HP 1980A/B oscilloscope adds the accuracy and counting modes of a universal counter to the setup and display capabilities of a programmable oscilloscope. The HP-IB programmable HP 1965A performs universal counting and gated timing measurements with 500-ps resolution, ± 10 ps. The combined, integrated system has a trigger view feature that eliminates measurement uncertainty and replaces the technique of externally gating a counter with an oscilloscope. Continuous calibration allows specification of any waveform portion as the interval to be measured; an additional waveform is generated on the display to show the interval being measured.

Without manual setup, the system measures rise time, fall time, pulse width, duty cycle, propagation delay, and phase shift. A menu-driven auto-parameter key provides a choice of accurate, repeatable measurements. The system finds absolute maximum and minimum, sets trigger levels, and measures time intervals for standalone applications. Timing measurements can be made on amplitude signals as low as 3 mV; trigger circuitry offers a wide dynamic range and measures complex waveforms with resolution to 40 μV.

Scope and counter measurement paths are characterized to each other to reduce systematic errors. Together, they make period and frequency measurements up to 100 MHz with 9-digit resolution. A time-interval function measures the time between user defined start and stop points. Typical time-interval measurements include time between edges of a complex pulse train and the propagation delay between a clock and a data stream.

Events functions, which are selected through soft keys defined by the oscilloscope's CRT, count the number of occurrences of one or more signals. Events functions can be used to detect glitches or intermittent pulses and include A (gated), A during B, ratio A/B, totalize A, totalize A + B, and totalize A − B.

Also accessed through the display menu, the reference function can zero all paths to the probe tip of the reference signal. This makes it possible to null out propagation delays caused by different cable or probe lengths. In addition, a known value can be set as a reference for frequency, period, time-interval, and events functions. Reference functions can also be set up manually when measuring variances or drift.

Unarmed, armed, and gated modes are generated using the scope's main and delayed sweeps. This gating capability makes it possible to specify the desired waveform interval for measurement. Burst frequency, time interval between pulse train edges, or propagation delay between specific edges on channels 1 and 2 can be measured.

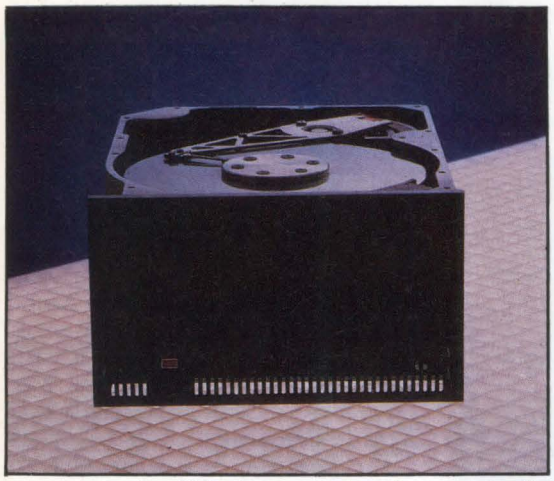
For accurate measurement-interval gating, arm delay positions the start of the intensified marker, and gate width controls the marker's duration. The system then calibrates readouts and measurements. Counting sources A and B can be assigned to main or delayed signals as channel 1, channel 2, external, or line.

Besides channel 1, channel 2, and trigger-view waveforms, the system will generate a count view showing the interval being measured on a realtime waveform. Measurement resolution can be selected based on the digits of resolution required and measurement time allowed. In auto-resolution mode, the counter/timer automatically selects the resolution to update measurement results every 2.5 s.

Other system features include a 50-setting alarm timer and a realtime, battery-backed clock displayed on the CRT. Two auxiliary BNCs on the counter provide a 10-MHz oscillator I/O and a TTL pulse for driving devices like a trace recording camera.

The HP 19800A waveform measurement library has software for automating time-domain measurements and performs statistical analyses on measurement results. Given the software library and full HP-IB programmability of both counter/timer and scope, many setup and measurement functions can be completely automatic. Moreover, the system can be set up from the front panel and the setup learned by a computer. The HP 1965A gated universal counter costs $2535; the HP 1980A/B scope is $10,500, and the HP 19800A waveform-measurement library, $1000. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 318

5¼″ Winchesters pack up to 380M bytes



EXT-4000 family disk drives employ the company's enhanced small disk interface (ESDI) to transfer data between disk and host computer at 10M bps. This is twice the transfer rate of the standard ST506/412 interface, and the company is actively working to make the ESDI an industry standard. Drives have capacities of 75M bytes (2 disks), 175M bytes (4 disks), 280M bytes (6 disks), and 380M bytes (8 disks). The fast transfer rate allows up to 14,873 flux changes/in.

A 2,7 run-length limited encoding scheme yields a bit density of 22,310 bpi, which is 50% higher than is possible with conventional MFM encoding. The drives use nonreturn to zero data transfer between drive and controller, since the data separator is on the drive itself—not on the controller, as in ST506 compatible drives.

Moreover, the family's Whitney-type ceramic composite head sliders are 33% smaller than the conventional Winchester sliders. They feature 2-rail construction, with the ferrite recording gap at the outermost edge. This design, in conjunction with the small slider size, allows a higher exploitation of the disk surface than with conventional Winchester heads.

Using plated media, the drives store 25.5M bytes per disk surface, with 1224 cylinders. Average access time is 30 ms. EXT-4000 members are designed with a spindle motor that allows up to 8 disks to reside within the 5¼″ form factor. Standard features include Maxtorq rotary voice coil actuator, closed-loop servo system with dedicated servo service, and Maxpak printed circuit board with surface mounted devices for control and read/write electronics.

In quantity-1000, the drives cost from $1295 to $3695 each, depending on capacity. **Maxtor Corp,** 5201 Lafayette St, Santa Clara, CA 95050. **Circle 319**

Color printers integrate text and graphics on plain paper

Series 200 EPM (Photo) employs a solid state raster line printhead that produces 200 dots/in^2 on smudge-free plain paper. Because the printer is based on nonimpact technology, it can be programmed to generate a virtually unlimited array of text and graphics characters and symbols.

The 8.27″ (21-cm) wide printhead has over 200 nibs/in, with an "all points addressable" feature for graphics. The printer processes up to 6 pages each minute—equivalent to about 300 lines/min. Built-in sheet feeder and output stacker manage paper flow.

Series 200 input is a 1-MHz video bit stream, which is buffered internally, then fed to the printhead one raster scan line (1680 pixels) at a time. The image is transferred to paper from the ink donor roll, which consists of thin backing material coated with a nondegradable dry ink. Thermal nibs melt the ink on the donor roll just before a pressure roller pushes it against the paper. Each donor roll produces up to 1300 pages.

A second release, the Series C ink jet printer, also uses plain paper—either cut sheets or rolls—and prints 20 cps with 120-dot/in^2 resolution. Clay coated paper can be used for high quality color printing. Ink dries on standard paper in 1 s.

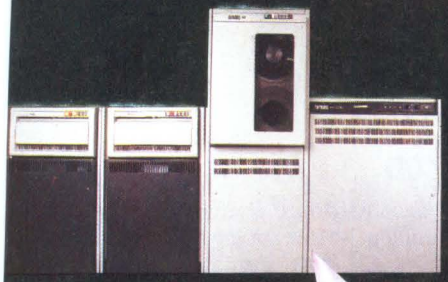
Sixteen-nozzle head featuring drop-on-demand technology can put a dot of ink virtually anywhere on the page. The desktop unit uses 4 nozzles for each of 4 colors to produce a total of 7: cyan, black, magenta, yellow, violet, green, and red. The ink jet generates color backdrops, halftones, multiple color intensities, and complementary imaging. Five halftone levels are available for printing graphics.

When printing text, the unit employs a 4-pass mode that generates 12 x 16 resolution; when printing special graphic mosaics or symbols, a 5-pass mode prints with 12 x 20 resolution. The 96-char ASCII set and 64 mosaic chars are stored in PROM. Besides the U.S. configuration, 5 standard European character sets are available: French, Norwegian/Danish, Spanish, German, and British.

Series C ink jet printers will be available in the 3rd quarter 1983, at about $1250. Series 200 EPM is available 90 days ARO and lists at $4995 quantity-one. **Diablo Systems, Inc,** 24500 Industrial Blvd, PO Box 5003, Hayward, CA 94545.
Circle 320

D/3D INTERACTIVE COLOR TERMINAL

MATROX GXT-1000



THE NEW MATROX GXT-1000 color graphics terminal delivers true 2D/3D interactive performance. It's fast. It's intelligent. It's high resolution. And it costs less than $10,000 in OEM quantities. Complete.

THE GXT-1000 TRANSFORMS, CLIPS AND DRAWS lines at speeds of up to 20,000 vectors / second. Area filled rectangles at 5000 rectangles/second. True 3D 1000 polygon pictures with hidden surfaces removed and shaded in 10 seconds.

HOST WORKLOAD AND COMMUNICATIONS ARE GREATLY REDUCED. The GXT-1000 allows the user to down load complete object data files, using 64K x 64K x 64K virtual co-ordinates, to local memory. The terminal contains up to 22 Mbytes of RAM and disk memory for local picture segment storage, (up to 2000 active segments). Once downloaded, all data manipulation and viewing can be performed locally, in near real-time, without host support.

HIGH RESOLUTION

- up to 1280 x 1024
- 4 to 16 video planes
- 256 color look-up table per surface
- 19" high res. color monitor
- interlaced or non-interlaced

HIGH SPEED

- 80286 graphics engine
- 6 pipelined slave processors
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HIGH PERFORMANCE

- 64K x 64K x 64K virtual addressing
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- local segment storage up to 1 Mbyte (2000 segments) in RAM
- full 2D transformations standard
- 3D with hidden surface removal and shading optional
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- host interface via RS-232, RS-422/449 or parallel DMA
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- complete interfaces for data tablet, optical mouse, printer & plotter
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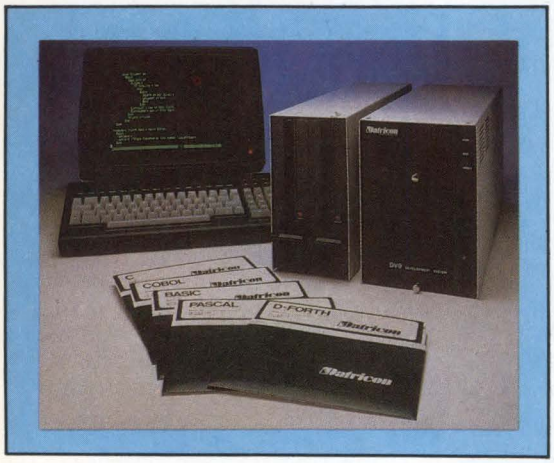
CIRCLE 106

STD-bus development system matches language to job



An advanced software development system gives board-level microcomputers a self-contained hardware/software environment for developing realtime applications. DV-9 features 2 independent STD-bus systems: a development computer and a target backplane. Dual-backplane architecture maintains a stable, full-function development system apart from the experimental target application. In addition, the system supports a software library offering Pascal, COBOL, BASIC, C, and D-Forth, as well as assembly language. In many cases, this lets engineers choose the language that best fits a particular application as well as their own language preference.

Development tools operate under OS-9, a modular operating system similar to UNIX that controls a full multi-user, multitasking environment. The system will generate ROM resident software based on either OS-9 or D-Forth. The development computer generates and maintains application source code and develops OS-9 based applications, while the target backplane configures application hardware and software.

Basic hardware configuration is built around a 2-MHz 6809 CPU. Hardware includes 62K-byte memory; 3 serial I/O ports; 32 bits of parallel I/O; two 1.1M-byte double-sided floppy disk drives; a floppy disk controller for up to 4 drives; an EPROM programmer for JEDEC 2716, 2732/A, and 2764 devices; and the front-accessed target backplane.

Standard software comprises the OS-9 modular operating system, BASIC09 interpreter/compiler, macro text editor, 6809 assembler, and interactive debugger. System prices start at $7500; high-level language compilers cost from $125 to $400 each. The system complies with FCC class A regulations on radiation emission. **Datricon Corp,** Datricon Plaza, 155 B Ave, Lake Oswego, OR 97034.
Circle 321

LSI based networking microcomputer

Entering the microcomputer market with its microSystem 6/10, Honeywell is touting a compatibility range that brings mainframe data communications networking power to the single-user microcomputer level. The 16-bit machine is hardware and software compatible with the company's 16- and 32-bit DPS 6 minicomputers and runs applications developed on those systems. It can serve as an end point in a distributed data processing network with Honeywell or IBM host computers, or as a complete standalone system.

Firmware-controlled LSI Micro 6 CPU is fully compatible with the DPS instruction set. In addition, the microcomputer runs menu-driven General Comprehensive Operating System (GCOS) 6 MOD 400, Release 3, which is used on the larger DPS 6 and Level 6 minicomputers. Program development capabilities include full-screen editor and ANSI standard FORTRAN, BASIC, COBOL, and Pascal. Moreover, an 8086 processor option plugs into the system's base logic board to support MS-DOS, CP/M 86, and a wide range of application software.

The computer has 128K-byte main memory expandable to 512K bytes: one or two 5¼" diskettes store 650K bytes each (formatted). The desktop version field upgrades to a floor model that provides another 20M bytes of Winchester disk storage as well as support for a second video workstation.

A separate processor controls I/O and provides full functional compatibility with DPS peripheral systems. Two RS-232-C/RS-422-A asynchronous ports and an optional synchronous port are supported. The synchronous port communicates with Honeywell's distributed systems architecture (DSA) and non-DSA Honeywell hosts, as well as with IBM hosts that use BSC and SNA protocols. The computer also supports public and private X.25 packet-switching protocols that access public data and value-added networks. Character-synchronous or bit-synchronous protocols are supported in half- or full-duplex modes.

An antiglare 12" (30-cm) green phosphor screen offers 720 x 300 resolution in an 80-column x 25-line display. A character generator table contains up to 256 symbols that are software loaded to accommodate different character sets. The ergonomic design features tilt and swivel monitor base and reprogrammable detached keyboard with color-coded function keys. Desktop microSystem 6/10 configuration starts at $3995; hard disk model starts at $9995. **Honeywell Information Systems Inc,** 200 Smith St, Waltham, MA 02154.
Circle 322

adac...

The leader in LSI·11 I/O interfaces now offers software to match.

ADAC offers the widest selection of complete LSI-11 systems and function cards... both analog and digital. And now two new software subroutine libraries support all of ADAC's extensive line of interfaces for LSI-11. ADLIBRT is fully compatible with RT-11 (single user) real-time operating system software. ADLIBRSX enhances RSX-11M (multi-tasking/multi-user) operating system software.

Both ADLIB packages are simple to use, yet powerful, software tools that slash the time needed for program development.

ADLIBRT and ADLIBRSX support:

- mV Level A/D Conversion
- Temperature Measurements
- High Level, High Speed A/D Conversion
- TTL Level Digital I/O
- Discrete, High Voltage, AC/DC Interfaces
- Pulse Counters and Pulse Trains Out
- Optically Isolated Discrete I/O
- Contact Closure Sensing
- Discrete High Current Outputs
- Programmable Clock
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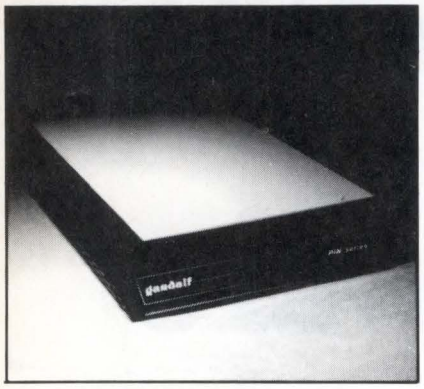
CIRCLE 107

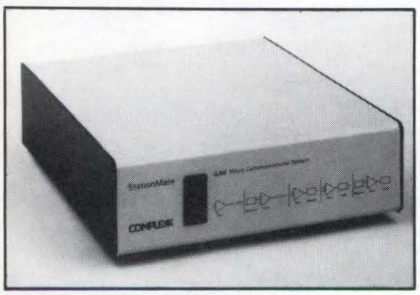
Stat MUX provides data protection



Statistical multiplexer PIN 9106 was developed for async minicomputer systems requiring error correction from remote terminals or printers. Two async channels can operate at up to 9.6k bps; 4 channels at 4800 bps. Combined data rate is 19.2k bps, while composite link operates at 9600 bps sync or async. Multiplexer is compatible with 212-type 1200-bps full-duplex modems, and features 2K-byte buffer, menu-driven parameter selection, and LED diagnostic indicators. **Gandalf Data Inc,** 1019 S Noel, Wheeling, IL 60090.
Circle 323

Micro/mini datacom

StationMate is a data communications system consisting of a stat MUX; an intelligent modem with auto-dialing; and a LAN interface, XLAN, which supports 64 devices over a 5000′ (1524-m) bus. System is Bell X.25 compatible and has 3 data ports with RS-232-C connectors. Other features include 16K-byte segmented buffer, auto baud, diagnostics, menu-driven setup and configuration with password security, and error-free data transmission with detection and retransmission on error. System is priced at $1450. **Complexx Systems, Inc,** PO Box 12597, Huntsville, AL 35802.

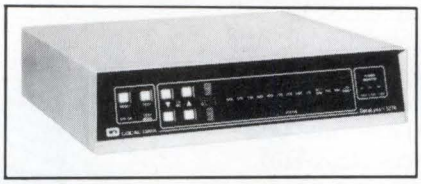


Circle 324

PBX voice/data modem

Full-duplex, 2-wire ComNet 48 provides sync and async data communications at 4.8k bps, and isochronous operation at 300 to 1.2k bps. Use of existing twisted pair wires eliminates need for a central switch, additional cabling, and changes to the main distribution frame. The unit plugs directly into an existing wall telephone jack, and features auto-answering of terminals and computer ports. As a standalone unit, ComNet 48 rackmounts to accommodate 12 modules in one 8.75″ x 19″ (22.23- x 48-cm) cage. **Avanti Communications Corp,** Aquidneck Industrial Park, Newport, RI 02840.
Circle 325

Protocol link to small computers

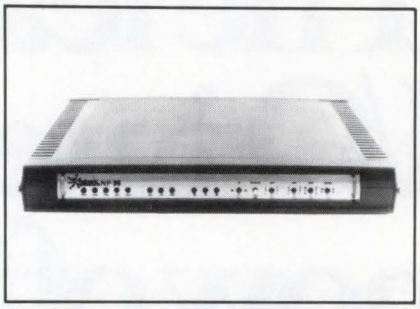


Stored on a 5¼″ floppy diskette, a software package enables small computers to emulate the IBM 3278 bisync display terminal when attached to a DataLynx/3270 or /3274 protocol converter via dedicated or dial RS-232-C series port. The program also allows a computer to emulate the ADM3A terminal. Moreover, it permits an IBM PC to operate at 9.6k bps, and includes menu options for 300-, 1.2k-, 2.4k-, 4.8k-, or 9.6k-bps operation. **Local Data,** 2701 Toledo St, Torrance, CA 90503.
Circle 326

Compact component modem

Mounting directly into a PCB, CH1760 is an 8 in^2, Bell 212A compatible modem. In component form, the modem offers a TTL host interface that allows the host to send serial async commands over serial lines. As an intelligent modem, it provides call progress tones and 6 dialing procedures. The component stores a 32-digit last number dialed, but supports an external RAM port for storing up to 52 additional numbers or log-on messages. Other commands include 8 diagnostic test modes, voice/data switching, and data transparency. Priced at $495, volume discounts are available. **Cermetek Microelectronics,** 1308 Borregas Ave, Sunnyvale, CA 94086.
Circle 327

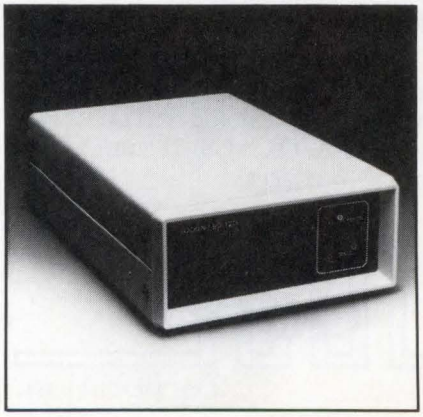
Single-board sync modems



Two sync modems, NP-96 and NP-48, provide baud rates of 9.6k and 4.8k bps, respectively. Designed for full-duplex, point to point applications, modems are CMOS-LSI implementations of QAM modulation, phase jitter compensation, and equalization techniques. Front panel indicators display line status and diagnostic and configuration information. The NP-96 provides fallback rates of 7.2k and 4.8k bps when line conditions do not support the full rate. The NP-48 sells for $1800, the NP-96 for $2750. **Network Products, Inc,** Research Triangle Park, NC 27709.
Circle 328

Network stat monitor

LocalNet 50/120 statistical monitor connects to a network via an RS-232-C interface. Users specify time periods for the screen to display cumulative information and peak data value on data packets transmitted, characters sent, sessions connected, and channel usage. This allows flexibility to monitor network conditions and optimize network traffic. Monitor uses standard ASCII terminal and 1-page 24 x 80 format. **Sytek Inc,** 1225 Charleston Rd, Mountain View, CA 94043.



Circle 329

THE BUS STOCKS HERE:

PSM-512A: 512 kbyte Multibus™ memory with ECC, 275 nsec access time. Fixes single-bit errors, flags multi-bit errors.

CIRCLE 108

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CIRCLE 109

PSM6463: 64 kbyte non-volatile CMOS Multibus memory, 200 nsec access time. 350 hour standby with on-board rechargeable NiCd's, 8 years with lithium. For process control, telecommunications, other critical applications.

CIRCLE 110

NEW PSM1VA: 1 megabyte VERSAbus™ memory with ECC, 300 nsec access time. Lots faster and much less expensive than Motorola and IBM equivalents. Full 32-bit VERSAbus compatibility.

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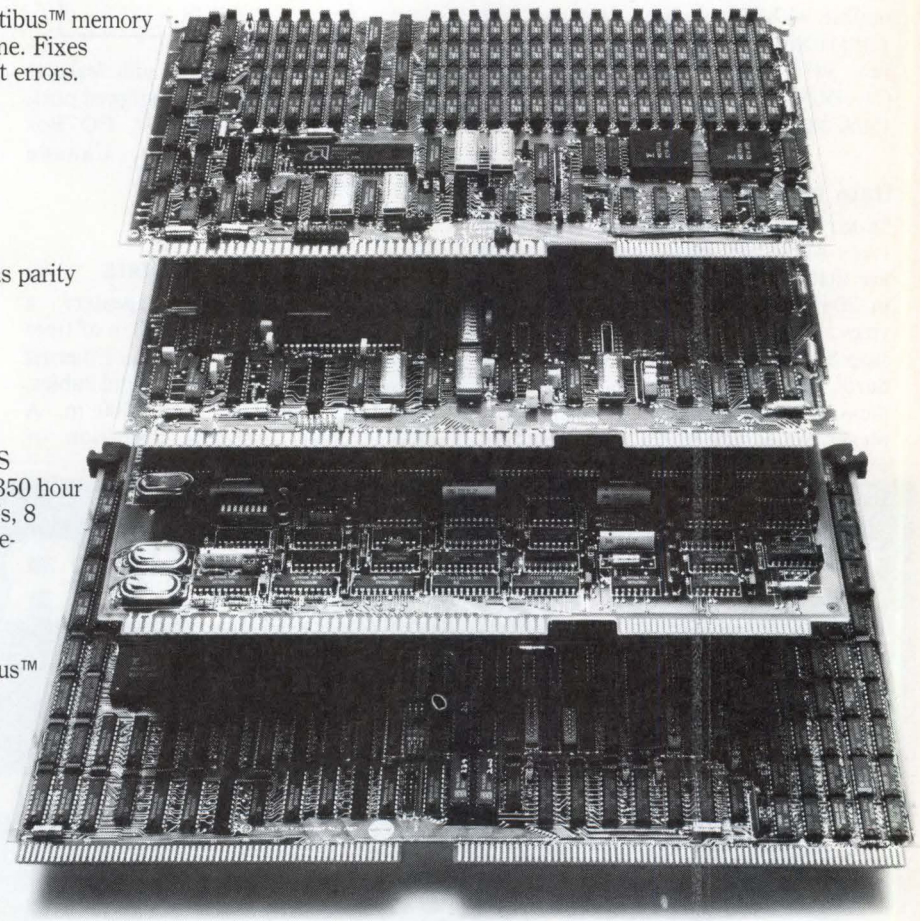

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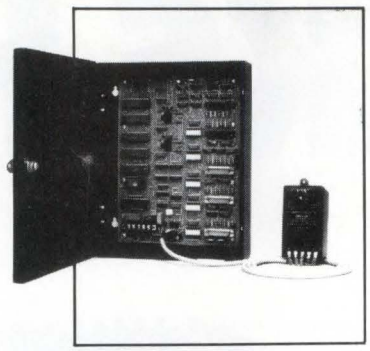
Digitizer improves voice quality

Series 1000 voice digitizer converts voice to digital bit stream for full-duplex transmission. Digital interface is RS-232-C and voice interface is PBX tie or other voice channel. Speech, data, and several voice channels can be transmitted simultaneously using multiplexers. Built-in diagnostics from the board to system level via keypad or loop-back configurations are standard. Digitizer is compatible with other series 1000s and with TSP 100/200. **Time and Space Processing, Inc,** 3410 Central Expy, Santa Clara, CA 95051.

Circle 330

Data multiplexer for PABX

SX-200® and SX-100® divide output from a PABX RS-232 port into 4 categories. Data are then transmitted via RS-232 interface or 20-mA loop to separate terminal devices. Programmable character length, stop bits, baud rate, and parity are standard features. Housed in a compact, locking metal cabinet, the data multiplexer comes with its own power supply.



If commercial power fails, unit features data "cut through" to preassigned port. **Mitel Corp,** 350 Legget Dr, PO Box 13089, Kanata, Ontario, Canada K2K 1X3.

Circle 331

Ethernet network repeaters

When used with local repeaters, a remote unit allows up to 1000 m of fiber optic cable to be added to the Ethernet network between any 2 baseband cables, extending the network to 2500 m. A local repeater prevents distortion of information traveling more than 500 m over baseband cable segments. Both versions operate at a 10M-bps data rate. The local repeater is $2500 and the remote repeater (including a local repeater), $7700. **Ungermann-Bass Inc,** 2560 Mission College Blvd, Santa Clara, CA 95050.

Circle 332

High speed modem

The Data Mover V.29 modem operates at 9600 bps. Its manufacturer claims that using it for data transmission over a leased line for one hour per day over a 5-day week (48-week year) is cost competitive with using lower speed modems to send data over the PSTN. The Data Mover incorporates a single PCB that makes extensive use of CMOS LSI circuitry; the calculated MTBF exceeds 30k h. Seven front-panel LEDs indicate operational status, and routine system diagnostics can be carried out via three PCB mounted switches. **Easydata Ltd,** 7 Carleton Rise, Welwyn, Herts AL6 ORP, England.

Circle 333

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We're the largest producer of electro-magnetic digitizers. So we can deliver field proven tablets in the quantity you need... when you need them.

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  The pressure sensing pen option gives the operator a more natural input... perfect for the artist.
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  The 4D option provides another independent variable proportional to stylus tilt and direction ... like a joy stick.
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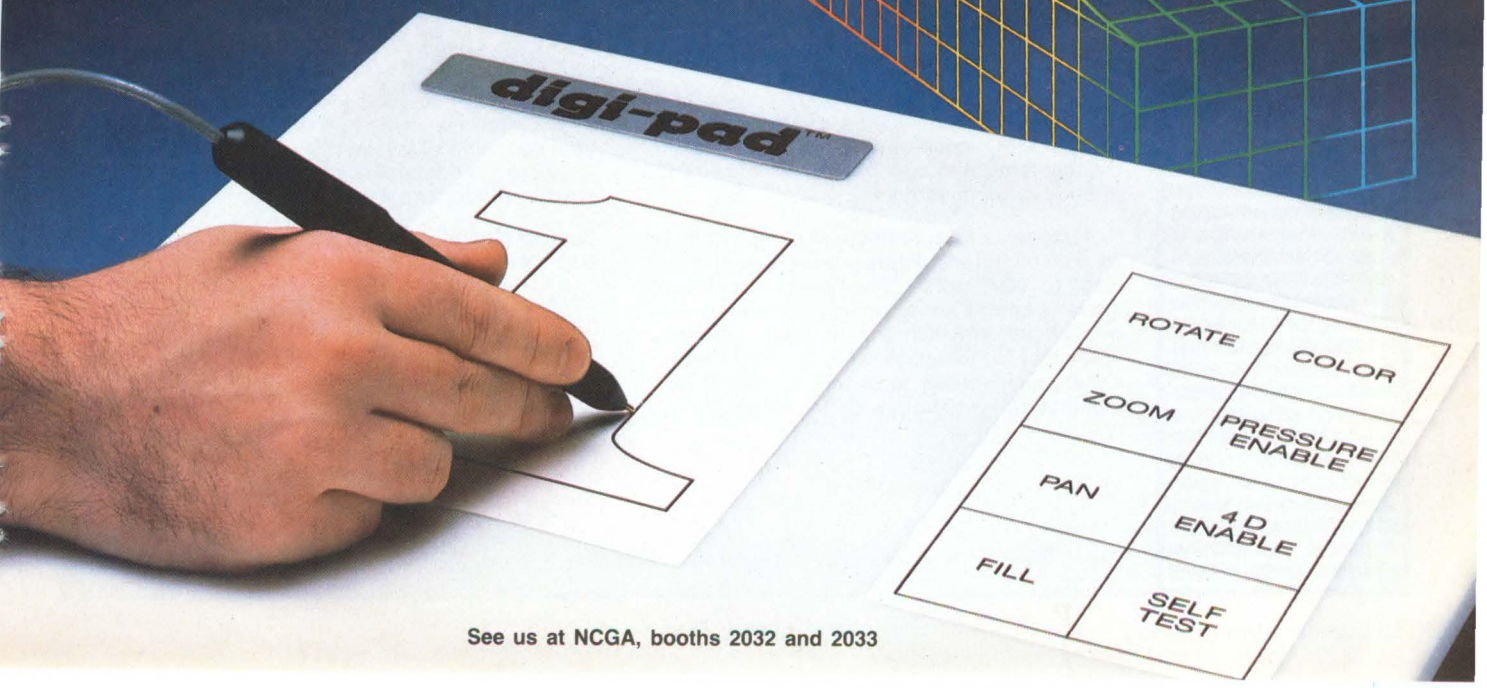
  A 4-tone alarm reports test results for all components including the tablet grid... insuring digitizer integrity.

Every Digi-Pad is compatible. So when you develop your software and interface around our smallest and least expensive Digi-Pad (under $1000), you can interchange any other size Digi-Pad without redesign. Digi-Pad is also compliant with U.L., FCC and many other standards.

Give your system an edge. Choose the number one digitizer from GTCO. Call us at (301) 279-9550 today.



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CIRCLE 113

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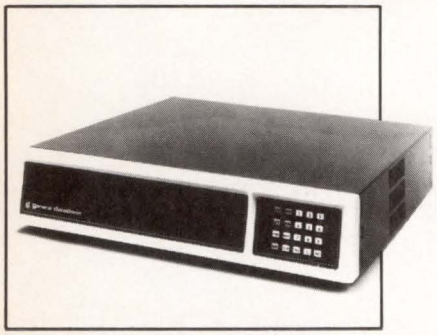
Network multiplexer



GEN*NET 1262 is an async/bisync network multiplexer. Design includes 168k-bps speed on 4 composite links, high buffer storage, and 96 channels. System is available in 8- or 24-channel models. Multiplexer has a supervisory port and provisions for auto retransmission of data on error. All link and channel characteristics are selected and set individually for flexibility. Channel priority, diagnostics, and password protection are also featured. **General DataComm Industries Inc,** 1 Kennedy Ave, Danbury, CT 06810.
Circle 334

Small DDP office system

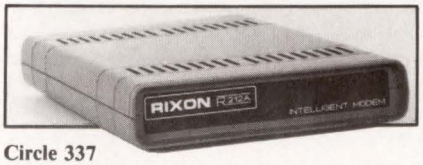
With multifunction capabilities, model 565 is a small cluster distributed data processing system. It provides a Winchester disk drive and streaming cartridge tape backup, and supports 4 terminals. Hardware capabilities include up to 512K bytes of memory; 185-ns, 6-MHz processor speed; and communications support. Operating system, interpreter, and 25 utilities are part of the software, while word processing, text editor, and compiler are optional. **Northern Telecom Inc,** 259 Cumberland Bend, Nashville, TN 37228.
Circle 335

VAX Ethernet connection

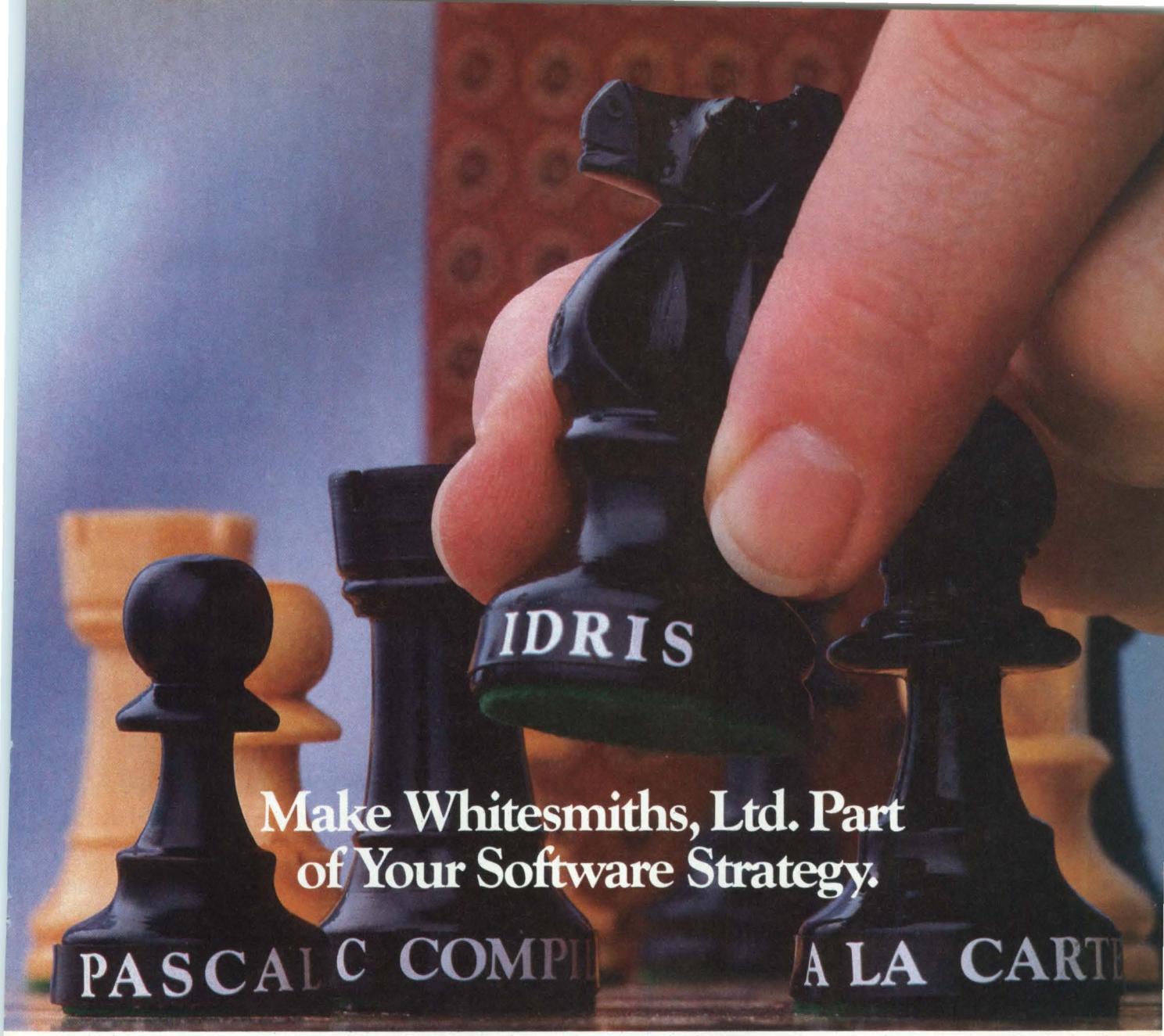
DEUNA, Ethernet-to-Unibus communications controller, is a microprocessor based design for maximum throughput with minimum host intervention. Controller implements channel access and data link management functions. Onboard diagnostics detect device errors and provide simple isolation. Loop-back diagnostics allow more detailed isolation. With 32K-byte buffer space, the unit is priced at $3500 and is scheduled for delivery in July. **Digital Equipment Corp,** 146 Main St, Maynard, MA 01754.
Circle 336

Intelligent modem

R212A is an auto-dialer modem that can store up to 10 phone numbers, each with an accompanying 30-character description. With HELP commands, user can dial from the keyboard or use a single keystroke to dial from the memory. If line is busy, modem can automatically link to an alternate number or redial the last number dialed, even if the number is not in memory. Software allows all option settings and test features to be controlled from the keyboard. Priced at $495, modem is Bell compatible (212A, 103, 113) and has battery protected memory. **Rixon Inc,** 2120 Industrial Pkwy, Silver Spring, MD 20904.



Circle 337



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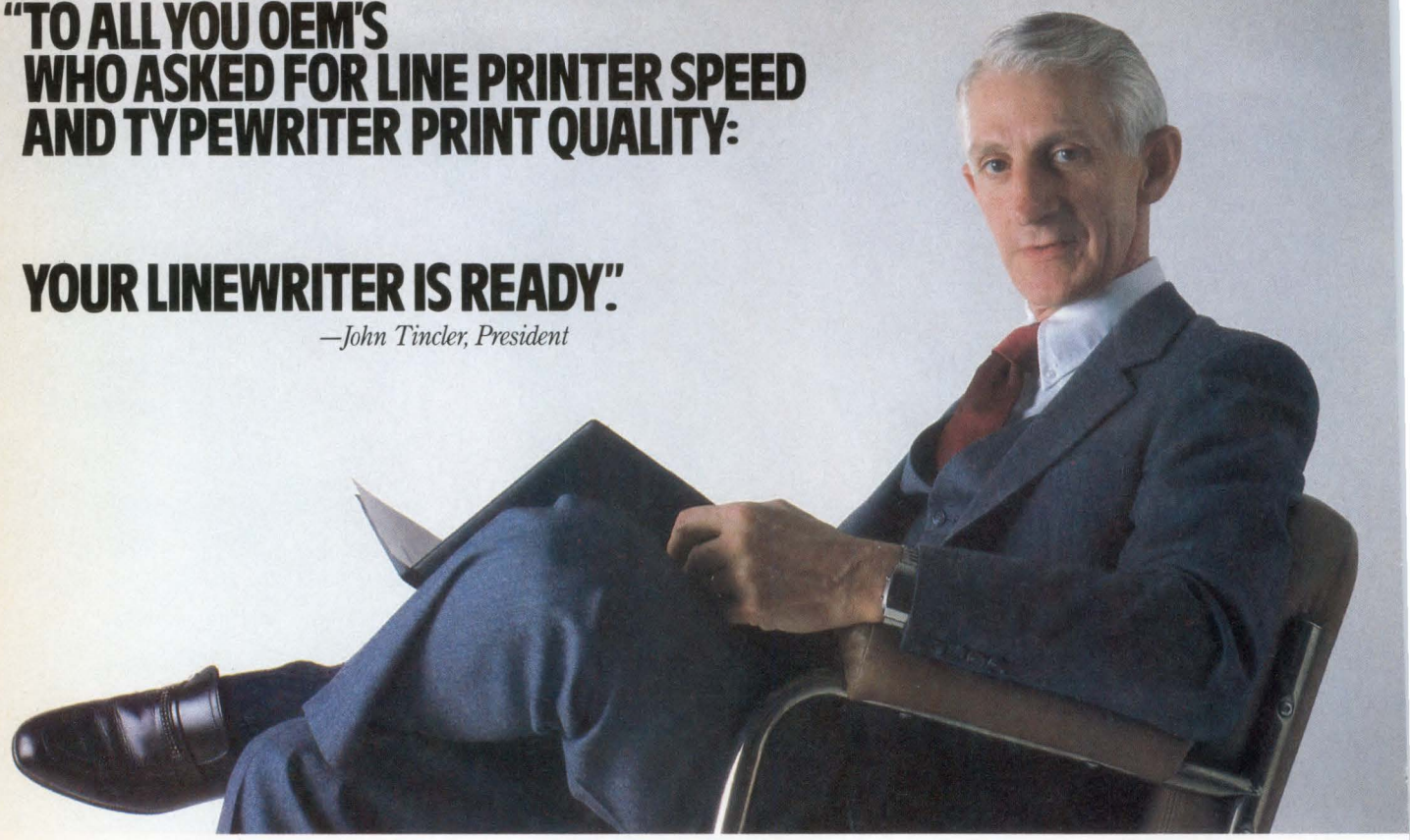


Recently we asked what you wanted most from the next generation of line printers. You told us in no uncertain terms: typewriter quality print at line printer speed; more reliability and less need for service.

So we built it—a printer that embodies everything you want and eliminates everything you don't want.

We built *your* line printer. The Centronics Linewriter 400.

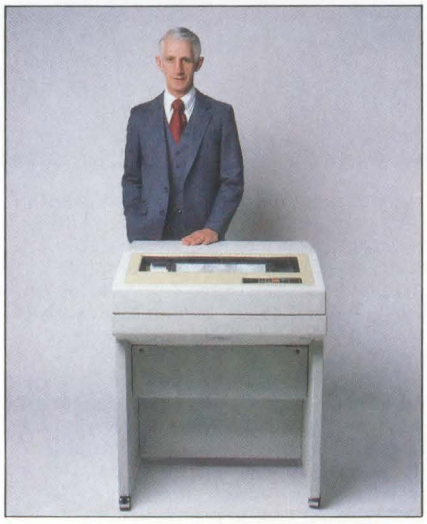
We can't describe the superior print quality—so we'll let you judge for yourself. Just look at the unbelievable difference between the Linewriter 400 and standard band printer samples.

Sample of Linewriter 400 quality.*

Sample of standard band printer quality.*

On top of that, the Linewriter is smaller, quieter, easier to operate and maintain, with the lowest cost of ownership of any 300-500 LPM line printer ever made.

To build the Linewriter, we developed some proprietary innovations that redefine established line printer technology.



These include true linear free-flight hammers to eliminate character clipping (especially on multi-part forms); and slower, clockwise band rotation to reduce character smudging.

For reliability—LSI and VLSI electronics and up to 15 KV ESD immunity throughout. To improve throughput we included statistical printbands and early end of print. Then we finished it off with human-engineering features: extensive self-diagnostics and an alphanumeric display to pinpoint specific problems; resonating ribbon cassette that doubles ribbon life; 2860 hr. MTBF; 0.5 hr. MTTR and *no scheduled preventive maintenance,* plus a 55 dBa (optional) sound level.

The result is the Linewriter 400—the line printer that makes every other 300-500 LPM printer obsolete.

Which is no less than you should expect in a line printer you had such a large part in specifying. And one it took Centronics technology to build.

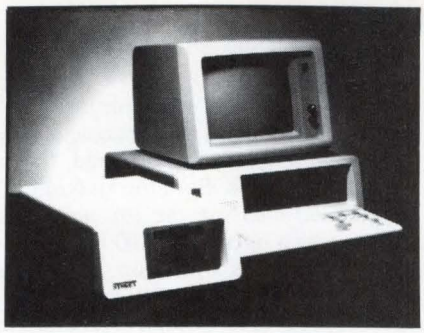
To find out more about the Linewriter 400 call our Line Printer Division (313) 651-8810, Ext. 342. Or write to us for more information and free print samples to Centronics Data Computer Corp., Dept. A, One Wall Street, Hudson, NH 03051.

*Offset reproduction.

CENTRONICS® PRINTERS

CIRCLE 115

Cassette backup Winchesters



II-10 (10M bytes) and II-20 (20M bytes) are Winchesters for the IBM PC. Featuring a high speed streaming tape cassette backup, the systems can be user configured in up to 10 logical volumes under PC DOS and up to 14 logical drives under CP/M-86. Utility programs include preserve, which saves and restores data on volumes in image fashion. Also included is filesave, which saves and restores data as single files or sets of files. Storage systems allow DMA operation and parity and error checking. The II-10 is priced at $2995; the II-20 is $3795. **Sysgen Inc,** 47853 Warm Springs Blvd, Fremont, CA 94539.
Circle 338

Memory subsystem increases VAX capacity

Memory modules contain 64K-bit chips to increase VAX-11/780 main memory to 32M bytes. Memory subsystem contains memory controller and array boards that plug into the memory backplane. Existing systems users can upgrade memory through the controller and array boards or through the expansion cabinet. Prices, with controller, range from $28,900 for 2M to $36,000 for 4M bytes. Memory modules, sold in 2M-byte increments, range from $9000 for 2M to $34,000 for 10M bytes. **Digital Equipment Corp,** 146 Main St, Maynard, MA 01754.
Circle 339

Board expands 8086 memory

VLS-C memory system expands capacity by 24 times and increases operating performance of 8086 based single-board computers by 50%. Both ports can access 1.5M bytes of ECC RAM with 450-ns cycle time and 250-ns access time. Board is supplied with contiguous and/or noncontiguous addressing, memory mapping, paging, and 32K-byte segmentation through 16M-byte range. Error status is displayed by onboard LEDs and through status registers. Basis for future cache memory implementation is available. All semiconductor components are in sockets for easy repair. OEM prices range from $1395 for the 512K to $3895 for 1.5M-byte system. **Advanced Digital Technology,** 696 E Trimble Rd, San Jose, CA 95131.
Circle 340

Floppy/Winchester memory system

Multibus compatible, 5¼" floppy/Winchester Stacpac module provides a 500K-byte double-sided floppy drive and either a 40M- or 20M-byte Winchester. Two controller/interfaces are available: 5215 handles 5¼" Winchester and floppy and ¼" streaming tape; 5217 adds file-oriented tape transfer capability. Prices for the floppy/Winchester module begin at $3895; controller/interfaces begin at $950. Volume discounts are available. **Data System Design, Inc,** 2241 Lundy Ave, San Jose, CA 95131.
Circle 341

Q-bus compatible memory

PINCOMM 23S+ memory card has 1M-byte "quad-wide" CSR parity and uses 64K RAM technology. It is compatible with the DEC Q-bus series, PDP-11/23S, and other DEC Q-bus or extended Q-bus computers. PINCOMM 23S+ has double the capacity of the DEC MSV11PL (M8067) and can be installed in H9273-A or DDV11-B backplanes. Its 22-bit addressing capability needs only 4 slots to allow user to add memory to complete the 4M-byte range. All board functions are switch selectable. Memory capacity ranges from 128K to 1M bytes. The 18-bit wide memory is organized with two 8-bit data bytes and two byte parity bits. **Trendata Corp,** 3400 W Segerstrom Ave, Santa Ana, CA 92704.
Circle 342

Magnetic tape drive

A compact magnetic tape drive equips medium-sized IBM computers with many performance and storage capabilities of the company's larger units. IBM 3430 magnetic tape subsystem offers about 3.5 times the data rate and storage capacity of the current comparable model, the 3410. The device can operate with the IBM System/38 models 4, 5, and 7, as well as with virtual storage System/370 models 135 to 168, and 303X and 4300 processors. **IBM Corp, Information Systems Group,** 900 King St, Rye Brook, NY 10573.
Circle 343

High-density memory boards

A high density Multibus-compatible DRAM module with 197-ns access time and 303-ns cycle time (typ), the TMM40020 comes with up to 512K bytes of onboard RAM. The device provides memory expansion for all Intel iSBC80 and iSBC86 systems and can be upgraded to 2M bytes. Available with or without parity checking, the unit complements the TMM40010A, a Multibus-compatible module that includes std error detection and correction onboard. The TMM40020 operates in an address space of up to 16M bytes and supports word transfers, as well as high, swap, and low-byte transfers. **Texas Instruments Inc, Semiconductor Group,** PO Box 401560, Dallas, TX 75240. **Circle 344**

Winchester subsystems

Available in 16M- and 24M-byte capacities, the ISIS-II-compatible DataSafe Winchester subsystem can be placed directly on top of Intel Series II and III (or MDS-800) development systems. This allows engineers to increase their development system's speed and capacity without sacrificing bench space. The subsystems automatically protect data during power failures without special power-down sequences. The portable units can be moved without mechanical interlocks or other special precautions. Prices are $6500 for the 16M-byte version and $7995 for the 24M-byte model. **Winchester Systems Inc,** 14 Laurel Hill, Winchester, MA 01890. **Circle 345**

Streaming tape subsystems

MTS-1012/130 and MTS-1012/150 are 0.5″ (12.7-mm), 9-track, 1600-cpi, IBM/ANSI/ECMA and ISO-compatible magnetic tape systems for DEC's Unibus and Q-bus computer systems. Both the 130 (Unibus) and 150 (Q-bus) use the IDT series 1012 Virgo, which operates at 100 ips streaming and 12.5 ips start/stop. All drives support up to 10.5 reels. Features include 160k-byte/s data transfer in streaming mode, over 6500 hours MTBF with diagnostic and self-test, DEC TM-11/TU-10 emulator, and IBM and DEC packing in either byte or word transfer. Unit price is $6495. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117. **Circle 346**

INTERFACE

4-function IBM card

SystemCard for the IBM PC features serial and parallel interfaces, up to 256K bytes of RAM, and a calendar/ clock with battery backup. Centronics-type parallel interface includes a print spooler buffer memory that allows use of the computer while printing a document. Async serial interface allows hookup to std remote data transmission terminals, modems, or letter quality printers. The device comes with either 64K or 256K onboard RAM. Disk emulator software is included. **Microsoft Corp,** 10700 Northrup Way, Bellevue, WA 98004.
Circle 347

STD bus board

Z80 Smart Card operates with a 4-MHz Z80A processor; includes RAM, ROM, serial I/O, and diagnostic firmware; and is RS-232 compatible. Onboard switch selects either standard or STD bus diagnostic unit processor mode; programs can be executed in either mode. In processor mode, card acts as regular CPU and can drive additional memory or I/O cards. In diagnostic mode, it will test any card in the system with functions such as display/alter memory, test keyboard, test RAM, and read/write to I/O port. In quantities of 2 to 9 the card is $245. **Forethought Products,** 87070 Dukhobar Rd, Eugene, OR 97402.
Circle 348

Serial coupler

A microprocessor controller board designed to be used as a remote data acquisition and control unit, the SBC6803 includes one serial port for communication with a host controller and two 8-bit parallel I/O ports configured for use with its manufacturer's APB family of signal-conditioning subsystems. The serial port can be set for baud rates ranging from 150 to 9600; a plug-in adapter furnishes RS-232 and RS-422 interfacing. Parallel ports allow the unit to handle a wide range of analog and digital I/O tasks. **Micro-Mation Inc,** 2615 W Casino Rd, Bldg 3D, Everett, WA 98204. **Circle 349**

Color graphics controller

Based on a 16-bit microprocessor with 128K bytes RAM and 64K bytes PROM, Model One/25 color graphics controller is suited for imaging applications. Supporting image memory configurations of 512 x 512 with 24-bit planes, controller allows data to be represented in 16M colors. A pixel mover and DMA are available for high speed data transfers. Software features include integrated debugger, HELP facility, local command interpreter, and 4014 emulator. With applications in business graphics and CAD, the controller sells for $10,500. **Raster Technologies, Inc,** 9 Executive Park Dr, North Billerica, MA 01862.
Circle 350

S/H board is LSI-11 compatible

DT3368, a simultaneous sample/hold (S/H) analog board, has 12 channels and dual-port architecture for LSI-11 based systems. User can freeze 12 analog values within a ± 5-ns aperture uncertainty interval. A-D conversions occur at 100-kHz throughput rates. Two DMA transfer paths are available: the standard LSI-11 bus and an external port that is compatible with DT3369 dual-port RAM/controller board. Suited for signal processing, simulation, and materials testing applications, the board sells for $3295; RAM board is priced separately starting at $1675. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752.
Circle 351

Temperature controller

A temp controller, 8203 RIOS, designed for use with a video terminal or computer, provides 8 temp input channels. Each channel has 0.25 °C resolution over a 60 °C span and is user adjustable from −55 to 150 °C. Controller incorporates a microprocessor, 4K bytes of EPROM, and 2K bytes of optional EEPROM. Up to 64 remote stations with 1024 separate control points can be directed from as far as a mile away. Controller will be available at a single-quantity price of $400. **Crydom, div of International Rectifier,** 1521 Grand Ave, El Segundo, CA 90245. **Circle 352**

New panel printers: ordinary paper is one of many smart benefits

Plain paper
Digitec's new family of panel mount printers uses plain paper. Benefits: It's inexpensive and readily available. It won't gum up the printhead as thermal and electrosensitive coated papers can. Your output is crisp, easy to read, won't fade. It reproduces.

OEM applications
New Model 6610 is $150 below competitive units. It's the first panel mount printer to feature a true RS-232-C/20mA I/O. Benefit: standard port permits easy interface with computers, controllers —any serial device, including the new generation of μP-based DPIs.

New Model 6620 with byte serial port offers off-the-shelf compatibility with byte serial computers and peripherals.

Both new 24-column OEM printers feature an exclusive, optional 2K nonvolatile buffer. Benefits: large bursts of data can be accepted without slowdown. Battery backup prevents data loss in power outs. Get more speed and reliability than other panel printers offer.

Since our new OEM printers are μP-based, application-matching is easy. Graphics? Just tell us what you require.

- Use plain roll paper.
- Drop-in replacement for thermal and electrosensitive panel printers.
- DIN size adaptable.
- Choice of serial, byte serial, and BCD inputs for easy interface.
- μP-based for custom OEM application.
- Programmable and addressable dot matrix printing; graphics.

New DPI printer
For replacement or new panels, 16 or 22 column Model 6630 with parallel BCD input interfaces directly with most digital panel instrumentation. Half the price of competitive designs, the 6630 offers you the full value of our new printer technology.

An exclusive battery-backed program clock option lets you print calendar headers, real time, or both. It can also trigger timed readings from DPIs.

Request Bulletin 4400, or call for demonstration.

Contact Digitec. **513-254-6251**

Digitec Corporation
918 Woodley Road, P.O. Box 458
Dayton, Ohio 45401-0458
Telex: (310) 687-4219

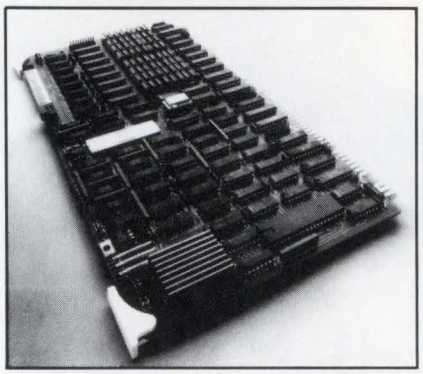
DigiTec®

CIRCLE 117

DMA interface

The GPIB-796 is a Multibus to IEEE-488 interface that supports DMA transfers to/from Multibus memory in 64K bytes at 500k bytes/s. Memory addressing capability lies in a high speed 24-bit counter that allows the user to place buffers in memory regardless of size. Present software package is compatible with UNIX operating system; other modules will be available written in C and microprocessor assembly languages. Provided with full documentation, the interface is priced at $1295 with OEM discounts available. **National Instruments,** 12109 Technology Blvd, Austin, TX 78759.
Circle 353

Compact graphics controller



The HRG2 packs a high resolution color graphics controller on a Multibus board. Hardware capabilities include 5K-byte video RAM, 80-MHz video output, 16-color simultaneous display, DMA interface, and up to 2M pixels/plane. Analog and digital output formats are provided. With the addition of a multiplane controller board, multiple HRG2 boards can be used to create a 256-color raster display. Std configuration is 1K x 1K x 4 (interlaced); additional overlay plane on daughterboard is optional. **Ikier Technology, Inc,** 42 Pleasant St, Watertown, MA 02172.
Circle 354

Z8 BASIC controller board

Based on the Zilog Z8671, a Z8 computer/controller comes with a BASIC interpreter, up to 6K bytes of RAM and EPROM onboard, an RS-232 serial interface with switch-selectable baud rates, and 2 parallel ports. The self-contained board expands to 124K and is optimized for use as a dedicated controller. CRT terminal connection allows immediate programming in BASIC or machine language. **The Micromint, Inc,** 561 Willow Ave, Cedarhurst, NY 11516.
Circle 355

Q-bus and Multibus interfaces

Interface cards integrate model 521 high resolution display and digitizer/viewer systems with Q-bus and Multibus computers. The 4 interface registers appear as contiguous memory locations including 1 for image data and command register, and 2 to address image memory. Multibus interface is equipped with prefetch/delay store to increase data transfer speed. Each interface is one bus load to the host and at $1995 includes interconnecting cable and documentation. OEM discounts are available. **Datacopy Corp,** 1070 E Meadow Cir, Palo Alto, CA 94303.
Circle 356

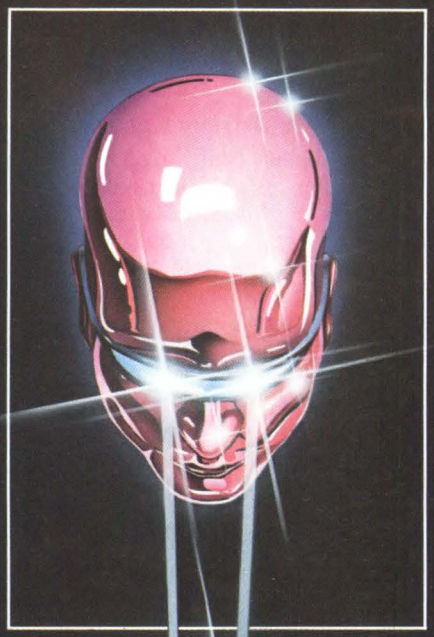
The Convergence Factor.

Convergence: the single most critical factor in color CRT performance.

Until now, Delta-gun tubes were the best way to achieve near perfect convergence, but only with costly adjustment electronics. Meanwhile, many in-line tubes are plagued by perceptible misconvergence. Which can lead to poor picture quality. A poor quality image for your product. And poor, bleary-eyed operators.

The Panasonic achievement: low cost in-line color CRTs with better-than-Delta convergence performance.

Without complex adjustment electronics . . . and none of the convergence drift inherent in active correction systems. At last, high resolution in-line tubes with stable performance that stands up to the ravages of time and tough office/industrial environments.



How did we do it? With a preconverged in-line tube/yoke combination unlike any other. Our precision S/ST (saddle/saddle toroidal) deflection yoke is ideally matched to each tube, for near perfect convergence, high repeatability and stability over a wide range of operating conditions.

We combine it with a specially-designed OLF (overlapping field lens) gun and unitized grid construction, providing spot uniformity across the entire screen and near-Delta resolution.

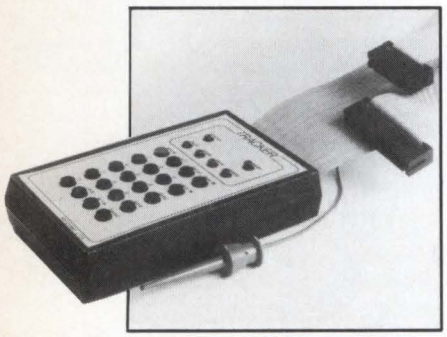
The result: a triumph over the convergence factor. Find out what it can do for your next color terminal or monitor, and ask about our full line of quality color and monochrome CRTs. Write or call: Panasonic Industrial Company, Electronic Components Division, One Panasonic Way, Secaucus, N.J. 07094; (201) 348-5278.

The achievement of Panasonic high resolution in-line color CRTs.

Panasonic
Industrial Company

CIRCLE 119

Winchester disk exerciser



The Tracker handheld Winchester tester exercises 5¼″ drives having a Rodime or ST 506 interface without corrupting data on disk. All unintentional write operations are prevented by the write protect interlock facility. Main interface status lines are constantly displayed on 6 LEDs; operational errors are indicated via audible alarm. Step rates are programmable over 30μs to 25.5 ms to emulate the step rate of most disk controllers. The unit can address up to 1024 cylinders. The single 5-V operational power supply can be obtained from the disk drive. Std data transfer rate is 5M bps. Single-unit price is $500. **Rodime PLC,** 25801 Obrero, Mission Viejo, CA 92691.
Circle 357

Portable data transmission testing

A transmission-impairment measuring set (TIMS) and a bit-error rate test set (BERT) combine to form HP 4935S, a data transmission set. System makes the required measurements to troubleshoot and verify proper installation of data links up to 72k bps. TIMS performs loss, gain slope, noise, and signal-noise tests, while BERT simultaneously measures bit-error and block-error rate and errored seconds on sync and async networks. Data transmission set is $5315; standalone BERT is $1765. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 358

Digital event trigger generator

DET-18 digital event trigger generator allows users to generate 1 output from a group of specified input states. Up to 18 TTL or LS/TTL compatible inputs are accepted, including clock and control lines. When the digital event occurs, 1 trigger output is generated. The true level for each of the 18 signal lines is switch selectable for high, low, or "don't care" input states. Generator derives its 5-V at 50-mA power from the circuit under test. Input connector is a std 20-pin header with 0.025″ (0.064-cm) square posts. Price is $99, or $129 with 20-conductor input cable. **Connecticut microComputer,** 36 Del Mar Dr, Brookfield, CT 06804.
Circle 359

Analog board test system

Implemented in Motorola's EXORbus compatible modules, the Sleuth ATS (analog test system) measures voltages within a ±100-V range in its std configuration. Resolution is selectable down to 500 μV. Std counter/timer permits frequency measurements in the audio range. All input multiplexer functions are implemented in arrays of fast mercury-wetted relays. Std modules include A-D and D-A converters, as well as sample/hold and peak measuring instruments capable of single-ended and differential measurements. **Sleuth Tester Div, Engineering Consultants and Publications,** 9 S 69th St, Upper Darby, PA 19082.
Circle 360

Digital storage scope offers 4-channel display

PM3305 35-MHz digital storage scope provides 8K bytes of divided memory. Display mode uses 4K-byte memory and includes 2-channel input, sensitivity from 2 mV to 10 V/div, and time-base speeds from 100 ns to 0.5 s/div. Pretrigger facilities include time-base extension to 5 s/div and 2 additional floating channels. A sequential sampling system stores repetitive signals up to the 35-MHz bandwidth and supplies an integral min/max function for storage and detection of glitches and pulses as short as 50 ns. Display can be expanded 10 times and memory segments can be displayed on a 4 or 40 times greater scale. **Philips Test and Measuring Instruments, Inc,** 85 McKee Dr, Mahwah, NJ 07430.
Circle 361

Protocol monitor simulator

The latest in a line of protocol monitor/simulators, the Dyna-Test 1600 portable tester can be used to isolate malfunctions; perform qualitative measurements; or simulate a modem, terminal, or computer port in the data network. Principal features include an integral tape capable of capturing data at rates as high as 56k bps, a protocol key that stores operating parameters for 7 different lines, and clear text display of the SDLC or HDLC control bytes. The device supports most std protocols, including IBM 3600. Std interfaces and data codes are available. **Dynatech Data Systems,** 7644 Dynatech Ct, Springfield, VA 22153.
Circle 362

MICROPROCESSORS/ MICROCOMPUTERS

Single-board CP/M computer

Multibus compatible board RG-802, when combined with CP/M 2.2, forms a single-board computer with 64K-byte RAM. Z80A CPU runs at 4 MHz and board can support single- and double-density disk formats that interface to Shugart 801 disk drives. Other features include 4K-byte boot PROM, 2 RS-232-C ports, 8 vectored interrupts, and a CP/M+ 2.2 operating system. Price is $995. **Raster Graphics Inc,** PO Box 23334, Tigard, OR 97223.
Circle 363

Rocker switches

The 0815 series switches are rated at 12 A, 125 Vac, and 0.5 HP, 125 to 250 Vac, and come optionally with 15 A, 125 Vac, 0.5 HP ratings. Solid or lighted rockers are available in a range of colors, with customized legends. Std bezels are black. One-piece molded plastic, snap-in mount cases fit into 0.55″ x 1.125″ (1.4- x 2.858-cm) openings and hold securely in 0.031″ to 0.251″ (0.079- to 0.638-cm) thick panels. Quick disconnect 0.25″ (0.64-cm) terminals or 16-gauge wire leads are supplied. Circuits available are SPST, SPDT, SPDT center-off, and SPST with integral 125-Vac neon lamp or optional 6- to 14-Vdc or 28-Vdc filament lamp. **McGill Manufacturing Co, Inc,** 1002 N Campbell St, Valparaiso, IN 46383.
Circle 364

VICOM Digital Image Processor

The Architectural Breakthrough

The latest development in digital image processing is here! It's a major breakthrough in systems architecture from Vicom Systems, Inc. And it *combines* patented hardware and software features you've been waiting for to give you unequalled speed and flexibility in a variety of applications.

The Fully-Integrated System The VICOM Digital Image Processor is a versatile computing tool . . . the *first* to use the architecture of the Motorola 68000 microcomputer. The entire system—lookup tables, image pixels, registers, array processor, and RAM memory—resides in the direct address space of the 68000, providing the ultimate in accessibility and efficiency.

The VICOM system can operate as a real-time scene analyzer, a peripheral processor to a host computer, or a stand-alone digital image processor.

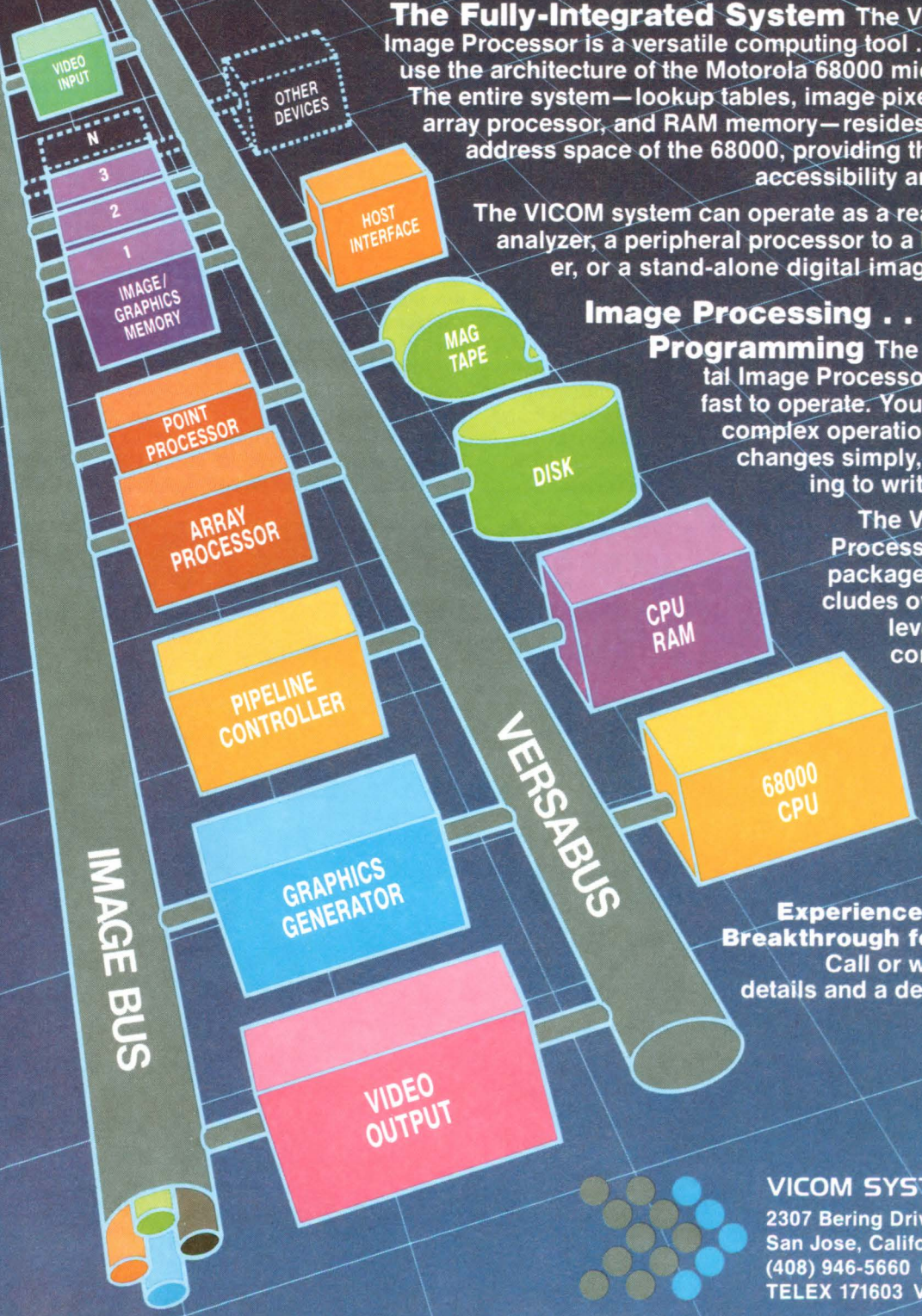


Image Processing . . . Without Programming The VICOM Digital Image Processor is easy and fast to operate. You can perform complex operations and make changes simply, *without* having to write a program.

The VICOM Image Processing Software package (V.I.P.S.) includes over 100 high-level interactive commands that significantly reduce project implementation and execution time.

Experience the VICOM Breakthrough for yourself. Call or write for more details and a demonstration.

VICOM SYSTEMS INC.
2307 Bering Drive
San Jose, California 95131
(408) 946-5660 (800) 538-3905
TELEX 171603 VICOM SYS

VICOM. The next generation in image processing.

These days, it takes more than superior features to sell your imaging system.

It takes a dazzling image, be it color or monochrome. Because from your customers' point of view, what's *on* the screen is more important than what's *behind* it. That's why you should look into using a high resolution KRATOS monitor in your system.

MINIMIZED JAGGIES

At best, most raster-scan monitors display curves as staircases, and straight lines as jagged ones. To improve this situation, some manufacturers alter their image through software manipulation. But that merely disguises the problem. KRATOS has a better approach.

Model	Color/ Mono	CRT size (diagonal)	Deflection angle
M1000	mono	19-inch	114°
M1100	mono	19-inch	90°
M1200	mono	25-inch	90°
KM1400	color	19-inch	90°

1024 LINES, NON-INTERLACED

Our 1280 pixel x 1024 line format is *non-interlaced.* So at any given instant, KRATOS monitors display twice as much data as comparable top-of-the-line interlaced monitors.

And that's clearly an advantage for you.

HIGHER REFRESH RATE AND BANDWIDTH

As you can imagine, presenting data at this high rate is no easy task. So to keep the display from flickering, KRATOS monitors provide a 60Hz refresh rate (64kHz horizontal scan rate).

And that's nothing to blink at.

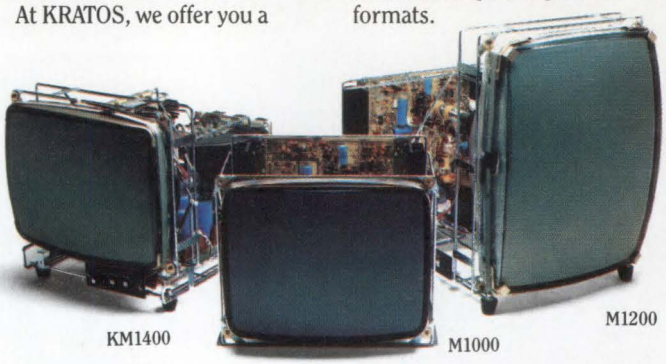
To further refine your image, KRATOS monitors use a video amplifier with a bandwidth of 100MHz. Technically speaking, that means a rise and fall time of less than 3.5 nanoseconds per pixel. To your customers, it means a brighter, clearer view of things.

COLOR OR MONOCHROME

At KRATOS, we offer you a clear choice of high resolution monitors: both color and monochrome models.

Our KM1400 color monitor is probably the best raster-scan monitor on the market. It maintains color fidelity without a flicker. The result is no eye strain, and something every customer likes to see—improved productivity.

We also offer three picture-perfect monochrome models: the reliable M1000, the precision M1100 with its smaller spot size and 90° deflection tube, and, to give you the big picture, the 25-inch M1200. All models are available in both landscape and portrait formats.



SEE US SOON

So no matter what your application: CAD/CAM, medical imaging, NMR, or graphic simulation to name a few, KRATOS can do wonders for your image. Not to mention your sales.

For more information about these and other KRATOS products, call or write us at 101 Cooper Court, Los Gatos, CA 95030; phone (408) 395-3700; TELEX 171946.

WHAT A KRATOS MONITOR CAN DO FOR YOUR IMAGE.

KRATOS | Display Systems

CIRCLE 121

See us at NCGA booth #2251

Flexible single-board computer

Eliminating the need for separate memory, I/O, and time functions, the STD-147 is a Z80A single-board computer. STD bus compatible, it features 3.69-MHz Z80A with crystal clock, program disable of 16K-byte EPROM, time/calendar, 8 programmable control lines, and 2 programmable timers. With optional 64K-byte DRAM the unit is $395; without, $250. **Micro-Link Corp,** 14602 N U.S. Hwy 31, Carmel, IN 46032.
Circle 365

19M-byte, 16-bit micro

Model 1540 offers 50% more disk storage capacity—19M bytes in contrast to 12.8M bytes—than other models in the 1000 series. Basic configuration includes CPU with 128K bytes of main memory; 1M-byte floppy disk drive; 5.25″, 19M-byte hard disk drive; and 2 RS-232-C ports. Including operating system, this configuration costs $8995. **Micro Five Corp,** 17791 Sky Park Cir, Irvine, CA 92714.
Circle 366

Z80A based universal board

M-11, a Z80A based computer board, provides 64K-byte RAM with 12K-byte EPROM capacity, 4 onboard series interface ports, and a parallel interface port. Designed for a CP/M operating system, the board features simultaneous and mixed control of 5¼″ and 8″ floppy drives. BIOS uses 4K-byte RAM for autoboard rate detect and high speed sector skew for operating software control. Single unit sells for $595; OEM quantity pricing is available. **James Electronics, Inc, Computer Div,** 4050 N Rockwell St, Chicago, IL 60618.
Circle 367

Multitasking microcomputer

A dual-processor unit brings the power of the 16/32-bit MC68000 to Z80A based series CS-3A microcomputers, while maintaining compatibility with CP/M and existing 8-bit software. Other std features include up to 4M-byte main memory, 2.4M-byte dual floppy drives, and 21 backplane expansion slots. Optional built-in hard disk stores another 21M bytes. The 2-processor configuration runs Cromix-D, multi-user, multitasking operating system whose features and user interface are similar to UNIX. Dual-processor system with 256K RAM costs $7995. **Cromemco, Inc,** 280 Bernardo Ave, PO Box 7400, Mountain View, CA 94039.
Circle 368

Single-chip microcomputer

HMOS II processed 8050AH achieves video speed, low power, and high reliability in a general purpose single-chip microcomputer. The 8-bit 3050AH is compatible with the software and architecture of the 8048 and 8049. The unit contains 4K bytes of program ROM, 256 bytes of data RAM, 27 I/O lines, and an 8-bit counter timer. It has an 11-MHz clock and can be expanded with MCS-80 and MCS-85 peripherals. Two versions, 1 without ROM and 1 with EPROM, will be available soon, as will the ICE-49A 11-MHz in-circuit emulator. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 369

16-bit micro with 1024K RAM

Black Box 3/60S is based on a high speed 16-bit 8088 microprocessor. The microcomputer features 256K bytes of RAM, expandable to 1024K bytes. RS-232 serial ports operating up to 19.2k baud interface the computer to 16 peripherals. In addition, the unit includes an IEEE 488 interface operating at 800K bytes/s. An integral 5¼″ Winchester disk provides 19M-byte unformatted data storage; a 5¼″ floppy stores another 1M byte. The 3/60S runs under MP/M-86 and supports BASIC, COBOL, and Pascal, as well as word processing, spread sheet, and database application programs. **Rair Microcomputer Corp,** 4101 Burton Dr, Santa Clara, CA 95050.
Circle 370

High speed process controller

The TM990 103, a 16-bit CPU in the TM990 series of microcomputer modules, allows onboard expansion of I/O via 2 sockets. Additional modules can provide such I/O capabilities as speech synthesis, floppy disk control, or EPROM programming. Memory provides up to 80K bytes of RAM and 32K bytes of EPROM. Memory expansion platforms supply additional memory in various combinations. Other features are an 87-member instruction set, onboard fault indicator, and hardware debug panel interface. Prices range from $1660 to $1830. **Texas Instruments Inc, Semiconductor Group,** PO Box 401560, Dallas, TX 75240.
Circle 371

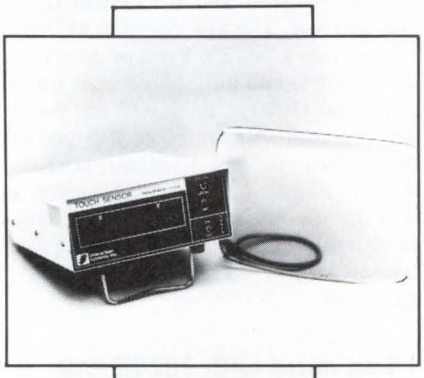
Bit-slice/micro development system

The DS370 development system features 16 levels of trigger/trace control, symbolic debugging with user defined mnemonics, and time measurements for performance analysis. System uses an internally bit-sliced processor and an 80-bit wide, 4K-byte deep trace memory that offers 64k breakpoints. Controllable from user's host system, it provides automatic test equipment capability. Downloading allows setup features like complex formats and mnemonic tables. Prices start at $11,000. **Hilevel Technology, Inc,** 18902 Bardeen Way, Irvine, CA 92715.

Circle 372

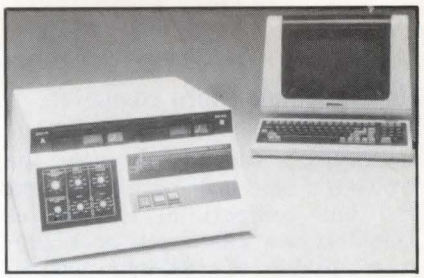
Touch-sensitive development system

Digitized CRT touch development system TK-1000 detects touch with an X-Y coordinate method. Features include transparent screen for installation on a CRT screen, LED position display, RS-232 communication port, and power supply. Screens are available in 12″, 15″, and 19″ sizes. The system is microprocessor based and provides tools for application software such as word processing and graphics. **Interaction Systems, Inc,** 24 Munroe St, Newtonville, MA 02160.



Circle 373

Microcode development station



STEP-7/FITS firmware integration and test station supports all bit slices, high speed controllers, and digital signal processing circuits. Microprocessor designs receive realtime support (to 36-ns access times) from the station's memory and ROM emulation. System emulates high speed memory, controls target system clock, and analyzes target's logic state. The single-unit station has a full-sized CRT terminal, 3 serial I/O ports, and 6 slots (expandable to 10) for memory emulation and logic state analyzers. Two floppy drives and CP/M OS provide over 1.5M-byte storage. Prices range from $8500 to $60,000. **STEP Engineering,** 757 N Pastoria Ave, PO Box 61166, Sunnyvale, CA 94086.

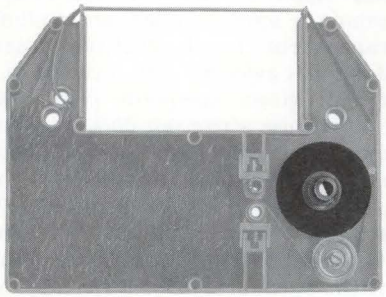
Circle 374

When was the last time you dramatically improved your printer's performance?

Today's measure of a printer's performance goes beyond line speed and purchase price. The true test is print quality and cost-per-character operating expense. Porelon ink rolls, designed specifically for impact printer ribbon cartridges, will dramatically improve the number of quality impressions and greatly increase the life of every ribbon.

Better impressions, increased ribbon life. At less cost. That's what you'll get every time you design a ribbon cartridge featuring Porelon ink rolls.

Find out how simple it is to add this performance feature to your impact printers. For further information, call 615/432-4134, or write: Porelon, Inc., 1480 Gould Drive, Cookeville, Tennessee 38501.

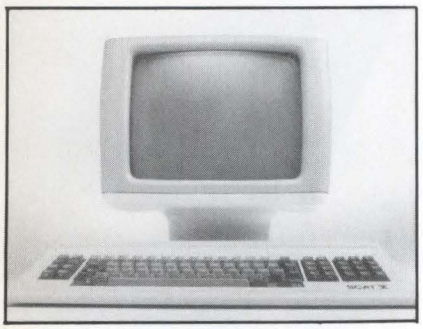


PORELON

YOUR LAST IMPRESSION IS WHERE WE BEGIN

CIRCLE 126

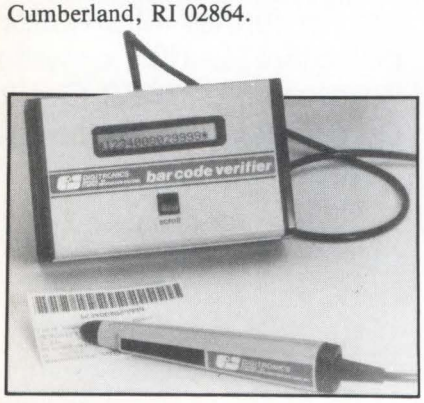
Replacement for IBM 327X terminals



Scat X is plug compatible with IBM's bisync communications lines and can operate as an IBM 3278 terminal in either a standalone or cluster environment. The unit supports copy and addressable printers. It features a standard IBM 3278 typewriter-style keyboard, a 14″ (36-cm) diagonal, high resolution, nonglare screen with tilt and swivel adjustments, and RS-232/RS-422 interfaces. One terminal costs $1995; versions for cluster use, which requires a terminal controller, cost $1295 each. **Peripheral Technology, Inc**, 14784 NE 95th, Redmond, WA 98052.
Circle 375

LOGMARS bar-code verifier

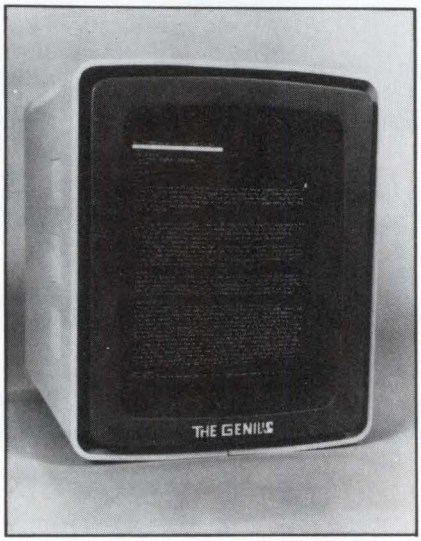
Designed to read bar codes complying with the Logistics Application of Automated Marking and Reading Symbols (LOGMARS) established by the U.S. Department of Defense, the Bar Code Verifier ensures that labels are bar-code readable and accurate. The handheld battery operated unit displays 16 chars at a time and scrolls up to 30 chars. Unit price is $595; rechargeable battery is optional. **Digitronics, Div of Comtec Information Systems, Inc**, 53 John St, Cumberland, RI 02864.



Circle 376

Improved screen speed display

An RS-232 version of The Genius display completes a full page, 57-line x 80-char screen in less than 3 s. The high resolution, flicker free monitor's interface functions up to 19.2k baud with all interface functions controlled by a Z80 microprocessor. Internal memory is 16K and provides buffering and an internal screen memory. The display operates at 100/120 V, 60 Hz or 220/240 V, 50 Hz. It is available with white, green, or amber phosphors and provides reverse video and flashing attributes. A 128-char interchangeable ASCII char generator is used; foreign language char sets are optionally available. **Micro Display Systems, Inc**, PO Box 455, Hastings, MN 55033.

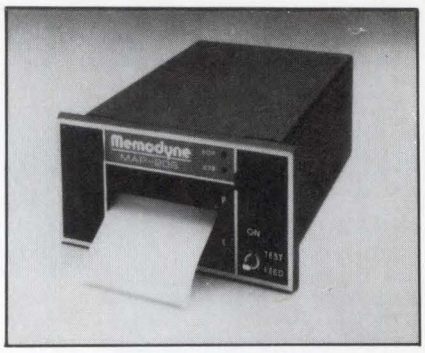


Circle 377

Touch-sensitive screens

Touch-sensitive monitor, compatible with Apple II, IBM PC, and others, features a screen divided into multiple transparent touch-sensitive areas. Monitor is available with a choice of 3 screens: green, composite color, and RGB. For use where fast data entry and response is required, such as data retrieval, building directories, and teaching aids, system provides 12″ monitor, cables, cards, and Program-That-Writes-a-Program software. Basic system sells for $1450; different configurations are $1550 and $1950. **Touch Technology, Inc**, 3 Church Cir, Annapolis, MD 21401.
Circle 378

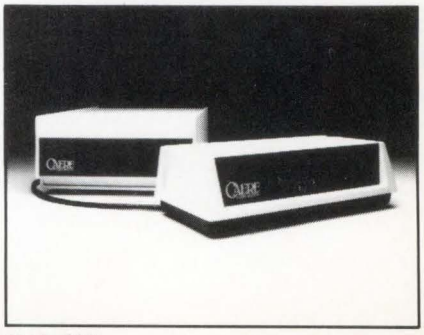
Alphanumeric thermal printer



MAP-20SL series microprocessor compatible 20-col thermal printers operate over a −40 to 50 °C temperature range. One model operates on 110 or 220 Vac; another operates on 11 to 40 Vdc. Both feature RS-232-C and 20-mA current loop interfaces, logic-selectable baud rates from 75 to 9600, a 2-line/s print rate, a 96-char print set, programmable controls, a built-in self-test program, and electronic end-of-paper sensing. Both models measure 4.44″ x 2.75″ x 7″ (11.28 x 7 x 17.8 cm). **Memodyne Corp**, 220 Reservoir St, Needham Heights, MA 02194.
Circle 379

Low cost OCR system

Optical character recognition (OCR) system, series 500, employs LSI for data recapture. System applications include remittance processing and inventory control by reading characters printed on inventory tags and computer generated invoices. Data, in a string of up to 80 characters, are entered with either a wand or slot reader and include a variety of fonts with programmable data formats. Standard model is priced at $1295. **Caere Corp**, 100 Cooper Ct, Los Gatos, CA 95030.



Circle 380

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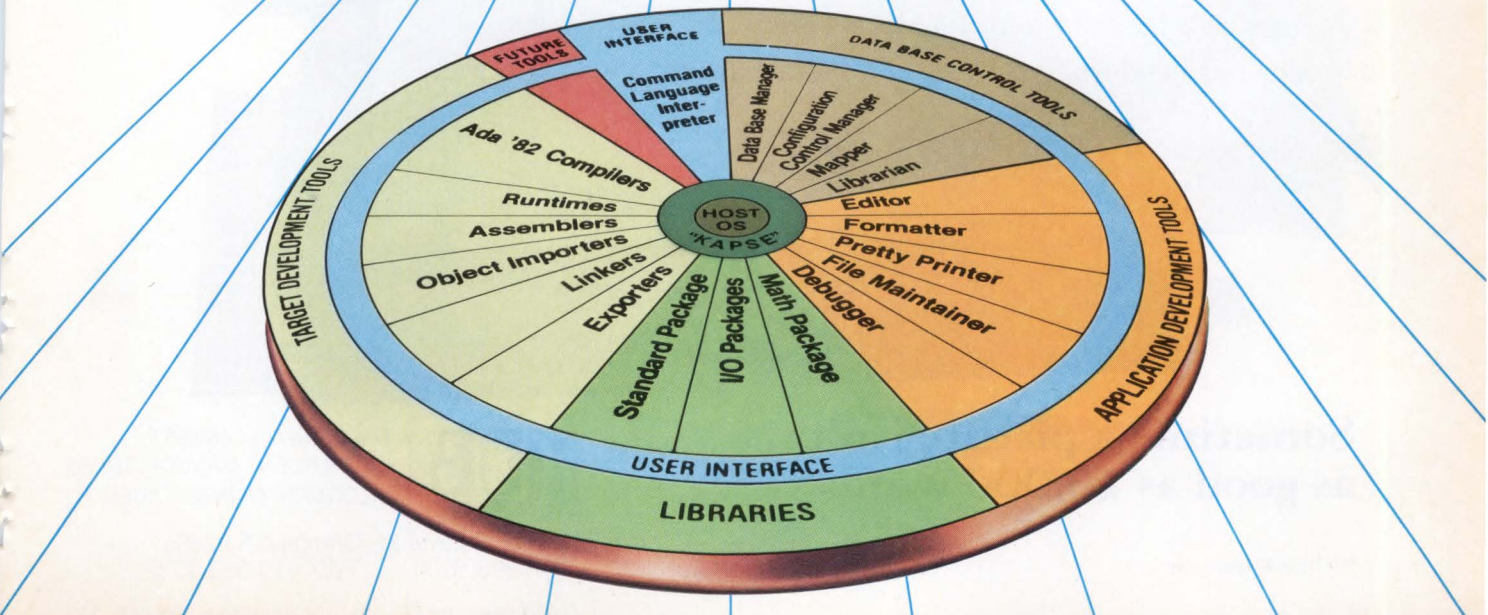
CIRCLE 127



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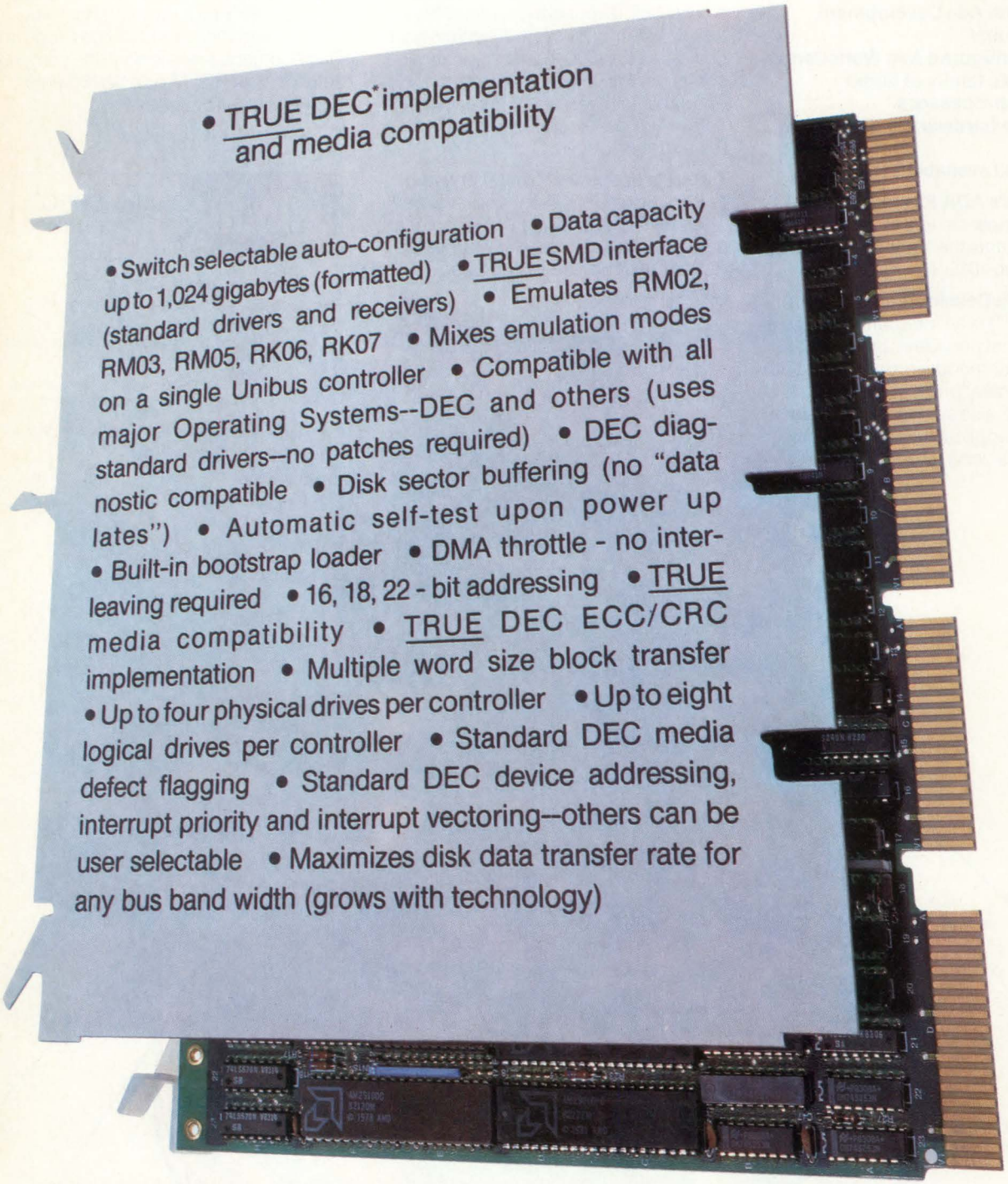

Sometime a picture isn't as good as 10,000 words.

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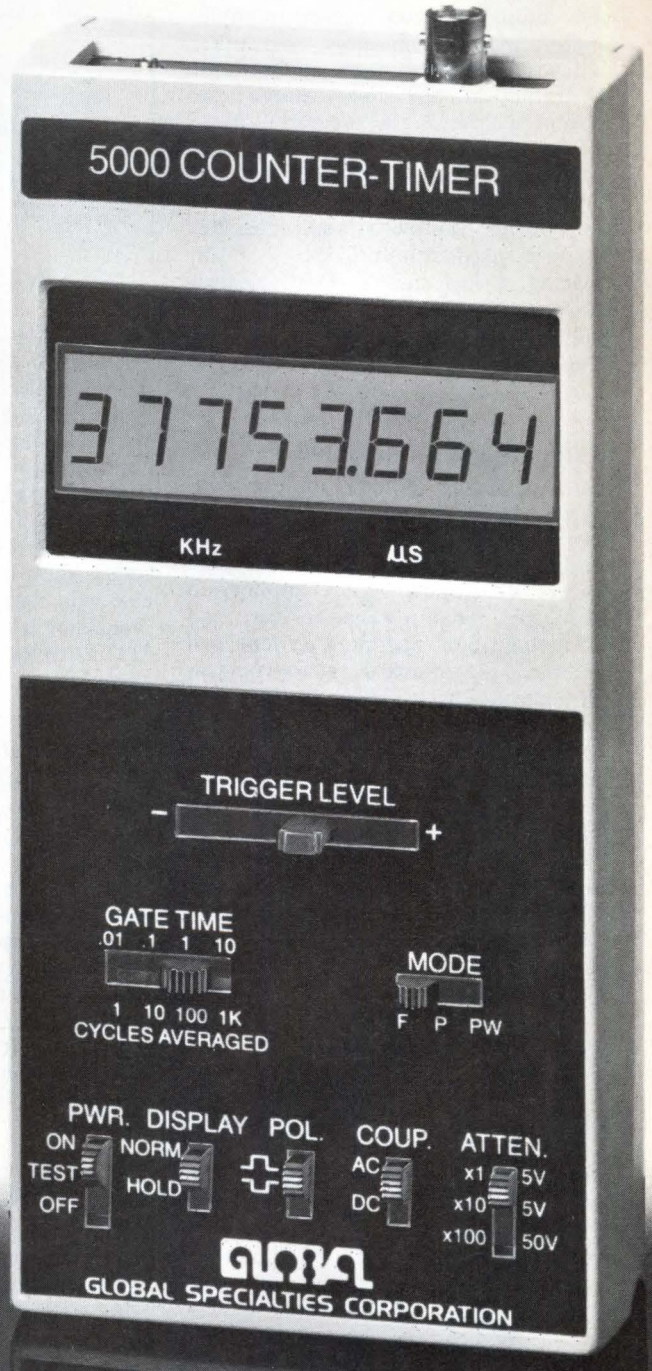
- Display storage function maintains last reading

SPECIFICATIONS

Input: BNC	
Impedance:	1M Ω @ 25pF in all modes
Sensitivity:	30 mVRMS — 1 kHz to 30 MHz 50 mVRMS — DC to 50 MHz
Modes:	
Frequency:	.1 Hz to 50 MHz (gate times 0.01, 0.1, 1.0, 10 s)
Period:	50 ns to 10 s (1, 10, 100, 1000 cycle averages)
Pulse Width:	25 ns to 10 s (1, 10, 100, 1000 cycle averages)
Full Signal Conditioning:	
Coupling:	AC or DC switch selectable
Attenuation:	x1, x10, x100 switch selectable
Polarity:	+/− edge Freq. & Period; >/< trigger level, Pulse Width
Trigger Level:	variable 0 ± 500 mV x attenuator setting
Time Base:	10 MHz crystal oscillator (± 4 ppm, 0-40°C.)
Controls:	Power/Test/On, Mode, Gate Time/Cycles Averaged, Display-Norm/Hold, Trigger Level, Polarity, Coupling, Attenuation
Power:	6AA Cells (Nicad or Alkaline) 10 hrs continuous operation Optional AC Charger/Adapter
Dimensions:	7.60 x 3.75 x 1.72 inches, (193 x 95 x 44 mm)
Weight:	14 oz., (397g), without batteries



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CIRCLE 85

Alphanumeric impact printer

The NAP-16-I line of panel mounted printers provides hardcopy output for test equipment, data loggers, multiple-station message repeaters, and other industrial and laboratory applications. Operating at one 16-col line/s, the printer achieves a 500k-operation mean cycle before failure. Wire-impact printing mechanism forms 5 x 7 dot matrix chars on plain paper using a single-color (purple) ribbon cassette. Stepper mechanism provides 7-line/in spacing. Prices start at $395. **Keltron Corp**, 225 Crescent St, Waltham, MA 02154.
Circle 381

Terminal conversion system

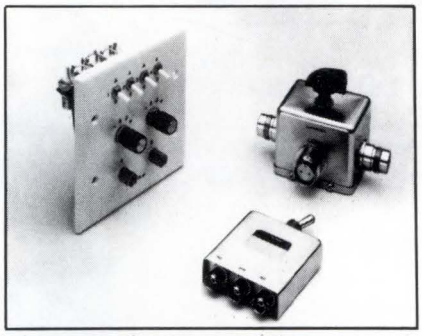
Microprocessor based terminal converter, TC3278, allows IBM 3278/3178 terminals to retain all regular features while adding local computing. Local system offers development and application software, data storage devices, and communication operating system and utilities. Single-board microprocessor provides 64K RAM, 3 async serial ports, and 2 coaxial interfaces for the 3278 and 3274/3276 cluster controllers. Storage is available in single or dual floppies for 1.6M bytes or in a diskette and Winchester combination for 5M, 10M, or 20M bytes. The system is priced from $1995 with quantity discounts available. **3R Computers Inc**, 18 Lyman St, Westboro, MA 01581.
Circle 382

15″ monochrome CRT

Complementing its manufacturer's line of 5″, 7″, 9″, 12″, and 14″ diagonal models, a 15″ diagonal monochrome CRT display extends horizontal operating frequencies to 24 kHz, compared to a 19.2-kHz max rating for the manufacturer's similar units. Offered in portrait or landscape versions, the CRT offers an optional range of switching power supplies and custom designed, injection-molded cabinets to accommodate a variety of customer logic board designs; users can also choose from several phosphors and face treatments. **Zenith Radio Corp**, 1000 Milwaukee Ave, Glenview, IL 60025.
Circle 383

SYSTEM ELEMENTS

EDP isolated ground data switches



Series 362 rf coaxial switches accommodate in-wall coaxial wiring where data signal ground must be isolated from system ground. Features include wall, desk, or panel mounting to 3.5″ x 19″ (8.9- x 48-cm) rack. Switches terminate with keyed Twinax or isolated BNC/TNC connectors. Toggle, push-button, and rotary knob manual operation is available with 1P2T or 1P2T-1P5T capabilities. Frequency is 0 to 50 MHz. **Amphenol**, 2122 York Rd, Oak Brook, IL 60521.
Circle 384

Panel mount LEDs

Model 2L501 super bright T-1 size LED indicators fit in a 0.25″ (0.64-cm) diameter hole. Light output is up to 18 mcd (typ at 20 mA), or more than 4 times std LED brightness. The LEDs are available with an all-metal threaded body, wire leads or wirewrap terminals for soldering, and flat or domed transparent or translucent lens (colored, clear, or white). Light can be powered by sources up to 14 Vdc with optional built-in resistors. **Sloan Co**, 7704 San Fernando Rd, Sun Valley, CA 91352.
Circle 385

Line-voltage selector switches

Series SE features fully enclosed housings. Ten-A, 125-Vac and 5-A, 250-Vac models meet UL, CSA, and SEV requirements; a 2-A (resistive load), 250-Vac version meets VDE requirements. Terminal styles include normal and right-angle PCB mounting configurations; other models come with solder terminals. **ITW Switches, An Illinois Tool Works Co**, 6615 W Irving Park Rd, Chicago, IL 60634.
Circle 386

Dual BIFET switch

The SW05 is a dual single-pole, single-throw monolithic BIFET analog switch that enhances the DG200 CMOS device by providing improved performance and a lower max V_{ERROR} = 10 uV ($I_{D(ON)}$ x R_{ON}) at 125 °C. With fast switching speed guaranteed for 25 to 125 °C, SW05 can operate from dual- or single-power supply systems. TTL input compatibility with 400-mV noise immunity is guaranteed. In 100-piece quantities, the SW05BK (military) is $8.20, SW05FK (industrial) is $2.75, SW05GP (commercial plastic) is $2.50, and SW05BK 883 (improved military grade) is $11.05. **Precision Monolithics, Inc**, 1500 Space Park Dr, Santa Clara, CA 95050.
Circle 387

DC motor driven blowers

Series WBM-570 includes integral brushless dc motor drives and a 1-, 2-, or 3-stage backward-curved centrifugal fan configuration in a 5.7″ (14.5-cm) diameter package. The blowers are designed to equal or surpass performance of 9.5″ (24.1-cm) diameter blowers. Units achieve vacuum performance to 28″ (71 cm) of water at 0 cfm. A variable 12- to 42-Vdc voltage controls speed. Blowers come with an 8-conductor ribbon cable lead and can be face-mounted in any position via 3 tapped mounting holes on a 4″ (10-cm) circle. Double ball bearings provide quiet operation and long life. **Ametek, Inc, Lamb Electric Div**, 627 Lake St, Kent, OH 44240.
Circle 388

Mini slide switches

Instrumentation grade slide-actuated miniature switches, the K series features a potted/sealed base and terminals that allow the switches to be PCB mounted at the same time as other components for wave soldering processes. The switches are rated from 10 mA/5 Vdc through 2 A/250 Vac, depending on specified contact. Options include actuator location and size, contact type, terminal spacing, single and double circuitry, and several switch functions. An optional clear plastic cover inhibits accidental operation and provides dust protection. **Crouse-Hinds® Co, Arrow Hart Div**, 103 Hawthorne St, Hartford, CT 06101.
Circle 389

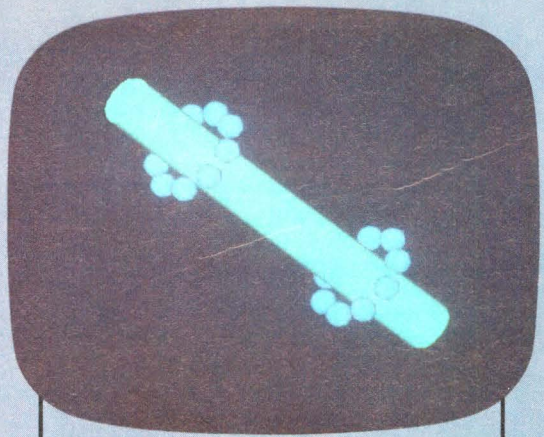
Now you can build in seconds what used to take forever.

If you have been waiting to view your solid models, your waiting days (or even minutes) are over. Now there's SOLIDVIEW.™ A revolutionary, new display technology for viewing solid models that significantly increases system speed. And significantly decreases host overhead, software development time, and total system cost.

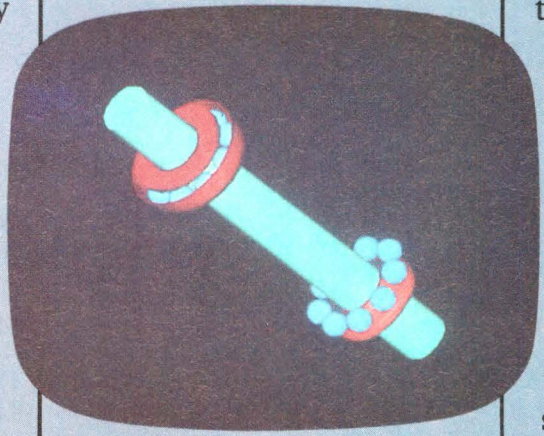
By processing tasks like hidden surface removal, visible surface shading, sectional views, contouring, and even piercing objects, SOLIDVIEW slashes image construction time from minutes to seconds. The host is then free to handle viewing transformations and clipping concurrently; system throughput is greatly improved.

What's more, SOLIDVIEW constructs images using polygons instead of pixels. These images are built piece by piece, instead of line by line. So you not only get more speed; but more information.

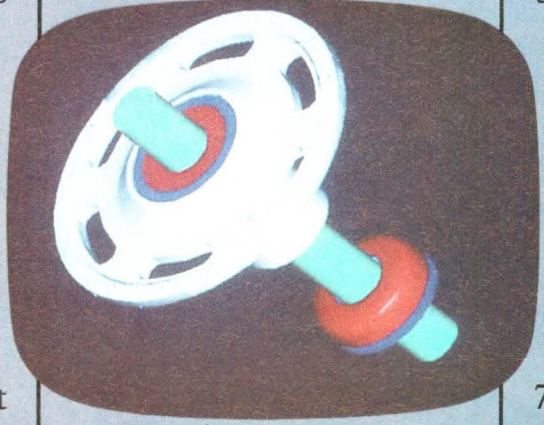
You can also do more with SOLIDVIEW. You can add new parts without redrawing the entire screen. You can manipulate objects with a minimum of recalculating. You can make exploded or sectional views in seconds. You can even use translucent shading to see behind surfaces.



Construct images in less than four seconds.



Then build incrementally. In seconds.



Create complex solids just as fast.

SOLIDVIEW by Lexidata.

SOLIDVIEW is available in two models, with a wide array of features. Both offer you 12 × 24 color lookup table, 19″ monitor, and the power required to view your images interactively for the first time. Options include pan/zoom, four overlays, hardware cursor, serial interface, and a selection of peripherals.

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Low noise amplifier

Four-channel monolithic Model TRA403 amplifier achieves a 330-mV/μA gain and a 7-ns response time. The device operates on less than 25 mW/channel and maintains noise levels under 25 nA rms. Amplifier comes in 20-pin DIP or 18-pin LCC configurations; PCB-mounted version facilitates evaluation and prototyping. The unit suits amplification of small current pulses obtained from low capacitance devices (20 pF or less) and can be used with solid state radiation and light detectors. Price is $35. **LeCroy Research Systems Corp,** 700 S Main St, Spring Valley, NY 10977.
Circle 390

Axial Schottky rectifiers

USD1120, USD1130, and USD1140 Schottky devices come in the same axial-leaded plastic packages as 1N5817, 1N5818, and 1N5819 rectifiers. Compared with 1N5817 devices, however, the USD models offer 250-mV lower forward-voltage drops, higher op temps (150 vs 125 °C), and a higher surge current rating (50 vs 25 A). Among other applications, the rectifiers can serve as freewheeling or polarity-protection diodes in low voltage, high frequency inverters. 1000-piece prices range from $0.59 to $0.74. **Unitrode Corp,** 5 Forbes Rd, Lexington, MA 02173. **Circle 391**

Pressure transducer

Model 151B comes in 13 pressure ranges from 0 to 300 psi (gauge, differential, or absolute). Std features include infinite resolution, low power consumption, ±0.5% static error band (BSL), and long-term stability. Unit operates from choice of 4 regulated dc supplies with 3 options for high level dc output. **Robinson-Halpern,** One Apollo Rd, PO Box 248, Plymouth Meeting, PA 19462.
Circle 392

Low cogging dc motors

Low cost size 20 motor series features highly permeable 11-slot laminations to minimize cogging and electrical noise. High torque to inertia ratio and low self-inductance ensure quick response. Diamond turned commutators, lubricated double-shielded ball bearings, die-cast aluminum end bells, and totally enclosed carbon steel housings are used. Motors are 100% run-in and tested to ensure proper brush/commutator seating and use UL recognized materials. Twenty std size 20 models, with several stack lengths and choice of replaceable or nonreplaceable brushes, are available. **Harowe Servo Controls Inc, a sub of Bowmar Instrument Corp,** PO Box 547, West Chester, PA 19380. **Circle 393**

Compact transformers/inductors

A series of compact single-hybrid transformers and feed-bridge inductors includes models in two configurations. Larger transformer versions feature an above-board height of 0.8″ (2 cm) and handle 120-mA max loop currents, with a balance of 28 to 31 dB at 1 kHz. Smaller transformer versions are 0.52″ (1.32 cm) high and handle 0.5-mA maximum loop currents, with a 27-dB balance at 1 kHz. Std feed-bridge inductors are available in both sizes. **Prem Magnetics, Inc,** 3521 N Chapel Hill Rd, McHenry, IL 60050. **Circle 394**

INTEGRATED CIRCUITS

Printer-controller chip

Designed to work with Matsushita/National/Panasonic EUY-10E series electrosensitive dot matrix printer mechanisms, Model A10EC printer-controller chip accepts Centronics-type parallel and RS-232-C serial TTL-level data inputs. It provides motor and head control for any EUY-10E unit and can control printing of 24 cols. Chip includes inputs for paper-feed control and self-test. The manufacturer also offers a single-board configuration, the A10EB, that includes the A10EC chip. **Able Systems Ltd,** Unit 3, Kingfisher Ct, Northwich, Cheshire CW9 7TU, England.
Circle 395

Octal logic circuits

Five circuits have been added to the line of locally oxidized CMOS (LOCMOS/isoplanar) devices: an inverting (HEF40240B) and a noninverting (HEF40244B) buffer chip, an asynchronous bus transmitter/receiver for 8-bit parallel 2-way communication between buses (HEF40245B), a transparent latch chip (HEF40373B), and a D-type flipflop for use with an 8-bit positive-edge-triggered storage register (HEF40374B). They are pin and function compatible with their TTL equivalents, with TTL compatible 3-state outputs. Circuits tolerate a 3- to 18-V operating voltage range and typically dissipate less than 400 mW. Propagation delays range from 30 to 85 ns, depending on supply voltage. **Signetics Corp,** 811 E Arques Ave, Sunnyvale, CA 94086.
Circle 396

Batteryless nonvolatile RAM

Combining CMOS semiconductor technology with STD bus compatibility, the NVR8020 nonvolatile RAM memory board contains 1K to 4K bytes of memory. Board applications include industrial control, data acquisition, instrumentation, and security access systems; maintenance-free, no-battery design provides reliability. Suited for systems where online data need to be stored, accessed, and changed, the memory board is priced at $250 in 100-unit quantities with additional discounts available. **Stynetic Systems Inc,** Flowerfield Bldg 1, St James, NY 11780.
Circle 397

Switched-mode power supply ICs

Series 8160 ICs can be voltage sourced (18 Vdc max) or current sourced (30 mA max). They contain temperature-compensated reference, sawtooth-waveform generator, pulse-width modulator, and output driver. Housekeeping functions include low and high voltage protection, loop-fault protection, and current limiting and double-pulse protection. Other features are maximum duty cycle adjustment, feed-forward control (duty cycle is inversely proportional to input voltage), and remote on/off switching. **Sprague Electric Co, sub of GK Technologies,** 555 Marshall St, North Adams, MA 01247.
Circle 398

Nonvolatile EPROM

Electrical programmability, UV erasability, and 256k-bit capacity describe the 27256 EPROM. Device is designed for use in industrial control, telecommunications, and other applications where occasional program changes are needed. EPROM programming is accomplished through a fast algorithm that checks each bit in sequence. Memory is organized into 32k bytes, allowing the programming voltage to be reduced to 12.5 V. EPROM sells for $131.10 in 10k quantities. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 399

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CIRCLE 129

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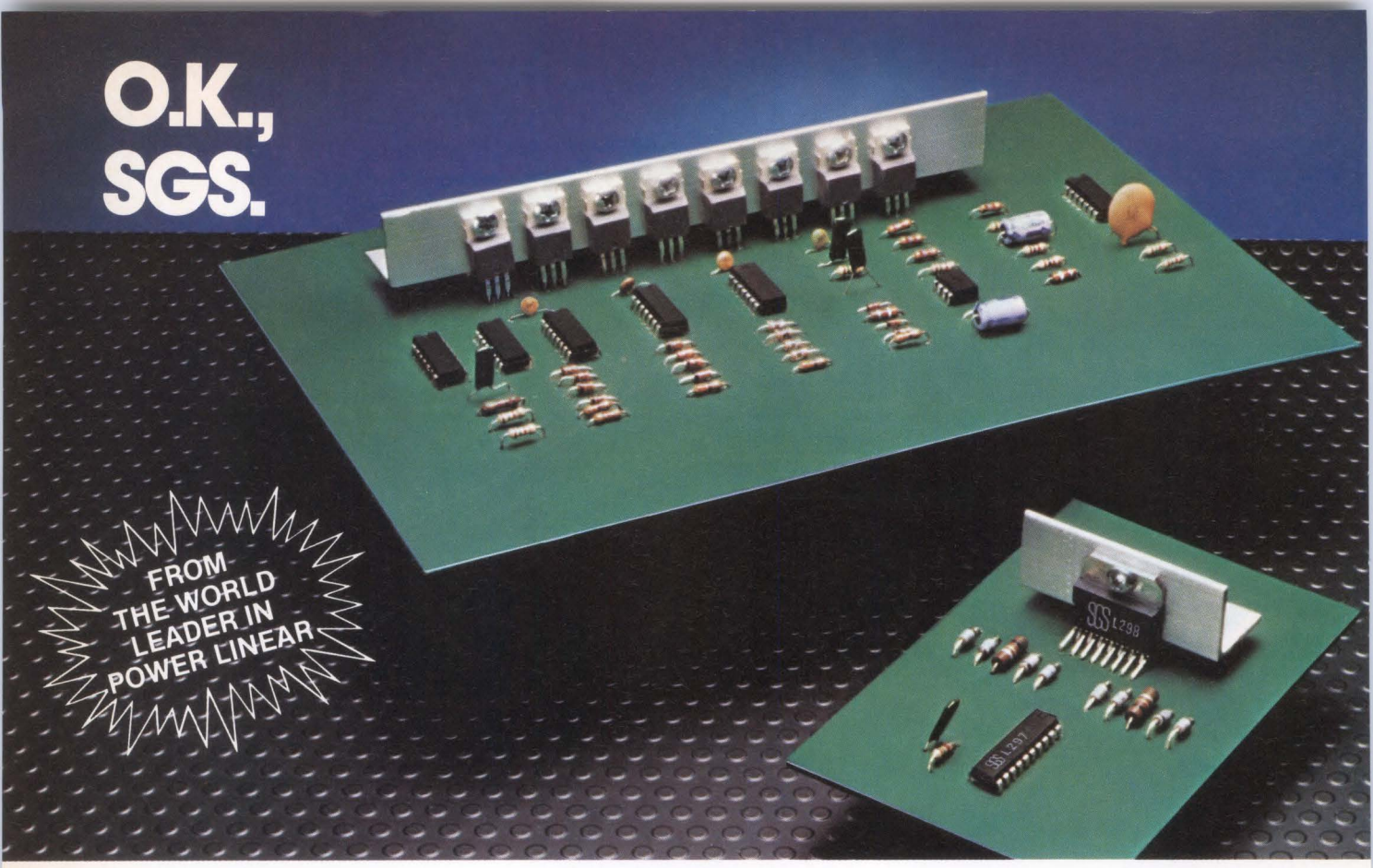


Tell me how to drive bipolar stepper motors in less space, at half the cost.

The L297 and L298 monolithic ICs from SGS may be the total solution to your bipolar stepper motor drive requirements. In fact, the L297/L298 combination provides all necessary interfacing functions between microprocessors and fractional horsepower bipolar stepper motors without additional active components. Applications include carriage control and daisy wheel positioning in printers and head positioning in disk drives.

The L297 Stepper Motor Controller
The L297 needs only clock and direction input signals to generate the four phases required to drive the motor. The L297 features full or half-step modes, with 2 steps per clock pulse possible in the full step mode. The device accepts input commands for clockwise or counter-clockwise operation. In addition, a home signal is generated to detect when the motor is in the home position.

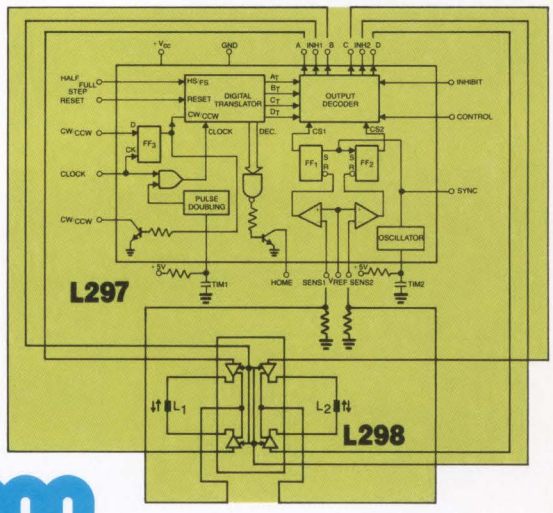
The L298 Multiwatt® Dual H Driver
The L298 is a dual full-bridge driver in SGS' popular Multiwatt® packaging. It effectively replaces 8 power transistors (2.5A each), inverter stages, resistors and other level-shifting components. The four phase signals necessary to drive the L298 can be provided by the microprocessor or the L297.

Cut Constant Current Drive Costs in Half
The L297/L298 combination can also be used with external sensing resistors to provide constant current drive to the motor. Normally, this requires a minimum of two additional ICs (gate and comparator packages). This function is also implemented in the L297 along with the four phase drive signals. By using the L297 and L298 instead of discrete devices, it is possible to cut installed circuit costs by as much as 50 percent.

L293 Dual H Driver
The L293 power amplifier can be used in place of the L298 for lower current, lower power motor drive applications.

Multiwatt® is a registered trademark of SGS-ATES Semiconductor Corporation.

Block Diagram and Typical Application



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CIRCLE 130

Auto power-down ROMs

SY23128A and SY23256A ROMs are characterized by auto power-down controlled by a chip enable input (for power savings) and an output enable function to eliminate bus contention. Data are accessible in less than 200 ns. SY23128 and SY23256 are nonpower-down models with 3 programmable chip selects allowing multiple ROMs to be OR-tied without external decoding. In 1k quantities, prices range from $6 for the 128K nonpower-down to $12 for 256K power-down version. **Synertek Inc,** 3001 Stender Way, Santa Clara, CA 95054.
Circle 400

Fast 64K EEPROM

X2864A EEPROM writes 1 byte or a 16-byte page in 5 ms and operates from a 5-V supply. By internally latching addresses and data, the host system is free for a 5-ms write period. Write speed is 25.6k bps; read access time is 300 ns. DATA-polling feature enables device to signal processor when write is finished, eliminating need for ready/busy signal and all write timing/verification hardware. Two-line control architecture ends system bus contention. **Xicor Inc,** 851 Buckeye Ct, Milpitas, CA 95035.
Circle 401

Isolated feedback generator

UC1901 series features an amplitude modulation system that allows a loop error signal to be coupled with a small rf transformer. Diode demodulation achieves accurate, stable transfer characteristics, while the programmable, 5-MHz oscillator permits the use of smaller, less expensive transformers. Performance features include an internal 1.5-V reference accurate to within 1%, 4.5- to 40-V supply operation, and a high gain error amplifier. **Unitrode Corp,** 5 Forbes Rd, Lexington, MA 02173.
Circle 402

High speed multiplier/accumulator

Sixteen-bit, 100-ns multiplier/accumulator (MAC) employs LSI technology for faster processing with less power. TDC1043 provides 35-bit double-precision internal accumulator and 19-bit extended precision output. Packaged in a standard 64-pin DIP, chip applications include array and image processors and interactive graphics. In 100-piece quantities, the MAC is $190. **TRW, LSI Products Div,** PO Box 2472, La Jolla, CA 92038.
Circle 403

Voltage symmetry in DAC

Monolithic 11-bit (10 plus sign) DAC-210S provides ±10-V output, precision voltage reference, logic controlled polarity switch, and output amp. DAC offers sign magnitude coding, which gives an analog output of 0 V for a digital input of all zeros, and is unaffected by offset of gain drift. Chip operating temps for full-range analog values are within ±10 mV (±1 LSB) at 25 °C and within ±2 LSB at extreme temperatures. In 100-piece quantities, the DAC is $27.75. **Precision Monolithics Inc,** 1500 Space Park Dr, Santa Clara, CA 95050.
Circle 404

Technical applications computer

Model 36C, an MC68000 based computer, offers 4 graphics memory planes, gray scale, and a software accessible color map. Available with Pascal and BASIC, graphics language extensions enable users to program single lines for graphic images. Interfaces include HP-IB, RS-232-C, and 16-bit parallel, among others. Unit has 128K-byte RAM expandable to 640K bytes and is software compatible with other Series 200 products. Base price is $15,140; a configured system sells for $17,660. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 405

Low cost multi-user minis

Series 5 Naked Mini 4/85 supports 32 users with access to 8M bytes of memory when paired with UNIX System III; with CARTOS, it supports 64 users. Memory cycle time is 650 ns; write access is 270 ns. Model 4/95 has 1M-byte virtual memory (expandable to 8M bytes), cache support, and 2 power supplies. NM4/85 costs $11,600. NM4/95 has been reduced over 50% to $13,690. **Computer Automation Inc,** 18651 Von Karman, Irvine, CA 92713.
Circle 406

Voice recognition on single board

PVRT-300 voice recognition unit, in conjunction with host computer's mass storage, can recognize an unlimited vocabulary kept offline and downloaded. Online capacity is 100 words or phrases with a max utterance duration of 1.25 s. Data are entered by keyboard command or by voice instructions via headset or microphone. With applications in inventory control, robotics, password security, and CAD, the system is priced below $1300. **Plessey Peripheral Systems, Distributor Products Div,** 2632 Du Bridge Ave, Irvine, CA 92714.
Circle 407

CAE workstations

A graphics workstation for CAE, the Idea 1200, offers a set of logic design, analysis, and documentation tools. System combines processing, simulation, and timing verification with a local network and distributed data base. With the system, users can design and document digital logic used in PCBs, VLSI, gate arrays, and standard cells. Consisting of 32-bit architecture, graphics display, 1.5M-byte program memory, and 34M-byte Winchester storage, the system, with applications software, is priced at $49,000 in quantities of 4 or more. **Mentor Graphics Corp,** 10200 SW Nimbus Ave, Suite G7, Portland, OR 97223.
Circle 408

SOFTWARE

Graphics software

PLOT 10 Easy Graphing II is a graphing command language with interfaces for 2 user types. A conversational interface is designed for users performing iterative graphics tasks that require alterations. A second interface aids users with occasional graphics support requirements. Supporting both monochrome and color displays, software is available in FORTRAN source code for host mainframes, or in object code for Tektronix programmable terminals. Host version is priced at $2600 and can be used by an unlimited number of users, while the local version is priced at $310/copy. **Tektronix, Inc,** PO Box 1700, Beaverton, OR 97007.
Circle 409

LISP version available

Using artificial intelligence techniques, Cromemco LISP is designed for robotics, CAD, and design automation. LISP features include fixed and floating point arithmetic, error-trapping capabilities, 150 utilities, Macro facilities, and a table-driven, user modifiable parser. Priced at $595, this version includes full documentation and choice of 5¼" or 8" diskettes. **Cromemco Inc,** 280 Bernardo Ave, Mountain View, CA 94043.
Circle 491

Monitoring and control software

With a modular set of standard and optional software, Maxpac is designed to monitor and control realtime industrial processes. The software uses preformatted tables that can define system parameters such as process variables, conversion factors, alarm thresholds, control loops, and digital inputs and outputs. **Modular Computer Systems Inc (MODCOMP),** PO Box 6099, 1650 W McNab Rd, Ft Lauderdale, FL 33310.
Circle 492

C compilers for logic development

C compilers for HP 64000 logic development system support the 8086/8088, 68000, Z8001/Z8002, 6800/6802, and 6809 microprocessors. C programming permits closer interaction with the processor than with Pascal without sacrificing Pascal's language structure, readability, or ease of maintenance. The HP 64000 system linker enables the C compiler to pass key information into the emulator analyzer to speed debugging. The linker also brings together relocatable object modules from assembly language or brings compiled C and Pascal into an executable program. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 493

Macro assembler for 8086/8088

With performance level between that of a conventional assembler and a compiler, the ASM87 relocatable macro assembler and linking loader processes the full structured assembly language specified by Intel for its 8086/8088 processors; the assembler also supports Intel's 8087 chip. The ASM87L package adds a librarian utility program, and the assembler allows user-specified segment names, symbolic and relative addressing, forward references, and a disk-paged large capacity symbol table. **Microtec,** PO Box 60337, Sunnyvale, CA 94088.
Circle 494

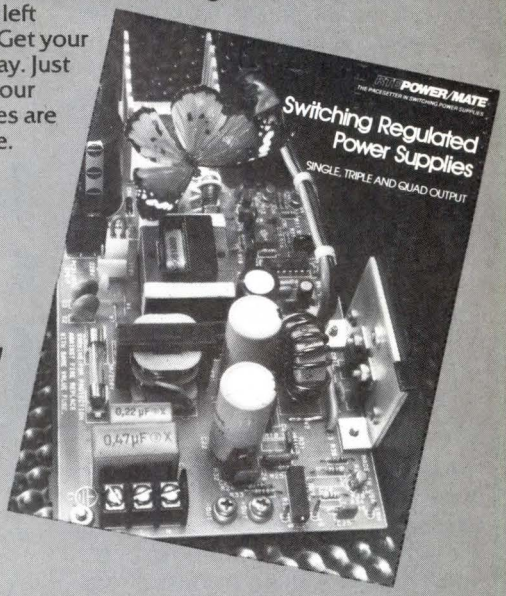
Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

A Switching Regulated Power Supply Catalog Designed For Designers.

We're designers, too. We know how time-consuming and confusing it is to jump from section to section in search of features, diagrams and specifications. That's why we designed this new 8 page catalog just for you – the design engineer. It's an ideal reference showing general information, specifications and dimensions, all in an easy-to-use format. No flipping pages back and forth. Now, each section contains all the information you need on one spread.

This brand new catalog is packed with information on the EVS, EVD and EVQ series of single and multiple output switching regulated power supplies from Power/Mate. These series are the top of the line, meeting or exceeding specifications according to **UL, VDE, FCC, CSA and IEC.** It's quality you can count on from a leader in the industry.

In this convenient catalog, you'll find the answer to your power supply needs. No searching. No time wasted. No questions left unanswered. Get your free copy today. Just call or write – our representatives are at your service.



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CIRCLE 132

Database management software

A database management and application development system for UNIX and IBM PC, Contel Tools includes programs for various business applications. Four modules within the system handle data storage and entry, and supply report writer and menu system functions. Included are utilities for updating and modifying files. Available separately are a set of accounting modules. The data entry forms allow flexible design and automatic editing. **Contel Computer Corp,** 4204 Meridian St, Bellingham, WA 98226.
Circle 495

X.29 software support

Using a single-sync communication line, the X.29 networking facility ties remote terminals to host computers. A dial-up line per terminal sends traffic to appropriate host in a single message stream. Terminals can also be concentrated locally in a packet assembler/disassembler with either public or private connections. Network conforms to CCITT X.3/X.29 standards. X.29 software license is $1000 with an X.25 license as a prerequisite. **Stratus Computer, Inc,** 17 Strathmore Rd, Natick, MA 01760.
Circle 496

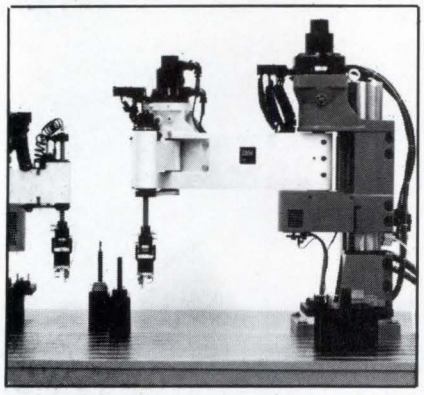
Software integrates proNET and DECnet systems

Ringway software unites DECnet software with multi-access local area network proNET. System provides networking capabilities including file transfer, remote file access, remote job submission, and remote log-in. Hardware and software combination offers 10M-bps throughput, less delay, and decreased memory requirements as packets are sent directly to their destination host. Fiber optic links are available for long distance use. **Proteon Associates, Inc,** 24 Crescent St, Waltham, MA 02154.
Circle 497

July Preview—
Watch for a major staff-written review on workstations for computer aided engineering.

CONTROL & AUTOMATION

Programmable robotic system



Industrial tasks can be automated with the 7540 manufacturing system, which includes a microprocessor based controller and a servo-controlled jointed arm. Control unit stores 5 multiple point routines. The arm is capable of 4-direction movement—horizontal arc of 200° and 160° for X-Y axes motion, 100-mm Z-axis motion, and 180° wrist-like motion for the gripper/tool. System is programmed with an IBM PC using AML/Entry version 2 which features a menu system, editor, and compiler. Price for the 7540 is $37,000 with quantity discounts available. **IBM, Advanced Manufacturing Systems,** 1000 NW 51st St, Boca Raton, FL 33432. **Circle 498**

Programmable controllers

Two programmable controllers, Series One and Series Three, offer 1K to 4K of CMOS memory, 8 to 400 I/Os, and battery backup. Series One has 24 Vdc/115 Vac I/Os and features a handheld programming panel that monitors logic, timer and counter values, and 16 I/Os. Series Three has 115 Vac/5, 12, 24 Vdc I/Os, and an instruction set provides math, data moves, and a subroutine. Prices range from under $425 for Series One to approx $3200 for Series Three. **General Electric Co,** PO Box 8106, Charlottesville, VA 22906. **Circle 499**

Microcomputer offers industrial capabilities

IMC4000 industrial microcomputer employs 68000 hardware and software for applications such as communications, robotics, and data collection. CPU is a 16-bit processor with 32-bit architecture; memory consists of 256K-byte RAM; serial I/O provides four RS-232-C channels with baud rates up to 19.2k; and parallel digital I/O has 16 inputs and outputs with handshaking. Software package provides downloading and debugging. Utilities are included for program control, math, data conversion, and string manipulation. **Gould Inc,** 3 Graham Dr, Nashua, NH 03060.
Circle 442

16-output programmable controller

Self-contained model 2020 features branching, counting, and timing capabilities. It executes up to 256 steps, each step having an output status and 1 or more instructions for leaving the step. The sequential program has a 1-to-1 correspondence with the machine it controls. Other features include 24 general purpose inputs, 4 dedicated inputs, full opto-isolation, and internal switching power supply. **Control Technology Corp,** 82 Turnpike Rd, Westboro, MA 01581.
Circle 443

INTERCONNECTION & PACKAGING

Fiber optic connector

Eliminating the grinding and polishing associated with conventional connectors, Simplex fiber optic connectors assemble without special tools. The all-aluminum units screw in to achieve fiber-to-fiber attenuation less than 2 dB. Compatible with 100- and 140-μm fiber cables, the connectors suit point to point or fiber to fiber splicing terminations. Per-unit cost is $7.50. **Mohawk Cable Co, Optical Group,** 9 Mohawk Dr, Leominster, MA 01453.
Circle 444

Multibus-compatible extender card

Version R includes 14 AWG vertical steel rails to support extended cards during system testing and troubleshooting. A stiffener bar allows 0.5" (1.3-cm) component heights on extended boards; nylon card guides enable smooth insertion and extraction. A solid groundplane on the board's backside reduces crosstalk; all system bus signals are distributed on the front. Solder mask on both board sides helps prevent shorts. **Prototek, Inc,** PO Box 46512, Cincinnati, OH 45246.
Circle 445

How to get a lot more color for your money.

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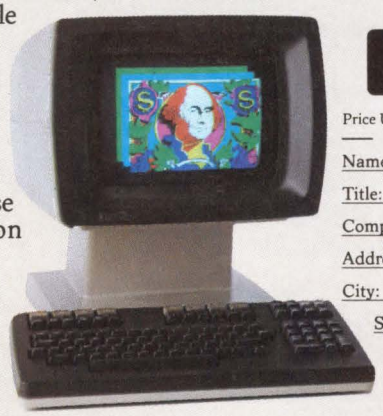
Introducing the HP 2627A Color Graphics Terminal.

Now you can have a bright, sharp image that's easy to read. For only $5,975. Which means our compact new color graphics terminal is setting completely new price/performance standards.

You get 8 basic colors, plus hundreds of additional user-defined ones. Including colors that match our plotter pens. On a black screen with 512 x 390 line resolution. You get raster display technology for fast, selective screen updates. You get vector graphics and polygonal area fills, a combination that makes it easy to create complex shapes, symbols, and even typestyles. In a lot less time. With a lot more precision.

Of course, it's also software-compatible. In addition to HP's DSG/3000 and Graphics/1000-II software, the 2627A runs PLOT 10 from Tektronix, SAS's SAS/GRAPH, Precision Visual's DI-3000 and GRAFMAKER, ISSCO'S DISSPLA and TELL-A-GRAF.

But that's not all; the 2627A has user-definable softkeys and graphics edit keys that make this one of the easiest-to-use terminals on the market. It even gives you complete alphanumeric capability. In a separate memory. So whether you're interested in business or technical applications, just return this coupon and we'll send you more information. Or call your local HP sales office. We're listed in the white pages.



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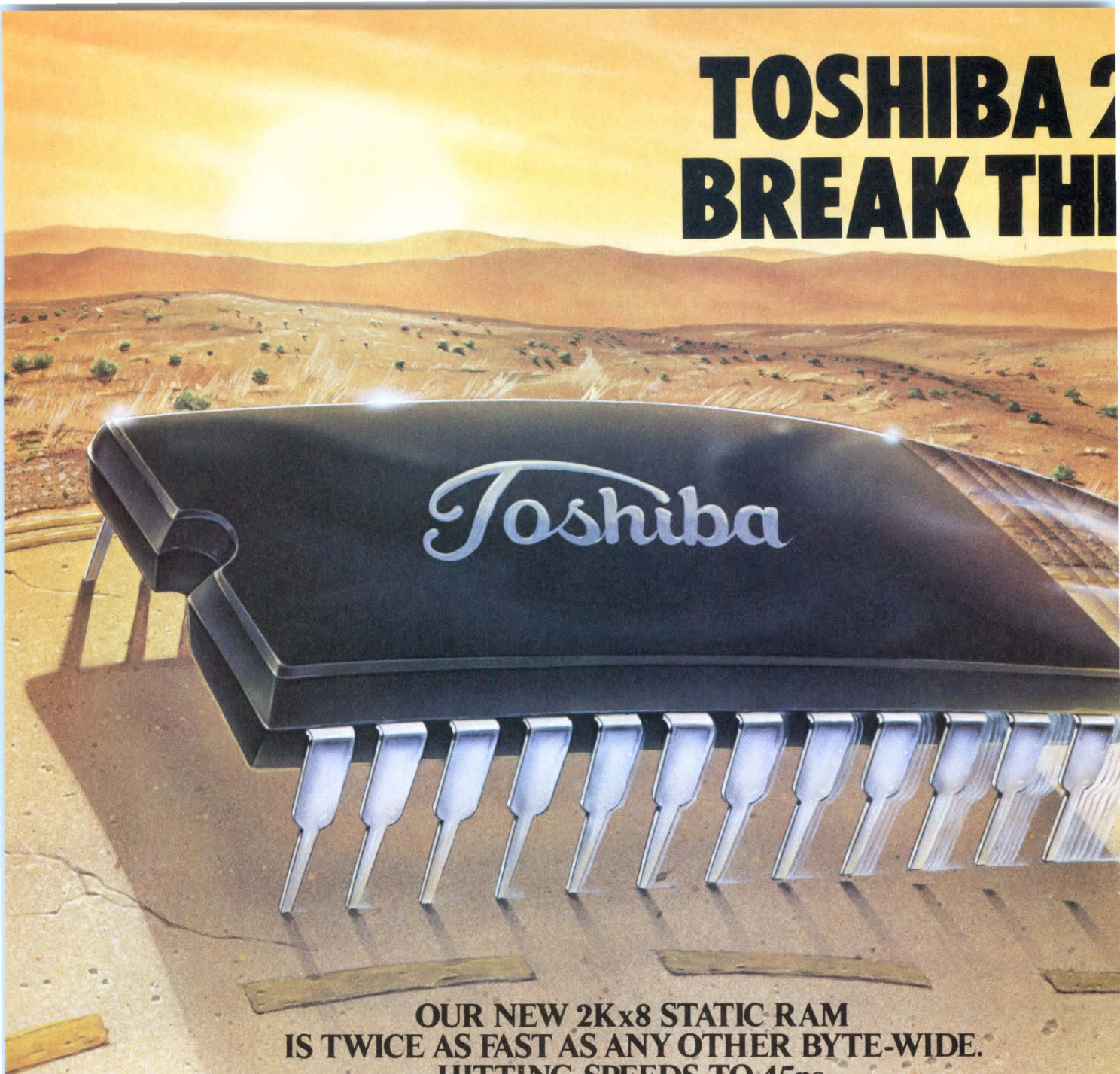
CIRCLE 133

TOSHIBA 2
BREAK THI



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All our high-speed *NMOS* and *CMOS* 2K x 8's are designed for maximum compatibility with microprocessor bus structures.

In fact, ours were the first 16K CMOS RAMs on the market. We designed them for a maximum 1μA standby current.

Operating from a single 5V power supply, our byte-wide RAMs are available in a 24-pin package, DIP (.300″ or .600″), flat pack and a variety of other configurations.

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Part No.	Type	Access Time (Max)	Operating Current (Max)	Standby Current (Max)
2016P	NMOS	150ns	100mA	15mA
2016P-1	NMOS	100ns	120mA	15mA
2016P-2	NMOS	200ns	140mA	30mA
*2016AP-9	NMOS	90ns	80mA	7mA
*2016AP-10	NMOS	100ns	65mA	7mA
*2016AP-12	NMOS	120ns	65mA	7mA
*2016AP-15	NMOS	150ns	65mA	7mA
**2018D-45	NMOS	45ns	120mA	20mA
**2018D-55	NMOS	55ns	120mA	20mA
5516P	CMOS	250ns	55mA	30μA
5516P-2	CMOS	200ns	55mA	30μA
5516PL	CMOS	250ns	55mA	1μA
5516PL-2	CMOS	200ns	55mA	1μA
5517BP	CMOS	200ns	25mA	30μA
5517BPL	CMOS	200ns	25mA	1μA
5518BP	CMOS	200ns	25mA	30μA
5518BPL	CMOS	200ns	25mA	1μA

*Also available in a .300" wide package — Part No. 2015-XX.
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CIRCLE 134

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Right-angle female headers

Double-row headers mate with 0.025 in^2 (0.161-cm^2) posts on a 0.1″ x 0.1″ (0.3- x 0.3-cm) grid, and come in 2- to 126-contact configurations. Contacts are selectively gold plated or solder plated. Each header's dielectric body is made of glass-filled polyester and is unaffected by flow soldering or board cleaning solvents. Twin-beam redundant contacts furnish reliable performance, and the headers' solder tails are positioned by a notched insulator for easy insertion onto PCBs. **Aptronics, Div of Products Inc,** PO Box 540, Mentor, OH 44060.
Circle 446

Wrappable logic board

Multibus compatible Series 2200 board features a universal layout for 0.300″, 0.400″, 0.600″, and 0.900″ (0.762-, 1.016-, 1.524-, and 2.286-cm) spaced devices; it also includes a 68-pin JEDEC type A LCC socket with wrappable pinouts. Board capacity is 28 cols of 53 pins each. Edge connectors include one 86-pin model [two rows of 43 pins each on 0.156″ (0.396-cm) centers] and one 60-pin model [two rows of 30 each on 0.100″ (0.254-cm) centers]. **Methode Electronics, Inc,** 7447 W Wilson Ave, Chicago, IL 60656.
Circle 447

PCB connectors

A 2-piece PCB connector consisting of a recepticle assembly and a perpendicularly mounted pin assembly provides high density interconnection. Recepticle assembly employs box-type contacts with 4 areas of contact/connection; pin assembly is available with flow solder or compliant pins. Contacts are arranged in 2, 3, or 4 rows with 60 to 684 rows per connector. **AMP Inc,** Harrisburg, PA 17105.
Circle 448

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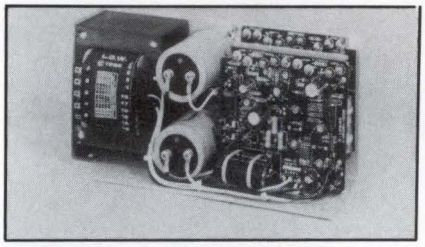
POWER SOURCES & PROTECTION

Linear power for disk memory



Model CP687 open frame dc power supply can drive any std 8″ or 5″ floppy, Priam or Seagate 506 hard disk, Shugart SA1000 series and QIC tape streamer. Output voltages and currents are 5 Vdc at 8 A avg, 9 A peak; −5 Vdc at 2 A; 12 Vdc at 3.5 A; −12 Vdc at 0.7 A; and 24 Vdc at 5.5 A avg, 7 A peak. Unit measures 10.88″ x 3.88″ x 5.5″ (27.64 x 9.86 x 14.0 cm). Input voltages include 100/120/220/230/240 Vac, ± 10%, 47 to 63 Hz. Power supply is designed for operation where adequate moving air is available. Unit price is $230. **Condor Inc,** 4880 Adohr Ln, Camarillo, CA 93010.
Circle 449

Transient suppressor board

Transient suppressor board HT-1301-B, for OEM and industrial control applications, provides dissipating capacity of 300 kW/ms, response time of 5-ns rise/10-ns recovery, and an alpha factor greater than 60. Board features autoranging for line voltage variations and auto adjust to clamp at 20% greater than line voltage peak. Unit operates on a standby current of less than 3 mA at 130 V and requires 2 power leads—a 110 to 130 Vac or Vdc and a 5-A external fuse. Available from stock, the board is priced at $172. **Hi-Tech Systems, Inc,** 3985 N State Rd 39, Lebanon, IN 46052.
Circle 450

Batteries back up memories

Lithium batteries can be soldered directly into PCBs and deliver a rated 3 V for memory backup. Three flat types have rated capacities from 120 to 200 mA, continuous discharge current of 0.1 to 0.2 mA, and pulse discharge current from 3 to 5 mA. Two cylindrical batteries have rated capacities of 160 to 1k mA, continuous discharge current of 1 and 2.5 mA, and pulse discharge current of 30 and 70 mA. **Sanyo Electric Inc, Battery Div,** 200 Riser Rd, Little Ferry, NJ 07643. **Circle 451**

Voltage surge suppressor

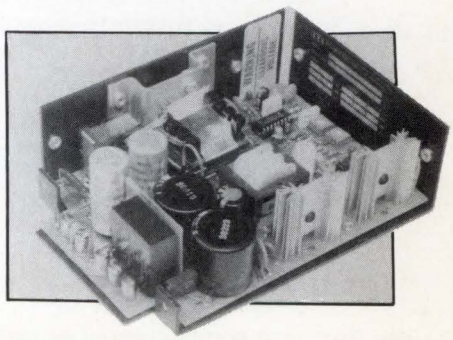
Model DPC-Plus Spike-Spiker has 8 individually switched, 120-V, 15-A outlets divided into 2 banks of 4 outlets each. Six-stage common- and differential-mode voltage spike suppression starts at 131 V and responds within 1 ps; absorption capacity equals 174.5 J. A 5-stage inductive/capacitive series/parallel low pass network furnishes noise filtering in both common and differential modes. **Kalglo Electronics Co, Inc,** 6584 Ruch Rd, Bethlehem, PA 18017.
Circle 452

Triple-output power supply

The ET50-3601 power supply, designed for microprocessor and CRT applications, can power 5″ disks, small printers, and cassettes. The supply uses a 15-pin DIN41612 connector and provides 5 V at 5 A, 12 V at 0.7 A, and REI filter, and VDE 0871 level B noise specs. Standard features include input surge, short circuit and overvoltage protection, and a power fail detect circuit. With triple output, the power supply sells for $91 in 100-piece quantities. **Boschert Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94086.
Circle 453

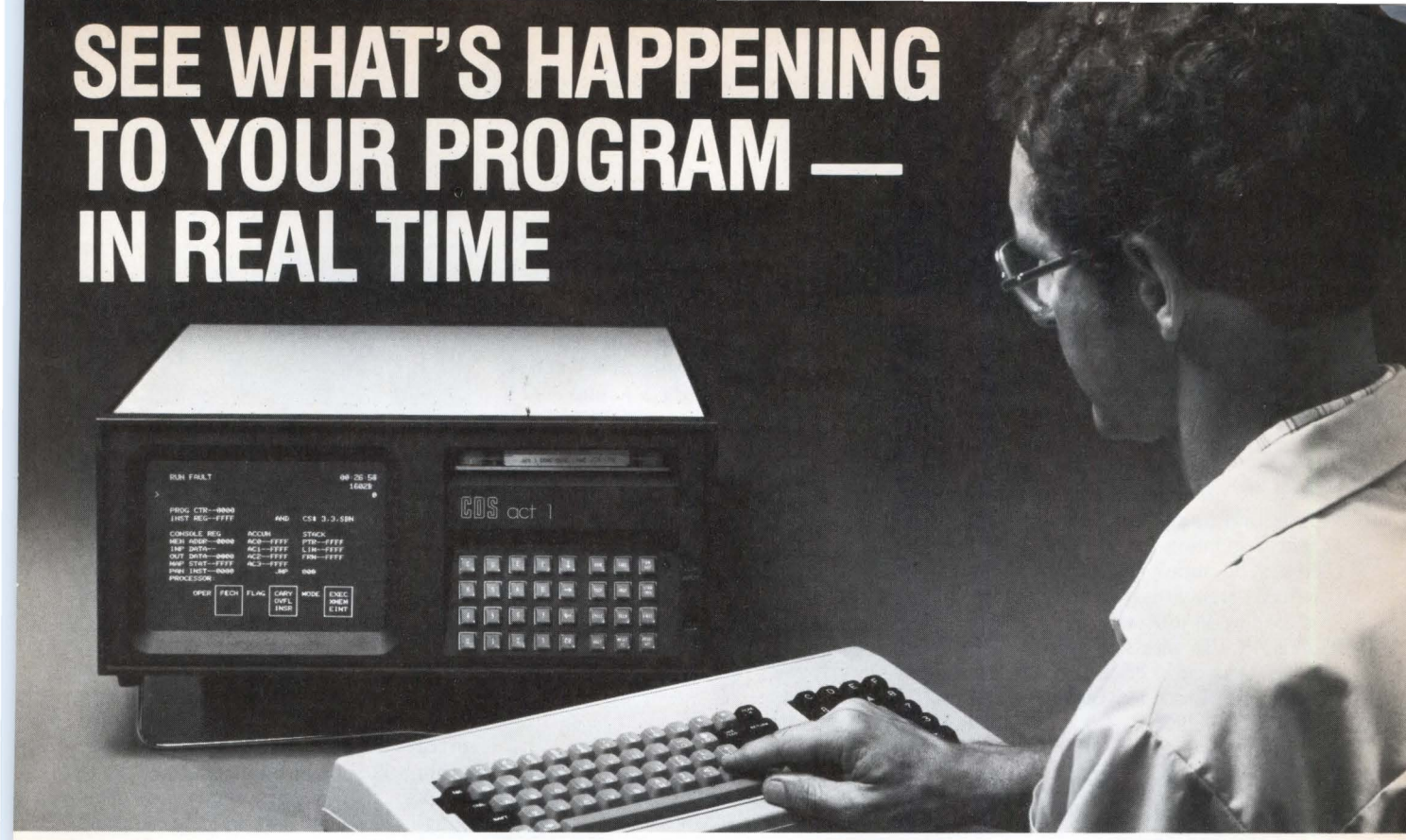
50- and 100-W switchers

ESP series switching power supplies include five models each at 50- and 100-W rating. They feature 100-kHz switching and input rfi filters to keep conducted interference within FCC specified limits. Std features include automatic current limiting, overvoltage protection, remote sensing, reverse voltage protection, soft starting, remote shutdown, and inrush current limiting. Input voltage is 95 to 130 Vac or 180 to 260 Vac; outputs include 5, 12, 15, 24, and 28 Vdc. Ripple and noise are 50 mV peak to peak; op temp range is 0 to 70 °C. **Power Pac Inc,** 32 Meadow St, South Norwalk, CT 06854.



Circle 454

SEE WHAT'S HAPPENING TO YOUR PROGRAM — IN REAL TIME



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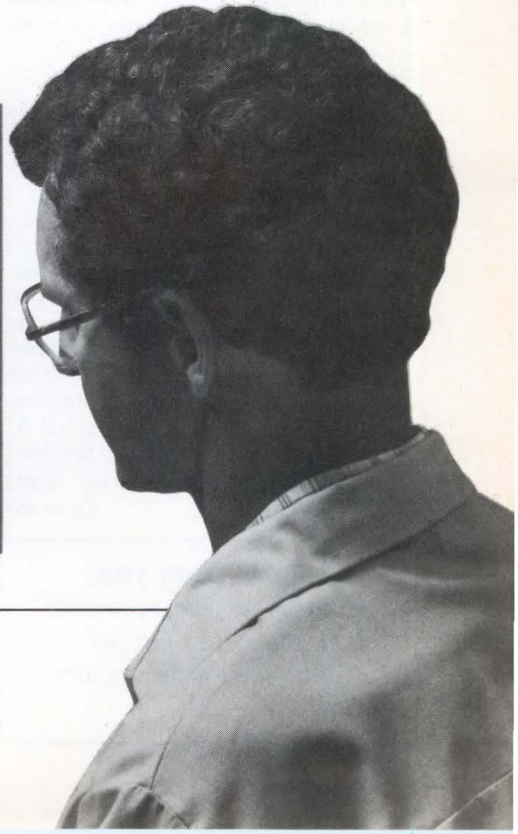

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CIRCLE 135

Switchers for low voltage ICs

Model PM2496A type 3.3D100 switching power supply is a single-output offline switcher that provides 3.3 V ±10% at 100 A, making it suitable for 3.3-V (nominal) logic level devices. Regulation is ±100 mV over the full ac input range, load variations, 0 to 50 °C op temp range, and initial warmup. Overload, overvoltage, overtemp, and reverse voltage protections are featured. Std features are remote sensing, ac input fuse, and power loss holdup that maintains regulation for 30 ms after ac input loss. The supply meets UL478 and CSA safety standards and radiated emi according to VDE 0871B. With an external filter, it also meets VDE 0871B specs for conducted emi. Price is $508. **Pioneer Magnetics Inc,** 1745 Berkeley St, Santa Monica, CA 90404. **Circle 461**

EEPROM power source

Compatible with EEPROM requiring 21 Vdc bias and operation, the VA 10.5-10.5 power source converts 5 V input to ±10.5 or 21 V with max current of 40 mA. Specs include noise of 50 mV RMS/100 mV peak to peak, I/O isolation of 10 MΩ, and an operating temp range of −25 to 70 °C. Power source is packaged in a dual-inline configuration, 1.1″ x 0.6″ x 0.4″ (27.9 x 15.2 x 10.1 mm) and is mounted directly on the PC board. Price per unit in quantities of 500 or more is in the $20 range, with delivery from stock. **Reliability Inc, Power Products Div,** PO Box 218370, Houston, TX 77218. **Circle 462**

Switching power on open PCB

The AC 8254 50-W multi-output switching power supply is suited for small microprocessor based systems running mixed logic applications that call for a 24-V supply. Unit offers jumper selectable input voltage for either 115 or 230 Vac and meets European safety standards. Fully tested with 100% thermal cycle, device also features a built-in emi filter, vacuum impregnated transformers, low output ripple, and overvoltage and short circuit protection. Outputs are 5 V at 2.2 A; 24 V at 1.3 A; and −5 V at 0.14 A. **Astec Services, Ltd,** 2840 San Thomas Expwy, Santa Clara, CA 95051. **Circle 463**

Let's hear from you

We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

65-W switching power

SX53-3501 is a fit, form, and function multi-output supply to the Boschert XL53-3501. It meets regulation and transient response on the 5- and 12-V outputs. Series meets VDE, UL, and CSA requirements with outputs of 5 V at 6 A; −5 V at 0.6 A; 12 V at 2.5 A; and −12 V at 0.6 A. Unit size is 7.75″ x 4.25″ x 2″ (19.69 x 10.80 x 5 cm). Features include short circuit and overvoltage protection, soft start, input emi filtering, 20-ms holdup, brownout rating, and user selectable 120/240 Vac. Price is $60. **Summit Electronics, Inc,** 750 S Sherman, Richardson, TX 75081.
Circle 464

DATA CONVERSION

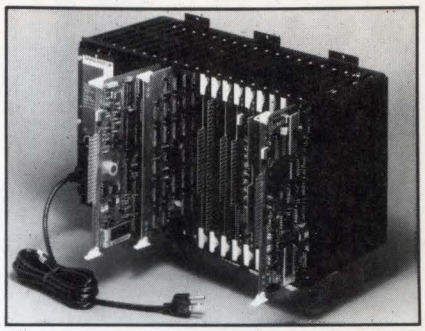
Differential absolute encoders

Scalable Series DDS90 encoders indicate the absolute difference between two rotating shafts with accuracies to 1 part in 3600. The devices convert any 2 shaft inputs to BCD or binary data, and 3-, 4-, and 5-digit, 0.5″ (1.3-cm) high LEDs are available. Data outputs are TTL compatible; data transfer and data hold lines simplify computer interface. The basic data update rate is 2.5 ms; 600-μs performance is optional. Op temp range is 0 to 70 °C or −55 to 85 °C. NEMA 12, waterproof, and explosion-proof transducer housings are optional. Prices start at $595 per axis in unit quantities. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731.
Circle 465

Inductosyn-to-digital converters

Series SDC-19100 converts the slider outputs of Farrand Industries's Inductosyn devices to digital codes. With an LSI chip and hybrid construction, the units achieve 10-, 12-, or 14-bit resolution at ±21-, ±8.5-, or ±5.3-min accuracies, respectively. A Type II tracking loop design eliminates velocity lag when operating at or below the specified tracking rate (960 rpm for the 14-bit unit to 15,000 rpm for the 10-bit unit). Three-state latched outputs facilitate microprocessor interfacing. Other features include direction and count outputs and 1-LSB repeatability. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.
Circle 466

Data acquisition system



The ANDS440 is a close-coupled, coprocessing multiloop system for regulating temp, pressure, voltage, and current in industrial environments. Compatible with RS-232-C or 2-mA serial port, the system provides fully isolated analog and digital I/O. There are 3 versions: prompt proportional/digital controller, prompt PID/digital controller, and BASIC PID/sequencing coprocessing controller. Plug-in cards are available to extend the system for both processing and programming. **Analogic Corp,** 14 Electronics Ave, Danvers, MA 01923.
Circle 467

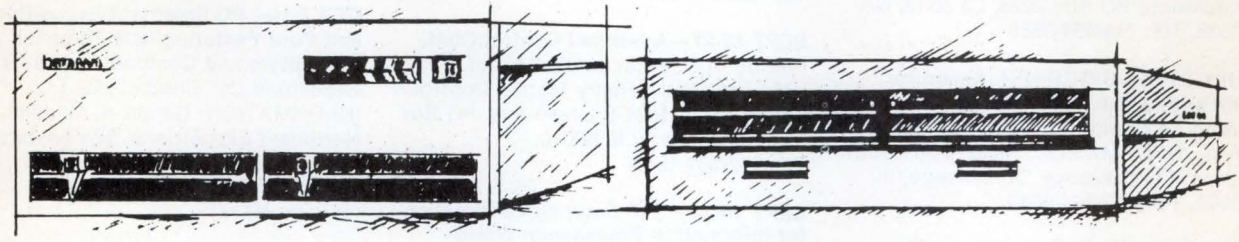
Color-mapped video DACs

Compact RGB DAC 4T, 8T, and 8E units combine 3 complete sets of video frequency DACs with color lookup table RAMs and associated logic and control circuitry. The 4-bit DAC displays up to 4096 colors and provides update rates to 40 MHz with a 5-ns settling time to 1 LSB. Eight-bit models have over 16.7M possible colors. The 8T operates at 70 MHz and the 8E at 135 MHz; both have an 8-ns settling time to 1 LSB. The 4T and 8T are TTL compatible; 8E is ECL compatible. **Intech, Inc, Microcircuits Div,** 2270 Martin Ave, Santa Clara, CA 95050.
Circle 468

High accuracy DAS

ICE-108A data acquisition and control system operates as a computer peripheral on the IEEE 488 bus. Accurate to 0.005% at 23 °C, the instrument offers 39,999-count resolution and a voltage range of 399.99 mV to 300 V. Floating bipolar differential input, 140-dB CMRR, ±300-Vdc CMV, and 90-dB NMRR are also featured. ADC performs 10 samples/s and 9.7 scans/s. Main chassis provides an integrating DVM and 8 plug-in boards, as well as addressing and data/control interfaces. **Advanced Technology Research Laboratories Ltd,** 5645K General Washington Dr, Alexandria, VA 22312. **Circle 469**

DEC-COMPATIBLE DISKS FOR LESS



Dataram has acquired Charles River Data Systems' DEC-compatible product line. We will continue to offer their popular FD-311 dual floppy subsystems and have added an exciting new floppy-based system, Dataram's A21.

Q-bus and UNIBUS compatible versions of the FD-311 provide dual RX02-compatible 8" floppy drives for $2,400. Our new 7" high A21 combines dual RX02-compatible 8" slimline floppies with an 8-quad slot Q-bus card cage for only $3,500. Both products are supported by the industry's widest range of LSI-11 compatible products. Call or write for details.

DATARAM

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CIRCLE 136

CONFERENCES

JULY 11-13—Computer Simulation Conf, Hyatt Regency Vancouver, Vancouver, BC, Canada. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 714/459-3888

JULY 25-29—SIGGRAPH (Assoc for Computing Machinery Special Interest Group on Computer Graphics), Detroit, Mich. INFORMATION: SIGGRAPH Conf Office, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

AUG 9-11—World Congress on the Human Aspects of Automation, Univ of Michigan, Ann Arbor, Mich. INFORMATION: Pat Van Doren, Technical Activities Dept, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1080 X369

AUG 23-26—Internat'l Conf on Parallel Processing, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 12-14—IEEE Internat'l Conf on Computer Aided Design, Santa Clara, Calif. INFORMATION: John A. Domiter, American Bell Inc, PO Box 3505, New Brunswick, NJ 08903

SEPT 13-15—Autofact Europe, Palexpo Conf and Exhibition Ctr, Geneva, Switzerland. INFORMATION: Automated Systems Assoc, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500

SEPT 13-15—Federal Computer Conf, Washington Conv Ctr, Washington, DC. INFORMATION: Federal Education Programs, PO Box 368, Wayland, MA 01778. Tel: 617/358-5181; 800/225-5926 (outside Mass)

SEPT 13-15—Midcon, O'Hare Expo Ctr and Hyatt Regency O'Hare, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Mini/Micro-Midwest, O'Hare Expo Ctr, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Peripherals, Moscone Ctr, San Francisco, Calif. INFORMATION: Cahners Expo Group, Cahners Plaza, 1350 E Touhy Ave, PO Box 5060, Des Plaines, IL 60018. Tel: 312/299-9311

SEPT 13-15—WPOE (Word Processing and Office Environment Show and Conf), San Jose Conv Ctr, San Jose, Calif. INFORMATION: Cartlidge & Assocs, Inc, 4030 Moorpark Ave, Suite 205, San Jose, CA 95117. Tel: 408/554-6644

SEPT 19-21—Advanced Control Conf, Purdue Univ, West Lafayette, Ind. INFORMATION: Henry Morris, Control Engineering, 1301 S Grove Ave, PO Box 1030, Barrington, IL 60010. Tel: 312/381-1840

SEPT 19-23—IFIP (Internat'l Federation for Information Processing) World Computer Congress, Paris, France. INFORMATION: Philip H. Dorn, Dorn Computer Consultants, Inc, 25 E 86th St, New York, NY 10028. Tel: 212/427-7460

SEPT 20-21—Data Storage, Marriott Hotel, Santa Clara, Calif. INFORMATION: Cartlidge & Assocs, Inc, 4030 Moorpark Ave, Suite 205, San Jose, CA 95117. Tel: 408/554-6644

SEPT 26-29—Compcon Fall, Mariott Gateway, Crystal City, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 26-28—Maecon, Kansas City Conv Ctr, Kansas City, Mo. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 29-30—CAD/CAM and Simulation Conf, Westin Hotel, Boston, Mass. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 619/459-3888

OCT 2-5—Robotech (Internat'l Conf and Exposition for the Application of Automated Manufacturing Technology), Curtis Hixon Convention Hall, Tampa, Fla. INFORMATION: Tom Will, Latcom Inc, 4135 Laguna, Coral Gables, FL 33146. Tel: 305/667-5150

July Preview—
Watch for a major staff-written review on workstations for computer aided engineering.

OCT 3-6—Data Communications Symposium, Cape Cod, Mass. INFORMATION: Kenneth J. Thurber, Architecture Technology Corp, PO Box 24344, Minneapolis, MN 55424. Tel: 612/935-2035

OCT 8-10—PC (Internat'l Exposition and Conf Featuring IBM Personal Computers and Compatibles), Bayside Exposition Ctr, Boston, Mass. INFORMATION: Gerald A. Milden, Northeast Expositions, 826 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/343-2222 (outside Mass)

OCT 10-13—ISA (Instrument Society of America) Internat'l Conf and Exhibit, Astrohall, Houston, Tex. INFORMATION: Philip Meade, ISA, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

OCT 12-14—Fiber Optic Communications Local Area Network Applications, Atlantic City, NJ. INFORMATION: Tom Coggeshall, IGI, 167 Corey Rd, Brookline, MA 02146. Tel: 617/739-2022

OCT 18-20—Internat'l Test Conf, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Doris Thomas, PO Box 371, Cedar Knolls, NJ 07927. Tel: 201/267-7120

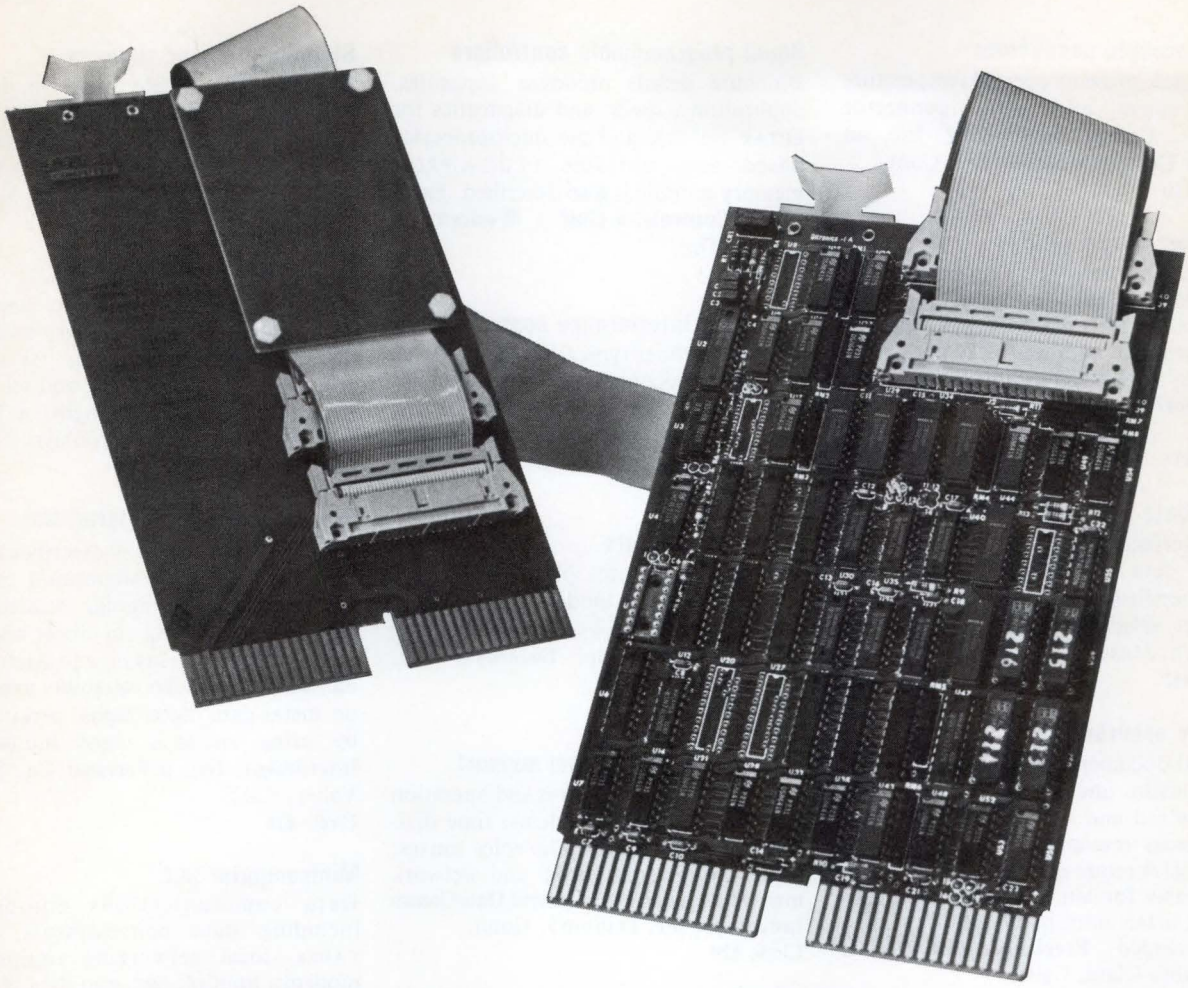
WORKSHOPS

AUG 1-5—Hands-on Pascal Computer Programming, AUG 8-12—Hands-on Programming in Ada, AUG 15-19—Interactive Computer Based Systems Design and Development, AND AUG 16-19—Intelligent Robots: The Integration of Microcomputers and Robotic Technology, George Washington Univ, Washington, DC. INFORMATION: Douglas Green, Continuing Engineering Ed, George Washington Univ, Washington, DC 20052. Tel: 202/676-8512; 800/424-9773 (outside DC)

AUG 8-12—Contemporary Data Communication Networks: Planning Analysis and Design, AND AUG 15-18—Software Design Techniques and Ada, Univ of Michigan, Ann Arbor, Mich. INFORMATION: Viola E. Miller, Continuing Engineering Ed, 300 Chrysler Ctr, North Campus, Ann Arbor, MI 48109. Tel: 313/764-8490

AUG 8-18—Data Communications, Iowa State Univ, Ames, Iowa. INFORMATION: Paul Bond, 131K Coover Hall, Iowa State Univ, Ames, IA 50011. Tel: 515/294-1526

PDP-11/23 with 4 Megabytes of Q-BUS Memory. Impossible? Read On.



If you've outstripped your 256 kbyte addressing capability, if you want a reliable solution to your memory expansion needs, and if budget is a concern, we have the answer. We have made life on the Q-Bus a lot easier. QNIMAP,™ another outstanding Q-Bus product from Able Computer, allows for full memory expansion up to 4 megabytes of main memory and the use of existing Q-Bus DMA devices. With QNIMAP,™ you get system performance you never thought possible along with complete support from Able. The QNIMAP™ consists of two easy to install dual width boards and is software compatible with RSTS/E, RSX-11 and UNIX.

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- QNIVERTER™ – Bi-directional Q-Bus to Unibus/Unibus to Q-Bus signal converter for memory and peripheral devices.
- UNIMAP™ – Memory expansion to 4 megabytes on the PDP-11/23. Allows use of 18 bit Unibus devices.
- INTERLINK™ – DMA interprocessor link between two Unibus, two Q-Bus, or one Q-Bus and one Unibus system.

Find out more about QNIMAP™ and the rest of of our Q-Bus products. Write or call for details. Able Computer, 1732 Reynolds Avenue, Irvine, California 92714. National offices: Irvine CA (714) 979-7030, Burlington MA (617) 272-1330, Rumson NJ (201) 842-2009. International offices: Canada (Toronto) (416) 270-8086, England (Newbury) (0635) 32125, W. Germany (Munich) (089) 463080. For immediate, toll-free information, dial (800) 332-ABLE.

ABLE COMPUTER

Q-Bus, Unibus, RSTS/E, RSX/11 and PDP are trademarks of Digital Equipment Corporation. UNIX is a trademark of Bell Laboratories.

CIRCLE 137

Thermocouple connectors
Handbook presents over 50 temperature measurement and panel connector systems. **Omega Engineering, Inc, an Omega Group Co,** Stamford, Conn.
Circle 410

RF emission regulations
Booklet gives overview of standards for acceptable rf emission from electronic products in various countries; address and telephone numbers of 26 regulatory agencies around the world are listed. **Sierracin/Power Systems,** Chatsworth, Calif.
Circle 411

LSI-11 data acquisition
Bus interface products for A-D, D-A, and digital data conversion are illustrated and specified in catalog that includes product selection tables. **ADAC Corp,** Woburn, Mass.
Circle 412

Quality assurance
Manual documents basic procedures for manufacture and reliability monitoring of standard and custom-contract products; cross reference of MIL-Q-9858 and MIL-M-38510 requirements, in addition to flowcharts for MIL-STD-883 method 5004 class S, B/JAN 38510, and C qualifications, are included. **Precision Monolithics, Inc,** Santa Clara, Calif.
Circle 413

Printer selection
Guide profiles a variety of 27- and 40-column models, outlining printer specs as well as controller, power supply, and mechanical subsystems for custom assemblies. **Printer Products, div of Capitol Circuits Corp,** Boston, Mass.
Circle 414

Elastomeric keyboards
Wild Rover® KB series 3 x 4 keyboards are examined in spec sheet that sets forth features and applications as well as circuit and dimensional diagrams. **REFAC Electronics Corp,** Winsted, Conn.
Circle 415

Motor reference
Catalog gives complete specs and application data for off-the-shelf motors, gearmotors, and electronic motion controls. Photos and selection information tables complement dimensional drawings and text. **Bodine Electric Co,** Chicago, Ill.
Circle 416

Small programmable controllers
Brochure details processor capacities, applications, specs, and diagnostics for EPTAK 210, 220, and 240 microprocessor based PCs; portable PLUG-A-PROM memory module is also described. **Eagle Signal Controls, a Gulf + Western Co,** Austin, Tex.
Circle 417

Computer interference control
Booklet outlines typical applications for equipment isolators, ac power line filters/suppressors, line voltage regulators, and ac power interrupters. **Electronic Specialists, Inc,** Natick, Mass.
Circle 418

Computer printers
Brochure introduces principal features and options of 9 models ranging from basic dot-matrix to 4-color multipurpose printers. **Facit, Inc, Dataroyal Div,** Nashua, NH.
Circle 419

International telecomm support
Booklet describes features and operation of 300- to 16k-bps modems; time division, statistical, and data/voice muxes; local network products; and network management systems. **General DataComm Industries, Inc,** Danbury, Conn.
Circle 420

Nonvolatile memory
Handbook provides detailed data sheets and application notes for electrically alterable memory ranging from an 82-bit EAROM to a 16K-bit word-alterable EEPROM and a 4K-bit nonvolatile static RAM. **General Instrument Corp, Microelectronics Div,** Hicksville, NY.
Circle 421

Surge protection and test
Introductory guide outlines circuit design and test techniques for countering transient voltage spikes and current surges, and examines IEEE 587 standard for ac power lines. **KeyTek Instrument Corp,** Burlington, Mass.
Circle 422

Microminiature D connectors
High density metal- and plastic-shell MIL-C-83513 connectors are specified in booklet that lists performance data/materials, cutout dimensions/contact arrangements, and mounting/coupling hardware. **Malco, div of Microdot Connector Group,** Montgomeryville, Pa.
Circle 423

Switching power supplies
Booklet reviews state of the art design, along with measurement techniques, paralleling, load sharing, and switching supply applications. **CEAG Electric Corp, Power Supply Div,** Hauppauge, NY.
Circle 424

Illuminated push buttons
Catalog describes switches, specifies electrical/mechanical ratings, and lists materials and finishes for 554 series; schematics, tables, charts, and selection guide are included. **Dialight, a North American Philips Co,** Brooklyn, NY.
Circle 425

Semicustom Linear/digital ICs
Application note APN-30 describes how a high speed logic configuration can be implemented on bipolar semicustom chips primarily used for linear applications; APN-32 explains how to stretch the limited linear design capability available on metal gate CMOS digital array chips by using an MLA CMOS monochip. **Interdesign, Inc, a Ferranti Co,** Scotts Valley, Calif.
Circle 426

Minicomputer DCE
Data communications equipment including data concentrators, data PABXs, local networking equipment, modems, multiplexers, and data sets are described in short-form ordering catalog. **Micom Systems, Inc,** Chatsworth, Calif.
Circle 427

High density Euro connectors
Catalog gives specs, dimensional drawings, and application data for 2-piece DIN-41612 connector types R, B, C, D, F, G, and H. **Methode Electronics, Inc,** Chicago, Ill.
Circle 428

Private communication networks
Tutorial brochure explains networking economics and technologies in available systems. Request on company letterhead from: Judith Allen, **Harris Corp, Telecommunication Networks Div,** PO Box 1040, Melbourne, FL 32901.

Fiber optic data cables
Brochure describes cables with 4 to 6 graded index fiber channels, as well as general purpose simplex and heavy duty duplex versions, tabulating performance/installation specs and attenuation ranges. **Valtec,** West Boylston, Mass.
Circle 429

Bar-coded or alphanumeric labels, tickets, and tags...

1, 2, or 200 at a time.

The new Zebra™ Demand Printer offers unmatched flexibility. Unlike general-purpose printers, it delivers labels, tickets, or tags **when** and **where** you need them—in a form that's easy to use. It dispenses pressure-sensitive labels, either in strips or individually with the backing removed. It's ideal for tag and ticket printing, since it handles multipart forms and card stock up to .016" (16 point). And the Zebra saves you money because it doesn't require expensive thermal or pin-fed papers. There is no waste—you print only what you need.

The Zebra is a high-speed, bidirectional, dot-matrix printer that offers the complete flexibility to print nine different bar code symbologies (including LOGMARS) in 37 different sizes—all in specification—plus OCR and four sizes of alphanumerics. And you're free to change printing format with each printout, so the Zebra can meet a variety of printing needs.

The Zebra is a "smart" printer, too. Interface the Zebra with a basic ASCII keyboard or CRT and you'll have a complete label preparation system. Or input data from your computer via a standard RS-232C port.

The Zebra is built to last and is "ruggedized" to withstand industrial environments. Its unique harmonic drive motion significantly reduces vibration, giving you more accurate printing, with a print-head life rated at 300 million characters. You may have thought you couldn't cost-justify a bar code printer. But the Zebra is priced at **less than half** that of comparable printers, so you can conveniently set up one or more in your operation.

Find out how the Zebra can improve your information handling—call or write today.

Zebra
DEMAND PRINTER

Data Specialties, Inc.
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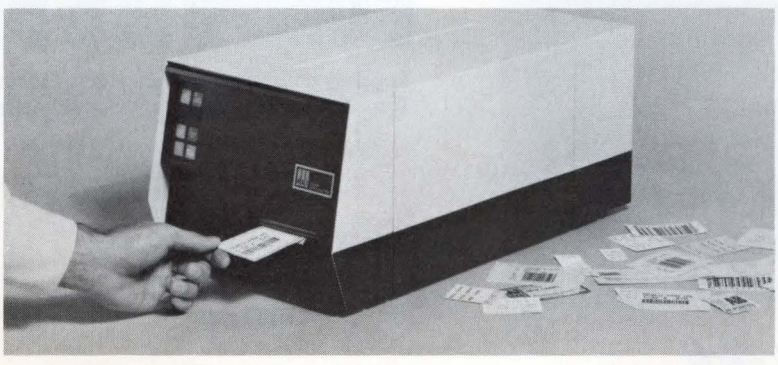
Northbrook, Illinois 60062
(312) 564-1800
Telex 206230



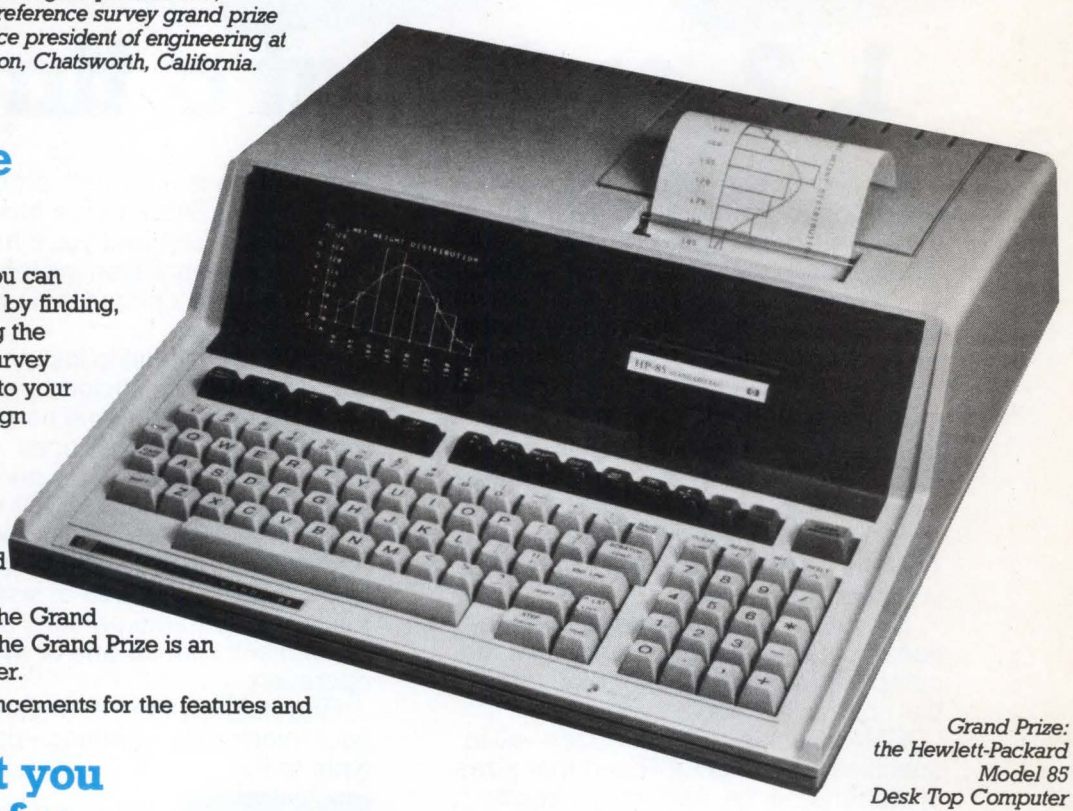
CIRCLE 138

COMPUTER DESIGN ANNOUNCES . . .

Tom Boris (left), Computer Design representative, presenting the Designer Preference survey grand prize to Mr. Stan Nackdymon, vice president of engineering at Waugh Controls Corporation, Chatsworth, California.

the GRAND PRIZE WINNER!

Stan Nackdymon wins the HP-85 in our Designer Preference survey prize drawing.



Grand Prize: the Hewlett-Packard Model 85 Desk Top Computer

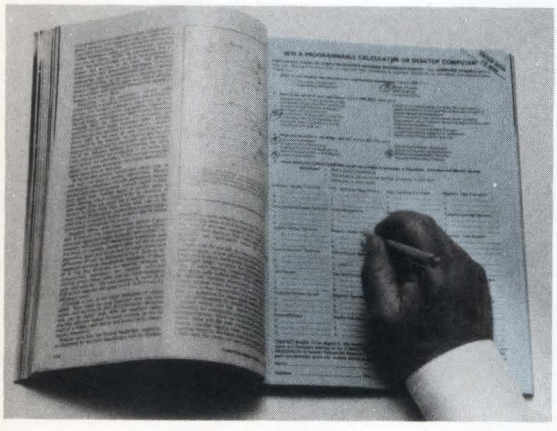
What about your chance to be a winner?

You can enter the prize drawing by finding, filling out, and returning the Designer Preference Survey questionnaire bound into your copy of Computer Design every month.

Your entry goes into a monthly drawing for an HP 41C calculator. Winners are announced monthly. In addition, all entries are eligible for the Grand Prize annual drawing. The Grand Prize is an HP-85 desk top computer.

See our monthly announcements for the features and details on the prizes.

Here's what you should look for



Best of Luck!

COMPUTER DESIGN

The only computer magazine that concentrates on design.
The only design magazine that concentrates on computers.

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July 25-29
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- Two evenings of computer-generated film & video shows
- A public showing of computer-generated art

The full spectrum of graphics

SIGGRAPH '83 attendance is mandatory for professionals striving to keep their computer graphics knowledge sharp. For registration information, contact the SIGGRAPH '83 Conference Office, 111 East Wacker Drive, Chicago, Illinois 60601; (312) 644-6610. Or, plan to register on site in Detroit on Sunday, July 24, between 1 p.m. and 11 p.m.

acm

Line printer maintenance
Booklet examines major aspects of operation, summarizing how to keep units functioning well in an applications environment. **Digital Associates Corp,** Stamford, Conn.
Circle 430

Monitor/control systems
Leaflet specifies Digistrip® IV and Digi-Link IV, showing process diagrams of control features and applications. **Kaye Instruments Inc,** Bedford, Mass.
Circle 431

3-output dc-dc converters
Technical data sheet gives electrical/mechanical specs for C series 9-W units, with application information, photos, and dimensional drawings. **Stevens-Arnold, sub of Computer Products, Inc,** South Boston, Mass.
Circle 432

Office automation planning
Brochure reviews office automation strategy, from architecture and selection to implementation. **McQuillan Consulting,** Cambridge, Mass.
Circle 433

Motor controllers
Brochure covers series 5600 programmable controllers, discussing capabilities as well as relay, timing, arithmetic, and sequencing functions. **Gould Inc, Industrial Controls Div,** Westminster, Md.
Circle 434

Network management
Data sheets for remote sense/control and automatic calling units examine features, benefits, and technical specs; sample configuration diagram of each is included. **Paradyne Corp,** Largo, Fla.
Circle 435

Time dimension multiplexer
Line drawings and photos illustrate brochure that describes applications and system operating principles of bit synchronous processors. **Scitec Corp,** Middletown, RI. **Circle 436**

Factory automation
Brochure reviews Loginet system, highlighting programmable controller networks designed to improve productivity; several applications examples are included. **Logicon, Process Systems Div,** Fairfax, Va. **Circle 437**

6502/6522 measurement system
Application note describes TSC7135 A-D converter interface to microprocessor based data acquisition and process control, including circuit schematics and hardware/software examples. **Teledyne Semiconductor,** Mountain View, Calif.
Circle 438

Miniature power supplies
Single-, dual-, and triple-output models are examined with detailed specs and outline drawings for screw connections as well as logic/op amp PC board mounts. **Acopian Corp,** Easton, Pa.
Circle 439

Proving computer/controller
Folder covers operating features, interfaces, and specs, in addition to system and application diagrams, for model 1010. **Waugh Controls Corp,** Chatsworth, Calif. **Circle 440**

MIL-C-5015 connectors
Catalog gives insert arrangements, conversion tables, dimensional drawings, and photos of connectors and assemblies. **Crown Connector, Inc,** San Fernando, Calif. **Circle 441**

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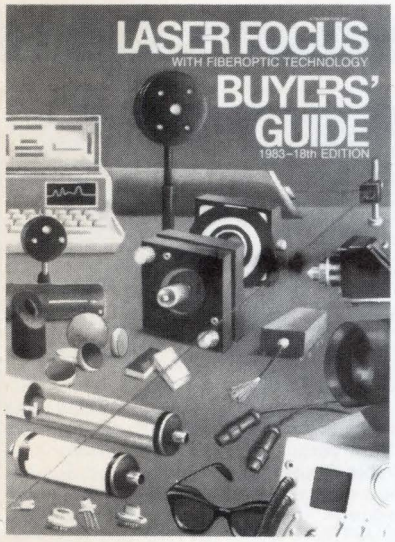

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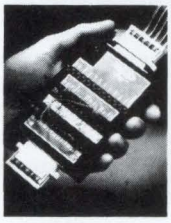

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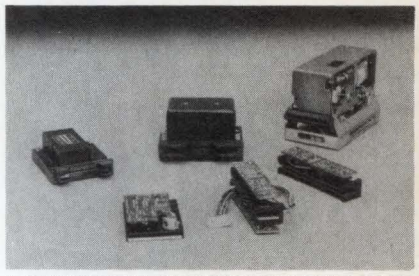

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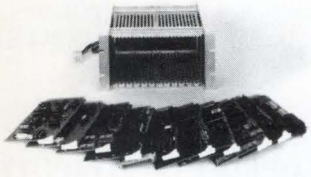

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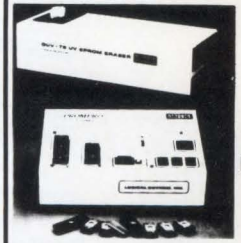

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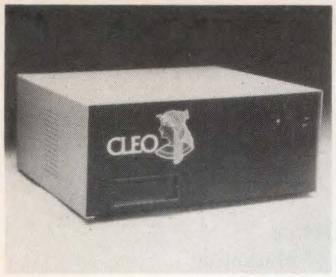

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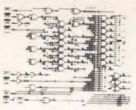

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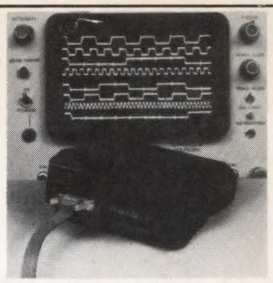

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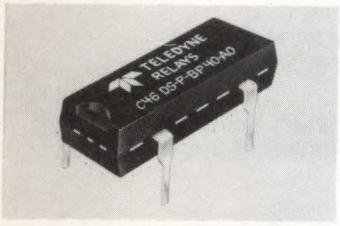

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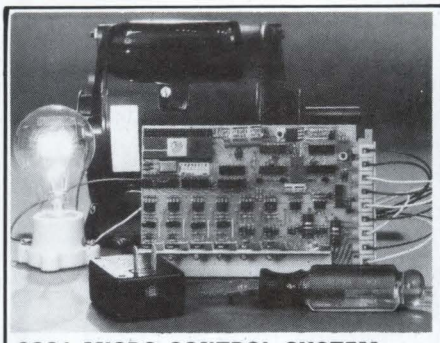

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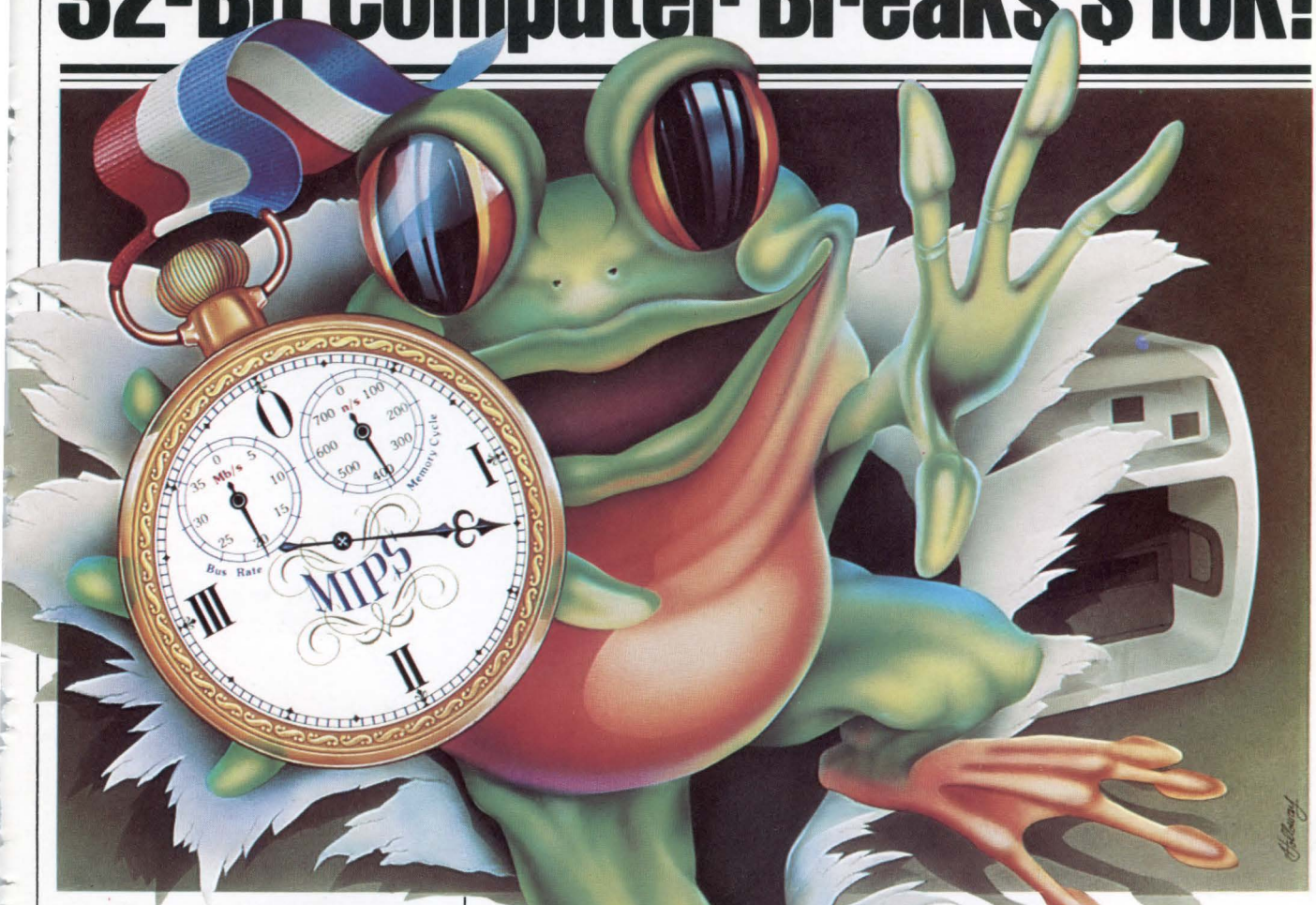

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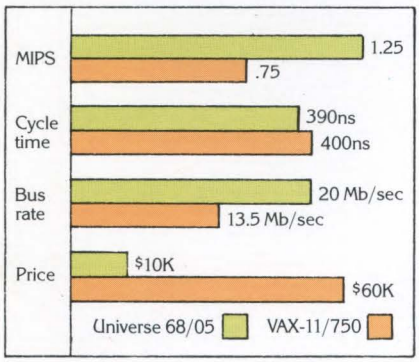

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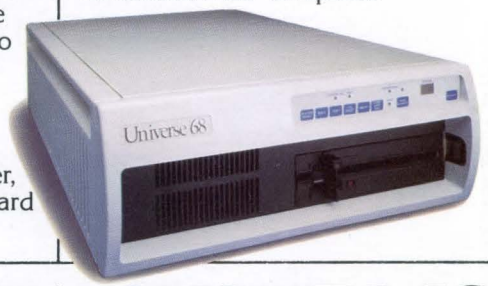

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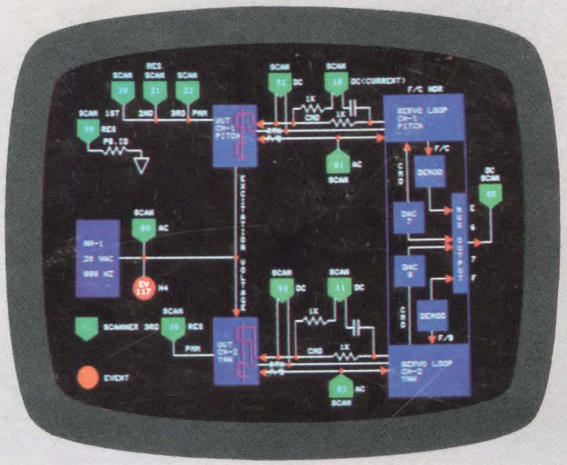

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