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MARCH 1984

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

ADVANCED DIGITAL ICs

DESIGNING SEMICUSTOM CHIPS

DOT-MATRIX PRINTER TECHNIQUES

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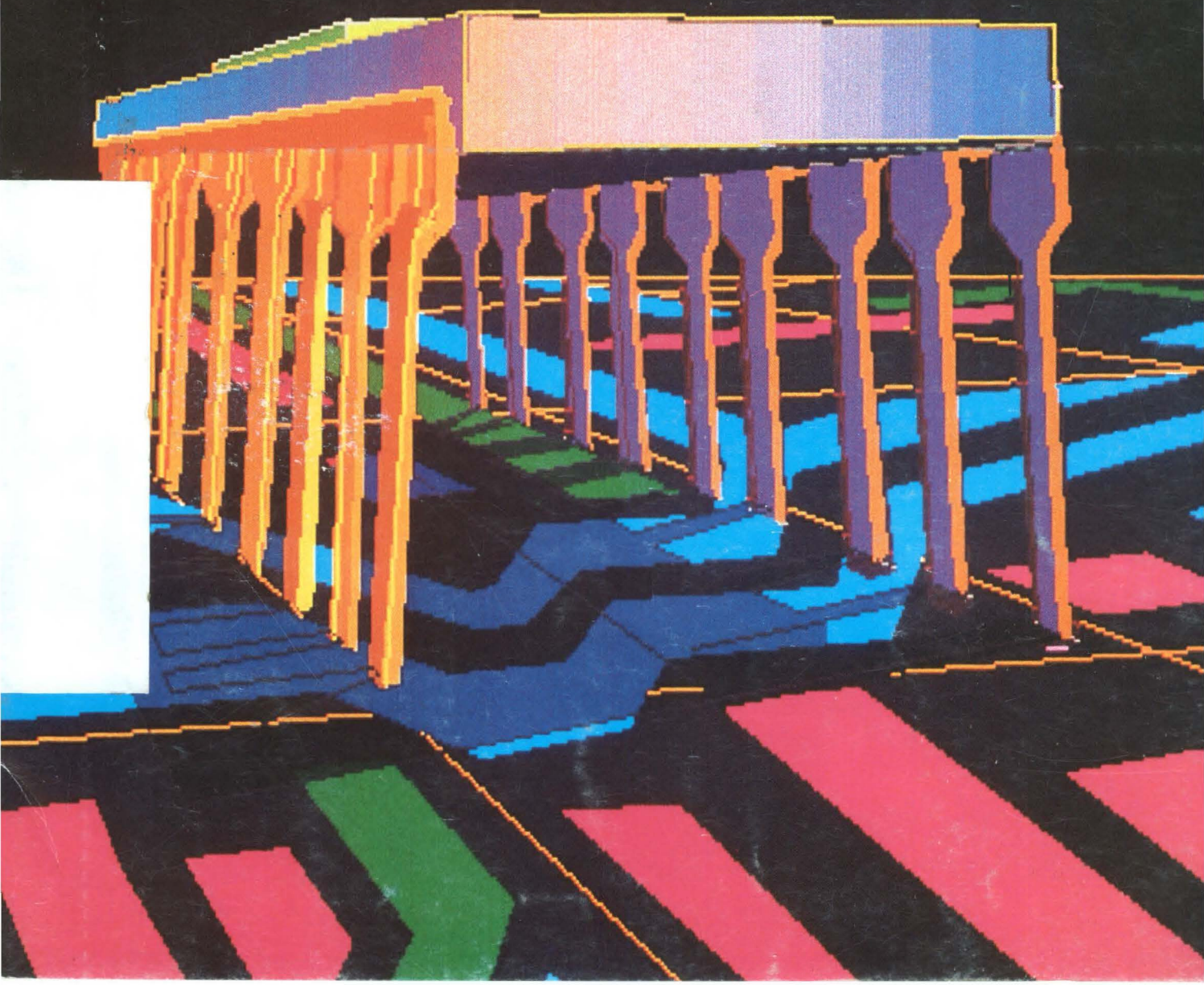

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CIRCLE 1

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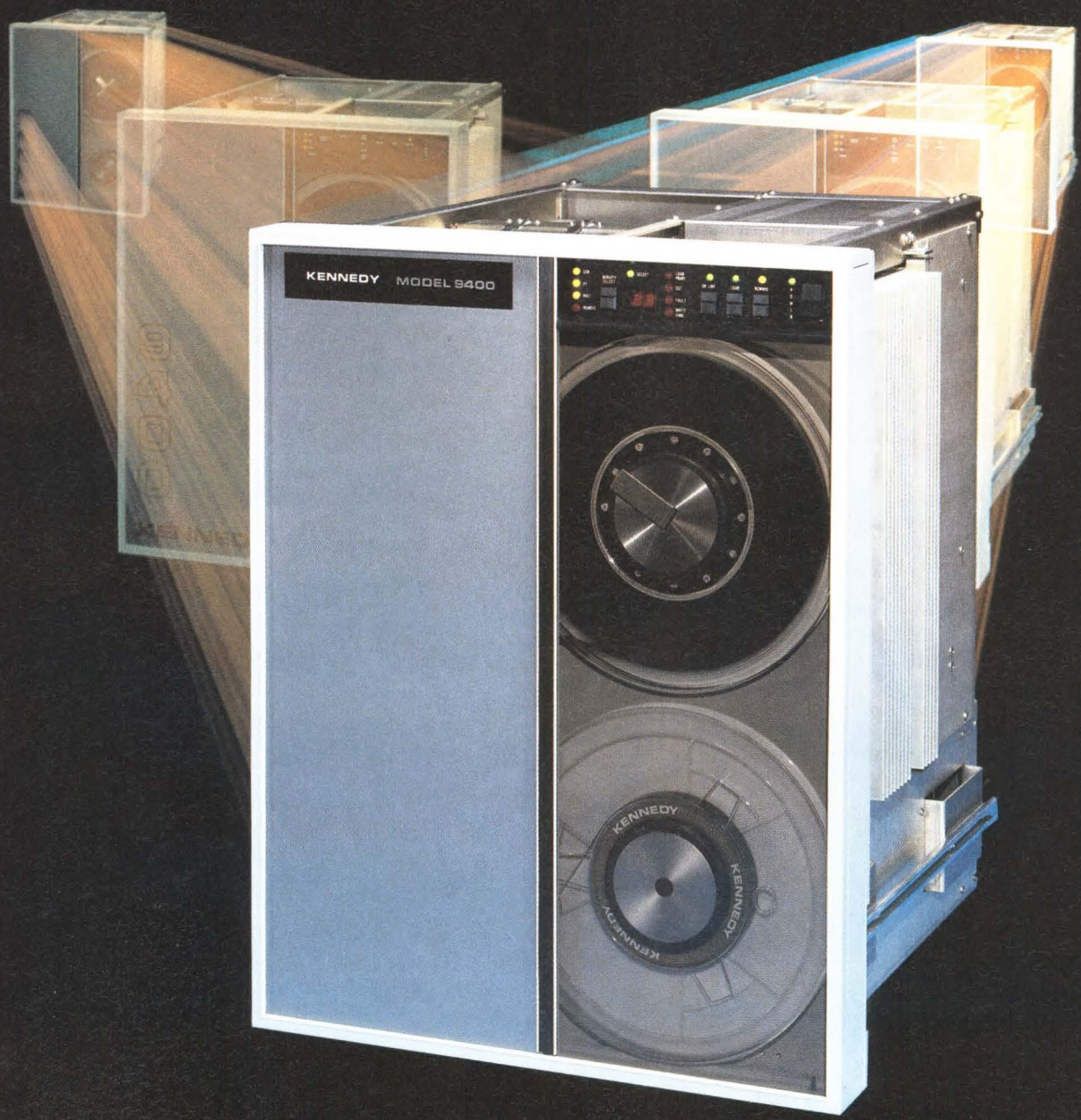

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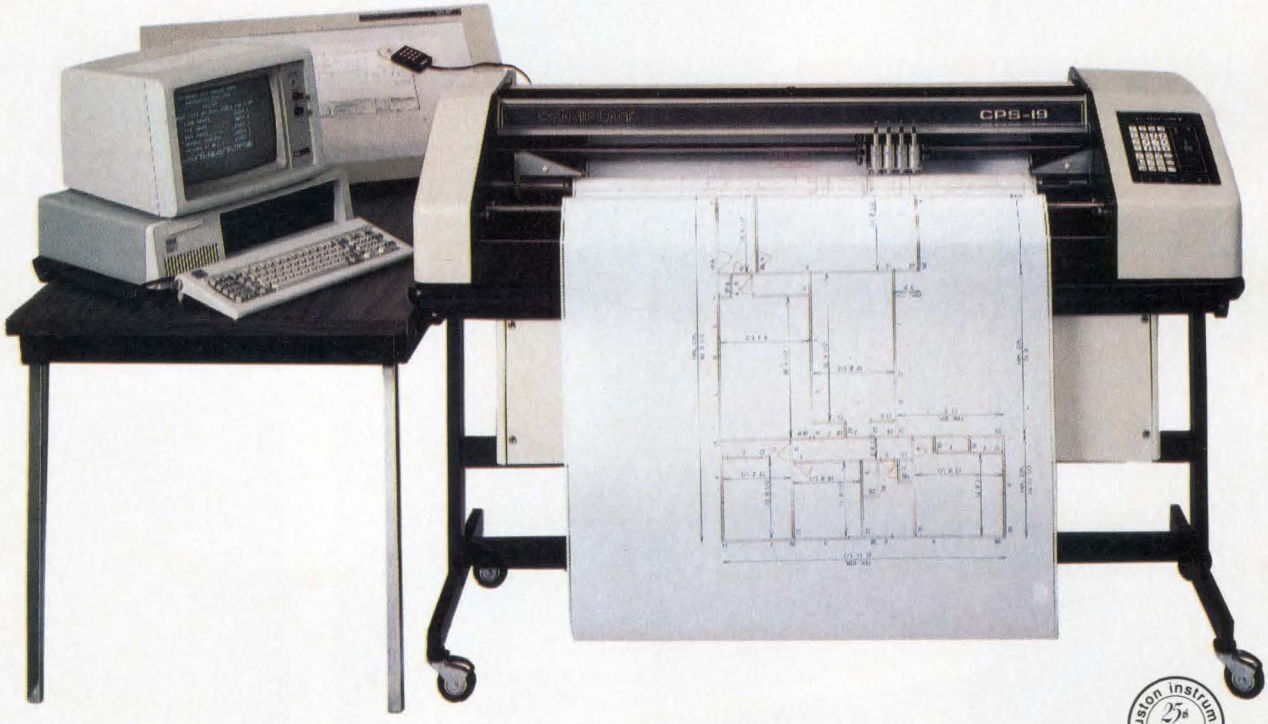

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CIRCLE 3

UP FRONT

IBM announces portable PC and networking capability

Simultaneous with the announcement of a portable version of its personal computer, IBM said that it will now sell a group of products that allows up to 64 IBM PC versions to be connected in a cluster. The IBM Personal Computer Cluster Program will support connection of PCs, PC XTs, Portable PCs, and PCjrs, with performance varying according to the combination and number of systems as well as applications. Each system will require a separate license. Workstations in the cluster will share information and storage space on a fixed disk drive at one machine in the cluster. The company will supply all necessary interconnection adapters, attachments, cables, and connectors. Each 30-lb Portable PC features from 256 to 512 Kbytes of RAM, a 9-in. amber monitor displaying both text and graphics, and a 360-Kbyte diskette drive. A second drive can be added. Like the PC, the Portable PC uses a 16-bit 8088 microprocessor and can use most of the software already available for the PC.

Three 1-Mbit RAMs secure Japanese center stage at ISSCC

The Japanese stole the limelight at the International Solid State Circuits Conference with the debut of three 1-Mbit RAMs. Besides the anticipated chip from Hitachi (*Computer Design,* Jan 1984, p 61), NTT Atsugi Electrical Communication Laboratory appeared with a submicrometer 1024-K x 1 dynamic RAM sporting a built-in, 4-bit-at-a-time error checking and correction circuit. By selecting one of the four corrected data from the ECC, the chip achieves a 4-bit static access mode of 20 ns. This 6.4- x 8.2-mm package is made using a molybdenum-polysilicon gate, n-well CMOS process with 0.8-μm minimum pattern width. Access time is 140 ns; cycle time is 350 ns with 250-mW active power dissipation (5 mW standby). Also, NEC Corp described a nonmultiplexed 128-K x 8 DRAM made using 1-μm NMOS, double-aluminum/double-polysilicon technology. This 30-pin, 9.4- x 8.07-mm package boasts a 120-ns access time and 290-mW active power dissipation at a 300-ns cycle time. Standby power is 15 mW.

A symphony of words and numbers

Hardware's natural tendency to integrate more and more functions onchip is now used by the software industry. Among the latest integrated software packages to appear is one from the Lotus Development Corp (Cambridge, Mass). Symphony is a single-disk software package that integrates five commonly used functions on the personal computer. In addition to the three functions that have been available on the company's 1-2-3 product for the last year—spreadsheet, graphics, and information management—Lotus has added word processing and communication capabilities. The company expects to penetrate the international market with Symphony and has developed the Lotus International Character Set (LICS), which will allow translation of menus, prompts, and manuals.

QIC-36 interface almost a standard

The Working Group for Quarter-Inch Drive Compatibility (QIC) has approved a proposed basic level interface standard for quarter-inch streaming tape drives. This QIC-36 proposal complements the QIC-02 intelligent interface in that it provides a basic drive-level standard for integrators who prefer not to use some of the intelligent features of QIC-02. Both interfaces can be used with the QIC-24 recording format, which addresses the problem of interchangeability between recorded cartridges. The Working Group has submitted its proposal to the ANSI X3T9 committee for adoption as a formal standard.

UP FRONT

DEC previews possible VAX equivalent chip sets

According to technical papers presented at the International Solid State Circuits Conference, Digital Equipment Corp (Hudson, Mass) may be coming closer to the long awaited VAX on a chip. These VLSI chips could conceivably be used to build machines with performance approximating that of the 32-bit wordlength VAX 11/780 supermini. One chip described was a 32-bit microprocessor that executes the instruction set and demand-paged virtual memory of the VAX. Another chip described by DEC is an NMOS interface chip for a new 32-bit synchronous backplane bus. In addition, a VLSI implementation of the VAX was presented that compresses full functionality and comparable performance into four chips—equivalent to 1,220,550 transistors. The four chips are an instruction fetch and execution chip, a memory/peripheral subsystem chip, a floating point accelerator chip, and a high density patchable control store chip.

Database computer handles terabytes

Limitations encountered with relational database management implementations are overcome by integration of hardware and software specifically directed toward the relational task. According to Teradata Corp (Los Angeles, Calif), the solution lies in harnessing multiple microprocessors in parallel using an intelligent tree-structured network. The resulting DBC/1012 computer handles data bases ranging from megabytes to terabytes. Attaching to a host mainframe, the system processes data asynchronously to realize the aggregate power of all processors. It can also achieve a 2.5-instruction/s rate.

Ada to run on supermini

The Ada programming language will be a standard offering on the Harris line of superminicomputers in the third quarter of 1984. The high level military and general purpose language has been licensed from Telesoft (San Diego, Calif), the developer of the only Department of Defense certified Ada compiler. Harris engineers will provide the code generator. Systems that will port Ada include the Harris 600, 700, 800, and 1000. Ada has been commissioned as the next generation software language by DoD to ensure compatibility and standardization of military projects. Now, users will be able to develop software on large multi-user superminis and retarget the software to other processors.

Circuit-switched networks function like telephones

Circuit-switched data networks offered by Western Electric (New York, NY) and Doelz Networks (Irvine, Calif) promise to make end-to-end communications as simple as dialing a telephone. With the specification of the destination address, both Datakit/VCS (from Western Electric) and Espirit establish virtual circuits prior to the actual transmission. This is similar to dialing a telephone number before actually talking. The approach has a lower overhead and higher potential throughput when compared to packet-switched networks such as X.25. Packet sizes are smaller during transmission since the destination address is already specified.

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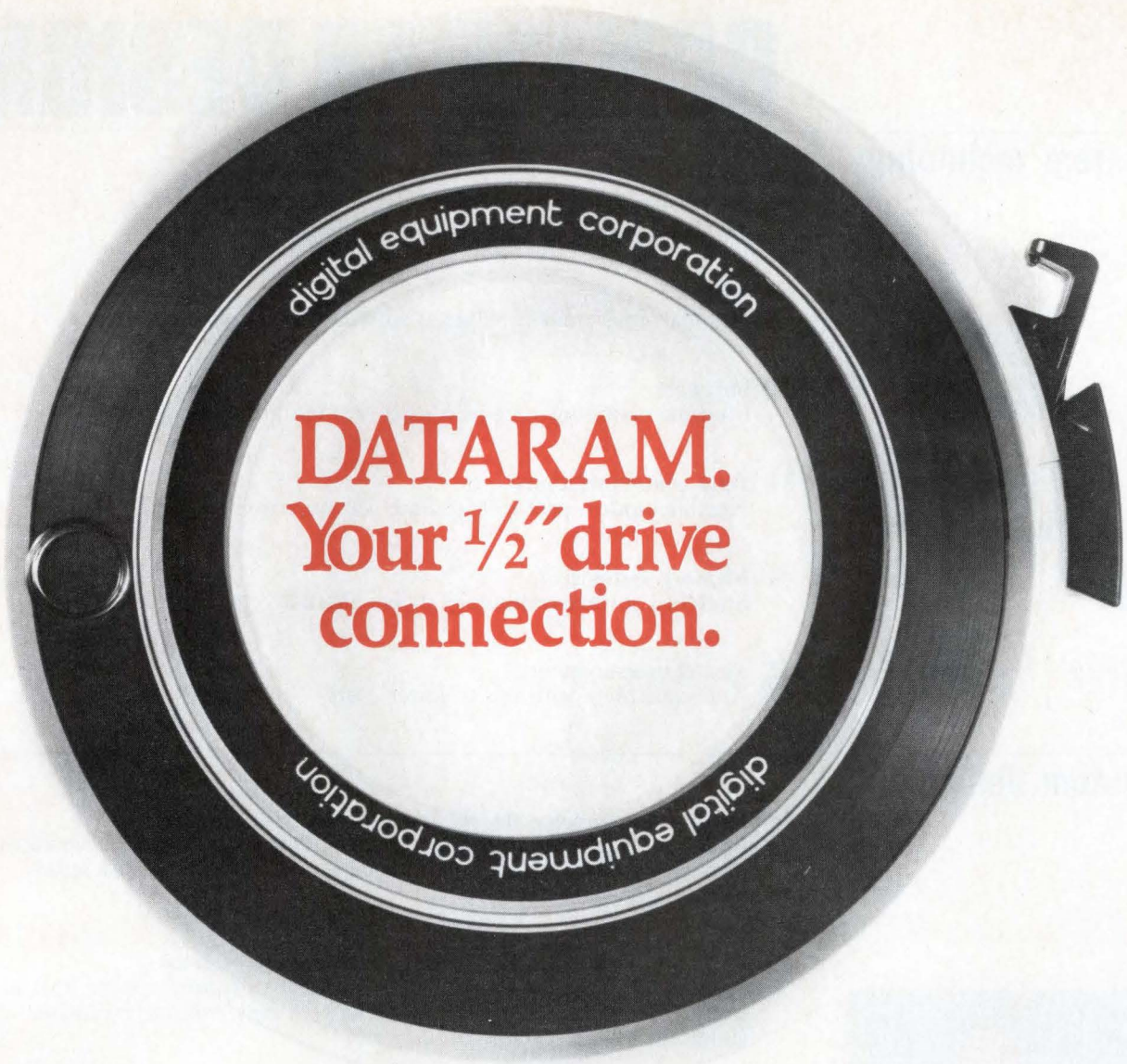

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CIRCLE 4

COMPUTER DESIGN®

System technology

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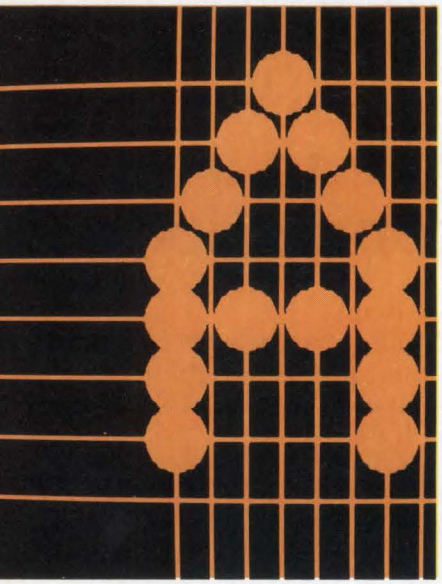
System design



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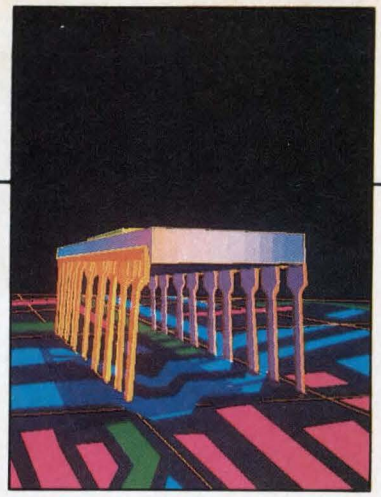
Special report on advanced digital ICs



This month's cover was created and designed by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.

System components

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CIRCLE 7

THE NEW INDUSTRIAL REVOLUTION

At last, America's smokestack industries seem ready to harness computer technology in a big way and thus bring their operating efficiencies up to levels mandated by increasingly tough overseas competition. All the prerequisites for the long-heralded "second industrial revolution" are falling into place. Barring economic catastrophes, the next several years should show sustained high levels of capital spending—with the computer industry grabbing a lion's share.

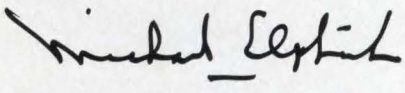
For many years now, engineers in this country have been frustrated onlookers while the Japanese and others took U.S.-developed technology and used it to gain dominance in our traditional markets. Though the electronics industry itself made giant strides in automation, it was unable to convince heavy industry to follow its example. Such technologies as robotics, CAD/CAM, and computer-based flexible manufacturing had the least impact on those industries where they offered the greatest benefits.

There have been several reasons for the delayed arrival of the new industrial revolution in this country. Unlike Japan, U.S. industry has been largely controlled at the top by lawyers, accountants, and salespeople—rather than by engineers. Also, investors have emphasized short-run profitability and return on investment to the detriment of long-term growth. Furthermore, blue-collar labor unions often opposed automation to protect jobs—or they would accept productivity tools only if all the cost benefits were used to inflate wages. Even those companies sold on automation found themselves unable to make the necessary investments because of poor cash flow and high interest rates.

During the last few years, however, most of the investment barriers have been removed. Lower interest rates and improved tax credits now encourage investment. Both labor and management have learned that if they don't cooperate to stay in business, everybody loses. Investors, too, have grown more sophisticated after seeing major corporations with near-sighted investment policies go out of business or slash dividend payments.

Perhaps most important to engineers, however, is a new emphasis on the operations side of industry in the boardrooms of corporate America. Once again, after many years of virtual exclusion, engineers are in the driver's seat in Detroit. Hence, for example, we find that General Motors has a vice chairman who specializes in advanced technology while the president concentrates on current production. Similarly, the president of Ford and the chairman of Chrysler are both engineers by training. Other engineers in control of giant industrial corporations include the chairmen of General Electric and Westinghouse Electric.

So it would seem that the system indeed works the way it is supposed to. Though the process has been slow and painful, the people who have the technical knowledge to rescue American heavy industry from years of neglect finally have the power to make major capital investments. And what's good for General Motors is not only good for America, but for the computer industry as well.



Michael Elphick
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Control CPU speed with Zilog's

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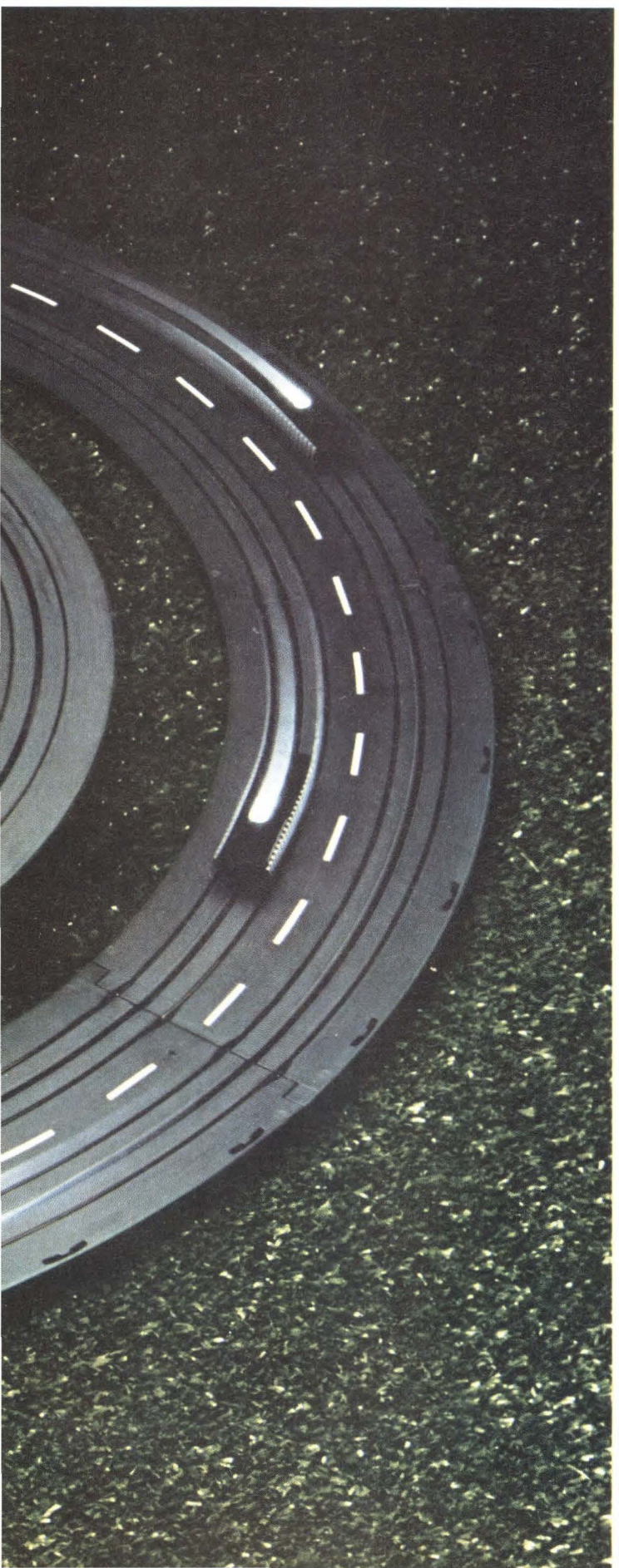

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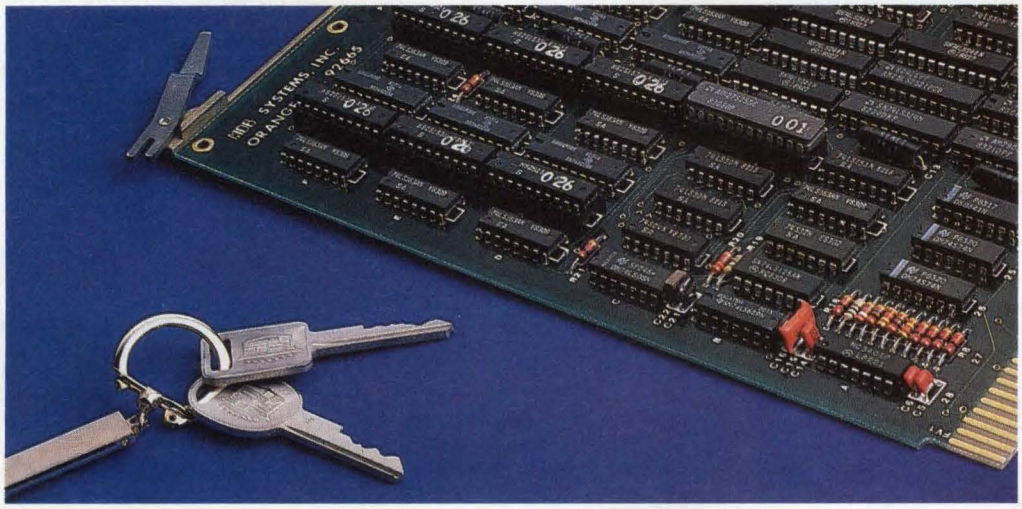

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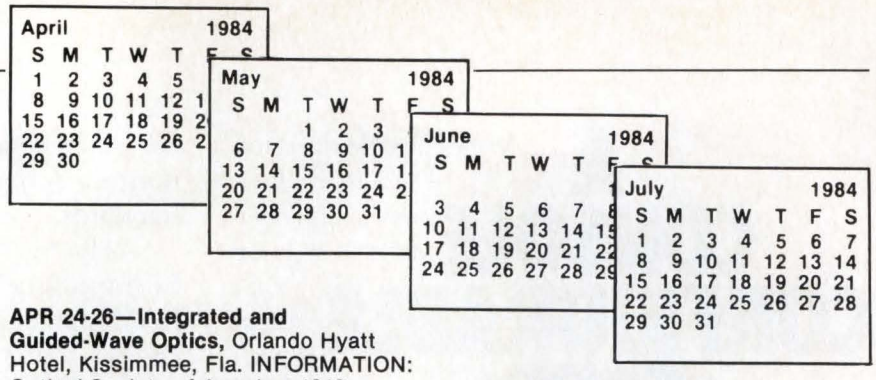

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APR 3-6—Dexpo East, Bayside Expo Ctr, Boston, Mass. INFORMATION: Expoconsul Internat'l, Inc, 55 Princeton-Hightstown Rd, Princeton Junction, NJ 08550. Tel: 609/799-1661

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APR 5-7—Comdex/Winter, Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

APR 10-12—Infocom, Hotel Meridien, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 18-20—Optical Data Storage, Monterey Convention Ctr, Monterey, Calif. INFORMATION: Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. Tel: 202/223-8130

APR 18-20—Simulators Conf, Omni Internat'l Hotel, Norfolk, Va. INFORMATION: Charles Pratt, Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 619/459-3888

APR 19—California Computer Show, Hyatt Hotel, Palo Alto, Calif. INFORMATION: Norm De Nardi Enterprises, 289 S San Antonio Rd, Suite 204, Los Altos, CA 94022. Tel: 415/941-8440

APR 24-27—Compdec (Internat'l Conf on Data Engineering), Bonaventure Hotel, Los Angeles, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last-minute changes.

APR 24-26—Integrated and Guided-Wave Optics, Orlando Hyatt Hotel, Kissimmee, Fla. INFORMATION: Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. Tel: 202/223-8130

APR 25-27—Friendly Systems: 1984 or 2001? Sheraton-Atlanta, Atlanta, Ga. INFORMATION: Donald Chand, Dept of Information Systems, Georgia State Univ, Atlanta, GA 30303. Tel: 404/658-3886

APR 30-MAY 2—Workshop on Computer Vision, Hilton Hotel, Annapolis, Md. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAY 8-10—CAM-I Internat'l Computer Integrated Manufacturing Seminar, Montreux, Switzerland. INFORMATION: Rhonda Gerganess, CAM-I, Inc, 611 Ryan Plaza Dr, Suite 1107, Arlington, TX 76011. Tel: 817/860-1654

MAY 13-17—Computer Graphics, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: National Computer Graphics Assoc, 8401 Arlington Blvd, Fairfax, VA 22031. Tel: 703/698-9600

MAY 14-17—Internat'l Conf on Communications, Congresscentrum Rai, Amsterdam, The Netherlands. INFORMATION: K. Teer, Philips Research Lab, 5600 MD Eindhoven, The Netherlands.

MAY 14-17—Internat'l Conf on Distributed Computing, Hotel Meridien, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAY 15-17—Electro, Bayside Exposition Ctr and Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 15-17—Mini/Micro-Northeast, Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 22-25—Comdex/Spring, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

JUNE 4-7—Robots 8 Conf and Expo, Cobo Hall, Detroit, Mich. INFORMATION: Patricia Van Doren, Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-1500

JUNE 4-8—SID (Society for Information Display Internat'l Symposium), San Francisco Hilton, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

JUNE 5-7—Internat'l Symposium on Computer Architecture, Rackham Building, Ann Arbor, Mich. INFORMATION: Keki Irani, ECE Dept, Univ of Michigan, Ann Arbor, MI 48109. Tel: 313/764-8517

JUNE 5-7—Symposium on Mass Storage Systems, Marriott Mark Resort, Vail, Colo. INFORMATION: Bernard O'Lear, NCAR, PO Box 3000, Boulder, CO 80307. Tel: 303/494-5151

JUNE 6-8—Communications Architectures and Protocols, Montreal, Canada. INFORMATION: Rebecca Hutchings, Honeywell/FSD, 7900 Westpark Dr, McLean, VA 22102. Tel: 703/827-3982

JUNE 19-22—Internat'l Symposium on Fault Tolerant Computing, Hyatt Orlando, Orlando, Fla. INFORMATION: Richard Sedmak, Sperry Univac, PO Box 500, MS C1SW12, Blue Bell, PA 19404. Tel: 215/542-3638

JUNE 24-27—Design Automation Conf, Albuquerque Convention Ctr, Albuquerque, NM. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 9-12—National Computer Conf, Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 23-27—Siggraph Conf on Computer Graphics and Interactive Techniques, Minneapolis, Minn. INFORMATION: Lynn Valastyan, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

JULY 30-AUG 2—Internat'l Pattern Recognition Conf, Montreal, Canada. INFORMATION: ICPR Secretariat, 3450 University St, Montreal, Quebec, Canada H3A 2A7. Tel: 514/392-6744

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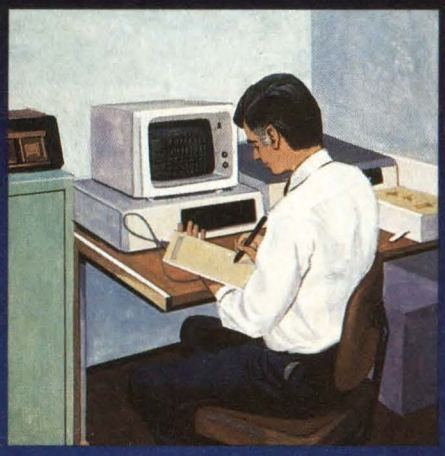

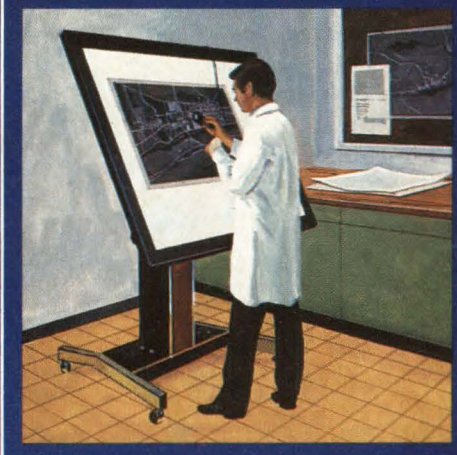

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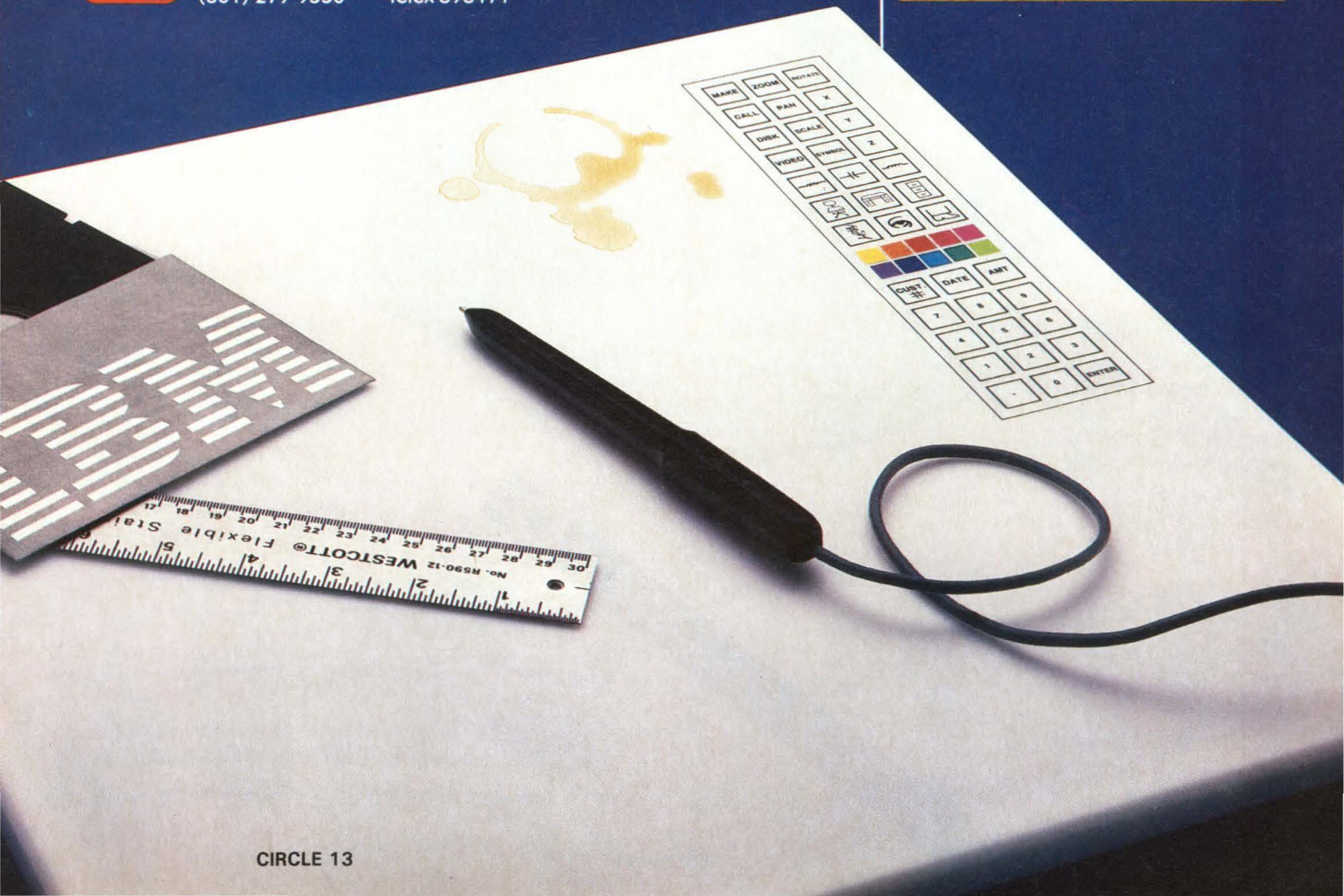
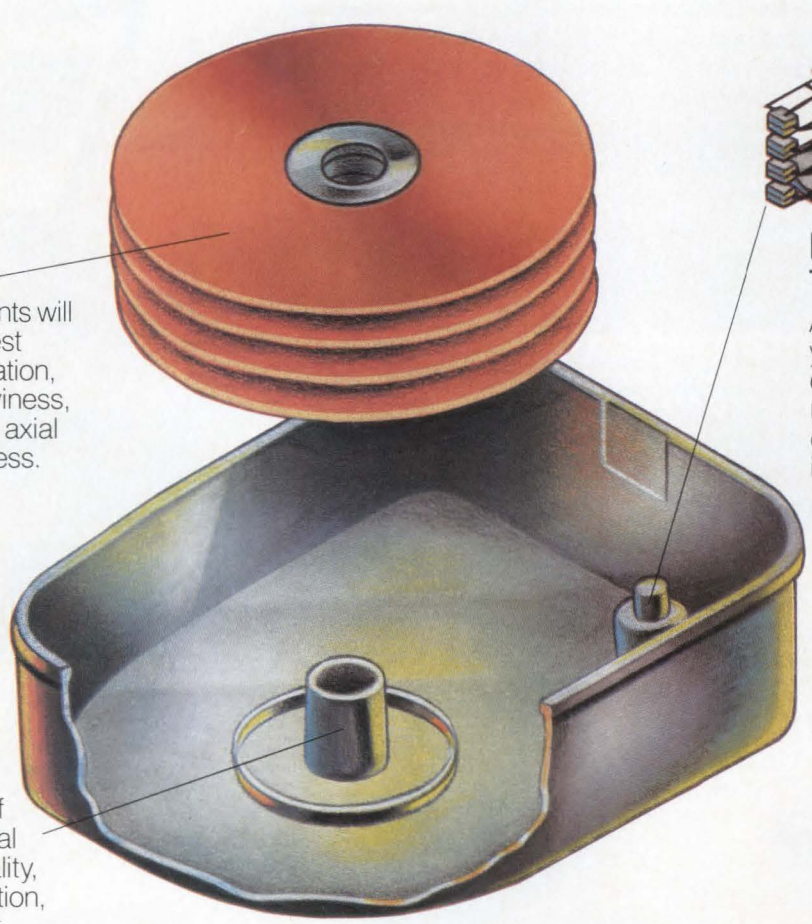
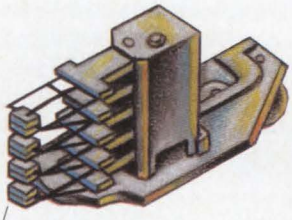


CIRCLE 13

A CRASH COURSE IN DISK AND DRIVE TESTING:





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CIRCLE 12

Voice I/O adds new dimension to computer interface

Voice technology has finally been commercialized as an I/O option for the personal computer. Recently, two leading computer manufacturers have introduced sophisticated voice synthesis and recognition products that could set a trend in making voice I/O an integral interface medium. While special voice I/O applications have existed for some time, the latest offerings by Digital Equipment Corp (Maynard, Mass) and Texas Instruments (Austin, Tex), as optional peripherals to their respective personal computers, have elevated speech to the status of a leading interface technique. DEC introduced DECtalk, a speech synthesizer that can speak an unlimited vocabulary from a computer's ASCII code in various voices, while TI has provided Speech Command, a speech recognizer option for its professional computer that recognizes an individual's limited vocabulary.

Although both developments are not ready to render commonly used interface methods such as keyboards or mouses obsolete, they are adding another dimension through which users can communicate with computers. At the same time, voice I/O frees the operator from constantly using the screen for both monitoring operational functions and displaying data.

Both products use TI's TMS320 digital processing chip as the core for speech analysis. DECtalk is a standalone computer system that converts unrestricted ASCII text to understandable speech. It consists of a 68000 microprocessor, a TMS320 digital processing chip, a 64-Kbit RAM, a 256-Kbit ROM, and a few other interface chips.

Text is converted into speech in a three-part process. ASCII text is first converted to a phonemic code where each symbol in the alphabet has only one pronunciation. Then, the phonemic text is converted into 18-word synthesizer control messages. Each message sets the center frequency and bandwidth of several filters, as well as the amplitude and frequency of the voice source driving the filters. A message is generated every 6.4 ms. In stage three the digital signal processor uses the filter parameters to synthesize a speech waveform at a 10,000-sample/s output rate.

Speech Command, an option for TI's Professional Computer, adds voice I/O to the system's input and output repertoire. Recognizing connected streams of words, the unit has a 99-percent recognition rate.

To convert the text to phonemes, a clause parsing module breaks the input stream into separate words and locates some clause boundaries. A number parsing module also expands the digit stream into English words from its understanding of common number formats.

A sophisticated heuristics function breaks compound words and those words with embedded nonletters into their component parts, thereby yielding words in their final pronounceable form. Strings of ASCII text that do not form English words are spelled out letter by letter.

The heuristics function calls on two dictionaries for a word search—the user dictionary, and the built-in dictionary. Words that are found in either dictionary are directly transmitted to a phrase structure module. Meanwhile, a letter-to-sound module uses a large library of English pronunciation rules to assign phonemic form and lexical stress patterns to words not found in the dictionary. Finally, the phrase structure module processes all phonemic output from the dictionary and the letter-to-phoneme subsystems. Clauses are initially analyzed for syntax recognizing end of phrase and end of clause punctuation. Recognized clauses are passed to the phoneme-to-voice subsystem. Here, the phonemes are recoded and each phonemic segment is assigned a proper time duration as well as a fundamental frequency.

Every 6.4 ms, the phoneme-to-voice subsystem also generates 18 synthesizer parameters that are sent to the digital signal processor. The parameters have been carefully chosen to follow the almost exact computer simulation model of the human vocal tract that gives DECtalk its high intelligibility. The synthesizer

(continued on page 20)

Voice I/O interfacing
(continued from page 19)

Sensitive to the touch

While voice is the most natural interface between man and machine, touch-sensitive displays provide an intermediate method that falls between the currently predominant keyboard entry technology and voice I/O. With this method, it is now possible to access several personal computers by using touch-sensitive screens to input commands and answer queries much more directly than if one used a keyboard. What usually requires a half-dozen entries on a keyboard can now be done with one touch.

On their new HP 150 personal computer, Hewlett-Packard (Palo Alto, Calif) engineers have installed a screen that is touch-sensitive to every row and every other column (see Photo). The HP 150's 9-in. screen has a capacity of 24 lines x 80 columns. LEDs placed on the periphery of the green phosphor screen pick up the breaks in the infrared signal cross sections as the finger is removed from the screen, and transmit electrical signals to generate the proper software commands.

Principally aimed at the business user, the HP 150 offers all popular word processor, graphics, and spreadsheet programs. However, unlike other computers, it now allows the user to make entries and changes principally via the screen, with the keyboard available for complementary tasks. As an example, to make a chart, the only time that users need to use the keyboard is to type in number, labels, and titles. Thus, with the graphics software package, users can practically "draw" all pie, bar, line, and text charts with their fingers. Transferring files from other applications requires no use of the keyboard at all.

The interface has become so popular that the company has set up a software submission program to recruit and evaluate third-party software vendors' products. Hewlett-Packard expects to have close to 500 software products for the HP 150 by midyear. More than 200 vendors have offered products that are specifically written for the touch-sensitive environment.

Another company that is making a go at touch-sensitive technology is Touch Technology, Inc (Annapolis, Md). A manufacturer of touch-sensitive monitors, the company has recently signed an agreement with Technical Analysis Corp (Atlanta, Ga) to produce a device that allows touch monitors oper-

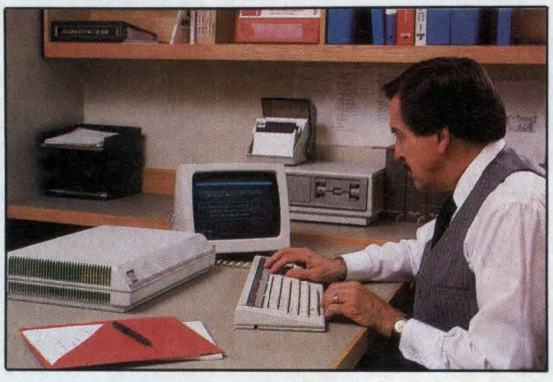
parameters set filter frequency, bandwidth, and gain for five formant frequencies. The first three formants are set every 6.4 ms, while formants four and five are set by the speaker definition. The parameters also set the frequency and amplitude of voicing, as well as the amplitude of fricatives and aspiration. Filters are used to simulate the nasal resonator. Both the heuristics and the vocal tract model were developed by a leading linguistics researcher who consulted DEC—Dennis H. Klatt of MIT.

DECtalk has already been applied on a custom basis by a number of hospitals, universities, and manufacturers. Children's Hospital in Boston is using DECtalk as a communication aid for the speech impaired. A touch-screen display allows children who may not yet be able to speak or type by conventional means to select ideas from layered menus of representative pictures and "speak" those ideas through DECtalk.

In another application at Clemson University in South Carolina, students are able to call in at any of the campus telephone booths and communicate with DECtalk by using the push buttons as prompts for certain queries. For example, a student can order theater tickets for a campus performance up to an hour before curtain time, using this realtime automated ticket agent.

An application that is closer to the lay audience is MCI Mail, a product of MCI Communications Corp (Washington, DC). It utilizes DECtalk to allow customers to call up and have their electronic messages read to them by telephone. Moreover, RVA Technologies, Inc (Newburyport, Mass) has applied DECtalk as voice support for computer-based instruction, thereby allowing users to "walk through" computer program training. DECtalk talks in various male, female, and child's voices at speaking rates of 120 to 350 words/min. Connection to most computers is via serial RS-232 cable interface. The surprisingly compact unit is available immediately for $4000, and can be heard before acquiring by calling 617/493-TALK. According to DEC publicity, hearing is believing.

Meanwhile, TI's Speech Command is both a speech synthesizer and a speech recognizer. TI engineers say they have solved many of the fundamental problems that have existed both in speech synthesis and speech recognition. As in the DEC product, the key to TI's success is in being able to conserve on the amount of memory required for speech recognition by using the TMS320 digital signal processor chip. The linear



A standalone computer system, DECtalk converts ASCII text into spoken words, adding another interface dimension to the computer. Speaking in a male, female, or child's voice, the unit communicates at a 120- to 350-word/min rate.

ating with IBM PCs to communicate with an IBM mainframe. Using a coaxial cable to an IBM 3274/76 communication controller and a modified communication board inside the PC, IBM PC users can retrieve data from the IBM mainframe using the touch-sensitive screen. In addition, the company is going a bit further by offering the Touch Mouse, which can be used with various templates. These templates can incorporate various application software from different vendors. Touch Mouse is not really a mouse, but a peripheral "box" that sits next to a computer keyboard. It has a clear, resistive analog membrane cover measuring 5 x 6 x 1 in., below which rests a touch pad that is activated by the touch of a finger or a dull object.

Touch Mouse is functionally similar to other computer "mice" that come as optional peripherals to personal computers, such as Apple's Lisa. It is compatible with software written by Microsoft, Inc (Bellevue, Wash). Unlike other mouse devices, however, Touch Mouse uses a smaller planar area to find its target, remembers past cursor positions, and even allows entry of numeric data into the computer. Currently, three templates are available from Touch Technology: a numeric keypad, a musical organ for writing and editing music, and a graphics package. Touch Mouse can interface with the IBM PC, IBM XT, and Compaq computers and costs $249.

predictive coding algorithm used with the TMS320 models the human voice by employing a method that requires only 2400 bits/s as compared to other systems that consume memory much more quickly. TI engineers claim that whereas perhaps only a few seconds of speech could be stored on a microcomputer using previous technology, the TMS320 uses high density information compression that makes speech storage fit within microcomputer memory constraints.

Thus, Speech Command can store 16 min of speech on a floppy diskette and up to 4 hours on a 5-Mbyte or 8 hours on a 10-Mbyte Winchester disk. Real storage of input speech is also actually higher, since Speech Command and DECtalk automatically reduce unnecessary pauses, and empty space in phrases and sentences. In compressing the information to fit microcomputer requirements, the voice quality of Speech Command is comparable to others that operate at higher bit/s rates.

Speech Command uses a speaker-dependent method of voice recognition. However, since it recognizes connected streams of words (connected word recognition), users can speak in normal sentences instead of pausing after each word. Even with this flexibility, the recognition rate is high. TI laboratory tests consistently resulted in greater than 99-percent recognition after the user's vocabulary is enrolled.

All of the voice processing is performed using TI's TMS320 digital signal processor to perform realtime voice analysis and synthesis. The telephone interface is performed with another TI processor chip, the TMS7000. Telephone management capabilities allow the system to record incoming phone messages, dial numbers, deliver outgoing phone messages, and provide playback of recorded messages that can be actuated from a remote telephone.

The TI's Speech Command concurrently accepts and provides voice inputs and provides voice output via a speaker, headset, or telephone. The system can be integrated with any of TI's professional computer MS-DOS software programs.

The system includes two piggyback circuit boards, a headset, a user's manual and two software diskettes, an installation/diagnostics guide, a diagnostics diskette, and a telephone cable. The unit is now available at a list price of $2600. A Speech Command development kit is also available and includes the programming tools necessary for third-party developers, manufacturers, and other resellers to design unique applications using speech technology. The kit has routines that provide an application program with convenient access to the Speech Command system's capabilities. Also included in the kit are a programmer's guide, the processing algorithms in object-code form, device service routines for the Speech Command hardware, and a library of runtime routines for the high level programming languages—MS-Basic, MS-Pascal, and Lattice-C.

Applications written in any of these languages or in 8088 assembly language can link the runtime routines with the program in order to use the capabilities of the Speech Command system. The development kit, which includes a software license and the right to sublicense, is priced at $8000 plus a product royalties discount.

—Nicolas Mokhoff, Senior Editor

SYSTEM TECHNOLOGY

(continued on page 28)

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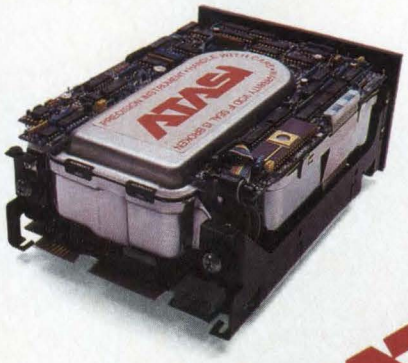

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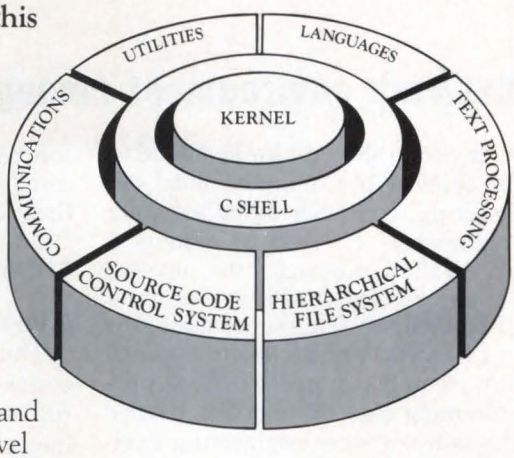

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GENIX Summary

National Semiconductor
MICROCOMPUTER SYSTEMS DIVISION

CIRCLE 156

Network environment manages software engineering projects

A new term should now be added to the concept of computer aided engineering: computer aided software engineering. The job of managing large software projects that involve periodic rereleases of a product (and often many different configurations to fit a variety of hardware systems) now requires more than just programming aids. Apollo Computer's Domain software engineering environment is specifically tailored to the needs of development, management, and maintenance of large software engineering projects.

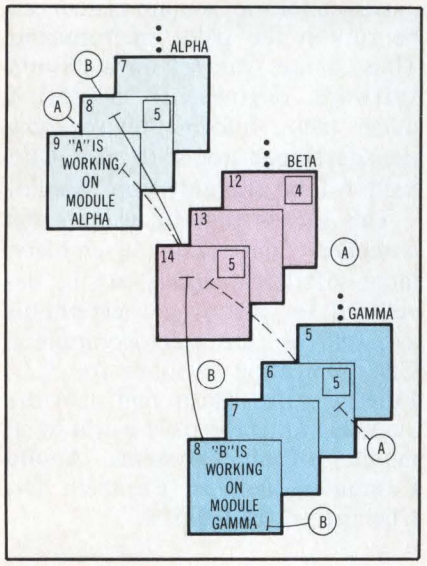
The Domain software engineering environment (DSEE) works with the window-oriented user interface of the Apollo Domain system, which links individual computing stations in a very large virtual address space. Essentially, DSEE can oversee and control the evolution of any textual elements, but in addition to text (for source code and documentation), it can also manage binary code. To do this, DSEE uses primitives derived from the Domain distributed data management system.

Software environment functions

Thus, DSEE is really a means for connecting software tools (eg, editors, compilers, linkers, and debuggers) to the user interface and the data manager. It further extracts and correlates information about user activity and changes it to software elements under development. Among its major functions are history management, configuration management, and task management.

History management is essential in a project where a number of team members are working semi-independently. DSEE keeps only one copy of each module's version and records each instance where a user "checks out" a module. For any change, the history manager records the time and date, the programmer's name, and the name of the workstation. The user is then prompted to enter a comment explaining why a change was made. This makes the act of failing to make a remark into an active decision rather than an omission.

Therefore, DSEE is able to maintain a multiversion "line of descent" for each element. All previous versions are available online until they are removed to archival storage. In this way, it is possible to trace not only the history of each module, but also to reconstruct previous releases of the software product. If, for example, a certain module remains unchanged through several revisions of a software system, DSEE maintains only one copy of it but recognizes it as



With configuration threads, users can define configurations of a software system by specifying selected module versions. Users can thus build customized software releases.

belonging to all subsequent versions until it is modified. At that point, DSEE keeps both the original and modified version, with notations as to the release to which they belong.

Configuration management allows the user to establish "configuration threads" that tie together various versions of different source-code modules. In this way, it is possible to customize, for example, an operating system to a hardware environment that has specific disk and tape drive requirements simply by specifying the modules and versions needed. By doing this, DSEE can minimize compile time by first checking the available binary versions before compiling any source code, and then only recompiling those modules that are not already available in binary form. Thus, any previous version in any configuration can be reconstructed by consulting the history manager and setting up the proper configuration thread.

The task management aspect of DSEE is primarily a tool that allows the project manager to assign tasks to various team members, and to track the progress of their work. This involves creating a list of things to do for each team member. Tasks refer to the module, its creator, and creation date. As a team member finishes a task, it is checked off. Programmers can enter the steps they took to do the job and DSEE will automatically record all element change information, such as modules affected by the change. This data can then be used for documentation, and for initiating new team members to procedures.

Task management also interacts with what can be called advice management. On one level, advice man-

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Managing software projects

(continued from page 29)

agement keeps track of dependency relationships between modules. If a change is made to some module, DSEE notifies all calling modules that a change has been made to a called routine. Task management will then automatically place predefined tasks in the appropriate person's task list so that all modules affected by the change are updated.

Advice management

In a looser sense, advice management also allows project managers and team members to place comments and advice in the project's data base. New team members can consult this advice for guidance for both goals and procedures, and the information can be extracted to assist in the documentation effort.

In fact, the same tight version control that manages the source and object modules in the software development effort can be used to control the documentation. Thus, text files for documentation would receive version and modification numbers corresponding to the versions and configurations of the software system. Ideally, this would ensure that a manual could be put together to not only correspond to the current software release, but to also be specifically tailored to the customized configuration for the target system.

DSEE runs under both operating systems available for the Apollo Domain: Aegis and Aux. Aux is the Apollo version of Unix System III with Berkeley enhancements. Both Aux and Aegis share the same large virtual address space and network-wide sharing of programs and data. Any combination of editors, compilers, and debuggers, etc that are available for the Domain system can be run in the DSEE environment. Thus, a user can set up a custom software engineering operation under DSEE. Information to allow user-developed tools to run with DSEE will be available from Apollo.

This means that by using cross compilers and cross assemblers, large software projects can be developed for mainframe superminis as well as for microcomputers. Communication facilities for X.25, Ethernet, IBM Hasp and 3270 are available to tie the DSEE world to all manner of other systems. **Apollo Computer, Inc,** 15 Elizabeth Dr, Chelmsford, MA 01824.

—Tom Williams,
West Coast Managing Editor

Multiple operating systems coexist on multiprocessor system

Virtual machine concepts implemented on the series 3000 MICRO-mainframe from Syte Information Technology permit several operating systems to coexist on the same central processor. Likewise, the system disguises its multiprocessor architecture so that it appears as a single processor to these operating systems. Finally, both operating systems and the application programs executing under them can access resources at other nodes of a local area network as if the resources (eg, physical devices or files) were physically attached.

Global environment manager

Devised to offer mainframe processing power in a desktop package, the systems are based on multiple tightly coupled microcomputers organized in a mainframe architecture. Each system can perform the floating point calculations necessary to computer aided engineering or can serve as a general purpose office machine.

At the heart of this sleight of hand is the global environment manager (GEM). It takes the place of the basic input/output system, event scheduler, file manager, and user interface portions of the operating system so that virtual environments can be created for each executing operating system. The supervisor portion of GEM runs on each processor module (a maximum of four) to handle the low level functions (eg, print drivers, and record access) required of the operating systems running under it.

This supervisor runs in a separate address space (or mode) from the 16-Mbyte logical address space dedicated to each user execution environment. As many as 255 user-execution environments can exist on each processor node. Moreover, each operating system can use several such environments to handle multiple tasks or multiple users, or a user can perform simultaneous tasks on different environments using a single operating system.

In a sense, the supervisor address space is a global address space because it maps all resources available on the network as though it were physically attached. GEM's object orientation makes this possible. Physical resources represented as uniquely identified objects include disk drives, graphics displays, and input devices. Objects also represent abstract resources such as directories, files, and executing programs.

Any primitive operations that occur within GEM use defined procedures (or methods) that operate on the data structures associated with these objects. These operations are grouped as classes so that they can operate only on a defined set of objects. For example, floating point operations (or methods) cannot operate on objects containing text files or binary object programs. GEM can be easily modified without adversely affecting the rest of the system since changes in methods affect only its associated objects.

Such encapsulation extends beyond low level functions contained within GEM. Operations such as database management are also divided into subsets based on the functions being performed and the types of data

(continued on page 32)

"BUBBLES ARE HELPING NIXDORF BREAK INTO NEW SALES FIGURES."

—Axel Hass
Sales Director of Retail Industry
Nixdorf Computer AG

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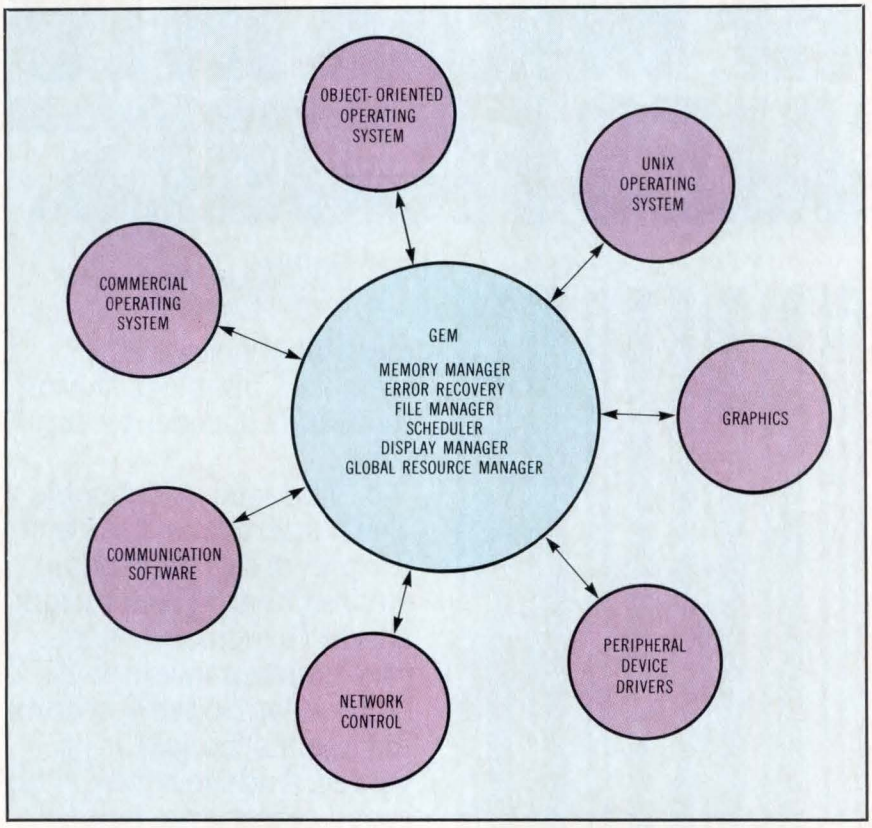
CIRCLE 16

Multiple operating systems
(continued from page 30)



The global environment manager (GEM) implements the machine-dependent portions of any operating system (eg, device drivers and file system) executing on the Syte 3000. New operating systems can be added simply by porting over systems calls and message handlers.

required, both in hardware and software. This allows system functions to be physically distributed across the network because the data and procedures needed to manage the resource stay with that resource.

Messages hold one key to making this approach work. Instead of issuing a system call to operate on a resource, a message is sent to the object that represents the resource. The message includes the name of the function and the name of the target object. The sender only needs to know the object's name, not its class or location on the network.

Directories serve as the other key to making GEM work. They are organized into a network-wide hierarchy so that users can refer to a resource by its unique name without knowing its physical location. Directories also serve as the principal means of access control since they also contain such information as user identification, group (a collection of users), node, and area (a collection of nodes).

Contrasting approach

With this object-oriented approach, the Syte system differs sharply from the time-honored method of implementing concurrently executed operating systems. One approach, favored by Convergent Technologies Inc (Santa Clara, Calif) with its MegaFrame system, calls for multiple operating systems to run their own dedicated processor and memory (see *Computer Design,* July 1983, p 99).

MegaFrame supports Unix on a 68000 microprocessor, while its own CTOS operating system executes in a separate address space on an 80186 processor. The Unix call handler was modified so that messages were routed to CTOS in response to resource requests. In a sense, Unix needed to be taught about interprocessor communications.

On the other hand, the Syte approach executes Unix on the same physical processor as GEM. Unix system calls are issued as if the operating system had full access to a single CPU and associated peripherals. GEM dynamically assigns multiple Syte processing units to execute programs and service requests, independent of the user execution environment (ie, operating system).

The other means of supporting multiple operating systems is to translate the system call of one operating system into the system calls of another. Apollo Computer (Chelmsford, Mass) implements its Aux version of Unix in this manner. Its own operating system, Aegis, takes requests issued from C-shell command interpreters (both the Bourne and Berkeley 4.2 versions) and converts them into the suitable Aegis calls. All compilers, application programs, and utilities exist under Aegis rather than Unix.

The Unix operating systems running under GEM implement the full Bell System V (or soon Berkeley 4.2) specifications with system calls handled in the same manner as if they were issued on a Digital Equipment Corp (Maynard, Mass) VAX-11/780. What GEM replaces is the machine dependent portions of the operating system, such as the device drivers, file manager, and user interface.

Each workstation in the series 3000 is equipped with a NS16000 microprocessor with memory management and floating point capabilities as the main processor, and an 80186 for high speed disk and network processing. Memory can be expanded from 1 to 15 Mbytes, with Ethernet used to access remote data bases through a demand paging technique. The single-unit price for a model 3000 with 1-Mbyte memory and 19-in. 1024 x 800-pixel monochrome display is $21,900. **Syte Information Technology,** 11339 Sorrento Valley Rd, San Diego, CA 92121.

SYSTEM TECHNOLOGY
(continued on page 37)

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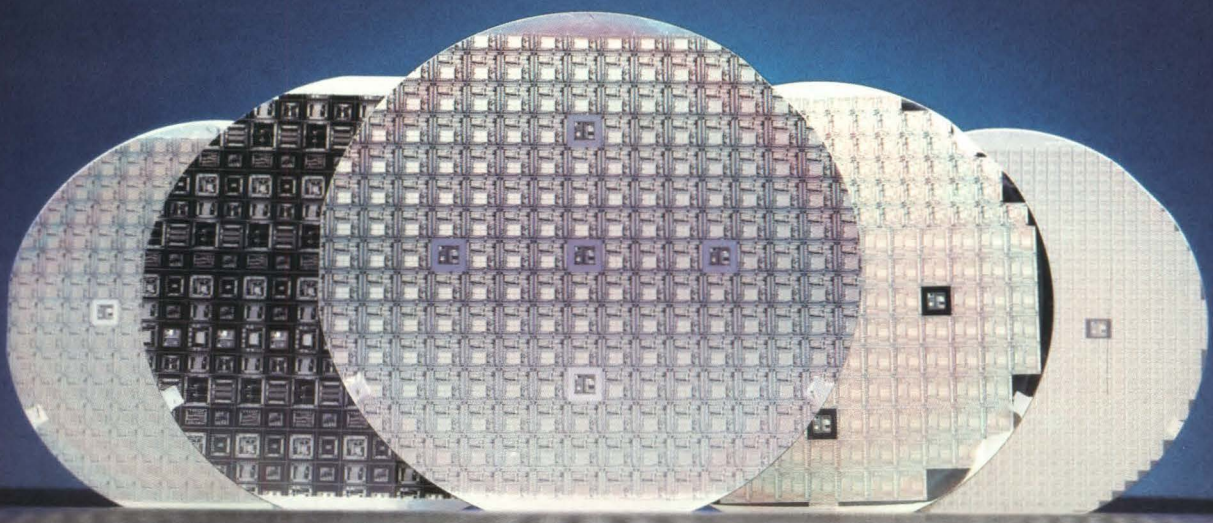

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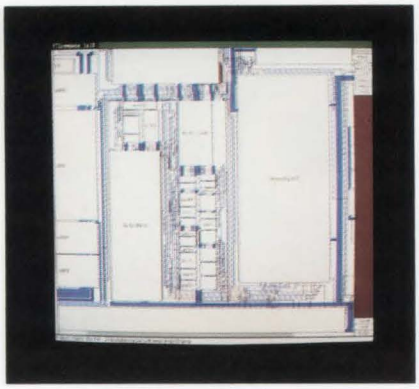
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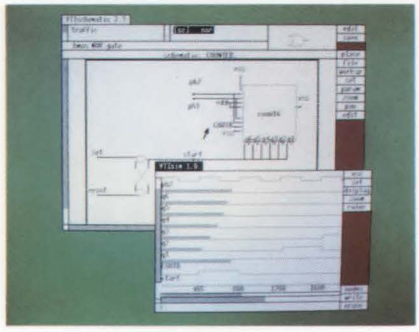
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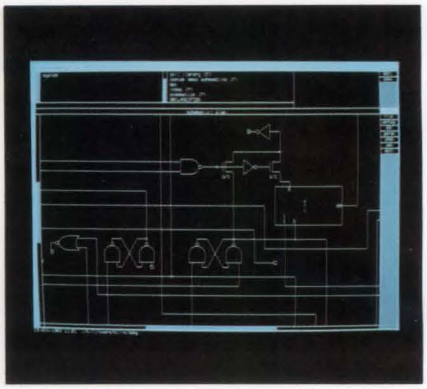
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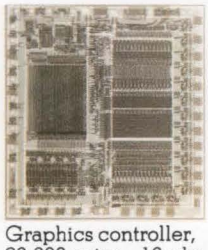
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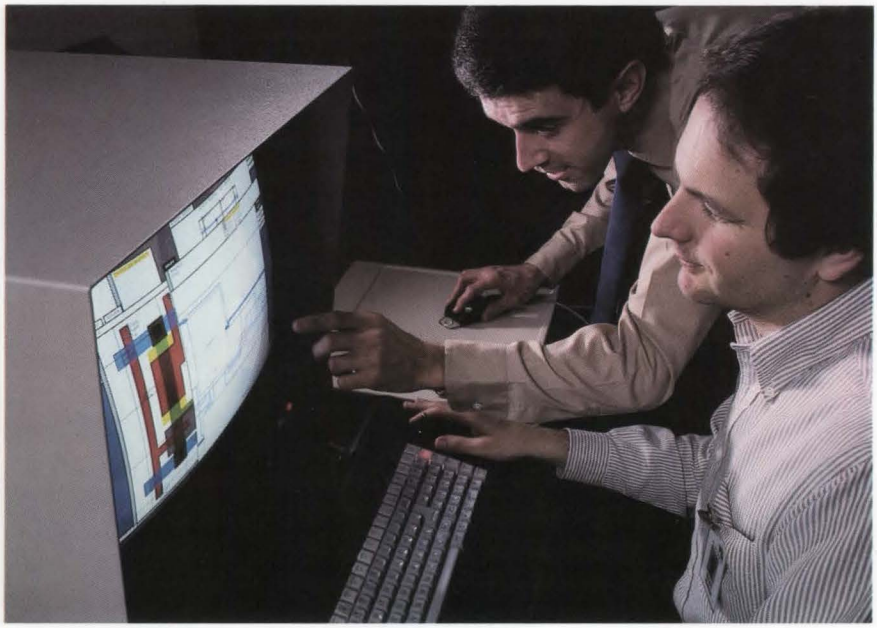

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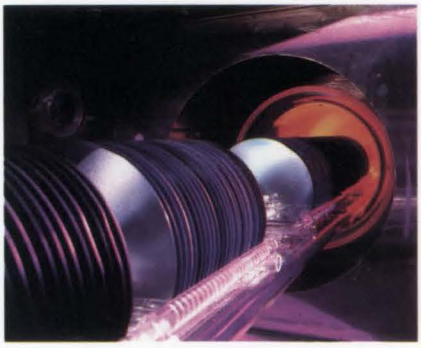

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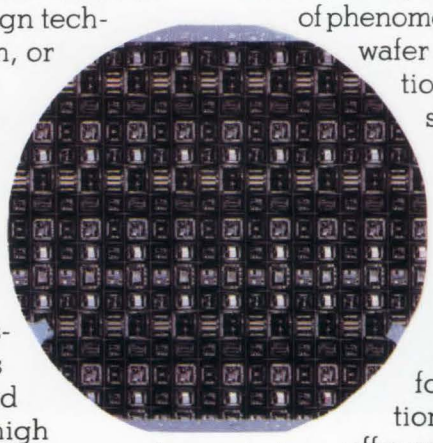

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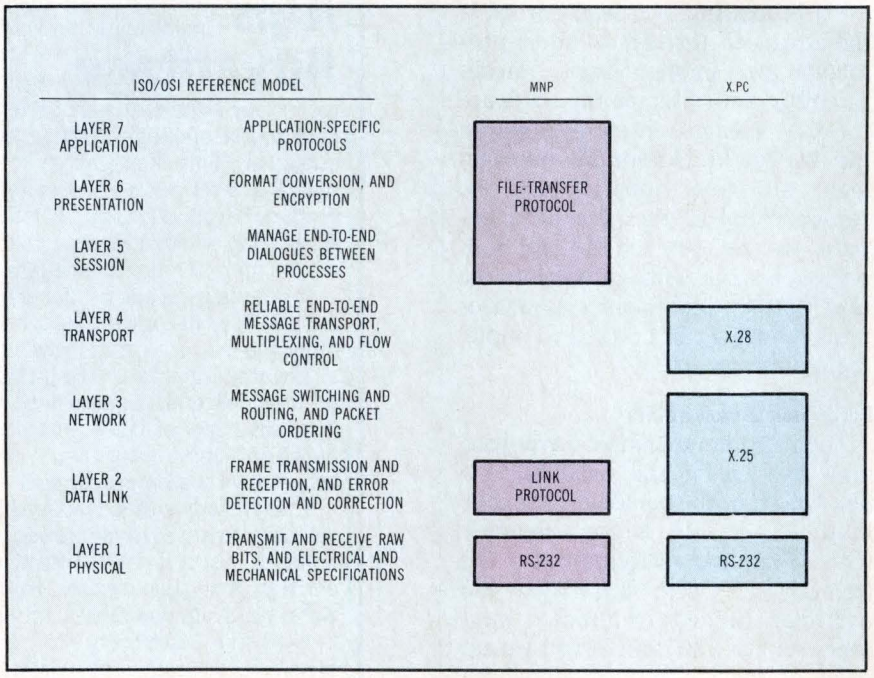
Flexible modem protocols declare war on errors



Tymnet X.PC and Microcom MNP protocols implement network services at different layers of the ISO/OSI model. However, they both use dumb asynchronous modems as the physical link.

Enhanced modem protocols promise error-free communication links between personal computers as well as between personal computers and larger hosts. These schemes provide more flexibility than currently available protocols (eg, XMODEM, offering such capabilities as message framing error detection and retransmission based on 16-bit cyclic redundancy check codes, and sophisticated flow-control procedures. Competing for industry acceptance are two announced specifications: the Microcom (Norwood, Mass) networking protocols, or MNP, and the X.PC specification developed by Tymnet, Inc (San Jose, Calif).

However, a price must be paid for such functionality. Error detection and retransmission adds significant overhead to the actual data being transferred. In addition, both specifications rely on the host CPU within the personal computer for communication processing. In single-tasking operating systems, this forces other related application programs (eg, spreadsheets and word processing) to be suspended until data transmission ceases.

Similarities and differences

The MNP specification supports data transfers as either byte streams or files. Framing techniques mark the beginning and end of each data unit. Likewise, the X.PC specification implements the data packet format called for in the International Consultative Committee for Telephone and Telegraph (CCITT) X.25 specifications for public networks. A file-transfer mechanism is not defined within X.PC, but the protocol does implement the required multiple data streams of the X.25 specification.

As for overall design, the specifications have more similarities than differences. The MNP and X.PC protocols implement network functions in the same general manner, although implementation specifics differ. Asynchronous RS-232 serial links form the physical layer [layer 1 of the International Standards Organization (ISO) Open Systems Interconnection (OSI) model].

The same three-step procedure establishes links in both versions. First, the sender issues a link request to the receiving node. The receiver acknowledges the request by issuing its own link request, and the circuit is finally established when the caller issues a link acknowledgment. The link will not be established if a "not-acknowledge" is received anytime during this procedure.

Once the link is established, the X.PC and MNP specifications call for byte-oriented data transmission of each message. The formats follow the same basic two-part construction using a header and an optional user data portion. The header typically contains packet function type (eg, user data and link establish), message sequence numbers, and a 16-bit cyclic redundancy check (CRC) code.

Subsequent messages also follow the same acknowledge/not-acknowledge scheme used for the initial link setup. The link can be broken if several not-acknowledge messages are received that cause retransmission. This typically occurs after the CRC uncovers any corrupted data.

Here, similarities between the two protocols end. The header used in the X.PC specification is fixed so that the overhead for a 256-byte (maximum) message remains the same as the minimum message size—8 bytes. On the other hand, the MNP specification calls for a header consisting of a variable-sized segment in addition to a fixed-size segment. The fixed portion contains such information as the length of the total header and packet-function type, while the variable portion contains parameter information that affects packet-function execution. Overhead for a 256-byte message approaches 14 bytes, with byte stuffing used to fill out messages.

Gary Pierson, systems architect with Microcom, notes that this is a small penalty to pay in order to ease

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Flexible modem protocols

(continued from page 37)

integration into many personal computers. He points out that the bit optimization found in the X.PC specification makes it more difficult for byte-oriented registers in the microprocessor to handle. For example, the X.PC specification calls for all data terminal addresses to have an odd number of bits.

Other differences center on features found in one specification, but not in the other. Perhaps the most significant is the inclusion of a file-transfer protocol in the MNP specification. The X.PC protocol, on the other hand, relies on the file transfer facilities already implemented as Tymnet value-added services (X.25, SNA/SDLC, SNA/BSC).

The file-transfer protocol is implemented at layers 5 through 7 (session, presentation, and application, respectively) of the ISO/OSI model. At the session level, corresponding computers exchange information including device type, operating system file type, and application identification, as well as source and destination addresses. Once this information has been exchanged, corresponding computers can issue open and close file commands and transfer data between files. A virtual file format is used as the intermediary between the two file systems by appending attributes such as file names, passwords, file types, and record lengths to the actual information.

Meanwhile, Tymnet has chosen X.PC for implementation of the multiplexed data channel feature already found in the X.25 specification. Built into the packet header is logical channel identification that allows users to initiate up to 15 simultaneous data sessions over the same physical link. Although this feature may be impractical for most present personal computers, the emergence of window managers such as VisiON from VisiCorp (San Jose, Calif) and Windows from Microsoft Corp (Bellevue, Wash), as well as multitasking operating systems such as Concurrent CP/M-86 from Digital Research provide possibilities for future use.

It may be impractical, however, to ask personal computers to bear the extra processing overhead burden if the advanced features of these protocols are implemented. Packet assembly and disassembly software for X.PC executes in the CPU within the IBM PC, while both link management and file transfers are the responsibility of the personal computer in the MNP scheme. In both protocols, processing moves into the host CPU so that cheaper asynchronous modems can be used to implement either protocol.

Performance constraints

Such communication overhead may overwhelm the available I/O bandwidth of the personal computer itself. Roger Tsur, project engineer with Computer Development, Inc (Beaverton, Ore), notes that the overhead needed to process messages sent at 1200 bits/s will eat up most of the 25-kbyte/s bandwidth found on many personal computers. Overhead includes taking the message off the serial port, calculating CRC checks, and transferring data to disk. Such communication processing requires that application programs be suspended until the message is stored on disk.

Additional processing needed for file-format conversion or the demultiplexing of data channels may require a frontend communication processor like that found on some public data networks such as Tymnet, according to Tsur. Intelligent modems, such as the ETC100 from Computer Development, Inc (see *Computer Design,* Apr 5, 1983, p 42) or the Era 2 from Microcom, with dedicated microprocessors and memory, represent such frontend processors. Handling the necessary communication overhead in parallel with the application processing done on the personal computer may be the only way that the enhanced capabilities of these protocols can be optimized.

—Joseph Aseo, Field Editor

SYSTEM TECHNOLOGY

(continued on page 44)

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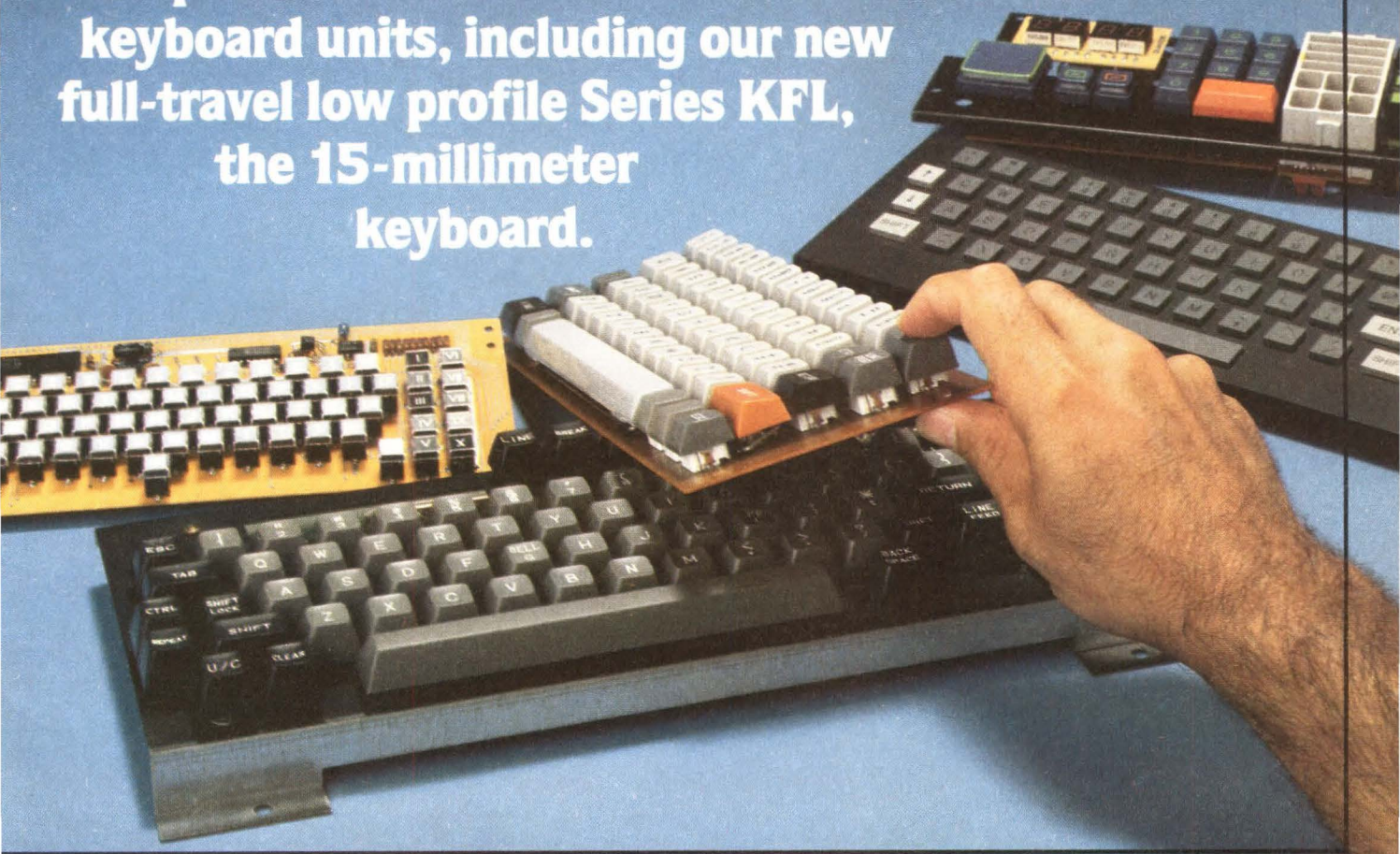

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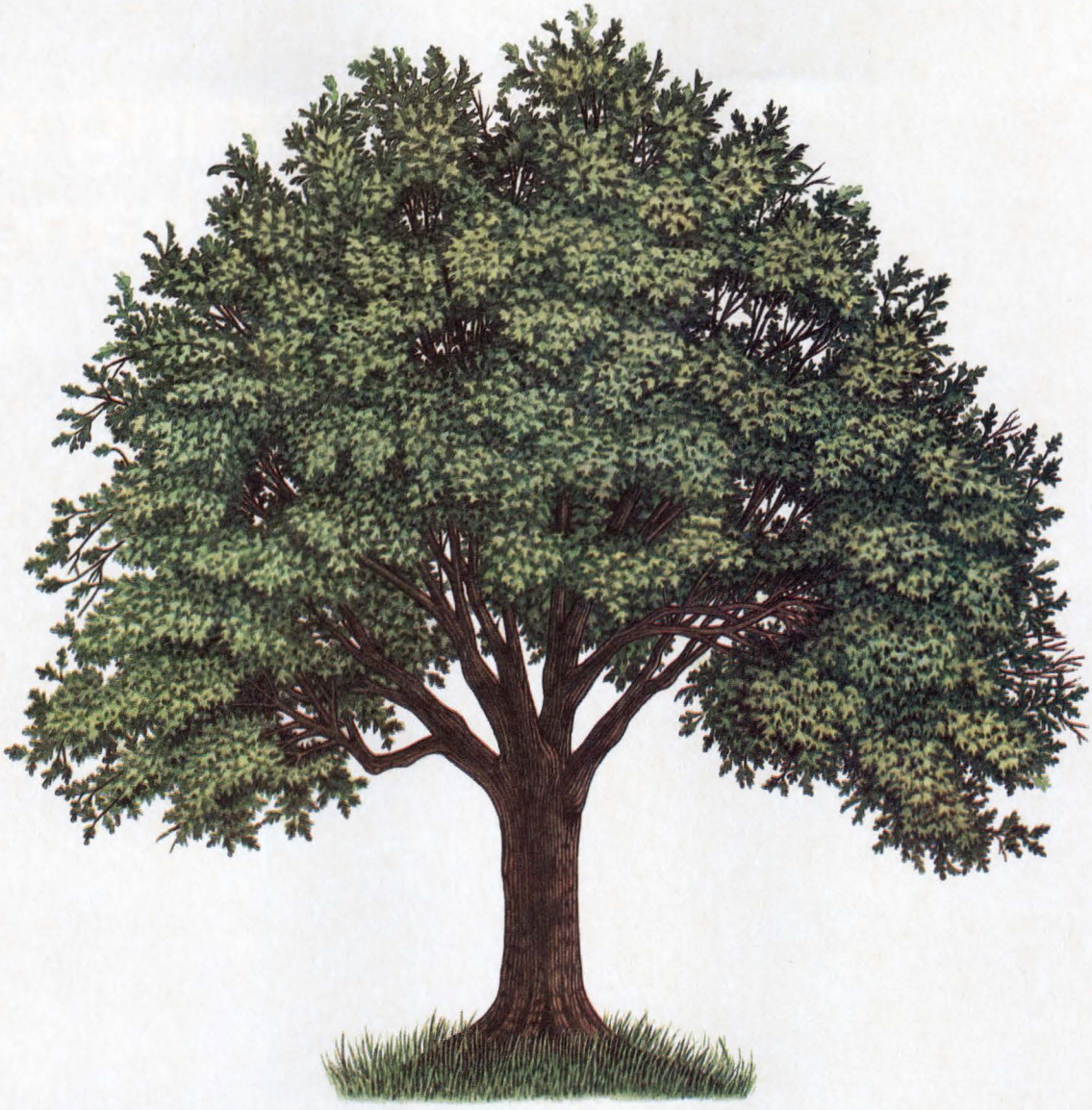

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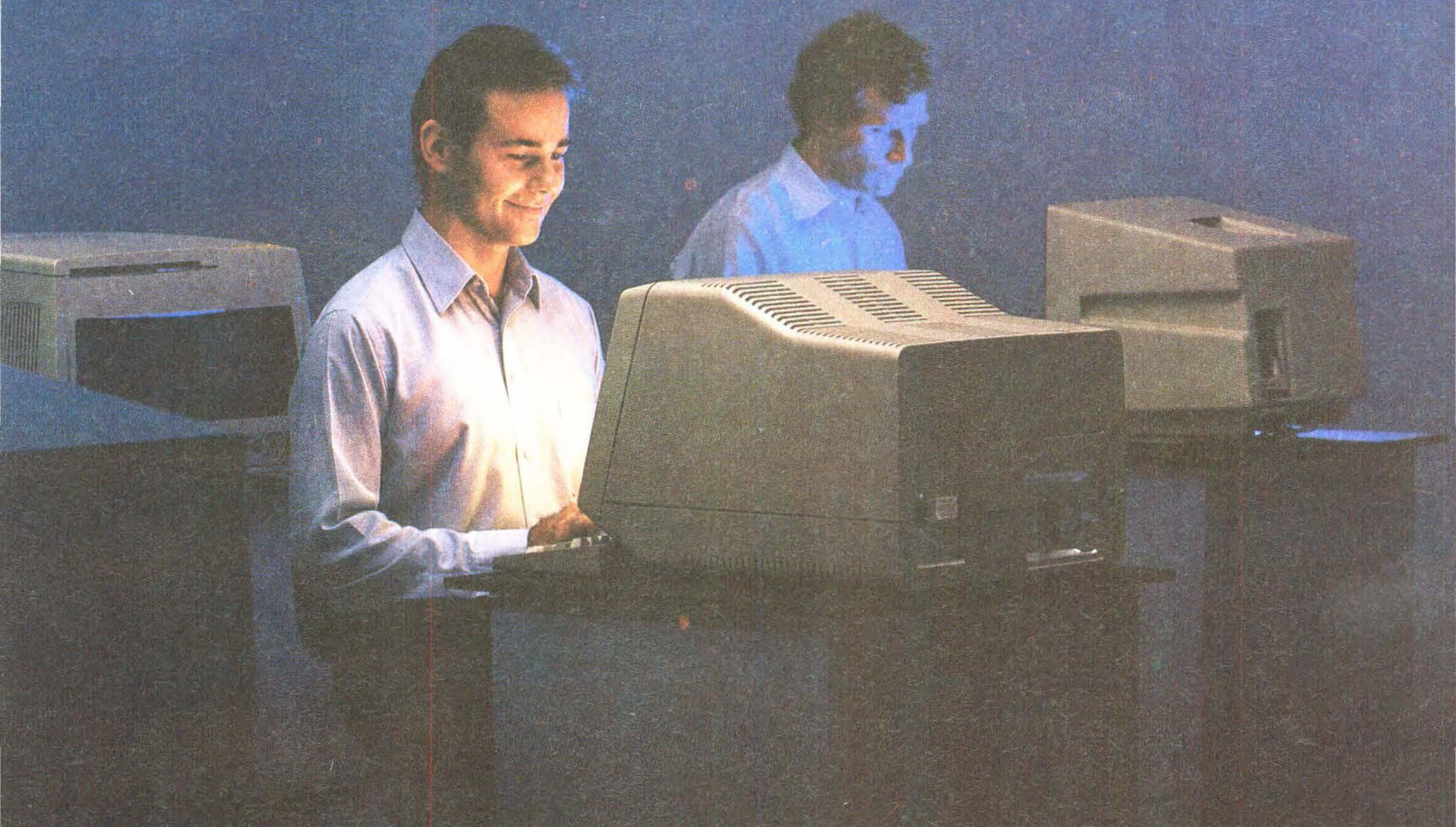

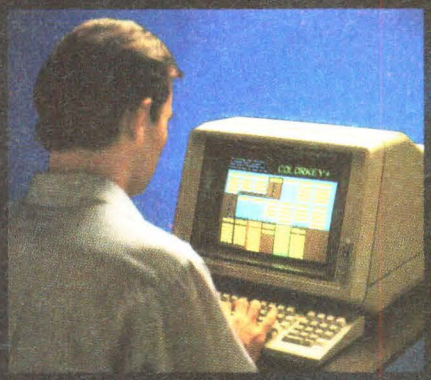

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Circle 20 for Literature
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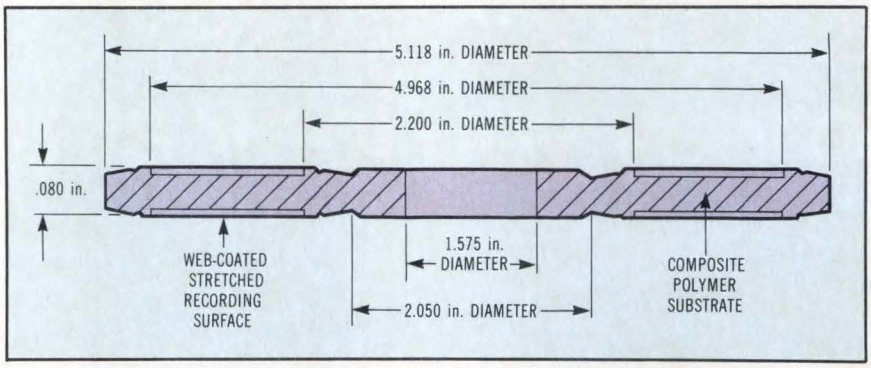
Stretched surface technology offers alternative to rigid disks

While the industry strives to perfect exotic magnetic recording technologies to meet the vast storage needs of the future, it is widely recognized that their practical use is still 5 to 15 years down the road. Rigid disk media in the 5¼-in. format range from single-platter, 5-Mbyte units that meet most small system needs to multi-platter devices that use plated media to pack in almost 400 Mbytes.

For applications making less stringent demands for both capacity and rapid access, however, flexible disks remain the media of choice. Tolerance to less than ideal environments and low cost have caused flexible disks to gain this status. Already promising to provide the first commercial devices using vertical recording techniques, the media also demonstrate their potential using other technologies.



In this profile of stretched surface technology, a rigid polymer composite substrate with 10-mil raised rims at the periphery and center hole supports a flexible media surface.

Flexible magnetic media products have already surpassed standard 300-oersted media operating in the 6000 flux changes per inch (FCPI) range, which has served the industry for years. Currently in their second generation, flexible-disk media now lie in the 500- to 700-Oe range and supply densities as high as 60,000 FCPI. Utilizing cobalt modified gamma ferric oxide, these media can generally be found in high capacity products such as Amlyn's 3.2-Mbyte floppy drive, in Iomega's Bernoulli disk cartridges, and in sub-5-in. diskettes.

Raising areal densities

Useful for recording 48 to 96 tracks/in. and storing from 500K to 1 Mbytes on 5¼-in. diskettes, the 300-Oe ferric oxide coating has served the industry well. Its follow-on 600-Oe media raise track density to 200 tracks/in. and bit density to 15,000 bits/in. This allows 2 to 5 Mbytes to be stored on a double-sided 5¼-in. diskette.

An 800-Oe medium made from cobalt enhanced isotropic particles, Isomax yields capacities from 5 to 10 Mbytes on 5¼-in. flexible disks. Developed by Eastman Kodak's Spin Physics subsidiary in San Diego, Calif, the medium allows track densities of 200 to 400 tracks/in., thereby serving as a bridge between conventional oxide media and thin films. One drawback is that the medium requires protection against contaminants in order to achieve its potential 45,000-bit/in. recording densities. In addition to a hard jacket with shutter assembly (similar to that used in Sony's 3½-in. microfloppy cartridges),

(continued on page 46)

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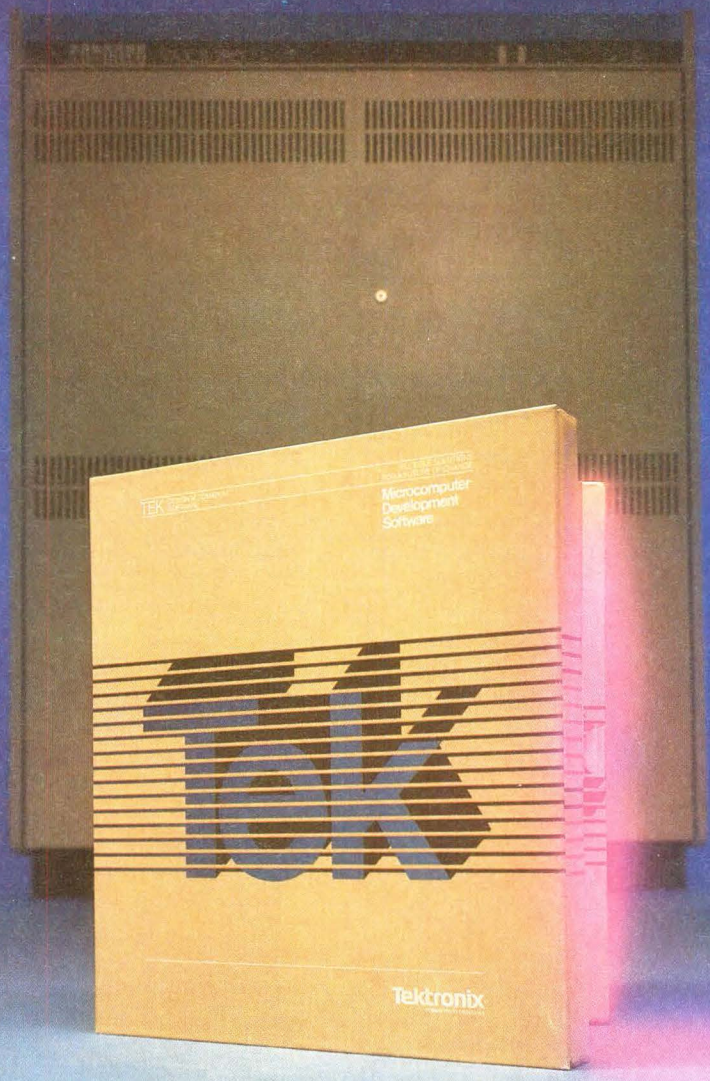

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Circle 23 for Literature
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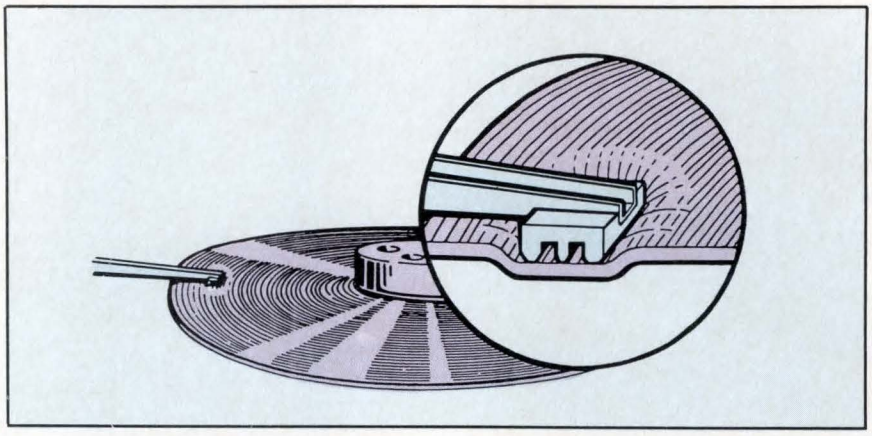
Stretched surface technology
(continued from page 44)



The flexible media surface of 3M's Keystone technology "dimples" as the head flies above it. This disperses many physical contaminants, thus minimizing head crashes.

Another contender aims to raise flexible media capacity without compromising traditional immunity to environmental hazards. The prototype, from 3M Co's Memory Technology Group, mounts flexible media on a rigid substrate to obtain rigid disk capacities. Used in the Keystone disk prototypes, this "stretched surface" technology achieves 20 times the storage capacity of ordinary diskettes, while retaining similar environmental tolerance.

Flexible media with rigid substrate

The prototype uses a rigid polymer composite substrate that has raised rims at the outer perimeter and near the center hole. A stretched 60-μin. thick 600-Oe flexible media base is bonded to the rims. The flexible medium lies 10 mils above the rigid substrate to form a resilient surface on both sides of the substrate. Resulting track stability shows anistropy of 200 μin.—about one-sixth that of standard diskettes or one-third that of high density diskettes.

Magnetic read/write heads fly above the media's surface as in rigid disk technology. However, the resiliency of the medium creates a "dimple" at the site of the head. This dimpling of the medium helps cast off dropout-causing debris, allowing the media to endure environmental hazards that conventional media will not normally tolerate. Error rates exhibited by prototypes equal those of rigid oxide or thin-film media—1 soft error in 10^{10} bits.

Existing disk drives need only minimal modification to accommodate the medium. For development purposes, manganese-zinc heads were slightly contoured and track width was reduced. Data band dimensions were slightly different, as were record current and amplifier gain. However, the performance of existing heads meets electromagnetic requirements and three-rail construction provides close (5 μin.) stable head-media spacing at the gap.

Prototypes have achieved reliable storage of 5 Mbytes/side in a 5¼-in. form factor using servo track definition. Initial products are expected to have 345 tracks/in. (fixed) or 200 tracks/in. (removable). Using particulate oxides, designers foresee capacities of 48 Mbytes/disk (fixed) or 37 Mbytes/disk (removable) on 728 and 580 tracks/in., respectively. Capacities to 100 Mbytes are expected when perpendicular or thin-film media come into use.

The Keystone disks will be offered as an alternative to metal substrate disks now used in Winchesters and other sealed media disk drives, as well as in removable cartridge drives. Prices are expected to be less than $10 each. **3M Co,** PO Box 33600, St Paul, MN 55133.

SYSTEM TECHNOLOGY
(continued on page 52)

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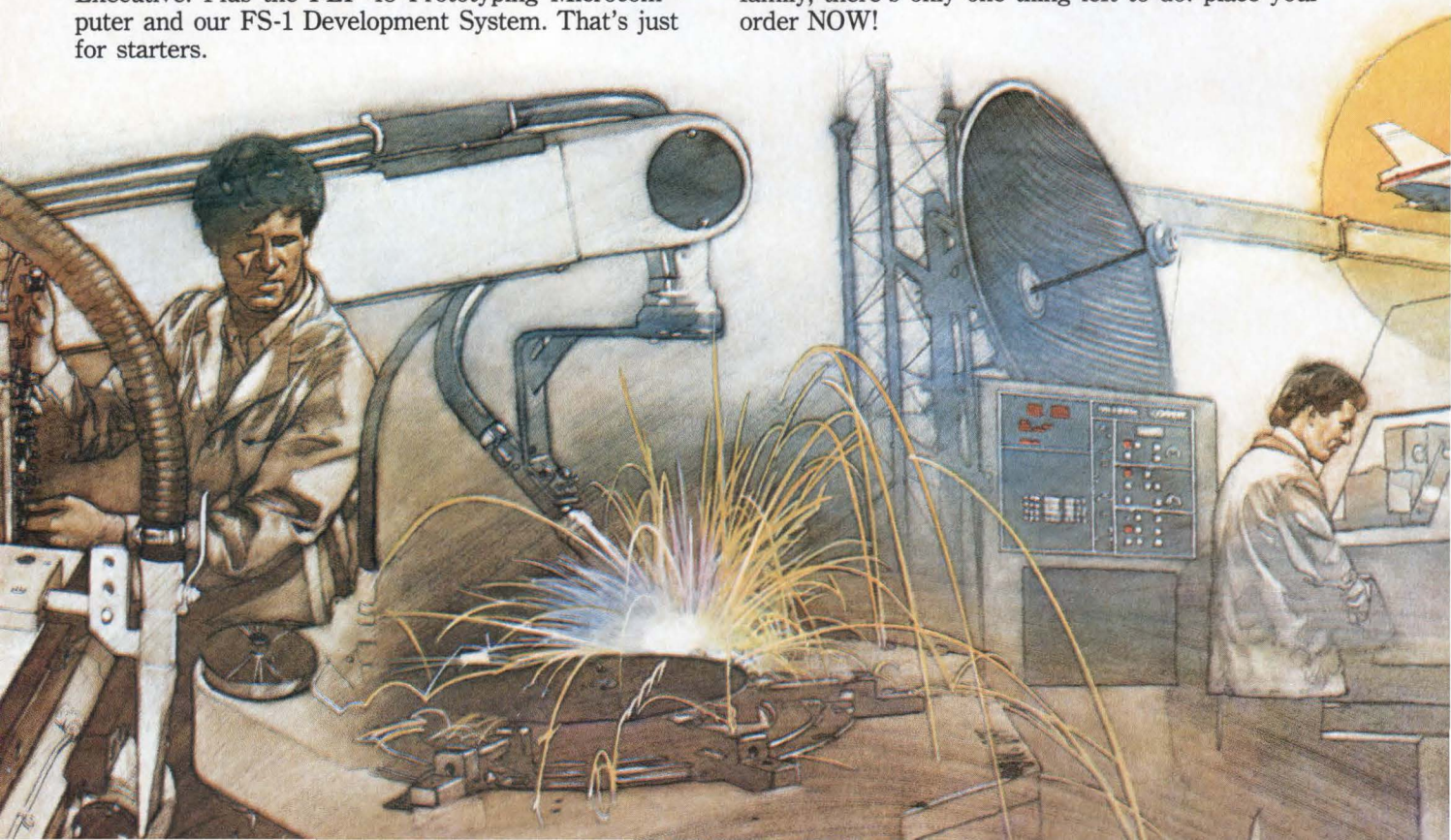

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F9444DC	Memory Management and Protection Unit Extends F9445 Addressing to 4MB Available 1st QTR 1984	85	27
F9470PC	Communications and Console Controller	74	22
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PEBUG45XX	PEPBUG-45 Monitor in ROMs	$250 ea	$100 ea
PEPTEST45X	PEPTEST-45 — Set of ROMs That Contain Test Program	400	160
PEPBAS45X	PEPBASIC-45 — Set of ROMs That Store PEPBASIC-45 Interpreter	170	95

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EMREX45XXX	EMREX-45 Real-Time Multitasking Executive	3,000	100
Cross Software and Linkers			
VAXCAS45XX	CASM-45 — VAX/VMS-Based Cross Assembler	600	40
FSIVAXLNKX	VAXLINK Allows linking of FS-1 and VAX™Computers	2,000	70
Compilers			
FSIPCIXXXX	F9445 Pascal	3,800	130
FSIFRTN66X	F9445 Fortran IV	3,400	115
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*100-Unit Prices Available on Request

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CIRCLE 26

After a few Northern

TI's Chicago Regional Technology Center saved Northern Telecom time and money with three logic-array prototypes.

Easy to design with, TI's TAL004 logic arrays are used in Northern Telecom's high-capacity MERCURY 8-inch Winchester disk drive (right) and in an optional controller for its advanced FLASHBACK tape drive (left).

Twice, Northern Telecom's Memory Systems Division relied on the nearby Texas Instruments Regional Technology Center in Chicago for semicustom circuits. And twice, TI came through.

First, with a TAL004 logic array to perform the data-integrity function in a Winchester disk-drive controller.

And second, with two TAL004 logic arrays to provide both the data/tape interface and data-integrity functions for an optional intelligent cartridge-tape controller.

Both controllers were going into state-of-the-art products. Northern Telecom's MERCURY™ 8-inch Winchester disk drive—90-225 MB capacity, less than 25-ms average positioning time. And

◀ **Working side by side,** TI and customer engineers run simulations to debug designs. Teamwork like this enabled Northern Telecom to do a month's work in four days at TI's Chicago Regional Technology Center. And thereby accelerate its product development schedule by three weeks.

days with Texas Instruments Telecom saved three weeks.

its FLASHBACK™ ¼-inch streaming cartridge-tape drive—nine-track (45/75 MB) or 12-track (60/100 MB).

Reduced IC count, costs, and time

Each semicustom TI logic array replaced 12 to 25 MSI chips for Northern Telecom. This allowed extra functions to be added at no extra cost in boards or parts.

Fewer ICs, fewer interconnects, a smaller board, and simpler manufacturing all combined to reduce costs by 50% to 75% vs. conventional SSI/MSI parts.

Custom LSI chips, too, would have been far more expensive. And would have taken 50% longer to design.

As little or as much support as you need

Northern Telecom selectively used the capabilities of TI's Regional Technology Center. In one case sending an engineer there to work alongside TI designers for two weeks. In another, they simply provided TI with the schematics, a functional description, and diagrams. TI engineers ran the simulations, identified bugs, and consulted daily with Northern Telecom engineers.

In both instances, Northern Telecom got "what it wanted, when it wanted it" from TI's Chicago Regional Technology Center. And plans to rely on the TI Center in the future. ■

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Uncomplicated complexity

TI's Low-power Schottky arrays—TAL002 and TAL004—provide a cost-effective, relatively simple entry point into semicustom circuit design (see table). Both interface directly with TTL-compatible devices, including all the microprocessor and memory components. When you work with TI logic arrays and with TI's new High-speed CMOS standard-cell products, you develop new systems using familiar design rules and can upgrade present systems easily.

TI TAL Logic Arrays

	TAL002	TAL004
Gates	280	400
Technology	LPS*	LPS*
Gate Delay	5.0 ns	5.0 ns
Gate Power	1.25 mW	1.25 mW
I/O Signals	29	42

*Low-power Schottky

Economical customization

With TI products, you get a customized device at a cost near that of standardized products. When you finalize your circuit, TI computer-verifies the design, builds prototypes for approval, and is ready for volume production.

Tap a Regional Technology Center for help

Your nearest TI Regional Technology Center is ready to help. Staff members will evaluate your needs at no charge to see if Low-power Schottky arrays are best for you. Or if one of TI's more complex logic arrays or one of TI's new High-speed CMOS standard-cell solutions would be your better choice.

If you wish, the Technology Center will contract to provide any or all necessary engineering services.

In fact, your nearest Regional Technology Center (see below) is your most convenient access to TI's unmatched combination of products, knowledge, and experience: Technical courses and seminars. Hands-on experience with a variety of TI semiconductor products. Demonstrations. Well-equipped laboratories. And midnight oil when necessary.

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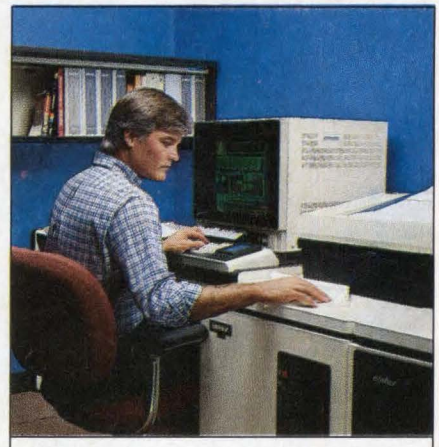

Computer-aided design: TI Regional Technology Centers are equipped with advanced engineering work stations to simplify semicustom product design, improve performance reliability.

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CIRCLE 27

Analyzers mate with personal computers to lower costs

Cost and wide availability make personal computers ideal candidates for a new group of peripherals—logic analyzers. By taking advantage of processor and display resources already supplied in Apple II, Tandy model II, and IBM PC hosts, these analyzers provide capabilities previously found on units exceeding $15,000. They have as many as 80 data input channels in addition to extensive trace and trigger functions at 10-MHz bus cycle rates.

Estimates suggest that there are nearly 450,000 personal computers used in scientific and engineering applications (typically scientific calculations, data acquisition, and production testing). Such vendors as Northwest Instrument Systems (Beaverton, Ore), Total Logic Corp (Fort Collins, Colo), and Treline (Irvine, Calif) hope to add state and timing analysis to these capabilities through a tight coupling of the test and measurement hardware with the processor and display resources of the personal computers via parallel links. This approach is in sharp contrast with the present industry practice of using either dedicated microprocessors, or linking instruments and controllers via an IEEE 488 general purpose interface bus (GPIB).

Logic Analyzer Comparison

	Northwest Instrument	Total Logic	Treline
Central processor	Apple II IBM PC	Apple II IBM PC	Apple II TRS-80
Number of data channels	16 to 80	16 or 32	8 to 112
Trigger word	15	16	8
Acquisition memory depth	2 Kwords	1 Kwords	2 Kwords
Sample rate	10 MHz	15 MHz	25 MHz

Architectural differences

One of the biggest benefits of this tightly coupled approach is that users can still access standard operating systems and languages on the host. Thus, users can take advantage of desirable application programs (eg, word processing, and spreadsheets), as well as floppy and rigid disk drives for mass storage, and retain familiar keyboards and displays.

Some analyzer vendors such as Dolch Logic Instruments (San Jose, Calif) and Kontron Electronics (Culver City, Calif) supply dedicated analyzers with similar capabilities at a higher cost. Among these are the ATLAS 9600 (see *Computer Design,* Dec 1982, p 66) and KLA 32. For example, a Kontron KLA 32 analyzer sells for about $14,500 with 32 input channels, dual disk drives, ASCII keyboard, and CP/M operating system. A similar system configured with an Apple II as the host as well as logic analyzer modules and associated software is available from Treline for less than $6000.

For dedicated analyzers, a large portion of the higher costs lies in a central processor design as well as keyboards and displays for user interaction. This is in addition to those facilities needed for data acquisition and storage, according to Chuck Nobles, product manager with Northwest Instrument Systems. On the other hand, personal computer-based analyzers need only provide the test and measurement hardware and software.

Another approach loosely couples standalone instruments with personal computers via an IEEE 488 parallel link (otherwise known as the GPIB). In this configuration, analyzers from vendors like Hewlett-Packard (Colorado Springs, Colo) and Tektronix (Beaverton, Ore) depend on personal computers such as the HP 200 for instrument setup, post acquisition analysis, and data formatting according to user specifications.

However, users often pay for duplicate sets of processor, memory, and display resources (in the instrument and computer). In addition, the IEEE 488 link can quickly bog down if several users frequently access acquired data on the bus.

A drawback to both dedicated and loosely coupled analyzers is the relatively low volumes that are sold (Nobles estimates 1000 units/year for certain models). This necessitates a higher price to offset design and development costs. Conversely, personal computer vendors like IBM and Apple charge much lower prices since they can spread costs over a larger number of units. Personal computer-based analyzer vendors hope that the large installed base in engineering and scientific labs gives them a similar cost advantage.

Analyzer comparisons

A prime example of the tightly coupled approach is the model 2100 state analyzer from Northwest Instrument Systems. It resides as a card set in a separate chassis linked to the backplane of the Apple II or IBM PC via a high speed parallel link. Within such a configuration, users place a controller card and up to five data acquisition/memory cards to get as few as 16 or as many as 80 data channels for state analysis.

A single 14-slot card cage houses the LA25-8 data-gathering modules and ETC-16 trigger and clock

(continued on page 54)

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CIRCLE 28

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Analyzers mate with PCs

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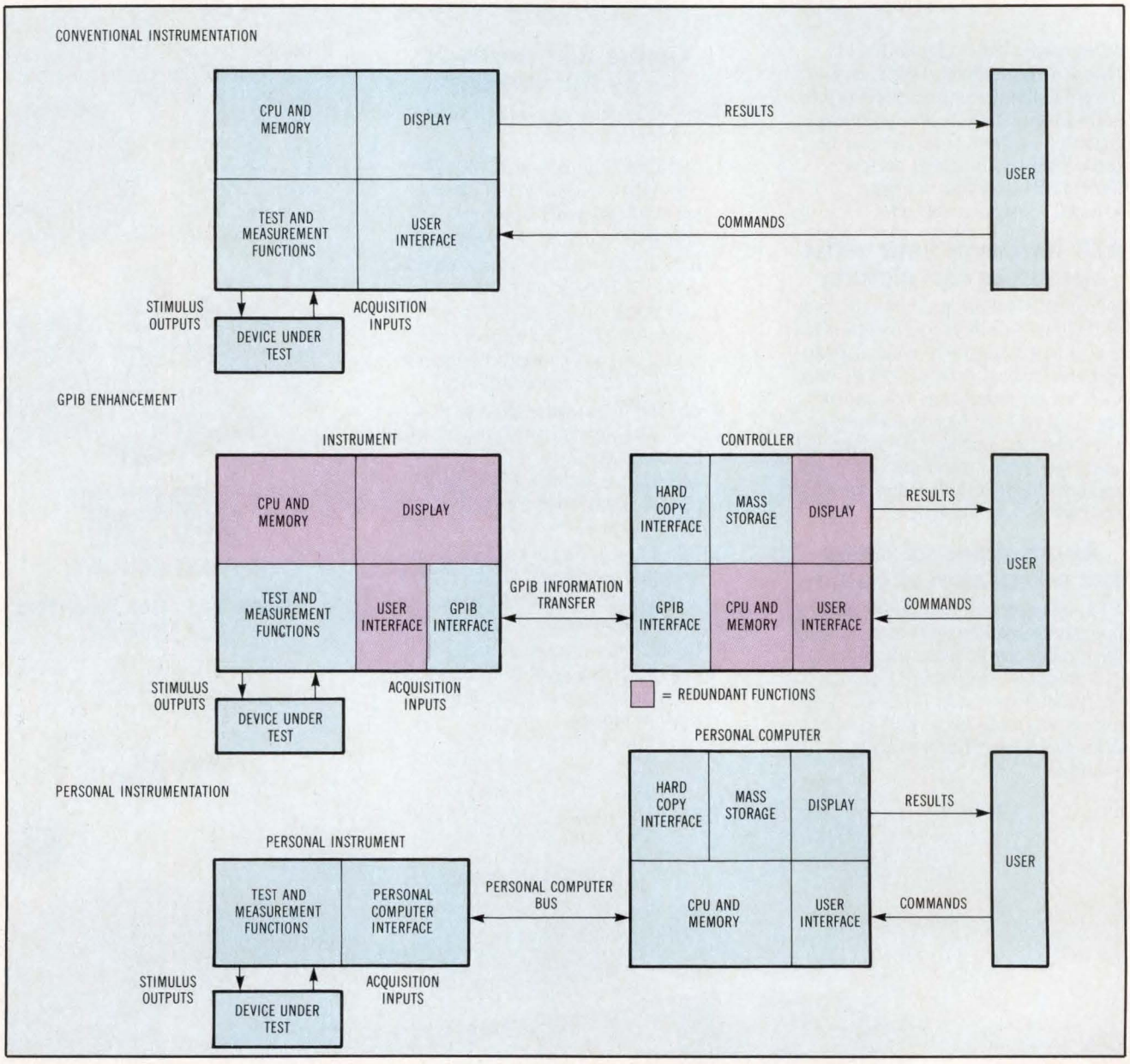

The personal computer-based instrumentation approach eliminates the need for a dedicated CPU with associated memory and display resources. This redundancy is a drawback to both the conventional dedicated instrument and loose coupling via a GPIB interface.

modules supplied by Treline. Like the model 2100, the Treline analyzer ties into the backplanes of Apple II and Tandy TRS-80 computers via a high speed parallel link (25 MHz typical). Users can configure the Treline system to handle from 8 to 112 channels on a single 14-slot card cage. The analyzer modules from Total Logic differ by physically residing on the backplane of an Apple II (LA-100) or IBM PC (LA-200). The LA-100 provides 16 data-input channels, while the LA-200 supports 32 channels.

The high speed parallel link (10-MHz data transfers), coupled with fast data acquisition memory mapped directly into the host processor address space, allows the model 2100 to have the same operating speed as if physically located on the backplane itself. Here, the user establishes a memory window in the analyzer by placing the beginning location into the segment register of the 8088 microprocessor. Through this 4-Kbyte memory window, the user directly manipulates either analyzer module to acquire data, set event conditions, or monitor system clocks. A similar scheme is used for both the Treline and Total Logic implementations.

For all three systems, programs and work space for calculations remain in the personal computer's main memory. A minimum of 128

(continued on page 56)

THE MULTIBUS*-
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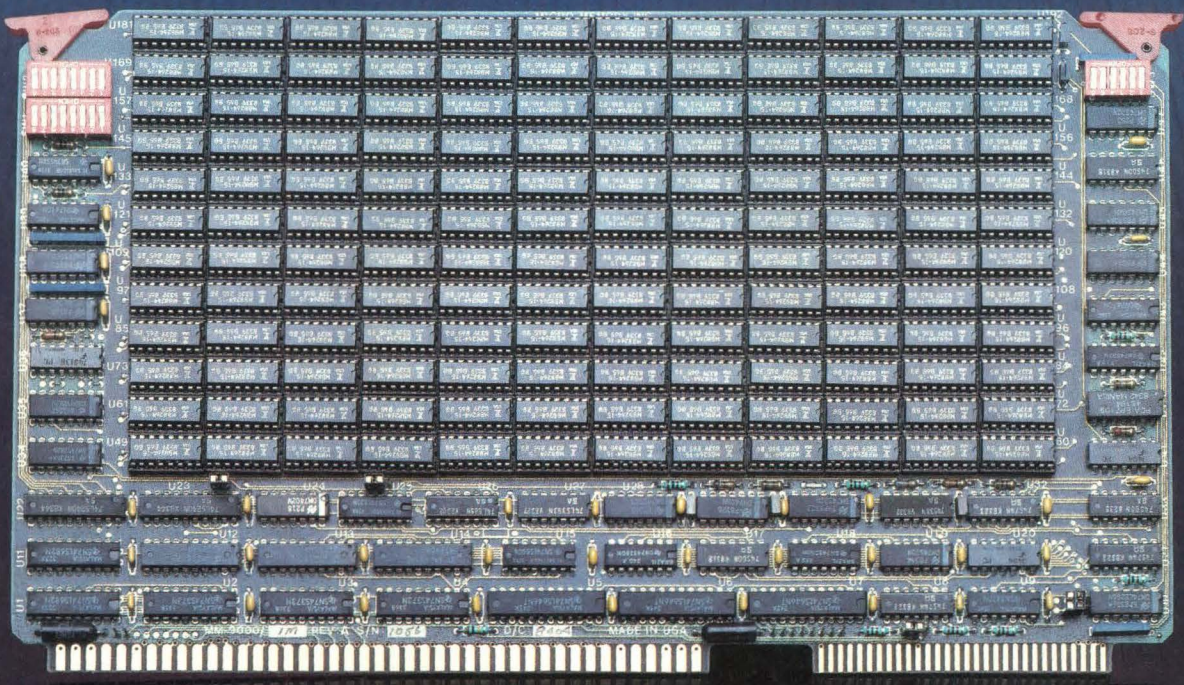

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PART NO.	CAPACITY	TYPE
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CIRCLE 29

Analyzers mate with PCs

(continued from page 54)

Kbytes is required to support the model 2100 analyzer (running under UCSD p-System Pascal) since code segments are heavily overlayed, with array sizes of 256 Kbytes more desirable for increased performance. The Treline analyzer requires a minimum of 48 Kbytes to run the Basic programs used (as does the Total Logic configuration for the Apple II).

In addition, the user can employ a portion of program memory to store reference data for comparison against data acquired from the model 2100. The Treline system uses the floppy disk for such purposes. Floppy disks are suitable for most applications on all three systems, although Northwest Instrument Systems recommends rigid disks if users continually switch analyzer setups.

The model 2100 state analyzer acquires data at bus cycle rates up to 10 MHz. Furthermore, users can synthesize their own sample clock from as many as five clock/control signals to track software in systems with complex bus cycles. Multiplexed buses easily unravel when two hold clocks latch information transferred during a two-phase bus cycle (address and data).

Trigger and trace

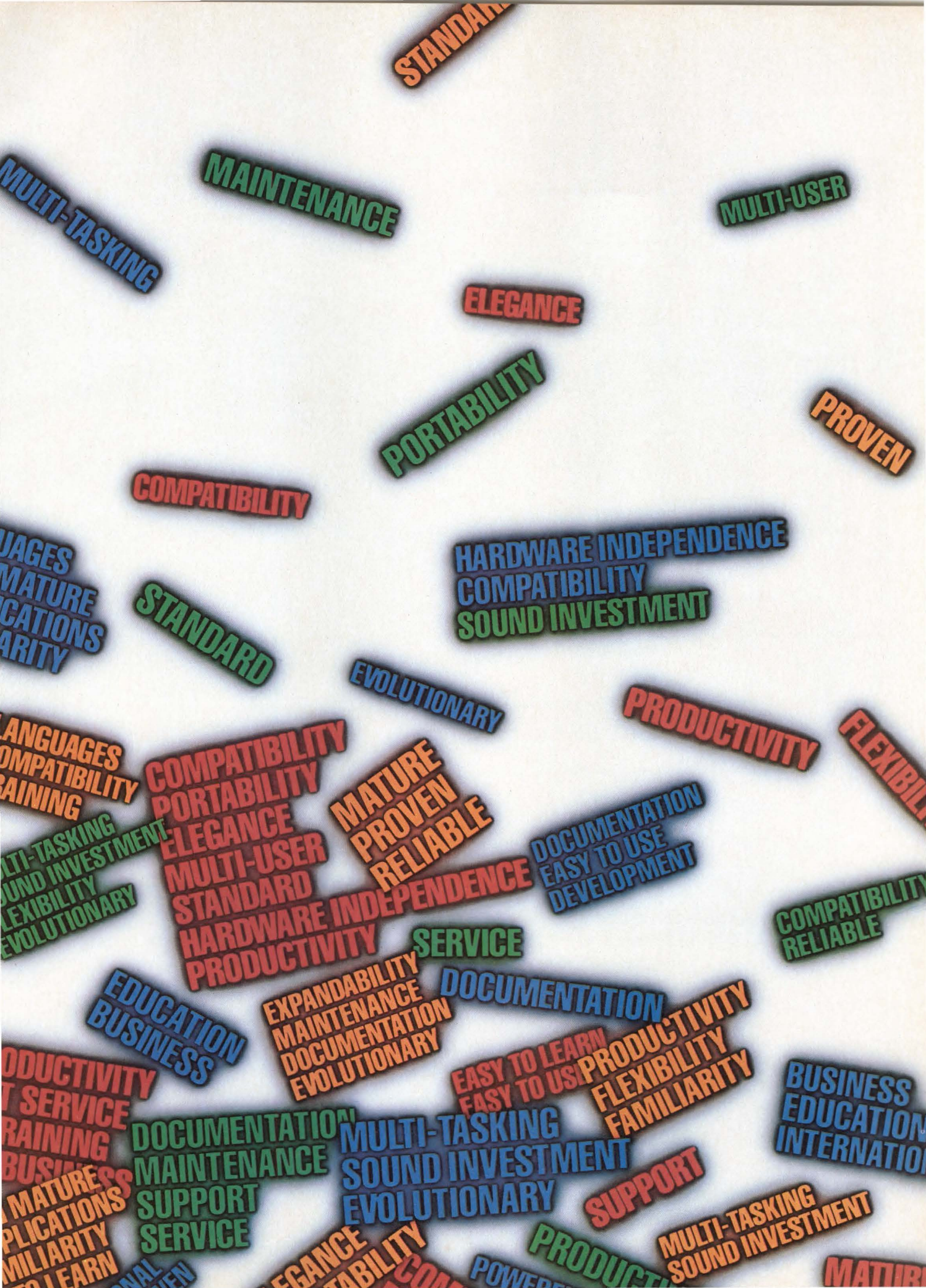
Extensive triggers on the model 2100 (as many as 15 trigger/store states) simplify tracing high level language execution. Users can define IF-THEN-ELSE condition sequences, as well as count iterations of events and specify logical relationships between conditions. Both trigger events and acquired data can be stored ondisk for future use.

As for the Treline analyzer, menu-driven displays format 8 bits of trigger information for each analyzer module. To eliminate race conditions, users can specify trigger filters of 0 to 7 cycles before enable, as well as trigger delays of up to 65,000 clock cycles before data collection begins. Greater depth than the 2 Kbits offered on a single card occurs when the eight probe inputs are tied to those of another module. In a similar way, trigger words can be extended from 16 to 512 bits (maximum).

The LA-100 analyzer has a 16-bit trigger word (the LA-200 has a 32-bit trigger word) with data stored up to 1024 words. Both have programmable delays from 0 to 1024 clock cycles in length. They also have two clock qualifiers (low and high).

Going beyond these capabilities, the model 2100 also supports object-code disassembly for many popular microprocessors. These include the 8080/Z80 and 6800 families of 8-bit microprocessors and such 16-bit processors as the 68000, Z8000, and 16032.

—Joseph Aseo, Field Editor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MULTI-USER
ELEGANCE
PORTABILITY
PROVEN
COMPATIBILITY
HARDWARE INDEPENDENCE
COMPATIBILITY
SOUND INVESTMENT
STANDARD
EVOLUTIONARY
PRODUCTIVITY
COMPATIBILITY
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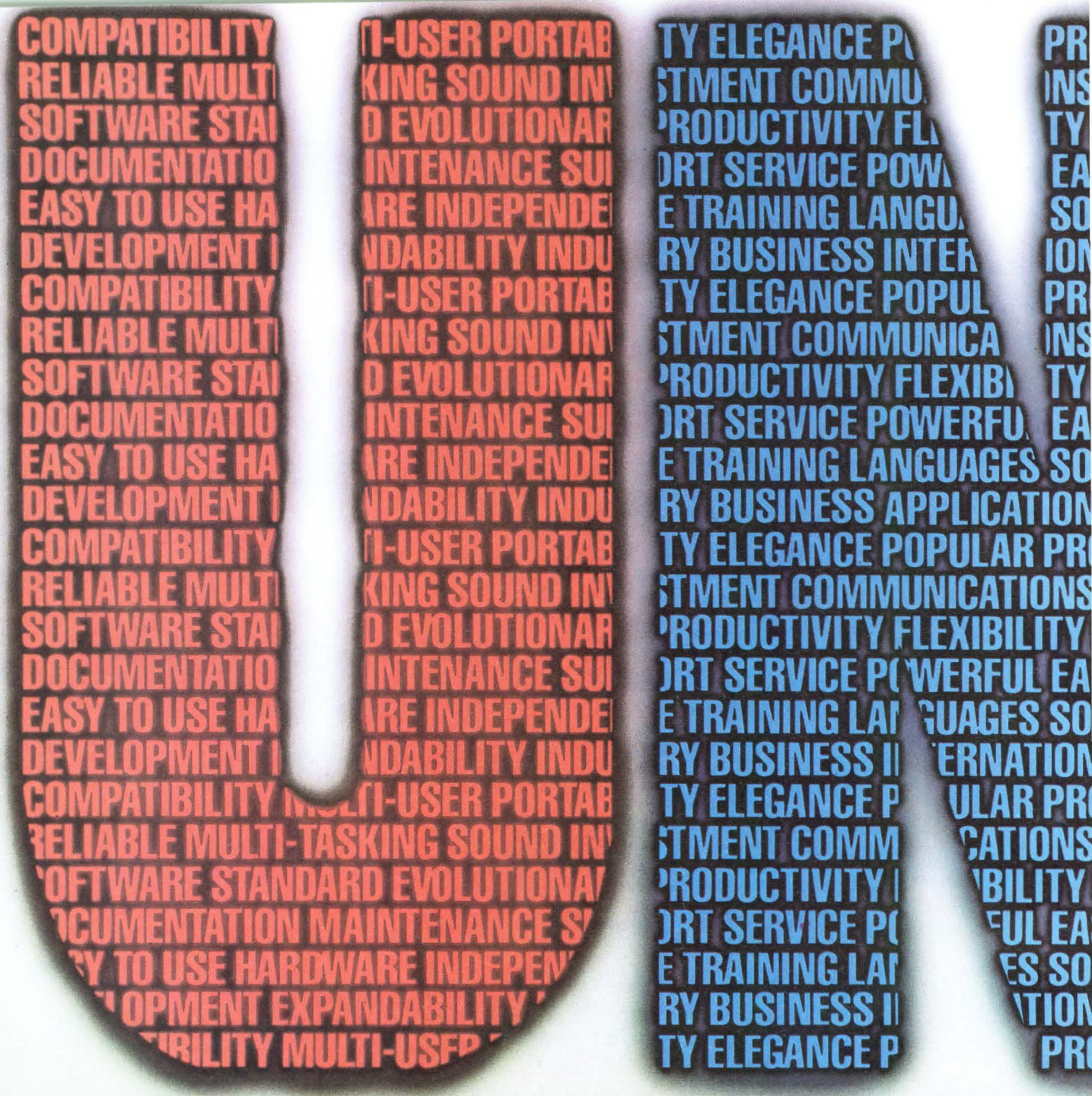

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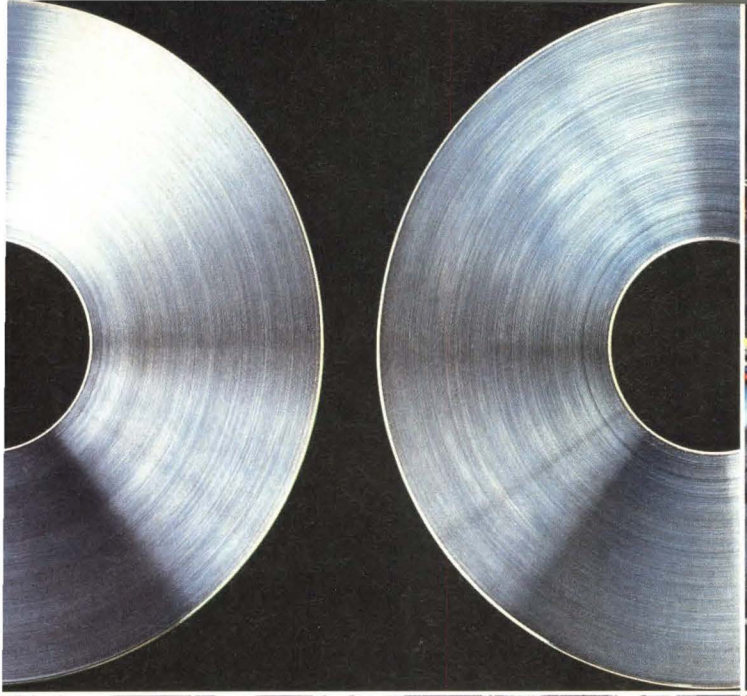
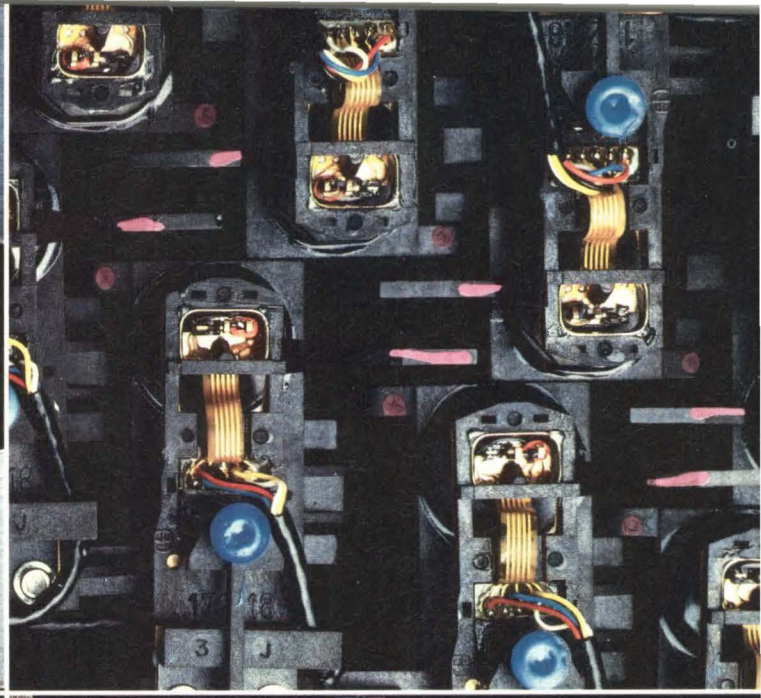
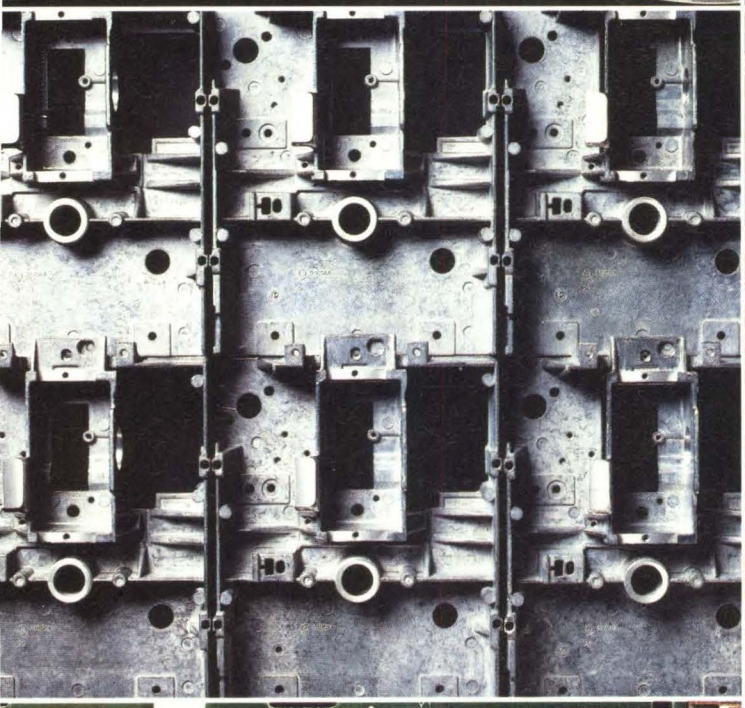
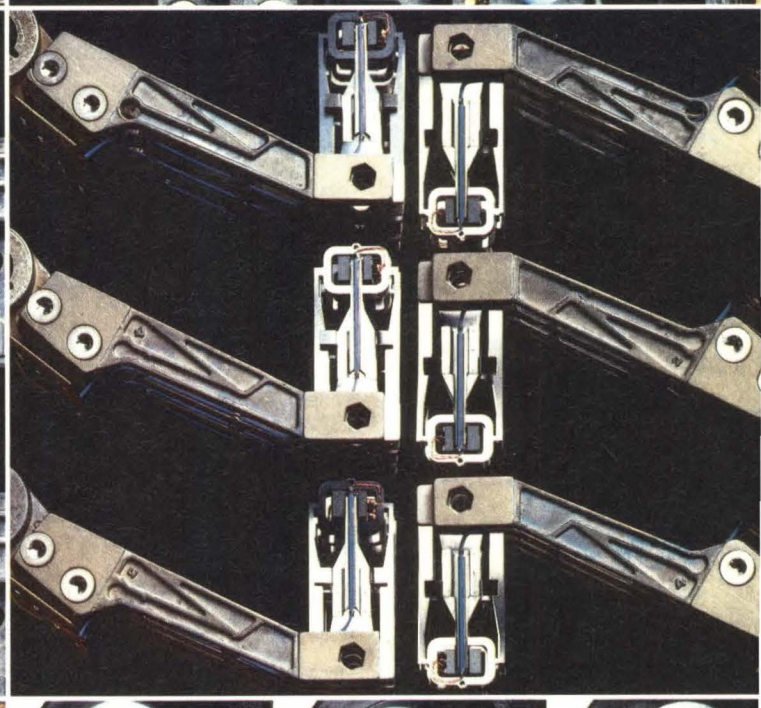
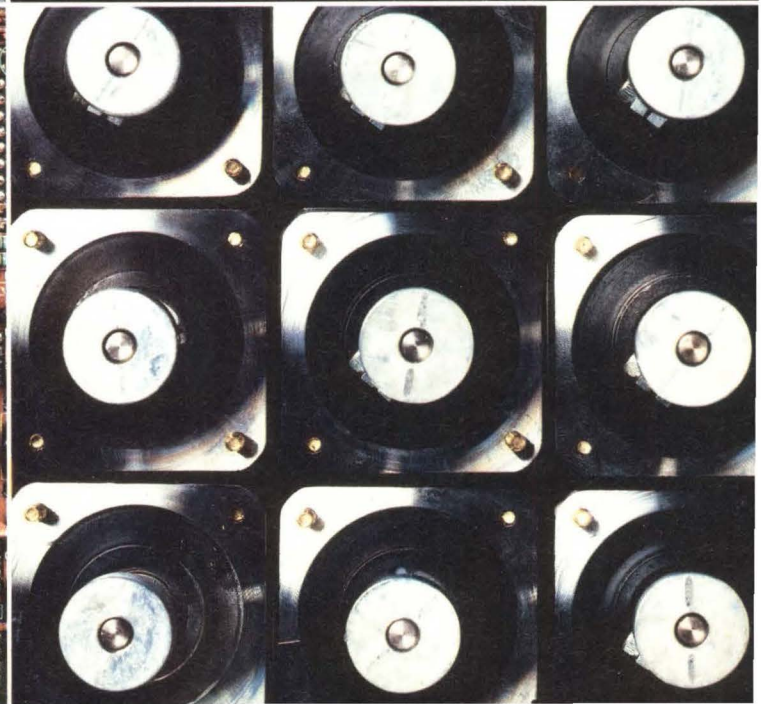
CIRCLE 32











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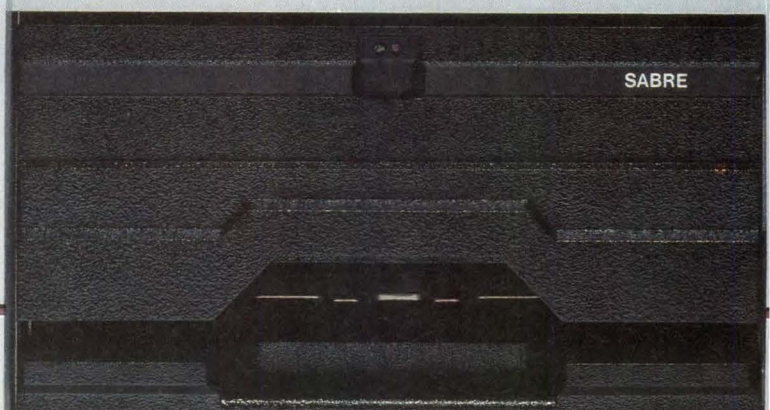

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Space-saving SABRE is 5¼" high, slips into any standard 19" Retma enclosure and comes complete with power supply, host adapter and connecting cables. It needs one-eighth the space and draws one-quarter of the power of four RL02's. Further, SABRE slashes hardware and installation costs by eliminating the need for a separate system bootstrap, bus terminator and clock control board.

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CIRCLE 33

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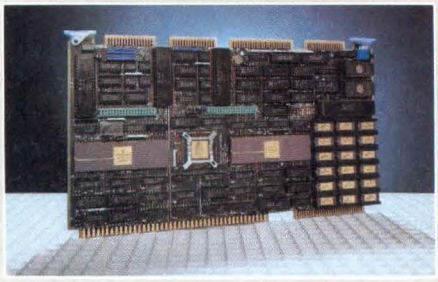
MLZ-90A single board microcomputer with nine byte-wide memory sockets for use with RAM or ROM (AM9511 and floppy disk drive controller optional).

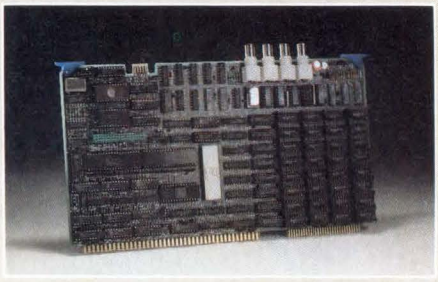
MLZ-91A single board CP/M™ system with on-card floppy disk drive controller, winchester interface, optional AM9511, streamer tape interface, two serial ports, one parallel port, 64K bytes RAM with parity, two EPROM sockets, and GPIB CONTROLLER.

MLZ-92A single board CP/M™ system with four serial ports on-card, floppy disk drive controller, winchester interface, optional AM9511, Centronics printer interface, 64K bytes of RAM with parity, and two EPROM sockets.

MLZ-93A single board CP/M™ system with 128K bytes of dual ported RAM, four EPROM sockets, floppy disk drive controller, optional AM9511 and powerful serial port features including SDLC and HDLC protocol support and modem controls.



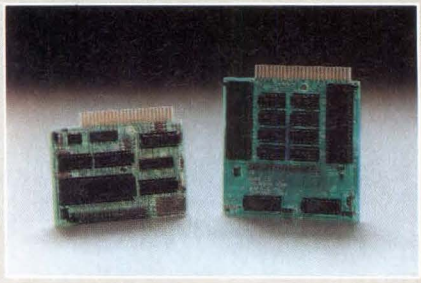
HK68™ powerful and versatile single board UNIX™ or CP/M-68K™ system with MC68000 CPU, MMU, quad channel DMA, four serial ports, 128K or 256K bytes of on-board RAM with parity (expandable to 1M byte on-board!), and two iSBX™ connectors for I/O expansion.



MLZ-VDC intelligent 640 x 480 x 4 color graphic controller based on the NEC 7220 controller chip with on-board Z-80 CPU, DMA controller, and user definable FIFO interface to Multibus.™ Users may display up to 16 colors from a 4K palette. Up to 1024 x 1024 x 3 interlaced also available.

iSBX Expansion Models
Heurikon also stocks iSBX™ modules for I/O expansion on its HK68 and MLZ-VDC. These modules may be used on any other board complying with Intel iSBX specifications.

Presently available are the SBX-FDIO floppy disk controller module and the SBX-SIO serial port expansion module.



The SBX-FDIO can control up to four single or double sided, single or double density 5¼ inch or 8 inch floppy disk drives. A software toggle allows both 5¼ inch and 8 inch drives to be intermixed on the same cable!

The SBX-SIO is a quad serial port expansion module utilizing Zilog SCC controller chips with built in baud rate generators. The SBX-SIO is available in synchronous and asynchronous models.

Systems
Heurikon also supplies completely integrated systems with your choice of CP/M-80™, MP/M-80™, CP/M-68K™, and "Berkeley enhanced" Unix operating systems.

Systems are available with four, six, and fourteen slot enclosures with 5¼ inch or 8 inch dual floppy or floppy winchester drive combinations.

CIRCLE 34

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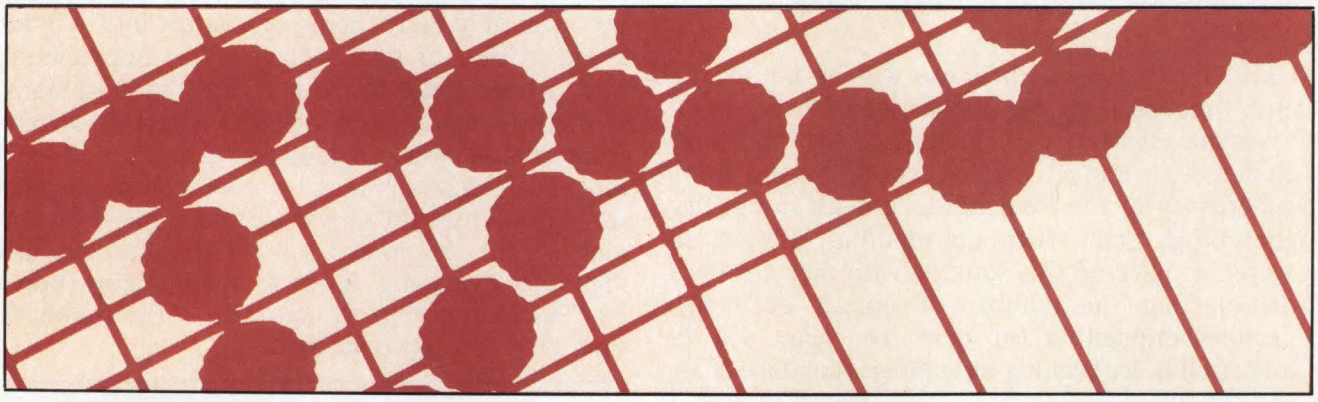

by Bryan M. Doherty, Jr and David V. Bryant

In the last few years, a bewildering array of hardcopy computer output devices has appeared on the market as the result of fast-paced technological advancement and ever-increasing application requirements for computer printing. While technical developments have generally accelerated the output of the printed word, only recently have printer manufacturers started paying a great deal of attention to improving the quality of the print. In the quest for print quality, engineers have probably spent more time and money on developing matrix printing techniques than on any other method used to create character shapes on paper.

Two converging elements have fueled the race for better print quality: the explosive growth in the use of computers in business, with the vast majority of computers (and hence printers) placed in executive offices where more applications require high quality output; and the desire to automate the office, which influences the type of office printing used. As a result, a strong emphasis on integration has yielded new multifunctional workstations that combine data processing, word processing, and graphics capabilities. This equipment needs to be interfaced with printers that can provide multifunctional output. And, with more integrated software packages giving the user the option to mix text, data, and graphics on the screen comes the printer requirement to replicate this mixed screen image on paper. Of all the printing techniques, only matrix printing technologies offer the potential for this variable print quality.

The requirement for multiple levels of output quality has stimulated much research and development in matrix printing technology. At the high end, full-page printers have improved in both print quality and speed, while decreasing in cost. Most page printers, however, remain prohibitively expensive except in very high volume applications.

On the other hand, low end nonimpact technologies, such as ink-jet and thermal transfer, have finally begun to emerge in greater numbers. However, past reliability problems and a natural cautiousness concerning the acceptance of a new technology continue to hinder their growth. In addition, ink-jet and thermal transfer printers have not yet demonstrated true letter-quality output.

Bryan M. Doherty, Jr is a founder and vice president of marketing at Advanced Matrix Technology, Inc (AMT), 1157 Tourmaline Dr, Newbury Park, CA 91320. Mr Doherty holds an MBA in marketing from San Francisco State University.

David V. Bryant is a senior software engineer at AMT. He is the creator of the printer driver for AMT's Office Printer, and the Font Generator Program.

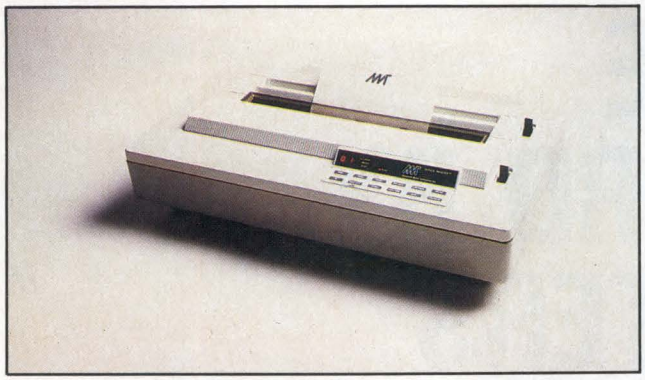

Fig 1 The Office Printer allows letter-quality, dot-matrix printing in three modes: 45 chars/s, 100 chars/s, and 250 chars/s. In addition, its multigraphics sport a resolution up to 240 x 720 dots/in. Multiple fonts are available and are embedded in firmware. Printer price is $2895.

Until that happens, their use will be limited for multifunctional printer applications.

Advanced Matrix Technology (AMT) thus concluded that impact printers could be the prime beneficiary of the tremendous growth in business computing and office automation. Market researchers back up this forecast with their own prediction that the number of impact dot-matrix printers shipped in the next five years will far exceed all other printing technologies combined. The reasons they cite are many: the proven reliability of a mature technology; prices that are in line with the overall system cost; the ability to handle existing business papers and forms; multiple-font flexibility that is suited to scientific and international requirements; color printing; and even more significant, the recent dramatic improvements in print quality, which place the printed output on a par with fully formed character printers.

Only a few printer manufacturers have been able to offer a product with all the desired features. Achieving a level of quality that will pass the critical test of acceptance for business correspondence and formal documents, as well as produce high speed output and high resolution graphics, has presented dot-matrix printer manufacturers with some difficult problems.

Defining print quality

The first and perhaps most controversial issue that any printer manufacturer faces is defining print quality. Without standards by which to judge the final output, it is difficult to set engineering and manufacturing goals. This is further complicated by individual objective and subjective evaluations of print quality.

Objectively, print quality can be judged by measured character elements. Dot separation (resolution), dot size, accuracy of placement, contrast, and dot density are all variables that influence the perception of dot-matrix image quality. In addition, each variable can be quantified. Both IBM (Armonk, NY) and Xerox Corp (Stamford, Conn) researchers conducted extensive studies in print quality in order to establish the threshold at which the human eye detects dot-matrix printing. (Studies include the IBM Report TR00.2464, Aug 1973, and the Xerox Report in the *Journal of the Society of Photo-Optical Instrumentation Engineers,* Bellingham, Wash, vol 310, 1981.) By graphing dot diameter versus resolution (dots/in.), the researchers were able to describe a "region of uniform edge perception." The results from both companies were remarkably consistent and continue to provide a guideline for manufacturers setting product/print quality goals.

The subjective evaluation of print quality has experienced equally extensive scrutiny over a much longer period of time. Much of the appreciation for "proper" letterforms started with the Romans. A person's visual ideas of good letterforms come from models based on good past designs, and from the transformations they have undergone through the years. Thus, the challenge that is faced by dot-matrix font developers, or for that matter, any digital font designer, is not so much to copy previous letterforms, but to conform to the standards that have been set over time.

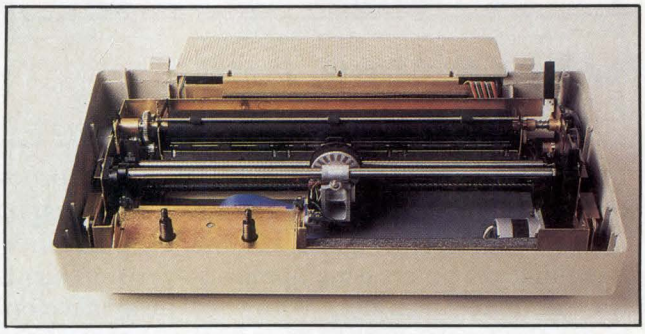

Fig 2 The printer's sturdy mechanism is one key element that ensures high quality print. Its single-piece frame creates a rigid foundation for accurate, vibration-free printhead movement. A stepper motor control, in conjunction with a lead-screw/nut assembly for preventing backlash, also contributes to accurate dot placement.

There are good reasons for dot-matrix font developers to study the past. The quality of the letterforms determines the quality of the entire communication method. Witness the staunch resistance to accepting anything less than "letter" quality for business correspondence. Familiarity is a large factor in legibility, and legibility is an important measure of quality. For example, the familiarity that the business community has with the IBM Selectric typefaces, such as Courier and Letter Gothic, has a very strong influence on the judgment of acceptable print quality from alternate technologies.

One additional key aspect of print quality and matrix font development has to do with taking

character sets or fonts as a whole. Michael Parker, president of Bitstream, Inc (Cambridge, Mass), a company developing digital typefonts, sums up this concept by stating that, "A good font is not a group of beautiful characters but rather a beautiful group of characters." In other words, characters must be taken in context as parts of words and sentences, and judged on their quality and harmony with the whole. Having once made the effort to study and establish print quality goals, the dot-matrix printer manufacturer can then set out to specify the product for engineering.

To refine is to excel

AMT's primary design objective is to have true letter-quality printing at speeds comparable to daisy wheels. To achieve that objective, the company's first product, the Office Printer (see Fig 1) was constantly refined during the prototyping and testing of mechanical and electronic systems. This refinement was done to determine the variables and interactions that would affect print quality.

The output quality from the mechanism proved to hinge on the frame's rigidity. This conclusion also confirmed the belief that a true letter-quality printer had to be designed from the ground up. Single-unit frame construction created an extremely strong and rigid foundation fundamental to highly accurate, vibration-free movement of the printhead.

The carriage assembly consists of a stepper motor drive, Teflon-coated lead screw, antibacklash nut, and printhead platform (Fig 2). The precision stepper control and the antibacklash properties of the lead-screw/nut combination are critical to the accuracy and repeatability of dot placement and the minimization of printhead oscillation.

The printer uses a DH Technology, Inc (Sunnyvale, Calif) 16-wire printhead. The wires are arranged in two staggered columns of eight wires each. Wire diameter is 0.012 in. Letter-quality print is achieved by dual-pass printing. After printing the first pass, the printhead returns to make a second pass in the same direction as the first. Prior to the second pass, a precision microshift mechanism mounted on the printhead platform increments the printhead, resulting in a one-quarter dot offset in the vertical axis. This produces a density of 240 vertical dot positions/in. At the same time, the printhead and carriage drive electronics and printer driver firmware are working in unison to provide precise firing of printhead wires and carriage movement. This delivers 1/720-in. position accuracy, of 720 dots/in. horizontally.

The ribbon system is an often overlooked factor in achieving optimum print quality. Contrary to some preconceived ideas, AMT engineers found that multistrike Mylar ribbons did not produce the best print quality when compared to a nylon fabric ribbon with carefully chosen fabric weave and ink formulation. For instance, for the given wire diameter (12 mil), the Mylar ribbon produced a denser but somewhat larger dot than that produced with the fabric ribbon. Also, in informal testing, the wider stroke widths produced with the Mylar ribbon were judged less acceptable than those produced with the fabric ribbon. Finally, the ink formulation on the ribbon proved to be highly significant because traditional matrix inks have a tendency to bleed over time and degrade the image. Thus, AMT engineers opted to develop a proprietary ribbon that optimizes both print quality and print life.

Font-asizing can be productive

The printer driver firmware, the last element of the printer's design, contributes significantly to high quality print. The firmware provides the intelligence to direct and monitor the mechanical subsystems with the timing essential for accurate dot placement. The firmware also receives and processes data while accessing and interpreting complex character lookup tables for printing out the data. The lookup tables are stored in 8-Kbyte ROMs

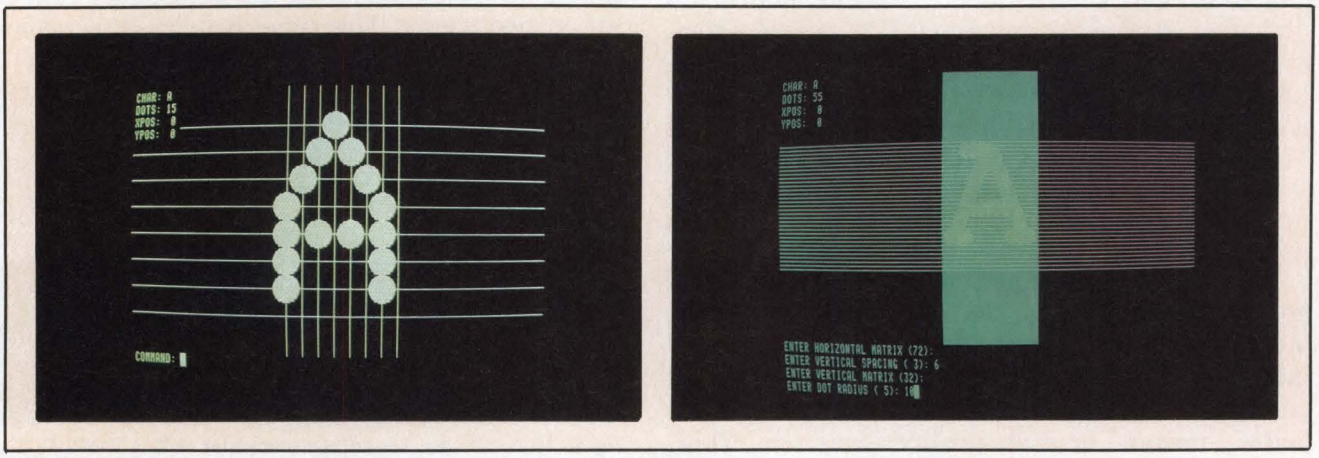

Fig 3 Here, an example of an 8 horizontal x 8 vertical draft/data quality matrix (a) is compared to a 72 horiztonal x 32 vertical letter-quality matrix (b). The letter-quality matrix screen display on right also shows matrix setup variables at the lower left.

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BODY FORCE IN MATERIAL MEDIA, STATIONARY

$$\mathbf{f} = \rho\mathbf{E} + \mathbf{J} \times \mathbf{B} - \frac{\varepsilon_0}{2}E^2\nabla\kappa - \frac{\mu_0}{2}H^2\nabla\kappa_m + \frac{\varepsilon_0}{2}\nabla\left(E^2\frac{\partial\kappa}{\partial\rho_m}\rho_m\right) + \frac{\mu_0}{2}\nabla\left(H^2\frac{\partial\kappa}{\partial\rho_m}\rho_m\right)$$

$$\mathbf{f} = \rho\mathbf{E} + \frac{\mathbf{J} \times \mathbf{B}}{C} - \frac{E^2}{8\pi}\nabla\kappa - \frac{H^2}{8\pi}\nabla\kappa_m + \frac{1}{8\pi}\nabla\left(E^2\frac{\partial\kappa}{\partial\kappa_m}\right)\rho_m + \frac{1}{8\pi}\nabla\left(H^2\frac{\partial\kappa_m}{\partial\kappa_m}\rho_m\right)$$

NAVIER-STOKES EQUATIONS OF MOTION FOR AN INCOMPRESSIBLE FLUID

P = Pressure
$\mathbf{F}$ = Body Force Density
μ = Viscosity

(a) Vector

$\mathbf{V}$ is the velocity vector.

$$\rho\frac{D\mathbf{V}}{Dt} = \rho\left[\frac{\partial\mathbf{V}}{\partial t} + (\mathbf{V}\cdot\nabla)\mathbf{V}\right] = \rho\left[\frac{\partial\mathbf{V}}{\partial t} + \nabla\left[\frac{V^2}{2}\right] - \mathbf{V}\times(\nabla\times\mathbf{V})\right]$$

$$= -\nabla P + \mathbf{F} - \nabla\times(\mu(\nabla\times\mathbf{V}))$$

(b) Cartesian Tensor

w_i is the velocity in the x_i direction.

$$\rho\left[\frac{\partial w_i}{\partial t} + w_j\frac{\partial w_i}{\partial x_j}\right] = -\frac{\partial P}{\partial x_i} + F_i + \frac{\partial}{\partial x_j}\left[\mu\left[\frac{\partial w_i}{\partial x_j} + \frac{\partial w_j}{\partial x_i}\right]\right]$$

In this sample printout, the optional general scientific character set shown at top may be mixed with other fonts to produce equations using common symbol conventions.

and generally represent a letter, memo, and draft quality of a given font.

In their quest for high resolution matrix printers capable of true letter-quality printing, matrix printer manufacturers have increased the data storage and processing requirements for a given character set. Low resolution matrix printers might feature character matrices of only 5 x 7 or 9 x 9 dots/character, or 35 to 81 possible dot positions. This makes the job of designing fonts by hand on paper a manageable task. AMT's letter-quality character matrix, on the other hand, is 72 horizontal x 32 vertical potential dot positions/character (Fig 3). This is more than 2300 possible bits/character, or up to 220,000 bits/96-character set. While no font has characters that occupy every dot position in the matrix, the obvious tedium and time involved in designing high resolution fonts has urged manufacturers to seek more automated font development methods.

In order to reduce the time required to build an extensive font library, AMT's software engineers have written a font generation program designed not only to speed the font development task but also to accommodate the variable matrices used for letter-, memo-, or draft-quality characters. Thus, the Office Printer, which is designed for the office automation market, has fonts available that represent many of the most commonly used business fonts, such as Courier 10 and 12, Letter Gothic 12, Orator, and numerous specialized character sets (see sample printout).

The font generation program is implemented on a Northstar Advantage (San Leandro, Calif) microcomputer with a 5-Mbyte hard disk using Northstar Graphics CP/M and a custom Z80 assembly program (Fig 4). An additional program for automatic generation of circles and ellipses is written in Microsoft Basic. The average time required for development of a letter-quality font is one to two weeks. This time includes font review and two to three iterations of character refinement.

Fig 4 A Northstar Advantage computer with a 5-Mbyte hard disk is used to develop all fonts for the Office Printer. On the average, letter-quality fonts can be developed in one to two weeks using this system.

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SUPER. MICRO.

CIRCLE 35

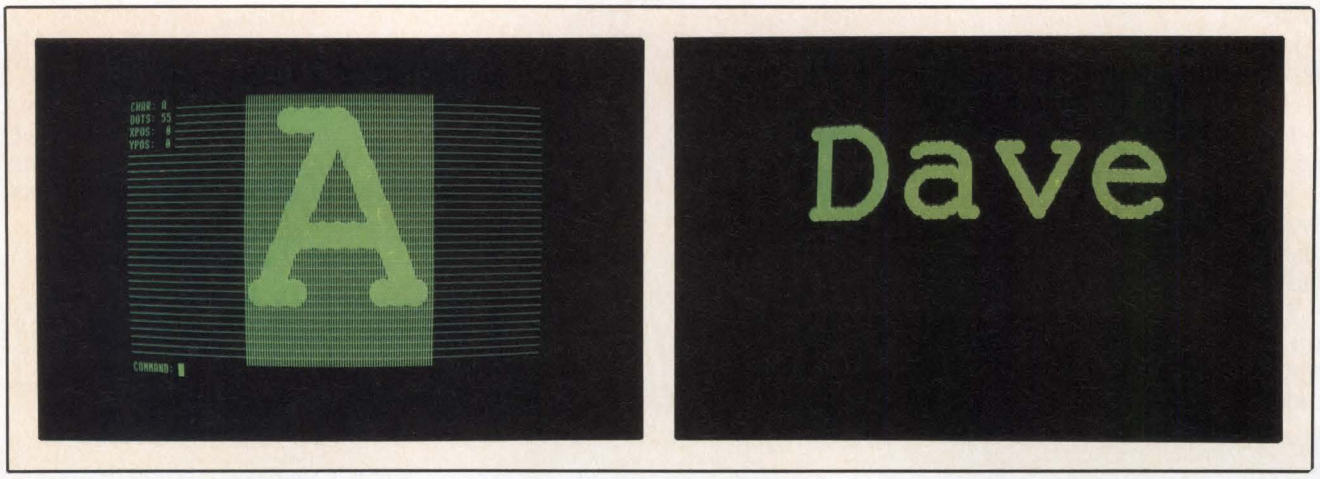

Fig 5 The actual character shape in a letter-quality 72 horizontal x 32 vertical matrix sports true portion dot diameter. The character name, number of dots in character, and X-Y position of the cursor are displayed in the upper left corner (a). A screen display of characters in context helps font developers visualize character interaction, thereby allowing subjective evaluation of a font in terms of actual use in words and sentences (b).

The first step in font development involves the measurement and analysis of the selected font. This work is performed on paper prior to going to the computer. Typically, daisy wheel printwheel books are used as the standard reference, and the characters are measured using an optical comparator or microscope. Baselines are first established for the various types of characters (eg, the top and bottom line of caps, and the bottom line for lowercase descenders). Then, proceeding character by character, the end points of lines and the characteristics of ellipses or circles are determined. These dimensions are then converted into matrix numbers or dimensions. At this point, the data is ready to be entered into the computer, usually in character groupings with similar lines or shapes.

A flexible matrix allows the program to adapt to various resolution levels and to different printers.

The font generator program features a graphics screen display and help menu to prompt various functions. The screen display's advantage is that is depicts matrix ratios, dot sizes, and dot shapes correctly, thus allowing the character to be displayed in true perspective. A flexible matrix allows the program to adapt to various resolution levels and to different printers.

Varying the matrix density with a given dot size allows software developers to predetermine an optimum character matrix before the hardware is available to test it. Once sample characters have been generated, the screen image is photographed, reversed, and reduced to produce a very accurate approximation of the final character shape. This information can then be fed back into engineering to aid in specifying the necessary dot resolution.

Other features simplify and speed the character image development. Automatic generation of circles, ellipses, and lines improves the accuracy and consistency of frequently repeated shapes. Similarly, character shape and character file borrowing save time by reducing unnecessary replication of shapes, such as the circles for an "o" or "e," or characters, such as punctuation. Character viewing in context helps to visualize the interaction of characters in order to create, as stated before, a "beautiful group of characters" (Fig 5).

The final step in the font generation process is to translate the printer's character lookup table into a PROM format. With a single command, the program takes the raw X-Y dot data and generates a coded PROM image in hexadecimal format. The PROM programmer burns a PROM to be loaded into the printer, which can then print out the newly developed character set for review. Following that, the characters undergo final editing, thereby completing the font development process.

AMT engineers believe that the Office Printer has the level of print quality and versatility required for the executive office. An increase in magnitude has been achieved, but AMT engineers concede that they have yet to find a way to automate the process of subtle character refinement that differentiates between "a group of characters" and a "beautiful group of characters."

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CIRCLE 36

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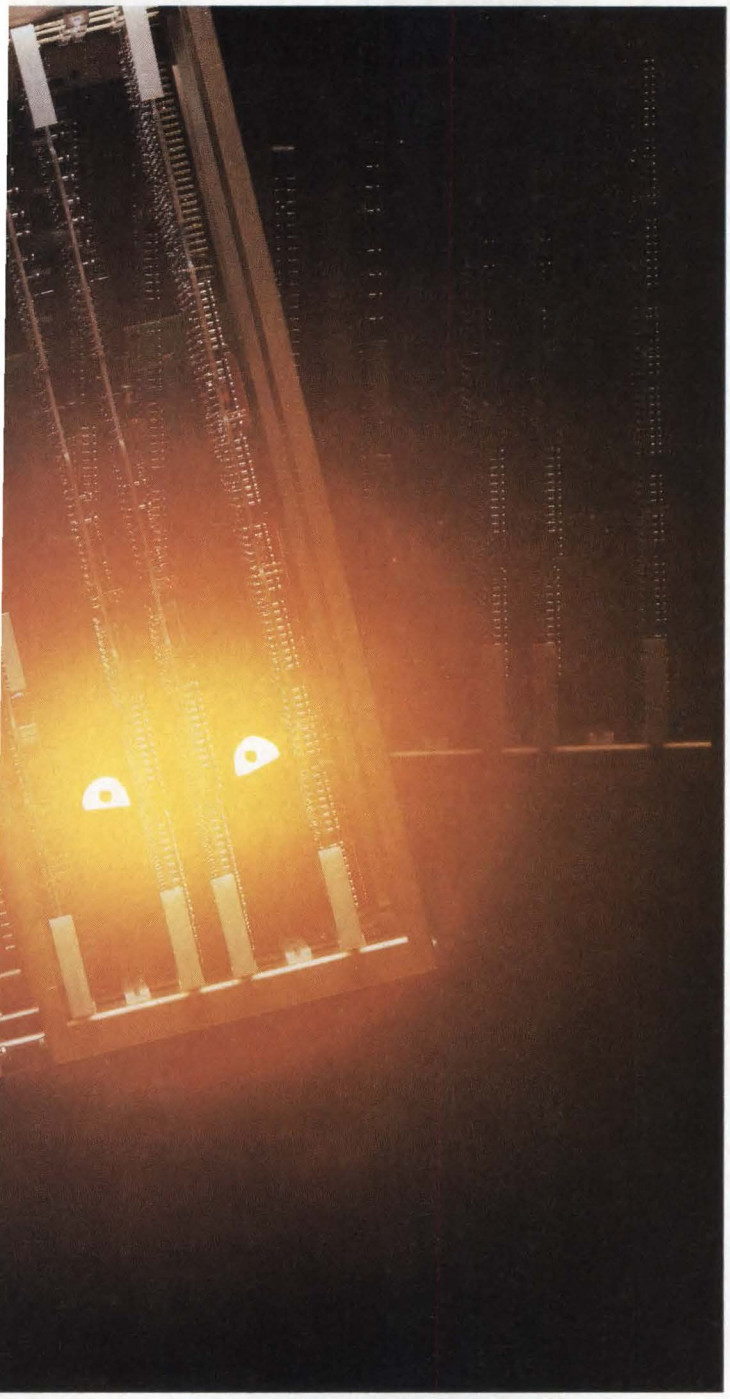

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CIRCLE 37

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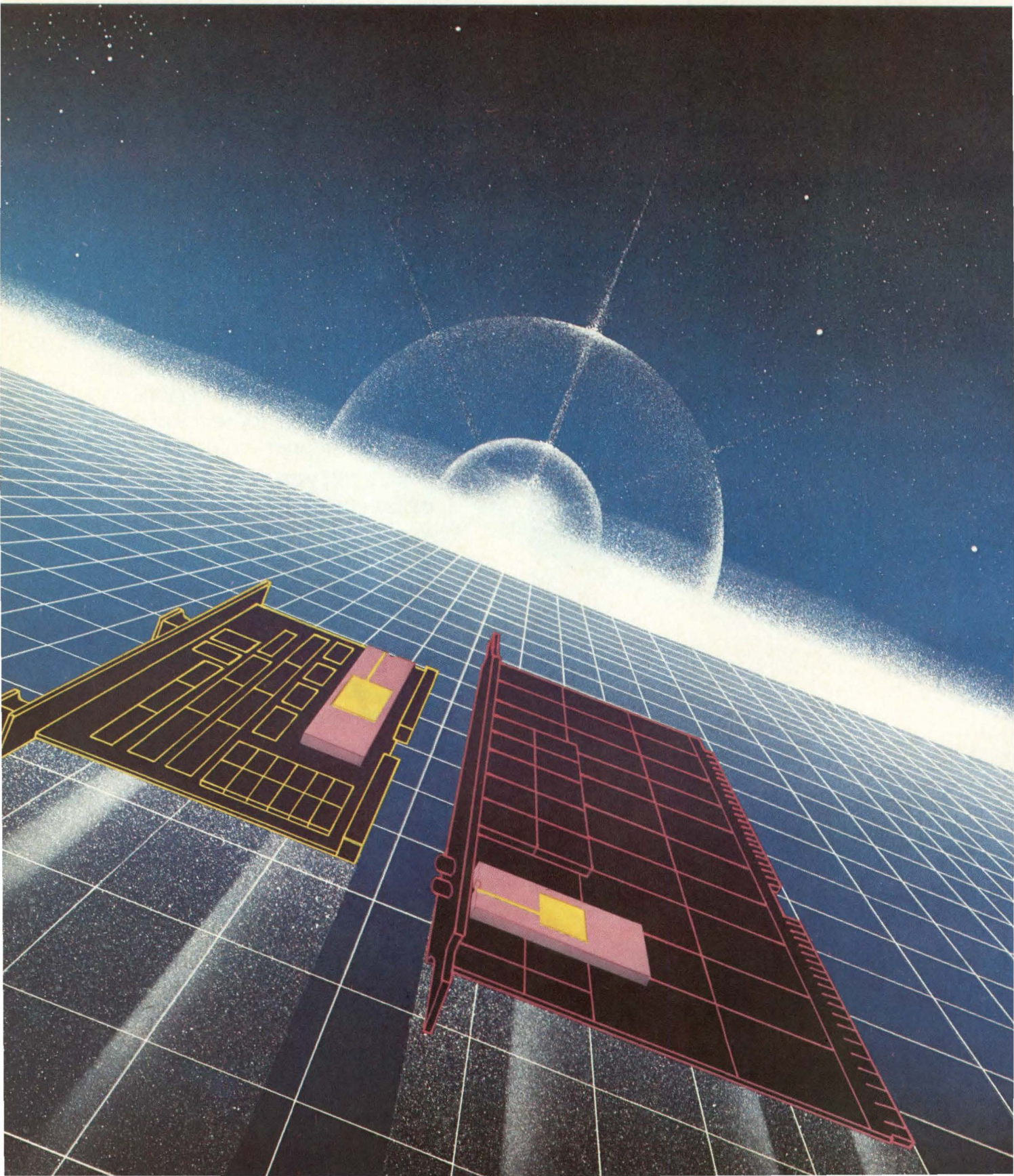

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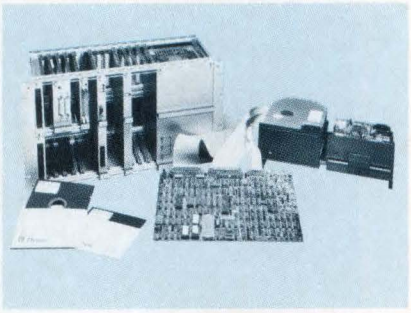

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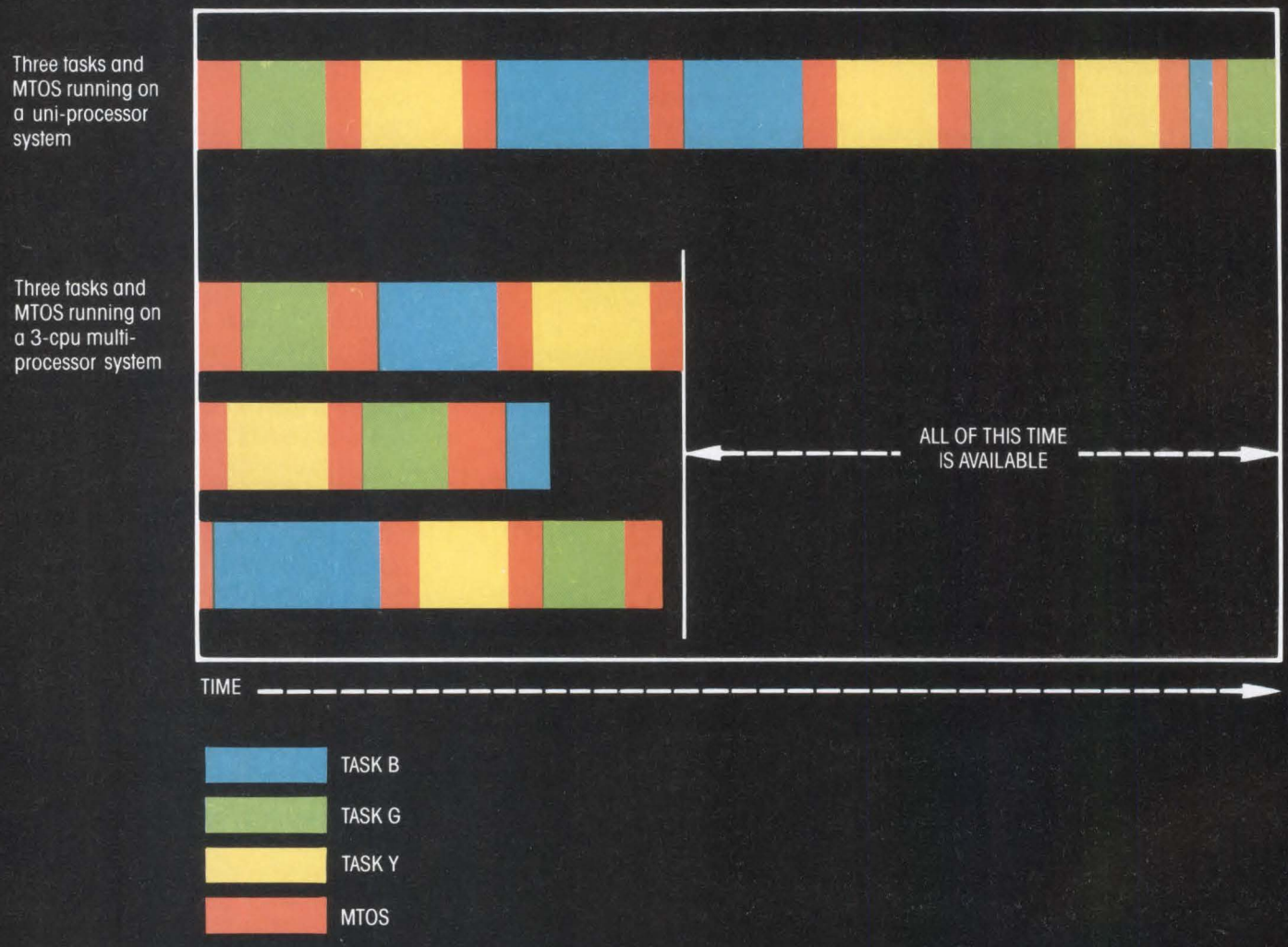

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CIRCLE 40

VAX EXECUTIVE DEVELOPS REALTIME APPLICATIONS

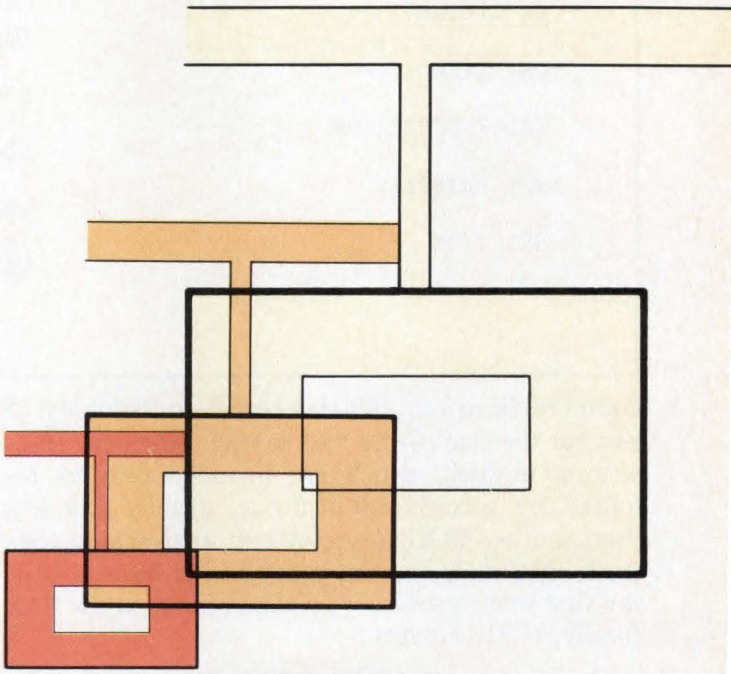
As a general purpose operating system, VMS is overkill for most dedicated applications. A new realtime executive simplifies MicroVAX support.

by Roger Heinen, Jr

Superior computational power and unconstrained memory addressing inherent in 32-bit computer architectures vastly extend realtime system capability. Yet, dedicated applications can only be cost-justified at system prices associated with microprocessors and low end minicomputers. However, the cost of a general purpose operating system and its hardware can be eliminated with a compact executive that fits comfortably on a microcomputer and effectively supports application execution in a realtime environment.

Regardless of processor power or the number of bits in a data word, developing realtime applications has traditionally been a complex procedure requiring expert programmers who are intimately familiar with the target computer, the assembly language, and the high level programming language. In addition, because most high level languages have not been designed to handle concurrent processes, the application has often had to include an operating system for scheduling and controlling execution. Application developers have also had to understand the operating system's inner workings.

When Digital Equipment Corp extended the role of its 32-bit VAX computer family more fully into dedicated realtime systems, the company took a different approach to system software development. Oriented to general purpose computing,



DEC's VAX/VMS operating system is, in a sense, "overkill" for dedicated realtime service on small computers. Consequently, VAXELN, an object-based realtime executive (kernel), was designed for small size and simplicity.

Simplicity was a primary consideration in order to encourage realtime application development by experts in different fields, rather than by computer programmers. Moreover, the conceptual structures of the executive software, the high level programming language, and application development are all simple in nature.

Thus, conceptual simplicity was the paramount design constraint for VAXELN, even if its inner workings were complex. The VAXELN kernel occupies only 20 Kbytes of main memory, which is

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VAXELN Objects and Procedures

Objects	Procedures (and objects they can act on)
DEVICE	ALLOCATE/FREE: MEMORY
EVENT	CREATE/DELETE: DEVICE, EVENT, JOB, MESSAGE
JOB	NAME, PORT, PROCESS, SEMAPHORE
MEMORY	CLEAR: EVENT
MESSAGE	CONNECT_CIRCUIT: PORT
NAME	DISCONNECT_CIRCUIT: PORT
PORT	ACCEPT_CIRCUIT: PORT
PROCESS	DISABLE/ENABLE: PROCESS
SEMAPHORE	EXIT: PROCESS
Utilities	SEND/RECEIVE: MESSAGE
GET_TIME	SIGNAL: DEVICE, EVENT, PORT, PROCESS, TIME
RAISE_EXCEPTION	SUSPEND/RESUME: PROCESS
SET_PRIORITY	TRANSLATE: NAME
SET_TIME	WAIT_ANY/WAIT_ALL: DEVICE, EVENT, PORT
	PROCESS, SEMAPHORE, TIME

comparable to the RSX-11M kernel and roughly 15 percent the size of the VMS kernel. Ancillary DEC-written utilities, which are included only as required by specific applications, usually add less than another 50 Kbytes to system software. In contrast, minimum main memory of the MicroVAX I, the first microprocessor-level computer in the VAX family, is 512 Kbytes.

Using a simple structure

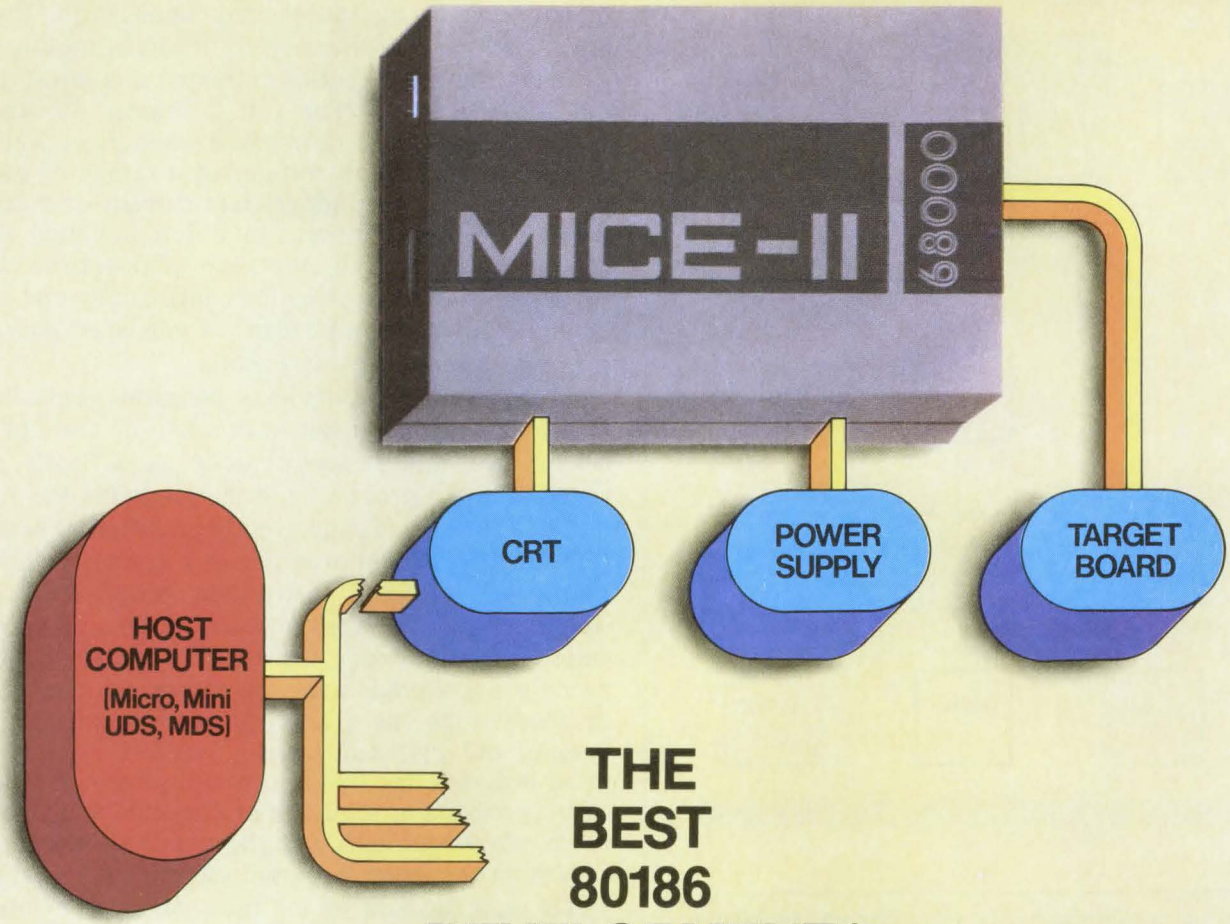
Managing hardware resources (chiefly main memory and CPU time) on behalf of application programs written by developers is a realtime executive's function. The finished software placed in the target system also includes DEC-written utility services and a runtime library of commonly executed subroutines. However, the kernel itself, in conjunction with the programming language, establishes the character and procedures of application development.

The realtime executive defines a small number of hardware or software resources (objects) and a small number of actions (procedures) that the system can perform in regard to those objects. Among the most commonly used objects are MEMORY, PROCESS, MESSAGE, and DEVICE. Among the most commonly used procedures are CREATE and DELETE, SEND and RECEIVE, and WAIT_ANY and WAIT_ALL.

The Table lists most of the objects, procedures, and utilities defined by VAXELN's kernel. Although there is at least one other commercially available realtime object-based system, VAXELN is the only such system to drastically limit the number of procedures and objects. Thinking in terms of what is needed by the application, the developer combines easy-to-use procedures and objects to accomplish whatever must be done (not all procedures apply to all objects).

In a realtime application, the system's response to external events is critical. The time consumed in allocating hardware and software resources, and in having these resources perform assigned functions, must be short enough not to affect the application's natural external behavior. To accomplish this, two factors are important: to do things as fast as possible; and to do things in a predictable amount of time.

Sometimes, these factors do not go hand in hand, as the fastest way is not always the most predictable. VAXELN's simple design makes it efficient: simple operations require small amounts of



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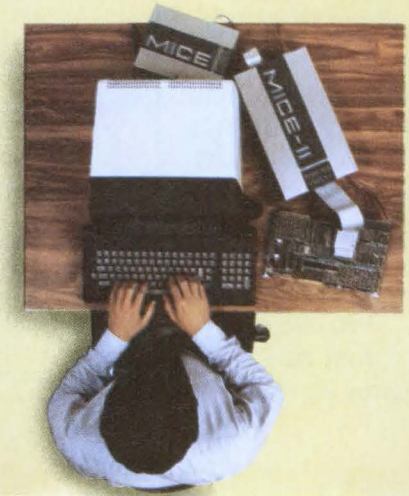

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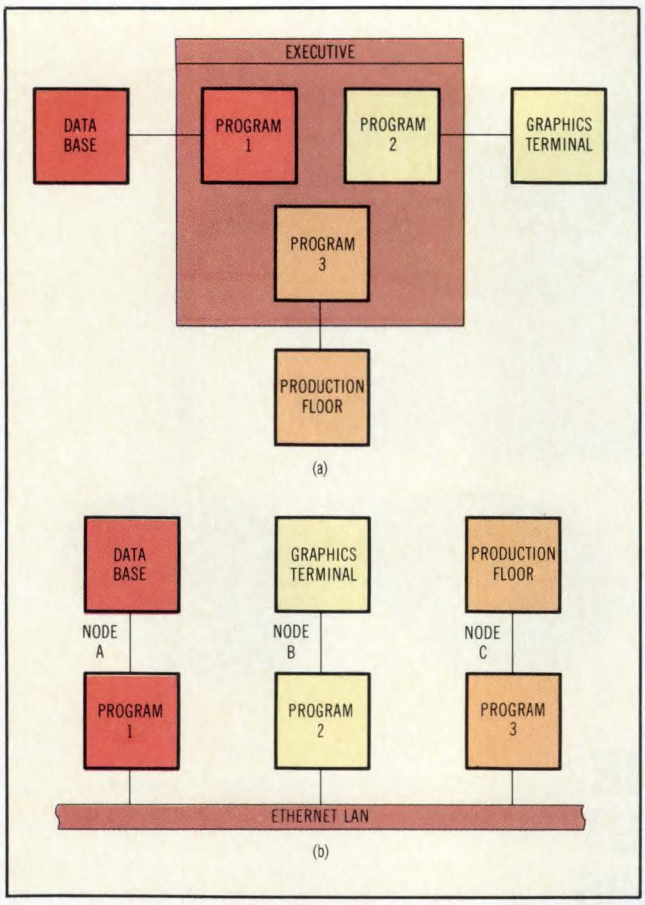

Fig 1 In multiprogramming, more than one application program (P1, P2, P3...Pn) can run on one processor (a). In multiprocessing, more than one application program under control of a single executive can run on two or more processors at different nodes in a LAN (b).

resources. Predictability is a product of careful implementation. The kernel, for example, can only request data space in small, fixed-size chunks. If more space is needed, it must make a second (and perhaps a third) request for another chunk. Since the time to allocate a chunk is fixed, this technique guarantees that context switches cannot be blocked for arbitrary lengths of time. In other systems such as VAX/VMS, the operating system takes the time to search for an available block of memory appropriate in size for the data. This is efficient in memory utilization but unpredictable in elapsed time.

A realtime environment

While individual functions described by objects and procedures may be performed efficiently, they cannot operate together effectively in a realtime system without concurrency. Concurrency operates at four levels in the realtime executive. These are the multiprogramming level, the multitasking level, the multiprocessing level, and the distributed processing level.

At the multiprogramming level, more than one application program (P1, P2, P3...Pn) can run on one processor [Fig 1(a)]. Each program can either handle a portion of one multiprogram application or can support an independent application. Programs exchange information by means of messages.

Each program execution is treated as a job at the multitasking level. (The job is created for that specific purpose and terminated when execution is completed.) Each job consists of a family of processes (one or more independent threads of execution). The initial process in a job is called the master process and all others are subprocesses. All processes in a job can execute concurrently and exchange information by means of messages, shared memory, semaphores, or events.

At the multiprocessing level, programs controlled by a single executive can run on two or more processors in a multiprocessor node. And finally, at the distributed processing level, programs P1, P2, and P3 can execute concurrently on different nodes [Fig 1(b)] in a local area network (LAN). In both multiprocessing and distributed processing, the developer does not need to know whether an application is to run on one processor, or more than one processor at a single node, or on processors at two or more nodes in a LAN. In a nonmultitasking system, the CPU sequentially executes the entire main program line by line. In multitasking, a part of the program or sequence of lines can be invoked to execute concurrently with the main code sequence.

A nonconcurrent program cannot do its work faster than the sum of the times taken to execute each part of the program, such as subroutines. In concurrent programming, the speed of the program is, in principle, the speed of the slowest thread of execution. While the slowest thread is waiting for various external events, such as I/O completions, other processes can use the CPU.

Fig 2 shows the relationship between jobs and processes in an executing VAXELN system. For example, the kernel creates startup program 1. That job's master process executes the code in main program block 1. Among other actions, the master process can call a CREATE_PROCESS

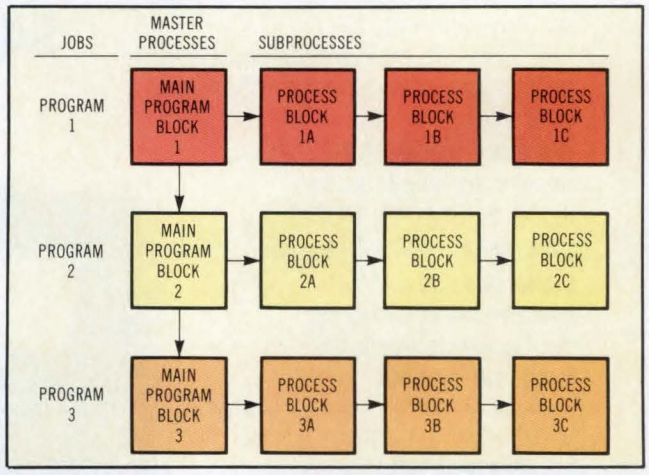

Fig 2 Jobs that execute application programs usually consist of a master process and one or more concurrently executing subprocesses.

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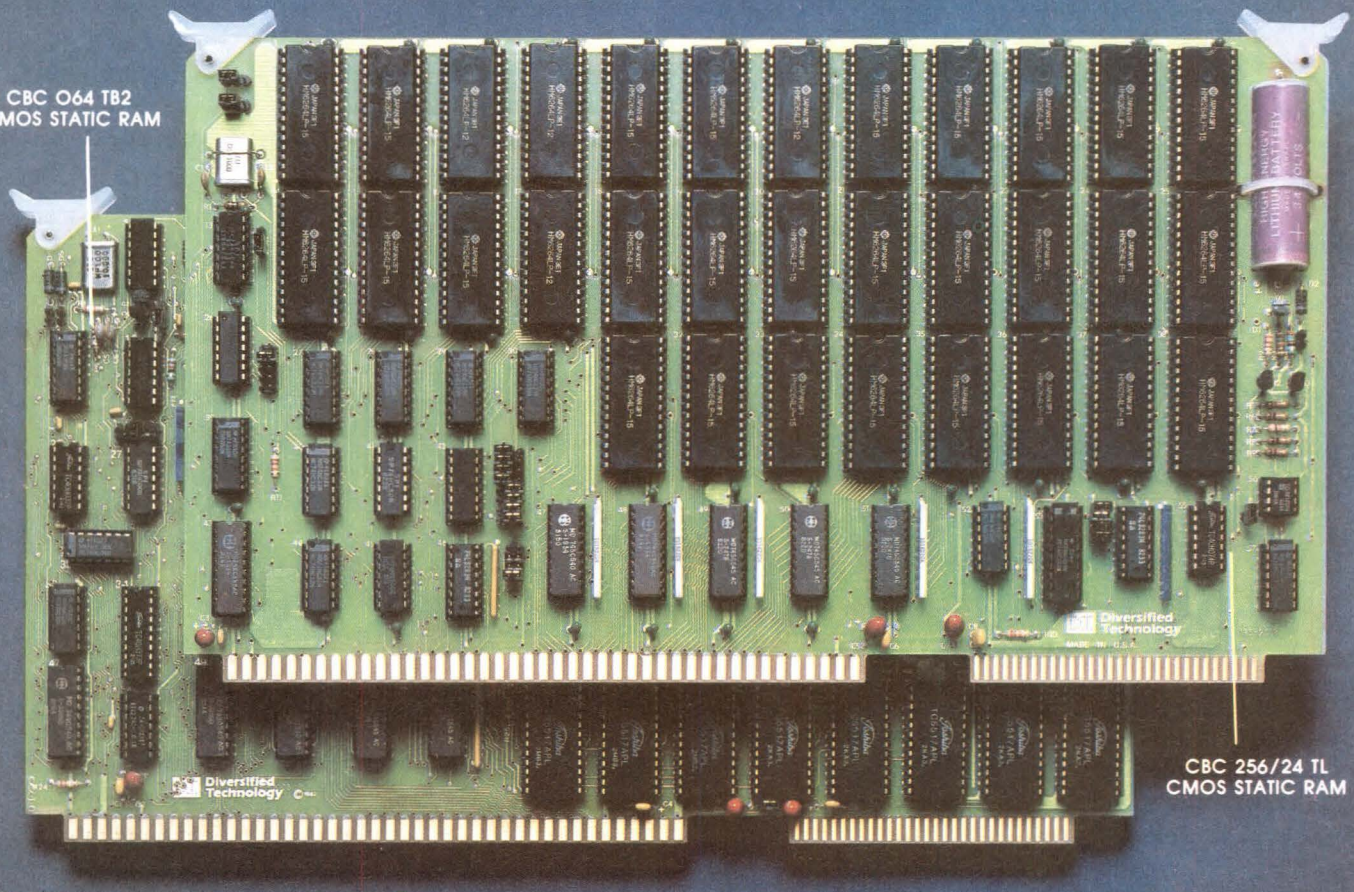

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procedure to initiate a subprocess that executes process block 1A. This process block might in turn initiate a second subprocess to execute process block 1B, and so forth.

Each subprocess is an independent thread of execution specifically created to execute its process block. It is deleted when the block terminates. Another subprocess can be created when the same process block is to be executed again. The kernel deletes the job when all code in main program block 1 has been executed. Meanwhile, execution of programs 2 and 3 can continue.

A transaction handling system, for example, typically involves a large number of I/O operations in accessing a data base. In that case, a transaction is defined as whatever must be done from the start of transaction to completion of the disk I/O. The sequence of VAXELN procedure/object steps for the master process of this job would be something like:

```
WAIT (JOB_PORT)   master {process  waits  for
      a  transaction  request}
RECEIVE  (JOB_PORT, MSG)  {receives a message
      containing  transaction data}
CREATE_PROCESS  (TRANSACTION,    MSG)    {executes
the process block that completes
the transaction concurrently}
UNTIL false;
```

The subprocess TRANSACTION, whose instructions are located in a process block isolated from the main application code, decodes the message and performs the specified disk I/O operation. In the meantime, one or more additional transactions may have been received, and other processes are concurrently executing the same block of code in performing transactions. Therefore, handling incoming transactions is specified by only a few lines of code in the master process. Without multitasking, the CPU would have to wait for completion of disk I/O on the first transaction before beginning to process a new transaction.

Process-to-process communication

A job's master process and subprocesses communicate by means of shared variables declared in the program. Because these processes execute concurrently, access to shared data must be synchronized by means of statements within the program and process blocks involved in that job.

On the other hand, VAXELN jobs (families of processes) can communicate only by means of messages. Messages have two inherent advantages. First, the programmer does not have to be overly concerned with synchronization. Second, the programs can be physically redistributed among processors at different nodes [Fig 1(b)] and still be able to communicate via messages as if they were running on the same processor (ie, without changing their communication code).

In VAXELN, messages from node to node are automatically encapsulated with protocols that provide reliable, sequential message transmission. The protocols are compatible with the DECnet architecture used by other DEC systems such as VAX/VMS. By using the DECnet Network Services Protocol (NSP), VAXELN systems can coexist with other DEC systems in the same network. An Ethernet provides the actual data transmission.

Each subprocess is an independent thread of execution specifically created to execute its process block.

Another DECnet protocol, Data Access Protocol (DAP), is used for all VAXELN Pascal file I/O functions and interaction with device drivers, even when the source and target are on the same node. By using this protocol, the program accessing the data is independent of the data location, whether it is local or remote. Of course, programmers can use their own simple protocols to exchange messages between cooperating processes.

Regardless of the process-to-process protocol used, developers write application programs to run on any processor in a LAN. If one or more programs are relocated to processors at other nodes, the network service software in that node handles message protocols, without requiring the attention of either the developer or user. The network service is supplied as a user program that can be included in any VAXELN system.

Two characteristics make programming message traffic within a single processor particularly easy. First, messages can be any length that the sending and receiving processes are capable of handling, whereas other systems have a maximum message length. And second, transfer time is low and predictable because message descriptors, not the messages themselves, are what actually pass between processes on the same node. (Because of variations in data path length, node-to-node transfer time for messages in a LAN is unpredictable.)

The VAXELN PORT object represents a system-maintained dedicated message queue. A port is automatically created when a job is created, whether or not executing its code requires sending or receiving messages (jobs that do not require any port are rare). If necessary, a given thread of execution will acquire more than one port. Each port in the network is uniquely identified by a 128-bit value—and may even be associated with a name—so that it is readily available to other jobs and processes at the same node or at different nodes.

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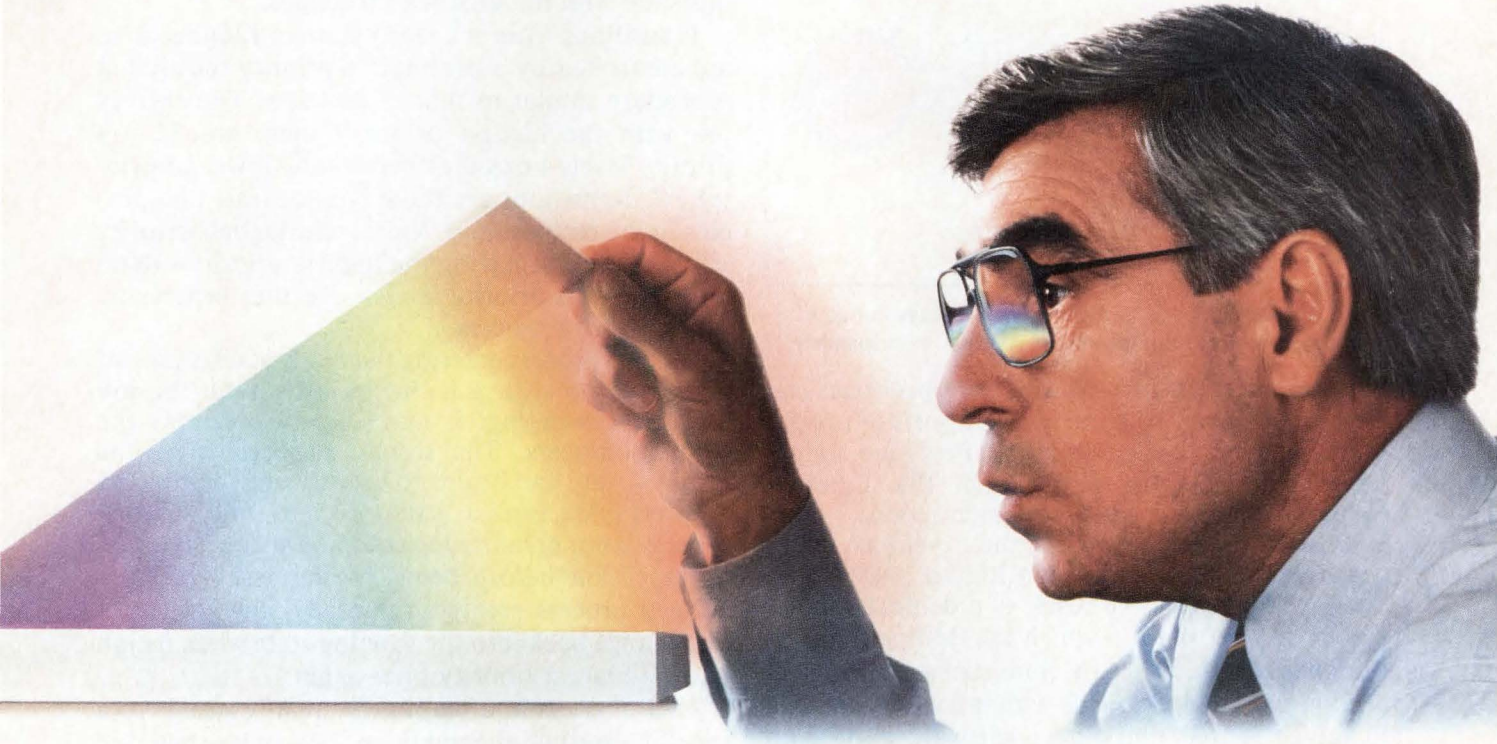

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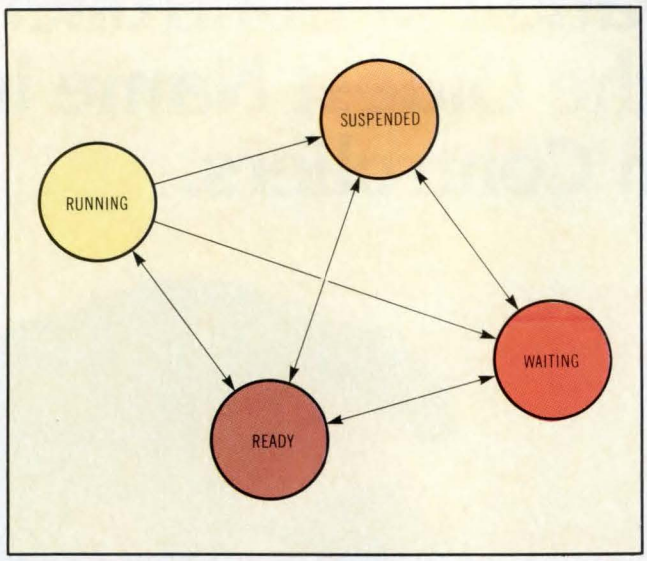

Fig 3 A master process or subprocess is always in one of four process states: running, ready, waiting, or suspended.

Communication between different processes can be set up by means of either generic ports or private circuits between dedicated ports. Ports are simply targets for messages and model the Ethernet semantics of message and port interaction.

To set up a private circuit, the developer writes special statements such as CREATE_PORT and ACCEPT_CIRCUIT. The result is a dedicated port-to-port transfer path in which the destination port is implicit. In addition to eliminating the need to specify target address fields with messages, another advantage is that the system software itself does more in handling private circuits: it informs the source process when there is a disconnection (a separate "end of transaction" message is unnecessary), guarantees message sequence and delivery, and provides some privacy by restricting access to the destination port.

Even though message and port objects and procedures are easy to use, programmers can apply standard Pascal I/O statements such as READ and WRITE to perform these low level functions. For instance, a circuit is established when a Pascal file is opened, and the file is a message stream connected to another process. In this case, the partner port/circuit acts as a file server, whether or not the data stream comes from a mass storage device.

Process states and scheduling

The master process and the subprocesses are always in one of four process states (Fig 3). In the running state, the process is in control of the CPU and executing. In the ready state, the initial state of every process immediately after its creation, the process is eligible to execute. The process is standing by for a specified set of conditions to be satisfied in the waiting state. It may be waiting for a particular amount of time to elapse, for the occurrence of a particular event, or for the receipt of a message. A process can put itself (and only itself) in this state by calling the WAIT_ALL or WAIT_ANY procedure. Finally, in the suspended state, the process is not eligible to execute (ie, cannot enter the ready state) until it is resumed explicitly. A process can put itself or any other process in the same job in the suspended state with the SUSPEND procedure. One process can remove another from this state with the RESUME procedure.

Transitions from the ready state to running state are controlled by a preemptive priority scheduling procedure similar to that in RSX-11M. The current job with the highest priority—there are 32 job priority levels—executes before any lower priority job. (Current jobs are those with at least one process in the ready state.) Within that highest priority job, the process having the highest priority—there are 16 process priority levels—executes before any lower priority process.

When a process entering the ready state is part of a second job with a higher priority than the job currently executing, it immediately preempts the running process. The second process enters the running state and begins to execute until completed or preempted (unlike VMS, the currently running process is not permitted to complete a time quantum of execution before being preempted). The preempted process reenters the ready state, where it can change back into the running state when its job has the highest priority once again.

Each process in a realtime system responds to a specific external phenomenon, and more than one phenomenon may require attention at any given time. The developer's first step is to see that each process, given control of the CPU, can handle its portion of the job's response in an acceptable amount of time. After that, the jobs and their processes must all be given high enough priorities to ensure that they can exercise this capability.

Synchronizing processes

Processes must be synchronized with other processes and with external phenomena. (It may be necessary to prevent two processes from occurring at the same time, as in controlling shared data accesses.) The WAIT_ANY and WAIT_ALL procedures (see the Table) provide means for processes to hold in the waiting state and to change to the ready state.

WAIT_ANY and WAIT_ALL act on the following objects, that define the processes for which they are waiting. The first object is an EVENT, a defined occurrence that can only take place at one point in time; the same occurrence at another time is another event. When an event is signaled, all processes waiting for it can enter the ready state. The second object is SEMAPHORE, a gate that controls access to one or more resources, such as shared memory. A binary semaphore protects only one

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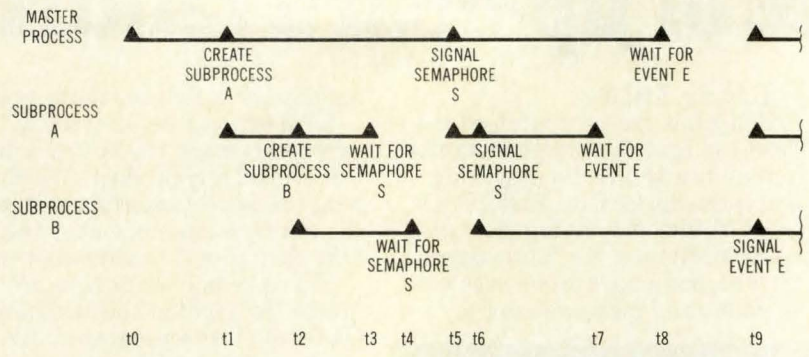

Fig 4 A master process and subprocesses A and B make use of semaphore A and event E to synchronize execution. (A solid horizontal line represents either the ready or running state.)

resource. When a process completes a memory access, it signals the semaphore so that another process can proceed with its memory access. A counting semaphore protects many similar resources and, when any one of them becomes free, the freeing process signals the semaphore and a waiting process is permitted access.

The next object is PORT, which is a message queue. A WAIT on a port is satisfied when a message is available. Another object, DEVICE, is a connection between a hardware interrupt and an interrupt service procedure. A WAIT on a device is satisfied when a connected interrupt service procedure executes. Finally, a PROCESS is a separate thread of execution. A WAIT on a process is satisfied when the process terminates.

WAIT_ANY provides for a process to change state from waiting to ready when any synchronizing object is signaled (up to four objects in a single WAIT_ANY). WAIT_ALL provides for a process to change state only when all specified conditions have been signaled. A time-out feature forces the process to the ready state if the waiting conditions have not been met before a specified time.

Binary semaphores are efficient, easy-to-use locking mechanisms. RSX-11M and VMS programming, in which semaphores are unavailable, requires two event signals to lock a resource (open door to let one process in, close door to keep other processes out). A semaphore, like a revolving door, opens and closes in one operation.

Fig 4 shows how a master process and subprocesses A and B use semaphore S and event E in synchronizing execution. After beginning execution at time t0, the master process creates subprocess A at t1 and continues in either the ready or running states. Among other things, the master process signals semaphore A and later goes in the waiting state for event E.

Meanwhile, subprocess A has created subprocess B at t2 and has gone into a waiting state at t3. When the master process signals semaphore S at t5, subprocess A begins to run again and itself signals semaphore S at t6 to bring subprocess B from the waiting to the ready and running states. When subprocess B signals event E at t9, both the master process and subprocess A go into the ready state. When all three processes complete, the job is terminated.

Selecting a high level language

A high level programming language, which effectively handles all realtime software elements, including device drivers, simplifies application development. The language has to be readily compatible with the executive software's procedure/object structure.

The recently introduced VAXELN executive software supports realtime applications in a variety of environments: single processors, symmetrical multiprocessors, and distributed systems in Ethernet LANs. Although distributed realtime systems appear complex, VAXELN's conceptual structure is such that developing a distributed system—eg, for a factory, bank, or warehouse—is essentially the same as developing a single embedded microcontroller.

Originally designed as a teaching language, standard Pascal (as defined by ISO/TC-97/sc5-678, Nov 4, 1981) has become the language of choice in many university-level computer science courses. Standard Pascal, however, was not developed as a system programming language and is relatively difficult to use at the bit level, which is necessary in controlling external devices and writing device drivers.

VAXELN Pascal, a minimal extension of standard Pascal, is the high level programming language used for VAXELN applications. To enhance user software productivity, standard Pascal was selected because it is a widely accepted structured programming language. Given the right set of enhancements and a carefully planned system, Pascal can be used effectively in all areas of the system without the performance penalty associated with general purpose programming languages. VAXELN applications can be completely programmed in Pascal, effectively eliminating the need for

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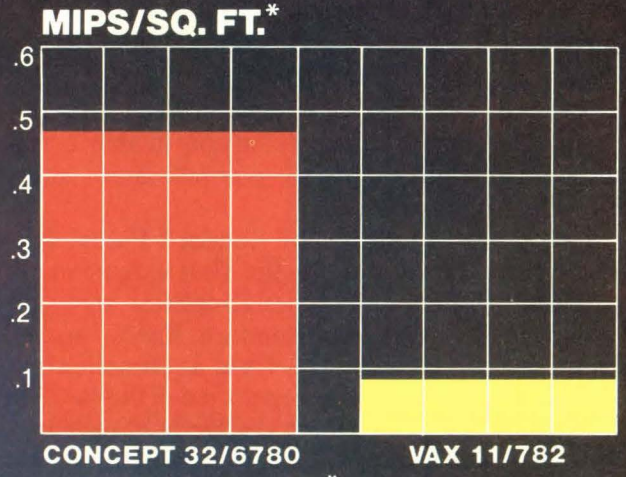

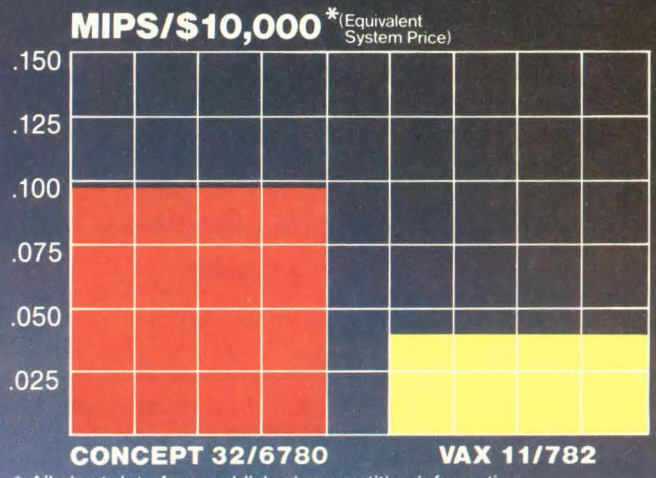

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assembly language routines. Application development is done on a larger VAX computer running the full VMS operating system.

Although Pascal was the overwhelming choice of the DEC users interviewed, Fortran, C, Modula, and Ada were among the high level languages considered. Modula, Nicholas Wirth's own realtime extension of standard Pascal, is not yet well known outside the academic world, but provided VAXELN Pascal (or EPascal) with the concept of concurrent Pascal for multiprocessing. Ada, a structured language very much like Pascal, is somewhat complex, but might well have been selected for VAXELN if its development had been further along.

EPascal strengthens standard Pascal as a realtime language. Extensions are minimal to keep EPascal as simple as possible and to avoid incompatibilities with present and future standard Pascal. EPascal is a true extension in that a standard Pascal program will compile and execute without modification.

Two major extensions of standard Pascal relate to its basic data types. In the first extension, the availability of flexible types simplifies array and record coding. While a standard Pascal array is statically defined (its size is fixed at compile time), the extent of a developer-specified EPascal array need not be specified until that array is actually used, and that extent need not be known at compile time. In standard Pascal, for example, an array data type might be defined as

```
TYPE MATRIX
     =ARRAY [1....10, 1....10]
     OF INTEGER;

In EPascal, the definition would instead be

TYPE MATRIX  (M, N:INTEGER)
     =ARRAY [1....M, 1....N]
     OF INTEGER;
```

The values of M and N are not established until the type is used. For example,

```
VAR
   mat23:  MATRIX (2,3);
```

Flexible types are used in VAXELN Pascal to provide basic string functions without the need to add any other special types. For instance, the PL/I varying string type is built into VAXELN Pascal as

```
TYPE varying_string (n: INTEGER) =
  PACKED RECORD
     length : 1..32767;
     text : PACKED ARRAY [1..n]
          OF CHAR;
     END;
```

The second major extension to standard Pascal types involved adding VAXELN objects as basic data types. Programming is simplified because, among other things, the developer need not repeatedly consider the detail of calling the executive. For example,

```
VAR msg : message;     {msg variable is of type message}
    p : ^ integer;     {p points to an integer}
CREATE_MESSAGE(msg,p);
```

This statement assigns a value to the message variable msg and places the address of the data part of that message in the pointer p. The program can then put the data to be sent in the part of the message addressed by the pointer, and the message can be transmitted with SEND(msg).

EPascal's simplicity is apparent when the developer handles interrupts. With many realtime executives, device drivers must be written in assembler and added to the kernel to synchronize hardware interrupts. With EPascal, the device driver is written as part of the application program in only a few lines of this form.

```
{attach interrupt service to a hardware interrupt}
    CREATE_DEVICE('DISK',
            device_variable,
            interrupt_service_procedure);
    .
    .
    .
{wait for hardware interrupt and interrupt
     service execution}
     WAIT_ANY(device_variable);
```

CREATE_DEVICE establishes a connection between an external hardware interrupt (indicating occurrence of an external stimulus) and an interrupt service procedure. The EPascal statements in the interrupt service procedure begin running one machine instruction after a hardware interrupt. If the interrupt service needs to signal the device driver process, it uses the SIGNAL_DEVICE kernel procedure. WAIT holds the currently running process in the waiting state, and SIGNAL_DEVICE returns the current process to the ready state (where it can change again to the running state) when the interrupt service procedure ends.

Considering application development

Application development has also been simplified, primarily in the process of creating source code for application programs, and in debugging. The VAXELN Pascal compiler has been extended to provide separate compilation (ie, developers can create and compile source code in separate modules). This is useful in planning and sharing development among several programmers, both in

writing and modifying application code and in debugging the target system.

In separate compilation, the source code modules are individually compiled and filed in a work library. As each module is compiled, declarations or cross references involving it and the modules already in a program library are automatically checked for consistency. The EPascal compiler also provides for a one-time definition of declarations that covers all uses of the declared item in other modules. The compiler detects inconsistencies in declarations and usage and reports them to the developer. Without one-time definition, declarations must be redefined in each module, and mismatched declarations can be very troublesome. In effect, these features extend Pascal type checking to separately compiled modules.

A program builder then combines the modules to produce an executable image of each program. An interactive system builder provides the system image (Fig 5) by combining executable program images (P1, P2, and P3) with other software elements: VAXELN kernel, runtime library, and whatever DEC-written ancillary software services and standard device drivers are needed in the application.

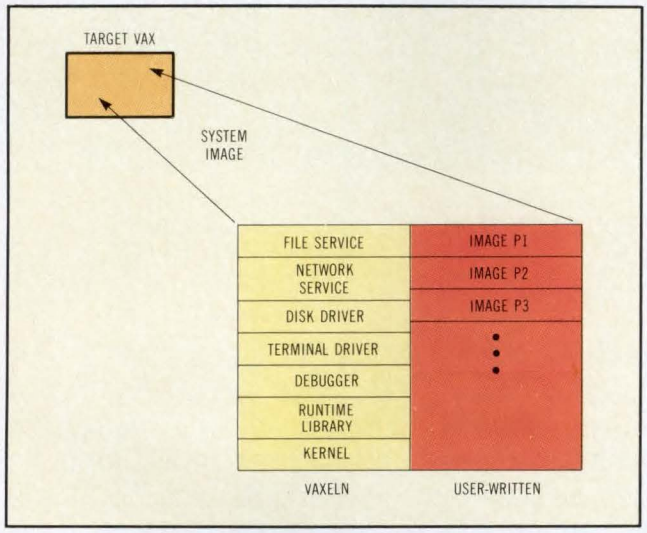

Fig 5 The system image created by the system builder consists of developer-written program images and DEC-written VAXELN kernel and ancillary software.

The ancillary software includes file service, network service, disk driver, terminal driver, and debugger (network service handles interjob communication among different nodes in a LAN). To minimize the size of a system image, the runtime library is both modular and shareable. The system image contains only one copy each of only those routines needed by the system's programs.

The system image, developed under the VMS operating system running on a VAX host computer, is then loaded onto the target VAX computer. The image can either be placed on a disk and bootstrapped onto the target, or downline loaded from the host to the target at a node in an Ethernet LAN (Fig 6). Once the system image has been transferred to the target computer, VAXELN provides for either local or remote debugging. If the target configuration includes a console terminal [Fig 6(a)], the onboard version of the debugging software can be run locally. If not, as in many embedded standalone realtime applications, debugging is done remotely from the host [Fig 6(b)], with only a small debug nucleus on the target.

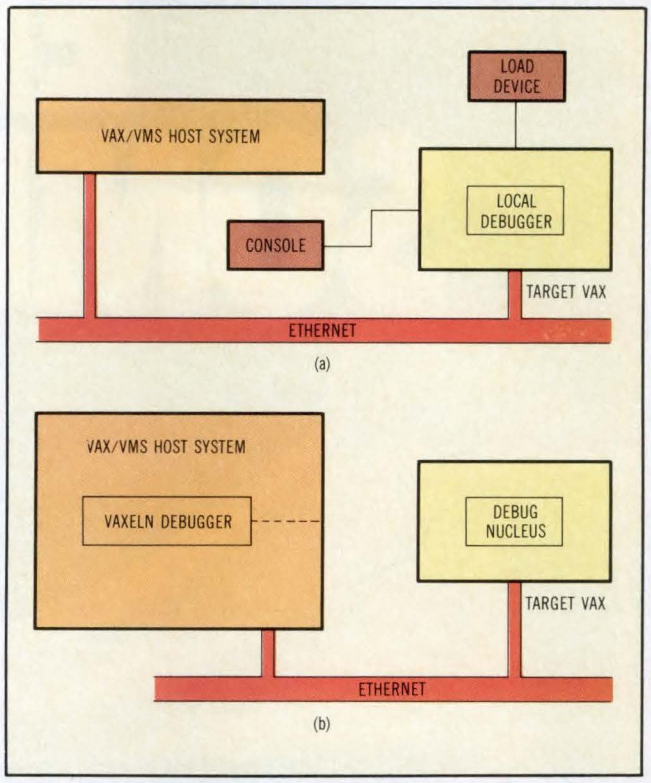

Fig 6 The target system can be debugged remotely from a VAX host running the VMS operating system (a) or locally from a console on the target VAX (b).

The same debug command language is used in testing and examining all levels of system software. All processes (threads of execution) on all nodes in a VAXELN network can be debugged from one terminal. During a debug session, the debugger provides symbolic access to variables, as well as access to the program source code, machine instructions, and hardware registers.

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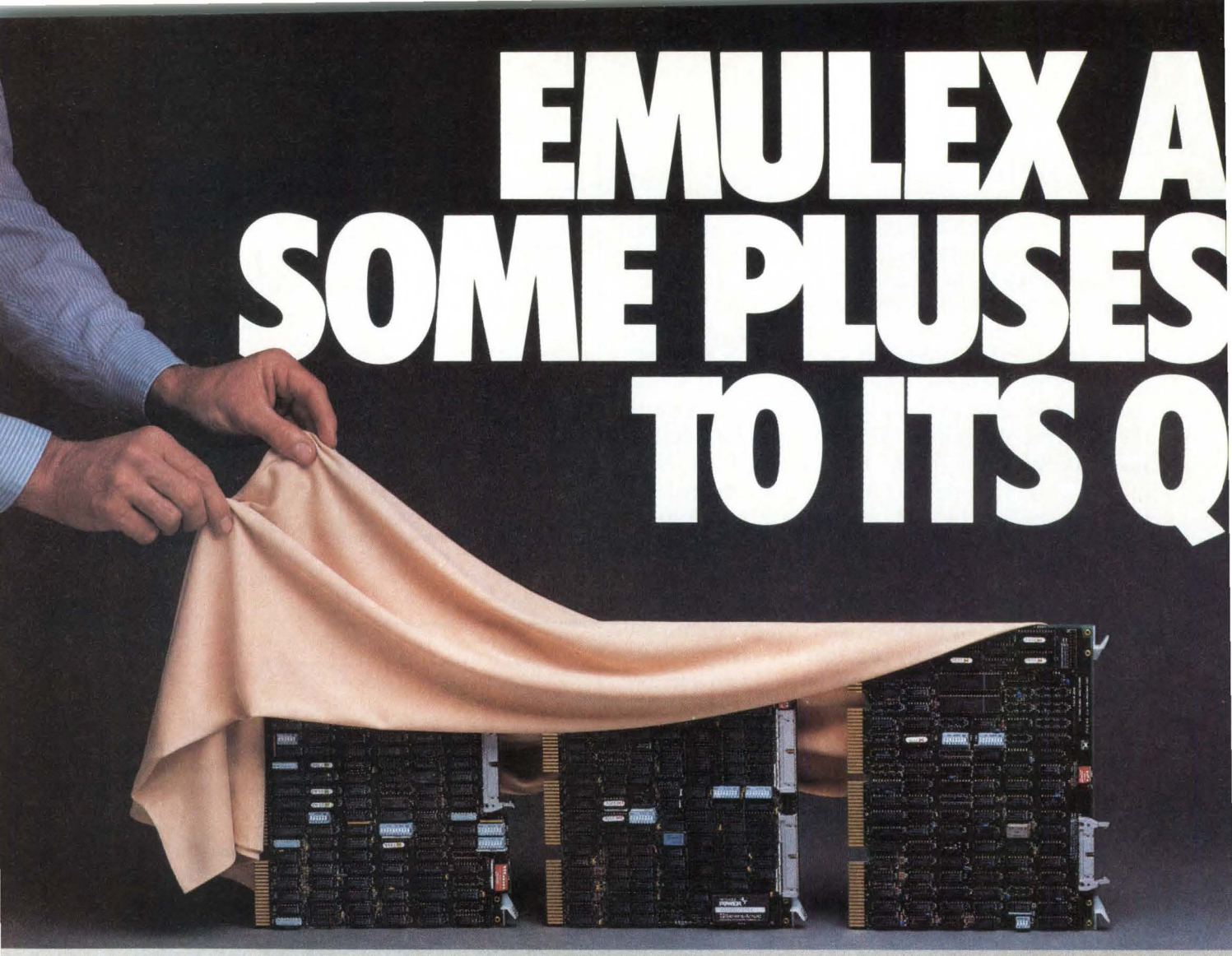

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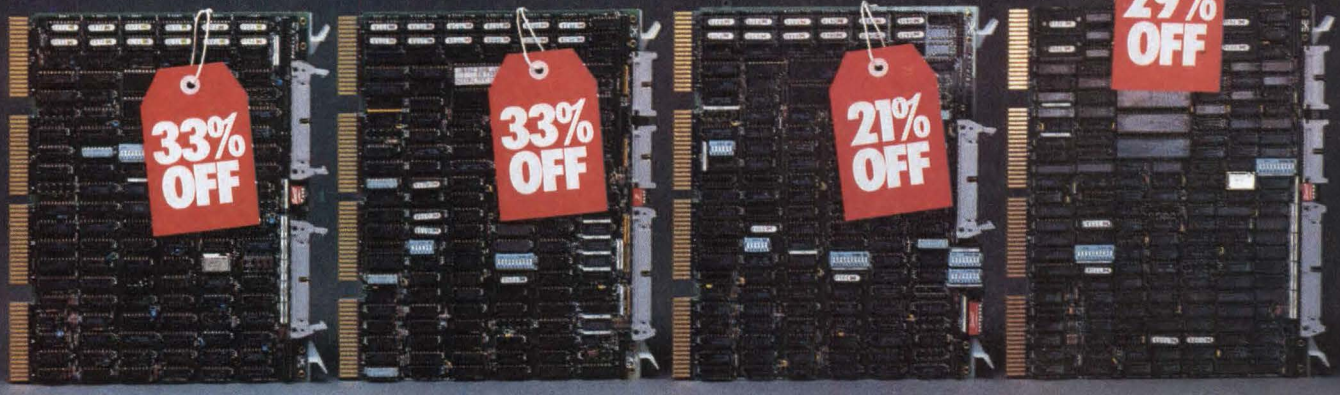

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CIRCLE 47

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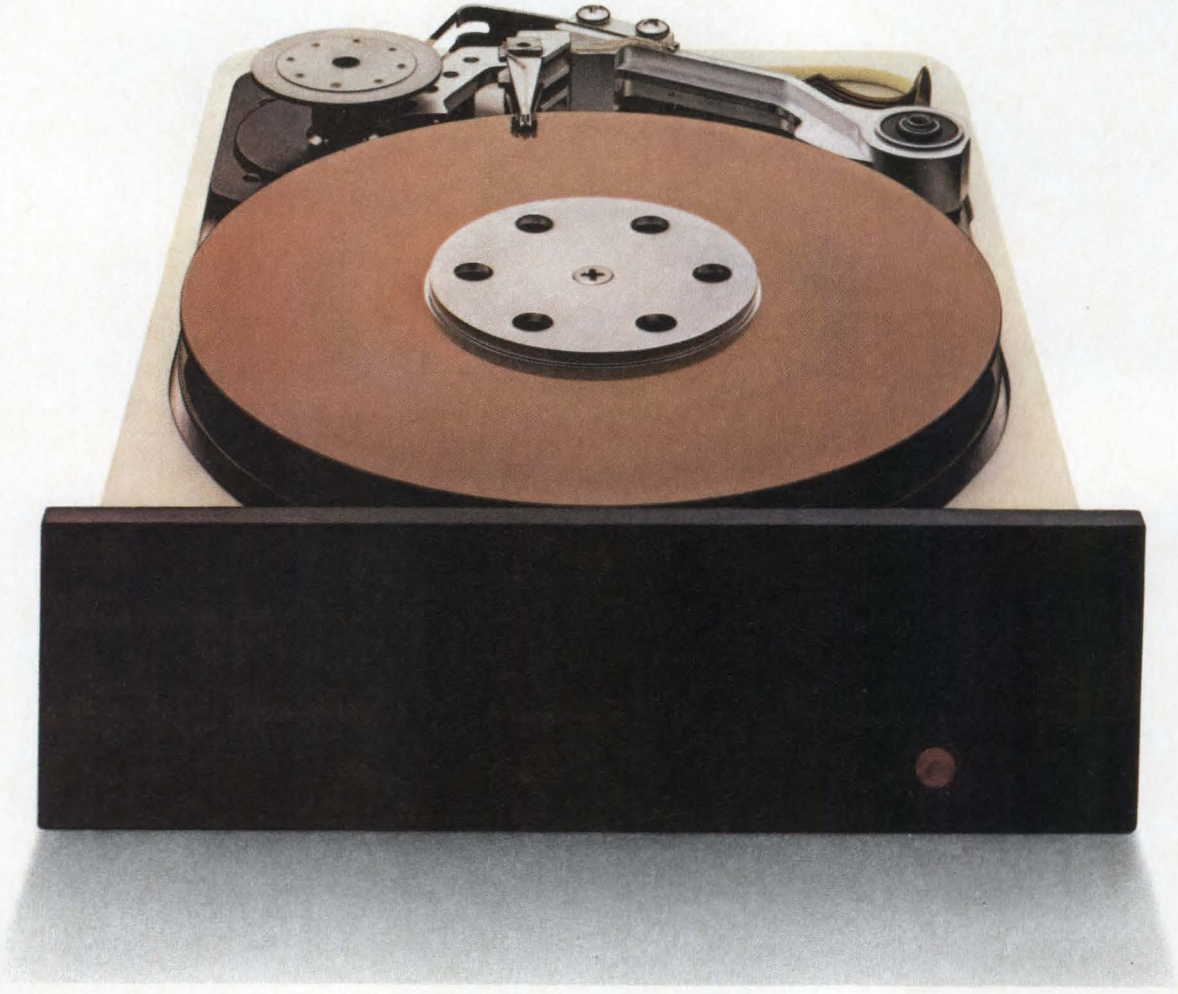

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CIRCLE 52

MULTIBUS CACHE PROMOTES PROCESSOR INDEPENDENCE

Using cache memory for microprocessors is an alternative way to increase throughput without adding higher speed memories.

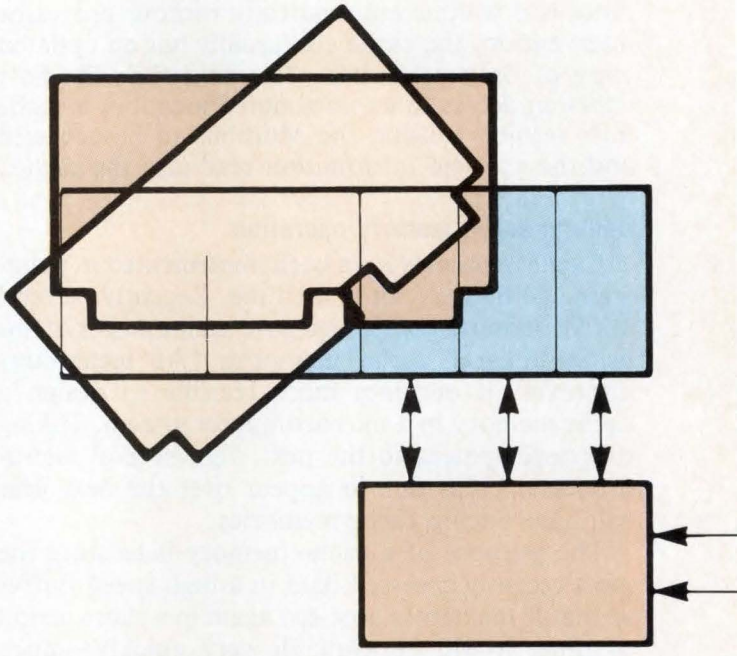
by Jeffrey Roloff

As system processor speeds increase, it becomes more and more difficult to use the memory available on a commercial bus without inserting many wait states. To solve this problem, Intel Corp developed the iLBX bus, a high speed, memory-only bus that is an extension placed on the P2 connector of the Multibus. With this bus, the processor has a high speed port into the system memory, allowing access with considerably fewer wait states compared to the Multibus system bus.

Unfortunately, a system's complexity grows substantially when iLBX memory boards are added to it because the boards are dual ported. This dual-ported architecture causes problems not only in the system's architecture, but also in the software for multiprocessor systems. Central Data's solution to these problems is to provide high speed memory on the iLBX bus. This cache memory is arranged so that it images the entire Multibus memory (16 Mbytes) using a two-set least recently used (LRU) caching algorithm (Fig 1). The cache memory also stores 2-K words (16-bit) of the most recently used memory accesses.

It has been proven that program execution tends to be localized. This often causes recently used memory accesses to be referenced again in a short period of time. The cache memory provides access to such refetched data in under 100 ns, much faster than any dynamic RAM board could operate.

Naturally, the cache does not have a 100 percent hit rate (the ratio of memory accesses that are found on the cache board/total memory accesses). Assuming a cache hit rate of 80 to 90 percent (as expected for this board), and a Multibus memory access time of 500 ns, the average access time for read cycles is (.85 × 100 ns) + (.15 × 500 ns) = 160 ns. Therefore, the average access time of the cache memory is less than half of the access time for currently available iLBX dynamic memory boards.



Because of the cache architecture, a write-through algorithm is used. This means that writes from the host processor to the iLBX are written not only to the cache memory, but also to the Multibus. Therefore, writes to memory operate at the Multibus memory rate, and there is no improvement in speed for such accesses.

The cache memory continually monitors and buffers into first in, first out (FIFO) all write operations that other masters on the system send to the Multibus. Since these writes mean that an old copy of data could be stored on the cache, control

Jeffrey Roloff is president of Central Data Corp, 1602 Newton Dr, Champaign, IL 61821. Mr Roloff holds an associate's degree in electrical engineering technology from Parkland College.

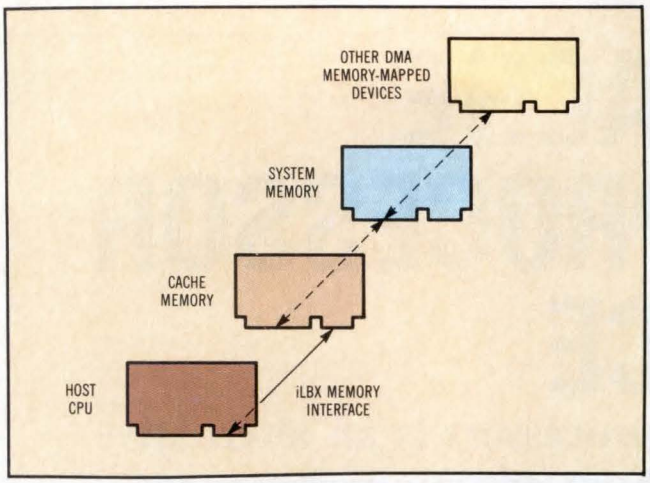


Fig 1 The cache memory is the host's gateway into the Multibus memory addressing space.

circuitry on the board invalidates any cache locations that have been updated on the Multibus. Since this is done automatically without processor intervention, the cache continually has an updated copy of only valid data. The next time the host starts an access to an invalidated location, a cache miss results, causing the Multibus to be accessed and the updated information read into the cache.

General cache memory operation

Cache memories have been implemented in mainframe computers for some time. Recently, several microcomputer companies have announced systems using integral cache memories. As technology improves, it becomes more feasible to design a cache memory in a microcomputer system. Taking this development to the next step, several microprocessor chips due to appear over the next year will have onchip cache memories.

The purpose of a cache memory is to store the most recently accessed data in a high speed buffer so that if the data is accessed again in a short period of time, it will be available very quickly—much more quickly than if a normal access route is taken. The cache memory itself is broken into two areas: the data area, which stores the actual data being referenced; and the tag area, which stores the address for the data. The cache memory described here has two sets of memory areas, each 1 Kword long. This makes the total size of the cache 2 Kwords, or 4 Kbytes.

The cache operates in the read mode by using the lower address lines to access the data/tag memory. The output of the tag memory is then compared to the upper address bits. If they are equal, there is a hit. This means that the memory address being referenced is in the cache. If the data in the tag memory does not equal the upper address bits, then a miss occurs, meaning that the cache location contains data from another area of memory. When a hit occurs, the data memory is transferred immediately to the iLBX bus, where the processor can read it. Since memory devices used are very fast (45 ns or faster), total data access time is under 100 ns.

In the case of a miss cycle, the cache board accesses the Multibus. The address previously specified on the iLBX bus is read and the data is stored into the cache. The data is then passed to the processor for its use. If that location is accessed again before the cache location is overwritten, it will be immediately available, with a hit cycle.

Write cycles, as mentioned earlier, write the data not only to the cache memory but also to the Multibus so that the Multibus memory always has current data. If this step is not done, and the cache is always updated while the Multibus is updated only when a cache location is cleared, other processors on the bus would not have current data written by this processor.

To control the cache's operation, three additional memory bits are used. Two of the bits indicate whether the corresponding sets of cache data are valid. These bits are initialized to the false state and are automatically switched on and off as needed by the cache during its operation. The last bit indicates which of the two sets of data has been least recently accessed. This information is used in the replacement algorithm. It determines which set should be overwritten when new data is placed into the cache.

Two major factors affect cache performance: the size of the cache (the one described here is 4 Kbytes), and the number of sets a cache contains. Today, many cache memories designed for microcomputer systems use only one set, with no LRU algorithm needed. After a certain size is achieved, there are diminishing returns for adding additional memory. Further, adding two sets instead of one causes dramatic increase in the cache hit rate. For these reasons, the chosen size of the cache and the number of sets are 4 Kbytes and 2, respectively.

Technology advances make it more feasible to design cache memory in microcomputer systems.

One factor significantly complicating the design of the cache memory is the need to monitor the Multibus for any writes made by other masters on the bus. This is needed in order to guarantee that valid data remains in the cache. For example, if a location in the cache happened to be in the area of a disk buffer, and the disk controller was doing a DMA operation into that buffer, the cache must be informed that its data is no longer valid. Otherwise, the processor will never see the data that was put in memory.

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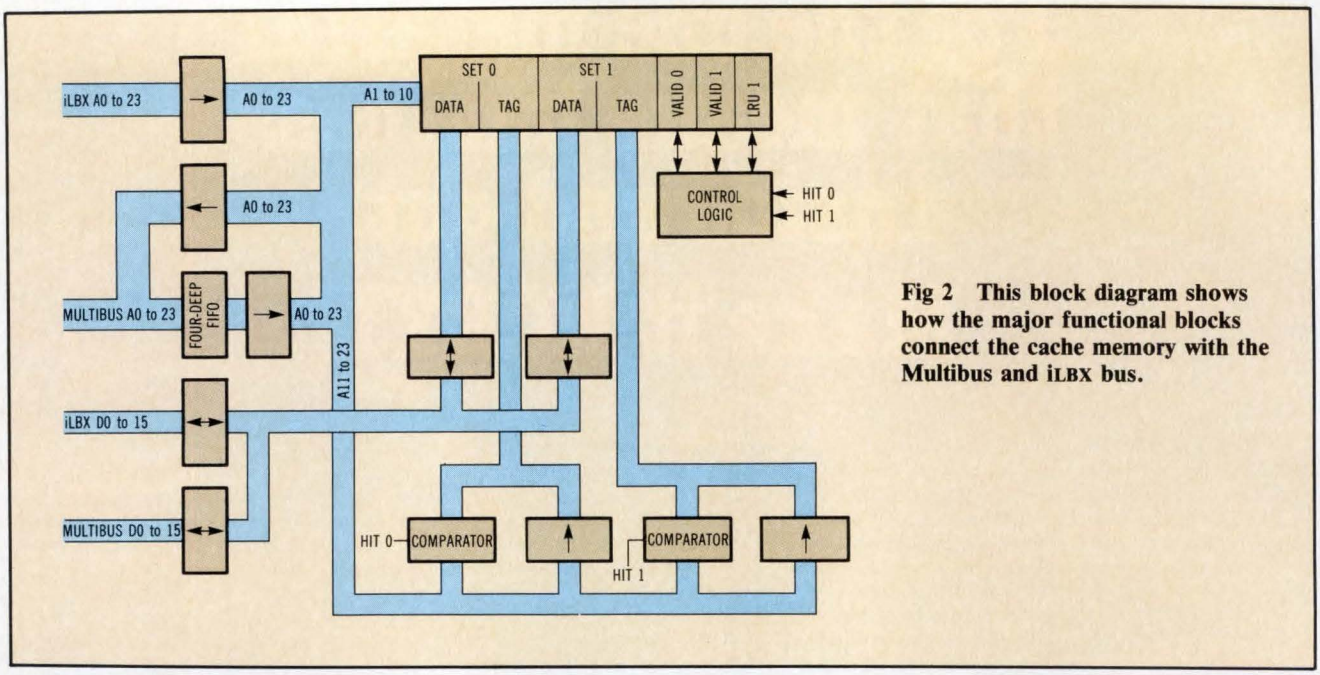

Fig 2 This block diagram shows how the major functional blocks connect the cache memory with the Multibus and iLBX bus.

the cache between each iLBX cycle. In this way, any cache locations overwritten on the Multibus are invalidated (by clearing the valid bit in the memory) so that any future access to the location will force a miss. This guarantees that the processor will always receive the most current data available.

Cache memory organization

Fig 2 illustrates the block diagram for the cache memory. As shown, the address bus for the board is split into two sections: lower addresses (A1 to A10) that are used to access specific memory locations and upper addresses that are used in a comparison operation to the memory tag bits. Buffers are provided for upper address bits so that the tag memory can be overwritten when a cache location is updated. If a miss occurs, buffers are provided to drive the Multibus address lines (after proper arbitration). This allows the Multibus to be accessed correctly. A four-deep FIFO is also provided to buffer the addresses of memory writes done on the bus by other bus masters.

The data section uses four bidirectional buffers, allowing data to be transferred from either cache set to the iLBX or from the iLBX to the Multibus. This feature allows the complete flexibility needed for both hit and miss cycles. Finally, the control logic on the board accesses the three additional RAM bits that determine which cache sets are valid and which cache set is least recently used. The control logic also monitors the outputs of the two comparators (the HIT lines) to determine if a hit/miss cycle is being performed.

A read cycle starts when the host processor makes its addresses available on the iLBX bus. These addresses are latched by the board and immediately start the cache operation. After the access time of the cache tag memories and the delay for the comparator occur, the HIT 0/HIT 1 signals are valid. If either set had a hit, the data is gated directly to the iLBX data buffers for presentation to the host processor.

If a miss occurs, the control logic requests the Multibus system bus. When it is obtained, the addresses from the iLBX are sent directly to the system bus and a 16-bit read is performed. This data is then made available to the iLBX data buffers and is also used to overwrite one set of the cache memory. The LRU1 bit determines which set is overwritten. If this bit is set, SET 1 is overwritten, since it was the least recently used. Conversely, if this bit is cleared, SET 0 is overwritten. Note that the Multibus performs a 16-bit read, regardless of whether the miss was an 8- or a 16-bit operation. This is done because the cache is accessed only in 16-bit increments, and a full word is needed to update a cache set. The iLBX is always presented with 16 bits of data; it will take the proper half in an 8-bit operation.

When a write occurs to the cache, more complicated control procedures must be implemented. To accomplish this, four possible write operations are each handled differently on the board. The first, an 8-bit write hit operation, cannot be implemented by the board since the board is set up to handle only 16-bit data. Therefore, the set that has hit is made invalid because only 8 bits cannot be updated, and the 8-bit data is written to the Multibus. With the second operation, the 8-bit write miss, the board again can only handle 16-bit data, thus the write is simply performed directly to the Multibus. In this case, however, neither set of cache data contains this memory address, so neither set needs to be invalidated.

The third operation, the 16-bit write hit, causes the data to be written to the cache hit set as well as

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CIRCLE 54

Cache Memory		
	Input	Output
b0	Double hit error	Cache on
b1	Valid bit error	Test on
b2	Parity error	Write on
b3	Overrun error	Not used
b4	Time-out error	LED 1
b5	Not used	LED 2
b6	Not used	LED 4
b7	Not used	LED 8

I/O port definition: the I/O port assigned to the board (accessible)

to the Multibus. Finally, the 16-bit write miss causes the cache to determine which set should be overwritten (just like a read miss), and also causes the data to be written to the Multibus. As described, all write operations cause data to be written directly to the Multibus, and 16-bit write operations also cause data to be stored into the cache.

Multibus "cleaning" operation details

The board contains an iLBX 24-bit FIFO buffer that is written each time a Multibus write occurs from another master. Between each iLBX cycle, this FIFO is examined for any new addresses. If there are any, the board's control logic checks to see whether the address causes a hit on the board for either set. If either set has a hit, that set is invalidated, forcing the board to access the Multibus the next time that address is read.

Cache memories without this "cleaning" feature can cause a significant software burden. They require the host software to determine areas of memory that should bypass the cache, and do so accordingly. This cache, however, is designed to be totally transparent to the host and requires no host intervention after operation has begun.

Setting a flag on the board can disable the automatic cleaning operation. This feature can be useful if it is known that no cache locations will ever be overwritten by bus accesses. The board then stops monitoring the Multibus for writes.

One feature not previously discussed for the cache, and new to this cache architecture, is the forced miss map. This map breaks memory into 1024 pieces, each 16-Kbytes long. There is a bit in the map for each block, indicating whether the cache should operate for that block or not. This allows the cache to bypass areas of dual-ported memory on the system bus. Such memory areas can be contained on other processor boards (where the Multibus is not written), although the memory may be updated by the onboard processor. The map forces a miss cycle for any access to such a location, thus causing all read/write cycles to such locations to be performed directly on the Multibus.

Since such memory locations are known at system start-up, this map can be initialized by the bootstrap PROM (at the same time the cache memory is tested and initialized), and does not need to be accessed by the host after that. Alternately, this forced miss map can be used in lieu of the automatic cleaning operation. This does, however, require that the host know exact physical addresses where data blocks that are common to two masters will reside on the bus. For this, the host overhead may be substantial. Most users prefer to use the automatic cleaning since it does not require host software effort.

Diagnostic features of the board

All of the board's memory can be tested using the iLBX interface before the cache is put into operation. This can be done by setting the output flag TEST ON (see the Table). As recommended, a complete memory test should be done on the cache when the system is powered up. Also, after the diagnostic is done, the cache must be initialized so that the valid bits are all cleared. The memory map for the iLBX interface during test mode is shown in Fig 3. Any accesses in test mode that are outside the range shown are routed directly to the Multibus.

The cache data and tag areas all contain parity checking circuitry. This circuitry ensures that the board is not the weakest link in the system's chain. Without parity, it would be assumed that no error detection would be necessary for 85 percent of the accesses to system memory. This seems like a very poor assumption considering today's fault tolerant system environment. Any parity error causes the cache to be shut down and all accesses to be routed directly through the Multibus. In addition, an interrupt can be generated on such an event.

If both comparators for the cache show that both banks have hit data (a double hit error), the cache is also shut down. This problem should never occur, due to the operation of the board's control

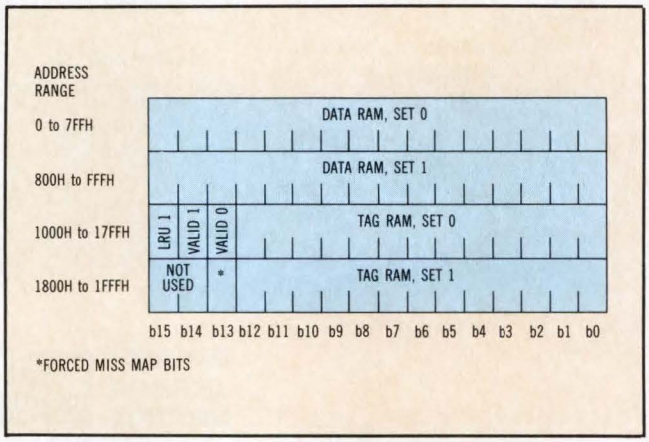

Fig 3 When the board is in test mode, all of the cache memory is accessible. This allows testing of the board as well as a setup to the proper state before start-up.

logic. The procedure is simply another way of preventing the cache's continued operation upon a known fault.

The cache provides a general purpose, processor-independent, high speed memory for Multibus-based computers.

Another type of hardware error that the board flags is a VALID bit error. If a hit is found in one set of the cache using the VALID bit for the set and the tag comparator (but a later operation finds the same VALID bit to be cleared), a hardware error occurred. Finally, if the FIFO for Multibus writes overflow, or if a Multibus access causes a time-out, the cache is also shut down. This occurs because the cache data is considered invalid at that point since a write occurred to the bus that the board did not catch in the first case, or an unexpected event occurred on the Multibus in the second case. It should be noted that the FIFO is designed to work in the fastest possible Multibus environments (with 200-ns Multibus cycle times), and never to lose any accesses. However, this is one more fault tolerant device that prevents problems from a bad board.

It should also be noted that all types of fault occurrences shut down the cache in such a way that the host will not see any bad data. When the error condition is detected, the current cycle is forced directly to the Multibus—as are all future cycles—until the cache is turned back on.

Four LEDs are provided on the board's top to indicate error conditions. These LEDs can be written by the host to indicate any cache fault to the user. This is often done when the system is initialized to give a general working/not working status to any technician debugging the system.

The cache memory board described provides a general purpose, processor-independent, high speed memory for Multibus-based computers. The host processor simply accesses the iLBX interface for all memory accesses, and the cache memory does the rest. Any needed accesses to the Multibus are done automatically by the board, making it invisible to the host. In times when processor speeds are ever-increasing, the cache memory board provides, with a minimum amount of effort, a reasonable alternative to adding many very fast (and expensive) memory boards to a system.

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CIRCLE 56

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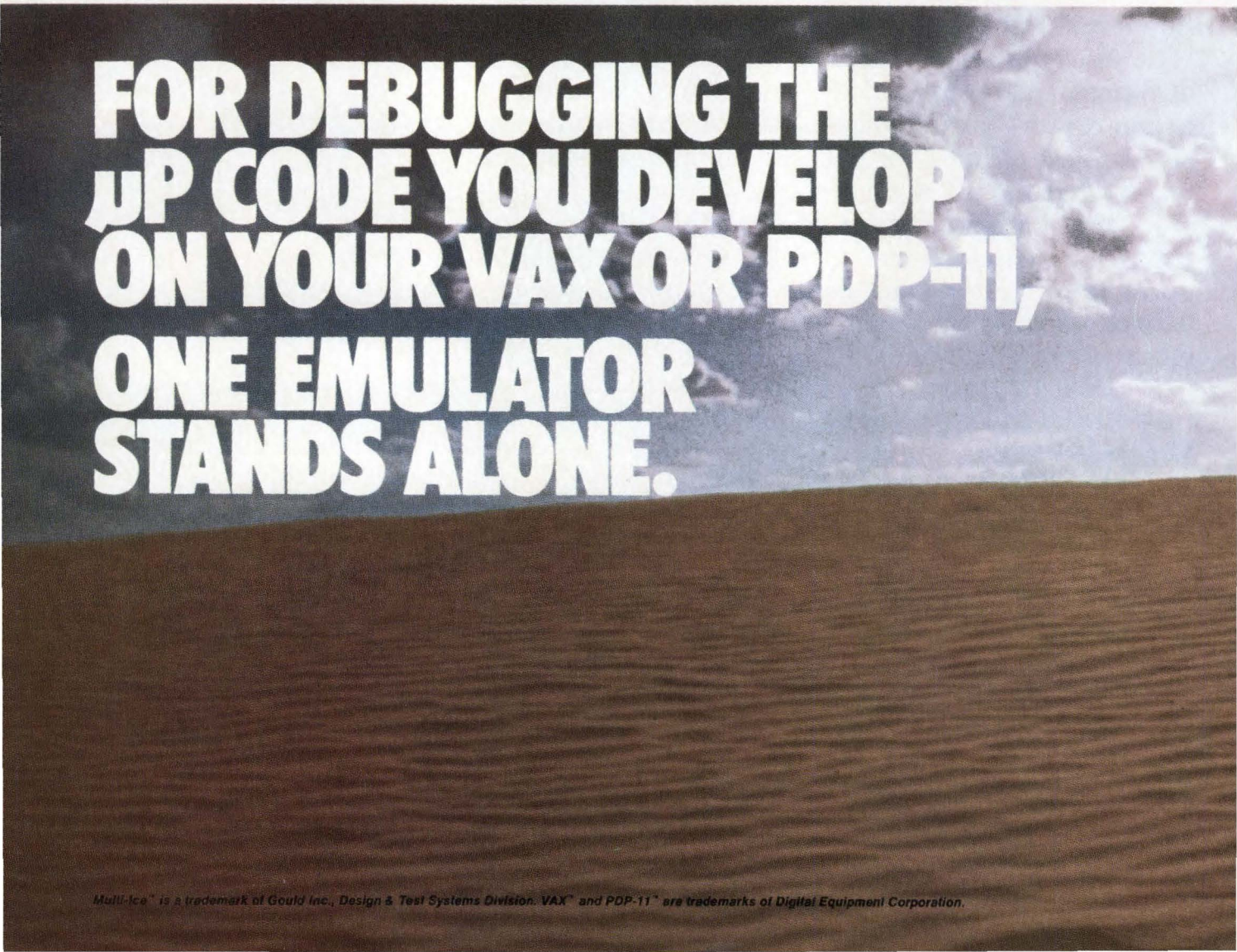

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CIRCLE 57

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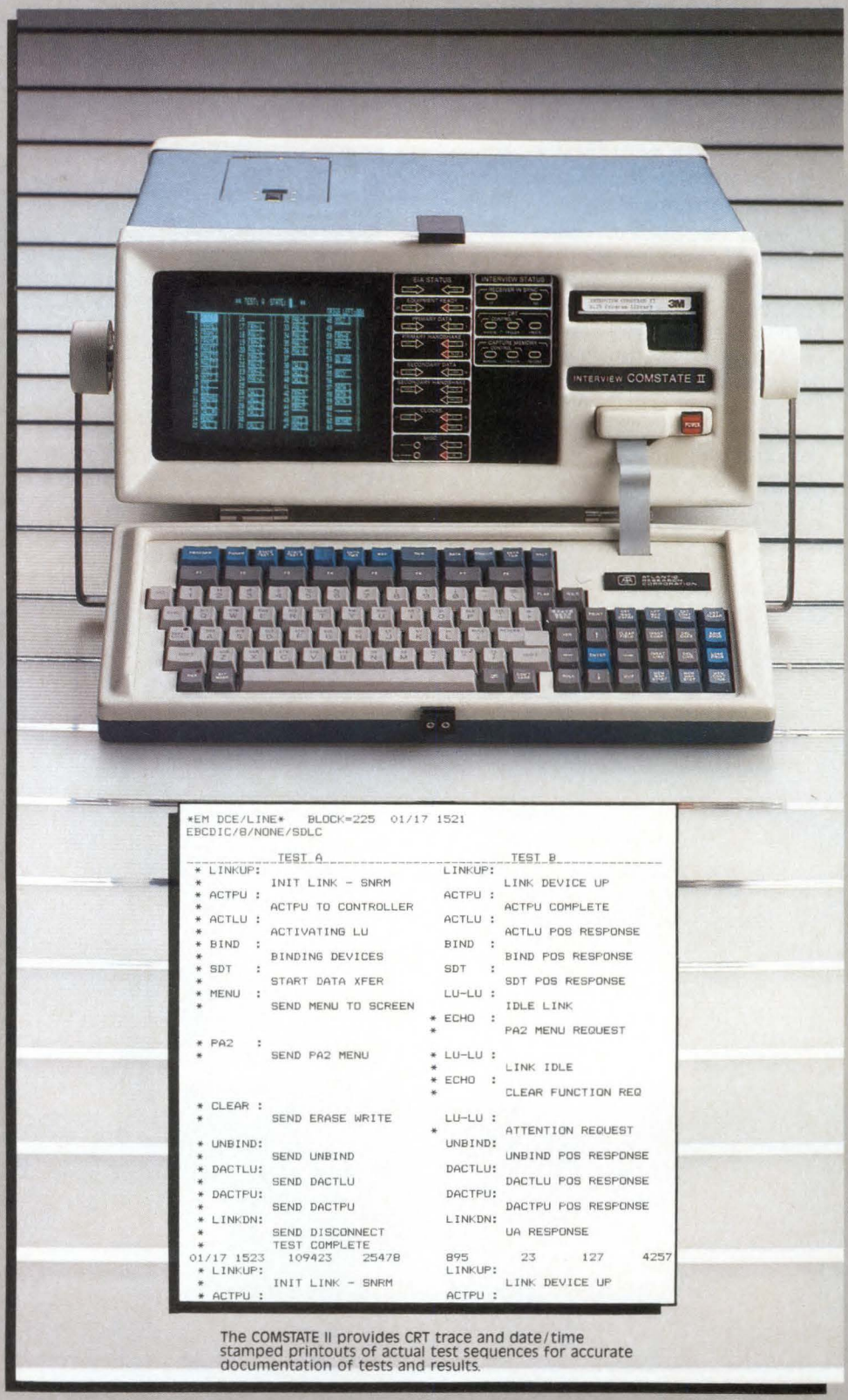


```
*EM DCE/LINE*    BLOCK=225  01/17 1521
EBCDIC/8/NONE/SDLC

                TEST A                                  TEST B
 * LINKUP:                                  LINKUP:
 *          INIT LINK - SNRM                           LINK DEVICE UP
 * ACTPU :                                  ACTPU :
 *          ACTPU TO CONTROLLER                        ACTPU COMPLETE
 * ACTLU :                                  ACTLU :
 *          ACTIVATING LU                              ACTLU POS RESPONSE
 * BIND   :                                 BIND   :
 *          BINDING DEVICES                            BIND POS RESPONSE
 * SDT    :                                 SDT    :
 *          START DATA XFER                            SDT POS RESPONSE
 * MENU   :                                 LU-LU  :
 *          SEND MENU TO SCREEN                        IDLE LINK
                                          * ECHO   :
                                          *          PA2 MENU REQUEST
 * PA2    :
 *          SEND PA2 MENU                  * LU-LU  :
                                          *          LINK IDLE
                                          * ECHO   :
                                          *          CLEAR FUNCTION REQ
 * CLEAR  :
 *          SEND ERASE WRITE               LU-LU  :
                                          *          ATTENTION REQUEST
 * UNBIND:                                  UNBIND:
 *          SEND UNBIND                                UNBIND POS RESPONSE
 * DACTLU:                                  DACTLU:
 *          SEND DACTLU                                DACTLU POS RESPONSE
 * DACTPU:                                  DACTPU:
 *          SEND DACTPU                                DACTPU POS RESPONSE
 * LINKDN:                                  LINKDN:
 *          SEND DISCONNECT                            UA RESPONSE
 *          TEST COMPLETE
01/17 1523   109423     25478       895        23        127       4257
 * LINKUP:                                  LINKUP:
 *          INIT LINK - SNRM                           LINK DEVICE UP
 * ACTPU :                                  ACTPU :
```

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CIRCLE 58

COMNET: A CUSTOM PBX/LAN DESIGN

A private branch exchange network furnishes universal access to a variety of computer resources.

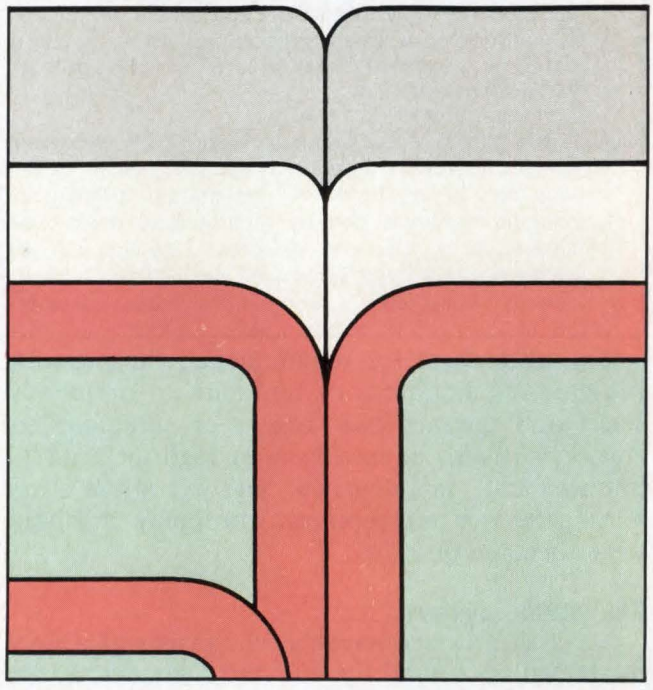
by Albert J. D'Arcy

Choosing an appropriate local area network requires an intuitive knowledge of the particular applications and careful consideration of the suitability of the networking medium. Factors such as network capability, reliability, and productive lifetime must be considered by every potential end user. In addition, the potential for growth should not be underestimated.

Currently, local area networks (LANs) are touted in publications as constantly "emerging": emerging standards, emerging technologies, and emerging schemes. In this context, "emerging" implies a product that is not yet ready to be marketed. In certain applications, some end users are well served by these emerging LAN technologies and techniques, which provide a comprehensive turnkey system capability.

However, most available turnkey systems are not general purpose. A system that is wholly applicable to office automation requirements does not adapt well to a process control environment, and vice versa. Although some LAN end users are well served by these systems, others require a network dedicated to more general purpose applications. One such network is General Electric's Communication Network (COMNET).

Albert J. D'Arcy is currently supervising engineer for computer-based hardware support and development at General Electric, Re-entry Systems Operations, 3198 Chestnut St, Philadelphia, PA 19101. COMNET is a phase of the computer aided engineering development effort directed by Dr John Schina, manager of the operation's computational systems design group.



Many factors were considered before COMNET's design was committed and developed by Re-entry Systems Operations (RSO), a branch of GE's Space Div. These factors required careful deliberation because aerospace applications for computer resources cover a broad range. Computer aided engineering resources, computer aided office resources, engineering analysis, process control, and data entry and retrieval in support of laboratory and shop requirements are essential to aerospace applications, many of which are interactive. Thus, user throughput on the network must not be affected by the number of users contending for service. The communication network must be field-proven and reliable, as well as general purpose, easily implemented, and immediately useful.

Gandalf speeds data communication

Many key COMNET subsystems are from Gandalf Data Inc, a major supplier of central networking nodes for port contention since the early 1970s. The Gandalf PACX IV is an intelligent circuit switch based on a high speed, bit-oriented, time-division multiplexing technique. A special high speed microprocessor controls all the PACX switching, connecting, and disconnecting.

In COMNET's dual version of the PACX IV, up to 512 attached devices can contend for as many as 256 simultaneous data connections to computer ports. Channels are continually scanned, in sequence, with total transparency and negligible throughput delays. Expanded versions of the PACX line can support up to 4000 simultaneous connections in a network serving as many as 12,000 attached devices. Larger configurations can be supplied for specific application requirements.

All standard speeds up to 9.6 kbits/s for asynchronous data and 19.2 kbits/s for synchronous data are supported with complete transparency to protocol on all channels. An auto-baud feature detects the asynchronous terminal speed and routes the connection to a requested service computer port with a matching data rate. COMNET utilizes the EIA RS-232 standard, but PACX optionally supports RS-422, RS-423, 20-mA current loop, and MIL-STD-188C.

Any one terminal can select from 128 classes of computer service. Optionally, specific classes of service can be restricted to designated terminals or specific terminals can be restricted to designated classes of service. All classes of service can be password-protected. Moreover, designated terminals can be "back-listed," thus limiting access attempts to specific classes of service for a predetermined period of time. Log-on messages can be sent to terminals and file closure messages can be sent to computer ports when a session is terminated. A timed port disable feature further protects open files from being accessed by new incoming calls.

All critical system elements—interface boards, power supply cards, control logic, and processor boards—are plug-in modules that enhance system upgrades, changes, and maintenance. Redundant power supplies and control logic provide protection against extended service interruptions. In the event of primary power outage, operating parameters are saved for up to 15 days by auto-recharged, battery backed-up RAM.

An integral control panel allows for central node configuration, system status checks, and channel data activity monitoring. An RS-232 console port permits network management from a terminal or, as in the case of COMNET, a host computer. Monitoring, diagnostic testing, system parameter programming, message generation, reconfiguration, and security restrictions can be enacted through the console port.

The PACX series is supported with a broad line of complementing data communication peripherals, such as modems, including a super modem that yields full-duplex, 9.6-kbit/s bandwidth across two unconditioned voice lines; a private intelligent network series of statistical multiplexers; Line Miser DOV systems; and an ASCII to 3270 network converter, and BSC/SNA gateway converters. Future products will include PACXNET modular gateways to baseband and broadband LANs.

To fulfill these GE requirements, the network must permit hundreds of terminals to optionally select and interact with dozens of computer resources and also be intelligent enough to facilitate management, maintenance, and reconfiguration without service interruption. And finally, it should never become obsolete.

The COMNET system

COMNET's development level consists of a LAN implemented around the Gandalf Data, Inc PACX IV private branch exchange (PBX). This standalone system performs all necessary contention and switching functions (see the Panel, "Gandalf speeds data communication"). This capability enabled the immediate implementation of an efficient distributed access to shared computer resources.

Since COMNET went online in October 1981, the network has yielded productive, cost-effective, and reliable performance. To keep up with emerging technologies, COMNET continues to develop in stages consistent with compounding requirements.

COMNET went online with 32 terminals (located in four remote clustered locations) that could selectively access and interact with three classes of computer service. Currently, more than 300 internal user terminals can optionally select and work with 28 internal classes of computer service. Network components (eg, terminals or computers) are considered internal if they are within COMNET's perimeter. The network's internal perimeter includes several large buildings, up to 25 miles apart. Dedicated communication channels link the GE-RSO main building in Philadelphia with all other locations within COMNET's perimeter.

COMNET's internal network computer resources include one or more of the following types: Digital Equipment Corp's VAX-11/780, PDP-11/70, and PDP-11/34; Hewlett-Packard's HP 3000 and HP 1000; IBM's 3033N; Honeywell's DPS-8/70; Gould SEL's 32-87/80; and Intel's MDS-80. All are accessible from EIA-ASCII terminals at speeds of 1200, 4800, or 9600 baud.

Within the organization, a potpourri of equipment is dispersed among many departments. Interactive terminals and hardcopy devices for data output are located wherever they are most convenient to user productivity. Laboratories, offices, conference rooms, shops, and service areas are equipped with units positioned at desk side, at workstations, or at any convenient location. Terminal activities cover a full range of applications including engineering analysis, data logging and retrieval, computer graphics, word processing, and electronic mail. A variety of burst-mode, ASCII asynchronous terminals are used, including keyboard

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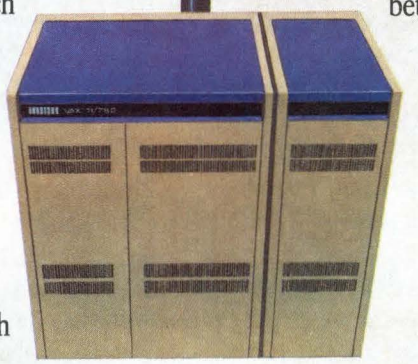

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CIRCLE 59

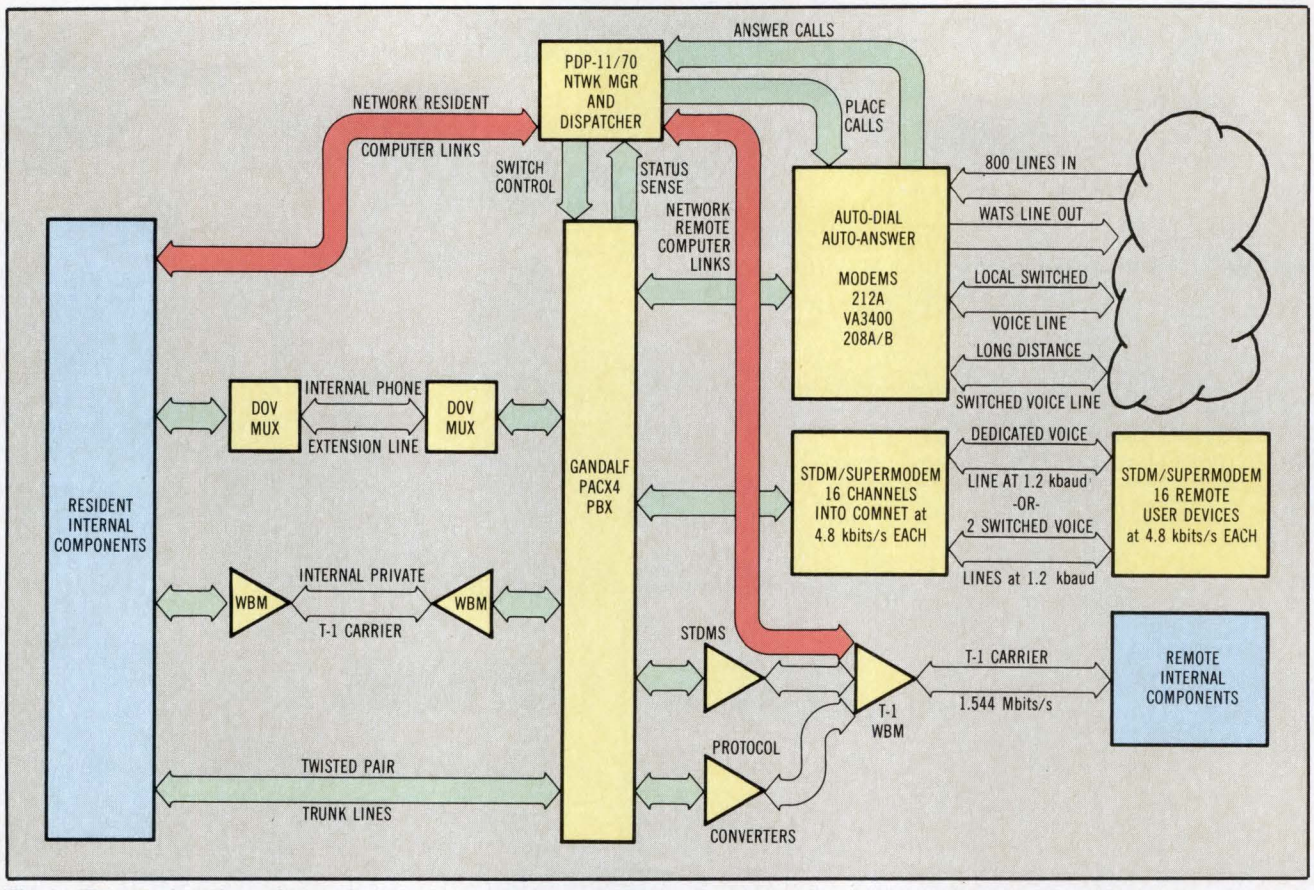

Fig 1 To permit universal use of COMNET terminal components, the convention of EIA RS-232-C, ASCII (green paths) is the communication medium to COMNET subsystems (yellow). Ports of most network internal computer components also operate on this convention. Converted forms of ASCII data are for adaptation to alien computer port protocols or for the expedience of multiplexed communication media. As network manager, the Dispatcher expedites most high speed intercomputer links (red) as well as tariffed carrier communication. Increasing speed and density of intercomputer data traffic is accommodated by a broadband bus medium.

printer types, graphics storage tubes, and multipersonality video display types. GE-Terminet and DEC LA100 printers are distributed to provide computer quality output print. Qume daisy wheel printers, equipped with cut-sheet feeders, product letter-quality output, while Tektronix and Versatec copiers and DEC LA100 printers are used to produce graphics hard copy.

COMNET's architecture comprises a star network, with the COMNET Center occupying the central node. COMNET Center includes the PACX IV data PBX, the network-managing Dispatcher computer, and all related communication and interfacing subsystems. Every network component (eg, terminal or computer port) requires a discrete connection to an access port at COMNET Center. Nearly all components require only four wires as an interface to the data PBX. Three wires (transmit, receive, and signal ground) provide full-duplex, asynchronous data communication. The fourth wire allows data terminal ready toggling of the network component to begin or end a COMNET session.

Creating, as nearly as possible, the semblance of a network with the characteristics of an open system interface is the goal behind COMNET. Conceptually, such a network allows every terminal access to every internal computer resource, even multiple resources. This requires special consideration for interfacing terminals and computer ports. Also, alien protocols must be matched and wide-area access must be provided for ports outside the network. The media used to communicate data among COMNET subsystems and network user components are illustrated in Fig 1.

COMNET Center, located in Philadelphia, occupies a laboratory room centered in a large, environmentally controlled, raised-floor area. Some of the COMNET computer resources are in labs in this same area. Direct, hardwiring under the floor is best suited here as an interface medium. Computer ports and terminals plug into connectors on distribution panels at satellite access nodes throughout the raised-floor area. Low capacitance, shielded trunks concentrate wiring from the satellite nodes to COMNET Center, where distribution panels fan the wiring out for discrete connection into PBX access ports.

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CIRCLE 60

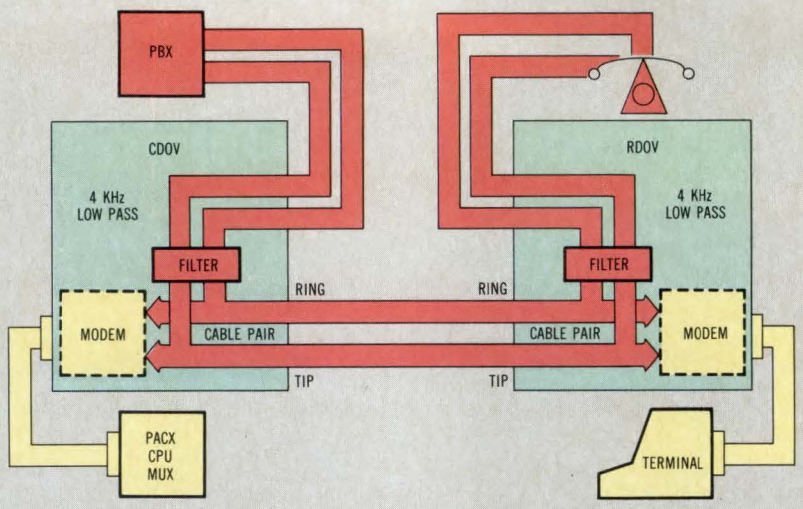

Fig 2 The Gandalf Line Miser DOV multiplexer communicates a single channel of full-duplex, synchronous or asynchronous data between a remote user device and the PACX IV at COMNET Center. The simultaneous communication of both voice and modulated data is on a totally noninterference basis, using only two extension telephone wires (ring and tip).

These are interfaced via Teltone Inc wideband multiplexers through which 32, 9.6-kbit/s data channels are concentrated on an internal T-1 backbone for demultiplexing and access to data PBX ports at COMNET Center.

As COMNET user resources expanded in scope, it became apparent that the most productive form of user access was through individually located terminals at lab workstations or at office desk side. Hardwire interface to accommodate these circumstances is an impractical investment in both material and manpower. A junction box that can be used almost anywhere permits relocation of staff members (with their terminals), a frequent occurrence in the aerospace industry's dynamic working environment. The terminal connects to the network through the box without installation and clutter of cables.

The data over voice (DOV) multiplexer is an analog modem that uses existing analog telephone extension wiring to communicate a single channel of 9.6-kbit/s data through the internal telephone network to a port on the data PBX at COMNET Center, while still permitting normal phone voice usage (Fig 2). Both the phone and a terminal are plugged into a DOV station unit which, in turn, is plugged into the phone's wall jack. Voice and modulated data communicate, without interference, over extension phone wiring. Dialing is unnecessary for data channel connection, which exists whether the phone is on or off hook, and there is no additional tariff for phone line use.

Installation is minimal; when the using party is relocated, the terminal and station unit are simply moved to the new location and plugged in. Using statistical multiplexers in combination with a DOV permits the interface of eight or more clustered terminals (or computer ports) on a single phone line, with all data channels operating at up to 9.6 kbits/s. More than 100 DOV multiplexer channels, supplied by both Gandalf Data Inc and Teltone are part of the network.

As the network's use has grown, interface among buildings internal to the network has been upgraded to accommodate increasing bandwidth demand. Initially, the 25 miles between Philadelphia and GE's Space Div headquarters in Valley Forge, Pa, was accommodated by a single, leased 4.8-kbit/s synchronous modem. Subsequently, a leased 56-kbit/s digital dataphone service link was used. Now, a dedicated 1.544-Mbit/s T-1 link handles multiple data channels (see Fig 3). Leased carriers, at bandwidths to 19.2 kbits/s, currently accommodate COMNET links among the several buildings in Valley Forge. This line-of-sight cluster of buildings is well adapted to use the GE GEMLINK S-band microwave communication system, which is being considered to provide T-1 service among them.

Long distance interfacing

Interface between internal network buildings not in line-of-sight range requires tariffed carrier service that includes monthly lease cost. In these cases, it is extremely economic to use a wideband carrier service such as the T-1 link. The T-1 link's capacity is equal to more than 1200 discrete 1.2-kbit/s leased lines between two termination points; yet the T-1 monthly lease cost is equal to the cost of only 50 of these discrete lines.

Using statistical time-division multiplexers (STDMs) is also cost effective. The STDM takes advantage of the terminal activity burst-mode characteristics, using data compression and buffering techniques, to make conservative use of carrier bandwidth. This allows four 1.2-kbit/s terminals to operate in the bandwidth space of one. This additional four-to-one bandwidth conservation raises the potential capacity of the T-1 link to 5000 terminals, still for the lease cost of only 50 discrete lines. All existing COMNET terminal data traffic, using leased dedicated channels, operates through STDMs. This reduces the current potential channel bandwidth need for that traffic from 24 to 6

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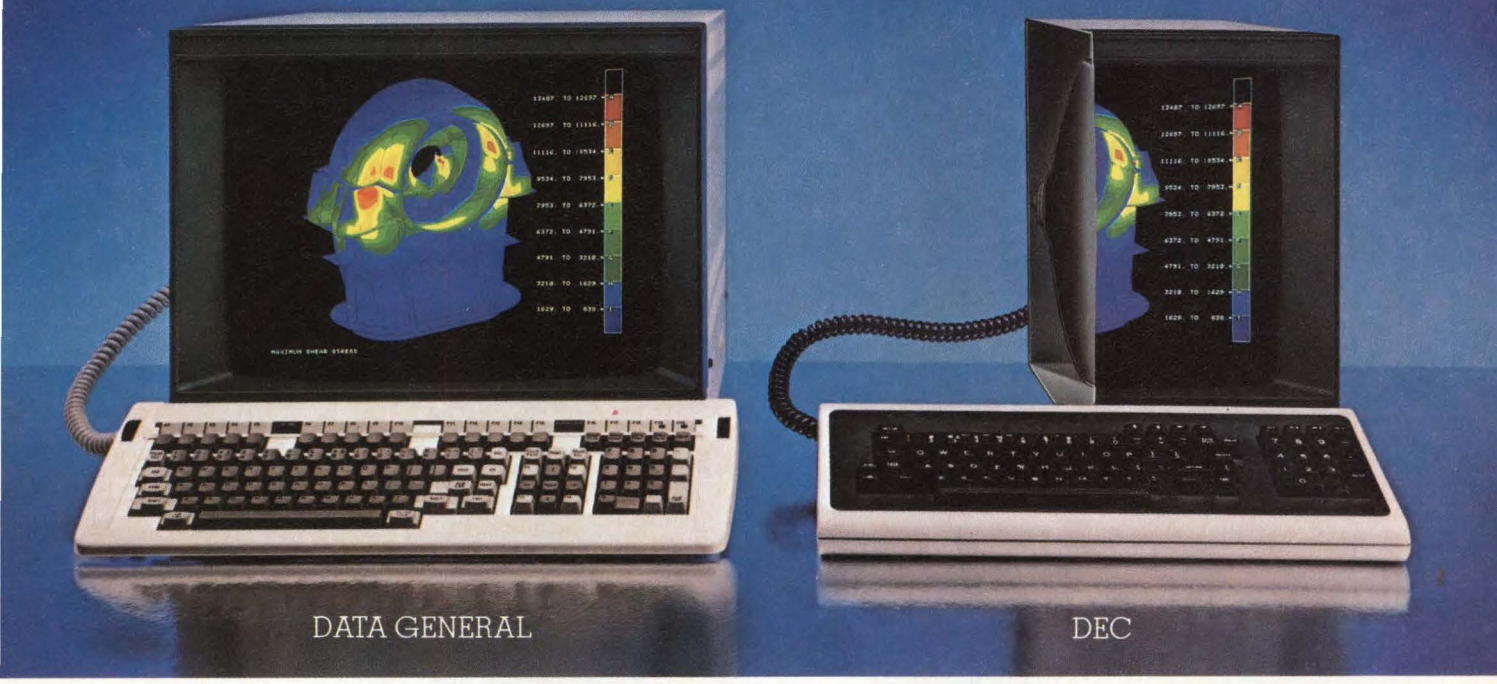

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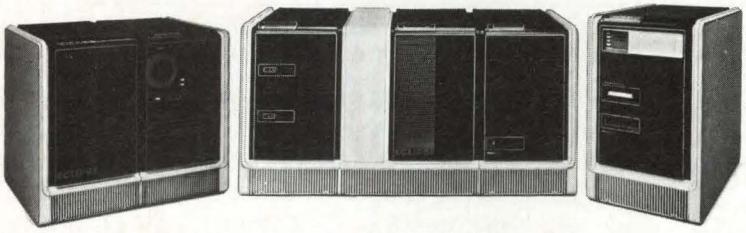

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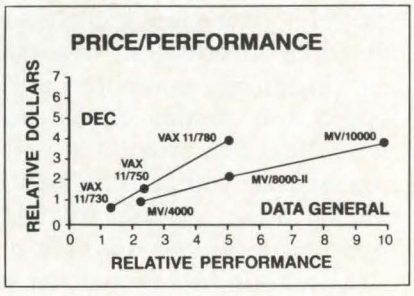

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CIRCLE 61

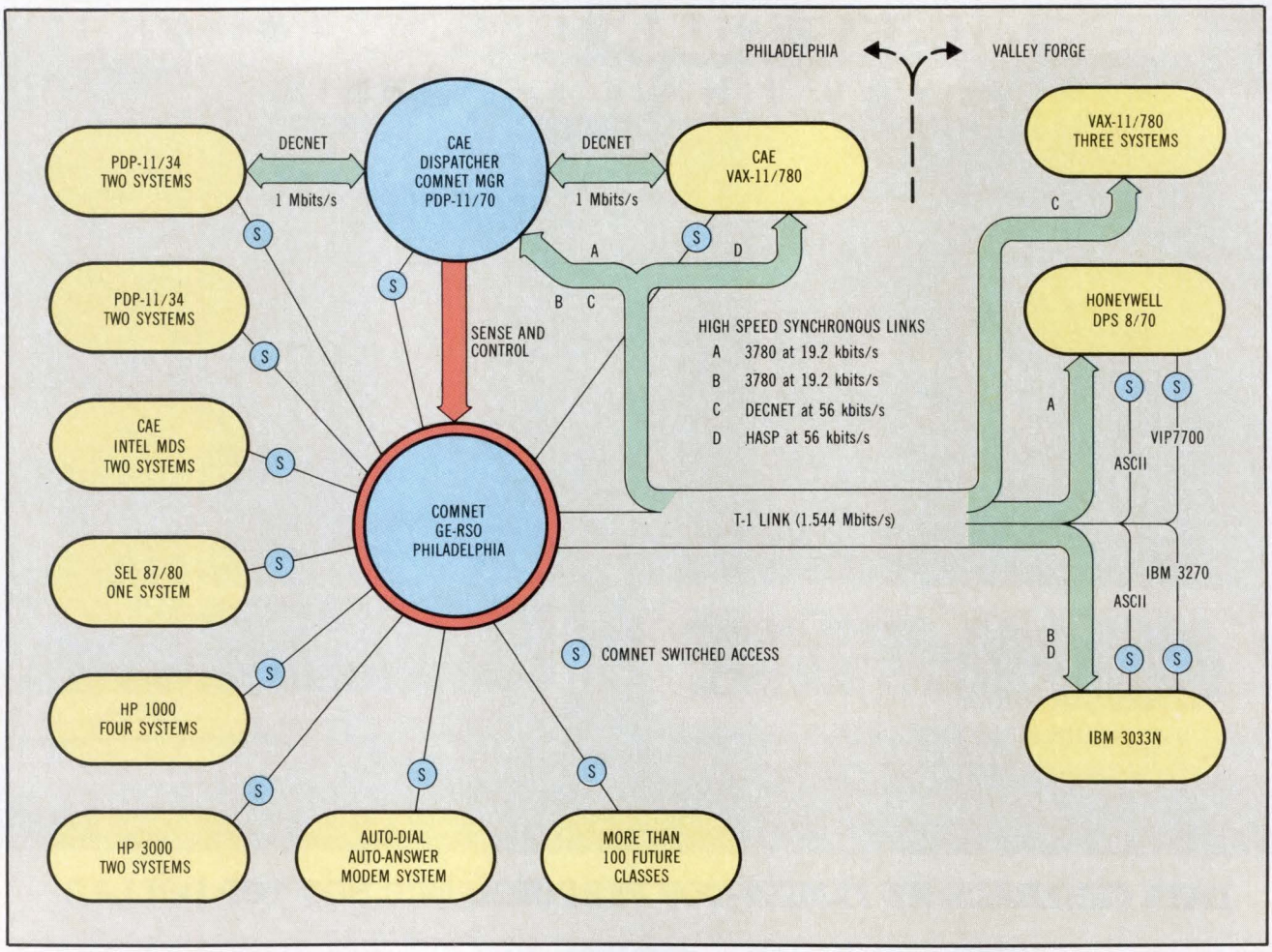

Fig 3 COMNET **users can choose among any of the illustrated computer systems that their access credentials permit. Existing intercomputer links are a stage in the development of an aggregate base of** COMNET **resources.**

percent. The greater share of the bandwidth is thus reserved for the high speed intercomputer links.

Dedicated high speed intercomputer channels incorporated into COMNET permit effective user access to multiple computer resources. The Dispatcher, for example, a PDP-11/70 computer that functions as network manager, is interfaced to the PACX IV data PBX control and statistics port. Every PACX IV connect and disconnect activity tagged with PACX IV channel address and time of day is logged into a Dispatcher file from the PACX IV statistics port. According to related PACX IV channel addresses, data relating to every network component, including information concerning terminal types and locations, computer port identities, etc, is logged into another Dispatcher file. By accessing these files, data relating to every COMNET transaction can be retrieved, yielding information concerning users, specific terminals, computer ports used, and time and duration of the transactions.

In addition, the Dispatcher serves as the hub for high speed synchronous data links among network computer systems (see Fig 3). On demand, a DEC Datatrieve file management utility residing in a network VAX computer will—across a DECNET channel—access and cross-reference these Dispatcher COMNET statistics files. Datatrieve extracts, sorts, and organizes the COMNET files, producing information useful to efficient network maintenance. For example, being able to examine port queuing and idle time enables the number of COMNET resource computer ports to be optionally maintained. Continuously updated vital network statistics can be retrieved at any time for review. These include the terminals in use, the COMNET classes of service they are being used for, how tariffed carrier services are used, and the level of usage of the various COMNET resources.

The information produced strongly supports network maintenance and is vital to the network's productivity, development, growth, and operating cost control. This type of multiple resource communicates across a 1-Mbit/s DECNET channel linking various DEC computer systems. The transaction is user transparent. Other high speed channels in use combine the resources of Honeywell, IBM, and DEC systems. Ambitions are to unify all COMNET resources that can be served to a practical advantage with high speed data channels.

"High speed" is an irresolute term when applied to data communication channels. The 1-Mbit/s DECNET channel that worked at only 9.6 kbits/s

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two years ago now has a speed 100 times that. Though impressive, this only manages to meet the increased requirements relative to COMNET user demand. As user activity increases, not only in number of users, but also in the coherent use of multiple resources, speed requirements continue to increase.

It is reasonable to project channel bandwidth requirements in the 100-Mbit range within two years. To support that data traffic density level, COMNET will be further upgraded by incorporating a broadband bus. The resulting hybrid network will continue to use the data PBX to do what it does best—handle the sporadic data flow of burst-mode terminals without needing to contend for access to a busy bus. The bus will support the expanding high density data communication requirements among COMNET computer resources and between serving hosts and intelligent workstations, such as personal business computers and systems for the automated office environment.

COMNET's high speed intercomputer channels permit effective user access to multiple computer resources.

Not all classes of service for existing network computer resources are directly accessible by asynchronous ASCII terminals, however. An IBM 3033N computer, for example, includes ports for IBM 3277 protocol terminals. Ports for VIP-7700 protocol terminals are on a Honeywell DPS-8/70 system. Both the IBM and Honeywell protocols are synchronous and require specifically adaptable synchronous terminals with associated preprocessing controllers. The controllers enable the specialized terminals to be used in a highly efficient block mode that permits full screen editing and the timesaving use of programmable function keys. Though desirable as a COMNET user option, the synchronous terminals are unadaptable to universal network usage and impractical for widespread and convenient distribution. Thus, the existing asynchronous ASCII video terminals have been adapted in COMNET to make use of both user-efficient protocols. Protocol converters from Thomas Engineering, Inc emulate the functions of both specialized synchronous controllers. Each converter concentrates data for up to 16 ASCII terminals for conversion and is listed as a standard COMNET class of service.

While internal computer services may be complete and comprehensive, there will always be business exigencies that require internal access to discretionary external resources. Likewise, communication to internal resources from random external locations will always be necessary. Tariffed carrier services are needed to provide this wide-area access capability. The local switched network and AT&T long distance common carrier services are used to accommodate the present volume of COMNET wide-area requirements. All inbound and outbound phone transactions are processed by the Dispatcher computer. Asynchronous data traffic is handled by a Racal-Vadic Multiline Automatic Calling System equipped with triple carrier modems. A Universal Data Systems RM-8 Multi-Modem System equipped with 208 compatible modems handles synchronous data traffic.

Processing phone transactions

A typical scenario of an inbound transaction for a single user involves a staff member placing a call from a terminal at home or at a remote business location. The call is placed through terminal keyboard command by a compact, portable, autodialing 212 modem issued for this use. An AT&T 800 area code service relieves the calling source of toll or message unit charges. In answering the call, the Dispatcher queries the caller for keyboard entry of an access code for security and accounting purposes. Upon satisfaction of this requirement, the calling terminal is transferred to the data PBX and ENTER CLASS is displayed on the screen to begin a standard COMNET session. A simple, straightforward, keyboard-executed dialogue enables access to any class of COMNET service from a terminal. Each class of service is identified and addressed with a 3- or 4-character mnemonic such as VX1 for VAX-11/780 no. 1. To access this class, the requesting terminal user proceeds in the following way:

KEYBOARD ENTRY:	SHIFT/BREAK CR
COMNET RESPONSE:	ENTER CLASS
KEYBOARD ENTRY:	VX1 CR
COMNET RESPONSE:	VX1 START

At this point, the terminal is connected to a port on VAX no. 1 and remains connected until the user terminates the session. The user proceeds with normal VAX protocol as though the terminal were connected directly to a port of that system. After a standard log off from the VAX, the user terminates the COMNET session with SHIFT/BREAK. Now another class of service can similarly be entered from the same terminal.

The user might select any of the 28 internal network resources in the same way. But if the next application requires external network access, the class of service requested would be utility (UTIL). For this class of service, the requester is presented in menu format, with a display of user utility options. The DIALER option displays a list of frequently called data phone numbers, each listed with an identifying mnemonic and information describing the destination computer resource. Keyboard entry of the mnemonic, along with a password, causes the phone number to be dialed and the connection to be completed by COMNET. If the

number is busy, COMNET has the option of repeated retries. The requester also has the option to self-dial a number from the terminal keyboard when that number is not on file.

COMNET terminals are in contention for the fixed number of computer ports on each class of service. Occasionally, all ports on a specific computer are busy. When this happens, the requester has the option of being put in queue for that class of service. The terminal displays the requester's position in queue as it advances, and an audible wake-up alarm informs the requester when a port is available. Since the data PBX functions on the principle of a time-division multiplexer, COMNET terminals are never required to contend for network access. Moreover, the number of users on the network never affects throughput.

UTIL, a continuing software development effort, provides COMNET users with other fundamentally useful utilities. When the UTIL class of service is invoked, the menu list of UTIL services is displayed on the terminal. Selecting a service results in a user-friendly prompting dialogue that leads the requester through its proper usage. UTIL services support three unique requirements: information retrieval, network maintenance, and network usage support.

Utility class PHNBK, for example, produces an up-to-date display of information previously available only from an annually updated phone book. The search-string capability for this service is very useful, (eg, when the user knows the room that a certain party occupies, but forgets the party's name and phone number).

Utility class SERVICE displays a form on the terminal screen with prompts to guide the entry of a service request from maintenance support personnel. The request subsequently enters a file that is regularly reviewed and acted upon by maintenance personnel.

And finally, utility class SNAP yields a display of all network activity at the instant a "snapshot" for this information is initiated. A listing of all current network transactions will be displayed with data relating to users, computer resources in use, connect times, and lapsed times since connect. In addition, a directory of HELP aids for information dealing with network computer and terminal usage is being developed.

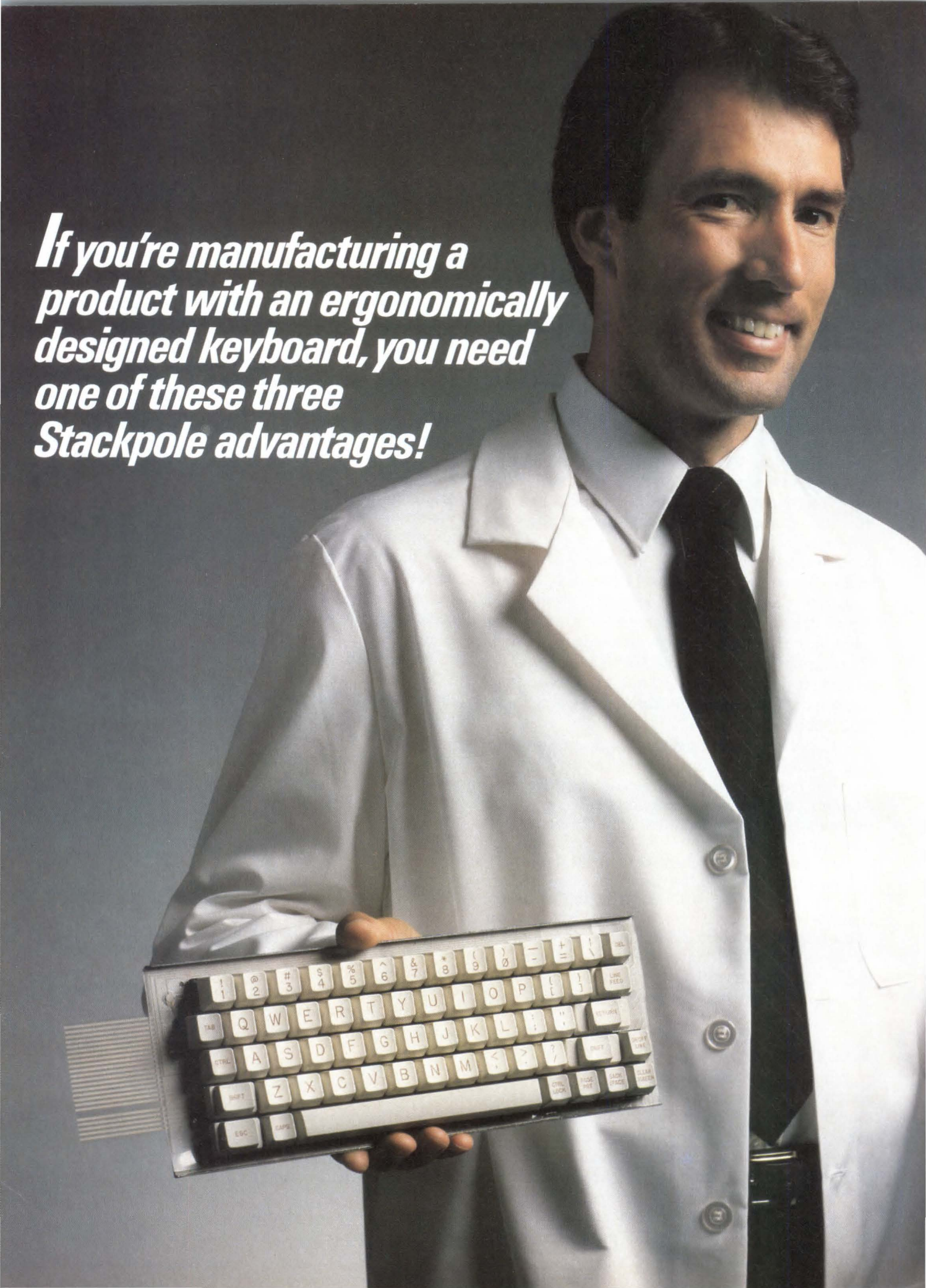
Economy of choices

When a single user invokes the DIALER subset of the UTIL class of service for an outbound transaction, the Dispatcher selects the most economical carrier service, then places the call. The choices are between WATS long distance toll service baud 5 range and public carrier for medium distance toll or local calls. If the volume of COMNET wide-area requirements increases to an established critical level, the common carrier form of service will likely be replaced by one of the value-added carrier services such as GTE-Telenet or Tymnet X.25 packet-switched networks. In addition to economic considerations, this form of service enhances reliability with alternate routing options and error checking/correction support.

A typical SNAP display of COMNET usage reveals that during normal working hours, 75 users are accessing 10 computer resources. If a new SNAP tally is examined 15 min later, usage is similar, but with a slightly different mix of terminals and classes of service being accessed. The conclusion is that COMNET is serving its intended purpose—random distributed access to shared computer resources. Aside from an occasional outage of a network computer or terminal component, user-tolerance to a COMNET failure has never been put to the test.

This reliability is due to a VLSI hardware subsystem design and a firmware-upgradable microprocessor intelligence. Another factor is that all key subsystems include redundant backup logic and power supplies. The Gandalf PACX IV, for example, incorporates a "warm transfer" standby processor that is automatically and continually updated with current operating parameters. It can also be switched online to replace the active processor. This backup feature has only been used for testing. Finally, thorough network management—consciousness of network performance at all times—is an effective preventive practice.

The cost-per-user terminal on COMNET averages $750. Some of the returns for this investment are directly measurable: elimination of the many leased modems formerly used for remote access and consolidation of interbuilding leased carrier services have resulted in an overall annual savings of more than $30,000. The more substantial advantages gained by increased productivity of both equipment and working staff have not been evaluated critically; but if acceptance of the concept is any indication of its worth, then it is overwhelmingly positive. Computer use is no longer the obscure domain of a staff specialist. Company sponsored training courses for computer usage are in great demand. A full cross section of staff members, from management to maintenance, has adapted to and relies on COMNET's expanding resources. Just as significant as considerations for productivity and economic advantage are the experience and insight gained by the users of COMNET.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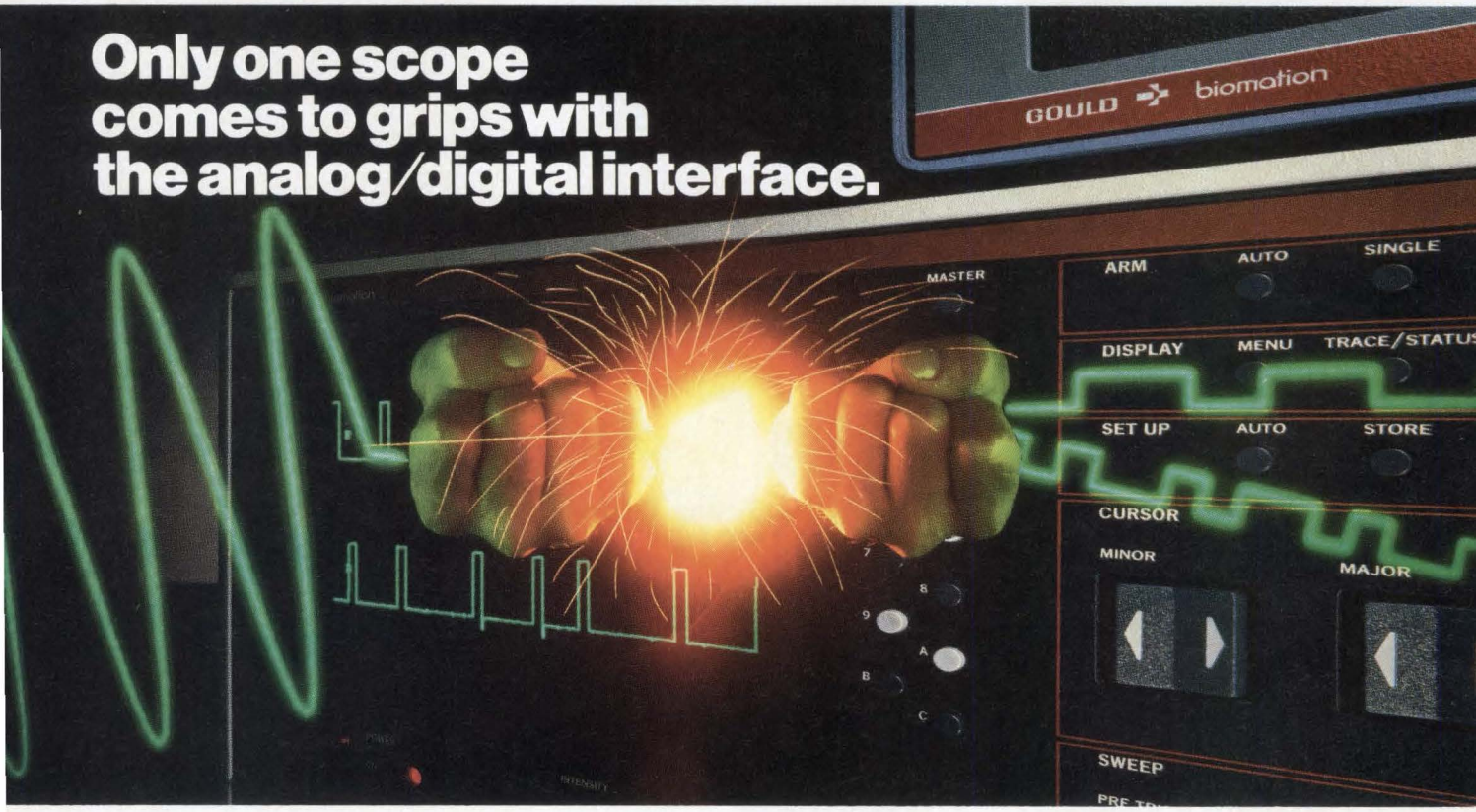

GOULD
Electronics

CIRCLE 64

CHOOSING THE RIGHT ENCODER SIMPLIFIES MOTION CONTROL

With microprocessor-based servos assuming an increasingly important role in automation, encoder selection has become as important as microprocessor choice.

by Mike Glass

The proven advantages of numerical position control systems ensure that microprocessor-based servo design will assume an increasingly critical role for machine tools and robots. Some advantages of digital position control are high accuracy and repeatability, direct communication with supervisory control and monitoring computers, and improved noise immunity. In addition, digital control (as opposed to analog) lends itself to more advanced statistical and adaptive control techniques.

Important issues in the design of such systems revolve around the microprocessor selection, and the implementation of the numerical control algorithm. In addition, of primary concern is the specification and interface design of position and velocity shaft encoders and their associated conversion electronics. This last design area, in particular, warrants serious consideration.

Microprocessors, particularly the 8-bit variety, allow the robot control designer to build low cost, modular, single-axis controllers. For most applications, the computational ability of the more advanced 8-bit micros (ie, the Motorola 6809) is sufficient for single-axis control and, in many instances, for multi-axis control. For more demanding applications, such as those involving inter-axis and/or very fast dynamics, or where tight control of velocity and/or acceleration is required, another approach must be used. This entails high speed arithmetic processors operating adjunct to the 8-bit units, or the use of 16-bit or bit-slice processors. In many robotic or machine tool applications, the 8-bit microprocessor-based controllers respond to commands from 16-bit microprocessors, or from 16- or 32-bit minicomputers. The more powerful processors typically perform the functions involved in overall supervision. This often entails substantial mathematical manipulation (ie, geometric coordinate transformation), in addition to the sequence and setpoint control for the particular operation being performed (ie, painting, welding, and/or pick-and-place).

Fig 1 illustrates a simplified block diagram of a single-axis microprocessor-based position servo. The motion control indicated is for a single axis, using a single-turn absolute shaft encoder for position feedback and an additional transducer, such as a dc tachometer generator, for velocity feedback.

Encoders: the critical components

As in any control loop, the feedback devices constitute the most critical elements. For purposes of robot motion control, resolution and accuracy of the position signal are important, but repeatability is often more so. Two other important factors are encoder dynamic response and accurate velocity feedback for servo loop stabilization.

The position encoder is most typically a potentiometer, an optical encoder, or a resolver. Potentiometers are the lowest priced of the alternatives. However, they have many inherent disadvantages. They are not accurate beyond 8 bits of resolution and require an A-D converter for interfacing. Furthermore, they tend to be noisy, and suffer from low reliability, particularly when used in dirty or harsh operating environments that are subject to high temperature and vibration.

Mike Glass is a senior engineer at ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716, where he is responsible for design of synchro instruments and I/O subsystems. He holds a BSEE and an MSEE from the State University of New York at Buffalo, and an MS in computer science from the Polytechnic Institute of New York.

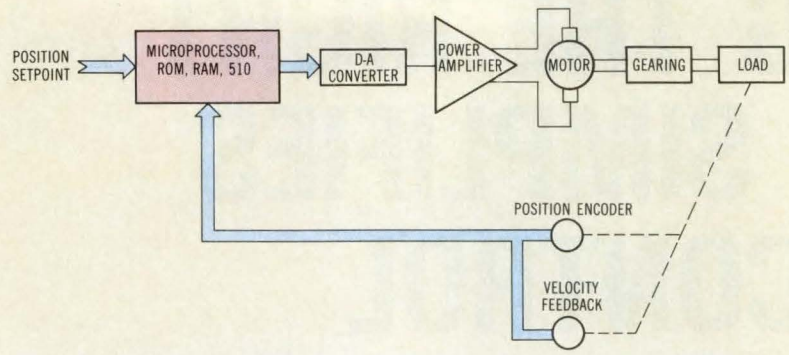

Fig 1 In a simple single-axis position servo based on a microprocessor, performance can be enhanced by using a tachometer to provide velocity feedback.

Of the three encoder types, the optical encoder has the most accuracy per bit of resolution. In addition, its interfacing electronics are enclosed within its encoder housing. Like the potentiometer, it requires only a single power supply and is well suited for many applications, particularly where incremental (as opposed to absolute) position feedback is adequate. Its principal drawbacks are high cost for absolute resolution beyond 10 bits (1024 counts/turn), large size, and reduced reliability in environments with high temperature, vibration, oil, or dirt.

Of the three encoder types mentioned, the resolver offers the most in terms of mechanical ruggedness and reliability, which is of particular importance in tough operating environments. A typical resolver position-sensing system has a reference oscillator (generally in the range of 400 to 5000 Hz), a resolver transducer, and an external resolver-to-digital (R-D) converter (Fig 2). In addition to ruggedness and reliability, a resolver-based feedback system offers several other advantages over an optical encoder system. A resolver is smaller, making it mechanically more suitable for space-critical applications such as robots. A resolver transducer, because it is an electromechanical analog device, has infinite resolution. While a resolver/converter will usually not have the inherent accuracy found in an optical encoder, this can be corrected by software system calibration.

In terms of repeatability, which is the critical performance parameter for many robotic servos (as opposed to absolute accuracy), the resolver system can very closely approach the optical encoder. Furthermore, the resolver transducer has only six connecting wires, compared to 16 for a 14-bit absolute optical encoder. Also, cost is a major consideration, since a 14-bit absolute optical encoder costs about $1000. A comparable resolver with associated oscillator and converter electronics has a total price tag of about $250.

Fig 3 illustrates in detail the required interface between a resolver transducer and a 6809 microprocessor. The configuration employs a DDC model RDC-19146-303 R-D converter to implement a single-axis, single-turn control loop. A built-in test (BIT) logic signal may be easily derived from the converter ac error signal, (eg, by means of a peak detector and comparator circuit as shown.) The BIT line gives a ready indication of whether or not the converter loop is functioning properly. A large error signal indicates that it is not.

The diagram also indicates one significant economy of resolver-based feedback: both position

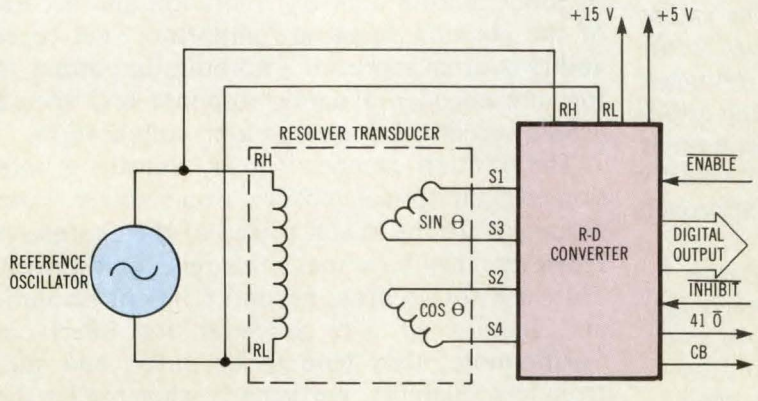

Fig 2 A typical position-sensing system consists of a resolver transducer, a reference oscillator, and an external converter to digitize the position information.

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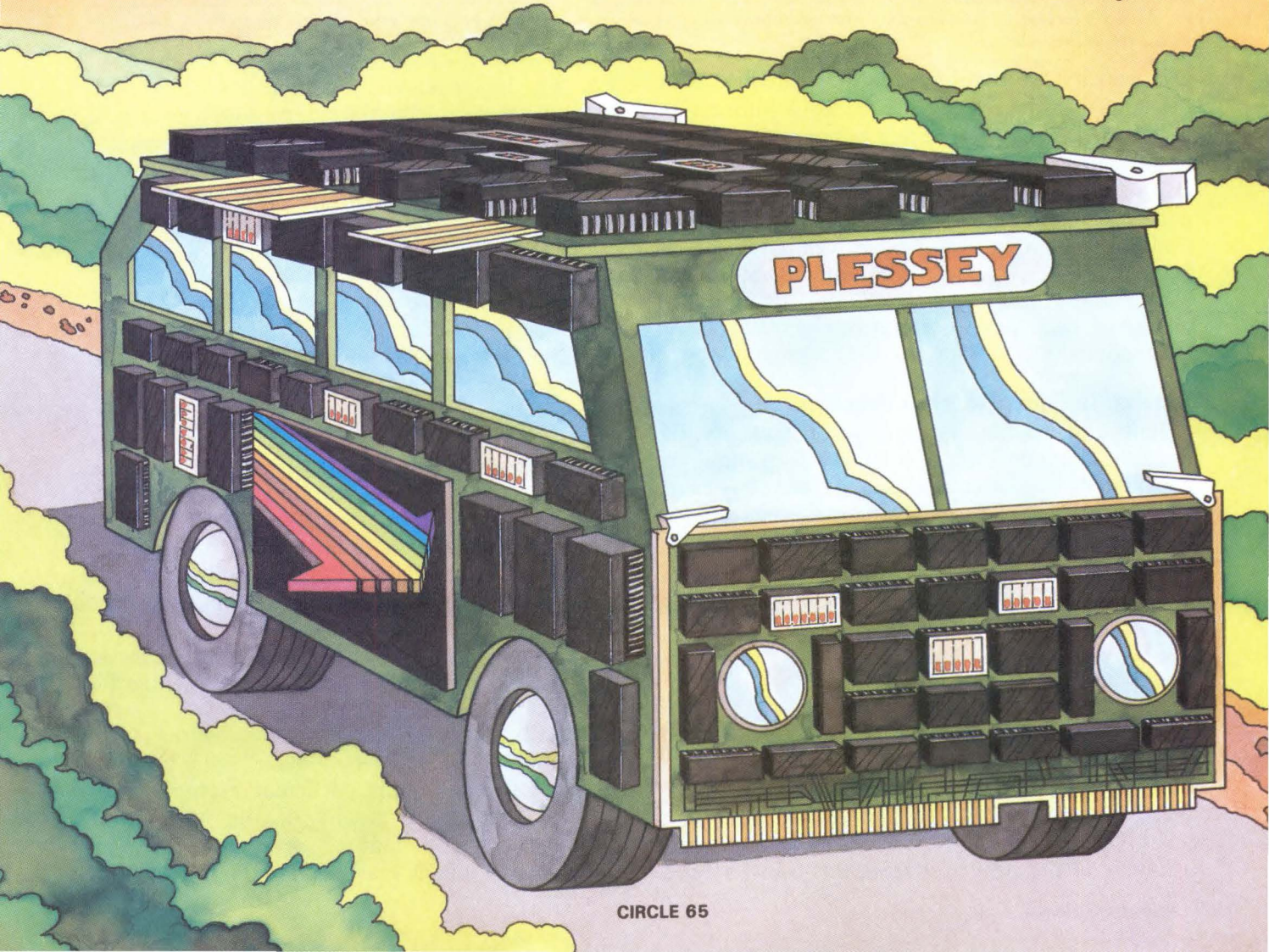

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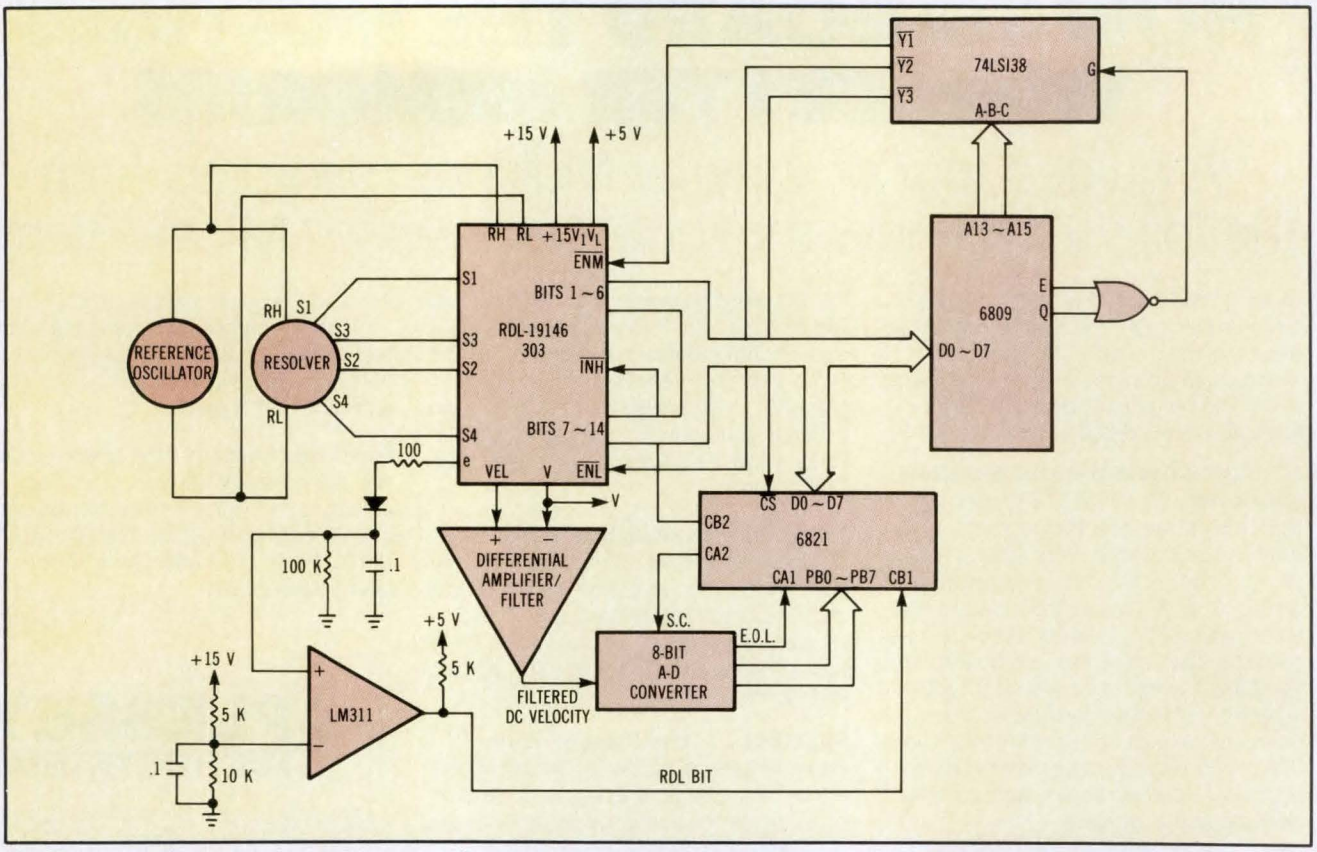

Fig 3 To interface a resolver with a 6809 microprocessor, a converter, such as DDC's RDC-19146-303, can be used as shown in this schematic.

and velocity information are readily derived from the same transducer. Velocity feedback information is provided in the form of a dc voltage. This voltage is developed intrinsically in the R-D converter as part of the conversion process. In addition to being necessary in situations where velocity and acceleration are to be tightly controlled, velocity feedback is used in the two most common digital control algorithms: "minimum-time" or "bang-bang" control, and proportional-integral-derivative (PID) control.

Resolver-to-digital converter dynamics

Before discussing motion control strategies, the dynamic characteristics of R-D converters should be considered. The internal design of R-D converters, such as the RDC-19146-303 (Fig 4), comprises a type II servo loop. That is, its simplified transfer-function block diagram may be represented as a forward loop gain of G and a feedback gain of unity, where:

$$G = \frac{A^2 \left(\frac{s}{B} + 1\right)}{S^2 \left(\frac{s}{10B} + 1\right)}$$

For the RDC-19146-303, A = 610 and B = 300. A number of things may be inferred about the dynamic behavior of the converter from this transfer function. The inclusion of the double integrator term ($1/s^2$) denotes the type II loop, (ie, the converter is able to track constant position and constant velocity motion with zero position error). This is indeed the case, provided that the input angular velocity does not exceed the converter's maximum tracking speed. The maximum speed for this particular converter is 20 rps. The 10-bit version of the same converter, the RDC-19106-301, can track up to 320 rps.

The large A^2 term indicates the following: the converter has a wide effective bandwidth of 610 radians/s (97 Hz); and the converter will track a constant accelerative motion with a very small acceleration error. For example, a 20 rps tracking converter with the above open-loop transfer function will have an insignificant dynamic position error, less than 1 LSB, if accelerated from 0 to maximum tracking speed over a time interval of 2 s. The dynamic errors reflected on the converter's dc velocity output are also miniscule, allowing this signal to provide useful $d\theta/dt$ feedback. The lead compensation, $(s/B + 1)/(s/10B + 1)$, ensures the dynamic stability of the converter's internal tracking loop.

Fig 5 illustrates the classical block diagram for a "minimum time," or "bang-bang" type position control scheme. In this particular example, it is assumed that the dynamics of the motor and mechanical system loading may be accurately modelled as a double integrator. That is, it assumes

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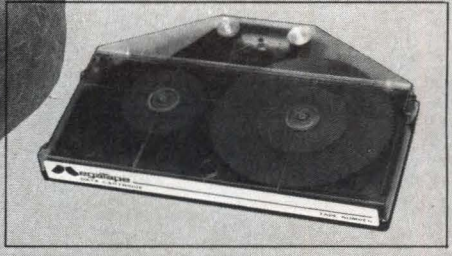

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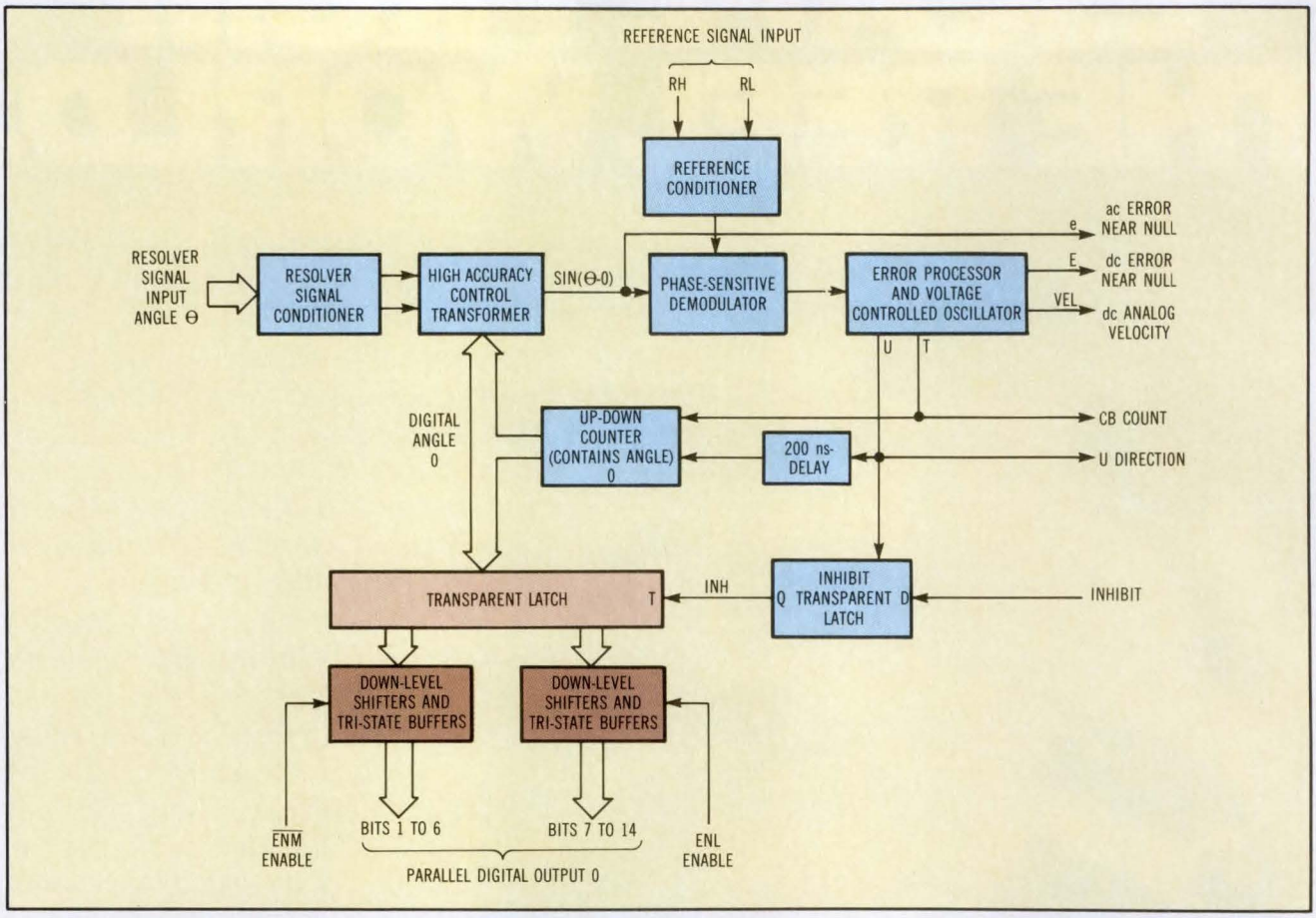

Fig 4 Internally, a typical tracking-type R-D converter functions as a type II servo.

that the overall load on the motor is chiefly inertial, with rotational inertia J, a reasonably close approximation in many applications. By applying either full accelerating torque or full decelerating torque, the servo motor's load may be programmed to travel from its origin to destination points in minimum time. The control law for such a system would be

$$I_{MOTOR} = \begin{cases} +\,|I_{max}| \text{ if } \dot{e} \le 0 \text{ and } \dot{e} > +\,\dot{e}^2/2\,|A_{max}| \\ \quad \text{or } \dot{e} > 0 \text{ and } \dot{e} \ge -\,\dot{e}^2/2\,|A_{max}| \\ -\,|I_{max}| \text{ if } \dot{e} < 0 \text{ and } \dot{e} \le +\,\dot{e}^2/2\,|A_{max}| \\ \quad \text{or } \dot{e} \ge 0 \text{ and } \dot{e} < -\,\dot{e}^2/2\,|A_{max}| \end{cases}$$

Where $|A_{max}| = |K_T\, I_{max}/J|$; K_T is the motor torque constant. Note that for this control law, the motor current may assume only the two limiting values of $\pm\,|I_{max}|$, resulting in corresponding acceleration of $\pm\ A_{max}$.

Velocity feedback a necessity

It is important to note that accurate velocity feedback is an essential ingredient in this design. This may be implemented by numerically differentiating the digitized position error, e. Naturally, this is the most economical method. However, this scheme has two principal drawbacks: it is very noise susceptible, and the designer is forced to trade off, by choice of sampling time, between poor resolution and data staleness. That is, a velocity indication derived from the difference of two successive quantized position readings is stale by approximately one-half the sampling interval. It is limited in resolution, and thereby in accuracy, by the relatively small number of LSBs traversed during a single sampling interval. Since the velocity feedback is used as an anticipatory indication, this staleness can result in undesired effects (eg, jittering or overshoot) in the loop's dynamic response.

Another scheme employs the use of a high speed clock, plus counters and additional logic, to measure the period between converter busy (CB) update pulses from the converter. This time period may be sampled along with the position information and converted to velocity via software. By use of a 25-MHz clock and appropriate high speed counters, full-speed velocity resolution/accuracy of about 1 percent (the worst resolution occurs at max speed) may be achieved. Although such a technique does provide fresher feedback data, it has the drawback of requiring the additional hardware of the clock oscillator and counters.

Using a direct speed-measuring device such as a dc tachometer provides accurate, fresh velocity information, but it is far less economical in that it entails the use of an additional transducer and an additional A-D converter. A nonstale velocity signal may be derived from the position transducer by using a resolver and a type II tracking converter, since a dc signal proportional to angular velocity is embedded in the type II conversion loop. A low pass filter to eliminate carrier ripple followed by a low cost linear A-D converter could be used to interface the R-D converter's dc velocity output to the microprocessor.

Along with the "bang-bang" type of control, the other type of digital position control algorithm commonly used is the PID technique. With this scheme, the motor command signal is derived from the raw error signal, and its digitized time derivative and integral. The relative amounts of the three terms are generally tuned online to optimize the loop response. The proportional term, modified by the derivative term for damping, constitutes the essential control law for translating between setpoint positions. The integral term provides a measure of stability near the null and compensates for long-term disturbances such as static friction. Dynamic response is often improved by clamping the integral term to zero during periods of motion, allowing it to come into play only when the loop is near null.

The PID type control law, while not providing a minimum time response as in the "bang-bang" system, offers the advantages of improved accuracy as well as superior stability (jitter-free) near the error null. It should be emphasized, however, that both algorithms require a source of fresh, accurate angular velocity feedback as well as an encoded position feedback. In some advanced controller schemes, the two algorithms are combined, reaping the advantages of both. The "bang-bang" law is used for making large step changes; the PID control law is then utilized near the error null.

Software calibration and tuning

The advent of nonvolatile IC memories in the form of nonvolatile RAMs (NOVRAMs) and electrically erasable PROMs has helped to facilitate the implementation of two critical functions of modular digital motion control. These two functions are calibration and tuning.

One simple algorithm of software calibration for a resolver-based feedback system is to correct the converter output angle per the following equation: $\theta_{\text{corrected}} = \theta_{\text{converter}} + \theta_1 + \theta_2 \text{ SIN } 2\theta_{\text{converter}}$. The θ_1 term corrects for resolver and system offset, which is largely mechanical. The θ_2 term corrects for transformation ratio mismatch errors in the resolver, isolation transformers (if used), and conversion electronics. This correction technique has the advantage of requiring only a simple, two-point calibration. Although it will not completely eliminate system error, it will usually reduce it by about 60 to 80 percent. If tighter absolute position accuracy is required, this can be attained by the implementation of a table-driven correction scheme. The correction table would have to be set up as part of a more lengthy system calibration procedure and stored in the nonvolatile memory.

In addition to storing calibration data, the NOVRAM may also be used for storing controller tuning coefficients. For the "bang-bang" example given, these would consist of the maximum motor current I_{max} and the corresponding maximum acceleration rate of A_{max}. For the PID controller, the coefficients would be the transfer gain A, integration time constant τ_I and derivative time constant τ_D. In either case, using stored controller constants allows for flexible online tuning to personalize the individual

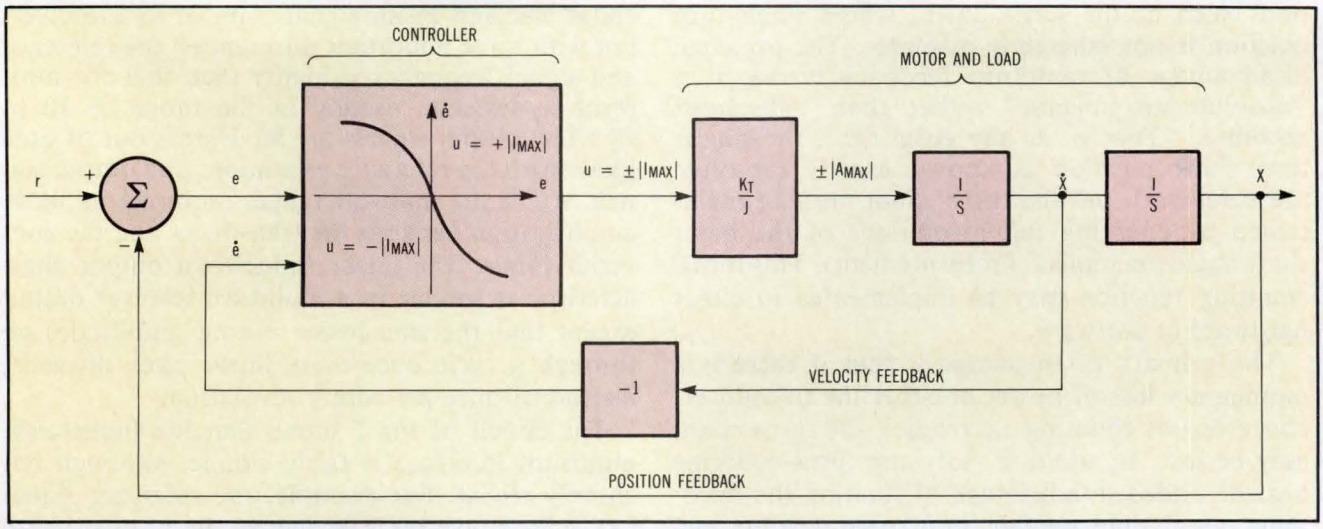

Fig 5 This block diagram for a "bang-bang" type of motion controller assumes that the mechanical servo dynamics can be accurately modeled as a double integrator.

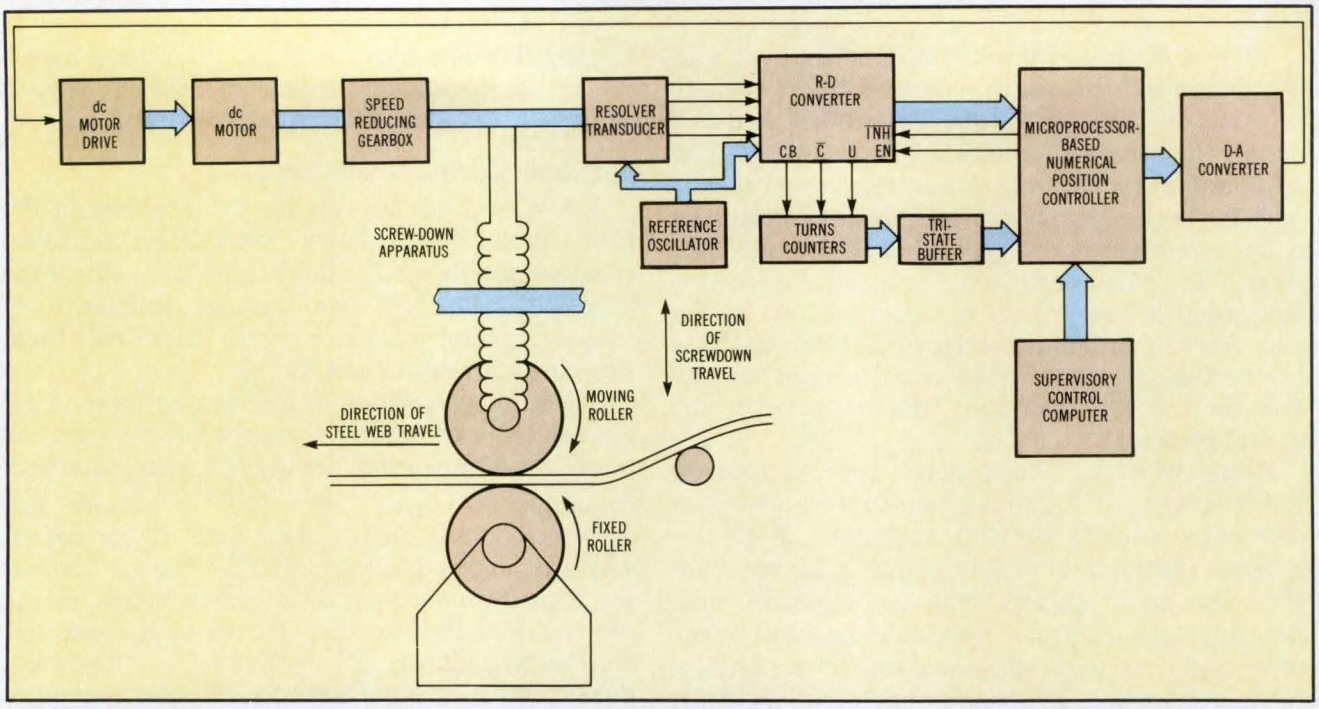

Fig 6 Multiturn feedback provides improved resolution and is required to provide the necessary accuracy in applications, such as this screw-down controller for a steel mill.

controller boards for the particular loop to be controlled. In addition, the need for jumper wires and/or relatively large, costly, and unreliable onboard switches is eliminated.

Multiturn position feedback

In an increasing number of applications, it is desirable to use multiturn as opposed to single-turn position feedback. An example of multiturn measurement is a screw-down system on a steel rolling mill. Fig 6 illustrates such a system.

The essential advantage of multiturn position measurement is that it provides improved resolution and therefore improved accuracy over single-turn sensing. A second advantage is that it eliminates the need for a speed reducing gearbox in applications such as the screw-down, where single-turn position is not inherently available. The principal disadvantage of multiturn feedback is that it is "absolute/incremental" rather than "absolute/absolute." That is, at any given time, the single-turn shaft position is known exactly (absolute measurement), but the turns count must be maintained by counting full revolutions of the input shaft angle (incremental measurement). This turns-counting function may be implemented in either hardware or software.

The primary disadvantage is that if there is a momentary loss of power in either the transducer, converter, or counting electronics, the turns count may be lost. In addition, software turns-counting has the added disadvantage of limiting the maximum permissible angular shaft speed (rps) to one-half the system sampling rate. If this speed is exceeded, one or more turns counts can be missed.

Fig 7 shows the interface between a Farrand Industries Inductosyn® transducer and a 6809 microprocessor as part of a numerical position servo. Industosyn transducers may be used to measure either multipole rotary or linear position. The linear Inductosyn depicted in Fig 7 can be used to measure the linear motion of a machine tool to an accuracy as tight as ±.0001 in. Rotary Inductosyns have typical angular accuracies of ±2 s of arc. An Inductosyn transducer consists of a printed wire type element (scale) with many parallel turns in a repetitive pattern etched on a flat surface. The sinusoidal excitation applied to the scale is inductively coupled to a pair of windings that comprise the moving element, or slider.

The Inductosyn output signal consists of double-ended sine and cosine signals, similar to a resolver, but with three important differences: the reference and signal frequency is higher than that for most resolver systems, usually in the range of 10 to 20 KHz; output signals are 90 degrees out of time phase with the reference excitation; and output signals are in the millivolt range, requiring accurate amplification between the transducer and the converter input. The linear Inductosyn output characteristic is similar to a multiturn resolver output except that the sine-cosine output amplitudes go through a cycle once every linear pitch distance, instead of once per rotary revolution.

The circuit of Fig 7 shows that the Inductosyn multiturn interface is fairly simple, although not entirely trivial. For example, the reference signal fed to the converter is 90 degrees out of time-phase (leading) to the Inductosyn excitation. Tri-state buffers are used to interface the position and turns

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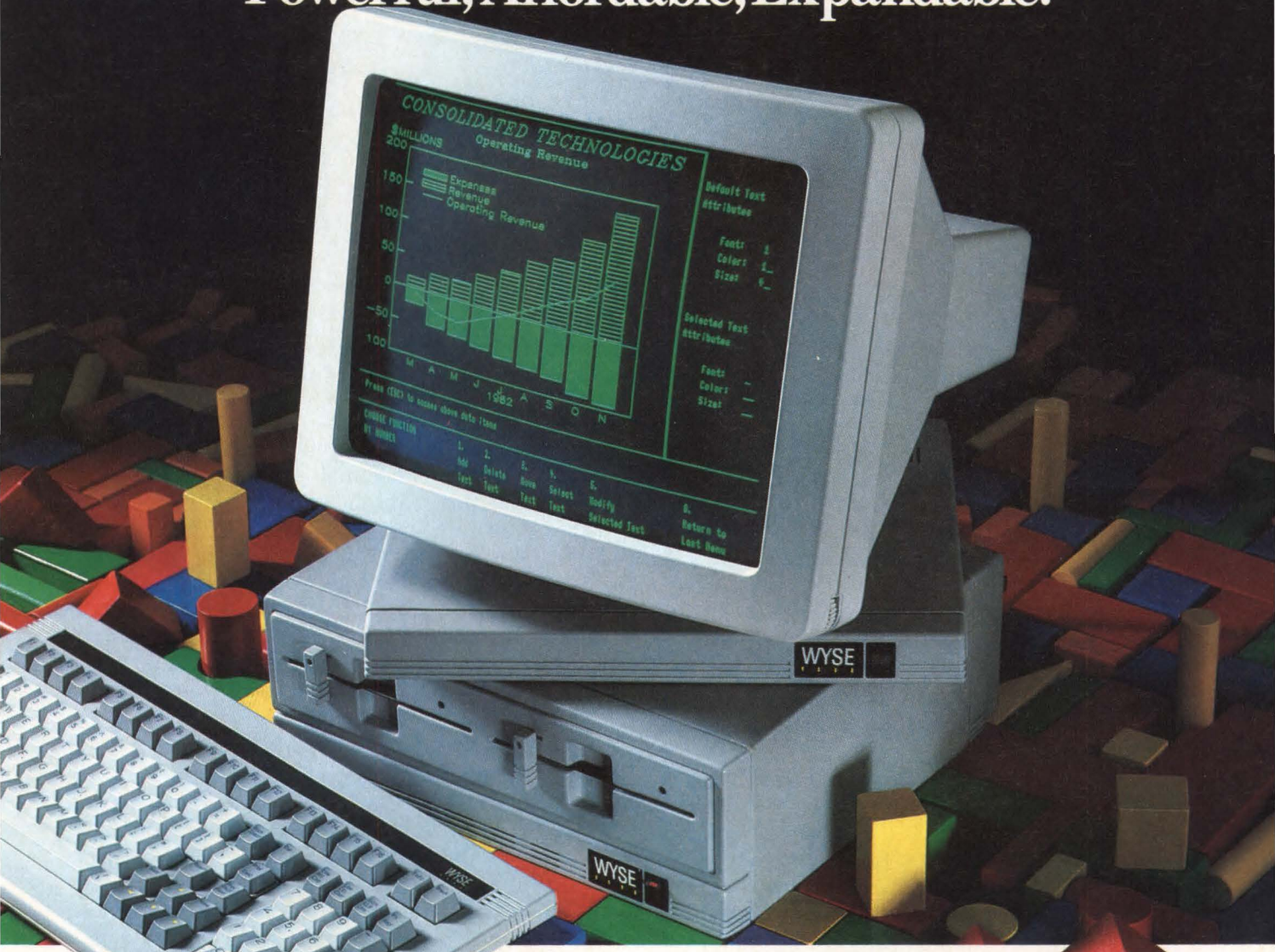

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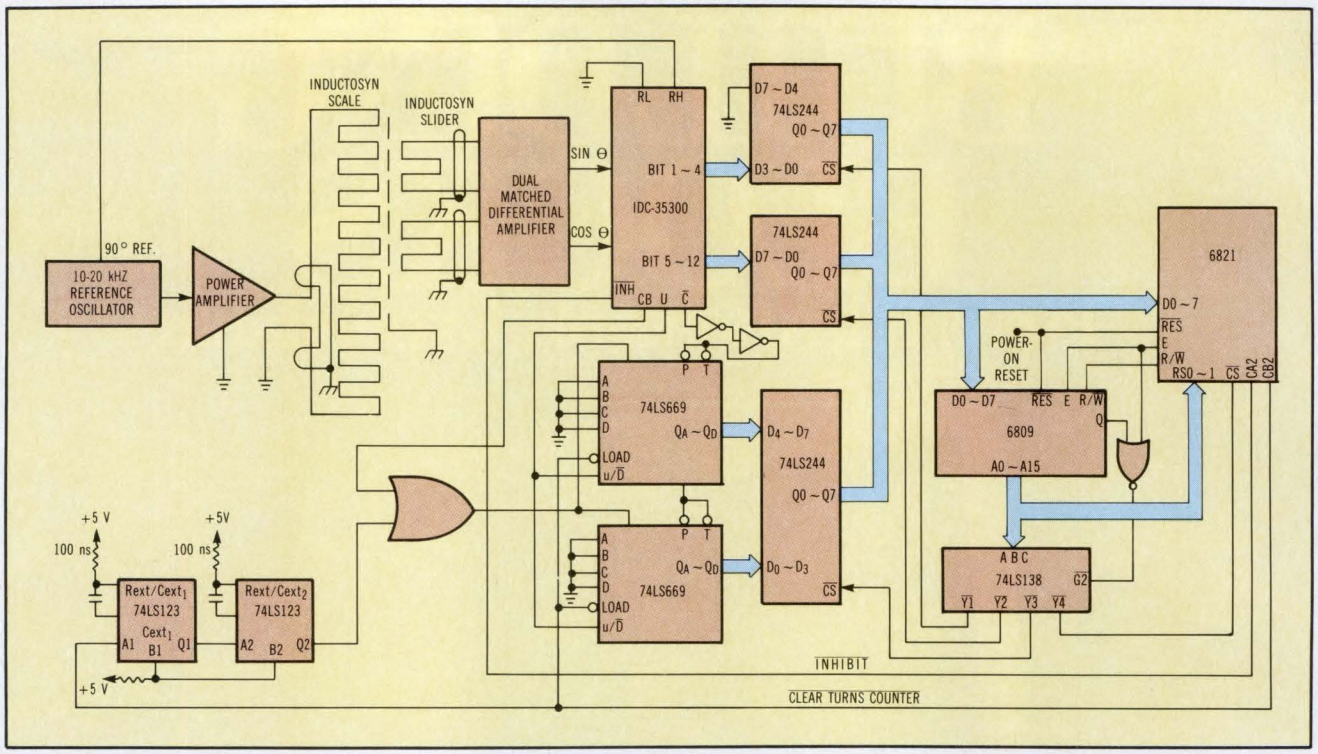

Fig 7 A linear Inductosyn® transducer can be interfaced to a 6809 microprocessor, as shown in this schematic for a highly accurate numerical linear position servo.

count outputs to the microprocessor data bus. Also, the Inductosyn converter shown (DDC's IDC-35300) features a Carry output, used for turns counting. In addition, the converter has Inhibit logic that freezes the parallel data outputs and disables the CB count output in such a way to preclude the possibility of skipping over the 00...0 code. This would otherwise result in a missed Carry pulse and turns count during a period of time when Inhibit is asserted. For the multiturn Inductosyn application, this feature is an absolute necessity.

This is a modification from other converters that are intended for single-turn use. An additional feature of the interface is a logic circuit consisting of a single-shot and an OR gate that ensures that at least one rising edge is provided to the clock inputs of the synchronously loading up/down turns counters when a clear turns counter command is applied. This command is used for setup purposes to zero the turns count.

Performance of resolver systems can be improved by employing a two-speed configuration. Then, the system has two position transducers, one coarse and one fine. The fine transducer, usually a resolver, will rotate many turns (typically from 8 to 36) for each turn of the coarse transducer. In addition, rotary Inductosyns are available that output a "multiturn resolver" type signal with effective speed ratios ranging from 180 to 1000. The coarse transducer may be an absolute optical encoder (6 or 8 bits), a potentiometer, or another resolver. The two-speed system is truly "absolute/absolute" in that the current actual positions of both the coarse and fine transducers are always available. There is no turns count to maintain and therefore power outages do not present a problem. The essential advantage of the two-speed system is that it provides an extremely high resolution and accuracy measurement of the single-turn (coarse) angle. The inaccuracy of this measurement is equal to the angular inaccuracy of the fine measurement divided by the speed ratio (gear ratio).

For the future, digital motion control will use high speed microprocessors for demanding control applications, such as robots employing vision systems. Such systems will require multivariate (multi-axis, velocity, acceleration, etc) realtime control. The results will be that fast, high accuracy position encoding devices, such as optical encoders, resolvers, and Inductosyns will be increasingly used to provide the necessary feedback signals to controllers. Future advances will contribute to the development of cheaper, higher performance data converters for resolvers and Inductosyns if these advances in digital motion control are to continue.

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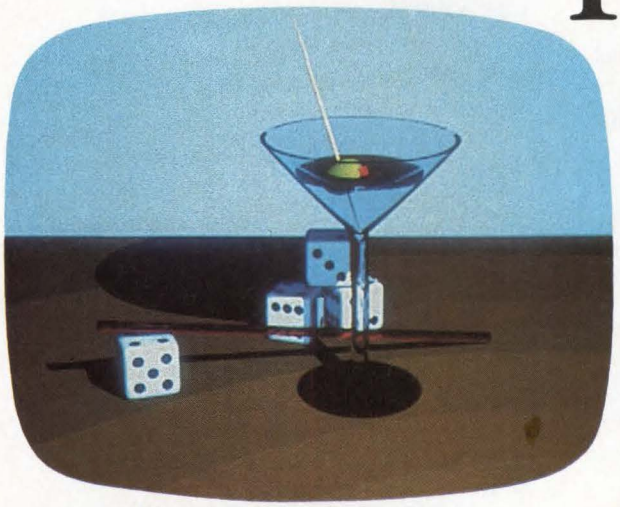

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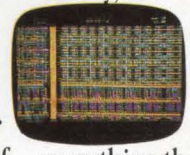

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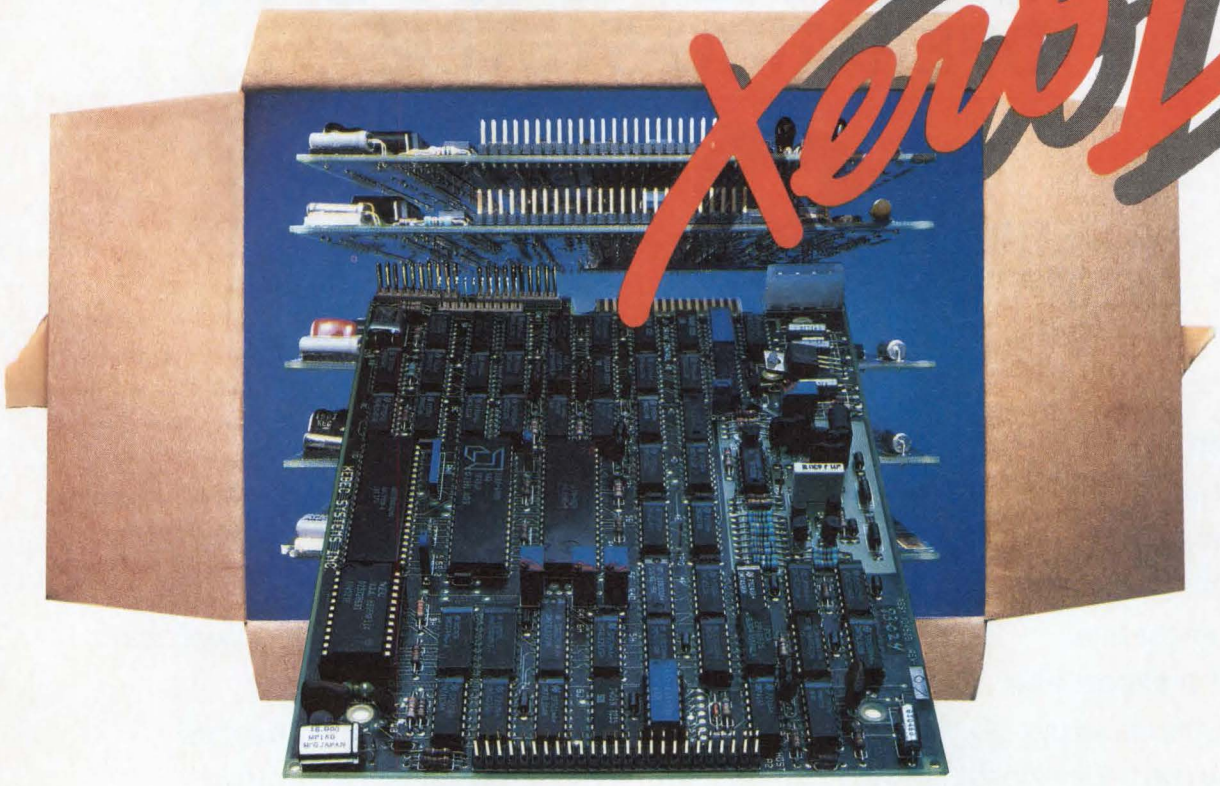

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MICROCOMPUTER CUTS PRINTER CONTROLLER CHIP COUNT

The addition of a UART, timers, and an onboard ROM to an 8-bit microcomputer gives designers a simple, effective way to implement a complete controller for a dot-matrix printer.

by James J. Millar
Bennett S. Scott, and
Bart Butler

Computer peripherals such as dot-matrix printers are among a growing number of devices that can benefit from the control features of single-chip microcomputers. The control of a dot-matrix printer, in fact, offers a good example of how hardware-enhanced microcomputers simplify the design and increase the efficiency of such peripherals.

With the same onboard microprogrammed CPU, RAM, and I/O as all of Texas Instruments' 7000-series processors, the TMS7041 contains 4 Kbytes of onboard ROM and a serial I/O port. In a printer application, the microcomputer is usually required to control several simultaneous asynchronous operations. Thus, a suitable controller must be equipped with internal timer/event counting circuitry to handle disassociated operations. The TMS7041 provides this capability in the form of two 13-bit timer/event counters supported by flexible interrupt features, such as maskable and priority set interrupts. Moreover, when additional control capability is needed, the 7041's baud-rate timer can double as an additional general purpose timer.

To run a printer without placing excessive management and software burdens on the host processor, the controlling microcomputer must be able to store control programs locally and provide a small amount of ROM for specialized routines. With its 4-Kbyte ROM, the chip's capacity is more than ample for these purposes.

Communication is another requirement of dot-matrix printer controllers, and for this reason, the TMS7041 is equipped with a serial port that enhances its I/O and communication performance. While the serial port operates in a variety of modes, the most important for a printer controller is one that allows interfacing with a universal asynchronous receiver/transmitter (UART). The inclusion in a controller of a hardware-constructed serial port reduces the amount of code that must be stored in ROM, and permits higher data transmission rates than can be achieved with software. The TMS7041's full-duplex serial port contains both a double-buffered transmitter and a receiver.

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Bart Butler is a microcomputer applications engineer at TI, Houston, where he is responsible for 8- and 16-bit microprocessor system architecture designs. He holds a BS in electrical engineering from Texas Agricultural and Industrial University.

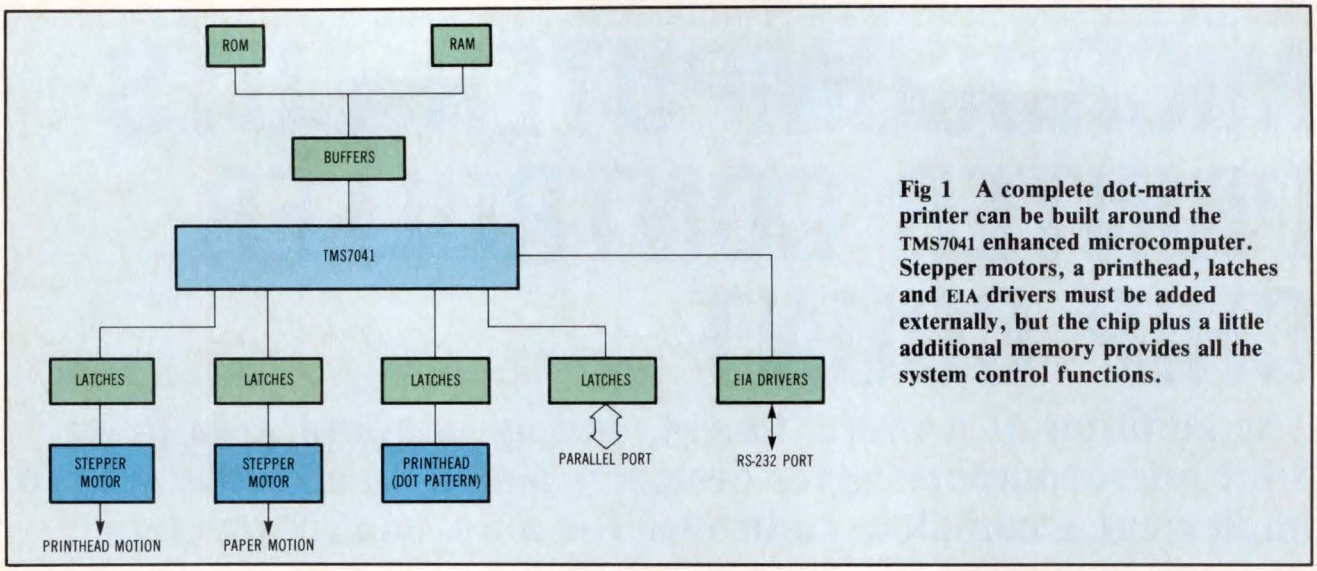

Fig 1 A complete dot-matrix printer can be built around the TMS7041 enhanced microcomputer. Stepper motors, a printhead, latches and EIA drivers must be added externally, but the chip plus a little additional memory provides all the system control functions.

Just a few years ago, a 150-char/s dot-matrix printer with sufficient intelligence to perform bidirectional seeks, communicate with its host, offer conventional and exotic print fonts, and provide form control would have required a board full of hardware to support the controlling microprocessor. Options such as a receiver buffer RAM or diagnostic capability would have necessitated extensive changes to the system software, in addition to extra hardware.

By comparison, with today's advanced microcomputers, a complete printer controller can be designed starting with a TMS7041 microcomputer and adding the appropriate Electronics Industries Association (EIA) drives, latches, system timer, and ROM/RAM. Fig 1 shows the system block diagram of such a controller, including the printer hardware-stepper motors and printhead. Additional functions can be integrated with minimum impact on the control unit by taking advantage of the controller chip's modular, multitasking operating system. Table 1 lists the functions performed by the single-chip microcomputer shown in Fig 1. The primary features of the TMS7041 used in the printer application include the onboard timers and the serial communication port (UART).

An innovative interrupt technique that allows priorities to be assigned to interrupts at the software level is responsible for handling the asynchronous printer operation. The primary features include high speed (150-char/s) printing with multiple character fonts, graphics capability, and form control. The printer can communicate with its host processor over a serial or parallel communication link, and a designer can add diagnostics to check out printer operations before the machine begins a task.

Microcomputer complements printer needs

The first requirement of a dot-matrix printer is that the machine run at high speed when putting dots on the paper. A printing algorithm must operate—on the fly—during printing, to achieve this high speed. While the printer's horizontal resolution is 1/200 in., its vertical resolution is even finer at 1/144 in., or 1/2 dot. It should be noted that the printer offers a range of dot densities to support various printing speeds. With the TMS7041 as the controller, dot densities from 60 to 500 dots/in. can be implemented. In addition, the controller permits the intermixing of any combination of character sizes and graphics.

All microcomputers in printer control systems store the printing algorithm in ROM. Dot-pattern tables are placed in ROM and are read as needed,

TABLE 1

Microcomputer Functions in a Printer Controller

Single-Chip Microcomputer Controls Printer

- Single-chip microcomputer
- External ROM and RAM
- External latches
- EIA drives
- System timer

Make up all electronics for printer

Microcomputer Features used by Printer

- Timer 1: Motor motion timing
- Timer 2: Dot control timing
- UART: Serial communication
  - 7/8 bit data
    - 7 data, 1 parity
    - 8 data, no parity
  - Baud rate
    - 200
    - 300
    - 600
    - 1200
    - 2400
    - 4800
    - 9600
- Interrupts:

Reset	
Parallel port (Data strobe)	INT1
Carriage motor (Timer 1)	
System timer	INT3
Dot timer (Timer 2)	

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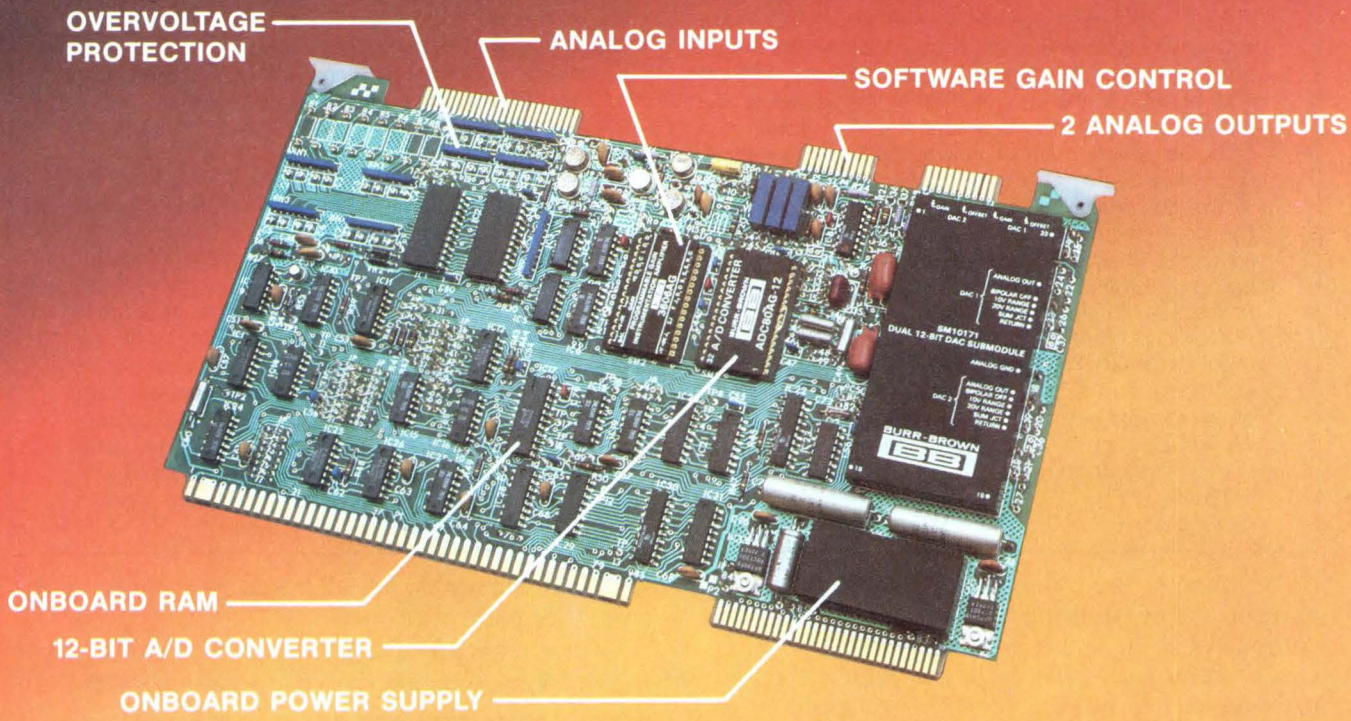

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Multibus™ Intel Corp.

SCAT beefs up microcomputer hardware

With its TMS7040 microprogrammable microcomputer providing the intelligence, the TMS7041 chip surrounds itself with a UART, programmable timers, and an onboard ROM in order to deliver a complete control integrated-circuit for dot-matrix printers or for a variety of other applications in a single chip. This latest member of the TMS7000 family is easily hardware-upgradable because of its so-called strip-chip architectural topology.

Features such as a UART can be added along the edge of the TMS7041's silicon real estate since strip-chip architectural topology (SCAT) allows new functions to be laid out strip-wise. This means that data and control paths run on higher metal levels than other interconnections. Thus, the connections can run over active devices below, conserving valuable real estate. Data paths run in a direction corresponding to the way individual bits line up. Bit 0 or register 0, for example, runs directly over bit 0 of register 1; however, the control paths run perpendicularly to the data paths because they connect to an entirely different set of elements.

A unique feature of the TMS7041 is its multiple protocol capability for multiprocessor systems. Multiple protocols are extremely useful to designers who must upgrade existing systems, since they permit the controller chip to step into a design regardless of which manufacturer's microcomputer was used originally. In the Motorola protocol, data blocks are distinguished from other information by a longer idling time between the frames that comprise the blocks. This type of protocol is used for transmitting large data blocks on an infrequent basis.

On the other hand, Intel's protocol requires an additional address/data bit immediately before the stop bit. One block is distinguished from the next by setting the address/data bit. In this protocol, idling time between blocks has no meaning. As a result, the protocol offers the exact opposite characteristics of Motorola's—it is best suited to the frequent transmission of small data blocks. The TMS7041 is equally at home in either of these hardware environments.

In addition to its protocol versatility, the controller chip operates in any of the three popular data-transfer formats: asynchronous, isosynchronous, or clocked serial. The first two formats are more applicable to communications between UARTs. Clocked serial is preferred for dumping data into serial shift registers.

The TMS7041 serial-link UART is a viable technique for providing a communication bus in multiprocessor systems. Such systems are gaining popularity in process control applications that require each microcomputer to be dedicated to a specific task under the direction of a host or central computer. The printer controller applications have a strong resemblance to process control, so a similar type of hardware can serve in both cases. A serial port consisting of a UART and baud-rate generator is also well suited to the character-oriented applications found in dot-matrix printers.

rather than using valuable CPU time to generate patterns. The limiting factor for most microcomputers is the speed at which these dot patterns can be referenced. To satisfy a printer's realtime printing needs, the controller chip relies on indexed and indirect addressing.

In indexed memory addressing, a memory address containing the operand is specified. This address is the sum of the contents of one TMS7041 register and a 16-bit direct address. Using this addressing technique, the execution of a mosaic character-set printing algorithm requires indexing into a table three times.

The TMS7041 architecture effectively provides sixty-four, 16-bit registers for indirect addressing. That is, the chip's entire 128-register capacity can be used for indirect addressing. Indirect addressing uses a 16-bit value stored in two consecutive 8-bit registers as the operand address. This technique permits an algorithm to execute at rates up to six times faster than on microcomputers having one or two index registers.

The strategy behind the controller chip's adaptability for printer applications lies in the use of table-driven code. Essentially, the technique consists of putting the major share of the microcomputer's intelligence into tables to reduce the CPU section's calculation burden. Of course, the chip's 4-Kbyte onboard ROM supports this approach. An additional benefit is that relatively simple table modifications permit the design of a line of printers with many features, but all based on a single microcomputer controller.

Overall control of the TMS7041 is exercised by a multitasking, channel-based operating system. In

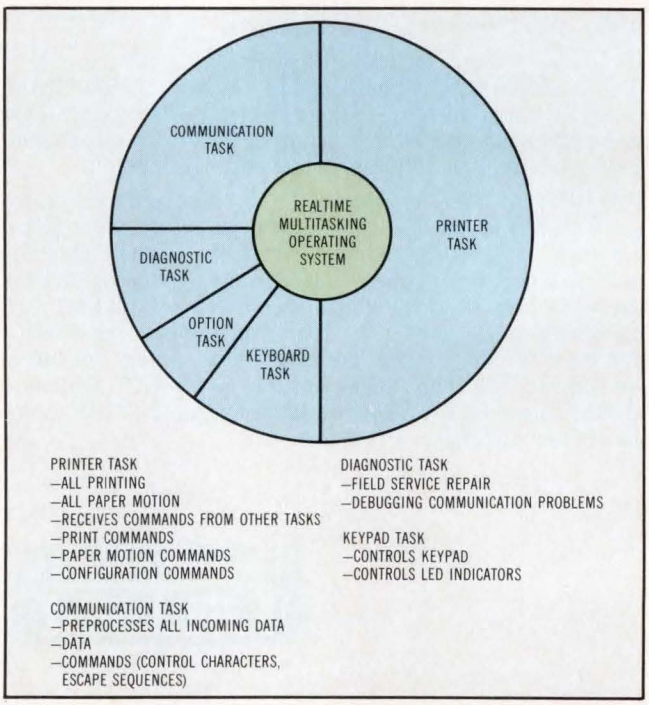

Fig 2 At the heart of a printer's microcomputer controller is the system firmware, anchored by its multitasking operating system. The operating system, stored in the TMS7041's onboard ROM, directs the activities of individual tasks.

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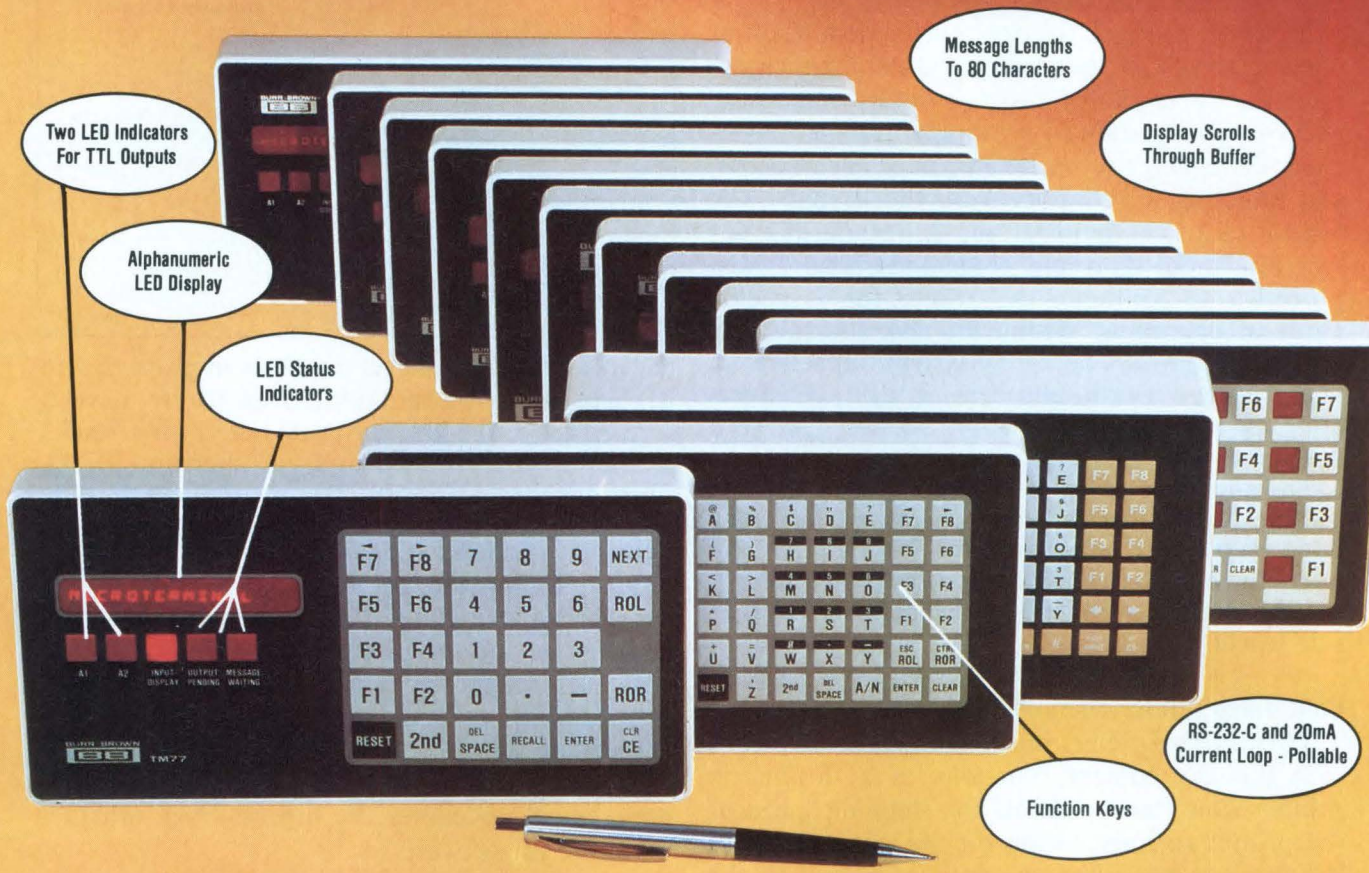

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TM77-I/O	16	110-19200	320(1)	Numeric	14	Larger keys	+5VDC
TM71B TM71MS	16	110-19200	320(1) 5 x 50(2)	Alpha	16	Bar Code Wand	+24VAC/ DC
TM77B TM77MS	16	110-19200	320(1) 5 x 50(2)	Numeric	16	Mag Stripe Reader	+24VAC/ DC
TM71M	16	110-9600	320	Alpha	14	Military	+5VDC
TM70	12	300 & 1200	36	Alpha	8	Low cost	+5VDC
TM76	12	300 & 1200	36	Numeric	8	Larger keys	+5VDC
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such an operating system, one task communicates with another by sending a message to a channel or another mailbox. Although the operating system is capable of managing complex operations, such as time slicing of tasks, in the printer application it need handle only two basic functions—task control and task communication.

As shown in Fig 2, the operating system has four main tasks within its control and communication domain. Three of the tasks—printer, diagnostic, and keypad—pertain to printing and paper movement, debugging the machine when problems occur, and handling data inputs from the keypad. The fourth task, communication, is responsible for receiving input data and commands from a host processor to configure the printer for a specific mode of operation. Within the task control category, the TMS7041's operating system can activate a task, suspend a task, and delay a task. The operating system's communication portion can read from and write to a mailbox.

The operating system does not contain a separate routine for performing error checks on incoming data; each task is responsible for that function. All operating system functions affect only the printer—its operation is completely transparent to the outside world.

Controlling printer operation

Two internal timers on the controller chip provide the key control functions of a dot-matrix printer. One timer controls the stepping speed of the printer carriage, while the second looks after the dot density—where the dots are placed on the paper. Both timers operate completely asynchronously and independent of each other. A third timer, external to the microcomputer, sends interrupts to the control system every 50 ms.

Timers are important in printers that operate in an open rather than a closed control loop (this article describes the design of an open-loop system). Closer control can be achieved in a closed-loop control system, but such a system requires precision control elements. Moreover, because of stability considerations, a closed-loop system must be capable of higher operating speeds than an open-loop system. Since open-loop systems have no need for precision elements, they are less expensive to design, and operate more reliably. The open-loop approach is also more suitable for microcomputer controllers (such as the TMS7041) that rely more on table-driven code and less on the chip's internal computation ability.

Associated with the system timers is the controller chip's interrupt structure. The TMS7041 provides six interrupt levels, and one of the chip's features is the ability to set priorities for these interrupts in software. At the hardware level, however, the highest priority interrupt is level 0, which is reserved for the Reset function. Level 1 follows in priority, and is a user-defined external interrupt (INT1). Level 2 is reserved for the first hardware timer, while level 3 is another user-defined external interrupt (INT3). Level 4 is the serial-port interrupt and level 5 is the second hardware timer. All external interrupts and Reset have Schmitt-trigger inputs.

TABLE 2

TMS7041 Hardware/Software Interrupt Priorities

Interrupts

TMS7041 flexible interrupt structure allows printer firmware to set (and change) software priority levels

	Hardware level	Software level
Reset (INT0)	0	0
Parallel port (INT1) (Data strobe)	1	3
Carriage motor (INT2)	2	1
System timer (INT3)	3	5
UART (INT4)	4	4
Dot timer (INT5)	5	2

0: Highest priority
5: Lowest priority

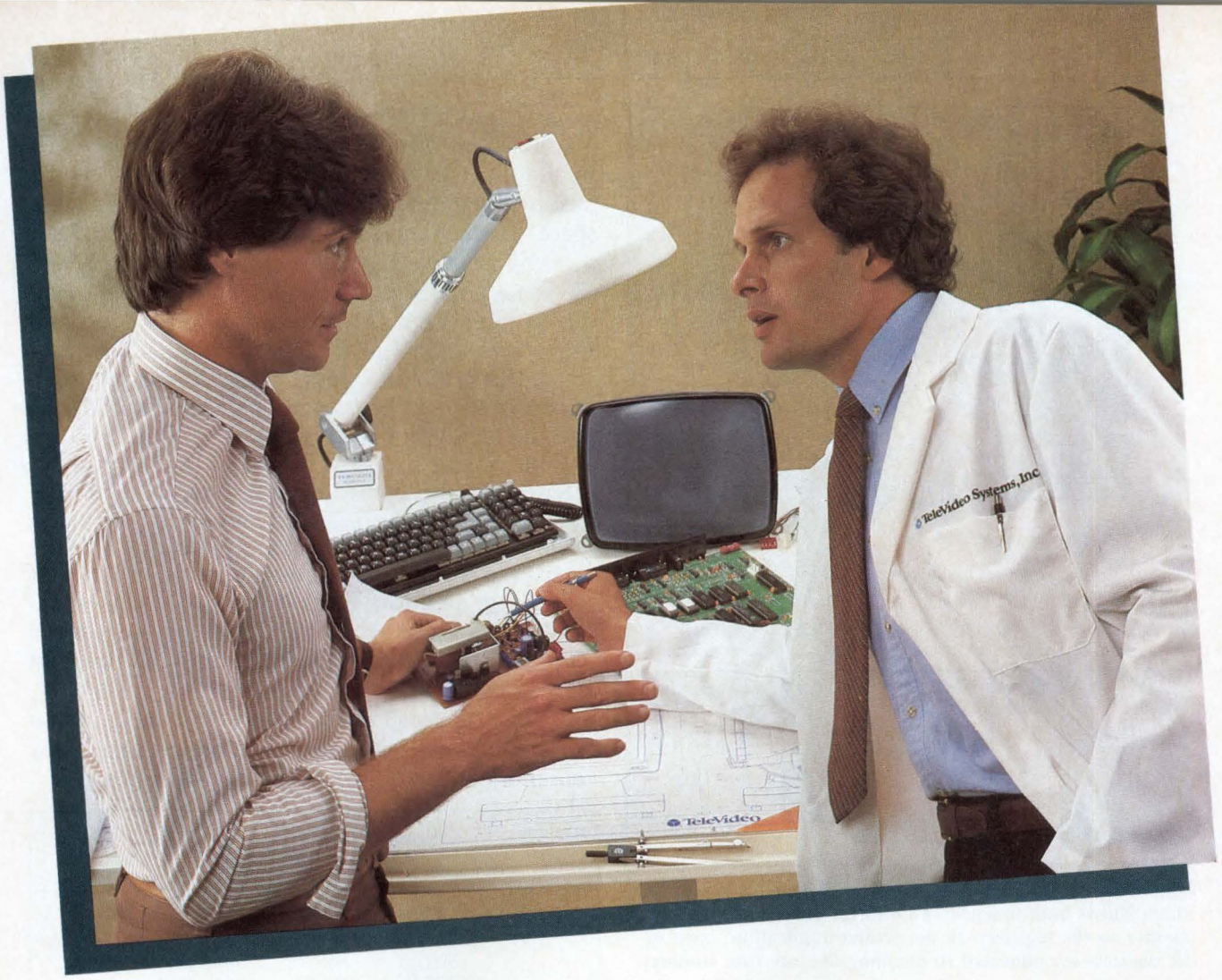
Table 2 illustrates the hardware-level interrupts described above along with the priorities assigned in software for the printer application. The two onboard timers—for carriage and printhead control—have the highest priorities at the software level. Note that the carriage motor is on software level 1 and the dot timer is on software level 2. Reset always occupies the highest level, whether hardware or software.

In addition to the carriage and printhead, the communication tasks are also assigned interrupts, but at lower levels. As shown, the parallel port is on software level 3 and the UART on level 4. The lowest software interrupt priority is assigned to the external system timer.

In any printer system, priorities are assigned on the basis that certain operations must be performed at a specific time. Otherwise, the system fails to operate, while other operations can be performed when time is available. Another consideration is the time required for the operating system to execute.

Each of these factors is variable and depends on the printer and the operations it is designed to perform. For example, the parallel port must have a higher priority than the system timer. This is because the printer needs sufficient time to receive data and then acknowledge its correct receipt to perform the printing task. On the other hand, the system timer does not perform time-critical functions and can be serviced whenever time is available.

The top priority is assigned to the carriage movement because motor-phase voltages are involved. If the motor phases are incorrectly timed, velocity



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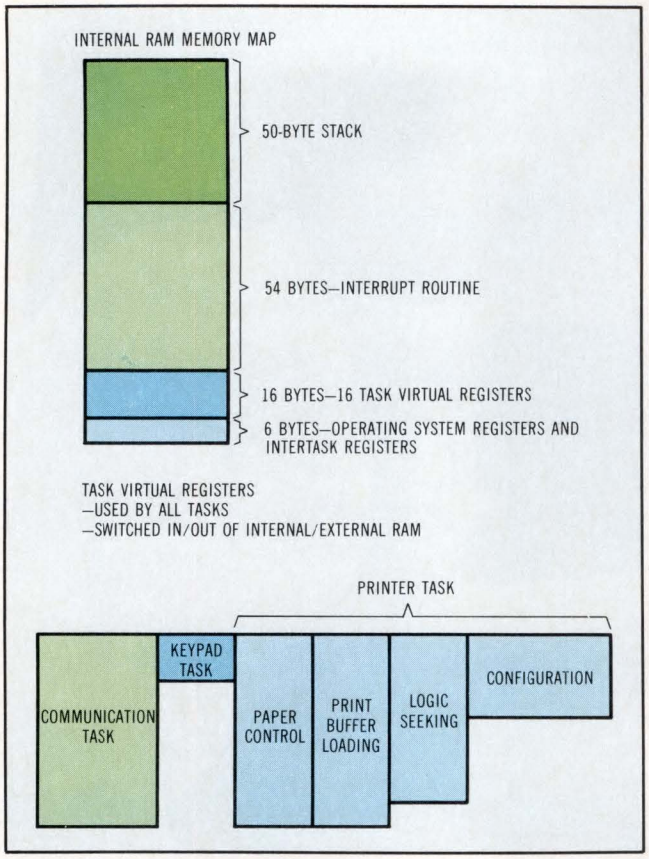

Fig 3 The TMS7041's 128-byte register is memory mapped, which allows both indexed and indirect instructions to operate on the registers. In the printer application, most of the registers are allocated to handling the interrupt routines.

variations will cause motor jitter, resulting in uneven and illegible print. A feature of a high priority interrupt such as carriage movement is its frequent activation. Because of this, and because its activation is likely to interrupt other system operations, such interrupts must be kept very short. Thus, the carriage motor interrupt is about 70 μs (occurring every 800 μs), and the printhead interrupt is approximately 100 μs (occurring every 550 μs). By comparison, the serial-port interrupt occurs just once every millisecond, and when the interrupt activates, it must be serviced within 1 ms. But the keypad's operation is so slow and unpredictable (it depends on an operator) that it does not need interrupts associated with it. It is scanned every 150 ms.

Since the interrupt structure is at the printer operation core, approximately half of the controller chip's 128 registers are assigned to these functions. About 30 registers are used for the stack to execute the operating system commands. All registers are memory mapped so that the chip's 128 bytes of RAM are implemented as general purpose registers. Fig 3 shows the internal RAM memory map. Notice that 16 bytes are allocated as task-virtual registers, and can be shared by each printer task. These registers can be switched in and out of the internal/external RAM.

Communication between the printer and the host is established either through the serial port controlled by the UART or through a parallel port that can be memory mapped in the TMS7041's general address space. The serial port consists of a receiver (RX), a transmitter (TX), and onboard timer 3. To activate the serial port, a set of control words must be sent out to initialize it. These words allow the port to support the desired communication format. The control words establish characteristics of the port such as baud rate, character length, parity (even/odd/off) and the number of stop bits.

Control and access to the serial port is through registers in the controller chip's peripheral file. Table 3 shows the registers associated with the serial port. The SMODE register, for example, is the receiver/transmitter's write-only mode and format register. In addition, the SCTLO register is its write-only control register. The SSTAT register is the receiver/transmitter's read-only status register, and all read operations from register P17 access SSTAT. Since the TMS7041's transmitted (TXD) and received (RXD) data lines are multiplexed on I/O lines, they can be used as I/O lines in the system if needed.

TABLE 3

Registers and I/O Lines

Register	Name	Type	Function
P17	SMODE	WRITE	Serial Port Mode
	SCTLO	WRITE	Serial Port Control-0
	SSTAT	READ	Serial Port Status
P20	T3DATA	R/W	Timer 3 data
P21	SCTL1	R/W	Serial Port Control-1
P22	RXBUF	READ	Receiver Buffer
P23	TXBUF	WRITE	Transmission Buffer

(a)

INPUT/OUTPUT		
Dedicated I/O lines		
—Port A: (INPUT)	AUTO FEED	
	RXD (UART)	
	PAPER OUT	
	SET TOF SET FORMS	
	SET LF	
	SET FF	
	SET ONLN-	
—Port B: (OUTPUT)	CLOCK OUT	
	ENABLE	
	WRITE STROBE	
	ADDRESS LATCH	
	TXD (UART)	
	PRINTHEAD	
	ACKN. -PARALLEL PORT	
	BUSY -PARALLEL PORT	
—Port C: (I/O)	AD0 to A07	
—Port D: (I/O)	A8 to A15	
MEMORY MAPPED		
	PRINTHEAD REGISTER	
	PAPER MOTOR REGISTER	
	CARRIAGE MOTOR REGISTER	
	DIP SWITCH INPUT	
	PARALLEL I/O	

(b)

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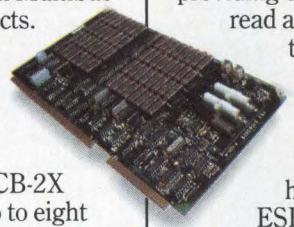

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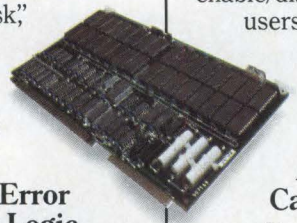

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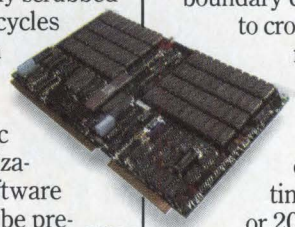

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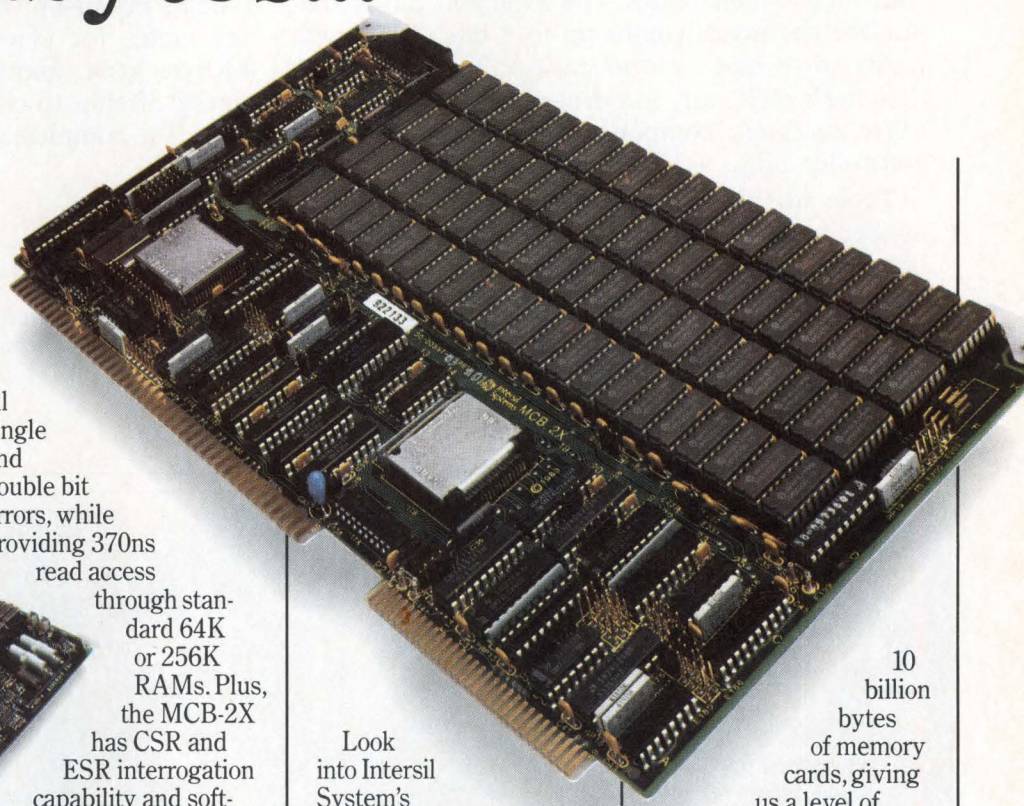

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While timer 3 can be used as a general purpose timer, it is set up as a baud-rate generator for the UART in the printer application. In general, however, the serial port can be driven either by timer 3 or by an external baud-rate generator. The principal advantage of using the internal timer is that its period is software programmable. Thus, a printer could be programmed to operate over a wide range of baud rates—up to 312 kbaud. For the printer, however, a much smaller range is selected—200 to 9600 baud.

The controller chip's UART characteristics—RX and TX—are responsible for its ability to handle a wide range of baud rates. The serial port can accommodate character lengths up to 8 bits (7 bits with parity, or 8 bits with no parity). To simplify the designer's task, only EIA drivers need be added; all other necessary components are included on the controller chip.

Table 3(b) shows how the chip's 32 I/O lines are applied in the printer application. Port A, a bidirectional port, is defined as the system's input port and handles functions such as input from the keypad. Line 5 of port A—called A5—serves as the UART receive line. The overall role of port A is to monitor printer operations.

Port B, an output-only port, controls the parallel port, UART transmissions, the memory bus, and the printhead, among other functions. Ports C and D are the multiplexed lower byte address/data and upper byte address ports respectively. The memory bus uses the C port to send multiplexed addresses and data to the chip, and the D port to send the upper byte of the 16-bit address.

Because of the TMS7041's advanced instruction set, the system firmware centered around the multitasking operating system offers a variety of functions. All of the tasks previously described—printer control, communication, diagnostic capability, and keypad monitoring—are under operating system control. While the code for the operating system, power-up, initialization, and 3 Kbytes of dot tables for characters fits into the onboard 4-Kbyte ROM, another 8 Kbytes of ROM are required offchip to store information for the tasks. Thus, the complete printer runs on just 12 Kbytes of ROM.

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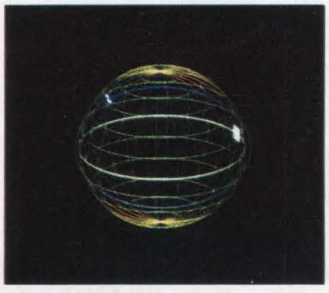

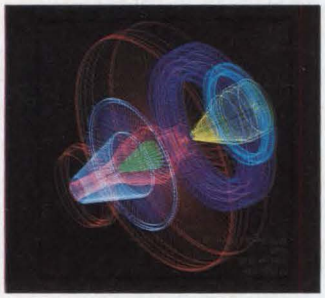

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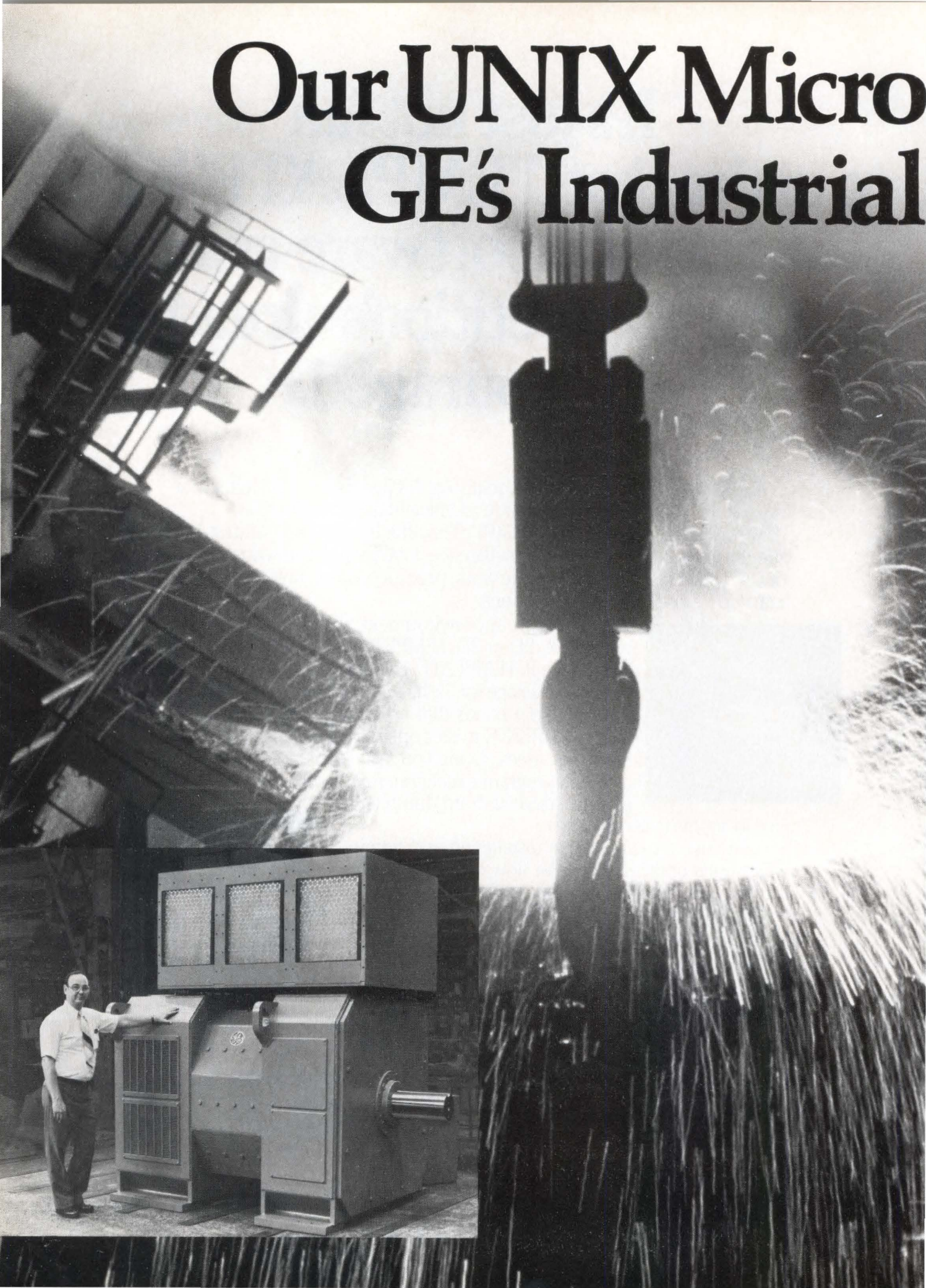

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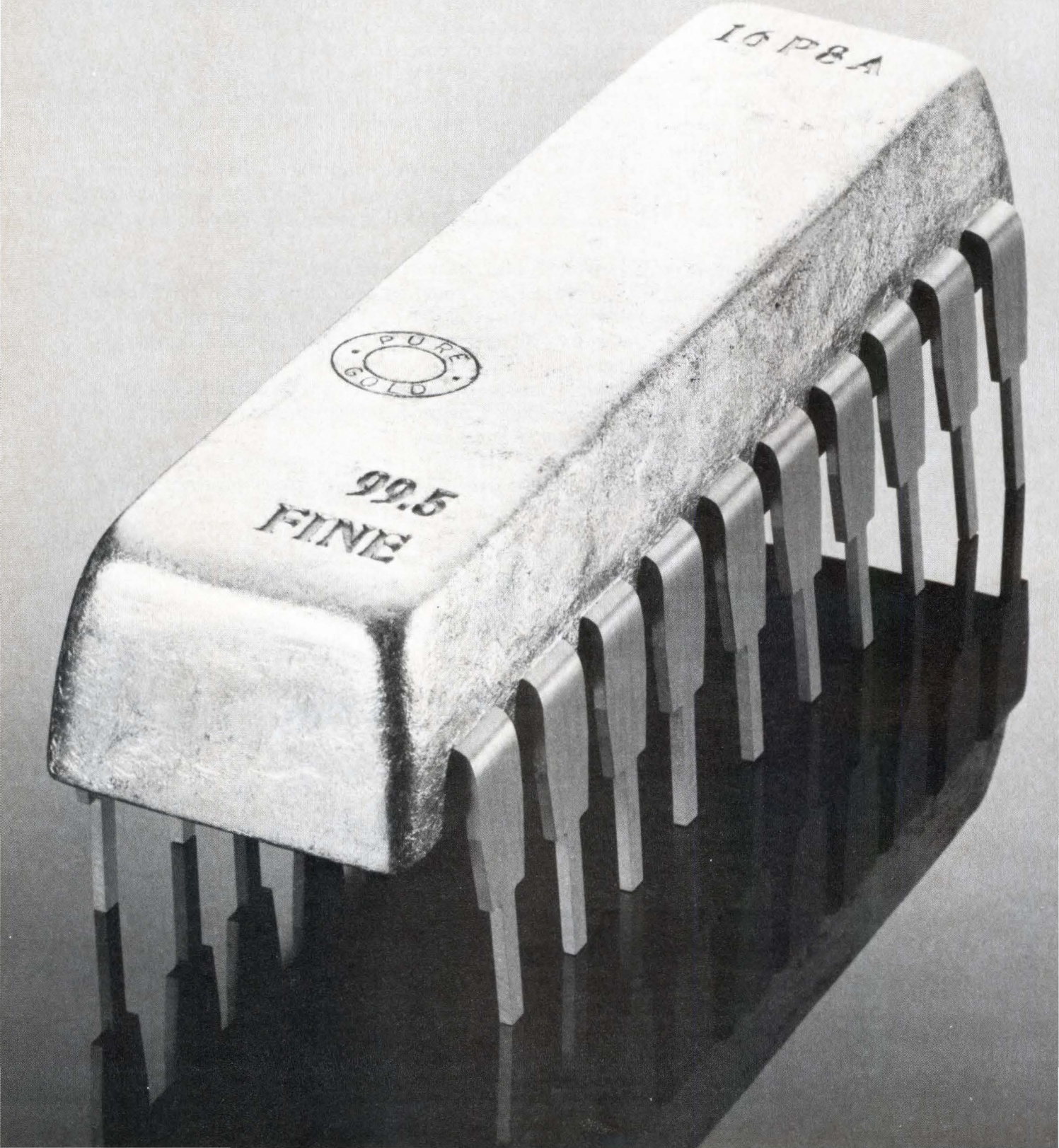

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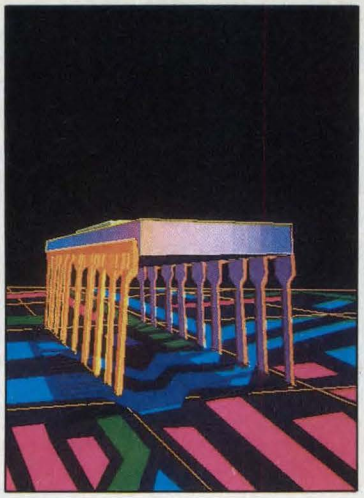

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CIRCLE 80

SPECIAL REPORT ON

ADVANCED DIGITAL ICs

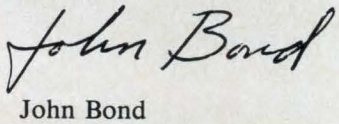
Advances in ICs continue to transform computer systems. As individual ICs themselves become complex systems, the interest of computer system designers grows apace. Consequently, *Computer Design*'s coverage of this important area has grown as well. This issue reflects our commitment to expanded coverage of semiconductor technology and its relevance to system design.

One current hot topic for designers is semicustom, application-specific ICs. These are represented by a range of products positioned between standard logic and full custom chips. Thus, the designer has to make an informed choice among programmable logic devices, uncommitted logic arrays, macrocell gate arrays, and standard cells. To make an intelligent decision, designers must understand the trade-offs in speed, gate density, and power consumption that the different semiconductor technologies permit.

Of nearly equal importance is the organization of the chosen semicustom chip because it can cause dramatic differences in throughput even though the gate delays of two competing designs may be the same. Related factors include the computer aided design tools available from competing manufacturers. These can have a noticeable effect on the time it takes to see silicon for a particular design. Moreover, a product's development time is perhaps the most important factor to be examined. Time and cost considerations are, after all, the main criteria used in deciding which type of logic device to go with in the first place.

Of course, there is more to advanced ICs than semicustom devices. As the total available market for particular functions reaches a reasonable level, the semiconductor companies design VLSI circuits to fill those niches. These complex VLSI circuits give designers new tools to develop systems. Until recently, disk controllers, alphanumeric CRT controllers, graphics display controllers, and digital signal processors were just a few of the chips typically implemented on boards. These VLSI systems have had to be developed to match the scale and performance of the ubiquitous microprocessor.

Sometimes, however, the performance of microprocessors is insufficient for high performance computer systems. Advances in bit-slice processor technology take care of high end performance and prove that advanced digital ICs have something for everyone.



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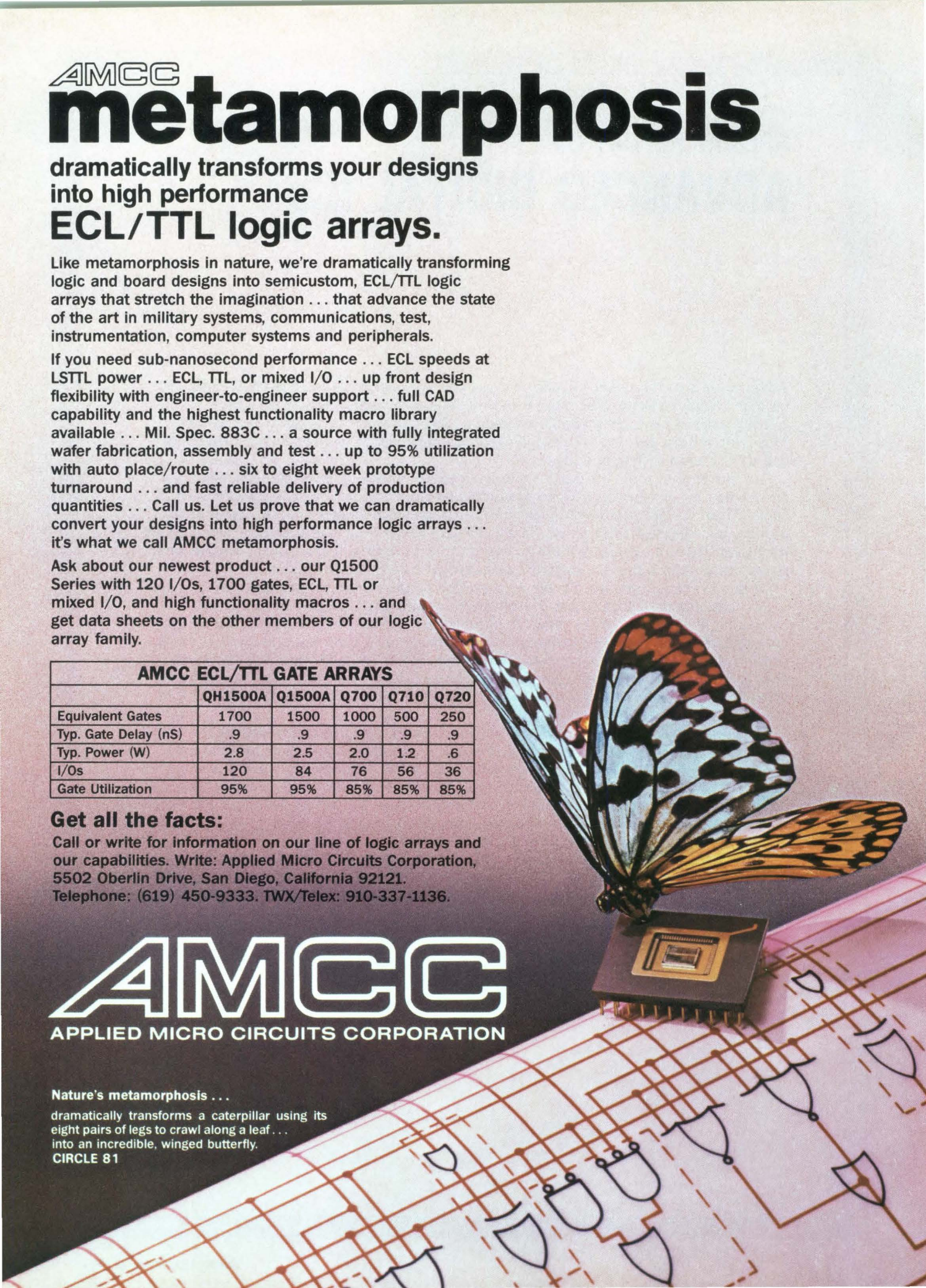

Nature's metamorphosis . . .

dramatically transforms a caterpillar using its eight pairs of legs to crawl along a leaf . . . into an incredible, winged butterfly.

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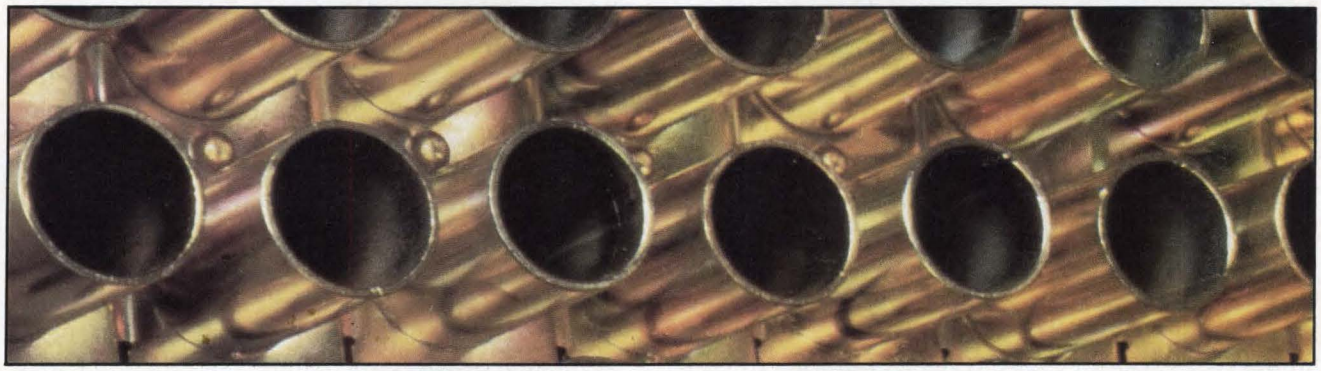
SEMICUSTOM CIRCUITS ARRIVE

With components becoming chip-level VLSI systems, the need for higher density logic to tie these systems together has sparked an explosive growth in application-specific ICs.



by John Bond,
Senior Editor

In the progress along the road from discrete transistors to silicon nirvana, application-specific ICs are a major step. They represent the future for logic. Programmable logic devices, gate arrays, macrocell arrays, standard cell libraries, macrosystems, and custom circuits all have a place in the logic hierarchy. Consequently, designers must understand the differences and trade-offs among these, as well as their relationship to standard logic.

Until recently, the very success that semiconductor manufacturers enjoyed in the development of standard logic slowed the acceptance of application-specific ICs (ASICs). Standard prepackaged circuits were responsible for the initial popularity of TTL logic. This, in turn, spawned other bipolar families using the same standard functions—Schottky, low power Schottky (LS), and more recently, advanced versions such as advanced low power Schottky (ALS), advanced Schottky (AS), and Fairchild advanced Schottky technology (FAST). These logic blocks are now available in high speed CMOS (HCMOS). Moreover, for those requiring blinding speed, the current switching family of ECL devices is available.

Yet, despite the continuing acceptance of standard logic, there is a growing need for higher levels of integration than can be provided with standard logic blocks. This becomes more apparent as VLSI pushes ever larger circuits onto single chips (eg, microprocessors, microcomputers, dense memories, disk controllers, coprocessors, data communication circuits, in short, almost anything with a general enough usage to be economically produced in high volume). That still leaves an enormous area uncovered by VLSI.

Until the last few years, unique, user-specific applications either had to be done in custom chips or implemented in standard logic. Since most users have neither the necessary volume nor the time for full custom designs, standard logic continues to be used for most application-specific functions. Of course, VLSI functions have to be tied together with something, usually SSI/MSI standard logic "glue."

Against this background, manufacturers have started making a wide variety of uncommitted logic that can be programmed by either the system designer or the manufacturer to implement user-specific functions. There is, understandably, a certain amount of resistance at first to the close customer/vendor relationship this entails. After all, users must give up much of their design autonomy to the data

base in the manufacturer's computer aided design (CAD) system.

Furthermore, there has already been some early fallout that has left users exposed. As recently as a year ago, Texas Instruments (Dallas, Tex) was touting the TAT-10 and TAT-20, 1000- and 2000-gate Schottky transistor logic (STL) arrays. The products ultimately proved unmanufacturable and TI had to remove them from the market. Although this temporarily hurt customers who had committed to the products, and left TI's reputation somewhat tarnished, the experience gained was extremely important to TI's present strong position in ASICs, especially in the area of sophisticated CAD tools.

Despite such false starts, 1983 was a banner year for semicustom circuits. Not only did the traditional semiconductor manufacturers enhance their position in this market with a stream of new products, but it seemed as though new vendors sprung up daily. Some of these are little more than silicon foundries, but others bring new techniques and expertise to the game (see Table 1). Thus, after several years of slow starts and user resistance, ASICs are finally taking off.

Application-specific circuits

The technology is settling down to a mainline process of HCMOS, with ECL or other bipolar technologies providing the extra high speed needed for certain applications. Despite this, there are numerous variations within the technology to confuse the potential ASIC user. A solid understanding of ASICs will therefore be as important to system designers as logic design has been with the standard logic families.

With ASIC growth accelerating, industry sources estimate that it will account for a third of the total IC market by 1985, and nearly half of the dollar volume in ICs by 1990. This growth will continue because ASICs permit customized, innovative products while reducing size and increasing reliability. Also, the user has the opportunity to design unique products that are not easily copied.

Programmable logic devices are at the lowest complexity level of application-specific devices. This category includes user-programmable or mask-programmable logic devices, as well as some types of PROMs. The next steps up in density or complexity are gate and macrocell arrays. Above these are standard cells. Then, there are macrosystems or functional blocks that are enlarged standard cells—eg, a microprocessor core, memory, ALU, and A-D converter. Finally, at the top of the ASIC hierarchy are full custom designs (Fig 1).

Programmable logic devices can be used for simple random logic. Gate arrays or standard cells are used largely where large logic blocks are to be integrated, such as in mainframes and superminicomputers. Because they offer a less expensive and more timely way to develop ASICs, programmable logic devices have met with considerable success. Engineers like them because they can program the devices themselves and not lose control of the design. Also, computer programs to develop the correct fuse patterns are readily available.

Monolithic Memories, Inc (Sunnyvale, Calif) is the major player in this low end of the ASIC field. The programmable array logic (PAL) was invented by the company and is its trade name. Advanced Micro Devices (Sunnyvale, Calif), National Semiconductor (Santa Clara, Calif), TI, and Motorola (Phoenix, Ariz) second-source PALs. Each PAL can replace up to 12 logic chips. Signetics (Sunnyvale, Calif) makes field programmable logic arrays (FPLAs). PLAs were the first such devices on the market and are similar to PALs and FPLAs. There is also a variation called hardwired array logic (HAL). HALs, however, are mask programmable rather than fuse programmable. Consequently, they are more like ROMs than PROMs, while most programmable logic devices are fuse programmable like PROMs. HALs are slightly faster but they are, of course, not programmable in the field. Just as ROMs often replace PROMs or erasable PROMs as the design solidifies and the volumes grow, HALs may be used to replace PALs.

PROMs and programmable arrays use similar technology except that they are organized differently. However, there are devices called registered PROMs that include registers and can be used for some logic functions, thus blurring the distinction between the two. Of course, programmable logic devices are used mainly for logic applications and PROMs for memory. Any type of glue function that is not too large can be done simply with programmable logic. There has been an increasing use of programmable logic devices for a variety of other applications as designers learned how to use them effectively. For example, the use of PLAs is growing with the expanding use of state machines, which have a variety of applications such as counters, adders, and standalone controllers.

The primary function for which programmable logic devices are being used most effectively is in the replacement of SSI/MSI logic parts. The short development cycle, low cost, and off-the-shelf availability make these devices very attractive. However, speeds in programmable logic devices are not as fast as gate arrays. Typical input to output speeds are 25 to 50 ns in programmable logic. When programmable arrays become available in ECL in the near future, they will be much faster.

A new type of fuse-programmable logic device, combining some of the features of both programmable logic and gate arrays, was recently announced by Advanced Micro Devices. The Am PAL22V10 can replace logic with 500 to 1000 gates. More importantly, although it is similar to other PALs in that

it has an array of AND gates, the output section consists of macrocells, like a gate array. These allow the I/O pins to function as input, output, or bidirectional ports. Pins can act sequentially or in combination, and with either active highs or lows. This allows the architecture to change to suit the application. The worst-case input to output delay is 25 ns.

A gate array may contain from several hundred to many thousands of uncommitted gates waiting for the last mask or two to tie these together into

TABLE 1

Semicustom Competitors Organized by Performance and Technology

	Typical Gate Delay					
	1 ns	1 to 2 ns	3 to 5 ns	6 to 9 ns	10 to 15 ns	15 ns
Standard Cells	—	Alphatron Hughes MCE NCM Plessey Signetics Silicon Systems Toshiba Universal Motorola	Alphatron AMI Array Technology Circuit Technology Fujitsu Harris IMP Master Logic MCE NCR NCM RCA Signetics Synertek Toshiba VTI Zymos	RCA	AMI Integrated Circuit Systems MCE Plessey RCA Zymos	Integrated Circuit Systems Master Logic
Bipolar Gate Arrays	AMCC AMD Fairchild LSI Logic Motorola National NEC Plessey Signetics	Fairchild Fujitsu Harris Motorola National NEC Plessy	Ferranti/ Interdesign Raytheon Signetics TI	Fujitsu	Custom ICs Harris	Cherry Exar MCE
CMOS Gate Arrays	—	AMI Fairchild Fujitsu GE-Intersil Hughes IMI Integrated Microcircuits LSI Logic Microcircuit Technology Mostek Motorola National Plessey Siliconix Toshiba Universal	AMI Array Technology Barvon California Devices Circuit Technology Custom MOS Arrays Exar Fairchild Fujitsu General Instrument GTE Harris IMI LSI Logic Master Logic Mitel NEC Plessey RCA Semi-Processes STC Telmos	Exar Fujitsu GE-Intersil Interdesign NCM Plessey RCA Signetics Telmos TI	California Devices Integrated Microcircuits Interdesign Telmos	IMI Master Logic MCE Microcircuit Technology RCA

Table is based on material supplied by Applied Micro Circuits Corp (AMCC), San Diego, Calif.

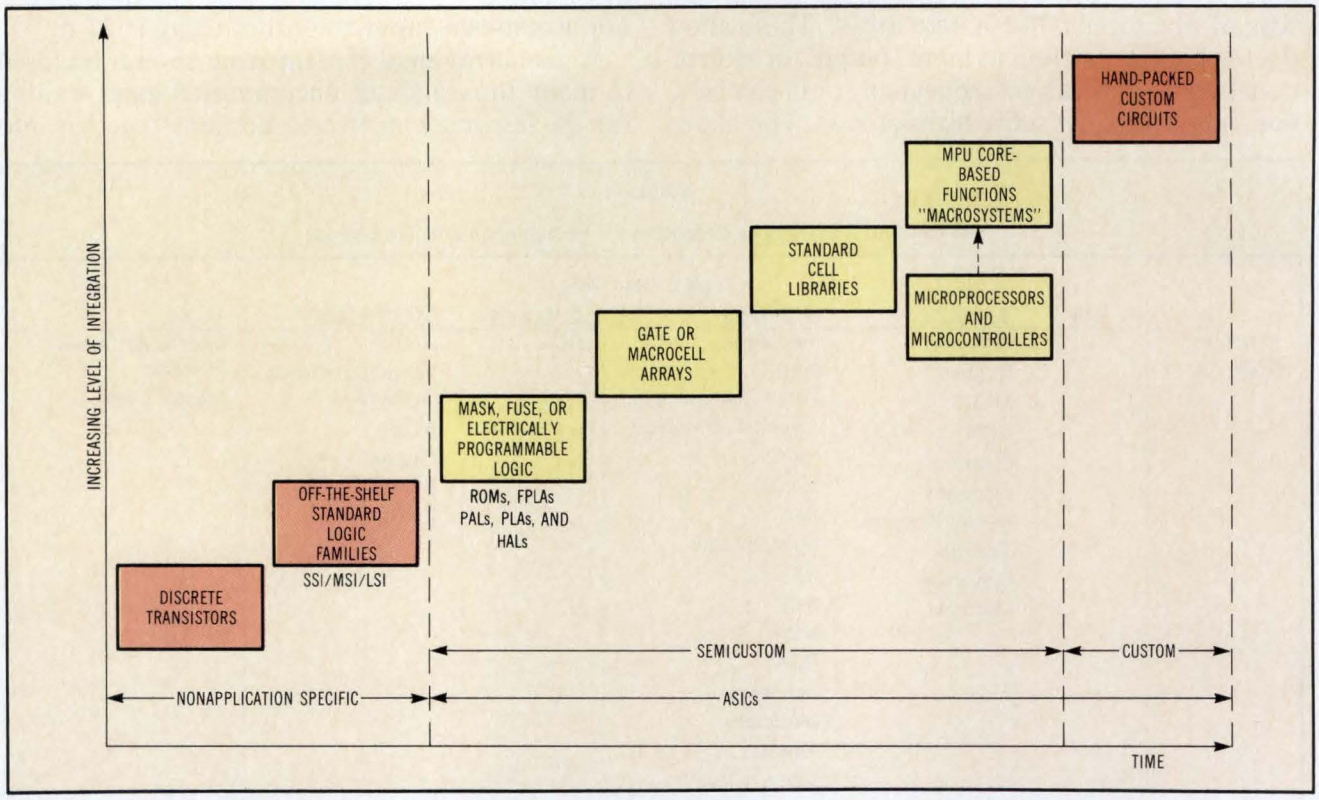


Fig 1 The logic migration path shows the increasing level of integration from discretes and standard logic through the various levels of semicustom logic to full custom circuits.

a circuit. Such an uncommitted logic array (ULA) is known as a sea of gates. More common in gate arrays today is the use of a macrocell approach. Each macro is a preselected logic function that fits into a standard-sized cell. Very few manufacturers are still building ULAs, and even where they do, standard selectable library functions exist in software. In effect, they use software macros rather than hardware macros.

With hardware macrocells, whenever a macro is called up on the CAD system, it appears on the screen, totally precharacterized. In such a macrocell array library, each macro is totally characterized when designed. Wherever it is put on the chip, it always remains the same, fitting into a major cell geometry slot. The only thing that differs is the length of the interconnects between macrocells.

In an uncommitted gate array, the CAD system can pick gates in different parts of the chip to build a logic function. However, if a second layout is required, the logic will probably be routed differently. Therefore, performance will vary within macros as opposed to just between macros. Thus, the major advantage of macrocell arrays is that they are fully precharacterized. For that reason, it takes less time and costs less to use hardware macrocells than to design uncommitted array logic.

There are those who disagree, however, finding macrocells to be an inefficient use of silicon. One company that has taken the "sea of gates" concept the furthest is California Devices, Inc (San Jose, Calif). The company has developed a new architecture of two-layer metal CMOS arrays. The DLM series of gate arrays is essentially a channel-less geometry that eliminates internal wiring of channels by folding the channel interconnects over active cell areas. The array is designed from the top down with the required interconnects determined first. Transistors are arranged to conform to the interconnects and are joined by short, straight lines into the logic cells, which virtually disappear in a "sea of gates."

By providing a larger ratio of active area to interconnect area, this technique can cut die size in half. This rivals the size, performance, and cost of full custom and standard cell devices. California Devices currently makes a 990-gate chip with the technology and plans to offer arrays up to 10,000 gates. Despite the advantages of channel-less "sea of gates" design, the most common approach continues to be macrocell and California Devices itself exploits that logic arrangement with its older HC series.

Swimming in the mainstream

There can be no question that the mainstream semiconductor technology for arrays has become HCMOS. Yet, where brute speed is required, bipolar still rules, and the fastest of the fast remains ECL despite power consumption and the need to remove the heat generated. Thus, a typical lineup of arrays for semiconductor companies includes a family of CMOS arrays as well as a family of high speed bipolar arrays.

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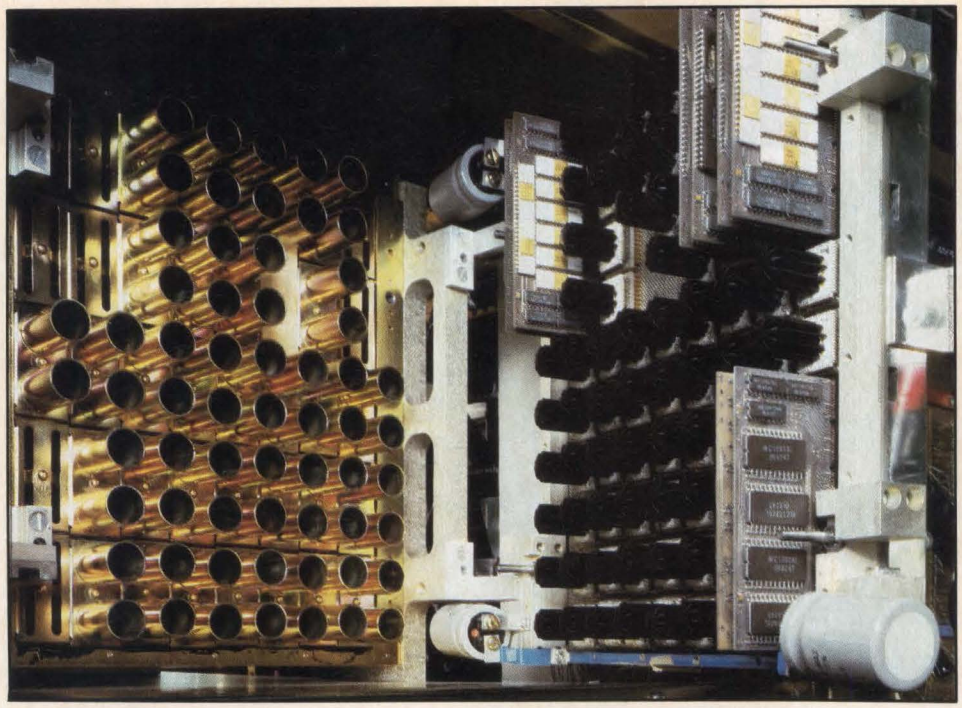

Fig 2 The ST-100 array processor from Star Technologies Inc achieves its 100-million floating point operations/s performance by using ECL macrocell arrays. To cool these arrays with a black heat sink mounted on each, the hinged processor board shown is swung inward to mate the heat sinks with the brass duct nozzles. This directs cooling air from an air plenum over each heat sink and the arrays.

Motorola and National Semiconductor are representative of this trend. The two companies provide second-sourcing for each other and make three types of macrocell arrays—ECL, advanced low power Schottky (ALS), and HCMOS. Maximum size and typical gate delays for each are 2472 gates and 0.3 ns for ECL; 2800 gates and 1 ns for ALS; and 4800 gates and 2 ns for HCMOS. Each manufacturer uses a 3-micron HCMOS process, but both are well on the way to implementing a 2-micron process.

As noted, the largest ECL array, the 2472-gate MCA2500ECL, has a typical gate delay of 0.3 ns (0.5 ns maximum). By powering down to 2.5 from 6.5 W, as is done in the ALS versions, the same ECL gates have a typical speed of about 0.6 ns. Also, the ECL gates are surrounded by slower ALS buffers. (Typical input receiver delays are 1 ns and output driver delays are 5 ns). The result is that those requiring full ECL speed must use the MCA2500ECL, which requires a heat sink, while the lower power MCA2800ALS does not.

The need to cool ECL gate arrays has generated some interesting solutions as the picture of the Star Technologies (Portland, Ore) array processor will attest (Fig 2). Because of this and higher density, HCMOS will be the dominant technology in gate arrays, as in processors and other areas. Yet, the future is still bright for selected high speed applications of ECL, at least until CMOS speed approaches ECL.

There is a possibility that gallium arsenide will find a position in high performance devices. Tektronix (Beaverton, Ore) has announced that it will enter the foundry manufacturing of very high speed GaAs analog and digital circuits. This will include arrays of up to 500 gates and custom circuits. Nonetheless, HCMOS is the fastest growing technology and it will eventually supplant most bipolar, including much of ALS and probably all of standard low power Schottky.

Semiconductor technology aside, there is another issue that causes differences in performance between arrays—layout of the macros. For example, simply wiring a macro in series through each gate adds the gate delays and slows throughput. To avoid this, some ECL arrays use a technique called series gating. This is done by putting gates in series vertically from source to ground with a common source to the gates. The technique lowers power consumption and enhances speed because of fewer transistor switches.

As a result, a macro that takes 1 ns to accomplish its function in an array with series gating might take 4 ns in a similar array without it. By the time macros are connected, there can be considerable delays in competing macrocell arrays. Here, properly designed hardware macrocells may have an advantage over the uncharacterized software macros of ULAs.

In either case, both types are gate arrays and share many of the same benefits and drawbacks. The benefits are high speed (compared to programmable logic devices); a variety of array sizes for efficient utilization of chip area; CAD systems to help develop the chips; and a variety of process technologies available to give users a choice of speed, power density, output drive, and cost. Macrocell arrays offer the added advantage of a comprehensive library of SSI/MSI building blocks.

However, there are drawbacks to gate/macrocell arrays. The unit costs of chips are high and the macros available are similar only to the lower end

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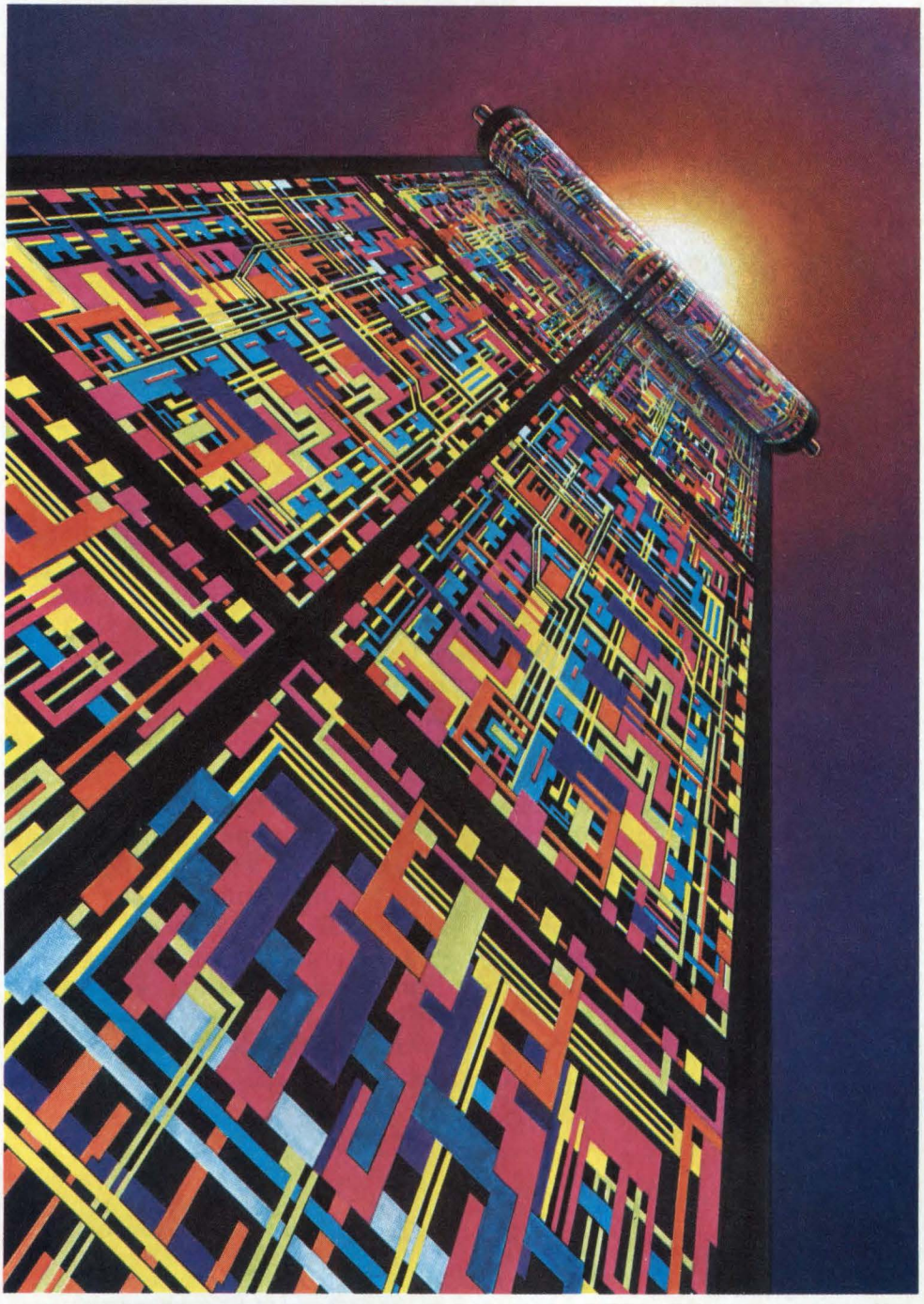

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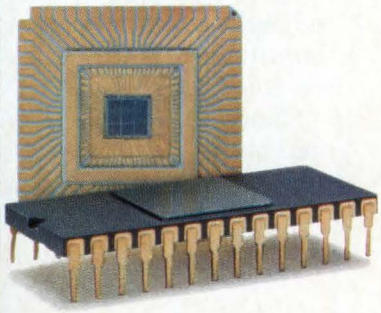

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*ULA is the Ferranti brand name for uncommitted logic arrays and is a trademark of Ferranti plc.

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TABLE 2

Spectrum of Technology Choices

	Programmable Logic	Gate/Macrocell Arrays	Standard Cell/ Macrosystems	Hand-packed Custom
Chip Density	a few gates	from 16 gates to 20,000 gates	from hundreds to many thousands	from hundreds to many thousands
Percent of wafer preprocessed	100 percent	80 to 90 percent	0 percent	0 percent
Time to prototypes in 1983	off-the-shelf	7 to 13 weeks	13 to 26 weeks	39 to 104 weeks
Option development cost per chip (depends on complexity)	none	$10,000 to 40,000	$40,000 to 100,000	$100,000 to 500,000
Ability to make design changes or corrections	Minimal cost	Easy, fast, and inexpensive	Easy, but somewhat more expensive and slower than arrays	Hard, slower, and more expensive than standard cell/ macrosystems
Unit cost of chip	low	high	medium	lowest

of the logic family spectrum. More complex logic functions have to be built by combining macros. For something more akin to building systems with standard logic families, standard cell libraries come closest (Table 2).

Standard cell libraries

Gate/macrocell array wafers are 80 to 90 percent prefinished and require only the last one or two metal layers to be complete. From the beginning of the design to prototype now takes an average of 7 to 13 weeks. If production volumes are expected to be higher and time to prototype is not too critical, then a standard cell approach can be more cost effective. Like fully custom circuits, standard cell designs are not preprocessed, but customized for the user from the beginning of the production process. Unlike custom circuits, they use standard, predefined cells and are consequently much faster to develop.

Standard cells also have an advantage over the macrocells they somewhat resemble. Macrocells are all the same size. Each macro function fits into the same size cell. It may not use the full capacity of the cell, or it may be limited to the number of gates that can fit into the cell. Thus, macros are limited to SSI and smaller MSI logic functions with larger MSI circuits built from combinations of macros.

In a standard cell, not all of the macros are the same size. Each is designed from the ground up to perform a certain function, with no more silicon than is needed, and then placed in the standard cell library. Because each cell is hand-packed, it wastes less silicon. Furthermore, it does not have routing channels, so each die is a different size depending on the system function that is implemented. A standard cell device takes longer and costs more than a gate array to develop, but the cost per chip is less. Simply put, standard cells are more silicon efficient and gate arrays are more time efficient (Fig 3).

Carried to their logical conclusion, cell libraries can contain very complex cells that might include memories and microprocessor cores—macrosystems.

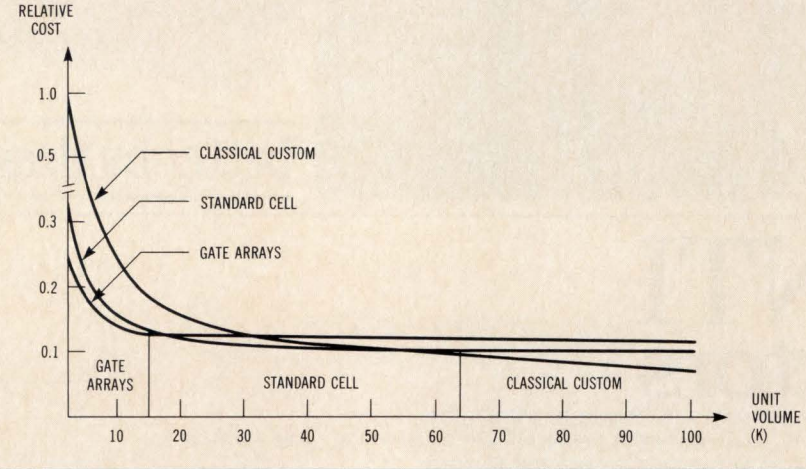

Fig 3 Unit volumes determine the relative cost of ASICs. The intersections of the curves indicate the volumes at which gate arrays, standard cells, and custom design approaches start to make economic sense.

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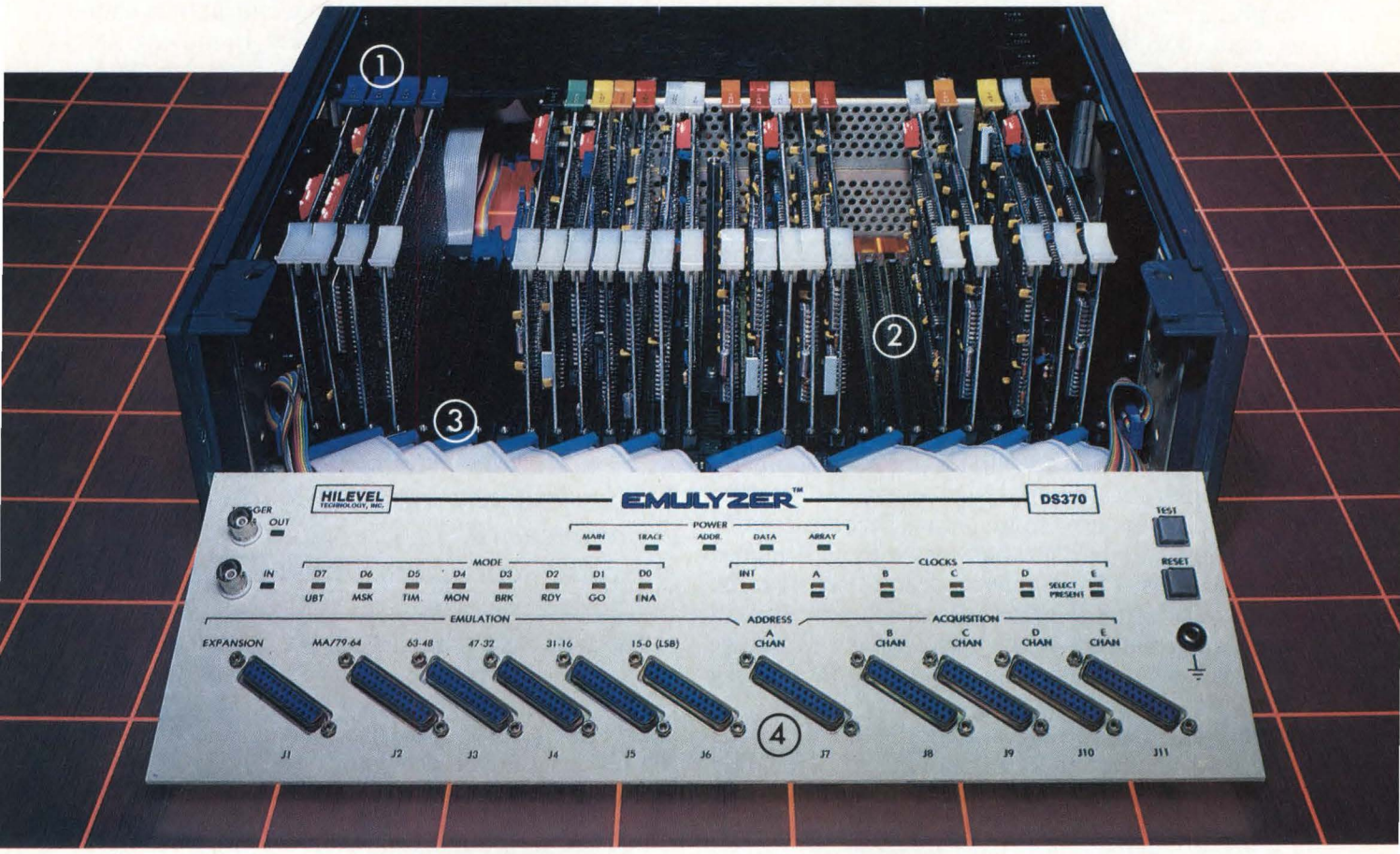

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Such macrosystems can be nearly as unique as full custom devices. Yet, because they are built from previously designed fully characterized logic, processor, and memory circuits, development time is much faster. They are easily tailored to specific applications. Since the number of interconnections is fewer, such circuits are intrinsically more reliable. Finally, as with gate arrays, it is relatively easy to get back into the CAD data base to modify the design with a software change.

Logic designers with no IC design experience will feel more at home with standard cell/macrosystem design. This is because the cell functions are more analogous to standard logic functions than uncommitted gates or even the higher level of integration found in macrocells.

Logic modules of different sizes and shapes have been designed by custom chip designers to avoid "reinventing the wheel" each time a new chip was designed. Thus, companies with considerable custom design experience often have large libraries of logic functions that can be adapted to cell libraries. Synertek (Santa Clara, Calif) is one such company with extensive custom IC design and manufacturing experience. Not surprisingly, it has become a major force in the standard cell business with its 3-micron CMOS process. (The 3-micron-feature cells can be scaled without redesign to a 2-micron process—an important point for those wishing to take advantage of semiconductor technology advances without going through a major redesign.)

Synertek's cell library is a good example of the variety of functions that can be obtained. It includes the usual gates, inverters, flipflops, and I/O pads that are available in macrocells. It also contains RC oscillators, Schmitt triggers, RAM, ROM, universal asynchronous receiver/transmitter (UART), D-A converter, 6502 microprocessor core, and numerous other cells and variations on those cells. A designer can build everything from simple logic to microprocessor-based macrosystems. Although logic designers might be more comfortable with standard cell design than with gate arrays, it is still different than designing a PC board with standard logic.

A cell library design cycle includes computerized schematic entry, logic simulation, placement and routing, electrical network continuity, and design rule checking. A whole new set of skills is required to really be considered expert. Most suppliers recognize this and offer different levels at which customers, from neophyte to expert, can be involved in the design process.

Chip-level standard logic cells

Why not just make standard cells that are a direct copy of standard logic? Then it would be a simple matter to order up something like a 74S299 8-bit shift register or a 74S182 lookahead carry generator, add some other parts, and tie them all together according to the schematic. Unfortunately, it is not that easy, since it is necessary to deal with numerous IC subtleties.

In the first place, the cells will have different characteristics than standard logic parts, and even those characteristics can be changed by altering cell size. Also, cell placement is much more critical on a chip than part placement on a PC board. In moving the circuit from PC board to chip level, there are many pitfalls, with race conditions and other timing anomalies as the most likely results. Nonetheless, the idea has such obvious appeal that it was only a matter of time before someone found a way to do it.

Using 3-micron CMOS technology, TI recently introduced its SN54/74SC family of standard cells. These cells are IC-level versions of SN54/74TTL logic functions. At present, the family only includes the most popular functions, but those will be expanded over time. This year, all functions of the SN54/74HC HCMOS logic family will also be available in standard cells.

Logic designers with no IC design experience will feel more at home with standard cell/macrosystem design.

The SN54/74SC standard cell is compatible with a predefined interconnection grid. Just as standard logic components are placed on a PC board interconnection grid with 0.1-in. spacing, the standard cell functions are implemented on a silicon chip with 9-micron (.000353-in.) spacing. Thus, engineers can design standard cell ICs using traditional TTL and PC board design techniques, and without learning the intricacies of IC design.

None of this is as easy as it sounds. It requires the use of very sophisticated computer-based design tools and considerable help from TI designers. Even for a given logic function, there are trade-offs in the physical cell design. For example, power dissipation and fanout capability are directly related to die size. Larger cells provide higher performance at the expense of overall size. This has to be taken into consideration by the design system and the manufacturer's IC designers.

Given the customer's logic diagram, TI describes the performance of the SN54/74SC functions under typical and worst-case conditions, and then does the chip layout using standard cell functions. Each function is represented by multiple physical cells with varying output drive and size. Minimum size cells that conform to the customer's specification are selected for each function. Thus, the customer's logic designer ends up with a semicustom chip offering low power Schottky equivalent performance, while avoiding actual IC design. The vendor provides that

service. However, if logic designers require better than low power Schottky equivalent performance, they may have to get involved in cell selection and placement to achieve those performance goals.

Custom chips and other considerations

Standard cells are aimed at the midrange volume user—from approximately 15,000 to 65,000 units per year. At these volumes, lower unit costs balance off higher development expenses to make standard cells more cost effective than gate arrays. Unit costs are lower because a standard cell design is always smaller, typically by 30 percent, than a gate array version of the same circuit. However, the full custom approach typically saves another 25 percent in size over a chip built from a standard cell library.

Thus, a custom chip is usually the best choice for high volume, price-sensitive applications. Of course, that only applies if you have the time to develop a custom circuit. That is often not the case in a hotly competitive environment where time-to-market is critical. Yet, for those who meet the basic requirements, the optimized silicon area of custom circuits means lower unit costs to balance off high development costs. Furthermore, since parts can be fully customized, the user can bring unique products to market.

Gate arrays/macrocells, standard cell libraries, and full custom chip design depend heavily on computer design automation. The progress thus far would not have been possible without such systems, as can be illustrated by a typical VLSI design problem. A 256-Kbit dynamic RAM has over 500,000 transistors. If the chip were to be designed manually, it would take an enormous amount of time. For example, allowing 2 min per transistor, design rule checking alone would take nearly 17,000 hours. Thus, the development pace for VLSI and especially ASICs is greatly influenced by computer design automation. Progress in this area will have as great an effect on growth as the advances in semiconductor technology.

There are a number of pieces to the design automation puzzle, although software addressing many of those problems already exists. CAD systems carry the designer from layout to the mask-making data base. Programs exist to generate mask patterns from the data base. There are algorithms to do logic simulation, transient analysis, design rule checking, schematic entry, logic extraction and verification, placement and routing, test pattern, and test program generation, etc. Unfortunately, many of these design tools run on different systems, using different languages and data bases running under different operating systems.

The industry is working to develop more integrated design systems, and considerable progress has been made in that direction. However, the present fragmentation of design tools that can exist within one manufacturing organization points up a problem of which potential ASIC users should be aware. Primary and second-source vendors should both use the same design tools. There are IC manufacturers who make a point of this and it should be an important factor in vendor selection.

ASIC technology is on the way to supplanting standard logic families. Advances will occur in speed and density, but just as important is progress in design automation tools. With increased density, better testing methods, including onchip test structures, will become increasingly critical. As ASIC technology becomes more pervasive, true commodity-style second-sourcing (including design tools) will become more common. Finally, although replacing digital logic will provide the impetus for the ASIC revolution, analog functions are already appearing in gate array macros and standard cells. The future of ASICs points to more of such integration.

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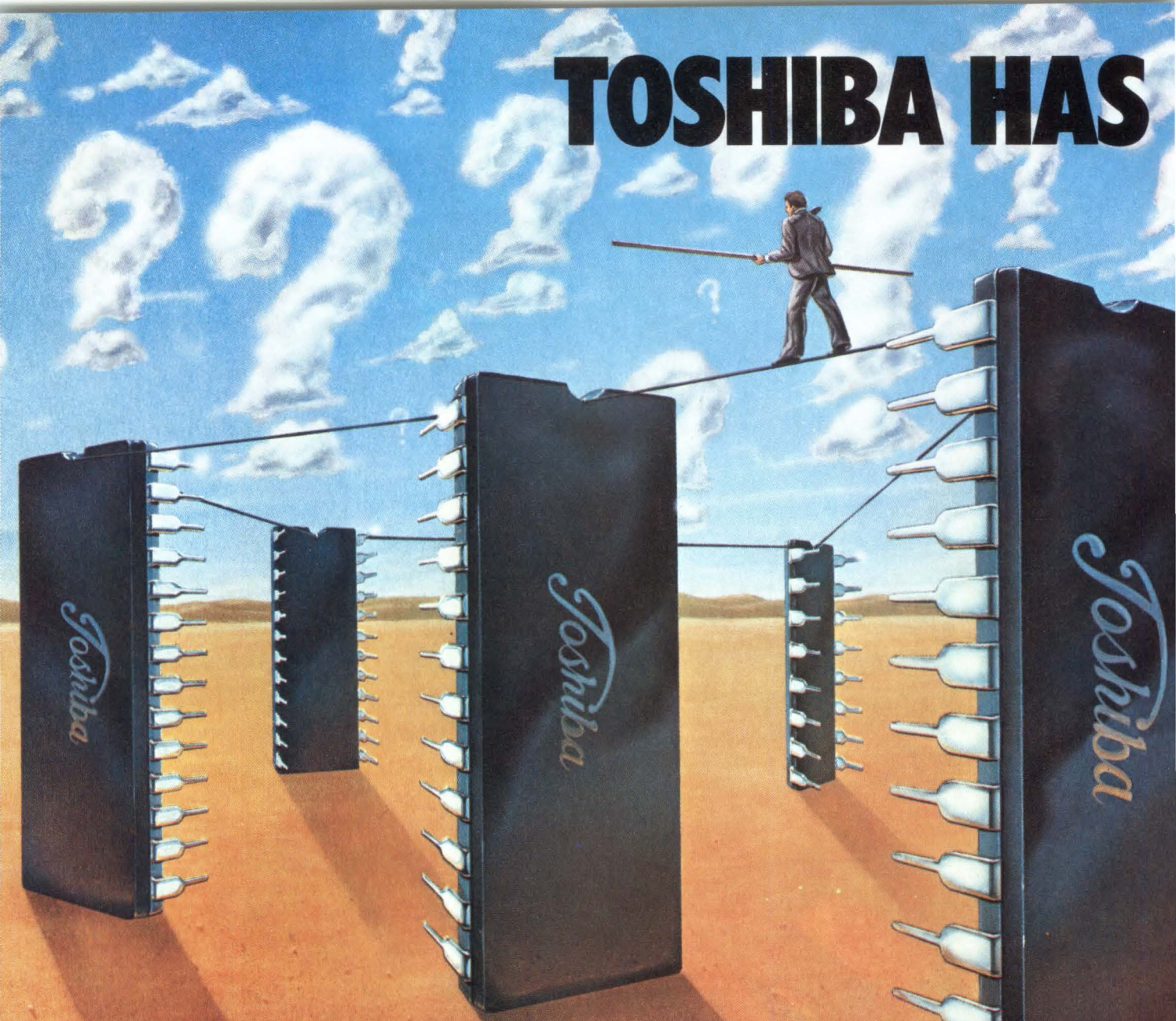

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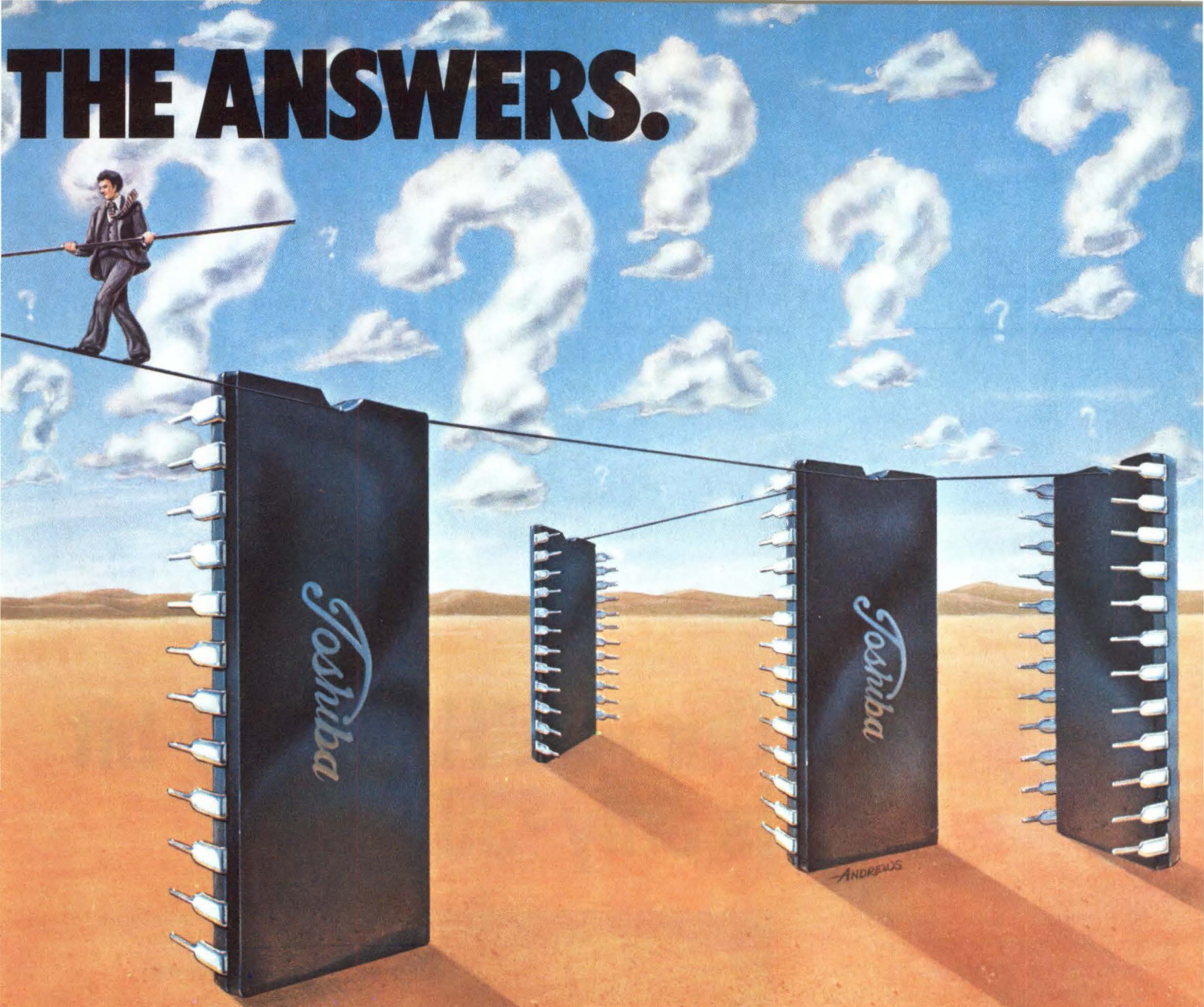

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Max. Clock Freq. (typ) J/K F•F (C_L= 15pF)	60MHz	45MHz	20MHz	2MHz
Quiescent Power Diss. (typ) (GATE)	0.01μW	8mW	0.01μW	0.01μW
Noise Margin V_{IH} (min)/V_{IL} (max)	3.5V/1.5V	2.0V/0.8V	4.0V/1.0V	3.5V/1.5V
Output Current $\|I_{OH}\|$ (min)/I_{OL} (min)	4mA/4mA	0.4mA/4mA	0.36mA/ 0.8mA	0.12mA/ 0.36mA
Op. Volt. Range	2-6V	4.75-5.25V	2-8V	3-18V
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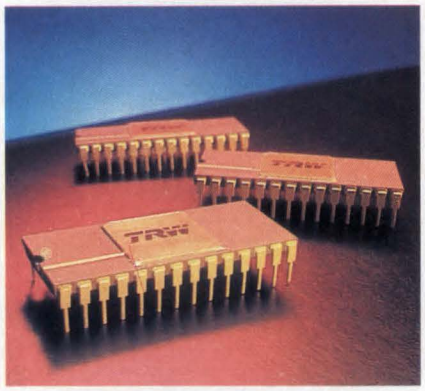

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PROGRAMMABLE LOGIC DEVICES CUSTOMIZE APPLICATIONS

By using programmable logic, system designers can quickly make "glue" functions with a higher level of integration.

by Dev Chakravarty and Erich Gottlieb

Programmable logic devices have been recognized as a major design tool only in the last couple of years. Even now, however, the full potential of these devices remains to be tapped. In exploring their use in engineering designs, it is valuable to take a brief look from the product standpoint, outline areas for future product development, and identify the application-specific IC choices available to design engineers.

Computer system designers are faced with a variety of choices that are often conflicting in nature. While the fiercely competitive marketplace dictates low price product usage, the growing breed of discerning computer users warrants segment targeting with custom built ICs that serve specific user needs. At the same time, the market demands product positioning at the right time. This creates the familiar dilemma for the innovative system designer—the requirement of fast turnaround times in implementing the unique "market-catching" design ideas into silicon versus lengthy chip design time (over a year) for custom designed chips.

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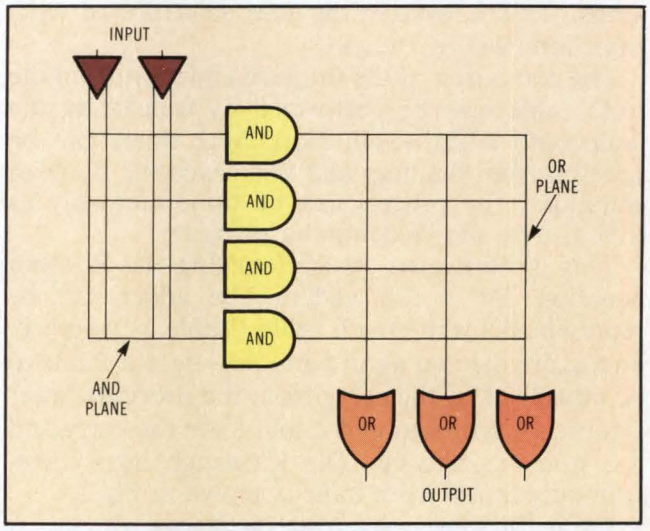

Fig 1 The structure of programmable logic devices (PLDs) consists of an array of AND gates and OR gates that can specify logic patterns.

A possible answer to this dilemma is the judicious use of programmable logic devices (PLDs). PLDs have come of age only recently, and as system designers become familiar with them, their growth becomes more widespread. A study made by Dataquest showed the world usage of PLDs as $35 million in 1981. A conservative forecast estimates the world market will be $250 million in 1985—ie, a compound growth rate of over 60 percent in the four-year time frame.

Surveying programmable logic

The common feature of all PLDs, which cover a whole family of products, is a basic structure consisting of an array of AND gates and OR gates (Fig 1). The inputs to the devices enter the array of AND gates, commonly referred to as the AND plane. The

TABLE 1
Truth Table for a Full Adder

I1	I2	CP	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

device output is the output from the array of OR gates, referred to as the OR plane. The number of product terms refer to the number of AND gates grouped together by the OR gate output.

The pattern of AND gates followed by OR gates is especially suitable for logic applications. This is because it is possible to specify most logic applications in the form of a truth table, where the output patterns (high/low/or don't care) can be exactly determined for each input pattern, and the truth table can be directly translated into a Boolean equation with AND terms grouped together by OR terms. This is exactly the PLD structure of AND gates followed by OR gates.

The derivation of the Boolean equation from the truth table may be performed by translating the table onto a Karnaugh map. Max terms can be selected from the map and this yields the Boolean equation. The process can be done manually as well as by a simple computer program.

This is illustrated by constructing the Boolean equation for a full adder. The adder can be represented by the truth table (Table 1) where I1 and I2 are the two input variables—ie, the 2 bits to be added. CP is the carry from the previous lower significant position, and C and S are the carry and the sum respectively. The Karnaugh map corresponding to the truth table is shown in Fig 2.

Using the Max terms from the Karnaugh map, it is possible to derive the following Boolean equation from the map.

$$C = I1 \cdot \overline{CP} + I1 \cdot \overline{I2} + I2 \cdot \overline{CP}$$
$$S = I1 \cdot CP \cdot \overline{I2} + \overline{I1} \cdot CP \cdot I2 +$$
$$= I1 \cdot CP \cdot I2 + I1 \cdot CP \cdot I2$$

Both the above equations can be easily represented in a two-level gate structure consisting of AND gates followed by OR gates, which is precisely the PLD structure.

System engineers traditionally construct designs, using a variety of standard low power Schottky parts that cover a wide range of functions from NAND, NOR, gates to flipflops, and counters. Designers need user PLDs to specify each function as a truth table. For example, a 3-bit binary counter has to be illustrated on a truth table, and only after the entire design process is executed does the PLD become a counter.

Traditionally, system designers would just pick the counter off the shelf. This process is not as cumbersome as it first sounds. Once designers get used to the process, it becomes relatively simple to use, and they have more control over the end products. Also, software aids are being developed to help simplify the process. Finally, the major advantage is that designers are able to customize the part to fit the design, rather than customize the design to fit the part.

The PLD generic family includes a variety of products such as field programmable logic array (FPLA), programmable array logic (PAL), hardware array logic (HAL), and PROM. A brief explanation of each is given in Table 2. The major attraction of PLDs lies in their inherent simplicity, as every digital logic system designer does not have problems with thinking in terms of AND followed by OR gate functions. According to C. Mead and L. Conway in their *Introduction to VLSI Systems* (Addison and Wesley Publishing Company, 1980), "Fortunately, there is a way to map irregular combinational functions onto regular structures, using the programmable logic array (herein referred to as may be significantly changed without requiring major changes of either the design or layout of PLA structure."

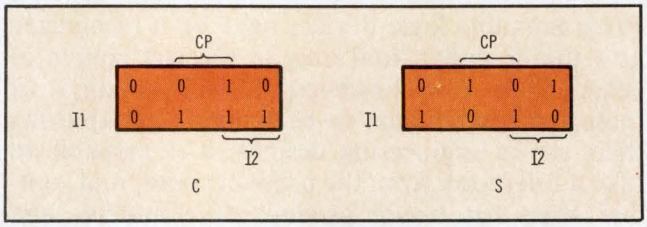

Fig 2 As shown, the Karnaugh map corresponds to the truth table for the logic application (full adder) in Table 1.

This "fortunate" strategy not only applies to combinational circuits, but also to sequential circuits. In the process of feeding back the output through a buffer to the inputs, the PLD can be used as a state machine. It therefore caters to all sequential circuits—counters, adders, shift registers, etc.

Existing PLDs come in a variety of package sizes, the 20- or 24-pin versions being the most widely used today. Designers identify the input and the

TABLE 2
List of Common PLDs

		AND Terms	OR Terms
PAL	Programmable array logic	Field programmable	—
HAL	Hardware array logic	Factory programmed	—
FPLA	Field programmable logic array	Field programmable	Field programmable
PROM	Programmable read only memory	—	Programmable

output pins of the package as per the manufacturer's specifications. They then identify these input and output pins with the inputs and outputs of their own system circuits and assign symbolic names (conforming to the system of the various PLD pins). The standard pinouts such as GND and VCC as specified need only to be identified. Boolean equations are then stated by the system designers, linking the outputs to the inputs. For example, the Boolean equations for the configuration would be stated simply as

```
C = I1 * CP   + I1   * I2   + I2   * CP
S = I1 * /CP  * /I2 + /I1  * CP  * /I2 +
    I1 * CP   * I2   + /I1  * /CP * I2
```

A simple computer program takes these pinout specifications and the Boolean equations as input and generates the output in the form of a fuse map for the PLD in a matter of minutes. A complete function or truth table defining the outputs at various input configurations may also be input. This checks the accuracy of the logic equations, thus ensuring reliability.

For designing sequential circuits—ie, using the PLDs as state machines—the design process is similar to the one mentioned above. However, in such cases, the outputs are bidirectional and may therefore be used as inputs. For example, in the adder, the output C can be fed through a D flipflop back to the input to become CP.

To design such state machines, the designer may construct a state table from the system specifications. The number of states will determine the number of I/O pins. A Karnaugh map may then be drawn for each output pin in terms of the previous state and the input. This subsequently determines the Boolean equation for that output pin. The resulting pin specifications and the Boolean equations are then entered into the program exactly as described. This creates the fuse map which is then entered directly into programming machines, a variety of which are available in the market. This blows the fuses of the individual PLD ICs.

Upgrading PLD versatility

Most PLDs that are available today are in the TTL version. High speed PALs and HALs with an impressive propagation delay of 25 ns are available. ECL HALs will be available shortly, driving down the propagation delays to below 10 ns. CMOS PALs with higher gate densities and lower power dissipation are also in the pipeline and will be made available in the near future.

The present 20- to 24-pin PLDs are equivalent to a 200- to 300- gate array. Upgrading to 40 and 84 pins in leadless chip carrier packages or pin grid arrays will permit gate densities of over 1000 gates. These PLDs will therefore usefully serve the lower end of the gate array market, especially from large to small quantities.

While PLDs have been used in a variety of different and often ingenious ways, only the major broad categories are worthy of examination in order to give system designers a perspective. One major PLD application is as a "glue" between standard blocks such as microprocessors, I/O devices, gate arrays, and standard cells. To configure a peripheral interface adapter with a microprocessor, a glue chip in the form of an address decoder is needed to access the ROM/RAM configuration. This can be easily constructed from a PLD. An interrupt controller is required to interface a peripheral device with an MPU, and this can again be constructed using a PLD.

One PLD can also replace as many as 5 to 10 SSI/MSI devices. This can be done by combining a variety of gates, flipflops, and registers, by defining the Boolean equations of particular functions such as a barrel shifter or character transmitter, and by using only a single PLD. This leads to significant cost and space savings. For example, David Carlson of Digital Equipment Corp reported ("Care in Packaging Off-the-shelf LSI Keeps 32-bit Minicomputer Compact," *Electronics,* Oct 6, 1982, vol 55, p 115) that the use of PALs in the VAX 11/730 helped reduce board area for the CPU by a factor of four, and halved component cost, as compared with equivalent performance MSI.

As discussed earlier, PLDs find a variety of uses as state machines. Thus, ripple counters and full adders can be constructed easily with PLDs conforming to customized requirements.

As stated above, many PLD advantages, such as significant space and cost savings when compared to SSI/MSI devices, have already become apparent. Essentially, PLDs allow the creation of low risk custom circuits with fast turnaround time. Some disadvantages of other application-specific IC components—eg, macrocell arrays and standard cells include longer times to prototype, higher option development costs, and difficulty of making design changes, but these are resolved by PLDs. Yet, PLDs have higher handling costs, and gate densities are lower than macrocell arrays. At higher volume requirements and high gate counts, macrocell arrays or standard cells may be a better alternative to PLDs. In the hands of innovative system designers, however, PLDs are a versatile tool. The inherent simplicity in PLD design, fast design turnaround time, and ease of customizing will no doubt generate a rapid increase in their use in the near future.

CDI gate arrays & Ven-Tel modems — Another CDI partnership pays off

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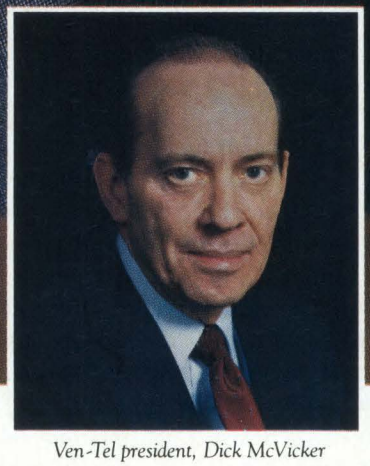

Ven-Tel president, Dick McVicker

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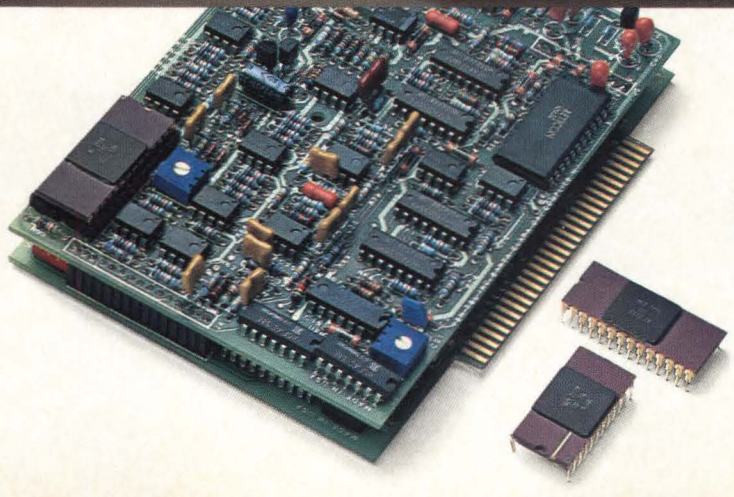

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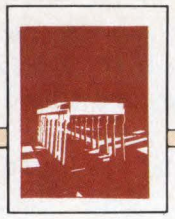

VLSI CHIPS COMBINE TEXT AND GRAPHICS

A pair of VLSI display controller chips can be used to provide both text and graphics displays for workstations. Some attention has to be given to timing, but otherwise design is straightforward.

by Bradley A. May and Andrew M. Volk

Office workstation users want their machines to talk to them with pictures as well as words because pictures transmit information faster than words—graphic depictions make trends in data much more obvious than in a tabular format. Workstation users can also use a cursor to select the symbol representing an action without remembering command strings or reading lengthy menus. Although such graphic interfaces are expected to become widespread, there will still be a need for high quality text that can be rapidly displayed and edited.

Controller designs to optimize displays have to be different for text and graphics. Display subsystems for office workstations require several qualities. The first is a simple user interface. Typically, this interface is operated by selecting items from a menu or using a mouse to position a cursor over the symbol representing the desired action. In addition, nontechnical people should be able to operate the workstation. Another quality is a medium to high density display that can exhibit a full 8½ x 11 in. page of text. High resolution character fonts, subscripts, special symbols, and alternate character fonts are often included. The CRT display should represent as exactly as possible the final printed document.

The subsystem should also have business graphics. While charts and graphs are primarily used, the graphics capability can include photographic information, company logos, signatures, blank business forms, etc. Animation is only necessary on a limited basis, usually to translate graphics from one place on the page to another.

Finally, the system should have help files, which are usually requested by moving the cursor to the word or symbol in question and pressing a help key. A help file pops up on the screen, superimposed on what was already displayed. When the user enters the next command, the help information vanishes, uncovering the previous display.

Approaches to CRT control

Using bit-mapped displays, each pixel on the CRT screen is mapped into a bit of RAM. Color systems map several bits of RAM per pixel to encode color information. During display, data words are fetched from RAM and serialized to form a video signal. This parallel-to-serial conversion reduces the memory bandwidth by a factor equal to the width of the word, in bits; 16- to 32-bit words are common in workstation designs.

The advantage of bit-mapped graphics is that any data that can be drawn in two dimensions can be displayed. This is limited only by the display resolution. On the other hand, the large amounts of RAM required can be a disadvantage. Display

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sizes of 800 x 600 pixels are common, requiring ¼ Mbyte of RAM for a 16-color display. However, this disadvantge has diminished as dynamic RAM prices have dropped over the past several years.

A more important limitation of a bit-mapped system, in terms of office workstations, is slow text manipulation. This slowness is due to the necessity of moving characters pixel by pixel. Also, because the bit-mapped RAM is usually shared between the CRT controller and the microprocessor, some dual-port memory scheme is needed to give the microprocessor access to the text. Depending on implementation, this scheme can be slow or it may require fast RAMs—twice as fast as needed to meet the CRT refresh requirements—to allow interleaving memory accesses between the CRT controller and microprocessor. Faster RAMs increase system cost and expensive static RAMs would possibly be required.

At the cost of a second controller, text and graphics performance is increased several times.

Alphanumeric controllers, on the other hand, take advantage of the nature of the information displayed. Characters to be displayed are stored in encoded form (eg, ASCII). Using ASCII, only a 7-bit code must be stored, rather than the 117 bits required to store a 9- x 13-pixel character field. This considerably reduces the amount of RAM required, yielding a cost advantage. Data transferred to the CRT controller to refresh the display is reduced by the same amount. This means characters may be placed in system RAM and transferred to the CRT controller fast enough to refresh the display, but still leave most bus bandwidth available to the microprocessor. Because the text is in system memory, the microprocessor can access it quickly, without resorting to dual-ported or interleaved memory schemes.

In an alphanumeric CRT controller, character codes are used to address ROM containing pixel-by-pixel character definitions. Multiple character fonts can be displayed by storing all fonts in ROM, or by implementing a character RAM, which may be loaded with different fonts. Because a character RAM lets fonts be stored on disk, the number of fonts available is virtually unlimited.

Character codes are stored in system memory. If a pointer mechanism is used to access the characters, they need not be placed in consecutive memory words in their order of display. This frees the system programmer to organize displayed data in whatever form makes editing software most efficient. Characters do not have to be moved when text is inserted or deleted. Rather, only those characters within one string have to be moved.

Alphanumeric systems support graphics with special graphics characters. Figures to be displayed are split into character-sized pieces and stored in the character ROM. They are addressed by character codes, or sequences of codes not used to address the regular characters. Only limited graphics can be displayed this way. More general graphics can be displayed by using a RAM rather than a ROM to store the graphics characters. Keeping a large set of graphics characters in mass storage to load into character RAM as needed in the display also increases graphics capabilities.

One disadvantage is that character graphics limits graphics to bar charts, letterheads, and standard company forms, unless a RAM-based character generator is used. This, however, increases hardware costs. Also, manipulating such graphics (eg, rotation, scaling, and translation), when possible, is extremely slow and cumbersome.

As an alternative to bit-mapped graphics and alphanumeric systems, some designs use a bit-mapped approach, but reserve part of the bit map for encoded character information. The controller uses this information to address a character ROM in the usual way, reducing the text storage requirements. Text manipulation is also faster because now only character codes, not pixel-level data, must be moved. Limitations still exist, however. The microprocessor must access the data via a dual-port interface, a disadvantage shared with pure graphics systems. Moreover, data organization is not as flexible as it is with advanced alphanumeric controllers.

Examining separate controllers

A design using separate VLSI controllers for text and graphics is another approach. The 82730 text coprocessor displays text stored in system memory, while the 82720 graphics display controller (GDC) displays the bit map and draws into it to create shapes such as lines, arcs, rectangles, and filled areas. Both controllers fit business graphics requirements and run independently, except that one must generate video sync signals for both parts. Video outputs must be combined and software must synchronize the two controllers, allowing them to make changes to the display simultaneously (eg, slow scrolling).

At the cost of a second controller, performance in manipulating text and graphics together is increased several times. This is partly because the two controllers operate concurrently, and partly because each controller is optimized for a portion of the display task. Additional complexity compared to a combination controller is minimal, if any. Because the controllers are independent, various text-over-graphics effects are easily achieved.

The text coprocessor supports high resolution displays of up to 200 characters per row. A

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10-MHz maximum character rate (up to 80-MHz video rate for the companion 82731 video interface chip), and up to 2048 scan lines of monitor resolution support full-page text displays. Up to 32 scan lines per row (64 when using the double height attribute) allow very high quality character fonts. Horizontal sweep rate, sync width, front porch, and back porch timings are programmable to the nearest reference clock (RCLK) period. Vertical sweep rate, sync width, front porch, and back porch timings are programmable to the nearest horizontal sweep period. This adjustability allows optimal use of high performance monitors.

In addition, the text coprocessor supports workstation display features such as proportional spacing, subscript and superscript characters, two independent cursors (especially useful if one is a menu cursor), lightpen detect, and smooth vertical scrolling (smooth horizontal scrolling is done with proportional spacing). Six character attributes are implemented internally: reverse video, blinking, invisible (the character is output, but blanked), two separate underlines (programmable to any scan line in the row and usable as overbars or strikethroughs), and graphic character. The last attribute overrides the normal character height parameters to allow graphics, such as business forms, to extend without breaks across text row boundaries. Fifteen character outputs allow a maximum of 32,000 characters, but any number of these can be used to control user-defined attributes. This allows manufacturers to design distinctive displays.

Users define attributes

Each character is stored in 2 bytes. The MSB is used to distinguish characters from data stream commands that affect display of other characters (eg, lowering for subscripts). This leaves 15 bits per character, the number of character output pins on the text coprocessor. The six character attributes can be controlled by an attribute bit, by data stream commands (requiring no bits in the character word), or simply not used. If these attributes are controlled by attribute bits, the corresponding output pins are redundant. The text coprocessor uses these pins by defining four general purpose attributes (GPAs), which are controlled by data stream commands and mapped to redundant attribute outputs. These GPAs can control user-defined attributes (eg, color or font selection).

The text coprocessor also has an 80186-like bus master interface and an onchip DMA channel, which allow it to fetch data to refresh the display without CPU intervention. The 80186 is an integrated 16-bit microprocessor that incorporates an 8086 processor core. Data is stored in strings in memory accessed via a list of pointers, allowing text manipulation by changing pointers. Text movement is minimal. Text editors can therefore run faster than would otherwise be possible. The text coprocessor supports display windows. Blocks of text can overlay other text on the screen and later be eliminated. This is done solely by manipulating pointers and does not affect characters in memory. Although done by software, the controller's list-based data structures make manipulation easier. Display windows are especially useful for displaying multiple concurrent processes and pop-up menus.

All command and status information is passed back and forth via communication blocks in memory. The list of commands the microprocessor can give to the controller is lengthy. Two, however, are important for the design example—MODESET and START DISPLAY. MODESET allows CRT monitor parameters (including interlace), character and row display parameters, appearance of cursors and underlines, and DMA parameters to be initialized or changed. As changes take effect during vertical retrace, the display is not disturbed. No sync pulses are output until a MODESET operation is finished. START DISPLAY begins display of the process of fetching data. Because onchip registers are not read or written, the controller and the microprocessor can be separated by a dual-port RAM in larger systems where the microprocessor bus is heavily used. Use of bus bandwidth for CRT refresh would be undesirable in such systems.

Figures can be drawn by replacing, setting, clearing, or complementing existing memory contents.

The second controller, the GDC, supports up to ½ Mbyte of bit-mapped RAM (equivalent to 2048 x 2048 pixels in monochrome or 1024 x 1024 in 16 colors or grayscale levels). It quickly draws lines, rectangles, arcs, circles, and graphics characters into the bit map at up to 1.25 million pixels/s.

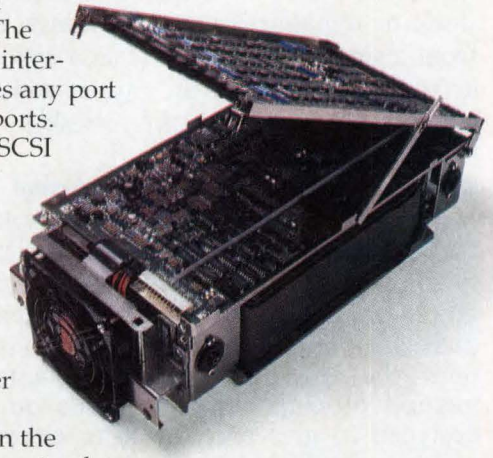
A GDC graphics character is a user-definable shape, up to 8 pixels square. It can be used for alphabetic characters, pattern fill, etc. Figures can be drawn by replacing, setting, clearing, or complementing existing memory contents; line segments may be solid, dotted, or dashed as determined by a rotating 16-bit pattern register. The GDC supports two display partitions of user-defined height (they must be the full width of the display) that can be mapped to any window of the bit map. These windows may be panned horizontally or vertically and zoomed for display.

Interface to the host microprocessor is via an 8-bit slave peripheral interface. Commands and data are passed to the GDC via an onchip 16-byte first in, first out (FIFO) register. The GDC provides

Will Fujitsu's SCSI INTERFACE *Please Stand Up?*

For some time now, the disk drive industry has talked about the SCSI Interface. But all this talk has resulted in very little action. Until now. Today a leader in the SMD market is offering their OEM customers the option of the SCSI Interface. That leader is Fujitsu America Inc.

SCSI, the ANSI-approved small computer systems interface, is a byte wide intelligent interface designed for host computer systems and peripheral units and can transfer data at up to 2MB/s. The computer and peripherals are interconnected on an eight port matrix bus, which enables any port to initiate communication to any of the other seven ports.



Fujitsu America now offers the state-of-the art SCSI interface option on the high performance 8" M2312 drive which has a capacity of 84 MB and an average positioning time of 20ms. Previously this drive was only available with an SMD interface.

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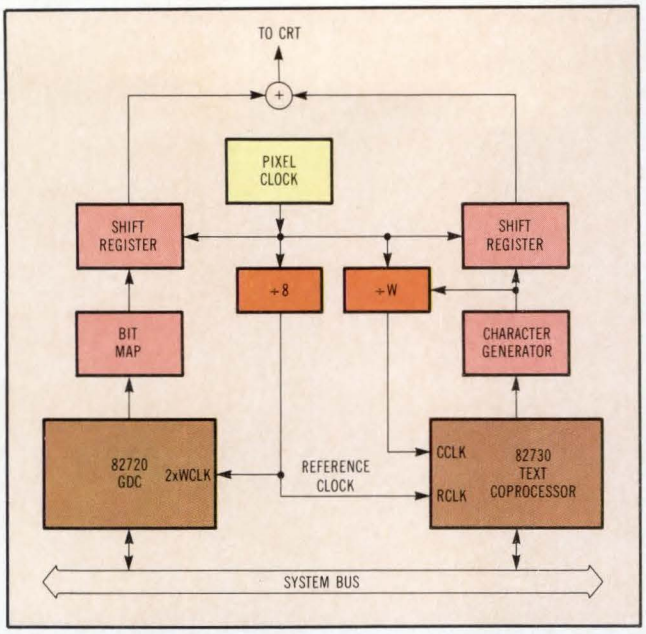


Fig 1 Providing a common clock is the easiest way to synchronize graphics and character displays. The "W" input to the text coprocessor's CCLK controls displayed character width.

FIFO EMPTY and FIFO FULL bits in its status register. The microprocessor monitors these bits to keep the GDC stoked with commands. Because the FIFO can hold the longest command and all its parameters, and still have some bytes free, the GDC seldom has to wait long for the next command.

Providing HSYNC, VSYNC, and BLANK signals for video logic, the GDC can be synchronized to an external VSYNC source. It has an internally debounced lightpen detect input and also provides two signals (DBIN# and ALE) that can be used to control either static or dynamic RAM. All timings are generated from a single clock signal (called 2xWCLK, because its frequency is twice the rate at which GDC reads memory words during CRT refresh.)

Combined text/graphics system design

Designing a text and graphics display with both the GDC and text coprocessor basically involves synchronizing the operation of the separate graphics and text subsystems, as well as combining their video outputs. Synchronization is necessary at both the video and host CPU interfaces. The method of combining the video outputs can be designed to give precedence to either the text or graphics display as required.

To synchronize the two video systems, the horizontal and vertical sync signals must be kept at the same frequency and phase. Several methods can establish the proper frequency. The simplest is to provide each chip with the same reference clock (to 2xWCLK on the GDC and to RCLK on the text coprocessor), and then program each with a compatible set of timing parameters. Fig 1 shows this connection, which will be used for the examples in this article. Because the reference clock connection is common, the reference clock must be eight pixel clocks to satisfy GDC's requirements. This does not affect the text coprocessor's handling of character width, as this is controlled by the separate character clock (CCLK). This restriction does fix the text coprocessor's hardware tab spacing, which is controlled by the reference clock.

A slight variation of this connection still uses a common pixel clock, but also uses separate reference clock dividers for the two subsystems. This allows the designer to choose the text coprocessor clock divider to suit the required tab spacing. However, the total number of dot clocks per horizontal sync interval must be identical. This restricts the possible dot clock values to a common multiple of the two clocks, unless an odd length "make-up" clock can be provided in one of the clocks during horizontal retrace.

Phasing of the vertical and horizontal intervals is done by designating either controller as the master video sync source. The other chip is then programmed to be a slave that synchronizes the master's signals. The two possible connections (either chip as master) are shown in Fig 2. Both chips can be synchronized to external sync sources. The choice of configuration depends on the system design, especially if an interlaced display is used.

When the GDC is master and the text coprocessor is slave in a noninterlaced display [Fig 2(a)], the rising edge of each vertical sync from the GDC resynchronizes the text coprocessor's video timing generator. The text coprocessor can recover synchronization even if it is momentarily lost. Use of the GDC in master mode reduces the minimum retrace interval by two reference clocks. However, this configuration is not suitable for interlaced displays, as the text coprocessor cannot slave to the GDC's interlace sync timing.

Fig 2(b) shows a configuration for interlace or noninterlace with the text coprocessor as master

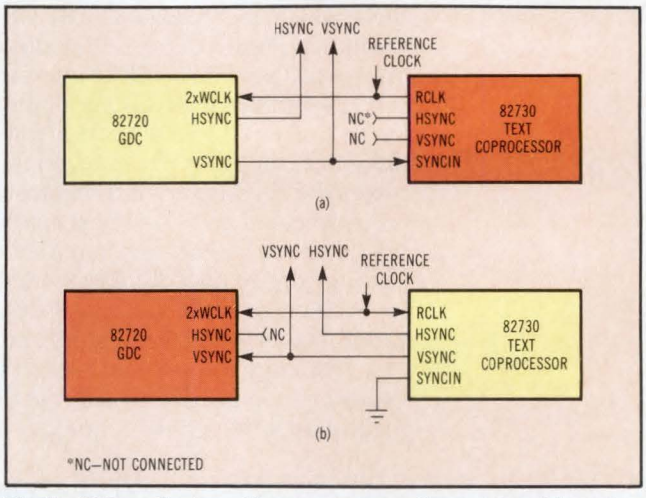


Fig 2 Either display chip can serve as the master video sync source. The GDC acting as master (a) is suitable for noninterlaced displays, but the text coprocessor must act as master (b) for interlace, since the text coprocessor cannot slave to the GDC's timing.

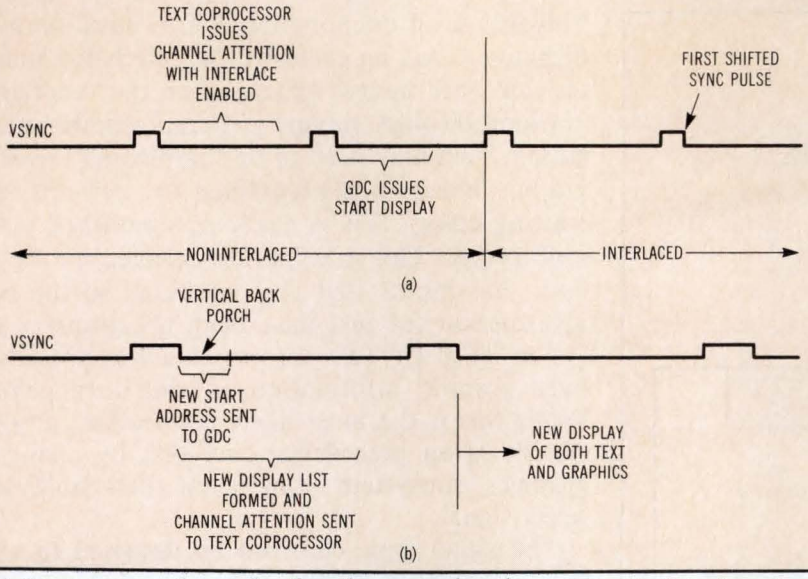


Fig 3 The GDC must get at least one vertical sync signal before beginning interlaced mode (a). Care must also be taken to update both chips simultaneously when updating the screen or scrolling. The display update command timing diagram (b) shows that the modifying commands are issued one vertical sync pulse before the update is required. This is necessary because the GDC does not have automatic frame synchronization.

and the GDC as slave. In the slave mode, the GDC synchronizes its timing generators during initialization. It must see at least one vertical sync from the text coprocessor before the START DISPLAY command begins display. After this command, the GDC's timing generators are free running. They remain in sync with the text coprocessor through the identically programmed timing intervals. Synchronization of noninterlaced displays requires no further action.

Initialization in interlaced mode is more complex because the frame timing consists of two fields that also must be synchronized. To be sure that the two chips' video timing generators start together in a known phase, they are started in noninterlaced mode. The GDC automatically assumes noninterlaced mode during its initialization (before the START command is issued) even if it has been set up for interlaced mode. The first MODESET command to the text coprocessor specifies noninterlaced. To start them running together requires giving the GDC its START command and the text coprocessor a new MODESET command, with interlace enabled, in the proper sequence.

Besides allowing interlaced displays, the connection in Fig 2(b) has other advantages. The text coprocessor's video timing generator is more flexible than the GDC. For instance, there is no restriction on the sync timing relative to the display field. Moreover, the text coprocessor automatically times the vertical sync pulse during interlaced mode to minimize scan-line pairing.

Synchronizing software

Most of the time, the system software deals with the text and graphics subsystems independently. Timing of the commands between the two subsystems is generally not important. What matters is the effect the commands have on the display. However, there are two instances in which care needs to be taken: during initialization (especially in interlaced mode), and whenever the screen information changes position (eg, in scrolling). In both instances, data bases must be manipulated so that the text and graphics displays change or move together.

Because the text coprocessor can compensate on the fly, display initialization of noninterlaced displays, where the GDC is master, requires no special sequences to get the hardware to track. When the GDC is the slave, the software must initialize and start the text coprocessor's sync generators first (through the MODESET command). The text coprocessor needs to see at least one vertical sync pulse before its display is started.

Initialization of the interlaced mode with the text coprocessor as master is more complicated, as previously suggested. In this case, not only does the GDC have to be started after seeing one vertical sync, but the text coprocessor must be changed from noninterlaced to interlaced mode at the proper time to have both controllers in field and frame synchronization. Fig 3(a) shows the proper sequence of commands to start an interlaced display.

Commands must also be timed properly when the display is changed or scrolled. Both chips interpret the information they use for changing the display as the change is encountered during screen scanning. The GDC examines its internal FIFO and the text coprocessor takes the information from its memory resident display lists. Keeping the displays in sync from the software side requires issuing commands to the controllers so that the commands take effect on both chips in the same frame.

Two events govern the timing of changes to the text coprocessor's display list. The first two rows are fetched during the vertical retrace interval, after any channel command and interrupts are handled. After this, the data is fetched during the row previous to its display. Two methods can establish the frame in which the change will happen. First, knowledge of where the change is to be

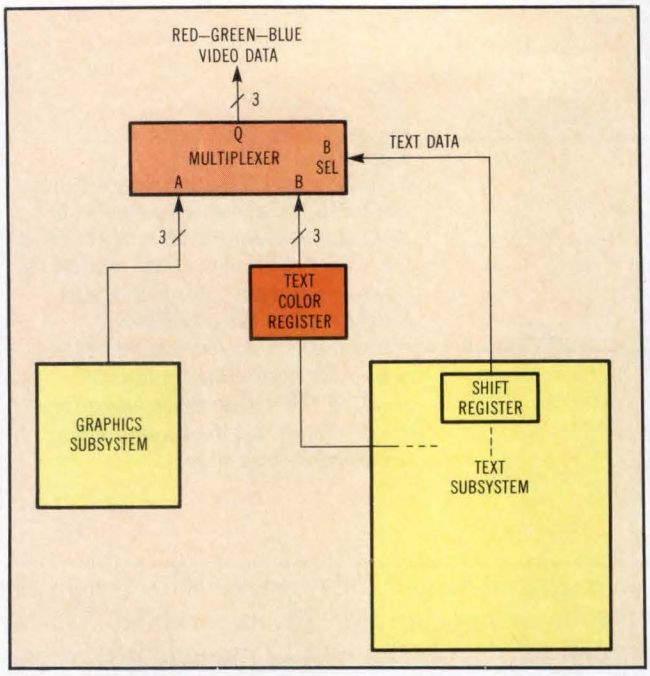


Fig 4 A multiplexer can be set up to give precedence to either text or graphics. Text has precedence in this case, and the text color register controls the color of the letters.

made allows the host CPU to directly change the data using text coprocessor timing signals to synchronize it. For instance, data that is not in the first two rows can use VSYNC to time the change.

The second method is a more uniform approach using the two string pointer lists in the text coprocessor. The strings to be changed are copied to a free area of memory and modified (in the case of scrolling a window, this is just two 2-word strings). The current display list is copied, and pointers to the new strings are substituted for the old. Changing the screen is then just a matter of changing the alternate string list base pointer and issuing any convenient command (any command causes the LIST switch bit to be read). The change occurs in the next frame without worry about where in the screen it occurred.

Because the GDC does not have automatic frame synchronization mechanisms, the modifying command should be issued after the vertical sync pulse of the frame prior to the one in which the change should occur [see Fig 3(b)]. The CHANNEL ATTENTION that sets up the text coprocessor should also be issued during the same frame.

Combining video outputs

After the display is synchronized, the video data from the text and graphics subsystems must be combined. Data can be mixed with simple combinational gating or with windows controlled by either chip (see Fig 4).

Combinational gating can be as simple as ORing the two video signals together. In a monochrome system, this gives the "white" level predominance, when text and graphics overlap. A NOR gate gives "black" level predominance for black-on-white displays. Using an exclusive OR gate helps guarantee that both images appear when they overlap.

Color displays require different combinational gating. Text may need to be "impressed" over the graphic image in a predefined or, perhaps, contrasting color. This is easily accomplished with a multiplexer. This multiplexer, selected by the text data, has inputs that are connected to the color information for text data from the graphics subsystem (Fig 4). Text information has precedence over graphic information in this arrangement. While this is the most likely connection, graphics can be given precedence over text by giving the graphics subsystem control of the multiplexer select signal.

The video logic can also be designed to allow either the text or graphic data to be displayed only within a window (see Fig 5). Windows can be used to enforce a format between graphics and text or to allow data outside the window to be blanked. For instance, if a full page of graphics data never needs to be displayed, then a full complement of bit-mapped memory does not have to be provided. The memory that is not yet written in or is not present can be blanked by choosing proper dimensions for the window. Data from the bit-map memory can be placed anywhere on the screen using the GDC's panning capabilities. Windows can also be used to close off areas while the image is being built. Useful when the display is updated with new data, this allows only one chip to control the blanking and formatting of the display instead of having to coordinate the data from both subsystems at once.

Either chip can control the window (Fig 6). Complexity versus resolution is the trade-off. The greatest resolution is available through the GDC, where the window boundary can be defined to the pixel. One method is to define the window as filled areas in a separate bit plane. The GDC can rapidly

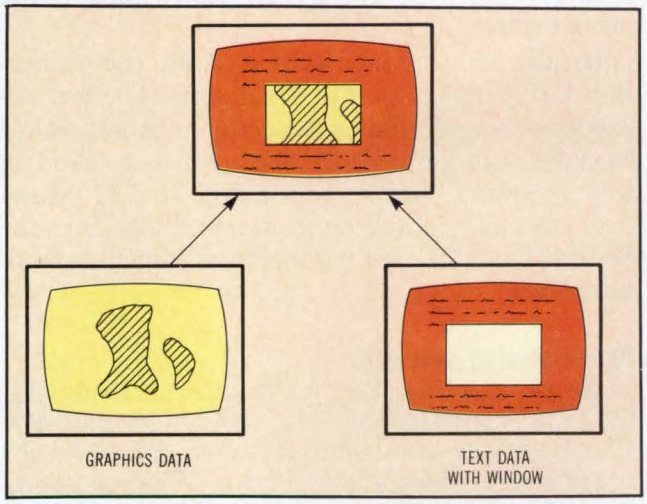
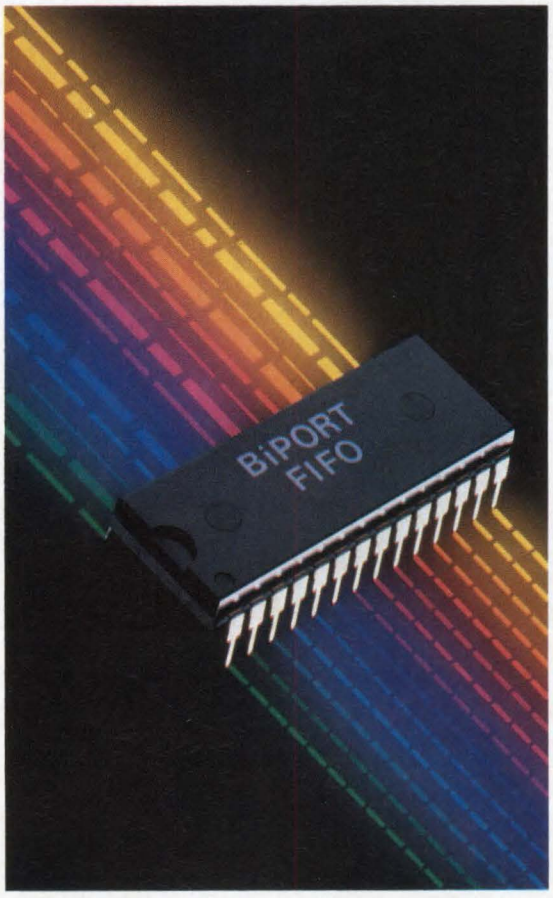


Fig 5 When text has precedence, graphics can be displayed only in a window. A full graphics display is generated, but only the part within the window appears on the CRT display.

SYNC THE UNSYNCABLE



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CIRCLE 93

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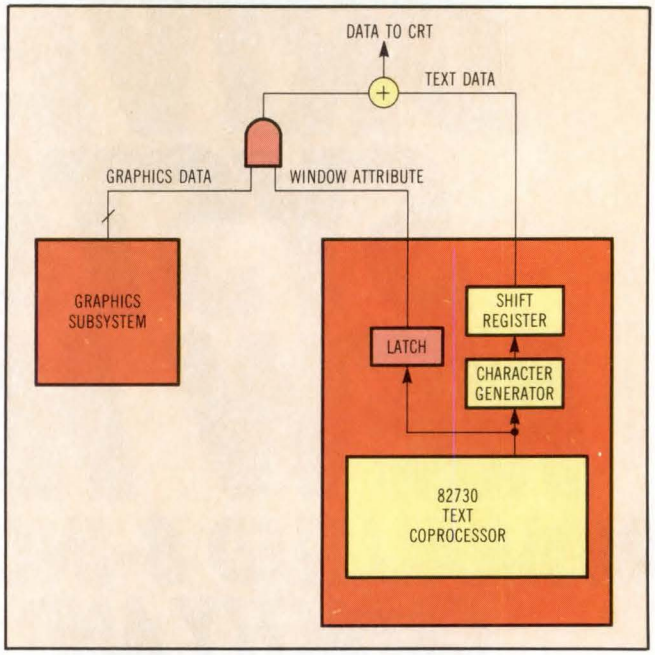

Fig 6 A text-defined window can be controlled by an attribute bit from the text coprocessor. In essence, during the times when the bit is on, graphic data will be written to the screen. At all other times, only text will be written.

generate and fill rectangular areas. Using a separate bit plane allows graphic images to be generated within the window using other bit planes. However, this can be quite costly in terms of memory. In multiple bit-plane applications, where text and graphics are mutually exclusive, a particular pixel bit value could be used to set the window. This saves most of the memory cost while preserving resolution.

Where pixel resolution is not required, the text coprocessor can control the window in character cell increments with less expense and complexity. Control of the window can use a memory bit for character-by-character control. This same bit can be activated by the FIELD ATTRIBUTE MASK command. The GPA command can also establish windows over a larger area. Finally, a window can be defined using the text coprocessor's virtual display mode, where an independent data base sets the window characteristics. If designers choose one of the four video data output pins that are controlled by the GPA command (DAT 9 through DAT 12), then they can use any or all of these methods to define the windows without changing the hardware. This allows considerable flexibility in software management of the windows.

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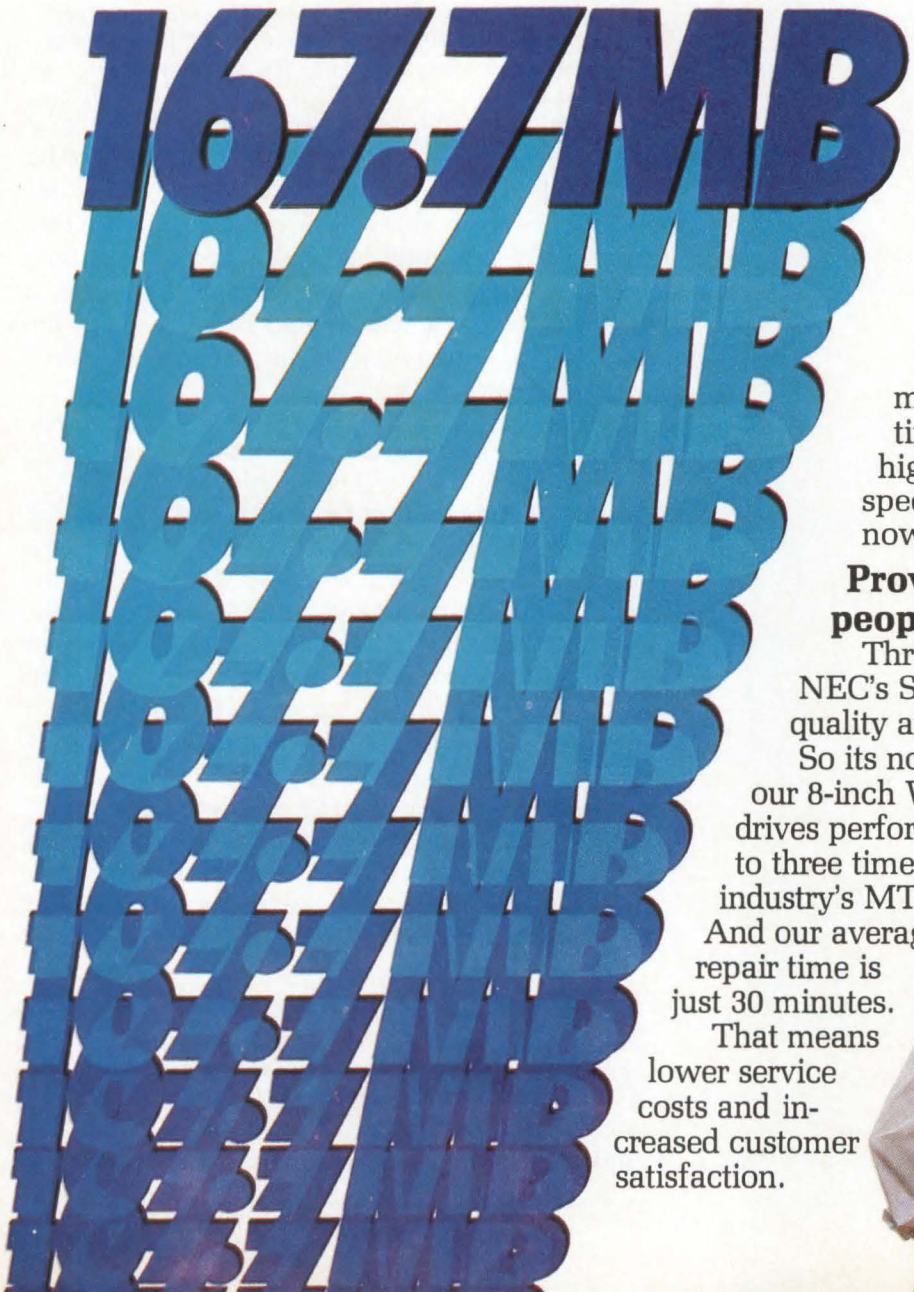

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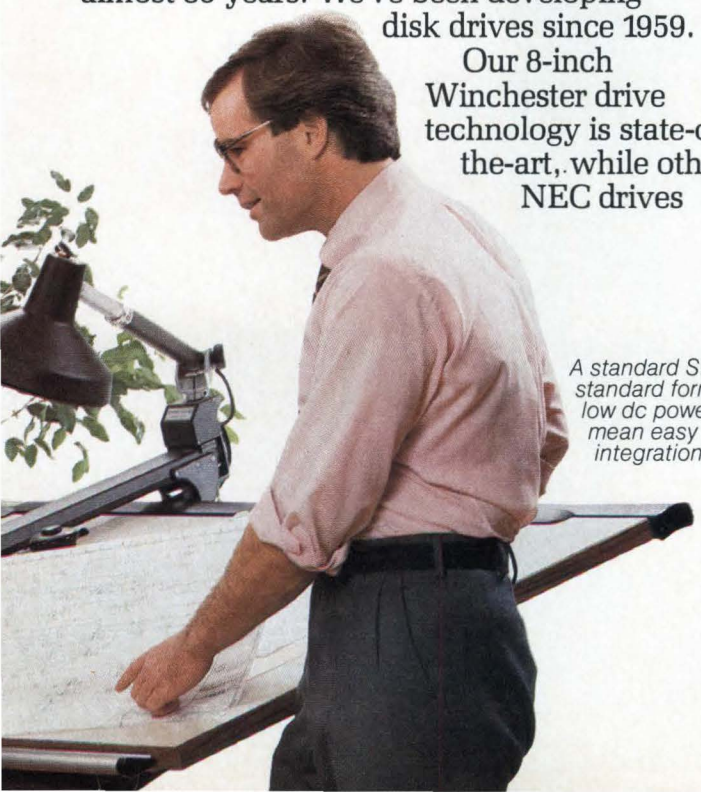

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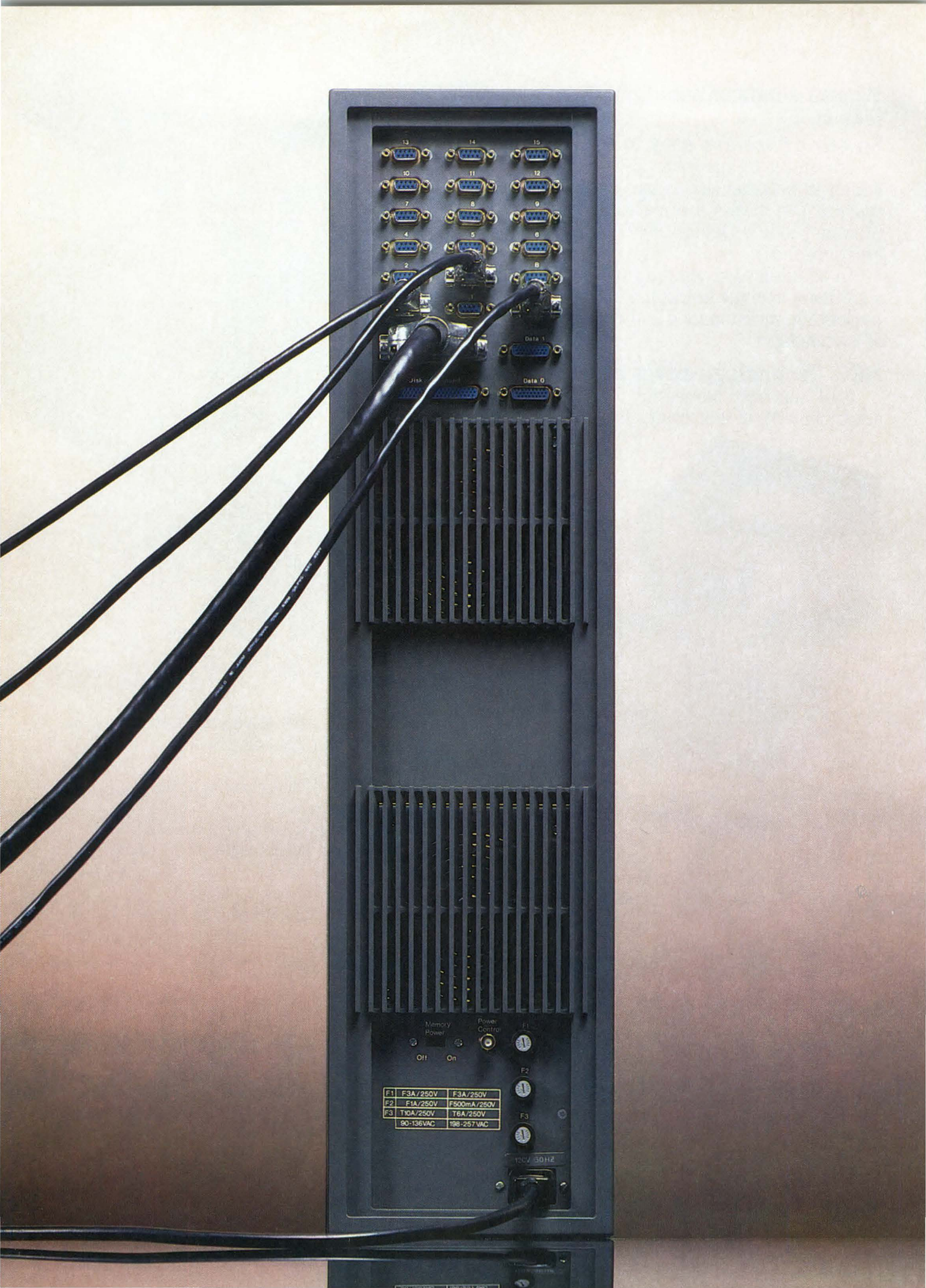
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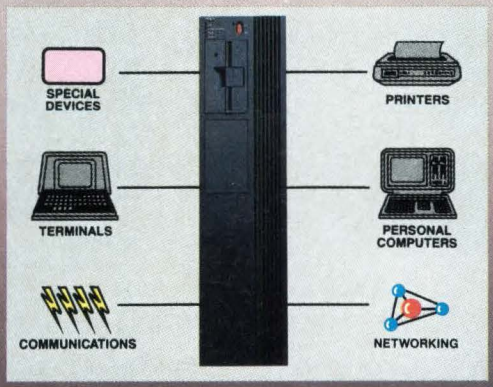

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CIRCLE 97

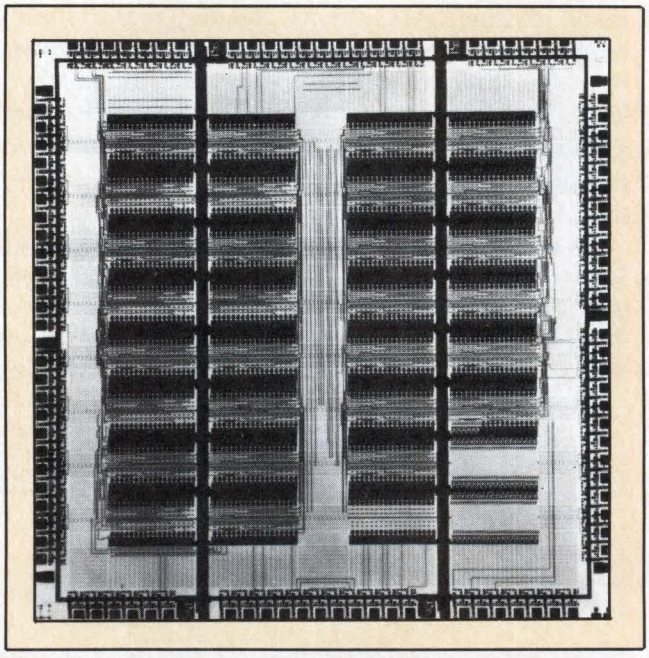
AUTOMATION CUTS DESIGN TIME FOR GATE ARRAYS

A self-contained automated silicon design system cuts design time for complex uncommitted logic arrays from 24 to 8 weeks.

by Anthony V. Walker

Systems being developed today using uncommitted logic arrays approach the level of complexity that previously took a team of engineers several years to attain. Such a project would have been split into sections, often into separate PC boards. Each section was breadboarded and analyzed in great detail as the design evolved. Once the final set of PC boards for the system was produced, it was standard practice to revise each board several times and produce design change notices for the backplane wiring. Today, this complexity is achieved on one piece of silicon with the expectation that it will work the first time and in a shorter time than achieved by the PC board design route.

Over the years, the complexity of uncommitted logic array (ULA) designs has increased to several thousand gates along with an ever-increasing requirement to produce them faster. Consequently, a need for ever more powerful computer design tools has emerged. These should allow the required designs to evolve as engineers gradually clarify their thoughts. To meet these needs, Ferranti Semiconductors has developed the Silicon Design System. This is essentially a design methodology that offers a total logical environment for data entry, design simulation, and full simulation. In addition, its physical environment handles all aspects of the physical chip implementation including autolayout. The design system also provides a design management control environment to ensure adequate design control when a team of engineers is working on a project.



This 3000-gate auto-routable ULA was created by the Silicon Design System's silicon compiler.

One of the most important goals of semiconductor companies is to cut chip design time. With the Silicon Design System, companies can make their own silicon chips in a third of the time it previously required. For a complex chip, that can mean cutting

Anthony V. Walker is currently uncommitted logic array (ULA) product manager at Ferranti Semiconductors, 87 Modular Ave, Commack NY 11725, where he is responsible for managing the ULA Gate Array Design Center. He holds a BS in electronic engineering and physics from the Loughborough University of Technology in Loughborough, England.

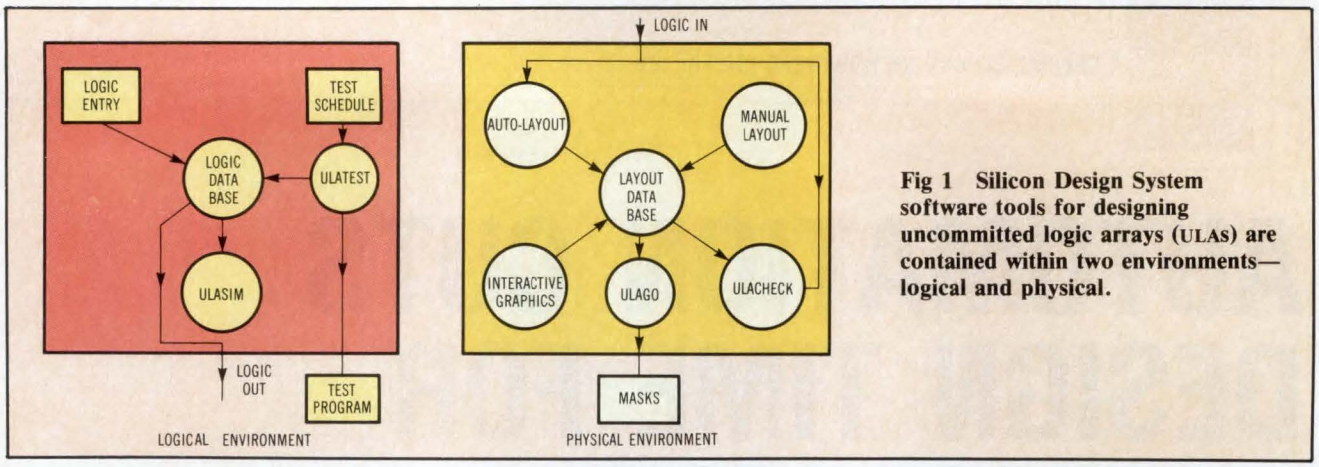


Fig 1 Silicon Design System software tools for designing uncommitted logic arrays (ULAs) are contained within two environments—logical and physical.

design time from 24 to 8 weeks, moving products from drawing board to marketplace much faster. This system can actually draw up the base layers for some chips in 5 min, where it used to take a month. Instead of several weeks to prepare final connections, it can take as little as an hour.

Software for the ULA design system, developed over a period of several years, serves the needs of designers without unnecessary constraints. In too many existing CAD systems, the design automation requirements are more important than the designers in order to make neat computer solutions to problems. But, a good CAD system should offer designers as much freedom as possible within reasonable constraints. CAD should be regarded as the designers' tool, not as the designers' master.

As the complexity of ULA designs increases from 500 to more than 3000 gates, facets of CAD appear that are not always well understood. Common to these is CPU time. Program execution time is not always related to the gate count of the developing system. In physical design rule checking, time is related to size. In the case of auto-layout, time may or may not relate to size but is dependent on the type of problem. For logic simulation, the time factor is related to gate interconnect complexity rather than gate count. Many of the problems in designing complex chips, and the computer time required to run CAD software on them, can be simplified by engineers adapting structured, or hierarchical, design techniques.

Main Elements of the Silicon Design System

Logic entry	Can be via schematic capture, interactive graphics, or Ferranti logic description language (FLDL).
Test schedule	Written in the Ferranti test description language (FTDL). Features include table input, pin change lists, waveform input, and vector manipulations.
Logic data base	The central logic reference data base.
ULATEST	Control segment for all test schedule operations.
ULASIM	Logic simulation segment incorporating the Erica event driven logic simulator.
Layout data base	The central data base for the physical chip description of all designs. From here is produced a dynamic load file to be fedback to the logic data base for final full chip dynamic simulation.
ULACHECK	Full layout checking system for use on the manual, channel-less ULAs.
ULAGO	Instruction for generation of mask and manufacture of prototypes.

Examining the Silicon Design System

The Silicon Design System contains software tools to perform all design tasks associated with designing ULA gate arays (see the Table). These are contained within two environments: logical and physical, each having its own data base. This arrangement separates the design into two independent tasks (Fig 1).

In the first task, which uses the logical environment, the engineer designs the logic using batch or online interactive simulation, and then verifies the design and its test schedule. The second task involves deciding which physical options to choose for the particular application and design and verifying the layout in the physical environment. The tools available for this enable full interactive editing and verification of manually designed arrays or the complete auto-layout of the new AR series of completely auto-routable arrays. Alternatively, after completing the design within the logical environment, the verified logic data base can be transmitted to the local ULA design center where Ferranti system engineers create the chip design's physical aspects.

Developed using virtual memory techniques, the Silicon Design System runs on any host VAX computer system without affecting the other tasks and data on the system. The system is driven by a series of hierarchical nested menus that make system operation natural to engineers, not requiring them to be aware of computer operating systems or file names, etc. It is run within a control environment that offers complete design management and version control. The software is normally supplied on a standalone design station but it can also be run on any VAX system independently of other system users.

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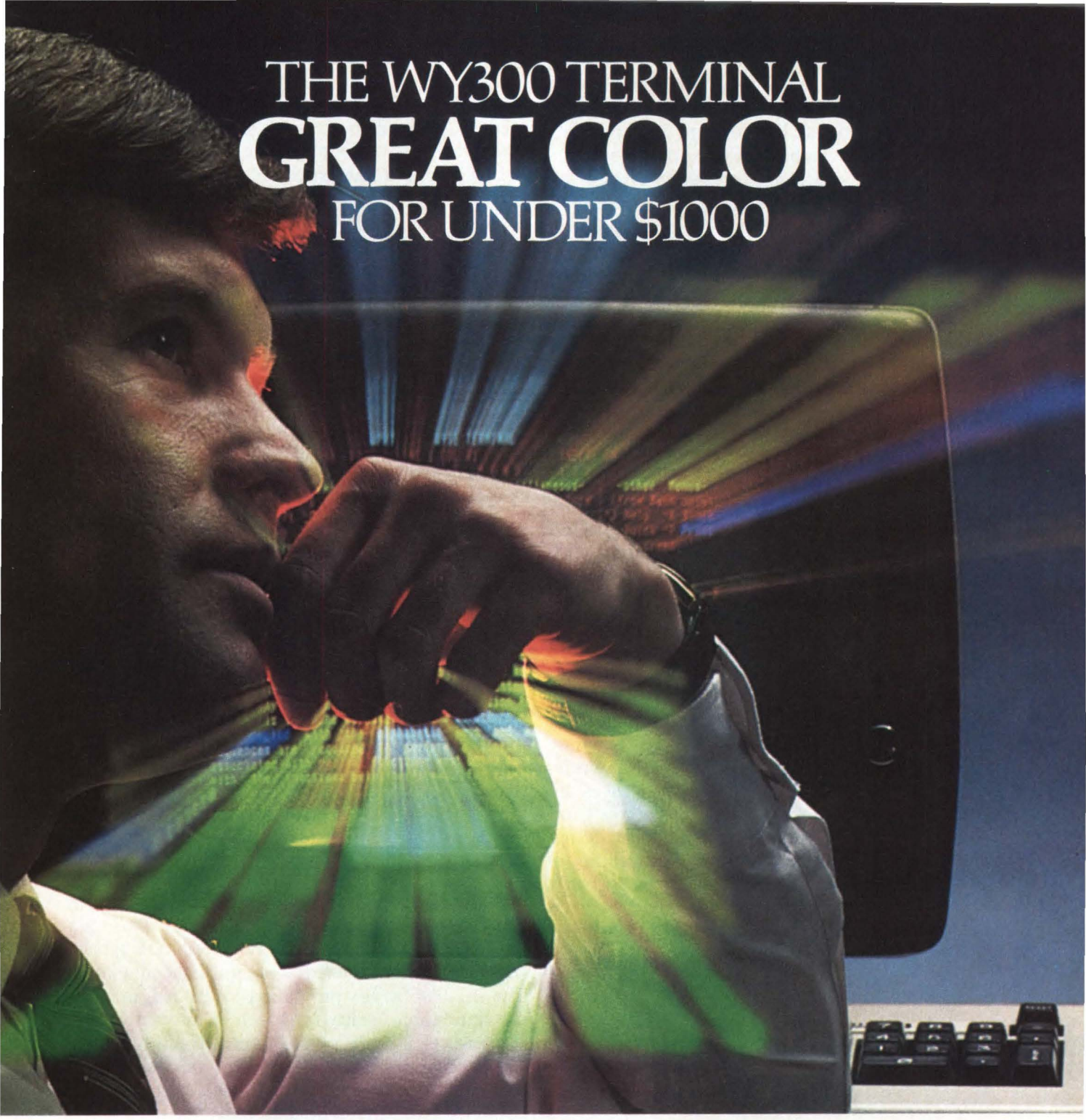

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The logical environment is capable of handling the design from the functional system conception stage through to detailed gate level design. Designs from 100 to 10,000 gates can be developed on the system. As ULAs enlarge and engineers design systems of 2000-plus gates, ordered design techniques become vital. Structured or hierarchical design techniques are recommended for the design of ULA systems. Advantages include faster, testable, and maintainable design, and easier interfacing between groups of engineers working on the same project.

Initially, the design is considered as a series of functional blocks or modules. These modules can be individually simulated and verified as correct logic before being incorporated into the whole system. The initial system can be functionally simulated at a high level before the gate level modules are inserted. Once the system is functionally correct and the modules have all been designed at gate level, the full ULA can be simulated at gate level, taking into account full timing. At this stage, the engineer should have a sound verified design to progress onto the physical chip implementation of the ULA.

The stages given in the design method are very simple and may appear obvious, but frequently engineers do not take a logical course in implementing a design, trying instead to commit it to silicon before verifying it. Alternatively, they may try a full system detailed simulation without ensuring that the system building blocks themselves are correct. As always, design discipline achieves good design. This structured approach to logic design resembles the structured programming techniques that have been longtime standards in the software industry. They have been regarded as producing the most effective method, sometimes the only method, by which a complex program can be developed in a reasonable time.

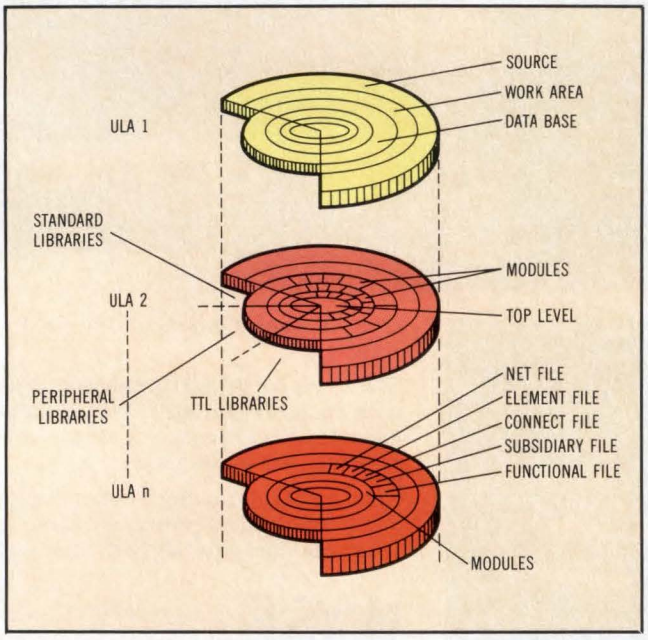

Fig 2 The logic data base stores design information in hierarchical form that supports the use of structured design methods.

Logic designs can be entered into the system in several ways. For instance, most logic design starts on paper. This is the method engineers use to clarify their thoughts before committing the design to the CAD system. If initial drawings of the logic exist, then schematic capture is the fastest and most accurate way of entering the data into the system. It then becomes simple to check the production quality diagram produced by the system for correctness. Generation of the net list from a set of captured schematics is automatic and error free. Logic can also be entered directly with the interactive graphics terminal, which is suitable for small schematics but is normally used for editing design changes.

Ferranti logic description language (FLDL) is another way to enter designs. FLDL is a high level language for describing logic as a completely structured set of hierarchical modules. Typically, the code produced would contain a series of calls to the ULA logic library functions with sections of gate level coding used where required. Validated logic from other simulators can also be accepted.

Simulation system functions

The logic data base is the reference data base central to the overall logical environment. It is a fully structured file data base controlled and accessed by a data base manager, giving complete control over design validity and current version. All design information in the system is stored in a hierarchical form that supports the use of structured design methods. Information in the data base is stored in source, work, or compiled areas (Fig 2). This data base is accessed by the ULASIM simulation system that incorporates the Erica event driven simulator. The ULASIM facility provides a controlled, easy-to-use simulation facility for batch or interactive use. Its features include online interactive simulation, full dynamic timing, and hazard or spike detection. The network description for Erica is automatically compiled from the logic data base.

For the last 15 years, simulation for both circuit and logic level has been available. It is only recently, however, that it has been widely used on design development outside of the larger organizations. This is because it is an area that can be misunderstood; also, computing power and manpower costs can run quite high. Simulation comprises five areas: design, verification, dynamic or timing, test schedule generation, and test schedule verification.

Data used for design simulation can be at one of three levels: circuit, logic, or functional. There is an increasing need for mixed mode simulation (ie, simulation of a group of modules that are not all defined at the same level). Presently, simulation on

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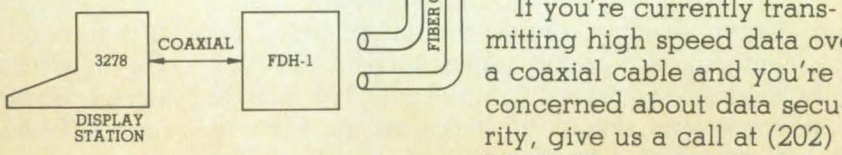

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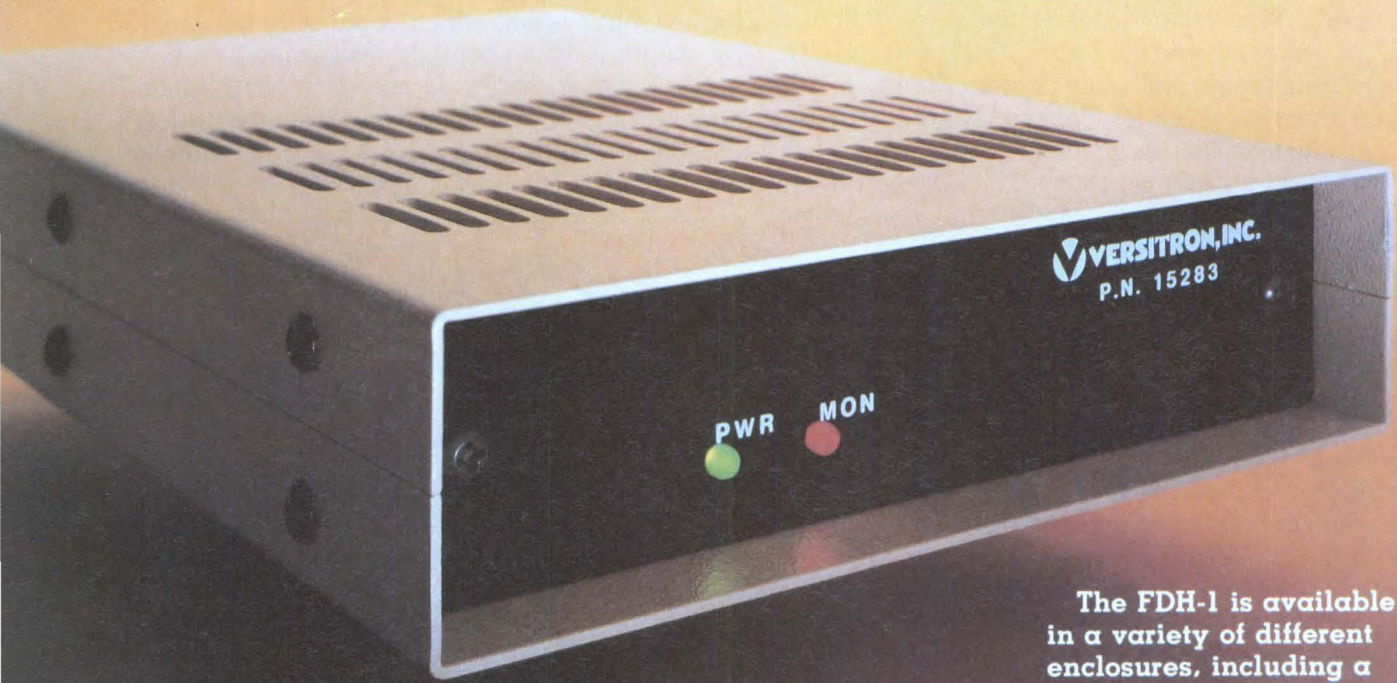

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CIRCLE 99

the Silicon Design System is at logic level with the Spice simulator available for circuit level simulation. Functional level simulation will be available on the system this year.

Most electronic system designs go through several changes before being frozen. The database control environment has been developed for this situation. Actions that change any of this data (eg, recompiling the data base with modified source files) are recorded in a design history record. The integrity of the data base is maintained at all times. Any attempt to use the compiled database information when changes have occurred in the source is accompanied by relevant warning messages.

Available with the data base are separate logic libraries to support the full range of arrays. Database features include the automatic calculation of gate delays and power requirements (Fig 3). System capabilities include interactive simulation, batch simulation, dynamic timing simulation based on nominal fan-in, fan-out, and related delays plus physical tracking delays. Other capabilities include functional level simulation based on the Ferranti behavioral level language (FBLL), a Pascal-like language for abstract functional behavior descriptions; hazard and spike detection; test schedule verification; and waveform output analysis on VT-100 type display terminals.

ULASIM is based around the Erica event driven logic simulator. Erica's key commands, which can be used interactively or from batch control files, include define vectors, define signal, set value of net or vector, increment vector, trace nets, modify trace command, print trace at given time step, and print trace on given net change. Additional commands include halt race when network stable, halt simulation on given net change, initialize, save and restore state of network, modify gate delays, and compare nets or vectors with given value.

The ULATEST area within the logical environment handles the development, verification, and translation to tester machine code of the test schedule. Complex stimuli may be required to drive logic designs. The Ferranti test description language (FTDL) lets engineers define their initial test schedule in a high level language. FTDL allows engineers to describe a test schedule in the most convenient way for a given design. This could be truth table, pin change lists, vectors, and waveform input. Detailed timing requirements for full dynamic simulation can be included within this test schedule as required. The FTDL to Erica stimuli translator can verify the test schedule entered into ULATEST against the logic. This process of test schedule verification is completely automatic; the system produces a printout of errors found.

The physical environment handles full physical design verification for the traditional channel-less ULAs. These arrays offer state-of-the-art performance and can contain a large linear content if required. This environment also has a 100-percent automatic auto-layout system based around new chip architecture design and a set of silicon compilers. This approach solves all the traditional auto-layout system problems associated with uncompleted nets and the need to manually edit them.

The auto-layout system

Traditionally, auto-layout systems have supposedly been able to achieve a certain percentage completion rate for utilizing a certain percentage of the available silicon or gates. In practice, the percentage completion achieved on these systems is quite variable and dependent on the interconnect complexity inherent in the logic. A thousand inverters in series is very different from 1000 gates attached to a 16-bit wide bus.

Unconnected nets, even if they are only a small percentage of the design, can take an engineer days or even weeks to route on a graphics screen. The nets left by the system for the engineer to route are usually the most difficult.

In studying auto-layout systems for several years, Ferranti engineers came to two conclusions. First, an auto-layout system and the range of arrays it is to work on must be developed together. Secondly, penalty in manufacturing costs, and possibly development costs, are incurred when an auto-layout system is used. The study also concluded that what was needed was a 100-percent success auto-layout system, which could only be achieved by adapting silicon compiler techniques.

Chip architecture for the company's auto-routable range of arrays (AR series) was developed in close conjunction with the associated silicon compilers. The architecture is unique in its use of minor

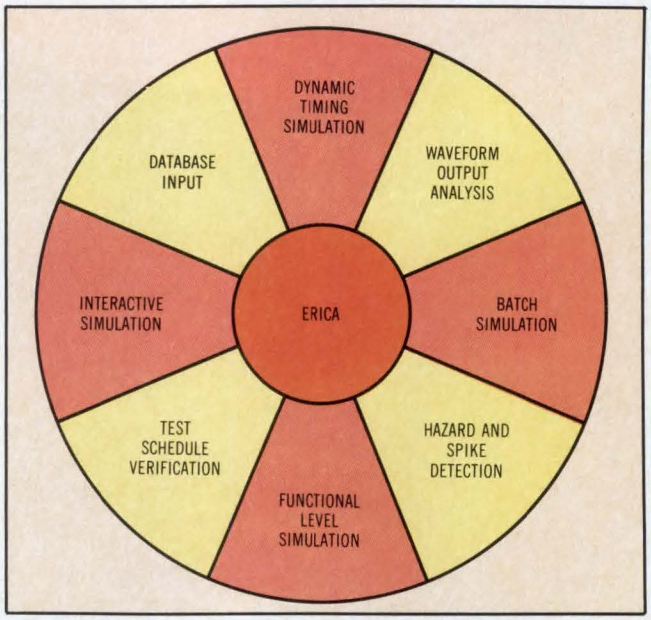

Fig 3 The ULA data base includes numerous simulation capabilities.

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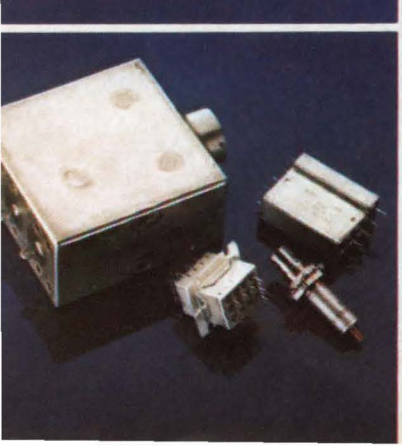

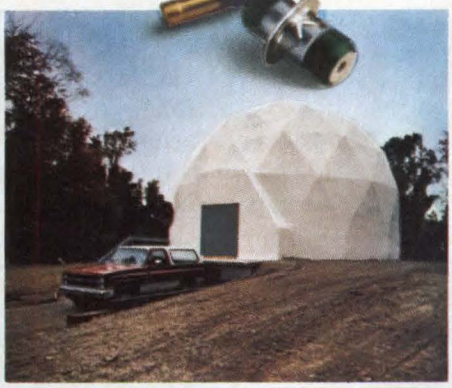

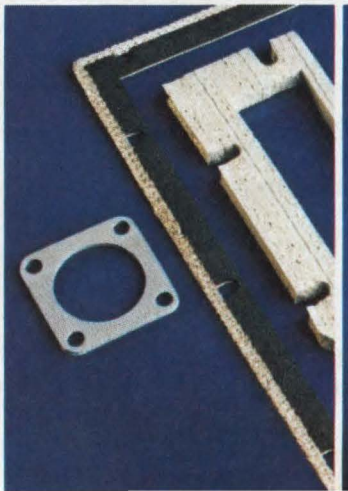

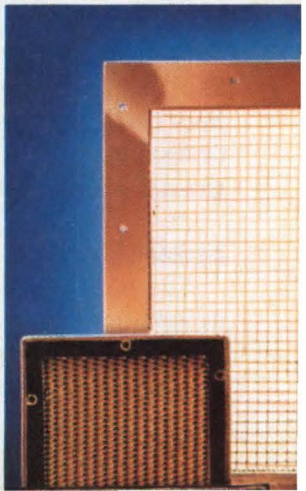

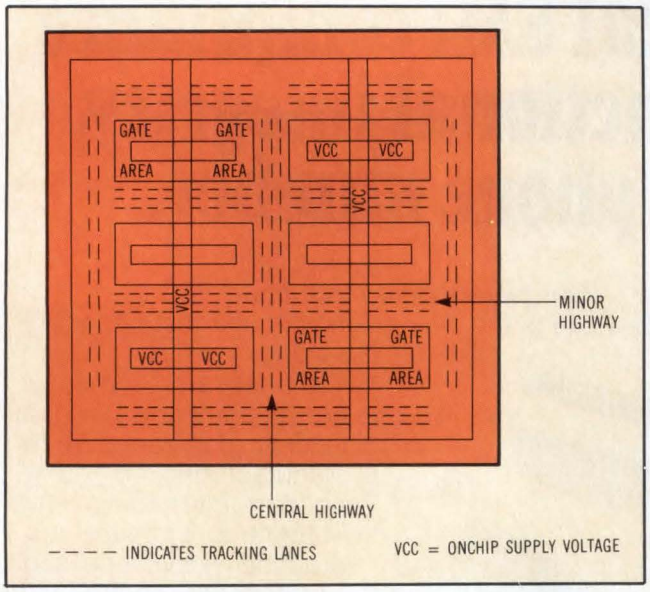

Fig 4 The AR series of auto-routable arrays uses central and minor highways.

highways, central highways, and feedthroughs between the gate cells (Fig 4). Routing accessibility has been greatly improved from the pure highway approach by the introduction of a number of feedthroughs between the gate cells (Fig 5). The combination of silicon compiler and architecture has produced an auto-layout system that is successful on single-layer metallization interconnect.

The Silicon Design System can now be used on the full range of the company's channel-less arrays as well as the AR series.These arrays are initially available in a range from 1000 to 5000 gates with gate speeds down to 1 ns. Arrays without channels are efficient users of silicon and can be produced in a way that is economical for designs requiring full custom-type volumes and flexibility. The AR arrays are approximately 25 percent larger in silicon area but can be laid out completely automatically.

The AR array diffusion layers are produced by the silicon compiler from eight defining parameters. This compiler takes less than 5 min to produce the necessary design file, ready for output to the pattern generator. As a result, a new member of the array family can be generated in a very short time and is guaranteed to be correct.

The auto-layout system will do a 100-percent auto-layout from the logic data base to design file—ready for output to a pattern generator—in approximately one hour. The system's success is due to using a series of silicon compilers, and designing the system so that it takes advantage of the design's structure in the logic data base.

System hardware

The hardware was chosen to create a powerful, adaptable system capable of future enhancements. A 32-bit CPU gives the power needed for simulation of large logic circuits. This, combined with a high resolution graphics system and a 6800-based graphics manager gives mainframe-like power to a computer facility in a package compact enough to be used as a completely independent engineering design tool.

A VAX-11/730 with a 1-Mbyte memory, an R80 120-Mbyte Winchester disk, and an RL02 10-Mbyte disk system constitute the hardware. The high speed interactive graphics are provided by the Westward 2115 high resolution display monitor linked to a graphics manager. This graphics manager contains 500-Kbyte local memory and gives very high speed windowing, painting, and editing capabilities. There is also a full-size digitizer tablet and optional plotter.

Silicon Design System software is available for operation on any host VAX computer system but is also packaged as a standalone advanced workstation

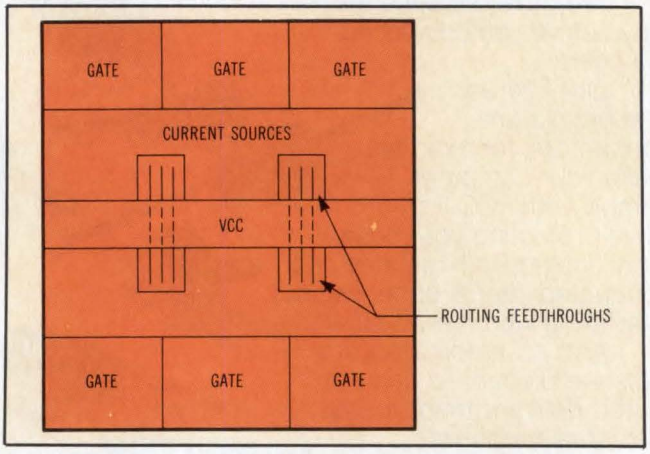

Fig 5 A closer look at an AR series gate array reveals routing feedthroughs between the gate cells.

based on the VAX-11/730. This standalone system gives design engineers the full CAD tools required for ULA design in their own office. In most organizations the design group's large VAX-11/780 installation would be used by a large number of people and could have perhaps 10 or 20 tasks running concurrently. VAX-11/780s are usually considered too expensive to be used on dedicated design tasks. In these situations, the VAX-11/730 often offers the designer a faster response for CPU-intensive operations such as interactive graphics and simulation.

Once a design is completed on the system, it is transmitted to a Ferranti design center using the 2400 dial-up modem service for output to a pattern generator and prototype manufacture. At the same time, the test schedule is transmitted to create the program for the appropriate tester.

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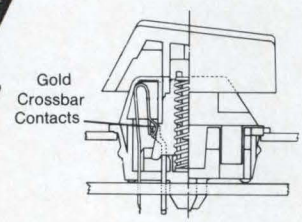

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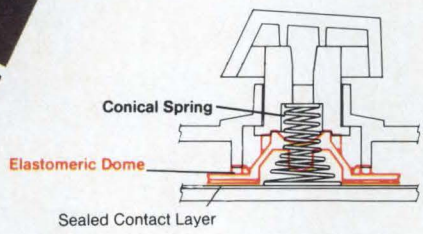

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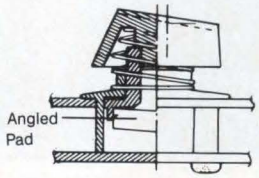

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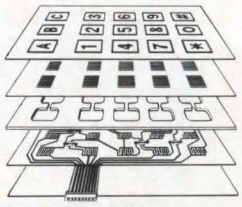

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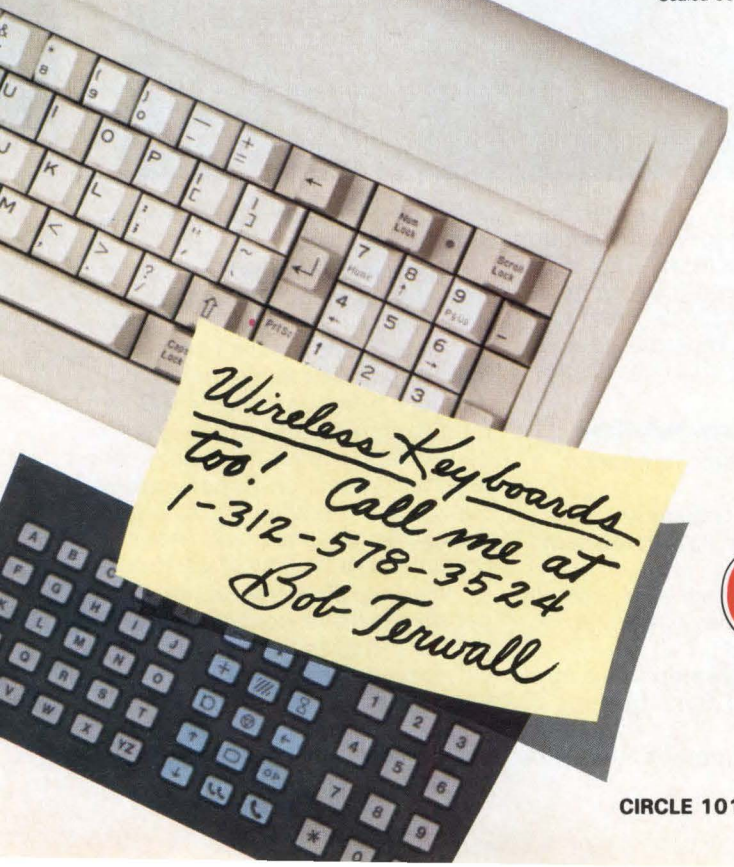

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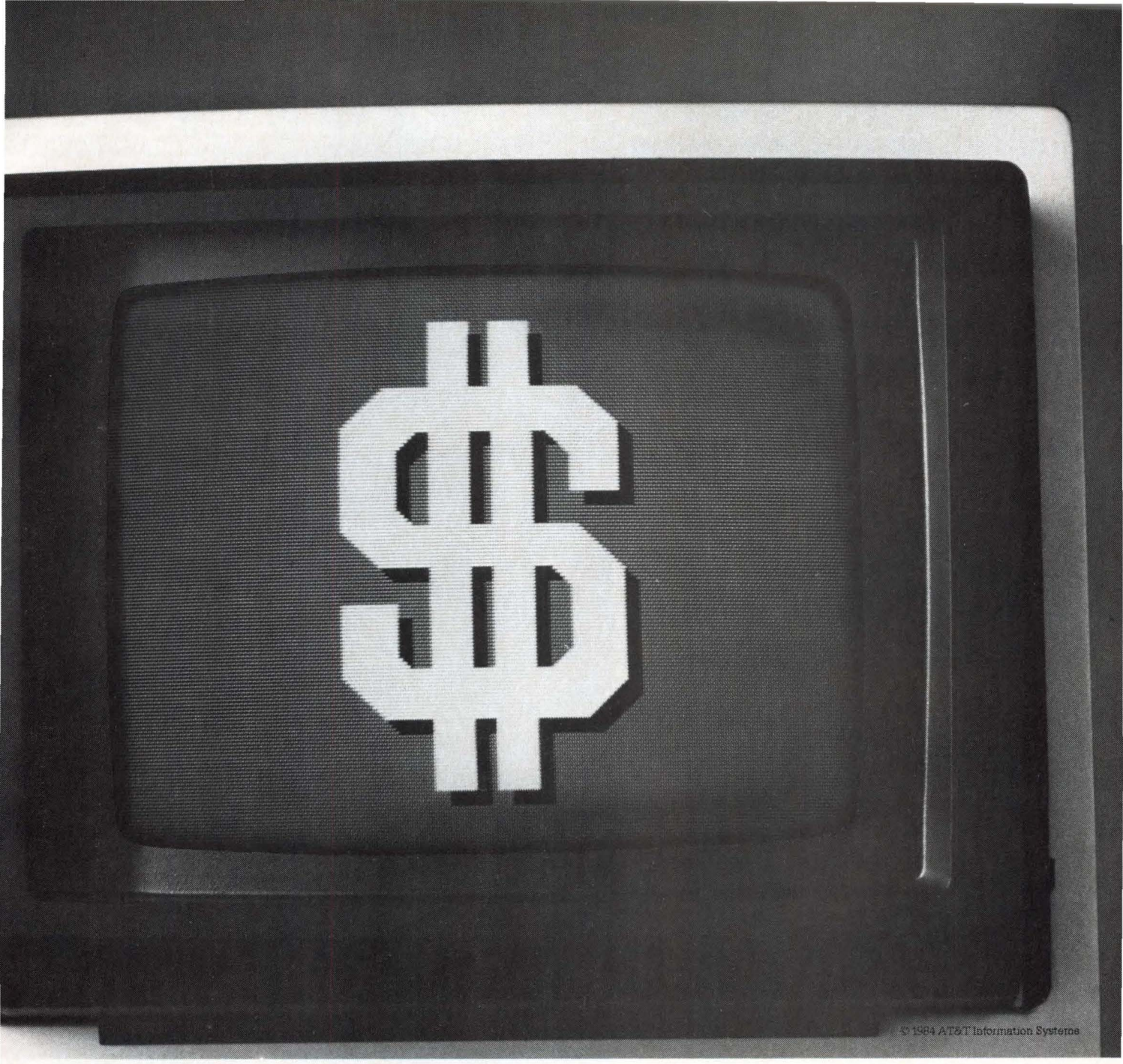

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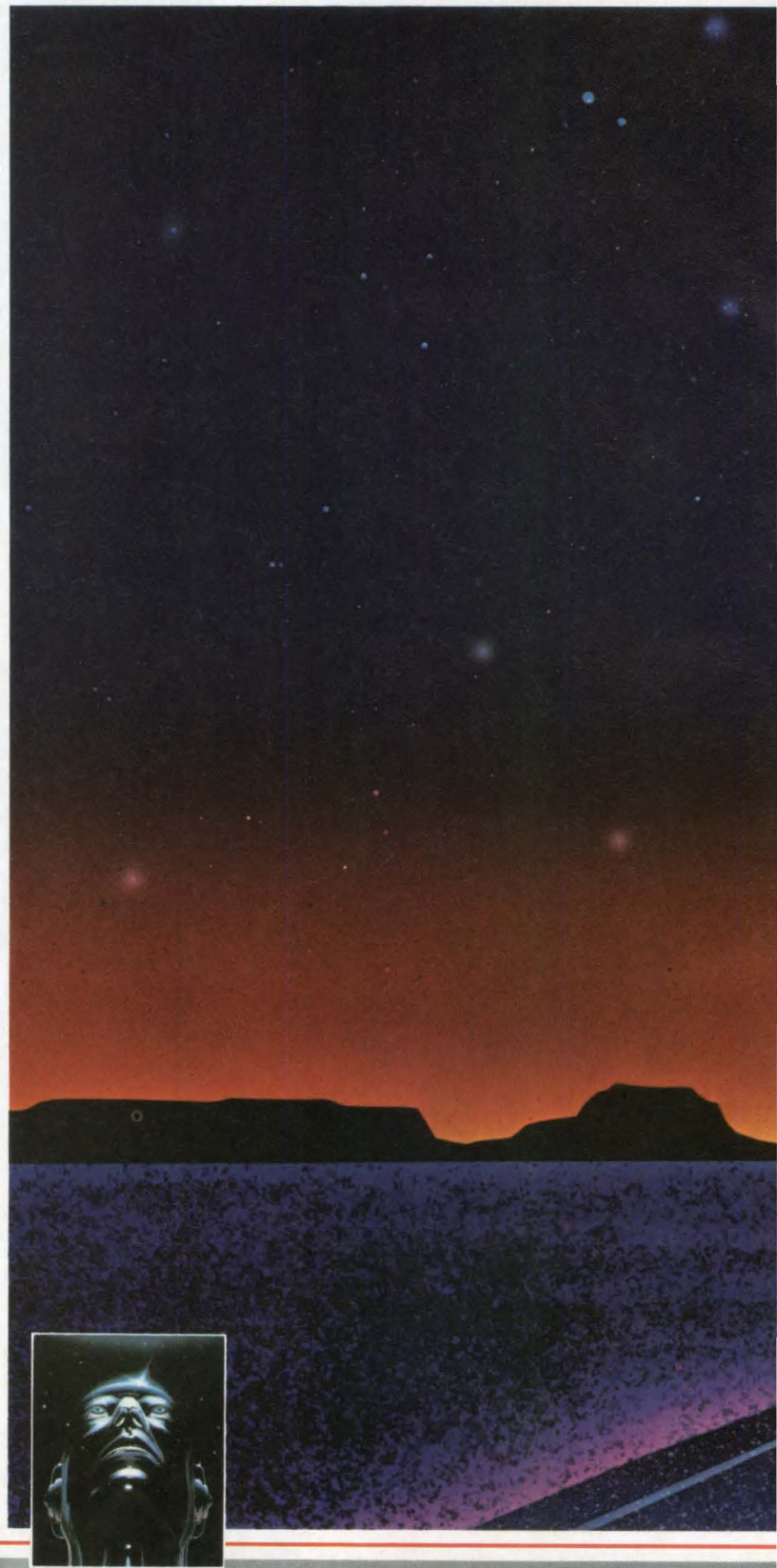
Dynamic RAM		•	•				•		•		•		•	
ROM	•		•							•	•	•	•	•
PROM				•	•		•	•	•					
EEPROM			•						•					
UV EPROM	•		•						•	•	•	•		

[1]MMOS refers to Mixed-MOS technology (CMOS and NMOS).
[2]High speed 4K and 16K devices available.



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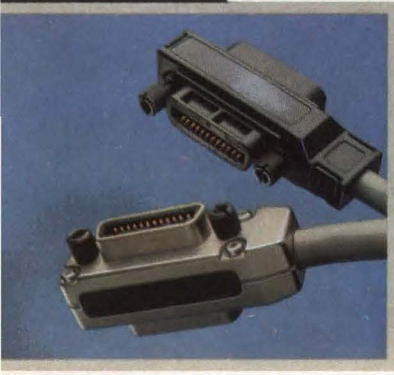

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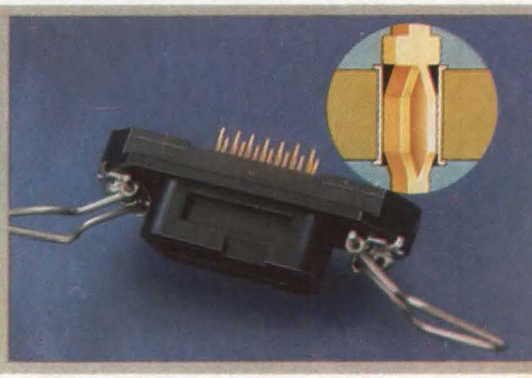

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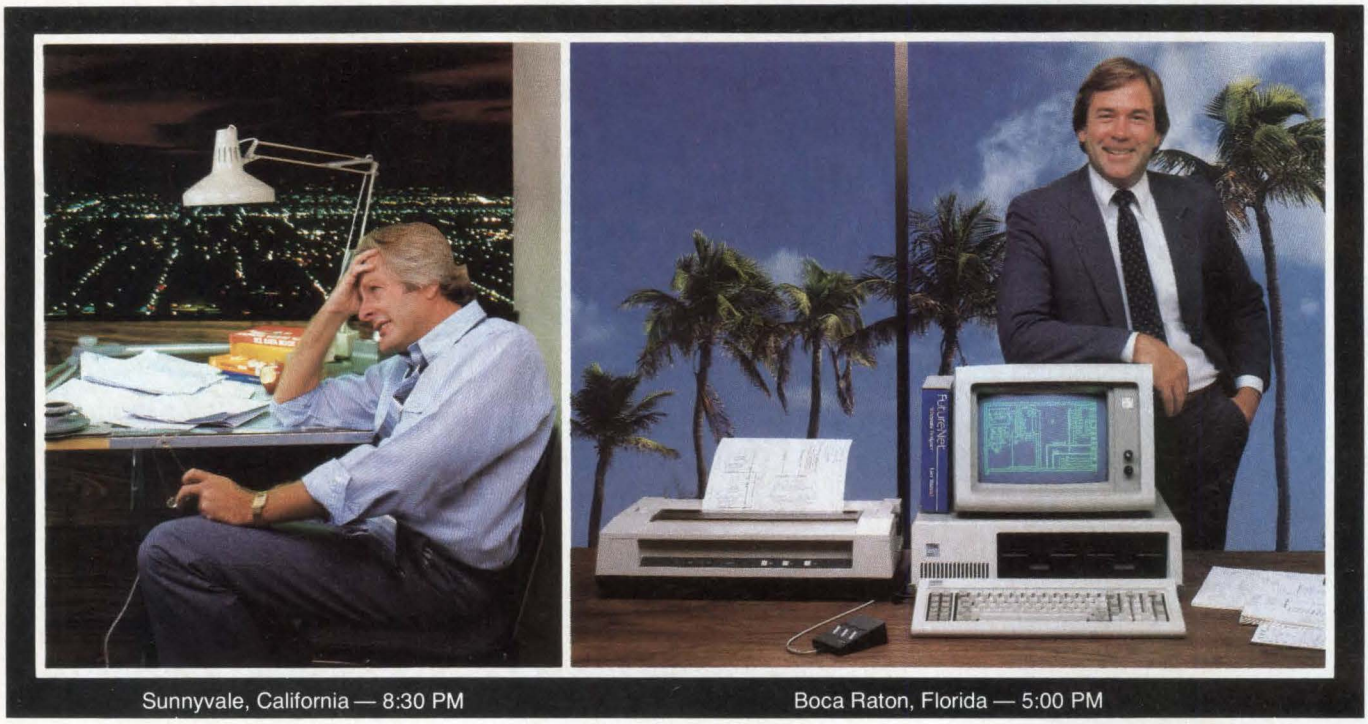

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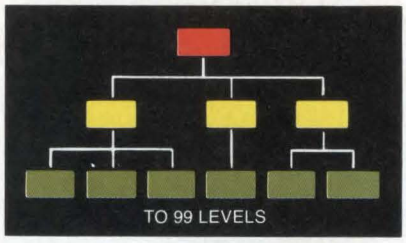

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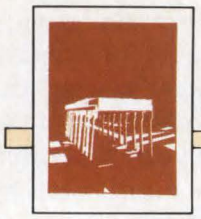


MICROPROGRAMMING AND BIT-SLICE ARCHITECTURE

Use microprogrammable CMOS/SOS bit-slice processors for sophisticated high speed applications.

by Kaare Karstad

Although the idea of microprogramming is more than 30 years old, and most computers today are microprogrammed, the concepts of bit-slice architecture and user-microprogrammable systems are unfamiliar to many in the growing number of microcomputer design engineers. It seems important, therefore, to take the mystery out of the terms "bit-slice" and "microprogramming" and relate them to familiar system organizations.

Microprogramming a computer is not the same as programming a microcomputer. Microprogramming is simply a technique for designing control systems. However, a control system could be a standalone system simply turning control lines on and off in some timed fashion. In a classical von Neumann computer architecture, a main memory contains instructions and data on which it will operate. The ALU processes the information, and a computer control unit (CCU) oversees the flow of control signals that determine ALU operation and steer data to and from the ALU, as well as into and out of I/O devices. Other functions essential to operation include a memory address register (MAR) and program counter, some scratchpad registers incorporated in the CPU, and an instruction register (IR) made part of the CCU block. The CCU decodes the operation code portion of the IR and generates the sequence of control signals needed by the CPU, memory, and I/O portions of the system.

Organization inside a typical microprocessor chip is divided into two major parts: the control system, which makes decisions and issues commands to the rest of the hardware; and the ALU area, where calculations are actually carried out. Control lines connecting hardware logic direct the processing and flow of data. These lines must be turned on and off at the right moment in order to get the right control signals to the right place. Precise timing is called for so the processor's entire rhythm is synchronized to a clock. Each machine level instruction corresponds to a sequence of clock cycles, with each clock cycle marking a single information transfer along the data path. The control system's function is to supply control signals during the correct clock cycles.

In the early days of computers, the control system was hardwired with a network of logic to recognize each machine level instruction. Each instruction generated a different sequence of control signals. Thus, the system became quite complex as the number of instructions increased. Changes could only be made (and bugs removed) by rewiring.

In his 1951 paper, "The Best Way to Design an Automatic Calculating Machine," M.V. Wilkes proposed a new way of designing control systems to overcome the complexity and inflexibility of hardwired or permanent control systems. He suggested thinking of the control system as a matrix (see Fig 1). Each row of squares corresponds to a clock cycle and each column relates to a control line. The control lines go to the CPU and other parts of the system, and choosing a sequence of

Kaare Karstad is a member of technical staff with RCA's Solid State Division, Route 202, Somerville, NJ 08876. He holds an MSEE from Norway's Institute of Technology.

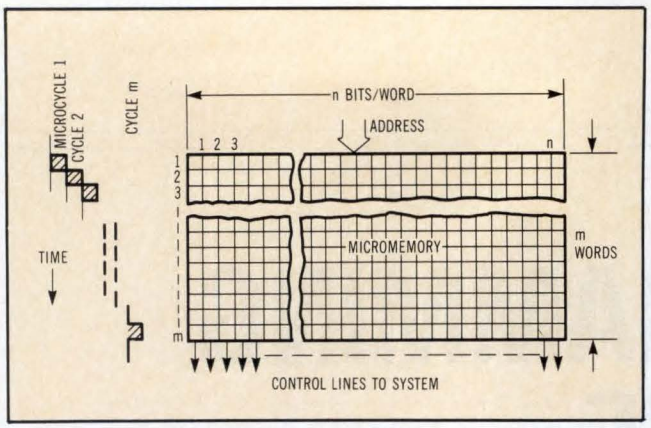


Fig 1 With the control system designed as a matrix, the hardware equivalent is a memory structure (micromemory) where each row of squares corresponds to one clock cycle or one microinstruction and each column relates to a control line.

operations becomes a matter of putting the right binary symbols in the squares. A "1" signifies that a particular control line is on during a specific clock cycle.

Clearly, the hardware equivalent of the control matrix is a memory structure. It is called micromemory to distinguish it from main memory. The content of each cell in a row determines the state of the corresponding control line for the duration of one clock cycle. The content of each row becomes a microinstruction or a microword. The machine level instruction, which is fetched from main memory and stored in the instruction register, serves to select a row (or sequence of rows) in the control memory. Hence, the machine level instruction (hereafter referred to as macroinstruction) becomes an address that designates a row or a start address in micromemory. A microinstruction sequence that executes a macroinstruction is called a microprogram. These concepts are illustrated in Fig 2 which shows the macroinstruction interpreted or decoded by the microcode in order to yield control signals that manipulate the information flow in the data path.

The number of bits in a microword can be quite large, so designers developed techniques for reducing microprogram memory cost. Generally, when executing a single microinstruction, only a few of the control lines are active; the rest are off. It is often possible to supply the same control information by encoding. The approach is to find two wires that are not both active for the same microinstruction, eliminate one, and make the other serve a dual purpose. This results in a larger number of microinstructions, but each requires fewer bits.

An encoded set of microinstructions is described as "vertical" because the resulting microprogram usually appears tall and narrow. A nonencoded set of microinstructions is described as "horizontal" because the resulting microprogram is usually short and wide. Horizontal microcoding generally means a faster computer, since more operations can be done simultaneously.

Specially tailored designs

Most microcomputers today are microprogrammed, but few of them allow the user to write the microcode. The microprocessors have a fixed-instruction set and are general-purpose problem solvers. In a user microprogrammable configuration the computer can be specifically tailored for a given application and the user designs a unique, optimum instruction set. Most microprogrammed control sections store microinstructions in ROMs or PROMs. It is, however, possible to use RAMs for the micromemory (ie, have a writable control store). By loading different instruction sets, a fixed hardware configuration appears as different machines dependent on the instruction set. The design is said to emulate different computers. It is also possible to change the microprogram memory's content dynamically with a writable control store while the computer is in operation.

Bit slice machines differ from single-chip processors primarily in the architectural philosophy underlying their CPU design. Single-chip microprocessors

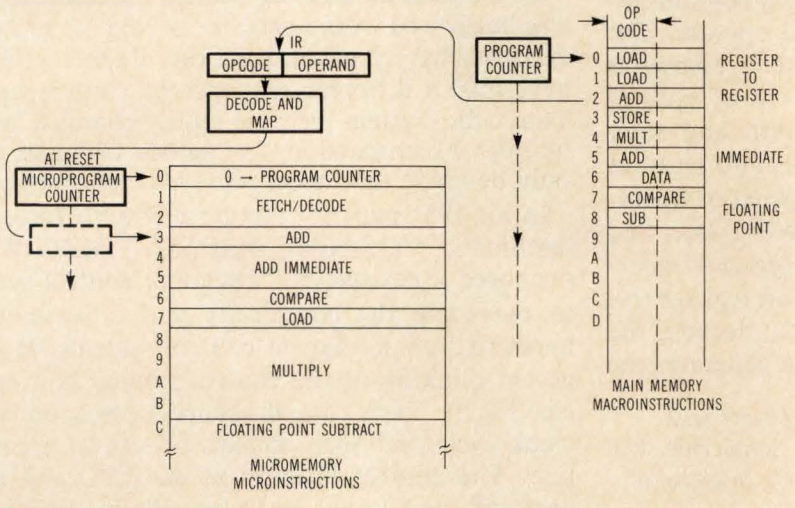
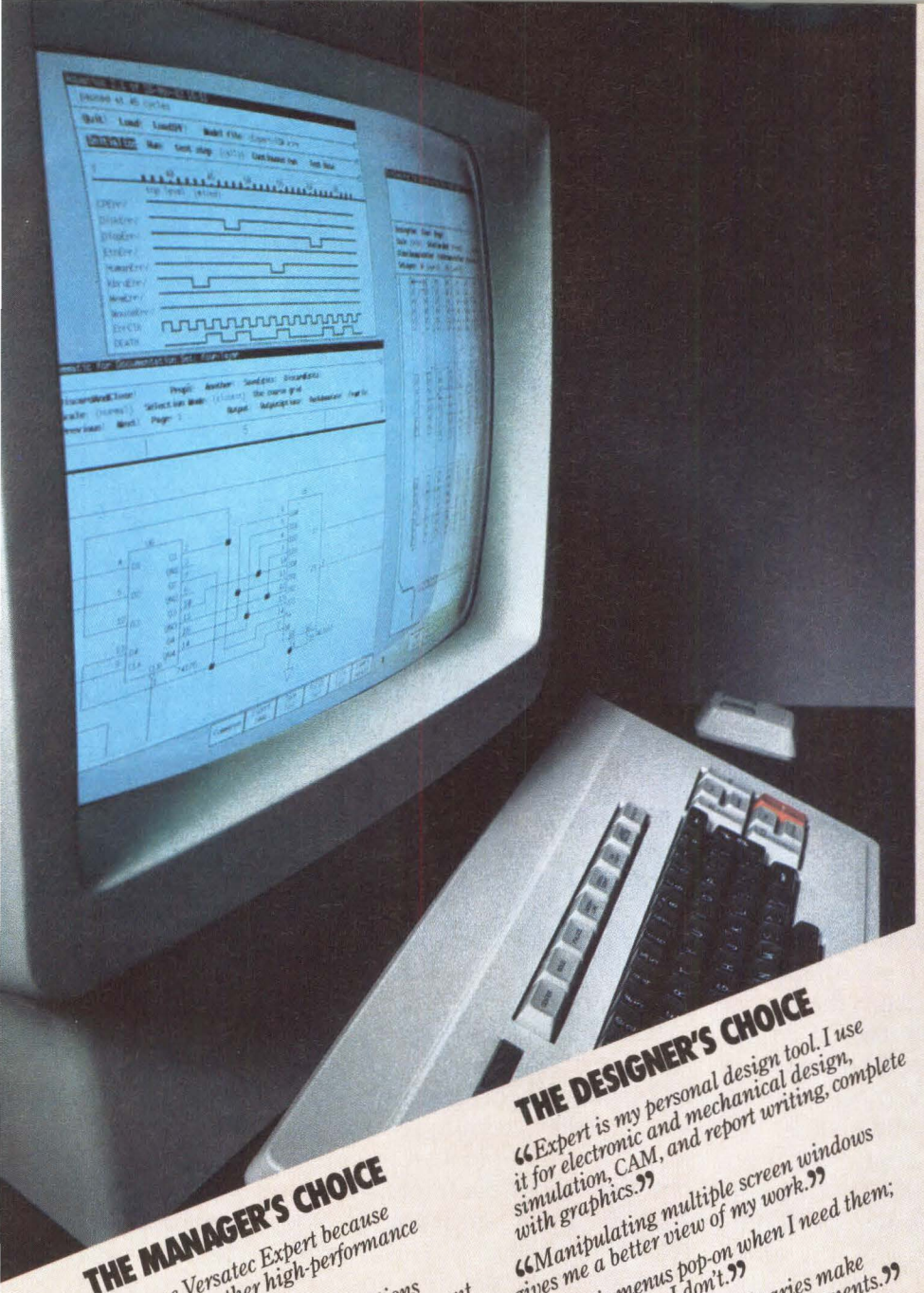


Fig 2 During the interplay of main memory and micromemory, each machine level macroinstruction is decoded and interpreted by one or more microinstructions that yield control signals to the system.



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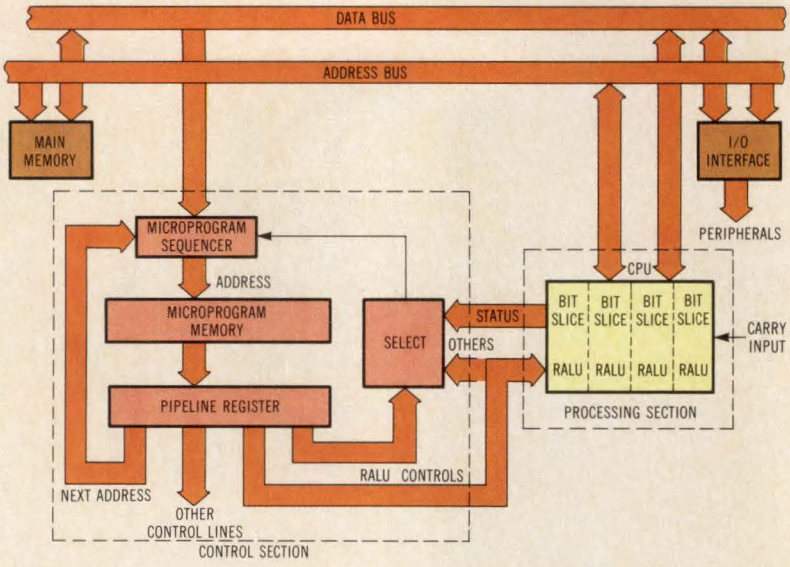

Fig 3 Pictured is a functional diagram of a microprogrammable bit-slice microprocessor. The arithmetic or logical operations and the sources and destinations for the ALU are the same for all slices.

have data processing functions and control functions (ie, the decoding circuitry for the instructions) hardwired on the same chip. Single-chip processors have a predefined and unchangeable word-length architecture and a fixed instruction set. The opposite holds for microprogrammable bit-sliced microprocessors. They can be configured to provide a wide variety of digital system architectures with various word lengths and instruction set capabilities.

The term "bit slice" is derived from the limitations on chip complexity, pin numbers and chip size. The processing section of the CPU is therefore partitioned along functional lines vertically instead of horizontally. Vertical partitioning slices the registers and the ALU into equal length and functionally equivalent parts called bit slices. These bit slices are sometimes called the register and arithmetic logic unit (RALU). Commercially, the RALU generally handles 2, 3, or 8 bits and can be cascaded to form a wider processing section to any width that is a multiple of the basic unit. Fig 3 depicts a bit-slice microprocessor that is microprogrammable. The cascaded arrangement requires all control lines for each slice to be connected in parallel, and the carry output of one chip is connected to the carry input of the next. Arithmetic or logical operations and the sources and destinations for the ALU are the same for all slices. The input data bus is divided into sections of the proper length when entering the processor slices, and the output data bus is recombined upon exiting.

The control section, as shown in Fig 3, typically consists of a microprogram memory, a microprogram sequencer or controller, and some additional logic. The microprogram memory, which can be ROM, PROM, or RAM, contains the microinstructions that specify the steps through which the machine sequences and controls parallel operation of the bit slices. The sequencer provides the macroinstruction decode logic and determines how the next microprogram address is generated for sequencing the microprogram.

The size of the microprogram memory expands vertically, dependent on the number of macroinstructions that are included in the instruction set. Horizontally, the width of the microinstruction is expanded by cascading a number of similar memory chips. A nonencoded microinstruction can be as wide as 200 bits.

All arithmetic and logic operations are carried out in the processing section. This section is composed of functionally equivalent bit-slice chips. A typical slice generally contains some or all of the following: an ALU, a multiple word register file, a shifter, input and output data lines, and control inputs.

In the basic configuration, the microprocessor fetches macroinstructions from the system's main memory under the direction of microinstructions read from its microprogram memory. The microprogram sequencer interprets the operation code of the macroinstruction (ie, mapped into a microprogram memory address and then executed as a series of microsteps). If any operand portions of the macroinstruction are routed to the bit slices, such operands are either used in computations or in main memory address manipulation.

It is important not to confuse the functions of main memory and micromemory. The system's main memory contains the application program expressed with macroinstructions or machine level instructions. The control section's microprogram memory contains microprograms defining the macroinstructions that give the machine its personality or specific instruction set. Note that the microprogram memory also generates control pulses timed to control the rest of the system. These pulses typically latch data into registers or enable data onto buses.

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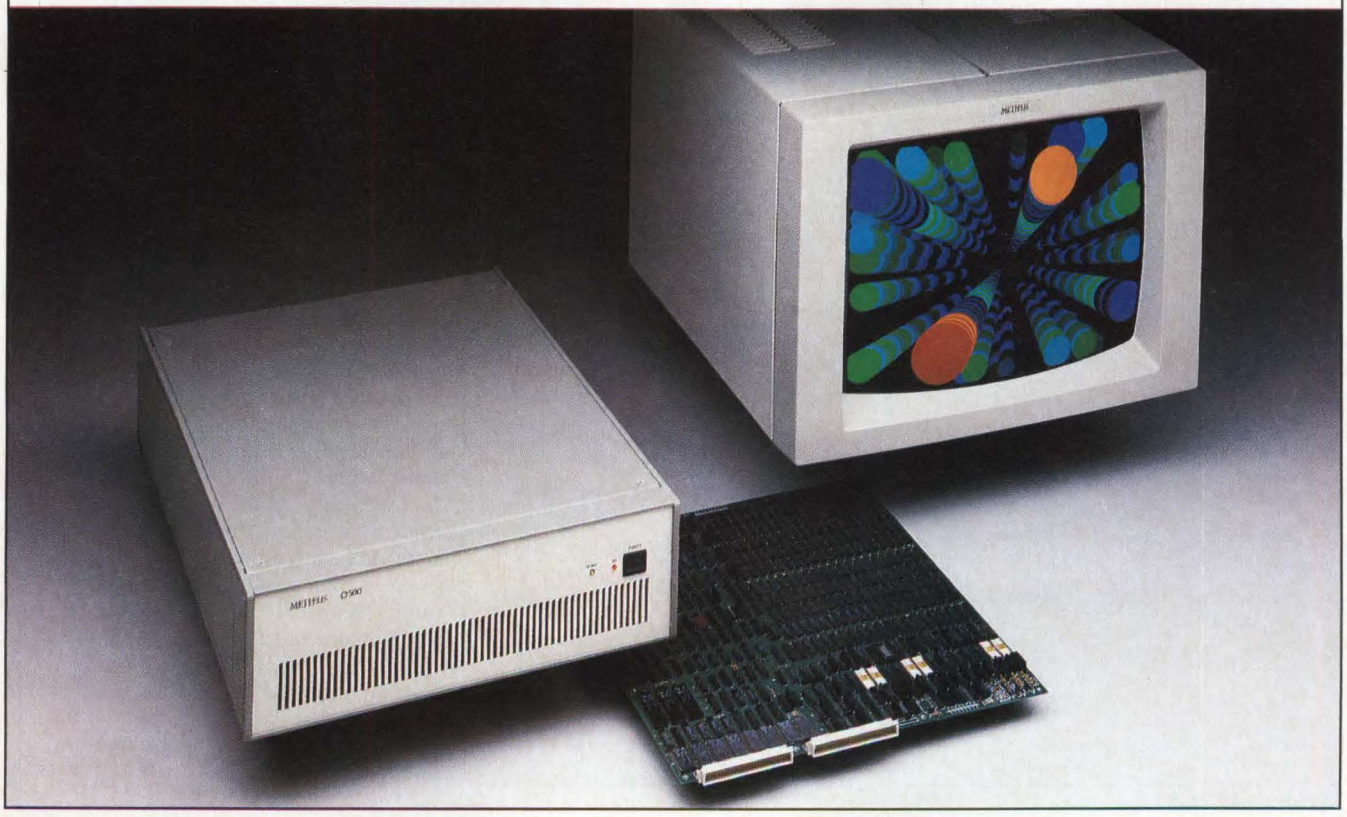


CIRCLE 106

A designer of microprogrammable bit-slice computers is concerned with two levels of programming: the macro level, and the micro level. Designers must define or choose a macroinstruction set for application programs, as well as implement a set of microprograms that executes macroinstructions and gives the computer its unique character.

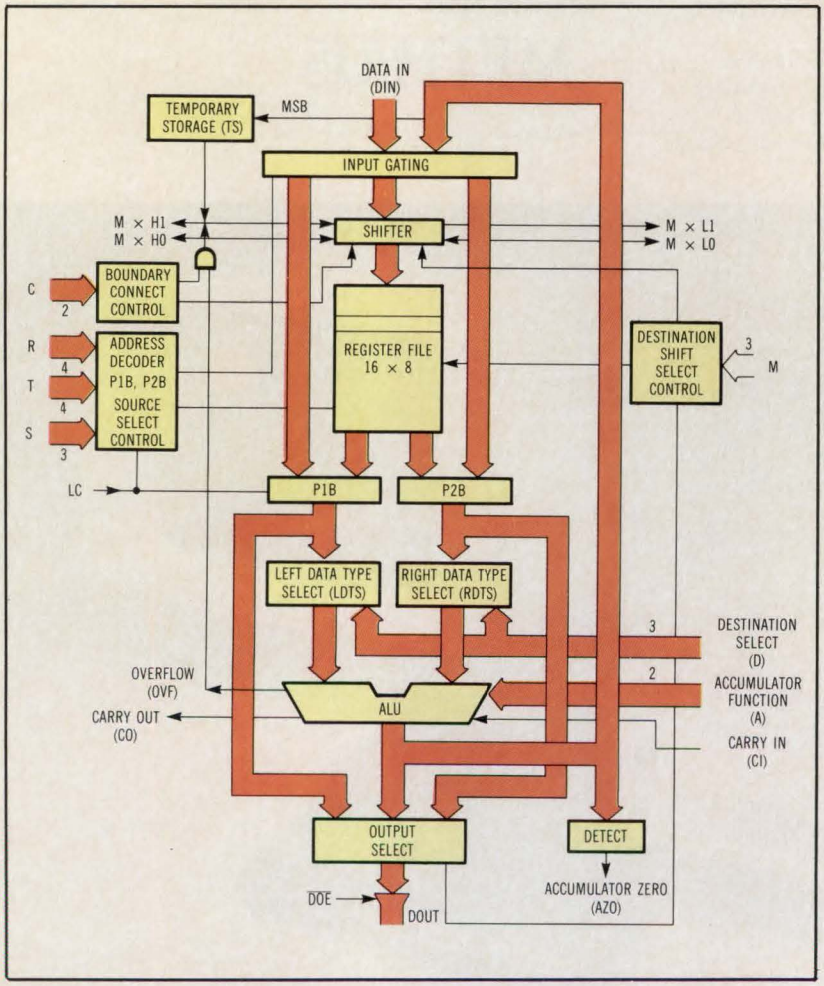
A simple but functionally operational 16-bit microcomputer that employs both microprogramming and bit-slice architecture, as discussed above, can be constructed from the key building blocks of the Emulation/and Programmable IC (EPIC) chip family. This family contains more than a dozen LSI CMOS/silicon on sapphire (SOS) chips. In various combinations these chips can be configured into microprogrammable computers with great flexibility in architecture, data format, and overall capability. In addition to all the advantages of CMOS technology, SOS offers excellent tolerance to radiation, important in aerospace applications. The EPIC family centers around an 8-bit slice, two controllers or sequencers, an interrupt controller,

General processor unit GP001

The GP001 is an 8-bit CPU bit slice implemented in CMOS/SOS technology. The part is comparable to AM2901/2903 in speed and performance, but has the added advantage of an 8-bit wide slice, low power of CMOS, and the high radiation tolerance of SOS. The GP001 can be cascaded to allow emulation of any computer with word lengths in multiples of 8 bits.

The ALU functions selected by a 2-bit field A are ADD, AND and OR. The operands are derived from two port buffers P1B and P2B, but can be modified before entering the ALU by a 3-bit select field D. The data type operands, left and right, can feed the ALU unmodified, inverted, or equal to zero. Hence, a greater number of arithmetic and logic functions can be executed. At a minimum, the following operations can be selected and performed in one microcycle: ADD, SUBTRACT, COMPLEMENT, INCREMENT, CLEAR, PASS, AND, OR, NAND, NOR, and SHIFT RIGHT and ADD. An additional control field also allows SHIFT LEFT or RIGHT ONE BIT and SHIFT RIGHT TWO BITS. In general, the instruction fields support high speed iterative operations, multiplication, nonrestoring division and floating point arithmetic. Each bit-slice has carry-in and carry-out leads, with fast group look ahead carry incorporated on the chip.

The register file is comprised of sixteen 8-bit words and is a dual-port file accessed by the two address fields R and T (see Figure). The content of a register addressed by the R field is transferred to the left port buffer P1B, while the content of the register addressed by the T field is transferred to the right port buffer P2B. If R = T, of course, identical data is read from the two ports simultaneously. Each register can be written into from the data in leads when selected by the R field and the clock is high. The register file and the port buffer act in a master/slave configuration. Thus, pipelining the CPU is possible, ie, previous stored content in a register can be read while new data is loading during a high clock cycle. In addition to the write mode just described, the port buffers (P1B and P2B) can operate in other modes depending upon the 2-bit S field; data in can be latched into P1B directly or stored indefinitely in P2B, or P1B and P2B can act as slaves to the register file.



The megabits, together with the C field, provide left/right shift capability for the ALU output before it is stored in the register file. The shift select (M) moves the ALU output one or 2-bit positions right, one position left or pass data without shift. The 3-bit boundary control field C determines what is output on the shift lines and which ones are in input mode. When cascading bit slices, the high shifter output leads (MXH) are connected directly to the low shifter output leads (MXL) of the next more significant slice. For ring-shift operation, no external parts are required. The most significant leads MXH are looped back to the least significant leads MXL. The ALU's status is provided by separate carry-out and All-Zero-Detect leads. Overflow of the ALU is indicated on the MXH1 line which is timeshared.

an 8 x 8 multiplier slice, RAM and ROM, and a number of universal gate arrays that integrate the logic required to join the major system blocks into a minimum-parts computer system.

The tutorial computer uses the 8-bit slice GP001 (See Panel, "General processor unit GP001), and the sequencer GP502, but otherwise it uses readily available CMOS RAMs and erasable PROMs with high speed (74HC) CMOS latches and registers to connect the key system parts into a viable computer. For practical reasons, the system runs at 5 V since speed is not a primary factor in the demonstration model. The EPIC chips should be operated at 10 V for maximum speed, but this conflicts with the voltage rating of the 74HC family of high speed logic. The 5-V system is satisfactory to demonstrate concepts and for evaluation. In an optimized full speed minimum-parts system, a designer might want to choose some existing EPIC parts for interfacing the control and processing parts of the system, or choose to implement custom logic in CMOS/SOS universal gate arrays.

The control section of a microprocessor gives the machine its personality. The two main parts of the control section are the microprogram memory, which holds the microinstructions, and the microprogram sequencer. The main purpose of any sequencer is to present an address to the microprogram memory so that a microinstruction is fetched and executed.

Sequencers can be implemented for simple sequential control circuits without branching capabilities. In a sequencer's simplest form, all that is required for stepping through the microinstructions is an address counter. The address of the next microinstruction is selected by incrementing the address counter by one on each clock cycle. The counter technique permits only sequential control; neither conditional nor unconditional flow is possible. In another configuration, the address register is loaded with the next address from a field in the currently executed microinstruction. This adds unconditional jumps in the program but no conditional change in control flow. Logic and features could be added until a flexible and powerful LSI controller resulted. One such device is the GP502, which is essentially a small microprocessor in its own right with its own instruction set. The GP502 is implemented in CMOS/SOS technology and is functionally and pin equivalent to the popular industry standard AM2910.

The GP502 allows addressing of up to 4 Kwords of microprogram. The controller contains a four-input multiplexer used to select either the register/counter, microprogram counter, direct input, or the stack as the source of subsequent microinstruction addresses.

The register/counter is the source when a load instruction is used and the register load (RLD) line is low. The counter is loaded from data in (DI) on a positive clock pulse. The second source for the multiplexer is the direct inputs. This source is used for branching. The GP502 contains a 12-bit microprogram counter and incrementer. When the carry-in to the incrementer is high, the microprogram register is loaded on the next clock cycle with the current output word plus one, thereby executing sequential microinstructions. When the carry-in is low, the incrementer passes the output word unmodified so that the μprogram counter is reloaded with the same word on the next clock cycle. The same microinstruction is thus executed any number of times. The fourth source at the multiplexer is a 5-word x 12-bit stack. This stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer that always points to the last file word written.

Sixteen instructions are implemented in the GP502 by a 4-bit input field I. They control not only the source to the multiplexer but also three enable signals: $\overline{\text{PL}}$, $\overline{\text{MAP}}$, and $\overline{\text{VECT}}$. For each instruction, only one of these three outputs is active. They normally control 3-state enables as the primary source for microprogram jumps. $\overline{\text{PL}}$ normally enables the next address field of a pipeline register. $\overline{\text{MAP}}$ enables a PROM that maps the macroinstruction to a microinstruction starting address. In addition, $\overline{\text{VECT}}$ enables a third source, usually the vector output of an interrupt controller. External parts must be added to the sequencer to obtain these features.

Overall system design

A 16-bit microcomputer configuration is shown in Fig 4. The processing section contains two concatenated GP001 8-bit slices. The control section consists of a microprogram memory and the GP502 sequencer with additional logic in the form of a mapper ROM and condition code multiplexer. Microprogram memory is 2048 words deep with a nonencoded horizontal microinstruction of 64 bits. The micromemory is implemented as a writable control store and uses 74HC574 octal registers for pipeline. The pipeline, on the output of the micromemory, is optional but permits overlapping of fetch and execute cycles, thus increasing throughput. The 2-K x 8 6116 CMOS RAM chips require an 11-bit address input from the sequencer. An 11-bit field in the microword format is dedicated as a next address field and enabled from the sequencer's PL output. Under 3-state control, either the next address field or the mapper ROMs output provides data input to the sequencer. The main memory is also implemented with 2-K x 8 memory chips for a 16-bit data format. Adding MAR, IR, data in/out registers, clock and timing logic, and using a scratchpad register as a program counter makes the computer complete and operational.

A typical mode of operation involves several steps. Micromemory initiates a fetch of a macroinstruction

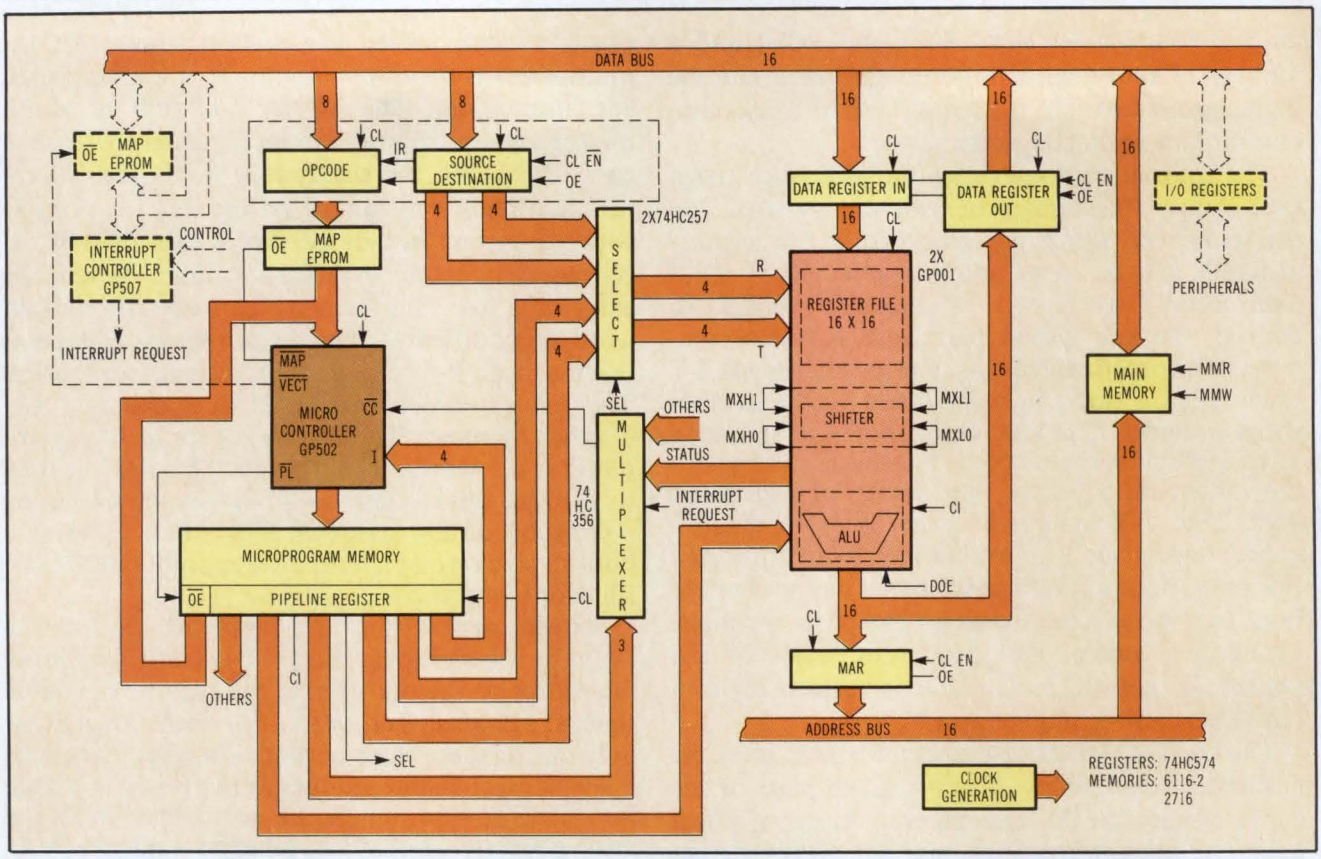


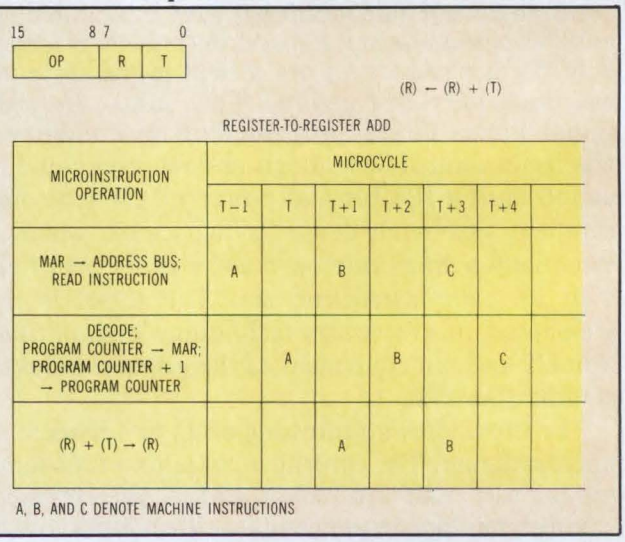
Fig 4 The processing section of this 16-bit microcomputer is comprised of two concatenated GP001 8-bit slices. The control section consists of a microprogram memory and the sequencer GP502 with pipeline register and support logic. With addition of MAR, IR, DA I/O registers, and main memory, the computer becomes operational.

from main memory; ie, the pipeline register instructs the CPU to output the program counter's content to the MAR, and enables MAR to the address bus. The opcode is next decoded by the controller, which outputs an address for the entry point of a microroutine that executes the fetched macroinstruction. The opcode is translated by the mapper ROM to the proper entry point address. The content of the addressed micromemory location loads the pipeline register. The bits in the micromemory direct the CPU to execute the desired instruction and provide necessary timing pulses to memory, registers, or other system components. An instruction might read, "add the operands from two scratchpad registers and load the result back into one of them." This is done in one microcycle. However, some macroinstructions may require more than one cycle, depending upon the nature of the instruction and the architecture's sophistication.

The architecture shown provides two ways of addressing the register file in the CPU. The operand part of the instruction may contain the R and T address, or the addresses may come directly from the microcode. A bit in the microword selects one of the two sources.

Most of the 16 control instructions for the sequencer are conditional, depending on the input at pin $\overline{CC}$. Status signals from the CPU such as carry-out, overflow, all-zero-detect, and other system flags are input to a multiplexer. The selected output of the multiplexer is tested by the sequencer at the pin $\overline{CC}$ location.

This simple computer's operation is further illustrated by looking at two instruction formats for the ADD operation. A register-to-register instruction format, for instance, can consist of an 8-bit opcode and two 4-bit source operand specifiers (Fig 5). Assume the operands are found in two internal



MICROINSTRUCTION OPERATION	MICROCYCLE						
	T−1	T	T+1	T+2	T+3	T+4	
MAR → ADDRESS BUS; READ INSTRUCTION	A		B		C		
DECODE; PROGRAM COUNTER → MAR; PROGRAM COUNTER + 1 → PROGRAM COUNTER		A		B		C	
(R) + (T) → (R)			A		B		

A, B, AND C DENOTE MACHINE INSTRUCTIONS

Fig 5 The register-to-register ADD instruction features an 8-bit opcode and two 4-bit source operand specifiers. Note that a pipeline register in the system allows the fetch and execution parts of a macroinstruction to overlap, resulting in increased speed.

Does the 60-Hz monitor you're considering meet these design parameters?

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CIRCLE 107

scratchpad registers that have already been loaded. The macroinstruction ADD that is to be executed is defined as (R) + (T) ⟶ (R). As shown, a standalone instruction takes 3 microcycles. At startup one can assume that MAR already holds the program counter for instruction A. During the first microcycle, a bit in the microword enables the content of the MAR onto the address bus while another control bit enables a read of the macroinstruction from main memory. A third control bit has enabled the IR so that at the end of the clock cycle, the instruction is latched in the IR.

During the next microcycle, the opcode portion is decoded by the mapper ROM and sequencer, and the microcontroller outputs an address for the microword that executes the fetched macroinstruction. At the end of the second microstep, the content of the addressed micromemory location loads the pipeline register. A portion of the microword dictates execution of the desired ADD instruction in the third cycle. A 4-bit field R denotes source of operand number one and destination of result. The field T points to the source of operand number two. The contents of the registers are read with P1B and P2B in a slave mode with respect to the register file. The operands are added with carry, and the ALU's output is written back into the destination register, all in the same step. If a carry-out is generated, it is available on a separate pin.

Perhaps the biggest advantage of a microprogrammed architecture is ease of structuring the control sequence.

Note that in the third cycle, a control bit is assigned to enable the content of MAR to the address bus and read the next instruction B. In the decode cycle the CPU, otherwise idle, is used to increment the old program counter and load MAR in readiness for next instruction fetch. Therefore, the fetch and execution parts of a macroinstruction are overlapped, resulting in increased speed.

The pipeline technique to increase throughput can (at the cost of microprogramming complexity) be carried out at one or more additional levels. Another example would be a register IMMEDIATE ADD instruction, (R) + DATA ⟶ (R). The instruction format would have a 16-bit operand as immediate data to be added to the content of the register addressed by R. The result is returned to the same scratchpad register.

The microcode sequence is similar to the register-to-register format but has one extra microcycle since another fetch is done to get the immediate data. The word is temporarily stored in the data in register. The last step is the execution phase. Port buffer P1B is slave to register (R) while P2B follows data in, which is enabled from the data in register (DARI). As previously, the execution phase overlaps the first fetch cycle and the output of the ALU is written back into register (R). The computer, as discussed, can of course be modified or expanded from this basic kernel to greater sophistication and higher speed. An interrupt controller GP507 can be added. The interrupt output line simply connects to one of the condition code multiplexer's inputs and a map PROM is enabled from the $\overline{\text{VECT}}$ output of the sequencer. A hardware multiplier, built from GP503 8 x 8 bit slices, can be interfaced to the data bus to increase throughput during multiplication instructions. Similarly, interfacing peripherals to the data bus, for both serial and parallel I/O devices, follows standard practice.

Advantages, limitations, and applications

Substituting simple memory structures for complex hardwired control circuits yields two main advantages. It makes it easier to understand and build the control system, and system modification is easier. One can correct a mistake in a microprogrammed control system simply by changing the content of the memory.

Perhaps the biggest advantage of a microprogrammed architecture is the ease of structuring the control sequence. A bit or a group of bits is allocated in the miocroprogram memory to control a certain function (ie, ALU function, ALU source-register selection, next address calculation selection, status selection, MAR enable). For each microstep, one can write the appropriate state (low to high) of these bits into the memory field. Such a structured implementation makes testing, debugging, and documentation easier. Special macroinstructions can also be included to provide inline checking of software operation.

With the microprogrammed approach, very complex macroinstruction sets can be implemented as sequences of relatively primitive microinstructions. In addition, special microcode can provide substantial speed improvement. For certain aerospace applications, dynamically reconfigurable systems are desirable. Such a system can respond to a fault and reconfigure the system to bypass the faulty element until it is replaced.

The use of parallelism, using bit slices and pipeline registers, along with the added capability of defining processor word length, has tremendously increased effective processing speed and system flexibility. Note that the microprogramming technique is also effective in non-CPU applications. LSI memories today are fast and inexpensive, making it practical to use microprogramming techniques in a wide range of complex digital systems.

Another interesting feature of user microprogramming is the ability to emulate other machines. By altering the microroutines or substituting another microprogram memory, the functional complexity of the machine is changed. It executes a

completely different set of macroinstructions, has a different architecture, and can be tailored to specific applications.

From a designer viewpoint, the microprogrammable bit-slice approach offers the advantage that the same processor components may be used to define various products. Designing a new system simply means the development of a new microprogram, rather than repetition of a lengthy overall system design cycle. For some applications the bit-sliced microprogrammable approach provides the only practical means of achieving special features and high throughput rates.

Some notable application areas include signal processing, image processing, digital filtering, fast Fourier transform, online systems, data communications, process control, high speed controllers for disks, video and graphic displays, and emulation. Some of the instruction sets the EPIC chip set has emulated in designed equipment include the MIL-STD-1750A, AN/UYK-20, and PDP-11.

The advantages, however, are not free. Working with bit-slice microprocessors is more difficult and time consuming than working with single-chip processors. There are at least two levels of control and two levels of programming to consider: the macro level, and the micro level. The designer is concerned both with definition of the macroinstruction set and its implementation as a microprogram set.

Design and software supports, while they exist, are less extensive than those for single-chip processors. Commercial design aids available offer emulation of micromemory with trace capability, and include a meta-assembler through which a user can define mnemonics. Also, multichip designs are less reliable than single-chip processors because of the increased number of interconnections. Despite these limitations, microprogrammable bit-slice architectures are finding increased use for high speed sophisticated applications.

Acknowledgment

The parts in the EPIC CMOS/SOS family were developed under sponsorship of the USAF Avionics Laboratory. The parts were designed by Tracor, Inc and RCA Advanced Technology Laboratories.

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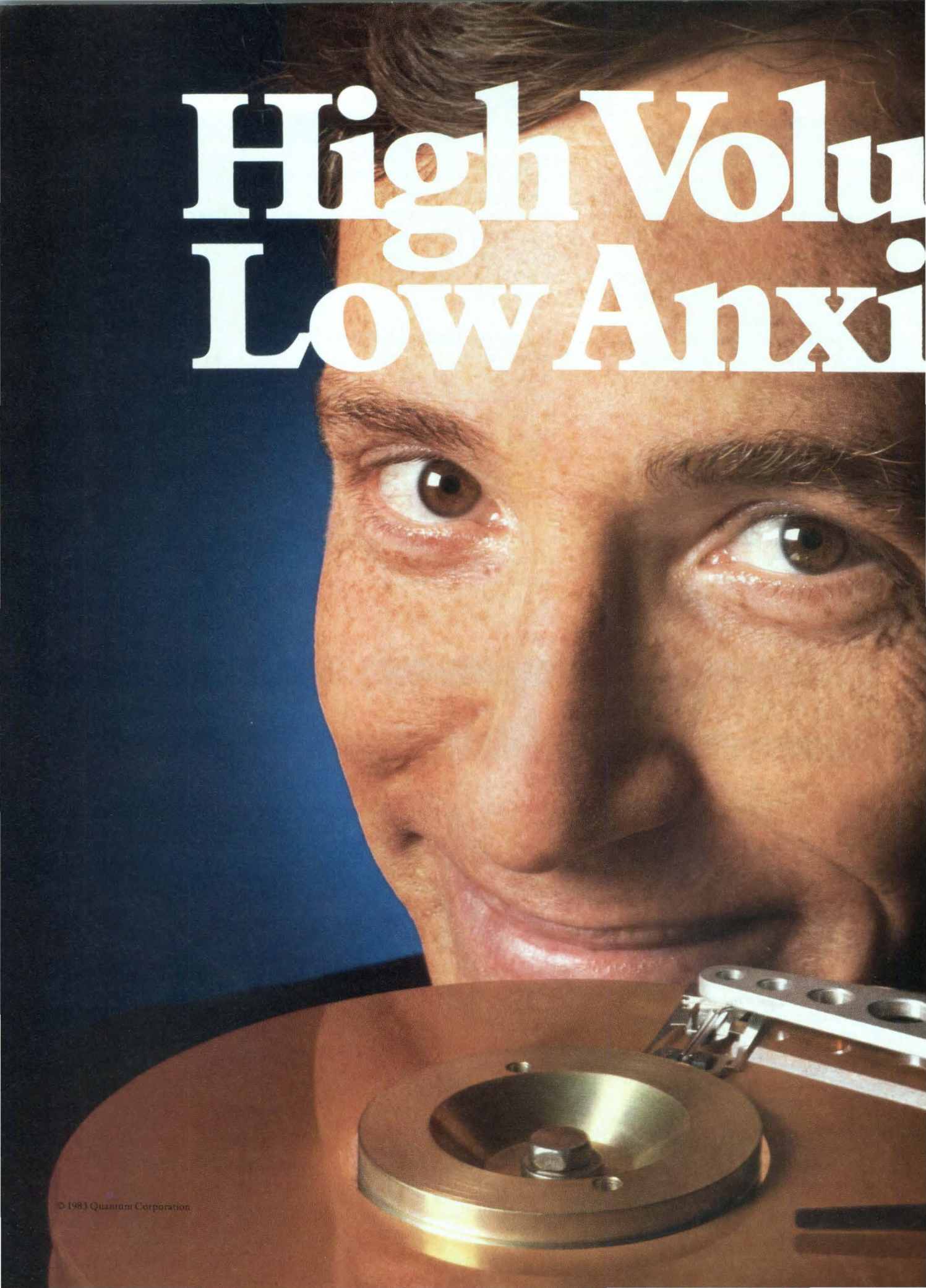
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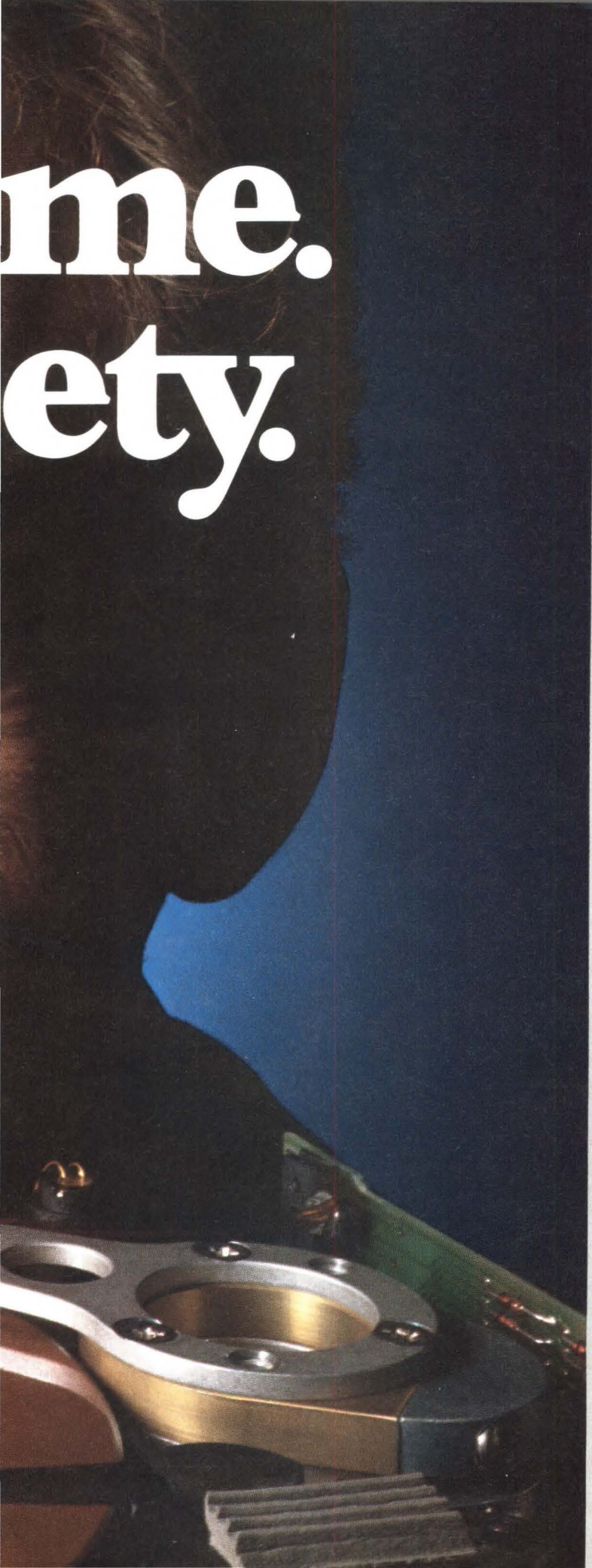

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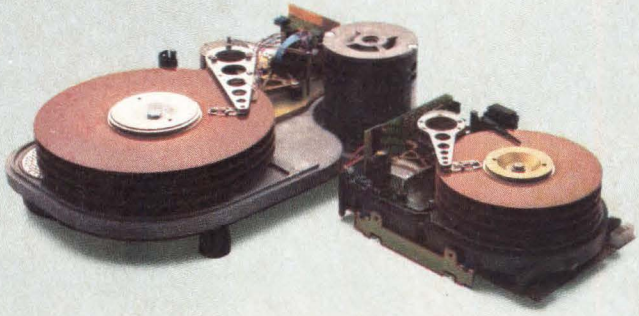

CIRCLE 109


Trace_List
State 7, 60 channel, 68000 emulation bus
68000 Mnemonic
hex
symbols
SRC_ADDR:Mon 68K
MAGIC_SQU+00001C
MAGIC_SQU:E68000 - line
Pascal program to generate a magic square
matrix of numerical entries where the sum
column, or diagonal is constant. The sq
of entries on a side, specified by the
BEGIN { M_Square_Gen }
COL := SIZE/2;
MAGIC_SQU+00001E MOVE.W
STAT4:Mon 68K
MONITOR_CONTROL:
MAGIC_SQU+000020
MAGIC_SQU+000022 EXT.L
STATUS: Awaiting state command - use
_source on
display <LINE #> disassemb so
Trace_List
State 7, 60 channel, 1750A emulation bus
Label: line #
ADDRESS
1750A Mnemonic
Base:
hex
Map:
ADDR_MAP and symbols
+011 12* aHANOIa+1109 LISP R2,1
+012 NUMBER_DISKS:aHANOIa 0014
+013 12 aHANOIa+110A STB
HANOIa:MILO - line
" Jovial routine for solution of the
L3: IF NN<>1;
+014 13* aHANOIa+110B LISP
+015 NUMBER_MOVES:aHANOIa
+016 13 aHANOIa+110C CB
+017 13 aHANOIa+110D BEZ
+018 NUMBER_DISKS:aHANOIa
HANOIa:MILO
Begin NO(JP)=NN;
+019 14* aHANOIa+110E
STATUS: Awaiting state command - userid
_source on
display <LINE #> disassemb source
Trace List
State 7, 60 channel, 68000 emula
68000 Mnemonic
hex
symbols
MAGIC_SQU+00003E MOVE.W 0008[A6],D1
MAGIC_SQU+000040 0008 user program read
MAGIC_SQU+000042 MULS.W D1,D1
MAGIC_SQU+000044 MOVE.W 2006[A5],D2
MAGIC_SQU+000046 2006 user program read
MAGIC_SQU:E68000 - line 40 thru 42
/* this procedure, written in -C- fills out the square matrix
/* initialize the row pointer */
for (COUNT = 1; COUNT <=SIZE*SIZE; COUNT++) {
M_SQUARE_3:MAGI CMP.W D1,D2
MAGIC_SQU+00004A BGT.W MAGIC_SQU+00009A
MAGIC_SQU+00004C 004E user program read
MAGIC_SQU+00004E MOVE.W 2002[A5],D3
MAGIC_SQU+000050 2002 user program read
STATUS: Awaiting state command - userid CONTROL
display <LINE #> disassemb source
show
execute

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CIRCLE 111

Cache RAM accelerates Winchester disk subsystems

DisCache delivers top speed and high performance to low end microcomputers. The 10- or 20-Mbyte subsystem includes a 5¼-in. hard disk, a RAM cache (up to 256 Kbytes), a specialized microcomputer, and an incremental backup system.

The subsystem improves microcomputer performance levels by making some programs and/or data on the Winchester immediately available from RAM rather than disk. Optimized for typical micro database programs, the system returns around 75 percent of all sector access requests from RAM instead of disk. Maximum access time for a sector from RAM is only 100 μs, compared with a typical maximum of 200 ms from a Winchester.

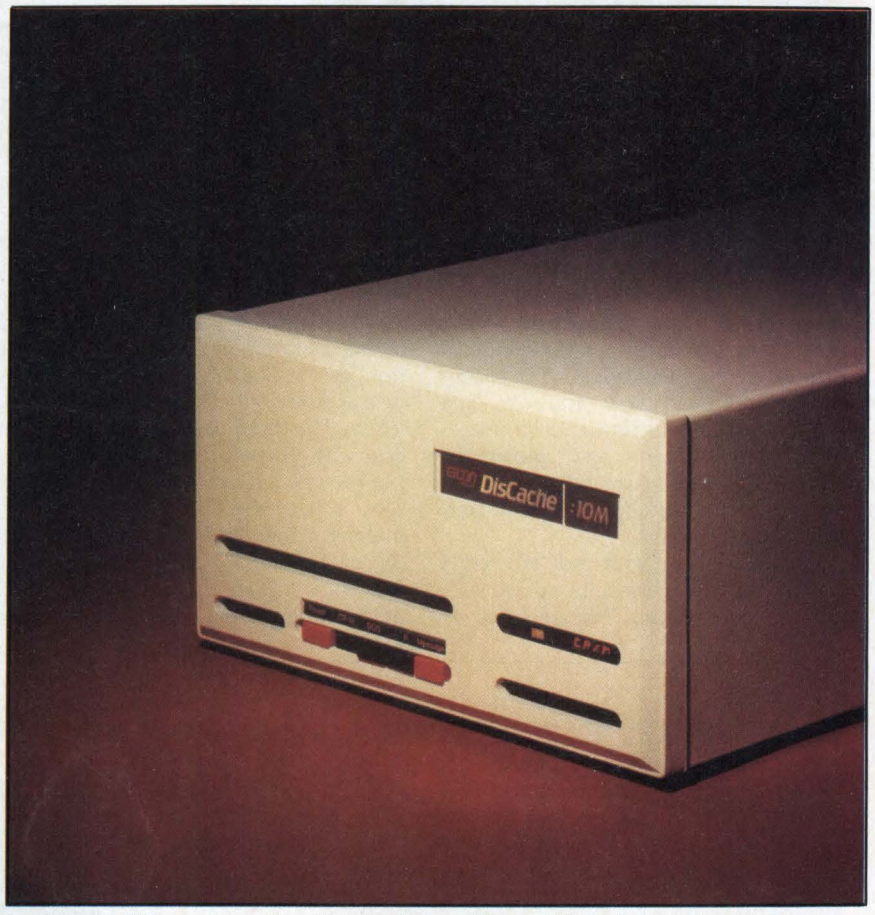
An independent processor makes these fast access times possible. DisCache constantly monitors the sectors requested from the disk, and automatically keeps frequently used sectors in the RAM "cache" for immediate access. The caching algorithm continually optimizes the cache contents.

Part of the cache is reserved for anticipatory buffering. The requested sector as well as 31 neighboring sectors load into the cache. Statistically, these additional sectors will probably be requested next by the host computer.

Speed is also improved when writing a sector to disk. The processor immediately accepts a sector and stores it in RAM. This allows a user's program to continue running without a disk access delay. After pausing for additional sectors from the same track, the processor transfers the new sector to disk.

For security backup, the processor keeps track of which sectors on the disk are being updated. The option remains with the user to write only updated sectors to a security backup on the floppy disk system, or to make complete copies. The updated copy typically takes 30 s, eliminating the need for backup devices.

The complete option minimizes the required number of diskettes and relieves the need to supervise the process. Software manages the process to ensure that all data is backed up. It also validates each diskette and checks for the correct sequence in the Winchester restoration process. Another feature of the daily backup facility restores the disk to its earlier state, thereby undoing corruptions and erroneous deletions.



A print spooling facility accepts virtually unlimited printer output at a high data transfer rate. This permits the microcomputer to continue running as though the print operation is complete. Data transfers from the spool are then considered a background task by the processor. Multiple print jobs queue off the system. An optional second printer port allows separate spools for two printers, which can run simultaneously.

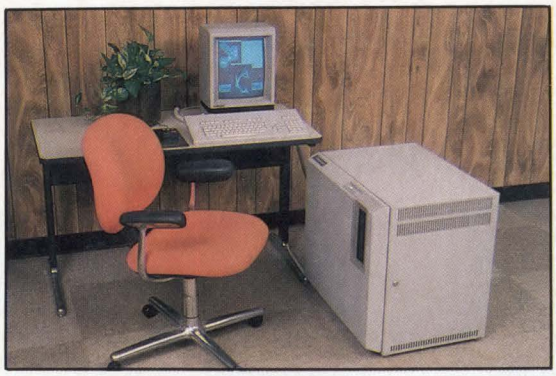
Cache-Net acts as an enhancement to the system. It permits up to 21 personal computers (NEC, IBM PC, Apple II) and operating systems to share access in any combination. At a basic line speed of 1 Mbyte/s (similar to Ethernet), Cache-Net allows data transfers at the full DMA speeds of the computers themselves. Average sustained rate is 250 kbytes/s.

Since DisCache's internal processor handles the polling of users, it eliminates the need for an additional multiplexer box, or master or supervisory computer. Each additional machine daisy chains to the previous one via a cable. The expandable chain accepts different types of computers at any point.

For long cable runs, which normally do not support high data rates due to cable capacitance and cross talk, the system offers electronic repeaters. These repeaters (fitted in line every 30 ft) draw their power from the data cable. For even longer distances, a serial line converter can be substituted. This enables a run of up to 1000 ft of twisted-pair cable to replace the usual flat cable, without affecting the data rate.

Price for the DisCache subsystem is $3000. **Eicon Research, Inc,** 2157 Park Blvd, PO Box 60456, Palo Alto, CA 94306. **Circle 260**

Bus-based system promotes flexibility and performance



The Nu Machine capitalizes on bus technology and processor independence to create a communication-centered architecture. Supplied with a 10-MHz 68010 processor, the workstation-oriented computer features a 4-Kbyte cache memory and a hardware implemented memory management system. The NuBus supports 32-bit data transfer and addressing as well as future 32-bit microprocessors. This bus also allows the design of systems using other standard microprocessor families or special purpose instruction sets.

The NuBus is a wide and efficiently controlled data freeway. In addition, it provides a maximum transfer rate of 37.5 Mbytes/s. Using the bus technology, the system implementer can have each processor running a different operating system or have multiple processors running one operating system. Bus structure is based on the master/slave concept. For each transaction, a device takes control and addresses another unit. A simple handshake protocol between the master and slave permits modules of different speeds to use the NuBus interface.

Based on the 68010, the CPU generates 24-bit virtual addresses allowing access to 16 Mbytes per virtual address space. A state machine translates the virtual addresses to physical addresses. In addition, a 45-ns cache stores both data and instructions, which are treated equivalently. The cache has a hit rate of 85 percent with no wait states on hits.

The system diagnostic unit contains an 8088, RAM, ROM, and serial ports—making it independent from the rest of the computer. By reading ID ROMs on individual cards, the unit performs an auto-configuration. This allows the system to use a new or replacement card immediately. It will then bootstrap to the system software. An independent function of this board converts between the NuBus and the Multibus. This conversion allows masters on either bus to address slaves on the other bus. The Multibus subsystem operates independently of the NuBus, except during cycles that use them both.

Two Winchester disk storage systems offer either 84 or 474 Mbytes with access times of 20 and 18 ms, respectively. For the disk backup, half-inch streamer and quarter-inch cartridge units are available.

The operating system derives from Unix but adds enhancements to support graphics and other hardware features. High resolution raster graphics are available through an 800 x 1024, 60-Hz noninterlaced display. A windowing system provides capabilities for multiple virtual terminals on the display. Available programming languages are Fortran and C.

Depending on quantity and configuration, prices for the Nu Machine range from $33,680 to $50,370. **Texas Instruments Inc, Data Systems Group,** PO Box 402430, Dallas, TX 75240.

Circle 261

Standard APL development station front-ends array processor

By using an IBM PC as its workstation, Analogic's APL Machine brings the low cost, flexibility, and responsiveness of a desktop microcomputer to high speed array processing. Through this interface, the system begins to overcome previous drawbacks to developing high speed array processing applications, such as inflexibility and difficult programming. Previous APL/array processing development was confined mostly to large, computation-intensive installations because conventional linear computer architecture is not hardware efficient for processing arrays. Conversely, array processing hardware is generally infeasible for executing high level programming languages.

As interface to the APL Machine, the PC becomes an APL programmer's workstation; alternately, it functions in native mode. Whereas array processors typically execute libraries of assembly language or Fortran subroutines, the APL Machine's array processor directly executes ISO-validated APL programs written on its own or external hardware. Moreover, Unix-like shells incorporating non-APL code accommodate applications using compiled or assembled code.

The Unix-derived operating system creates a multi-user, multitasking environment with virtual memory. Three processing units make up the system architecture: a 12.5-MHz 16/32-bit control processor, pipelined ALU, and address generator. APL primitives and operators reside in pipeline microcode. This architecture supports several levels of overlapped and parallel processing; a memory manager coordinates nested applications and shared code among concurrent processes.

Though the array processor has been benchmarked in specific applications between 2 and 10 MFLOPS, the company claims that hardware design efficiencies sometimes push those figures into the 15-MFLOPS ballpark. The workstation's InSight operating environment lets each user display up to 10 concurrently running tasks on overlapping and sliding windows; 10 function keys on the workstation keyboard correspond to active windows. Keycaps are labeled with both APL and ASCII characters.

A typical system configuration includes the IBM PC, 4-Mbyte AP500 array processor, 124-Mbyte hard disk, dual-mode tape drive, and I/O processor supporting 8 to 16 terminals. System prices range from $80,000 to $100,000. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.

Circle 262

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CIRCLE 112

Supermini optimizes physical, virtual, and cache memory

With up to 64 Mbytes of multiported physical memory and 1 Gbyte of virtual memory, the 32-bit Classic 32/85 serves time-critical applications. These include scientific measurement and control, communication, and factory automation. The system consists of one or more CPUs and I/O controllers connected to the input ports of the memory subsystems.

Each system handles from one to eight memory subsystems. Each subsystem, in turn, is available with capacities from 2 to 8 Mbytes and consists of a memory controller board, one to four memory array boards, and one to three memory interface boards. The controller board contains port arbitration logic, memory module interface and control logic, and subsystem maintenance logic. It provides required address decodes and timing signals for memory module access, including dynamic memory refresh control.

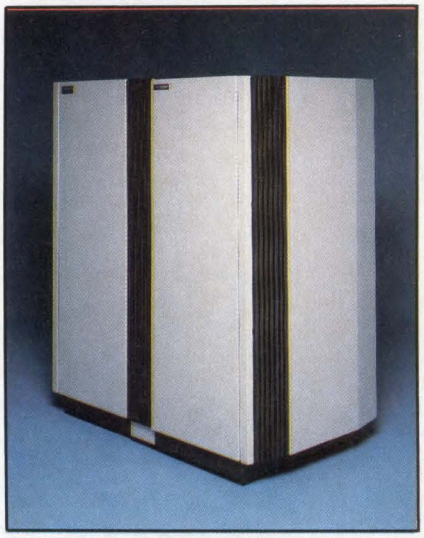
The array boards each consist of 2 Mbytes of memory implemented with 64-Kbyte dynamic RAMs. Error correction code logic corrects all single-bit errors and detects all double-bit and some multiple-bit errors. The maintenance console logs all reported errors.

Six concurrent memory ports provide CPU and I/O access. The master CPU uses one port while other CPUs and I/O controllers use the other ports. Each port performs read and lock cycles for implementing semaphores. Any memory subsystem can be independently shut down via the maintenance console.

The CPU is made up of a memory management unit (MMU) with mapping processor and cache and the instruction set processor. The MMU provides the CPU with logical-to-physical address translation mapping and cache memory (to improve the memory access rate), as well as the main memory interface. Memory addressing converts a 32-bit virtual address, defined by the instruction, into a 29-bit physical address. Up to 64 Mbytes of physical memory can be addressed. After the virtual address is generated, it is mapped into the physical address in the MMU.

Cache memory consists of a four-way, set associative memory with 16 Kbytes/set. A least recently used algorithm maintains a record of the LRU set for each group of four 32-bit words in cache.

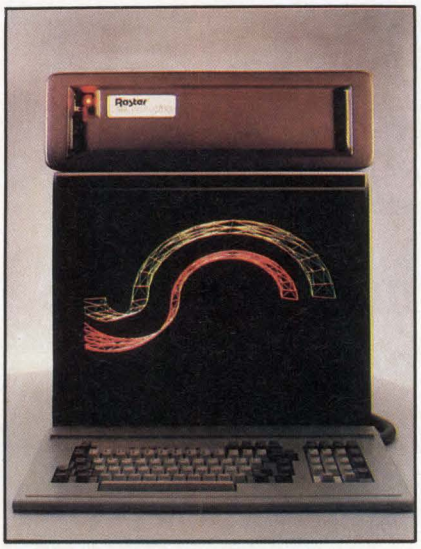
The instruction set processor is a complete ALU containing a microprogrammable processor with hardware multiply and floating point arithmetic. There are two instruction sets. The first is compatible with the Classic II series and adds firmware implementation of a specified set of transcendental functions. Initially, the firmware will map virtual space to actual space and start bootstrap execution in nonvirtual mode.



Basic configuration is $148,500 in single units. **Modular Computer Systems, Inc,** PO Box 6099, 1650 W McNab Rd, Fort Lauderdale, FL 33310.
Circle 263

Sophisticated graphics controller draws fast response time

Model One/80 outfits general purpose 32-bit computer systems with the electronics to develop sophisticated graphics applications. At an attractive cost/performance ratio, the controller's prime applications span from computer aided design/engineering, architectural drafting, and computer animation to land resource analysis. Prices for a basic configuration, including monitor and keyboard, start under $20,000.



To the host computer, the controller looks like a high speed peripheral. It supports 1280 x 1024 resolution with 8-bit planes of image memory, furnishing 256 colors from a palette of 16.7 million. Moreover, 60-Hz noninterlaced refresh and pixel updates as fast as 8.7 ns/pixel combine with other features to provide interactive three-dimensional modeling and simulation.

The system draws up to 70,000 one-centimeter random vectors/s. Onscreen, a local programmable window clips vectors at the full draw rate. In double-buffered mode, the bipolar processor has total access to image memory, thereby allowing a vector draw rate that approaches 115 million pixels/s.

Bipolar processor and proprietary VLSI hardware accelerators directly execute most common graphics functions—such as move, draw, fill/unfill area, and transfer pixel image—with minimal host intervention. Vector-defined text can be generated in vertical and horizontal formats. Both formats rotate in one-degree increments and scale from 8 to 256 pixels independently in X and Y.

An 8-MHz, 16-bit microprocessor controls serial I/O and local programming facilities. This tightly coupled unit comes with 96-Kbyte PROM and 32-Kbyte RAM for instruction set, local macro programming, and interactive debugging. A resident command interpreter tests and executes graphics sequences without a host.

Integrated DMA interface conforms to industry-standard specifications for fast image and command transfers to DEC's PDP-11 and VAX families, as well as systems from Data General, Perkin-Elmer, Prime, IBM, and Gould/SEL. Four serial ports at up to 38.4 kbaud are standard. With an I/O subsystem that accepts data at up to 6 Mbytes/s, the Model One/80 can be closely coupled to a host for I/O-intensive applications.

System commands include CORE and GKS functions, as well as standard primitives; application software is compatible across the entire Model One family. All controller electronics come in a 5.25- x 17- x 21-in. (13.34- x 43- x 53-cm) rackmount box that weighs 50 lb (23 kg). **Raster Technologies, Inc**, 9 Executive Park Dr, North Billerica, MA 01862.
Circle 264

Industrial computer uses customized slide-in processor boards

Based on multiple processors instead of a single CPU, the IMP-68000 can be tailored to execute diverse applications in parallel. Each processor runs independently and consists of a standard section and an I/O section.

The 68000-based system provides 16 Mbytes of direct addressing. Subdivisions include local, remote, and mass memory. Local memory comprises the static RAM and/or erasable PROM (up to 128 Kbytes) that reside in the processor's eight memory sockets. Remote memory has the same capacity as local memory, but resides on the other processor boards in the system chassis. Mass memory consists of dynamic RAM on a dedicated memory board. Each processor board can directly access any portion of system memory unless it is prevented by interboard memory protect logic.

Memory is configured so that each processor board contains eight 28-pin JEDEC sockets for 128 Kbytes of memory. Organized into four socket pairs, each pair requires two compatible memory chips. The other four pairs can hold different type, size, and speed memory chips.

An additional 4 Kbytes of SRAM are part of the nucleus board. This SRAM overlays a portion of the EPROM in the first pair of memory sockets and overlay select logic determines which type of memory is accessed. Data cycle instructions access the SRAM, while program cycle instructions access the EPROM.

Both digital and analog I/O sections are available on a board. The digital board contains 32 digital modules. Each is bidirectional—it can be used for either inputs or outputs. Other features include 5- to 80-Vdc range, 4-A continuous output drive rating, and response times of 200 kHz for the first group of 8 points, 20 kHz for the others.

The digital board also contains a dedicated timing controller for autocounting and/or generation of pulse I/O. It is programmable and provides five independent 16-bit counting registers.

The analog board provides 16-bit resolution, with interfacing for 16 differential inputs and four analog outputs. The D-A converters can drive up to 1 A each, while the A-D converters operate at 10 kHz. An onboard 10-Vdc precision reference source provides automatic zero and span of the A-D converter. **Indocomp Inc**, 5409 Perry Dr, Drayton Plains, MI 48020.

Circle 265

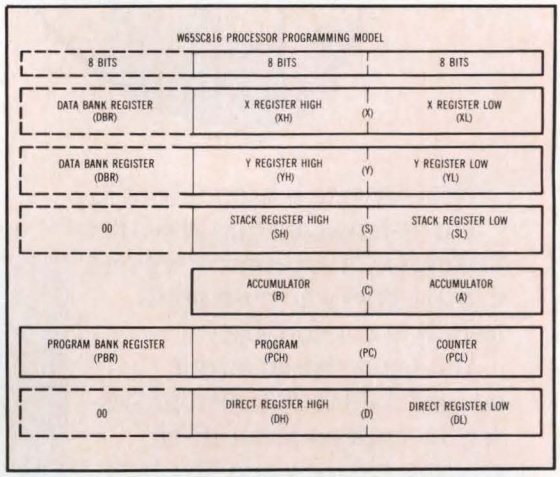
Family of 16-bit CMOS processors extends 6500 capabilities

Pin compatible with NMOS and CMOS versions of the 6500, W65SC8XX and W65SC9XX chips have a 24-bit addressing range. Despite enhanced features, the family retains software compatibility with existing 6500 code.

Made using the proprietary OXI-CMOS technique, the processors will appear in 1-, 2-, 3-, and 4-MHz versions. The W65SC802 is pin compatible with 8-bit 6502 devices, while the W65SC816 extends the address range to 16 Mbytes. A software switch puts the processor either in 8-bit emulation mode to run existing software or in 16-bit mode to use the 16-bit internal registers and address the full 24 Mbytes of memory.

Internally, accumulator, ALU, X and Y index registers, and stack pointer have been extended to 16 bits. The new processors also contain a 16-bit direct page register to augment the direct page addressing mode. Separate program bank and data bank registers extend the X and Y and program counter registers to address 24 bits of address space. Besides the thirteen 6502 addressing modes, the family provides 11 new modes, including stack relative addressing, block move addressing, and absolute indexed direct addressing.

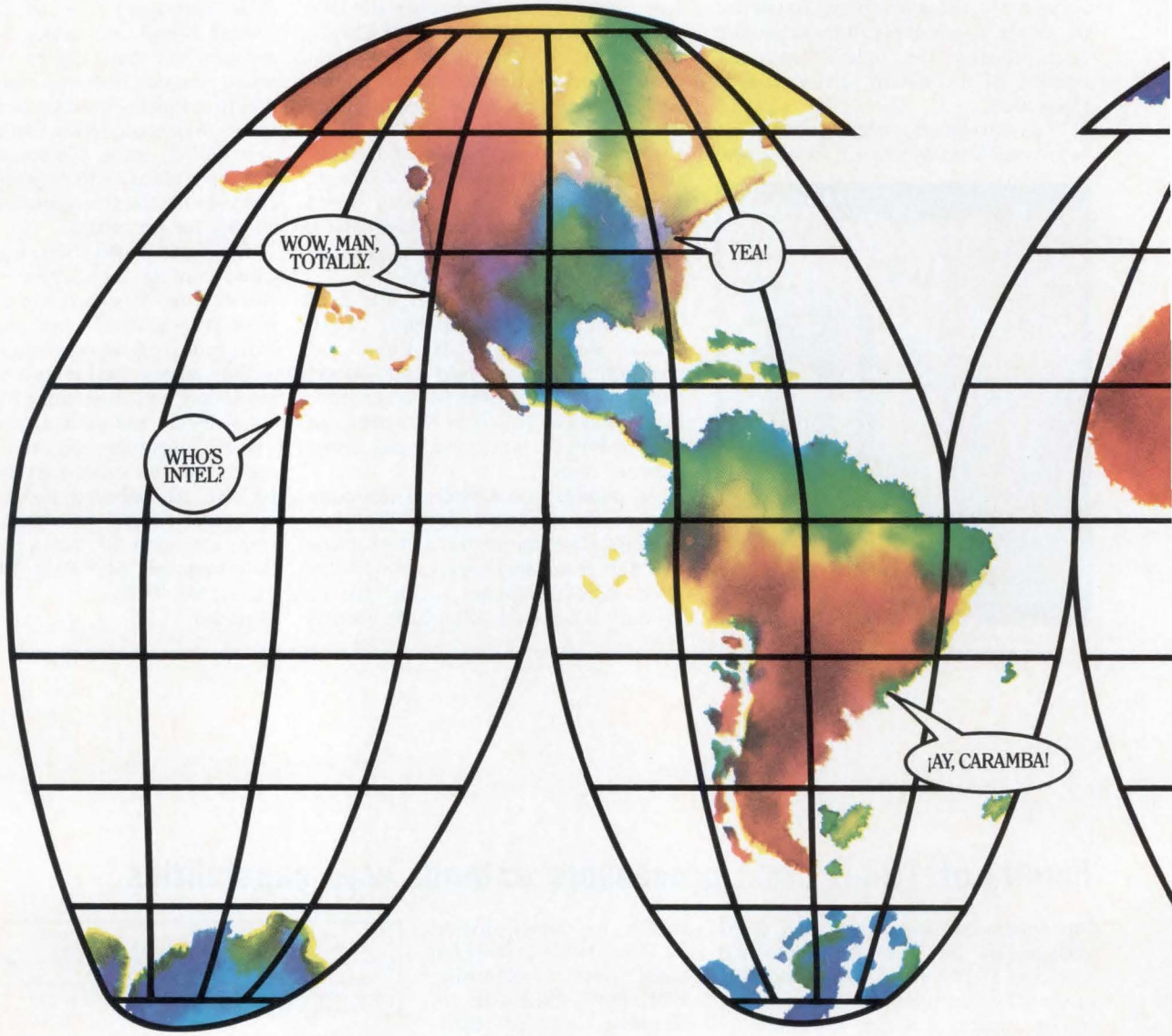
On the W65SC816, four additional signals create a range of options for system configuration. The abort input signal can interrupt a currently executing instruction without affecting the internal registers. Two outputs enable the designer to create dual-cache memory by telling the system whether a valid data segment or a valid program segment has been addressed. Vector pull output can be monitored to tell whether to modify a vector. The latter signal goes low during the two cycles when a vector address is being pulled, and also goes low for all interrupt vector pulls.



While the W65SC8XX and 9XX family chips are implemented in 3-μm silicon gate CMOS, a 1.5-μm version will be developed in the near future. Presently, the devices perform one execution cycle per memory fetch; versions running up to 10 MHz are expected by the end of 1984.

Samples of the 1-MHz version are available at a price of $95 each. **Western Design Center, Inc**, 2166 E Brown Rd, Mesa, AZ 85203. **Circle 266**

WHEN WE INTRODUCED OUR PEOPLE HAD



Not everyone is happy about it.

For instance, our new 286/310 multi-user, multi-tasking OEM supermicro is going to make guys who push minis awfully uncomfortable.

You see, it's based on our advanced iAPX 286 microprocessor, the most powerful 16-bit processor in the world. To which we've added our 80287 math co-processor as a, shall we say, turbocharger?

That little bit of technological tinkering makes it a very fast supermicro. Faster than a VAX* 11/750. In fact, according to independent benchmarks, the 286/310 is the world's fastest Xenix* supermicro.

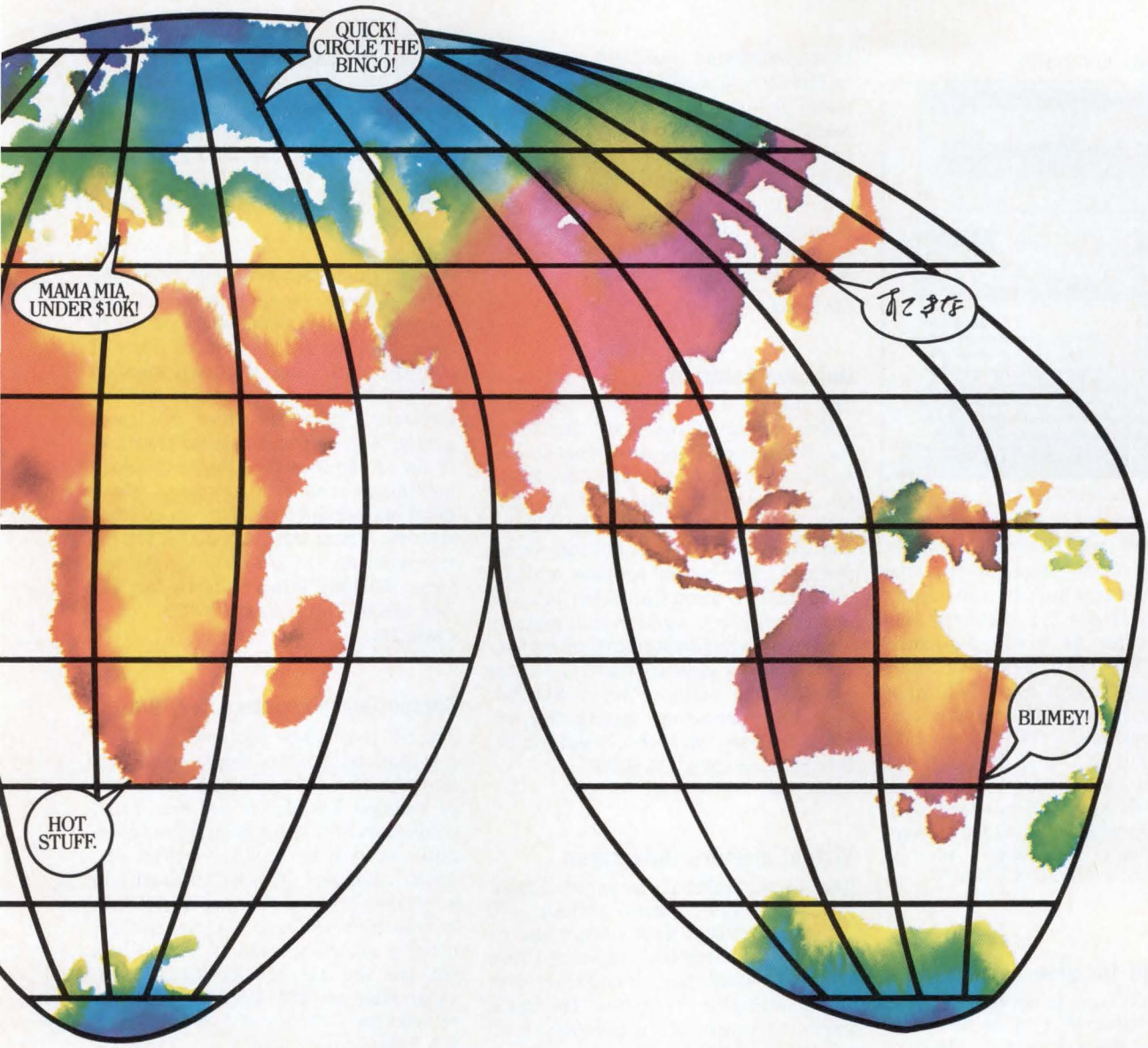
286/310 Supermicro System

It doesn't do too badly in iRMX™ real time OEM applications, either (3x the performance of any comparably-priced system.)

The kicker is the 310 costs less than $10,000. And that's list, quantity one. OEM quantities are so much less expensive it's embarrassing.

But before you start thinking about all the money you can make with the 310, let us tell you

NEW SUPERMICRO SYSTEM, LITTLE TO SAY.



a little about how easy it'll be.

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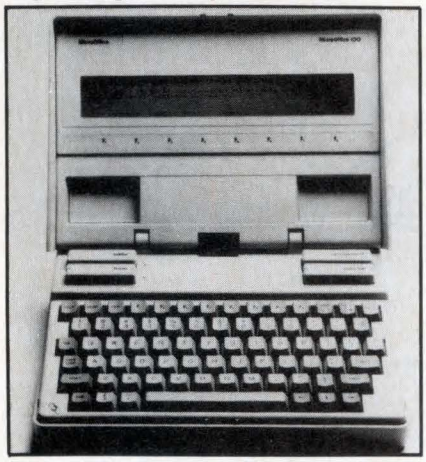
CIRCLE 114

Lightweight computer



The 5-lb MicroOffice 100 uses removable, reusable cartridges for high speed storage with no moving parts. Features include an 8-line x 80-character tilt-adjustable LCD built into the cover. The display shows 255 characters and has full-graphic 64 x 480 dot-matrix capability. The 73-key keyboard comes with 18 function keys (eight for single-key menu selection). The computer consists of a single-board CPU built around a Z80-compatible, 2.5-MHz data bus, and a 16-bit address bus micro with a main memory of 64 Kbytes of RAM and ROM. In 1000s, price is under $1500. **Micro-Office Systems Technology, Inc,** 35 Kings Hwy E, Fairfield, CT 06430.

Circle 267

Supermicro for nine users

The 986 is fully compatible with the Altos 586 and accommodates up to nine users via ten RS-232 ports. It offers 1 Mbyte of main memory and configures into a network using Worknet networking software. The system includes an integral port for twisted-pair cabling and will accept the Ethernet chip set. Files can be accessed from anywhere on the network without initial local copying. The system runs its 8086 at 10 MHz and uses two Z80 processors to handle DMA. Price is $12,990. **Altos Computer Systems,** 2641 Orchard Park Way, San Jose, CA 95134. **Circle 268**

Computer with DEC compatibility

At the heart of its configurations, the 3000 can use PDP-11/23 Plus, /24, /44, or VAX processors. It offers 160-Mbyte fixed Winchesters and 80-Mbyte removable backup. The system has total emulation of RSTS/E, RSXIIM, Unix, and TSX, as well as 256-Kbyte to 8-Mbyte memory. Additional features include peripheral bus mapping module, 18- and 22-bit LSI-11 backplane handling old and new controllers, 4- to 16-port serial interface for terminals, large 6 x 9 backplane, and communication options to MUX and modems. **Unitronix Corp,** 197 Meister Ave, Somerville, NJ 08876.

Circle 269

Unix workstation

The Micro/32 is a 32-bit computer system featuring the 68000 micro and Regulus, an operating system that accommodates all other Unix software. Regulus features user source compatibility with Unix versions 6, 7, and System III, and completely supports all Unix kernel features. The system contains a single quad size CPU board with 32-bit data and address registers, together with memory managers having 64 segments of associatively mapped memory and 512 Kbytes of RAM with parity. Price is $11,950, including operating system license. **MDB Systems, Inc,** 1995 N Batavia St, Box 5508, Orange, CA 92267.

Circle 270

Virtual memory Unix micro

The 16-bit Multibus-compatible Sampson multi-user system includes 70 Mbytes of integral disk storage and 67 Mbytes of formatted tape cartridge capacity. Dual-bus architecture uses 16-bit intelligent I/O boards. The Sunix operating system provides access to all system resources and many software packages. A system for 10 ports is configured with a Multibus, 10 card-slot chassis, and 512 Kbytes of onboard memory. Price is $24,900. **SGS Semiconductor Corp,** 1000 E Bell Rd, Phoenix, AZ 85022.

Circle 271

Dual 8/16-bit CPU computer

The M68 provides 1-Mbyte standard memory for the 256-Kbyte dynamic RAM. With expansion slots, three memory boards of 1 Mbyte each give a total of 4 Mbytes of memory. Sixteen-bit performance is based on the 10-MHz MC68000, and 8-bit on the Z80A. The computer uses CP/M-80 software and C, Fortran, Cobol, and APL on CP/M-68K. Character display is 80 x 25, 512 characters; graphics display is 640 x 400 dots, 16 colors. With large internal memory, the machine can take full advantage of the 68000's 32-bit architecture. **SORD Computer of America, Inc,** 200 Park Ave, New York, NY 10166.

Circle 272

Array processors with IBM interface

The FPS-5500/5600 series attach to the IBM 370, 30XX, and 43XX computers via a high speed data-streaming interface. Flow of control, data, and status-information between machines is handled by this interface. Data transfers or status queries are controlled by host programs or the array processor using IBM's block multiplexer with data streaming. Maximum performance ranges from 30 to 48 MFLOPS. Prices start at $98,000 for the 5500 series and at $134,000 for the 5600 series. **Floating Point Systems, Inc,** PO Box 23489, Portland, OR 97223.

Circle 273

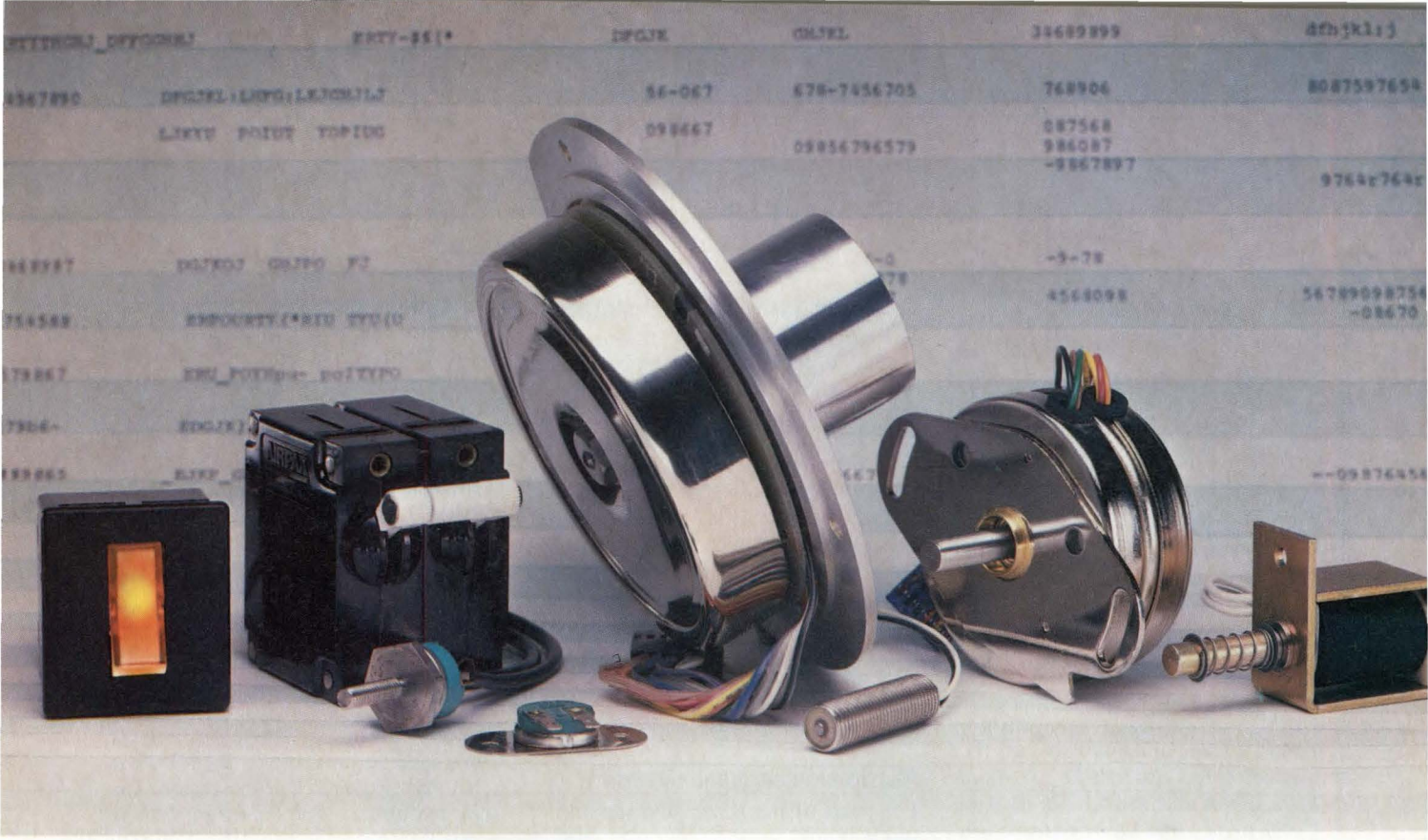
Compatible computers for IBMs

The TPC II is a 16-bit portable computer. It is available in a dual-floppy configuration with each drive providing 360 Kbytes of storage. The device has rear panel connectors for a color monitor and composite video. It can be linked with the personal computer network through an RS-422 network port that provides access to network features such as shared files, printers, and electronic mail. System uses the 8088 and has 128 Kbytes of RAM, expandable to 256 Kbytes. **Televideo Systems Inc,** 1170 Morse Ave, Sunnyvale, CA 94086. **Circle 274**

Distributed processing

This multi-user desktop package creates a standalone system or an intelligent node in an existing network. Elite consists of one distributed processing controller, a micro-based communication computer containing four I/O and four interface ports, and 1 Mbyte of 256-Kbit RAM. A second board expands RAM to 3 Mbytes and connects to a dual-ring LAN. Adding CRT, keyboard, printer, and disk drives allows standalone configuration. Cost is $7400. **Incomnet,** 2772 Johnson Dr, Ventura, CA 93003.

Circle 275



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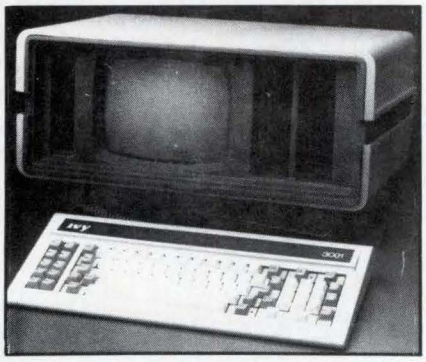
CIRCLE 115

Faster chip PC compatibles



The 3000 series uses the 80186 running at 6 MHz so all software can run up to four times faster than on the PC or PC XT. The 3001 version offers two half-height 5¼-in. diskette drives and 256 Kbytes of RAM. The 3002 offers one half-height 5¼-in. drive, one half-height 5¼-in. Winchester (10 Mbytes), and 256 Kbytes of RAM. The keyboard is fully compatible with the PC and XT. No cooling fan is required due to very low power consumption and convection cooling. A single-board, built-in 300/1200 baud smart modem is optional. Prices range from $2995 to $3995. **Ivy Microcomputer Corp,** 220 Ballardvale St, Wilmington, MA 01887. **Circle 276**

Multiple micro system

With a variable processor architecture, the Convertible changes easily from one multiple configuration to another via plug-in boards. It operates concurrently with up to three different micros using different operating systems. Equipped with both Z80H and TI 995 micros, it can be expanded to include 80186/286 and 68000. Prices start at under $6000, which includes 128 Kbytes of RAM (expandable to 1 Mbyte), diskette drive, video display, DIN standard keyboard, and a letter-quality printer. **Omnidata,** 5717 Corsa Ave, Westlake Village, CA 91362.

Circle 277

Computer with 10-MHz operation

The 68000-based SBE-250 features no wait state dual-ported RAM, a choice of three operating systems, and a six-slot Multibus card cage for expansion. The computer has 256 Kbytes of RAM; 320-Kbyte, 5¼ in. floppy; 10-Mbyte, 5¼ in. Winchester; parallel I/O; and two serial I/Os. Options include a 40-Mbyte Winchester, a Centronics parallel printer port, and an intelligent 10-channel serial I/O board. Operating systems are Unix-compatible Regulus, CP/M-68K, and PolyForth/32. Price is $4795. **SBE, Inc,** 4700 San Pablo Ave, Emeryville, CA 94608.

Circle 278

Multiprocessor/user system

The heart of the Dimension system is a single-board 80186 processor and a 13-slot IBM bus. Supporting up to 12 workstations, the system gives each user a dedicated processor attached to the bus. This CPU is an 8088-2, which is a faster version of the 8088. Operating system is compatible with PC-DOS 2.0 and has built-in electronic mail capability. Standard equipment includes one 360-Kbyte floppy drive, one 15- or 30-Mbyte fixed disk, and add-in spaces for other drives. Complete system with 15-Mbyte hard disk is $7000. **North Star Computers, Inc,** 14440 Catalina St, San Leandro, CA 94577.

Circle 279

Multi-user microcomputer

The 186 series implements a multi-user version of Concurrent CP/M-86, as well as Oasis-16 or MBOS/BB3. Based on the 8-MHz 80186, the computer comes with 256 Kbytes of memory that expand to 512 Kbytes in 256-Kbyte increments. Ports include six RS-232-C, one 8-bit parallel, and two disk/tape expansion. Display features a 14-in. nonglare blue or green phosphor screen and a 256 ASCII character set with graphics. Intelligent keyboard with multilevel programmable function keys frees the system processor to handle interactive processing. Price is $4495. **Onyx Systems, Inc,** 25 E Trimble Rd, San Jose, CA 95131. **Circle 280**

SYSTEM ELEMENTS

Signal-protected preamp

The Si1000 combines a low noise, low leakage FET, two diodes, and an optional resistor on a single die. It matches the impedance of infrared sensors and works equally well with electret or crystal microphones and electrostatic proximity sensors. Diodes protect the FET from any input signal voltage spikes. Typical gate-to-source breakdown voltage is 40 V with typical gate reverse current at 1 pA. Saturation drain current is 0.2 to 4 mA and gate-source cutoff voltage is typically 2 to 3 V. Unit price is $0.60 for 5000 pieces. **Siliconix Inc,** 2201 Laurelwood Rd, Santa Clara, CA 95054.

Circle 281

Low cost mouse

The compact controller employs optical encoding techniques offering 160 logic states/in. of travel high resolution. It offers high reliability with 1000 miles of travel. The RK280 is built with a modular construction and a user-removable ball. Usable on any flat area, it requires minimal operating surface. Interface is Schmitt trigger with quadrature output pulses. Options include RS-232-C interface and connector-type and pin assignment, as well as colors, shapes, and cable lengths. Prices range from $50 to $145 depending on quantity. **Optomicronix Inc,** 430 Ferguson Dr, Mountain View, CA 94043.

Circle 282

Tactile or linear feel keyboards

In two different keycap styles, the Next Generation Keyboard combines low cost, full travel, and sealed silver contacts for long life. Low profile KB IV sculptured keycaps are top mounted and removable. Smaller KB II keycaps are low profile and rectangular. The tactile model uses a dome-shaped silicone elastomer layer, while the linear version employs a conical-shaped metal spring. Based on an 83-key array, cost is $0.57 per key position, or $45 for a fully encoded serial output keyboard. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60087. **Circle 283**

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DSD would like to suggest that you can't back up that much Winchester with floppies.

Here's why.

It just takes too many floppies—20 or 40 (depending on capacity) to back up a 20 Mb Winchester.

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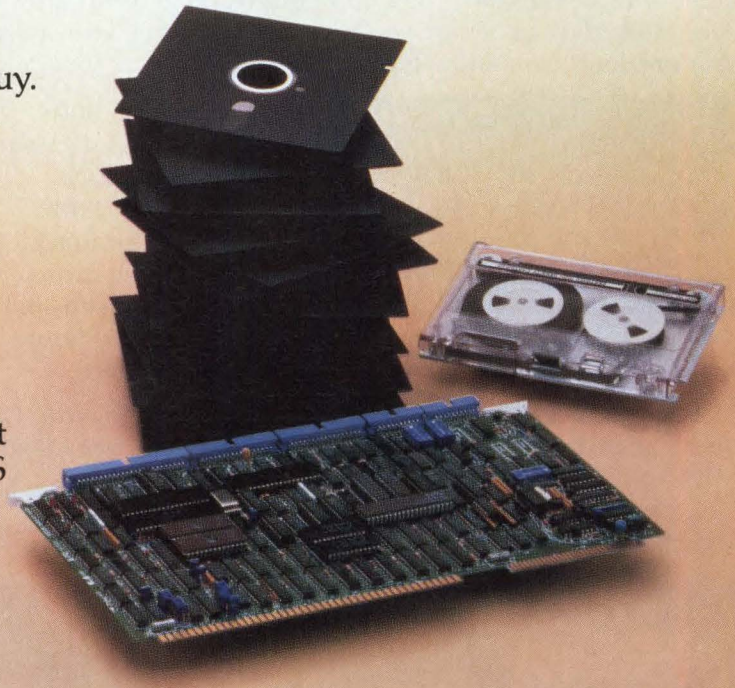

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CIRCLE 116

Q U A L I T Y

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At Brown Disc, we have spent the last two and a half years developing sophisticated flexible disc coating formulations, processes and quality methods. We have timed our developments to coincide with the growing maturity of the flexible disc industry.

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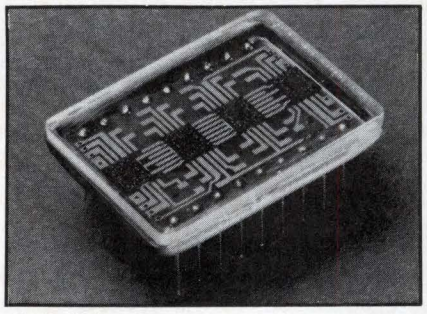
CIRCLE 117

Intelligent display

The MDL-2416 is a four-character peripheral with 0.15-in. high nonmagnified red, 16-segment (plus decimal) monolithic characters. It comes in a metal hermetically sealed package with a flat quartz lens and is manufactured to MIL-STD 833/Level B. The display can be stacked end-to-end to form lines, or top-to-bottom to form rows. The device is TTL and micro compatible and requires only a 5-V supply. The IC contains memory, ASCII ROM decoder, multiplexing circuitry, and CMOS drivers. In 100s, prices range from $85 to $125. **Siemens Components, Inc, Litronix Div,** 19000 Homestead Rd, Cupertino, CA 95014.



Circle 284

Spindle motor for 5¼-in. floppies

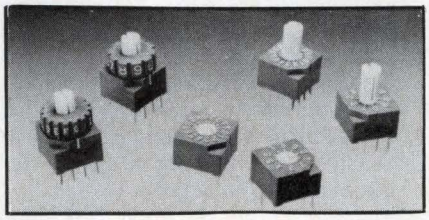
An ultraflat brushless direct drive motor, Model E2SLR uses a two-phase excitation motor for 1-in. thickness. Other features include a small circuit section (containing control and drive circuits) and outer rotor construction that minimizes magnetic leakage. Rated voltage is 12 V ± 10 percent; rated load is 150 g-cm; and rated speed is 300 rpm. **Sankyo Seiki Manufacturing Co Ltd,** 20911 Western Ave, Torrance, CA 90501. **Circle 285**

Low profile DIP switch

With the same dimensions as a TO-16 IC package, the series AD DIP switch is just 0.167-in. high. The gastight contacts rate contact pressure at 280,000 psi. The switch can withstand a 30-s solder dwell at 245°C. Housing and actuator are made of 94-VO rate polybutylene terethylate, which is compatible with aqueous, Freon, and chlorinated cleaning agents. Available in 2 to 10 positions, the switch is rated at 5000 cycles with price for the 8-position version at $0.61 in 10,000s. **Alcoswitch,** 1551 Osgood St, N Andover MA 01845.

Circle 286

Miniature DIP switches

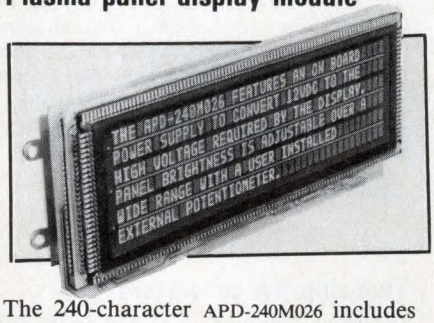


The SMS series is designed for electronic programming and presetting applications. The rotary coded devices are available in three configurations: screw driver, extended shaft, and shaft with number ring. In addition, four coding formats are available: BCD, BCD complementary, hex, and hex complementary. Features include gold-plated contacts and fully sealed construction. They can be flow soldered, fit into standard sockets, and are immersion washable. In 100s prices range from $2.52 to $3.36. **Shelly Associates, Inc,** 2942 Dow Ave, Tustin, CA 92680. **Circle 287**

Capacitor for power supplies

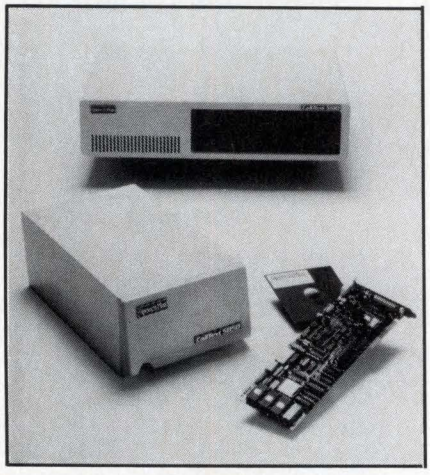
The hermetically sealed solid-electrolyte tantalum type 550D handles frequencies up to 100 kHz. It features low equivalent series resistance with a capability of handling high ripple current. Capacitance values range from 5.6 to 330 μF; voltage ratings range from 50 to 6 Vdc. Prices range from $2.84 to $6.68 each in quantities of 100 pieces, depending on rating. **Sprague Electric Co,** Marshall St, N Adams, MA 01247. **Circle 288**

Plasma panel display module



The 240-character APD-240M026 includes drive electronics and a dc-dc converter to develop necessary panel voltage. It provides six lines of 40 dot-matrix characters. Viewing characteristics include 30 ft-lamberts of brightness, neon-orange color, and 150-degree viewing angle. An external pot controls brightness. Basic price is $450 in quantities of 100. **Dale Electronics,** Box 609, Columbus, NE 68601. **Circle 289**

Phone retrieval of text data



CallText family devices combine a phone interface with a proprietary text-to-speech technology that automatically converts serial ASCII text to speech in real time. This allows a touch-tone telephone to access text information stored in data bases. The line includes an RS-232 peripheral unit operating under host control, a programmable system operating up to six channels simultaneously, and a module for the PC and compatibles. Each can answer the phone or initiate calls. **Speech Plus Inc,** 461 N Bernardo Ave, Mountain View, CA 94043.

Circle 290

Converter board with 16 channels

The 12-bit VMEbus compatible A-D board features software-programmable analog input gains from 1 to 1024. Typical conversion time for DSSE16AD12-2 is 25 μs. Settling time at gains less than 10 is 15 μs. Nonlinearity is $\pm$ ½ LSB; gain and offset errors are adjustable to zero. Jumper-selectable input modes include bipolar, unipolar, and 0 to 20 mA, 4 to 20 mA current loops. Common mode rejection at gain of 2 is typically 90 dB. The board takes eight consecutive memory locations. Price is $1995. **Data-Sud Systems/ U.S., Inc,** 2219 S 48th St, Tempe, AZ 85282.

Circle 291

Multibus-compatible board

Three-channel MCI-1794 converts Inductosyn or resolver signals into 12-bit resolution data words for machine applications. It offers complete electrical compatibility with 8080-, 8085-, and 8086-based systems as well as guaranteed minimum tracking up to 10,200 revolutions of pitches/min., and interfaces directly with 8- or 16-bit buses. Seven I/O ports are provided for read and write operations to and from each channel. The device can be ordered for operation with reference/signal frequencies of 400 Hz, 2.6 kHz, 5 kHz, or 10 kHz. Prices start at $1000. **Analog Devices Inc,** Two Technology Way, Norwood, MA 02062.

Circle 292

Flash converters

The SP9770 D-A converters combine 75-MHz sampling rate compatibility and 10-bit resolution with the ability to function as multipliers at 20 MHz. With complementary outputs, they can directly drive transmission lines at currents up to 30 mA. The converters accept inputs ranging between -0.81 and -0.96 V high, and -1.65 and -1.85 V low, and are ECL compatible. Settling time for LSB is 12 ns and resolution to ½ LSB is 10 bits or 0.098 percent. The 1- to 25-piece price is $220. **Plessey Solid State,** 3 Whatney St, Irvine, CA 92714.

Circle 293

Input MUX cards

The 6847 and 6848 plug into any EXORcisor backplane and contain complete isolation and multiplexing circuitry for up to 16 inputs. Both cards accept millivolt inputs with 15- to 150-mV spans. Circuit design uses an amp-per-channel approach employing a single transformer for signal and power isolation. A voltage to current converter for each channel generates current proportional to the low level input signal. Each card offers input channel sampling rates up to 5500 channels/s. **Acromag, Inc,** 30765 Wixom Rd, Wixon, MI 48096.

Circle 294

Two-chip D-A converters

Designed for high accuracy and wide temperature range, the DAC870/MIL suits military, industrial, and ATE applications. The 12-bit chip comes in an LCC that conforms to JEDEC Standard No. 1. Total accuracy without trim adjustments is $\pm$25 percent FSR, decreasing to $\pm$0.4 percent FSR over temperature. Differential linearity error is less than $\pm$1 LSB over temperature, guaranteeing monotonicity from 55 to 125 °C. Gain drift is less than 25 ppm/ °C. Prices start at $35 in 100s. **Burr-Brown,** International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734.

Circle 295

Converter boards

The SCB-15 series interfaces with multiple pole or geared synchros/resolvers. The two-speed boards have standard speed ratios of 1:8, 1:16, 1:32, or 1:64. Accuracy is $\pm$3.3 s to $\pm$64 s over temperature, while repeatability is as low as $\pm$2 s of arc. Automatic phase correction eliminates errors. Input synchro/resolver misalignments of up to 8 degrees will not cause ambiguous output readings. Unit prcing ranges from $670 to $995. **Control Sciences, Inc,** 9509 Vassar Ave, Chatsworth, CA 91311.

Circle 296

Multichannel conversion system

Designed to interface with most control logic, the LCDAC12 features 12-bit resolution, dual-rank input registers, and 500-kHz data update. Principal application is in function generator systems for simulation or model testing and structural analysis. The 12-bit resolution has a full scale accuracy of $\pm$0.01 percent when operated from a high stability internal reference voltage. Each channel provides a minimum of 5 mA with a $\pm$10-V output. Output impedance is 1 Ω or less. A typical 64-channel system is priced at $14,900. **Preston Scientific,** 805 E Cerritos Ave, Anaheim, CA 92806.

Circle 297

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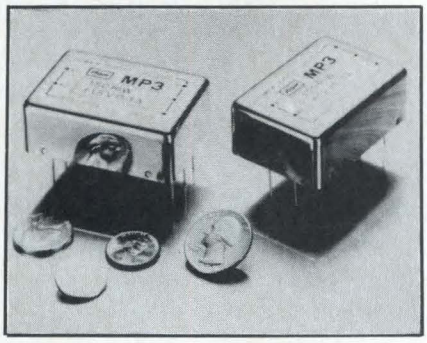
Otari Singapore Pte., Ltd. *Golden Mile Complex, 5001 Beach Rd. #03-50, Singapore 0719 Phone: 294-5370, Telex: RS36935 OTARI*

OTARI®

CIRCLE 118

Encapsulated switchers



Compact power supply series MP3 has high speed switching capabilities and high efficiency (65 percent). Single- and dual-output units provide an input voltage range of 90 to 132 Vac and meet UL and FCC specifications. Components are designed for applications emphasizing small size, light weight, and low cost. Weight is 80 g. **KSC Electronics, Inc,** 543 W Algonquin Rd, Arlington Heights, IL 60005.

Circle 298

Power transistors

The npn silicon power devices are housed in isolated S^2 Pak (TO-228AB) and TO-61 cases. The 1500-V transistors can handle up to two times more current than conventional types. High power dissipation and increased thermal characteristics are features. They are available with custom or standard leads. Both versions were designed for high voltage, fast switching power supply applications. In 1000s, prices range from $45 to $54. **Solitron Devices, Inc,** 1177 Blue Heron Blvd, Riviera Beach, FL 33404.

Circle 299

Fast switching transistors

Specifically designed for 220-V line operated push-pull switching configurations, the MJ16006A/10A (8 and 15 A) feature high, safe operating areas. At 100°C, fall times of 80 ns at 5 A and 50 ns at 10 A are available. Fast switching within a safe operating area comes from a high periphery-to-area ratio. Hollow emitter structure optimizes the current density under the emitter during transistor turnoff and helps alleviate current pinching effect. The 100 and up price is $4.85 to $7.30. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.

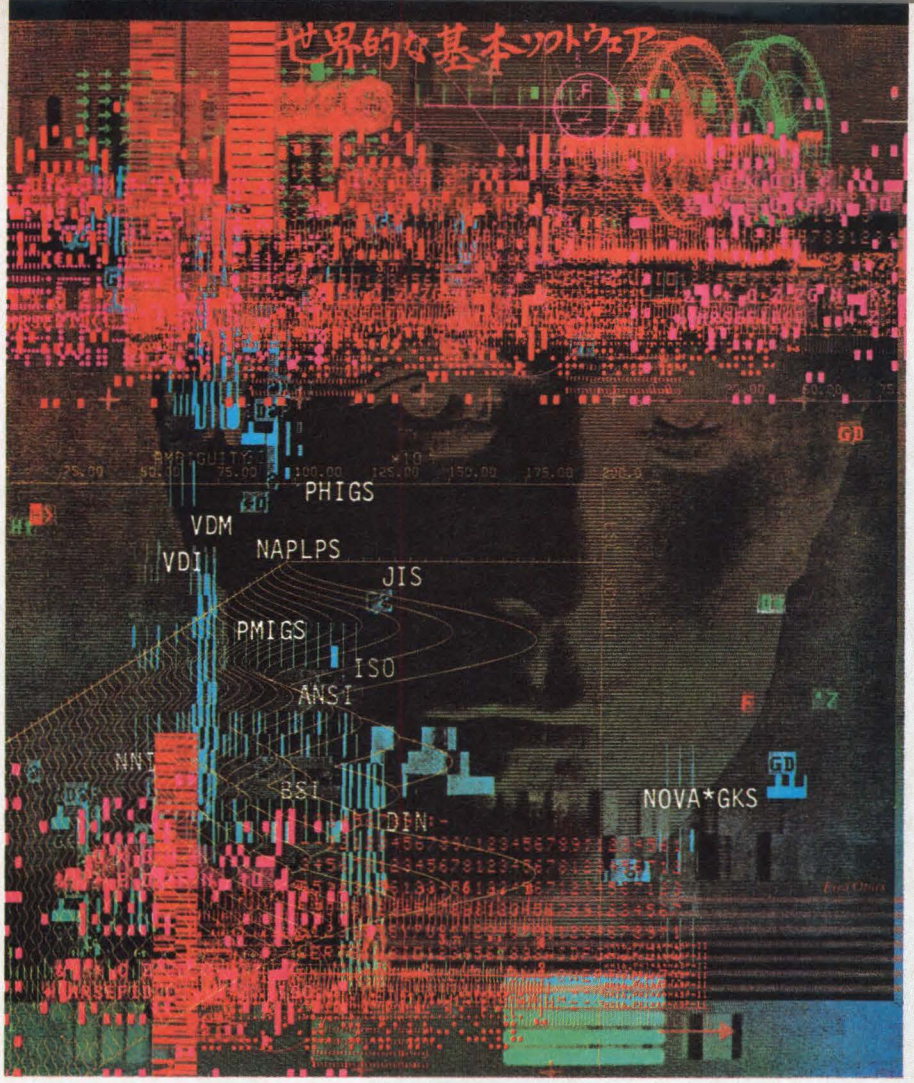
Circle 300

Talker/listener for power supply

The TLA communicates with computer controllers using the CIIL language over an IEEE 488 bus. It recognizes and responds to the nouns and verbs of CIIL using a built-in 8088 CPU to drive field installable analog cards. Each card handles up to four independent power supplies. Examples of commands include function, set, close, open, reset, internal self-test, confidence test, and status. Prices range from $2950 to $5950. **Kepco, Inc,** 131-38 Stanford Ave, Flushing, NY 11352.

Circle 301

CIRCLE 119



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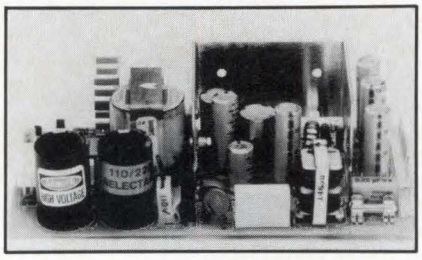
CIRCLE 120

Supply for CRTs and floppies



Both the XL50-3603 and -3655 are four-output, open frame switchers designed specifically for CRTs and 5¼-in. drives. One 12-V output provides enough current to power two 5¼-in. floppies—while the other provides clean, highly filtered current for the CRT. The 7 A on the 5-V output can power a 16-bit micro. Supplies run at 60- to 65-W output power and include a 110/220-Vac, user-selectable input voltage, input surge protection, and over-voltage protection on the 5-V output. In 100 units, price is $80 each. **Boschert Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94086. **Circle 302**

Power supplies

The MX series yields 60 kV at 0.8 mA with voltage and current regulation better than 0.01 percent. It operates on a standard 120-Vac input, thus eliminating the need for an auxiliary low voltage dc supply. Features include remote voltage and current programming/monitoring, automatic crossover from voltage to current regulation, and low stored energy for safety. Twenty different models range from 0 to 5 kV at 10 mA and 0 to 60 kV at 0.8 mA. Prices range from $620 to $1385. **Glassman High Voltage,** Rte 22, PO Box 551, Whitehouse Station, NJ 08889.

Circle 303

Winchester power supply

The CP542 powers a 5¼-in. Winchester disk drive and disk-drive controller board. Outputs are 5 V at 2.6 A and 12 V at 1.5 A (continuous); 3.5 A (peak surge). Line regulation is 1 percent for a 10-percent line change, while load regulation is 1 percent for a 50-percent load change. Output ripple with peak to peak maximum is 25 mV. Other specs include transient response of 50 μs for a 50 percent load change and a 55-percent typical efficiency. Price in 1- to 24-piece quantities is $54.95. **Power-One, Inc,** Power-One Dr, Camarillo, CA 93010.

Circle 304

Power MOSFET

A high voltage device with a fast-reverse internal diode, the BUZ211 derives reverse recovery characteristics from a reduced minority carrier lifetime. Electrical specifications include minimum breakdown voltage of 500 V, maximum onstate resistance of 0.8 Ω, and maximum permissible drain of 9 A. Operating and storage temperatures range from −55 to 150 °C. Prices are under $15 in 1000-piece quantities. **Siemens Components, Inc, Colorado Components Div,** 800 Hoyt St, Broomfield, CO 80020.

Circle 305

Terminal controllers

Providing all basic functions of a data terminal, including text and graphics control, the NS455 controllers act as terminal management processors. The series includes NS456 masked-ROM version for high volume applications; ROM-less NS405; and NS455, which is preprogrammed for standard character-oriented terminals. The terminal controller chips replace as many as seven separate devices with a single 48-pin IC. Based on 8-bit 8048 microarchitecture and instruction set, units operate in character or graphics mode. Volume pricing is approximately $19. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 306**

Monolithic instrumentation amp

Capable of delivering high output current, the AMP-01 supplies up to 90 mA peak and is stable with capacitive loads to 1 μF. Characteristics include low noise, low offset voltage and drift, 16-bit linearity at a gain of 1000, and common mode rejection of 130 dB. Bias current is 3 nA to minimize errors from high signal source resistance. Any gain between 0.1 and 10,000 can be selected by suitable external resistor ratio selection. In 100-piece quantities, chip pricing starts at $16.90 for military and $9.90 for industrial. **Precision Monolithics Inc,** 1500 Space Park Dr, Santa Clara, CA 95050.

Circle 307

Chip set for controller design

A third-generation CMOS VLSI set consists of three separate devices: data sequencer, four-channel memory controller, and MFM data separator. The fully programmable PFM 5050 sequencer provides high speed bit-serial data management, format control, and error detection. The sequencer is used directly with NRZ interfaces such as SMD, LMS, and ESDI. A four-channel memory controller provides buffer management and data transfer control functions. Prices in quantities of 10,000 range from $5.75 to $30.51. **OMTI,** 557 Salmar Ave, Campbell, CA 95008. **Circle 308**

Single-port multiplier/accumulator

Architecture of the ADSP-1110 allows it to fit in a 28-pin plastic DIP. The MAC dissipates 150 mW maximum and provides a 40-bit internal accumulator, as well as logic to reduce external circuitry and simplify digital signal processing design. Operating with a 10-MHz clock, it alternately loads X and Y operands and outputs at a 100-ns I/O cycle time, all through a single port. Input and multiply/accumulate operations overlap to attain 200-ns MAC time. Other features are an onchip overflow flag and saturation logic for setting either the MSB or LSB. Price is $72 in 100s. **Analog Devices Inc,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. **Circle 309**

Linear phase data filters

A CMOS dual low pass switched-capacitor filter chip, the MC145415 provides band limiting and signal restoration filtering. Onchip digital clocking circuitry allows an external clock to tune low pass break frequencies. Features are low operating power consumption (30 mW typical), two fifth-order low pass filters, and ± 5- to ± 8-V power supply ranges. Passband edges are tunable with a clock frequency from 1.25 to 10 kHz. Price is $3.03 in quantities of 1000. **Motorola Inc, MOS Microprocessor Div,** 3501 Ed Bluestein Blvd, Austin, TX 78721. **Circle 310**

Onchip diagnostics for PROMs

Designed for board- and chip-level testing of digital systems, the 53/63D1641/43 features onchip shadow registers that eliminate embedded diagnostic codes. These codes (test vectors) are serially shifted into the shadow register, then transferred to the output register for execution. The 16-Kbyte devices can be serially cascaded in applications for wide control words in microprogramming. Both devices provide 24-mA output drive and feature maximum setup speed of 40 ns and clock-out time of 20 ns. Organized as 4096 words x 4 bits, the 24-pin package is priced at $50.40 in 100s. **Monolithic Memories, Inc,** 2175 Mission College Blvd, Santa Clara, CA 95050.

Circle 311

Advanced Schottky family

Twenty-two functions upgrade the ALS/AS family. These functions include counters, comparators, flipflops, transceivers, and buffer/drivers. Many are pin compatible with existing Schottky or low power Schottky parts, and offer improved throughput plus reduced power dissipation. Other features include wider threshold and noise margins, and improved line-driving and -receiving capabilities. The functions are characterized for operation over the commercial temperature range and are available in plastic DIPs and LCCs. Prices depend on function. **Texas Instruments, Semiconductor Group,** PO Box 401560, Dallas, TX 75240.

Circle 312

Fully static CMOS RAM

The 32,768 x 8-bit EDH8832C is pin compatible with JEDEC bytewide memory pinout. Operating with a single 5-V supply, the chip has address access times of 120, 150, and 200 ns. Maximum active power dissipation is 650 mW and standby is 25 mW. It is EBM-pack compatible and conforms to the industry standard 28-pin DIP mechanical outline. In 100-pieces, the 150-ns version is $312.95, and the 200-ns version is $299.95. **Electronic Designs Inc,** 35 South St, Hopkinton, MA 01748.

Circle 313

Interrupt control coprocessor

Used in combination with the 200-ns 8X305, the 8X310 adds hardware interrupt and subroutine handling for interrupt-driven realtime control systems. It unburdens the host by operating synchronously on the system's instruction and data buses. The chip monitors binary flow to capture, decode, and process interrupt and subroutine call requests. It features three maskable, priority-set interrupts, interrupt disable, four-level LIFO stack, and stack-full flag. In quantities of 100 to 999, the chip is $15 for plastic and $23.50 for ceramic. **Signetics Corp,** 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086.

Circle 314

April Preview
Special Report on Disk Memory

Two-micron gate array

The SCX6248 is a high speed, 4.8-Kbyte CMOS device with a typical gate delay of 1 ns. The array has eight pairs of power and ground pins, one test pin, and 107 signal pins (53 input-only, 54 bidirectional I/O). Input signal pins can be selected in any combination of TTL or CMOS compatibility, with or without pull-up resistors. An internal test feature forces all output buffers to high/low or 3-state conditions. A 3-μm size version is also available with gate delay of 2 ns. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 315**

Multiplier with bipolar speeds

The 12 x 12 parallel MPY-121IMI provides 2's complement, unsigned magnitude, or mixed mode. It operates with power consumption of less than 150 mW at 5 V. The CMOS version features a typical multiply time of 150 ns, while faster versions with multiply times equivalent to bipolar are also available. Besides the currently offered 64-pin DIP and flatpack, the multiplier will be supplied in LCC, pin grid, and leaded chip carrier packages. **International Microcircuits Inc,** 3350 Scott Blvd, Santa Clara, CA 95051. **Circle 316**

Skinny NMOS RAM

Organized 2-K x 8, the 2015 has a width of 0.3 in. Four access times are available: 90 ns with an operating current of 80 mA, and 150, 120, and 100 ns with an operating current of 65 mA. All have a standby current of 7 mA. The chip is directly TTL compatible and operates from a 5-V single power supply. Packing of the 24-pin DIP is JEDEC standard. Chip is designed for cache or buffer memory applications. Pricing, in 100s, is $7. **Toshiba America, Inc,** 2441 Michelle Dr, Tustin, CA 92680. **Circle 317**

Linear arrays

Measuring 123 x 156 mil, the MON monochip includes more than 1100 linear components. Available components include npn transistors, dual-collector pnp transistors, vertical pnp transistors, Zener diodes, bonding pads, and assorted resistors. The MOK design kit containing all the information needed to design a MON integrated circuit is available for $59. Integration fee, which includes 50 prototypes, is $9000. Production prices range from $3.50 to $15 depending on volume, type of packaging, and type of screening and testing required. **Interdesign Inc,** 1500 Green Hills Rd, Scotts Valley, CA 95066. **Circle 318**

Track and hold amplifier

Delivering 14-bit performance, the AD389 offers a typical acquisition time of 2.5 μs $\pm$0.003 percent. The typical 400-ps aperture jitter permits 14-bit conversion at rates to 40 kHz. Maximum droop rate of 1 μV/μs and elimination of offset drift due to self-heating permits 14-bit conversion times to 300 μs for slower conversion rates. It accepts a $\pm$10-V input and provides a -1 V/V gain. Typical dc specs include $\pm$0.01 percent gain error, $\pm$0.001 percent gain nonlinearity, and 1 ppm/°C gain drift. Prices in 100s from $74 to $121. **Analog Devices Semiconductor,** 804 Woburn St, Wilmington, MA 01887. **Circle 319**

Precision op amp

This dual amplifier combines low offset, low noise, high speed, and guaranteed amp matching characteristics in one device. The MP-OP-227's construction obviates external components for offset nulling and frequency compensation. Specifications include noise 3 nV/$\sqrt{\text{Hz}}$, voltage match of 25 μV, and offset of 10 μV. Applications include tape heads, wideband instrumentation, low level transducers, and threshold detectors. Prices, in 100s, range from $6.95 to $49.50. **Micro Power Systems, Inc,** 3100 Alfred St, Santa Clara, CA 95050. **Circle 320**

Controller for CRT

Together with a suitable micro and 4-Kbyte minimum memory, the SAA5350 allows the construction of a Videotex terminal. Data representing codes of the displayed characters passes, under micro control, to the chip. Product includes timing chain, character generator, attribute logic, DRCS logic, video screen logic, and micro interface. Onchip ROM uses all characters in the ISO norm. Character shape is based on a 12 x 10 dot-matrix cell. The chip is packaged in 40-pin plastic. **Philips Electronic Components and Materials Div,** PO Box 523, 5600 AM Eindhoven, The Netherlands. **Circle 321**

INTERFACE

Micro peripheral board

Interfacing RTD signals directly with process control computers, the MP8430 is a multiplexed 16-channel input digitizer. Each channel is line-length compensated by an exciter circuit. This circuit produces voltage proportional to the temperature reading, which is then filtered, amplified, and sent to the 12-bit A-D converter. Features include input noise filtering, programmable gain instrument amp, and 16- or 20-bit memory, or 8- or 12-bit I/O mapping. The board occupies 4 bytes of address space and fits on any 4-byte boundary. Price is $750 in one to nine quantities. **Burr-Brown, Data Acquisition and Control Systems Div,** 3631 E 44th St, Tucson, AZ 85713. **Circle 322**

Floppy disk controller

Using DMA arbitration to handle any combination of four 8- or 5¼-in. drives, the Disk 1A is designed for high level industrial and scientific microcomputer systems. It conforms to all IEEE 696/S-100 specifications and is fully compatible with six CP/M- and MP/M-based operating systems. Features include a high speed cycle-stealing DMA interface that allows processor independent data transfer up to 10 MHz between memory and disk. The interface also provides 24-bit DMA addressing across 64-Kbyte boundaries, with data transfer throughout the 16-Mbyte memory. Price is $695. **CompuPro,** 3506 Breakwater Ct, Hayward, CA 94545. **Circle 323**

Graphics controller for PC

Implementing the ANSI GKS virtual device interface standard, the Graphcard 100 expands the PC or XT to a high performance monochrome graphics system. Standard features include both serial and parallel printer ports as well as a serial mouse port. The 80186 provides fast graphics display at 720- x 352-pixel resolution and an intensity level for highlighting. Concurrent rasterization and application processing enable supported dot-matrix printers to generate output at the highest resolution available in formats up to 11 x 14 in. Cost is $1250. **Concept Technologies, Inc,** PO Box 5277, Portland, OR 97028. **Circle 324**

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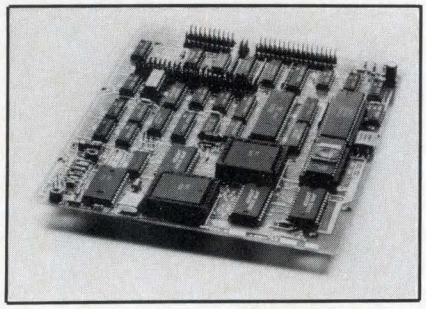
CIRCLE 123

Multifunction disk controller



The series 5000 attaches ST506 interface-compatible 5¼-in. Winchester and floppy drives along with 1/4-in. streaming tape drives, to host computers. Features include consecutive sector data transfer, 2-Mbyte host data transfer rate, and an intelligent buffer management system. Models in the series support from two to four drives in combinations of fixed, fixed/removable, or removable. Prices in quantities of 1000 range from $199 to $344. **OMTI,** 557 Selmar Ave, Campbell, CA 95008.
Circle 325

Multibus-compatible motherboard

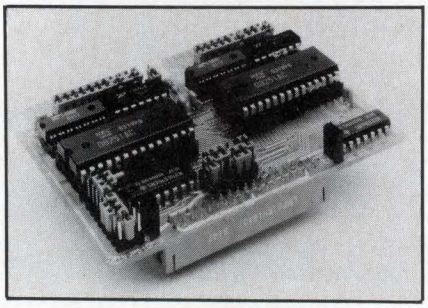
The Am94/2000's six connectors support single- and double-width modules not requiring DMA. The board also includes resident Multibus address decoding and data buffering plus Multibus/SBX timing reconciliation. Onboard connectors handle 8- or 16-bit SBX modules. In addition, the Am94/1530 is a programmable dual-channel serial communication module, allowing the user to add I/O capability to a Multibus system. It can handle asynchronous formats, synchronous byte-oriented protocols, and synchronous bit-oriented protocols. Motherboard is priced at $495, while the communication module is $395. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 326

Universal controller

The two-channel 316 DMA controller is a Q-bus peripheral providing data block transfer capability between memory and other peripherals. Each of the two channels performs peripheral to peripheral and memory to memory transfer. A search mode compares data read from memory or peripherals to the content of a pattern register and sets a flag bit as a match. It can operate with either byte or word data sizes and data transfers through byte-wide peripherals are provided by the byte packing/unpacking capability. **Grant Technology Systems Corp,** 11 Summer St, Chelmsford, MA 01824.
Circle 327

Two-channel expansion module

Based on two 8251A USARTs, the GDX-Serial-2S is an RS-232-C compatible module for adding serial peripheral devices to single-board computer systems. It receives timing signals from the host board, a modem, or an external source. With an 8-bit data bus the module is compatible with both 8- and 16-bit systems. Data transfers originate by polling the status register of the USARTs or by interrupts from four separate USART signals. Price for one module is $160. **General Digital Corp,** 700 Burnside Ave, E Hartford, CT 06108.



Circle 328

Peripheral link from PC to STD-bus

The PC/STD link consists of two circuit cards linked by a ribbon cable. It serves as an interface and controller between the systems, providing parallel communications with optical isolation and parity checking. The two boards can be up to 200 ft apart and are optically isolated. Companion Mac Pac holds up to 13 STD-bus cards, and contain a power supply and internal cooling system. Each device is priced at $1295. **rmac,** 716 Capitola Ave, Capitola, CA 95010.
Circle 329

Disk controller

Plug-compatible with the burst MUX channel on Data General minicomputers, the BMX-1 allows selection of any SMD interface disk drive. It offers four disk drive connect ports with software-configurable drive characteristics on a port by port basis. The controller ensures data integrity and error recovery through an onboard 32-bit ECC, offering error detection with burst error correction to 11 bits. EEPROM eliminates the need for switches and makes all functions configurable via downline loaded software. Price is $4995. **Custom Systems, Inc,** 6850 Shady Oak Rd, Eden Prarie, MN 55344.
Circle 330

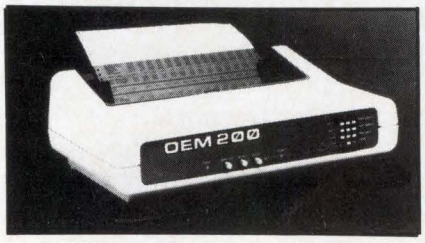
Tape coupler

The TC7000 brings GCR tape format high density performance to the VAX 11/750 and /780. The extended hex-size PC board plugs into the CMI bus via a slot in the V-Master chassis that can reside in the SBI terminator space of the VAX. It supports both industry standard Pertec and STC tape formatter interfaces. Format is operator selectable. Tape speeds from 12.5 to 125 in./s can be handled. Internal self-test routines are automatically executed at power-up. Power requirement is 5 V at 10 A. In 100s, cost is $2880. **Emulex Corp,** 3545 Harbor Blvd, PO Box 6725, Costa Mesa, CA 92626.
Circle 331

PERIPHERALS

Matrix printer

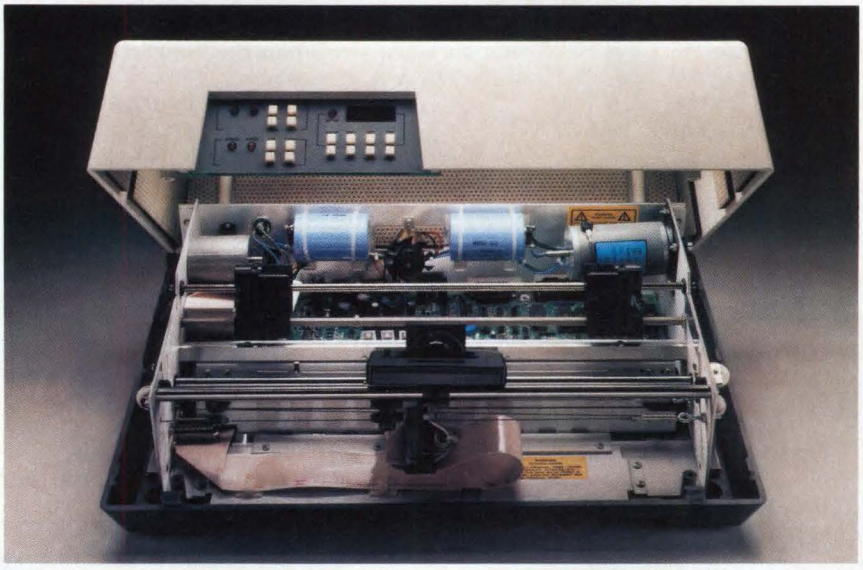
The OEM 200 has a heavy duty printhead rated for continuous duty and an expected lifetime of over 100 million characters. It can print a full 136-char line at 10 chars/in., or through a 17 char/in. density, 231 columns can be printed. The 7 x 9 dot-matrix is used for high speed data printing while an 11 x 9 is used for near letter quality. High resolution dot-addressable graphics capability is included. The printer costs $1045. **Micro Peripherals, Inc,** 4426 S Century Dr, Salt Lake City, UT 84123.



Circle 332

HIGH PERFORMANCE

IT'S WHAT'S UNDER THE HOOD THAT COUNTS



Take a close look under the hood of a Datasouth printer. Inspect for loose parts, cheap fittings. Search for things that show more concern for speed on the assembly line than the communications line.

You won't find them. Instead you'll find the source of the Datasouth reputation: design, engineering and materials dedicated exclusively to *high performance* value.

Now look closer.

MORE THAN THE HUM OF ITS PARTS

Count the moving parts in a Datasouth printer. You won't find many. Most of those are dedicated to transporting the printhead and the paper from point to point with optimum speed and accuracy, while the rest of the printer sits quietly with the motionless authority of a Stonehenge.

And thinks.

Under the hood of every Datasouth printer is a highly intelligent microprocessor. Its sophisticated brainwork eliminates the need for many parts still common in other printers, and optimizes carriage and paper travel so the printhead intelligently follows the shortest path from one printable character to the next. So more work gets done with less strain on the machinery.

MODULAR MAINTENANCE

Datasouth design simplicity assures easy maintenance. All control electronics are on a single printed circuit board. The 9 wire printhead is rated at over 500 million characters, and is easily replaced in minutes. Everything that matters is easy to reach, right there under the hood. Even the cartridge ribbon, rated at 3 to 4 million characters, snaps into place in seconds.

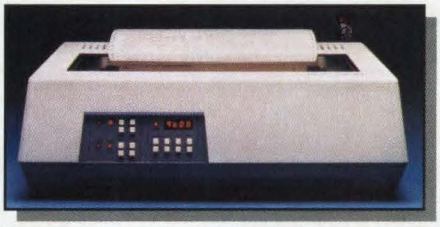
JUST TURN THE KEY

Datasouth printers are easily driven by virtually any mini or microcomputer. The fully instrumented dashboard allows the user to program up to 50 different applications features at the touch of a few buttons. Meanwhile, the digital readout shows everything from programming prompts to line count.

TAKE YOUR CHOICE

Datasouth reliability comes in two high performance models. The DS180 is a legendary workhorse that delivers crisp data quality printing at 180 CPS. The new multimode DS220 cruises at 220 CPS for high speed data printing and at 40 CPS for letter quality word processing. Both models print precision dot-addressable graphics.

If you have a high performance printing need, Datasouth has a high performance printer to fill it.



DRIVE ONE TO WORK TODAY

Both the DS180 and the DS220 are on display at more dealer showrooms every day, including one near you. So go take a hard look at the kind of hard copy you get from high performance Datasouth printers.

See what *really* counts when you compare printers.

datasouth

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CIRCLE 124

Datasouth Computer Corporation
Box 240947 · Charlotte, NC 28224
704/523-8500 · Telex 6843018 DASOU UW

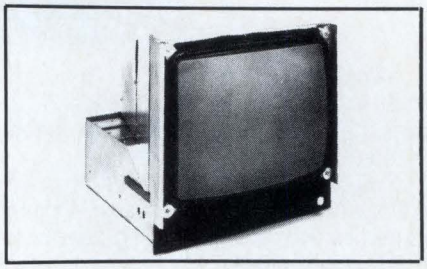
Dual-mode plotters

The 107X family features three plotters with diagonal plotting speeds ranging from 21 to 52 in./s. They feature a 36-in. wide continuous roll-feed, as well as 34- x 30-in. cut-sheet plots. The units come with 68000 micros that provide scaling techniques, rotation, mirroring, and form alignment. The plotting bed is set in a vertical position so the operator can see the plot as it is drawn. Field upgradable, the plotters range in price from $14,950 to $24,500. **California Computer Products, Inc,** 2411 W La Palma Ave, Anaheim, CA 92801.
Circle 333

Fast dot-matrix printer

The 7065 is fully compatible with both Epson and Anadex escape codes. It operates at a high speed draft copy rate of 300 chars/s; at 250 chars/s in compose mode; and 125 chars/s in near letter quality. Letter-quality prints at 65 chars/s. In the graphics mode, resolution of up to 144- x 144-bit-mapped dots/square in. at a repetition rate of 1500 dots/s per activated needle is available. Other features include proportional spacing, right-hand margin justification, auto-underline, overprint and bold, downloadable fonts, and an expandable buffer. Cost is $1995. **North Atlantic Industries, Inc, Quantex Div,** 60 Plant Ave, Hauppauge, NY 11788. **Circle 334**

Color raster monitors



Designed for graphics applications, the ST310/64 features a 1280- x 1024-addressable pixel resolution with a 60-Hz flicker-free refresh rate. The rackmountable monitor is 18 x 17.5 x 18 in., and the electronics are completely encased in metal to meet FCC energy emission requirements. Because it is designed for FCC class A certification, no further certification is required. Price is $3120 in quantities of 500 units. **Saber Technology Corp,** 79 S Third St, San Jose, CA 95113.
Circle 335

Speech output module

Combining high quality speech, low price, and flexibility, the module can be used wherever human speech is the preferred form of communication. It connects directly to a computer, terminal, printer, plotter, or other peripheral. The module communicates via a serial RS-232 hardwired line at speeds to 19,200 bits/s. Vocabulary can be downloaded from a host computer file or can reside in user-defined EPROM. The EPROM-based vocabularies contain 200 words, while the downloaded version is limited only by host memory. Cost is $781. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 336**

CIRCLE 125

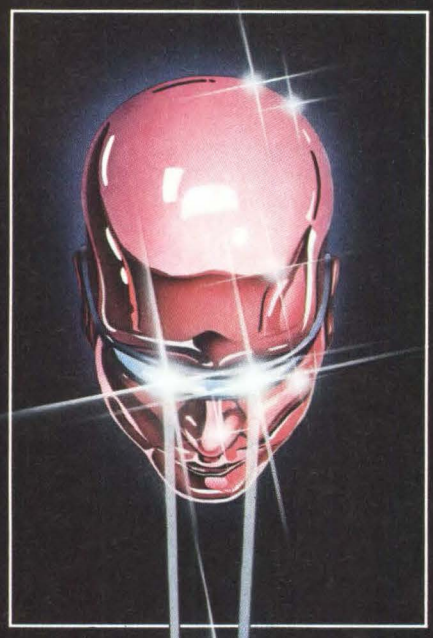
The Convergence Factor.

Convergence: the single most critical factor in color CRT performance.

Until now, Delta-gun tubes were the best way to achieve near perfect convergence, but only with costly adjustment electronics. Meanwhile, many in-line tubes are plagued by perceptible misconvergence. Which can lead to poor picture quality. A poor quality image for your product. And poor, bleary-eyed operators.

The Panasonic achievement: low cost in-line color CRTs with better-than-Delta convergence performance.

Without complex adjustment electronics . . . and none of the convergence drift inherent in active correction systems. At last, high resolution in-line tubes with stable performance that stands up to the ravages of time and tough office/industrial environments.



How did we do it? With a preconverged in-line tube/yoke combination unlike any other. Our precision S/ST (saddle/saddle toroidal) deflection yoke is ideally matched to each tube, for near perfect convergence, high repeatability and stability over a wide range of operating conditions.

We combine it with a specially-designed OLF (overlapping field lens) gun and unitized grid construction, providing spot uniformity across the entire screen and near-Delta resolution.

The result: a triumph over the convergence factor. Find out what it can do for your next color terminal or monitor, and ask about our full line of quality color and monochrome CRTs. Write or call: Panasonic Industrial Company, Electronic Components Division, One Panasonic Way, Secaucus, N.J. 07094; (201) 348-5278.

The achievement of Panasonic high resolution in-line color CRTs.

Panasonic
Industrial Company

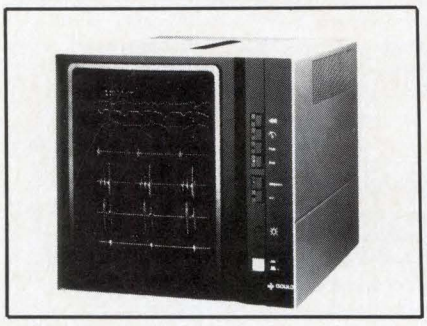
CIRCLE 165

High speed serial printer

A multifunction, high speed serial dot-matrix printer is designed for mini and microcomputer applications. The MT-440 features variable quality printing, operator-programmable type pitch, and a choice of paper feeds. Printer runs at 400 chars/s in draft mode and 100 chars/s in letter-quality mode. Tabbing feature allows the printhead to travel at speeds of up to 650 chars/s when bypassing blank parts of a line. It can print 10, 12, or 16.7 chars/in. Prices range from $2395 to $2995. **Mannesmann Tally Corp,** 8301 S 180th St, Kent, WA 98031.

Circle 337

Monitor for chart recorder



The V1000 video display shows a full 8½- x 11-in. page and allows users to see changing signals on the CRT as they are sent to the ES 1000 chart recorder. The chart drive need not be operating for CRT monitoring to take place. The terminal has a high resolution 12-in. TV monitor with 945 lines of 1024 dots and an internal memory of 880 x 1024 bits. All timing and control signals are generated by the recorder. Four modes are available for control: roll, refresh, page, and stop. Prices start at $4995. **Gould, Inc, Recording Systems Div,** 3631 Perkins Ave, Cleveland, OH 44114.

Circle 338

Processing terminal

Designed with IBM PC architecture, the device reduces the load on a central computer by distributing processing power without decentralizing data bases. Main processor has an 8088 with 8087 math coprocessor chip, up to 256 Kbytes of RAM, two serial ports, and a parallel port. A micro-controlled communication board handles bit-oriented protocols and a video board interfaces with both monochrome and color display monitors. A memory board supports RAM, EPROM, and EEPROM in various densities. **Datamedia Corp,** 7401 Central Hwy, Pennsauken, NJ 08109.

Circle 339

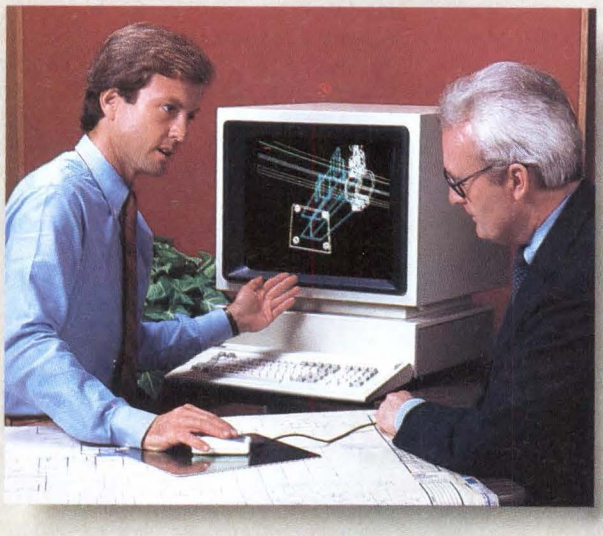
Letter-quality printer

The 20-char/s LetterPro 20 is compatible with most personal computers. Interface options include Centronics parallel, RS-232 serial, and Qume Sprint 3. The printer uses ribbon cartridges and a 96-character printwheel. More than 100 different printwheels are available. MTBF is 2000 hours. Price is $899. **Qume Corp, Sub of ITT,** 2350 Qume Dr, San Jose, CA 95131.

Circle 340

CIRCLE 126

FOR A REFRESHING NEW LOOK AT COLOR GRAPHICS PUT A GENISCO G-2200 IN YOUR SYSTEM. IMPELL CORPORATION DID!



The G-2200 is truly a refreshing approach to raster color graphics. It combines vivid colors, flicker-free picture clarity, and big screen readability with high speed graphics and extensive software support. The result is the most cost effective system on the market. That's why Impell Corporation selected it as the perfect color graphics companion to CAEMIS, their Computer Aided Engineering & Management Information Services package.

Impell is a major supplier of computer software and computer based management and engineering services to the utility industry worldwide. CAEMIS is a modular, three dimensional engineering design and data base management system which provides simultaneous access for all design functions and on-line access to design information. And, the Genisco G-2200 is its window to the world.

The G-2200 has all the features desired for CAD/CAM, CAE, scientific and business graphic applications including built in peripheral support for mouse, tablet and printer. It is software compatible with the Tektronix 4014 and supported by third party software. It will also emulate the DEC VT100 for text editing and data entry.

But the best reason to put a G-2200 in your system is picture quality. Up to 16 colors can be selected from a palette of 4,096 hues with a unique black matrix glass bringing them vividly to life. Graphics are displayed on a big 19 inch screen that is refreshed at 60Hz for flicker-free viewing while the 1024 x 792 resolution ensures sharpness and clarity. No comparably priced system can match the picture quality of the G-2200.

The G-2200 is available as an attractive, ergonomically designed desktop terminal, or it can be integrated in your own system as a board or as a controller. Whatever the configuration, you can be sure of Genisco's commitment to design and production excellence and to on-site support by its international network of offices.

For details on how the G-2200 can color your system, call us for a demonstration. It will be a most refreshing experience.

Genisco

GENISCO COMPUTERS CORPORATION
3545 CADILLAC AVENUE
COSTA MESA, CA 92626
(714) 556-4916
TWX 910-595-2564

CIRCLE 160

Protocol converter

The PA-1000 allows terminals such as the VT-100 to emulate an IBM 3278-2 or personal computers to attach to an IBM host via a coaxial cable. Terminal port is RS-232-C compatible, 300 to 9600 baud programmable with modem control. EIA signals include transmit data, receive data, clear to send, and data set ready. For passthrough mode, modem controls transmit from port to port. In addition to the VT-100, the converter supports IBM 3101, LSI ADM5, Televideo 910, and ADDS Viewport. **3R Computers,** 18 Lyman St, Westboro, MA 01581.

Circle 348

Communication system

Designed for both voice and data communication, CBX II features a distributed architecture using fiber optic links. Modular expandability supports 16 to 10,000 users. Communication handling capacity is 4.4 Gbits/s. The system consists of from 1 to 15 nodes. A single-node system supports several hundred users with each node independent of the others. Architecture is based on a high speed parallel time division multiplexed bus at each node. **ROLM Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.

Circle 349

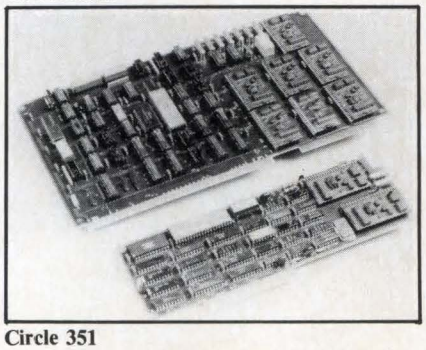
High speed transmission MUX

The 330B dataplexer lets 32 independent data channels share a single composite data link. In addition to a standard RS-232-C interface, an integral digital line driver/receiver provides 64,000-bit/s communication over common housewire for distances of a mile or more. Menu-driven programming system lets users select system and individual-channel parameters, execute diagnostics, and retrieve operating statistics. **Tellabs, Inc,** 4951 Indiana Ave, Lisle, IL 60532.

Circle 350

Local area network capability

The Zebra computer family now offers LAN capability via Arcnet. Using controllers, up to 255 Zebra computers link in a variety of network configurations to exchange data and messages. The controller uses a modified token-passing protocol to transfer data at a 2.5-Mbit/s rate. It handles variable-length data packets, with 16-bit CRC generation and checking; it also performs all network protocol handling, and data buffering with an integral 2-Kbyte buffer. The controller is self-reconfiguring, so systems can be easily added or removed from the network. **General Automation,** 1045 S East St, PO Box 4883, Anaheim, CA 92803.



Circle 351

Digi-Data Series 2000
THE COOL STREAMER

Digi-Data Series 2000 streamers put the heat on the competition—and off the tape.

Unlike our competitors, whose streamers draw air over hot components before blowing it into the tape compartment, the Series 2000 keeps its cool by pulling air from outside the rack directly across the entire tape path. The cooling fan moves large amounts of cool air over the tape, keeping it below the easily exceeded ANSI limit of 90°F regardless of rack temperature. And by exhausting air outside of the rack, the streamer does not increase rack temperature.

This cool tape path is just one of the reliability features Digi-Data designed into the Series 2000. Solid state sensors and microprocessor controlled calibration and power-up diagnostics are standard. Step-write, microprocessor controlled read electronics and extended deskew buffer make 3200 bpi operation more reliable.

And Series 2000 performance matches its reliability. With speeds up to 125 ips for 1600 bpi and 62.5 ips for 3200 bpi, the streamer can back up 92M bytes on a single tape reel in under 10 minutes (including rewind). A unique adaptive streaming feature enables the Series 2000 to adjust its tape speed to match the data rate.

Series 2000 is just one of Digi-Data's full line of ½" and ¼" tape drives for streaming and conventional start/stop operation.

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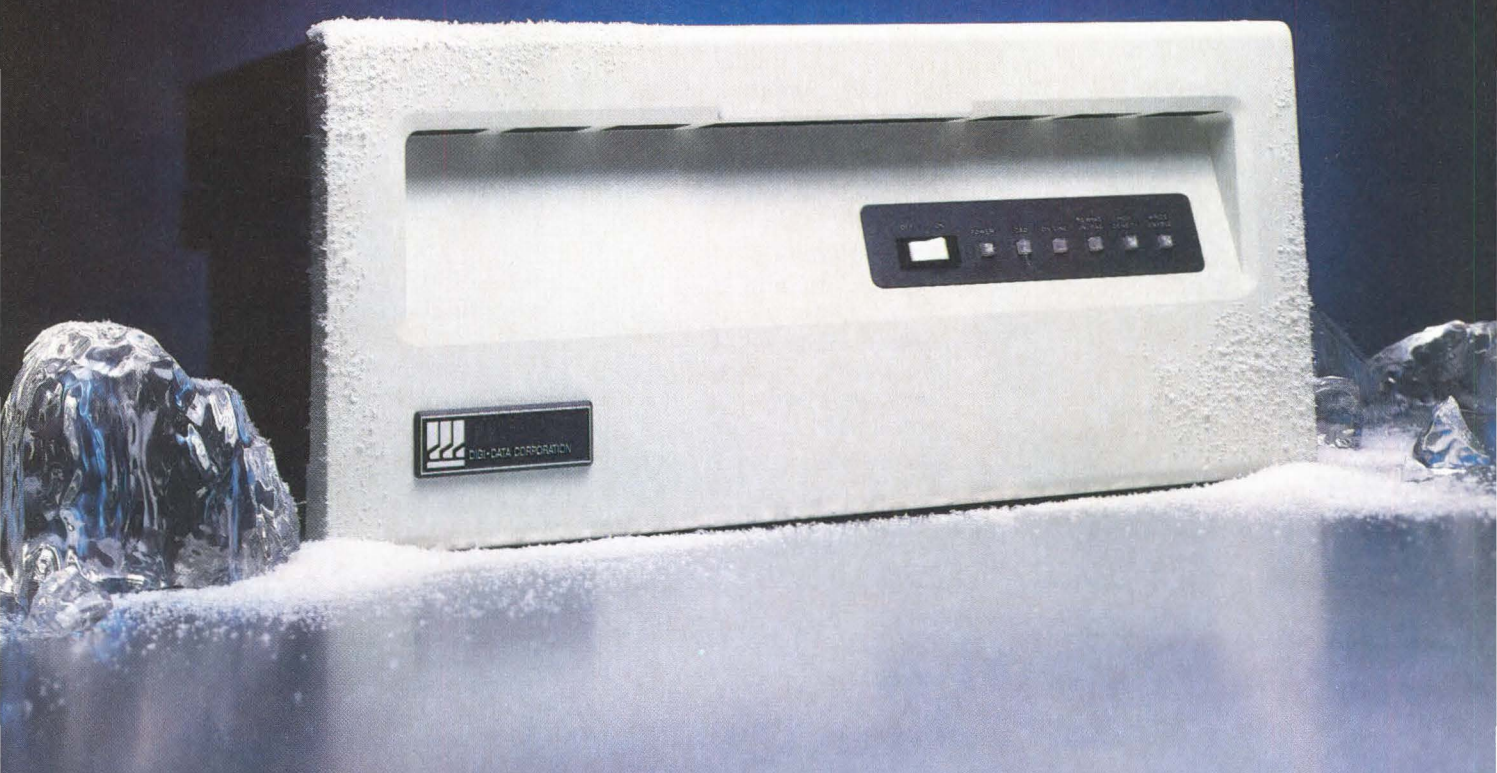
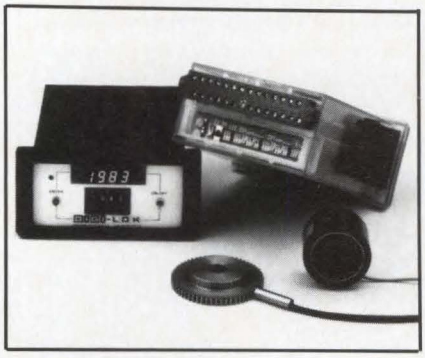


CIRCLE 161

Industrial controller

Linker 100 controls single intelligent peripherals from a central location. Featuring an intelligent display, keyboard, and CPU, it can be programmed to run any controller, printer, or simulator via full-duplex asynchronous serial I/OS. It includes a central onboard computer that communicates with two internal peripherals and the equipment under control. The 48 keys on the keyboard are software definable. Multiple processing permits Basic and machine language to function concurrently. Price is $400. **Analogic Corp,** 14 Electronics Ave, Danvers, MA 01923. **Circle 360**

Phase lock loop control



Fourth-generation Digi-lok servo controls offer micro-based (Intel 8748) phase lock loop with a 12-bit up/down count technique. This enhances setpoint resolution by minimizing bobble. Existing SCR controls and adjustable frequency drives can be regulated to 0.05 percent of set speed. Moreover, PC board-mounted bit switches can program process applications, including master four-channel frequency generation. The DLC100 is the 115-Vac input model; DLC200 is the 230-Vac model. Both controls sell for $565. **Minarik Electric Co,** Box 54210, Terminal Annex, Los Angeles, CA 90054. **Circle 361**

Data acquisition and control

The CompuDAS 3 acquires data, performs calculations, generates control signals, prints reports, and stores trend data. An 8086 combined with an 8087 arithmetic processor enhances realtime operation and allows memory expansion in 128-Kbyte increments to 768 Kbytes. Erasable PROM holds the compiler Basic, operating system, and special routines. Battery-powered RAM prevents data loss when power goes off. Battery-powered realtime clock ensures accurate timing. **Ithaco, Inc,** 735 W Clinton St, PO Box 6437, Ithaca, NY 14851. **Circle 362**

Seven-axis robot

A waist joint enables model 705S to position a six-axis arm within its 360 degree work envelope. Applications include mounting odd-shaped components on PC boards, handling silicon wafers, and assembling disk drives. The robot offers repeatability of ±0.0025 in. It consists of a robotic arm and end-effector (gripper), a control computer, and a separate auxiliary computer for end-effector control and monitoring of safety devices. Programmed with Robot Basic, the 705S uses three methods of programming in the robot offline. Cost is $60,000. **Intelledex, Inc,** 33840 Eastgate Circle, Corvallis, OR 97333.

Circle 363

Front end for controller

As an enhancement to programmable controllers, the Microtie 1200 provides data acquisition, floating point math, and host computer communications. The system expands to 27 ports handling multiple PC data highways, CRTs and printers of different manufacturers. Up to 1 Mbyte of memory stores messages and report formats, performing calculations and buffering data for reports or transfer to a host computer. All functions are configured with English language menus and prompts. The controller uses a realtime, multitasking operating system and 16-bit processors for high speed. **Automation Technology, Inc,** PO Box 91000, Mobile, AL 36691.

Circle 364

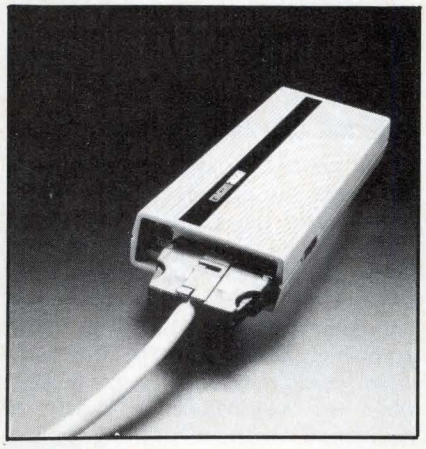
User-programmable motion system

Offering precise digital control of 14 axes, the C-1012 is programmable in Basic and assembly language. The package includes a complete development system with a menu-driven utility library, text editor, and erasable PROM programmer. Powered from a 120-Vac line, typical applications include performance testing, X-Y table control, and dimensional inspection of critical components. Speed ranges up to 10,000 rpm, and acceleration to 500,000 rad/s^2. Positioning is accurate to 0.01 degrees. The system operates standalone or in conjunction with a host or programmable controller. **Buckminster Corp,** 99 Highland Ave, Somerville, MA 02143.

Circle 365

Optical interconnect system

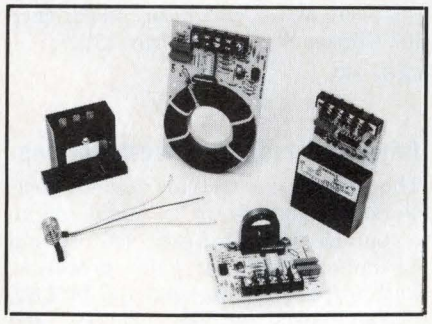
The 2000 interconnect transmits simultaneous data bidirectionally via single optical cables at speeds to 100 kbits/s. Benefits include immunity to electromagnetic and radio frequency interference, fast transmission rates, safety, data security, and low power requirements. Built-in logic automatically adjusts to device speed, detects line tapping, and allows use of advanced data encoding techniques. Packaged version costs $130 in 1000s, while the circuit board version is $100 in the same quantity. **Raycom Systems, Inc,** 6395 Gunpark Dr, Boulder, CO 80301.



Circle 366

Current sensors

The CS series is available with digital or linear output for either ac or dc. Thin-film and Hall effect technologies are used with the 0.5-A and the 5-A digital units, as well as 100-A devices having a magnetically sensitive thin-film nickel-iron alloy on a silicon IC. The TTL and MOS compatible digital output sensors indicate if current is flowing in a sensed circuit. Through-hole design electrically isolates the sensor to protect against damage from overcurrent or high voltage transients. **Micro Switch, a Honeywell Div,** 11 W Spring St, Freeport, IL 61032.



Circle 367

DEVELOPMENT SYSTEMS

Video graphics board set

Designed for 100-MHz video bandwidth color monitors, the 1024 set supports 1024- x 1024-pixel screen resolution. Multibus boards configure in four or eight video planes with programmable lookup tables. With the 7220 VLSI graphics processor, the boards write to eight video planes simultaneously in a single cycle. Drawing speed is 45,000 vectors/s. Software support includes a C subroutine library for 68000 Unix-based workstations and CP/M-86. Board set is priced at $3709. **Phoenix Computer Graphics, Inc,** PO Box 52667, Lafayette, LA 70505.

Circle 368

Program execution analyzer

The PXA is designed for the IBM PC/XT and IBM-compatible products. Functionally, it supplies the programmer with a nonintrusive window on code execution. The package consists of a single plug-in board and supporting software. It monitors 31 channels of bus information through an expansion connector. Users can gather, display, and analyze address and data information relating to stack operations, variable handling, and DMA access. The analyzer captures 512 events leading to and following the occurrence of a defined trigger qualifier. Cost is $750. **Micro Integrations Engineering Corp,** 11 Clearbrook Rd, Elmsford, NY 10523.

Circle 369

Workstation for CAD/CAM

The PW150 has a 19-in. color display that uses a high speed multiplane graphics processor. Initially, it will support Medusa CAD software, which features three-dimensional solid modeling. A remote expansion cabinet with a single power supply supports eight processors. The cabinet can be 328 ft from the host and each workstation can be 328 ft from the cabinet. Features include realtime pan and zoom using the function keys and joystick. The workstation can magnify images, in increments, up to 16 times. A single CRT is used for both graphics and commands. Price is $25,000. **Prime Computer, Inc,** Prime Park, Natick, MA 01760.

Circle 370

Ergonomic workstation

The ICEM includes 1280- x 1024-pixel color graphics with 60-Hz noninterlaced refresh, a separate alphanumeric display, keyboard, and data tablet. All units are compatible and provide a 3-D display file with 512 to 2000 Kbytes of RAM. The file features a 500-kbaud host interface to a Cyber 170 mainframe and displays up to 200,000 transformed vectors/s. The workstation displays 16 to 4096 colors simultaneously. Ergonomic features are an adjustable table; display head with height, tilt, and swivel adjustments; and a removable hood for controlling glare. Prices start at $30,000. **Control Data Corp,** PO Box 0, Minneapolis, MN 55440. **Circle 371**

Ethernet CAD/CAM systems

Expert 1000 and 2000 systems are based on the Xerox 8000 network, the 8010 workstation, and the Ethernet LAN. Each allows users to create, process, file, edit, print, and distribute information electronically. The workstation has a high resoultion black and white display with keyboard and mouse. The 1000 automates the entire PC board design process, while the 2000 handles a variety of mechanical design and drafting applications. Standalone workstation configurations start at under $30,000. **Versatec, a Xerox Co,** 2710 Walsh Ave, Santa Clara, CA 95051.

Circle 372

Software development

The VME 9100 includes a 10-Mbyte 5¼-in. Winchester disk for developing software for VME-based systems. The single-user system is based on CP/M-68-K, which is written for the 68000. File system supports up to 32 Mbytes per file. Hardware includes an eight-slot motherboard, system controller, 68000 CPU, 128-Kbyte RAM, and quad serial port module. Programming tools are assembler, linker, C compiler, and C processor. **Mizar Inc,** 302 Chester St, St Paul, MN 55107.

Circle 373

Advanced technical workstations

The Sun-2 family features local area network communication as standard, an ergonomic design for user comfort, and an optional floating point processor. Each workstation provides a 32-bit CPU, demand-paged virtual memory, and high resolution bit-mapped graphics display. LAN hardware and software allow resource sharing among clusters. Each workstation uses a Multibus backplane with 9 or 15 slots, depending on the model. Memory management design supports up to 4 Mbytes of memory with no wait states, so main memory is as fast as cache. A standard configuration is priced at $16,900. **Sun Microsystems, Inc,** 2550 Garcia Ave, Mountain View, CA 94043.

Circle 374

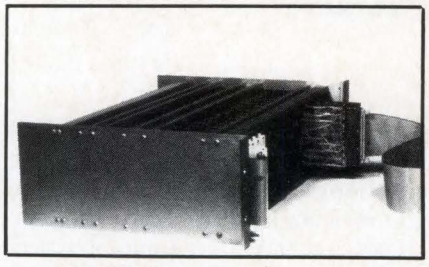
Graphics display controller

The STD-800 provides 512- x 512-pixel resolution with 16 colors on a single STD bus board. It uses a GDC 7220 VLSI graphics controller chip for hardware vector and circle generation, high speed character drawing, DMA, and split-screen smooth scroll and pan. The card also features a complete onboard 4096-color lookup table and lightpen interface. Either interlaced or noninterlaced operation can be selected. Price is $995. **Matrox Electronic Systems Ltd,** 5800 Andover Ave, Montreal, Quebec, Canada H4T 1H4.

Circle 375

INTERCONNECTION & PACKAGING

High speed packaging



The Metric series is a modular system based on the DIN/Eurocard format. Each board size comes in one of three families for conventional TTL circuit packaging, high speed Schottky, and ultrafast 10-K and 100-K ECL devices. All boards interconnect via stitch-wire, insulation displacement wiring, or wirewrap. ICs plug into precision-machined individual socket pins with four-leaf internal contact. **Interconnection Technology, Inc,** 5542 Buckingham Dr, Huntington Beach, CA 92649.

Circle 376

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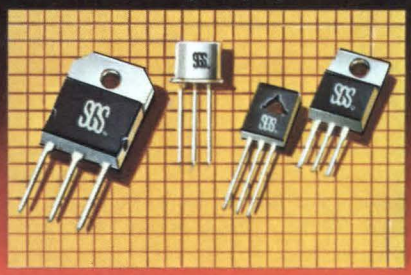

Sales Offices: Atlanta, GA (404) 446-8686; Boston, MA (617) 890-6688; Chicago, IL (312) 490-1890; Dallas, TX (214) 733-1515; Indianapolis, IN (317) 241-1116; Irvine, CA (714) 863-1222; Long Island, NY (516) 435-1050; Los Angeles, CA (213) 716-6600; Phoenix, AZ (602) 867-6100; San Francisco, CA (408) 727-3404; Sao Paulo, Brazil (11) 647-245.

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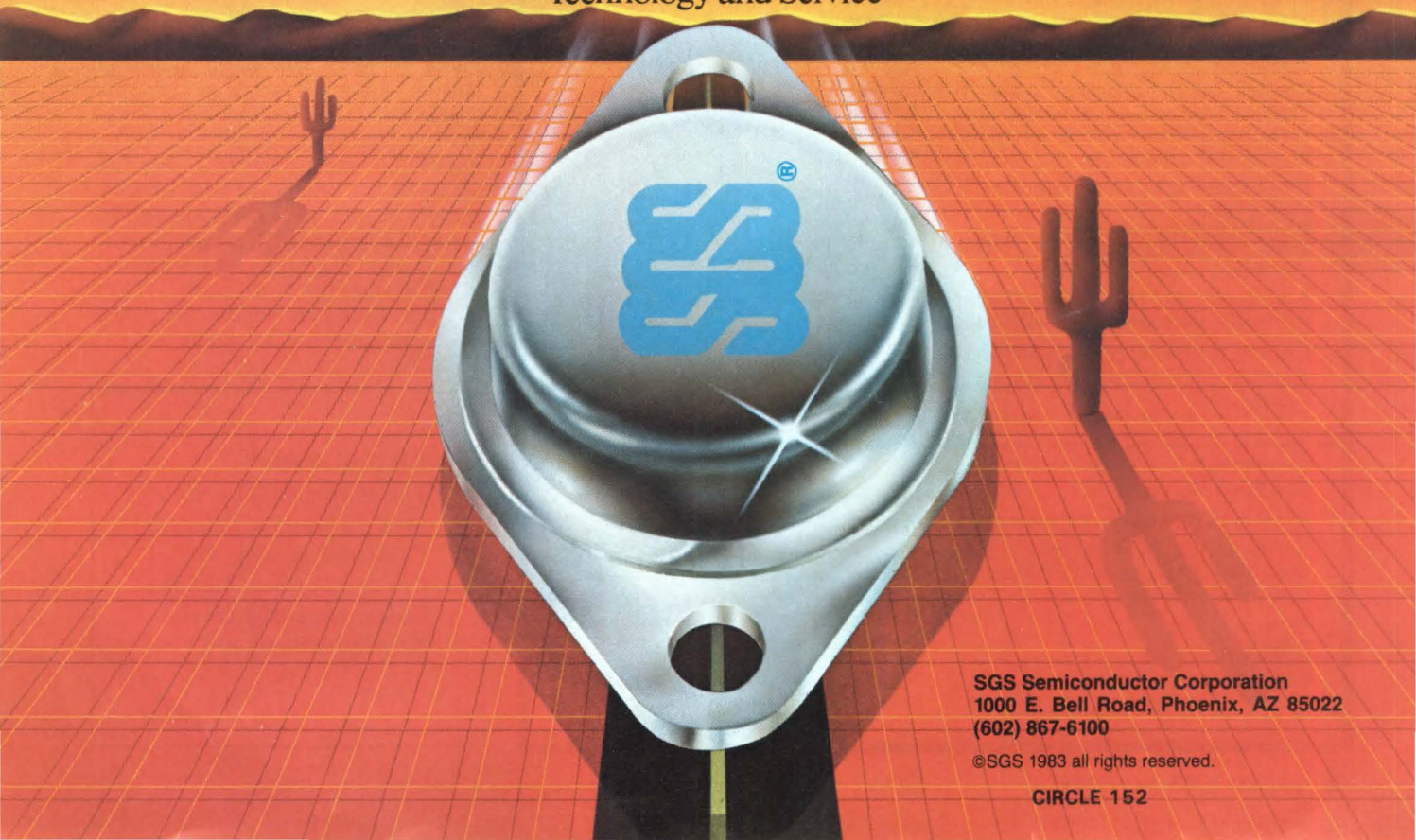


SGS Semiconductor Corporation
1000 E. Bell Road, Phoenix, AZ 85022
(602) 867-6100

CIRCLE 152

Data cables

Designed to connect a host computer to peripherals, the Data Spec cables are fully shielded 25 conductor cables with 25-pin D subminiature (RS-232) connectors. The cables have twenty-five 20 AWG twisted wires, and shields with flexible aluminum shields covered with a 2-mm PVC sleeve. They are available in lengths of 3, 5, 10, and 25 ft with a 25-pin D male plug on both ends, or a 25-pin D male on one side and female on the other. **Ora Electronics,** 18215 Parthenia St, Northridge, CA 91325.

Circle 377

Clip-on heat sinks

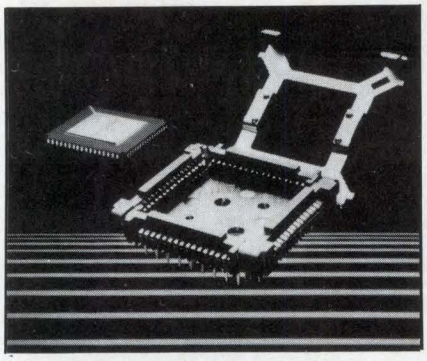
Cooling devices fit TO-202 and TO-220 plastic power semiconductor devices. The 5742 and 5942 series come in three styles, with a fin on the right side, the left side, or both sides. With an input of 2 W, the dual-fin heat sinks have a 37 °C rise above ambient. The aluminum-alloy devices are available in black anodize or gold chromate finish and install after the final PC board is assembled. Pricing for the 5742B (without tabs) is $0.115 in 1000s. **Aaall, Inc,** 161 Morrill St, Gilford, NH 03246. **Circle 378**

Socket assemblies

Designed to meet MIL-S-83734, series SO-M accommodates 8 through 40 flat lead DIP ICs or round leads for high retention. The two-piece screw machined contact consists of a four-leaf BeCu inner contact and mechanical outer sleeve designed to accept short IC leads. Closed construction of the outer sleeve eliminates solder or flux wicking problems. Assemblies are packaged in tubes compatible with automatic insertions. Insulating material consists of thermoplastic polyester, UL rated 94 VO. **Precicontact, Inc,** 1150 Wheeler Way, PO Box 798, Langhorne, PA 19047.

Circle 379

Low profile connectors



Mounting to PC boards with holes on a 0.100-in. grid, 44- through 100-position receptacles accept ceramic LCCs. Polarizing features ensure proper package to socket registration and socket to PC board polarization for each receptacle. A spring-loaded hold-down frame secures the package and latches to exert contact normal force on the metallized pads of the ceramic package. The connectors come JEDEC type A, B, and D, with electrical specs of 0.4 x 10^8 MΩ, capacitance of 0.5 pF, and mutual inductance of 3 nH. **AMP Inc,** Harrisburg, PA 17105.

Circle 380

Socket/carrier system

The RN system consists of a PRC carrier to hold an IC, and a PRM socket soldered into a PC board. The carrier is inserted into the socket and, when an IC must be changed in the field, the new IC is placed in the protective carrier and shipped for installation. Both socket and carrier are polarized so ICs cannot be inserted incorrectly. The socket has BeCu contacts for gastight performance. It is available with 8 to 28 pins. The 24-pin socket is $0.517 in 1000s, while the 24-pin carrier is $0.08 in 1000s. **Robinson Nugent, Inc,** 800 E 8th St, New Albany, IN 47150.

Circle 381

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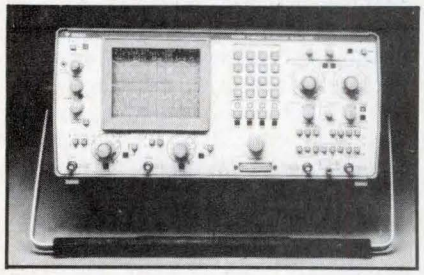
Digital storage scope

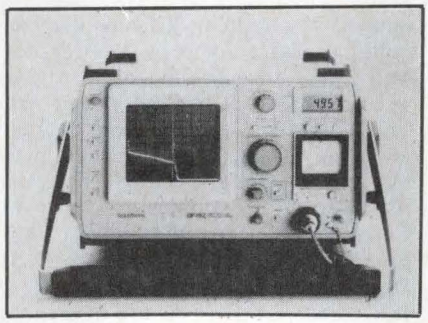


Addressing both repetitive and transient waveform capture applications, the 100-MHz 5110 scope operates in either nonstorage or storage mode. The intelligent dual-trace device acquires and displays two waveforms simultaneously. An IEEE 488 interface allows programming applications under controller or computer operation for offline waveform processing. The scope provides an 8-bit digitizer for better than 0.4-percent vertical resolution and two 1-Kbyte memories. Price is $12,900. **Gould Inc, Design & Test Systems Div,** 4600 Old Ironsides Dr, Santa Clara, CA 95050.

Circle 382

Fiber optic reflectometer

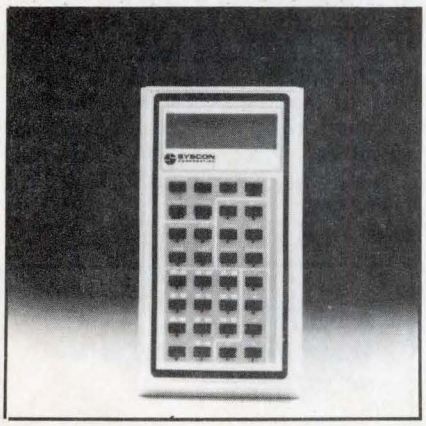
Operating at 1300 nm, the OF152 locates faults and breaks, and measures splice loss in multimode fiber links. The time domain reflectometer makes repeatable, quantitative, calibrated loss and distance measurements, providing at-a-glance answers on a CRT and an instant view of fiber length. It typically measures breaks through a maximum 35-dB cable loss, and splices to ±0.1 dB through a 12.5-dB one-way cable loss. Price is $19,500. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.



Circle 384

Data-gathering terminal

The Versaterm can be programmed to record data for lab experiments, monitor industrial processes, and schedule. Data can be loaded and unloaded from a variety of host computers through a special interface. Automatic parameters program the handheld terminal to call out operator errors. The unit feeds data directly into a computer without keypunch operations. Features include 32 keys (64 functions), two-line, 32-character LED display, and a CMOS micro and memory. Unit sells for $3000. **Syscon Corp,** 3990 Sherman St, San Diego, CA 92110.



Circle 383

SOFTWARE

Natural language option

The conversational language inquiry option (CLIO) is designed for use with the R:base series 4000, a relational DBMS for small computers. It allows the user to build a synonym dictionary for words or operations associated with the data base. The software can search through the data base to retrieve records based on adjectives or qualifying terms. The option can simultaneously make inquiries into five files from among the 40 available concurrently in R:base. Interface will sell for less than $200, while R:base is $495. **Microrim, Inc,** 1750 112th Ave NE, Bellevue, WA 98004.

Circle 385

Pascal validation

The Pascal Validation Suite consists of 734 test programs that systematically exercise a Pascal compiler to determine its ability to process programs written in ISO standard Pascal. The Standard Pascal Model Implementation includes both a compiler and an interpreter, which together process the validation suite tests. A static checker audits Pascal programs for conformity to the ISO standard. The PVS and SPMI are available in machine readable source code for $450 each. **Software Consulting Services,** Ben Franklin Technology Center 125, Murray H. Goodman Campus, Lehigh University, Bethlehem, PA 18015.

Circle 386

Dasher emulator for IBM PC

Consisting of 100 percent assembly language software that bypasses DOS and BIOS calls, EMU achieves true 9600-baud terminal emulation. Designed for direct connect applications, it can also be used in remote and dial-up systems. The software transfers data to and from any PC-DOS file and onto a different disk through a subdirectory structure. Software is distributed on a noncopy protected diskette. Binary license is $95 and the source code is available for modifications. **Rhintek, Inc, Computer Engineering,** PO Box 220, Columbia, MD 21045.

Circle 387

Universal cross assembler

The MOPI software development package allows users to define their own set of instructions. It can generate the machine code for any 8-bit micro. Types of instructions are definable, assembly language, and macro. It converts macro-type instructions into calling sequences to relocatable subroutines that perform the desired function. Required locatable load modules are automatically appended to the program, producing an executable object file. Software license is $150 plus options. **Voice Operated Computer Systems,** PO Box 3705, Minneapolis, MN 55405.
Circle 388

Graphics software

The Frame Editor is used with the PLP200 color graphics terminal, while the software runs on the IBM PC-XT, VAX, and Plexus. For use with a digitizing pad or mouse, the software allows nonprogrammers to interactively create free-form graphic designs. The designs use squares, circles, rectangles, and other forms in 16 colors, selected from a palette of 4096 colors. Prices range from $500 to $2000, depending on the host computer. **Verticom Inc,** 545 Weddell Dr, Sunnyvale, CA 94089. **Circle 389**

Interpretive computer language

With minimal programming, an interpretive language allows sophisticated analysis of physiological systems and signals. The NEXUS interpreter runs automated, or interactively when a high degree of control over the stages of analysis is required. Versions are currently available for VMS, DEC Professional, and TSX. The language requires at least 28 Kwords of memory and 3000 blocks of mass storage. Basic package performs plotting, signal analysis, nonparametric linear system analysis, filtering, and utility operations. **MEDNET Computer Service, Biomedical Engineering Unit,** McGill University, 3655 Drummond St, Montreal, Canada, H3G 1Y6. **Circle 390**

Cross assembler in C

Software designed for the NS16000 turns the IBM PC into a system capable of developing programs for 32-bit computers. Written in C, the package consists of four utility programs: a cross assembler, cross linker, debugger, and librarian. Features include macro capabilities, floating piont and memory management units with support. The system requires two 360-Kbyte drives, 192 Kbytes of memory, and DOS 2.0. The entire package, including manual and all four programs, sells for $595. **Program Concepts, Inc,** PO Box 8164, Charlottesville, VA 22901.
Circle 391

Extendable Basic

Direct addressing of a 1-Mbyte memory is only part of Megabasic's capabilities. Users can also load libraries, subroutines, and functions into memory that can execute from the running program with a single statement. The software gives users of MS-DOS and CP/M-86 operating systems full use of a micro. Other features include variable names to 255 characters, trace and edit functions for debugging, and BCD arithmetic to eliminate rounding errors. The software comes with complete documentation. **American Planning Corp,** 4600 Duke St, Alexandria, VA 22304.
Circle 392

Forth software

A text formatting program, FMS is patterned after ms of Unix. Present editor can be used to prepare source text. In typewriter mode, text is printed as it is typed. Price is $150. FWG is designed for creating Forth code to place in EPROMs of dedicated computers and therefore can provide Forth development. Price is $50. FLH is a Forth extension containing words equivalent to the list handling functions of Lisp. Symbol generation allows automatic creation of new list names and variables. Price is $50. **Innovatia Laboratories,** 5275 Crown St, West Linn, OR 97068.
Circle 393

April Preview
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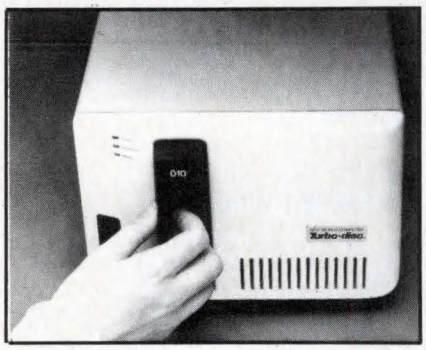
Winchester disk drive



The Turbo-Disc has 12 read/write heads on each side. Its head slider assembly mounts on a parallelogram, which moves the heads across a rotating media surface in 1/12th the time of a normal, single-head drive. The 5¼-in. drive uses a 10-Mbyte configuration (5 fixed/5 removable) and maintains 425,000 characters of data under 48 heads at all times. Access time is 8 ms for data under the heads and 16 ms average. With a standard ST506/412 interface, the drive is available in three versions. Prices range from $1800 to $4950. **New World Computer Co, Inc,** 6624 Owens Dr, PO Box 1479, Pleasanton, CA 94566.

Circle 394

Winchesters with 14-in. capacities

Intended for use in multi-user, multitasking computer systems, models 806, 807, and 808 offer 188, 300, and 500 Mbytes of storage, respectively, in the standard 8-in. form factor. Each drive uses six disks with 20,160 to 30,240 bytes of track capacity. Average seek times range from 20 to 25 ms. Features include automatic carriage and spindle locks that protect the drives during power-off conditions, and automatic head retraction into a dedicated head landing/shipping zone. Prices range from $3095 to $4150. **Priam Corp,** 20 W Montague Expy, San Jose, CA 95134.

Circle 395

Memory expander

Specifically for the DEC Falcon SBC-11/21, the FMX-11 extends the Falcon's onboard capacity to 60 Kbytes. It also adds batter support for CMOS static RAMs and provides a CMOS calendar clock and power failure-detection logic with battery backup. The expander supplies address, data, and control signals at onboard memory cycle speeds so programs execute quickly without wait states. A PROM address decoder allows the system integrator to link any combination of 2-, 4-, and 8-Kbyte memory chips. The dual-width Q-bus board is available in two versions. Cost is $700. **Infosphere, Inc,** 4730 SW Macadam Ave, Portland, OR 97201.

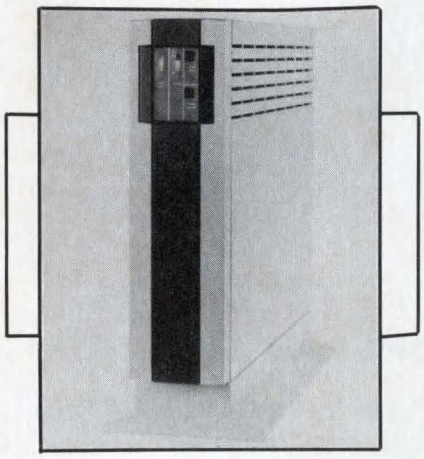
Circle 396

Static RAM board

Loaded with 2-Kbyte x 8-bit 6116 RAMs, the 8800GR17 is an IEEE 696/S-100, 64-Kbyte RAM board. It provides less than 150-ns access times and allows operation with 10-MHz 8088 or 8086 micros. A switch-selectable address line configuration allows either extended addressing for 16-Mbyte memories or 16-bit addressing for 64-Kbyte memories. DIP switches allow the enabling and disability of any 16-Kbyte block or any 2-Kbyte block at E000, E800, F000, and F800 (for memory-mapped systems). Price is $450. **Vector Electronic Co, Inc,** 12460 Gladstone Ave, Sylmar, CA 91342.

Circle 397

Disk storage system



The VIP/X has a capacity of 760 Mbytes with an architecture that uses multiple disk actuators. These actuators are controlled by several micros with 512 Kbytes of onboard multiported cache. Average access time is less than 10 ms. The subsystem can access any host; initial shipments will offer host adapters for the VAX-11 and PDP-11 families that are protocol compatible. Price, including the host adapter, is $23,995. **U.S. Design Corp,** 5100 Philadelphia Way, Lanham, MD 20706.

Circle 398

Built-in controllers

Three miniature reel-to-reel tape drives feature intelligent controllers. The 510i, 520i, and 540i are used for backing up 5¼-in. Winchester disk drives and include either SCSI or QIC-02 compatible controller. They offer 10, 20, and 40 Mbytes of formatted capacity, respectively, in the streaming mode. The recording medium is a removable 450-ft x 0.15-in. high density four-track digital cassette. Drives are set for 30 or 90 in./s and provide transfer rates of 24 to 112.5 Kbytes/s depending on the unit. Prices start at $350. **Memtec,** Keewaydin Dr, Salem, NH 03079.

Circle 399

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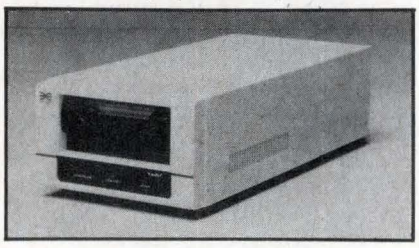
Streaming tape subsystem



This 1/4-in. cartridge system provides enhanced storage and backup capabilities to DEC LSI, PDP, and VAX-11 computers. The Vault consists of Control Data's Sentinel streamer and the TC05 Q-bus of TC15 Unibus tape coupler. Transparent operation emulates all functions of the TS11 1/2-in. tape subsystem. At up to 50 Mbytes formatted capacity, depending on block size, a single cartridge provides backup equal to most 5¼-in. Winchesters. Price is $3975. **Emulex Corp,** PO Box 6725, 3545 Harbor Blvd, Costa Mesa, CA 92626.

Circle 404

Bubble memory cassette

One-Mbit MBS-2011C offers lower access times and lower error rates after correction than floppy disk systems. Bubble media exhibits longer lifetime and smaller physical volume. In addition, it provides better behavior in harsh environments. Standard parallel 8-bit microprocessor interface is available. Applications include portable terminals, robotics, instruments, and personal computers. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.

Circle 401

Microfloppy disk drive

This double-sided drive stores 1 Mbyte on standard 3½-in. media. The 350 operates with the ANSI working standard 3½-in. hard shell cartridge media format. It provides a 6 ms track-to-track access time and 80 tracks/side. Using a straddle erase head, it supports the 10 x 512-byte sector format yielding 409.6 Kbytes/side (formatted). Specifications include 250-kbit/s transfer rate and MTBF is 10,000 power-on hours. In quantity, cost is under $200. **Shugart Corp,** 475 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 402

Half-height Winchester

The HH-506 5-Mbyte drive stands 1.6 x 5.75- x 8 in. and weighs 3 lb. It uses 15 W with a dc voltage requirement of 12 V ±5 percent at 0.9 A typical, and 1.8 A start and 5 V ±5 percent at 0.85 A. Track-to-track access time is 3 ms with average access time of 85 ms. Data transfer rate is 5 Mbits/s with an average latency of 8.45 ms. Track density equals 648 tracks/in. and recording density is 9680 bits/in. Price is $400 in quantity. **Microscience International,** 575 E Middlefield Rd, Mountain View, CA 94043.

Circle 403

Streaming tape drive

The D5160 1/2-in. drive offers 40-, 80-, or 160-Mbyte tape reels operating in a package that mounts in the same space as a standard 5¼-in.drive. It supports the basic 1/4-in. tape drive, QIC-02, and SCSI interface standards. Applications include Winchester backup, file restructuring, and online memory expansion. The drive supports either 90- or 130-in./s tape speeds allowing transfer rates of 90 or 130 kbytes, respectively. MTBF is 5000 h with MTTR less than 30 min. Volume pricing is $750. **Rosscomp Corp,** 16643 Valley View Ave, Cerritos, CA 90701.

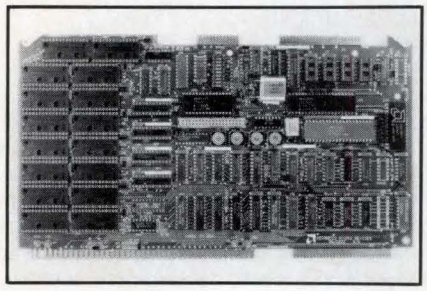
Circle 400

Compatible VMEbus RAM

The IV-1611 dynamic RAM board offers 2-Mbyte capacity using 256-Kbyte RAM chips. Features include byte parity checking, 32-bit transfer capability, supervisor-only access mode, and on-board interleave. Read access time is typically 210 ns, with 250 ns maximum. Write access time is 140 ns typical; 180 ns maximum. Board's cycle time is 35 ns for sequential access, allowing block transfers at up to 4 MHz. Board cycle time is 330 ns for nonconsecutive addresses with two unchanged LSBs. In quantity one to four, the board costs $1795. **Ironics Inc,** 117 Eastern Heights Dr, PO Box 356, Ithaca, NY 14850.

Circle 405

Programmable memory and I/O



The Multibus compatible Am96/5232 has sockets for 256 Kbytes of EPROM, 128 Kbytes of static RAM, or 32 Kbytes of EEPROM. The board's I/O portion includes RS-232-C serial port, parallel interface with 24 lines, counter/timers, programmable interrupt controller, and SBX connector. It can support 8- and 16-bit micros by providing 20- and 24-bit addressing, 8- and 16-bit memory data, and 8- and 16-bit I/O addresses. In quantities of one to nine, the board costs $895. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.

Circle 406

Optical storage disk

Glass based, 12-in. DC 301 stores 1.5 Gbytes (or 46,000 pages) when both sides are used. Track density is 16,000 tracks/in. and recording density is 19,500 tracks/in. The disk achieves a low bit error rate equivalent to that of magnetic disks. It comes in a protective case that slides open when the disk enters a front-loading drive. The disk can be used with Hitfile 60—an optical disk storage system designed for document filing and mainframe linkup. Price is $200 for a one-sided disk and $300 for double-sided. **Maxell Corp of America, Computer Products Div,** 60 Oxford Dr, Moonachie, NJ 07074.

Circle 407

Drives with closed-loop technology

Flexible 5¼-in. disk drives triple the capacity of current 96-track/in. floppies. Model 1722 provides accurate ontrack performance through closed-loop positioning. Unformatted capacity is 3.2 Mbytes at 170 tracks/in. Both 48- and 96-track/in. floppies can be read by the drive. Track-to-track access time is 3 ms and MTBF is 800 h. Average access time is 88 ms, and the floppy is plug-compatible with 8-in. floppy controllers using an ST 850 interface. Drive eliminates the need for backup-only devices by featuring both backup and program load capabilities. Price is $500. **MPI, sub of CTS Corp,** 9754 Deering Ave, Chatsworth, CA 91311.

Circle 408

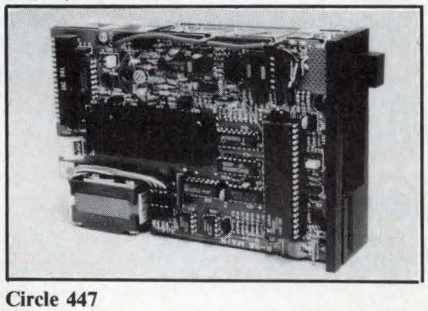
Winchester 5¼-in. drives

The 3075 and 3065 deliver 75 and 65 Mbytes of unformatted storage, respectively. Both feature 24-ms average access time and MTBF of 18,000 power-on hours. The 3075 uses five platters and eight heads for its storage, while the 3065 uses four platters and seven heads. Drives use a closed-loop servo system and a voice coil linear actuator for rapid access to data and higher density. Both use the industry standard ST412 interface. The 3075 is $1950; the 3065 is $1800. **Atasi Corp,** 2075 Zanker Rd, San Jose, CA 95131.

Circle 409

Battery-powered floppy drives

The SMD-100 series features storage capacities ranging from 125 Kbytes to 1 Mbyte. Data transfer rate is 125 kbits/s for single-density versions, and 250 kbits/s for double density. The 3.5-in. drives were designed for use in battery-powered micro products. Power consumption is 0.05 W for standby and 3.3 W for read/write. Track-to-track access times range from 3 to 6 ms. While average access times range from 96 to 97 ms. Track densities range from 67.5 to 135 tracks/in. **Epson America, Inc, OEM Products Div,** 3415 Kashiwa St, Torrance, CA 90505.



Circle 447

Cartridge tape drive

With a 130-Mbyte capacity, the STR-Stream II drive offers both start/stop and streaming modes. Streaming capacity is 130 Mbytes formatted and start/stop is 83 Mbytes. The unit streams at 75 in./s, runs start/stop at 50 in./s, and search/rewinds at 150 in./s. Data transfer rate is 225 kbytes/s in the streaming mode. The 1/2-in. drive has a 5¼-in. form factor with MTBF of 15,000 power-on hours and MTTR of less than 30 min. In 10,000s, price is less than $1000. **Electronic Processors, Inc,** 1265 W Dartmouth Ave, PO Box 569, Englewood, CO 80110.

Circle 448

High performance Winchester

The CM7000 series has unformatted capacities that range from 60 to 80 Mbytes. Drives have a rated MTBF of 12,000 hours with a MTTR of 30 min. Average access times are 40 ms. Increased encoder density enables data to be written with a track density of 1173 tracks/in. Head-position accuracy is ensured through a closed-loop servo system with a head parking zone, head locking mechanism, and onboard micro. Units require 5 V at 1 A maximum and 12 V at 3.5 A maximum during seeks and 1 A on track. **Computer Memories Inc,** 9216 Eton Ave, Chatsworth, CA 91311.

Circle 449

Microfloppy compatible drive

A 5¼-in. plug-compatible version of the 3½-in. drive can replace standard minifloppy drives without interfacing problems. Data transfer rate is 250 kbits/s double density. Storage capacities range from 500 Kbytes to 1 Mbyte. The drive measures approximately one-quarter the size and one-half the weight of conventional 5¼-in. drives and uses about 50-percent less power. A semirigid cartridge-type housing encases the disk for protection. **Sony Data Products,** Sony Dr, Park Ridge, NJ 07656.

Circle 450

Winchester disk subsystem

The Whams 1-XT upgrades the IBM PC to the storage capacity of the IBM XT and uses the PC's power supply. The 10-Mbyte system provides a half-height drive, an IBM-compatible RS-232 port, drive connector cable, and the option to add 256 Kbytes of memory. The board fits into the PC's second floppy disk slot and requires only two cable connections. All necessary software, logic, interfacing, and controller functions are embedded in the card. Price without RAM is $2375. **PIICEON, Inc,** 2045 Lundy Ave, San Jose, CA 95131.

Circle 451

Expanded diskette family

The HD 600 is a high density magnetic recording diskette that stores 3.3 Mbytes of unformatted data on a single 5¼-in. diskette. It offers a coercivity of 600 oersteds. Technology is based on a proprietary chemical process producing smaller, more uniform magnetic particles. These particles are egg-shaped (instead of resembling microscopic needles) and exhibit complete isotrophy so they can be magnetized equally well in any direction. **Eastman Kodak Co,** 343 State St, Rochester, NY 14650.

Circle 452

Dynamic memory module

Fully Multibus compatible, the MCB-2X provides onboard ECC. Using industry standard 64- or 256-Kbyte RAMs provides fast memory response—370-ns read access. All single-bit errors are continuously scrubbed during refresh cycles without system interruption. With address mapping the board can start on any 4-Kbyte boundary and occupy a continuous 512-or 2048-Kbyte memory space within a 16-Mbyte range. Users can dynamically relocate one or several memory blocks to a 64- or 256-Kbyte boundary within this range (under software control). Prices range from $2040 to $6995. **Intersil Systems, sub of General Electric,** 1275 Hammerwood Ave, Sunnyvale, CA 94086.

Circle 453

Winchester with 83 Mbytes

The 5¼-in. drive offers an average seek time of 25 ms, including settling. The 1305 supports the ST506/412 interface and has noise levels below 51 dBa. A balanced rotary voice coil positioner provides immunity from vibration during operation. Other standard features include automatic positioner lock, disk brake, head retraction to a free landing zone, and adjustment-free electronic system. Volume pricing is $1635. **Micropolis Corp,** 21329 Nordhoff St, Chatsworth, CA 91311.

Circle 454

Flexible disk cartridge drives

Combining density and access speed of rigid files with low cost and removability of floppies, this 5¼-in. drive is based on the principles of fluid dynamics. A circular plate controls airflow around the cartridge. As the disk spins at a high speed, the air envelopes the media and lifts it to within 10 μin. of the recording head; this prevents hard contact between head and media. It holds about 5.2 Mbytes of formatted storage with 424 tracks/square in. **Iomega Corp,** 4646 S 1500 West, Ogden, UT 84403.

Circle 455

Eight inch Winchester

The M2333 offers 337 Mbytes of unformatted storage in a 5- x 8.5- x 15-in. package. Average positioning time is 20 ms, and an SMD-plus interface transfers data at 2.4 Mbits/s. An optional rackmount kit allows installation of two side by side drives in a standard 19-in. rack, providing 674 Mbytes of storage. The drive is priced at $5500 in 100-piece quantities. **Fujitsu America, Inc, Storage and Peripheral Products Group,** 3075 Oakmead Village Dr, Santa Clara, CA 95051.

Circle 456

MICROPROCESSORS/ MICROCOMPUTERS

Compatible CP/M microcomputer

Based on the 6-MHz Z80B micro, the Quark/100 uses programmable array logic and gate array technology. An on-card 80-column video display interface supports 50- and 60-Hz frame rates and operates in both alphanumeric and bit-mapped graphic modes. Direct-drive and composite video outputs, as well as inputs for wired-only keyboards, connect the board to standard CRTs and keyboards. Interface capacity includes floppy disk interface for both 5¼- and 8-in. drives, two RS-232-C ports, and parallel printer port. Cost is $995. **Megatel Computer Corp, Inc,** 150 Turbine Dr, Weston, Ontario, Canada M9L 2S2.

Circle 457

Microcomputer module

The compact desktop WY-1000 uses the 80186 16-bit micro. System is configured with a smart editing alphanumeric terminal, two 5¼-in. floppies, 128 Kbytes of RAM, and three I/O ports. Options include high resolution graphics that operate with a monochrome or color terminal. Monochrome resolution is 800 x 338, while color is 800 x 286 in 16 simultaneous colors. Graphics display option provides two additional RS-232-C ports. The module is offered with MS-DOS. **Wyse Technology,** 3040 N First St, San Jose, CA 95134. **Circle 458**

Micro with EEPROM and conversion

The 8-bit HCMOS MC68HC11 achieves a 2-MHz nominal bus rate and has 4 Kbytes of ROM, 512 bytes of EEPROM, and 256 bytes of RAM. All RAM is saved during standby. The time system includes three input captures and five output compares. Serial interfacing consists of an enhanced NRZ system plus a serial peripheral interface. The micro also includes an 8-channel A-D converter, an 8-bit pulse accumulator circuit, a real-time interrupt circuit, and a watchdog system. Two packages are available: 52-pin quad surface mount plastic and 48-pin DIP. In 1000s, price is $19. **Motorola Inc, MOS Integrated Circuits Group,** 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 459

Single-chip 4-bit micros

The HMCS402AC/404AC are 5-V devices executing instructions at 1.33 μs each. The 402AC uses 2048 words of ROM and 160 nibbles of RAM, while the 404AC uses 4096 words of ROM and 256 nibbles of RAM. Both chips have binary and BCD calculation functions and a direct addressing mode. Of the 99 instructions, 76 consist of one-word for programming efficiency. Each has a serial communication interface, 32 standard I/O lines, 26 high voltage output lines, and two 8-bit timer/counters. **Hitachi America, Ltd,** 1800 Bering Dr, San Jose, CA 95112.

Circle 460

Board-level CPU with management

Implementing the 68010 virtual memory processor with four memory management units, the OB68K/MMU is specifically for large memory-managed computer systems. The board has full address and bus arbitration for single- and multiprocessor systems and is compatible with a range of IEEE 796 products. The MMU equips the operating system to allocate, control, and protect system memory over the entire 16-Mbyte, 24-bit addressing range. In addition to onboard memory, the board features two RS-232 ports—one to accept a standard terminal and another to download from a host. **Omnibyte Corp,** 245 W Roosevelt Rd, Chicago, IL 60185.

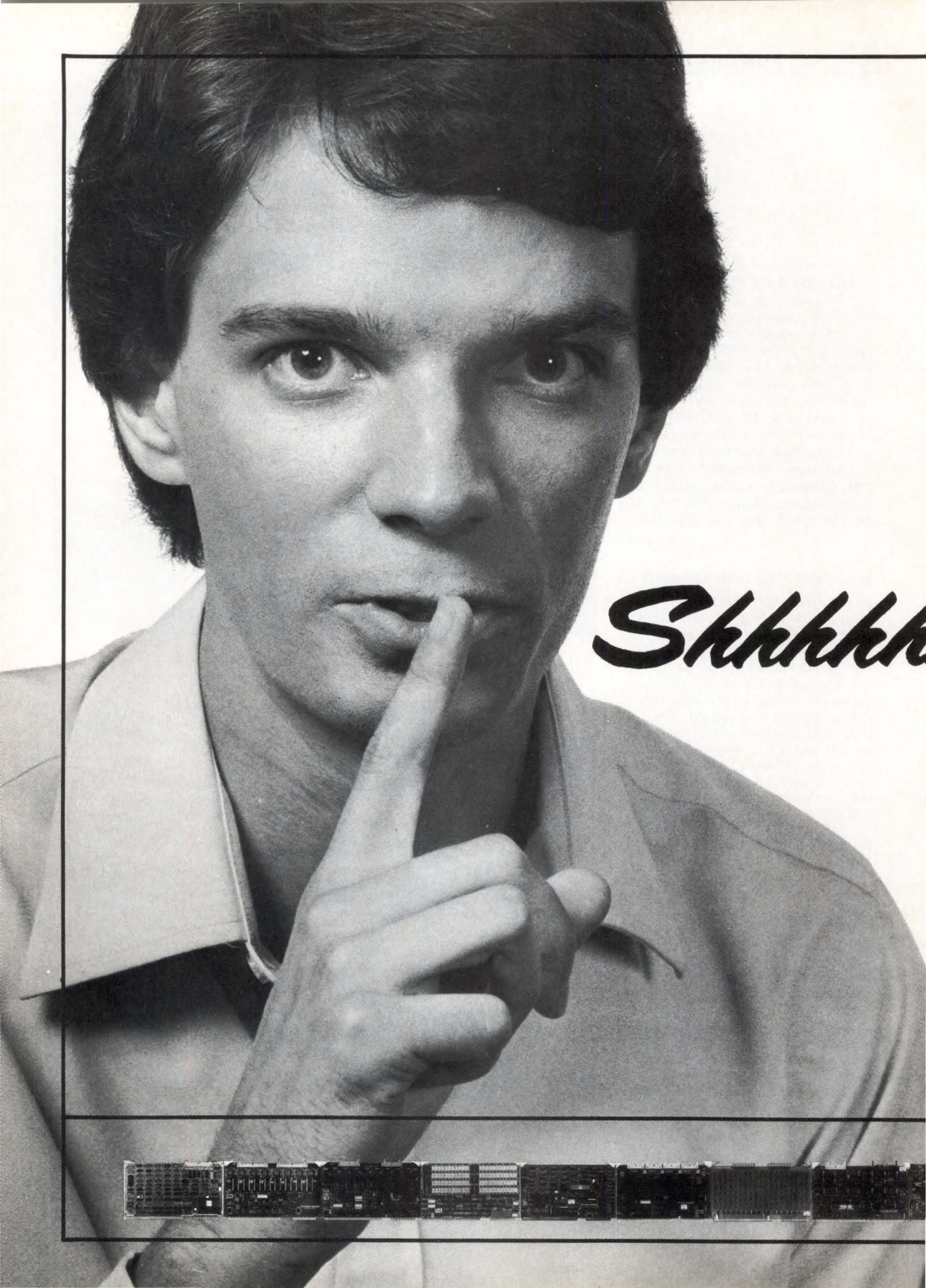
Circle 461

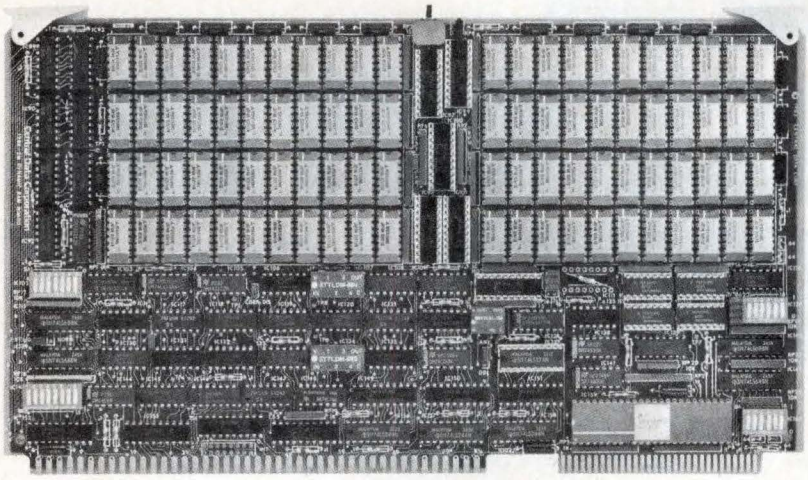
Micro Z80 family in CMOS

Pin compatible with the NMOS version Z80, TMZ84CXXX family members use only one-sixth the power of their NMOS counter-parts. The CPU's low operating current and wide operating voltage range suit the CMOS chips to battery-operated applications. Features include an extended temperature range (−40 to 85 °C) and high electrical noise immunity. Pricing in small quantities is $8.95. **Toshiba America, Inc,** 2441 Michelle Dr, Tustin, CA 92680.

Circle 462

April Preview
Special Report on Disk Memory


Shhhhh



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You told us that you wanted more speed and fewer noise problems from a complete line of Dynamic RAM boards. Central Data's EDC and Parity Only boards deliver just that and more. Our primary design objectives were speed and reliability, and we've achieved that by the unique combination of features engineered into these boards.

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Dynamic RAM Boards are especially susceptible to noise problems. It is therefore essential that a heavy power and ground plane be run throughout the board and that an adequate number of bypass capacitors be used. Central Data's Dynamic RAM Boards have 4-layer and 6-layer construction, with at least 2 of the internal layers dedicated to power and ground.

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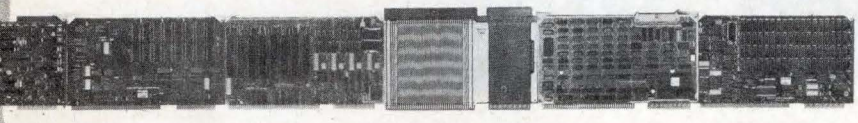

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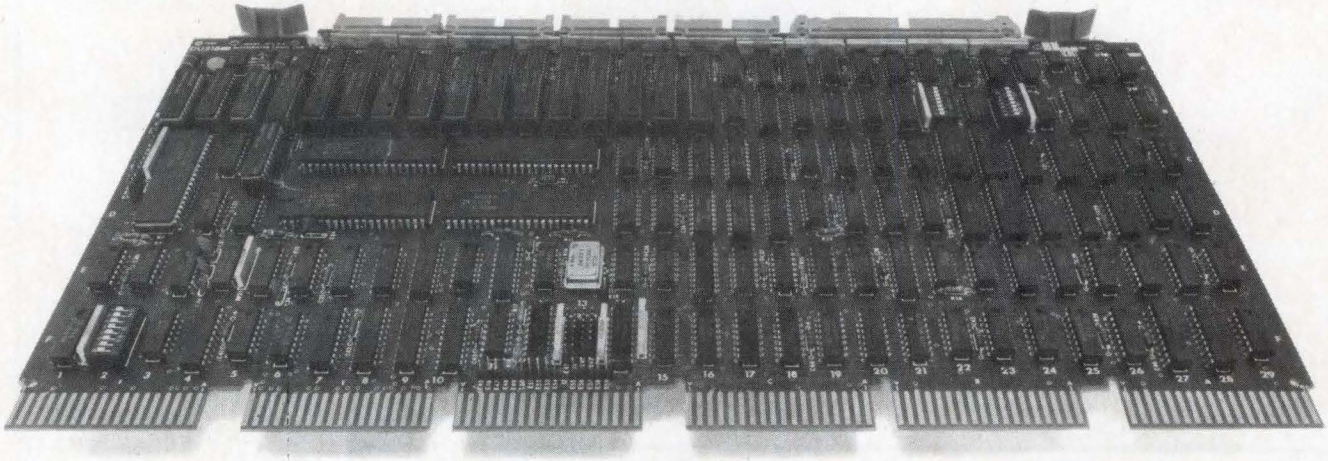

RM02-RM05

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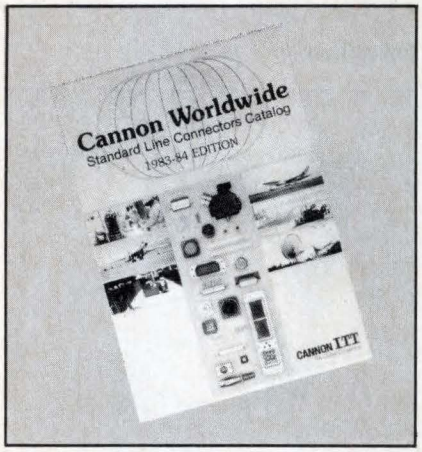
Line connectors



Catalog of standard line connectors and manual/semiautomatic assembly equipment contains 300 pages of technical information. **ITT Cannon,** Fountain Valley, Calif. **Circle 410**

Infrared light emitting diodes

Data sheet highlights plastic replacement devices for TO-46 hermetic types; charts, graphs, and illustrations accompany data on dimensions, absolute maximum ratings, and electrical characteristics. **TRW Electronic Components Group, Optoelectronics Div,** Carrollton, Tex.
Circle 411

Compact quad switchers

Data sheet describes features, specs, and ratings of 2.5- x 5- x 10.5-in., E200 series 200-W switchers. **Deltron Inc,** North Wales, Pa.
Circle 412

Rotary uninterruptible power

Brochure highlights standard features and options of Rups line, including a table of specs for 12.5- to 500-kVA systems. **Computer Power Products,** Gardena, Calif.
Circle 413

Custom control components

Brochure summarizes features of low voltage control elements, such as relays and contactors, push buttons and indicating lights, and fuseless motor protective breakers. **Klockner-Moeller,** Natick, Mass.
Circle 414

Electronic wire and cable

Enlarged edition is divided into 18 sections, including flat cable, coaxial connectors, plenum cable, and computer and coaxial cable. **Manhattan Electric Cable Corp,** Rye, NY. **Circle 415**

Fiber optic illumination

Drawings and specs fill the 36-page catalog of Fiber-Lite systems and accessories; applications and technical data detail a range of illuminators, light guides, and systems. **Dolan-Jenner Industries, Inc,** Woburn, Mass.
Circle 416

Membrane keyboard design

Seventy-page reference manual gives technical data, graphs, and tables for writing a detailed custom membrane keyboard specification. **Dorman Bogdonoff Corp,** Andover, Mass.
Circle 417

Electronics definitions

Revised *Functional Definitions for the Electronics Industries* includes a selected glossary of terms used throughout user, merchandiser, distributor, and sales segments. Request on company letterhead ($5 postpaid) from: **Components Group, EIA,** 2001 Eye St NW, Washington, DC 20006.

Data communication year

"Sherry Says" wall calendar for 1984 lists significant events in communication history, as well as 42 major industry conferences and exhibitions. **Racal-Milgo,** Miami, Fla.
Circle 418

Components data book

An 850-page reference manual describes company microprocessors, development systems, and board-level products; book includes data on Z80,000, Z800, and Z8070, along with established product lines. **Zilog, Inc,** Campbell, Calif.
Circle 419

Creating R&D partnerships

Guidebook explains how to structure a partnership, as well as how to arrange a buyout; appendices detail attendant tax and accounting issues. **Deloitte Haskins & Sells,** New York, NY.
Circle 420

Membrane touch panels

Three application notes give an overview of membrane touch panels; the first note reviews approaches to basic membrane switching construction; the second considers effects of electrostatic discharge on semiconductor devices; and the third outlines usage parameters, sealing, and environmental considerations for choosing gold or silver contacts. **Micro Switch, a Honeywell Div,** Freeport, Ill.
Circle 421

Unix-compatible 32-bit micros

Twenty-four page booklet describes features and applications of multi-user, multitasking Universe 68 family, which runs both UNOS and AT&T-licensed CRDS System V operating systems. **Charles River Data Systems,** Framingham, Mass.
Circle 422

Vibration measurement

Thirty-page handbook containing glossary and troubleshooting guide examines vibration in rotating machinery; major sections cover vibration measurement, analysis, and instrumentation, along with dynamic balancing and applications. **Rochester Instrument Systems,** Rochester, NY. **Circle 423**

Development language

Four-page brochure highlights features of PL/N, a high level software development language for Route-commander and A-Line information management systems. **Norand Corp,** Cedar Rapids, Iowa.
Circle 424

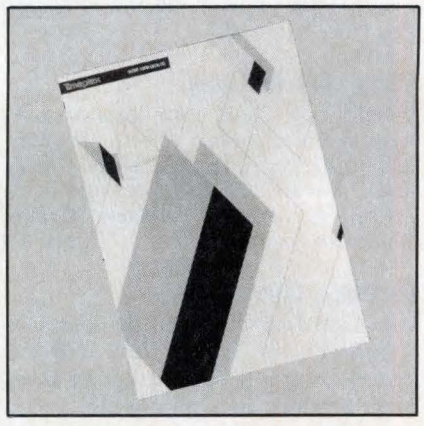
Computer accessories

Over 2400 products are described in 124-page cross-reference catalog of media, supplies, and cables. **Inmac,** Santa Clara, Calif. **Circle 425**

Wire and cable

Tabular product reference itemizes specs for critical applications in computer, power and control, and high temperature conditions. **Lapp Inc,** Fairfield, NJ.
Circle 426

Data communication equipment



Short-form catalog highlights features of network managers and individual products, including modems, microplexers, stat MUXes, packet assembler/disassembler, and data concentrator. **Timeplex, Inc,** Woodcliff Lake, NJ.
Circle 427

Electromechanical equipment
Ninety-eight-page catalog illustrates and describes off-the-shelf components for R&D, prototype engineering, maintenance, and testing. **American Design Components,** Moonachie, NJ.
Circle 428

Data for ac-dc and dc-dc power
Engineering and selection guide offers detailed electrical and mechanical specs for over 400 standard switcher, linear, and converter sources; 48-page reference comes with application notes and glossary of technical terms. **Semiconductor Circuits Inc,** Windham, NH.
Circle 429

Cables and accessories
Line catalog covers cables and assemblies for installing and expanding computer systems, local area networks, and data/telecommunication systems. **Support Systems International Corp,** Richmond, Calif. **Circle 430**

Miniature cables
Forty-page guide discusses how to select, buy, and use miniature cables, assemblies, and aircraft control cables. **Cable Manufacturing and Assembly Co, Inc,** Fairfield, NJ. **Circle 431**

Display/instrument interface
Product note gives schematics, programming code, and operational description of general purpose interface for hooking HP 1345A to the 68000 processor (and others). **Hewlett-Packard Co,** Palo Alto, Calif. **Circle 432**

Linear and switching
Twenty-page short form catalog gives electrical/mechanical specs, features, and ordering information for ac-dc linear and switching supplies and dc-dc converters. **Power Products Group,** Pompano Beach, Fla. **Circle 433**

Cartridge tape system
Technical data sheet details quarter-inch TapeSaver 969 storage and retrieval system for IBM Series/1. **Ultimate Computer Services, Inc,** Denville, NJ.
Circle 434

Per-channel electronic filters
Twenty-page brochure overviews 32-channel filter system, giving specs and performance graphs. **Precision Filters Inc,** Ithaca, NY. **Circle 435**

Pascal videotape courses
Folder describes series of 18 half-hour lectures, covering modern programming concepts from the 1960s through Ada and Modula-2 in the 1980s. **Engineering Renewal & Growth Program, Colorado State University,** Fort Collins, Colo.
Circle 436

Synchro conversion
Twenty-page product selection guide describes features and applications of hybrid and modular products, and lists second sources. **Natel Engineering Co, Inc,** Simi Valley, Calif. **Circle 437**

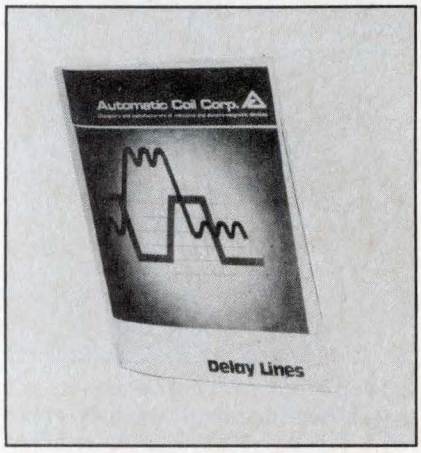
Unix command summary
Reference packet alphabetically lists Unix release III commands, describing format and options; VI reference with C library is included. Request on company letterhead (for $10, less in quantity) from: **Specialized Systems Consultants,** PO Box 7, Seattle, WA 98125.

Code conversion
Folder charts decimal, binary, octal, and hexadecimal base conversions, as well as conversions to ASCII (2), EBCDIC (71), and card code; command lists summarize Hiplot plotter functions. **Houston Instrument,** Austin, Tex.
Circle 438

Power supplies
Fifty-six pages of data profile complete line of power supplies offering outputs from 1 to 20 V, 60 A; miniaturized modules, dc-dc converters, and a range of programmable and unregulated versions are covered. **Acopian Corp,** Easton, Pa.
Circle 439

Designing PC boards
Brochure profiles CDX-5000 standalone CAD system, discussing 32-bit internal architecture, built-in database management, and object-oriented interface that controls system functions through graphic symbols and optoelectronic mouse input. **Cadnetix Corp,** Boulder, Colo. **Circle 440**

Analog-to-digital I/O
Pamphlet introduces hardware, software, and function modes of Dascon-1 data acquisition and control interface board for the IBM Personal Computer. **MetraByte Corp,** Stoughton, Mass.
Circle 441

Delay lines


Catalog features over 650 standard active and passive lines, including TTL digital delay and function modules; photos, dimensional drawings, and specs for 14-, 16-, and 24-pin DIP configurations are shown. **Automatic Coil Corp, sub of Designatronics, Inc,** Hialeah, Fla. **Circle 442**

Linear and conversion IC data
A 736-page book contains technical information for line of ICs, including sections on dice and reliability; also inside are guides for direct and functional replacements. **Precision Monolithics Inc,** Santa Clara, Calif. **Circle 443**

Plasma display technology
Article highlights benefits of plasma display terminals for commercial and military applications, reviewing plasma technology development as well as construction and operating principles of the SAIT ac display terminal. **SAI Technology Co, div of Science Applications, Inc,** San Diego, Calif. **Circle 444**

Protocol converters
Brochure describes Micro7400, which enables up to 12 asynchronous terminals to access IBM mainframes as if they were 3270-class devices; specs and block diagrams round out 12-page text. **Micom Systems, Inc,** Chatsworth, Calif.
Circle 445

Optical cable
Six-page brochure gives overview of communication design applications for transmitting data, voice, and images in computer, process control, data entry, and wired office systems. **Siecor Corp,** Hickory, NC. **Circle 446**

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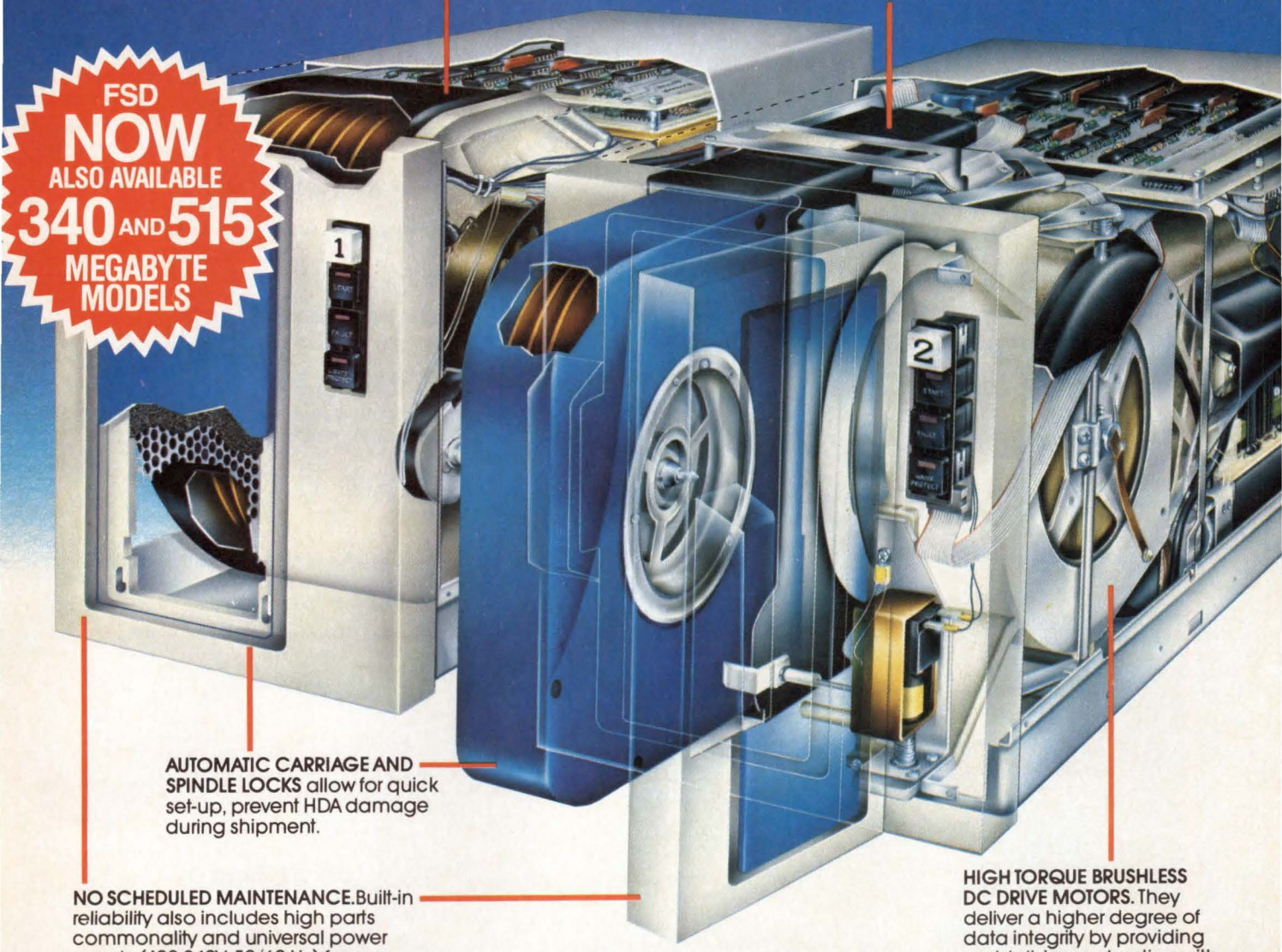

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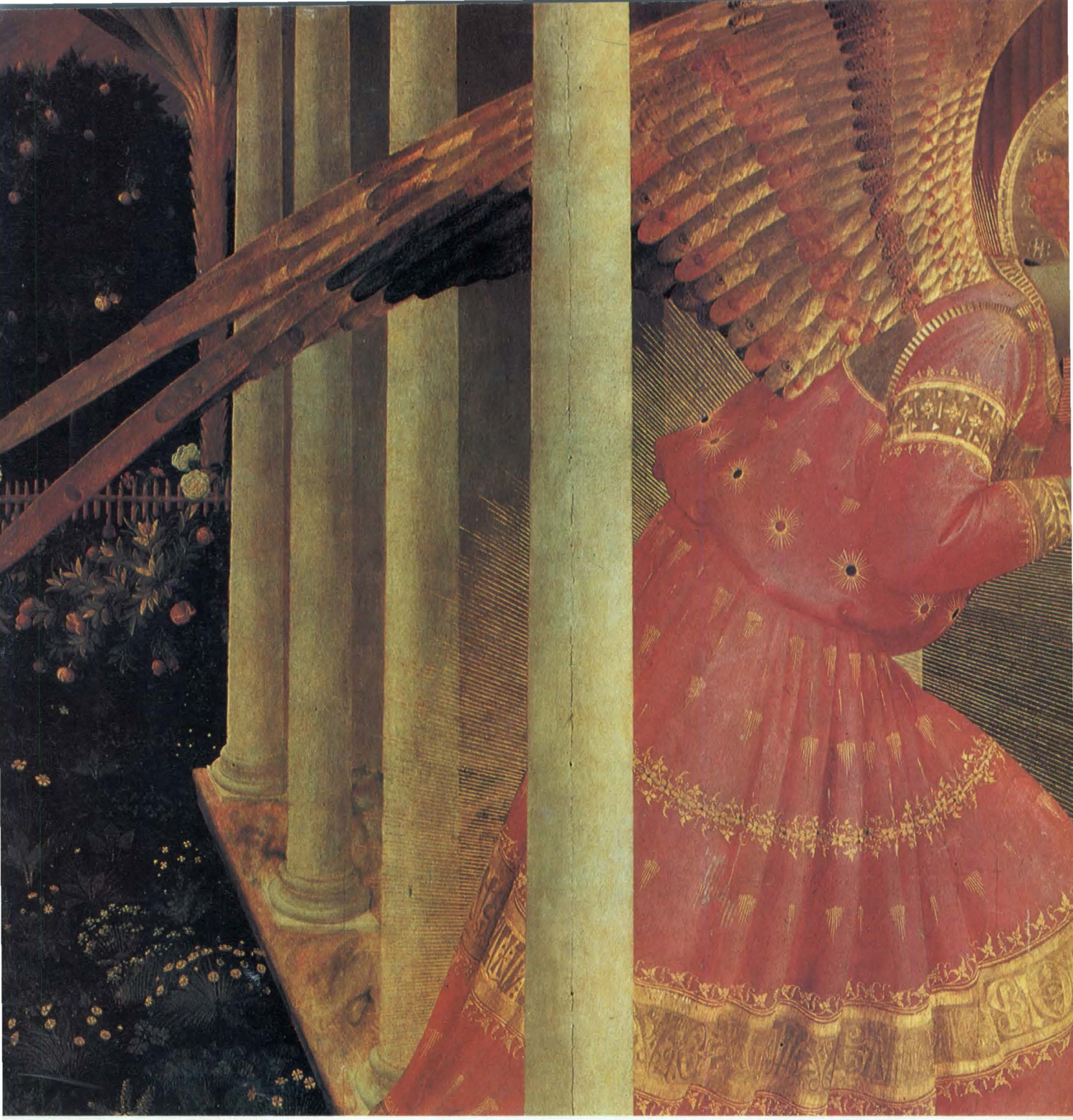

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Designer's Bookcase

SYSTEMS DEVELOPMENT DOCUMENTATION: Forms method

By *Technical Communications Associates, Inc.*

This 430 page publication presents a series of simple procedures for preparing documentation that evolve around the use of prestructured forms that record the results of the task performed during the system development cycle. The forms cover a wide range of system development functions and are formatted to present all types of documentation. Also suggested in this publication are standards for documentation preparation.

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AREA-EFFICIENT VLSI COMPUTATION

by *Charles E. Leiserson*

The microelectronics revolution has obliterated the traditional distinctions between hardware and software. The complexity of very large scale integrated (VLSI) circuits has become so great that each integrated circuit chip is a complicated system. The award-winning research reported in this book shows how techniques of algorithm design, which are usually applied to software programs, can be applied directly to the design of VLSI systems.

136 pages, 41 illus., $22.50 **CIRCLE 465**

ALGORITHMIC PROGRAM DEBUGGING

by *Ehud Y. Shapiro*

This book formulates and explores a potentially productive new subarea of computer science that combines elements of programming languages and environments, logic, and inductive inference. It devises a theoretical framework for program debugging and develops techniques that will partly mechanize this activity. In particular, it formalizes and validates algorithmic solutions to finding and then fixing program bugs.

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By *John A. Kuecken*

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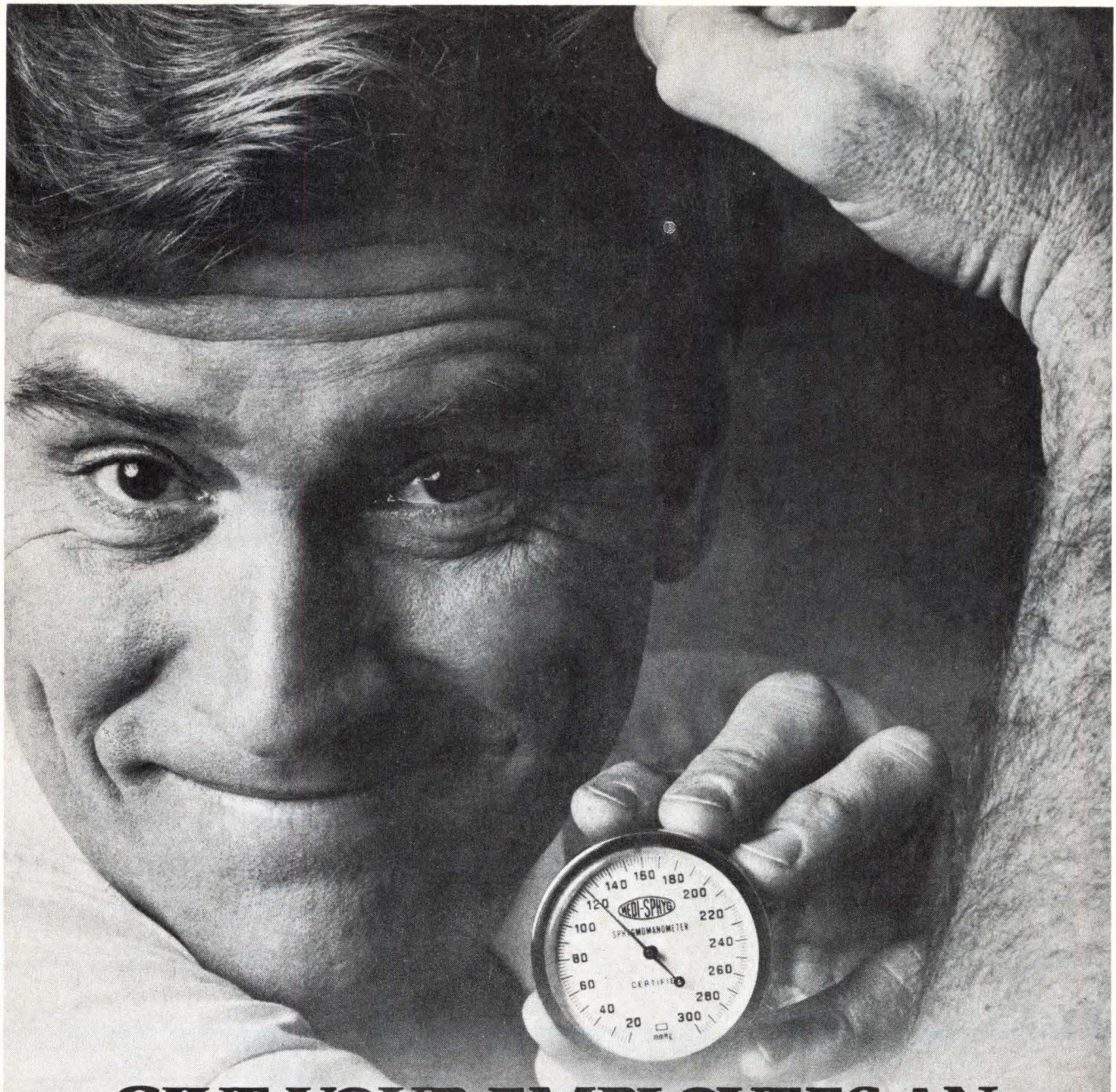

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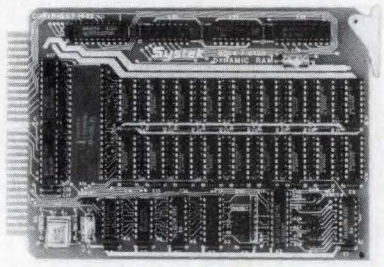

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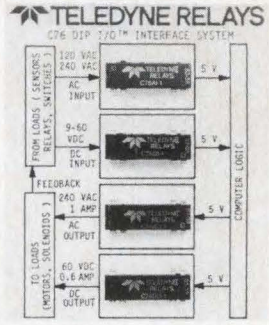

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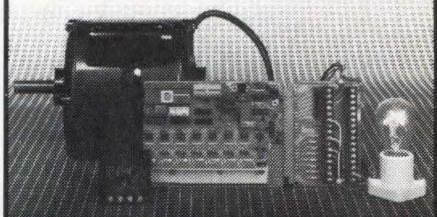

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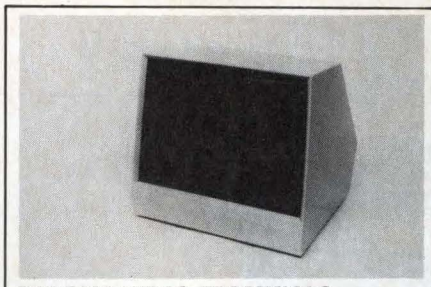

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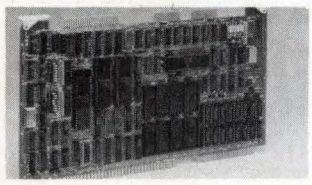

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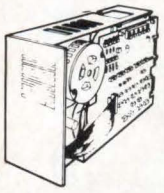

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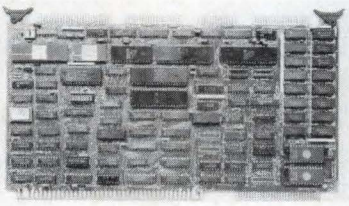

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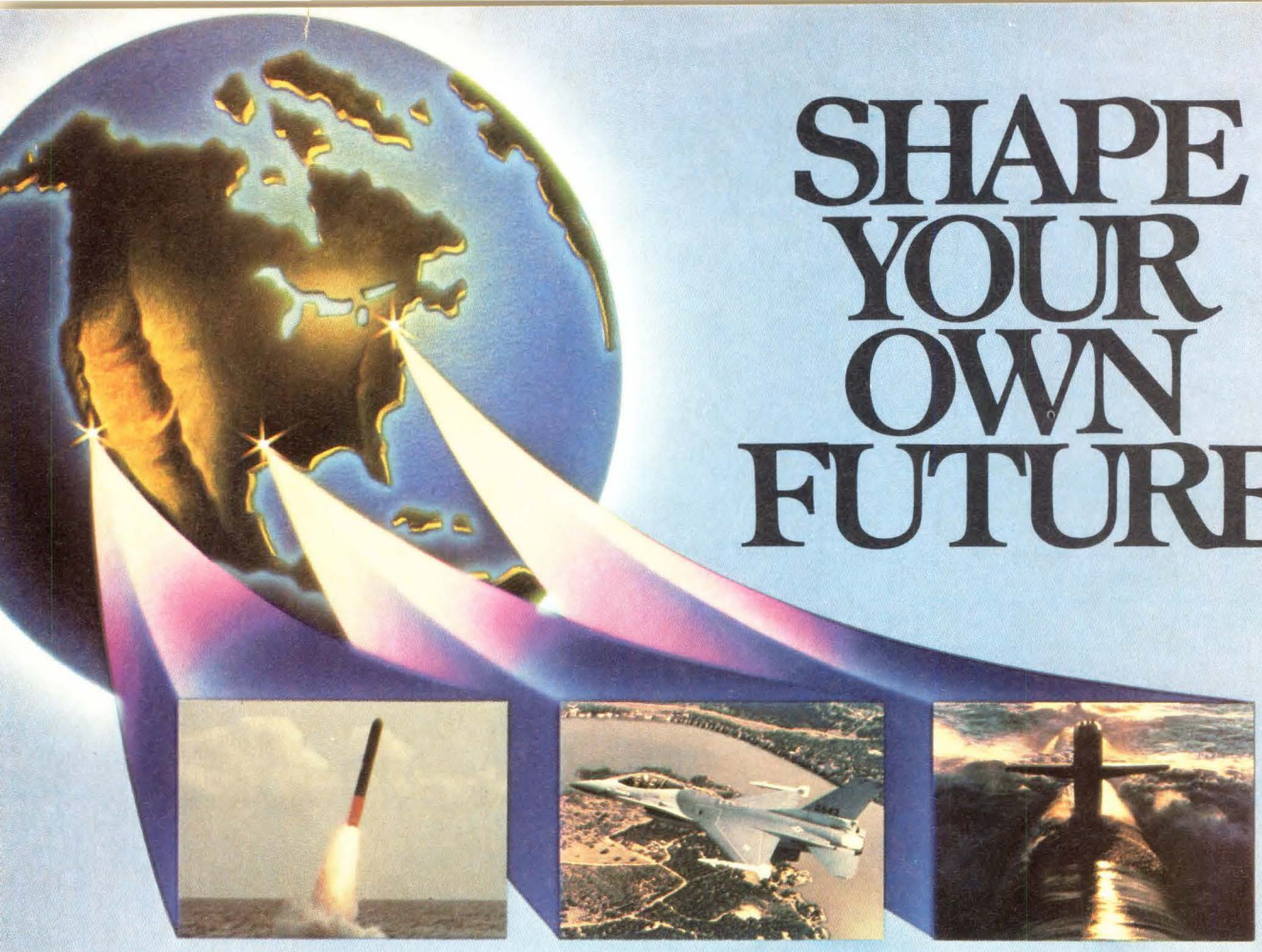

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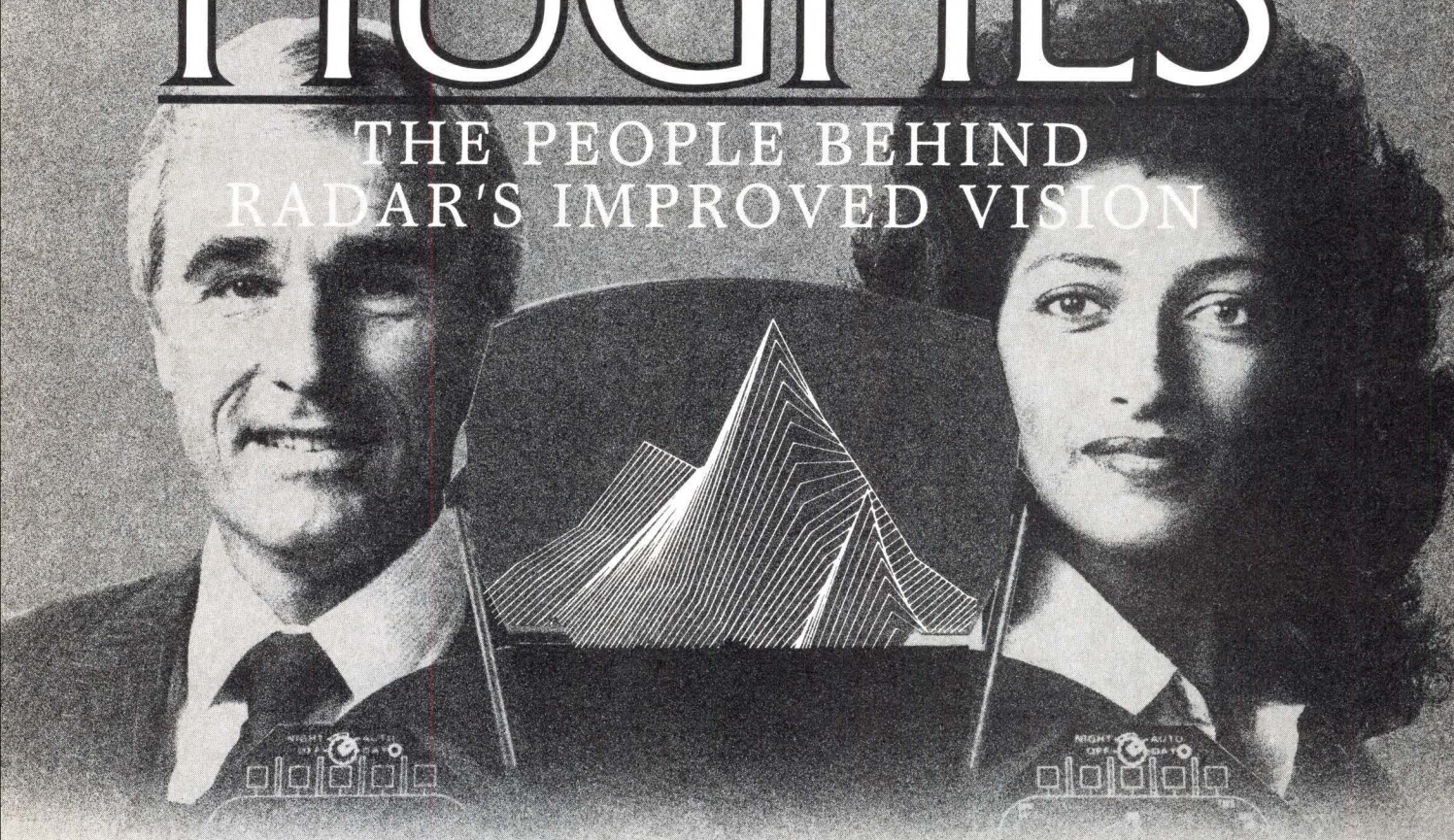

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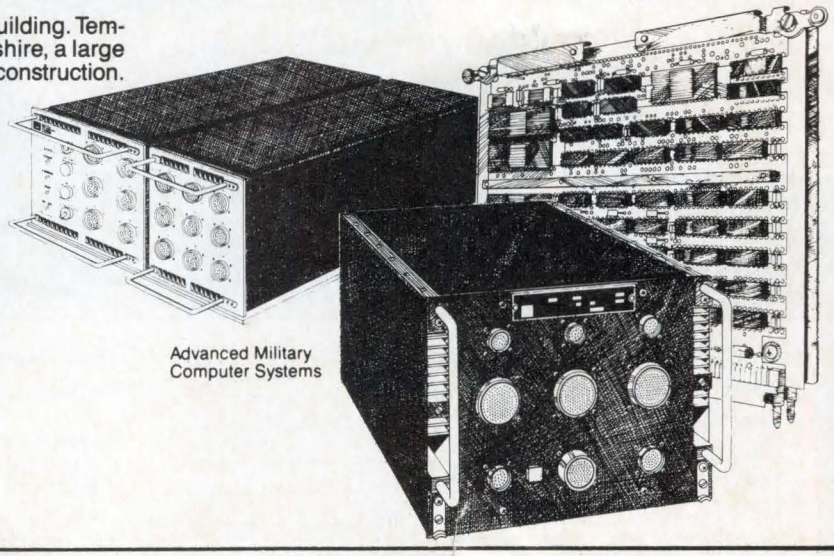

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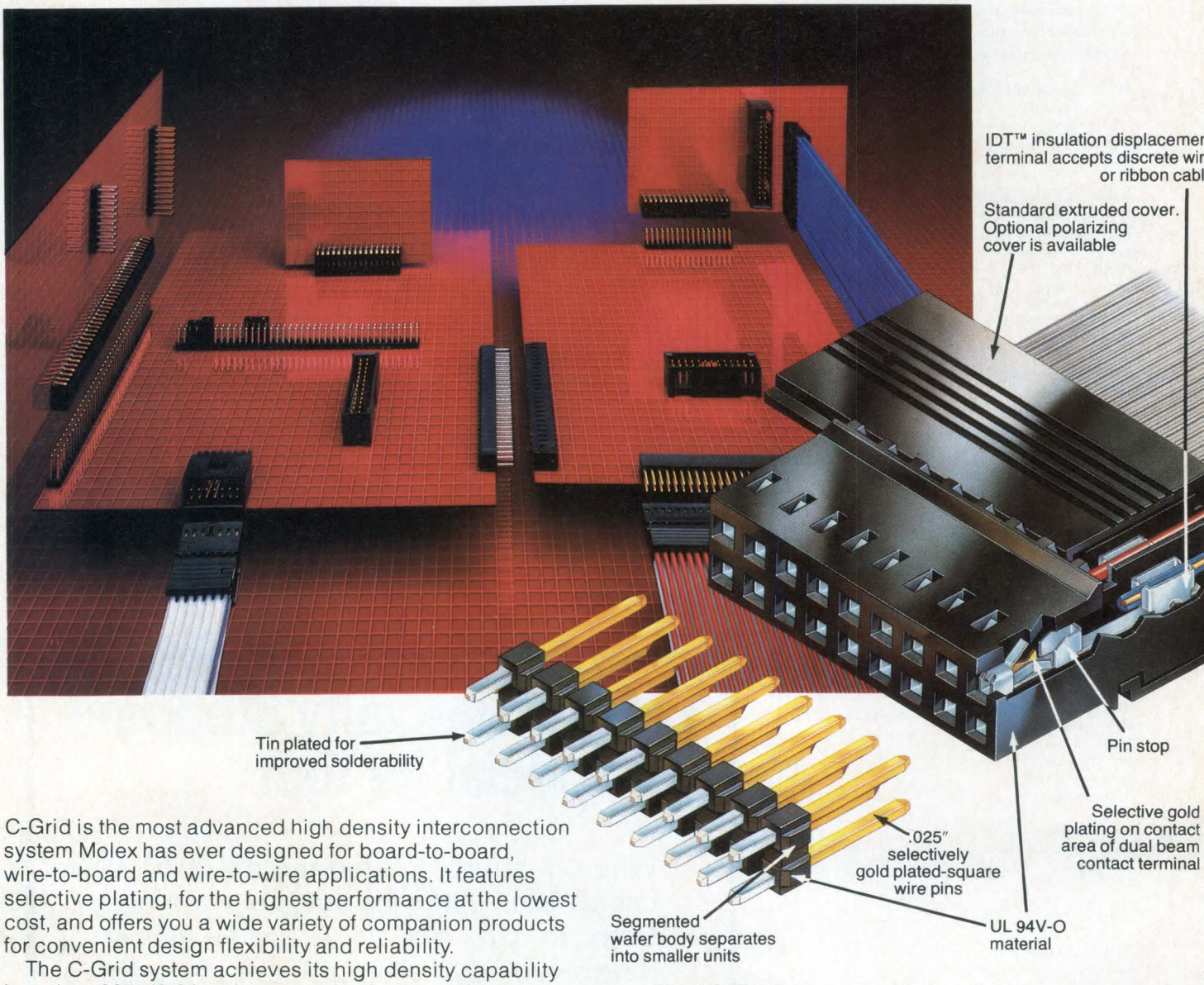

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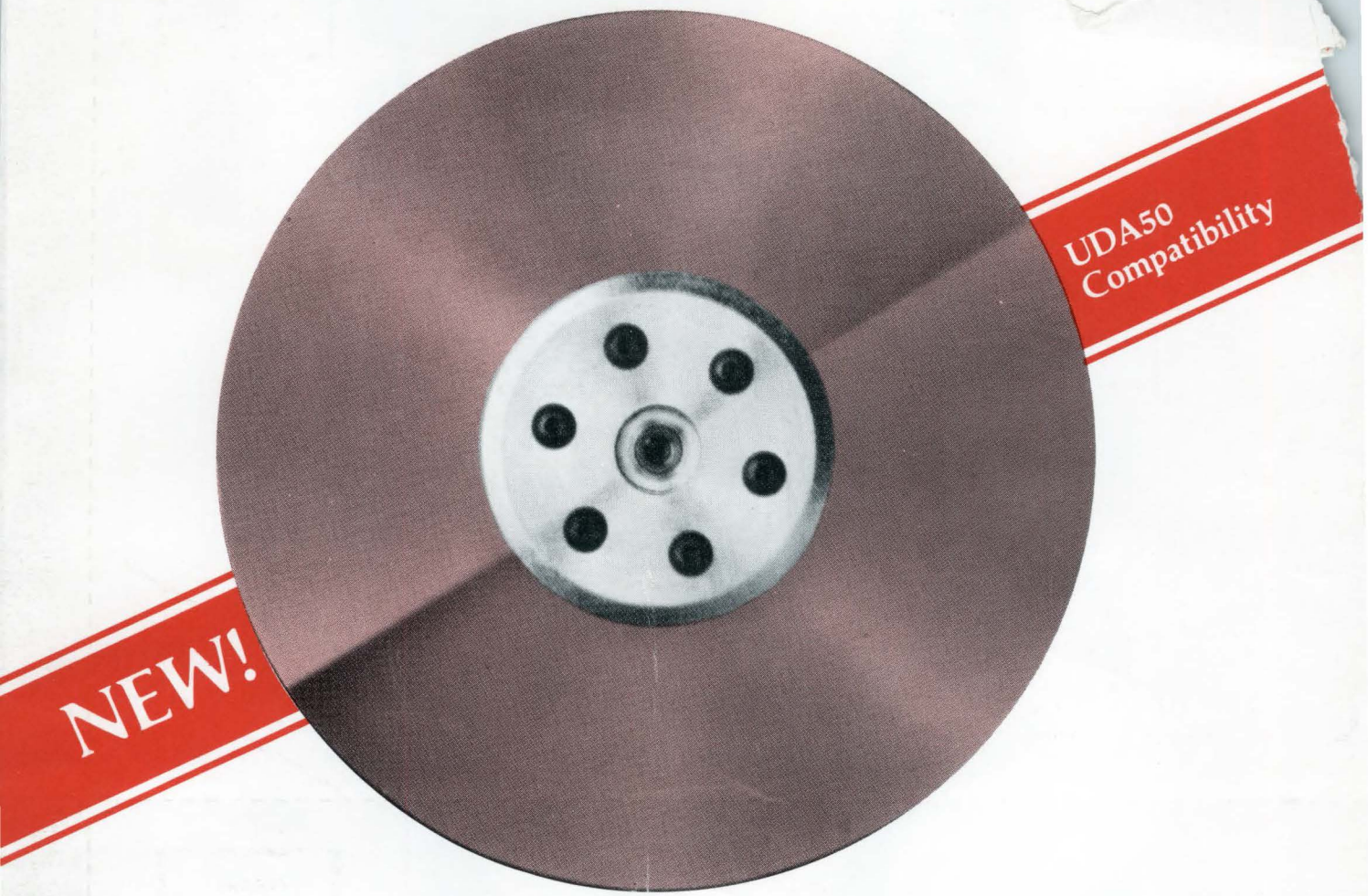

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