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CIRCLE 2

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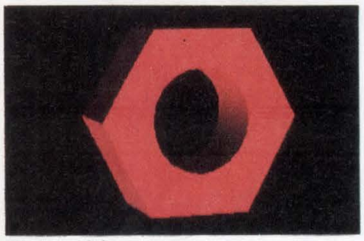
System technology



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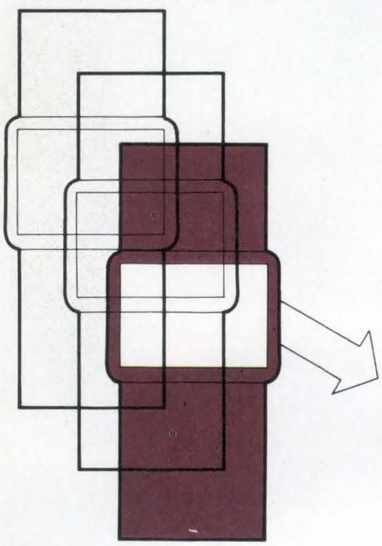
System design



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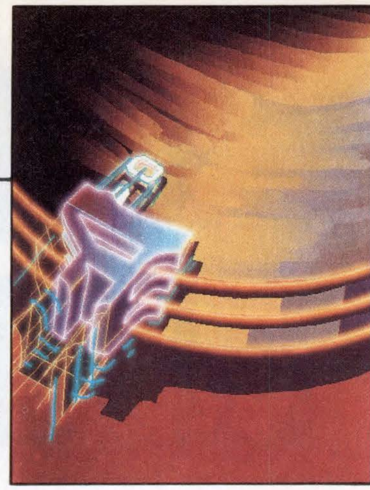
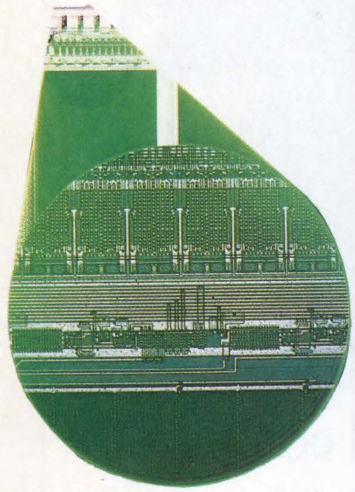
Special report on disk memory



This month's cover was created and designed by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.

System components



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Departments

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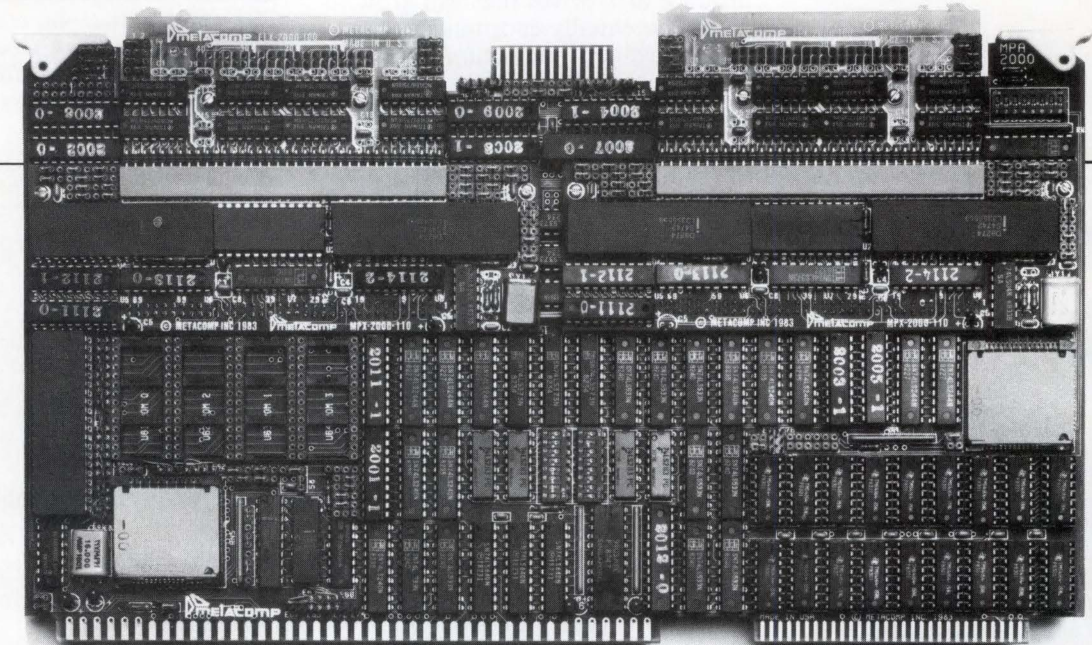

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CIRCLE 3

UP FRONT

Bell's 32-bit chip takes only 12 months to design

A second-generation 32-bit microprocessor chip with separate 32-bit data and 32-bit address lines has entered production at AT&T Technologies, Western Electric Div (New York, NY) after only a 12-month design and test cycle. The WE 32100 chip is a successor to the BellMAC-32A chip, which it can replace in existing equipment without software changes. The new CMOS chip contains 180,000 transistors—roughly 30,000 more than its predecessor—and runs about three times faster. The speed increase stems from a reduction in channel width from 2.5 to 1.7 μm and an onboard cache memory that holds up to sixty-four, 32-bit words. By storing often-repeated program instructions, the cache avoids wait time. The 5-V chip dissipates 1.9 W and is enclosed in a 132-pin ceramic package.—*N.M.*

Partnership gives VME community a boost

When the No. 2 supplier of VME boards worldwide joins forces with a leading European supplier of commercial and military CPU- and memory-based boards, it can only be for one reason: to become the No. 1 supplier of VME-based boards worldwide. Currently, that position belongs to Motorola (Phoenix, Ariz). However, Force Computers (Santa Clara, Calif), the leading VME board supplier in Europe, has teamed up with Plessey Microsystems (Northants, England) to displace Motorola. The agreement between the two companies calls for Plessey's U.S. operations (Pearl River, NY) to manufacture and market board-level VME-bus products and accessories currently produced and marketed by Force. Jointly offered products will be pin compatible. The industry's first 2-Mbyte dynamic RAM board for the VME bus will be one of the first newly designed Force boards that Plessey will second source. This board contains 256-Kbit dynamic RAMs supplied by NEC and is available this month.—*N.M.*

Soviets may have optical memory breakthrough

The U.S.S.R. has a memory system based on a 5-cm square plate containing multiple Fourier microholograms, according to a report from International Resource Development (Norwalk, Conn). A computer controlled playback machine stores a number of these plates, selects a desired plate, and displays the holographic image on a monitor. Elsewhere, research is under way in both the U.S. and France. Harris (Melbourne, Fla) is already in the forefront with a system that translates data from electronic to optical form, using holographic interference patterns on microfiche cards.—*M.B.*

Codex redefines the modem

Rising to "network system resource" status, 2600 series modems from Codex (Mansfield, Mass) are based on a 68000 microprocessor that manages a bus architecture. The 2660 version uses trellis coded modulation to provide an error correction scheme using special algorithms for choosing correct data. It accomplishes this by comparing redundantly transmitted information and correcting distorted bits. This 8-state scheme yields increased immunity to noise and other disturbances. Top speed of the 2660 is 16,800 bits/s. The modem also has an adaptive rate system that directs the modems to transmit at the maximum speed the line will allow. Options include 4- or 6-channel buffered multiplexers, registered dual dial restore, and an XL-1 system that provides support for the standard or custom modem features.—*M.B.*

Heavyweights take a stand on tape standards

Free interchange of recorded data, long hampered by lack of an established standard, is the aim of two industry leaders. A joint program conducted by 3M's Data Recording Products Div (St Paul, Minn) and Digital Equipment (Maynard, Mass) is expected to create the necessary standard—at least in the half-inch tape cartridge world. As presented to the ANSI X3B5 committee, the proposal covers both the cartridge and recording format. The cartridge itself, called CompacTape, is a single-reel unit that measures approximately 4-in. square and 1-in. thick, and stores 100 Mbytes of formatted information. The associated drive, code-named "Maya," is currently under development. According to knowledgeable sources, it will use the existing TS-11 start-stop interface, but will also allow for streaming operation. Maya's formal introduction later this year should be followed by that of a 500-Mbyte device, code-named "Yankee," which will ensure wide upward compatibility for data stored on all CompacTape cartridges. Look for the higher capacity drive in 1986.—*J.A.*

Industry and academia break the ice on new R&D fronts

Industry is actively pursuing universities to form research-and-development partnerships that will cultivate advanced technologies for CAD/CAE/CAM and networking—two fields that have been light on academic research before now. In such ventures, company scientists and engineers are working closely with university staffs to exchange fundamental research and application expertise. For one, GE Calma (Santa Clara, Calif) plans to locate an advanced systems group inside Rensselaer Polytechnic Institute's (Troy, NY) "incubator program" for future high technology enterprises. In turn, RPI will develop computer architecture, hardware, software, and simulation for CAD/CAM/CAE systems that Calma may manufacture. Another recent agreement has made Codex (Mansfield, Mass) an industrial partner in the Massachusetts Institute of Technology's (Cambridge, Mass) ongoing Athena project. The immediate application will be a network interconnecting approximately 2600 computers and workstations installed in over 100 campus buildings. Technology being refined for this purpose will involve local area networking, wide area networking, internetworking, and network management.—*D.H.*

Real devices take part in complex circuit design simulation

Two companies are breaking new ground in system simulation technology by incorporating hardware in the VLSI circuit design process. This eliminates the time and errors inherent in building a behavioral model of the reference device, and frees the designer to concentrate on creating the new system part. Valid Logic Systems' (Mountain View, Calif) Realchip uses actual microprocessors, controllers, gate arrays, and custom chips as hardware models. Working together with the company's SCALDsystem workstations, Realchip plugs into "software schematics" that result in a virtual logic analyzer exercising a virtual breadboard with worst-case timing characteristics. A Daisy Systems (Sunnyvale, Calif) upgrade to the MegaLogician workstation comes with an electrical interface that is general enough to hook up almost any device—from single DIP to complete computer system—with the simulation process.—*M.B./S.B.*

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CIRCLE 4

Superminicomputers battle for performance specs

Harris and Gould (both of Fort Lauderdale, Fla) are at it again, carving out a broader superminicomputer market share. The 48-bit Harris 60 packs nearly 1-MIPS performance in an office-styled 30- x 19- x 30.5-in. cabinet. A cache memory option speeds memory access while increasing performance by 20 percent. The low end system is upwardly compatible with other Harris models and is priced at $69,500. Gould's 32-bit Concept 32/97 benchmarks from 4.67 to 10 MIPS. An optional multiply accelerator is the booster for this performance rating. The 32/97's basic configuration includes a 32-Kbyte cache, expandable to 128 Kbytes for increased cache hits and improved system performance. These machines range from $245,000 for a basic configuration to $495,000 for a fully configured version.—*M.B.*

Protocol analyzers wager ergonomic features

"User friendly" is now the watchword, even in instruments as esoteric as network protocol analyzers. Recent introductions by Digilog (Montgomeryville, Pa) and Hewlett-Packard (Palo Alto, Calif) help engineers diagnose network problems by including features for softkey and automatic setup as well as network and setup data storage. Also equipped with intelligent displays, machines from both companies automatically determine line protocol, data code, speed, parity, and the like for bit-oriented multilevel protocols. Capacity for setup and line data storage in Digilog's analyzers ranges from 32-Kbyte EEPROM in entry-level model 200 to 10-Mbyte Winchester disk in top-of-the line model 800. Hewlett-Packard's 4951A and 4955A have interchangeable tape storage. In addition, various levels of statistical analysis with graphics are coming available on higher end models, with color on the Digilog 800.—*T.W.*

Ring network uses tokens to switch messages

Using a dual-bus token ring network as its backbone, Incomnet (Ventura, Calif) can pass messages as long as 64 kbytes between any two of 1024 nodes on a single local network or across any of 255 connected LANs. A Unix-like network operating system maintains a directory of all nodes on all networks so that internet routing can take place without addressing specific physical locations. The proprietary network access method developed for the Incomnet 3000 moves a token freely around the ring rather than from node to node. As a result, the token is taken only when messages are transmitted. Acknowledgment occurs when the originating node sees the token again without the message.—*J.A.*

X.25 chip gets the go-ahead from GTE Telenet

Western Digital's (Irvine, Calif) WD 2511 X.25 packet-switching communication controller has received certification from GTE Telenet to operate as an interface device on the link level of GTE Telenet's data network. Designers can thereby add communication capabilities to their systems at minimal cost in PC board real estate, chip count, and power consumption. Along with Ethernet controller chips from other vendors, such as Intel and Seeq Technology, the new device is following the industry trend toward putting sophisticated functions onchip to simplify the system implementation process.—*S.B.*

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CIRCLE 5

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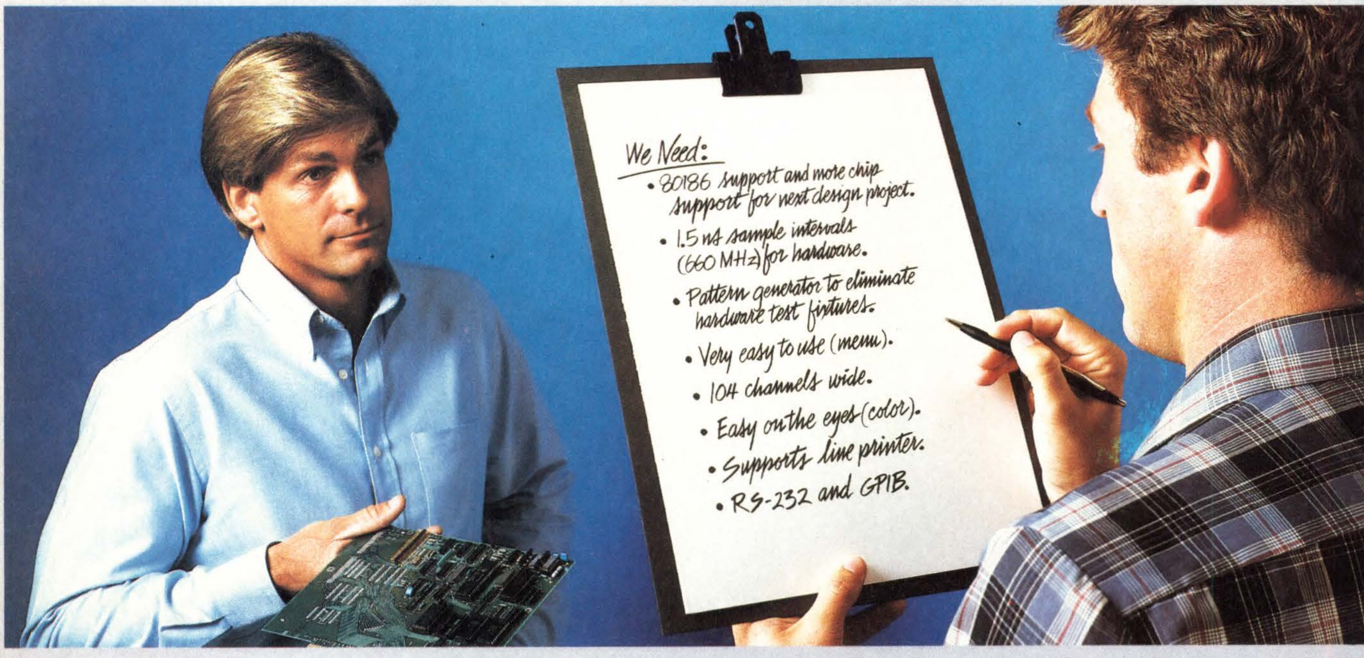

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DON'T LOOK BACK

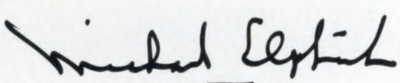
A few months ago, a young computer engineer on our staff asked me if I had ever played a pinball machine. Apparently, she had discovered one of these dinosaurs parked behind the videogames in some amusement arcade. I admitted I had occasionally played pinball machines between classes at engineering school. I was tempted to mention that I had also used a slide rule and once helped design a computer that contained vacuum tubes, but I kept my big mouth shut. Even though I didn't mention the vacuum tubes, however, she figured I must be over the hill. Thereafter, she always seemed surprised whenever I demonstrated any knowledge of today's technology.

One of the sadder aspects of the computer industry is the lack of understanding young engineers display towards older engineers. In Tracy Kidder's book, "The Soul of a New Machine," for example, some of the young engineers at Data General tried to figure out what happened to older engineers, because there didn't seem to be any in their department. They concluded that perhaps they were "turned out to pasture or else made into dog food." However, the real villain of Kidder's book seemed to be not the young engineers—who were themselves innocent victims—but an industry that placed such an apparently irrational premium on youth.

But age discrimination could not exist in the computer industry unless it made some sense economically—because people running this industry are rarely stupid. Unfortunately, older engineers often are less productive than their younger and more enthusiastic rivals. The real key to an engineer's value, though, is not chronological age but attitude of mind.

Because of the industry's obsession with youth, older engineers have become a relative bargain in the labor market. I discovered this several years ago when I was with another magazine. At that time I hired two engineers who were approaching normal retirement age. Both men were highly qualified and their salary requirements were quite reasonable considering their accomplishments. In their job interviews, though, the two contrasted sharply. The younger of the two persisted in recalling past glories and waded through a seemingly endless portfolio of patent applications for relay logic schemes he had devised. The older one, however, suddenly seemed thirty years younger as he talked excitedly about the frontiers of advanced research. Both proved successful in the sense that they are still working as editors. But the forward-looking one is now an internationally recognized authority on trends in computer software, while the backward-looking one spends a lot of time grinding out surveys of electromechanical components.

Like people, magazines can also age if they lose their enthusiasm for the subjects they cover. *Computer Design* recently celebrated its 21st birthday—which makes it ancient by comparison with most computer magazines. But, because we love to discover new things that are happening in this dynamic industry, we feel like a two-year-old. If we ever forget the secret of perpetual youth and you find us looking back instead of ahead, please tell me. We would hate to grow old.



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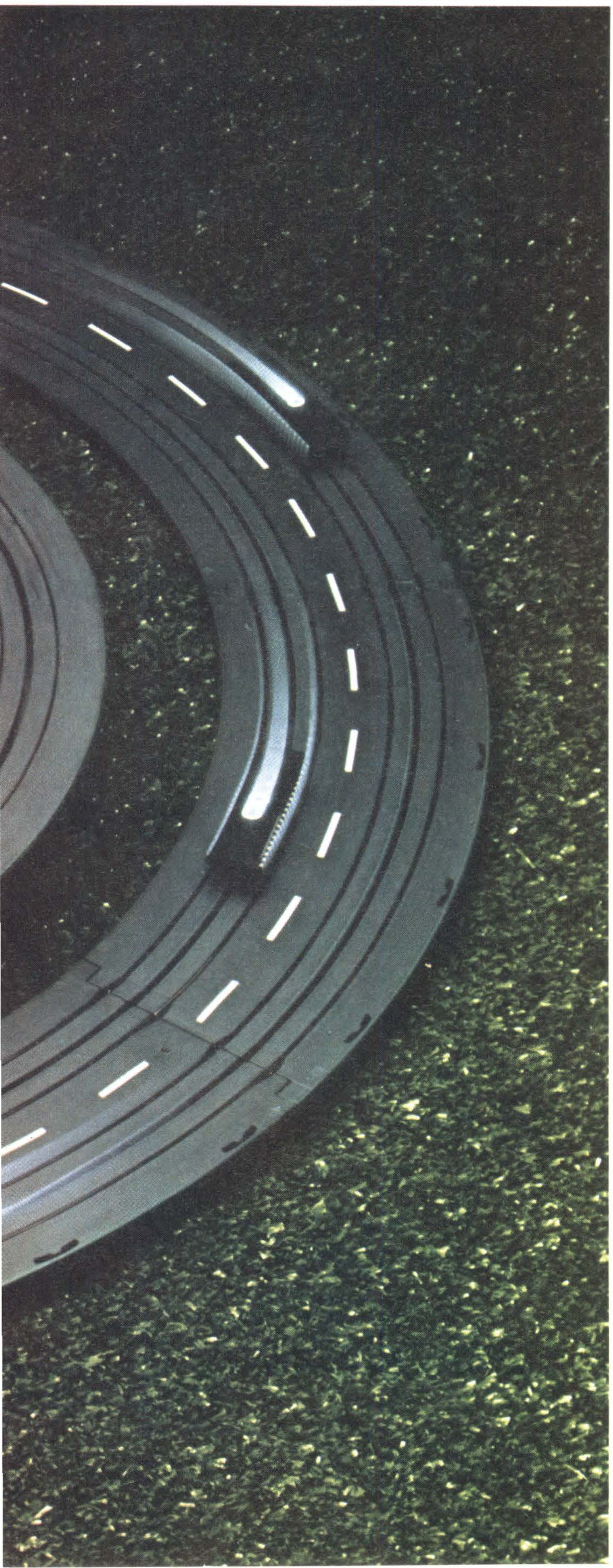

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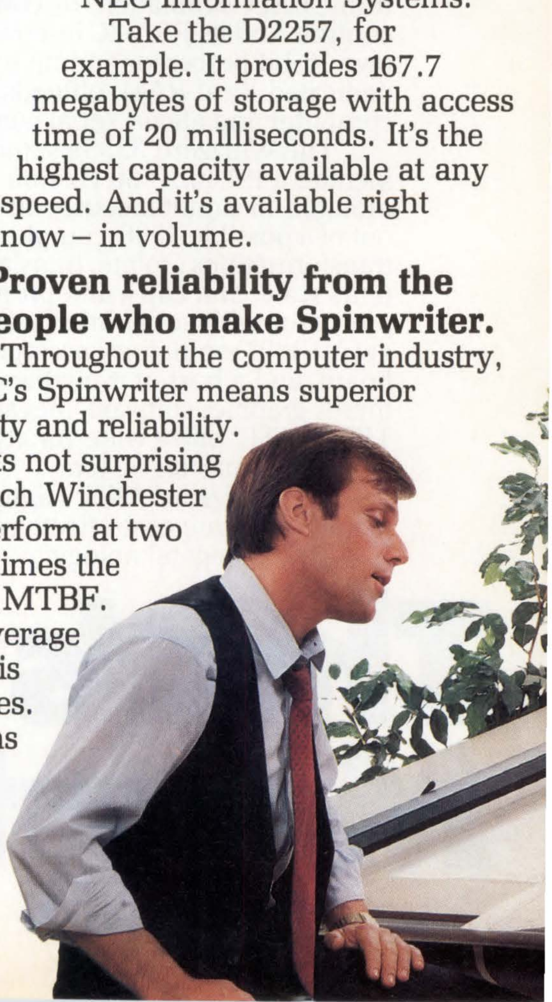

Added power

I was very interested in Deb Highberger's article, "Power Supplies Come to Grips with MOS Technology" (Dec 1983, p 213). The article made a number of excellent points. However, while discussing online and offline backup systems for CMOS systems, it stated, "Unfortunately, online approaches already popular in mainframe and minicomputer installations are usually too expensive a solution for today's bumper crop of low cost computer equipment." Maybe that was once the case, but no longer.

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Newton E. Ball
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5625 Kearny Villa Rd
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Cross developments

The article, "Development Systems: Big Chips Require High Level Tools" (Jan 1984, p 149) failed to describe the most powerful approach to micro software development: cross development using a superminicomputer or mainframe. Overall development time is typically cut by 25 percent or more compared to even the newest micro-based development systems.

The article mentions some cross tools, but overlooks First Systems Corp. Our MicroSET-86 tools provide the most complete set of cross development tools available for the Intel 8086 family. Translators include a highly extended Pascal-86 suitable for system programming, full PL/M-86, Fortran-77, C-86, and Macro Assembler-86—all generating Intel-compatible, relocatable object modules. After translation, modules are linked by an Intel-compatible Linker and Locater. All languages support the 8087.

Mary E. Avera
First Systems Corp
865 Manhattan Beach Blvd
Suite 200
Manhattan Beach, CA 90266

Keep it simple

I could not agree more with Michael Elphick's editorial (Feb 1984), "The Computer Illiteracy Threat," deploring the current hype surrounding computer literacy issues. I feel it has long been wishful thinking (and much propaganda) on the part of computer manufacturers (and lately educators) that everyone, to survive the socioeconomic future, must become computer literate. This is hogwash!

If manufacturers had designed the computer (particularly the personal computer) right in the first place, there would be no need for an indepth understanding of operating systems, programming, and cryptic-like command dialects that prevail in the computer marketplace. Leave this perplexing dominion to the technocrat.

Unfortunately, computers were originally designed by engineers and programmers for other engineers and programmers. The fact that these systems would be used by "civilians" never crossed their minds.

As designers, we have the ability to configure a system any way we see fit. A computer is a "smart" device and it seems ludicrous that software designers insist on forcing users to learn some cryptic, obscure command structure to do even the simplest of tasks. For instance, what does "PIP" have to do with the concept of transferring files?

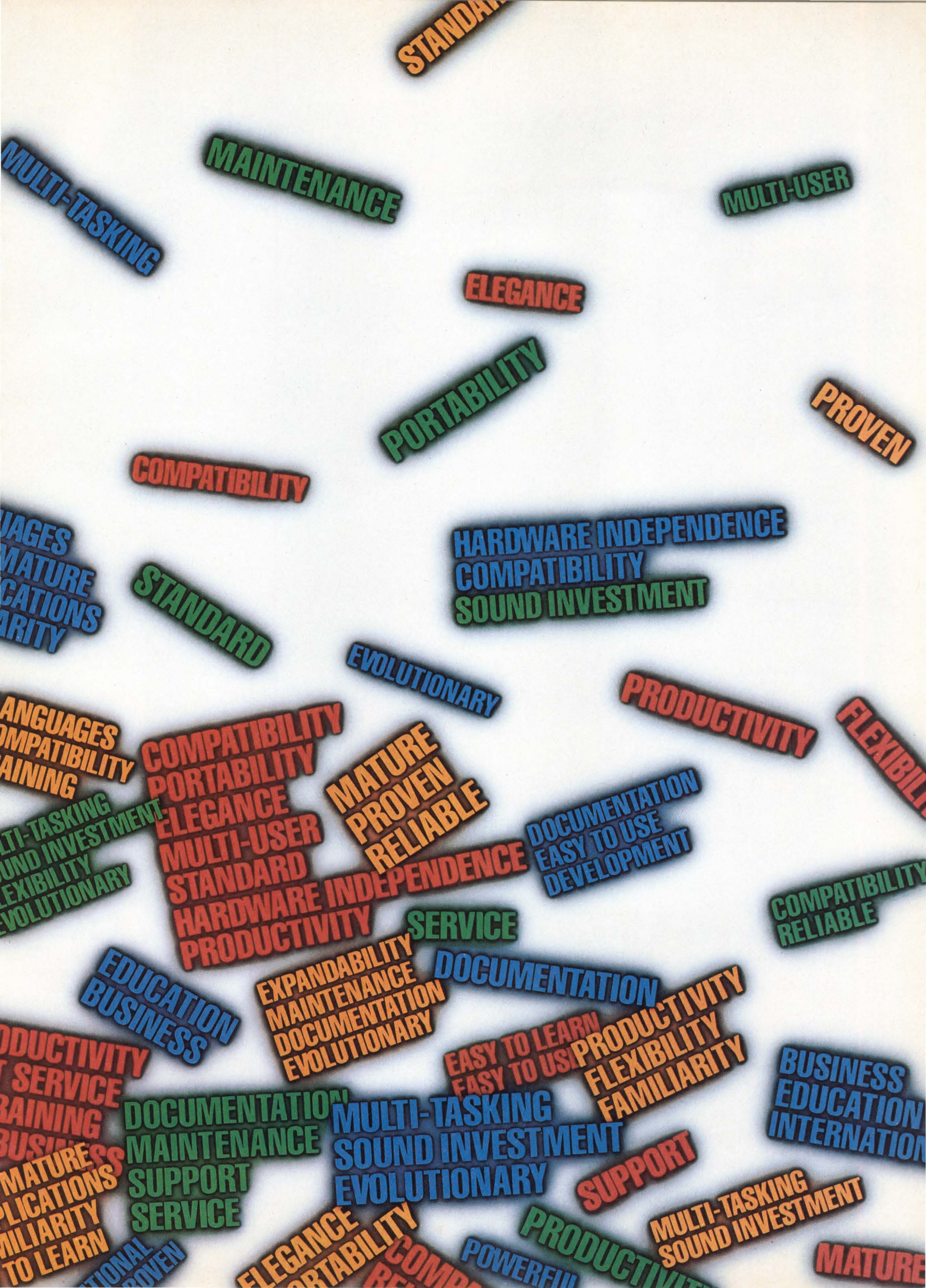
The technological winds are beginning to shift toward the uninitiated. Observe, for example, Apple Computer Inc's newest system—the Macintosh. The emphasis placed on this new design is in running application software with minimal operator participation in the internal workings of the system. With its Lisa and Macintosh systems, Apple is attempting to address the nontechnical users' needs, instead of computer "hackers."

This is as it should be. I believe it is incumbent upon the computer industry to wake up to the fact that the vast majority of future computer users will never understand the difference between a bit and a byte. Efficiency in performing a necessary job function will compel them to buy a computer, not to learn to program in Basic.

I would also agree with Mr Elphick's assessment that educational software has a long way to go before it becomes an effective tool in the classroom. Too many teachers these days are using the computer as a convenient, automated babysitter.

E. Francis Avila
Litton Engineering Laboratories
PO Box 950
Grass Valley, CA 95945

November/December designer's preference study winners: Eugene W. Smith III, Nixdorf Computer Corp, November; Richard L. Coleman, Wavetek Corp, December—winners of the HP 41CV programmable calculator.



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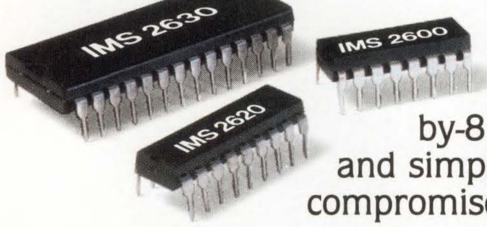

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	120	190	IMS2620-12
	150	240	IMS2620-15
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CIRCLE 19

Lisp/APL merger supports functional programming concepts

The last thing that software practitioners need is yet another programming language that promises to solve all their problems. Indeed, it is already difficult enough to handle the available languages. Now, however, there is Nial, a very high level, fifth-generation programming language with features that can prove highly beneficial even to the most skeptical software person.

Synthesizing ideas from APL, Lisp, and structured and functional programming, interactive Nial (a mnemonic for nested interactive array language) is a functional language. Like Lisp, it allows creation of new operations and transformers, and can treat programs as data. Like APL, Nial is terse, and based on data objects that are treated as arrays. But, unlike any other language—even array-handling ones—Nial carries the array-as-data-object concept further. It can easily work with nested arrays or arrays of arrays.

Nial applications include expert systems, computer aided design, and data bases. Thus, it has already been used to do chores in logic programming, prototyping, VLSI programmed logic array generation, forms management, and data system design. Designed to operate with such operating systems as AT&T's Unix and IBM's DOS and VM/CMS, Nial has unique debugging tools. It can display the contents of its array-based data structures even as calculations are in progress.

According to Michael A. Jenkins, president of Nial Systems Ltd (Kingston, Ontario), "Software designers who use a programming language as a thinking and design tool to help them develop applications need and will use Nial because it's a good way to improve productivity." As Jenkins told attendees at January's Uniforum Conference in Washington, DC, Nial takes the concern for tedious details and exceptional circumstances out of programming. This is because it is based on general data structures and operations, and simple syntax.

```
# GETFILE - Make a list of lines of characters from a text file.
  Each line of the file is made an item of the list.  Parameter
  required is the file name you wish to read from.


      getfile IS OPERATION Fname  {
         A := open ( Fname "r ) ;
         IF ??~= type A THEN
            Lines := vacate" ;
            Line := readfile A  ;
            WHILE Line ~= ??eof DO
               Lines := Lines append Line ;
               Line := readfile A ;
            ENDWHILE ;
            close A ;
            Lines
         ELSE
            A
         ENDIF
         }
```

Nial provides library scripts for use within the system. These are documented in its help facility and can be accessed using the "library" operation. The sample shown is designed for file handling.

An extensible language

Perhaps most important for the designer using Nial as a thinking tool is that the language is extensible. Like Lisp, its software mechanisms allow newly created operations and transformers to be used in exactly the same ways as predefined ones. The new operations, Jenkins explains, are "created incrementally either in successive interactions or by reading a script file containing definitions."

New transformers—functional objects that map operations to operations to define new operations—are created in a similar way. A transformer is applied to an operation to form a result operation called a transform. "There is no evaluation in such an application," Jenkins says.

Nial was designed by Jenkins and Trenchard More, Jr of the IBM Scientific Center (Cambridge, Mass). According to Jenkins, the language is based on More's theory of nested arrays as data objects. This theory serves as the data manipulation model in the Nial system and also provides the definition for the language's data operations.

However, Jenkins says that the Nial user need not know array theory. "On the contrary," Jenkins notes, "the language is suitable as a first programming language for students with no programming experience and could replace Pascal because it teaches even better programming habits." For example, besides containing the control-structure capabilities of Pascal, Nial goes steps further and encourages the decomposition of problems into functional units. Each unit is implemented as an operation. Thus, a problem solution is readily structured along functional lines.

Jenkins does admit that Nial's terseness—like APL—and its symbol

(continued on page 30)

Lisp/APL merger
(continued from page 29)

```
putfile IS OPERATION Fname Lines {
    A := open ( Fname "w ) ;
    IF ??~= type A THEN
        ITERATE A writefile Lines ;
        close A ;
    ELSE
        A
    ENDIF
    }
```

In this example of Nial file handling, #PUTFILE puts a list of character strings into a file. Here, each item of the list is one line in the file. Required parameters include the file name and a list.

manipulation capabilities—like Lisp—require mathematical concepts unfamiliar to the beginner. He insists, however, that these potential problems can be overcome by appropriate documentation.

Problem-solving aid

In Nial, an operation can be applied to any kind of data. Thus, it is ideal for experimenting with problem solving. Programmers can try a possible command and learn immediately if it is correct. Interpreted Nial, like APL and Lisp, executes each of its input commands immediately. In short, programmers can see how the data is transformed by the operation they are defining.

The advantage of this language design is immediacy. When all the statements required to solve a problem have been proven, the log of the programming session can be edited. Only those commands that worked are edited into the final program. As Jenkins points out, "It is this interactive environment, an extensive list of commands, the symbol-handling capabilities of Lisp, and the use of nested arrays that combine to make the improvements in programmer productivity and problem understanding that Nial offers."

Nial's portable implementation, known as Q'Nial (developed at Queen's University in Kingston, Ontario), uses standard unix files, an editor of the programmer's choice (including the Berkeley Unix VI), and Unix commands from within Q'Nial.

The Q'Nial interpreter is written in C and, as might be expected, parameterizes machine dependencies to allow simple host operating system interfaces. Originally developed on a Digital Equipment Corp VAX under the University of California at Berkeley Unix 4.1 BSD operating system, it will be ported to seven other systems this year. These range from the low end IBM PC to the large scale IBM 4341 system.

Q'Nial interfaces with Unix for file management, text editing, and command processing. Moreover, it is possible to call any Unix utility and have it create or modify a Q'Nial-accessible file. This open design means that Nial also works with software written in other languages. Its user can pick and choose the appropriate language and program for the problem at hand.

Design philosophy

Nial is designed as an interactive language with both an immediate execution mode and the ability to execute extensive program texts read from text files or loaded as predefined operations. It is an expression-based language—thus, the unit of computation is an expression that returns a value. The expressions are written in a syntax based on common mathematical notations. Moreover, they are combined with the linguistic constructs common to most programming languages.

In Nial, the result of an expression evaluation is an array. In the immediate execution mode, this is displayed as a picture on the user's terminal. The picture shows the structure and content of the evaluation result. This aids programmers in understanding the data structures that they input and the results of their manipulation.

Such a programming aid is quite unusual and has only been available in such debugging tools as Microfocus's Animator, and some tools developed at Brown University. The picture is not shown during program execution (except in the immediate execution mode) and does not affect program execution speed.

For flexibility, Nial need not only be used in the immediate execution mode, but can be used in a command-oriented way. Thus, an expression may be viewed as an imperative by ignoring its result. Nial furnishes the syntax for this suppression.

Nial execution occurs in a work space containing the data and objects defined by the user. For convenience, access to outside-the-work space data and programmed interaction with the terminal are provided by system operations for input and output. The host system interface edits all program text.

System operations also provide the linguistic mechanisms used to translate program text to Nial internal forms. In addition, a built-in syntactic mechanism converts program text to Nial internal form for use in program construction under program control. In short, as mentioned earlier, the user can treat program text as data, much like in the functional language Lisp.

A step forward

Nial combines the features of Lisp and APL in a manner that supports the so-called functional programming proposed six years ago by renowned computer scientist John Backus. Backus was attempting to define a way to liberate programs from the style imposed by von Neumann architecture—and Nial is an implementation of some of his ideas.

A major advantage of Nial is the direct way it captures the inherent parallelism of an algorithm. Thus, like Lisp and Prolog, Nial is a candidate language for the fifth-generation parallel computer architectures being developed in laboratories worldwide.

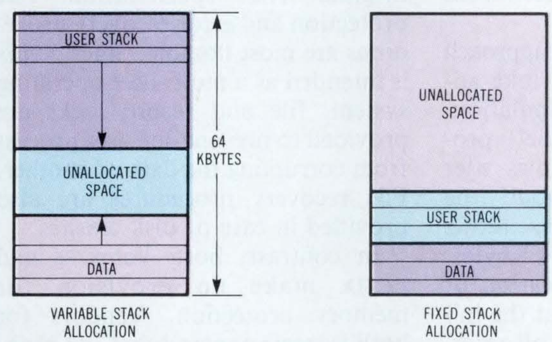
A binary object-code license for the VAX version of Q'Nial ranges in price from $1600 to $8000, depending on the number of system terminals supported. Clearly, Q'Nial is not a casual purchase and this fact is recognized by an evaluation license being available at a lower cost. Prices range from $400 to $10,000 for other binary object-code Nial versions that run on the Xenix, Unity, PC-DOS, Tops 20, and VM/CMS operating systems. Finally, $25,000 buys the source code.

—Harvey J. Hindin, Special Features Editor

Mainframe-style tools move down to personal computers

Unix ports to the IBM PC promise mainframe-style software development support at a relatively low cost. Programs and utilities, such as source-code debugging (sdb) and lint (portability analysis), previously found only on larger machines, ease the task of high level language programming on personal computers. Multitasking capability is thrown in as an extra benefit.

Unix comes in various flavors on the IBM PC. Both the Personal Computer Interactive Executive (PC/IX), from IBM's Information Systems Group (Rye Brook, NY) and Xenix, from Santa Cruz Operation (Santa Cruz, Calif) base their versions on AT&T's Unix System III. VenturCom (Cambridge, Mass) bases its Venix/86 port on the earlier version 7 release. These ports have been enhanced with utilities taken from other Unix versions (eg, Berkeley 4.2) as well as modifications (eg, file and record locking) not found in Unix itself. Such variety may diminish as these vendors move toward the System V specification favored by AT&T.



Instead of variable allocated user stacks, as is typical in Unix implementations, most IBM PC-based Unix ports implement fixed-size stacks to reduce the size of unused memory.

Portability problems

There is, however, no completely efficient way of moving Unix to the micro world. Users of PC-based versions must sacrifice some performance in exchange for the power provided by the utilities and multitasking capability. Myron Zimmerman of Interactive Systems (Santa Monica, Calif), architect of the PC/IX kernel, notes that computation-bound or disk-bound operations will execute more slowly on personal computers than when executed on larger multi-user hosts. On the other hand, he notes that interactive tasks such as text editing have better response on a personal computer.

Its beginning as a minicomputer operating system makes Unix oriented toward machines that offer multitasking support in hardware, rather than microprocessors like the Intel 8088 that are most efficient at executing single programs. Most visibly absent in 8088/8086 processors are extensive memory management hardware and the lack of separate supervisor and user address spaces. As a result, Unix ports to the PC modify algorithms implemented in the original kernel to overcome the limitations and optimize performance.

Hardware limitations imposed by the PC affect the system user stack most. In typical Unix implementations, the user stack containing information about current processes starts at the highest logical data address and actual data starts at the lowest address. The user stack grows down and data grows up, yet both are contiguous in physical memory. As a result, addressing logical memory between the user stack and data becomes infeasible.

The technique balances space efficiency versus time efficiency, since it requires additional memory to be added on demand. However, all Unix versions running on the PC allocate a fixed 64 Kbytes of memory for both the user stack and data when programs are declared variable stack. (This is because the 8088 processor has only two programmable address registers to mark the starting location in memory and an offset from that start.) Portions of a segment cannot be mapped to a different starting location. Thus, the user stack and data cannot be swapped in and out as their sizes increase to exceed 64 Kbytes.

In addition, much wasted space exists within a user segment if the user stack and data are small. To minimize the "doughnut hole," all PC versions also place the user stack immediately above the user data. This requires, however, that the maximum runtime size of utilities and runtime libraries be determined and declared as fixed stacks.

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Mainframe-style tools

(continued from page 31)

Beyond the lack of memory management hardware is the lack of a nonprivileged mode that separates user operations from supervisor operations handled by the kernel. This is typically handled through different logical address spaces. As a result, any user process can alter its base registers and perform operations anywhere within main memory.

Bypassing this obstacle, PC/IX calls for programs to be written in a "small" mode, whereby the program never modifies all segment registers. This limits program size to 64 Kbytes, but allows these registers to separate user processes from kernel operations.

Both Venix/86 and Xenix approach the problem differently to take advantage of segment manipulation. Both implement a "middle" programming model that allows user processes to dynamically modify the code segment register. This allows code segments to exceed 64 Kbytes. However, the physical location of the code segment is fixed at the initial program loading, and all references to the code segment are fixed to that location. Likewise, the code segment must always swap to that location because physical relocation is not supported with hardware mapping.

To implement memory management within this scheme, Venix/86 breaks a large code segment into smaller pages. This facilitates code swapping, and a mapping table is always resident in memory. In contrast, both PC/IX and Xenix implement no such scheme for code swapping. All three ports limit user data as well as text spaces to 64 Kbytes each.

Comparisons of Unix Ports to the IBM PC

	IBM PC/IX	SCO Xenix	VenturCom Venix/86
Unix-licensed versions	System III single-user	System III multi-user	Version 7 single- or multi-user
Suggested memory requirements	512-Kbyte RAM, two 10-Mbyte rigid drives	384-Kbyte RAM, one 10-Mbyte rigid drive	256-Kbyte RAM, one 10-Mbyte rigid drive
Suggested no. of users	1	2 to 3	2 to 3
Memory protection	none	File/record locks	none

Implementation differences

Similar modification schemes in the porting process do not necessarily mean that the kernel is the same size for all versions. On the contrary, kernel size ranges from 50 Kbytes for Venix/86 to over 128 Kbytes for Xenix. Each vendor has also made individual choices on which enhancements it wishes to make to the original Unix version.

Santa Cruz Operation (SCO) has chosen to enhance its System III version with capability not found in the original AT&T specification. File protection and error recovery procedures are most notable. Since Xenix is intended as a multi-user operating system, file and record locks are provided to prevent one user process from corrupting the data of another. File recovery procedures are also provided in case of disk crashes.

In contrast, both Venix/86 and PC/IX make no provision for memory protection. Vendors for both systems contend that the probability of file corruption is so small that it does not justify the extra code needed to implement file protection. Furthermore, file protection might hinder software development (the primary application area for both systems) because programmers desire free access to physical resources.

Enhancements to the kernel, such as file protection and floating point support (which all versions handle), directly affect memory requirements, as well as the number of users able to log on to the system. Desired sizes for main memory run from as little as 256 Kbytes for Venix/86 to as much as 512 Kbytes for PC/IX. All three versions work best with one 10-Mbyte rigid disk drive acting as auxiliary storage. A second 10-Mbyte rigid drive with the IBM version is suggested for additional storage.

Within the 256-Kbyte memory configuration, Venix/86 will support as many as three users with reasonable performance. Xenix recommends 384 Kbytes for the same number of users. On the other hand, PC/IX supports a single user with its suggested 512-Kbyte configuration.

Program utilities and software tools take a big bite of the memory not reserved for the kernel (always resident in main memory). The command shells can easily occupy 50 Kbytes, with compilers and editors each grabbing as much as 60 Kbytes. A full Unix system with utilities and shells can take up as much as 6 Mbytes without taking application programs into account.

Furthermore, both PC/IX and Venix/86 allow MS-DOS programs to coexist on the same rigid disk. For example, PC/IX can occupy 7 Mbytes of a 10-Mbyte rigid disk, with the remaining 3 Mbytes reserved for MS-DOS applications. Utilities are provided for file transfers between the two operating systems. This arrangement is why IBM suggests a second rigid disk drive to allow both faster access to programs and data, and also to accommodate larger programs that can reside under each operating system.

System designers evaluating the feasibility of using Unix on the IBM PC should carefully balance the need for a powerful software environment and portable object code (if C is used as the principal language) against the massive memory requirements and slower performance. Cost also plays an important role when these Unix implementations are compared against more expensive engineering workstations and minicomputers. Indeed, you get what you pay for.

—Joseph Aseo, Field Editor

SYSTEM TECHNOLOGY

(continued on page 38)

One-Two Punch!

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CIRCLE 16


NCR
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THE CASE F

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Windows graft multitasking onto single-task operating systems

Trickery best sums up the efforts of a spate of integrated operating environments that fool single-task operating systems into running multiple application programs. Each application program running under these environments assumes it has full access to processor resources, while the operating system sees only one application program running—the operating environment.

Most operating environments choose MS-DOS from Microsoft Corp (Bellevue, Wash) as the host operating system. In addition to the company's own Windows environment, there is Inview from Graphicon Software, Inc (Palo Alto, Calif), DesQ from Quarterdeck Software (Santa Monica, Calif), ConceptVP from Scientia, Inc (Wellesley, Mass), and Visi On from VisiCorp (San Jose, Calif). The UCSD p-System obtained a similar environment with the recent announcement of the Insight window manager from SofTech Microsystems, Inc (San Diego, Calif).

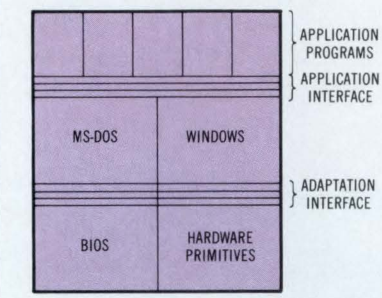
However, there is a price for such flexibility. More main memory and disk memory are required beyond that presently required to run the application programs. Another important consideration centers on the exact mechanism that facilitates data exchanges between programs. Both factors directly qualify their effectiveness.

Memory hogs?

Efficient use of memory is the problem that all operating environments must tackle, since so many critical functions are emulated in software. Both the program state information and the contents of screen buffers must be saved as a user moves from one application to another.

In a real sense, many such integrated environments are operating systems in their own right. They trap system calls issued by each application program in order to redirect keyboard input and screen output to the proper window. Typically, the host operating system provides only the file system and physical device interface.

An effective way to implement this approach gives each application program its own copy of the MS-DOS kernel. This approach is taken within the Inview environment. In this case, all the window manager need do is collect the system calls from each window and make sure the desired action (eg, scrolling) occurs within the proper window. The Insight environment operates in a similar manner for p-System machines.



Microsoft's Windows follows a typical implementation of an integrated operating environment. The application interface provides the necessary hooks to support windowing functions and data exchanges. Likewise, Windows taps the physical resources of the system through the adaptation interface.

Nonetheless, this approach limits the number of applications by the size of main memory. Graphicon advises a 192-Kbyte allotment for main memory, while SofTech recommends 64 Kbytes. Both Graphicon and SofTech concede that only two or three application programs can be opened at one time within their environments, since program state is stored in main memory. Processor registers normally used for such functions are under the control of the host operating system. Unfortunately, single-task operating systems like MS-DOS and p-System do not provide multiple context buffers that integrated environments can manipulate. Thus, increasing the number of application programs also increases the size of main memory.

An alternative to increasing RAM requirements is to swap seldom used data and code segments out to disk. Both DesQ and Visi On take a more ambitious approach by implementing virtual memory techniques to increase the number of active application programs supported, as well as to assume event scheduling from the host operating system. Both maintain context registers in main memory for each application program currently active to save program state information and screen buffers. In addition, they implement least recently used algorithms in order to swap out dormant data segments in much the same manner as the multitasking operating system Xenix.

However, virtual memory increases the code size of the integrated environment. Address translation tables must also be kept in order to match disk addresses with their main memory counterparts. Moreover, both Visi On and DesQ require 512 Kbytes of main memory, as well as 5- or 10-Mbyte rigid disk drives.

Potential drawbacks to either approach move the other packages to a middle-of-the-road method. ConceptVP and Windows implement an event scheduler within their systems rather than duplicate copies of MS-DOS, as Graphicon does. Both environments also swap seldom used data and code segments to disk, but stop short of implementing virtual memory techniques. Although the main memory requirements hover around 256 Kbytes, auxiliary storage can be provided with floppy disk drives.

Considering data interchange

Memory utilization addresses only one side of the picture—the environment itself. Effective exchange of data between programs addresses the idea of program

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CIRCLE 22

Windows graft multitasking
(continued from page 38)

Integrated Environment Comparison

	Host Operating System	Suggested Configuration	Data Interchange Formats
Graphicon Software Inview	MS-DOS	192-Kbyte RAM, two 320-Kbyte floppy drives, and graphics controller	ASCII (format conversion planned)
Microsoft Windows	MS-DOS	192-Kbyte RAM, two 320-Kbyte floppy drives, and graphics controller	SYLK ASCII Binary
Quarterdeck Software DesQ	MS-DOS	512-Kbyte RAM, 5- or 10-Mbyte rigid disk, and graphics controller	Handles format conversions
Scientia ConceptVP	MS-DOS	256-Kbyte RAM, two 320-Kbyte floppy drives, and graphics controller	ASCII
SofTech Microsystems Insight	p-System	64-Kbyte RAM, two floppy drives	ASCII
VisiCorp Visi On	MS-DOS	512-Kbyte RAM, 5- or 10-Mbyte rigid disk, and graphics controller	DIF ASCII Binary

integration. At issue is the ability to pass format-dependent information from one program to another. For example, passing cells from a spreadsheet for incorporation in a table created on a word processor requires positional information (ie, fourth column and fifth row) to be passed along with the numbers contained in the cell.

Several environments pass only certain types of data between programs (eg, ASCII text strings), while others can convert data from one format to another (eg, ASCII to integer). The major obstacle to data interchange centers around one program's ignorance of another program's data structures. Tables constructed by a word processor, for instance, have no numerical values—they only represent character strings. Passing these tables to a spreadsheet program would have little meaning since most spreadsheets have no concept of what a text string is. In order for a useful data exchange between two different programs, there must be a way to add knowledge about data structures and functions to each program.

There are three schools of thought on this matter. Visi On and Windows favor adding such knowledge to the applications, and using the operating environment as an arbiter. On the other hand, DesQ and Inview lean toward putting such intelligence in the operating environment, so that it handles any necessary format conversions during the transfer process. Finally, ConceptVP and Insight provide for intelligence in neither the application nor operating environment, and essentially pass information in a cut-and-paste fashion using text strings.

The first approach implements object-oriented programming concepts. Each application program is an object that sends and receives messages. In addition, data messages are separate from the program operations that manipulate them. This separation permits the programmer to define the way in which data is passed between objects.

Visi On and Windows define general classes of data that will be passed between programs: application-specific (eg, DIF or SYLK) information such as formulas used in spreadsheets, ASCII text strings, or unformatted binary code. It is up to individual application programs to specify which data classes they will accept from or send information to. The operating environments then arbitrate to find a common format for data exchange.

In order to effectively implement this scheme, application developers must have the tools to build such intelligence into programs. Existing applications also require modifications to add data exchange capabilities. Tool kits are available for these purposes, as well as to make full use of the window manager's capabilities as pop-up menus or mouse pointing devices (see *Computer Design,* Feb 1984, p 52).

The latter approach, favored by DesQ and Inview, assumes that application programs have no knowledge of data types other than those they already use. However, users can teach the window environments how to transfer data between these programs by going once through the transfer procedure. Users can then initiate future transfers with a macro command.

In this scheme, users first pick data in one program manually, perform any necessary format conversions within the window environment, and place the data in the desired location. For example, a user can teach DesQ to grab columns from a table created on a word processor (including column and row headings) and transfer the information to a spreadsheet with the row and column headings reversed. Although more time consuming initially than the first approach, this learning mode permits existing applications to readily operate in a windowed environment without modification.

Choosing the package

Prospective users evaluating these packages should take several factors into consideration. The need to integrate existing applications into a single environment might favor packages that support learning modes if free data interchange is desirable. New application programs can be developed using either

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Windows graft multitasking
(continued from page 40)
interchange approach since tool kits are available for both types. The concept of data classes may appeal to developers who want well-defined interfaces to their applications.

Likewise, memory requirements directly affect the operating environment's overall performance. Virtual memory implementations work best in applications that have the user constantly switching between several large programs (eg, spreadsheet, database manager, and graphing programs). Here, disk swapping can adversely affect response times. Less memory-intensive packages shine more brightly if application requirements dictate that existing systems be supported, or if data exchanges between programs rarely occur. In short, users must carefully match application requirements with the capabilities of competing operating environments.

—Joseph Aseo, Field Editor

Operating systems contend for position as industry standard

Several operating systems are competing to become the standard for micro and minicomputers in distributed computing environments. Of these, Unix, from AT&T's Bell Labs (Holmdel, NJ) has probably received the most attention, but Pick, from Pick Systems (Irvine, Calif), and RM/COS, from Ryan-McFarland (Rolling Hills Estates, Calif) provide interesting choices. All, of course, run on both micro and minicomputers, and are not tied directly to a hardware manufacturer, but each has its own strengths and weaknesses that warrant serious consideration during multi-user system design.

Of the three operating systems, Unix and its clones have received the most attention. While Unix may draw the most notice, it has probably also had the most programming hours spent on fixing, extending, and transferring it to other machines. Created originally as a programming tool, it is almost universally used by programmers.

Straight talk about Unix

Unix has virtually every conceivable tool and trick built into it (the standard set of Unix files runs to several megabytes) and supports most programming languages. It is also written in C, a very good system programming language, for which compilers exist on almost every computer made. Moreover, it is endlessly modifiable (a large subculture of programmers—proudly dubbed "Unix hackers"—specialize in tinkering with the internals), and is terse (two- and three-letter commands, usually unpronounceable, are common).

On the other hand, non-programmers do not like Unix. It is so complex that nobody can be expected to understand it in a finite period of time; it hogs precious space ondisk, and is written in C—a far cry from Cobol, in which most applications are written. The whole system has a bad habit of changing completely every time a new system programmer works on it, and the list of commands might as well be in Shqip (Albanian)—which even looks like a Unix command. The supplied documentation, by its sheer weight and incomprehensibility, is guaranteed to give an English major a hernia and hysterics, not necessarily in that order.

On the positive side, the Unix "shell"—that section of the system the user sees and deals with—can be changed. Instead of cryptic abbreviations and mind-boggling lists of parameters, English (or French) menus can be displayed, and numerical responses can be translated into command sequences that the system understands. Several Unix vendors are working on user-friendly shells, but no standard exists, and there are very few patterns.

Another strength is that Unix is a multi-user and multiprocessing system. One copy of it, running on one machine, can handle several users simultaneously, and each of the users can run several jobs (eg, editing text files, and compiling programs) concurrently. A hierarchical file structure exists whereby each directory can have one or more subdirectories, which can in turn have their own subdirectories. This lets the programmer group sets of related files together, instead of having to pick out the needed files from a long (and possibly confusing) compiled list. Both of these facilities are being integrated into modern microcomputer operating systems, and will probably become standard in time.

A standard facility (called "uucp") transfers files between Unix systems via telephone. Several vendors of Unix variants have built in interfaces to local area networks (LANs) such as Ethernet. The system thus has the potential to operate as a true distributed processing environment, where data and programs can be passed around at will, and processed as needed.

From a hardware standpoint, Unix needs a fast processor, lots of memory, and extremely fast disks to operate satisfactorily in a multi-user environment. Several programs can run in memory concurrently, but when one must be halted for some reason, the entire program and data are swapped out to disk. When it can run again (ie, when some other program has ended, or stopped temporarily), it must be reloaded from disk, and reconnected to the operating system. The disk, along with its data transfer rate, is thus the critical resource in a Unix system.

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CIRCLE 24

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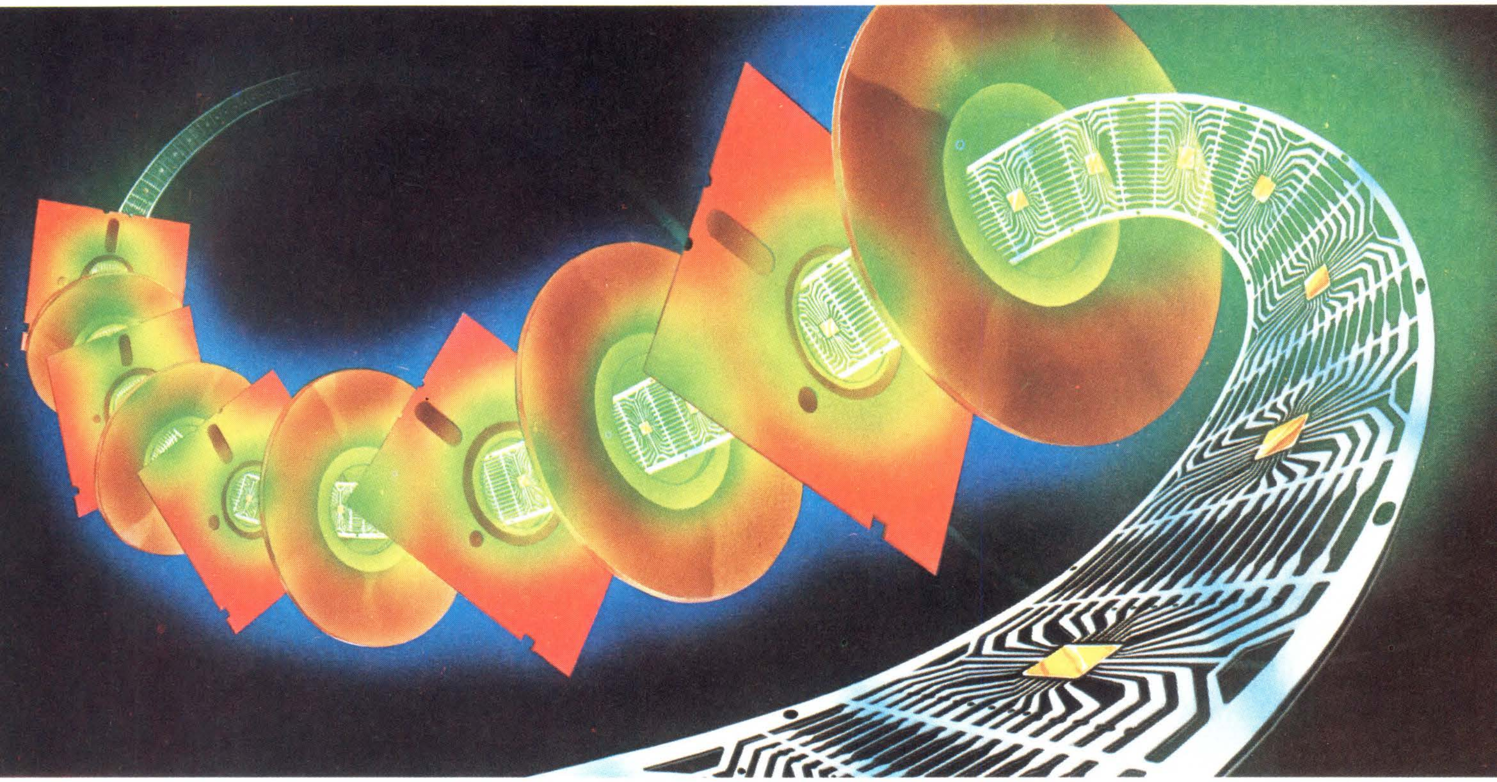

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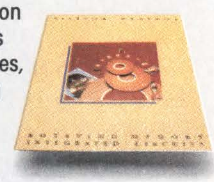

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INNOVATORS IN INTEGRATION

CIRCLE 25

Operating systems contend

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Microcomputer implementations of Unix are likely to show noticeable response degradation with more than 6 heavy users, and unacceptable response with more than 12.

Overall, Unix is an extremely good environment for creating software, but a frustrating one to use it in. As a conservative estimate, it would take as much (or more) time and money to create a good user interface and documentation, as it would to create the applications to be run with it.

Pick—a useful system

As a business system, Pick is a stable, useful tool with a great many application and utility programs, and has an enthusiastic group of users. It has been built up over the last 10 years from a database system for IBM computers to a full-fledged system that runs on machines from several manufacturers.

Like most modern microcomputer operating systems, it takes its input from terminals rather than cards or tape, and uses commands that are a recognizable subset of English. The system documentation describes the commands as "verbs," and—like English nouns—file and program names can be of almost any reasonable length. This is an advantage over systems such as CP/M and MS-DOS, which limit a file name to eight characters, with a three-character extension.

While the system itself is transportable (with difficulty—it is completely written in assembly language for each new machine), programs are definitely not transportable to other systems. Most programs are also written in assembly, and therefore will not run on Pick implementations that run on different manufacturers' hardware. The rest of the programs are written in a proprietary business-oriented dialect of Basic. These should prove transportable (in source-code form, at least) if there are no media or formatting incompatibilities between the two different systems.

No other languages are offered (in particular, not Cobol), and the vendor shows no special interest in implementing them. This, together with the lack of transportability, limits the number of available application programs, as well as the number of third-party vendors who will see it as in their interest to produce software for Pick-based systems.

There is no mention made of networking or interactive file transfer in the system documentation, although with some care, it should be possible to make one Pick system act as a terminal on another. There should also be the potential to define a LAN as a disk-type storage device that can be shared between systems. However, no such standard device is defined on all systems, and it would have to be built from scratch.

Pick seems to be a good multi-user system for medium to large businesses, as well as for divisions within larger corporations. It is, however, expensive to implement *de novo* on new hardware, and does not meet the criteria for program and data transportability, or for the availability of many software packages from outside vendors.

RM/COS caters to small systems

Ryan-McFarland's commercial operating system (RM/COS) does not pretend to be a general operating system. It was designed expressly for the execution of Cobol applications on small business systems, according to the sales literature and documentation. In addition, it supports all software written in the vendor's RM/Cobol, and is available on systems built around the Texas Instruments 990 and Motorola 68000 processors.

Given this limitation, it seems to be a well-designed multi-user, multitasking system. It supports hierarchical directories, record locking (two users cannot access the same file simultaneously), and has optimized its file types to conform to the requirements of Cobol.

Files can be shared interactively between two or more users or application programs, which at least makes distributed processing via a LAN possible. The thoroughness with which the system features were designed indicates that building LAN

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Operating systems contend
(continued from page 45)
connections should not be technically difficult, despite the lack of mention in the documentation.

The Cobol around which the system is built is standard ANSI 74. This means that source code for programs written in it on other machines should compile and run with few or no changes (given media compatibility, of course). In addition, RM/Cobol is available as a standalone language on most 8- and 16-bit microprocessor systems, as well as IBM mainframes.

Thus, application programs should be widely available. Indeed, a portion of the company's sales documentation includes a listing of available applications and the names and addresses of the third-party vendors. The key phrase when evaluating RM/COS is "small business systems." By not trying to produce a general operating system, the vendor has evidently succeeded in serving its carefully chosen customers.

—*Sam Bassett, Field Editor*

Objective C bridges gap between Unix and artificial intelligence

Object-oriented programming techniques reduce application-dependent code, resulting in simpler, more reusable routines. These techniques, as applied in artificial intelligence systems, allow programmers to build natural user interfaces that correspond closely to the problem's structure. Objective C allows these same techniques to be applied by programmers using the C language within a Unix environment.

Objective C, brought to light during the swirl of activity at Uniforum (the recent international conference of Unix users), extends C to include many of the constructs used in Xerox Corp's artificial intelligence (AI) language—Smalltalk. Dr Brad Cox, vice president of Productivity Products International (Sandy Hook, Conn), designed Objective C for programmers working in a Unix environment. Since it consists of extensions to the C programming language, Objective C effectively bridges the gap between object programming and conventional C programming under Unix.

Object-oriented or symbolic programming is an AI technique used to manipulate objects or at least the symbols (eg, words or numbers) that represent those objects. The technique was developed by AI researchers to emulate the way people think about things. This is accomplished by encapsulating not only the object with the operations natural to its type, but also by encapsulating the object's characteristics and relationships to other objects. Thus, each object is a small data base containing not only the object's description, but also those operations that it can perform. When an object receives a message that specifies one of its encapsulated operations, the object performs that operation.

Consequently, an object infers much more than its name or symbol. It categorizes and implies a range of behavior and characteristics, according to its nature, as in our own natural language. Several object or symbolic processing languages are now available. These include languages such as Lisp, Prolog, and Smalltalk.

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Objective C bridges gap
(continued from page 47)

Unix—ubiquitous but not yet uniform

The 8000 attendees, 150 exhibitors, and other true believers at the Unix conference, Uniforum, need no convincing that Unix will emerge as the standard operating system of the computer industry. To further dispel doubt, AT&T (New York, NY) is now taking a much more aggressive stance in developing and supporting Unix. Along with an enhanced version of Unix System V, AT&T announced a cooperative relationship with Digital Research Inc (Pacific Grove, Calif) to expand application software. One specific project is an application library focusing on well-supported, sophisticated, and portable applications. Independently developed applications from different companies will be standardized and marketed by Digital Research.

Digital Research further expanded its commitment to industry standard software in a joint announcement with Motorola to develop software for the M68000 family in Unix System V, CP/M, and Concurrent DOS (a multitasking operating system that provides PC-DOS support). Languages and utilities are being written in C to provide application portability across these operating systems, thus providing an entry into the Unix world for 68000-based machines using smaller operating systems. Since Digital Research has ported Unix to other micros as well, the developing trend is clear: applications will be processor independent and transportable from personal computer-type operating systems into the Unix world.

As a step in that direction, IBM introduced a new Unix-derived operating system for the PC/XT. Called PC/IX, it was developed by Interactive Systems Corp (Santa Monica, Calif). Other Unix-based systems for personal computers abound. It is paradoxical that, in the drive for industry-wide operating system compatibility, so many versions of Unix have appeared that it threatens the very standardization sought. Of course, the biggest contender to Unix System V is the University of California, Berkeley Unix (4.2 BSD). Derived from AT&T's Unix System III, this is a virtual operating system and thus has found favor among numerous computer manufacturers. Many of its enhancements have found their way into System V and AT&T expects to offer a full virtual implementation in the near future. That future version of Unix, coupled with AT&T's new emphasis on strong marketing and support, should move the industry a step closer to a single Unix standard.

The principal advantage of object-oriented programming languages is programmer efficiency. However, these languages reduce machine efficiency. Smalltalk-80, for example, costs nearly three orders of magnitude in machine performance. Interactive graphics, dynamic binding, and an automatic garbage collection algorithm take a toll on computer performance although they make the programmer's life easier. (Much of this performance loss can be overcome through special architectures, such as those found in Lisp machines.)

Objective C attempts to bring the most useful concepts of Smalltalk into the Unix environment without reducing performance. Smalltalk-80 set out to revolutionize programming but Objective C attempts to bring about an evolutionary change. Objective C is a hybrid language that allows Smalltalk-type object-oriented programming, when needed, without diminishing the ability to do full C programming. Added tools—objects, classes, messages, and inheritance—are available to the C programmer, but neither efficiency nor access to C facilities is sacrificed. Unlike Smalltalk, Objective C is not intended to provide a user-friendly environment for inexperienced computer users. However, it does enable professional programmers to easily write user-friendly application programs for beginners.

As used in both Smalltalk and Objective C, an object is the thing (operand) talked about, encapsulated with those functions (operators) that can be performed by it. A message specifies which one of an object's operations is to be performed. A class is a description of one or more similar objects (eg, the object "DC-10" is an instance of the class "airplane"). Inheritance is the ability of an object to take on characteristics from its class.

Each class in turn can inherit characteristics from the superclass to which it belongs, and so on until the top level of the hierarchy is reached. There, all the general properties of classes and objects lower in the hierarchy can be described. Objects acquire these properties through inheritance. As powerful a concept as inheritance is for hierarchical structures, it has some drawbacks. Often, classes are not hierarchically related. These cases require a technique called multiple inheritance to allow properties to be inherited across unrelated classes.

Multiple inheritance was first used in the Smalltalk-derived "Flavors," an extension to Lisp. The latest version of Smalltalk-80 features multiple inheritance and Productivity Products International has this technique under development for Objective C as well.

One of the major trends in software today is the spread of Unix into every conceivable computing environment. Another major trend is the development of AI and object-oriented languages to support the growth in AI applications. However, the two trends seemed far apart, until now. Objective C, although not a full-fledged object programming environment, is a major attempt to bridge that gap.

—John Bond, Senior Editor

SYSTEM TECHNOLOGY
(continued on page 53)

There comes a time in the life of an innovative, technology-oriented company, when the corporate name on the door no longer matches everything that comes out through it. Since 1972, the products of Custom Systems Incorporated have changed dramatically. CSI has become the leader in peripheral controllers for Data General and Texas Instruments minicomputers. And we think there's even more we can do as computer technology advances through the '80s and '90s. So instead of CSI, you'll be seeing a new name at the bottom of our controller ads and a new name on one of our corporate doors. That new name is...

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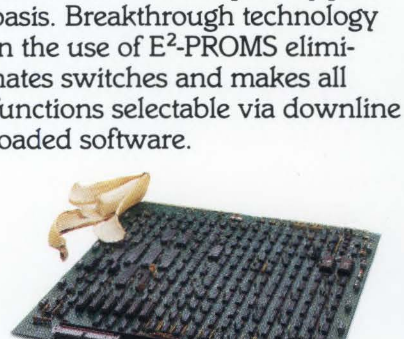

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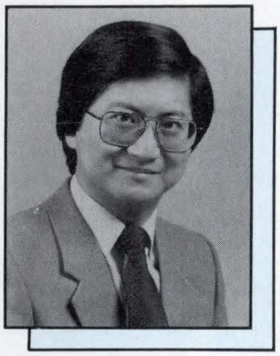
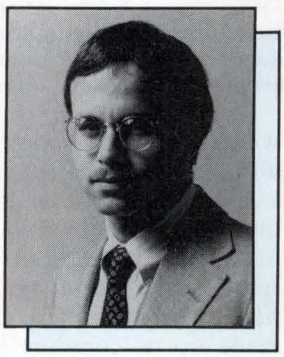
Circle # 12

NAPLPS: a standard for drawing and sending pictures?

Recently, both the American National Standards Institute (ANSI) and the Canadian Standard Association (CSA) adopted the North American Presentation Level Protocol Syntax (NAPLPS) as a standard for coding, storing, and transmitting computer graphics information. The initial effort of the code designers was slated for videotex applications (interactive retrieval service for consumers between their television sets and computer data banks). NAPLPS's features, however, make the standard also appropriate for certain engineering applications.

To review NAPLPS's salient points as well as discuss what NAPLPS is not, Computer Design *asked Bill Chu, vice president of engineering, and Mark Gordon, marketing manager, of Verticom, Inc (Sunnyvale, Calif) to answer the 10 "most frequently" asked questions about NAPLPS. (Verticom develops medium-resolution graphics terminals that are specific to NAPLPS applications.)*


Bill Chu


Mark Gordon

What is NAPLPS?

As a device-independent data format for encoding text and graphics, NAPLPS is ideally suited for information; the protocol is screen-oriented and expresses coordinates as fractions of a unit screen. Known as PLP for short, it is actually a derivative of Canada's Telidon system. Developed by the Canadian Department of Communications, Telidon currently provides agricultural information to farmers. It is the Canadian videotex and is one of the candidates for the North American form of videotex. NAPLPS is in the process of becoming a North American standard as both ANSI in the U.S. and the CSA in Canada are simultaneously moving toward its adoption. By enhancing Telidon, AT&T Information Systems (Morristown, NJ) helped develop the NAPLPS, and has been involved with various trials using it in the U.S.

The designers of this protocol regard it as an example of the sixth of seven layers of the International Standards Organization (ISO) reference model. (The ISO model describes a communication system as a series of seven layers.) Lower layers are concerned with the physical details of establishing and maintaining a link, and with data integrity—eg, RS-232-C and X.25. The seventh and highest layer addresses user application needs. The Graphical Kernel System (GKS) and Core are examples of this layer. The sixth, or presentation layer, of which the NAPLPS is an example, considers the coding scheme or format used to uniquely describe a particular output that a user would view.

Why is NAPLPS important to graphics?

NAPLPS provides the rapidly changing computer industry with an efficient standard for extending traditional ASCII-based applications to include color graphics. With its tremendous coding compaction of graphics information, NAPLPS speeds telecommunications and reduces storage for computer applications.

Because the NAPLPS addresses the sixth of seven protocol levels defined by an ISO model, it is closely oriented to the user's application. Lower levels of this model are concerned with the details of sending bit or byte streams between the ends of a communication link while the highest (seventh) level speaks directly to a user's application.

Thus, this standard is designed with communications in mind and compactly describes text and graphics in an ASCII-based format. The same ASCII codes normally used to represent characters take on more meaning when used under the auspices of NAPLPS. Under certain circumstances, they represent normal characters, under others, specific bit fields within each byte are dedicated to other purposes. In general, 7- and 8-bit codes are used to designate and involve sets of commands or symbols to display.

What are the advantages of NAPLPS for microcomputer graphics?

A graphics frame encoded in NAPLPS typically requires less than 3 to 4 Kbytes. A single floppy disk can therefore store many NAPLPS frames for microcomputer applications. This compact coding is achieved in several ways. One is its definition of high level objects or graphic primitives. These "primitives" are well-known geometric shapes, each of which has a unique code dedicated to signaling the desire to draw it. The attributes of a primitive (color, fill and line texture, size, etc) are controlled by operands or commands received previously.

Examples of primitives are arc (where circle is a special case), rectangle, polygon, and incrementals.

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NAPLPS: a standard?
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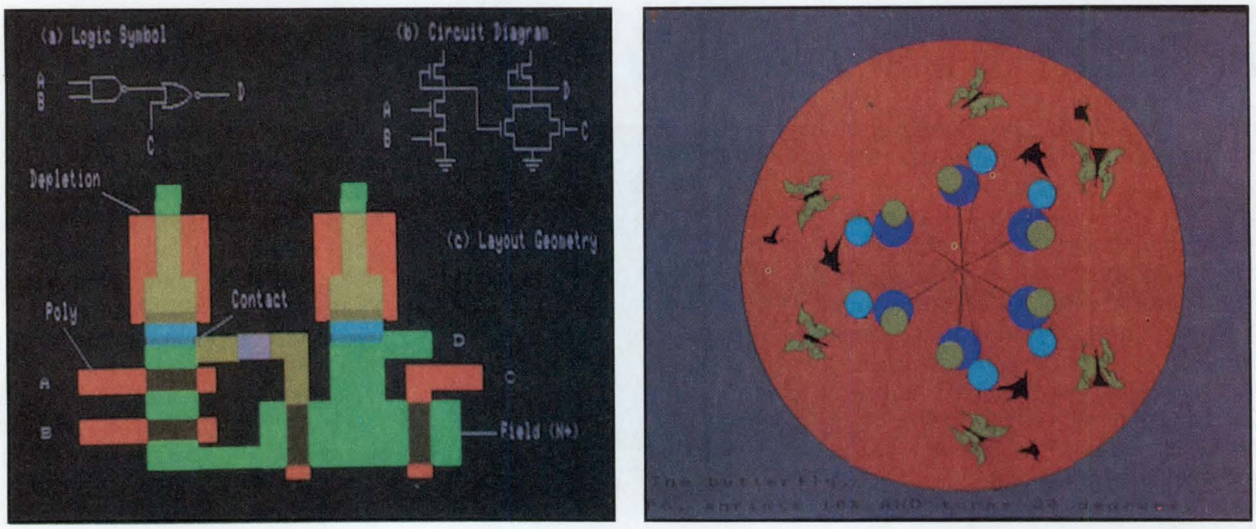

The NAPLPS codes comprise primitives whose attributes are controlled by previously received operands or commands. The primitives are geometric shapes in the forms of an arc, rectangle, polygon, and incrementals. Using these primitives, an operator can generate graphics on the order of these two examples.

The latter, incrementals, actually consisting of three separate primitives, provide a means for compact coding of the following: rasterized images (incremental point); unfilled figures (collections of line segments, such as incremental line or a person's signature); and closed, filled figures consisting of line segment series (incremental polygon). Point and line primitives are also provided.

Another means of ensuring compact coding is the definition of macros as a part of the NAPLPS. These consist of lists of instructions for drawing figures or depositing characters (actually any sequence of valid codes which are given a single character name). A future implementation will have the previously defined list executed by simply placing the 96 entry macro set in the in-use table and multiple copies of identical structures. Significant reduction in the total number of codes transmitted can be achieved by sending macro definitions to the decoding device and then calling the desired macros repeatedly.

Compactness is also achieved by using variable-length coordinates. The NAPLPS permits definition of coordinate values in increments of 3 bits, up to a maximum of 24 bits. Both relative (to the last position at which some action took place), and absolute coordinates are defined. For applications where only a certain resolution is required, data bases may be coded at this desired resolution. Since a significant portion of any graphics data base is made up of coordinates, reducing the size of this data type can shrink the size of the data base substantially. Independence from the resolution of particular output devices is achieved by defining coordinate values.

What are the benefits for a software vendor supporting the standard?

Software vendors have been burdened in the past with writing a large number of device drivers to support proprietary graphics devices. With the device-independent feature of NAPLPS, software and hardware vendors can meet on common ground. In the future, this feature will allow software vendors to develop a single-device driver for all NAPLPS-compatible devices. By defining the output surface (regardless of physical size or resolution) as a unit screen—lower left corner of the screen has a coordinate location of (0,0) and upper right corner has a location of (1,1)—all coordinates can be expressed as fractions of this greater area. Thus, the size and location of objects is referenced to the edges of the screen and not some physical or logical quantity (like the number of dots on the screen or the dimensions of some imaginary coordinate space).

For example, a circle located at the center of the screen whose diameter is one-tenth the width of the screen looks the same regardless of the output device's screen size or resolution. The curve of the circle looks smoother on a device with higher resolution, but its location and size relative to other objects and the screen edges do not change. Thus, pictures coded in NAPLPS can be created at one resolution and displayed at another.

How difficult is it to develop a NAPLPS device driver for existing software?

The development time for a NAPLPS device driver is comparable to that for a proprietary device, typically two months. However, NAPLPS is a powerful graphics standard. Many graphics applications will initially use only a subset of the standard. As stated, one device driver in NAPLPS will work for many different NAPLPS terminals from different manufacturers. Close examination of the NAPLPS reveals
(continued on page 57)

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CIRCLE 41

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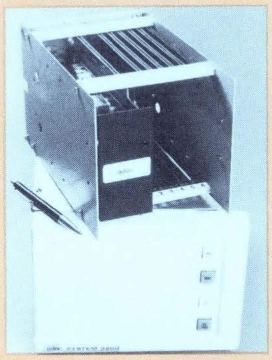
Special Report From adac

New ADAC Systems Improve Q-Bus Performance.

ADAC, the leading supplier of interface boards and integrated hardware/software systems for LSI-11, now offers the industry's broadest selection of Q-Bus system components. Select from the largest collection of backplanes, enclosures and CRT annunciators with unique ADAC advantages.



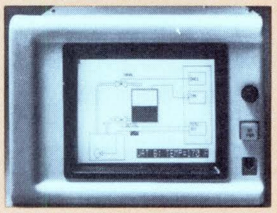
Ultra-Compact Q-Bus Enclosures For Mobile Or Remote Data Acquisition.

Capitalizing on the small size/high functionality of the SBC 11/21 Falcon, ADAC has packed an LSI-11 backplane, power supply and 6-slot half-quad card cage into only 6″ × 6¼″ × 10″ of space. Model 3200 backplane-power supply assembly "nests" the SBC 11/21 Falcon (or LSI-11/2 or LSI-11/23) plus up to 5 I/O, memory, and/or mass storage interface boards in an extremely compact package that is ideal for NEMA enclosures, control consoles, and other space-restricted OEM black box applications.

In addition to being available as an OEM backplane/card cage/power supply assembly for "build-in" applications, the Model 3200 comes as a Q-Bus enclosure with full front panel controls and access in a compact 7″ high × 8½″ wide × 13½″ deep package.

Both Model 3200BPS and 3200M feature 22-bit addressing, power monitoring for orderly up-down sequences and a plug-in power supply module that provides +5V@10A and +12V@1.8A. Powered from AC mains or 24VDC. CIRCLE 197

Unique 7″ Annunciator CRTs Offer Exclusive Text And Graphic Features.

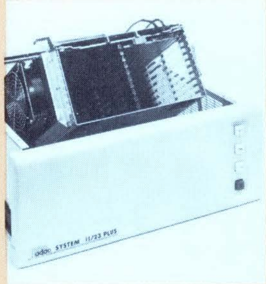


ADAC's new Models 2200CR and 3200CR feature outstanding readibility on a 7-inch CRT. These unique displays offer normal or double-size characters (on a character-by-character basis), bold writing mode, flashing alphanumerics, reverse type presentation and sight-saving green phosphor display.

In addition, Models 2200CR and 3200CR deliver real-time bar graph presentations of temperature, level or other process variable inputs with appropriate scaling or operating limits programmed by the user. Full 512 × 240 bit-mapped graphics is optionally available.

Models 2200CR and 3200CR fill the need for compact, low cost, easily readable CRT annunciators for industrial and scientific monitoring and control applications.

Functionally identical, both models are half-rack width, only 7″ high. The 2200CR is 22″ deep while the 3200CR goes back only 13.5″. CIRCLE 198



ADAC 11/23Plus Offers More Features At 20% Lower Cost Than DEC.

New System 11/23Plus enhances the DEC KDF11-BA CPU with exclusive bus enclosure features such as greater board capacity, more expansion space, more power capability and improved overtemperature protection at savings of more than $1,000 per system when compared with the PDP11/23-PLUS Computer Box from DEC.

System 11/23PLUS provides 19 expansion slots in a 7″ high rack-mounted enclosure. ADAC's universal center card guide allows 9 full quad and 1 half-quad boards, or up to 19 half-quad boards, to be added, providing almost 3 times as much expansion space as the DEC system.

ADAC's System 11/23PLUS features full front access with tilt-up card cage for ease of system set-up and testing. Fan failure detection and overtemperature protection is standard with an output signal for alarming as well as user-strappable orderly system shut-down if desired.

Operating under RT-11, RSX-11M, RSX-11M-Plus or RSTS/E, System 11/23PLUS addresses up to 4M Bytes of RAM and supports 1M Bytes of parity memory. Either 256K, 512K or 1024K Bytes of RAM are included in the basic system, as are two serial I/O lines.

System 11/23PLUS is an excellent general purpose and technical computer system, supporting all LSI-11 compatible peripherals in real time applications. CIRCLE 199

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NAPLPS: a standard?

(continued from page 54)

that it is a very useful mechanism for coding of graphics and text regardless of the application.

Numerous organizations have realized this and are putting it to use. Precision Visuals (Boulder, Colo) writes software packages useful for graphics creation in traditional color graphics markets and has endorsed the NAPLPS and written a device driver that uses it. Several computer aided instruction companies are either currently using it or investigating its usage. One of Verticom's Fortune 100 customers has decided to use the NAPLPS exclusively for coding business graphics used by top corporate executives.

What are the disadvantages of NAPLPS?

No thorough overview of a standard would be complete without some mention of what it lacks. Although the NAPLPS designers did an excellent job, the standard is not without some flaws and implementation dependencies.

As NAPLPS focuses on the definition of text and graphics within a unit screen, a NAPLPS-compatible device cannot be easily used to operate beyond the unit screen. This implies that applications requiring large coordinate systems must perform graphic operations in a virtual coordinate space, at a higher software level. Also, the use of fractional coordinates demands more processing power.

The ease of presenting text is very much tied to a particular implementation. Several predefined (and a nearly infinite number of user-defined) text sizes that specify their height and width as fractions of the output surface are permitted. The number of characters on a line will not vary if one of these sizes is used with an equal intercharacter spacing for all characters. However, the NAPLPS also permits a proportionally spaced test, which is, as the standard clearly states, font, and thus implementation dependent. Thus, the number of characters fitting in a particular space will vary with the font used on the output device. This desirable feature provides more capability at the cost of some portability.

Another area of potential problems is the generation of polygons, whose vertices are defined using a series of relative coordinate specifications. This is done by having the next point coded as an offset from the last point at which something was done. On low resolution devices where unused bits of resolution are usually discarded, significant errors can accumulate if a large number of vertices are drawn close together. This assumes that a host computer keeps a larger number of significant bits than the decoding device uses.

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NAPLPS: a standard?

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For example, an output device with a resolution of 256 x 256 will only look at 8 bits. If the host computer uses 12 bits, and some of the relative moves used to specify polygon vertices only change one or more of the low order 4 bits, the decoder will draw a number of coincident points the host considers discrete.

Even when successive relative moves in the low order 4 bits add up to a move that is significant within the resolution of the decoder, it may not be seen by the decoder (which may ignore the low order 4 bits being sent to it). If the host then draws an identical object with absolute coordinates, the object will not overlap exactly. To avoid such a problem, an appendix to the ANSI specification (the Service Reference Model or SRM) states that a decoding device should maintain coordinates internally to a precision that is greater than that displayed.

What is the distinction among the GKS, the VDI, and the NAPLPS?

Both the Graphical Kernel System (GKS) and the Virtual Device Interface (VDI) are functional specifications at the application software level (level 7 of the ISO model), whereas NAPLPS is a precise, bit-by-bit definition of text and graphics representation at the device level. As previously stated, NAPLPS is at the presentation layer (level 6). A NAPLPS device driver, however, can be written to interface to a VDI.

In general, graphics standards offer a common ground for both the development of graphics software tools (ie, the application program interface) and the interfacing of these tools to graphics hardware. The VDI provides such an interface. The tool standard, such as GKS, define a set of general-purpose subroutines or procedures that can be called from an application program to generate a graphics image. The VDI standard is important to graphics hardware vendors and software developers who must support several devices as part of a device-independent graphics tool system.

Will the industry develop a competing standard to NAPLPS?

As part of the activity to develop the VDI as a standard, the ANSI X343 committee is also formulating the Virtual Device Metafile (VDM) as a text and graphics data format. VDM can potentially develop as a competing standard to NAPLPS in the future for computer aided design/computer aided manufacturing (CAD/CAM) applications. However, much progress still has to be made before VDM will be precisely defined.

Compared to Core's metafile, GKS's VDM has several improvements related to the state of the device at the start of a picture. This allows for redundant information translations, such as time selection of area fill techniques and character quality, as well as binary and character bindings.

Is NAPLPS useful for CAD/CAM/CAE applications?

NAPLPS can be used as an upgrade for Tektronix (Beaverton, Ore) 4010/4014 compatible CAD/CAM and computer aided engineering (CAE) applications. However, NAPLPS's unit screen concept may not be acceptable to high end CAD/CAM/CAE applications.

Tektronix 4010/4014 compatibility offers monochrome text and line graphics capability originally developed for use with storage tube displays. NAPLPS is developed to work with color raster scan CRT displays and offers significantly more powerful instruction sets for color text and graphics display capability. The Tektronix 4010/4014 uses a screen coordinate system of 1024 x 760, but NAPLPS is resolution independent.

There is an implementation dependency worthy of note. It is a fact that the unit screen, which is always one unit wide in the X dimension, may be less than one unit high in the Y dimension. The NAPLPS standard states that the maximum Y dimension must be at least three quarters that of the maximum X dimension. This is to permit display

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NAPLPS: a standard?
(continued from page 58)
of NAPLPS frames on home TV (traditional consumer videotex application) which has always had a 4:3 aspect ratio (maximum Y is three quarters that of the maximum X). However, the standard also leaves the implementor the choice of how large to make the maximum Y dimension (between .75 and 1.0). Generally, created pictures should not have valid data in the Y region above .75 in order to ensure compatibility with the devices that have a 4:3 aspect ratio.

What is the link between NAPLPS and videotex?

Videotex is the consumer information industry that uses NAPLPS in a low resolution (256 x 200 x 4) application. The videotex industry is creating a large NAPLPS data base for the consumer at home to access information through a NAPLPS decoder attached to a TV. Videotex information can therefore be accessed by any NAPLPS-compatible device.

Evolving from the need of the videotex industry to create very large graphics data bases and to mass distribute the information through low bandwidth channels, NAPLPS is well suited for any graphics database implementation on large computers. Currently, NAPLPS provides a viable standard to extend existing data bases to color graphics and should accelerate color graphics database development. For example, a number of companies have endorsed NAPLPS for developing their own data bases. AT&T, now divested of its operating companies, is ready to compete in the computer business and to attempt to maintain its vast lead in the long distance telephone market. The telecommunication potential of the NAPLPS no doubt played a role in its having been enhanced by AT&T.

Tektronix, the major color graphics force, is another endorser of the NAPLPS. A leader in many of the traditional color graphics markets, the company probably perceives this standard as a flexible, nonproprietary interface to equipment which will broaden the graphics market for all. Software suppliers (Microsoft, Digital Research, ISSCO, Precision Visuals, and Graphic Software Systems) also see it as relieving some of the confusion and hard work necessary to permit software to drive various pieces of hardware.

—Nicolas Mokhoff,
Senior Editor

SYSTEM TECHNOLOGY
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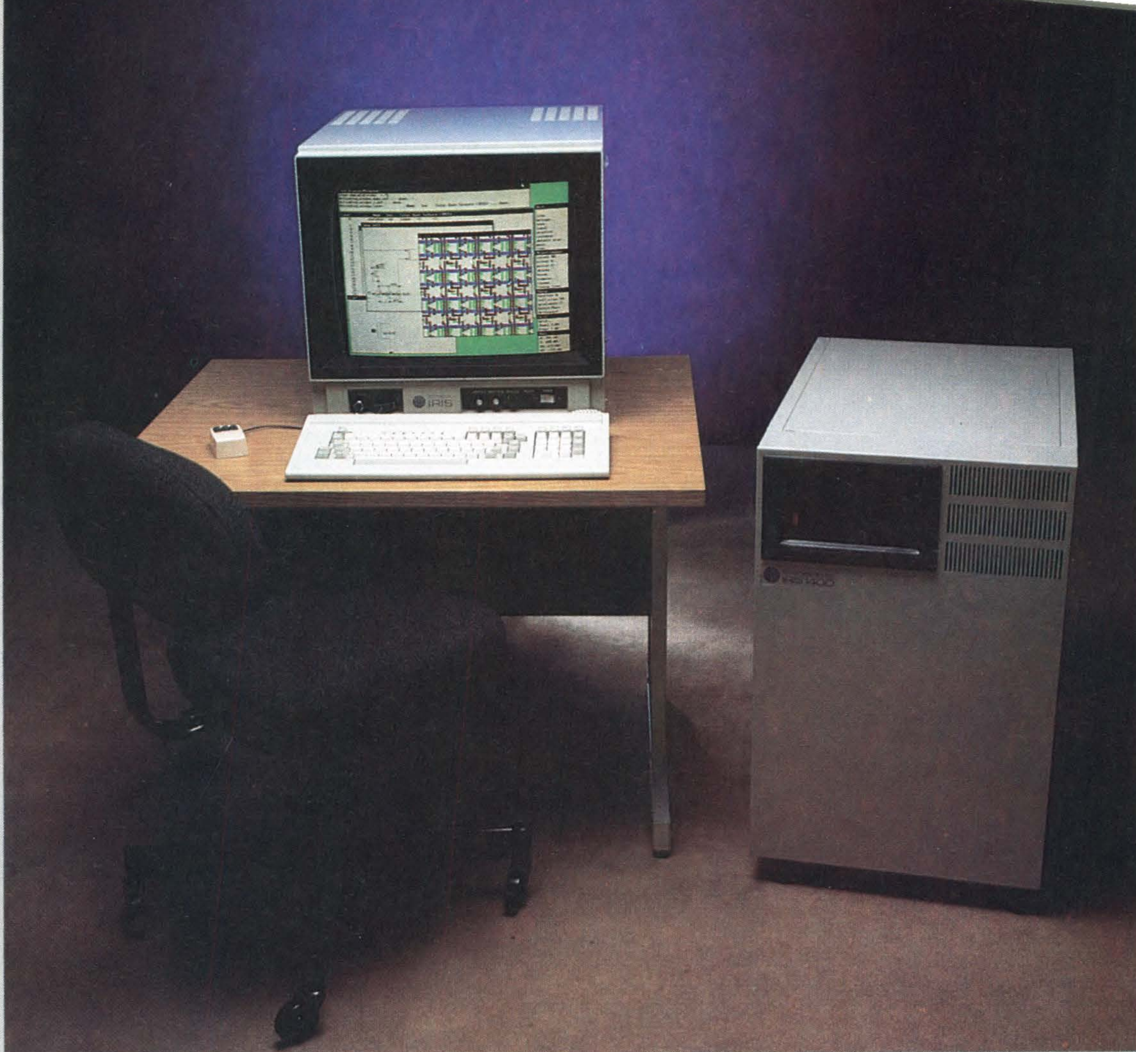

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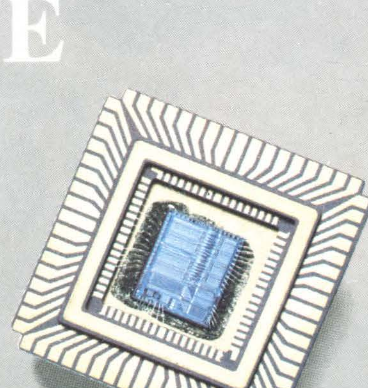

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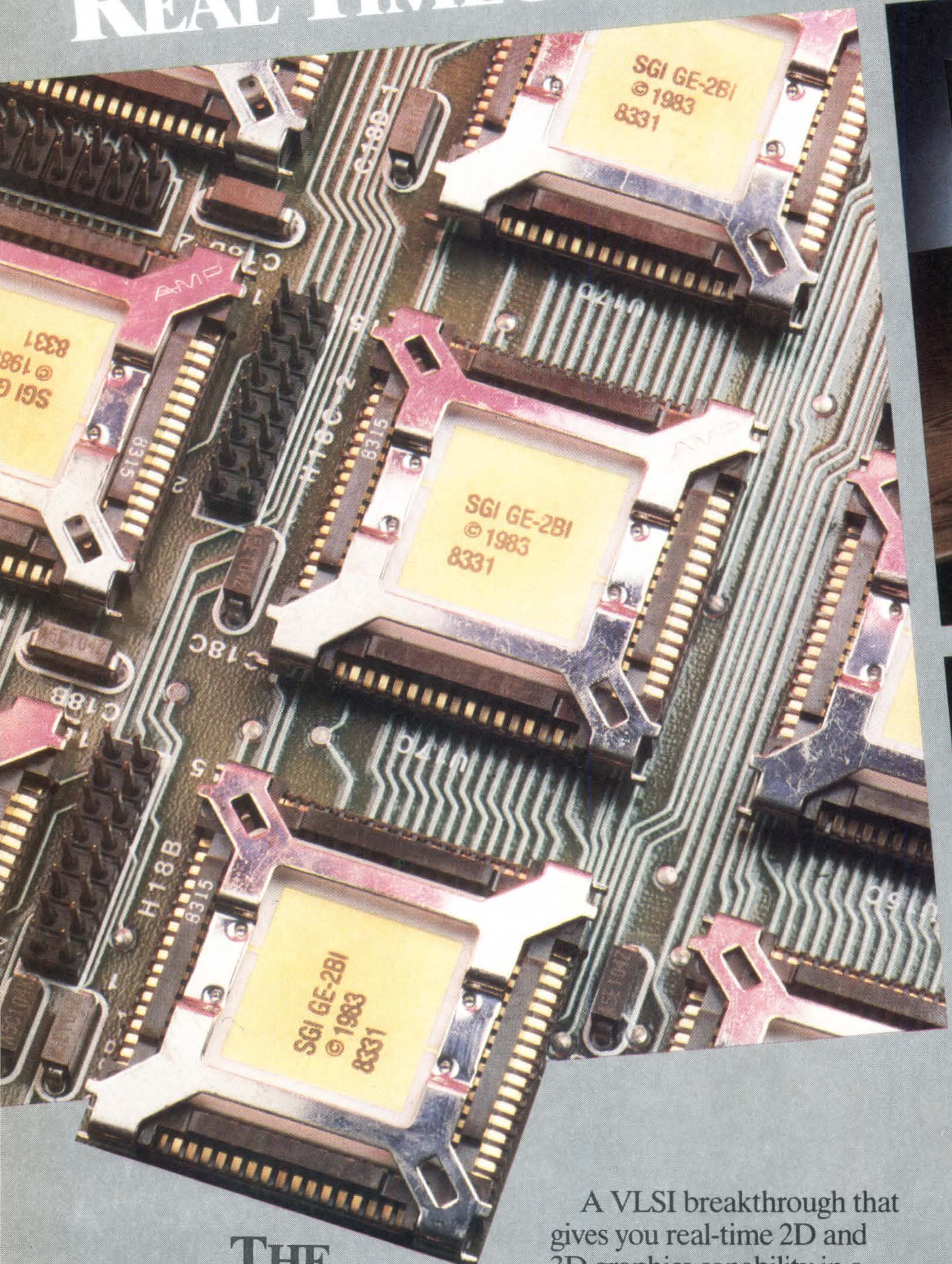

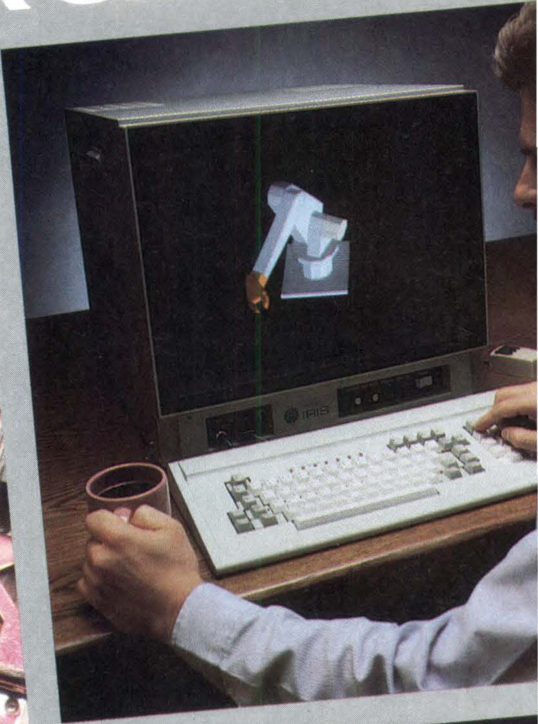

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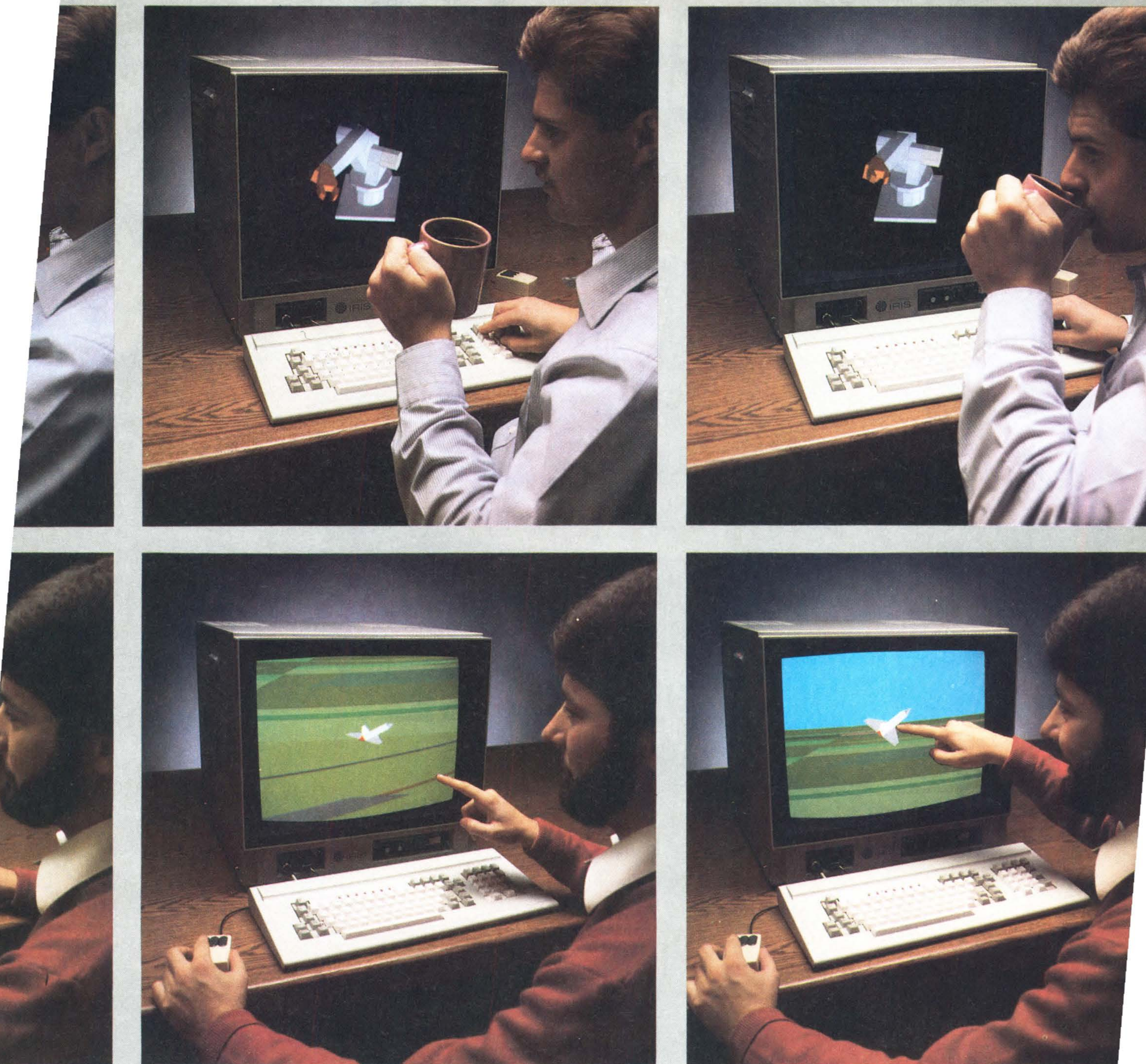

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New UC02 emulating host adapter using Mass Storage Control Protocol (MSCP).

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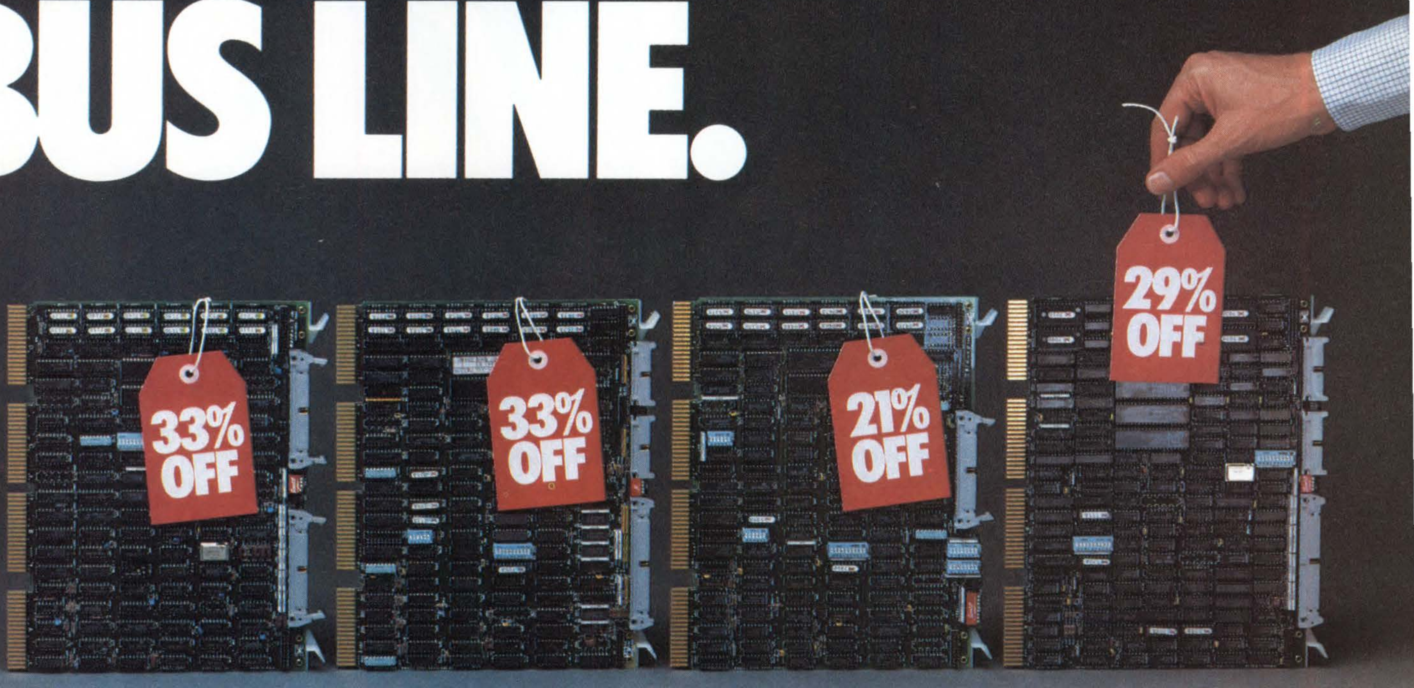

TC02 TS11-compatible tape coupler.

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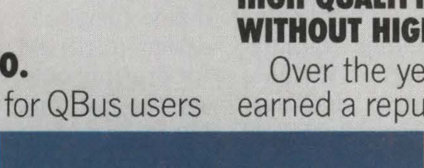

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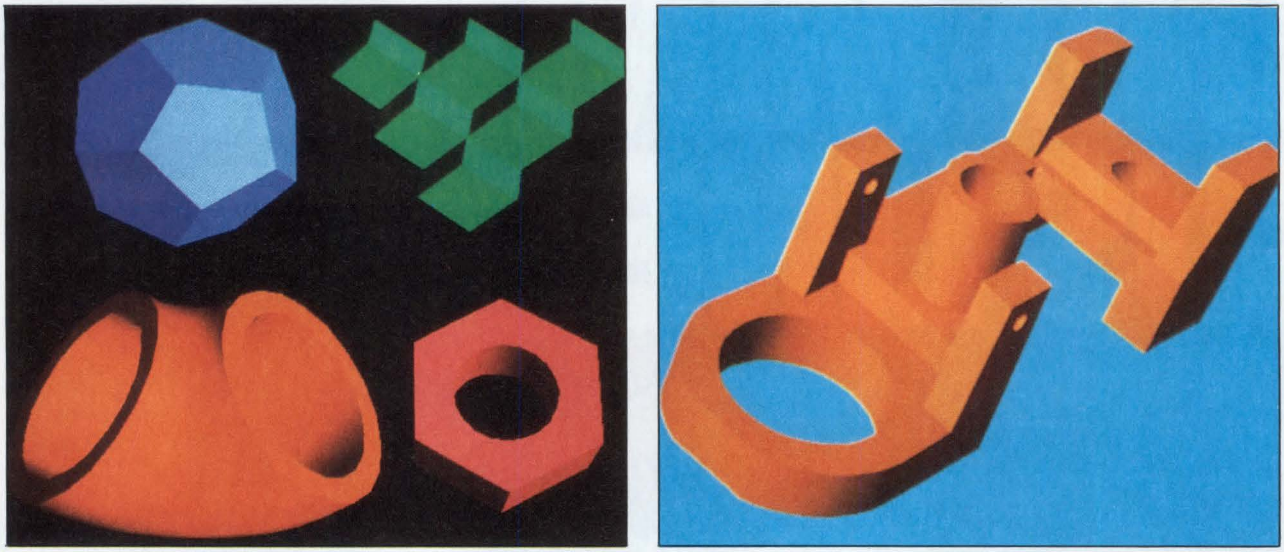
CIRCLE 37

Personal instrumentation takes off in all directions



Using a high resolution color monitor, three-dimensional surface-shaded solid models are created on the IBM PC with the CS-5 design system from Cubicomp Corp.

As personal computers have taken their places on engineers' desks, personal computer-based engineering tools have followed close behind. So-called personal instruments cover a broad range of design/test tools. Although the modest computer systems for which they are designed do not permit these instruments to achieve the high performance of dedicated instruments or design systems, they do keep costs low.

Consisting of add-ins, add-ons, or, in some instances, software packages, these enhancements are relatively inexpensive. Some of the more complex systems, however, compete with engineering workstations in both price and performance. Their main attraction is that instruments or design facilities may be added to the computer on the engineer's desk less expensively than can be obtained with separate systems. Another advantage is that software comes with these systems, whereas systems using the general purpose interface bus (GPIB) may require considerable programming.

Personal instrumentation covers a spectrum of uses including data acquisition, design, system development, and test/analysis. Probably the most established of these applications is for data acquisition systems. It was only a small step from minicomputer plug-in analog/digital I/O boards to personal computers.

A leader in data acquisition boards for the IBM PC, Data Translation, Inc (Marlboro, Mass) makes plug-in I/O boards that sample analog signals from multiple transducers. Joining the trend toward personal computer-based data acquisition are systems from MetraByte Corp, Data Acquisition Systems, Inc (both of Boston, Mass), and Gould (Cleveland, Ohio).

Both the number and type of instruments for test and analysis functions are expanding rapidly. This instrument category includes logic analyzers, spectrum analyzers, waveform generators, oscilloscopes, and data loggers. But, perhaps the biggest expansion is due in the area of system development. There, development systems, in-circuit emulators, PROM programmers, and logic analyzers (to borrow one from the instrument group) are making it easier and cheaper to develop microprocessor-based systems.

A look at personal CAD

Many companies now offer computer aided drafting systems based on personal computers. These are usually fairly primitive if adequate for printed circuit board layout. Most do not have the graphics resolution or computer power necessary for more than the simplest mechanical design.

An exception is Cubicomp Corp (Berkeley, Calif). That company's CS-5 solid modeling system is designed for three-dimensional modeling with shaded surfaces. It consists of a graphics module, interface adapter, IBM PC, and a 512- x 512-pixel resolution, intelligent RGB monitor.

Despite the simpler two-dimensional graphics of electronic design, many personal computer aided design (CAD) systems are intended for drafting only. They cannot manage the full range of printed circuit board or IC design tasks required of an engineering workstation. Most of the present applications have been designed for either Apple or IBM personal computers and are stuck with the limited power and graphics resolution of those systems.

One company that has pushed the technology as far as possible is Chancellor Computer (South San Francisco, Calif). By requiring an IBM PC/XT with a 512-K memory, a 10-Mbyte Winchester, and an 8087 floating point coprocessor, Chancellor wrings quite a lot out of the

(continued on page 68)

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CIRCLE 38

Personal instrumentation
(continued from page 66)

Strength in numbers

To advance the use of personal computer-based tools for electronic engineering, an industry/user group was formed at the last Wescon conference. Started by Northwest Instrument Systems and FutureNet, it is intended to encourage feedback between vendors and users. The steering committee presently consists of three manufacturers: Northwest Instruments, FutureNet, and Valley Data Sciences (Mountain View, Calif), a PROM programmer manufacturer. The group also includes users and editors of electronic publications. The group will further the exchange of applications, programs, and other engineering information.

Although the market is currently small, the information-sharing networks will be needed because personal instrumentation is set for an explosive growth. The last count of companies, provided by the steering committee, showed 112 companies ready to enter the market or already producing hardware or software for it.

The main limitation on growth will be the speed with which personal computers appear on engineers' desks. In addition, this will no doubt be influenced by the interchange of information that the user society envisions.

Ten manufacturers attended the second meeting of the group on Feb 10 in San Jose, Calif. At that meeting, a step was taken to broaden the interest in the group and more properly reflect its charter by changing the name from Personal Instrument Computer Users' Society (PICUS) to Personal Engineering Computer Users' Society (PECUS). If PECUS can gain sufficient support, its first newsletter will appear by Electro/84 in May.

PC. Then, as with Cubicomp's solid modeling system, the IBM monitor is dispensed with altogether.

Instead, the company offers several optional monitors. The best of these is a 19-in. color monitor with 1024- x 768-pixel resolution. The system also offers bit-pad graphics entry and an optional printer and plotter. Software includes graphics entry and edit, schematic capture and netlist extraction, and an interactive logic simulator. This puts the Chancellor C2000 at the high end of the personal computer-based CAD performance scale. It also makes the C2000 among the highest priced of such systems at $23,500 with the XT.

At the other end of the price scale, but still providing much more than just personal computer aided drafting is FutureNet (Canoga Park, Calif) with the Design Aid Schematic Helpmate (DASH-1) schematic design system. FutureNet skirts the limitations of the IBM PC display without replacing it. The company's plug-in graphics controller card temporarily cuts out the IBM video display driver when the DASH-1 is in use and drives the display itself. This effectively doubles resolution to 640 x 360 pixels.

The DASH-1 can create, update, and print schematics quickly—moving or deleting components, modifying or replicating the circuit in seconds. The system can generate lists of materials, engineering change orders, and netlist information. Four different levels from circuit diagram down to the gate level can be displayed and there are interfaces for most popular CAD systems enabling the DASH-1 to function as a frontend input station to larger systems. A parts library included with the system has templates for most standard logic parts. Despite its name, the DASH-1 is not limited to printed circuit board design; it is currently being used for IC layout as well.

Different approaches

The two personal computer/CAD companies mentioned (Chancellor and FutureNet) have both built systems that are far more comprehensive than the usual computer aided drafting generally available as a personal computer add-on. However, their approaches are quite different. Chancellor has opted for high performance graphics that will put it head to head against 68000/Unix workstations in the market. Meanwhile, FutureNet has decided that its prices must stay in a range appropriate to the price of the PC. Even Chancellor has hedged its bets with a cheaper, lower resolution system, the C1000.

The pioneer in the personal instrument segment of this market is Northwest Instruments, Inc (Beaverton, Ore). The company's first product was a digital memory oscilloscope, the model 65 aScope made for the Apple II and IIe. The model 85 aGen, a programmable function generator, is also made for use with Apple computers. The company's model 2100 Interactive State Analyzer is available for both Apple and IBM personal computers.

Northwest Instruments is a Tektronix spin-off with considerable in-house expertise in conventional instrument design. Despite that, the company has chosen to manufacture personal instrumentation. This was done not only because of market need but because of perceived deficiencies in conventional instruments. The computer within a conventional instrument is not accessible for user-defined programming. An outside computer is often required for automated instrument setup, post acquisition analysis, and formatting of results. This is usually accomplished by configuring instruments with interfaces to the IEEE 488 GPIB and adding a GPIB controller.

This approach has several drawbacks. To begin with, it is not cost effective. Because each instrument was designed to stand alone, the user must purchase the computer, memory, and display with each instrument as well as with the controller. Also, instrument functions

(continued on page 70)

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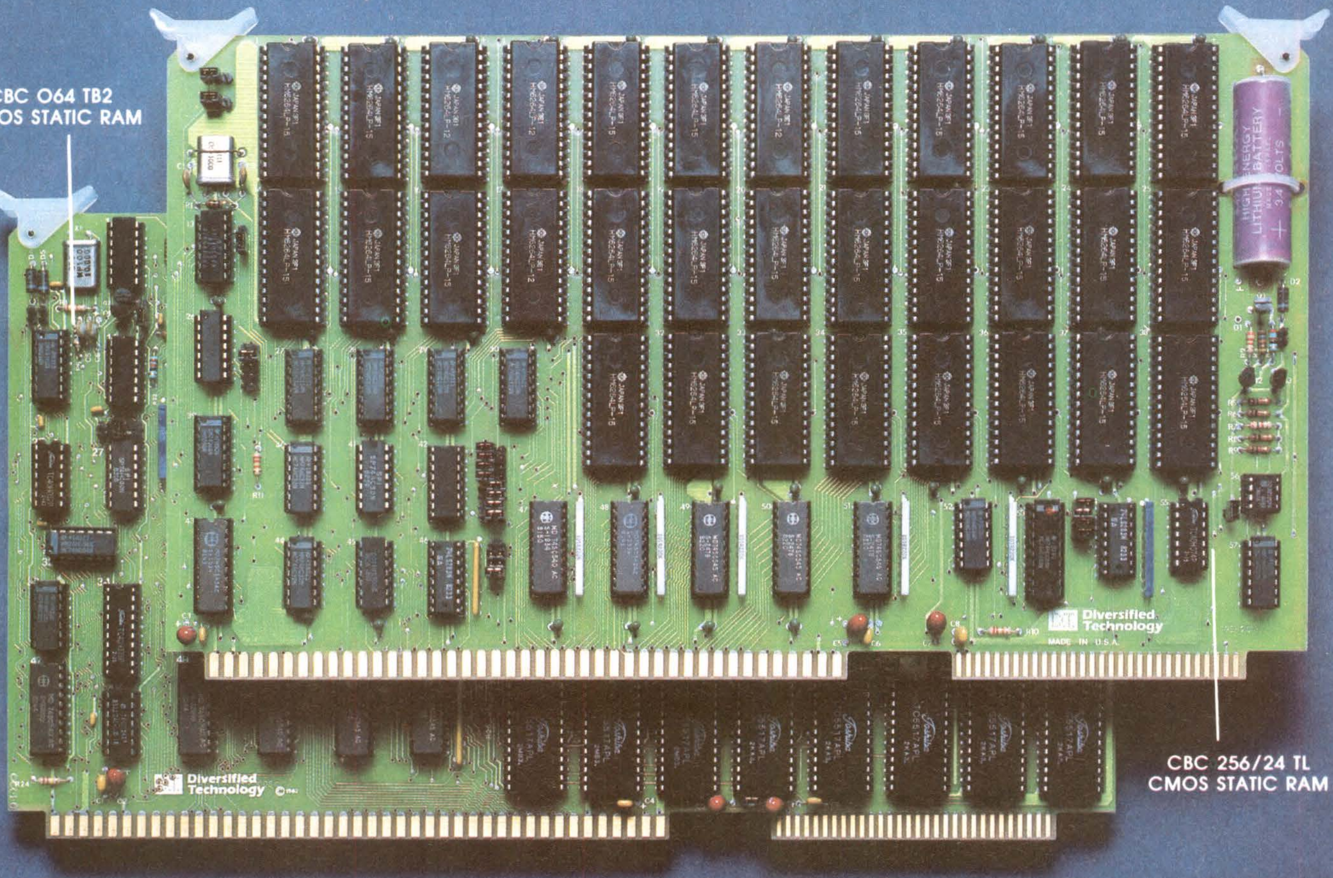

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CIRCLE 39

Personal instrumentation

(continued from page 68)

have to be programmed in the format specified by the vendor. This is inefficient where frequent user interaction with acquired data is necessary.

To overcome these deficiencies, a personal instrument performs only test and measurement. A tightly coupled parallel interface joins it to the personal computer where all display, computation, and user interfacing are performed.

Nonetheless, the IEEE 488 bus will be hard to dislodge from its preeminent position with thousands of different instruments from hundreds of manufacturers now able to interface to that bus. Also, many of these instruments and bus controllers offer a performance level that is hard to duplicate with personal computer-based instruments. Furthermore, there is often a requirement to run more than one instrument at a time. In such cases, the GPIB-based instruments and controllers have the advantage over the personal computers with personal instruments.

Several manufacturers, such as Tecmar (Cleveland, Ohio) and National Instruments (Austin, Tex) offer IEEE 488 interface cards for the IBM PC. This allows the PC to function as a relatively inexpensive controller on the GPIB but offers none of the advantages of nonredundant electronics that make the personal instrument concept attractive.

—John Bond, Senior Editor

SYSTEM TECHNOLOGY
(continued on page 78)

May Preview
Special Report on Graphics Technology

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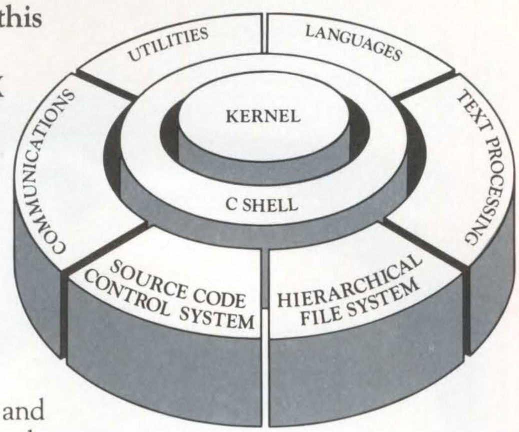

The custom match of GENIX with the NS16000 architecture is an obvious benefit. Besides providing all the proven benefits of the Berkeley 4.1 bsd version of UNIX--such as multiprogramming, a hierarchical file structure, and over 200 powerful utilities--GENIX adds value. GENIX supports true Demand Paged Vitual Memory and floating point operation. High level languages are also supported by an optimized C compiler and an optional, powerful Pascal compiler.

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CIRCLE 42

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Capacity	Part No.	Organization	Access Time Max. (ns)	Power Dissipation Max. (mA) Active	Standby
NMOS MASK PROGRAMMABLE ROM					
16K Bit	TMM334P*	2K x 8	450	80	—
32K Bit	TMM333P*	4K x 8	450	100	—
32K Bit	TMM2332P*	4K x 8	350	100	15
40K Bit	T6635**	4K x 10	350	90	—
64K Bit	TMM2364P**	8K x 8	250	40	15
64K Bit	TMM2365P**	8K x 8	200	100	25
64K Bit	TMM2366P*	8K x 8	200	100	25
64K Bit	TMM2368P*	8K x 8	200	100	—
80K Bit	T6436**	8K x 10	350	90	—
128K Bit+	TMM23128P**	16K x 8	200	80	20
128K Bit	TMM23127P**	16K x 8	200	80	—
256K Bit	TMM23256P**	32K x 8	150	40	10
CMOS MASK PROGRAMMABLE ROM					
32K Bit	TC5332P*	4K x 8	450	7	.02
32K Bit	TC5333P*	4K x 8	450	7	.02
32K Bit	TC5334P*	4K x 8	450	7	.02
32K Bit	TC5335P*	4K x 8	450	7	.02
64K Bit+	TC5364P**	8K x 8	250	7	.02
64K Bit+	TC5365P**	8K x 8	250	7	.02
64K Bit+	TC5366P*	8K x 8	250	7	.02
256K Bit+	TC53257P**	32K x 8	200	40	.02

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CIRCLE 43

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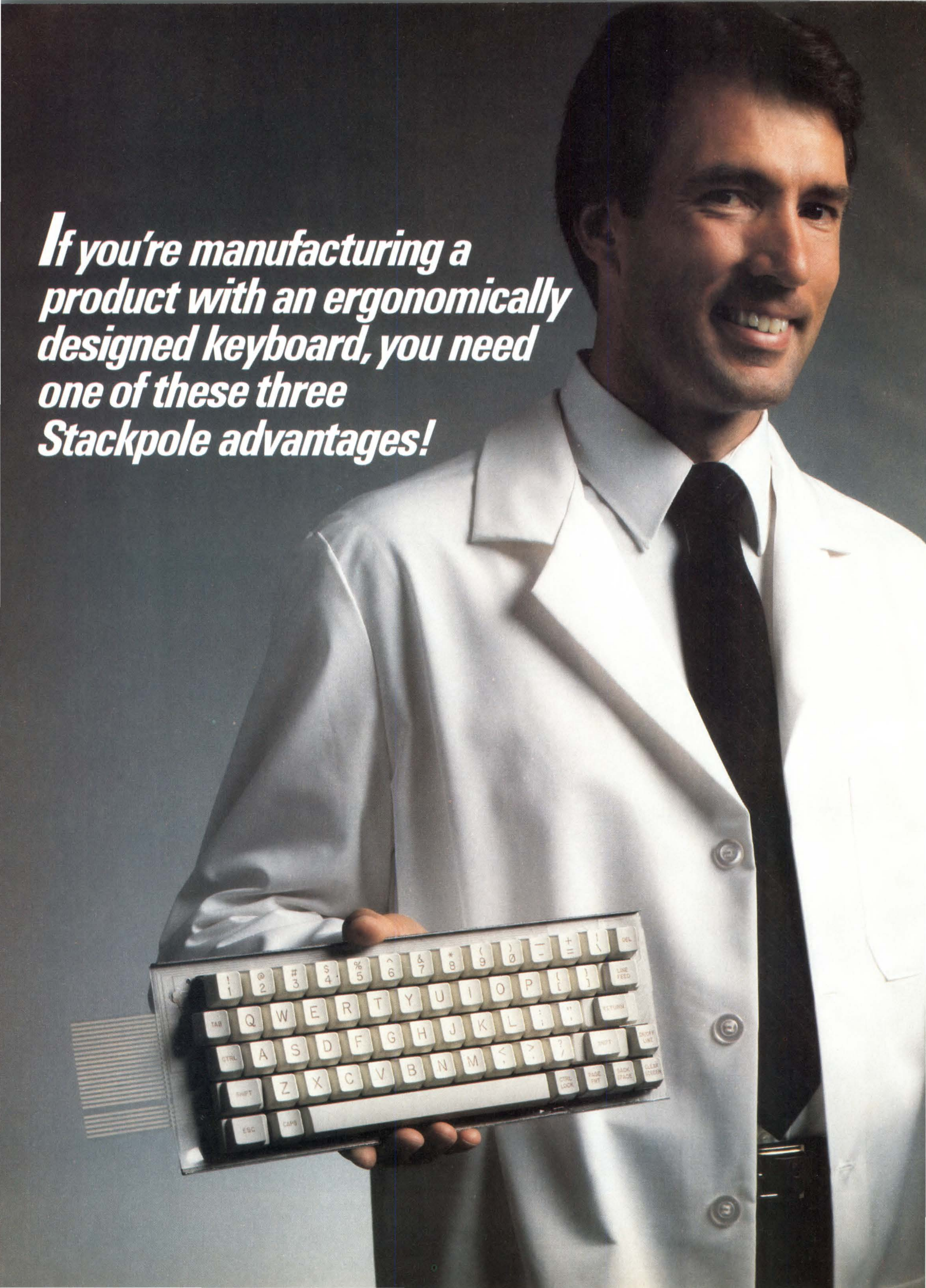
If you're manufacturing a product with an ergonomically designed keyboard, you need one of these three Stackpole advantages!

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In the KS-200E, Stackpole has combined the newer discipline of human engineering with its tradition of engineering components to work well and last longer. The result – a full-travel, ergonomically designed, highly reliable keyboard that projects quality where the fingers meet the machine. The KS-200E meets the most recent DIN requirements.

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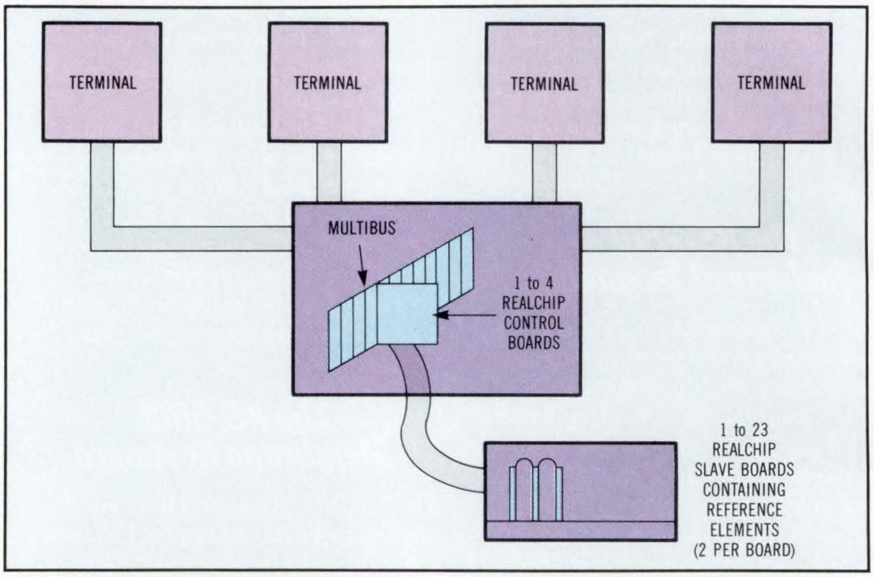
CIRCLE 44

CAE system ties real chips into software model

Today's computer aided engineering systems do a very good job of simulating logic for the design of custom and semicustom ICs and gate arrays. Many are also quite capable of logic simulation for board- and system-level designs. They allow the system designer not only to design and test the logic, but also to use off-the-shelf parts by referring to a database device library. Such libraries are created from the manufacturer's own data sheets and are gate-level software simulations of the parts.

However, a big problem arises when a board- or system-level design incorporates a 16- or 32-bit microprocessor or some other (often proprietary) VLSI circuit. How to produce a proper simulation of such a chip for inclusion in a computer aided engineering (CAE) design is a difficult task. To complicate matters, the manufacturer is not about to supply enough information for a proper simulation model at the gate level.

Even if enough data is available, the development task to model even one such chip is prohibitively expensive and time-consuming, as well as difficult to verify and maintain. In addition, the execution time for the code of the VLSI chip model can severely delay the overall simulation execution.



SCALDsystem's central control section has a Multibus that accepts up to four Realchip control boards, each controlling up to eight slaves. The actual refer elements containing the chips reside in a separate 23-slot card cage. Thus, up 64 devices can be modeled at one time.

Using the real chip

Valid Logic Corp overcomes this problem by simply using the actual chip in place of the cumbersome software model. Valid's Realchip system works within the company's SCALDsystem CAE system, which uses a device data base of over 1000 software models of off-the-shelf parts. When Realchip is installed in the SCALDsystem, a VLSI part can be treated as a hardware subroutine so that it appears in the schematic and in all logic simulations as a part of the overall CAE simulation.

Physically, Realchip works in conjunction with the SCALDsystem—a four-workstation CAE system using a central unit for mass storage, data communications, and graphics control. Local processors for manipulating schematic capture, editing, displaying timing diagrams, etc, reside in the individual workstations. One to four Realchip control boards can plug into the Multibus backplane of the S-32 central unit. Each control board can control up to eight slave boards that plug into a separate 23-slot backplane with power supply.

In turn, each slave board can contain two reference elements, or modules, that hold the actual chips being used in the simulation. Reference modules come in two types: one to accommodate DIP packages of up to 64 pins, and one for chip carriers of the type used for 80286 processors.

For the chip to run properly, each reference element supplies power and clock signals to its respective IC. But, the physical clock rate is decoupled from the simulated clock rate and the chip's operation is synchronized with the rest of the software model. Thus, devices modeled using Realchip can be freely mixed with software-modeled devices in the user's design. In addition, since the simulation treats the chips as hardware subroutines, only a single chip is necessary for multiple device instances in the design.

Each Realchip model consists of a graphics software "template" for use in the schematic capture operations on the SCALDsystem, and a personality element containing the real chip sample. The user must then create a device definition file that will be used to tie the chip to the template and serve as a reference for all future occurrences of that chip. This file typically has less than 100 lines and contains the pin names, pin types, and the output delays. Information for the device definition file is entered directly from the manufacturer's data sheet, thus allowing the user to enter and work with worst-case timing specifications.

By using worst-case timing specifications, the designer can ensure the rest of the circuit's operation with the chip in question. And, as these

(continued on page 80)

NO DEC IS AN ISLAND.

Able's new Easyway/E Ethernet port controller makes tying together networks of UNIBUS PDP-11 and VAX computers easier than ever.

Easyway/E provides DEC systems with plug-in access to IEEE 802.3/Ethernet LAN's, with less CPU overhead and less network software than other Ethernet ports.

That's because Easyway/E implements ISO/OSI protocol layers 1 thru 4 on a single board occupying one UNIBUS backplane hex slot. Much of the potential LAN software you need is already in the firmware. So, your initial network development time and costs for DEC systems with VMS and RSX won't drag you under.

And this lifesaving implementation of protocol on-board also offloads the CPU, freeing up the processor to handle other tasks.

What's more, Easyway/E meets IEEE 802.2, 802.3 and NBS-4 standards for ISO/OSI layers 1 thru 4, so current and future communications with other DEC systems will be smooth sailing.

In fact, Easyway/E's architecture is designed to accommodate future networking needs. The single board is comprised of two modules, so tomorrow's protocols can be implemented quickly with less expense. Additional protocol support including X.25, SNA and TCP/IP will soon be available, as will software support for DECnet and UNIX.

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CAE system ties real chips
(continued from page 78)
specifications change, or faster versions of the chip become available, the design's timing can be tightened up. Moreover, because a real device is in the circuit, the simulator can correctly sense pins that are in a high impedance state and propagate that information throughout the system.

Approach speeds design

The ability to use the actual chip as the model for the software simulation has several advantages that help accelerate design. For example, there is no need to design and debug "around" the big VLSI chip and then build a breadboard prototype. This method usually entails in-circuit emulation using a development system and/or logic analyzer. It often takes considerable time before the in-circuit emulation modules are available for new microprocessors.

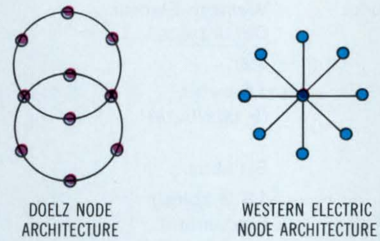
With the Realchip approach, the designer can incorporate the new processor or other part into the design as soon as working samples are available from the manufacturer. Even proprietary IC designs, such as gate arrays or semicustom VLSI parts designed by the user on the very same SCALDsystem or other CAE system, can be used in place of their original software models once silicon is available. This accelerates the simulation even further. Moreover, in-circuit emulators often do large chunks of processor operations concurrently and display the results. Realchip gives a nanosecond-by-nanosecond simulation of every cycle.

In addition to a full hardware simulation, Realchip lets prototype software for the design be tested in the simulation. By defining ROMs or other memory chips from the device library, the designer can "program" them to exercise the design. The processor will fetch and execute exactly as it will when the hardware is built. Thus, it is possible to debug the logic, as well as the microcode before any implementation.

A system such as Realchip implies that a feedback loop can be established between system design and debug, and VLSI design. Using Realchip, a kind of software test bed can be established for "first silicon" during the initial IC manufacturing phase. On the other side is the more rapid ability to develop systems incorporating new VLSI designs. Such feedback loops tend to be regenerative and greatly speed up the total design cycle. **Valid Logic Systems, Inc**, 1395 Charleston Rd, Mountain View, CA 94043.

—Tom Williams,
West Coast Managing Editor

Circuit-switched networks connect like telephones



Doelz Networks distributes redundancy using overlapping rings as its network topology for Elite One switching nodes, while Western Electric chooses a star topology to centralize network control for its Datakit/VCS.

Circuit-switched data networks promise to make data transmissions as simple as dialing a telephone. By specifying the destination address prior to actual transmission, these networks establish virtual circuits. As can be seen, this operation is similar to dialing a telephone number before actually talking on the phone.

When compared to packet-switched networks (eg, X.25), this approach has lower overhead and higher potential throughput. Packet sizes are smaller during transmission since the destination address is already specified. As a result, throughput increases because the packet need not be disassembled and reassembled at each node in the network. Treating packets as bit streams also frees these networks from user protocols and transmission speeds.

According to Frank Conners of Doelz Networks (Irvine, Calif), fragmentation occurs as designers attempt to connect disparate local area networks (LANs) with wide area networks (WANs) and other means of data distribution. In Band-Aid fashion, bridges connect separate LANs with gateways providing similar services when networks use incompatible protocols and transmission speeds (eg, Ethernet to X.25).

Such measures are necessary because present networks entangle message formats and transmission schemes with the data. These formats and schemes must be translated when moving data from one network to another. For example, Ethernet users wishing to send messages across a public data network such as Tymnet need to know their terminal transmission speed, and mode of transmission (synchronous or asynchronous) as well as specific bit- or byte-oriented

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Circuit-switched networks
(continued from page 81)

Circuit-switched Data Networks

	Doelz Networks Elite One	Western Electric Datakit/VCS
Topology	ring	star
Packet size	24 bytes	16 bytes (9 bits/byte)
Transmission speed	56 kbits/s	56 kbits/s
Asynchronous interface	9600 bits/s (maximum)	19.2 kbits/s (maximum)
Synchronous interface	9600 bits/s (maximum)	9600 bits/s (maximum)
Protocols supported	BISYNC SDLC X.25	3270 BSC

protocols eg, X.25 or IBM systems network architecture/binary synchronous communications (SNA/BSC). This is because transmission characteristics may not be the same for both the sender and intended receiver.

Furthermore, physical medium and transmission speed greatly influence both the format and transmission scheme of each network implementation. For example, the carrier sense multiple access (CSMA) scheme used in Ethernet networks could not work in the noisy environment of voice-grade telephone lines. Likewise, a token-ring scheme would be inappropriate for the high throughput required in a public data network like Tymnet.

Transparent transmission

Such tedious deliberations are akin to worrying about whether the mailman's truck uses gasoline or diesel, according to Conners. They should have no direct bearing on the physical act of moving bits from one point to another. Circuit switching takes a different approach by treating data as a continuous byte stream rather than as a distinct object (or message) as current networks do.

In fact, both Datakit/visually coupled system (VCS) from Western Electric (New York, NY) and Elite One from Doelz Networks, make no effort to obtain control and routing information from user messages. Rather, they append their own control blocks to the messages and transmit these transparent to user-defined protocols, transmission rates, and physical medium. Only at the terminal interface is the bit stream transformed back into messages that contain such information.

Network packets are kept small to maintain fast network response, but are big enough to avoid excessive overhead for control and addressing. Under the Datakit scheme, data is formatted in 9-bit bytes (with 1 bit used for control), with as many as 16 such bytes tied together for longer packets.

On the other hand, Doelz uses normal 8-bit bytes for its 24-byte packet. Of this total, 19 bytes are reserved for data with the remaining 5 bytes containing cyclic redundancy check (CRC) codes and control and address information. As many as 16 such packets can be linked for longer transmissions.

Comparing channel support

Datakit and Elite One also differ in the number of channels supported. In the first case, a single channel (as in Ethernet) is the physical link where terminals compete for access. Elite One has two data links each with four logical channels transmitted end-to-end. Contention resolution is the primary means to determine network access in Datakit, while the Elite One can support four user-defined priority levels.

Specifically, Datakit uses address comparison rather than a CSMA scheme implemented in Ethernet. Two contending terminals have their respective interface modules transmit a binary address to the switch control module, where it is altered. Comparing the two transformed addresses bit-by-bit eventually eliminates one terminal, thereby giving the other terminal access to the switch.

This increases network response time because both terminals need not back off and wait different time intervals (as with Ethernet). Western Electric estimates that the delay will be less than 1 ms through each node using this scheme.

Similarly, the Doelz approach leaves network access in the hands of the Elite One switching concentrator, with some help from the user. Each packet has a user-assigned priority level attached to it that is checked as it is passed from node to node. It can be placed on a queue in the node processor if a packet already in the queue has a higher priority. In that case, the node processor then transmits the packet with the higher priority. A watchdog timer on the node processor can also cause a packet to be placed on the queue if another packet has waited a long time.

Differing network topologies

Another difference between the Doelz and Western Electric approach focuses on network topology. Western Electric implements a star-cluster configuration with network administration handled by a single node. On the other hand, Doelz places its nodes in overlapping rings, with one node also handling network administration. At issue is the ability of the network to recover from breaks in the link, or the elimination of nodes.

In a ring configuration, dual paths are available to each node starting at any point on the ring and moving either clockwise or counterclockwise. If a node or link is broken, an alternate path is always available to reach the other nodes on the ring. Overlapping each ring also provides two separate paths across individual networks through different nodes. Redundancy is an integral part of the design.

On the other hand, a star cluster provides point-to-point connections
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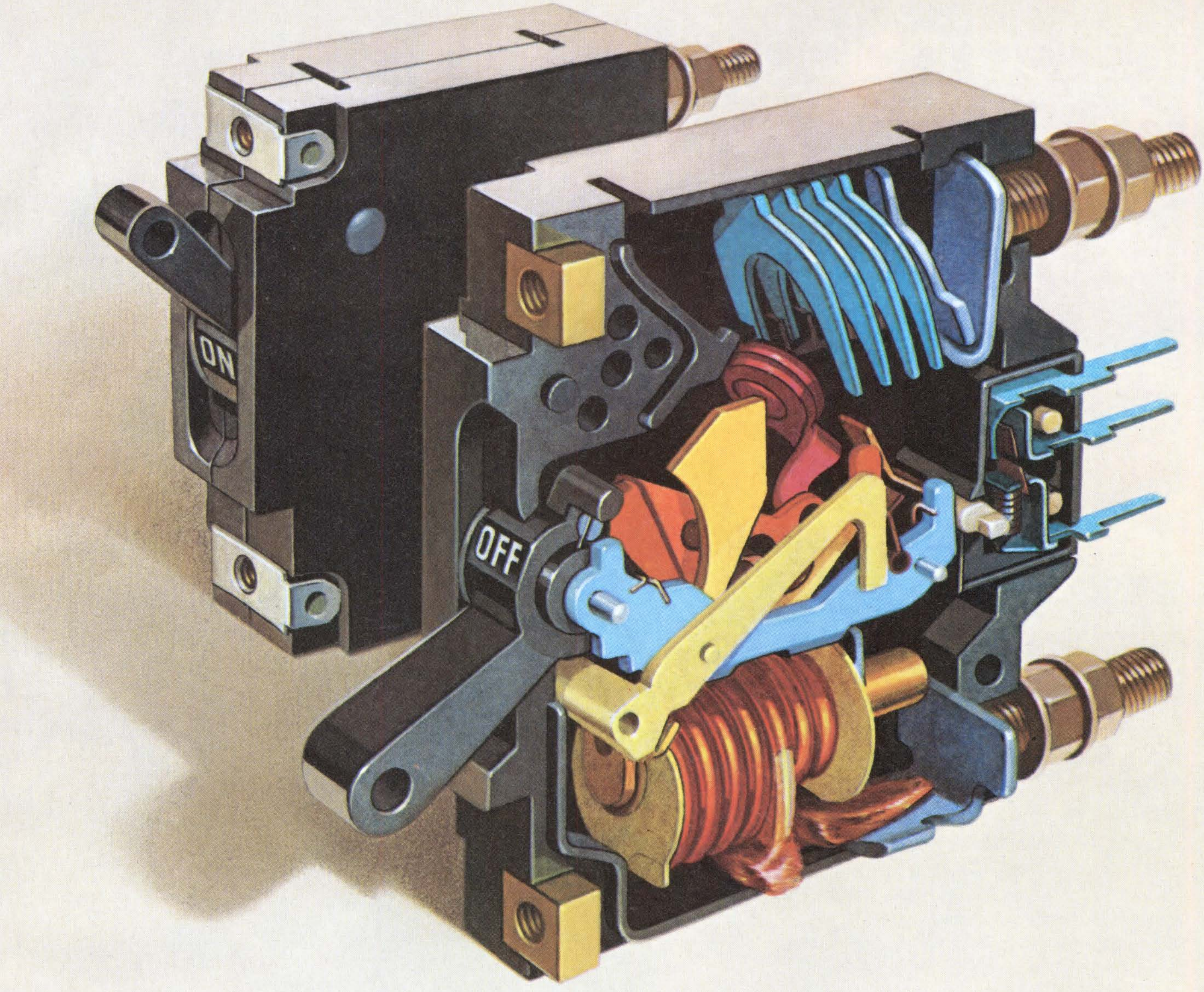

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CIRCLE 48

7626

Circuit-switched networks

(continued from page 82)

between nodes through a single point. The loss of a link or the central node cannot be as easily bypassed. Redundancy must be consciously planned in the duplication of both the physical links as well as elements of the central node to provide the same level of reliability as found in the ring topology. A key advantage of the star cluster is centralized control, according to James Hahn, one of the architects of Datakit/VCS. Ring topologies typically required distributed control necessitating more software implementation.

Other principal differences between Datakit/VCS and Elite One center on end-to-end error control and flow control. Datakit only provides error retransmission during block transfers between host computers. Other levels of services involving character transmissions between terminals leave error retries up to the user. Flow control (to prevent data overruns) also follows similar procedures. On the other hand, Elite One provides flow and error control for both host-to-host and terminal-to-terminal transmissions.

As far as physical implementations go, a typical Datakit network consists of synchronous and asynchronous terminals (with host computers) connected to dedicated interface modules. These modules reside in a single cabinet (the VCS) node with the trunk interface, switch, switch control, and timing modules. Dual 8-Mbit/s paths provide a measure of redundancy in case of component failure. Transmission rates range from 9.6 to 56 Kbits/s.

A typical network using Elite One packet-switching concentrators consists of multiple 6800 and 68000 microprocessors on a single card with dual buses providing the interconnect. Transmission rates will range from 56 to 1.544 Mbits/s.

Joseph Aseo, Field Editor

SYSTEM TECHNOLOGY
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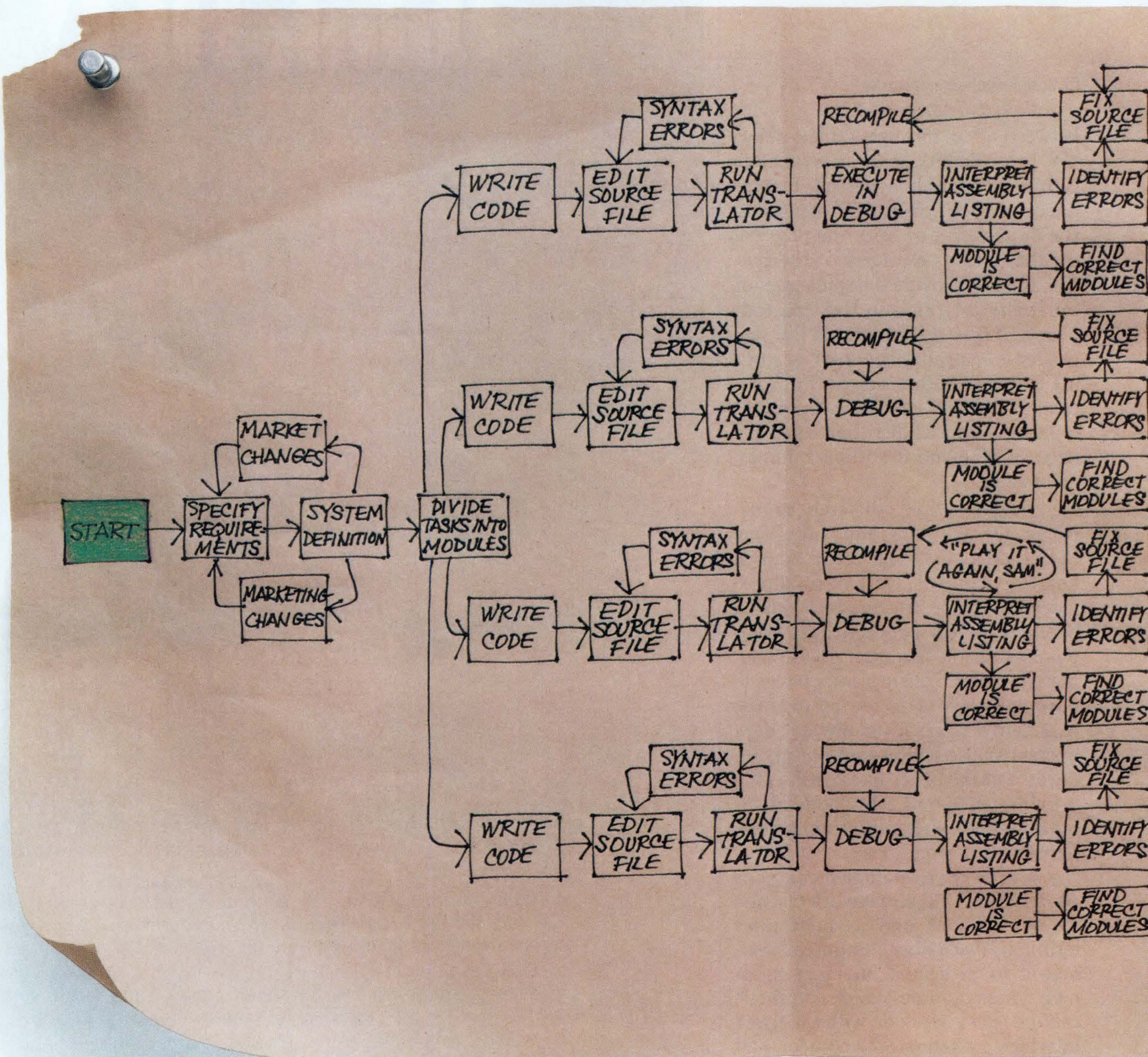
WHOEVER FINIS



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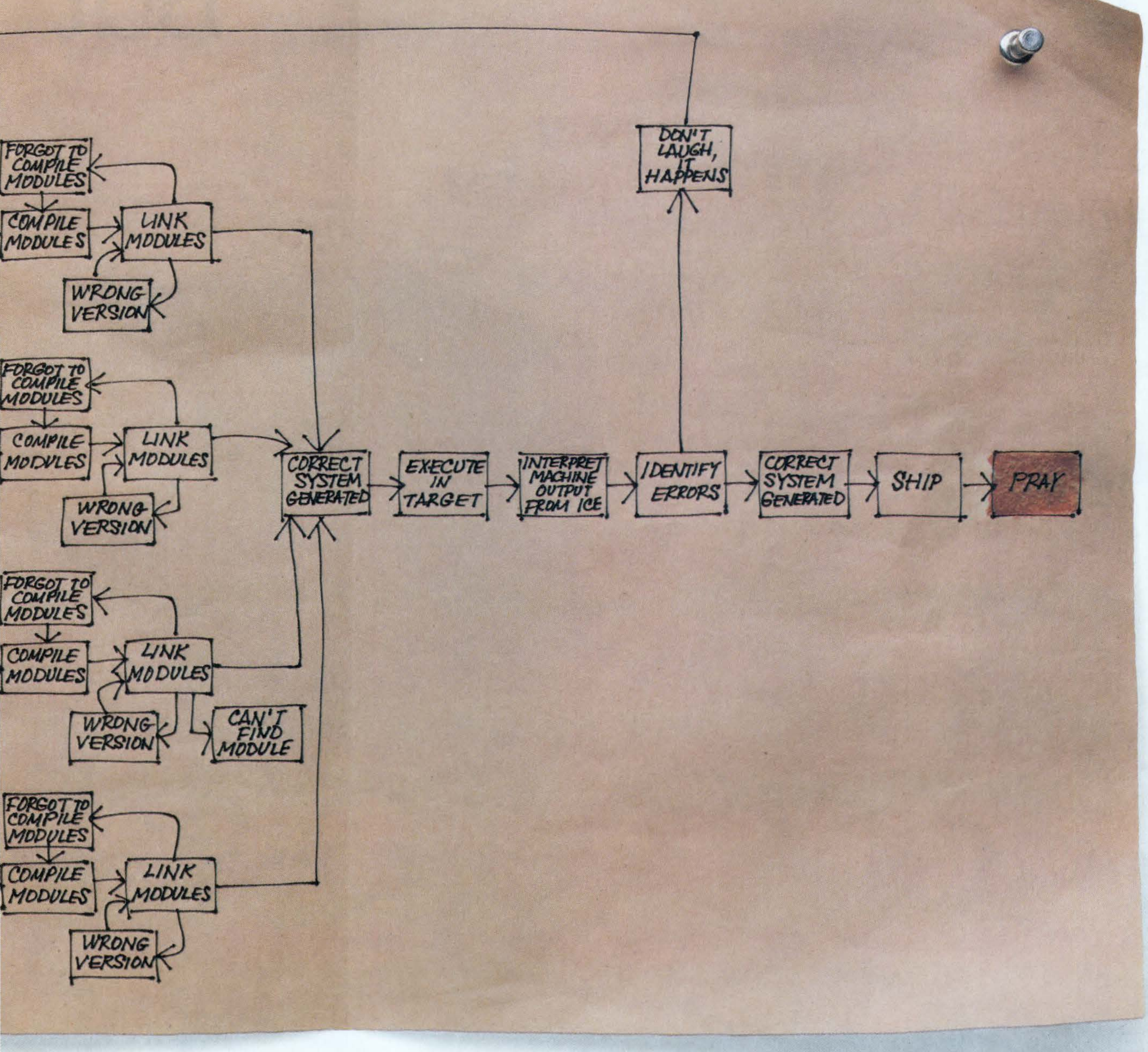

cally recompiles those modules that need it, and produces the complete, correct system. Automatically, of course.

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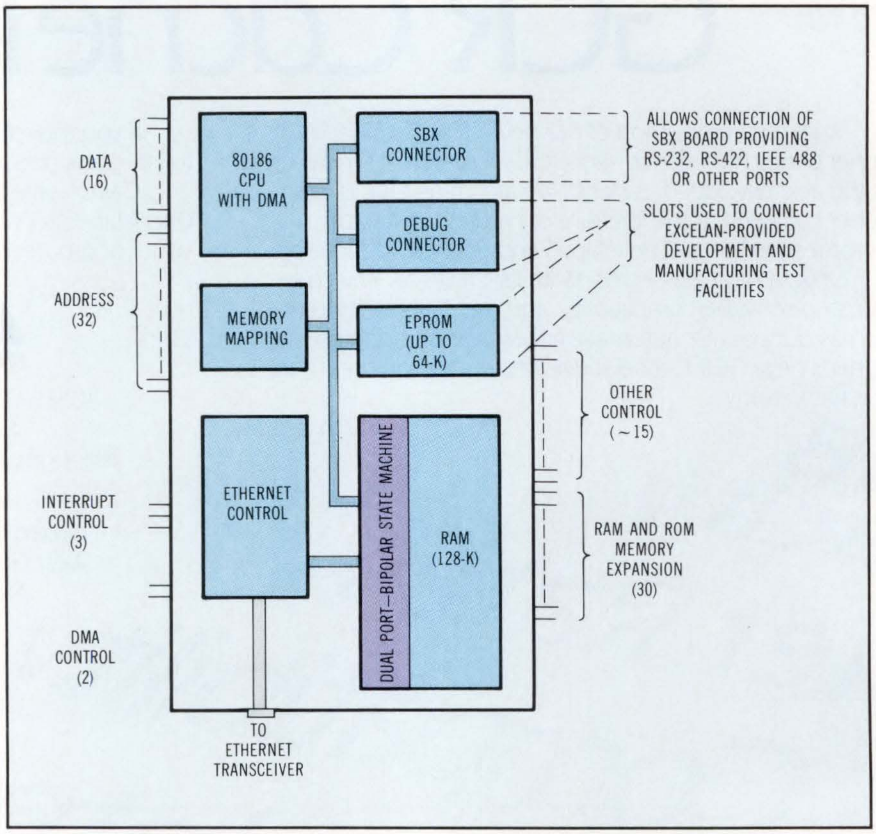
Ethernet now available on various buses—or custom boards

Ethernet local area network interfaces have emerged since Ethernet's 1980 definition by Xerox, Intel, and Digital Equipment Corp. Some have been hardware modules separate from the system using the LAN, imposing speed and interface penalties to the separate module. Others have been designed as an integral part of a given system, with all the attendant engineering costs. Excelan, Inc, in contrast, has undertaken to design and build interfaces that can be easily integrated into a system design. This provides the added function at a reasonable cost to the manufacturer.



The core module of the Ethernet controller, called the EXOS 200, is designed to be bus independent. All data and control lines are brought out so that it can be easily integrated into manufacturers' designs.

Introducing controller board series

To date, Excelan has produced interface boards for the Multibus, with a suite of device drivers for diverse operating systems, as well as software to handle various communication protocols. The company is now in the process of introducing a series of Ethernet controller boards for the VMEbus, Multibus, and the DEC Q-bus and Unibus. Specifications and design documentation are also available for designers who need or want to incorporate an Ethernet controller on their own boards.

Occupying an area of 4.5 in. x 9 in., the EXOS 200 series boards are software compatible with the company's earlier 100 series units. The most recent series uses the Intel 80186 CPU in place of an 8088, and can have up to 256-K RAM and 64-K ROM on board. The module also includes an Intel SBX port that allows direct connection to the controller and the use of the various interfaces (RS-232, RS-422, etc) for which peripheral boards are available.

Redesigned to provide the same functionality in a smaller package, the core module uses the Intel 82586 Ethernet controller and the 82501 line driver to talk via the local area network (LAN), and a bipolar state machine to control the bus interface and address mapping. One chief design criterion was that the core module be standard and bus independent, so that it could easily be integrated into any given system. Since the plans and design information are maintained on a computer aided design workstation, they can be readily available for licensees to integrate into their own products.

Improving traffic flow on LAN

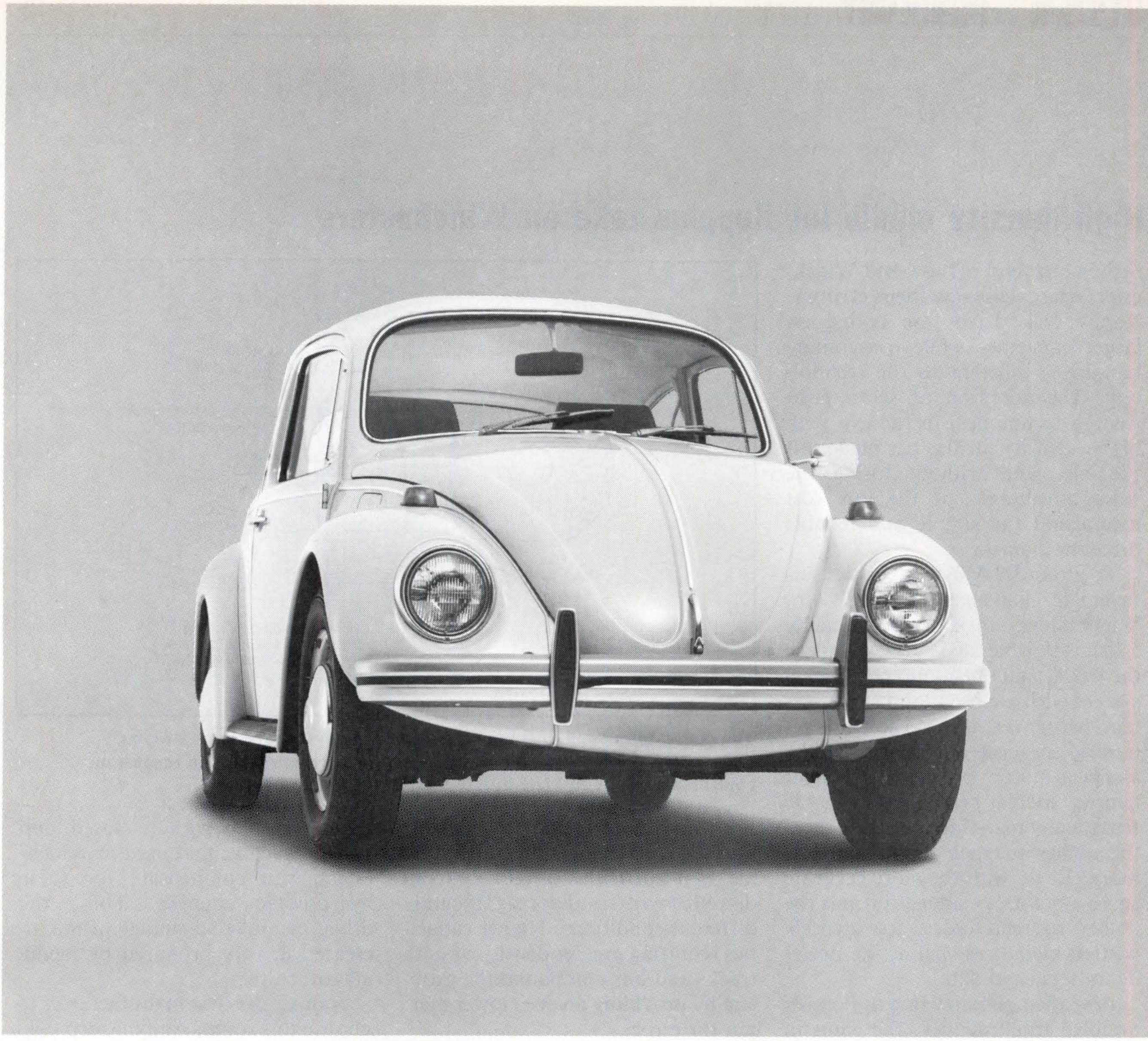
The design of the bipolar state machine allows the 200 series controllers to assign up to four 64-Kbyte areas in the host processor's memory space as individual message buffers. In this way, up to four users can pass traffic over the LAN simultaneously, without software intervention by the host or the interface controller.

Excelan says it will continue to develop the Ethernet interface, in cooperation with the company's customers, to provide the 1980's equivalent to the universal synchronous/asynchronous receiver/transmitter using the best available technology. Research and development are underway to provide the interface for all levels of systems, from mainframes to "intelligent" terminals.

The EXOS 201, for the Multibus, is priced less than $2000; the EXOS 202, for the VMEbus, is priced under $2500; the EXOS 203, for the Q-bus, costs less than $3000, while the EXOS 204, for the Unibus, is priced under $4000. All prices include appropriate device drivers and communication software. **Excelan, Inc,** 2030 Fortune Dr, San Jose, CA 95153.

—Sam Bassett, Field Editor

SYSTEM TECHNOLOGY
(continued on page 92)



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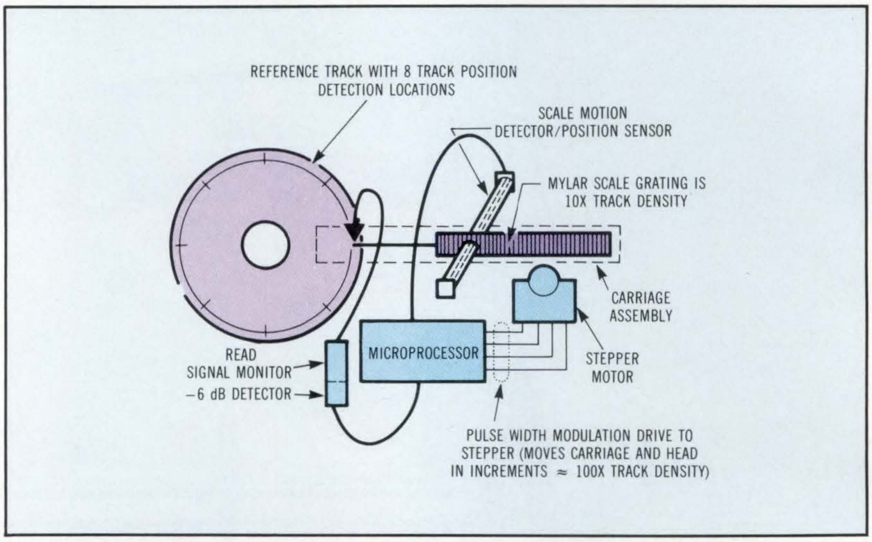
High density media let floppies take on Winchesters

Striving to fend off low end Winchesters encroaching on their territory, floppy disk drives are taking on larger capacities while overcoming handicaps inherent to the technology. The adoption of servo positioning techniques, in tandem with higher density media, has made this possible, and without losing the price advantages of the low cost media and the simple and reliable drive mechanisms.

To attain 3.3-Mbyte capacities sufficient to challenge low end 5¼-in. Winchesters, these high capacity 5¼-in. flexible disk drives replace the traditional open-loop positioning system with a closed-loop servo system. Moreover, they do so while retaining the cost advantages of the stepper motor positioner. Higher density media becoming available from many manufacturers give them the ability to pack tracks and bits more closely with the more accurate servo system. An added touch is the ability to read older, less densely written media, as well as the newer densely packed data.

Past attempts show that as floppies doubled track density, the gains in capacity tend to be accompanied by a drop in data integrity. The expansion and contraction of flexible media due to changes in temperature make it difficult to reliably read diskettes written under significantly different conditions. Higher capacities requiring greater density of both tracks and bits compound the problem by providing an even lower margin for error.



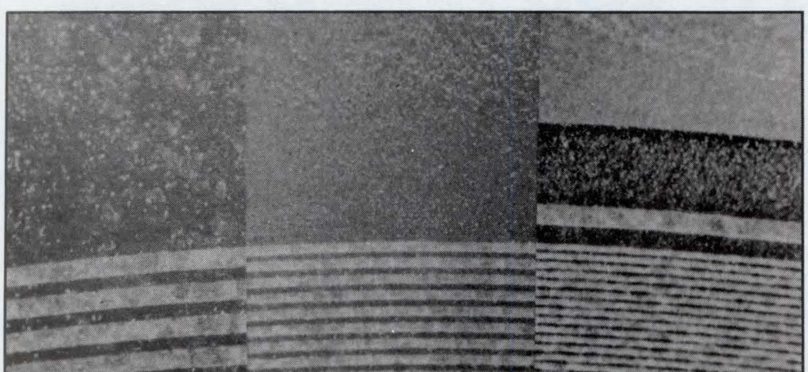
The closed-loop head positioning system in Amlyn's drive uses a Mylar scale with a motion detector/position sensor to compensate for expansion/contraction of the diskette due to humidity and temperature.

However, replacing the floppy disk drive's traditional open-loop positioning system with a closed-loop system, such as that used in Winchesters, can compensate for these hygroscopic changes. Thus, the drives can take advantage of the increased density promised by media manufacturers.

Among the first manufacturers to choose this route, Amlyn Corp (San Jose, Calif) uses a spin-coated diskette to achieve a 3.3-Mbyte capacity. The read/write head assembly in the model 1860 is driven by a microstepping stepper motor that locates tracks packed at a 170-track/in. density. Closed-loop feedback from a scale sensor through a microprocessor provides the ability to accurately locate tracks.

The closed-loop servo system on which the drive relies for head-to-track positioning consists of a reference track on each diskette, an optical scale located on the head carriage, a high speed precision stepper motor, and microprocessor control. All data tracks are located from the reference track on each diskette. Because the optical scale is made of the same material as the diskette substrate, it changes dimensions in the same proportions as the

(continued on page 94)



Relative sizes of data tracks record at 48, 96, and 170 tracks/in. (left to right). Closely packed tracks require significantly greater accuracy in the head positioning mechanism to ensure media interchangeability.

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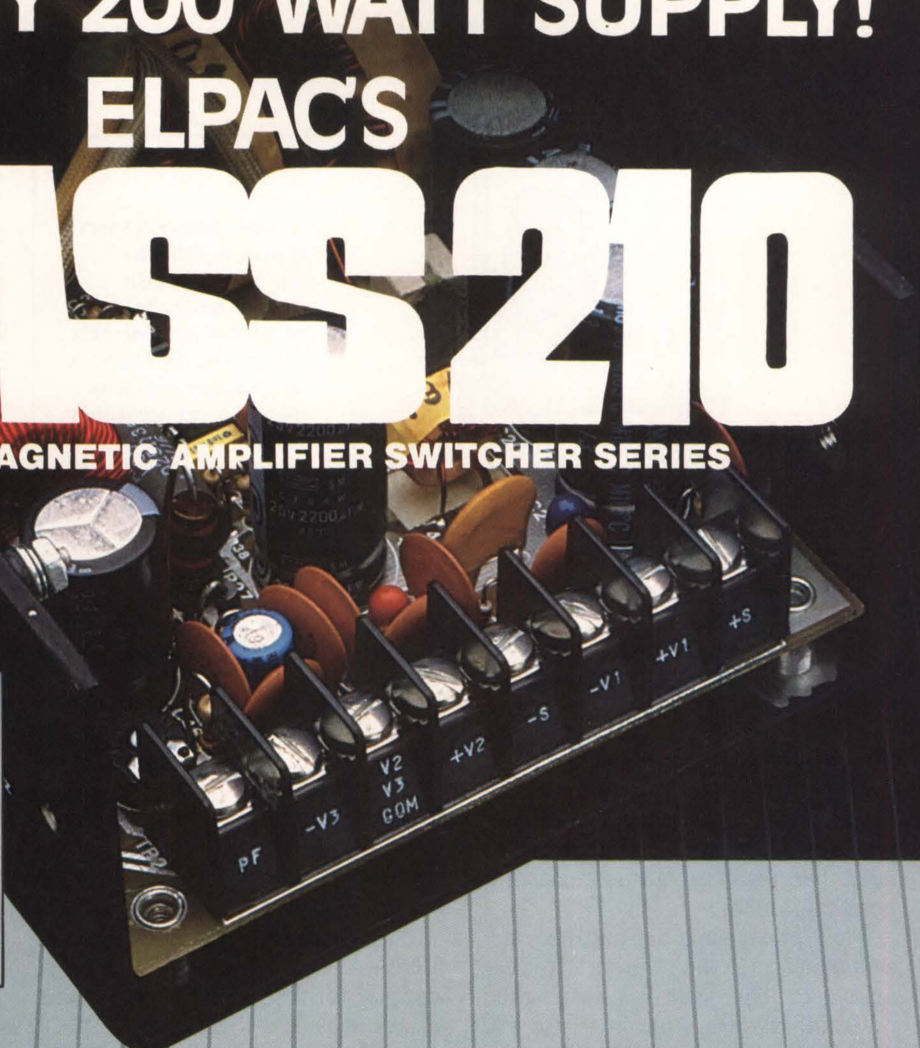

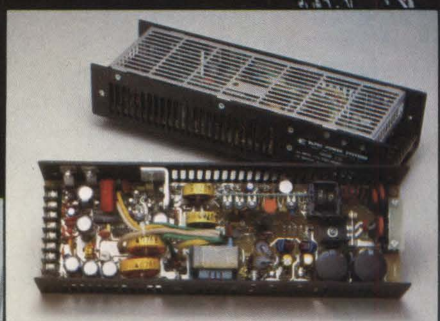

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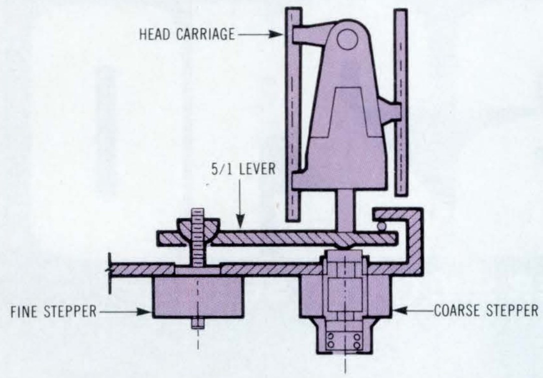

A track-following servo system in Drivetec's unit uses a coarse stepper motor to position head assembly at the selected track. A fine stepper motor is then used to accurately locate the track centerline.

diskette when temperature and humidity change.

The reference track on each diskette serves as the point from which all data tracks are located. It is also used for analysis of and compensation for anisotropic changes in the substrate due to fluctuations in temperature and humidity. Since it is resident on each disk, there is no need for track 00 adjustment and head alignment.

The optical scale defines the track centerline once the reference track is analyzed. The scale is photoetched on 3-mil Mylar. Scale lines are 590 μin. apart, with track centerlines 5.9 mils from each other (10 scale lines). Microcomputer control provides for head carriage movements in increments as small as 59 μin.

The 1.8-degree precision stepper motor can be microstepped as necessary to follow the centerline of the data track, with track offsets determined from reference track analysis. This ensures high accuracy for head carriage positioning.

In its 1722 Megadrive, Micro Peripherals, Inc (Chatsworth, Calif) combines Amlyn's 170-track/in., 10,250-bit/in. recording technology with its 96-track/in. drive mechanism. Resulting from a cross-license agreement and a parallel development effort by the two companies, the drive combines Amlyn's optical scale drive and quadrature detection circuit with MPI's plastic and die-cast metal components. Amlyn's head elements are built into MPI's sliders, head carriage, and upper-arm assemblies.

With capacity equivalent to that of the Amlyn/MPI drive, the 320 Superminifloppy from Drivetec (San Jose, Calif) is packaged in a half-height 5¼-in. form factor. This drive compensates for hygroscopic effects of the media by using a closed-loop servo system that reads a burst of servo information already prerecorded within each track.

Two stepper motors are used in this drive—one for coarse positioning, and one for fine positioning. During a track seek, the coarse stepper positions the head to the data track. The fine stepper then responds to the burst of servo information obtained from that track to step the heads in smaller increments until the track's centerline is reached.

This track-following servo allows data to be recorded at a 192-track/in. density. Rotating at 360 rpm, the drive records on 160 tracks/surface at a bit density of 9908 bits/in. Average access time is 160 ms.

Also credited as contributing to the density attained in Amlyn's drive are the read/write heads themselves. Using the same design familiar in Winchester drives, the composite heads are formed of hot-pressed manganese zinc. The bottom head is a button-style ceramic slider. A tripliant head set is used for the top head to provide maximum compliance with low load force.

Designed to reduce media wear, the proprietary design used in Drivetec's unit is based on a rounded rather than flat shape. The heads have no sharp angles to scratch the media's surface. One head is rigidly mounted, the other is loaded with a spring force that exactly matches the opposing force from the diskette. This improves media-to-head compliance.

A recent agreement between Drivetec and Eastman Kodak's Spin Physics Div (San Diego, Calif) will match the 320 Superminifloppy with Kodak's Isomax media to provide even greater capacities. While diskettes are currently recorded at about 10,000 flux changes/in. (FCPI), the Isomax media offer the potential for recording at 20,000 FCPI. Diskettes using the proprietary Isotropic recording technology to attain 800 oersted have been demonstrated to offer 5- to 10-Mbyte storage capacities in 5¼-in. drives.

The ability to read older, less dense media as well as the tightly packed data generated by these drives taps existing software libraries. To read 48- and 96-track/in. diskettes, drives run at 600 rpm; they run at 360 rpm to read the more densely written media. When adding this to the compatibility with standard 8-in. floppy disk interfaces, drives can be upgraded without changing controller software or undergoing a database conversion. The capacity provided by drives of this genre using closed-loop control systems can be further expanded when vertical recording media become available.

—Peg Killmon, Senior Editor

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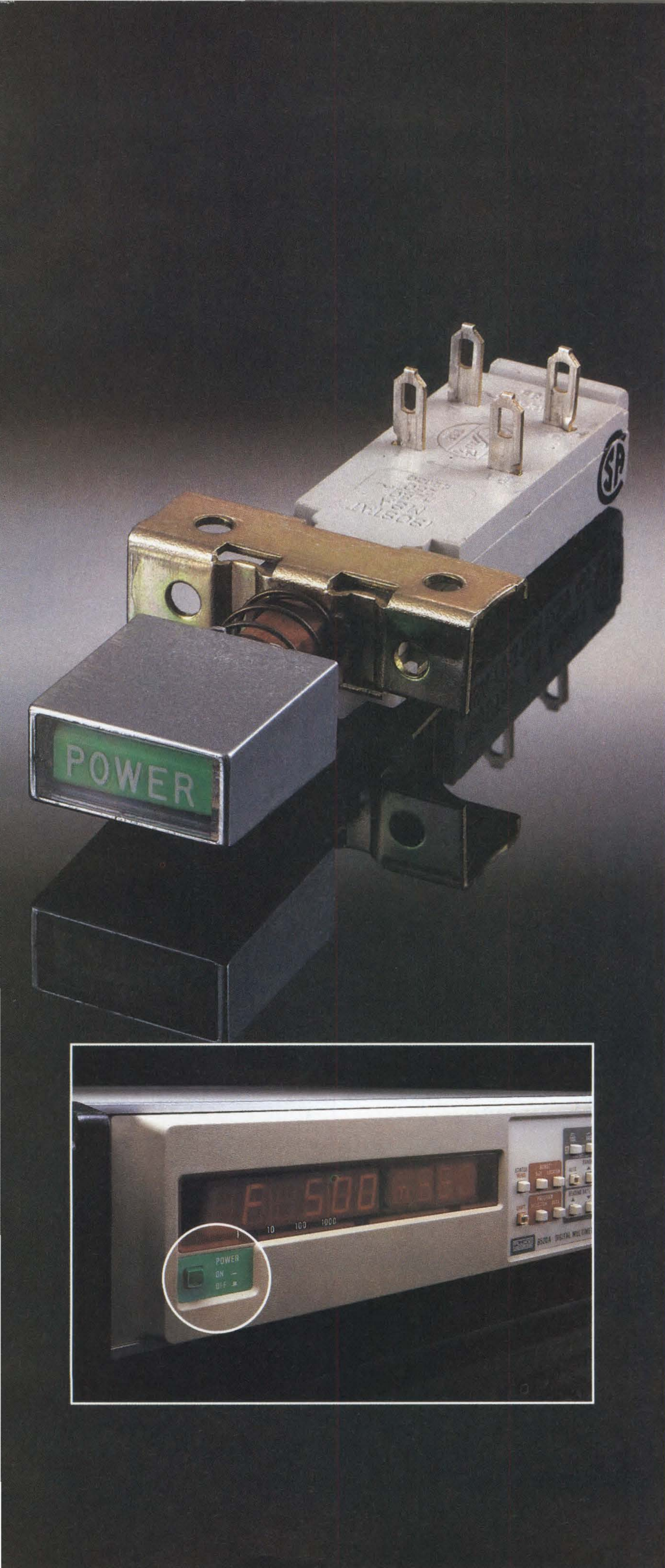

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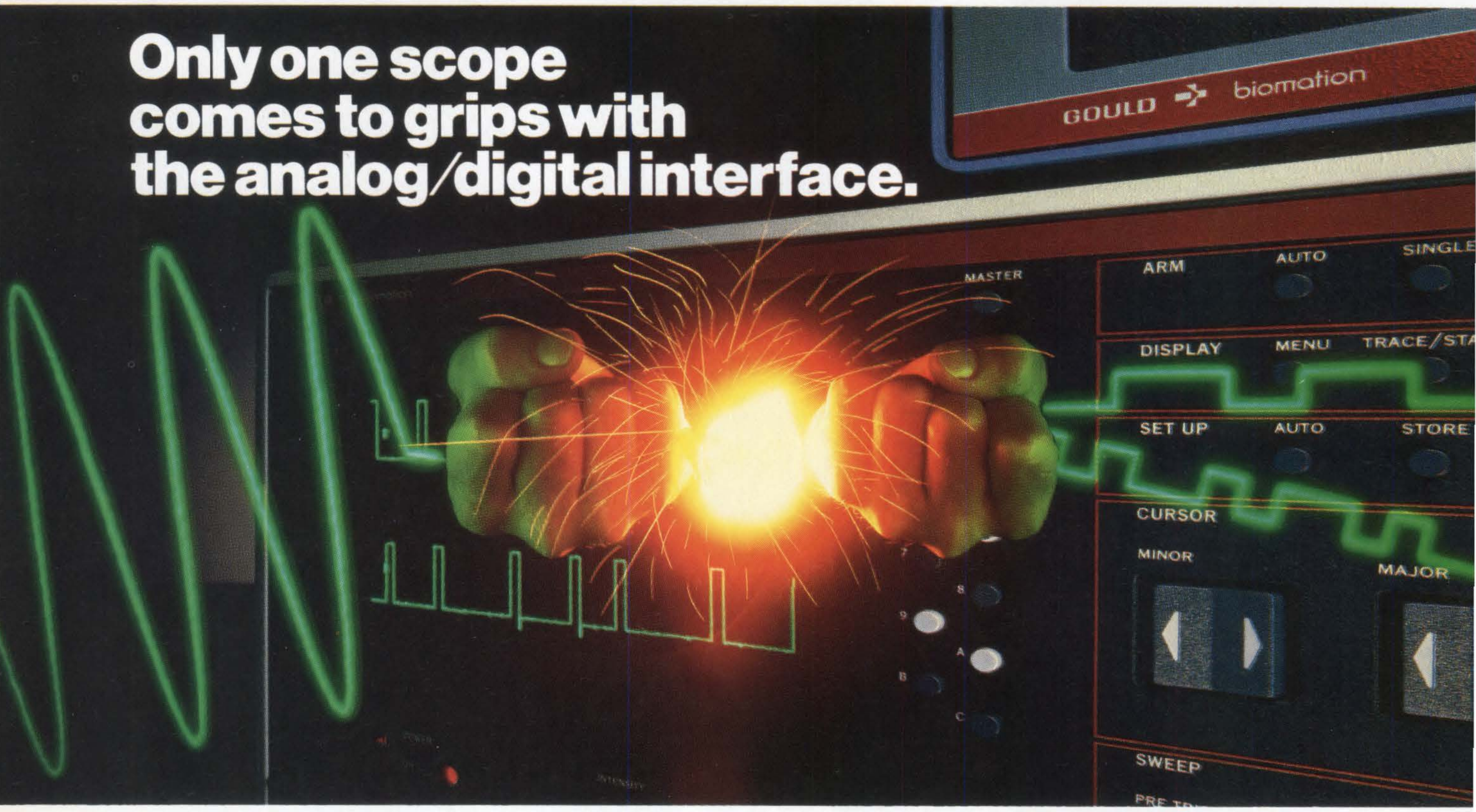

GOULD
Electronics

CIRCLE 59

Electro/84 Mini/Micro Northeast

Electronics Show and Computer Conference

Hynes Auditorium and Bayside Exposition Center, Boston, Massachusetts May 15 to 17, 1984

From chips to intelligent systems, the news out of research and development labs reported at Electro and Mini/Micro-Northeast will be making up-to-the-minute distinctions between state-of-the-art technology and technology at hand. Attendees at the paired electronics show and computer conference will have a chance to filter through the issues and products at both. Over 45,000 computer and electronics engineers are expected at Electro's professional program and 600 exhibits, and another 10,000 at Mini/Micro. Both events are cosponsored by regional chapters of the IEEE and ERA.

After communications deregulation, the computer industry has been busily putting the pieces back together. On deck at Mini/Micro will be speakers who will help sort out the current data transmission morass. They will give overviews of global communication networks, small area networks, local area networks, and the rest, then focus on applications where semiconductor solutions are apropos. Alex Goldberger, technical marketing manager at Exel Microelectronics (San Jose, Calif), will lead with a synopsis of the changing picture in data communications.

Between the two shows, six sessions will address communication issues. On the roster are papers concerning digital communication networks, fiber optic local and wide area networks, and videotex. Additional silicon-oriented discussions will range from incorporating LSI modems into computer products to introducing VLSI technology into the integrated services digital network.

Perhaps the hottest papers, however, will be the ones that flash the latest details on upcoming releases that many in the field consider prime design prospects. At the top of this "most-wanted" list are components such as the Inmos Corp (Colorado Springs, Colo) Transputer, a reduced instruction-set computer designed for parallel fifth-generation computer architecture. The internal workings of this chip, which was formally announced at Wescon last November, will be examined during the Mini/Micro session on 32-bit microprocessor architecture.

The Transputer is not the only yet-to-be-seen chip for which advanced-system designers have a hankering. Other such chips to be reviewed in the 32-bit microprocessor sessions include Motorola's (Austin, Tex) MC68020 and Zilog's (Campbell, Calif) Z80,000. The 32032 from National Semiconductor (Santa Clara, Calif) will also be described. Beyond the features of each particular chip, speakers will assess issues governing the integration of cache, coprocessor interfaces, and memory management support.

More chip-talk will highlight developments in single-chip microcomputers, peripheral ICs, and pipelined architectures for high speed processing systems and ICs. Solutions in CMOS—for many applications no longer a matter of whether, but of when—are now growing by leaps and bounds. Witnessing that trend, two Mini/Micro sessions will explore new-breed CMOS microprocessors. One will examine emerging single-chip CMOS microcontrollers, while the other will look at existing CMOS versions of popular NMOS microprocessor architectures.

Dynamic RAMs flex their features

Even though the new year ushered in three prototype megabit RAM chips (see *Computer Design*, Jan 1984, p 61, and Mar 1984, p 3), the near-term state-of-the-art for system architects is 256 Kbits. In fact, through 1986 the 64-Kbit RAM is projected to factor largest in market share. At that time, analysts expect a crossover putting price per bit for 256-Kbit chips on a par with that for 64-Kbit versions.

By 1989, dynamic RAMs may speak for as much as 52 percent of the total semiconductor memory market, and 65 percent of all DRAMs in that market are expected to be 256 Kbits or denser, reports Betty Prince, strategic marketing manager of Motorola's MOS Memory Div (Austin, Tex). Moreover, the denser chips are gaining speed and reliability while simplifying control logic. As the market matures to meet diverse requirements, DRAMs are inclining toward a spread of I/O organizations and will tend to

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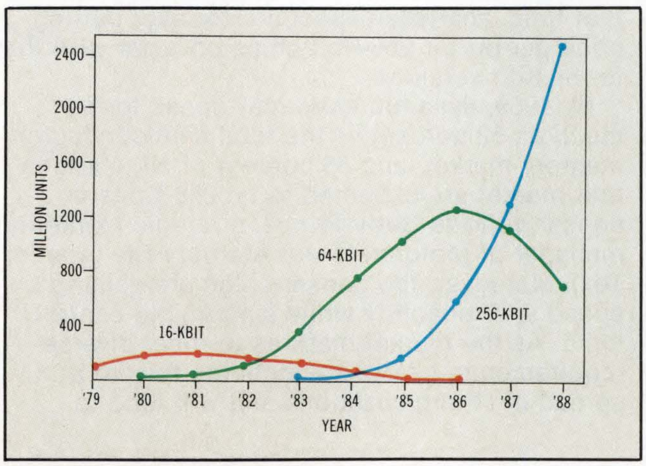
feature varied onchip functions geared to specific system needs.

Such demand is driving automated factories to produce low cost, standardized 256-Kbit chips. Despite different means of implementation, prospective 256-Kbit suppliers as a group are working for a basic core of comparable features and pinouts. Nonetheless, there will probably be plenty of room for memory chips optimized to particular applications. Burgeoning memory-intensive applications from high resolution digital TV to voice synthesis and artificial intelligence will clamor for all kinds of memory configurations.

According to Fred Jones, memory applications manager at Inmos Corp, densities will spiral for at least two more generations. As a class, dense chips are likely to join the overwhelming industry trend toward high performance CMOS. Apart from its attractive operating features, at the 256-Kbit level and beyond CMOS offers simpler and less expensive fabrication than NMOS. Thus, Jones indicates that NMOS wafer costs at 256 Kbits become comparable to CMOS wafer costs. Moreover, CMOS can significantly reduce the peripheral circuitry area—which takes up about half of the overall NMOS die area—thereby reducing die size.

Another virtue of CMOS technology is its lower power dissipation. In nonswitching circuits, this means that static designs in CMOS can replace the dynamic circuits that NMOS must use to conserve power. Static circuits are also faster and do not need to be precharged, so cycle time is reduced. Compared with NMOS RAM, for instance, static column decoding circuitry is relatively simple. Static column decoding is appealing because it removes the critical timing relationships between row address strobe, column address strobe, and the multiplexed addresses that often limit system performance. Though it latches row addresses conventionally, static column decoding accesses column addresses asynchronously—more in the manner of a static RAM.



Dynamic RAM markets (Courtesy of Dataquest)

In the same package, multiplexing addresses using a static column decode technique could extend byte-wide devices significantly beyond present density limits, Jones asserts. Whereas today's maximum density for a 28-pin read/write RAM is 32 Kbits x 8, the static column address multiplexing concept would push these strictures to 1 Gbyte, he contends. In a 24-pin package, the ceiling would be 4 Mbytes. Jones envisions both standard byte-wide devices and static column decode addressed multiplexed devices coexisting in the same physical array.

Fast EEPROMS are doing more

A growing list of onchip functions is making electrically erasable PROMS feasible for byte-wide memory sockets, with minimal or no support circuitry. Some devices now read and write like SRAMS while others are fine-tuning performance of features such as page mode. Moreover, EEPROMS are becoming sophisticated enough to implement nonvolatile reconfigurable data storage. Progress in chip features and concerns in designing with EEPROMS will be the topic of an Electro session on sophisticated electrically erasable memories.

Several advanced chips will be described by Steven Grossman, memory product marketing manager at Exel Microelectronics (San Jose, Calif). These include an 8-Kbit x 8 low power CMOS EEPROM that is written with standard microprocessor write cycles, much as an SRAM. This chip carries a mechanism that puts additional features under user software control. Also described will be a 4-Kbit x 8 CMOS EEPROM with 70-ns access times that compete with bipolar PROMS.

Grossman foresees the 64-Kbit chip in battery-powered applications as an interface to CMOS microcomputer logic chips and CMOS memories. Besides low power, this EEPROM features a JEDEC standard 28-pin, byte-wide memory configuration. Onchip, a set of static registers contains advanced features collectively dubbed "status word," which a user reaches through software. The status word is read or written by pulling $\overline{SW}$ (pin 1) low and applying the usual 150-ns memory read/write cycle.

Previous industry-standard pinouts called for high voltages often unavailable in logic systems to control many of these features directly from the device pins. This chip's special register features include a charge pump that boosts the internal programming voltage level from 5 to about 20 V in order to avoid false writes caused by power transients. When the charge pump is

(continued on page 104)

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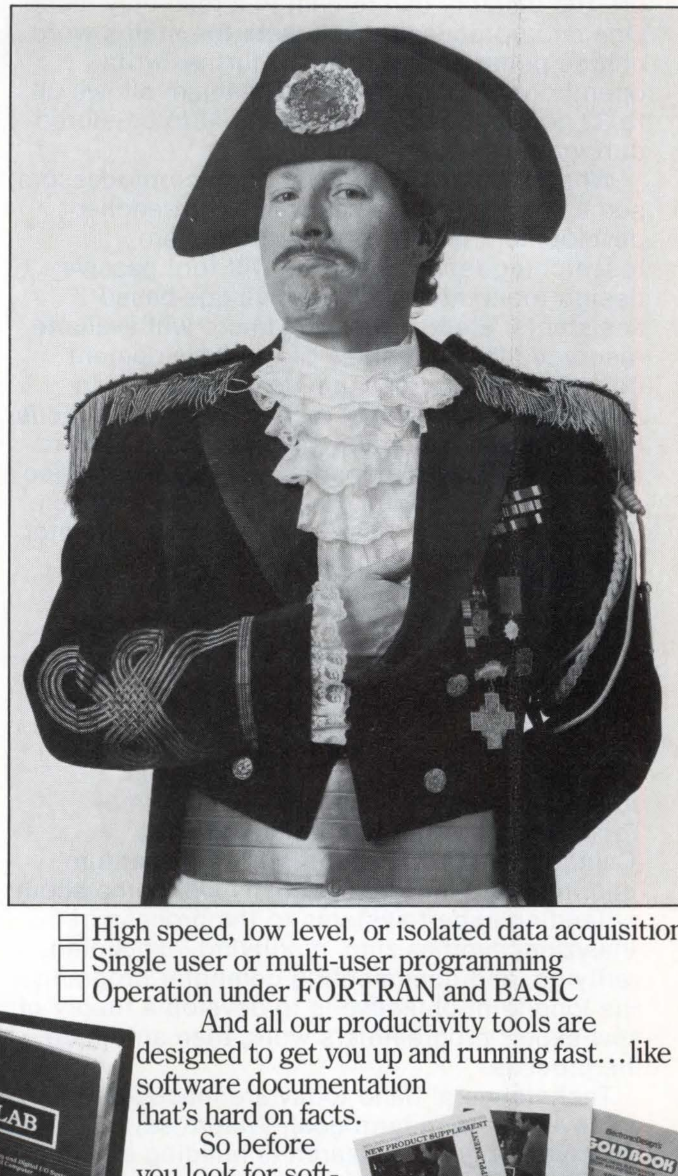

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CIRCLE 60

(continued from page 102)

off, the memory can remain in a read-only mode. One microprocessor cycle sets the status word charge pump enable to allow further write operations. A page mode mechanism allows up to 32 contiguous bytes of memory to be stored during one programming cycle.

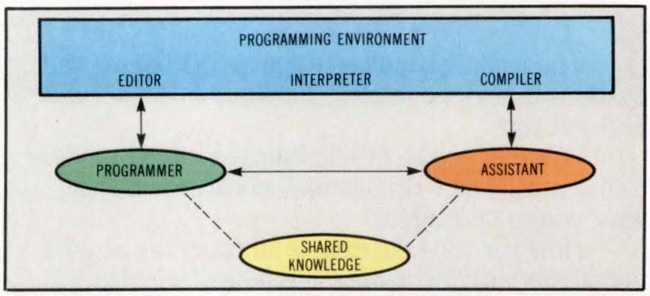
When it comes to cultivating microprocessors, some are seeking alternatives to entrenched development systems, while others are researching techniques that will turn passive design tools into active, knowledge-based assistants. Electro and Mini/Micro will evaluate resources for both sides of the development coin. One Electro session on alternatives to microprocessor development systems will focus on options for selecting development software languages and performance, using a centralized engineering computer, choosing programmable device support, and using an in-circuit emulator. Another will analyze new tools for testing programmable logic and digital systems, elaborating on the latest in software tools, algorithms, and devices used for functional digital testing at the chip and system level.

Development systems and CAD grow smarter

As Richard Waters, principal research scientist at the Massachusetts Institute of Technology's Artificial Intelligence Lab (Cambridge, Mass) sees it, the next quantum leap in programmer productivity will come about by lending expert systems to the process of analyzing, synthesizing, modifying, explaining, verifying, and documenting computer programs. His long-term objective is to develop a theory of how expert programmers work, then automate the process.

Techniques at hand today are inadequate to achieve that long-term goal, Waters says. However, ongoing research is building a foundation by developing an active, knowledge-based programming tool that will take over rote tasks. This tool can simplify a programmer's job by issuing commands that refer directly to the logical structure of the algorithms being used, rather than to commands that refer to the textual or syntactical structure of the program. Existing program editors often change many separate parts of the program text to effect a single logical change. The knowledge-based editor, on the other hand, regularly completes such changes with one command.

In essence, the key to constructing an effective programmer's assistant is shared knowledge. The analogy is that of a chief programmer (the expert human) heading a development team (the automated assistant). Through two-way communication tapping a shared knowledge base, the programmer and the



Automated editor in programmer's assistant metaphor presents a basic model for expert systems. The keys are a division of labor and a large knowledge data base accessible to programmer and assistant.

assistant both interact directly with the programming environment.

One day soon, artificial intelligence techniques will likely combine with computer aided design tools to create a new discipline called intelligent CAD. Assessing that trend, Stephen Emmons, Jr, graphics programmer at Michael Leesley Consulting (Austin, Tex), will summarize how CAD and artificial intelligence now differ, and what must happen before they can join forces.

Presently, practical problems keep the two apart. Modes of communication between them form a major obstacle. Whereas expert systems typically conduct textual dialogue, CAD systems often convey important information in drawings. Computer graphics enhanced by powerful database modeling will be instrumental in bridging the two disciplines, says Emmons. The other area where artificial intelligence and intelligent CAD will have to swap techniques is information handling. For instance, expert systems learn by comparing recent information against preexisting knowledge bases, while CAD systems focus on capturing, maintaining, and adapting to new information.

To effectively represent diverse sets of objects and their relationships, Emmons asserts that graphics modeling techniques must work hand in glove with database management techniques. After all, effective use of a knowledge base hinges on the information system's physical storage and retrieval mechanisms. As information handling techniques broaden their horizons, knowledge bases in general will be better equipped to synthesize and report on the bulk and variety of data we now ask them to analyze.

—Deb Highberger, Senior Associate Editor

For registration information, contact Kent Keller, Electronic Conventions Management, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

(Conference coverage continued on page 106)

(continued from page 104)

Professional Program Excerpts*

Session 3: High Density Interconnections
Tues 10 am to 12 noon

Chair: I. P. Ayoub, E. I. du Pont de Nemours & Co, Inc/Berg Electronics AP&S Div, New Cumberland, Pa

3/1 "Overview: High Density Interconnections"
I. P. Ayoub, E. I. du Pont de Nemours & Co, Inc/Berg Electronics AP&S Div, New Cumberland, Pa

3/2 "Design Requirements for High Density PC Card Connector"
H. Andrews and D. Upperman, AMP, Inc, Harrisburg, Pa

3/3 "High Density Impedance Controlled Connector"
B. C. Desai, E. I. du Pont de Nemours & Co, Inc/Berg Electronics Div, Camp Hill, Pa

3/4 "Interconnection and Connector Requirements for High Density Packaging"
H. Waltersdors, Thomas & Betz, Raritan, NJ

Session 6: Gate Array Technology: Promises and Problems
Tues 1:30 to 3:30 pm

Chair: R. A. King, Motorola, Inc, Austin, Tex

6/1 "Multichip Logic Array Design: Problems and Solutions Using Simulation Tools"
K. Lobo, LSI Logic, Milpitas, Calif

6/2 "Engineering Workstation Aids Logic Array Design"
G. Beck and L. Bogle, Motorola, Inc, Austin, Tex

6/3 "Reliability and Multilevel Routing Methods"
R. Muns, Harris Semiconductor, Melbourne, Fla

6/4 "Gate Arrays: The Hidden Cost Savings"
B. Sullivan, AMI, Santa Clara, Calif

6/5 "Application Consideration in Subnanosecond CMOS Array"
J. De Rosa, National Semiconductor, Santa Clara, Calif

Session 9: High Speed, Low Power Bipolar Logic
Tues 4:30 to 6:30 pm

Chair: D. A. Ferris, Fairchild Semiconductor, Digital Products Div, South Portland, Me

9/1 "AC Production Testing of FAST TTL"
S. LeGrady and K. Siez, Motorola, Inc, Bipolar Military Products Operations, Tempe, Ariz

9/2 "An Oxide Isolation Process for Bipolar LSI Circuits"
D. DeSimone and M. Richard, Digital Products Div, Fairchild Semiconductor, South Portland, Me

9/3 "Noise Considerations in Fast Systems"
S. Hinkle, Signetics Corp, Digital Bipolar Div, Orem, Utah

9/4 "FAST—A User's View of Applications—Advantages and Problems"
D. Jensen, IBM, Federal Systems Div, Manassas, Va

9/5 "Design of a Fast System Backplane"
P. Richardson, Digital Equipment Corp, Mid-range Systems, Littleton, Mass

Session 10: Alternatives to Microprocessor Development Systems
Wed 10 am to 12 noon

Chair: M. D. Polen, Applied Microsystems Corp, Redmond, Wash

10/1 "Selecting Development Software—Languages, Performance, and Usability"
S. Wieczner, Boston Systems Office, Waltham, Mass

10/2 "How to Use the Centralized Engineering Computer"
F. Taku, Digital Equipment Corp, Marlboro, Mass

10/3 "Factors in Choosing Programmable Device Support"
R. C. Nyder, Data I/O Corp, Redmond, Wash

10/4 "In-circuit Emulator Options"
S. Rolfe, Applied Microsystems Corp, Redmond, Wash

Session 11: State-of-the-Art Electrically Erasable Memories
Wed 10 am to 12 noon

Chair: S. Young, Exel Microelectronics, San Jose, Calif

11/1 "EEPROM: The Market and Its Growth Potential"
L. Mason, Dataquest Inc, San Jose, Calif

11/2 "RAM-easy EEPROM Design Provides Hassle-free Nonvolatile Versatility"
R. Orlando, Xicor Inc, Milpitas, Calif

11/3 "Designing with 28-pin EEPROM Products"
B. Courlang, Intel Corp, Santa Clara, Calif

11/4 "Revolutionary Advances in EEPROM Features"
S. Grossman, Exel Microelectronics, San Jose, Calif

Session 14: Recent Innovations in Dynamic RAM and Support
Wed 1:30 to 3:30 pm

Chair: Z. Amitai, Monolithic Memories, Inc, Santa Clara, Calif

14/1 "New Concepts in Dynamic RAMS"
F. Jones, Inmos Corp, Colorado Springs, Colo

14/2 "Reducing Soft Errors in Dynamic RAMS"
S. Karoulias, Mitsubishi Electronics America Inc, Sunnyvale, Calif

*Program sessions are subject to last-minute changes.

(continued on page 108)

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CIRCLE 65

(continued from page 106)

14/3 "LSI Control and Error Correction for Dynamic RAMS"
S. Rajpal and Z. Amitai, Monolithic Memories, Inc, Santa Clara, Calif

14/4 "High Speed Memory System Design"
D. Hile, Mosaic Technology, Billerica, Mass

Session 15: Applications of Voice I/O Technology

Wed 1:30 to 3:30 pm

Chair: C. Muther, Votan, Fremont, Calif

15/1 "Military Applications for Voice Technology"
J. Hamilton, SCI Systems, Huntsville, Ala

15/2 "Integrating Interactive Voice Technology into Factory Automation Systems"
A. Cohen, Westinghouse Electric Corp, Pittsburgh, Pa

15/3 "Systems Oriented Design Provides Complete Voice Capabilities on Single Multibus Board"
R. M. Melnicoff, Votan, Fremont, Calif

Session 16: New Tools for Testing Programmable Logic and Digital Systems

Wed 4:30 to 6:30 pm

Chair: V. J. Coli, Monolithic Memories, Inc, Santa Clara, Calif

16/1 "Diagnostic Devices and Algorithms for Testing Digital Systems"
I. Bengali, F. Lee, and V. J. Coli, Monolithic Memories, Inc, Santa Clara, Calif

16/2 "Programmable Logic CAD Tools Enhance Testability"
M. A. Mraz, Data I/O Corp, Redmond, Wash

16/3 "High Level Design with Automatic Function Testing and Large Scale Programmable Devices"
R. K. Scott, Structured Design Corp, Santa Clara, Calif

16/4 "Automatic Test Vector Generation for Programmable Logic"
B. Osann, Assisted Technology Inc, San Jose, Calif

16/5 "The CAD Environment for Programmable Logic Design"
K. Ow-Wing, AMD, Sunnyvale, Calif

Session 17: The 256-K Dynamic RAM

Wed 4:30 to 6:30 pm

Chair: R. Phlegar, Motorola, Inc, Austin, Tex

17/1 "Optimizing System Performance Using High Density CHMOS Dynamic RAMS"
J. Fallin, Intel Corp, Hillsboro, Ore

17/2 "A Quarter-million-bit Solution"
B. Prince, Motorola, Inc, Austin, Tex

17/3 "High Performance 256-K Dynamic RAM"
H. Sussman, Mostek, Inc, Carrollton, Tex

17/4 "A 256-K DRAM Organized for Applications Solutions"
J. O'Hare and G. B. Clark, Texas Instruments Inc, Stafford, Tex

Session 22: Advances in A-D Converters Simplify System Design

Thurs 1:30 to 3:30 pm

Chair: R. A. King, Motorola, Inc, Austin, Tex

22/1 "Practical Techniques for Interfacing the Real World to Microprocessors"
S. Miller, Analog Devices, Inc, Wilmington, Mass

22/2 "New LinCMOS A-D Peripherals Offer High Speed, Cost-effective System Solution"
H. Davoody, Texas Instruments, Inc, Dallas, Tex

22/3 "Serial A-D Makes System Design Easy and Cost Effective"
K. S. Padda, Motorola, Inc, Austin, Tex

22/4 "High Speed 14-bit A-D System Performs Self-calibration"
C. Allen, GE Intersil Inc, Cupertino, Calif

22/5 "A 5-V, Low Power 10-bit CMOS Charge Redistribution A-D Converter"
V. Zazzu, A. Dingwall, and S. Wietcha, RCA, Somerville, NJ

Session 25: High Voltage/High Power ICs

Thurs 4:30 to 6:30 pm

Chair: E. Oxner, Siliconix Inc, Santa Clara, Calif

25/1 "Power Control with Integrated CMOS Logic and DMOS Output"
R. A. Blanchard, Siliconix Inc, Santa Clara, Calif

25/2 "A 500-V Junction-isolated BIMOS High Voltage Integrated Circuit"
E. J. Wildi, General Electric Corporate R&D Center, Schenectady, NY

25/3 "Monolithic Analog Multiplexers for High Voltage Applications"
J. Pohlman, Supertex Inc, Sunnyvale, Calif

25/4 "CMOS Integrates with High Power Devices in New ICs"
G. Fay, Motorola Semiconductor Products Group, Phoenix, Ariz

Session 27: Nonvolatile Memory Alternatives

Thurs 4:30 to 6:30 pm

Chair: S. Grossman, Exel Microelectronics, Inc, San Jose, Calif

27/1 "New Generation ROMS"
P. Koons and C. Zatz, General Instrument Corp, Hicksville, NY

27/2 "The Economics and Applications of EPROMS"
D. Knowlton, Intel Corp, Santa Clara, Calif

27/3 "High Speed PROMS with Onchip Registers and Diagnostics"
V. J. Coli, Monolithic Memories, Inc, Santa Clara, Calif

27/4 "The System Impact of E^2PROM"
R. G. Huff III, Exel Microelectronics, Inc, San Jose, Calif

27/5 "The NOVRAM Family—A New Domain of System Possibilities"
R. Orlando, Xicor, Inc, Milpitas, Calif □

(Conference coverage continued on page 110)

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CIRCLE 66

(Conference coverage continued from page 108)

Professional Program Excerpts*

Session 1: Current Applications of Voice Input and Output

Tues 10 am to 12 noon

Chair: C. L. Berney, Speech Plus, Inc, Mountain View, Calif

1/1 "Cost-effective Voice I/O for Personal Computers"
J. Baker, Dragon Systems, West Newton, Mass

1/2 "Voice Applications in the Office of the Future"
W. F. Rosenberger, Wang Labs, Inc, Lowell, Mass

1/3 "The Human Interaction: A Framework for Operator Expectations"
D. F. Fink, Intel Corp, Santa Clara, Calif

1/4 "A Text Talking Terminal for Proofreading"
L. Storch, Verbal Technologies, Inc, New York, NY

1/5 "Industrial Applications of Voice Input and Output"
R. S. Van Peursem, Eastman Kodak Co, Rochester, NY

Session 2: Latest Developments in Single-chip Microcomputers

Tues 10 am to 12 noon

Chair: B. Huston, Motorola, Inc, Austin, Tex

2/1 "Highly Integrated 16-bit Microprocessor for a Wide Range of Applications"
M. Passi, Intel Corp, Chandler, Ariz

2/2 "New Single-chip Microcomputer Approaches High End Performance"
J. Langan, Motorola, Inc, Austin, Tex

2/3 "Microcontroller Communications for Small Area Network"
A. Kingsbury, Signetics Corp, Sunnyvale, Calif

2/4 "An 8-bit MCU Ideal for Intelligent Telephones"
R. Ott and D. Stanley, RCA, Somerville, NJ

2/5 "New Single-chip Microcomputer Has 16-bit Internal Architecture"
J. Campbell, NEC Electronics, Natick, Mass

Session 3: Digital Communications Networks

Tues 10 am to 12 noon

Chair: C. W. Anderson, New England Telephone Co, Framingham, Mass

3/1 "Digital Communication Networks— A Designer's View"
H. Cravis, A. D. Little, Inc, Cambridge, Mass

3/2 "Digital Communication Networks— A Provider's View"
G. Benjamin, New England Telephone Co, Boston, Mass

3/3 "Digital Communication Networks— A User's View"
D. Dill, Boston University, Boston, Mass

Session 4: Microcomputer Applications in Robotics

Tues 1:30 to 3:30 pm

Chair: R. E. Parkin, Robotics Lab, University of Lowell, Lowell, Mass

4/1 "Vision Processing: The Key to the 'Factory-of-the-Future'"
R. H. Peterson, Synthetic Vision Systems, Inc, Ann Arbor, Mich

4/2 "Advanced Techniques Used in Robotic Vision"
D. Harms, Intelledex, Inc, Corvallis, Ore

4/3 "A Communication Network for Automatic Hybrid Assembly"
D. H. Young, Quad Systems, Horsham, Pa

4/4 "An Inexpensive and Self-calibrating Force Feedback Sensor for Robotic Applications"
R. Meyer, Controlonics Corp, Westford, Mass;
R. Davis, General Electric Co, Lynn, Mass; and
S. Einarson, Varian Assoc, Beverly, Mass

4/5 "A Programmable Obstacle Avoidance System for Mobile Robots"
L. T. Simon and D. Dayton, Wang Labs, Lowell, Mass

Session 5: Architecture for 32-bit Microprocessors

Tues 1:30 to 3:30 pm

Chair: R. Druian, Motorola, Inc, Austin, Tex

5/1 "The MC68020—A Full 32-bit Member of the 68000 Family"
D. Mothersole, Motorola, Inc, Austin, Tex

5/2 "The 32032 32-bit 16000 Family Member"
R. Mateosian, National Semiconductor, Santa Clara, Calif

5/3 "The Z80,000 32-bit Microcomputer"
G. Favor and M. Yamamura, Zilog, Inc, Campbell, Calif

5/4 "The T424 Transputer"
P. Wilson, Inmos Corp, Colorado Springs, Colo

Session 6: VLSI Solutions Promote the Integrated Services Digital Network

Tues 1:30 to 3:30 pm

Chair: F. Cherrick, Intel Corp, Chandler, Ariz

6/1 "CMOS LSI Integration Enhances Voice and Data Networks"
A. Mouton, Motorola, Inc, Austin, Tex

*Program sessions are subject to last-minute changes.

(continued on page 112)

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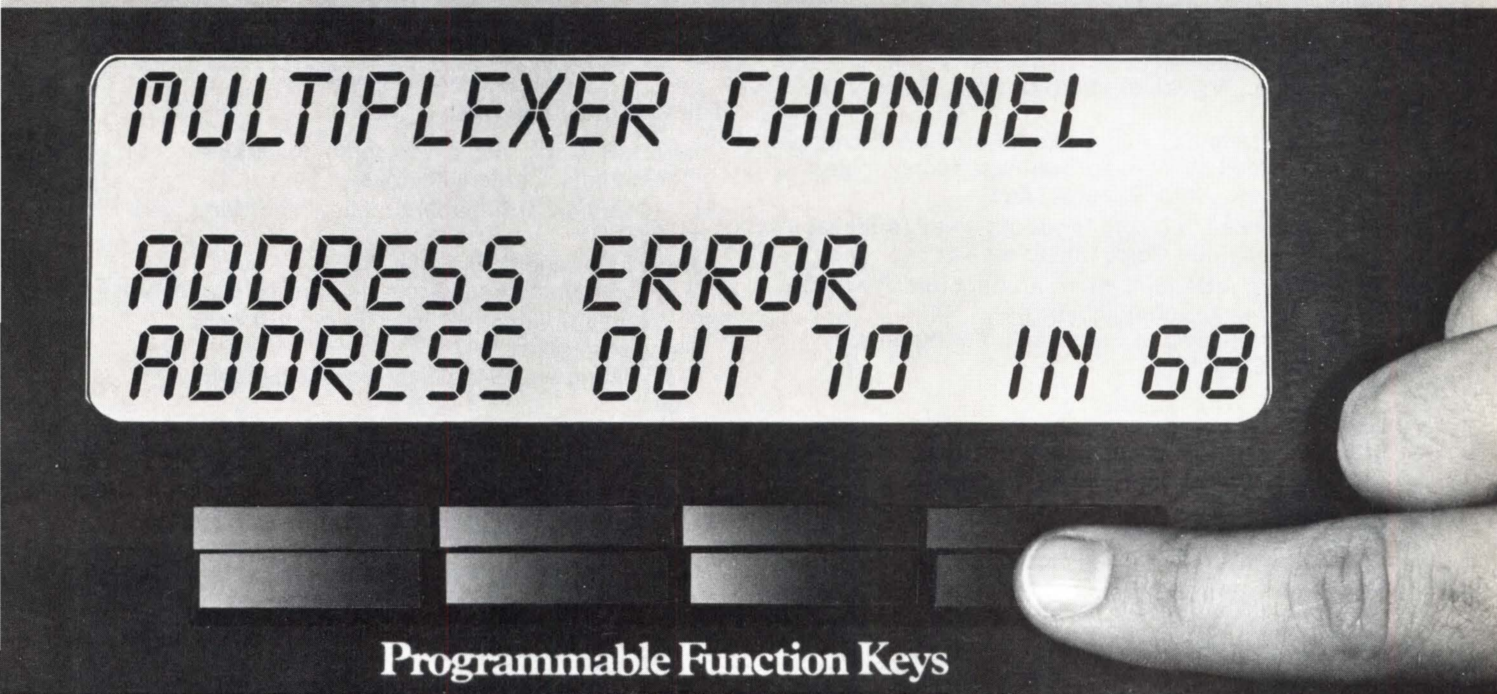

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CIRCLE 67

(continued from page 110)

6/2 "VLSI Technology Evolution Toward Digital Customer Access"
H. Ihrahim, Advanced Micro Devices, Sunnyvale, Calif

6/3 "New Complex Functions for Modern Exchanges Are Provided by World-proven VLSI Technologies"
A. Ugge, SGS Corp, Phoenix, Ariz

6/4 "Enhanced Telecom Products—Key to the ISDN"
C. Stevens, Intel Corp, Chandler, Ariz

6/5 "ST-BUS: A Serial System Architecture Providing Twisted-pair Communication"
B. Broomfield, Mitel Semiconductor, Kanata, Ontario, Canada

Session 7: Industrial Automation for Process Manufacturing

Tues 4:30 to 6:30 pm

Chair: J. A. Ward, IBM Corp, Houston, Tex

7/1 "Integrating Program Logic Controllers to Large Control Systems"
G. Van de Hoef, Waterloo Centre for Process Development, Waterloo, Ontario, Canada

7/2 "The Application of the IBM Personal Computer to a Small Process Control Project"
G. R. Sullivan, Pracon, Waterloo, Ontario, Canada

7/3 "Process Education Using Large-scale Simulation Capability"
L. B. Koppel, Purdue University, West Lafayette, Ind

7/4 "Requirements for a Process Control Oriented Personal Computer"
J. A. Ward, IBM Corp, Houston, Tex

Session 8: Clever Peripheral Integrated Circuits Tackle Demanding Applications Cost Effectively

Tues 4:30 to 6:30 pm

Chairs: T. Marischen, Motorola, Inc, Austin, Tex; and K. Thomas, Zilog, Inc, Campbell, Calif

8/1 "Zilog's Universal Peripheral Controller, a Custom Tailored Microprocessor Peripheral"
K. Thomas, Zilog, Inc, Campbell, Calif

8/2 "Innovative Application of an Intelligent Peripheral"
D. Gonzales, Motorola, Inc, Austin, Tex

8/3 "Serial CMOS Realtime Clock Adds Features while Reducing System Costs"
W. Cohen and D. Derkach, RCA Solid State Div, Somerville, NJ

8/4 "Second-Generation Videographics for Small Computers"
R. Peterson, Texas Instruments, Inc, Houston, Tex

8/5 "Improved Functionality Simplifies Disk Controller Design"
B. Cayton, Standard Microsystems Corp, Hauppauge, NY

Session 9: Fiber Optics in Local and Wide Area Networks

Tues 4:30 to 6:30 pm

Chair: D. B. Brick, Aetna Telecommunications Consultants, Centerville, Mass

9/1 "Overview of Fiber Optic Local and Wide Area Networks"
H. A. Elion and D. B. Brick, Aetna Telecommunications Consultants, Centerville, Mass

9/2 "An Experimental Fiber Optic Local Area Network—'D-NET'"
C-W. Tseng and B-U. Chen, TRW, El Segundo, Calif

9/3 "Light Wave Applications in Telecommunications: Evolution or Revolution?"
A. L. Prest, Western Electric Corp, Burlington, Mass

9/4 "Future Fiber Optic Applications to Air Force Networks"
J. S. Katz, U.S. Air Force, Electronic Systems Div, Hanscom Air Force Base, Bedford, Mass

9/5 "Components and Applications for Fiber Optic Local Area Networks"
M. D. Drake and B. D. Metcalf, The Mitre Corp, Bedford, Mass

Session 10: Pipelined Architectures for High Speed Processing Systems and ICs

Wed 10 am to 12 noon

Chair: S. Rajpal, Monolithic Memories, Inc, Santa Clara, Calif

10/1 "Systems Solution for a High Speed Processor Using Innovative ICs"
N. Lodhi and S. Rajpal, Monolithic Memories, Inc, Santa Clara, Calif

10/2 "Modular Array Processing for Imaging Processor"
A. Lukas, Computer Design and Applications, Waltham, Mass

10/3 "A High Speed Floating Point Accelerator Board"
G. Shapiro, Sky Computers, Lowell, Mass

10/4 "A Use of Modular Array Processor Systems in Signal Processing Applications"
P. Alexander, Numerix Corp, Newton, Mass

Session 11: Protecting and Exploiting Software Developments

Wed 10 am to 12 noon

Chair: M. A. Lechter, Foley & Lardner, Milwaukee, Wis

11/1 "Legal Mechanisms for Protecting and Exploiting Software and Firmware"
M. A. Lechter, Foley & Lardner, Milwaukee, Wis

(continued on page 115)

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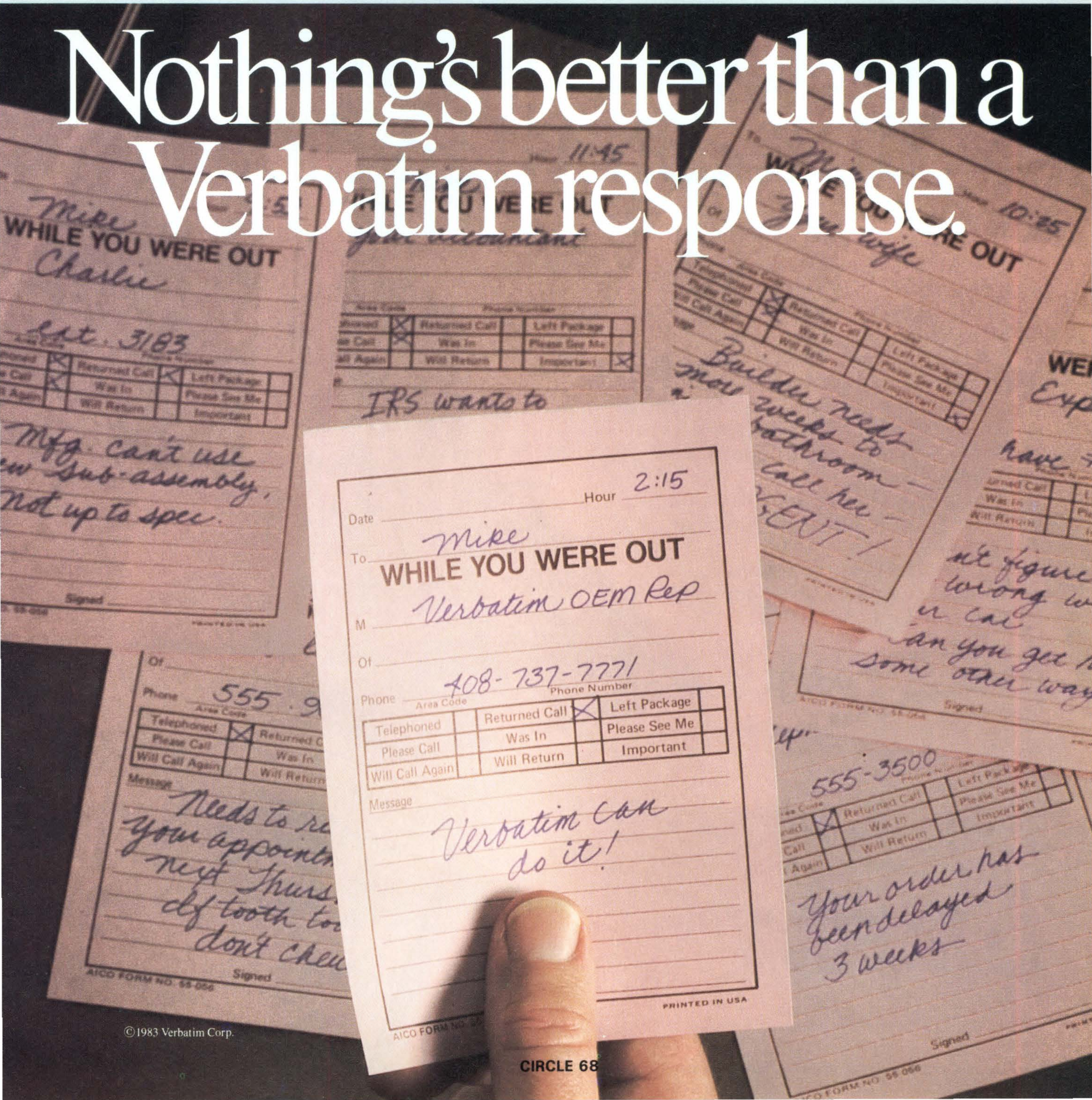

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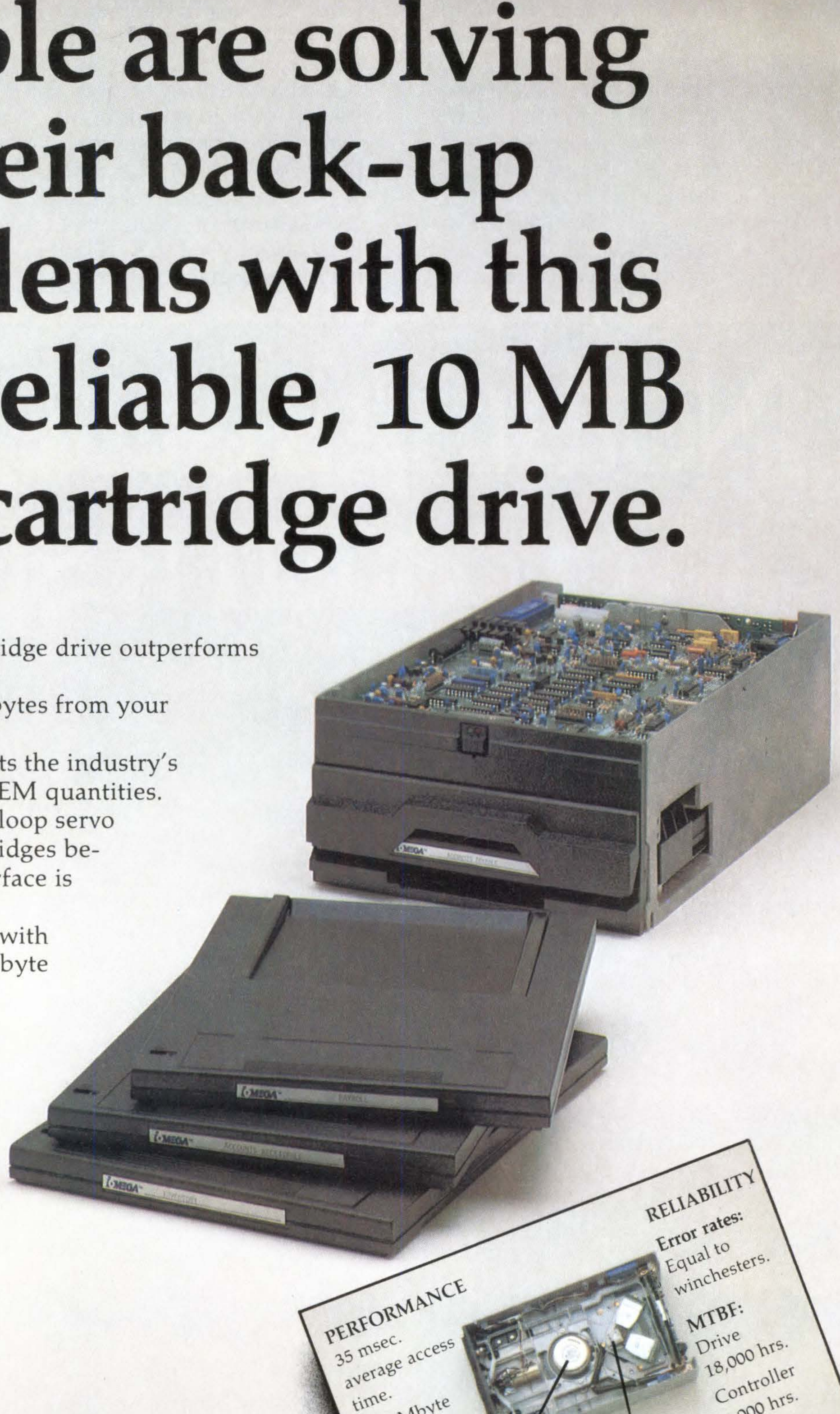

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(continued from page 112)

11/2 "Financing and Tax Aspects of Software Development"
H. Busbee, Coopers & Lybrand, Atlanta, Ga

11/3 "Silicon Solutions to Software Security"
W. W. Wyatt, Motorola, Inc, Austin, Tex

11/4 "Making Money through Software Licensing"
M. Ishimaru, John Fluke Manufacturing Co, Everett, Wash

Session 12: Data Communication—What Does It Mean Today?

Wed 10 am to 12 noon

Chair: A. Goldberger, Exel Microelectronics, Inc, San Jose, Calif

12/1 "The Changing Picture in Data Communications—An Overview"
A. Goldberger, Exel Microelectronics, San Jose, Calif

12/2 "Silicon Solutions for Small Area Networks"
C. Kaplinsky, Signetics Corp, Sunnyvale, Calif

12/3 "Evolution of Tiered Networks for Offices"
B. Dahlberg, Intel Corp, Santa Clara, Calif

12/4 "New Silicon Solutions for Global Data Communications"
P. Madan, Exel Microelectronics, San Jose, Calif

12/5 "Silicon Solutions for Local Area Networks"
B. Segal, Mostek, San Jose, Calif

Session 13: Array Processors

Wed 1:30 to 3:30 pm

Chair: R. C. Borgioli, CSPI, Billerica, Mass

13/1 "The CSPI Line of Array Processors"
T. F. Litrenta, CSPI, Billerica, Mass

13/2 "The FPS Line of Array Processors"
R. E. Higginbotham, FPS Inc, Rockville, Md

13/3 "The Star Technologies Array Processor"
S. Osborne, Star Technologies, Rockville, Md

13/4 "The Numerix Mars-432 Array Processor"
P. Alexander, Numerix Corp, Newton, Mass

Session 14: Alternatives in Graphics System Design

Wed 1:30 to 3:30 pm

Chair: C. M. Collins, Motorola Semiconductor, Austin, Tex

14/1 "The Trend Toward Intelligent CAD Systems"
C. Young and S. Emmons, Michael Leesley Consulting Inc, Austin, Tex

14/2 "Display Processor Architecture in the Tektronix 4115B"
J. C. Dalrymple and S. Bigger, Tektronix IDD, Wilsonville, Ore

14/3 "A Software Perspective for the Design of a Graphics Processor"
J. C. Nash and G. Walker, Motorola Semiconductor, Austin, Tex

14/4 "Graphics for the IRS Workstation"
S. Bourne, Silicon Graphics, Mountain View, Calif

Session 15: LSI Modem Applications

Wed 1:30 to 3:30 pm

Chair: S. J. Durham, Cermetek Microelectronics, Inc, Sunnyvale, Calif

15/1 "CMOS LSI Modem Technology Enhances the Role of the Digital PBX"
A. Mouton, Motorola Semiconductor, Austin, Tex

15/2 "Intelligent 212A-type Modem Integration"
S. J. Durham, Cermetek Microelectronics, Inc, Sunnyvale, Calif

15/3 "1200- to 9600-bit/s Plug-compatible Modem Peripherals"
J. Higgins, Rockwell, Newport Beach, Calif

15/4 "New 1200-bit/s LSI Modem Integrated Circuits"
J. Lange, Exar Integrated Circuits, Inc, Sunnyvale, Calif

(continued on page 116)

(continued from page 115)

Session 16: State-of-the-Art Interactive Software Tools

Wed 4:30 to 6:30 pm

Chair: R. Murray, Analogic Corp, Wakefield, Mass

16/1 "The Programmer's Apprentice: Knowledge Based Program Editing"
R. C. Waters, MIT Artificial Intelligence Lab, Cambridge, Mass

16/2 "InSight: A General Purpose, Multiple-window Management Package"
R. Murray, Analogic Corp, Wakefield, Mass

16/3 "Using the 1-2-3 Macro Command Language"
C. Morgan, Lotus Development Corp, Cambridge, Mass

Session 17: VLSI Alternatives in Graphics System Design

Wed 4:30 to 6:30 pm

Chair: P. Madan, Exel Microelectronics, San Jose, Calif

17/1 "An Innovative VLSI Solution to Video Display Applications"
B. Peterson, Motorola, Inc, Phoenix, Ariz

17/2 "A Unique VLSI Solution for Bit-mapped Graphics"
H. Mason, NCR Corp, Colorado Springs, Colo

17/3 "Novel Graphic System Architectures Using the NEC 7220 Graphics Controller"
H. Assarpour, NEC Electronics USA, Inc, Natick, Mass

17/4 "Dual Controllers Optimize Support of Text and Graphics"
B. May, Intel Corp, Santa Clara, Calif

17/5 "Color Graphics with the Transputer Family"
P. Wilson, Inmos Corp, Colorado Springs, Colo

Session 18: Mainstream Micros for CMOS System Designers

Wed 4:30 to 6:30 pm

Chair: R. Mateosian, National Semiconductor, Santa Clara, Calif

18/1 "The MC6801 Gets a CMOS Cousin"
J. F. Stockton, Motorola, Inc, Austin, Tex

18/2 "NSC800 and NS16000 CMOS Families Span the Full Microprocessor Range"
S. Imsen, National Semiconductor, Santa Clara, Calif

18/3 "The DCJ11 CMOS Microprocessor"
E. Strange, Digital Equipment Corp, Hudson, Mass

18/4 "CMOS 80C86 Gives New Power to Low Power Systems"
W. Niewierski, Harris Semiconductor, Melbourne, Fla

(continued on page 118)

(continued from page 115)

Session 19: Personal Instrumentation

Thurs 10 am to 12 noon

Chair: R. T. Leatherman, Microcosm, Inc, Beaverton, Ore

19/1 "The Personal Computer Software Development Environment"
D. A. Baker, RTCS/Realtime Computer Science Corp, Camarillo, Calif

19/2 "Advanced In-circuit Emulators Hosted on the IBM PC"
R. T. Leatherman, Microcosm, Inc, Beaverton, Ore

19/3 "A Personal Computer-based Interactive Logic Analyzer"
C. Nobles, Northwest Instruments Systems, Inc, Beaverton, Ore

19/4 "A PC-based Programmable Memory and Logic Design Workstation"
S. Walters, Valley Data Sciences, Mountain View, Calif

Session 20: High Performance Microcomputer I/O Subsystems Using the SCSI Bus

Thurs 10 am to 12 noon

Chair: P. Devin, Xebec, Sunnyvale, Calif

20/1 "Small Computer System Interface—What Is It?"
J. Cunningham, Western Digital Corp, Irvine, Calif

20/2 "SCSI Bus Arbitration and Message System"
D. Loski, Shugart, Sunnyvale, Calif

20/3 "SCSI Host Adapter and Controller Command Structure"
J. Lohmeyer, NCR Corp, Wichita, Kans

20/4 "High Performance I/O Subsystems through SCSI"
W. A. Horton, Adaptive Data, Pomona, Calif

Session 21: CMOS Single-chip MCUS Are Opening New Avenues of Applications

Thurs 10 am to 12 noon

Chair: J. Bates, Motorola, Inc, Austin, Tex

21/1 "CMOS Dual Processor"
D. Smith, Rockwell Semiconductor Products Div, Newport Beach, Calif

21/2 "CMOS Processors with Power to Spare"
T. Hardy, Motorola, Inc, Austin, Tex

21/3 "An 8-bit MCU Ideal for Portable Terminals"
D. Stanley, RCA, Somerville, NJ

21/4 "CMOS One-chip Microcontrollers Open New Avenues and Applications"
D. Yeskey, Intel Corp, Chandler, Ariz

21/5 "Super Processing with CMOS"
R. Goburu, National Semiconductor, Santa Clara, Calif

Session 22: Personal Computers: What's Next?

Thurs 1:30 to 3:30 pm

Chair: J. Cohler, *Digital Review* Magazine, Boston, Mass

22/1 "Integrating the PC in the Engineering Environment"
B. J. Fulson, Digital Equipment Corp, Littleton, Mass

22/2 "Networking Personal Computers"
C. R. Larson, Microsoft Corp, Bellevue, Wash

22/3 "Networking Personal Computers for Productivity"
B. Eisenhard, Corvus Systems, San Jose, Calif

22/4 "Microcomputer User Interface Design"
R. D. Briggs, Apple Computer, Marlboro, Mass

Session 23: Popular Serial Buses

Thurs 1:30 to 3:30 pm

Chairs: W. W. Wyatt, Motorola, Inc, Austin, Tex; and Y. Sohn, Intel Corp, Santa Clara, Calif

23/1 "HP-IL: An Ultralow Power Interface Especially for Portable Systems"
S. Harper, Hewlett-Packard Co, Corvallis, Ore

23/2 "Advantages of Serial Processing Techniques"
B. Huston, Motorola, Inc, Austin, Tex

23/3 "A 2.4-Mbit/s Serial Bus for Distributed Intelligence"
C. Yager and Y. Sohn, Intel Corp, Santa Clara, Calif

23/4 "Serial Bus for Realtime Data Acquisition"
J. Moon, Spacelabs, Hillsboro, Ore

23/5 "Super Serial Systems"
J. Magill, Signetics Corp, Sunnyvale, Calif

Session 24: Built-in Test and Fault-tolerant Computer Design

Thurs 1:30 to 3:30 pm

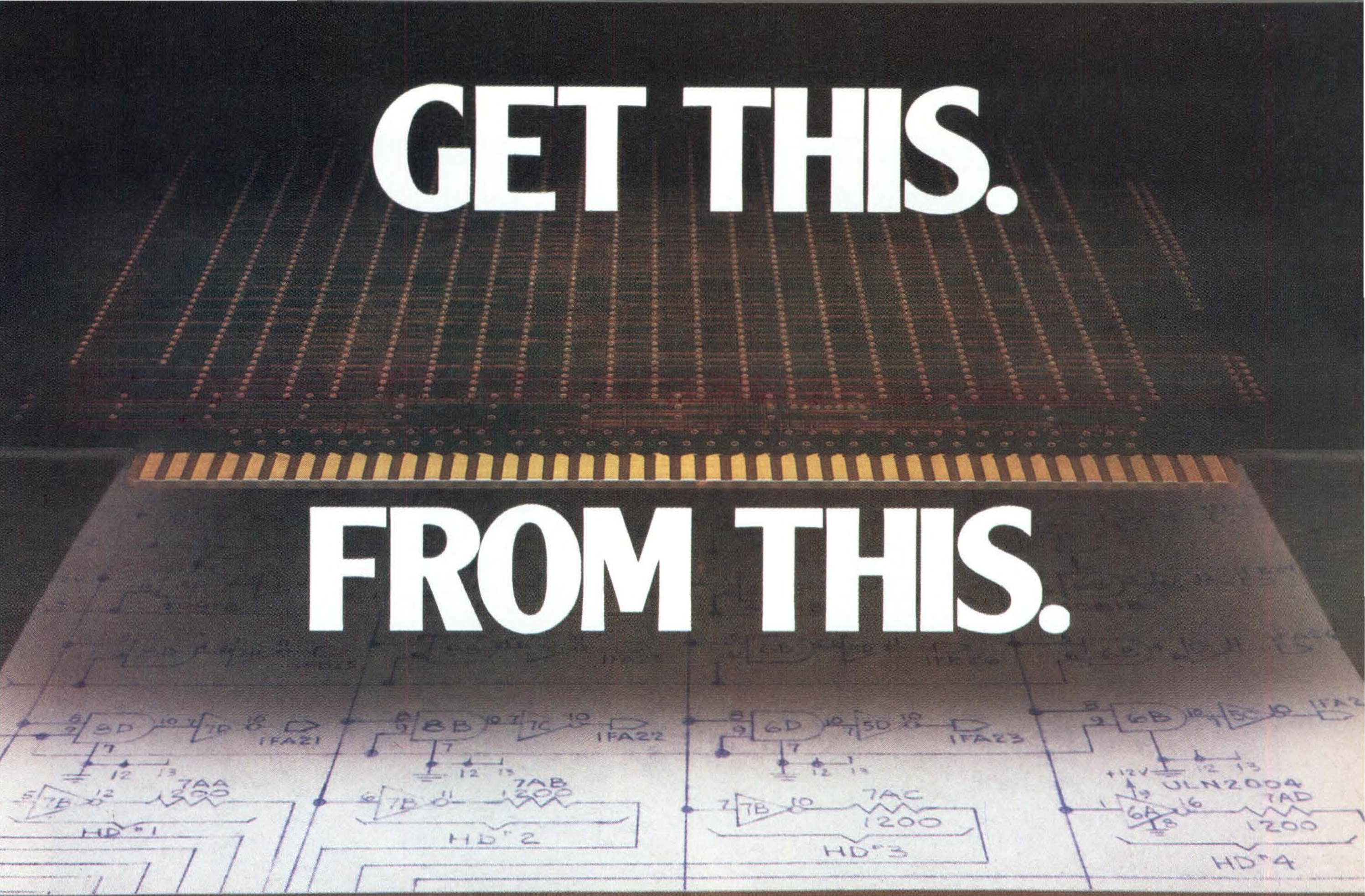
Chair: R. M. Yanney, TRW, Redondo Beach, Calif

24/1 "Recent Advances in Fault Tolerance and Built-in Test"
W. C. Carter, IBM Watson Research Center, Yorktown Heights, NY

24/2 "Built-in Test for Military Computers"
N. Endo, TRW, Redondo Beach, Calif

24/3 "Built-in Test for VLSI"
T. Mangir, UCLA Computer Science Department, Los Angeles, Calif

24/4 "Fault Tolerance in Spaceborne Systems"
H. Hecht, SoHar Inc, Los Angeles, Calif □



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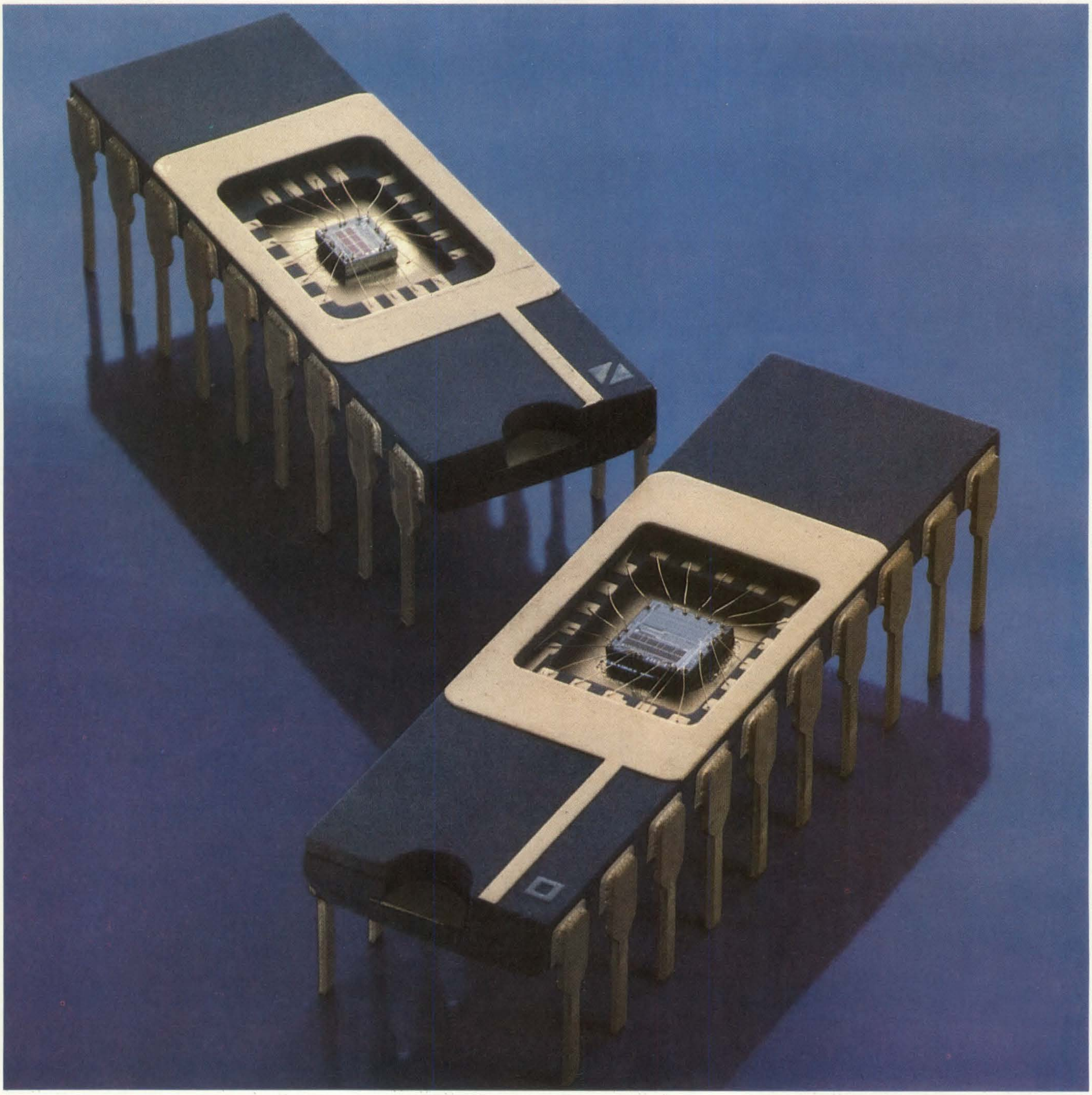
CIRCLE 74



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CIRCLE 76

Computer Graphics '84

Anaheim Convention Center, Anaheim, California **May 13 to 17, 1984**

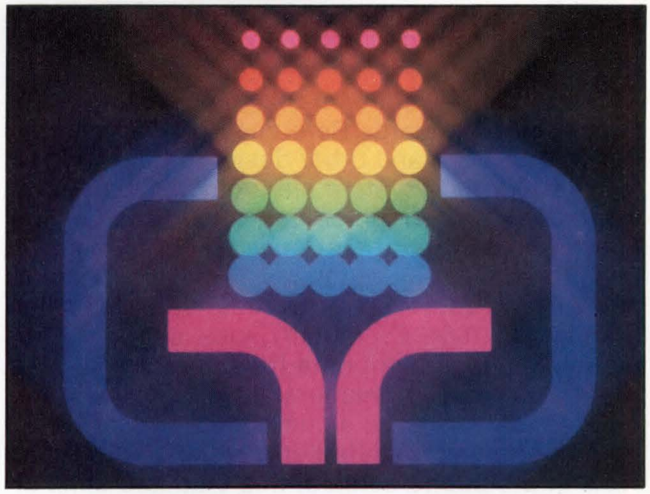
Next month, the National Computer Graphics Association's fifth annual conference will be the focal point for assessing many aspects of graphics technology and applications. From desktop computer aided design/computer aided engineering to realtime supercomputer simulation, graphics system technology is becoming as instrumental to the process of computer design as it is to the development of sophisticated applications on installed computers. More of a grace note just a few years ago, computer graphics today has become a vital entree to new vistas in computer system design. Increasingly sophisticated technology behind intelligent displays is interactively manipulating object geometry to help interpret complex data of every ilk.

Acknowledging that microcomputers are masterminding a hefty palette of technical, industrial, and commercial graphics applications, the Computer Graphics '84 program committee plans to focus on this field. Overall, the 70-paper technical program will examine the role of computer graphics from microprocessor to mainframe in over 20 areas. Chief among these will be architecture and engineering, pattern recognition and image processing, computer-integrated manufacturing, and artificial intelligence.

Two closely related sessions will cover future software and hardware directions. Speakers plan to analyze the influence of graphics support software on hardware display implementation, and speculate about the ramifications of integrating graphics windows and icons into system software. Other issues will include the impact of standardized software interfaces on a distributed graphics system, and the interface from Ada to Graphical Kernel System (GKS) functions. On the hardware side, speakers will project developments in computer aided digitizing, realtime solid image manipulating, interactive videodisk systems, and new hardcopy techniques.

Together, the conference program and exposition are expected to draw over 25,000 attendees. Over 200 companies specializing in integrated systems, peripherals, storage media, and components will exhibit. Throughout the week, a series of forums will allot exhibitors 25-minute platforms for presenting their wares in a theater-style setting.

For the forward-looking, perhaps the most important sessions at this year's Computer Graphics conference will cover evolving industry standards. Several presentations will mark progress toward international guidelines and spell out key specifications for the chief



interfaces. Panelists will debate the status of the major players and how they relate to one another. A subsequent session will focus on user experiences with the various standards. In addition, a three-day session will explore development and applications of the GKS.

Gene Lynch, senior human factors engineer at the Tektronix Information Display Div (Wilsonville, Ore), contends that the keys to successful standards are compatibility, timeliness, and wide use. To that end, the NCGA's Technical Research and Standards Committee bases its *raison d'etre* on clarifying and promoting standards that shape the international graphics industry.

Toeing a standard line

All in all, two types of graphics standards concern the computer industry: those pertaining to hardware and software technology, and those pertaining to ergonomics. Speaking for NCGA, Lynch will take stock of existing guidelines and ergonomics legislation that is coming to bear on the graphics industry. Specifically, he will address NCGA's endorsement of the draft proposal for adopting GKS as an American national standard in cooperation with the International Standards Organization's (ISO) GKS.

To manage that and other efforts, Lynch points to the need for a certification body. For instance, while the American draft proposal of GKS contains a mechanism to standardize language bindings, and a Fortran binding has already been implemented, the C binding will be trickier because that language has yet to be standardized itself. In addition, although the developing Programmer's Hierarchical Interface to Graphics (PHIGS) standard is a promising potential guideline for integrating software into dynamic systems, many anticipate compatibility

(continued on page 124)

(continued from page 123)
problems with the GKS. Furthermore, Lynch indicates that the North American Presentation Level Protocol Syntax (NAPLPS) is ripe for misuse if it is mistaken for a generalized Virtual Device Interface (VDI).

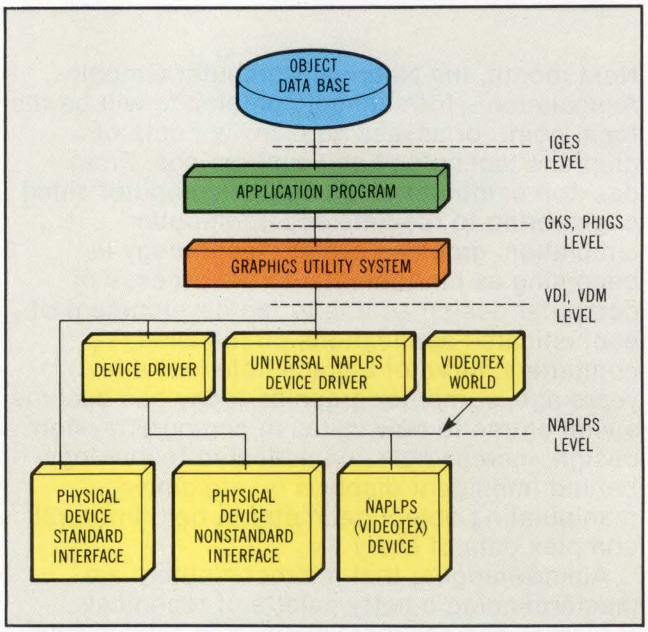
The American National Standards Institute (ANSI) X3H34 Standards Reference Model charts out where these and other design guides fit into today's graphics system hierarchy. At the lowest level, the Initial Graphics Exchange Standard (IGES) is a file format that links an object data base to application programs. First published in 1980, it was approved as an American national standard in 1981. Essentially, IGES is a machine-independent data format that describes product design and manufacturing information created and stored in a computer aided design/computer aided manufacturing (CAD/CAM) system. Now in the public domain, this standard aims at achieving portability among CAD/CAM systems from different manufacturers.

Next in the hierarchy come GKS and PHIGS, which work between an application program and a graphics utility system. The GKS is a software standard for two-dimensional computer graphics. Originally developed by the Deutches Institut für Normung, the West German standards-making group, the GKS is about to become an American national standard as well as an international standard.

A proposed standard device-independent interface is the VDI, which is a two-way communication protocol between the graphics utility system and device-dependent drivers. A working draft of the VDI proposal should be ready for public review by May 1985, and final ANSI review by early 1986. The VDI has not yet been submitted to ISO as a work item.

VDI functions will divide into device classes (most likely input, output, and input/output) and function sets (required and nonrequired). Each device in a given class will have to support a basic set of required functions; beyond these, the unit will be free to select one or several options. Option sets will comprise required and nonrequired functions. A device will be able to support some (or none) of the options, but, if it does support a particular option it will have to support all the required functions of that option set. An attendant set of inquiry functions will enable the device-independent part of the graphics package to determine what a particular graphics device offers.

Preliminary review of the Virtual Device Metafile (VDM), which was pushed ahead of the VDI work, designates a standard, device-independent means for transferring picture files from one graphics device to another. The VDM creates a device-independent vehicle for transferring picture information from one unit to another. It targets a completely different level of application from that of the IGES. By far a more comprehensive standard, IGES will provide for transferring a complete product data base—encompassing geometric and nongeometric information—across CAD/CAM systems. The VDM aims to convey an image from one graphics machine to another without redrawing.



ANSI X3H34 **Reference Model**

At this point, the approaches of the American Graphics Standards Planning Committee Core-system metafile and the international GKS metafile differ. The Core-system metafile looks like another graphics device to the device-independent graphics system. Moreover, Core-system metafiles function independently of the graphics system and range from basic graphic elements to a full system. GKS metafiles, on the other hand, do not look like another graphics device. Rather, they are tightly coupled to GKS, appearing to the GKS metafile as a chain of application subroutine calls. After being read by GKS, each metafile is returned to the application program.

The VDM, jointly approved by ANSI and ISO last year, is up for first public review through May 6, 1984. Final joint approval is anticipated for early 1985. To satisfy both American standard and international standard perspectives on metafiles, VDM specifiers are seeking a middle ground. Each picture will be defined individually in two dimensions. The resultant international guidelines will support GKS level 0 and Graphics Standards Planning Committee Core-system functions, except for segmentation and three-dimensionality.

(continued on page 126)

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(continued from page 124)

The proposed NAPLPS standard uses concise byte-coding sequences to describe a picture comprised of graphics and text. It is thought of primarily in terms of enhanced videotex, but it is also being used to encode graphics and text for computer aided instruction and graphics software packages. Though such applications arouse concern over possible conflict between NAPLPS and GKS, in fact NAPLPS complements rather than competes with the GKS. The two address different needs.

For the most part, NAPLPS is device independent because coordinates are plotted on a unit screen, regardless of physical size or resolution; all the coordinates exist in a fraction of the area described from location 0,0 (lower left) to 1,1 (upper right). As a result, object size and location reference the edges of the unit screen instead of a particular physical or logical quantity.

While he is a proponent of the presentation-level protocol, Mark Gordon, marketing manager of Verticom, Inc (Sunnyvale, Calif), maintains that NAPLPS has its drawbacks in graphics applications. For example, the screen is always one unit in the X dimension, but the Y dimension can vary between 0.75 and 1.0. Gordon suggests that created pictures avoid valid data in the Y region above 0.75 in order to stay compatible with devices having a 4:3 aspect ratio.

Also, Gordon explains that polygons displayed on low resolution devices, which discard unused bits of resolution, can accrue significant errors. This comes about when vertices defined by a series of relative coordinates are drawn closely together. For instance, if a host computer—which computes and sends NAPLPS sequences to a decoding device—keeps a larger number of significant bits than the decoding device uses, the decoder will draw coincident points that the host considers to be discrete. This problem is overcome by establishing coordinates inside that are more precise than those the decoding device can actually display. (For a closer examination of NAPLPS, see article on p 53 of this issue.)

Shaping a less tangible construct: ergonomics

The user interface architect is an indispensable intermediary between the prospective computer operator and the computer builder, according to James Foley, chairman of the Human Factors session at Computer Graphics '84. Foley, professor of electrical engineering and computer science at George Washington University and president of Computer Graphics Consultants (both of Washington, DC), compares the interface designer's role in computer design to the architect's role in building construction.

Pressure from all sides is driving the industry to take care of ergonomic concerns, and Foley joins his peers in recommending that a new job niche be created to do it right. The ideal user interface architect's background will embrace computer science, perceptual and cognitive psychology, graphic arts, and human factors. As he sees it, the quality of human/computer transactions can be responsible for more than high productivity or low fatigue at the end of the business day. Now that computer systems are penetrating every facet of command, control, and operational functions, weak interface design can literally become a matter of life and death.

From the technical user's standpoint, Gene Lynch notes that interactive graphics technology has spurred a marked change in the way we engineer. Reading between the lines, we can expect that desktop CAD and computer aided engineering (CAE) stations will go beyond revolutionizing product design cycles and shortening product lifetimes. They will also create new considerations for interfacing computers with creative technical users.

Technical preview

An interactive display architecture that attempts to render images stored in complex data bases more efficiently than expensive CAD/CAM systems—but with relatively uncomplicated hardware—will be introduced by Marc Berger, University of Colorado (Colorado Springs, Colo) and Sushing Chen, National Science Foundation (Washington, DC). They propose a software structured hierarchical model that compresses image data to expedite refresh, scan conversion, and dynamic changes.

The scheme segments each geometrical object into display file blocks. Then each block assumes a separate layer at a different resolution so it can be encoded independently. Parallel architecture puts one encoding processor and an associated encoded image at each level in the pyramid. Moreover, the technique eliminates the most expensive part of the image generation process by incorporating in the image space hierarchy operators that compute cell coordinates, level, and intensity. These operators (which would probably reside in a special processor) allow the user to alter an image without having the system recompute scan conversion steps.

—Deb Highberger, Senior Associate Editor

For registration information, contact the National Computer Graphics Association, 8401 Arlington Blvd, Suite 601, Fairfax, VA 22031. Tel: 703/698-9600

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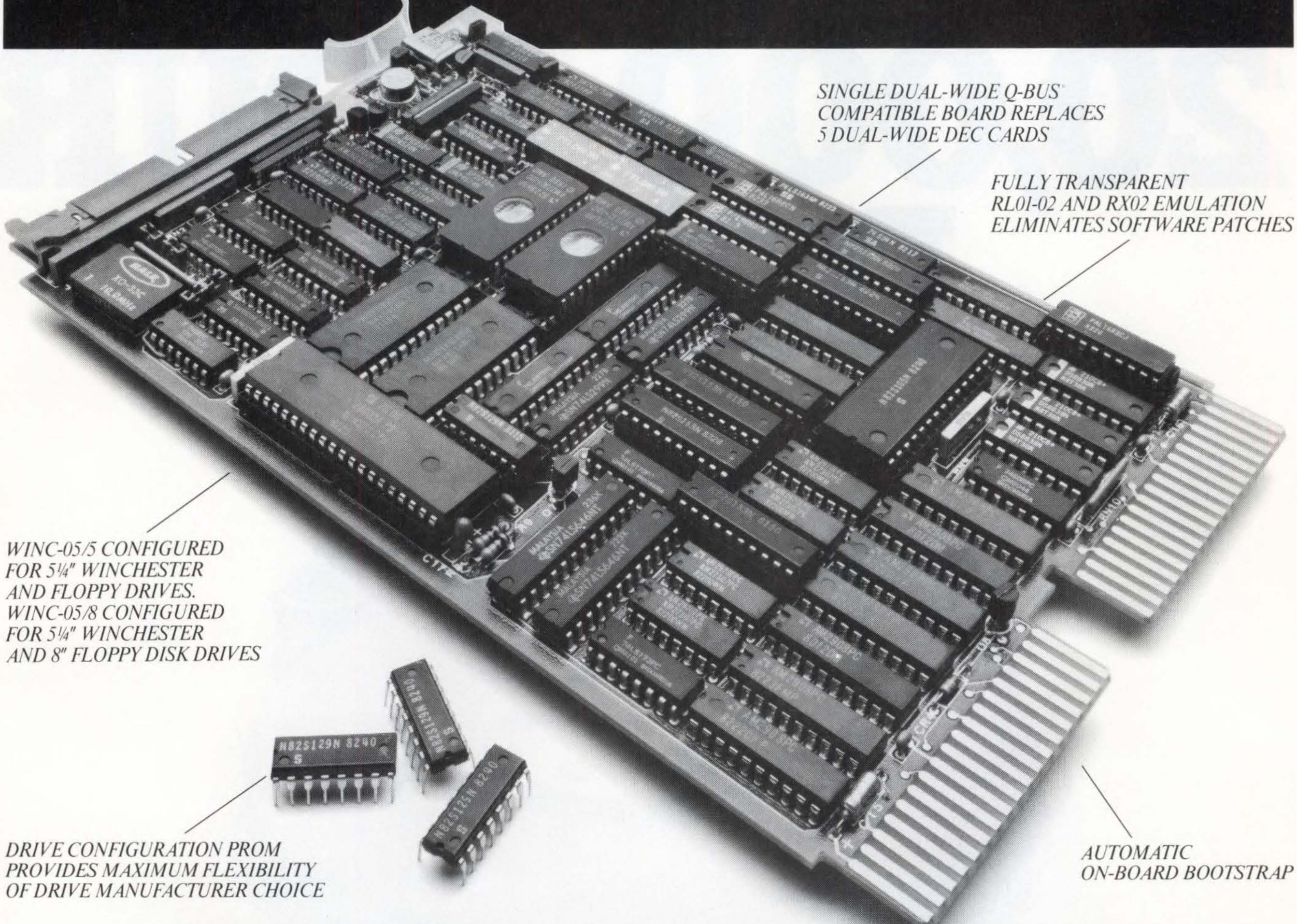

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CIRCLE 78

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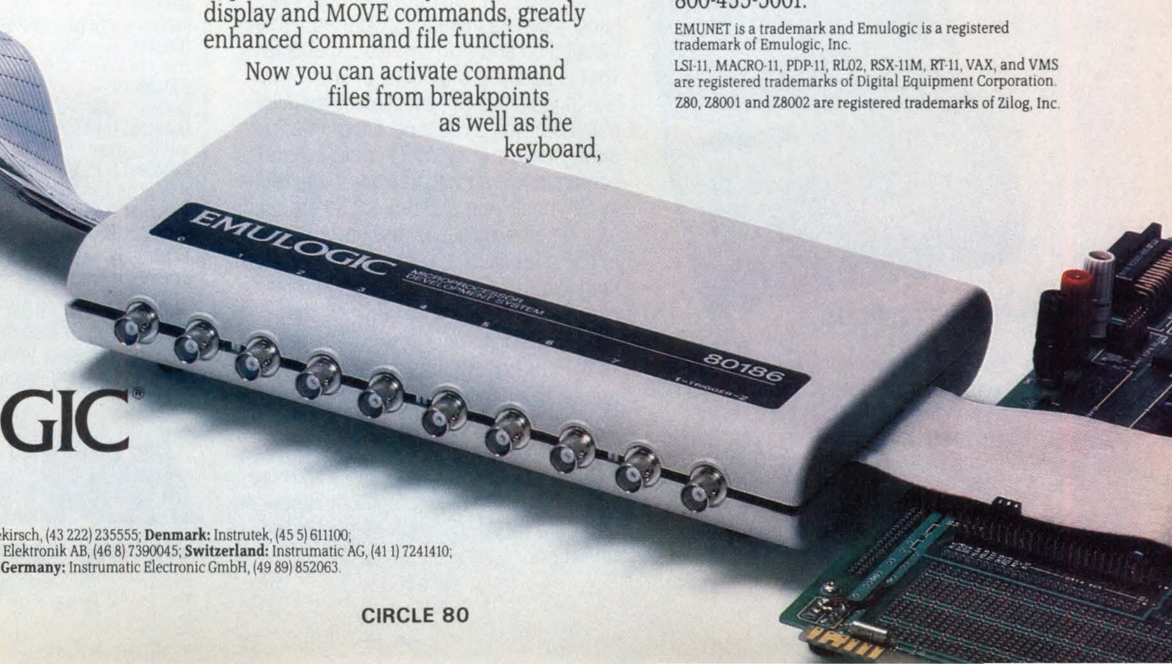

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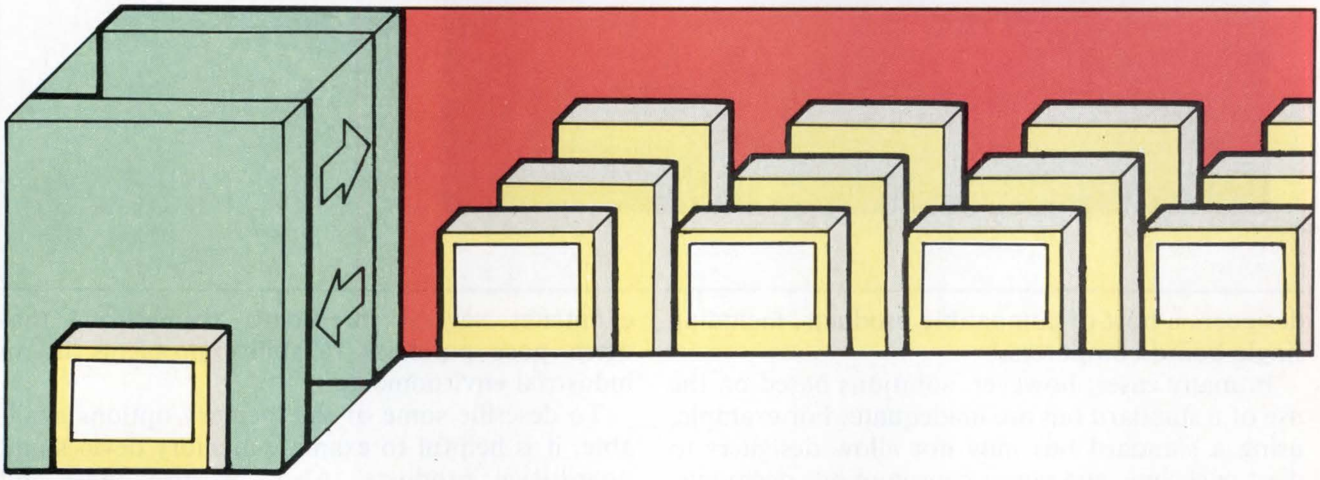
CIRCLE 80

MEMORY COMPONENTS SERVE INDUSTRIAL CONTROL NEEDS

Including chip- and board-level products, as well as complete subsystems, a variety of memory devices and assemblies help designers bring computer technology to the factory floor.



by Rick Nelson, Contributing Editor

Availability of rugged memory components and subsystems is fueling the growth of microprocessor technology throughout industrial environments. Such memory products are performing tasks that previously required complicated hardwired control systems and constant intervention of highly skilled operators.

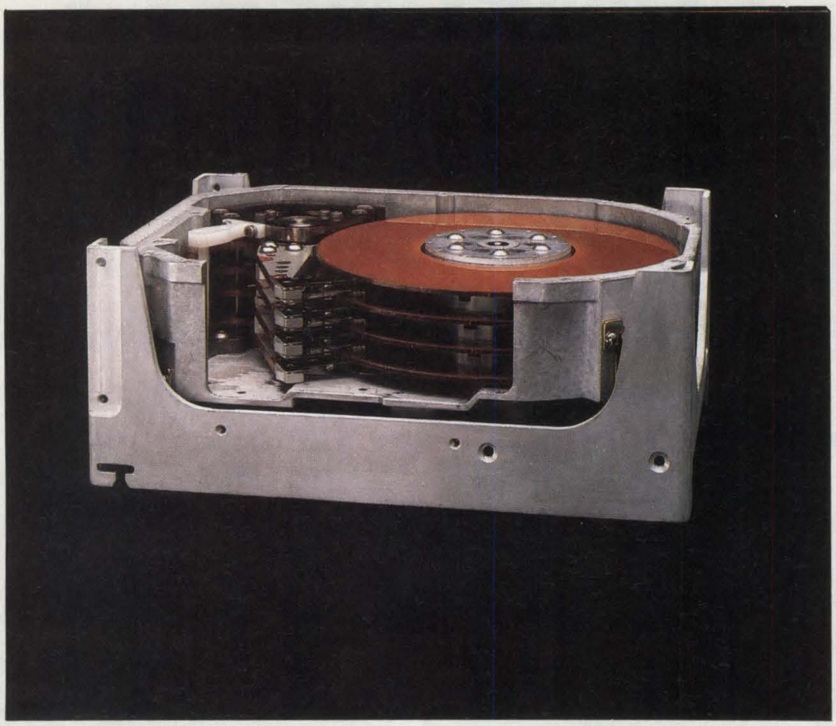
Prior to the development of the microprocessor, computer-based industrial control systems were designed around mainframes or minicomputers. Out of necessity, both computers and associated memory devices had to be isolated from the processes being controlled. They could not function properly in association with temperature extremes, power fluctuations, and harsh environments.

However, the advent of microprocessor technology offered a partial solution to such problems. Because microprocessors do not require a computer room environment, they have the ability to operate at the site of the process being controlled. Of course, this means that the memory devices must also be able to function under the same conditions.

Now, a variety of high density, low power memory devices as well as easy-to-use subsystems are available for industrial applications. They range from electrically erasable PROM, RAM, and bubble-memory devices to board-level products employing those chips. And, although they do not offer the reliability of their solid state counterparts, rotating storage subsystems (including disk and tape drives) should be considered for industrial applications. Many such subsystems also include features that enable them to tolerate harsh factory environments.

Memory options abound

The solid state memory products that system designers can most easily use are board-level products. Such memory boards are designed to interface with standard microprocessor buses, such as the Multibus and the STD bus—two bus configurations often used in industrial applications. Because each of these buses is supported by more than 100 manufacturers, selection of such a bus ensures



To isolate their head disk assemblies from shock and vibration, Micropolis's 1300 series 5¼-in. Winchester disk drives feature a chassis-within-a-chassis construction. One model in the series provides 83 Mbytes of storage.

designers a host of compatible products, including single-board computers.[1]

In many cases, however, solutions based on the use of a standard bus are inadequate. For example, using a standard bus may not allow designers to meet packaging and power consumption constraints. Yet, using custom boards for high volume designs might prove more cost effective than using off-the-shelf boards. Designers may even need to design their own boards, employing such memory devices as standard RAMs and PROMs, if none of the standard bus boards offers the combination of features needed for a specific application. Designing battery-backed CMOS RAMs, EEPROMs, or nonvolatile RAMs (NOVRAMs) can help designers meet data-retention requirements.

To illustrate the flexibility that custom designs allow, consider the following design of a custom board for a robotics application.[2] The board features eight processors, including six 8-bit, axis-control processors with associated RAM and erasable PROM, as well as such devices as A-D converters and timers. A 16-bit processor, one with as much as 256 Kbytes of RAM and 64 Kbytes of EPROM, serves as the master processor, and a final 8-bit processor serves as backup. This complex design example, which does not lend itself to a standard bus solution, illustrates the importance of memory devices in industrial applications and demonstrates the advantages available to designers of custom boards. For example, the single-board solution eliminates several interboard connections that often pose potential reliability problems in an industrial environment.

To describe some of the memory options available, it is helpful to examine memory devices and board-level products. Also, because chips and board-level products are not the only solutions to industrial data storage, it is important to analyze magnetic tape and disk drives that can serve in applications requiring mass-storage capacities, for which semiconductor memory may not be practical.

Chips suit industrial control

It is easy to find a solid state memory chip that can be used in industrial control applications. Designers need only search through various manufacturers' data sheets to find RAMs and ROMs with the power consumption, access time, storage capacity, and temperature range specifications necessary for a given application. Nevertheless, some devices are particularly well suited for industrial control applications.

Military versions of standard parts, for example, should be more than adequate to handle even extremely harsh industrial environments. Such parts can typically operate from −55 to 125 °C. Since many parts are available in military configurations, designers have considerable flexibility in selecting components. Two of the newest military-grade memory devices are Intel's (Chandler, Ariz) model M27128 ultraviolet EPROM and model M2164 dynamic RAM. The EPROM operates over the −55 to 125 °C military temperature range while the DRAM operates from −55 to 110 °C.

The EPROM is a 16-K x 8-bit device that features a 250-ns maximum access time and is designed to work with high speed processors used in avionic systems. It operates on a single 5-V supply, drawing 150 mA during normal operation and 50 mA in its standby mode. It also incorporates Intel's Inteligent Programming algorithm, which permits the entire device to be programmed in 3 min, compared to the 14 min that a standard programming method requires. It is fabricated using Intel's HMOS-E technology, an NMOS process.

Intel's military-grade DRAM features a 64-K x 1-bit configuration and a 150-ns access time. Operating on a single 5-V supply, the device draws 55-mA active current or 5-mA standby current. It has a high memory cell capacitance to reduce software error rates to less than 0.1 percent per 1000 hours.

However, it should be noted that using military-grade devices can be overkill for industrial applications requiring neither operation over the full military temperature range nor the strict testing procedures mandated by military specifications. It can be expensive overkill as well—the M27128 EPROM sells for $412 in quantities of 100; near the other end of the EPROM price/performance spectrum, a 64-Kbit version of Intel's plastic, window-less EPROM is only $6.60 in manufacturer quantities. The company's production EPROMs are also available in 32-Kbit versions (with access times as low as 200 ns). These window-less devices are designed to be programmed only once and are aimed at cost-effectively meeting volume production needs.

Among other chips suited to industrial use, any CMOS memory part operates well in harsh environments because of its noise immunity and low power consumption. These are two attractive factors for industrial applications where power lines are prone to disturbances from heavy inductive loads. In addition to facilitating battery backup, the low power consumption of CMOS limits heat dissipation during normal operation, thus making it easy to design CMOS devices into dust- and oil-tight enclosures that can protect circuitry from harsh industrial atmospheres.

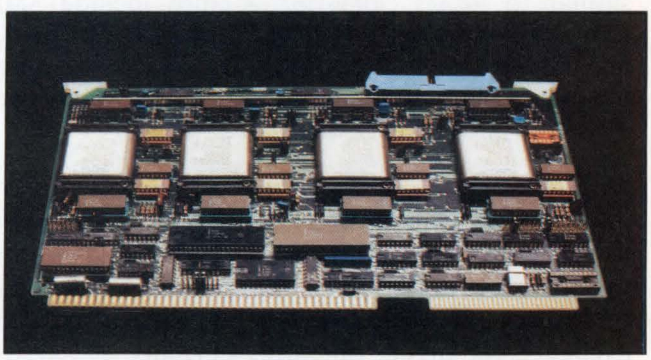
CMOS chips, however, are not always ideal for industrial applications. They are usually more expensive than their NMOS counterparts, and devices such as mask-programmable CMOS ROMs may not offer sufficient flexibility for process-control system design. Despite their typical low current drain, CMOS gates can consume considerable power during switching, making CMOS chips more power hungry at high frequencies. When using CMOS, designers thus face a trade-off between low power consumption and operating speed. To serve applications that can tolerate higher power dissipation in order to obtain higher speeds during normal operation (but that require low power consumption for memory retention during power outages), many CMOS parts feature standby modes that permit low power data retention.

Nonvolatile chips retain data

Other devices particularly suited to industrial environments include EEPROMs and NOVRAMs. For industrial control applications, EEPROMs can store programs and process parameters that do not need to be changed often. They continue storing such information throughout power failures or equipment shutdowns until they are reprogrammed with new process data. NOVRAMs can similarly maintain data during power outages; they operate as RAM during normal operation but act as ROM when power is removed. Bubble memories, which are nonvolatile, also suit industrial applications by combining the reliability of solid state devices with the capacities of mass-storage subsystems.

In the CMOS technology area, RCA's Solid State Div (Somerville, NJ) offers a selection of CMOS RAMs and ROMs. RCA's newest ROM (model CDM53128) is a 128-Kbit, mask-programmable device (arranged in a 16,384 x 8-bit configuration) with a 250-ns access time. The chip's power consumption characteristics demonstrate the dependence of CMOS parts' power consumption on operating frequency—current drain is 30 mA at a 250-ns cycle time but only 10 mA at a 1-μs cycle time. In standby mode, selected via the chip's CE1 and CE2 pins, current drain is 2 μA typical, 50 μA maximum. Plastic-packaged devices operate from −40 to 85 °C; ceramic units operate from −55 to 125 °C.

Mask-programmable ROMs can have drawbacks in industrial applications as well. They are economical only in large quantities. Also, turnaround time for samples is typically five weeks after RCA receives the customer's program pattern on a master device, floppy diskette generated on an RCA



This version of Intel's Multibus-compatible iSBX 254 board contains four 1-Mbit bubble-memory devices, for a total capacity of 512 Kbytes. Other versions of the board are available with 1- and 2-Mbit capacities. The boards are supported under RMX/80 and /86 realtime multitasking operating systems for use with compatible microcomputers in industrial applications.

development system, or on computer cards. Production quantities are typically available in eight weeks. Thus, in low volume, process-control applications where ROM program changes can be expected, user-programmable devices such as EPROMs may be a better choice.

RCA also offers a line of CMOS RAMs, including 2-K x 8-bit devices available in three versions. These offer a trade-off between operating speed and power consumption. The versions are functionally identical, with the exception of their pin 20. That pin serves an output-enable ($\overline{OE}$) function on the CDM6116 version, a chip-select ($\overline{CS}$) function on the CDM6117, and a chip-enable ($\overline{CE1}$) function on the CDM6118.

The version with the $\overline{CE}$ function offers the lowest power consumption. When that input is false, read/write functions are disabled, regardless of the state of the chip's write-enable ($\overline{WE}$) pin, and the chip goes into a reduced-power standby mode. A microprocessor can strobe the $\overline{CE}$ input to activate the chip only during the access portion of a memory cycle. This reduces average operating power but increases access time by approximately 100 ns compared to faster versions.

The versions with the $\overline{OE}$ and $\overline{CS}$ functions at pin 20 can operate at higher speeds—for example, the 6116's read/write cycle times equal 150 ns. The $\overline{OE}$ function controls the output buffers to prevent bus-contention problems without disabling the rest of the chip, therefore allowing the higher speeds. The $\overline{OE}$ function, however, does not place the device in a low power mode. Similarly, on the 6117 version, pin 20 serves as a ($\overline{CS}$) function that can disable the chip's output drivers and read/write functions but cannot establish a low power standby mode. All three versions include a standby mode that can be enabled by their pin 18. This mode limits current drain to 100 μA or less, compared to the normal 20-mA (typical) operating currents.

Other manufacturers offering CMOS RAMs similar to RCA's CDM6116/7/8 chips include AMI (Santa Clara, Calif), Fujitsu (Santa Clara, Calif), and Harris (Melbourne, Fla). Harris also offers a line of 16-Kbit CMOS PROMs and plans to introduce a 64-Kbit model early this year.

Modern EEPROMs operate on one voltage

Despite the low power standby modes of CMOS RAMs, those devices do require battery backup to maintain data during power outages. Since they offer a battery-free alternative to data retention in exchange for higher operating currents, EEPROMs maintain data throughout power losses by acting as ROMs, but they can be reprogrammed in circuit. Although early EEPROMs required special voltages (typically 21 V) for reprogramming, modern devices can be reprogrammed while operating on a single 5-V supply.[3] Moreover, earlier models often required that a complete array or page be erased before new data could be written. Today, modern devices permit single bytes to be modified without disturbing other data, and they automatically handle erase operations as part of their write cycles.

One such device is Intel's (Santa Clara, Calif) model 2816A, a 16-Kbit unit. It includes an onboard 5- to 21-V charge pump that allows it to operate on a single 5-V supply. Write operations take 9 ms; read operations require only 150 ns.

EEPROMs and NOVRAMs are well suited to industrial environments.

Xicor (Milpitas, Calif) similarly offers a 16-Kbit EEPROM that features a write time equal to 10 ms maximum, and read time specifications at 350 ns maximum. The firm also offers a 64-Kbit unit (model X2864A), which operates on a single 5-V supply. Access time is 350 ns; write time is typically 5 ms for 1 byte. Moreover, the device includes a 16-byte latch that allows reprogramming of as many as 16 bytes in one write cycle. This yields a 300-μs/byte effective write time. Normal chip current drain is 110 mA; a standby mode reduces current drain to 50 mA.

Despite the X2864A's impressive effective write time, EEPROM write times are still considerably slower than RAM write times. Overcoming this drawback (in exchange for reduced memory density) is Xicor's line of NOVRAMs. These devices require only a 5-V supply and incorporate a static RAM with a shadow EEPROM memory. The devices are fabricated using the company's n-channel floating gate MOS technology.

During normal NOVRAM operation, data read and write transactions operate at high speeds within the RAM. By putting the device's TTL-compatible $\overline{STORE}$ input low, RAM contents are transferred to the EEPROM section, where data is maintained during a power outage. Since the store operation requires 10 ms, $\overline{STORE}$ must be pulled low at least 10 ms before chip power is removed (Fig 1). This timing requirement can be easily met in most designs that use switching power supplies for system power because switchers typically provide at least 16 ms of ride-through time after a power outage. Thus, if $\overline{STORE}$ is pulled low immediately after detection of an input ac line power failure, the switcher's ride-through capability will power the chip long enough to ensure data transfer to the shadow EEPROM.

A pin labeled $\overline{ARRAY\ RECALL}$ is used to transfer data from the EEPROM back to the RAM. A low level on this pin initiates data transfer to the RAM. Any data in the RAM is overwritten, thus leaving the EEPROM contents unchanged.

Xicor NOVRAMs in 18-pin packages feature 256- x 4-bit, 64- x 4-bit, and 1024- x 1-bit configurations; a

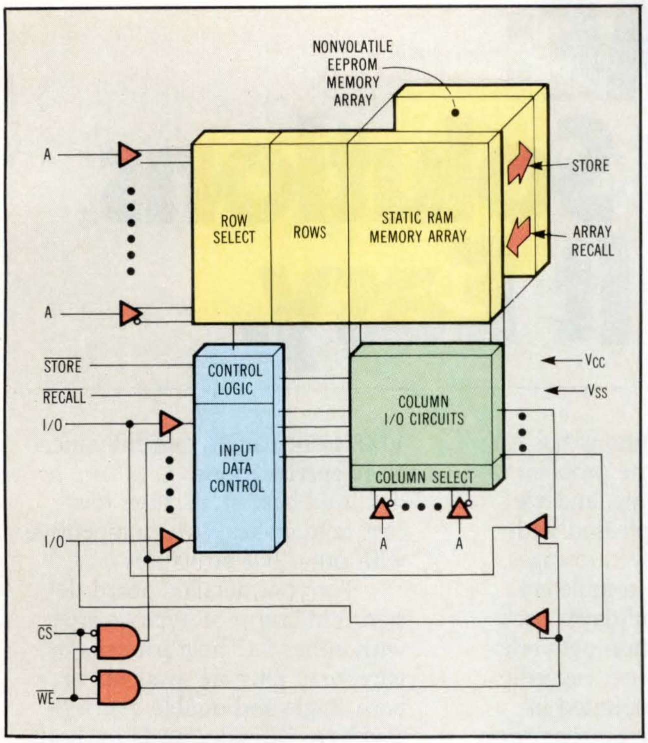


Fig 1 Essentially a static RAM backed up by an EEPROM, Xicor's NOVRAM transfers data from the RAM section to the EEPROM on assertion of the STORE signal. To prevent data loss, this signal must occur 10 ms before chip power is removed. Assertion of the RECALL signal when power is restored copies data back into the RAM.

16- x 16-bit serial version is available in an 8-pin package. Standard operating temperature ranges for the chips are 0 to 70 °C; industrial versions operate from −40 to 85 °C; military units operate from −55 to 125 °C. Typical power-supply currents are 35 to 40 mA (15 mA for the 16- x 16-bit version).

Although NOVRAM memory densities are considerably lower than those of EEPROMs, they are used in a variety of applications. For example, they can replace DIP switches on PC boards, thereby allowing reprogramming over a microprocessor data bus. A skilled technician is thus no longer needed to disassemble equipment when changing switch settings in order to adapt the equipment to a specific application. NOVRAMs can also be combined with D-A converters to serve as analog trimmers. Each of these examples illustrates that NOVRAMs eliminate potential reliability problems that mechanical components may be subject to in industrial environments, where vibration and contaminated atmospheres can adversely affect switches and potentiometers. In addition, the NOVRAMs can be easily tested by automatic test equipment, while testing DIP switches and trimmers adequately and economically can be quite difficult.

In general, NOVRAMs best suit applications that are well served by small amounts of memory, such as in the DIP switch and trimmer substitution examples. Using NOVRAMs when larger amounts of memory are required may, however, create a significant cost penalty—the NOVRAM cost/bit can be six times that of an EEPROM. Therefore, NOVRAMs are not economical for high memory and density applications unless an application requires fast data-capture rates that an EEPROM cannot achieve. For a further analysis, it might be helpful to examine EEPROM versus NOVRAM trade-offs, as well as NOVRAM operation.[4]

Bubbles furnish mass storage

Bubble-memory devices are ideal for industrial applications requiring read/write memory capacities larger than the amount that can be implemented conveniently and economically with standard RAMs or EEPROMs. These solid state units achieve the storage capacities available on disk and tape drives, but can also easily tolerate factory environments. Bubble memory technology is becoming increasingly popular, and although originally intended for harsh industrial environments, it is now used in point-of-sale terminals and portable personal computers.

Intel, for example, organized its Intel Magnetics subsidiary in 1977 to develop and market a family of bubble-memory subsystems. In demonstrating the suitability of bubble memory for industrial applications, the company points out that its bubble-memory products are used in machine-tool numerical controls manufactured by White-Sundstrand and Allen Bradley.[5] Bubble technology allows White-Sundstrand's DEC LSI-II based Micro softwired integrated numerical control (SWINC) to fit within the multi-axis machine it controls. Allen Bradley chose bubble memory as backup storage for its model 8200 computer numerical control's system RAM after also offering battery backed-up RAM and floppy disk drives.

Similarly, bubble memory has been used by International Paper Corp (Tuxedo Park, NY) in a batch makeup and application processor that facilitates raw material inventories. Before International Paper used bubble memory for this task, the heat, humidity, and vibration on the plant floor required that the processor be located away from the plant location so that such mass-storage systems as hard disks could be used.

Bubble prices are becoming more economical, as evidenced by Intel's 1979 introduction of a 1-Mbit bubble-memory kit costing $2500. As of the first quarter of 1984, 1-Mbit bubble-memory kits cost $149 in quantities of 10,000; by late 1984 they are expected to cost $99 in lots of 25,000.

Bubble memory devices consist of flat, thin, magnetic garnet wafers that are magnetically polarized in one direction. The bubbles are cylinders of reverse magnetic polarity distributed throughout the wafer (Fig 2). Driven by rotating magnetic fields generated by a pair of crossed wire-wound coils, these bubbles move along fixed storage loops and I/O tracks within the wafer. Data

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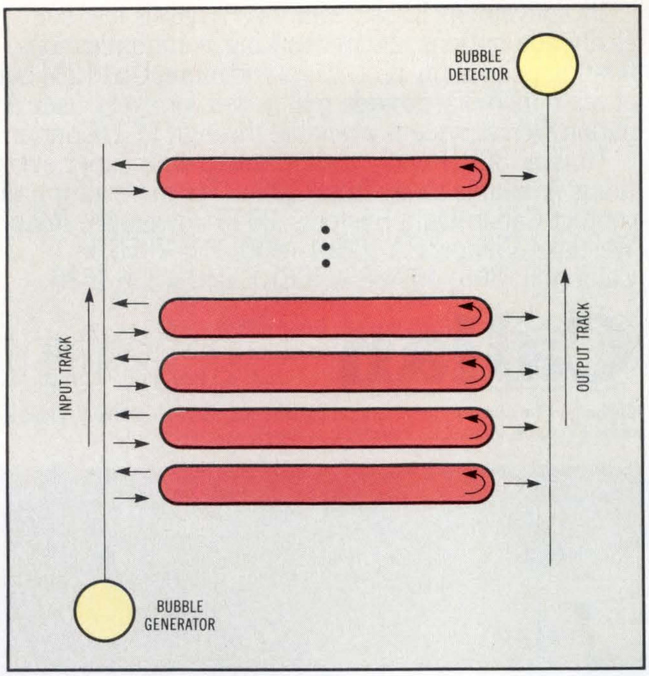

Fig 2 Bubble memories use a block-replicate architecture that stores data in a number of endless loops accessed by I/O tracks. Intel's model 7110 bubble-memory device includes 272 such loops to furnish a 1-Mbit storage capacity.

is stored in the device in the form of binary-coded, bubble or no-bubble sequences of 1s and 0s.

The serial movement of bubbles through the storage loops and I/O tracks slows bubble-memory access times compared to those of RAM and ROM devices.[6] It also makes access time depend on a particular bubble's location at access time. Nevertheless, at an average access time of 41 ms (the time required for a bubble to traverse half of its storage loop plus the output track), bubble devices are faster than many disk drives.

Bubble-memory fabrication is similar to silicon-wafer fabrication in that photolithography places conductor and magnetic patterns on the garnet wafer. Next, the crossed wirewound coils are installed, followed by a pair of permanent magnets and a sleeve of magnetic shielding material. The sleeve protects the bubble device from external magnetic fields, allowing it to operate near equipment that generates strong magnetic fields.

Among Intel's bubble-memory products are prototyping and production kits that use the company's 1-Mbit model 7110 bubble-memory device. In industrial applications, this device can replace 1000 ft of numerical control tape. The kits also include the support chips required by the 7110: a 7220-1 bubble-memory controller, which can control as many as eight 1-Mbit subsystems; a 7242 formatter/sense amplifier; a 7230 current pulse generator; a 7250 coil predriver; and two 7254 driver transistor assemblies (Fig 3). Prototype/production kits based on Intel's 4-Mbit model 7114 bubble memory are also available. The model iSBX 254 board is also available in 1-, 2-, and 4-Mbit versions. Two such boards can yield 1 Mbyte of storage. Intel's model iSBX 251 is a 128-Kbyte bubble-memory device that can plug into the firm's single-board computers.

Board-level products ease design

Although the memory products discussed so far give the designer flexibility, board-level products compatible with a standard microcomputer bus might be more convenient for many designs. Such boards are available in numerous configurations. One series of boards particularly suited to industrial applications includes Diversified Technology's (Ridgeland, Miss) static CMOS RAM boards, which are compatible with Intel's Multibus. Although 16-, 32-, 64-, 128-, and 256-Kbyte versions occupy a single Multibus card slot, a 512-Kbyte version takes two slots.

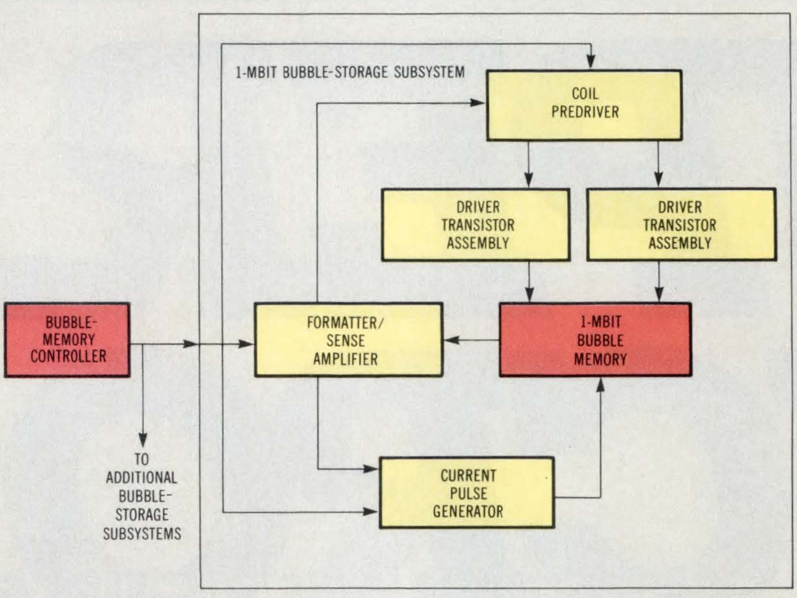

Fig 3 A 1-Mbit bubble-memory device requires six support chips: a bubble-memory controller that can support as many as eight 1-Mbit subsystems, a formatter/sense amplifier, a current pulse generator, a coil predriver, and two driver transistor assemblies.

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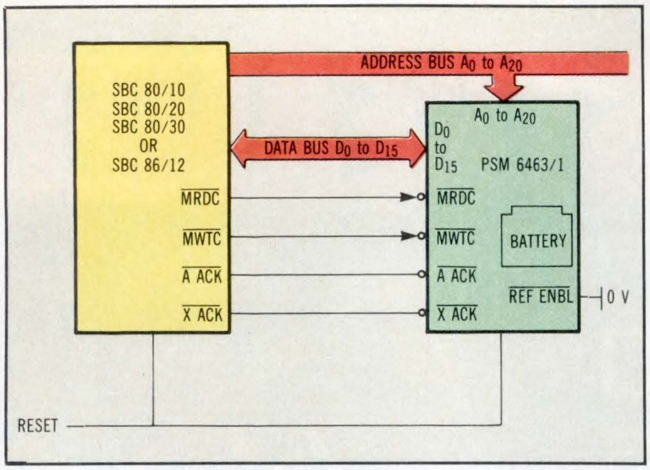

Fig 4 The Plessey Microsystems model PSM 6463/1, 64-K x 8-bit CMOS memory card includes onboard NiCd batteries to provide as much as 350 hours of standby operation and is compatible with Intel's Multibus. It readily interfaces to such single-board computers as the SBC 80/10, 80/20, or 80/30. When used with the SBC 86/12 16-bit computer, the PSM 6463/1 automatically configures itself as a 16-bit wide memory.

The company's CBC series of boards, with 16- to 256-Kbyte capacities, can interface with 8- or 16-bit microcomputers. Boards designed to plug into an all-CMOS bus dissipate from 75 to 100 mW maximum during normal operation. Versions designed to interface with TTL buses include TTL interface-logic circuits that increase board power dissipation from 20 to 26 mW.

The boards permit one of three battery-backup options. The first option is an onboard nickel cadmium rechargeable battery. This option is best used in systems that are typically shut down overnight or on weekends. However, this option is available only on commercial 0 to 70 °C temperature-range versions.

The second option is an onboard lithium battery that provides 3000 hours of data-retention time on a 64-Kbyte board. This option best suits applications where system power is applied continuously and where data retention is required only during temporary power failures. It is available on boards designed for industrial applications and that operate over a −30 to 85 °C temperature range. The third backup option involves an offboard battery.

Plessey Microsystems (Rockville, Md) also offers Multibus-compatible CMOS RAM boards that operate over a 0 to 55 °C temperature range with forced-air cooling. Its model PSM 6463 board is available in 16-, 32-, 48-, and 64-Kbyte versions and requires 1.5 A at 5 V (Fig 4). Onboard NiCd batteries provide as much as 350 hours of data-retention time.

One manufacturer offering Multibus-compatible memory boards (although not CMOS versions), is Monolithic Systems Corp (Englewood, Colo). The company's model MSC 4805, for example, provides from 128 to 512 Kbytes of RAM and supports either 8- or 16-bit data buses. Dissipation specifications are as much as 25 W per board. Built-in error detection and correction logic corrects any single-bit errors and detects any double-bit errors. Two onboard LEDs indicate correctable and uncorrectable errors, and the host processor can poll the board's error register to check for error conditions. Optionally, board jumpers can be installed to initial processor interrupts when single- or double-bit errors occur.

The MSC 4805 can be used with 20-bit addressing. ROM-coded, board-address selections that are programmed according to user specifications prevent the reliability problems associated with switch-selectable addresses. The model MSC 4808 also supports 24-bit addressing.

Plessey similarly offers Multibus-compatible memory boards with error checking. The 512-Kbyte model PSM 512A corrects single-bit errors and detects double-bit ones. In addition, the PSM 512P version features a byte-parity error management function that can interrupt the host processor on detection of a parity error.

Monolithic Systems also manufactures memory boards that are compatible with computer systems from Digital Equipment Corp. The model MSC 4806, for example, is compatible with DEC's LSI-11 based Q-bus and includes 256 Kbytes of RAM. The board features a control/status register that allows program control of onboard parity functions; diagnostic information is furnished via that register if a parity error occurs. Memory boards for the VAX- and PDP-11 based systems are also available from the company.

Other popular buses include Motorola's Versabus and Pro-Log's (Monterey, Calif) STD bus. Among the manufacturers that support the Versabus, Plessey offers a 1-Mbyte Versabus-compatible RAM board that permits 8-, 16-, and 32-bit data transfers. The board detects and corrects single-bit errors and generates an interrupt on double-bit error detection.

For STD bus applications, Pro-Log offers its model 7707. With 64-Kbit DRAMs, that card furnishes a 64- or 128-Kbyte capacity. It can work with 8- or 16-bit processors, including the Z80A, 8085A, 6809, and 8088. The board permits memory expansion to 384 Kbytes when used with 8-bit processors, and to 896 Kbytes when used with the 16-bit 8088. Moreover, a parity bit for each memory byte is used for error detection.

For low power STD bus applications, Pro-Log's model 77C08 furnishes as much as 64 Kbytes of memory (Fig 5). It accepts as many as eight 8-K x 8-bit CMOS RAM or EPROM chips in any combination. Unused board sockets can be disabled to prevent them from occupying system memory space.

Although solid state memory components and board-level products can offer the highest degrees of reliability in harsh environments, disk and tape

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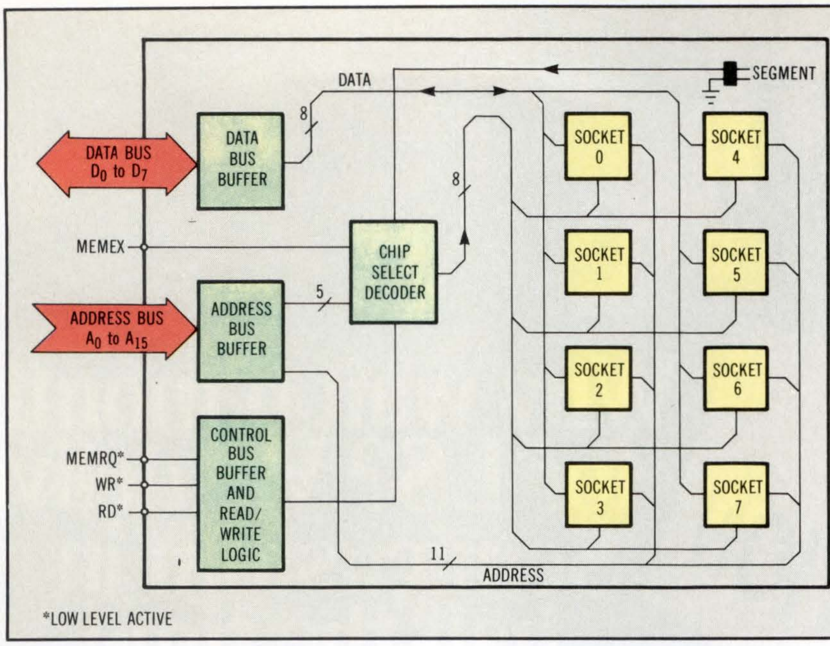

Fig 5 Pro-Log's STD bus-compatible model 77C08 provides as much as 64 Kbytes of storage and can accept as many as eight 8-K x 8-bit CMOS RAMs or EPROMS.

drives may also be suitable for many industrial applications. Indeed, they might prove to be the only suitable solution for some mass-storage requirements. Consider, for example, the Micropolis (Chatsworth, Calif) 5¼- and 8-in. Winchester disk drives. The 5¼-in. 1300 series models furnish 25.9-, 43.2-, 51.9-, and 83-Mbyte capacities; the 1400 series 8-in. versions provide 83- and 165.9-Mbyte ratings. As many as sixteen 8-in. units can be daisy chained to yield capacities to 2.65 Gbytes. The 8-in. drives are hardware and software compatible with the industry standard SMD interface. The 5¼-in. models feature ST506/412 compatibility.

Rotating memories can be rugged

To provide the reliability required in industrial environments, the Micropolis Winchester drives use a chassis-within-a-chassis design to isolate the head/disk assembly from shock and vibration. A balanced rotary voice-coil positioner further increases the drives' resistance to vibration-related failures during operation. To help customers decide if the drives are sufficiently rugged for their applications, Micropolis also publishes vibration specifications. For example, the drives can operate when subjected to vibration of 0.006-in. peak-to-peak amplitude in the 5- to 40-Hz range, and to 0.5 G peak acceleration from 40 to 300 Hz. Also during operation, the drives can tolerate 3 G accelerations for 5 ms and 1 G accelerations for 20 ms.

The suitability of Micropolis's drives for rugged usage is affirmed by Miltope (New York, NY), a manufacturer of ruggedized and militarized computer systems and peripherals. The company has recently purchased the rights to certain Micropolis severe-environment disk technologies for use in a classified disk-drive product line under development. Although specific details are unavailable, some of the technology involved in the sale derived from the development of the Micropolis 1300 series of 5¼-in. drives.

Other manufacturers offering rugged disk drives include Amcodyne (Longmont, Calif). That firm's Arapahoe 7110 features an SMD interface and a fixed/removable 50-Mbyte hard disk configuration. To prevent contamination from hostile environments, the unit includes a proprietary active hub seal around the spindle that protects the fixed disk when the removable disk cartridge is removed. The 7110 also includes a clean-air system with a recirculating filter that furnishes 20 times the air scrubbing capacity found on a typical Winchester drive. To further enhance reliability, the 7110, as well as Amcodyne's newer 160-Mbyte Comanche 8160, 8-in. rigid disk drive, includes a Whitney head suspension system that enhances disk life.

If an application requires Multibus compatibility, consider Monolithic System's model MSC 8411. It is suitable for 10- and 20-Mbyte applications, and accepts 10-Mbyte replaceable cartridge disks capable of purging themselves of contaminants, such as dust and smoke. For LSI-11 compatibility, Monolithic offers its MSC 8412 20-Mbyte removable-cartridge disk drive. Access times for this unit are 35 ms; start and stop times are 4 to 5 s. When used as a backup device, the MSC 8412 can store 10 Mbytes of data in approximately 30 s.

For STD bus applications, Pro-Log offers its model 702 STD Disk Pak. It contains two 8-in. double-sided, double-density floppy disk drives that provide a total of 3.2 Mbytes of unformatted storage. In addition, the package includes a 13-slot STD bus card rack (with ⅝-in. center-to-center card spacing), a four-voltage switching power supply, and a fan. It thus helps users avoid time-consuming package design tasks. As a system-oriented product, the model 702 illustrates a new trend in Pro-Log's support of its STD bus. Before the model 702, the company's STD bus line only included board-level products and accessories.

If compact data storage is needed, consider such products as Teac's (Montebello, Calif) model FD-30A, a 3-in. floppy disk drive that is plug compatible with industry standard 5¼-in. drives. The FD-30A features a 250-Kbyte capacity and is functionally equivalent to Teac's 5¼-in. models FD-50A and FD-55A. It has 40 tracks at a 100-track/in. track density and consumes only 3 W of power, compared to 4.9 W for FD-55A models. As many as four FD-30As can be daisy chained.

In addition to its disk drives, Teac also offers a line of tape transports, another alternative for mass storage. Two-track models in the firm's MT-2 digital cassette transport line achieve 760 Kbytes of formatted storage capacity (using 300-ft, CT-300 cassettes) and 24,000-bit/s data-transfer rates. Recording density equals 1600 bits/in.; tape speed is 15 in./s during data and read/write operations and 45 in./s during operation of the units' fast search (fast forward) function. Rewind speed is 75 in./s. A two-track head allows recording on both sides without the need to turn over the cassette. With the addition of a DMA controller, one model in the line supports DMA data transfers, allowing overlap of data transfers and other CPU operations. The units measure 120 x 105 x 91 mm and weigh 1.2 kg. They operate on 12 Vdc at 1.8 A maximum, 1 A average, and 5 V at 0.4 A maximum.

Among other manufacturers of tape drives, Quantex (Hauppauge, NY) offers a line of tape storage systems designed to meet the requirements of military and severe-environment applications. Its model 5100 is available with one or two tape drives and a formatter for 8-bit parallel interfacing. Options include RS-232 as well as ROLM, PDP-11, LSI-11, and Nova/Eclipse compatible interfaces.

Model 5100's RS-232 interface, located on a single PC board, allows data transfers at switch-selectable rates from 50 to 19,200 baud. A double buffer allows asynchronous writing of data blocks as large as 1 Kbyte and reading of blocks as large as 2 Kbytes. Parity, stop-bit, and word-length options are switch selectable. Tape speed equals 30 in./s during write and bidirectional read operations, and 90 in./s during rewind and high speed search. Recording density is 1600 bits/in., and the data-transfer rate is 48 kbits/s. Moreover, data capacities extend to 4.32 Mbytes.

Although far from being an inclusive list of memory products suitable for industrial applications, the products discussed illustrate the range of options available to designers who need to select memory components and systems that must operate in harsh environments. Indeed, memory products are rapidly evolving to keep pace with the data storage requirements caused by the migration of sophisticated computer systems to the factory floor. Therefore, as designers juggle functional requirements on the one hand and environmental restrictions on the other, they are likely to find a variety of memory devices and assemblies that suit their applications' requirements, whether they are for component-, board-, or system-level products.

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ROM	•		•							•	•	•	•	•
PROM				•	•		•	•	•					
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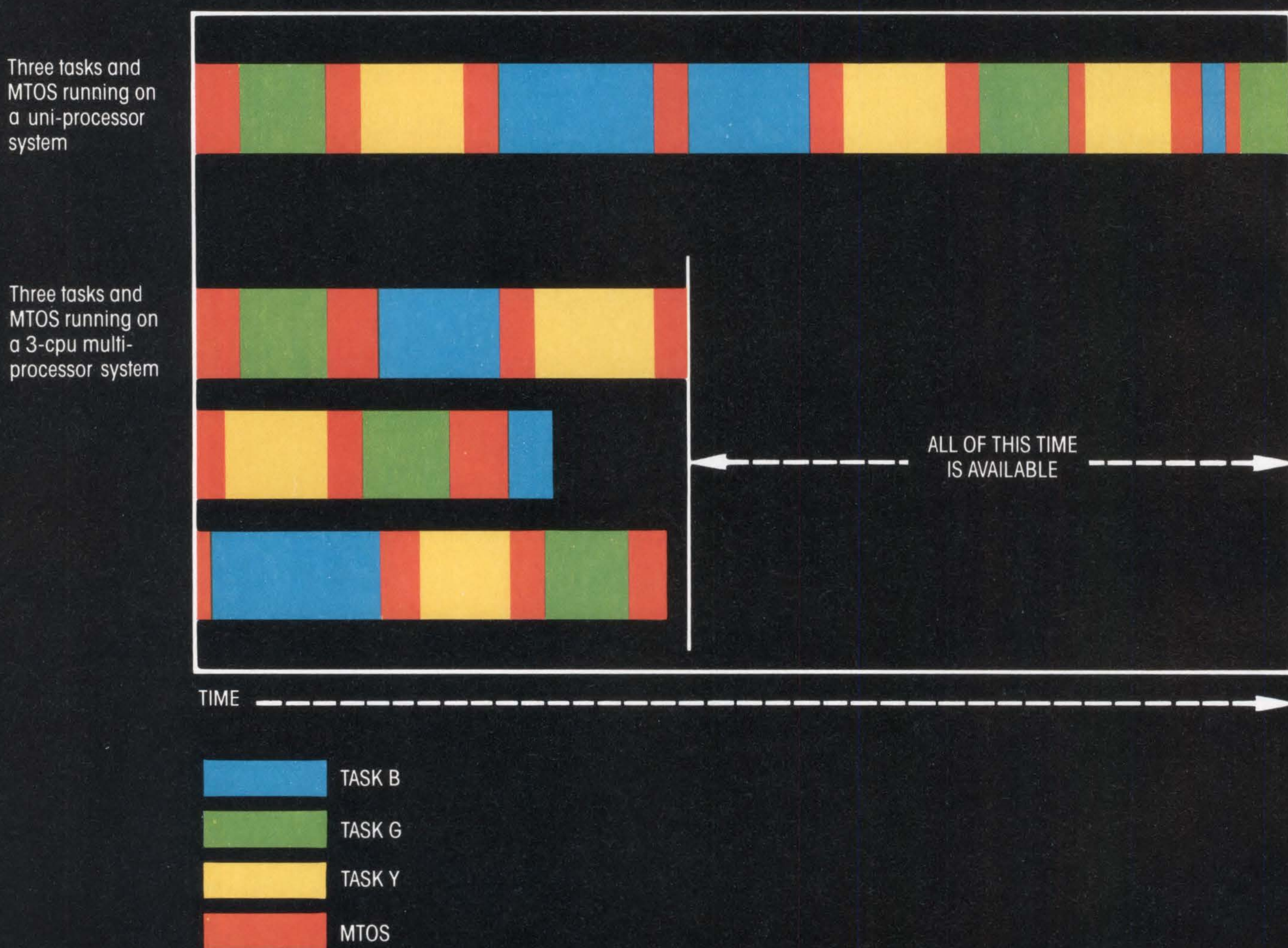

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CIRCLE 88

OPERATING SYSTEMS ADAPT TO HANDLE DATABASE APPLICATIONS

Traditional operating systems, conceived as programming environments, can cause performance barriers. For a certain set of business applications, a functional reorganization can leap those hurdles.

by Lowell W. Dunn

As the microcomputer becomes a more dominant force in the computer industry, it is necessary to reevaluate the direction it is taking. Now, for example, one strong application area for the microcomputer emerges from the small business world. Beyond basic accounting packages, there is a call for application software coming from such vertical markets as the medical, legal, insurance, and real estate fields.

However, with this tremendous potential come some real problems for the microcomputer manufacturer. One of the foremost problems is the need to expand the microcomputer into the multi-user office without an excessive cost increase. Burdened by relatively slow hardware and inefficient operating systems, the realistic user limit to concurrent multiuser operations is two or three, with many systems still limited to a single user.

The microcomputer industry faces a very basic problem—how to achieve high performance application systems based on limited capability hardware. The introduction of the 16-bit microcomputer promises a partial solution, but in the final analysis, all the factors causing performance degradation in 8-bit machines still exist in operating systems for 16-bit microcomputers. The operating system's ability to achieve acceptable response to each user thus limits the number of concurrent users.

The heart of the problem is a conflict between application environment goals and operating system design. A quick look at the traditional uses of operating systems reveals the source of the conflict.

Traditional microcomputer operating systems were created to aid program development and consist primarily of two functions: an executive and a file manager. The executive manages task processing. It organizes and sets priorities for all tasks currently running on the system while the file manager organizes data on mass-storage devices. Most tasks on the system are high level language application programs designed to handle the data for a particular application.

The database manager and the database dictionary, functioning as a central point of interface, are relatively new expansions of the microcomputer operating environment. Within this structure, software talks to the database manager, and the database manager talks to the operating system. This eliminates a variety of application programs interfacing separately with the operating system, and results in a much "cleaner" data structure. However, the system now consists of three operation levels: the operating system, the database manager/database dictionary, and the application environment. This kind of structure impedes system operation in three ways: the slowdown caused by high level language, complications in file management, and the burden placed on available memory resources.

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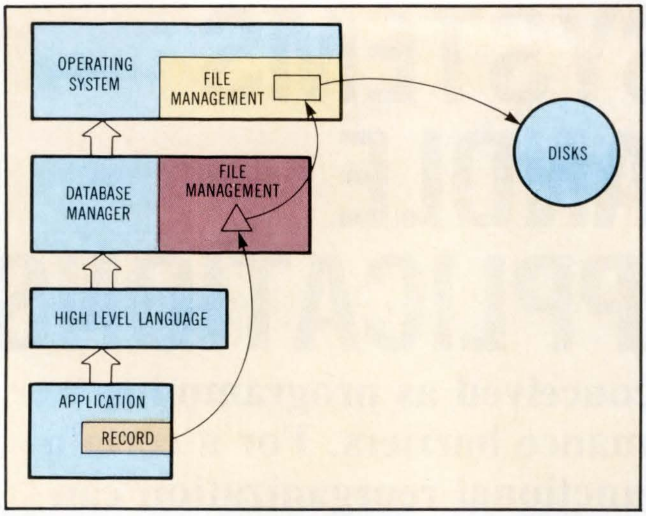


Fig 1 Using typical file handling methods, a request from the application must go through three levels, each with its own concept for representing data, before it finally gets to the information on the disk.

Most application programs today are written in a high level language such as Basic, Cobol, or Pascal. A high level language will generally slow down software execution by approximately 2:1. Various implementations of Cobol, Basic, and Pascal, depending on whether they are compiled or interpretive, could reduce performance by a factor of up to 20.

Additional database management problems

Recently introduced program generators are an aid to the programmer in generating many standard code sequences. These, however, are only designed to make the programmer's task easier and do not deal with overall system organization.

The multilevel handshaking of the operating system/database manager/application program architecture also causes some loss of performance. The operating system imposes a certain logical image on the mass-storage device and generalizes data into as many as five different methods of data representation (ie, file structures).

In addition, the database manager organizes the mass-storage device into its own logical representation. Database managers tend to be very sophisticated file managers specializing in random record access. Besides defining file structures, they also define data interrelationships. Thus, the database manager has its own logical image of the storage device that must be mapped to fit the operating system image of the disk. The final result is the constant mapping of storage device file images, as illustrated in Fig 1.

Having three to four interaction levels between the application software and the actual data storage device can cause minor to severe performance degradation. This degradation is the cost of mapping between the actual data organization on the disk and the application program via several intermediary steps.

Most application systems require a great deal of memory for operation. For example, a high level language/database manager interface package can use 20 to 30 Kbytes of memory. DBMSs supporting features such as query packages can require even more memory. In addition, the standard organization of application programs requires a separate copy of the application operation work space for each user. This amounts to an absolute minimum of 48 Kbytes of main memory per user. For this reason, most systems require memory configurations of 128 Kbytes or more in order to service more than one user on the system. To make the most of memory, available programs are typically overlaid and/or chained, resulting in a further performance penalty due to bustling mass-storage access activity.

Each of these factors (high level languages, file management, and memory overload) contribute to the low performance levels that are common among microcomputer systems. Degradation is most evident in multi-user systems, typically limited to both in speed of servicing each user and, particularly, in the number of users that can be supported. On the other hand, the application environment required for widespread business applications must emphasize fast data input/retrieval and task management. DBMSs were developed to adapt the operating system environment to this type of application, but in doing so they introduced new problems.

Optimizing microcomputer performance to meet application environment needs requires some reevaluation of the handling of certain operating system functions. The application environment is primarily an I/O handling environment rather than a program development environment. It must thus emphasize efficiency in moving data rapidly through application functions, the operating system, and mass storage handling routines, and an optimum distribution of functions between the database manager and operating system. It must also pay attention to proper interrupt handling as well as the setting of priorities.

A very flexible system architecture is required to control all these functions in the most efficient manner. Flexibility, however, is not a part of the traditional system architecture, where the operating system and application system are two separate entities. For this reason, a special organization of system functions is required for the microcomputer application environment.

Smoothing the road to better performance

In designing a high performance application-oriented system independent of existing operating systems, four functions of the system operation must be carefully examined. These include architecture, executive efficiency, disk buffering, and control of the database manager.

In order to obtain maximum performance in an application environment, it is necessary to have control over functions throughout the system structure. Traditionally, trade-offs have been made between what the task performs, what the executive performs, and what the database manager performs. Within an existing operating system, programmers often find the need to "get around" the operating system or to include functions in applications that would be better executed by the operating system. This complicates the application architecture, and often proves to be a bottleneck in system performance.

As for the executive, two functions are critical to maintaining efficiency in an application environment: interrupt handling of output to CRTs/printers and task/buffer management. These functions are especially critical for those microcomputers lacking DMA data transfer to the terminal and printer drivers. Each time the executive handles scheduling or an I/O request, time that the CPU could have used for actual processing is lost. Most Z80 operating systems overuse the executive by interrupting it for each character printed or displayed on the CRT, causing much performance degradation.

Systems that deal primarily with sequential file structures need to process large data blocks serially from the disk device. Database applications, however, more frequently make random accesses to the disk and process small blocks (records) of data.

Thus, the greatest benefit for a system geared to random access mode is the ability to buffer the disk so that data read from the disk is kept in memory as long as possible on the chance that it will soon be accessed again. The likelihood of reaccess is greatest when data records are being created and changed because data is often broken into accounts or other logical groups for operating entry. In terms of performance, the value of disk buffering depends greatly on the number of records that can be retained in memory.

In handling the creation and filing of data records and their location and retrieval, the database manager often makes functional trade-offs that can greatly influence system performance. This depends on whether a function is assigned to the database manager or to an application code. For example, from a multi-user point of view, it is undesirable to have the database manager perform lengthy functions because other users tend to be blocked from the system until that specific procedure is completed.

Of the three standard types of database structures (hierarchical, network, and relational), the relational is the easiest to deal with from the user's point of view. However, the network database structure is the fastest in performance. (The hierarchical is a subset of network.)

A node structure that is expandable in any direction characterizes the network structure. The network structure has direct relation-oriented data, a capacity for handling complex structures, and high performance. In this structure, any record in the system can, if desired, own any other record or list in the system. This type of data base is illustrated in Fig 2. Relying on directories for data location, network structures provide very rapid location of nodes within the system. However, such structures are usually complex and tend to be difficult to use from the end-user point of view.

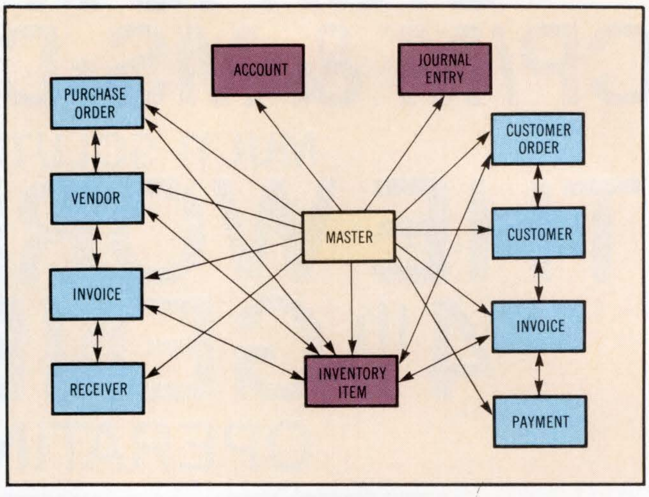


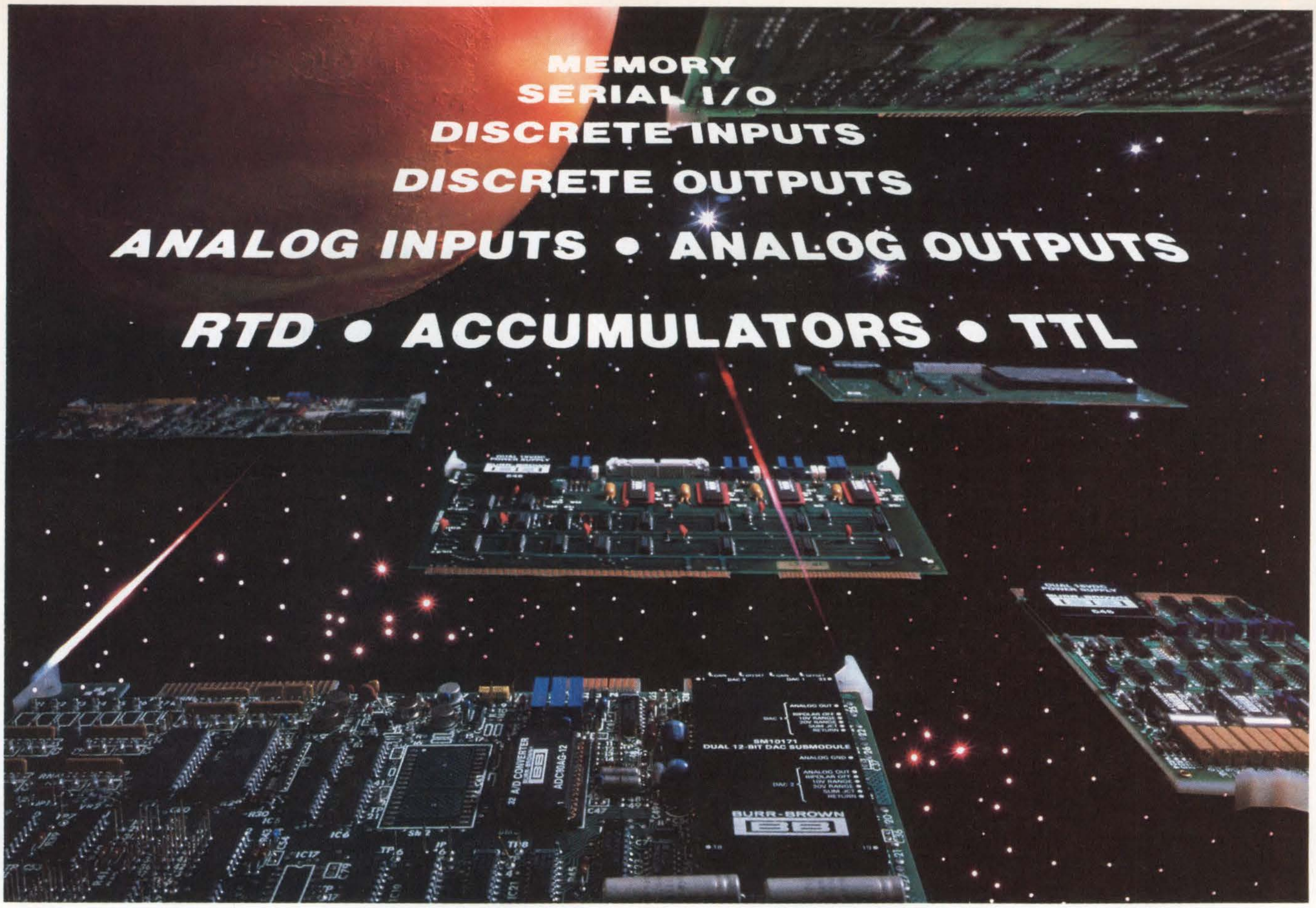
Fig 2 In a network data base, any node or record in the system can be directly related to any other node, as desired for the application.

The relational structure is characterized by the table data structure, data independence, and easy use. Data is accessed by name rather than location and is ordered by value, not by file sequence. Tables are related by fields within the table, not by pointers. The relational structure's popularity over the network structure is no doubt based on its user friendliness, rather than its performance.

A unique solution

The end result of this evaluation takes concrete form in Business Express, an application system developed by Systems Group and American Computing Enterprises, Inc (Orange, Calif). Up to now, the consensus was that operating systems were built for programmers and optimized for program development. What was needed for the small business environment, however, was an operating system optimized for application environments and aimed at dealers and system houses. The resultant system design represents a rather different approach to system control functions. The structure and design concepts applied to Business Express are methods of implementing solutions to the problems that have traditionally plagued application software products.

Business Express's internal structure was specifically designed to maximize system performance in a multi-user environment. It is an application system designed as a self-contained package, independent



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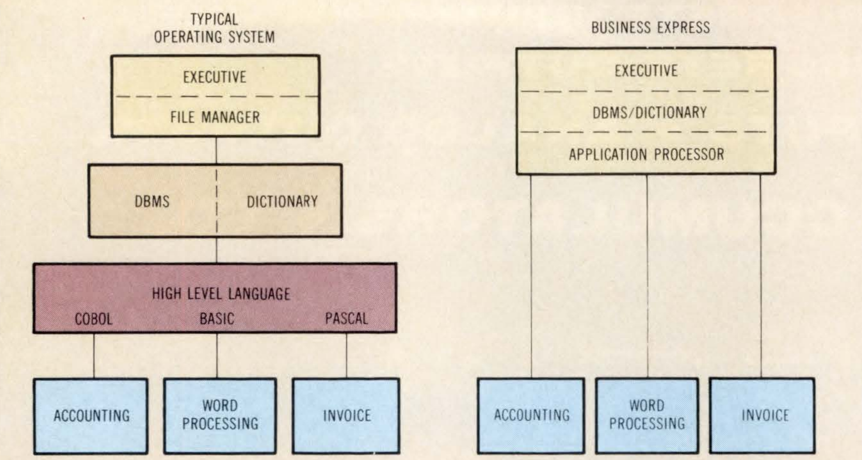

Fig 3 In this illustration of traditional operating system structure versus Business Express, the integrating executive, DBMS, and application processor increase performance. Eliminating high level languages reduces some flexibility, however.

of any other operating system. Moreover, it offers the end user a simple-to-use system that is easily customized to the specific needs of the user's application.

In light of the problems inherent in existing operating systems, the system is designed to be operating system independent and dedicated solely to application development and operation. Business Express creates a virtual image of how the hardware should process data. For performance and efficiency, the entire system is written in Z80 assembly language, including the application processing logic.

As shown in Fig 3, the system has three parts: the executive, the database manager, and the application processor. Because Business Express is designed as a complete standalone unit, many performance trade-offs are made among the executive, the database manager, and the application processor. During development, for example, the word processor designer asked for special features from the executive. In order to implement these features and still maintain performance, certain functions had to be traded for the database manager. There were also several cases where performance was tuned by removing a function from the database manager, and placing it in the application processor.

Business Express's executive is a simple multitasking executive optimized to process interrupts and schedule tasks. Because Business Express must support as many terminals as possible without becoming I/O bound, interrupt processing is a very critical control point. Although constraints come from the actual processor speed, interrupt performance is optimized by reducing both the amount of software required to process the interrupt, and the frequency of interrupt requests. Tasks request processing from the executive with a string or a line, rather than a character, to be transferred. Then the task remains idle while the interrupt response code, which is short and fast, is executed.

Because the data interrelationships in the data base are of prime importance, the network type of database manager is used for internal operations. The network accommodates many things that cannot be accomplished with relational database structure. Among the features of Business Express that could be included because of network architecture are "list fields" and "forms-within-a-form." In addition, the network database manager offers a high performance level and increased flexibility.

However, the network structure cannot handle certain indirect relationships. These indirect relationships specify how one piece of data affects another piece of data. As a result, the system accommodates a special relational field used to store the relationship between two pieces of data. For example, a relational field could specify how many parts have been ordered from a specific supplier or, as shown in Fig 4, how many parts are used in a specific finished product. In an application environment, these types of indirect relationships can often be very important. Thus, the system's database manager is actually a hybrid of the network and relational database structures.

The database manager, which interfaces directly with the disk, performs the file management functions. In this way, the database manager is free to make its own logical image of the disk without an intermediary file manager to complicate disk interface. The database manager in Business Express is optimized for locating data quickly and a rapid reading of data from the data base.

To achieve the kind of flexibility required to meet the design objectives, the unit's database manager was designed to support dynamically variable record size. Individual fields within existing records in the data base can be changed, thus altering the record size. Even the record definitions themselves can be established or modified after the system is in use and data is entered. This is contrary to most systems that require all record definitions to be established before any data can be entered into the data base. Many data bases can accommodate some changes by

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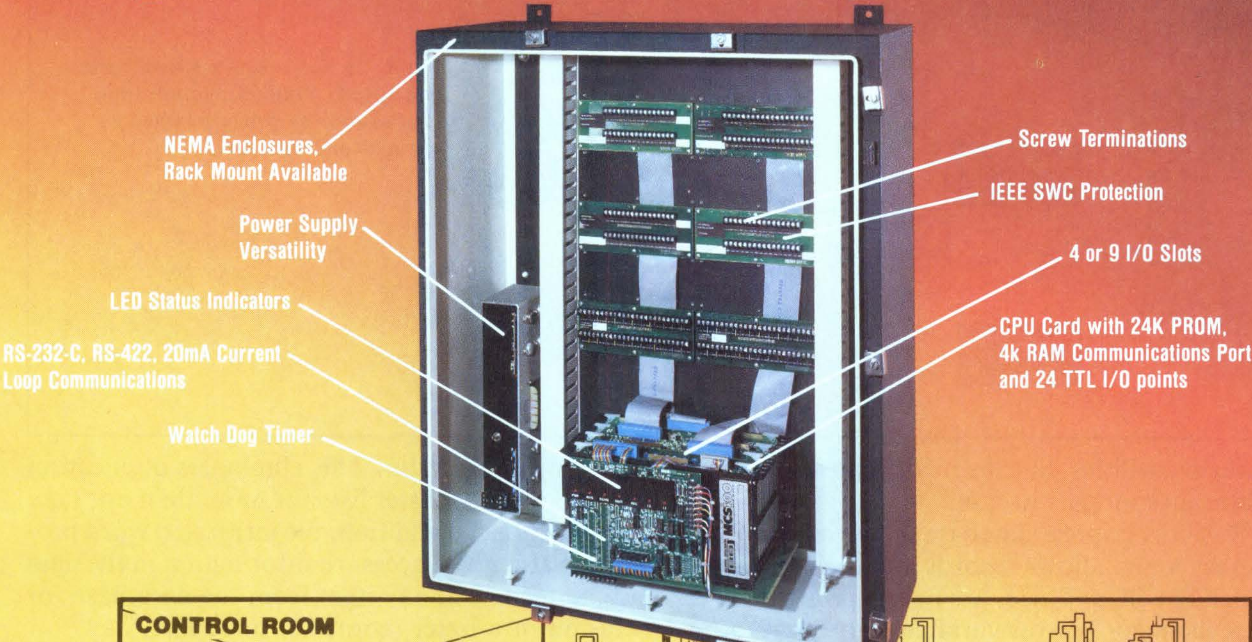

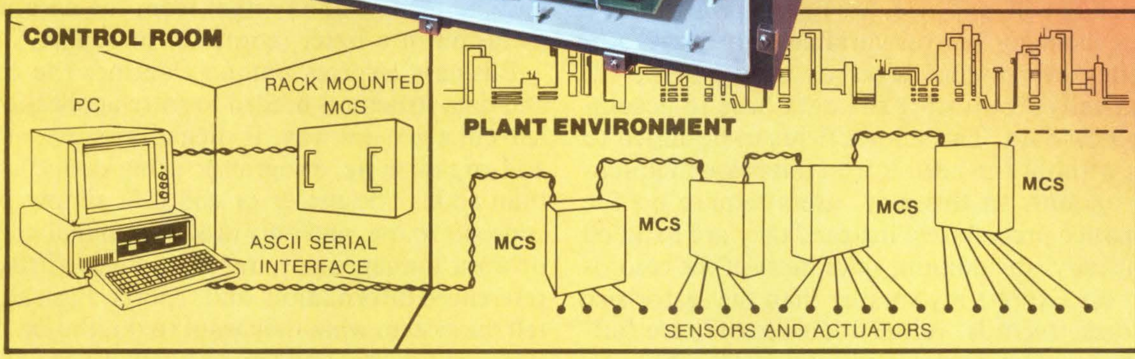

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CIRCLE 91

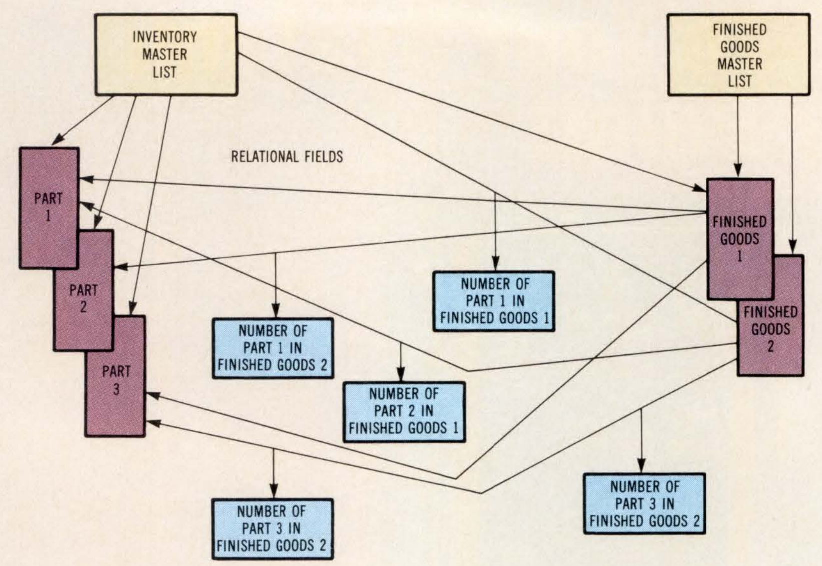

Fig 4 In the relational field, users can specify indirect relationships that cannot be solely handled by the network structure.

restructuring utilities, but the inconvenience of this procedure discourages its use.

The Business Express database manager, through proprietary logic, allows records and their fields to be defined at will, and sizes are never specified. The database manager accepts variable record sizes and establishes new record sizes as data is entered, automatically readjusting the data base to accommodate new data. This allows fields to be added to records without the need to run database maintenance programs. In this way, users require no file maintenance procedures; instead, they are handled automatically. In addition, since most of the records in Business Express are smaller than the sector size of the disk, records, rather than sectors, are buffered. Thus, users need not advance guess every possible field or record format that may be required.

The application processor is the largest code segment in the system. It contains the logic to build the database structure (the define command), the logic to process the data base (the access and report commands), and the word processor. The application environment is responsible for all the overhead and brainwork that keep track of the relationships between the various lists and records. At the heart of the application processor is the database dictionary and the data structure map.

Like the executive and the database manager, the application processor is highly structured; it is essentially a table processor. When the system analyst defines an application, the application processor sets up tables that define relationships among various data groups. The table processor interfaces with the database manager, database dictionary, and the data structure map to translate user needs directly into data structures and formats.

Because all applications are coresident in the application processor, all data in the data base is accessible by any application. This eliminates duplication of such items as master lists for more than one type of application. In addition, the integrated word processor is also given access to information in the data base, and can call any item from the data base for inclusion in a letter, contract, or report.

Business Express uniquely defines the concepts and data structures needed to solve application problems in a general way. It then allows users to select and organize (ie, program), using concepts rather than code. The dealer or end user simply puts the concepts to use, and only needs a minimal knowledge of data management, records, fields, lists, cross-referenced information, and reports. Basically, users tell the system what they want to do, the list of items they want to use, and any resultant reports that need to be generated. Through a question and answer dialogue, the system collects the desired operation parameters and data sources to be used in the application task.

Redefining the application process

The application processor also handles record coordination and lockout. Many users can access a data record, but only one user at a time can make changes. When the first user modifying the record completes entry, the updated version of the record immediately appears on the screens of any users waiting to make changes. The processor also prevents lockout—ie, users sometimes make extensive data entries only to find themselves locked out. The first keystroke informs users that the record is locked.

As discussed, it is in the application processor that Business Express takes form for the user. In order to make the system as user friendly as possible, a relational format exists in the application environment. Therefore, the system's external interface is designed to give the user a simple structure, while the internal architecture is more complex and performance oriented.

To avoid using up vast amounts of memory, programs resident in memory are accessible to all users on the system.

While data errors on a disk with contiguous record files only cause data loss where the error occurred, data errors on a disk with structured data can ruin the integrity of the entire disk. To prevent such data vulnerability to hardware and software errors in the data base, two types of backup were designed. One provision backs up the entire data base, and the other automatically stores raw input data into its own data area or backup device. If necessary, this data can be used to reconstruct the data base, much like using a card reader.

For performance and efficient memory management, all of the unit's software is continuously resident in memory without the use of overlays, and all applications are resident reentrant code. The application processor contains the application processing functions, list and form processors, cross-referencing logic, the report generator, and the word processor. This means that Business Express uses considerably more memory than that required for the standard operating system, in which many of these operations are part of the application program. To avoid using up vast amounts of memory, programs resident in memory are accessible to all users on the system (reentrant). This eliminates the need to maintain a separate program copy for each concurrent user. Because the system has defined all the data management and manipulation functions, including word processing, there are no memory requirements for users other than a small work space, (8 Kbytes for individual users). This is a drastic reduction from the 48 Kbytes required under standard application systems.

Although Business Express and standard operating systems have common attributes, there are significant differences. As its own operating system, Business Express must be ported to each type of computer system.

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CIRCLE 92

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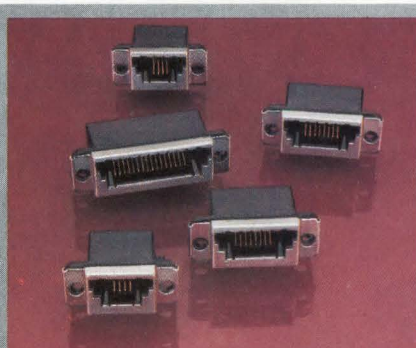

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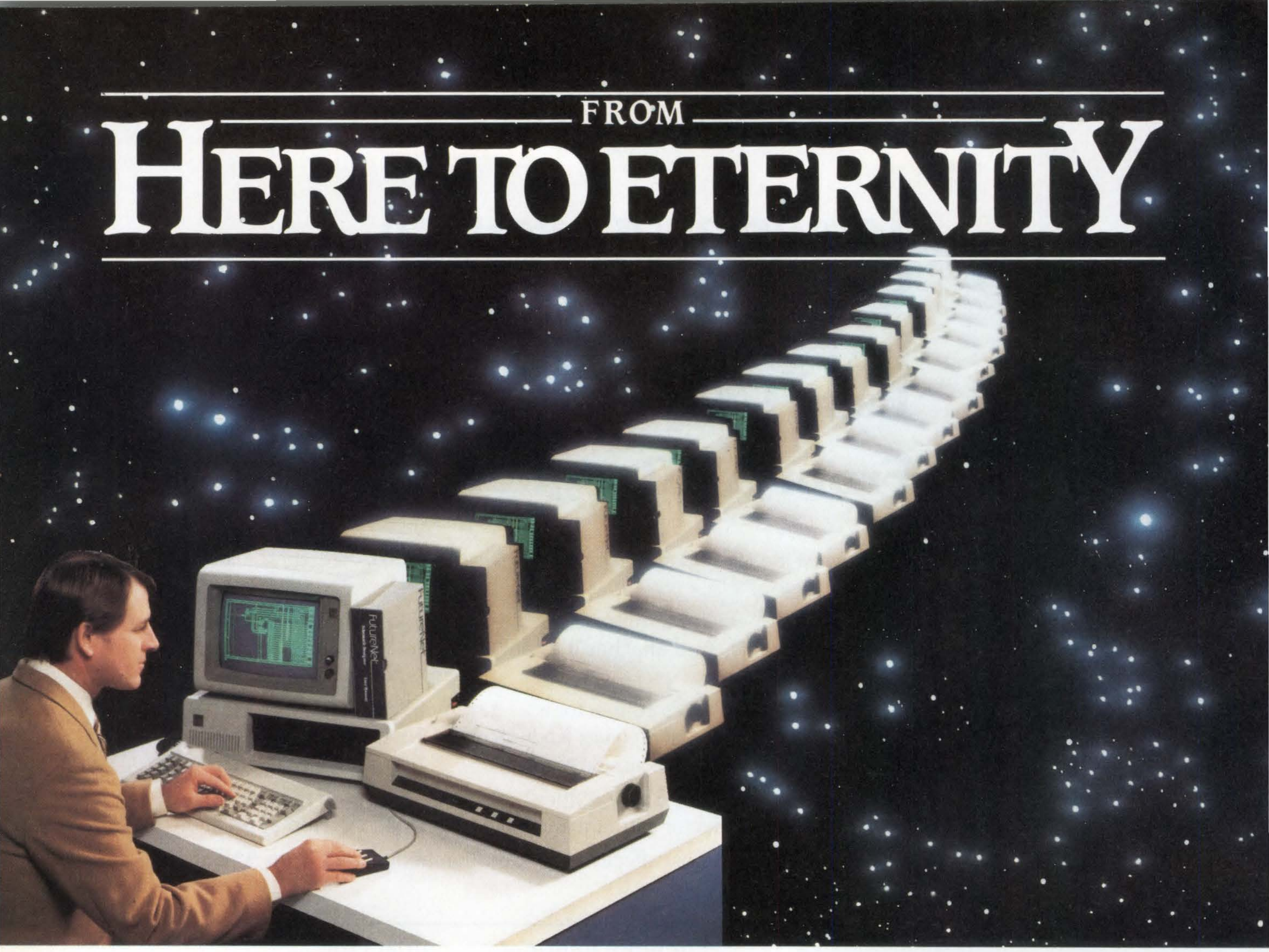

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CIRCLE 94

INTEGRATED DBMS KEY TO CAE PRODUCTIVITY

Integrating a hierarchical DBMS into a computer aided engineering workstation relieves the designer of much routine work, permitting modular design and automatic updating of all levels.

by Donald M. Laughlin

A major problem with conventional computer aided engineering systems is the lack of sophisticated database management. Most computer aided design systems are really computer aided drafting tools. The DBMSs in these configurations allow schematic capture, but provide few facilities for building a flexible, hierarchical design methodology.

For example, in designing a counter timer circuit, an engineer builds a model of the counter by using standard AND, OR, and inverter gates from the computer aided engineering (CAE) workstation library. After the design is verified at the logic gate level, the engineer may want to optimize the resulting transistor circuit in order to reduce the number of components. Such a reduction may be necessary to meet space requirements on the chip or board in which the circuit will be used.

Most CAE workstations' DBMSs cannot maintain more than one representation of the same circuit function. Thus, a designer cannot refine the design and keep subsequent representations in the same data base. Moreover, CAE workstations of the present generation do not have any way to switch between a logic gate level representation and a transistor level representation of the same circuit. Having such a feature would allow design and simulation at the functional, logic gate, and transistor circuit level, as well as switching between the different representations while the design is refined.

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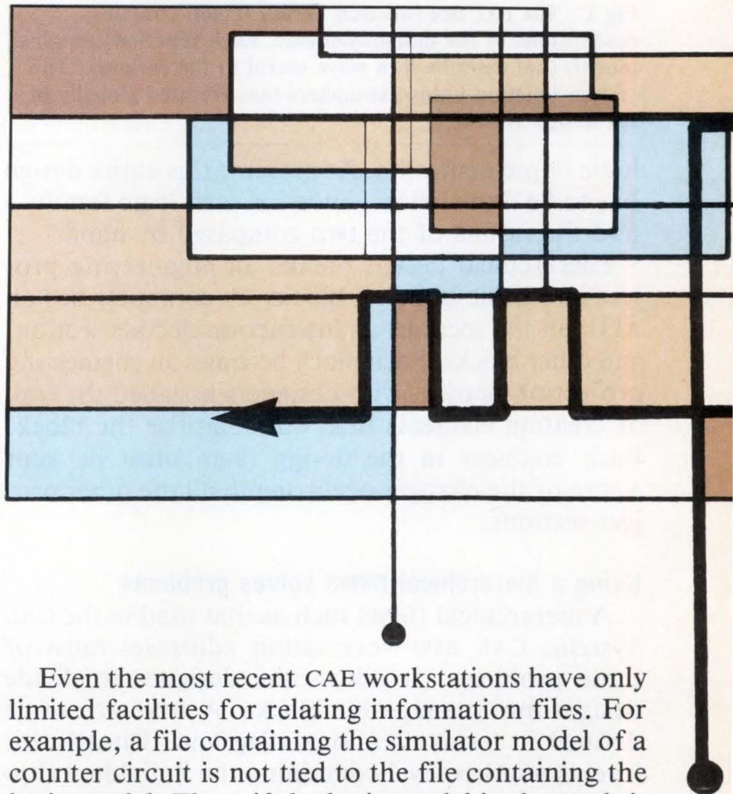

Even the most recent CAE workstations have only limited facilities for relating information files. For example, a file containing the simulator model of a counter circuit is not tied to the file containing the logic model. Thus, if the logic model is changed, it is not automatically updated in the simulator model. The burden of updating all design documentation still remains with the engineer. In addition, most CAE systems' DBMSs are geared to handle one or two design tools, such as simulators. Handling more tools requires software revision.

Another useful feature in a CAE system would be the updating of a change throughout a design to permit fast "what if" analysis of an entire project. For example, it might be desirable for a logic designer constructing a counter to see the effects of using the circuit in series 74 TTL logic, as compared with the cost and performance of a series 74LS TTL

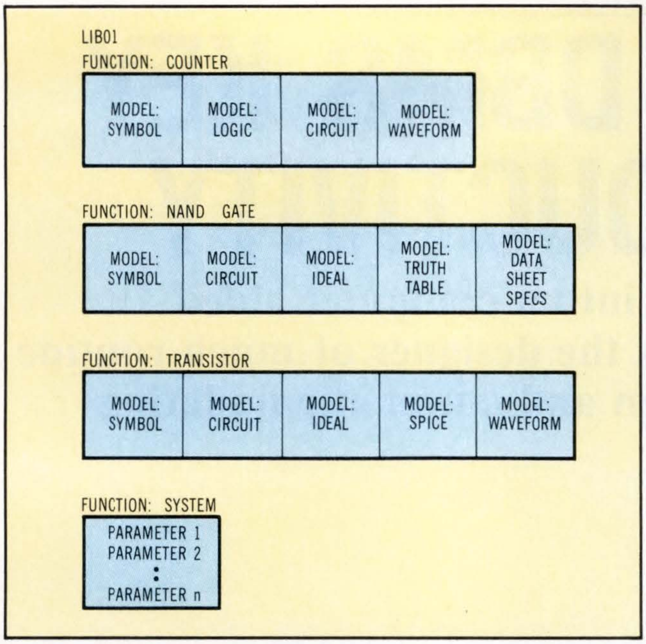

Fig 1 The CAE 2000 function library (LIB01) contains descriptions of the design elements. Each function contains models that describe it in ways useful to the designer. The system function holds parameters that are used globally in the design system.

logic implementation. At present, this entire design has to be done twice—once for each logic family—and the results of the two compared by hand.

Hierarchical design breaks an engineering project into basic building blocks. A computer has an ALU, an I/O section, an instruction decode section, and other blocks. Each block becomes an engineering project of its own, with designers assigned the task of creating elements that will comprise the block. Each engineer in the design team must be kept aware of the changes occurring in all the other project sections.

Using a hierarchical DBMS solves problems

A hierarchical DBMS such as that used in the CAE Systems CAE 2000 workstation addresses most of these problems. It allows the designer to divide designs into manageable blocks. A counter can be defined in terms of a logic diagram. Beneath this level is another level containing the individual flipflops, gates, and inverters used in building the counter. Below this is yet another level containing the transistors used to construct these flipflops, gates, and inverters.

Using the hierarchical approach to design a counter illustrates how the data base actually handles the various levels. This approach also shows how conventional computer aided design (CAD) system problems are easily solved by the DBMS found on the CAE 2000.

In the data base, a collection of information is called a file. The file name consists of the following: library/function.model (revision no.). Library designates a collection of logical functions. A designer typically has access to one or more design libraries, each of which contains a complete design or portions of one. A function can be any element in a design, from something as complex as a computer to something as simple as a basic transistor. As shown in Fig 1, the functions contained in the library include a counter, NAND gate, and a transistor. Inside each function reside several blocks containing models of the function.

For example, the NAND gate function has five models. Besides symbol and circuit, there is also a truth table model of the gate, as well as a set of data sheet specifications for the gate. Finally, there is also an Ideal simulator description of the gate. The Ideal simulator (used on the CAE 2000) simulates logic gates, flipflops, and transistors. The designer can choose to simulate at the higher logic level, or the lower transistor circuit level. The transistor function also contains a Spice simulator model of the circuit. Other simulator models could also be linked to the transistor models, and logic gate simulators could be linked to the logic gate models.

Relationships in the data base

Thus far, the only relationships described have been the links between models within a function. These links are particularly useful each time the design is simulated prior to final implementation. Besides the links within each function, relationships exist between functions. To illustrate how functions are related, again consider the evolution of a design using the hierarchical design approach.

The counter design might begin with the engineer specifying a functional description of a single counter cell [Fig 2(a)]. At the next higher level in the design hierarchy, the designer makes the desired-length counter by stringing lower level counter cells together. After the functional description is entered into the data base, the engineer expands the design by creating a logic diagram model [Fig 2(b)].

The logic diagram is a collection of descriptions of standard AND, NAND, NOR gates, and inverters. To use these standard gates, the designer establishes an "instance" of the logic gate in the counter cell logic representation. In Fig 3, the instance of the lower level gates in the counter logic diagram is shown by the lines running from the symbol models of the gates to the counter logic model.

Once the designer creates the logic representation of the counter cell, the simulation of cell operation forms the next step. To do so, the design must be submitted to a tool like the Ideal simulator. The CAE 2000 uses two commands—generate and evaluate—to extract the design from the data base and prepare the input file for a particular simulator.

The generate command creates a network description of a model, along with its input and output stimuli. The description is placed in a net list file,

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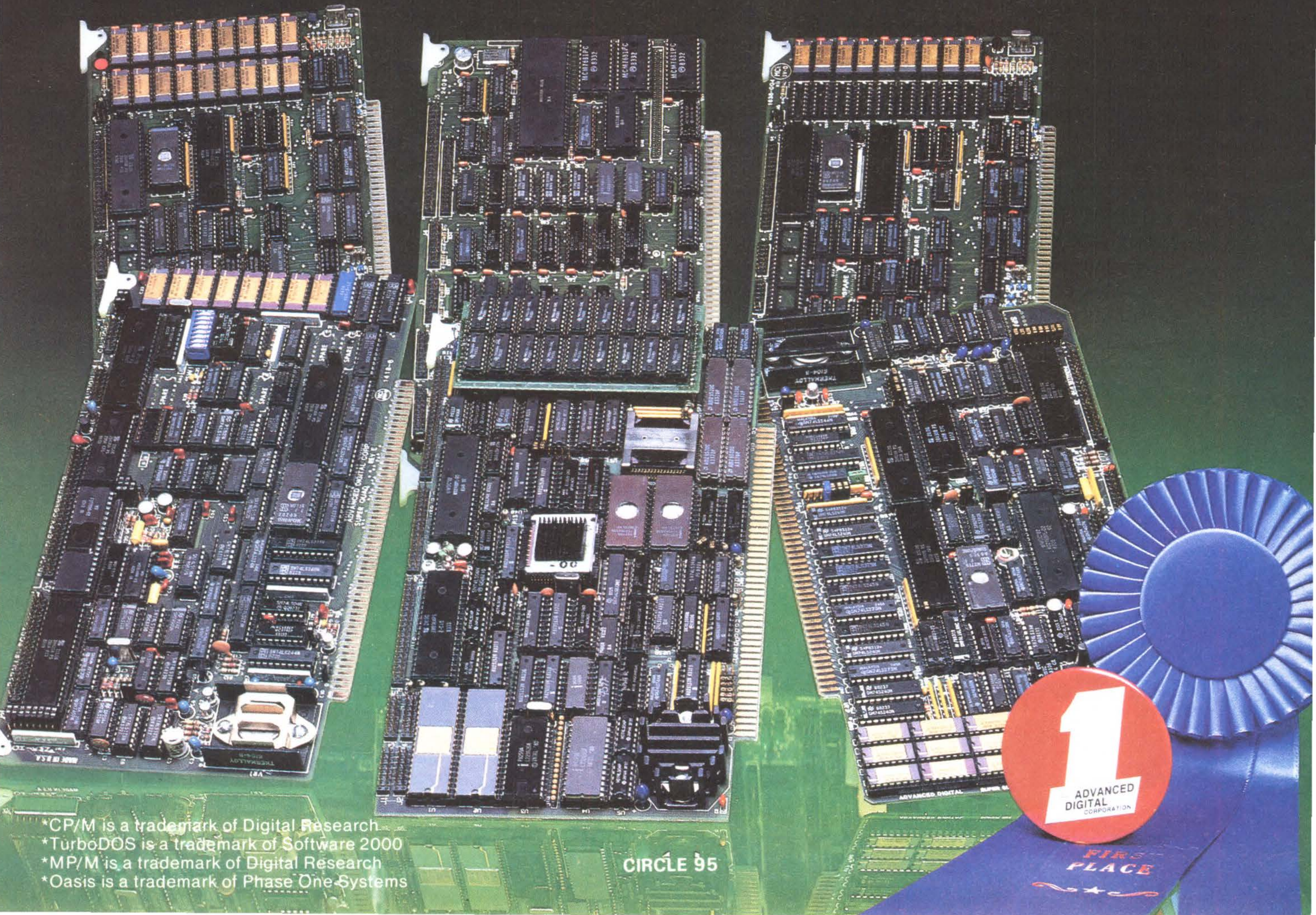

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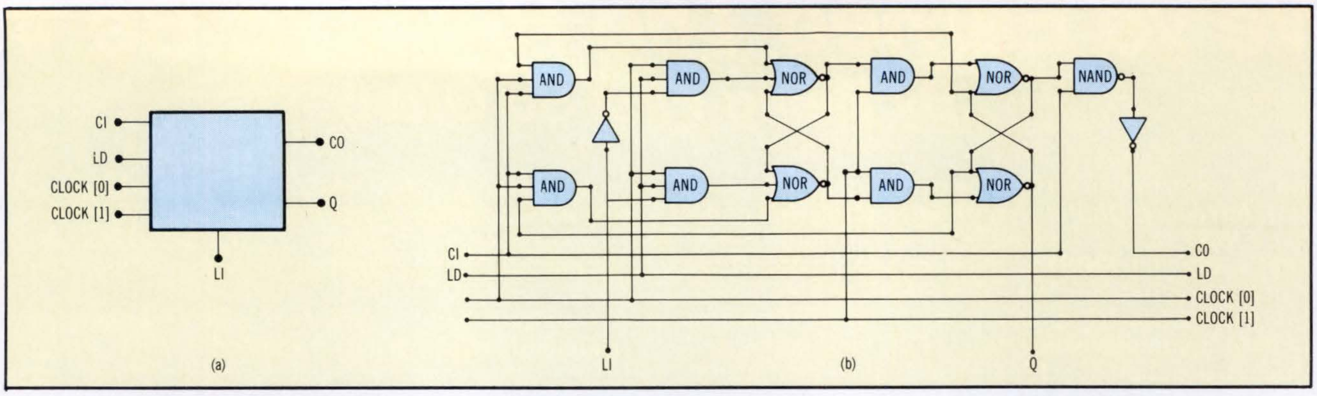

Fig 2 A graphic representation of the counter/timer circuit in the model:symbol section of the counter function can be accessed for inclusion in a logic diagram of a higher level design (a). At a lower level, the logic gate representation expands the symbol "black box" to show how the function would be implemented in SSI TTL logic (b).

which is then used by the evaluate command to produce the input for a particular simulator—in this example, Ideal. In issuing the generate command for the counter design, the engineer specifies which simulator is being used, and the level at which simulation will occur. Here, a logic model is created, so a logic level simulation is called with Ideal.

When executed, the generate command searches the data base and divides a model into the primitive components needed by the simulator—here, logic gates and inverters. To separate the model, generate traverses the data base down the design hierarchy from the counter logic model. As it moves down the hierarchy, it looks for instances of lower level gates appearing in the counter. For each gate with an instance in the counter logic diagram, generate looks for the associated ideal logic model linked to the gate symbol. This ideal model is extracted from the data base and used in preparing the net list input for Ideal.

The result of the generate command is a logic model in computer memory of the counter cell shown in Fig 2(b). However, this gate level model has little significance to a simulator such as Ideal. Thus, generate produces a text equivalent of this logic model understandable to Ideal. In place of each NAND gate, generate puts a pointer to the ideal model 'linked' to the NAND gate symbol in the NAND gate function library. It does the same for the AND and NOR gates and inverters. In addition, it provides an appropriate text that describes the interconnection of the various gates.

Once generate completes, the evaluate command executes. It extracts from ideal the information needed to create stimuli the simulator uses to verify design model operation. Thus, in the net list file, not only is there a network description, but there is also a set of stimuli required to test the circuit's function (as well as the expected response from the logic circuit). Evaluate can also provide other functions such as numbering the nodes within a logic circuit (a requirement for Spice, a transistor level simulator).

The evaluate command assembles and formats information in the net list file before submitting it to the simulation tool. Formatting requires evaluate

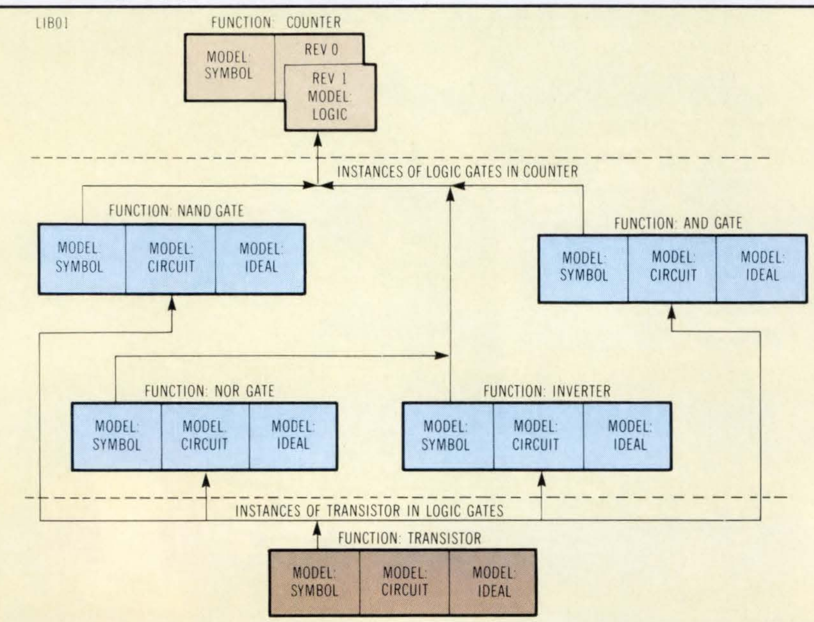

Fig 3 The CAE 2000 function library is hierarchically structured so that high level functions are built up from lower level ones. This approach allows automatic updating of designs at every level of abstraction when lower level functions are changed.

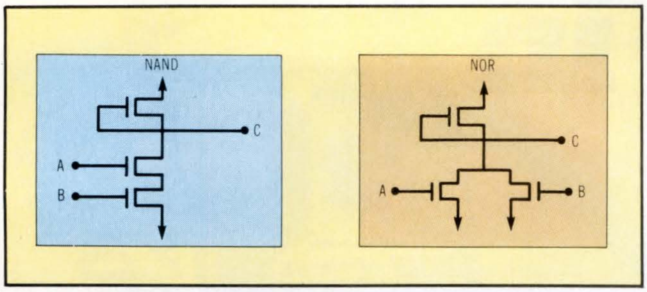

Fig 4 At the lowest level, individual gates are modeled as collections of transistors, as they would be when built onchip. Starting from this model, the CAE 2000 can perform automatic optimization at the gate level, reducing the number of gates needed to implement a circuit.

to expand on stimulus references and then perform the actual translation of a net list into a file that is acceptable to the particular simulation tool. Once the input file for a simulator is prepared, it is sent to a remote computer for execution.

After the counter's logic model is simulated, the designer may want to simulate down to the transistor circuit level. As in the logic model example, the designer issues the generate command, specifies the simulator to be used (Ideal), and then directs simulation to occur at the transistor circuit level.

The generate command again traverses the data base, but now, instead of stopping at the logic gate level in the hierarchy, it goes on to the transistor level. Thus, the transistor equivalent circuits for each of the gates are automatically inserted. Fig 4 shows the equivalent transistor for the NAND and NOR gates. As before, instead of the actual transistor circuit, generate assembles the ideal model of each transistor and provides interconnection data needed to simulate at the transistor level.

Simplifying revision control

Simulation results will typically point out some error or deficiency in the first design attempt and the engineer will use the simulation results to make changes. To illustrate how the data base facilitates revision control, consider the example in which the counter cell logic model exists in the data base and thus has been assigned a revision 0 version number.

At this point, other designers in the engineering team may use the standard counter cell to build the adjacent higher level circuits. For example, an ALU designer could sprinkle counters in various parts of the logic model. Meanwhile, the engineer in charge of the counter looks at ways to improve counter logic. When the counter logic model is changed, the engineer enters a revision of the model into the data base, but the original version remains intact. After revision 1 of the logic model enters the data base, all others using the counter cell in their designs automatically receive the latest counter logic model revision.

In the past, members of a design team would be working with different revisions of lower level system components, simply because of the time it took to promulgate the change through the documentation of the design. With the CAE 2000, a designer automatically learns of the lower level model's revision upon establishing instances of the higher level model. Thus, by examining the revision level, a designer immediately knows if a logic model has been updated since the last time it was used. Moreover, a designer, seeing that the logic model has been changed, can opt not to incorporate the revised version of the model immediately. This could be desirable if the designer has a higher level design problem and is trying to isolate the trouble. Before complicating the debug effort by introducing a revised lower level model, the designer may choose to continue using the older revision until the problem is found. Only then would a change to the newer revision be made.

Another case in which revisions are automatically promulgated without designer intervention is inputting of the net list file to the simulator design tools. As the designer changes the logic model of a counter cell, no separate net list file is needed to simulate the latest revision of the design. The generate and evaluate commands produce a new net list each time a simulation is requested. Thus, all revisions are automatically incorporated at simulation time.

Besides the automatic dissemination of the latest revision afforded by the data base, the designer can also send Unix mail messages to other design team members concerning revisions. This electronic mail capability contrasts with the older method of getting all design team members together to discuss the latest revision as well as changes made to their respective designs.

In addition to changing the logic model of a design, the designer may choose to alter its transistor level circuit representation. This may be done for any of several reasons. Foremost is that using standard logic gates may produce a circuit too large to fit the space allotted for the counter in the final chip or PC board implementations.

Easier circuit optimization

Circuit optimization is another function that a CAE workstation could handle for the designer. As previously shown, the four logic gates—AND, NAND, NOR, and inverter—all have an associated circuit model. NAND and NOR equivalent circuits are shown in Fig 4. Notice that each of these gates requires three transistors. The NAND and NOR gates in the upper right portion of the counter logic model [Fig 2(b)] alone require nine transistors. The entire counter cell could thus require as many as 30 transistors. There is obviously a lot of incentive to optimize and reduce the number of transistors.

With the CAE 2000 data base, the optimization process is made easier by the concept of links

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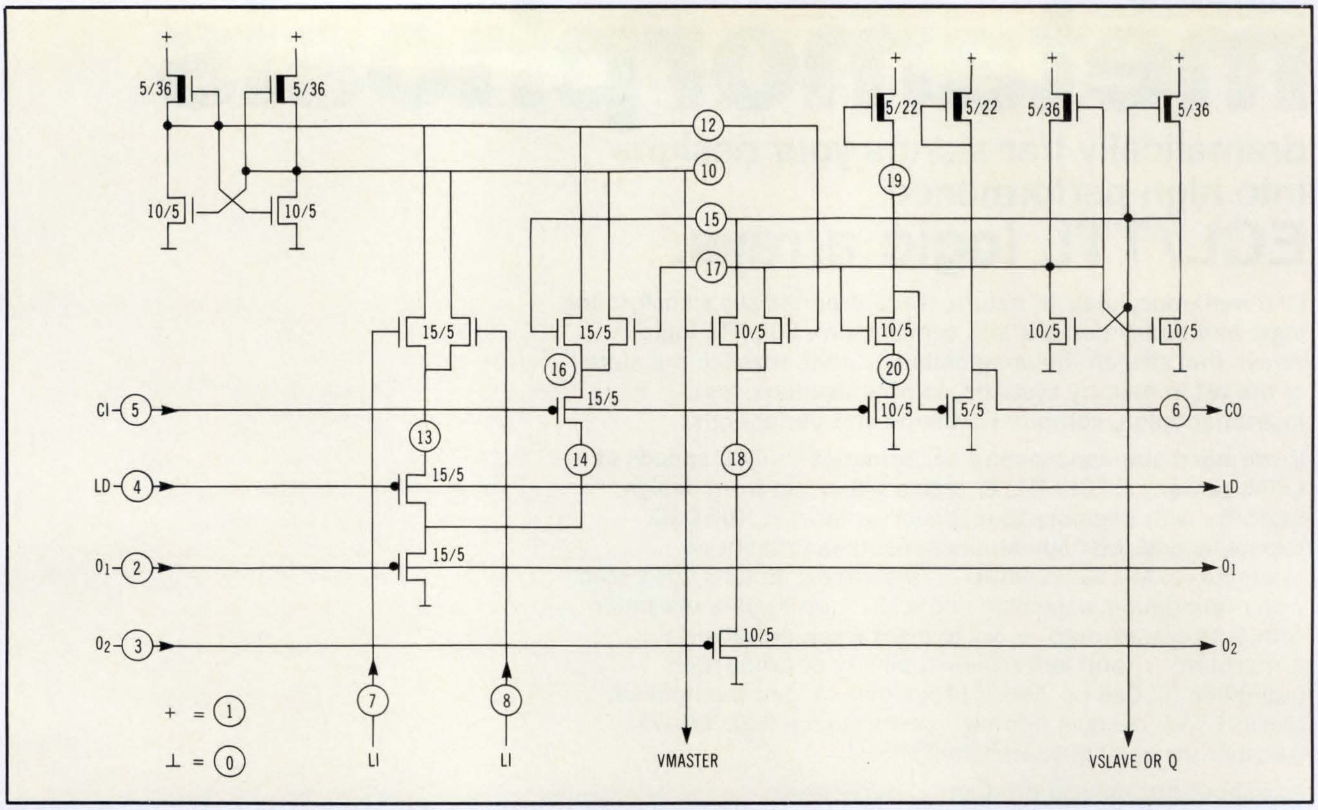

Fig 5 At a lower level, the circuit model shows the counter/timer implemented in MSI, or as part of an LSI device. This circuit is optimized by using transistors instead of logic gates.

described earlier. The designer can design an optimized version of the counter cell using transistors rather than logic gates, resulting in the optimized circuit shown in Fig 5. When the designer creates a circuit model of the counter cell, the model is linked to other models in the counter function (Fig 6). The designer concurrently creates an instance of the basic transistor symbol in the circuit model of the counter.

The CAE 2000 data base differs significantly from other DBMSs in its ability to accommodate link and instance relationships. Most other systems allow the user to establish a symbol and logic model of a given function, but few allow multiple models of the same function. Most other systems could handle the hierarchical relationship previously shown in Fig 3, but few could handle the dual hierarchical relationships shown in Fig 6.

The ability to handle multiple hierarchical relationships and multiple models of the same function has yet another benefit for the overall design effort. Perhaps a designer wants to use a counter cell

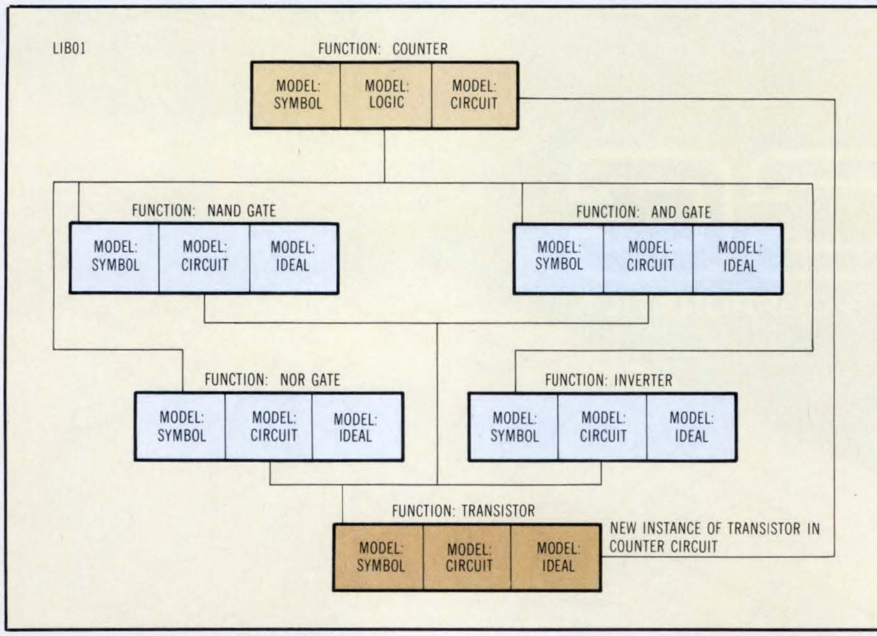

Fig 6 The hierarchical database model used in the CAE 2000 allows multiple links between different levels of the data base. In this way, a gate level description of a high level circuit is updated immediately, and does not depend on the updating of the intermediate levels.

in a high level logic circuit design (while working with a logic representation of the counter cell), but has not yet reached the circuit-level simulation stage. When the counter cell model is accessed, the designer wants to use the logic model, not the circuit model. The data base must be able to support multiple models in order to allow this.

In the CAE 2000 data base, this is as simple as creating an instance of the logic model in the next higher level design, instead of an instance of the circuit model. Moreover, the designer using the counter cell can switch between the logic and circuit models of the counter cell as needed.

Propagating a change

It is often desirable during a design task to make significant changes in the entire design. An example might be the addition of a new type of transistor to the data base. In this case, making the alteration is a matter of changing the instances of transistors already in the design to instances of the new device.

The data base allows even more dramatic changes with very little effort on the part of the designer. Take the example of the counter function shown before in Fig 1, where the designer initially specified that the function be implemented in series 74 TTL logic. As design completion draws near, the designer sees that it might be possible to upgrade the configuration to use higher speed series 74LS TTL logic, and wants to know what the upgrade will do to cost, performance, power consumption, and other variables. This is a "what if" analysis typically found in engineering.

To achieve this result, the designer previously had to do a completely new design of the same function in the higher speed TTL logic. The CAE 2000 data base now offers a way to make a massive change by making a small alteration to one file. The data base allows the designer to specify a file containing parameters used throughout a design. For example, consider a file inside of LIB01 called function:system. Transistor delay times, power consumption, and other parameters are in the file. Thus, when the system requires information on a transistor (eg, its delay time) and the data is not contained in a data sheet file linked to the transistor symbol model, the system automatically refers to the function:system file to find the information.

One entry in the function:system file could be a parameter specifying the means of implementing the overall design. For example, the parameter could call for series 74 TTL logic. Thus, all calculations for the design are based on using this type TTL logic. By changing this parameter in the function: system file, the designer could change the entire design. Calculations such as transistor delay times and power consumption per gate would be based on the faster logic. The engineer could implement the circuit in both logic families, and make determinations based on the results. Moreover, drastic changes in the data base would not be needed to achieve the comparison.

One significant contribution made by a common hierarchical DBMS such as that used in the CAE 2000 is the ability to automatically provide the required input files demanded by the wide variety of available simulation tools. On previous CAD systems, the designer had to produce a separate input file for each simulator chosen for use in verifying a design. Each time a revision was made in a design, the input file to each simulator had to be updated.

This situation is complicated by having a number of different design tools, each for simulating a specific part of the design. Spice, for example, is a transistor level simulator. It goes through a design and computes voltages and currents as a function of time. The input to Spice is a schematic representation of a circuit with the nodes numbered in a particular fashion.

In contrast, Logis—a logic level simulator—handles higher level functions like flipflops and gates. Others might handle RAM, ROM, counters, and shift registers. The input requirements for each of these tools are entirely different and the designer has to prepare individual net list files for each. The problem is having multiple representations of the same data being produced by different sources, all of which exist in the system at the same time, but may not necessarily reflect the same revision level.

The hierarchical data base specifically addresses this problem. It is used by the system to prepare the input net list for a variety of different simulators. Thus, each time a revision occurs to any part of the design, it is automatically used for creating the input file for any simulator specified. In other words, there is one source for all input files to all simulation tools.

The data base allows multiple models for any given function. Each function has a model for various simulators supported by the system. Currently, the CAE 2000 DBMS supports the Ideal and Spice simulators. However, support for Tegas, Logis, and others will come in time. Adding each new simulator to the system is as simple as adding the file to a given function and linking the file to the symbol model of the function.

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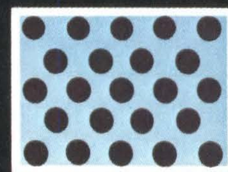
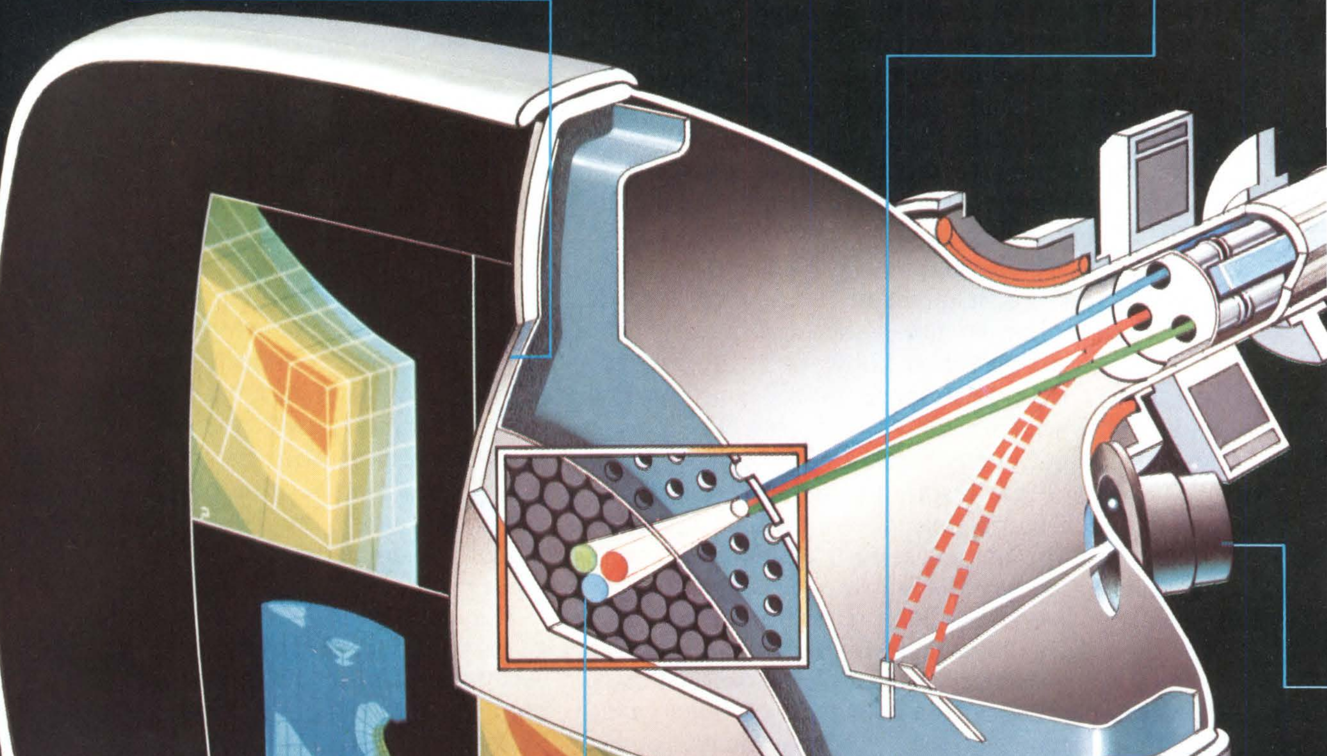
High 707 *Average 708* *Low 709*

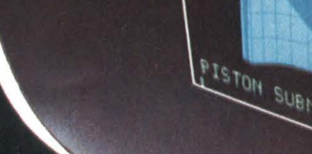
Who solves the misconvergence problems no one else will talk about?

An aluminum layer between the shadow mask and the screen reflects light from the phosphor dots out toward the viewer and at the same time prevents errant screen light from reaching the photodetector.



The 4115B's patented AutoConvergence is accomplished by applying non-parallel indexing phosphors at precise angles and positions at the rear of the CRT shadow mask, detail at left.





Delta configuration of the electron guns helps maintain both high resolution and optimum spot profile throughout the screen—not just the center.

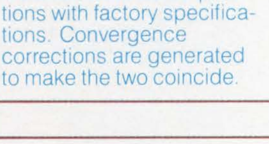
Tektronix.

The higher the visual resolution of a color display, the more difficult it becomes to converge the color beams at a precise point.

Yet, without precise control of convergence, productivity gains promised by high resolution graphics simply can't be realized.

That's why Tek designed the 4115B with AutoConvergence as our engineering prerequisite.

The engineering work environment is tough on high resolution displays. A shift in display angle for better viewing. Mild vibration from a stray elbow. Minor temperature change. Circuit drift. Tube aging. The earth's magnetic field.



A photodetector picks up light from the indexing phosphors. A microcomputer then compares instantaneous beam positions with factory specifications. Convergence corrections are generated to make the two coincide.

They all can cause the color line blurring effects commonly called *misconvergence*.

Loss of detailed information, especially in corners. Fuzzy, fringed colors. And visual ambiguity. All of which can lead to user fatigue, error and loss of productivity.

Until the 4115B, manual reconvergence was typically up to an hour-long task for a service technician—resulting in even more lost time.

No wonder most display manufacturers won't talk about the problem. But Tek will. Because we solved it with our exclusive AutoConvergence.

Push one button on the 4115B and all three electron guns are converged automatically. In 20 seconds. Not just in the screen center but from corner to corner.

Convergence accuracy is within .25mm, as compared to the 0.3mm to 1.0mm achievable by manual or other techniques. There's no interruption to work, so there's no loss of productivity.

The 4115B's high performance doesn't stop with AutoConvergence. It just begins there. You can apply its 60 Hz non-interlaced, 1280 x 1024 display, 50,000 vector/second redraw speed and user selectable 32-bit coordinate space to optimize productivity on any application.

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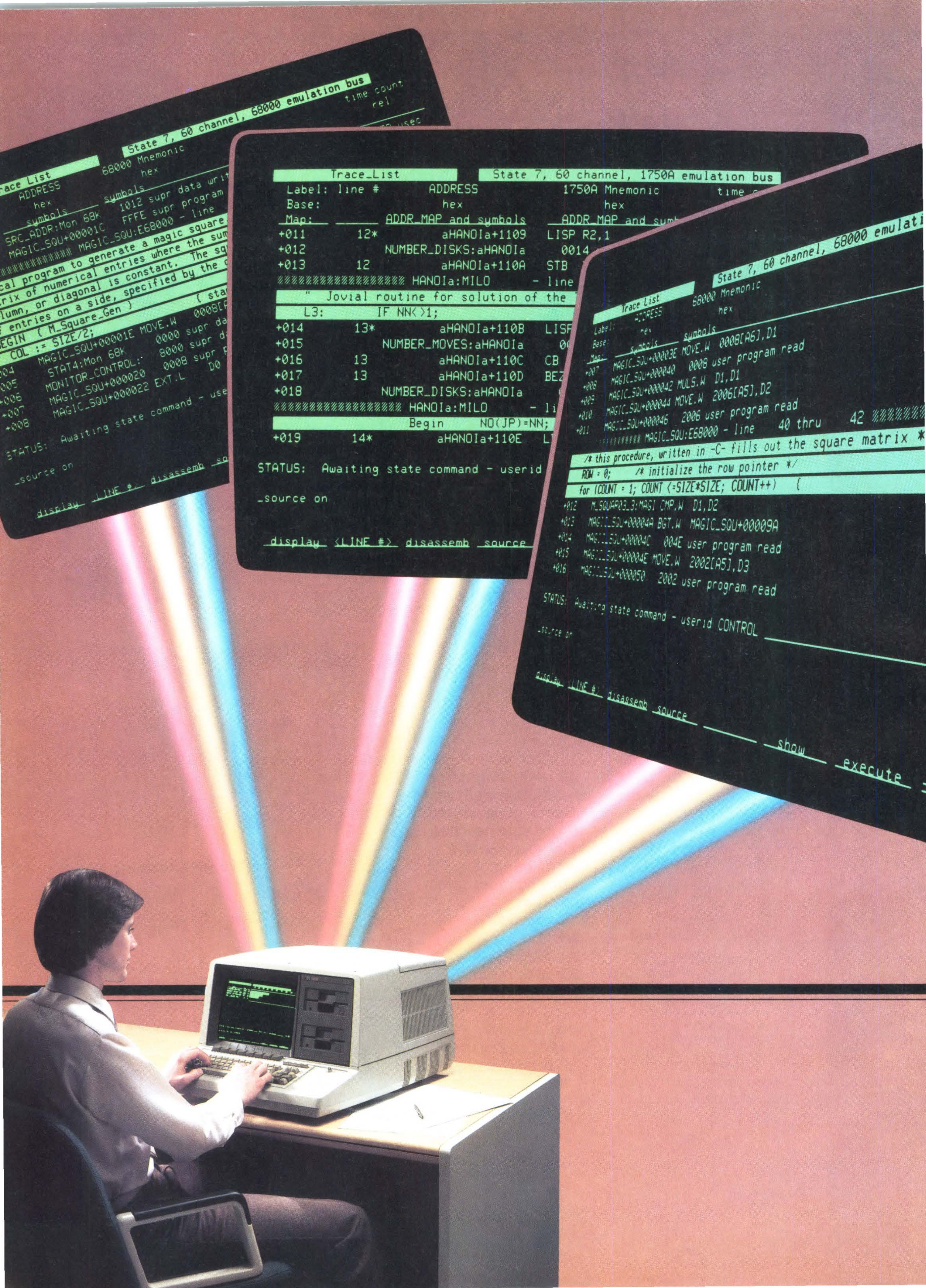
Trace_List
State 7, 60 channel, 1750A emulation bus
Label: line # ADDRESS 1750A Mnemonic
Base: hex hex
Map: ADDR_MAP and symbols ADDR_MAP and symb
+011 12* aHANOIa+1109 LISP R2,1
+012 NUMBER_DISKS:aHANOIa 0014
+013 12 aHANOIa+110A STB
HANOIa:MILO - line
" Jovial routine for solution of the
L3: IF NN<>1;
+014 13* aHANOIa+110B
+015 NUMBER_MOVES:aHANOIa
+016 13 aHANOIa+110C CB
+017 13 aHANOIa+110D
+018 NUMBER_DISKS:aHANOIa
HANOIa:MILO
Begin NO(JP)=NN;
+019 14* aHANOIa+110E
STATUS: Awaiting state command - userid
_source on
display <LINE #> disassemb source
State 7, 60 channel, 68000 emulation bus
Trace List
68000 Mnemonic
MAGIC_SQU+00003E MOVE.W 0008[A6],D1
MAGIC_SQU+000040 0008 user program read
MAGIC_SQU+000042 MULS.W D1,D1
MAGIC_SQU+000044 MOVE.W 2006[A5],D2
MAGIC_SQU+000046 2006 user program read
MAGIC_SQU:E68000 - line 40 thru 42
/* this procedure, written in -C- fills out the square matrix */
ROW = 0; /* initialize the row pointer */
for (COUNT = 1; COUNT <=SIZE*SIZE; COUNT++) {
STATUS: Awaiting state command - userid CONTROL
disassemb source show execute

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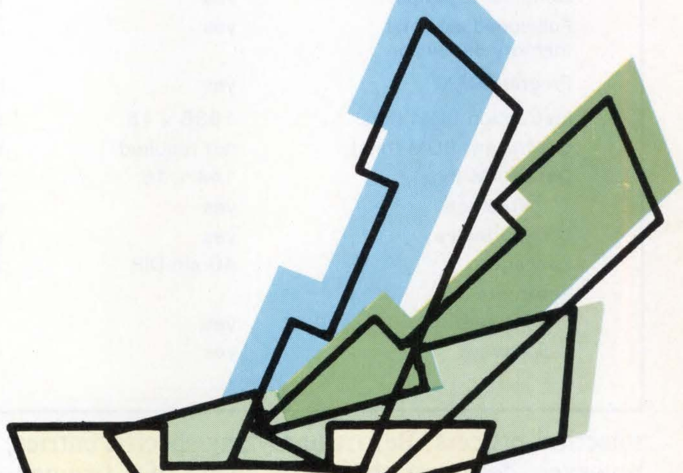
SIGNAL PROCESSING CHIPS INVITE DESIGN COMPARISONS

Selecting one of the new number-crunching digital signal processing ICs calls for a comparison of hardware, software, and development system features.

by Surendar S. Magar



Digital signal processing techniques are taking over a wide variety of instrumentation, numerical processing, and sensing and control functions that were formerly filled by purely analog systems. These techniques offer better precision and accuracy at a lower cost than do analog components. In addition, digital signal processing elements are less susceptible to drift, and are relatively insensitive to supply voltage variations. In analog signal processing, precision to 0.1 percent is considered excellent, but it is almost impossible to achieve with current components and design techniques within a reasonable cost. Digital systems, on the other hand, can achieve such precision with ease.

Methods for processing signals numerically have been researched for over 20 years. However, general purpose, digital signal processing (DSP) building blocks have only recently been available to designers. These building blocks are a special class of microcomputer chips designed to support high speed, numeric-intensive applications. In effect, they digitally implement many well-known analog functions. The goal of all DSP chips is to provide the numerical processing capabilities of array processors on a single chip.

Four commercial single-chip DSP devices are currently available to designers. These include the TMS32010 from Texas Instruments (Houston, Tex), the μPD7720 from Nippon Electric (NEC) (Natick, Mass), the American Microsystems (AMI) (Santa Clara, Calif) S2811 and the 2920 from Intel Corp (Santa Clara, Calif). Although the four have some similarities, there are significant technical differences in such features as chip architecture, arithmetic speed, onboard memory, I/O capability, instruction sets, and software-development support tools. Since all the chips are relatively new, most designers will be unfamiliar with the technical trade-offs in selecting one of the devices for a specific task. The best way around this is to compare the devices' capabilities using published data.

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Surveying DSP arithmetic capabilities

Table 1 summarizes the major features of the available DSP chips in a comparison format. It includes arithmetic capabilities, in addition to other technical characteristics frequently used in the

TABLE 1

Competitive Features of DSP Chips

Feature	TI TMS32010	NEC μPD7720	AMI S2811	Intel 2920
Data-word size (bits)	16	16	16	25
Coefficient size (bits)	16	13	16	Variable
Accumulator width (bits)	32	16	16	28
Saturation arithmetic	hardware	software	hardware	hardware
Boolean logic operations	yes	yes	no	yes
Multiplier implementation	hardware	hardware	hardware	software
Multiplier precision (in x in = out)	16 x 16 = 32	16 x 16 = 32	12 x 12 = 16	12 x 25 = 28
Multiplication time (ns) (worst case)	200	250	300	4800
Parallel I/O (bits)	16	8	8	4 in/8 out
Instruction word (bits)	16	23	17	24
Instruction cycle (ns)	200	250	300	400
Subroutine levels	50	4	1	none
Iteration (loop) counter	yes	no	yes	no
Conditional jumps	yes	yes	yes	no
Full-speed external memory expansion	yes	no	no	no
Program RAM	yes	no	no	no
Instruction ROM (bits)	1536 x 16	512 x 23	256 x 17	192 x 24
Coefficient ROM (bits)	not required	512 x 13	120 x 16	—
Data RAM (bits)	144 x 16	128 x 16	128 x 16	40 x 25
Z^{-1} function	yes	yes	yes	no
Lookup tables	yes	yes	yes	no
Package	40-pin DIP	28-pin DIP	28-pin DIP	28-pin DIP
Interrupts				
Hardware	yes	—	—	—
Software	yes	—	—	—

selection process. Before analyzing specific entries, however, designers should be aware of a few general considerations regarding DSP devices.

For most applications, a single chip is preferable to multichip designs. Single chips eliminate the need to pass data and instructions from one processor to another. Such "handoffs" can lead to timing and synchronization problems, and may require special software to permit multiple processors to work together. Moreover, multiple processor systems consume more power, are less reliable, and more expensive.

Although arithmetic speed is, of course, a key prerequisite of DSP devices, speed alone cannot sufficiently handle many applications. The ALU of an ideal DSP chip should also perform Boolean operations to provide bit-manipulation capability. Such logical operations (eg, AND, OR, and Exslusive OR) can control those occurring both on and off the DSP chip. Three of the four chips being considered provide this capability.

Any discussion of DSP components must focus on device speed since the chips are, first and foremost, number crunchers. For example, TI's TMS32010 can execute at the rate of 5 million instructions per second (MIPS). In DSP particularly, actual operation-execution times—and ultimately throughput—are critical, whereas the system clock rates and cycle times are only significant in their effects on final throughput.

Complex mathematical operations in the analog domain (eg, differentiation and integration) are implemented in the digital world by means of multiplications and additions. Therefore, the speed at which a DSP chip multiplies and accumulates is one reliable indicator of its overall arithmetic capabilities. Moreover, according to Table 1, a hardware implementation of the multiplication function provides the fastest operation. Multiplication of two 16-bit numbers can run up to 200 ns in DSP chips.

Such signal processing microcomputers deliver this level of high speed multiplication via dedicated onchip hardware rather than relying on slower software routines. Fig 1 shows a typical implementation of an advanced signal processing microcomputer. Here, a 16-bit T register temporarily stores the multiplicand, and the P register stores the result. Multiplier values come either from data memory

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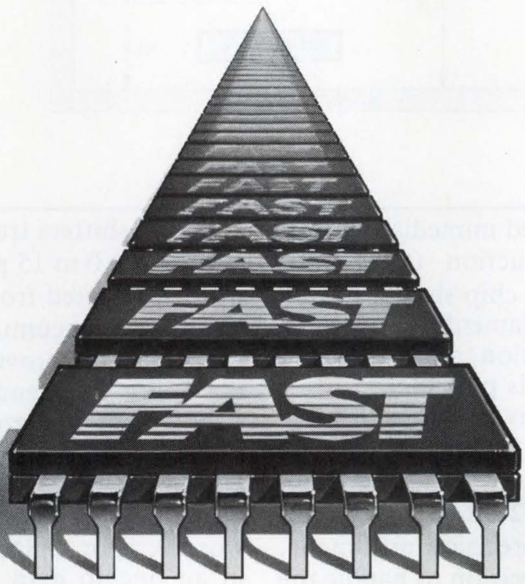

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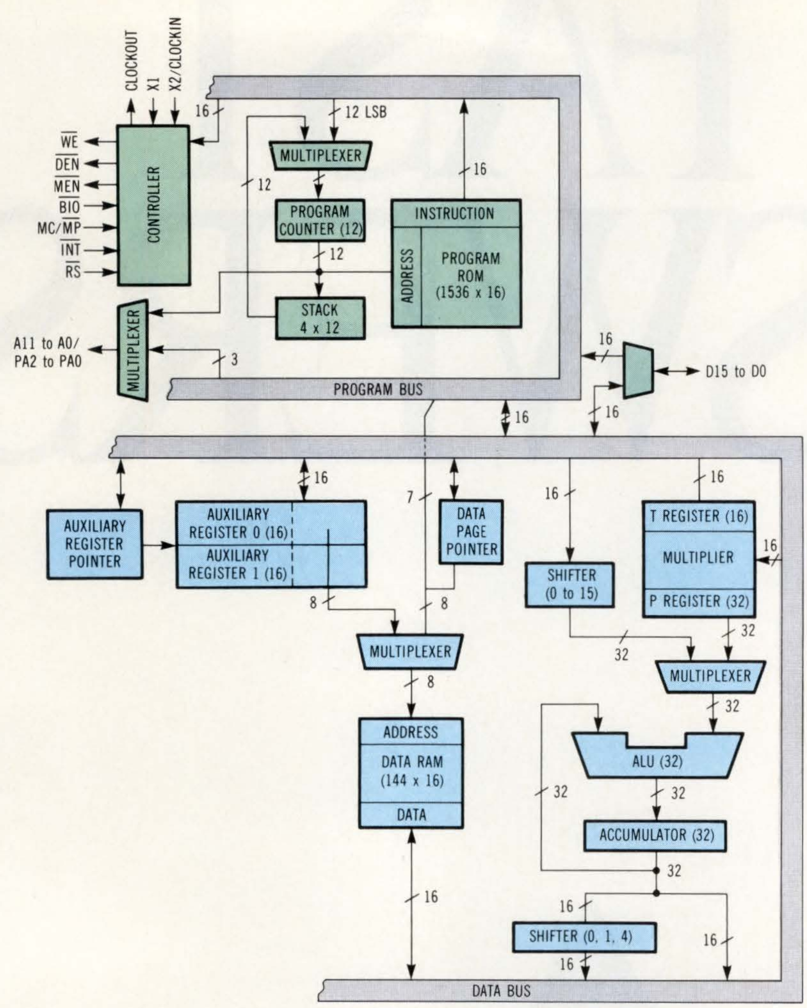


Fig 1 A modified Harvard architecture adds speed to flexibility. Moreover, it allows transfers between the program and data memories so that data stored in the program ROM can be moved to the data RAM.

(via the data bus) or are derived immediately from the multiply-immediate instruction (MPYK). In addition to multiplication, the chip should be able to rapidly perform other fundamental DSP operations (eg, convolution, correlation, and transversal filtering—2.5 x 10^6 samples/s is possible).

While a hardware multiplier is vital to high speed arithmetic performance, other dedicated hardware arithmetic elements such as the ALU/accumulator and shifters play key roles. A 32-bit ALU and accumulator support fast double-precision arithmetic. This provides the necessary precision to handle the 16- x 16-bit multiplier output without losing data. Though most DSP calculations are fixed point, floating point calculations must sometimes be implemented efficiently. Another onchip hardware element, a barrel shifter, which operates over entire 16-bit data words, can speed up both bit-manipulation and floating point operations. Thus, a hardware barrel shifter adds control and dynamic range capability to a DSP microcomputer. To be most effective, onchip barrel-shifter outputs should be directed to the ALU/accumulator.

Barrel shifters transpose the data within a 16-bit word from 0 to 15 places before the bits are loaded into, subtracted from, or added to a number in the DSP chip's accumulator. This shifting capability automatically provides 2's-complement arithmetic capability by extending the highest order bit of the data word and zero-filling the low order bits. One way to complete a chip's total shifting requirements adds a second onchip shifter (see bottom of Fig 1). This shifts the upper half of the 32-bit accumulator word 0, 1, or 4 places while its data is being stored in an onchip data RAM. Both shifters come into play in scaling and bit-extraction operations.

Onchip and offchip memory considerations

Each of the four DSP contenders offers varying amounts of instruction (ROM) and data (RAM) memory. The ROM portion is usually mask programmable at the manufacturer's factory and holds the user's program. Obviously, the faster the onchip memory is, the better. When coefficients for the processing in progress can be stored in the program memory along with instructions (as in a modified Harvard architecture) a separate coefficient ROM is not required. Microcomputer chips for signal processing that combine large onchip RAM with Harvard architecture are, therefore, more flexible than their Von Neumann counterparts.

Computers built around a Harvard architecture, from room-sized mainframes to single chips, separate program and data memories into two distinct spaces. This structure permits full overlapping of instruction-fetch and execution cycles. While still retaining this speed-enhancing parallelism, a Harvard architecture can be modified to allow transfers between the program and data storage spaces. Signal processing microcomputers that provide this capability are more flexible for DSP operations. The result for designers is often simpler, faster-acting code.

A modified Harvard architecture, for example, permits coefficients stored in program memory to be read into data memory. This eliminates the need for an onchip ROM solely dedicated to storage for specific coefficients. The RAM data can be updated, revised, or totally changed on the fly, whereas once data is burned into an onchip ROM, the chip becomes dedicated to that function alone. Moreover, if the microcomputer's data memory is 16 bits wide, 16-bit coefficients can be stored in one addressed location, making the processing faster than if several fetches are needed.

Both the TMS32010 and AMI's S2811 provide 16-bit data memory while NEC's μPD7720 and Intel's 2920 do not. Moreover, coefficients stored in program memory can be accessed more quickly via a Table Read instruction. The instruction uses the chip's accumulator as an address pointer to a table of coefficients. This facilitates the numerous table-lookup operations often required in signal processing operations.

In addition to fast onchip memory, signal processing microcomputer chips must often operate with offchip memory. Some programs contain many complex algorithms. Such operation becomes more flexible when the chip can operate at its full processing speed and maintain maximum system-level throughput while working with offchip memory. Many of today's larger DSP programs require up to 8-Kbytes (4-K words) of memory, and the programs are expanding all the time (Fig 2).

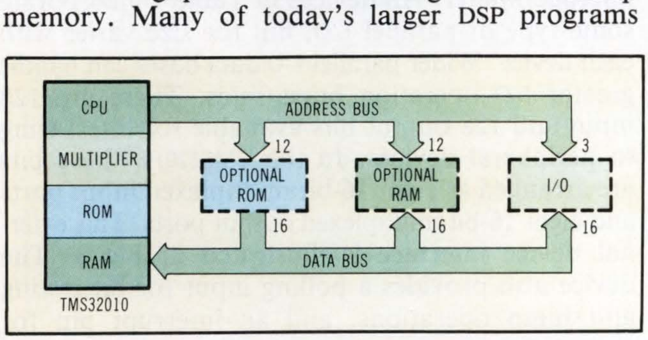


Fig 2 The only DSP chip capable of executing from an offchip memory, the TMS32010 can access an additional 2560 words without losing processing speed.

Execution at full speed from offchip storage translates into several benefits. First, prototyping and development work become simpler and more reliable using at-speed offchip storage. The offchip memory can be used to hold data that changes often or is updated. Secondly, downloading code from another system is simpler in an offchip memory. Then, the program can execute from an external RAM. This effectively increases the system's total storage capacity. In addition, offchip storage capacity lets designers specify the off-the-shelf memory device that is closest to the unique price/performance requirement of a particular system.

Sixteen-bit data words permit simple transitions between instruction and data memory in modified Harvard architectures.

Operation with offchip memories of various speeds helps tailor the memory parameters—cost, speed, and power capacity—to individual needs. Memory-expansion capability also lets the user run several programs that share common subroutines. Such common code might be stored onchip, while application-specific code can be stored offchip. Then, either through downloaded programming or personality modules, the character of a signal processing microsystem can be altered.

At 144 words x 16 bits, the TMS32010 data RAM's 288 bytes are the largest of any of the four DSP chips. While the NEC and AMI devices come close at 128 words, the additional 16 words in TI's RAM serve a highly useful purpose. For example, the TMS32010 is the only device that allows the computation of a 64-complex point fast Fourier transform (FFT) using onchip RAM only. The 128 words can hold the data, and 16 words can be used as scratchpad or temporary storage.

As Table 1 shows, 16 bits is the most popular data-word size in DSP chips. One reason is that the size is compatible with conventional 16-bit data buses and memory chips. Sixteen-bit data words permit simple transitions between instruction and data memory in modified Harvard architectures. However, this data word/instruction word compatibility is not universal.

Some DSP chips use a 16-bit data word as the input, but internally the word must be expanded further to obtain the precision necessary for many computations. In general, inputs to a DSP device from A-D converters or other I/Os range between 12 and 16 bits. Signal processing microcomputer chips expand these further to stretch the dynamic range of the data processing system.

Another rationale for the 16-bit data word is based on the method of entering data into the DSP chip from the converter. For example, if a 16-bit input is read in two passes—8 bits at a time—data processing becomes more difficult since the two words must be properly synchronized when processed by the chip. The result is that two-pass techniques require complex software, complex hardware, or both.

Instructions and processing capability

A DSP device's ideal instruction set minimizes the number and complexity of commands in order to support high speed computation and program execution. As Table 1 illustrates, each DSP chip handles instructions in a different manner. Intel's instruction-set word for the 2920 is the largest at 24 bits, while its instruction cycle for the device is the longest. TI, on the other hand, uses the smallest instruction word (16 bits) coupled with the fastest instruction cycle time. As the entries for the other devices show, longer words do not necessarily lead to faster execution times.

One way to increase a DSP chip's execution speed is to use a large proportion of single-cycle instructions. Only less frequently used commands such as branch and I/O instructions should spread over multiple cycles. Another advantage of short, single-cycle instructions is that communications are simplified when operating with an offchip memory.

Arithmetic instructions, in particular, must execute at a high speed to enhance a DSP chip's number-crunching ability. The TMS32010's multiply (MPY) command, for example, executes in a single cycle (200 ns) and the conditional subtract for divide instruction (SUBC), which performs the shifting and

A DSP device's ideal instruction set minimizes the number and complexity of commands to support high speed computation and program execution.

conditional branching for division, is also a single-cycle command. However, DSP algorithm designers usually shun division.

Although DSP devices mainly perform calculations, they should provide some special functions specifically related to DSP operations. One such function, called the sample delay of operation or Z^{-1} (see Table 1), uses such a dedicated instruction. The Z^{-1} function is required to handle filtering, convolution, and correlation operations. All but one signal processing microcomputer chip offer this feature.

Arithmetic overflows create special problems in DSP computations. Overflows can cause swings between large and small numbers, leading to erratic

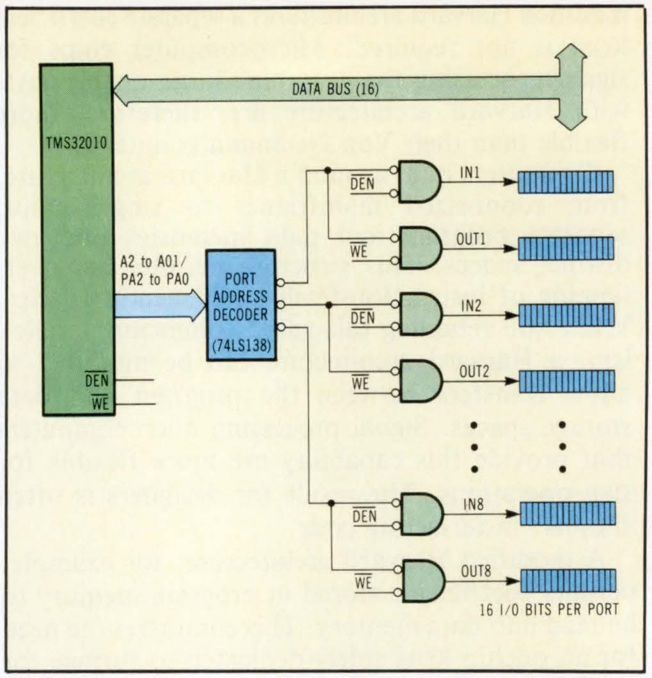


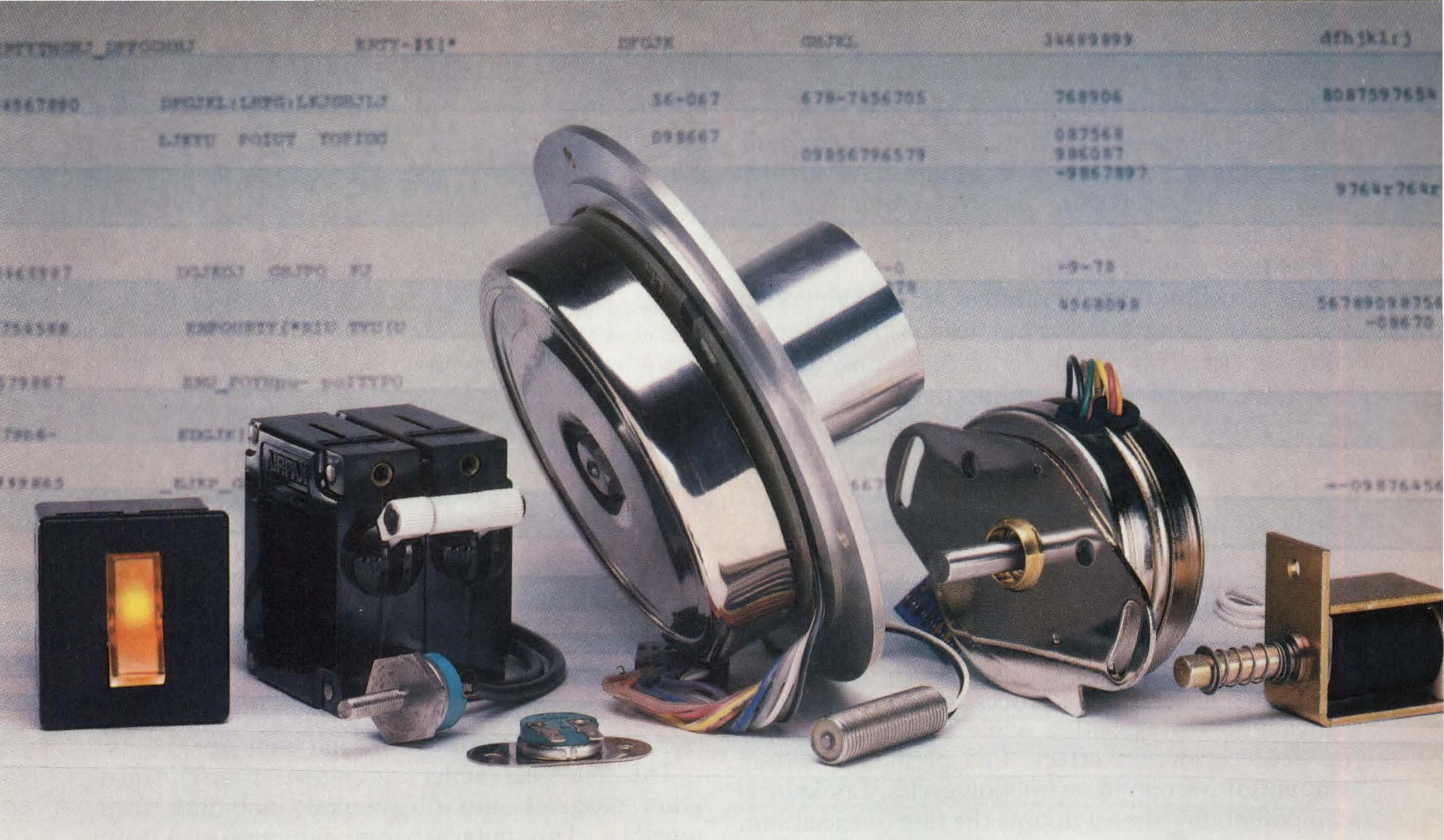
Fig 3 External peripherals interface with the TMS32010 through eight 16-bit multiplexed input ports and the same number of output ports. These ports provide 128 input and 128 output bits for communicating with external devices.

system behavior. DSP chips use a variety of hardware and software techniques to compensate for this behavior. A special overflow mode set by a dedicated instruction serves as the simplest design method. This causes either the largest or smallest representative value of the ALU to be loaded into the accumulator, which essentially models the saturation characteristic of an analog system. When another instruction disables the overflow mode, unmodified overflow results are loaded into the accumulator.

An instruction called branch on overflow (BV) can then check the overflow flag register. This produces a branch if an overflow occurs. Thus, it is possible to test for overflows without infringing on the time used for speed-critical routines.

Besides arithmetic operation performance, a chip's I/O capability is an important issue in a DSP microcomputer. All devices in Table 1 incorporate some type of parallel I/O, but the size varies with each device. Wider parallel I/O data buses can handle greater I/O operation burst rates. There are 128 input and 128 output bits available for interfacing to peripheral devices. In the TMS32010, these bits are arranged as eight 16-bit multiplexed input ports and eight 16-bit multiplexed output ports. This external device interface is illustrated in Fig 3. The device also provides a polling input for bit testing and jump operations, and an interrupt pin for multitasking.

As with manufacturers of conventional microprocessors and microcomputers, DSP chip manufacturers can make endless device parameter comparisons



without ever fully documenting one chip's superiority over another. For this reason, comparisons made using a benchmark procedure have greater validity. This procedure involves comparing the time it takes for two or more devices to run a well-defined, recognized routine.

One of the most useful routines for benchmarking signal processing microcomputers is the 64-point complex FFT. This calculation is commonly used in DSP applications. Table 2 shows the results of performing the FFT on both the TMS32010 and the μPD7720. The FFT program occupies 2.9 Kbytes of the total 4-Kbyte memory space. This leaves 1 Kbyte for control programs to implement FFT-intensive systems. Such systems are of the vocoder and spectrum-analyzer type.

A major reason for the high performance of all DSP chips is their use of parallel processing—sometimes called lookahead—in the arithmetic unit. In parallel processing, a processor can prepare one instruction for execution while actually executing its predecessor. In effect, this permits a certain amount of overlap in instruction cycles. Lookahead can potentially almost double the rate of execution. In parallel operation, instructions are issued to specialized execution units, each of which operates independently and simultaneously.

Pipelining is an extension of parallel processing in which instructions are broken down into a series of simple, short operations. Each operation is executed in assembly-line fashion with simultaneous computations on different sets of data. A multiplication operation, for example, can be reduced to a number of segments, each executing in one clock period. When the first segment is complete, its intermediate results are passed to the second segment; when the second segment is complete, results are passed to the third. This process continues until the entire multiplication is finished. Meanwhile, the first segment begins a second multiplication as soon as its first operation is ended. This allows a DSP chip to perform high speed arithmetic calculations.

A totally pipelined architecture imposes difficult constraints on system designers and programmers. Hence, the best signal processing microcomputers use more parallelism than pipelining. Instruction sets then become simpler and more user efficient.

Ensuring adequate software support

DSP microcomputer chips require the same degree of hardware/software support as a general purpose microcomputer does for any application. For the user, this means that a careful evaluation must be made before selecting a chip, since semiconductor manufacturers have not been traditionally strong in software support.

A useful set of development tools would include host-independent hardware (along with software) that runs on a variety of popular supermini or mainframe computers (eg, the DEC VAX and the IBM 370). In the initial development phase, a designer needs an evaluation module to characterize the signal processing microcomputer's performance. More sophisticated development operations are then performed with a package that provides a macroassembler, linker, simulator, and emulator.

TABLE 2

Benchmark Comparison
TMS32010 versus μPD7720

	TMS32010	μPD* 7720	Unit
Biquad filter	1.8	2.25	μs
Sine or cosine	4.8	5.25	μs
μ/A law to linear conversion	0.8	0.5	μs
32-point complex FFT	0.254	0.7	ms
64-point complex FFT	0.555	1.6	ms
Normalized total:	1.0	2.7	

*Benchmarks from NEC Electronics' Digital Signal Processor Data Sheet, 1982 Microcomputer Division Catalog, p 551.

The macroassembler and linker translate program modules into object code and link them together. This puts program modules in a form suitable for loading into the simulator or emulator. The simulator provides a fast means for initially debugging software, while the emulator permits realtime in-circuit emulation to enable total system-level debugging. For development work on the 320 family of signal processing microcomputers, TI offers such a kit of tools—the XDS 320.

If a DSP chip achieves wide acceptance among users, independent software suppliers will write chip-compatible programs. One such package is now available from Digital Signal Processing Software, Inc of Ottawa, Canada. The company sells a complete signal processing software package that interfaces the TMS32010 to a DEC PDP-11 minicomputer. In addition to the software, the user obtains hardware that includes an A-D, D-A, 4-Kbytes of RAM and an interface to the PDP-11 via a standard DR-11 16-bit controller. The hardware (together with the assembler and signal processing software) provides software development, assembly, and downloading from any PDP or LSI-11/RT-11 system. Results from the signal processing microcomputer's program and data RAM can be transformed into the PDP-11 for user examination. Programs are available for a biquad filter, linear predictive code synthesis, FFT butterfly structures, auto-correlation, windowing, and other DSP operations.

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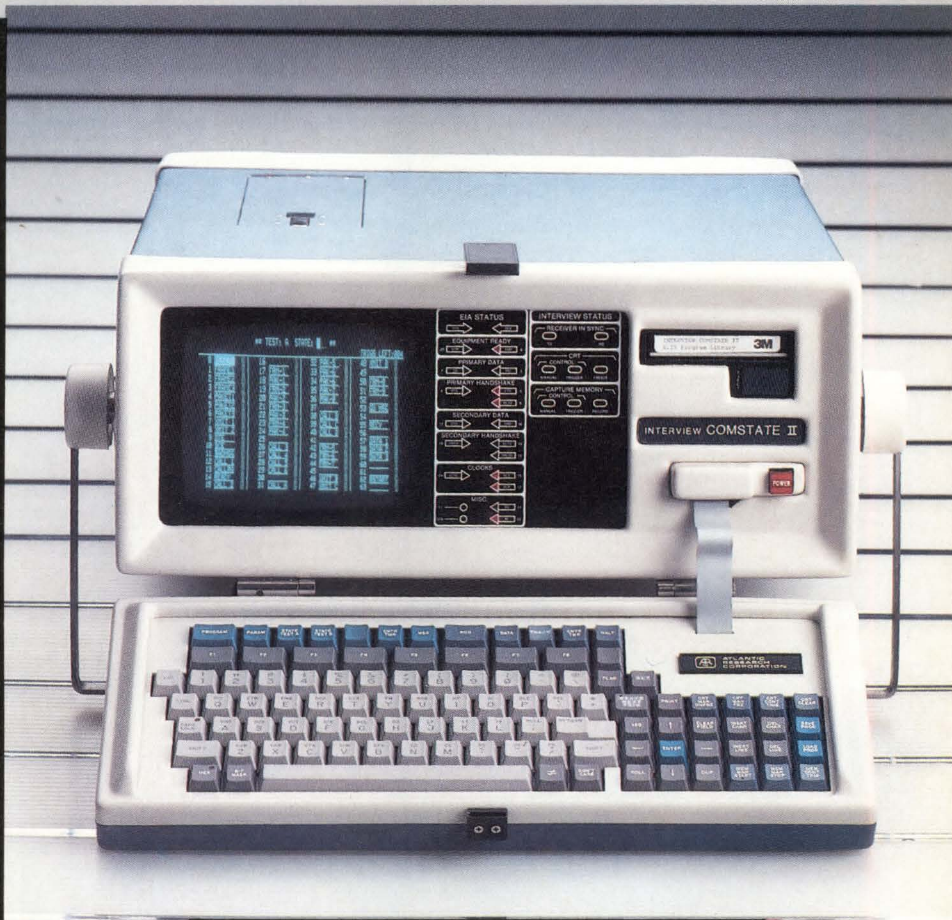


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*EM DCE/LINE*   BLOCK=225  01/17 1521
EBCDIC/8/NONE/SDLC

            TEST A                          TEST B
* LINKUP:                          LINKUP:
*         INIT LINK - SNRM                  LINK DEVICE UP
* ACTPU :                          ACTPU :
*         ACTPU TO CONTROLLER               ACTPU COMPLETE
* ACTLU :                          ACTLU :
*         ACTIVATING LU                     ACTLU POS RESPONSE
* BIND  :                          BIND  :
*         BINDING DEVICES                   BIND POS RESPONSE
* SDT   :                          SDT   :
*         START DATA XFER                   SDT POS RESPONSE
* MENU  :                          LU-LU :
*         SEND MENU TO SCREEN               IDLE LINK
                                 * ECHO  :
                                 *          PA2 MENU REQUEST
* PA2   :
*         SEND PA2 MENU          * LU-LU :
                                 *          LINK IDLE
                                 * ECHO  :
                                 *          CLEAR FUNCTION REQ
* CLEAR :
*         SEND ERASE WRITE         LU-LU :
                                 *          ATTENTION REQUEST
* UNBIND:                          UNBIND:
*         SEND UNBIND                       UNBIND POS RESPONSE
* DACTLU:                          DACTLU:
*         SEND DACTLU                       DACTLU POS RESPONSE
* DACTPU:                          DACTPU:
*         SEND DACTPU                       DACTPU POS RESPONSE
* LINKDN:                          LINKDN:
*         SEND DISCONNECT                   UA RESPONSE
*         TEST COMPLETE
01/17 1523    109423     25478     895       23        127       4257
* LINKUP:                          LINKUP:
*         INIT LINK - SNRM                  LINK DEVICE UP
* ACTPU :                          ACTPU :
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The processing speed of a bit-slice-based computer. In a single, 40-pin package. That's the new TMS320 Processor from Texas Instruments. Making digital signal processing (DSP) feasible anywhere, anytime.

For example, the lineman's advanced testing unit shown here. Only a concept now, it could be a reality tomorrow. The new TMS320 would enable the unit to process a staggering amount of data. Permit portability. Assure reliability. And allow quick programming changes for performing a wide variety of analyses to diagnose trouble, even up the pole.

5,000,000 instructions per second

This incredible performance is achieved through TI's modified Harvard architecture. It allows the TMS320 to fetch one instruction while executing another. In a typical application, more than 90% of all instructions are executed in a 200-ns cycle by the TMS32010 version.

32-bit precision

While the TMS32010 accepts 16-bit inputs and has a 16-bit output, its 32-bit arithmetic logic unit (ALU) and accumulator carries all of the arithmetic functions to 32 places. The ALU also features a 16-bit × 16-bit parallel multiplier that can form a 32-bit product in 200 ns.

Large on-chip memory

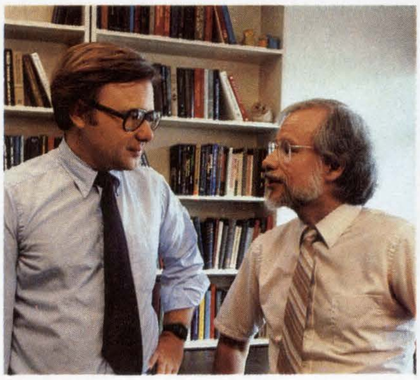
Data memory is supplied by 288 bytes of random-access memory. Enough to hold the data needed to perform a 64-point complex fast Fourier transform (FFT) while maintaining system-linkage variables and constants for other functions.

◀ **Low-cost digital signal processor,** TI's TMS320 is the inexpensive, single-chip alternative to multichip bit-slice systems and custom VLSI devices now used to process signals digitally. TMS320 speed and economy will open unlimited design opportunities for DSP such as the portable telecommunications circuit tester shown here conceptually.

27-4960

economy. 200-ns cycle. TI's new processor makes DSP practical.

Digital Signal Processing: Coming of Age



Highlights from a discussion with Thomas W. Parks and G. Sidney Burris, Professors, Department of Electrical Engineering, Rice University.

Q. In your opinion, why has digital signal processing rather suddenly become practical and economical?

A. Well, digital signal processing has been possible for some years. We've had computers and bit-slice approaches that could do the job, but these were cumbersome, expensive, and consumed lots of power. One major factor accelerating the implementation of digital signal processing is the onward thrust of the electronic components industry.

The continued development of VLSI devices, by packing more and more circuitry on chip, has shrunk processor size dramatically. Throughput rates and architectures have also been improved enormously so that complex algorithms can be computed with incredible speed and reduced power consumption.

Of course, the development of these extremely efficient algorithms has contributed greatly to wider use.

Q. What do you consider the most outstanding advantages of DSP?

A. Digital signal processing provides the flexibility, precision, and speed required to execute increasingly sophisticated signal processing.

For example, spectrum analysis is frequently integral to signal processing, but for years there were no efficient, high-resolution methods to implement it. Now that VLSI digital signal processors can speed through the fast Fourier transform algorithm, such analyses are greatly simplified at a feasible cost.

Digital processing eliminates most voltage, temperature, drift, and noise problems associated with analog techniques. Digital filters can reliably meet tough specifications on magnitude and phase that would be difficult, or impossible, for analog filters to meet.

Q. What new applications do you see for DSP in the near future?

A. We are seeing digital technology applied to signal processing in image, seismic, and speech processing as well as in telecommunications, instrumentation, and high-speed control. In the near term—say, five to ten years—it is probable that we'll see digital signal processors becoming ubiquitous in the home, office, and factory. ■

Full development support

In-depth support for the TMS320 consists of a host-independent development system, as well as software that can be run on a variety of host computers. An evaluation module, macro assembler/linker, simulator, and full in-circuit emulation are now available.

Choice of three

The TMS320M10 microcomputer is designed for applications where up to 3K bytes of program memory are mask-programmed into the read-only memory (ROM), expandable with up to eight kilobytes of total program memory (5K bytes off chip at full speed).

The TMS32010, a microprocessor without on-chip ROM, addresses up to 8K bytes of off-chip program memory at full speed.

A military version, SMJ32010JDL, is available processed to the requirements of MIL-STD-883B.

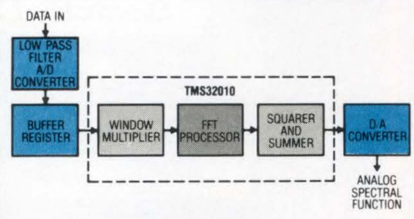
With full-speed memory expansion capability, the TMS320 DSP family can be used in many other applications. ■

TMS320 processors excel at realtime applications.

Because of their high-speed numeric capability, the new TMS320 processors can be used for realtime computations in many applications: Telecommunications. Instrumentation. Voice recognition and synthesis. Image processing. High-speed process control.

The TMS320 family can handle all the signal processing for spectrum analysis: Autocorrelation, windowing, and FFT—performing a 64-complex point FFT in only 580 µs!

Image enhancement, pattern recognition, and data compression are all possible with TMS320 processors. They can extract features, then perform a template comparison to achieve optical character recognition.



New TMS32010 simplifies spectrum analysis

The efficient TMS320 devices can also be used to build high-speed modems having rates up to 9600 baud.

For more information on the new TMS320 Digital Signal Processor, contact your nearest TI sales office or write Texas Instruments Incorporated, Dept. SPR023OS, P.O. Box 401560, Dallas, TX 75240.

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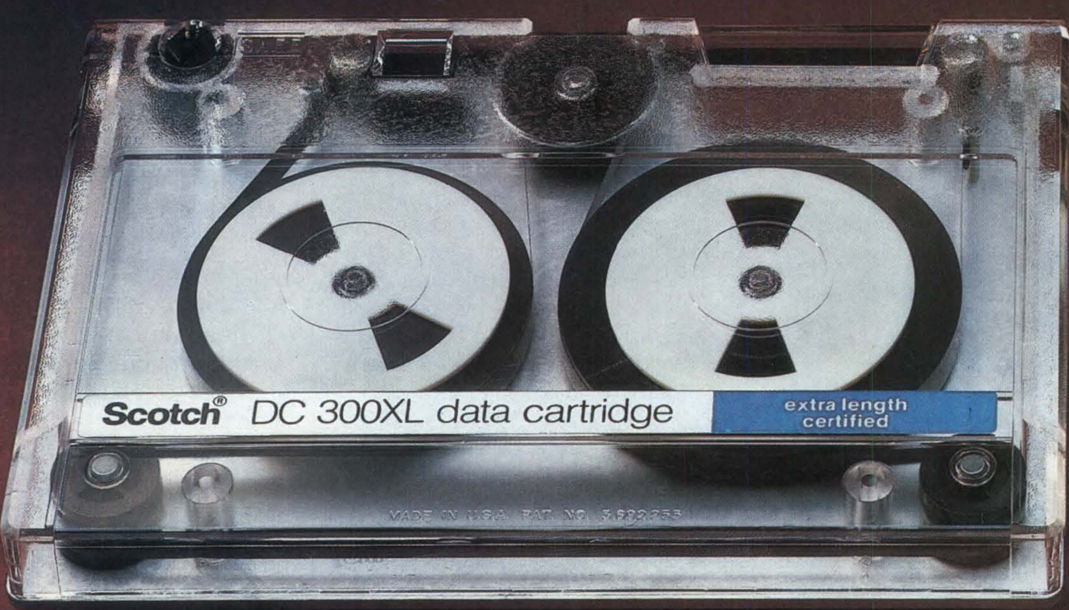

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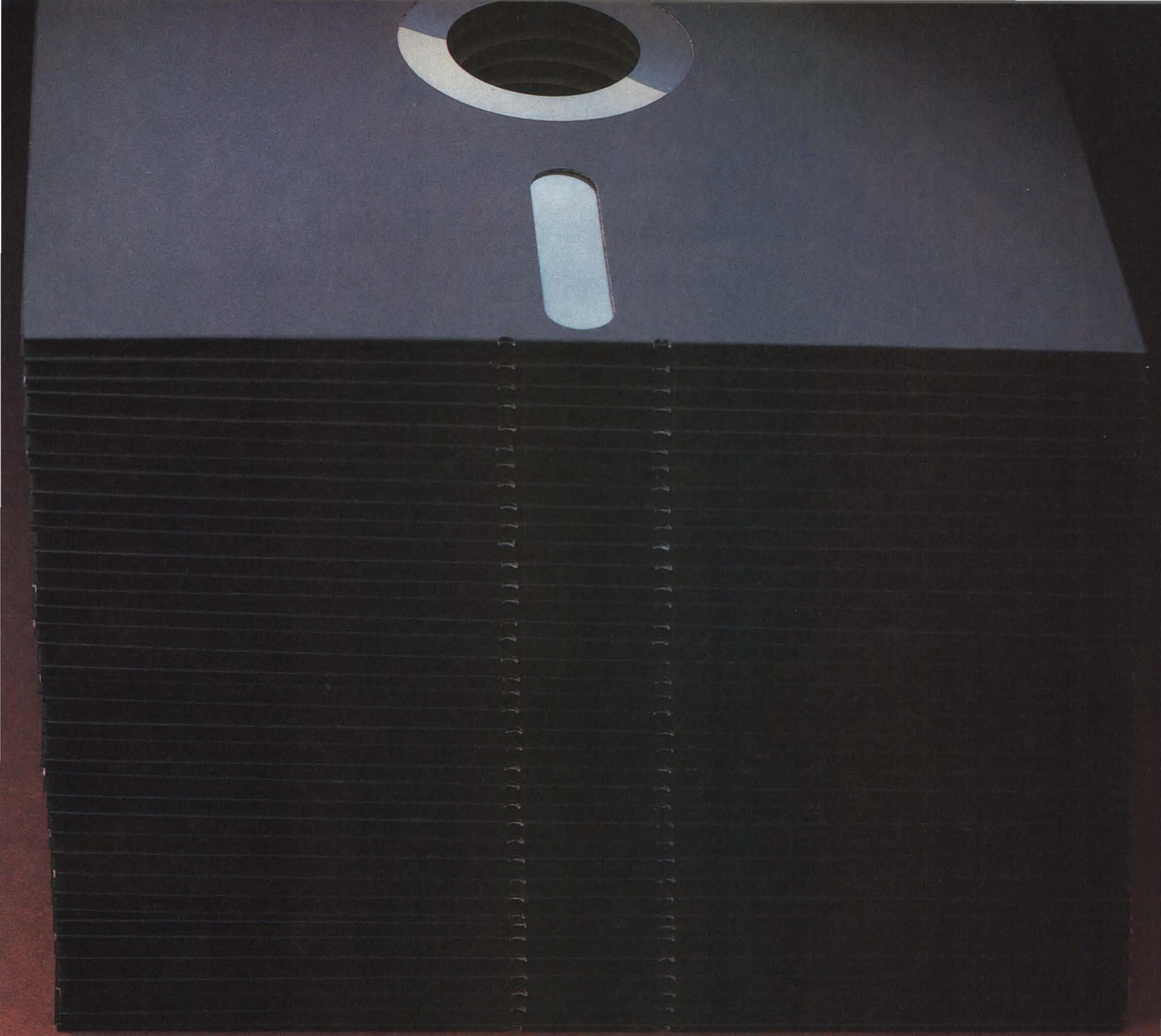

back-up that eliminates stack-up.

This means concerns about compatibility are diminishing.

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The ¼" data cartridge is the logical choice for designers specifying back-up systems for Winchester drives. It's small, reliable, easy to handle and transport, and has a very low cost per megabyte.

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For more information:

For more information on how 3M ¼" data cartridges can save your customers time, space, and money, write to Chris Binner, National Sales Manager—OEM Market, Data Recording Products Division, Building 223-5N, 3M Center, St. Paul, MN 55144.

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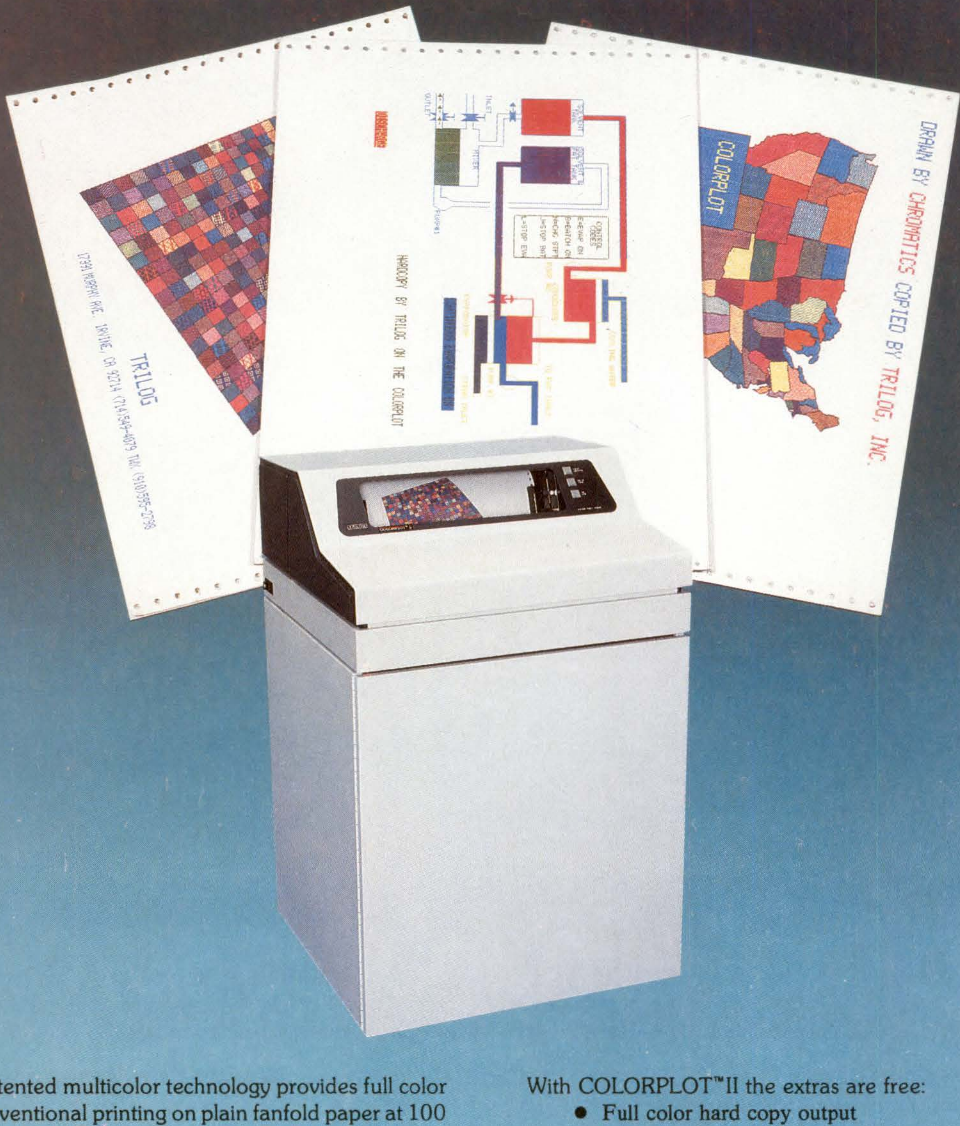

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CIRCLE 108

DATA SCROLLING COMBINES TECHNIQUES

Combining CRT-type softcopy graphics with stripchart recording, data scrolling is a flexible, interactive method for displaying graphics data.

by Tom Ryan

Applying softcopy graphics to stripchart recording techniques yields data scrolling, a powerful tool for monitoring and analyzing data in real time. By definition, softcopy graphics use a volatile device, usually a CRT display, to illustrate and update graphical information. Particularly suited for use in interactive computer graphics systems, data scrolling is a highly flexible analysis tool. For example, a data scrolling system can be designed to scroll several traces onscreen at one time. It can independently control the speed and direction of the traces and provide a hardcopy "snapshot" of scrolling data.

A data scrolling display system consists of three parts: a processor, I/O, and a CRT display module. The configuration of these three can vary anywhere from a high power, multitasking computer with high speed I/O and dumb display to a relatively low power processor with lower speed I/O and an ultra-intelligent display. In the first case, a multitasking computer is needed if it is to perform functions other than updating the display. This is because a dumb display must be constantly updated by the computer. A high speed I/O is needed if the information is to be displayed in real time because it must be refreshed constantly by the computer. In the last case, the ultra-intelligent display reduces the number of I/O transfers, but substantially increases the display's price. This also dedicates the computer to one function—running the display.

A configuration somewhere in between is the best compromise, with a low to medium speed I/O such as the IEEE 488 and an intelligent display unit such as the HP 1347A. Such a configuration offers several benefits. The 1347A contains firmware that provides data scrolling of up to 32 traces, hardcopy output, and an HP-IB (IEEE 488) interface. It also has an internal refresh memory that significantly lowers the number of I/O transfers. So, while it is a softcopy graphics display with built-in scrolling, it can also provide a hardcopy snapshot of scrolling data when used with a plotter.

With such a system, the user can scroll through and visually inspect large amounts of data, and then make a hardcopy record of a specific area at the push of a front-panel button or with a simple program instruction. This provides some of the best features of both hardcopy and softcopy scrolling devices. The 1347A display can also be used with larger mainframe computers as an external peripheral if the system requires mainframe capabilities.

Make versus buy

After a company decides to incorporate a data scrolling device into a system, there is the inevitable question of whether to buy or build. If the company chooses to buy, there are few displays that provide softcopy data scrolling capabilities except for the 1347A. Many applications require that the data scrolling device interface with analog signals. This tends to leave digitally interfaced devices out of the running unless designers are willing to build an A-D converter.

If the decision is made to build, other questions arise. For example, it is necessary to decide if the

Tom Ryan is a product marketing engineer at Hewlett-Packard, 1900 Garden of the Gods Rd, Colorado Springs, CO 80907, where he is responsible for the 1630 A-D logic analyzers. Mr Ryan holds a BS in electrical engineering and computer science from Colorado State University.

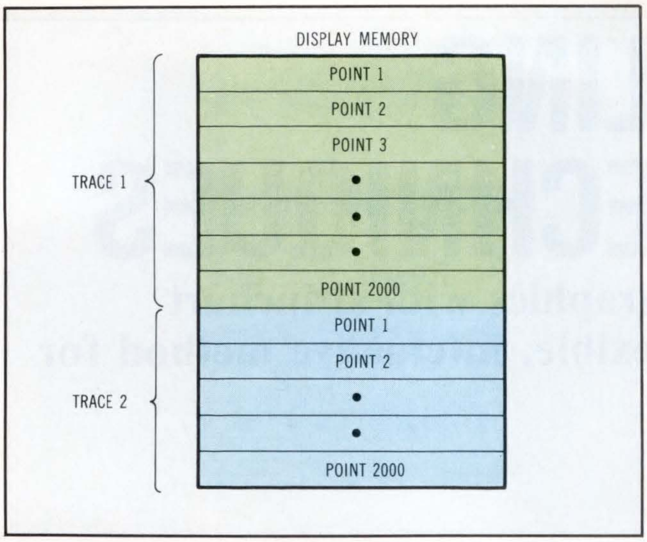

Fig 1 Display memory is segmented. Each segment contains a different trace represented by an array of contiguous locations, each containing the deviation from the baseline.

system should be hardware or software/firmware based, how many capabilities will be needed, how much time it will take to do the design, and if the expertise is available to design the system in the first place. The following are some of the capabilities a softcopy scrolling system should provide. First, it should provide the number of traces (eg, to consider how many data traces must be displayed and if more will ever be needed). If so, the software should allow programmatic changes in the number of traces. Second, in a software system, the number of points per trace is important because it tells the computer how much memory to allocate for each trace. A default parameter could be used, but it may be larger or smaller than what is really needed. Specifying the number of points allows the system to allocate only as much memory as is needed to contain each trace.

The delta increment is another important capability. This parameter determines the size of the display window in memory. It is not a zoom function, but is rather an expansion of one axis. In other words, the traces can be stretched out to show detail. This function does not add resolution; in fact, it can decrease it. For example, if there are 500 data points in memory for a given trace, and the addressable resolution of the display is 2000, each location in memory will be 4 display units long. If the trace contains 2000 points, the contents of each memory location will map onto exactly one display point. Hence, the system can display no more detail than is in the data list.

Other valuable capabilities include offset, start/stop position, and the scale factor. By adding an offset, the programmer can position the traces anywhere onscreen. This parameter is added to the incoming data to shift it a certain number of units above the bottom (or side if the data is scrolled vertically) on the screen. The start/stop position allows the programmer to specify the width of the display onscreen. This is essentially an onscreen view port when used with an offset. Moreover, the scale factor multiplies all incoming data before adding the offset.

A look at software techniques

From a software point of view, there are several ways to scroll data. These examples assume the use of a random vector display because most raster systems are hardware intensive. The first method involves memory segmentation. Memory in this and the following example is represented as a single-dimension array of contiguous locations.

Each location contains the Y deviation from the baseline of the data trace, assuming horizontal scrolling. The X parameters are not stored here to save memory but are incremented from a separate register. Given three data traces, each is stored in a separate memory segment as shown in Fig 1. As the memory is run through sequentially, each trace is drawn until all traces are onscreen. The data can be scrolled in either direction by moving pointers indicating the beginning and end of the display window in memory (WINDOW_START and WINDOW_END, respectively). Fig 2 is a simplified diagram of such a configuration with display windows on each of the memory segments. This allows a different display window to be applied to each data trace.

This method has several advantages. First, the data traces are independent of each other and can be made to scroll at different rates or even directions. Second, it simplifies labeling, especially when the labels and/or graticules must scroll with

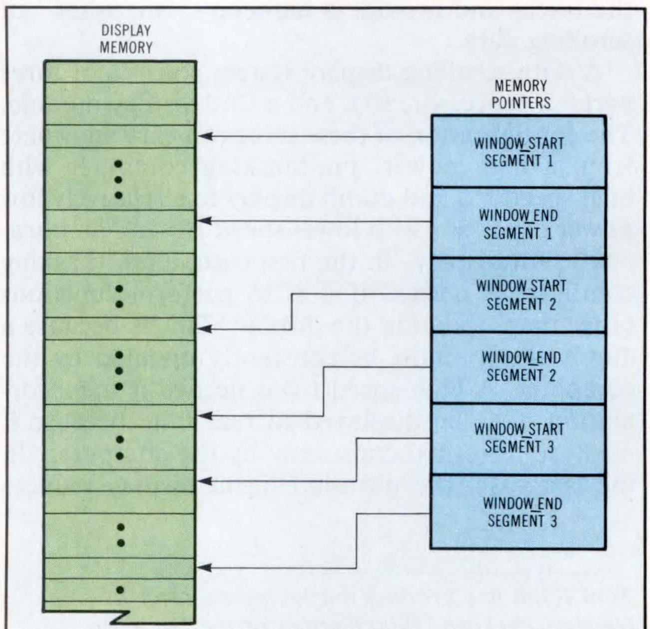

Fig 2 Moving pointers show the beginning and end of the display window in memory, allowing data to be scrolled in either direction.

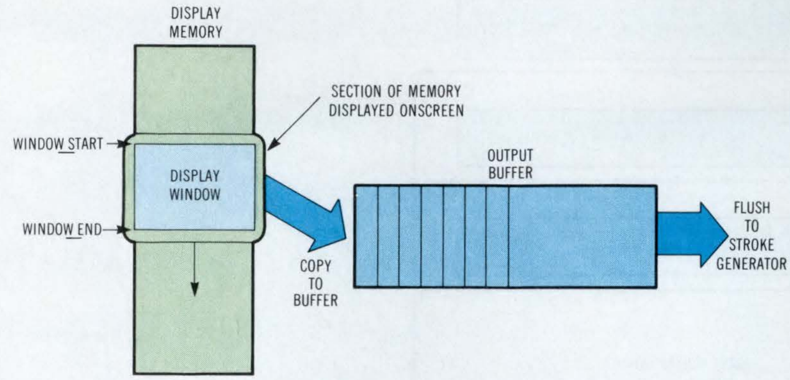

Fig 3 The buffer-dump scrolling method pushes new data from memory into one end of the buffer, forcing the oldest data out the opposite end.

the data. This is particularly important in data logging applications that use the display as a softcopy stripchart recorder. Third, it conserves memory fairly well. It is necessary to maintain a few registers to keep track of window start and end points, delta X increments, and other trace parameters. If each trace has 15 characteristics and 32 traces, only 480 locations are needed, assuming that each memory location is 16 bits wide and the screen resolution is in the range of 0 to 2047. This method is used in the 1347A.

A second method is one that could be called "buffer-dump." The programmer builds a buffer that holds a copy of the trace in memory, as shown in Fig 3. Depending on the direction that the trace is scrolling, a shift right 1 or shift left 1 operation is then done to the buffer to eliminate the oldest data point while the new data point is pushed into the other end of the buffer. The buffer size does not change—data is simply shifted out one end and pushed in the other in a first in, first out (FIFO) manner. The buffer's contents are then flushed out to the display. The data in memory is unaffected because the buffer contains only a copy of the data. Moreover, if the system is used in a data monitoring application where there is a need to look at the data already shifted out (assuming that the data is stored elsewhere for later retrieval), the memory is not needed.

Two drawbacks of this method are the amount of memory used for the buffer and the need to dynamically reallocate the buffer size. If the screen resolution is 1000 points, the buffer would also have to be 1000 locations long to produce a trace as wide as the screen. This is already more than twice the size of the required memory space for the memory segmentation method. If the system is to be committed to firmware, this amount of memory overhead could be a problem. In addition, if the programmer wants to change the size of the trace onscreen, the buffer size should be reallocated. Many operating systems do not allow the buffer size to be changed dynamically, leaving the system with a section of memory that is never used, and yet cannot be freed for other purposes.

Surveying hardware techniques

Data scrolling with hardware presents some interesting difficulties. For a raster display, a typical architecture is shown in Fig 4. An A-D converter for each data channel (S1 to S3) changes the analog signal to digital information, which is stored in the trace registers. Each string of trace registers contains one register for each data point. The information is clocked into the registers from the A-D converter on the positive edge of the clock, and the information from the registers is clocked into a set of latches on the following falling edge of the clock. The information from the latches is sent to a frame buffer, which is in turn sent to a video generator. There, it is converted into a raster picture.

Although the above example is basic, it points out several interesting problems. First, for the system to work in real time, the registers, latches, and frame buffer must be very fast, which probably means an ECL architecture must be used. Second, after they are defined in hardware, more traces can be added only by adding more hardware. The more traces added, the slower the system becomes because each string of trace registers must be serially accessed.

Hardcopy data scrolling, or stripchart recording as it is more commonly known, is popular in applications that demand permanent records of data. It has many shortcomings, however. If a graticule is desired, the user is tied to linear, log-log, or semilog types that are available on stripchart paper. User-defined graticules are not possible with stripchart recording. Also, data must be labeled by hand after it is recorded because a stripchart recorder cannot generate text. Using text labeling and graticules that are not available on paper is

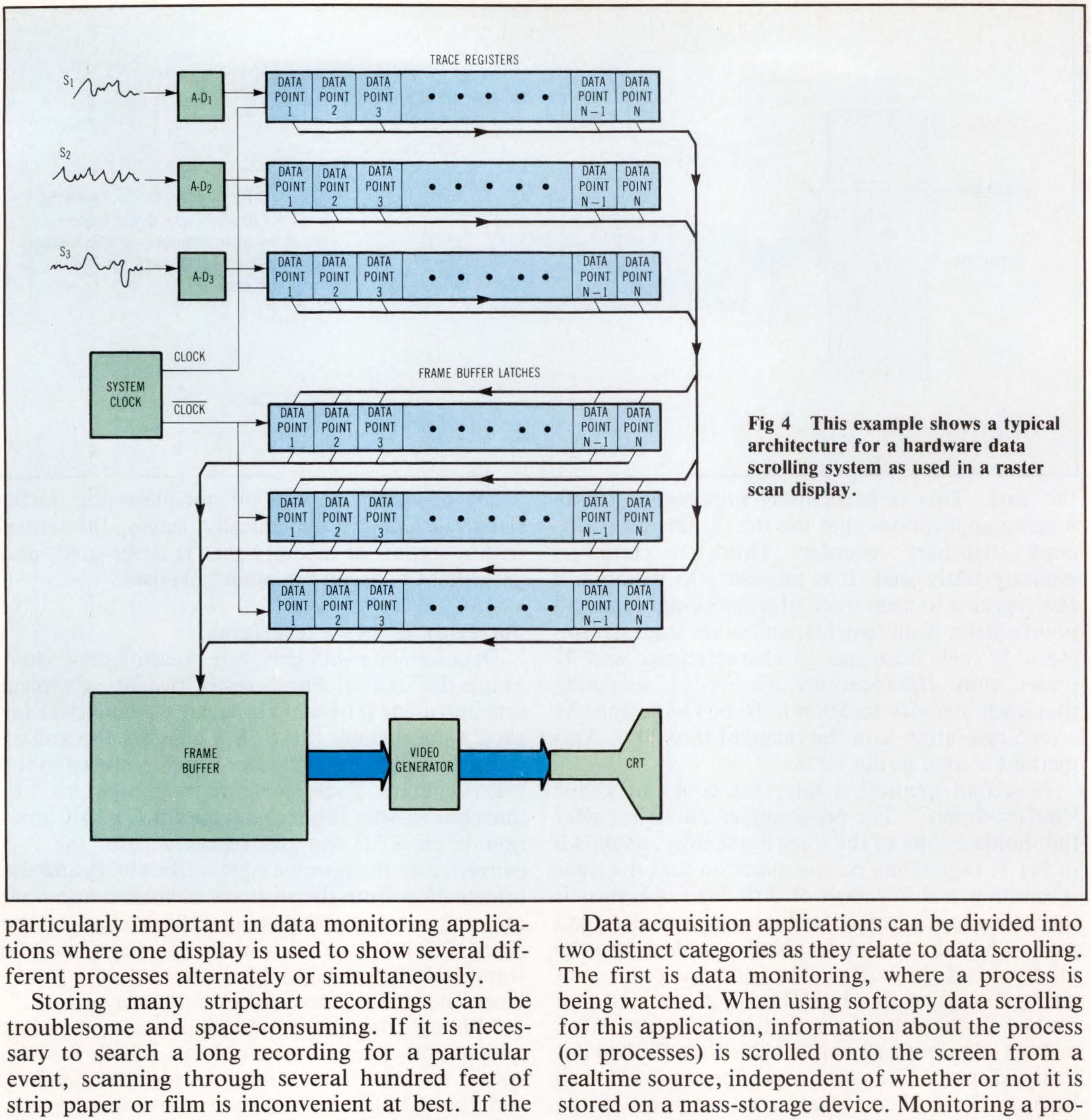

Fig 4 This example shows a typical architecture for a hardware data scrolling system as used in a raster scan display.

particularly important in data monitoring applications where one display is used to show several different processes alternately or simultaneously.

Storing many stripchart recordings can be troublesome and space-consuming. If it is necessary to search a long recording for a particular event, scanning through several hundred feet of strip paper or film is inconvenient at best. If the data must be processed after it is gathered (eg, compressing the horizontal axis to display long-term trends, or smoothing curves to remove unimportant excursions), the data must be plotted again. This can be very time-consuming. Finally, an operator can easily monitor a CRT from a comfortable distance in a variety of ambient lights.

On the other hand, although stripchart recorders are not usually the most convenient media for displaying data, the software needed to run them is minimal. Most softcopy data scrolling systems require substantial software. For example, data logging systems that use hardcopy devices, such as film recorders, are analog. To implement softcopy data scrolling into the system requires a high speed A-D converter that puts the data into a usable form for a computer.

Data acquisition applications can be divided into two distinct categories as they relate to data scrolling. The first is data monitoring, where a process is being watched. When using softcopy data scrolling for this application, information about the process (or processes) is scrolled onto the screen from a realtime source, independent of whether or not it is stored on a mass-storage device. Monitoring a process with data scrolling is particularly useful in industrial applications where an operator must make decisions based on an ongoing graphical presentation.

The second category involves analyzing data that has been gathered and stored on disk or some other medium, and is to be reviewed or evaluated. With softcopy data scrolling, the display's memory can be filled with data and scrolled through bidirectionally to find events of interest.

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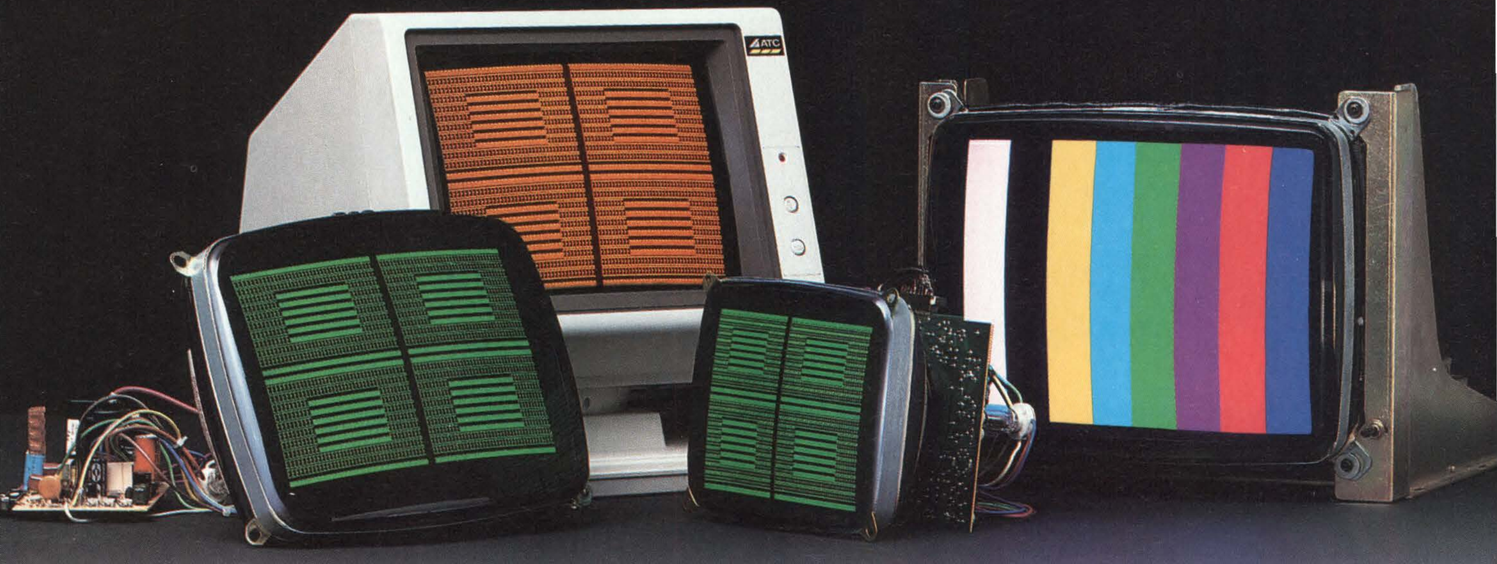

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CIRCLE 109


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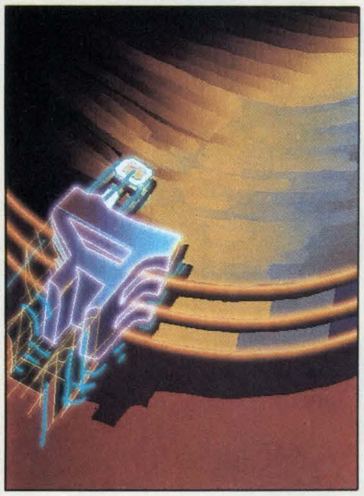

Special report on disk memory

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CIRCLE 112

SPECIAL REPORT ON

DISK MEMORY

The potent combination of fast access, small size, and rising capacity bestowed by Winchester disk drives matches today's storage demands. More tracks to the inch, more bits per track, and greater capacity in each box mark the trend in hard disk drives destined to supply online storage to increasingly powerful processors.

While 16-bit processors and 64-Kbit RAMs are just now hitting their stride, 32-bit microprocessors and 256-Kbit RAMs loom on the horizon. Given the data storage demands made by current systems, the oncoming giants portend dramatic increases over the next several years. The 32-bit microprocessors, running increasingly complex programs, will demand faster access to continuously expanding amounts of data. And, since large disk drives do not fit neatly on a desktop or even below a desk, the current preoccupation with footprint shows no sign of abating. Indeed, the "smaller is better" mania is destined to spread.

Ongoing development efforts centering on vertical recording techniques and vertical media, as well as optical storage devices, will ultimately fill massive future storage demands. However, less esoteric means will suffice over the near term. Thus, minicomputer/microcomputer disk technology aims at low cost, small size, and manufacturability. To achieve these goals, drives are adopting media, actuator techniques, and magnetic heads already proven in larger drives. Such evolutionary changes accommodate steadily shrinking form factors as we await the revolutionary changes promised by vertical and optical techniques.

Riding the crest of the wave generated by microcomputer mania, the stars in the Winchester race are currently those with a 5¼-in. form factor. Whether single disk 5-Mbyte units or multiple platter models capable of packing in 300 Mbytes, these units fill identified data storage demands. The units fall into two groups. One uses conservative technology to provide low capacity, low performance drives. The other group aims at perceived high capacity, high performance system needs by adopting far more innovative techniques.

Those who push technology in search of higher capacities, however, are faced with limiting factors. To overcome one hurdle, a concerted effort has been launched to gain acceptance for an interface capable of handling the increased data rates that come with incremental increases in bit density.

Articles in this special report focus on interfaces vying for acceptance and on factors relating to the media that will result in further increases in density. The task of matching drives to the application at hand can be resolved by techniques that determine whether a drive performs to its published specs.

Peg Killmon
Senior Editor

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AMS 571—our largest, fastest disk memory—is loaded with value. New thin film heads and oxide media put 590 megabytes into a very compact, very economical package. To enhance system performance we've increased the data transfer rate to 1.98 megabytes per second while reducing the average head positioning time to 19 milliseconds. All for OEMs. And all at a very competitive price!

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CIRCLE 113

HARD DISKS BOOST CAPACITY WHILE SHRINKING SIZE

Keeping pace with rapacious appetites for data storage displayed by computers of every size, rigid disk drives continue to whittle off the inches while driving capacities up and access times down.

by Peg Killmon, Senior Editor

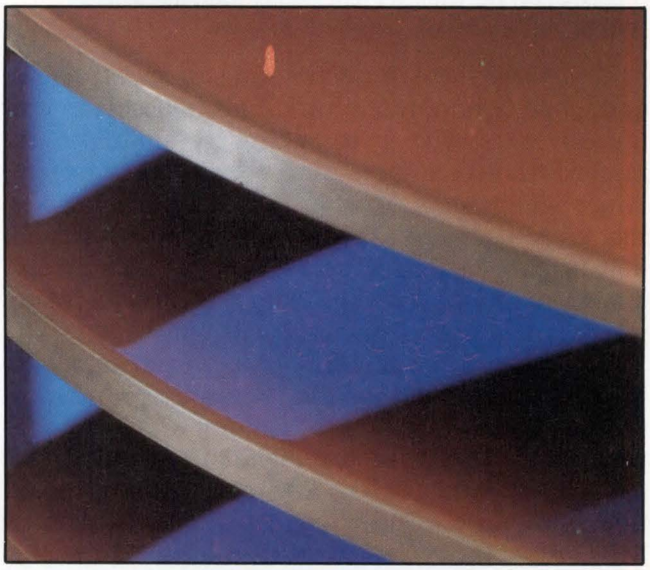
Rigid disk subsystems are essential elements of computers. As computer systems have spread into virtually every conceivable application, their demands for vast amounts of storage are growing simultaneously. Disk drives, in response to this challenge, are packing more and more bits into every square inch possible.

Currently available technology crams as much as 6 Mbits of data into a single square inch of plated thin-film media using thin-film recording heads. Drives of the future promise to increase this by a factor of 10. Still further ahead lie the massive stores possible when vertical and magneto-optical recording techniques are finally realized.

Drives destined to supply the voracious appetites of mainframe systems will struggle to achieve gigabit capacities through such esoteric technology. However, the swelling numbers of minicomputers and microcomputers present less rigorous demands. These needs can be met by compact rigid drives that adopt time-proven methods to drive capacities up and access times down.

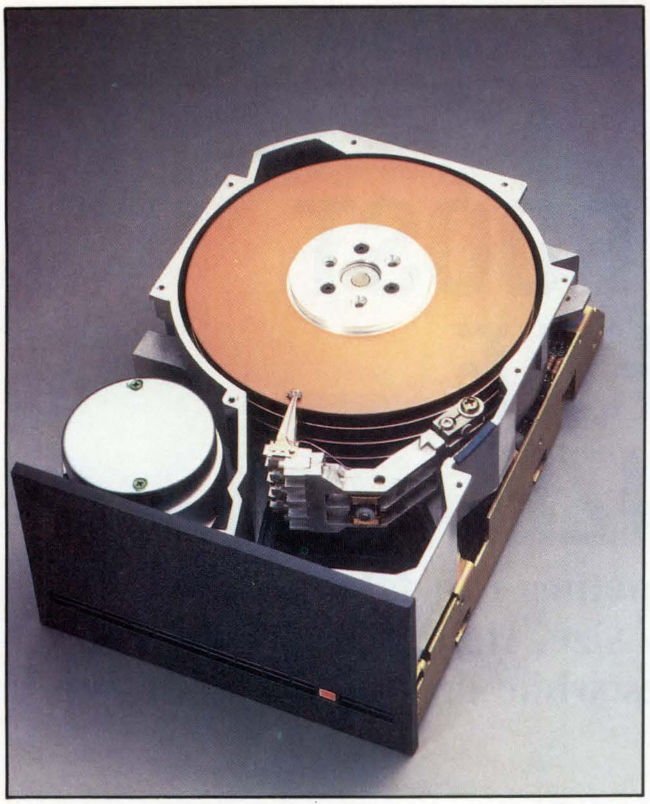
In the current spotlight

Rapidly outgrowing the storage capability of the 5¼-in. flexible disks that initially served data storage needs, personal computers provided the spur to development of Winchester disks having the same



form factor. Similarly, the adoption of multitasking operating systems on these same systems has propelled the drives to increase capacity and supply faster access to data.

Today's rotating storage units have taken Winchester technology far beyond its origins. While newer technologies move in to replace Winchester methods in the 14-in. drives, less rigorous storage demands are being met by more compact rigid disk drives. These drives combine techniques derived from large Winchester drives with those on which cheaper floppy disk drives are based. Ranging in capacity from 5 to above 300 Mbytes, they provide a range of access times from 18 to close to 100 ms.



An 80-Mbyte capacity, 5¼-in. drive, Computer Memories' CM7880 writes data on four platters. The ability to pack platters into the compact unit results from mechanical design and use of 3370-type head flexures.

To achieve these distinctions in storage capacities and, equally important, variations in access times, the drives use diverse technologies—some proven in flexible disk drives, others scaled down from larger Winchesters. Most in demand, 5¼-in. drives that store under 30 Mbytes come in both full- and half-height versions. The rash of recent startups aiming at the 5¼-in. half-height market plans to use a variety of techniques to cut unit height.

Positioned in the low end, units storing under 20 Mbytes from vendors like Seagate Technology (Scotts Valley, Calif) and Tandon Corp (Chatsworth, Calif) are most in demand. These units, also supplied by Miniscribe (Longmont, Colo), International Memories (Cupertino, Calif), and Computer Memories Inc (Chatsworth, Calif), face the challenge of oncoming 3½-in. drives already introduced by Rodime PLC (Mission Viejo, Calif), Control Data Corp (Minneapolis, Minn), Syquest Technology (Fremont, Calif), and Microcomputer Memories Inc (Van Nuys, Calif). Other challenges in the form of half-height 5¼-in. units come from startups that include Cogito Systems (San Jose, Calif), Microscience International Corp (Mountain View, Calif) and Tulin Corp (San Jose, Calif).

Supplying midrange drives between 20 and 50 Mbytes, Rodime, Miniscribe, and International Memories have used performance and price competitively to form a solid base. With capacities in this range, some aim to provide high performance while others meet low cost needs by settling for less than optimum access times.

On the high end lie high capacity, high performance drives such as those from Atasi Corp (San Jose, Calif), Maxtor (San Jose, Calif), and Vertex Peripherals (San Jose, Calif). Joining these are Control Data Corp, Micropolis (Chatsworth, Calif), and Priam (San Jose, Calif). Competitive with 14- and 8-in. drives in capacity, these units propose to fill the storage needs anticipated when multitasking operating systems take over the microcomputer world by also taking care to supply fast access to data.

While IBM's (White Plains, NY) choice of a 10-Mbyte hard disk drive for use in the PC/XT has fueled growth in the low end, midrange devices should soon share the wealth. Rumors that IBM is seeking 20-Mbyte (and up) drives for its next additions to the PC family are stimulating a push to enter the 20- to 50-Mbyte capacity area. Drives of 50 Mbytes and up are proving their viability in multitasking, multi-user systems. Demand should grow as more sophisticated operating systems invade the microcomputer world.

A drive for every storage need

Among the technologies that made 5¼-in. drives possible in the first place, there are those that contribute to high performance, and others that minimize cost and enhance manufacturability. Low end drives that strive to minimize cost have typically used floppy techniques to produce rigid drives. Their use virtually ensures that products will be manufacturable—a key issue—while placing constraints on capacity and limiting access speed.

Credited with producing the first hard disk drive to appear in the 5¼-in. form factor, Seagate maintains its leadership in the 10- to 30-Mbyte capacity range. Its original stepper-driven ST506 has been joined by drives that take capacity from the original 5 up to 25 Mbytes. To make this jump in capacity, Seagate had to switch to a voice-coil actuator in the new design.

Tandon's low end units supply from 6.4 to 19.1 Mbytes using standard oxide disks and stepper motor actuators that put access times in the 100-ms range. Other drives providing capacities in this range come from Nippon Peripherals (Kawasaki, Japan), International Memories, Mitsubishi Electronics America (Torrance, Calif), and Shugart Corp (Sunnyvale, Calif).

Key to holding costs at a low level are the use of stepper motor positioning mechanisms and open-loop control circuits. The simplicity of these techniques not only keeps costs low, but supplies a very reliable system. However, the stepper motor's electromechanical nature limits positioning accuracy, thereby limiting the tracks/inch that can be attained on a disk's surface. In open-loop stepper systems, the drive moves the head a fixed predetermined distance from the starting point with each step pulse. This limits the track density, because tracks can only be so close together. Since the track position on the media is affected by media expansion/contraction, movement of internal parts, and wear effects, system positioning accuracy can vary. The stepper positioner also restricts the access time to a range between 50 and 100 ms.

Stepper motor split-band actuator mechanisms allow densities to about 350 tracks/in.—about 10 Mbytes of data storage capacity per surface on a rigid disk. Taken from floppy drives, these positioners are widely used in low end Winchesters. Consisting of an anchored metal band wrapped around a capstan, a stepper motor typically rotates the capstan 1.8 degrees at a time to move the positioner, providing a track-to-track access time of 3 ms.

Used with a rotary positioner, the stepper motor rotates the capstan, moving the arm carrying the head in an arc over the radius of the disk's surface. Since rotary motion is maintained, this system achieves high shock resistance. Linear positioning systems convert the rotary motion of the stepper motor into a linear motion at the head. The head positioning mechanism moves straight in and out on a radius over the disk's surface.

To combat the resonance problems of rotary mechanisms with a cantilevered arm, a balanced rotary technique has been used. This third alternative shortens the length of the actuator arm, reducing the effects of resonance as well as the amount of power needed to position the arm.

Another form of positioner for an open-loop system consists of a rack and pinion mechanism. Here, the stepper motor drives a toothed pinion (bar) on a toothed rack to convert rotary to linear motion. Heads move across the disk's surface on the radius. This method provides access times equivalent to those of the split-band positioner with a cheaper to manufacture mechanism.

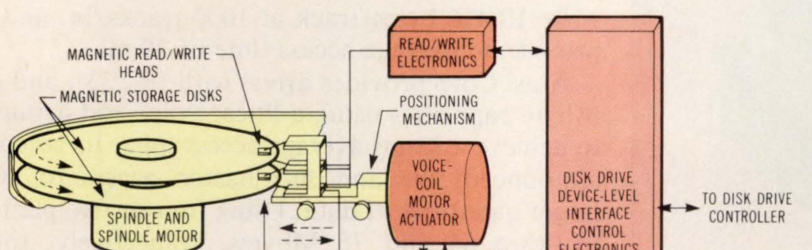
While the stepper motor mechanism limits access times to the 90-ms range, when it relies on step pulses provided by the drive controller, an onboard microprocessor can improve this. The drive controller issues individual step pulses to move the rotor one position at a time. Using a microprocessor and a buffered seek technique, such as that in series 5000 drives from Computer Memories or Miniscribe's V series, these pulses can be stored and transmitted to the drive as a burst of pulses. Now, rather than stop after each pulse, the rotor can move continuously. This results in step rates of 0.6 ms/step rather than 3 ms.

Half-height units in this capacity range have stirred the fancy of manufacturers who, cramped for space, need to incorporate backup units in their systems. Targeted to meet those needs, International Memories supplies 6.4 and 12.8 Mbytes in its half-height 2000 series drives. Traditional stepper motor technology achieves an 85-ms average access time. Shugart, mastering this technology while manufacturing floppy disks, is producing half-height 6.4- (SA/706) and 12.8-Mbyte (SA/712) Winchesters that fill growing demands of single-user systems for drives of this type.

Computer Memories supplies 6- and 12-Mbyte capacities with its half-height series 3000 drives. These drives record on a single platter using a twin head design. The swing arm actuator, powered by a stepping motor, achieves 690 tracks/in. and 9275 bits/in. using embedded track zero sensing.

Cogito Systems Corp aims at power-sensitive applications such as those of portable computers. Its stepper driven half-height consumes just 12 W. With 85-ms access times and capacities of 5 and 10 Mbytes, Cogitator series 1 drives incorporate a spindle lock that rapidly stops disk rotation when power is turned off. The drives are shock-mounted for extra protection.

Portable computers' needs for ruggedness were also considered by Microscience International



In a typical closed-loop voice-coil servo system for a rigid disk drive, the type of positioning mechanism may vary, but most elements are similar from drive to drive.

Corp in designing the HH-612. This half-height 12.8-Mbyte drive uses plated media for durability and has been tested to withstand shock to 10 G and vibration between 5 and 60 Hz.

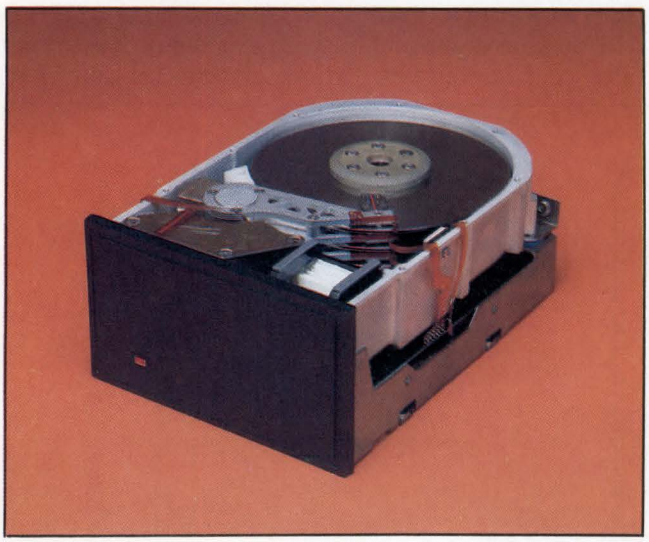
Closing the loop

To take capacities into the midrange (20 to 50 Mbytes/surface), manufacturers have used closed-loop positioning systems with stepper motors. Ampex Corp (El Segundo, Calif) uses conventional steppers with servo temperature compensation in its Pyxis series. These drives handle capacities from 7 to 27 Mbytes with a 90-ms access time. When used with steppers capable of microstepping—making steps in 0.9 degree or smaller increments—servo systems promise other benefits.

Another newcomer, Tulin Corp features a design that drives a rotary actuator by a microstepping motor that reads positioning data from a single servo sector. This drive promises to supply 13-Mbyte capacities in a half-height form factor.

Closed-loop positioning improves on the accuracy of open-loop systems by feeding positioning information back from the heads to servo circuits. This compensates for the effects of thermal expansion and contraction, movement of internal parts, and effects of wear. By allowing the head position to be corrected as needed, it provides greater placement accuracy. In the series 5600, International Memories uses this technique to write at a track density of 606 tracks/in. and access in 49 ms. Moreover, Mitsubishi Electronics America writes at 690 tracks/in. in its MR521.

Closed-loop systems differ in the type of servo system used. A dedicated servo system requires that one recording surface store only positioning data and that one head be reserved to read this data. This method allows continuous monitoring of track position and continuous correction for head drifts. While it is possible to attain track densities of more than 1000 tracks/in.—three times that of open-loop systems—one surface is unavailable for storage.



Tandon's TM705 uses standard Winchester heads with plated media to store 50 Mbytes on three platters. Track density of 1000 tracks/in. is achieved using a closed-loop servo system with rotary voice coil positioner.

Another widely-used servo system records positioning information between data sectors on every track. This embedded servo system makes positioning information available only intermittently rather than continuously, limiting accuracy and head positioning speed. However, it requires no dedicated disk surface, thus making more space available for data storage. It also allows all heads to be used for data, rather than reserving one to read servo information.

An option sometimes used is an optical servo positioning system. Based on a precision optical scale attached to the head carriage, this system uses no part of the recording surface, yet offers high accuracy. A LED and photocell combination track the location of the head mechanism on the optical scale by counting the number of lines that pass by the light. Quantum Corp (Milpitas, Calif) uses this technique in its D500 series drives, writing 591 tracks/in. on eight platters to record a total of 42 Mbytes.

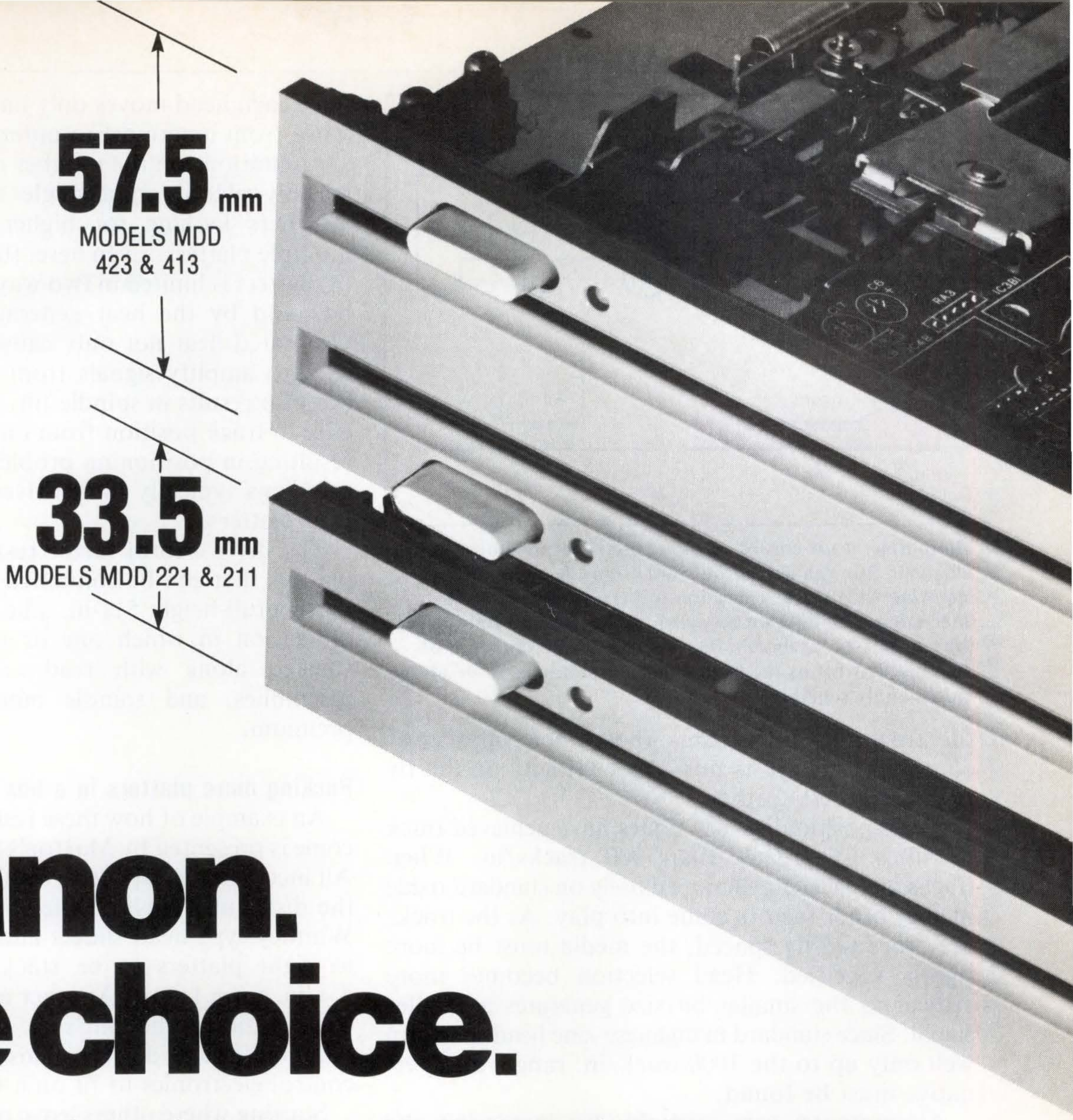
Servo systems, when used with voice-coil actuators, achieve not only higher track densities, but also supply the faster access speeds demanded of high capacity, high performance drives. Activated by one or more magnets, the voice coil moves the head carriage in or out over the disk's surface. Essentially a linear motor, a voice coil positioner is both fast and accurate. Thus, most drives providing capacities of more than 20 Mbytes will use servo systems along with voice-coil actuators.

Speedy access to more data

Using servo systems with voice-coil actuators is the technique that Tandon Corp has chosen to bring its line up to the midrange. Its TM705 provides 50 Mbytes on three platters. The closed-loop rotary voice coil actuator uses a dedicated servo system to write 10,416 bytes/track at 1000 tracks/in. and to provide an average access time of 39 ms.

Atasi Corp provides drives with 19-, 33-, and 46-Mbyte capacities using a linear voice-coil actuator to achieve a 33-ms average access time. Its recently announced 3065 and 3075 hasten access to even larger quantities of data. Using four or five platters to store 64 and 75 Mbytes, respectively, these drives achieve an average access time of 24 ms, using a closed-loop embedded servo that writes at 9490 bits/in. on 980 tracks/in.

Using a proprietary Faseek actuator control system, Micropolis records from 42.6 to 85.2 Mbytes, writing 9824 bits/in. at a 1000-track/in. density. These drives manage a 25-ms average access time by starting positioner movement when they receive



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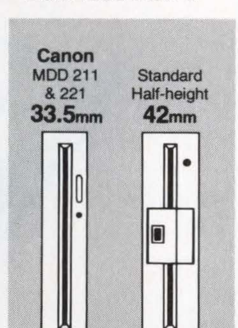

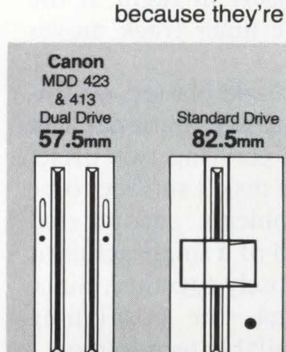

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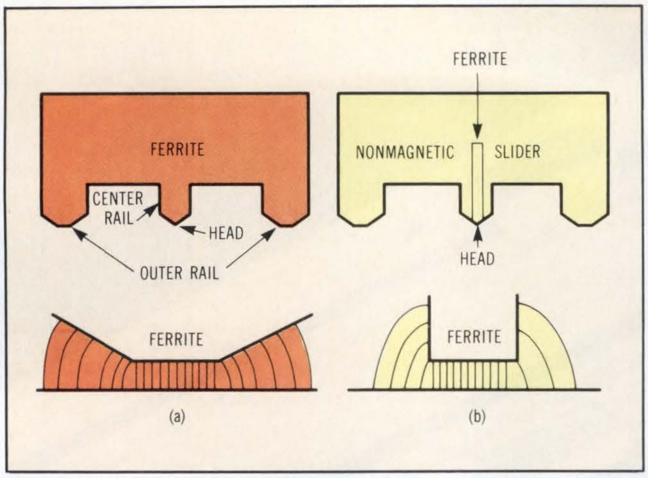


Monolithic heads consist of the entire slider as shown in (a). Magnetic flux can spread outward from the angled walls, requiring wide track separation to keep stray flux from interfering with data on adjacent tracks. Composition heads (b) reduce stray magnetic flux because of the thin core of material that forms the head. This allows tracks to be placed more closely together.

the first step pulse. An onboard microprocessor continuously adjusts positioner velocity on the fly to speed access further.

These positioning techniques have achieved track densities of greater than 900 tracks/in. When tracks are packed any more closely on standard oxide media, other factors come into play. As the tracks are more tightly spaced, the media must be more tightly specified. Head selection becomes more critical as the smaller bit size generates a smaller signal. Since standard manganese-zinc heads perform well only up to the 1000-track/in. range, an alternative must be found.

Attempts to gain capacity by increasing the recording area on a disk surface have not been entirely successful because of the need to maintain a balance between the linear bit density on the innermost and the outermost tracks. Head stability problems have also been encountered in attempts to use this approach. While stable in flight at the speeds provided at the disk's outer perimeter, standard Winchester heads become wobbly in flight at the low speeds encountered as the inner track moves closer to the spindle.

Dual bands of tracks on a single platter, a technique pioneered by Microscience International, can be served by a head assembly carrying two offset heads. This allows more of the disk's surface to be used while avoiding the problems encountered when trying to stretch the reach of a single actuator arm or to pack tracks more closely together. Since tracks retain standard spacing, the positioning mechanism can use readily available technology.

Laying down twin bands of 306 tracks on a single platter, Seagate achieves 65-ms average access time in its ST/212 half height. Two offset heads mounted on the ball-bearing supported carriage each read one of the 306-track bands. This speeds access, since each head moves only half the maximum distance from innermost to outermost track.

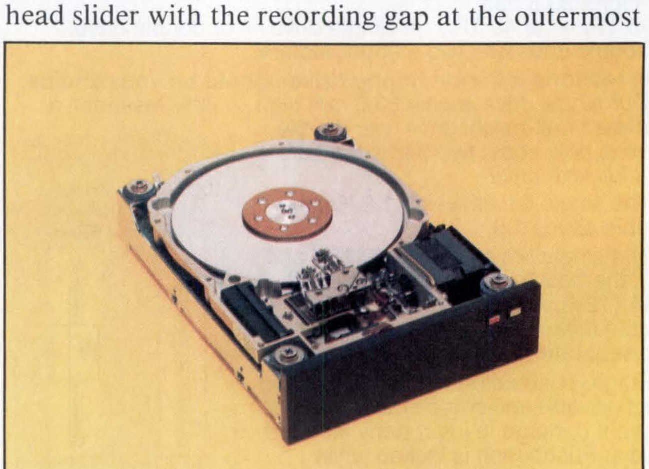
Limitations on the number of tracks that can be feasibly placed on a single surface have forced designers looking for higher capacity to go to multiple platters. Even here, the maximum number of platters is limited in two ways—by the size of the box and by the heat generated within the box. Generated heat not only causes failure of the ICs used to amplify signals from the recording head, but also results in spindle tilt. This causes a difference in track position from one platter to another, resulting in positioning problems. All in all, these problems typically limit drives to a maximum of four platters.

The drive's form factor restricts the number of platters that can be contained within the package. Since a full-height 5¼-in. unit has a 3¼-in. vertical dimension in which one or more disks must be stacked along with read/write heads, carriage assemblies, and spindle motors, space is at a premium.

Packing more platters in a box

An example of how these restrictions can be overcome is presented by Maxtor's 5¼-in. Winchesters. All incorporate a space-saving spindle motor inside the disk hub. This, coupled with the use of small Whitney type head sliders and flexures, allows up to eight platters to be stacked in the standard 5¼-in. form factor. Another contribution to space conservation is the unit's use of miniature surface-mounted circuit devices. This allows all drive and control electronics to fit on a single PC board.

Starting where others leave off, the units demonstrate capacities of 65, 105, and 140 Mbytes on four, six, or eight platters. First of the series, the XT-1000 records at 9875 bits/in. on 918 tracks/surface, and transfers data at 5 Mbytes/s. Increasing the tracks/surface to 1224, the XT-2000 incorporates a two-rail head slider with the recording gap at the outermost



Staggered head arrangement on Microscience's HH612 allows data to be recorded on two narrow bands on the same surface. Each head serves only one band to improve access time without pushing technology.

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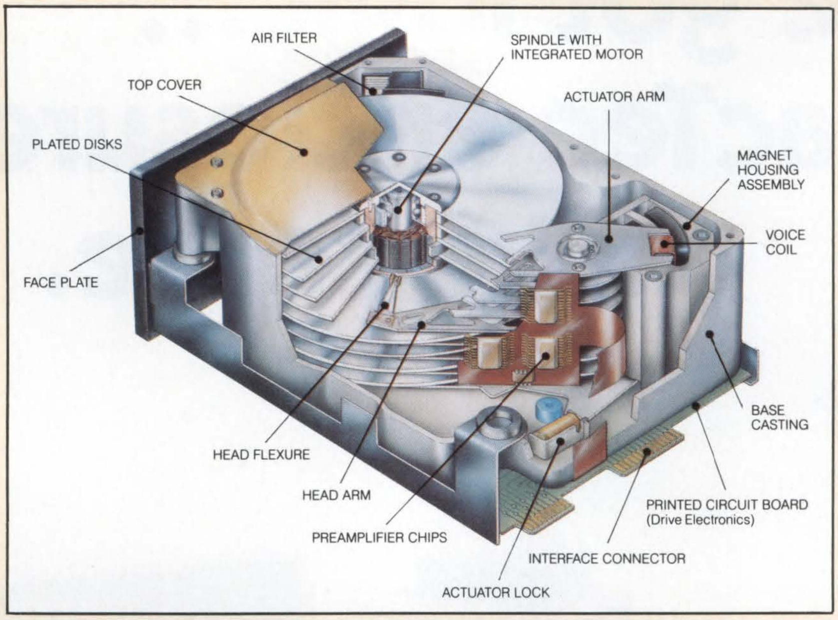


Eight platters can be packaged in standard 5¼-in. form factor when the spindle motor is integrated with the spindle as in Maxtor's XT series drives. Other space saving devices include single electronics board and Whitney type heads and flexures.

edge. This allows a 33-percent increase in storage capacity to be attained while keeping the access time in the under 30-ms range. With capacities of 85, 140, and 190 Mbytes, these drives also transfer at 5 Mbits/s.

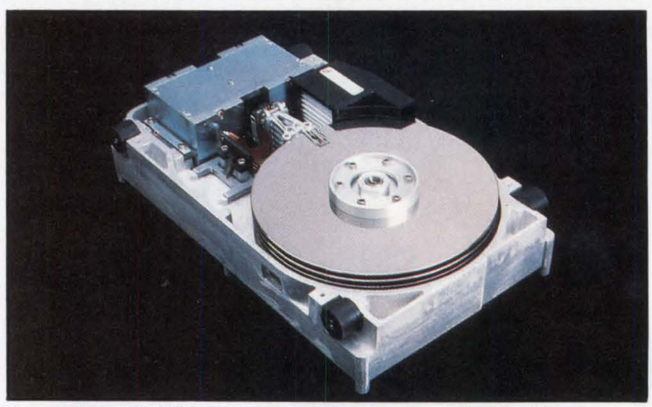
To accomplish the next capacity increase, however, the series EXT-4000 records more bits/in. and changes the encoding scheme. Any increase in bit density requires a different controller design, since as bits/inch increase so does the rate at which data is read from the disk and transferred to the CPU. While more data can be recorded in fewer bits using advanced encoding techniques such as run-length limited (RLL) codes, some means must still be provided to put data read from the disk into a form that can be transferred to the CPU. Hence we encounter the need to provide even more circuitry within the box.

In addition, encoding schemes such as RLL, while they stretch capacity by compressing recorded data, require the read channel to have wider bandwidth than the modified frequency modulation (MFM) techniques that are more commonly used. These channels are more susceptible to noise. Designs operating at 900 tracks/in. or better use less signal energy and are more susceptible to off-track interference. The signals generated may be as low as 0.4 mV rather than the 2 to 5 mV of lower capacity drives.

A partial solution is the location of the signal preamplifier on the actuator arm near the read/write heads. This improves signal-to-noise ratio by amplifying the signal before additive noise is introduced. However, the transfer rate is non-standard, requiring a change in the interface to accommodate it. Therefore, Maxtor supports use of the Enhanced Small Device Interface (ESDI) that transfers data at a 10-Mbit/s rate.

An ambitious startup, Applied Information Memories (Milpitas, Calif), plans on using the systems measuring device (SMD) interface to handle its Dart-130 drives. These four-platter drives will provide 140-Mbyte capacity on sputtered thin-film media written 1000 tracks/in. at over 18,000 bits/in. Using a proprietary linear actuator, they will attain an 18-ms average access time.

Using a fully servoed linear voice-coil actuator, Priam saves space in its six-disk drives by splitting the voice coil in half—called a split bobbin approach. Another space saver in this drive is the use of staggered Winchester type heads. Two heads are mounted side by side on the actuator, one facing up and reading the bottom of the upper disk, the other facing down to read the top surface of the lower disk. This technique allows two heads to mount in the vertical space normally required by one. With capacities of 71 Mbytes on four disks and 111 Mbytes on six, models 503 and 505 record at



Capacities of 500 Mbytes are attained by Priam's 8-in. Winchesters. To pack six disks into the drive, a staggered arrangement is used with the 3370 type heads. Two heads are mounted side by side on the actuator. One reads the bottom surface of the upper disk; the other, the top surface of the lower disk.

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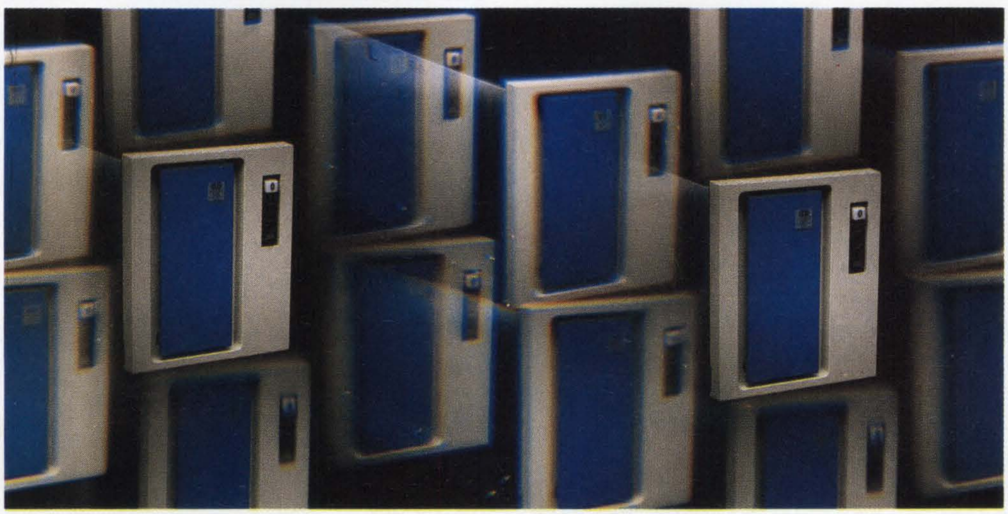

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960 tracks/in. with a linear density of 11,886 bits/in. To handle the increased data rate, the drives mount the data separators on board rather than relying on the controller to perform this function.

Thinner media and smaller heads

Among the factors that enable these capacities to be reached in 5¼-in. products, thin-film media and low profile read/write head suspensions play a major part. Increases in the per surface recording density are due to both.

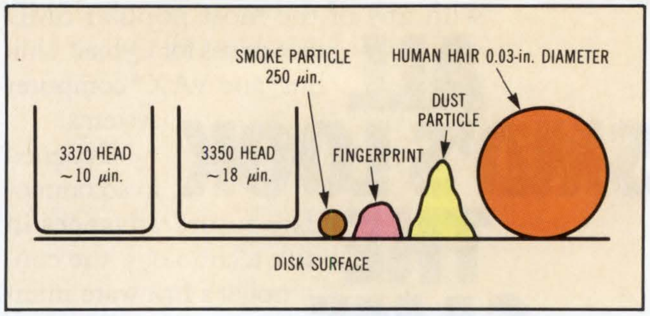
While standard coated ferrous oxide media can be used at track densities to 1000 tracks/in. with 12,000-bit/in. bit densities, reliable readings for data recorded at these densities are difficult to obtain. Many high capacity manufacturers have overcome these problems by using miniWinchester or Whitney type recording heads. Developed by IBM, these heads provide higher recording densities by supplying better signals at lower flying heights.

The 3350 type head commonly used has a three-rail monolithic design. As introduced on the IBM 3340 in 1973, Winchester heads are made of a monolithic ferrite slider that forms half of the head's magnetic circuit. The core that forms the other half is glass-bonded on the back of the slider and handwound with a conductor. As enhanced for use in the IBM 3350, this head flies 18 μin. above the disk's surface, as it records 480 tracks/in. and 6425 bits/in.

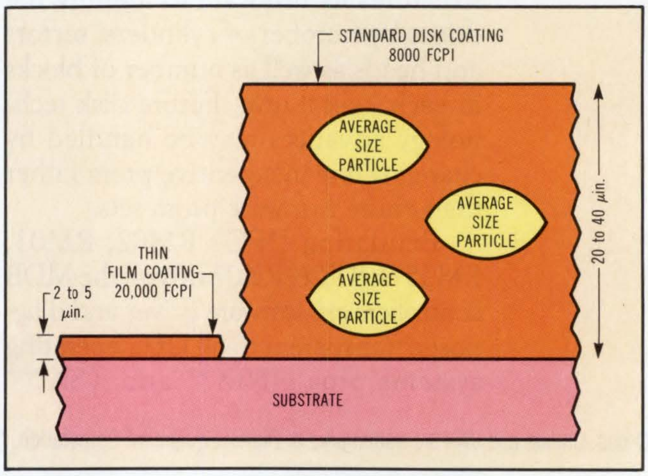
Improving on this design, 3370-type mini-Winchester heads mount composite or monolithic manganese-zinc read/write heads on a low profile head suspension assembly. Composite heads use ceramic sliders and have 90-degree core sides. This minimizes track fringing by concentrating the magnetic field. Mounted on a 3380-type assembly, mini-composite heads reduce mass and provide 85 percent of the efficiency of thin-film transducers. Full benefit of the actuator mechanism is derived when it is combined with a thin-film head as IBM intended. As used in the 3380 disk drive, this design achieves 15,000 bits/in. on 800 tracks/in. with the heads flying at 10 μin.

A very stable read/write platform, the Whitney suspension holds the head rigidly in the disk plane while allowing it to follow variations in surface topography. Stability is provided both by geometry and by reduced mass. The load beam is similar in size and function, but has been streamlined by eliminating the familiar Winchester wings. This eliminates the cause of torsional resonance and reduced mass.

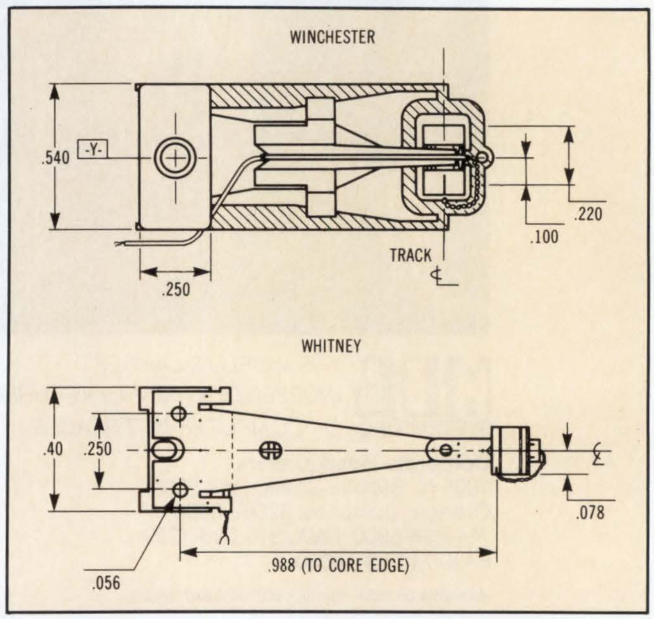
Thin-film plated media contribute to higher capacity by providing better signal-to-noise ratios and increased durability. Having the potential for 2000 tracks/in. and 25,000 bits/in., thin-film media achieve these densities by packing magnetic particles closely in a more orderly fashion than is



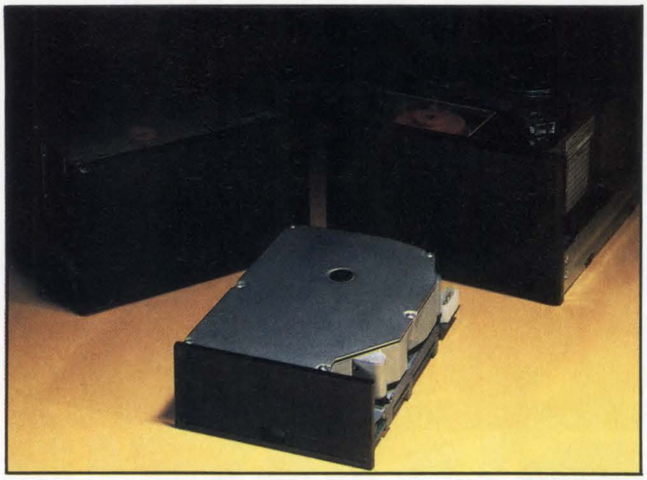
Potential contaminants of a rigid disk system, while in themselves miniscule, have proportions that are large relative to the distance that the head flies above the medium's surface.



Thickness of standard disk coating is contrasted to that of thin-film coating now coming into use. Thin-film coating uses smaller particles to produce a smoother surface that allows heads to ride lower, and provides a sharper signal to the read circuit.



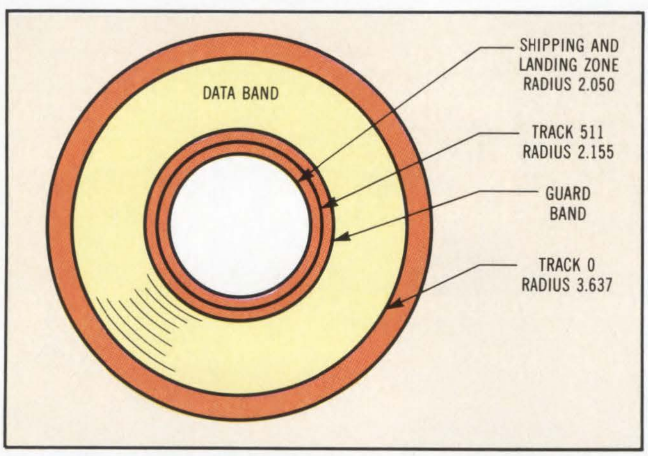
Similar in function to the Winchester suspension, the Whitney type suspension eliminates the wings of its predecessor. This allows the load beam to be streamlined, eliminating torsional resonances that plague Winchester suspensions.



Rodime packs 12 Mbytes onto two platters in their 3½-in. drive, the RQ 352. Measuring 1.625 x 4 x 5.25 in., the drive occupies the same volume as a half height 5¼-in. unit, offers 85 ms average access time, and transfers data at 5 Mbits/s.

achieved with the bigger particles of typical oxide media. The reduction in thickness of the magnetic layer permits denser recording and faster flux reversals, and results in higher signal strengths. Increases in media coercivity also increase areal density by decreasing the adjacent bit demagnetization. Used with conventional heads and actuator mechanisms, thin-film media provide higher capacity by permitting higher bit densities.

Vertex Peripherals achieves linear bit densities of 16,000 bits/in. with a 25-ms average access time in its V2100. The four-disk drive uses 3370 type miniWinchester heads. RLL code records 33 percent more information in a given number of bit cells than is possible using the more conventional MFM encoding scheme. To handle the increased rate of data transfer inherent in the high bit density and the coding scheme, the read channel has been optimized for tolerance to noise and to minimize the effects of fringing.



To protect the recording surface of a rigid disk drive, many manufacturers dedicate one area of the disk's surface solely for the heads to land on. Some drives also include a guard band between the data and landing zone. Approximately 1.5 in. of the disk's surface is used to record data.

Control Data Corp has taken its Wren family up to 80 Mbytes with the 5-platter 9415-80. This unit uses low mass, light load thin-film heads with a balanced rotary arm voice-coil actuated positioner, and achieves 35-ms average access times.

The heads themselves are thin film—read/write transducers are fabricated directly on the slider using semiconductor deposition techniques. A vertical side wall construction (angled sidewall on monolithic Winchesters) reduces fringing from adjacent tracks during read operations.

And yet another form factor

Taking the 5¼-in. form factor down another notch, as the microfloppy drives have, sub-4-in. Winchesters are beginning to emerge. First out of the gate, Syquest Technology has a 6.2-Mbyte drive using 3.9-in. plated media disks. Drives use either fixed disks or removable cartridges.

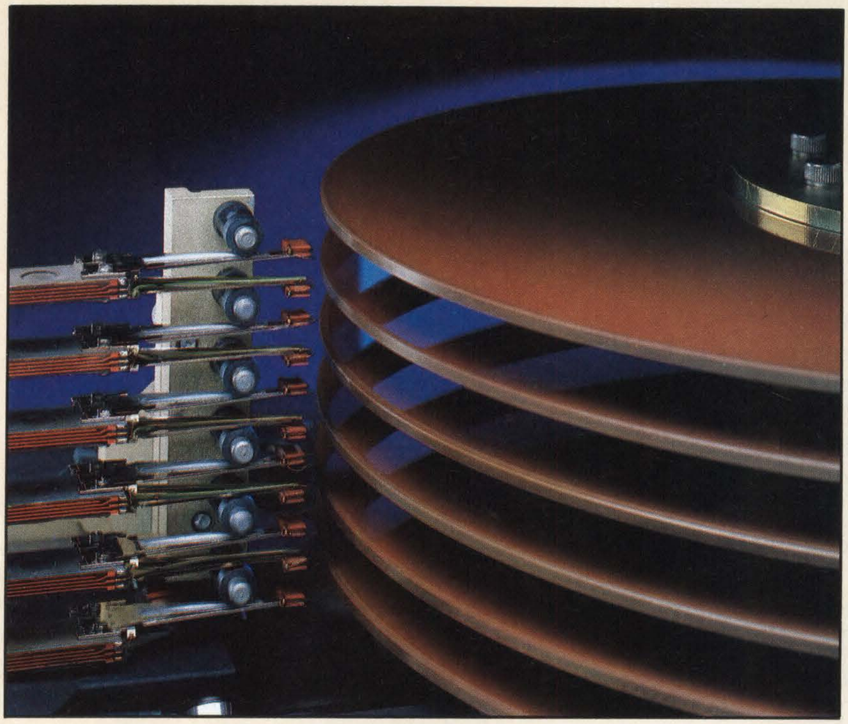
Track density is 435 tracks/in. Each side of the platter has 306 tracks recorded at 12,000 bits/in. The stepper motor drive positioning system steps at 0.9 degrees and uses a proprietary DigiLok closed-loop embedded digital servo system that leaves both surfaces of the disk free for data storage. Access times are 85 ms. Fixed media drives, the recently introduced SQ312, SQ325F, and SQ338F, store 12.75, 25.5, and 38.2 Mbytes using 1, 2, or 3 platters.

Rodime PLC provides a 3½-in. unit, but this one has no removable feature. The RO 250/RO 350 reaches from 6.37 to 12.75 Mbytes in capacity, writing 575 tracks/in. at a bit density of 11,000 bits/in. The stepper motor drive in this unit can access in 85 ms.

Although Control Data did introduce a drive in the 3½-in. form factor, it has since retrieved it. However, as introduced, the Cricket recorded using thin-film heads on both sides of a plated media platter. The heads use a negative pressure air-bearing slider to achieve a lower flying height with a low load design. The unit's band positioning system used with the stepper motor drive provides a 117-ms average seek time. An embedded closed-loop servo system allows densities of 450 tracks/in. and 15,390 bits/in. to be maintained.

Microcomputer Memories Inc announced a 3½-in. hard disk drive that is specifically designed to resist shock, one hazard of portable applications. Storing 6.4 or 12.8 Mbytes of data, the drive uses a time tested standard technology stepper motor, oxide media, and manganese-zinc heads. It packs tracks at 545 tracks/in. and bits at 11,000 bits/in.

The 8-in. Winchester drives that were responsible for the "smaller is better" criteria that marked the beginning of this age of compact rigid disk drives have been relatively stable over the past few years, as more and more effort poured into 5¼-in. units. However, now that the storage needs are pushing



Mechanical reliability of Amcodyne's 8160 head/disk assembly is improved by combining ramp loading techniques with retractable heads. Minicomposite heads are used on a Whitney suspension to supply stable flight at low heights.

upward with the proliferation of multi-user systems, another flurry of products in the 8-in. form factor is emerging. These drives, ranging upwards from 100 Mbytes, unlike their smaller brethren, address the great number of minicomputers in existence as well as the masses of microcomputer systems.

Bigger players stay in the game

Believing that 8-in. drives can best fill the 100 to 300-Mbyte capacity range, Micropolis, the company that provides the 1400 series, promises to cover the 83- to 166-Mbyte range, using three or six platters. A 331-Mbyte drive, the 1456, doubles the capacity of the six disks used to obtain 166 Mbytes by using a double head/double track band design. Mounting two heads for each surface on the carriage assembly, this drive can access two separate sets of 823 cylinders. It achieves a 20-ms average access time and writes at 12,899 bits/in., on tracks having a 1160-track/in. density.

The use of two separate cylinders on each surface makes the drive appear as if it has more platters, and allows it to adhere to the SMD interface. It also decreases access time since each head travels only half of the distance between outer and inner tracks.

Achieving a 500-Mbyte capacity by packing bits at 18,200 bits/in. on plated media, Priam's top of the line 808 uses six platters and writes with 3370-type heads. This drive uses the same staggered head design as the company's 5¼-in. drives to accommodate six platters within the 8-in. form factor.

Northern Telecom (Ann Arbor, Mich), in its Mercury series, supplies a 222-Mbyte capacity as well as 44-, 133-, and 178-Mbyte units, using from two to six platters. These drives use an embedded servo for head positioning and write at 985 tracks/in. and 10,084 bits/in. on oxide media.

New to the 8-in. arena, Seagate recently revealed an 8-in. drive in a half-height version. In this half-height package, Seagate has stuffed three gamma ferric oxide coated platters which store 100 Mbytes. Using low load, manganese-zinc ferrite minislider heads positioned using a proprietary linear voice-coil actuator, the ST8100 has an average access time of 30 ms, and transfers data at 10 Mbits/s.

Differentiated by design innovations that improve the mechanical reliability of the head/disk assembly, Amcodyne's (Longmont, Colo) 8160 drive stores 165 Mbytes and gives a 22-ms access time. Any head to disk contact is eliminated by a

Sizes of standard 5¼-in. full-height (rear left) and half-height (rear right) are compared with that of half-height 8-in. package (foreground). Seagate's 8-in. half-height ST8100 stores 100 Mbytes. The height of the package allows all control electronics to fit with the drive in a standard full-height form factor.

proprietary technique for dynamically loading heads. Heads are launched only after the disk reaches full rotational speed so that they settle on an air bearing rather than on the disk's surface. This ramp loading is combined with full retraction of the heads when not in operation to abolish head/disk chatter during handling, a leading cause of Winchester failure.

Patterned after IBM 3370/3380 technology, the dynamic load suspension system contributes to the head loading technique. It also creates a very stable read/write platform to provide improved read/write signal stability as a result of flight stability. The drive has six disks that provide 10 recording surfaces. A dedicated servo allows 823 tracks to be spaced 960 tracks/in. and to be written at a linear recording density of 9750 bits/in. The use of 2,7 RLL code increases the amount of data that can be written by 50 percent.

Drives are also being produced by Japanese firms to fill user needs in the 8-in. area. Mitsubishi's M4870 stores 251.4 Mbytes on eight platters and supplies 20-ms access times. The six-disk 180F from Toshiba (Kawasaki, Japan) uses RLL code to provide capacity for 132 Mbytes formatted on six disks. Fujitsu America's (Santa Clara, Calif) 8-in. M2333 packs in 337 Mbytes and accesses in an average of 20 ms.

The Eagle (M2312), itself a 10½-in. unit, circumvents problems of 8-in. drives, capitalizing on the extended surface area provided by the larger diameter disk to supply a 474-Mbyte capacity. Now, Fujitsu plans to produce a parallel transfer version of this drive. Capable of simultaneously reading/writing on four or five channels in parallel, the M2350 transfers at 9.3 or 7.4 Mbytes/s. Six disks within the unit are written using two heads for each data surface. The heads are controlled by a rotary voice-coil actuator to provide an average access time of 18 ms.

Control Data Corp, following the same general philosophy as that applied by Fujitsu in selecting the 10½-in. form factor, has chosen to use 9-in. platters for its fixed storage drives. A 340-Mbyte unit, the 9715-340 uses seven disks written at 960 tracks/in. and 9492 bits/in. With a 516-Mbyte capacity, the 9715-500 uses RLL code and packs in data at 15,159 bits/in. Both drives use thin-film heads as will all future drives announced by CDC. Also choosing a 9-in. form factor, NEC Information Systems (Boxboro, Mass) stores 520 Mbytes on plated media. This unit claims to provide a 15-ms average access time.

These 9-in. units, although only 1-in. larger in diameter than 8-in. drives, can provide greater capacity per surface using conventional technology. This makes them highly competitive with 14-in. units, particularly when rack mounting is considered. Two 9-in. drives slide side by side into a standard 19-in. rack, easily providing 14-in. capacity or better within the same rack space.

Using 19 thin-film heads to read/write on five 14-in. platters, Century Data's Advanced Marksman Series 571 meets high capacity, high performance needs. Multiple heads/platter cuts average access time to 19 ms.

Retaining their position at the top of the heap, 14-in. drives, however, will be difficult to displace for those needing to store immense quantities of data within one drive. The IBM 3370 stores 600 Mbytes on 14-in. platters, writing at 12,134 bits/in. and accessing at an average of 20 ms. However, the XMD-800, CDC's highest capacity Winchester packs in 825 Mbytes on five platters. This unit records 15,400 bits/in. at 960 tracks/in. using RLL 2,7 code. Using an extended SMD interface, transfers occur at 14.5 Mbits/s, 50 percent faster than if the standard SMD interface were used.

Century Data (Anaheim, Calif) recently announced the Advanced Marksman series 571. Meeting large storage needs, this drive supplies a 571-Mbyte capacity and an average access time of 19 ms. It uses 19 thin-film heads to read/write on five platters, recording at 10,000 bits/in, on tracks at 800 tracks/in. The unit uses a modified SMD interface to transfer data at 1920 kbits/s. Access time is 19 ms average.

Supplying an 871-Mbyte drive, Memorex Corp (Santa Clara, Calif) accesses data using two independent actuators to accomplish an average access time of 19 ms. The horizontal axis used in the 3695 allows a single motor to drive both spindle and air flow system. This kind of capacity combined with average access times as low as 16 ms gives large systems the kind of storage capability needed. It also gives 14-in. designs some breathing room, at least in this capacity range. It will be sometime before even the most adventurous drive designer can figure out how to pack that much storage into a 5¼-in. box.

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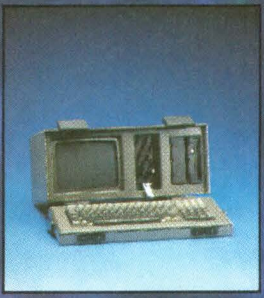


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CIRCLE 120

HOW TO CHOOSE A DISK DRIVE, PART I:

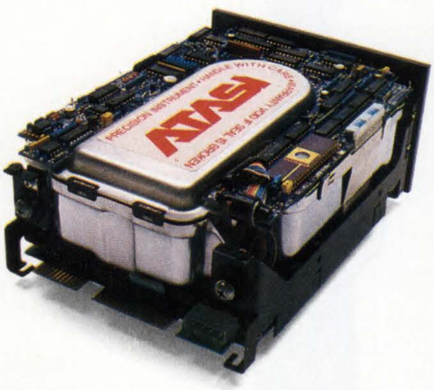
Your new computer system may be in for a cool reception.

Here's a cold, hard fact that should influence your selection of a disk drive for multi-user computer systems or local area networks: In today's energy-conscious offices, temperatures can vary enough during the day to affect the performance of a disk drive. We made the operating range of ATASI drives up to 25% greater than most competitive drives because poor performance under thermal stress can result in system downtime and even lost data. Here's how it happens.

In most drives, the bottom of the bowl serves as the base-plate where the carriage and spindle assemblies are

THERMAL STRESS

mounted. There is no thermal isolation. Heat from the motor, PC boards or a power supply can result in differential expansion of the baseplate, so that it temporarily warps. This can change the alignment of the carriage and spindle, which in turn affects the drive's ability to find data reliably.



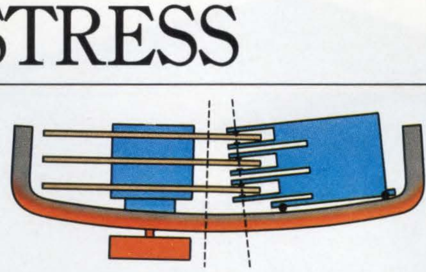
ATASI's 46 Mbyte, 5¼-inch Winchester disk drives are available in production quantities immediately.

Alignment problems

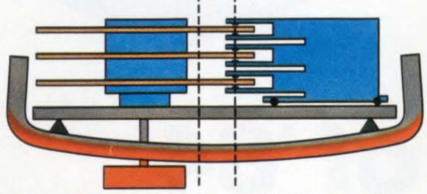
In high-performance, closed-loop drives, servo information carried on the bottom surface of the disk stack is used to position the data heads on all other surfaces. Assume that data is recorded when the drive is "cold." If the carriage and spindle go out of alignment when the drive gets "hot," the servo system cannot properly position the read/write heads to recover the data. This may mean that data written in the morning won't be accessible the same afternoon!

Thermal isolation

To prevent this from happening with ATASI's 5¼-inch Winchester disk drives, the ATASI design incorporates a baseplate which is separate and thermally isolated from



Heat can temporarily warp a drive's baseplate, causing alignment problems between carriage and spindle.



Thermal isolation in ATASI's proprietary design eliminates the problem.

the lower half of the bowl. The baseplate is therefore protected from external sources of localized heat. Even if the drive heats up, it does so uniformly, with no resultant deformation of the baseplate, and no alignment problems.

Extra margins

Thermally isolating key mechanical components is one way we improve the performance of ATASI drives, but not the only one. Everywhere in the design there are margins of safety other drives don't offer. For example, our proprietary spindle motor design provides substantially greater dissipation of heat away from the disk module than competitive drives.

PERFORMANCE SPECIFICATIONS

MODEL NO.	3033	3046
CAPACITY	33 MB	46 MB
ACCESS TIME (AVG.)	30 ms	30 ms
DATA RATE	5 Mbits	5 Mbits
INTERFACE	ST 506	ST 506

Available in high volume today.

MODEL NO.	3065	3075
CAPACITY	65 MB	75 MB
ACCESS TIME (AVG.)	24 ms	24 ms
DATA RATE	5 Mbits	5 Mbits
INTERFACE	ST 506	ST 506

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The ATASI White Paper

At ATASI, we are proud of the quality we build into every drive we make, and we encourage clients to test our products rigorously. To help, we have prepared a White Paper on thermal testing which discusses test methods and interpretation of test data in detail.

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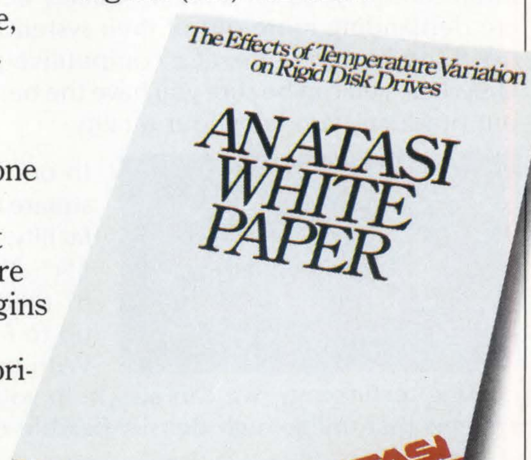


ATASI

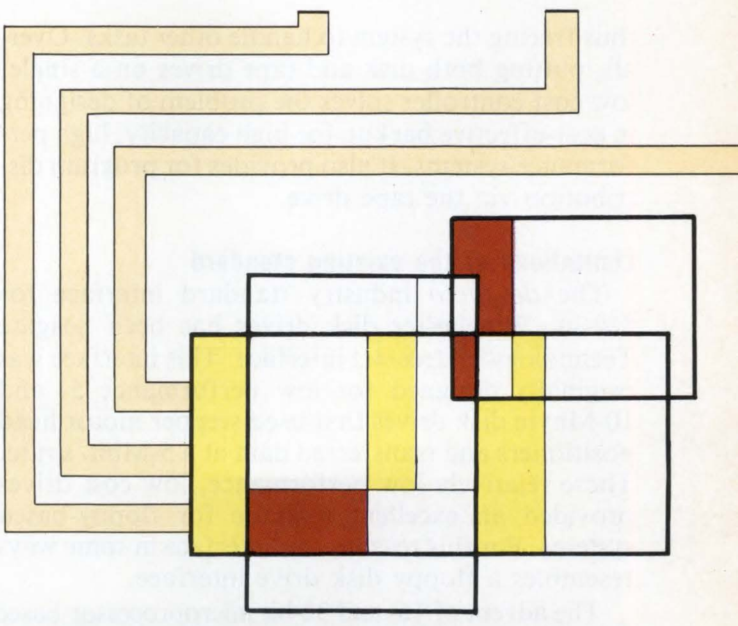
INTERFACE PAVES THE WAY TO HIGH PERFORMANCE

Removing the restrictions placed by existing interfaces on 5¼-in. hard disk transfer rates, the Enhanced Small Device Interface clears the way for higher recording densities.

by Frank Seuberling

During the past year, an interface has emerged that will not only handle today's mass storage needs, but will also expand to meet foreseeable future needs. The Enhanced Small Device Interface is designed to handle a variety of 5¼-in. Winchester disk and tape drives. It opens the door to higher performance system designs by incorporating more intelligence into the drives, and by allowing higher data transfer rates—10 Mbits/s and above. Thus, it allows higher recording densities and, ultimately, higher storage capacities in the 5¼-in. form factor.

By facilitating the design of multiple device controllers, the Enhanced Small Device Interface (ESDI) will allow system designers to mix and match disk and tape devices to meet designer needs on a single controller, independent of the system bus (Fig 1). Microprocessors are used in both the control units and the disk/tape drives. Thus, firmware can accommodate different command structures, and connector pin designations will be the same for both disk and tape devices.



The single controller provides several advantages for the system designer. First, the host need not provide buffer space in backup operations. (Other configurations require buffer space because disk and tape devices rarely operate at the same data rate.) Second, the system bus is not tied up during data transfer. Using ESDI, a minimum number of commands may be sufficient to back up an entire disk,

Frank Seuberling is a development engineer at Maxtor Corp, 61 Daggett Dr, San Jose, CA 95134. He was responsible for the digital design ESDI, and for developing the microprocessor code for interface and servo control. Mr Seuberling holds a BS in physics and a BA in mathematics from Humboldt State University, Arcata, Calif.

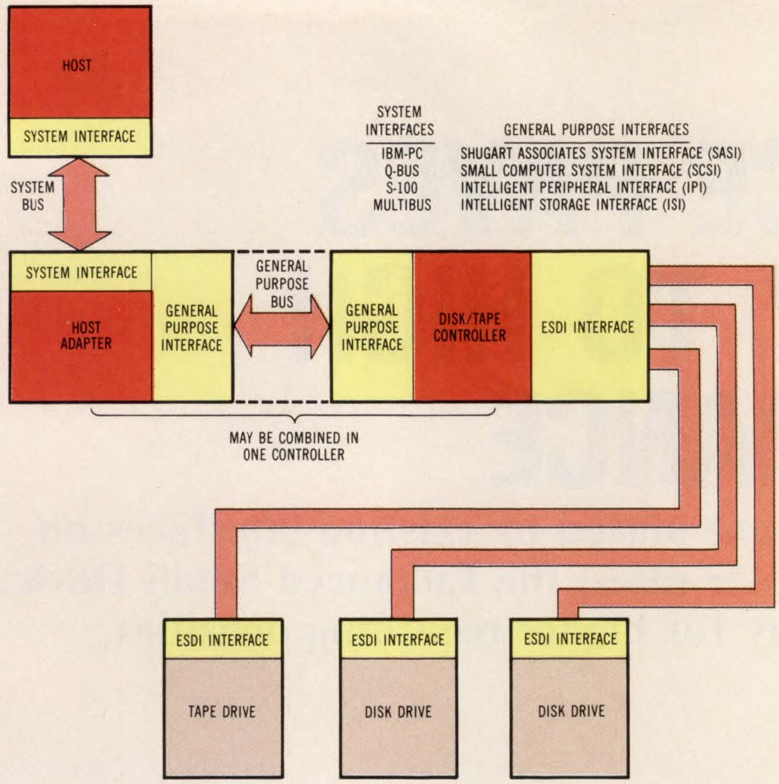


Fig 1 The Enhanced Small Device Interface (ESDI) defines the connection of disk and tape devices to the controller; it does not define the controller-host interface. Thus, the ESDI can be configured into systems using a variety of general purpose and system interfaces with a minimal impact.

thus freeing the system to handle other tasks. Overall, putting both disk and tape drives on a single, low cost controller solves the problem of designing in cost-effective backup for high capacity, high performance systems. It also provides for program distribution via the tape drive.

Limitations of the existing standard

The *de facto* industry standard interface for 5¼-in. Winchester disk drives has been Seagate Technology's ST506/412 interface. This interface was originally designed for low performance 5- and 10-Mbyte disk drives that used stepper motor head positioners and transferred data at a 5-Mbit/s rate. These relatively low performance, low cost drives provided an excellent upgrade for floppy-based systems. For this reason, this interface in some ways resembles a floppy disk drive interface.

The advent of 16- and 32-bit microprocessor-based systems, however, has caused an increase in the demand for higher storage capacity in smaller packages. Since the ST506/412 interface served as the 5¼-in. *de facto* standard, it was the obvious first choice for a higher transfer rate interface design. However, considering the capacity and performance desired, it has two serious limitations. It assumes a stepper motor positioning system, and it limits the data transfer rate to 5 Mbits/s.

There are three ways to increase capacity on a disk storage device: increase the track density, measured in tracks/in.; increase the flux reversals/in. (FRPI); or increase the recording area (number of platters) in the package. All three methods pose problems with the ST506/412 interface.

Increasing the FRPI increases the transfer rate, thus putting the device in immediate violation of the ST506/412 standard. Increasing the number of disks also violates the standard since it allows only eight heads to be selected. Furthermore, since open-loop positioning systems (usually stepper motors) typically have an upper limit of less than 500 tracks/in., increasing track density requires that a more accurate closed-loop positioning system be used. Closed-loop servo systems generally employ a voice coil actuator. Since the ST506/412 is designed to operate as a stepper motor interface, the full performance benefit of the drive will not be realized. Increasingly, as drive designers turn toward thin-film heads, thin-film media, and closed-loop, track following positioners to provide high capacity, this interface imposes a limitation on performance.

These limitations induced a group of controller and disk drive manufacturers to meet, beginning in October 1982. Addressing the current and future interface needs of the industry, in March 1983, the meetings resulted in the Enhanced Small Disk Interface. In August 1983, another series of meetings between controller and tape drive manufacturers brought forth the Enhanced Small Tape Interface. In November 1983, these interfaces were combined

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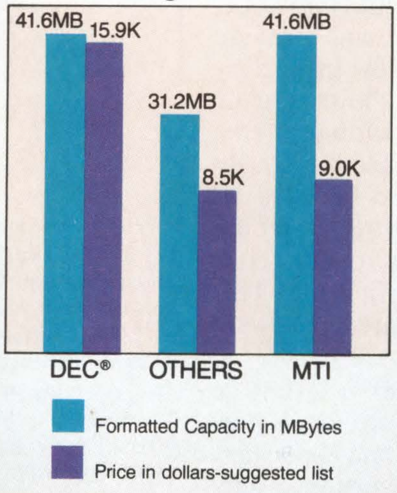

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ESDI Controllers under Development

Manufacturer	Model	Interface supported
Adaptec	—	SCSI
Concept Development	—	Multibus
DSD	—	Multibus
DTC	500C series	SASI
Distributed Logic	—	Q-bus
Emulex	SC05	Q-bus
Interphase	unknown	IBM PC
Konan	DGC-100	S-100
	DJ	SASI
	Taisho	Multibus
OMTI	6100/6300	SASI
Xylogics	421	Multibus

into one specification, ESDI, to provide a system solution to disk storage and tape backup for both current and future needs. Controllers implementing the interface are currently under development by a number of vendors (see Table).

The cable used to connect the disk drives and tape drives to the ESDI controller is the same as that used with the ST506/412 interface. A control cable is daisy chained to all devices connected to the controller, and carries signals to the drives and multiplexed signals from the selected drive. In addition, each device is connected to the controller through its own radial data cable.

Defining the ESDI

The ESDI allows two modes of implementation—step mode or serial mode. Either step mode or serial mode can be used for disk drives, while only serial mode can be used for tape drives. Very similar in definition to the ST506/412 interface, step mode is designed for stepper motor positioning drives. However, "index," as well as "seek complete," and "sector/byte clock/address mark found" are available on either the daisy chained or radial cable, making overlapped seeks possible.

On the other hand, serial mode takes advantage of more intelligent, higher performance devices such as disk drives that use closed-loop servo systems and voice coil actuators. When serial mode is implemented, the full benefit of ESDI becomes apparent. Voice coil actuator positioning systems provide access times of around 30 ms and allow track densities in excess of 800 tracks/in. This allows systems that run multi-user/multitasking operating systems to obtain the capacity and performance previously attainable only with large drives (8 and 14 in.), with 5¼-in. form factor drives. In addition, attaching serial interface disk and tape drives to ESDI controllers allows systems to be self-configuring. This simplifies the task of writing software for a wide variety of devices.

Since the purpose of a disk or tape drive is to store or retrieve data, a key feature of any interface is how that data is transferred between drive and controller. In the past, most 5¼-in. drives have transferred data in the same manner in which it was encoded on the drive, ie, in a modified frequency modulation (MFM) format. The ESDI, however, specifies that data separation is done on the drive, and that data transferred between the drive and controller are non-return to zero (NRZ). Since NRZ data is not self-clocking, separate read and write clocks must be provided (Fig 2). Although the requirement that each drive have its own data separator adds to the drive cost, the advantages that it provides over interfaces transferring MFM data seem to justify the added cost. These advantages include more reliable data transfer between the controller and drive, the ability to interface disk drives that transfer data at different rates, and the flexibility to incorporate advanced encoding schemes on the drive.

The data interface is more reliable because NRZ encoded data is transmitted. Instead of transmitting a single signal composed of both clock and data pulses down a cable, the drive or controller provides a separate 50-percent duty cycle clock. This allows data bits to be a full bit cell in length, and makes NRZ data much less susceptible to noise and jitter than MFM.

The variable data transfer rate stems from the fact that all ESDI drives provide a reference clock signal that determines the drive's transfer rate. On the other hand, with the ST412 HP interface, the controller sets the data rate. Thus, if the manufacturer wishes to take advantage of the standard interface, drive performance may be impaired. Furthermore, the encoding scheme used on the drive becomes almost transparent to the interface because data is transferred in NRZ format.

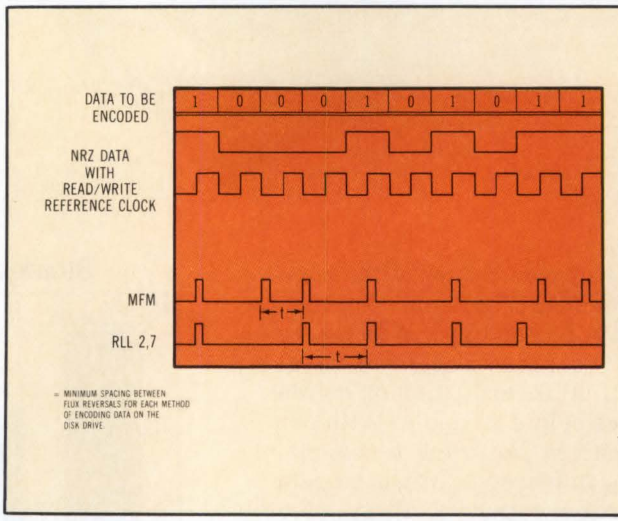
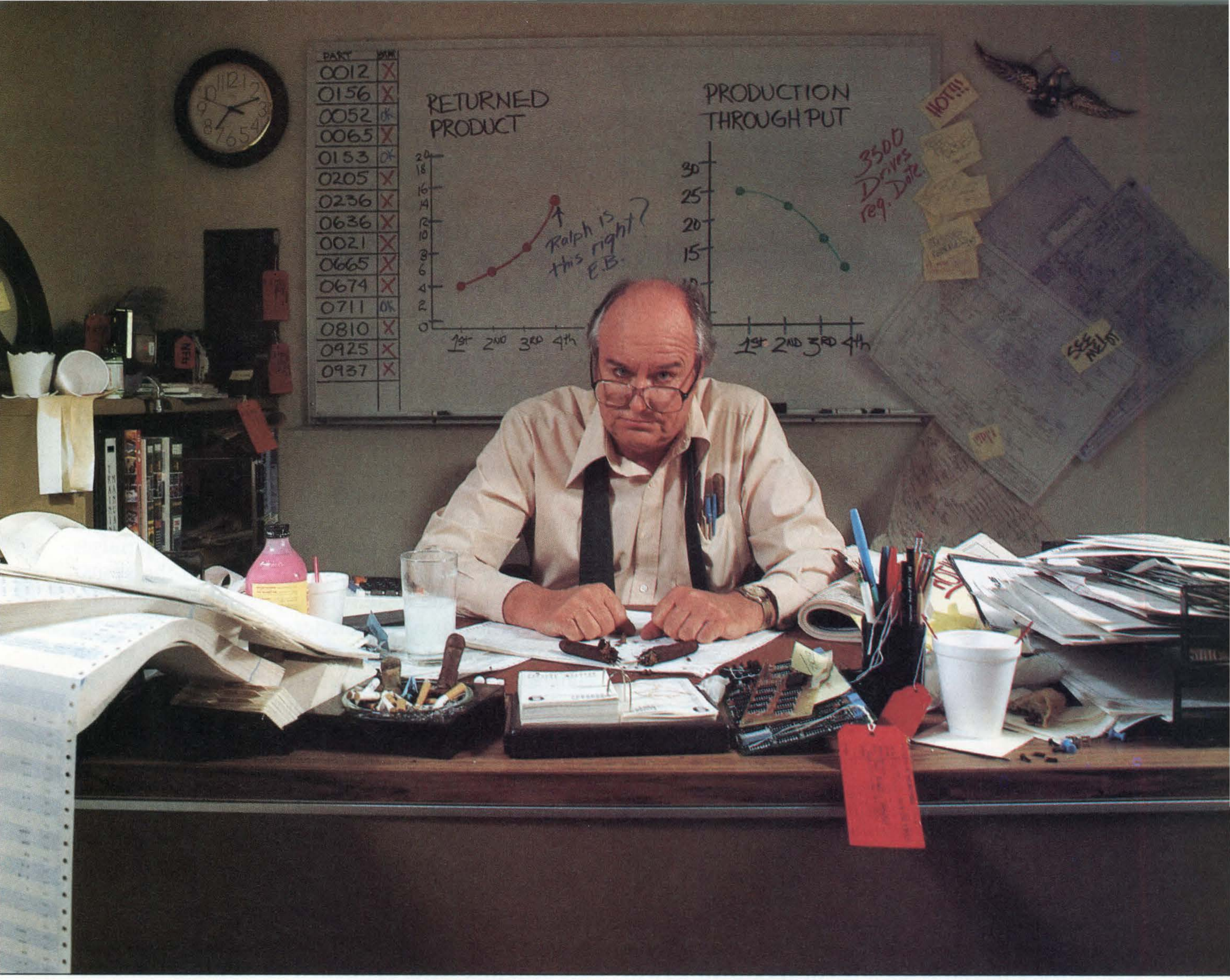


Fig 2 The ESDI calls for data separation to be done on the drive, with nonreturn to zero (NRZ) data transferred between drive and controller. As NRZ data transfer requires read/write reference clocks, it provides a reliable controller to drive interface. Modified frequency modulation (MFM) data encoding or an advanced encoding scheme such as a 2,7 run-length-limited (RLL) code may still be used on the drive. The diagram shows that advanced encoding schemes offer significantly increased bit density.



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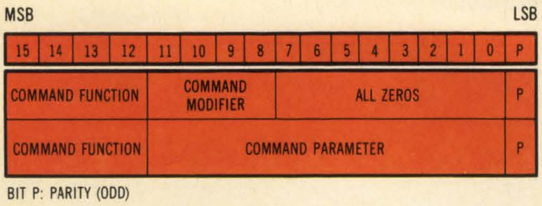


COMMAND FUNCTION BIT 15 14 13 12	DISK DRIVE COMMAND FUNCTION DEFINITION	TAPE DRIVE COMMAND FUNCTION DEFINITION
0 0 0 0	SEEK	LOCATE BLOCK (OPTION)
0 0 0 1	RECALIBRATE	LOAD TAPE (OPTION)
0 0 1 0	REQUEST STATUS	REQUEST STATUS
0 0 1 1	REQUEST CONFIGURATION	REQUEST CONFIGURATION
0 1 0 0	SELECT HEAD GROUP (OPTIONAL)	SELECT TRACK
0 1 0 1	CONTROL	DECK CONTROL
0 1 1 0	DATA STROBE OFFSET	READ
0 1 1 1	TRACK OFFSET	UNLOAD TAPE (OPTION)
1 0 0 0	INITIATE DIAGNOSTICS (OPTIONAL)	INITIATE DIAGNOSTICS
1 0 0 1	SET BYTES PER SECTOR (OPTIONAL)	SPACE FORWARD/REVERSE
1 0 1 0	RESERVED	FAST POSITION EOT/BOT
1 0 1 1	RESERVED	WRITE
1 1 0 0	RESERVED	ERASE FIXED LENGTH
1 1 0 1	RESERVED	RESERVED
1 1 1 0	RESERVED	RESERVED
1 1 1 1	RESERVED	RESERVED

Fig 3 The serial mode of implementation for disk and tape devices takes advantage of added drive intelligence. Communications with the drive are carried out through 16-bit commands and responses, followed by a parity bit. Thus, the system can be self-configuring, simplifying the writing of software to handle a wide variety of devices.

This transparency allows data to be encoded using high density methods such as MFM or a variety of run-length limited (RLL) codes. The trade-off in selecting a code is one of circuit complexity versus bit density. For example, 2,7 RLL code increases bit density by 50 percent over MFM, while maintaining the same number of FRPI. However, the implementation of 2,7 RLL code requires much more circuitry than does MFM.

Perhaps of greatest significance to system designers is the fact that the driver provides the data separation function internally. Thus, the drive manufacturer can control the drive error rate more precisely, independent of the controller used. This is not the case with MFM data transfer, as different controller manufacturers use different data separators. Thus, disk drives with NRZ data transfer can provide higher data integrity with a wide variety of controller designs.

The performance benefits attained by putting the data separator on the drive more than offset the cost in terms of system efficiency and reliability. Furthermore, NRZ data transfer is not new to the world of disk drives. For years, 8- and 14-in. drives have used NRZ interfaces. MFM data transfers were used for 5¼-in. Winchesters because they evolved in a floppy-disk drive environment. With ESDI and NRZ data transfers, 5¼-in. disk drives can incorporate the performance and data reliability traditionally provided by larger drives.

Surveying step and serial modes

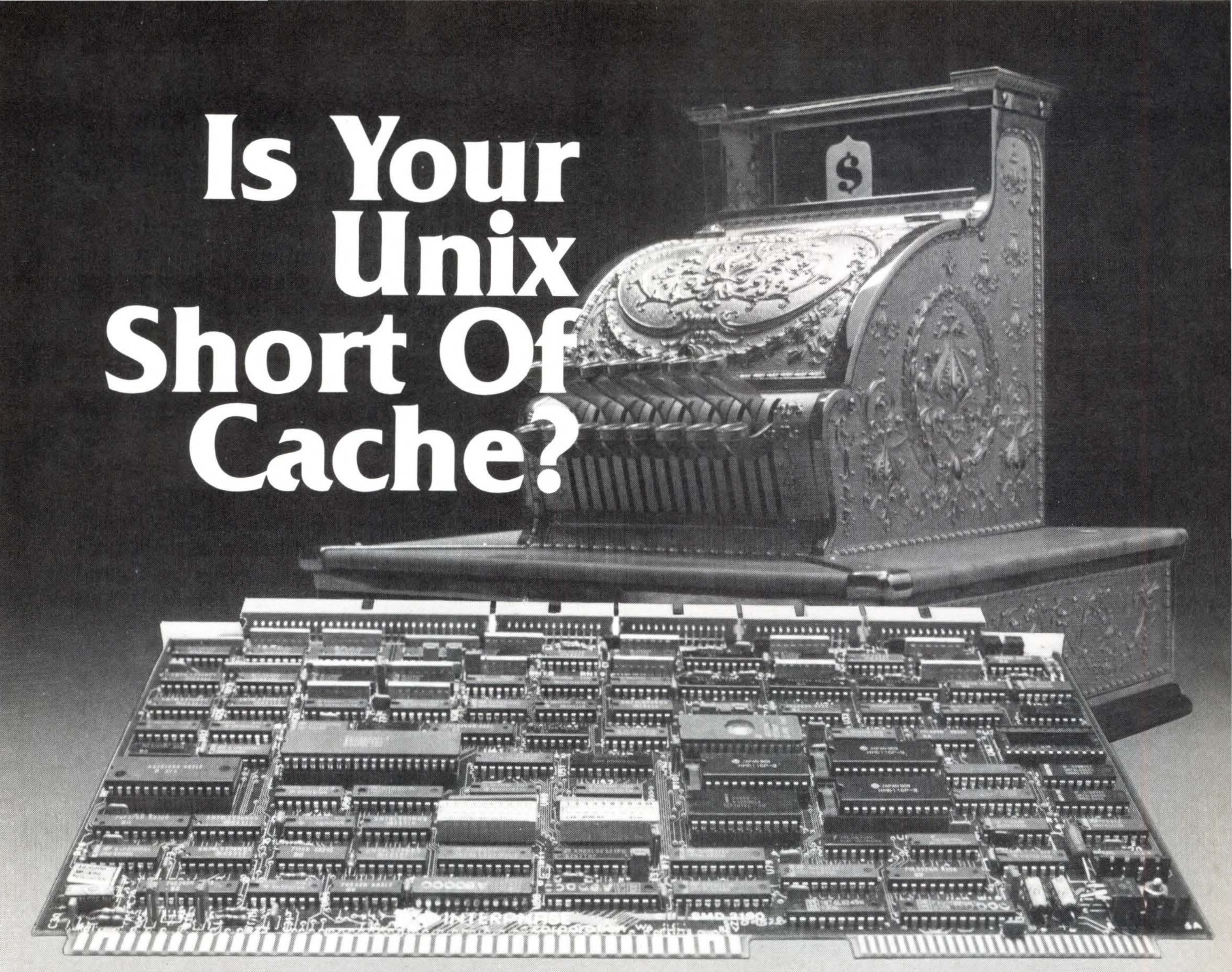
The ESDI step mode is intended for drives with stepper motor positioning. This mode is very similar to the ST506/412 interface; however, the data transferred is NRZ. A maximum of three drives is supported in this mode. Each drive can have up to 16 heads (if fixed media), or eight heads (if removable media). In a removable cartridge drive, the most significant head select line is used as an optional "remove cartridge" line, allowing the spindle motor to be stopped for cartridge removal.

In step mode, head positioning is achieved with the controller setting the direction line, and issuing a step pulse for every track to be moved. Step pulses can be sent at up to a 4-μs rate. As with the ST506/412 interface, the system is responsible for keeping track of the drives' parameters (ie, number of heads and cylinders). Usually, the controller must be initialized with this information before the drive can be used for normal operations.

Serial mode, which supports up to seven devices, assumes a more intelligent drive, and is intended to take advantage of the high performance capabilities of disk drives with voice coil actuators and closed-loop servo systems. Communications between the controller and the drive are carried out using a series of 16-bit commands and responses with a parity bit (Fig 3). With a simple request/acknowledge handshake protocol for each bit, commands and responses are sent in a serial fashion. The controller initiates all transfers. A drive can request that the controller read the drive's status by asserting the attention line on the interface.

Performance benefits attained by putting the data separator on the drive offset cost through efficiency and reliability.

Commands consist of a 4-bit command function code, followed by either 12 parameter bits, or 4 bits of command modifier and 8 bits set to 0. The command function code determines the type of command, such as seek or request configuration. The parameter bits are used to pass information to the drive, such as a cylinder address in a seek command. The modifier bits are used to obtain up to 16 variations of each command. Through various modifier bits, the request configuration command can determine all of a drive's attributes. With the modifier bits set to 0, the command returns the general configuration, while 1 in the modifier bits, for example, would return the number of fixed cylinders in a drive.



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BIT POSITION	FUNCTION
15	RESERVED
14	REMOVABLE MEDIA NOT PRESENT
13	WRITE PROTECTED, REMOVABLE MEDIA
12	WRITE PROTECTED, FIXED MEDIA
11	RESERVED
10	RESERVED
9	RESERVED
8	POWER ON RESET CONDITIONS EXIST
7	COMMAND DATA PARITY FAULT
6	INTERFACE FAULT
5	INVALID OR UNIMPLEMENTED COMMAND FAULT
4	SEEK FAULT
3	WRITE GATE WITH TRACK OFFSET FAULT
2	VENDOR UNIQUE STATUS AVAILABLE
1	*WRITE FAULT
0	REMOVABLE MEDIA CHANGED (REMOVABLE MEDIA HAS BEEN CHANGED SINCE LAST STATUS REQ)

(a)

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	GENERAL CONFIGURATION OF DRIVE AND FORMAT
0	0	0	1	NUMBER OF CYLINDERS, FIXED
0	0	1	0	NUMBER OF CYLINDERS, REMOVABLE
0	0	1	1	NUMBER OF HEADS
0	1	0	0	MINIMUM UNFORMATTED BYTES PER TRACK
0	1	0	1	UNFORMATTED BYTES PER SECTOR (HARD SECTOR ONLY)
0	1	1	0	SECTORS PER TRACK (HARD SECTOR ONLY)
0	1	1	1	MINIMUM BYTES IN ISG FIELD*
1	0	0	0	MINIMUM BYTES PER PLO SYNC FIELD
1	0	0	1	NUMBER OF WORDS OF VENDOR UNIQUE STATUS AVAILABLE

(b)

Fig 4 Standard status responses to the controller's status request command include error reports and state of the drive information (a). Responses to the request configuration command (b) return information as to drive type, sectoring (hard or soft), encoding method, and capacity.

In serial mode, the controller passes the cylinder address to the drive as part of the seek command (direct cylinder addressing). The drive calculates the direction and magnitude of the seek to be performed. Other commands allow the controller to request the drive's status, start or stop the spindle motor, and perform other functions. Optional data strobe and track offset commands can be used to attempt data recovery in case of error.

Responses to the request status command allow the controller to gain information as to the current drive state [Fig 4(a)]. This includes error reporting and some state information such as drive write protected or removable media not present in a cartridge drive. Values other than 0 for the modifier bits in the request status command allow the controller to read status words unique to the drive vendor, such as diagnostic results.

Responses to the request configuration command return static attributes of the drive including 16 bits of general configuration. The general configuration gives the controller such information as the drive's type, whether it is hard- or soft-sectored, and whether or not it uses MFM encoding [Fig 4(b)]. This last point is very important in the design of controllers that use error correction circuitry to detect and correct errors. A media defect that will cause a single-bit error in MFM can cause an error up to 5 bits long in 2,7 code system. (This propagation in error occurs since 2,7 code encodes data up to 4 bits at a time.) Therefore, a controller that attempts correction in a system using 2,7 code should be able to handle a burst error of at least 5 bits.

The other responses to request configuration return physical and format information necessary for drive use. The result is that the system need not keep track of the device's parameters in order to use

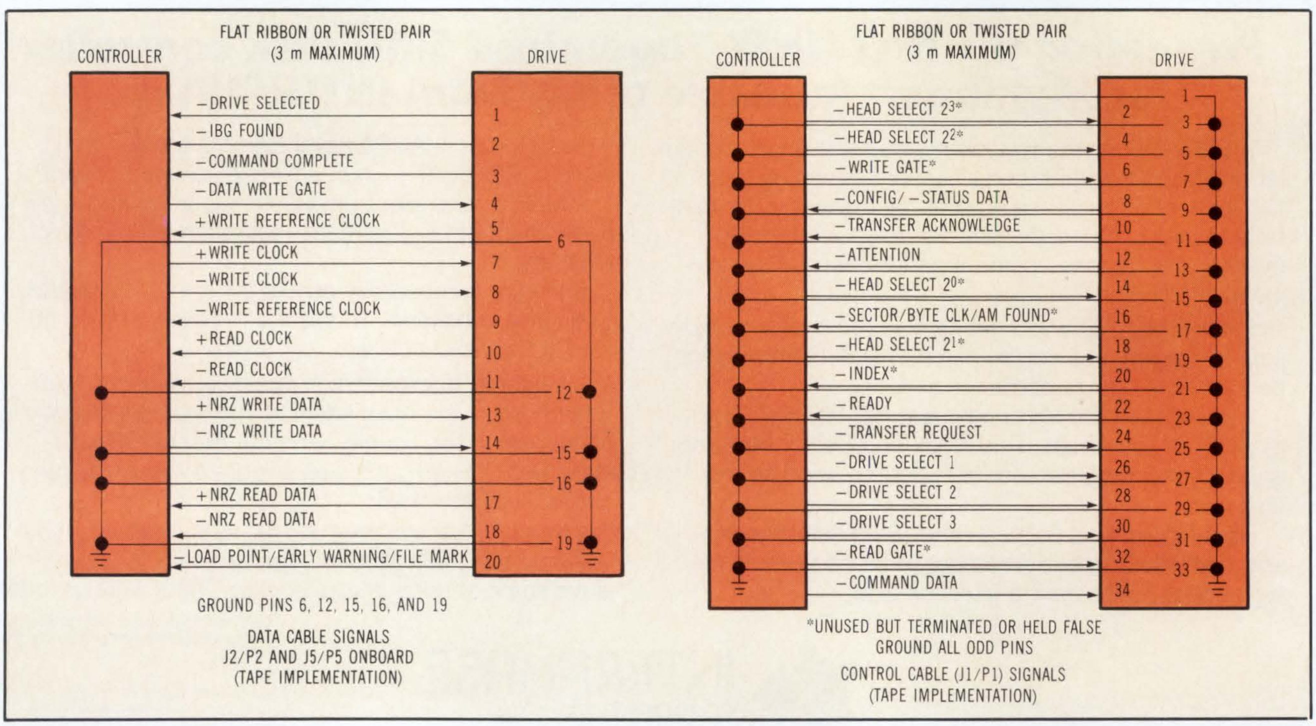

Fig 5 In ESDI tape implementation, pin assignments differ slightly from those used for disk implementations. Only serial mode is supported, and a write reference clock has been added to allow read after write operation.

it. This greatly simplifies the task of using different storage devices in a system.

Tape drive implementation

Tape drive ESDI implementation differs slightly from that for disks. Only serial mode is supported for tape drives, and an added write reference clock signal allows read after write operation (Fig 5). In this case, the write reference clock from the drive controls the NRZ data transfer rate during write operations.

Implementating disk drives and tape drives on the same controller reduces system overhead and controller count.

The ESDI supports two types of tape devices: streaming and start/stop tape drives. As with disk drives, the controller can obtain the tape drives' operating characteristics from the request configuration command. An optional locate block command adds considerable flexibility. When this command is issued, the controller may deselect the drive and monitor the drive's command complete signal on the data cable while the drive searches for the specified block. This allows the controller to tend to other tasks while the tape drive locates the correct block. The space forward/reverse command allows single block movement; it can also be used to search for file marks if supported by the drive. Although the streaming tape capabilities provided by the ESDI are similar to those of the QIC-02 interface, the ESDI goes further by allowing devices to be streaming, start/stop, or to have the capability of both modes.

Thus, the EDSI offers system designers a number of benefits. Implementation of both disk drives and tape drives on the same controller reduces system overhead and controller count. Because controllers have standard host interfaces, they can be easily incorporated into systems. Maximum reliability and efficiency from all devices are attained by virtue of NRZ data transfer. Self-descriptive drives provided by the interface's serial implementation allow systems to be self-configuring. In these ways, the interface provides the tools that designers will need to meet the demands of oncoming high performance storage devices.

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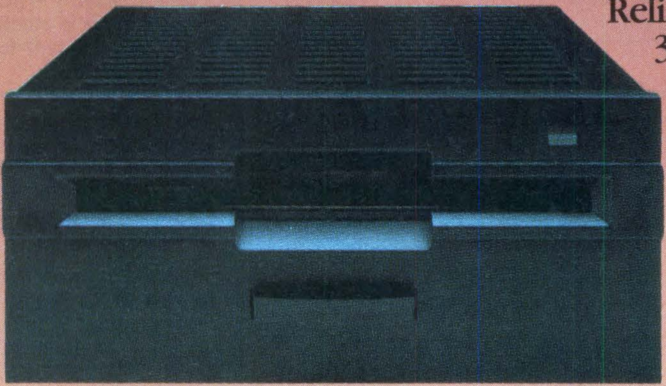

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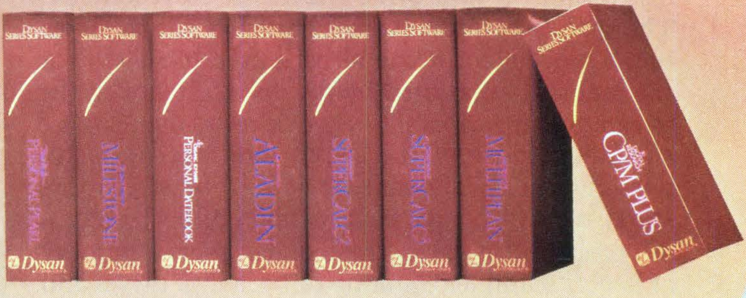

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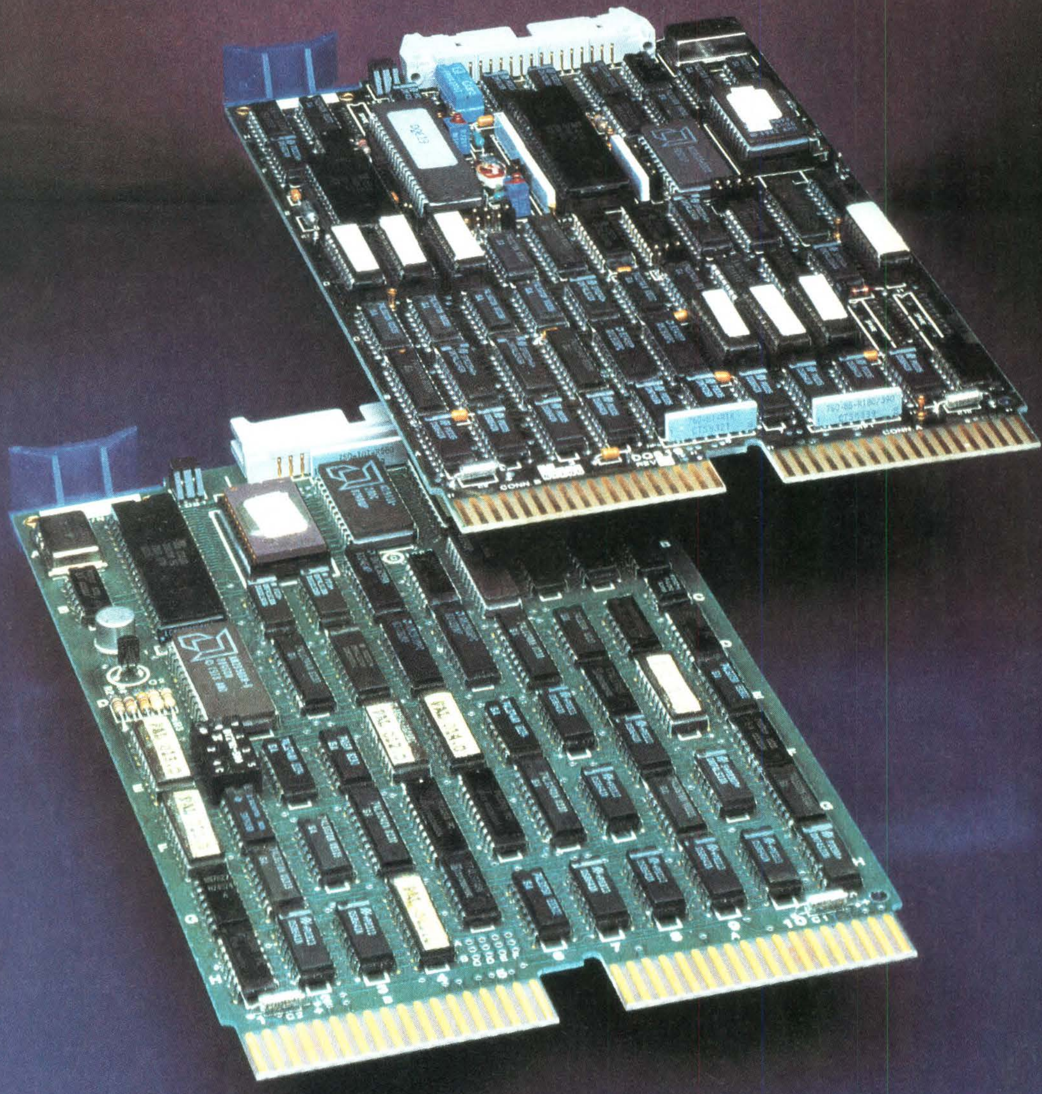

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INTERFACE SPEEDS DATA TRANSFER AND RECOVERS LOST DATA

Recovery mode—a method of recovering data lost because of head positioning errors—is embedded in a disk drive interface that allows data transfers to occur three times faster than existing standards.

by Don Nanneman

Compact high performance Winchester disk drives continue to add capacity in response to the storage needs of powerful microcomputer systems. Drives have taken advantage of all the techniques at their disposal to increase track densities and thus gain more capacity per recording surface. However, the next round of storage expansion will depend on increases in linear bit density, which will result in a higher data transfer rate. Although media will support large increases in bit-packing densities, the interfaces that are available will not support the resultant data transfer rates.

These problems are taken into account by the ST412 HP (high performance) interface, which specifies a maximum data transfer rate of 15 Mbits/s—three times that of current standard interfaces. The impact a new interface has on system and controller designs is minimized by retaining all features of the existing ST506/412 interface, a recognized standard for 5¼-in. disk drives. Signal functions and definitions remain essentially the same as those defined in the ST506/412 interface specification. There are major enhancements that system integrators should be aware of, however. Among the most important of these is the provision of a method for recovering misread data.

Using the ST412 HP's recovery mode, a drive can reposition its read/write heads during read operations on command from the controller. To allow increased storage capacity by putting more bits in each track, the interface's data read/write channels accommodate data transfer rates as high as 15 Mbits/s, compared to 5 Mbits/s in the ST506/412 interface. Access time improvement results from increasing the stepping rate.

The enhanced interface permits the minimum time between step pulses to range as low as 1 μs, as compared to 5 μ in the ST506/412 version. Potential capacity is improved by doubling the maximum number of head selects.

Probably the most significant aspect of the ST412 HP interface to system designers and users is the availability of recovery mode. Previously, Winchester subsystems that encountered difficulty reading a block of data from the disk had only one alternative to try and recover the data. Data had to be reconstructed using the error correction codes (ECCs) previously recorded on the disk. However, if the problem was caused by faulty positioning of the read and write head over the data track, the drive was not

Don Nanneman is product marketing manager at Seagate Technology, 920 Disc Dr, Scotts Valley, CA 95066. He is responsible for Seagate's Winchester disk drive controllers and high capacity drives.

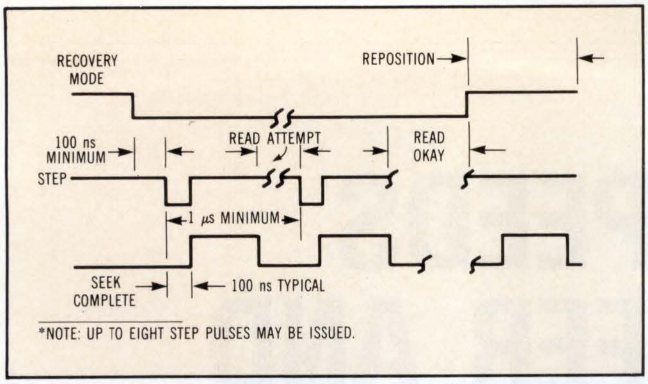

Fig 1 When in recovery mode, a controller pulses the step line to tell a drive to perform another recovery operation. The drive responds with a seek complete signal to indicate when the controller can attempt to read data. After the controller turns off recovery mode, the drive moves the read/write heads back to their nominal positions, eliminating any offset produced by micropositioning.

able to read the ECC information any better than it could read the data itself. The final result would be lost data.

Although Winchester disk drives are highly reliable, in rare instances they can misplace data. The culprit in most cases is offtrack head positioning, a problem compensated for by recovery mode. The problem arises in the first place because of mechanical variations. Factors such as temperature or humidity can cause the disk's positioning system to place the head slightly to one side of a recorded track. This position prevents the head from reading the strongest signal of the recorded data. If the head is far enough off the track, the signal is too weak for the controller to read reliably.

Positioning accuracy becomes increasingly important as small Winchesters move into ever higher recording densities. These higher track densities leave a much lower margin for positioning error. Provision of recovery mode by the ST412 HP will benefit high performance systems as they grow in capacity.

Recovery mode at work

To understand recovery mode operation, consider what happens when a positioning error occurs in a drive that uses a voice-coil actuator. Remember that recovery mode can be implemented in different ways, depending on a specific drive's capabilities. The implementations discussed here are only examples of how a drive might handle recovery.

After positioning the disk's read/write heads, the computer system's controller normally reads data from the disk and calculates ECCs. The calculated codes will match those recorded on the disk when the data was written, if the data was read accurately. However, in this case, offtrack heads prevented accurate reading and the two sets of codes do not match. In response to the error, the controller first commands another read. This second attempt has a good chance of working, especially if the error resulted from a slightly noisy signal. In fact, a controller will generally initiate up to eight rereads. However, because the error results from faulty positioning, each read results in a read error. Therefore, the controller instructs the drive to enter recovery mode.

To enter recovery mode, the controller sets the recovery mode line true and generates a step pulse (Fig 1). When the drive receives this pulse, it sets the seek complete line false and starts recovery procedures. First, the drive backs the heads up two tracks and repositions them over the original track from a positive direction. This operation can correct a faulty position by overcoming any hysteresis in the actuator mechanism. As soon as the heads settle, the drive sets seek complete true, informing the controller that it can read data again. Note that the system remains in recovery mode.

If the controller's attempt to read data is unsuccessful, it issues another step pulse. Because recovery mode is still active, the drive will perform the second recovery operation. After setting seek complete line false, the drive this time moves the heads two tracks forward and repositions them from a negative direction. Seek complete returns true, and the controller again tries to read data. An unsuccessful attempt to read data correctly this time causes the controller to issue another step pulse. The drive will now microposition the heads offtrack in an attempt to find a stronger signal. In this example, the drive moves the heads backward one-tenth of a track from the nominal track position. If data cannot be

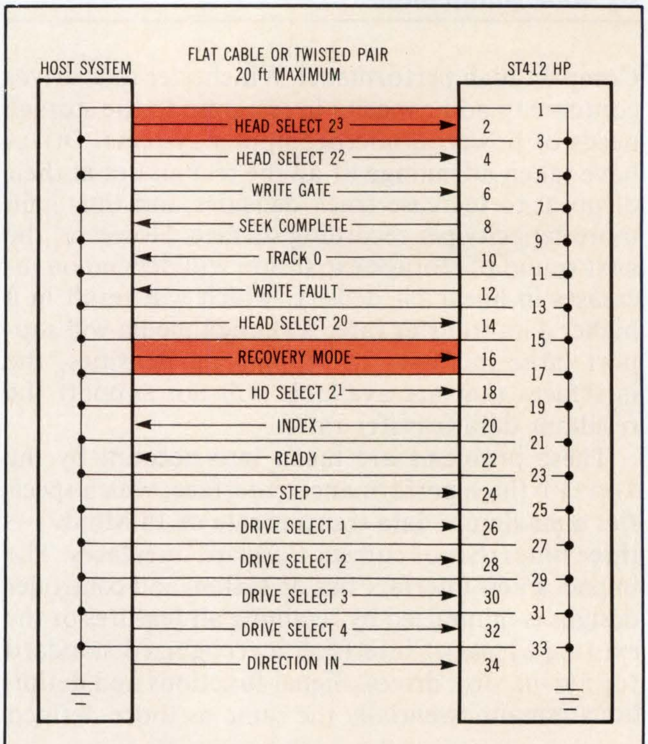

Fig 2 The control signal connector in the ST412 HP employs two lines that were reserved on the ST506/412 interface: recovery mode and an additional head select. These changes represent the only pinout differences between the two interfaces.

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read at this location, the drive will move the heads another one-tenth track backward. Failure to read data on this attempt causes the drive to move one-tenth track away from the nominal position in a positive direction and then, if necessary, by another one-tenth track increment.

The controller can issue as many as eight step pulses while in recovery mode. Whenever one of the drive's recovery methods results in a successful read, the controller returns the recovery mode line false, and the drive returns the heads to their nominal position. If all attempts to read the data while in recovery mode fail, the controller can then resort to reconstructing the data using the ECC information. Since positioning correction methods (ie, recovery mode) were not successful, it can be assumed that the read problem may be media related. However, the system should attempt all available mechanical means of recovering data, such as recovery mode, before trying to use ECC.

If ECC is used before mechanical repositioning methods are exhausted, the controller may, in fact, alter correct data and send it to the host. ECC effectiveness relates directly to the clarity of the information given for correction.

Stepper-actuated drives use similar methods

Recovery mode is beneficial not only for high performance drives using voice-coil actuators, but it can also be used with drives employing stepper motor positioning systems. Although most steppers cannot fully implement micropositioning—part of their function is stepping one whole track with each movement—they can handle other recovery mode procedures. In the same read-error situation described for the voice-coil example, the controller for a stepper-based drive would still attempt several standard reads after the first read failed to work. If this approach fails to produce good data, the controller enters recovery mode as before and issues a step pulse to the drive.

At this point, the recovery method followed by the stepper-based drive differs from that of the voice-coil device. In this case, the drive responds to the first step pulse by initiating a recalibrate procedure, which returns the read/write heads to track 0 position. Then, the heads are sent to the problem track in order to allow the controller to attempt another read operation. If this read fails, the drive and controller can continue through the recovery operations. First, they can back off two tracks and reposition the heads from a positive direction. If this fails to recover the data, they can then move forward two tracks and reposition from a negative direction. As with the voice-coil drive, these movements attempt to overcome any hysteresis in the actuator mechanism.

These are some of the functions that a drive equipped with standard stepper motors can use to recover data mechanically. It is interesting to note that some of today's controllers already employ these techniques. Because no microstepping is required, the methods work equally well on any drive. To support higher track densities, some stepper motors now provide incremental track stepping (ie, one-quarter or one-half track steps). A possible contributor to offtrack errors in drives equipped with incremental steppers, in fact, is missing one of those increments in a series. This could leave the heads one-quarter track off—a fault that recalibration should correct. With incremental steppers, the drive could step the heads one-quarter track forwards and backwards from the problem track in recovery mode.

Recovery mode is one of two ST412 HP features that define two additional pinouts to the ST506/412 version. The other involves the head select lines, which determine the maximum number of read/write heads that a drive can use. Because high performance Winchesters can benefit from more than eight heads—the maximum number allowed by the ST506/412 interface—the ST412 HP increases the number of head select lines from three to four. Addition of this line doubles the allowable number of heads, making 16 heads available. When these additional heads are used, a high performance drive can access data faster and increase capacity. The control signal connector carries both head select and recovery mode lines (see Fig 2).

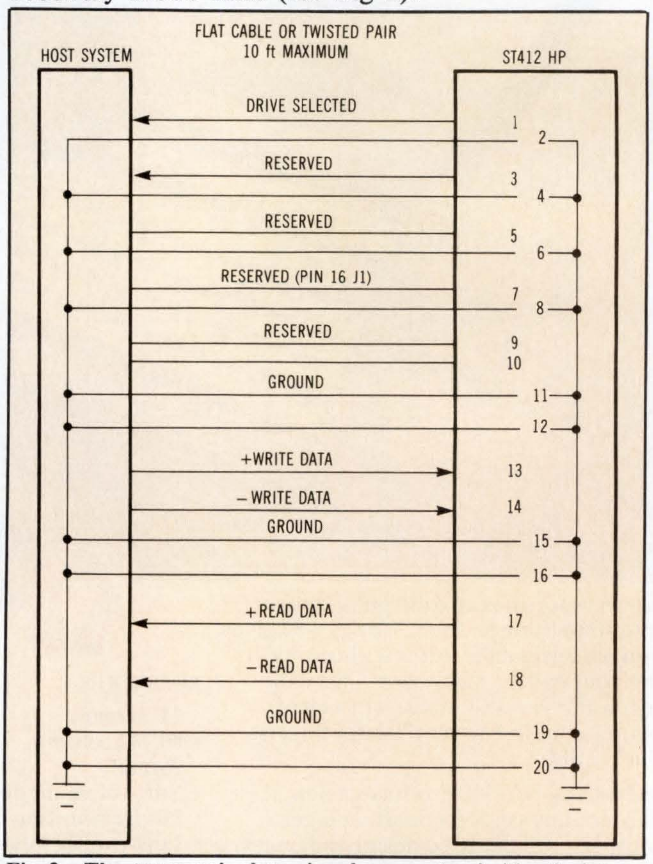

Fig 3 The ST412 HP's data signal connector is identical to that used in the ST506/412 version. The ST412 HP's maximum data transfer rate is higher, but that change does not affect the pinouts. However, the maximum cable lengths were reduced from 20 to 10 ft.

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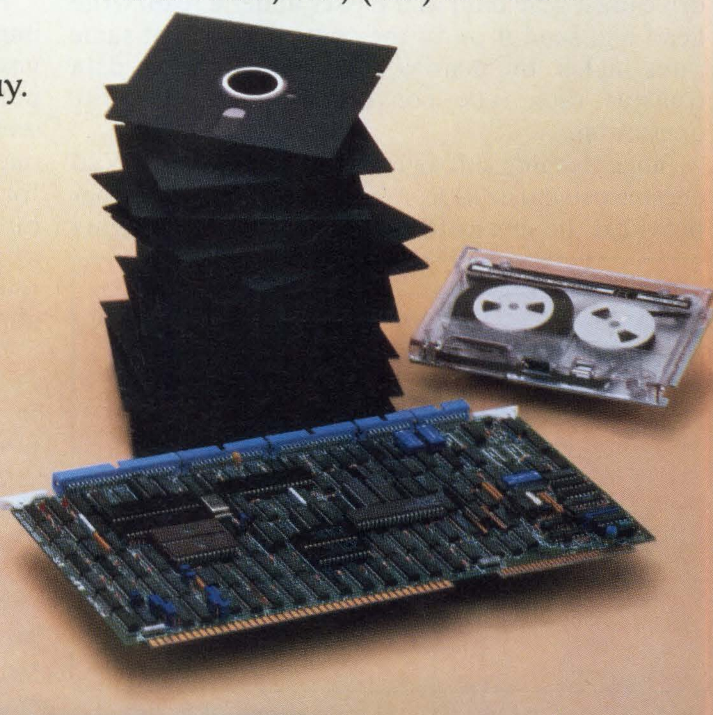

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CIRCLE 130

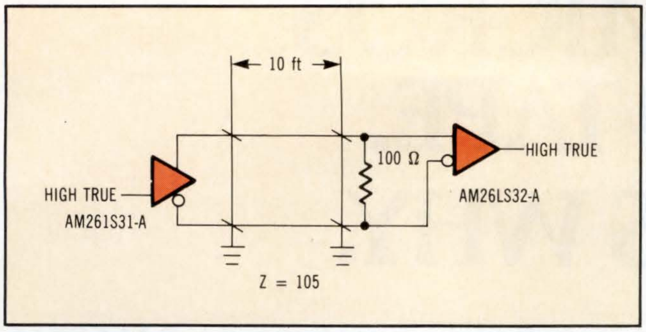

Fig 4 The data line driver/receiver combination used in the ST412 HP constitutes an EIA RS-422 driver/receiver pair, which employs flat ribbon cable or twisted-pair wiring. A proposed "Dash A" version specifies additional high performance parameters.

Another important change in the ST412 HP interface increases the maximum data transfer rate between the drive and its controller to 15 Mbits/s. The connector that carries read/write data and related signals, however, remains unchanged (see Fig 3). Although the maximum data rate has been increased, Winchester subsystems using the ST412 HP can transfer data at lower rates. In fact, the first drive manufactured by Seagate for use with the enhanced interface (the ST8100) transfers data at a 10-Mbit/s rate. This rate satisfies the needs of most second-generation small Winchesters.

While increasing the data rate does speed up the drive's data I/O, there is a more important benefit. Storage capacity is increased because bits can be recorded at a higher density in each track. Since the drive must read data as it passes under a read/write head and send it on to the controller at that same rate, higher bit density results in a higher data transfer rate. The converse is true for write operations.

Since Seagate introduced the first 5¼-in. Winchester drive (the ST506), improved technology has provided the means to record data at much higher bit densities. To maintain compatibility with existing interfaces, however, drives had to maintain the same bit density in order to use the same data rate. Thus, a valuable method of improving storage capacity was unavailable. Drives instead raised storage capacity through the use of alternatives such as increased track density and data-encoding schemes, which did not affect the data rate. By providing a higher data transfer rate, the ST412 HP clears the way for the use of higher bit densities to attain increased storage capacity, while maintaining compatibility with the standard interface.

Data transfer with the ST412 HP uses two pairs of balanced signals: write data and read data. For the write data differential pair, a flux reversal on the disk track results when the +write data line goes more positive than the −write data line, if write gate is active. For the read data pair, a flux reversal on the track of the selected head causes the +read data line to go more positive than the −read data line. The drive/receiver combination used for transfers both to and from the drive is depicted in Fig 4.

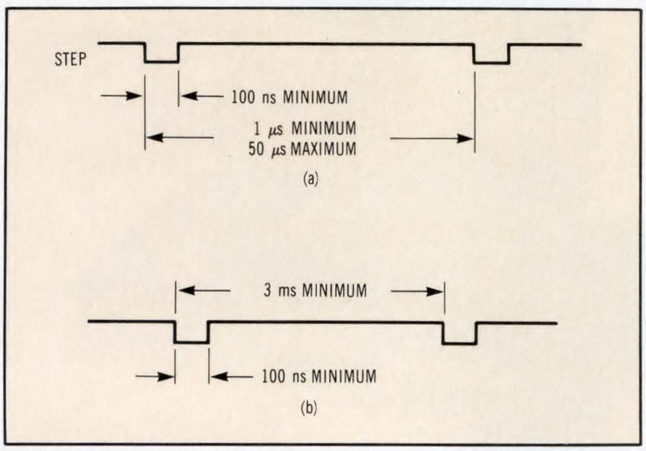

Fig 5 One of the two types of seeks permitted by the ST412 HP is a buffered version that lets the controller send a step pulse every microsecond (a). The second type of ST412 HP seek is a slow seek (b). Here the read/write heads move at the rate of the incoming step pulses—a minimum of every 3 ms.

Step pulse rate allows faster accesses

Another difference between the ST506/412 interface and the ST412 HP is the maximum rate at which a drive can accept step pulses. As with the data transfer rate change, the increase in the step rate does not alter the interface pinouts. In fact, the increase in step rate does not physically alter anything in the interface; it is a specification change only.

Here again, the change is necessary because of improvements in Winchester technology. Drives can now step faster, thanks to improved actuator technology. A buffered seek technique saves time on seeks when the heads must move several tracks at once. Rather than sending one step pulse and waiting for the heads to move before sending another pulse, buffered seek allows the controller to send a burst of pulses. This lets the heads traverse the distance to the selected track without settling at each track along the way.

A 5-μs minimum time between step pulses on a buffered seek and 3 ms on a slow seek is specified by the ST506/412. The ST412 HP specifies a 1 μs minimum on buffered seek operations to allow very fast access [Fig 5(a)]. The interface also reduces timing on slow seeks from 3 ms to 50 μs [Fig 5(b)]. The slow seek specification allows the heads to move at the rate of the incoming step pulses.

This change in the maximum seek pulse rate does not change the seek procedure from that specified by the ST506/412 interface. The seek procedure (see timing diagram in Fig 6) begins when the controller deactivates the write gate line and activates the appropriate drive select line with the drive in the ready condition and seek complete true (indicated by the ready and seek complete lines, respectively). Next, the controller selects the appropriate direction for the heads to move using the direction in line. A low on the direction in line causes a seek inward toward the drive's spindle; a high initiates a move outward toward track 0.

Then, the controller pulses the step line, causing the head to move one track either in or out on each pulse, depending on the state of the direction in line. On buffered seeks, the drive stores the pulses until it receives the last one (defined by a delay of 50 μs). It then executes the seek as one continuous movement.

When the controller begins sending step pulses, seek complete goes false. When this line returns true, the controller can select the required read/write head by placing that head's binary address on the head select lines. Now the controller can read data. If a write operation is needed instead, the controller must first ensure that no write fault conditions exist. It can then activate the write gate line and place data on the write data line.

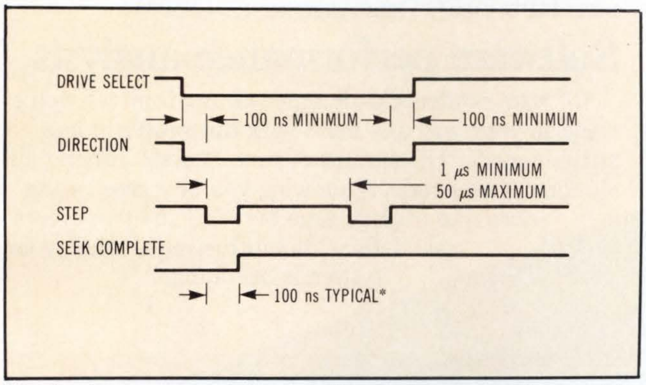

Fig 6 An ST412 HP seek operation proceeds exactly as with the ST506/412 interface. Note that the seek complete signal goes low 100 ns after the step pulse's leading edge.

Write fault is used by the drive to indicate a condition that could cause data to be improperly written if left uncorrected. The line monitors five conditions: a head receives write current without write gate active or there is no write current with both write gate and drive select active; multiple heads are selected or no heads are selected; dc voltages are grossly out of tolerance; write gate is active with no seek complete; and write gate (a last condition that results from the addition of recovery mode to the ST412 HP interface) is active while the drive is in recovery mode. A low on the write fault line indicates that the drive has inhibited further writing until the fault condition is corrected. The controller cannot reset write fault, it only monitors the line for the signal's appearance. The controller should edge-detect this signal.

The physical interface

The most important aspect of the ST412 HP's physical interface is that it is identical to that of the ST506/412 interface. The two connectors that are involved carry the control signals (J1) and the data signals (J2). J1 can be multiplexed in a daisy chain configuration. This connector mates with an edge

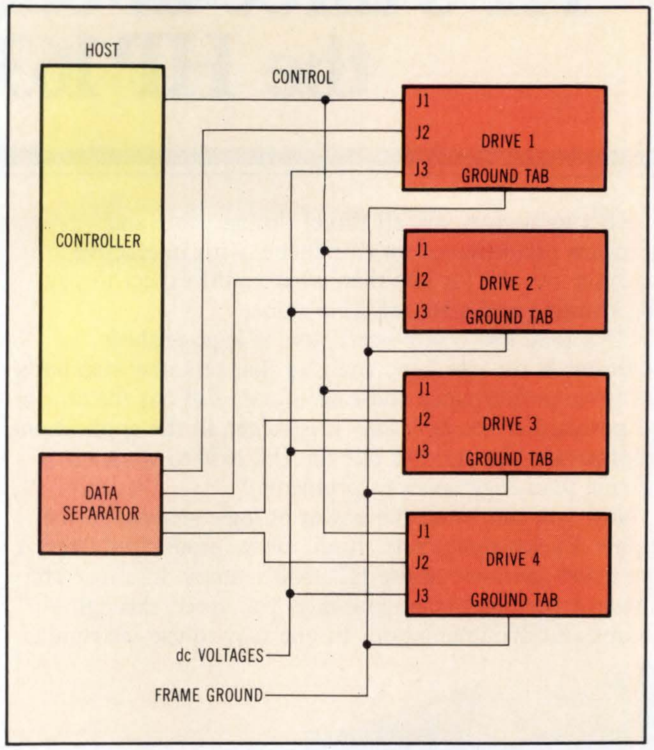

Fig 7 A typical connection for a four-drive Winchester subsystem shows the daisy chained control lines and radial data lines. Note that the data separator is part of the controller.

connector on the drive's PC board. Recommended connectors for J1 include AMP ribbon connector 88373-3 or Molex 15-35-1341. J2 is configured in a radial fashion. An edge connector on the drive's PC board also mates with J2. Recommended connectors are AMP ribbon connector 88373-6 or Molex 15-35-1201.

A typical connection for a four-drive Winchester subsystem (Fig 7) routes power inputs to the drives via connectors designated as J3. Note that the control lines between the controller and the drives are in a common connection, while the data lines connect radially between each drive and the data separator. The data separator is isolated here to emphasize both the radial arrangement and the signal separator requirement in multidrive configurations.

Whether a Winchester subsystem employs four drives or only one, the ST412 HP interface enables system designers to take advantage of very high capacity drives while maintaining standard interface compatibility. Thus, it offers versatility, opportunity for greater storage capacities, and an ST506/412-like interface that permits straightforward controller enhancements for standard designs.

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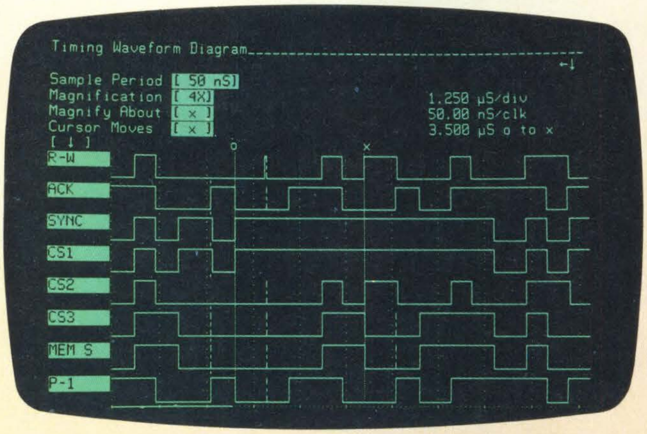

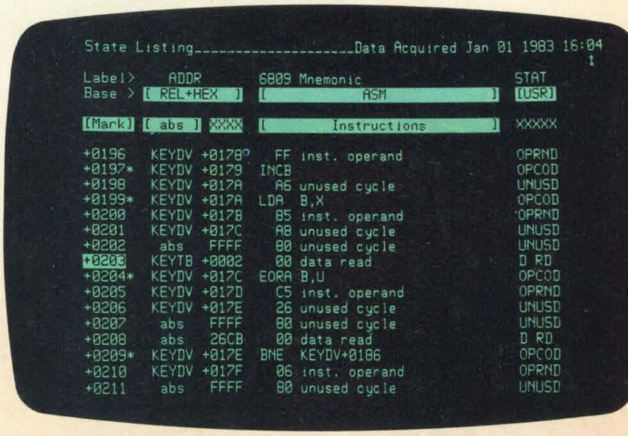

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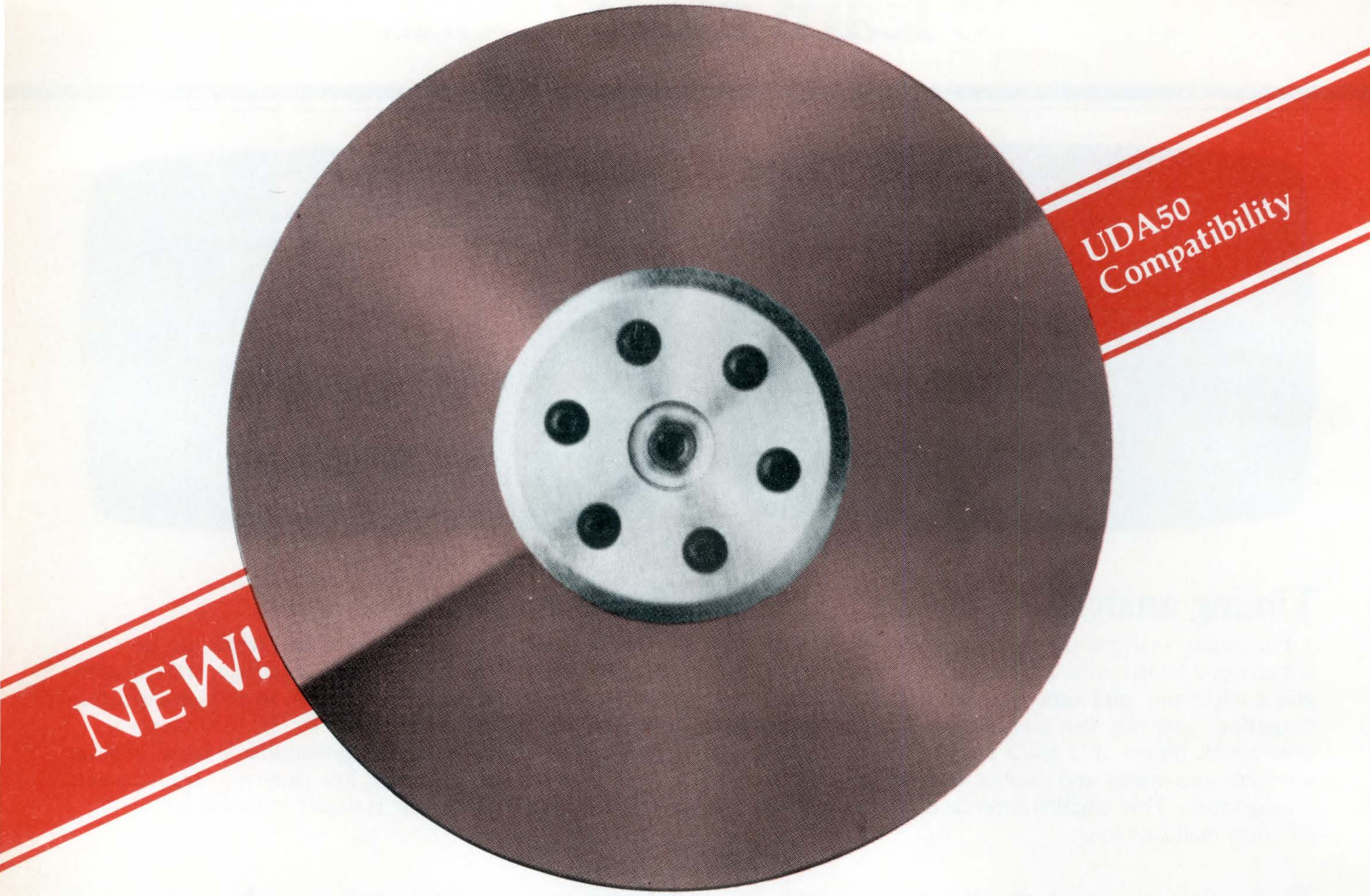

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CIRCLE 132

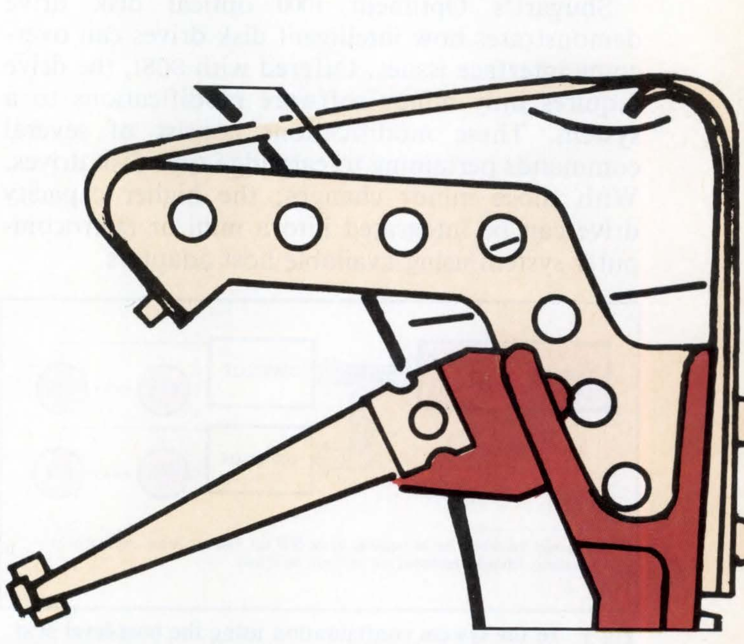
INTELLIGENT DISK DRIVES SIMPLIFY SYSTEM INTEGRATION

Freed from constraints imposed by device-level interfaces, designers concentrate on throughput rates and access times.

by Richard Freedland

A host of "intelligent" products are emerging in response to manufacturer demands for higher performance disk drives in compact, easily integrated packages. These drives are considered intelligent because they handle numerous housekeeping functions previously managed by the host CPU, (eg, formatting, data error detection and correction, and defect mapping). Such drives, including Shugart's 700S series of 5¼-in. Winchesters, accomplish this by implementing the Small Computer System Interface, an intelligent, host-level interface within the drive, thereby relieving the host of many tasks and allowing independence of the peripheral from the host CPU. This interface simplifies system integration and improves drive performance.

A broad range of disk drives are currently available. Those ranging in capacity from 125 Kbytes to 1 Gbyte are accessible to mini and microcomputer manufacturers. Fixed drives are offered with varying data rates, number of heads, heads per surface, and number of cylinders. Removable media disk drives range from the 3½-in. hard cartridge microfloppy diskette to 12-in. optical cartridge products. However, the lack of a standardized drive-level interface has hampered the use of this wide selection. (The most common disk drive interfaces for



Winchester-type drives are listed in Table 1.) This lack of a standard combined with the subtle differences between controller designs slows the evaluation process and the system integration task. Many manufacturers now test controllers and disk drives separately. Then, after the individual components are selected, they test the drive and controller again—as an integral unit.

Intelligent disk drives can solve this longstanding problem. By definition, these drives support a host-level, industry standard interface. The *de facto* host-level interface standard in the microcomputer industry is the Small Computer System Interface (SCSI). Initially introduced as the Shugart Associates System Interface (SASI), the SCSI allows system-level communication between the host computer and onboard intelligence within the disk

Richard Freedland is the product manager for intelligent disk drives and SCSI subsystems at Shugart Corp, 475 Oakmead Pkwy, Sunnyvale, CA 94086. He holds a BSEE from Syracuse University and an MBA from Golden Gate University.

TABLE 1			
Winchester Drive-level Interfaces			
Name	Transfer rate	Number of lines	Type of drivers/receivers
SMD	10.0 Mbits/s	60—control 26—read/write	differential
ANSI X3T9/1226	10.0 Mbits/s	50	single-ended or differential
SA4000	7.1 Mbits/s	50—control 20—read/write	single-ended—control differential—read/write
ST506	5.0 Mbits/s	34—control 20—read/write	single-ended
SA1000	4.3 Mbits/s	50—control 20—read/write	single-ended—control differential—read/write

drive. This combination of controller functions and Winchester mechanics eliminates the concern over drive-level interfaces. Controller manufacturers no longer need to build products with specific device-level interfaces. Computer manufacturers can use host adapters to the SCSI bus to easily integrate new products.

Shugart's Optimem 1000 optical disk drive demonstrates how intelligent disk drives can overcome interface issues. Offered with SCSI, the drive requires only minor software modifications to a system. These modifications consist of several commands pertaining to cartridge-type disk drives. With those minor changes, the higher capacity drive can be integrated into a mini or microcomputer system using available host adapters.

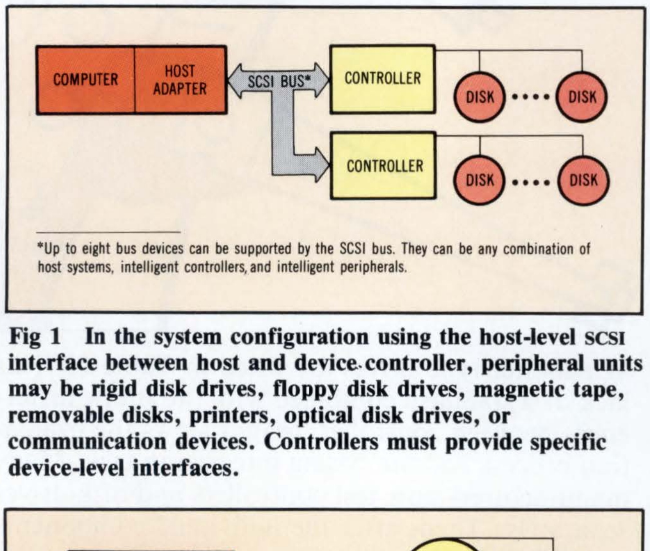


Fig 1 In the system configuration using the host-level SCSI interface between host and device controller, peripheral units may be rigid disk drives, floppy disk drives, magnetic tape, removable disks, printers, optical disk drives, or communication devices. Controllers must provide specific device-level interfaces.

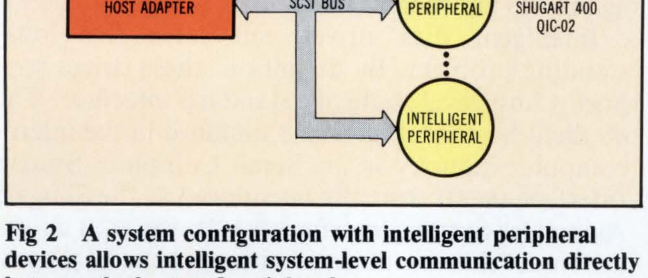


Fig 2 A system configuration with intelligent peripheral devices allows intelligent system-level communication directly between the host and peripheral.

Although system manufacturers primarily benefit from intelligent drives, disk drive manufacturers also gain advantages. Drives that offer device independence, simplified system integration, and high performance help speed customer acceptance. The ability to provide value-added products eases competitive pressures caused by reduced prices and profit margins. This greatly reduces the need to rely on outside vendors to provide controllers. Moreover, evaluation results are no longer affected by subtle differences in controller and drive products from different manufacturers. A comparison of Figs 1 and 2 illustrates the simplicity of a system configuration using intelligent devices.

Smart drives pay dividends

Implementing the SCSI in the 700S series provides intelligence through a low cost 8-bit microprocessor such as the Zilog Z8, with 8-Kbyte erasable PROM, which operates as the onboard processor within the drive. In conjunction with company-developed custom LSI controller devices that include the 1682 disk controller, 1681 buffer controller, 1683 encoder/decoder, and data separator subsystem, this 8-bit microprocessor forms the heart of the drive (Fig 3).

True device independence allows standard software to support present and future peripherals. The generic SCSI command set, including inquiry and read capacity commands, allows the selection of drives with different capacities, transfer rates, or removability characteristics (see Table 2). Drive parameters need not be downloaded from the host at each power-on or prior to dialogue with a different drive. Multitasking and multihost configurations may contain up to eight SCSI devices. The message system, attention signal, and message-out phase also allow host bus disconnect/reconnect capability in high performance systems.

Bus disconnect/reconnect is supported by the 1610-2 set of firmware. Other firmware sets support existing SCSI subsets. Because several subsets of the SCSI/SASI specification came into use prior to official recognition of the American National Standards Institute X3T9.2 SCSI document in 1984, various

TABLE 2

Generic SCSI Command Set

Inquiry command	Informs the host of the type of peripheral to which it is connected.
Read capacity	Informs the host of the address and size of the last block on the disk drive.
Write command	Transfers to the peripheral the specified number of blocks to be written at the specified logical block address.
Read command	Transfers the specified number of blocks starting at the specified logical block address to the host computer.
Request sense command	Returns to the host computer unit sense data perserved in the peripheral controller. The command originated in the host, complete with an error report.
Format unit	Ensures that the media are formatted so all data blocks can be accessed.
Mode select	Provides a means to specify media type, unit, or device parameters. The parameter list contains block descriptions specifying the number of blocks, block size, and density code.

firmware sets implement different command protocols. Firmware in a single 8-Kbyte EPROM upgrades the existing command set. This also allows system manufacturers to incorporate private-use SCSI subsets and thus inhibit or reduce the add-on disk drive market for their computers.

Write/verify and verify commands facilitate media certification. Hard or soft reset capabilities and command chaining are useful features. In a multitasking, multihost system, the soft reset option allows one host to reset the bus without disturbing the uncompleted commands from other hosts.

Media defects are handled at a sector level. Thus, the CPU can perform operations internally or with other devices while the SCSI drive is operating. This completely automatic approach makes defects entirely transparent to the user.

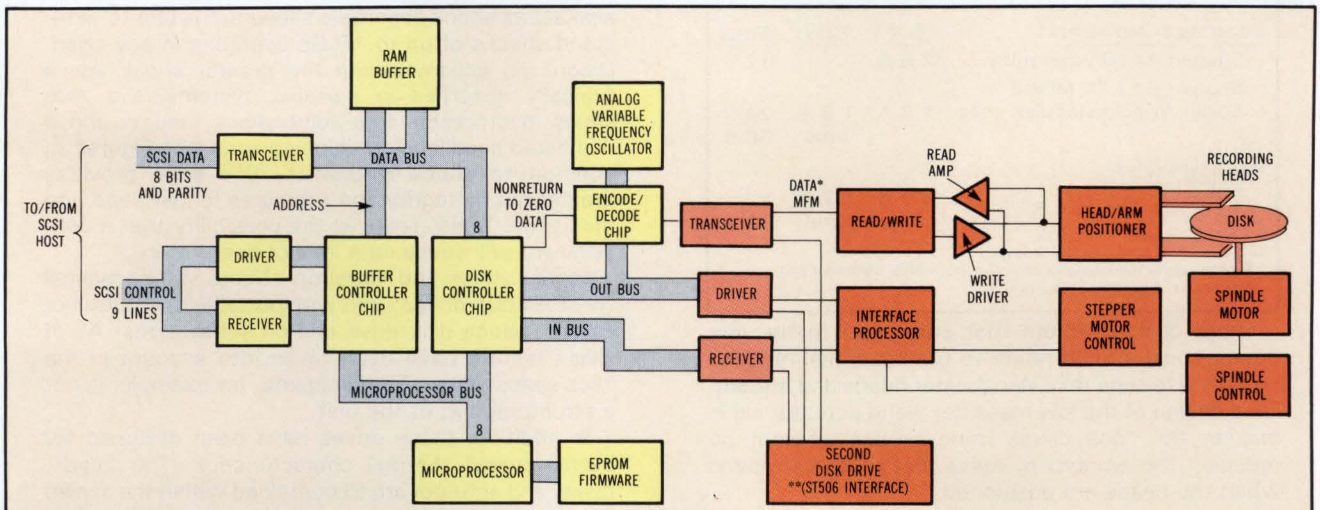
Each physical sector containing a media defect is replaced in logical order by the next physical sector (Fig 4). This minimizes access time by eliminating potential head access to an alternate cylinder or track. All error mapping information is stored on the disk itself, allowing the drive to be treated as continuous logical sectors. The user issues an initial read capacity command that returns the highest number logical sector in the unit, thereby providing the number of valid blocks available.

All block addressing is done on a logical basis. The user need not keep track of physical sector locations. The 700S series drives use 21- or 32-bit logical block addressing. Blocks (or sectors) may be 256,512, or 1024 bytes long. A single command can transfer up to 64,000 blocks, the equivalent of reading or writing an entire 16-Mbyte disk with one command (assuming 256 bytes/sector).

Detection and correction of soft errors within the drive are handled using a computer-generated, 32-bit polynomial. Providing powerful detection capability and 8-bit correction, this method is more efficient than common Fire code techniques. Correction takes place in an internal buffer; all retry and correction is transparent to the host.

Internal buffer speeds data transfer

An internal data buffering scheme promotes fast data transfers and absorbs differences in data rates



*Modified frequency modulation, frequency modulation or run-length limited.
**Future versions will permit QIC-02, or other drive-level interfaces.

Fig 3 An intelligent disk drive, as shown above, incorporates chip-level implementations of disk controller, buffer controller, encoder/decoder, and data separator subsystems, as well as an 8-bit microprocessor. These devices provide features that ease system integration.

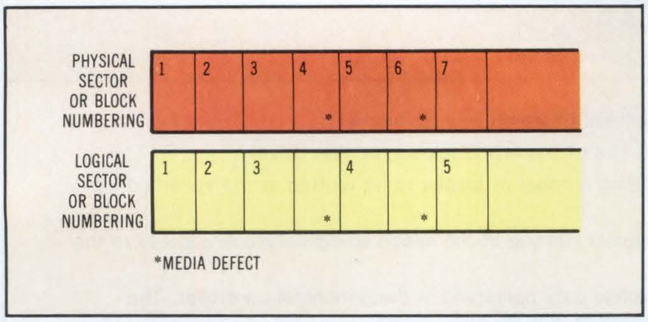


Fig 4 Media defects are handled on a sector level. Each sector containing a defect is replaced in logical order by the next physical sector.

between the host and the synchronous disk drive. Using a 1-Kbyte dual port circular first in, first out (FIFO) buffer for transfer speed, drives can support transfers at rates up to 1 Mbyte/s. (The buffer need not be filled before data transfer starts.) Data buffering also allows transfers of a full track of data within one revolution of the disk—called an interleave of one. Track-to-track seek time is 16.2 ms (less than the latency of a single revolution), thus allowing a full track to be transferred in a single revolution. Because of the buffer, a second nonintelligent disk drive can be handled within the 5-Mbit/s drive-level transfer rate. This second drive can have a different number of heads, cylinders, and disks.

By reducing reliance on drive parameters, the data buffer frees designs from constraints imposed by current and future drive-level interfaces. Since the system-level interface can handle various drive-level interfaces and transfer rates, higher capacity drives can be used. For example, if a technology or technique increases linear bit density by 50 percent, the resulting increase in transfer rate makes the drive nonstandard. An intelligent drive, however, can handle any transfer rate up to the SCSI maximum of 1.5-Mbytes/s with single-ended termination, or 4 Mbytes/s with differential controllers.

More about the 700S drives

Many factors contribute to the extremely low power requirements of the 700S. The use of LSI SCSI and data separator devices has reduced the number of discrete components. Located on the controller in previous configurations, the LSI implementation also allows the data separator to move inside the drive. Since it is closer to the read/write head, it provides more reliable signal handling and achieves better data integrity. It can also be incorporated in drive electronics. The chip count is 40 percent less than typical controller/drive combinations sold as separate components. The overall power requirements of an intelligent disk drive can also be 20 percent less than separate drive and controller units. Power requirements for various controller/drive combinations are compared in the Table.

Power Requirements Comparison

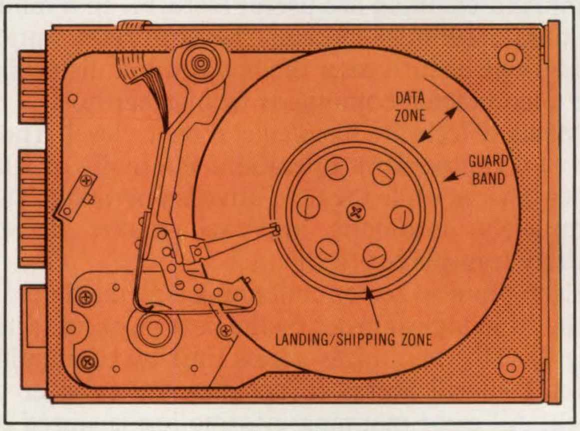
Separate components*	5 V	12 V	Watts
Shugart 1410A controller	2.5 A	—	12.5
Shugart 612 10-Mbyte 5¼-in. Winchester disk drive	1.2 A	1.5 A	24.0
		total	36.5
Intelligent drive			
706S	3.0 A	1.2 A	
		total	29.4

*Typical power requirements of similar SCSI/SASI controller and Winchester disk drive products.

Other design factors that contribute to the low power consumption relate to the head/disk module. Use of 3370-type mini-Winchester heads and streamlined design of the low mass flex-band actuator aid in making the 700S drives more power efficient by reducing the amount of mass that must be moved when the heads are positioned.

Added shock resistance

The 3370-type mini-Winchester heads provide the additional benefits of improved flying height and shock characteristics. The heads fly more uniformly from outer diameter to inner diameter than 3350-type heads. There is less chance of contaminants being lifted off the disk surface. Vibration isolators also act as shock absorbers allowing the unit to withstand shocks of up to 10 Gs operating in any orientation. To accommodate the greater shock levels typically absorbed in portable systems, the 700S series incorporates four-point shock mounts and a dedicated head landing/shipping zone (see Figure). In addition to shock resistance, this zone provides greater data integrity and promotes longer head and media life. It also reduces the possibility that a contaminant will cause data loss or head failure.



Higher shock and vibration effects will be typical for small disk drives used with portable computers or as standalone disk drive add-on subsystems. All of these factors have been taken into account in the 700S series drives. The faceplate, for example, is not a structural part of the unit.

In addition, these drives have been designed for better overall thermal characteristics. The heads, disks, and actuator are all contained within the sealed module to provide improved thermal stability. This series was designed so that all components are part of the drive's airflow system, designed to trap contaminants in a particle filter before air is returned to the disk/head area, a major improvement over most full-height 5¼-in. head/disk modules.

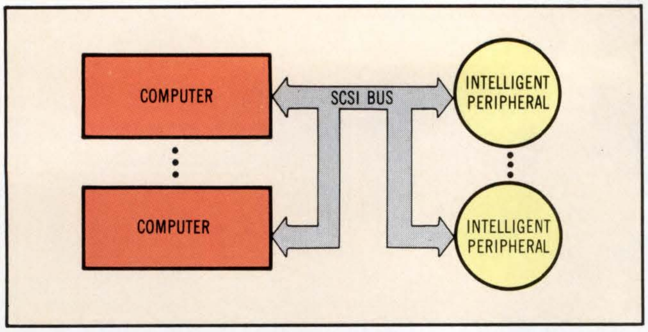


Fig 5 This future configuration includes embedded host adapters in multihost systems. Migration of the SCSI into the CPU's motherboard will eliminate the need for a host adapter board and allow direct connection of a peripheral to SCSI ports on the host.

Strong self-diagnostic capabilities ensure proper operation by providing easy yet significant self-tests. In the case of the 700S, each drive contains power-on and maintenance diagnostics for both the interface electronics and the mechanical head/disk assembly. Two separate microprocessors monitor and report on these areas, providing the data necessary to support reliability specifications.

The streamlined testing that intelligent drives offer yields subtle yet significant benefits. Since a drive contains all controller functions, it can be supplied with the customer's format and defect map already recorded. As a result, users need not write software to avoid media defects. Users can test the drive using single SCSI generic commands to determine type, capacity, and actual data storage provided. Incoming/receiving inspection by the computer manufacturers can be accomplished using small, portable SCSI test systems designed for that purpose. Forthcoming SCSI test systems will function as diagnostic analyzers and full field-capable test and repair stations. These systems will be able to verify, analyze, and diagnose SCSI interfaces from the host or peripheral standpoint.

Promise for a bright future

What do intelligent disk drives promise for the future? Within the next two years, both drive and SCSI electronics will merge onto a single PC board that will fit within the form factor of existing half-height 5¼-in. drives. This component reduction will be achieved using 2- to 3-micron VLSI device technology. Providing the potential to reduce the current three SCSI LSI controller devices to one, this VLSI technology will also make it possible to incorporate the data separator in the single SCSI controller device. Similarly, the electronic components of the read/write channel and the servo system/actuator arm can be placed in a single LSI device. Incorporating these functions into LSI or surface mounted devices (SMDs) will tremendously improve reliability. A related reduction in overall power consumption will further cut operating costs and enhance capability by minimizing heat dissipation.

Self-diagnostic capabilities of future intelligent drives will be expansive. Rather than the blinking LEDs common to today's drives and controllers, diagnostic data words will be available at the SCSI interface. Higher level diagnostics will go beyond spindle motor error detection and microprocessor registers into read channel activity. Drives will have the ability to write data to reserved cylinders and make comparisons to known inputs. This will allow the drive to verify proper operation of all data path elements from the head/media interface right up to the SCSI port. Improved diagnostics will detect head amplitude, media defects, spindle latency, and actuator arm problems. Temperature compensation schemes will be introduced to reduce the potential for data loss during environmental extremes.

While this merger of intelligent interface into disk drive electronics is taking place, the trend toward inclusion of SCSI ports on the CPU motherboard should also accelerate. The availability of SCSI host adapter chips, (eg, NCR's 5385 or 5386), will eliminate the need for a separate host adapter board (see Fig 5). This migration of the interface into the CPU will occur at the same time that SCSI generic software drivers are being written into the CPU's operating system. Thus, the inclusion of SCSI ports will allow intelligent drives of all types to be incorporated into a system without affecting controller electronics or operating system software. As SCSI chip sets reach higher volumes and thus drop in cost, intelligent drives will extend beyond Winchester and optical products to include removable media and floppy disk devices.

SCSI ports are not limited in use by mass storage devices such as disk and tape drives. These ports can also be applied to printers, plotters, modems, and other peripheral or communication devices.

Using the SCSI port will let computer manufacturers concentrate on hardware and software to increase the computer's utility. It will free peripheral manufacturers to concentrate on reliability, manufacturability, and price/performance. Thus, the intelligent drive approach promises a more definite future. Integrating computer peripherals into systems will not be the painstaking effort it is today. The disk drive industry trend to "plug and play" peripherals will offer a competitive edge to computer manufacturers who accept the intelligent drive approach to higher performance, simplified system integration, and device independence.

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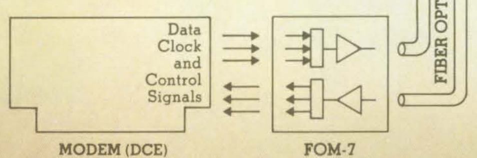

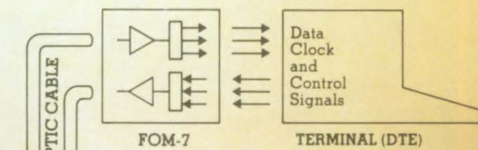

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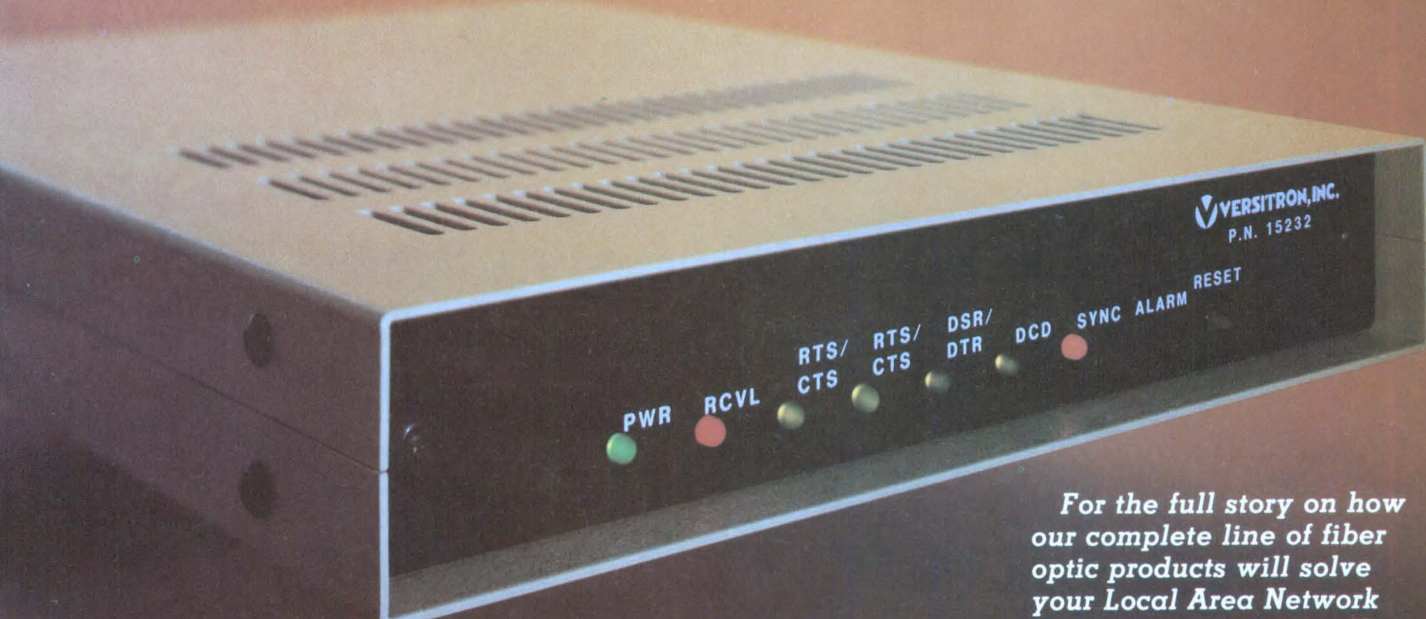

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CIRCLE 134


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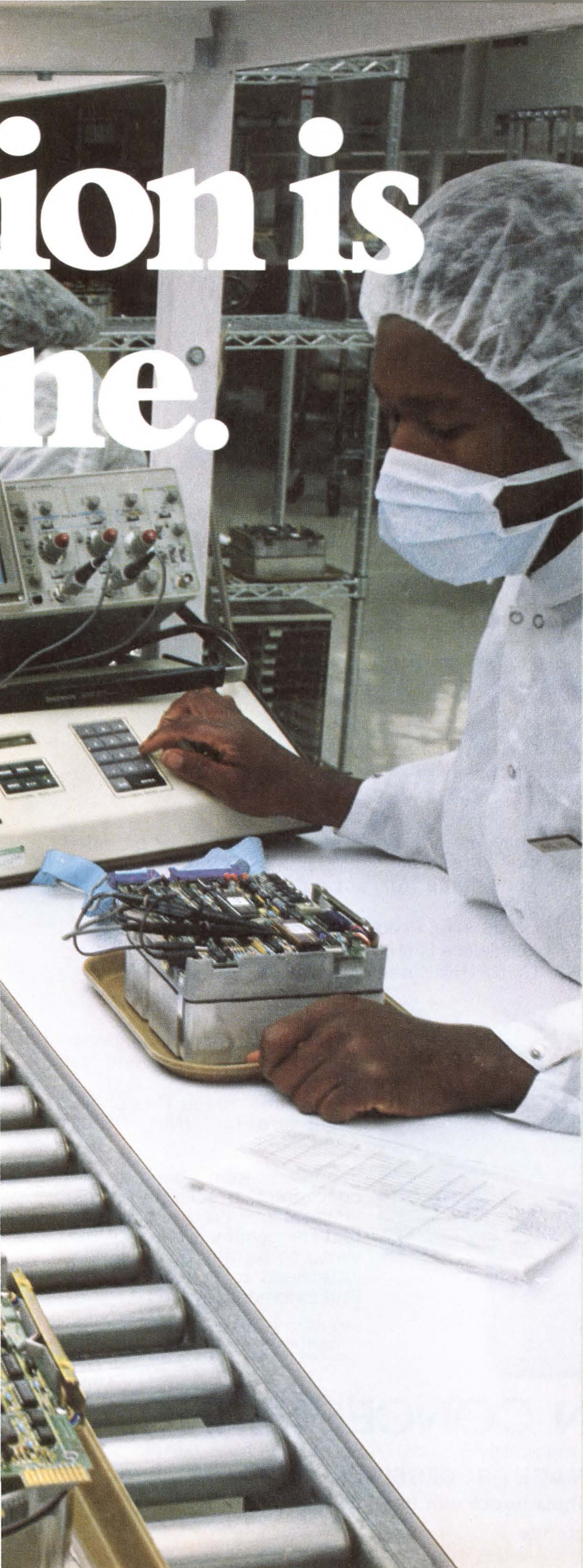

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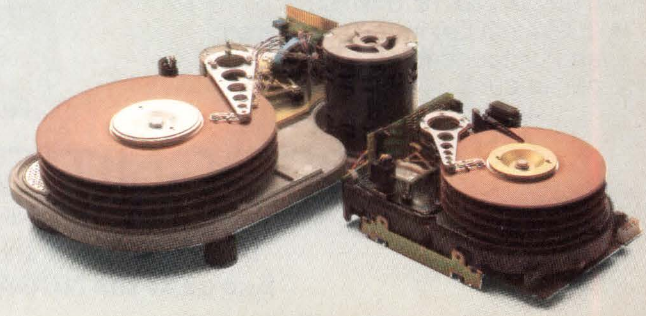
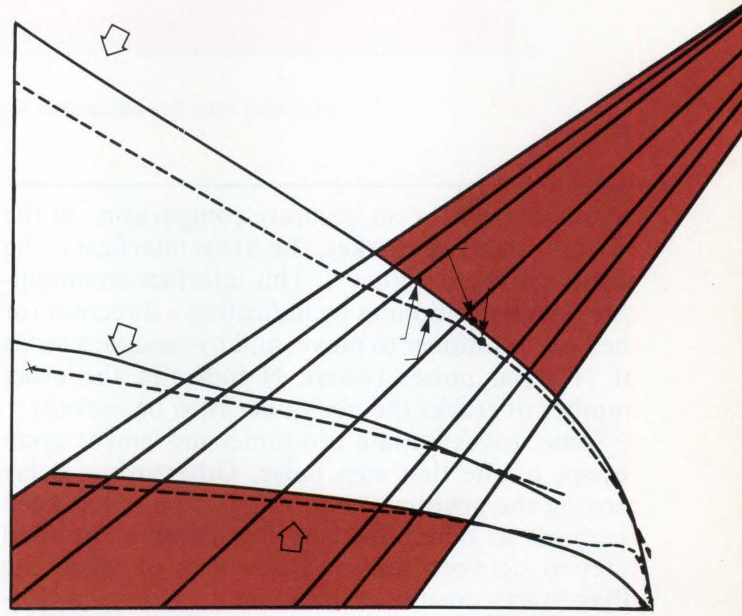


CIRCLE 135

SPECIAL REPORT ON DISK MEMORY

COMPARING SPECS—EASIER SAID THAN DONE

An accurate comparison of 5¼-in. disk drive performance specifications hinges on a detailed understanding of what is being specified, as well as what is not included in the specification.



by Tony Maggio

An important factor in choosing a high performance rigid disk drive is its seek time—the average time required to perform a seek to a cylinder of stored information. Although data file optimization can enhance system performance, a drive's raw average seek time determines its basic capabilities. Therefore, average seek time is one of the most significant parameters to consider in measuring and comparing disk drives.

All manufacturers' drive specifications include values for track-to-track, average seek, and maximum seek times. However, comparing these specifications does not necessarily result in a reasonable comparison of seek performance between two drives. Moreover, several factors significantly influence overall seek time measurements and comparisons. These factors include head positioning time, when to start counting, head settling time, latency, servo lock time, the capacity being accessed, and whether the specifications are for "maximum" or "typical" values.

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Positioning time is the time required to move the head positioner from its current track position to a desired track. If the data to be accessed is on the same cylinder as the last seek command, no time is required. Factors such as direction of seek, drive orientation, drive power supply levels, and operating temperature can affect positioning time. The exact seek time profile, covering all possible seek distances from a single-track seek to the maximum seek distance, determines the overall positioner performance.

Factors to consider

To determine overall positioner performance, it is important to know when to start counting. Knowing how the drive manufacturer specifies positioning

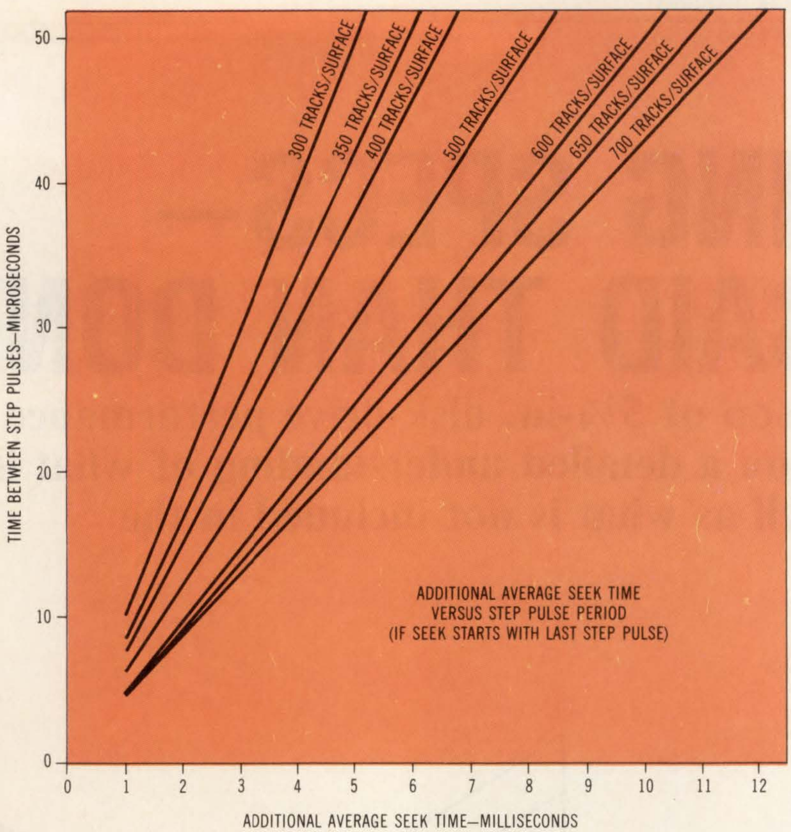

Fig 1 Actual head positioning time can vary from that specified, depending on whether the first or last step pulse initiates positioner movement. Drives that wait for the last step pulse before starting a seek have an additional average seek delay, as shown for a range of step pulse rates and maximum tracks/surface.

time is critical for an accurate comparison. In the 5¼-in. rigid disk market, the ST506 interface is the current *de facto* standard. This interface communicates track positioning by indicating a direction for the head positioner to move, and by sending a series of N serial pulses (where N indicates the exact number of tracks the positioner is to be moved).

Some drives initiate positioner movement upon receipt of the first step pulse. Other drives delay moving the positioner until the last pulse has been received, as determined by a maximum specified interval between pulses. Regardless of when the drive starts positioner movement, system performance is affected starting with the first step pulse. Measuring positioning time from the first or last step pulse at the drive level is debatable. However, to accurately compare positioning time between drives, all drives must be measured from the same starting point.

Unfortunately, many manufacturers' specifications do not indicate whether the first or last pulse is used to determine specified positioning time. Depending on the step pulse rate used and the maximum tracks/surface, this single factor could typically add at least 1 to 4 ms to the specified average seek time on drives having 600 or more tracks/surface (see Fig 1).

Another factor influencing positioner timing is settling time. This is the time required for the positioner to settle from overshoot or resonance after reaching the destination track. Varying from drive to drive, this is a once-per-seek event. Unless specifically stated, settling time may or may not be included in the manufacturers' specified seek time. This factor alone may add 3 to 15 ms to all specified seek times (track-to-track, average, and maximum), depending on whether or not the manufacturer has included it in the seek time specification.

Latency is the time required for one disk revolution. One-half revolution is the average time it takes to reach the desired sector after the positioner has arrived at the desired track. Thus, this factor could be significant in determining total access time. Almost all 5¼-in. rigid disk drives with 5-MHz transfer rates, however, rotate at 3600 rpm, which allows this parameter to be ignored in comparisons. An exception is when the drive being considered uses an embedded (wedge) servo for final positioning.

Servo lock time must be considered in drives using a wedge servo. This is the time required for the positioner to lock on track prior to reading and writing. Some drives use a wedge servo to determine fine positioning of the actuator. Typically, the servo burst is available only once per revolution. Some drives require more than one revolution before final positioning is established. Since latency time (16.67 ms) in 5¼-in. rigid disks is significant relative to the seek time, this factor must be taken into account when comparing the wedge servo drive seek times.

Obviously, drive performance relates directly to the average time required to seek over its total capacity. If the capacities of two or more drives are equivalent, comparison of their specified seek times may be valid. However, if one drive has a capacity of 30 Mbytes and another 35 Mbytes, it is incorrect to directly compare specified seek times. For example, if both drives have specified average seek times of 35 ms, the drive accessing 35 Mbytes has a higher system performance since it can access more information in the same amount of time as the 30-Mbyte drive.

To make valid comparisons, an equivalent storage capacity must be determined. The maximum cylinder to be addressed should then be adjusted for each drive to match the desired total storage capacity. For example, a 30- and a 35-Mbyte drive may both have five data surfaces and the same track capacities, and 30 Mbytes may be the system capacity requirement. For that 30-Mbyte range, the 35-Mbyte drive has roughly a 17-percent seek performance advantage over the 30-Mbyte drive, even though both drives have a 35-ms specified average seek time. If the 35-Mbyte drive has a linear seek time profile, its effective average seek time for the desired 30 Mbytes could be 29 ms instead of the manufacturers' specification of 35 ms.

When comparing average seek times, all drives should be measured at the same drive capacity. This can usually be done by adjusting the maximum number of tracks/surface on the larger capacity drives.

"Maximum" versus "typical" values

Before comparing manufacturers' specified seek times, it is essential to know if the values are guaranteed "maximum" or "typical." Typical seek values are generally specified under nominal voltage, temperature, and drive orientation. These values portray a representative sample of manufactured drives (ie, some faster, some slower). Differences in parts alone can cause a variance of from 3 to 5 ms from the specified typical average seek value. Moreover, larger variances can be expected if orientation, temperature, and voltage extremes are introduced.

Maximum values, however, should be stated under worst-case conditions of voltage, temperature, and drive orientation. These values ensure that all drives shipped are equal to or better than the specified value. Consequently, it can be misleading to compare one drive's typical to another drive's maximum values. Unfortunately, many manufacturers do not indicate whether their values are typical or maximum.

A drive's raw average seek time determines its basic capabilities.

Considering all of the above, the best way to compare drive seek times is to measure drives from different manufacturers and compare the results. But, even drive testers and systems differ in how they make an average seek time measurement: there can be significant differences when measuring the same drive on different testers. Some of this variance can be explained by differences in algorithms used to measure average seek time.

Test time required to accurately measure average seek time can be substantial, considering the number of possible seek combinations that must be exercised. To shorten test time, some test equipment manufacturers take shortcuts to estimate average seek time.

For example, the Applied Data Communications (ADC) T-650 tester measures the time to seek over one-quarter of the total tracks on a surface. The Wilson Labs MWX1000 tester, on the other hand, measures the time to seek over one-third of the total tracks on a surface. Both testers rapidly

TABLE 1

Manufacturers' Specifications

	WREN-9415	Brand X
Drive capacity (three-disk model)	36.2 Mbytes	33.6 Mbytes
Track capacity	10,416 bytes	10,416 bytes
Tracks/in.	800	800
Tracks/surface	697	655
Single-track seek	9 ms	3 ms
Average seek time	45 ms	30 ms
Seek settling time	(included in average seek time)	3 ms
Seek specification	maximum values	typical values
Positioner moves with	first step pulse	last step pulse

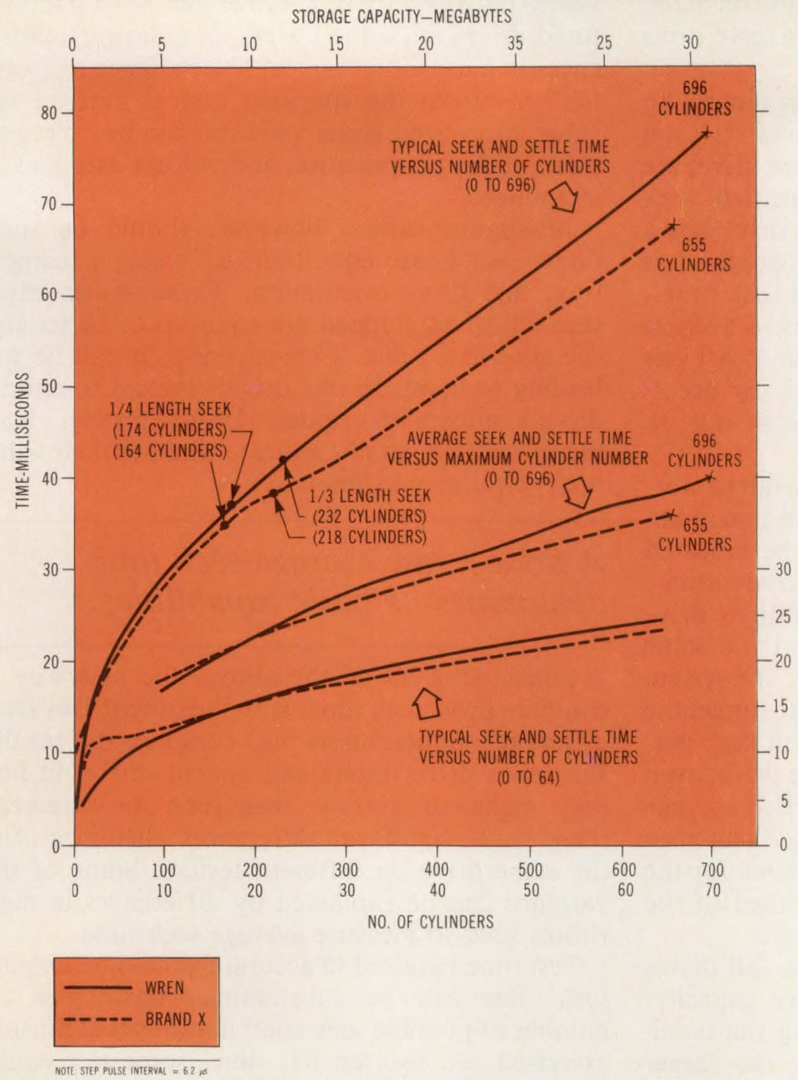

Fig 2 Seek profile measurements made on two disk drives allow the average seek and settle times for specific seek distances to be compared.

measure positioning time over a certain number of cylinders. However, results cannot be reliably compared to each other or to the manufacturers' drive specifications for average seek time.

Measurement comparisons

It can be shown mathematically that the average distance of all possible seek combinations approximates almost exactly one-third the maximum seek distance. If seek time versus distance were a linear function, this time would be an exact measurement of average seek time. For most drives, however, seek time is not linear over the total seek distance. Therefore, the one-third stroke measurement may be close for some drives, but not for others.

TABLE 2

Seek and Settle Time versus Number of Cylinders

Seek distance	WREN-9415	Brand X
0 to 10 cylinders	Faster	
11 to 100 cylinders	—Approximately Equal—	
101 to 655 cylinders		Faster
Measured (average seek time) (655 cylinders)	38.6 ms	36.0 ms
Manufacturers' specifications (average seek time)	45 ms (maximum)	30 + 3 = 33 ms (typical)

A comparison of two high performance 5¼-in. drives demonstrates the differences that can exist between manufacturers' specifications and measured seek times. For this comparison, a Control Data Corp (CDC) WREN-9415 and a competitive drive (brand X) were selected at random. Seek times were measured on various testers under nominal conditions. Manufacturers' specifications for the two drives are given in Table 1. In this comparison, there appears to be a 15-ms difference in average seek time: brand X seems to be 33 percent faster.

The seek profiles obtained on a Magnetic Peripherals, Inc test system measuring the WREN-9415 and the brand X drives (Fig 2) display seek performance comparisons between the two drives. The relationships are shown in Table 2. Measurements indicate that there is only a 2.6-ms difference in average seek time. In addition, the WREN is shown to be faster on short seeks.

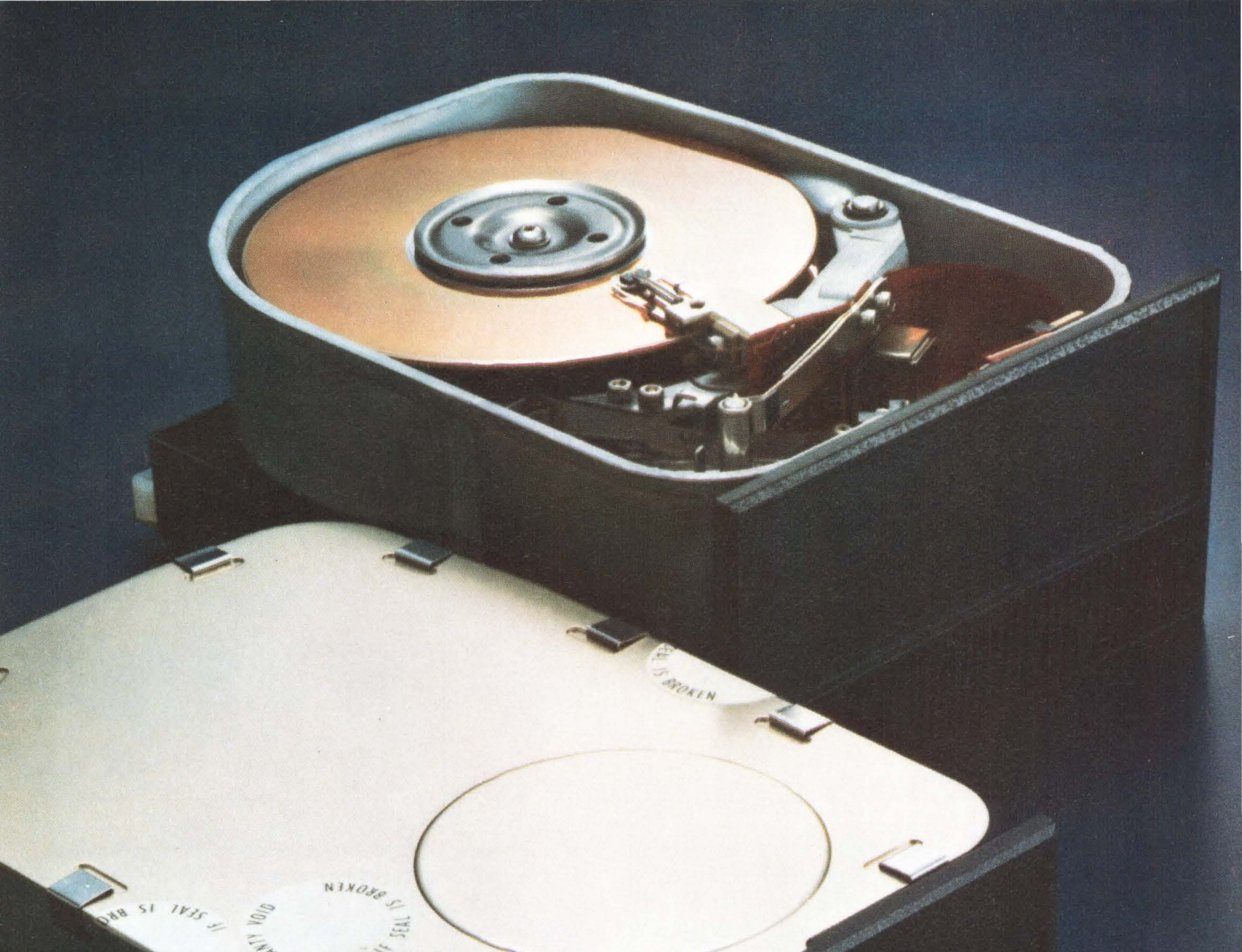

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TABLE 3

Measured Parameters versus Manufacturers' Specifications

Manufacturers' specifications		ADC T-650 tester (15.5-μs step)	Wilson Labs MWX1000 tester (20-μs step)	Magnetic Peripherals test system (6.2-μs step)	TRS80-II/ XEBEC-S1410 (15-μs step)
Average seek time		(1/4 stroke)	(1/3 stroke)	(Average all combination seeks)	(Average random seeks)
WREN					
697 cylinders	45 ms (maximum)	37.4	41.1	40.0	39.9
655 cylinders		36.3	40.8	38.6	39.1
Brand X	30 ms seek	36.7	42.5	36.0	37.6
655 cylinders	3 ms settle				
	33 ms (typical)				
Maximum seek time					
WREN					
697 cylinders	90 ms (maximum)	79.2	78.5	77.9	78.0
655 cylinders		75.7	74.9	74.6	75.0
Brand X	70 ms seek				
655 cylinders	3 ms settle	76.5	79.6	67.7	72.5
	73 ms (typical)				
Single-track seek					
WREN	9 ms (maximum)	3.6	4.1	4.2	3.6
Brand X	3 ms seek				
	3 ms settle				
	6 ms (typical)	8.8	8.6	8.6	8.6

Then, the two drives were tested on four different test systems (see Table 3), which determine average seek time in different ways. The Magnetic Peripherals test system calculates the average seek time by measuring the time to perform all possible combinations of seeks and dividing by the total number of seeks performed. The ADC T-650 tester measures the time to perform five seeks in each direction, where each seek is equal in distance to one-quarter of the maximum seek distance. It then divides this time by 10 and presents the results as average seek time.

The lack of uniformity in specifying seek times demands that manufacturer specifications be questioned in depth.

The Wilson Labs MWX1000 tester supplies an average measurement of a number of seeks, where each seek is equal to one-third of the maximum seek distance. And, the TRS80-II/XEBEC-S1410, a typical small system, has been programmed to measure the time to perform 10,000 seeks to random cylinder addresses between zero and maximum cylinder. It divides the total time by the 10,000 seeks.

There are noticeable differences in the results of these comparisons. Also, the measured seek times differ significantly from the manufacturers' specifications for the two drives. Although the measurements vary from tester to tester, the average seek times for the two drives measure very close to each other on all testers when compared at the same capacity (655 cylinders). Measured average seek times are much closer than the 15-ms difference indicated by the manufacturers' specifications. On all four testers, the WREN measured more than twice as fast as brand X on single-track seeks.

An accurate comparison of drive seek times requires careful choice of how and with what information the comparison is made. Taken at face value, manufacturers' specifications can be misleading. The lack of uniformity in specifying seek times demands that manufacturers' specifications be questioned in depth. What is specified, as well as what is not included in the stated specifications, must be clearly understood before accurate comparisons can be made.

The best possible way to evaluate and compare drives is to use an operating system and a benchmark program that are representative of the final system application. This approach will provide the most accurate measure of actual drive performance.

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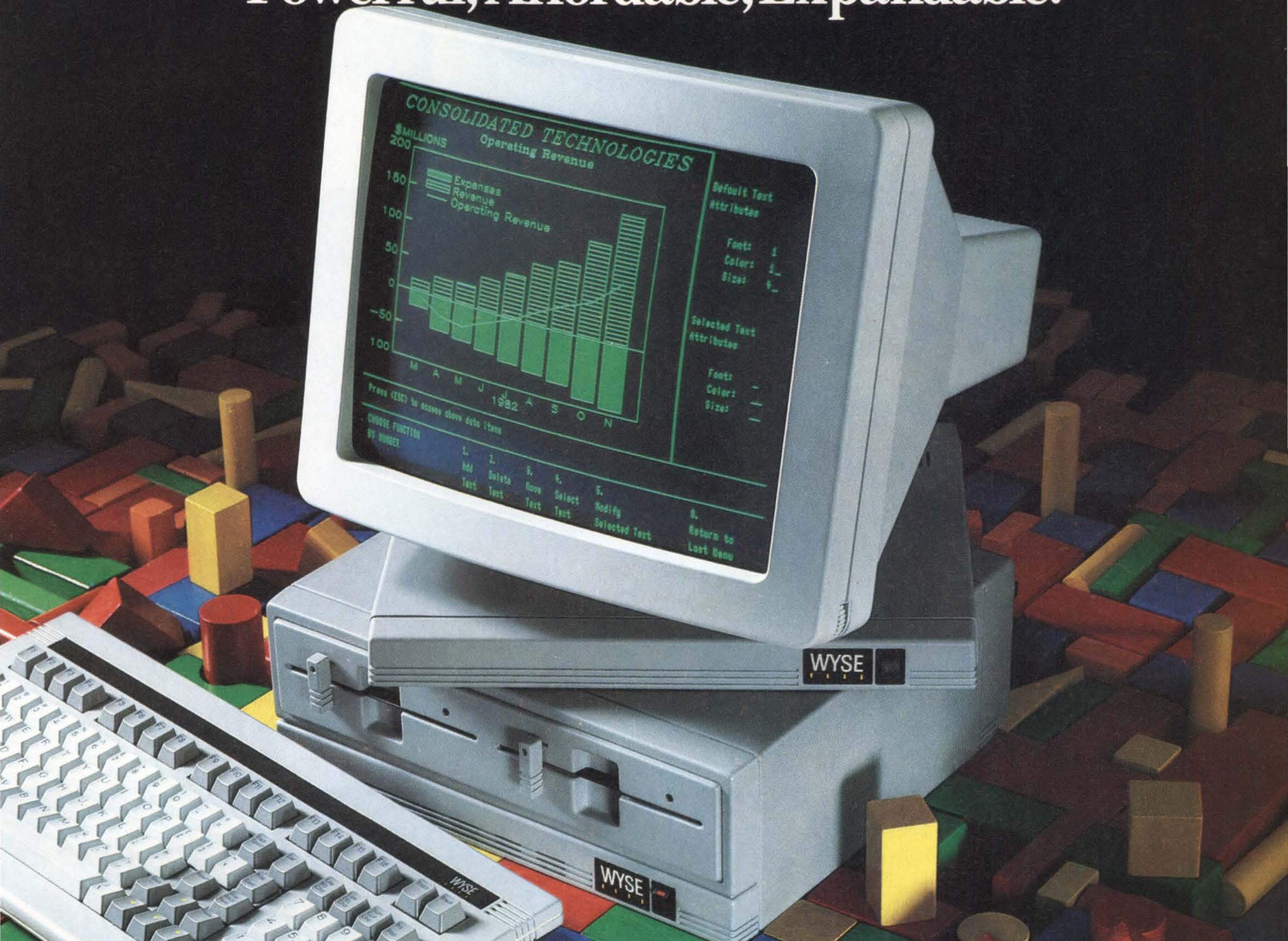

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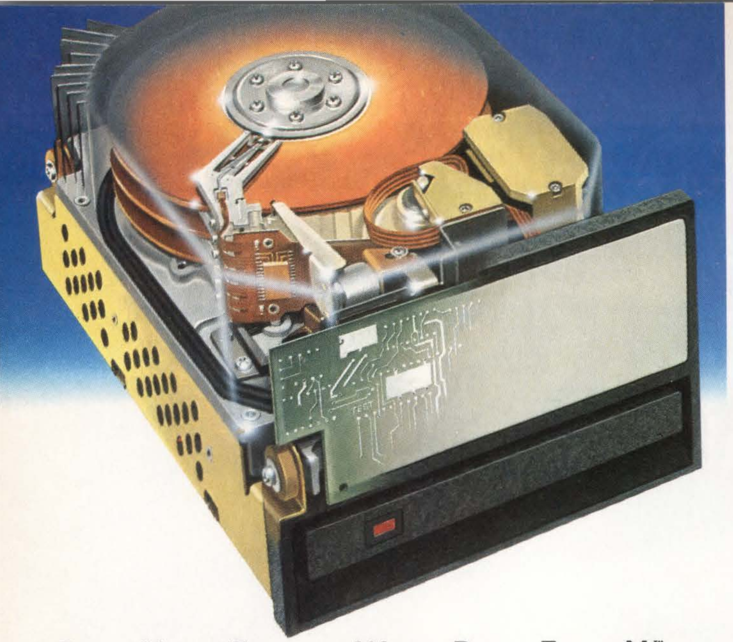

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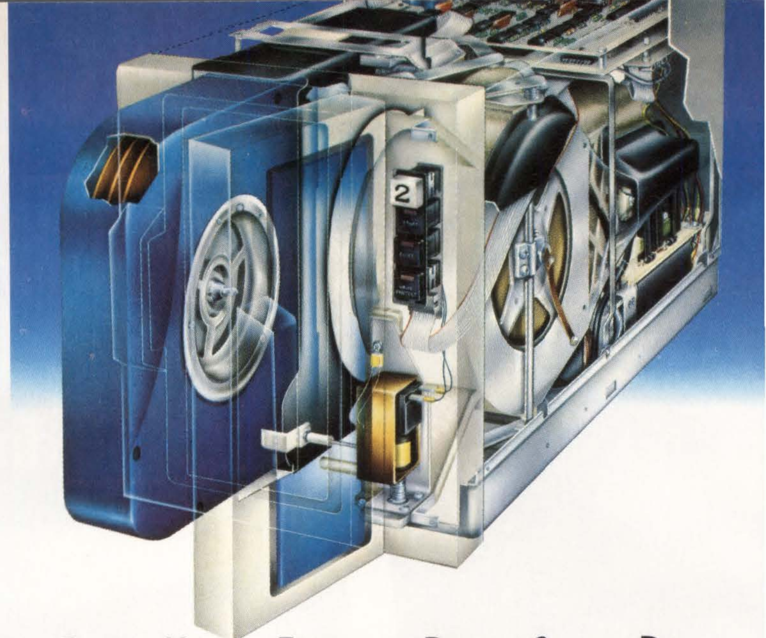

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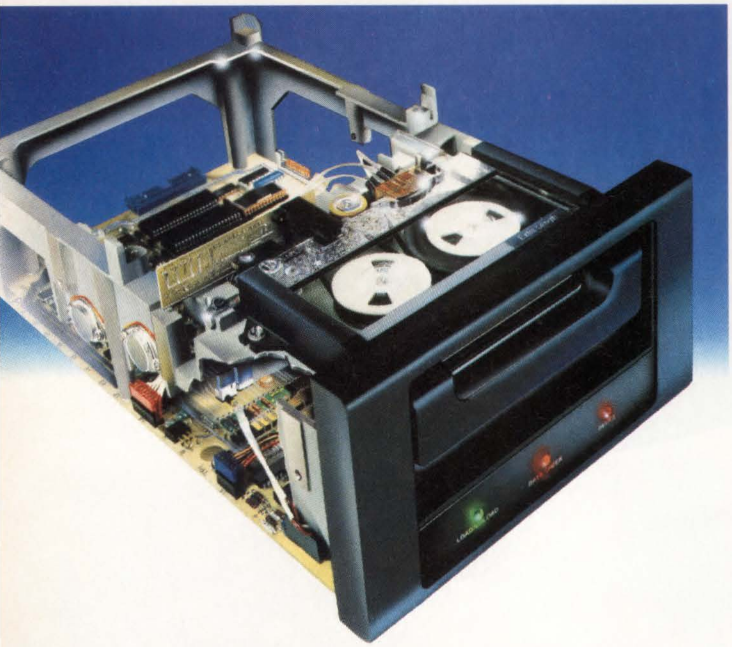

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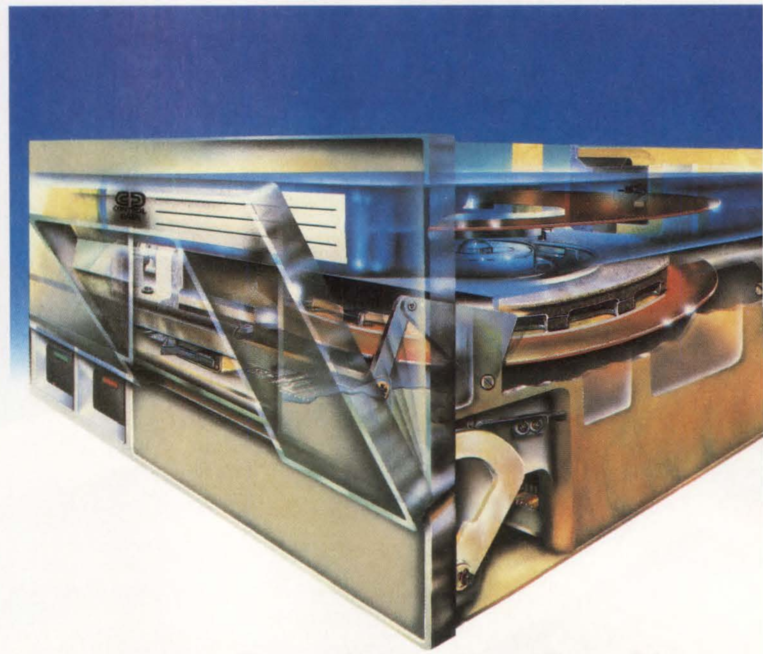

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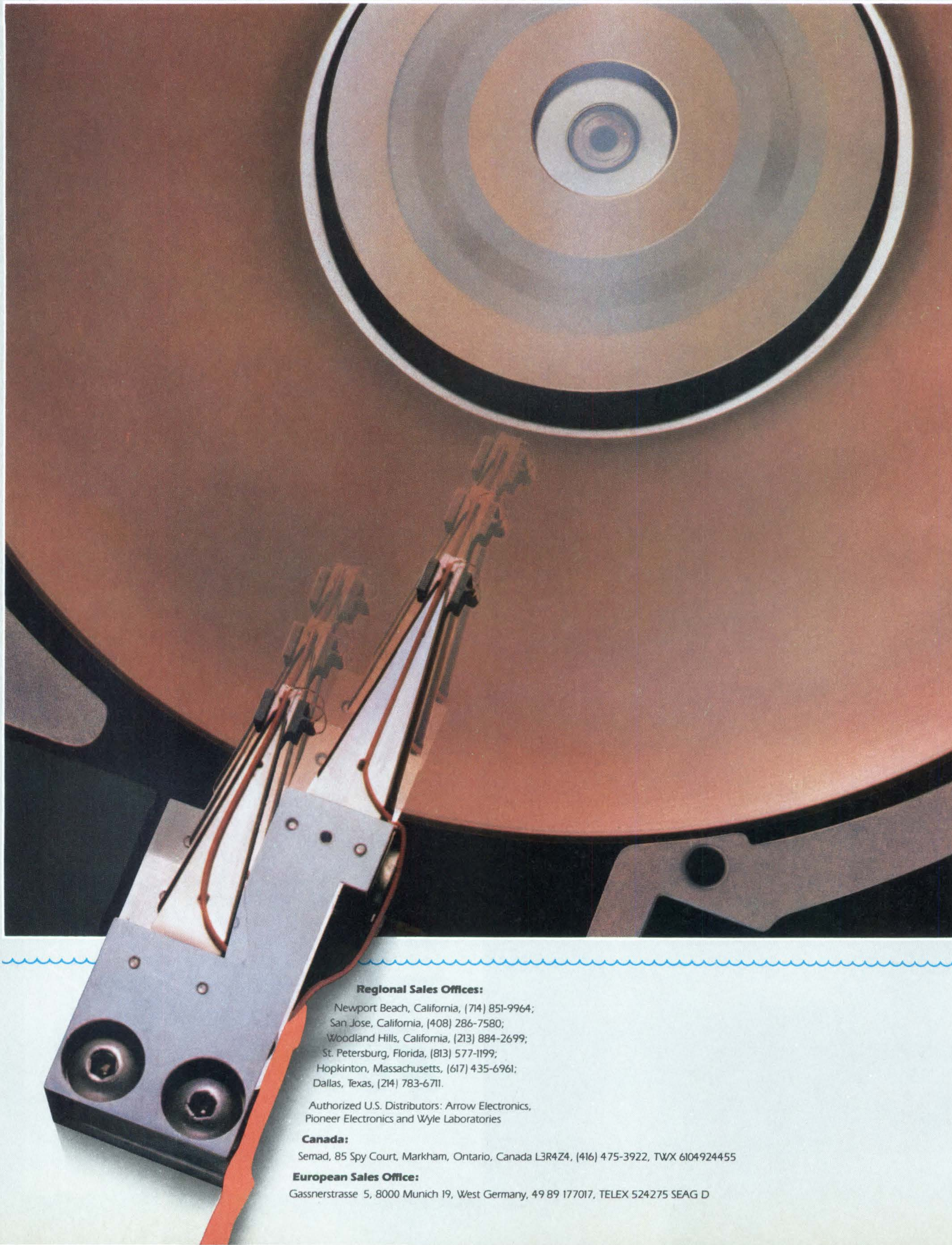

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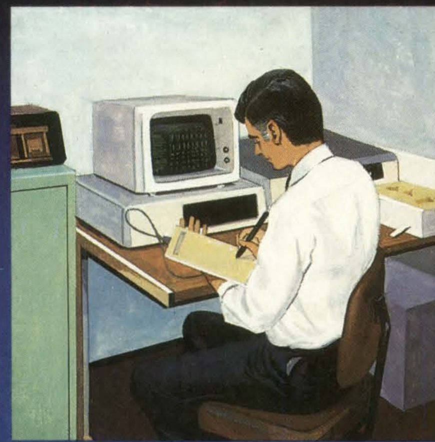

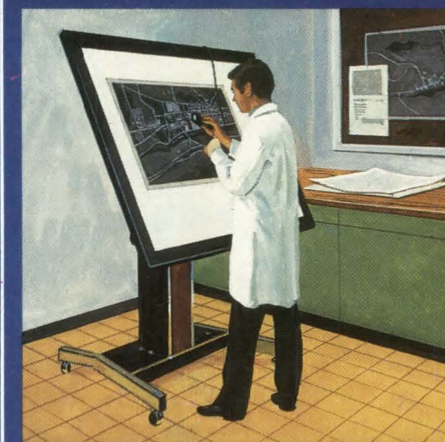

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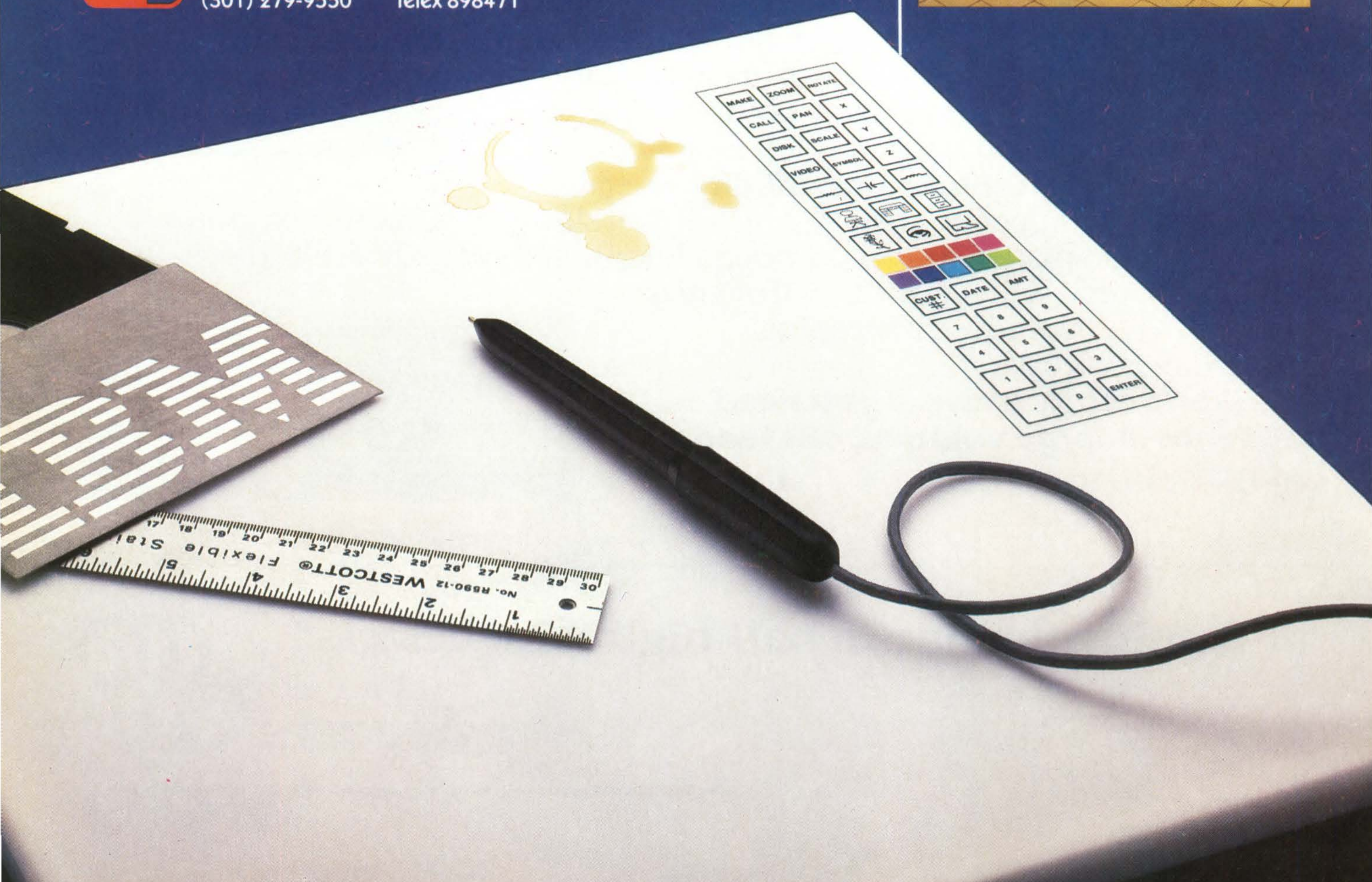


CIRCLE 142

THIN-FILM MEDIA MEET INCREASED STORAGE DEMANDS

Mechanical properties and magnetic characteristics of thin-film media combine to meet today's high density storage needs and promise potential for next-generation recording technologies.

by James H. Smith

Traditionally, Winchester-type rigid disk drives have relied upon iron oxide particulate media. The rigid disks used in such devices consist of a 0.075-in. (0.190-cm) thick aluminum substrate that is stamped from aluminum sheets and then machined. The magnetic coating applied to this substrate is usually a mix of iron oxide particles, a wear-resistant material such as aluminum oxide, and an epoxy binder. Typically, 20 to 30 μin. thick, the magnetic coating fills in surface irregularities within the substrate. A lubricant overcoat is then applied over the magnetic coating (Fig 1).

In the manufacturing process, the iron oxide particles within the magnetic coating are oriented in one direction during the epoxy curing process to provide a uniform, basic magnetic orientation. During recording, the read/write head can flip these magnetic domains to change their magnetic orientation. These flux reversals represent the written digital data in the form of N-S pole orientations that are defined as "1s" or "0s."

Typically, thin-film media disks also consist of a machined aluminum substrate that is first plated with 300 to 600 μin. of electroless nickel, and then polished to provide a flat, hard surface. A 3 to 4 μin. thick magnetic coating is then applied. Usually a cobalt/phosphorous or cobalt/nickel/phosphorous layer, this coating is applied using one of several deposition techniques. A surface overcoat on top of this protects the disk from corrosion and lubricates it against abrasion.

No matter what deposition method is used, however, the resulting films are metallic and highly reflective. Alloys containing cobalt are most often employed in commercial magnetic recording devices, since they have the required magnetic properties of high coercivity and high resolution. However, they may also contain nickel and/or phosphorous. Alloys containing chromium, iron, tin, antimony, tungsten, and other metals have been reported. Cobalt/chromium alloys have recently received particular attention for vertical recording applications.

Thin-film media provide inherent advantages over iron oxide media. These include increased storage capacity, fewer errors, and greater durability (see the Table). Increased capacity results from the potential for greater bit and track densities that are supplied by the small particles. Bit size in iron oxide media must be larger than any magnetized particle. Typical limits are from 6 to 10 kbits/in. for oxide media. The smaller particles of thin-film media allow up to 20 kbits/in. or more. Thin-film media resolution also allows for more tracks/inch. This contributes to the higher storage capacity of drives that use this media.

James H. Smith is currently director of advanced media development at Evotek Corp, 1220 Page Ave, Fremont, CA 94538. He holds a BS in chemistry from Yale University and a PhD in organic chemistry from the University of California at Berkeley. In addition, Dr Smith was a postdoctoral fellow of the California Institute of Technology in chemical physics.

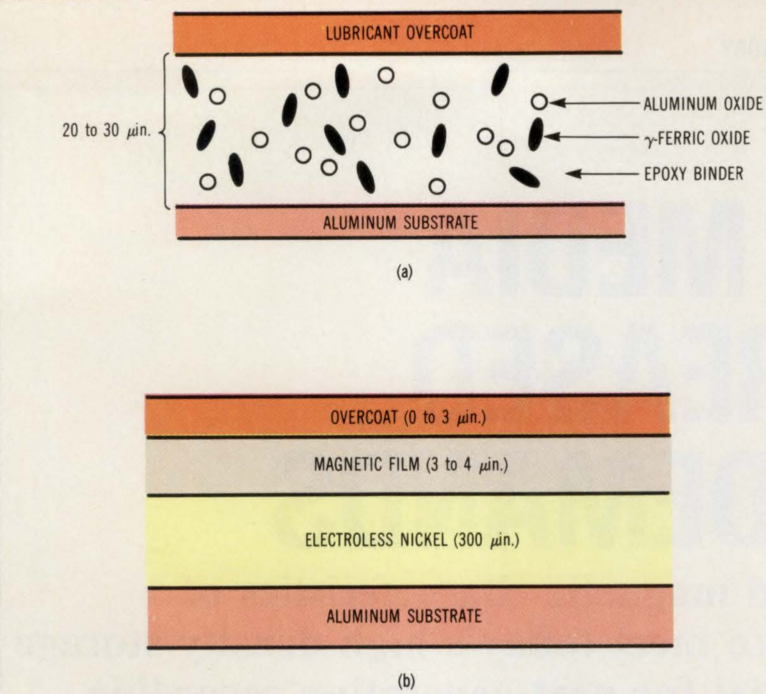


Fig 1 Depicted are cross sections of typical magnetic coatings of oxide (a) and thin-film (b) disk media. Magnetic material used to form thin-film media typically consists of cobalt/phosphorous or cobalt/nickel/phosphorous.

Fewer read/write errors are another mark of thin-film media. Flat, uniformly smooth disks provide better signal quality. A smoother medium allows lower head-flying height, which means increased amplitude and resolution. The thin medium needs a lower magnetic field to saturate it and a smaller head fringing field pattern. Fewer intrinsic read/write errors can reduce the need for advanced error correction techniques in drives using thin-film media.

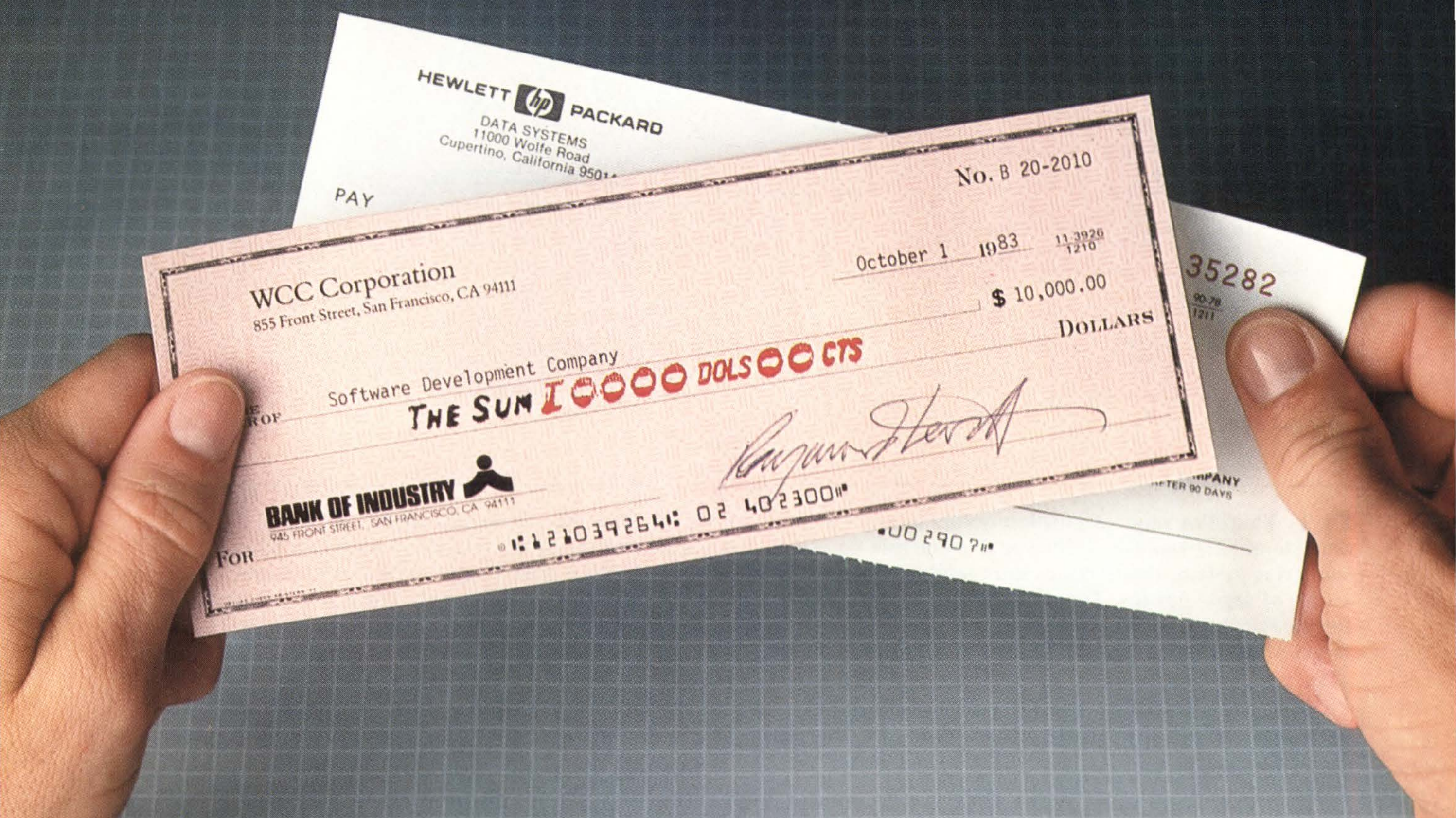
Durability of the media also supplies a number of advantages to users. The disks are better protected in transit (a plus for portable computers with integral disk drives) and in business settings. Particulate spilling does not occur as with oxide media because the magnetic coating is more strongly bonded to the substrate. Fewer particles generated inside thin-film media drives lessen the chance of damage from head crashes. Corrosion problems have largely been overcome by using aluminum substrates and overcoatings.

The combination of higher data capacities with fewer errors and increased physical durability enables high performance drives to be put in smaller packages. For those manufacturers who incorporate thin film into their drives, especially

Comparison of Oxide and Thin-film Recording Media

	Oxide media	Thin-film media	Advantages of thin-film media
Magnetic properties			
Coercivity (oersteds)	350 to 400	500 to 700*	Higher amplitude and resolution and reduced bit shift is possible
Remanence (gauss)	3500 to 4000	7000 to 8000	
Squareness (M_r/M_s)	0.45 to 0.55	0.80 to 0.95	
Thickness (μin.)	8 to 10	3 to 4	
Physical properties			
Surface smoothness (μin.)	1.0 to 1.5	0.5 or less	Lower flying height possible
Surface hardness		~1000 x harder	Less susceptible to head crashes
Overcoat	fluid	dry	Reduces attraction of particulate contaminants
Possible head-flying height (μin.)	~18	~10	Significant amplitude increase to the disk surface
Surface adhesion	poor to good	excellent	
Recording properties			
Bit density (bits/in.)	~8000	>15,000	Increased bit density and storage capacity
Resolution (percent)	~65	>80	Improved signal to noise
Amplitude**	low	high	Decreased bit shift and fewer errors
Bit shift	high	low	

*The upper limit of the coercivity is about 1700 Oe with thin-film media, but this is not useful in longitudinal recording because the heads cannot erase the disk.
**For a given head and head-flying height



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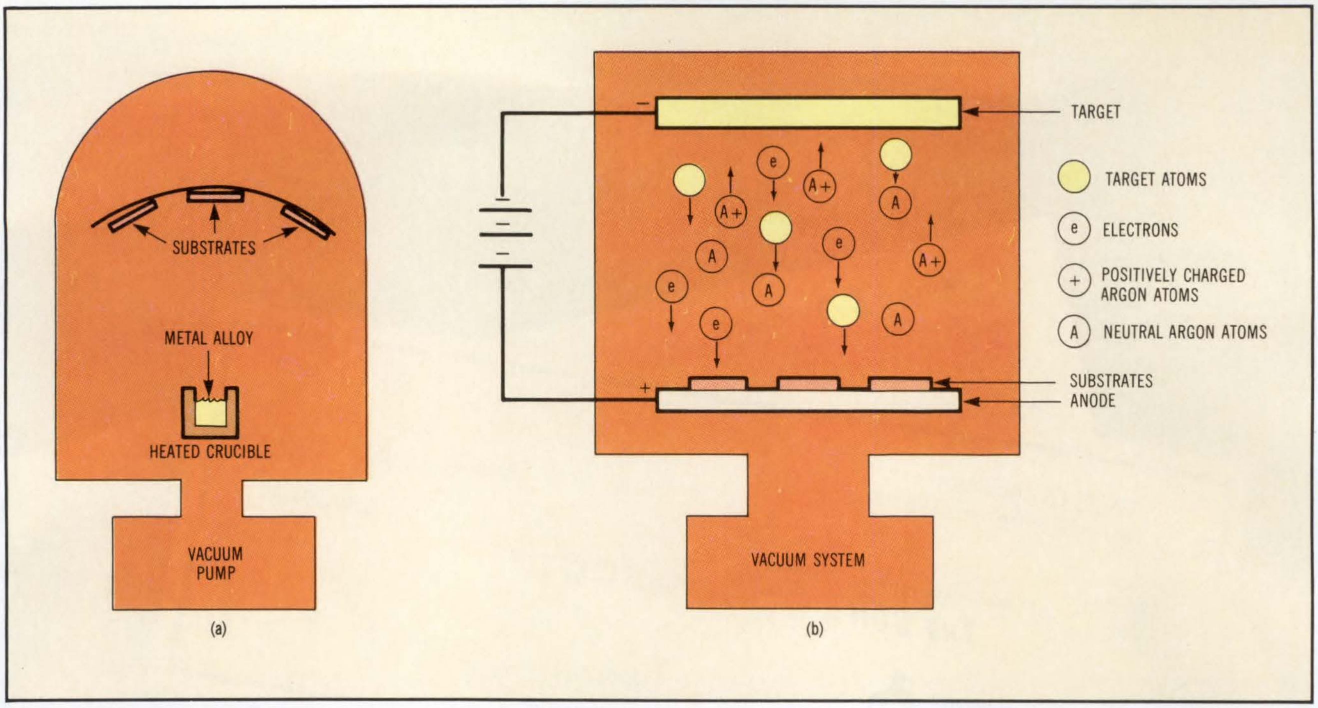

Fig 2 Thin-film vapor deposition occurs in an evacuated bell jar (a). The alloy to be deposited is heated in a crucible until it vaporizes. The vapor condenses on the cool substrate and forms the thin-film layer. In a basic sputtering system, the electrons are rapidly accelerated by the electric field (~2000 V) and collide with neutral atoms of argon gas (b). The argon atoms are then ionized and accelerated toward the target. When they hit the target, they knock off target atoms, which drift toward the substrate. Since the substrate is relatively cool, the target atoms condense onto the substrate, forming the thin film.

those manufacturing their own plated media, the pathway from longitudinal to vertical recording becomes easier.

At present, it may seem that oxide media are easier to produce. However, this perception is influenced by the large technological and capital investment in oxide media over the years. Although a thin-film medium requires somewhat more sophisticated production capability, its production is becoming commercially feasible.

Thin-film deposition methods

Four basic methods are currently used for depositing magnetic thin films on a disk substrate. These include vacuum deposition, sputtering, electroless (chemical) plating, and electroplating. Each method exhibits unique characteristics. Vacuum deposition has been used to prepare thin-film media for both longitudinal and vertical recording. The material to be deposited is first heated in a crucible (by direct electrical current, radio frequency, or electron beam) above the melting point of the metals. Metal vapor deposition occurs on the cooled surface of the disk substrate [Fig 2 (a)].

While deposition rates are usually high, the vacuum deposition method has a serious drawback when it requires alloy deposition. Since the two or more metals in the alloy have different vapor pressures, they evaporate at different rates. This causes the stoichiometric ratio of the diverse materials in the deposited alloy to change as the materials in the crucible evaporate. The continuously changing composition of deposited material makes it extremely difficult to maintain accurate control of the deposited alloy's composition. Since small composition changes usually have a large effect on the film's magnetic properties, producing large quantities of disks becomes difficult.

In the laboratory, sputtering produces excellent longitudinal and vertical thin films. The process involves a glow discharge in a high vacuum chamber. Target materials to be sputtered act as the cathode, and the substrate to be coated acts as the anode. When argon is introduced into the evacuated chamber at low pressure, and a glow discharge current is applied across the cathode and anode, the electrons in the discharge region accelerate rapidly. These high energy electrons collide with the argon atoms, ionizing them and producing a positively charged argon atom and a second electron. This positively charged atom is accelerated toward the target (ie, the cathode). The resulting impact knocks neutral atoms from the target material. These atoms drift toward the disk substrate and build up the magnetic film [Fig 2 (b)].

Sputtering has advantages over other thin-film deposition methods. The most important advantage is that the deposited material's composition is identical to that of the target material. This means that alloy deposition can be done repeatedly with excellent composition control. In addition, the process is easily automated, resulting in high process

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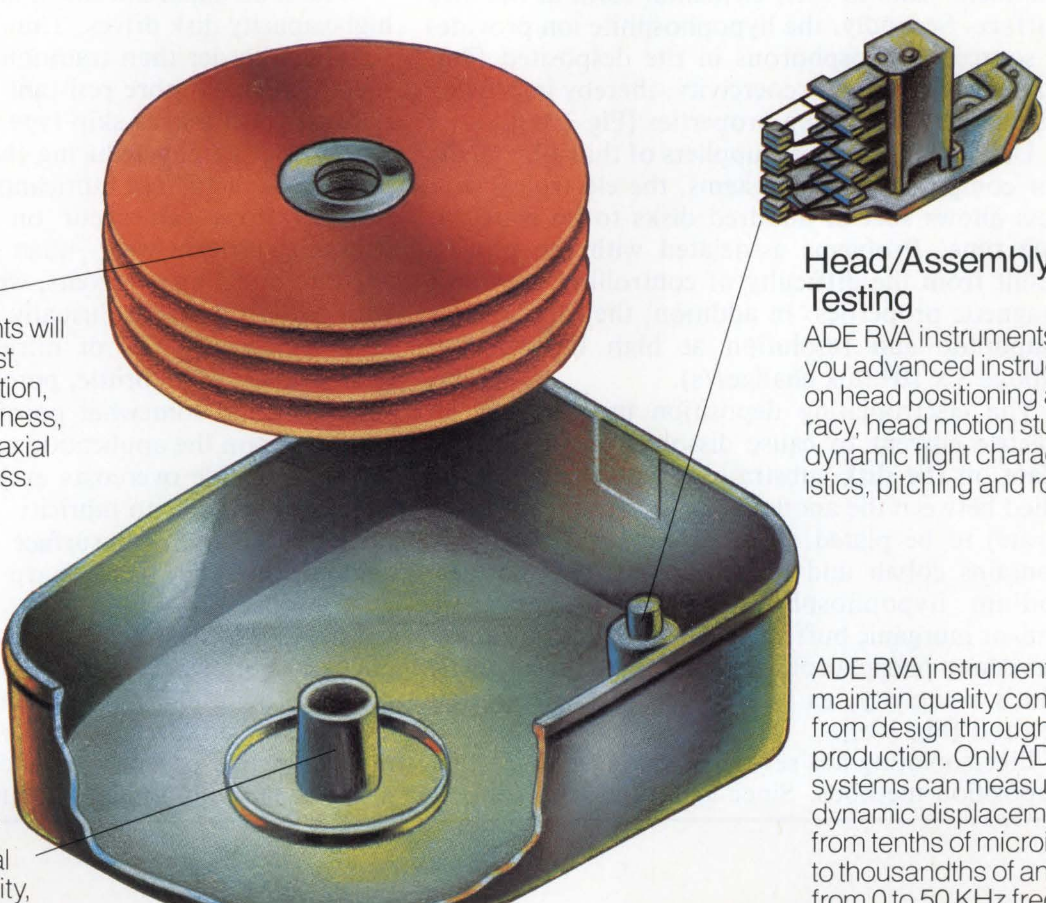

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yields and reduced labor costs compared to plating techniques. Moreover, the process results in minimal toxic chemical waste, significantly reducing disposal problems.

Sputtering is not without problems, however. The equipment necessary to produce disks on a commercial scale is just becoming available. In addition, the high sputtering rates needed to make the process economically feasible are difficult to achieve, and anticipated capital costs are high.

The electroless plating process produces deposits similar to those obtained through electroplating. However, it is a chemical process in which the metals to be deposited are present as sulfate or chloride salts in aqueous solution. A reducing agent such as sodium hypophosphite is also necessary. Sodium hypophosphite serves first to reduce the metal salts to their elemental form at the disk surface. Secondly, the hypophosphite ion provides a source of phosphorous in the desposited film. This raises the film's coercivity, thereby improving its magnetic recording properties [Fig 3 (a)].

Used by commercial suppliers of thin-film media for computer storage systems, the electroless process allows several hundred disks to be plated at one time. Problems associated with the process result from the difficulty of controlling the film's magnetic properties. In addition, the film has low amplitude and resolution at high bit densities (above 8×10^6 flux changes/s).

The electroplating deposition process uses an electric current to cause dissolved metal salts to plate on the disk substrate. Direct current is applied between the anodes and the cathode (the substrate) to be plated. The plating bath commonly contains cobalt and nickel sulfates or chlorides, sodium hypophosphite, and various organic and/or inorganic buffers. The hypophosphite anion serves as a phosphorous source to raise the magnetic film's coercivity, as in the electroless deposition method [Fig 3(b)].

Electroplating has several advantages over other deposition methods. Since agitation, pH, temperature, hypophosphite concentration, and metal salt concentrations have a predictable effect on the magnetic properties of the thin-film deposit, the method allows excellent control of read/write characteristics. From the manufacturer's point of view, the capital investment in electroplating equipment is low for manual operation and the process can be readily automated or robotized.

Mechanical properties of thin-film media

Important mechanical properties of thin-film media include wear characteristics, types of overcoating materials, and surface finish characteristics. Evaluation criteria for these mechanical properties are now being formulated with a view toward establishing industry-wide test standards and specifications.

Wear is an important factor in today's high speed/high capacity disk drives. Thin-film media are substantially harder than traditional oxide media and therefore much more resistant to scratching. This hardness also makes skip-type head crashes much less likely, thereby reducing the risk of lost data. Even without surface lubricants, a greater number of start/stops can occur on thin-film media—wihout significant wear—than on oxide media.

Nonlubricating overcoats, which cannot be used with oxide media, are usually based upon silicon oxides (SiO or SiO_2) or nitrides (Si_3Ni_4). Oxide overcoats are often brittle, porous to various corrosive ions, and somewhat porous to moisture, depending upon the application technique. Although the hard nitride overcoats exclude moisture quite well, they provide no lubricity. In addition, a contaminant on the disk surface can cause SiO_2 to agglomerate and form sharp unwanted surface protrusions.

Lubricating overcoats, such as sputtered amorphous carbon, which also cannot be used with oxide media, provide significantly better wear characteristics than nonovercoated or SiO_2 overcoated media. In this process, a bonding layer of nickel oxide or chromium metal about 50Å thick is first

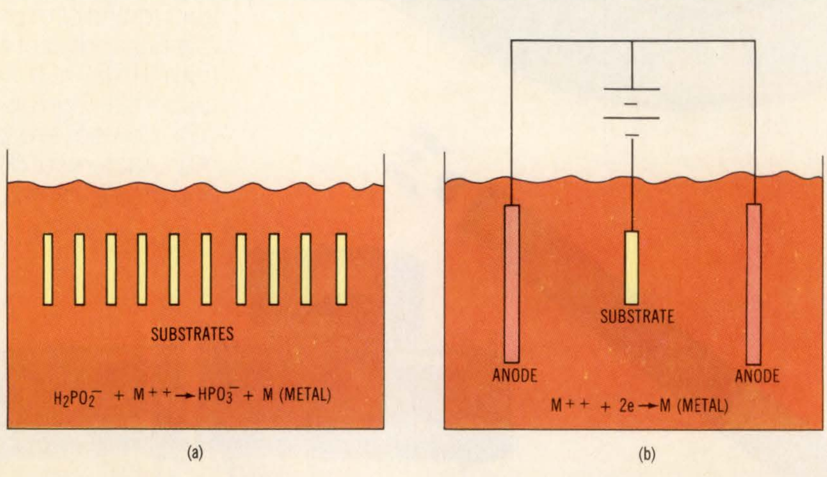

Fig 3 Electroless plating is a chemical reaction of hypophosphite and metal ions to form a metallic alloy of the metals and phosphorous (a). Electroplating is an electrochemical reduction of metal ions to form the metallic thin film (b). If hypophosphite ions are also present, they codeposit to form metal/phosphorous alloys.

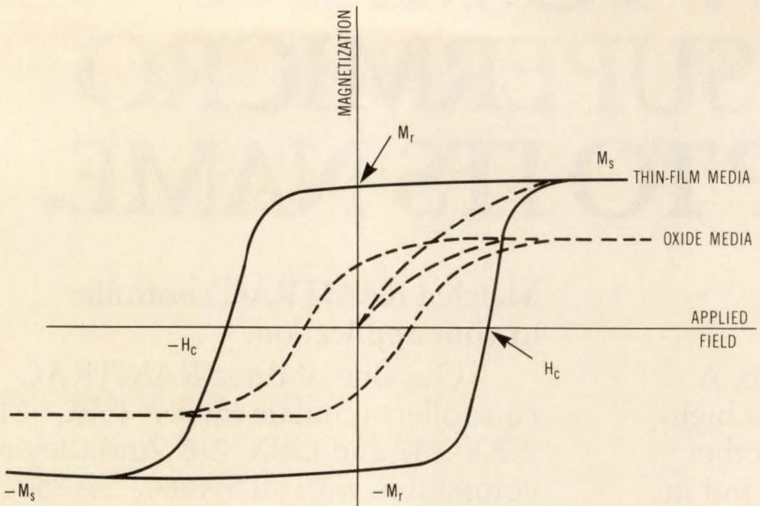

Fig 4 With magnetic hysteresis or M-H loops, when a magnetic field is applied to a magnetic field and slowly increased, the film is magnetized until it reaches a saturation level, M_s. When the applied field is reduced, then reversed, the material remains magnetized. At zero field (H = 0), the material remains magnetized at a level of remanence (M_r) until the applied field is reversed. The applied field required to demagnetize the material (H_c or $-H_c$) is the coercivity.

sputtered on the magnetic film. Then 2 to 3 μin. of carbon are sputtered from a graphite target without exposing the disk to air. The amorphous carbon deposit has characteristics of both graphite and diamond. If the head and disk are very clean, more than 230,000 start-stop cycles can be achieved with a 5¼-in. Winchester disk and a 3350-type manganese/zinc/ferrite head flying at 8 to 10 μin.

Surface finishing of the substrate is extremely important with thin-film media. Electroless nickel substrates can be polished to a surface finish of less than 0.5 μin., peak to valley. The magnetic thin-film media and their overcoat mirror the substrate's surface finish coat because they are so thin. Since the surface is so smooth, head-flying heights of 10 μin. or less can be achieved, significantly improving the disks' signal amplitude and resolution. In contrast, typical peak-to-valley tolerances for oxide media are 1.0 to 1.5 μin. and head-flying heights are 18 μin. or higher.

The deposition method used for thin-film media affects the surface finish. The electroless method performs least efficiently since the resulting film is most porous. Altering deposition conditions cannot modify the surface finish. Electroplating thin-film media is significantly better because the process allows finer control of plating conditions. Organic additives, usually polybasic acids, can be added to the plating bath to further improve the finish. Sputtering methods produce very smooth surface finishes, but available equipment limits production quantities.

There are as yet no standardized evaluation criteria for thin-film media disks. Of special concern to the ANSI *ad hoc* committee on thin-film disk media standardization—presently at work defining standards for thin-film magnetic media—are questions relating to the adhesion of thin film to substrate. The adhesive properties of oxide media, for instance, range from poor to relatively good when a common test is applied. The Scotch tape test consists of pressing tape to the medium and pulling it off again to see if the medium comes off with the tape. Thin-film media disks pass this test easily, whereas oxide media disks do not always perform well. Another criterion, the bend test, involves bending a disk against a round mandrel and examining the results. Thin-film media will fracture but will not come off, however, oxide media will flake off easily. Such flaking can contaminate the disk drive, causing data loss and damaging drive components.

Recording characteristics

Magnetic properties of thin-film media result in a significantly higher, sharper output signal. The greater resolution that results enhances the system's ability to distinguish data on the disk. Classically, magnetic properties are measured by plotting the amount of magnetization that remains in the media after an applied field is removed, against the external magnetizing force (applied in this case by the drive head). The resulting hysteresis cycle is an image of the interplay between coercivity and remanence (Fig 4).

Read/write characteristics relate directly to magnetic properties. Thin-film media produce higher amplitude, resolution, and phase margin than oxide media, thus permitting higher bit and track densities. With oxide media, bit size is limited to the size of the ferric oxide particle. Bit size in oxide media, therefore, exceeds the minimum bit size found in thin-film media.

Oxide media particles have partially random pole orientations that lower the signal-to-noise ratio and broaden the signal peak. This reduces bit density. The problem is partially compensated for by applying an orienting magnetic field that causes the oxide particles to line up magnetically. This manufacturing step is not required in the thin-film media process. Furthermore, particles within the oxide media appear in a range of sizes. This affects bit density and uniformity of output amplitude. Extremely large particles cause a bit "dropout" since the energy available during write mode is not sufficient to flip polarity.

The uniform small magnetic domains present in thin-film media do not pose these problems. Bit density is limited only by the size of the microcrystal in the metal film. Minimum size for a single magnetic domain in thin-film media is an order of magnitude smaller than that for oxide particulate media. Microcrystal size can be closely controlled using the electroplating deposition method.

Error characteristics also provide a means of comparing oxide with thin-film media. Errors in oxide media arise from variations in media thickness, particle size variations, and nonuniform distribution of particles in the epoxy binder. Both oxide and thin-film media occasionally exhibit pin holes in the surface that cause missing bits. These error-causing traits can be controlled within certain constraints. The thin-film media are not subject to problems associated with particle size variation or nonuniform particle distribution. Pin holes in thin-film media can be controlled by paying careful attention to production details such as cleaning, and using pure chemicals and deionized water. However, modulation errors may occur in thin-film media because of slight thickness variations. Local areas of very high coercivity may cause extra pulses to occur if previously written data cannot be erased completely by the read/write head. These problems can be controlled by providing adequate agitation to the plating bath during manufacture.

The ability to closely control both the magnetic and mechanical properties of thin-film media during manufacture allows production of reliable, highly durable storage devices. These factors combine with thin-film media's inherently high bit density to not only feed today's increased storage demands, but to pave the way for the vertical recording devices of the next generation.

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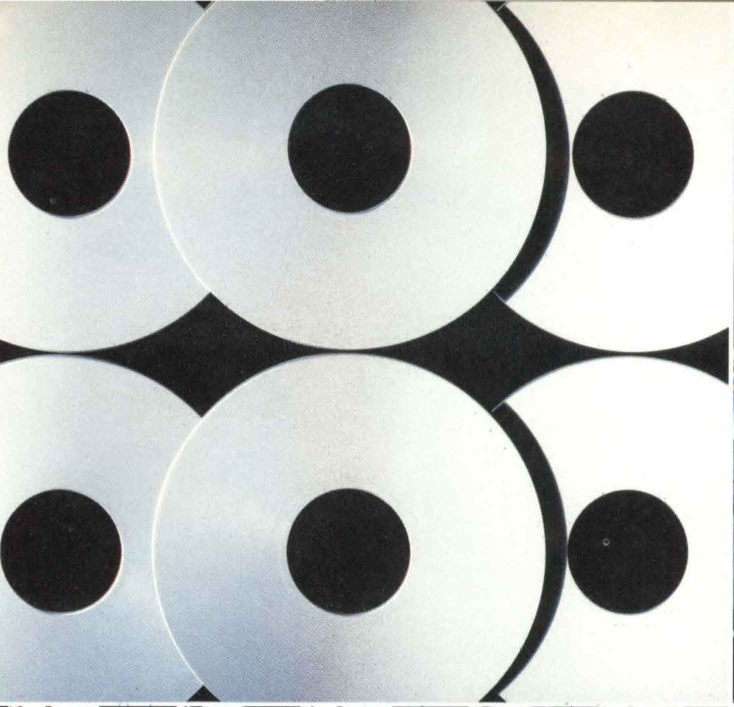
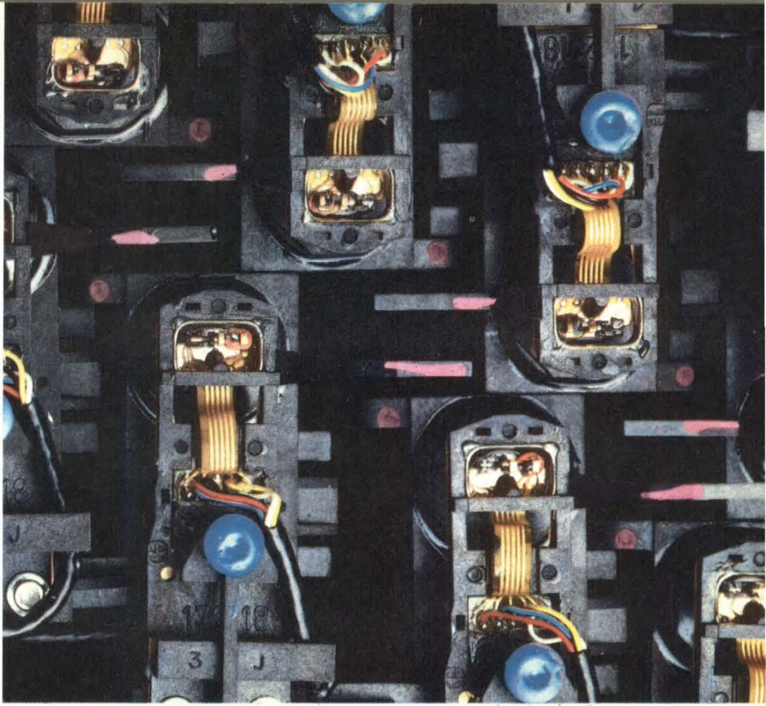
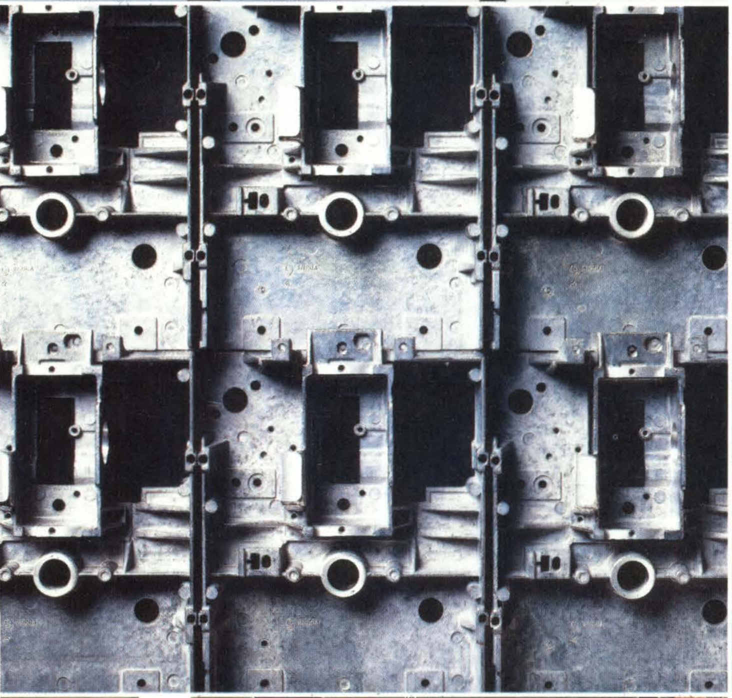
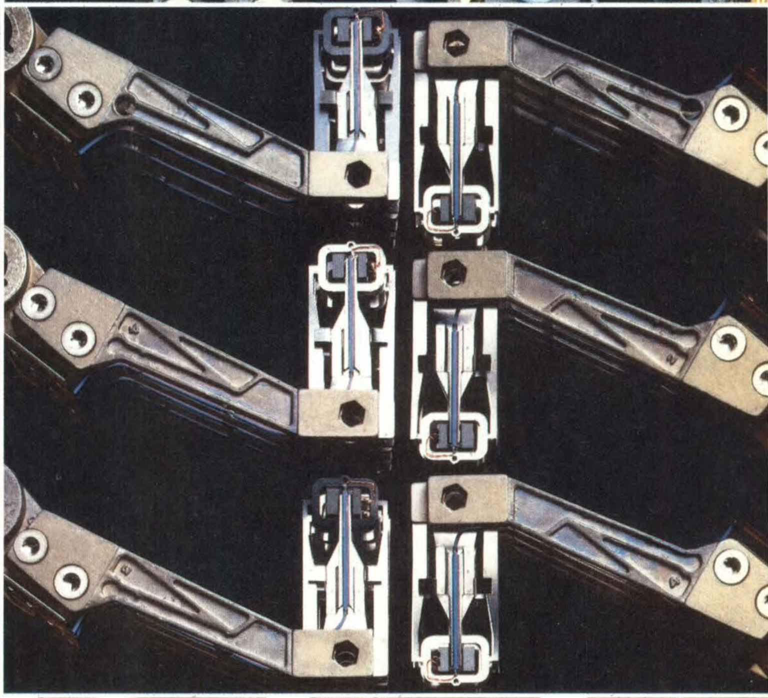
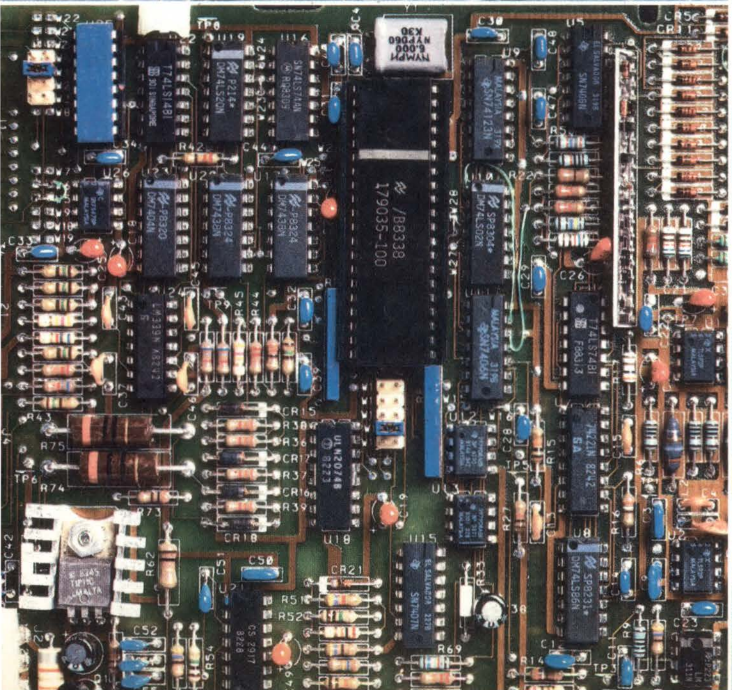
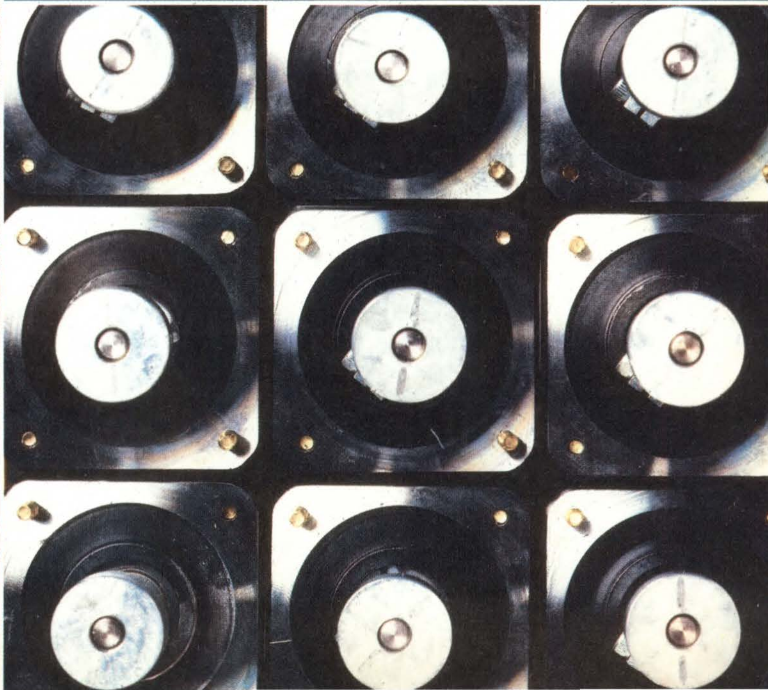

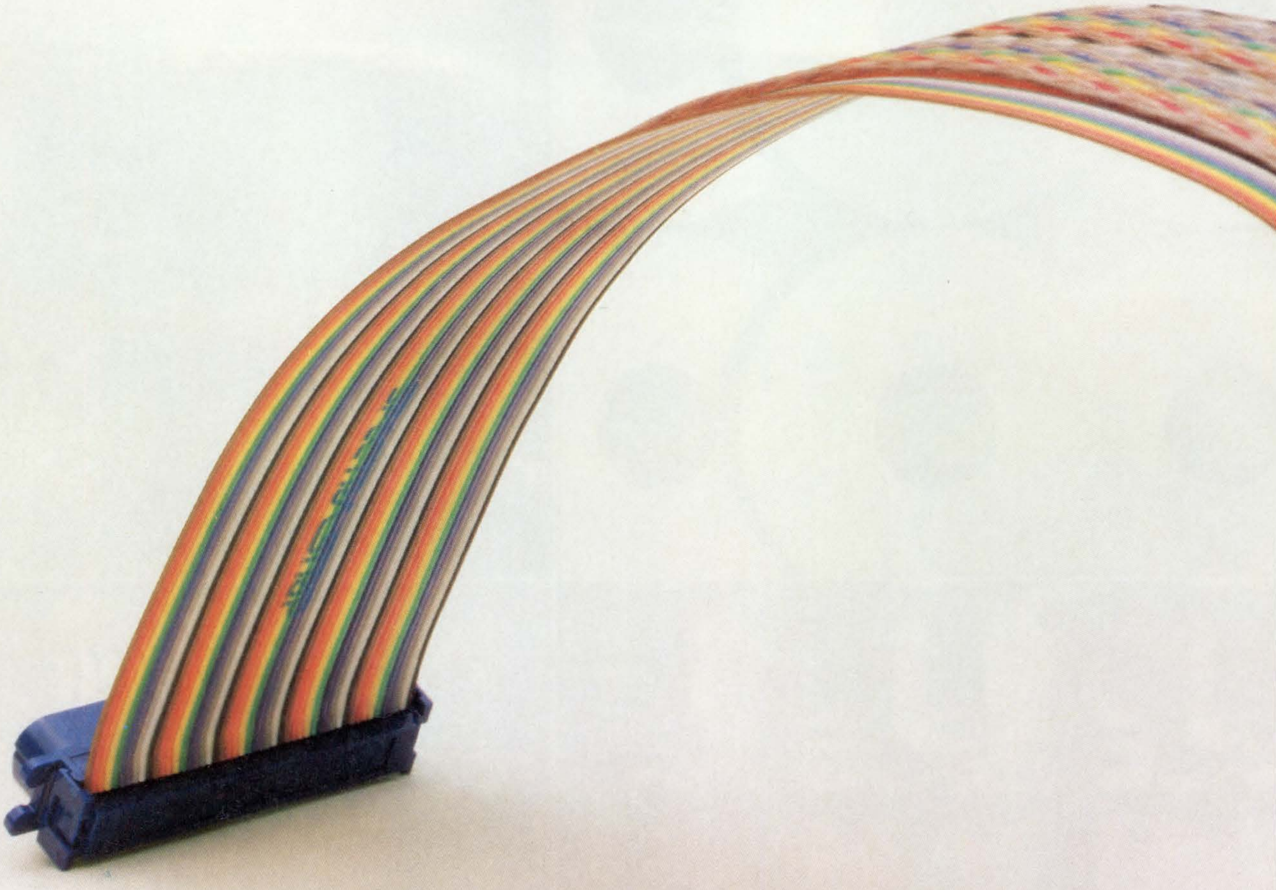

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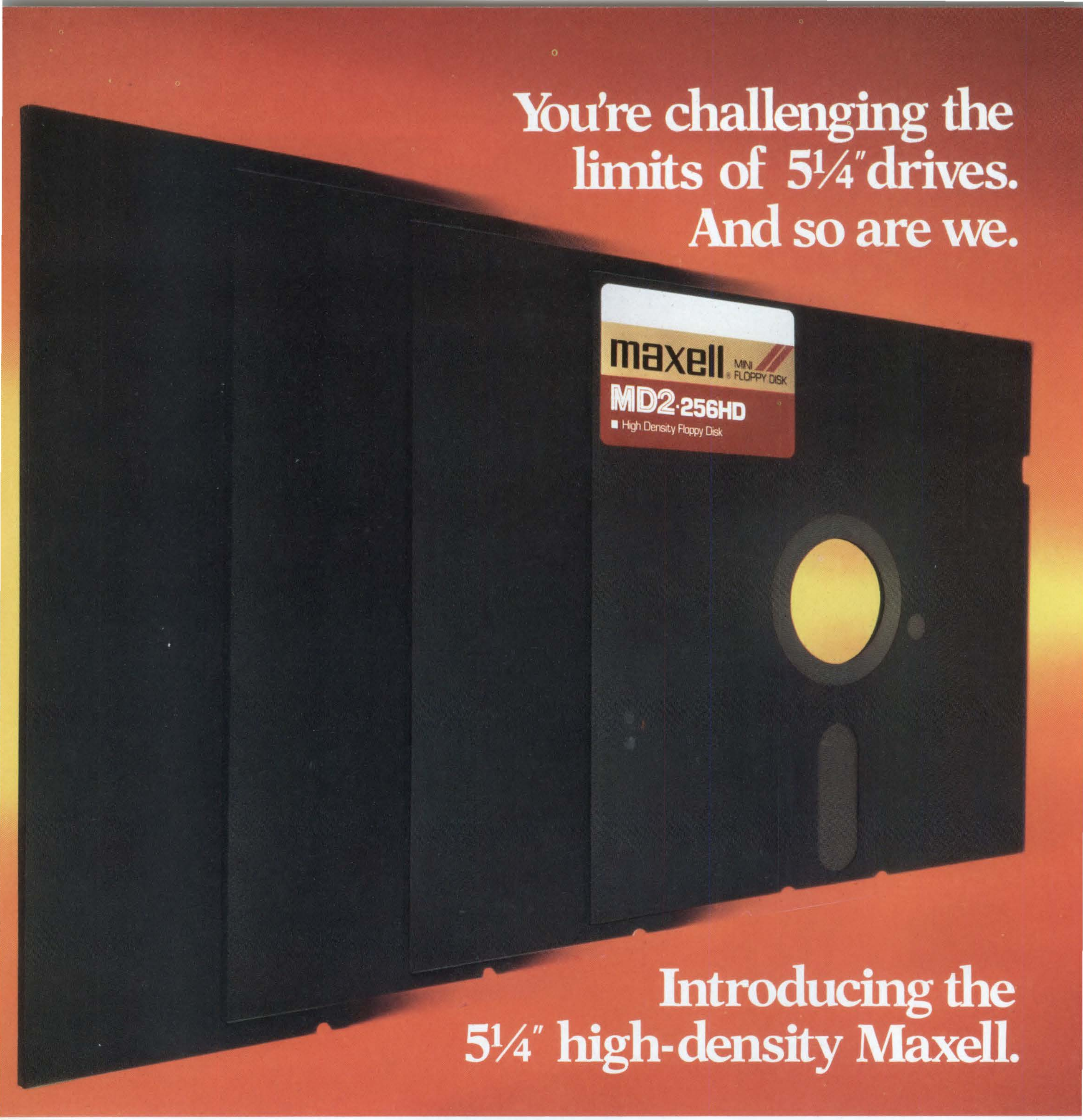
CIRCLE 149



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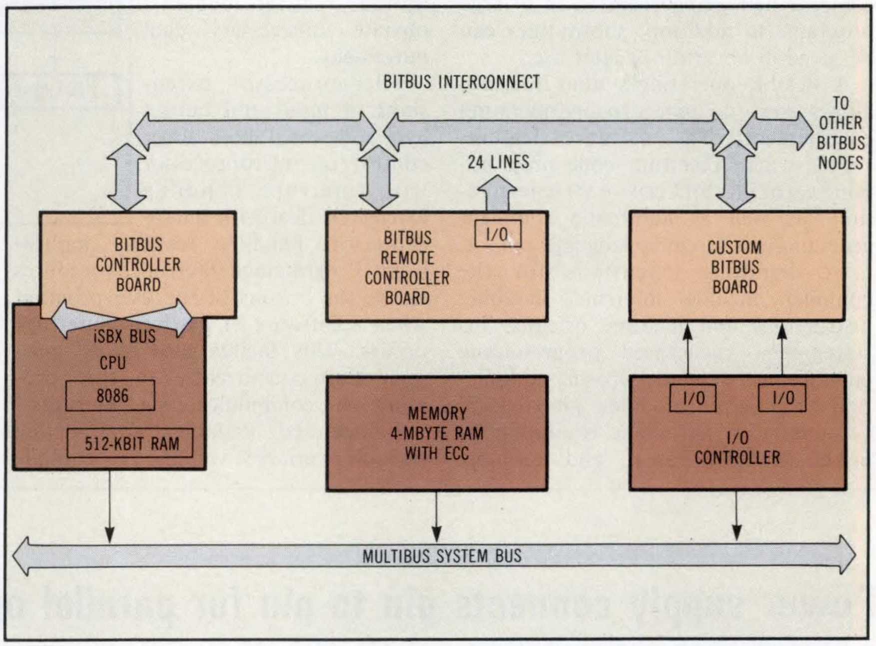
CIRCLE 150

Standardized microcontroller bus paves distributed pathways

A high speed, realtime communication link connects diverse control components from different vendors to their respective systems. This not only allows designers to coordinate the operation of individual elements within a larger work cell, but also reduces the cost and effort for such integrations. Based on existing industry standards and an open-system architecture, Bitbus offers hardware and software interfaces to Multibus, Eurocard, portable control, and custom board-based systems.

In many applications, the Bitbus can replace numerous custom point-to-point interfaces to local functions with one standard, expandable interconnect. In addition, the microcontroller bus assumes minimal CPU overhead and no realtime contention for CPU power. As a result, exchange of control is simpler and faster than in data communication schemes, which often entail burdensome CPU time and custom software.



Following the SDLC protocol, the RS-485-compatible physical connection uses twisted-pair wiring. The serial bus is optimized for high speed transfer of short control messages in a hierarchical system. Bitbus messages assume a standard format that includes node and task addresses as well as fields for command, response, and status. A preconfigured software interface between the Bitbus data path, devices, and realtime operating systems resides onboard in the controller's ROM.

Three data transmission rates provide a mix of speeds and distances. The fastest connection—zipping up to 30 m over four-wire cable at 2.4 Mbaud—supports up to 30 Bitbus nodes. The other two rates transmit over two-wire links, and connect up to 28 Bitbus nodes between any two repeaters. The 375-kbaud line transmits 300 m between repeaters with up to two repeaters between any two nodes, and the 62.5-kbaud line stretches to 1200 m between repeaters with up to 10 repeaters between two nodes. Cost per node is roughly $20.

Two distributed control module (iDCM) boards lay the groundwork for Bitbus microcontroller interconnections. The iSBX 344 Bitbus controller board attaches to an iSBC single-board computer to provide iSBX I/O interface and additional memory sockets. This expansion board is based on the 12-MHz 8044 chip, which is a monolithic dual processor comprising an 8-bit 8051 and an SDLC controller that frees the 8051 from communication tasks. Onchip 8044 firmware controls the Bitbus interface, iRMX 51 realtime multitasking executive, user tasks, remote access and control, and power-up diagnostics.

Also based on the 8044 chip, the iRCB 44/10 intelligent remote controller board conforms to a standard single-width, single-height Eurocard package with DIN connectors. It offers 24 digital I/O lines, as well as an iSBX I/O connector, extra memory sockets, and 8044 controller firmware.

On both iSBX 344 and iRCB 44/10 boards, the iRMX 51 operating system nucleus resides in 8044 ROM. This realtime, multitasking software handles task scheduling, interrupt handling, and message passing. The executive also performs all communication tasks: it provides remote access to external RAM and I/O as well as user programs, and allows the controller to set, clear, or toggle I/O ports, determine device and message status, and more.

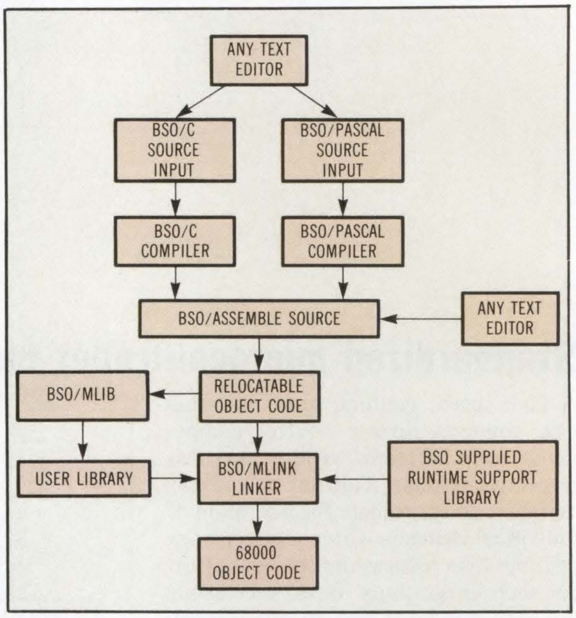
Apart from its role as runtime executive, the iRMX 51 acts as a software tool for developing and implementing microcontroller applications. The iRMX 510, a software utilities package for iRMX 51 applications, contains software interface drivers for iRMX-86, -88, -286R, and iPDS Isis, as well as controller firmware files and executive libraries.

In single-unit quantities, both iSBX 344 and iRCB 44/10 cost $450; licenses for iRMX 51 operating system nucleus are $3000, and iRMX 510 utilities are $1800. The company expects to begin shipping this month. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.

—D.H.

Circle 260

Optimizing C compiler targets 68000 microprocessor on VAX



The BSO/C is an enhanced compiler conforming to the Kernighan and Ritchie standard and proposed ANSI standards for C. In addition, it offers extensions that permit easier C language programming for 68000 application development. General features include extensive optimization, assembly language output to permit manual optimization, and a runtime math function library.

The compiler divides a large program into several more manageable modules. The program modules can be checked and debugged individually to avoid most complex debugging required in a large program. In addition, subroutines can be saved in libraries for later use.

A flexible operating system interface allows users to connect to any operating environment. The software features recursive and reentrant code programming capability and ROM/RAM segmentation, as well as automatic comment generation on assembly language output.

I/O handling extensions for the compiler include interrupt handling instructions and realtime oriented I/O statements. Structured programming enhancements include separate compilation of program modules, global/local variables with automatic resolution by linker, and C, Pascal, and assembly language module linking. With these enhancements, programs can be written in three different languages.

Optimized output results by simplifying addressing mode, optimizing branches, and storing contents of registers. Simplifying addressing mode leads to smaller code, while branch optimization leads to more compact code (when both long and short branches are available). Stored register contents obviate unnecessary data movement.

Microprocessor extensions of input and output byte and word allow direct control of microprocessor I/O. Interrupt handling extensions deal with microprocessors handling realtime applications. Programmed interrupt procedures define the actions of the user program when a software or hardware interrupt occurs. This facility also allows programming concurrently so that programs can communicate via interrupts.

Enumerated variable types define possible variable values. At compile time, the compiler checks the values to ensure that they are only assigned to a particular variable. Predefined functions offer truncation or rounding for floating point to integer conversion. Availability is slated for May. **Boston Systems Office**, 469 Moody St, Waltham, MA 02154. —*M.B.*

Circle 261

Power supply connects pin to pin for parallel operation

A single output switcher, the 1000-W HL1000 fits the standard 5- x 8- x 11-in. format. Pin-out compatibility provides several control features including supply paralleling, advance thermal warning, power fail detect, remote sense output status, and remote inhibit.

Supplies are constructed from ac input, output, and control modules. The input module includes an rfi filter, ac line rectifier and filter, 24-V housekeeping supply, power fail detect, and drive and power switching circuitry. The output module contains the power output transformer, rectifier, and filter. The control module is a 4.25- x 4.5-in. PC card containing control and supervisory circuitry together with an external control interface.

When the supply operates in parallel, the difference between output currents of parallel units is less than 10 percent of the full load value. In a redundant configuration, parallel outputs deviate less than 2 percent as a result of inhibit, shutdown, or failure of a parallel supply.

Some control features pertain to the parallel supply configuration. The parallel signal controls current sharing in the main modules. Current sharing is insensitive to output voltages, resulting in a value to within 10 percent of the total current. A slave triggering signal ensures simultaneous triggering of all main crowbar protection circuits when one is activated.

The current mode features a built-in voltage proportional to the current. Placing the units in parallel results in an average voltage. Current mode switching reduces the need to compensate for changes in load, lessening the supply's dependence on the input voltage.

Both the current mode and the proportional drive reduce parts count and power dissipation of control and drive circuitry. This increases efficiency and reliability. Output sharing is also available using a single control wire between units. The total power varies between 600 and 1000 W, depending on the selection of output and control modules.

Other power supply features include overvoltage and overcurrent protection, remote supply inhibit, power fail warning, an output status line, and over temperature with advance warning signal.

Supply is priced at $775 in quantity with availability scheduled for July. **Boschert Inc**, 384 Santa Trinita Ave, Sunnyvale, CA 94086.

—*M.B.*

Circle 262

Tape drives enhance high performance of GCR with cache technology

The GCR CacheTape line is a family of compact, high performance, group code recording tape drives. The initial member of the family is the model M990, which offers the high performance of GCR coupled with cache technology; the M991 is a higher end version offering these same benefits.

Cache technology is the key element in the drive's design. The high speed solid-state cache memory replaces more costly and less reliable vacuum column and compliance-arm GCR mechanics. Though two-track error correction is usually possible in GCR drives, cache memory allows four-track correction. This results from a bidirectional (forward and reverse) correction scheme. The cache also provides start/stop software compatibility.

Model M990 features a 128-Kbyte cache size and a 450-kbyte/s maximum transfer rate. Maximum block size is 32 Kbytes. Model M991 has a 256-Kbyte cache and a 790-kbyte/s maximum transfer rate. Maximum block size is 64 Kbytes. This model also features downstream erase to eliminate tape repositioning on write error retries.

Both models use the standard Cipher half-inch tape interface for hardware integration. The cache approach produces an error-free interface. The outboard error (defect) management relieves the host system of performance-limiting tasks such as handling media defects.

The 6250-bit/in. drives provide up to 180 Mbytes of data storage on a single tape reel—nearly four times the storage capacity of conventional 46-Mbyte phase encoded drives. This lets the M990 support the backup of a 500-Mbyte Winchester disk drive with less than three reels of tape.

The low profile half-inch tape drive measures 14 in., an advantage when space is at a premium. In addition, user-friendly features include a patented front-loading and threading design with understandable, front-panel word displays and service maintenance messages.

The M990 will be priced between \$6000 and \$7000, while the M991 will cost between \$7000 and \$8000. Volume production begins in June for the M990. **Cipher Data Products, Inc,** 10225 Willow Creek Rd, PO Box 85170, San Diego, CA 92138.

—M.B.

Circle 263

Programmable logic array design software runs on IBM PC

A CAD software package to compile fuse maps for programmable logic devices enables designers to program such devices by creating truth tables, state diagrams, or Boolean equations. Data I/O's advanced Boolean expression language (ABEL) runs on IBM PC or Digital Equipment Corp VAX computers in conjunction with its programmable logic development system (PLDS). Compiled fuse maps are downloaded to the PLDS to physically program the device.

Software descriptions support different manufacturers' devices, including programmable logic array (PLAs) and integrated fuse logic (IFL). ABEL itself is written in C to ensure future portability and efficiency. Moreover, it consists of seven programs: Parse, Transform, Reduce, Fusemap, Document, Simulate, and To ABEL.

To program a device using ABEL, the user first creates a source file (using a text editor) to define the logic design, including pin definitions for the device. The source file can be created using a free form syntax that does not depend on line and column numbers. In addition, the user can invoke macros and preprocessor commands from the input file as well as specify functional test vectors. Set notation groups related pins and operates them as a unit.

The parser processes this file's ASCII output. Truth tables and state diagrams are converted to Boolean equations. The Transform program first converts all equations with sets or relational operators to equivalent equations using only Boolean operators. The Reduce program then minimizes the Boolean equations using the standard theorems, including DeMorgan's theorem. Further logic reduction is performed using the Presto algorithm.

The resulting near-minimum equations are converted to a fuse map for the respective device by the Fusemap program. This fuse map can be sent to the PLDS as a standard JEDEC load file for programming.

Before the fuse map is downloaded, the Simulate program can test it. Simulate applies test vectors to the fuse map to simulate its operation. Users can set breakpoints and do single-step tracing to aid in the debugging process. The Document program produces documentation including chip diagrams, fuse diagrams, equations, and test vectors.

ABEL supersedes an earlier assembler-level language called Palasm. To ensure users consistent programming routine libraries, the company provides a program called To ABEL that converts Palasm files to ABEL source files. Thus, previously created fuse maps can be documented and tested to the same standards as newly created ABEL designs.

For the IBM PC, ABEL is priced at \$895; the DEC VAX version is \$2495. **Data I/O,** 10525 Willows Rd NE, C-46 Redmond, WA 98052. *—T.W.*

Circle 264

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Small table top applications can use the MDX80000 foundation system with five Multibus slots, 10, 15, or 40Mb of 5-1/4" Winchester storage plus an 8" IBM compatible floppy.

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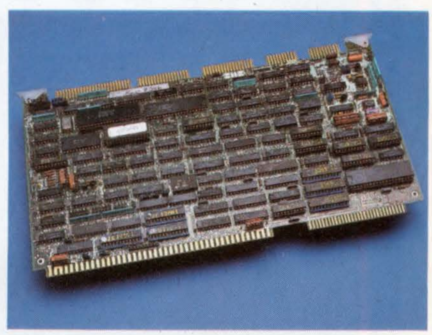

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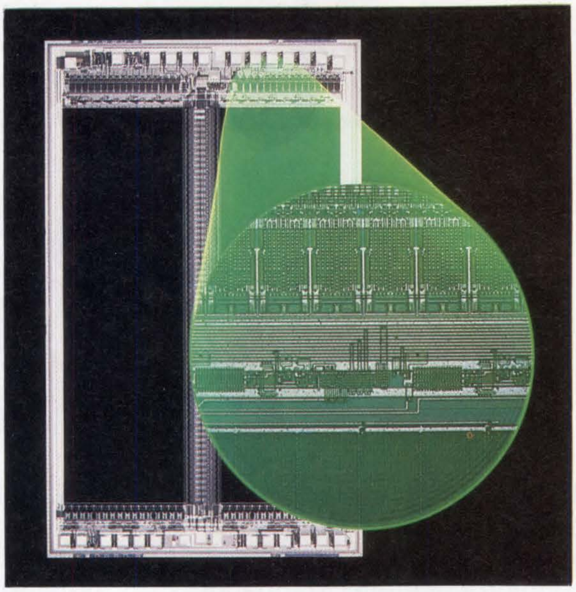


The next rung on the erasable PROM density ladder comes in the form of the 512-Kbit Am27512. This chip closely follows the company's previous announcement of a 256-Kbit EPROM (*Computer Design*, Sept 1983, p 220) distinguished by its 170-ns access time. The 512-Kbit version features many of the same characteristics, but unlike the 256-Kbit version (which used only row redundancy) the 512-Kbit model uses both row and column redundancy.

Organized as 65,536 words x 8 bits, the UV EPROM has a solid capacity to store such microprocessor operating systems as CP/M or MS-DOS on a single device. Putting the software directly onchip allows quick and reliable data access. In addition, the device can store microprocessor control programs for minicomputers.

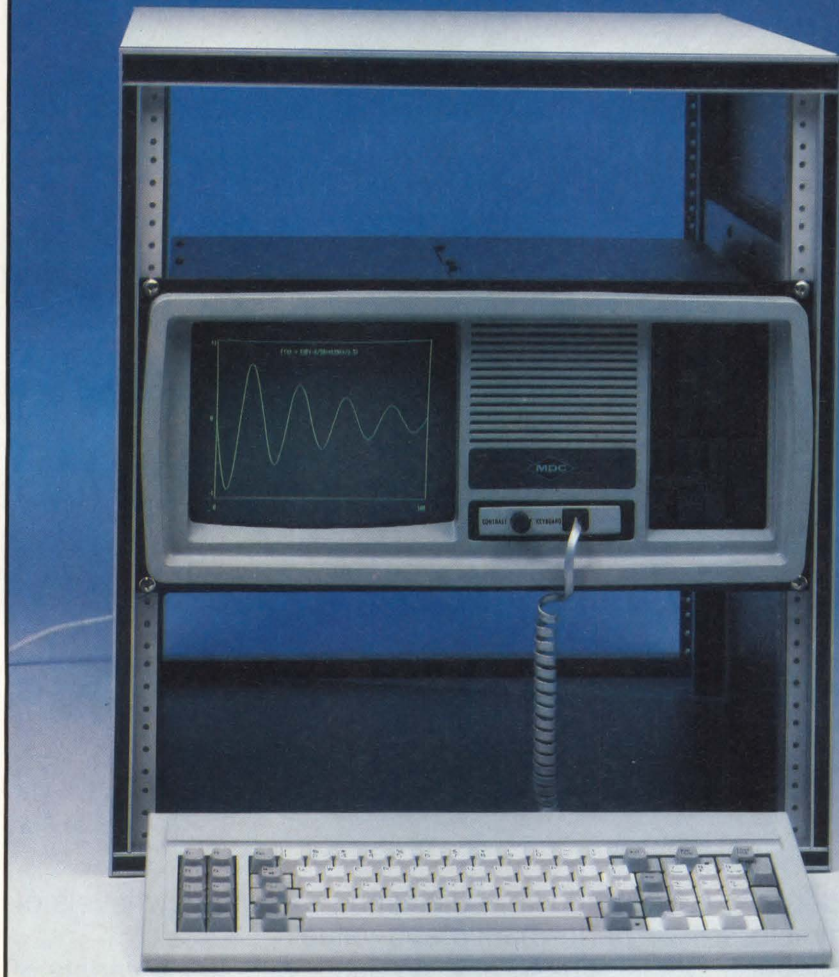
An auto-select mode automatically reads the EPROM's binary code containing device manufacturer and type. This enables programming equipment to mate the device with its programming algorithm. Using an interactive programming algorithm, the chip requires as little as 6 min for programming. This algorithm uses 1-ms pulses that give each address only the number needed to reliably program data. A 12.5-V programming voltage puts the Am27512 into programming mode. Bit locations can be programmed singly, in blocks, or at random.

Dissipating 132 mW standby and 525 mW active, the device reduces overall power requirements. It operates on a single 5-V supply and is packaged in a 28-pin JEDEC-approved pinout. The EPROM is pin compatible with the Am2764, Am27128, and the Am27256 EPROMs, as well as the Am92256 256-Kbit ROM.

Output and chip enable eliminate bus contention in multibus processor systems. The chip enable is the power control and is used for device selection. Output enable accomplishes output control and is used to gate data to the output pins, independent of device selection.

Available access times include 250 and 300 ns (commercial) and 450 ns (military). Price for the 250-ns version is $395.60 each in 100s with samples now available. **Advanced Micro Devices Inc**, 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 265 *—M.B.*

You won't find this PC in an office.



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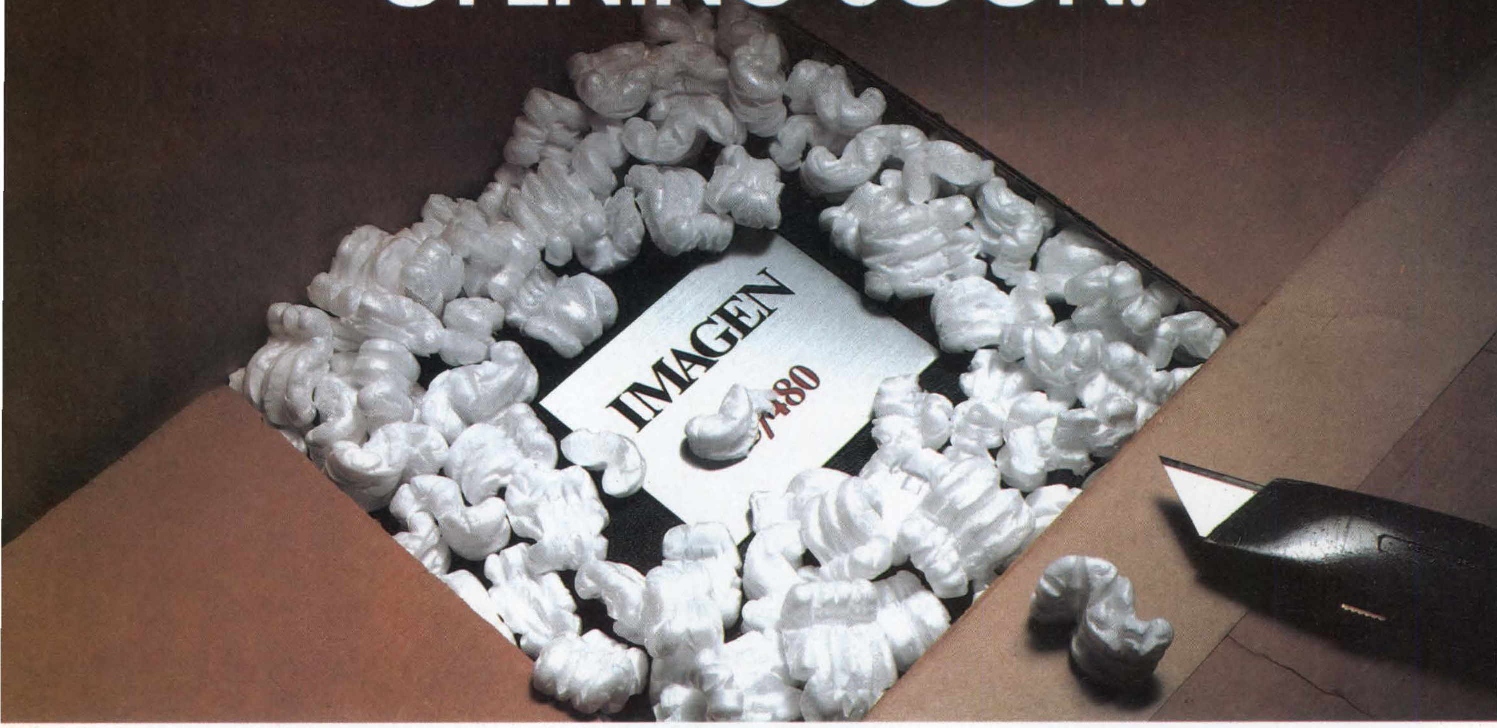

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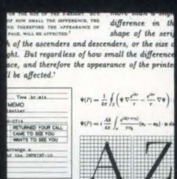

PRINTING

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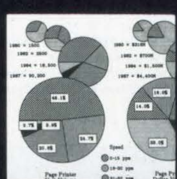

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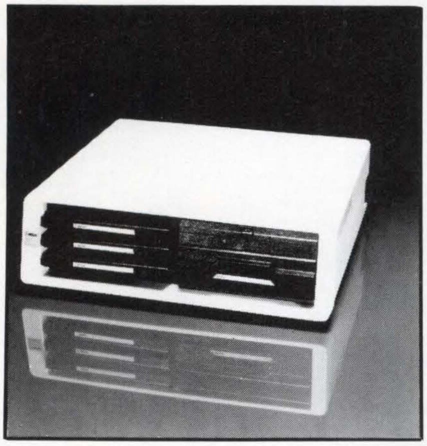
CIRCLE 154

Single-drive subsystem for PC/XT



The 10-Mbyte system has a built-in compartment for cartridge storage. Removable media enable users to format as many cartridges as needed. Embedded closed-loop servo ensures interchangeability from drive to drive. The drives employ the Bernoulli principle of fluid dynamics to achieve high density and access speeds equal to rigid files. A 10-μin. clearance creates a soft interface between head and media for longer media life. The 10-Mbyte version is priced at $2695 and is upgradable to a 20-Mbyte version. **Iomega Corp,** 4646 S 1500 West, Ogden, UT 84403.

Circle 266

Winchester for multi-user system

The ST8100 8-in. drive stores 102.10 Mbytes of unformatted data in a half-height package. Average access time is 30 ms using a proprietary voice coil linear actuator design. Transfer rate is 10 Mbits/s. The drive uses three 8-in. oxide-coated disks, a dc spindle motor, and manganese-zinc ferrite read/write heads. In quantity, prices are less than $1500. **Seagate,** 920 Disc Dr, Scotts Valley, CA 95066.

Circle 267

Hard disk controller for PC

The 32-Mbyte capacity hard disk/controller emulates the IBM PC-XT controller operating under MS-DOS 2.0. It ensures compatibility with all other operating systems that work with the XT including CP/M-86 and UCSD Pascal. It is also compatible with IBM work-alikes, including the Compaq portable computer. It will also accommodate all networking protocol and future products that operate under MS-DOS 2.0. The hard disk and controller card are faster and have improved error correction capabilities over IBM offerings. **Mountain Computer, Inc,** 300 El Pueblo Rd, Scotts Valley, CA 95066.

Circle 268

Winchester disk drive

The 4114, 264-Mbyte fixed media drive is designed to bring flexibility, reliability, and price/performance to the NonStop transaction processing systems. The formatted storage capacity is provided in a sealed module. The drive is at the top of a two-drive cabinet. When configured at 240 Mbytes, the plug-compatible drive mirrors the 4104 removable head drive. An external unit select plug allows address change of any 4114 to that of any other 4114 or 4104 drive. Price is $20,500. **Tandem Computers Inc,** 19333 Vallco Pkwy, Cupertino, CA 95014.

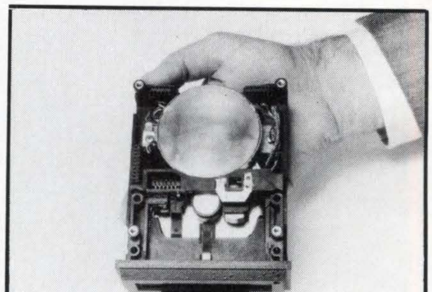
Circle 269

Winchester/cartridge subsystem

A peripheral subsystem for minis and micros, the VectorSafe series VS provides a choice of 8-in. Winchesters with 83 to 212 Mbytes and streaming cartridge tape backup. Interface options include SMD for the disk with QIC-02 for tape or the ANSI-proposed standard SCSI. Winchesters have 11.5-kbit/in. recording density and 1.2-Mbyte/s data transfer rate. Track-to-track positioning is 7 ms with 45 ms as average. Latency for all units is 8.3 ms and nonrecoverable errors are one in 10^{12} bits transferred. In 100s, prices range from $4640 to $8610 each. **Vector Electronic Co,** 12460 Gladstone Ave, Sylmar, CA 91342.

Circle 270

Backup tape drives



As a micro size unit, the 210 fits into a sub-4-in. opening. The 110 features both electronics and mechanism in a half-high, 5¼-in. form factor. Capacity is 10 Mbytes on a DC-100A cartridge using DC-600 media. Host interface is hardware compatible with SA450 minifloppy controllers. The drive features a command set via an onboard micro and can operate in either a streaming or start/stop mode so the unit can support either micro image or file by file backup. In 5000s, price is $225. **Irwin Magnetics,** 2311 Green Rd, Ann Arbor, MI 48105.

Circle 271

Tape subsystem kit for System 36

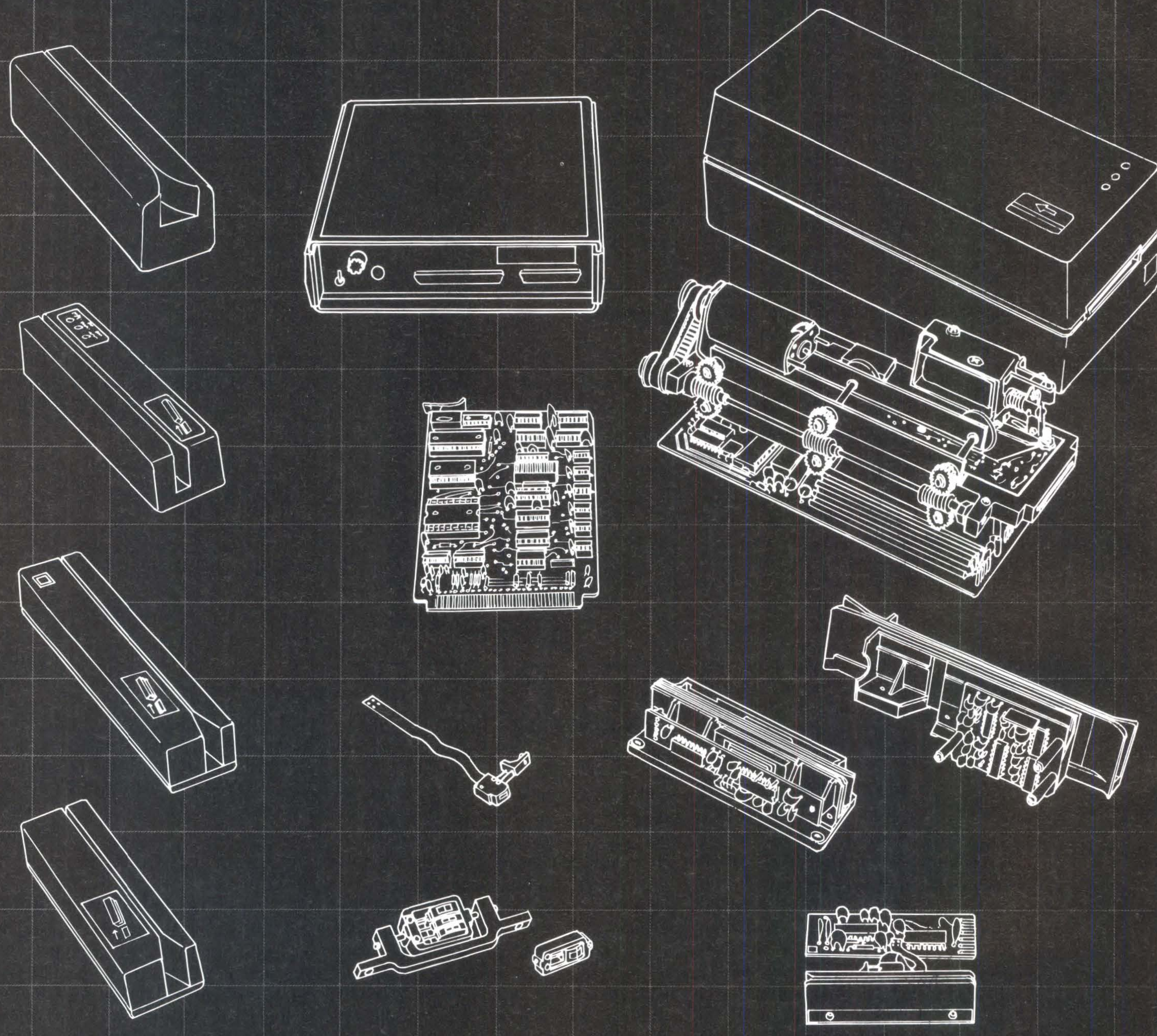
A complete field-upgradable System 34 to System 36 kit requires only firmware and software changes. The unit's hardware connects to the System 36 by twinax cable and configures as a workstation. The tape drive and controller form one hardware unit, when supplied with the appropriate software. A single command selects files/libraries to be saved or restored. An optional feature allows users to output printer data directly from the program work area to spool file or tape. **Thorn EMI Datatech, Ltd,** Spur Rd, Feltham, Middlesex, England.

Circle 272

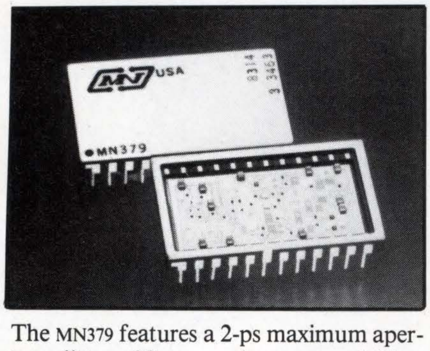
Dynamic RAM module

The HP1-6418V is a 64-Kbyte device in a 1.60- x 1.05-in. package. The compact design results in shorter current carrying distances, lower distributed capacitance, higher speeds, and fewer support components. It requires 5 V and expands in 64-Kbyte increments. With the module, a double-sided backplane instead of a four-layer motherboard can be used. Pricing, in 100s, ranges from $125 to $150. **Hybrid Packaging Technology, Inc, sub of Stanford Applied Engineering,** 760 San Aleso, Sunnyvale, CA 94086.

Circle 273



Track/hold amplifier



The MN379 features a 2-ps maximum aperture jitter, 30-ns maximum acquisition time, and a 100-MHz bandwidth. The amp slews at a minimum of 300 V/μs and drives instantaneous output currents up to ±100 mA. The chip provides stability with capacitive loads up to 500 pF. I/O voltage range is ±2.5 V; minimum gain is 0.92, and pedestal guaranteed not to exceed ±20 mV. An internal reference supplies TTL compatibility. The amp is packaged in a standard 24-pin cerDIP. Prices range from $149 to $226. **Micro Networks Co,** 324 Clark St, Worcester, MA 01606.

Circle 274

Byte-wide static RAM

Organized as 2048 words x 8 bits, the MCM2016H offers 45-ns access times. The device uses HMOS technology and design techniques that combine fully static operation features without external clocks or timing strobes. This provides a low standby power dissipation without address setup and hold times. A chip enable controls the power-down feature, using a chip control that affects power consumption rather than a clock. The chip is available in a 24-pin DIP or skinny DIP. Prices, depending on quantity, size, and access time, range from $17.60 to $44. **Motorola Inc, MOS Integrated Circuits Group,** 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 275

Edge-triggered PROMs

Available with synchronous or asynchronous enable, 63RS/RA1681 and 81A are 2048-word x 8-bit devices. The bipolar chips offer maximum clock to output times of 20 ns and 15 ns, respectively. A flexible initialization scheme offers a startup and timeout sequencing choice of 16 programmable words for controlled system startup. Synchronous devices are used when multiple registered PROMs are bused together to increase word length. The asynchronous device is used when multiple gates are not or when the outputs are gated to a bus. The 81 version costs $47.60 each and the 81A version is $61.60 each in 100s. **Monolithic Memories, Inc,** 2175 Mission College Blvd, Santa Clara, CA 95050.

Circle 276

Fuse-link PROM

A higher speed version of the MH-6616, the HHM-6616B is configured as 2 Kbytes x 8. The 16-Kbyte CMOS device offers long-term data retention and low power with maximum access time of 90 ns. Standby power supply current limit is 50 μA. The chip's polysilicon fuses provide permanent, stable data storage characteristics over a wide temperature range. Pinout is compatible with the industry standard 2716 type for upgrades. In quantities of 100, prices range from $28.60 to $85.80 each. **Harris Corp, Semiconductor Sector,** PO Box 883, Melbourne, FL 32901. 32901.

Circle 277

Speech synthesizer in CMOS

The M50800 is a single-chip speech or melody synthesizer that uses the PARCOR method. The 28-pin shrink package contains a 32-Kbit ROM, clock oscillator, D-A converter, and speaker-driving circuitry. The ROM provides a speech synthesis time of 15 to 18 s and up to 64 words of vocabulary. Chip generates a melody tone with a three-octave range for up to 60 s. Vocabulary expands by adding external memory. Initial charge is a recording fee of $1000, a speech analysis charge of $250/s, and a mask charge of $4500. **Mitsubishi Electronics America, Inc, Semiconductor Div,** 777 N Pastoria Ave, Sunnyvale, CA 94086.

Circle 278

May Preview
Special Report on
Graphics Technology

Nonvolatile byte-wide RAM

The NCR 52001 operates from a single 5-V power supply. The 1-Kbit device consists of a 128 x 8 RAM array with a duplicate EEPROM array for backup. Typical access time is less than 300 ns for each device. Maximum access times for commercial/industrial and military use are 300 and 450 ns, respectively. The RAM is suitable for applications where critical data is continually modified, and where data is to be retained during power interruption. Number of possible store cycles is guaranteed to be at least 10^4 with 1 year data retention. In 100s, price is $15.02 each. **NCR Corp, Microelectronics Div,** 8181 Byers Rd, Miamisburg, OH 45342.
Circle 279

Monolithic dc-dc converters

Accepting a single 5-V output, the AD7560 generates −5-, −10-, −15-, 10-, and 15-V outputs. The chip contains two cascaded dc-dc voltage converters, a Zener diode, an op amp, and an oscillator. User has the option of using either the onchip oscillator to drive the converters or an external clock for system synchronization. The −5-V output has a maximum source resistance of 200 Ω and a minimum conversion factor of 0.85. All outputs are short circuit protected and latchup free. The device is packaged in a 16-pin plastic DIP and is available for $4.75 in 100s. **Analog Devices,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.
Circle 280

Data communication circuits

Two CMOS circuits, the 82C52 serial controller and the HD-6406 programmable communication interface, include an asynchronous 1-Mbaud serial data rate UART. They also have an onchip bit rate generator. CMOS design allows operation from dc to 16 MHz and reduces operating power to less than 100 mW with a single 5-V supply. Programmable via a standard bidirectional bus, the chips' bit rate generator allows one of 72 different data rates to be selected. Prices for the devices range from $12.10 each to $59.40 each in 100s. **Harris Corp, Semiconductor Sector,** PO Box 883, Melbourne, FL 32901.
Circle 281

COMPUTERS

Multi-user micro system

With a standard 6-MHz Z80B CPU for the master and a Z80A for each of the two to five individual slaves, the QDP-400 provides high system throughput. It uses the Turbodos operating system to provide a CP/M-compatible environment. It features a 1.2-Mbyte (formatted) 5¼-in. Winchester drive and a 60-Kbyte transient program area. Menu-driven configuration allows the user to configure peripheral devices. The master has 128 Kbytes of bank-selectable RAM expandable to 256 Kbytes, while the slave has 128 Kbytes expandable to 512 Kbytes. Prices range from $9995 to $12,995. **QDP Computer Systems,** 10330 Brecksville Rd, Cleveland, OH 44141.
Circle 282

Supermicro with performance disks

Offering 66 Mbytes of disk storage, the Model 11-Plus features average access times of 30 ms. The system also offers 512 Kbytes of parity memory (expandable to 1 Mbyte), and a 17-Mbyte tape cartridge for backup. The unit comes standard with one high performance 33-Mbyte Winchester drive, expandable to two and measures 26 x 18 x 8 in. The 11-Plus with one drive is available immediately for $18,950; the second drive will be available in the second quarter of this year for $5950. **Zilog Inc,** 1315 Dell Ave, Campbell, CA 95008. **Circle 283**

High performance portables

Weighing in at about 10 lb, the model 1100 features a full-sized, flat-panel screen, 384 Kbytes of nonvolatile bubble memory, 256 Kbytes of RAM, and Intel's 8086/8087 processors. Model 1109 comprises a modem and 512 Kbytes of RAM. It uses Hitachi's 256-Kbit chips for large memory capacity. Disk storage options include a portable 360-Kbyte drive, 10-Mbyte hard disk/360-Kbyte floppy storage, or file server. A single GPIB interface support up to 15 peripherals. Model 1100 is $5595 and the 1109 is $7995. **Grid Systems Corp,** 2535 Garcia Ave, Mountain View, CA 94043.

Circle 284

VMEbus-based, multi-user system

Combining the 16-bit VMEbus with Unix, the VME Matrix 68K is designed around the MK68000 micro. The system features a 10-slot card cage with three slots for system expansion. There are seven cards within the system: memory management CPU, system controller, SASI interface, serial I/O, two DRAMs, and a floppy disk controller. Main memory is 640 Kbytes on DRAM boards and in the memory management CPU. The configuration runs under the Unix-derived UniPlus operating system. Other software includes a C compiler, 68000 assembler, and system diagnostic package. Price is $16,500. **Mostek Corp, sub of United Technologies Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 285

Database computer system

Harnessing the power of 1024 microprocessors operating in parallel, the DBC/1012 handles data volumes from megabyte files to tera byte data bases. The machine attaches to an IBM (or equivalent) mainframe, relieving it of the burden of maintaining a data base. There are two functional processors—an interface processor that translates host requests into internal commands, and an access module processor that performs required data manipulations. The basic system is priced at $480,000 and includes six micros, 1.9 Gbytes of data storage, and full relational DBMS software. **Teradata Corp,** 12945 Jefferson Blvd, Los Angeles, CA 90066.

Circle 286

INTERFACE

Vector processor

The VP-10 controller allows the connection of raster output devices to a mainframe. It eliminates host computer overhead associated with the vector-raster conversion task. The processor accepts random vectors, symbols, and other graphic information from a host, translates the data at computer speed, and drives various outputs. Capacity is 200,000 vectors. Features include a 128-Kbyte memory expandable to 2 Mbytes, color support for both intensity modulated and dithered devices, diagnostics, and integrated communications. **KMW Systems Corp,** 8307 Hwy 71 West, Austin, TX 78735.

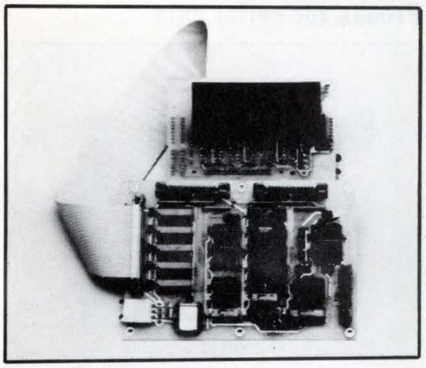
Circle 287

Memory mapped frame buffer

The MFB-512 provides 512 x 512 x 8 frame memory for realtime image acquisition, manipulation, and display. The buffer is designed for image processing applications requiring rapid access to image data or high transfer rates. It enables the user to map all or part of the buffer memory directly into the host's address space. The pixel transfer rate can be every 400 ns over the Multibus. Two adjacent pixels are packed into a single-word transfer when the host is a 16-bit processor. Price is $3995. **Imaging Technology, Inc,** 400 W Cummings Pk, Woburn, MA 01801. **Circle 288**

CIRCLE 158

Encoder interfaces



The devices are designed to simplify interfacing between optical encoders and the system environments. Combining one or more modules allows for connection to displays, controllers or computers, or the formation of standalone process control stations. The three interface groups include direct interface, standard bus, and voltage translators. Direct interface modules do not require programming. STD bus modules are fully programmable and can be used with a keyboard/display panel for local control or monitoring. Voltage translator modules permit combinations of supply voltages and logic levels to be used with any encoder. **BEI Electronics, Inc, Position Controls Div,** 819 Reddick St, Santa Barbara, CA 93103.

Circle 289

Multibus communication board

The Com-1 is a single-board communication controller. A bidirectional 16-bit parallel port provides a high speed interface to a DEC DR-11W interface card. Data rates are up to 400 kwords/s. Three serial channels conform to the RS-232-C interface standard and use RS-423 line drivers and receivers to accommodate rates of 307.2 kbaud. Two DMA controllers support DMA between Multibus memory and I/O ports. Price is $2495. **Matrox Electronic Systems Ltd,** 5800 Andover Ave, Montreal, Quebec, Canada H4T 1H4.

Circle 290

Doubled capacities in interfaces

Designated the SN54/74LS793 (8-bit latch) and -94 (8-bit D flipflop), the interfaces combine two separate functions into one 20-pin package. Both devices are low power Schottkys that read stored data back onto an input bus on demand. Read-back capabilities allow register or latch data through input pins and then read back through the same pins. When used directly on a system bus, the components can implement a stack, hold a pointer, or implement a scratchpad memory. Commercial version is priced at $3.51 in 100s. **Monolithic Memories, Inc,** 2175 Mission College Blvd, Santa Clara, CA 95050.

Circle 291

Disk controller

The SC72 permits intermixing of disk drive types, using the same controller, on DEC PDP-11/70 CPUs. It was designed to operate on the cache bus using standard system software and diagnostics without alteration. Using existing CPU backplane slots, it embeds directly in place of DEC's RH70. Any four industry-compatible disk drives, operating at data transfer rates up to 2 Mbytes, can be integrated into a single subsystem. Controller microprogramming provides 32-bit ECC for data error correction/detection on single-bit error bursts. Price is $7950. **Emulex Corp,** 3545 Harbor Blvd, PO Box 6725, Costa Mesa, CA 92626.

Circle 292

Oncard bus controller and RTU

The BUS-65500 is a dual-redundant MIL-STD-1553 bus controller and RTU with a VME interface. It provides a complete intelligent controller and RTU between a serial MUX data bus and a parallel VME bus. Supporting all message formats, it implements 11 mode codes and provides complete wraparound built-in test capability. The board includes a 4-K x 16-bit dual-port memory, six subsystem command registers, and four interrupts. Prices are $7695 each. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.

Circle 293

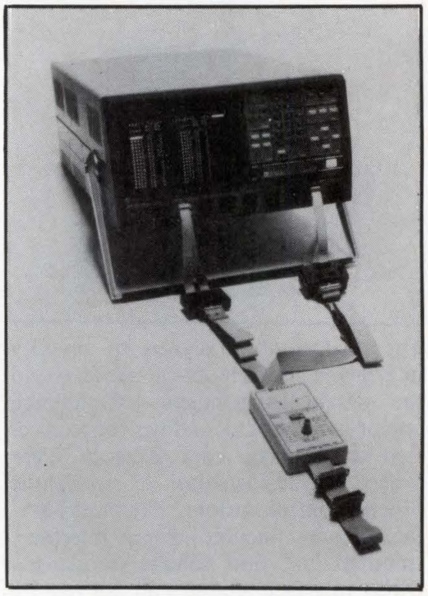
Talk to the editor
Have you written to the editor lately? We're waiting to hear from you.

Portable scopes

Both 2213A and 2215A incorporate standard features such as a 10-MHz bandwidth limit switch, a single sweep mode and power-on light, and separate A/B dual-intensity modes (for the 2215A). Vertical accuracy is specified over a wider temperature range than previous models, while sweep accuracy (in 10X) has increased. The 2213A weighs in at 12.8 lb while the 2215A weighs 13.5 lb. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

Circle 294

Probes for serial data



The SIP 80E interface probe configures the front end of a logic analyzer for analysis of asynchronous V.24/V.28 serial data. It connects into a serial communication link through standard RS-232-C, 25-pin D-connectors. The device converts each serial character into a parallel data format for storage in memory. Displays are available in ASCII, binary, hexadecimal, and octal. Features include the ability to monitor a serial link's send and receive lines (simultaneously or individually), and the ability to transmit any selectable ASCII characters on those lines. The probe accommodates data rates to 19.2 kbaud. Price is $1300. **Dolch Logic Instruments, Inc,** 3052 Orchard Dr, San Jose, CA 95134.

Circle 295

Test module for A-D

Designed for use with TM-7A and TM-7B linear test heads, the converter configuration card allows a variety of ac and dc tests on industry standard A-D converters. It features hardware-controlled logic to ensure high speed device testing from 6 to 14 bits. This module performs full dc parametric tests on all pins. It can also measure all device power supply currents. The hardware tests devices with internal or external references, various binary output codes, and direct or bus interface I/O. The card sells for $4500. **Pragmatic Designs, Inc,** 950 Benicia Ave, Sunnyvale, CA 94085.

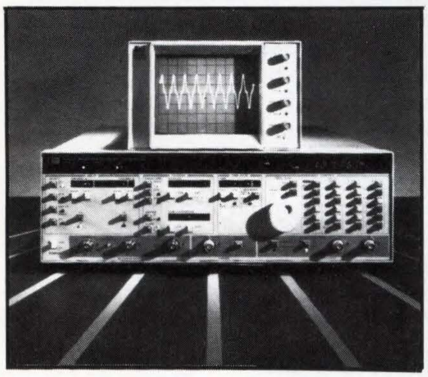
Circle 296

Dual-channel oscilloscope

The 1580 is a 100-MHz, dual-time base scope with a 5-mV/div vertical sensitivity over the bandwidth. Vertical sensitivity to 50 MHz is 1 mV/div in the X5 mode. V mode displays two signals unrelated in frequency. User can select from 23 calibrated sweep time ranges—0.5 s/div to 20 ns/div in 1-2-5 sequence. Signals are displayed on an 8 x 10 div (1 div = 10 mm) rectangular CRT with internal graticule and 16-kV accelerating potential. Price is $1995. **B & K-Precision/ Dynascan Corp,** 6460 W Cortland St, Chicago, IL 60635.

Circle 297

Waveform recorder/generator



The HP 5182A combines high speed waveform capture with arbitrary waveform generation. It captures input waveforms with a 20-MHz, 10-bit A-D converter and stores them in memory. Waveforms can be regenerated one at a time in single-slot mode, or pieced together end to end for a continuous waveform. The unit has 16,384 words of memory that can be segmented into 32 separate records. Captured records are maintained in battery backed CMOS memory for easy transport. The price is $23,000. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 298

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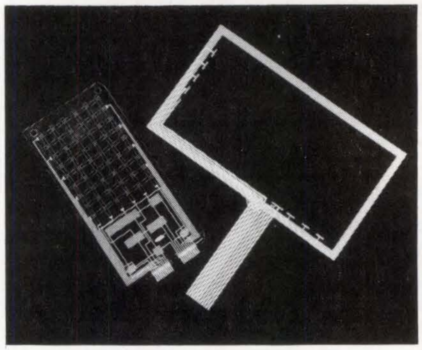
Broadband transistors

Operating in the 13- to 15-GHz frequency range, models C2421H-1500 and C2422H-1500 FETs are made of GaAs. The single- and dual-cell power transistor chips, which mount on internally matched chip carriers, operate in a 50-Ω system over a full 2-GHz bandwidth. The devices cascade directly for multistage amplifier applications and/or combine with quadrature couplers to achieve higher power levels. Prices start at $343. **Hughes Aircraft Co, Electron Dynamics Div**, PO Box 2999, Torrance, CA 90509. **Circle 299**

Membrane switches



Designed to be placed directly over CRT, LED, plasma, or backlit control panels, TT/GTC and TT/FCM retain a see-through area of 90 to 100 percent. The TT/GTC version uses a gold deposition technique for unobstructed viewing area. The TT/FMC version uses fine-line, 5-mil conductors, which makes them virtually invisible during normal operation (with transparent legend filter overlay). The transparent devices test at over 1-M actuations per switch and meet military specifications. Price ranges from $55 to $500 (quantity 25). **CAM Graphics Co, Inc,** 145 Toledo St, Farmingdale, NY 11735. **Circle 300**

Flat-profile CRT

Flatness of the FP series is measured in terms of a 50-in. radius with common CRT radii being 20 to 25 in. The flat design improves text and graphics readability because it eliminates the curving at the edge of the screen. Wedging (thicker glass on corners and edges) is also eliminated for uniform screen brightness. The screen is available in a 12-in. diagonal version to serve the popular terminal size. It has the same ear mounting holes and the same 3 to 4 aspect ratio as standard 12-in. tubes. **Clinton Electronics Corp,** 6701 Clinton Rd, Rockford, IL 61131. **Circle 301**

Touch screen with software support

A touch-sensitive screen for the VT100, the Management-Touch is based on a capacitive touch technique. It allows the VT100 terminal to be used in normal input mode, touch-only mode, or a combination of the two. The screen can be ordered in either a 32-zone or continuous X-Y format and is supported with diagnostic and application software routines. Under program control, options enable and disable the screen and keyboard. **Tentime, div of Research Information Corp,** 5375 Western Ave, Boulder, CO 80301. **Circle 302**

Sealed relays

The 1575S series consists of low cost miniature 3-A relays. Their size is suitable for high density packaging and terminals mount directly to a PC board. The relays have both UL and CSA approval. Sealing makes the relays impervious to a water wash at 170 °F (77 °C). Mechanical life is 1 million operations, while the expected electrical life is 100,000 operations minimum at rated load. Units come in 6 to 48 Vdc with 100- to 6400-Ω coil resistances, respectively. Maximum time values are 15 ms for pull-in/drop-out. **Guardian Electric Manufacturing Co,** 1550 W Carroll Ave, Chicago, IL 60607.

Circle 303

Calendar/clock CMOS module

Designed for MicroVAX I and 11/73 and other LSI-11 systems, the C-Timer comes in a dual-wide Q-bus module. It includes watchdog timer and 2-K x 16-bit CMOS RAM for user-defined functions. The watchdog timer automatically reboots a system when a hardware/software problem hangs it up. The device provides time and date information from 0.1 s to years. The RAM provides 2048, 16-bit words of memory. Complete software support incudes source code listings for RT-11 and RSX-11 operating systems. Price is $395. **Codar Technology Inc,** 1428 Florida Ave, Longmont, CO 80501.

Circle 304

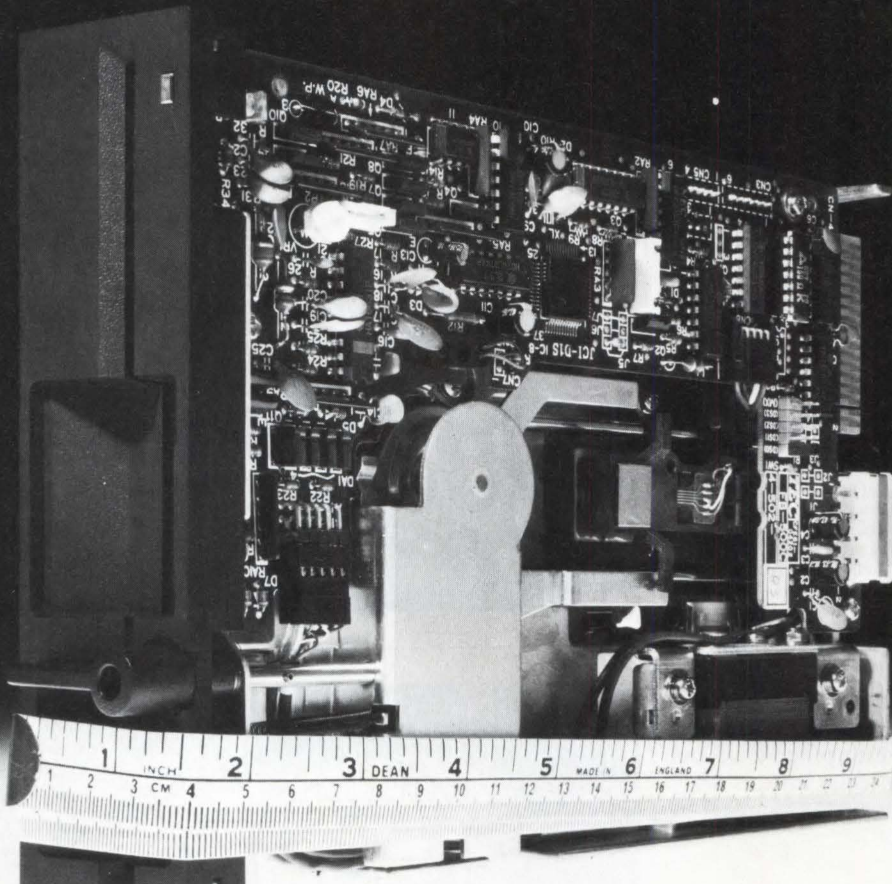
Touch-sensitive panels

Rows of LEDs and phototransistors in EMS panels surround a display, producing a grid of infrared light beams across the screen's surface. Touching a finger or stylus to the screen interrupts the light beams, which in turn transmits touch data to the host. The panels configure with an opto frame and logic circuitry; the frame contains an LED-transistor matrix, multiplexer switches, and light and noise reduction circuit. Two configurations are available: box frame for most CRT displays, and window frame for flat displays. **Electro Mechanical Systems, Inc,** 801 W Bradley, Champaign, IL 61820.

Circle 305

May Preview
Watch for a special article on VLSI circuits

HALF-SIZE 5¼ INCH FLOPPY DRIVES FROM NSA



Smaller. Faster. Shugart compatible. With a new standard of reliability.

Introducing a family of super thin, mini floppy disk drives that measures up to the most demanding OEM specifications. NSA's new FB500 Series offers 3 msec. track-to-track access at 96 TPI (6 msec. at 48 TPI). Their compact 41 × 146 × 209 mm size lets you install two in the space normally allotted for a single conventional drive. And their Shugart plug compatibility enables easy integration without hardware or software modifications.

Manufactured by Tokyo Electric Company, Ltd., the drives are virtually maintenance-free. Offer fail-safe disk insertion. One-step ejection. Long-life ceramic heads. Advanced stepping motor design. Direct drive, brushless DC motors. 250–1,000 KB capacity. And a MTBF you'll have to test for yourself to believe. Call or write today for an evaluation unit and complete details.

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CIRCLE 167

Single-board computer

The IBM PC's bus structure forms the base of the R188 computer. It uses an 80188 processor operating at 4.77 MHz and is upward compatible with 8088 software, but allows use of the 80188 expanded instruction set. The board includes processor, 64-Kbyte dynamic RAM, 160 Kbytes of user erasable PROM, and RS-232-C serial console port. A Basic I/O system ROM supports the software interrupts used by the PC so software can directly execute on this system. A debugging ROM routine is also available. Price is $795. **I-Bus Systems,** 9235 Chesapeake Dr, San Diego, CA 92123.

Circle 306

Programmable EPROM micro

An 8-bit micro, the MC68704P2 is implemented as a 1-bit serial processor. Transfers, arithmetic operations, and address operations are done serially. It contains 1024 bytes of user-programmable EPROM, 64 bytes of data space EPROM, 320 bytes of self-check ROM, 32 bytes of RAM, 2½ 8-bit parallel I/O ports, and an 8-bit timer. The chip stacks four levels of subroutines and supports an external interrupt. A breakpoint register simplifies debugging programs. Pricing in quantities of 1000 is $7.75 each. **Motorola Inc, MOS Microprocessor Div,** 3501 Ed Bluestein Blvd, Austin, TX 78721. **Circle 307**

Multi-user, single-board computer

The Multibus-based MLZ-92A has the capability of running a multi-user operating system without the need for additional cards. Based on the Z80A, the board has up to 128 Kbytes of parity protected DRAM. Hardware arbitration allows communication with the Multibus as a master, slave, or in multimaster mode. Interfacing is via four RS-232 serial ports. For mass storage peripherals, computer has oncard hard disk interface and streaming tape interface. Ports are set up for onboard DMA. **Heurikon Corp,** 3001 Latham Dr, Madison, WI 53713.

Circle 308

Processor for S-100 systems

An 8086 board delivers true 16-bit high speed performance to the S-100 bus. An 8-MHz version is used with the 8-MHz 8087 numeric data processor. The board has a memory address range to 16 Mbytes. It acts as a standalone CPU, with the SCP-301 CPU support board, or as part of a three-card CPU/CPU support/MMU set. The support card includes two serial ports, a parallel port, five 16-bit timers, a vectored interrupt controller, and an EPROM socket. A 10-MHz version is also offered. **Seattle Computer Products, Inc,** 1114 Industry Dr, Seattle, WA 98188.

Circle 309

Let's hear from you

We welcome your comments about this issue. Just jot them on the Reader Inquiry. Card.

CIRCLE 168

The K105-D analyzer with Trace Control™ helps you find faults quickly and easily.

For most engineers, the frustration is not in solving the problem. But in finding it.

Not anymore. Take the Gould K105-D logic analyzer. It can help you isolate errors and their causes quickly and easily. Because now you can capture and examine several possible cause areas with a single pass.

Advanced program tracking and data capture.

Flexibility is the key.

With 8 levels of Trace Control, you can follow every bend and turn in your program flow. No matter how complex. And capture widely-separated slices of code better than any other triggering method.

Although faults and their causes may be separated by thousands of lines of code, the K105-D records only what you want to see.

Once captured, the K105-D brings these windows of information directly to the screen for your analysis.

This selective recording conserves memory. While it helps you get at the problem—and solve it—in less time than ever before.

An analyzer that speaks your language.

The K105-D speaks simple assembly language, not complex object code. Quite fluently, we might add.

With our disassembly modules for the 68000, 8086, 8080, 8085A and Z80® B microprocessors, you need only one analyzer for debugging most popular processors.

Clear, concise pattern definitions.

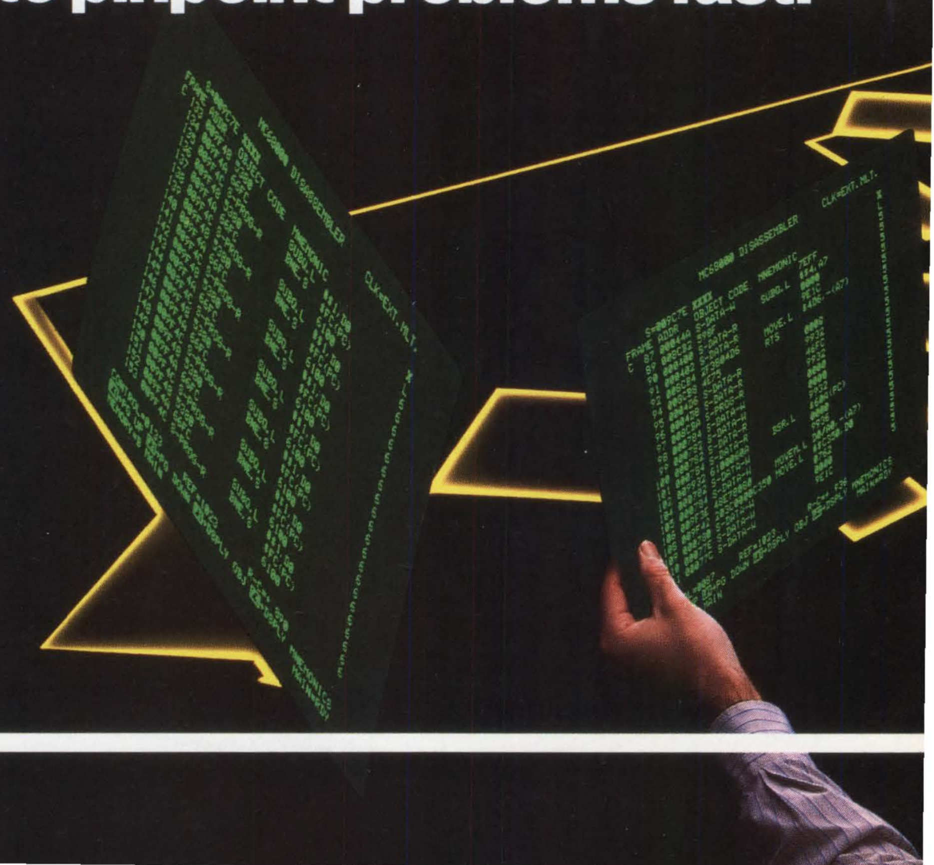
With the K105-D, you can define all your event patterns with symbolic labels. These labels can represent address locations, data values, fetched instructions or any control signal you're monitoring.

And since you create them, they're easier to understand and remember.

What's more, Trace Control uses English-like commands which make for shorter set-ups. Quicker comprehension. And a more productive engineer.

To make debugging even easier, add the optional dual floppy disk drive. With it, you can store up to 35 set-ups and associated recordings on a single diskette for instant recall.

Now, capture up to 4 segments of complex program flow to pinpoint problems fast.



You won't get caught in a loop.
By using the K105-D's loop counter, you can follow a sequence of events for a specific number of iterations. Then stop at will.

It's a quick way for you to test the repeatability of a program function. And verify that your code is having the predicted effect.

Integration made easy.
For the hard part (hardware/software integration), now there's a simpler solution. The K105-D's 100 MHz high speed link.

It's an extremely precise way to see how timing affects software execution. And vice-versa.

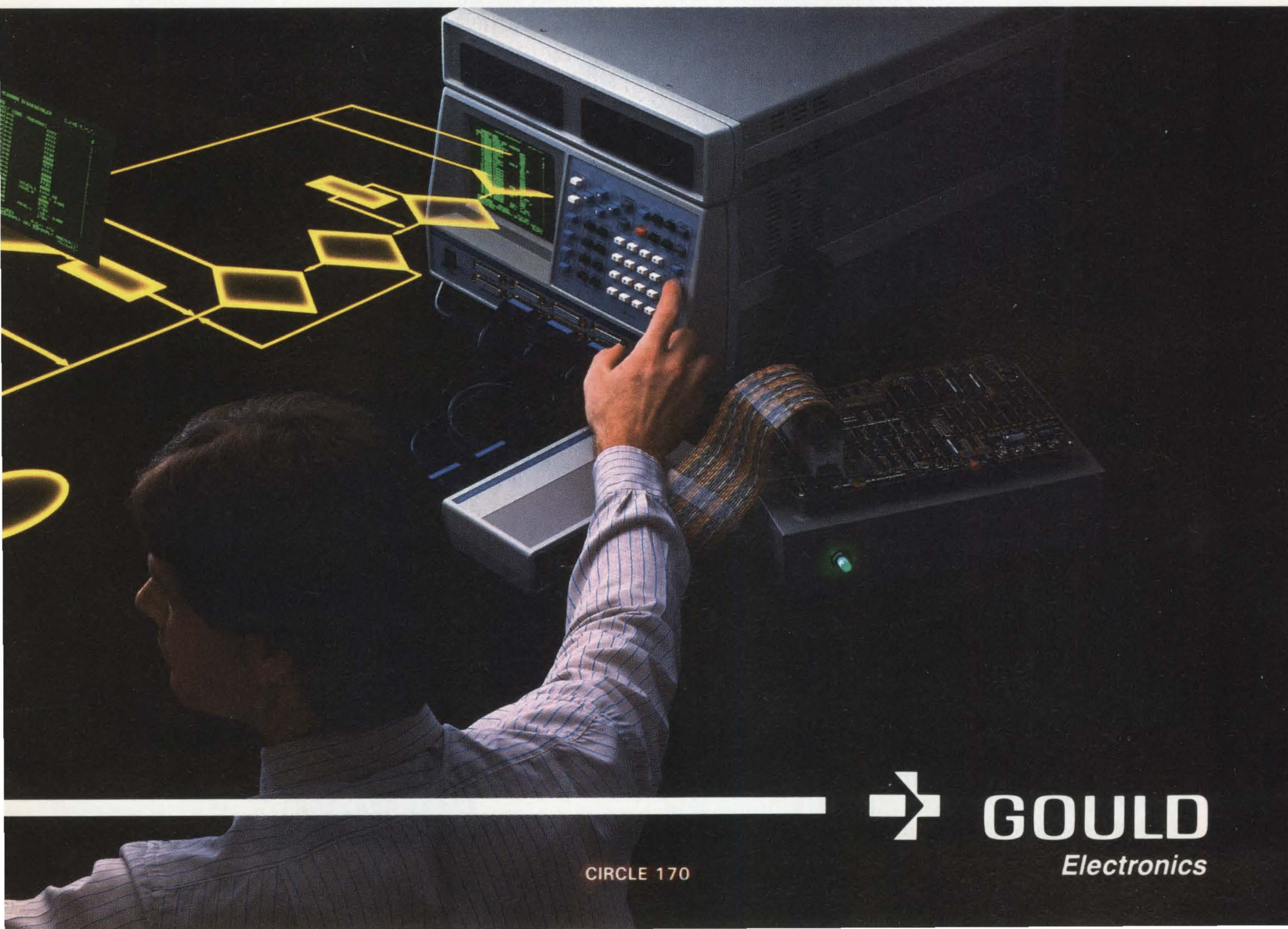
Again, for this task, Trace Control can help you track down hard-to-find faults. So you end up with a program that flows smoothly. Error free. In a fraction of the time it used to take.

Performance above all the rest.
At Gould, we engineer every instrument to be clearly the best in its class.

So now with your insight and the K105-D analyzer, you can capture the problem. And solve it. Fast.

For the name and number of your nearest Gould sales representative or for a detailed brochure and application notes, call us toll-free at (800) 538-9320. In California, call (800) 662-9231 or (408) 988-6800. Or write Gould, Inc., Design & Test Systems Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050-1279.

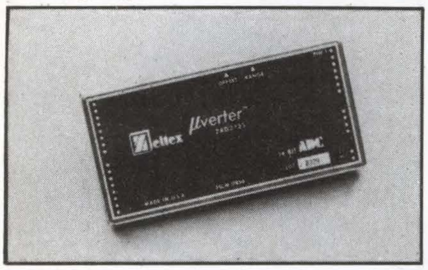
The K105-D gives you two levels of HELP at the touch of a button. First, step-by-step operating instructions that appear along the bottom of the analyzer screen. Second, a menu that allows you to select more detailed "help" should you need it.



CIRCLE 170

GOULD
Electronics

Analog-digital converter



The 14-bit ZAD 2725 features a 7-μs conversion rate, guaranteed monotonicity, and low linearity error drift. Differential nonlinearity is ± ½ LSB maximum (0.003 percent FSR). Three-state latches ease interface to 8-bit data buses. Mounted in a compact metal case measuring 2.0 x 0.4 in. (5.1 x 1.0 cm), the device provides six-sided protection from rfi noise typically experienced in micro systems. In 100-piece quantities, the converter is priced at $195. **Zeltex, div of Silicon General, Inc,** 940 Detroit Ave, Concord, CA 94518. **Circle 310**

Parallel output A-D ICs

Two 8-bit data acquisition chips are fabricated with silicon-gate LinCMOS technology. The TLC532A and TKC533A perform 67,000 and 33,000 A-D conversions and samples/s, respectively, at their maximum clock speeds of 4 and 2 MHz. Accuracy is ± ½ LSB. Typical power dissipation is 6 mW. Each chip includes an 8-line, TTL-compatible, three-state bidirectional data bus. In addition, each chip contains a 12-channel MUX, control logic sample and hold, and three 16-bit data registers. The devices are packaged in 28-pin DIPs. The 100-piece price ranges from $5.69 to $7.93. **Texas Instruments Inc, Semiconductor Group,** PO Box 401560, Dallas, TX 75240.

Circle 311

Replacements for D-A converters

Manufactured to MIL-M-38510 class B, the AD DAC85 and AD DAC87 have an MTBF of 161,000 hours. The D-A converters dissipate 450 mW maximum. Features include operation wihout a 5-V power supply and operation with either a ±12- or ±15-V supply allowing direct replacement of either standard or Z versions. Settling time is 3 μs maximum to ±0.01 percent. Maximum unipolar and bipolar offset drift is ±3 and ±10 ppm/°C. Maximum gain drift is specified at ±20 ppm/°C, including internal reference drift. Pricing in 100s is $32 and $75, depending on the version. **Analog Devices,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. **Circle 312**

Multibus-compatible expander

When used with the MP8418 analog input board family, the MP8418-ISOE provides an additional 16, 32, or 48 isolated input channels. The board uses a flying capacitor technique to provide 400-V input and channel-to-channel isolation. Low thermal emf relays minimize errors in low level operation. A low pass filter on each input provides 60-Hz normal mode rejection. In quantities of 1 to 49, the board costs $750. **Burr-Brown,** International Airport Industrial Park, PO Box 11400, Tucson, AZ 85734.

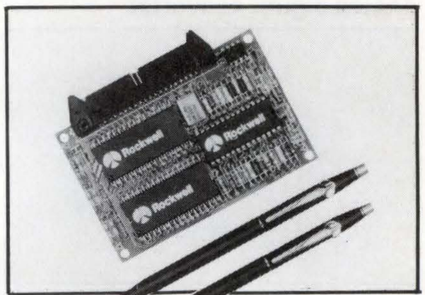
Circle 313

Intelligent standalone modem

Containing 48 Kbytes of battery-backed memory for sending, receiving, and storing messages, the Visionary 1200 features auto-send and receive. It transmits at either 1200 or 300 bits/s and includes two serial ports. The device contains a Bell 212A modem and an 8085. Auto features include answer, dial, redial on busy, answerback, log on, data capture and retrieve. Data format is binary, serial, asynchronous, 7 or 8 data bits, 1 or 2 stop bits, odd, even, or no parity. The modem transmits either half or full duplex. Prices range from $795 to $1095. **Visionary Electronics,** 141 Parker Ave, San Francisco, CA 94118.

Circle 314

Modem card



Half-duplex 9600-bit/s R98FAX meets CCITT recommendations V.29 and V.27, T.30, and binary signaling capabilities. Auto-adaptive equalization maintains reliable synchronous and asynchronous communication over unconditioned lines. Together with an RS-232 port, a micro bus interface simplifies host integration. Based on a proprietary VLSI three-chip set, the modem measures 100 x 65 mm and operates from supplies of 5 and ±12 Vdc. It consumes 2 W. In 1000s, price is $310 per unit. **Rockwell International, Semiconductor Products Div,** 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660.

Circle 315

Smart modem

Two LSI chips make up the Operator 103: one is a single-chip micro for all control functions, and the other a modem chip that includes the necessary filters. The auto-dial, auto-answer device uses the command interpreter developed for the automatic calling unit. It provides normal and fast speed pulse dialing and runs at 300, 200, 150, and 110 baud. Users need type only the first letter of commands and the modem echos the full command word. Price is $189. **TNW Corp,** 3444 Hancock St, San Diego, CA 92110.

Circle 316

Host interface unit

A 32-port version of the Unibus host interface, the XP-UN32-A converts terminal subsystem of VAX from a character at a time to a fully intelligent message processor. It provides the system with equivalent capabilities of the IBM 3270 terminal family. The host interface unit acts as the 3725 front end; a cluster controller provides the functions of the 3274 controller and the 3278 terminal. The unit's DMA capability on I/O data handling removes character processing from the VAX. **Xyplex, Inc,** 100 Domino Dr, Concord, MA 01742. **Circle 317**

Communication controller for VAX

An intelligent frontend processor, the KCT32 is designed for networking and custom applications. Supporting software enables it to run under the VAX/VMS operating system. The controller has 56 Kbytes of user-programmable memory and implements the PDP-11 instruction set. Using a single hex-wide board, the unit installs by line, for bit/byte-wide synchronous or asynchronous data transmission and reception. It supports two lines at 64 kbaud per line, or a single line at 130 kbaud, full duplex. Prices range from $6900 to $7400. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.

Circle 318

Data communication tester

The DCT-100 provides industry standard breakout panel with the ability to print received or transmitted data stream. This printout is on a 20-col thermal printer. It provides absolute verification of transmitted data and commands and allows time to analyze and study them. A baud rate detection mode is available. The printer has three switch-selectable print formats; ASCII characters only, ASCII characters and control codes, or hexadecimal values for all codes. Prices range from $795 to $995, depending on quantity. **Telpar, Inc,** 4137 Billy Mitchell Rd, Addison, TX 75001.

Circle 319

Communication systems

Two versions of Era 2 create hardware/software communication systems for micros—one for the IBM PC and one for the Apple IIe. Each includes communication software, a 1200-baud modem, manual, and telephone cord. Bell 212A or 103-compatible modem is FCC certified, and can transmit at full or half-duplex. The system provides auto-answer, and pulse or tone dialing asynchronously. Software gives online printer control and maintains up to 33 digits/stored telephone number. Price is $429 per unit. **Microcom, Inc,** 1400A Providence Hwy, Norwood, MA 02062.

Circle 320

Talk to the editor
Have you written to the editor lately? We're waiting to hear from you.

CIRCLE 190

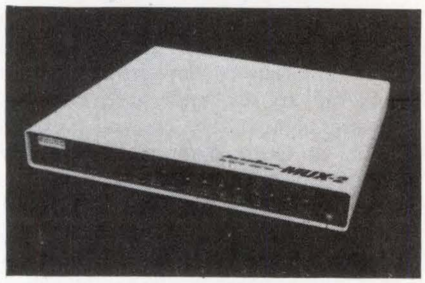
CIRCLE 174

Terminal concentrator

Reducing the cost of access to public and private data communication networks, the ATC can serve up to eight users simultaneously. It performs automatic, independent speed detection in a 110- to 9600-bit/s range for each asynchronous terminal port. Two standard network ports support speeds from 2400 to 9600 bits/s. RS-232-C modem control signals are available on all ports. The ATC also has hardware diagnostics including complete communications and remote reporting software for both terminal and network connections. Price is less than $3500. **Tymnet, Inc,** 2710 Orchard Pkwy, San Jose, CA 95134.

Circle 321

Data compression unit and stat MUX



Supporting either two 1200-bit/s or two 2400-bit/s data streams, the turboMUX-2 combines data compaction with a two-channel stat MUX. It offers error detection and retransmission features. Transmission mode is selected via front-panel switches. Local and remote diagnostics are standard. The device attaches with RS-232-C connectors and transmits over a single Bell 212A or compatible modem. **Chung Telecommunications,** 4046 Ben Lomond Dr, Palo Alto, CA 94306.

Circle 322

Telecommunication processor

An advanced X.25-based communication network node, the Telepac II provides direct interface to composite traffic from stat MUX networks. This micro-based system has automatic callout to X.25 public data networks. Alternately, users can be routed to multiple hosts from a single terminal interface. Up to 250 terminals per node can be dynamically routed to user specifications. This includes host port contention and resource queuing. Depending on configuration, throughput ranges from 10,000 chars/s to 1.2 Mbytes/s through a single node. Prices start at $9000. **Telefile Computer Products, Inc,** 17131 Daimler St, Irvine, CA 92714.

Circle 323

Communication translator

The user-configurable PCT-100 is an RS-232 interface with two bidirectional ports. A communication translation language (CTL) is internally implemented so users can configure the device to almost any translation algorithm. Using CTL, the unit performs terminal or printer emulation and provides compatibility and macro-function keys for software applications. Other features include type-ahead and data buffering, baud rate adaptation, DEC and IBM compatibility and handshake protocol conversion. Cost is $369. **Method Systems Inc,** 19751 S Lakeshore Blvd, Euclid, OH 44119.

Circle 324

CIRCLE 175

Full-duplex modem

The 224 SD runs at 2400 bits/s and combines a three-port stat MUX, error correction, and auto-dialing. It is intended for applications involving multiple asynchronous devices with error-free data communication requirements. The stat MUX supports 14 synchronous port speeds from 50 to 9600 bits/s and an auto-baud port for automatic matching. As an auto-dialer, the system supports both pulse and tone dialing. it will fall back to match the speed and modulation of an incoming call for a remote 212 modem. **Concord Data Systems,** 303 Bear Hill Rd, Waltham, MA 02154.

Circle 325

Expander for auto-testing

The AMO series equips one RS-232 serial port to drive from 8 to 32 RS-232 devices. Control codes in the data stream direct serial input to the respective output. All 25 lines of bidirectional data flow can be supported. Realtime switching via user-selectable code makes units suitable for test and burn-in of multiple printers, plotters, modems, and workstations. The units provide the RS-232 line with the same expansion capability as the IEEE 488 bus. Prices start at $1843. **Advanced Systems Concepts, Inc,** 434 N Lake Ave, Pasadena, CA 91101.

Circle 326

Simultaneous voice/data modem

The SPM-94A allows the transmission and reception of full-duplex voice plus half-duplex asynchronous data at speeds up to 300 bits/s. The modem creates a low speed data channel within a portion of the voice band; using proprietary filtering techniques, it suffers no significant voice quality degradation. Interface modules allow the device to meet specific requirements of data terminals or CPUs. Five front-panel LEDs are provided for monitoring operation and diagnostics. **Coherent Communications Systems Corp,** 60 Commerce Dr, Hauppauge, NY 11788.

Circle 327

Packet network concentrator

Advanced network processor 2520 uses CCITT X.25 and ISO level 3 structure, providing a public or private data network interface. It features 300-packet/s throughput, multiple protocol support, management through a centralized network controller, and optional redundancy for unattended locations. The system has a distributed, modular 16-bit micro architecture allowing the user to build processing power as needed. Other features include variable port size configurations and multiple high speed trunks up to 64 kbits/s. **Databit Inc,** 110 Ricefield Ln, Hauppauge, NY 11788.

Circle 328

Multiport transceiver

The DS3695 accommodates up to 32 drivers and receivers on one transmission line. Extended common mode range permits the implementation of a multiport differential bus. Capable of data transmission over a 4000-ft line at 100,000 baud, or a 40-ft line at 10 Mbaud, the transceiver is suited for high speed serial data transmission. Thermal shutdown protects against faults. Glitch-free power-up/down protection is provided at driver outputs. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Circle 329

Bell-compatible modem board

Capable of accessing telephone systems at either 300 or 1200 baud, the SB8630 equips STD bus systems to use phone lines for communications. In Bell 103 mode it can be used full-duplex at 300 baud and in 202 mode it operates half-duplex at 1200 baud. Features include auto-answer, auto-dial, and auto-originate for both pulse and touch-tone dialing. Interface is via an existing RS-232-C or RS-422 serial I/O port. This interface is compatible with all Micro/sys serial I/O boards for the STD bus. In quantities of 10, price is $540 each. **Micro/sys,** 1367 Foothill Blvd, La Canada, CA 91011.

Circle 330

It pays to communicate

You can further your career by writing technical articles about the advanced work you're doing. Also, we pay an honorarium for all manuscripts that we publish. For a free copy of our Author's Guide, circle **502** *on the Reader Inquiry Card.*

A DRAMATIC ADVANCE IN HALF-HEIGHT WINCHESTERS...

STRAIGHTALK

With all the claims and counter-claims regarding capacities, availabilities and shipments of half-height 5.25" Winchesters, it's sometimes difficult to determine the facts.

FACT. In early 1983, Microscience asked over 40 OEMs to participate in a 120-day evaluation program of our HH-612 10 MB half-height drives.

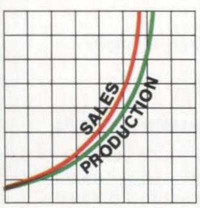
We randomly selected 150 drives for these field tests.

The evaluation proved that Microscience has the performance, quality and price today's small business and portable computer manufacturers demand.

FACT. Microscience ended 1983 with a significant order backlog. We could have shipped more, but we will not sacrifice quality for quantity.

1%

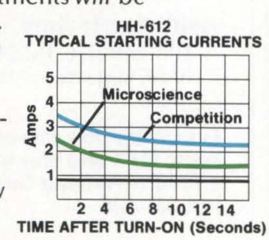
Our returns are less than 1%. Every drive undergoes rigorous testing in our advanced, computer-controlled test facilities.



FACT. Microscience is rapidly expanding its highly automated manufacturing operation in California.

By the end of the first quarter, 1984, we will be able to meet more of the demands of large OEMs and distributors. And by the end of the year we will have expanded production by a factor of five.

Until then, when we commit to a quantity and shipment date, those commitments *will be met.* No ifs... no ands... no buts.

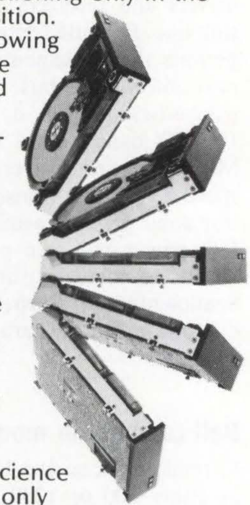


FACT. Microscience disk drives have extremely low voltage requirements... the lowest in the industry.

Small business and portable computers don't have the luxury of a lot of excess power capacity.

In every stage of our design we used procedures and components that would be misers with power yet still provide long-term performance and reliability.

FACT. Microscience drives aren't limited to functioning only in the horizontal position.



With the growing use of portable computers and increasingly compact packaging, we designed our stepper motor and head carriage assembly to permit flexible placement of the disk drive.

Positioning that is best for you, not us.

FACT. Microscience engineers use only proven technology advances in an innovative manner to produce disk drives that perform reliably.

That's why we incorporated plated media, microprocessor-controlled spindle motors and servo-positioning, embedded guard bands, extensive self-diagnostics and optional signal processing.

Plated media will stand up to the rigors of portable computer usage.

Microprocessor-controlled servo-positioning keeps the heads precisely on track by reading servo information written in the gaps on both sides of each data track.

Microprocessors constantly monitor drive performance and report irregularities to the user. They make repeated checks during operation and test themselves during Power Up.

Media-embedded guard bands keep the carriage head from exceeding pre-determined limits and protect the drives against "wall crashes."

Microscience uses only standard, off-the-shelf mechanical and electronic components in our drives so we can meet your demands as your system sales grow.

And, every component is second-sourced to ensure tested and approved availability.

FACT. In addition to our 10 MB half-height Winchesters, we have several other major advances in development.

But we will not announce them until they have been thoroughly tested and proven in our manufacturing and test operations as well as in the field.

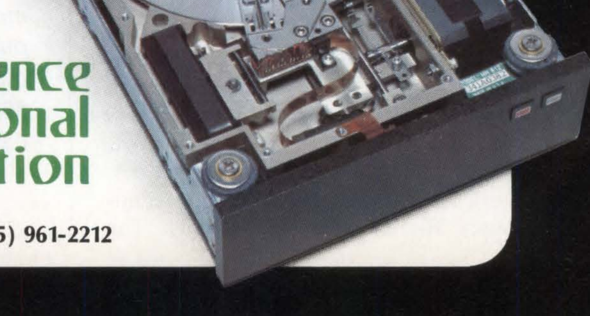
When we say they are available later this year, they *will be* available.

FACT. Microscience has one of the best, most responsive support teams of engineers available in the industry today.

We will not vie for your business on price alone.

We are concerned with providing a product that is reliable... a product that has extensive capabilities and expanded performance... a product we can deliver in volume... and a product we can produce for you at a fair price.

For more straight talk regarding your half-height Winchester needs, call or write us today.



Microscience International Corporation

575 E. Middlefield Road
Mountain View, CA 94043 (415) 961-2212

CIRCLE 192

Native mode Unix implementation

For midrange and high end VAX computers, Ultrix-32 operating system provides a pure Unix environment for technical applications. The software is an interactive, virtual memory, timesharing system supporting up to 16 users on 11/730s and 64 or more users on 11/780s. It features a hierarchical file system with demountable volumes for enhanced performance, shared I/O resources, and asynchronous process execution. Configured with a VAX, 2 Mbytes of memory, and the software, systems cost from $23,500 to $150,500. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.

Circle 331

Operating system kernel

The K286 gives designers a high level, easy-to-use interface for the architectural features of the iAPX 286. These features include multitasking, memory management and protection, and 1-Gbyte virtual memory. The modular kernel is available in source code form. It is designed for realtime industrial automation systems, communication systems, and workstations. It consists of 60 primitives, or subroutines, that access all iAPX 286 hardware functions. In source code format, the software sells for $27,000. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 332

Software development tool

Formix is a screen management system composed of a runtime executive to manage all data traffic between the user and the application program. It provides screen layout capability in which both the positioning and edit/validation criteria of all screen elements are defined interactively in "paint the screen" mode. The software's language interface enables application programs written in standard programming languages to load a defined screen form and call the executive. With support programs, application screens can be created, tested, modified, and accepted by the user, without a single line of application code. Single license price is $495. **Master Computer Systems, Inc,** 9531 W 78th St, Eden Prairie, MN 55344.

Circle 333

File server to network software

Software allows 64 PCs, XTs, and work-alikes to share 150 Mbytes of disk storage and three printers attached to a NetWare file server. NetWare/E implementation provides a network card for each personal computer connected to the server. Each user has a password for automatic access privileges to specified areas of shared disks. For maximum throughput, disk caching is used, as well as directory caching/hashing and elevator seeking. Software package is $1495. **Novell Inc,** 1170 N Industrial Park Dr, Orem, UT 84057.

Circle 334

Compiler in C for IBM 370

The C/370 permits C program development in the IBM mainframe environment. It also allows system houses and VAX users to move existing C and Unix applications to the 370 by simple recompiling and relinking. The standard package includes a Pascal-to-C translator. The compiler runs on all IBM 370, 43XX, 30XX, and plug-compatible mainframe systems under MVS, VS1, SVS, MVT, and MFT. Also includes is a system interface library for porting applications to, or developing new programs on 370 architecture. Price is $5000. **Whitesmiths, Ltd,** 97 Lowell Rd, Concord, MA 01742.

Circle 335

Unix for Q-bus-based systems

The 4.2 BSD version features a fast file system for throughput gains up to 10 times over older Unix versions. It supports DARPA standard TCP/IP communication protocols and high level application protocols such as FTP, Telnet, and SMTP. For existing users on the System III, an upgrade kit is available. The operating system has full and transparent demand paging and reduces system overhead. **Integrated Solutions, Inc,** 1350 Dell Ave, Campbell, CA 95008.

Circle 336

Cross assembler development

The MACXXX series cross assemblers enable any MS-DOS/PC-DOS system to serve as a development station for Motorola 6800/01/03/11, 6805, or 6809; Intel 8085; or MOS Technology 6502. These software systems feature a macro assembler, a cross-reference generator, a screen editor, a hexadecimal file converter, and offloading facilities. Assembler mnemonics adhere to assembly language defined by chip manufacturers. Macro assembler includes full macro and conditional assembly features and the ability to include a series of source files together during a single assembly. Programs must be offloaded to the target processor for test. Systems are $150 each. **Allen Ashley,** 395 Sierra Madre Villa, Pasadena, CA 91107.

Circle 337

Database management software

Family software for the System 8000 includes Informix DBMS, Ace custom report writer, and Perform screen generation packages. Informix helps build database applications on Unix systems. It includes an interactive query language, menu creation facility, data entry, and maintenance. Based on an indexed sequential access method, the software lets users work with an unlimited number of indexes, adding or deleting as needed. Perform allows users to create custom screen formats. The package is available for $1700. **Zilog, Inc,** 1315 Dell Ave, Campbell, CA 95008.

Circle 338

Relational DBMS on Unix

Available under Unix System V, DBMS is written in C for portability. Of its 2000 modules, only 30 need to be modified to move to almost any 16- or 32-bit operating system. The software bypasses a host operating system by implementing its own file management system. The separation of kernel from user interface is valuable for designing distributed systems or file servers. The system can split communicating systems so that the data base and kernel are resident on a central processor, and the interface and tools are resident on workstations. **Oracle Corp,** 2710 Sand Hill Rd, Menlo Park, CA 94025.

Circle 339

Cross-development environment

An integrated cross-development facility for the 68000 family runs on Prime 50 series computers. The C68, a cross compiler, is source level compatible with the Prime native mode C compiler. The A68 is a Motorola Exormacs-compatible M68000 cross assembler. L68 is a 68000 cross linker with library support. A 68000 simulator, S68 allows the contents of both memory and registers to be examined and changed from within the simulator. Breakpoint can be set and instruction mnemonics displayed. Packages range from $1500 to $5000. **Pacer Software, Inc,** 1227 Pearl St, La Jolla, CA 92037.

Circle 340

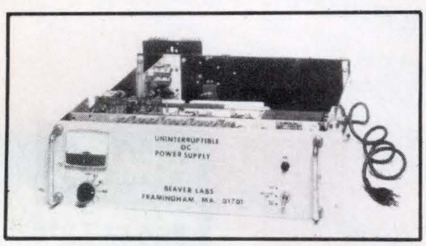
Lattice C compiler

With the VRTX C interface library, programmers using VRTX/86 realtime operating kernel can employ the Lattice C compiler to write realtime applications for 8086-based systems. VRTX is a software component used in micro-based systems that require fast reliable software. VRTX can be plugged in, without modification, to micros or single-board computers regardless of hardware configuration. The interface library comes on 5¼-in. diskettes with complete documentation for $750. **Hunter & Ready Inc,** 445 Sherman Ave, Palo Alto, CA 94306.

Circle 341

POWER SOURCES & PROTECTION

Uninterruptible power supply



The 100-W dc UPS generates a 5-Vdc ±1 percent, 20-A output for online system bus power. Fused access is available to the 24-Vdc zero maintenance battery system for powering a disk during power failure periods. A precision-regulated supply float charges the battery system and powers a high efficiency output switching regulator with a ±0.6-percent load regulation. A power-fail logic signal for CPU control and provisions for external UPS shutdown control are available. Price, in 100s, is $1129. **Beaver Electronic Laboratory,** PO Box 1290, Framingham, MA 01701.

Circle 342

Power sources for batteries

Miniature 5-W switching mode sources provide high I/O isolation, wide input voltage tolerance, high efficiency, and precision output regulation. Designated 5A7.17R5, -12, and -15, all three devices accept input voltages from 7 to 17 Vdc, and provide regulated outputs of 5, 12, and 15 Vdc. Remote shutdown circuitry allows the converter to be in standby mode drawing less than 5 mA input current, thereby lengthening battery life. Prices are in the $90 range. **Reliability Inc,** PO Box 218370, Houston, TX 77218.

Circle 343

Switching power supplies

Specifically designed for microprocessor applications, model SC1142 offers 62 W, while SC1143 offers 11-W triple outputs. The supplies feature dual inputs of 90 to 132/180 to 248 Vac at 47 to 63 Hz. The 12-V output on SC1142 has a continuous rating of 2 A and handles the surge current required for initial start up of two 5¼-in. floppy drives. The 12-V output of the SC1143 delivers 4 A continuously and provides the surge capacity for one 5¼-in. floppy and a 5¼-in. Winchester. Price for the 62-W version is $85 and the 100-W version is $95. **Sierracin/Power Systems,** 20500 Plummer St, Chatsworth, CA 91311.

Circle 344

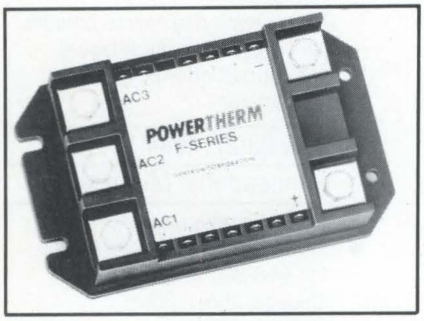
Open-frame switchers

Adaptable to applications in the 200-W range, the DP-200-R series offers preset voltages of ±5 V at 20 A, ±12 V at 4 A, ±5 V at 2 A, and ±24 V at 4 A. Another model allows user-specified voltages. The main output as well as outputs 4 and 5 have linear regulators that provide load regulation of ±2 percent, while loads of other outputs are semiregulated to within ±5 percent. Features include isolated returns on all outputs, remote sensing of cable losses up to 250 mV on main output, and TTL-compatible adjustable trigger-point. MTBF is 30,000 hours. **Datapower, Inc,** 3328 W First St, Santa Ana, CA 92703.

Circle 345

Power hybrid modules

The Six-Pak F-series is rated at 35 to 150 A up to 1400 V. Single- and three-phase rectifier and SCR bridges are available in three-phase, six SCR full converters, and triple ac switches. Suppressor, free-wheeling diode, and gate-to-cathode capacitor options are available. Applications include phase controls, motor controls, dc power supplies, and lighting. One thousand-piece prices begin at $25. **Gentron Corp,** 6667 N Sidney Pl, Milwaukee, WI 53209.



Circle 346

PERIPHERALS

Low cost printers

The 40-col Alphacom 42 is priced at $99.95 including interface cable, while the 80-col Alphacom 81 goes for $169.95 without cable. Both thermal printers link to most computers by plugging the appropriate interface cable into a cartridge-like slot. Interface cables for the 81 model cost $44.95. An RS-232/Centronics interface cable allows the printer to be used with most small computers. **Alphacom, Inc,** 2323 S Bascom Ave, Campbell, CA 95008.

Circle 347

Enhanced printer

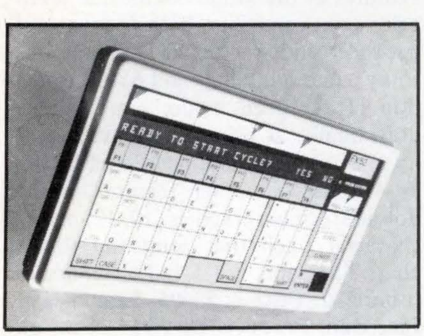
The 2700 II interfaces with IBM's systems network architecture (SNA). This distributed electronic printer offers improved capabilities for creating documents, and provides up to four times the memory and five times the internal font storage of the 2700. The printer communicates with the 2770, 2780, 3780, and 3274/3276, and 3770 networks using SDLC. Software includes a remote print management facility for the creation, storage, and printing of forms and charts. Another software package is a document composition facility. The printer can store up to 256 Kbytes. Price is $19,995. **Xerox Corp, Printing Systems Div,** 880 Apollo St, El Segundo, CA 90245.

Circle 348

Battery power counter

For high frequency applications, the LDC-831 provides up to 6½ digits of resolution. The five most significant digits are displayed using the 0.01-s gate time. By then switching to the 1-s gate, all 4 digits to the right of the decimal point are displayed. The combination of the two readings yields the 6½-digit resolution. The 150-MHz frequency counter has a basic accuracy of ±10 ppm and carries a two-year warranty. **Leader Instruments Corp,** 380 Oser Ave, Hauppauge, NY 11788. **Circle 349**

Panel-mounted terminal

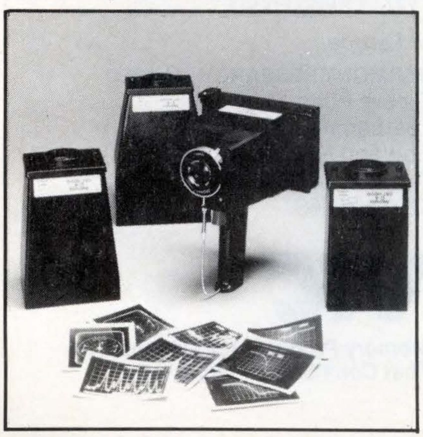


The FX/52 provides a 32-char LED with 56 tactile feedback membrane keys. Offering a keyboard customized to specific purposes, it has software-labeled function keys and four user-labeled function indicators. Terminal capabilities include baud rates up to 38.4k, even, odd, mark, or space parity. Serial ASCII interface is available with RS-232-C, RS-422-A, and 20-mA current loop conditioning. Up to 62 terminals can connect to one line in the polled mode. Other modes include block and conversational. **Termiflex Corp,** 18 Airport Rd, Nashua, NY 03063.

Circle 350

Camera for scope/CRT photography

The C4 documents CRT waveform displays and CRT information for analysis and record keeping. The handheld unit combines camera and CRT hood system, allowing a variety of screen sizes by changing hoods. Three CRT/scope hoods can take black and white or color pictures off various sized displays. The user need only set f/stop and shutter speed. Holding the pistol grip and squeezing the trigger produces the instant print. The camera and one hood are available for $370. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.



Circle 351

Industrial terminals

The 3092A industrial display terminal packages a full-sized CRT and all the functions of an office terminal into a sealed, steel enclosure. The 3093A graphics terminal adds graphic capabilities while the 3081A industrial workstation terminal is a compact version for factory data collection applications. Both CRT terminals feature a detached, sealed membrane keyboard. The terminals are protected against dust, dirt, grease, oil, and liquids, and can be cleaned off with a hose. Prices range from $1038 to $6040. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 352

Letter-quality printer

Offering 44-char/s printing rates, the TP 740 has a 96-char printwheel. On paper widths up to 15 in., it prints 132 characters at 10 chars/in., 158 characters at 12/in., and 197 characters at 15/in. With proportional spacing, it produces from 113 to 263 chars/line. The device has a bidirectional carriage and uses Silver Reed/Diablo printwheel and Diablo HyType II cartridge ribbons. Centronics parallel interface is available as well as RS-232-C, Qume, and IEEE 488. **Televideo Systems Inc,** 1170 Morse Ave, Sunnyvale, CA 94086. **Circle 353**

Second-generation color printer

The TIP-302 provides 75 to 300 lines/min and three printing qualities: compressed, data processing, and letter. It uses a 9 x 7 matrix character and offers both 13.3 and 16.6 chars/in. Applications include CAD/CAM, mapping, scientific research, and color graphics. A dual-printhead provides reliability because one part will continue to print at half-speed if the other is disabled. Price is $6900. **Trilog Inc,** 17391 Murphy Ave, Irvine, CA 92714. **Circle 354**

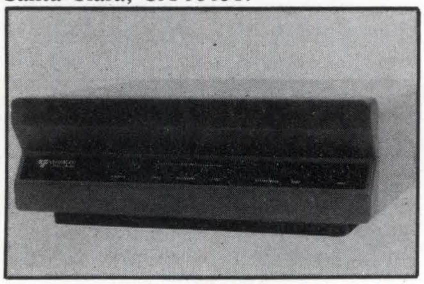
Joystick with RS-232 ASCII output

Turbo stick offers high pointing speed and high resolution (1 part in 4096). Handle uses two fingertip-operated microswitches for switching between an absolute mode (high pointing speed) and rate mode (high resolution). The switches can be redefined under software control to perform different functions. Applications are in graphics and instrumentation systems. The joystick is priced at $395. **KA Design Group,** 6300 Telegraph Ave, Oakland, CA 94069.

Circle 355

Disk-based plotting systems

A random element processor and IBM online plotting controller are available with an optional 40- to 140-Mbyte, 5¼-in. Winchester. The disk options enable plotting systems to handle longer more complex plots in color or black and white with less CPU overhead. Acting as a raster data buffer, the disk spools the raster image for a high speed transfer to the plotter. The disk option adds $13,500 to the price of the random element processor or IBM plotting controller. It costs an additional $1500 for infield upgrades to existing systems. **Versatec, a Xerox Co,** 2710 Walsh Ave, Santa Clara, CA 95051.



Circle 356

Terminal with DEC/TEK features

The CIT-467 allows simultaneous use of DEC alphanumeric software commands, Tektronix 4027A color graphics command structure, and 4010/4014 emulation mode. The color graphics terminal provides rectangle, polygon, circle, arc, and pie command functions, and is compatible with 4027A graphics primitives. Other features include full dot addressability, user-programmable scale factor, and relocatable origin. Standard interfaces are EIA RS-232-C and 20 mA current loop, as well as full- and half-duplex operation. Price is $2995. **CIE Terminals, Inc,** 2505 McCabe Way, Irvine, CA 92714.

Circle 357

Dot-matrix printer

Features of the Model 530 include seven-color print capability, both friction-feed, cut-sheet and tractor-feed, continuous-form paper handling, and 55-dB operation. Three print modes are available: draft quality at 180 chars/s; memo quality at 90 chars/s; and near-letter quality at 45 chars/s. Other features include dot-addressable graphics, 10, 12, or 16.5 character pitch that prints up to 224 chars/line, and a 1.5 billion character printhead. Price is $2495. **Lear Siegler, Inc, Data Products Div,** 714 N Brookhurst St, Anaheim, CA 92803.

Circle 358

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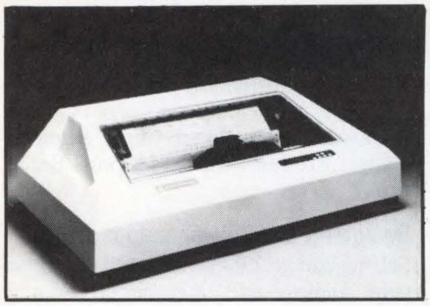
The editors invite you to write technical articles for Computer Design. For a free copy of our Author's Guide, circle ***503*** *on the Reader Inquiry Card.*

CIRCLE 183

High speed printers



The B series provides printing speeds from 180 to 250 chars/s at 10 to 16.7 chars/in., respectively. The printers provide a parallel interface with optional RS-232-C. Front-panel switches control top of form, form feed, and online functions. For graphics, resolutions range from 60 x 72 to 144 x 144. Model DP-9725B is a color version with modes for one-pass data processing, one-pass enhanced, one-pass condensed, and two-pass correspondence. Prices range from $1200 to $1625. **Anadex, Inc,** 1001 Flynn Rd, Camarillo, CA 93010.

Circle 359

Keyboard printer terminal

Designed for use with APL, the AJ 864A dot-matrix printer terminal sustains printing speeds of 180 chars/s. It comes with an APL character set and keyboard with full overstrike and underscore capability. The entire keyboard is programmable so frequently used keys can be conveniently placed. Seven function keys can be programmed with multikey sequences of up to 31 characters. A 16-Kbyte extended buffer memory is standard. Price is $3250. **Anderson Jacobson,** 521 Charcot Ave, San Jose, CA 95131.

Circle 360

Color display for graphics system

Designed for the PS 300 family, the color calligraphic display offers dynamic lines and characters without jagged lines associated with raster displays. The unit allows a PS 300 family member to present complex high resolution three-dimensional line drawings in a programmable selection of over 1800 colors. It is the same size and uses the same cabinetry as the PS 300 dynamic 19-in. monochromatic calligraphic display and the static color raster display. Price is $22,000. **Evans & Sutherland,** PO Box 8700, 580 Arapeen Dr, Salt Lake City, UT 84108.

Circle 361

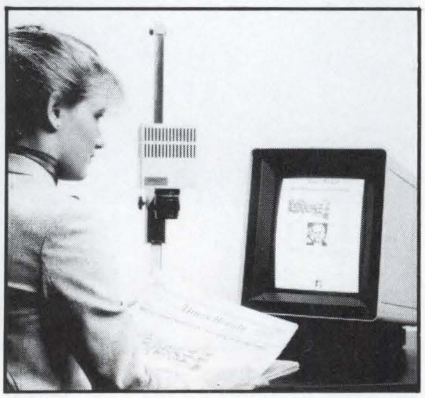
Dual-speed thermal printer

The TP-X prints 100 chars/s, or 50 chars/s for high print quality. The 24-element print head has 180-dot/in. resolution. The printer accepts 10-in. wide, 100-ft paper roll that cuts sheet to any length, and prints to an 8-in. width. Font density adjusts for various printout needs. It uses either a thermal transfer on plain paper or thermal dot print on thermal sensitive paper. Thermal ribbon has a 155,000-character life. **Ricoh of America Inc,** 20 Gloria Ln, Fairfield, NJ 07006.

Circle 362

Bit-mapped display

The high resolution 200-dot/in. model 500 displays a full page (including pictures, drawings, 3-D objects, or 38,400 readable characters) onscreen. Applications include document storage and retrieval, CAD, graphic digitization, and laser printer page makeup. The display has 23 address lines with 1.6-μs read/write access times. The monitor provides 1728 x 2200 viewable points, a 15-in. diagonal screen size, and 60-Hz refresh. Model 500 is $17,950. **Datacopy Corp,** 1070 E Meadow Circle, Palo Alto, CA 94303.

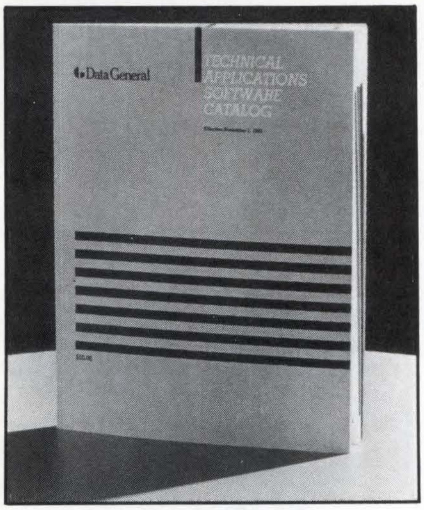


Circle 363

Drafting plotters

The 7586B handles both cut-sheet and roll media. It can draw frame to frame long axis plots up to a length of three frames or 12 ft by plotting a series of 48-in. back to back plot segments. A built-in optical sensor enables the plotter to align segments for a continuous plot. It offers 21 character sets, an 18-Kbyte partitioned buffer, polygon area-fill instructions, downloadable character sets, and block-mode data transfer with the RS-232-C interface. Price is $21,900. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 364**

Technical software



Catalog features about 300 scientific and technical application packages running on Eclipse MV family computers; CAD/CAM/CAE programs developed by third-party suppliers (part of the company's independent software vendor program) are also described. **Data General Corp,** Westboro, Mass. **Circle 410**

Robot position sensors

Six-page application note reviews potentiometers, incremental and absolute optical encoders, and conventional and brushless resolvers; text examines multiplexed, type II tracking loop, and absolute two-speed approaches for converting resolver-based position information into digital data. **ILC Data Device Corp,** Bohemia, NY. **Circle 411**

Lasers, optics, and fiber optics

The 500-page, 19th-edition *Laser Focus Buyers' Guide* includes tutorials that cover the basics in areas such as gas semiconductor and solid state lasers, laser systems, and fiber optics; the product directory covers related entries sequentially within 20 distinct sections, while the vendor directory lists over 1300 manufacturers, consultants, institutions, and professional societies. Address orders ($35 postpaid) to: **Laser Focus Buyers' Guide,** PO Box 1111, Littleton, MA 01460.

Power protection

Four-page leaflet reviews performance and design specs for line of uninterruptible power systems and conditioning equipment. **Solidstate Controls, Inc,** Columbus, Ohio. **Circle 412**

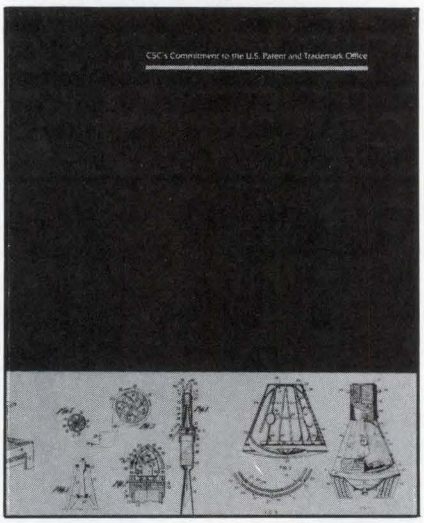
Semiconductor power products

The 1983/1984 digest examines MOSFETs, Schottky and silicon rectifiers, diode bridges, and protective devices; also detailed is the IRel reliability program, which has chalked up over six million device hours of Hexfet tests to keep outgoing defect rate under 200 ppm. **International Rectifier Corp,** El Segundo, Calif. **Circle 413**

Data bookshelf

Comprehensive products guide for 1984 describes eight-volume reference set encompassing handbooks on memory components, microcontrollers, telecommunication products, microsystems, military, development systems, OEM systems, and company or company-designated third-party software. **Intel Corp,** Santa Clara, Calif. **Circle 414**

Automated patent system



Brochure introduces design team that proposes to automate the U.S. Patent and Trademark Office; players and specialties include Derwent for foreign patent data base, Integrated Automation for image storage and retrieval, Mead Data Central for online full-text search, and Computer Sciences Corp for system integration. **Computer Sciences Corp,** Falls Church, Va. **Circle 415**

Factory automation

Catalog features 30 titles drawn from books, special reports, conference proceedings, and reference documents on subjects such as industrial robots, flexible manufacturing systems, computer vision, and automated assembly. **Tech Tran Corp, The Manufacturing Technology Bookstore,** Naperville, Ill. **Circle 416**

Semiconductor data

Technical information covers company's complete semiconductor product line. **Rockwell International Corp, Semiconductor Products Div,** Newport Beach, Calif. **Circle 417**

Designing CMOS semicustom arrays

Self-teaching, 286-page manual of precision analog and A-D circuits details TMG6000 series, covering instrumentation, sensor subsystems, switched capacitor, data acquisition, and signal processing applications. **Telmos Inc,** Sunnyvale, Calif. **Circle 418**

Modular system DMMs

Ten-page brochure specifies performance of remote-programming 8505A and 8506A units, describing 12 plug-in modules that tailor each DMM to a specific application. **John Fluke Manufacturing Co, Inc,** Everett, Wash. **Circle 419**

Relays

A 64-page catalog gives dimensional drawings and specs for sealed, enclosed, open, and power relays; sockets; magnets; solid state devices; and steppers. **Guardian Electric Manufacturing Co,** Chicago, Ill. **Circle 420**

Adjustable-speed ac drives

Ten-page technical data book lists operational features, options, drive protection, and design characteristics of 1- to 50-hp Power Plus line. **Borg-Warner Electronics Corp, Power Electronics,** Ithaca, NY. **Circle 421**

Intelligent memory module

Illustrated data sheet examines model 45C92, a compact, nonvolatile memory duplication and storage device with 2-K x 8 EEROM for offline security. **Reliance Electric Co,** Stone Mountain, Ga. **Circle 422**

Shaft angle encoder

Data sheet lists technical and design information for MicroSeries model 17/23, which provides up to 17 bits of resolution in a compact package. **Itek Measurement Systems Div, Litton Industries,** Newton, Mass. **Circle 423**

Oscillographic recorder

Product brochure and spec sheet summarize performance and features of microprocessor-based 3410 thermal pen recorder. **Soltec Corp,** Sun Valley, Calif. **Circle 424**

Ultraviolet erasing equipment

Twelve-page catalog highlights Spectroline EPROM erasing equipment handling from 9 to 336 chips; ultrahigh intensity grid lamps, digital ultraviolet radiometers, and protective gear are also described. **Spectronics Corp,** Westbury, NY. **Circle 425**

Step-motor driver ICs

Application note summarizes basic performance of various IC drivers in terms of available power, giving motor-drive torque and speed data. **Oriental Motor USA Corp,** Torrance, Calif.
Circle 426

Analog I/O for microcomputers

Catalog gives 192 pages of technical specs and application information for data acquisition products ranging from solid state signal conditioning to analog and digital I/O systems for LSI-11 and PDP-11, Multibus, STD bus, IBM PC, and Apple II series computers. **Data Translation,** Marlboro, Mass. **Circle 427**

Schematic design station

Brochure profiles features, specs, and operation of Dash-1 workstation/IBM PC in eight pages; structured interactive design system, hierarchical CAE package, and low cost pen plotter are also described. **FutureNet Corp,** Canoga Park, Calif. **Circle 428**

Data communication equipment

Illustrated short-form catalog and price list detail intelligent product line comprising local networking, voice/data multiplexers, data concentrators, data PBXs, modems, multiplexers, miniature local data sets, and protocol converter. **Micom Systems, Inc,** Chatsworth, Calif.
Circle 429

Solid state relays

Catalog organizes engineering and performance specs for CMOS- and TTL-compatible board and panel mount units; dimensional drawings and ordering information accompany text. **Grayhill, Inc,** La Grange, Ill.
Circle 430

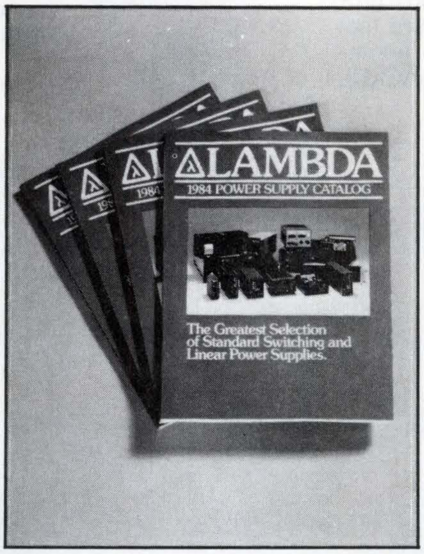
Cooling equipment

Sixteen-page selection and ordering guide presents tube axial fans, variable-speed blowers, and cooling accessories. **AMCO Engineering Co,** Arlington Heights, Ill.
Circle 431

Filtering emi

Combination in-stock catalog and cross-reference guide presents AeroFilter line, then explains applications, specs, and performance characteristics for a range of standard emi filters. **RTE/Aerovox, Inc,** New Bedford, Mass.
Circle 432

Power supplies



Catalog has 144 pages of detailed specs, outline drawings, and prices for all current supplies, systems, and accessories. **Lambda Electronics, div of Veeco Instruments Inc,** Melville, NY.
Circle 433

Miniature dc servos

Four-page bulletin covers Elcom brushless motors; accompanying 10-page technical paper discusses brushless motor performance and drive electronics. **The Pittman Corp,** Harleysville, Pa.
Circle 434

Hardware/software emulator

Role of 9508S universal integration station in designing and debugging 8-bit systems is analyzed in eight-page leaflet; specs and special command features follow text. **Gould Inc, Design & Test Systems Div,** Santa Clara, Calif.
Circle 435

Lighted push buttons

Twenty-page booklet features common specs, construction materials, LED and incandescent lamp choices, filters, diffusers, optional accessories, and standard mounting hardware. **NKK Switches of America Inc,** Scottsdale, Ariz.
Circle 436

Data conversion

Twelve-page brochure examines line of synchro, resolver, and Inductosyn to digital converters with 10- to 16-bit resolutions; performance specs and applications section discusses product range from three-chip hybrid to three-channel Multibus compatible board for multi-axis control. **Analog Devices,** Norwood, Mass. **Circle 437**

Floating point applications

A 30-page booklet and two application notes focus on the 32-bit floating point WTL 1032 multiplier and WTL 1033 ALU; FFT processor booklet describes floating point chip set use in digital signal processing, four-page note outlines a subsystem that interfaces to a high performance bit-slice processor, and 12-page note summarizes floating point division and square root operations, as well as ROM lookup, accuracy considerations, and IEEE compatibility. **Weitek Corp,** Sunnyvale, Calif.
Circle 438

Printed circuits

Guide features line of products and services in six pages; flowchart that summarizes process cycles for producing PC boards is also included. **LeaRonal, Inc,** Freeport, NY.
Circle 439

Custom analog to digital

Twelve-page booklet summarizes performance of combined amplifier/multiplexer/analog-digital systems to determine channel configuration, speed, and accuracy; diagrams and interface data complement text on custom data conversion systems. **Preston Scientific,** Anaheim, Calif. **Circle 440**

"TELEX reduced solder bridging 60% and saved $100,000 by specifying VACREL® dry film solder mask."

"We're TELEX Terminal Communications, one of the largest manufacturers of plug compatible peripheral equipment in the world.

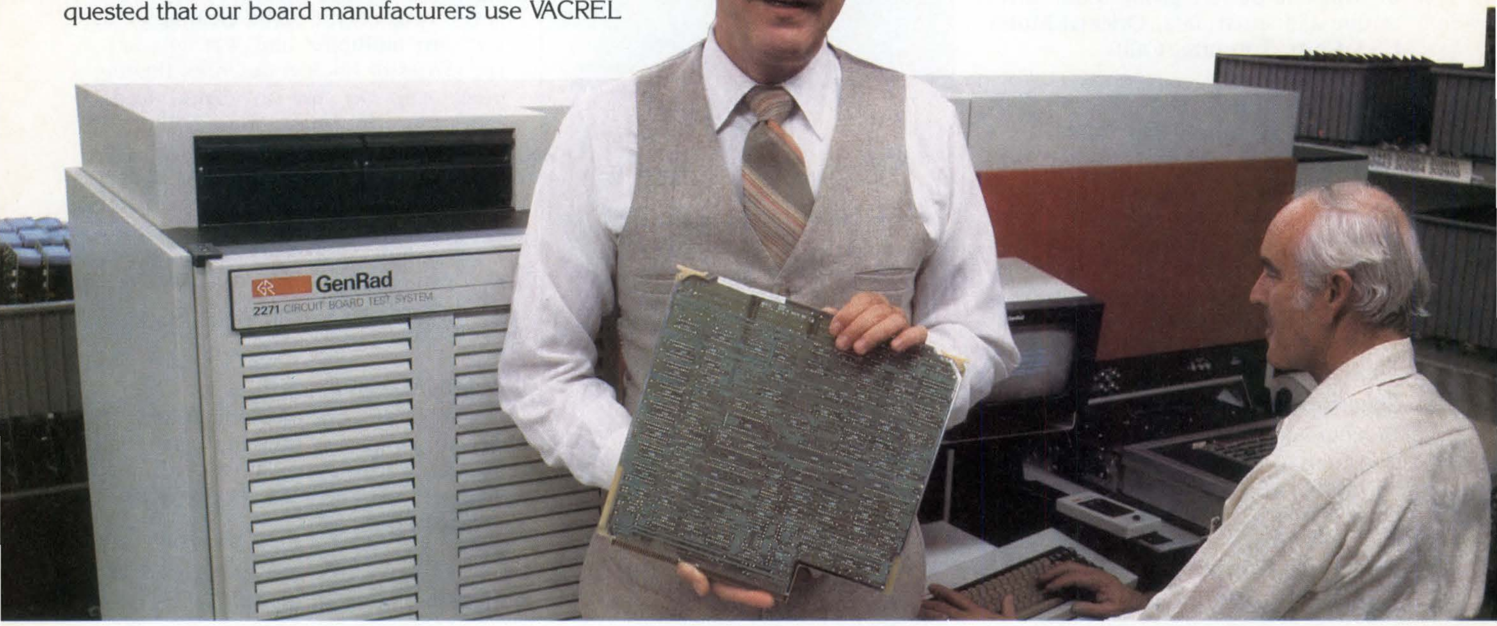
At TELEX, today's electronics industry's requirement for higher-density wiring in printed circuit boards posed quite a challenge for the screen printed solder masks we had been using. Boards with tight lines and spaces were requiring rework at an increasing rate due to shorts caused by solder bridging.

Our screened solder mask simply didn't provide the protection and resolution capabilities that are needed to prevent solder bridging. So we requested that our board manufacturers use VACREL dry film solder mask from Du Pont.

As a result of switching to VACREL dry film solder mask, our productivity increased and we saved over $100,000 in a year. Our PWB assembly has never been more profitable.

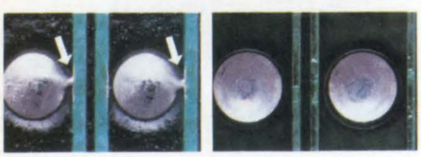
That's why we now specify VACREL dry film solder mask for all our high-density PWB's."

Douglas J. Blackley
Director, Product Assurance
TELEX Terminal Communications
Raleigh, North Carolina



Unlike screen printed inks, VACREL dry film solder mask is photo imaged which provides excellent resolution for high-density PWB designs with up to three traces between IC pads.

The film is uniformly thick, which means no low points on pad edges to permit solder overflow and costly solder bridging. It is vacuum laminated to the board, so your most delicate circuit lines are protected by total encapsulation.



VACREL solder mask (right) reduces the occurrence of solder bridging on high-density PWB's that often occurs with the screen printed process (left).

The changeover to the VACREL solder mask process from the screen printing process can lead to increased assembly productivity, efficiency and profitability. To find out for yourself, ask your board manufacturer for circuit boards with VACREL dry film solder mask.

Find out more about how you can increase your PWB profitability with systems, services and innovative technology from Du Pont. Send for the brochure that details the benefits and advantages of protecting your printed wiring boards with VACREL dry film solder mask. Write Du Pont Company, VACREL Dry Film Solder Masks, RISTON® Products Division, Room N-2526, Wilmington, DE 19898.

Lower assembly costs by keeping solder in its place.

An electronics company.

DU PONT
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CIRCLE 191

CONFERENCES

APR 29-MAY 4—Internat'l Society for Optical Engineering Technical Symposium, Hyatt Regency Crystal City Hotel, Arlington, Va. INFORMATION: SPIE East '84, PO Box 10, Bellingham, WA 98227. Tel: 206/676-3290

MAY 7-8—Micro Wars: Shape Up or Shake Out, Mark Hopkins Hotel, San Francisco, Calif. INFORMATION: Laura Greenfield, Internat'l Data Corp, 5 Speen St, Framingham, MA 01701. Tel: 617/872-8200

MAY 8-10—CAM-I Internat'l Computer Integrated Manufacturing Seminar, Montreux, Switzerland. INFORMATION: Rhonda Gerganess, CAM-I, Inc, 611 Ryan Plaza Dr, Suite 1107, Arlington, TX 76011. Tel: 817/860-1654

MAY 13-17—Computer Graphics, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: National Computer Graphics Assoc, 8401 Arlington Blvd, Fairfax, VA 22031. Tel: 703/698-9600

MAY 14-17—Internat'l Conf on Communications, Congresscentrum Rai, Amsterdam, The Netherlands. INFORMATION: K. Teer, Philips Research Lab, 5600 MD Eindhoven, The Netherlands.

MAY 14-17—Internat'l Conf on Distributed Computing Systems, Hotel Meridien, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAY 15-17—Electro, Bayside Exposition Ctr and Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 15-17—Mini/Micro-Northeast, Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 22-25—Comdex/Spring, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

MAY 23-24—Trends and Applications 1984: Making Data Base Work, National Bureau of Standards, Gaithersburg, Md. INFORMATION: Vincente Galindo, Sperry Corp, 12010 Sunrise Valley Dr, Reston, VA 22091. Tel: 703/620-7189

JUNE 4-7—Robots 8 Conf and Expo, Cobo Hall, Detroit, Mich. INFORMATION: Patricia Van Doren, Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-1500

JUNE 4-8—SID (Society for Information Display Internat'l Symposium), San Francisco Hilton, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

JUNE 5-7—Internat'l Symposium on Computer Architecture, Rackham Building, Ann Arbor, Mich. INFORMATION: Keki Irani, ECE Dept, Univ of Michigan, Ann Arbor, MI 48109. Tel: 313/764-8517

JUNE 5-7—Symposium on Mass Storage Systems, Marriott Mark Resort, Vail, Colo. INFORMATION: Bernard O'Lear, NCAR, PO Box 3000, Boulder, CO 80307. Tel: 303/494-5151

JUNE 6-8—American Control Conf, Hyatt Islandia, San Diego, Calif. INFORMATION: Herb Rauch, Lockheed 52-56/205, Palo Alto Research Lab, 3251 Hanover St, Palo Alto, CA 94304. Tel: 415/493-4411 X5677

JUNE 6-8—Communications Architectures and Protocols, Montreal, Canada. INFORMATION: Rebecca Hutchings, Honeywell/FSD, 7900 Westpark Dr, McLean, VA 22102. Tel: 703/827-3982

JUNE 19-22—Internat'l Symposium on Fault Tolerant Computing, Hyatt Orlando, Orlando, Fla. INFORMATION: Richard Sedmak, Sperry Univac, PO Box 500, MS C1SW12, Blue Bell, PA 19404. Tel: 215/542-3638

JUNE 20-22—Internat'l Conf on Computers and Applications, Fragrant Hill Hotel, Beijing (Peking), China. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JUNE 21-22—VLSI Multilevel Interconnection (V-MIC) Conf, Hotel Intercontinental, New Orleans, La. INFORMATION: Thomas Wade, Microelectronics Research Lab, Electrical Engineering Dept, PO Drawer EE, Mississippi State, MS 39762. Tel: 601/325-3721

JUNE 24-27—Design Automation Conf, Albuquerque Convention Ctr, Albuquerque, NM. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 9-12—NCC (National Computer Conf), Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 23-25—Computer Simulation Conf, Copley Plaza Hotel, Boston, Mass. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 800/225-7654

JULY 23-27—SIGGRAPH Conf on Computer Graphics and Interactive Techniques, Minneapolis, Minn. INFORMATION: Lynn Valastyan, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

JULY 30-AUG 2—Internat'l Pattern Recognition Conf, Montreal, Canada. INFORMATION: ICPR Secretariat, 3450 University St, Montreal, Quebec, Canada H3A 2A7. Tel: 514/392-6744

AUG 2-6—Autofact Japan Conf and Expo (held conjointly with **Mechatronics**), Osaka, Japan. INFORMATION: Leslie Hossack, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0023

SHORT COURSES

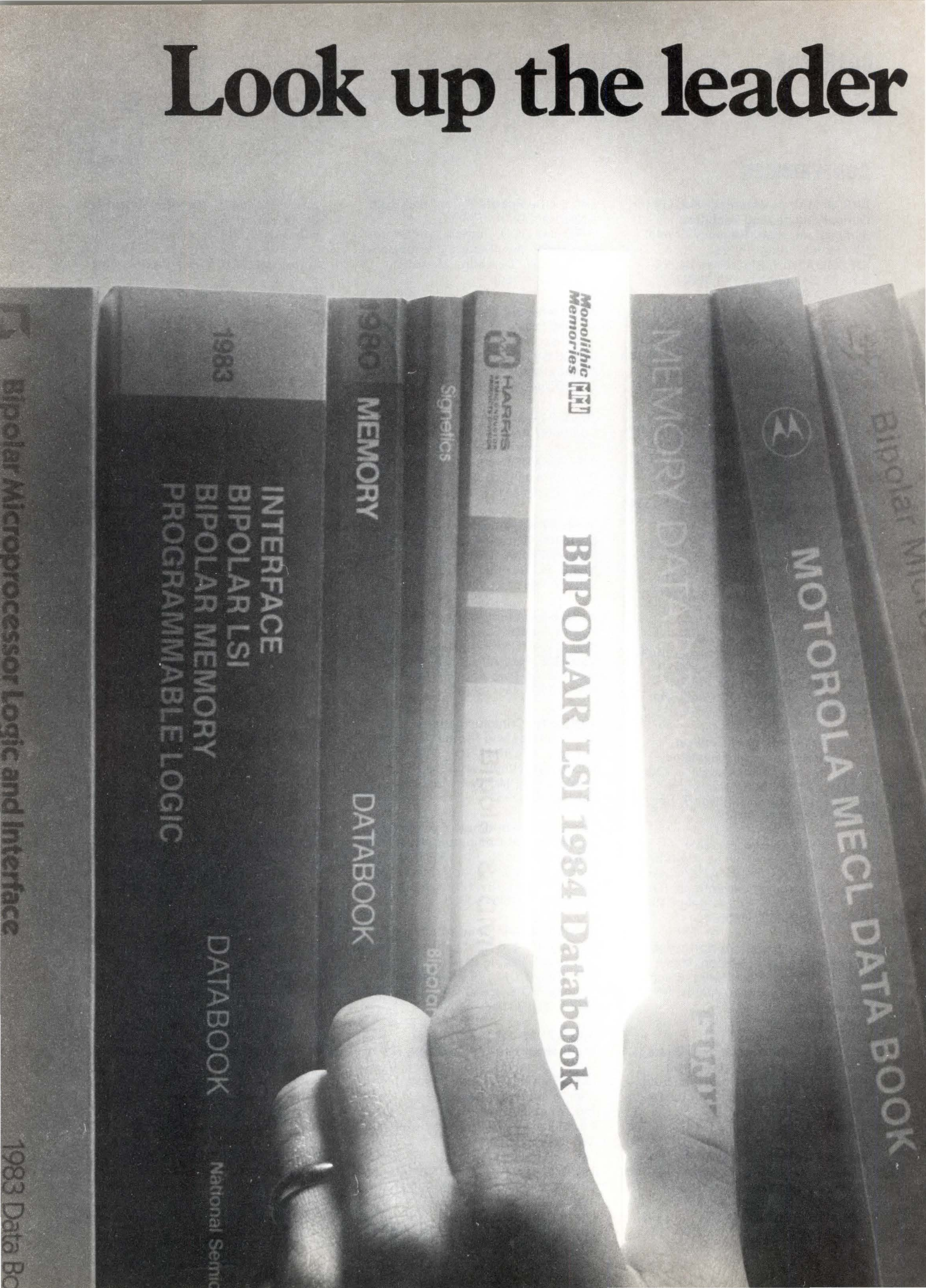
APR-MAY—Implementing Voice Technology, various cities and dates. INFORMATION: Votan, 4487 Technology Dr, Fremont, CA 94538. Tel: 415/490-7600

APR-MAY—Local Area Networks: Equipment and Systems, various cities and dates. INFORMATION: Architecture Technology Corp, PO Box 24344, Minneapolis, MN 55424. Tel: 612/935-2035

MAY 9-11—Advanced Signal Processing, Pacifica Hotel, Culver City, Calif. INFORMATION: Donald Rauch, Evolving Technology Institute, 3725 Talbot St, Suite F, San Diego, CA 92106. Tel: 619/224-3788

MAY 10—VLSI Packaging, Marriott Hotel, Minneapolis, Minn. INFORMATION: Integrated Circuit Engineering Corp, Seminar Coordinator, 15022 N 75th St, Scottsdale, AZ 85260. Tel: 602/998-9780

MAY 14-17—Software Engineering with Ada, Hilton at Logan Airport, Boston, Mass. INFORMATION: U.S. Professional Development Institute, Dept A B, 1620 Elton Rd, Silver Spring, MD 20903. Tel: 301/445-4400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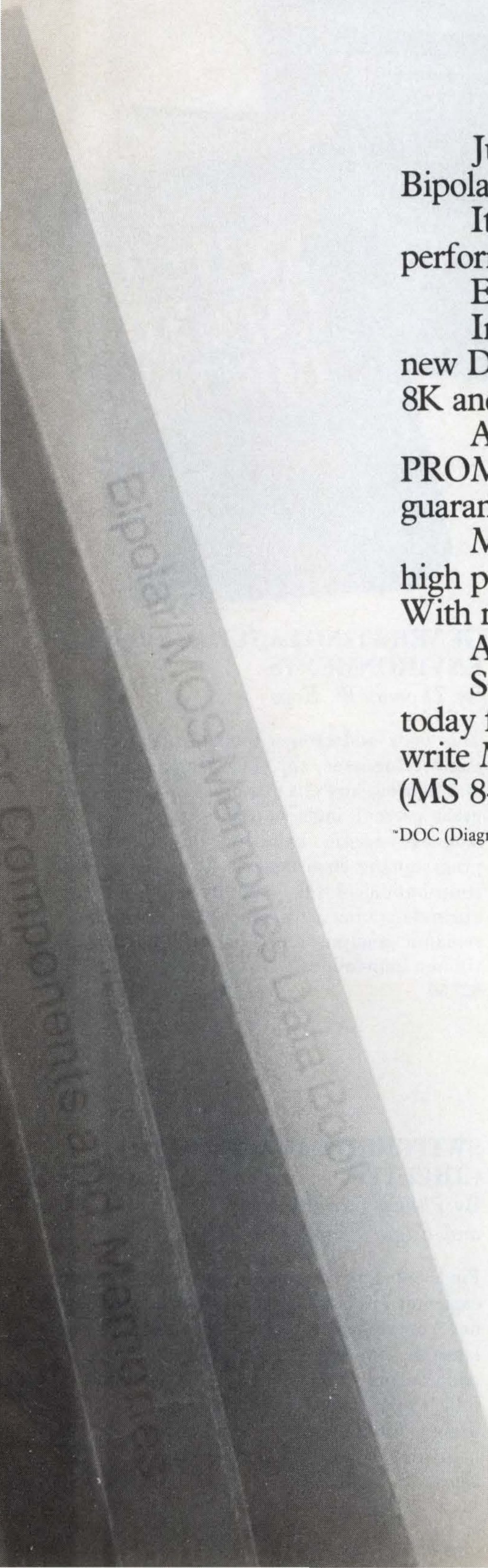

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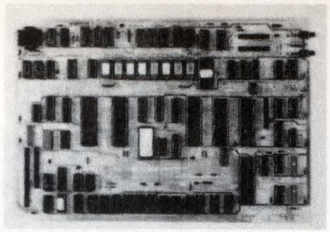

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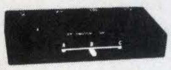

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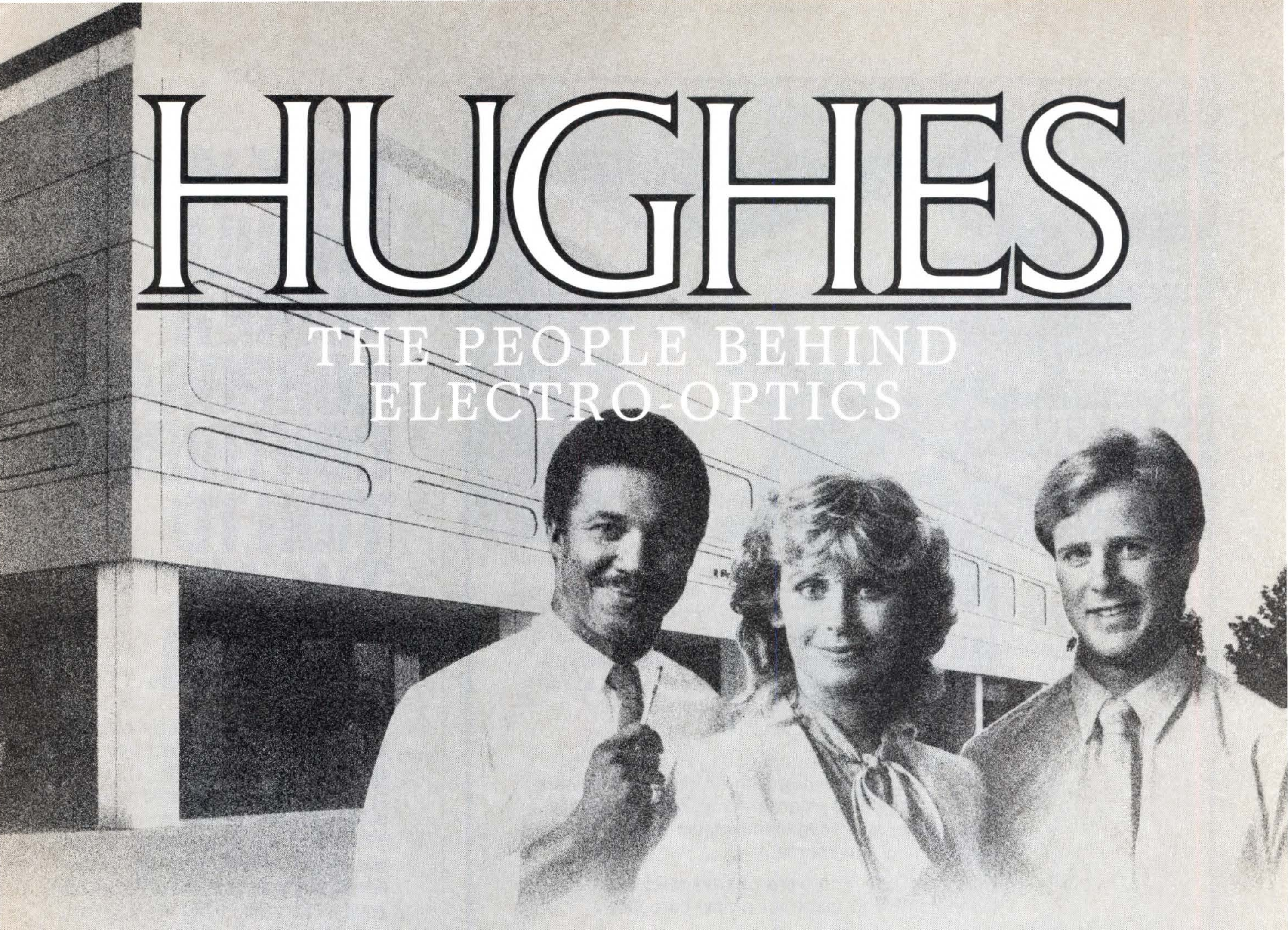

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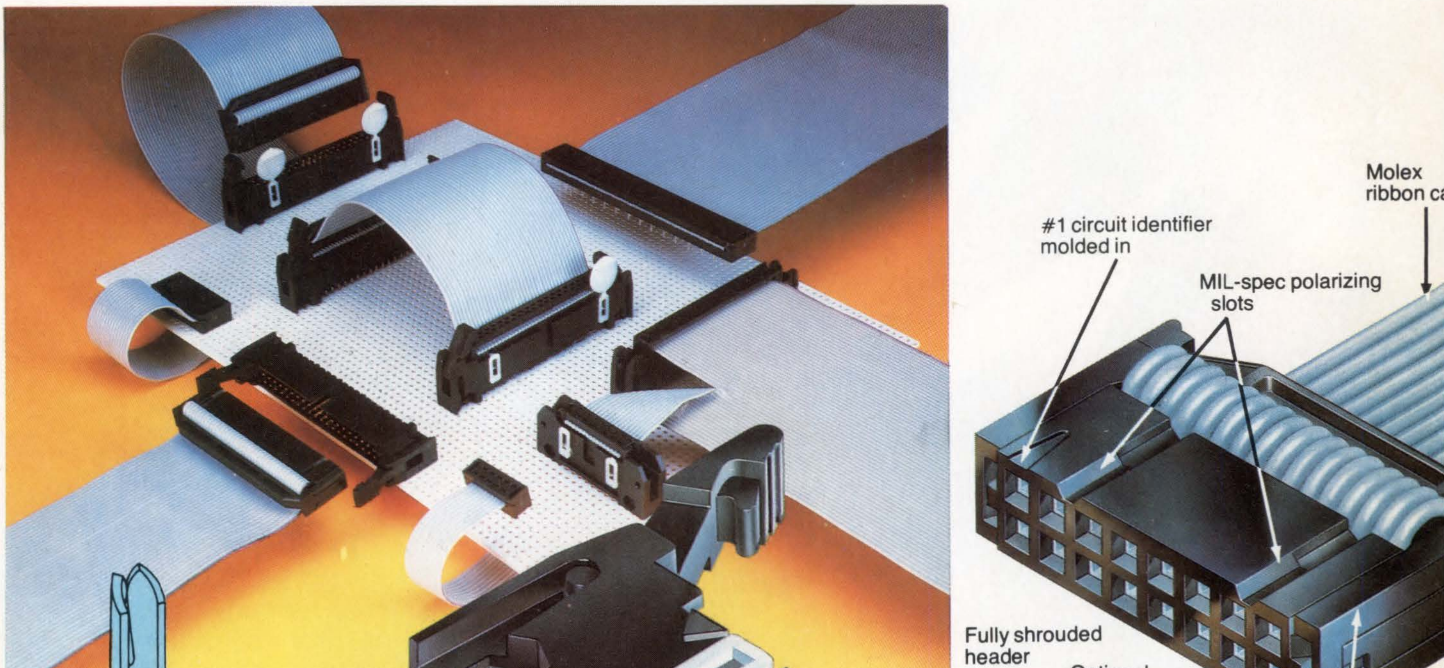

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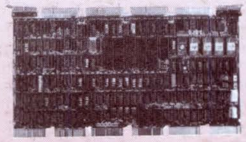

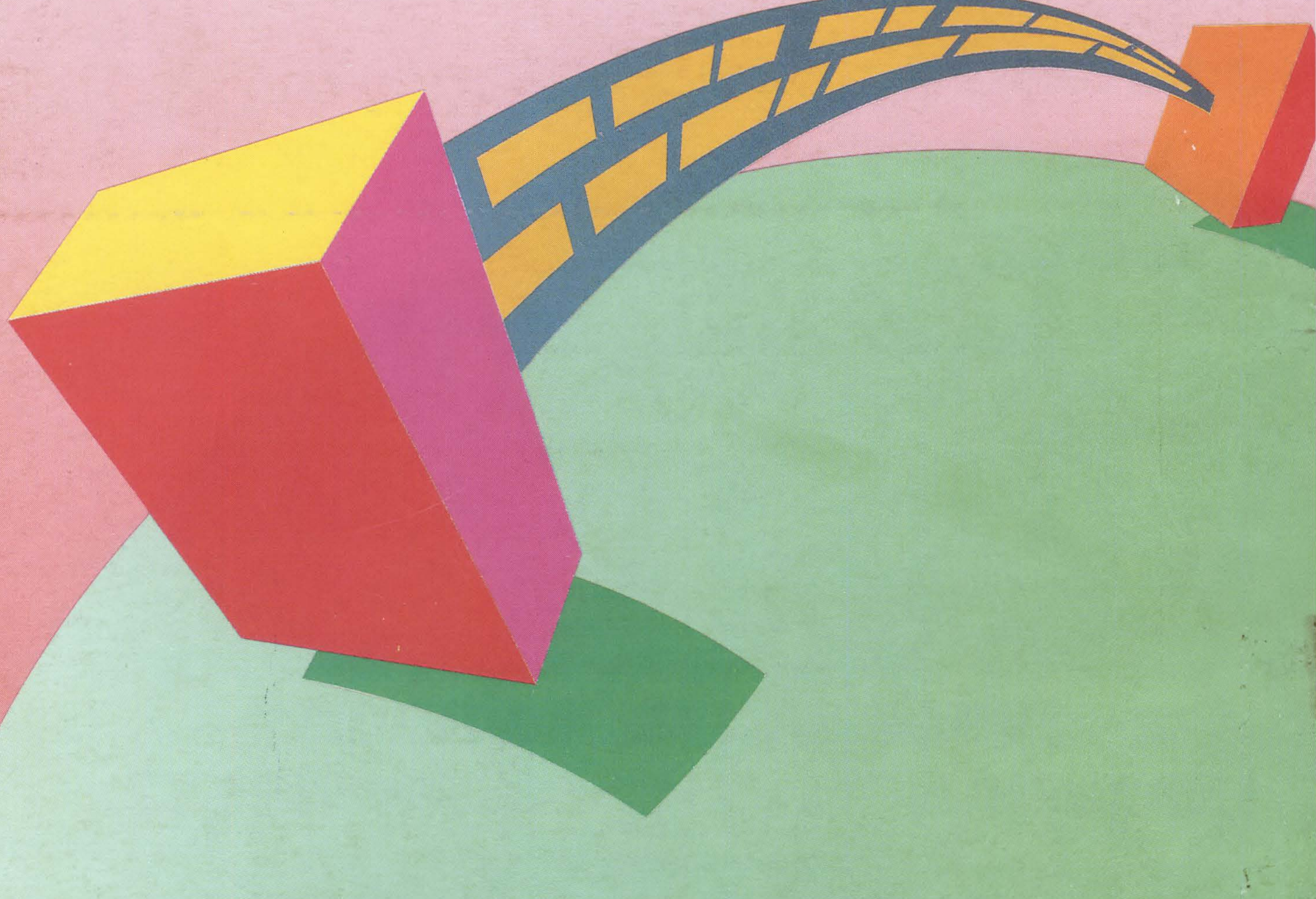

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