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COMPUTER DESIGN®

AUGUST 15, 1988

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION

Designers' Buying Guide to Single-Board Computers

Fast GaAs and silicon BiCMOS parts rekindle designers' interest in ECL

Prototype testers put ASIC characterization into designers' hands

2,400-bit/s modem ICs add functionality, preserve design flexibility

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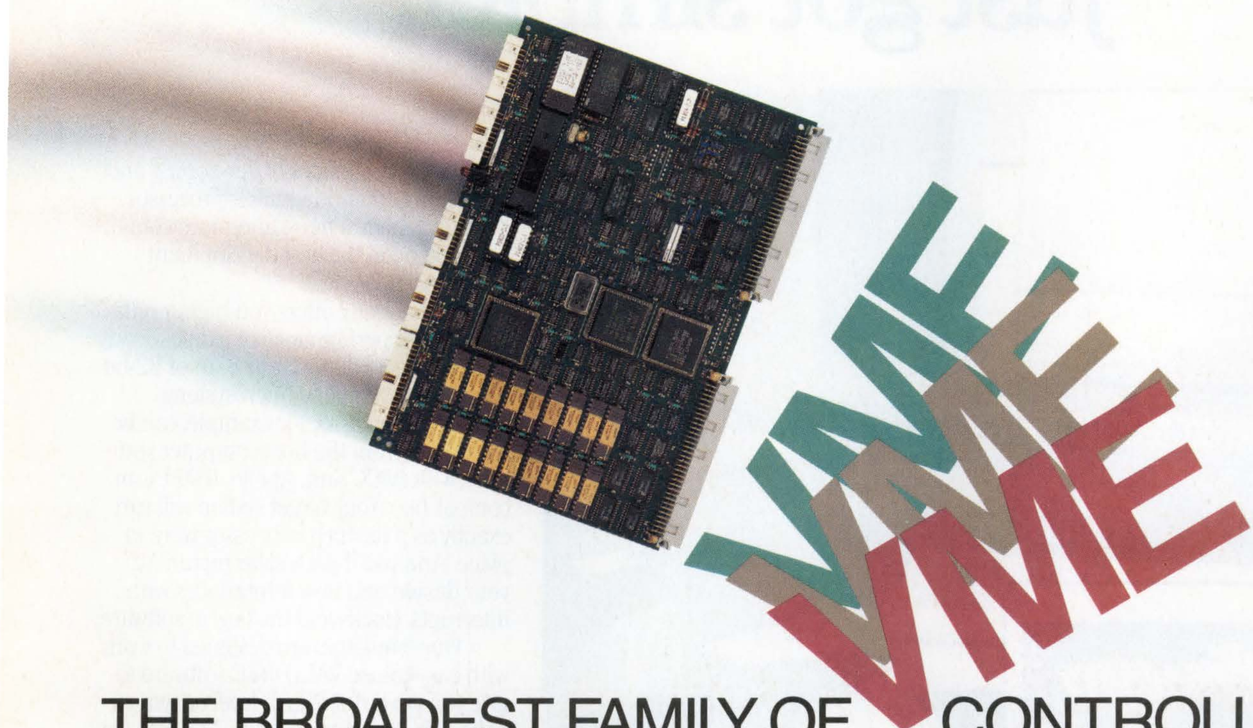

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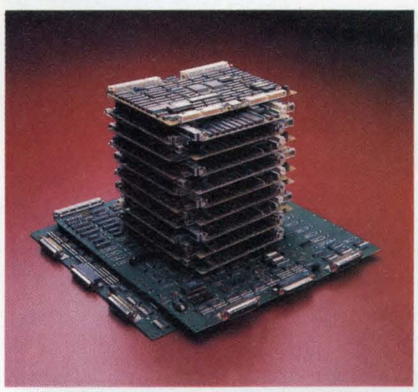

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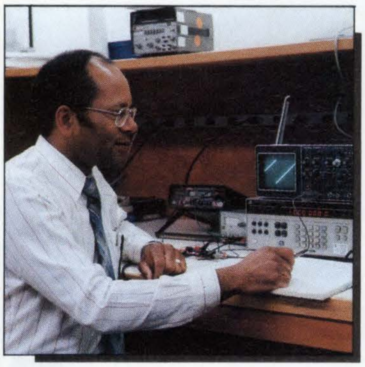

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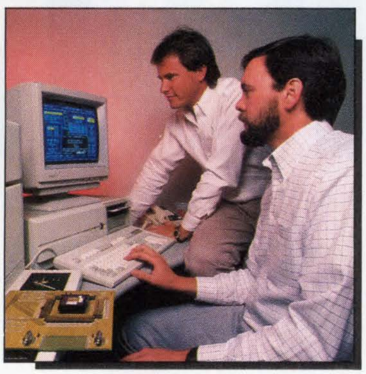
■ TECHNOLOGY UPDATES



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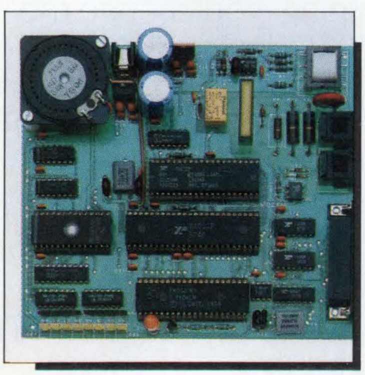

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■ NEW PRODUCT HIGHLIGHTS

■ DEPARTMENTS/COLUMNS

How the fa

Our new 7.5ns PAL® device is fast enough to prove that standard logic shouldn't set the standard anymore.

It's also fast enough to finally let today's new microprocessors run at the speeds for which they were designed—breathtaking.

Raising your standard.

How fast would you like your standard logic?

How about faster than any TTL logic around? Even FAST™ or AS? You've got it with the 7.5ns PAL device.

And the fact that you can configure it yourself means you can get exactly what you want.

If you want to redesign something, you change the PAL device. Not the board.

Not only is this the fastest way to get high speed logic, it's also the most practical. One 7.5ns PAL device replaces two to six standard TTL devices.

Which cuts down on board size.

And cuts down chances for a device failure.

7.5ns PAL Device vs. FAST & AS

SSI/MSI		FAST	AS	7.5ns PAL Device
Combinatorial				
74138 Decoder	tPD	8.0	10.0	7.5
74151 Mux	tPD	11.0	15.0	7.5
Register/Latch				
74374 Octal Register	tCO	10.0	9.0	6.5
74373	tPD	8.0	6.0	7.5
Octal Latch	tLEO	13.0	11.5	7.5
Counters				
74161	tS	5.5	8.0	7.0
Four bit Ctr	tCO	11.0	13.5	6.5
74269/869	tS	2.5	5.0	7.0
Eight bit Ctr	tCO	10.0	11.0	6.5

st get faster.

What to give the microprocessor that has everything.

We suggest the first PAL device that can keep up with it.

The 7.5ns PAL device runs at 74 Mhz. It can deliver the speed the new high performance microprocessors need.

Processors like the 29K, the 386 and the 68030.

This PAL device delivers 25% more speed than any other PAL device.

We even have the fastest 22V10.

Our 15ns 22V10 runs at 50Mhz. That's 10ns faster than anyone else on the market. And it lets you run at twice the rate of the new 25Mhz microprocessors.

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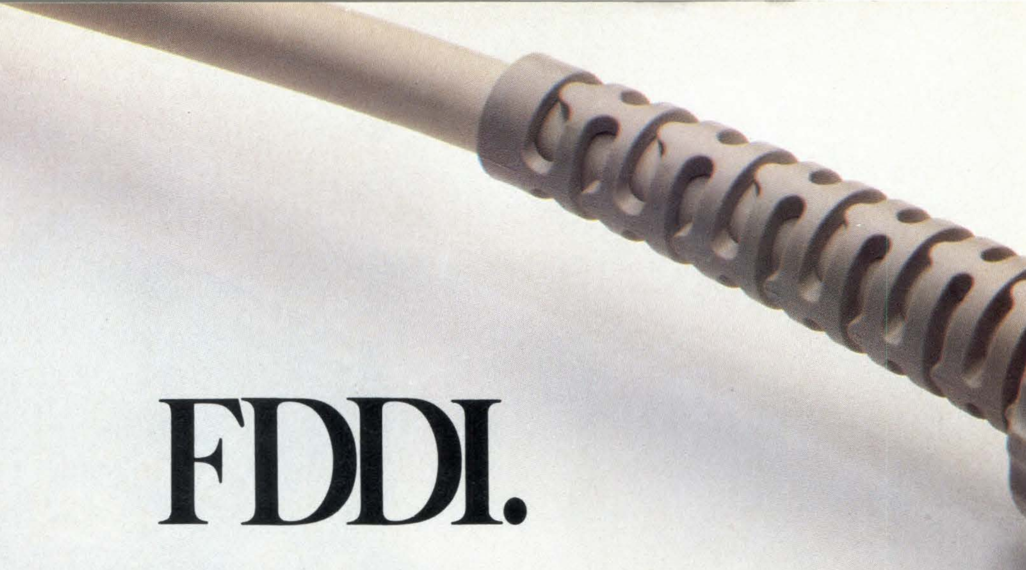
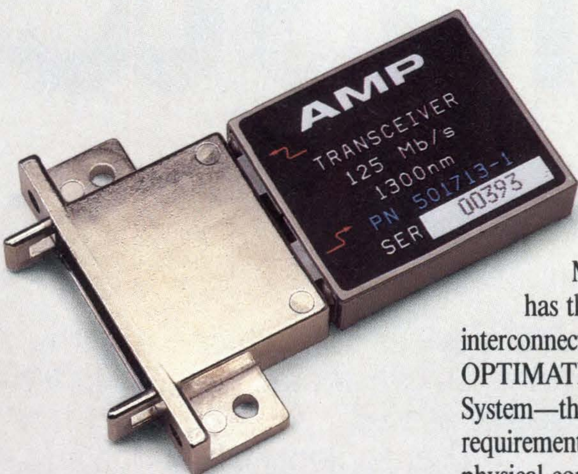


FDDI.
From deskwork to network.

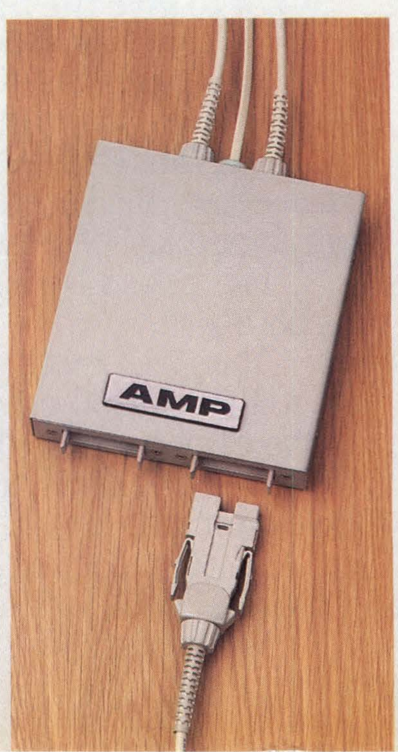


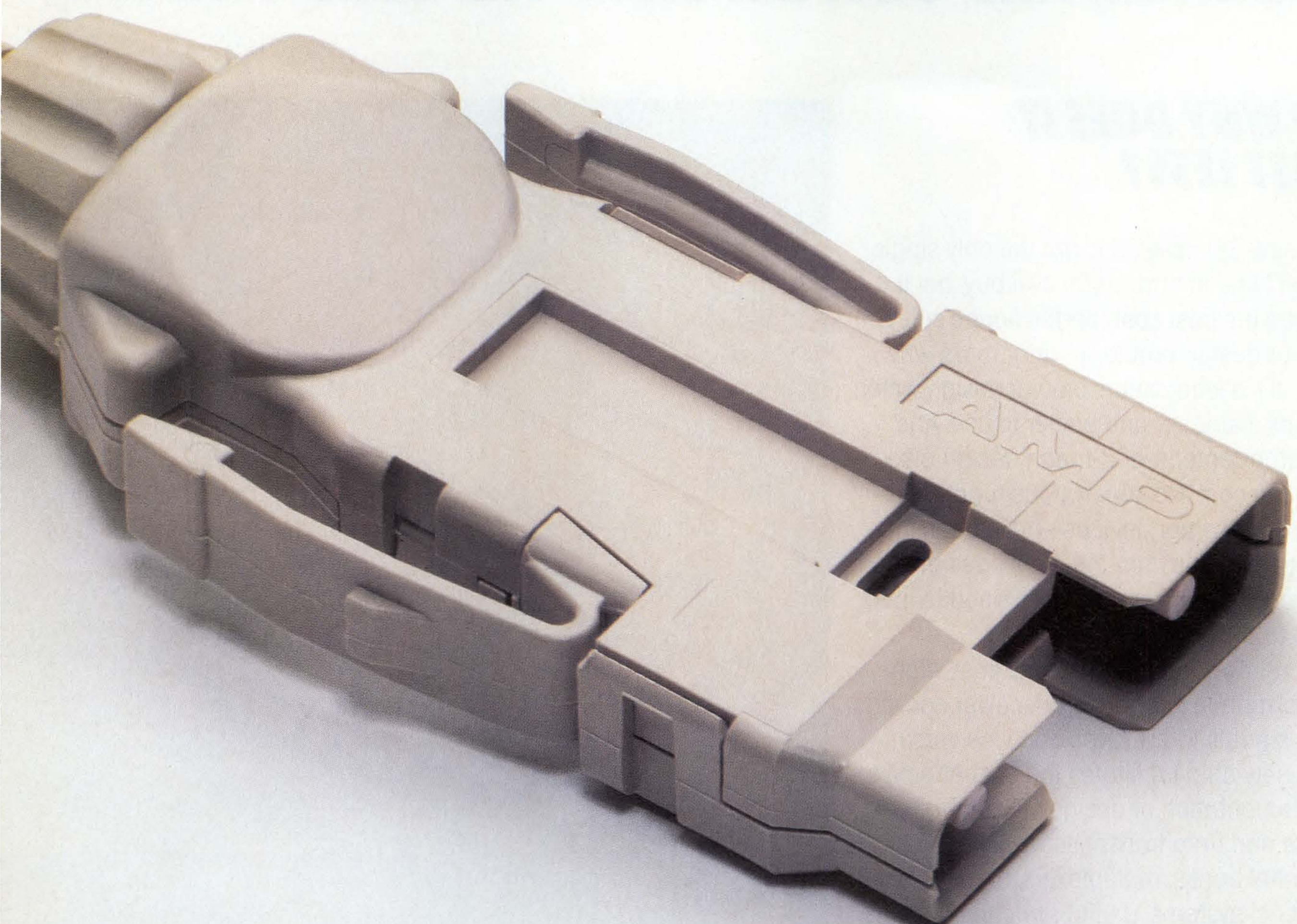
Good news for networks!

The X3T9.5 Task Group, under the procedures of ANSI Accredited Standards Committee X3, has reaffirmed approval of the Media Interface Connector (MIC) for the proposed FDDI (Fiber Distributed Data Interface) Physical Layer Medium Dependent (PMD) document.

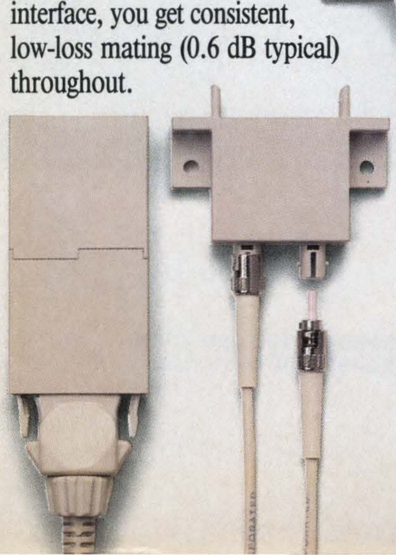
More good news! AMP has the complete fiber optic interconnection system—the AMP OPTIMATE Fixed Shroud Duplex System—that meets all FDDI PMD requirements. And includes all the physical components you need to make your fiber optic network a reality.

Of special note: the transceiver—the first of its kind—is capable of operating at data rates up to 125 Mb/s. Available in standard or raised (+5v) ECL logic, it gives you a compact, board-mount data link in a single 24-pin module. Reliable duplex mating and electro-optic conversion are now easier than ever.





All system components, in fact, are easy to install and reconfigure. Our field termination kit makes short work of attaching duplex connectors to fiber cable. And because all interconnections use a floating interface, you get consistent, low-loss mating (0.6 dB typical) throughout.



You can also order complete, custom-built cable assemblies from us. Either way, you'll have the assured compatibility that comes from dealing with only one supplier for all your FDDI interconnection components. A supplier whose capability in fiber optic technology is everything you'd expect from the world's largest connector company.

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AMP Interconnecting ideas

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It's a lean, mean, bipolar design which makes it smaller and easier to use. And our smarter lean-and-mean design also cuts the cost. No superfluous functions—best left to other devices—have been integrated into this chip. Yet it provides all the transceiver performance you need to interface to a T1 line.

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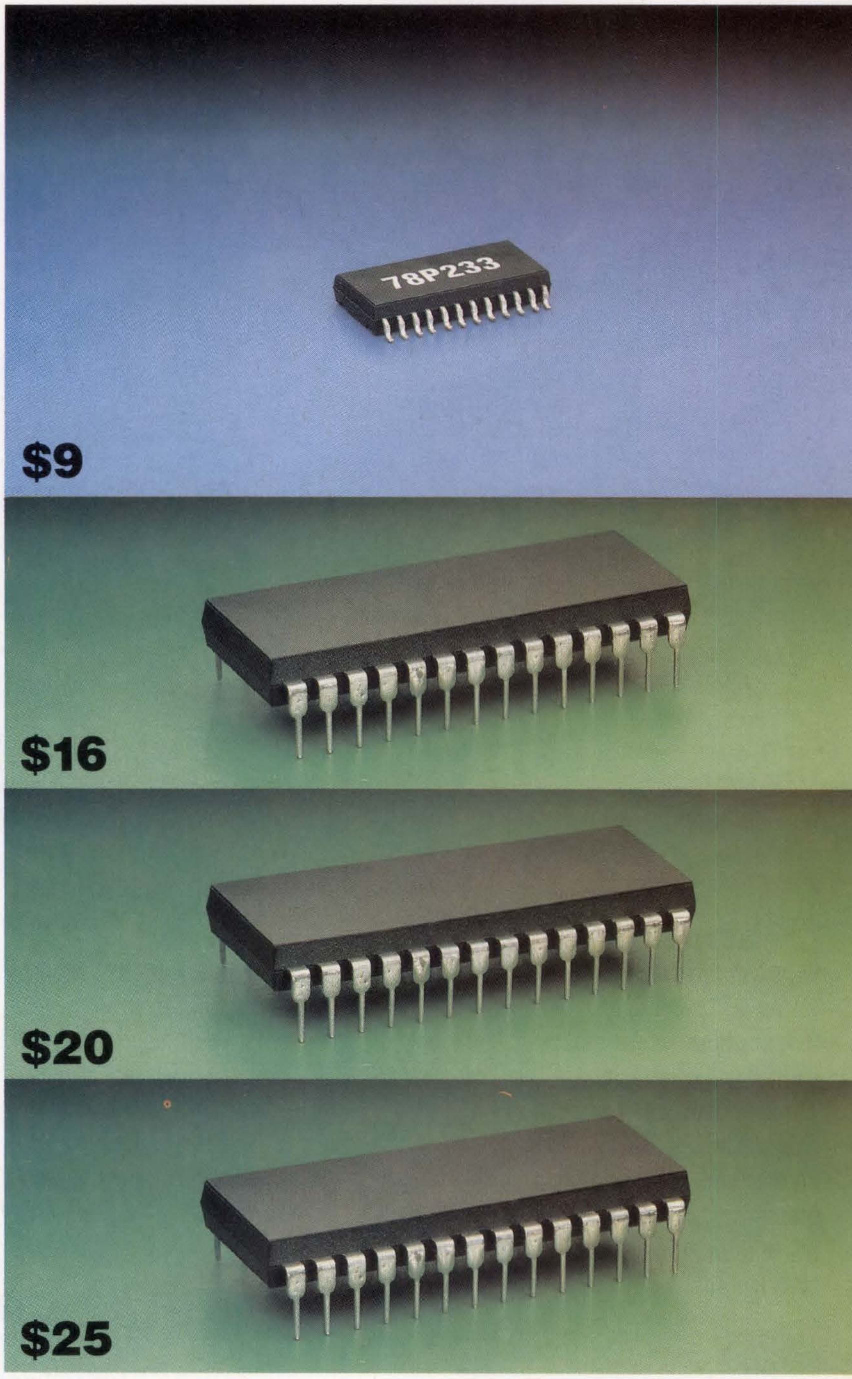

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3½-in. "floptical" drive packs 25 Mbytes

Optical servo tracks engraved in the oxide media of a standard, high-density 3½-in. floppy disk let a specially designed head mechanism read and write data at 1,250 tracks/in. for a capacity of 25 Mbytes (unformatted). The Floptical drive from Insite Peripherals (Santa Clara, CA) will use media initially supplied by Kodak and Xidex. The two companies will etch the servo tracks in their media with equipment developed and supplied by Insite.

The optical servo tracks are cut to a width of 4 microns with a laser. In between, magnetic tracks 15 microns wide are used to record sector formatting information and data. An infrared light-emitting diode shines on the optical tracks. A four-element photodetector is used to align head position to compensate for thermal variations in the media, to seek across tracks and to perform track following. Insite president James Adkisson predicts capacities of up to 100 Mbytes once barium ferrite vertical recording media becomes available.—*Tom Williams*

R.I.P. SMD

System designers have long been predicting that sooner or later the SMD disk drive interface, stretched to a 24-Mbit/s serial data transfer rate in recent years, would eventually run out of steam. It would be replaced, it was predicted, by the 16-bit parallel IPI-2 interface, which has an initial maximum transfer rate of up to 10 Mbytes/s and a slew of other advantages over the old SMD. The transfer rate of first-generation IPI-2 drives, however, generally hasn't exceeded 3 Mbytes/s—offering little motivation for system developers to offer the up-front investment needed to make the changeover.

Nevertheless, IPI-2 drives that can pass data at about a 6-Mbyte/s rate are on the way, offering a perceived advantage for those systems that have had their performance hindered by a disk I/O bottleneck. Before the end of the year, expect to see the announcement of several IPI-2 controller boards for the popular open-architecture buses, with the VMEbus being the most probable first beneficiary of the higher-performance interface.
—David Lieberman

The RISC race is on

At last, reduced-instruction-set-based single-board computers for industry-standard buses are starting to emerge from the labs into the real world. Many single-board computer manufacturers have spent considerable resources over the last year or so determining whether the time has come to move to a high-performance RISC micro and, if so, to which one.

It should start to become apparent by year's end which RISC chips will gain a significant number of design wins, which innovative design strategies have been developed to efficiently implement a RISC architecture within the confines of a single board, and whether existing bus architectures are up to the job.
—David Lieberman

Open Software Foundation and AT&T/Sun group may be communicating

Unconfirmed reports claim that the two separate consortia working to develop Unix standards, the AT&T/Sun Microsystems group and the Open Software Foundation (OSF), may be talking to each other. Many observers have viewed the announcement of the joint effort by AT&T (New York, NY) and Sun Microsystems (Mountain View, CA) as an attempt by the two companies to close the Unix environment to outside participation. Similarly, observers have viewed the creation of OSF as a challenge to this effort by major computer companies, including IBM and Digital Equipment Corp. Now, the reports of talks between the two groups have raised hopes that separate and incompatible open environments can be avoided.
—Ron Wilson

IBM joins X/Open Unix standards consortium

In an unusual show of support for a not-invented-here standard, IBM has joined the X/Open consortium. The move implies that IBM will contribute resources to the development of X/Open's Common Applications Environment specification, and then will introduce products that comply with the specification. IBM's move, following commitments from such pivotal vendors as Fujitsu, NCR and Sun Microsystems, virtually assures the X/Open interface spec of a permanent role in the evolution of Unix-based software.

The X/Open specification covers five areas of the interface between an application program and its operating environment: languages, operating system, data management, networking and user interface. IBM's announcement suggests that the company's AIX version of Unix will move into compliance with the IEEE Posix specification included in the operating system segment of X/Open's environment spec.—*Ron Wilson*

First RISC processor appears on VMEbus

Ironics (Ithaca, NY) and Advanced Micro Devices (Sunnyvale, CA) have announced development of a VMEbus CPU board based on AMD's 29000 reduced-instruction-set computer processor, apparently the first announcement of a RISC CPU board for the VMEbus. The board, which Ironics claims has about five times the computing power of the company's own 68020 boards, includes caches, interleaved on-board memory and a high-speed daughter card interface to exploit the latent speed of the 29000 processor.

If the introduction is any indication, it appears that RISC processors will enter the board-level computer market as expensive, high-powered and self-contained compute nodes, suitable for taming large, performance-critical tasks or for collecting a number of smaller tasks onto a single, cost-efficient engine.—*Ron Wilson*

Compiler brings real-time Ada to 80386 board

With the introduction of its DACS-80X86 Ada compiler system, DDC-I (Phoenix, AZ) has liberated real-time Ada from the confines of defense-oriented CPU environments. The software runs on Force Computer's 80386 VME board and can deliver performance equal to that of other real-time operating systems. Since code size is minimal (from 1 to 20 kbytes), applications can be put into ROM for use in embedded systems. The compiler features hard-deadline scheduling (HDS), which prioritizes processes based on importance as well as task duration. Under HDS, long-duration, high-priority tasks are prevented from locking out lower priority, short-term tasks, ensuring higher processor utilization.—*Mike Donlin*

Prime bows out of minisupercomputer market

Intense competition has forced Prime Computer (Natick, MA) out of the minisupercomputer arena. Prime's entry into the market for the small special-purpose system was actually a product of Cydrome (Milpitas, CA). A strategic partnership between the two, which included OEM and software development agreements, was announced last year. Designed for scientists and engineers who perform heavy numerical calculations, the 320-Mbyte MXCL5 was unveiled by Prime last January with speed specifications of up to 10.4 MFlops. However, price wars within the minisupercomputer marketplace forced discounting of up to 60 percent. Customers and prospects for the system are being referred to Cydrome, which will continue to sell and support the machine under its own name, the Cydra 5.—*Mike Donlin*

Multibus II is flying high

The selection of a 32-bit bus architecture for computers aboard the future U.S. space station has been made by IBM's Systems Integration Division (Houston, TX)—and it's going to be Multibus II. It's been a more-or-less lethargic year or so for the bus, which has found use in a flight simulator here and a few computer systems there. The visibility that this high-flying application will lend to the bus may be just what's needed to get OEMs thinking about the benefits of a synchronous message-passing bus that enjoys high-level software standardization.

According to Steve Cooper, manager of the architecture proliferation group at Intel's OEM modules operation (Hillsboro, OR), however, next year will bring more big news for Multibus II. "In the second or third quarter of 1989, about a half-dozen minicomputer manufacturers will announce that they're making the bold move to off-the-shelf microprocessors, industry-standard operating systems and open architecture buses," predicts Cooper. Although the minimakers' chips of choice will vary, a near-unanimous nod will be granted to Unix and to Multibus II, Cooper claims.—*David Lieberman*

MS-DOS breaks the 32-Mbyte file barrier with version 4.0 release

Partitioning large hard disks into 32-Mbyte or smaller files should become a thing of the past with the release of MS-DOS version 4.0 by Microsoft (Redmond, WA). The new DOS version allows disk volumes as large as the drive if needed. Microsoft also built in support for the expanded memory specification (EMS 4.0) that allows applications, memory-resident programs and operating environments such as Windows to use memory above the 640-kbyte DOS limit.

Also announced by Microsoft is a file-directory management system that includes pull-down menus and gives the user a visual (although not a high-resolution graphics) way to oversee and organize files. Microsoft will be distributing MS-DOS 4.0 only through hardware manufacturers.—*Tom Williams*

Universal PS/2 chip set adapts to 80286 or 80386

In an effort to simplify the design process of PS/2 clones, G-2, an affiliate of LSI Logic (Milpitas, CA), and Groupe Bull (Paris, France) are offering an IBM-compatible set of seven gate arrays and a BIOS. G-2 provided the BIOS, while the chip set was developed by Bull Micrel of America (Roseville, MN), a Groupe Bull subsidiary. Unlike competitive chip sets, which are compatible with one specific processor, the new offering gives clone makers the first set of circuits capable of functioning with all three Intel microprocessors: the 80286, the 80386 and the 80386SX. To compensate for the differing timing requirements of systems based on the 80286 and 80386, Bull integrated control pins and logic that let the set operate in any of several modes. G-2 claims the BIOS is also compatible with all three Intel processors and is self-scaling to match processor speed and type.—*John Mayer*

Single-chip autodial modem has tight analog-digital marriage

Modem IC manufacturers continue to demonstrate a progressive ability to integrate analog and digital functions on a single chip. The latest development is that of the first autodial single-chip frequency shift key (FSK) modem by Advanced Micro Devices (Sunnyvale, CA). Designers can build an intelligent autodial, autoanswer FSK modem using the chip under the control of a host microprocessor and supported by a data-access arrangement circuit.

Operating at 300 bits/s full duplex or 1,200 bits/s half duplex, the chip's digital signal processing architecture eliminates the need for an external dialer chip by adding a dual-tone multifrequency (DTMF) generator on-chip. External filters are avoided with the integration of a call progress tone detection function. Designers can also forget about using external hybrid op-amp circuits because the modem's analog interface has an internal hybrid for four-to-two wire conversion.—*John Mayer*

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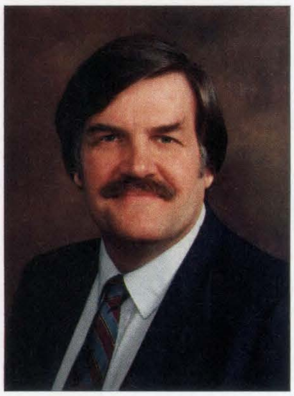
CIRCLE NO. 9

Will R&D soon mean retreat and defeat?

"What counts is how adequately you support the best and the brightest that you have."



John C. Miklosz
Associate Publisher/ Editor-in-Chief

The presidential campaign is now in full swing, and Michael Dukakis is drawing analogies between his campaign and that of John Kennedy, nearly three decades earlier. One of Kennedy's themes back then was that America had the "best and the brightest" and could accomplish anything it set out to do. That belief was supported—one might even say confirmed—by a manned moon landing less than 10 years later. While there's no doubt that it took some of the "best and the brightest" to put a man on the moon, it's easy to overlook the fact that it also took a lot of money. It took a lot of money poured into basic research at universities and private companies, along with a lot of money poured into engineering development.

Kennedy's best-and-brightest theme wasn't original, and the belief wasn't unique to him. Americans have believed that we're the best and brightest for at least a couple of hundred years. After all, we whipped the all-powerful British, tamed a continent, won two world wars (almost single-handedly, we like to think) and became the world's banker, farmer, merchant, benefactor and protector in that time. It's not surprising, then, that our egocentrism pins the credit on having the best and the brightest and conveniently lets us forget the enormous wealth committed to this success.

It wasn't always called R&D, so it's easy to forget that until the 1970s, the United States poured more money, both public and private, in absolute terms and as a percentage of its gross national product (GNP), into basic research and *both* engineering and industrial development than any other nation in the world. Last year, for example, we spent more than $120 billion on R&D, which was more than Japan, West Germany, France and the U.K. spent together. Of that, about one-half—$58 billion—was spent by private industry. While $58 billion sounds like a lot, and it's more than our competitors spent, it falls far short of what our competitors are spending in terms of GNP. In 1986, for example, the Japanese spent about 3 percent of their GNP on nondefense R&D and the West Germans about 2.6 percent. The U.S. spent only 1.8 percent.

Whether you have more of the best and the brightest is totally irrelevant. What counts is how adequately you support the best and the brightest that you have. It may be a simplistic view, but the percentage of a nation's wealth spent on R&D is a better measure of *commitment* to support its best and brightest than the total amount spent. On that basis, there are at least a couple of more serious competitors in the race. If we don't reevaluate this commitment—along with a few others, primarily one to education—then all of the hoopla about more jobs, a second coming of the Massachusetts Miracle (for those who believe in miracles) and a better America is nothing but hoopla. If we don't, R&D won't mean research and development; it will mean retreat and defeat.

John Miklosz

How To Wring Workstation-Level PCB Designs Out Of Your PC.

P-CAD's new Master Designer turns an ordinary PC into a full-fledged PCB workstation.

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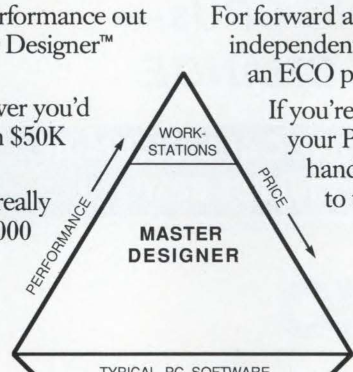

For forward annotation of logic changes and "history independent" back annotation, Master Designer also has an ECO processing option.

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CIRCLE NO. 13

INTEGRATED CIRCUITS

Fast GaAs and BiCMOS parts rekindle designers' interest in ECL

Ron Wilson, Senior Editor

The I/O specifications of ECL, long associated with power-hungry silicon bipolar circuitry, are being usurped by newer technologies. In the process, the newer technologies may move this 25-year-old interface standard to center stage in digital design. Within three years, some observers predict, ECL may be the dominant logic I/O scheme in the industry.

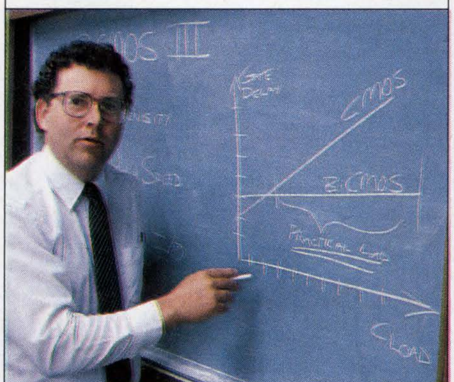
Three trends support ECL's move to dominance. First, ECL's current-steering, noise-resistant I/O spec is the choice for new parts that run faster than conventional bipolar silicon. Second, BiCMOS technology, by combining dense CMOS logic with bipolar drivers, is finally providing the high-speed, high-density VLSI parts ECL has previously lacked. Third, designers who have been bloodied by struggles with TTL's growing switching-noise problems are reevaluating ECL's reputation as a hard-to-use technology.

Breaking speed limits with GaAs

One company's recent announcement makes it clear that ECL remains the I/O scheme of choice for vendors at the furthest edge of the performance envelope. Microwave Semiconductor (Somerset, NJ) has announced a family of gallium arsenide logic devices that are pin-compatible with, but twice the speed of, existing 100K ECL parts. In fact, the company sacrificed some of the potential speed of its GaAs process to make the four new logic parts drop-in compatible with corresponding 100K ECL parts.

"We define compatibility to mean same power-supply requirements at similar consumption, same rise and fall times, and same temperature compensation," says Curtis Kraut, Microwave Semiconductor marketing engineer. "You can pull a conventional F100113 quad driver out and put our GaAs G100113 in, and the circuit will work. Everything will be the same except that the G100113 will have about half the propagation delay that the silicon part has."

The four parts include the quad latch, a 100141 8-bit shift register, a 100179 look-ahead carry generator and a matching 100180 6-bit adder. "We chose to start out with the parts that showed up in the most critical paths of existing designs," Kraut says. "All four parts are sampling now. By first quarter 1989, we'll be sampling a total of 14 devices in the G100K family." Later that year, Microwave Semiconductor expects to announce a family of 100K-compatible GaAs gate arrays to complement the company's standard products.



With BiCMOS, you can spend the bulk of your power budget on the few bipolar drivers that are on critical paths, according to Charles Hochstedler, product planning manager for the memory division of National Semiconductor. This strategy lets National's 256-kbit BiCMOS static RAM with ECL I/O achieve both 15-ns access time and very low power consumption.

ECL and BiCMOS work together

A growing family of ultrafast ECL elements and arrays perfectly complements the plans of BiCMOS vendors. "BiCMOS has some key advantages—and disadvantages—in the ECL world," says Charles Hochstedler, product planning manager for the memory division of National Semiconductor. "For very fast parts such as 3-ns RAMs, other technologies can do a better job today. It's very difficult now to design level translators that are fast enough to go between the CMOS and bipolar portions of a BiCMOS circuit at those speeds.

"But in the 15-ns range, BiCMOS provides extremely high packing densities at low power consumption. Essentially, BiCMOS lets you spend the bulk of your power budget on the few bipolar drivers that are on critical paths. The majority of the circuit elements can demand very little power," says Hochstedler. National cites its 15-ns, 256-kbit static RAM with ECL I/O as an illustration of this principle.

Integrated Device Technology agrees wholeheartedly on the important role of BiCMOS in the ECL world. "Physics is on our side," points out David Wyland, IDT manager of product definition and applications. "As you shrink a CMOS die, both the on-resistance and the capacitance of the transistors go down. As a result, speed increases at about the square of the change in dimension. With our current .8-micron L_{eff}, CMOS devices driving on-chip loads have propagation delays comparable to those in the best bipolar processes."

IDT recognized this trend some years ago, according to Bill Snow, ECL marketing manager. "We saw that we were going to have very fast on-chip logic, but that for high-current needs—when a signal had to leave the chip, for example—CMOS drivers were always going to be slow. So we targeted our BiCMOS process at this problem."

IDT chose to make a 64k×1-bit SRAM the technology driver for the process. The company designed the part with a CMOS memory array, but bipolar word line drivers, sense amps and pin I/O. Recently, the vendor announced that the part has achieved 10-ns access times.

The ability of BiCMOS to make dense, low-power VLSI devices available at ECL speeds has been a godsend to designers of high-end computers. In Cray-class machines, huge arrays of main memory must function at 15- or 20-ns access times. The new BiCMOS parts have substantially reduced the size and power consumption of these memories.

But SRAMs are just the first of a long line of VLSI BiCMOS ECL parts. As more and more complex devices

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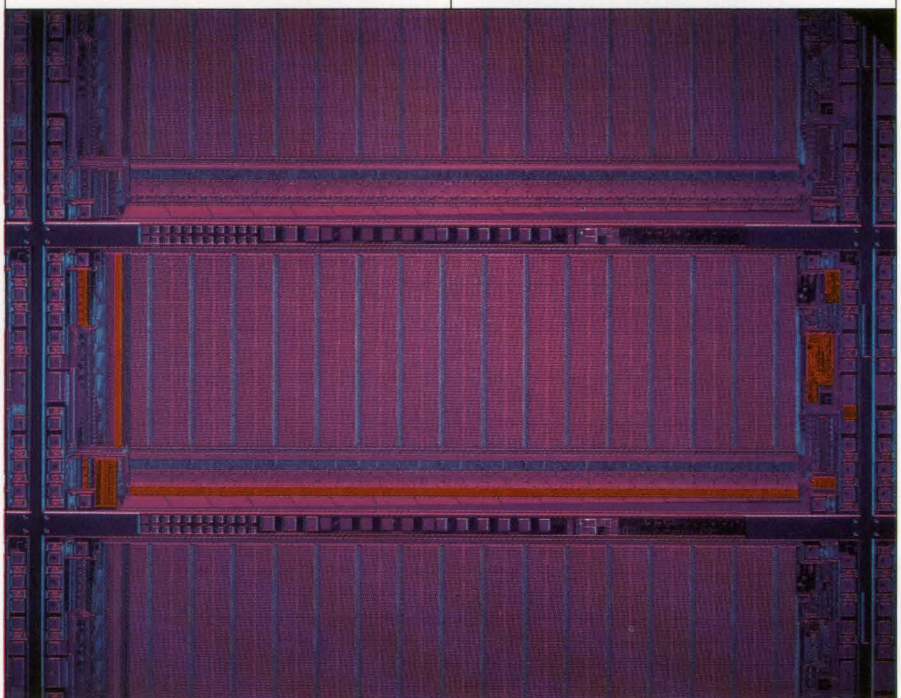
appear from the BiCMOS vendors, their availability will change the role of ECL in the industry.

A thicker parts catalog

"Ever since Motorola introduced ECL as an interconnect strategy for high-speed circuits, it's been the interface standard above 25 MHz," says Snow. Wyland adds, "Now, vendors are talking about RISC microprocessors with cycle times around 10 ns. TTL can't support that kind of speed. But ECL I/O—inherently three or four times faster than TTL—can."



A BiCMOS device uses CMOS to implement the bulk of the logic, and employs bipolar transistors only where higher currents are necessary. In IDT's 64-kbit static RAM, for example, bipolar circuitry—shown in red—makes up a small fraction of the total chip area but contributes greatly to the device's 10-ns speed.

But engineers, even when faced with the almost insurmountable noise problems of high-speed TTL design, have remained hesitant about moving to ECL. "One of the biggest issues for most designers has been the lack of a thick ECL parts catalog," observes National's Hochstedler. "But the underlying support chips are there. As ECL PLDs and ASICs begin to fill in the gap, this disadvantage will go away."

Wyland agrees. "There hasn't been a huge variety of ECL parts. But now, BiCMOS can combine very high integration with ECL's low interchip delays and can produce VLSI parts better than either CMOS or bipolar ECL could make by itself."

"We're already hearing rumblings of a RISC microprocessor with ECL I/O," points out Snow. "In one sense, it's already been done. A number of people have implemented RISC processors with ECL gate arrays."

ECL's changing reputation

The last important barrier to the widespread use of ECL I/O is an old prejudice. Many engineers who are comfortable designing with TTL feel that ECL, with its 50-Ω balanced lines and strange-sounding design rules, is inordinately difficult to use. But the increasing speed of TTL interconnect, as well as TTL's waining ability to deal with the speed, may be making this point of view obsolete.

"People hate worrying about transmission lines," agrees Hochstedler, "but there's no way to avoid it anymore. Even at the lower speeds of advanced TTL, you have transmission-line effects to think about, so you have to do that work anyway. And with TTL, you have the switching-noise issues. ECL may actually turn out to be the simplest, not the hardest, solution."

So for the speeds demanded by next year's microprocessors, ECL I/O design rules may be simpler than even TTL design rules. The traditional view of ECL devices as power-hungry small-scale parts from a thin catalog is being revamped by new BiCMOS offerings. And the center of the action in new, faster-than-bipolar GaAs parts is shifting toward strict ECL compatibility.

"We've seen this phenomenon before," claims Wyland, "when CMOS technology took over TTL. The I/O standard stayed, but a new device type moved in." In general, observers seem to agree that I/O specifications, like TTL or ECL, are related to operating frequencies, not implementation technologies. Today, as the action moves into a frequency range TTL can't handle, it's logical that the best implementation technology would move to ECL I/O.

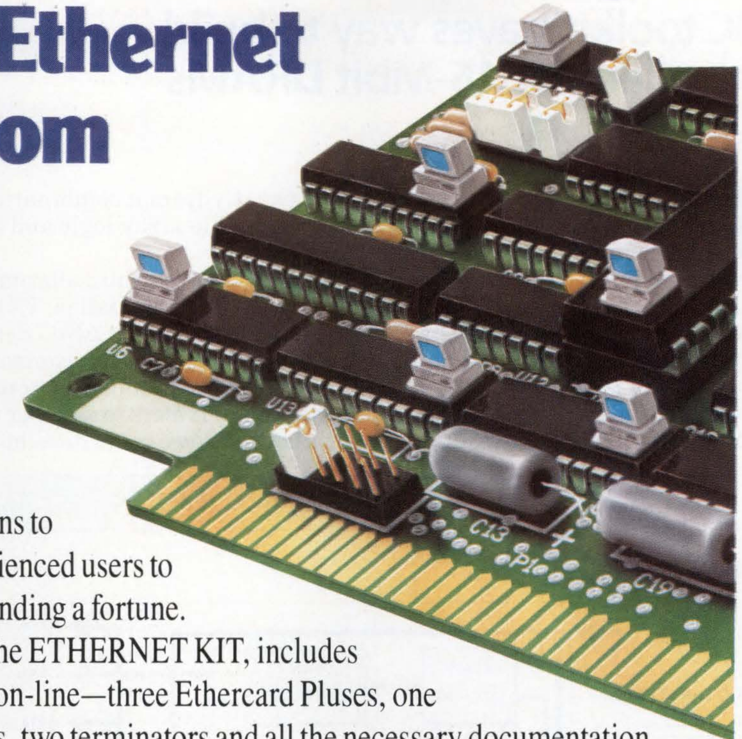
As the process continues, TTL I/O could become stale, used only in noncritical designs. A new group of parts could emerge, operating in the area beyond ECL speeds. Here, technologies like GaAs, diamond film and superconducting logic could be free to optimize I/O for their own internal needs, without the slowing constraints of ECL compatibility.

But the mainstream of digital technology would shift to ECL I/O. Most new parts would be available with ECL compatibility, and most new designs would use ECL rules. In a fine irony, the logic family long avoided as complex and demanding could, after a 25-year wait, emerge as the simple solution to increasing digital speeds. ■

Coming September 1

Watch for Ron Wilson's Technology Report on 16-bit microprocessors.

Hall-Mark makes networking easier with Ethernet Solutions from Western Digital



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CIRCLE NO. 15

INTEGRATED CIRCUITS

ASIC toolkit paves way to build controllers for 16-Mbit DRAMs

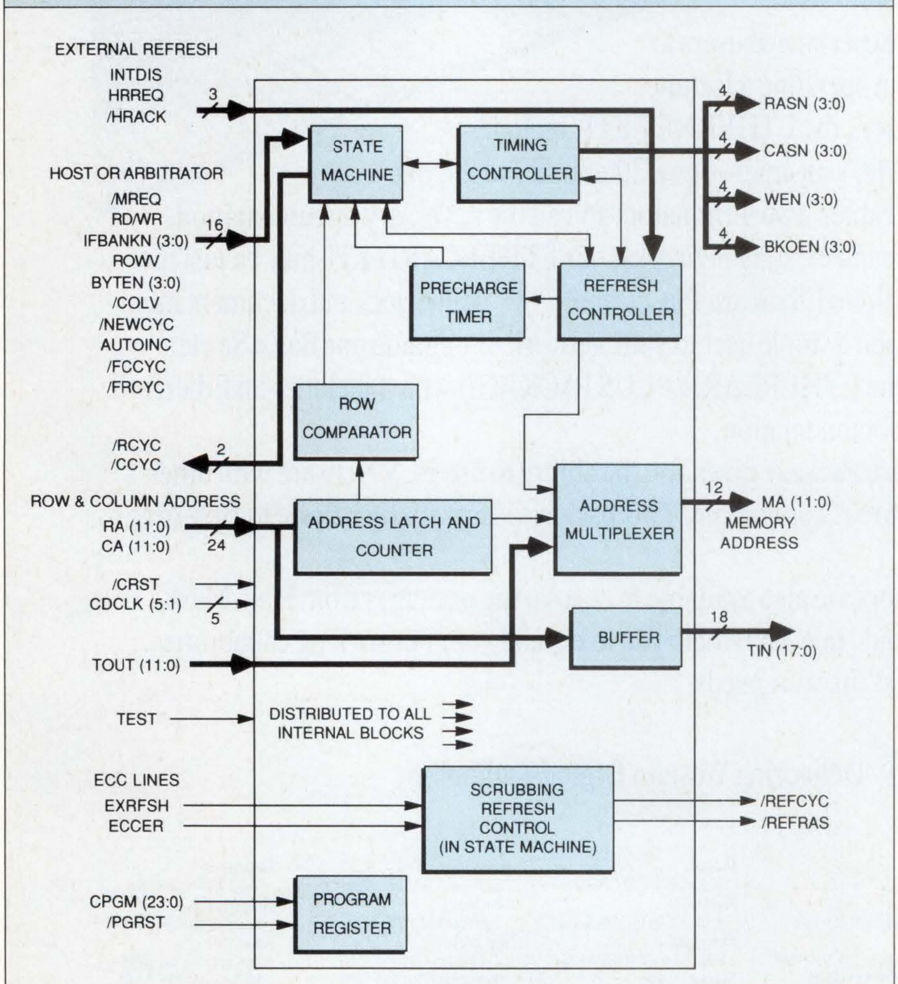
S. Louis Martin, Contributing Editor

Hot on the heels of 1-Mbit dynamic RAMs, 4-Mbit DRAMs will arrive soon. And 16-Mbit DRAMs, if not around the corner, are certainly just down the block. As DRAMs have become crucial, so have the controllers for them. But until now, designers of memory systems have had only two options—to buy controllers off the shelf or to roll their own, usually from a combination of programmable array logic and MSI/SSI devices.

But now there's a third alternative. Texas Instruments (Dallas, TX) will announce this fall an ASIC designer's toolkit for DRAM controllers that contains a number of standard cells, which TI refers to as super macros, that help designers develop controllers for up to 16-Mbit DRAMs. The toolkit has macros for the most advanced features of the new generation of DRAM controllers, including the accommodation of a variety of processor interfaces.

Inclusion of the processor interface is a feature of the newest generation of off-the-shelf DRAM controllers. The recently introduced DP8420/21/22 standard-product controller from National Semiconductor (Santa Clara, CA), for example, is progammable via a 22-bit register, which lets it be interfaced to a variety of processors. A similar part, the KS84C21/22 controller from Samsung Semiconductor (San Jose, CA), also provides register programmability and mask programmability. (See "Fast, full-featured 4-Mbit DRAM controllers begin to surface," *Computer Design*, Aug 1, p 26.)

ASIC DRAM TOOLKIT CONTROLLER BLOCK



The controller macro of the TI toolkit offers multiple row-address strobe (RAS) and column-address strobe (CAS) outputs for bank selection and byte or word access. It operates with a 50-MHz clock, and RAS-to-CAS low time is programmable in 20-ns intervals. Via a test mode pin, the address bus may be used to transmit test data onto a test bus, allowing completely independent testing of the memory system.

Toolkit supports five interfaces

Separate macros in the the TI toolkit support five processor interfaces—the 68020, 68030, 80186, 80286 and 80386. "These blocks are direct-marry blocks to the processor. They include all the decode logic," says Steve Gumm, product manager. TI will add macros for other processor interfaces to the library, according to Fred Tabaian, program manager. Users also have the option of designing their own custom interfaces. Other devices such as direct memory access (DMA) controllers can also be interfaced.

The most outstanding feature of the TI approach is that up to four interfaces, on a fixed-priority basis, can be included on a DRAM controller built using the new toolkit. As a result, the toolkit can provide what might be called "multiple accessing"—comparable to the dual-accessing feature of the new controller from National. But the TI approach is more flexible, letting as many as four processors gain access to the same memory or bank. (The Samsung Semiconductor part doesn't provide dual accessing.)

A further distinction between the National part and the TI toolkit has to do with external logic. While the National controller allows accessing by different processors, like a 68020 and an 80386, additional logic is required for whichever processor is port

B. With the TI toolkit, the interface is complete for all ports. "By the time you put the toolkit together, you don't need any external logic," says Gumm. Moreover, all interfaces are asynchronous, as opposed to the standard product from National, where port A must be synchronous and port B must be asynchronous.

The latch-and-go write capability

A unique feature of the toolkit is the read and write registers in the interface blocks, which provide a "latch-and-go" read/write capability. "Let's say you have a 68020 interface," explains Gumm, "and the 68020 wants to do a write. You can program up for a latch-and-go write where that write would be latched with zero wait states for the 68020, and the latched data would be written to memory later when memory became available." A complementary capability is available for read operations.

"The controller is the heart of the system, and it has an extreme amount of flexibility."

—Fred Tabaian, Texas Instruments

■ ■ ■

The latch-and-go write capability maximizes the CPU bandwidth. In turn, the latch-and-go read capability maximizes the memory bandwidth, since memory access isn't slowed by waiting for a processor to fetch its data. "As soon as the data is available from memory, it's latched and the memory system is free to go on and process someone else's request," says Gumm.

Another noteworthy feature of the TI toolkit is that the number of wait states is separately programmable for each of the interface macros that a design requires. For port B in the National part, external logic is required for wait-state support.

Flexible controller macro

The centerpiece of the toolkit is a controller macro that includes traditional DRAM controller functions such as address multiplexing, row-address strobe (RAS) and column-address strobe (CAS) generation, refresh address counters, and timing and control. "The controller is the heart of the system, and it has an extreme amount of flexibility," says Tabaian.

The controller macro supports DRAMs from 256 kbits to 16 Mbits. And it allows use of DRAMs with access times ranging from 80 to 150 ns. "It covers a whole spectrum of DRAM capacity and speed," says Tabaian. The controller block supports multiple RAS and CAS outputs. The RAS0-3 outputs let users

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select up to four banks of DRAMs, while CAS0-3 can be used for various combinations of byte or word access.

Also supported are a variety of a refresh modes and numerous accessing modes. In addition, the tools support both external scrubbing and error checking and correction. Two signals from the controller block allow the cycle to be extended for error correction when required.

The controller macro uses a 50-MHz clock for the base frequency and a phase-locked loop to derive a signal with an edge at 10-ns intervals that can be used for timing purposes. Row-address hold time is programmable in 10-ns intervals; RAS-to-CAS low time is programmable in 20-ns intervals. In comparison, the off-the-shelf device from National operates up to 25 MHz, while Samsung Semiconductor is promising a version that will operate up to 40 MHz.

The toolkit also provides a test bus that lets the complete controller chip (interface blocks, arbiter block and controller) be tested independently of any other logic that may be included on the same piece of silicon. A test pin throws the device into test mode, allowing test data to be brought in over the address bus and each block in the DRAM controller system to be independently addressed and tested.

■ Toolkit part of broader effort

The toolkit, along with extensive documentation on how to build DRAM controllers, is a supplement to the TSC-500 standard cell library from TI. The tools, which run on a Mentor workstation, are currently available, though they haven't been formally announced.

The DRAM controller toolkit is, in fact, part of a broader effort at TI to develop toolkits for a number of specific applications. "The approach of the toolkit is to provide a complete information package that lets designers build customized versions of standard products, such as DRAM controllers. We provide preconfigured super macros—predefined functional blocks designed using standard cell methodology," says Jerry Koontz, ASIC merchandizing manager. Thus, TI spares the system designer from having to design from the ground up—and in the case of a DRAM controller, provides advanced features and an easy upgrade path. ■

Microcontrollers with on-chip A-Ds raise speed, accuracy issues

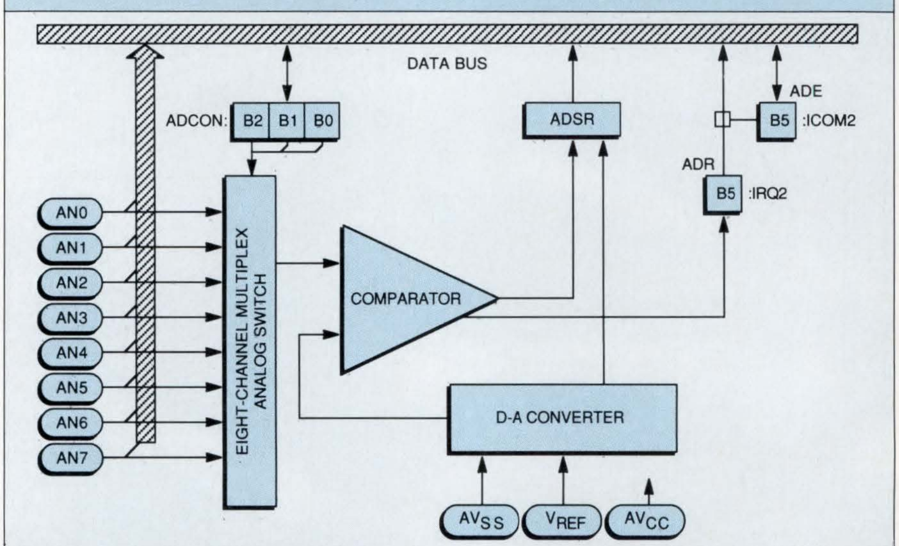
Ron Wilson, Senior Editor

The most fashionable accessory for the well-dressed single-chip microcontroller this season is an on-chip analog-to-digital (A-D) converter. This integrated A-D capability, highlighted in recent announcements from Mitsubishi Electronics America and Signetics (both of Sunnyvale, CA), can save space and effort for designers of embedded systems. But the on-chip converters are very specialized devices and are easily misused. Designers need to understand the limitations of integrated A-D converters and be aware of the alternatives now available for embedded-system data conversion.

"The majority of A-D converters on single-chip microcontrollers are 8-bit, successive-approximation devices," says Ike Saeed, manager of microprocessor applications engineering at Mitsubishi. "The parts evolved to meet the needs of appliance and consumer product applications." In these applications, according to Saeed, the A-D converters are generally used for such tasks as reading transducers or digitizing slowly changing signals, such as temperatures in ovens and exposure in cameras.

As the popularity of on-chip A-D converters increases, the parts are finding new applications. "We have seen designs where the on-chip converter digitizes voice signals in a message system or serves in a feedback loop in a disk controller," notes Saeed. But when designers use the parts to digitize higher frequency signals, they risk using the converters improperly. "The cost of a separate A-D converter can be high," warns Azmat Malik, Mitsubishi's ASIC/MCU product manager. "This tempts some engineers to misuse the integrated A-D converters. In some applications, you can get away with that, but in others, you're going to get burned."

A-D CONVERSION CIRCUIT STRUCTURE



Nearly all analog-to-digital converters on microcontrollers are of the 8-bit successive-approximation type, as shown in the M37450M2 device from Mitsubishi Electronics America. The converter selects each successive bit of the digital output based on the difference between the current output and the input.

Better specs needed

The first barrier designers face in using the integrated A-D converters is the lack of appropriate specifications. Data-sheet figures reflect the original intent of the on-chip converters: digitizing static signals. So the only specifications available may be resolution and conversion time.

But it can be quite difficult to relate these dc characteristics to the actual behavior of the converter. For example, vendors generally list the resolution of an A-D converter as the number of bits of data it provides to the microcontroller. This can be quite different from the accuracy of the device: it's not uncommon for an 8-bit on-chip A-D converter to give 5-bit accuracy in actual applications.

"On almost all the chips I've looked at, the accuracy of the converter isn't specified," observes Nick Gray, applications section head for data conversion and interface products at Signetics. "Because the accuracy of conversion depends so much on whatever digital activity is taking place on the chip, the data sheets practically say, 'Yes, there's an A-D converter on here; use it at your own risk.'"

Conversion time can also be misleading to a designer trying to digitize rapidly changing signals. In this case, the problem isn't that conversion time is imprecisely specified; it's that by itself it can't tell a designer whether the converter will be fast enough to handle a given signal.

> ***"The majority of A-D converters on single-chip microcontrollers are 8-bit, successive-approximation devices."***
>
> *—Ike Saeed, Mitsubishi Electronics*

Neither of these specification issues is the result of a vendor's attempt to mislead customers. If the designer wants to digitize a near-dc signal with 2 to 5 percent accuracy—the type of task for which on-chip converters were conceived—the data-sheet specifications tell the entire story. It's when designers try to use the A-D converters for more ambitious tasks that data-sheet figures are inadequate. In this realm, where higher accuracies or higher signal frequencies are an issue, designers must understand more about the design of on-chip converters and the devices' consequent limitations.

Physics affects performance

"The fundamental problem with accuracy in on-chip A-D converters is a phenomenon called charge injection," says Signetics' Gray. "High-

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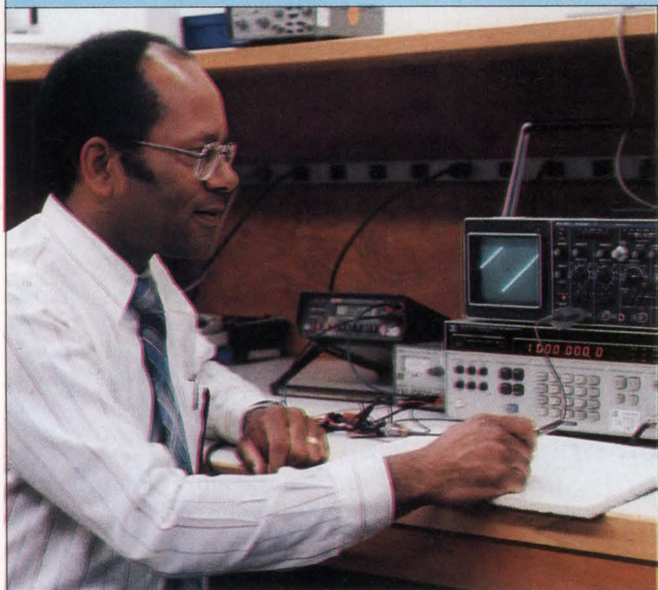


Data sheets indicate resolution and conversion time, but, from the experience of Nick Gray, Signetics' applications section head for data conversion and interface products, the accuracy of an integrated A-D converter is rarely specified. "Because the accuracy of conversion depends so much on whatever digital activity is taking place on the chip, the data sheets practically say, 'Yes, there's an A-D converter on here; use it at your own risk.' "

speed digital activity on the microcontroller injects energy into the chip's substrate. This energy gets into analog circuitry and hurts the accuracy of the converter. It requires very special design and layout techniques to isolate the analog section of the chip from the digital section for even 8-bit accuracy."

The effects of charge injection show up in accuracy specifications. Mitsubishi lists the absolute accuracy of the 8-bit A-D converters of its new MELPS740 series of microcontrollers at ±3 least-significant bits, worst case. This works out to just over 1 percent of full scale. Such accuracy is acceptable for applications where signals are likely to be near full scale under operating conditions and where 5 or 10 percent absolute accuracy is sufficient.

In applications that need greater accuracy, some designers have tried to minimize the interference from the digital portion of the chip by simply halting the microcontroller. But this approach cuts into processing time and locks out interrupts for the 20 μs or so required for A-D conversion, although on some microcontrollers it can improve accuracy.

The long-term solution, though, will come from better isolation techniques. Gray reports that Signetics' efforts in this direction are producing results. The 80C552 chip, which offers a 10-bit on-chip A-D converter, is a beneficiary of the company's development work in isolation techniques.

"Some customers are reporting 9-bit accuracy from the part in actual applications environments," says Gray.

■ Limits on input frequency

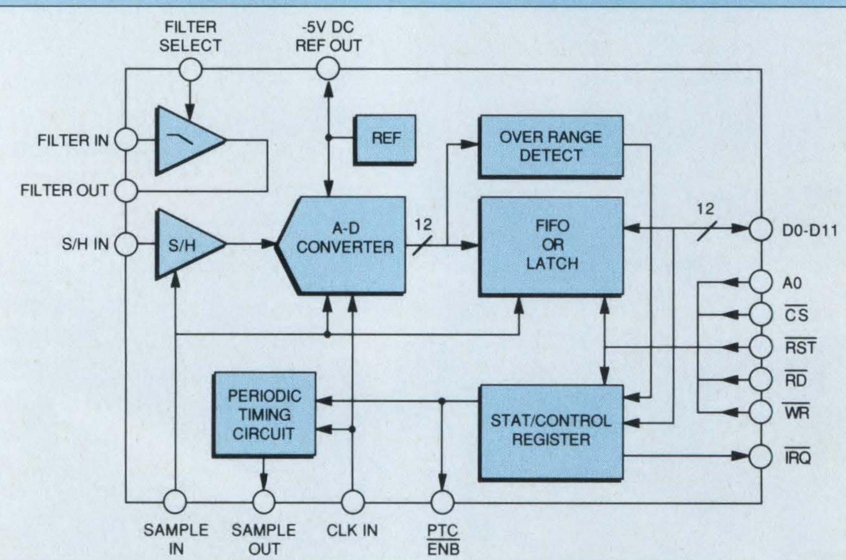
The charge-injection phenomenon also plays an indirect role in limiting the signal frequency on-chip converters can handle. Charge injection makes it impractical to build a sample-and-hold (S/H) circuit on the microcontroller chip. And the lack of an S/H severely limits the converter's ability to accommodate changing signals.

"Vendors don't put S/H circuits on the chips because S/H devices must have an absolutely quiet substrate," claims Gray. But the absence of an S/H creates a fundamental problem for the converter. "These on-chip A-D converters are successive-approximation devices," says Gray. "Since they compare the input to their output throughout the conversion process, the input must remain stable during the entire conversion time."

This requirement has a big impact on input frequency requirements. Most designers think of input frequency constraints for A-D converters in terms of the Nyquist criterion, which requires the maximum input frequency to be less than one-half the sample rate. But the Nyquist criterion assumes instantaneous sampling. Without an S/H, the requirement that the input remain constant within conversion accuracy during the conversion time is vastly more demanding.

For example, a well-designed on-chip converter might achieve 7-bit accuracy with a 20-μs conversion time. In this case, the input signal couldn't change more than about 0.4 percent in the 20 μs. That works out to a maximum frequency for a full-scale sine

THE AD1332 ANALOG-TO-DIGITAL SUBSYSTEM



Highly integrated analog-to-digital subsystems, such as Analog Devices' AD1332, can pack all the necessary stages of an ac data-conversion system into a single chip not much bigger than an external sample-and-hold (S/H) unit. Such packages provide an important alternative to on-chip A-D converters for non-dc applications.

wave of around 30 Hz. With a precise S/H, the Nyquist criterion would allow an input frequency of around 20 kHz, almost 1,000 times greater.

Going external for speed

Vendors of discrete data-conversion products are quick to note the frequency limitations of on-chip A-Ds. "Unless your signal is very slow moving, you're going to need some external components," claims William Schweber, senior technical marketing engineer for Analog Devices (Norwood, MA). He notes that there are three stages in a data-conversion system: a frequency-limiting filter, an S/H and an A-D converter. It's only the assumption of near-dc input that lets a microcontroller user leave out the first two stages.

When the signal to be digitized contains audio—or higher—frequencies, each stage plays an important role. The antialiasing filter removes frequencies greater than those allowed by the Nyquist criterion, thus preventing aliasing from creating false components in the digitized waveform. The S/H samples the signal at precise intervals. "This precision is essential, since jitter in the sample interval translates directly into noise in the digitized output," claims Schweber. And the S/H holds the input to the A-D converter constant during conversion, so the A-D converter can function properly.

So for higher frequency applications, an external filter and an S/H are necessities. But vendors of standalone A-D converters argue that if the system is going to require external packages for these functions anyway, it makes sense to use an external A-D converter as well. "As a general rule, demanding applications are going to be better off with a separate A-D converter," says Signetics' Gray. "Once you move the converter off the microcontroller chip, there are a lot of alternatives."

Not surprisingly, Analog Devices' Schweber agrees, observing that separating the converter from the microcontroller greatly improves conversion accuracy and speed. In addition, when the converter is used as the front-end in a signal-processing application, separate A-D converters may offer other advantages.

"Many A-D converters are becoming closely tuned to their intended applications," Schweber says. "For signal-processing applications, where integrity of the waveform is more important than dc behavior, we have been measuring and specifying ac characteristics such as signal-to-noise ratio and harmonic distortion. These figures determine what the converter is going to do to your signal, but they're unknowns for most parts." This novel approach to characterizing A-D converters is producing a new generation of parts, optimized for their ac characteristics rather than their dc performance, according to Schweber.

No increase in package count

Finally, champions of discrete A-D converters point out that moving the converter off-chip may not increase the design's package count. Once the design commits to one external package for an S/H unit, that one package may be able to accommodate the entire data-conversion subsystem.

An example of an off-chip alternative is Analog Devices' AD1332. This device offers a 12-bit, 125-kHz A-D converter with a programmable four-pole Butterworth antialiasing filter, an S/H and a microcomputer interface with a first-in, first-out buffer, all in a single 40-pin package.

So designers have a wealth of available options. If the microcontroller must digitize a slowly changing signal with moderate accuracy, an on-chip A-D converter may handle the job splendidly. If the application is concerned with the shape of the incoming waveform rather than with static values, or if more than 2 or 3 percent accuracy is necessary, the designer may be wise to investigate highly integrated, separate data-conversion parts. The key to success is to compare the nature of the data-conversion task against the restrictive design assumptions implicit in the on-chip converters. ■

Graphics coprocessors meet increasing demands for floating-point math

Tom Williams, Western Managing Editor

A major boost in floating-point math capability for board-level graphics controllers is on the way with the introduction of a next-generation graphics processor from Texas Instruments (Dallas, TX). The TMS34020, which by itself would be an upgrade of TI's present 34010, comes with a 40-MFlops floating-point coprocessor that does standard arithmetic as well as a number of math-intensive graphics operations. The pair, which were developed concurrently, appear to be a firm indication that today's graphics applications, especially three-dimensional graphics, are making tremendous demands for floating-point math.

The current generation of graphics processor ICs has been a study in trade-offs between speed and flexibility. Hardwiring a selected set of graphics functions makes graphics processors run very fast but reduces their programmability. A high degree of programmability lets a graphics processor adapt to new algorithms, but the multiple-cycle instructions tend to slow the chip down.

No matter how much clock speed is increased through advances in process technology, the basic trade-off choice remains. On the one hand, we've seen devices like the 82786 from Intel (Santa Clara, CA) and the 95C60 from Advanced Micro Devices (Sunnyvale, CA)—processors with relatively small sets of hardwired functions. On the other hand, we've seen the 8500 raster graphics processor from National Semiconductor (Santa Clara, CA) and TI's 34010 graphics system processor—chips that closely resemble general-purpose CPUs in their programmability but have added specialized graphics instructions. All attempt to optimize both functionality and speed.

But in continually moving toward more sophisticated modeling and rendering, graphics processing is making increasing demands on silicon. One demand is for floating-point arithmetic both in geometry opera-

INTEGRATED CIRCUITS

tions such as rotation and scaling and in pixel-rendering operations such as the shading of surfaces. Once the domain of high-end workstations, 3-D images are showing up on IBM PC ATs, 80386-based platforms and, no doubt soon, Macintosh platforms. The need is growing for board-level products on these platforms equal to the new graphics task. These products will require a graphics engine that can execute high-level commands with little intervention from the host CPU across the system bus.

For a graphics engine to do that, it will need its own floating-point capability or, at least, exclusive access to a floating-point coprocessor. Because of the number of floating-point operations needed and the bus overhead involved, farming out floating-point operations to the host CPU, even an 80386/80387 pair, will no longer be adequate. For example, a 3-D wireframe image that takes 0.3 MFlops to render at 1 frame/s could take more than 20 MFlops to render as a shaded solid at a dynamic frame rate of 20 frames/s. The more complex the scene, the greater the demand becomes.

■ Coprocessor tailored to graphics

Responding to the need for floating-point capability, TI has included a powerful floating-point coprocessor, the TMS34082, with its recently announced second-generation graphics system processor, the TMS34020. The 34082 connects directly to the address and data buses of the 34020 and includes a number of functions specifically tailored to graphics.

The 34020 is what one might expect as a follow-up to the 34010. It's fully upward-compatible with 34010 software and has the same internal 32-bit CPU as the 34010. But it also has a full 32-bit-wide data bus and a 4-Gbit address range. That means individual bits can be addressed directly by specifying x and y coordinates, letting a programmer access, for instance, one bit plane in a frame buffer to change a color or to perform a block transfer without having to access and mask out unwanted bits.

One of the main criticisms of the 34010 was that although it was very good as a line-drawing engine, it tended to bog down in applications that required many large bit-boundary block-transfer (bitblt) operations. This failing became particularly apparent in window-oriented applicaions. TI claims to have improved the situation by using two- and three-operand block-transfer instructions and by implementing a window clip/pick function in hardware. The new hardware cuts down on the compute-intensive chore of clipping an image to the boundaries of a window.

TI has also redesigned the memory interface so that it can directly control 64-kbit, 256-kbit and 1-Mbit dynamic RAMs and video RAMs. The new interface actually has capabilities well beyond what it needs for current parts, according to Frank Laczko, manager of advanced systems for TI's VLSI logic division. "The 34020 has the multiplexing and refresh capability to handle 64-Mbit DRAMs, if they existed," he says.

Like its predecessor, the 34020 connects directly to video RAMs. In fact, TI is announcing a 1-Mbit CMOS video RAM, the TMS44C251. This RAM is organized as four 512- ×512-bit arrays so that the arrays are available for CPU writes during the time in which 512 four-bit pixels are being serially shifted out of a single RAM chip.

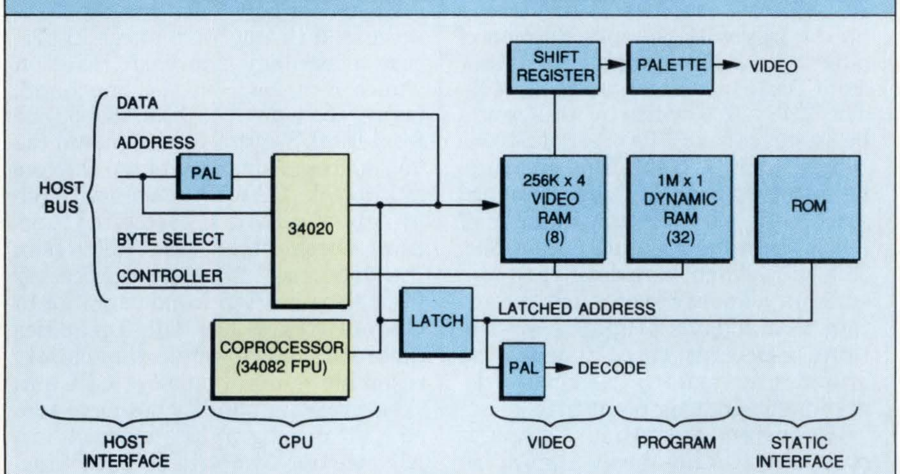
■ Multiple FPUs accommodated

What makes the 34020 more than just a second-generation graphics processor—besides its coprocessor interface—is the existence of the 34082. The 34020 can accommodate multiple floating-point units (FPUs)—up to eight, in fact. In addition, multiple 34020s can be ganged in parallel, making multiple CPU/multiple FPU configurations a possibility. The 34082, derived from TI's IEEE single-chip, 30-ns 8847 FPU, has a peak burst processing rate of 40 MFlops. In addition to supporting the IEEE-754-1985 floating-point standard, the 34082 includes internally microcoded floating-point functions specifically aimed at graphics applications.

Matrix floating-point operations, for example, are needed to move, rotate and scale an object on the x, y and z axes of its world coordinate system. World coordinates define the nature of the space in which an object being modeled exists. For instance, an astronomy model might use parsecs, while a molecular model might use angstroms. In each case, the coordinate system needs a large dynamic range and high accuracy, making floating-point arithmetic more efficient than integer. The 34082 supports these operations directly, as well as polygon clipping and 2-D and 3-D linear interpolation.

The FPU also supports 2-D and 3-D cubic splines, polynomial equations

A TYPICAL SUBSYSTEM ARCHITECTURE



This is one example of a graphics subsystem architecture using the TMS34020 graphics system processor and the TMS34082 floating-point coprocessor from Texas Instruments. The 34020 has equally direct access to the video RAM frame buffer and to dynamic RAM program memory, thus enabling the host to transfer large sections of code in a single operation, reducing bus overhead. In addition to its internal functions, the 34082 has access to user-designed microcode stored in ROM.

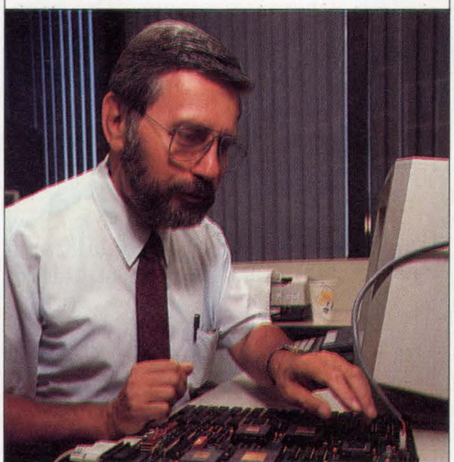
that increasingly are being used to represent curved surfaces. In addition, there's support for a class of vector operations that's useful in lighting and shading calculations. Viewport scaling and conversion are also supported. These functions help map points from the more abstract world-coordinate system to the final screen coordinates, which must be integer addresses in the frame buffer. In addition to these and other functions that reside in 512 words of hardwired microcode, the 34082 can address 64k 32-bit words of external microcode that let the user program customized floating-point algorithms for graphics or other specialized operations.

Support in other designs

There are, of course, other graphics processor designs in which the need for floating-point coprocessors has been recognized. Workstation graphics subsystems such as those from Raster Technologies (Westford, MA), Silicon Graphics (Mountain View, CA) and Hewlett-Packard (Palo Alto, CA) have long used specialized floating-point silicon—either custom-designed or dedicated commercial parts—to help more general-purpose processors perform graphics functions. And floating-point coprocessors are now finding their way into lower-end graphics solutions.

One lower-end graphics solution is the 32CG16 from National Semiconductor. Intended mainly as a printer processor, it's a full 32-bit CPU with additional bitblt and alignment commands as well as commands for binary data compression and expansion. The 32CG16 interfaces directly with two of National's FPUs: the 300-kFlops 32081 and the 480-kFlops 32381. Because the 32CG16 isn't intended for high-end 3-D color graphics control, its floating-point needs are more modest than those of the 34020. The FPUs serve mainly for 2-D scaling and rotation—an important operation for font handling in printers, says Les Wilson, National's manager of electronic imaging.

Wilson cites several designs built around National's DP8500 raster graphics processor that address the floating-point needs of higher-end graphics display systems. While the 8500 is an integer machine, it can work in conjunction with National's latest 32-bit CPU, the 32532, which itself can use a dedicated floating-point coprocessor, according to Wilson. National supplies a 32580 FPU interface chip so the 32532 can work with the 3164, a 64-bit floating-point processor by Weitek (Sunnyvale, CA). The idea is that the 8500, which is much like an integer CPU in its own right, would receive high-level rendering commands derived from floating-point calculations done by the 32532 and its coprocessor.



By teaming a floating-point coprocessor with a graphics processor, Texas Instruments is attempting to integrate integer, floating-point and graphics functions on a single processor. "We're trying to cover the whole range of processing requirements for graphics, from language and command processing to CRT control," says Frank Laczko, TI's advanced systems manager. How well such an approach pushes performance and flexibility has yet to be evaluated by the industry.

Single chip vs. pipeline

The TI approach tries to integrate integer, floating-point and graphics functions on a single processor that can get additional floating-point assistance from its own coprocessor when needed. "We're trying to cover the whole range of processing requirements for graphics, from language and command processing to CRT control," says TI's Laczko.

But, argues John Blair, National's strategic marketing manager for graphics, "Just because you can put everything on a single chip, it doesn't mean it's always a good idea." Blair claims that truly high-performance applications often do better with a pipelined architecture, where different operations can take place simultaneously. A single-chip solution often makes one operation wait until another operation is completed before the whole process can continue. It also makes it harder to tailor a hardware configuration to the needs of a given application.

While TI's ideal is clearly stated, it will remain for the industry to evaluate how well the company's latest move pushes performance and flexibility. Both the TMS34020 and the TMS34082 are expected to sample this fall and be generally available in the first quarter of 1989. ■

DESIGN AND DEVELOPMENT TOOLS

EDA vendors cooperate on EDIF and proposed CAD framework standard

Bill Harding, Contributing Editor

Transferring designs from one CAE system to another, integrating tools from different vendors into your CAE environment, or even changing CAE vendors without scrapping your design data base: designers have dreamed of these capabilities. And the dreams could come true within the next few years, if CAE vendors support EDIF (Electronic Data Interchange Format) Version 2.00 and if the recently announced CAD Framework Initiative (CFI) is successful. In a flurry of uncharacteristic cooperation at this year's Design Automation Conference (DAC) in June, six well-known EDA vendors demonstrated how designs can be passed from one vendor's schematic editor to another through the use of the EDIF 2.00 standard. Representatives from Mentor Graphics, Valid Logic Systems, Cadnetix, Hewlett-Packard, Texas Instruments and Viewlogic ran the demonstration. Meanwhile, also at DAC, CFI was announced by an interim steering committee. If successful, CFI will define a framework—a set of standards covering such things as human interface, data base structures, intertool communications and design management—that will let CAE/CAD tools from different vendors work together in an integrated system.

At first, it may appear that EDIF and CFI are competing methodologies, since both have the objective of providing a means for unlike tools to work together. That, however, is definitely not the case.

EDIF is a design interchange standard, defining an intermediate file format for transmitting component and connectivity information from one system to another. It defines how nets and symbols should be represented in an ASCII file format, and it addresses the top-end translation of files and their storage.

A framework, on the other hand, works at the operating system level rather than at the data file level. A framework addresses core data models to define how design data will be exchanged among tools and supports functions that go far beyond the transmission of file information from one application to another. EDIF, for example, supports only the transmission of component and connectivity information while a framework addresses human interface standards, design management and intertool communications.

Where EDIF stands today

When EDIF was formed, there were about 80 schematic-entry packages on the market. But because each system defined symbols and nets in a different way, a schematic couldn't be transferred from one system to another. EDIF's objective was to define a standard way for describing a net. By translating their schematics into this standard representation, users would be able to move designs from one schematic-capture package to another, and even move the designs to other tools such as layout packages.

Two early versions of EDIF were primarily experimental attempts to meet this goal and never became standards. But now that EDIF 2.00 has been accepted as an Electronic Industry Association standard, EDIF's objective has been met, at least in the area of schematic transfer.

A CAE vendor can support EDIF 2.00 by offering each of two products: an EDIF schematic writer and an EDIF schematic reader. The schematic writer translates a schematic file from the vendor's internal format into the standard EDIF format. The schematic reader does the reverse: it reads standard EDIF format files and translates them into the vendor's internal format.

But it remains to be seen how many CAE vendors will actually support EDIF 2.00. Like any standard, EDIF 2.00 must have industry buy-in to be successful. It finally appears to be getting that, in large part because of a growing demand among the CAE customer base for EDIF support by their CAE vendors.

> ***"There are too many issues that CFI isn't attempting to address."***
>
> *—Frank Costa, Mentor Graphics*

"This demand has become more pronounced over the last six months as customers perceive EDIF as an answer to many of their tool interface problems," says Elsa Reddy, EDIF representative at Valid Logic Systems (San Jose, CA). "The problem is that many customers expect more from EDIF than it can deliver."

David Ressler, EDIF product manager at Mentor Graphics (Beaverton, OR), agrees with Reddy that some people may be engaged in wishful thinking as to what EDIF can and can't do. EDIF doesn't carry all simulation models compatibly from one system to another, it doesn't yet address printed circuit board designs, and it isn't considered to be a good language for simulation. Also, since EDIF normally involves two translation steps when moving a design from one system to another, it can be inefficient.

What EDIF does is carry design connectivity, instances and graphics so you can get a basic design from one system to another. And that makes EDIF very useful, even with its limitations, according to Ressler.

"It will take several years to work out all the wrinkles," Ressler says. "But customers have capabilities now that they never had before. Many users are willing to put in extra effort (touch up a design, write a routine to handle library transfer, and so forth) because the design transfer capability is so important to them." He also pointed out that in cases where libraries are compatible from one system to another, or where no libraries are used, EDIF 2.00 works without any extra effort.

CFI: the new integration attempt

While EDIF appears to be the best technology available today for design interchange between systems, CFI offers the greatest hope for the more distant future. CFI represents a different approach to CAE/CAD standards. Its ambitious objective is to establish standards under which electronic design automation vendors can create tools that will work together within a total engineering environment.

While CFI won't define an industry-standard framework for several years, there are commercially available frameworks on the market today. EDA Systems (Santa Clara, CA) is a pioneer in frameworks for the CAE/CAD industry and can provide some insight as to what the CFI framework may eventually contain. CFI doesn't endorse the EDA product or any commercial framework product.

"A framework allows cooperation among tools," says Tony Zingale, marketing director at EDA Systems and CFI delegate. "For example, a schematic editor from vendor A can live in the same environment, on the same network and in the same workstation as a simulator from vendor B." He also points out that a framework means much more than just being able to transfer a net list. The framework includes management of data and of the process taking place. How does a change made to a sche-

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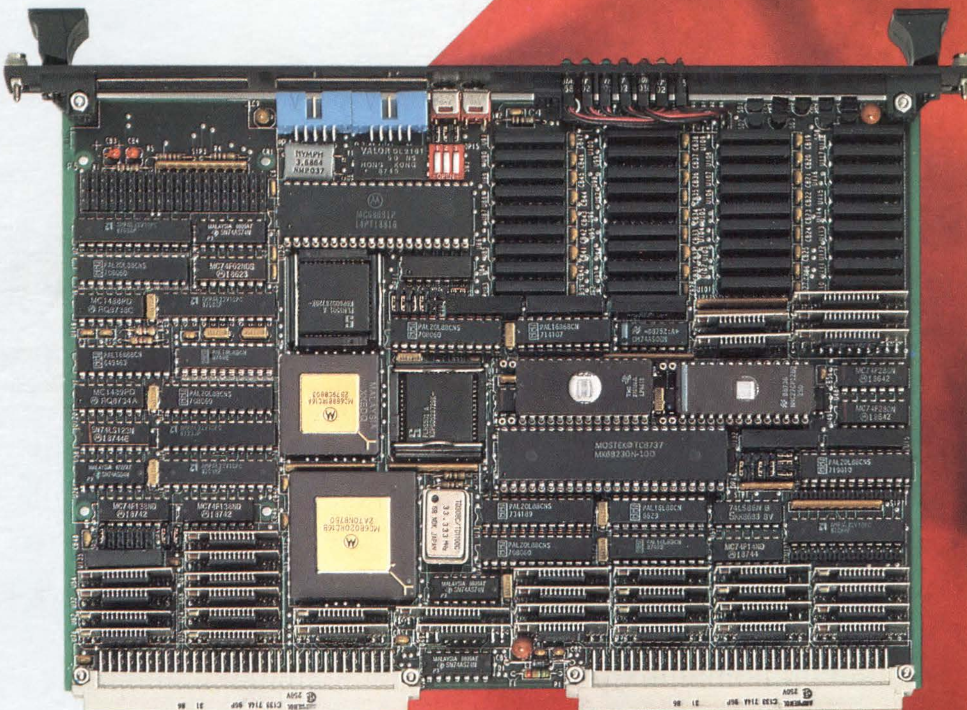

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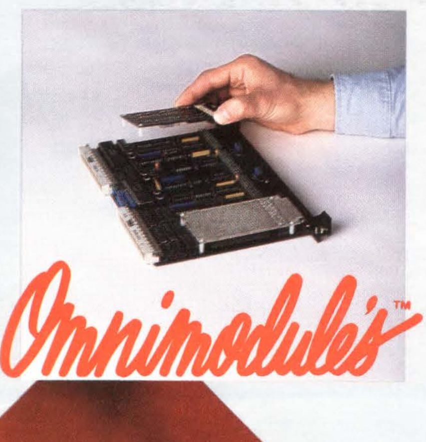

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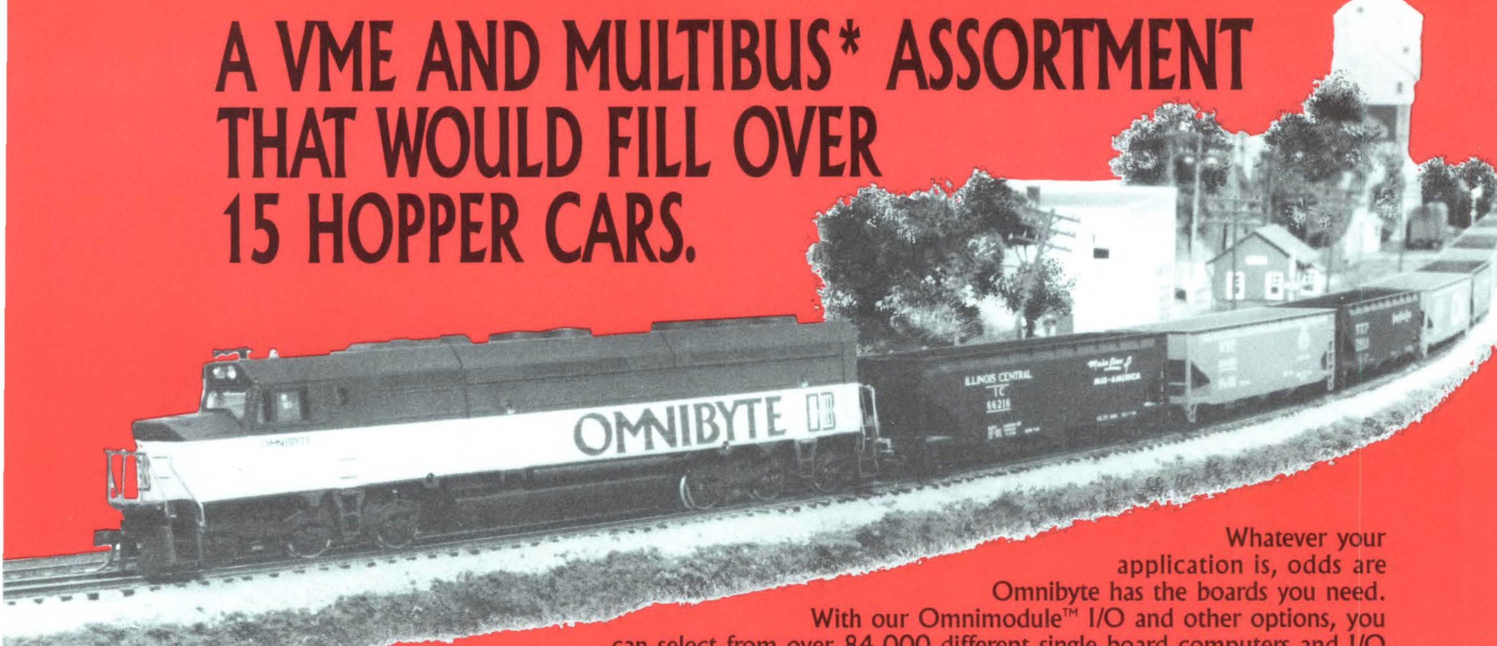

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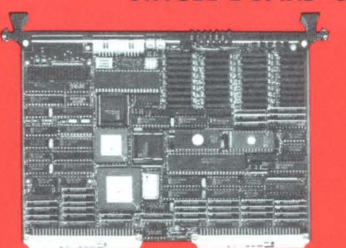

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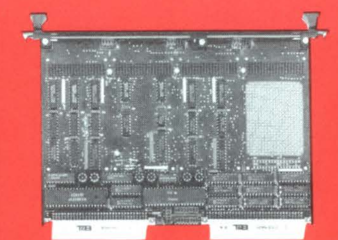

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- One (1) interrupt per Omnimodule, two (2) optional

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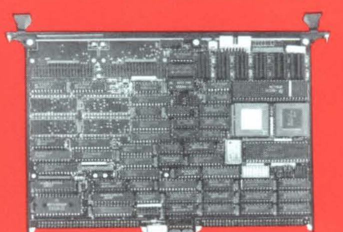

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- (3) 16-bit counter/timers
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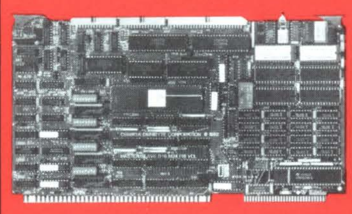

- 10MHz 68000 CPU
- 128K/512K of zero-wait-state dual ported RAM
- Up to 192K bytes of EPROM
- (2) RS-232C serial ports
- (2) 16-bit parallel ports
- A triple 16-bit timer/counter
- (7) Prioritized-vectored interrupts

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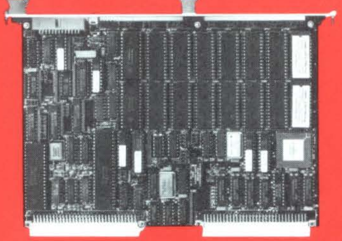

- 12.5MHz 68000 CPU
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- System controller

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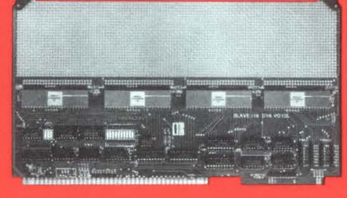

- 96 bits of software definable parallel I/O
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matic affect all the data previously generated? For example, if a library model is changed, the design management system ensures that all designs that use that model are updated. Or when a net list is changed during simulation, the design management system ensures that the schematic reflects the change.

Why a framework?

A framework appears to offer benefits to all parties. Customers want to be able to use the latest technology and don't want to be locked into a single vendor. If necessary, they want to be able to change their minds after having selected a vendor.

"The major customer investment is in data, not CAE equipment," says Mike Price, CFI delegate and Valid's vice-president of engineering. "Customers spend hundreds of man-years developing data, and if it isn't transferable, they're locked in."

Benefits aren't all on the side of the customer. Larger CAE vendors see CFI as a way to open up their competitors' customer bases as fresh sales opportunities. Vendors with specialized point solutions such as high-performance simulators or layout systems, one of the fastest-growing market segments, see CFI as a way to penetrate more design environments. Equally important to the vendor is that adopting standard human interfaces and data bases will free up R&D dollars that now go to supporting a nonstandard human interface or data base.

Frank Costa, CFI delegate and vice-president/general manager for Mentor's design and analysis division, inserts a word of caution, however. "We don't believe that, over any reasonable time frame, users will be able to buy a framework and a random set of applications tools and have them work together," he says. "There are too many issues that CFI isn't attempting to address, and too many areas of technology that aren't yet mature enough to make that kind of system possible."

Don't expect short-term results

CFI offers tremendous promise, but it will be several years before any concrete results appear. EDIF began five years ago and just achieved recognition, and that's considered to be fast in some quarters. Because of its greater complexity, CFI could take even longer.

"I hope people don't expect too much too fast," says Mentor's Costa. "The scope of what we're trying to look at goes well beyond what any group of this type has ever tried to look at before. Many of the standards that we're looking at, such as EDIF and VHDL, have taken years to gain recognition. With this in mind, people shouldn't expect the world to change overnight, because such expectations could kill the momentum of the group."

Members of the steering committee include Cadence Design Systems, Digital Equipment Corp, EDA Systems, Hewlett-Packard, Honeywell, Mentor Graphics, Microelectronic and Computer Technology Corp, Motorola and Valid Logic Systems.

The committee must determine what CFI's relationship should be to the Engineering Information System (EIS), a DOD-funded group that's chartered to build a framework. There's considerable overlap between the goals of the two groups. According to Valid's Price, EIS appears to be building a system that it would like to donate to industry as a proposed standard. The existence of EIS may indicate that the DOD was impatient and wasn't sure that industry would come up with an acceptable solution. ■

DATA COMMUNICATIONS

FDDI moves closer to fruition as standard network backbone

Sydney F. Shapiro, Research/Special Projects Manager

Although the recent Enterprise Networking Event in Baltimore was intended to be a showcase for broadband coax factory networking, the conference unexpectedly brought the Fiber Distributed Data Interface (FDDI) into the limelight. Digital Equipment Corp (Littleton, MA) prompted the surprising focus on FDDI by announcing at the conference its plans to back FDDI and by making a public commitment to building FDDI-compliant products for availability in the early 1990s.

FDDI first made a big splash about a year ago when a five-chip silicon implementation was introduced by Advanced Micro Devices (Sunnyvale, CA), but the proposed standard has mostly remained in study mode while Accredited Standards Committee X3T9.5 continues its work to define it. Meanwhile, various companies have evaluated the chip set and the implications of FDDI itself, and have researched how they might implement fiberoptic networks for their own purposes. And ever since DEC initiated recent FDDI discussions,

Advanced Micro Devices is preparing to release a revised Fiber Distributed Data Interface chip set this December, according to Patrick Green, manager of strategic marketing. The new product will contain every sublayer except station management (SMT). But since most of SMT can be done in station software, the revised chip set will be as close as possible to what ANSI is likely to accept.

DATA COMMUNICATIONS

network and computer vendors have suddenly become willing to discuss their plans for implementing the as-yet-unapproved standard.

Need for 100-Mbit/s throughput

Until recently, LANs such as Ethernet, Arcnet and the other commonly used proprietary and semiproprietary versions were adequate for most users' requirements. LAN speeds of 5 or 10 Mbits/s were, and still are, sufficient for most of the predominantly used microcomputers and minicomputers. In other cases, despite the considerably greater stand-alone capabilities of today's small- and medium-sized computers, even a 10-Mbit/s throughput is becoming a drag on system operation. Increasingly, even multiple-Mips workstations are handling such large chunks of data that they often have to offload portions of their tasks to host computers that act as computational centers. It's here that FDDI's 100-Mbit/s throughput is beneficial.

But 100-Mbit/s throughput requires a fundamental change in data-encoding techniques. Ethernet and token-ring networks use Manchester encoding, which requires two signal changes for every bit of information transmitted. A 10-Mbit/s Ethernet would, therefore, really be signaling at 20 MHz. If this encoding method were used with a 100-Mbit/s LAN such as FDDI, the required 200-MHz signaling rate would be prohibitive because it would require costly, specialized chips on every board.

To provide for 100-Mbit/s throughput, FDDI uses 4B5B encoding. Instead of sending two signals for every bit, the 4B5B procedure sends five signals for every four bits of information. Signaling at 125 MHz, therefore, provides 100 Mbits of data.

Initially, there will be three main applications for FDDI: as a high-speed backbone architecture to route communications among many slower LANs, as a direct connection for extremely high-performance workstations, and as an interconnect for high-speed peripherals. All three applications would take advantage of the potential for improved communication for all sizes of networks because of the tenfold increase in throughput rate.

Except for the preliminary AMD chip set, however, there are no FDDI products available today. And even the AMD chip set has been available only to a relatively few beta-site users, who are evaluating the chips and suggesting changes for the next generation of silicon.

Beta-site users include 20 beta-one sites, which are closely coupled to AMD and managed directly from the factory. About 25 more sites are coupled to field-application support. "The beta-one sites in particular have helped debug system problems, have aided in testing the chips and have identified boundary conditions that weren't foreseen," says Patrick Green, manager of strategic marketing at AMD.

Some of these companies claim that they will have FDDI implementations by 1990, while others admit that 1991 or even 1992 are more realistic targets.

Combining Ethernet and FDDI

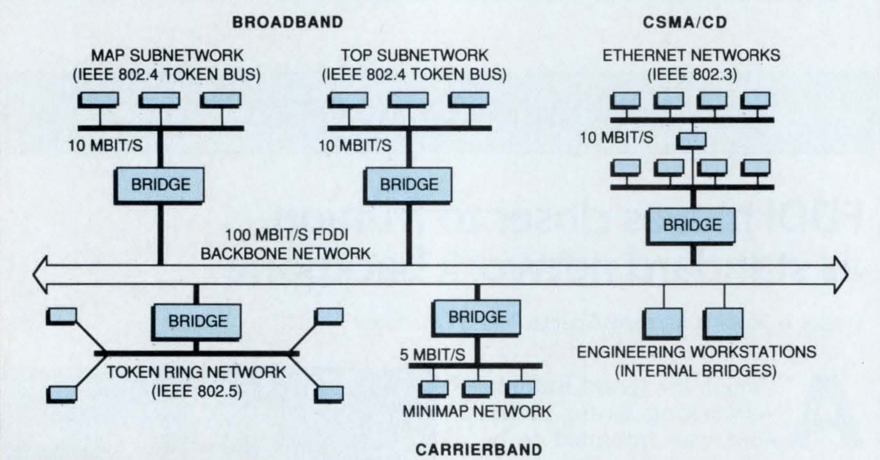
Although DEC announced its commitment to FDDI, the company certainly has no intention of deserting its Ethernet LAN implementation. DEC will continue to back Ethernet and believes that Ethernet will remain as a viable LAN for a long time to come. DEC's plan is to take advantage of FDDI's throughput capabilities by tying several Ethernets to an FDDI backbone network.

"Ethernet is a first-generation network, and its 10-Mbit/s throughput is inadequate for future networking systems," says Karl Pieper, extended LAN marketing manager. Although DEC has no FDDI products yet, the company has been talking about fiberoptics to some interested customers on a nondisclosure basis. "DEC decided that it wasn't sensible to merely double Ethernet's speed," says Pieper. "Even if there were no technology problems, that relatively small increase in throughput speed would require lengthy standards-committee discussions and costly delays before approval. Since such discussions were inevitable anyway, DEC opted for a leap to the 10-times improvement potential of FDDI."

Although the proposed FDDI standard allows up to 500 connections to the backbone, DEC believes that number to be too high for a practical network. If individual loads aren't too great, each Ethernet can support as many as 1,024 workstations or computer subsystems. Even at fewer than the 500-link maximum, FDDI's potential is appealing.

The initial FDDI-compliant prod-

THE FDDI BACKBONE NETWORK



Its 100-Mbit/s throughput will enable the Fiber Distributed Data Interface (FDDI) to serve as the backbone support for many slower speed LANs, such as IEEE-802.3 twisted-pair or coax Ethernet, IEEE-802.5 token ring and IEEE-802.4 broadband coax MAP. Bridges betweeen the slower LANs and the fiberoptic backbone will be external for most applications, but will be built into devices such as larger computer systems.

ucts to emerge from DEC will be bridges to tie Ethernet LANs to the FDDI backbones. Eventually, DEC will build FDDI controller boards into VAX computers, but that will be done only for high-performance systems. Small systems probably couldn't handle FDDI, and DEC sees no reason to include such capability in its smaller VAXes or desktop VAXes when they become available. Some people may simply choose to stay with lower cost LANs such as Ethernet because they believe that the benefits of FDDI aren't worth the cost, according to Pieper.

Other plans for FDDI

Many other computer manufacturers and network specialists are now openly discussing their plans for FDDI. At Ungermann-Bass (Andover, MA), the need for some mechanism to tie LANs together has been created by the move to the use of twisted-pair solutions for LANs, a higher amount of LAN traffic, and an increase in LAN sizes, says Greg Hopkins, vice-president of engineering. He views FDDI as a backbone network to provide that needed tie.

Ethernet and token ring will be the dominant subnetwork architectures, although neither provides the speed necessary for future networks, says Hopkins. Accordingly, there's a need for FDDI-compliant products to serve as data-link mechanisms to let those subnetworks communicate with the FDDI backbone, he adds.

Hewlett-Packard (Roseville, CA) has been a beta site for the AMD FDDI chip set and has built breadboards and other components for the proposed standard, according to Dave Harris, networking division marketing manager. The company is testing protocol chips in both backbone and workstation interface applications.

Apollo Computer (Chelmsford, MA) isn't ready to talk about specific commitments to FDDI. Yet, the company has been very active in FDDI standards committees and has provided strong input to the system-management area of the specification, says Dave McCrabb, senior networking product manager of DEC/LAN communications. "Apollo anticipates being one of the initial vendors with an FDDI implementation, probably with an FDDI bridge built into its workstations," says McCrabb. "Because fiberoptics so readily matches the requirements of technical or workstation environments, FDDI could initiate the replacement of broadband. But it's more likely that manufacturers will retain broadband as a complement to fiberoptics."

Matching LANs to applications

There are two probable directions for LANs over the next four to five years, according to McCrabb. The first is a gradual movement toward twisted pairs as a replacement for Ethernet and token-ring coax cables at slower speeds (between 1 and 15 to 20 Mbits/s). The second is for FDDI to become a corporate backbone to connect many work groups with minicomputers, superminicomputers, mainframe computers and higher performance workstations.

The twisted pair, as envisioned by McCrabb, will interface with the two lower layers (physical and data-link) of the open systems interconnection (OSI) communications model, which is where Ethernet also interfaces. FDDI networks will then interface with the remaining upper five layers, with bridges or gateways from the twisted pair to the fiberoptics.

Prime Computer (Natick, MA) is another company that's "not ready to set a date" for its first FDDI announcement, according to Douglas Hunt, senior technical consultant. But Prime does expect to be an early implementer of FDDI, he says. That should occur, he adds, early in 1989, according to the availability of FDDI chip sets.

"Prime intends to have a complete systems approach both to support Prime platforms and to be sure we can interface with platforms from other suppliers, including attachments between FDDI and other network technologies such as Ethernet," says Hunt. Prime doesn't intend to be all things to all people in its first release, according to Hunt, but that product will serve in many applications because of its very high bandwidth and network management capabilities. Any FDDI products introduced by Prime will offer upward capability from FDDI 1, the presently proposed version of FDDI, to FDDI 2, the next version, and will provide interoperability wherever possible.

FDDI standards not yet approved

Several subcommittees are working toward developing FDDI standards that will be approved by ANSI and the International Standards Organization (ISO), according to Gene Milligan, manager of business and product planning for the small disk-drive division of Control Data (Oklahoma City, OK) and chairman of the X3T9.5 committee.

The X3T9.5 working committee is focusing on four discrete areas or sublayers: physical media dependent (PMD), physical (PHY), media-access controller (MAC) and station management (SMT). PHY is ISO-approved and is about to be ANSI-approved, MAC is ISO-approved and was approved by ANSI about a year ago, and PMD isn't yet ISO-approved, but is out for a second letter ballot for ANSI approval. SMT is the only sublayer on which the committee is still working.

> ***"LANs will get into the gigabit range—so FDDI may be only a temporary stopgap."***
>
> *—Douglas Hunt, Prime Computer*

"AMD won't wait for ANSI or ISO approval of the SMT sublayer and will introduce a revised FDDI chip set without that sublayer," says AMD's Green. "The new product will contain everything except SMT. But since most of SMT can be done in station software, the revised chip set will be as close as possible to what the ANSI group is likely to accept. Minor changes will have to be made later in software to work with other people's equipment. Although beta sampling will begin earlier, a final revision of the modified silicon will be available to ship to all customers in December of this year."

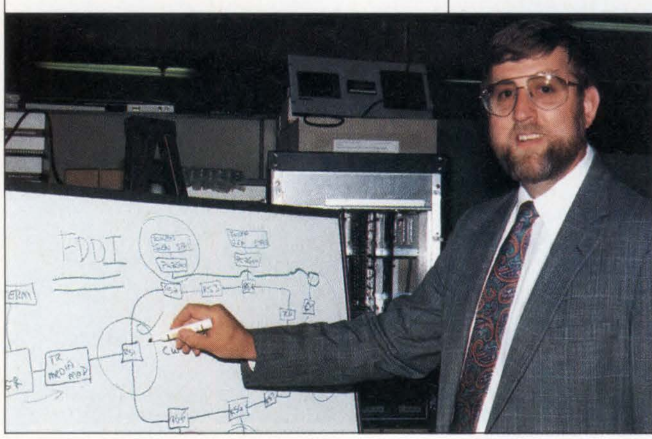
The future of FDDI will depend upon users' needs, particularly if it's to suffice for industrial applications. Projections for the next two to three years indicate that the study committee will have to consider the need for digitized voice, security systems and miscellaneous video, as well as possible specialized capabilities. Although it will be able to handle most current needs, as backbone requirements continue to grow FDDI will soon become inadequate.

Where FDDI is headed

"The presently proposed FDDI 1 standard is basically an asynchronous data standard," says HP's Harris. "Despite its pure, high-performance bandwidth, FDDI 1 has only minor provisions for handling synchronous traffic, such as for digitized voice or video. Such capabilities aren't expected to be fully available until the next version of the standard, FDDI 2, is accepted."

FDDI 1 is optimized for packet data, but it has some capabilities for handling real-time applications, says Control Data's Milligan. FDDI 2, on the other hand, will add a sublayer to change the optimized point from packet data to optimization for real-time applications such as voice, video and process control.

FDDI—both the currently proposed standard and the next version—isn't the ultimate solution. In spite of the seemingly large step up from 10-Mbit/s networks to the 100-Mbit/s FDDI, future users will demand higher performance. "Mips ratings are growing so rapidly that some applications such as those that are graphics-intensive are already demanding every bit of interconnect bandwidth that can be applied," says Prime's Hunt. "I believe that fairly soon, we'll be trying to move toward standardization of LANs getting into the gigabit range—so FDDI may be only a temporary stopgap." ■



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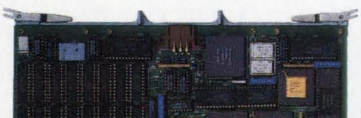

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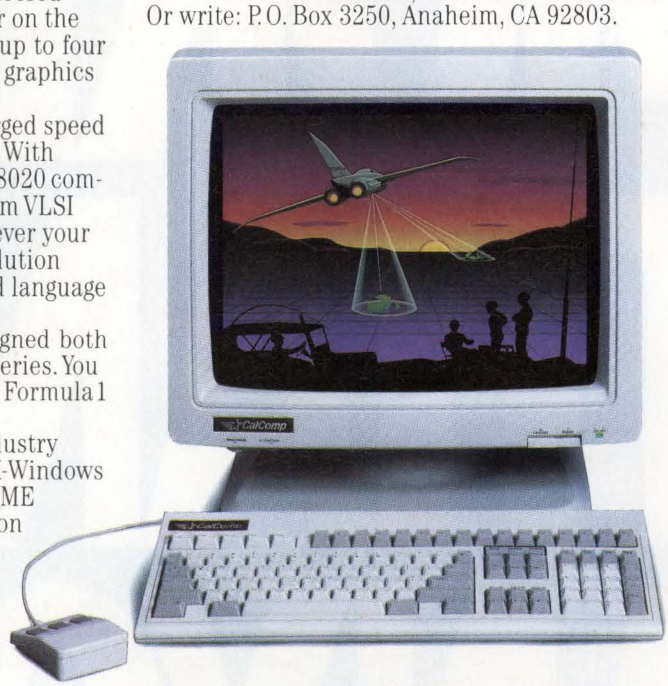

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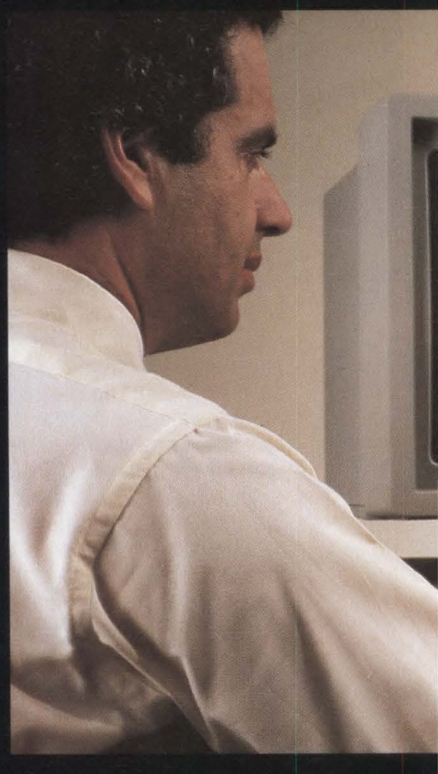

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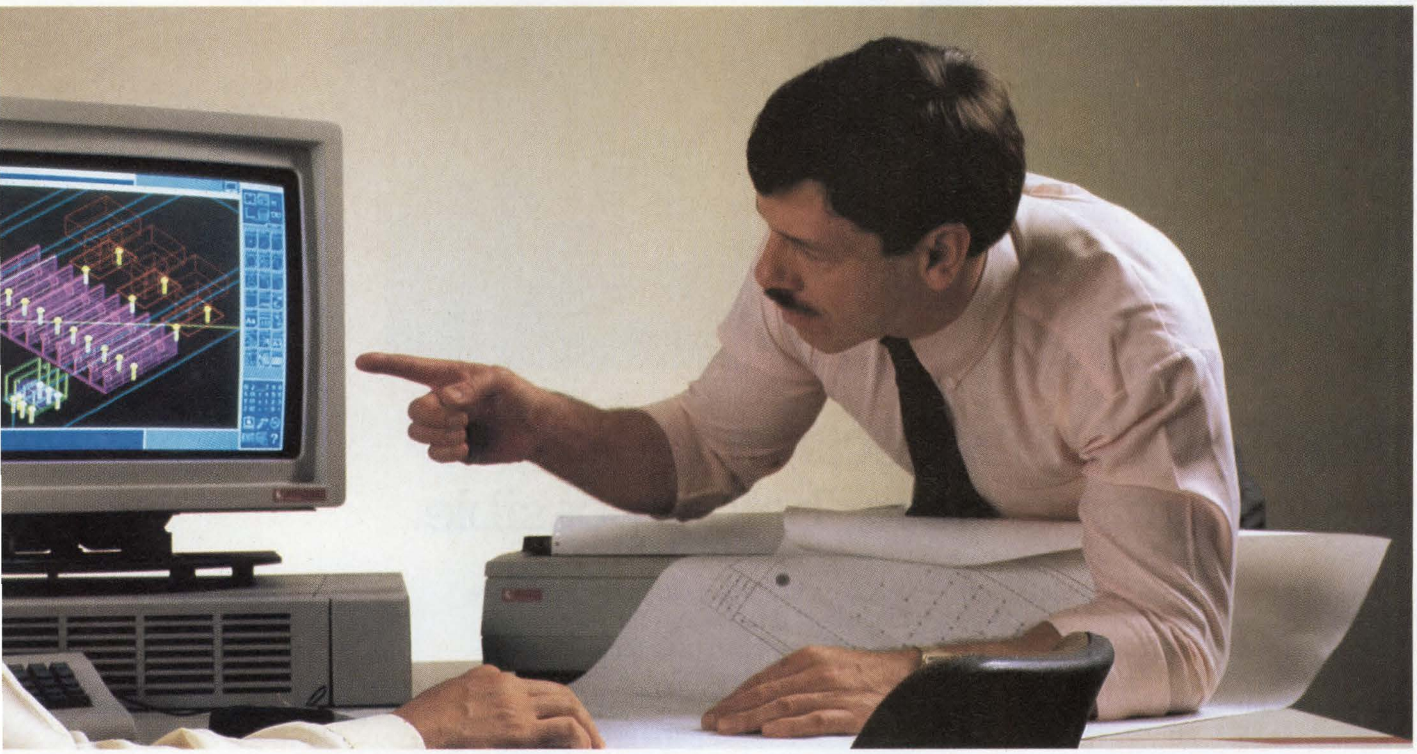

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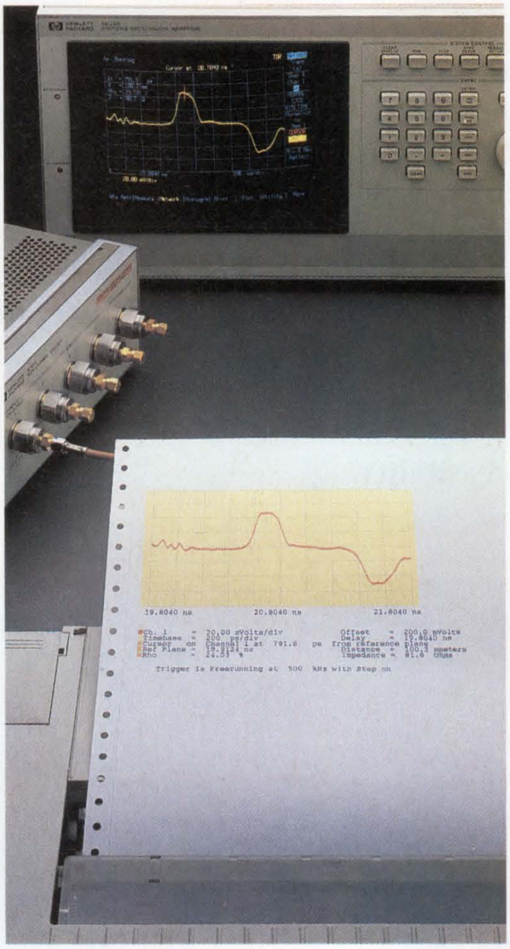

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HEWLETT PACKARD

Prototype testers put ASIC characterization into designers' hands

Functional verification may not be enough for complex ASICs or full-custom ICs. So IC designers are turning to prototype testers to provide accurate characterization data.

Richard Goering
Senior Editor

Paul Gifford (right), manager of systems engineering at Sequent Computer, and Steve Shovoly, engineer responsible for application-specific IC verification and procurement, use a Cadic STM5200 digital VLSI test system for ASIC design verification and characterization. Sequent, like many designers of complex ASICs, has turned to prototype testers because, according to Gifford, a foundry won't tell you how close you are to your operating margins.

First-time designers of application-specific ICs usually aren't concerned about verifying prototypes—they assume the foundry has adequately tested the device. But a growing number of designers of complex ASICs or full-custom ICs not only run their own functional verification, but also characterize IC prototypes over a range of operating parameters.

A functional verification determines whether a prototype works according to the designer's specification. Characterization, on the other hand, looks at the performance limits of the device. Designers might want to know, for example, how power-supply voltage will affect propagation delay, how temperature will affect performance, or how fast an IC will run. Such questions may be critical for determining whether a device will work within a system.

To run a functional verification, designers usually compare logic-simulation results to actual test results. This can be accomplished either with a logic analyzer/pattern generator combination or with a hardware modeler. But if designers want to look at ac or dc parametrics, use programmable power supplies or voltage drive levels, or sample within clock cycles to subnanosecond resolutions, they need either a production test system or a specialized IC prototype tester.

Prototype testers aimed at the engineering environment include the Logic Master family from Integrated Measurement Systems (Beaverton, OR), the Topaz family from Hilevel Technology (Irvine, CA), the Asix-1 from Asix (Fremont, CA), the STM5200 from Cadic (Beaverton, OR) and the HP81810S from Hewlett-Packard (Palo Alto, CA). Used for full-custom ICs, gate arrays and standard cells, these testers have many of the capabilities of $1 million production test systems—yet are priced typically from $50,000 to $350,000.

"If all an engineer wanted to do was functional testing, our class of instrument would be hard to justify," says Norbert Laengrich, vice-president for sales and marketing at Hilevel. "What the engineer is really doing is design characterization. He needs to set up operating margins to verify whether the chip will work in the system. If an ASIC requires a power-supply voltage between 4 and 5 V, he's got to provide that on the board."

Foundries run tests on ASICs before they're released to the customer, but these tests may not provide much information about how the ASIC will function in the system. A foundry test takes the test vectors supplied by the customer, which are usually derived from logic simulation, and runs them to ensure that the device meets the designer's specification. "We can't guarantee that the chip will work at the system level," says Van Lewing, director of marketing for CAE products at LSI Logic (Milpitas, CA).

Some foundries, however, believe they can ultimately predict system-level performance. According to Dan Skilken, software product manager at VLSI Technology (San Jose, CA), this can be accomplished if foundries forge tight links to CAE systems that support system-level simulation. Skilken points to recent library agreements that VLSI Technology has signed with such vendors as Mentor Graphics (Beaverton, OR) and Daisy Systems (Mountain View, CA) as steps in this direction.

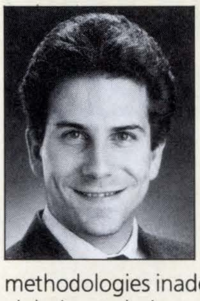
Skilken also argues that VLSI Technology can provide adequate characterization data for ASIC designers. "We characterize our process in advance for the customer, and we can give extremely accurate estimates on how the process parameters will affect propagation delay and various other operating conditions. We feed the parameters into our simulator and double-check each wafer for the same process parameters the customer simulated," he says.

Foundry testing no guarantee

Not all foundries provide the same level of information, and many designers of complex ASICs want more than estimates. "A foundry won't tell you how close you are to your operating margins," says Paul Gifford, manager of systems engineering at Sequent Computer (Beaverton, OR) and a recent purchaser of the Cadic STM5200. "It won't tell you that if you're 1 ns off, you're in trouble."

Western Digital (Irvine, CA) uses production testers to verify prototypes from ASIC foundries and then uses an Integrated Measurement Systems (IMS) Logic Master for a more detailed failure analysis. "Some foundries are better than others," says Winfield Scott, supervisor for device failure analysis. "We do a quality-assurance audit on foundries. If the process is good, we can adjust the frequency of our audits."

Proper test development streamlines ASIC verification



The verification of high-integration application-specific ICs has become a serious problem. The complexity of these designs makes normal test-development methodologies inadequate. Conventional design techniques and test-development procedures often leave designers wondering whether prototype chips will work to design specifications. Uncertainties in both the results of their design efforts and the quality of their prototype test programs are driving designers to find other means to verify their prototypes.

One option, although expensive and time-consuming, is to use a benchtop tester to aid in the development of more effective test programs. Test programs are debugged with the tester after designers receive their prototype parts. But with this option, a chip's production release is often delayed while test engineers work out test program problems. In addition, using a benchtop test for production test development only addresses the symptoms of bad test programs, not the problem of developing the proper test program from the start.

Often, production development schedules dictate that ASICs must move into full production as quickly as prototype parts are qualified. To address this problem, VLSI Technology (San Jose, CA) has taken a different approach to test development. By using the same test programs for full-production and prototype-production tests, prototype parts are better qualified, in less time, and give better information on future production yields for the chip. This doesn't leave time in the test-development process for interactive work to debug test programs on a benchtop tester.

In VLSI Technology's test methodology, the test program is broken down into hierarchical blocks, with automatic test-vector-generation software developing high-fault-coverage component tests for each functional block in a chip. Additional test software ties the complete chip test program back together and screens it for production test requirements. This automated methodology and careful screening have virtually eliminated test-development problems before prototype production, thus eliminating the need for interactive debugging of test programs on a prototype tester.

After receiving a prototype from the factory, some customers may turn to a benchtop tester to verify their design specifications. Again, the focus needs to be on the problem of designing to specification instead of on prototype verification. Advancements in high-level design specification have improved the accuracy of the overall chip specification. System-level design tools have also helped verify these specifications. As these design tools have improved, they have eliminated much of the uncertainty that might otherwise exist in prototype parts.

Customers may also use a benchtop tester to characterize the performance of their chips to the foundry manufacturing process. If a customer is using a stable and well-characterized process, however, the foundry can provide all the performance details needed to develop a working chip. When these performance parameters are integrated into a highly accurate ASIC simulator, they yield detailed measurements of the chip's performance. This lets designers adjust the design to meet performance requirements before the chip is fabricated. The burden of characterizing a design process should remain with ASIC manufacturers—they'll accept responsibility for the chip's performance to simulation predictions.

The focus needs to be on the problem of designing to specification instead of on prototype verification.

■ ■ ■

As the industry improves design specification, system simulation and test-development techniques, it eliminates uncertainties in the performance of prototype and production ASICs. These developments offer a better solution than simply dealing with the symptom of having to debug a low-yielding prototype part on a benchtop tester.

Daniel Skilken, BSCS, Manager, ASIC Product Marketing, VLSI Technology

When ASIC designers decide to do their own prototype verification, the first thing they're likely to do is test the prototype against their own simulation vectors—presumably, the same vectors used by the foundry. But the designer might want to add new vectors that don't come from simulation. "You really want to exercise the part functionally as it will exist in the system," suggests Larry Miles, director of IC development at DSC Communications (Plano, TX) and a Mentor Graphics customer. "That takes millions of vectors, and it's prohibitive to simulate them all."

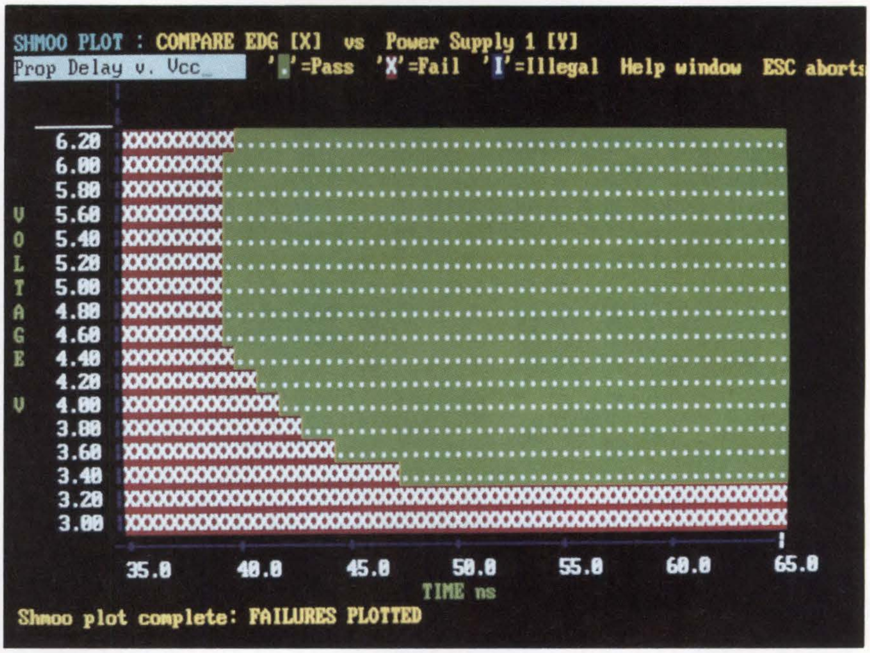
Several tools available

Three types of devices—logic analyzers, hardware modelers and IC prototype testers—can provide a comparison to simulation vectors. Miles uses Mentor's Hardware Verification System, a logic analyzer/pattern generator combination that's no longer sold by Mentor but is still in use by customers. Another logic analyzer/pattern generator combination that can compare simulation data to actual test results is the DAS 9200 from Tektronix (Beaverton, OR).

Although hardware modelers were designed for simulation modeling, they can also be used to stimulate a prototype IC and compare the results to simulation. Over 30 percent of the Daisy PMX hardware modeler users use it for prototype verification, according to Dave Stamm, vice-president at Daisy Systems. "A hardware modeler can do a quick functional verification, but it can't do a timing characterization," he says. "At some point, you've got to ensure that setup and hold specifications are met."

Specialized IC prototype testers like the IMS Logic Master offer an advantage over logic analyzers and hardware modelers because they provide a real-time comparison to simulation results while a test is running. This lets users program conditional instructions into a test. That's a helpful feature for supplying initialization sequences because it provides the capability to run multiple iterations of vectors until the device reaches an initialized state.

Prototype testers also provide programmable timing formats, such as return-to-zero and nonreturn-to-zero, a capability that lets the user control the edge placements of the data presented to a device. That can be important if an IC requires different timing sets on various input pins.



A Shmoo plot, an analysis tool included in prototype testers, lets users plot the interaction of any timing or voltage parameter against any other. A common application of a Shmoo plot is testing power-supply voltage (V_{CC}) against propagation delay, as shown here on the Hilevel Topaz V system.

Measuring ac parametrics

To measure ac parametrics such as setup, hold and propagation delay, IC prototype testers program repetitive tests within clock cycles. Setup time, for example, can be measured by delaying the leading edge of the data in 1-ns or better increments until a failure occurs due to a setup-time violation. Propagation delays can be measured by moving the output-pin sample time toward the start of the cycle until the test fails.

> ***"A hardware modeler can do a quick functional verification, but it can't do a timing characterization."***
>
> *—Dave Stamm, Daisy Systems*

A few logic analyzers can perform this type of measurement, but generally not to the same degree of accuracy as an IC prototype tester. The DAS 9200, for example, can test ac parametrics with a 1-ns edge placement, while the IMS Logic Master XL series and the new Hilevel Topaz V offer 100-ps edge-placement resolution.

When IC prototype testers were first introduced, users had to write short test programs to verify setup, hold or propagation delay. Now vendors of these test systems offer automated measurement capabilities that eliminate such programming. Asix, for example, offers its Analytical Toolset, which provides a timing-edge search for ac parameters. The search function can return a pass/fail report on selected parameters.

Many designers run ac parametric tests on multiple copies of a prototype to determine the range of setup, hold and propagation delay values. If designers are concerned about possible variations in the foundry's process, they might wish to draw samples from multiple foundry lots. "The timing performance of the die seems to change slowly from lot to lot," says Sequent's Gifford. "That's important because we like to select from lots to get the best speeds we can."

To help keep track of runs using multiple samples, several vendors let users develop their own spreadsheets using Lotus 1-2-3. IMS, for example, recently introduced its Characterization and Timing Analysis (CTA) software, which can collect the results of any Logic Master measurement and compile them on a spreadsheet. CTA provides preprogrammed routines for making ac and dc parametric measurements and lets users generate tables, charts and graphs. "In effect, you can create your own data sheet for a device," says Ken Lindsay, director of marketing at IMS.

Parameter plots boost value

One graphical analysis tool that's offered by all vendors of IC prototype testers is Shmoo plotting. A Shmoo plot lets users plot the interaction of any timing or voltage parameter against any other. Users might want to know, for example, how power-supply voltage (V_{cc}) affects propagation delay, how high and low voltage input levels (V_{ih} and V_{il}) impact output thresholds (V_{oh} and V_{ol}), or how fast a chip runs under varying supply voltage or temperature conditions.

Most prototype testers provide programmable power supplies, and because CMOS propagation delays vary with supply voltage, designers often use Shmoo plots to compare these parameters. Other timing parameters can fluctuate with supply voltage as well. "We find out what the range of supply voltage is for every critical ac parameter," says Yung Feng, manager of product testing for digital signal processors at Zoran (Santa Clara, CA) and an IMS Logic Master user. "We vary the clock frequency and find out what the minimum and maximum V_{cc} are."

The ability of the IC prototype tester to vary supply voltage and establish voltage thresholds can yield a lot of information about a device's operating limits. To exploit this capability, Cadic introduced its Voltage-Level Sensitivity Measurement (VLSM) software package, which lets users determine what power-supply levels are necessary to prevent device failure. "As you drop the supply voltage to a given level, the internal gates no longer propagate and you start getting failures," says Garth Eimers, Cadic marketing vice-president.

To use VLSM, the user selects a supply voltage and sets high and low thresholds for voltage inputs or outputs. The user runs a test, and if the sample device passes, the tester moves the threshold voltage until it fails. By programming repetitive tests, the user can deduce a window of operation for each power-supply voltage. The results can be charted on a Shmoo plot or reported in a text file.

A voltage-level search function in the Asix Analytical Toolset offers a similar capability, letting users examine device sensitivity to changing supply voltages and input levels. The toolset includes a lot summary report utility for evaluating multiple prototype runs. "The process is going to affect output voltage levels," says Richard Bullen, Asix marketing director. "If you're running a test with 100 devices, you might want to set up a certain condition on each device and do a level search across the range."

Programmable in many systems on a per-pin basis, variable voltage levels let designers accommodate the various drive levels required by ECL, CMOS, TTL and other technologies. Another capability that may become important is programmable loads, now available on a per-pin basis with the Hilevel Topaz V. A programmable load lets users quickly change the loading on a pin to mimic conditions on a printed circuit board.

Designers look at more than voltage fluctuations, however. Some designers also examine the effects of temperature on device timing and performance. Zoran's Feng, for example, uses a temperature controller from Temptronic (Newton, MA) in conjunction with the IMS Logic Master. Basically a hood that sits on top of the tester, this device provides a stream of temperature-controlled gas from $-70°$ to $+205°$ C. Thus, users can check temperature against ac timing parameters, voltage thresholds or maximum operating speed.

Measuring dc parameters too

Users who want to go even further with characterization can buy a dc parametric measuring unit (PMU), now available from all manufacturers of prototype verification systems. The PMU lets users force voltage and measure current, or force current and measure voltage, through a switching matrix. The switching matrix lets users rapidly connect and disconnect input and output pins without changing the wiring.

A dc PMU can be used for a gross leakage test, which verifies the device's leakage current through the power-supply pin. With this test, major process-related problems can be detected. This test is valuable to both foundries and designers of full-custom ICs. But its worth to ASIC designers is less clear, since they don't control the foundry's process.

But a dc PMU can also help determine whether an IC will work with the circuitry that surrounds it—a concern of ASIC designers. A PMU can measure the load that a device's input pins present to an external circuit, as well as measure the ability of a device's output pins to drive the load presented by an external circuit.

Rockwell International (Cedar Falls, IA) uses a dc PMU to verify gate arrays manufactured by commercial foundries. "We want to determine the characteristics of the gate arrays ourselves," says design engineer James Brown, a user of

REPRESENTATIVE IC PROTOTYPE VERIFICATION SYSTEMS

Vendor	Product	Maximum Test Speed	Channels	Price
IMS	Logic Master XL	60 MHz, 100 MHz	32 to 448 unidirectional	\$53,500 to \$400,000
IMS	Logic Master ST	20 MHz	32 to 190 unidirectional	\$16,800 to \$85,300
Hilevel	Topaz V	110 MHz	32 to 544 I/O	\$70,000 to \$500,000
Hilevel	Topaz FX	30 MHz	16 to 224 I/O	\$20,000 to \$85,000
Cadic	STM5200	25 MHz	32 to 352 I/O	\$42,000 to \$200,000
Asix	Asix-1	50 MHz (multiplexed)	64 to 256 I/O	\$70,000 to \$300,000
Hewlett-Packard	HP81810S	50 MHz	16 to 256 unidirectional	\$60,000 to \$500,000

With 100-MHz chips becoming available, designers are looking for IC prototype testers with higher test speeds. Both Integrated Measurement Systems (IMS) and Hilevel were able to increase test rates without sacrificing channel count. Other vendors, such as Cadic, have chosen to keep costs down and pin counts up.

Verification tool focuses on scan design

When designers use a scan-design methodology to improve the testability of their ICs, verification needs change drastically—and a new test system from Gillytron (San Jose, CA) reflects that change. The Scanmaster DV-6005 handles only circuits that use scan design, and it's intended for engineering verification and low-volume production test.

A scan-design methodology uses serial scan paths, in which latches are connected to form shift registers, to let a tester control and observe all the latches in the circuit. This makes sequential logic appear combinational to the tester.

To provide functional verification, the DV-6005 can shift extremely long test patterns in and out of the serial scan paths. A scan module can place 4 Mbytes of 32-bit-wide patterns behind a designated scan pin, and the system can support up to 1,792 functional I/O pins. This test isn't run at the device's rated speed, and Gillytron doesn't provide a comparison to simulation data, although the company will offer interfaces to simulators in the future.

The DV-6005 provides what's called a ring-oscillator test to verify ac performance characteristics. This test causes the circuit to oscillate at its natural frequency and then calculates the average of the gate delays in the circuit. This lets a designer determine whether a gate will operate properly without having to run it at speed.

A dc parametric testing unit also lets users check leakage current by forcing voltage and measuring current, or forcing current and measuring voltage.

Hilevel's Topaz system. "The specifications from the foundry aren't always adequate. They may give you a sink and source current that's adequate for driving TTL, but you may want to know if you have enough sink and source current to drive other CMOS circuitry."

Faster, wider and deeper

Not all designers are interested in dc parametrics, but most want to find out how fast their device will run. That's one reason why test speeds for IC prototype testers have been increasing. IMS' XL series, for example, introduced late last year, has maximum test speeds of 60 and 100 MHz. "A lot of people are buying 100 MHz because they want to push out the boundaries and see how fast their chip will run," says Dave Parmley, IMS marketing vice-president.

When Hilevel introduced a 110-MHz test rate for its Topaz V system this summer, it wasn't just to show up IMS. "One-hundred-MHz chips are becoming available. If you want to margin test such a chip, the tester must run faster than 100 MHz," says Hilevel's Laengrich. Unlike some systems, neither the Logic Master XL nor the Topaz V test rates require multiplexing, which halves the channel count when speed is doubled.

Cadic, on the other hand, chose to keep costs down and pin counts up. With a maximum test rate of 25 MHz, the STM5200 offers up to 352 I/O (bidirectional) channels. The Asix-1, with a multiplexed 50-MHz test rate, offers 256 I/O channels.

The Topaz V provides up to 544 I/O channels, while the Logic Master XL offers up to 448 unidirectional or 224 I/O channels. The HP 81810S, which is basically an instrument cluster with a data generator and a data analyzer, offers a 50-MHz test rate with up to 256 unidirectional channels.

As ASICs grow in complexity, designers are looking for more memory per channel. "We'd like memory to be deeper, and we'd like to be able to download vectors while testing a device," says Bob Krebs, manager of circuits in VLSI development at CCI Computers (Irvine, CA) and a Hilevel Topaz user. The Topaz V attacks that problem with what Hilevel calls "virtual vector memory," which lets users run long vector sets from an interleaved RAM memory without having to reload from disk.

Per-pin flexibility

To give users more flexibility in making measurements, many prototype testers are offering a per-pin architecture. Pioneered in the prototype verification market by Cadic, a per-pin architecture is now available with the Asix-1, the Hilevel Topaz V and the IMS Logic Master XL series.

None of these testers have a separate timing generator for each pin—the traditional definition of tester-per-pin in the production test world. But timing generators and other resources can be assigned to individual pins, rather than eight-channel groups. In addition to making test programming easier, a per-pin architecture virtually eliminates the need for users to wire connections between the device-under-test and the test fixture.

The per-pin architecture is the latest trend making IC prototype testers look more like $1 million production testers. As designers learn to use prototype test systems, they're using their new machines to take over many of the functions previously relegated to test engineers. That's particularly true as designers characterize their own devices according to timing, voltage and temperature. As a result, designers are gaining a greater understanding about how their ICs will function in the real world. ■

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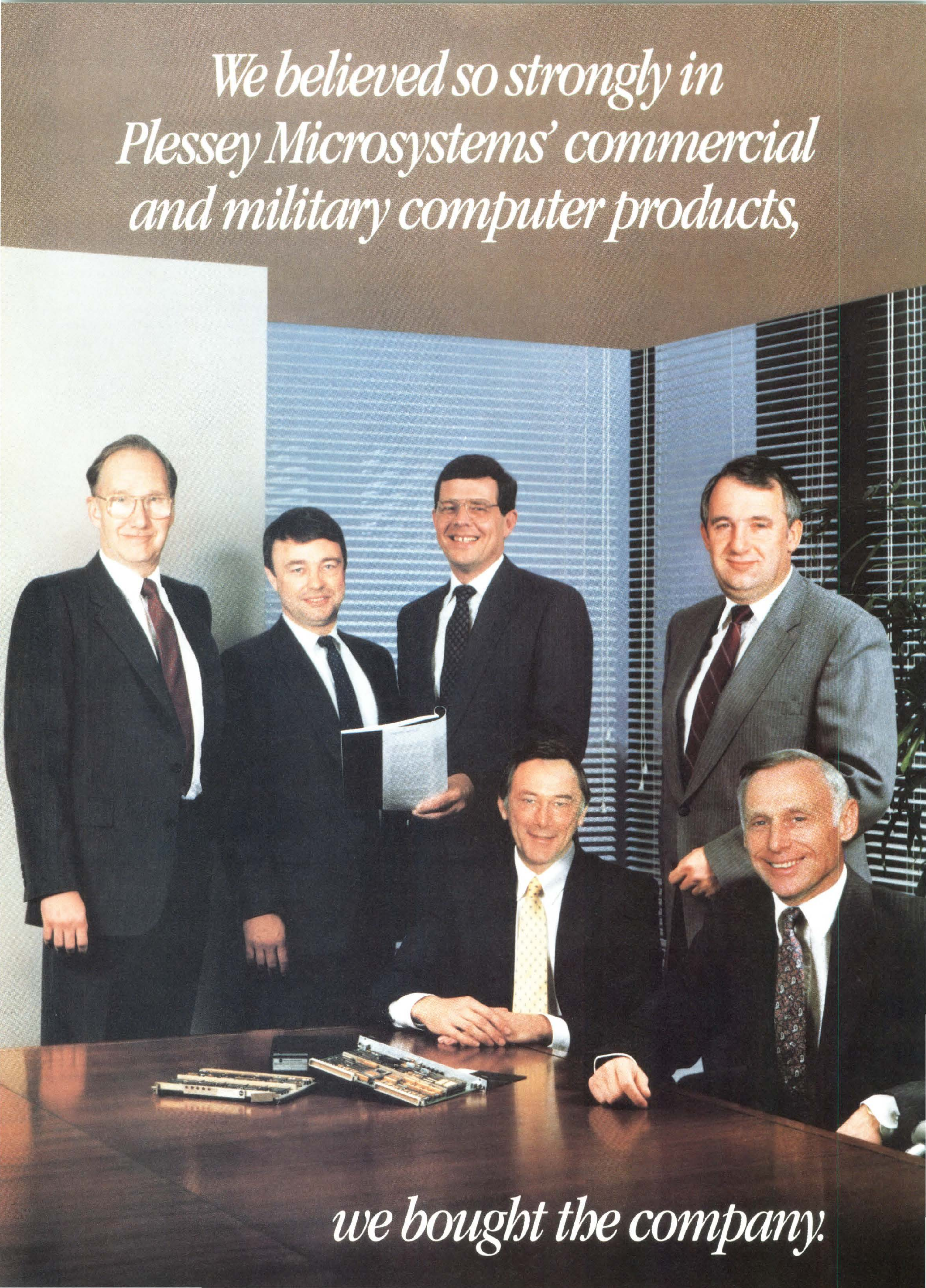
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CIRCLE NO. 21

Designers hone SBCs to utilize full 32-bit power

David Lieberman, Senior Editor

Sophisticated I/O and memory response strategies can mean the difference between a dead-end SBC design and one with the vitality to meet today's processing and system needs.

Gone are the days when the OEM was content to build systems around a "hunk of iron" purchased from a vendor of board-level computers. System integration has become too complex, time-to-market too critical and software costs too high for that approach. Also, the days when the potential user of single-board computers (SBCs) could afford to hand alternative boards over to a junior hardware engineer for comparative evaluation are rapidly receding. Increasingly these days, board evaluators are looking more closely at system-oriented hooks, bells and whistles—those seemingly finicky architectural details that can spell the difference between a dead-end design and one that can grow to meet future requirements. Increasingly, too, SBC selection is being driven by software support, and the choice among alternatives is becoming ever more heavily skewed toward application support.

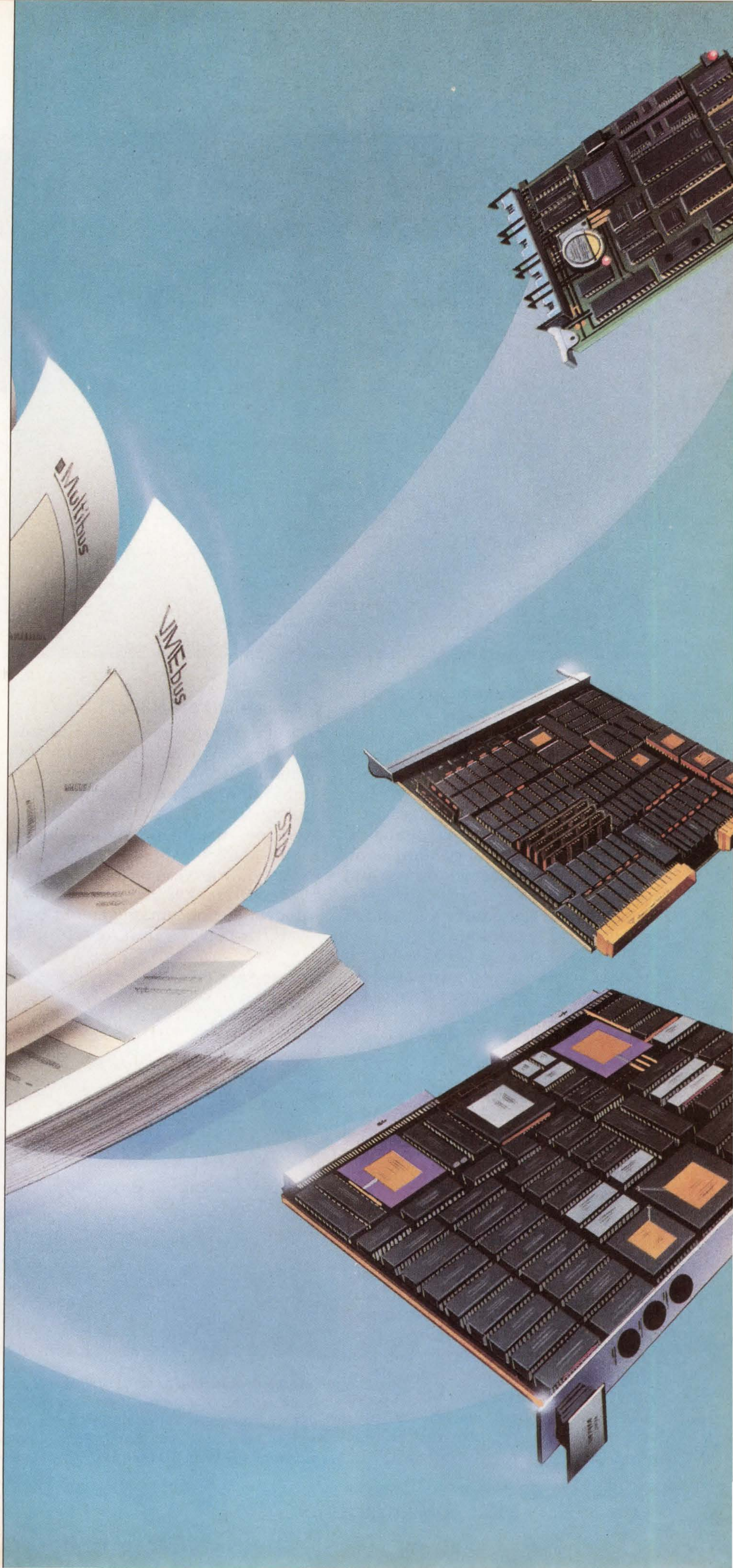
The activity in SBCs today is, if not chaotic, at least extremely energetic. This year, the "bus wars" of the past have given way to bus mania, with a slew of new buses, enhanced buses, extended buses and auxiliary bus schemes. Then there's processor mania. Whereas a year or so ago, there were only about four 32-bit microprocessors in serious contention for high-end Unix systems, for example, the choices today for the same level of performance have about tripled. Add to this the industry contention and fragmentation over Unix System V, Version 4—which was to be the "unified Unix"—and over real-time software standards for the VMEbus, and the chaos seems to propagate.

High-end SBCs most active

The most dynamic segment of the SBC world this year was at the high end. There were a lot of firsts at the heart of the boards: their 32-bit microprocessors. The year began, continued and ended with a slew of new Motorola 68030-based SBC designs, for example, which are helping to raise the baseline definition of high-end microcomputing. VMEbus SBCs based on the 68030 appeared from American Eltec (Pasadena, CA), Force Computers (Campbell, CA), Dual Systems (Hayward, CA), Integrated Solutions (San Jose, CA), Micro Industries (Westerville, OH), Mizar (Carrollton, TX), Motorola's Microcomputer Division (Tempe, AZ), Pacific Microcomputers (San Diego, CA) and Radstone Technology (Pearl River, NY).

Omnibyte (West Chicago, IL) is putting a 68030 on a Multibus SBC this year, and Synergy Microsystems (Encinitas, CA) has done the same, adding to it a 32-bit bus-extension technique called Multibus Plus. A 68020 showed up on an SBC from GW Three (Springfield, VA) that's touted to be the first "complete" 32-bit SBC for the STD Bus—by virtue, in part, of its 32-bit internal path to both dynamic RAM and floating-point coprocessor.

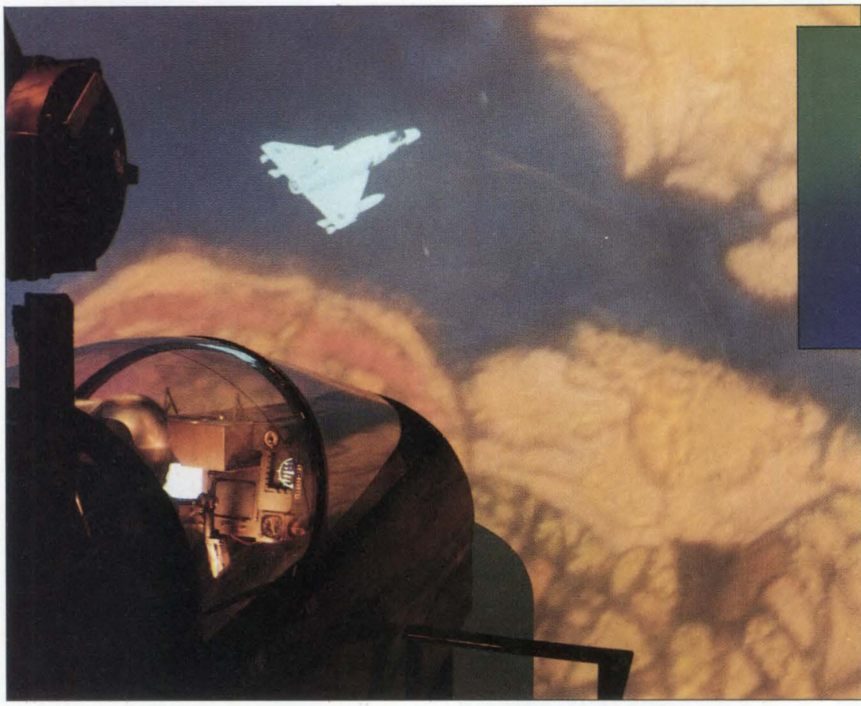
The year also saw the Intel 80386 designed into Multibus SBCs from Central Data (Champaign, IL) and Concurrent Technologies (Laguna Hills, CA), and into an 8- to 23-slot PC AT-compatible STD system from Computer Dynamics (Greer, SC). Heurikon (Madison, WI) and Xycom (Saline, MI) took on their first microprocessors from National Semiconductor (Santa Clara, CA) this year, building VMEbus SBCs with the 32532 and the 32332, respectively. The depth and breadth of National software support played a major role in Heurikon's decision to develop a family of products around a National core, says Clarence Peckham, director of engineering at the company. Heurikon also introduced 68030 SBCs for both Multibus and VMEbus this year.



This year, the "bus wars" of the past have given way to bus mania, with a slew of new boards, new buses and bus schemes. Cover by Sergio Roffo.

All this processing muscle may result in a lot of design headaches, but the problems can also present opportunities for creative solutions. "The most striking phenomena in SBCs are the dramatic growth in processor performance and the adverse effect that growth can have on other attributes of a system architecture," says Richard Billig, director of the Series 32000 value-added program at National Semiconductor. "Some people tend to focus on just the processor and completely ignore the I/O requirements of an application," he explains. "That's a problem because processor technology is ramping up at such a steep angle and SBCs are demanding substantially more I/O than in the past to create a balanced system."

In addition to increasing I/O requirements, the movement to a higher performance, higher speed microprocessor also puts dramatically greater demands on CPU-to-memory bandwidth, and there's no expectation that processor technology is going to slow its advance while interface technology races to keep up. "Within five years, digital technology is going to drop down from 5 V to 3 or 3.3 V as today's 1-micron technology becomes the ½-micron technology of the 1990s," says Wayne



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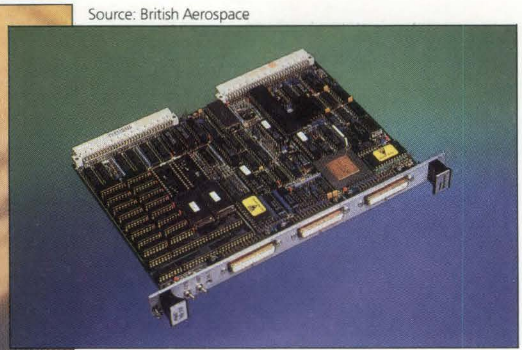

Today's leading-edge multiprocessing applications, such as this British Aerospace cockpit flight-simulation system based on Radstone Technology single-board computers, require both processing power and balanced I/O and memory access to achieve the speed that's required for a high degree of realism.

Fischer, director of marketing at Force.

So how do SBC designers keep the pipelines full, the current-technology processors busy, and time-critical traffic off the main system bus these days? In other words, how do they keep the monster fed? "Black art," the designers say, which seems to mostly include memory-addressing "tricks" and hierarchies, caches and cache hierarchies, coprocessor interfaces, a little brute force and a lot of intelligent program massage.

The 68030's ability to run out of internal caches—limiting the need for frequent off-chip memory accesses—represents a tremendous improvement over the 68020, and its cache burst-fill capability makes accesses to on-board memory more efficient, according to Joel Silverman, marketing manager for commercial products at Radstone (formerly Plessey Microsystems). "This makes the on-board memory more accessible over the system bus," he says, "and it's an ideal situation to efficiently implement true dual-port RAM."

As Silverman explains, when an SBC's "dual-access" RAM is accessed from the bus, the 68030 locks its internal bus and idles. With dual-port RAM, "The SBC has separate logic that serves as a traffic cop between the local bus and the VMEbus. If another board accesses the SBC's memory, the 68030 can still be running out of EPROM or internal caches—it doesn't have to sit and wait."

■ A hierarchy of MMUs

One of the most common architectural wrinkles in balanced, high-performance SBCs is the memory hierarchy; hierarchical arrangements among other system elements are, however, also being implemented. Like other 68030-based products, for example, one version of Synergy's SM31 SBC makes use of the 68030's integral memory-management unit (MMU) when it's in a low- to mid-range application. For high-end multiuser, multiprocessing and real-time applications that require frequent switching between large numbers of processors, however, another version of the board can bypass the on-chip MMU and take a more "brute force" approach: routing the task to an enhanced version of the Stanford University MMU (often referred to as the Sun MMU).

With its 256-Mbyte address range, storage for 64,000 descriptors and support for multiple contexts, the Sun MMU avoids the considerable overhead that MMUs based on descriptor caches incur during cache misses and process or context

"Some people tend to focus on just the processor and completely ignore the I/O requirements of an application," says Richard Billig, director of the Series 32000 value-added program at National Semiconductor. This concentration on processor performance causes a problem, according to Billig, because single-board computers are demanding substantially more I/O than in the past to create a balanced system.

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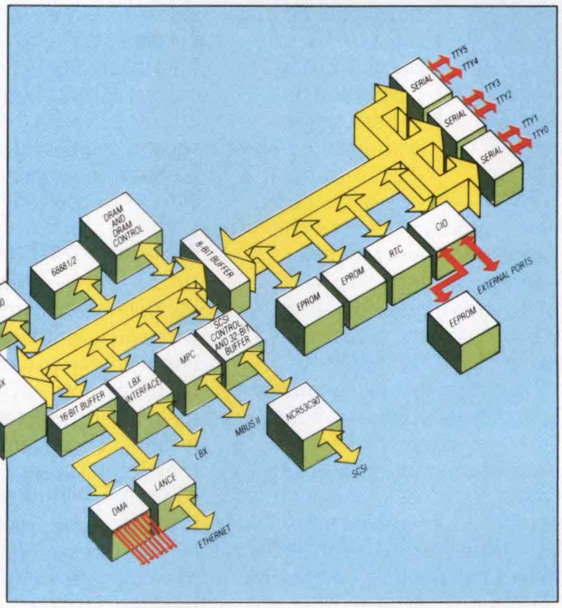
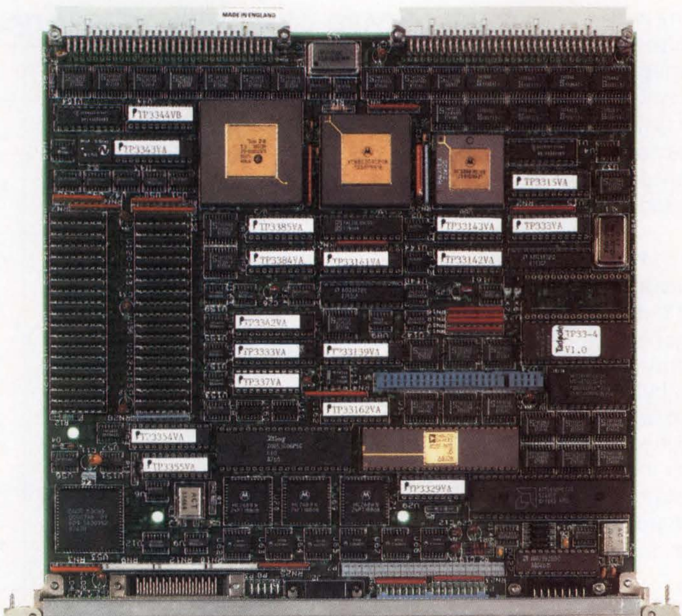
- NCR 53C90 DMA-driven synchronous or asynchronous SCSI interface
- AMD Lance IEEE 802.3 Ethernet with DMA
- 6 x RS232 ports
- Multibus II/iSBX/iLBX II interfaces
- Battery backed-up real time clock
- 2Kb SRAM • 256Kb EPROM
- TP-IX V.3.1* • VRTX
- VRTX - TP-IX* communications software
- Intel transport layer protocol drivers

CIRCLE NO. 22

•The Design•



• The Evidence•



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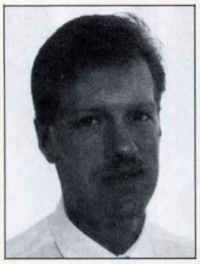
T A D P O L E

Unix performance merits extra design effort in SBC implementations



The basic functions required to run a Unix application can be implemented on either a single-board computer (SBC) or a multiple-board computer. Though each approach has its niche, the SBC approach offers a superior price/performance ratio for certain classes of systems by incorporating memory and I/O functions that would otherwise reside on additional bus boards. The system software required for SBCs, however, is typically more difficult to develop than that for multiple-board computers because an SBC is a more complete system with relatively unintelligent device interfaces. Also, since the CPU on an SBC is doing the work that would be done by several intelligent controllers on a multiple-board computer, performance tuning and balancing under load is especially important when configuring an SBC-based system.

Multiple-board computers are well suited for large systems, multiuser systems, or systems with high throughput and heavy loads. But for small systems, single- or few-user systems, or systems that have light loads, an SBC can be a better choice. The SBC also provides a good engine for workstations and embedded systems.

Regardless of which type of computer is used, the minimal hardware requirements for running one of today's Unix derivatives begin with a general-purpose CPU and a paged memory-management unit. At least 4 Mbytes of dynamic RAM is recommended for small systems, and 8 to 16 Mbytes can be put to good use. A tick timer that can generate a 60- to 100-Hz system clock is also required, as are a hard disk interface and at least one serial port for the system console.

Beyond this bare minimum, an interface to streamer tape and/or high-density floppy disk is needed for hard disk backup and software transport, and additional serial ports are necessary to add users, printers and low-speed intermachine communications. Also, since the introduction of Unix System V Release 3.0, networking hardware has become a de facto requirement for a full-featured Unix system. Often, applications will also need the performance afforded by a floating-point coprocessor and, increasingly, a graphics interface able to support the X Window System is expected.

■ SBC has performance edge

An SBC can be at least as fast as a multiple-board computer implemented with equivalent technology. It involves less overhead to use the on-board internal buses of an SBC to access specific memory and mass storage and communications subsystems than it does to use the external buses of a multiple-board computer, with all their generic protocols, to access diverse memory and I/O subsystems. Typically, too, an SBC has a more powerful processing engine than the intelligent peripheral controllers it replaces, and the engine can perform I/O operations more quickly. Considering this performance edge and the fact that the price of an SBC is usually significantly less than that of a multiple-board computer, the SBC offers a better price/performance ratio for small systems.

By providing more of the computer system's functionality on a single board, SBC-based systems can fit into smaller enclosures than multiple-board computer-based systems can. This makes the SBC route very attractive to OEMs and VARs who need a general-purpose engine for their custom boxes. In industrial-automation applications, for example, an SBC can often provide all the basic functionality required in a factory machine and can communicate with other machines in the factory or office.

The multiple-board computer route is usually the appropriate solution in systems for which expandability is an important requirement. With the backplane and external bus structure of a multiple-board computer, the system can easily support additions of memory,

SINGLE-BOARD COMPUTERS VS. MULTIPLE-BOARD COMPUTERS

	Single-board computers	Multiple-board computers
Chassis size	May be quite small	Large chassis required
Backplane	Required only with external bus interface (nonexpandable)	Multiple slots required
VAR/OEM applications	Easily built into custom boxes Good workstation engine	Not easily embedded Highly configurable
Performance	One CPU has entire work load For light loads and/or fewer users, performance may be better than multiple-board computer	Intelligent controllers share work load Superior performance for heavy loads and/or many users
On-board vs. off-board features	On-board memory and peripheral access is fast	Off-board memory and controller access is slower
Cost	Under $10,000 Less waste in small system Price/performance ratio better for small system	$20,000 to $80,000 Costs more for equivalent functionality Price/performance ratio better for large, multiuser system

David L. Barker, BSCS, system software development manager, Motorola Microcomputer Division

mass storage and communications controllers, and even processors. Application-specific boards can also be added.

System software considerations

Unix system software can be viewed as a core kernel, I/O drivers and networking software. Since the SBC is an entire system, it usually requires a full set of new drivers. When the hardware architecture of the SBC permits, however (as with the Motorola MVME147 SBC, for example), the system may make use of some previously developed drivers—making the first kernel for an SBC no more difficult to generate than a kernel for any other new CPU board. The first Unix kernel for a new SBC-based design typically includes some CPU-specific code, a new console driver and a new clock driver, which are merged with existing disk, tape and communications board drivers and the common kernel code. To support the onboard devices, new I/O subsystem and networking drivers later replace the drivers for external devices.

Whether on an SBC or on individual peripheral boards in a multiple-board computer, I/O and networking subsystems are often implemented using the small computer system interface (SCSI) and Ethernet, respectively. SCSI satisfies the Unix system requirements for an I/O subsystem. It provides hard disk, streaming tape and floppy disk interfaces on one chip as well as additional capabilities and expandability.

SCSI provides a technology-independent, upgradable I/O-subsystem standard that consumes a minimum amount of board space. SCSI can support up to seven SCSI devices, or controllers, on a ribbon-cable bus, with each device able to support up to eight peripherals, for a total of 56 peripherals. But since most SCSI peripherals have embedded SCSI controllers, the number of peripherals that can be configured on one SCSI is most often limited to seven. Since the SCSI can extend to 6 m, SCSI devices can reside outside of the SBC enclosure.

SCSI's technology independence simplifies the task of upgrading an I/O subsystem. As new and faster devices are developed, SCSI will support them without any hardware modifications to the SBC. At most, a software modification is all that's required to support a new device. SCSI not only supports mass-storage devices—both direct access (disk) and sequential access (tape)—but also processor output (printer) and processor input (scanner) devices. And a single SCSI chip and DMA controller can support multiple classes of devices. With the support of a microprocessor, SCSI can also be used to implement an inexpensive very local area network.

With its 5-Mbyte/s data rate, SCSI is fast enough to handle the SBC mass-storage devices of today and tomorrow. The fastest SCSI disks and ESDI (Enhanced Small Device Interface) disks can transfer data in the range of 2 Mbytes/s. There's also a strong movement throughout the mass-storage marketplace to SCSI. Most of the new mass-storage devices—3½-in. hard disks, optical disks and helical-scan digital tapes and so forth—have SCSI.

With its 5-Mbyte/s data rate, SCSI is fast enough to handle the SBC mass-storage devices of today and tomorrow.

Since SCSI is a non-time-critical interface, a SCSI interrupt can wait indefinitely to be serviced if the processor is busy with a higher priority task. Other interfaces—ESDI, serial communications and LAN, for example—must service interrupts in a specific amount of time to prevent data loss. SCSI can be put at an interrupt priority lower than these time-critical devices because there's no danger of data loss if SCSI interrupts aren't processed in a certain amount of time.

A SCSI chip on-board an SBC most often provides a relatively unintelligent interface when compared to a dedicated SCSI host adapter board. Typically, an adapter has its own processor and firmware that provide a high-level interface for a Unix driver. Some SCSI host adapters abstract the SCSI device interface, providing a consistent interface to the Unix driver for every supported SCSI device type, thus letting the same driver support a variety of peripherals.

Since the on-board SCSI chip doesn't provide this degree of functionality, the Unix driver must interface to the SCSI chip with low-level commands and actually drive the SCSI chip. The driver must also be written to support specific SCSI devices. The result is a complicated device-specific driver and a long debugging process. Some of this burden can be alleviated by including firmware on the SBC to control the SCSI chip. As with the dedicated host adapter approach, the on-board firmware can provide a high-level interface to the Unix driver and drive the SCSI chip.

Ethernet more time-critical

Unix also requires networking hardware capable of supporting remote file sharing, and Ethernet, with its 10-Mbit/s data rate, meets this requirement. Like the SCSI chip, an Ethernet LAN controller chip—such as AMD's AM7990 or Mostek's MK 68590-Lance chip—provides a relatively low-level interface, requiring device-specific code in the lowest layer of the network software.

Unlike SCSI, however, the Ethernet interface must be serviced within time constraints; otherwise, data can be lost or data packets may require retransmission, thus reducing system performance. The Ethernet chip support must therefore be written to handle the time-critical functions within an interrupt routine at an appropriate priority level. If a system developer wants to make the network driver support additional off-board network device options as well as the on-board LAN device, the driver becomes even more complex.

Also like the low-level SCSI, some of the LAN chip support can be put in firmware. However, it's usually more advantageous to use RAM-based code, as long as a local boot device such as disk or tape is available. The RAM is generally cheaper than ROM, PROM or EPROM, and RAM-based code is easier to maintain, especially code as complex as network software. However, if a developer wants to use an SBC as a diskless Unix node on a network and must boot over the network, some LAN chip support might be required. Even in this case, the ROM-based support may be so primitive that it would only be used to boot the system and would be replaced by RAM-based code.

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CIRCLE NO. 23

Application, not CPU, should drive design choices

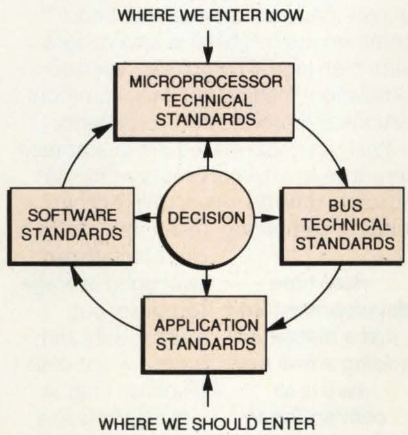
"Humans are taxonomic creatures," says Ray Alderman, vice-president at Matrix (Raleigh, NC). With that in mind, Alderman constructed a graphical model (see figure) to put some of today's major design decisions in perspective. As Alderman sees it, skewing the first-order design decision toward microprocessor standards is a dangerous habit and one that's quickly falling out of favor.

Alderman suggests that decisions have been skewed toward processors because the technical community is bombarded with technology standards from the semiconductor manufacturers. "The result of this is a nasty phenomenon called the sacrificial order," he says. "By accepting a set of microprocessor standards, we also accept limited alternatives to buses, applications and software methodology."

Alderman believes that skewing the decision toward bus standards is "precarious," since the battle over buses can degenerate into "emotional issues disguised as technical points." As he sees it, the bus structures created by semiconductor manufacturers are "the evangelists of their CPU standards and the hardware timing interface to their peripheral I/O chips.

"If you make your decision based on bus specifications alone, you will by default accept some restrictions on software standards," says Alderman. "If you adopt Multibus II, for example, you will code interrupt handling very differently than you would for a VME-bus system. If you choose a multiprocessor bus, your new software standard will be structured programming with segmented code.

"Let's talk about application standards instead," Alderman suggests. "What is the customer's ultimate goal? If he's Chrysler and he's going to build a comprehensive quality control data base, then the right data base is the key to the success of the project. The most sophisticated and capable data bases today run Unix, which also has all the required tools, networking and utilities, so that's decided. The next step is to study the microprocessor standards and match them to your software standards, and then decide on the bus structure or platform you feel is most appropriate for the application based on the CPU standard that you want."

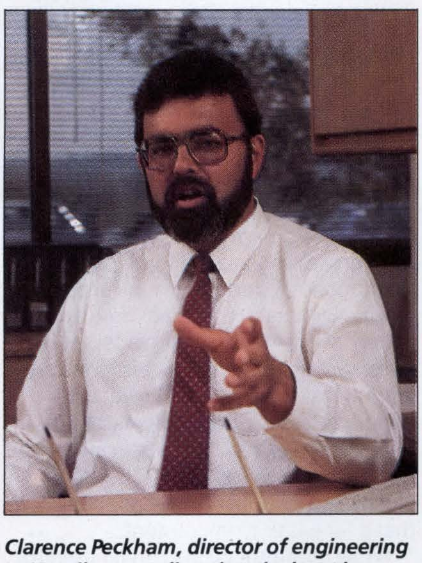


Entering the decision model at the applications standards level, Alderman concludes, avoids surprises and brick walls when it comes time to implement a system. "Study the applications pending now, evaluate how they might expand and where they might evolve in the near future," he says.

"Consider all the possibilities of I/O expansion in the system and gain a good understanding of the business problems to be solved," explains Alderman. "Decide if central processing or distributed processing is more advantageous. Look very hard at communications and networking to see if they'll be needed. Evaluate packaging, space requirements, environmental factors and budget estimates. Then go straight out and study software standards. Resist the urge to evaluate microprocessors. Why? Because a system's software costs can be as much as five times the hardware costs."

switches, according to Stan Skowronski, president of Synergy. "If there's a cache miss and the MMU doesn't have enough descriptors to describe an entire address space, the memory access cycle is put on hold for a retry while the MMU goes through the descriptor tables in main memory. Walking a descriptor tree can take as much time as two to 100 memory accesses, while the CPU just sits there and waits," Skowronski explains. As for switching overhead, Skowronski says, "The problem with most MMUs is that since the cache tags typically don't have context numbers for cache entries, all the cache entries are suddenly invalid when the CPU changes the process or context."

The trade-off of the Sun MMU approach, Skowronski admits, is that it's not a VLSI solution. The Sun approach requires "about 10 small, surface-mount chips." On the other hand, all descriptors are instantly available in very fast local memory, so it's possible to switch processes or contexts within a single CPU cycle.

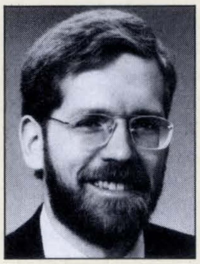


Clarence Peckham, director of engineering at Heurikon, predicts that the board vendors that survive into the 1990s will be the ones who provide a system solution, offering a real-time executive with drivers and all the development tools.

The SM31 is noteworthy on another front: the Multibus Plus extension, which pushes data transfers to 32 bits wide and memory addressing to 256 Mbytes, while adding a burst-transfer methodology that claims bus-transfer rates in the range of 32 Mbytes/s. (Multibus has a theoretical maximum limit of 10 Mbytes/s, but typical boards have a transfer rate of somewhere between 4 and 7 Mbytes/s.)

Novel memory architectures are at the heart of many of the newer high-performance designs. An integral part of the Synergy SBC's burst mode, for example, is the use of nibble-mode RAM chips, which, says Skowronski, "can get out a new piece of data every 40 ns." At Apollo Computer (Chelmsford, MA), a new 4500 desktop workstation gets optimal price/performance from its 68030 de-

Real-time computing demands new tools, methods and designs



Within the next few years, the shape of real-time computing will change dramatically. Single-board computers based on industry-standard bus structures will capture more of the real-time market, both as low-cost alternatives to minicomputer-based systems and as strategic upgrades for applications that have grown too complex for microcontrollers and embedded microprocessors.

Multibus and Q-bus will show continued strength in real-time markets, primarily because of the availability of excellent real-time software support. Over time, multiprocessing will play an increasingly important role in real-time systems, and proprietary real-time Unix operating systems will give way to "hybrid" operating system implementations that link standard Unix with dedicated real-time system software. Coming years will also see Multibus II and the IBM PC AT bus capture significant real-time market share—the former because of its sophistication and support for multiprocessing and hybrid operating systems, and the latter because of the appearance of real-time operating system support and its low entry costs.

A company's success in these emerging real-time markets will depend on its ability to understand and deliver the requisite performance for real-time computing. The design considerations for building real-time systems differ from those of other systems, and designers need to be reeducated in design concepts and methodologies. Real-time development isn't just a matter of adding a few new twists to conventional development practice; it represents a different way of thinking. In addition, standard development tools and test procedures are inadequate for real-time system design.

■ Defining real time

Real-time systems are appropriate for almost every computer application where a machine is controlled or monitored, ranging from home appliances to factory automation. Microcontrollers generally represent the low-functionality, low-cost end of the real-time market. The high end of the real-time computing arena is served by single-board computers (SBCs) and real-time systems. Many real-time systems are minicomputer-based, but these are rapidly being replaced by lower cost bus-based SBCs and microcomputers. While SBCs are appropriate for all types of real-time applications, their most common use has been in applications with high logical complexity, such as simulation, medical, military, communications and process-control systems.

Real-time systems require guaranteed response to external events within an absolute time deadline. Unlike other kinds of computing, real-time systems can't be satisfied with good average response, but must specify and meet a worst-case response time. A late response in a real-time environment is useless and can even be dangerous. If a sensor monitoring a robot signals dangerous movement, for example, the computer system must stop the dangerous movement within a limited time frame. Here, a late response could result in destruction of property or even human injury.

Real-time development isn't just a matter of adding a few new twists to conventional development practice; it represents a different way of thinking.

■ ■ ■

In the real world, many different agents are acting simultaneously on many different tasks, so multiprocessing is a natural part of real-time computing. The primary reason for using multiprocessing in a real-time implementation is to reduce its logical complexity. By breaking the real-time application into parts, each with a separate set of system resources, the interaction among tasks is greatly reduced. With additional sets of system resources, a highly complex real-time application can be structured as several low-complexity applications—an architecture that's far easier to implement.

While multiprocessing can be used to increase real-time performance, the requirements of real-time multiprocessing differ from those of multiprocessing in other computer applications. Multiprocessing implementations dynamically allocate the next job to the first available processor. But this is unacceptable for real-time applications, which need to know where the job will run so that they can know when the job will run and how long it will take to execute. Without this information, it becomes impossible to know when the system will respond to an outside event. Real-time multiprocessing is thus typically static: a job is set to always run on a particular processor within a fixed execution time.

■ Complexity dictates software

The logical complexity of a real-time application provides a key to the most appropriate solution for that application. In a real-time system, logical complexity increases with an increase in the number of tasks, as well as with an increase in the amount of interaction among those tasks.

Most applications with three or fewer tasks are low-complexity real-time applications. Those with more than three tasks may also be low complexity if there's little between-task interaction. The appropriate software solution for low-complexity applications is to use a synchronous mechanism, such as a large polling loop or a cyclic scheduler. This type of software is normally written from scratch by the system designer and provides very high performance.

Applications with between three and seven tasks are usually medium-complexity real-time applications. These applications are generally event-driven and, therefore, call for an asynchronous software solution. The appropriate software for these applications is usually a commercially available real-time kernel or the nucleus of a real-time operating system.

Applications with over seven tasks are normally considered high-complexity real-time applications. These applications are also generally event-driven, and they have a significant level of interaction among tasks. High-complexity applications may also be hybrid systems with both real-time and nonreal-time functions. The most appropriate soft-

Tom Willis, software product marketing manager, Intel/OEM Modular Systems Operation

ware for these applications is an object-oriented real-time operating system.

Seven tasks may not seem like a large number of tasks to programmers used to working with Unix or Unix-like interactive systems. The need to specify worst-case response times, however, requires the explicit consideration of many details that can be safely ignored in systems that only seek to provide good average response. The consideration of these extra details rapidly increases complexity.

Developing applications

Since real-time applications specify worst-case response times, the design team developing real-time systems must become familiar with the techniques that make worst-case response possible. These techniques fall into four broad areas: real-time problem analysis, design, implementation and evaluation.

Real-time problem analysis using traditional data-flow-oriented techniques hasn't been successful. The defining of a graphical modeling language by Paul Ward and Steven Mellor in 1985 in *Structured Development for Real-Time Systems*, however, represented a significant step forward in real-time analysis. This graphical language, which extended data-flow techniques to explicitly consider events and control, has been implemented by Index Technology (Cambridge, MA) in a PC-based tool called Excelerator RTS.

Although the real-time problem analysis arena is still relatively immature, a good start has been made with Ward and Mellor's work. We can expect the Ward/Mellor language to be enhanced and modified over time, new real-time graphical languages to appear and, eventually, front-end analysis tools to be fully integrated with tools for design, implementation and analysis.

In addition to learning about problem analysis, the designer of real-time systems must become familiar with a new set of design habits and system facilities. Unlike a time-shared system, a real-time system requires that the highest priority task runs when necessary, without disturbance and until completion. This preemptive priority-based scheduling, however, allocates only CPU time, not the other system resources required to run the task, such as memory, I/O devices or shared code. If a lower priority task controls any of the required resources, the highest priority task can't run, even if it's been allocated the CPU. The best-case result is that you can't guarantee worst-case response time or, hence, deliver real-time response. The worst-case scenario is deadlock or complete system failure.

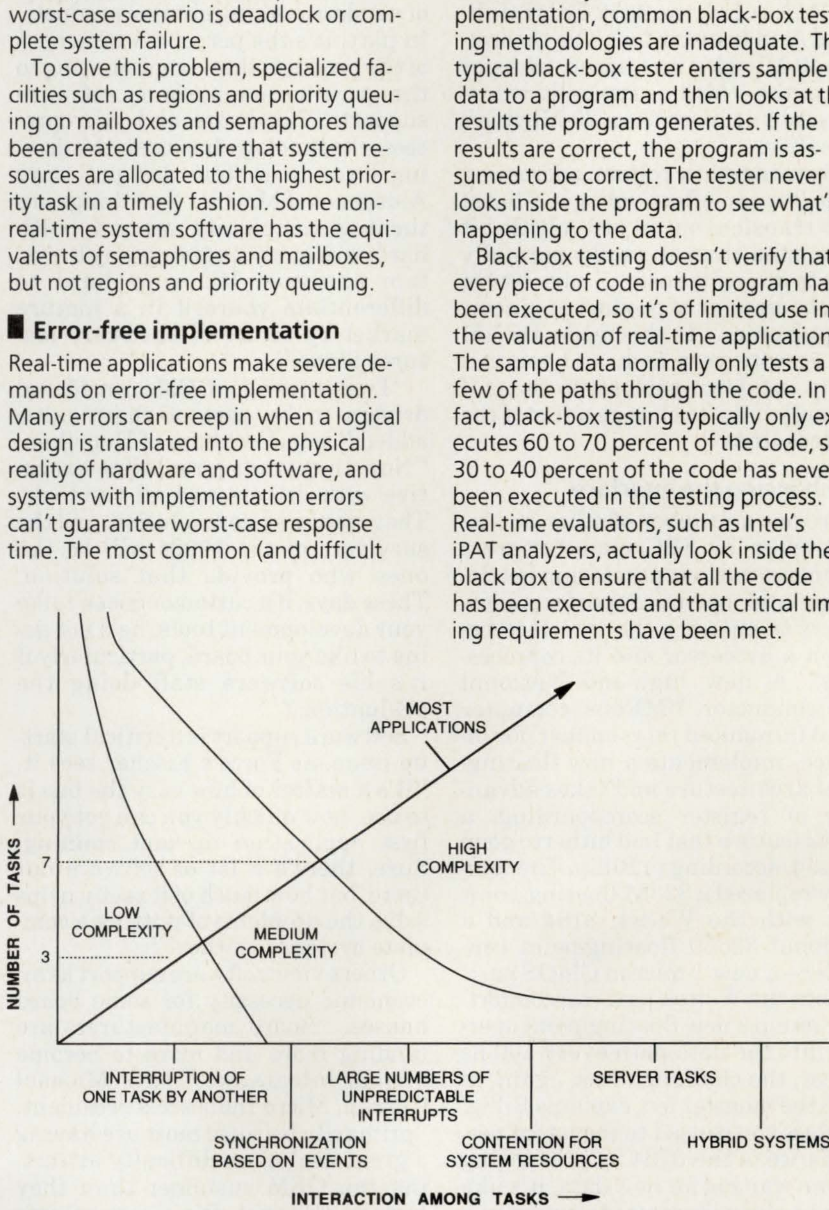
To solve this problem, specialized facilities such as regions and priority queuing on mailboxes and semaphores have been created to ensure that system resources are allocated to the highest priority task in a timely fashion. Some non-real-time system software has the equivalents of semaphores and mailboxes, but not regions and priority queuing.

Error-free implementation

Real-time applications make severe demands on error-free implementation. Many errors can creep in when a logical design is translated into the physical reality of hardware and software, and systems with implementation errors can't guarantee worst-case response time. The most common (and difficult to find) real-time implementation problem is the accidental memory overwrite. Memory segment protection, which for many engineers is only an academic theory, is essential for the reliable implementation of complex real-time applications.

Because of the more stringent need of real-time systems for error-free implementation, common black-box testing methodologies are inadequate. The typical black-box tester enters sample data to a program and then looks at the results the program generates. If the results are correct, the program is assumed to be correct. The tester never looks inside the program to see what's happening to the data.

Black-box testing doesn't verify that every piece of code in the program has been executed, so it's of limited use in the evaluation of real-time applications. The sample data normally only tests a few of the paths through the code. In fact, black-box testing typically only executes 60 to 70 percent of the code, so 30 to 40 percent of the code has never been executed in the testing process. Real-time evaluators, such as Intel's iPAT analyzers, actually look inside the black box to ensure that all the code has been executed and that critical timing requirements have been met.



The complexity of a real-time application and, thus, of an appropriate software strategy depends on both the number of tasks involved and the amount of intertask interaction.

sign by using interleaved memory and a 64-kbyte external cache, according to Cheryl Vedoe, director of workstation products at the company. And at Ironics (Ithaca, NY), the use of static column RAM is at the heart of the high-speed DMA capability added to a pair of 68020-based VME SBCs this year.

Ironics' SCBLT (static column block transfer) capability, according to the company, lets the IV-3201A and IV-3204A SBCs accept data at 30 Mbytes/s over the bus from an Ironics DMA board, the 3272 FSDT (full-speed data transporter). The theoretical 40-Mbyte/s maximum transfer rate of the VMEbus typically translates into no more than 20 Mbytes/s in reality.

"By using static column addressing mode, we can effectively get a burst of 16 transfers out in just a little bit more time than it would normally take to do one transfer," says Kevin Lynch, director of product engineering at Ironics. "In this mode, DRAM can operate very fast, and you can really cut down your setup times if you only have to change a few of the address lines."

Enhancing the interface

There are a number of other strategies taken by SBC manufacturers to remove various processing bottlenecks and optimize performance. One is to enhance the interface between a processor and its coprocessor(s). A new high-end National Semiconductor VMEbus computer board introduced this summer, for instance, implements a new floating-point architecture and takes advantage of register scoreboarding, a 32532 feature that had hitherto gone unused, according to Billig. The company replaced a 32381 floating-point unit with the Weitek 3164 and a National 32580 floating-point controller—a new 1-micron CMOS part.

Since the Weitek part can comfortably pump a new floating-point operand into the data path every 100 ns or less, the challenge was, again, to keep the monster fed, explains Billig. "Unless you can get to the latent performance of the 3164 by preventing it from waiting for new data, it's like using a sledgehammer to pound in a finishing nail," Billig says.

The design's interface to the Weitek chip uses a five-stage instruction pipeline and a 20-stage data pipeline so the monster never goes hungry; when it's finished one operation, it will find its next instruction decoded and its next operands fetched. Register scoreboarding keeps the Weitek chip operating concurrently with the main processor. "Compilers can figure out which instructions depend on the results of other instructions, find the overlap, and organize the instructions to optimize pipelining and concurrency," says Billig.

Need for software support

The enormous popularity of the VMEbus has attracted an abundance of vendors making similar products. In part, it's the perceived sameness of the products that's contributing to the growing emphasis on software support. "Hardware and microprocessor technology has been the driving force in system design," says Alderman of Matrix, "but things are turning completely around, with hardware analysis giving way to system analysis. It's very hard to differentiate yourself in a mature market by virtue of hardware features alone."

"Two years ago, OEMs considered drivers to be part of their value added," says Peckham of Heurikon. "Now they want a real-time executive with drivers and all the tools. They want a system solution, and the survivors of the 1990s will be the ones who provide that solution. These days, if a customer doesn't like your development tools, he's not going to like your board, particularly if it's his software staff doing the evaluation."

Software support is a critical start-up issue, as Force's Fischer sees it. "It's a matter of how easy the bus is to use, how quickly you can get your first application up and running. Sure, there's a lot of software out there, but how much of it really helps solve the problems of putting a complete system together?"

Others view software support as an economic necessity for some board houses. "Board manufacturers are tending more and more to become system integrators," says Michael Curran, Micro Industries president, "primarily because most are having a great deal more difficulty attracting the OEM customer than they have in the past. It's a cost/volume issue. As a result, many board houses haven't been able to establish a market for their new generation of products without that extra step."

National's Billig conditionally admits that software issues are dominant in SBC evaluation today. "It's true to the extent that people are using more sophisticated software tools in a broader set of applications now," he says. "When you're talking, let's say, about a board-level Unix engine, some of the same selection criteria that apply to choosing a complete computer system at the software level will also begin to apply to choosing an SBC. Here, we see people looking at what's really important to their application—overall delivered system performance—as opposed to single numbers like Dhrystones, Whetstones and Mips." ■

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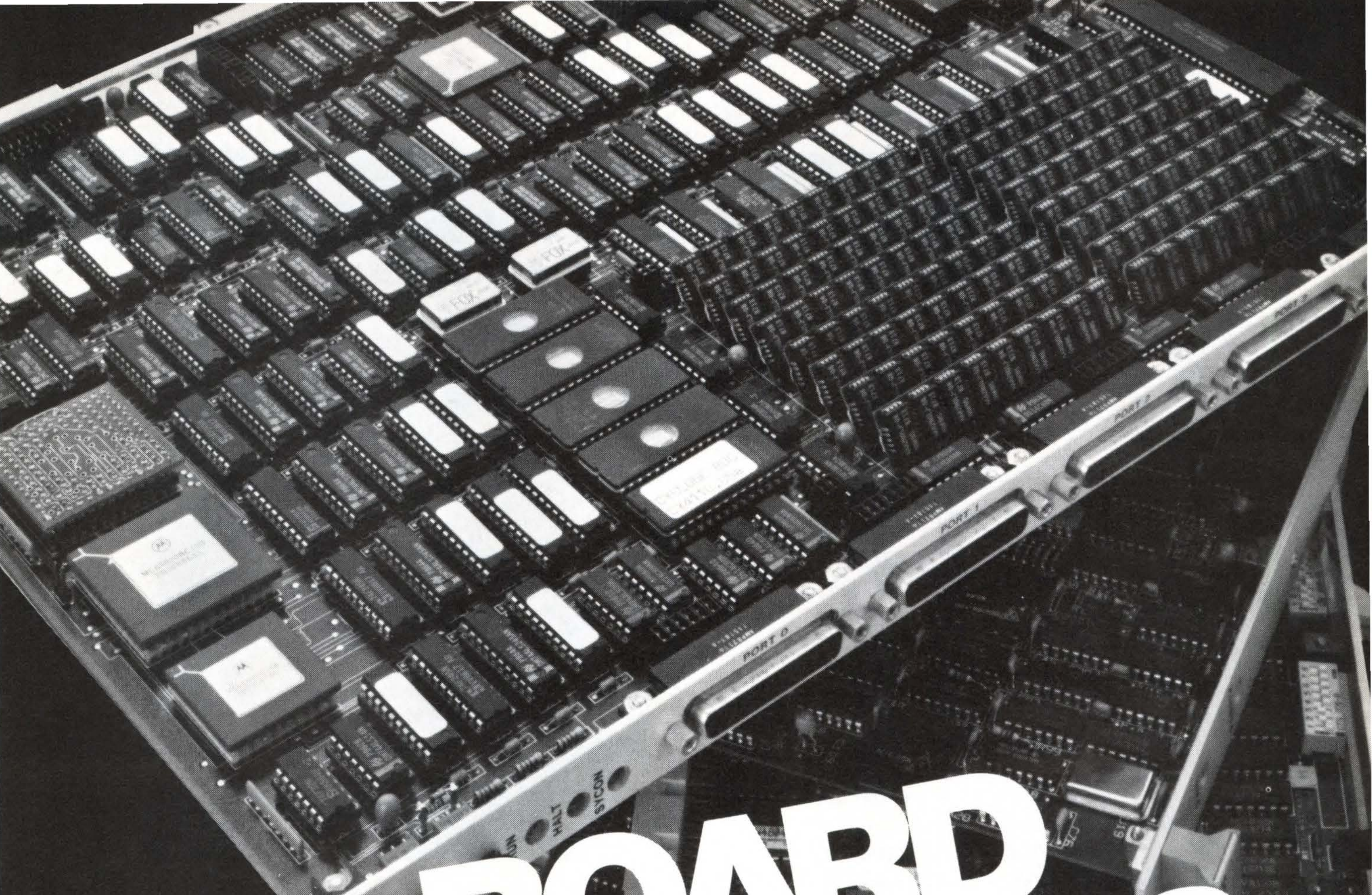

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•The Specification•

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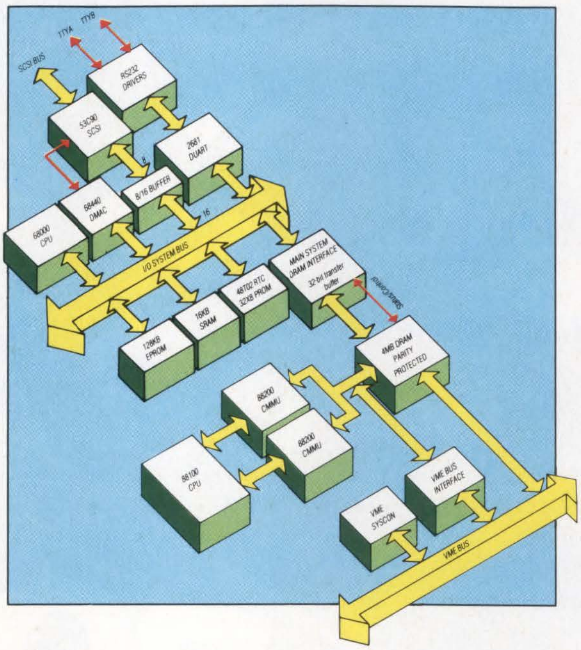
•The Design•



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T A D P O L E

DESIGNERS' BUYING GUIDE

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
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V3/50	8, 16, 32	24, 32	68020	12.5, 16.7	std	opt	1 8-bit	40	0/4M	0/2M	3×6U
V20	8, 16, 32	32	68020	16.7, 20	no	opt	none	—	0	0/1.5M	6U
V15	8, 16, 32	24	68000	12.5	no	no	1 16-bit	40	0	192k	6U
American Eltec 569 S Marengo Ave, Pasadena, CA 91101 (818) 449-1558											**Circle 310**
VME-AT	8, 16	24	80286	10	—	opt	—	—	1M	—	6U
IBAM	8, 16	24	68010	10	—	—	—	—	512k	64k/2M	6U
Eurocom 4	8, 16, 32	24, 32	68010	12	opt	opt	—	—	1M/4M	0	6U
Eurocom 5	8, 16, 32	24, 32	68020	16, 20, 25	opt	opt	—	—	1M/4M	0	6U
Eurocom 6	8, 16, 32	24, 32	68030	20, 25, 33	opt	opt	—	—	4M/8M	0	6U
SAC-7	8, 16	24	68070	10	std	—	2 16-bit	—	0	128k/2M	3U/6U
Cyclone Microsystems 25 Science Park, New Haven, CT 06511 (203) 786-5536											**Circle 338**
CY4110	8, 16, 32	16, 24, 32	68020	12.5, 16.7, 20	opt	opt	2	30	1M/16M	0	9U× 280 mm
CY4180	8, 16, 32	16, 24, 32	68020	16.7, 20, 25	—	opt	2	30	1M/16M	0	9U× 280 mm
CY4380	8, 16, 32	16, 24, 32	68030	20, 25, 30	—	opt	4 32-bit	30	2M/64M	0	9U× 280 mm
Dual Systems 3906 Trust Way, Hayward, CA 94545 (415) 785-8890											**Circle 348**
VMPU 4M	8, 16, 32	24, 32	68020	16	std	opt	—	20	4M	0	6U
VMPU SBC/16	8, 16, 32	24, 32	68030	16	std	opt	—	30	1, 2 or 4M	—	6U
VMPU SBC/25	8, 16, 32	24, 32	68030	25	std	opt	—	30	1, 2 or 4M	—	6U
DY-4 Systems 21 Credit Union Way, Nepean, Ontario, Canada, K2H 9G1 (613) 596-9911											**Circle 340**
DMV-154	8, 16, 32	16, 24, 32	68020	16	—	std	—	—	512k	—	6U
DVME-137	8, 16, 32	16, 24, 32	68020	16.7, 20, 25	—	opt	—	—	4M	—	6U
DVME-138	8, 16, 32	16, 24, 32	68030	25	—	std	—	—	4M/8M	—	6U
DVME-140	8, 16, 32	16, 24, 32	68020	16.7, 20	—	std	—	—	2M/8M	—	6U
Electronic Modular Systems 1325 Capital Pkwy, Carrollton, TX 75006 (214) 446-2900											**Circle 349**
CPU-1	8, 16	16, 24	68000/10	8	std	—	none	10	256k	0	6U
CPU-2RT	8, 16	16, 24	68000/10	8, 10, 12.5	—	—	4 16-bit	10	128k/ 512k	0	6U
CPU-2SC	8, 16	16, 24	68000/10	8, 10, 12.5	—	—	4 16-bit	10	128k/ 512k	0	6U

Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Real-time executive	Intrpt handler/gen levels	Debug monitor	Mailbox interrupts	Slave functions	Read-modify-write cycles	Dynamic bus sizing	System control functions	OEM price (in 100s)
none	2 RS232C, 1 MIL-STD-1553B	none	VSB	Unix	VRTX	7/0	•		•	•	•	•	—
none	1 RS232C/422	none	VSB	none	VRTX, pSOS, OS-9	7/0	•		•	•	•	•	—
1 16-bit	2 RS232C	none	VME	none	MTDS/UX	7/0	•		•	•			—
—	1 RS232, 1 keyboard	—	—	DOS	—	7/0		•	•	•	•	•	$1,720
2 printer opt	1 (18 opt)	yes	VSB	PDOS, OS-9, others	PDOS, OS-9	7/7	•	•	•	•	•	•	$1,224
—	2 RS232	—	—	PDOS, OS-9, Unix 5.3, VersaDOS	PDOS, OS-9	7/1	•	•	•	•	•	•	$1,600
opt	2 RS232 (8 opt)	1 32-bit	VSB	same as above	same as above	7/1	•	•	•	•	•	•	$1,990
opt	2 RS232 (8 opt)	1 32-bit	VSB	same as above	same as above	7/1	•	•	•	•	•	•	$3,180
—	3 RS232	—	—	same as above	same as above	7/1	•		•	•	•	•	$420
1 printer	4 RS232	—	—	PDOS, OS-9	PDOS, OS-9	18/7	•		•	•	•	•	$4,210
1 printer	4 RS232	—	VSB	PDOS, OS-9	PDOS, OS-9	18/7	•		•	•	•	•	$4,510
1 printer	4 RS232	1 8-bit	VSB	PDOS, OS-9	PDOS, OS-9	23/7	•	•	•	•	•	•	$4,980
none	none	none	—	Unix 5.2 pSOS 68k	pSOS	7/0	•	•	•	•	•	•	$3,990
—	2 RS232A/423	—	—	same as above	pSOS	7/0	•	•	•	•	•	•	$1,800 to $3,600
—	2 RS232A/423	—	—	same as above	pSOS	7/0	•	•	•	•	•	•	$2,400 to $4,200
—	1 TTL	—	—	—	harmony	7	•	•		•			—
—	2 RS232C	—	VSB	—	harmony	7	•	•	•	•			—
—	2 RS232C	—	VSB	Unix 5.2	harmony	7	•	•	•	•			—
—	2 RS232/422	—	—	—	—	7	•	•	•	•			—
1 printer	1 RS232	—	—	Unix 5.0	none	7/0				•			$1,200
1 printer	2 RS232	—	—	—	PDOS 3.2, pSOS	7/1	•	•	•	•			$1,430
—	4 RS232/ 4 RS422	—	—	—	pDOS 3.2 pSOS	7/1	•	•	•	•			$1,430

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- 2-channel, 400 megasample/s digitizing scope module (8 channels maximum)
- 50 Mbit/s pattern generator module (204 channels maximum)
- 16-channel, 1 GHz timing analyzer module (80 channels maximum)

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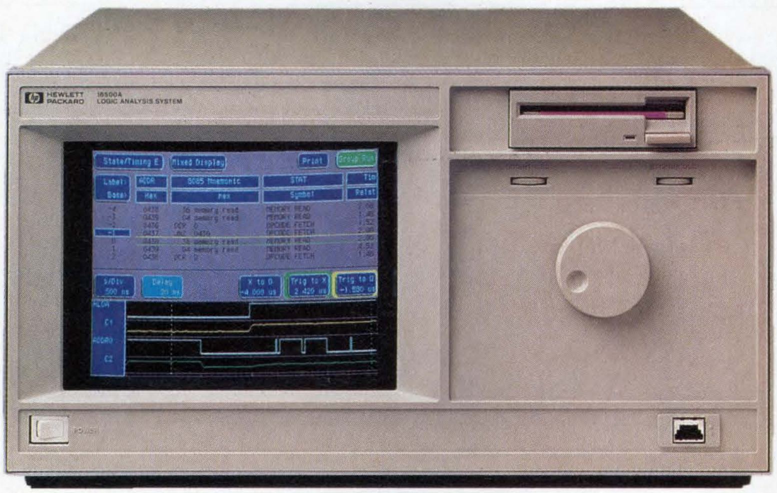

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Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
Electronic Modular Systems 1325 Capital Pkwy, Carrollton, TX 75006 (214) 446-2900 **Circle 349**											
CPU-2P6	8, 16	16, 24	68000/10	8, 10, 12.5	—	opt	4 16-bit	10	512k	0	6U
CPU-3	8, 16	16, 24	68000/10	8, 10, 12.5	1 std, 1 opt	opt	—	10	2M	0	6U
CPU-4RT	8, 16, 32	16, 24, 32	68020	12.5, 16.7, 20	—	opt	—	25	256k/4M	0	6U
CPU-4SC	8, 16, 32	16, 24, 32	68020	12.5, 16.7, 20	—	opt	—	25	256k/4M	0	6U
CPU-4QS	8, 16, 32	16, 24, 32	68020	12.5, 16.7, 20	—	opt	—	25	256k/4M	0	6U
CPU4-SX	8, 16, 32	16, 24, 32	68020	12.5, 16.7, 20	—	opt	—	25	256k/4M	0	6U
CPU-5RT	8, 16, 32	24, 32	86386	16, 20	std	opt	8 32-bit	25	2M	0	6U
Force Computers 3165 Winchester Blvd, Campbell, CA 95008 (408) 370-6300 **Circle 353**											
CPU-2	8, 16	16, 24	68000/10	10	—	—	—	4	—	512k/1M	6U
CPU-3	8, 16	16, 24	68010	10	std	—	—	4	—	128k/ 128k	6U
CPU-4	8, 16	16, 24	68010	12.5	—	—	—	4	—	128k/ 128k	6U
CPU-5	8, 16	16, 24	68000/10	12.5, 16.7	—	—	—	4	—	128k/ 128k	6U
CPU-6	8, 16	16, 24	68000/10	12.5	—	opt	—	6	512k/ 512k	—	6U
CPU-21	8, 16, 24, 32	16, 24, 32	68020	12.5 to 25	—	std	—	20	—	512k/4M	6U
CPU-22	8, 16, 24, 32	16, 24, 32	68020	12.5 to 25	—	std	—	30	1M/4M	0/32k	6U
CPU-25	8, 16, 24, 32	16, 24, 32	68020	12.5 to 25	std	std	—	20	—	512k/4M	6U
CPU-29	8, 16, 24, 32	16, 24, 32	68020	12.5 to 30	—	std	—	20	—	1M/1M	6U
CPU-30	8, 16, 24, 32	16, 24, 32	68030	12.5 to 25	in CPU	std	2 32-bit	30	1M/4M	0/32k	6U
CPU-31	8, 16, 24, 32	16, 24, 32	68030	12.5 to 25	in CPU	std	2 32-bit	30	—	256k/1M	6U
CPU-32	8, 16, 24, 32	16, 24, 32	68030	12.5 to 30	in CPU	std	—	20	—	1M/1M	6U
CPU-37	8, 16, 24, 32	16, 24, 32	68030	12.5 to 30	in CPU	opt	—	20	1M/4M	—	6U
CPU-386	8, 16, 24, 32	16, 24, 32	80386	16	in CPU	opt	—	20	2M/8M	—	6U
CPU-26	8, 16, 24, 32	16, 24, 32	68020	12.5 to 25	—	std	2 32-bit	30	1M/4M	0/32k	6U
General Micro Systems 4700 Brooks St, Montclair, CA 91763 (714) 625-5475 **Circle 358**											
GMSV06	8, 16	24	68010 (68020 opt)	10, 12.5, 16	no	opt	4 8-bit	20	512k/2M	0/0	6U
GMSV16	8, 16	24	68010 (68020 opt)	10, 12.5, 16	no	opt	4 8-bit	20	4M/8M	0	6U
GMSV07	8, 16, 32	32	68020	16, 20, 25	no	opt	1 32-bit opt	30	0/4M	128k/1M	6U
GMSV17	8, 16, 32	32	68030	20, 25, 33	std	opt	1 32-bit opt	35	0/4M	128k/1M	6U

Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Real-time executive	Intrpt handler/gen levels	Debug monitor	Mailbox interrupts	Slave functions	Read-modify-write cycles	Dynamic bus sizing	System control functions	OEM price (in 100s)
										Optional features			
—	2 RS232 opt	opt	—	—	PDOS 3.2, pSOS	7/1	•	•	•	•			$1,456
—	1 RS232	—	—	Unix 5.2	pSOS	7/1	•		•	•			$2,973
1 16-bit	2 RS232	—	—	—	PDOS, pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$1,500
—	3 RS232	—	—	—	PDOS, pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$1,500
—	4 RS232	—	—	—	PDOS, pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$1,500
—	2 RS232	—	—	—	PDOS, pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$1,500
—	2 RS232/ RS422	—	—	Unix 5.3, MS-DOS	IRMX, IRMK	7/0	•	•	•	•	•	•	$2,625
24 parallel	1 RS232	—	—	PDOS	PDOS	7/0	•		•	•			$1,825
—	1 RS232	—	—	Unix	PDOS	7/0	•			•			$2,630
2 8-bit ports	1 RS232	—	—	PDOS	PDOS	7/0	•			•			$1,950
24 parallel	2 RS232	—	VMX	PDOS	PDOS	7/0	•			•			$1,865
24-bit parallel	3 RS232	—	—	PDOS, VRTX	PDOS, OS-9	7/0	•			•			$830
—	3 RS232	1 flme	—	PDOS, OS-9	PDOS, pSOS, OS-9, VRTX, C-Exec	7/0	•			•			$2,540
—	2 RS232	—	VMX	PDOS	PDOS, VMEPROM	7/0	•	•	•	•			—
—	3 RS232	1 flme	—	Unix	—	7/0	•			•			$4,245
—	2 RS232	—	VSB	PDOS, OS-9	PDOS, pSOS, OS-9, VRTX, C-Exec	7/0	•			•			$2,115
—	4 RS232	—	—	PDOS, Unix	PDOS, VMEPROM	7/0	•	•	•	•			—
—	2 RS232	—	VSB	PDOS, Unix	PDOS, VMEPROM	7/0	•	•	•	•			—
—	2 RS232	—	VSB	PDOS, OS-9, Unix	PDOS, pSOS, OS-9, VRTX, C-Exec	7/0	•			•			$3,610
—	3 RS232	—	—	PDOS	PDOS, VMEPROM	7/0	•			•			—
—	3 RS232	—	—	Unix	VRTX, ADA, C-Exec	7/0	•			•			$3,390
—	4 RS232	—	—	PDOS	PDOS, VMEPROM	7/0	•	•	•	•			—
1 printer	2 RS232/422	1 32-bit 68020	none	PDOS, pSOS, OS-9, VRTX, VMEPROM	PDOS, pSOS, OS-9, VRTX, VMEPROM	7/0	•		•	•	•	•	$1,271
1 printer	2 RS232/422	1 32-bit 68020	none	same as above	same as above	7/0	•		•	•	•	•	$2,621
16 lines	up to 2	32-bit, memory I/O	VSB, SAMbus	same as above	same as above	7/7	•	•	•	•	•	•	$1,721 and up
16 lines	up to 2	32-bit, memory, I/O	VSB, SAMbus	same as above	same as above	7/7	•	•	•	•	•	•	$2,096 and up

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
Heurikon 3201 Latham Dr, Madison, WI 53713 (800) 356-9602											**Circle 361**
HK/68/VE	8, 16	20, 24	68000/10	10, 12.5	no	opt	4 32-bit	—	512k/1M	0/0	6U
HK68/VF	8, 16	20, 24	68000/10	10, 12.5	no	opt	4 32-bit	—	512k/1M	0/0	6U
HK68/V10	8, 16	20, 24	68010	10, 12.5	opt	opt	4 32-bit	—	512k/1M	0/0	6U
HK68/V2F	8, 16, 32	24, 32	68020	12.5, 16.7, 20, 25	no	opt	—	—	1M/4M	0/0	6U
HK68/V2E	8, 16, 32	32	68020	16.7, 20, 25	no	opt	—	—	1M/16M	0/1M	6U
HK68/V20	8, 16, 32	32	68020	16.7, 20, 25	opt	opt	4 32-bit	—	1M/4M	0/0	6U
HK68/V30	8, 16, 32	32	68030	20, 25	std	opt	4 32-bit	—	4M/16M	0/0	6U
HK32/V532	8, 16, 32	32	32532	20, 25, 30	std	opt	4 32-bit	—	4M/16M	0/0	6U
Integrated Solutions 1140 Ringwood, San Jose, CA 95131 (408) 943-1902											**Circle 366**
Liberator-SBC	16, 32	16, 24, 32	68020	16 or 20	std	std	—	80	4M/16M	64/—	6U
IO 2430 N Huachuca Dr, Tucson, AZ 85745 (800) 426-2876											**Circle 363**
V68/32	8, 16, 32	24, 32	68020	12.5, 16, 20, 25	no	std	none	10M	1M or 4M	0	6U
Ironics 798 Cascadilla St, Ithaca, NY 14850 (607) 277-4060											**Circle 370**
IV-1602	8, 16	24	68010	10, 12.5	opt	opt	none	4	512k/1M	0	6U
IV-900	32	32	Am29000	25	on chip	std	none	200	2/8/16M	—	6U
IV-3201A	16, 32	24, 32	68020	16, 20	std	std	none	30	1	0	6U
IV-320YA	16, 32	24, 32	68020	16, 20	std	std	none	30	4	0	6U
Logical Design Group 6301 Chapel Hill Rd, Raleigh, NC 27607 (919) 851-1101											**Circle 373**
VME-0286AT	8, 16	24	80286	10	no	opt	7 8-bit, 16-bit	4	1M/1M	0/0	6U
VME-112OD	16	22	DCJ-11	15	std	no	none	5	0/0	0/64k	6U
Matrix 1203 New Hope Rd, Raleigh, NC 27610 (919) 833-2000											**Circle 376**
MS-CPU100	8, 16	24	68000	12.5	—	opt	none	4.1	512k/1M	8k/8k	3U
MS-CPU110	8, 16	24	68010	12.5	—	opt	none	4.1	512k/1M	8k/8k	3U
MS-CPU00	16	24	68000	10	—	—	none	—	0	0/64k	3U
MS-CPU10	16	24	68010	10	—	—	none	—	0	0/64k	3U

Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Real-time executive	Intrpt handler/gen levels	Debug monitor	Mailbox interrupts	Slave functions	Read-modify-write cycles	Dynamic bus sizing	System control functions	OEM price (in 100s)
							Optional features						
—	2 RS232/422	1 16-bit iSBX	—	OS-9, VRTX, VxWorks	pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$1,125
—	2 RS232/422	—	—	OS-9, VRTX, VxWorks	pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$1,200
—	2 RS232/422	—	—	OS-9, VRTX, Unix 5.0, VxWorks	pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$1,895
—	1 RS232/422	—	VSB	OS-9, VRTX, VxWorks	pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$1,500
1 printer	4 RS232/422	—	VSB	OS-9, VRTX, VxWorks	pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$2,025
none	1 RS232/422	—	VSB	OS-9, VRTX, Unix 5.3, VxWorks	pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$2,250
1 printer	2 RS232/422	—	—	OS-9, VRTX, Unix 5.3, VxWorks	pSOS, OS-9, VRTX	7/1	•	•	•	•	•	•	$3,750
none	2 RS232/422	—	—	VRTX, Unix 5.3	VRTX	7/1	•	•	•	•	•	•	$4,500
—	2 sync/async	—	VME	Unix 5	Uniworks	yes/7	•		•	•	•	•	$5,995
—	2 RS232	1 32-bit	VSB or custom	PDOS, Forth	PDOS, pSOS	7/7	•	•	•	•	•	•	$1,700
2	2 RS232/422	none	none	Unix V.2	pSOS	1 to 7/ 1 to 7	•	•	•	•	•	•	$1,530/ $1,800
none	2 RS232	1 DRAM, 1 I/O	none	VRTX	VRTX/ EASI-MP	1 to 7/ 1 to 7	•	•	•	•	•	•	—
none	none	none	VMX	Uniflex	pSOS	1 to 7/ 1 to 7	•	•	•	•	•	•	$2,625
none	none	none	VMX	Uniflex, Unix V.2	pSOS	1 to 7/ 1 to 7	•	•	•	•	•	•	$3,790
1 printer	1 RS232	1, graphics	P2 implemented AT Bus	MS-DOS	PC AT compat.	7/4	•		•				—
20/1 port	4 RS232/422	1 printer, 1 prototype, 1 Opto 22 module driver	none	RSX-11M	RT-11	4 of 7/ 1 of 4	•	•		•			—
none	2 EIA232-D (EIA422/485 opt)	1 math accel., 1 serial port	—	OS-9	OS-9	7/0	•	•	•	•			—
none	same as above	same as above	—	OS-9	OS-9	7/0	•	•	•	•			—
none	2 EIA-232-D	—	—	OS-9	OS-9	7/0	•			•			—
none	2 EIA-232-D	—	—	OS-9	OS-9	7/0	•			•			—

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
Mercury Computer Systems 600 Suffolk St, Lowell, MA 01854 (508) 458-3100											**Circle 379**
MC3200VM	32	24, 32	XL-8032	10	—	std	1 32-bit	25	2M/—	—	6U
Micro Industries 691 Greencrest Dr, Westerville, OH 43081 (614) 895-0404											**Circle 381**
PG2004/10	8, 16	24	68000	8	no	—	—	—	0/0	0/64	6U
PG2005/10	8, 16	24	68000	8	std	—	—	—	0/0	0/64	6U
PG2008/10	8, 16	24	68010	10	no	—	—	—	0/0	0/64	6U
PG2009/10	8, 16	24	68010	10	std	—	—	—	0/0	0/64	6U
PG202X/10	8, 16, 32	24, 32	68000	8	opt	opt	—	—	512k/ 512k	0/0	6U
PG202X	8, 16, 32	24, 32	68010	10	opt	opt	—	—	512k/ 512k	0/0	6U
PG203X	8, 16, 32	24, 32	68010	10, 12.5	opt	no	—	—	0/0	0/0	6U
PG2050	8, 16, 32	24, 32	68020	16	no	std	—	—	0/0	0/1M	6U
PG2100	8, 16, 24, 32	24, 32	68020	16.7	opt	std	—	—	4M/4M	0/0	6U
Micro-Link 14602 N U.S. Highway 31, Carmel, IN 46032 (800) 428-6155											**Circle 384**
VME211	8, 16	—	68000/10	10	no	no	none	5	512k/ 512k	0	3U
VME212	8, 16	24	68010	10	opt	opt	none	5	512k/ 512k	0/64k	3U
VME220	8, 16	24	68020	16	no	opt	none	8	0	256k/ 256k	3U
Microproject 4551 Glencoe Ave, Suite 225, Marina Del Rey, CA 90292 (213) 306-8000											**Circle 390**
2501-2641-6	8, 16	24	68010	10	std	std	1 16-bit	40	1M	0	6U
Mizar 1419 Dunn Dr, Carrollton, TX 75006 (800) 635-0200											**Circle 393**
MZ 7100	8, 16	16, 24	68000/10	10, 12.5	opt	—	4 24-bit, opt	—	512k/ 512k	0	6U
MZ 7105	8, 16	16, 24	68000/10	10, 12.5	opt	std	4 24-bit, opt	—	512k/ 512k	0	6U
MZ 7120	32	32	68020	12.5, 16.7, 20	opt	opt	4 24-bit, opt	—	1M/1M	0	6U
MZ 8106	16	24	68000/10	10, 12.5	no	no	—	—	—	64k/64k	3U
MZ 8115	16	24	68000/10	10, 12.5	opt	opt	opt	—	512k/ 512k	—/64k	3U
MZ 8120	32	32	68020	16.7, 20, 25	opt	opt	opt	—	1M/1M	—/64k	3U
MZ 8130	32	32	68030	16.7, 20, 25, 30	opt	opt	opt	—	1M/1M	—/64k	3U
MZ 7122	8, 16, 32	16, 24, 32	68020	16.7, 20, 25	opt	opt	4 32-bit	—	1M/1M	—	6U
MZ 7124	8, 16, 32	16, 24, 32	68020	16.7, 20, 25	opt	opt	4 32-bit	—	4M/4M	—	6U
MZ 7130	8, 16, 32	16, 24, 32	68030	20, 25, 30	std	opt	4 32-bit	—	4M/4M	0/2M	6U
Motorola, Microcomputer Div. 2900 S Diablo Way, DW283, Tempe, AZ 85282 (602) 438-3518											**Circle 397**
MVME105	8, 16	24	68010	10	no	no	none	—	512k/ 512k	0/128	6U

Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Real-time executive	Intrpt handler/gen levels	Optional features						
							Debug monitor	Mailbox interrupts	Slave functions	Read-modify-write cycles	Dynamic bus sizing	System control functions	OEM price (in 100s)
—	—	—	VSB	Sun, Unix	pSOS	0/7	•		•				—
1 printer	2 RS232C	—	—	none	none	7/0							$760
1 printer	2 RS232C	—	—	none	none	7/0							$1,000
1 printer	2 RS232C	—	—	none	none	7/0							$1,000
1 printer	2 RS232C	—	—	none	none	7/0							$1,200
—	2 RS232C	—	—	none	none	7/0			•	•			$1,400/ $1,480
—	2 RS232C	—	—	none	none	7/0			•	•			$1,480/ $1,560
1 printer	2 RS232C	—	VMX	none	none	7/0			•	•			$1,200 to $1,480
2 8-bit	3 RS232C	—	—	none	none	7/7		•	•	•			$2,680
none	2 RS232C	—	VMS	none	none	7/7		•	•	•			$7,040
none	2 RS232	none	none	PDOS	PDOS	7/0	•			•			$569
none	4 RS232	none	none	PDOS/nix	PDOS	7/0	•		•	•			$1,127
none	2 RS232	prop	none	PDOS	PDOS	7/0	•	•	•	•	•	•	$1,250
none	4 RS232C	—	—	OS-9, VRTX, Unix 5.2	pSOS, OS-9, VRTX, MTDS-UX	7/0	•		•				—
2 8-bit	2 RS232	1 prop	—	OS-9, VRTX-32, VxWorks	OS-9, VRTX-32, VxWorks	7/7	•		•	•	•	•	$1,330
—	2 RS232	—	—	OS-9, VRTX-32, VxWorks	OS-9, VRTX-32, VxWorks	7/7	•		•	•	•	•	$1,540
opt	opt	prop	VSB	OS-9, VRTX-32, VxWorks	OS-9, VRTX-32, VxWorks	7/7	•		•	•	•	•	$1,750
—	—	—	—	OS-9, VRTX-32	OS-9, VRTX-32	7/7	•		•	•	•	•	$440
opt	2 RS232	—	MXbus	OS-9, VRTX-32, VxWorks	OS-9, VRTX-32, VxWorks	7/7	•		•	•	•	•	$1,095
opt	2 RS232	—	MXbus	same as above	same as above	7/7	•	•	•	•	•	•	$1,595
opt	2 RS232	—	MXbus	same as above	same as above	7/7	•	•	•	•	•	•	$2,635
opt	2 RS232/422	prop	VSB opt	same as above	same as above	7/7	•	•	•	•	•	•	$2,395
opt	2 RS232/422	prop	VSB opt	same as above	same as above	7/7	•	•	•	•	•	•	$3,895
opt	2 RS232	prop	VSB opt	same as above	same as above	7/7	•	•	•	•	•	•	$4,795
1 printer	1 RS232C, 1 RS485	none	none	VersaDOS	yes	7/0	•		•		•	•	$995

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
Motorola, Microcomputer Div. 2900 S Diablo Way, DW283, Tempe, AZ 85282 (602) 438-3518											**Circle 397**
MVME117-3FP	8, 16	24	68010	10	no	std	none	—	512k/ 512k	0/256	6U
MVME117A	8, 16	24	68010	10	no	std	none	—	2M/2M	0/256	6U
MVME133A-20	8, 16, 32	24, 32	68020	20	no	std	none	—	1M/1M	0/256	6U
MVME133XT	8, 16, 32	24, 32	68020	25	no	std	none	—	4M/4M	0/256	6U
MVME135/136	8, 16, 32	24, 32	68020	20	std	std	none	—	1M/4M	0/256	6U
MVME147/147-1	8, 16, 32	24, 32	68030	20, 25	std	std	none	—	4M/8M	0/256	6U
National Semiconductor 2900 Semiconductor Dr, PO Box 58090, Santa Clara, CA 95051 (408) 721-5000											**Circle 401**
VME532	8, 16, 32	16, 24, 32	32532	20, 25, 30	std	std, opt	none	up to 15	4M/16M	0	6U
VME332	8, 16, 32	16, 24, 32	32332	15	std	std	none	up to 15	1M/4M	0	6U
Omnibyte 245 W Roosevelt Rd, W Chicago, IL 60185 (800) 638-5022											**Circle 404**
OB68K/VME1	16	24	68000/10	12.5	no	no	none	40	0/0	0/448k	6U
OB68K/VME1M	16	16, 24	68000	10	no	no	none	40	0/0	0/256k	6U
OB68K/VSBC1	16	24	68000/10	12.5, 16	no	opt	4 16-bit	40	512k	0/0	6U
OB68K/VSBC20	16, 32	16, 24, 32	68020	12.5, 16.7, 20, 25	no	opt	none	40	4M/16M	0/0	6U
Pacific Microcomputers 6730 Mesa Ridge Rd, San Diego, CA 92121 (619) 453-8649											**Circle 407**
PV682	8, 16, 32	16, 24, 32	68020	16.67	std	opt	none	10	1M/1M	0/0	6U
PC/M 6805 Sierra Ct, Dublin, CA 94568 (415) 829-8700											**Circle 406**
MPU-1	8, 16, 32	24, 32	68020 4 ea	20, 25	no	2 ea	—	—	0	0.75M	6U
MPU-3	8, 16, 32	24, 32	68030 4 ea	25, 30	std	4 ea	—	—	0	1.5M	6U
Pep Modular Computers 600 N Bell Ave, Pittsburgh, PA 15106 (412) 279-6661; Am klosterwald 4, D-8950 kaufbeuren, Germany 08341/81001											**Circle 408**
VMPM68KA-2	8, 16	16, 24	68000	8, 10, 12.5	—	—	—	—	—	0/128k	3U
MPM68KB	8, 16	24	68HC000/10	10, 12.5	opt	opt	—	—	128k	—	3U
VMPM68KC	8, 16	16, 24	68020	12.5, 16.7	—	opt	—	—	—	1M/1M	3U
VMPM68KC-1	8, 16	16, 24	68020	20, 25	no	opt	—	—	—	1M/4M	3U
VMPM68KC-2	8, 16	16, 24	68020	12.5 to 25	no	opt	—	—	—	1M/4M	3U

Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Real-time executive	Intrpt handler/gen levels	Optional features: Debug monitor	Mailbox interrupts	Slave functions	Read-modify-write cycles	Dynamic bus sizing	System control functions	OEM price (in 100s)
1 printer	2 RS232C	none	none	VersaDOS	yes	7/0	•				•	•	$2,095
1 printer	2 RS232C	none	none	VersaDOS	yes	7/1	•		•		•	•	$1,995
none	2 RS232C, 1 RS422/485	none	none	VersaDOS	yes	7/1	•		•	•	•	•	$1,995
none	2 RS232C, 1 RS422/485	none	none	VersaDOS	yes	7/1	•		•	•	•	•	$2,995
none	2 RS232C	none	VSB	VersaDOS, System V/68	yes	7/1	•		•	•	•	•	$2,995/ $3,495
1 printer	4 RS232C	none	none	VersaDOS, System V/68	yes	7/1	•	•	•	•	•	•	$4,995/ $5,995
—	2 RS232C	—	—	Unix 5.3.1, VRTX	VRTX, VRTX-32	7/0	•	•	•	•			$4,690
—	2 RS232C	—	—	Unix 5.3.1, VRTX	VRTX, VRTX-32	7/7	•	•	•	•			$1,890
16/2	2 RS232C	none	none	C-Exec	C-Exec	7/0	•			•			$646
16/2	2 RS232C	none	none	C-Exec	C-Exec	7/0	•			•			$1,881
opt to 20/2	opt to 4 RS232/422	2 20-bit Omnimodules	none	C-Exec	C-Exec	7/7	•		•	•			$1,036
16/2 (up to 20/1 more opt)	2 RS232/ 422 std (2 opt)	1 20-bit Omnimodule	none	none	none	7/0	•	•		•	•	•	$2,076
none	2 RS423/422	1 32-bit PMIXbus	none	none	none	7/7	•	•	•	•	•	•	—
none	2 RS232	—	—	OS-9, Unix	built-in FLOS	7	•	•	•	•	•	•	$8,000
none	2 RS232	VSB	VSB	OS-9, Unix	built-in FLOS	7		•	•	•	•	•	$12,000
—	1 RS232	—	—	PDOS, OS-9, VersaDOS	PDOS, OS-9, VersaDOS	7/0	•						—
8-bit	2 RS232/ 422/485/ 20 mA	—	—	same as above	same as above	7/0	•						—
—	same as above	—	—	PDOS, OS-9	PDOS, OS-9	7/1	•		•		•	•	—
—	same as above	—	—	PDOS, OS-9	PDOS, OS-9	7/1	•		•		•	•	—
—	same as above	—	—	PDOS, OS-9	PDOS, OS-9	7/0	•	•	•	•	•	•	—

Performance Technologies 435 W Commercial St, East Rochester, NY 14445 (716) 586-6727 **Circle 409**

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
PT-VME 102	8, 16	24	68010	10	no	opt	4 16-bit	1.2	512k/2M	—	6U
PT-VME 105	8, 16	24	68000	10, 12.5, 16	no	opt	4 16-bit	1.2	512k/2M	0/1M	6U
PT-VME 118	8, 16, 32	24, 32	68020	12.5, 16, 20, 25	no	opt	32-bit	16	1M/2M	0/32k	6U
PT-VME 120	8, 16, 32	24, 32	68020	12.5, 16, 20, 25	no	opt	32-bit	16	1M	0/32k	6U

Philips Electronic Instruments 85 McKee Dr, Mahwah, NJ 07430 (201) 592-3800 **Circle 410**
Philips Industrial Automation PO Box 218, 5600 MD Eindhoven, The Netherlands +31 40 785509

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
PG2100	8, 16, 24, 32	24, 32	68020	16	opt	std	—	8, 3	4M/4M	0	6U
PG2050	8, 16	16, 24, 32	68020	16, 20, 25	no	std	—	4.5	0	64k/3M	6U
PG2020	8, 16	16, 24	68000/10	8, 10	opt	opt	—	2, 8	0.5M/ 0.5M	0	6U
PG 2010/10	8, 16	16, 24	68000	8	—	—	—	3	—	16k/320k	6U
PG 8000/10	8	16, 24	68008	8	—	—	—	—	—	0/32k	3U
PG 8010	8, 16	16, 24	68000	8	—	—	—	—	—	16k/16k	3U

Radstone Technology One Blue Hill Plaza, Pearl River, NY 10965 (914) 735-4661 **Circle 414**

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
68-32	8, 16, 32	16, 24, 32	68030	16, 25, 33	std	opt	none	—	4M	8k	6U
68-31	8, 16, 32	16, 24, 32	68030	16, 25, 33	std	opt	none	—	4M	8k	6U
68-25	8, 16, 32	16, 24, 32	68020	12.5, 16, 20, 25	no	opt	none	—	1M/4M	8k	6U
68-23	8, 16, 32	16, 24, 32	68020	12.5, 16, 20	no	opt	none	—	1M/4M	8k	6U
68-14	8, 16	16, 24	68000/10	10	no	opt	4 16-bit	—	512k/2M	0/128k	6U
68-12	8, 16	16, 24	68000/10	10	no	no	none	—	512k/4M	16k	6U
68-1B	8, 16	16, 24	68000	8, 10	no	no	none	—	128k/ 512k	0/16k	6U
CPU-1	8, 16, 32	16, 24, 32	68020	12.5, 16.6	no	opt	none	—	—	128k/ 512k	6U

SBE 2400 Bisso Ln, Concord, CA 94520 (415) 680-7722 **Circle 415**

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
VPG-20	8, 16, 32	24, 32	68020	16	no	no	none	—	0/0	64k/256k	6U
VLAN-E	8, 16, 32	24, 32	68020	16	no	no	none	—	1M/1M	8k/32k	6U

Sun Microsystems, OEM Board Products 2550 Garcia Ave, Mountain View, CA 94043 (415) 960-1300 **Circle 429**

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
3E120	8, 16, 32	16, 24, 32	68020	20	std	std	—	11.1	4M/16M	—	6U × 160 mm
4200	8, 16, 32	16, 24, 32	MB86900 (SPARC)	16.7	std	std	—	11	8M/128M	—	9U × 400 mm
4108	8, 16, 32	16, 24, 32	MB86900 (SPARC)	14.28	std	opt	—	8	8M/32M	—	9U × 400 mm
3200	8, 16, 32	16, 24, 32	68020	25	std	std	—	11	8M/128M	—	9U × 400 mm

Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Real-time executive	Intrpt handler/gen levels	Optional features: Debug monitor	Mailbox interrupts	Slave functions	Read-modify-write cycles	Dynamic bus sizing	System control functions	OEM price (in 100s)
—	2 to 8 RS232/422	16-/24-bit	—	PDOS	PDOS	7/7	•		•	•	•	•	$1,500
—	2 to 8 RS232/422	16-/24-bit	—	pSOS	pSOS	1/7	•	•	•	•	•	•	—
—	1 RS232	32-/24-bit	—	pSOS	pSOS	7/7	•	•	•	•	•	•	$1,600
—	1 RS232	32-/24-bit	VSB	pSOS	pSOS	7/7	•	•	•	•	•	•	$2,000
none	2 RS232	—	VMS	Unix 5.2, DRM, ERM	DRM or ERM	7/7	•	•	•	•	•	•	$6,600
2 8-bit	3 RS232/485	—	—	ERM	ERM	7/7	•	•	•	•	•	•	$2,600
none	2 RS232	—	—	Unix 5.2, DRM, ERM	ERM, DRM	7/7	•		•	•			$1,500
3 8-bit	2 RS232	none	none	ERM	ERM	3/7	•			•			$1,050
none	2 RS232	none	none	ERM	ERM	1/0	•						$750
none	2 RS232	none	none	ERM	ERM	4/7	•						$770
none	2 RS232/422	1 8-bit PEX	—	OS-9, Unix 5.3, VXcel	OS-9, VRTX-32	7/0	•	•	•	•	•	•	—
none	2 RS232/422	1 8-bit PEX	VSB	OS-9, Unix 5.3, VXcel	OS-9, VRTX-32	7/0	•	•	•	•	•	•	—
1 printer	2 RS232/422	1 8-bit PEX	—	OS-9, VXcel, VersaDOS	OS-9, VRTX-32	7/0	•	•	•	•	•	•	—
1 printer	3 RS232/422	—	—	PDOS, OS-9, VersaDOS	OS-9	7/0	•	•	•	•	•	•	—
—	2 RS232/422	1 8-bit	—	OS-9, VersaDOS	OS-9	7/7	•	•	•	•			—
1 printer	1 RS232	—	—	PDOS, OS-9, VersaDOS	OS-9	7/0	•		•	•			—
1 printer	3 RS232	—	—	same as above	OS-9	7/0	•		•	•			—
—	2 RS423	—	VSB	VRTX-32, VXcel, ARTX	VRTX-32, VXcel, ARTX	7/7	•		•	•	•	•	—
none	2 RS232	none	none	—	—	7/7	•	•	•	•	•	•	$1,995
none	2 RS232	none	none	Regulus	RTCK	7/7	•	•	•	•	•	•	$2,620
none	2 RS423, 2 TTL	—	prop memory bus	Sun OS, Unix, ONC, others	VxWorks	7/0	•		•	•	•	•	$4,440
none	2 RS423, 2 TTL	—	same as above	same as above	—	7/0	•		•	•	•	•	$17,536
none	2 RS423, 2 TTL	1 video (Sun P4)	—	same as above	—	7/0	•			•	•	•	$9,536
none	2 RS423, 2 TTL	—	prop memory bus	same as above	—	7/0	•		•	•	•	•	$11,776

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)	Form factor
Sun Microsystems, OEM Board Products 2550 Garcia Ave, Mountain View, CA 94043 (415) 960-1300											**Circle 429**
3004	8, 16, 32	16, 24, 32	68020	16.7	std	std	—	9.5	4M/16M	—	9U × 400 mm
Synergy Microsystems 179 Calle Magdalena, Encinitas, CA 92024 (619) 753-2191											**Circle 430**
SV20	8, 16, 32	24, 32	68020	12.5, 16.7, 20, 25, 33	opt	opt	none	32	1M/1M	0/0	6U
SV20C	8, 16, 32	24, 32	68020	12.5,16.7	no	opt	none	25	1M/1M	0/0	6U
SV21	8, 16, 32	24, 32	68020	12.5, 16.7, 20, 25, 33	opt	opt	none	32	4M/36M	0/0	6U
SV31	8, 16, 32	24, 32	68030	20, 25,33	std	opt	none	32	4M/36M	0/—	6U
TL Industries 2541 Tracy Rd, Toledo, OH 43619 (419) 666-8144											**Circle 434**
TVME 1611	8, 16	24	68010	10	—	opt	—	30	512k/4M	2k/8k	6U
TVME 1612	8, 16	24	68000	8, 10	—	—	—	30	—	0/192k	6U
TVME 1613	8, 16	24	68000	8, 10	—	—	—	30	512k/1M	0/192k	6U
Torch Computers Abberley House, Great Shelford, Cambridge, England CB2 5LQ +44 223 841000											**Circle 440**
VME32QX	8, 16, 32	24, 32	68020	16.7, 20	std	std	4 32-bit	80	4M/16M	0	6U
VME 542 Valley Way, Milpitas, CA 95035 (408) 946-3833											**Circle 441**
V4000-08	16	24	NC4016	8	—	—	—	8	—	128k/128k	6U
V4000-04	16	24	NC4016	4	—	—	—	4	—	64k/64k	6U
VME Specialists 558 Brewster Ave, Redwood City, CA 94063 (415) 364-3328											**Circle 442**
SBC-1	8, 16	24	68000/10	10	—	—	—	—	512k/ 512k	0/64k	3U
SBC-2	8, 16	24	68000/10	10	—	opt	—	—	512k/512k	0/64k	3U
SBC-3	8, 16	24	68020	12.5, 16	—	opt	—	—	—	512k	3U
Xycom 750 N Maple Rd, Saline, MI 48176 (800) 367-7300											**Circle 449**
XVME-682	8, 16	24	80286	10	—	opt	—	20	1M/4M	20/20	6U
XVME-600/601	8, 16	24	68000/10	10	—	no	none	20	512k/ 512k	0/128k	3U/6U
XVME-602	8, 16	24	68020	16	—	opt	none	20	0/0	256k/ 256k	3U/6U
XVME-650	8, 16, 32	32	32332	15	std	opt	none	20	1M/4M	0/64k	6U
Tadpole Technology 1601 Trapelo Rd, Waltham, MA 02154 (617) 890-8898											**Circle 455**
TP880V	8, 16, 32	24, 32	88100	20, 25	88200 x2	int.	2 16-bit	20	4M/16M	2k	6U
TP33V	8, 16, 32	24, 32	68030	16, 20, 25, 33	internal	opt	4 16-bit	20	4M/16M	2k	6U
TP30V	8, 16, 32	24, 32	68030	16, 20, 25, 33	internal	opt	—	20	8M/32M	2k	6U
TP22V	8, 16, 32	24, 32	68020	16, 20	opt	opt	—	16	4M/16M	2k	6U
TP20V	8, 16, 32	24, 32	68020	12, 16	opt	opt	—	16	2/8	2k	6U
TP21V	8, 16, 32	24, 32	68020	12, 16	opt	opt	—	16	2/8	2k	6U

Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Real-time executive	Intrpt handler/gen levels	Optional features: Debug monitor	Mailbox interrupts	Slave functions	Read-modify-write cycles	Dynamic bus sizing	System control functions	OEM price (in 100s)
none	2 RS423	—	same as above	same as above	—	7/0	•		•	•	•	•	$6,656
4 I/O	4 RS232	1 32-bit	VSB opt	PDOS, OS-9, Unix	PDOS or OS-9	7/1	•	•	•	•	•	•	$1,925
4 I/O	4 RS232	1 32-bit	VSB opt	PDOS, OS-9	PDOS or OS-9	7/1	•	•	•	•	•	•	$1,985
4 I/O	4 RS232	1 32-bit	VSB opt	PDOS, OS-9, Unix	PDOS or OS-9	7/1	•	•	•	•	•	•	$4,685
4 I/O	4 RS232	1 32-bit	VSB opt	same as above	PDOS or OS-9	7/1	•	•	•	•	•	•	$4,985
2 8-bit; SCSI	2 RS232	—	—	—	—	7/0				•			$895
0	1 RS232C	—	I/O	—	—	7/0				•			$620
0	1 RS232C	—	I/O	—	—	7/0			•	•			$795
—	2 RS232	—	—	OS-9, Unix 5.2	OS-9	7	•		•	•	•	•	$3,100
16	2 RS232	—	—	Forth	Forth	7/7	•		•	•			$2,800
16	2 RS232	—	—	Forth	Forth	7/7	•		•	•			$1,820
—	2 RS232	—	—	OS-9	PDOS, pSOS, OS-9, VRTX	7/0	•			•			$564
—	2/4 RS232	1 VME 750	—	OS-9	same as above	7/0	•		•	•			$727
—	2 RS232	expansion	6U or 3U	OS-9	pSOS, OS-9, VRTX-32	7/0	•	•	•	•			$1,240 to $1,340
1 printer	2 RS232/422	—	—	MS-DOS	PC AT compat.	7/0	•	•	•		•	•	$2,800
none	2 RS232	—	—	PDOS, OS-9	PDOS, OS-9	7/0	•			•	•	•	$430
none	2 RS232	1 32-bit VME	—	PDOS, OS-9	PDOS, OS-9	7/0	•	•	•	•	•	•	$1,500
none	2 RS232/422	—	—	Unix	VRTX	7	•	•	•	•	•	•	$2,800
SCSI	2 RS232	none	none	TPIX, Unix	no	7/7	•	•	•	•		•	—
SCSI, printer	4 RS232	none	none	TPIX, Unix	VRTX	7/7	•	•	•	•	•	•	—
—	2 RS232	none	VSB	TPIX, Unix	VRTX	7/7	•	•	•	•	•	•	—
SCSI, FDC	2 RS232, 10 async	none	none	TPIX, Unix UniPlus	VRTX, OS-9	7/0	•	•	•	•	•	•	—
SCSI	2 RS232	none	none	same as above	VRTX, OS-9	7/0	•	•	•	•	•	•	—
SCSI	2 RS232	none	none	same as above	VRTX, OS-9	7/0	•	•	•	•	•	•	—

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Aeroflex Laboratories 35 S Service Rd, Plainview, NY 11803 (516) 694-6700										**Circle 306**
M 86/30	8, 16	20, 24	8086	8	no	opt	none	4	128k/512k	0/0
M 286/00	8, 16	20, 24	80286	10, 12	no	opt	none	4	0/0	0/0
M 186/01	8, 16	20	80186	8	no	opt	2 16-bit	4	0/0	16k/64k
Central Data 1602 Newton Dr, Champaign, IL 61821 (800) 482-0315										**Circle 323**
CD21/8086	8, 16	20, 24	8086	5, 8, 10	no	opt	none	7	128k/1M	0/64
CD21/8286	8, 16	20, 24	80286	8	yes	opt	11 16-bit	7	512k/4M	0/64
CD21/8386	8, 16, (32)	20, 24	80386	20	yes	opt	8 32-bit	7	1M/4M	0/0
CD21/8086V	8, 16	20, 24	V30	5, 8 10	no	opt	none	7	512k/1M	0/64
Concurrent Technologies 25401 Cabot Rd #206, Laguna Hills, CA 92653 (714) 768-3332										**Circle 332**
CPI 386/016	8, 16	20, 24	80386	16	no	opt	8	7	0	128/1M
Grammar Engine 3314 Morse Rd, Columbus, OH 43229 (614) 471-1113										**Circle 360**
Mach I	8, 16	16, 24	68000	approx 8 to 16	no	no	none	4	128k/512k	0/0
Mach I-2B-	8, 16	16, 24	68000	approx 8 to 16	no	no	4 16-bit	4	128k/2M	0/0
Heurikon 3201 Latham Dr, Madison, WI 53713 (800) 356-9602										**Circle 361**
HK68/ME	8, 16	24	68000/68010	10, 12.5	no	opt	4	—	512/1M	0/0
HK68/M10	8, 16	24	68010	10, 12.5	yes	opt	4	—	512/1M	0/0
HK68/Mize	16, 32	32	68020	12.5, 16.7, 20, 25	no	—	4	—	1M/4M	0/0
HK68/Mizo	16, 32	32	68020	12.5, 16.7, 20, 25	yes	opt	4	—	1M/4M	0/0
HK68/M130	16, 32	26, 32	68030	20, 25	yes	opt	4	—	1M/16M	0/1M
Innovative Research 17071 Kampen Ln, Huntington Beach, CA 92647 (714) 842-0492										**Circle 365**
SBC 90A	8	20	Z80A	4	yes	yes	1	—	128k	0
Intel 3065 Bowers Ave, PO Box 58065, Santa Clara, CA 95052 (800) 548-4725										**Circle 367**
SBC 386/21/ 22/24/28	8, 16, 32	20, 24	80386DX	16	yes	yes	none	10	1M/16M	0/0
SBC 386/31/ 32/34/38	8, 16, 32	20, 24	80386DX	20	yes	yes	none	10	1/16M	0/0
SBC 286/12/ 14/16	8, 16	20, 24	80286	8	yes	opt	4	10	1/16M	0/0

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
no	24 prog lines	2 RS232/422	none	none	RMX 86	yes	yes	no	mil-spec conduction cooled	—
—	24 prog lines	2 RS232	none	none	RMX 86, 286	yes	yes	no	same as above	—
yes	16 prog lines	1 RS232, 1 RS422	none	none	RMX 86	yes	yes	no	same as above	—
no	24 prog lines	1 RS232	2 8-/16-bit SBX	none	—	yes	no	no	up to 256k EPROM, compat. w/Intel 86/3x	$945
no	printer	RS232/422, 3 RS232	1 8-/16-bit SBX	loc. memory/ LBX	—	yes	no	no	up to 512k EPROM, compat. w/Intel 286/1x	$1,255
—	no	1 RS232	2 8-/16-bit SBX	none	—	yes	no	no	up to 512k EPROM, compat. w/Intel 386/3x	$5,200
no	24 prog lines	1 RS232	2 8-/16-bit SBX	none	—	yes	no	no	up to 256k EPROM	$950
no	0	2	prop DRAM memory exp.	ISBX	Unix	yes	yes	no	32-bit DMA cont., SCSI	—
no	none	RS232	—	—	Unix	yes	yes	yes	intell. comm slave/coprocessor	$795
no	1 printer	2 RS232	—	—	Unix	yes	yes	yes	coprocessing platform	$1,295
—	8/1	2 RS232	2 iSBX	—	OS-9 Vxworks	yes	yes	yes	6 16-bit counter/timers; SCSI, 128k EPROM	$1,125
—	8/1	4 RS232	2 iSBX	iLBX	OS-9, Vxworks, Unix	yes	yes	yes	SCSI, 128k EPROM	$1,950
—	8/1	2 RS232	2 iSBX	iLBX	OS-9, Vxworks	yes	yes	yes	256k EPROM, SCSI	$1,800
—	8/1	2 RS232	1 iSBX	iLBX	Unix V.3, OS-9, Vxworks	yes	yes	yes	SCSI, 256k EPROM	$2,500
—	16 prog lines/1	4 RS232	1 8-bit iSBX	iLBX	Unix V.3, OS-9, Vxworks	yes	yes	yes	2M (E)(E)(P)ROM, SCSI	$2,900
—	16	2 RS232C	none	none	CP/M	yes	no	no	floppy controller, 16-bit I/O, math chip	$795
no	none	1 RS232	1 8-/16-bit SBX	prop	RMX I,II, Xenix	yes	yes	yes	64 kbytes cache	—
no	none	1 RS232	1 8-/16-bit SBX	prop	RMX I,II	yes	yes	yes	64 kbytes cache	—
no	16 prog lines	2 RS232/432	2 8-/16-bit SBX	prop	RMX I,II, Xenix	yes	—	yes	—	$2,636

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Intel 3065 Bowers Ave, PO Box 58065, Santa Clara, CA 95052 (800) 548-4725										**Circle 367**
SBC 286/10A	8, 16	20, 24	80286	6	yes	opt	4	10	0/16M	0/0
iSBC 86C/38	8, 16	20, 24	80C86	1, 8	yes	opt	none	10	1M/1M	0/64
iSBC 86/35	8, 16	20, 24	8086	5, 8	yes	opt	none	10	512k/1M	0/0
iSBC 86/30	8, 16	20, 24	8086	5, 8	yes	opt	none	10	128k/256k	0/0
iSBC 86/05A	8, 16	20, 24	8086	5, 8	yes	opt	none	10	0/0	8k/16k
iSBC 186/03A	8, 16	20, 24	80186	5, 8	yes	opt	2	10	0/1M	0/256k
iSBC 80/24A	8	16	8085A-2	2.4, 4.8	yes	—	none	10	0/32k	8k/8k
iSBC 88/25	8	16	8088	5	yes	opt	—	10	4k/8k	0/128k
iSBC 80/40A	8	16	8088	4.8/6.67	yes	opt	—	10	4/8k	0/128k
Megadata 35 Orville Dr, Bohemia, NY 11716 (516) 589-6800										**Circle 378**
M80748	8, 16	16, 24	M68020	16.7	yes	opt	—	10	1M/8M	0/0
M80736	8, 16	16, 24	M68010	8, 10	yes	—	—	10	1M/2M	0/0
M80781	8, 16	16, 24	M68030	10, 20	yes	opt	—	10	4M/64M	0/0
Metacomp 9466 Black Mountain Rd, San Diego, CA 92126 (619) 578-9840										**Circle 380**
MPA-2000	8, 12, 16	—	80186	8	no	opt	8 8-bit	1.6	128k/512k	0/16k
MPX-2000-160	8, 12, 16	—	80186	8	no	opt	8 8-bit	1.6	128k/512k	0/16k
Micro Industries 691 Greencrest Dr, Westerville, OH 43081 (614) 895-0404										**Circle 381**
MSBC 80/05	8, 16	16	8085A	9.8	no	no	none	—	0	256/256
MSBC 80/16D	8	24	8080A	2	no	no	none	—	0	16/64
MSBC 88/40A	8, 16	20	8088	4.8	no	opt	none	—	0	4k/24k
MSBC 86/05	8, 16	24	8086	5, 8	no	no	none	—	0	8k/8k
MSBC 86/35	8, 16	20, 24	8086	5, 8	no	opt	none	—	512k/1M	0/0
MSBC 286/12	8, 16	24	80286	8	no	opt	4	8	1M	0/256k
Microbar Systems 785 Lucerne Dr, Sunnyvale, CA 94086 (408) 720-9300										**Circle 386**
DBC68K2	8, 16	20, 24	68000, 68010	10, 12	opt	no	none	2	128k/512k	0/0
GPC68020	8, 16	20, 24	68020	12.5, 16.7	opt	opt	4	5	1M/8M	0/0
G20RT	8, 16	20, 24	68020	20	no	opt	none	5	1M/4M	0/0
G20FX	8, 16	20, 24	68020	16.7, 20, 25	no	opt	—	5	256k/1M	8k/32k
G30FX	8, 16	20, 24	68030	16.7, 20, 25	opt	opt	—	5	128k/1M	8k/32k
F20RT	8, 16	20, 24	68020	20, 25	no	opt	none	5	1M	8k/32k
Microdesigns 1874 Forge St, Tucker, GA 30084 (404) 493-6318										**Circle 388**
Multiboard-86	8, 16	20	8086-2	5, 8	no	opt	none	2	0/0	16k/128k

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
no	16 prog lines	2 RS232/432	2 8-/16-bit SBX	prop	same as above	yes	—	yes	—	$1,898
yes	24 prog lines	1 RS232C	2 8-/16-bit SBX	none	RMX I	yes	no	yes	all CMOS, 5W power	$1,796
yes	24 prog lines	1 RS232C	2 8-/16-bit SBX	none	RMX I	yes	no	yes	—	$1,540
yes	24 prog lines	1 RS232C	2 8-/16-bit SBX	none	RMX I	yes	no	yes	—	$1,310
yes	24 prog lines	1 RS232C	2 8-/16-bit SBX	none	RMX I	yes	no	yes	—	$876
yes	24 prog lines	2 RS232C, RS422	2 8-/16-bit SBX	iLBX	RMX I	yes	no	yes	SCSI 8/12 28-pin sites	$986
no	48 prog lines	1 RS232	2 8-bit SBX	—	RMX I	yes	no	yes	—	$945
no	24 prog lines	1 RS232	2 8-bit	—	RMX I	yes	no	yes	-	$790
no	24 prog lines	—	3 8-bit SBX	—	RMX I	yes	no	yes	32 analog inputs	$2,000
—	—	2 RS232	1 prop	—	—	yes	no	yes	1 8-bit EEPROM	—
—	—	2 RS232	1 prop	—	—	yes	no	yes	2 8-bit EEPROM	—
—	—	2 RS232	1 prop	—	—	yes	no	yes	1 8-bit EEPROM	—
—	—	1 RS232	2 MPX	—	MRTM	yes	yes	yes	MPX daughter boards	$1,825 to $2,175
—	—	16 serial	1 MPX site	—	MRTM	yes	yes	yes	MPX daughter boards	$1,255
no	22 prog lines	—	—	—	none	no	no	no	—	$295
no	48 prog lines	1 RS232	2 8-bit SBX	—	none	no	no	no	6 (E)(E)(P)ROM sites	$465
no	24 prog lines	none	3 8-bit SBX	—	none	no	no	no	32 SE, 16 analog inputs	$840
no	24 prog lines	1 RS232	—	—	none	no	no	no	—	$800
yes	24 prog lines	1 RS232C	2 8-/16-bit SBX	—	none	no	no	no	4 (E)(E)(P)ROM sites	$1,200
no	24 prog lines	1 RS232C/422, 1 RS232C	2 8-/16-bit SBX	—	none	no	no	no	2 28-pin JEDEC sites	$2,800
no	none	2 RS232	1/memory	none	none	yes	no	yes	high-speed memory access bus	$1,257
no	16 prog lines	2 RS232/422	1 8-/16-bit SBX, 11/ memory	none	Unix, VRTX	yes	yes	yes	opt TODC	$1,712
no	16 prog lines	2 RS232/422	same as above	none	—	yes	yes	yes	same as above	$2,303
no	—	1 RS232	1 FX module	FX bus, prop	—	yes	yes	opt	module provides 24 sq. in. of user app. area	$1,271
no	—	1 RS232	1 FX module	FX Bus	—	yes	yes	yes	same as above	—
no	—	2 RS232	1 SBX	—	—	yes	yes	yes	25 MHz, 1 wait state	—
yes	24 prog lines, 3 out/8 in	1 RS232	2 8-bit SBX, 2 8-/16-bit SBX	prop	none	no	yes	no	SBC 86/14 compat., prototype area	$746

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Monolithic Systems 84 Inverness Cir E, Englewood, CO 80112 (303) 790-7400 **Circle 394**										
MSC 8186-700	8, 16	16, 20, 24	80/86	8 MHz	no	yes	2 16-bit	—	1M/1M	0/0
Nissho Electronics 17320 Red Hill Ave, Suite 200, Irvine, CA 92714 (714) 261-8811 **Circle 402**										
N3101	8, 16	20, 24	8086	5, 8, 10	yes	opt	none	—	0.5M/1M	0/0
N3102	8, 16	20, 24	80286	8	yes	opt	4 16-bit	—	1M/2M	0/0
Omnibyte 245 W Roosevelt Rd, W Chicago, IL 60185 (800) 638-5022 **Circle 404**										
OB68K1A	16	24	68000, 68010	10	no	no	none	20	128k/512k	0/0
OB68K/MSBC1	16	24	68000, 68010	12.5	no	no	none	20	256k/2M	0/0
OB68K/MSBC30	16, 32	16, 24, 32	68030	16, 20, 25, 33	yes	opt	4 16-bit	20	4M/32M	0/0
Pacific Microcomputers 6730 Mesa Ridge Rd, San Diego, CA 92121 (619) 453-8649 **Circle 407**										
PM68D	8, 16	20, 23	68000/68010	10	yes	no	none	4	256k/1M	0/0
PM680K	8, 16	20, 23	68000/68010	10	yes	no	none	4	512k/1M	0/16k
PM680R	8, 16	20, 24	68000/68010	12.5	no	no	2 16-bit	4.2	2M/4M	0/0
PM682	8, 16	24	68020	16.7	yes	opt	none	4.6	1M/2M	0/0
PM682T	8, 16	20, 24	68020	20, 25	yes	opt	1 16-bit	5.6	2M/8M	0/0
Radstone Technology One Blue Hill Plaza, Pearl River, NY 10965 (914) 735-4661 **Circle 414**										
MP-1	8, 16	20	80C86	5, 8	no	yes	none	—	64k	64k
MP-2	8, 16	20, 24	80286	8, 10	no	yes	none	—	128k	64k
SBE 2400 Bisso Ln, Concord, CA 94520 (415) 680-7722 **Circle 415**										
MPU-28	8, 16, 32	24	68020	12.5, 20	opt	opt	none	—	1M/8M	0/64k
MPU-20	8, 16, 32	24	68020	16.7, 20	opt	opt	none	—	1M/2M	0/64k
M68CPU	8, 16	24	68000/68010	10	yes	no	none	—	512k/8M	0/0
M68K10	8, 16	24	68000/68010	10	no	no	none	—	128k/1M	0/16k
MPU-12	8, 16	24	68000/68010	12.5	no	no	4 16-bit	—	128k/4M	0/64k
Single Board Solutions 20045 Stevens Creek Blvd, Cupertino, CA 95014 (408) 253-0250 **Circle 421**										
MAT286	8, 16	20, 24	80286	10	yes	opt	4 8-bit, 3 16-bit	3	512k/4M	0/512k
MBx8000	8, 16	20, 24	Z8001/Z8002	4, 6, 10	yes	no	none	4	128k/512k	0/128k
Tadpole Technology 1601 Trapelo Rd, Waltham, MA 02154 (617) 890-8898 **Circle 455**										
TP20M	8, 16	20, 24	68020	12, 16	opt	opt	0	7	2M	2k

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
no	24 prog lines	1 RS232	2 8-/16-bit iSBX	—	iRMX-86, MS-DOS	yes	no	no	4 28-pin sockets	$1,095
—	24 parallel	1 RS232	1/memory	—	none	no	no	no	—	$1,000
—	—	2 RS232	—	—	none	no	no	no	2 to 8 16-bit EPROM	$1,775
—	32/2	2 RS232	none	none	Idris, Forth, VRTX,	yes	yes	no	—	$841
—	none	4 RS232	1 8-/16-bit iSBX	none	Idris, Forth, C-Exec	yes	yes	yes	—	$1,101
—	16/2	2 RS232, 2 RS232/422	1 20-bit Omnimodule	none	none	yes	no	yes	256 bytes cache; SCSI, GPIB opt	—
—	16/1	2 RS422/423	none	PMX16	Unix 5.0	yes	no	yes	5 16-bit counter/timers;	—
—	16/1	2 RS422/423	none	none	none	yes	no	no	5 16-bit counter/timers;	—
—	printer compat.	2 RS232	1 8-/16-bit iSBX	none	OS-9	yes	yes	no	3 16-bit counter/timers, dual port memory,	—
—	8-bit/2	2 RS422/423	1 32-bit PMIXbus	none	Unix 5.2, OS-9	yes	yes	yes	8 16-bit counter/timers; dual port memory	—
—	none	2 RS422/423	none	16-bit SCSI	Unix 5.2, OS-9	yes	yes	yes	5 16-bit counter/timers; dual port memory	—
no	—	1 RS423	—	20-bit local	iRMX-86	yes	yes	no	low power CMOS, comm. ruggedized, mil	—
no	—	2 RS423	—	24-bit ext local	iRMX-286	yes	yes	no	low power, 0 wait-state loc. bus	—
no	24	2 RS232	1 8-/16-bit iSBX	—	Regulus Unix V.2	yes	—	yes	SBE watchdog timer; mailbox; 8 M DRAM	$2,950
no	24	2 RS232	2 8-/16-bit iSBX	—	Regulus Unix V.2	yes	—	yes	SBE watchdog timer; mailbox	$1,950
no	—	2 RS232	1 8-bit, 1 16-bit iSBX	prop	Regulus	yes	—	no	no-wait-state MMU	$845
no	24	2 RS232	2 8-bit iSBX	—	Regulus	yes	yes	no	—	$700
no	24	2 RS232	2 8-/16-bit iSBX	—	Regulus	yes	—	yes	DMA support for iSBX connectors	$1,995
opt	18 prog lines	2 RS232	2 8-/16-bit SBX	ATBus header	PC/AT compat.	yes	yes	no	piggy-back EGA card, AT-compat. in 2 slots	$1,395
opt	40 prog	2 RS232	1 8-bit SBX	none	CP/M 8000 floppy, SCSI	yes	yes	no	8 28-pin mem sockets	$1,011
yes	SCSI	2 RS232	none	iLBX	UniPlus Unix	yes	VRTX	no	—	—

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Single Board Solutions 20045 Stevens Creek Blvd, Cupertino, CA 95014 (408) 253-0250 **Circle 421**										
MB4116	8, 16	20	Z8002	4	yes	no	none	2	32k/32k	0/0
MB4126	8, 16	20	Z8002	4	yes	no	none	2	128k/128k	0/0
MB1801	8, 16	20, 24	Z8001	10	yes	no	none	4	0/0	0/0
Strobe Data 13240 Northup Way, #19, Bellevue, WA 98005 (206) 641-4940 **Circle 428**										
FOX8532	16	16	F9445	16	yes	no	1 16-bit	3.6	64k/512k	0/512
Synergy Microsystems 179 Calle Magdalena, Encinitas, CA 92024 (619) 753-2191 **Circle 430**										
SM20	8, 16	20, 24	68020	12.5, 16.7, 20, 25, 33	opt	opt	none	10	1M/10M	0/0
SM21	8, 16, 32	20, 24, 28	68020	12.5, 16.7, 20, 25, 33	opt	opt	none	20	4M/24M	0/0
SM31	8, 16, 32	20, 24, 28	68030	16.7, 20, 25, 33	yes	opt	none	40	4M/24M	0/0
SM68E	8, 16	20, 24	68000/68010	10, 12.5	yes	no	none	5	1M/5M	0/0
SM68S	8, 16	20, 24	68000/68010	10, 12.5, 16	yes	no	none	7	128k/4M	0/0
Zendex 6700 Sierra Ln, Dublin, CA 94568 (415) 828-3000 **Circle 452**										
ZX-86/05A	8, 16	20	8086	5, 8, 16	no	yes	—	10	—	0/128k
ZX-186/30-812	8, 16	20	80186	8	no	yes	2	10	128/1M	0/0
ZX-286/ 12/14/16	8, 16	24	80286	8	yes	yes	4	10	1/4M	0/0
ZX-386-8	8, 16, 32	28	80386	16	yes	yes	8	20	1/8M	0/0

■ Multibus II

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Concurrent Technologies 25401 Cabot Rd #206, Laguna Hills, CA 92653 (714) 768-3332 **Circle 332**										
MCP386/016	32	32	80386	16	no	opt	8	32	0/16M	128/1M
Heurikon 3201 Latham Dr, Madison, WI 53713 (800) 356-9602 **Circle 361**										
HK68/M220	16, 32	26, 32	68020	16.7, 20, 25	opt	opt	4	—	1M/4M	0/0
Intel 3065 Bowers Ave, PO Box 58065, Santa Clara, CA 95052 (800) 548-4725 **Circle 367**										
iSBC 386/116	8, 16, 24, 32	32	80386	16	yes	yes	4 32-bit	40	1M/16M	64k/64k
iSBC 386/120	8, 16, 24, 32	32	80386	20	yes	yes	4 32-bit	40	1M/16M	64k/64k
186/100	8, 16, 24, 32	20	80186	8	no	opt	4	4	512k/512k	0/0
286/100A	8, 16, 24, 32	24	80286	8	yes	opt	4	2.3	0/16M	0/128k

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
—	24 prog	2 RS232	none	none	none	yes	yes	no	previously AMD 4116	$1,046
—	24 prog	2 RS232	none	none	none	yes	yes	no	previously AMD 4126	$1,116
—	none	none	none	none	Xenix	yes	no	no	LBX Bus compat. with 1034 and 1017	$1,046
yes	none	4 serial	none	none	yes	yes	yes	no	real-time/calendar clock; diskette controller	$1,975
no	4 I/O lines	2 RS422/423	1 32-bit	prop	Unix, PDOS	yes	yes	yes	256 bytes cache, SCSI, graphics cont.	$2,360
yes	4 I/O lines	2 RS422/423	1 32-bit	prop	Unix, PDOS	yes	yes	yes	same as above	$4,535
yes	4 I/O lines	2 RS422/423	1 32-bit	prop	Unix, PDOS	yes	yes	yes	512 bytes of cache and same as above	$4,835
no	4 I/O lines	2 RS422/423	none	prop	Unix	yes	no	yes	SCSI, 24 parallel I/O lines	$1,655
no	4 I/O lines	2 RS422/423	none	prop	Unix	yes	no	yes	SCSI port; 5 timers; 4 EPROM sites	$970
—	—	2	3	none	CP/M, RMX	yes	yes	yes	—	$775
—	—	2	2 SBX	none	CP/M, RMX, CDOS	yes	yes	yes	—	$1,025
—	—	2	2 SBX	none	RMX 86/286, Xenix	yes	yes	yes	SBC-286/12 alone	$1,985/$2,265
—	—	2	2 SBX	none	RMS 286/86	yes	yes	yes	—	$5,500(4M)/ $6,500(8M)
no	0	2 RS232/422	prop DRAM	CCBX	Unix	yes	yes	no	32-bit DMA controller	—
—	8/1	2 RS232	1 8-/16-bit iSBX	iLBX II	Unix V.3, OS-9, Vxworks	yes	yes	yes	128 bytes non-vol. RAM, 256k EPROM, SCSI	$3,000
no	none	1 RS232C	1 8-/16-bit SBX	none	iRMX, I, II.3, Unix V.3	yes	yes	no	64k bytes cache; 2 32-bit EPROM sites	$3,456 (1M)
no	none	1 RS232C	1 8-/16-bit SBX	none	same as above	yes	yes	no	same as above	$4,320 (1M)
—	24 parallel lines	1 RS232, RS422	1 8-/16-bit SBX	—	iRMX	yes	yes	no	parallel port config. as SCSI or printer; sockets for 512k EPROM	$1,436
—	24 parallel lines	2 RS232/422	1 8-bit SBX, 1 8-/16-bit SBX	LBX II	iRMX	yes	yes	no	2 28-pin SRAM sites	$1,796

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Micro Industries 691 Greencrest Dr, Westerville, OH 43081 (614) 895-0404										**Circle 381**
MIB II 386/100	8, 16, 32	32	80386	20	yes	opt	4 16-bit	13.3	2M/2M	—
MIB II 386/101	8, 16, 32	32	80386	20	yes	opt	4 16-bit	13.3	2M/2M	—
MIB II 386/102	8, 16, 32	32	80386	20	yes	opt	4 16-bit	13.3	2M/2M	—
MIB II 386/110	8, 16, 32	32	80386	16	yes	no	8 32-bit	32	—	128k/512k
MIB II 386/111	8, 16, 32	32	80386	16	yes	no	8 32-bit	32	—	128k/512k
MIB II 386/112	8, 16, 32	32	80386	16	yes	no	8 32-bit	32	—	512k/512k
MIB II 386/113	8, 16, 32	32	80386	20	yes	no	8 32-bit	40	—	128k/512
MIB II 386/114	8, 16, 32	32	80386	20	yes	no	8 32-bit	40	0	128k/512k
MIB II 386/115	8, 16, 32	32	80386	20	yes	no	8 32-bit	40	0	128k/512k
MIB II 386/120	8, 16, 32	32	80386	16	yes	opt	7 16-bit	8	2M/2M	114
MIB II 186/101	8, 16, 32	20	80186	8	yes	opt	2 16-bit	2	1M/1M	0/0
MIB II 186/102	8, 16, 32	20	80186	8	yes	yes	6 16-bit	2	1M/1M	0/0
MIB II 186/110A	8, 16, 32	32	80186	8	no	no	6 16-bit	2	512k/512k	0/64k
MIB II 186/110B	8, 16, 32	32	80C186	10, 12.5, 16	no	no	2	4	0	0/64k
Microbar Systems 785 Lucerne Dr, Sunnyvale, CA 94086 (408) 720-9300										**Circle 386**
MT20A	8, 16, 24, 32	32	68020	12.5, 16.67	opt	opt	4	5	1M/4M	0
Tadpole Technology 1601 Trapelo Rd, Waltham, MA 02154 (617) 890-8898										**Circle 455**
TP33M	8, 16, 32	32	68030	16, 20, 25, 33	—	opt	4, 32	40	4M/16M	2k
TP880M	8, 16, 32	32	88100 + 68000	20, 25	88200	—	4, 32	40	4M/16M	2k

■ STD Bus

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Advanced Micro Systems 31 Flagstone Dr, Hudson, NH 03051 (603) 882-1447										**Circle 302**
BAS-52	8	16	8052	11.0592	no	no	—	1.8	0/0	8/16
CPU-31	8	16	8031	11.0592	no	no	—	1.8	0/0	0/16
CPU-32	8	16	8032	11.0592	no	no	—	1.8	0/0	0/16
Computer Dynamics 107 S Main St, Greer, SC 29651 (803) 877-8700										**Circle 330**
CPU-186	8	20	80186	8, 10, 12, 16	yes	opt	2 8-bit	1	0/0	0/512k
CPU-188	8	20	80188	8, 10	yes	opt	2 8-bit	1	0/1M	0/32k
CPU-9	8	16	Z80	2.5, 4, 6, 8, 10	no	no	none	—	0	0/64k
CPU-2+	8	16	Z80	2.5, 4, 6, 8, 10	no	no	none	—	0	0/64k
STD-Bit Boss	8	16	8044/8051	12	no	no	none	—	0	8/40k
Cubit Div., Proteus Industries 190 S Whisman Rd, Mountain View, CA 94041 (415) 962-8237										**Circle 336**
7540	8	16	6502	2	no	no	none	—	0	0/56k
8020	8	20	64180	4.6	yes	no	1 8-bit	—	0	64k/64k
8400	8	20	V40	7.4	no	no	1 8-bit	—	0	64k/64k
8600	8, 16	24	80186	10	no	no	2 16-bit	—	0	64k/64k

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
—	—	1 RS232C	1 OME	none	no	yes	yes	no	SCSI	$4,400
—	—	1 RS232C	1 OME	none	no	yes	yes	no	64 kbytes cache; SCSI	$4,800
—	—	1 RS232C	1 OME	none	no	yes	yes	no	256 kbytes cache; SCSI	$5,600
—	—	1 RS232C	1 OME	none	no	yes	yes	no	1 16-bit (E)(E)(P)ROM; prototyping area	$3,200
—	—	1 RS232	OME	none	no	yes	yes	no	prototyping area	$3,600
—	—	1 RS232	—	none	no	yes	yes	no	prototyping area	$4,400
—	—	1 RS232	—	none	no	yes	yes	no	prototyping area	$4,000
—	—	1 RS232	OME	none	no	yes	yes	no	prototyping area	$4,400
—	—	1 RS232	OME	none	no	yes	yes	no	512 kbytes cache; prototyping area	$5,200
—	SCSI, printer	3 RS232, 1 keyboard	OME	AT	MS-DOS	no	yes	no	AT compat., real-time clock	$4,800
—	SCSI, printer	3 RS232	OME	none	yes	yes	yes	no	—	$1,600
—	SCSI, printer	1 RS232	OME	none	yes	yes	yes	no	—	$2,000
—	none	1 RS232	2 SBX	none	no	yes	yes	no	prototyping area	$1,600
—	none	1 RS232	none	none	no	yes	yes	no	prototyping area	$1,440
no	—	2 RS232/422	1 SBX	—	Unix, VRTX	yes	yes	yes	SCSI; opt TODC	$2,653
yes	SCSI, 8 I/O	6 RS232	8/16 SBX	iLBX II	TPIX 5.3.1	yes	VRTX	no	Ethernet interface	—
yes	SCSI	4 RS232	8/16 SBX	iLBX II	TPIX	yes	no	no	Ethernet interface	—
opt	24 in, 24 out	2 RS232	—	—	none	yes	yes	no	8k EEPROM std, 16k opt	$351
opt	24 in, 24 out	2 RS232	—	—	none	no	no	no	16k RAM, (E)(E)PROM opt	$256
opt	24 in, 24 out	2 RS232	—	—	none	no	no	no	same as above	$270
yes	24	2 RS232, 2 RS232/422/485	1 8BHSBX	—	MS-DOS	yes	yes	yes	16-bit wide memory, RTC	—
no	24	1 RS232, 1 RS232/485	1 8-bit SBX	—	MS-DOS	yes	yes	yes	12 CTC	—
yes	10	2 RS232/422/485	1 8-bit SBX	—	CP/M	yes	—	yes	RTC, master/slave	—
no	0	0	—	—	CP/M	yes	—	yes	4 CTC, 6 memory positions	—
yes	0	1 RS485	2 8-bit SBX	—	RMX-51	yes	yes	no	—	$450
no	56 prog lines	1 RS232	none	STD	none	yes	no	no	—	$251
yes	16 prog lines	2 RS232	none	STD	none	yes	no	no	ADC clock/calendar	$379
yes	24 prog lines	2 RS232/485	1 8-bit SBX	STD	none	yes	no	no	same as above	$470
yes	32 prog lines	2 RS232	1 8-/16-bit SBX	STD	none	yes	no	no	clock calendar	$565

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Enterprise Systems 6 Grove St, PO Box 698, Dover, NH 03820 (603) 742-7363										**Circle 351**
10812	8	16	6502	1, 2	no	no	none	1, 2	0	0/32k
10809	8	16	6809	1, 2	no	no	none	1, 2	0	32k
GW Three 7623 Fullerton Rd, Springfield, VA 22153 (703) 451-2043										**Circle 355**
SBC-20	8	24	MC68020	12, 16, 20	no	yes	none	2	—	128k/2M
SBC 95/2	8	16	TMS 9995	12	no	no	none	1.5	—	24k/96k
SBC 95/1	8	16	TMS 9995	12	no	no	none	1.5	—	0/4k
Matrix 1203 New Hope Rd, Raleigh, NC 27610 (919) 833-2000										**Circle 376**
TS9	8	16	6809	1, 2	no	no	none	—	—	0/64
MF9	8	16	6809	1, 2	no	no	1 8-bit	—	—	0/64
SP9	8	16	6809	1, 2	no	no	none	—	—	0/64
CP9	8	16	6809	1, 2	no	no	none	—	—	0/64
Micro-Link 14602 N U.S. Highway 31, Carmel, IN 46032 (800) 428-6155										**Circle 384**
STD202	8	20	68008	8	no	no	none	2	0/0	0/32k
STD203	8	24	68000	8	no	no	none	2	0/0	0/0
STD205	8	16, 20, 24	Z80	4	no	no	none	2	0/0	8k/192k
STD206	8	20	80188	8	no	opt	2 20-bit	2	256k	0/64k
STD245	8	16	8085A	4	no	no	none	2	0/0	0/64k
STD247	8	16	Z80A	4	no	no	none	2	0/64k	0/32k
Micro/Sys 1011 Grand Central Ave, Glendale, CA 91201 (818) 244-4600										**Circle 385**
SB8088	8	20	8088	5, 8	no	opt	none	2	0/0	0/32k
SB8082	8	20	V20	5, 8	no	opt	none	2	0/0	0/32k
SB8020	8	16	Z80	4	no	no	none	1	0/0	0/32k
SB8010	8	16	Z80	2.5, 4	no	no	none	1	0/0	0/32k
Microcomputer Systems 1814 Ryder Dr, Baton Rouge, LA 70808 (504) 769-2154										**Circle 387**
MSI-C988	8	17	80C88	5	no	no	none	—	0/0	0/32k

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
yes	32 prog lines	1 RS232	—	STD	none	opt	no	no	3 28-pin sockets for RAM, (E)EPROM	$190
yes	32 prog lines	1 RS232	—	STD	none	opt	no	no	same as above	$190
yes	3 prog lines	2 async	none	none	PDOS	yes	yes	no	256 kbytes cache; 32-bit wide RAM, 1M EPROM	$764
yes	8 input/ 8 output	2 RS232	none	none	PDOS	yes	yes	no	—	$350
no	8 input/ 5 output	2 RS232/422	none	none	PDOS	yes	yes	no	—	$290
yes	36 I/O lines	2 RS232C/ 423	none	none	none	yes	yes	no	3 16-bit counter/timers; watchdog timer, 1/2 MHz ver. bat/backed clock	$237
no	none	2 RS232	none	none	none	yes	yes	no	1/2 MHz ver.; 3 16-bit counter/timers	$222
no	none	1 RS232C	none	none	none	yes	yes	no	1/2 MHz ver.	$177
no	none	none	none	none	none	no	yes	no	1/2 MHz ver.; on-board watchdog timer	$143
no	2 8-bit	1 RS232, 1 RS422	—	—	PDOS	yes	yes	no	PC communications software avail.	$323
no	—	—	—	—	PDOS	yes	yes	no	Z80 mode 2 interrupts	$287
no	—	—	—	—	CP/M+	yes	no	no	supports Z80 mode 2 interrupts and RETI opcodes	$143
no	8+	1 RS232, 1 RS232/422	1 8-bit SBX	—	—	yes	no	no	—	$348
yes	1 24-bit	1 RS232	none	—	CP/M	yes	no	no	counters, real-time clock	$266
no	8/1	1 RS232	none	—	CP/M	yes	no	no	same as above	$205
yes	2 8-bit ports	1 RS232	—	STD	PC-DOS	yes	no	no	5 8-bit down counters; on-board interrupt cont.; up to 64k EPROM; standalone ROMable C compiler	$215
yes	2 8-bit ports	1 RS232	—	STD	PC-DOS	yes	no	no	5 8-bit counters; up to 64k EPROM; standalone ROMable C compiler	$215
yes	2 8-bit ports	2 RS232	—	STD	CP/M	yes	no	no	4 8-bit counters; standalone ROMable C compiler	$290
yes	—	1 RS232	—	STD	CP/M	yes	no	no	same as above	$155
yes	24 I/O	2 RS232	—	—	none	yes	no	no	1 real-time clock; 32k/64k PROM; 10-bit ADC; 3 16-bit timers	$360

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Microcomputer Systems 1814 Ryder Dr, Baton Rouge, LA 70808 (504) 769-2154										**Circle 387**
MSI-C800	8	16	NSC800	1, 2.5, 4	no	no	none	—	0/0	0/8k
MSI-C850	8	16	NSC800	1, 2.5, 4	no	no	none	—	0/0	0/32k
Mitchell Electronics 8481 Rock Riffle Rd, Athens, OH 45701 (614) 594-8532										**Circle 392**
M/E200	8	16	Z80	2.5, 4, 6	no	no	none	—	0/0	0/64k
M/E 300	8	16	Z80	2.5, 4, 6	no	no	none	—	0/0	0/64k
Mizar 1419 Dunn Dr, Carrollton, TX 75006 (800) 635-0200										**Circle 393**
MZ 77851	8	16	Z80	2.5, 4	no	no	none	—	1k/2k	—/2k
MZ 78785z	8	16	Am9511A	4	no	yes	none	—	—	—
MZ 77855	8	16	Z80	3.68	no	no	none	—	—	256/256k
MZ 77857	8	16	Z80	3.68	no	no	none	—	64k/64k	—
MZ 77858	8	16	Z80	2.5, 4	no	no	none	—	—/16k	—/16k
MZ 77859	8	16	Z80	2.5, 4	no	no	none	—	—/16k	—/16k
MZ 77870	8	16	Z280	8, 10	yes	no	4 20-bit	—	0/768k	—
Moya 9001 Oso Ave, Unit C, Chatsworth, CA 91311 (818) 700-1200										**Circle 398**
132	8	19	HD64180	9.216	yes	opt	2 8-bit	2.3	512k/512k	0/4M
RLC Enterprises 4800 Templeton Rd, Atascadero, CA 93422 (805) 466-9717										**Circle 413**
SBC-188	8	20	80188	5, 8, 10	no	yes	2 8-bit	2	0/0	0/256
SCC-188	8	20	80188	5, 8, 10	no	no	2 8-bit	2	0/0	0/256
SBC-188SL	8	20	80188	5, 8, 10	no	yes	2 8-bit	2	0/0	0/256
SCC-188SL	8	20	80188	5, 8, 10	no	no	2 8-bit	2	0/0	0/256
SBC-186	8, 16	20	80186	5, 8, 10, 12.5	no	yes	2 16-bit	4	0/0	0/256
SBIO-186	8, 16	20	80186	8, 10, 12.5	no	no	2 16-bit	4	0/0	0/256
DSP-320-20SL	16	20	TMS32020/ 320C25	20, 40	no	no	none	10	0/0	0/192
SBC-C188	8	20	80188 CMOS	8, 10	no	no	2 8-bit	2	0/0	0/256
SCC-C188	8	20	80188 CMOS	8, 10	no	no	2 8-bit	2	0/0	0/256
SBC-C186	8, 16	20	80186 CMOS	8, 10, 12.5	no	no	2 16-bit	4	0/0	0/256
SBIO-C186	8, 16	20	80186 CMOS	8, 10, 12.5	no	no	2 16-bit	4	0/0	0/256

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
no	24 I/O	none	—	—	none	yes	no	no	1 real-time clock; 2 2k PROM sites; 16-bit timers	$260
no	none	none	—	—	none	yes	no	no	1 real-time clock; 4 8k PROM sites	$240
opt	IEEE-488	2 RS232	none	none	Forth	opt	no	no	flexible memory mapping	$250
opt	16 prog lines	2 RS232	none	none	Forth	opt	no	no	same as above	$175
no	16 lines	—	—	—	none	no	no	no	—	$180
—	5 8-bit	—	—	—	—	—	—	no	—	$360
—	—	—	—	—	—	—	—	no	—	$160
no	1 8-bit	2 RS232	—	—	—	—	—	no	—	$280
no	2 8-bit	1 RS232	—	—	—	—	—	no	—	$220
no	—	—	—	—	—	—	—	no	—	$155
—	—	3 RS232	—	—	—	—	—	no	256 kbytes of cache	—
no	none	2 RS232, 1 clocked	STD Bus	STD Bus	CP/M, MaxDOS	yes	yes	yes	2 counter/timers; 5V only operation	$396
opt	16 prog lines	1 RS232	—	—	none	yes	no	no	3 16-bit counter/timers; 5 8-bit counter/timers; real-time calendar clock; support software avail.	$332 5 MHz/ $346 8 MHz
opt	none	2 RS232 or 1 RS232/422	—	—	none	yes	no	no	3 16-bit counter/timers; real-time calendar clock; software support avail.	$332 5 MHz/ $346 8 MHz
opt	16 prog lines	1 RS232	—	—	none	yes	no	no	slave processor with I/O interface to STD Bus	$350 5 MHz/ $364 8 MHz
opt	none	2 RS232 or 1 RS232/422	—	—	none	yes	no	no	same as above	$350 5 MHz/ $364 8 MHz
opt	16	1 RS232	—	—	none	yes	no	no	full 16-bit standard; 3 16-bit timers; 5 8-bit timers; real-time clock, software avail.	$374 5 MHz/$388 8 MHz
opt	32	2 RS232 or 2 RS422	—	—	none	yes	no	no	opto 22 compat. parallel interface, real-time clock, software avail.	$388 8 MHz/ $409 10 MHz
—	32	1 serial	—	—	none	—	no	no	slave DSP w/ memory and I/O interface to STD Bus	$416 20 MHz/ $556 40 MHz
opt	16 prog lines	1 RS232	—	—	none	yes	no	no	3 16-bit timers; 5 8-bit timers; real-time calendar clock; software, CMOS	$367 8 MHz/ $381 10 MHz
opt	none	2 RS232 or 1 RS232/422	—	—	none	yes	no	no	3 16-bit timers; real-time calendar clock; software, CMOS	$367 8 MHz/ $381 10 MHz
opt	16 prog lines	1 RS232	—	—	none	yes	no	no	full 16-bit, 3 16-bit timers; 3 8-bit timers; real-time clock, soft-ware, CMOS	$416 to $458
opt	32 prog lines	2 RS232 or 2 RS422	—	—	none	yes	no	no	opto 22 compat. parallel interface; real-time clock; software CMOS	$416 to $458

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Spurrier Peripherals 10513 Le Marie Dr, Cincinnati, OH 45241 (513) 563-2625										**Circle 423**
Z80-II	8	16	Z80	2.5 to 6	no	opt	none	—	—	2k/32k
6809	8	16	6809	1, 1.5, 2	no	opt	none	—	—	2k/64k
68008	8	20	68008	8, 10	no	no	none	—	—	2k/64k
Systek 1027 N Kellogg St, Kennewick, WA 99336 (509) 735-1200										**Circle 433**
8850	8, 16	20	V50	8, 10	no	opt	4	4	128k/512k	32k/128k
8810	8	20	V20	5, 8, 10	no	opt	—	2.5	0	0/64k
8887	8	20	V20	5, 8, 10	no	opt	—	2.5	0	0
8800	8	20	V20	5, 8, 10	no	no	—	2.5	0	0
Timark Microsystems 5220 E 65th St, Indianapolis, IN 46220 (317) 841-6555										**Circle 439**
Rescuer-I	8	16	Z80	2.5, 4	no	no	1	—	—	2k
Versalogic 3888 Stewart Rd, Eugene, OR 97402 (800) 824-3163										**Circle 444**
VL-188-1	8	20	80188	5, 8, 10	no	no	2	1.25	0/0	0/0.5M
VL-188-2	8	20	80188	5, 8, 10	no	no	2	1.25	0/0	0/0.5M
VL-7804	8	16	Z80	4	no	no	none	—	0/0	0/32k
VL-7806	8	16	Z80	2.5, 4, 6	no	no	none	—	0/0	0/128k
Winsystems PO Box 121361, Arlington, TX 76012 (817) 274-7553										**Circle 447**
LPM-SBC50	8, 16	20	V50	8, 10	no	opt	3 16-bit	10	0/0	0/512k
LPM-SBC40	8	20	V40	8, 10	no	opt	3 8-bit	10	0/0	0/512k
LPM-SBC8	8	20	8088	5, 8	no	opt	none	8	0/0	0/64k
LPM-102	8	16	Z 80	4, 6	no	no	none	6	0/0	0/64
LPM-SBC6	8	19	64180	4, 6	yes	no	2 8-bit	6	0/0	0/64k
LPM-SBC5	8	19	64180	4, 6	yes	no	2 8-bit	6	0/0	0/64k
LPM-SBC3	8	16	Z80	4, 6, 8	no	no	none	8	0/0	0/64k
MCM-SBC	8	16	Z80	4	no	no	none	4	64k/64k	0/0

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
no	—	1 RS232	none	—	none	yes	no	no	—	$295
no	—	1 RS232	none	—	flex	yes	no	no	expanded I/O map, 512 ports	$295
no	—	none	none	—	none	yes	no	no	supports 1 M address range via external address bus	$239
yes	parallel	2 RS232/ 1 RS485	—	—	MS-DOS	yes	no	yes	3 16-bit counters; watchdog timer; multiprocessor CMOS	$746
yes	8	1 RS232	1 8-bit SBX	—	MS-DOS	yes	no	no	3 16-bit counters; 9 interrupts CMOS −40 to +85° C	$296
—	none	—	—	—	MS-DOS	yes	no	no	CMOS −40 to +85°C	$169
—	none	—	—	—	MS-DOS	yes	no	no	same as above	$131
no	16 lines	2 RS232	—	—	no	yes	no	—	8 kbytes EPROM	$300
—	16 lines	1 RS232	—	—	—	yes	no	no	3 16-bit timers; 5 8-bit timers	$243
—	16 lines	1 RS422/485	—	—	—	yes	no	no	same as above	$250
—	—	—	—	—	—	no	no	no	3 16-bit timers	$127
—	—	2 RS232	—	—	—	yes	no	no	4 8-bit timers	$168
opt	24 prog	1 RS232, 422/485	1 8-/16-bit SBX	STD Bus	none	yes	no	no	3 16-bit counter/timers; watchdog timer; real-time clock; CMOS; −40 to +85° C oper. temp.	$575
opt	24 prog	2 RS232/422	1 8-bit SBX	STD Bus	none	yes	no	no	ext oper. temp −40 to +85° C; real-time clock; watchdog timer; 3 16-bit counter/timer	$525
opt	none	1 RS232/422	1 8-bit SBX	STD Bus	none	yes	no	no	3 16-bit counter/timer; watchdog timer; ext oper temp −40 to +85° C	$495
opt	none	2 RS232	none	STD	none	yes	no	no	replaces DY-4 DSTD-102 board; avail. in CMOS for extended temp operation	$295
opt	24 prog lines	2 RS232/422	none	STD	none	yes	no	no	2 16-bit timers; watch-dog timer; Z80 code compat.; all CMOS ext. temp. avail.	$395
opt	none	4 RS232	none	STD	none	yes	no	no	same as above	$395
opt	16 prog lines	2 RS232	none	STD	none	yes	no	no	4 timers; watchdog timer; all CMOS ext. temp. −40 to +85° C avail.	$265
no	none	2 RS232	none	STD	CP/M 2.2	yes	no	no	floppy disk controller on-board; complete system on a card	$695

Winsystems PO Box 121361, Arlington, TX 76012 (817) 274-7553 **Circle 447**

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
MCM-7815	8	16	8085	6	no	no	none	6	0/0	0/32k
MCM-CPU2A	8	16	Z80	4, 6, 8	no	no	none	8	0/0	0/64k
LPM-CPU3A	8	16	NSC-800	2.5, 4	no	no	none	4	0/0	0/64k
LPM-8088	8	20	8088	5	no	no	none	5	0/0	0/0

XYZ Electronics RR 12, Box 322, Indianapolis, IN 46236 (317) 335-2128 **Circle 448**

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
CPU-9A	8	16	68B09	1, 2	no	no	none	—	0/0	0/64k
CPU-68K8	8	20	68008	10, 12	no	no	none	—	0/0	0/64k

Ziatech 3433 Roberto Ct, San Luis Obispo, CA 93401 (805) 773-5854 **Circle 453**

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
ZT 8808/8809	8	20	NEC V20 (8088)	5/8	no	opt	none	—	0/0	8k/392k
ZT 8816/8817	8, 16	20	NEC V50 (80186)	5/8	no	opt	1 20-bit	—	512k/512k	64k/64k
ZT 8806/8807	8	20	8088	5/8	no	opt	none	—	0/0	0/128k
ZT 8814/8815	8	20	80188	5, 8	no	no	2 20-bit	—	0/0	0/32k
ZT 8830	8	20	8088	8	no	no	none	—	0/0	8k/32k

Ziltek 1651 E Edinger Ave, Santa Ana, CA 92705 (714) 541-2931 **Circle 454**

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
ASTD 101	8	16	Z80A	4	no	—	—	—	0/0	2k/32k
ASTD 118	8	16	Z80A	4	no	—	—	—	0/0	0/0
ASTD 152	8	16	Z80A	4	no	—	—	—	0/0	2k/32k
ASTD 153	8	20	64180	6.144	no	—	2	—	0/0	256k/512k
ASTD 154	8	20	64180	6.144	no	—	2	—	0/0	64k/64k
ASTD 158	8	16	Z80A	4	no	—	—	—	0/0	0/0
ASTD 801	8	20	8088	5	no	opt	—	—	0/0	8k/32k
ASTD 501	8	16	Z80C	4	no	—	—	—	0/0	4k/32k

■ STE Bus

Arcom Control Systems Unit 8, Clifton Rd, Cambridge, U.K., CB1 4WH **Circle 317**
U.S. Distributor (Val-Tech) (302) 738-0500

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
SCPC88	8	20	8088	4.77, 7	no	opt	4 8-bit	—	256k	—
SC280	8	20	Z280	10	yes	no	4 8-bit	—	—	0/96k

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
opt	none	none	none	STD	none	no	no	no	replaces Pro-Log 7805, 7815, 78C15; ext. temp. operation −40 to +85° C	$185
opt	none	none	none	STD	none	yes	no	no	replaces Mostek (Mizar) MDX-CPU2A and MDX-CPU2B	$185
opt	22 prog	none	none	STD	none	no	no	no	2 16-bit counters; watchdog timer; calendar clock; −40 to +85° C	$295
—	none	2 RS232	none	STD	none	yes	no	no	−40 to +85° C operation, 2 mA serial channels	$395
yes	none	1 RS232	STD Bus	—	OS-9	yes	yes	no	3 counter/timers (16-bit); real-time clock; custom mem map	$244
yes	8 single-bit	1 RS232	STD Bus	—	OS-9	yes	yes	no	2 counter/timers (8-bit); real-time clock	$371
opt	12 prog lines	1 RS232C, RS422A/485	none	none	STD DOS	yes	yes	yes	256-kbyte EEPROM capacity, ac/dc power fail protection	$531/561
yes	none	1 RS232C, RS422A/485	none	none	STD DOS	yes	yes	no	same as above	$1,169/1,199
opt	16 prog lines	1 RS232C, RS422A/485	none	none	STD DOS	yes	yes	no	320-kbyte ROM capacity EEP	$256/286
no	none	none	1 SBX	none	none	yes	no	no	64-kbyte ROM capacity EEP	$277/307
no	16 prog lines	1 RS232, RS422/485	1 SBX	none	STD DOS	yes	no	no	slave processor capability	$288
—	16 lines	—	—	—	—	yes	yes	—	1 CTC	$136
—	printer	1 RS232C	—	—	CP/M-80	yes	yes	—	—	$162
—	—	2 RS232C/ TTL	—	—	—	yes	yes	—	—	$169
—	printer	—	in-house	—	CP/M-80	yes	yes	—	—	$345
yes	16 lines	2 RS232C/ TTL	in-house	—	C/2	yes	yes	—	—	$645
—	—	—	—	—	—	yes	yes	—	—	—
—	—	—	—	—	—	yes	no	—	—	$164
—	16 lines	—	—	—	—	yes	yes	—	—	$168
—	—	—	—	—	MS-DOS, PC-DOS	no	no	no	STE PC	$548
—	—	2 RS232, 1 RS485	—	—	CP/M+	yes	—	no	up to 96k RAM; up to 128k EPROM	$468

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Arcom Control Systems Unit 8, Clifton Rd, Cambridge, U.K., CB1 4WH **U.S. Distributor (Val-Tech)** (302) 738-0500 **Circle 317**										
SC008	8	20	68008	8	no	no	none	—	—	0/64k
SC88	8	20	80188	8	no	no	2 8-bit	—	64k/256k	—
DSP Design LTD Unit 1, Apollo Studios, Charlton Kings Rd, London, NW5 2SB 44-1-482-1773 **U.S. Distributor (Val-Tech)** (302) 738-0500 **Circle 339**										
SV25	8	20	V25	8	no	no	2	5	0	32k/368k
SX180	8	19	HD64180	6, 9	yes	no	2	5	0/256k	8k/32k
SP180	8	19	HD64180	6, 9	yes	no	2	5	0	8k/96k
SZ801	8	20	Z80	4, 6	no	no	none	5	0	8k/96k
Val-Tech PO Box 9086, Newark, DE 19714 (302) 738-0500 **Circle 443**										
vt1088	8	20	80C88	5	no	opt	none	5	—	8k
■ S-100 Bus										
Fulcrum Computer Products 459 Allan Ct, Healdsburg, CA 95448 (707) 544-0202 **Circle 354**										
MPUZ	8	16, 24	Z80H	8	no	no	—	—	—	—
IBS 5915 Graham Ct, Livermore, CA 94550 (415) 443-3131 **Circle 362**										
Slavenet 186	16	24	80186	10, 12	—	—	3 16-bit	2	512k/1M	0/0
■ NuBus										
Mercury Computer Systems 600 Suffolk St, Lowell, MA 01854 (508) 458-3100 **Circle 379**										
MC3200NU	32	32	XL8032	10	—	yes	1 32-bit	25	2/8	—
Yarc Systems 5655 Lindero Canyon Dr, Suite 721, Westlake Village, CA 91362 (818) 889-4388 **Circle 451**										
McCray	32	32, 24	Am29000 (RISC)	20, 25	yes	opt	1	5	2/2	0.5/2.5
■ G-64										
Gespac 50 W Hoover Ave, Suite 2, Mesa, AZ 85202 (602) 962-5559 **Circle 359**										
GESSBS-6	16, 32	24	68000/68010	8/16	yes	—	—	20	0/0	256k/512k
GESSBS-4A	8	15	6809	1/2	yes	—	—	20	0/0	64k
GESSBS-5	16	15	8088	5	yes	—	—	20	64k	64k/128k
GESBDS-6	16, 32	24	68000/68010	8/16	yes	—	—	20	0/0	256k/512k

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
—	—	2 RS232 or 1 RS232/1 RS485	—	—	OS-9/68k	yes	yes	no	up to 64k RAM; up to 124k ROM	$421
—	—	2 RS232	—	—	Concurrent DOS	yes	—	—	bus arbiter	$543 to $936
no	24	2 RS232	no	no	Appcom, CDOS	yes	yes	no	—	$450
yes	none	2 RS232	1 prop	no	CP/M+, Z-system	yes	yes	no	—	$420
no	40 lines	2 RS232	no	no	CP/M+, Z-system	yes	yes	no	—	$360
no	32 lines	2 RS232	no	no	CP/M+, Z-system	yes	yes	no	—	$270
no	—	—	8087 math coprocessor	—	none	no	no	no	exCMOS; STEbus system controller funct.	$465
yes	1 printer	2 RS232	none	none	—	yes	yes	no	—	$225
—	none	2 RS232	1 SCSI	—	PNet TurboDOS	yes	no	yes	—	$495
no	—	—	—	prop	multifinder	yes	yes	no	64 kbytes cache	—
no	—	—	prop 32-bit	Nubus	Mac II	yes	no	yes	all memory full speed; up to 1 wait state	$4,000
yes	20 prog	2 RS232	—	—	yes	yes	yes	—	3 16-bit timers; clock/calendar	$676
yes	32 parallel lines	1 RS232	—	—	yes	yes	yes	—	multiple memory maps	$421
—	24 prog	2 RS232	—	—	complete devel.	yes	yes	—	multiple memory maps timers/clock/calendar	$506
yes	20 prog	2 RS232	—	—	yes	yes	yes	—	3 16-bit timers; clock/calendar	—

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Analogic/CDA 8 Centennial Dr, Peabody, MA 01961 (617) 246-0300										**Circle 313**
MicroMSP-4	16	22	68020	20	—	opt	4	3	0.5M/4.5M	64/256
■ Bitbus										
Datem 148 Colonnade Rd, Nepean, Ontario, Canada K2E 7R4 (613) 225-5919										**Circle 344**
530 Series	8	16	8044	12	no	no	none	1	0/0	40k/64k
220	8	16	8044	12	no	no	none	1	0/0	16k/64k
330	8	16	8044	12	no	no	none	1	0/0	16k/64k
335	8	16	8044	12	no	no	none	1	0/0	16k/64k
■ AMS Bus										
Micro Industries 691 Greencrest Dr, Westerville, OH 43081 (614) 895-0404										**Circle 381**
mAMS-M6-A8	8, 16	24	8086	8	—	opt	2 8-bit	—	0	0/32k
mAMS7-A8	8, 16	24	8086	8	—	opt	2 8-bit	—	0	0/32k
mAMS-M16-A81	8, 16	24	80186	8	—	—	2 8-bit	—	512k/512k	0/0
mAMS-M26-A81	8, 16	24	80286	8	—	—	4 8-bit	4	1M/1M	0/0
mAMS-M36	8, 16	24	80386	16	—	opt	8 32-bit	20	2M/2M	0/0
■ SMP Bus										
Micro Industries 691 Greencrest Dr, Westerville, OH 43081 (614) 895-0404										**Circle 381**
mSMP-E14-AX	8	24	8085A	3, 5	no	—	none	—	0/0	0/16k
mSMP-E17-AX	8	24	8088	5, 8	no	opt	4 8-bit	—	0/0	0/0
mSMP-E18-A8	8	24	80188	8	no	yes	2 8-bit	1	0/0	0/96k
mSMP-E19-A84	8	24	80188	8	no	no	2 8-bit	1	512k/512k	0/0
■ Exorbus										
Micro Industries 691 Greencrest Dr, Westerville, OH 43081 (614) 895-0404										**Circle 381**
M68MM01A2	8	16	6800	1	no	no	none	1	0	1k
M68MM17	8	16	6809	1	no	no	none	1	0	0/40k
M68MM19	8	16	6809	2	no	no	none	1	0	2k/34k

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
no	—	1 RS232	1 for memory	none	VMS	—	yes	—	coprocessor for μVAX system w/peak arith. rate of 20 MFlops	$9,900
yes	64 digital/ 6 analog	0	1 8-bit SBX	—	Basic, C, Ladder Logic, assembly	yes	yes	yes	3 memory sites, module sockets	$400 to $1,200
no	printer port	1 RS232 & 1 RS422 or 2 RS232	1 8-bit SBX	—	Basic, C, assembly	yes	yes	yes	3 memory sites	$390 to $470
no	48	none	1 8-bit SBX	—	yes, Basic,C, assembly	yes	yes	yes	same as above	$350 to $430
no	24	none	1 8-bit SBX	—	yes, Basic, C, assembly	yes	yes	yes	same as above	$280 to $360
no	24 prog lines	1 RS232	none	SMP	no	no	no	no	3 counter/timers; 8089 I/O processor	$1,720
no	—	1 RS232	2 SBX 8-/16-bit	SMP	no	no	no	no	3 counter/timers	$965
no	—	1 RS232	none	SMP	no	no	no	no	ECC; 2 counter/timers; 2 EPROM sites	$2,020
no	—	1 RS232	none	SMP	no	no	no	no	3 counter/timers; 2 EPROM sites	$2,995
no	—	1 RS232	32-bit OME	SMP	no	no	no	no	64 kbytes cache opt; 2 EPROM sites; 82380 controller	$5,895
yes	16 prog lines	1 RS232	none	none	no	no	no	no	5 counter/timers; 8256 MUART	$650/$670
no	—	—	none	none	no	no	no	no	—	$810
no	16 input/ 8 output	2 RS232	none	none	no	no	no	no	3 counter/timers; watch-dog; Z8530 serial cont.	$890
no	1 printer, 8 prog lines	2 RS232	none	none	no	no	no	no	3 counter/timers; Z8530 serial cont.	$1,215
no	32 prog lines	1 RS232C	none	none	none	no	no	no	4 (E)(P)ROM/RAM sites	$415
no	16 prog lines	2 RS232C	none	none	none	no	no	no	5 (E)(P)ROM/RAM sites	$415
no	1 printer/prog	1 RS232C/ 422/423	none	none	none	yes	no	no	4 (E)(P)ROM/RAM sites; counter/timer	$585

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Micromint 4 Park St, Vernon, CT 06066 (203) 871-6170										**Circle 389**
BCC180	8	20	HD64180	9.216	yes	no	2 8-bit	1.5	0/256k	32k/128k
BCC52	8	16	8052	11.0592	no	no	none	0.25	0/0	8k/48k

■ Xbus

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Micromint 4 Park St, Vernon, CT 06066 (203) 871-6170										**Circle 389**
SB180FX	8	20	HD64180	9.216	yes	no	2 8-bit	1.5	256k/4M	0/0

■ Unibus

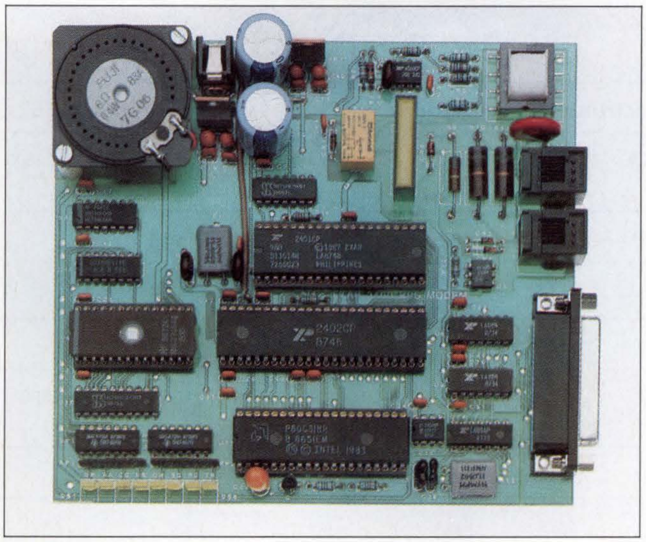
Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speeds (MHz)	MMU	Math coprocessor	DMA channels (no. and width)	Max bus trans. rate (Mbytes/s)	DRAM min/max (bytes)	SRAM min/max (bytes)
Nissho Electronics 17320 Red Hill Ave, Suite 200, Irvine, CA 92714 (714) 261-8811										**Circle 402**
N1100 Plus	16	18	J11	15	yes	yes	1 16-bit	4	1M/4M	0/0

Battery-backed	Parallel lines/ports	Serial ports (no. and type)	Daughterboard expansion (no. and type)	Interboard expansion	Operating system drivers	Debug monitor	Real-time executive	Mailbox interrupts	Other features	OEM price (in 100s)
yes	48/6	2 RS232/ 422/485, 1 sync	—	—	none	yes	no	no	multitasking Basic compiler, EPROM prog	—
yes	24/3	2 RS232	—	—	none	no	no	no	Basic interpreter, EPROM programmer on-board	—
no	24/3	2 RS232, 1 sync	—	—	2 system (CP/M)	yes	no	no	floppy interface, SCSI	—
yes	—	2 RS232	none	none	DEC compat.	yes	no	no	—	$8,950

INTEGRATED CIRCUITS

2,400-bit/s modem ICs add functionality, preserve design flexibility

John H. Mayer, Senior Associate Editor



V.22bis-compatible chip sets such as Exar's XR-2400 give designers maximum flexibility by supplying complete modem functionality in two compact packages. The set consists of the XR-2401, a general-purpose digital signal processor, and the XR-2402 analog front-end. Rather than use a dedicated controller, the chip set is designed to interface to popular off-the-shelf parts such as the 8051 and Z8.

Less than a year after a series of highly publicized product introductions, IC vendors are seeing a rising interest in modem chip sets capable of 2,400-bit/s operation. "They're on a steep climb right now," says Jim Lange, application engineering manager for Exar (San Jose, CA). Driving that demand is a combination of factors led by decreasing chip set prices and an increased recognition that higher speed modems deliver savings in communications charges and time. "Communications speed is a narcotic, just like process and cycle time and how much memory you have," says Jack Humphrey, general partner for Telequality Associates (Golden, CO), an independent consulting firm.

Designers and users are demanding chip sets that comply with the international handshake and interface standards outlined in the V.22bis specification from the Consultative Committee on International Telephone and Telegraph (CCITT). Equally welcome is the opportunity compliance provides to offer communications protocols capable of meeting a wide range of communications hardware and software. At the same time, the V.22bis-compatible, 2,400-bit/s ICs are preserving their ties to the popular Bell 212A standard for 1,200-bit/s operation.

Despite this growing consensus on standards and continuing improvements in telephone-line quality and modem chip set performance, the 2,400-bit/s market isn't perceived by all as a sure bet. Some analysts expect an eventual fallout in the 2,400-bit/s arena, with only a few of the V.22bis IC products finding commercial success. Others predict that the 2,400-bit/s level will function only as an interim stop for the low-cost modem market and that higher speeds offer more promise.

These reservations have influenced product-line evolution with some IC vendors. A number of major suppliers are sticking with the lucrative 1,200-bit/s market for the forseeable future and have opted to either drop initial 2,400-bit/s product development efforts or to simply stay out of the 2,400-bit/s market altogether.

Motorola (Austin, TX), for example, offers a line of 300- and 1,200-bit/s modem chips, but has abstained from delivering higher speed ICs. And after fielding its 2,400-bit/s S3500/S3551 chip set, Gould Semiconductor (Pocatello, ID) withdrew support for the product. In addition, after building anticipation for a planned 2,400-bit/s chip set heavily dependent on digital signal processing techniques, Advanced Micro Devices (Sunnyvale, CA) last year terminated the project. AMD recently indicated, however, that it will be sampling a new product in this class by the end of the year.

The chips and chip sets listed in the following table offer fairly complete solutions and let designers with little prior modem design experience build complete modems in a wide variety of systems. Aside from error correction, many of the design issues outside the chip sets themselves are identical whether designing a 1,200- or a 2,400-bit/s modem.

■ Partitioning a primary distinction

The primary distinction among 2,400-bit/s chip sets is how they partition modem functions. Product solutions range from four chips including a dedicated microcontroller down to a single chip capable of integrating both analog switched-capacitor filters and DSP circuitry on the same die. Although greater levels of integration supply more compact, complete solutions and often simplify a design task, they can also restrict a designer's flexibility.

Vendors use a wide spectrum of modem chip technologies to achieve varying levels of integration. Some manufacturers rely on a largely digital approach, claiming that at speeds of 2,400 bits/s and above, the demand for adaptive equalization—a technique in which the modem adjusts in real time to changing telephone-line quality—can best be served by this approach. The DSP 2400 chip set from Texas Instruments (Dallas, TX), for example, combines ROM-coded versions of the TMS320 DSP and the TMS7042 8-bit microcontroller. Other manufacturers allocate adaptive equalization and error-correction functions to a microcontroller and implement basic

■ 2,400-BIT/S MODEM ICS

Model	CCITT compatibility	Bell compatibility	DTMF generation	UART on-chip	AT command set	Interfaces	Diagnostics	Power consumption (mW)	Packaging	Price	Comments
Cermetek Microelectronics 1308 Borregas Ave, Sunnyvale, CA 94087 (408) 752-5000											**Circle 100**
CH1780	V.22, V.22bis	212A, 103	yes	yes	yes	S, TTL	analog, remote loops	2, 100	2.5×3.7 in.	$209	self-contained module
Exar 2222 Qume Dr, PO Box 49007, San Jose, CA 95161 (408) 434-6400											**Circle 101**
XR2400	V.22bis, V.22	212A	yes	no	yes	S, P	loopbacks	450	plastic DIP, PLCC	$22.50	two-chip set
Intel 1900 Prairie City Rd, Folsom, CA 95630 (916) 351-6289											**Circle 102**
89024	V.21, V.22, V.22bis	212A, 103	yes	no	yes	S	—	800	—	$27	two-chip set
Oki Semiconductor 650 N Mary Ave, San Jose, CA 94086 (408) 720-1900											**Circle 103**
PC Modem 224	V.22bis	212A	yes	no	yes	P	—	400	DIP, FP	$40	four-chip set
Rockwell International 4311 Jamboree Rd, Newport Beach, CA 92658 (714) 833-4839											**Circle 104**
R2424	V.22 A/B, V.22bis	212A, 103	yes	no	no	S,P	analog, digital, remote	2,300	DIPs, modules	$34	three-chip set
SGS-Thomson 1000 E Bell Rd, Phoenix, AZ 85022 (602) 867-6100											**Circle 105**
TS7524	V.21, V.22, V.22bis,V.23	212A, 103	yes	no	no	P	—	1,700	plastic DIPs	$40	four-chip set
TS7525	V.21, V.22, V.22bis, V.23	212A, 103	yes	no	no	P	—	700	plastic DIPs	$35	two-chip set available 4Q88
Sierra Semiconductor 2075 N Capitol Ave, San Jose, CA 95132 (408) 263-9300											**Circle 106**
SC11006/ SC11011	V.21, V.22, V.22bis	212A, 103	yes	yes	yes	S, P	full diagnostics	150/ 250	28-pin DIP, PLCC/ 68-pin PLCC	$59.50	two-chip set, MNP (classes 1-5)
Silicon Systems 14351 Myford Rd, Tustin, CA 92680 (714) 731-7110											**Circle 107**
73K224/ K224L	V.21, V.22, V.22bis	212A, 103	yes	no	no	S, P	full diagnostics	100/ 30 (L)	22-pin DIP, PLCC	$37.04/ $41.36	single chip
73D2402	V.21, V.22, V.22bis	212A, 103	yes	no	yes	S	full diagnostics	600	40-pin, 28-pin DIP, PLCC	$41.73	three-chip set
Texas Instruments Semiconductor Group, PO Box 809066, Dallas, TX 75380 (800) 232-3200											**Circle 108**
DSP2400 modem	V.22 A/B, V.22bis	212A, 103	yes	no	yes	S	—	600	—	$27	three-chip set
Xecom 374 Turquoise St, Milpitas, CA 95035 (408) 945-6640											**Circle 109**
XE2400	V.21, V.22, V.22bis	212A, 103	yes	no	yes	S	analog, digital, remote digital	800	module	$199	component modem with DAA
XE2400A	V.21, V.22, V.22bis	212A, 103	yes	no	yes	S	same as above	800	module	$179	asynch operation only
XE2400MNP	V.21, V.22, V.22bis	212A, 103	yes	no	yes	S	same as above	800	module	$249	MNP protocols, production 4Q88

Key: DAA=data-access arrangement; DIP=dual in-line package; DTMF=dual-tone multifrequency generator; FP=flatpack; MNP=Microcom Networking Protocol; P=parallel; PLCC=plastic leaded chip carrier; S=serial; UART=universal asynchronous receiver-transmitter

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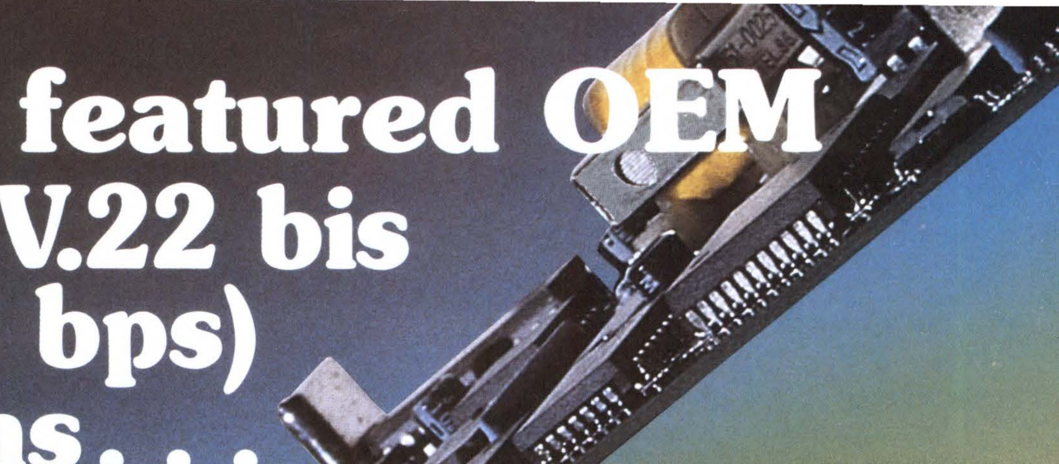

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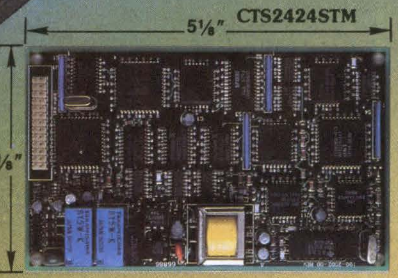
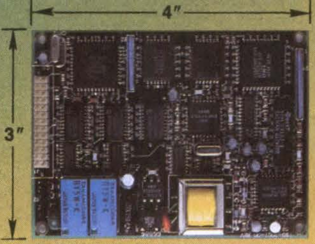
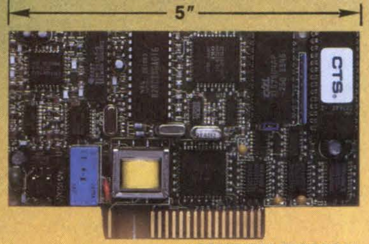
- **Low power**
- **Standard or custom**





CTS2424STH



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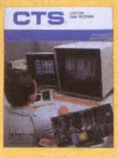

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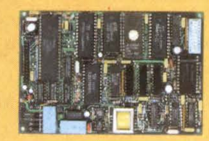

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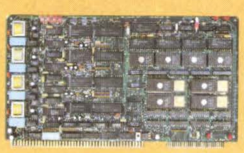

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Half-Pak #24 IBM† PC Compatible Half Card 2400 bps Modem
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modem functions such as filtering, modulation and demodulation in less costly, switched-capacitor technology.

The first manufacturer to convert CCITT's V.22bis specs into silicon was Rockwell International (Newport Beach, CA). Also compatible with V.22 and Bell 212A and 103 standards, the three-chip R2424 set supports links to both RS-232 and 8-bit microprocessor bus interfaces. Rockwell placed all filtering functions on a single part that uses analog and switched-capacitor technology. DSP and programmable functions for operation with the CCITT and Bell protocols are spread over two digital chips.

A somewhat similar approach was taken by Oki Semiconductor (Sunnyvale, CA) last year on its V.22bis 2,400-bit/s modem. Oki's four-chip set, which provides an 8-bit data bus, operates in full- or half-duplex mode. One of the chips, the M80C51-58 controller, performs modulation and converts transmitted data from synchronous-to-synchronous mode. The M6950 analog front-end supplies digital-to-analog (D-A) conversion, filters the result and outputs an analog signal. It also filters incoming analog signals, performs analog-to-digital (A-D) conversion and passes the result to the DSP for demodulation. The chip set adds a separate DSP, also designed by Oki, and a gate array capable of handling synchronous-to-asynchronous conversions and phase-locked loop.

■ On-board intelligence added

To help designers ensure software compatibility with handshake protocols or error-correction algorithms, IC vendors add on-board intelligence to simplify the software interface. Intel's 89024 two-chip set, for example, includes the 89026 application-specific processor. Based on Intel's 8096 architecture, the 16-bit processor implements a customized command set including functions such as diagnostics, echo suppression, dual-tone multifrequency generator (DTMF) autodialing and Hayes protocols. A second analog chip adds a modulator/demodulator, filtering, and two-to-four wire interface circuits.

Like the Intel set, Exar's V.22bis-compatible two-chip set merges all digital functions into a single IC. The XR-2401 provides modulation/demodulation, a carrier detect circuit, a scrambler/descrambler, a DTMF generator and an adaptive equalizer. The XR-2402 includes linear analog functions such as A-D and D-A converters for getting into and out of the DSP chip, programmable gain amplification, asynchronous-to-synchronous and synchronous-to-asynchronous conversion, and guard-tone amplification for CCITT applications.

Exar's chip set differs from the Intel set in that it's designed to tie to a general-purpose microcontroller. "These two ICs perform the entire modem function," says Exar's Lange. "Rather than share modem and controller functions within the controller, in our system the controller only performs control functions." The company offers a PC AT command set designed to sit in EPROM and support an 8031 microcontroller.

> ***"Communications speed is a narcotic, just like process and cycle time and how much money you have."***
>
> *—Jack Humphrey, Telequality Associates*

Exar's use of a standard, off-the-shelf microcontroller simplifies initial programming and eases product modification, according to Lange. "Everybody wants to add commands to differentiate their modem, and the Hayes command set is a kind of moving target anyway," he says. "The way we split the functions gives designers total flexibility if they want to add Microcom Networking Protocol, for example, or make simple changes to the controller."

■ "Open" approach adds flexibility

Rather than offer one dedicated controller, Sierra Semiconductor (San Jose, CA) offers designers a choice in its two-chip set. For the widest design flexibility, the company provides an "open-architected" controller—the SC11011. Capable of accommodating parallel and serial bus applications, the SC11011 offers a universal asynchronous receiver-transmitter (UART), an adaptive equalizer, carrier detection and data decoding. Firmware resides in external ROM or EPROM. "Instead of a closed system where you can address only internal memory, and where everything in that internal memory is inaccessible in terms of adding value, the designer can add certain features and functions in an open-architected approach," says Bill Nicholson, director of standard parts marketing.

For designers not requiring that kind of flexibility, Sierra offers two dedicated controllers. The SC11019 is optimized for parallel bus operations such as add-in cards for the IBM PC. For external or stand-alone product designs configured with an RS-232 serial interface, Sierra provides the SC11020. Both controllers add a UART, 16 kbytes of ROM and the industry-standard AT command set in on-board firmware.

■ Sierra stays analog

To minimize silicon area, Sierra uses switched-capacitor filter analog techniques rather than DSP in its SC 11006 modem chip. "We were able to use lower resolution A-D and D-A converters because we've done all of the predetection operations in the analog domain," says Nicholson. "It allows us a more efficient solution in silicon." Built in an advanced CMOS process, the SC11006 adds an integrated DTMF/guard-tone generator; a call-progress monitor; analog, digital and loopback diagnostics; and a programmable audio output port.

One of the most highly integrated modem solutions comes from Silicon Systems (Tustin, CA). The K224 incorporates a DSP on the same chip with other modem functions. Driven by an 11-MHz clock, the DSP interfaces directly to surrounding transmission circuitry and executes instructions at rates of 5.5 Mips. Memory-mapped registers link the K224's analog circuitry with the DSP.

This space-saving device supports V.22bis, V.22, V.21, and Bell 212A and 103 protocols for synchronous and asynchronous operation. The chip can be controlled by popular off-the-shelf controllers via an 8-bit multiplexed address/data bus or an optional serial command bus. ■

The MC88000 RISC Multibus II Single Board Computer

The TP880M from Tadpole

•The Philosophy•

The TP880M design brings together the outstanding performance of the Motorola MC88000 RISC processor set, the power of the full MultibusII/iLBX II interfaces, an MC68000/68440 I/O subsystem with SCSI and Ethernet, and the specially designed Tadpole 88000 RISC optimising C Compiler. The result is an outstanding product that offers users the very best of current SBC technology.

•The Specification•

- MC88100 RISC processor (20-33MHz)
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- 4-16Mb Nibble mode parity-protected DRAM
- iPSB interface implemented using the Intel Message Passing Coprocessor (MPC)
- iLBX interface and iSBX connector
- I/O Subsystem MC68000/68440 CPU/DMA provides SCSI 4 RS232 ports • Up to 128Kb EPROM
- 64Kb SRAM and optional ETHERNET networking
- TP-IX V.3.1*
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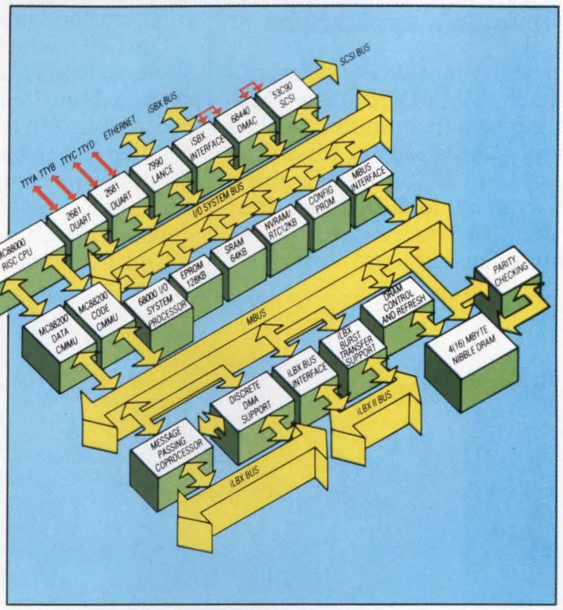
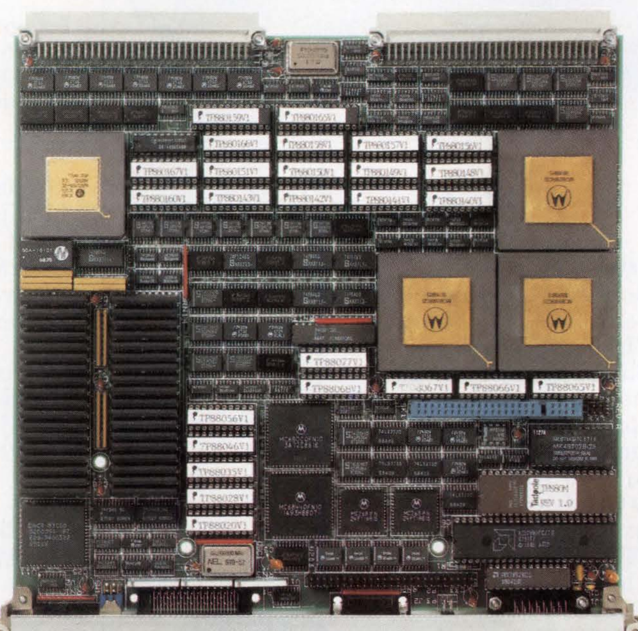
CIRCLE NO. 36

•The Design•



•The Evidence•



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T A D P O L E

COMPUTERS AND SUBSYSTEMS

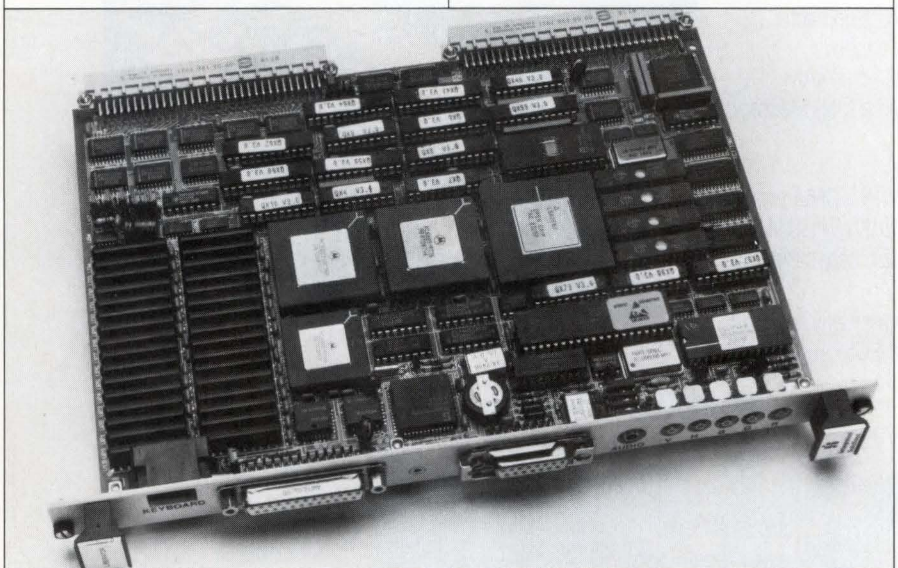
Single-board computer targets real-time Unix applications

Based on the Motorola 68030 microprocessor, the VME-68K30 is a VMEbus, single-board computer with a processing speed of up to 7 Mips. The board comes in a 16.67-MHz and a 25-MHz version and includes four 16-bit counter/timers with three designated for external interface. These counters, which can be either free-running or wrap-around, can be read without interruption.

The CPU, which acts as master and slave on the VMEbus and VME subsystem bus (VSB), supports multiprocessing. Up to eight CPUs can be coupled in the backplane to perform processor interrupts and interprocessor memory access and support independent soft and hard resets.

Eight on-board RS-232C serial ports allow direct connection to the CPU without the need for terminal multiplexers. The board supports up to four graphics displays through the X Window System and features 512 kbytes of memory and a cache that contains 64 kbytes of external memory. The standard memory management unit that's normally part of the 68030 microprocessor is disconnected to increase performance in real-time applications.

Specifically designed for Unix applications, the single-board computer provides virtual direct memory access, letting noncontiguous memory on the VSB appear contiguous on the VMEbus. The board also supports VMEbus burst mode, alleviating I/O bottlenecks and allowing the use of next-generation intelligent peripheral controllers. Standard networking protocols, such as Network File System and Transmission Control Protocol/Internet Protocol are supported by the CPU, which runs on the manufacturer's dual-universe Unix. Prices start at $4,995.



Integrated Solutions
1140 Ringwood Ct
San Jose, CA 95131
Circle number 152

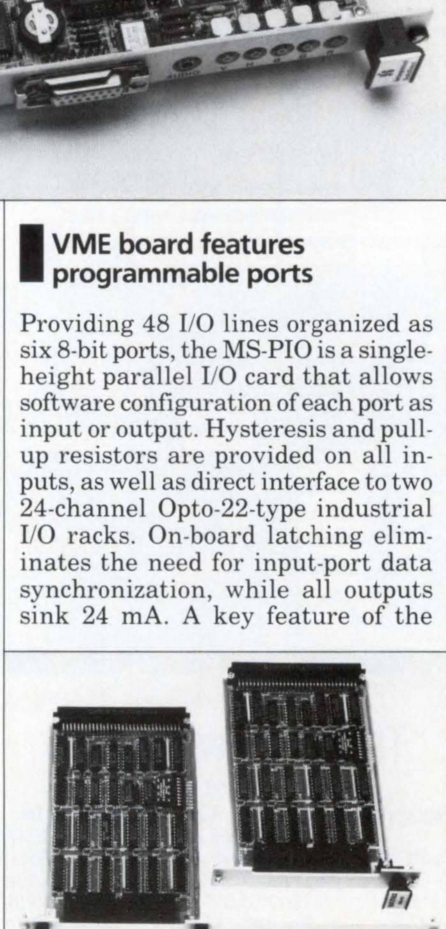
Real-time system runs on AT-bus hardware

A family of single-processor systems, System 120 is based on the manufacturer's iRMX II operating system for use in real-time applications. Using an 80386 microprocessor-based, AT-bus hardware platform, the family supports a range of real-time applications, including medical diagnosis, light industrial automation and financial data acquisition. The OEM platform version comes in two models, each with 2 Mbytes of RAM. One is diskless; the other has a 40-Mbyte disk and a 360-kbyte floppy. The development version is available on hard-disk models only and includes a toolkit with compilers, a debugger, a text editor and documentation. Prices start at $3,800.

Intel
3065 Bowers Ave
Santa Clara, CA 95052
Circle number 153

VME board features programmable ports

Providing 48 I/O lines organized as six 8-bit ports, the MS-PIO is a single-height parallel I/O card that allows software configuration of each port as input or output. Hysteresis and pull-up resistors are provided on all inputs, as well as direct interface to two 24-channel Opto-22-type industrial I/O racks. On-board latching eliminates the need for input-port data synchronization, while all outputs sink 24 mA. A key feature of the board is the output control register, which allows dynamic reconfiguration of each port for bidirectional data transfers and determination of port direction status for all six ports. The card is priced at $345.



Matrix
1203 New Hope Rd
Raleigh, NC 27610
Circle number 160

32-bit CPU board supports master/slave VSB transfers

The GMSV07-VSB-1 is a 25-MHZ, 68020-based single-board computer with a 68881 coprocessor for 32-bit operation, up to 1 Mbyte of zero-wait-state dual-ported static RAM, two multiprotocol serial ports and a configuration controller with timers. A mezzanine module lets any CPU be master/slave and look into every other CPU in the system, while providing memory-card access through

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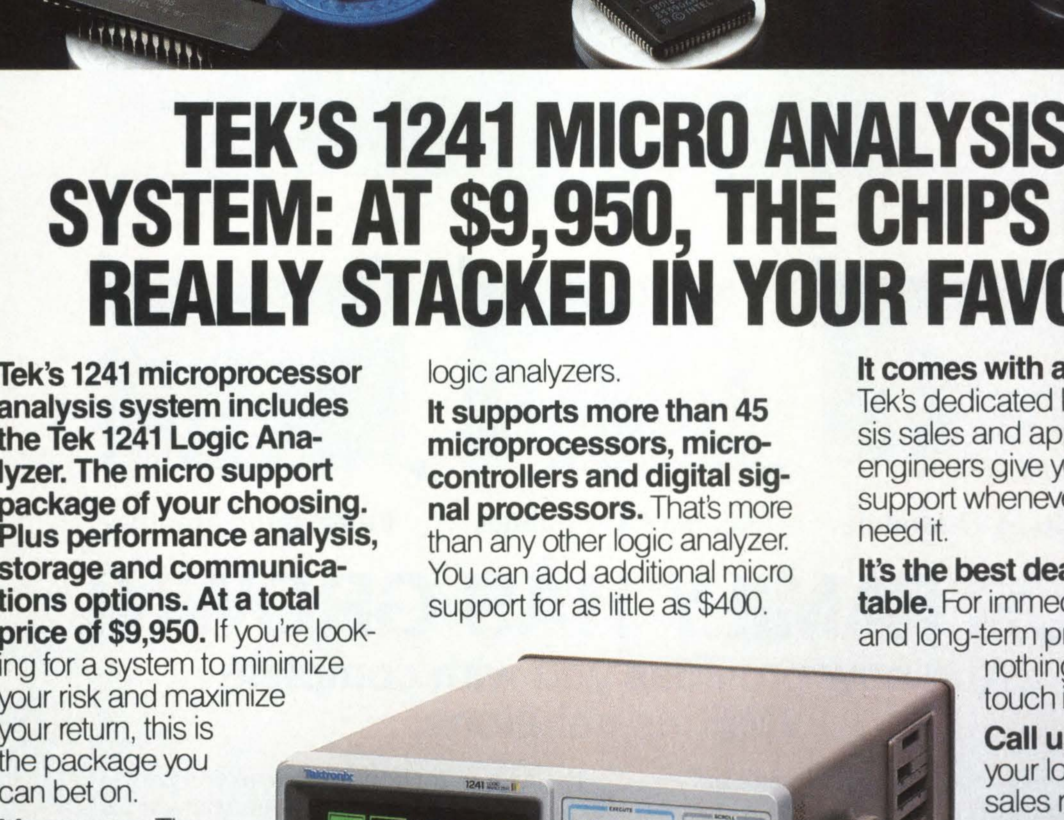

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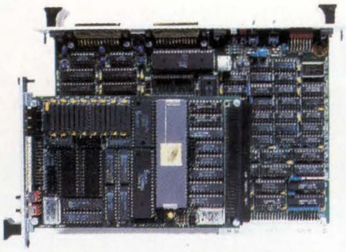
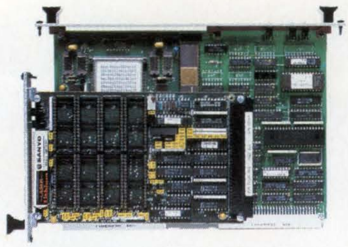
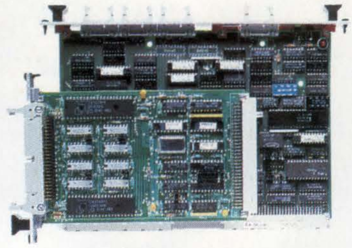
CIRCLE NO. 37 FOR LITERATURE
CIRCLE NO. 38 FOR SALES CONTACT



Processor Modules



Memory Modules



Peripheral Modules

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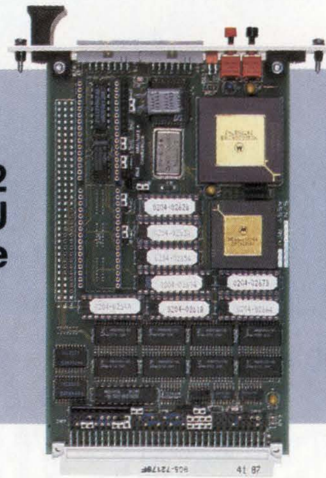
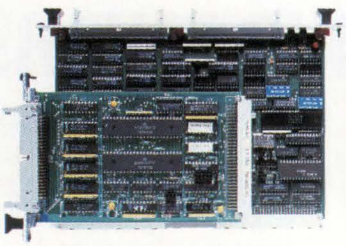
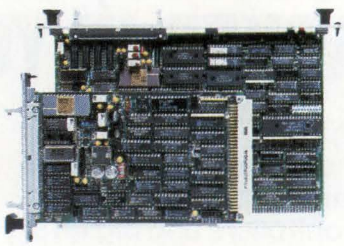
68020 CPU Module



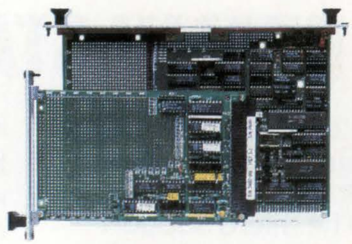
- **16 MHz 68020 CPU**
- **68881 math coprocessor site**
- **256Kbytes of dual-ported SRAM**
- **Firmware debug monitor**
- **User expansion connector**



Digital I/O Modules



Analog I/O Modules



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Analog I/O	1553 Interface Module		UNIX V/68K*
SCSI Controller	Thermocouple Input Module		SUN Workstations*
Winchester/Floppy Controller			VERSAdos*
			MTOS*

*Trademarks are acknowledged to: Microware Systems Corp. (OS-9); Eyring Research Institute, Inc. (PDOS); Motorola, Inc. (VERSAdos); V/68K Motorola, Inc. (UNIX); Software Components Corp. (PSOS); SUN Microsystems, Inc. (SUN Workstations); Industrial Programming, Inc. (MTOS).

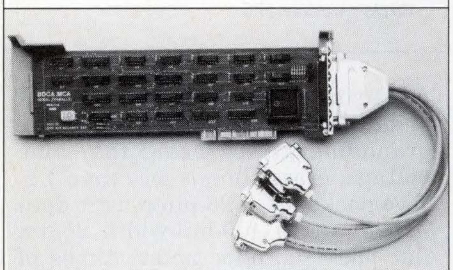
COMPUTERS AND SUBSYSTEMS

the P2 connector. Master or slave CPUs are determined by method of address, not by control register, allowing configuration changes during operation and eliminating VMEbus I/O bottlenecks. Packaged in a 9.2- ×6.3-in. double Eurocard, the board requires a single slot in a VMEbus card cage. The price is $2,917.

General Micro Systems 4740 Brooks St Montclair, CA 91763
Circle number 159

Micro Channel adapter provides three ports

Supporting the Micro Channel shared interrupt scheme, the Boca. MCA serial/parallel board features two 25-pin RS-232 serial communications ports and one 25-pin parallel port. Either serial port may be con-



figured as COM1 through COM8. The parallel port can be configured as LPT1 through LPT3. Installation is conducted via the IBM set-up program. The .ADF file is supplied with the board. The price is $210.

Boca Research 6401 Congress Ave Boca Raton, FL 33487
Circle number 154

Single-board computer supports multiprocessing

An MC68030-based, VMEbus single-board computer, the VMPU-SBC is designed to be the core building block for single or multiprocessing systems. The board features mailbox interrupts that let as many as seven units communicate with one another in a multiprocessing environment. The basic model of the computer comes with 1, 2 or 4 Mbytes of 100-ns dynamic RAM with byte-wide parity protection, and operates at 16 MHz with no wait states. A 25-MHz version can be configured with an 8-kbyte data/instruction associative cache. Additional features include two synchronous/asynchronous serial ports. Prices start at $2,995.

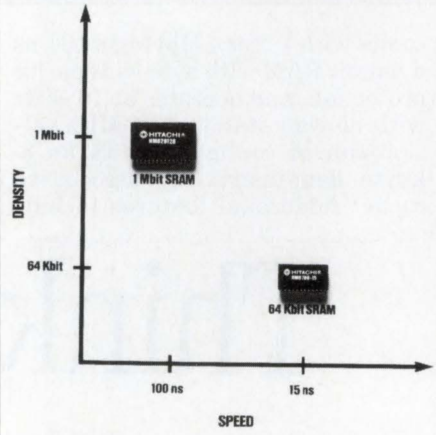
Dual Systems 3906 Trust Way Hayward, CA 94545
Circle number 157

INTEGRATED CIRCUITS

Static RAMs boast densities of 64 kbits and 1 Mbit

Consuming only 1 mA (typical) of standby current on a 5-V supply, the HM628128 static RAM can store more than 1 Mbit of data. During an access, the device draws 45 mA (typical) of current and has a data-retention mode that's activated when the 5-V supply is lowered to 3 V, which is the level for lithium batteries used in most electronic systems. Data is retained in this mode with a 1 μA (typical) current drain.

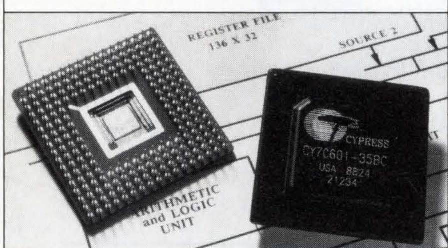
Data is organized in 8 bits×128 kbits, and all I/O are TTL-compatible. An 8-bit value can be stored or retrieved from the device in 70 ns. The device, which is built with a 0.8-micron gate-width process, houses over 4 million transistors. The chip is targeted for markets dominated by dynamic RAMs such as laptop computers, portable instruments and point-of-sale terminals, as well as for the development of microprocessor-based credit cards. Packaged in 32-pin plastic dual in-line package (DIP) or plastic surface mount, the chip is available in four speeds: 70, 85, 100 or 120 ns. The sample price is $220 each.



The 64-kbit family of SRAMs are manufactured with a BiCMOS process. They feature 15-ns access times, making them fast enough to feed data to high-performance microprocessors and reduced-instruction-set computer processors. One family member, the HM6789HP-15, has 64 kbits of data organized as 16k×4 bits. The device has an output-enable pin that gates the data coming out, eliminating the need for an extra buffer chip in certain applications.

Other family members include the HM6787HP-15 with 64-k×1-bit organization, which is used in workstations and mainframe computers, and the HM6788HP-15 with a 16-k×4-bit organization, without output enable. The 16-k×4-bit model is available in 24-pin small-outline J lead package and plastic DIP, while the other two devices in the series are packaged in 22-pin plastic DIP. Prices start at $59.10.

Hitachi America
2210 O'Toole Ave
San Jose, CA 95131
Circle number 176



RISC microprocessor executes 20 Mips

The CY7C600 reduced-instruction-set computer processor family is based on Sun's scalable processor architecture (SPARC) and executes instructions in single 30-ns clock cycles, or at an average rate of more than 20 Mips. Fabricated in a 0.8-micron CMOS process with a 0.65-micron electrical transistor size, the 7C600 is designed for fast, virtual caching that relies very little on the memory management unit (MMU) and the main memory.

Other family members include the 7C601 integer unit (IU) and the 7C608 floating-point controller (FPC). The FPC interfaces to a standard floating-point unit, the TMS 8847, to execute floating-point arithmetic concurrently with the IU. In addition, a second generic coprocessor can be interfaced to the IU.

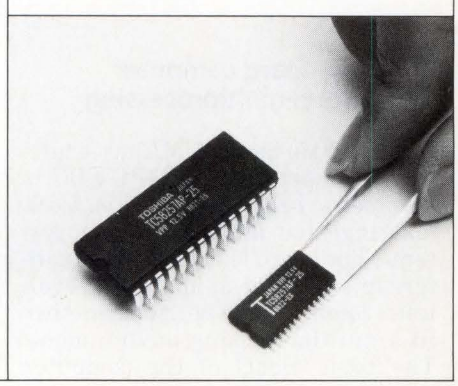
Featuring a large virtual cache space, the IU communicates with external memory via a 32-bit address bus and a 32-bit data/instruction bus and can be combined with the 7C603 MMU for high-performance workstation applications. The device provides user and supervisor modes to support a multitasking operating system. A large windowed file with two types of registers (working registers that store processes and control registers that monitor the IU's internal state) is provided on the chips. The price is $2,984.

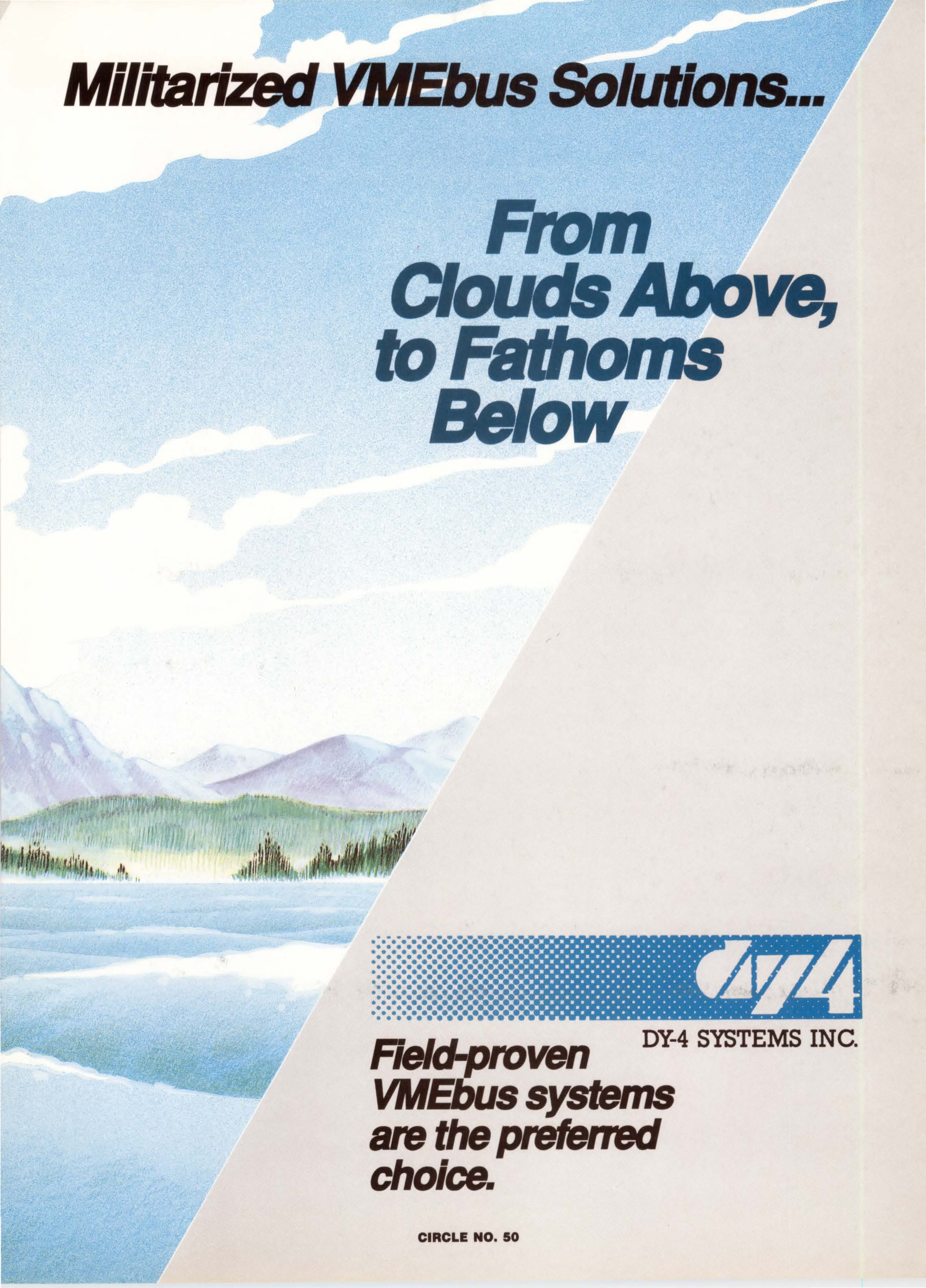
Cypress Semiconductor
3901 North St
San Jose, CA 95134
Circle number 177

"Flash" EEPROM has 170-ns access time

Organized in 32k words×8 bits, the TC58257AP/AF is a 256-kbit very large-scale integration CMOS device with 100-cycle program and erase endurance rates. The chip requires 30 mA of current in operating mode and 100 μA in standby mode. Programming time is about 4 s for 256 kbits of data using a 12.75-V, 100-ms programming pulse. Using the same voltage, erase time is less than 1 s. Two packages, a 28-pin plastic dual in-line and a 450-mil-width 28-pin flat package, offer access times of 170, 200 or 250 ns. Manufactured using 1.2-micron design rules, cells are reduced to less than one-third the size of NMOS EEPROMS, allowing faster access times and lower power consumption. In quantities of 100, prices start at $50.

Toshiba America
9775 Toledo Way
Irvine, CA 92718
Circle number 182

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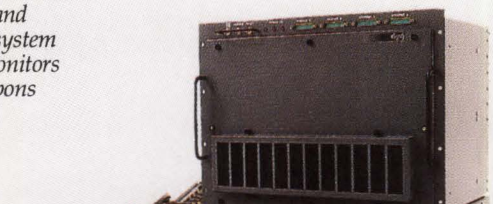

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CIRCLE NO. 50

INTEGRATED CIRCUITS

Chip set provides communications link

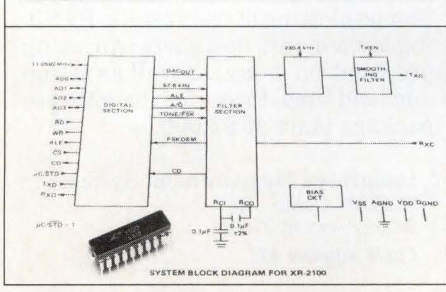
Providing a communications link between data-terminal and data-communications equipment at a rate of 48 kbits/s and 10 Mbits/s, the XR-T3588 (driver) and XR-T3589 (receiver) provide three independent drivers and receivers on each device. Both ICs are TTL-compatible and feature a power-down mode for each of the receivers and transmitters. The set is compatible with Consultative Committee on International Telephone and Telegraph V.35 and Bell 306 interface and is available in a ceramic dual in-line package. The price for the set is $4.18 in 5,000-piece quantities.

Exar
2222 Qume Dr
San Jose, CA 95161
Circle number 178

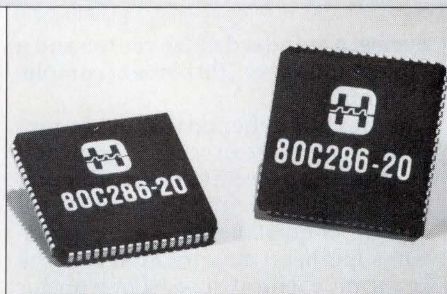
CMOS modem IC suits V.21 European standard

A low-power, Consultative Committee on International Telephone and Telegraph V.21 modem IC, the XR-2100 is a 300-baud CMOS device with a worst-case signal/noise performance of 6 dB. The modem provides transmit and receive filtering, as well as answer and call tone generation/detection. It includes circuitry for carrier detect and analog loop-back. Power-down mode for battery applications is featured, while typical power dissipation is 200 mW. Packaged in 20-pin dual in-line package or plastic leaded chip carrier, the unit operates ± 5-V power supplies. The price is $3.75.

Exar
2222 Qume Dr
San Jose, CA 95161
Circle number 187



SYSTEM BLOCK DIAGRAM FOR XR-2100



CMOS microprocessor consumes 310 mA

The 80C286-20 20-MHz microprocessor is guaranteed over the commercial (0° to 70° C) ambient temperature range. In 16-bit applications, the CMOS device executes 80286 code more efficiently than an 80386, using up to 30 percent fewer clock cycles to perform many instructions. Housed in a plastic leaded chip carrier, the microprocessor carries a maximum operating current of 310 mA. Price is $261.90 in quantities of 100.

Harris Semiconductor
PO Box 883
Melbourne, FL 32901
Circle number 180

Transceiver ICs achieve 2-km point-to-point range

A family of integrated services digital network transceiver ICs, the MC 145474 and MC145475 pass full conformance testing to the Consultative Committee on International Telephone and Telegraph I.430 recommendation and ANSI specification. An adaptive receiver structure automatically selects the optimum sampling phase and deduction threshold of the incoming signal, enabling the ICs to achieve a point-to-point range of 2 km, twice the I.430 specification. The transceivers include multiframing "S" and "Q" maintenance channels, a line driver that supports a 1:1 transformer ratio, selectable modes for line-card and terminal applications, and activation and deactivation functions. Prices start at $17 in 1,000-piece quantities.

Motorola
PO Box 6000
Austin, TX 78762
Circle number 186

Programmable array logic device runs at 7.5 ns

The PAL16R8-7 and PAL22V10-15 are 20- and 24-pin programmable array logic (PAL) devices with propagation times of 7.5 and 15 ns, respectively. The 15-ns version is capable of 50-MHz operation due to its flexible macrocell architecture. The entire PAL product family is supported by the manufacturer's Palasm design software, with programming accomplished via standard PAL device programmers. The 20-pin, 7.5-ns device is offered in dual in-line package and plastic leaded chip carrier (PLCC) and is priced at $10.45. The 24-pin, 15-ns version is available in skinny dual in-line and PLCC packages and is priced at $16.45.

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94088
Circle number 185

CMOS PLDs boast 12-ns propagation delay

Manufactured with E^2 CMOS technology, the GAL16V8A-12 (20-pin) and GAL20V8A-12 (24-pin) are programmable logic devices (PLDs) with a maximum propagation delay of 12 ns. The E^2 CMOS process allows complete ac, dc and functional testing of the PLDs, which are guaranteed for 100 erase/write cycles and data retention exceeding 20 years. Consuming a maximum of 115 mA of power, the devices are available in plastic dual in-line package or plastic leaded chip carrier with prices starting at $8.32.

Lattice Semiconductor
5555 NE Moore Ct
Hillsboro, OR 97124
Circle number 183

DESIGN AND DEVELOPMENT TOOLS

Printed circuit board CAD software supports moderate size designs

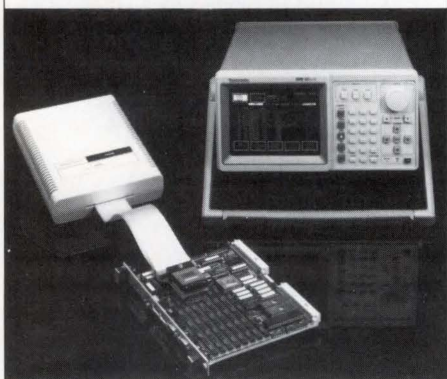
An entry-level printed circuit board design tool, Associate Designer is used to design boards of moderate size and complexity, including double-sided, surface-mount designs.

The software's interactive printed circuit board layout editor lets users design printed circuit boards with through-hole or surface-mount devices, while an integrated schematic-capture program speeds the accurate entry of circuit designs. Two router options are offered to shorten layout cycles: a standard maze router and a rip-up-and-retry 100 percent completion router.

A flexible schematic-capture program speeds the process of accurately entering a circuit design. Explicit knowledge of printed circuit board layout requirements and conventions has been incorporated into the program, facilitating design transfer to the printed circuit board and subsequent back-annotation.

A large schematic and printed circuit board library with more than 6,000 through-hole and surface-mount components is included with the package, which supports TTL, CMOS, ECL, microprocessor, memory, discrete, linear and electromechanical components. Interface options are offered, providing programs for manufacturing and data base interfacing. Automatic gate packaging, engineering rules checking, printed circuit board design rules checking, net-list comparison and photoplotter output are among the standard system utilities supplied. The price is $3,895.

P-CAD
1290 Parkmoore Ave
San Jose, CA 95126
Circle number 169



Logic analyzer supports 68030 microprocessor

An interface between the Motorola 68030 microprocessor and the manufacturer's 1240/1241 logic analyzer, the 68030 support tool consists of a 12RM33 mnemonics ROM pack and a PM206 personality module. The ROM pack provides instrument set-up and disassembly post-processing of acquired 68030 data by marking executed instructions and automatically tracking the three-stage instruction pipeline. The pack also decodes the dynamic bus-sizing mechanism and displays only the data that was actually transferred. The personality module provides a connection to the 68030's 128-pin socket through a low-profile, low-capacitance probe connector. The 68030 also supports clock frequencies of up to 25 MHz.

Tektronix
PO Box 12132
Portland, OR 97212
Circle number 172

Printed circuit board design package breaks DOS limits

Two versions of a printed circuit board layout design tool work on 80386- or 80286-based PC ATs or compatibles. The Ultiboard 386 runs on a system with extended memory (above 1 Mbyte) up to 24 Mbytes and a 20-MHz 386 plug-in board. The use of the 32-bit protected instruction set results in programs running at a sustained speed of 4 to 5 VAX Mips. The 286 version runs on ATs and compatibles with extended memory and uses the 286 protected mode. Previously under DOS, the maximum capacity for board layout was between 300 and 400 ICs. The use of 286 extended memory and 386 32-bit native mode extends this to virtually unlimited capacity, according to the manufacturer.

Ultimate Technology
233 Peachtree St NE
Atlanta, GA 30303
Circle number 173

Design-synthesis system works with ASIC libraries

The NCR design-synthesis system uses high-level behavioral language descriptions for the design of cell-based application-specific ICs (ASICs). The tool is coupled with the manufacturer's cell libraries, and includes both 2- and 1.5-micron digital and analog cells; supercells; and compiled functions for commercial, military and automotive applications. The system is an expert rules-based software tool that lets designers specify and simulate ASIC architecture in high-level conceptual terms on Mentor Graphics workstations. Using its data base of expert design rules, the tool automatically generates the logic necessary to implement the desired system-level functions. A license costs $51,000.

NCR Microelectronics
1700 S Patterson Blvd
Dayton, OH 45479
Circle number 171

Software simplifies ASIC development

Compatible with any product in the manufacturer's Logic Master application-specific IC (ASIC) verification family, the characterization and timing analysis software package lets the user automate any Logic Master measurement. Test data may be collected into formats for analysis, and ASIC verification may be controlled from a spreadsheet environment. The software provides menu-driven routines for making ac and dc measurements of prototype devices and for Shmoo plotting of test results. By filling out a menu, designers can set up propagation delay, as well as set-up and hold time. Prices for the software package start at $3,000.

Integrated Measurement Systems
9525 SW Gemini Dr
Beaverton, OR 97005
Circle number 175

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CIRCLE NO. 42

PRODUCT BRIEFS

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Io *Circle 128*

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Bicc-Vero *Circle 136*

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3Com *Circle 144*

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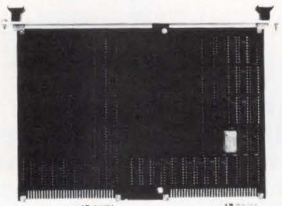

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CIRCLE NO. 221

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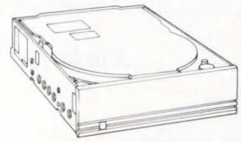

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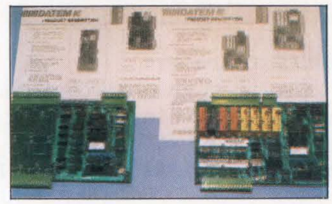
MITSUBISHI ELECTRONICS **CIRCLE NO. 222**

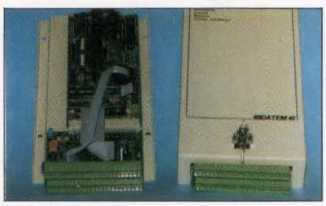
"DATEM's Single Board Industrial Controllers



—The dDCM53x family of intelligent BITBUS compatible analog/digital industrial controllers allow OPTO-22 compatible termination modules to be integrated within a DISTRIBUTED CONTROL NETWORK that supports up to 250 nodes over 8 miles. Programmable in C, BASIC and Ladder, modules are supported by a comprehensive set of network development tools for DOS, QNX, XENIX, VMS. DATEM Ltd., 148 Colonnade Road, Nepean, Ontario, Canada K2E-7R4 — (613) 225-5919.

CIRCLE NO. 223

"Intelligent Communication Gateways From DATEM"



—The dDCN5000 family of intelligent communication gateways allow a range of equipment to be integrated into a DISTRIBUTED CONTROL NETWORK. Firmware drivers support interfaces to RS232, RS422, RS485, IEEE-488, and CENTRONICS: multitiered BITBUS networks are also supported. DATEM Ltd., 148 Colonnade Rd., Nepean, Ontario, Canada, K2E-7R4 — (613) 225-5919.

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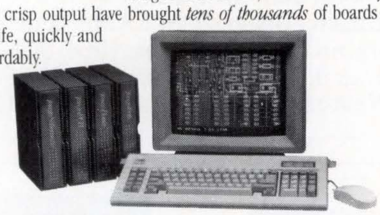

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CIRCLE NO. 225

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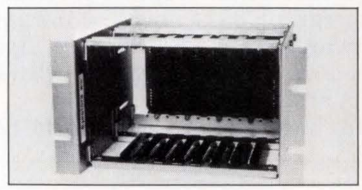

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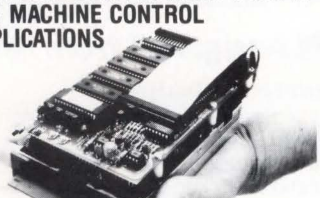
COMPLETE DEVELOPMENT SYSTEM FOR MACHINE CONTROL APPLICATIONS



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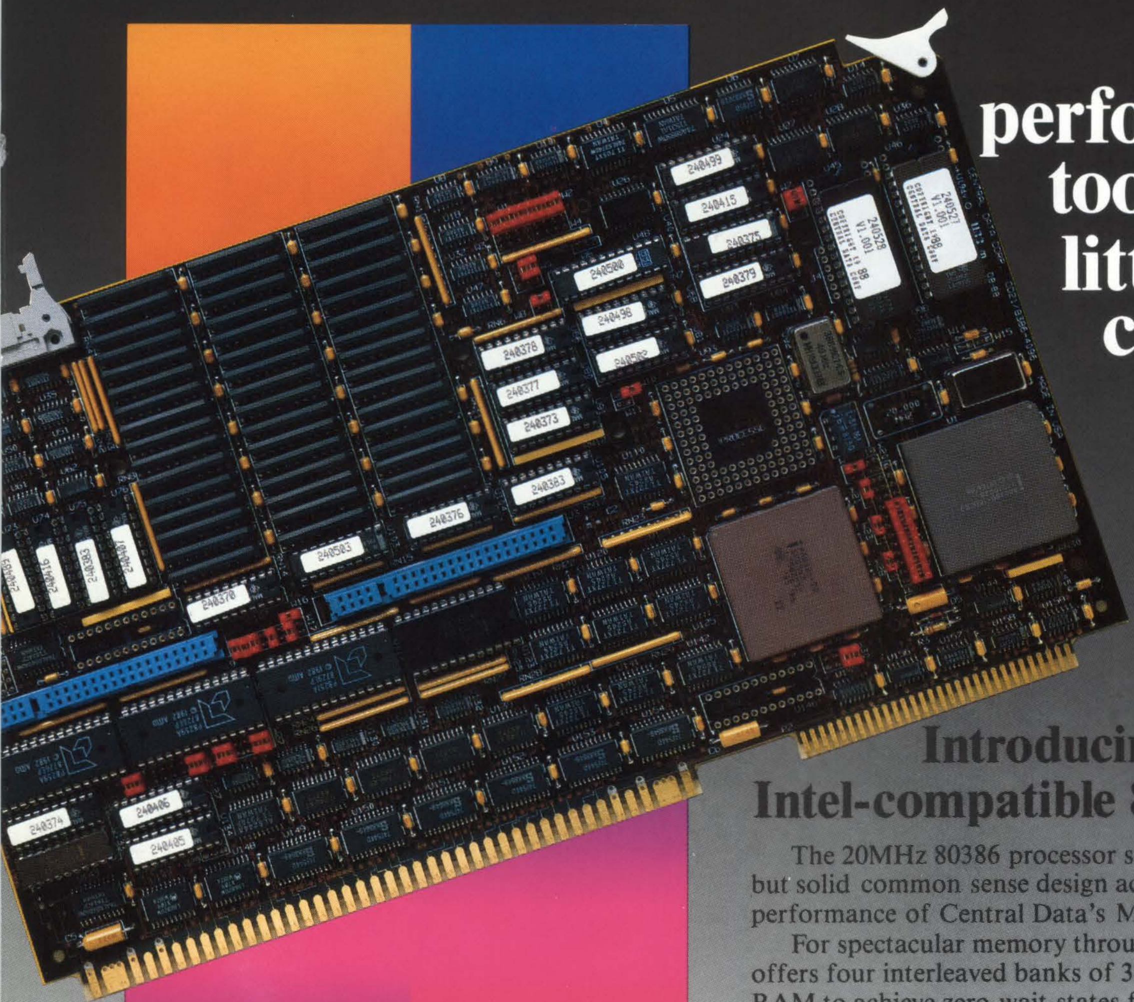

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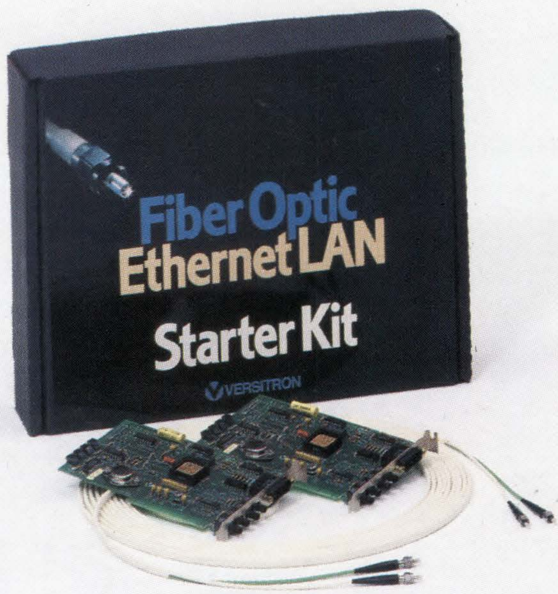

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