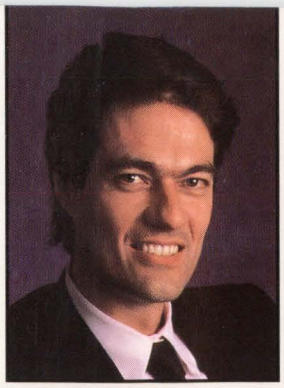

Joe Costello on
Concurrent Engineering

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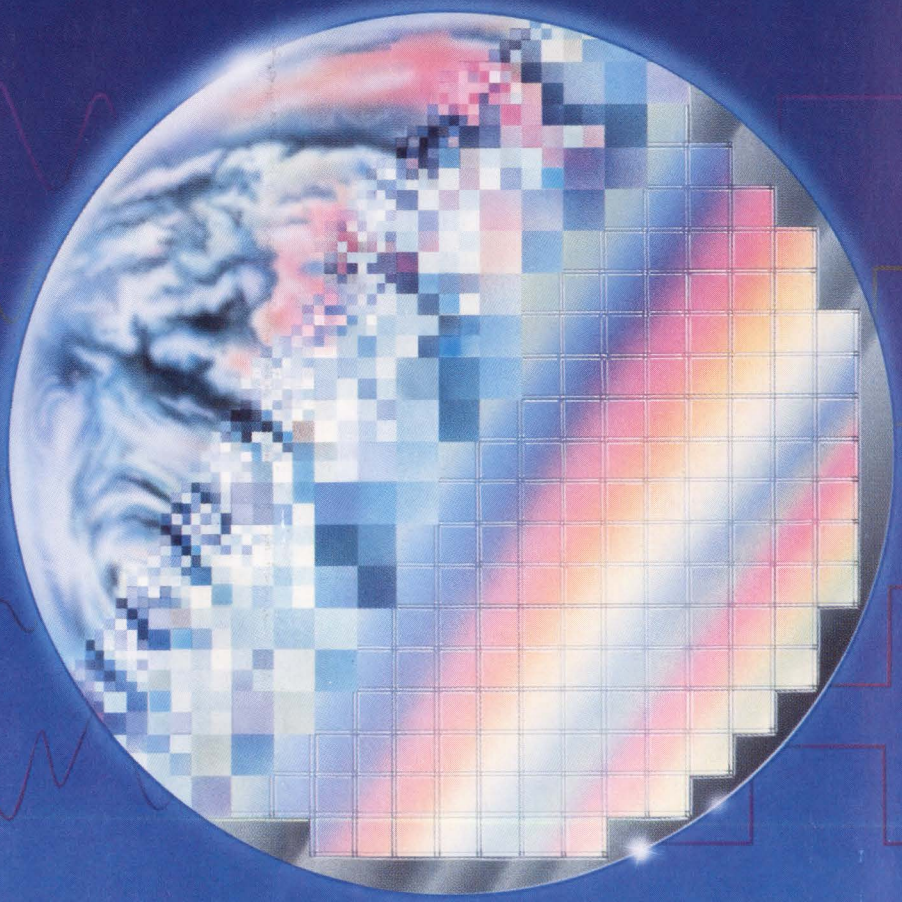

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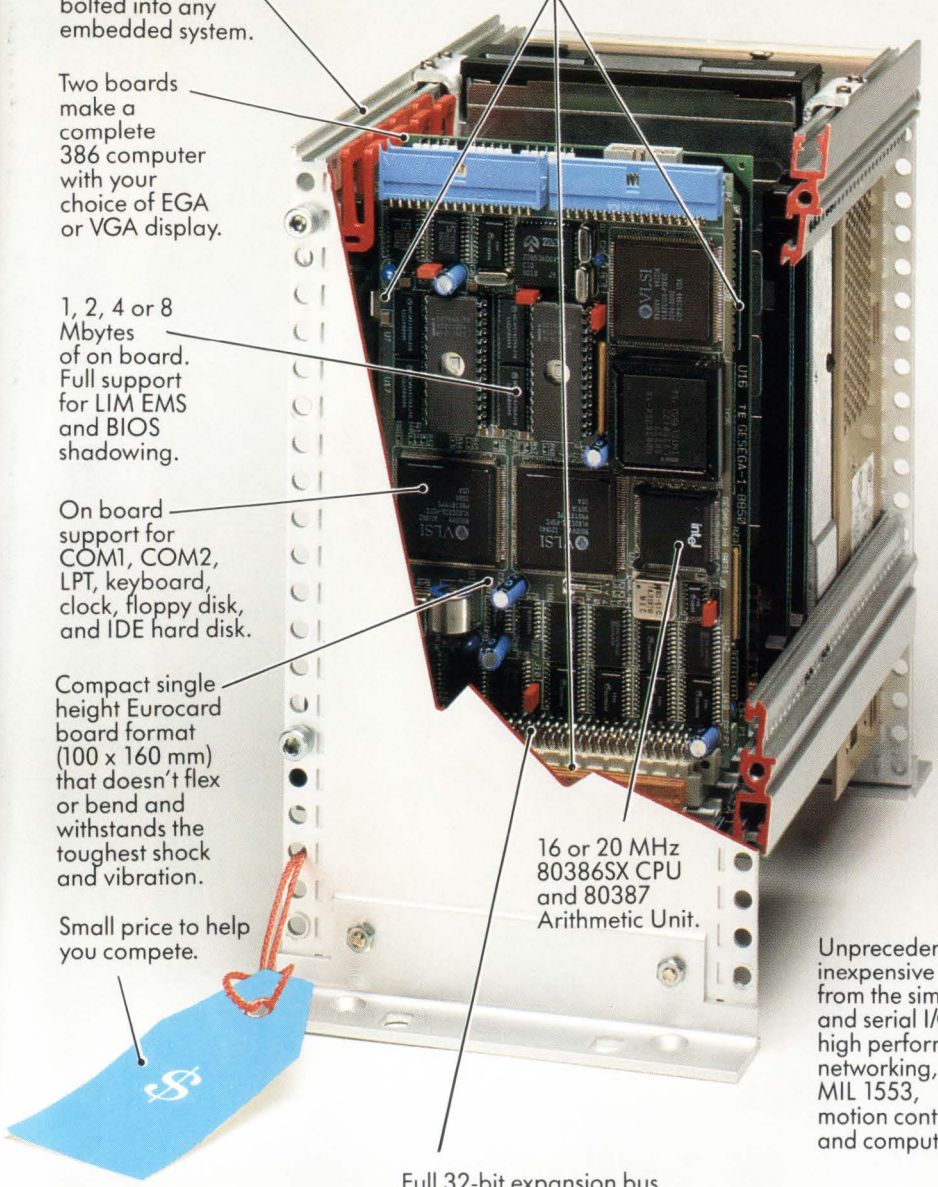

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CIRCLE NO. 1

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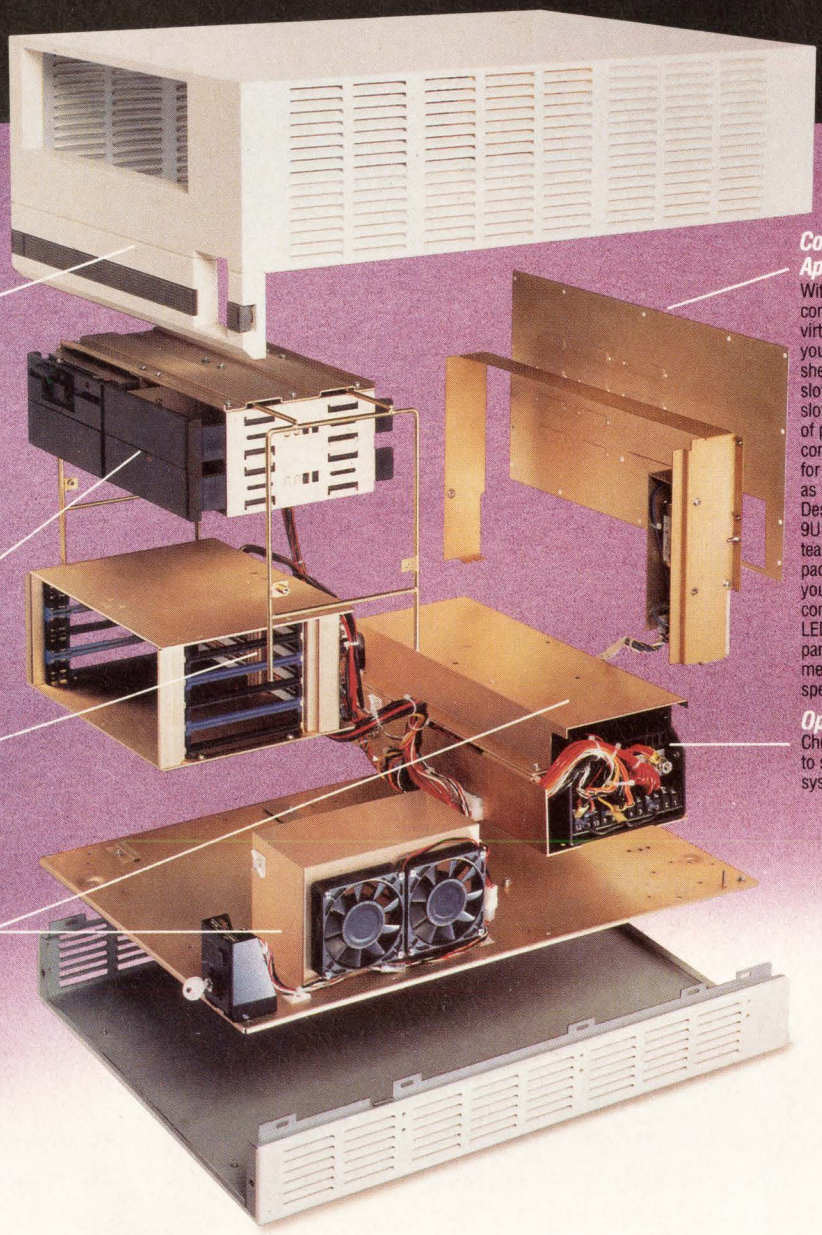
New



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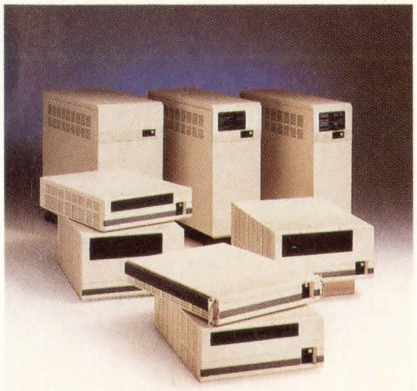

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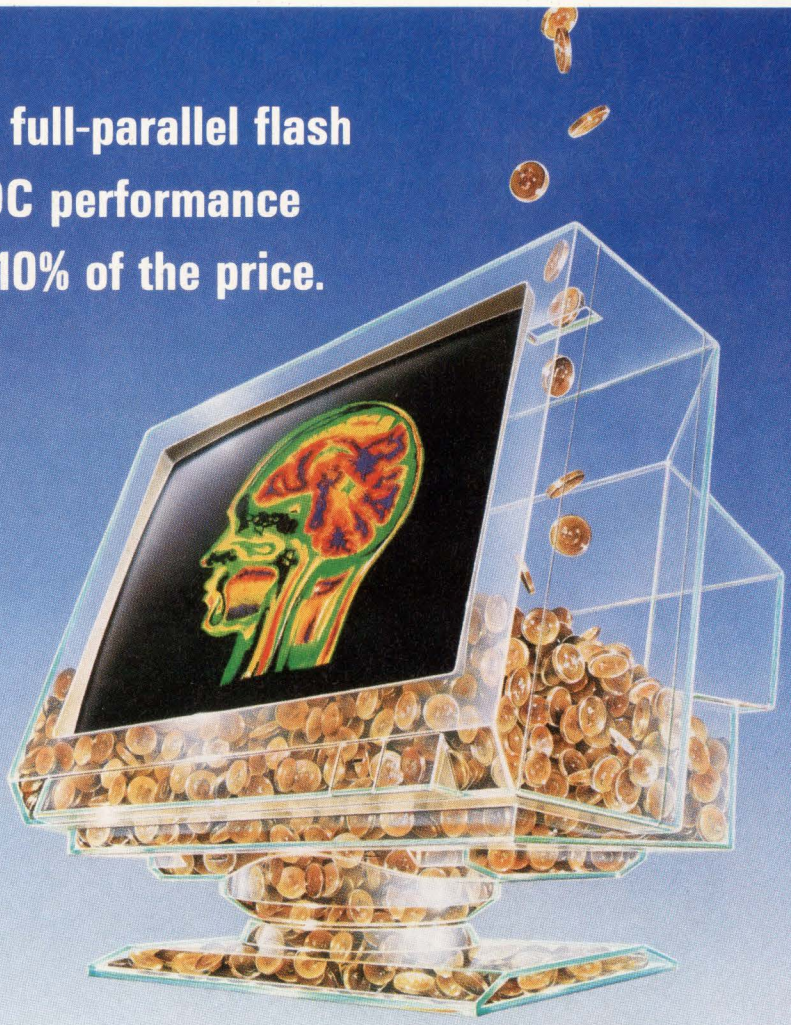

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VOL. 30, NO. 1 JANUARY 1, 1991

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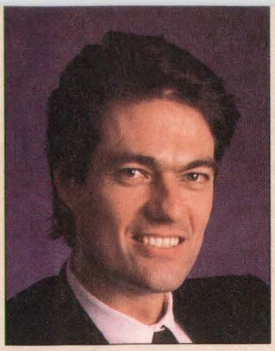

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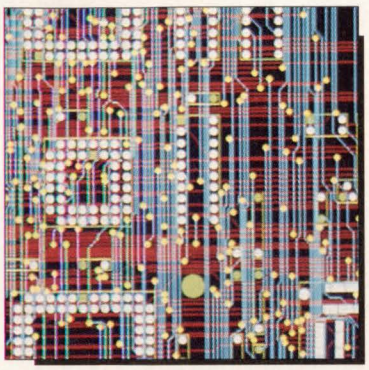

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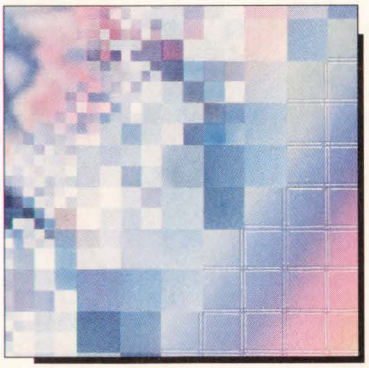

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AMP TBC (Twin-Beam Contact) Connectors steal the show for high-density, high-pin-count affordability. Three- and four-row versions deliver compelling performances in 32 to 540 position roles.

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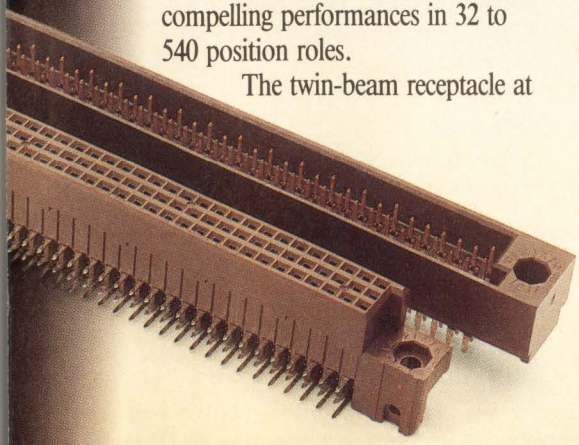

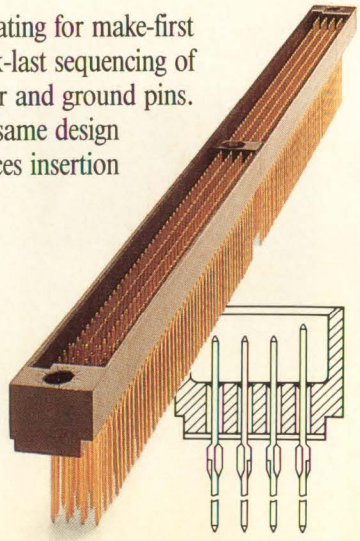

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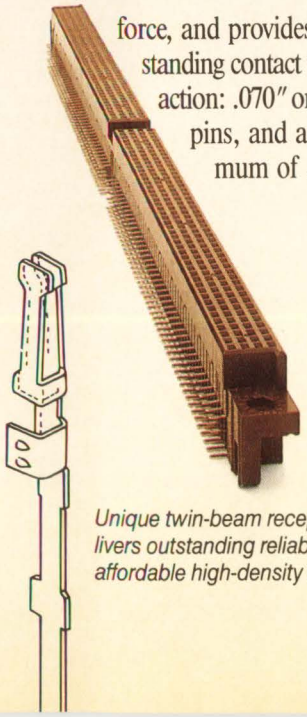

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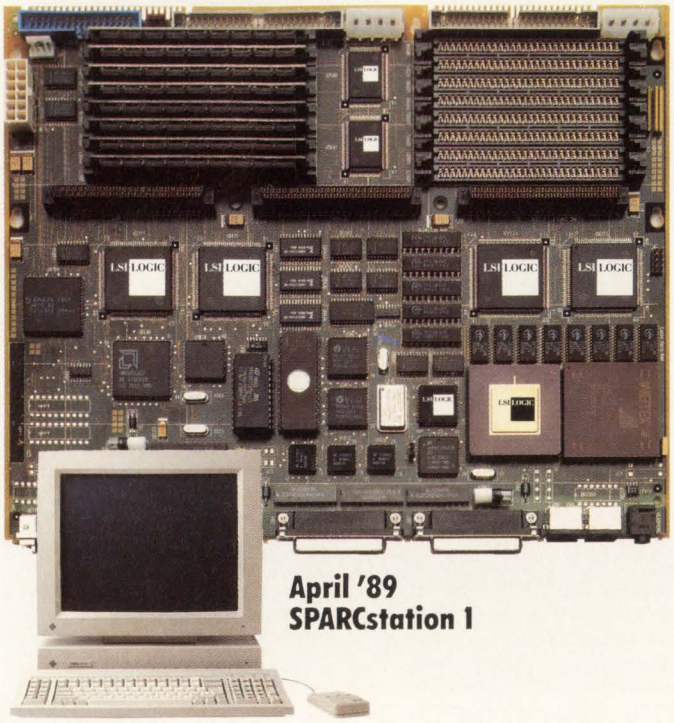
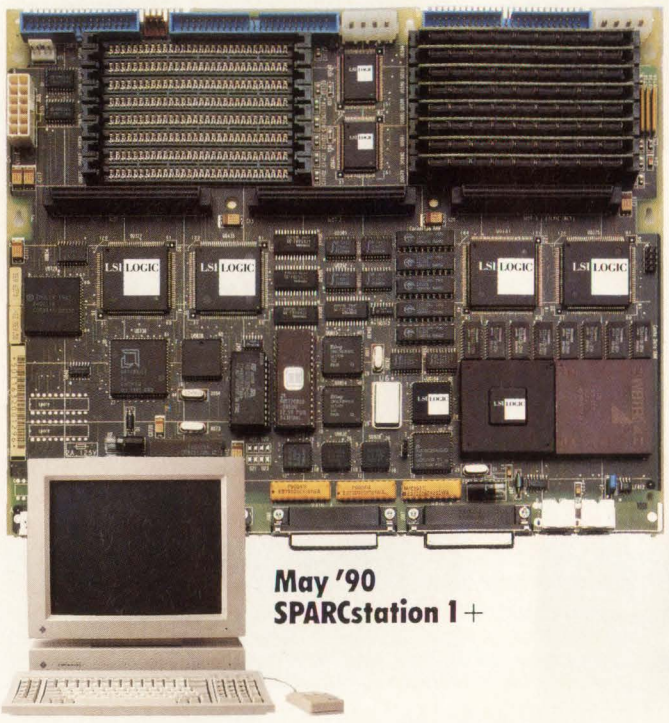
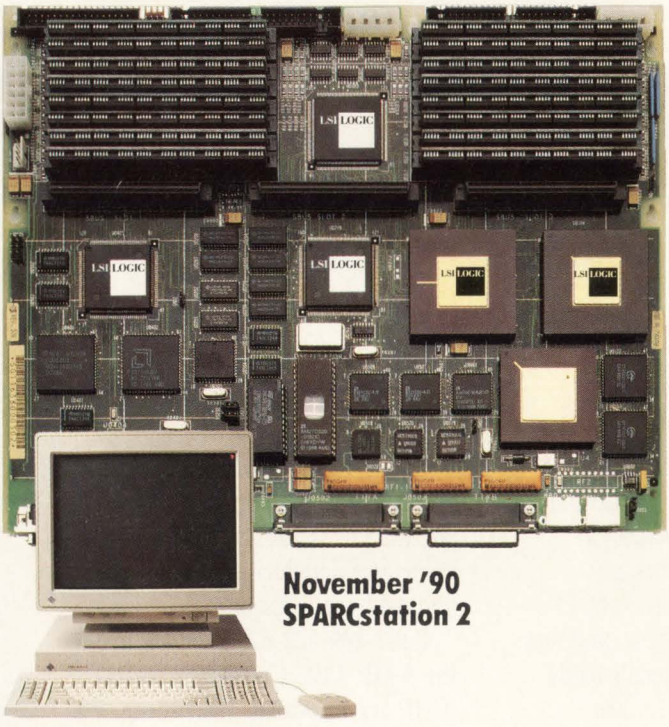
AMP Interconnecting ideas



April '89
SPARCstation 1



May '90
SPARCstation 1+



November '90
SPARCstation 2

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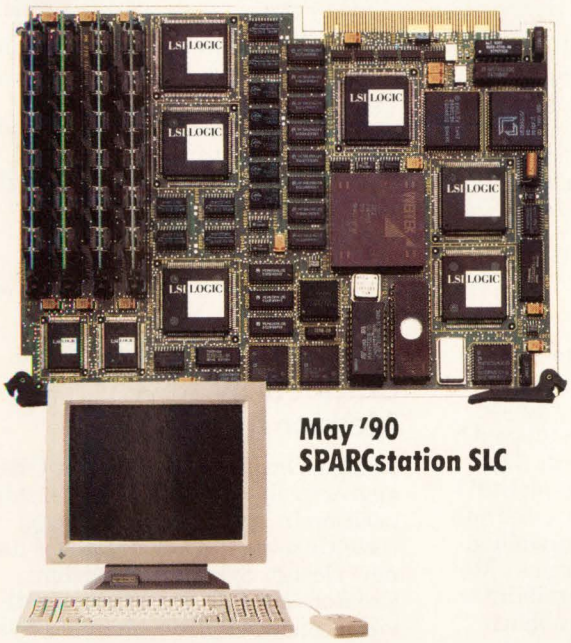
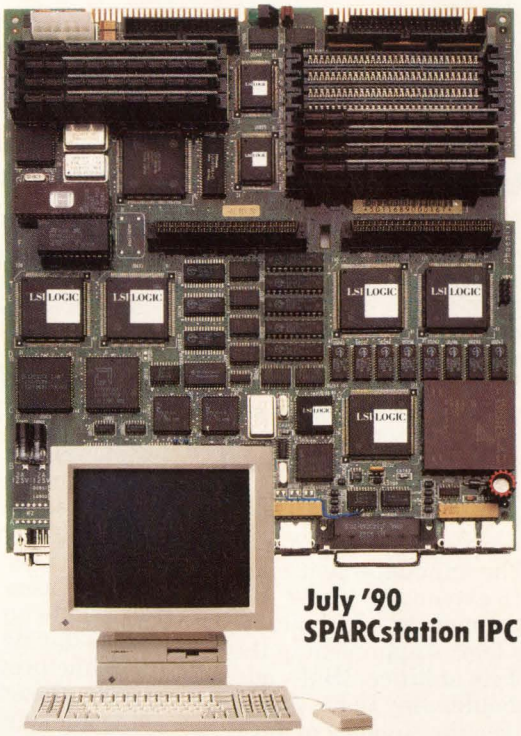


May '90
SPARCstation SLC



July '90
SPARCstation IPC

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Since introducing SPARCstation 1 in April '89, Sun has utilized LSI Logic's RISC and ASIC technology and design methodology to pack more processing power into smaller footprints.

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Sun's latest creation, SPARCstation 2, is a shining example. This powerful new workstation was brought to market just four months after the introduction of the SPARCstation IPC. By leveraging the power of LSI Logic's RISC and ASIC technology, Sun has quickly introduced a whole new level of price/performance in UNIX workstations.

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ACROSS THE BOARD

CIRCLE NO. 5

Silicon breakthrough boosts system speeds

IBM (Armonk, NY) has succeeded in growing silicon on a nonconductive substrate, an advance that not only boosts transistor switching speed, but also prevents power leakage and reduces an IC's vulnerability to radiation. IBM has already used the technique to make CMOS transistors that are three times faster than conventional devices, though the company admits that the discovery won't result in faster computers for a couple of years. The announcement is expected to extend the useful life of silicon technology, which many IC vendors fear is approaching the limits of its abilities. IBM's advance should allay those concerns and reduce the urgency of developing more expensive alternatives, such as gallium arsenide.

— Mike Donlin

Wafer-scale integration powers neural computer

Hitachi (Tokyo, Japan) has unveiled a prototype general-purpose neural computer system that could be used as a super-high-speed back-end processor or coprocessor for workstations. The system uses wafer-scale integration to achieve what Hitachi claims is the highest learning performance ever posted by a neural computer—up to 2.3 billion operations per second.

At the heart of the system are 5-in. wafers, made with submicron CMOS processing, that pack up to 20 million transistors divided into 60 very-high-density gate arrays on a single subsystem board. There are eight subsystem boards in the computer that host a total of 1,152 neurons.

Hitachi's prototype was able to perform a signature verification in just two seconds, a task that could previously be performed only by a large supercomputer. The system achieves this performance by simulating the dynamic and parallel processing functions of the human brain, albeit with a much smaller network.

— Mike Donlin

0.5-μm CMOS process refined

Motorola (Austin, TX) has developed a new CMOS process that could become a feasible way for building ultra-dense circuits with design rules below 0.5 μm. The process uses disposable sidewall spacers to protect source and drain areas during thermal annealing.

While previous research at Motorola unearthed the possibilities of using sidewall spacers fabricated from polysilicon, new research demonstrates that the polysilicon can be removed without damaging the underlying device structure. This was accomplished by adding an additional silicon nitrate to a thin polysilicon frame, making it impervious to the acid used to remove the sidewall structure.

Research results indicate that the silicon nitrate layer permits finer definition of transistor structures, leading to reproducible functioning devices under a half μm. The new process could form the foundation of a practical and economical ultra-large-scale circuit process.

— Jeffrey Child

Intergraph seeks framework partners

In an attempt to grab a larger share of the EDA market, Intergraph (Huntsville, AL) has unveiled Interlink, a program designed to integrate third design tools into Intergraph's newly named Simultaneous Engineering Environment framework. The program already encompasses existing OEM relationships, but Intergraph is aggressively seeking alliances with other vendors to broaden its base of EDA products—an area in which it has been relatively weak. By labeling and publicizing a framework that it has had for some time, Intergraph is signaling a more competitive stance against rivals Mentor Graphics and Cadence Design Systems who traditionally tout the benefits of their framework offerings. Though strong in mechanical CAD, Intergraph's market share is small—about 1.5 percent, according to Dataquest figures.

— Jeffrey Child

Synthesis objectives outlined by new Mentor division

Mentor Graphics (Beaverton, OR), aggressively pursuing a leadership position in synthesis technology, recently gave further details of its new Design Synthesis Division. Created last fall, the synthesis division resides within Mentor's Systems Group and is responsible for ASIC, IC and programmable logic device synthesis products. It will also oversee the digital signal processor synthesis technology being developed at the European Development Center (Leuven, Belgium), test synthesis technology from the company's Simulation and Test Division, and analog synthesis products from the Silicon Design Division.

The synthesis software Mentor currently offers can be traced to the acquisitions of Trimeter Technologies and Silicon Compiler Systems, a technology purchase agreement with Minc (Colorado Springs, CO) and internal development efforts. Mentor has completed the integration of the AutoLogic synthesis and optimization toolset for IC design—part of Silicon Compiler Systems' previous product offerings—into its Software Release 7.0 EDA environment. The LogicLib library of technology-independent macrofunction generators has also been integrated.

What the industry is really holding its collective breath for, though, is the release of the Design Consultant VHDL synthesis tool that Mentor expects to ship

Continued on page 10

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CIRCLE NO. 6

Continued from page 8

with phase II of Software Release 8.0 in the second quarter of this year. Beyond that, the workstation-based design system for DSP synthesis being developed in Europe is likely to be one of the hottest attractions at DAC '91 in San Francisco this June where Mentor expects to demo it for the first time.

— Barbara Tuck

What exactly is programmable interconnect?

Venture capitalists backing a programmable interconnect technology being developed by start-up firm Aptix (San Jose, CA) are evidently betting on the company's ability to develop the innovative technology demanded by changes in systems design. As for details on the product, currently in the process of being physically defined, Amr Mohsen, chairman, president and CEO of Aptix, says only that the first round of venture funding will allow the company to concentrate on developing "component interconnect technologies that will enable systems designers to achieve greater control and flexibility in the systems design process."

The Aptix description of its technology as "field-programmable integrated solutions for component interconnects" might leave some blank spots for those looking for a detailed product definition. But the empty spaces fill in rather quickly when industry trends are taken into account along with Mohsen's background as founder and former president and CEO of Actel.

A look at the company's management team roster is also revealing. It includes, among others, a former packaging engineering guru from National Semiconductor, a former software development director from Cadence and a former senior vice-president of marketing from Daisy/Cadnetix. Nevertheless, it will be interesting to follow this technology as it unfolds into product. *— Barbara Tuck*

Acorn RISC machine resurfaces at Apple

The Acorn RISC CPU, developed by Acorn Computer (Cambridge, England), has been one of the most obscure but most widely produced RISC processors. Built by VLSI Technology (Tempe, AZ), the chip has gone through several generations and has been used in Acorn personal computers as well as embedded applications. The device is remarkable primarily for its simplicity, small size and high speed for the money.

Now Apple Computer (Cupertino, CA) has formed a joint venture with Acorn and VTI called ARM to produce yet another generation of RISC chips on the Acorn architecture. Acorn and VTI will presumably get new products for their respective ventures—personal computers and custom embedded controllers—from the joint development effort. But the big question is Apple's interest in the little RISC chips. Speculation runs from the possibility of ARM CPUs as controllers for peripherals—laser printers, perhaps—to the notion of ARM-based portable or hand-held computers.

In any case, the move has to look like a repudiation of Apple's traditional CPU vendor, Motorola. That company has supplied all the CPUs for the Macintosh family and has been aggressively shrinking and integrating its 68000 CPU cores. In addition, Motorola has reportedly tried very hard to sell Apple on the 88000 RISC family. No matter how Apple intends to use the ARM chips, it will be in place of some major element of Motorola's product line. *— Ron Wilson*

Motorola ships 68040, sort of

Motorola (Austin, TX) has announced that it's finally shipping the production 25-MHz version of the 68040 microprocessor, but still only in limited quantities. The part was announced with considerable enthusiasm in March 1989 as the 68000 family's next-generation, RISC-beating CPU. And in fact the chip showed performance figures as good as those of any RISC processor shipping in 1989. The device's performance was impressive enough to draw design wins from the likes of workstation vendor Hewlett-Packard. But the chip has not been shipping. Reportedly a number of serious design, rather than manufacturing, problems have held up the device. Now Motorola feels confident in its mask set and is ready to take on the problems of ramping up such a complex die to full production status under its Baldrige-winning quality requirements. But in the beginning of 1991, the first question will be not whether Motorola can produce the 68040 in volume, but whether there remains, nearly two years after the announcement, a significant market for the chip.

— Ron Wilson

S3 puts multiprocessing chip set on hold

S3 (Santa Clara, CA), the startup that recently outlined its plans for a multiprocessing personal computer chip set, has put the idea on indefinite hold. In an effort to conserve cash, and perhaps in recognition of the absence of customers for multiprocessing architectures, the company has decided to focus all its efforts on a set of graphics products. The graphics design was originally intended to fit into the multiprocessing architecture, but now appears more marketable by itself. The change involved cutting about half of S3's technical and support staff. The company claims that it's still committed to the multiprocessing architecture and is seeking licensees to pursue further development. But without the designers who actually implemented the complex scheme in silicon, it's difficult to see how S3 could transfer the technology effectively should a licensee appear.

— Ron Wilson

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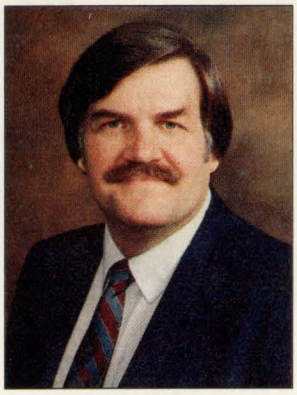
CIRCLE NO. 7

A digital way of life

The digital IC has turned nearly everything more complex than a pencil sharpener into a computer.



John C. Miklosz
Associate Publisher/
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There have been many technological turning points throughout the evolution of mankind that transformed forever the human condition. We can look back to the discovery of fire, the wheel, bronze, iron, gunpowder, paper, and the printing press. More recently we've had the development of the steam engine, as well as the discovery of petroleum and the subsequent invention of the internal combustion engine, the automobile and the airplane. The genesis of electronic technologies can be traced back to the discovery of electricity and the invention of the electric motor, the telegraph and the telephone, which was followed by the invention of the vacuum tube, and then radio, television and the electronic computer.

The two most recent turning points in this whirlwind of development were the invention of the transistor in 1947 and the invention of the IC in 1958. While the transistor was the seminal invention, the IC has been the primary driving force behind the digital transformation of our world—a transformation that's been underway now for about three decades and will essentially be complete before this decade is out.

This digital transformation has changed the nature of just about every product we touch. It also has resulted in other transformations that were undreamed of—even more significantly, were *impossible*—before the invention of the digital IC. In a very real sense, the digital IC, in its multiple variants, from microprocessor to memory, has turned nearly everything more complex than a pencil sharpener into a computer. It has made computers the most pervasive aspect of technological progress in our lives.

A computer, in the guise of a digital clock, is the first thing most of us hear and see in the morning and one of the last things we touch at night. While commuting to work, a computer in an engine controller lowers emissions and improves the mileage of our automobiles, and a computer in a braking system can keep our cars from skidding on slippery roads. At the office, computers take the shape of telephones, fax machines, copiers, and printers. Back home in the evening, a computer known as a compact disc player surrounds us with better sound than many of us can hear.

This digital transformation has special significance for all of us at *Computer Design* because we began publishing our magazine 30 years ago. That was, coincidentally, the same year that commercial—albeit primitive—digital ICs became a reality. We decided, then, to celebrate the beginning of this transformation with a Special Report that details some of the developments that occurred during those 30 years. There have been so many that the best we could do was give you a sampling. We hope that you enjoy reading it, and that you'll be as excited about the next 10 years as we are.

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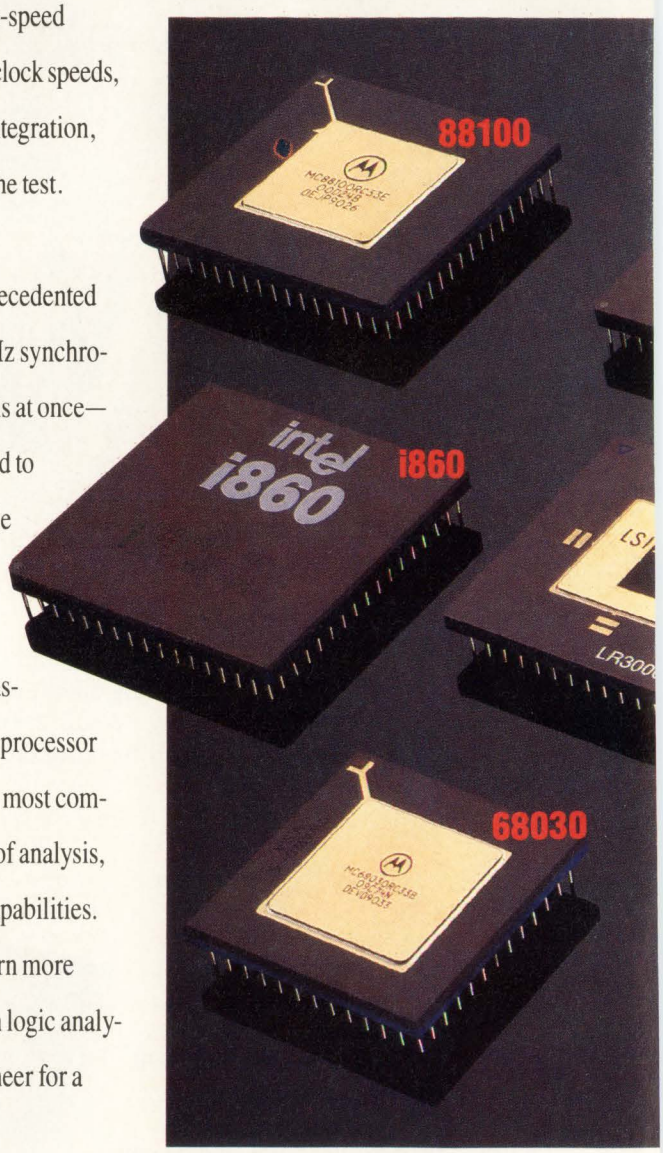

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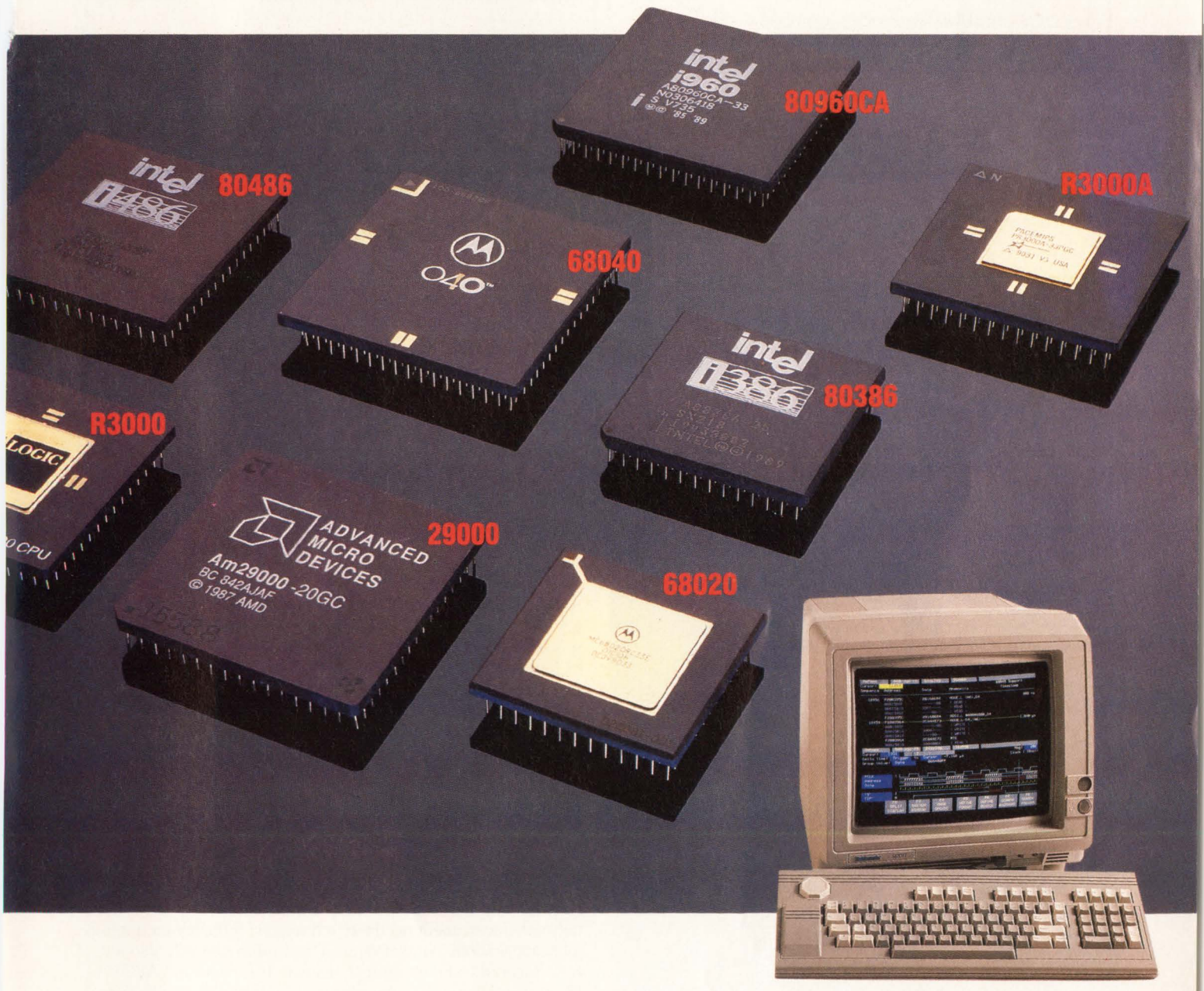

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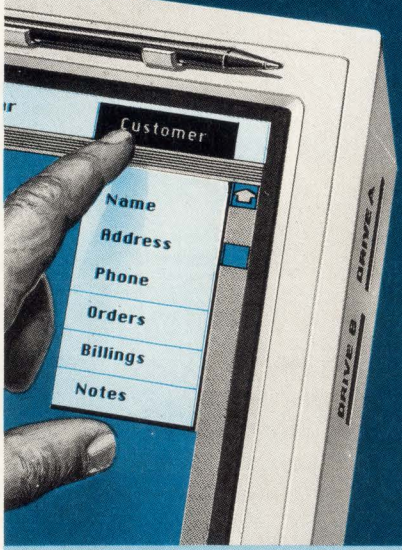

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CIRCLE NO. 12

CALENDAR

CONFERENCES

January 14-17
ATE & Instrumentation Conference

ATE & Instrumentation Conference

Disneyland Hotel, Anaheim, CA. This conference for test professionals will offer almost 50 sessions in design, manufacturing, management, service test, and systems integration. Session topics include "Testing in the 21st Century" and "Testing—the Competitive Edge." In addition, a four-day educational tutorial will follow the basics of design for test through to an actual production example of an integrated design and test board. Information: Miller Freeman Expositions, 1050 Commonwealth Ave, Boston, MA 02215-1135, (800) 223-7126. **Circle 366**

January 17-19
Landex '91 Southern California

LANDA

Hyatt Regency, Irvine, CA. Targeted to LAN resellers, Landex '91 will feature seminars pertaining to training and basics, technology, and business building, as well as super sessions. Specific topics include "High-Performance Topologies" and "The Successful VAR Formula." The LAN Dealers Association will also offer its certification examinations. Information: LANDA, 360 W Butterfield Rd, Suite 260, Elmhurst, IL 60126, (708) 279-2255. **Circle 367**

January 22-24
AFCEA/West

AFCEA

San Diego Convention Center, San Diego, CA. Co-sponsored by the U.S. Naval Institute, the 12th AFCEA Western Conference and Exposition will present exhibits from more than 150 companies. The three-day program will offer events featuring government, military and industry leaders in computers, communications, information systems, aircraft, R&D, and shipbuilding. Information: AFCEA Programs Office, 4400 Fair Lakes Ct, Fairfax, VA 22033-3899, (703) 631-6125. **Circle 368**

January 29-31
Buscon/91-West

BUSCON/91-WEST

Santa Clara Convention Center, Santa Clara, CA. More than 150 exhibits will be featured at this bus- and board-systems conference. Technical seminar topics include Futurebus+, VMEbus, Multibus II, PC bus platforms, embedded controller/systems programming, emerging bus architectures, and military applications. Information: Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856-4990, (800) 243-3238. **Circle 369**

February 5-7
AFCEA 2nd Annual Military/Government Computing Conference and Exposition

AFCEA

Hyatt Regency Crystal City, Arlington, VA. The exposition will offer the latest in computer software and hardware products to link military and government needs with the latest industry technologies, applications and services. The conference will also feature tutorials and technical tracks. Information: AFCEA Programs Office, 4400 Fair Lakes Ct, Fairfax, VA 22033-3899, (703) 631-6125. **Circle 370**

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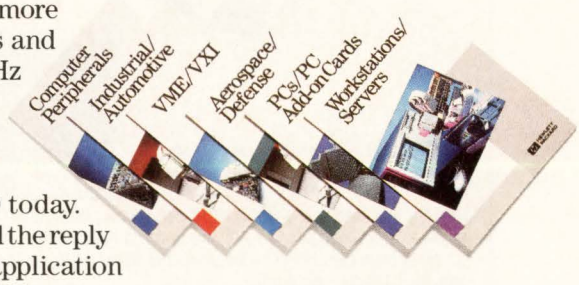

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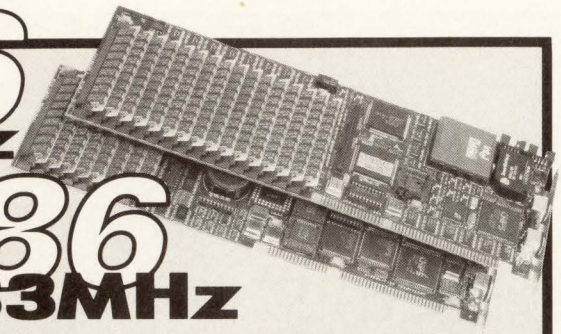

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CIRCLE NO. 15

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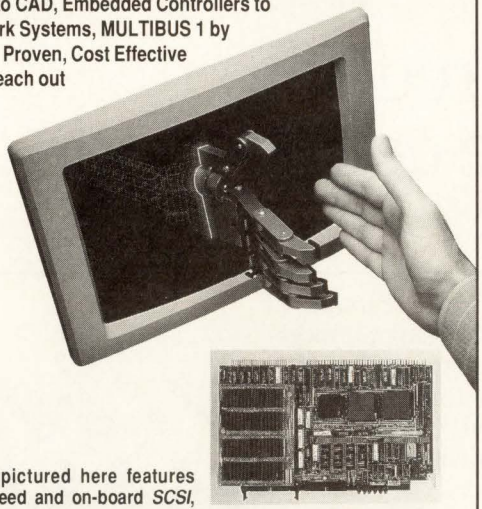

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CIRCLE NO.16

COMPUTER DESIGN

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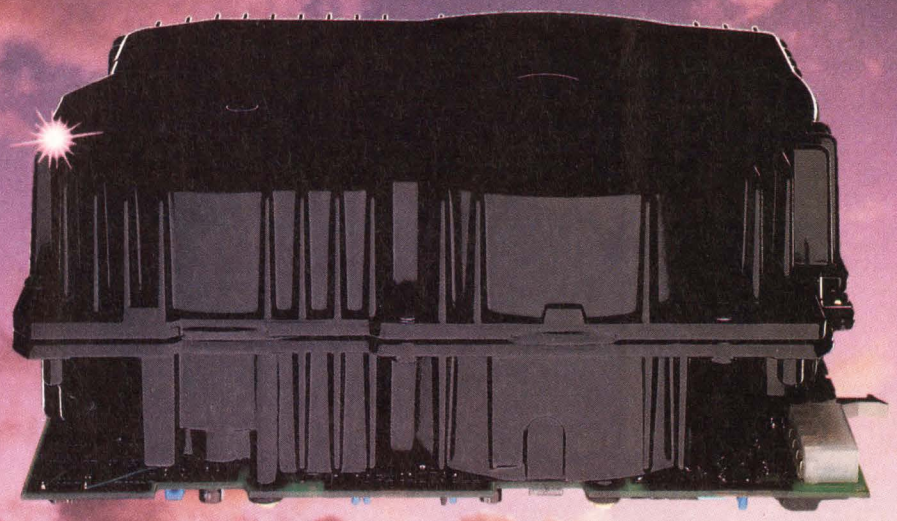

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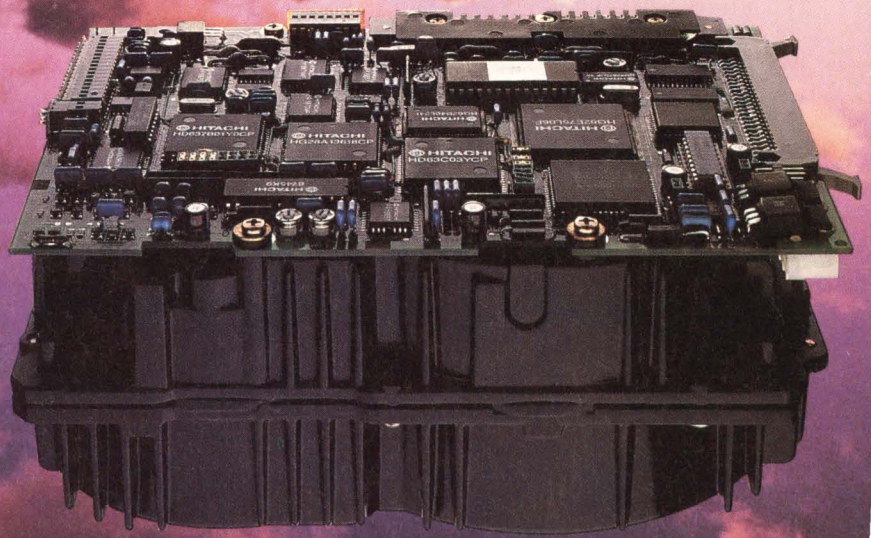

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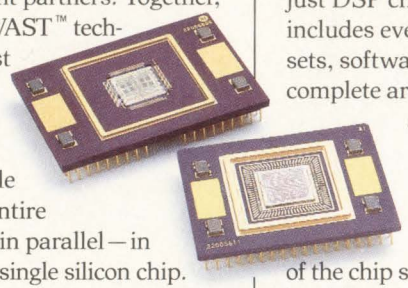

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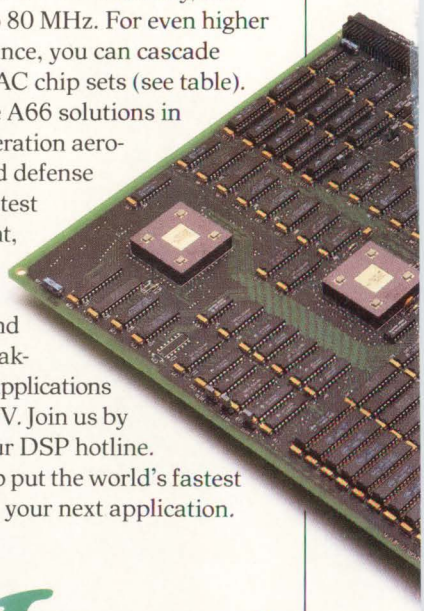

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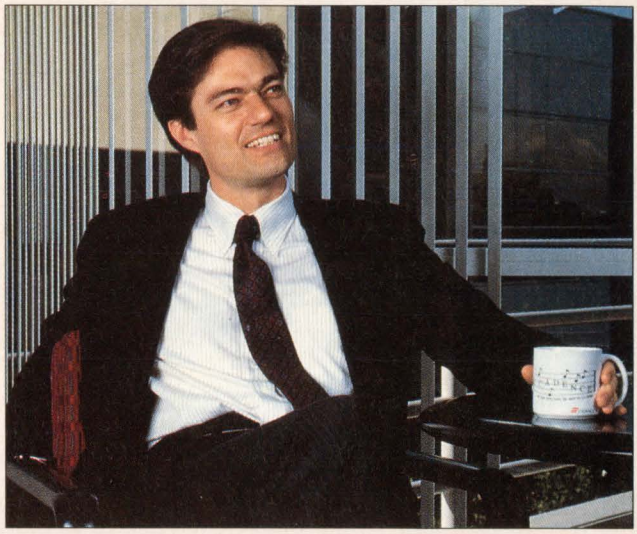
Joe Costello on: Concurrent Engineering



As the electronics industry enters the '90s, electronics manufacturers face greater challenges in delivering higher-quality, more-sophisticated products in ever-shortening market windows. Design automation can play a major role in helping organizations meet this time-to-market challenge.

Design automation is no longer simply a set of drafting tools or complex switch simulators available to a handful of designers. Instead, design automation delivers a broad range of capabilities that are now used throughout the product development process. To meet the market challenges of the '90s, organizations are looking to change both the way they approach individual engineering tasks and the entire design methodology.

An emerging design methodology that has received much attention, concurrent engineering is a methodology customers are addressing with design automation. This methodology promises to be a major factor in accelerating product development (see "Concurrent engineering: the official definition," p 22).

The goal of concurrent engineering is to shorten significantly the product development process by reducing the number of design iterations that result from failure to consider issues such as manufacturability or reliability early enough in the design cycle. In this context, design automation provides a key part of the infrastructure through which a company can begin to use concurrent engineering techniques.

But concurrent engineering isn't a product. A customer can't buy concurrent engineering from an EDA vendor. Customers must implement new design methodologies. Still, they can augment the process by using computer-based facilitators. It's important to differentiate between methodologies, such as concurrent engineering, and computer-based facilitators, such as design automation.

There is no one correct way of implementing new design methodologies. An organization's ability to implement successfully a methodology such as concurrent engineering is highly dependent on changes in design philosophy in an organization, and on the type of products being developed.

It's also important to understand that the role of design automation in concurrent engineering isn't limited to a set of technical requirements that any single CAD vendor can deliver. Multiple design automation disciplines and vendors within EDA, as well as mechanical CAD and CAM, should be able to be used in any concurrent engineering implementation.

Customers can augment the concurrent engineering process by using a computer-based facilitator such as design automation.

The responsibility of EDA vendors in helping customers meet the challenges of the '90s therefore goes beyond just providing products that might be labeled as concurrent engineering. Vendors must deliver the solutions, frameworks and tools that make it possible for customers to build environments that best suit their design requirements and methodologies. This, in turn, implies that the EDA industry must drive and support a broad set of standards within EDA. These standards must reach out to other design disciplines so that customers can choose the mix of suppliers that meets their requirements.

Customers that implement concurrent engineering must address the organizational and computer-based structures and communication mechanisms. Design automation is a facilitator that can help an organization change its design practices, but it's not a substitute for making those cultural changes.

Although not a magic formula, design automation will have a profound impact on the proficiency with which a methodology such as concurrent engineering is implemented and practiced. As noted in the sidebar, computer-based initiatives are critical to concurrent engineering in that they provide an infrastructure to support the organizational changes.

There are three key initiatives that EDA vendors

Concurrent engineering: the official definition

The Institute for Defense Analysis (IDA) report on concurrent engineering says it's "a systematic approach to the integrated, concurrent design of products and their related processes, including manufacture and support. This approach is intended to cause the developers, from the outset, to consider all elements of the product life cycle from conception through disposal, including quality, cost, schedule, and user requirements."

Organizations that adopt concurrent engineering try to get designers to identify critical dependencies between disciplines early in the design cycle. They do this by institutionalizing the process by which design teams explore optimization alternatives so that design changes will least affect the cost and duration of a project.

Though changing organizational behavior is always difficult at best, the benefits often outweigh the costs. The findings of an IDA survey of 11 companies that adopted some degree of concurrent engineering showed that it could shorten time-to-market. The study claims that concurrent engineering contributed to the following results: a 50 percent reduction in engineering change orders in early production; a 40 to 60 percent reduction in development cycle time; a 30 to 40 percent reduction in manufacturing costs; and a 75 percent reduction in scrap and rework.

The consistent comment among those that have adopted concurrent engineering is that there's no one best way to implement this methodology. However, the IDA survey did identify three complementary initiatives associated with successful implementation, and all the success stories placed varying degrees of emphasis on each of them. These three initiatives include engineering process initiatives (such as the formation of multidisciplinary teams), computer-based support initiatives, and the use of formal methods.

Engineering process initiatives are actions taken by management to improve the organizational structure and design process used to develop products. This requires making whatever cultural changes are necessary (often a difficult task) to increase communication between design disciplines.

Computer-based support initiatives are the installation of facilitating technologies such as design automation and verification tools, frameworks, and integrated design environments. Levels of sophistication vary, but a common theme is a drive to establish a design framework to provide consistency and compatibility of tools within and between design disciplines.

Formal methods vary greatly and are difficult to tightly categorize. They are best described as "a range of quality engineering techniques used to manage system trade-offs and to find optimum design and production process parameters." The fundamental goal of formal methods is to incorporate a scientific approach to identifying problems and solving them.

As is true with any major change in design methodology, successful implementation of concurrent engineering will be driven by new technology combined with substantive organizational realignment and cultural change. So significant commitment and participation is required by management to support the implementation of concurrent engineering.

and the EDA industry must adopt to support organizations' efforts to implement new design methodologies such as concurrent engineering. They are as follows: delivering open solutions that can be used with concurrent design practices; supporting industry standards to increase customers' flexibility and choice in building custom environments; and practicing what we preach, especially with regard to delivering quality products on schedule.

Open solutions

First, we must deliver open solutions that can support our customers' ability to automate the methodologies of their choice, including concurrent engineering. And the biggest step toward providing open solutions is propagating the use of design frameworks.

Within the realm of concurrent engineering, the key technical issue is to provide a framework that supports the flow of information between tasks, engineers, and the overall product development process. Different types of information flow are required for different concurrent processes.

An ASIC designer, for example, needs to know his design data and will want to see major changes to board logic, but will not want to know about every change related to the board layout. Only when the board layout designer has reached a certain level of completion in his design tasks will the information become relevant to the ASIC designer. Design frameworks provide the most efficient infrastructure for facilitating the right level of communication between tasks, and allowing an organization to extend and modify a design environment.

There are three levels at which frameworks can support concurrent engineering practices:

- Tool to tool during the engineering process;
- Designer to designer within an engineering team;
- Team to team.

At these levels the frameworks must be open. In any one environment, tools and frameworks will be supplied by multiple vendors. Reality suggests that no one vendor can provide the best-in-class tools spanning the entire development cycle. So frameworks must have the capability to integrate third-party commercial tools, proprietary tools, and other frameworks seamlessly into the design environment.

Information concurrency

It's useful to consider the different classes of user organization as levels in a hierarchy for implementing design concurrency. At the first level, one engineer could be using two or more tools together so that changes in a basic logical or physical representation of a circuit are rapidly reflected in the analysis tools. In the classic case, the engineer might be using a gate-level schematic design tool with a digital simulator, though in today's design environments he also might be using behavioral models, synthesis and

timing analyzers on the same circuit.

Ideally, in this first case, changes in the schematic design tool or in the logic simulator are reflected in the other as the engineer debugs the circuit. An update in the logic produces a change in the results of the analysis.

At the second level, several members of a team are working together on a single project. The project might involve digital designers, analog engineers, or printed circuit board or IC layout specialists. They may be sharing several tools integrated on one framework, different framework-based systems, or standalone tools with no explicit framework and from different vendors.

Within the second level, the information concurrency required can be very different. Every change made by each engineer shouldn't necessarily be communicated, nor should all data used by one engineer be downloaded to another. According to an organization's policies and methodologies, only relevant team data will be exchanged.

For example, engineers might have private workspaces where logic design iterations can be made, and policies would exist for how work should be checked into a central design space. Likewise, printed circuit board layout data would be checked in only after it has passed manufacturability tests. At that point, logic designers would receive only the layout data that was relevant to back annotation or logic simulation.

A key technical issue is providing a framework that supports different types of information flow.

At the third level, multiple teams from completely different disciplines are working as part of a single design environment. Mechanical, electronic, manufacturing, and computer-aided software engineering teams with different frameworks and tools from multiple vendors are working together. Again, very different types of information concurrency, subject to an organization's policies, are required. Much as in the team design process, only subsets of the data are transferred between teams. These subsets reflect major changes in the project. This information concurrency will be governed by release procedures, engineering change order policies, and other company-specific processes.

It's essential to recognize that each level of concurrency is highly dependent on the tasks, on the mix of vendors and tools, and on a company's methodology and policies. Different framework facilities are needed to support each class of data interchange and concurrency. Multidisciplinary engineering teams from different departments will choose the EDA, CASE and mechanical tools that best meet the requirements of a specific design, and integrate them into this environment.

This is why it's so essential for us, as EDA vendors, to deliver open framework-based solutions. The frameworks provide the glue that links the design teams and individuals together. Just as there's no single "right" set of tools needed for design, there's no one way to implement concurrent engineering. We must deliver the products and solutions that make it possible for a customer to take advantage of design automation in the context of the organization's methodologies and policies, whether it's concurrent engineering or another approach.

Promoting industry standards

Openness, as provided by any one vendor, isn't enough, however. The EDA industry must evolve to the point where we collectively can provide customers with the flexibility to build solutions to best support their design processes. Truly open solutions will only become a reality if we as an industry band together to drive real industry standards such as frameworks and electronic data interchange.

Creation of the CAD Framework Initiative (CFI) was the first essential step in defining meaningful industry standards to support users' requirements for building their solutions. The CFI has already taken major steps toward the development of guidelines for frameworks in some areas. A demonstration was presented at the Design Automation Conference last June, and vendors can move toward the overall proposal by adopting known standards such as Unix and the X Window System.

The first guidelines from CFI are scheduled to be released by mid-year 1991. We, as an industry and as vendors, must commit to implementing these guidelines in our frameworks, where appropriate, within one year of the standards' release. In other words, make the CFI guidelines real in 1992. Achieving this goal depends on real commitment of technical and business resources from CFI participants to drive the standards process.

Where should we be going?

Another step the EDA industry must take is to practice what we preach. The EDA industry has received notoriously low marks on delivery of high-quality solutions in a timely fashion. As individual companies, and as an industry, we need to invest in methodologies that will help us to correct this behavior. We need to instill the "quality first" philosophy and make the necessary changes in our design processes so that our stated product goals are actually supported.

And we need to keep the big picture in mind. Our basic charter as EDA vendors is to develop solutions that enable customers to deliver more sophisticated, higher-quality products in ever-shortening market windows.

But electronic design is only one of many functions that are necessary to get quality products to market, and today we're looking at only the first standards proposal from CFI. The EDA industry needs to continue to drive the standards initiatives for its own products, and to expand its framework vision to interconnect with other parts of the design process. Only then will we have done our job, as vendors and as an industry, in supporting our customers in their efforts to achieve the engineering and time-to-market challenges of the '90s.

Joseph Costello is president and CEO of Cadence Design Systems (San Jose, CA).

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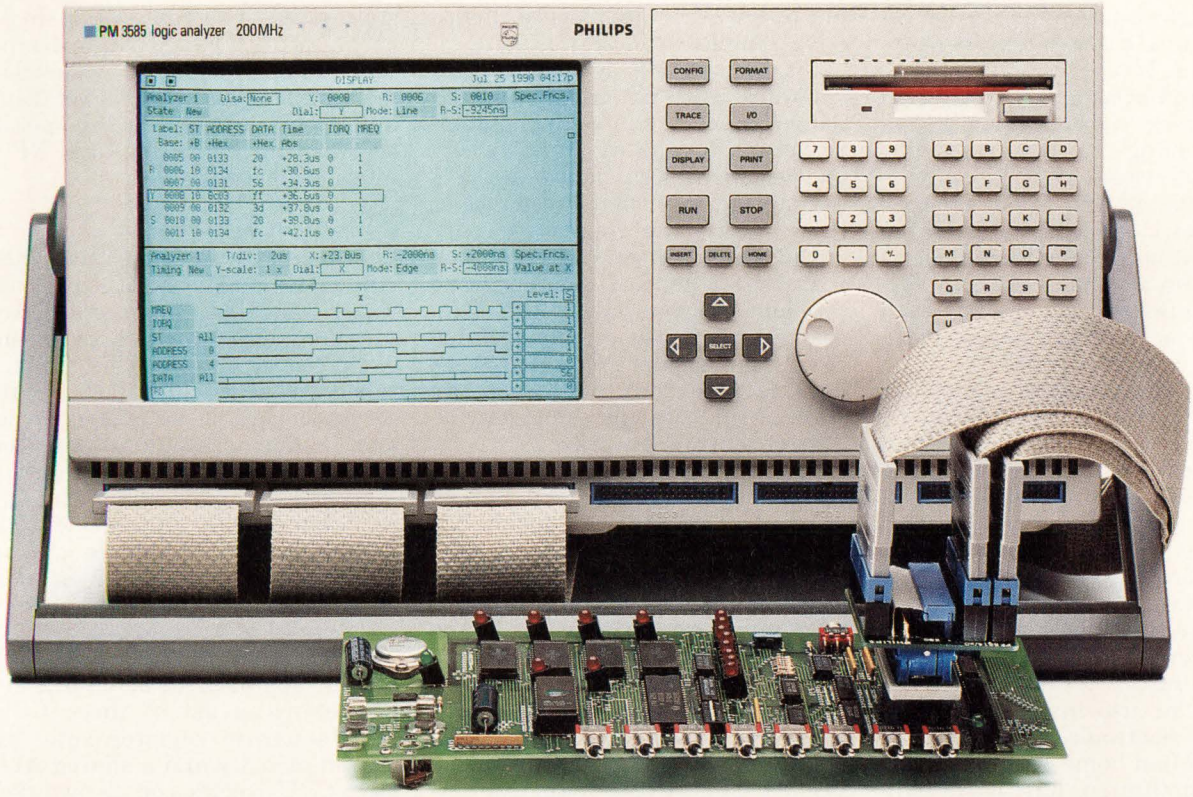

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INTEGRATED CIRCUITS

Controller-level network could revolutionize connectivity

Ron Wilson, Senior Editor

A LAN would be the perfect solution to many control problems. If you could just put the sensors and actuators of your VCR on a network, you could save a bundle on cabling and drivers. If you could connect your VCR, kitchen appliances, lights and climate control on a network, you could achieve the automated house. Similar thoughts have driven auto makers, manufacturing equipment vendors and even the designers of office towers to investigate control networks.

But existing network technology can't do the job. Ethernet and its relatives are comfortable only with large data packets, not with the small messages common in device control applications. Software for the seven-layer International Standards Organization protocol stack is too big and expensive to put in 8-bit microcontrollers. And the hardware cost of an Ethernet node—even with the latest 10Base-T technology—is far too high for use inside a piece of consumer electronics, an automobile or a suburban home.

These limitations have led designers to try other approaches. Inside boxes, engineers have tried point-to-point wiring with synchronous serial interfaces—a common approach for small networks of 8-bit microcontrollers. On larger designs a variety of specialized local networks have sprung up, such as the Controller Area Network for automotive use.

But now a Silicon Gulch start-up may have a general solution to the problem. Echelon (Palo Alto, CA), started by Apple cofounder Mike Markkula, has developed a network architecture that addresses the throughput, cost and complexity issues of control networks.

"Back in 1986," says Echelon vice-president of marketing Beatrice Yormark, "Markkula was wiring his house. He wanted to be able to centrally control most of the electrical things in the house, but the problem of running control wiring to all the individual pieces was a nightmare. There were control systems that used power lines for communication, but they weren't reliable enough to count on. He realized that what he needed didn't exist—a control network with a reliable protocol and the ability to use all the media at hand, but costing only about $10 per node. So he started another company."

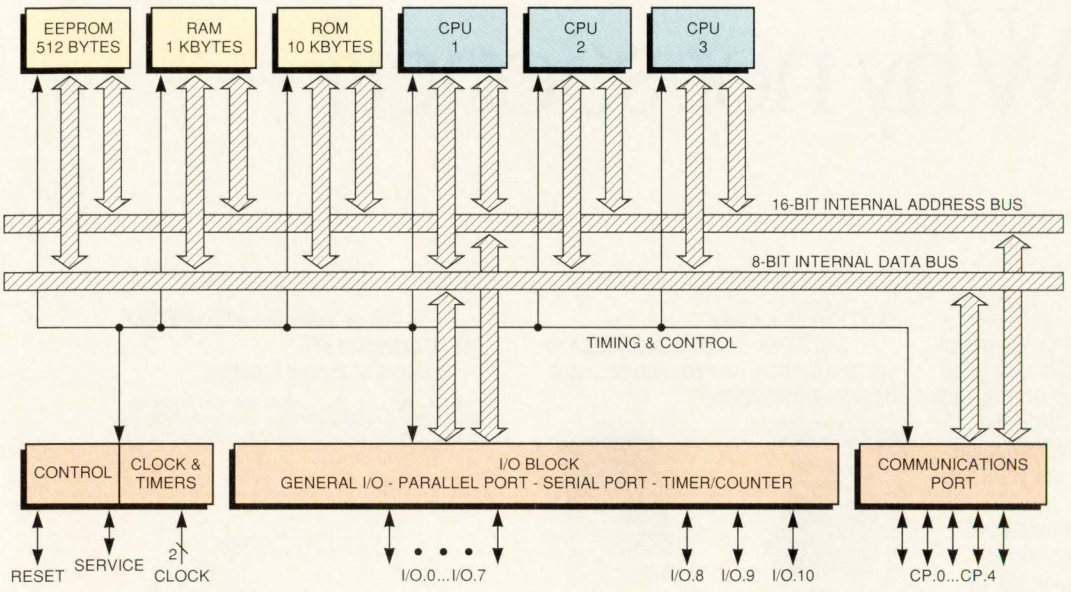
Echelon calls its development a LON (Local Operating Network). The architecture includes an ISO-style seven-layer protocol, a single-chip network termination, operating and protocol software, a development system, and a variety of transducers that let the network operate over any medium from local RF to infrared to power lines.

Silicon at the center

The only way Echelon could meet vice-chairman Markkula's cost criterion was by designing the architecture around the capabilities of a single piece of silicon. This focus is called a Neuron chip. Each Neuron serves as both network termination and, in many cases, local microcontroller for the device it connects to the network. This means the chip must handle the entire seven-layer ISO protocol stack, including an application layer that often includes simple control algorithms. That's a substantial computing order.

To meet it, Echelon developed a unique approach to on-chip multiprocessing—a set of three CPUs with separate register sets, but shared memory and a shared ALU. Each CPU executes on its own cycle

ECHELON'S NEURON ARCHITECTURE



The Neuron chip, the heart of Echelon's Local Operating Network, combines two dedicated CPUs that handle layers one through six of the network protocol, with a third CPU for applications. The three processors share various flavors of on-chip memory and an array of simple I/O devices.

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CIRCLE NO. 20

INTEGRATED CIRCUITS

of a three-phase clock, allowing the processors to share hardware. "You have essentially three 1-Mips CPUs in the chip," explains Echelon vice-president of engineering Michael Gilbert. "To achieve both low cost and concurrency, we dedicated the CPUs to separate functions."

One of the specialized Echelon processors is dedicated to the media access control layer of the stack, another handles layers two through six, and a final CPU—this one available to the user—handles layer seven, the application layer. "The user sees a stack-oriented C engine," Gilbert says.

The lower two CPUs operate transparently, their services available to applications through a set of system calls in a ROM-based multitasking kernel. So the user just works with variables that may be shared with other applications on other Neuron chips.

In addition to having the network connection, the user has enough resources to perform a simple control application. The Neuron contains 1 kbyte of SRAM, 512 bytes of EEPROM—where users would normally put their application code—and a variety of serial ports, parallel ports and counter/timers.

For more-involved applications, the Neuron will need to work with additional I/O and processing chips, and perhaps additional memory. In these situations, the Neuron can act as an 8-bit peripheral chip to a conventional microcontroller. A version of the Neuron will also be available with 2 kbytes of SRAM and, in place of the ROM, an external memory interface. This permits the device to reach up to 64 kbytes of external memory, and provides an emulation chip for development.

Onto the network

The Neuron actually talks to the LON through a special pair of pins called a LONtalk port. In one mode, the port communicates in differential Manchester-encoded data streams. "For simple applications where you're communicating within a box, you don't need a transceiver—you can just let the Neuron chips talk to each other," Gilbert maintains. But when the devices are connected through more-complex media, such as power-line modulators, the chip needs external Echelon-designed transceivers. Some of these transceivers use their own modulation schemes and need to control the data rate of the LONtalk port, so a second, handshaking mode is available for interfacing to them.

The Neuron implements a quite sophisticated network over its variety of media. The protocol is basically collision-sensing, but with retry algorithms that improve predictability and maintain maximum network bandwidth on saturated networks, according to Echelon. In addition, the scheme provides for prioritized messages and master/slave polling arrangements.

The LON may be a gateway to new levels of automation, not just another technology in which a design can become mired.

■■■

The underlying network runs at a maximum rate of around 1 Mbit/s, although this is highly medium-dependent. Echelon claims to get only about 10 kbits/s through a power line, for instance. Everything, from the architecture of the CPUs to the memory size to the protocol, is optimized around small messages—typically 10 to 15 bytes. This choice clearly reflects the LON's bias toward control applications, and away from the big packets used for transferring files on Ethernets.

Using these small messages over a 1-Mbit/s link, the network can handle about 800 packets/s, according to Gilbert. A single Neuron chip can process about 100 to 150 packets/s.

Help for developers

One barrier that Echelon will face is social, not technical—most of the target customers for the LON concept aren't experienced network developers. Instead, they're system designers interconnecting the subsystems in an appliance or television, or automotive engineers laying out the instruments, sensors and lights on a new car, or architects designing the HVAC (heating, ventilation and air conditioning) systems for an office. These people don't intend to take the summer off to learn about ISO networks.

Echelon has taken several steps to solve this problem. First, the workings of the network have been rendered as transparent as possible. One can simply program the Neuron application CPU in C or assembler, declaring network-global variables and using LON system calls to the embedded operating system. Second, the company has put together an elaborate development environment, including object-oriented development software, a C compiler for the Neuron's application processor, a ROM-based executive, a Neuron emulator, prototyping aids, evaluation boards for the Echelon transceivers, and a protocol analyzer. All these capabilities are configured around a PC/AT.

The company also recognizes that such a novel idea, no matter how valuable, can be hamstrung if it's available only from a start-up. "From the beginning," says Yormark, "our strategy has been to develop the technology and then license it, so that the idea can spread rapidly." Hence the Neuron chips aren't actually built by Echelon. Rather, they're being introduced by Motorola (Austin, TX) and Toshiba (Irvine, CA).

With a combination of novel technology, seasoned management and powerful partners, Echelon is in good shape to support rapid growth. But perhaps the most significant ingredient is the system-level solution that Echelon has devised, leaving almost nothing of the network architecture to be dealt with by the user. This may make the LON a solution to system design problems and a gateway to new levels of automation, not just another technology in which a design can become mired. ■

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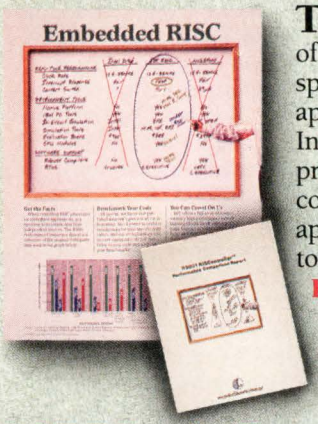

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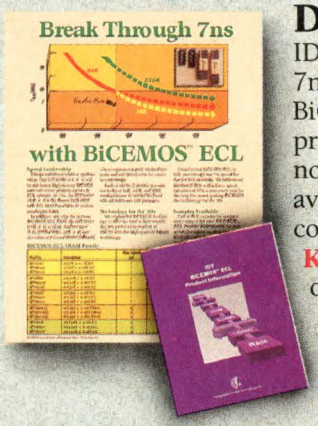

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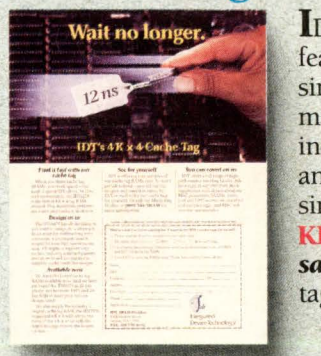

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CIRCLE NO. 21

DESIGN AND DEVELOPMENT TOOLS

Network-distributed processing reduces run times for complex designs

Barbara Tuck, Senior Editor

The elongated run times of increasingly complex IC and board designs have forced silicon and software vendors alike to chase after network-distributed processing. ASIC designers are finally getting a taste of the productivity promised by multiple CPUs operating in parallel as a handful of design tools with network-distributed-processing capability become available.

The trendsetters include the Concurrent Compiler Version 1.0 from Vantage Analysis Systems (Fremont, CA); the Parade ASIC place-and-route tool from Mentor Graphics' Silicon Design Division (San Jose, CA); the Explorer CheckMate IC verification tool, the result of a codevelopment effort between Mentor's Silicon Design Division and Texas Instruments (Dallas, TX); the LRC-2000 full-chip layout rules checker from Integrated Silicon Systems (Research Triangle Park, NC); and the Configuration Accelerator from Quickturn Systems (Mountain View, CA).

The Vantage Concurrent Compiler, the first of its kind for VHDL, went into beta test last month at the Avionics Division of Honeywell. The compiler divides a VHDL design into subsections for parallel compilation. It determines the sections of the source code that can be executed simultaneously, accesses unused resources across the user's network, and then runs the design sections concurrently. Vantage vice-president of marketing John Willey says that according to early indications, it seems that network-distributed processing will speed up VHDL compilation for Concurrent Compiler users as much as 10 times over single processor execution. At present, the compiler runs on a homogeneous network but will be upgraded to run on heterogeneous networks.

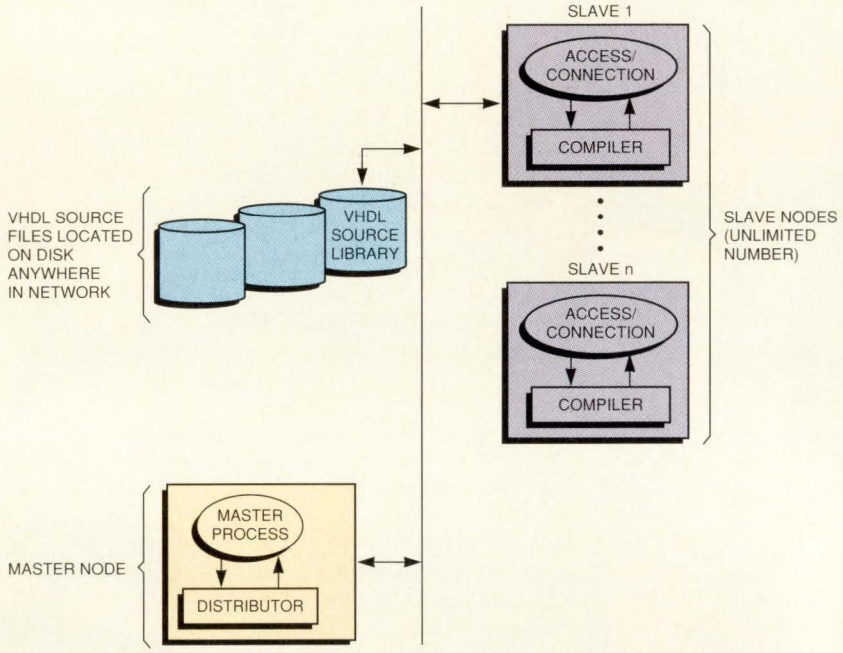
Failure not fatal

Absolutely key to the Concurrent Compiler is what Vantage calls its failed-process-recovery capability. Simply put, if a node goes down in the middle of a job, the user won't lose everything and have to start over. Instead, even when the compiler is unattended, the host server will detect slave node failure or a communications breakdown and will determine whether to resubmit the failed job to an alternate node. Even if a module fails because of user error, the compiler will continue to run concurrent modules that aren't dependent on the job being done by the failed module.

The complexity of VHDL makes network-distributed processing applications in that language more difficult than applications in C, for instance. The difficulty with VHDL is that the dependency list is so complex. When compiling a 50,000-line source file, one has to partition the design so that a portion not dependent on anything else will run first, so that interdependent tasks will run simultaneously, and so that run times for tasks dependent on the completion of other tasks will be appropriately delayed.

Will Vantage, whose VHDL simulator is one of the most respected on the market, eventually extend network-distributed processing to simulation itself? Vantage's Willey says that no one has been able to distribute simulation among multiple CPUs yet. "As complex as dependencies are in VHDL," he says, "they're nothing like the dependencies that exist in different pieces of a simulation." According to Willey, Vantage has assembled a research team to work on a concurrent simulator, but no product plans have

VANTAGE'S CONCURRENT COMPILER



With the Vantage Concurrent Compiler, VHDL compilation can be distributed among multiple processing nodes on a network. After VHDL source files are read, design units are sorted according to dependencies. After establishing connection to the slave nodes, the master starts compiler processes on each, sending compilation units in order of dependencies. If a slave connection is lost, its job is resubmitted to an alternate slave or executed locally.

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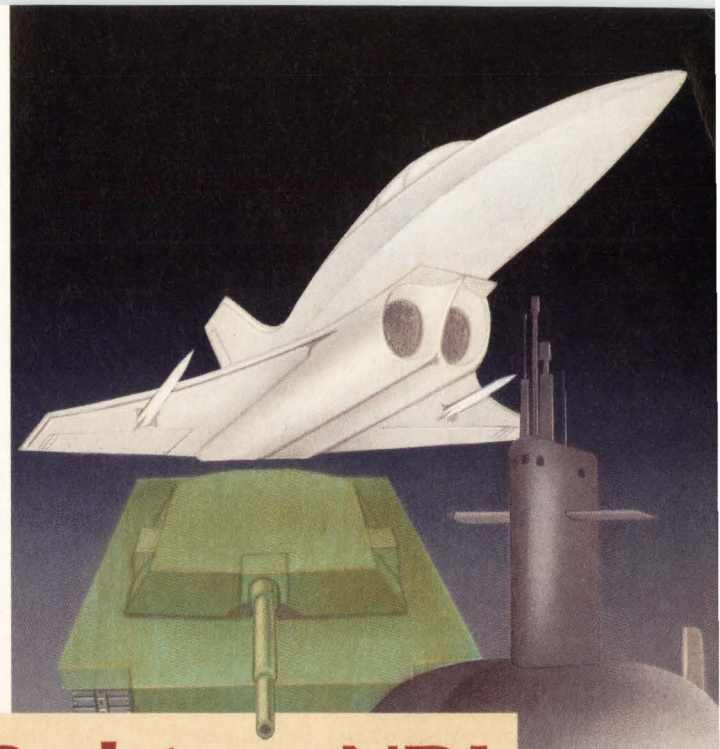

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CIRCLE NO. 22

DESIGN AND DEVELOPMENT TOOLS

been determined yet.

For the better part of a year, Valid Logic Systems (San Jose, CA) has been applying network-distributed processing to Spice-level simulations on its Analog Workbench II. Valid software sorts through Spice simulation pieces—both multiple-run analyses and individual simulations—and assigns them to run concurrently on multiple nodes of a heterogeneous network. A limiting factor at present is that if disrupted, a job terminates.

Solbourne Computer (Longmont, CO) is just one of the companies chasing after network-distributed processing as applied to high-level simulation. Meanwhile, Solbourne reconfigures its network at night to distribute multiple-run simulations among a bunch of compute servers. But that's a far cry from breaking up a single simulation into pieces, admits Solbourne.

It's not surprising that Cadence Design Systems (San Jose, CA) is actively pursuing the capability to apply network-distributed processing to high-level ASIC simulation.

"Network-distributed processing makes the best utilization of existing resources on the network."

—Kevin Curtis, Mentor Graphics

According to Tony Zingale, Cadence vice-president of corporate marketing, the company is working with Sun Microsystems (Mountain View, CA) on the software architecture details required to use parallel processing with Verilog. And Cadence has teamed up with the University of California at Berkeley in another network-distributed-processing project that involves the rewriting of Verilog so that it can be multithreaded. It's likely that Cadence won't be the only vendor to explore the ability to thread algorithms through multiple CPUs within a single machine.

Layout partitioned, too

Parade from Mentor is the first ASIC place-and-route system to offer network-distributed processing. With between five and 10 parallel processing nodes, Mentor is claiming a speed increase of about 10 times due to distributed processing. A disk-resident database lets Parade recover quickly from interruption and enables the software to place and route a 50,000-gate array in less than 16 Mbytes of main memory. Users can

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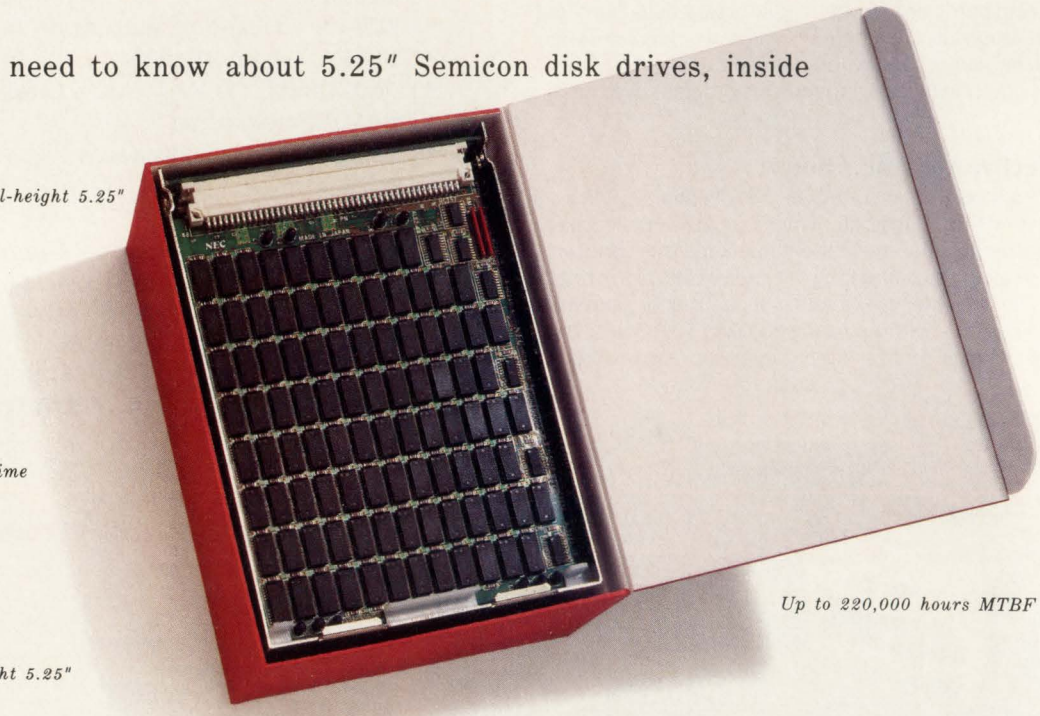

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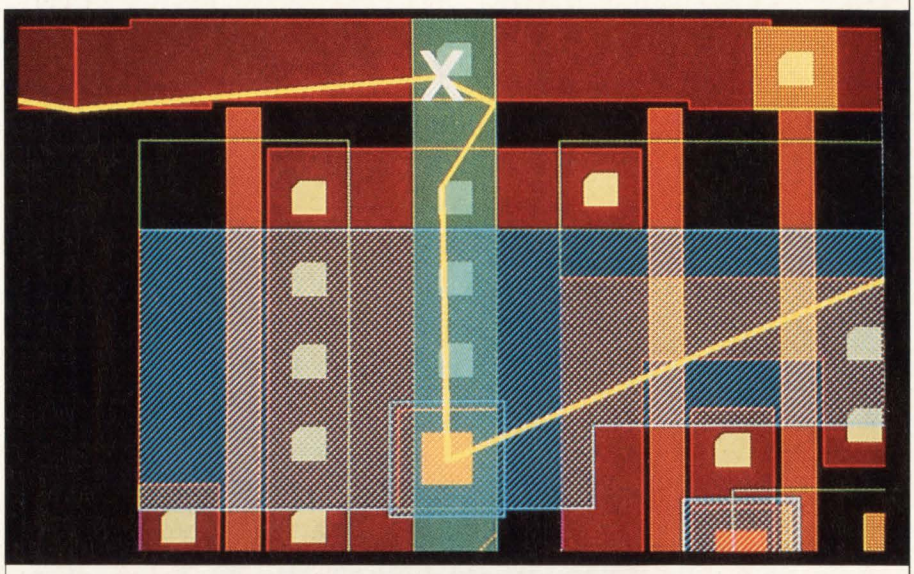
divide their task among heterogeneous network nodes at each layout phase.

Parade had its origins as the René gate array place-and-route tool, developed by Descartes Automation Systems about two years ago. Silicon Compiler Systems, now Mentor's Silicon Design Division, acquired the René tool when it purchased Descartes.

Network-distributed processing is also featured in Mentor's Explorer CheckMate IC verification tool. Intelligent parallel processing algorithms in CheckMate allow rules to be shared by other nodes. Mentor claims that CheckMate can achieve run-time improvements of up to an order of magnitude over single-processor verification systems such as Cadence's Dracula.

"Network-distributed processing makes the best utilization of existing—but often idle—resources on



Mentor's Explorer CheckMate IC verification tool uses intelligent tracing algorithms to provide graphical displays of information for debugging errors, such as these geometries causing a short between two signals. The tool distributes processing on homogeneous networks, but should run on heterogeneous networks soon.

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CIRCLE NO. 23

DESIGN AND DEVELOPMENT TOOLS

the network," says Mentor director of engineering Kevin Curtis. Though the new verification tool initially runs on homogeneous networks, the company plans to make it compatible with heterogeneous networks soon.

Explorer CheckMate is the result of a codevelopment effort between Mentor and TI. The core technology of CheckMate, including distributed processing algorithms, is TI-proven technology. Mentor has extended that technology to develop a product for the general marketplace.

The Integrated Silicon Systems (ISS) LRC-2000 verification tool also offers a parallel processing capability. Users of the hierarchical full-chip layout rules checker can operate the design-rule-checker function simultaneously on multiple workstations, with automatic partitioning and dynamic load balancing, according to ISS.

Both LRC-2000 and Mentor's CheckMate will meet heavy competition from the industry-standard Dracula verification software from Cadence. Though Dracula doesn't yet have a network-distributed-processing capability, Cadence's Zingale claims that sometime this quarter, the software will be given the capability of parceling design rules across multiple network nodes. This brute-force, short-term solution will be followed, he says, by a set of intelligent algorithms optimized for true parallel processing.

Now that it has proven practical to partition compilation, layout and verification tasks among multiple nodes on a network, there will no doubt be a flood of design tools featuring network-distributed processing. Quickturn's Configuration Accelerator, for instance, uses network computing technology to speed up the process of configuring the company's RPM Emulation System for ASIC emulation. The truly significant development for the design community will occur, though, when this technology can be practically applied to simulation—and to VHDL simulation, in particular. ■

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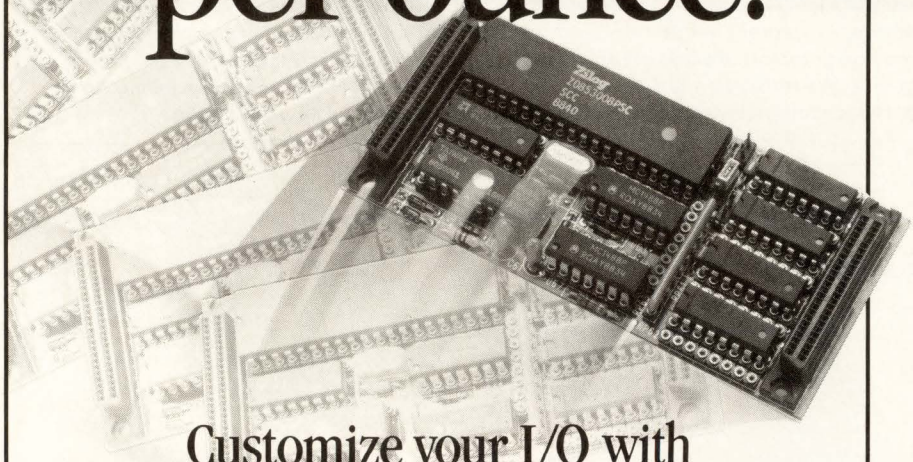

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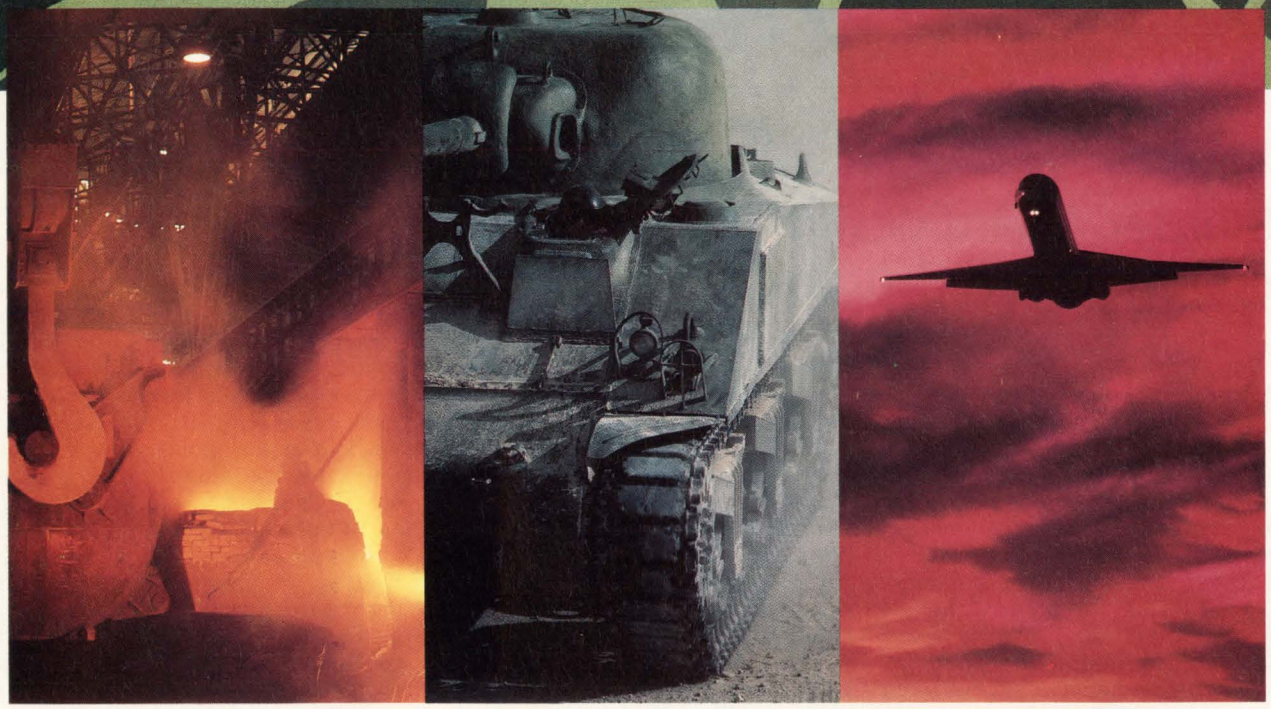

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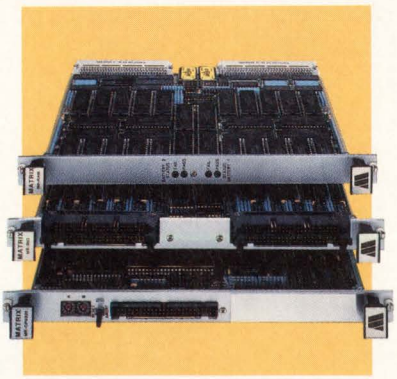

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CIRCLE NO. 25

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DESIGN AND DEVELOPMENT TOOLS

PC-based board design tools take on the workstations

Mike Donlin, Senior Editor

Personal computer-based circuit board design tools are becoming sophisticated enough to give the more expensive workstation-based products a run for their money. At trade shows such as last summer's Design Automation Conference (Orlando, FL), Electro (Boston, MA) and, most recently, the fall Wescon (Anaheim, CA), PC-based design tool vendors have demonstrated comprehensive sets of tools that can be used throughout a circuit board's design cycle, from schematic capture to placement-and-routing to simulation and prototyping.

"There are several forces at work in the PC-based design tool arena," says James Post, president and CEO of Ultimate Technology (Naarden, the Netherlands). "First of all, the increased power of the PC's microprocessor has allowed us to offer features that would have slowed earlier models to a crawl. Secondly, the extended memory capabilities have freed us from the memory budget restraints of the past. Lastly, our algorithms have gotten more sophisticated, which translates directly into faster iteration time in such areas as autorouting."

Ultimate's autorouter, Ultiroute GX, is a gridless, interactive tool that lets designers specify autorouting by window, net or component. Though gridless autorouters have the reputation of being slower than gridded versions, Ultimate has optimized the routing algorithm to increase its speed. According to Ultimate benchmarks, the Ultiroute tool can route a four-layer, 25-sq.-in. circuit board with 40 equivalent 16-pin ICs to 100 percent completion in about 1 hr and 20 min.

The tool does this by running the route several times, with each pass optimizing the design over previous iterations. On each routing run, Ultiroute compares the present trace path to a "shadow board" held over from the previous run. The tool then tries to find better routes with less vias compared to the shadow board.

After 100 percent completion has been achieved, users can sometimes reduce the number of vias further by using optimization runs that let them set parameters to evaluate trade-offs in the route. Via cost, for instance, can be set for any value from zero to 16. When via cost is high, the router will use less vias, but will route in all directions in order to put the trace in. Other parameters such as pin-channel cost, nonpreferred direction and hugging cost can likewise be set until the optimum route is achieved.

Adaptable tools

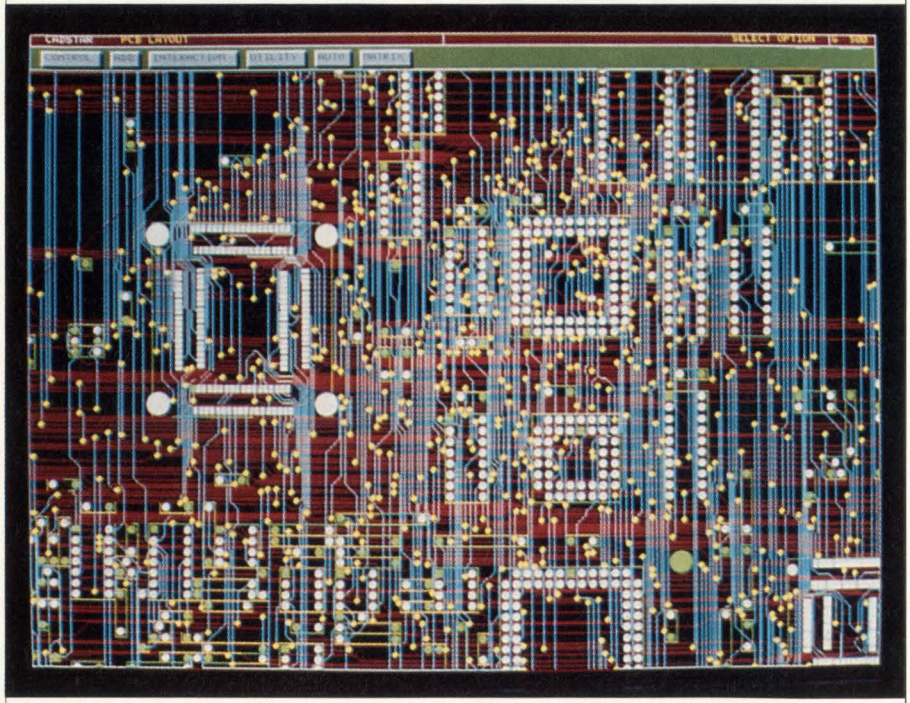
In addition to displaying increased speed and optimization features, PC-based routers have also become more flexible, an attribute that becomes significant in mixed-signal, mixed-package designs. On circuit boards such as these, the autorouter is challenged to find trace paths through the uneven pin spacings typical of ASICs, surface-mount and standard ICs.

"Flexibility is a definite advantage that gridless routers have over gridded ones," says Hal Barbour, vice-president of marketing at Racal-Redac (Mahwah, NJ). "Because the router isn't constrained by a grid, more traces can fit in a given space without violating design rules. With more traces allowed in the same space, denser boards can be routed to 100 percent completion."

Racal-Redac's gridless router, the Cadstar Advanced Router, is designed to handle dense, fine-line surface-mount-device boards. The tool shoves routes aside to make room for more traces and uses rip-up and retry capabilities to place routes until the board is completed to 100 percent. A feature called track fattening automatically produces the maximum possible copper width on user-specified traces.

Analog's special needs

In addition to offering the flexible routing techniques demanded by mixed-package designs, circuit board design tools need features to accommodate the mixed analog/dig-



Dense, fine-line circuit boards with a variety of component packages challenge personal computer-based routing tools. On this board, Racal-Redac's Cadstar tool has routed to 100 percent completion a circuit board with surface-mount and through-hole ICs and ASICs.

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CIRCLE NO. 26

DESIGN AND DEVELOPMENT TOOLS

ital architectures of today's advanced circuit boards. In applications such as power supplies and high-frequency circuits, for instance, signal lines must be protected from interference and crosstalk. Racal-Redac's Cadstar 6 circuit board layout tool accommodates these needs with features that let designers choose the optimum solution to an analog problem.

In high-frequency applications, a right-angle track (or T section) could unintentionally attenuate a signal by setting up a reflection. This transmission-line effect can be avoided if sensitive traces are replaced with curved lines, which Cadstar allows users to do.

Another capability that Cadstar 6 gives users is the ability to optimize circuit board pad shapes. Use of teardrop pad shapes, for example, contributes to the manufacturability of a board. Teardrop pad shapes avoid the acid traps that form in the sharp corners between a circuit board trace and a connected pad, and are particularly important in analog design.

Advanced PC-based board design tools may start to give workstation-based tools a run for their money.

■ ■ ■

Advanced features such as these, which were previously reserved only for high-end workstation tools, are gradually finding their way into PC-based tools. As system vendors adopt concurrent engineering practices that partition a design among a team of engineers, PC-based tools will probably enjoy a secure spot in the design process. In such an environment, some tasks will be handled by PCs, while others will be doled out to the workstations. Such a scenario lets design teams use PCs and workstations as complementary means to the same end. ■

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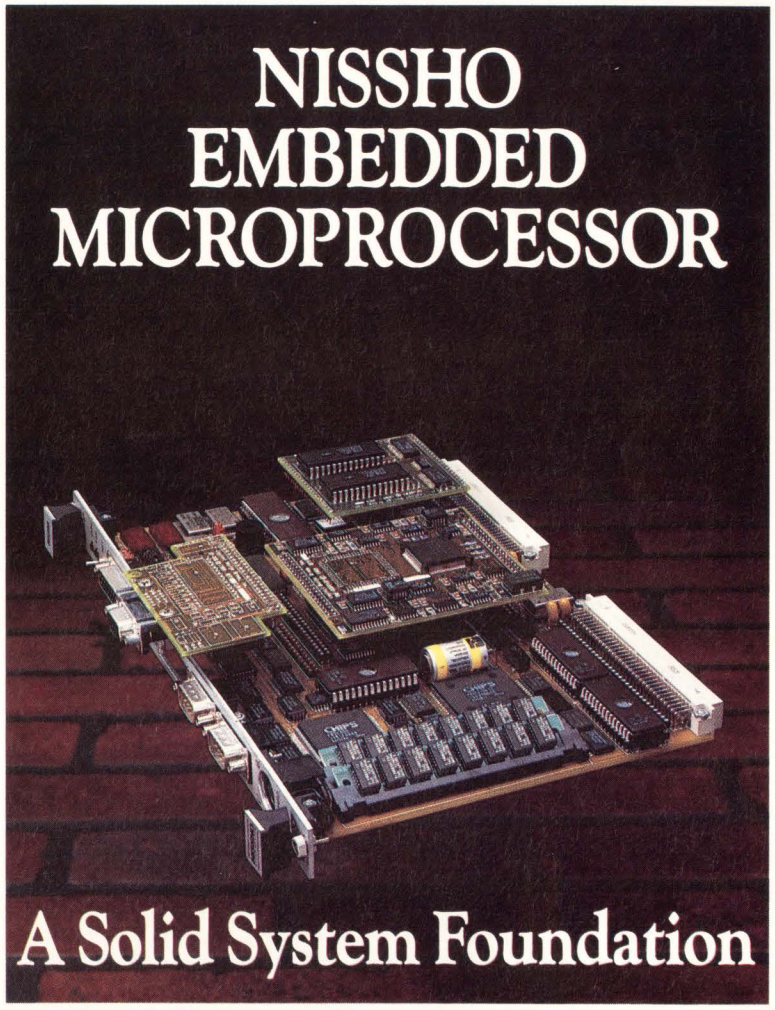

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CIRCLE NO. 28

SOFTWARE

CASE tool adds dynamic simulation of requirements analysis

Tom Williams, Senior Editor

In a major new release of Version 4.0 of its Teamwork integrated CASE environment, Cadre Technologies (Providence, RI) has included several enhancements. The new facilities are intended to make the design process more productive at the higher levels of design hierarchy, and to help companies enter a computer-aided software engineering environment without starting projects over from scratch. The enhancements include a source code reverse-engineering tool called Teamwork C/Rev; an Ada design-sensitive editor, Teamwork/DSE; and a simulation tool, Teamwork/SIM, to animate CASE models such as data flow diagrams and state machines.

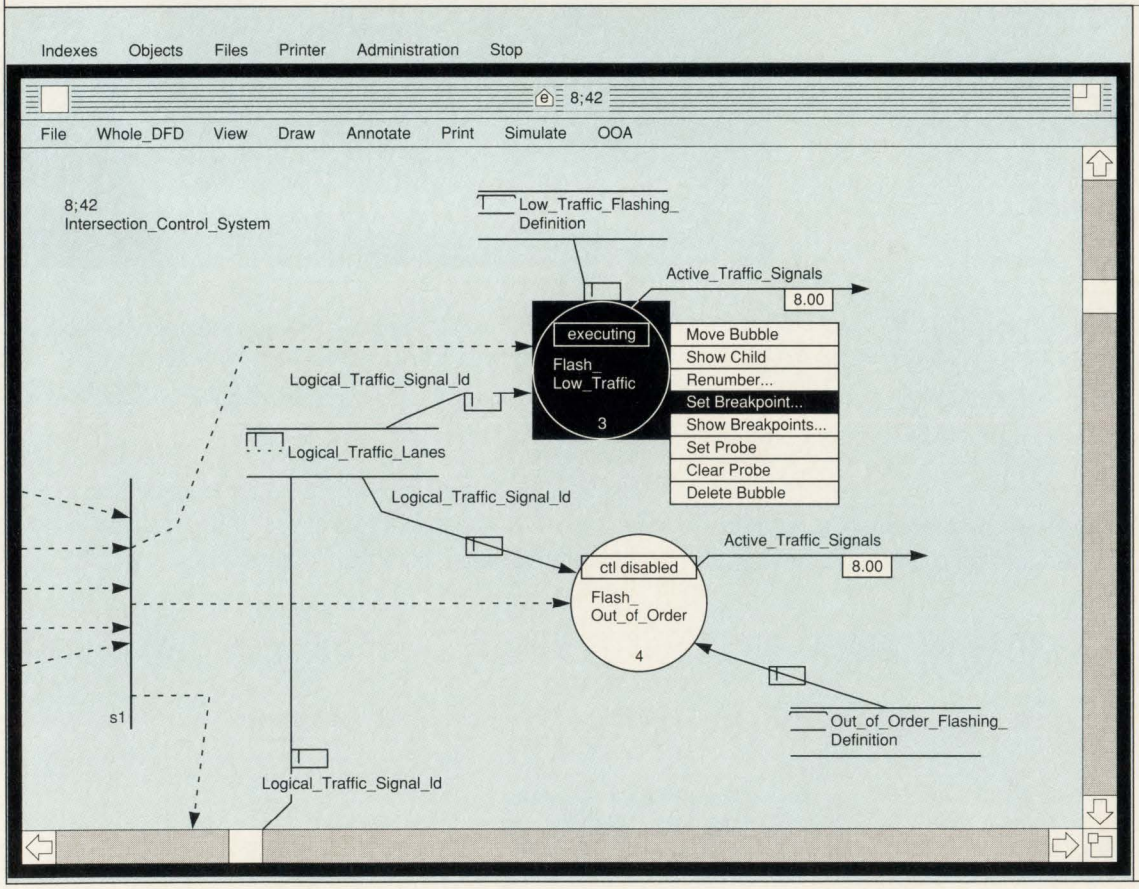
"One of the problems people have had with CASE tools," says Cadre chief technical officer Lou Mazzucchelli, "is that they can draw all the fancy bubbles and arrows and captions, but when they're done, all they've got is a static model that has been checked for consistency and completeness." While Mazzucchelli admits that such models are useful, he claims that they can be dynamic if the user is able to add a little more information. The advantage is that the user can then observe the model at the requirements-analysis stage of a system design project and predict how the system will perform.

The new Teamwork/SIM addition to Teamwork 4.0 essentially animates the data flow diagrams and state machines that form the basis of a real-time structured analysis model. As a result, it's now possible—at the requirements-analysis stage of a project—to see the system changing state in response to external events and see data propagating through the system.

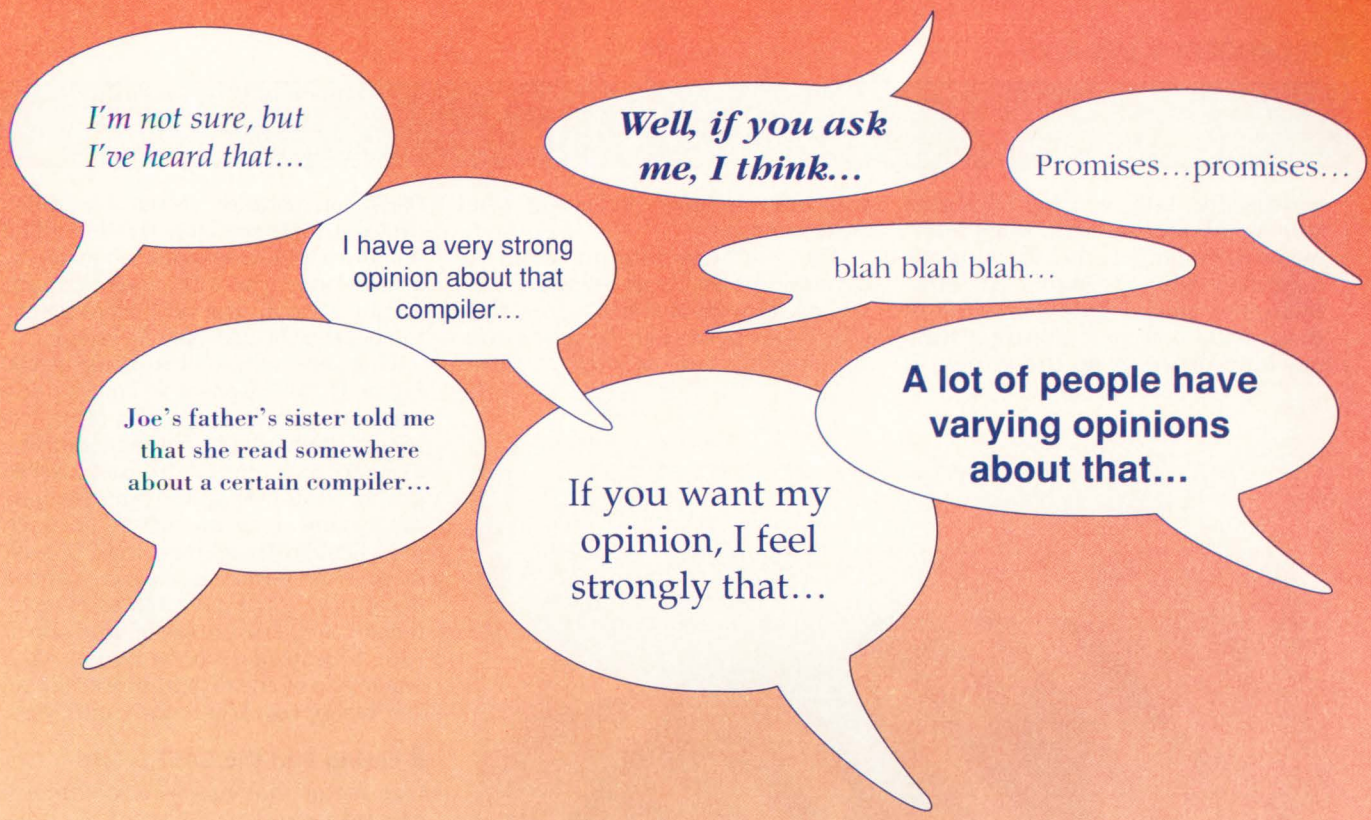
To be able, for example, to see where performance bottlenecks might occur at the data flow diagram stage can save time and effort down the line. In determining the required hardware resources, for example, it's possible to map functions in a model to anticipated hardware and categorize the hardware resources to see if they can do what the system needs. If not, one can change the hardware mapping before ever building a prototype.

Such high-level modeling isn't in itself brand-new, Mazzucchelli admits, but he claims that other such tools either are stand-alone or require a special kind of notation just to build a simulation model. With the Cadre tool, the user need only enter some additional information and the system then builds a "compiled model" for which labels will appear in the data flow diagrams of that model.

Each bubble, for instance, will have a label indicating what state that process is in: running, disabled,



Here, Cadre's Teamwork/SIM tool shows a data flow diagram with labels describing the status of interfaces between processes and the states of the processes themselves, which change dynamically on the screen.



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Sieve Benchmark[1]			
Memory model	*SMALL*	*TINY*	*SMALL*
Total execution time	*6.744 sec*	*8.388 sec*	*8.753 sec*
Module code size	*188 bytes*	*238 bytes*	*266 bytes*
Dynamic data size	*41 bytes*	*96 bytes*	*126 bytes*
Total code size	*1223 bytes*	*1626 bytes*	*1936 bytes*
Memory model	*LARGE*	*LARGE*	*LARGE*
Total execution time	*8.287 sec*	*17.295 sec*	*10.98 sec*
Module code size	*188 bytes*	*343 bytes*	*303 bytes*
Dynamic data size	*21 bytes*	*28 bytes*	*74 bytes*
Dynamic Xdata size	*8238 bytes*	*8259 bytes*	*10,351 bytes*
Total code size	*1292 bytes*	*2088 bytes*	*3467 bytes*
Dhrystone Benchmark[3]			
Dhrystones per second	*203*	*90*	*163*
Single Precision Whetstone Benchmark[4]			
Whetstones per second	*13*	*3*	*(Floating point not yet supported)*
Fibonacci Numbers Benchmark[5]			
Total execution time	*20.88 msec.*	*94.29 msec.*	*368.14 msec.*

1. Erathosthenes Sieve Program from BYTE (1/83), expanded with I/O and interrupt handling. (10 iterations)
2. Currently available only in Europe.
3. Dhrystone Benchmark Program C/1.1 from Reinhold P. Weicker, CACM Vol 27.
4. Single Precision Whetstone Benchmark Program (A001)
5. Fibonacci Numbers Benchmark Program, Embedded Systems Magazine, April 1989

CIRCLE NO. 29

SOFTWARE

waiting for data, waiting for a control signal, and so forth. Each interface will display a label showing the data flow rate through that interface—the initial rate for most of these will be zero. If there's a state machine diagram on the screen, it will have a label indicating what state is active.

The user can interact with the dynamic model via an on-screen control panel with buttons to run, stop, single-step or set breakpoints. Breakpoints can be used at interfaces, for instance, to see if modules are data starved or flooded. The model can be exercised in an interactive mode where the user supplies all the stimuli and sets breakpoints to observe the system's behavior.

Once the model is working satisfactorily in interactive mode, the user can supply large files of inputs to test the model in batch mode. The system can generate utilization graphs to tell the programmer how much time is being spent on each module. For those who wish to look at possible performance early in the design cycle, it's possible to characterize a microprocessor and clock rate. Simulation can be run at various levels of the design hierarchy as the design requirements are refined.

Easing into the CASE world

One factor that has inhibited many organizations from using a CASE environment is CASE's top-down approach. To have an entire project in a consistent CASE metaphor has meant starting with a new project or redoing much of an existing project from scratch. Cadre has added a piece of transitional technology to Teamwork that lets organizations get a handle on existing or poorly documented source code and move their operations toward fuller utilization of CASE for future projects.

Teamwork C/Rev is a reverse-engineering tool, or as Mazzucchelli puts it, a "structure recovery tool." C/Rev scans existing source code and derives a series of structure charts that it places in the Teamwork database. Programmers can then use the structure charts as a browsing tool to examine the source code.

The structure charts are graphical representations of the source code that help engineers understand code that they might not have developed. Because these charts let users identify major components and data structures, they can help users create accurate documentation and better assess the impact of changes to the software. Thus, organizations with a welter of different source files with different levels of commentary and documentation can impose standard documentation formats based on C/Rev structure charts throughout their operations. C/Rev has an open architecture that lets programmers use their favorite editors, and

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CIRCLE NO. 31

SOFTWARE

it can be customized to work with languages other than C.

One of the joys of a CASE environment is its ability to automatically generate detailed source code from higher levels of abstraction. Of course, programmers typically want to fine-tune generated code, so to keep such fine-tuning from inadvertently stepping on the generated code, Cadre has developed a design-sensitive editor (DSE) that works with the Ada structure graph tool in Teamwork. The structure graph tool lets programmers graphically express both system architecture and Ada structural detail in a form that can feed the code generator to produce Ada source code.

Consistent Ada editing

The DSE is aware that certain parts of the total Ada program are going to be generated by the source builder from the graphical representations, and it prevents the user from changing the code that was created by the code generator. "But it allows you to add details that aren't generated by the code generator, and it keeps the work of the programmer and the code generator in synchronization," says Mazzucchelli.

Like C/Rev, the DSE can be tailored to look like someone's favorite editor, and at the end of the day, all the code is in a common place in a common format. The Ada source builder can then take the diagrams along with whatever code programmers have added by hand and create a full Ada source program that can then go to a compiler.

In general, Release 4.0 of Teamwork is designed to further support object-oriented analysis (OOA) techniques. OOA gives users the ability, but doesn't force them, to look at a problem from an object-oriented perspective in terms of how they characterize a system's requirements and functions. So there's a practical ordering of some of the notation methods people have used in the past. These include entity relationship models to help categorize objects; finite state machines to help describe an object's life cycle; and data flow diagram fragments that describe the processes (called "methods" in object-oriented terminology) that are encapsulated within an object.

"This is a different way of using data flow diagrams," says Mazzucchelli. "They appear the same, but if you look closely, you'll see that what they're describing is object communication and the processes that are contained inside objects." ■

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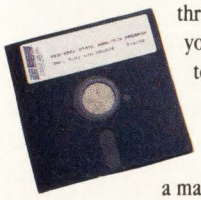

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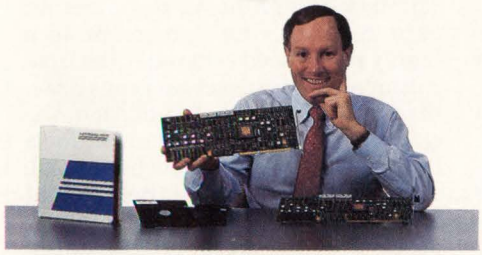

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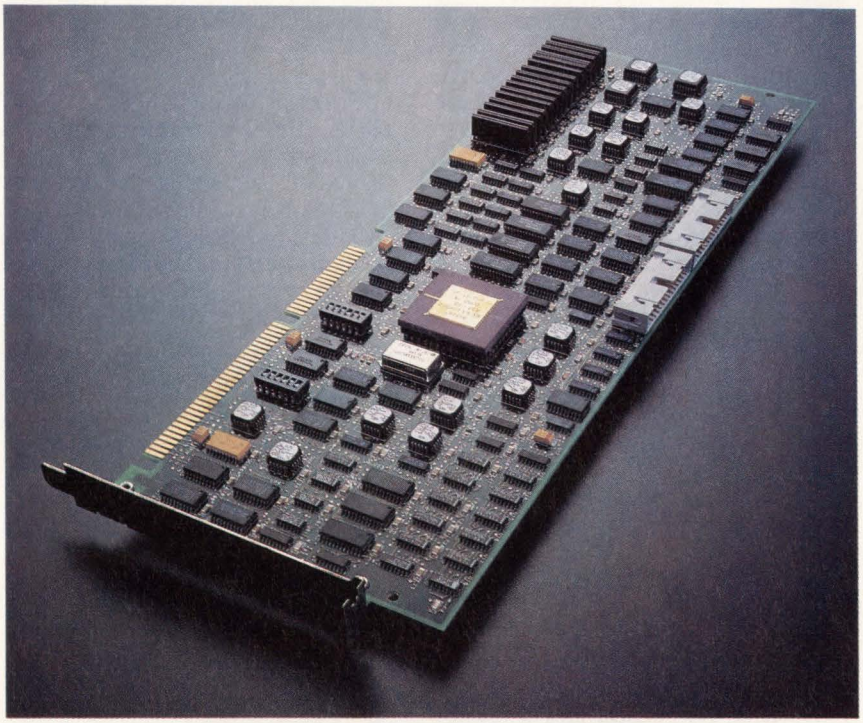

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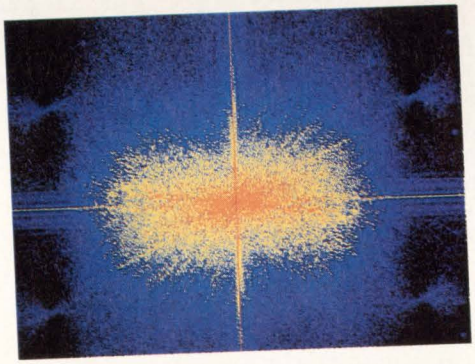

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CIRCLE NO. 33

COMPUTERS AND SUBSYSTEMS

Futurebus+ gains support from chip-development agreement

Warren Andrews, Senior Editor

A Futurebus+ parallel protocol controller optimized for cache operations is the first product to emerge as a result of a joint development effort between Texas Instruments (Dallas, TX) and Force Computers (Campbell, CA) inked late last year. This agreement is the second Futurebus+ contract to surface in the last half of 1990. The first was a second-source agreement joined between TI and Philips-Signetics (Sunnyvale, CA) in October.

Calling for the two companies to share all Futurebus+ silicon designs, the TI-Signetics agreement was a follow-up to the technology swap that gave TI rights to Signetics' Qubic BiCMOS process. According to the terms of the arrangement, TI obtained rights to Signetics' transceiver family, arbitration controller, protocol controller and data-packet FIFOs. Signetics received rights to chips that the TI-Force agreement produces.

The deal between TI and Force is the first evidence confirming the rumors that Force has had a significant Futurebus+ chip-development effort under way for some time. The agreement calls for the two companies to cooperate on the definition, design and development of a variety of Futurebus+ chips. So far, the only product mentioned is what the companies define as a PPC (parallel protocol cache-optimized controller).

"We've been talking with Force for some time, but it took a while to get everything together," says TI Futurebus+ technical marketing manager Harrison Beasley. "It's hoped that the agreement will help both companies reach the market with their respective products as much as six months earlier than if they worked independently.

"In defining the PPC," Beasley continues, "we've been able to take advantage of Force's board and system expertise, and Force has done a good job getting the design together and defining a second-level cache to snoop both the local and Futurebus+ buses. All we have to do is add our expertise and a few of the Futurebus+ macros we've developed, and we will have the most complete Futurebus+ protocol controller chip in the business."

Force vice-president of operations, Fred Rehhausser, echoes Beasley's statement on the importance of getting to market early. "We've been working on Futurebus+ product for almost a year, while most of the other board makers looking at the bus won't be starting until the end of next year," he says.

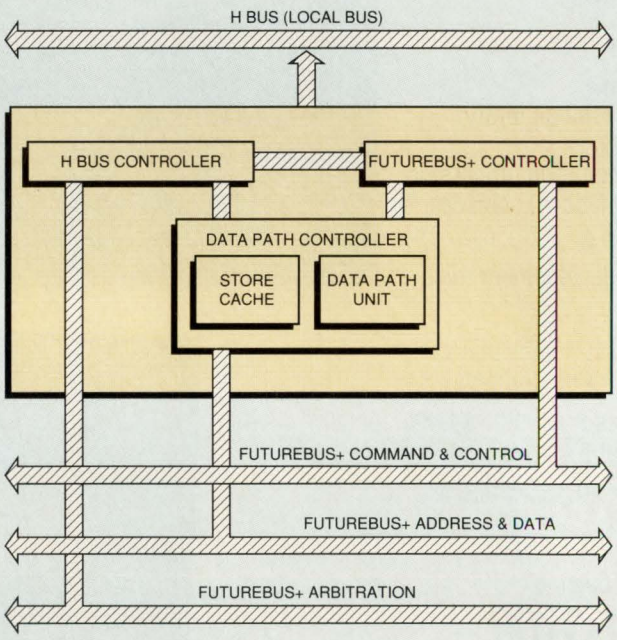
And while getting to market faster may be part of the philosophy behind the deal, there may be more to it. "The Futurebus+ specification is a complex document with many system as well as silicon implications," says Ray Alderman, technical director of the VFEA International Trade Association, which is shepherding Futurebus+ development in conjunction with the P896 working group. "It may be that truly effective Futurebus+ silicon will have to be produced by partnerships between board, silicon and system makers."

Cache optimized

The first design being put together as a result of the agreement is a highly integrated controller incorporating all 21 transaction types specified by Futurebus+. In addition, the chip provides separate control for a local bus, some level of cache control, and a data-path controller. "What makes the PPC different from any other product discussed to date," says Rehhausser, "is that it can handle both I/O and cached operations in either a compelled or packet mode.

"The Futurebus+ specification," he adds, "operates either as an I/O platform or as a system bus." These are currently defined as the difference between the B and A profiles, respectively. "When used as only an I/O bus, such as is planned by Digital Equipment Corp, Futurebus+ can be implemented without many of the transaction types specified in the 896.1 document," Rehhausser says. "But as a system bus, Futurebus+ must have all the system

TI-FORCE FUTUREBUS+ CONTROLLER



The latest Futurebus+ controller chip is a joint effort of Force Computers and Texas Instruments and is the first to be optimized for cache operations. To accommodate any of a variety of different processors, it incorporates a generic local bus, H bus, to tie the processor to cache and main memory.

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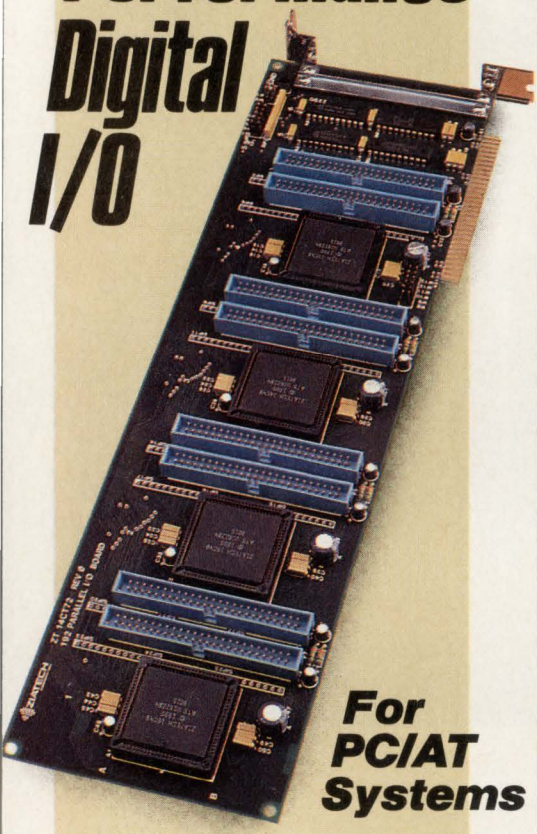

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CIRCLE NO. 35

COMPUTERS AND SUBSYSTEMS

transaction types, including those allowing for cache coherency."

As part of its cache optimization, the chip includes a "store cache" function that "provides a write buffer for write-through transactions," says Tom Tate, Force's Futurebus+ development manager. "In addition, the store cache can serve as an I/O buffer for write-backs out of main cache, or it can serve as a second-level cache if no external cache is provided. This allows the chip to accommodate a variety of cache-line sizes, as may be provided by different microprocessors." Tate adds that whether the store cache operates as a write buffer or as a second-level cache, it can significantly reduce traffic over the local bus.

Standard issues

Another unusual feature of the PPC is the H bus and H bus controller. According to Tate, the H bus is a Force-developed "generic" processor bus. "It's designed to hook up to a 68000 family processor as well as to the Intel family or any of the new-generation RISC machines now emerging," says Tate. "The bus is a multiplexed 64-bit address and data bus, and it's burst-oriented, with full cache coherency."

Besides serving as a local processor-to-memory bus, Rehhausser says, the H bus will be used, in conjunction with Force's Flexi-bus, as an I/O bus. Rehhausser is against any move to standardize on a single mezzanine bus for Futurebus+. "Futurebus+ will emerge with a number of different mezzanine buses to allow for the kind of flexibility required," he says. "Restricting the bus by establishing a single standard for mezzanine buses—such as SBus, which has been proposed—would limit both the performance and the flexibility of the bus."

Addressing the idea of a standardized local and mezzanine bus, VITA's Alderman says, "While it's possible, and been proposed, that some subset Futurebus+ be defined as an on-board local bus and SBus be defined as a 'standard' mezzanine bus, that may be too restrictive. The performance of any given board depends on the local bus, whose technology may be optimized for specific applications. Similarly, standardizing on a single mezzanine bus may also be too restrictive."

Regardless of the outcome of the mezzanine bus standard, the TI-Force chip promises to go a long way to making profile A silicon available. According to TI's Beasley, samples of the PPC should be ready by the fourth quarter.

"But the new chip won't be ready in time for the 'proof-of-concept' military boards we're making for Litton," says Rehhausser, "or for our own first commercial product. Those will be made using discrete implementations of the chip's functions."

While the TI-Force agreement isn't the first venture teaming a board maker with a semiconductor vendor, it's the first such agreement to cover Futurebus+. In addition, it may well turn out to be the most extensive in terms of the number of chips developed and in terms of chip complexity.

"It may be that truly effective Futurebus+ silicon will have to be produced by partnerships."

—Ray Alderman, VITA

Previously, Motorola's microcomputer division teamed with Plessey Semiconductor (then Ferranti) and, later, with its own semiconductor division to produce its VME interface chip. DY-4 Systems teamed up with Newbridge Microsystems in development of its VME64 AVICS chip, and the VITA Chip Consortium joined with VTC to develop and manufacture the VIC and VAC chips. But in all these cases, the product development has turned out to be limited to a basic chip. ■

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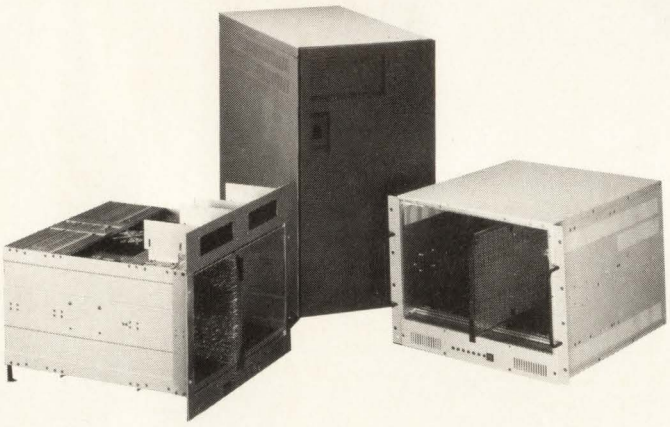

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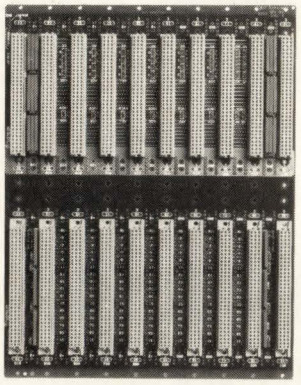

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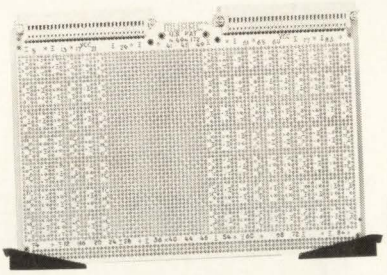

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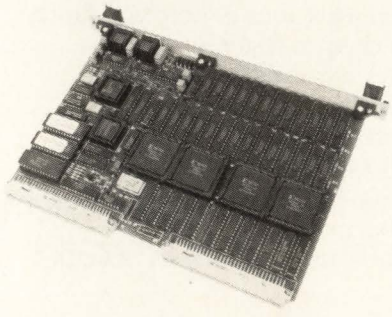

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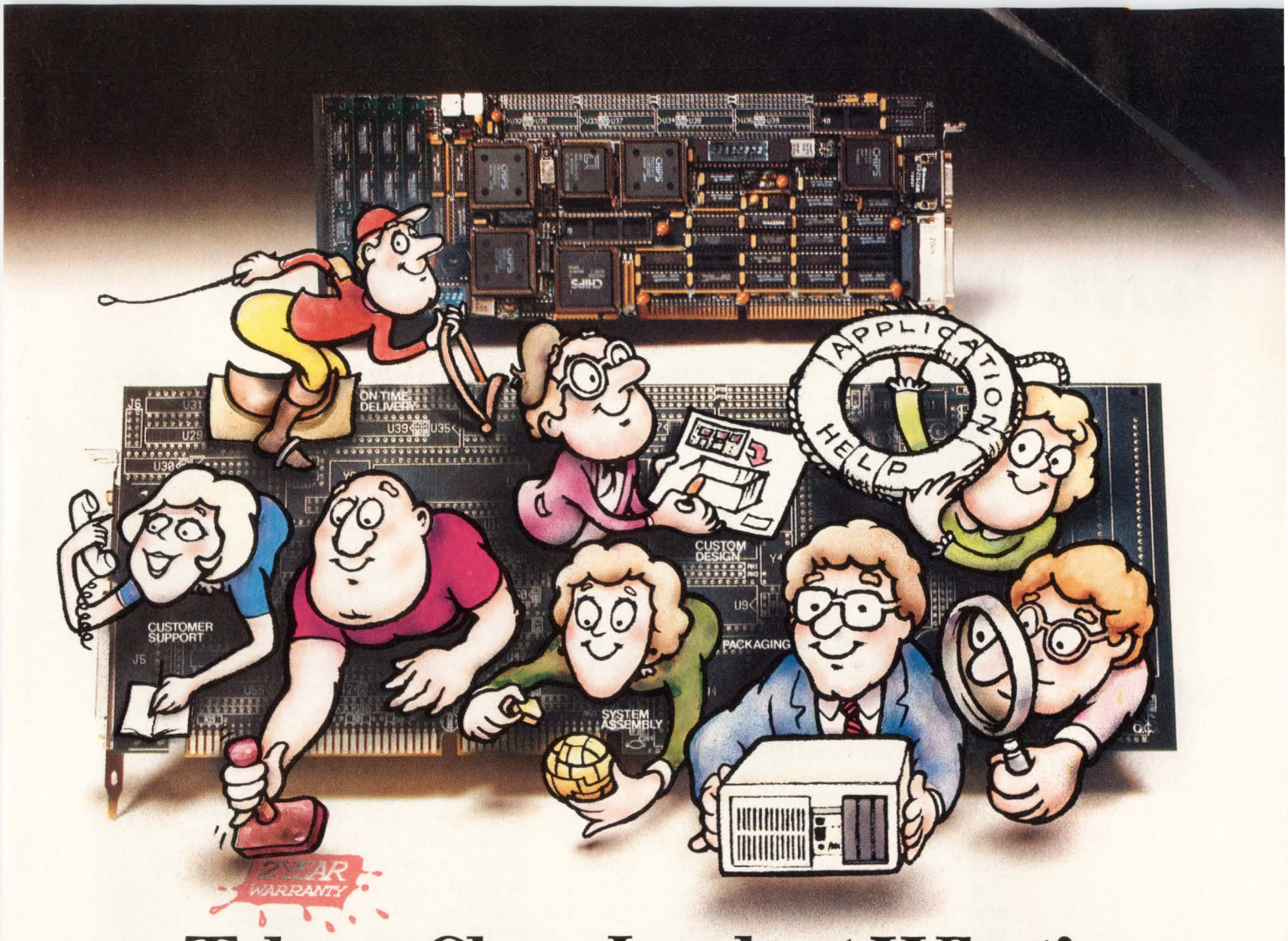

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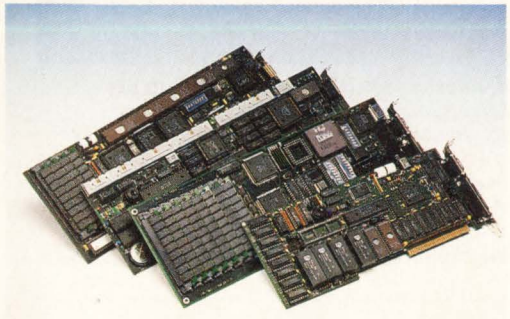

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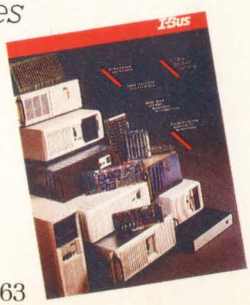

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CIRCLE NO. 13

IC, storage & display technologies have turned the world digital

Semiconductors are the primary technology driver of the digital revolution that began roughly 30 years ago. Densely packed ICs—the microminiaturization of transistors—have fueled revolutions in virtually all electronics applications. And the dominance of IC technology has had a profound impact not only on the circuits that engineers build but on the way engineers think. No longer a matter of measuring and controlling voltages and currents, electronics is now a matter of manipulating 1s and 0s.

There are at least two other technology drivers of the digital revolution—data storage and display technologies.

Data storage has allowed efficient access to ever-larger volumes of information, held in a form that permits manipulation or communication by digital means.

Display technologies provide the critical link between digital data and human perception. Advances in displays have made a host of products, including digital clocks, precision instruments, calculators and personal computers, a reality.

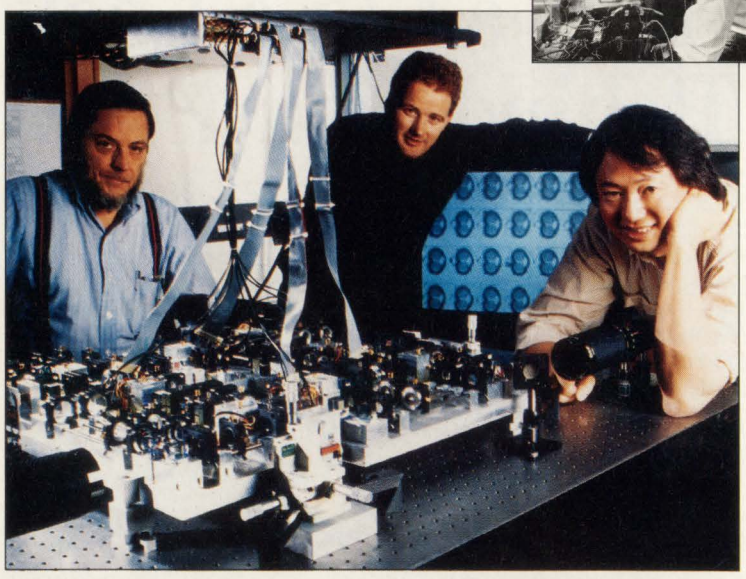
The impact of microprocessors and memories, however, is the one element in the digital revolution about which all technologists can agree. The pace of change has been dazzling. In just 10 years, from 1970 to 1980, single-chip microprocessors went from 4 bits (with 2,300 transistors on the Intel 4004) to 32 bits (with 68,000 transistors on the aptly named Motorola part).

In just 15 years, from 1971 to 1986, the capacity of commercial single-chip DRAMs leaped from 1 kbit for the Intel 1103 to 4 Mbits.

Moore's law, which states that the degree of IC complexity (in terms of the number of transistors per chip) will double every two years, has proved as true today as when it was first stated in 1970.

But there are some technologists who believe that this growth process will approach its limits in the late '90s. Manufacturing the 64-Mbit DRAM will require a semiconductor process that achieves line widths of only 0.25 µm, a level some believe represents a practical limit. The cost of developing the following generation, a 0.15-µm manufacturing line width, will be prohibitive—even for the industrial giants. At that point, futurists say, we'll have to live with what we've got.

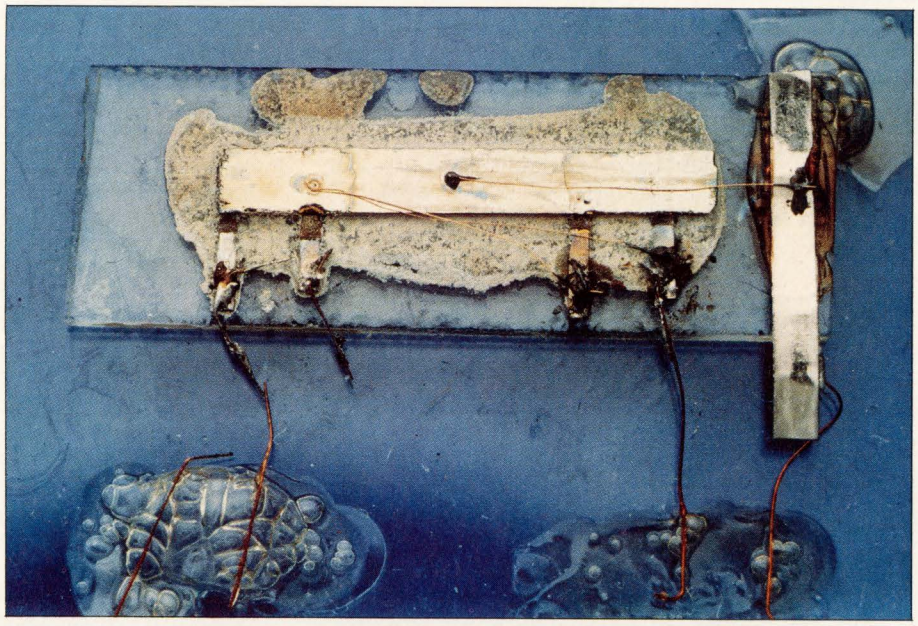
Experts at AT&T's Bell Laboratories in Holmdel, NJ suggest that the late '90s and early years of the 21st century will witness the displacement of ICs by other types of devices—particularly photonic



The digital optical processor photographed with these Bell Lab researchers in 1990 uses S-SEEDs (symmetric self-electro-optic effect devices) as its logic elements. Developed by Bell Labs, S-SEEDs may be the equivalent of TI's Series 51 logic ICs—the foundation for a new method of building Boolean circuits. The information accompanying Bell Labs' 1948 photo (top) of the inventors of the transistor stated that the transistor's "potentialities are such that Bell scientists and engineers expect it may have far-reaching significance in the field of electronics and electrical communication."

circuits.

The S-SEEDs (symmetrical self-electro-optic effect devices) developed by Bell Labs can function like logic gates or memories, propagating light pulses with input to output delays measured in picoseconds. Each of the S-SEEDs can be used as a two-input NOR gate (with two inputs and one output), and provides switching times on the order of 33 ps. A 64×32-bit S-SEED array has the equivalent of 6,144 logic connections and can control 16,384 separate light beams. Some technologists believe these photonic logic blocks may be the equivalent of Texas Instruments' Series 51 logic ICs—the foundation for a new method of building Boolean circuits.



The first IC, developed in 1958 by TI's Jack Kilby, was a phase-shift oscillator, consisting of a single mesa transistor and a p-n junction capacitor on a p-type germanium substrate (the bulk resistance of the germanium was used for resistors).

The developer of the S-SEED, David Miller, isn't convinced that S-SEEDs will replace digital semiconductors, or that they will become the CPUs of tomorrow's optical computers. He likens the S-SEED to a two-input multiplexer rather than a NOR gate: it's good for controlling inputs and outputs along a dense matrix; it wasn't developed for combinational logic functions. However, the ultrahigh density of interconnects provided by an optical matrix means that computer I/O signals don't have to be grouped as 8-, 16- or 32-bit data words. Unlike signals travelling over buses and backplanes, optical signals don't have to deal with the capacitance or line impedance of metallic interconnections. Ultimately, suggests Miller, this could dramatically alter the structure of future computers.

Busicom's engineers asked Intel to design a custom chip for this calculator. Intel's response was the 4004, the first single-chip microprocessor. Later, Intel purchased the rights to the microprocessor and, in 1971, marketed the 4004 as a standard product.

Any technologist looking at the history of the electronics industry over the past 30 years is bound to be amazed and confused by the overlap between analog and digital technology. Such early IBM computers as the 1948 Selective Sequence Electronic Calculator, for example, ran on vacuum tubes (12,500 of them). The vacuum tubes amplified currents that energized relay coils. It was the relays (21,400 of them) that would record and manipulate (add, multiply or divide) the digits.

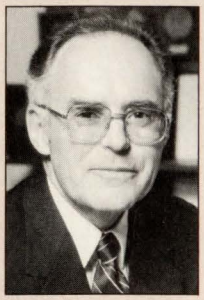
The first transistor publicly demonstrated by Bell Telephone Laboratories, then in New York City, on June 30, 1948, was identified as "a practical solid-state amplifier." Bell's research into solid-state physics was an outgrowth of early research on the thermionic emissions of vacuum tubes. Both Walter Brattain and William Shockley were trained in solid-state physics, and in their experiments, they attempted without much success to attach a control grid—like the regulating grid of a vacuum tube—to a copper-oxide rectifier.

It was Russell Ohl, a chemist at Bell Labs, who introduced silicon—a little-known material at the time—into the equation. Ohl had used silicon as cat's whisker radio detectors (a type of rectifier), and had already learned to distinguish between n- and p-type conductors. Much of this early research was completed by 1940 but was interrupted by World War II. It was in December 1947 that the Bell researchers created a working transistor.

The first users of transistor technology were military customers who needed the miniaturization and weren't constrained by price. Early transistor makers such as Raytheon, General Electric, Sylvania and RCA found ready customers for their products. By 1952, these companies held over $5 million in military contracts, and were each delivering over 5,000 units a week.

At first, electronic system manufacturers used the devices as analog signal amplifiers. But the dramatic improvement in transistor switching speeds—100 ps was obtained in a GE laboratory—meant that transistors would be used as more than just amplifiers. Once the electronics world learned to formulate its conditions as a sequence of on-off states, the full transition to digital technology could begin.

"We'll sell you a gate for $1.00"



Gordon Moore, chairman, Intel

Thanks to semiconductor technology, electronics has been the only industry in which the functionality and performance of its products continue to go up while the costs go down. But it hasn't always been that way, says Gordon Moore, whose companies have maintained leadership positions along this trend line.

Together with Robert Noyce, Moore cofounded Intel, which brought the first microprocessors and DRAMs to market 20 years ago. While Intel's 1103 1-kbit DRAM ushered in the LSI era, and the microprocessor has become the essential building block of practically all electronic products, Moore and Noyce spent over 10 years—from the founding of Fairchild in 1957 to the founding of Intel in 1968—selling ICs to reluctant customers.

"IC technology wasn't an instant success," says this Berkeley-trained chemist, who was manager of Fairchild's engineering department when some of the first ICs (the Micrologic series) were developed in the late '50s and early '60s. During the '60s, the primary users of ICs were manufacturers of military computers who needed the small size and who weren't sensitive to costs. Even then, Moore describes the rejection ("we can't use them!") he experienced trying to sell an IC with 12 flip-flops to users accustomed to building their own circuits with discrete components. "You can't measure the beta of the transistors, you can't measure the resistors," his potential customers told him. "How can you predict the reliability?"

"It was Noyce," Moore says, "who really got the market going—he said, 'We'll sell you a gate for $1.00.'" ($1.00 was then a recklessly low price.) It was at this price point, Moore says, that it became more economical to buy ICs than to build circuits with discrete parts.

By the time Moore and Noyce left Fairchild to start Intel in 1968, the technology had advanced well enough to build large circuits. Moore says, the problem with very large circuits was that they would usually have less appeal to broad market segments. The larger they got, the more specialized they would seem. Intel's philosophy, Moore suggests was to design and manufacture large ICs for broad market appeal. "The circuits should be complex," says Moore, "but their design and manufacture should allow for large volume."

One implementation of the Intel philosophy was in the design of the 4004—the first commercial microprocessor. Rather than designing a dedicated calculator, Intel designers Todd Hoff and Federico Faggin developed a general-purpose 4-bit computer. Its ROM-based microcode dictated whether it behaved like a calculator, an elevator controller, a traffic-light controller, a computer game, or anything else. The same reprogrammability was harnessed to successive generations of Intel processors.

Much honored with IEEE, university and professional society awards, Moore hesitates (only slightly) before making predictions about the future: "10 years ago you wouldn't have predicted the overwhelming success of the PC. Looking back on things, you really get humble."

Having said that, the past president of the Semiconductor Industries Association says that silicon IC technology will remain the workhorse of electronics well through the next decade. He sees manufacturing line widths going down to the 0.5-μm level. "That's still a lot of work," he says, "but things are in place to do that." There is a possibility of building circuits with 0.25-μm geometries, says Moore, but "only if we can do that optically. To me, the big discontinuity is where we abandon optical lithography." It's possible, suggests Moore, to build circuits (as IBM is attempting to do) with x-ray lithography. "If we do, it'll really jack up the cost." A transition to x-ray technology would reverse the trend toward greater functionality at lower costs that the electronics industry has enjoyed over the past 30 years. "Optical will be with us well past the year 2000," quips Moore, "and that's well past MY retirement!"

Like everyone else in the semiconductor industry, the Intel chairman is reflective about the high cost of advancing the technology year after year. Currently, the company turns over $1 billion—a major portion of its annual revenues—back into R&D and capital spending. With these numbers, Moore is no longer optimistic about the possibilities for small companies to succeed in the semiconductor business. It may be practical for ASIC "design centers," for example, to use the fabrication facilities of the bigger companies but only as long as excess fabrication capacity exists.

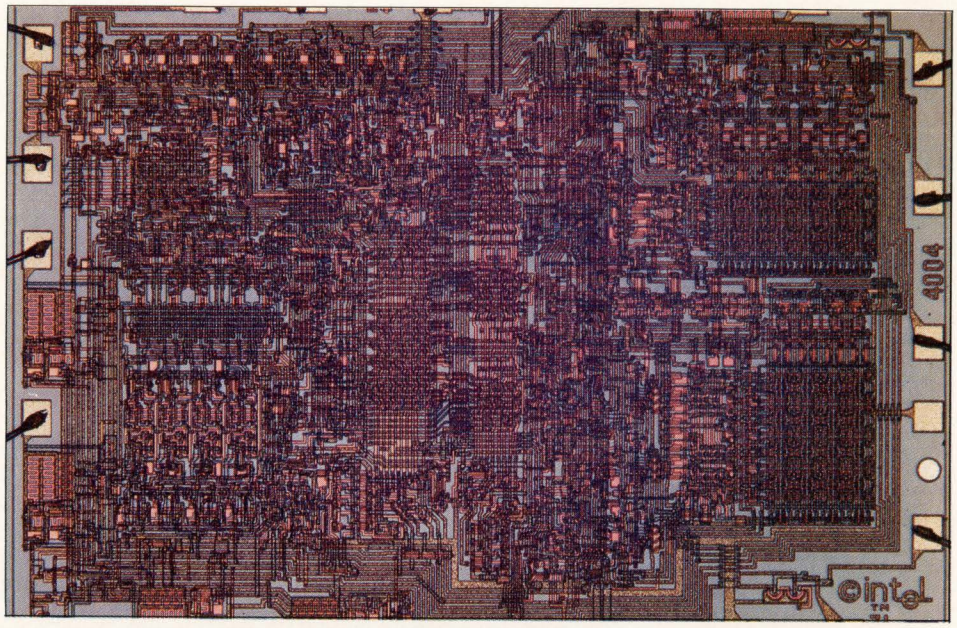
Semiconductor manufacturers will increasingly have hard choices to make about where and how to compete. Moore regards Intel's withdrawal from the DRAM market back in 1985 as particularly painful. The company had developed and marketed the industry's first single-chip DRAM, the 1-kbit 1103, in 1970. By the time 4-kbit DRAMs were marketed, Intel's design was using a four-transistor bit cell, compared to the more efficient one-transistor bit cell marketed by Mostek. In the boom period from 1979 to 1980, Intel was under pressure to ship both DRAMs and EPROMs, but didn't have capacity for both. Its position was stronger in EPROMs. By 1985, the company had produced a manufacturable 1-Mbit DRAM design, but was looking at an additional $400 million investment to get it into production—an investment, Moore suggests, that may not have been recouped in this fiercely competitive market. Fortunately, any regrets over the company's retreat from DRAMs have been erased by the overwhelming success of the 80386 32-bit microprocessor, also introduced in 1985.

Today, the cost of capital remains a limiting factor for the advancement of semiconductor technology. Moore says that Intel in the late '60s and early '70s was able to develop not one but two new technologies on a $3 million investment (Schottky-barrier bipolar ICs and silicon-gate MOS). Today, the investment in a small manufacturing facility for an existing technology is more than 100 times that. A 0.8-μm fab, Moore estimates, will cost about $400 million today.

This doesn't mean that companies such as Intel will give up pushing microprocessor technology to its limits. Just by extrapolating the current trends, Moore foresees the possibility (if not the probability) of 100 million transistors on a single chip. "Figuring out what to do with it will be the real challenge," he says. "With 100 million transistors you can build every circuit that's ever been built today on one piece of silicon."

TI began as a Dallas-based manufacturer of instruments for the oil well drilling industry. Like other companies, TI licensed the transistor manufacturing technology from Bell in 1952 and set up its own transistor laboratory under Gordon Teal. TI was the first to produce all-silicon transistors (replacing germanium), using a grown junction technique in 1954.

By the late '50s, many types of transistor structures (for instance, mesa and planar) were fabricated with many transistors on a single wafer. Manufacturers made transistors by scoring the wafer, separating the devices, attaching electrical leads, and packaging them. It seems surprising today that no one thought of simply connecting the transistors together on their unscored wafer. But the IC didn't surface until 1958.



The first microprocessor, Intel's 4004, was introduced in 1971. The 4-bit processor comprised 2,300 transistors and operated at 0.06 Mips. It could address 640 bytes of memory.

Though Jack S. Kilby was later awarded a National Science Medal by then-President Richard Nixon in 1970, the inventor of the IC and the hand-held calculator remains modest about his achievements (see "The inventor of the IC looks back on 30 years of progress," p 56). As an engineer with the Centralab Division of Globe-Union, Kilby attended AT&T's 1952 seminars on the transistor in Milwaukee, WI. After using transistors to build hearing aids for Centralab, Kilby went to work for TI in Dallas in May 1958. He was assigned to the micromodule program TI was conducting for the Signal Corps, and his first circuits were flip-flops built with discrete components.

The first IC, like the first transistor, was an analog device—in this case a sine-wave generator. It was a phase-shift oscillator, consisting of several germanium mesa transistors on a 7/16-in. sliver, diffused resistors and capacitors all on the same substrate, but interconnected by hand with gold wire. Kilby's notebook would record the impracticality of interconnecting miniature transistors with hand soldering methods.

Robert Noyce, who went on to found Santa Clara, CA-based Intel in 1968, was doing similar work on ICs at Fairchild Camera and Instrument in 1959. Noyce had worked with diffused resistors, but he was exploring the possibility of forming interconnections by evaporating metal lines onto a surface oxide layer. Fairchild would provide the first commercial ICs in 1961, just months ahead of TI. Part of the Micrologic family, the Fairchild chips contained four bipolar transistors and two resistors. Fairchild's method of data registration would become known as resistor-transistor logic. TI followed Fairchild into the marketplace with its own Series 51 Solid Circuits.

The experimentation with ICs that followed in the next decade reflected an ambivalence about these new devices and what they were supposed to do. Many developers of ICs were thinking of analog circuit applications, and cursing under their breath that the integration of transistors and resistors on one piece of silicon was a compromise for the sake of miniaturization; that this integration wouldn't allow the precise selection of components and the control of voltages, currents and frequencies that was possible with the use of discrete components. The digital revolution didn't gain steam until Kilby invented the hand-held calculator. His calculator project was started in September of 1965.

It wasn't until the development of MOS, however, that IC designers finally gave up on simply controlling voltages and currents. MOS, p-channel, n-channel and especially CMOS allow relatively "sloppy" transistors to function as high-speed switches. As kit parts, these transistor switches will "slam on" and "slam off," producing ringing and ground bounce, but they do it fast, predictably and with little power consumption.

Circuits built in 1963 by RCA's Solid State Division in Somerville, NJ used MOS and earned several basic patents for the company. In 1964, RCA fabricated an IC with what it called "complementary-symmetry MOS," or COS/MOS. These ICs required less power than bipolar circuits, though they were slower. It wasn't until 1967 that RCA actually used this technology to build a user circuit—a part for NASA's Apollo program. In 1968, RCA introduced the first standard CMOS logic family, the CD4000 series. These low-power ICs were especially useful for the cal-

culators and watches that were proliferating rapidly then. Today CMOS represents 40 percent of the global IC market.

From the mid-'60s, desktop calculators began to create a demand for low-power semiconductors in large volumes, and many companies struggled to satisfy this demand for ICs. Regis McKenna, the marketing guru credited with putting many companies and perhaps Silicon Valley itself on the map, saw the development of MOS circuits at General MicroElectronics (GME).

McKenna, now chairman of Regis McKenna Corp of Palo Alto, CA, remembers the four who founded GME: Howard Bobb (who went on to found American Microsystems), Phil Furguson (who gained expertise at TI and Fairchild), Earl Gregory and Colonel Lower. These people developed, McKenna says, the first MOS shift registers and the first MOS analog-to-digital converter. Some 29 MOS chips were built in 1963 and 1964 for Victor Comptometer. These included a binary coded decimal to binary converter, a dual 20-bit shift register, a dual four-input gate and a dual J-K flip-flop. The Victor 3900, the first completely MOS calculator, was introduced in 1965.

"MOS technology was immature and unstable," says McKenna, "but we saw the potential." He suggests that the technology went into the making of the first 1-kbit DRAM—the Intel 1103. It's widely conceded that this part, introduced in 1970, ushered in the LSI era.

Kilby's project to design a hand-held calculator using IC technology began in September of 1965. The ICs developed for the project integrated the equivalent of 6,000 transistors. The biggest problem, however, proved to be the packaging for the new circuits. Up to that point most TI circuits had 14 or 16 leads.

Apart from calculators, the development of semiconductors in the '60s was financed by military and government needs. The Defense Department's Minuteman project and NASA's Apollo program were the biggest drivers, and through these programs, the government became one of the first customers to emphasize reliability in the semiconductor industry. The Apollo space program, however, was one the last of the big government-financed programs to drive the semiconductor industry.

There was a shift in the late '60s and early '70s away from military circuits into commercial applications of digital electronics. The first big commercial customers for ICs were

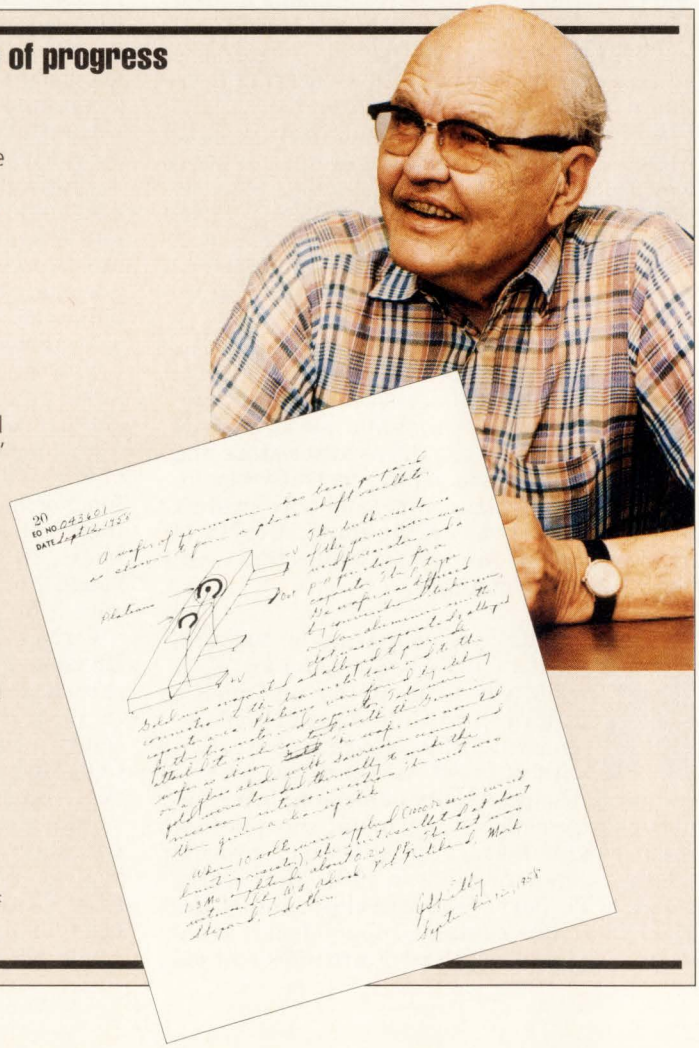
The inventor of the IC looks back on 30 years of progress

I don't have a lot of faith in future projections for the semiconductor industry," says Jack Kilby, who demonstrated the first IC at Texas Instruments back in September 1958. "If anyone would have a attempted to predict the course of the electronics industry when the first IC appeared 30 years ago, they would've missed it by a wide mile."

The first demonstration circuits were analog, although the first commercial products—the TI Series 51 devices—were digital logic gates. "There was a natural marriage between digital and IC technology," says Kilby, although the circuits he devised were intended to demonstrate capability in both analog and digital circuit processing. "It would be hard to tell where we would be today if analog circuits were all we had."

The original Series 51 chips, which came to market in 1961, consisted of approximately six gates and flip-flops. In spite of the levels of integration that the company was able to obtain, Kilby suggests, it took a good 10 years for ICs to be accepted.

Most fascinating to the man who led TI design teams developing single-chip calculators in the early '70s is the decreasing cost of circuit functions that IC technology has enabled. "The decrease in the cost per function has been much greater than that which could have predicted 30 years ago," Kilby says. The increase in device complexity—over six orders of magnitude—has had an incredible impact on all things electronic. It makes the electronics industry the only one in the world in which the cost per function perpetually decreases. However, the inventor of the IC remains modest about his own role in this: "This cost decrease isn't a consequence of any individual or company—it's an achievement of tens of thousands of engineers around the world."



computer makers. Machine tool manufacturers such as Honeywell and Cincinnati Millacron were quick to utilize IC controllers, but it was memory ICs such as Intel's 1103 that pushed open the doors of commercial computer makers.

Many observers believe 1970 was a major transitional year for the semiconductor industry. Not only does it mark the point when semiconductor manufacturers started turning away from military applications and toward more commercial ventures, but it marks the point at which major systems houses began purchasing semiconductors from outside vendors rather than relying on their own internal design and production.

Prior to 1970, suggests LSI Logic's technical marketing vice-president Rob Walker, many of the major systems houses—IBM, Control Data, AT&T and Sperry Univac—produced in-house semiconductors.

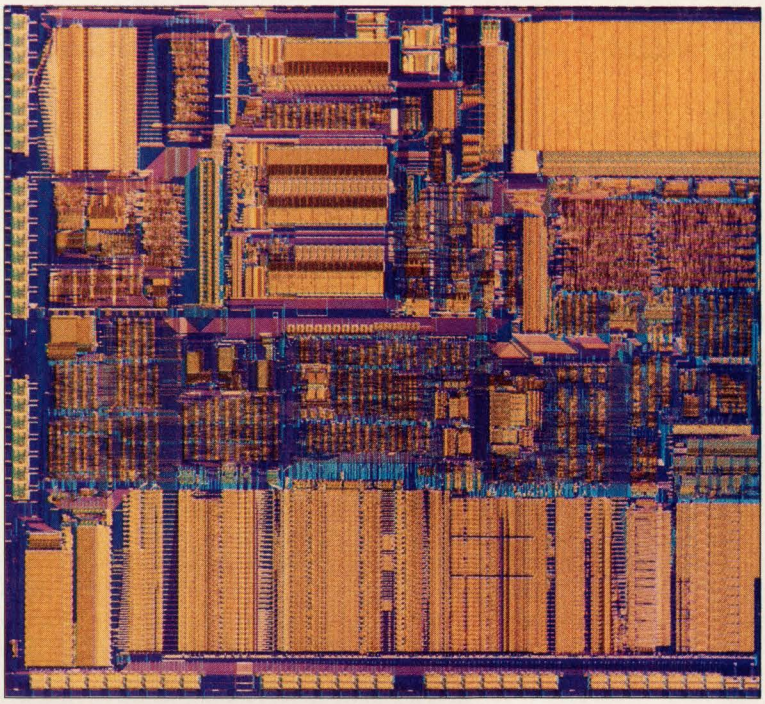
What was eventually marketed as the first single-chip microprocessor, the 4004, actually began life as a custom product developed by Intel for Busicom, a Japanese calculator manufacturer.

Following the success of the TI's little machine, hand-held calculators seemed to do well on the market. While semiconductor manufacturers would try to satisfy their customers with standardized products, the calculator manufacturers of the early '70s were demanding customized chips as a means of differentiating their products. IC manufacturers reacted by partitioning the logic of the calculator in ways that could generate standardized building blocks.

Intel was incorporated in July 1968 by Gordon Moore and Robert Noyce, who left Fairchild to set up a company dedicated to the economical manufacture of large-scale circuits (see "We'll sell you a gate for $1.00," p 54). Intel was asked to design a chip set for Busicom in August 1969. Marcian (Ted) Hoff, then Intel's applications manager, is credited with the inspiration for the calculator's architecture.

The Busicom calculator differed from others in that it used ROM-based program memory. The architecture of the chip, the 4004, designed for the Busicom machine resembled a general-purpose computer that was programmed to be a calculator. The 4004, designed by Stan Mazor and Federico Faggin, was a 4-bit microprocessor: it could take in only four digits (bits) at a time. There was no software. But it was supported with a 32-bit on-chip RAM, a 256-byte ROM and a 10-bit shift register and output expander. It could address up to 16 256-byte ROMs (4,096 bytes) and 16 RAMs (4,120 bits). With an instruction execution rate of 60,000 instructions per second, it had the same computing power as the early Eniac machine.

When the Busicom company closed, one of its top designers, Masatoshi Shima, joined Intel. In 1971, Noyce decided to buy back the rights to the chip. The first microprocessor was then advertised for sale in the fall of 1971.



In 1985 this 4004 descendant, Intel's 80386, featured 32-bit processing at up to 8 Mips, the ability to address 4 Gbytes of physical memory and 64 Tbytes of virtual memory (enough for an eight-page history of every person on earth). The chip included 275,000 transistors.

Intel followed up quickly, in April 1972, with the first 8-bit microprocessor, the 8008. It was an expansion of the 4004, incorporating a larger 8-bit register stack. It addressed up to 16 kbytes, and directly interfaced with standard memory ICs such as 1101 RAMs and 1601 and 1701 ROMs.

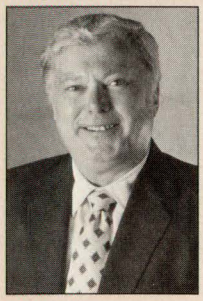
By 1973, the early potential of microprocessors had been generally recognized by the electronics industry. The year 1974 saw the emergence of several different microprocessor designs.

The first processor to be used in personal computers was Intel's 8080, introduced in April 1974. An improved version of the 8008, the 8080 had 10 times the throughput of the first generation. The new chip was designed by Shima, who later joined Zilog to build the Z80 processor.

The first CMOS microprocessor, the 1802, was introduced by RCA in 1974. Also introduced that year was the popular 4-bit microcontroller, the TI TMS1000, and one of the most adventurous designs, the Motorola 6800. Unlike the Intel-designed microprocessors, which multiplexed address and data lines, the Motorola products segregated address and data lines.

The 16-bit 8086 was introduced in June 1978. It was followed in rapid succession by other 16-bit parts such as Zilog's Z8000, Motorola's 68000 (1979) and National's 16000 (1981). Many of these early parts were structured to handle larger data words than their external address buses could handle. Both

High-density disks advance along a path set in the 50's



Alan Shugart, chairman, Seagate Technology

Current developments in magnetic storage technology aren't so different from the high-density storage of the late 1950s and early '60s, says Alan Shugart, founder and chairman of Seagate Technology. Born in 1979, Seagate brought the original 5-Mbyte ST-506 drives to market in the early '80s. The company is often credited with the commercialization of the 5¼-in. form factor. Shugart, who left IBM to found Shugart Associates in January 1973, sees the hard disk drives currently manufactured by Seagate and its competitors as using the same technology as the Winchester disk developed by IBM in the mid-'60s.

Shugart, who was RAM technical program manager at IBM's San Jose, CA facility during the '60s, cites Bill Goddard's earlier pioneering work on the RAMAC (1955). The RAMAC (random access method of accounting) actually introduced the concept of random access to data storage. The RAMAC was the first storage device to use an air bearing as a method of maintaining a gap between the read-write head and the magnetic surface of a disk. It was a refrigerator-sized unit that stored approximately 5 Mbytes with 1,000 bits/sq. in.

The early RAMAC used externally pumped air pressure to keep the heads afloat. In 1957, researchers at the IBM labs in San Jose—Ken Haughton, Al Osterlund, Russ Brunner and Bill Michaels—developed slider bearings that would keep the read-write head afloat without externally pumped air. Their IEEE paper on the subject—which Shugart regards as "the bible"—described how this air bearing could provide closer spacing between head and disk, which would provide higher bit densities and faster access times.

Winchester technology, a development of the mid-'60s, used multiple low-mass lightly loaded read-write heads on lubricated disk surfaces. Haughton and Don Johnson developed the basic technology, which is still in use today. Though the technology had little to do with personal computers, according to Shugart, it nonetheless paved the way for smaller form factors. Everything we understand today about high-density disk drives—thin-film heads, for example, or thin-film disks—is a logical extension of the IBM 3030 drives (the Winchesters) of the mid-'60s.

The technology's advances in bit and track densities never cease to amaze Shugart. He especially remembers the Merlin drive developed by Jim Patterson in the late '60s: "I didn't think we'd ever get beyond the 100 tracks/in. we were doing with the Merlin 3330. Now we're getting close to 2,000 tracks/in."

In the future, says Shugart, we'll see bit densities increase by Negative Pressure Sliders, whose air bearing are designed to force the read-write head downward toward the disk surface (rather than upward). One effect of this would be constant bit spacings across the surface of a disk—tighter spacings on the outer edges of the disk where velocity of the spinning disk is higher; wider spacings on the inner tracks of the disk where the velocity is lower.

Shugart remains sceptical that magnetic storage could be replaced by other technologies: "I've heard this for 35 years, but magnetic recording densities keep on growing—I don't see a stop."

the 68000 and the 16000, for example, had 32-bit internal architectures but only 16-bit data buses. This meant that two 16-bit data words would be placed side by side inside the microprocessor before an instruction would be executed. This provided some of the power of a 32-bit CPU, but with a more economical data bus structure.

The 8088 had a 16-bit internal architecture, but a multiplexed 8-bit address and data bus. The 8-bit I/O structure made the device initially very economical to use (much of the 8-bit software developed for the 8080 and its Zilog clone, the Z80, could be ported over rapidly). IBM eventually adopted the 8088 for its first personal computer, introduced in August 1981.

While the Motorola 68000 was billed as a 32-bit processor, the first full 32-bit processor—Intel's 432—appeared in 1981, less than a decade after the introduction of the 4-bit machine. Though many believed it was ahead of its time, the 432 was poorly received. Motorola's full 32-bit processor, the 68020, would appear in 1984.

With the full 32-bit processors, semiconductor vendors could hold up a chip that would rival minicomputers in performance. Hailed by their makers as "mainframes" on a chip, the 32-bit processors—particularly the Motorola 68000—became the foundation of the Unix workstations of Apollo, Sun Microsystems, Hewlett-Packard and others.

The rapid proliferation of 32-bit processors, however, put semiconductor vendors under pressure to distinguish their products from one another. While these devices offered many possibilities for computer CPUs and controls, designing them into products, getting them to work properly and tweaking their performance was an agonizing process. Generally, the semiconductor vendors resorted to one of two means of distinguishing their products: One method was to promote easy-to-use software programming tools; the other was to tout the program execution speed of the processor.

It was in this environment that RISC—a concept developed to build faster computers—became a buzzword for the '80s.

The use of RISC processors in workstations is now challenging the five-year dominance of Motorola's 68000 series CPUs and may yet challenge the dominance of Intel's 8086 series CPUs in personal computers.

The RISC processor revolution, however, wasn't an invention of the semiconductor manufacturers. The father of RISC is Sey-

mour Cray, who embodied what's now called RISC into the vector-processing machines he built for CDC in the late '60s.

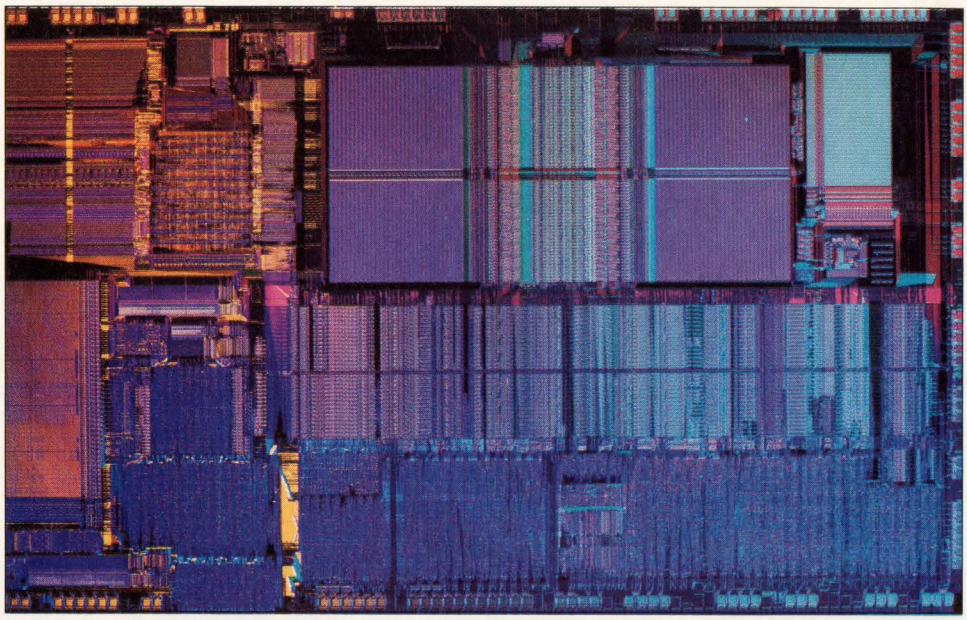
The common interpretation of RISC maintains that short, hard-wired instructions are easier to implement. Thus, RISC programs can be executed quicker than CISC programs, which rely on ROM-based microcoded instructions and require instruction decode hardware—an additional layer of complexity. This interpretation, though, doesn't communicate the true advantage of RISC machines.

RISC gets its performance improvement from a reduction in certain kinds of instructions—particularly memory-fetch operations. Cray believed that memory-fetch operations—the process of generating a memory address, fetching an instruction from that address location, generating another address, fetching a data word, and so on—was extremely costly in terms of clock cycles. In adding a long column of numbers, more than three-quarters of the processing power could go to memory addressing and fetching. Cray's method, with the CDC-Cyber 206 machines and his own Cray-1, was to avoid main memory accesses and keep instructions and data close to the CPU in a register chain. Current RISC processors emulate this philosophy with caching techniques.

The success of RISC, unlike other major developments in the electronics industry, hasn't been as dependent on big-company sponsorship. While John Cocke began a RISC project at IBM's Thomas J. Watson Research Center in 1975, and both HP and DEC maintained RISC development efforts in the early '80s, it was start-ups such as MIPS Computer Systems in Sunnyvale, CA and Sun Microsystems in Mountain View, CA that brought the first RISC processors to market in the mid-'80s.

Much of the thought processes for turning room-sized computers, like the Cray-1, into ICs for microcomputer building blocks was perfected at the University of California at Berkeley by David Patterson and by John Hennessy at Stanford University. MIPS Computer Systems was started, in fact, to manufacture the chip that students experimentally constructed at Stanford.

What the industry seemed to gain with microprocessors in the mid-'80s, though, it seemed to give up in semiconductor memories. Many U.S. manufacturers gave up the quest for higher-density DRAM memories, citing severe price pressure from Japanese manufacturers—NEC, Hitachi and Toshiba—as well as the high investment cost required to develop and manufacture successive generations.



The latest descendant of the 4004, Intel's 80486, has the same memory capacities as the 80386 but operates at up to 27 Mips. At 50 times the performance of the 8088 processor in the original IBM PC, the 80486 can scan the Encyclopaedia Britannica in 2 seconds.

It's clear that developing the manufacturing processes for 4-, 16- and 64-Mbit DRAMs requires a capital investment well beyond the capabilities of all but the largest electronics firms.

The reign of digital semiconductors will likely wind up as it began—under the umbrella of large companies. At the International Solid State Circuits Conference in February 1990, it was IBM that announced it had fabricated a 16-Mbit DRAM at its semiconductor facility in Essex Junction, VT.

But even the size of an IBM won't be enough to get us to the next generation: the 64-Mbit DRAM will be jointly developed by IBM and Siemens AG. X-ray lithography has been chosen as the means of etching the circuit lines onto the surface of the silicon. Because X-rays have extremely short wavelengths, they can be used to etch the submicron geometries on a wafer. X-ray lithography could be used even for 256-Mbit DRAMs—if that generation comes about. The National Synchrotron Light Source at the Brookhaven National Laboratory in Upton, NY will provide the X-ray lithographic equipment, possibly with funding from Sematech. Part of IBM's X-ray mask lithography research is also being funded by a $17.4 million DARPA contract.

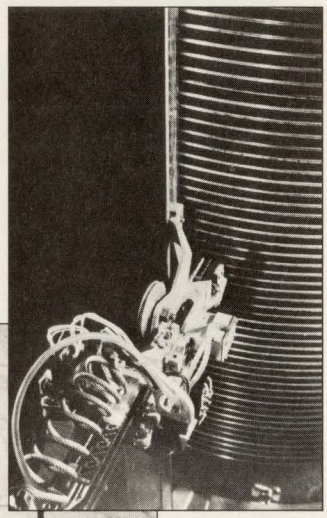
Though semiconductor development began at AT&T's Bell Labs, and was commercialized by other adventurous companies, practically everything we now understand and accept in the area of data storage can be traced to the laboratories of IBM's research center in San Jose, CA, which holds hundreds of patents

and awards on this technology.

The first hard disk storage unit was the RAMAC 350, which used the random access method of accounting. The RAMAC 350 stored 5 Mbytes of data on 50 24-in. platters when it was introduced September 4, 1956.

Many industry observers feel that the introduction of this device made a profound change not just in the method of data storage but on our conceptions of computing. Rey Johnson, the IBM engineer who drove the development of the RAMAC, was one of the first to receive a National Technology Medal, from then-President Eisenhower, as well as an award from the American Society of Mechanical Engineers.

In 1973, the Model 3340 direct-access storage device used a ski-like design for its read-write head to ride on a film of air just 18 microinches above the surface of the disk. This close proximity between the read-write head and the disk surface effectively doubled the magnetic bit density—to 1.7 Mbits/sq. in. While earlier hard disks were based on removable disk packs, the disks in the 3340 were permanently built into the drive unit. The name Winchester, now attached to all hard disk drives, was coined by developer Ken Haughton. There were two spindles in the IBM 3340, each capable of storing up to 30 Mbytes. Haughton likened the two 30-Mbyte disk modules to the Winchester 30-30 rifle.



The first hard disk storage unit was the RAMAC 350, a refrigerator-sized unit introduced in 1956 by IBM's San Jose Research Center. The RAMAC, which stood for random access method of accounting, replaced sequential access tapes with random access methods, and set the stage for interactive computing. The machine stored 5 Mbytes of data on 50 24-in. platters.

Another IBM development, the floppy disk, was used for loading microprograms into disk controllers for IBM System/370 mainframes. Developed in the mid-'60s, the first 8-in. floppy, a circle of flexible mylar coated with a magnetic oxide, resembled a limp vinyl record when it was introduced in 1970. Former IBM employee and magnetic storage pioneer Alan Shugart believes the floppy disk was one of the technology achievements that paved the way for the personal computer revolution.

Shugart Associates was founded in 1973 to commercialize the 8-in. floppy. The technology, even the 5¼-in. disk, Shugart freely acknowledges, was just a tick mark along the line from the first random-access storage devices of the late '50s and early '60s to the multigigabyte units being developed today (see "High-density disks advance along a path set in the '50s," p 58).

Like digital semiconductors, digital data storage capacity appears to double and quadruple every few years. Researchers at IBM recently demonstrated a magnetic disk with an areal bit density of 1 Gbit/sq. in.—about 1 million times the bit density of the original RAMAC. Commercial hard disk drives are currently produced with an areal density of 100 Mbits/sq. in.

Unlike semiconductors, whose dramatic density increases appear likely to level off between the middle and the end of this decade, magnetic data storage doesn't appear to be reaching its limit. Even the promise of optical storage is no threat to the dominance of magnetic data storage.

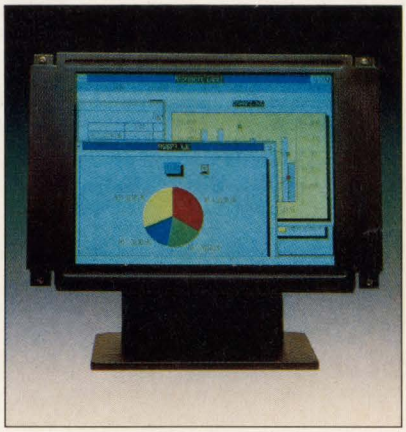
Optical storage is currently providing bit densities of approximately 300 Mbits/sq. in. To increase this density, suggests Dave Thompson, a Fellow at IBM's Almaden Research Center in San Jose, CA, the lasers that serve as optical read-right devices must resort to shorter wavelengths. In addition, the optical read-write equipment must resolve the same kinds of mechanical head-positioning problems encountered by magnetic storage devices. "At 300 Mbits we'll surpass them," says Thompson, a magnetic storage enthusiast.

Though advances in display technology didn't directly enable the digital revolution, they have been most directly responsible for its human appeal. LCD technology is now

providing the focus for the imagination of designers. Already, LCDs have paved the way for the current generation of battery-powered portable computers and televisions. The automotive industry is considering LCDs for dashboard instruments, control consoles and navigational displays. As we approach the year 2000, digital displays will reflect higher resolutions, greater variety and intensity of colors, and larger viewing areas.

LCD developers envision HDTV (high-definition television) and high-resolution computer graphics being shown on large, flat wall-mounted screens. For them, the focus of the competition between CRT and LCD technologies is on the slim-profile LCD screens.

CRT developers cite the superior production economics, resolution and achievable display sizes of proven CRT technologies as a powerful argument for the continued dominance of CRTs. They argue that large wall-panel LCDs will constitute the largest memory arrays known to man, and will be impossible to manufacture economically.



Sharp's 14-in. color LCD screen was demonstrated in 1988. The 1-in.-thick display has 308,160 pixels, arranged in a 640×480-pixel matrix. Each pixel is composed of four dots to ensure reliable operation.

The ideal HDTV unit will likely have a 40-in. diagonal screen. Currently, there are no LCDs that large. Sharp, in Osaka, Japan and Mahwah, NJ, and IBM (in conjunction with Tokyo, Japan-based Toshiba) have demonstrated 14-in. diagonal active-matrix color displays, showing 512 colors with eight light intensity levels. The essential drawback of this technology is its relatively high cost—a problem being addressed by over a dozen Japanese and American manufacturers.

Today's color LCDs are produced by creating a matrix of thin-film transistors (TFTs) on an amorphous silicon substrate. A 14-in color LCD requires about 308,160 pixels (642×480). Each pixel requires four dot drivers (one for each color, plus white), resulting in an active matrix with 1,232,640 TFTs. The matrix provides an addressable pixel array. Each element in the array serves as a shutter for white light, which passes through RGB color filters. The complexity of the LCD array imposes a cost penalty due to manufacturing yields: If a single transistor is bad, the entire array is useless. The problem with manufacturing large LCDs, suggests John Hull, marketing manager with Hitachi Semiconductor in Brisbane, CA, is the same as in manufacturing large memories. As the size of the array increases, the projected yield goes down exponentially. Current yields are in the range of 15 to 30 percent, which makes the cost of a color 14-in. diagonal LCD—at $1,000—four to 10 times that of an equivalent CRT display.

The LCD was first demonstrated at RCA in 1968, following a 1963 discovery that light passed through liquid crystal changes as the crystal is charged with electricity. The earliest LCD was demonstrated by George Heilmeier, now the senior vice-president and chief technical officer of TI, but then head of solid-state device research at RCA. Heilmeier was able to demonstrate that light passed through twisted-nematic liquid crystal materials could be blocked when a voltage is applied across the crystal.

As with ICs, calculators were among the first consumer devices to take advantage of this new technology. Sharp followed RCA into research in LCDs in 1970, and in 1973 introduced the first LCD calculator, the EL-805. It used a series of seven-segment elements in a single glass panel.

A big driver for LCD technology during the '70s was digital wristwatches. In the fall of 1974, National Semiconductor's Novus Consumer Products Division introduced watches for $220. By February of 1975, there were about 40 companies producing digital watches.

Regardless of where one sees the leveling-off point in semiconductor or magnetic storage development, these technology drivers have made it possible for us to reshape the electronics world in digital terms. They helped create a demand for knowledge, information—even music, art and literature—cast in the form of digital data. Whether this now-insatiable demand for data will ultimately be satisfied by semiconductors, magnetic storage, optical S-SEEDs or some other technology, the digital revolution would never have gone as far as it has without the microminiaturization of transistors and ICs.

By Stephen Ohr, Special Contributor

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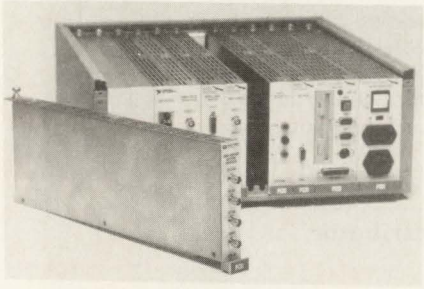
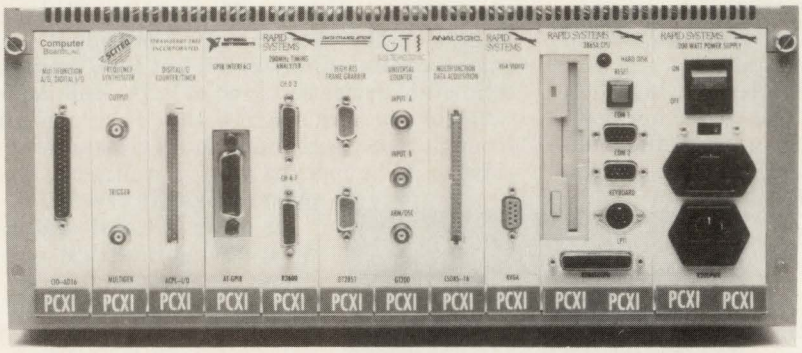


PCXI modules universally accept all PC cards. Instead of one source, you have your choice of the entire marketplace.



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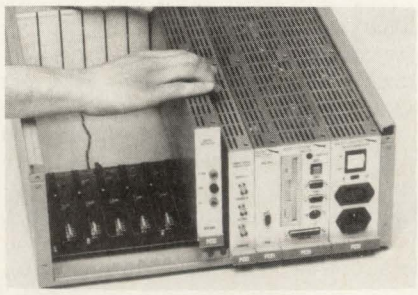

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CIRCLE NO. 70

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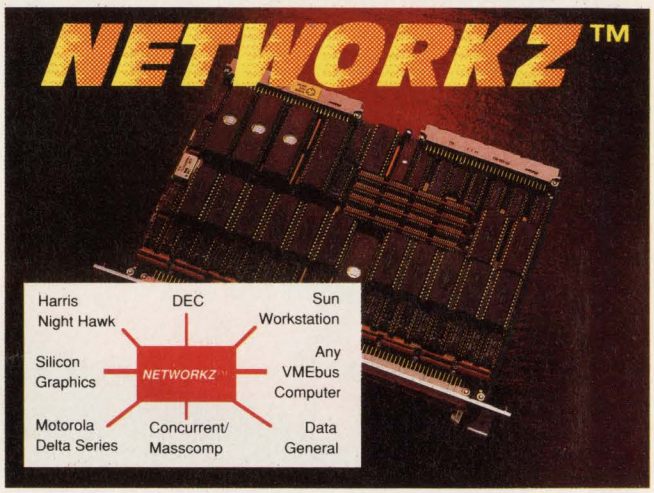

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CIRCLE NO. 38

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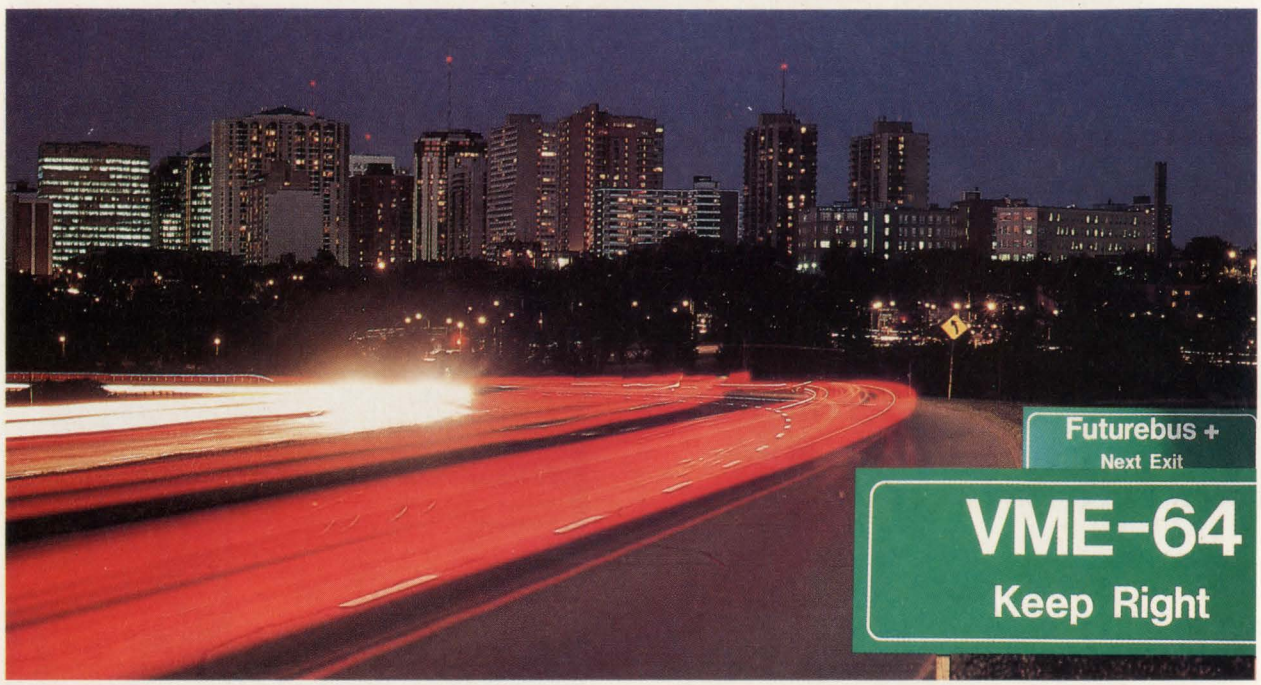

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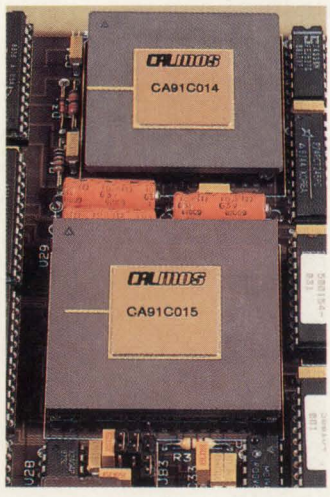

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CIRCLE NO. 39

Computers get personal

The time is the year 2000. The place, the executive suite of an office tower, high above San Francisco. Beyond the windows night spreads across the city, but inside, a senior executive sits down to a last few tasks. From a jacket pocket she draws her personal computer and unfolds it onto the arm of her chair. The surface of the device flickers a 3-D corporate logo as the machine checks into the local network cell, and then it speaks: "Yes, Dr. Forbes?"

Writing on the computer with her pen, sometimes speaking words or sentences, the executive cleans up the last of the day's work. She reviews a video of a teleconference—twice normal speed, and only those portions in which the Japanese executives are speaking, please. She pauses at a particular word, the name of a mechanical part, and by the recorded sound queries the corporate network for a physical model. This she examines for some time, turning it over, illuminating its crevices, watching an animation of its machining steps. At last she reviews her video mail and the evening news, telling the PC to use her customary subject filters. Then she folds the computer, absentmindedly tells it to summon an elevator and warm her car, and slips the device back into her pocket.

Today, such a device hovers between the realms of the likely and the fanciful. But such a computer won't be the work of a lone genius—rather, it will be one more step on the path to completely personal computing. The story of this movement begins about 30 years ago, a story of intertwining strands of hardware and software achievement, forming a lengthening braid. It's a story of growing CPU power, of growing interactivity with humans, and of shrinking physical size.

Thirty years ago, when *Computer Design* published its first issue, all of these advances were simply dreams, latent in what seemed to be a purely practical struggle—the effort of users to gain some control over their computing equipment. The story begins, not with a bang, but with a good deal of ill-tempered whimpering.

In the early 1960s, many scientists and engineers were night people—not by preference but by mandate. Their big, unpredictable applications were only permitted on the mainframe computer after midnight, when there was no danger of crashing the payroll program.

At many corporate research centers and

Freed from its ivory tower by industry innovators, the personal computer now touches all our lives. Today's elementary school children use learning tools that were unavailable at universities 30 years ago.

universities, researchers followed the same routine. By day they would collect data from their experiments, often using the new, inexpensive digital controllers to automatically measure data and punch it onto cards or paper tape. By night, they would carry their data down the dark hall, to the one lighted doorway in an otherwise-deserted building—the I/O room for the mainframe. There, they would hand their data and their source deck to a computer operator. Or perhaps, if the researchers had achieved enough clout, they would actually be admitted to the computer room, to place with their own hands their program before the beast.

Returning to their laboratories with the results of the night's run, many of these people must have gazed at the racks of controls in their labs and wondered if it wouldn't perhaps be possible, someday, to do the computing right there, where the data was collected. To most scientists it was just another five-in-the-morning daydream. But to a tiny core of designers at a young controller company in Maynard, MA, it was much more.

Several factors came together at Digital Equipment Corp. Founder and president Ken Olsen brought high-speed transistor logic circuitry from his work at the Massachusetts Institute of Technology. Core memory, then seen as an enormous advance over the rotating magnetic drums used in early mainframes, was just maturing as a fast, inexpensive technology. But perhaps the key ingredient was DEC's goal—interactive computing. Olsen believed in freeing the computer user from subservience to the batch-oriented mainframe, in making the computer responsive to both the user and the peripheral equipment. DEC's first system, the PDP-1, debuted in November 1960. This 18-bit machine had 4 kwords of core memory, a typewriter, a paper-tape reader, and a CRT. Its computational power was complemented by a real-time control capability, making the PDP-1 system popular for laboratory applications.

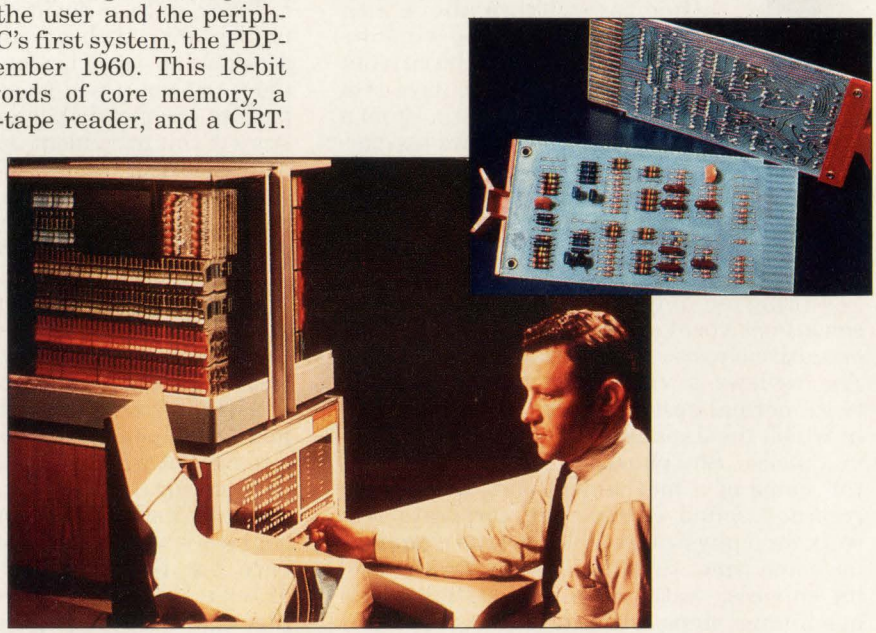
The main stem of DEC's computer genealogy burst forth in 1965 with the introduction of the PDP-8. The DEC designers fashioned an architecture around cost constraints, trading off expensive logic against performance and exploiting the relatively inexpensive core memory. The PDP-8 would have a load/store architecture, a single 12-bit accumulator and a small instruction set, reducing the cost of control logic. It would have an ample—for the time—4 kwords of core. The logic was packaged on plug-in modules inserted in a wirewrapped backplane. Except for the innovation of automated wirewrap technology, the physical assembly was similar to that of the enormous vacuum-tube and transistor machines used by MIT and the Air Force.

The PDP-8 would use the Model 33 teletype for I/O. Programs and data would go in on paper tape. The new computer would be capable of both controlling laboratory apparatus and performing computations, freeing the experimenter from his midnight vigil. The concept of the interactive, personalized computer had seen its first embodiment.

One measure of the PDP-8's success was the rapidity with which it changed. Almost immediately customers cried for more core, and DEC responded with a bank-switching scheme that moved the total up to a staggering 32 kwords. Complaints about paper tape brought faster reader/punches and, eventually, DECtape, a sort-of-addressable, inexpensive miniaturization of the huge nine-track tapes on mainframes.

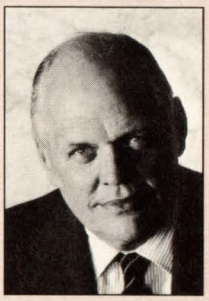
But core prices dropped and programs grew larger. And an even more dramatic change soon made the PDP-8's discrete transistor logic obsolete—the TTL IC appeared on the scene. With this much less expensive and much denser technology, it was time to rethink the cost-optimized architecture of the machine.

The new effort resulted in an entirely new,



Digital Equipment Corp's PDP-8 brought interactive computing to a broad audience. The PDP-8 logic was housed on plug-in modules and built with discrete transistors.

"THE GOAL WAS INTERACTIVE COMPUTING"



Ken Olsen, president, Digital Equipment Corp

Ken Olsen's initial contact with the computer industry was at the Massachusetts Institute of Technology, where he directed development of the computers used in the Sage air defense system, and later managed design of two pioneering transistor-logic computers, the TX-0 and TX-2. "The MIT approach was to use thoroughly designed, fast and simple transistor circuits," Olsen remembers. When Olsen left MIT to found Maynard, MA-based Digital Equipment Corp in 1957, that approach to circuit design came with him. "Those circuits were the basis of DEC, and I think they influenced much of the later work in digital semiconductors as well," he says.

From the beginning, the MIT philosophy of small, fast design fit into the direction of DEC. "When we started, the goal was interactive computing—interactive both with people and with equipment," says Olsen. "We had demonstrated the concept at MIT, but on the outside people still thought it was strange. There was a notion then that computers were supposed to have dignity; that they weren't supposed to respond to people."

Over the years since the PDP-8, DEC's product focus has shifted from single-user minis to massive, enterprise networks. "There are many strategies now, but we're still close to our original goal," Olsen maintains. "By creating an enterprise network, you create an equality among the employees, and the ability to build teams. Teams can come together for long-term projects or just for an hour or two—the network is the medium that makes this possible."

Ideally, Olsen's vision of networking would let any members of an organization interact with the whole computing, data and communications resource of the enterprise. But he says that there are still barriers—though not technical ones—to achieving this promise. "There's still a long way to go before the corporate structure understands what can be gained by networking. Before you can really exploit a network of this size—DEC has about 100,000 people on the network now, for instance—the corporation has to accept networking standards, just like it has had to agree on a common spoken language and a common set of accounting principles. And attitudes have to change—networking needs openness, not privacy, and it can't flourish if groups feel like they're competing with the rest of the company."

This egalitarianism fits well with Olsen's view that progress is a movement; that it's more than the work of a few brilliant individuals. "Most of the advances have been made by people whose names will never be remembered. There have been a few individual inventions—perhaps core memory is an example—but even then, there was still a lot of development work done by a lot of people. I think we've seen the most progress when engineers work in teams, and just get in and enjoy the opportunity to do exciting things, not when individuals work for recognition."

And the pace apparently will continue. "I can't get excited about museums right now," Olsen admits. "The future is moving too fast. With CPU speed, the level of integration, memory capacity and disk capacity all increasing so fast, we're seeing applications we never thought possible. Voice recognition is a good example. And just the opportunity to work with all these motivated people makes it an exciting business."

16-bit minicomputer, the PDP-11. In its economical use of TTL to produce a rich, orthogonal programming environment, many regard the PDP-11 as one of the quintessential achievements of computer architecture. Gordon Bell, who had contributed the instruction set for the PDP-8, created a general-register architecture with a variety of data types and address modes—a machine inexpensive to implement yet beautifully suited to compilers and operating software. The personalized computer had crossed the boundary from asceticism to elegance, a passage we would see again.

Even though the PDP-8 was obsolete by the mid-'70s, it wasn't without its admirers. A whole generation of technical programmers had grown up on the little machines. One who particularly admired the PDP-8, and what it meant to personalized computing, was Stephen Wozniak.

Wozniak, like Olsen a decade before, found himself at the confluence of a number of trends. The birth of the 8-bit microprocessor at Intel had accidentally created computer hobbyists. Groups of amateur programmers came together to build breadboard computers out of 8080 microprocessors and SRAMs, then struggled to connect the things to switch registers and teletypes. Wozniak was a computer club member, and also had access to the new 6502 microprocessor recently introduced by Rockwell. Observing the struggles involved in breadboarding a microcomputer, he decided to put together a kit that hobbyists could use to get going. This was the Apple I.

"The Apple I broke ground in more areas than most people realize," remembers Mike Markkula, founder and vice-chairman of Palo Alto, CA-based Echelon and a cofounder of Apple Computer. "It was the first board-level computer. But it was also the first microcomputer to use DRAM, and the first to have a language in ROM—Wozniak wrote his own integer Basic for the board." But as a consumer success the first Apple was lacking.

"It was just a raw board," Markkula explains. "You had to find your own power supply, your own keyboard and your own display. And the cassette interface wasn't particularly reliable. It was really just a product for the hobbyist."

In response to these problems, Wozniak went back to the drawing board. He conceived an entirely new approach, one that created an industry. The Apple II offered every-

thing—CPU board, keyboard, display and mass storage—in a single preassembled product line. "It was the first time anyone had collected all the things you need to do useful work at a reasonable price," Markkula says. It was the birth of the personal computer.

Just as the arrival of TTL made possible the creation of the PDP-11, the sudden explosion in the density of MOS VLSI made possible increasingly complex microprocessors. And, closely following the pattern of the earlier minicomputers, the 8-bit accumulator-based 8080 generation of chips was followed by 16-bit and 32-bit general-register chips, such as the 8086 and 68000. The new microprocessors dwarfed the computing capabilities of the 6502, and opened the door to a new generation of much more powerful, but more expensive, packaged computers.

The board-level Apple I required hobbyists to add a keyboard, power supply and case. The second product designed by Apple Computer's Wozniak and Jobs was the Apple II, the first personal computer for the mass market.

Barely four years after the Apple II appeared, a new venture in Chelmsford, MA unveiled its first product, the Apollo DN 100. "It was an idea that came from the universities," recalls Mike Greata, group architect at Hewlett-Packard/Apollo and one of the original Apollo designers. "They were the ones who figured out that such a machine should exist, and asked for it."

Essentially, the workstation concept was threefold: a machine that would run big programs under virtual memory, that would live in a network environment with a distributed operating system, and that would be interactive via a high-resolution display. These goals led to a physical package not unlike that of the Apple II, and also to a whole host of new technical problems.

Among the biggest was virtual memory. "The folks designing microprocessors took two or three shots to get virtual memory right," says Greata. "They essentially relearned all the lessons the mainframe and minicomputer people had learned." The practical result of the 68000 microprocessor's lack of virtual memory support was that Apollo had to include two 68000s on the CPU board, one backing the other up in case of a page fault. "We used to call it the world's most expensive set of spare registers," says Greata.

Apollo chose to use a 1,024×800-pixel display, managed primarily by the 68000 microprocessor. "We put in hardware for moving blocks of pixels, but none for drawing vectors or surfaces," Greata says. "It was mainly a matter of affordability."

By taking the concept of a personal, prepackaged computer from the performance range of the 6502 into the then-heady realm of the 68000, Apollo brought individual computing to an entirely new group of users—the scientists and engineers who had been time-sharing on mainframes or superminis. This move started an avalanche in software development, as programs that had been batch jobs with numeric output on mainframes were rewritten to become interactive, graphics-oriented jobs on workstations.

And the DN 100 started another shift as well, not at all unintended. "The idea of a user interface was already there in 1980, before we shipped the first machines," Greata remembers. That idea, which would become the hinge point of user interactivity, had been taking shape since the mid-'70s in Xerox's Palo Alto Research Center, Xerox PARC.

In 1976 in a PARC Learning Research Group technical report, researchers Alan Kay and Adele Goldberg wrote: "Several years ago, we crystallized our dreams into a design idea for a personal dynamic medium the size of a notebook...which could be owned by everyone and could have the power to handle virtually all of its owner's information-related needs."

As a step toward their dream, the PARC researchers put together a human interface system based not on the capabilities of any existing hardware but on their notions of how humans learn and explore. The resulting environment, with its windows, icons and mice, created the visual trappings appropriated by nearly every interactive computing system that has followed.

Much of the notoriety of the original PARC work came from its use in a junior high school, as an experiment in teaching kids to program. This association may have added a more than appropriate note of whimsy to the concepts that were taking shape—object-ori-

ented design, network operating systems, and a formal approach to defining user interfaces. People associated the Smalltalk language more with paint programs and music generation than with formal systems design.

In 1981, Xerox announced its attempt to apply the PARC concepts to a commercial product: the Star workstation. In the hands of product designers the screen became a desktop, the pictures icons, and the standalone "dynamic book" became a node on an Ethernet. Unfortunately, the Star, too expensive for secretaries and too involved for executives, failed as a product. But it had established in everyone's mind the image of a highly productive user interface, an image that would keep showing up in Apples, on workstations and in open standards such as Motif.

While the user interface work at PARC took shape, another revolution was sweeping across the face of computing, changing not only user interfaces but the whole notion of the computer as something people sit in front of. In 1972, Palo Alto, CA-based HP ripped the computer, or at least the scientific calculator, off the desk and stuck it into our pockets.

At $395, the HP-35 calculator was as expensive in 1972 terms as a modest laptop would be today, but companies put together corporate purchases to make the devices available to their engineers, and demand was so strong that HP had to establish a waiting list. Weighing 9 oz, running 4 hr on a battery charge, and running circles around many electronic desk calculators of the day, the HP-35 clearly proclaimed a new truth for the industry—with MOS VLSI chips, you could make anything as small as you wanted.

The calculator may also have been an early study in concurrent engineering. The development team's requirement of shirt-pocket size, high precision, long battery life and reasonable speed dictated new approaches for everything from computational circuitry to computing algorithms and display hardware. And since all parts of the design had to work together intimately, all phases of the design interacted.

The designers partitioned the calculator into two MOS ICs, one for control logic and one for the data path. The programs that produced the calculator's transcendental functions went into three 2,560-bit MOS ROMs, and a couple of bipolar chips drove the LED display. Miraculously, without access to either LCDs or CMOS, the device managed to run on 500 mW, and performed its slowest computations—trig functions—in about half a second. As a computational engine, the bit-serial HP-35 wasn't a barn-burner—but it ended, in one week, the reign of the slide rule.

Almost two decades later, another shrink job is changing the computing paradigm, blending the calculator's notion of instant access with PARC's ideas of a graphic environment. This time the agent of change is start-up Poquet Computer in Sunnyvale, CA. By condensing the PC into a literally pocket-sized package, the company has called forth a new wave of technology to face the problems of volume, power consumption and the user interface.

Poquet's solutions to the volume and power management issues have involved proprietary circuitry, on which 16 patents have been

"CHANGE DOESN'T HAPPEN IN STRAIGHT LINES"

Bill Poduska, president and CEO, Stardent Computer

John William Poduska Sr. claims to be a beneficiary of being in the right place at the right time. "The rate of technical change has been incredible," says Poduska, president and CEO of Concord, MA-based Stardent Computer. "Someone calculated the other day that there's more computing power in one Stellar computer than in all the computers on earth when I was in grad school."

Through all this change the common thread in Poduska's career seems to have been man-machine interactivity. "I went from MIT to NASA Cambridge, where they were working on man-computer graphics systems," he remembers. "In 1972, we took a lot of the work, including the operating system, from that project and tried to build a miniaturized, powerful time-sharing system. That was Prime Computer."

From Prime, Poduska moved on to found workstation pioneer Apollo Computer, and then Stellar, the minisuper vendor that merged with Ardent to form Stardent. Poduska says that these moves reflect the way technology developed in the industry. "Change doesn't happen in straight lines—there are sharp jumps and very flat plateaus," Poduska argues. "Prime really came about because you could build a single-board computer. For Apollo, the important thing was that you could get a whole, serious processor in one part. And the Stellar design was made possible by the emergence of ASICs. Now we're seeing another big jump, this time from RISC architectures. When you see these advances coming at you with cannonball fury, the challenge is to not get numb. Companies stumble when they fail to adopt new technology, not when they keep trying."

As technology drives us up the power curve, Poduska sees two major challenges. "One is what to do with all this power. Sometimes it should create new ways of thinking about things. Visualization, for instance, is becoming an important tool in molecular chemistry—we have added a whole new technique to science, called computational physics. Now we can do experiments entirely on the computer, and observe the results to a degree that wouldn't have been possible with a physical experiment."

The other key challenge will be standardization. "We need a broader sense of standards, for collaboration. That's starting to happen in visualization now—fortunately. I don't think we should be too proud of how we standardized on operating systems or languages in the past. There was a rush to standardize, and more than a little hubris involved."

Looking back, Poduska sees the industry's change made up of two different kinds of contributions. "You could compare it to 19th-century mathematics," he suggests. "We remember the great mathematicians by name. But there were all those artillery officers, civil engineers—people who had to actually use the theories to do things. You have to pay attention to both stories."

sought, according to market communications manager Gerry Purdy. Getting the whole PC into the package, and getting it to run on a set of batteries smaller than the computer, has taken a considerable amount of effort.

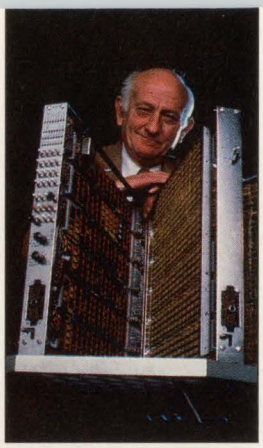
But the more challenging problems involve software. "Task management is a big issue," Purdy says. "A pocket computer creates new expectations—it's not acceptable to wait a few minutes for program loading anymore. What you want is to have all the programs active at once, so you get instant access to the application you want, as you would with a calculator."

A further evolution of the same idea will lead, Purdy believes, to new, pocket-specific applications. He suggests Lotus Agenda as an example of the direction in which applications may be moving. But the final enabling technology for pocket computing will come not from software but from telephony: the CT-2 small-cell wireless phone network.

The combination of a large number of channels and physically small transmitter, both made possible by CT-2's very small distance between stations, is ideal for the pocket computer. In such an environment, a combination of pocket computer and cellular phone can stay in continuous touch with electronic mail services, getting dialed up automatically any time a message appears. The continuously available communications software can download the message, and have it ready the next time the user opens the cover.

This level of services would be great, but it couldn't even be considered with the sort of computing power available to Apollo in 1980. The possibility for a microprocessor-based computer able to handle this sort of computation and multitasking came not from dramatic increases in IC performance—although that didn't hurt—but from yet another thread in the braid of progress, a little-noticed mainframe project named after a building.

By 1975, John Cocke was a veteran IBM CPU architect. He had participated in the Armonk, NY-based company's original advanced architecture effort in the '50s, the Strech project. More important, he had been involved in the mid-'60s Advanced Computer System project. The ACS, as it was known, was IBM's second major attempt to produce a breakthrough architecture. Like Strech, ACS never saw the light of day, but its ideas filtered into the market in diverse ways. One way was through Gene Amdahl, who left the ACS project to pursue the goal of advanced 370-type mainframes on his own. Another avenue was through Cocke, who returned to IBM's Watson Labs to follow some of his own notions about advanced architectures, along a path originally found in the '50s by M. Fromme at Zuse Computer in Bad Hersfeld, West Germany.

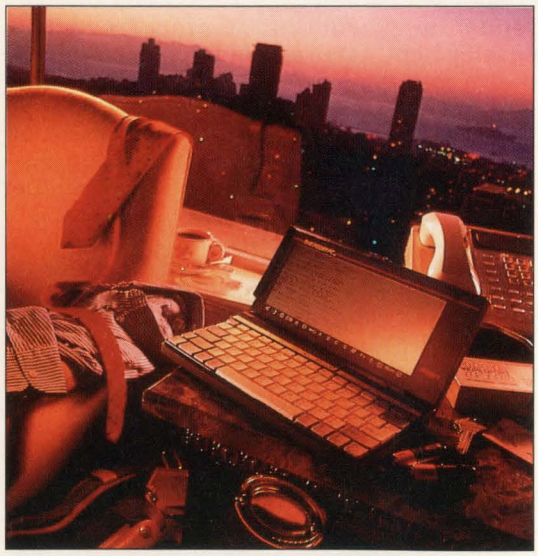


The early work of IBM computer architect John Cocke led to the RISC-based approach to computing. His first machine was called the 801, the number of the building where his lab was located.

"John became the principal spokesman for the idea of a small, advanced machine," says Mike Blasgen, IBM director of advanced RISC systems. "He walked the halls talking to people—it wasn't his way to write a lot of memos—until management finally decided to pursue the project." The result was an effort to build an extremely fast, minicomputer-sized box with mainframe power. In a salute to the great IBM mainframes of the old days, which allegedly took their names from the buildings in which they were conceived—the 701, 702, and so on—the new machine was christened after Cocke's building number at Watson Labs: 801.

"The original emphasis was on one instruction per cycle," Blasgen says. "But it was important to get there without a big increase in the number of instructions necessary to do the job. Also, from the beginning the instruction set was intended to be the target for the compilers—the team wanted to eliminate the use of assembly language. This led to a threefold project, in which the hardware, the compiler and the applications were all developed together.

"To get to one instruction per cycle, it was necessary to build a pipelined CPU and to use a split cache—one cache for instructions, another for data. To get good performance, a lot of time was spent on register allocation—and it was decided in mid-project that the 16



Some personal computer users can't leave their computers behind. This pocket-sized PC from Poquet Computer is one result of the evolution of PCs.

From calculator to computer

Advances in many fields made it possible to personalize computing, but it was IC technology, and IC economics, that delivered computing to the masses. The democratization of computing began with two concepts and two calculators. The concepts were integrating a complex circuit on a single chip and, later, allowing the functions of an IC to be defined by programmed instructions. The calculators were the first hand-held, developed by Texas Instruments, and a table-top model from Busicom.

When Jack S. Kilby, the inventor of the IC and the hand-held calculator, went to work for TI in Dallas in May 1958 he was assigned to the micromodule program TI was conducting for the Signal Corps. The first IC was an analog circuit, a phase-shift oscillator, consisting of several germanium mesa transistors, diffused resistors and capacitors on a 7/16-in. substrate, but interconnected by hand with gold wire. TI and other companies actively developed IC technology in the following years, but the digital revolution didn't really take off until Kilby invented the hand-held calculator.

Patrick Haggerty, TI's president in the mid-'60s and a great advocate of IC technology, pressured Kilby into using IC technology to build the first hand-held calculator. When work began on the project in September 1965, there was no precedent for the machine. Virtually everything had to be invented. The "calculator-on-a-chip" packed the equivalent of 6,000 transistors—the first large-scale integration—but the breadboard for the design took up the better part of a room. Kilby, together with Jerry Merryman and Jim Van Tassel, filed for a patent on the design in 1967, though the award (Patent #3,819,921) wasn't granted to TI until 1974.

The early IC industry was driven by customers who needed specialized parts, some of which would emerge later as standard products. The first commercial microprocessor was a case in point. What was eventually marketed as the first single-chip microprocessor, the 4004, actually began life as a custom product developed by Intel for Busicom, a Japanese calculator manufacturer.

Calculator manufacturers of the early '70s were demanding customized chips as a means of differentiating their products. The response of many semiconductor makers was to partition the logic of the calculator in ways that could generate standardized building blocks.

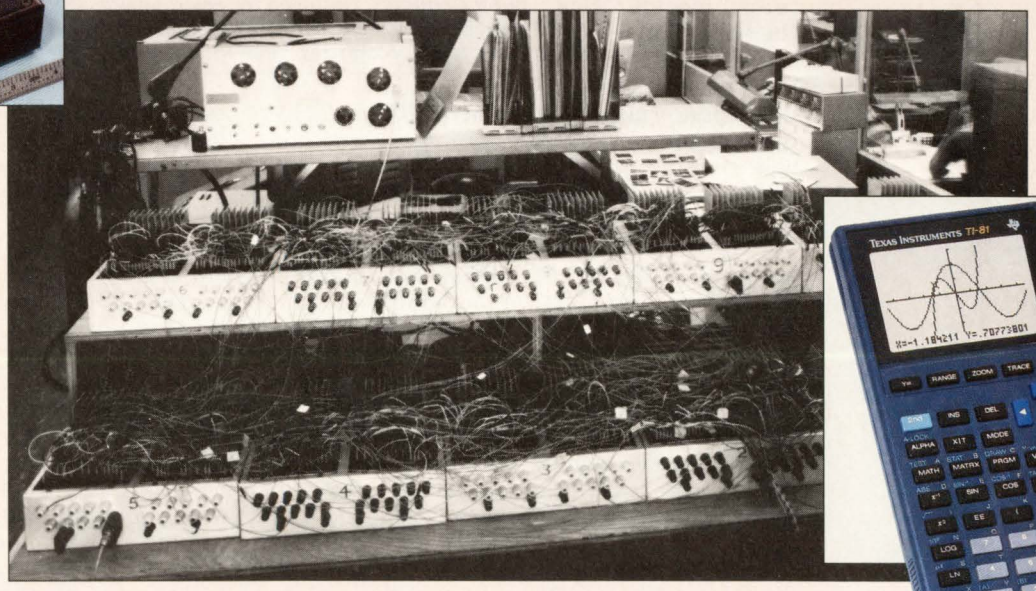
Intel was incorporated in July 1968 by Gordon Moore and Bob Noyce, who left Fairchild to set up a company dedicated to the economical manufacture of large-scale circuits. Intel was asked to design a chip set for Busicom in August 1969. Marcian (Ted) Hoff, then Intel's applications manager, is credited with the inspiration for the calculator's architecture. The Busicom calculator differed from others in that it used ROM-based program memory. Instead of building a dedicated calculator—an adder with some programming capabilities—the architecture of the Busicom machine resembled a general-purpose computer that was programmed to be a calculator.

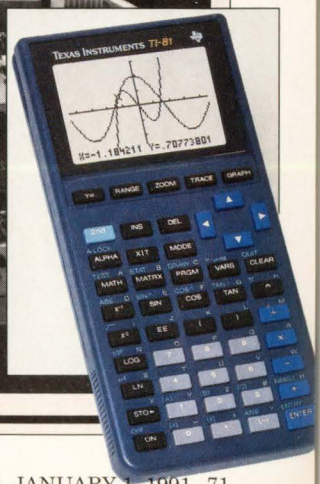
The 4004 was designed by Stan Mazor and Federico Faggin (who later became president of Zilog). The device was a 4-bit microprocessor: it could take in only four digits (bits) at a time. There was no software. But it was supported with a 32-bit on-chip RAM, a 256-byte ROM and a 10-bit shift register and output expander. It could address up to 16 256-byte ROMs (4,096 bytes) and 16 RAMs (4,120 bits). With an instruction execution rate of 60,000 instructions per second, it had the same processing power as the early Eniac computer.

The Busicom company was relatively short-lived. When one of its top designers, Masatoshi Shima, joined Intel in 1971, Noyce decided to buy back the rights to the chip. The 4004 was then advertised for sale in the fall of 1971. In April 1972, the first 8-bit microprocessor, Intel's 8008, was announced.

By 1973, microprocessors had outgrown their position as building blocks for calculators, and were being considered as general-purpose processors. Though they were much slower than minicomputer CPUs, practically everyone in the electronics industry could see their potential for reducing the size and cost of computer-controlled equipment.

The first processor to be used in personal computers—then intelligent alphanumeric terminals—was the 8080, introduced in April 1974.





The first hand-held calculator packed a tableful of discrete electronics (center) into a palm-size package (left). A fledgling IC house called Intel later designed the first microprocessor for Busicom, a calculator manufacturer. Today's calculators adopt features such as graphical displays and pull-down menus from the personal computers they helped spawn.

registers in the 370 architecture wouldn't be enough. So the 801 had 32."

The 801, implemented in ECL, clearly demonstrated that Cocke's approach was valid. A processor with a simplified instruction set, one instruction-per-cycle execution and heavy dependence on compiler technology could in fact yield enormous performance from a small package. But, like its predecessors, the 801 didn't go directly to market. It did show up, unknown to customers, as an I/O processor in the 3090 mainframe. And it received its final vindication when, starting in 1986, the 801 team worked with IBM's Austin, TX facility to reimplement the architecture in CMOS, producing the now crushingly powerful RISC System/6000.

But if Cocke's ideas didn't show up in the industry right away, they were certainly not lost on academia. Groups at both Stanford and the University of California at Berkeley picked up the RISC idea and ran with it. Both projects resulted in commercial microprocessors: the Berkeley group, with its emphasis on hardware, associated itself with Mountain View, CA-based Sun Microsystems and produced the Sparc architecture. The more compiler-minded Stanford group, meanwhile, formed MIPS Computer in Sunnyvale, CA.

The resulting microprocessors fired workstations to a new performance plateau, accelerating the shift of analytical software and complex user interfaces onto these platforms. But even as RISC was solving one set of computing problems, another was emerging. This new computing load threatened to be more than any general-purpose CPU could handle.

The human interface is a critical issue for personal computer designers. Designed for environments that make a keyboard or mouse impractical, the pen-based Gridpad system recognizes handwriting in 10 languages.

Ever since the mainframe days, researchers in a few fields had been struggling with one big problem—how to produce realistic images of solid objects. The problem of visualizing solids was important to molecular chemistry, where developers were learning to create molecules on the computer; to structural design, where computer models could show shape, range of motion, deformation under stress or heat flow; and in architecture, where computer modeling could cut months off the time required to model a new building.

But the numerical requirements for producing a lifelike 3-D image are staggering. And as algorithms evolved, the problem got worse—new algorithms tended to produce more accurate images, rather than to reduce the amount of computing required. Researchers tried Cray computers and graphics terminals. They tried powerful workstations. They tried Cray computers driving workstations. But interactive visualization escaped every attempt to subdue it with general-purpose hardware.

"We have made major progress in realism," claims Rick Mayes, marketing manager for HP's graphics technology division. "We've gone from wireframe images to flat polygon surfaces to Gouraud shading. Now we're working on radiosity—modeling how reflected light behaves."

This progress has been spearheaded by algorithm development on the Crays, but it has found its way to market in dedicated graphics chips. "As we moved to shaded solids, we also moved to hardware Z-buffers, transform engines and raster-op accelerators," Mayes says. "Now we have things like a dedicated Gouraud-shading chip."

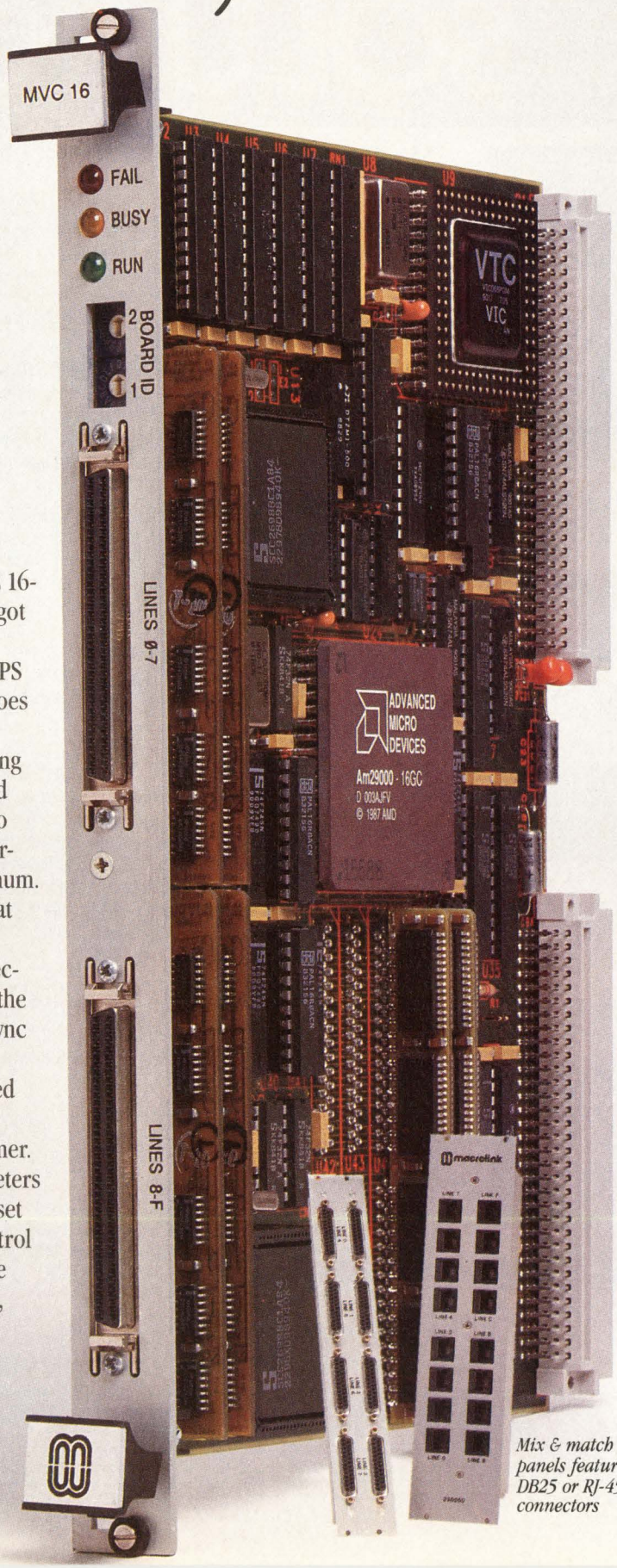
The intertwining strands in the braid are drawing together. Computational power, driven by new architectures and new processors, is still growing. Miniaturization, supported by the experience of several generations of pocket computing equipment, is up to the task. Special-purpose graphics hardware is ready to take on the challenges of visualization as an interface paradigm. And researchers are pouring their energies into such areas as pen input and voice recognition.

Within the sweep of 30 years' history, from the first PDP-8 to the 3-D workstations and pocket computers of today, the next step doesn't seem so large. You can almost close your eyes and imagine the personal system of the year 2000, waiting there in your pocket.

In the garage of her office building, the executive fingers her PC once again, telling it to unlock her car and, perhaps, to wake up her townhouse for her arrival. Then she snaps shut the thin plastic case that carries her connection to the electronic world, and her connection to 40 years of uninterrupted technical achievement.

By Ron Wilson, Senior Editor

16 lines, No waiting.



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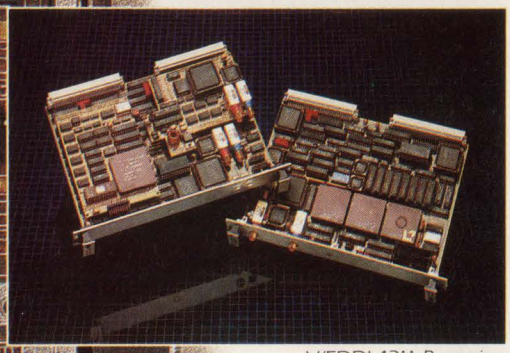
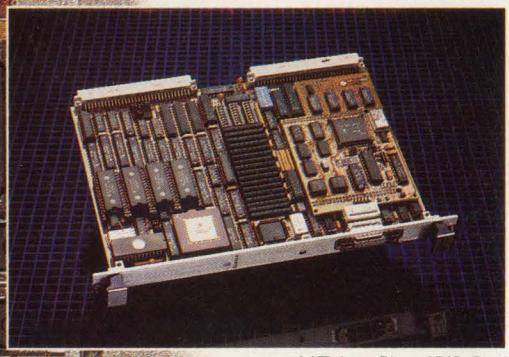
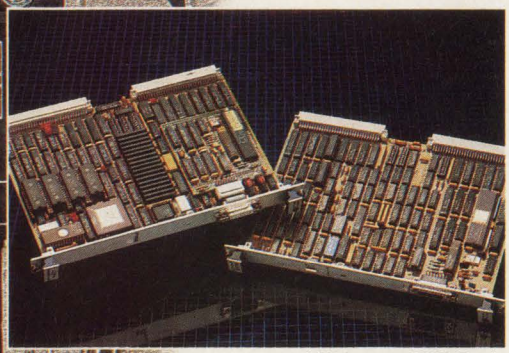


V/FDDI 4211 Peregrine
V/FDDI 3211 Falcon



V/Token-Ring 4212 Owl



V/Ethernet 4207 Eagle
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CIRCLE NO. 41

Digital communications link the world on wires, lightwaves and airwaves

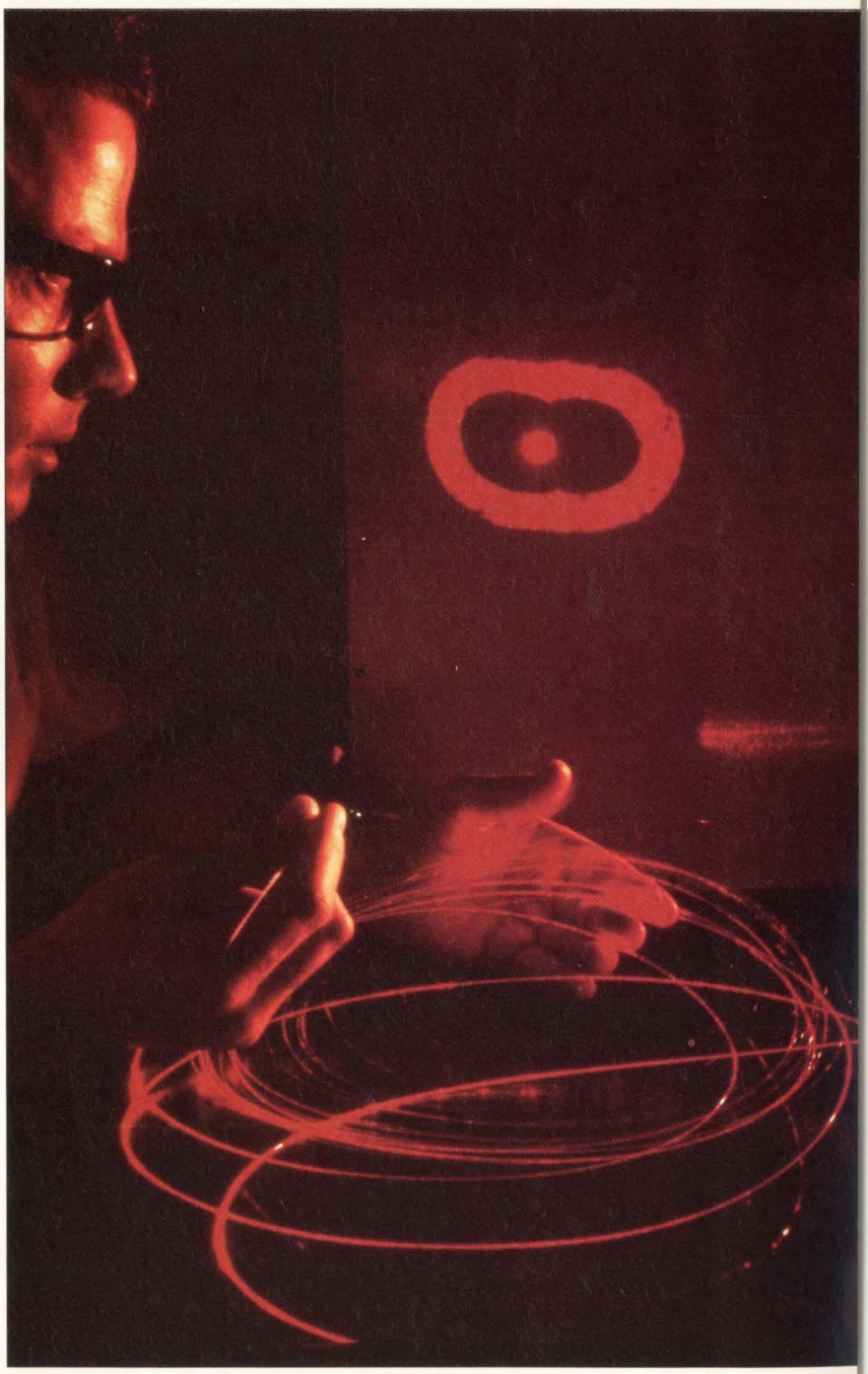
In the world of communications, digital technology is virtually shrinking the world. New communications technologies are bringing down the barriers of distance and time that used to separate people, ideas and information. But digital technology is only one part of a revolution that's equally fueled by breakthroughs in optical transmission, advances in semiconductor electronics, and progress in the telecommunications infrastructure (particularly in telephone call switching and wireless communications).

The impact of the communications revolution is changing the very fabric of society. And the road to this revolution begins with an evolutionary milestone in communications—the shift from analog to digital methods.

Many of the pioneers of digital telecommunications have stories to tell about the process of getting an analog-oriented manager to accept digital thinking. For example, Paul Baran, chairman of Sunnyvale, CA-based Inter Fax, is considered the father of packet-switching technology. Baran tells now-amusing stories about persuading management at AT&T to accept digital thinking in the early 1960s. The analog technologists within the Bell system were used to thinking of each call between, say, New York and California as a single electrical connection: "Wait a minute, son," says Baran, mimicking a supervisor. "You're telling me that the switch opens *before* the signal goes across the country?!"

Baran's work was implemented in the early '70s as a private telecommunications network—ARPAnet—using 1.5-Mbit/s pulse-code modulation (PCM). The implementation was undertaken by Cambridge, MA-based Bolt, Beranek and Newman (BBN). Four nodes were attached in 1969; 29 nodes were attached in 1972; and 37 nodes were up and running in 1973.

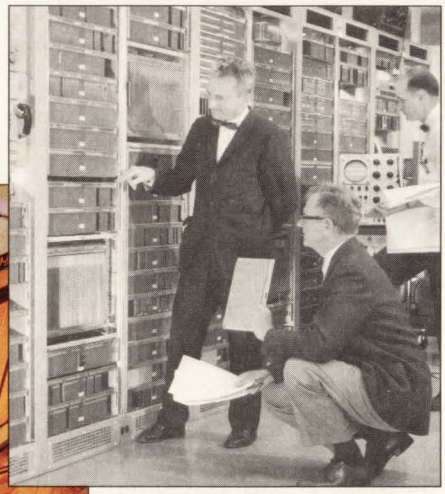
Once the Federal Communications Commission permitted private companies to enter the communications business (using leased lines from AT&T), BBN worked on making



Bell Labs' announcement of this optical fiber in 1973 foreshadowed the digital transformation of communications.

ARPAnet a commercial venture. Telenet Communications was formed by three employees of BBN in 1972 to build a nationwide packet-switching network. Telenet's first-generation network in 1975 was the basis for the X.25 packet-switching standard. Telenet was acquired by GTE in 1979. In 1986 GTE included Telenet in its portion of a joint venture with Kansas City, MO-based United Telecommunications. The venture was called US Sprint. Canada, France and Japan began work on packet-switching networks shortly afterwards, building impetus toward an international standard.

The International Telegraph and Telephone Consultative Committee, an agency of the International Telecommunication Union, issued the first standards for X.25 packet switching in 1976. The standards define the interface between user terminal and packet network: the X.25 protocols allow multiple services—voice and data—as well as multiple users on one multiplexed line. It's the forerunner of new services that will come in under the umbrella of ISDN (Integrated Services Digital Network).



The telephone system is evolving toward digital end-to-end service, termed ISDN. Key to this transformation are switching centers tailored to a digital environment. Today's 5ESS can handle 300,000 calls per hour; 1963's ESS-1 used digital techniques to switch analog signals.

In the early '70s, packet switching seemed ready to move into the public sector with an implementation by the Post, Teleohone and Telegraph in England. In 1975, Telenet introduced its own private service in the United States with a seven-node network. By 1977, public networks were operating in the United Kingdom and Canada. Telenet connected with the Canadian network in 1978. By 1982, public packet-switching networks were planned for more than 20 countries.

The need to send data between computers has driven the growth of LANs, as well as long-distance services. Of the prevailing LAN hardware, Ethernet—developed by Xerox's Palo Alto, CA Research Center in the mid-'70s—has come to dominate.

While Ethernet is a standard, its suppliers differ in their approach to protocols (which determine how data transmissions are formatted and read). Protocol choices for Ethernet have included Sun Microsystems' Network File System; Digital Equipment Corp's DECnet; Xerox's Network System; and the Defense Department's TCP/IP (Transport Control Protocol/Internet Protocol), which was originally developed for ARPAnet.

TCP/IP is now supported on all types of computers from personal computers to supercomputers. It defines layers three through seven of the Open Systems Interconnection communications reference model. The two lower layers have already been defined, largely in hardware by the IEEE-802 standards for LANs.

Not everyone is satisfied with the emergence of TCP/IP, though, since the protocol dissection required can slow down data transfer speeds. TCP/IP has been benchmarked at 1.2 Mbits/s, for example, compared to 1.5 Mbits/s for DECnet. (In principle, Ethernet allows data communication rates up to 10 Mbits/s, and the Fiber Distributed Data In-

terface will allow communication rates up to 125 Mbits/s.) But networking guru Judy Estrin, executive vice-president of Mountain View, CA-based Network Computing Devices, doesn't believe that there will be any serious challenges to the dominance of TCP/IP in the next five to 10 years: "It works and works well," says Estrin.

The first digital telephone system, the ESS-1 (electronic switching system), was announced by Bell Labs in 1963. The ESS-1 wasn't a digital transmission system at all—it was a computer-controlled system of interconnects for analog signals. (The switches were actually encapsulated reed relays.) Its memory included programs for opening and closing circuits based on the digits being dialed by a caller. It could handle up to 10,000 lines. In England, the British Post Office, in conjunction with Plessey, developed the TX-E2, which was put into service in 1966. This system could handle from 4,000 to 7,000 lines. The advantage to the user of these early systems was that they allowed calls to be processed faster, and provided additional services such as conference calling.

Concurrent with electronic switching in the '60s was digitally based telephone equipment built around the transistor and IC. Typical of this equipment was a private company switchboard—the private branch exchange—and a repertory dialer, which enabled customers to store numbers at the telephone station.

The digital private access branch exchange was developed, suggests Baran, under the assumption that only parts of the existing telephone network could be replaced. (The subsequent installation of fiber trunk lines in 1981 and the "deregulation" of the Bell System in 1982 would alter these assumptions drastically.)

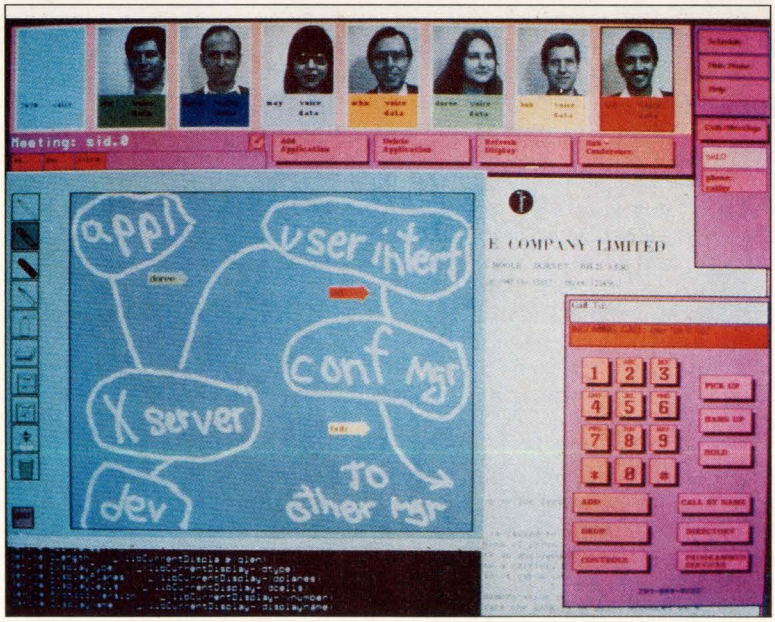
Advances in telephone communications typically balanced line cost and computer switching costs. In the early '50s and '60s, lines seemed plentiful and cheap, and the computer switching gear was expensive. The relationship reversed itself in the '60s and '70s, setting up the possibility for multiplexed lines, as well as the ability to use multiple lines in the service of one call. One example of this ability, the CCISS (common channel interoffice signaling system), set up a separate channel for directing calls using set frequency tones.

The SS-7 (signaling system), for example, uses a separate packet-switching network for directing calls on an otherwise conventional network. This provides translation and routing for dialed calls. The 800 toll-free numbers, for instance, must be translated into particular area codes and numbers before the call can go through. The information on 800 call routing is typically stored in a central database, and accessed with a separate packet.

To an otherwise conventional control channel, packet switching on the SS-7 contributes error detection, acknowledgement fields and distributed network access to a common database. Additional services that may be implemented are fast routing, the avoidance of busy signals on the line and the ability to see the telephone number of the caller.

However, it was the demand for data communication services that forced the telephone company to explore digital transmissions. The T-1 carrier systems—the first truly digital signal transmission networks, capable of a data transfer rate of 1.54 Mbits/s—were developed in the late '50s and are still regarded as workhorse technology today. T-1 service over leased cable lines is still the preferred long-distance carrier for large companies with far-flung networks. Companies with leased T-1 lines created private voice and data networks.

Each T-1 link normally carries 24 full-duplex 64-kbit/s voice channels using PCM. If adaptive differential PCM is used, the silence between signals is suppressed, and about a 5X improvement in throughput can therefore be expected. A signal T-1 line offers about 96 channels of toll-quality voice.



AT&T researchers are working on a distributed conferencing system that lets participants speak face-to-face through their own computers while sharing notes, data and video images.

The PBX allowed easier control of telephone lines than the traditional cord-and-jack switchboards it replaced. These 40-button telephones allow control of new services made possible by ISDN, such as calling-number identification.

Today's telecommunications technologies transmit more than voices and images; in some cases they seem to permit the transmission of 3-D objects. Digitizing and mathematical modeling transform solid objects into data files that can be manipulated and transmitted by computer systems. A physical prototype designed in one place today can be precisely reproduced on a computer screen or machine tool on another continent within minutes.

AT&T Bell Laboratories researchers in Holmdel, NJ are currently working on a remote conferencing system, in which all of the participants sit at their own computers. The system would let conference participants see each other face-to-face and share a central computer screen—called the "conference room." They would be able to enter or leave the room at will, view static or moving video images, and share and manipulate programs and data on the central computer screen. "All it takes is wider-bandwidth cable and image compression, but the technology is available," says Sudhir Ahuja, who heads the integrated computer communications research department at the labs.

Much of the hope for the future is placed in ISDN. AT&T in particular sees ISDN as the platform for all new-generation communications systems. ISDN, in fact, provides a "superset" for the digital communications services already established with T-1 leased lines, X.25 packet switching and SS-7.

ISDN is the first entirely digital end-to-end service. It's set up as a wideband network with three information channels per user. Computer and digitized voice are multiplexed on the same physical channel, but a separate D-channel serves as a supervisor.

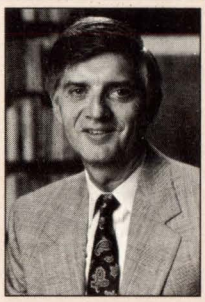
ISDN is a synchronous network, providing channels for speech and data. Speech is transferred at rates up to 64 kbits/s, while data can, in principle, be transferred at rates of 2, 8, 34, or 140 Mbits/s. Digitized video signals can also be multiplexed along this line. Separate channels in the network are required for each bit rate. Consequently, most implementations use narrowband communications that put all traffic on the line at uniform 64-kbit/s rates. Dynamic bandwidth allocation isn't a feature of current telephones.

Broadband ISDN, in contrast, provides bandwidth on demand to each user. So video transmission will automatically claim a high bandwidth (stream traffic), while ASCII text transmission will be delegated to lower data rates in the background (burst-mode traffic). Broadband ISDN allows an asynchronous transfer mode—a packet-switching scheme—in which packet lengths will vary, depending on the amount of bandwidth required.

Broadband ISDN is touted as the vehicle that will allow multimedia conferencing, secure voice and video telephone.

Munich, Germany-based Siemens implemented the world's first broadband ISDN system, the ISDN-B, in Berlin in October 1989. The ISDN-B provides 140-Mbit/s data rates. The Berlin Communications System uses the asynchronous transfer mode. An automatic broadband switching center provides

"Even without computers, we would have invented digital communications."



Robert Lucky, executive director of communications research at AT&T Bell Labs

Thanks to international telephone communications, the world is becoming smaller by the moment," says Robert Lucky, executive director of communications research at AT&T Bell Laboratories in Holmdel, NJ.

The author of *Silicon Dreams: Information, Man, and Machine* (St. Martin's Press, 1989) can identify many of the technological developments that have revolutionized the social landscape. "With nearly one-half of the current international traffic now facsimile transmission," Lucky points out, "the fax is clearly one of the great social revolutions of the '80s." Federal Express, cellular telephones and video stores are identified by Lucky as other examples.

He sees two major threads to technology development in communications. One is the transformation brought on by digital communications technology; the other is wideband networking that effectively ties everything together.

Though Lucky's own work began at the start of the digital revolution, his first assignment at Bell Labs was in analog modem development (1961). He contributed to development work on 300-bit/s and 1,200-bit/s analog modems (which resulted in the Bell 103 and Bell 212 communication standards). Lucky invented many of the adaptive equalization algorithms for 9,600-bit/s modems.

In the early '60s, digital telephony was still regarded as a "far-out technology" at AT&T, says Lucky, who was influenced by Oliver, Pearse and Shannon's late-'50s paper, "The Philosophy of PCM." It presented a case for why one should go digital. To Lucky, it was clear that digital transmission could prevent the accumulation of noise and distortion. "Even without computers, we would have invented digital communications," he says.

All-digital ISDN (Integrated Services Digital Network) is identified as the major platform for all new-generation communications systems. Broadband ISDN will provide bandwidth on demand, says Lucky, which will enable multimedia conferencing, secure voice conversations, video telephone, high-fidelity audio—almost any communication service imaginable.

The wireless Personal Communications Networks, however, will likely be the biggest growth area for the '90s, driven by the increased use of laptop computers. "Within five or six years," predicts Lucky, "the proliferation of wireless LANs will encourage the development of a wireless PABX (private access branch exchange)."

asynchronous communications at 2 Mbits/s and synchronous communications at up to 140 Mbits/s. The network currently links about 40 users, including universities, scientific institutes, Berlin city offices, hospitals, hotels, and a small number of corporations. Connection is made through fiberoptic cables. The system consists of some 30,000 km of fiber, and has feeder lines for cable television networks as well as public telephones.

The invention of the laser coincides with the start of the digital revolution in the early '60s. Much of the pioneering work was done by Arthur Shallow at Bell Laboratories, although there are continuing patent disputes. Robert Hall produced a gallium-arsenide injection laser at General Electric in Schenectady, NY at about the same time. This device produced so much heat that it needed liquid nitrogen as a coolant. Similar devices were developed at the same time at Armonk, NY-based IBM and at the Massachusetts Institute of Technology's Lincoln Laboratory.

Optoelectronics devices based on low-power LEDs blossomed in the '60s. The first LED was introduced in December 1962; the first commercial LED displays were sold in 1968.

The advantage of the GaAs laser was that it could direct light as monochromatic beams. In addition, it could transmit digital pulses or analog waveforms with equal facility, since its light beam could be regulated (much like the grid of a vacuum tube) by variations in the diode drive. The first room-temperature semiconductor lasers were demonstrated at Bell Labs in 1970.

In 1972, researchers at IBM produced a GaAs laser that could generate a beam of light only 2 μm in diameter. This was small enough to couple the laser power with the smallest diameter single-mode fibers. With low-attenuation fiber, fewer amplifiers and repeaters were needed. IBM researchers obtained data rates in excess of 100 Mbits/s.

By the mid-'70s, Bell Labs was reporting major increases in diode lifetime and was projecting 1 million hours of useful life. RCA, based in Somerville, NJ, introduced a planar diode in 1979 that could be made with IC fabrication techniques.

In 1971 Corning Glass of Corning, NY introduced a usable low-loss fiber—one that would attenuate a signal by only 20 dB over 1 km. While current fiber technology will provide signal attenuation as low as 0.2 dB/km, the 20 dB of 20 years ago was regarded as a breakthrough in transmission costs, since repeaters need be installed only at every kilometer, rather than every few feet along the cable.

In 1976, a Bell Laboratories experiment demonstrated the feasibility of mass-produced fiber cabling. Bell engineers showed that cables made up of 144 separate fibers could be mass-spliced without individual handling. These cables—½ in. in diameter—could handle almost 50,000 separate telephone conversations.

The first commercial fiber installation took

Putting data into packets

Paul Baran, chairman of Inter Fax

Paul Baran, chairman of Sunnyvale, CA-based Inter Fax, is the father of the digital communications technology known as packet switching. In brief, the concept of packet switching lets you send out a continuous message as a series of digital packets on a distributed network. Each of the packets may be routed by switches at the nodes of a network grid to reach a common destination. At their destination, they are reassembled into a coherent message. Baran was awarded the 1990 Alexander Graham Bell Medal for his pioneering work on packet switching.

Baran's early work for Santa Monica, CA-based Rand in the late '50s and early '60s was to develop survivable command control structures for the military. He conceptualized a communications network using a mesh connection of redundant links. The redundancy allowed by distributed networking meant that the network could have breaks in its structure and still be able to pass digitized message blocks. Packet switching could also build on existing links within the public telephone network.

The first major packet-switching network, ARPAnet, implemented in the early '70s, used fairly low data rates on leased lines. However, ARPA—what Baran calls "government money administered by academics"—funded several computer time-sharing projects at university sites, and has had a major influence on students of networking (including Judy Estrin, now executive vice-president of Network Computing Devices in Mountain View, CA). Baran says that ARPA then accounted for 60 percent of all computer research in the United States.

place in 1977, a joint effort of Stamford, CT-based General Telephone and Electronics and the Bell System. It was a short-distance system. By 1979 Tokyo, Japan-based Nippon Telegraph and Telephone had produced a fiber with 0.2 dB/km loss, and Bell Laboratories had demonstrated digital data rates up to 200 Gbits/s. The first long-haul fiber communications system, connecting New York City, Philadelphia and Washington, DC, was installed in 1981. Now, AT&T estimates that between 80 and 90 percent of all long-haul communications go across fiber cable.

Many believe that Personal Communications Networks on cellular telephone frequencies (825 and 894 MHz) can offer the same services as ISDN—mixed voice and data—to a mobile user. Within an office, wireless networks may replace much of the cabling, hardware and expense associated with Ethernet.

NCR of Dayton, OH has demonstrated a wireless network, called Wavelan, based on spread-spectrum technology. With a 2-Mbit/s data capacity, it can transfer serial data files, but it isn't fast enough for real-time transmission of bit-mapped graphics. Wavelan's advantage is that it costs far less than an Ethernet node and that it's easy to install. The entire unit, including an omni-directional antenna, can be plugged into the back of a PC/AT computer.

Spread-spectrum communications are used in military defense applications to prevent enemy jamming or eavesdropping on radio communications in the field. Spread spectrum uses low power across the frequency band from 902 to 928 MHz. At that frequency, the network is immune to interference from radios, cellular telephones and other communications devices (but not from military radar). Because of its low power, it requires no FCC broadcast license.

Motorola's Radio-Telephone Systems Group in Schaumberg, IL, however, has announced a wireless Ethernet replacement that offers a 15-Mbit/s data rate on an 18-GHz radio frequency. Called WIN (wireless in-building network), the system uses a six-sector intelligent antenna, an RF digital signal processor, a GaAs transmitter/receiver and a packet-switching controller. The power level of the WIN transmitter is about 20 mW, roughly 4 percent of what a standard cellular telephone requires. The use of the 18-GHz frequency—now designated the "digital termination service band"—takes advantage of an FCC ruling that allows low-power radio communications to be used inside buildings.

The revolution in wireless communications—hand-held data entry terminals, car and personal navigation systems, as well as cellular telephones and pagers—has forced a reexamination of the ways in which the RF spectrum is currently allocated and used by FCC licensees. Consequently, many of the changes in wireless communications may be driven more by politics and market forces than by technology.

The surge in mobile communications has encouraged Motorola to announce plans for Iridium, a satellite network that would let people call or receive calls from anywhere on earth. Satellite communication takes place at frequencies from 1 GHz to 60 GHz. This range will extend mobile communications to places not covered by cellular telephones.

Whether information is carried as photons or packets on fibers, wires or radio waves, a new age of communications based on digital technologies is unfolding.

By Stephen Ohr, Special Contributor

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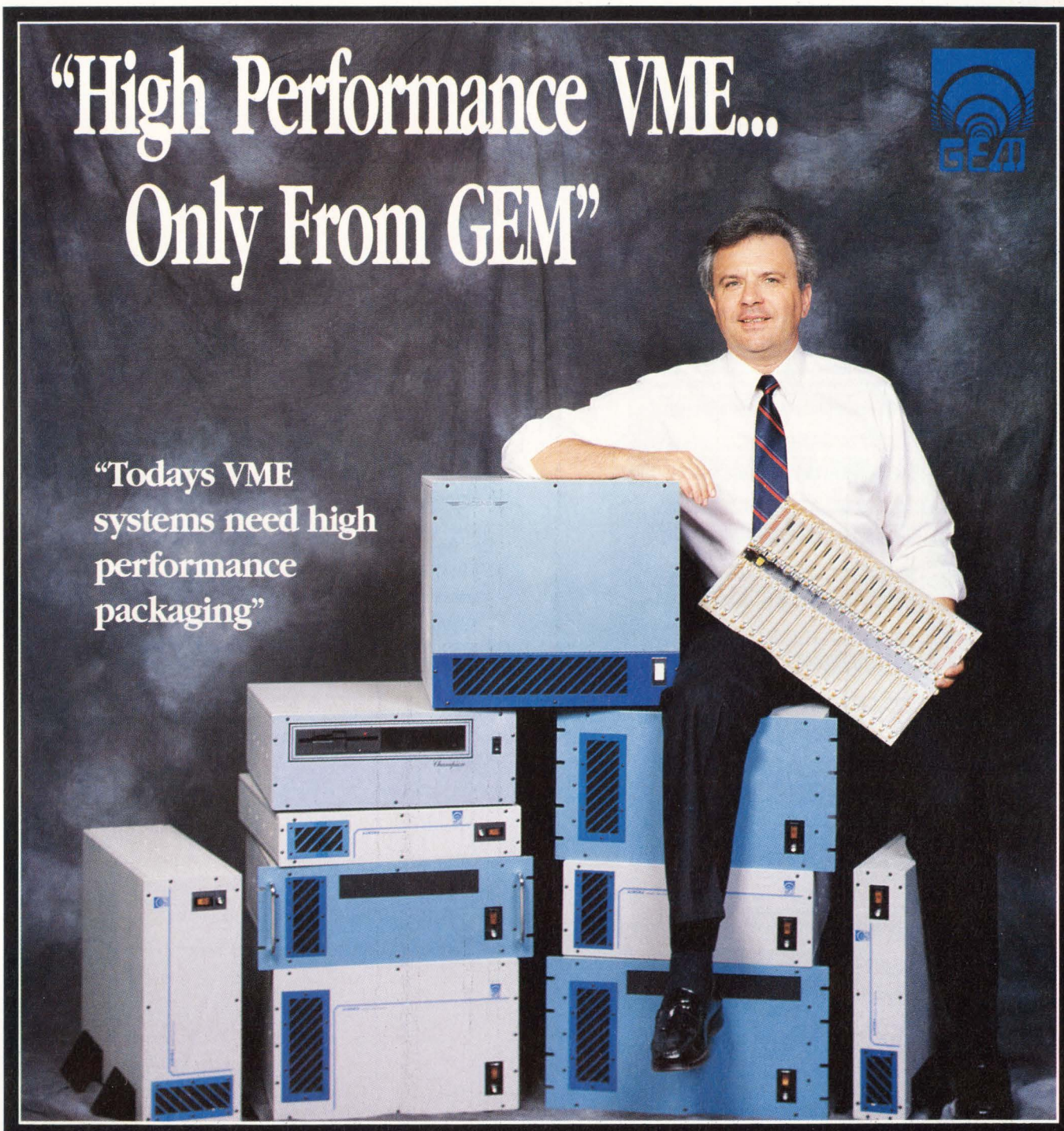

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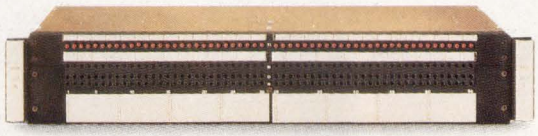

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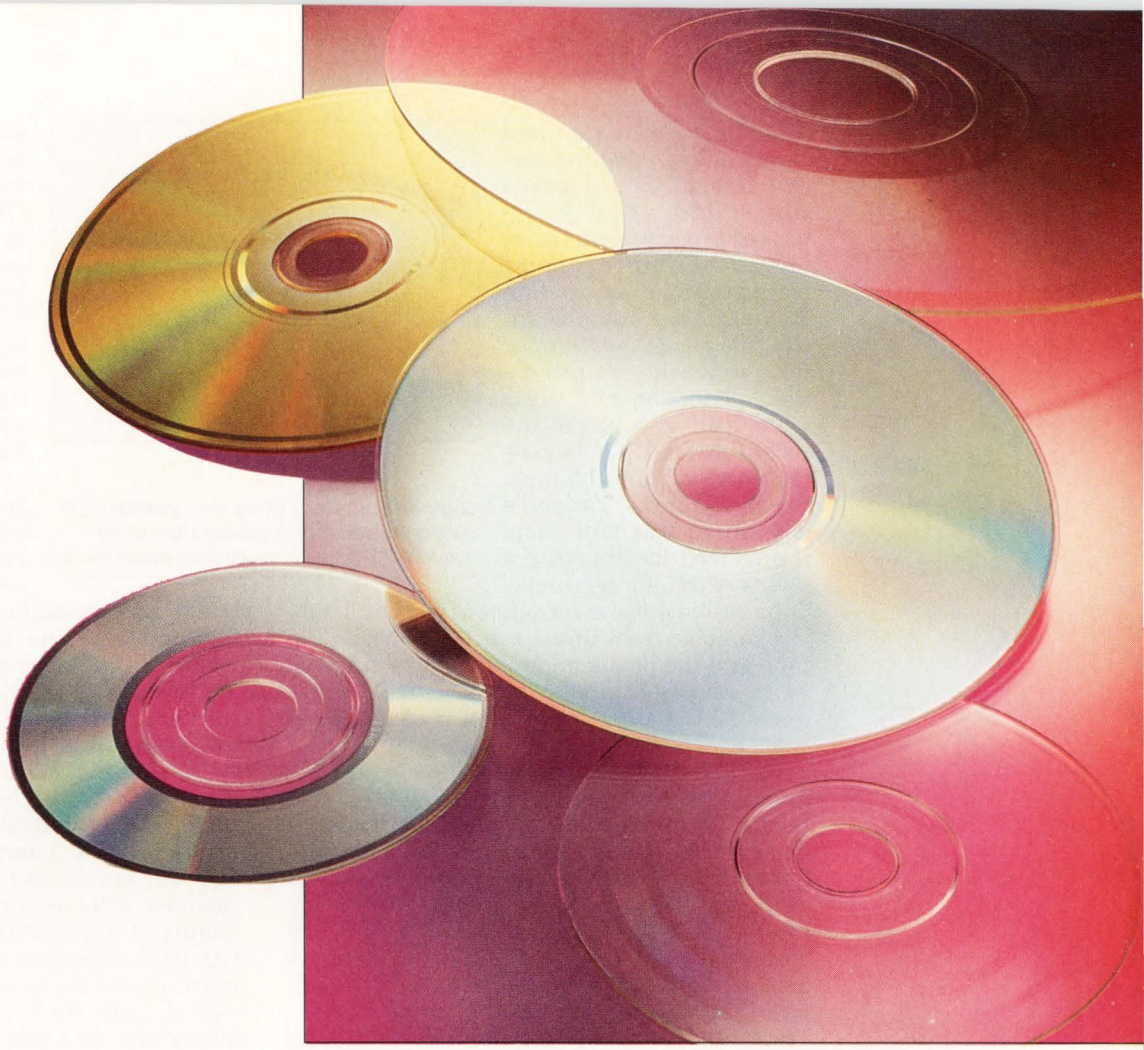


Digital designs conquer consumer music and video

A smile spread across the audiophile's face as the recorded sounds of a train wreck thundered from his speakers. In the room, a reel-to-reel tape deck turned slowly, and two metal boxes—pre-amp and power amplifier—suffused the room with a soft glow from their vacuum tubes. It was 1960, and audiophiles (along with ham radio operators) were the electronic hackers of the day. But unlike ham radio operators, audiophiles pointed the way to a potentially vast consumer market of music lovers ready for high fidelity and stereo sound if it could be packaged and priced attractively. How could the audiophile, who was pushing the technology edge of 1960, have guessed what the combination of a mass consumer market, solid state technology and, ultimately, the microprocessor would do for the quality and availability of recorded music?

Solid state technology has opened convenient, low-cost, high-quality sound systems to a mass market and has provided the basis for the next stage of evolution: digital sound made possible by microprocessor technology.

In the 1960s and '70s, serious shoppers for hi-fi and stereo equipment wrestled with specs such as frequency response curves, turntable rumble, wow and flutter, tape hiss, etc. But the specs of magnetic cartridges don't have a counterpart in laser compact discs, and digital audio tape takes away most of the fretting over hiss and frequency response in that playback system.

By 1980, the engineering in playback systems, primarily turntables and cassette decks, had reached a level that could bring the listener truly exquisite sound, or so it seemed at the time. Magnetic cartridges had been refined; tone arms with ultralight tracking

The compact disc embodies the digital transformation of consumer electronics. Combining superb sound quality and compact size, CDs have virtually replaced the LP as the leading distribution medium for recorded music.

weights were in use; and Dolby noise reduction and the use of metal oxide tapes had greatly improved taped sound. Increments of improvement were getting ever smaller. But no matter how elegant the playback system or how true the amplification, distortion and noise were still results of the recording and playback—the vinyl LP and the tape. Since Thomas Edison's day, music was still being reproduced by dragging a stylus through a groove. Tape systems, however refined, were still subject to noise from direct contact between the tape and the heads and to distortion through wear. Analog tape also has practical limitations in dynamic range and frequency response.

Digital technology gives this portable CD player better sound quality than older analog "hi-fi" systems costing much more.

In 1980, Sony chairman Akio Morita, Philips director of audio Joop van Tilburg, and Berlin Philharmonic conductor Herbert von Karajan held a joint press conference in Eindhoven, the Netherlands to announce support of a new recording technology pioneered by Philips and developed under a technology transfer agreement with Sony: the compact disc. By 1983 hundreds of thousands of compact disc players were coming on the market. Today, the compact disc has almost totally replaced the LP as the preferred distribution medium for recorded music.

The compact disc represented something entirely new in recorded music. It was digital. The analog music signal is sampled as 44.1 thousand 32-bit (16-bits per channel) samples per second, and combined with a sophisticated Reed-Solomon error correcting code. The music, represented as tiny dimples that stand for 1s and 0s, is stamped onto the surface of the compact disc. The solid state laser that reads the information never physically touches the surface, so there's no wear and none of the noise or distortion that tiny surface irregularities can produce in LPs. What's more, there's no loss of signal dynamics. LP recording engineers routinely reduce the dynamic range of program material by tens of dBs in order to keep the record's grooves narrow (higher levels require wider grooves and more spacing between grooves, and allow less recording per album side). Digital recording using 16-bit conversion can capture the full dynamic range of program material (in excess of 90 dB). Thus the data on a CD contains every bit of music information recorded on the digital master tape.

The widespread—almost universal—triumph of the compact disc has set a standard of consumer expectation that's influencing other areas. Many proposals for advanced television include the call for CD quality sound. Recently, Eastman Kodak and Optical Radiation, both based in Rochester, NY, have come up with a digital system for movie sound called Cinema Digital Sound. Instead of analog signals, optical digital dots are placed on the sound track of film. The recent film *Dick Tracy* was recorded digitally and shown with digital sound in theaters that had digital sound heads for their projectors. So digital movie sound doesn't require wholesale replacement of projection equipment; existing projectors can simply be retrofitted. The new generation of video discs include digital CD quality sound as well.

The one drawback of the compact disc, depending on whether you're a consumer or the recording industry, is that like the LP before it, it can't record. Of course, one can copy CD music onto standard cassettes, but then one will end up with the inferior sound quality of the cassette. To preserve the true CD level of sound quality, music on tape must also be recorded as digital data. Enter digital audio tape (DAT). The recording industry has been using DAT for some time in high-end multi-track recorders and mastering systems, but only recently, and only in 1990 in the United States, has it been available as a consumer product. DAT manufacturers hope that compact discs and DAT will co-exist in the market in much the same way as did the LP and the cassette tape.

DAT uses a type of metal tape that has a longer shelf life, better structural integrity and higher recording density than standard metal or oxide cassette tapes. The DAT drive uses a rotary recording head similar to that of a VCR spinning at 2,000 rpm. Data is written onto the tape in diagonal strips at a sampling rate of 48 kHz—faster than that of compact discs. Extensive error correction, with about twice the error correcting capability of compact discs, allows the system to re-create lost data on playback and to mute out noise that may result from any irretrievable data.

Along with the music and error correction data, both DAT recording and compact discs contain special subcode information that lets the deck automatically center information tracks on the head. The subcode timing and location data also lets DAT deck manufacturers add programming and search features, among others. Since the subcode information is recorded separately from the music, it can be edited without affecting the sound.

In addition to the standard PLAY, FAST

FORWARD, STOP, and REWIND features of cassettes, a DAT deck could offer Start ID, to mark the start of each section for search/scan; Skip ID, to program around selections one doesn't want to hear; and Renumber, to renumber all selections from the start of the tape. It's also possible to display absolute time either from the start of the tape or from the start of a current selection, which is useful for recording purposes.

DAT's ability to directly record the digital information either from a compact disc or from another digital tape has frightened the recording industry and delayed the introduction of DAT into the United States. But the possibilities for digitized music information plus the attractiveness of the sound quality will no doubt overcome such resistance. Sony has introduced a digital audio deck as well as a DAT version of its successful Walkman personal stereo to the U.S. market, and other manufacturers are expected to follow suit.

In recording from compact disc to digital tape, the digital data is taken off the CD player just before it's sent to the Digital-to-Analog converters. The CD has performed its error correction and properly reordered the music samples. The DAT deck then can compensate for the difference in sampling rates and apply its own error correction scheme and formatting to the data before writing it to the tape. More models of CD players are appearing with digital output jacks to let users get to the digital data, not merely for recording, but also for other uses such as musical instrument device interface control and sound field processing using digital signal processor technology.

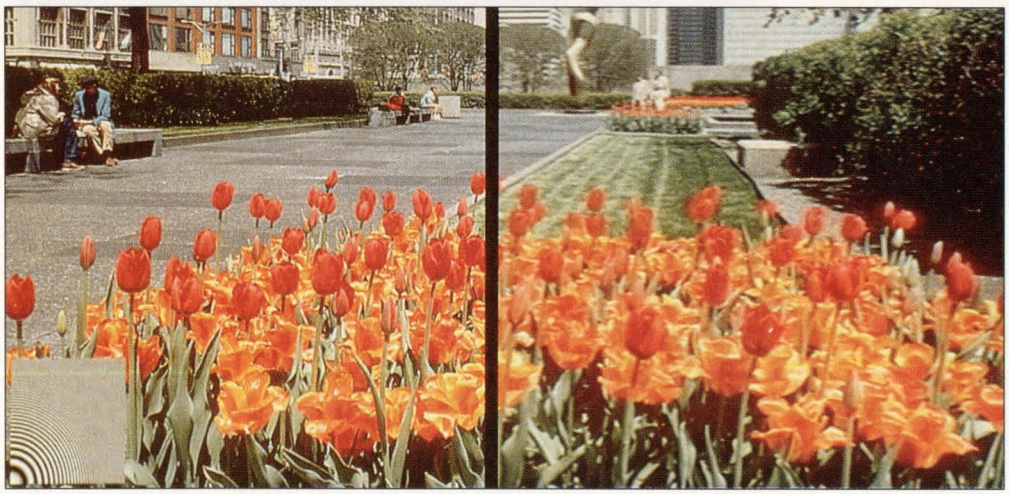
Having an audio signal in digital form not only preserves a level of sound quality, but it allows precise digital processing and manipulation of the audio data. The ability of modern DSPs to select bands of frequency from a signal and manipulate them digitally makes them excellent audio filters—with abilities beyond those possible with analog filters (such as zero phase shift). With digital analysis and processing it's even theoretically possible to isolate and remove the sound of a single violin in a recorded orchestra.

DSP has been used to enhance digitized rerecordings of older LPs such as jazz greats of the 1920s. Sound engineers have removed noise and scratches with selective filtering and have enhanced certain frequency bands that didn't reproduce well in the old medium, giving old recordings new life.

While the most obvious use of DSP in digital audio systems is filtering and digital equalization because of its ability to reshape the spectrum of a signal, DSP can also operate in the time domain, making it possible to insert time delays for given parts of a signal spectrum. This ability has led to an interesting application of signal processing for home and car audio systems. Los Angeles, CA-based Pioneer last year introduced a sound field processor that uses DSP to simulate the sound experience of various listening environments such as a concert hall, jazz club, disco, or church. Several other brands such as JVC and THX have incorporated DSP sound processing into audio amplifiers. The THX system by Lucasfilm is specifically oriented toward processing movie sound from Pioneer's Laserdiscs to re-create the sound experience of a large cinema within the confines of a home viewing room.

One might be tempted to say that the compact disc "started it all" when looking at what appears to be a reemergence of video disc technology that once seemed to have been permanently eclipsed by video tape. Actually, the compact audio disc came out of a project at Philips that was originally aimed at recording video signals. The first video discs were not a hit with viewers because the drives used constant linear velocity (CLV). CLV meant that the inner tracks contained the same amount of information as the outer tracks because the disc spun at a constant rate. Thus the viewer had to turn over a one-hour disc after 30 minutes.

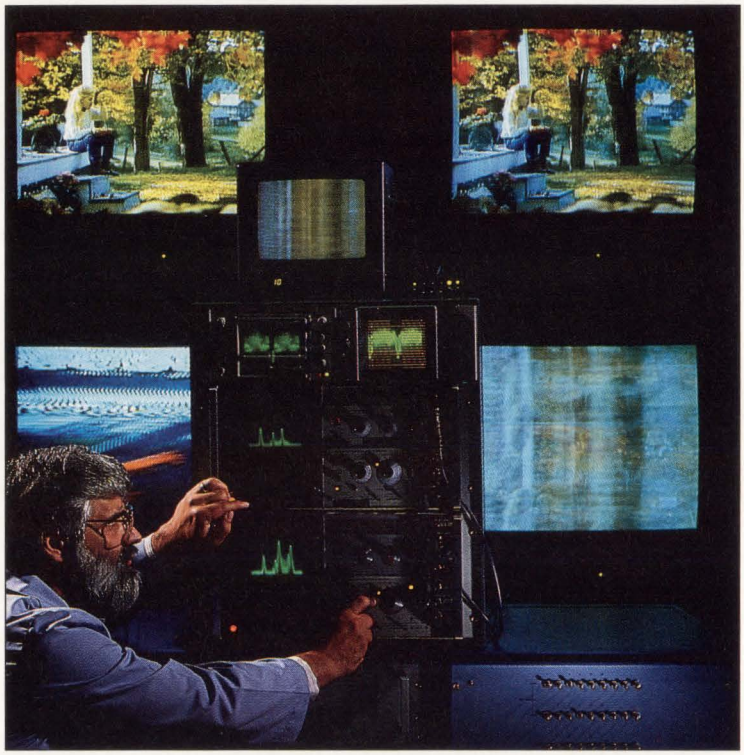
Today's constant angular velocity (CAV) drives slow down the motor speed as the beam moves from the center outward so that the outer tracks can hold much more information than the inner ones, resulting in a much longer-playing disc. Video discs, represented by the Pioneer Laserdisc, appear to be



The FCC is expected to select a U.S. standard for high-definition television broadcasting in early 1993. The higher image quality of HDTV will be teamed with CD-quality audio. HDTV's 24-30-MHz video bandwidth requirements are being matched to existing 6-MHz television channels through digital compression techniques.

poised for a comeback against the VCR thanks to their better picture quality and their ability to be used in interactive applications. In addition to improvements in disc capacity, digital processing of the video signal—which is recorded on the disc in analog form—and improvements in optical systems and stability have produced a noticeably better quality picture than is available from tape. Teaming CD-quality digital sound with the video disc is also expected to lure audio- and videophiles away from tape.

In fact, the optical disc appears on its way to victory as a medium for recorded entertainment in general. Combination players that can play video and compact audio discs are available from several manufacturers, and producers are putting an increasing number of movie titles on video discs. The discs' widespread acceptance by rental outlets will be the key to a switch among viewers to disc-based recorded video entertainment.



Current proposals call for HDTV and standard TV signals to broadcast on separate channels. Researchers at Zenith have demonstrated that even closely spaced channels need not experience interference.

Back in the early 1960s, television was undergoing its first major evolutionary change: the conversion to color. Back when only a few programs were broadcast in color, the novelty would send families with color sets rushing from the dinner table into the living room to watch the NBC peacock spread its tailfeathers across the screen. At the same time, broadcasters also underwent a major upgrade of their transmitter equipment.

One major consideration in the choice of technology for the switch to color TV was the Federal Communications Commission (FCC) stipulation that the color broadcast signal be compatible with existing black-and-white transmission so as not to obsolete the millions of black-and-white receivers already in homes. A similar situation exists with the second impending evolutionary change in broadcast TV: the move to high-definition television. HDTV, as the name implies, aims at a higher resolution picture than the 40-year-old National Television System Committee (NTSC) standard with its 525 scanning lines. It also holds the promise of broadcasting CD-quality sound.

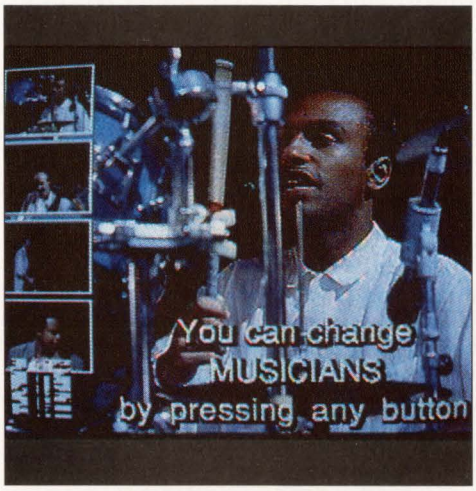
There's a plethora of proposals for how to implement advanced television systems with higher resolution. The proposals range from improved NTSC to full-blown digital broadcasting. Some of these are regarded as only interim steps to full high-definition viewing. At the moment, some order appears to be coming out of the chaos, and about six proposals are serious candidates. In addition to considerations of basic technology, there are questions of allocating channel bandwidth and accommodating different delivery methods including terrestrial broadcasting, satellite and cable. Despite the present apparent confusion, the HDTV Information Center of the Electronic Industry Association is confidently predicting that HDTV will penetrate 25 percent of U.S. households by the end of the century and that Americans will purchase HDTV sets faster than they did for either conventional color TVs or VCRs.

There's a popular myth that the United States is lagging Japan and Europe in the development of HDTV—an idea that is disputed by Sidney Topel, chairman of the EIA's Advanced Television Committee. Other countries, especially in Europe, are still in a confused state with many conflicting proposals as well, Topel says. "I didn't find any unified, advanced program (in Europe)," he says. "I did find a little pushing on the part of TV set manufacturers who would like to build bigger TV sets. What people really want is programs. They want a lot of programs, and that's what you can get with low-power satellites feeding cable systems as we have done in the United States."

A proposal by General Instrument (San

Diego, CA) to the FCC that's recently gained attention seeks the implementation of a fully digital system in the United States. The proposal calls for all-digital technology using video compression. "I'd say that's what's really new and that's where the United States is probably in the leadership position," says Topel. The intent to submit a second all-digital system for testing came last November from a consortium comprising David Sarnoff Laboratories, National Broadcasting Company, North American Philips, and Thomson.

Of course, an all-digital technology would not be compatible with NTSC. The real problem with digital TV is that it will require enormous bandwidth in order to take a high-definition television signal and get the right sampling rate for the high frequencies, and then the right number of bits—a matter of tens of megabits, maybe a hundred or so—to get the quality. Lately, there have been people who think they can get very, very high compression ratios to fit high-definition digital television into the 6 MHz bandwidth channel required by the FCC. "I think if we go forward on video compression technology, we can leave both the Japanese and the Europeans at the gate," Topel says.



Interactive television lets viewers participate in programs such as sporting events or game shows. In this system from ACTV, watchers can choose from any of four camera views.

Regarding compatibility with NTSC, Topel points out that the FCC didn't say that the same signal must carry both standards (as is the case with color broadcasting). It said people must be able to receive the same program at home, whichever type set they're using. By taking a simulcast approach—broadcasting the two standards on two different frequencies—the industry could satisfy the FCC's requirement and not compromise the technology. That, of course, would mean assigning two 6 MHz bandwidth channels to each broadcaster who wanted to broadcast HDTV along with NTSC. Having each television station require two clear channels for broadcasting may double the demand for channel assignments. According to the EIA's George Hanover, it might not mean doubling, but assigning some of the frequencies that were difficult to use and that few people wanted because of interference. The potential for increased interference in a more crowded spectrum is one issue to be addressed in testing HDTV methods by spectrum for terrestrial television. Broadcasters on those channels could use another advantage of digital electronics—error correction.

Whether or when digitally encoded video signals become the mainstream form of television broadcasting may not even be the most revolutionary aspect of the microprocessor's impact on the medium. Digital technology is opening the door to interactive television where viewers not only watch but also participate in the programming.

Interactive television is not a radically new idea. A children's show in the 1950s called "Winky Dink and You" sold a transparent screen overlay and a grease pencil for kids to use to solve puzzles and connect-the-dots as they were shown on the show to participate in Winky Dink's adventures.

In the early 1980s there was a flurry of efforts to harness cable television networks into a home information system. Called Videotex in the United States and Prestel in the United Kingdom, these systems gave viewers access to information services for weather, news, shopping, and other services such as airline reservations. Videotex failed largely because it was asking people to use their TVs—which are means of entertainment—as computers. The systems were not easy to use; one had to step through many levels of tedious menus, the graphics were low-resolution compared to a television picture and the system got in the way of a viewer's primary motivation for using a television—to be entertained.

Now a new generation of interactive TV is taking shape around more advanced technologies and a realization that to be successful, interactive TV must take advantage of people's desire to be entertained. One such scheme that's close to entering the mass market has been devised by Interactive Network in Mountain View, CA. Subscribers to Interactive Network's system can participate in TV game shows such as "Jeopardy" and "Wheel of Fortune," or play games with sporting events such as major league baseball, football or basketball. In the QB1 football game, for instance, viewers can guess what kind of play the offense will try next.

The system uses a small terminal that contains a concealable alphanumeric keyboard, microprocessor and memory, and an LCD display surrounded by eight buttons that can be defined by on-screen menus. The unit contains an FM subcarrier receiver and

an internal modem. Programs and data—even the operating system—are downloaded to the control terminal over the air.

The data is encoded on an FM subcarrier leased by Interactive Network for a given broadcast area. It's simulcast in synch with the regular TV broadcast. Alternatively, the data can be encoded in the vertical blanking interval (VBI) of the video signal. If this is done at the level of the network feed, then all affiliate stations can automatically carry the programming. For program data encoded in the video signal, the subscriber needs a booster, a box that extracts the data from the broadcast signal and sends it into the room as infrared light that's picked up by a sensor in the control terminal.

In our football example, viewers would have until the ball is snapped to make their choices. They can watch the formation and draw conclusions from how the players are lining up on the field as well as from their own strategic ideas. When the ball is snapped, Interactive Network sends a lockout signal preventing any further entry. An operator watching the game at the Interactive Network headquarters clicks on a menu in a program that encodes data to send out telling what play really happened. The program in the control terminal then tells the viewer if the guess was right and assigns a score.

Once viewers have finished playing, they can plug the unit's modem into their telephone line and send in their scores. Scores are stored in Interactive Network's central computer and used in a system of prize awards. The incentive for broadcasters to cooperate with companies like Interactive Network is simple: ratings. Studies have shown dramatic increases in viewers when the programs are interactive.

A somewhat different approach to interactive TV is that taken by Beaverton, OR-based Interactive Systems with its video encoded invisible light (VEIL) system. VEIL uses the actual picture frame portion of the TV signal to transmit information rather than the VBI, which can be inadvertently blocked and replaced by local station equipment, thus losing the encoding placed in a network feed. Digital information is encoded in the luminance component of the video signal in such a way that it can't be detected by the eye, but can be detected by a high-speed photodiode.

The data encoded in the luminance signal can be information and can be used to activate other functions in products used with the system. French television, for example, is currently running a children's program called "Saber Rider and the Star Sheriffs" that works with a toy distributed by Ideal Loisirs of France. The toy contains a photodetector and a microprocessor that responds to signals encoded with the program so that viewers can play along with the action on the screen.

The VEIL technology makes it possible to design a wide variety of interactive products that can be used with encoded programming. An electronic keyboard, for example, could be designed to receive the signals and light up keys or cords so that the viewer could learn to play along with broadcast music. For education, "electronic notebooks" could receive information from a teacher's desk. The data could be used for homework exercises, exams, etc., and even to take attendance. Students would interact with the data and program in the notebook, then use its built-in modem to send in their work.

Inreactive Systems is also developing a unit for consumer marketing that will sit on top of the set and let viewers interact by means of a handheld remote unit. The unit will contain a single-line display and a small thermal printer. One possible application will be for the unit to read the signal during a commercial and display something like "Discount coupon available" or "Available for purchase." Viewers could then signal their acceptance of the sale; the unit would dial up and send in credit card information already stored in the unit when it saw that the phone line was available, and then print a receipt.

Yet another form of interactive television, developed by ACTV in New York, NY, lets viewers customize the program they're viewing. Viewers of a sporting event, for instance, can choose between, say, a wide shot or a closeup of the action, or a different camera angle, or they may even call up the score to be displayed on the screen. The ACTV system is entirely one-way and does not allow the viewer to send back any information.

Under the current implementation, four frames representing, for example, either four camera shots, four levels of an exercise program, or perhaps four different musicians in a music program, are sent simultaneously over a 24 MHz-wide cable channel. The viewer can program the local converter box with a handheld unit to demultiplex the frames as desired. The results appear seamless to the viewer because they occur at the actual frame rate. ACTV is pursuing video compression techniques to try to compress the four signals to fit within a 6 MHz channel so that it can expand to wider commercial markets including broadcast in addition to cable delivery.

The future of television is being influenced by digital electronics that go far beyond merely digitizing the broadcast video signal. The ability to custom program viewing, interact with entertainment programs and—above all—to increase consumer purchasing via the media will open vast new markets and creative uses of the technology as the 21st century opens.

By Tom Williams, Senior Editor

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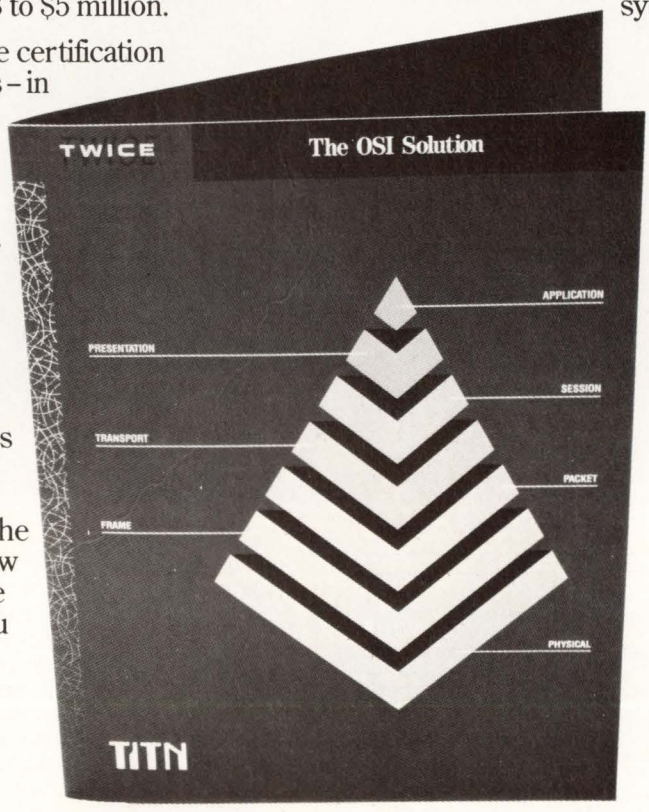

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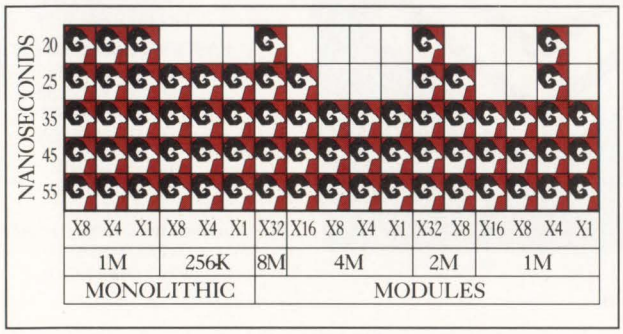

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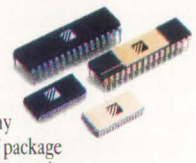

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CIRCLE NO. 45

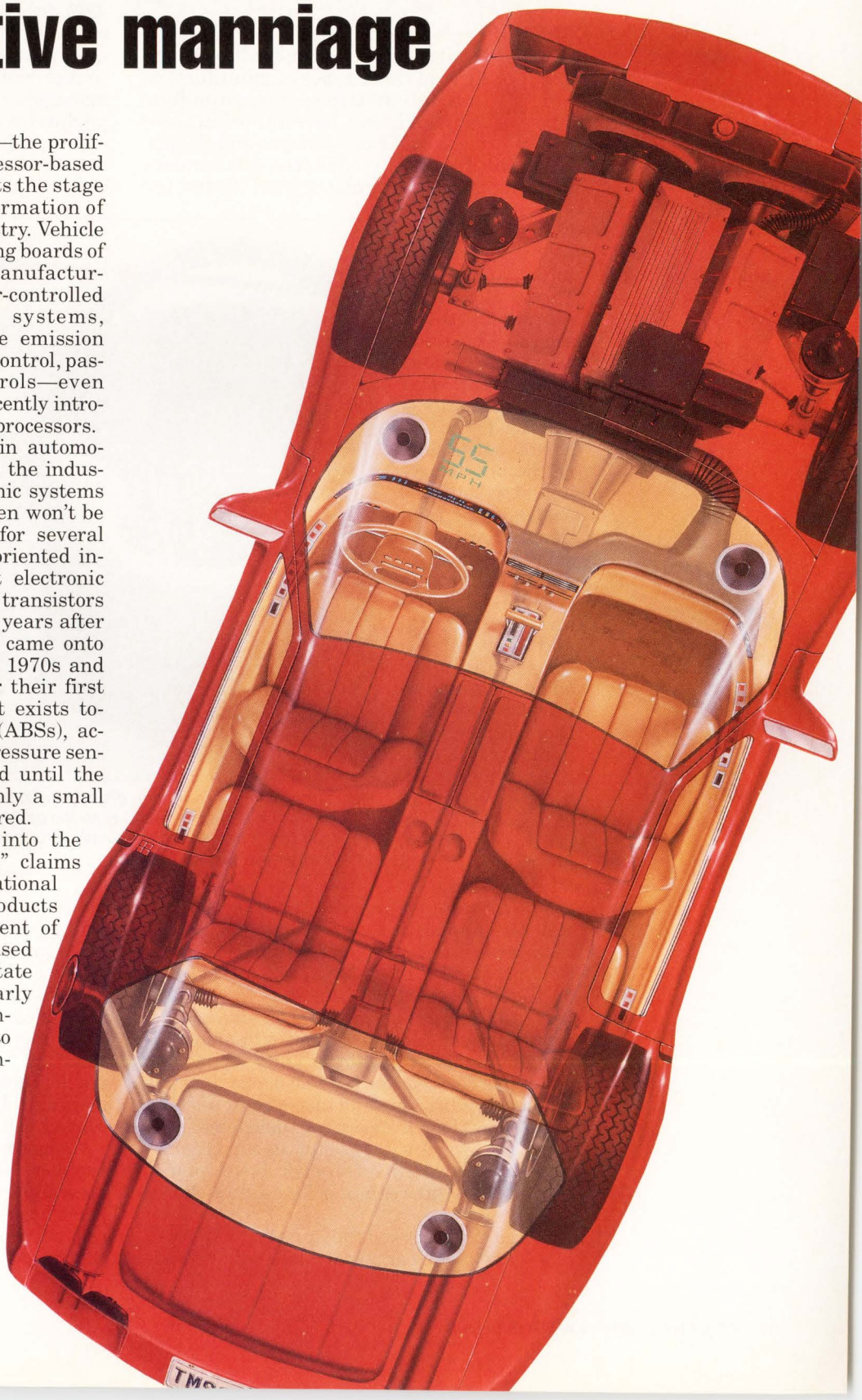
Automobiles and electronics: a long courtship promises a productive marriage

The digital revolution—the proliferation of microprocessor-based control systems—sets the stage for a radical transformation of the automotive industry. Vehicle designs on the drawing boards of major automobile manufacturers include computer-controlled air bag inflation systems, microprocessor-controlled engine emission systems, electronic transmission control, passenger seat and climate controls—even driver alertness warnings. One recently introduced sedan has no less than 34 processors.

Yet the history of electronics in automobiles should be examined closely: the industry's outward embrace of electronic systems has created expectations that often won't be fully realized in new products for several generations. This mechanically oriented industry has been slow to accept electronic technology. The automotive use of transistors didn't occur until 1967—a full 20 years after their invention. Microprocessors came onto the automotive scene in the late 1970s and early '80s, almost a decade after their first commercial use. Technology that exists today—anti-lock braking systems (ABSs), active suspensions, electronic tire pressure sensors—won't be fully implemented until the year 2000, and even then, on only a small proportion of the cars manufactured.

"Auto makers were dragged into the electronics business grudgingly," claims Paul Standish, former head of National Semiconductor's automotive products marketing, and now vice-president of applications at San Jose, CA-based Micro Linear. The federal and state emissions standards—particularly California's—were the largest single factor that pushed them into the business, according to Standish. "In the early '60s," he says, "auto designers began to realize that they weren't going to be able to meet the standards if they kept using conventional mechanical techniques."

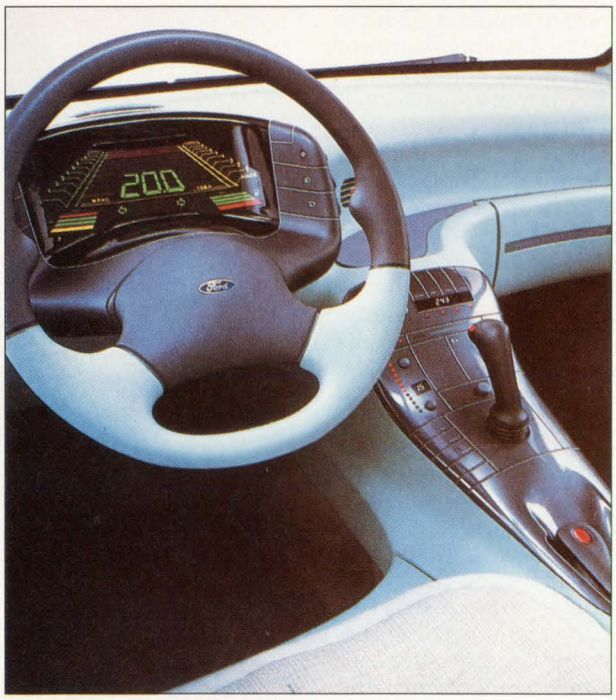
As engine control circuitry began to emerge, auto designers—perhaps pushed by the semicon-



ductor makers—began looking at other ways electronics could be used to enhance a vehicle's safety, reliability and, most of all, market acceptance. The entertainment, climate control and dash panels were among the first to benefit from electronics. It's only now that auto makers are examining all parts of the vehicle to determine which can be replaced or enhanced by electronic systems.

Developments in automotive electronics can be attributed to the efforts of three types of manufacturers: automotive system suppliers such as Bosch Electronics in Germany and Kelsey-Hayes and Bendix Electronics in the United States; semiconductor companies, particularly Intel, Texas Instruments, National Semiconductor and Motorola; and the Big Three U.S. auto companies themselves. (The European auto makers actually followed the leadership of the Big Three.)

Not surprisingly, the automotive industry has had a "lead-lag" relationship with the semiconductor industry, alternately resisting the analog-to-digital and microprocessor systems offered by the semiconductor vendors, then suddenly demanding state-of-the-art digital signal processing chips, 32-bit controllers and on-board EEPROM for everything.



The sophisticated information displays found in today's concept cars bring digital technology to the dashboard. Displays are being developed to provide information beyond simple engine status and speed.

The first automotive use of a silicon device was the application of high-current silicon rectifiers to the output of alternators. "The first production units to hit the street were on the 1959 and 1960 Chryslers," says Jack Morgan, one of the pioneers in automotive electronics at Motorola, now vice-president and automotive director at VLSI Technology in Tempe, AZ. Outside of some transistors put in hybrid radios, it would take almost another seven years for the next major development—the first use of a transistor in an automobile—to occur. This Chrysler development was a solid-state regulator for battery-charging current.

While 1967 marked the first production use of a transistor in an automobile, other developments were already in the planning stage. "There was a lot of work going on at Bendix throughout the '60s, though much of it never saw the light of day," says Jerry Rivard, president of Birmingham, MI-based Global Technology and Business Development, and former president of Bendix and later general manager of Ford Motor's electronics division. There was considerable work done on an ABS, for example, as well as on total engine control and fuel injection. But Rivard suggests that early designers of automotive electronics had a difficult time convincing their managers to implement these systems in a production vehicle; Detroit believed that any addition of electronics would be more costly than traditional mechanical systems.

In the mid-'60s, the idea of electronic ignition became popular, yet such a system didn't go into production until almost a decade later. "At the time, emissions and pollution legislation was just starting to hit the books," says VLSI Technology's Morgan. "Both federal laws and California legislation sent car makers back to their labs trying to find solutions."

"The first ignition modules to reach any commercial production were in the late '60s," says Micro Linear's Standish. "However, in the early versions, they did little more than simply replace the points and capacitor in the distributor. Magnetic pickup coils, and in some cases optical sensors, simply replaced the old-fashioned breaker points."

The early to mid '70s saw a lot of activity behind the scenes, but little commercial introduction. Even as emission standards became more stringent, auto designers were reluctant to jump into any type of electronic engine control. Instead, they looked to other mechanical systems such as air pumps to control pollution, says Morgan.

"Sometime in the early '70s, semiconductor suppliers started to recognize some of the special needs of the automotive environment," says Global Technology's Rivard. The first true engine control system, developed by Bendix, saw production in the 1975 model

DSPs make their mark in vehicle control

For vehicular control subsystems, designs based on digital signal processors offer overall system cost reduction and increased speed of response by replacing a microprocessor and its associated lookup table with direct, fast and accurate calculations. DSP-based subsystems can be implemented for vehicular applications in engine and transmission control, suspension control, and anti-lock braking and traction control, among others.

The internal architecture of the DSP allows the device to be programmed to precisely implement sophisticated algorithms. For the vehicle control subsystem designer this means that the DSP can best implement the proportional-integral-derivative, deadbeat, observer, adaptive control (both self-tuning regulators and model reference adaptive controllers), lead-lag and other algorithms.

The DSP's signal sampling rate is high enough to allow subsystems built with it to achieve the continuous (analog-like) but real-time performance that allows optimal control.

The automotive subsystem designer moving to DSP-based technology is learning new skills that allow better system designs. Designers who worked with lookup tables generated by trial-and-error or computer simulations, for example, now fully model their control systems. Lookup tables can't accommodate manufacturing variability, fuel quality, aging, engine wear, cold engines, and the like. Now, with DSPs, designers can use a precise mathematical description of what is being controlled.

The performance, for example, of today's open-loop electronic engine control subsystem can be improved by a DSP- and sensors-based closed-loop system. One set of these sensors is in-cylinder pressure sensors. These report the precise operating status of each cylinder at every engine cycle.

With such a sensor system, the control subsystem DSP performs an engine pressure waveform analysis. This analysis determines the best spark timing, optimum spark duration, and the best air-to-fuel ratio. The closed-loop subsystem tolerates age and wear effects while maintaining optimum engine performance and fuel efficiency. Pressure waveform analysis also allows detection and correction for anti-knock operation (by fast Fourier transform analysis) and monitoring for power train diagnosis.

Another example of what can now be done with vehicle control is the active suspension system. Conventional suspension systems, based on dampers and springs, can't respond to rapidly changing forces caused by changing road conditions and car attitude changes. Newer systems that use 8-bit microcontrollers to allow variable damping ratios in the dampers are better, although they have slow system response times and can't completely solve the external forces input problem.

DSPs make it possible to implement a fully active vehicle suspension. One example of such a design is the active suspension designed by sports car manufacturer Lotus. Its control subsystem uses four DSPs that control four hydraulic actuators.

The Lotus active suspension subsystem depends on multiple transducer inputs from each wheel. These inputs provide information to the subsystem's analog front-end and its associated analog-to-digital converters. Sensor outputs such as hub displacement, forward velocity, lateral acceleration and body attitude, are digitized by a fast A/D converter. The resulting data are passed to the DSP. With the aid of an on-board vehicle host computer, the DSP provides information to four servo valves controlling hydraulic actuators that determine the position of each wheel. Auto body dynamics such as pitch, roll and heave are accounted for in this active suspension design. And the control algorithms implemented by the DSP have their system parameters adaptively updated.

Another important vehicle control subsystem is anti-skid braking. Currently such subsystems use 8-bit microcontrollers to read each wheel's speed from sensors, calculate the skid, and control the pressure in each wheel's brake cylinders. Newer designs also allow control of wheel spin for optimum vehicle steerability and stability.

In these designs, the DSP performs (for each wheel) speed computation and filtering, wheel speed differentiation, reference computations, slip computations, and real-time diagnostics for fault detection. The end result is shorter braking distances and better vehicle stability and steerability.

In automobile entertainment systems DSPs perform graphics equalization and "surround sound" processing to provide an all-digital, high-fidelity audio entertainment system. In cellular phones, DSPs allow voice recognition of spoken telephone numbers as well as user verification, for safer use by drivers.

Finally, DSPs allow car navigation systems for global positioning. The complex mathematics required for such systems are easily handled by a DSP that performs such chores as Kalman filtering and dead reckoning.

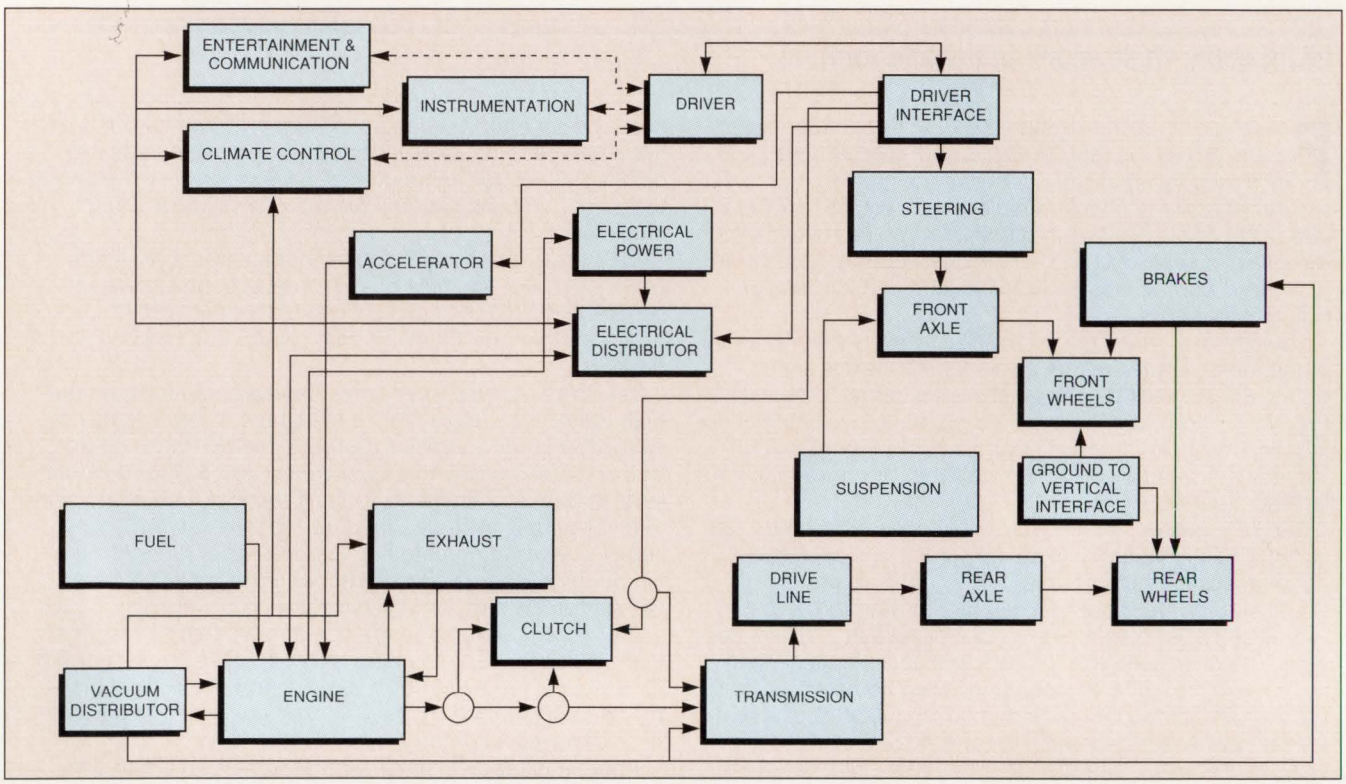
year of General Motors' Cadillac Sevilles.

"This was a major turning point in the industry," says Rivard. "Electronic engine control became a reality virtually overnight. This set the stage for the next two decades."

And Morgan says, "All of a sudden, auto makers became major factors in the electronics market—in that model year, GM made and sold more computers than IBM."

Early clean-burn engine control systems controlled fuel and spark by referencing microprocessor lookup tables for each set of conditions. While this significantly affected performance—and emissions—particularly during the critical first few minutes of operation, it was at best an approximation solution. The real test came when external sensors for oxygen and mass air flow were added to close the loop, letting the computer compensate for actual measured conditions, rather than anticipated conditions.

While GM had the lead, the other major Detroit auto makers weren't far behind. In 1977, Ford introduced its first electronic engine control system, EEC 1, which used a proprietary PMOS chip set of nine ICs. This



The current and planned use of digitally controlled systems in automobiles encompasses virtually all parts of the car. Digital controllers let designers increase fuel efficiency, enhance safety and improve comfort. Priorities for new uses of digital control will be set by regulatory and competitive pressures and consumer demand.

system controlled only two functions, exhaust gas recirculation and spark. The 1978 model year saw the EEC 2 using the same technology, but the chip count dropped to five and EEC 2 had more capabilities. The next-generation EEC 3 started appearing on 1979 model year cars and used N-channel MOS, though it still featured a proprietary architecture. The final generation, EEC 4, didn't see production until 1983. By that time, the system used a 16-bit microcontroller, the Intel 8061 (one of two chips in the module). EEC 4 also had more functions and monitored more sensors than the earlier systems.

"The proprietary architecture in the EEC 1, 2 and 3 was tough to program," says Fred Phail, former Ford electronics executive and now strategic marketing manager for the automotive division at Intel (Chandler, AZ). "The auto industry's move to standard-architecture controllers is driven to a large extent by the existence of a standard programming environment."

Early on, perhaps 1978, the first electronic instrumentation began to emerge. But, says Rivard, it was greeted with mixed feelings. Once again driven by federal legislation, work on an ABS began in earnest the following year. The first target application was pickup trucks, since braking ability varies dramatically with the load in the truck. Legislation required the future use of an ABS on all such trucks as a safety precaution.

But despite some dramatic advances, the road from early development to production is a long one for the auto industry. Typically, says Rivard, it takes anywhere from three to five years for technology to get from first prototype stage to final production. And though the electronic content of today's cars is increasing—currently, the average electronic content in a car sold in the United States carries a price tag of about $600—the development period hasn't shrunk. In some cases, it's been extended.

One example, says Rivard, is the air bag—the inflatable passenger protection device. The air bag has had one of the longest gestation periods of any electronic device—more than 20 years. Now, in 1990, a substantial number of vehicles are equipped with the safety device; yet this was first discussed and shown in the late '60s and early '70s.

"Interestingly," says Rivard, "air-bag technology, pioneered and currently provided by Detroit, MI-based TRW, takes a substantial amount of compute power." He explains that the air bag has a number of sensors at many different locations throughout the car. The air-bag computer is constantly sampling these sensors to make certain that they're on-line and working, and that they have or haven't sensed sufficient deceleration/acceleration to warrant inflating the bag.

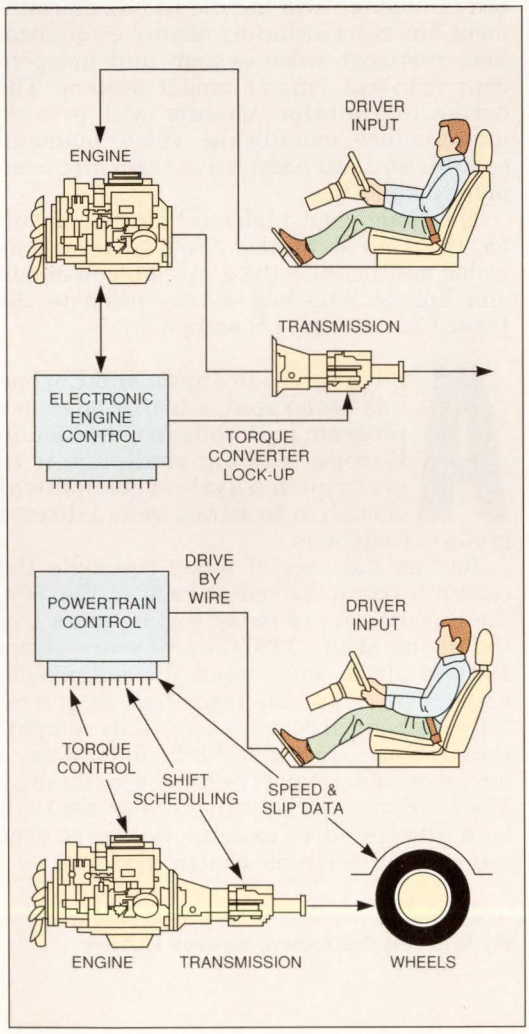
Engine control systems in future automobiles are going to need far more capabilities

to meet emerging emission and efficiency standards. "This new round of legislation will be a major challenge to auto makers," says Rivard. "I suspect the new systems will have to take into account alternate fuels as well as gasoline. And this means that auto makers will have to look at the entire power train—engine, transmission, axles and brakes—as a single entity."

One of the first steps in this direction is electronic transmission control. This move has been pioneered by Chrysler in selected 1989 and 1990 Dodge and Chrysler vehicles. According to the company's literature, the system is the industry's first fully adaptive, electronically controlled four-speed automatic transaxle (combining transmission and differential gearshift functions). The unit provides extremely smooth shifting with less noise, faster response and better fuel economy than conventional mechanical/hydraulic techniques.

Chrysler's adaptive approach uses real-time information from sensors within the transaxle to help determine how to apply the proper hydraulic pressure.

"One of the limiting factors to having the engine controller take over more than simple engine control is the fact that even 16-bit microcontrollers are starting to run out of processing power," says Intel's Phail. Though a microcontroller works incredibly fast compared with the speed of an engine, the lookups and calculations required for engine control are surprisingly complex, and there are a lot of them. Both Ford and GM, however, are reportedly working on 32-bit microcontroller designs for use around 1995 to handle the massive amounts of information and calculations.



Chrysler's adaptive, electronically controlled transaxle integrates control of the transmission and the differential. Future designs will integrate control of all drive train functions and will rely on a 32-bit processor to supply the required computing power.

With the envisioned proliferation of sensors in automobiles, the need to process signals efficiently will become critical. And increasingly, the output from sensors, whether located in a suspension component or combustion chamber, is a complex signal calling for some hefty processing power to make sense of it. Although standard microprocessors are becoming more powerful, they're not tailored to the particular demands of signal processing. DSPs are specifically designed to handle signal-based information efficiently, and current DSP chips boast multiple-Mips performance, with even higher levels promised for next-generation devices. Designers benefit from the dedicated development tools being fielded in support of leading DSP families (see "DSPs make their mark in vehicle control," p 93).

And while Ford and GM plan to use 32-bit controllers to provide higher levels of integration (Chrysler is probably only slightly behind), the same approach hasn't generally been taken by either Japanese or European automobile manufacturers. "Japan in particular has stayed almost a generation behind in auto electronics," says Rivard, who cites Honda as an example. "One of the reasons is the large lag time for getting electronics into new automobiles.

"It takes only three years to turn out a complete new model Honda," he says, "but it takes five years to design next-generation electronics for the same car." As a result, he continues, Japanese car makers have tended to keep systems intact and add additional processors for other functions rather than redesign a given module. Japanese automobiles, therefore, tend to have many discrete components rather than larger, more highly integrated systems. The new Lexus LS 400 luxury sedan from Toyota, for example, sports no less than 34 separate processors. The downside of this approach, says VLSI Tech-

nology's Morgan, is that for a given size, engine power and weight, Japanese automobiles tend to be less fuel efficient than their American counterparts.

There has also been an increased effort to provide more creature comforts for the driver and passengers. These take several different forms, from active suspension to speed control to a digital clock. There are even seat controls capable of remembering particular driver positions—which also automatically adjust mirrors, steering wheel position and radio preset selections to suit.

Display consoles and instrumentation have gone through at least one full iteration and look to be reverting to a more-conventional appearance. The touch-screen CRT introduced in the Buick Riviera in 1986 got some low marks for friendliness, requiring drivers to find sensitive spots on the touch screen to perform all functions, including tuning the radio and adjusting the volume.

Later GM models such as Oldsmobile's Tornado for 1989 include a color CRT with a series of touch buttons along the bottom of the screen so that they can be located by feel and not require drivers to take their eyes off the road.

And, of course, the radio is now an "entertainment center" replete with a digital audio disc player, a specially tuned speaker system that compensates for the shape and acoustic profile of the passenger compartment, full equalization and plenty of power. In addition, the cellular telephone is starting to take its place as original equipment in many high-end models.

Product turnaround in auto electronics is relatively slow. Even after a product achieves acceptance in high-end cars, it takes a long time to filter down to less-expensive models. According to a 1990 estimate, the average electronic content in an automobile sold in the United States is priced at about $600. By 1995, estimates have that price tag jumping to $1,200. And when the year 2000 rolls around that number will probably top $2,000. Where's the money going?

According to a Delphi V forecast released last year by the University of Michigan: 30 percent will have anti-lock brakes by 1995, 70 percent by 2000; 5 percent will have traction control systems by 1995, 15 percent by 2000; 5 percent will have active suspensions by 1995, 10 percent by 2000; 2 percent will have tire pressure sensors by 1995, 8 percent by 2000.

The addition of these systems will undoubtedly make the average cost of cars significantly higher. Add to this the more-sophisticated transmission/engine controller, safety features such as air bags and driver alertness/sobriety warning, and heated windshield, quick-heat system and elaborate climate control, and it all adds up to a costly package.

Rivard sees the car of the next decade with essentially three major computers on board: a vehicle computer handling safety and convenience as well as vehicle controls, a power train computer managing engine and transmission, and a body computer handling audio systems and driver information.

The vehicle computer, says Rivard, will handle a rear-view video system with fog penetration, collision warning system, emergency communication, and road and traffic information. In addition, the vehicle controls part will manage the collision avoidance/automatic braking function, integrated chassis control and suspension, four-wheel steering, and radar adaptive speed control.

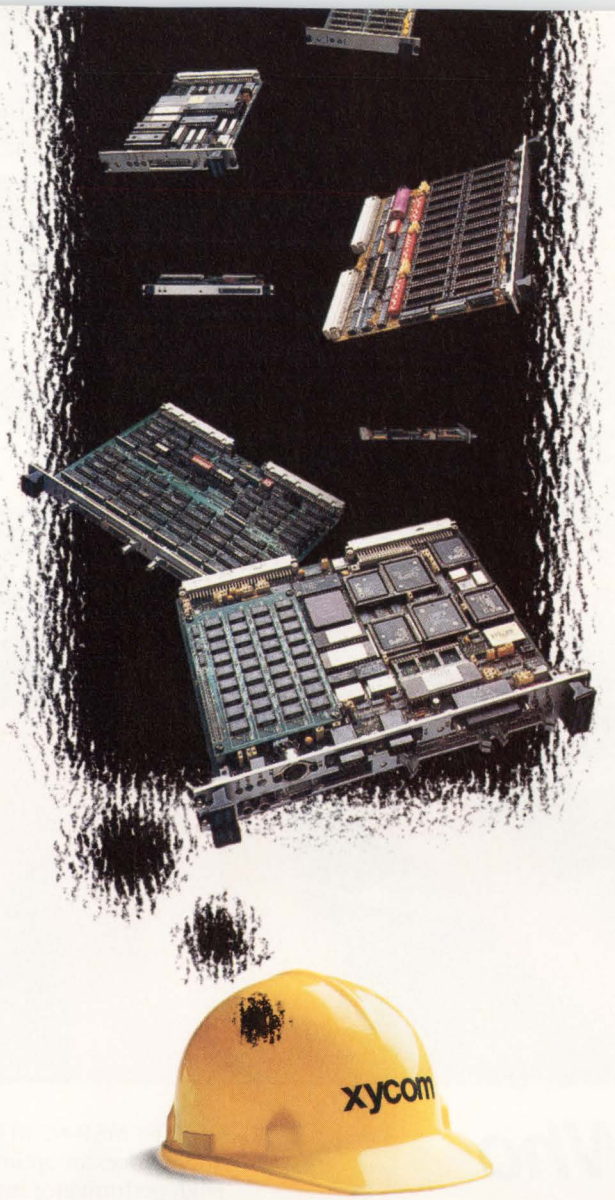
The power train computer will manage such things as total engine control, variable valve timing, engine idle/restart, drive-by-wire electronic throttle control, electronic transmission control, smart sensors, and full drive train diagnostics. The third unit, the body computer, will handle radio/entertainment functions including adaptive equalization, rear-seat video system and independent rear-seat entertainment system. The driver information module will provide maintenance monitoring, voice-command controls and full body, drive train and computer diagnostics.

The "intelligent highway" may be far off for the United States. "Features such as global positioning will be available in Japan and Europe long before they come to the United States," says Standish.

And progress in Japan and Europe has been rapid; a traffic advisory program is already in operation in Europe. The big challenge is to make such a system economical enough to be attractive to a diverse group of customers.

Just as the cars of today resemble the concept cars we looked at back in the '60s, the concept cars of today will be more like the reality of the 2020s. In 30 years—from 1961 to 1991—we've seen the automobile undergo a remarkable transition, from a totally mechanical beast to a partially computerized vehicle. Just as it's difficult for today's drivers to understand the hardships faced by Model T drivers, drivers in the year 2000 will be hard-pressed to imagine how cars ever ran without electronic control systems.

By Warren Andrews, Senior Editor



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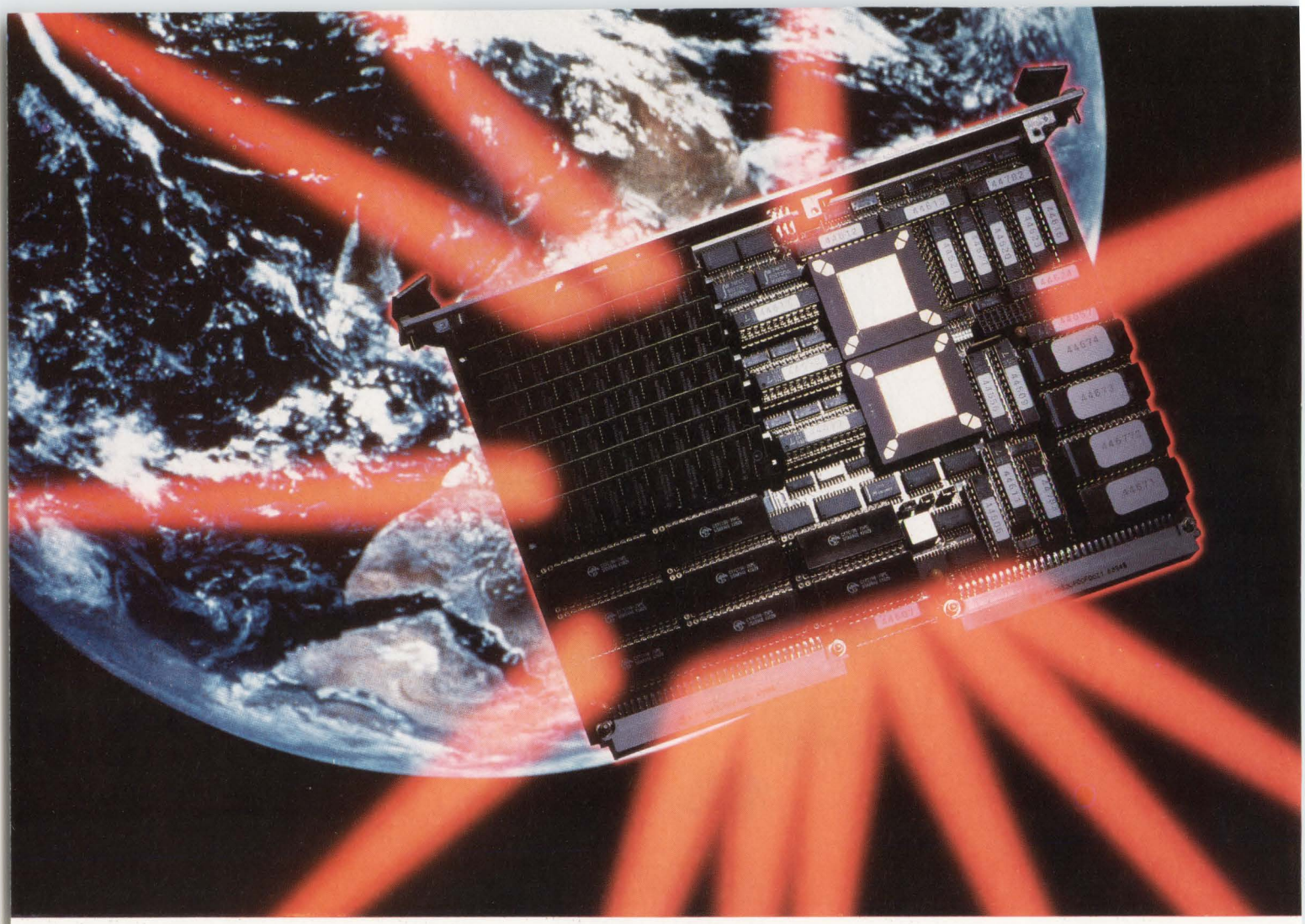

For Those Who Like It HOT

Announcing the MSP-6C30
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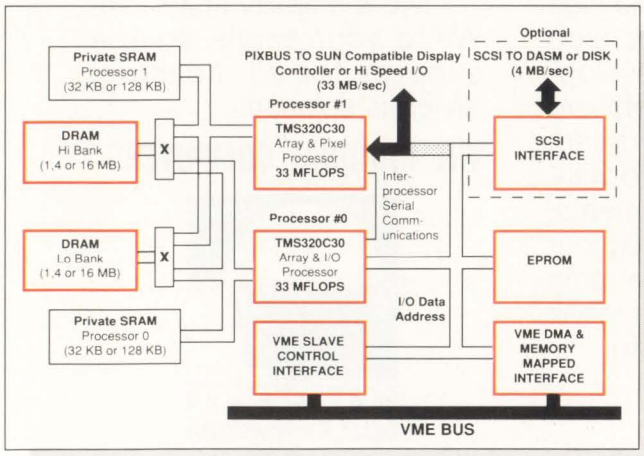

The MSP-6C30 is a 66 MFLOP, floating-point, VME array processor optimized for signal and image processing. High performance is assured through a unique, multi-banked, crossbar memory architecture, and high bandwidth is achieved with multiple, fast, industry standard I/O ports. Also available in a PC-AT version with optional VGA compatible display controller.

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CIRCLE NO. 47

Digitization broadens the scope of measurement and analysis

Analog-to-digital converters, digital displays, ICs, and microprocessors have allowed a digital revolution in instrumentation over the past few decades. An early digital readout called the nixie tube, made by Burroughs, changed forever the face of test and measurement instruments. Prior to the nixie tube, these instruments used an analog moving pointer meter. Engineers had to squint at their instruments to get a good reading. And the accuracy of even the best analog reading was limited.

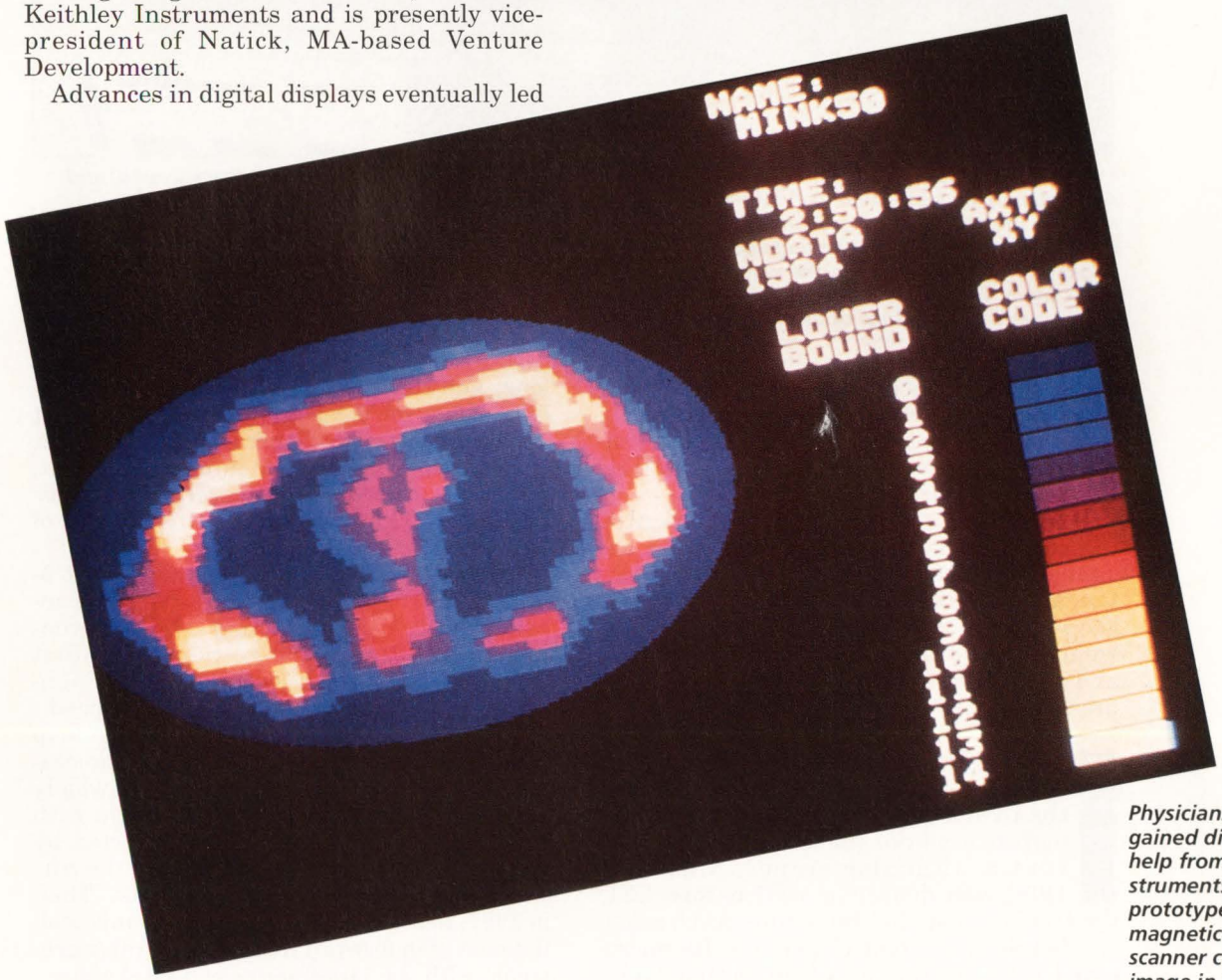
With digital displays, precision increased from 1 percent with an analog pointer to 0.001 percent with a five-digit readout. Customers were dazzled by the digital displays, according to Maurice Klapfish, who then was a design engineer at Cleveland, OH-based Keithley Instruments and is presently vice-president of Natick, MA-based Venture Development.

Advances in digital displays eventually led to the replacement of the nixie tube by LEDs, which were cheaper, easier to read, and less power-hungry. Next came LCDs, cheaper still and requiring even less power.

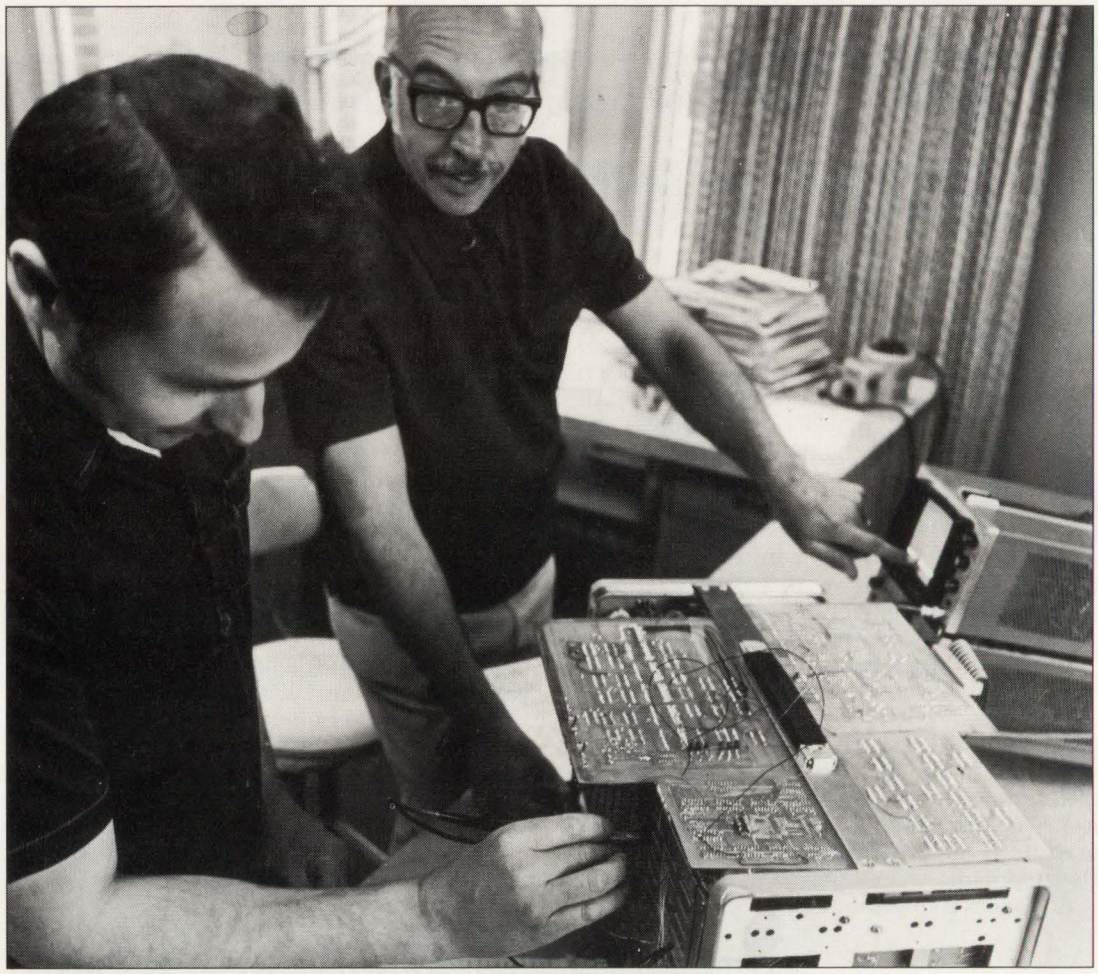
The multimeter is the most widely used instrument in electrical measurements. Its ability to measure voltages, currents and resistances made it an immediate mainstay of engineers and technicians. But the early analog versions were often costly, and required extreme care of operators in taking readings from their analog meters.

John Fluke Manufacturing of Everett, WA introduced its first digital multimeters (DMMs)—the 8100 DMM and the 8300 digital voltmeter—in 1969.

Today's DMMs offer tremendous gains in ease of use, resolution and precision over



Physicians have gained diagnostic help from digital instruments—the prototype nuclear magnetic resonance scanner captured this image in 1977.



The first digital oscilloscope, the 1090A Explorer, is tested by Nicolet's Robert Schulman (background) and Arthur Smith. Its instruction manual stated: "With little doubt, increasing use will be made of digital methods in oscilloscope design in the future, so time spent in understanding this oscilloscope is worthwhile beyond learning the behavior and operation of this particular instrument." The manual goes on to explain: "Unlike conventional scopes, the waveform display shown on the CRT screen is not directly produced by the input signal voltage. The beam is controlled digitally from information previously recorded in memory." Customers were initially suspicious of digitized waveforms.

yesterday's analog meters. Cost and size have also changed dramatically. Big analog benchtop instruments that cost thousands of dollars have been replaced by hand-held DMMs that cost between $50 and $100.

In contrast, microprocessor-based digitizing scopes carry a hefty price tag and are similar in size to analog scopes. But the performance and capabilities of digitizing scopes keep improving. Each new scope seems to be smarter, automates more measurements, and provides more analysis functions than its predecessors.

In 1972, Madison, WI-based Nicolet Instrument introduced the Explorer 1090, the first digital oscilloscope, offering higher resolution and accuracy than conventional analog scopes. Since the 1090 was designed well before LSI, the CPU consisted of numerous ALU, register, counter and multiplexer ICs. Its microcoded program was only 256 instructions long, and its A-D and D-A converters were built of discrete devices and SSI ICs. The first 1090 frames used core memory. Yet even that first model featured alphanumeric readout, computer interface, pretrigger, and longer memory (4,096 12-bit words) than many of today's digital storage scopes.

Different plug-in models of the Nicolet 5-MHz Explorer 1090 offered 12-bit A-D converters at 2 Msamples/s and 8-bit A-D converters at 10 Msamples/s. Since that first model, Nicolet has concentrated on the highest precision rather than the highest speed.

Measurement technology took a great leap forward in the early 1980s when microprocessor-based digitizing scopes became widely available. These "smart" scopes brought with them automatic measurements selected by pushbuttons—a major advance over the cursors and division counting of the past. Then in 1987, Beaverton, OR-based Tektronix took the next step forward in automatic measurements with the 11000 series of digital scopes.

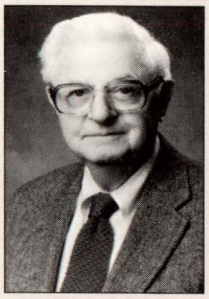
Some things never change

At least one thing hasn't changed in the test and measurement world in the last 40 or so years. That's the presence of Joseph F. Keithley as a prominent industry figure. Keithley founded Keithley Instruments in 1946 and is today chairman of the board. About four and a half decades ago, Keithley rented a shop with a leaky roof on Crawford Road in Cleveland, OH for $8.50 a month. The equipment he relied on at the time included a Hewlett-Packard oscillator and a Ballantine ac voltmeter.

Keithley recalls how his engineers questioned the need for digital technology a few decades ago. "Only the military and big companies with lots of money would buy digital instruments, some said." But Keithley saw things differently, and his first venture into digital instruments was with the nixie-tube-based 440 and 445 picoammeters introduced at an IEEE show in 1969. Next came the 615 digital electrometer, which "didn't operate very well," according to Keithley.

Keithley's acquisition of the rights to the technology in a 3½-digit meter displayed at a trade show in Berlin, Germany led to the introduction of the Model 160 digital multimeter (DMM) and the 163 digital voltmeter in 1970. "The 3½-digit 160 had seven dc voltage ranges from 1 mV full scale to 1,000 V full scale with 100 percent overranging on every range except 1,000 V. The integrator circuitry resided on the analog-to-digital board that slid into the instrument vertically.

The toughest problem that Keithley engineers encountered in designing the 160 was to find a DMM with superior accuracy that could be used as a test standard. The 160 was much more sensitive than what was on the market and sold at about twice the rate we had anticipated," recalls Keithley.



Joseph Keithley, chairman, Keithley Instruments

When asked about his reaction to how digital instruments have evolved, Keithley says, "We never would have dreamed that things would progress as they have. I don't know what the year 2000 will bring, but science and technology will still need to make fast, accurate measurements. I'm amazed that our very sensitive instruments are no more sensitive than they were in the 1860s, but the ease of getting the data and the accuracy of that data have certainly improved."

For the first time, these instruments provided live automatic measurements with full annotation and measurement statistics to show how much a measurement result varies.

The 11400 digitizing scopes, in particular, provided a combination of digitizing rate, bandwidth, record length, and resolution never before available in a single instrument. They incorporated the first multiple-microprocessor control platform, with dedicated processors for acquisition, display and waveform measurement, thus combining high-performance signal acquisition capabilities with waveform analysis functions.

Today's state-of-the-art digitizing scope from Tektronix incorporates proprietary digital signal processing technology, dubbed TriStar DSP, into an advanced acquisition platform. Having combined the TriStar DSP technology with the 11400 architecture for instant measurement and analysis of ultrafast transient or repetitive signals, Tektronix claims to have created a new and more powerful class of instruments it calls Digitizing Signal Analyzers. The DSA 600 series provides, in real time on a "live" display, analysis that previously required extensive and delayed signal processing from an external computer. The top-of-the-line DSA 602 acquires signals at 2 Gsamples/s and has a 1-GHz bandwidth and 8-bit vertical resolution.

As advanced as general-purpose digitizing scopes have become, they don't offer the complete test and measurement capabilities required by researchers, designers, troubleshooters and manufacturers of digital communications equipment. The high-speed data streams of communications modules and links have to be monitored for noise, jitter and bit error rates. These measurement tasks are most effectively accomplished with eye diagrams and bit-error-rate testing.

An eye diagram is formed by acquiring a random stream of serial digital data with an oscilloscope where the instrument is triggered by a synchronous clock. Tektronix has developed a specialized class of scope, the CSA 803 Communications Signal Analyzer. With bandwidths of up to 40 GHz and a continuously updated statistical database, the CSA 803 can automatically analyze eye diagrams and has on-board testing capabilities for the emerging FDDI, SONET and ISDN communications standards.

The CSA 803 samples a data stream at intervals of 10 fs, about the time it takes light to travel approximately three-quarters of a millimeter. As the scope samples the random bit stream, it overlays the high and low samples from many acquisitions on the display, resulting in an image that resembles an eye.

It's entirely possible that this technology could lead to an estimation of bit error rate, or a correlation of errors to waveform parameters that would cause the errors. With an error rate as small as 10^{-15}, an engineer using a bit-error-rate tester might have to wait for hours for an error to occur. For many data communication systems such an error could be very significant—like the decimal point in a checkbook balance, for instance!

About 45 percent of the instruments worldwide today are controlled by computers, and that will increase to 70 percent by 1995, according to George Sparks, general manager of the Hewlett-Packard Measurement Sys-

tems Operation in Loveland, CO. The significance of software development to the future of instrumentation is nowhere more evident than at Sparks' HP division, where 98 percent of the employees are involved in developing software.

Sparks sees the instrumentation industry right behind the computer industry in adopting standards. Two of the standards that will have the most impact, he says, are the programming language called SCPI (Standard Commands for Programmable Instruments), which evolved from HPSL and TMSL, and VXI, the VMEbus Extension for Instrumentation, which addresses the instrument-on-a-card concept.

One of the most exciting things that will happen in the next decade, according to Sparks, is that microprocessor-based instruments will get so smart that they'll be sitting on LANs by themselves. "We'll have a distributed measurement system," says Sparks.

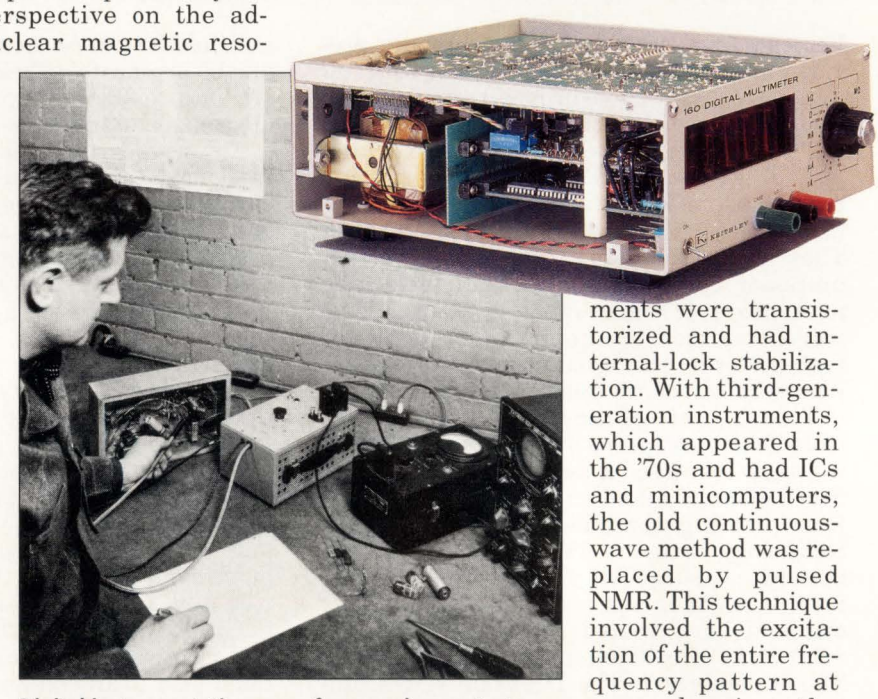
The digital revolution has transformed all areas of instrumentation, including areas that are less familiar to engineers professionally (but perhaps more important personally). A historical perspective on the advances made in nuclear magnetic resonance (NMR) shows the technological achievements in medical instrumentation.

The earliest work in detecting NMR signals was applied not to medical diagnosis but to physics. Felix Bloch of Stanford and Edward Mills Purcell of the Massachusetts Institute of Technology and Harvard University shared the Nobel Prize for physics in 1952 for the development of new methods of precisely measuring nuclear magnetism and for discoveries made with the aid of those methods.

In the nuclear induction method of detecting NMR signals used by Bloch and his Stanford colleagues, the induced emfs (electromotive forces) caused by changes in nuclear magnetization were picked up by a receiver coil, amplified, and then detected. A transmitter coil produced the original transitions and was kept close to the sample. To keep radio frequency energy from going directly from the transmitter coil to the receiver coil and blocking the amplifier, the two coils were wound at right angles to each other.

When Purcell returned to Harvard after a wartime assignment at the Radiation Laboratory at MIT, he used skills acquired in building airborne radar to probe the behavior of the proton and electron in the hydrogen atom. The relationship between the proton and electron, both of which spin like tops and act as magnets, can change only in certain ways, with absorption or emission of precise amounts of energy. To measure those energy transfers, Purcell used a method called NMR absorption. Purcell made atomic nuclei dance in rhythm with a radio wave. The atoms were placed inside the core of a high-frequency coil, which was in turn placed in the field of a strong magnet to align the tiny nuclear magnets. By subjecting the nuclear magnets to radio waves, Purcell changed their orientation. And by noting the frequency that permitted the atoms to absorb energy, Purcell found the energy for nuclear realignment, and thus the magnetic moment.

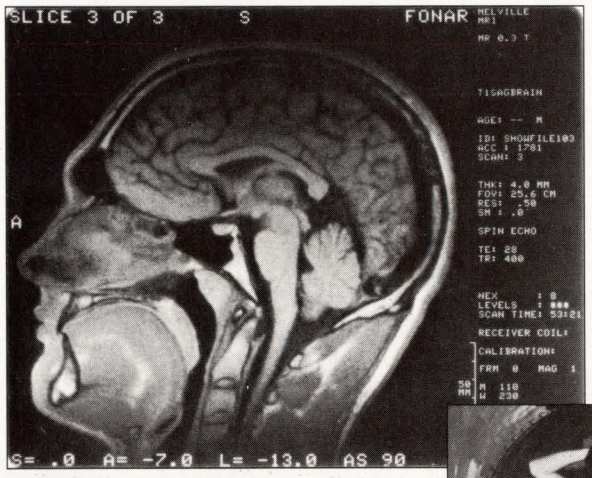
The first commercial NMR spectrometer was sold in 1953. Second-generation instruments were transistorized and had internal-lock stabilization. With third-generation instruments, which appeared in the '70s and had ICs and minicomputers, the old continuous-wave method was replaced by pulsed NMR. This technique involved the excitation of the entire frequency pattern at once, leaving the computer to untangle mathematically the time-based interference patterns of signals coming from the detector through the use of Fourier transformations.

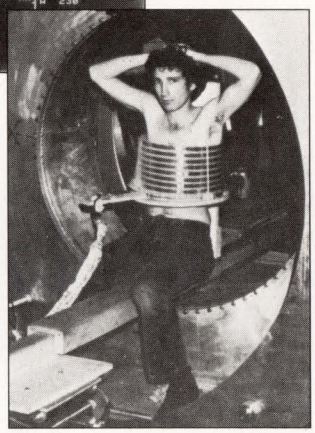


Digital instrumentation grew from analog roots. In an early photo, Joe Keithley works on an analog instrument. By 1970, his company introduced its first digital multimeter, the Model 160 (above).

In the late '60s and early '70s, Dr. Raymond Damadian, then a professor at Downstate Medical Center in Brooklyn, NY, successfully applied the principle of NMR to distinguish between healthy and diseased tissue. From his basic scientific research in

biophysics and biochemistry, the possibility occurred to Damadian that he might be able to obtain a radio signal from cancer tissue that a scanner could use to hunt down cancer in the human body. In 1970, Damadian removed some rat cancers, put them in test tubes, and put them into a laboratory NMR analyzer. He discovered that the radio signals from the cancerous tissue were dramatically different from the signals from normal tissue.





DSP techniques and computers manipulate scan images (left). A scan can be viewed in sequential slices. Computers that perform such manipulation weren't available in 1977 for the first scanner.

Though the scientific community at large considered it theoretically impossible to build a scanner based on NMR, Damadian and his assistants, Dr. Lawrence Minkoff and Michael Goldsmith, relying for the most part on used hardware, built the Indomitable, a prototype whole-body scanner based on a superconducting magnet. On July 3, 1977, this forerunner of all modern-day scanners delivered the first human image—that of Dr. Minkoff's chest. Since the magnet in the Indomitable had many undesirable characteristics, Damadian abandoned the superconducting approach and placed the Indomitable in the Smithsonian Museum. In 1980, Damadian's newly founded company, Fonar of Melville, NY, made available the first commercial NMR scanner. Fonar scanners are based on either an electromagnet or a permanent magnet. Other makers of NMR scanners continue to use superconducting magnets.

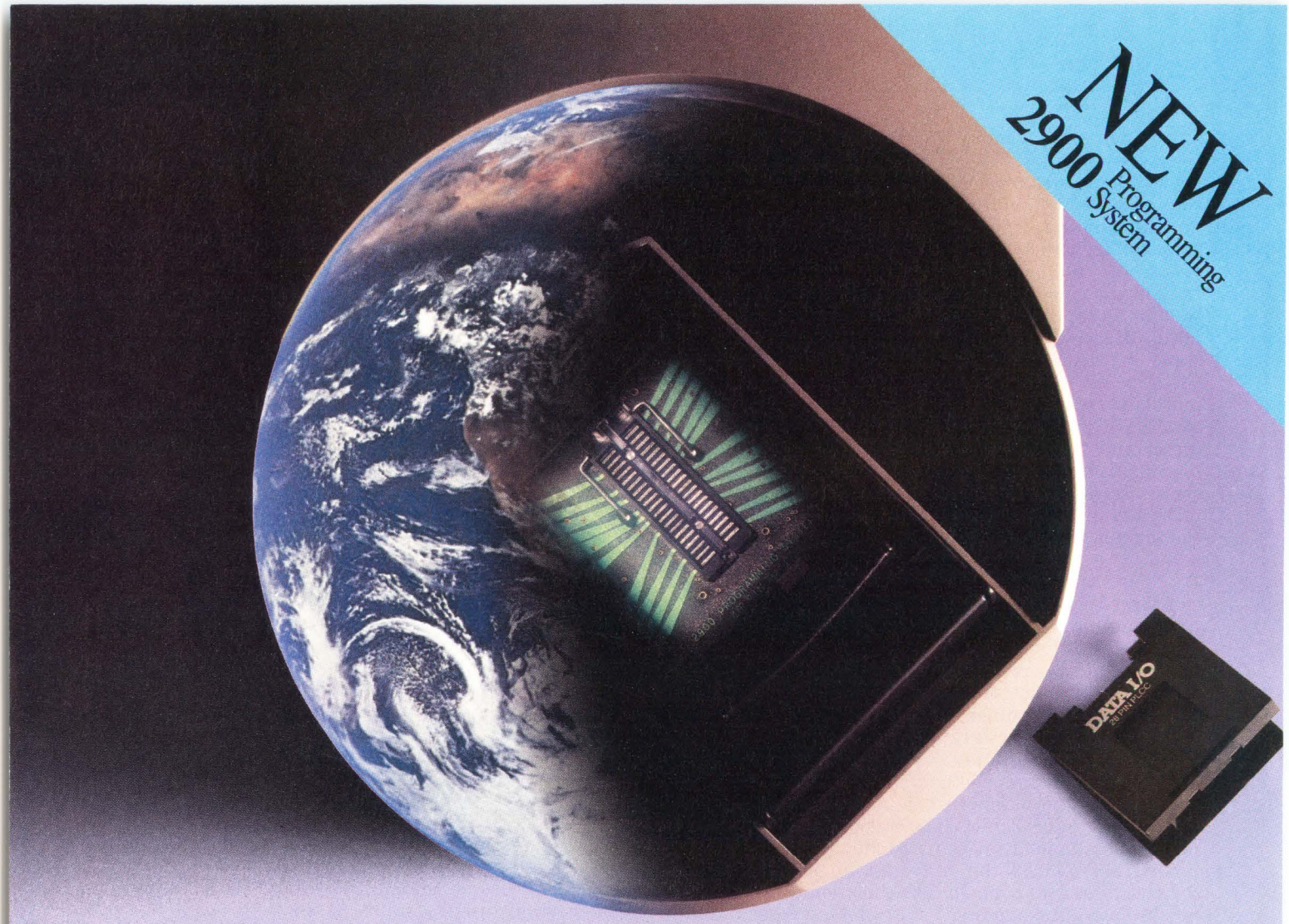
Damadian and Dr. Paul C. Lauterbur shared the National Medal of Technology, awarded by former President Ronald Reagan in 1988, for their independent contributions in conceiving and developing the application of magnetic resonance technology to medical uses including whole-body scanning and diagnostic imaging. Lauterbur, credited with the development of the first magnetic resonance images, had first demonstrated a method of converting NMR signals into images with two 1-mm capillary tubes of water in 1973.

Most medical applications of NMR use protons in the body to make anatomical images of structures. Magnetic resonance imaging involves the proton density data of a cross-sectional slice anywhere through a person presented as a 2-D color intensity plot of the anatomy at that cross-section. Among advantages over x-ray imaging, magnetic resonance images show much better contrast on soft tissue and involve no harmful radiation. The high-contrast capability of NMR stems from both the signals' dependence on the proton (hydrogen nuclei) density and the local environment of tissue water. The signals measured from water protons in tissue give information about local tissue conditions and change due to certain disease states of the tissue.

When inducted into the National Inventors Hall of Fame in 1989 for his invention of the NMR scanner, Damadian explained the significance of NMR to medical science: "Each type of atom puts out a signal at its own frequency, i.e., you can tune in your favorite atom the way you can tune in your favorite FM station. What we end up listening to on the receivers is a veritable atomic broadcast that informs us in remarkable detail of what's going on in the tissues of your body."

Damadian went on to say that he hopes that magnetic resonance scanner technology will eventually replace the surgical biopsy with an entirely noninvasive electronic biopsy and offer a truly effective treatment for cancer. He also sees magnetic resonance proving useful in detecting schizophrenia and in tracing the progress of manic-depressive patients as they undergo therapy.

By Barbara Tuck, Senior Editor



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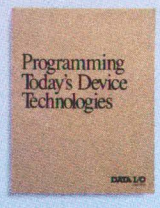

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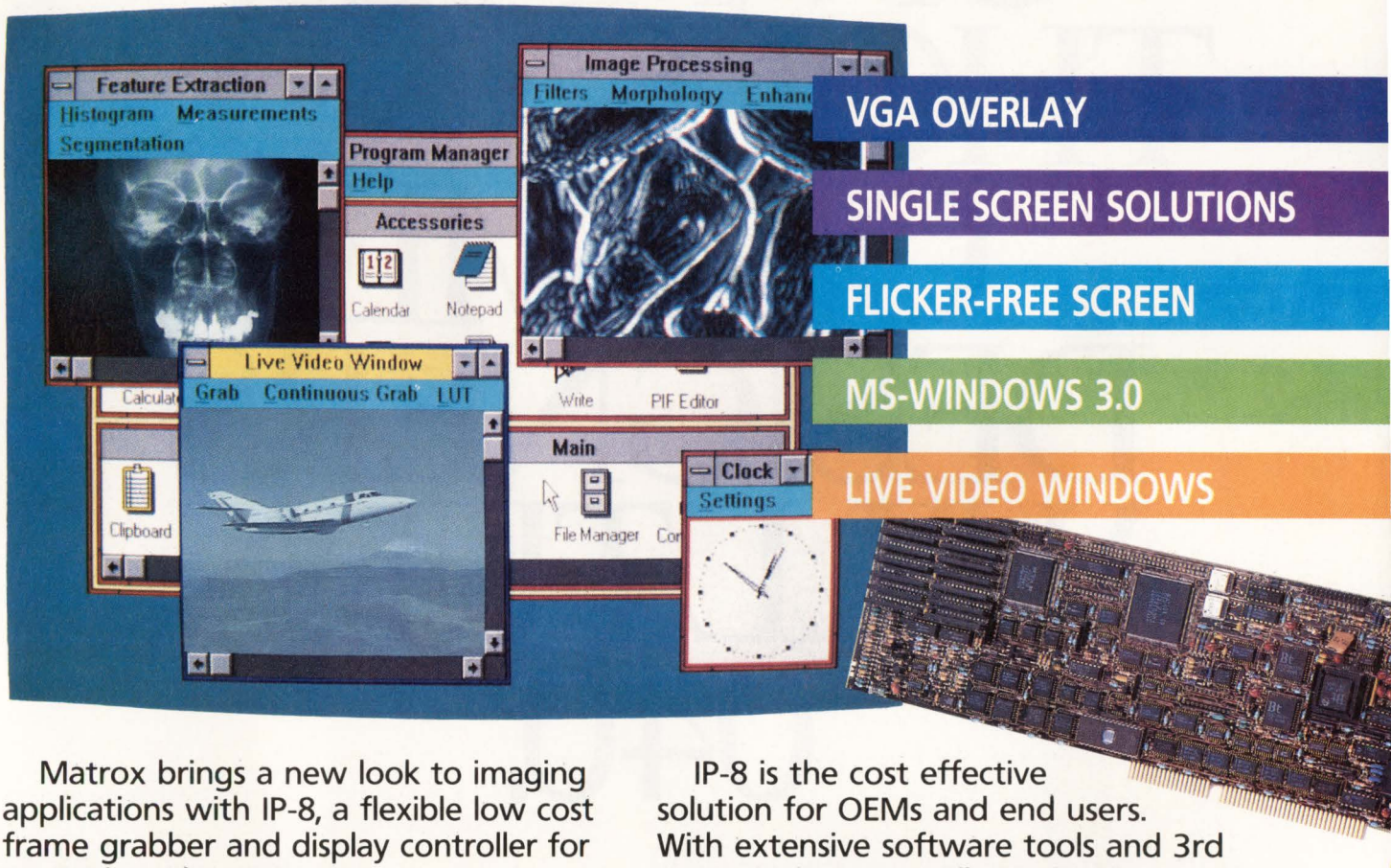

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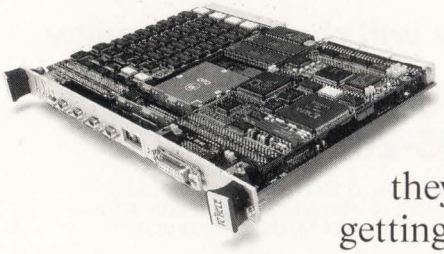

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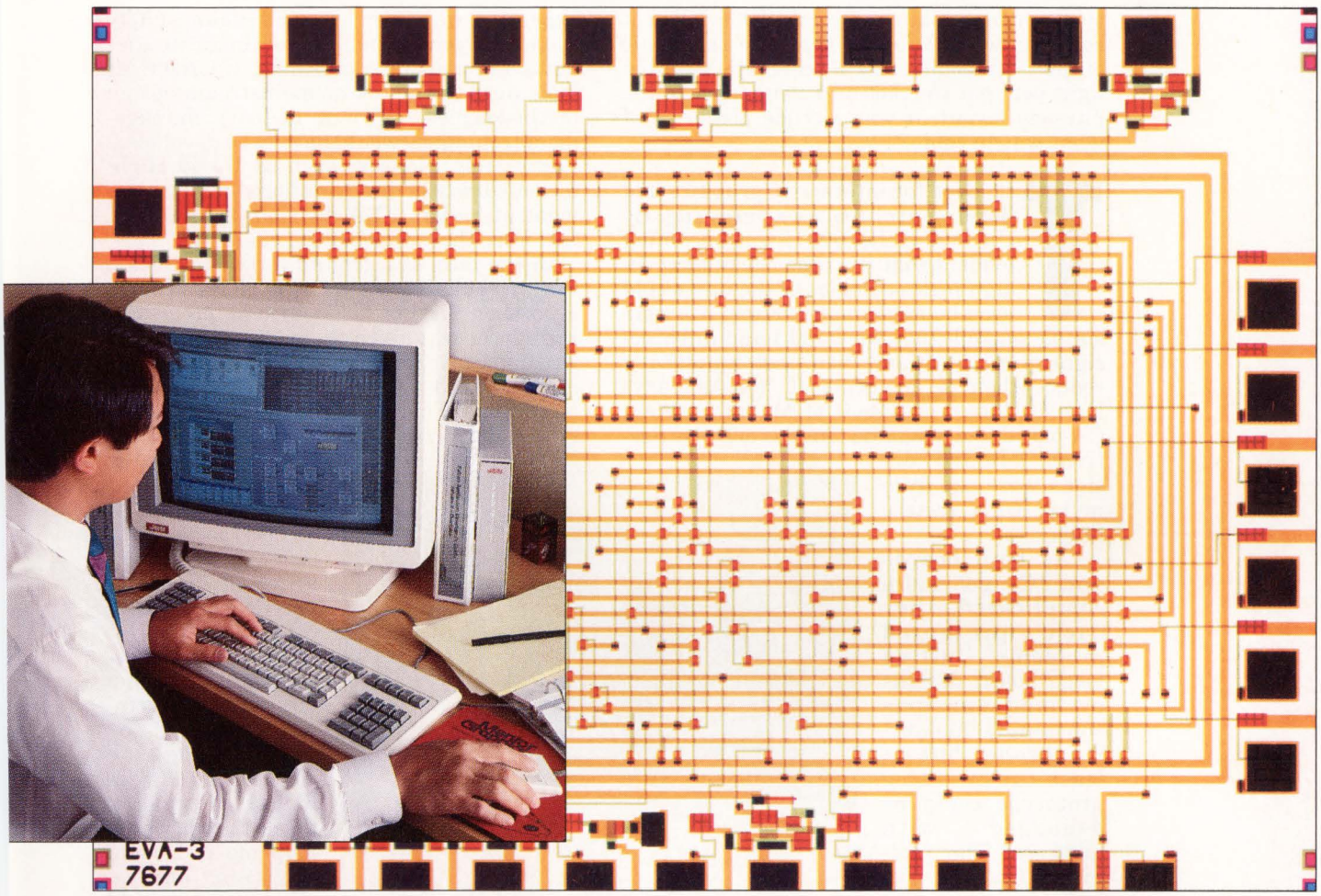


EDA—a success story in three decades

The history of CAD and CAE is an explosive one, starting out as an academic pursuit in the 1960s and snowballing into a $2.5 billion industry by the end of the '80s. Together, these design pursuits, commonly referred to today as EDA, have been engaged in a spiralling hardware/software design effort where better tools enable designers to build better computers on which to build better systems. The '90s will see this amazing escalation continue.

Today's EDA products are so available and affordable that it's easy to forget that only two decades ago there were but a few tools that could be considered to be automated at all, and they were primitive. The seminal effort that went on during the '60s and '70s was truly visionary. With few exceptions, the basic algorithms and interactive graphics used by EDA vendors today have their roots in those first two decades.

Though the first commercial CAD applications weren't available until the early '70s and were essentially automated drafting tools, there were prototypes being developed in the '60s by large systems houses such as Armonk, NY-based IBM. "I was working at IBM's East Fishkill facility in 1965, and became interested in connecting computers to the real world," recalls James Koford, chief technical officer and senior vice-president at LSI Logic in Milpitas, CA. "In the spring of 1965 I decided to tie a graphics display to a small computer to lay out IBM circuit models.

"I built a system with an old Sage display and a commercially available light pen and built the interface myself. Some people say that it was the forerunner of the early CAD

Early moves to improve design efficiency, such as this layout for a standard cell developed by NCR in 1968, had to depend on manual methods. Thirty years of advances in design automation now focus on integrated design environments, as with this system from Mentor Graphics.

systems from Calma. By mid-1966 I had it running on a plotter to generate schematic output. You could enter a schematic with the light pen, get the plot and compare it to the physical layout. It was a crude precursor of what was to come."

The need for interactive graphics and design entry tools was growing. By the end of the '60s it was becoming evident that the time-consuming design methodologies of the day would soon be inadequate. "Early ICs were simple enough that we could hand-draw designs on rubylith and then photographically reduce them to generate IC masks," says Harvey Jones, president of Mountain View, CA-based Synopsys and founder of Daisy Systems. "Board designs were cut from mylar with X-Acto knives.

"As both boards and ICs got more complicated, they each presented problems. Cutting large board designs by hand was time consuming and error prone, but at least the resulting prototype could be debugged with jumpers. The tooling cost of ICs was high, however, and you couldn't put jumpers on an IC. It became obvious that mechanized drafting tools and IC simulation were a necessity."

Hand-cut rubyliths were once the first step in transforming designs into hardware. As the complexity of designs increased, it became necessary to automate the drafting process, and the CAD system then replaced the X-Acto knife.

The first systems from Calma, Applicon and Computervision let designers digitize and automate the board- and IC-drawing processes. Though these systems were tremendously expensive (the best models were priced near $250,000), they were worth the investment to silicon and systems houses that needed the power to design their next generation of products. "Managers would work those systems around the clock," recalls Synopsys' Jones. "Three shifts a day would digitize ICs, edit them and produce masks. There were even plotters that had knives to cut the rubylith, but it still had to be lifted off by hand."

Even before such systems hit the market, it was clear that to advance to the next phases of design automation—namely, automatic placement and routing and IC simulation—it would be necessary to streamline the code for efficient memory management. The mainframes of the late '60s and early '70s used expensive core memory, and there simply wasn't enough available to run intricate simulation or routing algorithms. If CAD/CAE tools were to make it as mainstream design methodologies, efficient memory management techniques would have to be developed. Fortunately, pioneers such as David Hightower, currently director of product development at Seiko's EDA division in San Jose, CA, were there to meet the challenge.

In the late '60s, Hightower was a rookie working at Bell Labs in Holmdel, NJ. Known even then for his fast, efficient programs, Hightower was given the unenviable task of writing a printed circuit board routing tool in Fortran that could run on an IBM 7094 mainframe. The 7094, one of the most powerful computers available at the time, posted 0.25-Mips performance and sported 32 kbytes of memory, a capability that's almost laughable when compared to today's 2-Mbyte laptops.

After several frustrating months, Hightower accomplished the task by approaching the problem with imagination. "I began to think that it would help me if I could envision how a blind person would get around in a maze without walls, with just a bell ringing to guide him," recounts Hightower. "I needed to find the bell. Using this approach, I worked out a detailed algorithm." The algorithm was first written in Snoball, a Bell Labs software language, and later in Fortran. The Hightower algorithm represents two important firsts in router design—it was rule driven and gridless. It's still used today.

The other piece to the design automation puzzle, simulation, was in its embryonic stage at about the same time. Though it wasn't until the early '70s that simulators suitable for IC analysis became available, initial work was targeted toward the development of device and circuit analysis techniques. During this period, Tegas emerged as a standard digital logic simulator and Spice was being developed at the University of California at Berkeley as a model for analog simulation.

All of these enabling technologies would usher in the '70s and the next generation of ICs and systems. The products produced with

these tools—namely, the microprocessor and the minicomputer—would spawn the next phase of the EDA revolution.

In the early '70s, compute power was still limited and expensive. Though Maynard, MA-based Digital Equipment Corp had unveiled its PDP-8 minicomputer in 1965 for only $16,000, most of the CAD work in the early '70s was reserved for the expensive digitizing systems and large mainframes of the day. Engineers were, however, using the lower-priced DEC systems to develop simulation algorithms that would find their way not only into IC and board simulation but also into the emerging automatic test equipment arena.

"I started work in the '70s for an IBM-sponsored project at Carnegie-Mellon University," says Prabhu Goel, founder of Gateway Design Automation and president of the advanced CAE division at Cadence Design Systems in San Jose, CA. "Much of our work was in developing simulation and synthesis tools. Though the project was sponsored by IBM, most of our work was done on DEC PDP-10s and PDP-11s. After I graduated, I went to work for IBM and found problems in the error-correction portion of IBM's test algorithms and was given the task of fixing them. Our group came up with an algorithm called Podem that solved the problem. By 1975 we had developed Podem-X, a simulation-based test tool for VLSI chips with the equivalent complexity of 100,000 gates. In 1975, that was a lot of gates."

Though these test-generation algorithms would first be sponsored by large companies for use as in-house tools, they laid the groundwork for the commercial test and simulation products that would appear in the early '80s. In 1972, for instance, Lutz Henkels, president of North American operations at Mahwah, NJ-based Racal-Redac, was working at GenRad with fault simulation as a means of grading the quality of board test vectors. Henkels oversaw the development of the Caps simulator at GenRad, and after founding HHB Systems in 1977, produced a simulator in 1979 that simulated faulty device behavior without compounding the computer run time required. The simulation products that HHB eventually brought to market—namely, the Cadat simulator, introduced in 1983—built on this early work in fault simulation.

In parallel with the development of simulation tools, automatic layout tools, or autorouters, were beginning to take shape. Up to this time, layout programs required designers to create printed circuit traces by hand using a light pen and a keyboard. Component netlists were compiled manually from a circuit diagram and entered by typing them into the computer. The computer analyzed the circuit for stray capacitance, lead inductance and other analog variables.

In the mid-'70s, Racal-Redac was the first commercial vendor to offer an autorouting capability for board design based on the Hightower algorithm. Though the routed circuits invariably required some manual clean up, the tools were another steppingstone in the path toward shortening the time-consuming portions of system design.

"Layout was and is a downstream task that's basically a pain," says Racal-Redac's Henkels. "It isolates the designer from the finished product. Designers would place their project in the layout cycle, even if it was full of holes, because they knew it was going to take a lot of time and they wanted to get it into the queue. Unfortunately, we're still treating layout and test as processes apart from design." The automation of these processes did, however, close the productivity gap that had existed between design and manufacture. As the '70s drew to a close, most of the major design methods that we know today were in place. It was time for the EDA explosion to begin.

At the beginning of the '80s most of the place-and-route and simulation tools were proprietary solutions that began in universi-

In the early morning, a company is born

In the early days of EDA, resources were limited but talent and enthusiasm were high. For example, the founders of San Jose, CA-based Valid Logic Systems, L. Curtis Widdoes and Thomas McWilliams, met while completing their studies in Stanford University's doctoral program in computer science. "I was working on a DEC PDP-10 to design a superfast PDP-10," recalls Widdoes, now president, CEO and founder of Logic Modeling Systems in Milpitas, CA. "We were using Stanford's Drawing System, and we dubbed our computer the Super-Foonley. Anyway, our design was taken to Digital Equipment Corp and was the basis for DEC's ECL system, the KL-10.

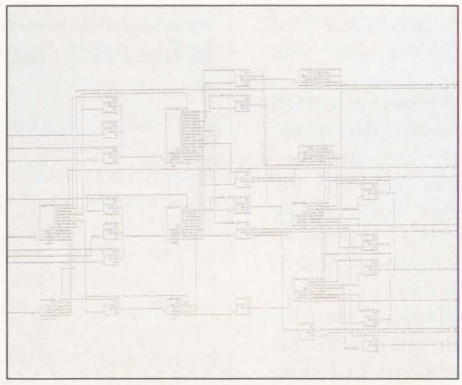
"In 1975, Tom and I were approached by Stanford's Lowell Wood to build a new supercomputer at the University of California's Lawrence Livermore Laboratory. The project was the S-1 Mark-1 computer, commissioned by the U.S. Navy. We knew that we'd need to develop special computer-based tools in order to handle the size and complexity of the system as specified: a 15-Mips, 5,500-chip, ECL-based, 10-kbyte processor. There was only one problem. We were told that computer time was tight, so we could only use the KL-10 from six to nine in the morning each day."

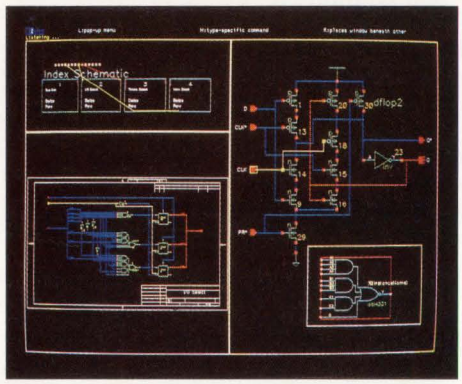
Widdoes and McWilliams focused on three essential capabilities for these tools: interactive graphics, hierarchical design structure and automatic verification. These three elements were the building blocks of the Scald (Structured Computer-Aided Logic Design) system, which would become the backbone of Valid's first system. In 1977, Widdoes and McWilliams completed both the development of Scald and the S-1. The Scald company was founded in January of 1981 and began operations in Sunnyvale, CA.

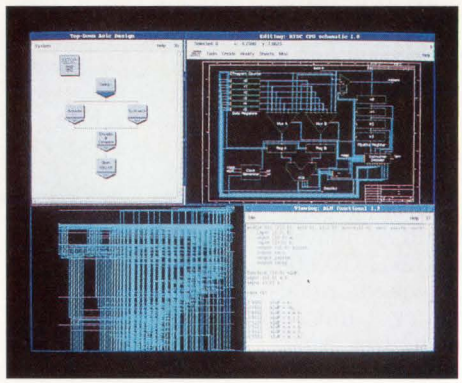
"We struggled for months with the name," says Widdoes. "I liked Scald, but everyone told me it sounded like some kind of Norwegian cocktail. Besides, our investment bankers pointed out that our competitors would have a field day warning people not to get scalded. Someone suggested 'Valid Logic Systems' and it stuck."

ties and were used by major systems and silicon houses. There were several reasons for this.

"For one thing, there weren't many good commercial tools on the market," says Jim Hammock, president of the silicon design division at Beaverton, OR-based Mentor Graphics and chairman of the EDAC executive committee. "Manufacturers also wanted to differentiate their products, not only with their individual manufacturing processes but also with their design expertise. Lastly, both silicon and system vendors felt that they were the only ones who could get the tools close enough to their manufacturing processes to do a good job of implementation."







Design systems have seen tremendous advances in the last 30 years. An example of a computer-generated schematic (top) is from the 1960s. The schematic editor (center) typified systems of the '80s. In the '90s, schematic entry is based on hardware description languages, as in this Amadeus system from Cadence Design Systems.

Most of the attention, however, was being placed on the layout and manufacturing end of the system-development process. The real beginning of the EDA revolution began when vendors realized that design engineers, not just layout personnel and manufacturing facilities, needed automation tools.

"It became clear to me that the next step had to involve the design engineer, a concept that I called 'up the design cycle,' " says Synopsys' Jones. "Companies were spending millions on layout and nothing on engineering, even though 80 percent of their salary expenses were for professional services. There was also a landmark Merrill Lynch research project predicting that all of the growth of the future would be in CAD. So off went Calma, Applicon and Computervision to pursue CAD and CAM. Art Kohlmeir and I saw an opportunity and started Daisy Systems."

In 1981, Daisy unveiled the Logician, a $75,000 workstation based on an Intel 8086 microprocessor, 512 kbytes of RAM and a 10-Mbyte disk. It offered schematic capture with a command-line interface. The following year, San Jose, CA-based Valid Logic Systems introduced Scaldsystem, a 68000-based workstation that was built around the public-domain Scald (Structured Computer-Aided Logic Design) methodology. This methodology was pioneered by Valid founders L. Curtis Widdoes, founder and current president and CEO of Logic Modeling Systems in Milpitas, CA, and Thomas McWilliams, vice-president of corporate architecture and technology at Amdahl in Sunnyvale, CA (see "In the early morning, a company is born," p 109). Valid's entry served up to four users and offered schematic entry, netlist compilation, logic simulation and timing verification.

Though both Daisy and Valid made the decision to bundle their tools on proprietary platforms, Thomas Bruggere and Gerald Langeler, formerly executives at Tektronix in Beaverton, OR, had a different plan when they started Mentor Graphics. "We decided right from the start that we didn't want to build our own hardware," recalls Bruggere, Mentor's CEO. "We despaired at first because there wasn't anything out there to suit our needs. Then we discovered a little company called Apollo and placed a $1 million order. It was a perfect synergistic match. We had no money and they had no sales. We suffered through those first years when Daisy and Valid were posting higher margins than we were, but when the next generation of hardware came out, and they found it hard to keep up, it looked like we had made the right decision."

Mentor's 1982 Idea Station bundled integrated schematics, logic simulation and documentation capabilities on Apollo's first workstation, the 0.3-Mips DN 100, for $120,000. The Idea Station introduced a key innovation—the ability to probe a signal or

select an object on the schematic for the simulator to analyze.

After 1982, dozens of companies jumped on the CAE bandwagon, including pioneer firms such as Metheus, CAE Systems and CASE Technologies and ASIC suppliers such as LSI Logic and VLSI Technology. Test manufacturers GenRad and Teradyne joined in as well, and instrumentation giants Tektronix and Hewlett-Packard followed suit. As the '80s wore on it became clear that the newborn CAE industry couldn't support that many players. There were several reasons for this.

First of all, stunning advances in workstation technology made users clamor for more compute power. As they did, their patience with proprietary platforms wore thin, and their need to integrate the best tools from a variety of vendors increased. Secondly, the resurgence of gate array and standard-cell ICs made EDA more of a necessity than a luxury. To stay competitive, IC and system vendors had to have the latest tools.

The Scald system derived from a Navy project at the Lawrence Livermore Laboratory in the late 1970s. Scald developers L. Curtis Widdoes and Thomas McWilliams founded Valid Logic in 1981 to market the technology.

At first, users were content with proprietary netlist interfaces to simulators or layout packages, but in the mid-'80s, the Electronic Design Interchange Format began to define an industry standard for interfaces. This development only whetted the design engineers' appetites, and they clamored for more standards.

One of the key elements in tool standardization came in the form of frameworks that promised to provide an integrated database and common user interface for tools supplied from various vendors.

In 1983 James Solomon founded SDA systems and offered a single, object-oriented database for IC schematic, simulation and layout tools. Based on framework research done at his alma mater, the University of California at Berkeley, Solomon's offering took some of the framework's key elements—the user interface, the idea of a single database and portable graphics—and bundled them with the Skill user language.

"The main problem we faced in those days was expense. Developing that kind of software cost far more than we had anticipated," says Solomon, president of Cadence's analog division. "We initially guessed that it would take about $10 million to launch the product, but it ended up coming in at around $20 million. The key decisions for us were when we realized that we couldn't just sell a framework, we needed tools. In addition, our decision to use Unix as an operating system—a bold move in the early '80s when it was new—gave us the portability that's been a key part of our success."

Frameworks continue to be a hot topic today, mainly due to the efforts of the CAD Framework Initiative, a group of EDA vendors committed to the realization of an open framework standard.

There were other areas where the lack of standards was hampering the burgeoning EDA marketplace—namely, the lack of hardware models as a basis for true simulation. "Around 1982 to 1983, we were having serious problems selling simulation," says Logic Modeling's Widdoes. "Though we knew our customers wanted to simulate complex systems, we also realized that to do this they needed an accurate simulation model for each device in the design. That was especially difficult for complex parts like the 68000 or the 8086. Developing a software model for these devices would be a costly enterprise both for us at Valid and for our customers. So I decided to plug the parts into a system and feed them stimuli, measure the response and send the data back to the simulator."

Valid introduced Realchip, the hardware modeler that was the result of Widdoes' work in 1984. Its popularity was immediately proven when similar offerings from Daisy, Mentor, Teradyne, Cadnetix, GenRad and HHB Systems hit the streets. The ensuing systems became embroiled in patent infringement suits with Valid, some of which continue to this day.

The confusion resulting from these myriad

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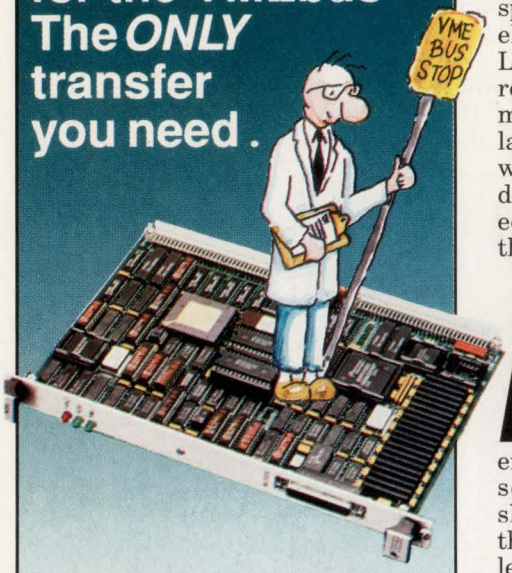

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products highlighted a problem with the hardware modeler market—namely, that each was dedicated to a specific simulator. The buying public's frustration with a lack of standards, however, inspired Widdoes to license the modeler technology from Valid and start Logic Modeling Systems, which rolled out the LM-1000 in 1989—a modeler that serves multiple simulators and platforms. This drive toward standards and more-efficient design methodologies will undoubtedly be the driving force of EDA in the '90s.

As EDA moves into the '90s it's faced with the task of providing tools and design environments that address the dilemma that IC and systems manufacturers are facing—device complexity is soaring and time-to-market is shrinking. The main weapons in the EDA arsenal to meet this challenge are hardware description languages (HDLs), logic synthesis tools and concurrent engineering environments. All three weapons address the way designers approach a project and see it through to completion.

HDLs, such as Verilog and VHDL, are generally accepted as the primary form of design entry that will be used in the '90s. Designs are getting too complex for designers to remain mired in gate-level detail, and systems are getting too complex to efficiently integrate these complex parts into coherent platforms. HDLs enable users to enter designs at a behavioral level, an ability that eventually will move them up the design cycle once again.

The enabling technology behind the acceptance of HDLs, however, is logic synthesis, which takes these high-level descriptions and translates them down to gate-level implementations. "In 1987, I saw the need to bridge another gap that I saw on the horizon," says Synopsys' Jones. "Just as we saw a shift from layout to gate-level tools in the '80s, it became obvious that we needed a shift from the gate to the functional level. There's an analogy not unlike what we saw in software a decade ago. Software engineers abandoned machine code when compilers became sophisticated enough to allow programs to be written in high-level languages. Likewise, HDLs and synthesis will eventually free designers from thinking about gates."

Concurrent design environments will let users partition the complex chip and systems designs of the coming decade into manageable parts. Ideally, each part can be designed by members of a design team, with a coherent database keeping the parts in sync during the design cycle. Concurrent environments won't just effect product designs, they'll follow the process through to manufacture, bridging a gap that has been traditional since the inception of EDA.

"The walls separating design, layout and manufacturing will have to come down in the '90s," says Joe Prang, Valid's vice-president of marketing. "The driving forces of top-down methodologies and frameworks will lead toward an integration of the design process. It's a natural next step after computer-aided drafting in the '70s and the engineering and design automation of the '80s."

The last 10 years especially have seen many breakthroughs and events that have driven design tool performance up and prices down. Spectacular price reductions in workstation and personal computer performance have brought mainframe power to almost every engineer's desk. Today's PC-based tools offer sophisticated board autorouter capabilities for under $1,000 that cost tens of thousands of dollars only a decade ago. And the blossoming EDA technology shows no signs whatsoever of slowing down.

"By the year 2000 there will be no need to prototype hardware in a conventional sense," predicts Cadence's Goel. "We'll be able to simulate accurately and build hardware right the first time. The lines between hardware and software design will blur, and we'll be thinking in terms of system design. One of the driving forces behind all of this will be time-to-market. It'll be a hell of a decade."

By Mike Donlin, Senior Editor

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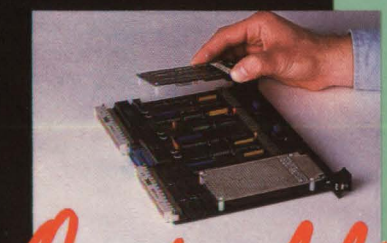

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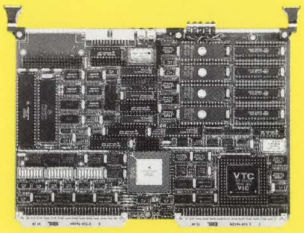

- 68020 16.66 - 33 MHz CPU
- (8) 28-pin RAM sockets for up to 265KB of dual-access zero-wait-state-static RAM
- (8) 32-pin sockets for up to 8MB of ROM, (4) sockets may be EEPROM
- (2) RS232C asynch serial ports
- (16) lines of parallel I/O
- (1) (OMNIMODULE socket for a wide variety of I/O (i.e. 2 serial ports, 20 parallel lines)
- VIC068 VME Interface Controller

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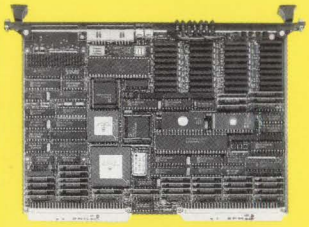

- 68020 16-33MHz, CPU
- 1-4 MB of dual-access, zero-wait-state DRAM with parity
- 68882 (optional)
- (2) 32-pin ROM sockets
- (2) RS232C serial ports
- (2) 8-bit parallel ports
- (1) OMNIMODULE socket for a wide variety of I/O (i.e. 2 serial ports, 20 parallel lines)
- 4 level bus arbiter (optional)

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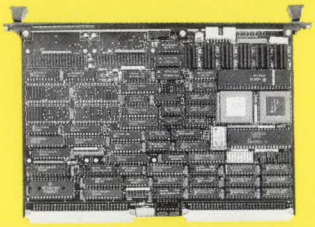
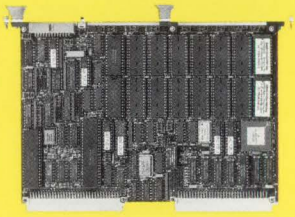


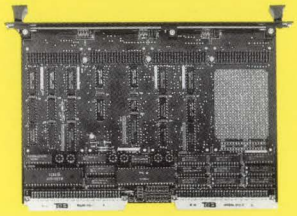
- 68000 12.5MHz 16/32 bit CPU
- 512KB of dual-access, zero-wait-state DRAM with parity
- (4) 28-pin ROM sockets
- (3) 16-bit counter/timers
- (2) Omnimodule™ I/O sockets for a wide variety of I/O (i.e. 4 serial ports, 40 parallel lines)
- DMA controller (optional)
- VME bus interrupt generator (optional)
- Optional 4 level bus arbiter
- Two year limited warranty

OB68K/VME1™ VME SINGLE BOARD COMPUTER



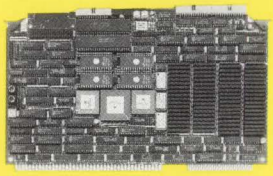
- 12.5 MHz 68000 CPU
- (8) pairs of 28-pin sockets for RAM or ROM
- (2) RS-232C serial ports
- (2) 8-bit parallel I/O ports
- System Controller

OB68K/VIO™ VME UNIVERSAL I/O BOARD



- (4) Omnimodule I/O sockets for a wide variety of I/O (i.e.8 serial ports, 80 parallel lines)
- One (1) interrupt per Omnimodule, two (2) optional

OB68K/MSBC30™ MULTIBUS I SINGLE BOARD COMPUTER



- 25-33 MHz 68030 CPU
- 4-32 MB dual access, zero-wait-state DRAM w/parity
- 68882 Math Co-Processor (optional)
- 2 channel DMA controller (optional)
- (2) RS232c sync/async serial ports
- (2) 8-bit parallel ports
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DESIGN AND DEVELOPMENT TOOLS

Logic analyzers offer RISC support and ease-of-use

Jeffrey Child, Associate Editor

The Centurion logic analyzer from Tektronix provides 100 channels (96 data, 4 clock), as well as 100-MHz sampling, clocking and triggering capabilities on a single card. Designed for use in the Tektronix DAS9200 mainframe, Centurion also offers asynchronous acquisition up to 400 MHz over 24 channels.

Challenged by continued speed advances in RISC processors, ever-faster CISC processors and DSP chips, designers of microprocessor-based systems are being forced to redefine the minimum acceptable tool to accomplish their design and debug tasks. Because emulators do not yet exist for many of the latest high-performance processors, designers are looking to logic analyzers to help them locate system bugs and refine their software/hardware integration.

The effectiveness of a logic analyzer, like any other design tool, depends as much on its performance as it does on how friendly it is to use. With this in mind, logic analyzer manufacturers are offering friendlier interfaces, support for an increasing number of processors and better ways to analyze and store acquired data.

Speed, number of channels and memory depth still drive the logic analyzer industry. To meet the demands of RISC-based, 32-bit and multiprocessor designs, logic analyzers must be able to monitor signals at higher clock rates, must provide more channels to monitor bigger address and data buses, and must have more memory to display larger segments of monitored waveforms.

Turning to modules

In the competitive high-end segment of the logic analyzer market, vendors have turned to modularity to preserve their investment. Users can configure their systems without purchasing any more power than they need. And many companies let users trade channel width for sampling speed by halving the number of channels in order to double the sampling speed for timing analysis.

The latest module designed for the DAS9200 mainframe from Tektronix (Beaverton, OR) offers 100-MHz performance on a single card. Called the 92A96 Centurion, this module offers 32-bit RISC and CISC support and can observe multiple processors simultaneously.

The effectiveness of a logic analyzer depends as much on performance as it does on how friendly it is to use.

Centurion features 100-MHz state analysis, 400-MHz timing analysis and 16 100-MHz triggering levels on a single card. Centurion supports asynchronous measurements of up to 400 MHz for 24 data channels, or for up to 384 channels with card extensions. Up to 1,536 data channels can be acquired at 100-MHz synchronous or asynchronous acquisition rates, with each channel backed by a minimum of 8 kbits of memory. A 32-kbit/channel version, the 92A96D, is also available.

Alleviating complexity

While logic analyzers serve as useful tools in debugging high-speed microprocessor-based designs, they've traditionally had a reputation for being difficult to use. On a complex circuit board, for example, it used to take hours to hook up all the necessary probes. And because they're usually expensive, one instrument would have to be shared by a whole design group or wheeled around on cart between departments.

To alleviate these difficulties, the Philips PM 3580 logic analyzer series from John Fluke Mfg (Everett, WA) reduces state and timing measurements to one probe connection. Furthermore, the 3580s feature a single setup and fully integrated state and timing triggering for a common user interface. All measurements are time-tagged with up to 5 ns of resolution.

The PM 3580 family has an architecture unique among logic analyzers. By using ASIC technology on the front-end, this architecture allows both state and timing data to be acquired simultaneously from the system on up to 96 channels, with just one set of probes. Performance specifications provide up to 50-MHz state capability, up to 200-MHz timing functions and 2 kbits of memory per channel.

Besides eliminating the headache

Model	Maximum synchronous clock rate (MHz)	Maximum asynchronous clock rate (MHz)	Maximum number of channels (state/timing)	Number of channels at maximum sample rate (state/timing)	Memory depth/channel (bits)	Triggering levels	Minimum glitch capture (ns)	Price	Comments
Arium 1931 Wright Cir, Anaheim, CA 92801 (714) 978-9531									**Circle 301**
ML4100	70	100	32/32	4/4	1k to 8k	4	5	$2,495	8- and 16-bit microprocessor support
ML4400S	50	100	80/80	20/20	2k to 8k	14	5	$5,895	8-, 16- and 32-bit microprocessor support, RISC and digital signal processor support, performance analysis
ML4400M	50	100	320/320	160/80	2k to 8k	14	5	$16,000	same as above
ML4400T	100	400	64/16	16/16	8k to 32k	14	5	$19,000	same as above
Biomation 19050 Pruneridge Ave, Cupertino, CA 95014 (408) 988-6800									**Circle 302**
CLAS 4000	100	200	384	96	4k to 16k	15	5	$19,950	32-bit microprocessor support, RISC and CISC support
K450B	100	400	80	20	2k to 8k	16	5	$10,000	8-, 16- and 32-bit CISC support
Bitwise Designs 701 River St, Troy, NY 12180 (800) 367-5906									**Circle 303**
LAC-04	25	125	320/320	—/8	4k	16	—	$2,800	PC/AT card, 40 channels/card
LAC-16	25	125	320/320	—/8	16k	16	—	$3,200	PC/AT card, 40 channels/card, ISA slot required
LAC-64	25	125	320/320	—/8	64k	16	—	$4,500	PC/AT card, 40 channels/card, includes windows-based software, leads, clips
BITWISE-32	25	25	32/32	32/32	4k	4	—	$1,295	PC card, optional oscilloscope, 100-MHz option
Logic-Boy	50	50	16/16	16/16	1,024	4	—	$1,795	hand-held logic analyzer, LCD, parallel printer port
Hewlett-Packard 19310 Pruneridge Ave, Cupertino, CA 95014 (800) 752-0900									**Circle 304**
1651B	25	100	32/32	32/32	1k	8	3 to 5	$3,900	targeted for 8-bit microcontroller applications, support 15 microprocessors, microcontrollers
1654B	35	100	64/64	64/64	1k	8	3 to 5	$6,700	designed for 8- and 16-bit microprocessors
1650B	35	100	80/80	80/80	1k	8	3 to 5	$7,900	supports 8-, 16- and 32-bit microprocessors
1653B	35	100	32/32	32/32	1k	8	3 to 5	$7,400	includes 2-channel oscilloscope
1652B	35	100	80/80	80/80	1k	8	3 to 5	$11,300	includes 2-channel oscilloscope, cross-module triggering
16500A mainframe	—	—	—	—	—	—	—	—	16500A mainframe for 165XX modules
16510B	35	100	80/80	80/80	1k	8	3 to 5	$5,600	supports 8-, 16- and 32-bit microprocessors, microcontrollers and DSPs
16515A/16A	—	1000	32/32	32/32	8k	1	2	$8,100/$7,100	timing analyzer, 1-ns timing resolution
16540A/41A	100	100	208/208	208/208	4k	4	10	$7,000/$8,500	designed for RISC support
John Fluke Mfg PO Box 9090, Everett, WA 98206-9090 (206) 347-6100									**Circle 305**
PM 3585/90	50	200	96/96	96/96	2k	8	3 to 4	$10,950	time stamping, transitional timing, dual analysis per pin, set-up and integrated triggering
PM 3580/60	50	100	64/64	64/64	1k	8	3 to 4	$6,450	same as above
PM 3655	100	400	96/96	96/12	2k or 4k	4	5	$10,950	MS-DOS PC included

Model	Maximum synchronous clock rate (MHz)	Maximum asynchronous clock rate (MHz)	Maximum number of channels (state/timing)	Number of channels at maximum sample rate (state/timing)	Memory depth/channel (bits)	Triggering levels	Minimum glitch capture (ns)	Price	Comments
Keithley MetraByte 440 Myles Standish Blvd, Taunton, MA 02780 (508) 880-3000									**Circle 306**
PCIP-DLA	20	20	16/16	16/16	4k	3	—	$1,295	PC-based, 16-channel board
Orion Instruments 180 Independence Dr, Menlo Park, CA 94025 (415) 327-8800									**Circle 307**
9250/9350/9450	34	204	48/48	8/8	16k to 64k	4	20	$11,450	includes 2-channel, 100-MHz digital storage oscilloscope; analog function generator; 24-bit pattern generator
9260/9360/9460	34	204	96/96	16/16	16k to 64k	4	20	$14,550	same as above
Outlook Technology 200 E Hacienda Ave, Campbell, CA 95008 (408) 374-2990									**Circle 308**
T-100A	1,000	2,000	32	4	4k to 32k	3	1.5	$34,950	configurable as a logic analyzer, pattern generator or both
T-132W	500	500	32	16	4k to 16k	3	1.5	$27,950	synchronous harmonic sampling
T-132EM	500	500	32	16	2M to 8M	3	1.5	$69,900	same as above
T-132D	500	500	32	16	512k to 2M	3	1.5	$54,900	same as above
1600	200	200	16	16	1k to 4k	1	1.5	$24,700	all channels may be a logic analyzer or a digital storage oscilloscope optimized for logic signals, 350-MHz bandwidth on each input
Rapid Systems 433 N 34th, Seattle, WA 98103 (206) 547-8311									**Circle 309**
R3800	100	50	32/32	32/32	16k	16	10	$3,995	PC based
R3600	200	50	32/32	32/32	8k	16	5	$2,495	PC based
R3200	100	25	24/24	24/24	2k	16	40	$1,995	PC based
Tektronix PO Box 4600, Beaverton, OR 97075 (800) 245-2036									**Circle 310**
DAS-92A60	20	20	360/360	360/360	32k to 128k	16	—	$9,990	single module price, entry-level system priced at $19,500
DAS-92A90	20	20	540/540	540/540	32k to 128k	16	—	$12,700	single module price, entry-level system priced at $21,500
DAS-92A16	200	200	384/384	384/384	4k	4	1.7	$8,050	single module price, 32-channel entry-level system priced at $34,000
DAS-92A96	100	400	1,536/384	1,536/384	8k to 128k	16	2.5	$17,950	single module price, entry-level system priced at $30,950
DAS-92HS8	350	2,000	8/160	8/160	8k	2	800 ps	$25,000	single module price
PRISM-30MPX	16.66	200	96/9	96/9	8k	7	—	$7,600	single module price, entry-level system priced at $9,900
PRISM-30HSM	150	2,000	18/20	18/4	12k to 120k	4	2.5	$6,500	single module price, entry-level system priced at $11,000
PRISM-1241	50	100	72/36	72/36	512 to 2k	14	6	$13,900	36-channel system, entry-level system priced at $8,950
PRISM-1230	25	100	64/16	64/16	2k	14	5	$2,995	16-channel system, 64-channel system priced at $6,725
Trace-Tek Instruments 1301 Denton Dr, Carrollton, TX 75006 (214) 446-9906									**Circle 311**
Logic Boy 16C50A	50	50	16/16	16/16	1,024	4	—	$1,795	hand held, battery powered, BNC trigger out, IBM printer port

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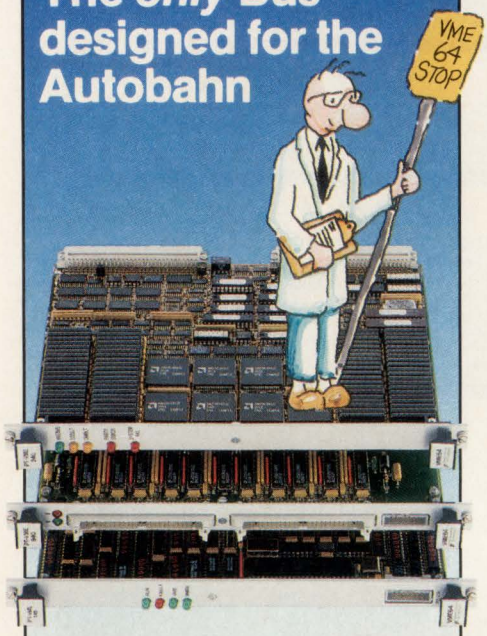

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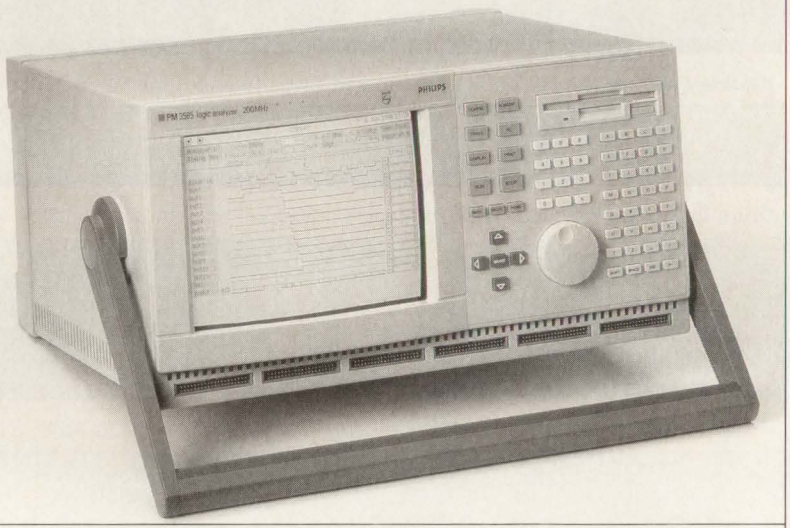
CIRCLE NO. 53

DESIGN AND DEVELOPMENT TOOLS



The Philips PM 3580 logic analyzer series from John Fluke Mfg reduces state and timing measurements to one probe connection. A dual-analyzer-per-pin architecture allows both state and timing data to be acquired simultaneously from the system on up to 96 channels, with just one set of probes. The instrument provides up to 50-MHz state capability, up to 200-MHz timing functions and 2 kbits/channel memory.

and unreliability of attaching multiple probes, this single-probe approach also reduces the excessive loading factors that burden the target system, according to Fluke. The 3580 series' architecture reduces capacitance loading to 7 pF, even when both state and timing information are recorded.

Processor support

Another ease-of-use related issue is processor support. Focusing on this area, the logic analyzers from Hewlett-Packard (Colorado Springs, CO) support over 95 processors and package types. "Package types are a considerable issue, because you have different probing schemes for them," says Greg Peters, product marketing engineer at Hewlett-Packard. The company also tries to maintain its processor compatibility across its entire logic analyzer product line.

Among the latest RISC and high-speed CISC devices are Intel's 80860, 80960 and 80486; MIPS' R3000; Motorola's 68040, 88200 and 88100; and AMD's 29000. Several bus interfaces are supported also, including SCSI, VME A-size and VME VXI B/C.

"While we've had RISC support in the past, customers want overhead," notes Peters. "They want to be able to have 100-MHz state analysis, but at the same time to have full-speed triggering, wider channel count, deeper memory."

Leading Hewlett-Packard's move toward RISC is its latest module, the 16540. Designed for use with Hewlett-Packard's 16500A mainframe, the 16540 provides 16 channels of 100-MHz state and timing analysis. Channel bandwidth can be expanded up to 208 channels using 16541 modules. Both the 100-MHz speed and 10-ns triggering are available across all channels. The device also features 4 kbits of memory on each channel and a variety of user interface options.

Among the user interface choices is a built-in color touch screen. The key contribution of the touch screen is intuitive control of the instrument. Other features can be added without adding more keys. Other user interface options include support for mouse, trackball or keyboard.

Simple triggering

Not letting the machine get in the way is a important theme in logic analyzers. Instruments with triggering sequences that are not straightforward can often distract a user from the task at hand. Arium (Anaheim, CA), a logic analyzer com-

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CIRCLE NO. 54

DESIGN AND DEVELOPMENT TOOLS

pany that targets the low end of the market, offers a logic analyzer that keeps triggering simple by presenting triggering logic options using English words instead of abstract symbols. The screen displays, for example, "If A then B" or "B without C."

By using clear English logic, the user doesn't have to worry about whether '+' means OR or AND.

Arium's ML4400 modular logic analyzer system provides up to 80 channels at 100 MHz or 16 channels at 400 MHz. While the logic analyzer's memory depth is normally 8 kbits/channel, standard capture cards can be added to provide up to 128 kbits/channel. Microprocessor support capabilities can grow by attaching support pods including those for the Motorola 88100-RISC series and the Intel 80960 and 80486. Another option is a 256-kbyte ROM emulator that speeds up code debug by using the target circuit.

Multiple analyzers

While logic analyzers have been noted for being difficult to use, using several logic analyzers simultaneously compounds the situation. To address this, Biomation (Cupertino, CA) chose the Apple Macintosh II as an integral part of its CLAS 4000 Configurable Logic Analysis System. The CLAS 4000 provides graphically oriented windowing for its human interface. Sharing the Macintosh for control and display, the system can be configured with up to four 96-channel logic analyzers in a single chassis. The four logic analyzers can function independently or can be combined into a single 384-channel instrument. User configurable windows allow data from multiple analyzers, in multiple formats, to be displayed concurrently. Time stamping within each module lets displays from different modules be correlated for display.

Each 96-channel logic analyzer module in the CLAS 4000 configuration supports a 200-MHz synchronous data-capture rate. As in the case of other high-end logic analyzers, the highest rates require fewer channels. The 200-MHz rate supports 24 channels, 100 MHz supports 48 channels and 50 MHz supports all 96 channels. Acquisition memory is 4 kbits per channel.

Logic analyzers capture data. But what is done with that data to help a user easily locate a fault can vary among analyzers. "You want to see the cause-and-effect relationship," explains John R. Adam, president of Biomation. "You're looking for either an event, or a sequence of events, and one of the primary functions of a logic analyzer is to allow you to specify that event or sequence of events." The CLAS 4000 architecture is designed so that users can choose those events across the whole width of the instrument. ■

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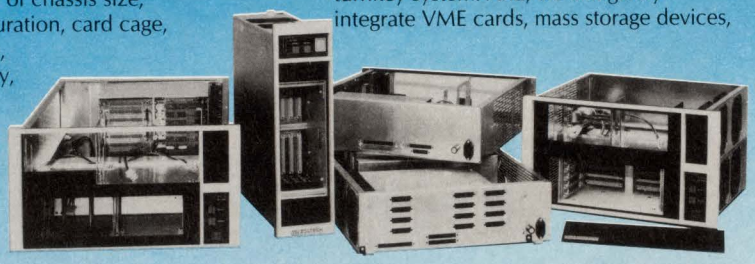

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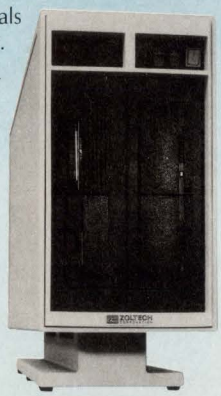

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CIRCLE NO. 55

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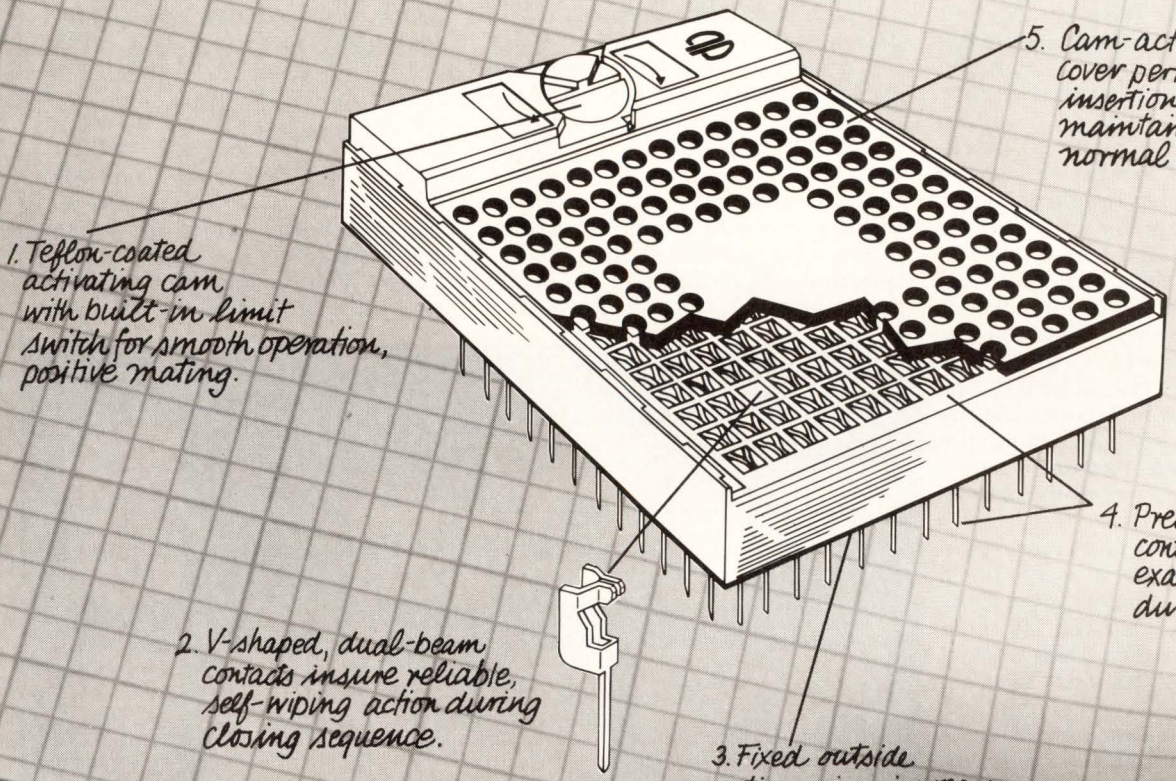

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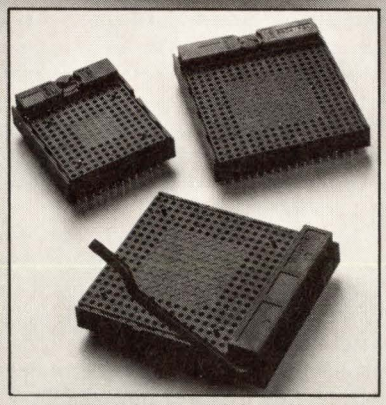

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CIRCLE NO. 56

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DESIGN AND DEVELOPMENT TOOLS

PC-based circuit board design tool incorporates framework technology

Workstation-based frameworks and their associated tools are being touted as the way of the future. The idea of being able to string together a choice of point tools and seamlessly integrate them under a common user interface is indeed an attractive concept. But with all of the attention being given to the high-end, workstation-based solutions, PC-based products have been brushed aside.

OrCAD, a supplier of PC-based circuit board design tools, hopes to change that with the release of ESP, a graphical design environment that it has integrated with Release IV of its DOS-based tools. OrCAD says the ESP framework improves the performance of the product line by providing easy tool selection, file management and automatic transfer of design information between software packages.

"A true framework is more than just a shell that lets a user pull up different tools," says John Durbetaki, CEO at OrCAD. "It must provide process control, that is, any action chosen by the user must set off multiple events. The database behind the framework must be a coherent force behind the design environment that lets a user change his view of a design from schematic capture, for instance, to layout in an integrated fashion."

The ESP framework provides links between different tools that are designed to transfer information about the design from one format to another. After a designer has created a schematic, for instance, ESP will automatically transfer the netlist, part and test vector information from the schematic file to the simulator to produce a graphical timing of the design. In addition, the framework is compatible with software from other vendors, including word processors and spreadsheets. Configuration menus let the user tailor the interface to accomplish user-defined tasks.

Enhanced tools released

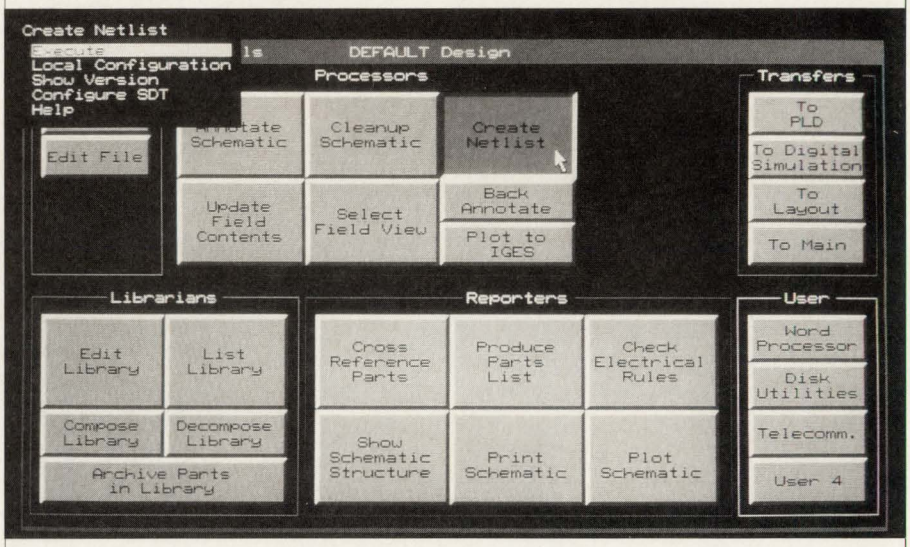
Along with the ESP framework, new versions of six OrCAD tools are being released. The schematic design tool set (STD) supports over 20,000 parts (compared with 6,200 in previous versions), including IEEE symbols, which can now be as large as 12.7×12.7 in. Common parts in TTL, ECL and CMOS, from simple gates to microprocessors, can be called up and placed either by keying in the part name or via the browser command. Other libraries for special tasks can be generated using OrCAD's graphical library object editor or purchased from third parties.

The new version of the verification and simulation tool set (VST) automatically takes information from the schematic created in STD and places it in the simulation editor. The tool also features on-line error checking and utilities for test vector generation. The new release includes a netlist format that supports incremental design changes. OrCAD says this feature increases the speed of the simulation cycle by up to two orders of magnitude over the previous version.

The updated version of the printed circuit board design tool (PCB) includes a new graphical interface, semiautomatic and automatic placement, improved speed, increased surface-mount technology support, and a larger library of modules. The ESP framework improves information-passing capabilities between PCB and STD.

A new version of the programmable logic design tool set (PLD) features an updated compiler with greater capacity and support for open architectures. Information-passing speed between PLD and other tools has also been increased.

OrCAD's modeling program (MOD), which creates VST-compatible models for simulating PLDs, now includes enhanced debugging, as well as better optimization and code generation to eliminate redundant gates. The tool reads standard JEDEC files created by OrCAD's PLD or other PLD design tools and uses the information to create simulation models of the programmable devices. The models are then exercised with models of all the other components in a circuit to produce a single, timing-based, board-level simulation. The new version also includes extensions to the definition language.



ESP and all the new integrated products will be available by the end of the fourth quarter. ESP will be sold with STD for $595. Other products will be priced as follows: VST at $995; PCB at $1,495; PLD at $495; and MOD at $495. —*Mike Donlin*

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Circle 354

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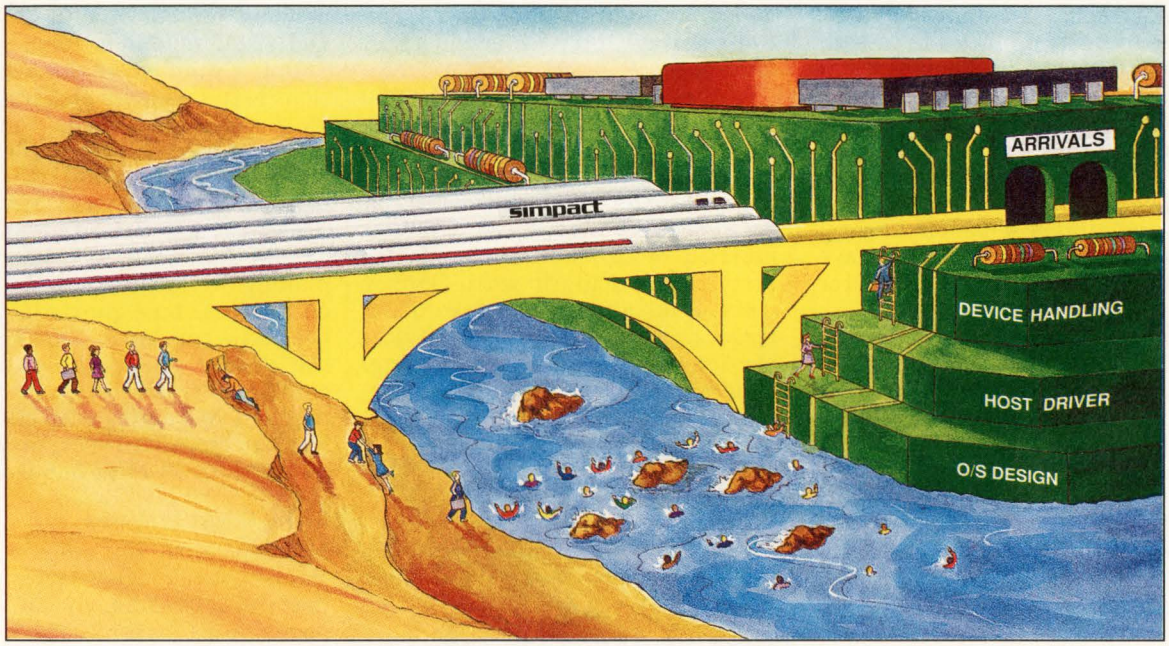

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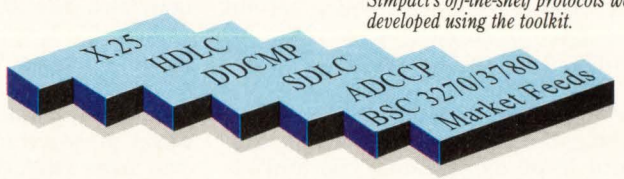

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CIRCLE NO. 57

INTEGRATED CIRCUITS

PC chip set provides more-sophisticated cache architecture

The first round of core-logic chip sets for 33-MHz 386 personal computers followed a fairly predictable pattern. The parts were speed upgrades on existing 25-MHz designs, some of which supported caches and some of which didn't. But even when these chip sets did offer cache controllers, the caches tended to be relatively small and simple. This left a hole in the market, into which several system vendors rushed with faster, more complex cache designs.

A key feature in these discrete implementations was a copy-back strategy, in which the CPU would write only to the cache on a write hit, and the cache would copy the new data back to memory only when absolutely necessary. This plan makes for a more complex cache controller, but its supporters claimed around a 15 percent improvement in system throughput—a claim that quickly was both proved and disproved by benchmarks, of course.

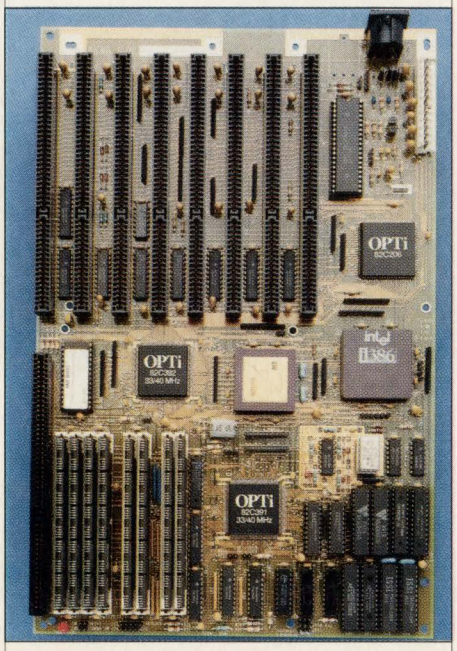
But a number of things have changed since those early 33-MHz parts appeared. On the technical side, chip set vendors are beginning to move to 1-μm CMOS processes, allowing both more speed and more complexity in their critical loops. Second, as CPU speeds increased, the difficulty of routing fast signals through the handful of chips necessary for a discrete cache began causing design headaches and system reliability issues. Third, the market has grown increasingly competitive, with far too many vendors chasing the 386 DX with far too few differentiating features.

Now Opti, the Chips & Technologies spin-off that cut a place for itself with the first 33-MHz cache-based DX chip set, is back with what it claims to be a second-generation part, the 386WB. For Opti, "second generation" means a number of things, all related to speed.

A new cache design

First, stealing from the earlier discrete implementations, the 386WB chip set includes a write-back cache controller. "The main reason for a second generation is that we can get 12 to 15 percent better performance from a superior cache architecture and some additional features," says Raj Jaswa, Opti vice-president of marketing.

The new cache controller in the 386WB is a relatively straightforward design. It implements a large—32- to 256-kbyte—direct-mapped cache with external tag and data SRAMs. "We chose a direct-mapped design because on faster systems, particularly when OS/2 or Unix is an issue, people are using larger caches," says David Lin, vice-president of systems engineering. "And once you get above 64 kbytes, there's little difference in hit rate between direct-mapped and set-associative caches. But direct-mapped controllers can have looser timing."



To keep speed up and tag RAM cost down, Opti chose a 16-byte line size. But the 16-byte lines risk an unhealthy lengthening of the miss penalty, so the designers included a burst fill operation in the cache and memory controllers. The burst operation places the CPU in wait state and uses DRAM fast page mode to pump 4 bytes out of main memory every two clock cycles.

There are useful systems-oriented features, such as a local-device input that suppresses the cache controller when a local-bus peripheral has been addressed. The controller offers two programmable noncached address ranges to avoid obvious problems with I/O areas, DMA buffers, and so forth.

But a number of the sophistications found on more elaborate workstation-oriented cache controllers are missing. One example is bus snooping—essential on look-through caches, where DMA activity doesn't reach the local bus. Opti avoids the need for snooping by making all memory activity happen on the local bus, guaranteeing that the cache can see it. This simplifies the design considerably, but precludes multiprocessing, or overlapping of DMA cycles with cache hits. Neither limitation is currently a big issue in the 33-MHz 386 market.

The latest features

In addition to the more advanced cache controller, Opti has made sure that the 386WB has the latest list of neat chip set features. These include use of hidden refresh modes on DRAMs, which Jaswa says cuts 90 percent of refresh overhead. Not only main BIOS but video BIOS can be shadowed, and video BIOS can be cached, options that Opti claims can speed up screen-intensive operations by 40 percent.

A hardware Gate-A20 feature monitors traffic to the keyboard controller, traps the Gate-A20 operation that IBM uses to shift into extended memory, and emulates the shift in a few nanoseconds. This can give substantial speed improvements in those environments where the system must move frequently in and out of protected mode. Finally, the parts offer the customary array of memory remapping, fast bus control and power-conservation features. BIOS support will be coming from a variety of standard suppliers.

The 386WB chip set is in production now. Sets will cost $75 in 10,000-piece orders. —*Ron Wilson*

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Circle 351

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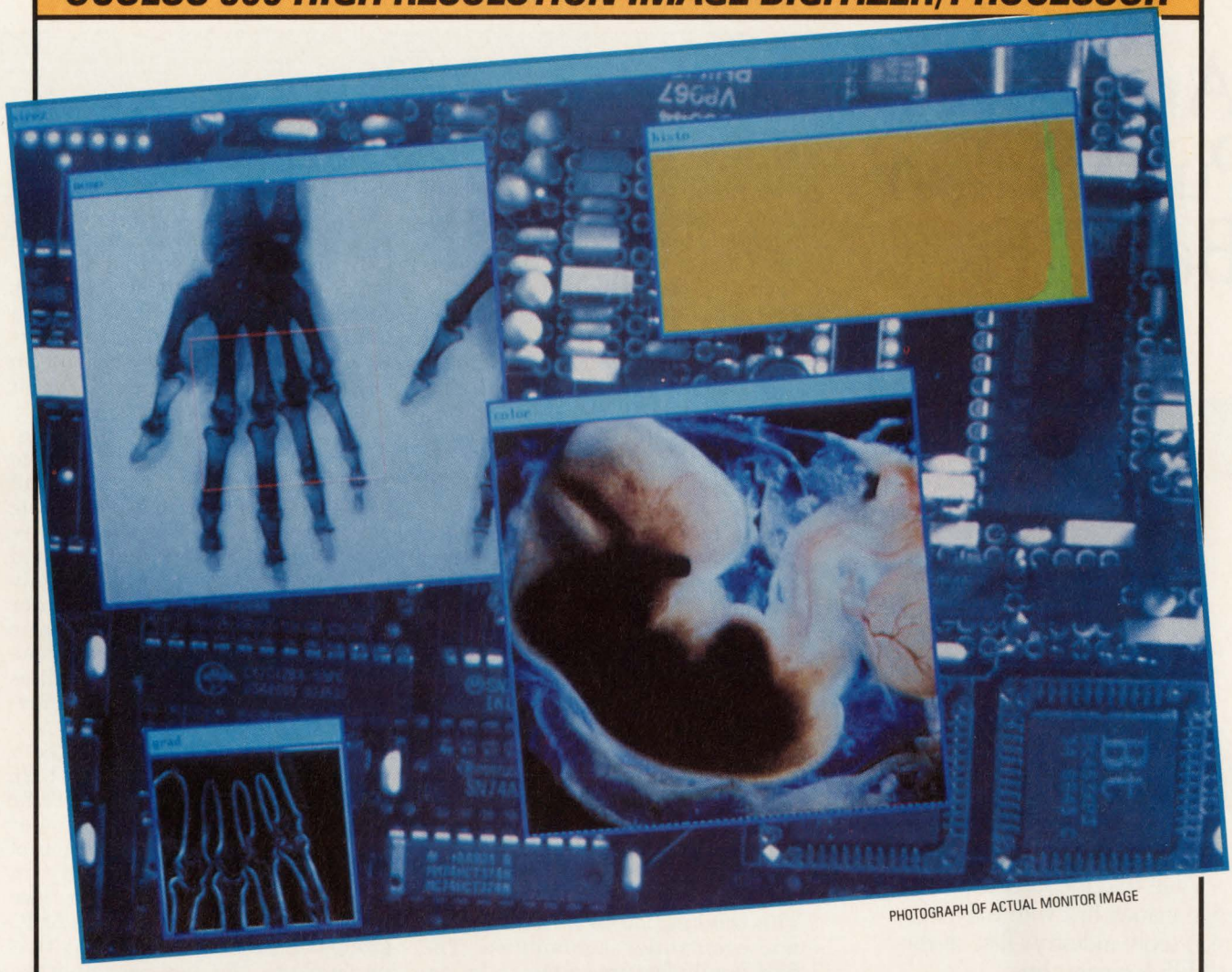

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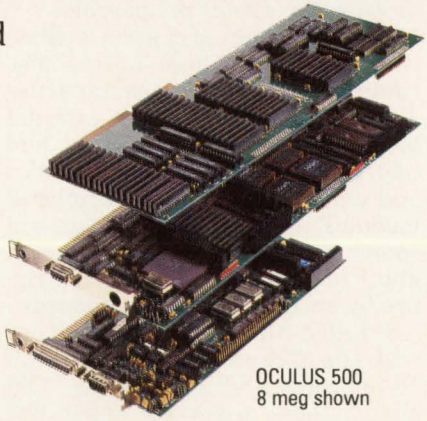

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CIRCLE NO. 67

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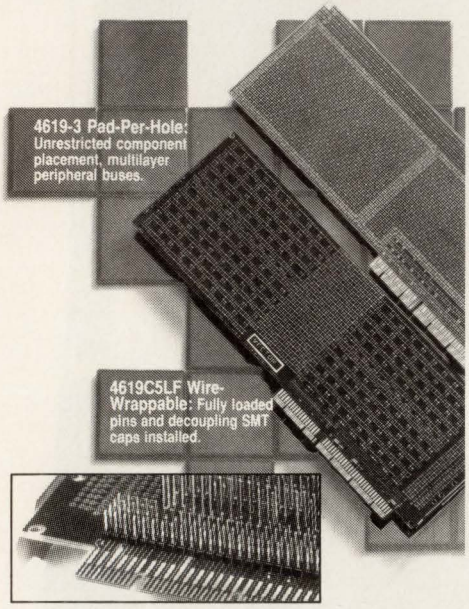

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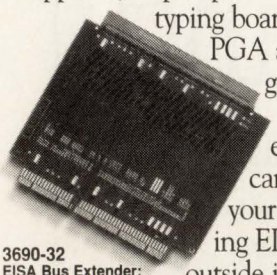
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CIRCLE NO. 68

INTEGRATED CIRCUITS

Oki unveils 8051-like controller family

Two unrelated concepts have been gaining popularity in the midrange microcontroller market lately. One is the idea of deriving new products from the venerable 8051 architecture. The other is the idea of a more-or-less compatible family of microcontrollers, reaching from a pure 8-bit, low-cost part to a pure 16-bit, high-speed part. Now Oki Semiconductor has combined the two ideas into a new product line—a nearly 80C51-compatible family of 8-bit and 16-bit microcontrollers.

Oki believes that what people need is not just a better 8051 but an entirely new family of components. The new devices should take advantage of the speed possible with today's processes and designs. And the family should offer the benefits of modularity derived from modern silicon design tools—the parts should be available as standard products, customer-specific products or application-specific standard products, using a cell library to cut and paste what the customer wants.

Three subfamilies

This thinking led Oki to a set of three microcontroller subfamilies. The 65K family features a pure 8-bit design—core and bus—with a 400-ns cycle time. Oki estimates the part will be about twice as fast as a 12-MHz Intel 8052 on typical code. (Typical here means the control code for a dot-matrix printer.) The 65K family's initial members will offer from 4 to 16 kbytes of on-chip ROM, 128 to 384 bytes of RAM, and the usual sorts of 8-bit peripherals.

The second group of parts is called the 66K family. These devices, also running on a 400-ns cycle time, use a 16-bit core and an 8-bit external bus—a combination of speed and cost savings. The 66Ks would also add some more elaborate peripheral modules. Initial 66K offerings will sport up to 32 kbytes of ROM and 1 kbyte of on-chip RAM, a sizable figure by current industry standards.

Finally, the family rounds out with the 67K parts, which have full 16-bit cores and 16-bit buses. Oki claims these parts are about five times faster than the 8051, and even noticeably faster than Hitachi's H8/330. The announced member of the 67K family has 16 kwords of ROM, 512 bytes of RAM and the usual peripherals. Extensions to the 67K line are planned that will enlarge the chip's external address space—the existing parts have a limit of 64 kbytes—and will add currently popular options such as an on-chip I/O processor and a 10-bit analog-to-digital converter.

The families share similar instruction sets, all based on the 80C51 model. None of the parts will be exactly code- or pin-compatible with the 8051. All of the parts share a basic design tool environment, and there are point tools for each family as well. These include a C compiler for the 67K, and semiautomatic 8051-to-Oki code translators for the 65K and 67K families. All families will initially be represented by one-time-programmable parts.

The company has also hatched a novel scheme to help customers take advantage of the customer-specific potential of the parts. If a customer wants a particular configuration of peripheral options not currently in production, Oki will supply a base microcontroller chip, and Oki's ASIC group will provide a gate array that implements the new peripherals. The company will guarantee functional and timing compatibility between this two-chip set and the finished standard-cell customer-specific microcontroller. The ability to customize functional blocks on the microcontroller die should be available by early 1991, according to Oki. The company also sees the possibility of combining the microcontroller cores with major functional units in the standard-cell repertoire.

Prices for the microcontrollers range from under $3 for the least expensive 65K parts to $6.50 for low-end 66K devices and around $7 for starter 67K chips. These prices are for 10,000-unit quantities.

—Ron Wilson

Oki Semiconductor
785 N Mary Ave
Sunnyvale, CA 94086-2909
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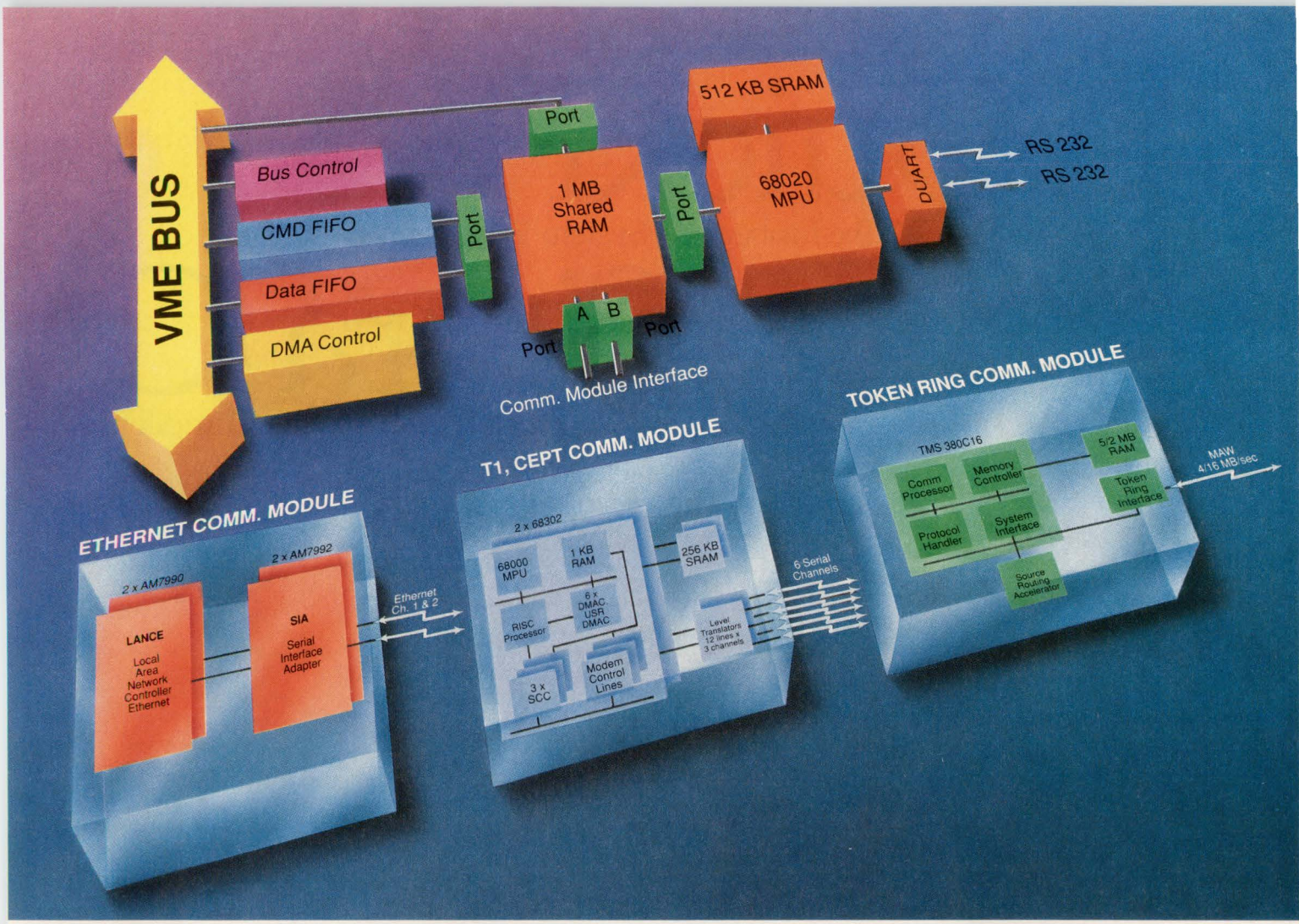
Circle 356



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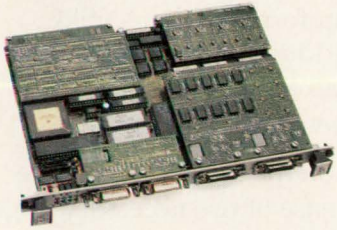

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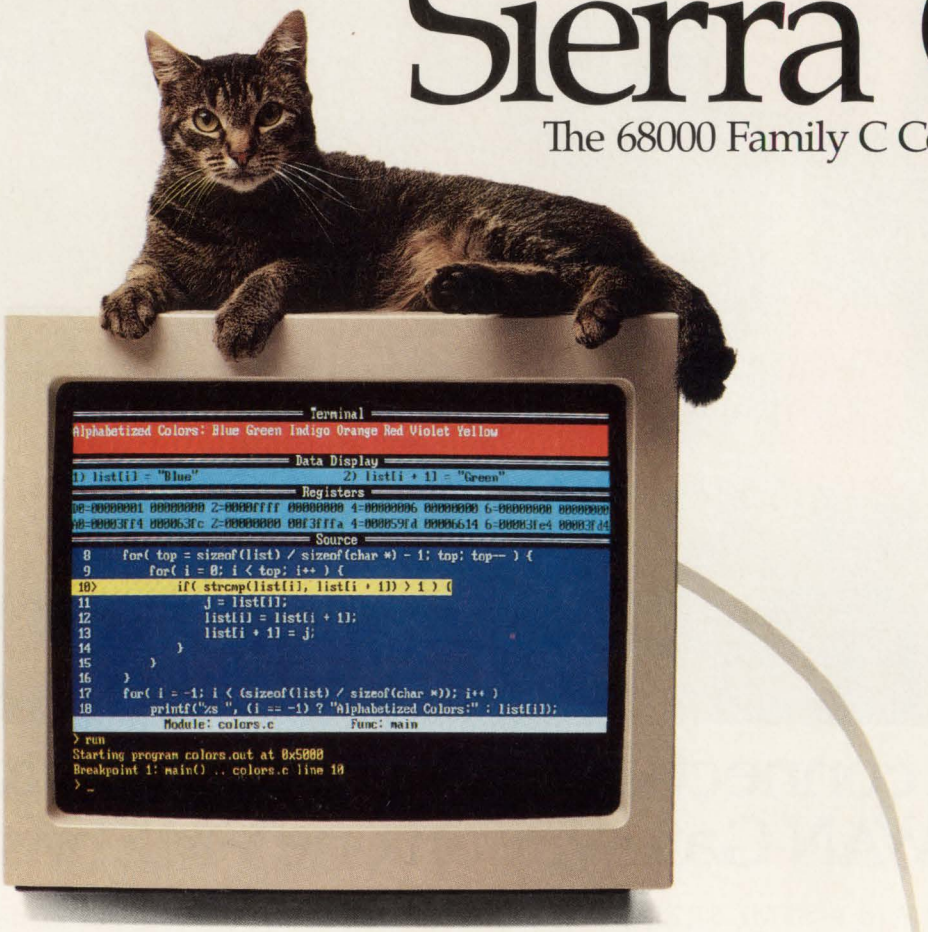

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CIRCLE NO. 59

COMPUTERS & SUBSYSTEMS

32-bit DSP board delivers 25-MFlops on STD Bus

The MCM-DSP32C digital signal processing board from WinSystems is the first 32-bit floating-point STD Bus board based on the AT&T DSP32C. At 25-MFlops, the board gives STD Bus users a performance level suited for computation-intensive applications such as signal and waveform analysis, process control and scientific calculations.

At the heart of the board is the DSP32C, AT&T's 32-bit CMOS floating-point processor. Rated at 25-MFlops, the chip features four 40-bit accumulators, 22 general-purpose registers and 6 kbytes of internal RAM.

Operating at a clock frequency of 50 MHz, the MCM-DSP32C is available with either 64 or 256 kbytes of high-speed RAM. This 25-ns memory permits 32-bit-wide, zero-wait-state operation at 50 MHz. Noting key benchmarks, WinSystems claims the board can execute a complex 1,024-point fast Fourier transform in 3.3 ms, and a 4×4 matrix multiply in 6.16 μms.

While data transfers between the DSP and the host occur at 3.5 Mbytes/s, programmed I/O frees the board's execution from interference from the STD Bus host CPU. The board supports either 8- or 16-bit data transfers to the STD Bus.

Daughterboard adapters

Because users' DSP application requirements vary, the MCM-DSP32C features a daughterboard adapter. Users can choose between four I/O daughter cards. The DBCS5339 daughterboard provides a 16-bit dual-channel 48-kHz delta sigma A-D and anti-aliasing filters for spectral analysis and filtering applications. The DBSerial board contains an interface to the DSP32C serial I/O channel. The DBProto board is for customers who need to design special-purpose interface electronics to the DSP board. While these daughter cards let users match application requirements with hardware, no daughterboards are required to use the MCM-DSP32C as a general-purpose math accelerator.

WinSystems supports programming and debugging for the board with D3EMU software, which runs on WinSystems' 80286 or 80386 STD AT-based system with the MCM-DSP32C installed in the same card cage.

Available now, the MCM-DSP32C is priced at $1,495. —*Jeffrey Child*

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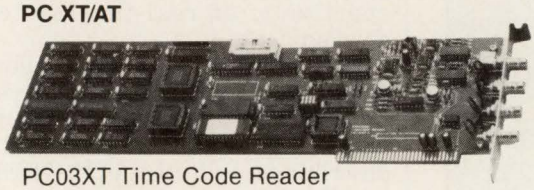
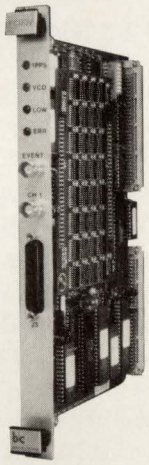
BUS LEVEL TIME CODE PRODUCTS

PC XT/AT



PC03XT Time Code Reader

VME bus



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VMEbus:
PC03V Time Code Processor
PC26V Time Display

Other:
M80D-LU Time Display
Synchronization App. Note
Model 9390 GPS Satellite Receiver

CIRCLE NO. 60

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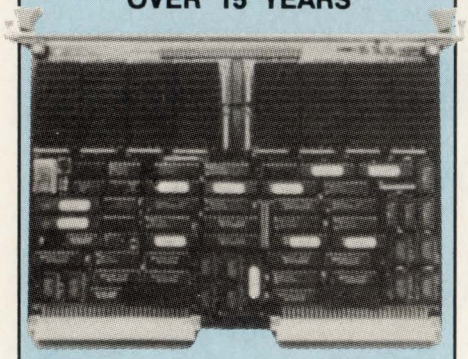

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CIRCLE NO. 61

SOFTWARE

Development module supports knowledge-based real-time systems

A development environment for knowledge-based real-time software lets system designers incorporate rule-based logic into systems that also use numeric computations in real-time applications. RT/Expert from Integrated Solutions is the latest addition to that company's family of CAE/computer-aided software engineering products. The family includes Matrix, SystemBuild, AutoCode, and AC-100, products that are used in the design, simulation, code generation, and testing phases, respectively, of real-time system development.

SystemBuild, for example, allows designers to graphically describe control structures based on numeric values. RT/Expert adds a method of describing a collection of IF-THEN-ELSE rules that can be based on an expert's knowledge and experience and used for diagnostics, monitoring, filtering, and mode selection applications. Such rules are particularly helpful for defining control logic for systems with imprecise dynamics or systems so complex they may present apparently ambiguous situations. RT/Expert can be used to represent the expertise of a skilled operator to sort out the options presented by numeric computations.

With RT/Expert working alongside SystemBuild, logical relationships between inputs and/or historic information (the expert's rules) are examined to evaluate the IF part of a control structure. Mathematical and logical operations can be performed in the THEN-ELSE structures in the same manner as normal control engineering practice. In this manner, the expert knowledge is used to define the condition that must be dealt with not only in terms of the current numeric input values, but also in terms of what those current values may mean to the system in a broader context, that is, in the light of an expert's experience. The THEN-ELSE branch decision can then be mathematically precise but intelligently chosen.

Like the entire Integrated Solutions CAE/CASE family of products, RT/Expert targets process control, manufacturing and petrochemical applications, especially in areas where monitoring functions must be combined with some sort of diagnostics or intelligent alarm system. Prototyping is assisted with the interactive animation module of SystemBuild that lets the designer set up a graphical control panel or representation of a physical plant and monitor its actions via changes in color, meter movements, etc. RT/Expert can monitor simulated inputs, make decisions based on them and let designers view the results in the same way they can under SystemBuild.

Prototyping by modules

Rapid prototyping is made easier, even when all the modules of a system are not fully understood. RT/Expert can be used to approximate the modules' behavior, and then the models created with it can be gradually refined. Control structures originally defined using RT/Expert's flexible logic can also be replaced later with numeric-based SystemBuild blocks if it turns out that the system, once better understood, lends itself to a numeric or Boolean solution.

RT/Expert's rule system makes it possible to generate self-testing or other control scripts that can become part of an embedded system. The RT/Expert module is capable of generating optimized Ada or C code in the same way as other discrete SystemBuild models. Control structures can be set up in a hierarchical way with a large "macro" structure decomposed into several layers of detail that can be mixes of RT/Expert blocks and other numeric or Boolean blocks.

RT/Expert, available immediately to run on Sun-3, Sun-4, Sparcstations, Vax, and Apollo workstations, is priced from $10,000.

—Tom Williams

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Circle 355

1991 Computer Design Magazine Edition UPCOMING ISSUES

Watch for these Special Features & Events in Computer Design Magazine

MONTH	SPECIAL REPORT	TECHNOLOGY FOCUS	PRODUCT FOCUS
January 1	30th Anniversary Issue — The Evolution Of Electronics Into Computers *COMPUTER DESIGN* editors		Logic analyzers *Jeff Child*
February 1 Buscon-W	Workstation buses *Warren Andrews*	FDDI ICs — *Ron Wilson* Design capture — *Mike Donlin*	High-speed D-A converters *Jeff Child*
March 1*	Fuzzy logic in embedded control *Tom Williams*	Mixed CMOS, ECL & BiCMOS — *Barbara Tuck* LAN controllers ICs — *Ron Wilson*	VME CPU boards *Jeff Child*
April 1 Electro	PCB layout tools *Mike Donlin*	Communication with standard buses — *Warren Andrews* Designing ASICs for testability — *Barbara Tuck*	Static RAMs *Jeff Child*
May 1* CICC Comdex	Superfast processors *Ron Wilson*	High-level design languages — *Mike Donlin* Object-oriented programming — *Tom Williams*	Emulators *Jeff Child*
June 1 DAC	Design synthesis *Barbara Tuck*	Mil-Spec standard buses — *Warren Andrews* Disk controller ICs — *Ron Wilson*	Op amps *Jeff Child*
July 1	CASE for real-time programming *Tom Williams*	Mezzanine buses — *Warren Andrews* Device modeling — *Mike Donlin*	Multibus CPU boards *Jeff Child*
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November 1 Wescon ITC	System simulation and verification *Mike Donlin*	High-density ASIC packaging — *Jeff Child* Multiprocessing in real-time — *Tom Williams*	STD CPU boards *Jeff Child*
December 2	Migrating PLDs to full ASICs *Barbara Tuck*	Accelerators to boost standard-bus performance *Warren Andrews* 8- and 16-bit microcontrollers — *Ron Wilson*	High-resolution A-D converters *Jeff Child*

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COMPUTER DESIGN Technology and Design Directions

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CIRCLE NO. 90

IN THE ERA OF MegaChip™ TECHNOLOGIES

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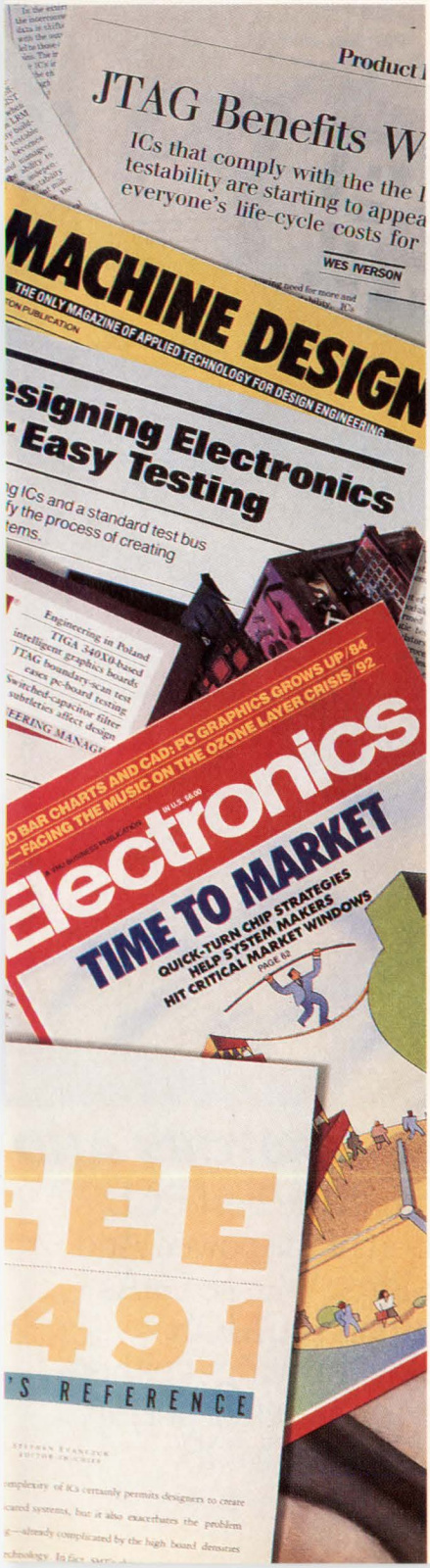
testability, but only one it. Texas Instruments.



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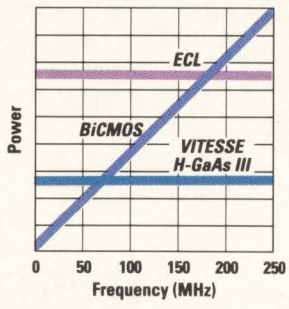

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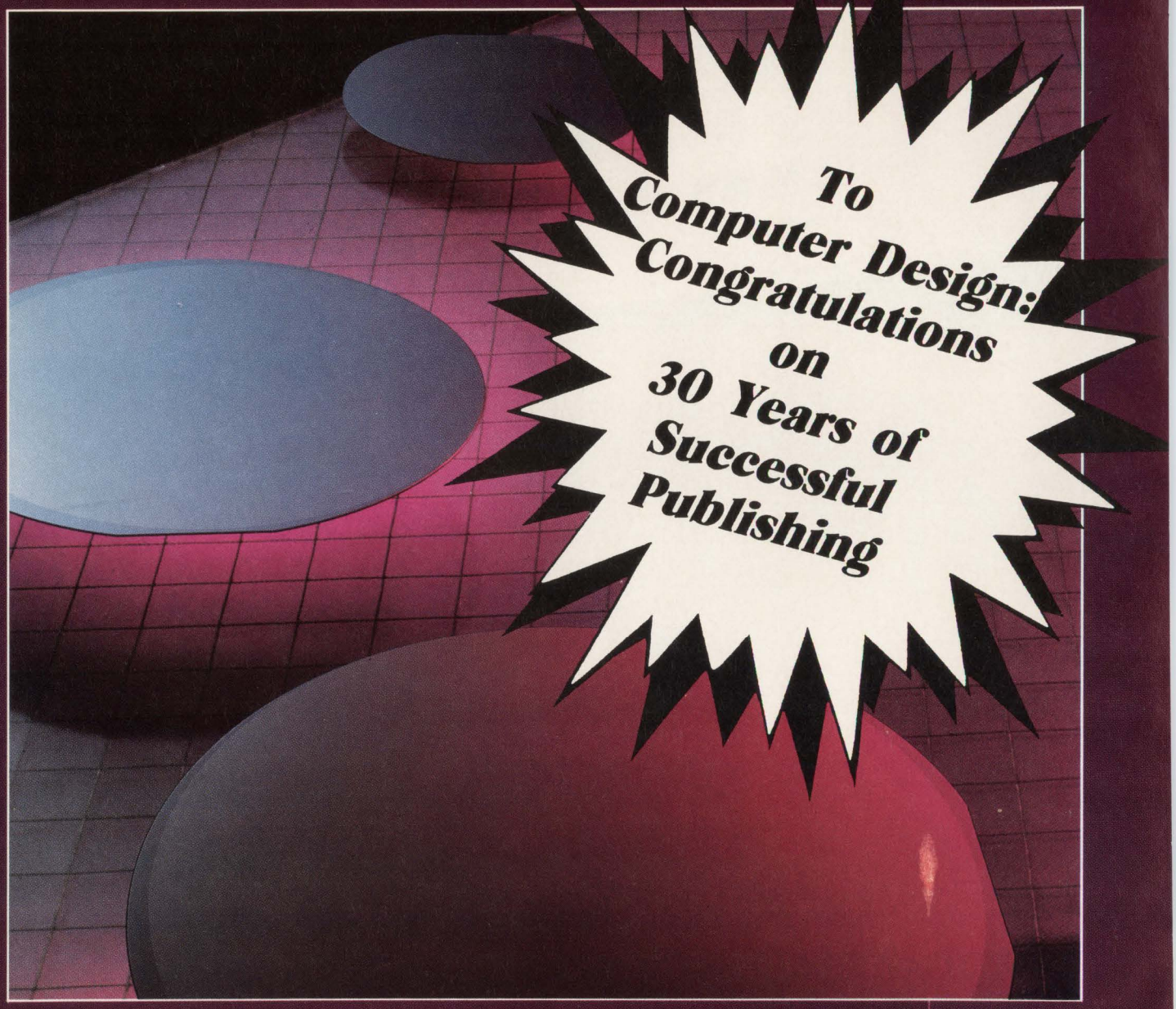
Worldwide Semiconductor Production

November 1990



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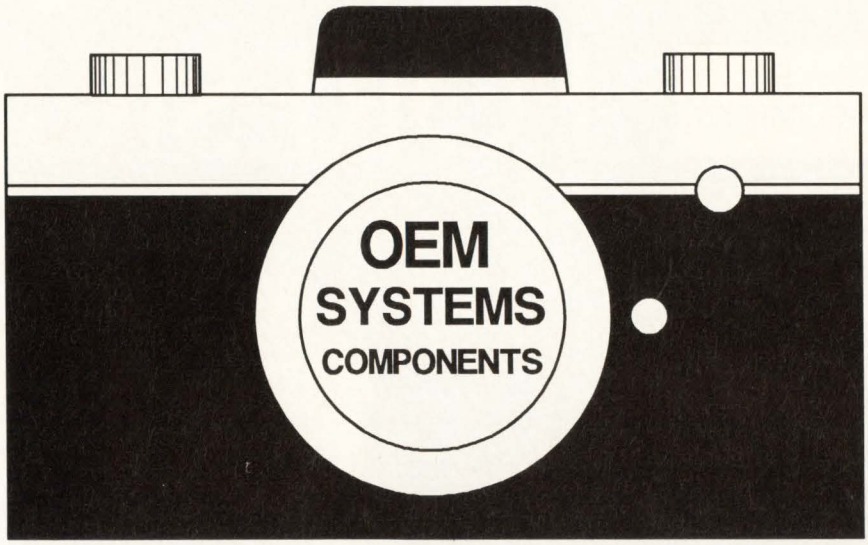

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40 FORESIGHT

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- VME Rev C IEEE1014:
  - System Controller
  - Interrupter and handler
  - 16 vectored interrupts
  - DTB Master/Slave
  - BLT transfers • 4Kb Mailbox
- VSB Master/Slave
  - Interrupter and handler
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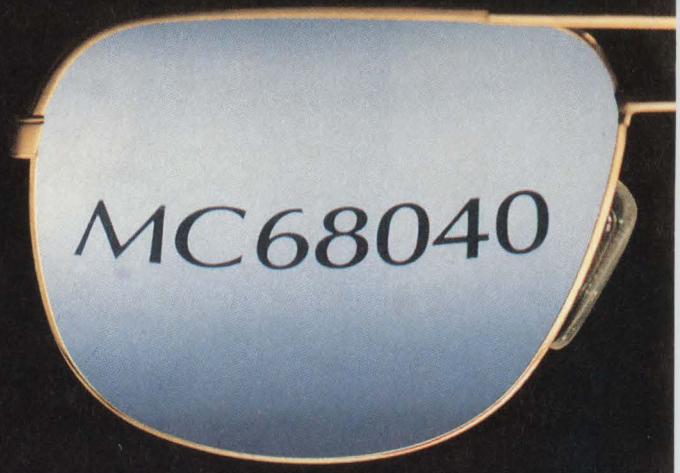

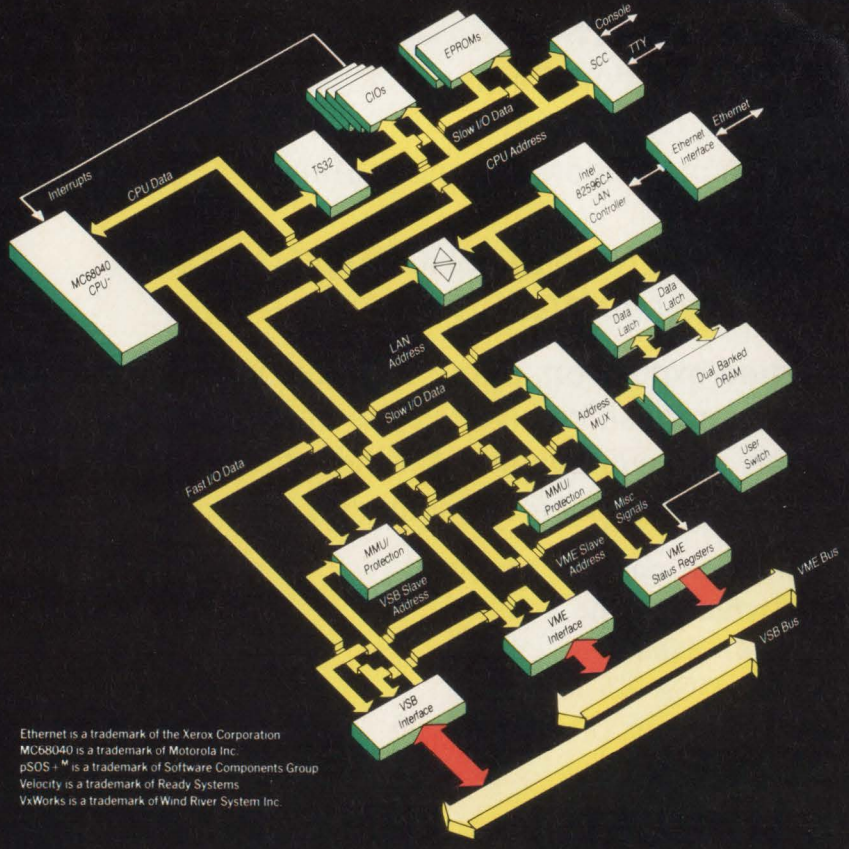

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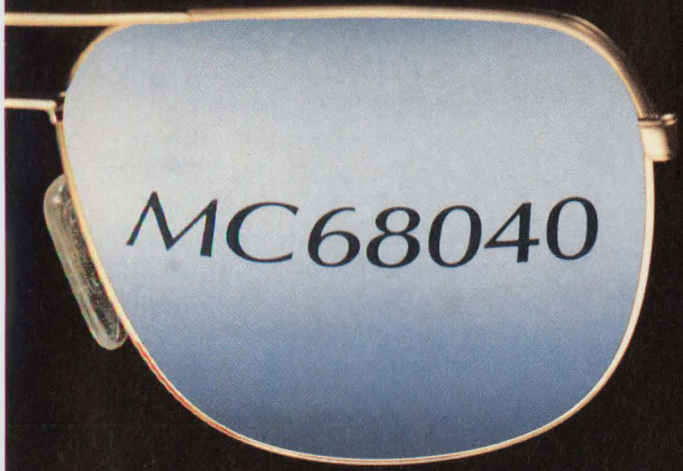

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- VME Rev C IEEE1014:
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  - Interrupt handler
  - 4Kb Mailbox
  - DTB Master/Slave
  - BLT transfers
- SCSI interface on P2. 32bit DMA and NCR 53C90A achieving sustained data transfers up to 4.5Mb/sec
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- RTC with 2Kb SRAM
- 8bit user I/O
- 2 x RS232 • 2 x CIO
- 6 x Counter/Timers
- Software support includes:
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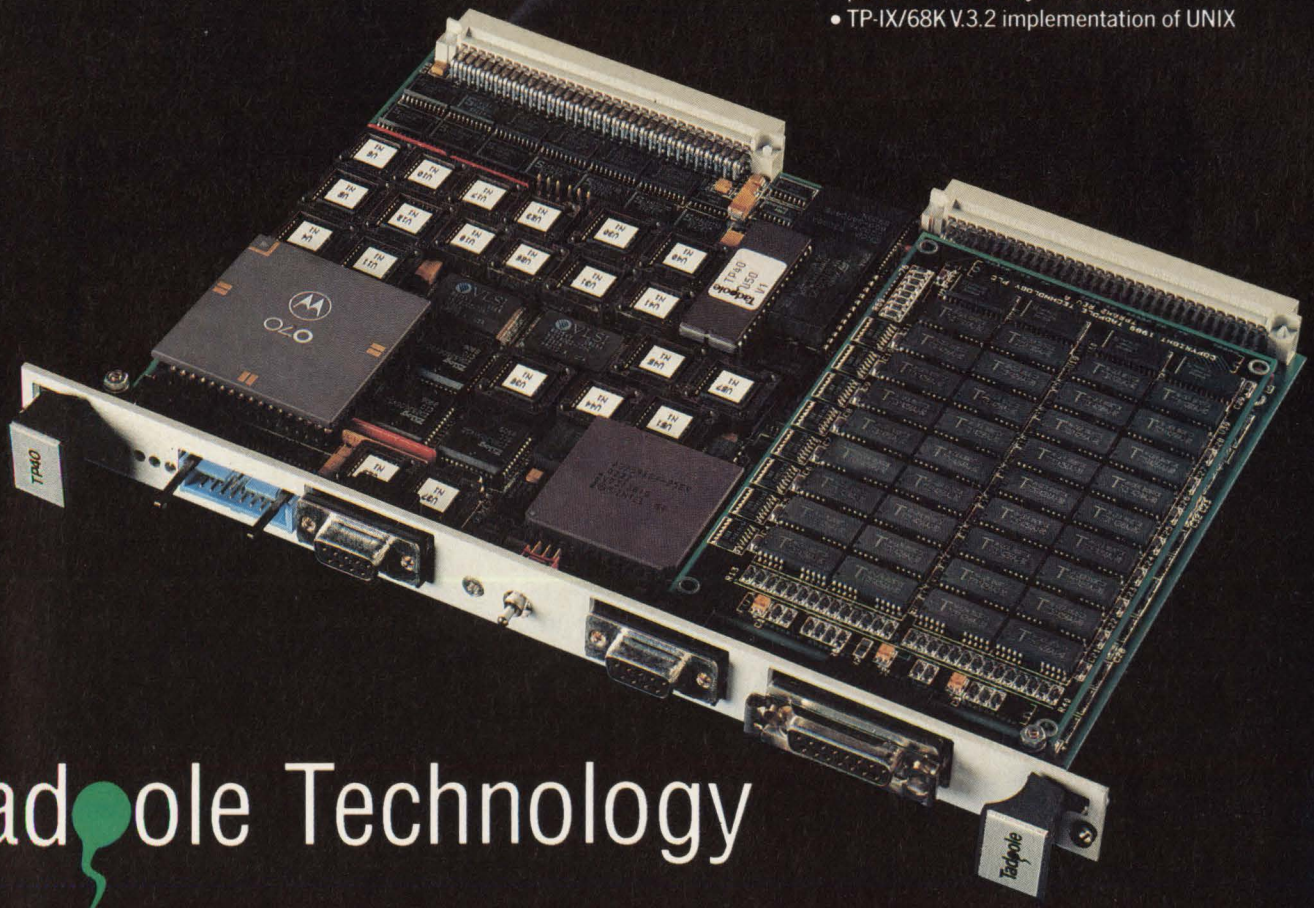
  - TP-IX/68K V.3.2 implementation of UNIX



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Tutorials: Proposals are solicited for one or two hour educational tutorials covering ASIC fundamentals, mixed signal design, timing and logic synthesis, design for testability, VHDL, managing ASICs, and manufacturing considerations. Contact the Tutorial Chairman:
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INSTRUCTIONS TO AUTHORS:

Authors for papers, tutorials, and workshops are asked to submit six copies of a review package, which includes a 500 word summary and a 50 word abstract, typed single-spaced on a 8-1/2 x 11 white paper for paper selection purposes. Author's name, affiliation, complete mailing address, telephone number and telex/fax MUST appear on the summary. The summary should clearly state: 1) Title of the paper; 2) The purpose of this work; 3) The major contributions to the art; 4) The specific results and their significance; and 5) Technical area.

HIGHLIGHTS

- **Workshops (2 days)**
- **Tutorial Sessions**
- **Technical Papers**
- **Technical Exhibits**
- **Proceedings of Papers/Tutorials**
- **Evening Panel Discussion**
- **Spouse Program**

Send Technical Proposals to:
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170 Mt. Read Blvd.
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Fax: (716)436-9370

* Summaries and proposals deadline: **March 1, 1991.**
* Notification of Acceptance: **April 15, 1991.**
* Final Camera Ready Manuscript by **June 10, 1991,**

Further information may be obtained from:

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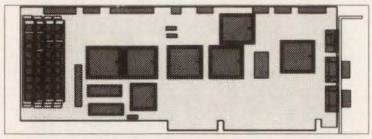

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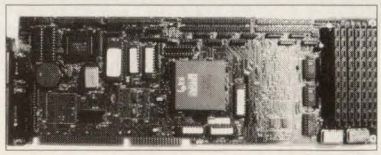

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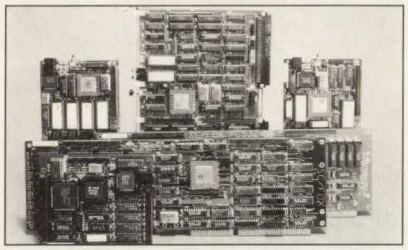

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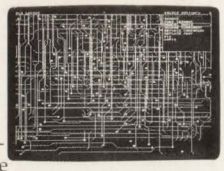

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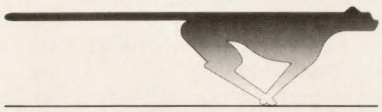

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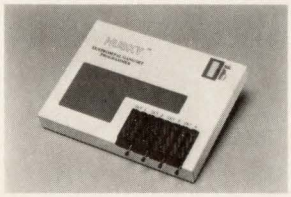

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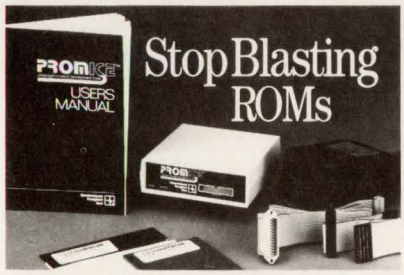

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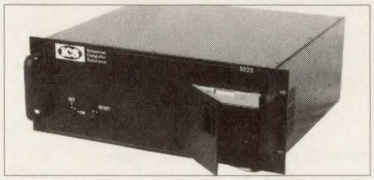

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April 1 Electro	PCB layout tools *Mike Donlin*	Communication with standard buses — *Warren Andrews* Designing ASICs for testability — *Barbara Tuck*	Static RAMs *Jeff Child*
May 1* CICC, Comdex	Superfast processors *Ron Wilson*	High-level design languages — *Mike Donlin* Object-oriented programming — *Tom Williams*	Emulators *Jeff Child*
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Fax: 89-904 35 26

Italy
Luigi Rancati
Rancati Advertising
Milano San Felice Torre 5
20090 Segrate Italy
Tel: (02) 70300088
Telex: 328601 RANCAD I
Fax: (02) 70300074

Japan
Sumio Oka
International Media Representatives, Ltd.
Room 100, 21 Bldg.
Z-2-22, Okusawa
Setagaya-ku, Tokyo 158
Tel: 03-502-0656
Telex: J22633 MEDIAREP
Fax: Tokyo 5706-7349

Jay G. Seo
Yong-Jin Park
Doobee International, Ltd.
Center Building (Byulgwan)
1-11 Jeong-dong, Choong-ku
CPO Box 4557
Seoul, Korea
Tel: 776-2096
Telex: K27117 DOOBEES
Fax: 755-9860

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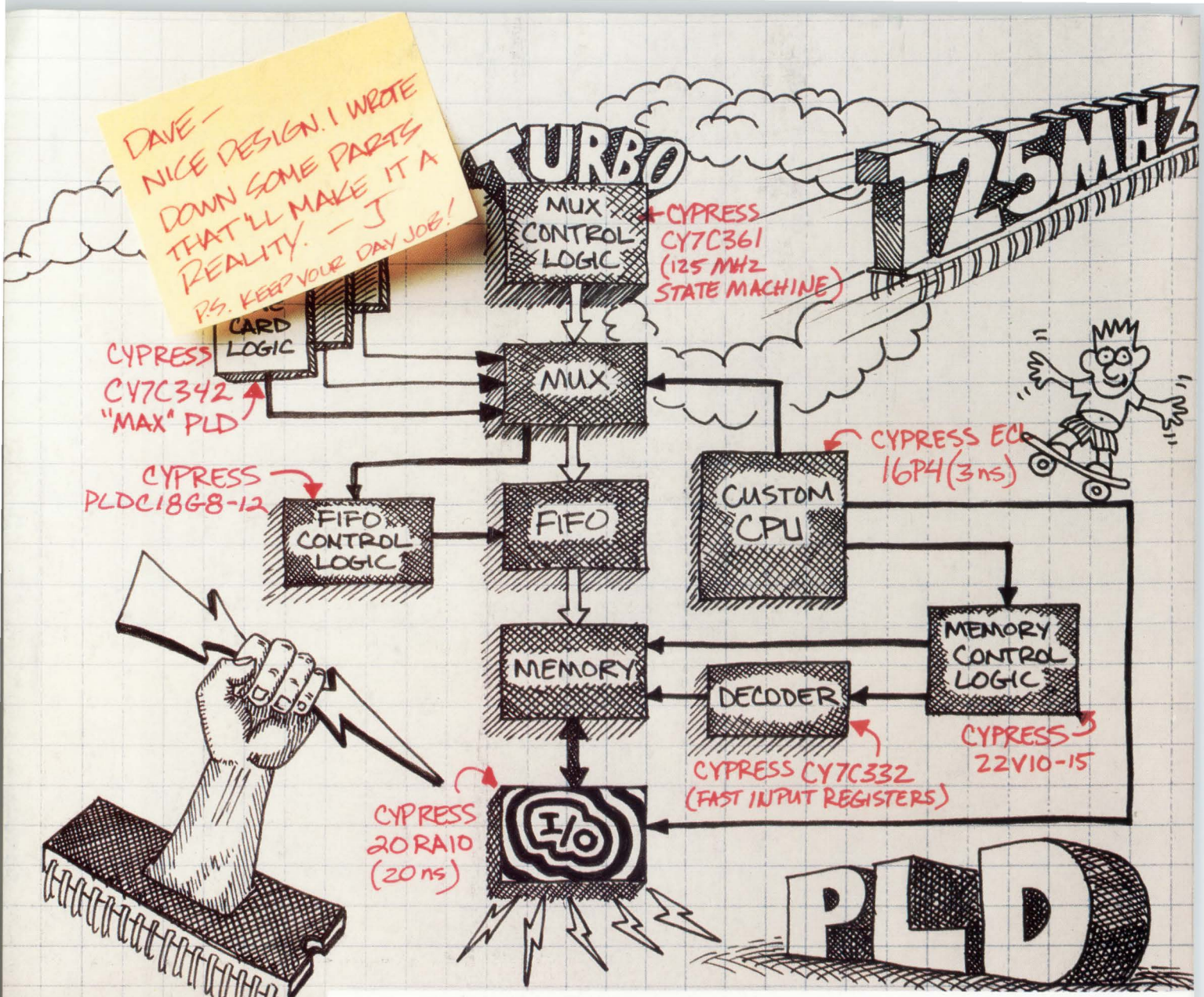

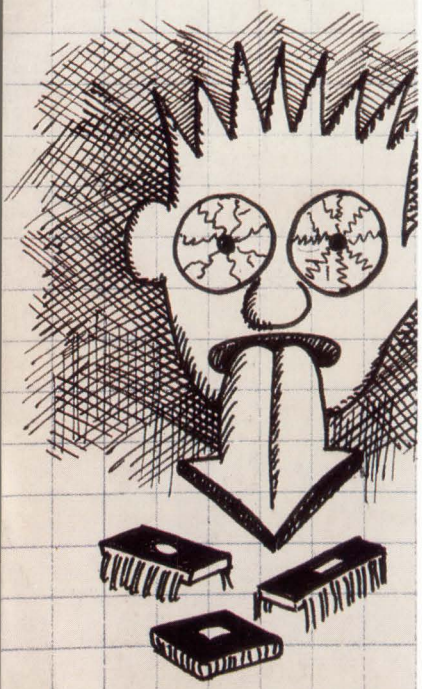

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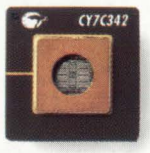

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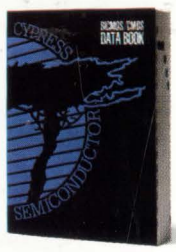

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