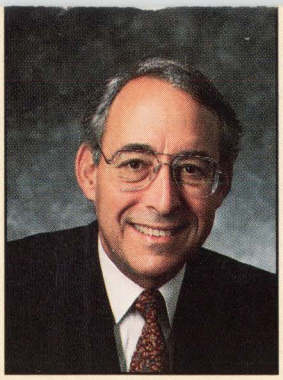
A PENNWELL PUBLICATION JULY 1991

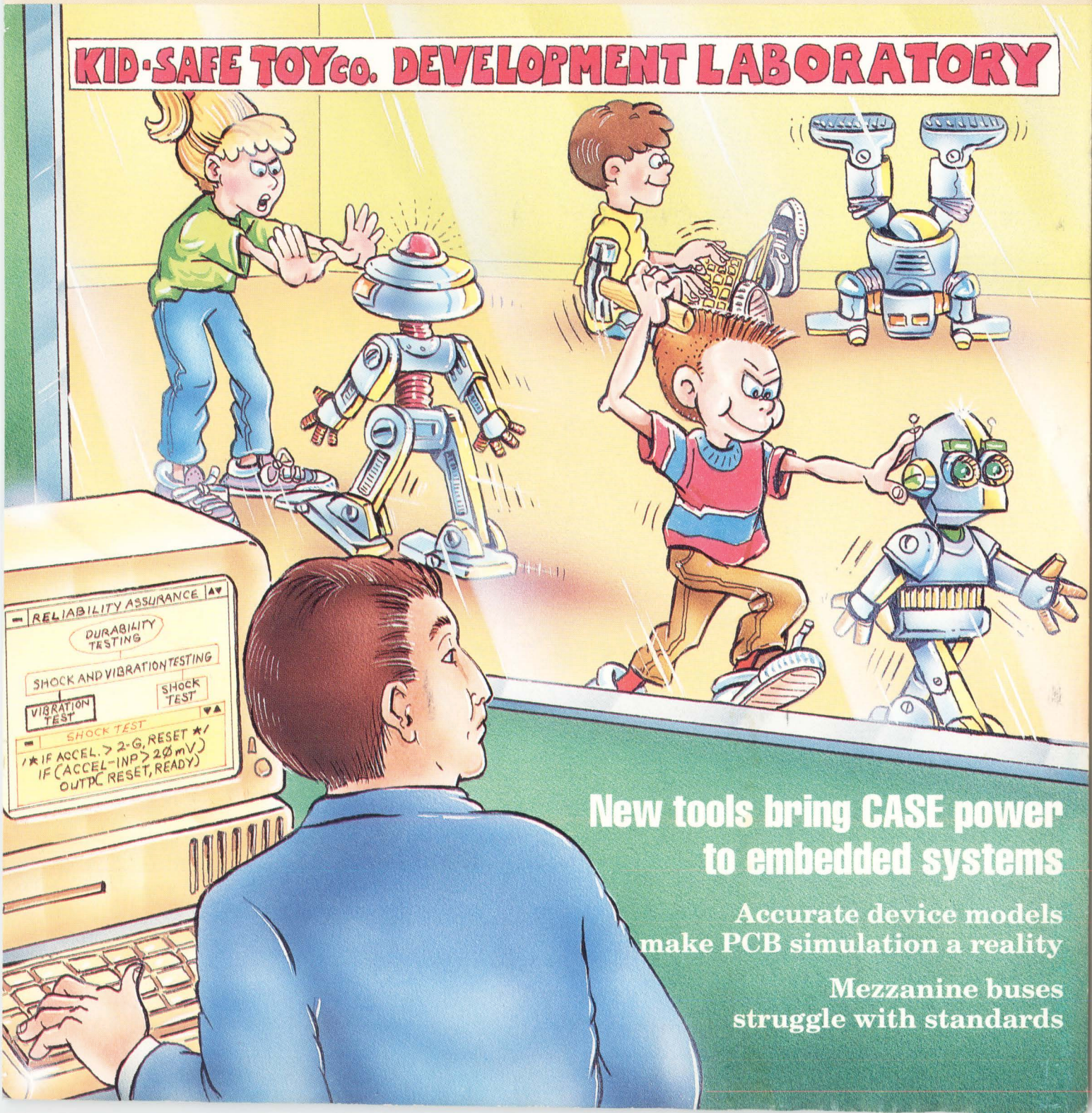
COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



M. Kenneth Oshman on: Distributed control



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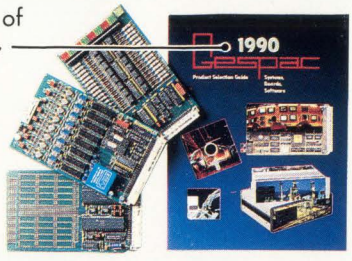

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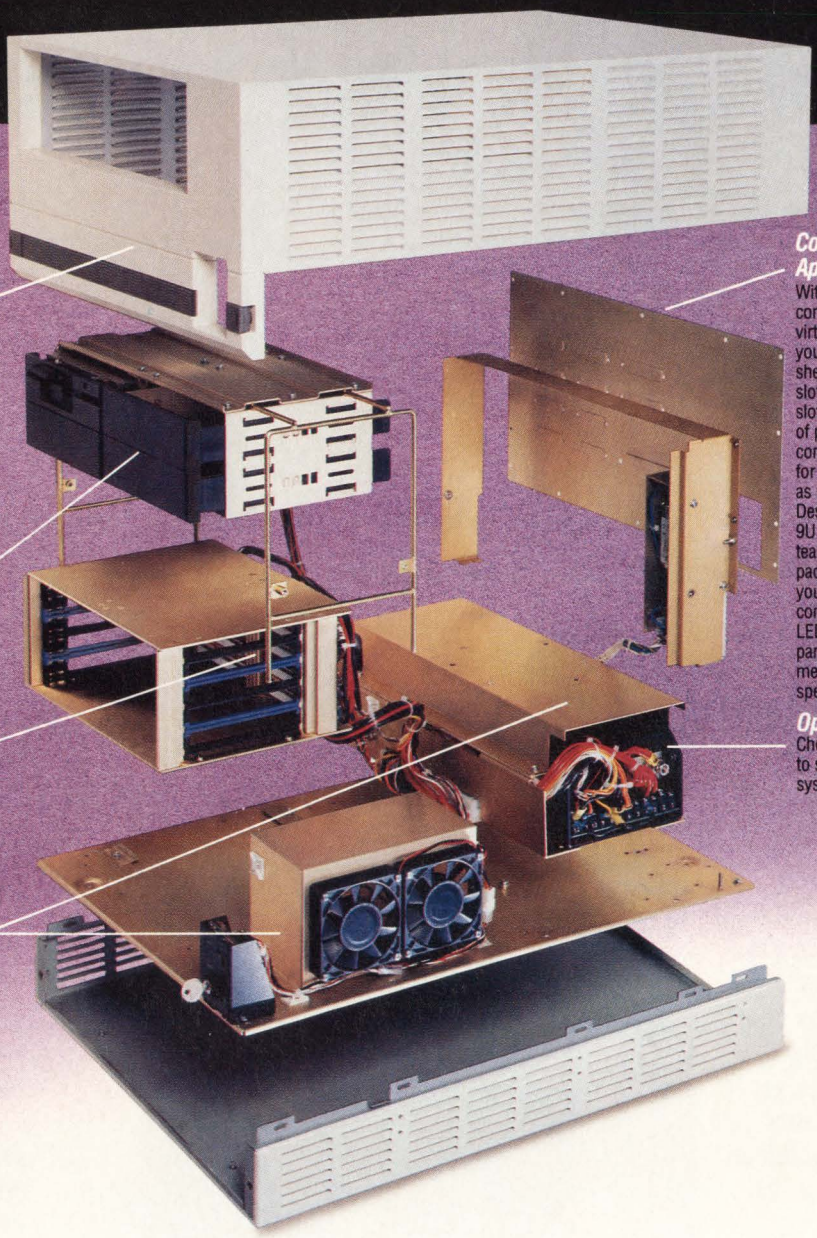
CIRCLE NO. 1

O M E G A

New



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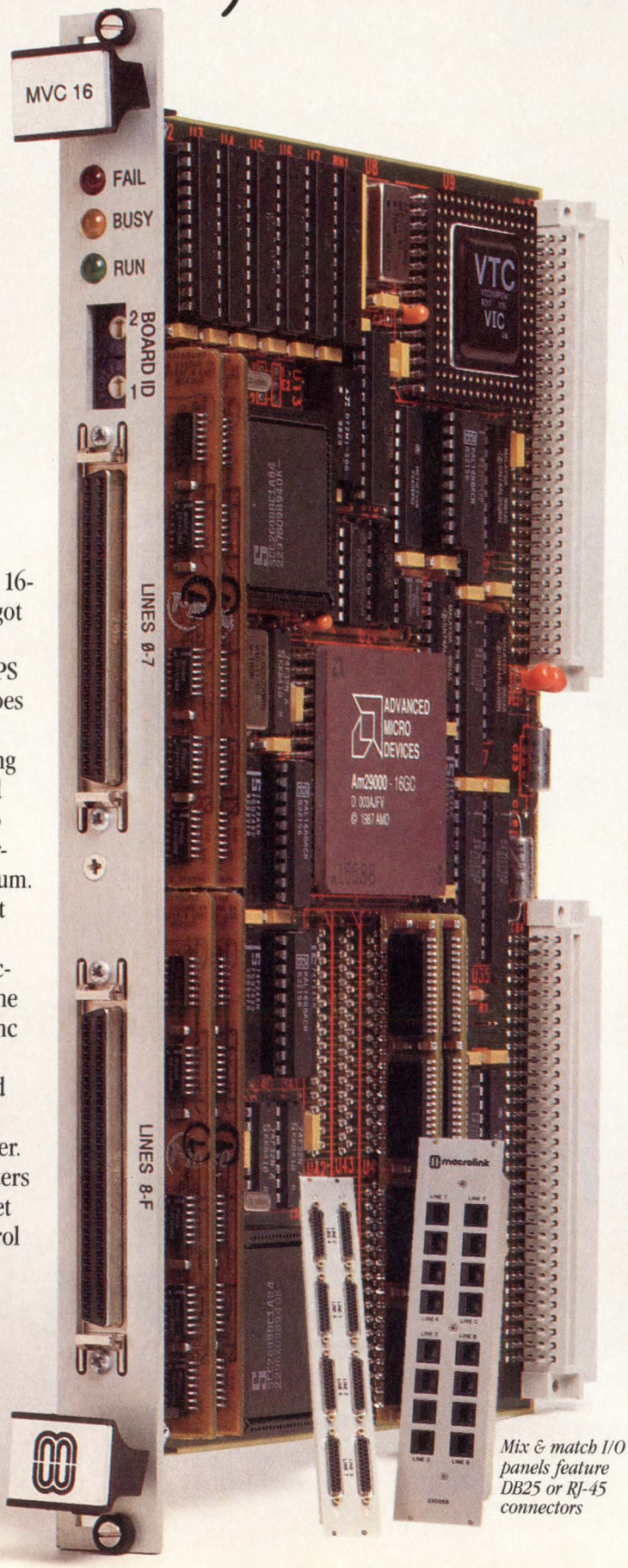

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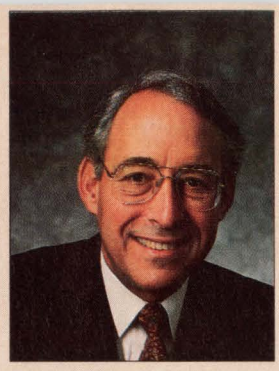

M. Kenneth Oshman on:
Distributed Control
Page 23

VOL. 30, NO. 10 JULY 1991

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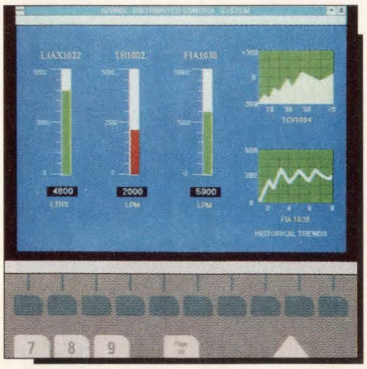
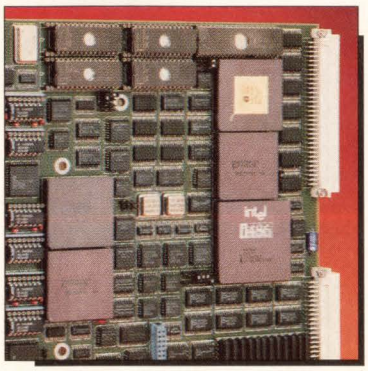


Page 58

TECHNOLOGY UPDATES

Page 71

TECHNOLOGY AND DESIGN FEATURES



Page 113

NEW PRODUCT HIGHLIGHTS

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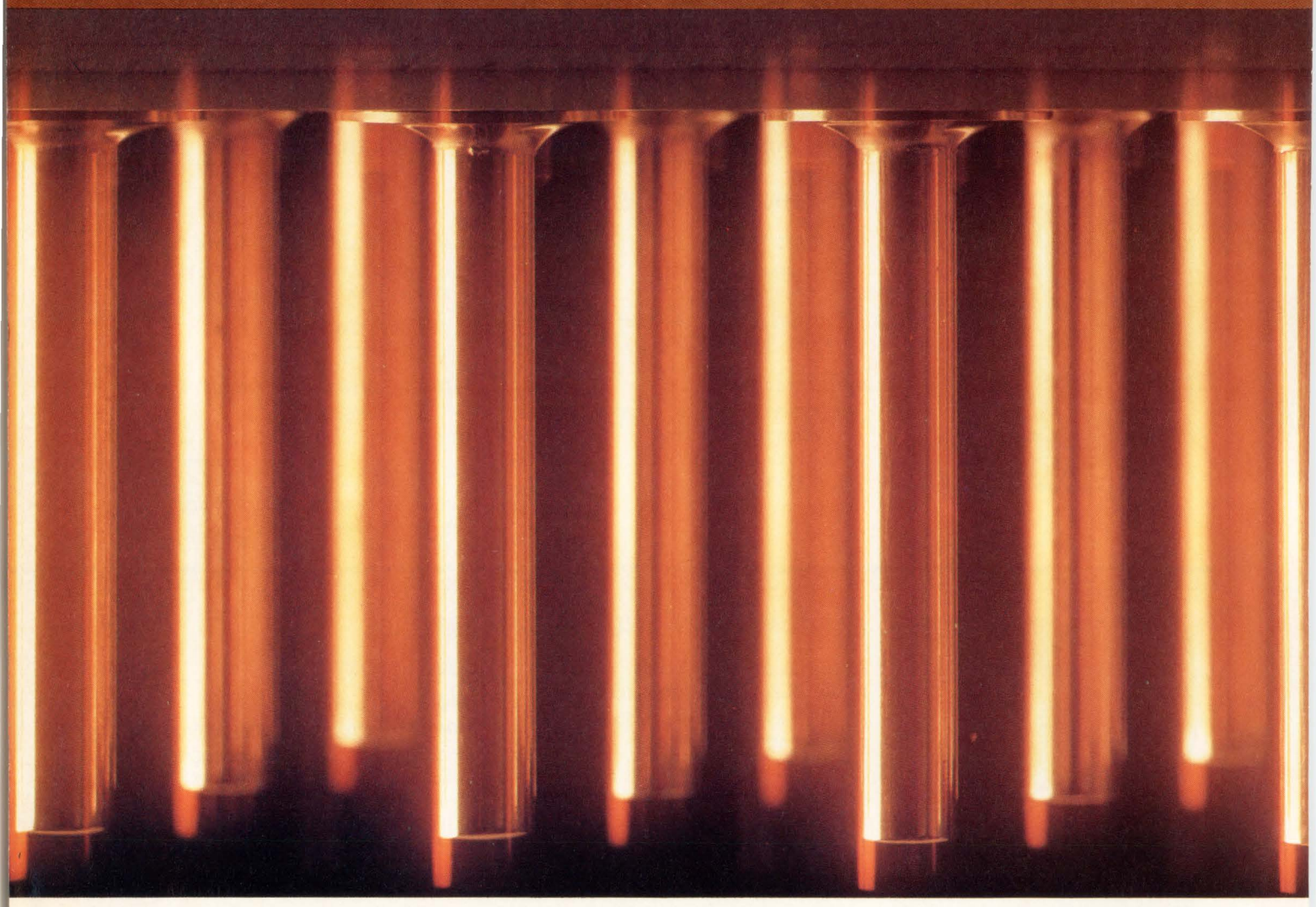
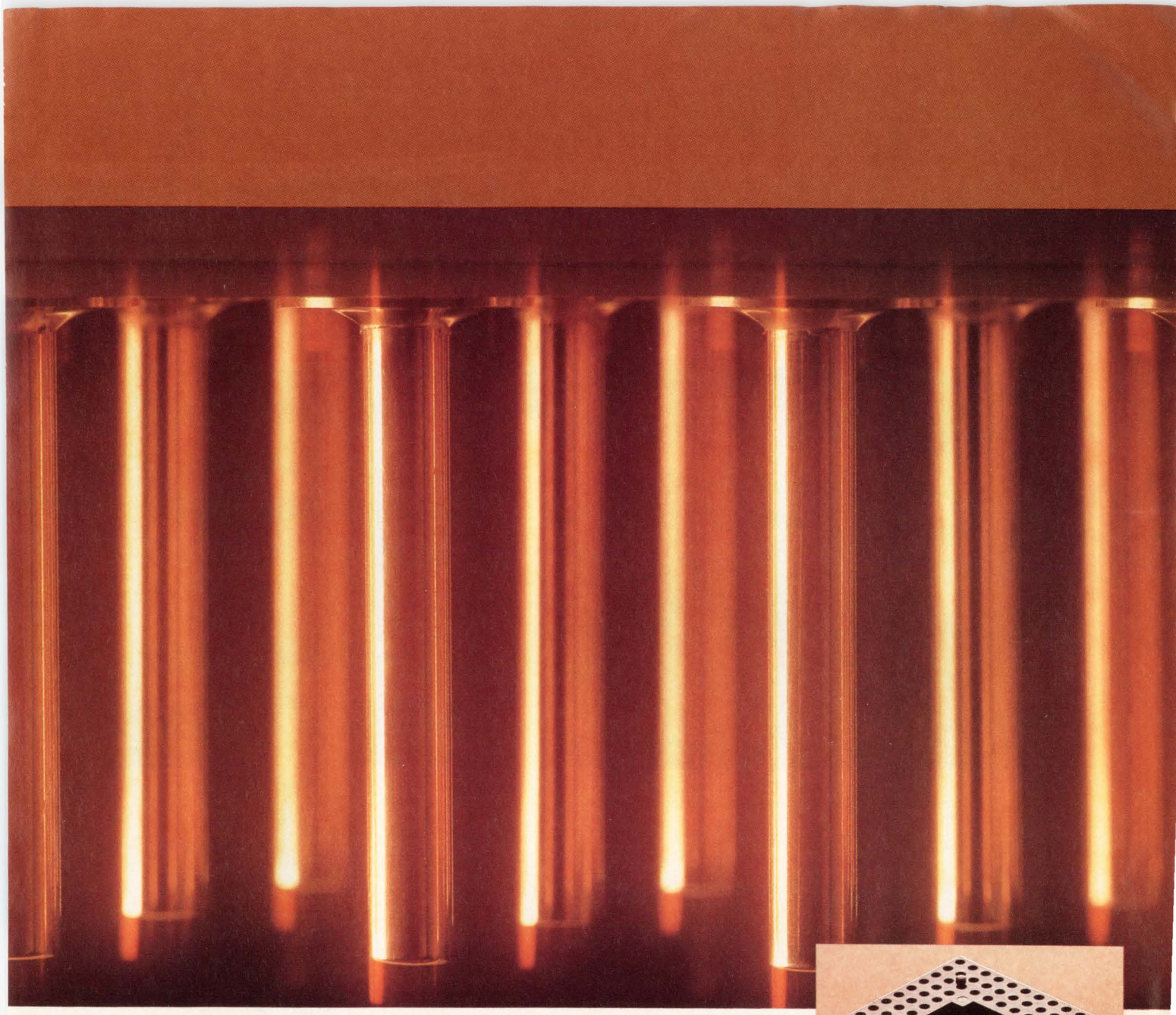
Helping production cope with the pressures of high pincount packages.



THIS IS AMP TODAY.

*J. B. Cullinane, "A User's Evaluation of Pin Grid Array Sockets", *Connection Technology*, June 1990.



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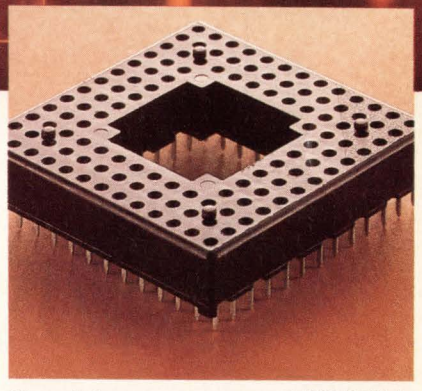

Dual-beam contact LIF PGA

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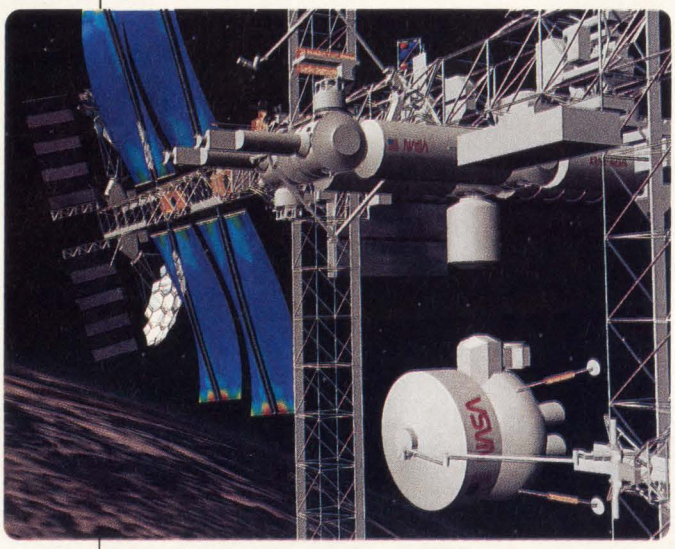

CASE and AI solutions include HP's SoftBench; Interactive Development Environments; Intellicorp; Inference; and Neuron Data.

Mechanical CAD solutions include SDRC; HP ME 10 and 30; McDonnell Douglas; Parametric Technology; and PDA.

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50-MHz 486— It's finally official!

After several system products had already been announced around it, Intel (Santa Clara, CA) officially launched the 50-MHz 486. Dave House, general manager at Intel, cited a Spec integer-only performance of 27.9 for the chip. This compares with a 39.0 integer-only score for Hewlett-Packard's PA-RISC system at 50 MHz and a 19.3 for a 40-MHz i860 device (benchmarked without external cache). When floating-point is factored in, the 486 can be expected to obtain a Specmark somewhat lower than 27.9. A 33-MHz 486, for example, has an integer-only rating of 18.2, but its floating-point rating is only 9.2. Accompanying the release of the chip came news of a 50-MHz CPU cache module that features a 82495DX second-level cache controller and nine 32-kbyte 82490DX dual-ported SRAMs.

The new 486 processor costs $665. The module with 256 kbytes of SRAM cache is $1,314. What's next? Some customers are already rumored to be sampling 66-MHz parts. *—Dave Wilson*

Microsoft to protect data and products with encryption

Microsoft has signed a contract to license software-encryption technology from RSA Associates (Redwood City, CA), presumably as a way of protecting its future products and possibly its internal data from theft and viruses.

Microsoft isn't saying just which, if any, of its operating systems or other products may incorporate the technology. But the deal with RSA reportedly is the largest contract yet for the small company, whose other customers are rumored to include Sun Microsystems, Apple, Motorola, Digital Equipment Corp, Northern Telecom, and Lotus. In fact, most major players other than IBM appear to have jumped on the RSA bandwagon, which could make RSA's technology a de facto encryption standard.

RSA's success also is a snub to the National Security Agency, which has been trying for years to curb the spread of encryption technology that would prevent it from reading electronic mail. The momentum behind the RSA technology may quash efforts backed by the NSA to force acceptance of a standard public key encryption method that NSA could easily crack. The RSA encryption method, which uses both a public and private key, is prohibitively expensive to crack. *—Tom Williams*

FPGAs gain more silicon and software support

With field-programmable gate arrays (FPGAs) holding on as industry darlings, vendors are struggling to put design strategies into place. As for new silicon, Toshiba America Electronic Components (Sunnyvale, CA) has added to its ASIC line 0.8-μm triple-layer-metal CMOS FPGAs based on technology out of Pilkington Microelectronics of the United Kingdom. The technology partners maintain that the Toshiba implementation will be different from the 1.4-μm Electrically Reconfigurable Arrays (ERAs) from Plessey Semiconductor (Scotts Valley, CA), which also are based on Pilkington technology.

Plessey had to go back to the drawing board for its place-and-route software when its first-generation ERAs were met with less-than-enthusiastic acceptance. The redesigned software is expected to make a big difference in FPGA performance and utilization, said Plessey. The firm also will support second-generation Pilkington-based 1-μm devices, to be introduced this summer.

In further developments supporting FPGAs, Mentor Graphics (Wilsonville, OR) debuted its AutoLogic FPGAs with architecture-specific optimization for Xilinx, Actel, and Altera devices. "AutoLogic FPGA targets our LCA architecture and, as a result, makes better use of the resources on the chip," said Xilinx CAE product line manager, Bob Zielke. Exemplar Logic (Berkeley, CA) also announced architecture-specific optimization for Xilinx and Actel devices in its recent of Release 1.0 FPGA toolset. And Cadence Design Systems (San Jose, CA) has now integrated Xilinx' XACT software into its Design Framework II.

—Barbara Tuck

Synopsys links synthesis to SGS-Thomson layout

Synopsys (Mountain View, CA) has forged a two-year strategic alliance with SGS-Thomson Microelectronics (Agrate, Italy and Grenoble, France) to link Synopsys synthesis to SGS-Thomson's IC-layout tools. In the face of heated competition from silicon and EDA vendors offering synthesis as part of front-to-back-end toolsets, it's not at all surprising that Synopsys made the move.

"We recognize that synthesis must have tight links to layout to ensure the highest quality timing and area optimization," said Synopsys' senior vice-president of engineering, Aart de Geus. "SGS-Thomson's successful experience with IC-layout tools, especially for submicron geometries, will be invaluable."

Implementation of the communications link between synthesis and SGS layout, based on tools from Cadence Design Systems (San Jose, CA), will be spread over two years. SGS' executive vice-president of central R&D for CAD and integrated systems, Joseph Borel, reports that the alliance also will cover a link to module generators for the layout of RAMs, ROMs and data path elements.

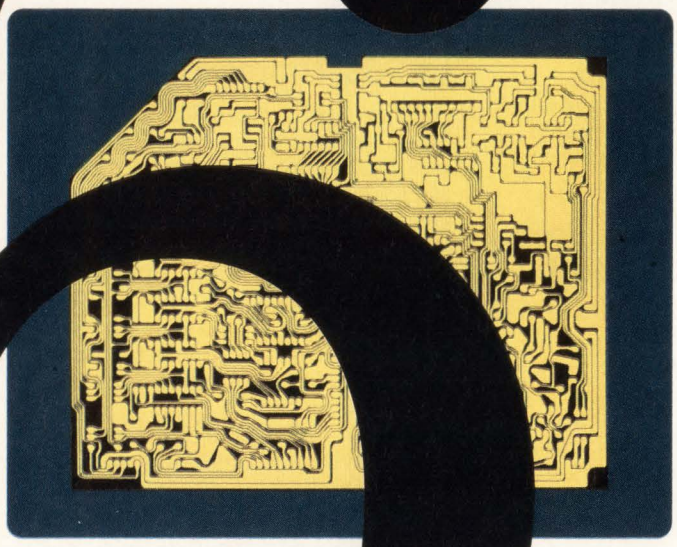
—Barbara Tuck

World's fastest computer clocks in at 9.03 GFlops

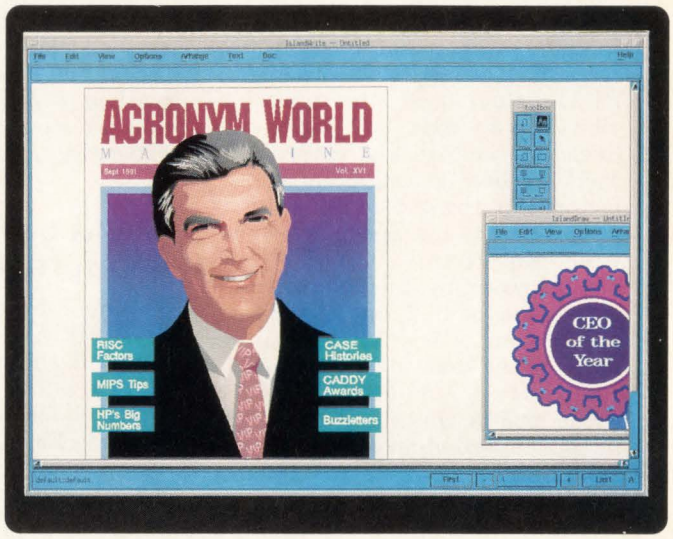
Retaking the lead from Intel in the race for supercomputer supremacy, Thinking Machines (Cambridge, MA) recently said its latest design clocked a blazing 9.03 GFlops in a Linpack benchmark and 17 GFlops in another test. This announcement came just one week after Intel claimed world's fastest status with its Touchstone Delta system. Using

Continued on page 10

6 MIPS!



For electrical CAD, software is available from Cadence Design Systems; Mentor Graphics; Zuken; Racal-Redac; and VLSI, among others.



For Electronic Publishing, Desktop Productivity and Database, available software includes Informix; Oracle; ASK/Ingres; Interleaf; and Island Graphics.

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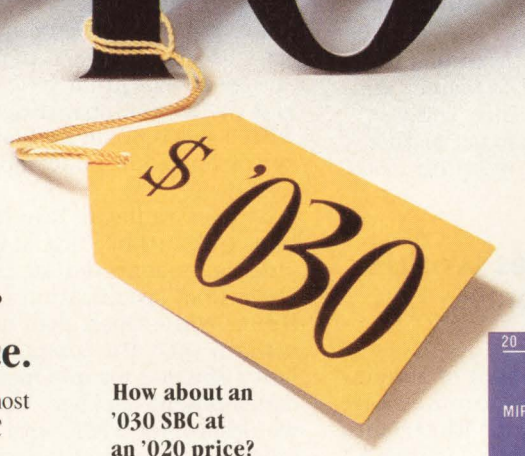
'040



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It's true. For only $2865*—less than the cost of most '030 boards—you can have a *full-featured* '040 SBC that gives your VME system vastly superior performance.

Synergy's new VME Workhorse VW40 is hardly a stripped-down SBC. There's SCSI and Ethernet on-board with 4 Mbytes of DRAM (2, 8 or 16 MB optional). There's a new multi-channel, intelligent DMA controller that handles both I/O *and* VME transfers—all concurrent with normal '040 operations.

Best of all, there's your choice of over a dozen EZ-bus modules with intelligent I/O—fully compatible with Synergy's entire line of '020, '030 and '040 SBCs. Compare that with any other manufacturer!

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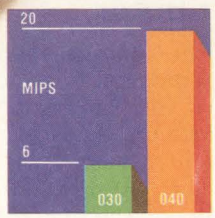
Our new VW30 SBC can plug '030 power and capability into your '020-based system, and at $1595* we'll keep your system price competitive.



The '040 has 3× the performance of the '030; 20 vs 6 MIPS at 25 MHz.

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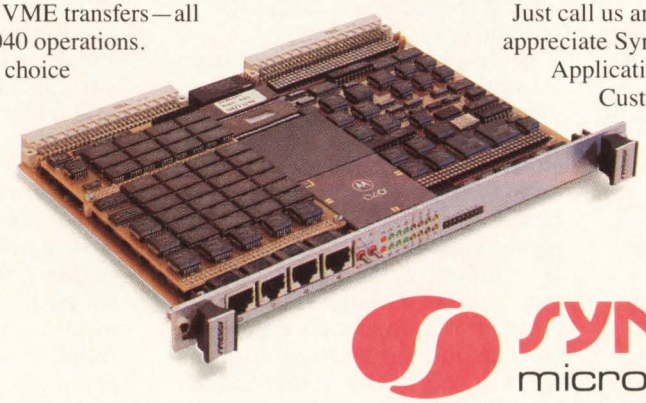

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CIRCLE NO. 6

Continued from page 8

528 microprocessors, the Intel machine delivered 8.6 GFlops.

As impressive as the benchmark performance is, it's perhaps not as important as the fact that the Thinking Machines design was built almost entirely with standard parts. The machine uses 64,000 64-bit floating-point processors. While the company wouldn't reveal the exact processor it used, spokespersons did say it was a commercially available processor. Likewise, the memory devices used in the design were standard 1- and 4-Mbit DRAMs.

This announcement also reflects the importance of the Linpack benchmark in judging supercomputer performance. "Most will agree that only a few benchmarks are any good, and Linpack is one of them," said a Thinking Machines spokesperson. "It's very hard for a company to come out and say they have the fastest machine in the world using something other than Linpack at this point." *—Jeffrey Child*

Arrow becomes world's largest electronics distributor

With the announcement of a definitive agreement to acquire Lex Electronics, Inc. and Almac Electronics Corporation, the North American electronics distribution businesses of Lex Service PLC, for approximately $160 million, Arrow Electronics, Inc. becomes the world's largest electronic distributor. Arrow's 1990 sales revenues totaled $971 million, while Lex (until recently known as Schweber Electronics) and its affiliate, Almac, had combined 1990 sales of $506 million. Arrow's president and CEO, Stephen P. Kaufman, said the company had three objectives beyond growth. He expects that enhanced economies of scale will lead to the lowest cost structure of any distributor, that customers will have access to more products and services, and that the company's earnings will be significantly enhanced. The purchase agreement has been approved by the boards of directors of both companies and is awaiting shareholder approval. The enlarged Arrow is expected to account for annual sales of $1.3 billion in North America and $375 million in Europe. *—John Donovan*

VITA committee selects future developments for VME

As this issue goes to press, the VFEA Industry Trade Association's technical committee has just completed its VME Revision D meeting.

Although many expected cache coherency and message passing to get a lot of attention, they were quickly dismissed in favor of more-exciting developments. The two areas garnering the greatest interest were the proposal to provide an Open Boot protocol for VME and the idea of providing VME with a mechanism for source-synchronized or noncompelled transfers.

Mitch Bradley of Sun Microsystems (Mountain View, CA) provided a presentation on Sun's Open Boot specification used on SBus. While Open Boot is a public domain spec, the company gets a hefty $50,000 for its Open Boot development package. Open Boot would provide VME with many advantages, particularly if it could be combined with some of the control and status register issues being considered along with Rev. D. Following further study, the Open Boot proposal could be endorsed for inclusion in the Rev. D standard.

By far, however, the most interest and time at the session was devoted to the idea of providing VME with a mechanism for source-synchronized or noncompelled transfers. The approach lets unescorted VME data speed along the bus at rates of up to 160 Mbytes/s. By eliminating the handshake protocol, blocks of data will be free to jump on the bus about every 50 ns. The only factor limiting transfer rate will be the ability of the bus to read information. This approach calls for using a throttle to slow down transfers if things get bogged down.

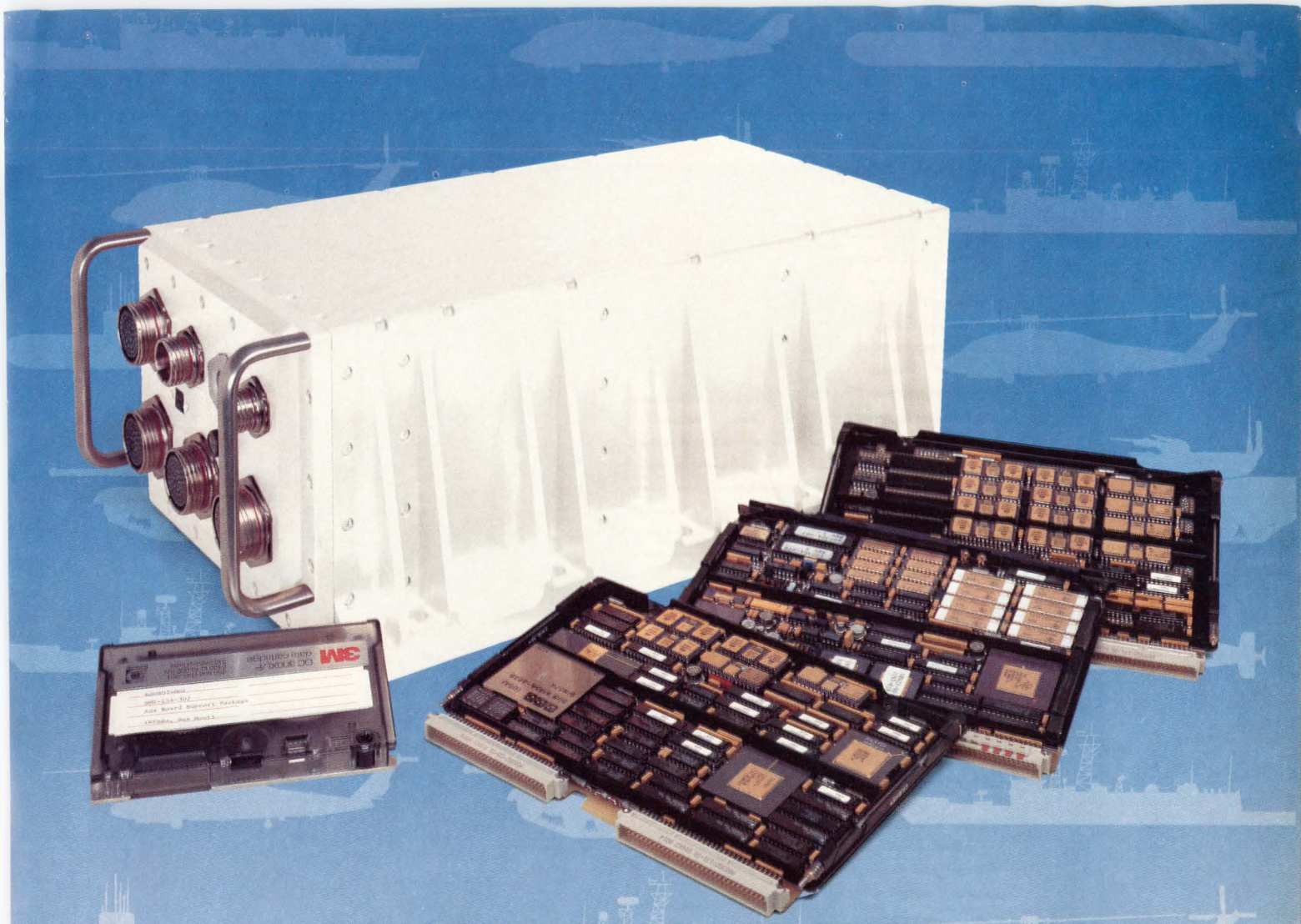
VME64 initially was the impetus behind a Rev. D of the initial 1014 VME specification. The basic 64-bit implementation, however, seems likely to drag a lot of additional baggage into the specification. But the bottom line isn't so much what's in the spec—it's who's adhering to it. VME64, although not yet a part of the VME spec (since Rev. D isn't yet finalized), is already accepted and widely used. The noncompelled or source-synchronized mode will play on that advantage—since SST uses only the VME64 mode—to further boost throughput.

—Warren Andrews

AT&T offers ASIC methodology at 3 V

In an attempt to increase its OEM business, AT&T Microelectronics (Allentown, PA) has made a 3-V standard cell library available to OEM vendors. According to department head for ASIC libraries and technology at AT&T Bell Laboratories, Kevin Kolwicz, AT&T is the first to offer a 3-V ASIC methodology. Shrinking geometries and the desire to continue to use inexpensive plastic packaging have been driving designers from 5- to 3-V technology. But until now, designs intended for battery-powered applications such as cellular phones and notebook computers, which operate at 3.3 V, haven't been supported by standard cell libraries.

The AT&T 3-V library includes cells, memory elements and high-level macrocells, including RAMs, ROMs, a UART (universal asynchronous receiver/transmitter), and a DMA controller that can be assembled into application-specific 3-V designs with AT&T's and third-party design tools. Because low-voltage chips may run slower, the library also includes higher-power cells for speed-critical paths. The macrocell library eventually will encompass a wide range of application-specific standard parts. *—Barbara Tuck*



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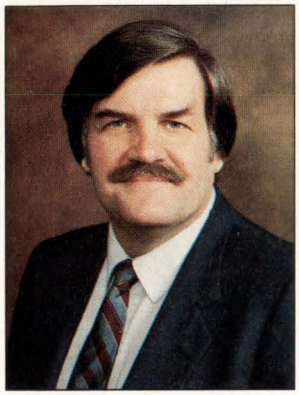

John C. Miklosz
Associate Publisher/
Editor-in-Chief

Show business! The smell of the grease paint, the roar of the crowd. How can anyone resist the excitement of show business? Well, we can't, and you'll notice advertisements in this issue for three shows that we're now involved with: the Analog & Mixed-Signal Design Conference, Buscon and SysComp. But since there's no smell of grease paint or roar of the crowd, why should we get involved in trade shows or conferences? Aside from a couple of obvious financial reasons, participation in appropriate shows reinforces our editorial position and opens up another avenue of communication with our readers. To see how the *right* shows do this, let's first look at the Analog and Mixed-Signal Design Conference (see page 128 & 129).

Whether it's a CAT scanner, a laser printer, a PBX, a CD player, a fuel injection controller, or just about anything else electronic, there's a microprocessor or other logic elements at its heart. All of these products are computers. They look different only because they interface with the outside world—an analog world—in different ways.

Because they are computers, they're designed mostly by digital designers. To be effective, these designers must know how to combine analog with digital or how to implement analog functions using digital approaches—which is what mixed-signal design is all about. This makes analog and mixed-signal technology—especially mixed-signal—an integral part of *COMPUTER DESIGN*. Our involvement in the technical sessions for the Analog and Mixed-Signal Design Conference strengthens this position.

Complex chips, whether digital only or mixed digital/analog, are rightfully considered systems. But systems are much more than chips. Industrial-, commercial- and military-strength products are often configured using a mix of in-house designed boards and subsystems and off-the-shelf board products. What's more, these systems are often embedded and used in real-time applications. Any publication that's systems-oriented must focus not only on chips and CAE/CAD tools, but on bus architectures, board-level products *and* real-time software. This is what *COMPUTER DESIGN* does, but it's also what Buscon (see page 135) is all about, and our involvement with the technical program underscores our commitment to these areas of design.

But most of these systems are more than chips, boards and software. They all need a power source, many of them use some form of display or mass storage. Driving these products and systems is the demand to make almost everything smaller, lighter, power stingy, less expensive, higher quality and to bring them to market faster. What's more, product development is changing dramatically, with isolated design, test and manufacturing groups giving way to concurrent engineering. Until SysComp (see page 119), there's not been a trade show that brought all of these elements together under one roof. Our involvement with it reinforces our ongoing commitment to concurrent engineering and the importance of OEM systems integration.

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CIRCLE NO. 10

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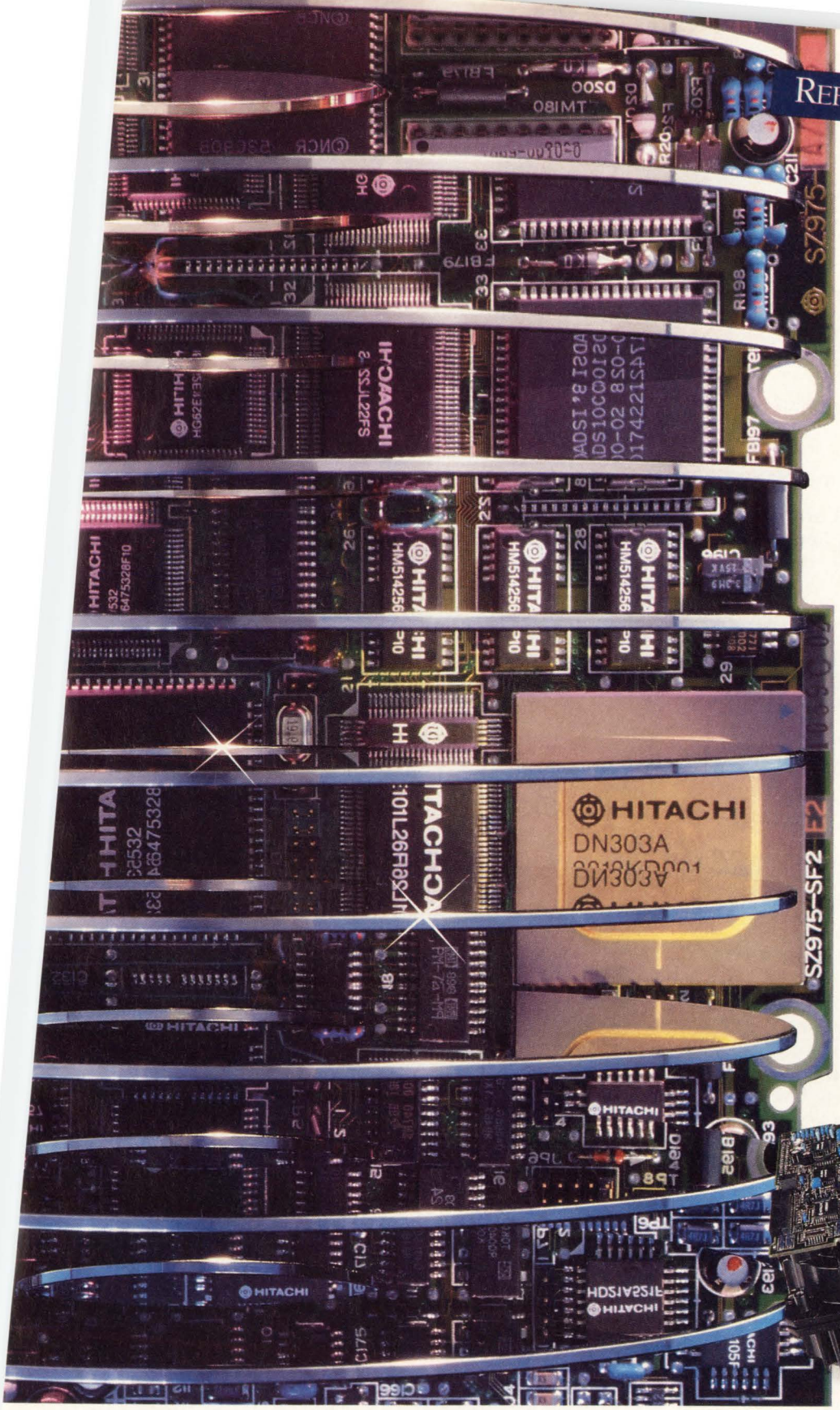

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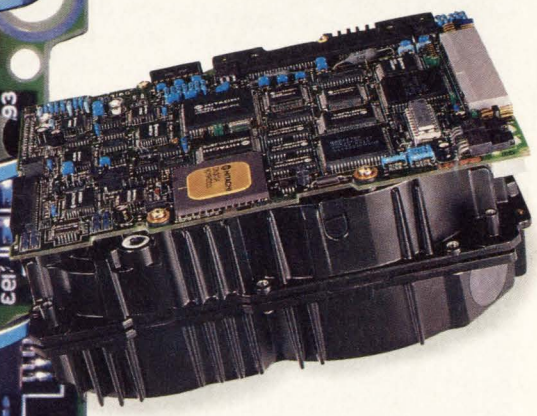

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CALENDAR

CONFERENCES

July 9 - 11
Engineering Workstations Conference

Hynes Convention Center, Boston, MA. Conference will feature the latest hardware, software, add-ons, and peripherals, and include daily new product briefings. Thirty conference sessions will focus on topics including CAD/CAE, CASE, peripherals, and project management. Information: Engineering Workstations Conference, PO Box 3275, Santa Monica, CA 90408, (213) 450-0500, fax (213) 450-0132. **Circle 366**

July 28 - August 2
SIGGRAPH '91

Las Vegas Convention Center, Las Vegas, NV. The 18th International Conference on Computer Graphics and Interactive Techniques is perhaps the world's most comprehensive exhibit of computer graphics products and services, with an anticipated 25,000 attendees. This year's theme, "Where Advanced Technologies Inspire Tomorrow's Realities," will be portrayed through an extensive program of courses, interdisciplinary workshops and panels. In multidimensional, interactive installations, attendees can grab the 3-D mice, joysticks and trackballs, strap on headgear, stereo eyewear and gloves, and experience the next step in show participation—"virtual reality." Information: SIGGRAPH '91 Conference Management, 401 N Michigan Ave, Chicago, IL 60611, (312) 644-6610, fax (312) 321-6876. **Circle 367**

September 11 - 13
BUSCON '91/East

Omni-Shoreham Hotel, Washington, DC. The industry's leading board- and systems-level show makes its Mid-Atlantic debut this year in Washington, DC. The first glimpse of advances in bus architecture, from Multibus II to VMEbus, Futurebus+, SBus and Turbochannel, plus the newest offerings among other elements of systems architecture—boards, backplanes, chips, embedded software and operating systems—will highlight the show. At the technical seminar program, attendees will have the opportunity to learn about new bus architectures directly from the people who developed them. Information: Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856, (800) 243-3238, fax (203) 857-4075. **Circle 368**

October 30 - November 1
Analog & Mixed-Signal Design Conference

Santa Clara Marriott, Santa Clara, CA. The Analog & Mixed-Signal Conference is dedicated to the unique needs of mixed-signal design. Forty-five lectures and workshops will focus on subjects including transmission line effects in high-speed design; mixed analog/digital design; modeling, simulation and test; and much more. Information: Angela Hoyte, Miller-Freeman, PO Box 7843, San Francisco, CA 94120-7843, (415) 905-2354, fax (415) 905-2630. **Circle 369**

Would you like your event listed here?

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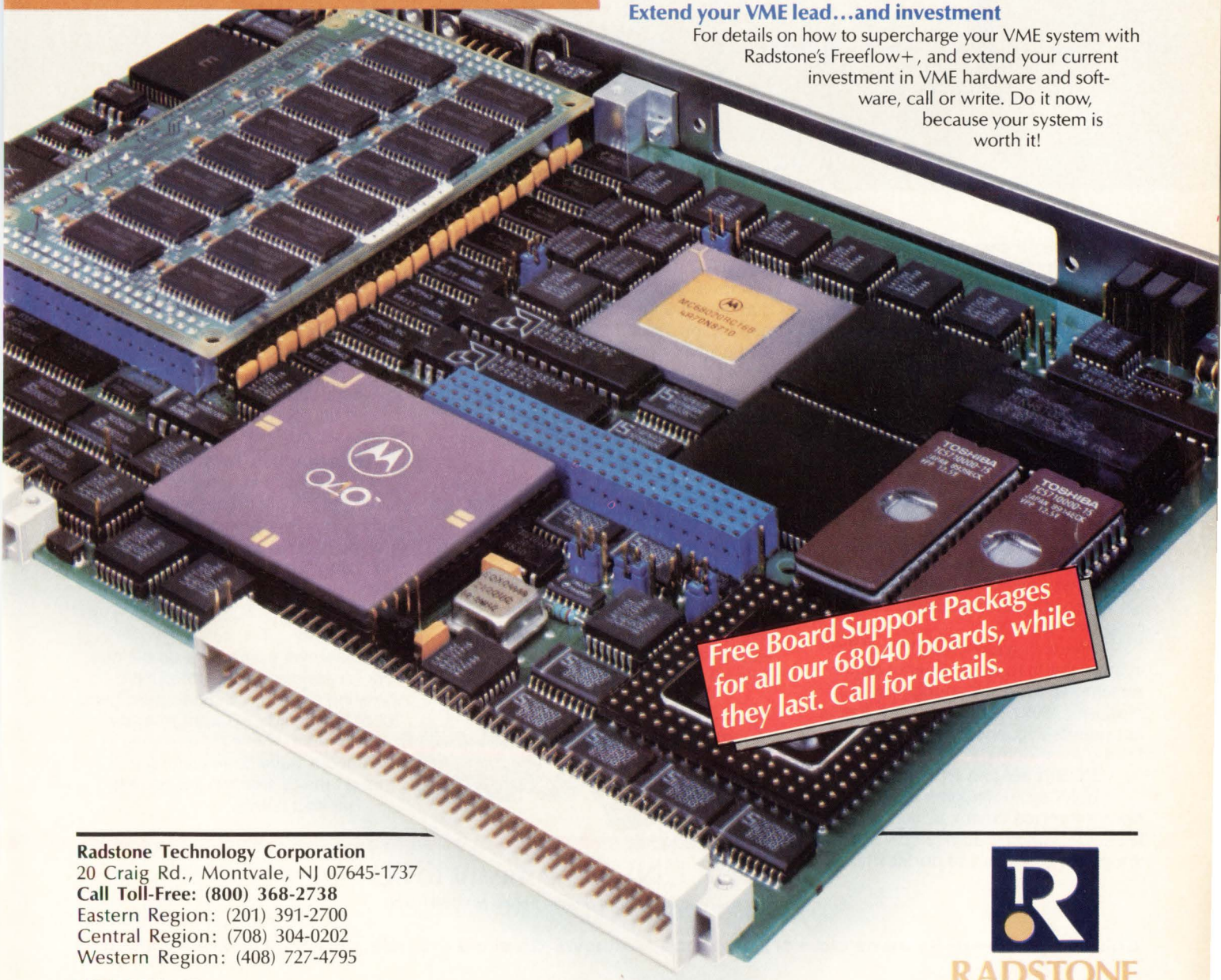

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CIRCLE NO. 17

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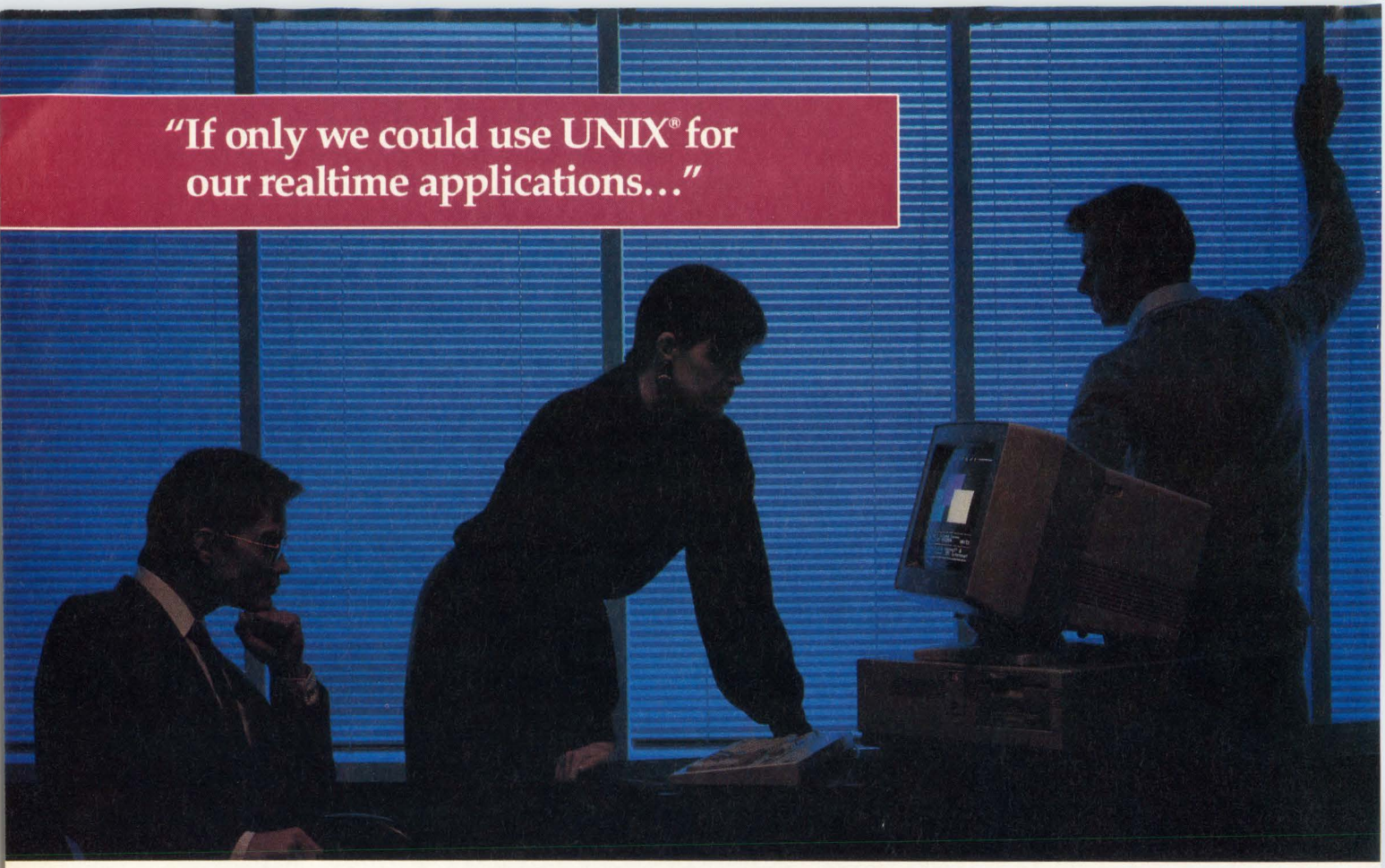

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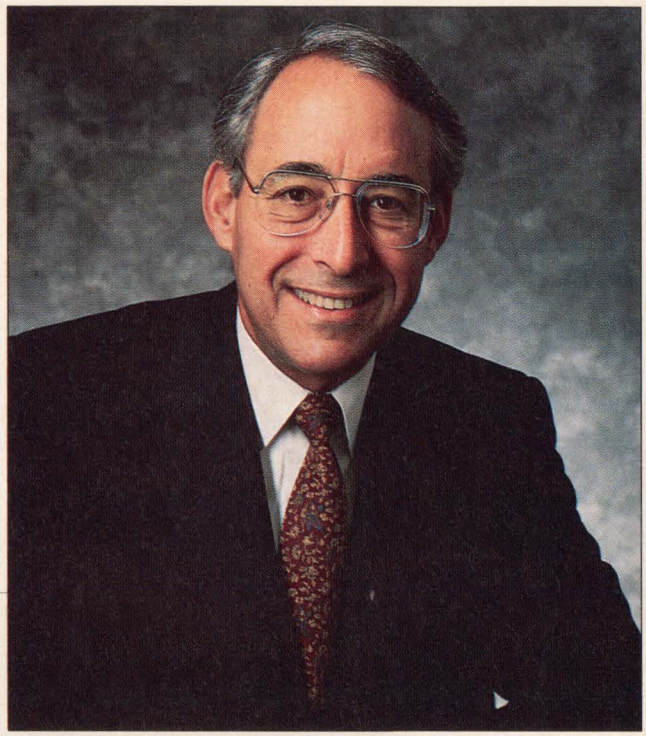
*"Who is the Real Dennis Ritchie?" UNIXWORLD, January 1991, p. 46.

CIRCLE NO. 18

M. Kenneth Oshman on: Distributed control



"The network is the computer," a phrase coined by Sun Microsystems, aptly captures the essence of distributed computing—independent processors functioning in a tightly integrated system. The market for distributed processing in the computer world far overshadows the market for large central computers. Small computers provide local intelligence and communicate over a variety of media with different protocols.

In the control version of distributed processing, the network becomes the controller. This is known as intelligent distributed control. Intelligent distributed control will pervade applications that today use centralized or nonintelligent control, and will move into applications that are currently not controlled at all.

Distributed-control systems already exist in high-end industrial-automation applications. These systems distribute specialized intelligence among nodes at the point at which sensing, control and actuation occur. Each node contains the necessary intelligence to communicate with other nodes to pass status and commands to other control points, so that the network operates as an integrated control system.

But the price of today's processors—typically between $1,000 to $10,000 each—has confined distributed control to high-end factory automation. This barrier begins to disappear when the cost of the intelligence and the network interface at each processing node of the system drops below $50.

When the per-node cost reaches $10, distributed control becomes practical in almost anything. A distributed system could be used, for instance, to control the operation of a photocopier, replacing the complex point-to-point wiring harness and dedicated control devices. Or control nodes could be built into lighting fixtures to permit distributed control of a building's lighting over ordinary power lines. HVAC systems, security systems, cars, and household products would all be likely candidates for this type of intelligence.

While distributed-control systems are in use today, several barriers beyond cost have hindered wider acceptance. One is the custom development that's required to implement distributed-control systems. Many of the key elements of a system may have to be newly integrated, or even built from scratch. These elements typically include communications hardware and software, a system operating kernel, and control interface hardware. By some estimates, as much as 90 percent of the effort may go into implementing communications and operations functions, when, in fact, 90 percent of the effort should be dedicated to developing the control functionality where the real added value lies. This nonproductive inflation of development costs would vanish if standard off-the-shelf support for communications and operating needs was available. Until it is, development costs effectively disqualify distributed control from serving many potential applications.

What is needed?

A distributed-control system consists of multiple control nodes distributed over some physical distance that communicate over a network. Each node contains local intelligence for control tasks and for communication with other nodes.

In providing solutions tailored for distributed control, one has to examine the tools needed. Since the architecture of an intelligent distributed-control system can be broken down into two major functions, communications and control, it's convenient to group the needed tools into these functional categories. Intelligent distributed-control nodes have common architectural requirements, as well as some requirements that are unique to individual applications, as shown in the table "Architectural needs of intelligent distributed control nodes."

Communications requirements

The need for reliability in most control systems directly affects the control network topology. A peer-to-peer network architecture is desirable because this con-

figuration affords higher reliability and robustness than does a master/slave configuration. In a master/slave network, the master processor represents an undesirable single point of failure unless expensive redundancy schemes are implemented.

In addition, each node needs sufficient supervisory intelligence to share the distributed operating control of the network with other nodes or with a supervisory node. Communications intelligence is required at each distributed node.

Architectural needs of intelligent distributed control nodes

Common requirements:
access to local control devices (sensors and actuators)
hardware, software and protocol to allow access to other nodes over the network
local computational capability to execute control algorithms
local operating kernel scheduling control (sense/actuate) steps according to the applications software
Application-unique requirements:
applications software driving the operating kernel to monitor and actuate events locally or at remote nodes
local sense/control hardware
a communication network allowing access to other nodes
additional local computation or control intelligence

The communications protocol must be optimized for control communications, which requires reliable data transport and real-time response. In distributed-computing environments, the size of each transaction may vary over a wide range, so the important measure for performance at each node is often the data-transfer rate in bytes/s. In control networks, transactions usually consist of a small number of bytes that must be received and acted upon within a fixed time. Thus, in control networks, the important measure is the arrival, or round-trip time, for each transaction.

A protocol for a control network needs to optimize all the components of arrival or round-trip response time, namely network-access time, transaction-transmission time, and the time to generate a response. Network-access time and transaction-access time affect the data rate or the channel capacity, and must be optimized in the context of the number of nodes in a network, the physical distance the messages travel, and other limitations of the media, such as noise susceptibility.

Topological options that let the network be divided into subnetworks, and include commonly interacting nodes on the same subnetwork, allow fast response times without the need for a high channel capacity. Priority and other methods of access control cut network-access time and can be used to tailor network real-time response.

Options in message services, such as one-way unacknowledged transmissions, or those that require individual acknowledgements or invoke multiple transmissions without requiring acknowledgement, let users balance the reliability of transmission over the network against the possibility of messages being lost. Such options should be easy to invoke by the engineer designing the control application, and shouldn't require other than high-level software programming and hardware integration.

In addition, the level of embedded protocol support should be built in, so that it doesn't have to be reinvented for every application. And it should also be completely transparent to engineers, so that their time is spent developing applications—not wrestling with communications protocols. With reference to the Open Systems Interconnection model, this implies that engineers interface with the communications protocol only at the applications layer. And if this transparent communication is to be successful in the real multivendor world of control applications, interoperability must be a part of the embedded protocol.

Interoperability key

To understand the importance of interoperability, consider that most distributed-control systems will include equipment from more than one vendor. If a hospital wanted to build a system with different types of bedside monitors, it may go to several specialized manufacturers. If a standard protocol didn't exist, all manufacturers would have to understand one another's protocol. This, in turn, would add to each manufacturer's overhead and to the cost of its products.

Faced with the lack of a standard, manufacturers usually respond by limiting the number of proprietary protocols they support. Thus, engineers' choice of products is limited. And even if a manufacturer only supports a handful of third-party protocols, how thoroughly can it afford to test and guarantee interoperability? What if, due to an incompatibility undiscovered in a manufacturer's testing, a control system fails in the field?

The need for a standard, interoperable protocol can't be overemphasized. Yet the availability of a such a protocol isn't enough. Suitable choices of physical media are also important. Many control applications may prefer the cheapest available communications medium. (This is especially true for applications without extraordinary needs for extended transmission distances or exceptional immunity to electrical noise.) Such nodes may communicate over common twisted-pair wire. On the other hand, some circumstances may call for more-exotic media, such as wireless communication via infrared or radio links.

Control applications in existing residential or commercial buildings, where rewiring is expensive or impossible, may only be viable if communications can be piggy-backed over existing wiring, such as ac power lines, unused telephone wiring or the common coaxial cable used for TV systems. Factory floors or other systems requiring high reliability, such as aircraft systems or critical-care medical equipment, may prefer the electrical noise immunity of optical fibers.

Within each medium, unique needs may dictate different data rates, for example, or modulation techniques for error minimization. And even in a single distributed system, different parts of the network

may require different media, which leads to the use of mixed-media routers and gateways.

Control requirements

At each node, the intelligence that's best suited for control tasks differs from that required for other types of computation because it must directly perform routine sense and control functions. Sense functions include level sensing, edge detection, pulse-width measurement, time-outs, and parallel data input. Control functions include data outputs on bits, nibbles, or bytes; serial data; and output of one pulse of a controlled width or pulse train of a controlled duty cycle. Control response must be deterministic. The control functions of any node should be directly controllable by the sense/time-out functions of that node or any other node within a fixed delay or within maximum specified response times.

The use of high-level languages to program the control algorithms is important. Since not all engineers can be assumed to be veteran programmers, the programming language should be a de facto standard and must be procedural, such as C. That way, the need for additional learning is minimized, and the program flow is governed by the control algorithms, rather than by language syntax. To provide the efficiency of a high-level language as well as provide efficient support for control applications, extensions to the language for sensor and actuator device support, or for event-driven syntax, may be added.

System-development requirements

Even the most-tailored solutions are ineffective without the tools to put them into use. Development tools for intelligent distributed-control systems have some unique needs, as well as other needs that they share with other development environments. They require a development environment that's low-cost, familiar, and easily available, for example. (In almost every case, this means a PC.) This development environment should be a rich and efficient framework for developing and debugging hardware and software for each node and for building the network to connect the nodes. The environment also should allow for quick emulation of nodes and network controllers.

In the final analysis, the true cost of implementation for the technologies used for intelligent distributed-control systems should be low. Development cost can be reduced by built-in support and an effective development environment.Various factors must be included in the final cost of a system for a specific application include: raw hardware and software, hardware assembly, software integration, node and system test, installation, and maintenance. Depending on the application, one or the other cost factor may be more important.

Who needs distributed control?

The potential applications for distributed-control systems are widespread. If key objectives such as cost/node, interoperability and ease of development are met, the potential market for intelligent distributed-control nodes is orders of magnitude greater than the markets for PCs—or even consumer electronics. At best, the per capita need for computers may be one to two per user (assuming one at work and one at home). The per capita need for telephones may be two to three per user (one or two at home, one in the car, one at the office, and, someday, a phone in everyone's pocket). Looking at the list of possible uses in the table, "Applications for intelligent distributed control" it's not hard to imagine 10 to 100 per user.

Applications for intelligent distributed control

Applications :	Tasks:
buildings	heating, ventilation, air-conditioning (HVAC) control; security; fire detection; lighting controls
factories	flow, pressure, temperature metering and control; programmable and numerical control; robots; automatic testers
labs	instrumentation
hospitals	diagnostic and monitoring equipment
transportation	cars, buses, trucks, planes, trains; traffic lights
retail	transaction-processing systems
agriculture	irrigation, crop and weather monitoring
homes	security, sprinkler systems, entertainment

Evolution of the technology

Distributed-control systems are expected to gradually replace and existing centralized control solutions—and eventually make them obsolete. Inevitably, this will happen in the form of a new industry with its own food chain, and there will be a significant business and economic impact.

Intelligent distributed-control systems provide a new frontier, and Echelon is working to develop suitable enabling technology for such systems. Its recently introduced LonWorks product family includes a highly optimized IC for control and communications (the Neuron Chip), a communications protocol (LonTalk) that provides high-level control-oriented network services to OEMs developing control applications, and a high-level development environment (the LonBuilder Developer's Workbench) for developing and debugging LonWorks nodes and networks.

Early applications of the new, affordable distributed-control technology will include building automation, industrial automation, office machines, and instrumentation. Over time, this technology will also find use in intelligent homes, cars, planes, and many other parts of everyday life. Echelon has identified over 400 uses of this technology. Other suppliers of enabling technologies, commercial products and services, and standards organizations must participate in this new wave of distributed control if it is to be successful. Wide availability of off-the-shelf hardware- and software-enabling technologies, development tools, products, and installation and maintenance services will generate this next revolution in the use of electronics in this decade, and will ensure the broad acceptance of the technology before this century runs its course.

M. Kenneth Oshman is president and CEO at Echelon (Palo Alto, CA).

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CIRCLE NO. 19

A look behind symmetric superscalar RISC

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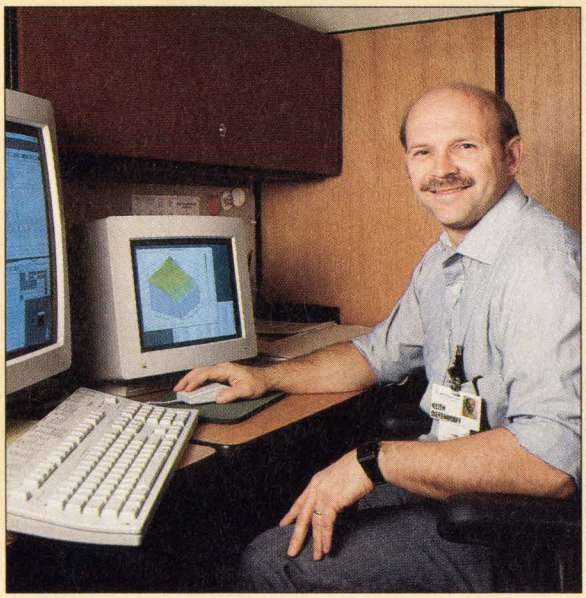
The 88110 superscalar RISC processor from Motorola (Austin, TX) represents an architectural leap forward in RISC processor design. Not only will the chip be superscalar, but it will offer the highest level of integration found in a commercial RISC processor. Two integer units will be complemented by both floating-point and 3-D color graphics facilities. Furthermore, the chip will offer cache-coherence logic and on-chip support for off-chip secondary caches, which will make it suited for multiprocessor systems. To top it all off, the processor promises to be between three and five times faster than the current-generation 88100 and 88200 three-chip sets.

Choosing an architecture

The Motorola design team, headed by chief architect Keith Deifendorff, evaluated and rejected vector and superpipelined architectures before embarking on the design of the chip. Vector architectures, commonly used in supercomputers, have traditionally been used in scientific applications that have large regular data structures, such as arrays, with few data interdependencies. Vector machines are deeply pipelined and can have long pipeline startup delays, making them unsuitable for general-purpose scalar applications.

Superpipelined and superscalar machines are two approaches that can recover fine-grained (instruction-level) parallelism on scalar code. A superpipelined machine exploits temporal parallelism by overlapping the basic hardware execution unit and running the pipeline at a multiple of the processor's clock rate. In this way, it can process more than one instruction for each clock cycle. The advantage of the superpipelined approach is that it uses transistors efficiently. But it must have higher internal operating frequencies. Therefore, its ultimate performance is directly dependent on the speed of its semiconductor process.

A superscalar machine, on the other hand, relies on dynamically recovering spatial parallelism: it rearranges the execution of instructions on the fly to match the parallelism available in its multiple execution units. Superscalar machines, because they're based on multiple execution units, require more transistors than superpipelined machines. But they have the advantage that internal circuits operate at lower frequencies for a given performance. The superscalar approach is, therefore, directly dependent on the circuit density capabilities of its semiconductor process.



Keith Diefendorff is the man behind the future Motorola 88110 RISC processor. "By the end of the decade, it should be possible to deliver 4,000 Mips on a single silicon chip—and that should make quite a nice little notepad computer," he says.

Superpipelined and superscalar machines have similar instruction issue restrictions. "But they take different approaches to recovering parallelism and have different design trade-offs as a result," says Diefendorff.

Motorola saw the superscalar approach as the better match for future semiconductor technology "because circuit density improves at about three times the rate of circuit speed over time," notes Diefendorff. "We believe that an unrestricted superscalar approach and dynamic instruction rescheduling techniques can recover nearly all the parallelism that's available in conventionally produced instruction streams." After all the implicit parallelism has been exploited from the instruction stream, Diefendorff's team plans to exploit parallelism at higher levels by employing special-purpose hardware, such as vector execution units, and by placing multiple processors on a single chip.

From top to bottom, the architecture was designed to support future generations of processors that exploit instruction-level parallelism to its fullest. Multiple independently pipelined execution units, out-of-order instruction execution, and dynamic instruction rescheduling, as well as superpipelining and superscalar instruction issue techniques, can all be implemented transparently, without affecting software compatibility. The simple register model of the processor makes it easy to construct multiported register files to supply the high-operand bandwidth needed in highly parallel implementations.

"And we've been extremely careful to avoid bottlenecks and features such as condition codes and kludge registers that might limit rescheduling opportunities," adds Diefendorff. With the 88110 chip under his belt, what is Diefendorff doing for an encore? He's now designing some support chips for the 88110 processor that will, among other things, provide support for a second-level cache.

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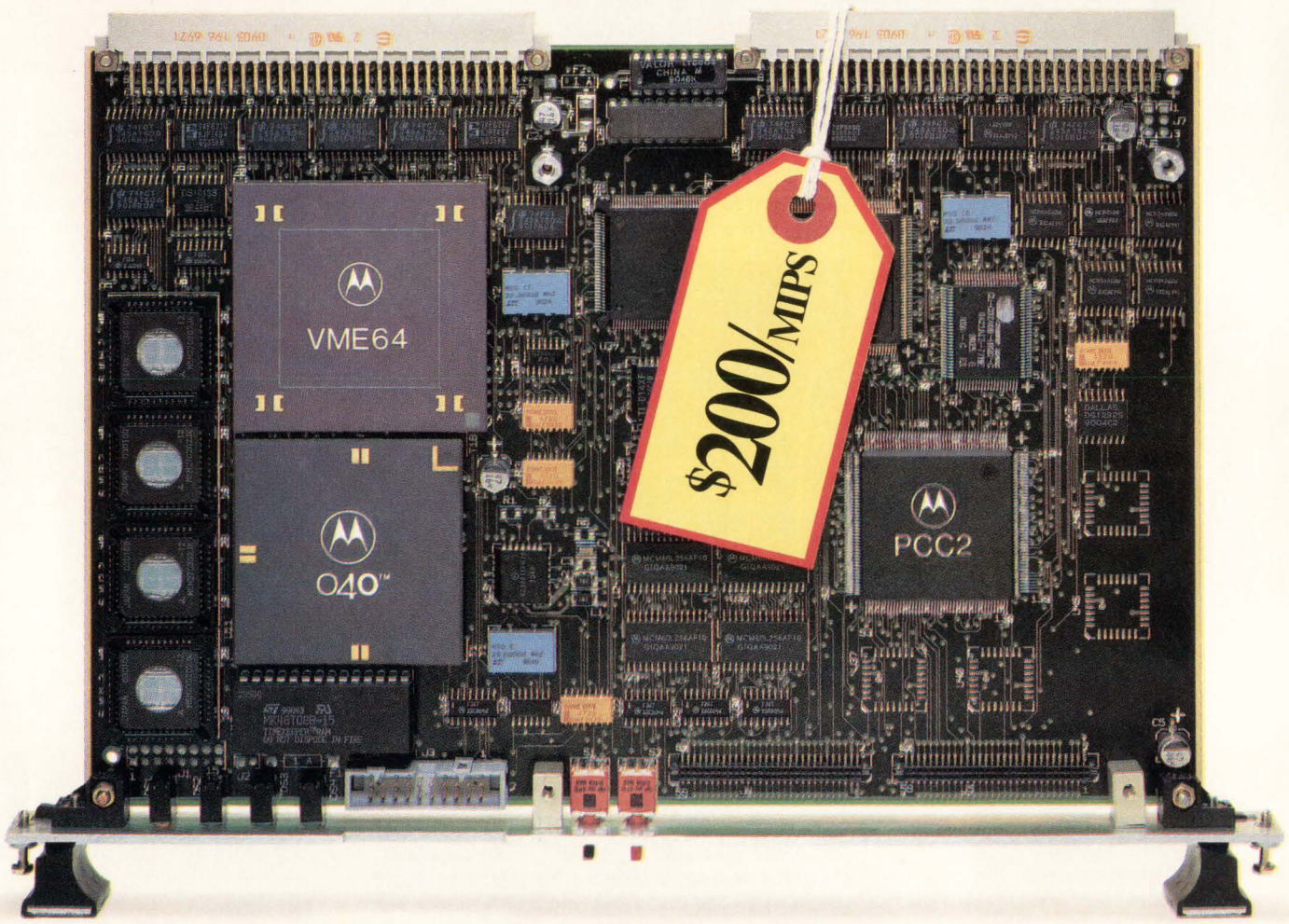

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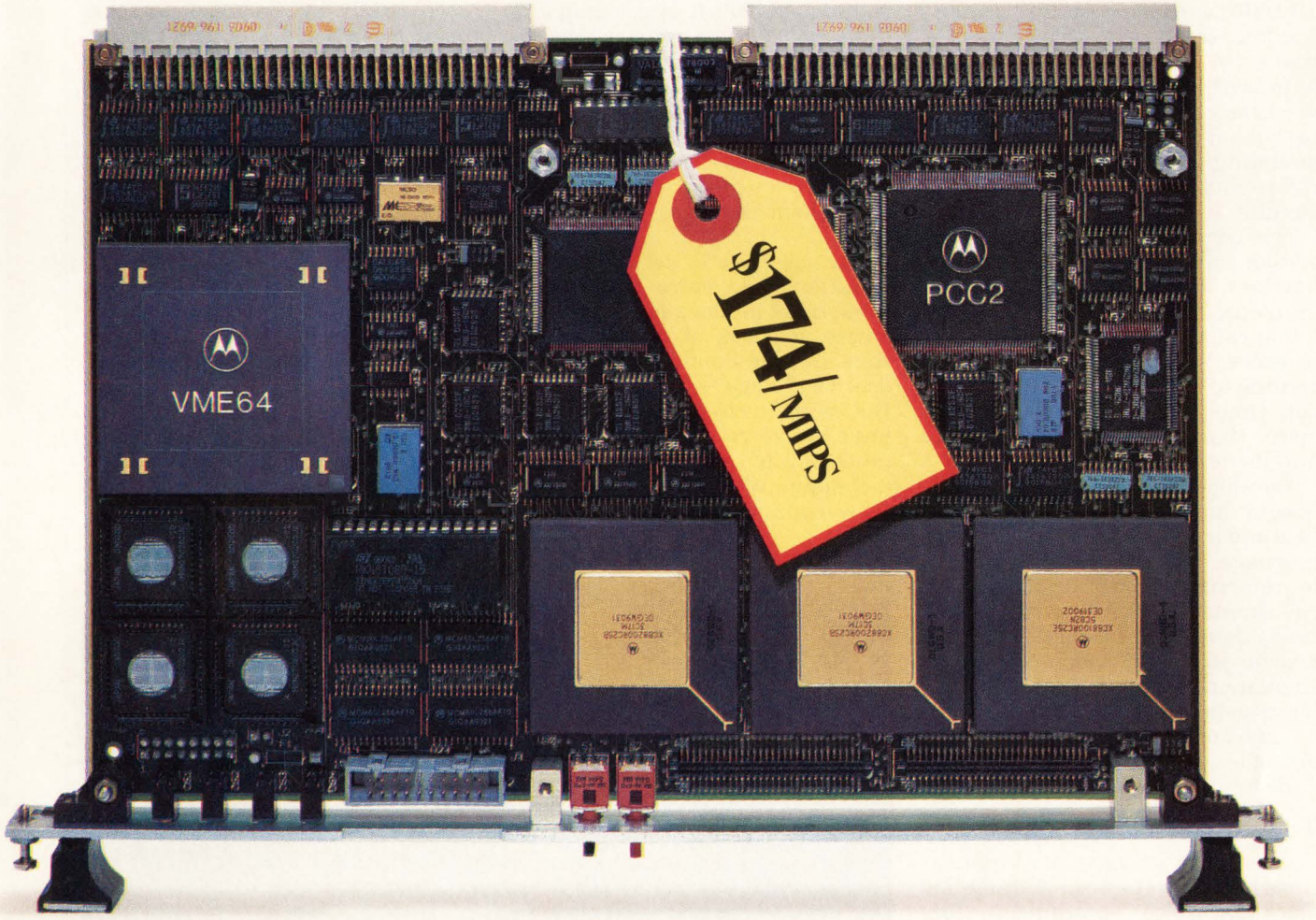

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CIRCLE NO. 20

CAE/CAD TOOLS

Analog simulator outstrips Spice in large designs

Mike Donlin, Senior Editor

Since the early 1970s, Spice has been the industry-standard analog circuit simulator. But as circuit complexities soar above the 10,000-transistor mark, Spice's weaknesses start to show. Over the years, Spice has been modified and improved by simulation vendors to meet these limitations—particularly in the areas of accurate device-modeling techniques, shorter run times and convergence of complex circuits.

Not content with simply another version of the venerable standard, however, Cadence Design Systems (San Jose, CA) has unveiled Spectre, a tool capable of simulating circuits in excess of 50,000 transistors. According to Cadence, Spectre achieves run times that are 3 to 10 times faster than those achieved by Spice and its derivatives.

Developed completely from scratch, Spectre has a new modular architecture and is written in C programming language. It uses recent innovations in numerical algorithms to yield circuit simulations faster and more accurately than Spice. In addition to handling larger circuits and speeding up simulation, Spectre offers enhanced convergence features that reduce set-up time and ensure successful completion of large simulations, according to Cadence.

Convergence snags

Convergence problems for large circuits have always been a stumbling block for Spice, according to Tom Quan, director of marketing for the analog division at Cadence. "At the beginning of a simulation run, all the nodes in a circuit are supposed to stabilize on some voltage values. In real life, that's called dc convergence. A software version of that same circuit can spend a lot of time waiting for the state to stabilize. Large circuits have feedback loops that keep changing the set-up parameters. This affects other nodes, so you end up with nonconvergence, a condition where you can't get all the nodes in a circuit to agree."

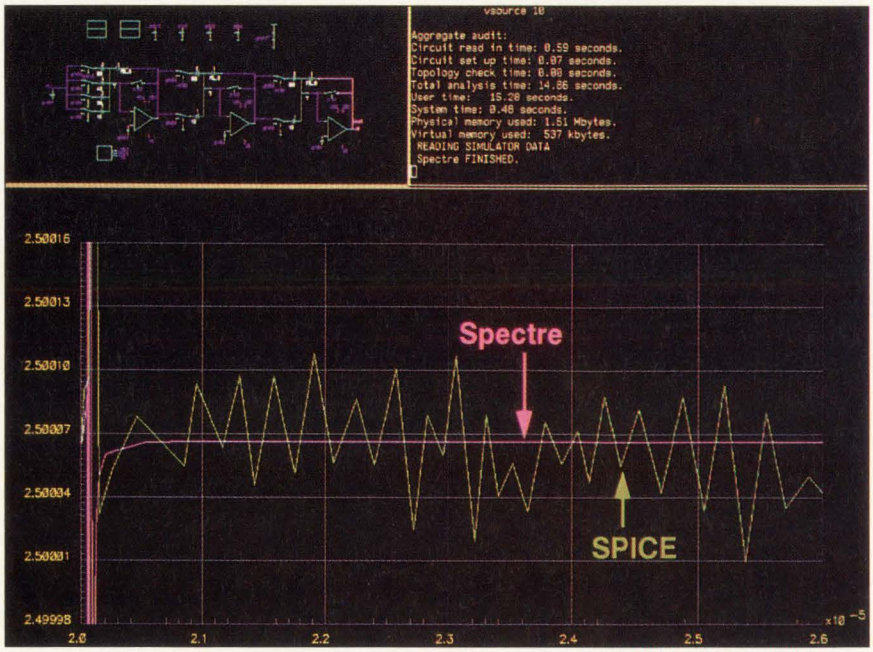
To address this convergence problem, Cadence uses an advanced sparse matrix technique and node-based algorithms. Sparse matrix techniques, which aren't unique to Cadence, let the simulator solve the complex interrelation of nodes in a device. "When you have a MOS device with a lot of set-up equations to solve, a change in a voltage or current establishes a new set of voltages or current relationships throughout the whole circuit," says Quan.

"So you have to set up all these equations and solve them at the same time, unlike a logic simulator, where you look at one event at a time. In logic simulation, if an event doesn't change, you don't touch it. But with a circuit simulator, you have to solve everything simultaneously. It's easier to use a matrix technique, which lets you solve all these equations more efficiently."

To back up its claims about Spectre's performance, Cadence cites benchmark data from the Microelectronics Center of North Carolina (Durham, NC), which simulated a total of 65 representative circuits. Spectre passed 100 percent of the convergence tests, while Spice simulations passed only 40 percent. In addition, over 200 circuits have been run successfully by Cadence partners using Spectre. In a 50,000-transistor chip simulation, Spectre posted a 10× improvement over Spice.

Spice problems aren't new

Because these convergence and accuracy issues have been around for some time, vendors who promote their own versions of Spice have learned to contend with them in different ways. The trick is to structure simulation algorithms in such a way as to get optimum accuracy without using hundreds of hours of simulation time. This speed/accuracy trade-off is usually focused on modeling techniques, and some simulator developers work with the models that drive the simulators rather than rewrite Spice from the



Cadence Design Systems' Spectre circuit simulator uses new algorithms to avoid common Spice problems (such as small time steps) resulting from piece-wise linear waveforms with many time points or transmission lines. According to Cadence, the improved time step control algorithm eliminates the numerical oscillations that are common with Spice-based simulators.

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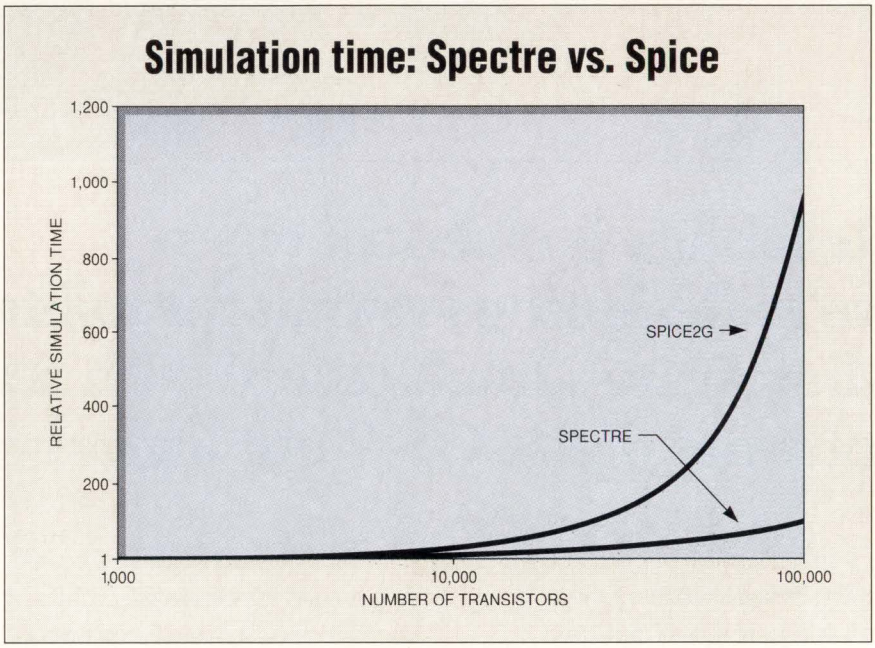
ground up.

"There's nothing wrong with the implicit numerical integration methods—the basic algorithms—of Spice," says Paul Wang, vice-president and general manager at Contec Microelectronics (San Jose, CA). "More often than not, the culprits are inaccurate device models, which result in convergence problems for the simulator. If it weren't for model inaccuracy and user mistakes, most convergence problems would disappear."

hours. "Too much simulation overhead discourages experimentation and places demands on the accuracy of the system," says Wang. "So we changed the way the model equations were written to reduce memory requirements. Our modified algorithms reduce memory size by up to one-fourth."

To back up the claim, Wang cited a simulation of a clock distribution system. An earlier version of Spice, Spice2G6, ran out of memory, while a later version, Spice3C1, took 28 min.



According to benchmarks run by National Semiconductor and Bell Northern Research, Cadence's Spectre posts 3 to 10x faster simulation times than Spice on circuits ranging from 10,000 to 100,000 transistors.

Contec's version of Spice, ContecSpice, concentrates on accurate modeling techniques to achieve reliable circuit simulations. ContecSpice provides the only commercially available analog simulation program that can simulate coupled lossy transmission lines, the company claims. At high speeds and high frequencies, interconnects behave like transmission lines, generating reflections and ringing, as well as crosstalk problems. Accurate simulation requires that such transmission line effects be taken into consideration.

But modeling these effects requires extra memory and processing power, or a simulation run can take

ContecSpice completed the simulation in 12 s—about 150× faster.

Accurate models essential

Most vendors agree that accurate modeling is the key to a reliable Spice simulation. But adding new models to Spice has been difficult for most engineers. In addition to understanding the characteristics of the device in question, model writers need to know the Spice code in which the models will ultimately run. As a result, many vendors have concentrated their efforts on model integrity and ease of use.

"Writing a simple equation for a device isn't really the problem," Cadence's Quan points out. "It be-

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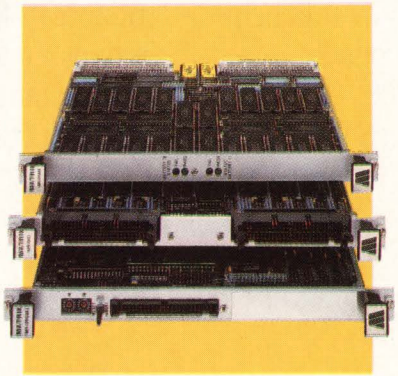

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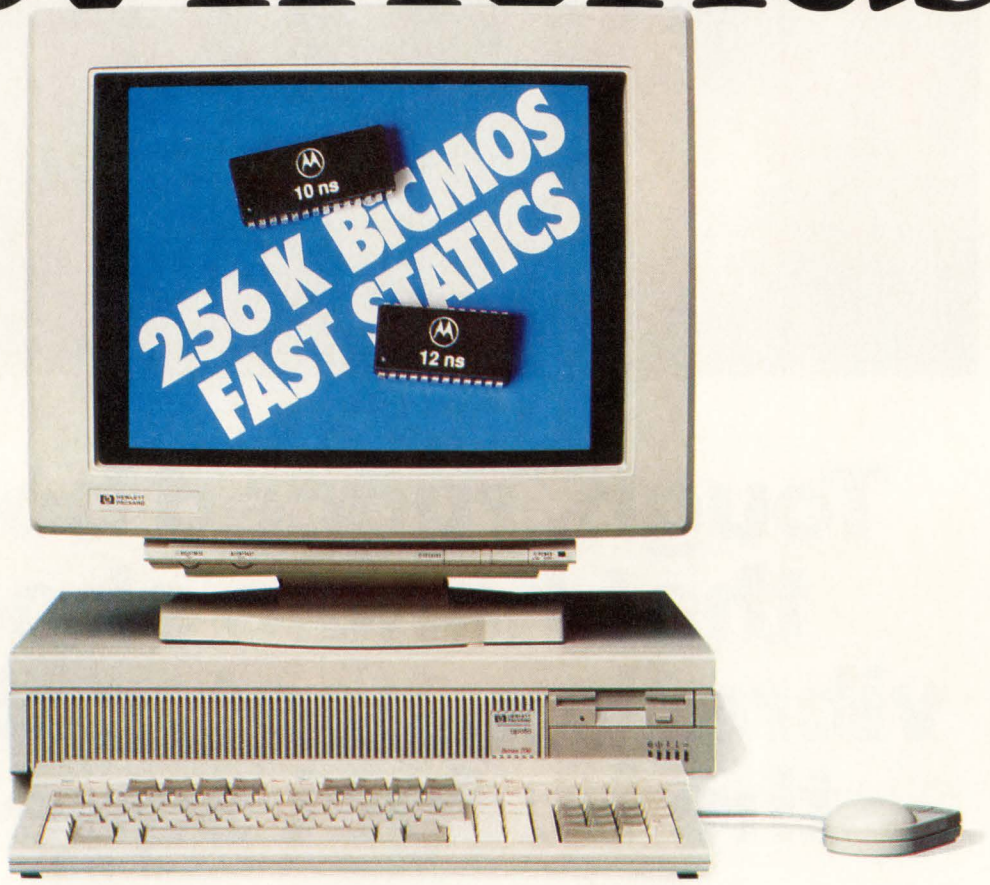

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comes difficult when you want to encode the equation into a programming language so the computer can solve it. In addition to knowing the software language involved (in Spice, it's Fortran), you need to know a lot about the relationship between the core simulator and the model code. In addition, Spice has model equations dispersed throughout many parts of the code, so you need to go through the simulator and replace each model."

"For today's analog designs that can reach as many as 50,000 transistors, we think a new simulation solution is needed to solve convergence problems and shorten simulation runs."

—Jim Solomon, Cadence Design Systems

Through a modular compiled-model interface, Spectre users can add models written in C. Because each model's code is concentrated into a single module, users can add or modify models separate from the actual simulator code.

Other vendors, working within their own versions of Spice, also have addressed the modeling issue. The PSpice simulator from MicroSim (Irvine, CA) offers an option called Parts, which semi-automates the process of creating model libraries. Using data sheet information supplied by the user, Parts estimates and verifies the parameter values to be used by the PSpice simulator. In addition, best-/worse-case models may be created for device variations and operating temperature.

Spice still the standard

Although most simulator vendors agree that Spice has its limitations, no one seems to be suggesting that it's obsolete—least of all, Cadence. "Spice has been and will continue to be a viable simulator for analog circuits in the 100-to-1,000-transistor range," says Jim Solomon, president of the analog division at Cadence. "But for today's analog designs that can reach as many as 50,000 transistors, we think a new simulation solution is needed to solve the convergence problems and to shorten simulation runs."

Not everyone agrees that Spice has run out of steam. Vendors of Spice and Spice-derivative simulators believe that with continued improvements in model accuracy and ease of use, Spice can handle any circuit that's feasible to simulate. "We can handle about 95 percent of the difficult circuits that our customers bring us with simple Spice," says Charles Hymowitz, chief applications engineer at Intusoft (San Pedro, CA). "When basic Spice fails, we have methods at our disposal, such as source-stepping, that get the circuit to converge most of the time.

"Actually there's not a whole lot to improve in Spice, so people talk a lot about convergence. To me, it's a nonissue," he adds. "As far as complex circuits are concerned, I think you have to break up the circuit to understand it anyway. Most analog engineers would tell you that it doesn't make sense to simulate an entire IC of any great complexity."

Whether Spectre will make inroads into the large installed base of Spice is anybody's guess. Cadence is banking on higher circuit complexity and increased simulation demands as a selling point, while other vendors will continue to improve on the traditional algorithms that drive Spice. One fact is certain: As analog effects creep into the behavior of high-speed digital systems, the need for accurate, high-performance simulation has never been greater. ■

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CAE/CAD TOOLS

Automated compilers let users configure their own SRAMs

Barbara Tuck, Senior Editor

Memory compilers—especially those for standard cell-based designs—have traditionally necessitated a lot of handholding between users and the factory. After parametrizing a memory with early RAM cell generators, designers had to send the database to the factory to get final silicon-layout data with accurate timing information.

A recent flurry of turnkey compiler introductions has advanced the state of the art to where systems designers, who are most often novices at memory design, can configure SRAMs to the desired level of accuracy right at their workstations. The new compilers, for submicron-to-1.2-μm CMOS gate arrays, extend this capability to both metalized and fully diffused memories. Usable gate counts in the hundreds of thousands are making it possible for designers to pull memories and other function blocks on chip and still have a good many gates with which to play. Users exploring ways to optimize their designs with regard to cost/gate/ns can either connect transistors in the base array for a metalized RAM or go with a totally customized diffusion set for an embedded RAM.

Metalized vs. diffused

Although metalized memories have the edge when design cycle time is the top priority, fully optimized diffused memories are far superior for density and speed. The many masks required for diffused memories naturally incur higher NREs (nonrecurring engineering expenses), but the level of automation of some of the new compilers eliminates any NRE charges that could be incurred for interaction between designers and the factory. And because the new compilers generate a database with up to 100 percent accurate timing information, silicon vendors have the confidence to build the diffusion set for the memories up to metalization while the gate array portion is being designed. Such concurrent design efforts make the cycle time for an embedded array more like that of a gate array than of a cell-based design.

For the first time, Motorola (Chandler, AZ) has put into its customers' hands the capability to configure application-specific, high-density, diffused memory in the gate array environment. Fully integrated into the Motorola Open Architecture CAD System, the new Memorist SRAM compiler brings a customer-defined array capability to Motorola's submicron CMOS H4C arrays, with up to 318,000 gates and 180-ps speeds. Triple-layer-metal signal and power routing provide 70 percent typical gate utilization in most applications.

Jointly developed with Mentor Graphics (Wilsonville, OR), Memorist is based on Mentor's GDT tool and written in the Genie language and C. Memorist design project leader, Jarvis Tou, says that the compiler was designed to meet application-specific memory needs with multiple architectures and with no engineering intervention. "It has to be extremely easy to use, with no handholding even for transistor-level simulation," he says. In addition to generating layout, Memorist provides all CAD support, models, netlists, and timing files.

Simulation accuracy levels

Memorist provides different levels of simulation accuracy; users can trade off simulation accuracy for CPU time. Motorola reports that benchmarks done on a 22-Mips Sun-compatible workstation indicated an

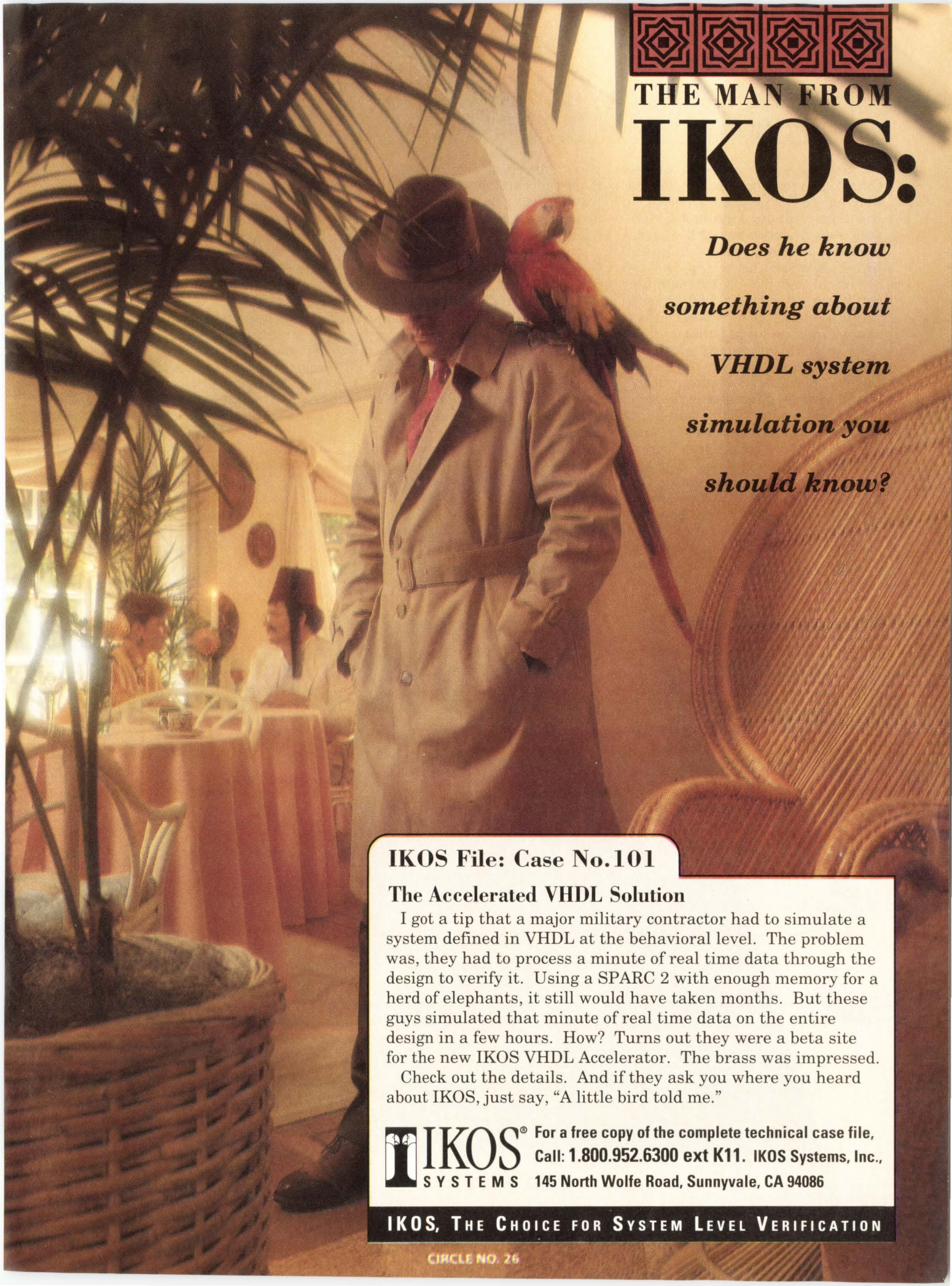
SINGLE-PORT SRAM COMPILATION TIMES

Configuration (words x width)	Front End (CPU min:s)	Back End (CPU min:s)	Total (CPU min:s)
64 x 4	0:20	19:49	20:09
512 x 8	0:20	28:57	29:17
1024 x 8	0:20	41:18	41:38
1024 x 16	0:20	61:30	61:50
2048 x 16	0:20	121:27	121:47

DUAL-PORT SRAM COMPILATION TIMES

Configuration (words x width)	Front End (CPU min:s)	Back End (CPU min:s)	Total (CPU min:s)
64 x 4	0:20	47:21	47:41
512 x 8	0:20	59:26	59:46
1024 x 8	0:20	71:34	71:54
1856 x 16	0:20	139:11	139:31

The CPU times necessary for the compilation of Motorola-developed test chip SRAMs on a 22-Mips workstation are shown above for single- and dual-port memories. Motorola used its CMOS H4C base array family to develop the test chips on its Open Architecture CAD System. The test chips contain compiled SRAMs ranging in size from 256 bits to 32 kbits in a variety of aspect ratios with one to four block implementations.



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The Memorist SRAM compiler can generate over 200,000 physical single- and dual-port SRAM configurations in sizes up to a maximum of 256 kbits. Given a word width and memory size, Memorist returns all the possible memory configurations, along with estimates of cycle time, read-access time, size, equivalent gate count, and power consumption. Minimum cycle time (clock period) for the largest single-port SRAM is approximately 15 ns using Motorola's submicron CMOS process under nominal conditions. The compiled memories automatically are placed and routed in the gate array structure. Moreover, Motorola has added an interface to isolate the RAMs for built-in self-test (BIST), leaving it up to users to customize an application-specific BIST methodology.

Quick turnaround

SGS-Thomson (Carrollton, TX) has also for the first time made single— and dual-port SRAM compilers—as well as ROM and PLA compilers—available directly to users. The compilers, referred to by SGS as "module generators," generate synchronous metalized memories for SGS' new 3.3-V-compatible submicron CMOS ISB24000 Complete family. SGS offers 18 base arrays with up to 288,000 gates (216,000 estimated usable) and a 250-ps typical loaded delay with fanout of two.

The SRAM compilers for the high-density gate arrays were developed by SGS within the Cadence Design Systems environment. SGS customers can optimize their memories for either density or performance. According to semicustom marketing manager of SGS' Programmable Products Group, Tim Chambers, the module generators give accurate prelayout information, letting users forward-annotate timing for RAM cells.

SGS uses Spice characterization to produce timing information for the leaf cells. As the compiler combines leaf cells to produce functions, it also produces overall timing for behavioral and gate-level models. Tools supported include Verilog, System Hilo and VHDL-XL. SGS offers JTAG support but doesn't offer support for BIST.

The largest single-port memory block generated by the SGS SRAM compiler is 64 kbits; 32 kbits is maximum for a dual-port memory block. Access times of 14 ns maximum are possible with memory sizes of up to

1k×8 bits. For higher performance and higher density, SGS plans to offer fully diffused embedded SRAMs and ROMs within six months.

Low on power consumption

VLSI Technology (San Jose, CA) has recently raised the level of integration available to its customers with the introduction of the VGC3RS2 gate array RAM compiler. VLSI claims that the new compiler, for VGT350 two-layer-metal, 1-µm CMOS gate arrays, is a lot more efficient than earlier compilers, which used a lot of transistor sites. VLSI, not a proponent of embedding fully diffused memories on gate arrays, has targeted its compiler at systems requiring synchronous metalized memories.

With the VLSI compiler, users can generate memories as large as 32 kbits with word widths of up to 72 bits and worst-case minimum access times of under 21 ns. Dependent on memory configuration, cycle times of 25 ns are possible. Compiled RAMs draw no dc power when the clock is fixed at a high or low state, and low dynamic power when active. This makes the compiler ideal for designs that require multiple small, low-power memories for data buffers, scratchpads or lookup tables. VLSI provides no Spice-level characterization for compiled RAMs. For testing, VLSI offers ATVG and BIST.

Usable gate counts in the hundreds of thousands let designers pull memories and other function blocks on chip and still have a good many gates left.

More embedded arrays

The IC Division of Fujitsu Microelectronics (San Jose, CA) recently announced an embedded array capability for its 0.8- and 1.2-µm CMOS gate arrays. Fujitsu memory compilers generate fully diffused single-, dual- and triple-port RAMs up to 64 kbits in size and ROMs up to 128 kbits, with word lengths up to 72 bits. Gate counts for logic implementation range from 75,000 in 1.2 µm to 120,000 in 0.8 µm. The compilers provide mixed-level (behavioral-/gate-level) simulation and test support for the compiled memories. Fujitsu is accepting design inputs with prototype

CAE/CAD TOOLS

turnaround in approximately 16 weeks.

LSI Logic (Milpitas, CA) has just announced its second generation of embedded arrays—the 0.7-µm CMOS LEA200K embedded arrays—with over 300,000 available gates and 215,000 usable gates, on which users can compile up to 256 kbits of fully diffused SRAM. The LEA200K memory compiler, part of LSI's Concurrent Modular Design Environment, lets system designers

Pulling high-density memories on chip is without a doubt the next logical step in system integration.

imbed single- and multiport fully diffused RAMs, ROMs, CAMs, and FIFOs anywhere within the cores of the 13 masterslices offered by LSI.

"Compared to cell-based methodologies," says senior vice-president Robert Blair, "this capability can speed prototypes up to one month. If a design iteration is required, the embedded technology can speed delivery time up to two and a half months."

Pulling high-density memories on chip is without a doubt the next logical step in system integration. If automated memory compilers can, indeed, ease the system designers' burden and guarantee accurate timing without engineering intervention, silicon vendors may create far greater customer interest in their jumbo gate arrays. ■

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Second-generation RISC chips: Intel intros family of i860s while Moto goes superscalar

Dave Wilson, Senior Editor

The second-generation RISC processors arriving on the scene these days share some similar features. Take the 88110 from Motorola (Austin, TX) and the N11, or i860XP, from Intel (Santa Clara, CA). Both have large on-chip data and instruction caches. Both have hardware hooks for multiprocessing, as well as multiple execution units. Both have 3-D graphics engines. But despite these similarities, the i860XP could be considered more of an evolutionary step, while the superscalar 88110 represents an architectural leap forward.

To understand the differences between the two processors, it's necessary to examine how well each architecture handles parallelism— coarse, medium and fine-grained. Fine-grained parallelism occurs at the instruction level when the execution units on the CPU can execute more than one instruction simultaneously. Medium-level parallelism occurs at the loop level, where, independent of the number of processors in a system, a number of iterations of a particular loop can be mapped to the number of processors in the system. In coarse multiprocessing, the processes are mapped out to different processors.

Parallelism isn't the only factor driving design. Sometimes, demands from the chip vendors' customer base may be key. To factor these in, it's necessary to look at a processor's past.

All bases covered

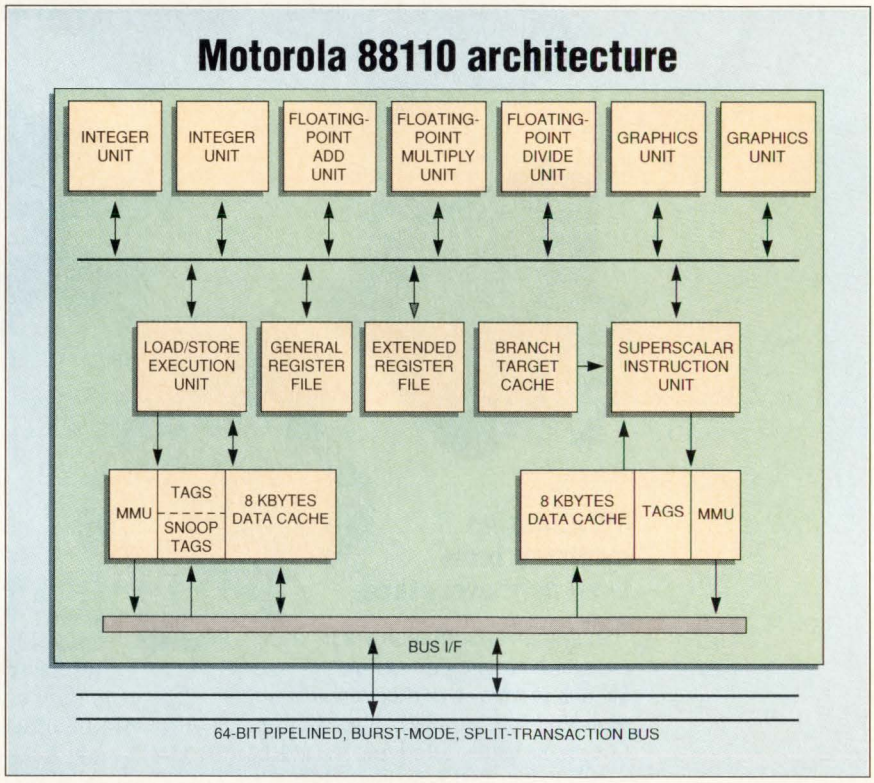
When Intel announced the i860, it was touted as a general-purpose engine. Despite design wins at Stratus Computer and Alliant, most engineers saw the chip differently. Due to its impressive floating-point capability, it was put to work as the heart of array processors and application accelerators from companies such as Mercury Computer Systems and CSPI. The graphics functionality of the device was exploited by a number of workstation companies, who surrounded the i860 with custom silicon and used it as a 3-D graphics engine.

In the design of the second-generation devices, Intel has responded to the demands of the general-purpose marketplace, the application accelerator marketplace and the graphics marketplace. As the high-end 50-MHz i860XP was announced, so too was the i860XR, at speeds of 25, 33 and 40 MHz. The price of the 25-MHz part is less than $200. Intel hopes that the price/performance of the low-range XR devices, coupled with the architectural enhancements of the higher-performance/higher-priced XP, will let it cover all the bases, from PC graphics to multiprocessing supercomputers.

Performance plus

The XP offers some improvements over the earlier device. Both the instruction and data caches are larger: while the original sported 4 kbytes of instruction cache and an 8-kbyte data cache, the XP has a 16-kbyte instruction cache and a 16-kbyte data cache. The XR only supports a write-back mode of cache operation; the XP offers both write-back and write-through options. Also, both caches now have both virtual and physical tags. These features are certain to please designers of multiprocessor systems.

Recent research from Hewlett-Packard appears to show that small caches of 4 to 8 kbytes result in a 25 percent miss rate in workstation ap-



Fine-grained parallelism: The Motorola 88110 is an architectural leap forward. Not only is the chip capable of caching 8 kbytes of data as well as 8 kbytes of instructions, but it also sports a superscalar architecture. Theoretically, this would mean that the chip could achieve a high degree of fine-grained parallelism, since the integer units, floating-point units and graphics units all could work in parallel.

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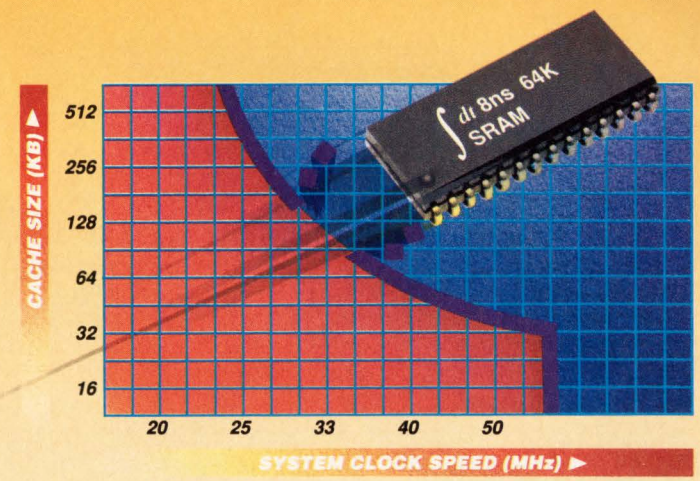

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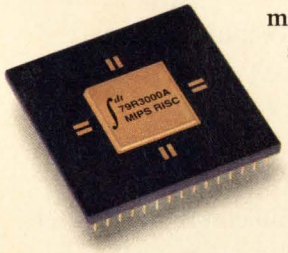

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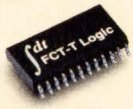

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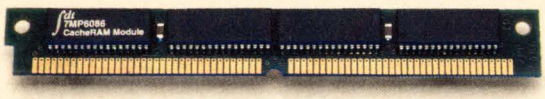

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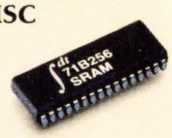

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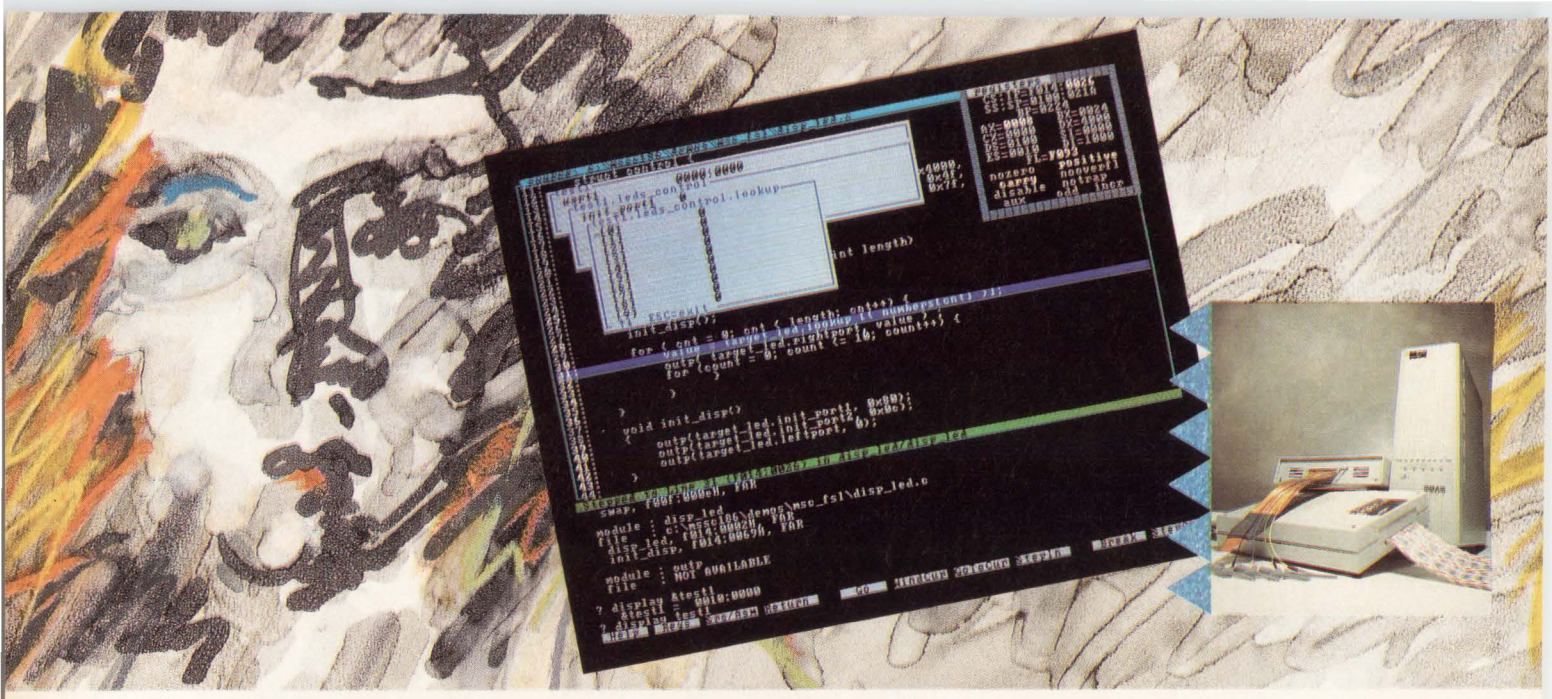

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plications, and that processing misses in the primary cache create a bottleneck. Considering those conclusions, placing lots of cache on the processor might look like the wrong way to go. Intel doesn't think so. "Unlike HP, we're not optimizing our system for a certain type of solution," says Benny Maytal, chief Intel architect for the XP. "We don't want users to need a second-level cache as a requirement in a system. If you have an 8-kbyte data cache on chip, in many cases, it's enough. On the other hand, with a bigger instruction cache you will always notice a difference."

While the i860 offered a memory bus bandwidth of 200 Mbytes/s, the XP doubles that. According to Barry Eisenstein of Mercury Computer Systems (Lowell, MA), designers

The i860XP could be considered more of an evolutionary step, while the superscalar 88110 is an architectural leap forward.

can use the chip in an existing design as a drop-in replacement, or rebuild the memory subsystem to take advantage of the faster bus. Some support has been added to handle interrupts through hardware, in addition to the original software mechanism.

In conjunction with the XP announcement, Intel disclosed details of support devices for multiprocessing architectures. These include a concurrency-control unit that supports loop-level parallelism among any number of processors, as well as a second-level cache controller coupled with intelligent cache memory (available only from Intel) that provides from 128 to 512 kbytes of write-back cache with multiprocessor cache-consistency support. The cache will be two-way set-associative with a least-recently used replacement algorithm. The memory bus interface can be either synchronous or asynchronous.

The processor protocols and policies that have been applied to the design of the second-level cache-coherency system will be applied to Intel's mainstream processor family. Soon, Intel should disclose another cache controller and more cache memory parts designed to work with the 486 processor.

At home at the high end

For its part, the Motorola 88000 has also found a home as a general-purpose CPU, as well as an embedded processor, in high-end applications. The design of the 88110 clearly indicates that Moto has no plans yet to target second-generation RISC devices at anything other than the high-performance market. The requirements of this base are somewhat straightforward: 3-D graphics, floating-point and lots of speed. The new chip is 3 to 5× faster overall than the old design; its floating-point performance will be even better.

The 88110 has two single-cycle integer units and a highly pipelined load/store execution unit. Two special function units implement floating-point and graphics; each has multiple independent execution units in them. The floating-point unit implements IEEE 754 single-, double- and extended-precision arithmetic. The floating-point adder and multiplier are fully pipelined, and the divider is a high-radix iterative design. The floating-point pipeline latencies are independent of operand precision and have been improved over the first-generation 88100. The graphics units implement a set of color pixel-processing instructions for rendering 3-D polygons in interactive graphics applications.

The internal operand data paths to the execution unit are all 80 bits wide. The register files can supply all of the operand bandwidth required to sustain the peak instruc-

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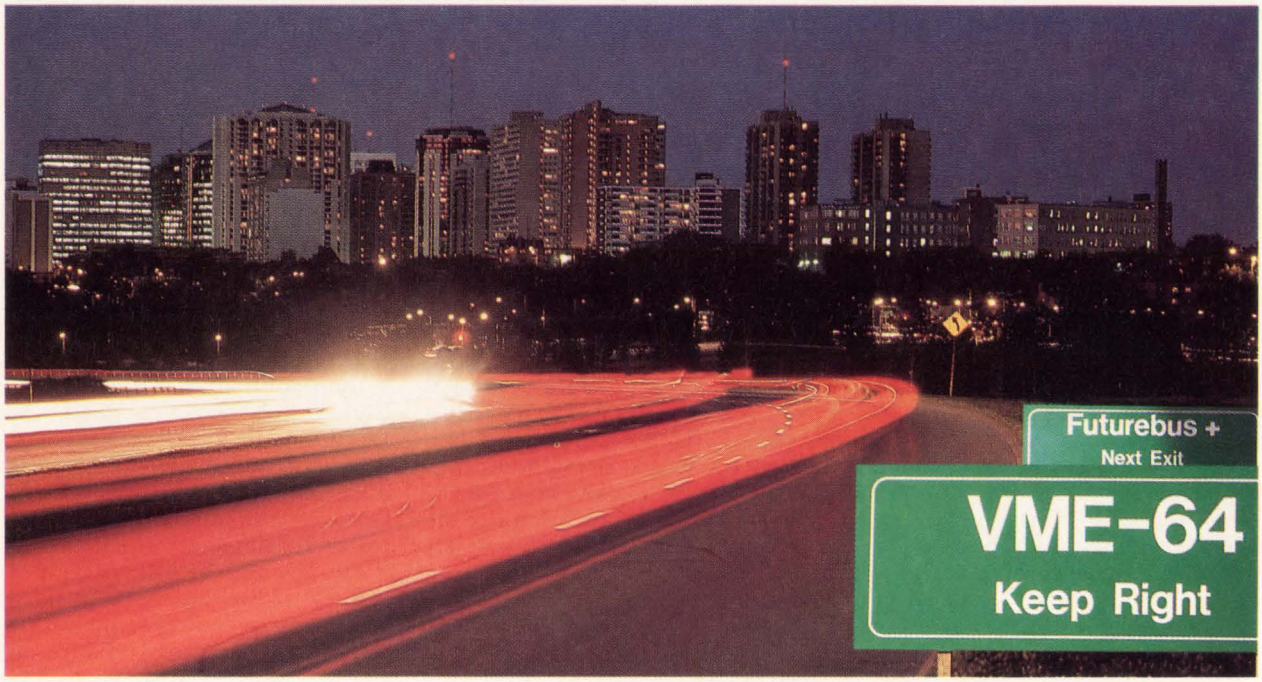

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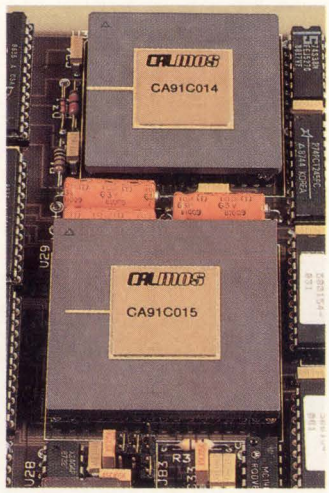

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tion issue rate, regardless of the instruction mix or operand sizes. Floating-point operations occur at the same speed, whether the operations are single-, double- or extended-precision. An internal Harvard architecture allows data and instructions to be accessed concurrently.

The instruction and data caches, which are 8 kbytes each, are two-way set-associative. The off-chip bus is a 64-bit-wide pipelined burst-mode split-transaction bus capable of supporting multiple processors. A bus-snooping protocol automatically maintains cache coherence in tightly coupled shared-memory systems. Cache is physically addressed; the chip maintains a duplicate set of tags exclusively for snooping, so that bus traffic doesn't interfere with the processor's access to the data cache. The cache uses a write-back protocol to maximize performance while minimizing bus use.

The 88110 is built around a symmetric superscalar instruction unit capable of issuing two instructions in parallel in each clock period. It imposes no artificial instruction alignment, ordering, or pairing of restrictions on the instruction stream to achieve parallel instruction execution.

In machines that execute multiple instructions per clock, branch-induced pipeline bubbles can impose a serious performance limitation. (A bubble is a period of time in which no useful work can be done because branching has broken the coherency of the instruction flow in the pipeline). In the 88110, attention has been paid to reducing branch latencies. The processor uses a special branch-target instruction cache to eliminate bubbles in the instruction pipeline caused by the delay in computing the target address and fetching a new instruction stream on a change of flow. The 88110 uses a combination of static compile-time code scheduling and dynamic run-time rescheduling to avoid pipeline hazards.

Although the 88110 completes instructions out of program order and can even execute instructions speculatively, it maintains a fully precise exception model. Whenever an interrupt or program exception occurs, the 88110 halts execution, clears its internal pipelines and automatically backs up the machine to remove any of the effects of instructions that completed out of program sequence. This leaves the machine in the precise architectural state that existed before the program exception instruction was issued.

What's ahead?

What's in store for the next generation of RISC processors? Chief 88110 architect Keith Diefendorff points to a third-generation architecture that will run instructions "wildly out of order," in an aggressive effort to seek out opportunities to execute instructions in parallel. Large internal caches, very fast wide bus interfaces and heavily buffered data units will be used to sustain extremely high throughput. Motorola is developing a BiCMOS process to manufacture the processor. Before that, however, Motorola will announce support chips to support a second-level cache for the 88110.

Clearly, many previous RISC architecture aficionados would like to discount the 88110 and the i860XP as coming too late in the market to make a difference. But there are more applications for a RISC processor than simply to form the heart of an engineering workstation. With its $200 XR, Intel may have recognized that higher volumes are to be found in embedded applications. It will be interesting to see if, or how, Motorola positions future 88XXXs for the embedded world. ■

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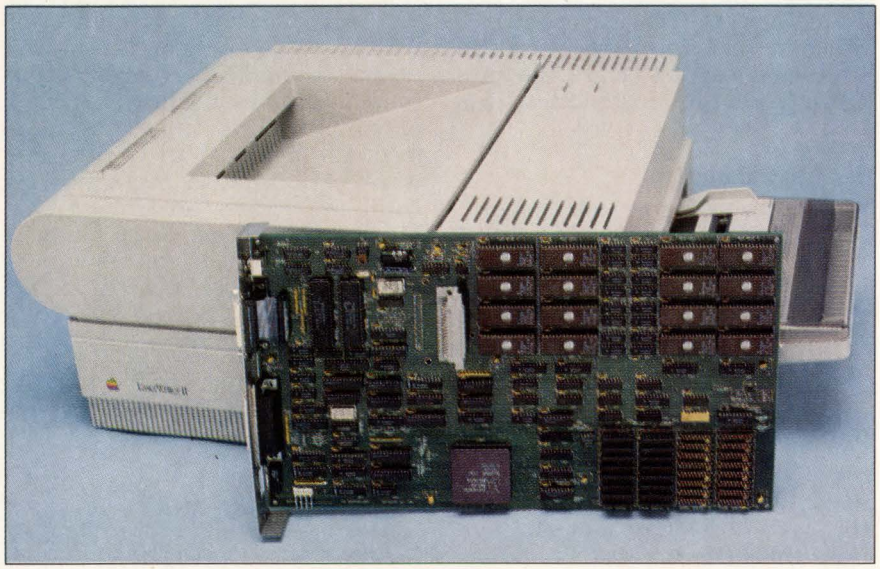
New 29000s promise faster laser printer designs



The Xante 29000-based PostScript controller helps improve the performance of Apple LaserWriters. Advanced Micro Devices' new 29035 processor could help manufacturers such as Xante reduce the board size, decrease the cost and improve the performance of their products.

Dave Wilson, Senior Editor

Further staking out its claim in the embedded marketplace, Advanced Micro Devices (Austin, TX) has released two new members of its RISC 29000 processor family, the 29030 and the 29035. Retaining software compatibility with the 29000, the new parts differ primarily in speed, size and variation of on-chip cache and packaging. While the 25- and 33-MHz versions of the 29030 offer an 8-kbyte two-way set-associative instruction cache containing 512 blocks, the 16-MHz 29035 uses a 4-kbyte direct-mapped instruction cache containing 256 blocks. Neither of the devices sports an on-chip data cache. Both parts seem to be just what the doctor ordered—if the doctor specializes in designing laser printer controllers.

Fine-tuned cache

While instruction cache has moved on chip, the branch target cache (BTC) used in the 29000 has moved off. After touting the BTC approach when the 29000 was originally announced, AMD has taken a turn in a different direction—and many users may be asking why.

Mark Hill, a professor at the University of Wisconsin, wrote his postgraduate thesis on the subject of cache memories. "If the instruction cache is less than 512 bytes, the BTC approach has an advantage," says Hill. "If the size is 8 kbytes or larger, the conventional instruction cache wins. The question is, what about the sizes in the middle?"

Apparently, the factor that determines the optimum cache sizes in this middle ground is the rate at which instructions can be accessed from off-chip memory. "If you can stream instructions from off chip quickly, then BTCs still compare favorably. On the other hand, if off-chip access is slow (because the processor is so fast that it takes several cycles to get anything from off-chip memory), then this tends to favor the conventional instruction cache approach," Hill concludes.

Aside from cache, the other major difference between the new parts and their predecessors is the addition of a programmable (8-, 16- or 32-bit) instruction/data bus; the 29035 also supports a programmable 16- or 32-bit data bus width. Of the two parts, the 035 will be the least expensive. Packaged in a PQFP, samples will be available in the third quarter. The 030, on the other hand, will be available as a 145-lead pin grid array; samples are available now.

Proof is in the printer

Many vendors now offer 29000-based laser printers and printer controller boards. "But since the design of a specific (RISC processor) board is very dependent on the memory architecture used, the performance of these boards can vary greatly," says Pat Wood, vice-president of R&D at Pipeline (Morris Plains, NJ).Wood's firm developed PowerPage, a LaserWriter-/Linotronic-compatible implementation of Adobe's PostScript that runs on the 29000 processor.

Another firm, Xante (Montrose, AL), manufactures 29000-based controllers that offer a 4 to 10× improvement in PostScript performance when used to replace existing controllers in Apple LaserWriters. Robert Ross, president of Xante, led the choice of the 29000 for the design of the controller board. He's also enthusiastic about the new AMD derivatives, especially the 29035. "The most complicated thing about the 29000 is that you have to get one instruction per clock cycle to the CPU to get the most performance out of it. That's very difficult with the 29000," says Ross. "But the 4-kbyte instruction cache [on the 29035] will simplify our design significantly."

To keep the processor fed with instructions in the Xante controller design, Ross needed to bank-interleave four banks, each consisting of four 1-Mbit EPROM devices for a total of 2 Mbytes of EPROM storage. Looking at the board, it's evident that this approach, while effective, took up a lot of board real-estate. In fact, in addition to the 16 EPROMs, around 20 glue parts are used simply to perform the interleaving.

"The 035 device with its 4-kbyte cache will allow us to use more dense EPROMs and not rely so heavily on EPROM performance," says Ross. With the 035 chip, Xante would be able to use four 4-Mbit EPROMs in the design. Further-

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more, the EPROMs wouldn't need to be interleaved to eliminate memory wait states, because the 4-kbyte on-chip cache would mean that around 85 percent of the time instructions would execute from zero-wait-state cache. This, in turn, would mean a smaller, less-complex board. "I would use the 29035 today if it were available," concludes Ross.

Performance upgrades simple

Because the new RISC processors offer scalable clocking capability, a feature that lets the processor bus run at half the processor clock rate, designers will be able to make performance upgrades without redesigning boards at all. As AMD introduces faster processors, designers will be able to use a 50-MHz 29030 in a 25-MHz board design. While the processor runs at twice the speed of the board, it can manage the memory interface to the slower memory. Instructions will run out of the processor cache at full speed; the rest of the instructions will run with a couple of wait states from on-board memory.

The 030 and 035 also let designers lock frequently used instructions into the cache. The instruction cache is locked by an instruction cache lock (IL) field. The value contained in the IL field determines which portion of the cache is locked. Locking a block prevents replacement of the block if it's valid; however, an invalid block may be replaced. In the 29030 processor, the IL field has the effect of locking the entire cache, locking only half the cache, or not locking the cache and allowing normal operation; in the 29035, the IL field has the effect of either locking the entire cache or allowing normal replacement.

"The ability to take one or both pieces of the cache on the 29030 and load it up with a program and lock it in is very nice," says Pipeline's Wood. In effect, you can make the cache a read-only device. If you have some low-level rendering code (rasterization code) smaller than 2 kwords, you can really benefit from this capability. That's the sort of thing we're looking to do."

For designers of higher-performance systems, AMD's 29000 road map points to a higher-performance device that's on the way. The device will undoubtedly incorporate a superscalar architecture, just as AMD's number one competitor in the RISC embedded market, Intel, has already done with the i960. ■

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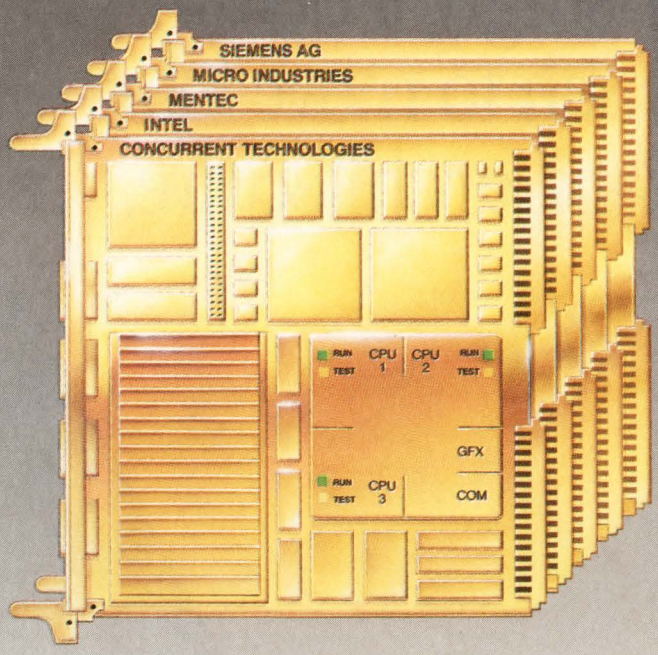

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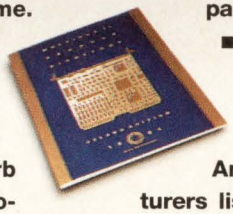

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CIRCLE NO. 35

COMPUTERS AND SUBSYSTEMS

PC-based controllers tackle time-to-market demands of embedded applications

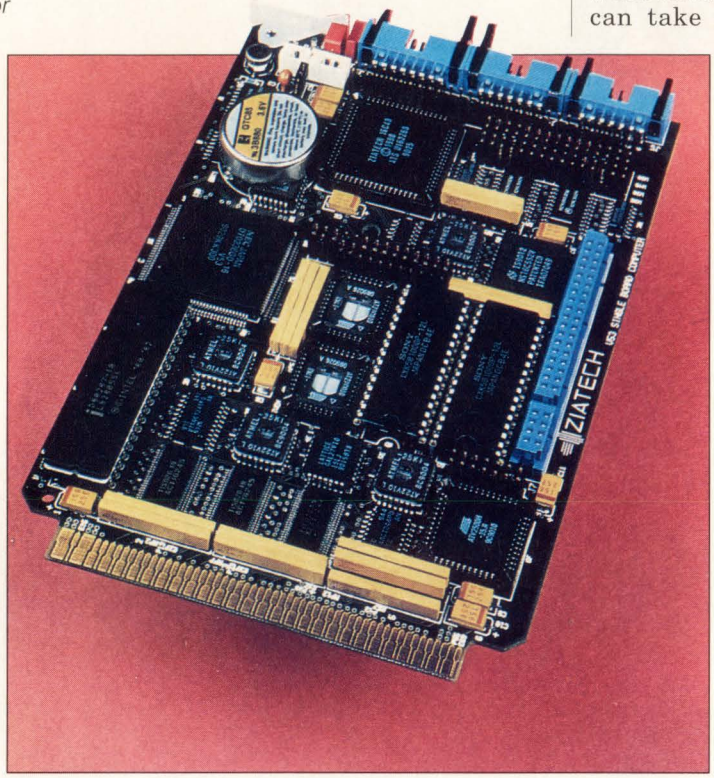
Warren Andrews, Senior Editor

As the embedded PC market continues to expand, OEMs are demanding more-compact, lower-cost and higher-performance systems for industrial applications. And as time-to-market pressures continue to escalate, designs must be turned around in months, instead of the year or more required to design a system from scratch.

The latest efforts to meet the need for higher performance, more-flexible I/O and faster time-to-market come in two distinctly different packages. The first is from Ampro Computers (Sunnyvale, CA), which has expanded its family of compact, stackable PC modules to include a 16-MHz 286 CPU, the CoreModule/286.

While Ampro offers a modular solution, Ziatech (San Luis Obispo, CA) has developed an alternative at the other end of the spectrum. Looking to satisfy OEM requirements for inexpensive, single-board PCs with customized I/O, Ziatech developed its Application-Specific Automation Processor (ASAP) technology. ASAP lets OEMs fully customize their I/O on a standard-configuration STD 32 board.

"Ziatech's approach brings to OEMs using board-level PC solutions some of the same advantages that board makers enjoy with ASICs," says Jim Eckford, Ziatech's vice-president of sales and marketing. "Our ASAP approach takes a standard-platform PC based on the NEC V53 286-compatible processor, and allows the customer to add whatever I/O or other functions are required. Using our latest CAD equipment, we're able to take the basic V53 building block, add the required functionality and deliver the finished, customized board in only 12 weeks."



A custom embedded PC-based controller on a standard bus card can be developed in only 12 weeks when its design relies on a library of tested function modules. Ziatech's Application-Specific Automation Processor series lets users specify custom controller configurations of modules around a 16-MHz 80286-compatible processor core.

Although the ASAP processors are built on a standard STD 32 board complete with card-edge fingers, most customers never use the connector, says Eckford. Instead, OEMs most often use only the single board with no backplane or card cage.

Benefit to standard boards

The standard board approach provides the customer with two advantages. First, says Eckford, it gives OEMs the possibility of expanding the system in the future by adding a limited card cage and connectors. He also points out that even though the design is custom, it's based on standard STD building blocks. So, during an ASAP's 12-week development cycle, customers can take a standard set of STD boards and proceed with software development as if they were working on a target system.

In addition, the base CPU function includes an iSBX expansion connector to accommodate functions that may not fit on the CPU board, or that may be optional for the customer. Ziatech and a broad range of other manufacturers provide iSBX modules ranging from general-purpose interface bus (GPIB) controllers and multiple digital I/O to data-acquisition and servo-motor controllers.

"OEMs are facing increasingly stiff competition both here and abroad; cost, time-to-market and performance are critical to their market acceptance," says Eckford. "Modular approaches, using either standard buses or proprietary connectors, don't always provide the most cost- and space-effective solutions." Too often, he adds, development constraints force acceptance of less-than-ideal solutions. With a semicustom approach, he says, many of these development constraints are eliminated.

At the core

Ziatech's core module is based around a 16-MHz NEC V53 processor. It provides 16-bit processing power with full I/O and code compatibility with 80286 processors. The core module—around which custom I/O is provided—is designed for control-oriented applications. In addition to the processor, the module includes memory, processor-specific peripherals, and STD 80 and STD 32

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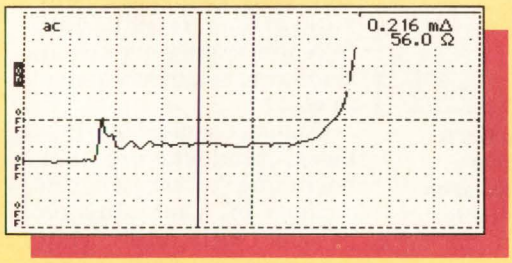

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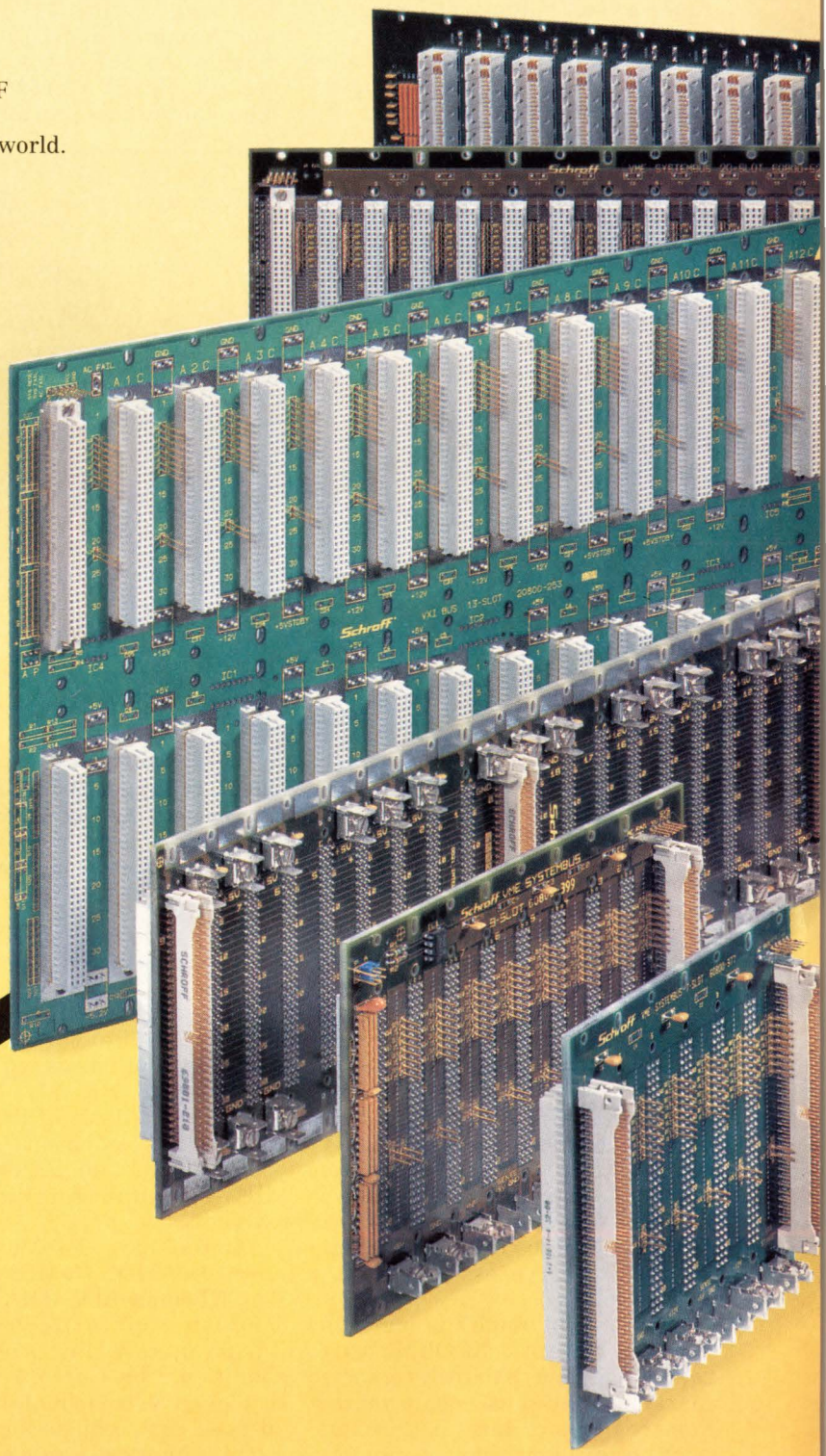

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CIRCLE NO. 36

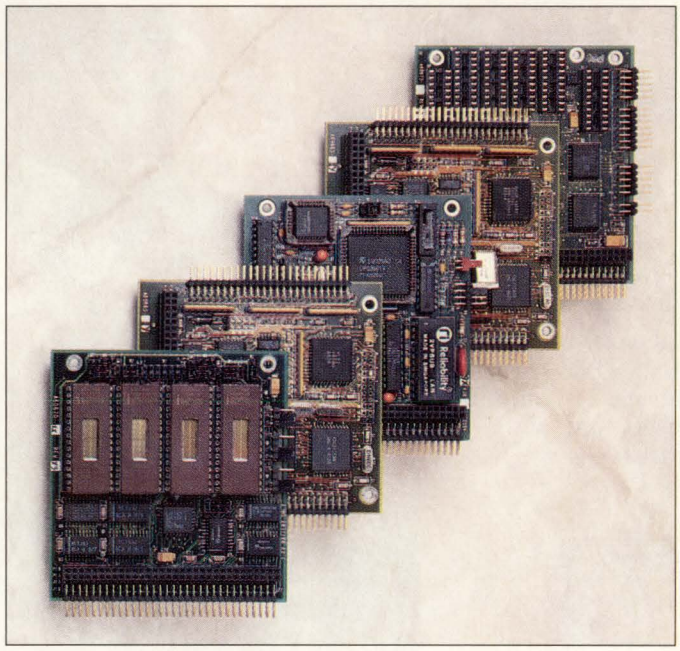
COMPUTERS AND SUBSYSTEMS

bus interfaces. Peripherals included in the core include a single RS-232 port, a programmable interrupt controller, three 16-bit counters, three DMA channels, a real-time clock, power-fail detection, a watchdog timer, a reset button, and a programmable LED.

"The application-specific module library is designed to give the designer optimum flexibility while staying within the confines of the standard board," says Eckford. "The amount of I/O that will fit on each card depends on the particular I/O library modules selected."

Typically, he says, about three modules can be squeezed onto a standard 4.6-×6.5-in. STD form factor board. The core module occupies roughly 70 percent of the board's real estate.

Typical library modules include dual-synchronous serial communications channels, a 48-point parallel I/O module, an Arcnet interface, and a GPIB interface. In addition to standard library modules, ASAPs can accommodate fully custom I/O. But, says Eckford, fully custom circuits take more time to develop and test compared to the standard library modules, which are all proven and tested.



One approach to the customization of PC-based controllers is Ampro's MiniModule series. System developers customize controller functions by specifying the appropriate combination of function cards, including processor, memory and I/O cards.

Stack pack

One alternative to custom, semicustom or standard buses is Ampro's line of MiniModules, palm-sized (3.6-×3.8-in.) PC boards with stack-through header connectors. (Actually, the family of embedded-system modules comprises MiniModule expansion peripherals and CoreModule CPU boards. The header connectors serve essentially as a stackable bus.)

Ampro's philosophy is much the same as Ziatech's. "If OEMs are to compete in today's fiercely contested markets, they must get to market quickly with products that are compact, affordable and geared precisely to an application's requirements," says Rick Lehrbaum, vice president of engineering.

The most recent additions to Ampro's family of MiniModules include a SuperVGA board, an Ethernet card, a solid-state disk module, and a pair of interface modules to handle the 16-bit bus of the company's latest CoreModule/286. These interfaces provide an RS-232 serial port, a SCSI or IDE interface (two versions), and floppy drive controllers.

The solid-state disk provides four 32-pin sockets for byte-wide memory that can accept either 28- or 32-pin SRAM, NOVRAM, EPROM, or flash EPROM devices. It includes provisions for battery back-up for the SRAM and lets OEMs offer fully functional diskless systems.

Ampro's new CoreModule processor uses AMD's 16-MHz 286 processor, AT-compatible DMA controllers, and interrupt controllers and sockets for up to 4 Mbytes of DRAM. In addition, the CoreModule/286 includes an AT-compatible bidirectional parallel port, configurable as either a printer interface or an 8-bit general-purpose I/O port; an RS-232 serial port; keyboard and speaker interfaces; and a real-time clock.

On-time development

The approaches taken by the Ampro and Ziatech product offerings—as well as similar single-board PC-based products from a variety of other vendors—underscore the critical value of standards in timely product development. Embedded controllers such as these are rapidly becoming the next-generation microcontrollers. They're also MS-/PC-DOS compatible, fully programmable and built for industrial applications.

At least for the present, however, such solutions are still too expensive to fit into traditional microcontroller applications. Ampro's MiniModules, for example, sell for somewhere between $100 and $150 each, which is two to four times the cost of a comparable microcontroller solution. But time-to-market considerations might well take precedence over even that large of a discrepancy in cost.

Compact embedded PC-based products are just beginning to scratch the surface of what may be possible with future chip development. Only three years ago, a compact PC-based module sold in the $500 to $700 range. With higher levels of IC integration, higher sales volumes and improved packaging techniques, prices will continue to fall. Some experts estimate that a complete PC for embedded applications will sell for well under $50 within the next five years. ■

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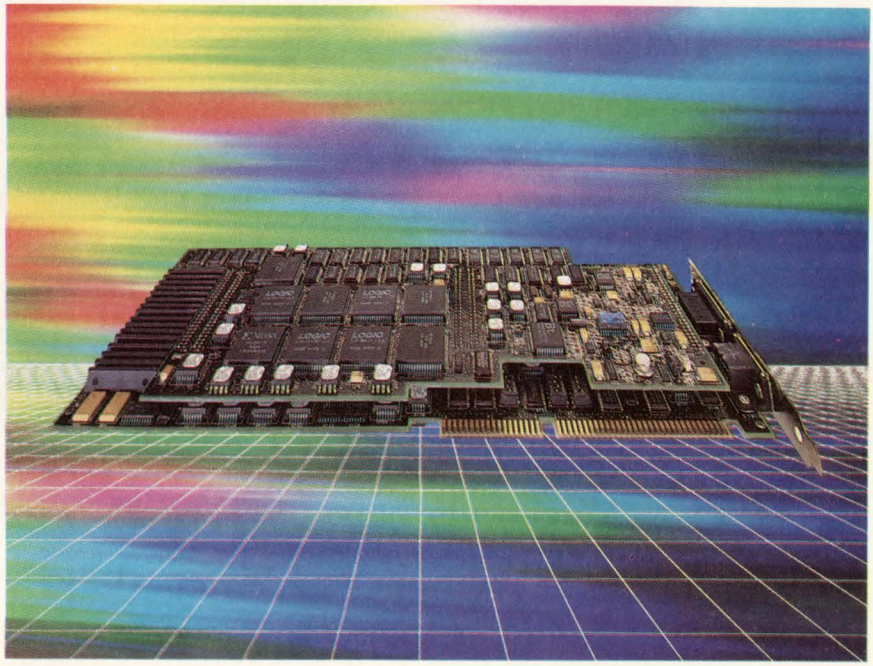

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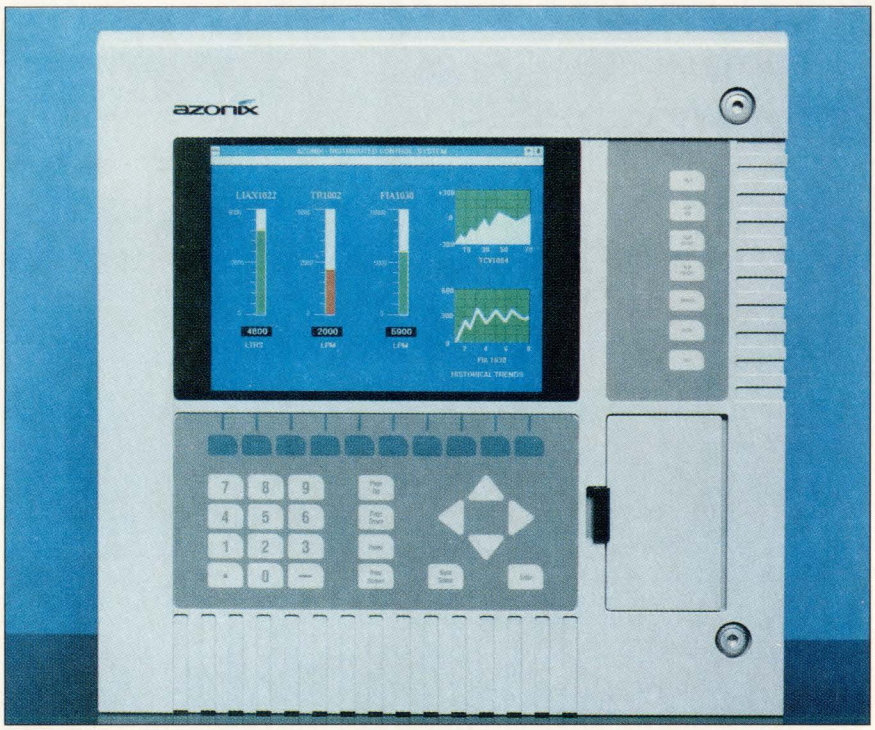
CIRCLE NO. 37

COMPUTERS AND SUBSYSTEMS



This compact industrial computer is ruggedized for NEMA-4 and -12 rated environments. The Azonix ProPanel is based on the PC/AT architecture and has a VGA-resolution color LCD screen with 8- or 256-color capability.

PC platforms ruggedized for industrial environments

Warren Andrews, Senior Editor

With hundreds of industrial software packages available for the IBM PC and compatibles, it's no wonder PCs are the popular choice for a broad variety of industrial-control applications. But hostile industrial environments—with extreme temperatures, airborne abrasive or conductive particles, corrosive pollutants, severe electrical noise, and vibration—are natural enemies of exposed electronic systems and the delicate mechanisms of disk drives. So OEMs and end-users have taken great pains to protect PCs from these environments.

A number of clever PC platforms are starting to emerge as solutions to the industrial environment dilemmas. One recent entry is a relatively low-cost, single-board solution from STD board maker Computer Dynamics (Greer, SC). Called DisplayPac EL, its front end combines a high-resolution monochrome electroluminescent (EL) display with a full 80386 PC/AT computer and an infrared touch-screen interface, all in a single compact (10.5-×6.875-×3.375-in.) package.

At the other end of the spectrum is a full, passive-backplane PC replete with a color LCD. Dubbed ProPanel by its maker, Azonix (Burlington, MA), the compact PC is packed in a NEMA-approved enclosure designed for convection cooling. Like Computer Dynamics' display, ProPanel features a relatively small form factor (17×17×8 in.) but includes shock mounting for direct installation on a wall.

DisplayPac's bright screen and gray scales are designed to be readable in a variety of industrial environments and lighting conditions. "The high-performance EGA EL display provides a bright amber image with high resolution (640×400) and excellent readability from any viewing angle, even exceeding 160°," says Kurt Priester, president of Computer Dynamics.

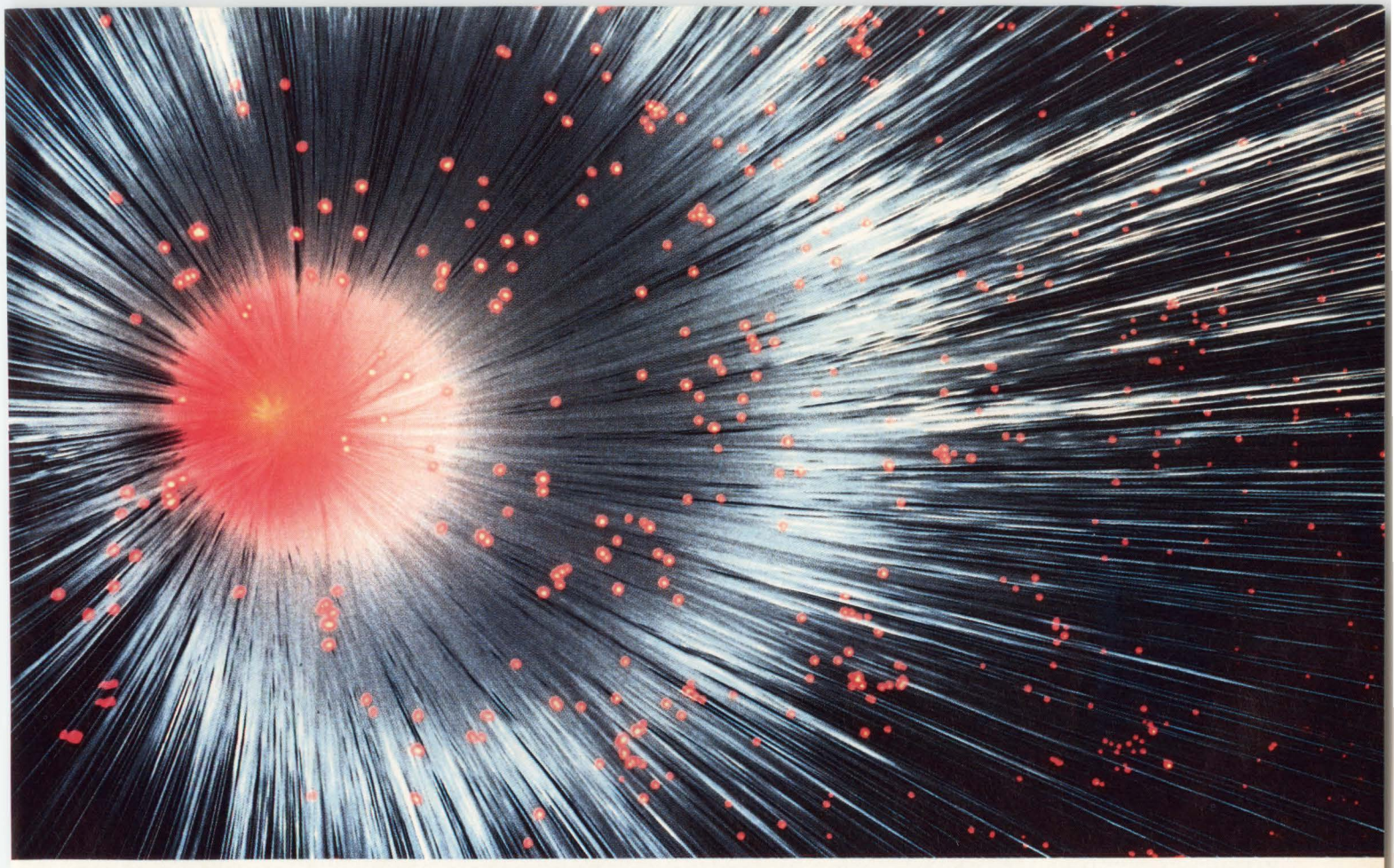
Computer Dynamics' single-board computer is powered by an 80386 CPU operating at 20 MHz. (A 12-MHz 80286 version is also available.) It drives the EL display as if it were a standard CGA/EGA CRT and offers the full complement of PC/AT functions. Options allow for up to 16 Mbytes of RAM, a 1-Mbyte EPROM, a speaker and keyboard ports, two COM ports, a printer port, a real-time clock, hard and floppy disk interfaces, an 80287, a math coprocessor socket, and a watchdog timer.

The system clearly was designed to withstand industrial environments. While it supports floppy and hard disk drives, it also can boot and run MS-DOS and an application program from its on-board ROM disk, allowing for a diskless target system. And, although the system is designed to be extremely compact, the interface can accommodate up to two external standard PC option boards for system expansion.

Full-color LCD display

Azonix has taken a somewhat different approach by providing the rugged interface along with specialized packaging, which meets NEMA-4 and -12 environmental requirements. "Replacing a CRT with the full-color LCD display let Azonix trim the total power requirement to only 25 W. This eliminates the need for fans and other cooling devices," says product manager Jena Araki. With the built-in heat sink the internal temperature rise is limited to 5°C over ambient temperature.

The small temperature increase also contributes to increased reliability, she adds. In addition, Araki says, the metal enclosure provides EMI/RFI radiation protection, and can withstand hose-downs and contact with noncorrosive chemicals. Even the control panel is what Araki calls "industrial strength"—a sealed-membrane type designed to withstand tough handling. And the optional hinged door, which allows access to the floppy disk, is sealed and fully complies with the NEMA ratings.



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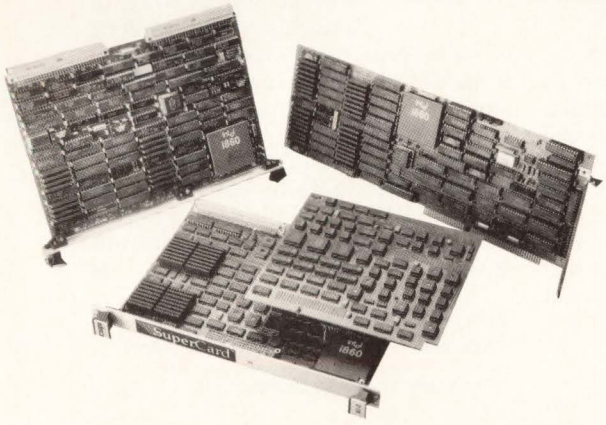

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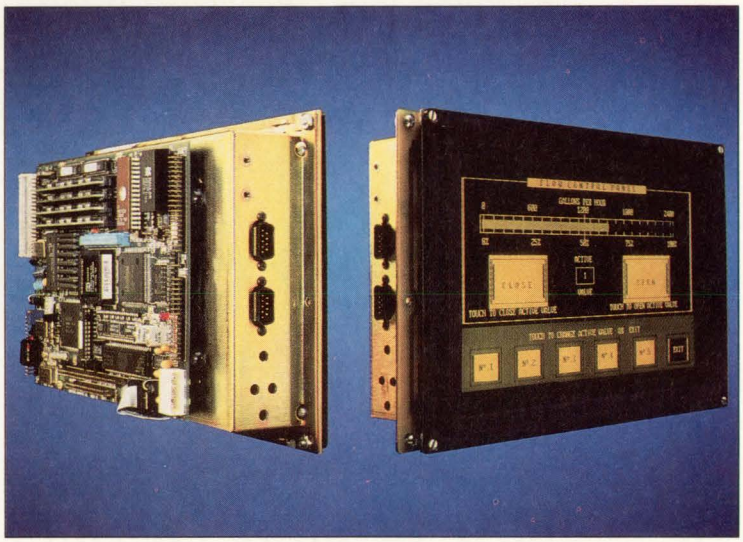
CIRCLE NO. 38

COMPUTERS AND SUBSYSTEMS

The color LCD built into Azonix' ProPanel is a thin-film transistor active matrix with a transistor per pixel that permits a wide viewing angle. The display provides VGA resolution (640×480) and is available with either 8 or 256 colors. The bright color display greatly simplifies interpretation of screen images, particularly warnings of hazardous conditions.

The computer housed in the enclosure is a passive-backplane PC that uses either an 80286- or 80386-based CPU card with a minimum of 1 Mbyte of RAM. In addition, the system is supplied with a 40-Mbyte, 2½-in. hard disk, a 1.44-Mbyte 3½-in. diskette drive, either two or four serial ports, and a parallel port. The serial ports are user-configurable for RS-232C, -422 or -485 protocols. In addition, they're optically isolated, and consistent with the industrially hardened package. The system backplane has two additional ISA slots, which can be used for optional plug-in adapter cards, such as Ethernet; for other communications schemes; or for other cards, such as data acquisition.



Meant for environments where standard PCs and CRTs would fail, this touch-sensitive 640x400 gray-scale electroluminescent display fronts for a full 20-MHz 80386 PC/AT processor. Computer Dynamics' DisplayPac EL mounts into a sealed enclosure, leaving its display accessible.

Azonix has paid particular attention to system security. A special door that lets engineers access the diskette, the parallel port, and an auxiliary keyboard port are all electronically locked and can only be opened with the proper password entered from the operator panel. The operator panel is a 35-key, sealed-membrane unit with tactile feedback. In addition to the standard numeric keypad, provision is made for softkeys, which can be configured by users.

Applications limited

Even before products such as Computer Dynamics' DisplayPac-EL and Azonix' ProPanel, conventional CRT-based PCs have been forced into service in industrial applications. Both as conventional PCs and as hybrid PCs residing on another bus architecture such as VME, STD or Multibus, these systems take advantage of the many popular process-control applications packages available.

Products such as Intellution's FIX, Iconic's Genesis, WonderWare's WonderWare and 50-or-so others focusing on everything from building and plant management to batch chemical processing provide a wealth of resources for control system developers. And these products bring reliable PC-based technology to the factory floor environment.

The human interface, however, is only part of the processing story. Although relatively simple control functions can be handled by the basic DOS display system provided by DisplayPac-EL and ProPanel, the limited processing power of the PC, the restricted add-on capabilities and the fundamental limitations of the ISA architecture largely limit applications to a single task.

Even when PCs have been integrated with other buses in hybrid solutions, the PC function has been largely relegated to the human interface. Bucking the trend, RadiSys (Beaverton, OR) recently introduced a PC-based VMEbus platform that lets both the process control and the human interface operate on the PC.

More and more, however, real-world applications are calling for the kind of increased sophistication found in multiprocessing systems, which aren't easily—if at all—allowed in the ISA architecture. Therefore, such systems remain restricted to serve as front-ends to other systems, which are usually VME- or Multibus II-based. However, EISA, the 32-bit extension of ISA, can handle multiprocessing—with the help of a little software magic. Last month marked the first get-together of parties interested developing a specification for passive-backplane EISA. After "slot zero" protocols and a few other issues settle out, such an architecture may show significant promise.

Thus, the logical extension to PC-based industrial-control systems will be to migrate to something more closely resembling an EISA architecture. One alternative might well be something like STD 32, developed by Ziatech (San Luis Obispo, CA). STD 32 is based on the basic EISA chip set but packaged in an industrially hardened STD form factor. According to Ziatech's vice-president of sales and marketing, Jim Eckford, STD 32 has already solved the slot zero problem and will soon be announcing a multiprocessing version of DOS for STD 32. Other solutions could include conventional passive EISA backplanes wrapped in hard packaging, such as that from Azonix. ■

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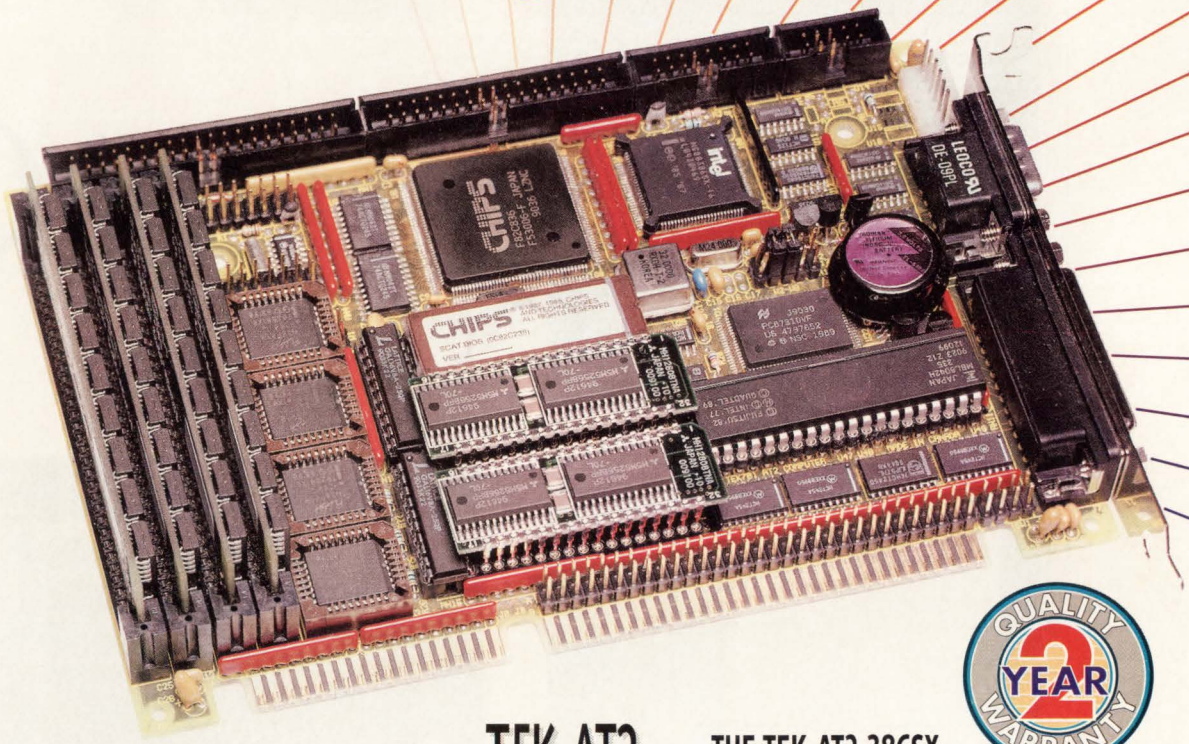

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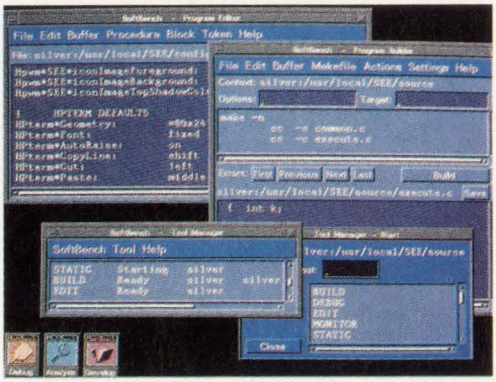

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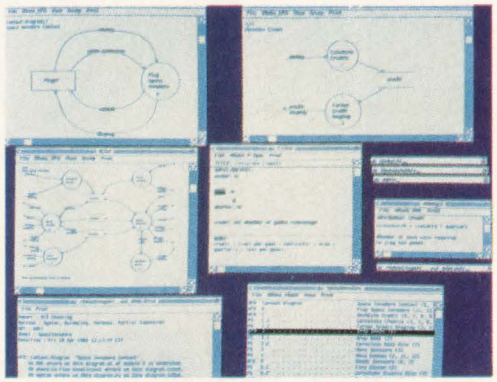

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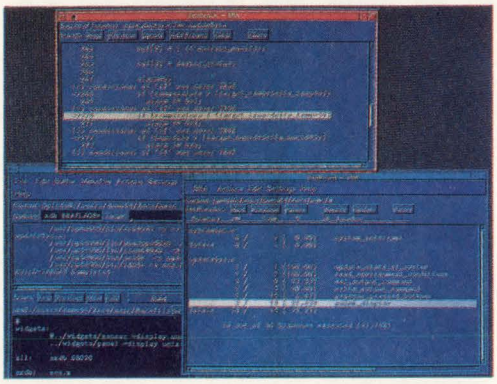

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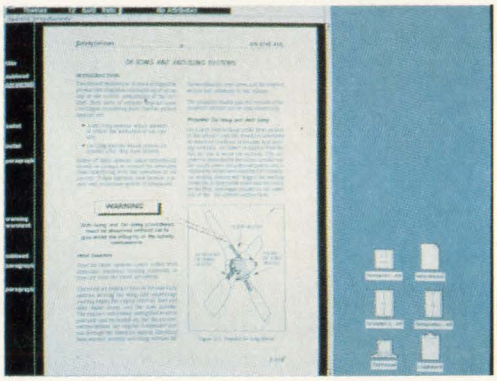

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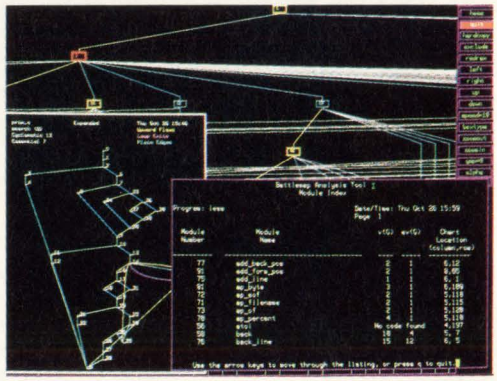

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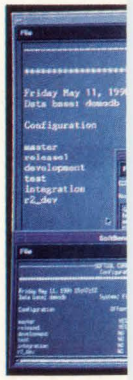

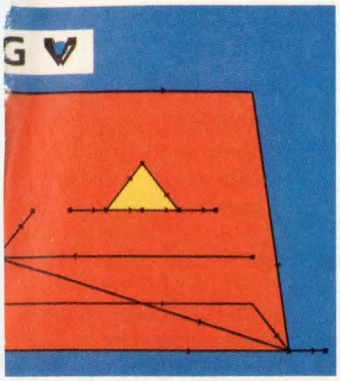

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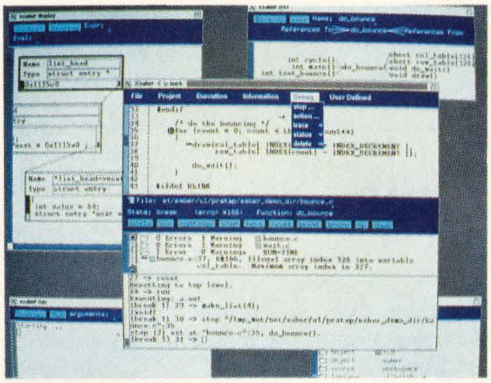

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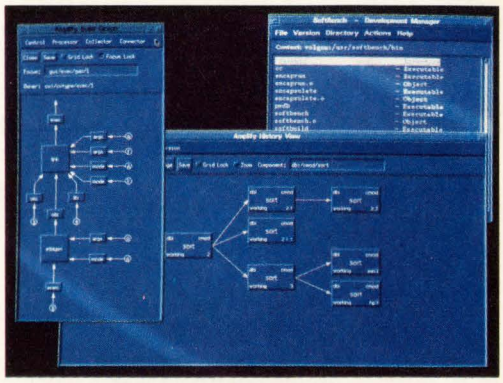

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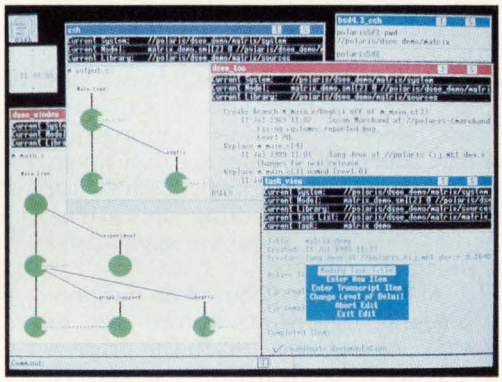

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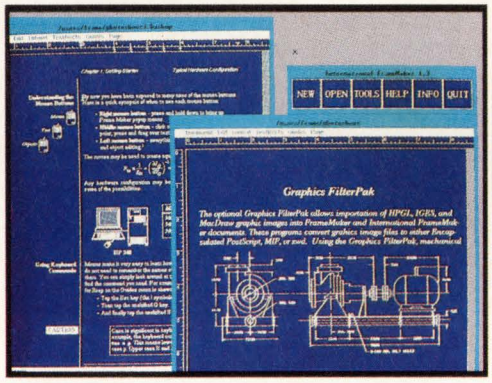

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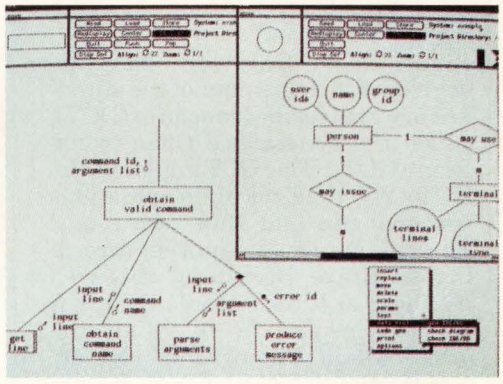

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CIRCLE NO. 40

SOFTWARE AND DEVELOPMENT TOOLS

New algorithms fuel the push for multimedia

Tom Williams, Senior Editor

With the rush toward multimedia, there's a flurry of activity in the semiconductor arena to produce fast, cost-effective chips to compress, decompress, store, and transmit sound and video. In addition to specialized video processors, digital signal processing chips promise to improve the performance of multimedia. There's also a push to improve the software methodology for video compression and decompression so that even general-purpose processors can tackle image-handling operations that formerly required specialized silicon.

Attention has focused on enhancing the algorithms at the core of these operations. But in the process of enhancing algorithms, companies must decide whether to adhere to standards or to deviate from them in favor of performance.

DCT refined

Ricoh (West Caldwell, NJ) has developed a refinement of the standard discrete cosine transform (DCT), called the generalized Chen transform (GCT). The GCT replaces the DCT's 256 multiplication operations with 64 add and shift operations. The only multiply required, according to Steve Blonstein, research manager at Ricoh's Menlo Park, CA research center, "is to satisfy the JPEG (Joint Photographic Expert Group) quantization step at the end of the transform."

Not only does the resulting algorithm comply with the JPEG standard and run faster than DCT on a general-purpose processor, it also makes custom silicon much simpler to build. Instead of hardware multipliers, the silicon can substitute a bunch of adders. "The algorithm carries over into silicon very well because it doesn't have multipliers," says Blonstein. "We're looking at a very tiny chip that will be able to do 30 frames/s of NTSC video at 30 MHz."

With the software alone running on a general-purpose processor, Blonstein says, "We can process a 512-×512-color image on a Macintosh fx in about 3.5 s."

That kind of performance, when translated to even faster processors, lends itself to applications such as image-filing systems or fax machines, where video frame rates aren't required. For systems that require video, custom hardware still will be required, but the improved algorithms are expected to bring down cost and complexity. Ricoh is actively interested in licensing its GCT technology to OEMs.

Less-complex technique

Using an algorithm that differs entirely from the JPEG-approved DCT, UVC (Irvine, CA) has developed compression/decompression technology that's about 50× less complex than DCT. UVC has built chips, is developing board-level products, and is licensing the software technology to third parties. One early licensee is Total Multimedia (Thousand Oaks, CA), which is forming alliances to address application areas in the multimedia market.

The UVC algorithm compresses a frame of video data by working on one scan line at a time. As each line is scanned, it is sampled. The analog signal is digitized according to the UVC algorithm. That digitized scan line is then compressed using run-length data-compression techniques. Both digitization and compression are done on the fly because storing the image in a frame grabber before performing the compression wouldn't sustain the frame rate that's needed for full motion video.

Using UVC's algorithms, Total Multimedia (TTM) has built a software package called SoftVideo that can play back compressed images at 30 frames/s at VGA (640×480) resolution on an 80286-based, PC/AT-class computer. According to the company's vice-president of technology, Taylor Kramer, hardware assist still is needed to compress and record video at frame rates. "We can do it in no-real-time with software only, but that's not where we're currently going," he says. The current SoftVideo product is aimed at decompression and playback of stored and distributed video material.

While using the UVC approach for compression and decompression, TTM has decided to opt for performance over compliance with a standard. "Very rarely have standards been implemented in advance of products," says Kramer.

Emphasis on performance

Meanwhile, other companies are pushing performance along with

New algorithms improve on an old standard

The standard method for color image compression and decompression, known as discrete cosine transform (DCT), has been around for over 20 years and is the method adapted by the Joint Photographic Expert Group (JPEG). The complex algorithms involved in DCT are the reason that so much research has gone into silicon to make image compression faster. At present software efforts are being aimed at either refining DCT or exploring alternate methods.

DCT is a frame-based compression method that breaks an image into blocks of 64 pixels (8×8). Since the probability is high that adjacent pixels will be fairly close in color and intensity, the transitions from pixel to pixel and from block to block can be represented as waves on a two-dimensional surface. DCT transforms the pixel values to this wave representation via a series of complex multiplication operations. The original algorithm involved 256 multiplication operations on an 8×8 block; recent refinements have brought that number all the way down to 150.

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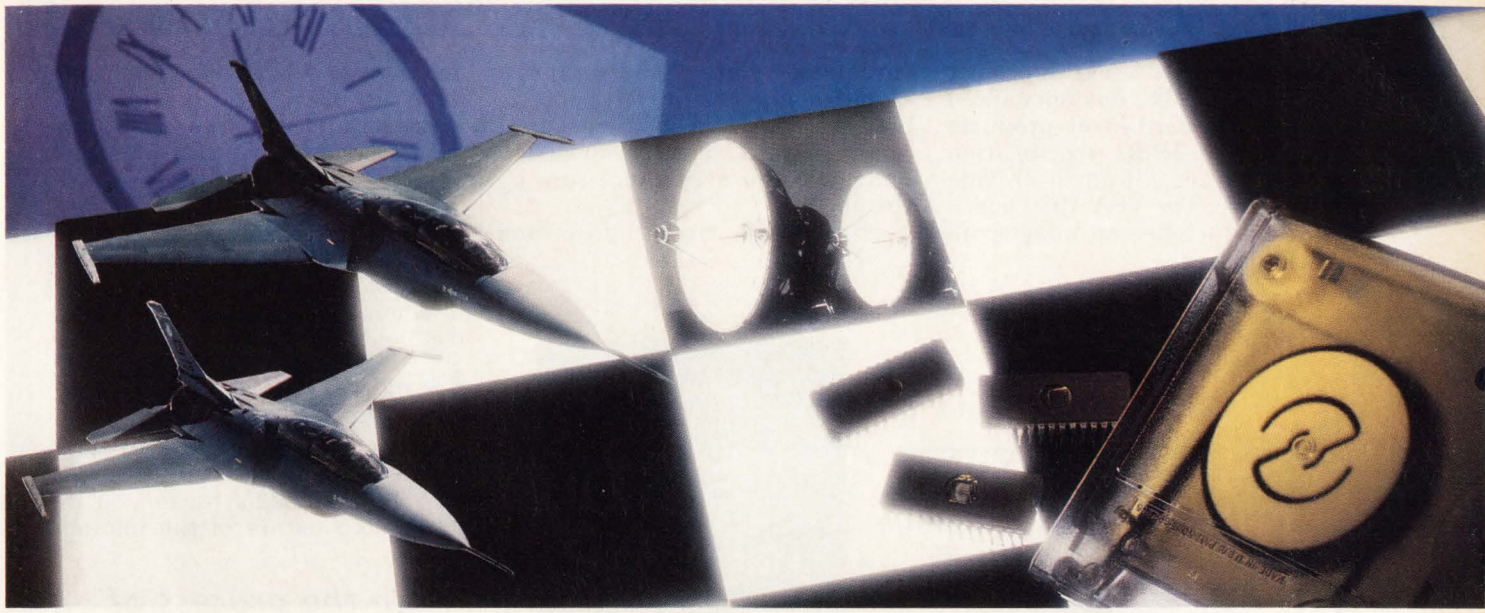

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JPEG compliance. Fluent Machines (Framingham, MA) has announced a family of board-level products based on the JPEG specification that depend on silicon to provide performance. The VSA-1000 board set, which includes an image-capture frame buffer and compression/decompression features, is based on an Intel i960 embedded processor that controls two CL550 image-compression processors by C-Cubed.

The system can compress and decompress NTSC video and audio data at 320×240 pixels at 30 frames/s and can time-stamp the data to maintain synchronization of video and audio. The VSA-1000 family is targeted at network applications and will soon incorporate the ability to monitor the available network bandwidth and to adapt video rates to the available bandwidth.

Standards on the horizon?

Price and performance will dictate acceptance and, ultimately, standards. But standards will be important in multimedia because of the distributed nature of the information—via CD-ROM, networks, phone lines, and so forth. Just because a professional association has adopted a standard doesn't mean that the standard will prevail in the market.

Multimedia will be a mass market, and there will be many more innovative approaches before the dust settles and anything that resembles standards emerges. ■

In the process of enhancing algorithms, companies must decide whether to adhere to standards or to deviate from them in favor of performance.

■ ■ ■

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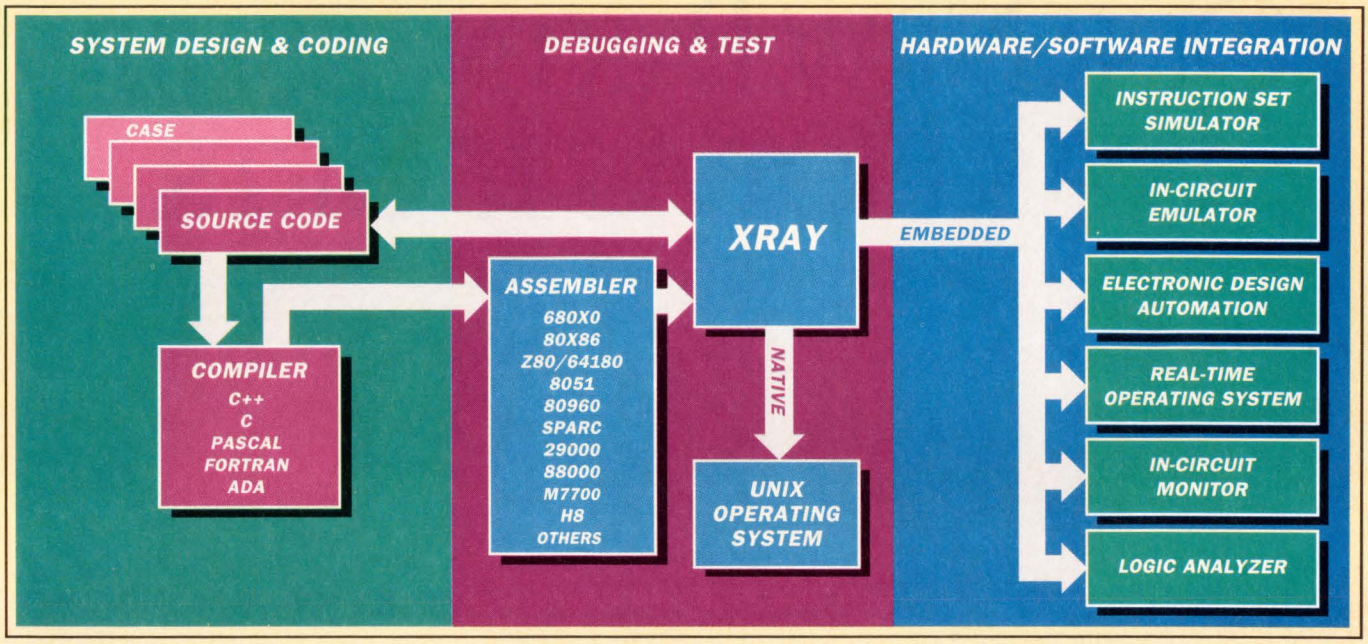

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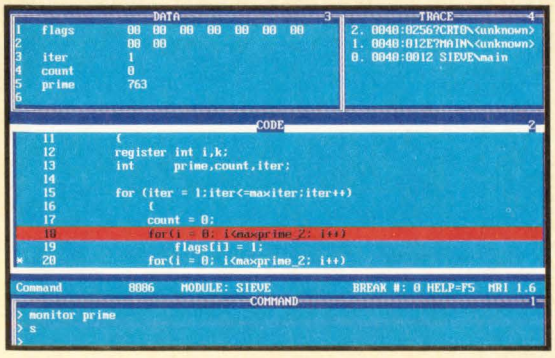

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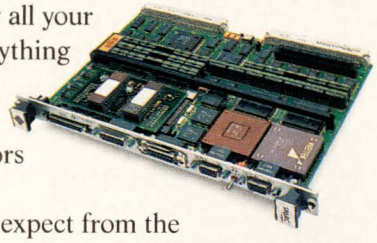

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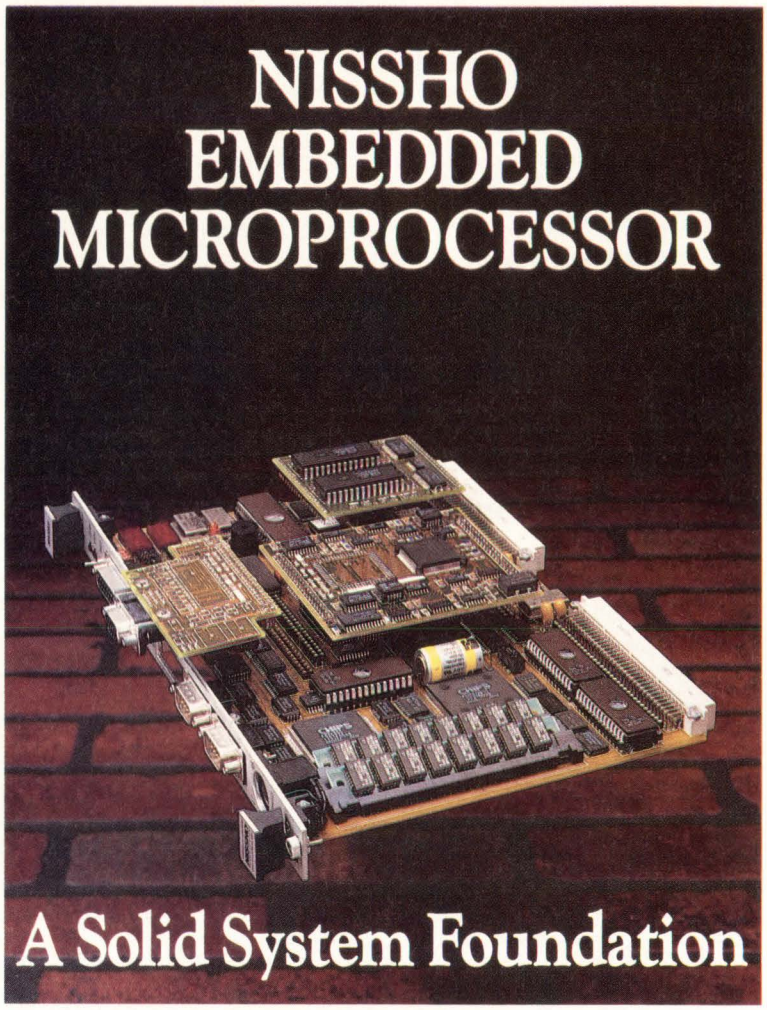

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CIRCLE NO. 45

Accurate device models make PCB simulation a reality

A reliable circuit board simulation can save weeks of prototype debugging time. But procuring the necessary models to perform such a simulation has been a problem that today's accurate device models are only now beginning to overcome.

Mike Donlin
Senior Editor

Logic Modeling's family of hardware modelers let users on an Ethernet network access multiple devices simultaneously. "Memory in the system is dynamically allocated," says Pete Jaeger (standing), model development manager. "This lets multiple users sample a device's behavior and return to their simulation environment while others access the device."

Accurate device models are the fuel that drives printed circuit board simulators. And simulation is quickly becoming a necessity as component densities, surface-mount devices and multilayer designs make traditional prototype debugging techniques obsolete.

For simulation techniques to gain wider acceptance, the prejudices against device models must be overcome. Traditionally, device models have either been expensive to create with hardware modelers or difficult to write in software. These limitations have been reflected in three areas—accuracy, availability and cost.

Accuracy has been a problem for device modeling not because it's unattainable, but because a full-blown structural model of a device might slow a simulator to a crawl. The accuracy of the model is further inhibited by the accuracy of the simulator—a model can only be as accurate as the simulator on which it runs. Many simulators, for example, aren't designed to handle the timing requirements of the latest generation of submicron ICs. Less-detailed bus-functional models are accurate as far as they go and won't slow down a simulator, but they represent only bus functions. Although such models are useful for design verification at the front end of a project, they lack the detail needed for complete simulation.

Despite the best efforts of CAE vendors, the availability of accurate models is still one of the biggest concerns of printed circuit board designers, mainly because the hundreds of new devices unveiled every year make it difficult for modelers to keep up. Silicon vendors are best suited to provide accurate models, but they're faced with a dilemma. To get design wins, they must provide models before their silicon is actually ready. They're reluctant, however, to reveal detailed proprietary model information that might get into the hands of competitors. Third-party model vendors, such as Logic

Automation (Beaverton, OR), have attacked this availability dilemma by entering into agreements with silicon vendors to protect their proprietary design information.

A new service called Model Bank from Protocol (Mt. Olive, NJ), a division of Zycad, promises to address silicon vendors' security needs. Model Bank lets users access foundry-supplied models of complex parts without compromising proprietary design information. The service, provided either on-site or through a dial-in connection, lets users perform system simulations that include the foundry model but prevents access to the proprietary model design information. Protocol has thus far entered into agreements with MIPS Computer Systems, LSI Logic and Integrated Device Technology for the service.

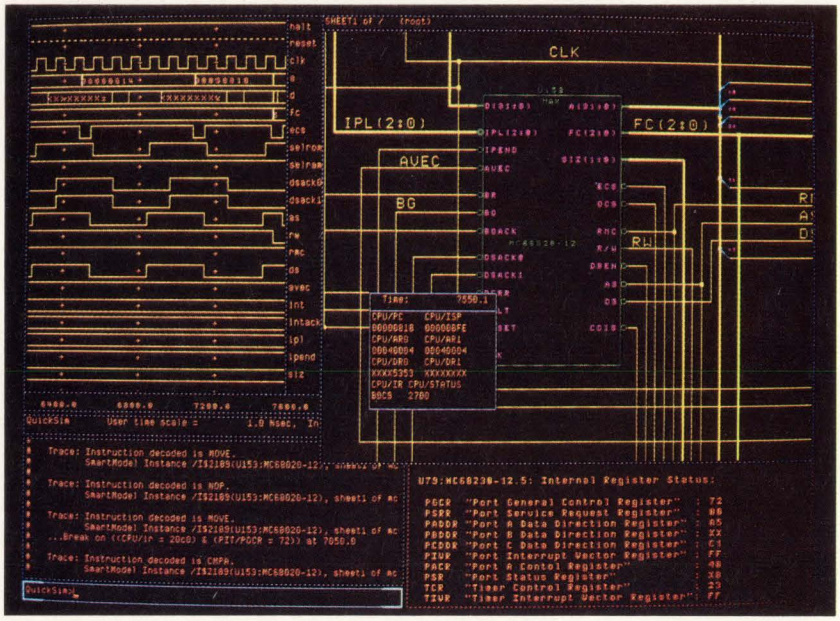
Cost concerns

Device model cost is another concern of many board designers, although some companies claim the contrary. Logic Modeling Systems (Milpitas, CA), for one, says that saving even a single prototype revision can pay the cost of its hardware-modeling system. Still, many companies are reluctant to spend $50,000 or more for model platforms and services.

"Device modeling hasn't been accepted as well as we'd like," admits Doug Lundin, board and test business unit manager of the simulation and test division at Mentor Graphics (Wilsonville, OR). "Traditional breadboarding methods seem cheaper than paying for models and simulation capabilities, but they really aren't.

"To build a breadboard, a designer spends money for the components a little at a time," he continues. "The cost of the time it takes to build and debug the board is also spread over time. Compare these gradual costs to an up-front capital expense for a hardware modeler or subscription to a software-modeling service, and they look small. But in the long run all these methods cost about the same."

Device models and simulation software also suffer from an image problem, namely that the products they're simulating don't physically exist. While breadboards and prototypes are real circuit boards with jumper wires that signify debugging in progress, simulations are merely waveforms on a workstation screen, and device models are the invisible components that run them. A breadboard signifies progress being made on a product, while model development and simulation are done without a circuit board in sight. Both hardware and software model developers are working hard to clear up these misconceptions by touting the time-to-market and cost advantages of debugging a design before committing to a prototype.



During simulation, most models appear as "black boxes": they give a behavioral description of a device's activity but won't let users observe the internal workings of critical components. Logic Automation's SmartModel Windows provide designers with more information than they would get from conventional waveform displays, including internal register status (lower left) and timing register contents (center).

Hardware vs. software models

Although competition exists between hardware and software modelers, there's a need for a full palette of models in most simulation environments. "We've found that many of our customers rely on all kinds of models for their simulation," says Robbie Wisdom, hardware modeling marketing product manager in the simulation and test division at Mentor. "A typical project might involve some software models that the designers wrote themselves, some that they purchased, some hardware models that they purchased, and some that they developed on an in-house hardware modeler. The key is having a model for every component on the board, or the simulation won't be complete."

The strengths and weaknesses of hardware and software modelers continue to be cause for debate. As a general rule, hardware modelers are completely accurate, because they employ an actual device. Their relatively high price tag, however, restricts their use to microprocessors and ASICs—devices that would be unwieldy to model in software.

Again, some vendors disagree that price is an issue. "You've got to remember that a hardware modeler is a shared resource," says Pete Jaeger, model development manager at Logic Modeling. "All simulators on the Ethernet can use the modeler simultaneously. If there are several devices installed in the modeler, any device can be accessed for simulation. The cost, when spread out over many users, isn't much of a hindrance."

Some advocates of software modelers point out that because a hardware modeler has to be accessed by the simulator as a device on the Ethernet, there's a speed penalty. This claim has also been disputed. "The microprocessor in the modeler is working at real-time speed, which means that it's six or seven orders of magnitude faster than the simulator that's running. Most of the time the microprocessor is waiting for the next execution instruction," says Jaeger.

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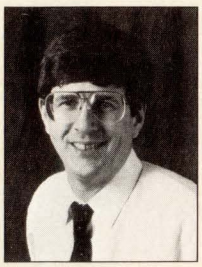
Digital logic's analog side: When digital is really analog



Digital systems historically have been designed "from the data sheet." Only when the systems fail does simulation become economically justifiable. And circuit simulation of digital systems only becomes necessary when the analog characteristics of the digital signals become electrically important. In instances where a digital circuit is simply a faster version of an old design, from a 33-MHz 386 to a 50-MHz version, for example, extensive logic simulations may not seem necessary. The integrity of the digital quality of the signals, however, may require careful circuit analysis.

The source of this signal-integrity problem is the digital-output driver. A high-speed digital-output driver can drive only a few inches of wiring before the noise and delay due to the wiring become a problem. To speed up the circuit simulation and modeling, analog behavioral models can be created that mimic the full analog characteristics in a fraction of the time.

Roadblocks to successful digital

The roadblocks to effective high-speed digital designs are noise and delay. The fundamental digital noises are: line-termination noise, ground-bounce noise and coupled-line noise.

Line-termination noise is the additional voltage that's reflected from the load back to the driver because of impedance mismatch. Digital-output buffers aren't designed to have accurately controlled output impedance, and most buffers have different rising and falling edge impedance.

The ground-bounce noise is generated where leadframes or other circuit wires can't be formed into transmission lines. The resulting inductance creates an induced voltage in the ground circuit, the supply circuit and the output driver circuit. The ground-bounce noise lowers the noise margins for the rest of the system.

Coupled-line noise is the noise induced from lines that are physically adjacent. This noise is generally most severe for data lines that are next to clock lines.

Circuit delays become critical as timing requirements become tighter. The key circuit delays are: gate delays, line-turnaround delays for tristate buffers and line-length delays (clock skew).

Logic analysis addresses only gate delays. The variation in the gate delay can be computed from circuit simulation only if the best- and worst-case manufacturing conditions are understood.

The line-turnaround delays add to the gate delays because an extra margin must be added so that multiple tristate buffer drivers don't simultaneously turn on.

The line-length delays have the greatest direct effect on the clock skew in most systems. As system cycle times approach the speed of electromagnetic signal propagation for the printed circuit board, consideration of line length becomes critical. The system noise and line delays interact with the electrical characteristics of the gates and may require circuit-level simulation.

Digital problems

Although exceeding the noise quota may not cause a system to fail, when a digital input is being accepted maximum noise can become a problem. If an engineer can decouple the system, much-higher noise can be tolerated.

Common decoupling methods are: including multiple ground and power planes on the printed circuit board, multichip module or pin grid array (PGA) level; separating signal traces with ground traces; decoupling capacitors; adding series resistors on output buffer drivers; and using twisted-pair transmission lines.

Selecting the best packaging methods at the printed circuit board,

Shawn Hailey, BS, president, Meta-Software

Real-world behavior modeling is valuable in other instances, such as fault simulation. "Of course, the primary purpose of hardware modeling is getting the device's behavior right," says Russ Hall, vice-president of marketing at Logic Modeling. "But a secondary gain is that you're thoroughly imitating a device's behavior under less-than-ideal circumstances. A person who designs a device might not thoroughly investigate what happens to it when a pin gets stuck high or low. Certainly the person who writes software models can't cover all those contingencies. So what you get is an ideal model which might behave inaccurately when an unusual event is presented in simulation. With hardware models, you can see what a device will do if you present it with unusual stimuli."

Software models, on the other hand, are especially valuable for SSI and MSI devices. Advocates of software models also point out that a hardware modeler needs actual silicon to operate—a drawback if a designer wants to use a part that isn't yet available for a next-generation printed circuit board. And although some might question the accuracy of a software model based on the specifications of a device still under development, the fact remains that having even a rudimentary model is better than waiting for first silicon.

"Of course, a full-functional model is going to give you all the functions that a device possesses," says David Hardman, product planning manager at Logic Automation. "But even though a microprocessor might have 300 instructions that it will eventually carry out under real-world conditions, most of what it does is at the bus level. This translates to about 20 types of bus-cycle instructions, such as read memory, write memory, input, and output. That's certainly enough to make sure a design is going to work.

"We try to work with silicon vendors to provide as much detailed behavior as we can, without sacrificing their proprietary information," he continues. "Remember, the right amount of information might secure a design win, so silicon vendors are realizing that they have to release as much information as possible as early as possible."

Although the accuracy of software models seems secure in the SSI and MSI domain, vendors continue to improve these relatively simple models. With the release of its Sys-

multichip module or PGA levels is perhaps the biggest headache in systems design. Extra ground and power planes are often necessary to lower the supply inductance and to provide decoupling. Decoupling capacitors must have low internal inductance to be effective for high-speed designs. Newer designs frequently use series resistance in the output drivers to lower the circuit ringing. Finally, in critical high-speed driver applications, twisted-differential-pair transmission lines are used.

Engineers must determine logic partitioning. The propagation speed of signals on a printed circuit board is about 6 in./ns. As digital designs become faster, the wiring interconnect becomes a factor in deciding how to partition the logic. The critical wiring systems are: IC-level wiring, package wiring, printed circuit board wiring, backplane and connector wiring, and long lines.

IC-level wiring is a problem for systems designers who must use ASICs or custom ICs as part of their logic-partitioning strategy. The more-familiar decisions involve selecting packages and arranging packages on a printed circuit board. Large systems generally have a central backplane that becomes the primary challenge at the system-partition level.

The following relationship gives an estimate of the wire length when transmission line effects become noticeable.

Length = risetime×velocity/8

A 1-ns risetime with a board velocity of 6 in./ns gives a 3/4-in. wire length before the first noticeable distortion. The models for each kind of wire can be automatically generated in the HSpice circuit simulator to give full-loss transmission line effects.

ECL design engineers have always partitioned systems by calculating the noise quota for each line. If most high-speed digital logic must be designed with respect to the noise quota, how much noise and delay can be accepted before the timing and logic levels fail?

The answer to the noise quota problem requires the calculation of the noise associated with the wiring. Large ICs can be separated into two parts, the internal logic and the external input and output amplifiers.

With mixed-digital and -analog products such as Meta-Software's HSpice and Viewlogic's Viewsim A/D, a complete system can be merged together with full analog-quality timing constraints and full digital representation. Noise quota calculation can be simultaneously evaluated subject to system timing.

tem Hilo 4 tool suite, GenRad (Concord, MA) plans to include software models of SSI and MSI parts based on hardware-modeling techniques. "Even in SSI and MSI devices you can get into trouble by having different qualities of models based on the different qualities of your model writers," says Ivan Ward, device library manager at GenRad's facility in Maidenhead, England. "So we're using a hardware modeler and applying complex waveforms to the device, then using our software tools to translate the response into accurate software models. We think that this is a much better solution than simply writing models from data books."

Analog issues

The struggle to adequately model the ever-evolving devices in the digital world is mirrored in the analog-modeling domain. Keeping a close handle on accuracy/speed tradeoffs is especially important in the analog world, where a detailed, transistor-level description of a device can choke a simulator. Although engineers at the front end of the design cycle have the same choices of behavioral models that digital engineers have to verify their designs, more-detailed models are mandatory when more-accurate simulation is necessary. Spice macromodels have been the answer to this need for accuracy, but some vendors are looking for ways to improve the traditional Boyle-Solomon models.

"One of the main limitations of the Boyle-Solomon models was the number of frequency poles—only two poles with no zeros," says James Wong, applications engineering manager at Analog Devices' Precision Monolithics division (Santa Clara, CA). "That's fine for a low-frequency op amp, but it compromises both ac and transient-response simulation accuracy. We've chosen a different technique that lets us use as many poles and zeros as we need to accurately shape a model's frequency response to conform to the actual device. For 26 of the 176 devices we've modeled, we include voltage and current noise, which lets designers predict system noise performance as part of the Spice simulation."

Accurate simulation requires more than just models of standard devices. Other components, such as fuses, need to be modeled to get a complete picture of a printed circuit board's behavior. Intusoft (San Pedro, CA) has what it believes to be the first accurate Spice-based fuse model available. Although a fuse seems like a simple element to simulate, accurate modeling of its behavior can become complicated because fuse characteristics vary depending on filament material, ambient temperature and line current. "It's also not possible to simply create a generic model for all fuses," says Charles Hymowitz, vice-president at Intusoft. "We can make a model for a fuse family and put in rated current. But changing from a fast-blow to a slow-blow fuse, for instance, means writing a different model."

AHDLs to the rescue?

To get around the difficulties of writing intricate Spice models, some vendors are touting the advantages of hardware description languages in describing component behavior. "Spice models have limitations that HDLs can overcome," says Ian Getreu, vice president of modeling at Analogy (Beaverton, OR). "A component model consists of two parts. One is the generic model, and one is a set of parameters. A simple example would be V = RI as a generic model for a resistor. R = 10K would be the parameter model specific to that component.

"In Spice, the set of generic parameters or equations is relatively limited, and it's very hard to write new ones. One of the things that our analog HDL (AHDL), called Mast, lets users do is write new generic models."

Although Mast is probably the

A close look at charge conservation in circuit simulation

Accurate simulation of many MOS circuits, such as DRAMs, switched-capacitor filters, phased-locked loops, charge pumps, and other MOS VLSI analog and digital circuits, requires that the device models conserve charge. When Spice was first developed in the early 1970s, there was no need to accurately simulate circuits with the extremely high impedances typical of modern MOS designs. Indeed, the prevalent technology of the time was bipolar transistors, which don't have extremely high impedance nodes.

Today's circuits, however, are likely to switch around small packets of charge, relying on the MOS devices' zero-gate current and the gigaOhm OFF impedances of MOS switches to trap the charge for long periods of time. This is a severe test for Spice-derived circuit simulators.

Unfortunately, although Spice has become the industry-standard circuit simulator, many of the Spice MOS models aren't charge-conserving. More specifically, any model that uses voltage and capacitance as its state variables won't be charge-conserving. The problem is that capacitance-based models tend to lose charge, and this loss of charge leads to inaccurate simulation results.

Why charge isn't conserved

Why don't capacitance-based models conserve charge? In Spice, the dynamic nature of the MOS devices is modeled with equations that give capacitance as a function of terminal voltages. The capacitances are nonlinear. For a given voltage step, the next value of charge is estimated by the voltage step times, the present value of capacitance, plus the present charge. Since a nonlinear CV characteristic implies a nonlinear QV characteristic, doing a first-order extrapolation of the charge is mathematically equivalent to doing a Taylor series expansion of the QV curve about the present voltage point, and then discarding all terms above the first order.

Consider the following simple example of a linear 1-μF capacitor connected across a voltage source. If we assume that the voltage across the source changes from 0 to 1 mV in one time step and then back to zero on the next, and that both time steps are 1 ns, then the waveform below is generated.

Computing current on the first step results in:

$$i = C\,dV/dt = 1A,$$

and the charge is:

$$Q = CV = 1nCoul.$$

On the second step, the charge flow is equal and opposite, with a net zero charge being supplied by the source after the second step. If the capacitor is nonlinear and described with an equation that gives capacitance as a function of voltage, neither the current nor the charge can be computed exactly.

Each can be approximated as follows:

$$i(t1) = C(V(t0))\,[V(t1) - V(t0)] / [t1 - t0]$$
$$q(t1) = Q(t0) + C(V(t0))\,[V(t1) - V(t0)]$$

Thus if:

$$C(0) = 1\mu F \text{ and } C(0.001) = 1.1\mu F,$$

then:

$$i(t1) = 1A$$
$$q(t1) = 1nCoul$$
$$i(t2) = -1.1A$$
$$q(t2) = -1.1nCoul$$

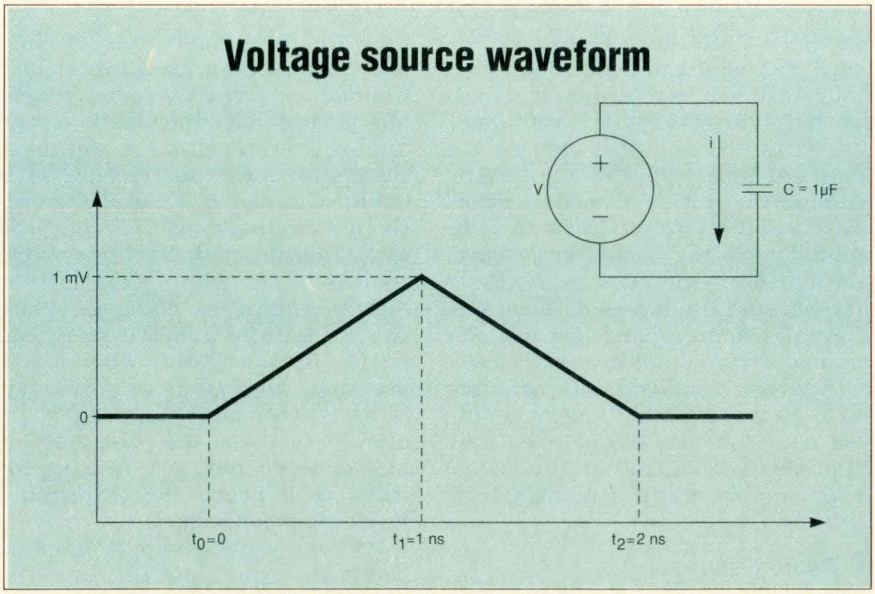
Thus, the net charge is –0.1nCoul, and charge has not been conserved. A charge-based model, on the other hand, creates no error. Assume the capacitor is modeled with the equation:

$$q(V) = CV + DVs(2),$$
where $C = 1\mu F$ and $D = 50\mu F/V$.

This equation was chosen because it satisfies $C(0) = 1\mu F$ and $C(0.001) = 1.1\mu F$. Now the current still has to be approximated, but the approximation is such that charge is always conserved:

$$i(t1) = [q(V(t1)) - q(V(t0))] / [t1 - t0]$$
$$i(t1) = 1.05A$$
$$q(t1) = 1.05nCoul$$
$$i(t2) = -1.05A$$
$$q(t2) = -1.05nCoul$$

The net charge is zero. Because charge is computed explicitly, if a charge-based capacitor model is evaluated for the charge at a particular voltage and then the voltage on the capacitor goes through some wild excursion but returns to its original value, then the charge must also return to its original value; it's computed with an algebraic expression that hasn't changed using the same input. With a capacitance-based model, the small errors made on each step of the voltage trajectory accumulate, and the final charge doesn't equal the starting charge.



Grant Erwin, BSEE, MSEE, senior application engineer, Cadence Design Systems

best established AHDL around, some EDA vendors are reluctant to embrace any AHDL until some standards are set. Other vendors, such as Valid Logic Systems (San Jose, CA), believe that a high-level description of analog circuits is necessary but take issue with critics of Spice. "Spice is still a very powerful tool," says Eric Filseth, product marketing manager for analog CAE at Valid. "Sometimes you have to get creative and work a little harder, but people need accurate models. To say Spice can't provide those is hogwash."

Valid recently unveiled its answer to top-down analog design with Profile, a tool that lets analog designers describe blocks or entire circuits at the behavioral level by using a combination of graphics and text. The tool lets users create and simulate an architecture without having to resort to a language-based behavioral-modeling technique. "Getting accurate models for parts that aren't entirely electrical, such as motors and sensors, has always been a problem," says Filseth. "But the characteristics of such electromechanical devices have a definite impact on the circuit that drives them.

"So if you want a good circuit, you need good models of these devices," he adds. "We don't think, however, that a purely language-based approach is going to work until an AHDL standard is defined."

Digital solution

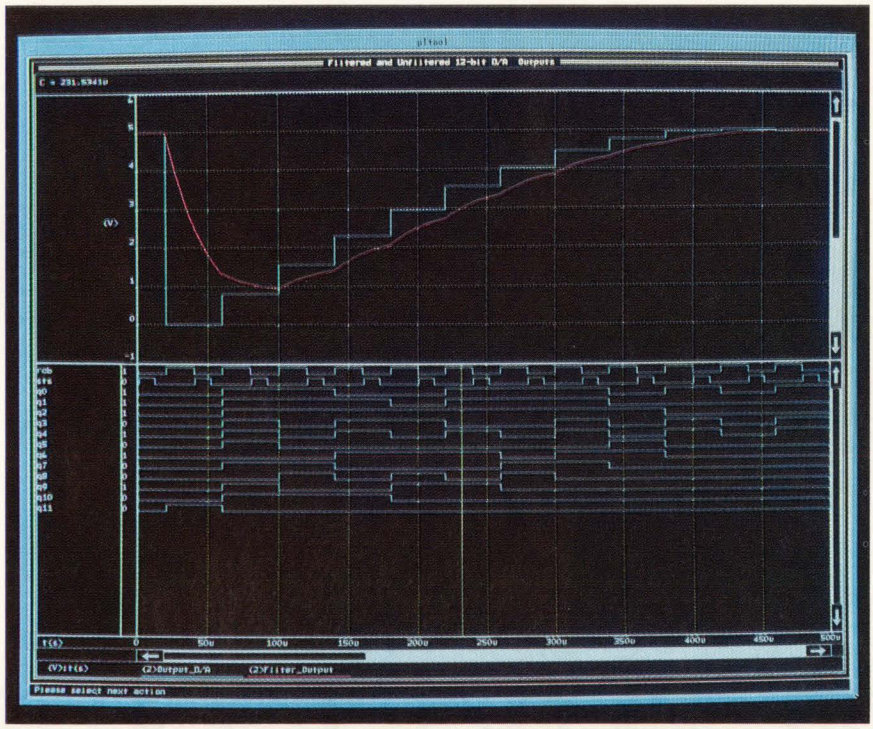
On the digital side of the spectrum, Verilog from Cadence Design Systems (San Jose, CA) has built itself an established position as an HDL modeling and simulation language. For simulation of complex devices, Verilog favors the behavioral approach, although a structural model is more efficient for less-complex devices. "We prefer to call our models structural rather than gate-level," says Matthew Kopser, product manager of board-level simulation at Cadence. "A gate-level model implies that it's a representation of the actual components in the device. We say structural to mean a primitive set of parameters as opposed to a behavioral set.

"In lower-gate-count devices, our structural models on average perform better than our behavioral," he continues. "After around 300 gates, the behavioral approach starts to pull ahead. That's contrary to other simulators, which always run faster at the behavioral level."

Although Verilog has an established base, VHDL will certainly be a powerful force for device modeling in the coming years. Among the obstacles in VHDL's path is the lack of programming expertise among many of today's designers. But some companies, such as Lewis Systems (Irving, TX), are providing tools that bridge the gap between a designer's concept and VHDL code. Lewis Systems' product, HUM, lets designers enter modeling information via a spreadsheet-like table. The program uses this information to generate VHDL code for simulation.

Tools such as these are expected to ease the migration path to VHDL. Time will tell whether they will last, as more and more software-literate engineers graduate from college and join the work force.

No matter which modeling technique is used, one fact won't change: As models become more accurate, accessible and cost-effective, the simulators they drive will draw closer to the real-world products they emulate. And if modeling techniques can keep up with the advances in silicon and printed circuit board technology, the day may come when the jumper-laden prototype becomes a thing of the past. ■



Accurate models of mixed-signal devices must emulate the digital and analog portions of a circuit's behavior. In this example, selected signals from a 12-bit AD574 analog-digital converter are displayed in Analogy's Saber simulator. The lower portion of the screen shows the digital timing diagram signals from the device, while the upper plots show the analog-output timing signals on the same timing axis as the digital signals.

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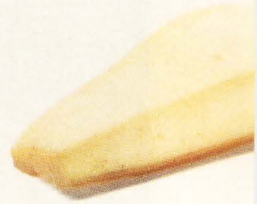

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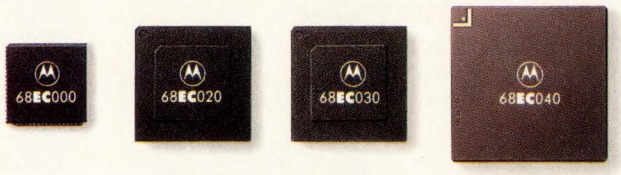

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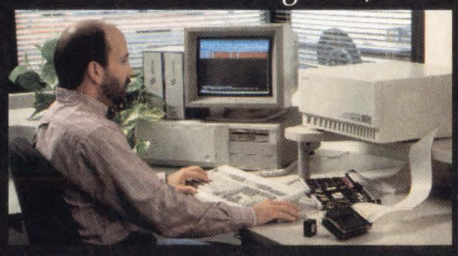

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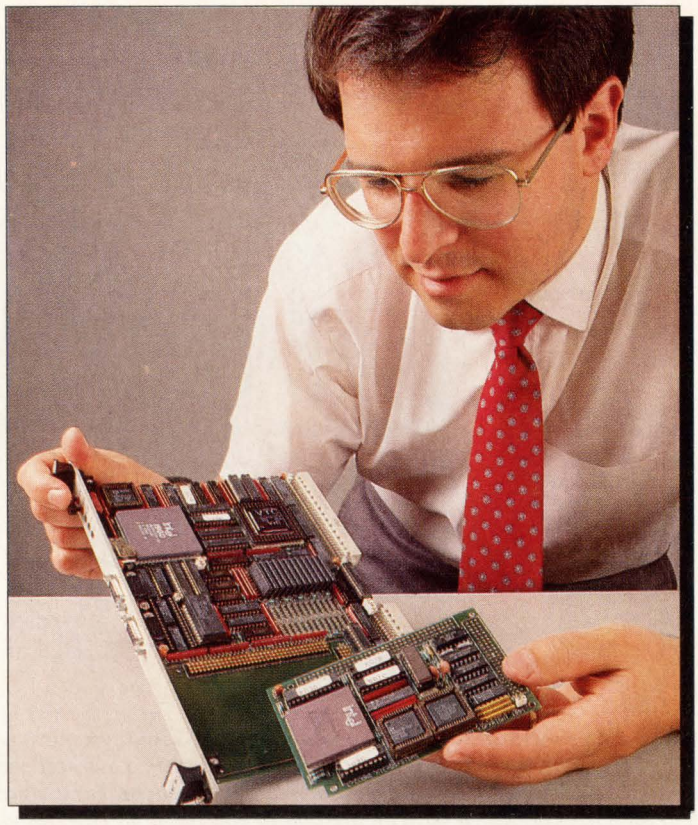
Mezzanine buses struggle with standards

Despite advances in the flexibility and performance of mezzanine buses, they've yet to win widespread adoption. Even with the success of SBus, emerging standards for this class of buses will find it difficult to gain momentum.

Warren Andrews
Senior Editor



While many mezzanine interface specifications have been released as open standards, they are usually designed for best performance with a specific processor. Cyclone Microsystems' Squall module interface is a public domain specification optimized for Intel's 80960CA. Only a few mezzanine buses have been accepted as industry standards by systems designers.

Mezzanine boards have a long history in the evolution of electronic circuitry. Traditionally in and out of favor for a variety of reasons—mostly related to reliability—these boards have come on with a vengeance over the past year or so, particularly on standard bus boards such as VME and Multibus.

Even companies such as Motorola, which not too long ago shunned mezzanine cards because they couldn't meet strict six-sigma quality/reliability standards, have reversed their position. (Motorola now uses a mezzanine card on its MVME147 and 167 CPU cards to mount the maximum complement of memory. Further, the company recently endorsed SBus as its choice for a Futurebus+ mezzanine bus.) In addition, the ultimate fussbudget on reliability issues, the U.S. military, is about to accept VME-bus cards with daughterboards attached.

While few would question that there has been a major turnaround in the acceptance of mezzanine buses, little effort has been focused at standardizing these buses outside of the Multibus area. And Multibus has concentrated on only a few such approaches, primarily iSBX, iLBX and MIX. In the VME camp, there are at least 25 different mezzanine buses, many of which are similar—but none of which are interchangeable.

"The proliferation of different mezzanine buses on VME is in some way related to the rich assortment of processor and memory architectures provided by VME," says Ed Schulman, vice-president of marketing at Ironics (Ithaca, NY). "In many cases, mezzanine buses represent nothing more than an extension of the processor address, data and control lines."

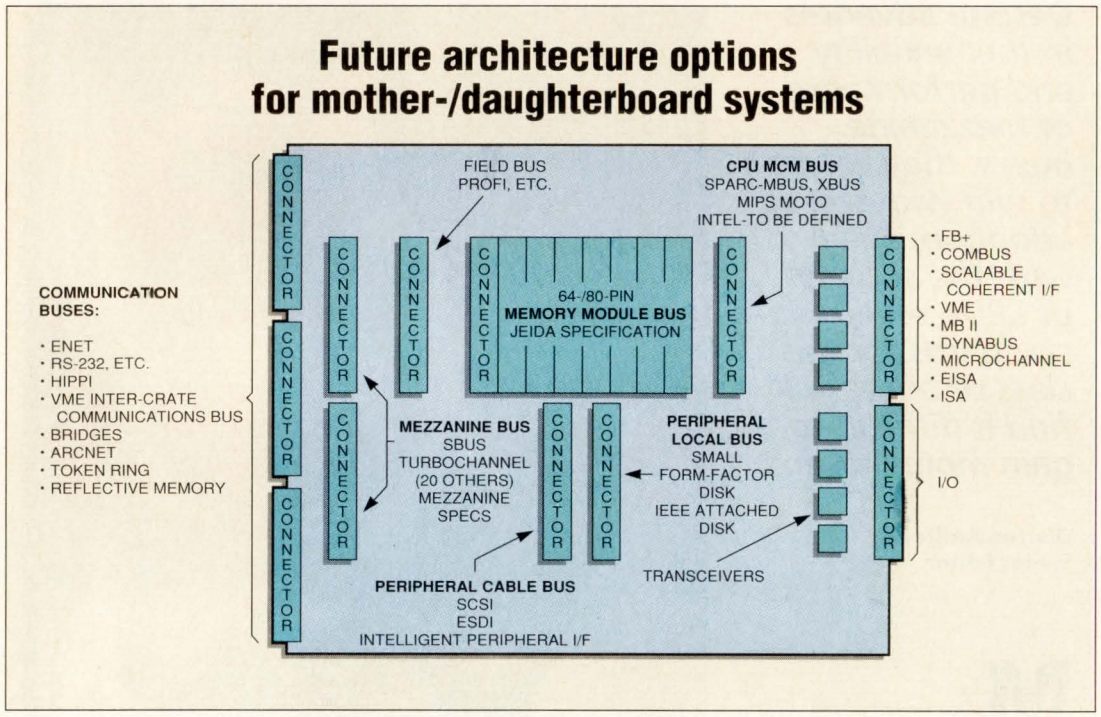
"What we see now may just be the crude beginnings of multiple-connector,

multiple-daughterboard strategies," adds Ray Alderman, technical director of the VFEA International Trade Association (Scottsdale, AZ). "Future boards are likely to incorporate a broad variety of functional expansion connectors, as well as sockets for processor subsystem multichip modules, memory multichip modules and communications modules.

"In fact," he continues, "future VMEbus boards—or even Future-bus+ boards for that matter—may include no more than basic bus interface circuitry and a number of connectors for subsystem interconnection." An example of this is illustrated in the figure above.

But this will be an evolutionary, not a revolutionary, changeover, Alderman emphasizes. "When I realized that it wasn't possible for the VITA membership to form any consensus on a single mezzanine bus for a VME standard, I decided it was important to publish the existing specifications for interested potential users," he says.

VITA requested information concerning mezzanine buses used on VMEbus modules from its membership and received full documentation from a dozen manufacturers. It assembled all the information into a mini-specification, which is available directly from VITA. Companies (and their buses) included in the specification are: Eltec Electronik Gmbh (LEB); Force Computers (FLXi-bus); General Microsystems (SAMbus); GreenSpring Computers (IndustryPack); Heurikon (COREbus); Ironics (IV3220, IV3272, IV9001); Matrix (Dbus-68); Omnibyte (OMNImodules); Performance Technologies (E PAK, I/O PAK); RadiSys Corp (EXMbus); Radstone Technologies (PEX, APEX); and Sun Microsystems (SBus).



The growing complexity and performance of board-based systems have driven designers to develop many off-board expansion solutions. Some see a future where a motherboard may hold only interface circuitry and connectors to off-board or mezzanine-based functions. For the present, however, designers are cramming as much as possible onto motherboards and turning to mezzanine boards for added functions.

Boards customized with ease

At present, the most common application of mezzanine buses is to let board vendors custom tailor boards to suit their customers' needs without completely redesigning them. "Let's face it, mezzanine buses are there for the benefit of the vendor, not the customer," commented one VME board vendor at a recent VITA technical meeting discussing the possible standardization of a single mezzanine bus. "They let board makers provide a variety of different products from a single base board—usually a CPU card. The only benefit to the customer is that they get exactly what they want without paying for functions not used." He added that the object of the mezzanine architecture wasn't to develop a mix-and-match strategy, but rather to be a fast and inexpensive way to customize a product.

Of the many different mezzanine buses, however, most offer basically the same I/O functions, along with some combination of serial ports, parallel ports, SCSI, Ethernet, or other basic I/O. Functionally, the majority of mezzanine buses are relatively simple, letting users implement their own application-specific functions as a daughterboard.

The major difference between most of the mezzanine approaches is that they're optimized for a particular processor. The PEX and APEX buses from Radstone Technology (Montvale, NJ), the FLEXibus from Force Computers (Campbell, CA), the SAMbus from General Micro Systems (Montclair, CA), and the DBus from Matrix (Raleigh, NC) are optimized for the Motorola 680X0 family of microprocessors.

Still other buses are aimed at other processor families. Cyclone Microsystems (New Haven, CT), for example, has developed its Squall module interface to take advantage of the 80960CA's capabilities as an I/O server and an embedded processor.

A special case of the mezzanine bus can be found on some digital signal processor cards where the DSP chip's data and control lines are extended so that additional DSP chips can be added for multiprocessor applications. Despite the fact that many cards use the same chip and basically extend the same processor pins, they usually aren't compatible.

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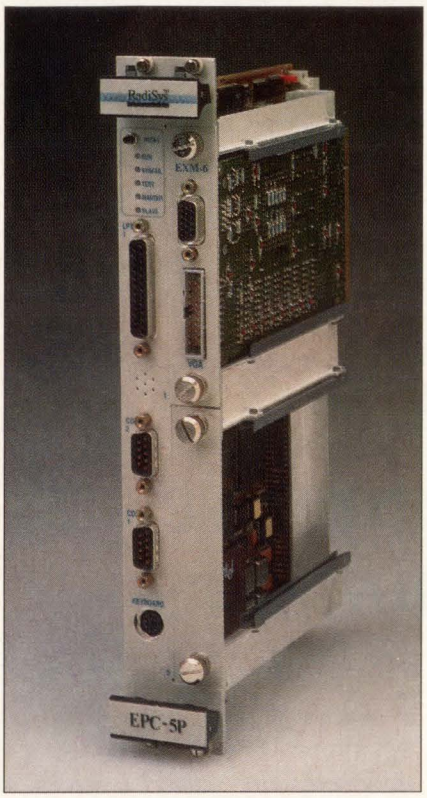


Even the PC's ISA bus has been added to the ranks of mezzanine buses. This EXMbus module from RadiSys implements the ISA interface in a form factor tailored for mezzanine service on VME boards. Others have built adapters to allow standard ISA boards to function in Multibus II systems.

While the aim of many mezzanine buses is to provide customers with a more flexible I/O offering, some mezzanine buses are geared strictly toward increasing performance. The COREbus from Heurikon (Madison, WI), for example, is designed to operate at blazing speeds—up to 200 Mbytes/s—for high-speed transfers required for high-resolution graphics, fast communications and coprocessor applications.

Other approaches, such as Ironics' IV series and multi-crate pipeline approach, are designed for fast communications between boards in a system, or between systems. They can provide communications over moderate distances (up to 10 m) at transfer rates approaching 60 Mbytes/s. Ironics is considering a move to fiberoptic media to increase transmission rates and allowable distances.

While some mezzanine buses offer either more-flexible I/O selection or faster communication rates than are available over conventional VME-bus, others, such as Radstone's APEX, provide both flexibility and performance enhancements. "VME-bus has a limited transfer rate, which, although it's adequate for most applications, quickly becomes a bottleneck if burdened with too much traffic," says Joel Silverman, marketing manager of commercial products.

"By keeping traffic on the system bus to a minimum, it's possible to keep a processor busy processing—not waiting for access to the VME-bus," he continues. "Using our APEX mezzanine bus along with other parts of our free-flow data architecture, it's possible to minimize the VME bottleneck.

"Radstone's APEX is designed to appear to the processor like a peripheral controller chip, with additional performance features such as read-modify-write," he adds. "In addition to the advantages afforded by the mezzanine bus, our free-flow architecture can take advantage of any number of other data avenues depending on the application." These include optional SCSI, Ethernet, or VME subsystem bus, in addition to the board's local bus and VME.

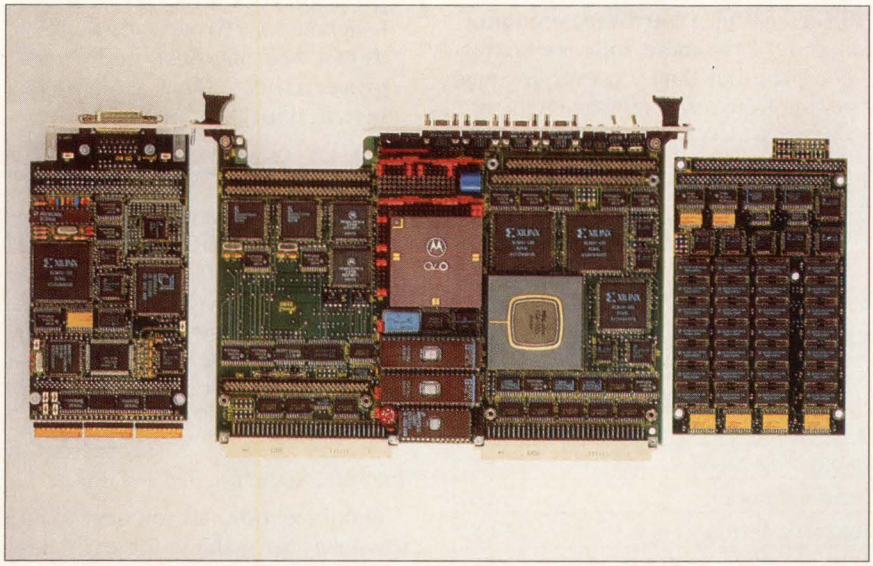
Military still a question mark

While mezzanine buses have been taking off in the commercial and industrial sectors, the military establishment has largely remained skeptical that such approaches could provide the reliability required in rough environments. As a result, the military has been relatively slow in accepting any standard-bus architecture. "We're just now on the verge of getting a mezzanine bus specification—bus, architecture and connector—approved for incorporation in a full MIL-STD board," says Doug Patterson, marketing manager of military products for Radstone. Although Patterson says the military has used motherboards with some mezzanine boards for memory expansion, these have been special cases.

Patterson wasn't about to reveal all the details of the new mezzanine bus but commented that it would look similar to Radstone's existing APEX bus. "Originally, we tried to implement the bus using a flex circuit. While it passed muster in terms of reliability, it turned out to be difficult to manufacture and too expensive," he says.

One of the main problems, Patterson adds, was to maintain the conformal coating on the flex circuit. "The latest version, which is now undergoing testing, uses a commercially available gas-tight connector that has already passed all the shake, rattle and roll tests, as well as other corrosive and harsh environment tests."

Implementing a mezzanine bus on a MIL-STD board, adds Patterson, involves far more than simply finding a suitable connector. "Other



Mezzanine boards can extend the motherboard's base function or add optional functions. The Force CPU-40 for VME systems uses mezzanine boards for both purposes. The CPU-40 is shown with two FLXi-bus boards, one for main memory extension and the other providing Ethernet, SCSI, floppy disk, and DMA interface functions.

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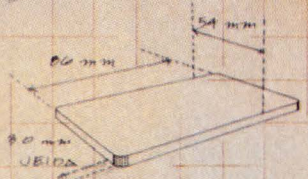

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SBus: technology meets the market

To a large extent, the full potential of a new technology is only realized when it's accessible to a potentially large market. The popularity of SBus has been built on the large market of Sun Microsystems' workstations and their clones. This market has attracted a sufficient mass of third-party support for SBus to ensure its rapid development and diversified base of supporting products. This base is now expanding to include industrial board markets such as VME and Futurebus+.

What mezzanine buses really bring to the party is an exceptional price/performance ratio. Essentially, the mezzanine buses of the '90s provide the same architectural interface, modularity and functionality as the backplane buses of the '80s, but at a dramatically lower cost. This is a logical consequence of the increased integration of electronics devices. It's also the result of the availability of that integration to the systems and board manufacturers, which has been made possible by ASIC technology. Quite literally, one could say that the new mezzanine buses are a consequence of the ASIC revolution; this is certainly true in the case of SBus.

The word mezzanine implies "another level" that's coplanar with a main level. The analogy with the architecture of buildings implies that the levels are horizontal, or one on top of another. That may not always be true, however, because SBus boards may be used either to provide I/O for desktop workstations or to modularize the I/O off the back edge of the vertically mounted standard backplane bus-board.

Optimum modularity

Mezzanine buses provide a more compact and cost-effective way to modularize a computer system, compared to backplane buses. Although obvious cost savings can be made by dispensing with the card cage and backplane, these are dwarfed by the less-obvious benefits of a well-designed mezzanine bus: low pin count, simple protocol interface and limited number of slots.

Mezzanine buses bring an exceptional price/performance ratio to the party.

SBus is an excellent example of an I/O interconnect that takes full advantage of the mezzanine environment to provide increased performance, lower cost and user-friendliness. Optimum modularity is provided through a postcard-sized interface board, which can accommodate full-height components on both sides. The single-chip interface possible with all SBus applications preserves the maximum possible mezzanine board area for use by board designers.

Another advantage of mezzanine buses is that they can be used in multiple size configurations. Since the board size is essentially constrained by the area of the main motherboard, rather than by the fixed positioning of card guides in a rack, it's possible to design a mezzanine card that uses an SBus interface but a larger-than-SBus card size.

The artificial limit on power dissipation for workstation expansion buses is dictated largely by user ergonomics. Designers may misunderstand the power limits because there are adequate power supplies in desktop workstations and the bus connector pins can carry significantly greater current than what they're restricted to by power limits. The power limit is dictated by the need for low acoustic noise in desktop workstations computers (i.e. no fans or low-speed fans) and the limited power capacity of laptop computers, which the SBus was designed to accommodate.

By constraining the electrical environment to four slots or less per physical segment, SBus considerably simplifies the assumptions that can be made regarding the electrical environment. While most backplane buses today are required to address the problems of crosstalk and signal-propagation delays, especially transmission line behavior, mezzanine buses such as SBus avoid these problems. That's because the two-way propagation delay across the limited physical distance of the motherboard and interconnect slots is much less than with a backplane bus.

SBus is an excellent example of how to optimally balance board area, cost, power dissipation, and performance. As an open standard, it provides an impetus to the rapid growth of the market for modular I/O for high-performance workstations. It also offers a valuable extension to the options for standard backplane bus-boards.

Paul Borrill, director of SBus engineering, Sun Microsystems

factors have to be considered, particularly mechanical considerations such as providing rigid mounting consistent with conduction cooling requirements," he says.

Acceptance slow in coming

Most of the mezzanine buses offered have been released to the public domain. But acceptance of most of these open standards by other manufacturers has been virtually nonexistent. For the few that are used outside their parent organization, the entire third-party user base consists of a customer or two building proprietary modules. However, at least two of the approaches stand out because they represent a popular standard architecture: PC bus and SBus.

One example of PC bus is EXMbus from RadiSys (Beaverton, OR). EXMbus takes advantage of the standard PC bus but implements it in RadiSys' own form factor so it can easily ride on VME as a mezzanine bus. The other mezzanine application of the PC bus is in Multibus II, where clever adapter boards allow the use of conventional half-sized PC boards in a Multibus II chassis.

The use of some kind of PC—with the attendant MS-/PC-DOS operating system and the availability of thousands of applications programs—on other bus platforms such as VME or Multibus has broad appeal. Formerly, the PC-based component of the system was used primarily for human interface functions, leaving the real-time control for some embedded kernel. However, in recent months,

RadiSys developed software that lets the PC-based function on a VME board handle both the interface and control functions in many industrial-automation and process-control applications.

SBus gains momentum

The other standard bus that has been rapidly emerging on the scene is SBus from Sun Microsystems (Mountain View, CA). Designed initially as an I/O workstation bus for use as a frame buffer in Sun workstations, SBus has experienced dramatic growth over the past several months. While still largely an I/O bus for Sun and compatible workstations, SBus is starting to emerge with a broad variety of other functions, including DSP, high-speed copper and fiberoptic communications and data acquisition. In addition, there are at least another 20 different boards under development expected to reach the market later this year.

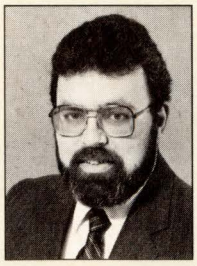
While SBus was designed as a compact, desktop workstation I/O board, it's probably not an accident that it also functions very well as a mezzanine bus on VME—two SBus cards fit comfortably on a single 6U VME card. Both the mezzanine bus and workstation bus share the same electrical and physical specification. In addition to offering its Sparcstation as a desktop workstation, Sun also offers it in board-level products, including a VME implementation of its Sparcstation 1 (its 1E board). Now, through a technology exchange and licensing agreement with Sun, Force Computers offers the 1E board as a second source and plans to offer the Sparcstation 2 in a 6U VME form factor.

Sun now offers at least one VMEbus adapter board with a pair of SBus sockets for using SBus cards in a VME environment. It's expected that Sun, Force and other companies wanting to play in the Sparc-compatible VME game will begin to offer a variety of cards with optional SBus sockets for added functionality.

Standard or not?

While SBus appears to fit the bill as a standard architecture for both workstation options and mezzanine buses, there are still some problems, says Fred Rehhausser, vice-president at Force. "SBus is a

Why SBus doesn't fit the bill



At BUSCON-91/West, SBus was proposed as a standard mezzanine architecture for VMEbus and Futurebus boards. Because of SBus' orientation as a workstation expansion bus, however, its selection as a mezzanine standard for real-time systems would be a mistake. Especially with the increasing use of VMEbus and Futurebus in real-time distributed multiprocessor systems, SBus lacks the performance and flexibility needed to support the full range of necessary I/O and coprocessor options.

The primary purpose of a workstation expansion bus such as SBus or Turbochannel is to provide low-cost I/O expansion for add-on modules, such as network or graphics interface cards. But an expansion bus is constrained by limits on space, power dissipation and physical access because of the compact configuration of desktop workstations.

Real-time VMEbus and Futurebus systems demand much greater flexibility and higher performance from their expansion buses due to the diversity and higher performance of their expansion modules. These modules run the gamut, from relatively low-performance I/O and data-acquisition devices to specialized memories, communications controllers and high-speed 64-bit coprocessors.

Five-year plan

As vendors and end-users collaborate on the definition of a mezzanine standard for VMEbus and Futurebus, the principal emphasis should be on flexibility and performance. And to facilitate a painless migration from VMEbus to Futurebus, the standard should be able to endure a five-year life cycle.

One capability that will be necessary to sustain a five-year cycle is processor independence. Presently, the mezzanine architectures used in workstation systems favor a single processor. Turbochannel, for example, is limited to MIPS and VAX chips. SBus, while theoretically processor-independent, has already been optimized for use with the Sparcstation architecture.

Another important capability that's needed to sustain a five-year life cycle is high performance. To support the 64-bit CPUs that will be used in next-generation VMEbus and Futurebus systems, an expansion bus must be able to handle 64-bit data transfers and 50-MHz clock speeds. It also should support block transfers and multimaster arbitration, which will be a necessity for next-generation intelligent distributed systems. And it must deliver these capabilities in a predominantly real-time application space.

Workstation mezzanine architectures fail to meet these needs. SBus Rev. B.0, for example, supports 64-bit transfers only through a multiplexed 32-bit address/data scheme. Turbochannel has similar limitations, supporting only 32-bit multiplexed address/data schemes and either 12.5- or 25-MHz clock rates.

Packaging technology

In addition to providing limited performance, workstation mezzanine architectures offer poor packaging flexibility. In a workstation environment, the mechanical and electrical packaging for the mezzanine bus and attached boards are highly constrained. The SBus configuration used in Sparcstation, for example, supports mezzanine card I/O access only via the front panel.

Because the packaging used in real-time systems varies considerably, the expansion bus must be able to adapt to a wide variety of thermal, space and I/O requirements. I/O access, for example, should be available not only through the front panel but through the back panel. This would facilitate replacement of boards without altering front panel cabling.

As users, CPU board vendors and peripheral board vendors tackle the definition of a standard mezzanine architecture, they should bear in mind that the primary market for VMEbus and Futurebus is likely to be embedded real-time systems. As such, simple workstation expansion buses such as SBus won't provide the necessary performance and flexibility. What's needed is a processor and system bus-independent architecture that can support the broad spectrum of low-cost and high-performance peripheral modules that will be used in next-generation real-time systems.

Clarence Peckham, vice-president of engineering, Heurikon

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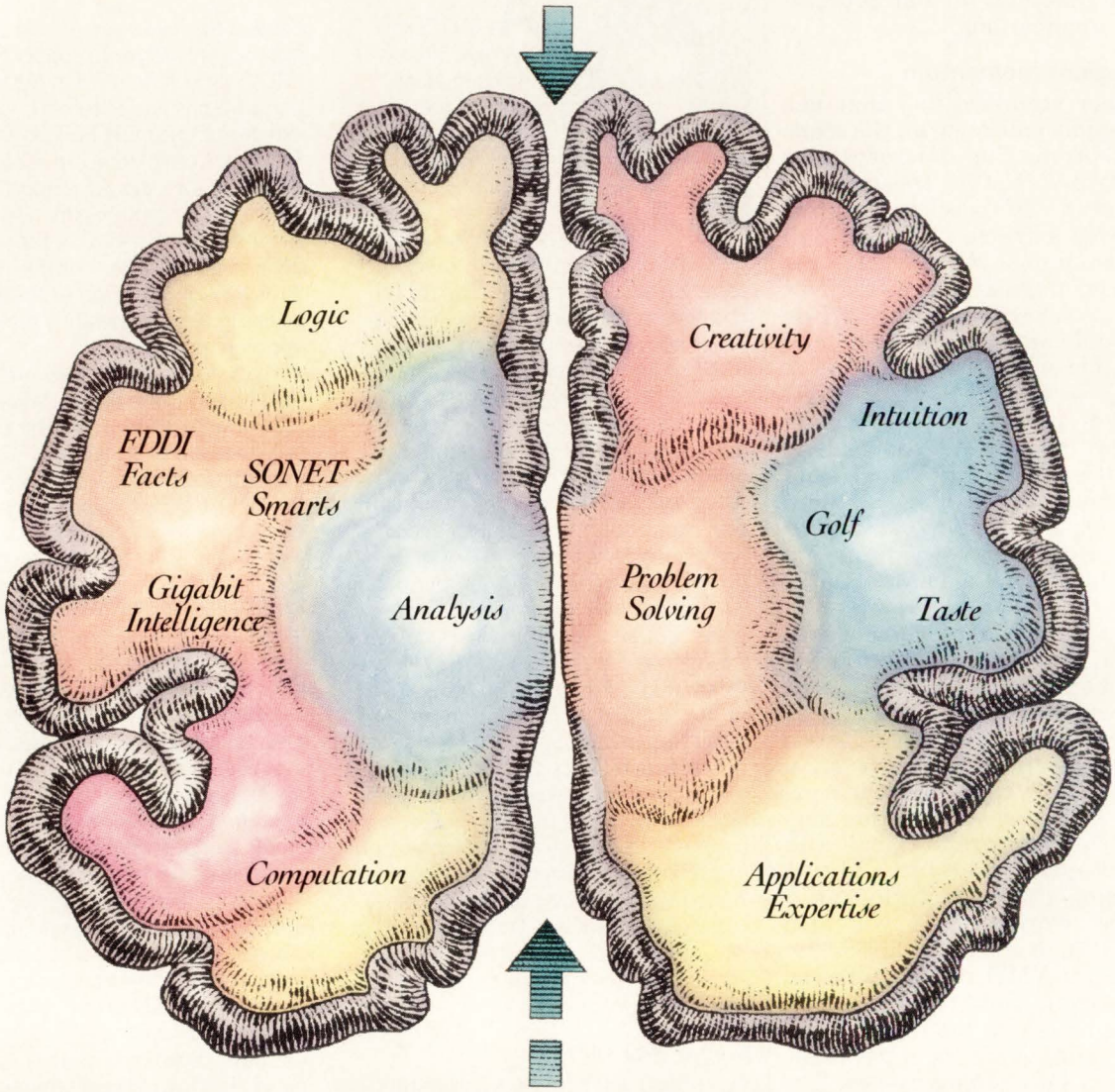

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two-slot solution and suffers from having the I/O at the wrong end," he says. "Most of our customers want I/O out of the P2 connector at the rear, not out the front."

SBus as presently configured uses a connector that, when plugged onto a VME board, exceeds the 0.8 in. height allowed for a board in a single slot. And, as Rehhausser notes, in all the present incarnations of VME-to-SBus adapters, the output is facing the front panel of the VME card. It would be a messy job to reroute ribbon cable to the rear of the VME chassis.

The day when a standard motherboard will comprise no more than a bus interface and a collection of connectors for mezzanine boards may still be somewhere in the future.

■ ■ ■

But help is on the way. Two connector manufacturers—Honda and Fujitsu—recently announced low-profile connectors that will permit fully compatible SBus connection to the workstation form factor and allow a single-high VME configuration. And there's little that prevents an SBus card from being turned around on its VME motherboard to allow connection to the back of the board for a P2 I/O.

SBus' position on Futurebus+ appears to be more secure than its position on VME since SBus is at least getting involved during the opening round. With its recent Version B.0 expansion to 64 bits, the bus is well-positioned to handle Futurebus+ I/O. But at this time, SBus hasn't been formally adopted as a standard; too many potential Futurebus+ vendors have other agendas.

Heurikon, for example, hopes to leverage its COREbus modules in future Futurebus+ boards. Similarly, Force plans to use its FLXibus, which has many hooks for a local 68000-based bus as well as high-speed transfer capability. In addition, Force is providing some strong hooks to its mezzanine bus in some of the ASICs it's developing for both VME and Futurebus+.

A board of connectors

As VITA's Alderman suggests, the day when a standard motherboard will comprise no more than a bus interface and a collection of connectors for mezzanine boards may still be somewhere in the future. First, good-quality, dense, reliable connectors aren't inexpensive and will undoubtedly add to the cost of circuit boards—both mother- and daughterboards. Second, despite the advanced packaging techniques that are available, board makers will have to use both the motherboard circuitry and mezzanine card options to achieve the kind of functional densities their customers will expect.

Even with the advent of multichip modules, board space will remain at a premium. Mezzanine buses will continue to fulfill two major objectives: to allow quick, inexpensive customization of standard boards and to offload more functions from the host system bus. Because of the high packing densities available using multichip modules and ASIC technology, the role of the host bus will largely be relegated to what Intel pictured as the function of Multibus II—a backplane LAN. Local buses combined with mezzanine buses—in some cases with multiple mezzanine buses—will serve the function of limiting traffic on the host bus. ■

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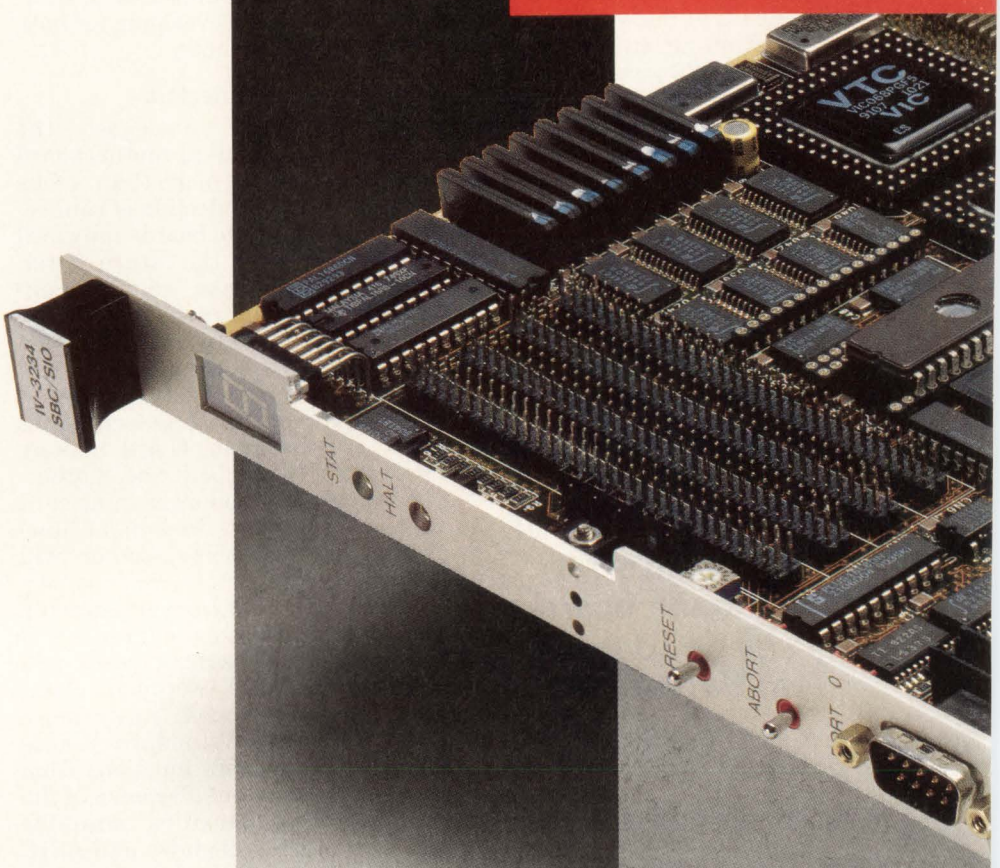

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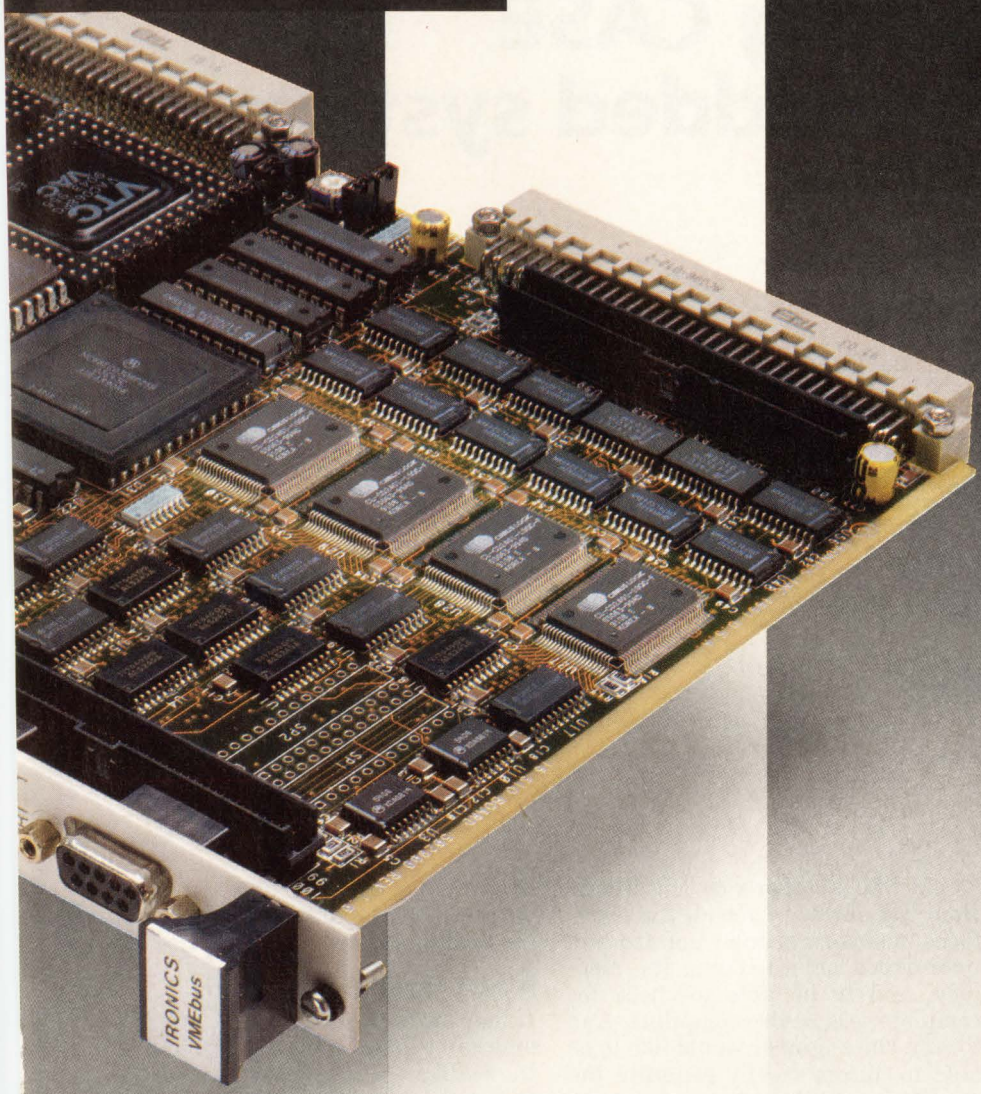

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CIRCLE NO. 51

New tools bring CASE power to embedded systems

Tom Williams
Senior Editor

Initially a disappointment for designers, CASE tools are making a comeback because they're needed to address the growing size and complexity of system designs. Today's tools extend CASE productivity gains to embedded system designers.

The early goal of CASE was to support and partially automate software development and to provide a top-down design environment that would take developers from abstract concept to finished code. The first CASE offerings failed to meet the expectations of embedded system designers, but a new generation of tools and tool environments appear to offer real gains in productivity and design accuracy.

The increasing size and complexity of software projects is driving the need for improved CASE environments. "The role of the CASE environment is to provide effective support for an efficient software-development process," says Ian Thomas, architecture coordinator of Hewlett-Packard's software engineering systems division (Sunnyvale, CA). "Early disappointments came from the fact that the first 'environments' didn't provide effective support. They were just collections of individual tools."

The engineer's wish list for CASE support, especially for major projects, would include the ability to look at the big picture by having a blueprint of the system under development. The engineer also would like to approach the design from top down, to get all the interfaces between modules defined and understood before coding the modules, and to be able to check for completeness before compiling. And finally, the engineer would like to be able to automatically generate the structure of the code, or even the code itself.

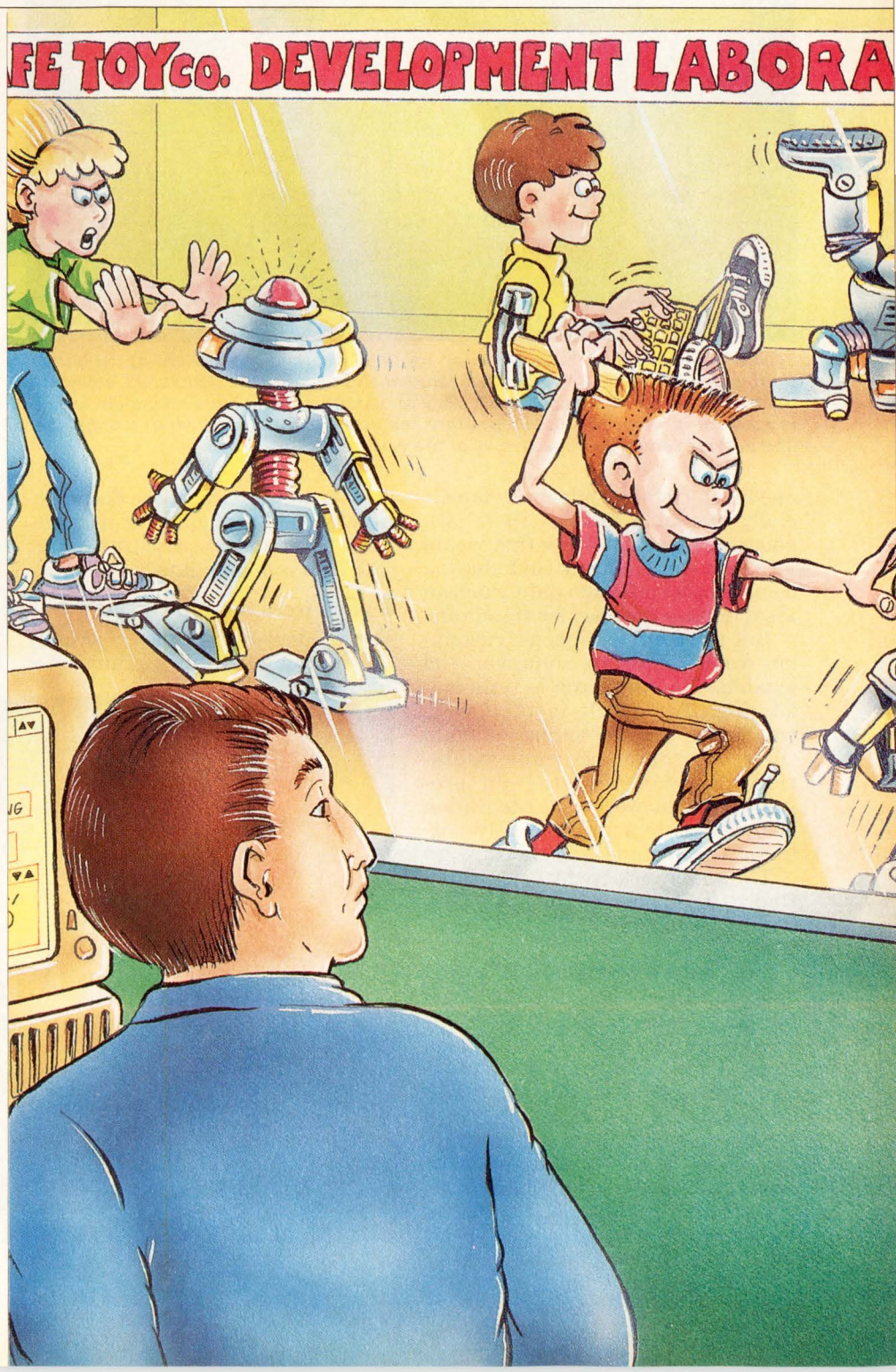
Part of the problem is that the environments have to meet the needs of two distinctly different groups—engineers and managers—who look at software engineering from different perspectives. Managers want to be able to track and control the process. Engineers want tools that will help them solve their problems and enhance the way they work. The conflicting support needs of these groups too often prevented early CASE attempts from meeting the needs of either.

"In the past, management pushed CASE on engineers, who resisted it because it hindered, rather than helped, them," notes Joseph Rothman, design tools product line manager for Ready Systems (Sunnyvale, CA). "Engineers don't want some 'methodology' crammed down their throats; they want to work with the same mental process they currently use, only enhance it."

Tools that meet real needs

It has been said that the crop of emerging CASE tools are "grounded in reality," a phrase with which Rothman is particularly fond. The phrase relates to the needs of embedded system developers, who must be able to relate the code they're working on to the real world. For embedded systems applications, the definition of the real world is based on detailed descriptions of the target system's execution environment (the operating system and processor, at least) and the external sensors and actuators that will be part of the final system. Embedded system developers need to do more than simply describe the real world; they need to simulate it. Some level of simulation capability is coming to be expected as a part of any embedded CASE environment. And the ability to maintain existing code via reverse engineering is also becoming a vital part of the CASE environment.

It's essential that CASE provide a means not only for managers to com-



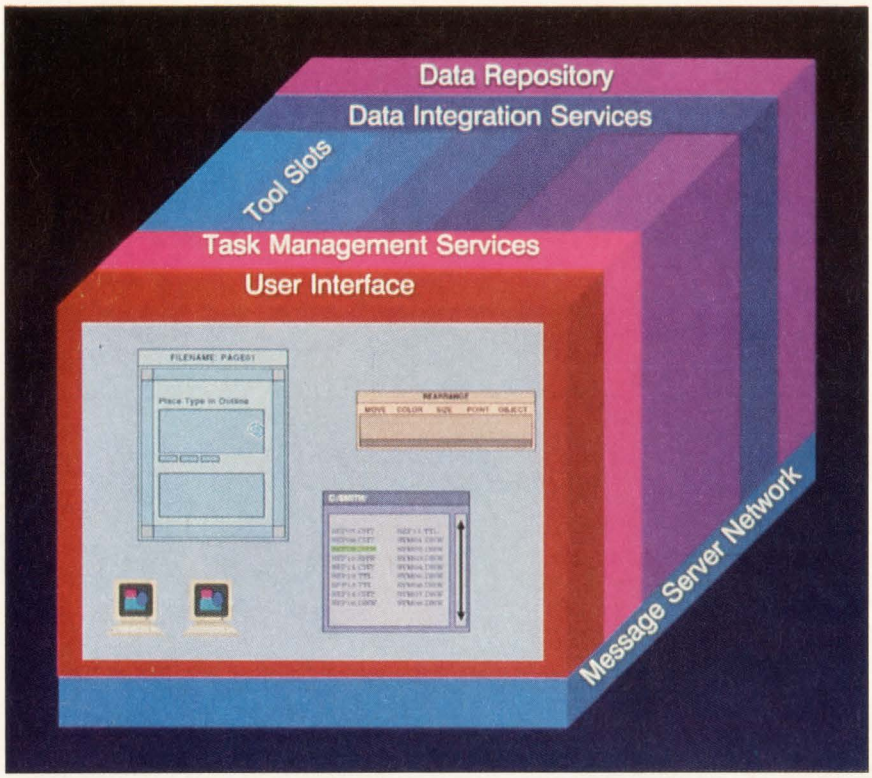
municate with engineers, but for engineers to communicate with each other. Everyone must be able to refer to the same document or structure chart in a meeting or to pass around instructions and suggestions that refer to specific parts of code.

The need for better management of software projects is growing. Software engineering is no longer the work of a group of isolated programmers turning out code; it's an organizational activity that must be coordinated. "Engineers are looking at tools, and managers are looking at frameworks," says Rothman. But both are needed to make a large development project work.

And, as HP's Thomas points out, "Software development is a capital-intensive process." CAD has for some time has been recognized as capital-intensive. Companies expect to spend large amounts of money for fast hardware platforms and sophisticated CAD tools for hardware engineering, but that realization has been late in coming in the case of software engineering.

Open tool environment ideal

An ideal for software engineers would be an open tool environment,



Typical of the so-called "toaster model" for CASE environments is Hewlett-Packard's Softbench. Vertical tools include structured-analysis tools, code generators, debuggers, and reverse-engineering tools. They're tied together by horizontal tools, including control-coordination, data repository and user interface tools, which coordinate and provide service to the activities of the vertical tools.

one in which they could use commercially available tools of their own choosing in a framework that would let them communicate and share a common pool of design data. Such an ideal implies the need for standards.

But as so often happens, customers want immediate solutions, and establishing standards is time-consuming. The result is that some companies are hastening to build their own database implementations for design data and proprietary frameworks for integration of tools, while simultaneously participating in standards efforts.

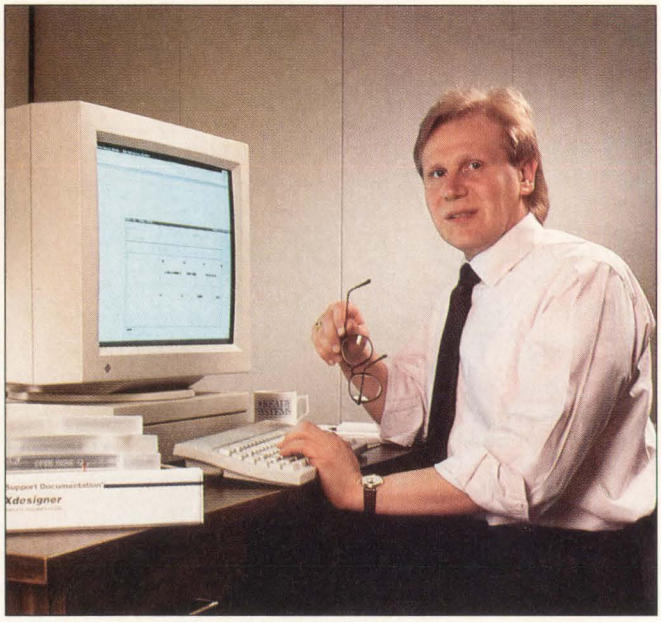
The Teamwork environment from Cadre Technologies (Portland, OR), the C Development Environment from Interactive Development Environments (San Francisco, CA) and the Softbench environment from Hewlett-Packard, for example, use variations on what is called the "toaster model." In this model, vertical tools, such as analysis tools, design tools, coding tools, and reverse-engineering tools, are integrated with horizontal tools that coordinate and provide shared services to the vertical tools. Horizontal tools include a common user interface for the vertical tools, documentation tools, configuration-management tools, and traceability tools, as well as a common data repository.

View from the top

The top-down view, which is actually the design blueprint in a number of CASE environments, is usually produced with a structured-analysis tool that gives a graphical description of the software architecture under design. Tools such as Teamwork from Cadre; the C Development Environment from Interactive Development Environments (IDE), which includes that company's software Through Pictures toolset; Framework/RT (part of Caseworks/RT) from Multiprocessor Toolsmiths (Nepean, Ontario); and VRTX Designer from Ready Systems let designers graphically describe the structure of the program, as well as specify data and control flow.

A structure chart serves as a reference when the design has progressed to actual code, helping users navigate through the code. The chart lets users see different views of the program, including the structure, data flow, control flow, and data dictionary views.

In the Cadre Teamwork family, for example, a design might first start from a requirements document produced with Cadre's Architecture Design and Assessment System, which analyses both hardware and software design considerations. The requirements document doesn't have an automated link to the design process other than an ability to check for completion of requirements. System designers begin the preliminary design by using Teamwork/SD, the structured design tool, to define modules and interfaces and to build a structure chart. A project leader can specify



Joseph Rothman, design tools product line manager at Ready Systems, says that it's important to bring hardware considerations into the early stages of software design. Designers must consider timing issues to see how all the combinations will affect the software system.

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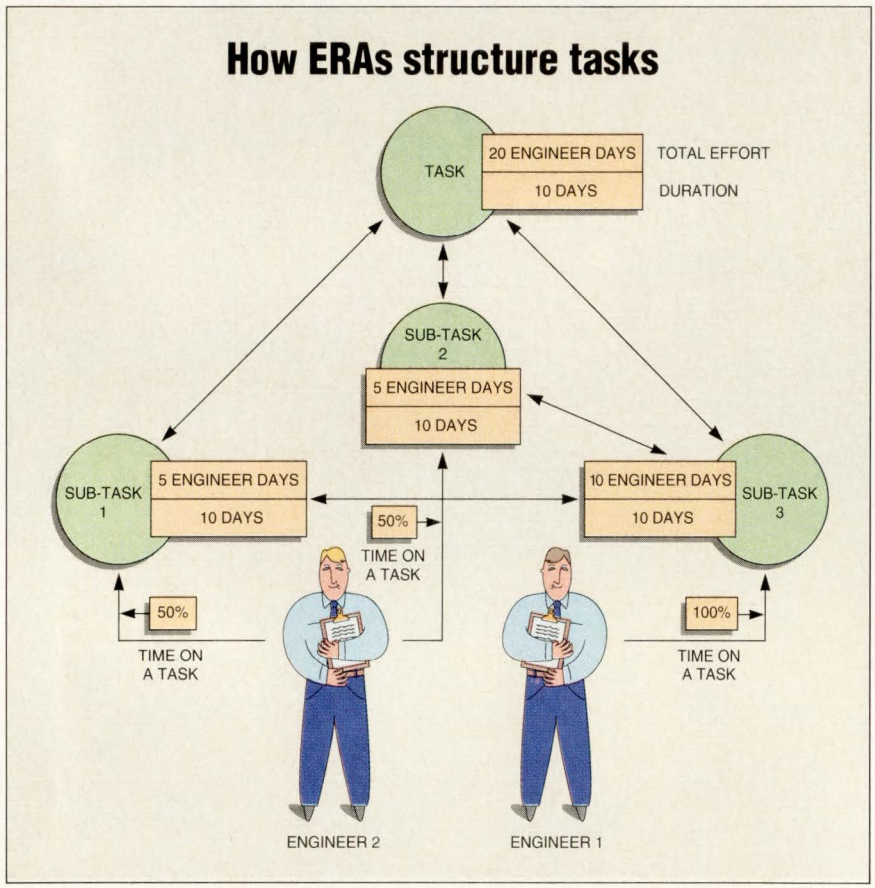
the function and the inputs and outputs of each module so that all the members of the programming team understand the structure and the interface specifications of the system on which they're working.

Cadre's product manager, John Blattner, notes that Teamwork serves as both a design tool and a communication tool. "It may not reduce the number of meetings, but it will reduce the amount of time you spend in them because everybody is looking at the same structure charts."



In an entity relationship attribute database for design data, some tasks share a parent/child relationship (red lines) and others are related by attributes of precedence (green lines). Relationships can be defined in terms of people assigned to tasks and the amount of time they spend on each (blue lines).

The next major step is to generate compilable source code. There's no way yet to fully automate this process. But users can specify all the parameters, variables, data types, and other factors. They also can describe in detail what a module is to do, either in free-form text or in some kind of pseudo-code. Programmers can then work on individual modules knowing exactly what inputs and outputs to use, what data types they must handle and what sort of algorithm they must produce. Cadre's Teamwork/C Sourcebuilder, for example, lets users click onto boxes representing modules created under Teamwork/SD and open them to enter information such as variable declarations, free-form text descriptions of the modules and actual code. The automatic code generation then pastes these modules together into a compilable source file, including calls to library modules specified at the design level.

IDE's C Development Environment Phase II can automatically generate C source code files from its structured designs, which are created by defining the structure, control and data flows, and code modules. If changes made at the source level affect the structure, they can be automatically reflected in the higher-level views.

Ed Mueller, director of applications marketing at IDE, stresses that it's not enough just to update the structure. Users must synchronize the design with the code if they make any change in the code that affects the design. "What if you change a data type?" he asks. IDE's C Development Environment has facilities to maintain this synchronization.

A common ability of the latest CASE tools is to let programmers get into the code to fine-tune its performance or make changes. Both Cadre and IDE have formed alliances with Saber Software (Cambridge, MA) to include that company's Saber-C language tool in their products. Saber-C runs in an interpretive environment that lets programmers experiment with routines while examining a source module. Programmers can write a routine in Saber-C, test it and, if it performs as expected, incorporate it directly into their source file.

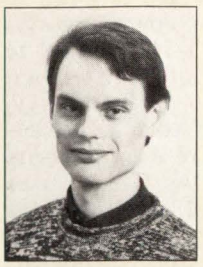
Two other aids to automating the process of producing code are the VRTX Designer from Ready Systems and SystemBuild from Integrated Systems (Santa Clara, CA). VRTX Designer specifies the function of tasks by letting programmers write pieces of pseudo-code to describe the functions within tasks. After doing system simulation to their satisfaction, designers can go in and flesh out the code skeletons by filling in C source code.

Integrated Systems' SystemBuild is based on libraries of control code modules for C, Fortran and Ada that can be graphically linked together and hierarchically nested. To these, programmers add parameters, variable names and other information to build up an industrial-control system. The system also can include models of actuators and sensors and their behavior. Users also have the option to create a custom module by entering their own code and algorithms. The module can then be included graphically in the design. When users want to produce compilable code, SystemBuild constructs a source file from the library modules along with the users' variables, parameters, module names, custom-written code segments, and comments.

Tools applauded by customers

The ability to automate the move from a high-level system description down to code and to work changes into the structure charts, while also generating full documentation (including mil-spec documents), has won praise from users—and some of

One answer for developers of hardware-dependent code



Developers of hardware-dependent code often find themselves in a bind. Because they can't test the code until they have a physical prototype of the system, they can't verify many system assumptions and design decisions until the hardware design is completed. Postponing integration and verification until the end of a project can cause integration problems which, in turn, can stall the overall project schedule.

It's important that software be tested in direct interaction with "ideal" hardware, or in a hardware environment free of line spikes, spurious interrupts, data line crosstalk, malfunctioning components, and hardware race conditions. Otherwise, isolating programming problems from those caused by hardware becomes far too complex.

Simulation lets developers isolate programming problems. An instruction set simulator (ISS) is currently the most efficient way to test hardware-dependent code. An ISS is a software-execution engine that interprets and executes a particular microprocessor's instructions. It has a simulated address/data bus and may have other functions of the target microprocessor. An ISS is based on clock cycle resolution and can execute many instructions per minute, but it doesn't preserve timing accuracy between clock cycles.

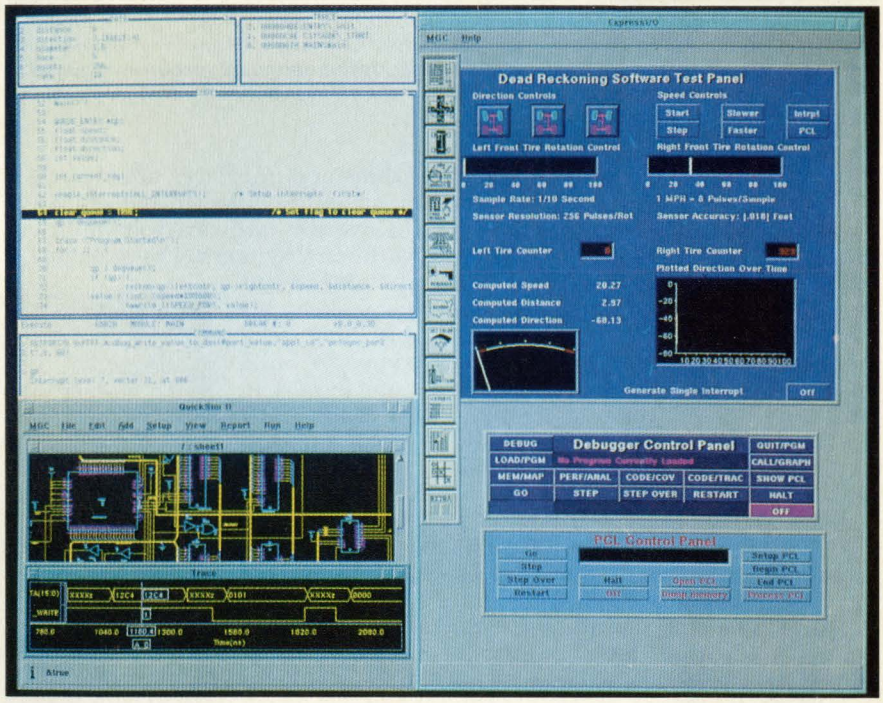
ISS technology lets developers test embedded software in a stable, predictable environment. It also lets users deal with a set number of problems without the occurrence of unknown external conditions, such as interrupts and malfunctioning components. Moreover, software can be developed concurrently with hardware using this technology.

Virtual-control panels simulate I/O

An ISS is only part of the solution for developers of hardware-dependent code. Embedded systems can't be tested without appropriate I/O interactions. When used in conjunction with a virtual-control panel that simulates I/O tasks, an ISS allows software testing under realistic conditions.

Virtual-control panels work to stress test the system without having to build a physical prototype. Users can answer critical questions, such as whether the interrupt handler can service all the interrupts at the specified interval; whether interrupt-contention problems can be solved by decreasing the speed of a serial port; and whether the system can perform adequately with DRAM.

Hardware designers have long used control panels and test jigs to verify correct functionality, without having to wait until the complete system was integrated. Creating panels and jigs in a virtual environment simplifies the task of developing interactive test systems.

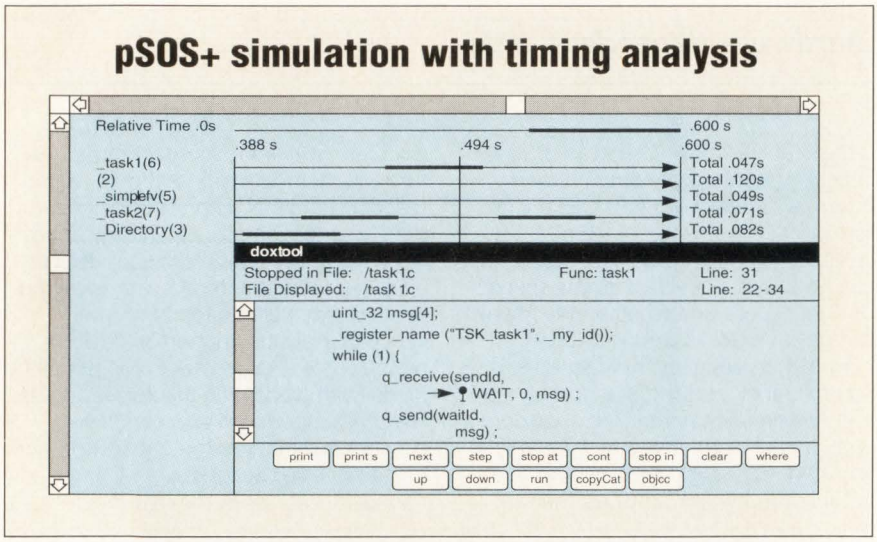


An example of a virtual-test environment simulating an embedded real-time system is shown in the photo above. The application is a dead-reckoning system, a part of an automobile-navigation system that tracks the speed, distance and direction of a car. The system reads sensors placed on the front wheels and uses the difference in speed between the wheels to calculate the car's direction. It determines the car's location by performing dead-reckoning calculations and then transmits the data to the display unit.

This example is based on Mentor Graphics' CodeLink Station. On the left is a high-level language debugger tied through memory-mapped I/O to a virtual-control panel. Express I/O, the control panel toolkit, models the surrounding environment and hardware devices, enabling users to interact with the simulated system. Built on top of Mentor Graphics' Decision Support System, Express I/Ouses a spreadsheet programming model with predefined graphical gadgets. The tool supports cell watchers, which continuously monitor the spreadsheet and trigger specified actions. Cells link to memory locations in the debugger, which lets CodeLink Station pass input and output between the two environments just like the final system will.

Models for the wheel sensors in this example appear in the upper part of the Dead Reckoning Test Panel. Spreadsheet statements describe the behavior of the sensor. Since the spreadsheet contains built-in math functions, it's easy to model heuristics, delays, temperature deviations, and other characteristics. Trade-off analysis of different types of devices can thereby occur by substituting the behavioral function for the specific device. This virtual-test environment provides verification that the physical system will behave correctly the first time.

Peter Fornell, product manager, Mentor Graphics CASE Division



CopyCat simulation under Multiprocessor Toolsmiths' Caseworks/RT shows a timing chart of different tasks. This lets users see if their tasks are meeting their timing constraints so they can, in turn, make decisions about the hardware resources required. The chart also lets users easily spot lockout or starvation conditions that may require adjustment of task priorities.

the users have won praise from their customers. The Space System Division (SSD) of General Dynamics (San Diego, CA), one user, was commended by the Air Force for the speed and quality of its work in software development and documentation for the Air Force's new advanced launch system (ALS). The ALS is a family of vehicles aimed at putting large payloads into low Earth orbits at much lower costs than previous systems.

General Dynamics' SSD built a multivendor CASE environment around IDE's Software Through Pictures, which is now included in the C Development Environment. The team even established a link between its CASE environment and the Air Force Space Systems Division office to ease communications. SSD set up a single data dictionary for the entire project to ensure consistency of all software.

The ALS is scheduled for delivery in 1998. General Dynamics was chartered to deliver requirements specifications in 16 months (and, later, a design document and an engineering design review) and was able to do so in 6 months. The Air Force major in charge of software engineering on the project rated it as one of the top 10 projects with which he had been associated.

Need for real-world simulation

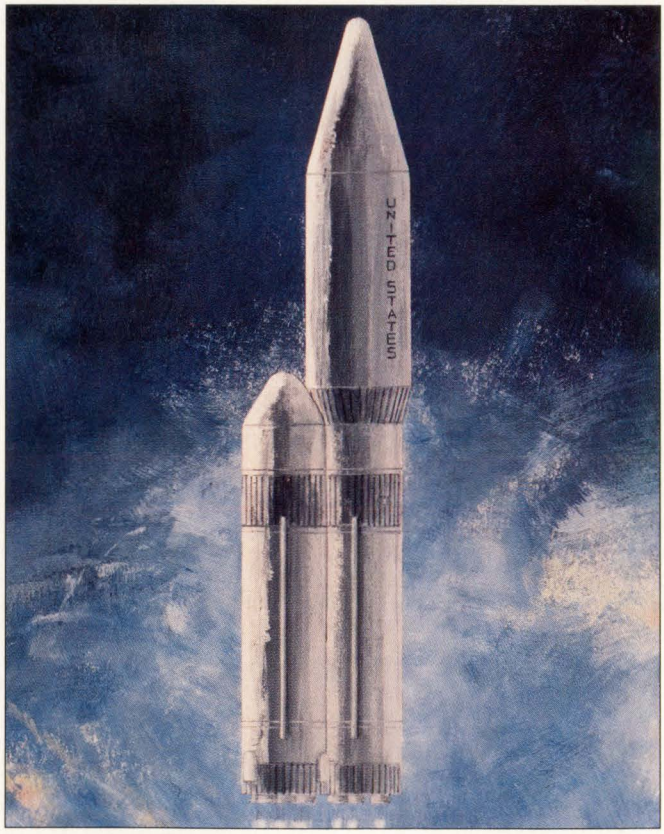
Simulation of software for real-time and embedded systems involves far more than just seeing if the algorithms and interfaces are correct. It must be grounded in the reality of the overall hardware/software/real-world environment. Every engineer at some point has asked, "Is this thing we're trying to build going to work in the real world?"

The application code comes face to face with the real world at several points and requires simulation to verify that it will work. It interacts with the hardware-execution environment, the hardware-dependent system software layer (the OS and/or the real-time kernel, device drivers and so forth), and the external set of sensors and actuators, which have their own behavior and timing constraints.

Ready Systems' VRTX Designer, which is optimized for Ready's own VRTX32 real-time kernel, and Multiprocessor Toolsmiths' Caseworks/RT are CASE environments that are tailored to a specific kernel or operating system. Caseworks/RT is oriented to Multiprocessor Toolsmiths' own real-time Unix-like operating system, Unison, and to the pSOS+ kernel by Software Components Group (San Jose, CA). Unison uses the pSOS+ kernel but includes Unix-like features such as sockets and Unix terminal I/O. The operating system-simulation tool used by Caseworks/RT simulates both the pSOS+ and Unison environments. Caseworks/RT also will support the yet-to-be-shipped Motorola's VMEexec real-time operating environment for Unix (also based on pSOS+).

Early evaluation helpful

Both VRTX Designer and Caseworks/RT let users enter graphic design specifications and generate skeleton code from which C code can be produced. Each also has a performance-modeling feature that dis-



General Dynamics' Space Systems Division came in 10 months ahead of schedule on its software-development project for the Air Force's new advanced launch system (due in 1998). The company worked in a CASE environment built around Interactive Development Environments' Software Through Pictures.

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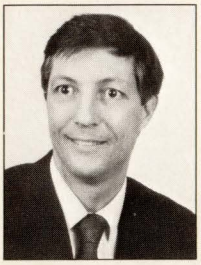
CIRCLE NO. 53

How to effectively introduce real-time CASE technology



The effective introduction of new software-engineering technology into a product-development or project environment can have broad implications for an entire company. But the learning curve associated with any new technology usually means that, at first, the new approach is less effective than tried-and-true methods. The key issue is how to inject new technology into the process to improve productivity and quality, while reducing risk. Some CASE users across the software industry over the last 10 years have been able to do exactly that.

The most important factor in choosing a new CASE technology is the application. All other factors take second place. The technology must be chosen to meet both the short- and long-term goals of the organization.

Next in importance is how different the new technology is from the existing way of doing things. The greater the difference, the higher the risk of failure due to user rejection, long learning curves and resulting lost productivity.

The third significant aspect is management's degree of commitment to the new approach. If management's commitment is misjudged, the entire program might be scrapped before substantial benefits have been realized.

The CASE hierarchy

CASE technology is used to some extent in all real-time computer companies. It can be roughly grouped into four categories. Upper CASE technology includes requirements analysis and prototyping tools. Middle CASE technology provides design, detailed design and coding tools. Lower CASE technology comprises compilers, linkers, assemblers, debuggers, real-time operating systems, and testing tools. The final layer, management technology, includes project-management tools, configuration-management tools, data repositories, standards data, and tracking information.

Most tools fall across boundaries within this definition of CASE technology. A simple example is a text editor that can be used for requirements documents, coding, binding executables, and writing management reports. Most companies use a mix of lower CASE technology and management technology, while more-advanced users add upper CASE technology. More-advanced companies are adding middle CASE technology, particularly to deal with real-time constraints.

Lessons from users

The first lesson from users who have effectively introduced the technology into their projects is to approach CASE with a reasonable set of expectations. It can't be expected to solve every problem instantly. Productivity increases in the 8 to 10 percent per year range are reasonable.

The second lesson is that training is essential. Employees must be educated and convinced to buy into the new technology. The greater the conceptual gap, the more training is required. If the conceptual gap for the new technology is large, 40 percent of the budget should be spent on training and 60 percent on tools. If the gap is small, on-the-job training will suffice.

Third, users shouldn't build what they can buy. CASE technology is difficult to develop and expensive to maintain, and most tools are used in low volume. Tools should be purchased, and the user's focus should be on integrating the pieces.

Users should turn to standards wherever possible to minimize risk, but beware of early adoption of single-vendor standards. IBM, Sun, Digital Equipment Corp, and HP/Apollo, for example, are trying to provide data repositories and/or tool managers to integrate various CASE technologies, but none is advanced enough in this area to provide a low-risk solution.

It's important to structure a plan for the adoption and evaluation of the new technology. To minimize risk, the technology should be added incrementally if possible and/or practical. Users should choose a small project to start with and view it as a learning vehicle. They should get management to sign off on their plan periodically and to give feedback as problems develop. And the plan should never be cast in concrete. Careful monitoring and replanning based upon experience is critical.

What to look for

Software reuse is the easiest and most practical means for a company to accelerate software-development results. So the ability to integrate existing designs and code into a CASE environment may be an essential concern. If it is, users should look for the ability to package existing code for use with an automatic code generator and the ability to reverse engineer existing code.

Management control and visibility becomes critical as the team size grows beyond 10 developers. If the project team consists of 10 or more programmers, it's essential to carefully evaluate the new technology's impact on the management level of the CASE environment.

Kim Rowe, MSEE, MBA, president, Multiprocessor Toolsmiths

plays the relative execution times of modules in Gannt chart form. The timing diagrams not only provide a sense of the performance users can expect with a given processor and clock speed, but also let users spot problems such as lockout and starvation early in the design process.

Gannt charts give an early look at the suitability of the execution environment. (Can I meet my timing constraints with a slower processor or do I need a faster one?) By giving a high-level view of the software architecture, they also let developers spot flaws in the design at the architectural level, such as the arrangement of task priorities, without having to start looking for bugs when the code finally crashes.

Taking operating system and processor constraints into consideration early in the design is extremely important, according to Tom Bishop, software project manager for Siemens Medical (Danvers, MA). Siemens Medical is using VRTX Designer to model an existing system so it can be ported to a VRTX real-time executive kernel. Bishop is so impressed with the tool that he plans to use it in his next "fresh start" real-time design. The firm

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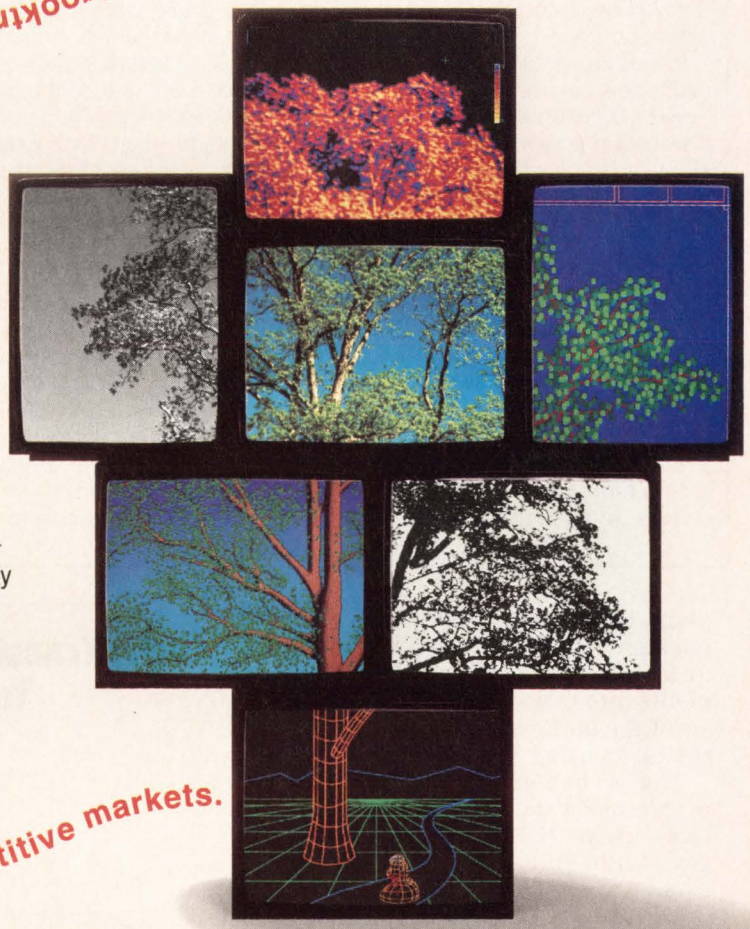

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CIRCLE NO. 55

CASE database design the key to frameworks

Perhaps the biggest challenge today in creating a homogeneous framework for CASE is establishing a data repository that's sufficiently rich and flexible to serve the needs of different types of tools and users. With operating system file services clearly inadequate and traditional relational databases also showing limitations, efforts are turning toward more object-oriented database models. But even object-oriented approaches don't satisfy all the demands that will be placed on a software design data repository.

In a design data repository, tasks might be stored according to which task "owns" which subtasks—a normal hierarchical scheme. But there would also have to be information on precedence, or which tasks must execute before which other tasks. Precedence wouldn't necessarily correspond to the task hierarchy. In addition, the database would likely be required to keep track of which programmers are assigned to which modules and what percentage of their time was spent in each. Additionally, document-management tools might require that data be organized hierarchically in terms of document, chapter and section, and also that references to tasks and program modules be tracked, as well as cross-references to other sections and to the author(s).

Such a data repository would store data entities and their relationships as defined by their attributes. It would thus be an entity relationship attribute (ERA) database rather than an object-oriented database in the traditional sense.

The ERA model is the prime focus of development activity in the CASE community. In the ERA model, data is stored in a single, complexly structured database that lets individual tools access data according to their own needs. Each tool's view of the data would be defined uniquely as required by the tool's function. Tools would communicate with each other via protocols that would alert other tools that, for instance, a given piece of data has been changed.

The data repository scheme that's gaining ever-wider attention is the object management system (OMS) embodied in the portable common tools environment (PCTE), which came out of the Esprit (European Strategic Program for Research in Information Technology) effort. PCTE's OMS is built on an ERA database. PCTE isn't a stand-alone tool environment available to software engineers, but rather is being evaluated by environment designers for possible commercial offering as a tool environment along the lines of Hewlett-Packard's Softbench. PCTE also addresses user-interface and control-integration issues. Softbench, it must be stressed, is not PCTE—nor does it use PCTE's repository. At present, Softbench addresses mainly the user-interface and control-integration aspects of an open CASE environment.

HP, however, supports adoption of PCTE as a standard. A number of tool vendors, such as Cadre and Integrated Development Environments, have versions of their tools that will run under Softbench and may now migrate toward PCTE.

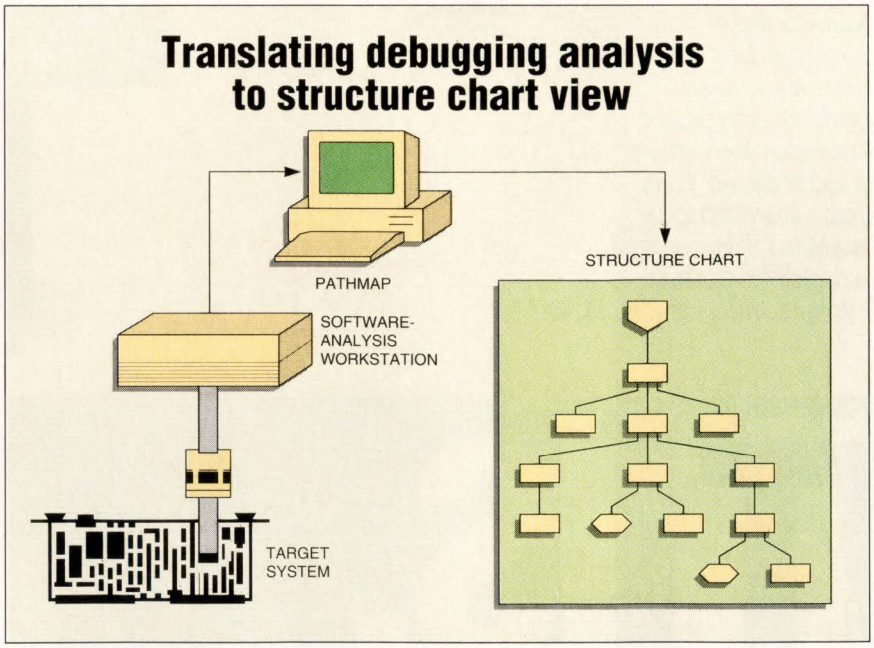
Frameworks such as Softbench and PCTE are meant to serve the needs of tool writers as software platforms for their products. In that sense, says Kim Rowe, president of Multiprocessor Toolsmiths (Nepean, Ontario), "The industry is shifting. And the shift is toward vendors of workstations to provide an integrated framework for CASE tools. So the reality from a individual [tool] vendor's point of view is that you have to be able to plug into their frameworks."

plans to use the Cadre Teamwork package to do the requirements analysis, translate the requirements into tasks based on an analysis of the data flow, and then design the tasks using VRTX Designer.

"We've had mixed success with people using the full suite of Cadre tools," says Bishop. "People could get caught in an endless modeling loop."

One benefit of a CASE tool that's oriented toward an operating system is that it has been designed with an understanding of the details of the operating system. This is especially important for designers who need to understand the behavior of a real-time system. "VRTX Designer understands that there's such a thing as an operating system that has overhead," Bishop adds.

Along with operating system considerations, workload must also be factored in, says James Browne, chief scientist for Scientific and Engineering Software (Austin, TX).



Using Cadre's Pathmap facility in conjunction with a software-analysis workstation, users can relate code running in the target system with structure charts created with Cadre's Teamwork/SD structured design tool.

"When you're going to do design evaluation, you can't just have the design itself. You have to have the workload that drives the design." Workbench from Scientific and Engineering Software (SES) graphically describes the architecture and timing characteristics of a hardware and operating system environment. Users can graphically model pipeline delays, scheduler behavior, or memory access and intertask communication delays, for example, without having to do a full gate-level simulation of the processor. Users can also model how operating system components, such as interrupt handlers, affect the execution of code in the target system.

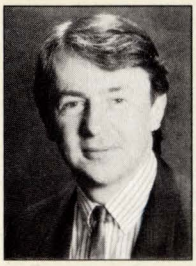
SES has allied with IDE to translate a software model created with Software Through Pictures so that it can drive an execution environment model created with SES Workbench. After generating code from the Software Through Pictures model, it's possible to look at how the instruction flow affects the hardware architecture to see if timing deadlines are met and to identify bottlenecks. According to Browne, it's important to be able to simulate the execution environment at the system level to simulate software performance because the complexity of modern systems make them impossible to fully simulate in software.

Focus on hardware dependencies

It's rather ironic that the software industry has made much more progress with software that models and simulates hardware than with modeling and simulating software. The CASE Division at Mentor Graphics (Wilsonville, OR), a longtime leader in hardware electronic design automation, is concentrating on the vital layer where hardware and software meet. "The software aspect we're talking about is the software that's really highly hardware-dependent, such as boot-up routines, diagnostics and device drivers," says Mentor's CASE Division marketing manager John DiFerdinando.

Mentor is advancing the idea of "virtual integration," or the ability to use a behavioral software model of the hardware to simulate the execution of actual code before either hardware or full application software is available. The traditional hardware-simulation models, which simulate at the register and gate

PCTE: building a foundation for CASE



The task of providing tool support in an integrated CASE environment is beyond the resources of any single organization. Software developers need an environment that lets different tools work together in an integrated fashion. Software tool developers need a set of basic environment-support services on which individual tools and integrated environments can be built. The best answer to these needs now seems to be the portable common tool environment (PCTE).

PCTE defines a set of basic services on which software-engineering environments can be built. The services are designed so that they can be implemented robustly on LANs. They're scalable as the amount of data and the number of developers in the environment increase. They don't favor a particular language for writing the tools that will operate in the environment. And they allow evolution of the environment while it's operating.

The services are far better suited to the needs of environment builders than are the basic services provided by operating systems. Their focus is on supporting the work of complex, concurrent, multiuser software-development projects, rather than supporting particular data-management needs for a single tool.

PCTE began as an Esprit (European Strategic Program for Research in Information Technology) project in 1983. The first PCTE specifications were published in August 1986. The project has since grown into the PCTE Initiative, with a total investment of more than $100 million. The PCTE+ project was started in 1987 to revise the specifications so that they could be used for the development of secure systems, including defense systems. Work on standardization of the interface definition also began in 1987. This effort led to the formal adoption in December 1990 of a PCTE standard by the European Computer Manufacturers Association (ECMA). ECMA is open to all information technology companies that have manufacturing capabilities in Europe. ECMA members who were active in the development of the standard include Hewlett-Packard, IBM, Digital Equipment Corp, and Bull-HN.

The ECMA PCTE standard describes the following set of services:

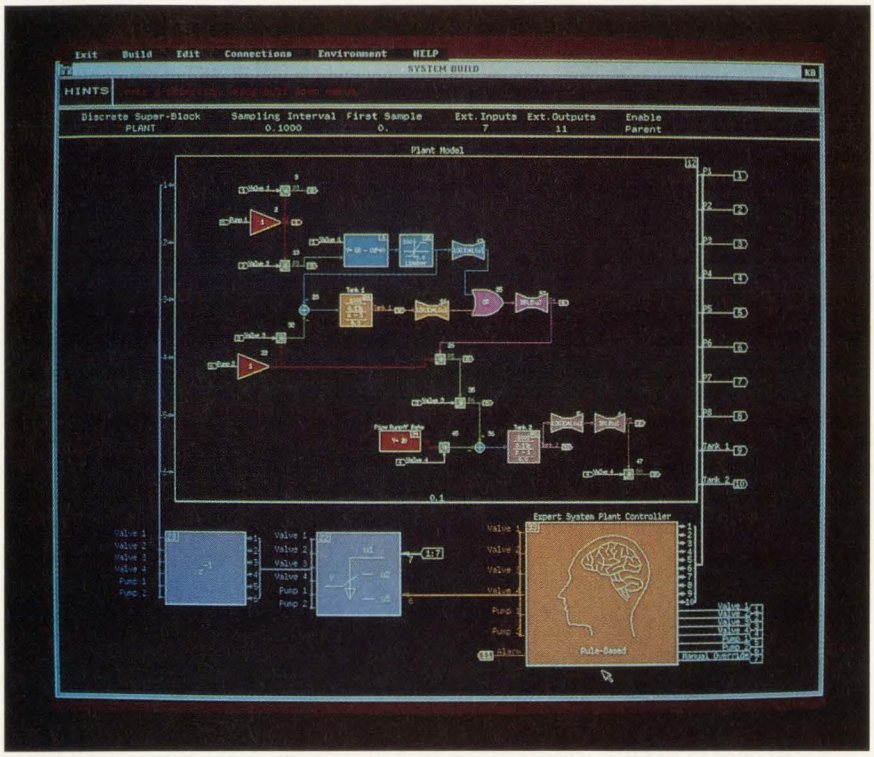
- object management—stores the environment's data
- schema management—describes the data managed in the environment
- object contents—reads and writes any data that's organized as files
- process execution—manages the execution of tools
- interprocess communication—lets executing tools communicate with each other
- notification—lets a tool declare an interest in an object and be notified when it's accessed
- concurrency and integrity control—protects data from concurrent access and also acts a transaction mechanism
- security—enables access control and mandatory security as defined by the U.S. Department of Defense
- auditing—monitors system usage
- accounting—records system resource usage

All of the preceding services are provided in a LAN so that distribution is transparent to the user and tool writer. The services appear to the tool writer as a library of about 220 different calls.

PCTE 1.5, which is available now, offers a reduced version of these services. Implementations of PCTE 1.5 are commercially available and are planned for HP's 9000 workstations, Sun-3 and -4 systems, IBM RS-6000, and Bull-HN workstations. The software is produced by a French company called Emeraude. Networks of heterogeneous machines will be supported in a release that will be available later in 1991. The first implementations of the ECMA PCTE standard are expected to be commercially available during 1992.

Few popular CASE tools run on PCTE. Since PCTE 1.5 is an upward-compatible extension of Unix System V, porting of existing Unix tools is usually easy, but the ports don't use PCTE's rich set of services to the fullest extent. Several of the CASE tool vendors are tracking PCTE and will port their tools to it as customer demand grows.

Ian Thomas, BS, MS, architecture coordinator, Hewlett-Packard



The SystemBuild tools from Integrated Systems let users construct a control system on screen using graphical elements that represent control algorithms. Users can animate a model they create using the characteristics of actual components to verify the correctness and robustness of the design. The blocks can then generate a compilable source file that can be run in a hardware environment to test the final design.

levels, aren't suitable for this because of their complexity and slow speed. Bus-functional models simulate hardware states and behavior at the pin and connector levels but have yet to incorporate an instruction set simulator. Mentor is proposing a level of simulation that would mate bus-functional hardware simulation with instruction set simulation.

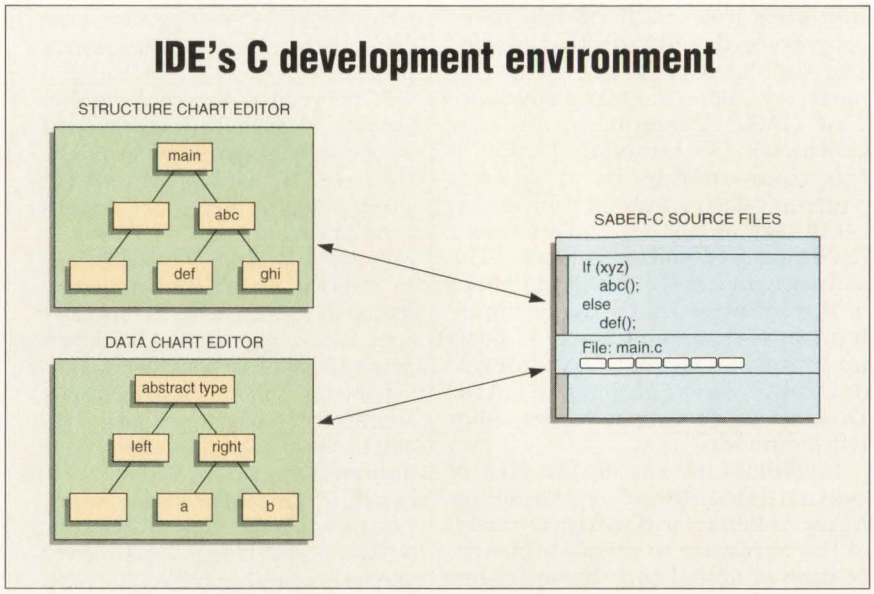
Such a combination would serve the needs of users who want to be sure they can boot their proposed operating systems on a new hardware design before committing to code or silicon. "On a full-functional model, it could take you as much as a week to boot up Unix," says DiFerdinando. So a bus-functional model combined with an instruction set simulator would be a compromise in terms of speed and detail.

"But the amount of software that will be simulated in this way will be small," he adds. "Anything that can be reliably proven in the native environment probably will be."

The SES and Mentor approaches to simulation complement the approaches taken by Multiprocessor Toolsmiths and Ready Systems, whose timing models of application tasks are based on known characteristics of the hardware-dependent software and on the known behavior of target processors. Mentor and SES extend that idea to the ability to define and simulate custom hardware/software environments upon which code can be tested.

Simulation for the real world is a prime focus of Integrated Systems; behavioral simulation up to and including animation is supported by the SystemBuild control design environment. SystemBuild starts with a model of the electromechanical system, which usually consists of motors, actuators hydraulics, gears, and sensors. Such a model can be built using the manufacturer's specifications of actual components. In addition, the company's XMath tool can help take data from actual physical devices and add it to the system model to include the variances in parameters that occur with any components. "The idea here is to base the CASE tool on a model of a physical system rather than on some abstract schematic," says Ben Tang, Integrated Systems' manager of product marketing.

From there, users go into the control design toolset, which is the heart of SystemBuild. They choose a control strategy and construct it using algorithm blocks, to which they can add parameters and interface details. The blocks can be nested to any depth. Using the block model with the system model, users can check whether the control strategy will work and see how robust it is. If an IC inserter doesn't hit the socket and bends pins, for



Under the C Development Environment from Interactive Development Environments, users can click a mouse for different views of the design. Programs can be viewed as structure charts, data structures or C source code. Changes made to one view will automatically be reflected in the other views.

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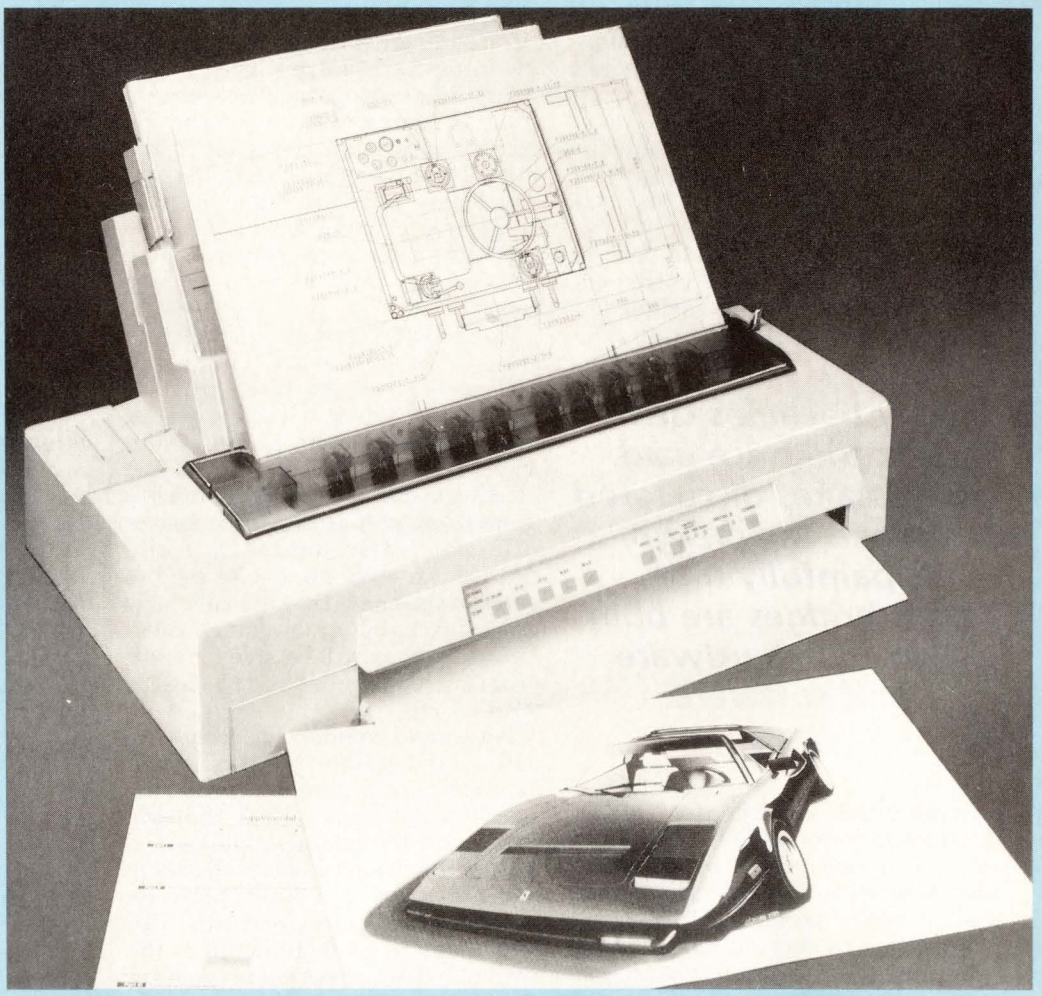

SPECIFICATIONS*

Printing Method:	Non-impact serial bubble jet
Printing Resolution:	360 x 360 dpi - High-Quality Mode; 180 x 180 dpi - High-Speed Mode
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Print Head Life:	200 million characters/ High-Speed Mode
Printing Speed:	300 cps in High-Speed Mode, 150 cps in High-Quality Mode
Printing Direction:	Bi-directional or uni-directional
Line-feed Speed:	40 ms/line
Line-feed Pitch:	Min. n/360 in. (n = programmable)
Paper Handling:	Plain paper; cut sheet (5.8 -14.3 in. wide ASF, 3.5 -17.0 in. wide manual feed), fanfold (4.0 -16.0 in. wide), envelope, transparency
Paper Weight:	14 - 33 lbs. (cut sheet manual), 16 - 23 lbs. (cut sheet ASF), 14 - 23 lbs. (fanfold)
Optional Auto Sheet Feeder:	Single- or dual-bin types (100 sheets per bin)
Ink Cartridge:	Color: black; Capacity: approx. 40 g; Life: 2 million characters High-Speed Mode
Acoustic Noise Level:	Less than 45 dBA
Power Source:	120 VAC, 60Hz; 230 VAC, 50Hz
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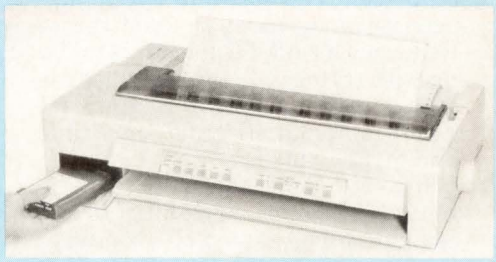

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CIRCLE NO. 56

instance, is it due to some inherent deficiency in the resolution of a stepper motor, or to something that can be solved via a different control strategy?

Since the SystemBuild blocks contain code that users fill in with variables and parameters, the control model can be fed into Integrated Systems' Autocode tool to produce compilable code with modules bearing the names assigned to blocks in the high-level design. The compiled code can then be run on Integrated Systems' AC-100 system, which contains up to 10 80386-based single-board computers, to see how well it really performs. Integrated Systems stops short of modeling an operating system and hardware-execution environment other than its own.

As it becomes clear that the price paid for mistakes discovered late in the design is painfully high, more bridges are built between hardware and software.

■■■

Dealing with dead programmers

One last important task to be considered for CASE is the maintenance of existing code. It's all very well to use CASE tools from scratch and hope to have well-documented, well-commented code that anyone can browse through using structure charts. But most organizations have vast quantities of code that wasn't created in this way. When they move into a CASE discipline, they need a way to document and maintain code consistently with their in-house standards.

Studies show that between 70 and 80 percent of a software operation's activity is devoted to code maintenance. Of that, 50 percent is taken up with trying to figure out what the code does. If ever there was a point where automation could save time and money, this is it.

Reverse engineering of code is something that's beginning to become an integral part of a complete CASE environment. Both Cadre and IDE, for example, have incorporated reverse engineering into their environments. Cadre's C/Rev lets users generate structure charts from C source code to get the big picture of what is going on in the program. Structure charts also let developers navigate through code. By simply clicking on a box representing a module, users can open up that module and view the source code.

IDE's Design generator for C (part of its C Development Environment) will read C source files; generate structure charts and data diagrams; and include the annotation embedded in the code. One of the near-term enhancements planned is to let users step through the source code while watching the structure chart. Users will be able to see the parts of the chart that are currently executing light up or change color. This way, they will be able to follow program execution at the design level.

No single vendor has come up with an environment that can cover all aspects of a computer-based design. As it becomes clear that the price paid for mistakes discovered late in the design is painfully high, more bridges are built between hardware and software. CASE still has a way to go to catch up to the level of hardware CAE, but tools are emerging that serve the real needs of users. And it's the users who will be the final arbiters of how future tools will be shaped. ■

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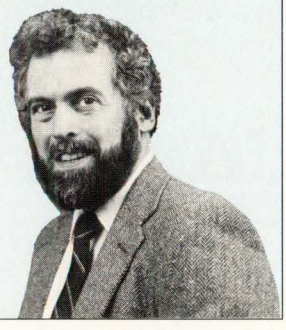
Post Script

In researching the topic of CASE tools, I was struck by the realization that software development is undergoing something of a cultural revolution. There has always been a conflict between engineers and managers—and certainly between engineers and marketers. Perhaps the early efforts at CASE environments actually did fail due to those conflicts. But the inexorably increasing complexity of systems is forcing a truce. Both sides need tools to handle the enormous pressures of system size, design complexity and dwindling time-to-market. To be successful, CASE must accommodate all those needs.

CASE is certainly more than a technology issue. It's also a people issue, where even error messages are sometimes carefully worded to avoid bruising egos. Design documents must be as useful for finding one's way through a mass of code as they are for discussing the issues at hand with coworkers and supervisors. Management must often impose a standard approach to get things done that may not result in the ultimate in efficient code. But the tools can't get in the way of those who use them for the sake of supervision and control. The whole thing has to work together for the people in the organization—or it won't work at all.

Some may regret that a bit of the romance associated with programming may disappear if the admission price for enabling technologies is out of the reach of small groups of innovative programmers. Hopefully, some of the truly impressive CASE tools and their supporting hardware will be more affordable. That will let the small-shop creative spirit survive and continue to contribute to our industry.

Tom Williams



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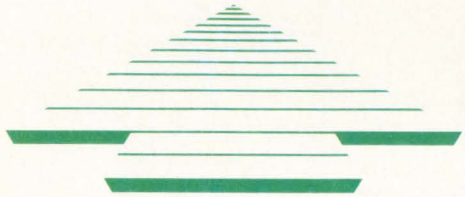
The Official BUSCON/91-EAST Show Guide



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- First is a marketing overview of the bus/board industry written by Warren Andrews. This overview will analyze the often confusing and contradictory data on the size of the board business and projections for its future development and growth.
- The second feature will be New Products, in which the products being introduced at Buscon, or which were introduced to the marketplace since Buscon/91-West, will be highlighted.

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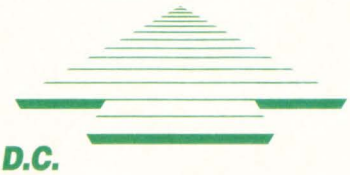

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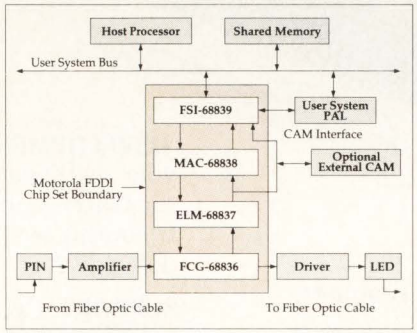

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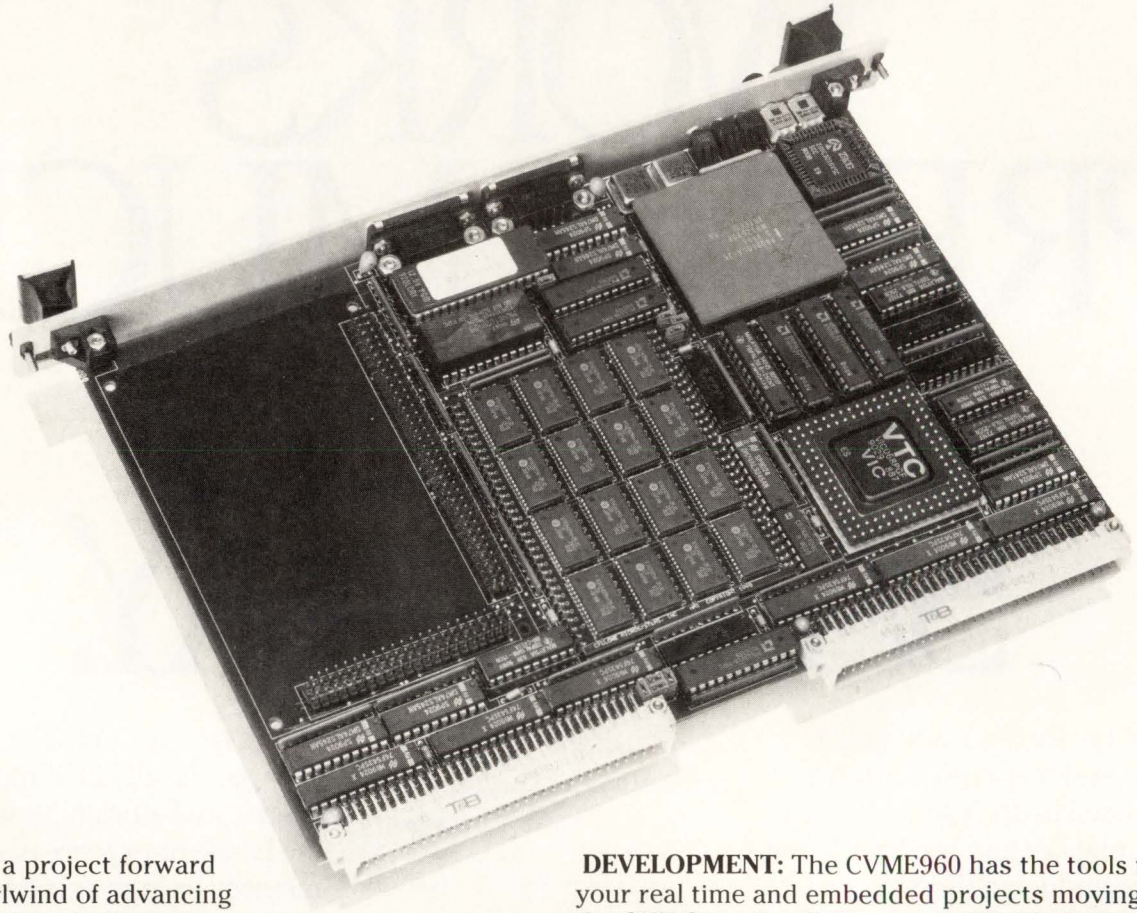

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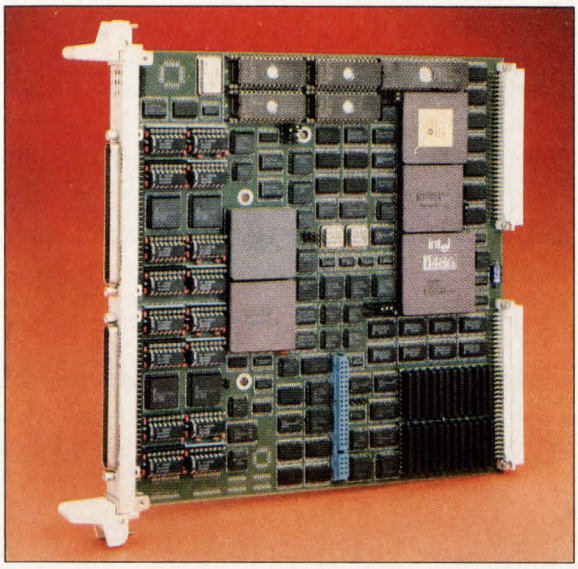
CIRCLE NO. 59

COMPUTERS AND SUBSYSTEMS

Power-packed processors communicate on Multibus II

Jeffrey Child, Associate Editor



Targeted for communications applications, the CC486/258 from Concurrent Technologies features a 25-MHz 486 and eight high-performance full-duplex serial channels. Supported by a 32-bit 82380 DMA controller, the 486 processor has the power to operate at high data rates on all eight channels

Driven by booming opportunities in communications applications and the trend toward distributed processing, Multibus II continues to gain momentum. In response, the number of new Multibus II CPUs has been on the rise in the past year. The current selection of boards for Multibus II CPUs ranges from general-purpose single-board computers to application-specific processor boards targeted for particular system requirements.

To solidify Multibus II's position as a high-performance next-generation bus, board makers are employing innovative architectures aimed at getting the most performance out of today's faster microprocessors. At the same time, they're cramming their boards with a variety of I/O functions. System integrators can now buy a single board to handle the tasks that once required three or four.

Because all Multibus II boards use the same message-passing coprocessor (MPC), users can be certain that any Multibus II board they buy will talk to other Multibus II boards in their system. This influences the type of boards that vendors offer; with such a rigorously defined standard, there's little room for more than a handful of boards that offer the same functions.

"In Multibus II, the vendors tend to be reasonably unique among themselves," says Susan Roll, Multibus II product manager at Intel (Santa Clara, CA). "Each one specializes in specific areas. As a result, users can get a broad range of products from people that specialize in those products."

Intel's strategy will be to focus primarily on CPU boards, says Roll. The company plans to continue evolving its line of CPU boards, and to incorporate the latest enhancements to Multibus II as they become standards.

Through extensive use of surface-mount technology and ASICs, Intel was able to cram a wealth of I/O onto the 486/133E, the company's flagship Multibus II board. Based on the 33-MHz 486, the board offers SCSI and a full Ethernet implementation. Memory includes up to 8 Mbytes of parity-protected fast-page DRAM on the main board. By adding 8-Mbyte modules, a total of 64 Mbytes can be supported.

Ideal for communications

Communications is the applications area where Multibus II is seeing the fastest growth. In fact, the performance and capabilities offered by Multibus II are naturally suited for communications users.

"As far as communications people are concerned, they're moving into what is really a software bus," says Glen Fawcett, president of Concurrent Technologies (Champaign, IL). "In Multibus II, they're completely isolated from all aspects of the hardware. When they want to send a message from one board to another, they just send it to another node, almost as if it were on a network. The message goes down through a seven-layer communication model and across the bus at 40 Mbytes/s. Of course, the communications people love that concept because they're used to working with networks and seven-layer models."

Targeted for use as the main CPU in communications applications, the CC486/258 from Concurrent Technologies is more than a simple 368-to-486 upgrade. Besides the 25-MHz 486, the board provides eight high-performance full-duplex serial channels. Supported by a 32-bit 82380 DMA controller, the 486 processor has the power to operate at high data rates on all eight channels simultaneously. The board supports T1 (2.048-Mbit/s) data-transfer rates, which is useful for connecting to ISDN systems and PABX systems.

Each of the serial channels has full 32-bit DMA for transmitting and receiving. Also important for communications systems is the 486's on-chip numeric coprocessor. "While the 386 is certainly powerful enough to drive those lines, there's little processing capability left to sort or manipulate the data once it's brought in," says Fawcett.

A user may, for example, want the data to come in at 64 kbits/s on seven of the channels, compress it, and use some fancy encoding scheme before sending it out on the eighth channel. Many telecommunications and military systems involve encrypting data, for instance. The added pro-

Model	CPU	CPU clock speed (MHz)	Math coprocessor	SRAM (bytes)	DRAM (bytes)	DMA channels (no. and width)	I/O ports (no. and type)	On-board/inter-board expansion	Price	Comments
ASC Computer Systems 26401 Harper, PO Box 566, St Claire Shores, MI 48080 (313) 882-1133										**Circle 301**
ASC/80386	80386	33	optional	32k	4M	1 32-bit 2 16-bit	2 serial 1 parallel	—	$4,000	—
Central Data 1602 Newton Dr, Champaign, IL 61821 (800) 482-0315										**Circle 302**
CD22/1386	80386	20	80387, Weitek 3167	—	1-16M	4 16-bit	1 RS-232	2 iSBX P2 bus	$3,225 to $3,785	fast-page/interleaved-bank memory design
Centralp Automatismes 16 Rue Gabriel Peri 92120 Montrouge France 33-1-42-53-36-17										**Circle 303**
FAB 086	80286	10	80287	512k	—	1 16-bit	2 serial	iSBX bitbus Ethernet	$4,000	multifunction, CSM, watchdog, battery backed-up clock
FAB 286	80286	8	80287	64k	2M	1 16-bit	4 serial	iSBX	$6,000	special industrial CPU design
FAB 486/860	80486	25	80860	512k	32M	1 32-bit	2 serial	video bus	$16,000	designed for high-end robotics and image processing
Concurrent Technologies 701 Devonshire Dr, Champaign, IL 61820 (217) 356-7004										**Circle 304**
CC 486/258	80486	25	—	—	2-8M	8 or 16 32-bit	8 RS-232/422	iSBX	$5,000	up to 4-Mbyte EPROM
CL 486/296	80486	25	—	—	2-8M	8 32-bit	2 RS-232/422	iSBX	$5,327	Ethernet and Cheapernet interfaces, up to 4-Mbyte EPROM
CC 386/208	80386	20	optional	—	1-4M	8 32-bit	8 RS-232/422	iSBX	$3,100	up to 4-Mbyte EPROM
CC 386/008	80386	16	optional	—	1-4M	8 32-bit	8 RS-232/422	iSBX	$2,726	up to 4-Mbyte EPROM
CL 386/296	80386	20	optional	—	1-4M	8 32-bit	2 RS-232/422	iSBX	$3,325	Ethernet and Cheapernet interfaces, up to 4-Mybte EPROM
CL 386/196	80386	16	optional	—	1-4M	8 32-bit	2 RS-232/422	iSBX	$3,150	same as above
CP 386/016	80386	16	optional	1M	16M	8 32-bit	2 RS-232	cCBX bus	$1,855	up to 4-Mbyte EPROM
CP 186/010	80186	10	—	—	—	2	1 RS-232 sync/async 2 RS-232/422/485 48 digital I/O	iSBX	$906	built-in self-test, debug monitor, software loaders, transport layer firmware
IO 386/16X	80386SX	16, 20	—	512k	1-4M	4 16-bit	1 RS-232 1 RS-232/422 1 bitbus interface 16 digital I/O	iSBX	$2,716	up to 2-Mbyte EPROM, 128-kbyte flash EPROM
Heurikon 8000 Excelsior Dr, Madison, WI 53717 (608) 831-0900										**Circle 305**
HK68/M230	68030	33	68882	—	4-16M	4 32-bit	2 RS-232 1 Ethernet 1 parallel	iSBX iLBX	$6,595	separate DMA for I/O and system bus; supports VxWorks, Velocity, Unix
Intel 5200 NE Elam Young Pkwy, Hillsboro, OR 97124-6497 (503) 696-7786										**Circle 306**
iSBC 486/133SE	80486	33	in CPU	—	1-64M	4 16-bit	1 parallel 2 serial	iSBX CSM002	$8,500	on-board SCSI and Ethernet
iSBC 486/125	80486	25	in CPU	—	1-64M	4 16-bit	2 serial	iSBX CSM002 iLBX II	$6,495	—
iSBC 386/PC16	80386	16	optional	64k	1-16M	4 16-bit	1 parallel 2 serial	ISA bus on P2	$3,900	—
iSBC 386/258	80386	16	optional	—	1-4M	4 16-bit	1 serial	iSBX CSM002	$3,595	available in various SCSI configurations

Model	CPU	CPU clock speed (MHz)	Math coprocessor	SRAM (bytes)	DRAM (bytes)	DMA channels (no. and width)	I/O ports (no. and type)	On-board/inter-board expansion	Price	Comments
Intel 5200 NE Elam Young Pkwy, Hillsboro, OR 97124-6497 (503) 696-7786										**Circle 306**
iSBC 386/133	80386	33	80387	64k	1-64M	4 16-bit	2 serial	iSBX CSM002 iLBX II	$4,995	—
iSBC 386/120	80386	20	80387	64k	1-16M	4 16-bit	1 serial	iSBX	$3,495	—
iSBC 286/100A	80286	8	optional	32k	—	4 16-bit	2 serial 1 parallel	2 iSBX iLBX II	$2,495	on-board SCSI
iSBC 186/100	80186	8	optional	—	512k	4 16-bit	2 serial 1 parallel	iSBX	$1,995	on-board SCSI
MIX 386/020	80386	20	optional	—	1-17M	4 16-bit	1 serial	MIX bus	$2,195	supports one to three MIX modules
Israel Aircraft Industries/MLM PO Box 45, Beer Yaakov 70350, Israel 972-8-272595										**Circle 307**
MAC 386	80386	20	80387	512k	—	2 32-bit 2 16-bit	—	—	$10,000	airborne control, guidance and navigation
MAC 486	80486	25	—	512k	—	4 16-bit	—	—	$10,000	same as above
MBII/1553B Gateway	80186	10	—	128k	—	—	—	—	$8,000	intelligent gateway between MIL-STD-1553 and MBII
Mentec Computer Systems 8399 Green Meadows Dr N, Westerville, OH 43081 (800) 338-2585										**Circle 308**
M860	80860	33, 40	—	256k	8-32M	8 32-bit	1 CSM002 1 serial	PSB	$10,995 to $19,995	supports Unix system V release 4
Microbar Systems 3350 Scott Blvd, Bldg 39, Santa Clara, CA 95054 (408) 748-2920										**Circle 309**
T20FX	68020	16, 20, 25	optional	8-32k	1-16M	4 32-bit	1 RS-232	iSBX FX bus	—	30 in.^{2} of prototype circuit area
T386FX	80386	20, 25	optional	optional	1-16M	8 32-bit	2 RS-232	iSBX FX bus	—	25 in.^{2} of prototype circuit area
Micro Industries 8399 Green Meadows Dr N, Westerville, OH 43081-9486 (800) 446-6762										**Circle 310**
MIBII 386/110	80386	25	80387	4M	—	8	—	OME	$3,450	32-kbyte cache
MIBII 960/110	80960CA	33	—	64k	1M	4	UART, timer	OME	$2,950	—
MIBII 386/120	80386	16	80387	—	2M	8	1 keyboard 1 printer	—	$3,950	MS-DOS compatible PC/AT at P2
RADA Electronic Industries 1950 W Corporate Way, Anaheim, CA 92801 (714) 535-7353										**Circle 311**
RCP 382	80386	16, 20	80387	500k	—	8	1 MIL-STD-1553 4 RS-232/422	32-bit local bus	—	MIL standard board, 500k EPROM, 19 interrupts, on-board monitor
Siemens AG Gleiwitzer Str 555, 8500 Nurnberg-Moorenbrunn,Germany 0911-895-4395										**Circle 312**
OSM-B37-Axx	80386	20	80387 WTL1167	64k	2-8M	4	3 RS-232 1 SCSI	OME	$4,500 to $6,200	SM on board, 3 counters/timers
OSM-B35-L25	80386	25	80387	—	2-8M	7	1 serial	AT bus (AT96)	$4,100 to $6,350	DOS-compatible with OSM-L356 peripheral controller
OSM-B17	80186	8	8087	—	1M	6 16-bit	3 RS-232 1 Centronics 1 SCSI	OME	$2,450	RTC, 3 counters/timers, monitor
SBC 1	80960	16	80960	—	4-16M	2	1 RS-232 1 X.21	DX bus module-interface	$6,550 to $14,400	—

Model	CPU	CPU clock speed (MHz)	Math coprocessor	SRAM (bytes)	DRAM (bytes)	DMA channels (no. and width)	I/O ports (no. and type)	On-board/inter-board expansion	Price	Comments
Tadpole Technology 8310 Capital of Texas Hwy N, Suite 375, Austin, TX 78731 (512) 338-4221 **Circle 313**										
TP33M	68030	16, 33	68881/2	—	4-16M	3 32-bit	1 SCSI 1 Ethernet 6 RS-232 8 bits user I/O	iLBX II iSBX iPSB	$4,200 to $14,800	2-kbyte nonvolatile SRAM, supports Unix, VxWorks, VRTX-32
TP884M	88100	24	in CPU	—	8-32M	8 32-bit	1 SCSI 1 Cheapernet 2 V24 ports	iLBX II iPSB	$15,000 to $21,000	error detection/correction, parity checking, 512-kbyte flash EPROM
TP860M	80860	33, 40	in CPU	—	4-16M	8 32-bit1	1 SCSI 1 Ethernet 3 RS-232 1 keyboard	iSBX iPSB	$10,000 to $14,000	—

cessing muscle of the numeric coprocessors comes in handy in such cases, says Fawcett.

Concurrent Technologies' board also offers either 2 or 8 Mbytes of DRAM, up to 4 Mbytes of EPROM, an iSBX interface for system expansion, and a watchdog timer.

Also featured on the CC486/258 is an on-board Central Services Module (CSM). In Multibus II, when a system powers up, different arbitration levels are attached to each board. The CSM assigns bus-arbitration priorities to each board. While the circuitry supporting this function is normally on a separate board or built into the backplane, the CC486/258 has the CSM built into the board.

With few exceptions, the Multibus II CPU boards available today are based on leading Intel 80X86 processors. This contrasts with the trend

in VME, where boards based on processors outside the Motorola 680X0 family are becoming more common. The main reason behind this is the broader range of performance levels addressed by VME systems, which demands a wider range of processor types. The higher sophistication and cost of Multibus II tends to relegate its use to complex systems that require multiple processors.

As the tables on the previous pages indicate, nearly all Multibus II CPUs are based on the 386 and 486. The exceptions are a handful of boards—including a pair of interesting RISC-based boards.

RISC performance on Multibus II

When Mentec (Dublin, Ireland) set out to design its M860 board, performance was given top priority. The M860 is based on Intel's 860 RISC processor. With support for Unix System V release 4, the board fills a niche as a high-performance Unix engine on Multibus II. Delivering up to 40 Mips at 40 MHz and offering a peak transfer rate of 40 Mbytes/s over the bus, the M860 is the fastest Multibus II CPU board available today.

Although the current version sports a 40-MHz 860, the board was designed for 50-MHz operation. Designers at Mentec found this to be quite a challenge. "The 50-MHz speed pushes the limit as far as board-level activity," says Chris Fairclough, managing director at Mentec. "It took a few iterations of the layout to get everything stable." The basic design will be used to support faster processors as they become available.

Key to the board's performance is the 64-bit 860 processor containing integer, floating-point and graphics units. The chip's 64-bit external data bus, 4 kbytes of instruction cache and 8 kbytes of data cache add to its performance. Other key elements of the board design are a fast I/O buffer and a memory architecture built to take advantage of the 860's high-performance features.

The M860's memory system limits the number of clock cycles between memory accesses. Consisting of either 8 or 32 Mbytes of static-column-mode DRAM, the memory system makes use of the 860's pipelined bus, and address and data latches to hide DRAM latency during most accesses. The first access to main memory requires five clock cycles, but all subsequent accesses have zero wait states.

The M860, when used to let the 860 processor buffer transfers to and from the Multibus II's Parallel System Bus (PSB), provides an I/O buffer area made up of 256 kbytes of 25-ns SRAM. When a data transfer is required to or from a device on the PSB, the 860 programs the MPC and the DMA controllers with the appropriate parameters for the transfer. The transfer then occurs under the complete control of these two devices. The SRAM acts a buffer during the transfer. Consequently, the 860 can run programs out of main memory while data moves between the SRAM buffer and the bus.

Another RISC-based Multibus II board, the TP884M from Tadpole Technology (Austin, TX), uses the Motorola 88000 chip set. Delivering

up to 21 Mips and 4.2 MFlops at 25 MHz, the 88100 CPU and its two associated 88200 CMMUs (cache MMUs) are carried on a low-profile plug-in mezzanine module. The design takes advantage of the special features of the 88000 to ensure data integrity; it implements a second module that contains another 88100 and two more CMMUs. This second processor operates in lock-step mode with the main CPU. Both CPUs run the same instructions. But the second 88000 doesn't drive any bus signals; instead, it compares its internal state with the external state of the main CPU and produces an error if a discrepancy occurs.

Another aspect of the TP884M geared toward ensuring data integrity is its 8- or 32-Mbyte error detection and correction-protected DRAM. The EDC circuitry automatically corrects single-bit errors and detects multi-bit errors. The CPU can snoop accesses to DRAM, thus ensuring cache coherency in multiprocessor applications. The DRAM is carried on a plug-in module and is dual-banked for fast burst transfers to boost performance.

The board also features a variety of I/O, including a full IEEE 802.3 Cheapernet interface. Two independent serial I/O interfaces and a SCSI interface are also provided.

System designers now involved in 680X0-based applications may be reluctant to migrate to Multibus II. The HK68/M230 from Heurikon (Madison, WI) addresses this concern. Based on the 68030, the board lets system designers migrate to Multibus II without abandoning their software investment in 680X0-based applications. The board supports Unix System V release 3, VxWorks and the VRTX32 real-time kernel.

Working concurrently with the board's CPU, an AT&T WE32204 processor controls data transfers between memory locations and between memory and peripherals. Memory on the board includes 4 or 16 Mbytes of DRAM. A buffered Ethernet controller and a SCSI are included on the board as well.

Opinions vary about the future of Multibus II. Some feel that efforts to reduce the costs of Multibus II boards are too little, too late, to influence users already comfortable with other high-performance buses such as VME. Others perceive Multibus II as the leading next-generation bus. They point out that many of the features defined for Futurebus+ are already available in Multibus II. "Capabilities that Multibus II doesn't have yet, such as cache-coherency for closely coupled multiprocessing, will be implemented in silicon soon," says Mentec's Fairclough. "So by the time Futurebus+ becomes widely available, it won't be all that useful." ■

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CIRCLE NO. 63

COMPUTERS AND SUBSYSTEMS

Multimedia comes to a PC near you

Although digital signal processors seem a natural fit for multimedia applications in the PC world, few vendors have been bold enough to place a DSP chip directly on a PC motherboard. Enter the DSP/PC single-board computer from Spectrum Signal Processing. Designed to operate in a passive backplane, the DSP/PC integrates a 25-MHz 386DX AT design with a 33-MHz TMS320C31 DSP from Texas Instruments on a full-size PC/AT plug-in card.

On the DSP/PC, the 386DX processor is supplied with 2 Mbytes of one-wait-state page-interleaved memory. Included is a socket for an optional 80387 or Weitek math coprocessor. Up to seven storage devices can be connected to the SCSI hard disk interface; the SCSI host can be accessed by either the PC/AT or the DSP system. The DSP chip is supplied with 64 kwords of zero-wait-state SRAM that can be expanded to 512 kwords.

Key to the performance of the dual-processor approach is a 66-Mbyte/s bus the company calls Media-Link. In the AT board design, the 80386 and the TMS-320C31 are connected using this bus. Media-Link lets the DSP chip directly access the AT memory and peripheral devices, such as video frame grabbers. Similarly, the 80386 can directly access the DSP memory, as well as devices such as analog I/O, connected through another 10-Mbyte/s called DSP-link.

The Media-Link bus is built around a custom chip developed by Spectrum. This Media-Link Controller (MLC), the SSP42C100, is a two-port device, with one side connected to a processor and the other to the Media-Link bus. Both processors in the system are interfaced in this manner, with Media-Link providing the common gateway.

When a data transfer is to occur, the originating processor sets up a description block with the parameters of the data to be sent, including the destination processor, a pointer to the data, and the length of the data block. Upon invocation of the MLC, the data is transferred via DMA to the destination processor. The destination MLC notifies the destination processor that data has been received, as well as its origin, location and length.

On the software front, two libraries of interface routines are provided to help with processor-to-processor communications. One, which is designed to execute on the 80386, is Microsoft C-compatible. The other, which is designed to execute on the 320C31, is compatible with TI's DSP software-development tools. In addition, a Microsoft Windows DSP driver will be developed to support third-party applications program development.

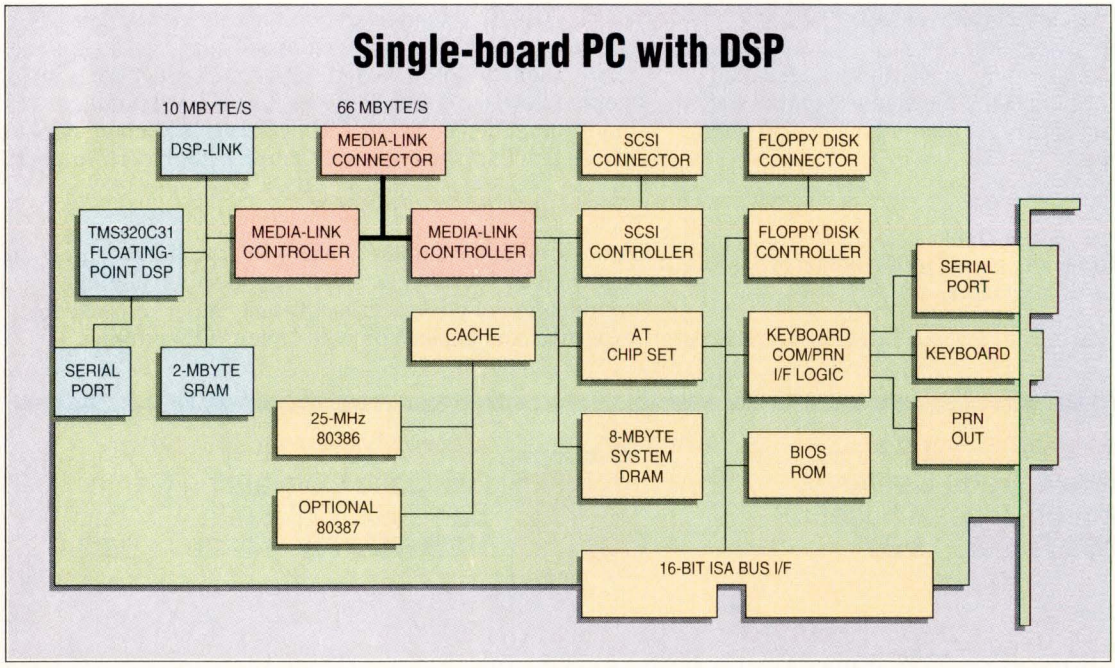
The Media-Link single-board computer will be available in 1Q92 at $3,500 in quantities of 25 to 50. The MLC will be available separately in 3Q91. — *Dave Wilson*

DSP/PC SBC at a glance:

- Full-size 386 PC AT card with TMS320C31 digital signal processing chip
- Media-Link controller for multiprocessor communication
- 66-Mbyte/s sustained data-rate transfer
- Software interface library routines

Spectrum Signal Processing
3700 Gilmore Way, Suite 301
Burnaby, British Columbia V5G 4M1
(604) 438-7266

Circle 351



The DSP/PC board is a fully compatible 386DX AT design augmented with a TMS320C31 digital signal processor. A 66-Mbyte/s bus called Media-Link provides the connection between the two processors.

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Since microprocessor and bus architectures play a major role in determining the performance and functionality of OEM systems, these will also get attention, with an emphasis on how they impact the selection of other major system components. In addition to this feature, a New Products section will highlight products being introduced at, or prior to, SysComp.

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PUBLISHER: David L. Allen, 508-392-2111 • ASSOCIATE PUBLISHER Tim L. Tobeck, 508-392-2116• NATIONAL ACCOUNTS MANAGERS: • WESTFORD, MA, Tim Pritchard, 508-392-2217 • SPRING, TX, Eric Jeter, 713-353-0309 • SAN JOSE, CA, Diane Palermo, 408-292-6837 • STRATEGIC ACCOUNTS REPRESENTATIVE: • WESTFORD, MA, Sue Nawoichik, 508-392-2118 • INTERNATIONAL SALES OFFICES: • SURREY, ENGLAND, David Round, 81-686-7655 • PARIS, FRANCE, Daniel R. Bernard, 1-39-14-6780 • MUNICH, GERMANY, Johann Bylek, 089-903-8806 • MILAN, ITALY, Luigi Rancati, 02-70-30-0088 • TOKYO, JAPAN, Toshio Equsa, 81-33-536-5404 • ASIA, AUSTRALIA, NEW ZEALAND, TOM GORMAN, 852-833-2181

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COMPUTERS & SUBSYSTEMS

Multiprocessor board boosts embedded designs to gigaflop range

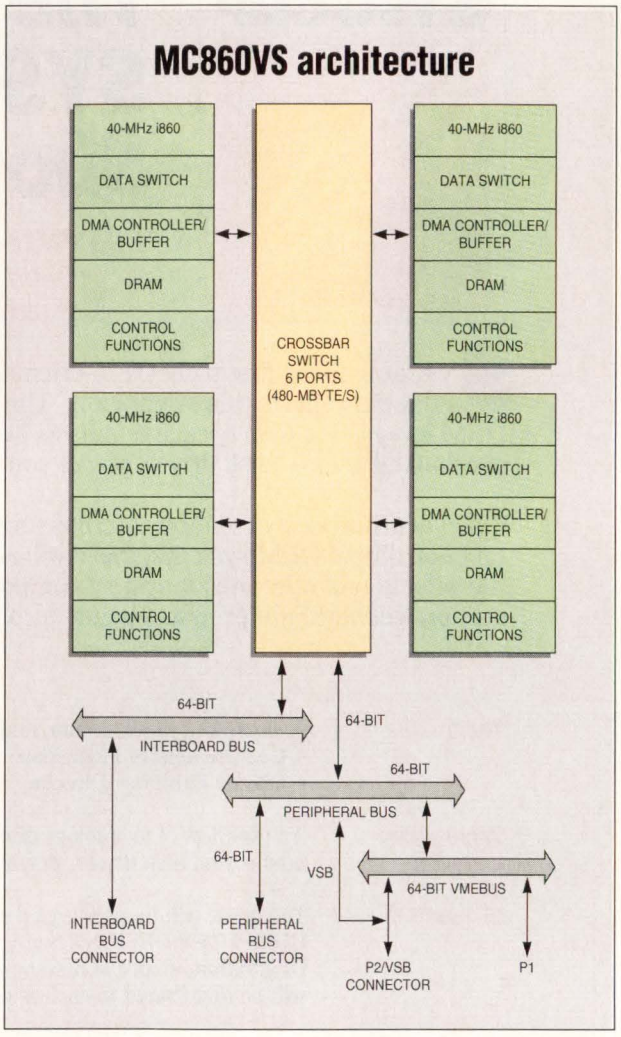
Gigaflop performance in a VME card cage is now possible thanks to a board-level multiprocessor design from Mercury Computer Systems. The MC860VS single-board computer can be configured with up to four Intel i860 processors using modular nodes on a 9U VME card. Each four-processor card can run at up to 320 MFlops. Up to eight MC860VS boards can be configured on a VMEbus in a snugly coupled processing environment. The 32 i860s of this maximum configuration provide a total processing potential of 2.5 GFlops.

Interprocessor communication is supported with shared memory or message passing. Fifteen of the MC860VS' 35 ASICs are used to implement a 480-Mbyte/s crossbar switch that lets three full-speed memory references take place between i860s on the same board at 98 percent of the rate of accessing local on-board memory. A 160-Mbyte/s interboard bus connects between each board's crossbar switch and allows direct i860 communication between boards. Thus, memory can be shared among all processors in a multiboard system at the 160-Mbyte/s transfer rate.

Three types of I/O

The MC860VS provides three kinds of I/O. First, the VME64 interface allows 70-Mbyte/s transfers over the VMEbus. Second, a VME subsystem bus (VSB) interface allows connection of standard VSB devices, such as CPUs and frame grabbers, using the P2 connector and permits a peak transfer rate of 35 Mbytes/s. Third, an open peripheral bus provides a 160-Mbyte/s peak block-transfer rate for tightly coupled peripherals. The MC860VS can be equipped with up to four DMA devices, which are part of the board's large complement of ASICs, to decouple slow devices from the board's memory system and to reduce memory contention by automatically buffering data. To aid the operating system's multitasking, the MC860VS dedicates a separate interrupt controller and clock/timer for each processor.,

The software en-



vironment of the MC860VS is a multiprocessing, pre-emptive multitasking operating system called MC/OS, which currently includes features of Posix and is evolving toward full Posix compliance. Part of MC/OS is MC ICS, the interprocessor-communication system that can support both shared-memory and message-passing mechanisms on the MC860VS architecture. It provides sockets for message passing and semaphores for synchronization. Sockets, semaphores and shared memory operate in a global name environment that's independent of the processor, so that processes can migrate from one processor to another without modification. In addition, the combination of software and hardware modularity makes systems based on the MC860VS easily scalable from a single i860 configuration up to a full 32-processor eight-board system.

Mercury also provides ANSI C and Fortran 77 compilers for support of X Windows, a library of over 450 routines, an editor, a compiler and debugger, and a profiler. The profiler is potentially the most useful tool for implementing multiprocessor systems since it can monitor which tasks are executed most often and show which processors are busy.

The MC860VS with four processors is priced at OEM discounts from $24,300 to $38,300, depending on memory and other configuration details. A 16-processor system with 16 Mbytes of memory on board running at 1.2 GFlops costs around $106,000. — *Tom Williams*

The MV860VS at a glance

- One to four Intel i860s
- 2 to 64 Mbytes
- 9U VME form factor
- 160-Mbytes/s interboard bus, one DMA controller for each processor, 64-bit data paths connecting all elements
- system software: multitasking operating system/executive
- C and Fortran compilers, debugger, and profiler
- Up to 320 MFlops in a single slot, 2.5 GFlops in an eight-board system
- VME, VME subsystem bus and open peripheral bus

Mercury Computer Systems
600 Suffolk St
Lowell, MA 01854
(508) 458-3100

Circle 360

CAE/CAD TOOLS

Design tool targets multichip modules

Multichip modules (MCMs) present engineers with some thorny design problems. Although at first glance an MCM can look like a tiny printed circuit board, the proximity of closely spaced traces and components on a substrate introduces crosstalk and transmission line problems that only a sophisticated design tool can address.

An MCM's small size also is misleading. Typically, an MCM can host more layers, traces and vias than a much larger printed circuit board. The thickness of an MCM substrate ranges from 4 to 30 layers, unlike printed circuit boards, which rarely have more than 8 layers. Die I/O signals number from hundreds at the low end of MCM technology to thousands at the high end of the design spectrum. In addition, track width and spacing within the substrate vary from 5 mil to 8μm. Printed circuit board traces, on the other hand, can only be as small as 3 mil. Also, an MCM can have as many as 15,000 interconnects.

With MCM Station, Mentor Graphics is the latest CAE vendor to tackle the complicated design problems of MCMs. The tool supports the design process from electronic design through placement and routing, thermal and electrical analysis, and interfacing with manufacturing. It lets users judge the performance of their designs before committing to tooling or hard inventory. By examining substrate and chip junction temperatures in software, engineers can insert thermal vias or modify parts placement as needed to rectify potential problems before manufacturing.

MCM Station contains a comprehensive rules-driven layout and routing package, as well as the thermal-analysis capabilities of AutoTherm, a finite element-based tool for static and dynamic modeling of heat flow and dissipation. The tool also incorporates software to analyze high-speed signal delay, electrical crosstalk and transmission line effects. These analysis tools from Quad Design Technology are integrated into MCM Station and may be invoked before and after device routing to avoid parasitics and to maximize reliability. MCM Station also offers capabilities for full compliance with military documentation standards.

MCM Station accepts chip and ASIC designs from various sources, including Mentor's Design Architect, a front-end schematic-capture toolset. The MCM portions of the design may be simulated using one or more of Mentor's digital- and

analog-simulation tools. Other Mentor tools, such as QuickFault, QuickGrade and QuickPath, also can be called up for test development and critical path analysis. Also included are tools to transfer a completed MCM design to the manufacturing environment via common file formats, such as GDSII and Gerber artwork outputs. Standard drill and milling formats also are supported.

MCM Station is available now on HP/Apollo platforms and will be ported to Sun Sparcstations in the second half of 1991. Pricing begins at $128,900 for the physical-layout, thermal-analysis and signal integrity package. *— Mike Donlin*

Mentor Graphics
8005 SW Boeckman Rd
Wilsonville, OR 97070
(503) 685-7000

Circle 357

MCM Station at a glance

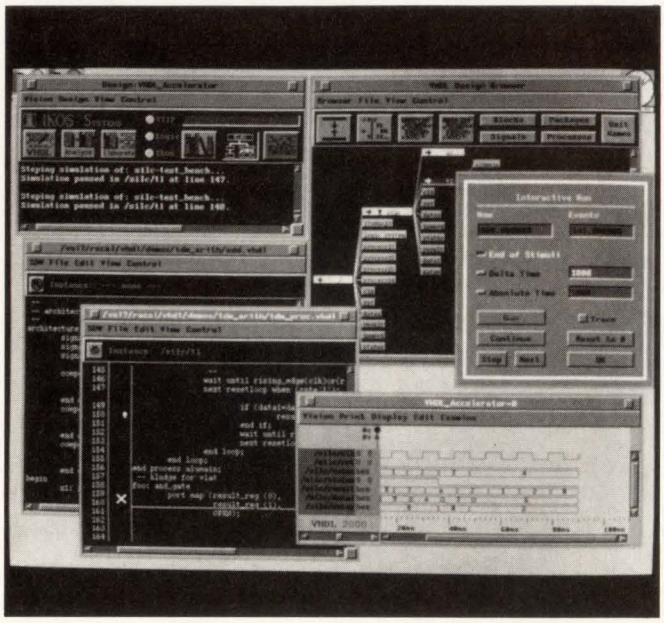
- Product: a software tool for the design of multichip modules
- Contains comprehensive rules-driven layout and routing capabilities
- Provides thermal analysis of substrate and chip junction temperatures
- Features high-speed signal-delay, electrical-crosstalk and transmission line effects-analysis capabilities
- Mil-spec documentation compliance
- Availability: immediate on HP/Apollo platforms; second half of 1991 on Sun Sparcstations
- Price: $128,900

CAE/CAD TOOLS

Hardware accelerator boosts VHDL simulation speeds

True top-down design requires that a system be simulated before any significant investment is made in detailed design. Ideally, a top-down approach will let an engineer design and test an architecture before making decisions about specific hardware considerations, such as bus width or silicon technology. Hardware description languages make such design and simulation possible, but the very flexibility that these languages offer places tremendous strain on simulation tools. Ikos Systems and Racal-Redac have teamed up to develop what they hope will be an answer to this dilemma with the VHDL Accelerator.

According to Ikos, the VHDL Accelerator can simulate a design module with 1,000 lines of VHDL code 20 to 50× faster than can software simulators running on a 28.5-Mips Sparcstation 2. Relative performance is even greater for larger system simulations—up to 100× faster for 5,000 lines of code and 1,000× faster for 50,000 lines.



The "dashboard" of the VHDL Accelerator (upper left window) shows controls the main functions of the simulation session. The source display windows (two windows in the lower left) let users monitor the concurrent processes in the simulation. The design browser (upper right window) provides either a graphical or textual representation of the elaborated design.

The practical capacity of workstation-based software simulators is about 10,000 lines of VHDL code (equivalent to about 100,000 gates of logic). On a design of this size, the simulation time becomes almost infinite for even a small number of simulation time steps. The Ikos accelerator's capacity exceeds 100,000 lines of VHDL source code. Parallel processing keeps the simulation performance practically independent from the design complexity.

Best from both worlds

The accelerator is being developed under the terms of a broad technology exchange between Ikos and Racal-Redac that combines Ikos' hardware-assisted mixed-level simulation technology with Racal's simulation, synthesis and object-oriented framework technology.

Racal-Redac's Vision framework gives the tool an object-oriented user interface with the look and feel of a conventional software-based simulator. Designers can step through the simulation, set breakpoints on statements or variables, trace and display variables, and perform other source-level debug functions using this interface. Users also can edit

the original source file from within the accelerator environment and incrementally compile the changes.

Designs simulated with the VHDL Accelerator can be automatically synthesized by Racal-Redac's SilcSyn system, providing a rapid path to silicon. The VHDL Accelerator uses SilcSyn to compile code into a data-flow network, using elements such as ALUs, multiplexers, registers, and incrementers. SilcSyn performs the same function as the code generator in a software simulator. A VHDL code generator produces executable C code, as well as a cross-reference file that makes source-level debugging possible.

VHDL Accelerator at a glance:

- Simulates 1,000 lines of VHDL code 20 to 50× faster than workstation-based simulators
- Larger-system simulations run up to 500× faster than they do on workstation-based simulators
- Capacity exceeds 100,000 lines of code
- Graphical user interface
- Resulting VHDL code is compatible with Racal-Redac's SilcSyn synthesis product

The real innovation here, according to Ikos, is that the accelerator can provide cross-reference data. Instead of mapping from statement to statement, the tool maps statements into events. Likewise, instead of mapping variables into variables, it maps variables into registers.

The VHDL Accelerator will be available 4Q91, with prices starting at $59,500. — *Mike Donlin*

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INTEGRATED CIRCUITS

Microcontroller series fills performance gap between 8- and 16-bit parts

Migrating a cost-sensitive microcontroller-based design from 8 to 16 bits can be an agonizing decision. The primary obstacle is the large price/performance gap between today's 8- and 16-bit parts. Hitachi has attempted to partially bridge this gap with its H8/300 series of high-performance 8-bit microcontrollers. Not intended to rival full-blown 16-bit microcontrollers, the H8/300 series is designed to meet requirements that go beyond traditional 8-bit needs.

Hitachi designed the devices to meet midrange needs. Running at clock frequencies as high as 10 MHz and cycle times of 0.2-μs, the H8/300 microcontrollers are two to three times faster than most other 8-bit controllers.

All the microcontrollers in the series are built around the same CPU core with a general register architecture. While chips' ALUs are 8 bits wide, their internal data paths are 16 bits wide. The devices implement a useful innovation in their memory architecture, with a data path that is organized as two 8-bit halves. This architecture lets users employ either eight 16-bit registers or sixteen 8-bit registers.

If external expansion is needed, the 8-bit external bus is implemented in a way that will be familiar to designers who have worked with other 8-bit controllers. The H8/300 microcontrollers can interface directly with any 68xx peripherals.

RISC-like features

Although a true CISC device, the H8/300 CPU core has several RISC-like features. The basic operations of the microcontroller are from register-to-register, instead of accumulator-based. The large number of registers on the chip also lends itself to high-level language use. All registers can act as accumulators. The CPU offers 54 instructions, including multiply and divide. And because embedded applications often involve a lot of bit processing or bit testing, a set of bit manipulation instructions have been included.

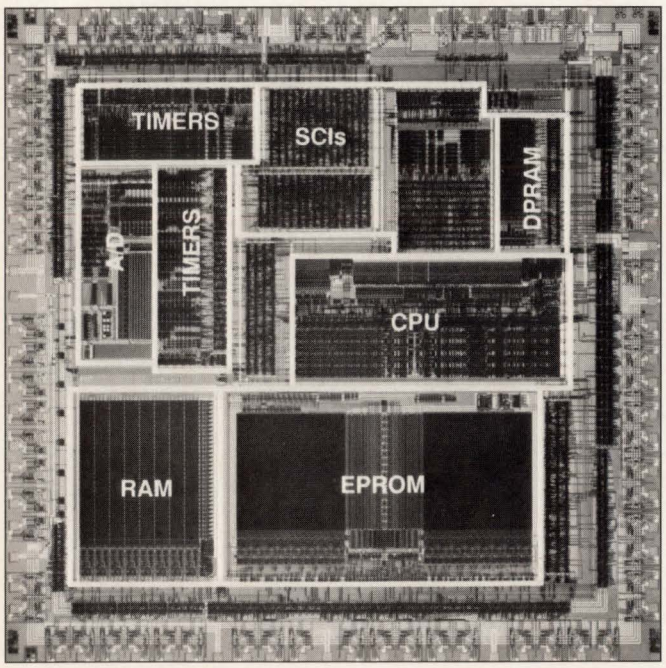
The first available member of the series, the H8/330, is specifically targeted for high-end real-time control applications. The chip provides five timers, a full-duplex serial communication interface, nine I/O ports and an 8-channel×8-bit analog-to-digital converter with sample and hold.

With 16 kbytes of EPROM on chip, the part has adequate memory for storing programs written in high-level languages. Volatile memory on the H8/330 includes 512 bytes of RAM and 15 bytes of dual-port RAM.

With the H8/300 family, Hitachi offers one-time-programmable memory with Hitachi's so called Zero-Turn-Around-Time (ZTAT) feature. The ZTAT feature lets designers program the device's on-chip memory in the same way as any conventional EPROM. For quantities from 5,000 to 10,000 units, the ZTAT OTPs are more cost-effective than masked-ROM versions of the same microcontroller.

H8/300 at a glance

- 8-bit, 10-MHz microcontrollers
- Direct interface to any 68xx peripherals
- 16 kbytes EPROM
- 512 kbytes RAM, 15 bytes dual-port RAM
- Register-to-register operations
- 2-3x faster than other 8-bit controllers



In addition to its compactly arranged, 8-bit CPU core, the H8/330 microcontroller integrates 16 kbytes of EPROM, 512 bytes of RAM, 15 bytes of dual-port RAM, an 8-bit analog-to-digital converter, and a full-duplex serial communications interface.

Development support for H8/300 series includes a broad range of software and hardware tools, available from Hitachi and from third-party vendors. Tools include real-time kernels, assemblers, C compilers, and software simulator/debuggers. An evaluation board and third-party in-circuit emulators are available. And the H8/300 devices are the first microcontrollers supported by a fuzzy logic compiler.

Available now, the ZTAT H8/330s are priced at $17.45 each (100s). This price is said to be representative of the entire H8/300 series. A mask ROM version costs under $10 at high volumes. Package types available for the part include an 80-pin QFP, an 84-pin windowed LCC and an 84-pin PLCC.

—Jeffrey Child

Hitachi America
2000 Sierra Point Pkwy
Brisbane, CA 94005
(800) 448-2244

Circle 355

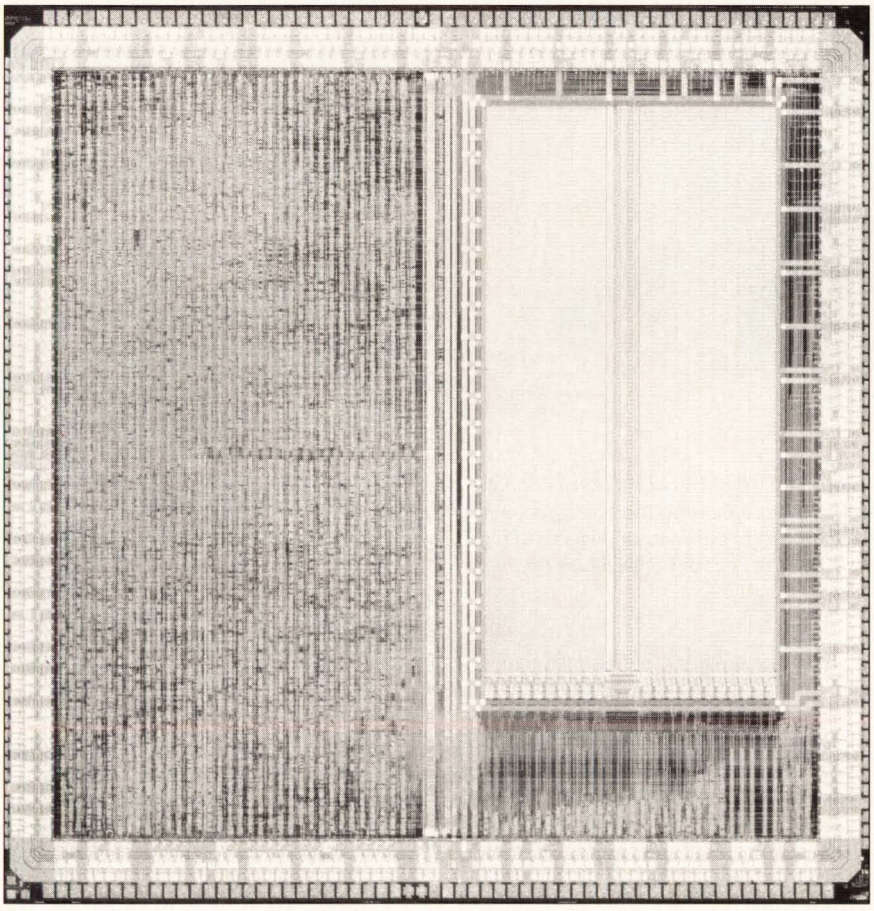
INTEGRATED CIRCUITS

Submicron arrays let users embed up to 256 kbits of SRAM

The LSI Logic 0.7-mm CMOS LEA200K Embedded Array Series, with 13 masterslice sizes, offers up to 307,500 available gates and 215,250 usable random gates. Users can embed cell-based single- and multiport fully diffused RAMs (up to 256 kbits), ROMs, CAMs and FIFOs anywhere within the core of the arrays.

LSI claims that the new LEA200K arrays offer 60 percent greater integration and 25 to 30 percent better performance than its first-generation LEA100K embedded arrays. The new devices target applications requiring up to 7× the memory integration of the LSI 0.7-μm LCA200K Compacted Array Turbo Series of gate arrays, on which users can compile metallized memories.

"Because the base array is manufacturable while the design is being finalized, the customer receives the best of both worlds: the design-optimization capability of customized cell-based technology and the reduced turnaround time of the Compacted Array devices," says LSI senior vice-president Robert Blair. If the design is targeted for multiple applications, an embedded masterslice can be optimized for each application by modifying the gate array logic. Both two-layer metal for I/O-limited designs and three-layer metal interconnect schemes are available. The two-layer metal prototype turnaround of six weeks is expected to decrease to three weeks in a few months. The three-layer metal turnaround time is expected to be five weeks by the end of the year.



This member of the LEA200K Embedded Array Series includes fully diffused, high-density RAM along with random logic.

In addition to high-density memory integration and quick turnaround, the embedded arrays offer a phase-locked loop, which minimizes system skew by compensating for clock trunk ramp time, process effects and chip clock skew. The arrays also have 70-Mbit/s backplane transceivers to improve I/O performance and reduce noise. For low-power applications, a 3.3-V power supply option is available.

Enhanced-modeling scheme

Designers of the LEA200K can take advantage of the Concurrent Modular Design Environment's enhanced-modeling scheme, which incorporates the nonlinear characteristics of submicron device features to increase simulation accuracy. Modeling techniques include consideration of cell input switching threshold voltage, iterative calculation of input ramp time due to loading, and piece-wise linear modeling of cell output resistance and intrinsic delay. The LEA200K cell library includes more than 400 macrocells and 300 macrofunctions, as well as more than 300 Intel, Motorola, AMD, MIPS, Sparc, and LSI Logic megafunctions. Initial third-party library support is included on Synopsys and Verilog.

LEA200K at a glance:

- 0.7-μm drawn channel-length CMOS with up to 307,500 available gates and 215,250 usable random gates
- 13 masterslice sizes
- More than 256 kbits of embedded SRAM

The LEA200K devices support Joint Test Action Group boundary-scan techniques. Packaging options include ceramic or plastic PGAs, ceramic or plastic LCCs, plastic and metal QFPs, and chip on tape. Prototypes will begin shipping in mid-September. *— Barbara Tuck*

LSI Logic
1551 McCarthy Blvd
Milpitas, CA 95035
(800) 451-2742

Circle 356

INTEGRATED CIRCUITS

Fast, high-density PLDs offer on-board reprogramming

Designers hunting for high density and performance in a programmable logic device may find what they're looking for in the pLSI and ispLSI, two high-density PLD families from Lattice Semiconductor. Delivering 70-MHz system speed, the devices combine the high performance and ease of use of PLDs with the density and flexibility advantages of field-programmable gate arrays. And the ispLSI family are the first high-density PLDs to offer nonvolatile, in-system programming.

There are eight devices in the pLSI and ispLSI families, four of which offer Lattice's proprietary in-system programming (isp) technology. System performance of 70 MHz is achieved with a total delay, from input to output, of 15 ns.

Except for a few inputs on the ispLSI devices (for controlling the isp function), the pLSI and ispLSI have the same internal arrangement. Their architecture consists of multiple generic logic blocks (GLBs), each of which implements 90 percent of all 4-bit MSI functions. A proprietary routing network provides global interconnect, 100 percent routability and over 80 percent device utilization. Devices range in pin count from 44 to 120 (with 32 to 104 I/Os). The equivalent PLD gate counts of the series range from 2,000 to 8,000 gates, according to Lattice.

Interconnect routing

At the heart of the pLSI's architecture is an interconnect routing method, which is handled by a global routing pool (GRP). The GRP is responsible for data transfers from either the inputs or the I/O of the device to a GLB, or from one GLB to another.

Key to overall device performance, the GRP takes only a few nanoseconds to perform such transactions. Unlike other routing structures, the GRP has a brief, predictable delay time. This delay, when added to a logic block's delay, results in a fixed total delay of 15 ns. This level of predictability isn't possible in FPGAs, where delay times are often dependent upon the location of the GLB.

The advantage of a predictable transaction speed between logic blocks is twofold. First, knowing the delay times ahead of time reduces the need for testing at every design iteration and, therefore, improves time-to-market. Second, the task of optimizing the speed paths in the design is less complex. With a set delay of 15 ns, it's easier for the simulation software to compile a design. Designers won't have to wait as long while their logic compilers crunch through their place-and-route schemes, optimizing high-speed paths.

pLSI and ispLSI at a glance

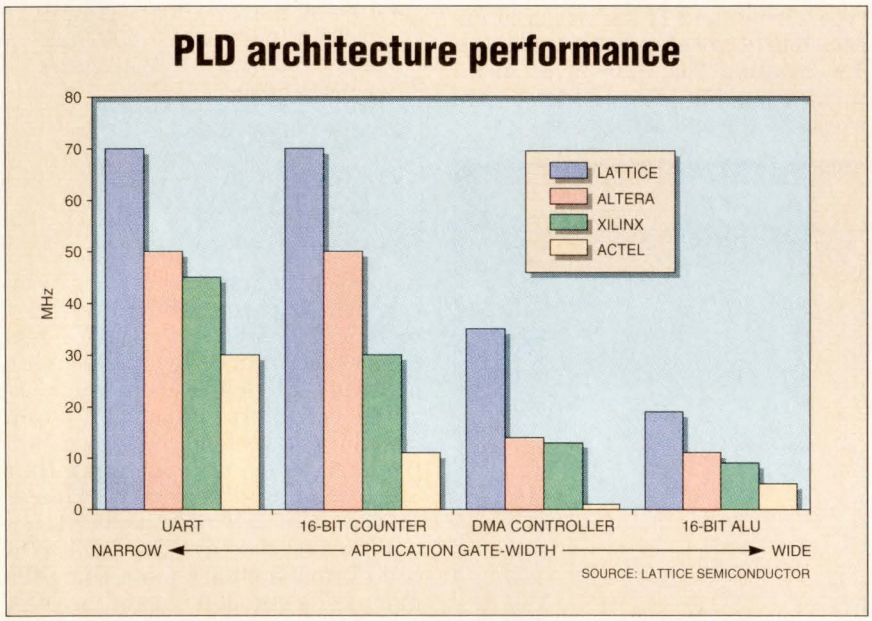
- First in-system programmable PLDs
- 15-ns input-to-output delay
- 2,000 to 8,000 equivalent PLD gates
- Multiple generic logic block architecture

On-board reprogramming

While otherwise identical to the pLSI devices, the ispLSI devices are the first electrically erasable and in-system programmable PLDs on the market. These features let the devices be programmed, reprogrammed, or reconfigured for test without being removed from the circuit board. They also let system designers perform real-time prototyping and debug. And they aid end users by letting the products they own be reconfigured or upgraded on the spot.

Through mode control, four of the dedicated inputs on the ispLSI can be turned into in-system programmable functions. Using only TTL-level programming inputs, the functions can be programmed, reprogrammed or erased, even when the device is installed on a board or multichip module.

Users can program part of the device or the whole device at once. The danger of accidentally repro-



According to tests conducted by Lattice Semiconductor, the new pLSI and ispLSI high-density PLD families operate at 70 MHz in narrow-gate logic functions, such as UARTs (universal asynchronous receiver/transmitters) and 16-bit counters. In wide-gate logic structures, such as DMA controllers and 16-bit ALUs, the Lattice architecture remains above 20 MHz.

INTEGRATED CIRCUITS

gramming the device is small because accessing those pins essentially requires state-machine programming. This provides a sufficiently complex combination lock to make accidental reprogramming unlikely.

Software support for the pLSI families consists of entry-level and advanced software packages. The entry-level package, which runs on PC compatibles, provides for Boolean and macro input. A second package for more-advanced users runs on PC compatibles or workstations and adds schematic capture, and logic- and timing-simulation tools.

Available now, the first of the pLSI family is the pLSI 32-70. This 84-pin device has 32 GLBs, 64 I/O pins and 192 registers. In a PLCC, the part is priced at $98.50 (100s). The first of the ispLSI devices will begin shipping 4Q91. —*Jeffrey Child*

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Hillsboro, OR 97125
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Circle 352

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SOFTWARE AND DEVELOPMENT TOOLS

Ada environment tailored to RISC systems development

Aiming at Ada program development for RISC workstations and RISC-based target systems, TeleSoft has launched the RISCAda family of development environments. The initial offering will be RISCAda/Sparc, which will run on Sparc-based workstations and servers from Sun Microsystems and be able to develop optimized code for Sparc-based native and target environments. The family will eventually cross-compile to 68000-, 88000- and i960-based target systems. Eventually, TeleSoft hopes to port the development environment to other RISC-based platforms with the X Windows-based OSF/Motif user interface.

TeleSoft uses a graphical user interface (GUI) to integrate all the tools in the RISCAda environment into a single framework/GUI called EZ-Ada. The user interface has modes of operation for both beginners and advanced users, context-sensitive help, and an icon builder that lets frequently used operations and commands be put under control of a user-designed icon.

Optimizing compiler technology

The core of the RISCAda system is an optimizing compiler technology aimed at RISC architectures. The compiler includes full data flow and control flow analysis, and graph-coloring register analysis. Global optimization lets the compiler analyze the application across package boundaries, including the run-time system (also written in Ada). The compiler can recognize and eliminate all unused subprograms and thus reduce the size of applications.

The compiler is self-hosted, in that it compiles itself before being delivered to customers. Not only is self-hosting a test of the compiler's robustness—the more than 2 million lines of code must be self-hosted before the product is shipped—it also offers customers the same kind of optimizations in their compilers that they expect the compilers to deliver in their applications.

Efficient library management is also cited as a factor in overall compilation efficiency and speed. TeleSoft claims a compilation speed of 1,667 lines/min for optimized code and 2,456 lines/min for nonoptimized code as against 519 lines/min and 1,747 lines/min, respectively, for the Verdix compiler that will form the core of Sun Microsystems' SunAda environment.

The RISCAda development system also will feature a new debugging tool called AdaTracer. It includes a macro-editing feature that lets frequently used macros become icons. Using the macro processing and storage facilities, users can build regression test suites, for example. The debugger also includes its own profiling tool as a convenience so that performance tuning can be done at the same time as error tracing.

Included with the RISCAda/Sparc environment is the Arcs 2.0 toolbox, a collection of tools for managing the complexity of large applications-development projects. The toolbox includes a graphical system browser that shows users a graphical representation of the architecture of the system they're building; and a cross-referencer that uses a hypertext engine to navigate along all the declaration-usage patterns of a large program, showing links between declared entities and where the entities are used.

The Arcs toolbox also contains a language-sensitive editor that provides syntax and semantics checking. A semantics-completion service brings up all possible completions available after the first few characters of a procedure. On-line documentation of the available Ada packages, procedures and functions is provided from within the editor. A semantic checker is available to run the source code through without compiling in order to remove syntax errors that would slow down a compile. The semantic checker runs 5 to 10 times faster than the compiler.

RISCAda provides bindings to industry and government standards including Posix and Sun's XView (Sparc version only). Optional binding includes Sybase, Oracle databases, X Windows, OSF/Motif, and X+. RISCAda/Sparc will be available next month. Prices will range from $6,000 to $12,000, depending on configuration. The various bindings are available at prices ranging from $895 to $2,500.

— Tom Williams

RISCAda/Sparc at a glance

- Integrated tool environment
- OSF/Motif graphical user interface
- Optimizing Ada compiler
- Global optimization across packages
- Window debugger with built-in profiler
- Separate graphics-oriented profiler
- MIL-STD-1815A
- Validated under suite 1.11

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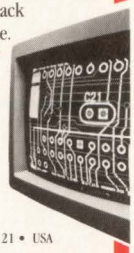

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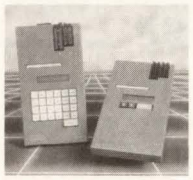

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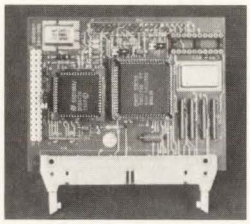

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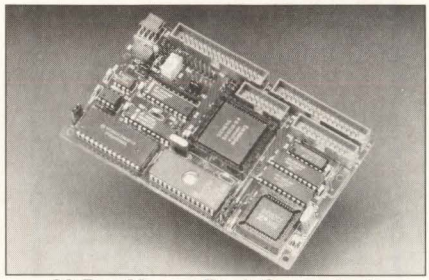

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COMPUTER DESIGN (ISSN-0010-4566) is published monthly by PennWell Publishing Company, 1421 S Sheridan, Tulsa, OK 74112. Second-class postage paid at Tulsa, OK 74112 and additional mailing offices. Editorial offices are located at One Technology Park Dr, PO Box 990, Westford, MA 01886. Annual subscription price: $88 in the U.S.A., $139 in Canada, $148 for Europe via air, and $192 other foreign via air. Call (918) 832-9263 for subscription information. Microfilm copies of COMPUTER DESIGN may be purchased from University Microfilms, a Xerox Company, 300 N Zeeb Rd, Ann Arbor, MI 48106. POSTMASTER: Send change of address form to COMPUTER DESIGN, Circulation Department, PO Box 3466, Tulsa, OK 74101.

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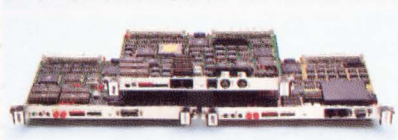

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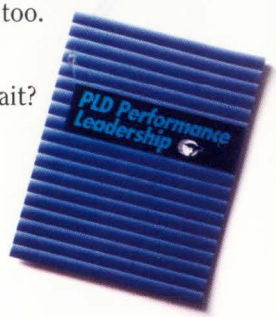

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