Heurikon's Abe Hirsh on:
VME vs. PLCs

A PENNWELL PUBLICATION MARCH 1992

COMPUTER DESIGN

Technology and Design Directions

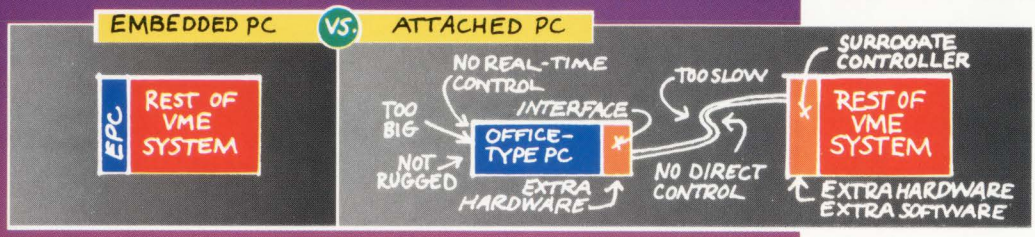
FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

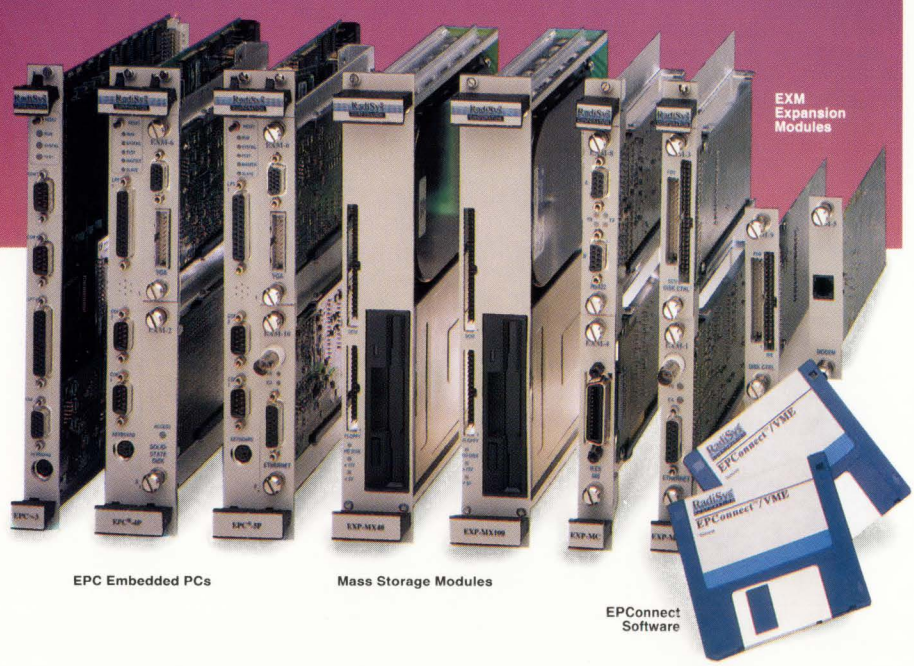
Designers can now take their pick of 32-bit debugging tools

Lack of standards impedes database management

Standard buses gain ground in image processing

RADISYS GIVES VME THE INSIDE ADVANTAGE





Integrating a PC with your VME system is a smart move. The "PC advantage" provides a superior human interface and access to the PC's huge base of system, application and development software.

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EPC MODEL	EPC-1 (shipping since Aug '88)	EPC-3 (shipping since Aug '89)	EPC-4 (shipping since Mar '90)	EPC-5 (shipping since Oct '90)
Processor Modules:				
CPU	80386	80386SX	80386	80486
CPU Clock	16 or 20MHz	16MHz	25 MHz	25 or 33 MHz
DRAM	1 or 4 MBytes	1, 2 or 4 MBytes	4, 8 or 16MBytes	4, 8 or 16 MBytes
Graphics	EGA (640 x 350)	VGA (800 x 600)	VGA (800 x 600)	VGA (800 x 600)
Mass Storage Modules:				
Hard Disk Capacity	40 MBytes		40, 100 or 200 MBytes	
Floppy Drive Size/Cap.	3.5" / 1.44 MBytes		3.5" / 1.44 MBytes	
Expansion Capabilities:				
PC Add-in Cards	Yes		Yes	
EXMbus Expansion	N/A	EXM Expansion Modules:		
		EXM-1 Ethernet	EXM-5 Modem	EXM-9 IDE/Floppy Ctrl.
		EXM-2 Solid State Disk	EXM-6 VGA Graphics	EXM-10 Ethernet
		EXM-3 SCSI/Floppy Ctrl.	EXM-7 RS232 Serial I/O	EXM-11 Timer/Counter
		EXM-4 IEEE 488	EXM-8 RS422 Serial I/O	EXM-12 Prototyping Card
Software Support:	EPConnect development, run-time, and multiprocessing software package for DOS, Windows, UNIX,and OS/2			

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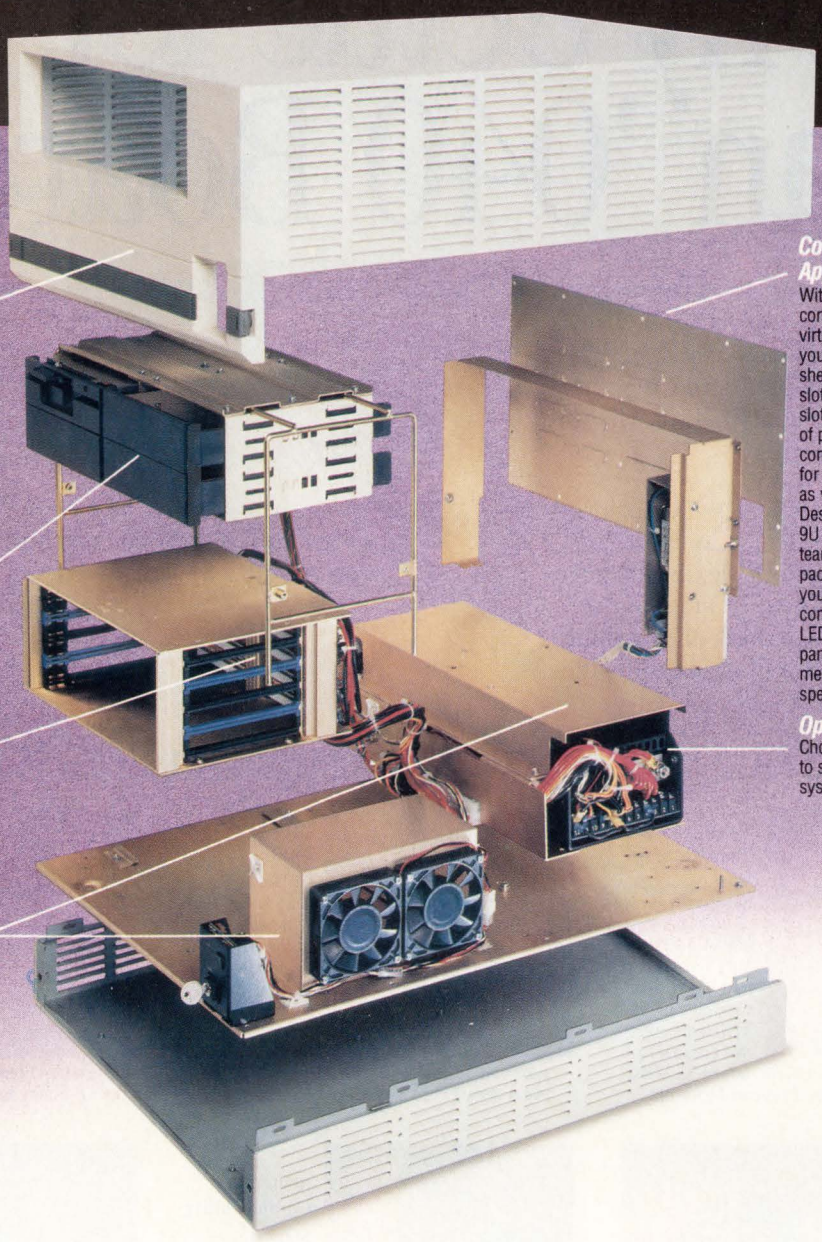
CIRCLE NO. 1

O M E G A

New



Easy Access = Maximum Accessibility
Quick access saves time in assembly, test, and maintenance. Loosen two captive fasteners and the front, top, and sides slide off for maximum access to all of the internal components. Each internal component comes out with two screws, or remove five hex nuts and the entire system lifts out of the bottom tray to provide a free-standing, fully functional development platform!

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Up to eight half-height 5¼" peripherals simply slide into their mounting brackets.

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Plug your VME system into the quietest backplane ever! Our new 10-LAYER VME backplanes handle the fastest VME signals with the absolute minimum distortion, crosstalk, and noise.

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Airflow is directed over the components that need cooling—the power supply and your boards. Separate chambers maximize cooling by channeling airflow and restricting recirculation.

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With over 2000 standard configurations you can virtually design the enclosure yourself—and still get it off the shelf. Choose from 3 to 14 slots for VME or 4 to 18 slots for Multibus. Loads of peripheral options and configurations are available for rack and tabletop models as well as floor-standing DeskMate™ verions that accept 9U × 400mm cards. Or let our team of engineers provide a packaging solution tailored to your specifications—from configuring the front panel LEDs to customizing the rear panel. Designing enclosures to meet your specific needs is our specialty.

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Choose from 175 to 1000 Watts to satisfy the demands of your system.

The Last Word in System Packaging

Now you can benefit from 12 years of design experience and innovation that has made Electronic Solutions the industry leader in system packaging. The Omega™ Enclosures will give your VME or Multibus system the attractive exterior your image demands with a rugged, well-designed interior to withstand the most demanding environments. And besides the Electronic Solutions' full 3-Year warranty, the Omega bears FCC approvals and is UL, CSA, and TUV listed to get your system to an international market in the shortest time possible.

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CIRCLE NO. 2

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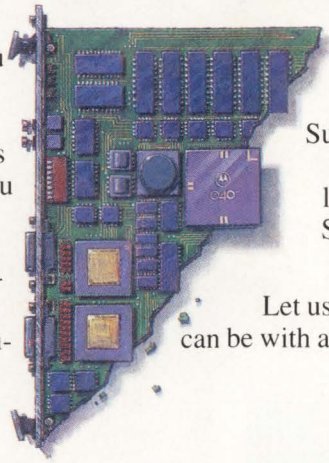
Why Settle for ½ an '040 Board?

You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

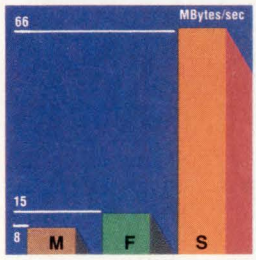
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.



Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

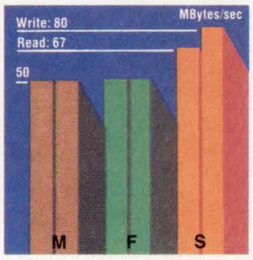
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



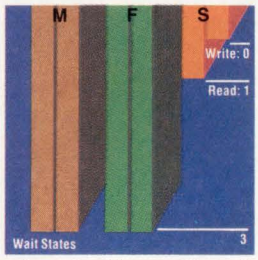
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



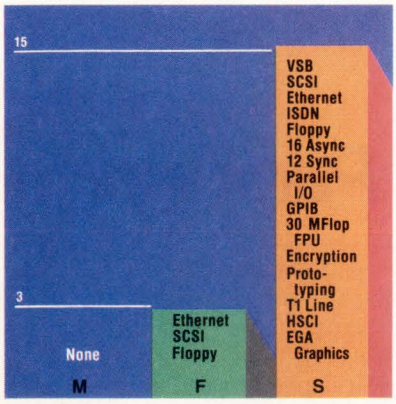
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



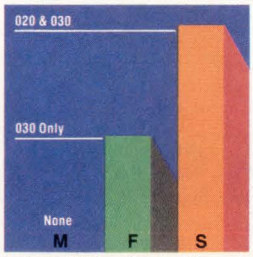
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



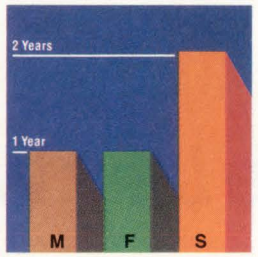
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



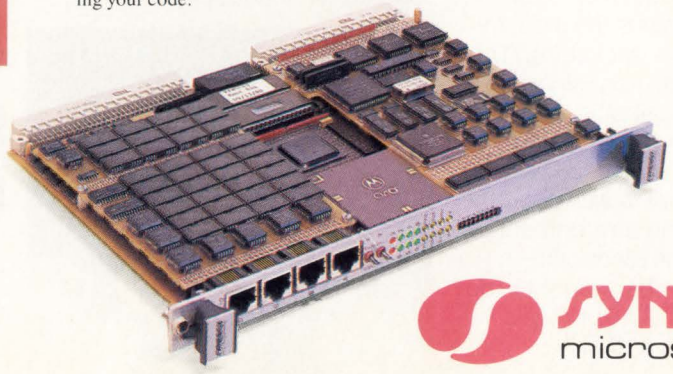
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

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CIRCLE NO. 3

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VOL. 31, NO. 3 MARCH 1992

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Technology and Design Directions®

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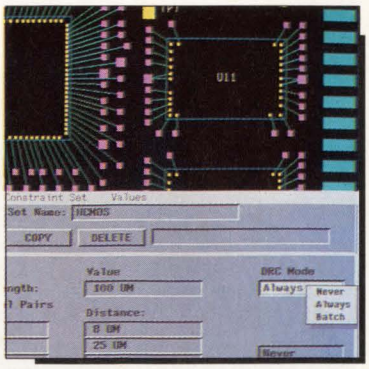

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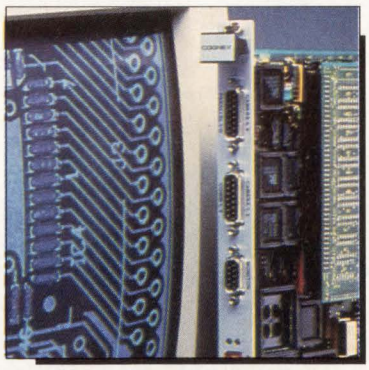
TECHNOLOGY DIRECTIONS



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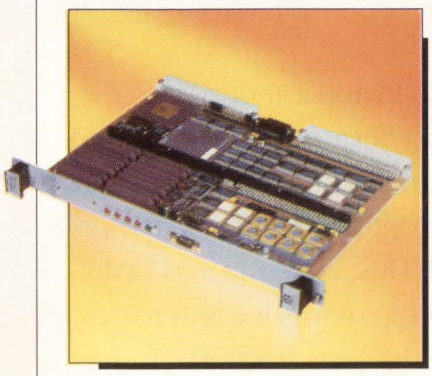
TECHNOLOGY AND DESIGN FEATURES



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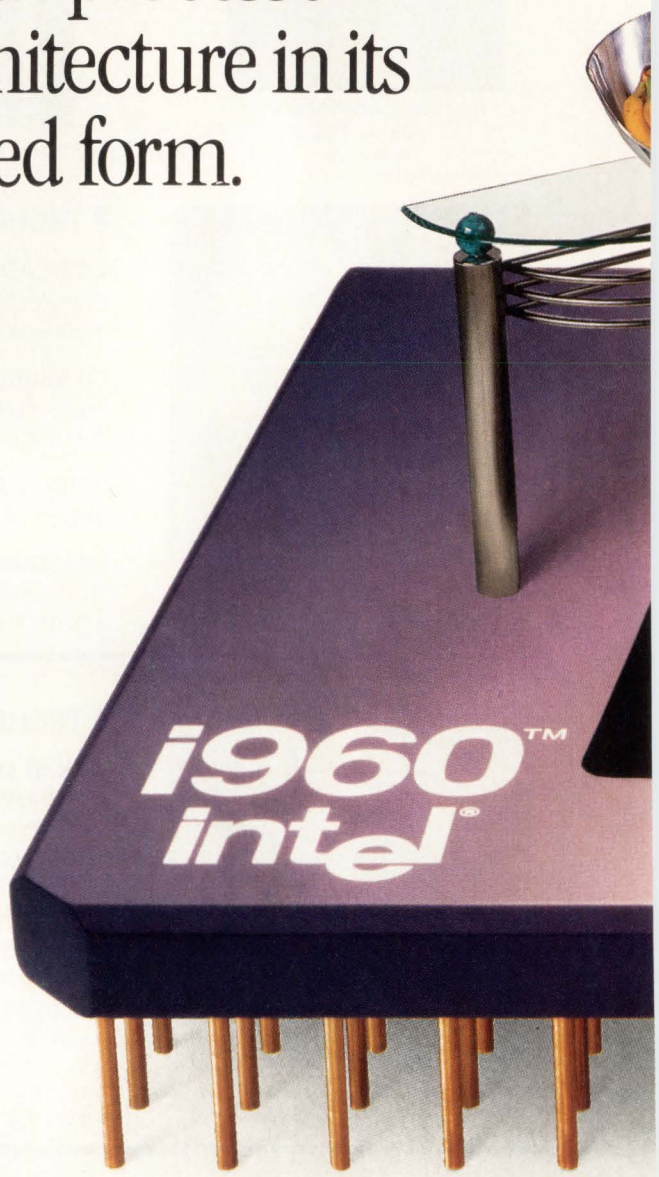
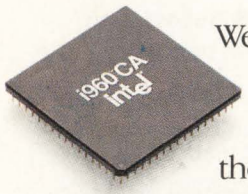
Cover Illustration: Gary Torrisi

NEW PRODUCT DEVELOPMENTS

Move into our i960™ CA processor and get our 32-bit architecture in its most sophisticated form.





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And while the i960 CA processor may be

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The Computer Inside.™

CIRCLE NO. 4

SilcSyn gets European support, contributes to R-R's comeback

Though the second-generation SilcSyn high-level synthesis tool from Racal-Redac (Mahwah, NJ) is not yet highly visible in this country, it's been gathering a lot of enthusiastic support in Europe. Total sales of systems including SilcSyn have exceeded $630,000 over the last calendar year in Belgium and Holland alone, reports Racal-Redac. Ahead of its time on its first go-round (supporting a proprietary hardware description language before HDLs were popular), SilcSyn now supports VHDL and also accepts structural netlists. Its capability to synthesize at a micro-architectural level is still beyond the scope of most synthesis tools available today. On top of that, Racal-Redac has added the capabilities of HHB's Intelligent ATPG tool to SilcSyn's test synthesis and has interfaced SilcSyn to its Cadat simulator.

As Racal-Redac builds support among ASIC vendors in the U.S., it will be exciting to see if Europe's enthusiasm for SilcSyn spreads to Silicon Valley and other American high-tech areas.

—Barbara Tuck Egan

Money for old wire

Having bought that 33-MHz 386/387 PC-based workstation, process controller or medical diagnostic equipment, you need to upgrade it to make it run faster. Now, for $499 you can, courtesy of two new chips from Intel (Santa Clara, CA). After purchasing Intel's RapidCAD engineering coprocessor—a set of two chips dubbed RapidCAD-1 and RapidCAD-2—you can use them to replace the 386DX and 387DX on your present motherboard. The result is a system that runs a Specmark 56 percent faster than your existing one.

RapidCAD-1, pin-compatible with the 386DX processor, integrates the 386 CPU and the 387 FPU on the same silicon chip. So what, you might ask, is the RapidCAD-2 for? Harry Laszlow, marketing manager of the RapidCAD chip set, explains that 386/387 system hardware assumes that floating-point calculations are performed by a device residing in the 387 socket and that the appropriate interrupt will be sent from the 387 to the 386. RapidCAD emulates that procedure.

"Although the 387 is already on the RapidCAD-1 device, the signal must still be routed through external logic," says Intel's Laszlow. He admits that, since that's the case, the RapidCAD-2 chip isn't particularly complicated, but defends the design as more than "just a wire." It's a matter of a few hundred gates, he says.

How can Intel charge $500 for the two chips, one of which the company admits has only a few hundred gates? "RapidCAD is aimed at end users who already have a 386DX-based system," says Laszlow. So the price [Intel charges] for the 386 or the 387 and RapidCAD isn't an issue from the point of view of a user who has a system already and is deciding how to upgrade it." *—Dave Wilson*

Material extends life of microbatteries

Researchers at Bellcore (Red Bank, NJ) have discovered a material that eases the task of building lithium power sources into integrated circuits. While lithium has become the preferred electrolyte for compact rechargeable batteries, using the highly reactive metal to make "microbatteries" at the chip level has been difficult. Lithium microbatteries are built by layering a lithium-based electrolyte film between cathode and anode films. To charge and discharge a system, lithium diodes must migrate between the center electrolyte film and the cathode. Cathode materials become unstable during that process, shortening the battery's life.

By using lithium manganese oxide as the film, researchers were able to achieve a higher lithium-ion density. The oxide lattice lets the lithium ions migrate while keeping its structure intact. In experiments conducted so far, researchers have demonstrated working microbatteries that sustain up to 70 charge/discharge cycles at 4.1 V without any degradation in performance.

—Jeffrey Child

H-P, Analog Devices ink mixed-signal deal

In an effort to speed development of advanced mixed-signal processes required for their future digital signal processors and system-level mixed-signal ICs, Analog Devices (Norwood, MA) has formed a strategic alliance with Hewlett-Packard (Palo Alto, CA). Under the terms of the agreement, Analog Devices gains immediate access to H-P's submicron CMOS and BiCMOS technologies. Because of the heavy technical and financial resources required to develop new submicron mixed-signal processes, the agreement also allows for joint process development.

While the initial products developed by Analog using these processes will be manufactured in H-P's facilities, the agreement gives Analog Devices the right to obtain a license to facilities when Analog's production requirements justify the investment needed to bring submicron manufacturing capability in-house. Analog's first 0.55-micron units, built on H-P's wafer fab, are expected to ship next year. *—Jeffrey Child*

Mentor plans four Unix ports

Mentor Graphics (Wilsonville, OR) continued to pursue its plans to become a software-only business when it recently announced plans to port its Release 8.0 software to Unix platforms from DEC (Maynard, MA), IBM (Armonk, NY), NEC (Tokyo, Japan), and Sony (Tokyo, Japan). Mentor also disclosed plans to integrate its Falcon Framework with Digital's PowerFrame, a move that all but assures PowerFrame will become the de facto industry standard for design data management. Though it's unclear just how tight the Falcon-PowerFrame integration will be, Mentor's support for PowerFrame comes as a bit of a surprise, because Mentor has been a stubborn holdout among leading EDA vendors who have endorsed DEC's framework. *—Mike Donlin*

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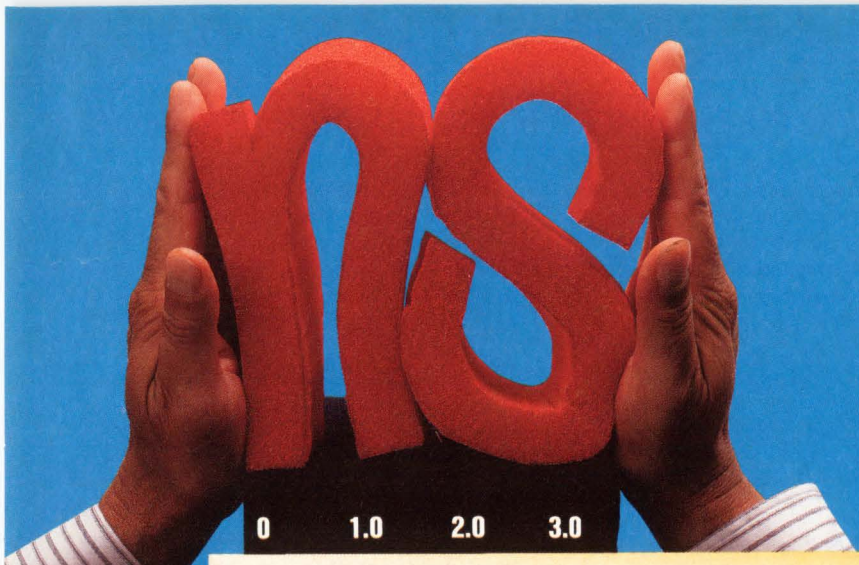

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FCT-CT logic has true TTL compatibility for ease of design. The reduced output swings and controlled output edge rate circuitry ensure low system noise generation. No other technology offers higher speeds or lower power consumption.

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Buffers	4.1ns	5.8ns	5.2ns
Transceivers	4.1ns	5.8ns	4.8ns
Registers	5.2ns	5.5ns	5.0ns
Latches	4.2ns	5.5ns	5.0ns

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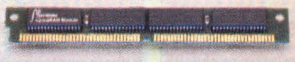

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CIRCLE NO. 5

Continued from page 6

CAE wars continue in Europe

Cadence Design Systems (San Jose, CA) chalked up a big win in Europe recently by inking a pact with Philips Semiconductor (Eindhoven, Netherlands). Under the terms of the multi-year agreement, Philips will purchase Cadence's IC design suite, including its synthesis tool and the Verilog simulator. Though both companies are contractually obligated not to reveal the value of the deal, some industry analysts are estimating its value at over $10 million.

The agreement's value isn't in dollars alone. Last fall, Cadence lost face in Europe when a deal it was forging with Siemens-Nixdorf Informationsysteme (Munich, Germany) fell through after archrival Mentor Graphics (Wilsonville, OR) slipped in to become SNI's vendor of choice. Though Cadence is still working on an alliance with SNI, its grand plan to form a joint sales and marketing company with Siemens in Europe is on hold for the time being. *—Mike Donlin*

3U VMEbus fires salvo

A newly formed group of 3U VMEbus manufacturers has fired its first salvo against other small form-factor buses such as STD, STD32 and G64/96. The group, headed by Mizar (Carrollton, TX), GreenSpring Computers (Menlo Park, CA) and PEP Modular Computers (Pittsburgh, PA), has some exciting ideas to boost bus performance and make it a more flexible medium. Each of the major participants will be bringing something to the party, which, when finished, will constitute a part of a secondary standards body to be known as IEEE-1014.2, Recommended Practices.

Mizar will bring its approach for multiplexing the P1 VME connector to provide a full 32 bits of data (by multiplexing the original 16 bits) and 40 address bits (by multiplexing the upper 16 address bits with the original 24). To that, PEP will add its Autobahn technology, providing a very high-speed (400 Mbytes/s) serial channel. GreenSpring will add its I/O Pak technology as a standard 3U mezzanine bus to provide flexibility to the approach. In addition, the group plans to standardize on a high-density I/O connector—in the area of 0.050-in. spacing—to bring high-density I/O to the front of the board. In addition to targeting traditional and upscale STD customers, the group will be aiming at making a major dent in the PLC business. *—Warren Andrews*

H-P, IBM in fiber-optic alliance

Hewlett-Packard and IBM plan to get together in developing and marketing components for high-speed fiber-optic communications links. According to the companies, the components will offer a substantial price-performance benefit over existing products.

One of the first things to come out of the agreement will be high-volume compact disk laser technology, followed by specialized optical link cards handling optical transmission using the ANSI Fiber Channel standard. The agreement will provide a framework merging IBM's technologies in optical link card manufacturing and CD laser applications with H-P's technologies for optical receivers and high-speed transceiver circuits. The first implementations will operate at the FC-0 level of the Fiber Channel Standard at 266 Mbytes/s. Future iterations will extend to the gigabyte (and beyond) transmission range.

The move is expected to benefit both companies—it's expected to enable H-P to manufacture optical-link cards in high volumes, while it lets IBM aggressively pursue its thrust into the OEM marketplace. *—Warren Andrews*

Sharp making deals with Apple and Intel

Japan's Sharp Corporation has been making some interesting marketing and technology transfer agreements with two U.S. companies—Apple Computer and Intel. Sharp has nailed down an agreement with Intel to build an $800 million fab line in Japan to produce flash memories under license from Intel. Both companies will market the chips, presumably with Intel limited to the U.S. market and Sharp to the Japanese. Ironically, flash memory is one technology that was invented in Japan (by Toshiba), but in which U.S.-based Intel achieved market dominance.

The deal with Apple comes as that company prepares a launch into the consumer electronics market with what is thought to be a line of handheld computers. Sharp, which is already well-known for its line of Wizard pocket data managers, will manufacture the devices in Japan and sell them under its name. Apple will sell them in the U.S. under the Apple name. The first product out of this agreement is thought to be a handheld computer with pen input and communications capability; it will include a built-in calendar and phone book. Although not explicitly announced, one would expect the line of Apple devices to be able to exchange data and programs with the Sharp Wizard line.*—Tom Williams*

Hot swap—the latest rage

Over the past several months, the Multibus Manufacturers Group (MMG) has been working on 'hot swapping'—a capability useful in telecommunications that involves replacing a card in a system while it continues to operate uninterrupted. The group's worked with Intel, Siemens and others to nail down the specifications, but the first company to introduce a product is Micro Industries (Westerville, OH). According to Michael Curran, company president, the approach is very similar to MMG's, and is ready for implementation—in fact, the company already has orders.

In the meantime, a number of VMEbus board manufacturers are also working on hot swap. Heurikon, Motorola, Themis Computers, and backplane maker Electronic Solutions are all developing the capability, either independently or with customers. Unless someone on the IEEE-1014 Committee acts fast, it's entirely possible we may see several approaches to hot-swap capability on VME before long. *—Warren Andrews*

VME performance at a price you can sink your teeth into! Heurikon's HK68/V3D offers VME standardization and design flexibility with a 33 MHz Motorola 68EC030 and 2 Mbytes of memory for only $1795 (less in quantity). That makes the V3D a cost efficient entry point into VME single-board computers. As a complement to our main course, you can add more memory, SCSI or Ethernet. VxWorks and OS-9 are also available.

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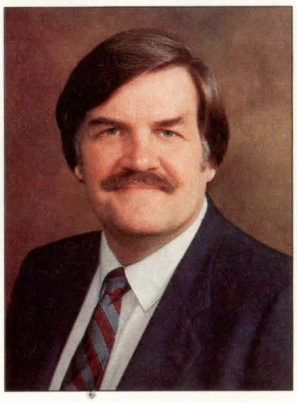
CIRCLE NO. 7

Bush gave bashing a bad name

Telling the truth isn't bashing.



John C. Miklosz
Associate Publisher/
Editor-in-Chief

When I was growing up, my mother told me to always tell the truth. She also relied on a well-worn cliche to remind me that the truth sometimes hurts. (Sorry, mom, but the "always" has been tough to live up to and I've hurt a few people by being a bit too honest.) While I can think of a lot of ways to describe being truthful—like honest, blunt, frank, even brutally frank—I would never have thought of using the term "bashing" to describe telling the truth.

When it comes to discussions of Japanese business practices and American/Japanese trade relations, however, there are a lot of people who would like you to think that being truthful is synonymous with bashing. Unfortunately, they all got a boost in their efforts from the recent comments made by President Bush blaming the Japanese for the current recession. Now, that's bashing because it's not the truth.

The current recession is home-brewed and we have no one to blame but ourselves. True, Japanese dominance of certain markets has devastated some industries (consumer electronics is the most relevant to us) and is well on the way to devastating some others (automobiles are probably the best example). These have contributed to our problems, but they're not the cause. The Japanese aren't responsible for our domestic woes, whether it's our deteriorating infrastructure; our deteriorating schools; our outmoded approach to manufacturing; the ineffectual relationship between government, business and labor; our wastefulness; or our budget deficit. And they're not responsible for the current recession.

The truth about Japanese business and trade practices has been laid out in great detail by writers such as James Fallows, Chalmers Johnson, Clyde Prestowitz, and Karel van Wolferen (the Gang of Four, as they've been called in certain circles). In books and numerous articles, these four (and many others) have documented the interlocking nature of directorships and the *keiretsu*; the penetration and elimination of the American consumer electronics business, which relied heavily on price fixing and dumping; the closed nature of Japanese financial markets and distribution system; the use of inspection and certification as a market barrier (aluminum baseball bats are a great example); lobbying and influence efforts in the U.S. to the tune of $400 million a year; discrimination against their own women and non-Japanese in business; and the Japanese proclivity for patience (which is synonymous with stonewalling).

The facts in all these matters have been documented repeatedly, perhaps too much. Perhaps so much, that the claims of bashing have been given unwarranted credence. But as my mother taught me, one should tell the truth. And sometimes the truth hurts. But telling the truth isn't bashing.

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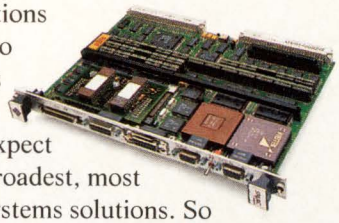

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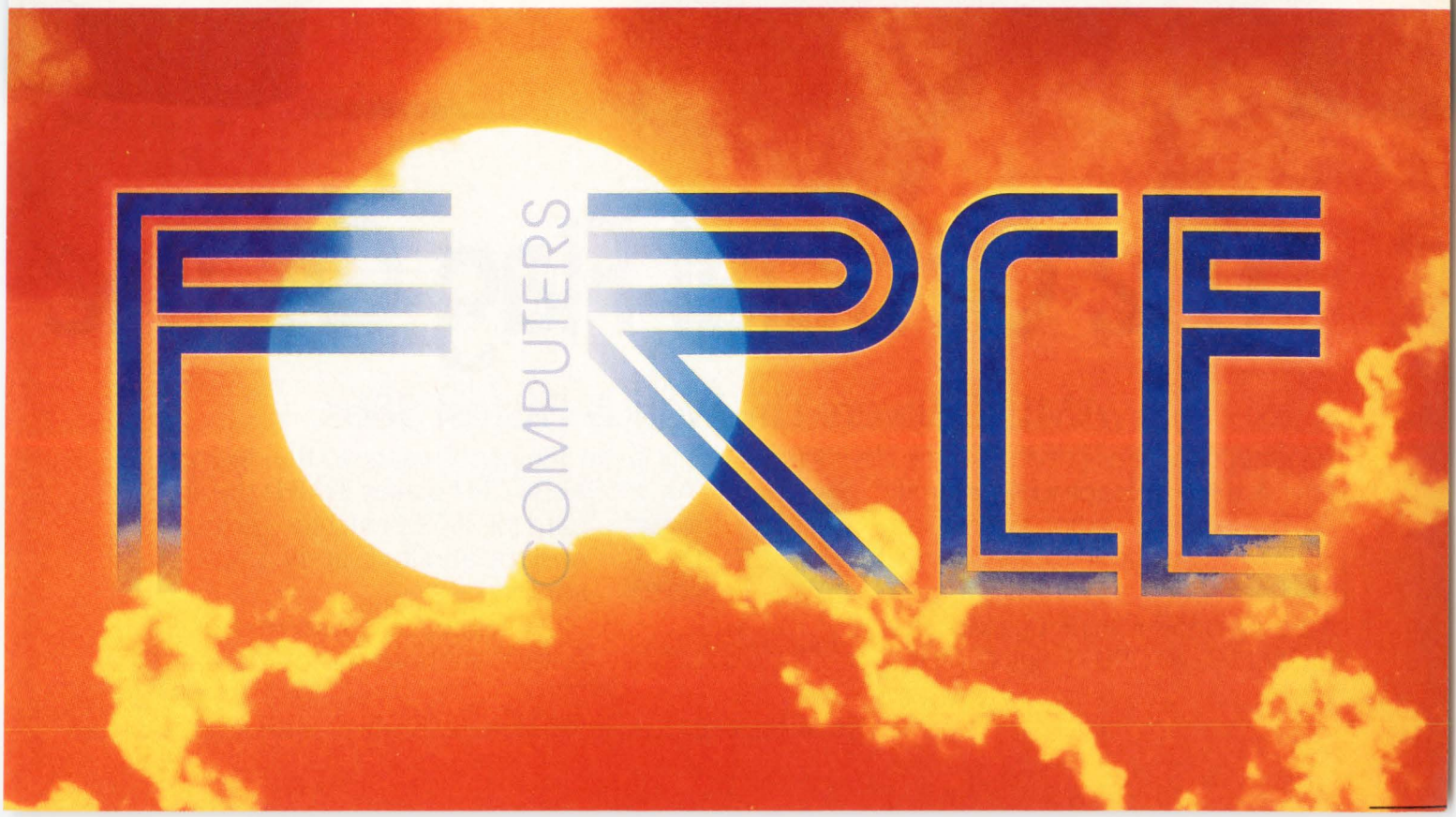
CIRCLE NO. 8



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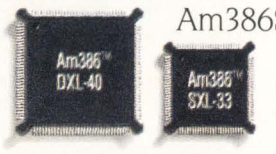

The 40MHz DXL-40 and the 33MHz SXL-33 are available in low-cost POFP packaging.

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Am386 Microprocessors.

And of course, they're proven-compatible with the IBM® standard.

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CIRCLE NO. 9

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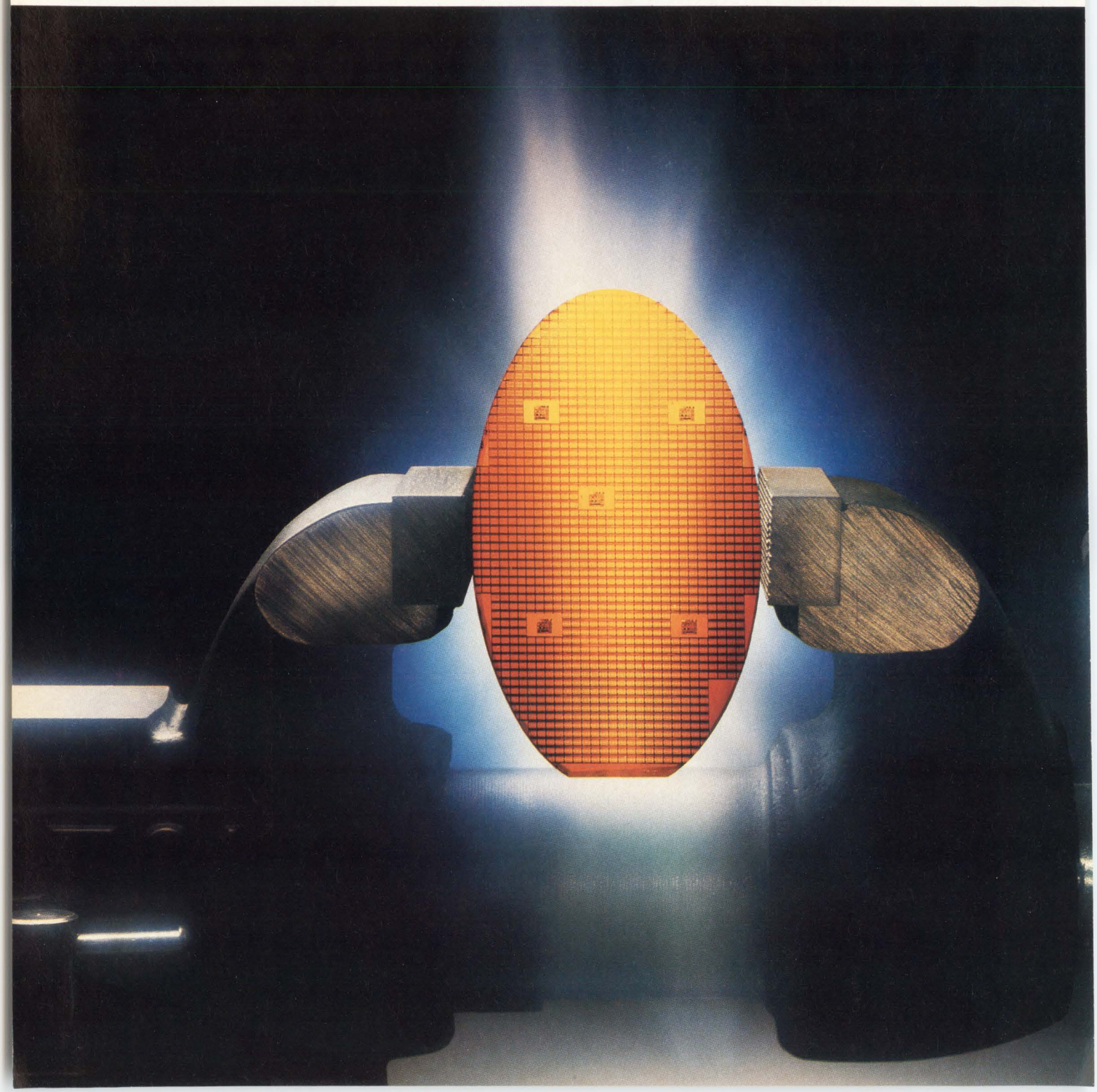

speed from our logic. as 4.1 ns!

With our new Advanced BiCMOS interface logic (ABT) family, you get the speed, drive and low power you need to optimize the performance of processors operating at 33 MHz and above.

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Other critical performance parameters are as impressive. Drive capability is 32 to 64 mA. Static power consumption is typically 2 mA (I_{CCH}, I_{CCZ}) and 30 mA (I_{CCL}). Ground bounce is less than 800 mV typ.

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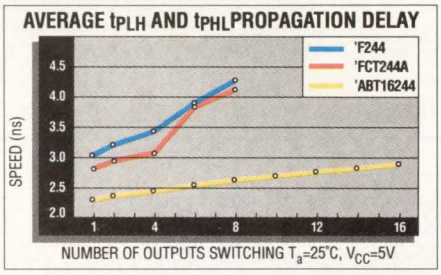
Also in volume production are the Widebus 'ABT16245 16-bit bidirectional bus transceiver and the 'ABT16543 and 'ABT16952 16-bit bidirectional registered bus transceivers.

As in our successful Advanced CMOS Logic (ACL) Widebus family, these devices come in our leadership surface-mount shrink small-outline package (SSOP) that gives you twice the number of I/Os as a standard small-outline package in the same space.

Unique additions included

There are also new devices in our ABT Widebus family featuring greater density and functionality. Our 'ABT16500A is a good example. An 18-bit registered transceiver, it combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.



TI's speed advantage: *In a one-to-one comparison, a TI 'ABT16244 16-bit Advanced BiCMOS driver proves to be much faster and more stable than Advanced Bipolar and standard CMOS octal drivers.*

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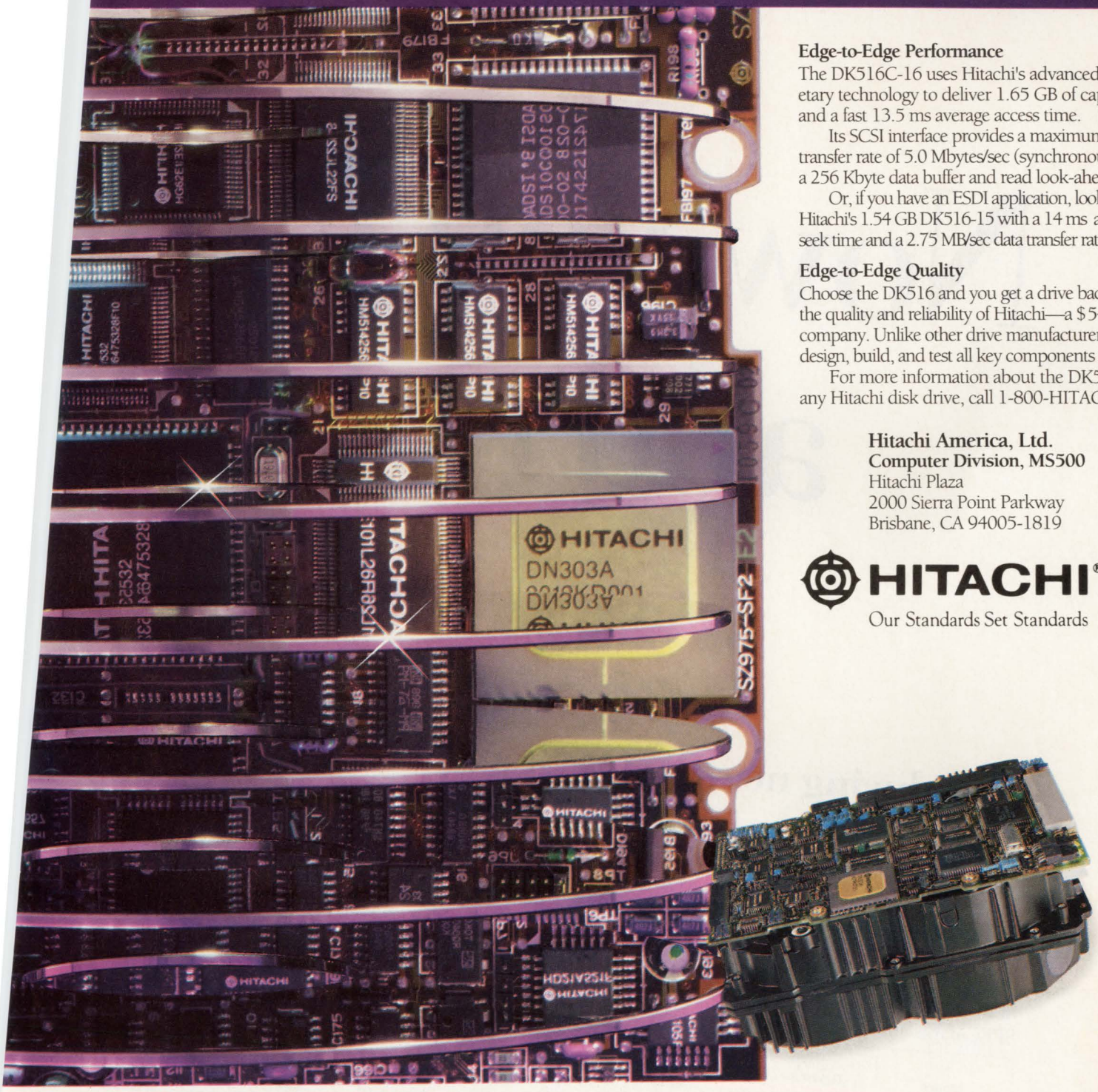

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CIRCLE NO. 13

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CALENDAR

CONFERENCES

March 10 - 12
SEMICON/Europa 92

Zuspa Convention Centre, Zurich, Switzerland. SEMICON/Europa is the largest trade show in Europe dedicated to the newest products and equipment in semiconductor processing and materials. Semiconductor Equipment and Materials International (SEMI) will hold standards meetings March 9 - 12. There will be five technical conference themes: "Process tool integration;" "Manufacturing science;" "Quality requirements for media and supply systems;" "Process monitoring;" and "The face of European test applications in the 1990s." Contact: SEMI North America, 805 E Middlefield Rd, Mountain View, CA 94043-4080, (415) 964-5111, Fax (415) 967-5375 or SEMI Europa, Avenue de Cortenberg, 79, B-1040 Brussels, Belgium, 32-2-736-2058, Fax 32-2-734-0622. **Circle 366**

March 10 - 12
SOUTHCON/92

Orange County Convention/Civic Center, Orlando, FL. This electronics conference and exhibition in the Southeast brings together design, test, manufacturing, and telesystems in one show. More than 300 exhibitors will feature the latest networking and data communications products; semiconductors; electronic design automation tools; test and measurement instruments; and passive components. Technical sessions and tutorials will include such topics as high-speed data communications, computer imaging and real-world applications of neural networks. Contact: Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045, (800) 877-2668, Fax (213) 641-5117. **Circle 367**

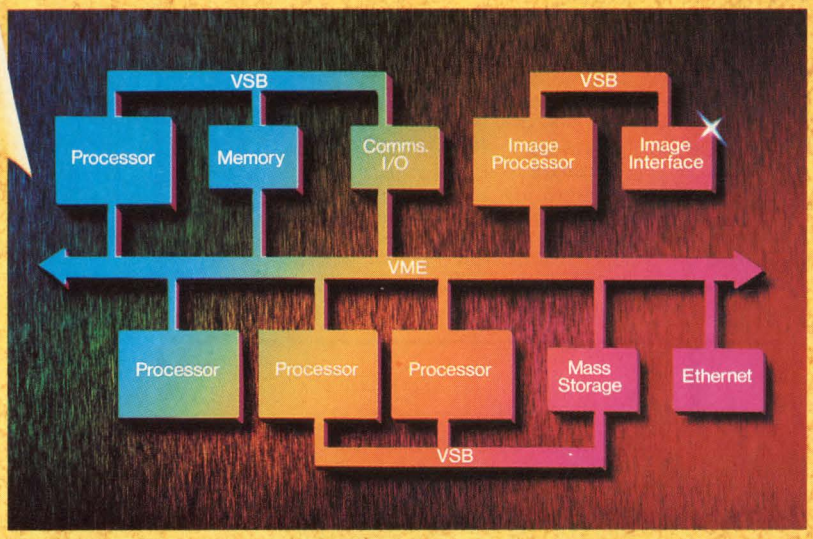
March 11 - 18
CeBIT '92

Hannover Fairgrounds, Hannover, Germany. More than 4,600 exhibitors from 40 countries will attract more than 570,000 attendees. Among the technologies highlighted are: software and systems, CAD/CAM/CAE, minicomputers and information systems, LANs, and new to the show is the "EDA at CeBIT" center. Contact: Interim Communications, 255 N Market St, San Jose, CA 95110, (408) 287-7980, Fax (408) 287-7981. **Circle 368**

March 16 - 19
EDAC-92

Palais des Congres, Brussels, Belgium. The European Conference on Design Automation will feature technical sessions and tutorials for CAD users, designers, suppliers, and researchers. Topics include: CAD systems and frameworks, application-specific CAD for system design, formal verification, layout synthesis and verification, logic and finite state machine (FSM) synthesis, simulation, testing, and high-level synthesis. Contact: EDAC-92 Secretariat, CEP Consultants, 26-28 Albany St, Edinburgh EH1 3QH, Scotland, UK, 44-31-557-2478, Fax 44-31-557-5749. **Circle 369**

Radstone reveals an ancient technique for designing an ultra high performance VME system...now.



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CIRCLE NO. 18

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CONFERENCES

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National Exhibition Centre, Birmingham, England, UK. This three-day show features hundreds of exhibitors plus eight different clinics and forums including: the ATE Center; the surface-mount clinic for surface-mount problems; the EMC forum; anti-static clinics for the best methods to prevent damage from electrostatic discharges; and the design center featuring the latest in microcontrollers, transputers, semiconductors, and ASICs. Contact: A-Z International Sales, Amanda Blaskett/Zena Coupe, 70 Chalk Farm Rd, London NW1 8AN, UK, 44-71-284-3171, Fax 44-71-284-3174.

Circle 370

April 6 - 9
Comdex/Spring '92

COMDEX/Spring The World's Leading Computer Trade Show for Resellers and End-Users

McCormick Place, Chicago, IL. This year's show for resellers and end users is devoted to programs that realize the potential of the desktop computer. Comdex has four programs with more than 90 sessions aimed at the desktop user: corporate solutions; network computing and Unix/open systems; multimedia; and imaging systems. Attendees will be able to visit the Windows World '92 exhibit as well as over 900 Comdex exhibits. Contact: The Interface Group, 300 First Ave, Needham, MA 02194-2722, (617) 449-6600, Fax (617) 449-2674.

Circle 371

April 27 - May 1
XWorld

X WORLD The X Info Xchange

Sheraton New York, NY. XWorld is the largest conference and exhibition devoted to the X Window System. Over 40 technical and managerial sessions will be offered as well as exhibits. Tutorials will include: "Using the X Toolkit," "Widget Writing," "Debugging X," "System Administration," "C++ Programming," and "Windows for X Programmers." Contact: SIGS Publications Group, 588 Broadway, Suite 604, New York, NY 10012, (212) 274-0640, Fax (212) 274-0646.

Circle 372

April 28 - 30
AFCEA Europe Spring Symposium and Exposition

AFCEA

Hotel Melia Castilla, Madrid, Spain. This conference on simulation and high technology C^3I will explore how to solve a broad range of C^3I operational, training and system design problems. The five major session topics include: "Simulation and modeling in support of C^3I system design and optimization," with subsessions on future NATO communications networks and more. Other topics discussed will be modeling and simulation as tools for operation analysis; simulation in support of cost-effective training; and technologies that support simulation and modeling. Contact: J. Spargo & Associates, 4400 Fair Lakes Court, Fairfax, VA 22033, (703) 631-6200, Fax (703) 818-9177. **Circle 373**

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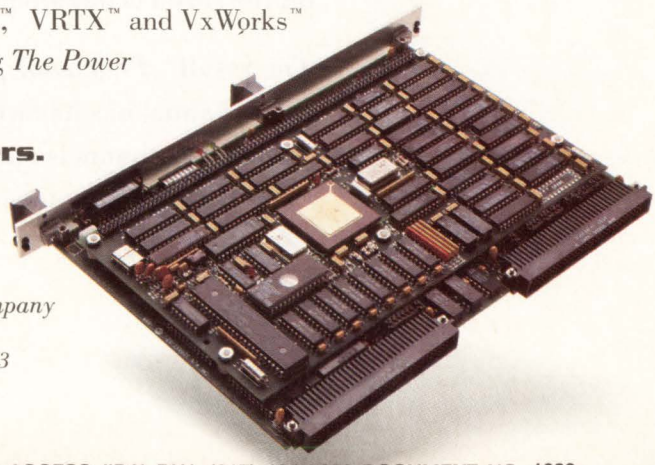

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CIRCLE NO. 21

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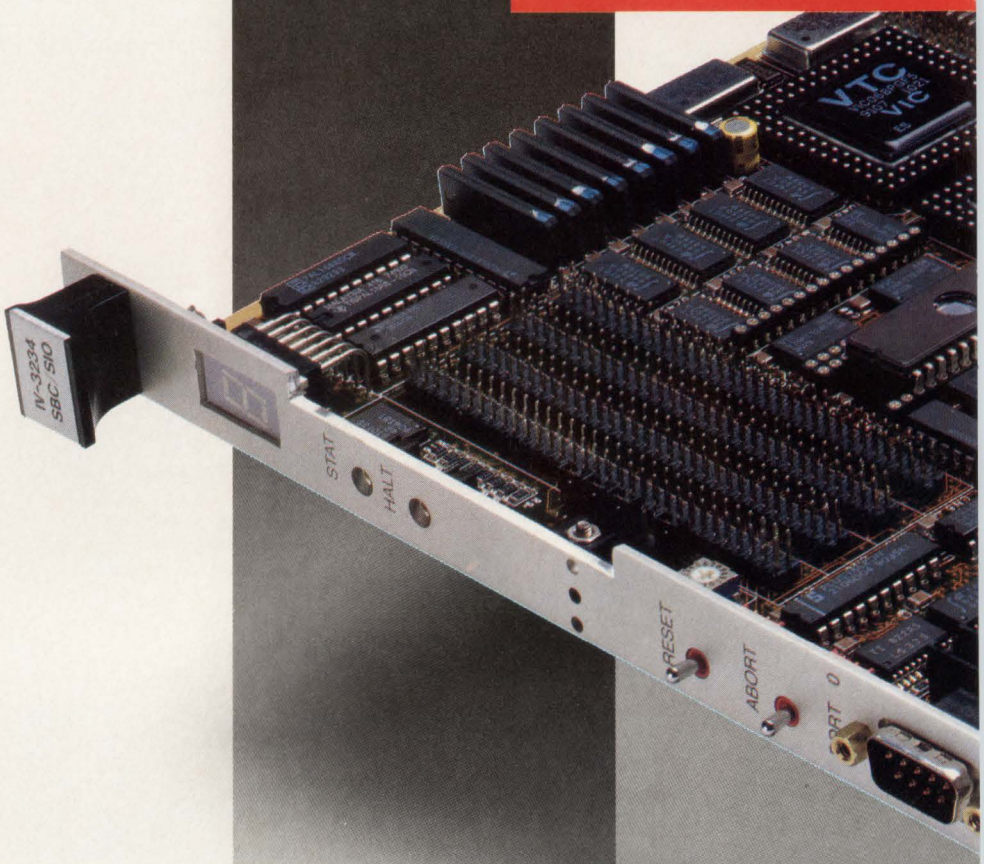

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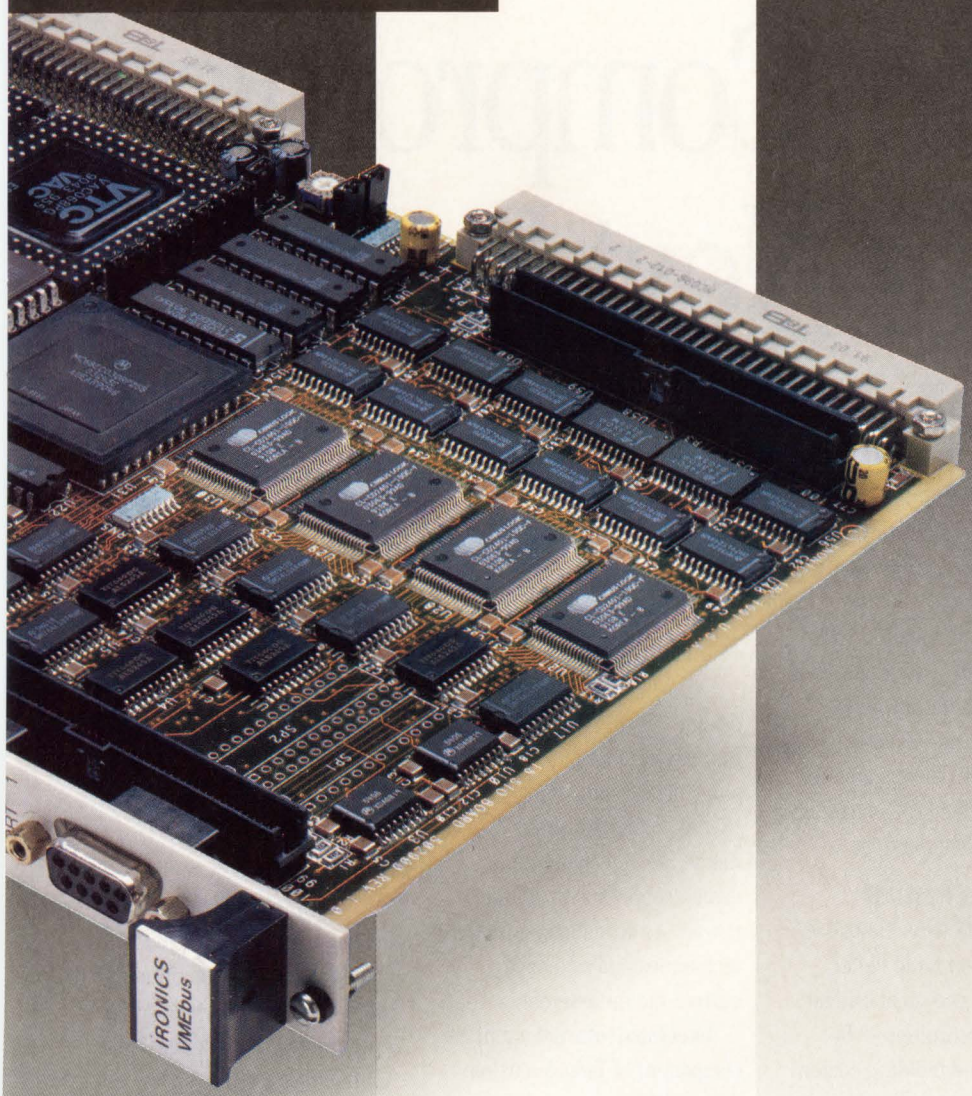

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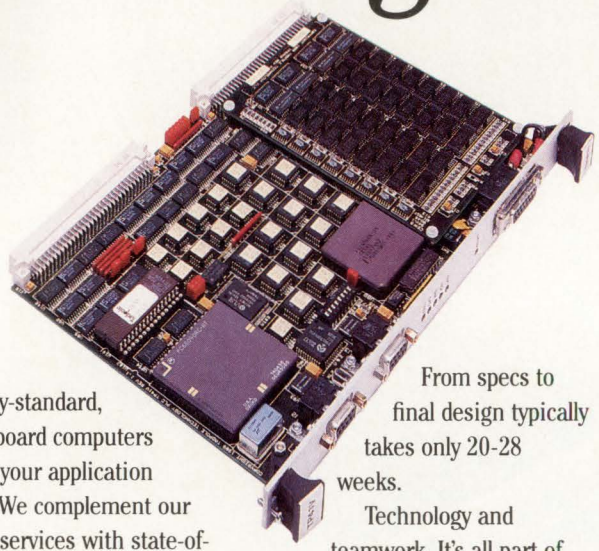

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Computing Without Compromise

T A D P O L E

CIRCLE NO. 23

Abe Hirsch on: VME vs. PLCs

Open VMEbus systems offer a number of advantages over proprietary programmable logic controls (PLCs) and other closed computer systems now used in factory-automation and process-control applications. Among these advantages are higher performance, lower cost, higher levels of integration, superior connectivity, and a broader selection of hardware and software.

Despite these advantages, VMEbus vendors have found both factory-automation and process-control applications tough to crack. One reason is the extensive hand-holding by suppliers of proprietary systems, particularly in the process-control market. For example, distributed control system (DCS) vendors often provide complete cradle-to-grave support, from hardware/software design and integration to maintenance, service and even operator training.

By taking complete control of the design, integration and maintenance processes, suppliers of proprietary systems have created a strong dependency among their customers. The downsizing of engineering staffs that has occurred in many factories has increased this dependency, making engineers even more reluctant to shake off their proprietary bonds.

For their part, suppliers of VMEbus products have done little to entice neophyte factory and process-control engineers to experiment with open systems. From a hardware standpoint, configuring and integrating VMEbus systems using boards from multiple vendors still requires considerable expertise, particularly in applications requiring multiple CPUs and bus masters. Most VMEbus board vendors lack the resources and commitment needed to guide an inexperienced factory or process-control engineer through the system-integration process.

An equally significant problem has been a lack of suitable vertical application software. Factory-automation and process-control engineers have grown accustomed to turnkey application-development environments that require little or no programming expertise. Most vendors of VMEbus board-level products, by contrast, still deal in components, providing only basic system-level software such as real-time operating systems, compilers and debuggers.

Abe Hirsch, general manager, Heurikon, Madison, WI

Open systems gain a foothold at high end

Despite this lack of vision among VMEbus vendors, VMEbus systems are beginning to gain a foothold, particularly in high-end applications. One reason is a growing dissatisfaction with the high cost of proprietary systems, not only for the base system but for post-installation commissioning and refinement, upgrades, maintenance, and other support services. Just as mainframe and minicomputer users did in the late 1970s and 1980s, process-control and factory-automation engineers are looking for less expensive solutions that limit their exposure to a single vendor.

Another reason that open systems are gaining a foothold in high-end distributed factory-automation and process control applications is growing application complexity. In many applications, proprietary systems have hit a wall, not only in terms of performance but also of connectivity and their ability to integrate an increasing range of noncontrol functions.

A significant reason for the lackluster performance that most proprietary systems offer is the ground-up design approach that PLC and DCS vendors take—from the CPU boards and backplanes to the I/O and networking subsystems. This ground-up approach makes it more difficult for DCS and PLC vendors to take advantage of technology advances. For example, while designers of open VMEbuses are already beginning to integrate 32- and even 64-bit RISC processors, DCS vendors are just now making the transition from the 80386 and 68010 to the 68020.

PLCs have also failed to keep pace with advancing technology. Most high-end PLCs, for example, are only about 30 percent faster than an 8086 PC when executing ladder logic control programs—not too impressive when you consider that PLCs are optimized for running such programs.

Another significant limitation of PLCs which results in decreased performance is a lack of general programming flexibility. While ladder logic provides an effective means of expressing the simple combinatorial logic required for a digital control panel, it doesn't provide an effective means of expressing functions such as analog control, math, PID (proportional plus integral plus derivative) loops, and batch process control. When these functions are implemented on a PLC using ladder logic—typically via patches—performance degrades considerably.

Limited I/O and networking capabilities

In addition to providing poor base-level CPU performance, PLCs and distributed process-control systems offer limited I/O and networking capabilities. Most DCS systems, use proprietary networks within their systems and provide relatively low-bandwidth serial links for communications with external systems.

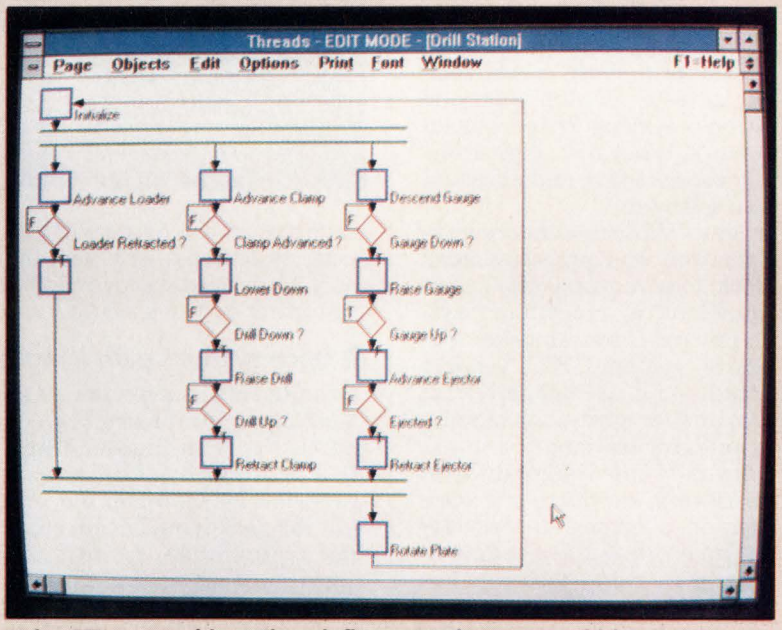
Communications with PLCs must also be implemented via relatively low-bandwidth serial ports. While adequate for polling and controlling simple I/O switches, these low-bandwidth serial connections make it difficult for PLC-based systems to access data from analog I/O sources and to communicate in real time with other computer systems. This, in turn, makes it difficult to incorporate PLCs into real-time closed-loop systems that perform functions such as statistical process control and statistical quality control and derive data from external devices such as bar code readers and machine vision systems.

PLC and DCS vendors have made a half-hearted effort to address the connectivity issue. Many provide communications bridges that link their proprietary serial I/O connections with standard LANs such as Arcnet and Ethernet. Unfortunately, this approach is ultimately constrained by the low bandwidth of the serial connection and the overhead associated with converting between the PLC serial and network protocols. Moreover, these bridges are often very expensive.

As factory applications grow beyond simple control and integrate diverse functions such as machine vision and bar code reading, the need for extensible open systems with diverse data-acquisition, I/O and connectivity capabilities is becoming more evident. Relative to proprietary computers, systems with open architectures such as VMEbus offer several advantages.

First, VMEbus systems provide higher baseline CPU performance, letting designers select from a broader range of standard high-performance CISC and RISC CPUs. Moreover, if a designer's application demands more horsepower, he or she can easily increase the system's performance level by adding more CPUs, all of which communicate with each other via a common high-speed backplane, to the VMEbus rack.

Most PLCs and closed process-control systems, by contrast, are limited to a single CPU. If designers need higher performance, they must string together multiple systems, which must, in turn, communicate with each other via relatively slow serial connections or other LANs.



Using ETI's menu-driven Threads flow control program, which runs on Heurikon's 68030-based VMEbus CPU board under OS/9, factory-automation and process-control engineers can build sophisticated control programs without writing a line of C code.

VMEbus CPUs also boost system-level performance by providing greater flexibility. While PLCs are optimized for executing ladder logic, general-purpose CISC and RISC CPUs can execute a broad range of functions efficiently—in addition to ladder logic. Just as important, they support multitasking, which lets a single CPU execute multiple functions simultaneously in real time. This reduces cost by minimizing the number of CPUs required for an application, and boosts performance by reducing interprocessor communications and minimizing the data that must be moved around the system.

In addition to providing higher baseline CPU performance, VMEbus systems provide higher-performance data-acquisition, I/O and networking capabilities. This is true not only for the devices themselves, but also for the communications channels used to connect the devices with each other and the host CPUs.

In a VMEbus system, the CPU communicates with other CPUs, I/O and data-acquisition devices via a common 40-Mbytes/s backplane. Communications with remote devices are easily implemented by adding network adapter cards for high-speed networks such as Arcnet, Ethernet and even FDDI (Fiber Distributed Data Interface, a 100-Mbit/s fiber optic

LAN). Because the network and CPU cards are linked via a common backplane, data transfers between the VMEbus rack and remote devices can be conducted at the full rated speed of the network.

Probably the most significant advantages of using an open architecture such as VMEbus are extensibility and the widespread availability of third-party hardware and software. With a VMEbus system, designers can select from a limitless array of CPUs and coprocessors, graphics and imaging devices, I/O, networking and data-acquisition boards, and specialized control functions. They can also select from a wealth of software products, including real-time operating systems, compilers, cross-development tools, debuggers, and vertical application packages. This selection makes it easy to modify and upgrade a system, and reduces dependence on a single vendor.

The wide selection of hardware and software also helps to make the market more competitive and create economies of scale, both of which help keep prices down. Typically, a distributed control system based on off-the-shelf hardware and software costs about 60 to 80 percent less than an equivalent proprietary system from a DCS vendor.

A proprietary DCS operations console, for example, costs between $50,000 and $80,000. A Sun workstation with an off-the-shelf process-control package, by contrast, costs about $15,000 and delivers equivalent—or better—functionality and performance. Similarly, DCS vendors charge between $250 and $400 per analog or digital I/O point. An open systems vendor, by contrast, offers the same I/O for from $50 to $100 per point.

While the migration to open systems is inevitable, PLC and DCS vendors are for the most part making only half-hearted efforts to unbundle their systems. Some DCS vendors, for example, now let customers use a DEC or Sun workstation as an operations console and development platform. They have yet to open up their backplanes, however, maintaining a firm hold on the front-end control and I/O functionality. PLC vendors have been somewhat more willing to open their systems.

The missing link

To capitalize on the opening left by proprietary systems vendors, VMEbus vendors will have to simplify the migration path and provide an integration and development environment more akin to that offered on the PC. That means delivering interoperable hardware and software components that can be installed without writing C code (for example, to select address maps and interrupt vectors) and that offer integration and debug assistance when users encounter roadblocks. It also means offering vertical factory-automation and process-control software that's comparable to what's offered with closed systems and that can be used by engineers with little or no programming experience.

Because of the diversity of its CPU, I/O and operating system options, VMEbus systems may never provide the seamless plug-and-play environment offered by the PC. Progress is being made in several areas, however. Interoperability problems, for example, are diminishing as more sophisticated VMEbus systems are deployed in the field and vendors take a greater role in the system-integration process.

Significant progress is also being made in the area of standards, particularly with regard to device drivers and application interfaces. Today, one of the most significant obstacles to simplifying integration in the VMEbus market is a lack of standardization among real-time operating systems, both at the device and application levels.

To help simplify the task of system integration, while preserving the versatility offered by the wealth of real-time operating systems, new standards are being developed that will provide common device driver and application interfaces. The device driver standard, known as OBIOS (Open Basic I/O System), will create a common set of I/O system calls that will enable a single device driver to work with any OBIOS-compliant operating system. Similarly, Posix will provide a common set of application-level system calls that will enable Posix applications to run on all Posix-compliant real-time operating systems.

The emergence of efficient Posix-compliant real-time Unix operating systems may simplify matters even more by letting designers develop and execute applications on a single system. The emergence of efficient real-time Unix will also reduce the need for proprietary real-time operating systems and will unite the industry around a single dominant operating system standard—just as DOS did in the PC world.

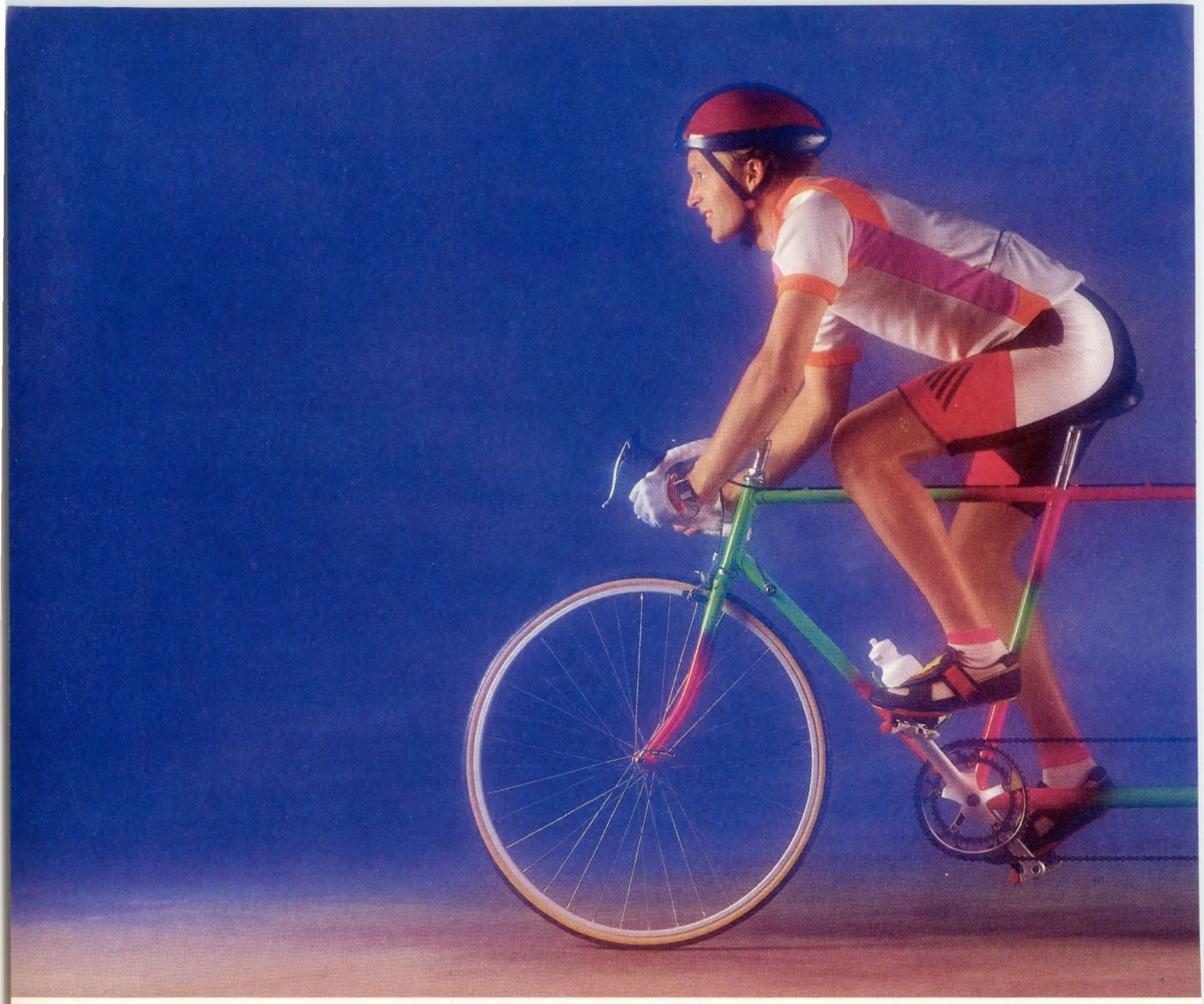
In the past, poor real-time performance has limited the use of real-time Unix. With the performance and efficiency of real-time Unix approaching that of proprietary kernels, however, the future of the latter may be short-lived. The Posix standard, which is heavily based on Unix, is a harbinger of this trend.

More powerful tools

To really entice engineers who are used to turnkey development environments, VMEbus vendors are going to have to offer comparable environments. In addition to the assemblers, compilers, bundled real-time operating systems, and cross-development tools, VMEbus vendors will have to provide vertically integrated software packages that use familiar process-control terminology and can be quickly mastered by engineers with little or no programming experience.

Some of these vertically oriented application packages are beginning to emerge. A good example is Event Technology's (Indianapolis, IN) family of CASE tools. Available for a wide variety of open systems, the tools currently run under OS/9 on Heurikon's 68030- and 68040-based CPU boards. A port to Heurikon's HKLynx real-time Unix is planned for the near future.

With the ETI CASE tools, engineers with no previous programming background can quickly build sophisticated distributed process-control systems. Using the icon editor, designers build applications by selecting objects with a mouse, popping them up on the screen and interconnecting them to define control relationships. Objects may be selected from a library of preexisting objects including PID controllers, ladder logic, an ISA symbol set, coils, contacts, timers, and analog inputs and outputs. Designers can also create their own objects.



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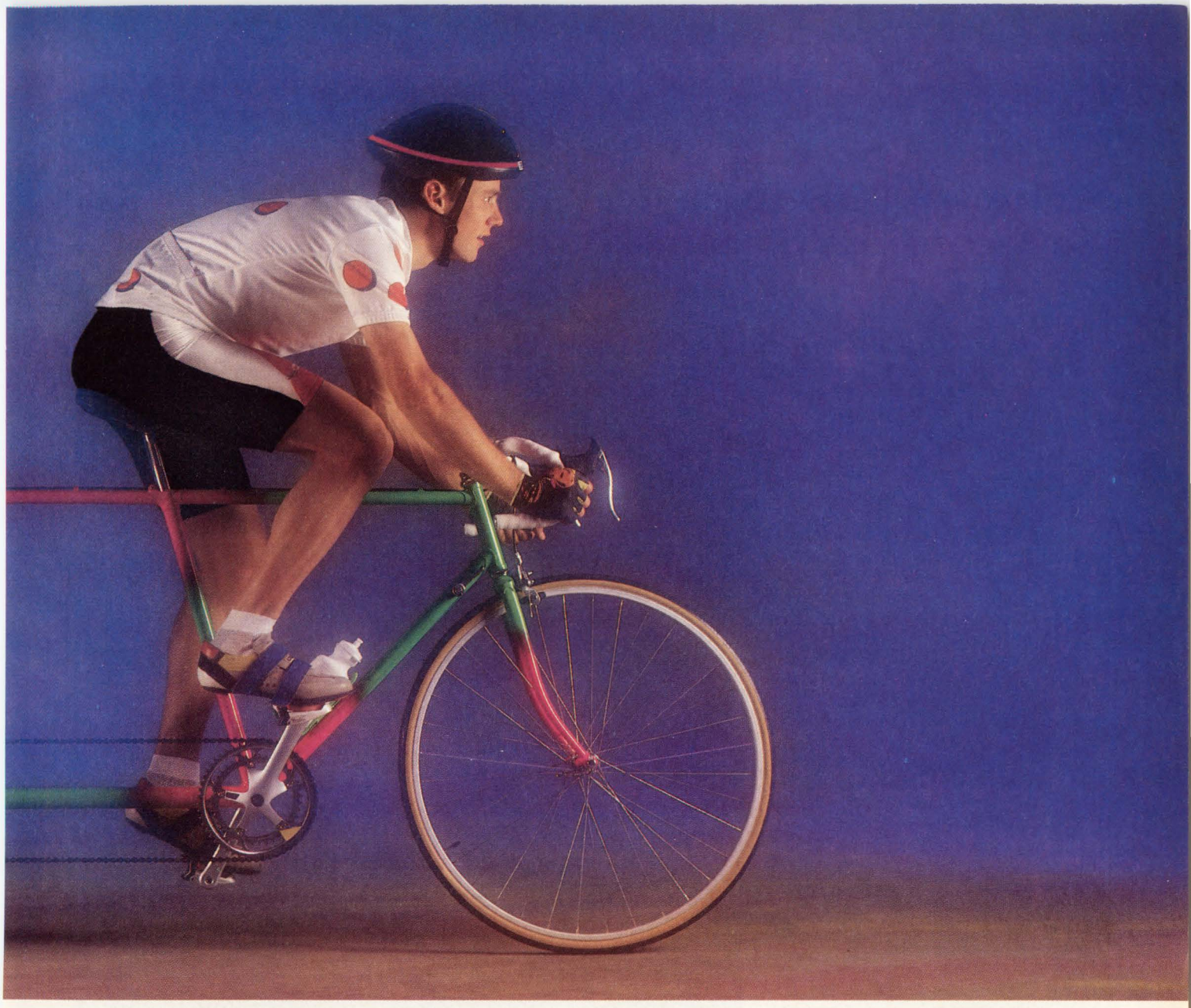

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CAE/CAD TOOLS

Complex PCBs force designers to reconsider placement tools

Mike Donlin, Senior Editor

To bolster their arguments, CAE vendors cite statistics showing that when a PCB is only 20 percent complete, about 80 percent of the decisions have been made that will affect the final product's performance and cost. It stands to reason, they argue, that CAE can help a designer choose and place components on a board and ensure that the needs of the other design disciplines are taken into account when these early, critical decisions are made.

Designers have resisted what they consider to be this "Big Brother" approach, arguing that human expertise is too formidable for any CAE tool to rival. But as PCBs get more complex and clock speeds exceed 50 MHz, design constraints are getting far too numerous for engineers to consider, and many of the man-versus-machine arguments start to favor the machine.

"Layout engineers and mechanical designers are running into the electrical impacts of their decisions," says Shiv Tasker, vice-president of marketing for packaging and interconnect at Cadence Design Systems (San Jose, CA). "It's impractical for them to learn electrical engineering, and the electrical engineers don't have the time to learn mechanical engineering. The solution to this dilemma is smarter tools that can guide the decision-making process."

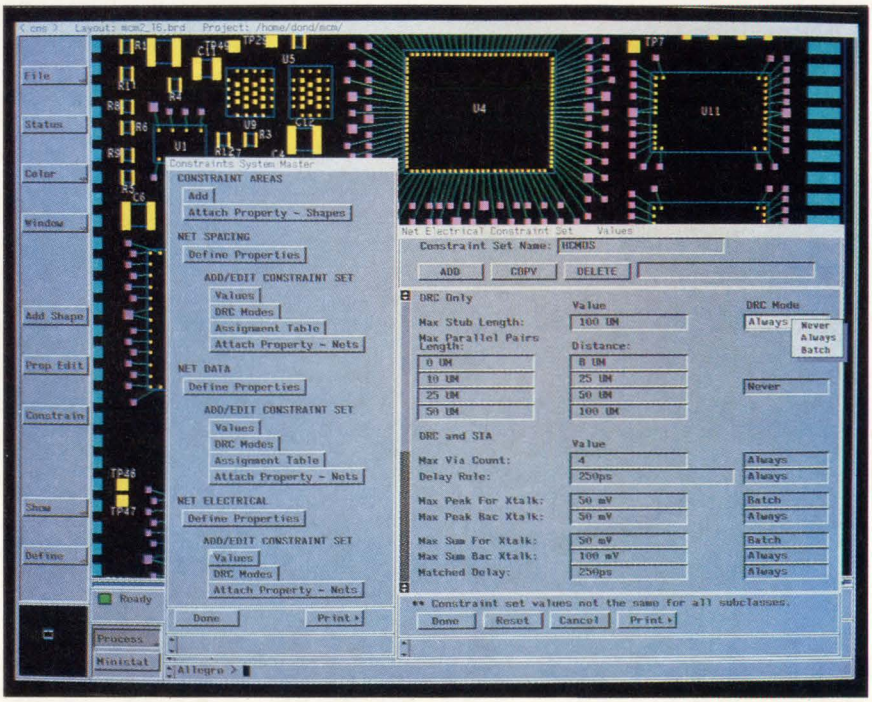
Layout system for PCBs

To this end, Cadence has just unveiled Allegro CBD (Correct By Design), a layout system for PCBs, multichip modules (MCMs), hybrids, and multiwire boards. The first product released since Cadence merged with Valid Logic Systems, the tool assigns design and technology constraints early in the design process and enforces them throughout the development cycle. These constraints are grouped into sets according to the types of elements they control. Specific constraints could be geared toward manufacturing or signal-to-noise ratios, for example, and would address component spacing restrictions required by board assembly equipment or net impedances, timing and allowable noise to ensure signal integrity.

While the concept of a constraints-driven layout tool separates Cadence's product from many post-layout analysis tools you could buy, it also might prove unsettling for those of you who believe that a computer can't bring the same intuition and experience to the design process that an engineer can. This isn't to say, however, that PCB design complexity is going unnoticed.

"PCBs are exhibiting all kinds of effects that make them difficult to place and route," says John Umina, president of ProDesign (Newton, MA), a PCB design bureau. "And if the EDA vendors improve their tools, I'm sure we'll use them. But right now, placement tools have a hard time just getting all the components on the board where they belong. We're working on an analog design, for example, where each component must be placed precisely to get all the lines the correct length. At present, that's still best handled with engineering expertise."

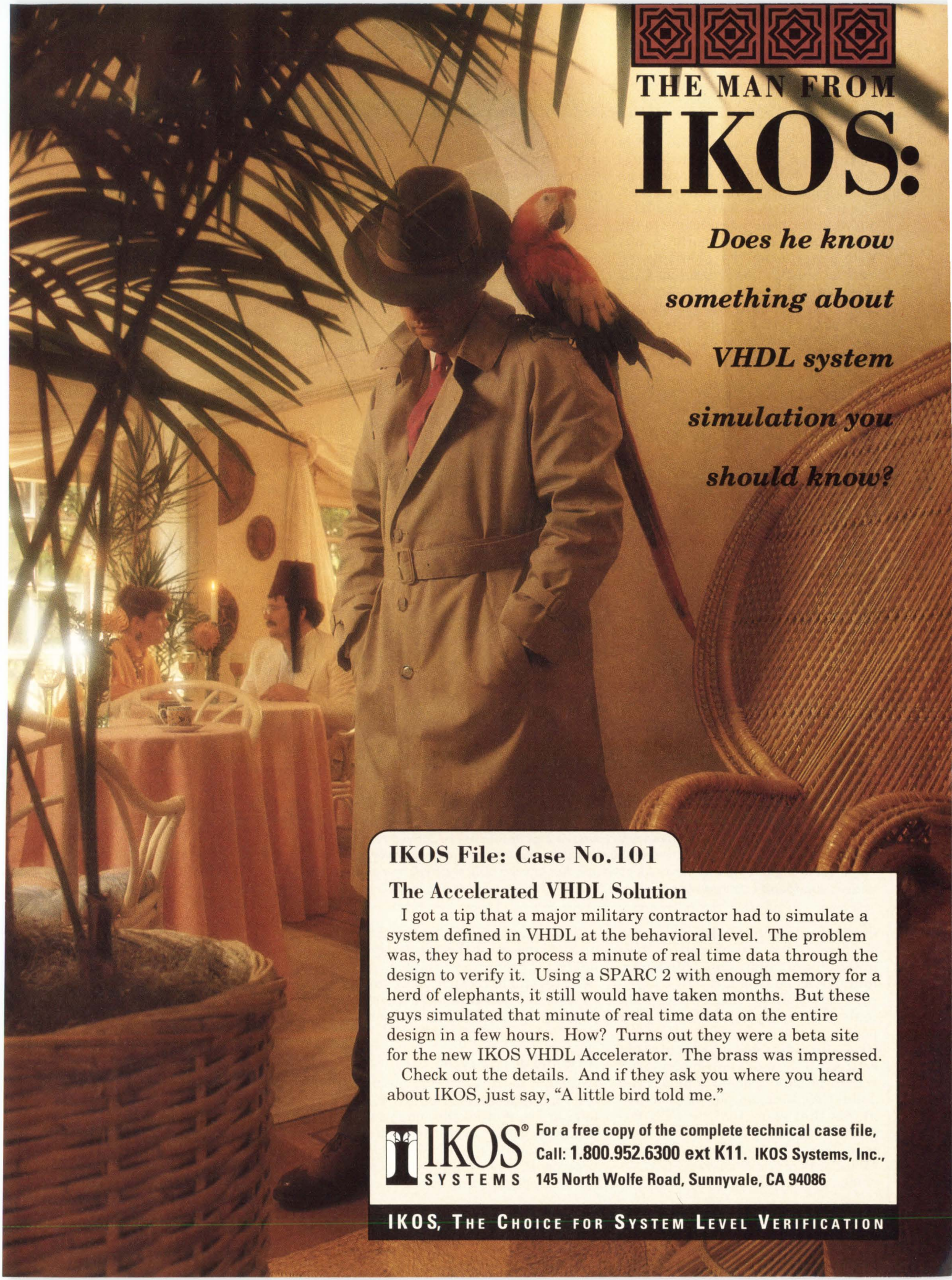
Though vendors such as Cadence hold out the promise that their placement tools can incorporate complex design rules into the layout process, many designers are wary of the possible setup time that such a tool might require. "Most of the placement tools I've seen can give a designer a part for placement that has the most connections to the components that are already placed on the board and that's helpful," Umina says. "But if a tool is hard to use, engineers are always going to prefer placing things by hand."



With the Allegro CBD Constraints Editor from Cadence, design and methodology definitions are established at the outset of the product-development cycle to drive all layout functions and ensure correct design. Stored in EDIF-like syntax, these constraints provide design process control. As illustrated on this screen, constraints may be always enforced, deferred or not enforced at all.

Easy and fast

EDA vendors are answering these objections in two ways. First, by incorporating window and spreadsheet interfaces, they promise to minimize the learning curve associ-



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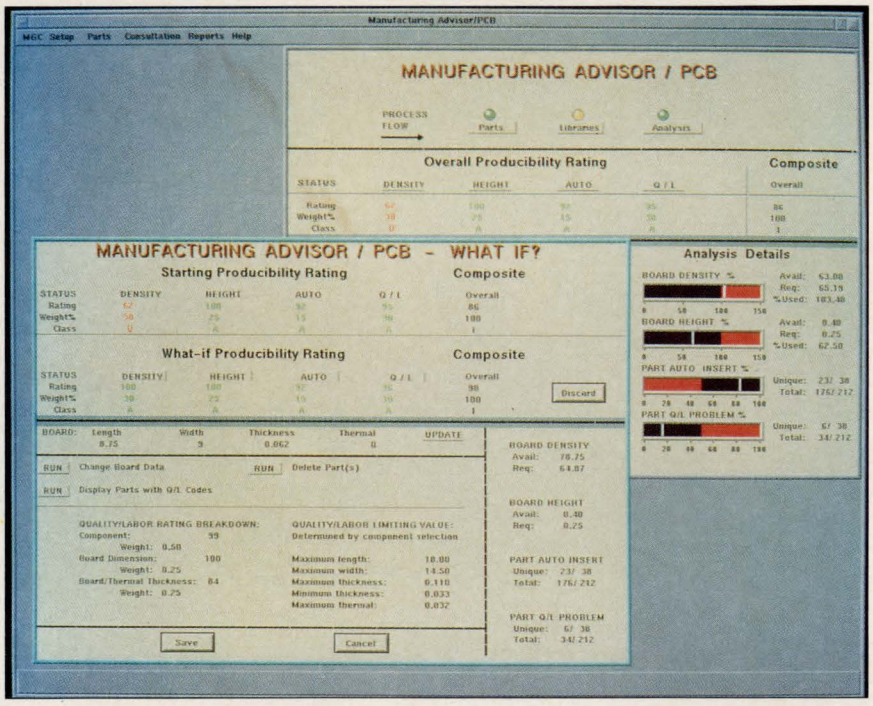
CAE/CAD TOOLS

ated with CAE tools. The Visula PCB design tool from Racal-Redac (Mahwah, NJ), for example, uses an Open Software Foundation Motif-like user interface with a "tool bar," making the system accessible to the casual user. You can perform any Visula operation by selecting an item on the bar and calling up a list of permissible operations on that item. You can then set, review and control the parasitic parameters of the design. According to Racal-Redac, this option can give you immediate access to all design, analysis, layout, and manufacturing tools in the environment suite with a minimum of learning effort.

In addition to ease of use, EDA tools are applying raw compute power to the tasks at hand, effectively turning aside arguments that setting up the tool's parameters isn't worth the time. Pacific Numerix (La Jolla, CA), for example, cites benchmarks that show that its PCB Explorer tool can place a 250-component board in less than a minute. "That placement carries with it rules for signal integrity, thermal and fatigue analysis," says John Roth, vice-president of sales and marketing at Pacific Numerix. "So it certainly seems worth any time spent setting up a list of priorities previous to running the tool."

No matter how complex PCBs get or how much assistance EDA vendors want to render, one thing is clear—designers are never going to be satisfied with a purely automatic tool that removes them from their designs. Constraints editors, placement tools and autorouters must be selective in removing that authority or they will surely be rejected by the design community. Cadence has been careful to retain that flexibility in its new Constraints Editor by letting constraints always be enforced, deferred or not enforced at all.



In the Manufacturing Advisor/PCB by Mentor Graphics, the overall analysis window in the background includes initial manufacturing ratings in four areas. The red text in the density column indicates a critical problem with component placement density. The sheet in the foreground shows that the user has interactively tested design alternatives and found a solution as seen in the "What-If Producibility Rating" window.

Up the design cycle

Although battles are still raging on the PCB placement front, EDA vendors are convinced they can provide compute power even earlier in the design engineer's decision-making process. Prior to placement, designers make decisions about component selection based on size, power consumption, availability, cost, and reliability. As the component count for PCBs increases, the complexity of these decisions also grows.

One product that addresses this problem is the Manufacturing Advisor/PCB from Mentor Graphics (Wilsonville, OR). The tool informs you about parts-related manufacturing problems during component selection. You can use the tool to perform "what-if" analyses to test the effects of recommended design alternatives. Prior to beginning schematic capture, you can enter a parts list and perform a preliminary analysis. As components are added to a design, the tool monitors the consumption of the available placement area and, if exceeded, will identify those components that could be mounted in an alternative configuration with a smaller footprint.

Mentor hopes that, as tools such as the Manufacturing Advisor infiltrate the domain of the design engineer, they will filter down through the placement, routing, test, and manufacturing stages of PCB development and set the stage for EDA's acceptance in all those areas. The issue is primarily one of trust, because designers live and die by how well their ideas are translated to working products, not by how well they've embraced EDA.

"There will always be people who won't believe that automatic tools can ever best a human designer," says Ralph Zak, director of marketing for Mentor's PCB division. "But on a board with 400 components and high-speed clock lines, the design rules can get overwhelming in a hurry. EDA vendors have to remember, however, that the object isn't getting high performance from a lot of tools, it's getting high performance from the circuit." ■

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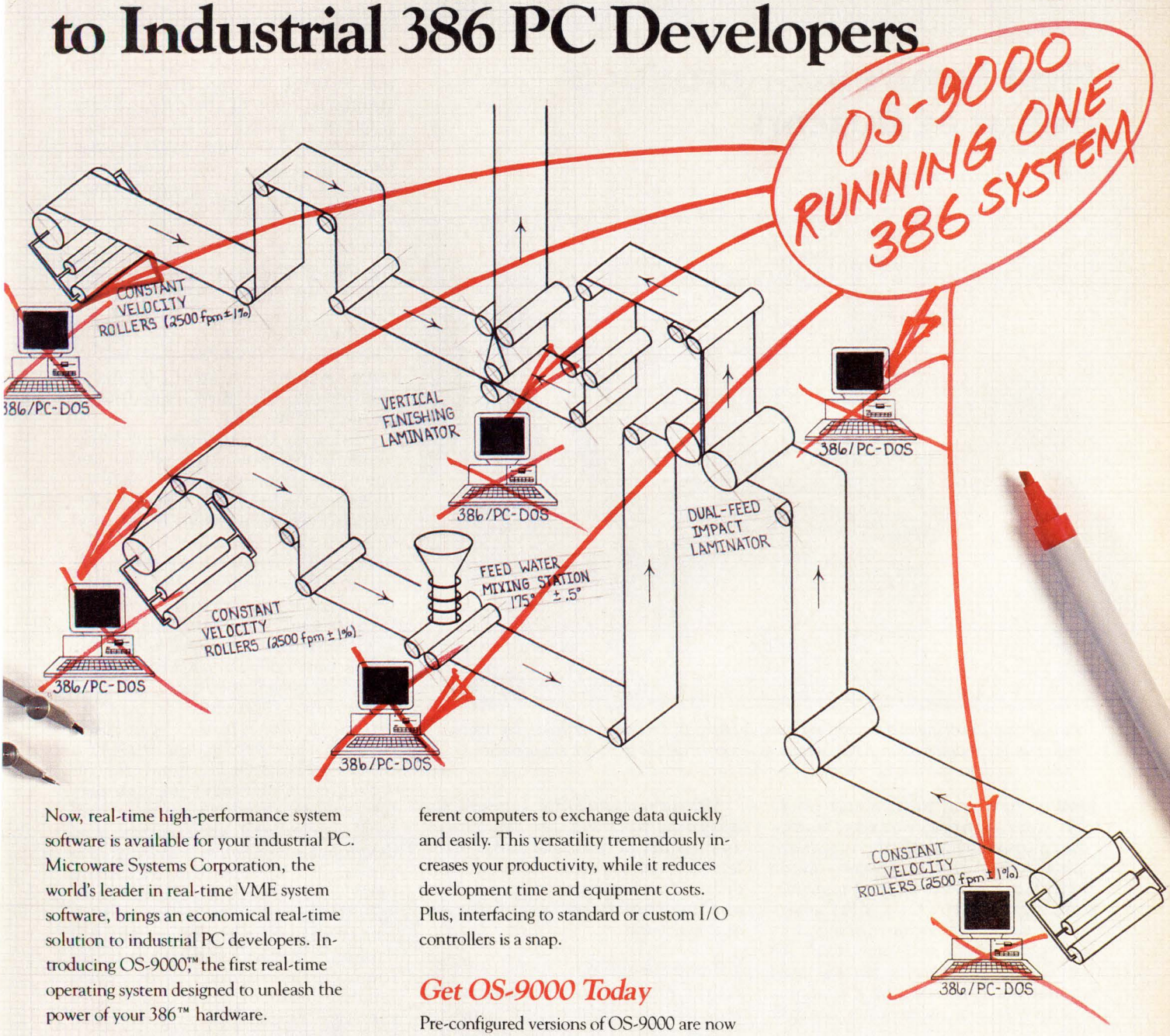

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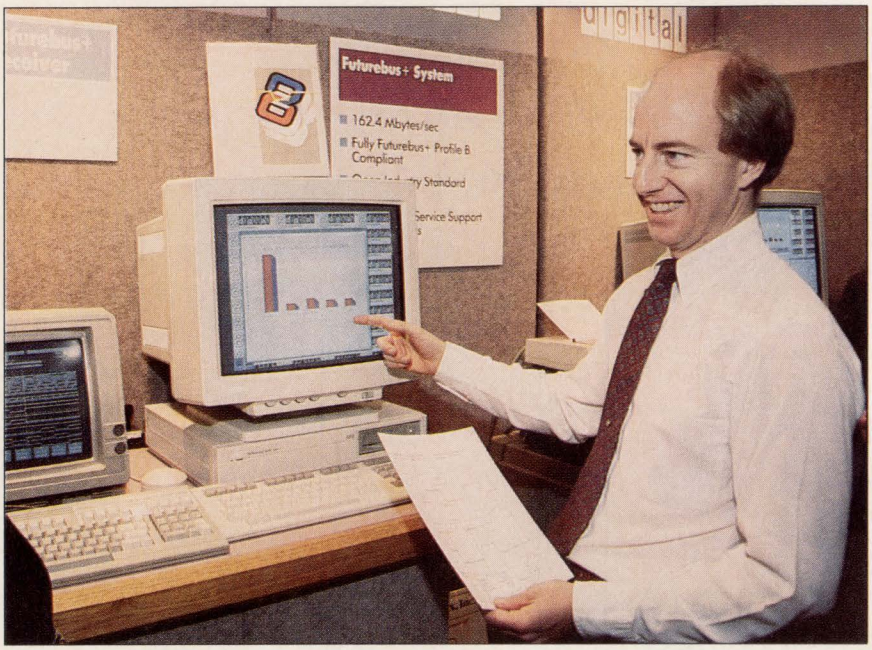
First Futurebus+ products debut at Buscon

Warren Andrews, Senior Editor



Digital's Jim Duval mans the company booth at Buscon. According to Duval, the major ingredients needed to launch Futurebus+ as a successful bus platform are present.

The first real Futurebus+ products—chips, boards, backplanes, systems, development platforms, and software—made their debut in February at a special showing hosted by the VME/Futurebus+ trade association during Buscon '92 West (Long Beach, CA). All told, some 20 manufacturers lined up to show their available products and, in many cases, to announce new ones.

Almost two years ago, Digital Equipment Corporation (Maynard, MA) joined with a number of other companies at the Futurebus+ roll-out, but the specification was incomplete at that time and there was no hardware to show. Now, says Jim Duval, DEC's Futurebus+ program manager, the major ingredients needed to launch Futurebus+ as a successful bus platform are present. The main ingredient is a solid specification, well defined in the IEEE-896.1 Protocol document and the A, B and F profiles in the IEEE-896.2 Physical Layer and Profiles document.

The other essential ingredients, according to Duval, are commercial availability of interface and controller ICs, boards from different vendors, a development platform for bus and applications analysis, software, and systems.

Premiere event

One highlight of Buscon was the world premiere of a complete DEC computer system using a fully operational Futurebus+ (Profile B) as the I/O bus. The premiere was doubly remarkable for unveiling the company's latest developmental RISC microprocessor, Alpha. The architecture of Alpha was disclosed later in the month at the International Solid State Circuits Conference (San Francisco, CA).

In addition to its main computer system, DEC demonstrated other products based on Futurebus+ technology, including a network router and communications and storage controllers.

Not to be outdone, Raytheon (Lexington, MA) displayed a high-performance workstation based on the Futurebus+ and Safenet open standards. One of the original contractors in the Navy's NGCA (Next-Generation Computer Architecture) program, Raytheon expects to launch a full set of commercial ventures in the immediate future.

For want of a chip

Handling the bus interface and board controller functions on Futurebus+ boards are chips from National Semiconductor (Santa Clara, CA), Newbridge Microsystems (Kanata, Ontario), Signetics (Sunnyvale, CA), and Texas Instruments (Dallas, TX).

National, the inventor of backplane transceiver logic (BTL) and one of the pioneers in Futurebus activity, announced increased performance levels for its existing data and handshake transceivers. The hardware now boasts typical propagation delays as low as 3 ns. In addition, the company announced its first protocol controller chip, the DS3805. The chip was codeveloped with Newbridge and will be marketed and promoted by both companies.

Until now, National has been reluctant to offer a protocol controller because the specification was still fluid. Phil Hughes, National's worldwide product manager for high-performance bus products, says the protocol controller's architecture was developed in response to real system needs, not those perceived during early revisions of the preliminary specification. The National controller is designed to implement the full Profile B protocol and has many of the hooks needed for Profile A compliance. National has not yet implemented the noncompelled, or packet, mode in its controller ICs. Hughes says the company is waiting until the specification is completed before building silicon. "This will save us and the board designer a lot of problems going forward," he adds.

National's chips are already appearing on boards; the company showed products from at least a half-dozen board makers who were using its silicon. Among them was a DEC board from its Hastings network controller project.

Signetics and its second source, Texas Instruments, were also much in evidence. Signetics was showing off its family of interface chips, com-

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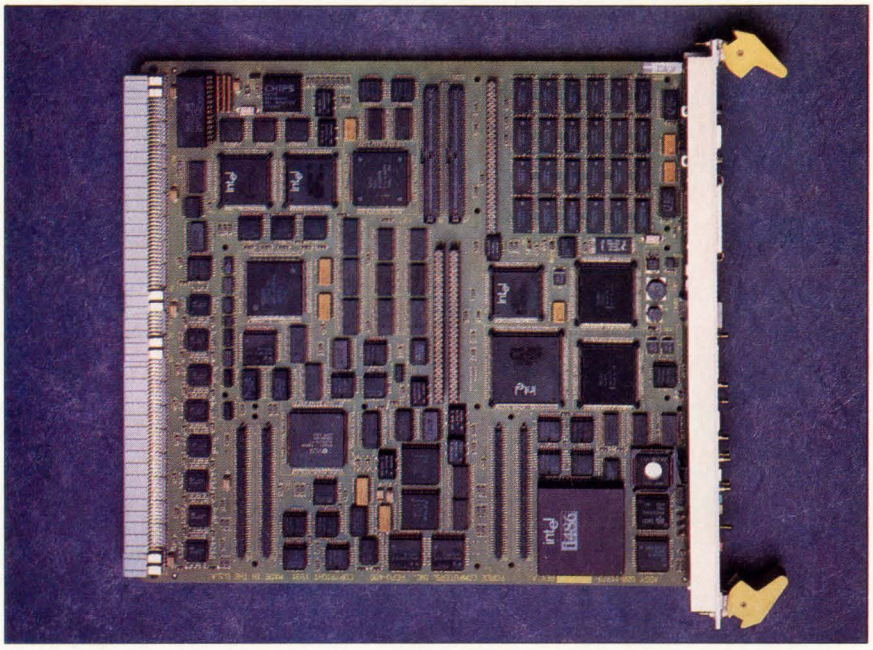
pelled and noncompelled parallel protocol controllers, arbitration controller, packet-data FIFO, and 7-, 8- and 9-bit transceivers. Similarly, TI announced a family of devices including an arbitration bus controller and I/O controller, as well as transceiver products. TI expects to start sampling these parts during the first half of 1992.

as a subcontractor to Litton, for whom Force developed an Intel 80486-based CPU board. What Force has come up with for the commercial market appears to be more than what was called for by the NGCA project. Its FCPU-486 module is a general-purpose single-board computer that can take advantage of all PC- and MS-DOS



Force Computer's FCPU-486 offers the advantages of an 80486 set up for multiprocessing and supporting up to 14 modules. The big thing, though, is that it's equipped with a Futurebus+-compatible PC BIOS to directly run any PC- or MS-DOS application. It can also run any PC/Unix software. And, if that's not enough, it includes a full EISA interface and connectors for two or four EISA/ISA boards, in addition to hard and floppy disk, Ethernet, serial, and SCSI interfaces.

Board makers are playing a key role in the Futurebus+ saga. At least four of the leaders, as well as some backplane makers offering wire-wrap prototypes, were represented at Buscon. Three of these have been prime or subcontractors in the Navy's NGCA program.

Boards and backplanes

CCT (Anaheim, CA), an early prime contractor to the Navy, has quietly developed its Futurebus+ products and now offers CPU boards based on Motorola's 680X0, AMD's 29000 and Intel's i860.

Force Computers (Campbell, CA), the only mainstream VMEbus board maker to announce a Futurebus+ product at the show, was also involved in the Navy's NGCA project

software—or it can run using PC/Unix software with no emulation because it uses a Futurebus+-compatible PC BIOS.

One of the keys to the board is that it offers multiple bus interfaces. On the Futurebus+ end, it conforms to both profiles A and B. But it also offers an EISA bus interface, as well as a choice of either two or four EISA/ISA expansion slots, which directly accept standard ISA/EISA cards. In addition, the board includes a high-performance Ethernet interface as well as a SCSI port. It also includes IDE hard and floppy disk interfaces, a serial interface, support for VGA graphics, and keyboard and mouse interfaces. Force is also offering a chassis and two different subracks.

Nanotek (Idaho Falls, ID), the first board maker to show a prototype Futurebus+ board, introduced a family of four different boards. Its processor module features a 25-MHz R3000 processor with an R3010 coprocessor to provide 20 Mips throughput. The board also includes 64 kbytes each of data and instruction cache, a secondary data/instruction cache of 2 Mbytes, 2 Mbytes private RAM, 4 Mbytes global RAM, 1 Mbyte of flash memory, timer clock, and serial ports.

Nanotek's other products include an interface module designed to provide a complete Futurebus+ interface for customization by users to support various applications. It offers a simple synchronous user interface, 32- and 64-bit data paths, 32-bit addressing, I/O through the backplane and mezzanine controller, and I/O interfaces. In addition, Nanotek offers a profile A and F arbitration module and a memory module providing up to 64 Mbytes of memory using 4M × 1, 80-ns fast-page-mode DRAMs.

Antel (Plano, TX) also offers a Futurebus+ memory card that provides expansion capability to 512 Mbytes (when 16-bit DRAMs become available). The memory module is designed to offer high-performance storage for compelled-mode Futurebus+ transactions. It supports 32- and 64-bit compelled transactions and is compliant with the A, B and F profiles. The module performs locked transactions with the memory start address configured through a control and status register (CSR). It may be defined on any 64-kbyte boundary within a 4-byte block.

Key components

The 2.0-mm connector specification has brought out the connector and tooling makers, all looking to participate in the growing Futurebus+ business.

Amphenol (Wallingford, CT) showed its high-density MeMs (Metric Modular System) series of board connectors. AT&T (Berkeley Heights, NJ) introduced the Futurebus+ subset of its Metral family of connectors. CECO Interconnect Products (Camarillo, CA) displayed its Micro-EYE right-angle receptacle press-fit Futurebus+ modules, boasting low insertion force and a

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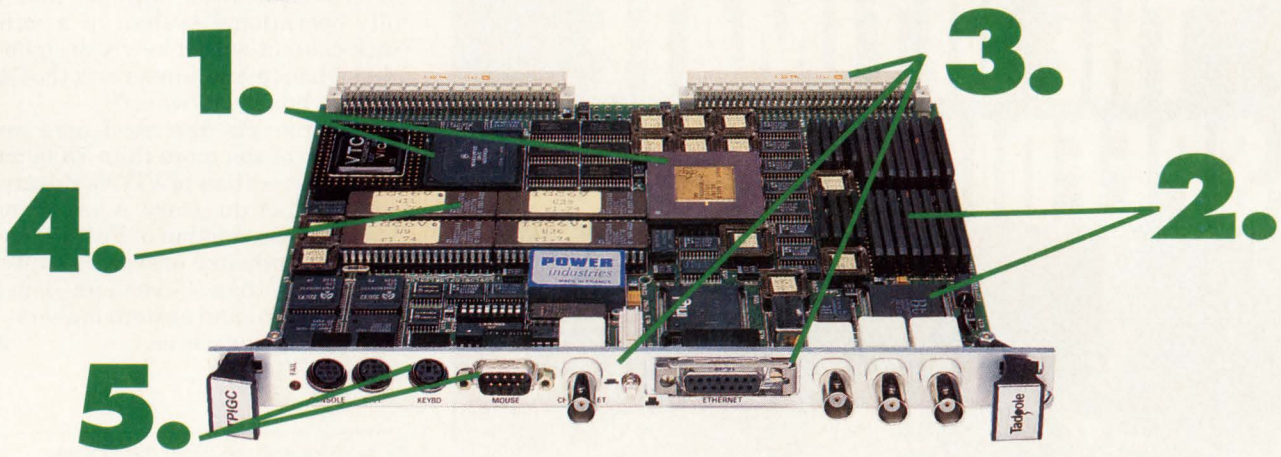

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tightly aligned tail for fitting the connector to a PCB.

DuPont (Wilmington, DE) displayed its Metral line of Futurebus+ products, which it claims is a minicoax connector system allowing more than 100 coax lines to be connected to a single, double-height Eurocard. The Tempus connectors from ITT Cannon (New Britain, CT) provide a scalable connector for anything from a 32- to a 256-bit bus. It's unique in its fabrication, yet is designed to mate with other Futurebus+ 2.0-mm connector systems.

Futurebus+ backplanes were represented by BICC-Vero (Hamden, CT), Hybricon (Ayer, MA), Mupac (Brockton, MA), and Schroff (Warwick, RI). All four companies showed high-performance Futurebus+ backplanes, subracks and enclosure systems. Highlights included BICC-Vero's backplane, designed for handling data at Profile F speeds; Hybricon's system enclosure, made for applications calling for 128-bit Futurebus+; wire-wrap development boards from Mupac; and a fully operational system in a minirack cabinet with a newly designed 14-slot backplane supporting the 64-bit data bus from Schroff.

The products described here are but a few of the more than 75 listed in the first edition of VITA's Futurebus+ product directory. A year from this first introduction of Futurebus+ products, industry observers expect to see more than 75 vendors—most of them board and system makers—offering similar wares. ■

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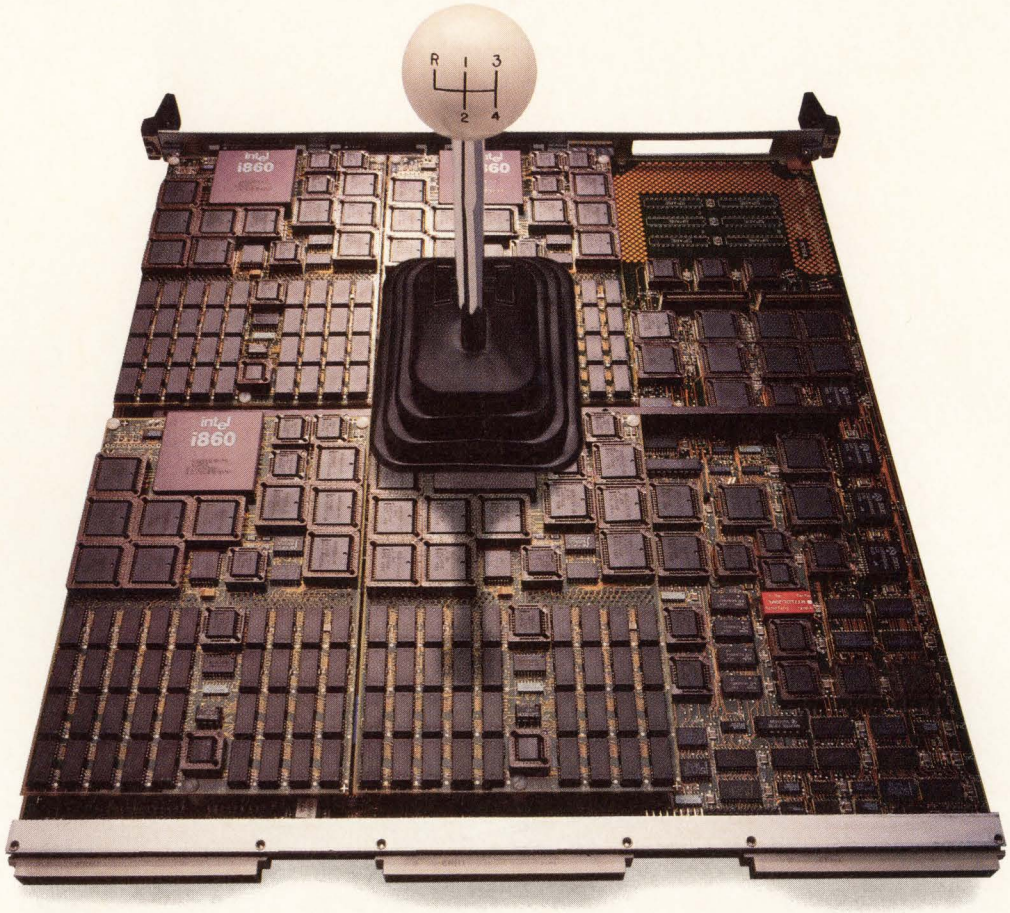

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VHDL: Standardizing a standard

Barbara Tuck Egan, Senior Editor

VHDL's relatively short development cycle has created a situation where expectations about its readiness to function as a fully useful and effective language have not been met. We tend to forget that VHDL's creation as a baseline standard was heavily funded by the government, with dedicated contractors working on it around the clock. But the government is contributing very little to the job of creating the guidelines and ancillary standards now required to give infrastructure to that baseline standard. It's leaving the job to the IEEE and VHDL International.

Moe Shahdad, chairperson of the IEEE VHDL standardization steering committee and a founding director of VHDL International, says, "Designers can use VHDL today, but broad market acceptance won't occur until infrastructure standards are developed. For the VHDL user base to expand, the IEEE and VHDL International have to work together to give users validation suites, benchmarks, guidelines, and standards."

Simulator certification

Toward that end, the Technical Advisory Committee of VHDL International is attempting to validate the credibility of the language by separating language standardization from tool standardization. The very flexibility of VHDL has led to simulators that might or might not comply with the full specification, to various logic value systems for ASIC library models, and to different methods of backannotating ASIC vendors' timing delay information. This diversity has been enough to confuse designers who have been encouraged to embrace VHDL for its portability and model interoperability.

By year's end, VHDL International should have a simulator certification program in place, according to the chairperson of the Technical Advisory Committee, Dave Coelho, who is also executive vice-president at Vantage Analysis Systems (Fremont, CA). A proposal for this program is being examined for final approval by the board of VHDL International, and preliminary discussions are underway with university groups being considered as neutral third-party administrators. "The idea of the program," says Coelho, "is to alleviate the confusion of users who don't know enough about VHDL to test the simulators themselves."

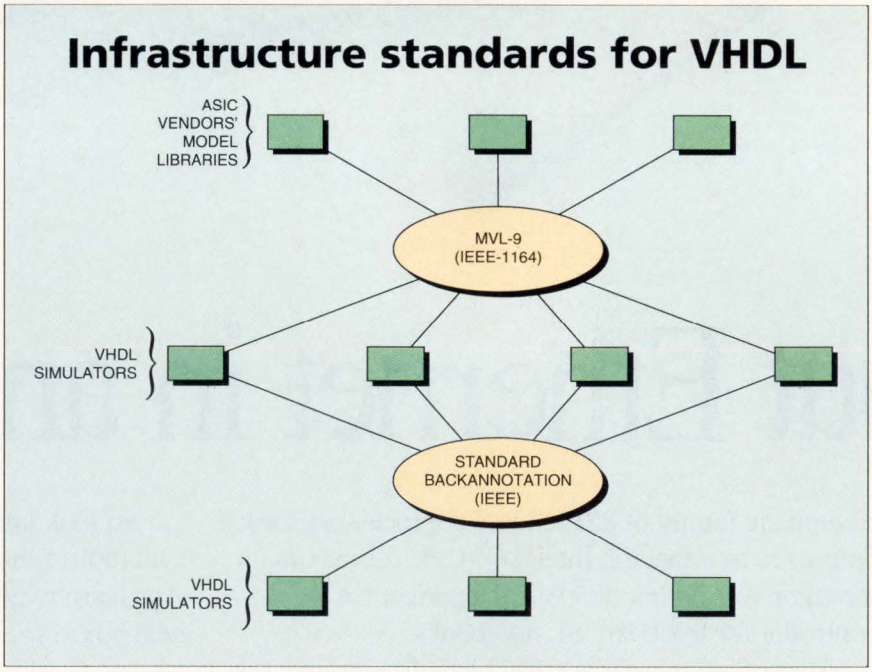
Until now, VHDL simulator vendors have provided a percentage figure to describe the degree to which their tools comply with the language. That's not enough information for users, who need to know if the simulators will or will not solve their problems, according to Coelho. Under the simulator certification program, a vendor's tool will be run through a validation suite of thousands of test cases written in VHDL.

Not a competitive benchmark

The test suite will measure a simulator's understanding of all VHDL constructs and permutations, not its run-time performance. "VHDL International is absolutely going to stay away from competitive benchmarks," says Coelho.

The second goal that VHDL International is addressing through the Technical Advisory Committee is to make model interoperability a reality by adopting a standard VHDL modeling methodology. As is the case with simulator implementation, the flexibility of VHDL has been a mixed blessing when applied to models. ASIC vendors and modeling houses have developed their own modeling techniques, so when designers secure models from multiple sources there's a high risk the models won't communicate with one another. Although there are data-type translations that can be used when working with different value systems, Coelho explains that they're very awkward and information can be lost in the conversion.

"There's very strong support to adopt the IEEE-1164 or the nine-level standard for multivalued logic (MVL-9) currently being balloted," reports Coelho. Almost every major VHDL simulator vendor is represented on the Technical Advisory Committee. "With that kind of clout,"



The IEEE and VHDL International are creating the guidelines and ancillary standards needed to make VHDL a fully useful and effective standard. Not until the industry ratifies a standard logic value system for ASIC vendor libraries, sets up a simulator certification program and adopts a standard methodology for backannotating timing delays will portability and model interoperability become realities of VHDL.

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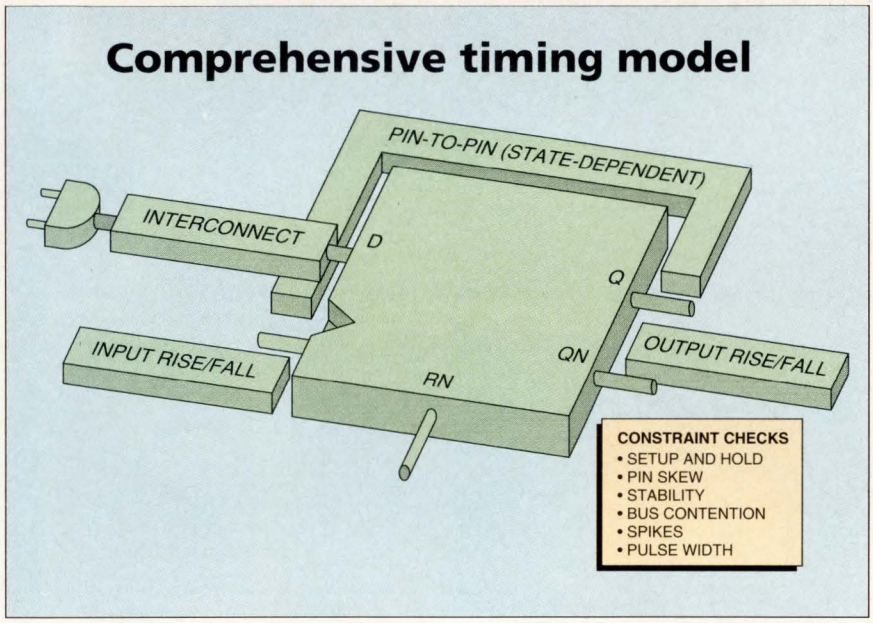
he says, "we should be in good shape to encourage the ASIC vendors to support the IEEE-1164 standard." Many ASIC vendors and third-party houses have hesitated to develop VHDL libraries in the absence of a standard modeling methodology. Once the standard is ratified, Coelho predicts that vendors will fall in line very quickly behind it.

That seems to be the case with VHDL International member LSI Logic (Milpitas, CA). Product marketing manager Susan Runowicz-Smith says that LSI Logic expects to endorse the MVL-9 standard as soon as it's ratified. In fact, Runowicz-Smith reports that, in a dramatic deviation from its position up until now, LSI Logic will make its ASIC library models available in source-level form to the public once MVL-9 becomes a ratified standard. Currently, most LSI Logic models are supported in protected form and can be accessed only through the company's own tools.

"Any tool that complies with VHDL," explains Runowicz-Smith, "will be able to compile and use LSI Logic's source-level models for any application. This will free us from doing another design kit for every new tool that comes out."

Offering a European perspective, Jacques Rouillard of the Institut Mediterraneen de Technologie (Marseille, France) enthusiastically supports the adoption of MVL-9, though there are trade-offs involved. Rouillard explains that, of the nine logic states of MVL-9, the states that might be criticized are X (conflict) and U (uninitialized), which have meaning for simulation, and D (don't care), which has meaning for synthesis only. "It may seem strange to have all these values in the same set, and to be obliged to discard one or the other depending on the application domain—synthesis or simulation," says Rouillard. "Moreover, the don't-care state is implemented in other languages such as Verilog as an algorithmic shortcut, not as a value in the value system. But it's all a matter of trade-offs."



Mentor Graphics' Advanced Modeling Process (AMP) lets QuickSim II model the full complement of delays required for submicron accuracy. The model specification resembles the ASIC vendor's data sheet representation. You can interactively select which delays and constraint checks to execute at any point in your simulation. Mentor would like AMP to become an industry-standard modeling specification.

Backannotating delay data

A major new effort of VHDL International's Technical Advisory Committee stems from its recent decision to officially sponsor the IEEE working group formed to develop a neutral format for transmitting ASIC vendors' technology-specific delay information in a simulator-independent manner.

Coelho reports that VHDL International will be donating people power and technical talent to the IEEE committee chaired by Vassilios Gerousis, manager of CAD system evaluation at Motorola's ASIC Division. When the committee meets, it will entertain several alternative proposals for a standard methodology for backannotating delays.

Once the IEEE committee has defined its goals and objectives, Mentor Graphics (Wilsonville, OR), also a member of VHDL International, will most likely release its Advanced Modeling Process (AMP) technology to the committee for consideration as a standard, according to Glenn House, Mentor's marketing manager for simulation and modeling.

Mentor has reduced the need for several different libraries by making its AMP modeling technology common across all its tools, including simulation, synthesis, timing analysis, and fault analysis. House says that Mentor won't push for a generic standard if the committee's sole intention is to make it generic. "It has to be a benefit to the customer," he insists. "We don't want to design yet another modeling strategy for sport."

The IEEE-1164 or MVL-9 value system for modeling is expected to be ratified as a standard long before the standardization of a methodology for backannotating delays. But Coelho says that users will be able to begin mixing and matching models as soon as MVL-9 is ratified, though they'll have to use different interfaces to pass timing information from layout to simulation tools. ■

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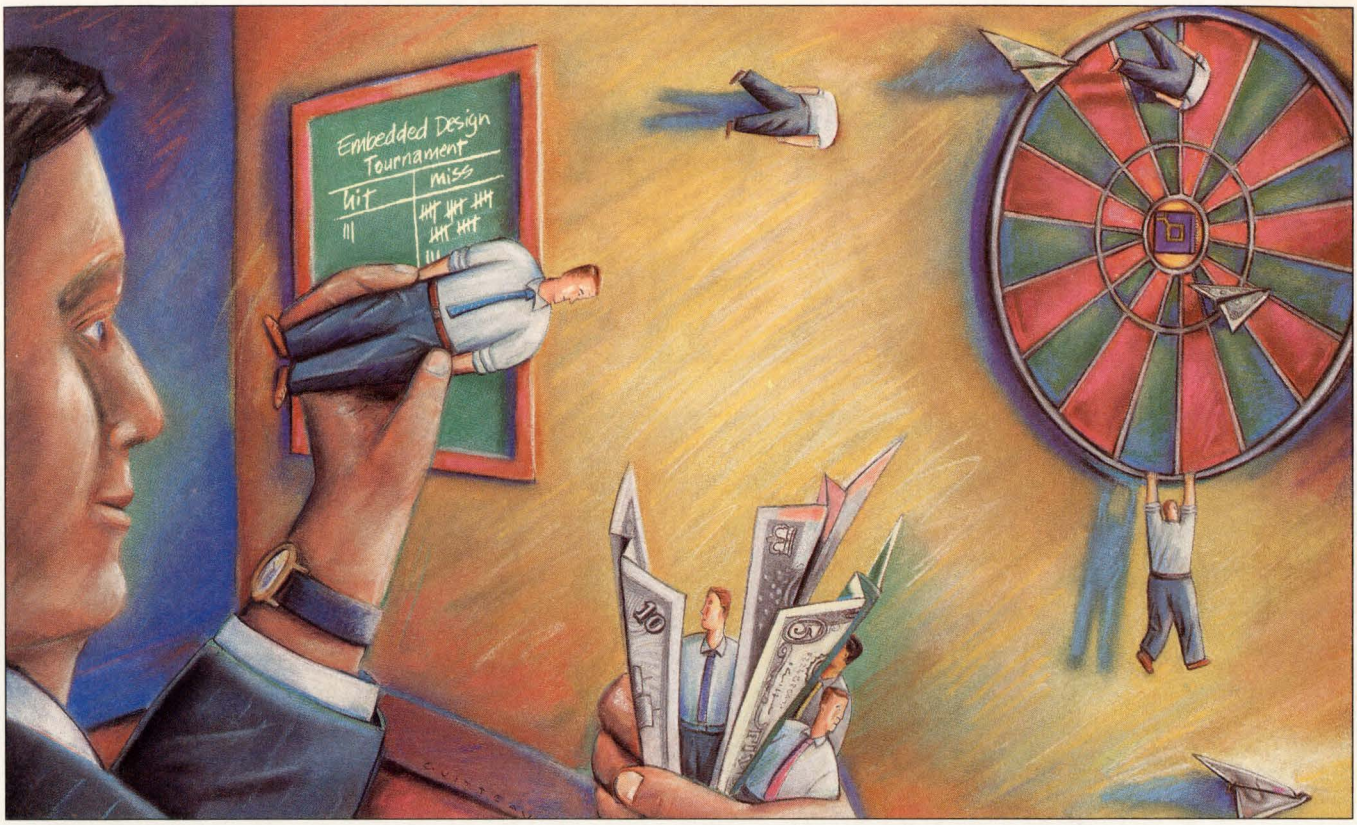

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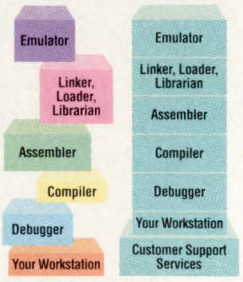

Mismatched, nonintegrated development tools can throw off a design team's efforts in no time.

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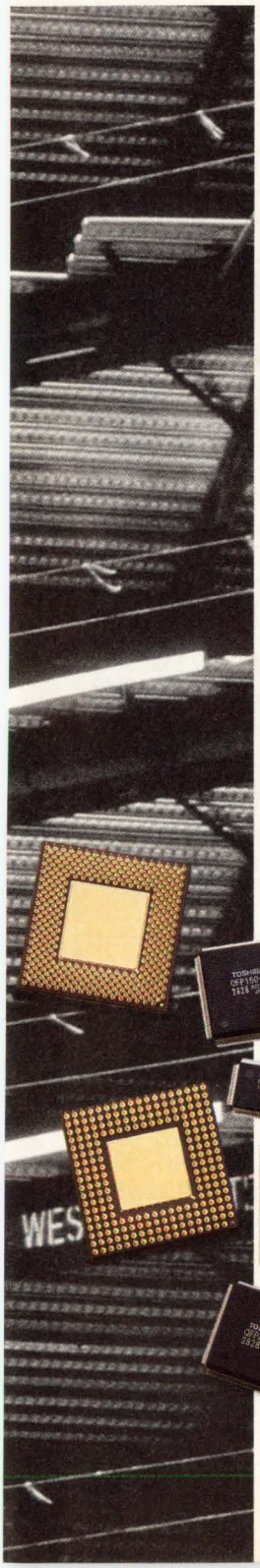

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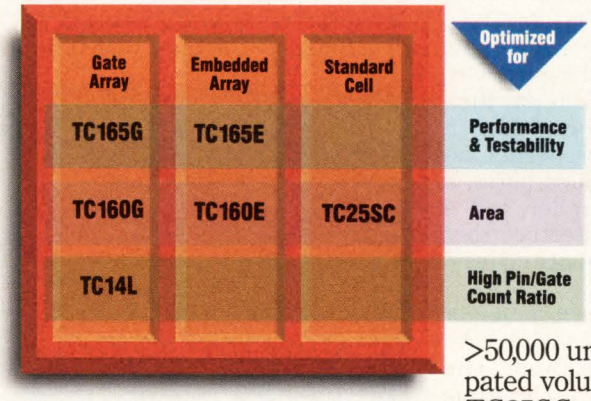

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CIRCLE NO. 32

INTEGRATED CIRCUITS

Third-party tools help DSP find a home in parallel processing

Dave Wilson, Senior Editor

As RISC processors challenge the hegemony of digital signal processors, where a general-purpose architecture may provide both time-to-market and programming advantages to the designer, it's in the area of high-end parallel processing where the benefits of DSP chips, such as the TMS320C40 from Texas Instruments (Dallas, TX), may maintain a unique advantage. Certainly, the part has the hardware hooks to make it useful in parallel-processing applications. And a wealth of on-chip peripherals includes six communications ports, a six-channel DMA controller and a dual external bus architecture that links the device with global and local memory.

Dr. Mark Smith, project manager at Hewlett-Packard (Palo Alto, CA), likes the part. "We chose the TMS320C40 because of its multiple message-passing links, dual memory buses and a high degree of internal concurrency that lets us exploit the parallelism intrinsic to our algorithms at different levels. The high link speed, large data transfer rates and fast floating-point performance fit well with our requirements," he says.

Defining hardware architecture

But before setting out to build a multiprocessor system, you must define the hardware architecture best suited to the application—and that's easier to do in some applications than others. One of the most useful features of the TMS320C40 is its flexibility; you can create many different hardware arrays, multidimensional as well as planar structures, using the six on-chip interconnects.

The easiest class of problems to solve, of course, is those where throughput is an issue but processing time is not. Pipelined processing systems, such as those used for speech recognition or graphics, where the application can be broken up into well-defined processing chores, is an example. Such problems are relatively easy to solve architecturally, in comparison to problems such as image extraction that may demand a planar lattice, hexagonal array or even a multidimensional structure of processors such as a cube.

As to how you can determine the best method of interconnecting the DSPs for any given application, David Wong, founder of Spectron Microsystems (Santa Barbara, CA), developers of the Spox real-time operating system for DSPs, has an answer. He says that this still has to be done mainly by analyzing the code and finding the bottlenecks. "You might do that by looking at which processes are using the most processor cycles or I/O cycles—or by using a profiling capability to determine where the cycles are going," he says.

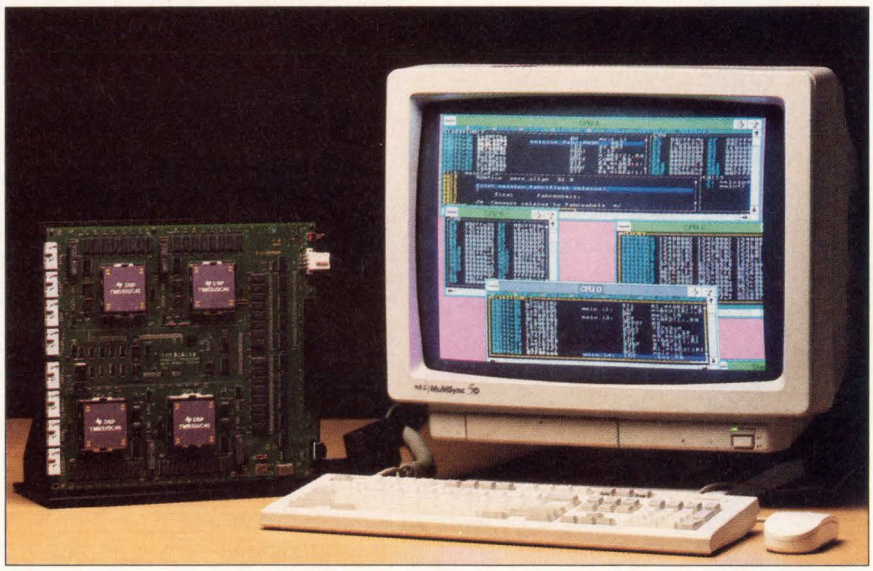
The other method is to experiment by just moving tasks around. But there's no easy answer. "We do require that the engineer have some idea what he's doing and where the bottlenecks are," Wong admits.

Brewster LaMacchia, the hardware and DSP marketing manager of Sonitech International (Wellesley, MA), a board and software development tool vendor, agrees with Wong. "Despite the fact that many tools are available for DSPs, I don't think that anyone has figured out how you make an algorithm aware of the [underlying] architecture it's operating on. You have to figure that out on your own," says LaMacchia. "Tools haven't been developed to do that for other parallel-processing machines and they don't exist for the TMS320C40 yet either."

Some tools available

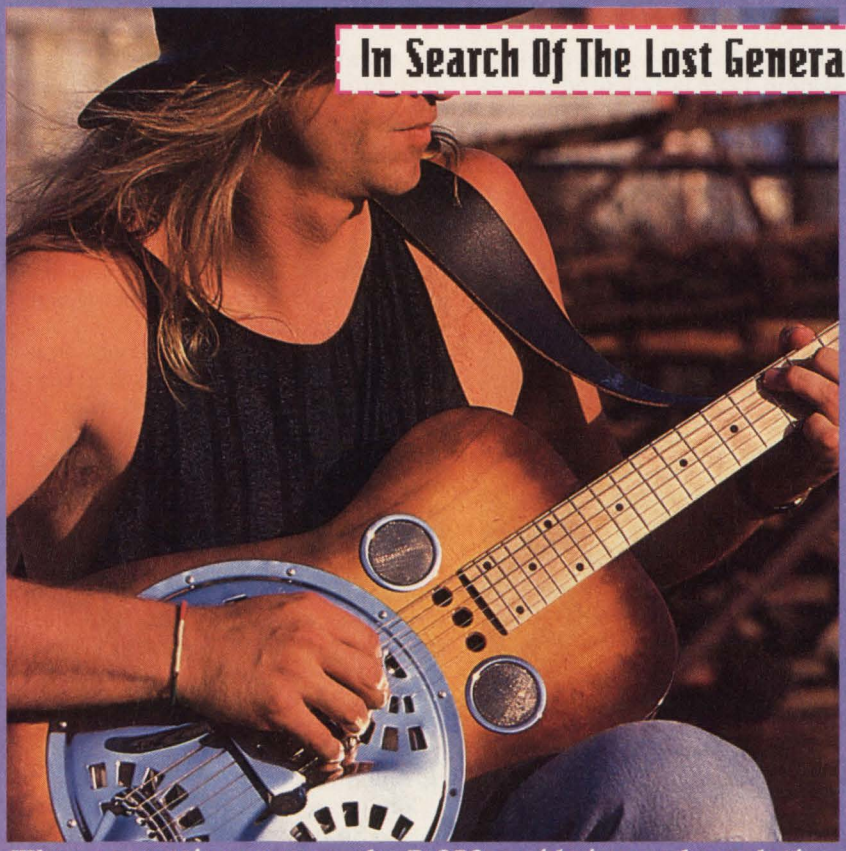
Even though existing tools might not help with determining what sort of multiprocessing array to build, TI does have tools to help with hardware development and verification. These include a scan-based parallel in-circuit emulator, the XDS510, as well as a parallel-processing development system (PPDS) that contains four TMS320C40s with 256 kbytes of local memory, 512 kbytes of global memory, communication port connectors, and an expansion connector. In addition, code-generation tools and C- and assembly-source debuggers are available.

The XDS510 emulator has a windowed C- and assembly-language source debugger interface that lets you monitor and debug several



The parallel-processing development system from Texas Instruments includes the XDS510 in-circuit emulator—claimed by TI to be the first to provide parallel debug capabilities for embedded applications—as well as parallel-processing development system hardware.

In Search Of The Lost Generation In Desktop Video



When outputting to tape, the Bt858 avoids image degradation and maintains the superior video quality as represented here.

When outputting video from desktop to tape, something gets lost in the translation. That something is **image quality** — which is why the resulting picture resembles a second generation copy of the original material.

Image degradation can be avoided, however, by outputting with an encoder at least one level higher than the tapedeck. Since most desktop video users rely on corporate-level video equipment with a 4 MHz bandwidth and a SNR of 43-50 dB — such as S-VHS — a studio grade encoder with a 5 MHz bandwidth and a SNR of 50-62 dB is necessary to maintain corporate-level quality.

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A videotape, **"The Ins and Outs of Video Out,"** discusses various aspects of the Bt858 in greater detail. Call Brooktree at 1-800-VIDEO IC for your free copy.

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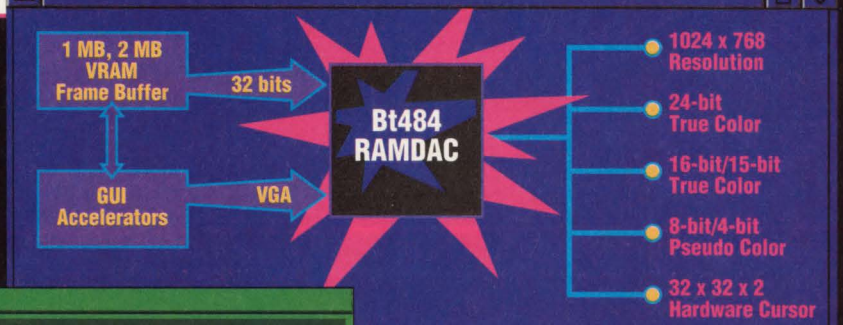

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TMS320C40s simultaneously. According to Texas Instruments, the XDS510 is the only emulator available that can perform the global start, stop and single-step commands so essential in a distributed processor system. A single XDS510 can debug all the parallel DSPs in a system and also determine whether the system load is balanced across the processors.

Third parties help

In addition to TI's software, third-party tools are available to support the chip. Comdisco (Foster City, CA), for example, has a graphical programming environment for developing systems that use multiple TMS320C40s. The MultiProx system lets you partition a signal-flow block diagram into regions for execution by separate DSPs. The system automatically generates separate C programs for each processor and analyzes the loading on each processor to minimize bottlenecks.

The Comdisco system lets you take a problem and allocate it across processors to find the best way to balance it. But despite its capabilities, the system can't take existing nonparallelized software and optimize it for a parallel implementation. But then TI's compiler can't take a generic C program and dynamically allocate tasks to different processors using hardware links either. Nevertheless, according to Bill Newman, vice-president of research and development at Comdisco, "Manual partitioning of the problem gets customers 99 percent of what they want."

For its part, Spectron is enhancing its Spox real-time operating system to support the chip. The enhanced version will include a high-level software interface, making it easy to utilize the chip's communication ports and DMA coprocessor. Spectron's Wong says the company will port Spox to TI's PPDS hardware and make the software available to TI's developers as a turnkey system. "As part of the feature set, we will provide the ability for each processor to pass data and messages to one another. We will also provide the ability for engineers to very easily move tasks from one processor to another without having to rewrite any code," he adds. The movement of tasks from one processor to the other will be specified by the designer using the system—the new operating system won't provide dynamic load balancing. ■

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INTEGRATED CIRCUITS

MCM DRAM accelerator boosts memory performance

Dave Wilson, Senior Editor

Building multiprocessing subsystems usually involves designing a complex custom memory controller to manage the data between multiple caches and DRAM arrays. To lift some of this burden from your shoulders, Cypress Semiconductor (San Jose, CA) recently debuted a three-chip multichip module (MCM) to help out. The device, the CYM7232 DRAM Accelerator, provides several high-level functions that maximize the system-to-DRAM interface and cache-line burst transfers and support cache-to-cache transactions. To broaden its appeal, Cypress has designed the module to work with a number of microprocessors, including the Intel 80486, Motorola RISC 88110 and Sparc.

First impressions

Early reviews from designers indicate that the new Cypress chip set looks like a winner. "In the past," says Thanos Mentzelopoulos, a project manager for engineering at Ironics (Ithaca, NY), a VME house, "I have had an inherent dislike of [off-the-shelf] DRAM controllers because they were always very slow. And they never were as good as the ones that I could design myself from discrete components. This time they've equalled me. In many ways, it's one of the few times when I've seen a chip manufacturer consider building a chip from a system perspective."

George Grey is the technical director of Tadpole Technology (Cambridge, England), a design firm that has built products around many high-performance RISC processors and peripherals. He also likes the chip set. "It's time that somebody paid a bit more attention to DRAM controllers, because although it's not difficult to design a simple DRAM controller, nobody has done a good job at designing a complex one. At first sight, it seems that Cypress has done a good job in terms of the architecture and the design of the 7232," he says.

The Cypress MCM design team—John Nemec, applications engineer (seated, left); Don Lieberman, project leader (center); and Suresh Bhaskaram, logic design engineer (seated, right). Says Lieberman, "We consulted with several key customers representing different processor and cache controller environments. They offered very specific suggestions that helped us optimize the 7232's bus interface. This helped guarantee a turnkey interface for all high-performance environments."

The DRAM accelerator module comprises three devices: an address/control chip complemented by two data path devices. The controller connects to the system bus with a 64-bit-wide data bus, a 36-bit-wide address bus and a set of bus transfer control signals. It interfaces to the DRAM array through a 16-byte-wide (128-bit) data bus plus check bits, a 12-bit row/column address bus, four row address strobe (RAS) outputs, four column address strobe (CAS) outputs, and four read control lines.

During write operations, the data is passed from the system bus through a FIFO array acting as an incoming queue. Writes can occur at the maximum FIFO transfer rate until the FIFO is full (16 64-bit words). The write FIFO supports cache line copyback and fill operations, reducing system bus traffic to a minimum. The write FIFO allows posted writes that permit cache line write-back at full FIFO speed, suspending the actual write to the DRAM until the cache line read is completed. This speeds cache line fill operations.

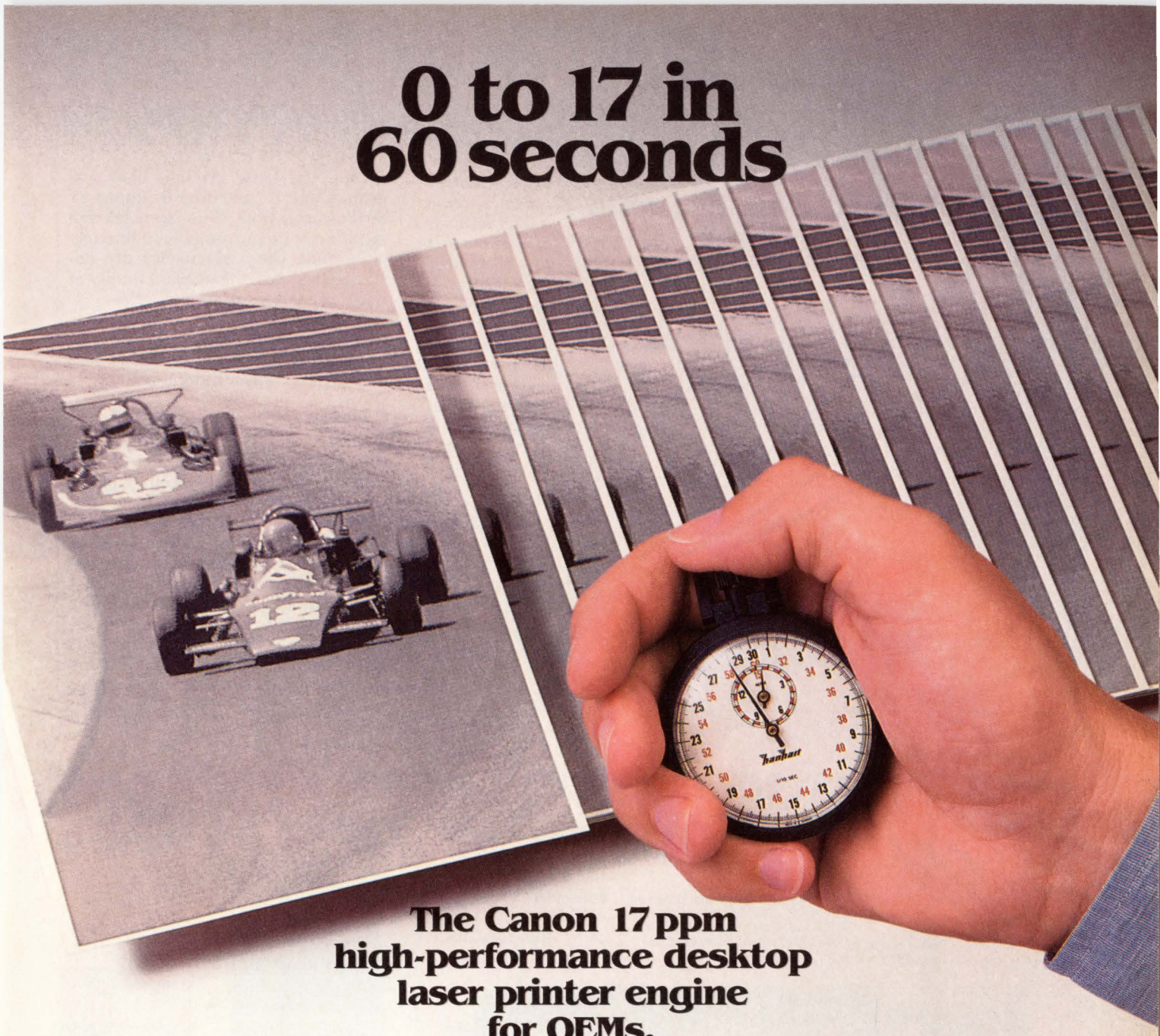
During read operations, the DRAM memory data is multiplexed from a 16-byte-wide DRAM access, pipelined to the error detection and correction circuitry and then supplied to the 64-bit system bus. This bus supports high-speed burst line fills with error-corrected data. Several features were added to make the device well suited to multiprocessor systems. These include the capability to inhibit reads and writes and to turn inhibited reads into reflective reads and inhibited writes into reads-for-ownership.

Full EDC possible

Since the module has a data path incorporated, it can perform full error detection and correction (EDC) on data as it's accessed. At present, the part has a 32-bit EDC, but for users preferring a 64-bit EDC version, Cypress will be building another data path chip that will be included on a next-generation module, the 7264. Because of the nature of the data paths, the 64-bit EDC version won't connect to 32-bit system buses.

The bus interface on the module is an extension of M bus, useful in a variety of applications. Four bus acknowledge/data strobe modes, for example, can support certain processor interfaces or can improve system performance. There are also selectable bus modes designed to support a variety of processors and cache controllers. Big endian/little endian convention is program-

0 to 17 in 60 seconds



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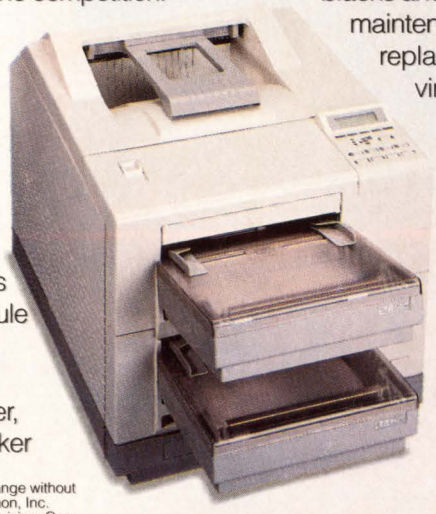

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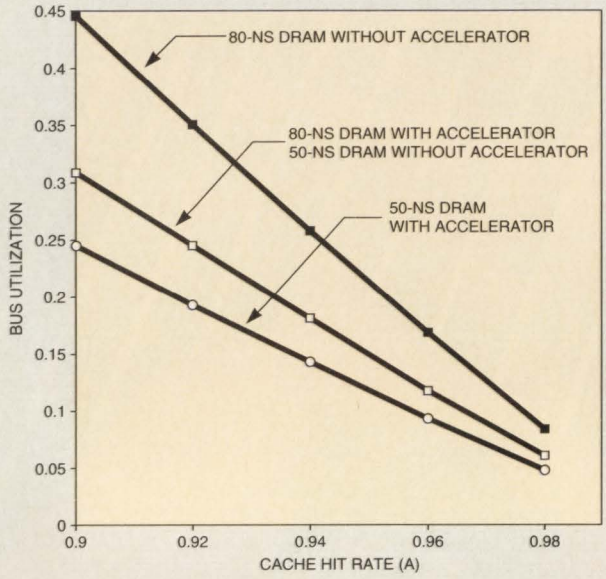
50-MHz RISC design example



By reducing the number of cycles it takes to access main memory after a cache miss, the DRAM accelerator enhances bus utilization, a key factor in determining the number of processors that can be used.

mable. The burst order is also programmable; it can either be linear- or 80486-compatible. Bus acknowledge signals are programmable to be early or normal; the early modes are designed to support the 88000 family of RISC processors from Motorola.

"Supporting 64 bits is a nice feature if you're designing systems around the 88110 and Sparc M bus or the i860," says Tadpole's Grey.

Memory coherency essential

Maintaining coherency between the cache and main memories is, of course, vital in any system. Coherency between data in the cache and the DRAM is left to the cache protocol to determine. The Cypress part, however, does maintain coherency in the device. If the processor needs to perform a read right after the FIFO has been written to, for example, the controller will write the contents of the FIFO out to system memory before letting

INTEGRATED CIRCUITS

the next read operation be performed, guaranteeing coherency in the part.

"One of the problems that most people struggle with when they design DRAM controllers is that they need to use a large number of pins. With a 64-bit part, especially, it starts to get very difficult in terms of the number of pins," says Tadpole's Grey. The Cypress module testifies to this fact—it will come packaged in a 400-pin PGA module at a cost of about $320. Cypress says that the high pinout of the device was one of the reasons the company used a multichip module rather than a single-chip device for the design.

Further, Cypress claims that building the part from three higher-yielding dies, rather than from one monolithic IC, makes the accelerator more economical.

"Supporting 64 bits is a nice feature if you're designing systems around the 88110 and Sparc M bus or the i860."

George Grey, Tadpole Technology

■ ■ ■

What kind of performance increase is attainable? To demonstrate its power, Cypress has tested the device in a 50-MHz RISC design. The accompanying chart illustrates the effect on cache hit rate and bus utilization in systems built with the Cypress part versus those built with a standard controller, defined by Cypress as one that has no FIFOs and doesn't support a difference between the width of the CPU bus and the DRAM bus.

The top line on the chart graphs a 50-MHz system with a standard DRAM controller and 80-ns DRAM memory. The middle line illustrates the performance advantage that the designer would gain by investing in 80-ns DRAM using the controller. As it turns out, it's the same as building a system around 50-ns DRAM without the accelerator. The bottom line shows the performance of a design with a controller and 50-ns DRAM. The reduction in bus utilization with systems that use the device is particularly important in multiprocessor systems, where bus utilization is a key factor in determining the number of processors that can be supported. ■

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SOFTWARE & DEVELOPMENT TOOLS

Windows on the world

Dave Wilson, Senior Editor

Microsoft's Windows NT (New Technology) is a new high-end version of the company's Windows operating system. It's an implementation for high-end machines such as 386, 486 and higher Intel platforms, as well as MIPS RISC computers and servers.

A self-contained operating system with full DOS emulation and all the features of the current Windows implementations, it also offers support for symmetric multiprocessing, integrated networking and both 16- and 32-bit Windows applications. In its first release, Windows NT will support Posix-compliant and leading OS/2 server applications, in addition to DOS and Windows applications.

The Windows NT operating system includes four classes of components. One set runs in the "privileged" mode and has direct access to hardware resources and protected operating system functions. Included are the Executive, providing the basic operating system services required by the other components, and the Privileged Mode Extensions, including device drivers, file systems and processes such as LAN file servers that require close interaction with device drivers and file systems.

A second set of components runs in the user system mode as separate processes, requesting services from the privileged components of the system; these are the protected subsystems and the application programs.

The heartbeat of Windows NT

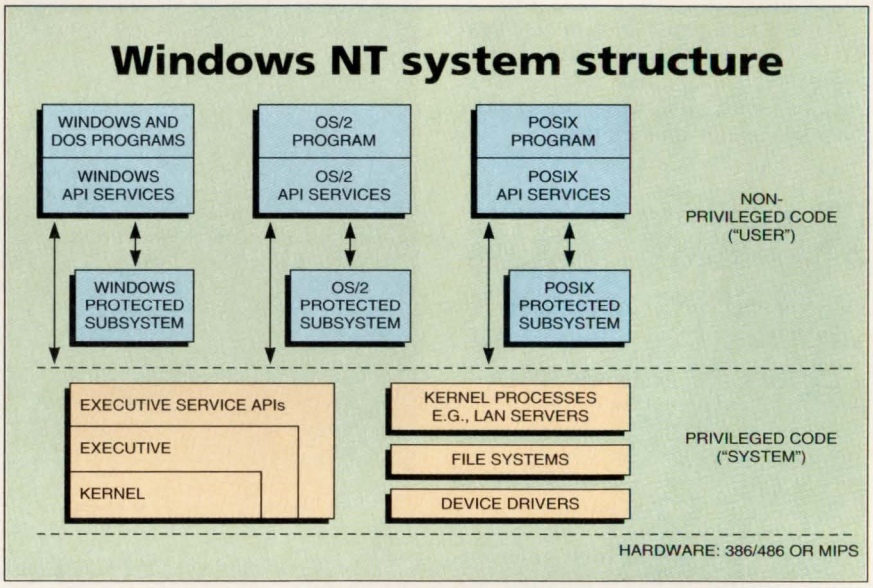
The Executive is at the heart of the system. It performs housekeeping tasks such as process and thread management, memory management and interrupt servicing so that protected subsystems can provide the services expected by their application programs. A microkernel (approximately 50 kbytes of compiled code embedded within the Executive) implements low-level, machine-dependent functions, multiprocessor synchronization, thread dispatching, and kernel objects. The remainder of the Executive utilizes kernel services and provides higher-level services to the rest of the system in turn. This code is fully preemptible, multithreaded and re-entrant.

System extensions can be made for code that must directly access hardware or that must be run in the privileged state of the machine. Privileged extensions comprise device drivers, file systems and privileged processes. In general, Windows NT device drivers are layered—for example, there will be one generic SCSI driver that will be layered on top of smaller, specific drivers for the various SCSI adapters, simplifying the job of writing a device driver. In addition, Windows NT will be able to support "streams"-based drivers, simplifying the tasks of porting a TCP/IP (Transmission Control Protocol/Internet Protocol) driver from Unix to Windows NT.

File systems

As to file systems, Microsoft will support the DOS-compatible File Allocation Table (FAT), the OS/2-compatible High-Performance File System (HPFS) and a CD-ROM file system.

Microsoft intends to develop three protected subsystems to support three classes of programs. The first is a Windows subsystem that will provide the system services—window management and graphics—needed by both 16-bit and 32-bit Windows programs, as well as by DOS programs. Microsoft has defined a new 32-bit Application Programming Interface (API) for software developers that want to retain the familiar Windows environment yet benefit from a flat 32-bit memory model. The Windows 32-bit API will be supported in Windows NT first, then in a future release of Windows on DOS. The second subsystem will be Posix, and will support programs written to the IEEE-1003.1 interface. Finally, the OS/2 subsystem will support programs written to the programming interfaces of OS/2 Versions 1.3 and 2.0. The initial release of Windows NT will support popular 16-bit server applications, such as SQL Server. ■



The initial release of the Microsoft Windows NT operating system will run on both 386/486 and MIPS hardware platforms. Not only will the new operating system run Windows and DOS programs, but OS/2 and Posix programs as well.

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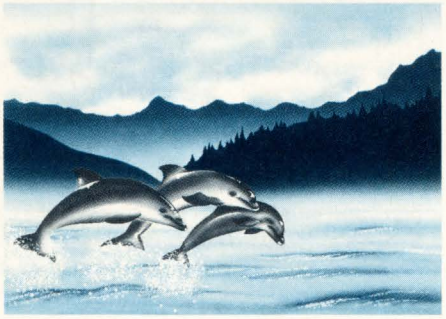

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Distributed real-time Unix builds on microkernel technology

Tom Williams, Senior Editor

An alliance between French Unix vendor Chorus Systemes (Paris) and the U.S. real-time control company Integrated Systems (Santa Clara, CA) has resulted in a real-time version of Unix specifically designed for use in distributed systems. According to Paul Wells, marketing manager for ISI, the need being met by the new product is "to bring flexibility and scalability through microkernel technology to customers who are also looking for a standard application programming interface (API)."

Aria, the new product, is based on Chorus Systemes' microkernel architecture and is the result of an agreement between Chorus and Software Components Group (SCG) which was concluded shortly before SCG was acquired by ISI. Wells says that Aria can accommodate the user who needs very fast, deterministic performance for certain tasks at a dedicated board level, but who also requires Unix services for distributed processing nodes.

A two-part approach

The basic implementation of Aria consists of a nucleus and a process manager. The nucleus, in turn, includes a version of the Chorus microkernel, a timer and a driver. There's also an interface to SCG's real-time kernel, pSOS+, if the user feels that pSOS+ is needed on any given board. The microkernel is largely machine-independent and includes a memory manager to control virtual memory and local memory resources. It also has its own preemptable real-time executive. The microkernel interfaces to the underlying hardware via a supervisor and a small amount of machine-dependent code.

Both the memory manager and the real-time kernel communicate with the process manager by way of the microkernel's interprocess communications manager. The process manager provides the Unix interface. Unix system calls sent to the process manager are interpreted and issued as calls to the microkernel. Conversely, requests for services from the microkernel are passed by the process manager to the Unix system. The process manager also passes data to the Unix system. Interprocess communication takes place via standard Unix sockets or the network file system (NFS), where the nucleus uses an NFS/sockets manager module.

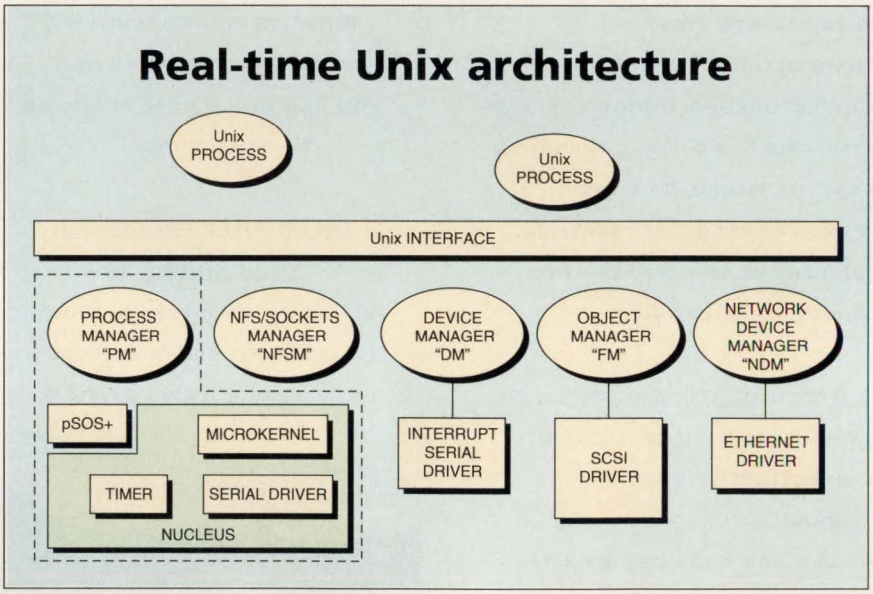
Threading through ports

Aria organizes its processing into execution units called "threads." The general mechanism for communicating between these threads, or tasks, which may be on the same site or at separate sites, is by exchanging messages via message queues called "ports." Ports enforce decoupling between tasks and messages, but also make dynamic system reconfiguration easier. Since ports are known to all sites in the system, they can be combined into port groups that send messages to multiple ports simultaneously. Tasks and services residing anywhere on a system can direct themselves to other tasks merely by addressing the proper port. On the same site, threads can communicate using shared memory primitives or "minimessages" that entail less overhead.

Although the microkernel's real-time executive features fast context switching and interrupt response, Aria addresses what Wells calls "moderately coupled" real-time, where certain things have to be scheduled before and after certain other things and meet certain time constraints. For the "hard" real-time requirements, which must meet absolute deterministic timing specifications, pSOS+ can be included. Aria doesn't dispatch pSOS+, but can supply its services when requested and can accept data from it. The role of pSOS+ in an Aria environment is to independently run hard real-time processes on a local node where it can guarantee determinism and initiate communications with the larger system.

Unix resources can reside either on a local board, where they can immediately be available to that board's microkernel, or they can reside elsewhere on the network and be requested by any local microkernel.

In addition to the nucleus, pro-



A distributed real-time Unix architecture supported by Aria is shown here. The minimal implementation of Aria—within the dashed lines—can be replicated on any number of single-board computers in the system. Other Unix services can reside on designated boards, and still be available to all Aria microkernels on the system. For dedicated hard real-time tasks, Aria provides an interface to the pSOS+ real-time kernel.

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gram manager and NFS/sockets manager, ISI provides about 40 Unix utilities in binary code so that you can add functionality such as an SCSI driver or an Ethernet interface at any given site. The initial offering will be for the Motorola 68030-based MVE147S single-board computer. Other binaries, such as for the 68040 and the Sparc architecture, are coming.

System not complete

ISI admits that Aria as presented—with only 40 utilities—doesn't represent a complete Unix system. But Alfred Chao, vice-president of ISI and SCG division president, points out that "since the system is binary-compatible with Motorola, a customer could take Motorola binary Unix utilities and run them on top of Aria and could actually build up a complete, full Unix that's compatible with System V/68." System V/68 is Motorola's implementation of Unix System V Release 3.2.

Currently, Aria supports the Sun Sparcstation as a host cross-development system, acting as an NFS server for editing and compiling real-time Unix applications. The host is also the site where code is linked and configured with the Aria kernel prior to being downloaded to the target system via an Ethernet link. It maintains a directory in its root directory telling which compiled and linked target applications get downloaded to which target nodes by copying the executables to the target file system.

According to Chao, whose division has implemented multiprocessor configurations of pSOS+, "Microkernel technology is really the proper architecture for doing distributed real-time; it's better than pSOS+ with its monolithic kernel. The strongly partitioned nature of Aria ensures that all the services get distributed to where the resources are, as opposed to where the user is." ■

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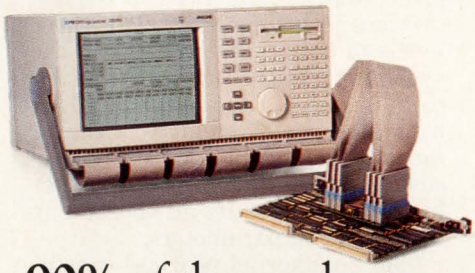

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Scalable real-time OS adapts to range of applications

Tom Williams, Senior Editor

A single, seamless real-time operating system with Unix/Posix interfaces is the goal of a new architectural technology from Ready Systems (Sunnyvale, CA). Useful for a wide range of applications—from small motor controls to large multiprocessor-based telecommunications systems—the scalable OS architecture, which Ready has begun building into the core of its product line, lets you select tradeoffs in size, performance and functionality so you can cover the domain of present real-time executives such as Ready's VRTX, the high end of real-time Unix systems and much smaller embedded controllers down to, but not including, custom state machines.

The planned operating system, according to Ready Systems executive vice-president James F. Ready, is "an overall architectural approach to have a family of interfaces that span a wide range of real-time applications." At the base of the architecture is what Ready has dubbed the "nanokernel," a compact, processor-dependent layer of code of typically less than five kbytes that provides basic real-time services to deeply embedded applications as well as supplying the building blocks from which higher-level communication and synchronization services can be built.

Small and versatile

The nanokernel interfaces smoothly with Ready's mainline real-time executive, VRTX, and can easily interface with other proprietary kernels—and even with emulations of real-time kernels, such as Wind by Wind River Systems (Alameda, CA) or pSOS+ by Silicon Components Group/ISI (Santa Clara, CA).

Another major layer of the system is a full Posix shell with real-time extensions which let you incorporate features of real-time Unix or lower-level kernel services, according to the needs of your application.

Each level of the real-time OS architecture is capable of passing data to levels above and below. Applications written to use the services of a given level, such as the nanokernel, can run independent of any higher level. Applications also can request services from higher levels if those levels of service are present in the system. A motor control program, for example, could run independently in a small area of memory within a much larger automation system, occasionally passing data to higher levels to be used by an operator to log operating parameters.

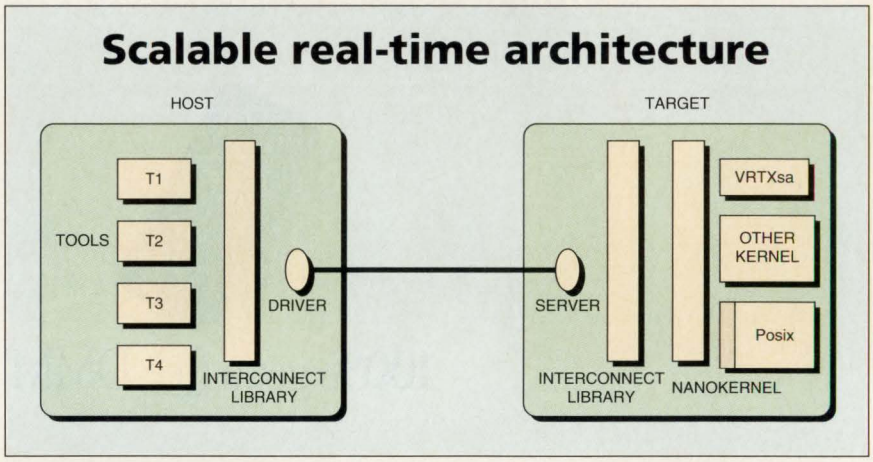
The nanokernel provides concurrency via lightweight shared-memory tasks called "threads," which pass messages by way of common addresses. The nanokernel provides basic facilities for creating and deleting threads at a more primitive level than does VRTX. These primitives support the creation of synchronization and communication services that can be used by applications that interface to the OS at higher levels of abstraction, such as the VRTX or the Posix call level. Applications can also call nanokernel services directly.

Ready emphasizes that this is not the same concept as "modularity, where you can add, say, a file management system or something." A file system, for example, would interface at the Posix level. But the same application that uses a file system could make a critical call to the nanokernel level if needed. More commonly, the nanokernel services deeply embedded applications where efficient use of resources is essential and that are constrained by limited memory, processor power or I/O. "It is a myth," says Ready, "that once you have real-time Unix all known real-time problems are solved. That's like saying, 'Now that we have 68040s, nobody uses 8051s anymore.' "

Flexibility without switching

The goal is to include the small, resource-constrained applications in the same Application Programming Interface (API) and design environment you use with much larger applications, so you're provided with the flexibility to allocate functionality, performance and cost considerations without having to switch programming environments.

The reality in the industry is that about half the existing real-time designs use customer-designed proprietary run-times. Users are looking for a way to get into standard environments without sacrificing their existing investment in



Ready Systems' new scalable real-time architecture lets you incorporate the basic nanokernel, which provides services and primitives for higher operating system layers. These can include Ready's own VRTX real-time kernel or other proprietary kernels, as well as a full Posix system interface. Host/target communications aim to minimize use of target resources and promote the ability to accommodate multiple tools on the host side.

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code. The ability to support kernel-level run-times, in addition to its own VRTX, gives the scalable architecture the ability to incorporate proprietary run-time systems by interfacing them to the nanokernel level—which is significantly easier than rewriting at the real-time executive interface level. "We can capture a customer's existing application code by an emulation of their existing kernel to the nanokernel level," says Ready.

The needs of small, resource-constrained target systems have been recognized in the way the Ready architecture addresses host/target communication. Today, when a host communicates via Ethernet with a target system under development, it requires a target-resident run-time of about half a megabyte, because most Ethernet communications rely on TCP/IP (Transmission Control Protocol/Internet Protocol), which uses Unix-style sockets for communication. The target has to support all the complementary protocols for handling such communications, which gets to be an enormous overhead when the target under development is a small navigation controller or an engine control.

No more target overloading

Under Ready's scheme, if the communication technology is Ethernet or some proprietary communication hardware, you need only supply a host driver and a relatively small (8- to 10-kbyte) target server to handle the network packets or other protocols. The communications is just low-level packet handling, not full TCP/IP. Ready points out that without TCP/IP, all you need is a driver and a small—under 10-kbyte—protocol handler to deal with debugging packets. "All of us are guilty of overloading the target in terms of symbol table management, daemons and the like," says Ready, and emphasizes that his company has made a philosophical commitment to unburden the target from communication overhead.

The new architecture will gradually be incorporated in Ready products, with a new VRTXsa (for scalable architecture) to be based on the nanokernel technology. In addition, a new version of the development environment, VRTX Velocity, is under development which will also incorporate the scalable nanokernel technology. Initial targets for VRTXsa are the Motorola 68000 family and MIPS processors. ■

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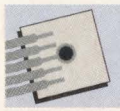

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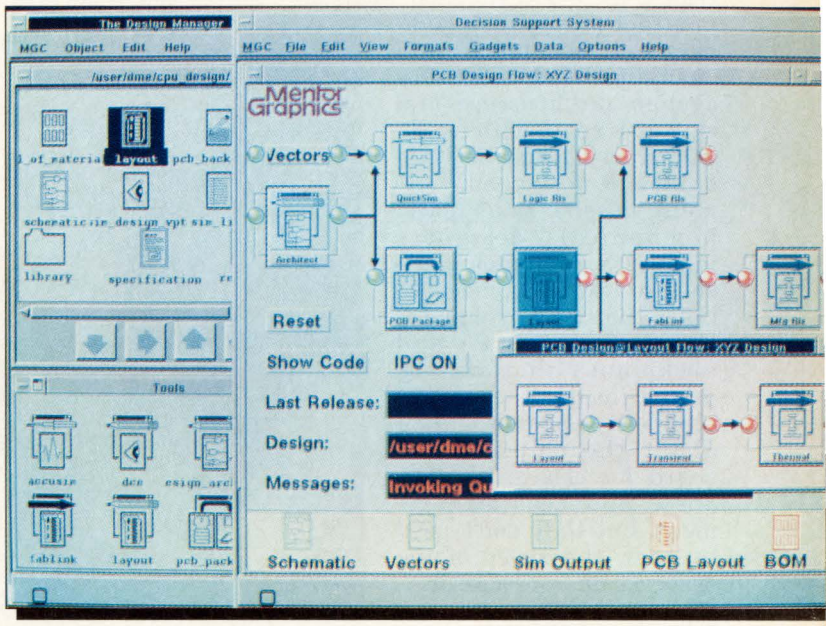
Lack of standards impedes database management

Trying to get everyone to agree on how and when to communicate design, test and manufacturing data is a battle that's likely to rage for some time.

Mike Donlin
Senior Editor



Tools such as Mentor Graphics' Decision Support System can manage portions of a design by linking multiple design tasks through a spreadsheet environment. In this example, the layout task (highlighted in blue) consists of a subset of tasks such as physical layout, transient and thermal analysis (window in foreground).

Managing design databases is a lot like wrestling an octopus—even if you get four arms under control, there are four left to contend with. Design tool vendors claim the way to manage today's complex development cycles is concurrent engineering, a strategy that considers everything from concept to final implementation early in the design phase. But if concurrent engineering is to be more than a buzzword, the many databases used in each phase of a design must communicate on some level or managing them is impossible. This means integrating the concerns of design, test and manufacturing under one large umbrella that will keep managers in each discipline aware of the needs of the others. Though the problem is easily stated, the solution is complex and cuts across many lines, both technically and politically.

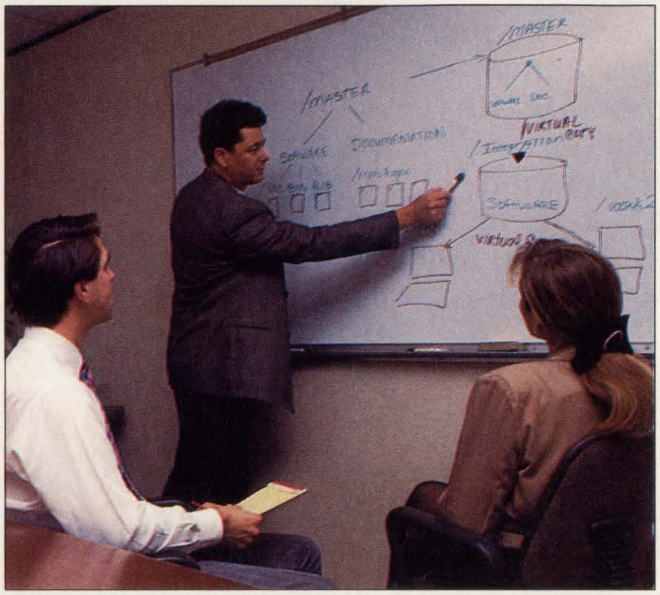
From a technical standpoint, interdisciplinary communication is complicated by the fact that the many databases and related tools usually grow up over time. Just as a library houses a number of volumes acquired over the years, a company may own a network of hardware platforms, operating systems, parts libraries, and databases that have been pieced together as needs dictated and technology became available. Just keeping track of who's using what software on which platform is a formidable challenge, and time-to-market pressures complicate the process because a company must remain productive while trying to get a handle on evolving technology.

Balancing everyone's needs

"Trying to get software to operate on all our systems is hard enough without trying to manage the whole thing," says Lester Schueler, system programmer at Ford Motor Company (Dearborn, MI). "And though we have 200 programmers working across the company, we still can't lose sight of the fact that we're a car company, not a software-development house. Right now we just put different tasks and their current revision levels on a large system to keep track of everything, but that means having to go through a long list to find out who's doing what. We can't just make everyone change their ways and adopt radical new procedures all at once. With all the tools

and computers showing up every day, people are getting interface shock as it is. Any changes will have to be done gradually."

One problem in managing design databases is that each design discipline has its own set of needs, priorities and data representation methods. To communicate needs between disciplines, tool vendors must decide on how much data to transport between each environment for proper task management. Too much data changing hands will slow system performance and clog disk space with irrelevant information. Too little data and design management doesn't take place. Mechanical designers making a computer chassis, for example, need to know the size and shape of the circuit boards and backplanes that will be placed inside. They might also need some information about the chips on the board for clearance tolerances and heat management, but they don't need to know the speed of the system's microprocessor.



TeamOne uses a baseline hierarchy approach to control versions of database files. "The master baseline contains all product components that have been tested and verified at some level," explains Patrick McGill (shown at blackboard), vice-president of marketing at TeamOne. "By creating virtual copies of this master baseline, a project leader can let team members make changes to a design without affecting users outside the group. "

Infrastructure key

Deciding what to include in a design management infrastructure is a key part of the solution. "No one product is comprehensive enough to manage all of the different types of information in today's design environments," says Jayaram Bhat, director of frameworks at Cadence Design Systems (San Jose, CA). "So if you're going to succeed in managing design databases, you have to take a multilevel approach. That means all of the tools and databases must be open—that is, accessible to any management software. Then you have to add information to your component database that other members of a design team might need, such as cost and reliability information. Once you have that, you have to think about how you're going to store that data, where you're going to archive it and how you'll manage all of this library information."

The requirements of each data storage level are different. Archived data, for example, must have current revision levels, availability, cost, and reliability information included so pieces of a design can be tracked. Archived data can reside in a commercial relational database and used to generate reports and spreadsheets for management. While this information must be updated regularly, it's not used interactively, as is the component data a layout engineer needs to place a device on a board.

In a perfect world, the layout engineer could retrieve data from an archived database, but to incorporate everything known about a component inside of each library would create an unwieldy database which would impair a tool's performance. Trying to get the two databases to communicate is high on the wish list of many designers, managers and accounting personnel. "The EDA vendors' databases are usually proprietary structures which won't work with a commercial database such as Oracle," says Harold Baker, systems analyst for Caterpillar (Peoria, IL). "Our EDA database is really an ASCII file generator which contains information that its related tools need, but which can't provide design management information. We're constantly having to convert from one type of database to another. That means having to write our own maintenance programs to extract data from multiple sources so we can manage it."

Who's responsible?

Because managing disparate data is such a thorny problem, many companies are reluctant to hand it over to any one vendor. Any solution must take existing data and manipulate it into a format manageable by the vendor's tool. This prospect is frightening to a company with enormous amounts of time and money invested in its component libraries. For their part, many EDA vendors are reluctant to get dragged into the fray and become saddled with the unprofitable task of becoming data managers instead of point tool vendors.

"We don't believe that an EDA company should be in the business of creating a design data management system at the enterprise or global level," says Lee Daniels, director of design software at Racal-Redac (Mahwah, NJ). "If an EDA company tries to manage all the various disciplines involved in producing a product, the management software is going to be biased to the EDA's needs. Our philosophy is to look to those whose business it is to write enterprise-level software. We'll provide an interface, but it won't be specific to any particular data management system."

For the present, some EDA companies provide design management software that will tie together tools related to a single part of the design. These products let you select tools and combine them with associated data to form a continuous flexible design process. The Design Data Management System from Mentor Graphics (Wilsonville, OR), for example, uses object-oriented database technology to support all design data with a series of related design data models. These models stem from a single "parent" design model, so they respond identically to tool requests, design management and user commands. In ef-

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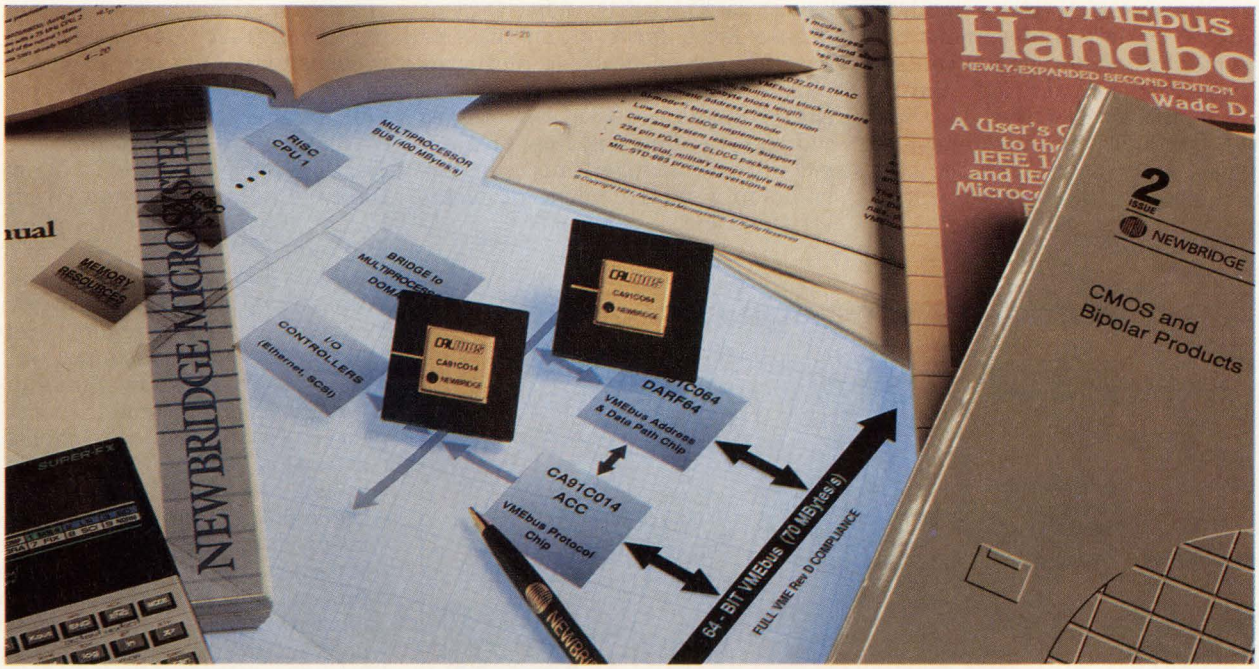

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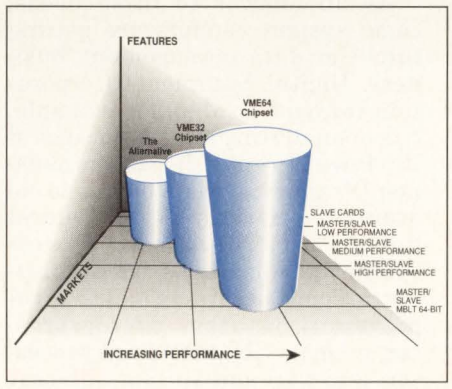

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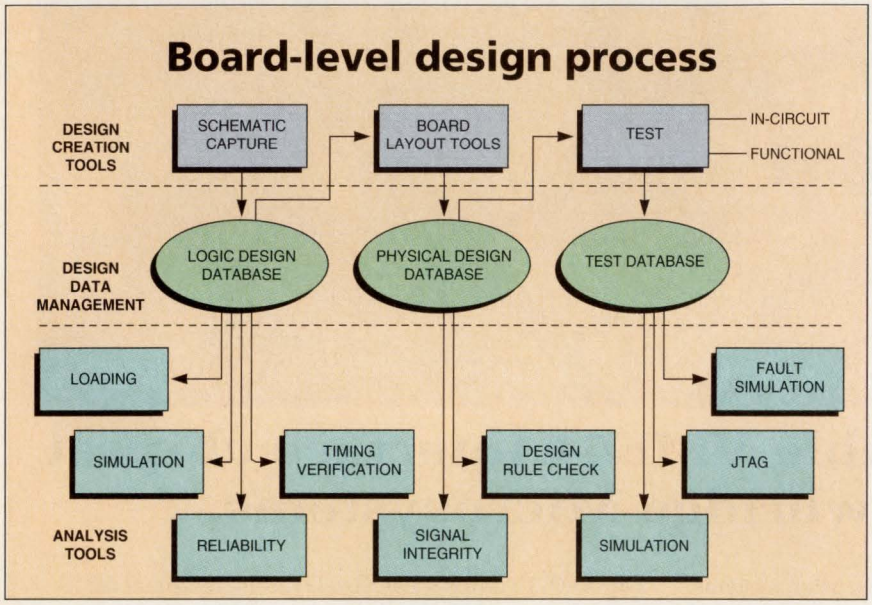
CIRCLE NO. 48

fect, the design models appear to the user as a unified database across all disciplines. Using these models, Mentor's Design Management Environment supplies version control, configuration management and release facilities. The Decision Support System provides a spreadsheet interface to string together the associated tools and data for the concurrent engineering paradigm.

across multiple domains without forcing customers to learn a lot of new tools. The software has to be at a base level, however, so that it's portable across multiple platforms and a number of environments. After all, the needs of a computer company are different from an automobile manufacturer, but the underlying data management problems are the same."



This PCB design paradigm is representative of the dilemma facing other disciplines in a product's development from mechanical engineering to manufacturing. Over time, suites of tools have been vertically integrated to solve the problems associated with a particular phase of a PCB's development. Real data management can only occur when a method of communicating between the isolated databases is established. Currently, little communication takes place at this level, mainly because of a lack of standards and designers' reluctance to change.

While management software such as Mentor's ties together tools associated with any one design task, data management at the company-wide, or global, level is a far more elusive goal. One suggested solution for the global data management problem is to treat the task as an extension of the operating system and provide hooks to existing databases via a software subsystem. This solution is appealing because it would let companies tie existing databases together at a primitive level without having to commit to any one vendor's proprietary solution. "I envision point tools which will manage data across a number of environments or frameworks through operating system extensions," says Bill Holbrook, manager of the data management group at Viewlogic Systems (Marlborough, MA). "This scenario would provide the appropriate views

As an answer to these needs, some system vendors are getting into the data-management business. Digital Equipment Corporation (Maynard, MA), for example, has been touting the advantages of its PowerFrame design-management framework as a means to coordinate electrical and mechanical design environments. PowerFrame includes tools for organizing a project according to its logical hierarchy (system microprocessor, memory, floating-point processor, and I/O) and storing different views of the data (schematics, netlists and test vectors) within that hierarchy. Specific CAE, CAD or CAT tools are joined to PowerFrame by aligning the model of how the files are used with PowerFrame's data model. This is done through a text file or, for more complex tools, through a C program.

Although PowerFrame lets you assemble a toolbox for any portion of a design, designers who are looking to integrate their relational databases to tool databases will have to wait a while. "Although we provide services to link tools together in their own environments, we can't yet encapsulate existing relational databases," says Michael Laine, PowerFrame marketing manager. "We are aware of the market's demands for such a capability, though, and we're working on a solution. The problem is interfacing the various formats at the byte level. Right now that's done through a cumbersome translation process with an error-checking routine. That means overhead which slows everything down."

Though the technical barriers preventing data management in large heterogeneous environments are daunting, they also present a unique opportunity to smaller companies who want to take advantage of the EDA community's reluctance to develop such global software. While it may be difficult for a start-up to compete with established simulator and schematic tool vendors, the data management market is open to anyone who accepts the challenge.

Independents go for it

Companies such as TeamOne Systems (Sunnyvale, CA) are developing file management products that aren't tied to any one EDA vendor or hardware platform. TeamOne's management product, TeamNet, works in design environments where tool encapsulation isn't necessary. According to TeamOne, encapsulating tools for tight integration to a framework is a time-consuming and often unnecessary task which requires extensive copying of data to and from areas on the network. TeamNet interacts with the Unix operating system on platforms from the leading workstation vendors to track shared data concurrently and manage any versions of design data that are changed during a task.

The design change control process takes place in two phases. First, you make changes in your local work area and then update the development baseline, which is a logical group of files that comprise the components of a given product. These baselines may represent components from one or many engineering domains—CASE, CAD, CAE, or

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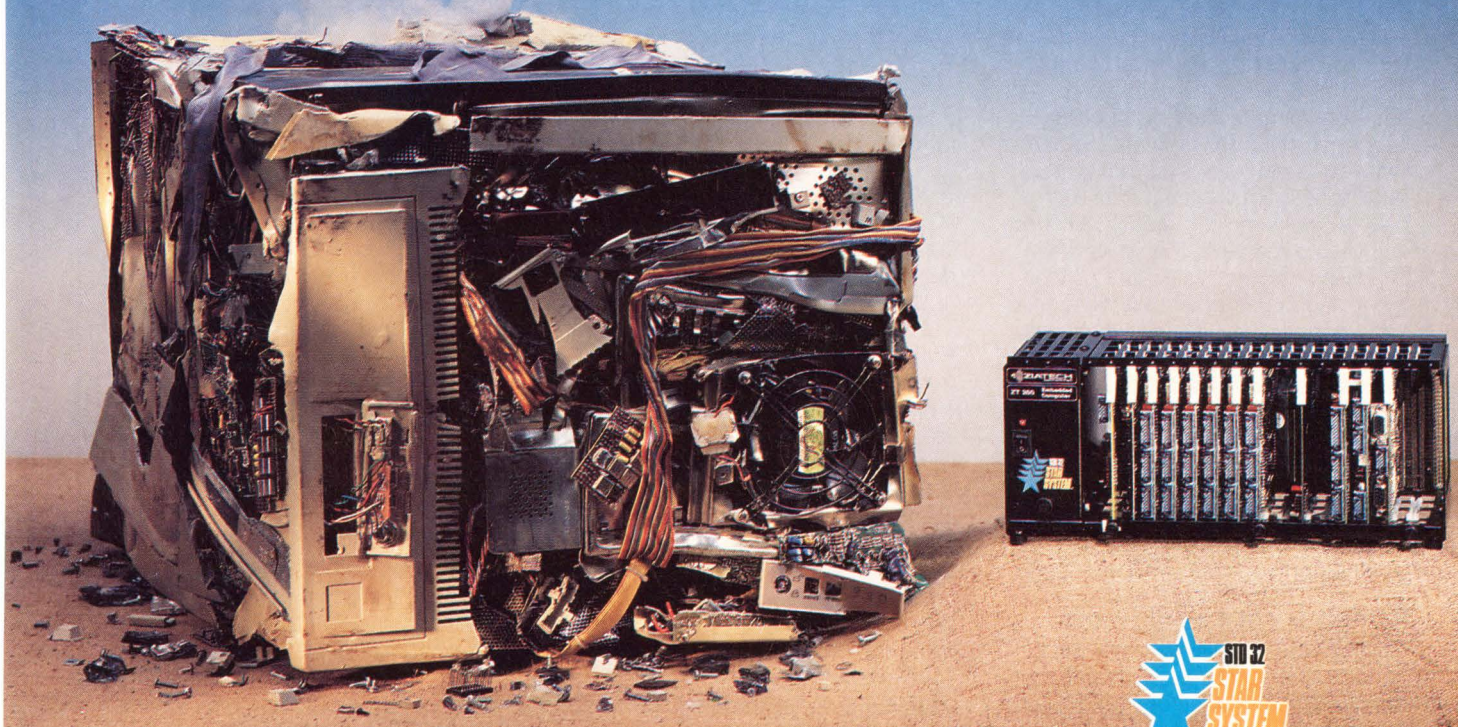

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DBMS: A key enabling technology

How can you get your product to market faster? The key today is concurrent engineering: the ability for multiple users and tools to cooperate simultaneously on the same design. This approach requires that you overcome the communication bottleneck and move data among tools and users. (A schematic editor may be easy to use, and a simulator may be fast and effective, but getting the data from one to the other and back again is slow and error-prone.) For multiple users and tools to cooperate they must share data. This is the key contribution of a database management system (DBMS). As long as data is kept in proprietary file formats, as most tools do today, users can't concurrently share it. The best they can do is move it sequentially from one tool to the next. This slows down the design process, eliminates concurrency, and becomes difficult when feedback loops occur in the design process. In addition, serial translation is imperfect. Information is often lost or distorted, or the user must go to great lengths to preserve the correct semantics. Finally, such translations are slow and can easily become the bottleneck in the entire process. Imagine how frustrating it is to have your file translation time take longer than your simulation time!

DBMS is not a magic wand

A DBMS doesn't magically solve all these problems, but it's the key enabling step. Sharing data requires that applications have a common data-access mechanism (the DBMS) and agree on data format (common data models or schema). Once DBMS technology is available, it's possible to begin the effort toward common data models, because you now have a facility that lets you actually define and use those data models. With object DBMSs that support encapsulation for active data, you can encode your own methodology. You tell the DBMS what you'd like to do automatically—for instance, spawn a simulation whenever a new design page is checked in, send E-mail to the test manager or schedule a nightly archive. The DBMS ensures these actions occur. The ultimate goal is to have one DBMS controlling access to multiple databases—for design, documentation, manufacturing, packaging, software, and test—as well as related tools for design and configuration management. The challenge is to reach this goal without completely disrupting current operations and without changing the current mode of usage or the design process.

Migration by layering

If your current environment includes a set of applications sharing a common data interface, you can replace that interface, or layer it over the new DBMS. The applications won't change, although relinking may be required if dynamic linking is unavailable. With this method, the applications can immediately use the new DBMS and enjoy at least some of its benefits.

For example, in one case where a site used Objectivity's product, the applications had previously been limited to databases that fitted within virtual memory, and they were facing limitations in swap space size. After the change they could immediately expand to virtually unlimited size; they also received the benefit of full distribution, heterogeneity and recovery.

Some of the capabilities of the DBMS, such as versioning and cross-database composite objects, will become useful at a later date. There are cases where this technique is applicable today, usually to a set of applications from a single vendor or environment. As standards such as the CAD Framework Initiative interfaces come into wider use, a DBMS will be even more applicable.

Migration via surrogate objects

But what if the applications have no common data interface, or at least none accessible to you? Use surrogate objects. In this approach there's an object in the DBMS that's a place holder or surrogate for the actual proprietary file or database used by the application. The application uses the same file format in the same way, and hence need not change. More capability is provided if the application changes to open and close its file via the surrogate object. This change may be done in the application, and is almost always very simple. If no access to the application source is available, the change may be done in a shell or script that is wrapped around the file.

This approach lets completely foreign "black box" tools into the DBMS environment. The tools remain unchanged, with whatever functionality, performance, capability, and limitations they had before. Now, however, they can participate in DBMS capabilities such as versioning, relationships and composites, with the limitations that they do so only to the granularity of the file and not for any of the primitive data within the file. This method may be freely mixed with native applications that use the DBMS directly, storing their primitive objects directly in databases.

Over time, as resources allow and need requires, more applications can be converted to move their data from the proprietary file format into native objects, with the result that they will better utilize the capabilities of the DBMS at any level of granularity, with unlimited size, recovery and distribution.

Drew Wade, vice-president and cofounder of Objectivity, Menlo Park, CA

technical publications. This update is then expanded into the larger development environment, which hosts the other components of a product where engineering teams are doing concurrent development.

While products such as PowerFrame and TeamNet address the data management dilemma from a framework perspective—an infrastructure through which tools are accessed and changes tracked—the managers of today's complex design environments demand more. And though the task of managing data looks like one which dictates a global perspective, the problems actually begin at a component- or library-model level. "The real issue is primitive but it's critical," says David Hardman, product planning manager at Logic Automation (Beaverton, OR). "The way we name all this data—the component names, the pin names and the signal names—have to be the starting point for real data management. Trying to get everyone to agree on these names is next to impossible, so we'll probably have to

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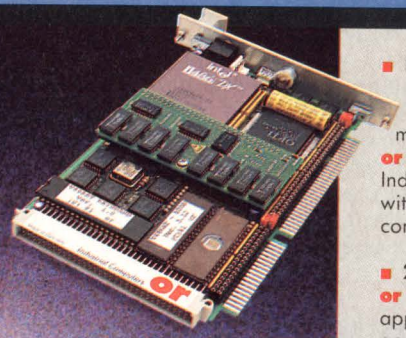

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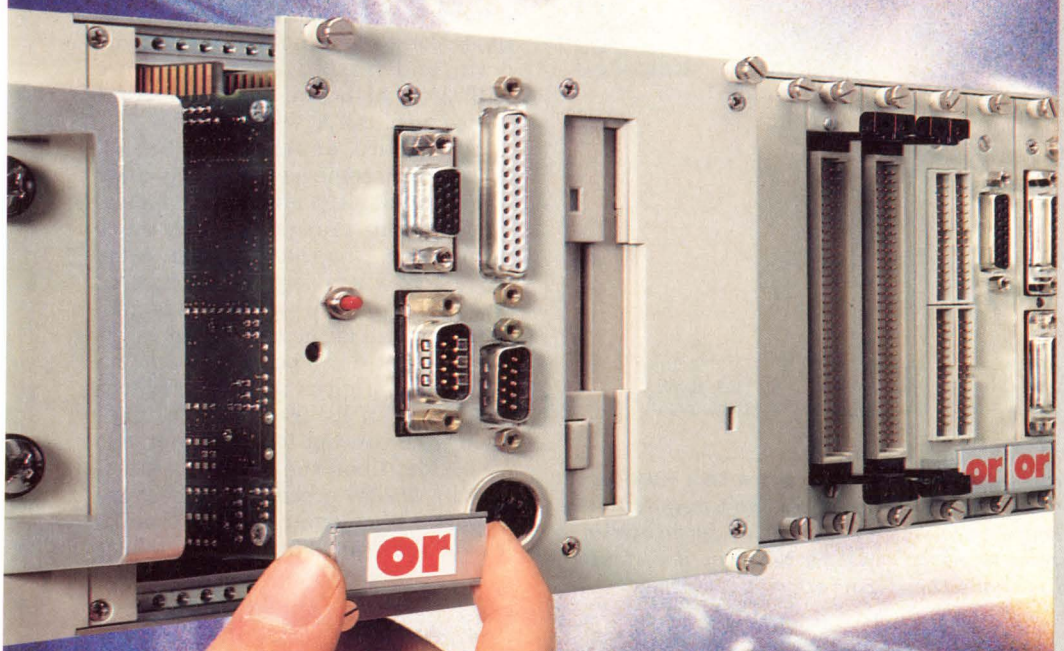

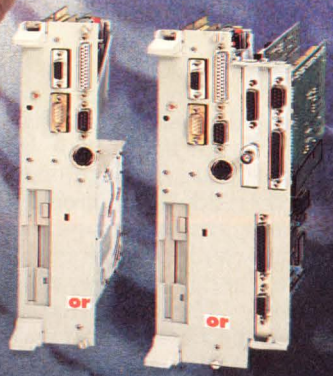

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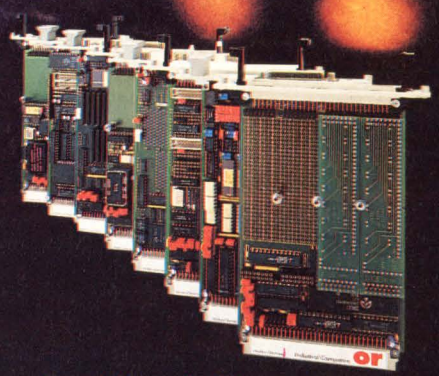

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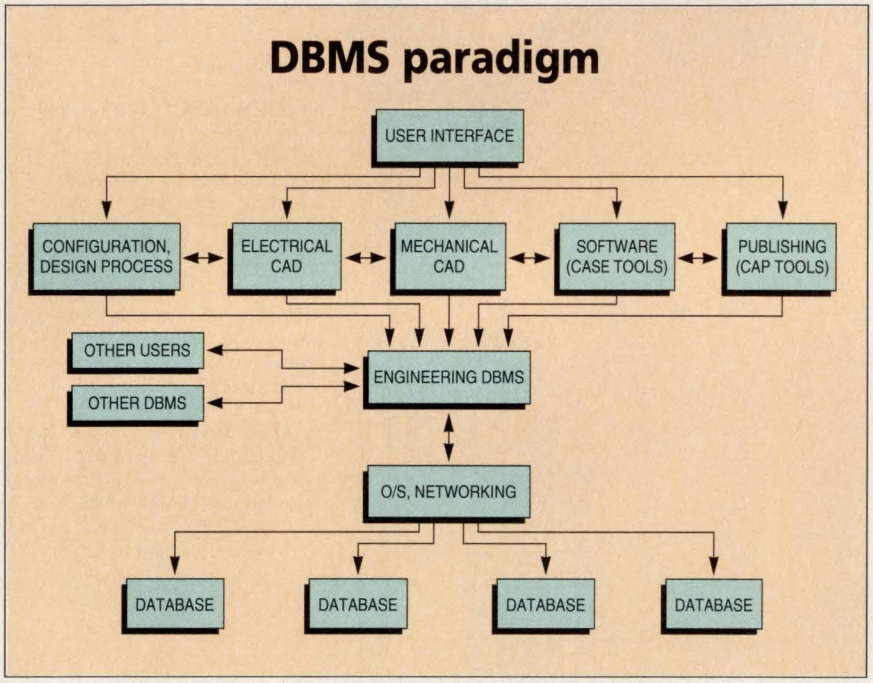
make the tools smarter to recognize what these names really mean."

CFI to the rescue

If relief through standards is going to come in the EDA arena, it will undoubtedly happen through the efforts of the CAD Framework Initiative (Austin, TX). One of the most important efforts for CFI right now is component information representation (CIR). While data representation is the way the components of a design are hooked together, CIR describes the library elements behind the design tools. Real integration of tools will come, therefore, when there are standards for libraries. "The key step here is to develop electronic data books to standardize CAD-sensitive information," says Joseph Flanigan, chairman of the CIR technical subcommittee at CFI. "We're trying to develop information models of components that everyone will understand so that we're all speaking the same language. The problem in trying to unify this data is that every company developed its own way of representing data over the years. But because it's such an important issue, we've gotten cooperation from the CFI members to try to hammer out standards. The hard part is getting engineers in the industry to believe that it's going to happen. Information used to be so proprietary and hard to get that you couldn't even ask a company for the structure of its CAD database. Now, no one would even consider buying a product without that information, or at least a procedural interface that would let them access it."

Similar efforts toward standardization of library elements are going on in the mechanical CAD world as well as in the CASE arena. When all these standards stabilize, interdisciplinary communication will undoubtedly be easier.



The ultimate goal of database management systems (DBMS) is to let the manager control access to multiple databases used for design, test, packaging, manufacturing, and software development. A drawing used in design, for example, can be used in manufacturing and appear in the product's manual. Changes to any portion of the design can be communicated on an as-needed basis to all affected disciplines.

Politics enters the fray

All of this activity to develop standards is directed at solving the technical problems that inhibit true interdisciplinary data management. There's another side of the problem which can't be solved by committees or standards—namely, getting corporations to change the way that they do things. The disciplines of electronic, mechanical and software design have traditionally operated as autonomous units, loosely connected through management meetings and over-the-transom communications. But even when the technology is available to manage the design data from these various groups, there will be battles over whose responsibilities and needs are paramount to a design's progress and whose are secondary.

It's clear that in addition to any technical solution offered, database-management companies must offer migration paths which will let people carry on with business as usual with minimum trauma to daily operations. No strategy will succeed if tool performance suffers or you're forced to spend inordinate amounts of time learning new interfaces. "No one's going to let a tool vendor come in the door and shove a methodology down everyone's throat," cautions Scott Passon, product marketing manager at Dazix (Huntsville, AL). "But management is telling their engineering teams that they want those long-standing walls to come down and many EDA vendors are willing to help find a solution that everyone can live with."

Managing design databases, then, will become a reality only after the technological and psychological barriers that impede its acceptance come down. One thing is clear. All of the glowing praise that concurrent engineering strategies have garnered and all of the talk about interdepartmental cooperation will remain meaningless until a product's progress can be tracked and managed from concept to production. No corporation has the luxury of starting the design process over because important information didn't make it over the transom. ■

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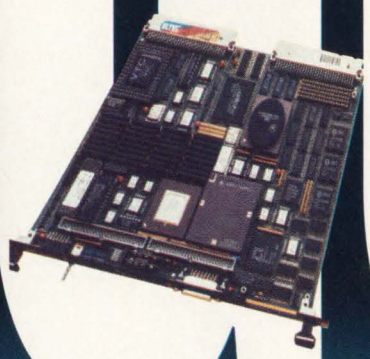

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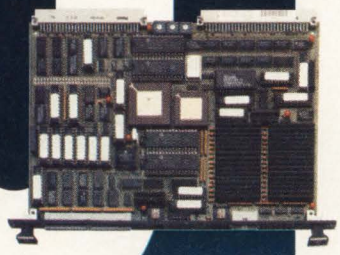

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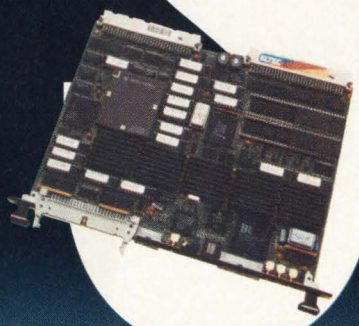

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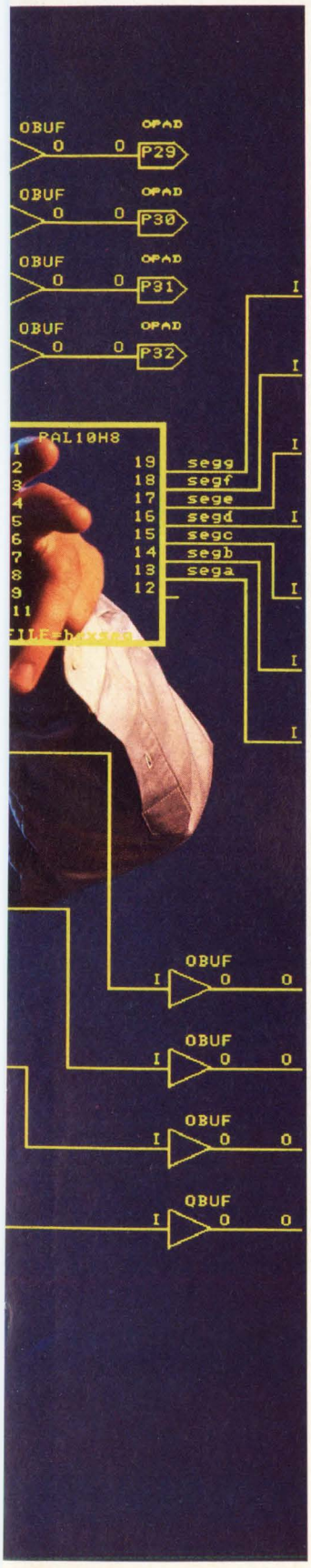

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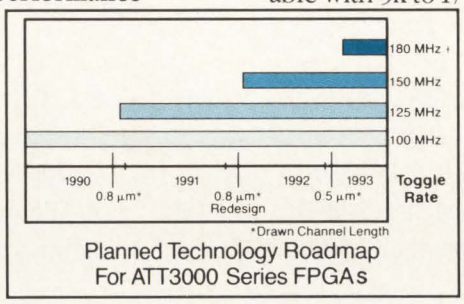

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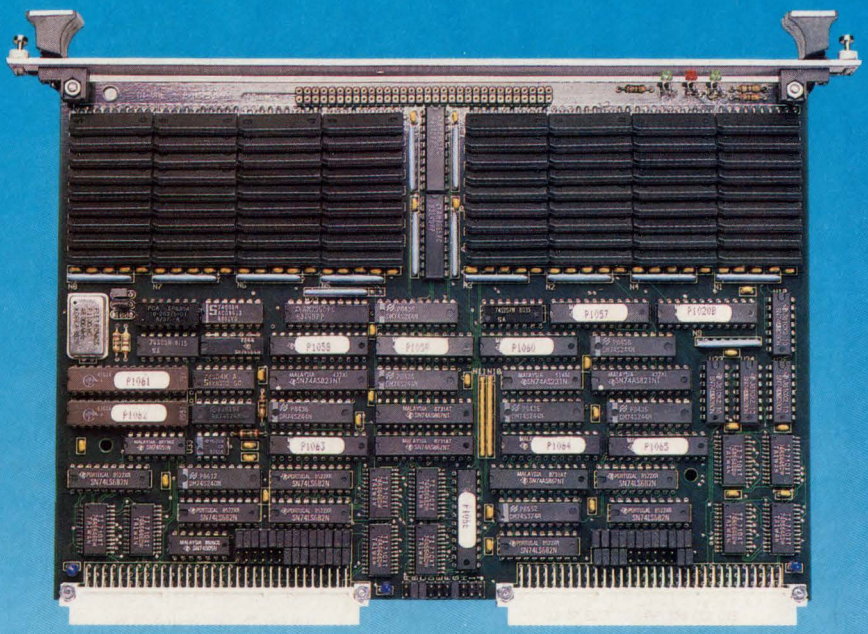

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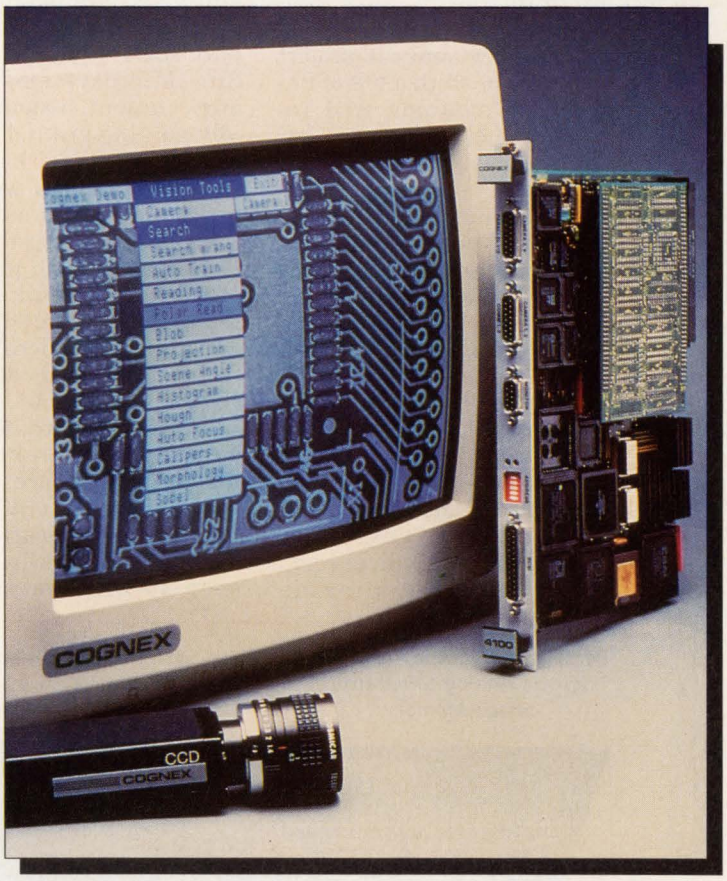
Standard buses gain ground in image processing

Image processing is getting a makeover, thanks to board-level coprocessors. Now, standard buses are accepting the technology into their social circle.

Warren Andrews
Senior Editor



Cognex has developed image-processing equipment using a VMEbus format optimized for machine vision, or what the company calls "image analysis," rather than image processing. As opposed to systems which provide enhanced or modified images, Cognex systems are designed to give a tangible result based on image analysis.

Image processing technology, though still in its infancy, has carved out an important niche for itself in the industrial and commercial computer world. Gains in this area have traditionally involved proprietary products, while makers of products based on standard buses have struggled to gain a foothold, but this situation is changing rapidly as the technology matures.

Improved chip technology—particularly for ASICs—has made practical real-time image processing possible, and putting these new chips to work on industry-standard buses promises advanced image processing to meet the high price/performance levels demanded by a broad variety of emerging commercial and industrial applications. "A number of things are acting to migrate image-processing technology to standard buses," says Mike Travis, product marketing manager of Data Translation (Marlborough, MA). "The major and most compelling reasons are those for which standard buses are being selected for other applications; these include system economies, interchangeability of subsystems, the ability to assemble systems from boards from multiple manufacturers, an upward migration path, and the ability to take advantage of standard operating systems, shrink-wrap applications and other software."

Steve Hendry, imaging graphics product manager for Radstone Technology (Montvale, NJ), concurs. "While there are no direct benefits to be derived from doing image processing on VME—or any other standard bus, for that matter—the indirect benefits that accrue are the same as for any other microprocessor-based system." Hendry says there may even be technical advantages to proprietary approaches, such as the ability to rapidly transfer image data from one subsection to another. At present, there's no established standard for transferring image data on any of the standard-bus

architectures, but the economic advantages and flexibility of standard-bus approaches far outweigh the possible disadvantages.

Volume pick-up

Although image processing is already a going technology, only a very small part of the action currently takes place on standard buses, and that activity is basically divided between VMEbus and ISA. "But the use of board-level products is going to pick up dramatically," says Hendry, "if market predictions are going to be met. Industry analysts project that the volume of shipments of image-processing systems will increase at a rate of 25 percent per year over at least the next four years."

This reflects a dramatic decrease in average selling price—some 14 to 15 percent per year. "The only way the industry will achieve this kind of reduction in the average selling price will be a migration to standard-bus-based systems," says Hendry.

While there's consensus that much image-processing hardware will migrate to standard-bus platforms, there's little agreement over which platform, if any, will be dominant. "A lot of applications," says Travis, "are migrating directly to the personal computer level. We see a tremendous interest in image processing on the PC in the scientific community, and now that's starting to move over to industrial applications."

However, Bill Kehret, president of Themis Computers (Pleasanton, CA), believes that most image-processing activity isn't occurring on PCs today, nor will it in the future. Much of the development work in this area is going on in the workstation environment, with its powerful processing and graphics capabilities—and primarily in the Sun Microsystems Sparcstation environment, although IBM is rapidly gaining ground with its family of RISC/6000 workstations.

"This focus on workstations for development and as embedded systems for industrial applications," Kehret says, "will provide a wealth of new opportunities on VMEbus and SBus for Sun-developed applications and on Micro Channel Architecture for those developed in an IBM environment."

Not everyone agrees. While workstations can handle some applications and are certainly used as development environments, "far too many applications today call for highly specialized hardware to keep up with real-time demands," says Susan Snell Solomon, product manager for Datacube (Peabody, MA).

VME continues strong

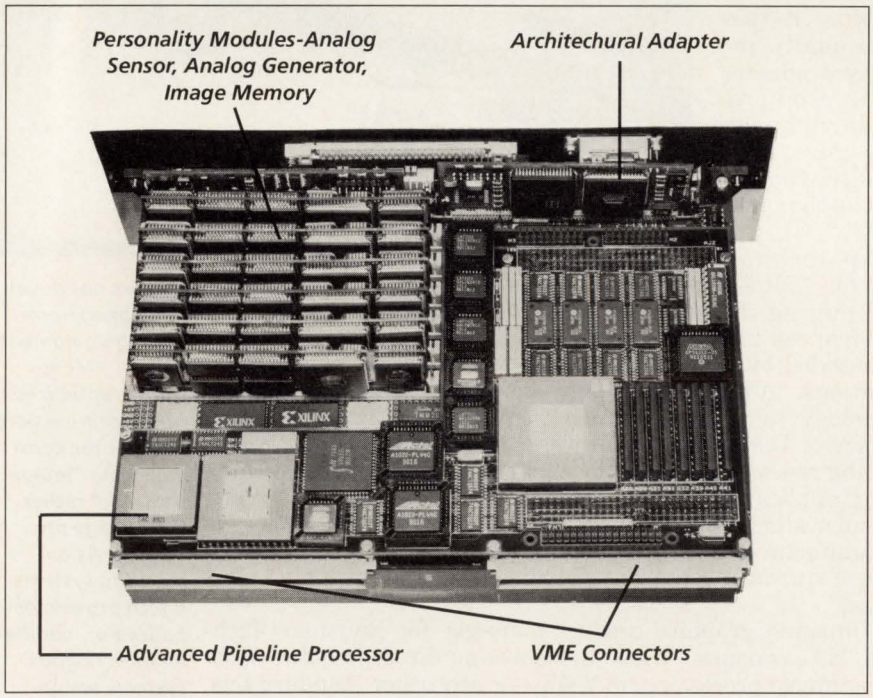
While some applications will undoubtedly move toward PC environments because of the relatively low entry cost and the wealth of DOS-based software available, there still exists a very strong base in the VME community. "For one reason," says Bob Ries, product manager for Cognex (Needham, MA), "many of the applications for image processing are on the factory floor, providing some kind of automated inspection, quality control or counting."

"Industry analysts project that the volume of shipments of image-processing systems will increase at a rate of 25 percent per year over at least the next four years."

—Steve Hendry, Radstone

These environments call for the kind of mechanical and electrical ruggedness that's been the hallmark of the VME form factor. In addition to ruggedness, there's also appearance. Customers purchasing an expensive system, whether it's a vision inspection system for the factory floor or an image processor for a medical instrument, don't like to see a relatively inexpensive PC controlling multi-million-dollar equipment. There also seems to be some agreement that VME offers real performance advantages which are often needed in image-processing systems.

On the down side, VME's data transfer rate of 40 Mbytes/s is fast enough to transfer only limited-resolution real-time image data, and there are some other problems as well. "First," says Reddiar Anbalagan, vice-president of Innovision (Madison, WI), "the system bus is often busy handling other tasks, such as system management and I/O, which are often critical in a real-time application. Second, properly transferring image data calls for a synchronous bus. Neither the



Taking advantage of specialized silicon and the flexibility of a standard bus is Datacube's MaxVideo family of image-processing boards. It uses the host VMEbus to communicate system information, while image data is transferred over the company-developed MAXbus.

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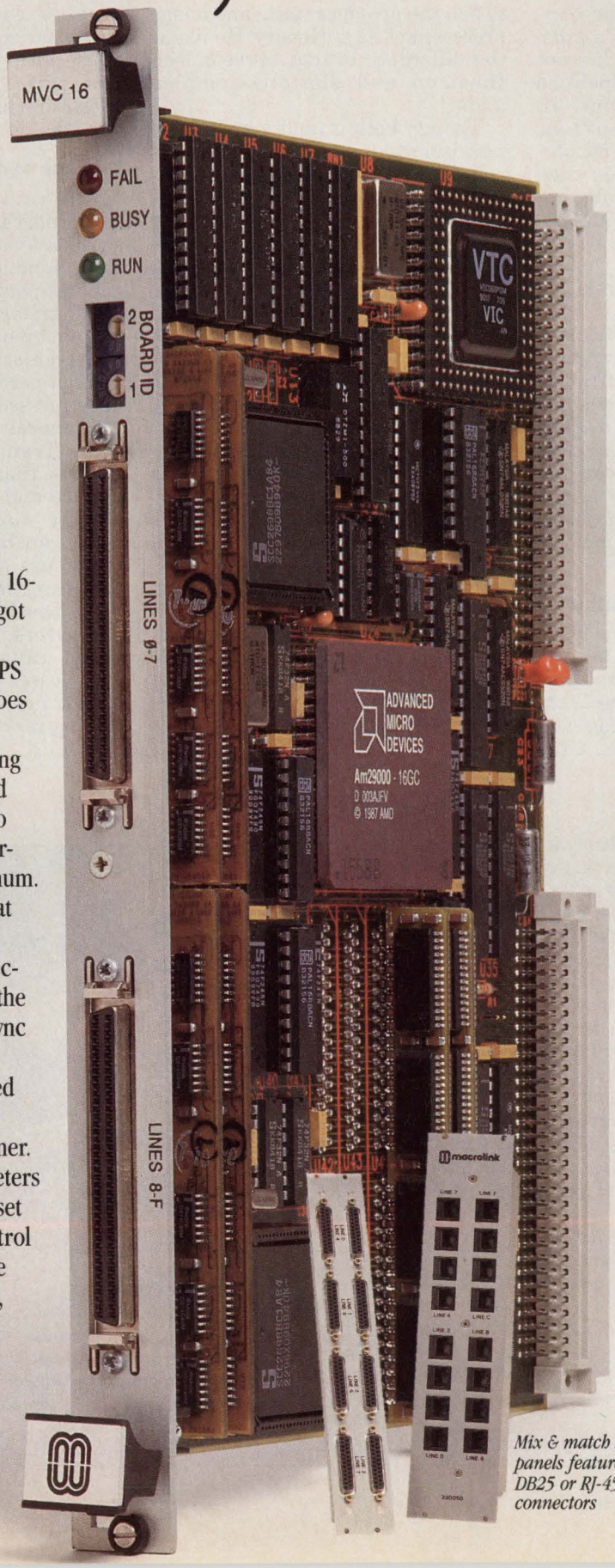

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VME system bus nor the optional VSB [VME subsystem bus] can fill the bill."

"But," Anbalagan continues, "VME is the only choice for complex imaging systems using a pipelined hardware approach. It's not possible to use such a pipelined approach using an ISA bus. In some cases, it's necessary to use one board to capture a frame and perhaps do some preprocessing, then feed that data directly to another that might, for example, do a histogram, and then on to other boards for additional processing."

"Aside from parameters relating strictly to performance," says Datacube's Solomon, "it's difficult to provide solutions in every format using one bus." Datacube staff made the decision early to select one bus architecture and stick with it. "The decision for that bus to be VME was helped along by one of our customers, General Motors, that demanded a bus architecture that met its stringent requirements. VME met its specifications," Solomon says.

Image processing and graphics

Though today's workstations have very powerful graphics capabilities, their processors are general-purpose RISC or CISC machines that can't manage the demanding and specialized number crunching demanded by many real-time image-processing systems. "There are some fundamental differences between the graphics world and image processing," says Hendry. He likens the difference to that between synthesized and digitally-sampled audio.

Though both graphics and image processing use similar approaches—a series of high-powered mathematical manipulations on pixels or groups of pixels—to achieve their goals, the actual way manipulations are done is different enough that the same hardware can't necessarily be shared (see "Image processing and vector graphics—the technologies combine," p. 87). Further, some image-processing applications are so complex that they require highly specialized hardware.

Despite this last fact, there are still entire families of applications that can be addressed with high-performance standard processors, says Kehret. "That's why Themis has taken the approach it has in developing a very high-performance, Sparcstation-compatible VME board that can handle image as well as other types of processing." (See "Full-featured Sparcstation 2 surfaces on VMEbus," *Computer Design*, February 1992, p. 128.)

"A few years ago," Kehret continues, "we developed a board exclusively for a particular type of image processing which combined a frame grabber with edge-detection circuitry for robotic control. The difficulty with that type of approach, though we've been quite successful with it, is that it addresses too small a market."

Image versus array processing

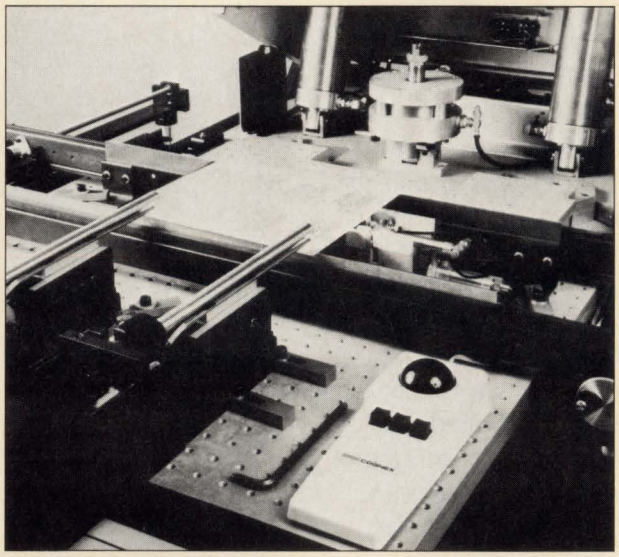
"There's no clear-cut definition of what constitutes image processing," says Travis. That's because the same functions can be handled by general-purpose processors such as the familiar RISC and CISC families, or by high-performance arrays of processors such as DSP chips, or by high-performance specialized image processors.

"General-purpose processing to Data Translation," adds Travis, "means that processor boards are flexible and can be programmed to do any number of things. Their cards can be DSP cards, and they might use a chip like the i860, or something like a Motorola 96000, or what has become known as array processors. They enjoy use in a broad range of applications. In many cases they are fast enough to handle non-time-critical image-processing tasks."

For machines only

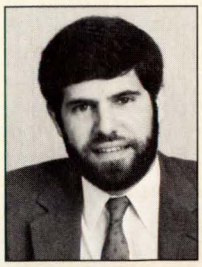
Cognex Corporation (Needham, MA), which specializes in machine vision systems, has developed a product family that's specifically optimized for image analysis. "We differentiate our approach from an image-processing system, which is something that's very good at processing raw pixels or numeric data on each position in an image," says Cognex product manager Bob Ries. "What we call an image analysis system, on the other hand, takes those images and produces some concrete result. Is there a defect or not? Or what is the x,y location of a particular part of the image? We do offer a full range of image processing, where you take one image and process it and get another image to, for example, highlight it. But the majority of our users are looking to analyze an image and get a result. This result is typically then sent over the system bus to another computer which, in turn, uses the result either as is, or with further processing, to generate some action."

To achieve their specialized functions, Cognex boards use one or both of a pair of specialized chips the company's developed and implemented as gate arrays. Its VC-1 vision chip is designed to perform certain specialized algorithms such as histograms, point transforms, normalized difference, projections, spatial averaging, boxcar filters, spatial moments, and normalized correlation. The companion chip, the VC-2, will perform real-time gray-scale edge detection, gray-scale morphology and rank-value filtering.



Cognex image processing/analysis equipment is used here to align material on an automated silkscreen printing machine. It takes advantage of image-analysis techniques such as edge detection and normalized correlation.

Image processing and vector graphics—the technologies combine



Historically, image and graphics processing have evolved as divergent technologies. One reason for this has been the different processing requirements for each. In the first, processing elements must be tightly coupled to pixel data acquired from a real-world input. In the second, the elements must be tightly coupled to the mathematical representations used to synthesize the polylines and polygons which, in combination, create the graphic image.

Increasing customer demand and the appearance of enabling technologies are now heralding the beginning of an era in which the convergence of the two disciplines has become a reality.

Complexity changes requirements

In the vector graphics world, architectures range from simple frame buffer and video controller designs to massively parallel processing elements and data paths. The frame buffer approach involves direct operation on the data by the host CPU, and, therefore, uses a sizable chunk of system resources for even fairly simple functions.

The addition of a display processor, such as the TMS340XX, offloads much of this work and greatly increases overall performance, requiring the host CPU only to issue commands and parameters. The coprocessor will handle all graphic drawing functions.

As application complexity increases—faster and more complex manipulations and shadings—so do the requirements for more processing power and more sophisticated architectures. Wider data paths and parallel processing are commonly used to produce acceptable high-performance solutions. A popular device used in this way is the Intel i860 processor, which uses 64-bit data paths and has the capability of running devices in parallel to increase performance still more.

Performance requirements above this level invariably require the use of array processing techniques, where each processing element performs a task in parallel and produces results that can be passed to other elements within the array for further processing. Data paths are wide, 64 bits or greater, and memory bandwidth is very high. Typically, this architectural approach is implemented using bit-slice techniques or custom VLSI, with drawing and transform algorithms stored in firmware or hard-wired.

A dedicated image-processing (IP) system usually has a pipelined architecture. An image is captured and well-defined operations are performed, typically one at each stage of the pipe, before final display and storage take place. The advantage of this approach is that each stage is optimized for its particular task—hence, high-speed processing is achieved. The down side is that the pipeline is dedicated to a limited application area and, therefore, may not be particularly cost-effective.

The requirements for high-performance graphics and high-speed IP engines, then, are very similiar.

Different approach needed

As is the case with high-performance graphics products, a more general-purpose image-processing engine demands a different approach—that of parallel array processing. Here an image is captured and placed in memory, where it can be accessed and operated upon by the processing elements, and the results are stored back into memory. Each element performs a pixel calculation, the result of which is fed to other elements in the array. This capability is essential for convolutions and other array-based algorithms.

By applying high memory bandwidth techniques, data can be transferred to and from the processing array in a highly efficient manner. Also, because it's a memory-based structure, the processor can access individual pixels to store and display intermediate stages of the processing. Since it's essentially software-driven, the system can be modified easily. A pipelined architecture can't typically be modified in this way.

One disadvantage of high memory bandwidth approaches is that memory cost increases. This increase is usually more than offset, however, by the inherent flexibility the approach brings to the system; this can provide substantial savings over dedicated pipelined machines. A general-purpose engine of this type is also typically implemented using bit-slice techniques or custom VLSI, with IP functions hard-wired or in microcode. The host computer then must only provide high-level function calls to implement sophisticated and high-speed IP functions.

The requirements for high-performance graphics and high-speed IP engines, then, are very similar—parallel array processing, wide data paths, bit-slice and custom VLSI, functions embedded in microcode or hard-wired. Developing an appropriate architecture can enable both graphic drawing functions—for example, fills, lines, shading, and transforms—and IP functions—thresholding, erosions and convolutions—to be efficiently implemented on the same machine without compromising the performance of either. Once so combined, the separate graphics and image-processing functions simply become a broad spectrum of image manipulation techniques.

Imaging × graphics = growth

The combination of imaging and graphics may well herald the growth of a substantial, commercially attractive marketplace. But no one should take the two for "the same thing" or underestimate some of the technical challenges faced in drawing them together. Imaging and graphics are an increasingly synergistic combination for enhancing work in the scientific, industrial, medical, military, and graphic communities—with even more benefit likely to result in the future from this powerful new tool.

Joel Silverman, marketing manager for commercial products, Radstone Technology, Montvale, NJ

In addition, there are instances where end users have highly specialized requirements that won't be satisfied with more restrictive image-processing hardware. Where users have developed their own algorithms to perform particular image-processing tasks, for example, general-purpose boards are the only choice. By definition, image-processing boards implement their processing algorithms in hardware, permitting them to run faster.

"But what really differentiates one from the other [image from general-purpose processors] is speed," says Travis. "As fast as DSP and general-purpose processor chips such as the i860 are today, none of them is fast enough to do image-processing work in real-time. The place for what we call specialized processors is really real-time work."

"For example," Travis continues, "we have a set of ASICs that does color-space conversions. It converts red, green and blue images from a conventional television camera into HSI [hue, saturation and intensity] signals which are easier to process digitally. That's a process that normally would take more than a minute per frame using a very fast 80486-based PC. Our chip set performs those conversions in real-time—about 60 times a second." The penalty for such use, he adds, is that the board isn't useful outside image-processing applications.

Speed or flexibility

Considering performance as a spectrum, it's possible to visualize specialized machine vision systems such as the one produced by Cognex at the top of the scale, and yet most limited in the type of applications it can address. At the other end of the spectrum are digital signal processor, array processor and general-purpose processor boards, which are greatly inferior in performance but yield the ultimate in flexibility.

Between the two approaches lie products such as Datacube's MaxVideo family of boards. Initially Datacube put together boards which shared the VMEbus, but used a secondary bus of Datacube's own design to transfer image information between boards in a system. In Datacube's approach, each VME board in the system was designed to handle a specific function in the image pipeline. Individual boards tackled different programmable tasks and the boards were tied together with the company-designed MAXbus.

Datacube relinquished all proprietary rights to its MAXbus and, according to Solomon, some 15 vendors now support the bus with various products. In addition, she adds, another 10 to 15 large companies use the bus internally. While Datacube makes extensive use of ASICs in its boards, they are more generic in the types of tasks they perform than Cognex boards. While this may result in some performance penalty, it's offset by flexibility.

Datacube recently introduced its next-generation product family, the MaxVideo 20, which uses small modules to combine the functions of its earlier family of VME boards onto a single board. The 6U VME board (motherboard) contains the VMEbus and MAXbus interfaces. Connecting all the plug-in modules is a 640 Mbyte/s, 32×32×8-bit internal crosspoint switch that permits high-speed data path switching at frame rates of 60 Hz and above. The board supports up to six image memory modules.

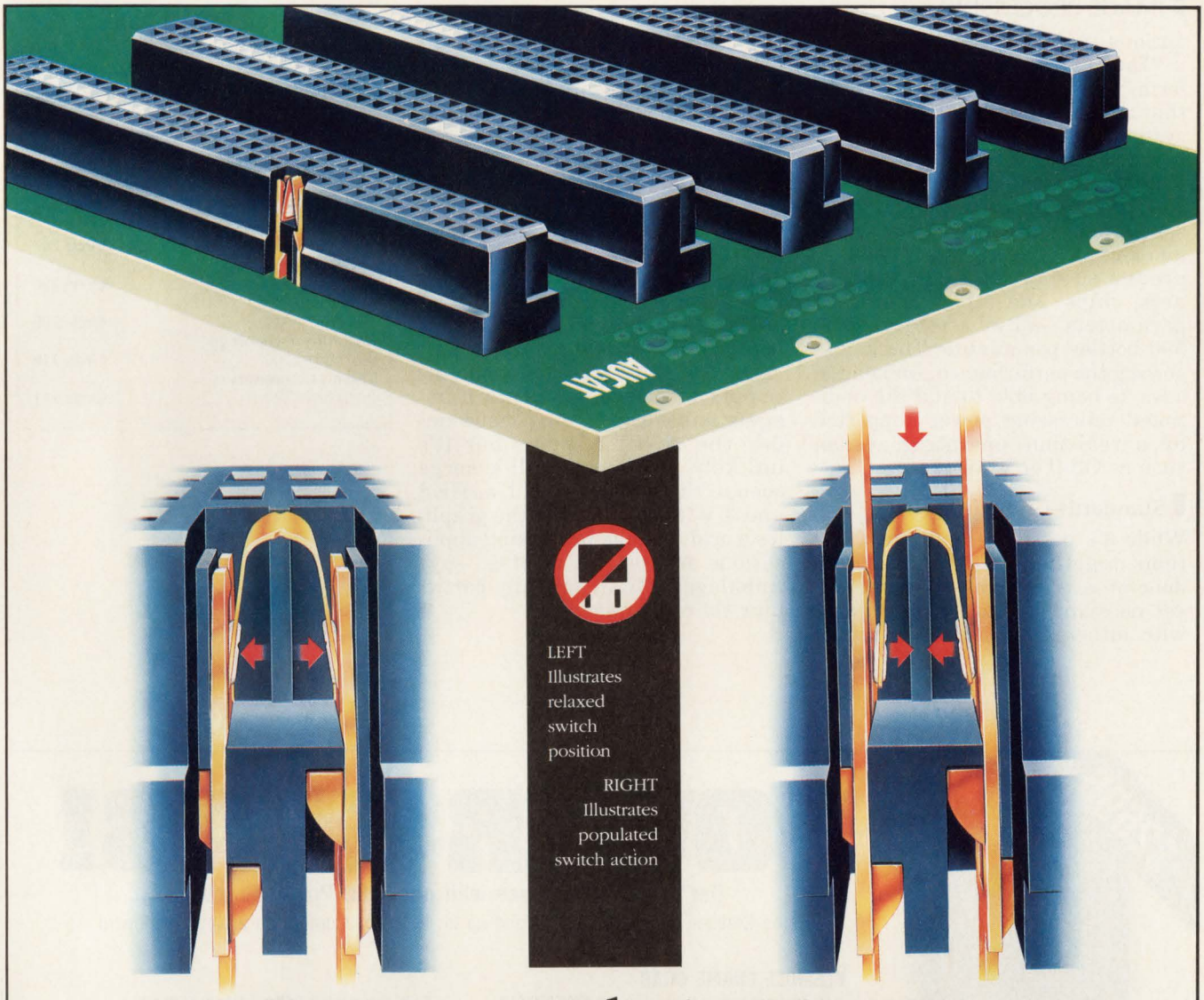
The daughter cards, called MaxModules, provide different processing capabilities for special user applications of the MaxVideo 20. Other functional boards are available to let you customize the MaxVideo 20 to specific applications.

Innovision has developed an image-processing system around the Datacube MaxVideo 20 VME board and a 68030-based host computer. The system offers both hardware and software flexibility to easily fit into a variety of image-processing applications. Its Idas image processing system's Interpreter software menu offers easy-to-use pulldown menus for manufacturing inspection, surveillance and tracking, as well as medical imaging such as the CT chest x-ray analysis shown here.

Applications oriented

Flexibility, believes Anbalagan, is an essential ingredient in the practical application of much of today's image processing hardware. "No two applications in image processing are the same," he says. "Each application is sufficiently different that it would not be practical to provide totally custom chip-level hardware solutions for each. Therefore, some performance has to be sacrificed to have the flexibility necessary to tailor the hardware to the application."

"Innovision," continues Anbalagan, "gets the flexibility it needs by using a MaxVideo 20 for the real-time imaging part of its Idas/MV20 system." The company's latest product uses, in addition to the MaxVideo 20, a 68030-based system controller and lots of image memory. In addition, it includes a standard collection of peripherals, such as hard and floppy disks, serial ports, and a parallel port, as well as other



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options.

"The advantage to the VME platform," according to Anbalagan, "is that it's possible to take a standard system and add additional processor boards as needed to fit into any particular application." He cites a European application involving inspection of bottles to be recycled as an example. The system checks for proper shape, labeling, cleanliness, chips, and other significant parameters—all at a rate of some 500 bottles per minute. The key to getting the performance, Anbalagan says, is being able to add the additional processing power supported by a real-time operating system such as OS-9 or VxWorks.

Standards—slow in arriving

While it's possible to put such systems together—and, indeed, it's done on a regular basis—there are yet no standards to help designers with either hardware or software. Datacube's MAXbus is probably the most widely used of any secondary imaging bus to communicate image data from board to board, yet it's far from being a standard. Similarly, Data Translation's DT-Connect and DT-Connect 2 have multivendor support, at least in the AT world, but they are similarly far from representing a real standard. Imaging Technologies (Bedford, MA) offers its version of a transfer mechanism, a Pixel bus, but it's not aimed at being an industry standard either.

On the software side, some attempts to develop a software image standard are being made under the ANSI banner, but it's unlikely standards will emerge soon in the imaging world, as GKS and X Windows have in the graphics world. "Image processing applications are just too diverse," says Anbalagan, "to fit into any particular set of standards." ■

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Designers can now take their pick of 32-bit debugging tools

Jeffrey Child
Associate Editor

Complex bugs in 32-bit embedded systems can seriously ruin your day. As processors get more sophisticated, many 32-bit projects require emulation more than ever. But the rising cost of emulators can burden budgets, forcing designers to choose between spending big bucks for bug-hunting tools or exploring lower-cost debugging alternatives.

Until its most threatening bugs have been hunted down and killed, no complex embedded system design is completely out-of-the-woods. For a long time, emulators were considered the best bug-hunting tool for embedded systems. But today, with a wider selection of debugging tools available, engineering managers have more decisions to make. Besides choosing the most appropriate tools for their applications, they need to select tools suited to each engineer's specific role in the software development and hardware/software integration processes.

It's difficult to know how much buying an emulator will gain you in productivity until well after you've made the investment. The value of most tools lies somewhere in the gray area between "desirable" and "absolutely vital," but the more expensive the tool, the more reluctant a design team manager will be to squander precious engineering dollars on it. With budgets under tight scrutiny these days, designers implementing the latest high-speed 32-bit microprocessor-based designs in embedded systems may welcome an alternative to buying an emulator. Most admit, however, that there's no real substitute for a full-blown in-circuit emulator for debugging systems in real-time. As processor speeds reach 33 MHz and go beyond, however, many designers are questioning whether it's feasible to build emulators at a reasonable price.

When it's time to put your money where your megahertz are, you must carefully choose what level of debug capability is required for your particular 32-bit embedded application. In general, this choice centers on two questions: Does the larger scale of 32-bit projects mean emulators are more vital then ever for solving complex debug problems? Or should you consider lower-cost debugging tools and instrumentation for some or all of the design team?

A question of productivity

"Before I can justify the dollars to management, what I'm looking for is productivity increases," says Stephen Butterfield, vice-president of hardware development at Peerless (Redondo Beach, CA), a maker of laser printer controller boards. "For under $10,000 you can find a fine logic analyzer that has disassembly capability. Before we step up from that $10,000 to a $25,000 emulator, we need to see the productivity increase that it will bring to the party. We spend well over half to two-thirds of the project time on the bench working with these instruments. I'm willing to spend the bucks for the productivity increases."

Statements like this illustrate the range of decisions faced by many engineering managers in charge of 32-bit designs. Emulators speed the tasks of finding bugs in the software and integrating intricate operating systems with the hardware by helping designers find bugs deductively, rather than inductively. "All of the cheap ways of solving something are based on inductive reasoning," says Richard Jensen, vice-president of new business development at Applied Microsystems (Redmond, WA). "Therefore, if you happen to have a problem that, because of complexity, scale or time relationship, is extremely hard to find, you can flounder for months. And if you have a whole project team that suddenly comes to a screeching halt because you're floundering, whatever you pay for an emulator doesn't matter compared to your project cost."

Much in common

While it's rare in the computer and electronics industries to find cases

where both emulator vendors and their users have the same perspective, by and large emulator vendors are quite sympathetic to the situation faced by embedded systems designers. Perhaps this isn't so surprising, considering that emulator vendors and designers are using the same sophisticated microprocessors. "Remember, the emulator itself is really an embedded system with a really tight design rule," says Jensen. "To do an emulator, we have to know a chip inside and out, backwards and forwards. So we have already solved the problem of making an embedded system using that chip."

Vendors and designers agree that the speed and complexity of 32-bit processors introduces a slew of problems that weren't an issue at the 8- and 16-bit levels. First, there are the simple linear problems that occur at 32 bits, such as wider addressing. The data capability of 32-bit chips means more pins and signals to deal with. Then there are the architectural complexities of 32-bit RISC and CISC devices—internal pipelines, multiple execution units for floating-point and on-chip caches.

While these boost performance, they also confound the emulator's ability to observe the internal work-

ings of the chip, which in turn inhibits the emulator as it tries to correlate activity on the system bus with high-level instructions. Finally, the speed of the latest processors contributes to the cost of emulation. The rule of thumb has been that you will pay $1,000 per MHz of clock speed; this rule still holds up reasonably well for most full-featured emulators, although a few emulator vendors have broken that barrier in the last year.

It's clear that the cost of emulation will continue to be a problem, especially because of the speed issue. Applying the $1,000/MHz rule, an emulator for a 25-MHz processor costs about $25,000. In fact, emulators introduced in the last few years for 32-bit RISC processors have all been priced at close to this figure. Emulators for the 68000 and 80X86 processor families have tended to cost a few thousand dollars less. If this trend continues, a 50-MHz emulator should cost about $50,000.

Worse, faster devices can process more instructions, leading to larger applications that require larger teams of engineers. Teams of 10 engineers are not uncommon on projects these days. To outfit a team this size working on a 50-MHz microprocessor-based design would cost $500,000—enough to make any manager think twice.

Among the reasons designers balk at emulator prices is that, more often than not, an emulator is built for a specific processor. If you decide on your next design to switch to another processor, even one in the same family, that often means buying a new emulator.

Emulator vendor Hewlett-Packard (Colorado Springs, CO) addresses the cost issue by providing a modular emulation system; modules are reusable, and the system can be upgraded. The 64700 emulator series, for example, starts with a basic frame containing a host processor, power supply, communication channel, LAN, and backplane. Within the backplane you can configure the system to suit your requirements, outfitting it with a logic analyzer module, a target module with a probe, or an optional real-time software performance analysis board. If you buy all this for the 68020, and then decide that your next project will have a 68030 in it, you save your frame, analyzer and target board and simply change the probe at the end of the cable. In such a case the upgrade would cost you only $9,000 to change to the new target.

From his experience developing laser printer controller boards based on 32-bit RISC processors, Stephen Butterfield (standing), vice-president of hardware development at Peerless, discovered that some processors have better tool support than others. Butterfield is willing to pay for an expensive emulator, provided it increases his team's productivity. He measures productivity in terms of an emulator's learning curve, features and its ability to provide reliable and accurate data. Also shown (inset) is the Peerless printer controller board in its system box.

Productivity and support

Butterfield and the design team at Peerless faced a support problem. Over the last two years, the team has developed several laser printer controller boards, all based on 32-bit RISC microprocessors—the Intel i960KX and i960CX series and the MIPS R3001, R3051 and R3052.

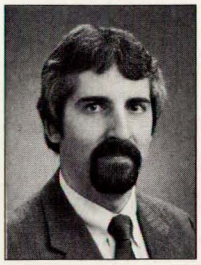
In the process, the Peerless designers found that some processors had better tool support than others. "For the Intel i960KX series we primarily use Intel emulators," says Butterfield. "Intel makes a very fine emulator for the i960KX. It's an excellent tool for debugging large bodies of hardware and software." For the i960CX, Peerless bought an emulator from Step Engineering (Sunnyvale, CA). After struggling with it for six months, the team decided to put it on the shelf. Butterfield explains, "The user interface is so cumbersome that it was impossible to use. It took far too many keystrokes to be able to key anything in. We had a hell of a time just getting it to even operate in the system." Step Engineering has since come out with new a i960CA emulator with a Windows front end to ameliorate the interface problem.

For development tools in general, Butterfield measures productivity in terms of the time they save. "[Effective time] is extremely difficult to quantify," he says. "Productivity involves issues of the user interface, of the learning curve for the tool, of the features that it has, as well as the reliability and accuracy of the data presented by the tool. We've had several debuggers that didn't disassemble code properly. Whenever you look at the screen you've got to wonder: 'Is this one of the misassembled instructions?' That sort of question forces you to take extra time in the debug process."

The right time and place

Senior staff engineer Jeff Rold at Hughes Aircraft (Newport Beach, CA) feels strongly that there's a time and place for an emulator: "When it's a new hardware design and you're writing all the code yourself," he says. "I also think that someone

Networking in-circuit emulators



For many embedded system designers, the in-circuit emulator continues to be the preferred tool for the integration phase of product development and debug. The nature of the development environment and the debugging task have changed significantly over the last 10 years, resulting in tools that have evolved to address those changes. One of the most significant developments in the in-circuit emulator has been the addition of networkable interfaces.

Advantages of network interface

To understand the advantages of a network interface, it's necessary to review the forces effecting the change. At the beginning of the 1980s, there were two popular approaches to in-circuit emulation—one the dedicated microprocessor development system (MDS), such as H-P's 64000, and the other the stand-alone emulator, such as Applied Microsystems' ES1800. The dedicated MDS typically comprised a proprietary development computer, cross-development software and an integrated in-circuit emulator. The stand-alone emulator, on the other hand, had a character-based RS-232 interface used in combination with program and symbolic information downloaded from a generic host computer. Each approach had its advantages, but over time the dedicated MDS was rendered obsolete by the introduction of the general-purpose desktop workstation and the personal computer. As larger 16-bit and subsequently 32-bit embedded designs became common, however, the benefit of the stand-alone approach started to diminish as code complexity and volume of symbolic information started to exceed the instrument's processing capacity.

Modern in-circuit emulators are generally computer-controlled pieces of equipment, a complex source-level debugger providing the operator interface of choice. The increase in addressing capacity of later processors, particularly 32-bit microprocessors, has had a significant effect on the size of applications and also the size and composition of development teams. While the number of emulator users may not be significantly greater than it was five years ago, many more engineers are involved in creating the application software that will eventually have to be tested in the prototype or "target" environment.

Key needs for networking

The volume of application code that's being debugged and, therefore, transferred between host computer and emulator has risen dramatically. Many emulator vendors now provide emulation memory options of several megabytes to support this trend. For large embedded application developers, the RS-232 suffers unacceptable delays when downloading these large applications; waiting for download can represent a significant enough interruption in concentration to be counterproductive. Point-to-point solutions such as SCSI can significantly improve download speed, but they are not as flexible as an Ethernet-based topology. Some SCSI emulator implementations can be remotely accessed over a network, much like a remotely mounted disk volume, but they still require physical proximity to at least one computer. The abstraction of the source-level environment carries a high communications overhead of its own. At the assembler level of programming abstraction, the stand-alone emulator user usually only issues one command at a time to the emulator—such as "display registers." A source-level debugger, on the other hand, will translate a debug command into requests for multiple actions by the emulator hardware. A typical source-line single step, for example, may require as many as 20 different emulator operations—memory requests, register requests and breakpoint settings—to support the windowed debugger display, as well as deal with possible multiple program exit points from a single source statement. A high-speed communications link is essential for the tool to be used productively. For many engineers working on larger systems, the prototype being developed is remote from their work cell or office. With the larger teams inherent in complex, large application development, it's no longer possible—or even appropriate from a project management perspective—for all engineers to have local access to targets and emulators. Workstations have also let embedded software engineers be most efficient at their own desks, rather than in a hardware-oriented development lab. It's essential, then, to be able to remote-access today's emulators from the engineer's local station.

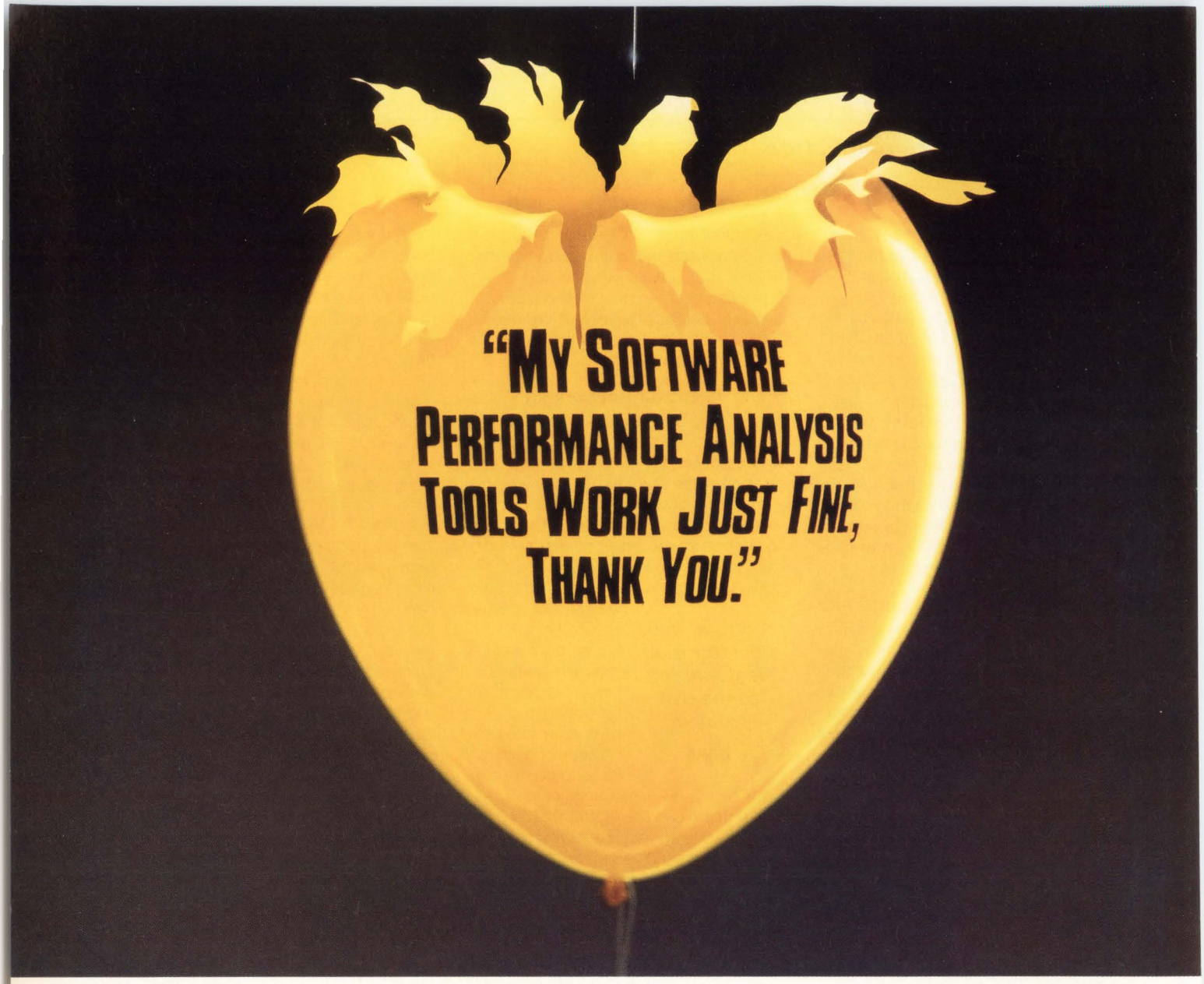
A networked emulator is an ideal solution to the cost problem.

Shave to save

Like the microprocessors they emulate, high-speed 32-bit emulators are much more expensive than their 8-bit counterparts. Over time they follow traditional technology learning curves and decrease in cost, but at the front of the technology envelope they are typically too expensive to proliferate throughout a large engineering team. It's extremely advantageous to be able to share a high-end emulator among several engineers. Coupled with a flexible network licensing scheme for the source-level debugger, a networked emulator is an ideal solution to the cost problem.

In many engineering environments, an Ethernet topology is already used, sometimes with several nets connected with bridges and gateways. A network emulator can then be added as easily as assigning a new node identification and tapping in to the network; the emulator can then be used anywhere on the subnets. Where several engineers have contributed to code integration, the ability to demonstrate a bug or anomalous behavior at each station, independent of tool placement, aids considerably in the debugging process for the lead engineer responsible for the project. An additional benefit of emerging X-based debugger applications and TCP/IP (Transmission Control Protocol/Internet Protocol) networks is that, even if the emulator vendor's debugger doesn't run on the chosen platform, it's possible to add a workstation as an emulator "application server."

Steve Dearden, director of product marketing, Applied Microsystems, Redmond, WA



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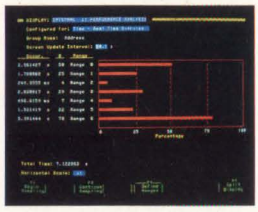

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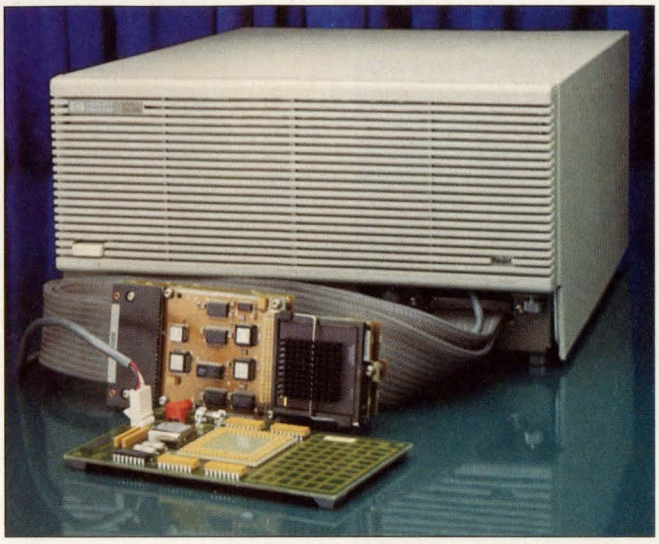
who's doing operating system development needs one." Hughes Aircraft, a manufacturer of display systems for air defense and air traffic control, has used emulators from Embedded Performance (Santa Clara, CA) to develop a graphics generator card based on the 29050 RISC processor from Advanced Micro Devices (Sunnyvale, CA).

In general, Rold feels that emulators are a necessity for solving certain hardware problems. "There are cases where there's a hardware problem that you can only induce through the CPU," he says. "This includes getting something simple to work, such as downloading code to RAM and having it execute. With an emulator it's much easier to just code in a loop and let the emulator run some routine that's causing your hardware to be exercised in a way that will make it fail." When Hughes designers had a memory problem on a card, they found the built-in memory test of the EPI emulator very useful.



One reason emulators are such a strain on engineering budgets is that every processor requires a separate emulator—even processors of the same family. To address this situation, Hewlett-Packard offers a modular approach with its 64700 emulator series. The 64700's basic frame has a host processor, power supply, communication channel, LAN, and backplane. You can add modules such as a logic analyzer, target debug module for the 68020 or real-time software performance analysis capability. When you decide to upgrade to a 68030, you need only add a new target module and probe.

Although designers at Hughes Aircraft typically use emulators, they've also found that simpler solutions may suffice, especially when several software engineers are working on a project. "We've done a lot of work in which we've put an operating system such as VxWorks on a Motorola MVME147 VME card, and then we don't use an emulator at all. Instead, we use software debugging provided by the operating system. That's a much cleaner environment to develop software in. On the other hand, using an emulator requires a fair amount of hardware knowledge. I'd fear throwing a computer science major at that kind of work," Rold says.

Honing your code

The place for emulators is on the desks of key system integration engineers, but there's more than one time in the design cycle to make use of emulation. In addition to its roles in the software development and hardware/software integration phases of a project, emulation plays a part at a later stage of design, when software performance analysis is taking place.

Most full-featured 32-bit emulators have the ability to do histograms and performance analysis on running software. You can determine how much time is spent in each module, how long it takes to process the data from a partition and other factors that reveal how many clock cycles are used for actions performed by software.

While such quality measures as software performance analysis are routine for military designers such as those at Hughes Aircraft, using it is also a good habit for any designer on a project in which speed makes a difference. "In a real-time graphics system, it's no good if you press a button and it takes two minutes for a display to update," says Rold. "An emulator is really essential there. It provides a real close look at how your code's executing. An emulator lets you examine the assembly code that your C compiler generated. Then you can tweak your C code to make the assembly code come out better."

Emulators not always needed

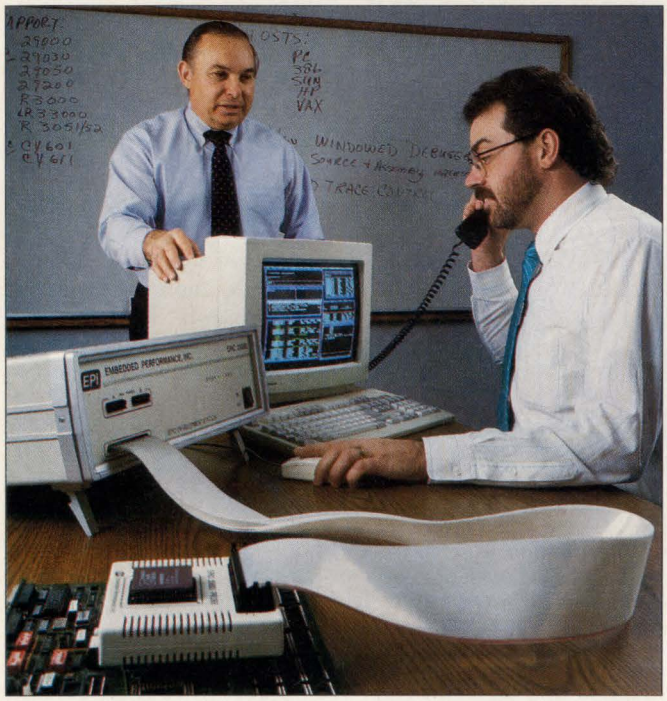
There's no doubt that software engineers now outnumber hardware engineers in creating 32-bit microprocessor-based designs. While such projects require more code development, 80 percent of their software must only interact with other parts of the software, since most complex embedded systems use a layered approach that isolates one part of the code from another. The remaining 10 to 20 percent of the software interfaces with the hardware, and is normally the only code facing complex time-domain problems. Developing this lowest layer of hardware-interactive code is the job of the emulator. For the rest of the code, software designers usually opt for a lower-cost tool such as an instruction-set simulator, ROM monitor/debugger or Applied Microsystems' Codetap.

ROM monitors, unlike emulators, connect directly into the system being debugged. This means that if the target system crashes, the ROM monitor crashes along with it. Both Microtec Research (Santa Clara, CA) and Intermetrics (Cambridge, MA) offer ROM monitor/debuggers that use their own symbolic debuggers as a front end. One key difference between the two debuggers is that the Microtec monitor can only be accessed via the host computer. The Intermetrics product, by contrast, provides the option of debugging directly on the target system. This lets you rule out bugs due to delays along the host-to-target interface. (For a discussion of ROM monitors see "Using ROM monitors for debugging 32-bit applications," p.104.)

Applied's Jensen describes his company's Codetap as a very watered-down emulator. It takes all the complexity out of the emulator—everything expensive, such as wide, deep trace buffering, the large number of signals needed to support trace, and conditional events that don't interfere with the clock rate. The advantage of Codetap over ROM monitors is that it provides hardware monitoring that a software monitor couldn't see. Unlike ROM monitors, Codetap brings its own resources into the game. You don't have to bind to your target system before you have a debugging tool.

Most software engineers don't need a full-blown emulator because they seldom need to run their code on the target system. When a problem is found whose solution isn't apparent from looking at the code, however, it's useful to move over to an emulator. To ease the transition, EPI has developed a small kernel that can be linked into your software, letting you interface the target board to the host computer and its debuggers. EPI calls this target-resident kernel an RSS (remote server software debug kernel) module.

"With this kernel, about 15 kilobytes of code actually get linked in the target," says EPI president Norbert Laengrich. "Of that, a little less than five kilobytes is the communications part of the code. If you're doing a complete custom interface to your board, you only have to touch five kilobytes of code to port it over to your board. So you're now dealing with a minimal amount of control software done at the target level, and all your debug power is up at the host level." Because the kernel is relatively small, porting it to the target system is fairly easy. In contrast, target-resident monitor/debuggers are at least 300 kbytes in size, and can take months to port in some cases.



EPI president Norbert Laengrich (standing) feels that it's important to provide a comprehensive set of tools to address the needs of the design team at each stage of the design cycle. To let software engineers start their work earlier in the cycle, for example, Laengrich suggests using tools such as instruction-set simulators or target-resident kernels instead of full-featured emulators.

Advantages of networking

As the larger teams required for 32-bit designs proliferate, the need for a networked tool becomes critical. Quite often the person who's doing the code integration isn't the person who actually wrote the code. In fact, it's more than likely that he or she didn't write it, since typically the person doing the integration is a senior-level system engineer with more overall project responsibility than someone who's writing software modules.

A team member with a problem doesn't want to be physically restricted to a single location, because quite often he or she must travel to find out what's going on with a particular piece of code. "When an engineer discovers that he's got some kind of problem in a certain area of the application, he'd like to be able to walk over to the guy's cubicle who wrote it [the code] and say, 'Let me show you what's going wrong and what I think is happening with your piece of code,' " says Steve Dearden, director of product marketing at Applied Microsystems. "That's not possible if he's got to physically move the target system and emulator to that location. But if you've got a networked emulator, then you just mount it like it was a printer somewhere off on the network—but you can do it from wherever you log into the network. That's probably the largest single advantage that networking emulators brings."

Networking emulators brings a number of other benefits as well. A good implementation means that your downloading speeds are considerably higher than they would be with a connector such as the RS-232. That's especially significant with 32-bit applications, because you're moving large amounts of application code from your development environment down into the debug environment. (For a discussion of networked emulators, see "Networking in-circuit emulators", p.95.)

According to Dearden, all of his workstation-based customers using Applied's EL3200 emulator ask for an Ethernet interface. More and more designers are asking for Ethernet on the personal computer as well. Dearden adds, "A lot of people have got a distributed file setup, where they have a Sun file-server somewhere but they can't afford to or they don't want to buy everyone a Sun workstation for their desks. So they've got PCs intermixed with Sun workstations and VAXs. With the exception of the PC, I'd say 95 percent plus go with an Ethernet interface."

Cutting download time

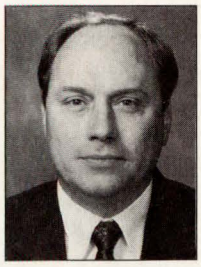
The three most common types of interfaces available on emulators are the RS-232, SCSI and Ethernet. The SCSI interface is useful for those who want to work in a very localized environment. SCSI is also fast. "Operating at disk-drive speeds, SCSI is probably the fastest way to go," says Dearden. "On paper it's faster than Ethernet. And with exactly the same application communicating across RS-232, downloading exactly the same piece of code into the target system, it can take something like 30 times longer over RS-232 than over SCSI."

When debugging a complex 32-bit embedded application, download time is critical. It's fairly common for the code to bomb and completely obliterate itself. So, if you're forced to do a download because you've encountered a problem that requires you to restore the image and restart, the difference between five minutes and 10 seconds is critical.

A designer of LAN systems, who preferred to remain anonymous, agreed that the rate at which an emulator can download code is a big issue. Using an emulator from EPI, downloads took tens of minutes, he says. "At that rate the EPI emulator is acceptable, but not outstanding."

In general, though, the anonymous designer considers EPI's

The integration of emulators with source-level debuggers



Whether an emulator manufacturer writes its own source-level debugger or ports an existing debugger to its emulators, decisions must be made on the depth of integration required between the two. The requirements for debugging software in an embedded system environment are often different from those found in other environments. The system under development is typically very hardware-intensive, and so the developer requires all the typical debugger features plus error-handling capabilities associated with hardware and access to the powerful features of the emulator.

The specific areas that you need to address are:

1. Hardware faults in the embedded system,
2. Software problems that prevent normal operation of the processor—for example, a double-bus fault or processor halt, and
3. Access to emulator features.

Problems with embedded hardware can range from design problems in new systems to improper software that puts the hardware in an invalid state. Two common hardware problems are input signals that are not properly terminated and lack of a processor clock signal. Another common problem is a chip failure that activates a critical input—for example, if the reset, halt or bus grant signals are improperly held active, the processor will not be able to function properly. If the interface software can accept error messages from the emulator, then these conditions are very quickly resolved with a minimum of downtime.

Probably the most common problem is software that generates a hardware fault condition. On a 68000 system, it's very common for the hardware to generate a DTACK signal for only the valid memory in the system. If the software tries to access memory that's not valid—with an invalid pointer, for example—no DTACK will be generated, and the 68000 processor will go into an infinite wait state.

Then there's the all-too-common software that "goes off in the weeds." This can result in accesses to invalid memory or in the processor going into a halt condition. Properly-designed interface software will detect these conditions and let you access the trace buffer to show where the coding errors occurred.

It's very common in embedded system development to require continuous processor emulation. In a multiprocessor environment, the system could crash if one of the processors were to stop executing code; at best, it could require a lengthy resynchronization of the processors. If the processor is controlling a high-speed tape system or an automobile braking system, then stopping the processor could result in physical damage to the system under development. In any system of this type, it becomes important to trace user code while the processor continues emulating. Most emulation systems permit access to the trace buffer under these conditions, but the important consideration is that the trace must be displayed with the high-level language source code and you must set trigger conditions at the same level.

Escaping from the weeds

If the software "goes into the weeds," the processor may continue to execute indefinitely in invalid memory space. Breakpoints are very difficult to use in this case, since a trace history typically shows invalid code executions, not what error actually caused the problem. One solution is to trigger the emulator's trace buffer on a piece of code known to be good and position the trigger point near the beginning of the buffer. This lets you work your way through good code until the bug is discovered. Setting the trigger could require pass counters, sequential triggering, address range definitions, or setting trigger points on lines of source code. These emulator features should be available from the debugger's operating environment, so that you can move easily between source code features and emulator features.

Interrupts, direct memory access operations and critical I/O timing provide similar complexity for embedded system programmers. These hardware-intensive operations require the real-time features of the emulator.

Working together

The key to all this is the level to which the debugger was written or modified to work with an emulator. A debugger written for a personal computer will not typically have the features discussed. Such debuggers may integrate well with compiler output files and display variables, and may set simple address breakpoints and single-steps and offer good solutions for developing code for a PC. When an embedded system is developed using a high-level language, though, all these features, in addition to the ones discussed earlier, are needed. If the debugger is simply ported to the emulator to provide the same capability found on the PC, then the user is missing the tremendous time-saving features built into the emulator.

Source-level debuggers and in-circuit emulators, then, provide very powerful features that, if properly integrated, can give the embedded system developer an effective tool to speed the development of hardware and software.

Charles W. Davis, president of Huntsville Microsystems, Huntsville, AL

debug support very strong. "The one EPI emulator we've used has been really useful, and provides quite a bit of hardware debug support," he says. "It provides all the processor pin signals in the trace. There have been some cases where we've had some hardware problems and we've been able to get clues by looking at the emulator's trace, without attaching a logic analyzer to the system."

The LAN designer also liked the way in which breakpoints are implemented on the EPI emulator. "Some emulators do breakpoints by putting a HALT instruction temporarily at the location. That's not really a good solution. In my embedded system, I'm frequently getting a new copy of code over the network into my device, but the emulator's unaware of this. So, if the emulator used the HALT instruction method, that HALT would get overwritten and the breakpoint would never be seen. The EPI emulator has hardware to

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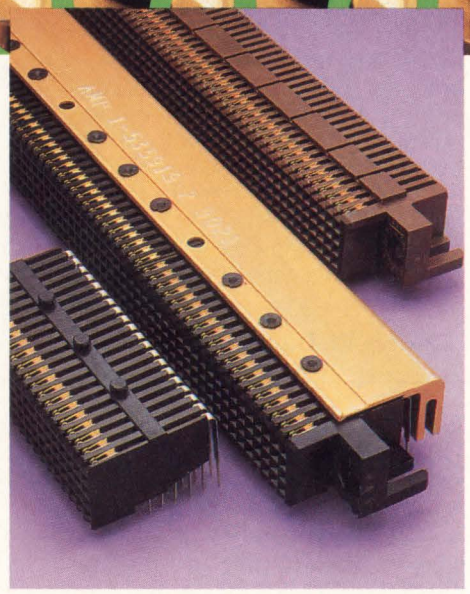

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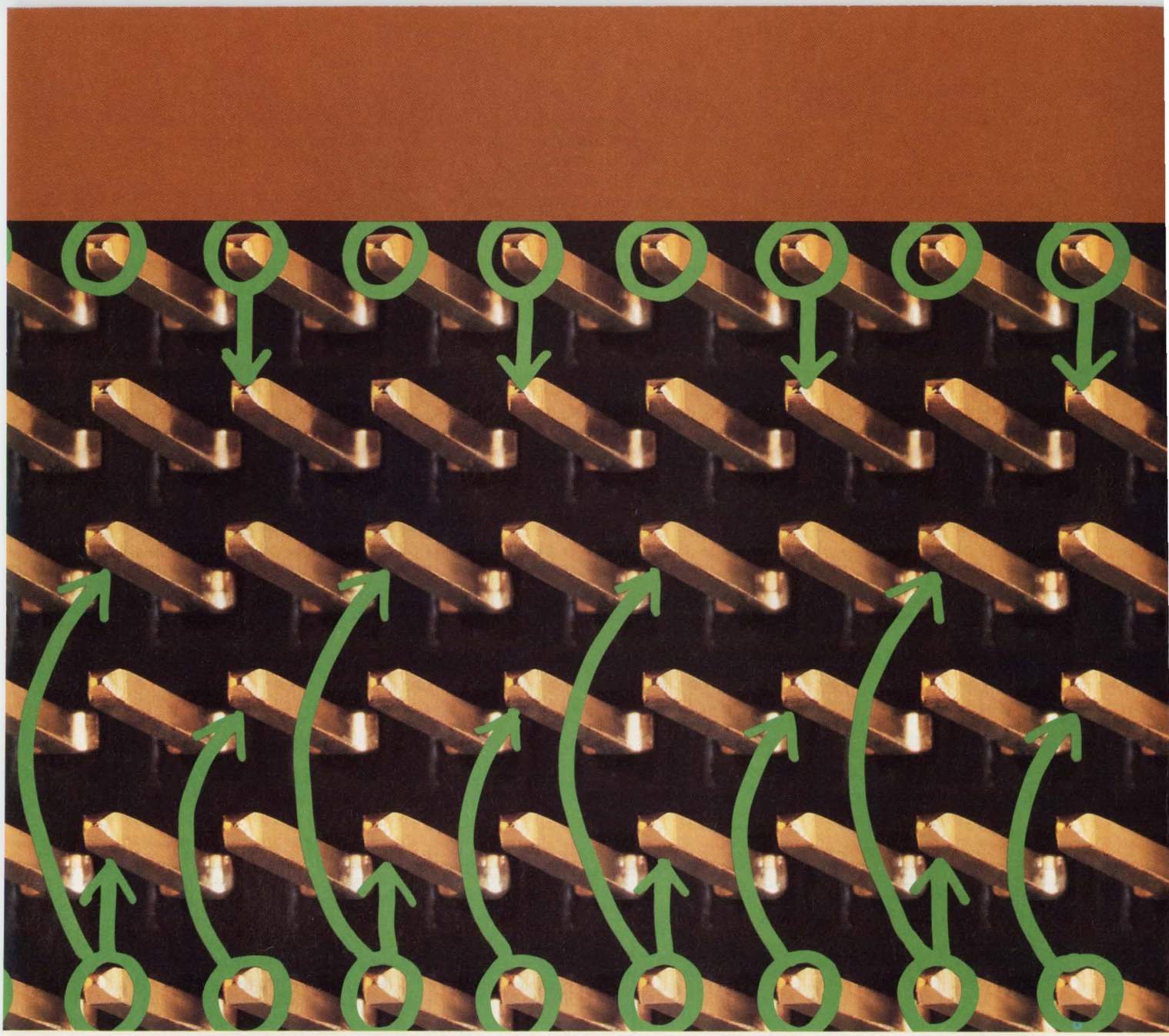

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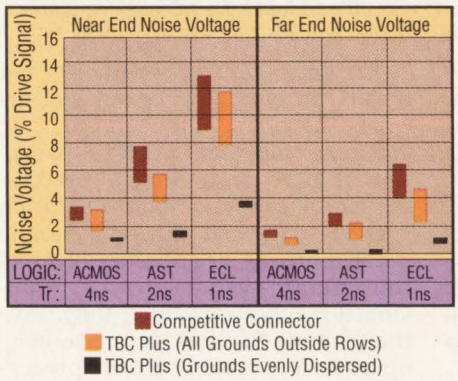


AMP

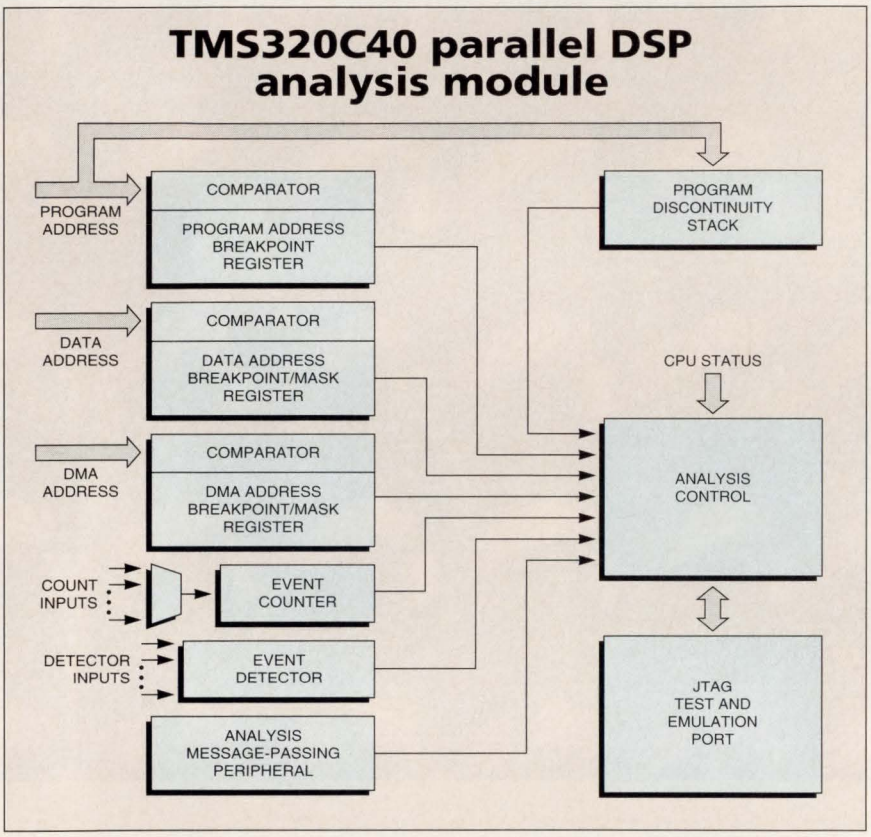
CIRCLE NO. 61

support breakpoints without altering the code."

Simulation option

Once they've finished writing their code, software engineers often want to execute it in a controlled environment prior to physically installing it in the hardware—and that environment is typically a simulator. The problem with the average simulator available for 32-bit processors is that it's constructed to be a logic or an architectural simulator designed to define the characteristics of a particular hardware architecture. While a tool such as this is useful to a hardware engineer who wants to test how a design will perform with a given memory architecture, there is little utility for the software engineer because the simulator executes code much too slowly. Furthermore, it doesn't lend itself to doing source-level debugging in a high-level language.

With this in mind, EPI created an instruction-set simulator that can run over 10,000 instructions/s under simulation. "It's sort of like running under real-time except that it's a simulation," says EPI's Laengrich. "This lets designers functionally debug their code prior to getting into the real world, so that when they do they can be assured that the code is functionally correct." Other errors that crop up can then be assumed to be either timing or integration problems, as opposed to functional errors in the C code.



Because many of their operations are invisible to the outside world, devices such as Texas Instruments' TMS320C40, a 32-bit floating-point DSP, are particularly difficult to emulate. To address this problem, TI includes emulation circuitry on the chip itself in the form of an analysis module. Accessed via the chip's JTAG test interface, this analysis module includes separate breakpoint comparators for program access and program discontinuity, trace stack capability and an event counter. Thanks to the TMS320C40's on-chip emulation support, TI was able to build the XDS 510 emulator, which lets you debug an unlimited number of TMS320C20s running in parallel.

The decision as to whether or not to buy an emulator becomes clear-cut in the realm of multiprocessing; you generally don't. With the exception of a few digital signal processing emulators, no true emulation systems yet exist that can handle several processors at once. None of the emulator vendors are even considering such a product; they have their hands full just trying to keep up with one speedy 32-bit processor at a time. The only option for now is to use several emulators linked together.

Ten processors, ten emulators?

For John Wakerly, vice-president of engineering at Alantec (Fremont, CA), a maker of high-performance, internetworked bridge routers, emulators were out of the question. Alantec's router ties together multiple Ethernets and FDDI (Fiber Distributed Data Interface) rings. The system has 12 Ethernet ports and is controlled with two R3052 processors. The company is currently working on an FDDI board that has two processors. "The designs that we do are multiple-microprocessor distributed systems," says Wakerly. "Not only do I have to plan out the system architecture, but I also have to plan out the budget. I'll be damned if I'm going to buy 10 emulators to fully debug a product that has 10 processors on it. Even if we had the emulators, it would be difficult physically to connect emulators to the processor in our system."

No doubt if Alantec's design had only one processor, Wakerly still wouldn't use an emulator. While he wouldn't quite call himself an opponent of emulation, he believes that simple but solid hardware design, combined with normal software debugging tools that can do breakpointing and single stepping, are all that's really needed.

To debug its own system, Alantec designers used a ROM monitor/debugger from IDT (Santa Clara, CA). The IDT debugger can set breakpoints symbolically and can also look at the contents of registers and stacks. Although it requires a serial port to operate, Alantec has simply used a spare RS-232 on its target system. "Sure, you could use an emulator as a way of tracing your code and finding out what's going on, but I find the old-fashioned techniques of using a symbolic debugger and putting checkpoints in your code works quite well," says Wakerly. "I think the only place for an emulator is where you have a process that really can't be slowed down by debug code, or where using a debugger of any kind would blow away the system you're trying to control—where you're controlling a stepper motor or something."

Wakerly, who also teaches at Stanford University, has been on a crusade to convince his students to design code with debugging in mind. "You have to instrument your code

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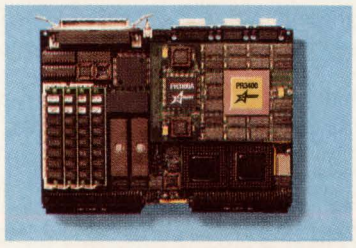

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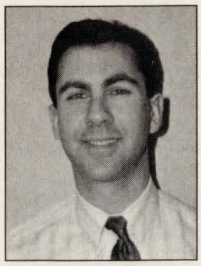
CIRCLE NO. 62

Using ROM monitors for debugging 32-bit applications



Traditionally, embedded system developers have debugged their 32-bit applications using source-level debuggers connected to in-circuit emulators. As the operating speeds of these processors increase, though, so do the cost and complexity of the emulators for them. In the interest of limiting costs while providing a larger number of debugging stations, developers are connecting their source-level debuggers to a combination of in-circuit emulators and ROM monitors to integrate and test their systems. Source-level debuggers which use the same user interface for both ROM monitor and emulator versions facilitate this strategy.

Manufacturing restrictions

There are several manufacturing issues which affect the availability of emulators for newer processors. One of these is the length of the cable which connects an emulator to the microprocessor socket on the target board. Faster processors require that this cable be very short if the emulator is to provide full-speed emulation of the target chip. A ROM monitor, by contrast, is software-installed in EPROMs on the target board. It can easily run a user's application at full speed because it uses the target microprocessor directly.

Another physical problem for emulators is with surface-mounted processors which might not be compatible with an emulator's probe tip. A ROM monitor is not concerned with the physical pinout of the processor; all it requires besides a RAM work area is a serial interface to a terminal or a source-level debugger.

Because they are not subject to some of these physical constraints, ROM monitors are frequently available before emulators for newer processors, particularly in the 32-bit world. Because monitors are supplied as software, their manufacturing cost is low. In fact, the cost of a ROM monitor can be 1/10 to 1/20 that of an emulator. Another advantage of having a debugger in software form is that a developer can leave the ROM monitor code on the board in the final shipped application and can then debug the product in the field.

Sharing the CPU is limiting

Compared with an in-circuit emulator, a ROM monitor's biggest limitation is that it must share a single CPU with the user's application program. Unlike an emulator, a ROM monitor doesn't have an auxiliary processor transparently observing bus activity. An emulator uses this auxiliary processor to accumulate instruction traces and to implement breakpoints on data locations without stopping the target processor.

Some ROM monitors support instruction tracing and data breakpoint simulation by accessing the traced execution mode supported by many processors. In the tracing mode of execution—activated by setting a bit in the status or flags register—the processor executes a single instruction and then control passes automatically to a trace exception handler. The trace exception handler can store into RAM the current program counter address after each instruction to accumulate a trace buffer.

ROM monitors are frequently available before emulators for newer processors.

Because it's not efficient to execute the entire application in this trace mode, ROM monitors let you enable and disable tracing at different code breakpoints. This lets the application run in real-time for a greater percentage of the program. It also makes the most efficient use of the monitor's limited RAM trace buffer by ignoring routines you know work correctly.

The trace exception handler can also compare the contents of a particular memory location with a specified value, effectively simulating some kinds of data breakpoints. Because this method doesn't rely on external data bus activity, it can be used to break on changes to a register value—a feature not supported by emulators.

A third use of the trace exception is to implement ROM code breakpoints. Traditionally, ROM monitors implement RAM code breakpoints by substituting the instruction's opcode with a TRAP instruction. This approach won't work when the instruction is in read-only memory. To implement ROM code breakpoints, the ROM monitor checks after every instruction to see whether the next instruction's address is in a list of ROM code breakpoints. This list of breakpoints is maintained in RAM.

Compensating capabilities

Although some ROM monitor functions temporarily suspend real-time execution, they can compensate for this shortcoming by offering some capabilities not normally available with emulators. Tracking changes made to registers is one example of such a capability. Another is the capability to provide more detailed instruction traces. Instruction tracing sacrifices real-time execution, but some monitors use the trace exception handler mechanism to save even more information than just program counter addresses. By doing this, they can produce an instruction trace which also shows the effect of each instruction on memory.

Unlike emulators, ROM monitors don't contain overlay RAM to be used in place of target memory. This overlay memory can be useful in debugging applications before target hardware is stable. In these cases, developers can use a ROM monitor in conjunction with a development board system, such as a Motorola EVS board. These boards offer RAM which can hold a downloaded application. Later in the development cycle, when you begin to use the actual product board instead of the development board, you can reconfigure the ROM monitor to work on the new board.

ROM monitors and emulators offer somewhat different capabilities at significantly different price levels. Emulators are most valuable for their ability to debug programs in the absence of any target hardware, or to detect certain kinds of real-time performance bugs. ROM monitors can be used for the rest of a project's algorithmic debugging, even after it has been shipped. Using a source-level debugger which has the same user interface for both target environments greatly simplifies the transition in using these two debugging tools. The end result is that a development team can make the most efficient use of its time and budget.

Andy Lantz, senior marketing engineer, Intermetrics Microsystems Software, Cambridge, MA

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for debugging to begin with," he says. "That's better than sticking on a contraption afterwards as kind of an afterthought. Certainly as we go to more multiprocessor systems, emulation becomes more and more impractical. Even if you had 10 emulators for 10 processors, you would still have the problem that interactions between multiple processes and multiple processors are very complex. And the debug hooks have to be thought out and hooked in from the beginning. There's just no way to capture the sequence of events as it occurs on multiple processors."

Designing in emulation hooks

While Wakerly's skepticism about emulating multiple processor systems may be well founded, emulating parallel processing is a reality today. Devices such as the TMS320C40 from Texas Instruments (Dallas, TX), a 32-bit floating-point DSP, is particularly difficult to emulate because there's so much inside it that's essentially invisible to the outside world. On the TMS320C40, you can do two data memory accesses every clock cycle, have program access, perform a multiply-add, and read COM ports—all without anything happening on the external pins, other than power and clock activity.

Faced with this problem, TI had no hope of providing any debug capability for the TMS320C40, unless the company put hooks for emulation on the chip itself. These hooks include a JTAG interface and an on-chip analysis module. "It's like a scope into the chip, if you will, where the JTAG gives us a very good, accepted, industry-standard method of talking to the chip," says Ray Simar, a senior member of the technical staff at TI. "And, once inside the chip, we have an analysis module that monitors internal hardware breakpoints and the program stack, does a traceback and counts events."

The TMS320C40 has another problem that isn't an issue with most other microprocessors. Since the chip was designed for parallel systems, TI needed to provide a debugging strategy that was scalable for any number of processors. The JTAG port came to the rescue again. "You can have any number of JTAG devices in a system. They can be hooked up over a JTAG, and we took advantage of that," says Simar. "So, designers can get the double benefit of JTAG for both emulation and test. But, JTAG is really just a window into the device. It's the analysis module that makes emulation possible." By putting embedded emulation circuitry on the device itself, TI was able to successfully build a parallel processing emulator/debugger system.

Build or buy?

With the price of emulators on the rise, it's tempting to assign one of your engineers to build your own, especially if the engineer has a fairly deep knowledge of the processor in question. But building emulators for 32-bit processors can be a million-dollar effort. Still, what if there's no emulator available for the processor you're using, and you can't design without one?

Even in this situation, Applied's Jensen approaches the problem with caution. "The problem with building your own is that you're throwing yourself in the critical path, because now you're building a tool that everyone else is depending on. You have to maintain it. If that engineer worked a whole year on the emulator, it cost you $100,000 fully absorbed—lights, power, capital equipment, everything else—to keep him employed for that year. At 10 times what that engineer is paid and what he absorbs, your company probably runs at about breakeven. Therefore, it cost your company a million dollars to spend that $100,000, because that engineer had no leverage. The only leverage he had was cost-avoidance for capital equipment." ■

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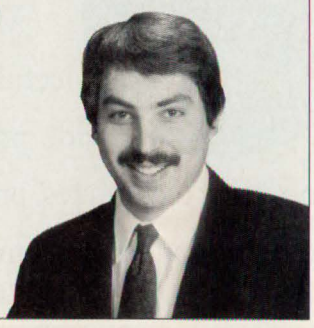
Postscript

Unless your design team is blessed with an unlimited budget, it behooves you to select your debug and development tools wisely. If your 32-bit microprocessor-based embedded system design isn't prone to complex time-domain problems, then consider a low-cost solution such as a Codetap or a ROM monitor/debugger. If your 32-bit system runs in real-time and has a large software component, however, invest in emulators—at least for your key system integration engineers. A good emulator should offer not only hardware breakpoints and extensive trace buffering, but should emulate the processor exactly.

At $25,000 and up, who can afford to put an emulator on every engineer's desk? If your team is particularly large, you might consider networking your emulators and workstations over Ethernet. This will not only help coordinate the intricate software/hardware integration process, but also avoids time wasted downloading code over serial cables. What's more, most of your software developers can stay in the comfortable (and productive) world of Unix workstations, where they can use inexpensive tools like instruction-set simulators or target-resident kernels.

Avoid vendors that only sell the emulator and not the support that goes with it. I've heard from users both accolades for tool vendors that provide thorough support and horror stories about designers who bought expensive emulators and were then left to fend for themselves. If an emulator vendor doesn't offer effective support, perhaps the vendor doesn't know enough about embedded systems to develop a decent emulator in the first place.

Jeffrey L. Child



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The program also features a panel discussion on Japanese and European VHDL activities. Representatives from recent European and Japanese VHDL conferences will present highlights of outstanding papers presented at each conference as well as report on their efforts in the support of VHDL.

The Tutorials

Four tutorials are offered and feature topics for both advanced and novice VHDL users. A full day introductory course of VHDL is tailored to teach the various aspects of the VHDL language to a beginner, with emphasis on the usage of the language and the various styles of descriptions. Three other half-day tutorials feature advanced topics on the impact of the 1992 revalidization effort, the proper use of register and bus signals, and selecting the proper synthesis tools for higher level design quality and productivity.

The Supplier Suites

New to the Spring Conference is the addition of supplier hospitality/demonstration suites. These informal suites offer attendees the opportunity of gaining hands-on experience with state of the art products from leading vendors. The suites are offered in conjunction with the program, and time has been allotted to allow attendees to visit suites without missing any of the technical program.

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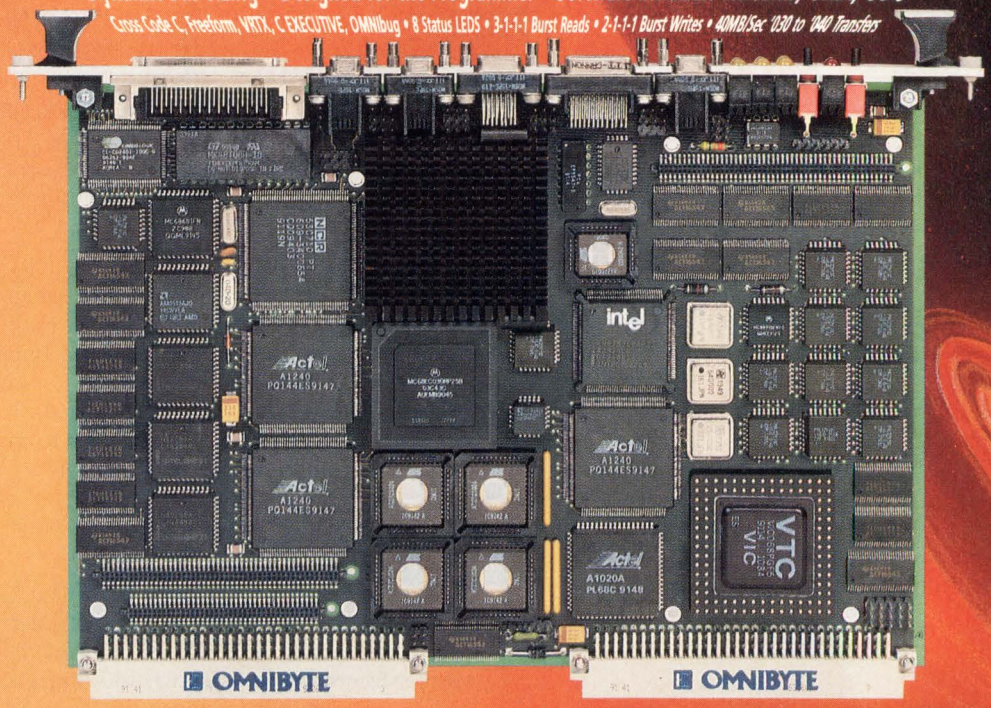

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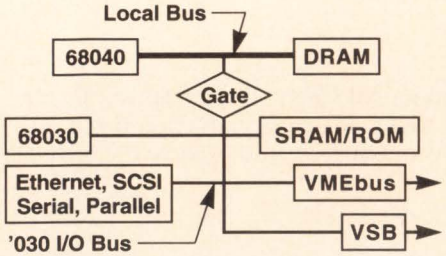

Taurus Dual Bus Architecture

The Taurus is a dual-processor and dual-bus single slot 6U VME board. Its dual-bus architecture allows the 68040 to execute code uninterrupted while the '030 processes all on-board I/O. This optimizes the 68040's performance. Writing code for the Taurus is very straightforward. The '030 can act as an I/O processor, communicating with the 68040 using control blocks. The '030 can also be used as a DMA controller with direct control of all on-board devices by the 68040. The '030 uses the 512KB of SRAM and the 128KB of code provided by Omnibyte in EPROM.

Extensive use is made of intelligent, on-chip DMA devices for Ethernet, SCSI and serial I/O minimizing processor intervention. DRAM is contained on up to 2 stackable modules allowing upgradable options from 4-256MB.

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Standard I/O	2 RS232D: 68681 DUART, 32 Lines Parallel I/O, or 16 w/ Centronics Printer Port
Memory	4MB to 256MB† DRAM, 512KB SRAM, 8KB NVRAM, 1MB FPROM, 4MB EPROM
Other	VSB†, VME64†, Watchdog, Calendar Clock, Mailbox, (6) 16-bit Timers, Snooping, Advanced Omnimodule Socket
Software	VxWorks[1], OS-9[2], UNIX[3] VRTX[4], CrossCodeC, FreeForm[5] C EXECUTIVE[6], OMNIbug

† Denotes optional features.

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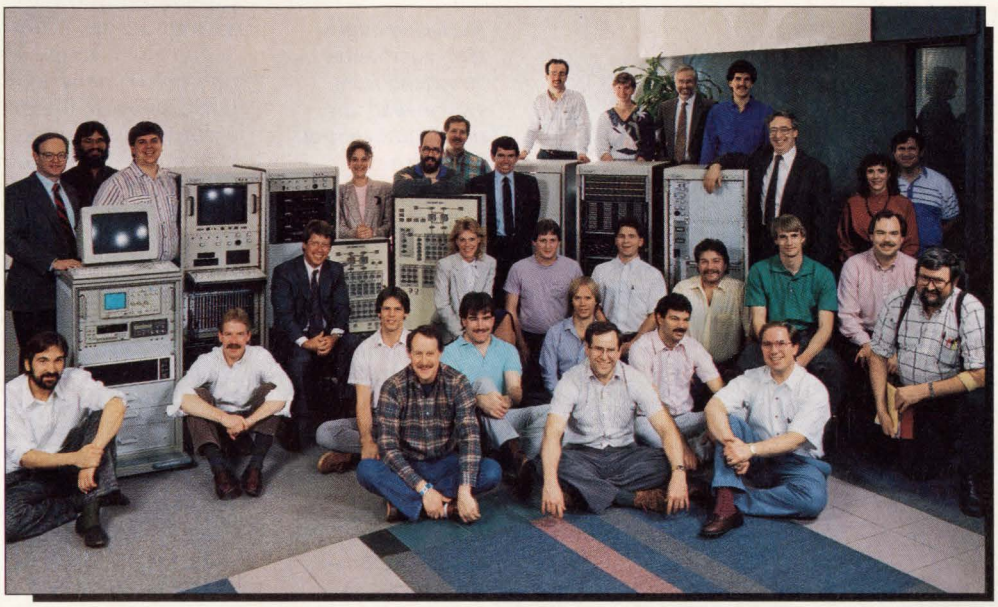
CIRCLE NO. 65

Divide and conquer strategy for New York's traffic control system



Bob Rausch, JHK associate vice-president and project leader for New York City's new Vehicular Traffic Control System (standing next to far right cabinet), with several of Heurikon's design and support personnel.

Depending on how you look at it, the task of modernizing New York City's traffic light control system could be called system integrator heaven—or hell. The design team at JHK & Associates (Norcross, GA) faced the massive challenge of building a system to manage traffic lights at up to 12,000 intersections throughout Manhattan and the remainder of the city. Now in its initial stage of installation, this phase of New York's Vehicular Traffic Control System (VTCS) implementation is a major step in a $50 million project to computerize the city's traffic signals. The system's design and development has taken three years to complete.

According to Bob Rausch, VTCS project leader and associate vice-president of JHK, the work required extensive use of standard, off-the-shelf VME-based CPU boards, custom VME I/O cards and a gargantuan number of peripheral devices, including power supplies, disk drives and modems. At the heart of the system are 18 area computers, each containing 10 to 12 68030-based VME boards. Each board in the system runs a real-time operating system—except for one in each area computer that runs Unix.

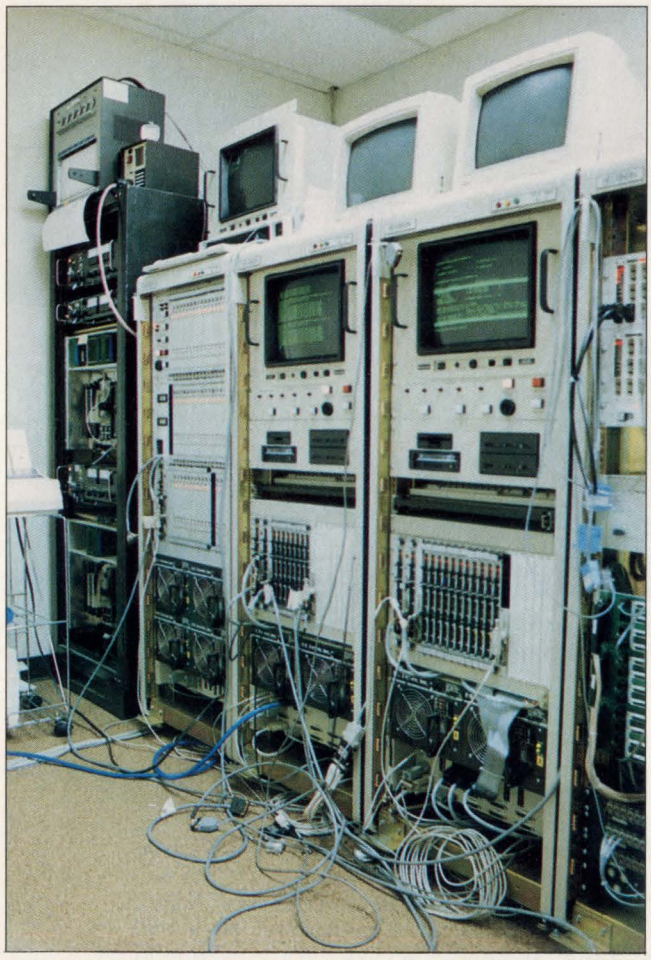
Out with the old, in with the new

New York's current traffic control system is based on 10 IBM 1800 computers connected to an IBM 4341 mainframe. A workhorse process-control machine of the late 1960s, the IBM 1800 was built before the widespread use of microprocessors and high-density ICs. The system, installed in the early 1970s, currently manages lights at 3,250 intersections. The broad goals of the new design include replacing this outdated equipment (which is

Jeffrey Child, Associate Editor

too expensive to maintain with current technology), connecting Manhattan into the system to improve traffic flow and decrease pollutants and allowing for future expansion.

Armed with a wealth of experience designing traffic control systems, Rausch and his team had a good grasp of the elements needed to make the design a success. Fundamentally these elements included relying on an open bus architecture, using an integrated real-time operating system and following a "divide and conquer" strategy to allocate design resources for the project.



Replacing huge IBM mainframes stretching from wall to wall, the new traffic control system uses several racks with multiple VME boards and redundant power supplies. The cabinets shown here include an area computer on the right and a digital I/O subsystem (DIOS) on the left. Each area computer contains up to 12 68030-based V30XE CPU boards from Heurikon. Each DIOS contains 48 custom digital I/O cards, three controller boards and one V30XE CPU. The VTCS consists of a total of 11 DIOSs and 18 area computers.

Pushing VME to the limit

According to Rausch, VME was chosen as the bus architecture for the project because it was the only established open-system bus. Even though JHK considered VME the only reasonable choice, its selection was still something of a gamble, since the sheer scale of the project would test the limits of VME.

"I believe we are among the first actually adopting a massively parallel master processor configuration in VME," says Rausch. At the time JHK began the project, others had put in one or perhaps two CPU cards in a system, along with several I/O and support boards, but JHK was putting 10, 12 and 14 processor boards in and expecting them to run independently and be able to take over the bus.

Other reasons for adopting VME were its reliability and the desire to get away from proprietary custom systems. "VME is reliable enough that we could assure a minimized mean-time-to-repair," says Rausch. "The current New York system is in a situation where it's extremely difficult and costly to repair."

The design team also needed to use Ethernet and have access to good development tools. Initially, the project looked relatively open-ended. But it had to be designed to be around for decades, so JHK couldn't afford to base the design on products that didn't yet exist. "We knew that Futurebus and VME64 were coming, but I had to cast my decision in 1989," Rausch comments.

System longevity important

Although Multibus II was an option, it didn't appear to be the best investment for the future. "In 1989 we saw the lifespan of Multibus II declining, while VME was on the rise," says Rausch. VME was a growing architecture, and the number of vendors supporting it and the power of their products were ever increasing. Comments Rausch, "Remember, we were interested in having a lot of vendors so I could get a low bid. It gave me a choice. I knew there were more powerful boards coming down—RISC boards, for instance. I wanted a configuration that I hoped would provide expandability and flexibility. VME gave me an open architecture and a choice of vendors, and I knew I could add boards as traffic control becomes more sophisticated. So, if I chose VME and I didn't fill the rack, then I knew that we could add in newer technologies later. Now I'm looking at adding in some fuzzy logic boards and high-end RISC machines." The new VTCS platform is intended to be the first step in developing New York City's Intelligent Vehicular Highway System (IVHS).

Because JHK isn't a hardware manufacturer, but rather is a traffic control system-integration and application-software development company, it needed to enlist a hardware company to handle the design and procurement of all the VTCS hardware. Having chosen VME as the bus architecture for the design, it made sense to choose a VME board vendor to accomplish this—and preferably a VME board vendor that could build both custom and standard boards, as well as select and procure the necessary support hardware, such as power supplies, disk drives and modems.

JHK's Rausch spent months writing a detailed specification of the type of hardware required. He decided the vendor would also have to provide the development software to go with the hardware. "I was not going to be the integrator for the development tools, and then use the tools to develop my own application," says Rausch. "We told the vendor, 'You know your hardware, we don't. So you provide us with an installed operating and development environment and we'll use it.'"

In 1989, JHK put out a specification describing the computer equipment it needed. According to Rausch, "I went to Buscon in October, 1989, and I wandered around the floor and gave out our New York City design spec. We asked vendors, 'Tell us what we don't know. Tell me where the system may be flawed. Tell us what products of yours will beat the competition.' Several VME board vendors responded to the request for proposals."

The choice was ultimately narrowed down to two bidders. Heurikon (Madison, WI) submitted the low bid and won the contract. The City of New York was Heurikon's customer, but the contract management and all of the technical decisions were reviewed by JHK. Heurikon had to prove, through a formal testing procedure, that the system worked to specification before Rausch would install it.

Setting out the rules

The specification laid out general guidelines for the processors, establishing their basic capabilities. Heurikon then had to decide which processor board to use to meet the specifications, how to configure the rack and how to get everything into the rack so that it would fit into a restricted space. According to Jeffrey Mattox, senior engineer at Heurikon and VTCS project manager, "We had to go to the vendors of the power supplies, CRT monitors and disk drives, and deal with all the issues of procuring and building all the components that go inside the racks."

One rack contains the digital I/O subsystem (DIOS), another holds the area computer. The existing equipment in New York City consists of the same functional components, DIOSs and area computers, but they're old IBM equipment and much bigger than Heurikon's. "We're replacing equipment that was five to seven times the volume of what we're installing," says Rausch. "For every pair of racks we put in, we remove seven or eight that were roughly the same size."

There are three different versions of the area computer—one of them connects to a DIOS, one links to a modem to talk to Manhattan and one connects to a lower-speed modem to communicate with outlying areas. Heurikon's end of the project has consisted of building the racks; specifying, procuring and installing all the boards and equipment in them; wiring it all together; and testing it. Heurikon also provides the system software, Unix and VxWorks from Wind River Systems (Alameda, CA), and wrote test software to meet the specifications for testing. Beyond that, the application code—the actual traffic control code—is being done by JHK.

OS choice critical

JHK evaluated VxWorks, OS-9, Vertex, and pSOS for possible use on the project. VxWorks wasn't perfect, but it was established and stable, and the development tools were very good. It was network-oriented and could run on Sun workstations. VxWorks supports a TCP/IP (Transmission Control Protocol/Internet Protocol) backplane driver. That gives the platform flexibility, so several people can be developing on it.

A drawback was VxWorks' price. Because of the cost sensitivity of the New York project, the $22,000 licensing fee for two Sun workstations was not taken lightly, but the price was worth it, according to Rausch.

The comprehensiveness of VxWorks was what convinced Rausch to use it as the real-time operating system for the project. He says, "VxWorks is robust. Not the best in terms of speed. The TCP/IP backplane isn't very fast. But it was there, it was foolproof and it works. That means my staff can concentrate on the application and structures, rather than debugging the environment."

Rausch uses the same argument against debugging with emulators. "In some cases, I've spent more time getting emulators to work than it took to fix the problems."

Divide and conquer

Because of the scale of the New York project, JHK employed a "divide and conquer" strategy in its design. Every functional element of the system was assigned specific responsibilities. This helped keep the project's complexity under control.

The typical area computer uses 10 processor boards, with their duties divided strictly according to function. These include one Unix database and peripheral manager, one real-time network manager, one traffic coordination processor, six second-by-second traffic signal control processors, and a communications processor. Some area computers have four communications processors.

Each area computer is designed to control 576 intersections within a geographic area. The area computers communicate with each other, providing real-time information on traffic at each intersection. In many cases, roads cross areas governed by different computers, so the computers have to communicate with each other to keep things coordinated.

A separate processor board is required to feed each intersection its "plan." A plan is a list of the time intervals between red, yellow and green lights. The geometry of each intersection determines how long the light stays in each phase.

In keeping with the divide and conquer strategy, an extra 68030 board was added to each area computer. Called a traffic coordination processor, its job is to look at time-of-day plan selections and traffic response plan selection control algorithms.

Coordinating drive-time

In real time, traffic lights change plans about once per minute, so the traffic coordination processor only has to send out a new plan that often, at the most. The traffic coordination board's sole job is to select the best plan for every traffic light. "Its job is to analyze the traffic control data as it comes in, consider the time-of-day scheduling criteria and arbitrate all these things to determine what the intersection should be doing," Rausch explains.

Once the real-time traffic control system was completed, it was time to consider the operator interface. That called for the ability to communicate with people in the outside world—in real time. According to Rausch, "In Manhattan there's a map on the wall that needs to change its indicators in real time.

There are also graphic workstations with maps that need to show real-time conditions. And there are 17 other area computers, and sometimes what one is doing is dependent on what another's doing."

Parameters have to be shared as real-time events. With this in mind the design includes a real-time 68030-based LAN processor in each computer. Like the other boards, the LAN has VxWorks running in real time. The LAN processor's sole job is to manage the real-time distribution of data—both as a supplier and a receiver. Again, divide and conquer. ■

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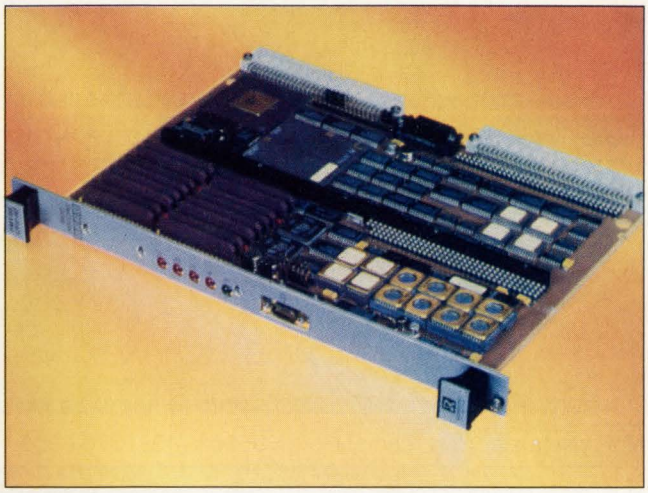
COMPUTERS & SUBSYSTEMS

VME CPU boards break barriers to reach compatibility

Jeffrey Child, Associate Editor



Many basic compatibility problems in VME have been alleviated through widespread use of standard VME interface chips, such as the VIC. Even military CPU boards such as the CPU-40 from Radstone Technology use the VIC to provide all their slot "1" interface features.

While compatibility problems are nothing new in the VME world, it's clear that there's been progress. Standard interface chips on VME CPU boards now let cards from one vendor talk to other VME CPU or peripheral cards in the backplane. In fact, many in the VME community claim that compatibility is no longer an issue. Still, system integrators know from experience that CPU board compatibility means more than meeting the VME electrical specification.

For system integrators at AP Labs (San Diego, CA), VME CPU board compatibility remains a problem. "VME is as close to compatibility across open systems as I've seen yet, but it's got miles to go," says Jack Davis, AP Labs product marketing manager. "We've run into a lot of problems with different implementations of VME interfaces. A lot of the features in VME are optional features. Sometimes you make assumptions about supported functions and features, and boards don't necessarily support them or support them in the way you'd expect them to. We have to watch that very closely."

To determine a VME CPU board's level of system compatibility, you need to ask some basic questions: How is the VME interface implemented? How does it access off-board memory and share its on-board memory with other boards in the backplane? What are the system controller's capabilities? The amount of I/O capability on the CPU board may also be an issue.

Although VME is a standard, its implementation is fairly open. Fortunately, many CPU board vendors have begun moving away from custom PAL-based implementations in favor of integrated ASICs that include the complete VME specification. These include the VMEbus Interface Controller (VIC), developed by the consortium of VMEbus vendors; the FGA002 gate array from Force Computers (Campbell, CA); and the MVME6000 gate array from Motorola (Tempe, AZ).

VIC and friends

Among these, the most widely used on today's VME CPU boards is the VIC. Because several vendors are implementing VME with an identical chip, compatibility has become somewhat less of an issue. "Using several boards that each have the VIC chip helps compatibility," says Clarence Peckham, vice-president of engineering at Heurikon (Madison, WI). "And using ASICs in general makes life easier, whether it's from Motorola or Force Computers, because they all seem to adhere to the VME spec closely. In a lot of the earlier, PAL-based designs, I think the board makers took a few liberties here and there with the VME specification."

Providing a VME-compatible interface means more than simply meeting the electrical specification. When Force designed its interface chip, the FGA002, the company decided to tackle logical compatibility as well. "We designed the chip to be VMEbus-compliant, and then included different types of tuning hooks in it," says Tom Griffiths, product marketing manager for Force.

These help the board deal with situations that were not covered by the original VME specification, but could create incompatibilities. The FGA002 can, for example, release the bus early or late and control the timing for read-modify-write (R-M-W) commands. This flexibility is particularly important for older processors such as the 68020. "There's a conflict in the way the 68020 and the VMEbus deal with a read-modify-write," says Griffiths. "Customers with a 68020-based board could run into a situation where one board in the system hangs up when a read-modify-write is issued across the VMEbus." By permitting timing control in such situations, the FGA002 lets a 68020 respond in a more graceful fashion.

Force's IBC-20 sports the FGA002, a 25-MHz 68020 processor and four Mbytes of SRAM. The board features two FLXi mezzanine bus slots to permit installation of two self-contained Eagle I/O subsystem modules. Because the 32-bit FLXi bus supports master as well as slave operations, both intelligent and non-intelligent I/O subsystems may reside on the Eagle modules. Also provided on the board are an independent 32-bit DMA controller, two message broadcast channels, a serial port, and eight multiprocessing mailboxes.

More memory to share

As memory gets denser and cheaper, VME board makers are putting more of it on the CPU board itself. It won't be long before 64 Mbytes of DRAM on a board will be commonplace. But

PRODUCT FOCUS/VME CPU boards

Model	CPU(s)	CPU clock speed (MHz)	Math coprocessor	Memory (Mbytes)	Memory speed (ns)	DMA channels (no. and width)	I/O ports (no. and type)	On-board interboard expansion	Price
Aeon Systems 8401 Washington Pl NE, Albuquerque, NM 87113 (505) 828-9120									**Circle 301**
VME300	rtVAX300	20	Yes	2-8	100	—	1 Ethernet, 2 RS-232	—	$4,995, $5,995, $6,995
VME300-E	rtVAX300	20	Yes	4-16	100	—	1 Ethernet, 2 RS-232, 1 SCSI	—	$6,495, $7,995
VME3000	R3000	25	Yes	4-16	80	1 32-bit	1 Ethernet, 2 RS-232	Custom mezzanine	—
Force Computers 3165 Winchester Blvd, Campbell, CA 95008 (408) 370-6300									**Circle 302**
CPU-30	68030	25	68882	4-16	100	1 32-bit, 1 8-bit	4 RS-232, RS-422, 1 parallel, SCSI, floppy, Ethernet	—	$3,490
CPU-40	68040	25, 33	Included	4-64	100	1 32-bit, 1 8-bit	4 RS-232, RS-422, 1 parallel, SCSI, Ethernet or VSB Ethernet	1 FLXi	$3,490 - $4,490
IBC-20	68020	25	None	1-4	100	1 32-bit, 1 8-bit	1 RS-232, 1 parallel, 2 expansion, I/O	2 FLXi	$1,690 - $2,490
Sparc CPU-1E	Sparc	20	Weitek 3170	4-16	100	None	SCSI, Ethernet, keyboard, mouse, serial I/O	SBus	$4,990
Sparc CPU-2E	Sparc	40	Cypress 7CY602	16-32	100	1 64-bit	SCSI, Ethernet, keyboard, mouse, serial I/O, audio, floppy	SBus	$9,990
Heurikon 8000 Excelsior Dr, Madison, WI 53717 (608) 831-0900									**Circle 303**
HK68/3BF	68030	33-50	68881/68882	2 or 8	70	On Corebus	2 RS-232, SCSI, Ethernet (w/DMA)	Corebus, VSB	$3,495
HK68/U3D	68030	33	—	2-16	70	—	2 RS-232	None	$1,795
HK68/V4F	68040	25-50	In CPU	2 or 8	70	On Corebus	2 RS-232C	Corebus, VSB	$4,795
HK68/Y30XE	68030	20-33	68881/68882	2 or 8	70	Four channel, 32204, 32-bit	2 RS-232	—	$4,395
HK80/V960E	i960CA	25-40	None	2 or 8	70	4 32-bit	4 RS-232, Ethernet	None	$3,995
Matrix 1203 New Hope Rd, Raleigh, NC 27610 (919) 231-8000									**Circle 304**
MC-CPU165	68040	25	Yes	4-16	80	None	2 EIA-232	VSB	$3,495
MC-CPU167	68040	25	Yes	4-32	80	3 32-bit	4 EIA-232, SCSI, Ethernet	—	$3,995
MD-CPU330	68030	25	Yes	1-8	80	None	2 EIA-232	Dbus-68	$2,295
MD-CPUE100	68HL000	12.5	No	1-4	80	None	4 EIA-232, Ethernet	—	$1,445
MS-CPU220	68020	16	Yes	1-4	80	None	2 EIA-232	Dbus-68	$1,695
Mizar 1419 Dunn Dr, Carrollton, TX 75006 (214) 446-2664									**Circle 305**
MZ 7130	68030/EC030	25	68882 optional	4-16	—	—	2 serial, 1 SCSI	Mezzanine bus, VSB, SCSI, Ethernet, serial/parallel	$3,895

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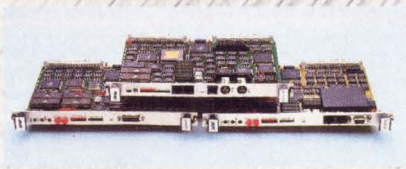

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Mizar 1419 Dunn Dr, Carrollton, TX 75006 (214) 446-2664									**Circle 305**
MZ 7140	68040	25	Internal to 040	4-32	—	—	1 Ethernet, 1 SCSI, 1 parallel, 2 serial	—	$3,495
MZ 8120	68020	16.7-25	—	1	—	—	2 serial	MXbus	$1,695
MZ 8135	68030/EC030	25, 40	68882 optional	1-4	—	—	2 serial	MXbus	—
MZ 8140	68040	25, 33	Internal to 040	1-4	—	—	2 serial	MXbus	—
Motorola Technical Systems Division 2900 S Diablo Way, Tempe, AZ 85282 (800) 234-4863									**Circle 306**
MVME143S	68030	16 - 25	68882	4	80	—	3 EIA-232	—	$1,995
MVME147S	68030	16 - 32	68882	4 - 32	60	1 8-bit	4 EIA-232, 1 SCSI, 1 Ethernet, 1 parallel	—	$3,495
MVME165	68040	25/33	—	4 - 16	60	—	3 EIA-232	VSB	$3,495
MVME167	68040	25	—	4 - 64	60	4 32-bit	4 EIA-232, 1 SCSI, 1 Ethernet, 1 parallel	Custom memory	$3,995
MVME187	88100	25	—	4 - 64	60	4 32-bit	4 EIA-232, 1 SCSI, 1 Ethernet, 1 parallel	Custom memory	$3,995
Performance Technologies 315 Science Pkwy, Rochester, NY 14620 (716) 256-0200									**Circle 307**
PT-VME118	68020	16.7, 25	68882	1-8	80	1 32-bit	21 serial, 1 parallel, 2 Ethernet	32-bit EPAK	$1,036
PT-VME130	68030/EC030	16.7, 25	68882	1-4	80	1 32-bit EPAK-based DMA	21 Serial, 1 parallel, Ethernet	VSB, 32-bit EPAK	$1,236
PT-VME131	68030/EC030	25	—	1-8	80	2 32-bit	22 serial, 1 parallel, 2 Ethernet, 1 SCSI	32-bit EPAK	$1,436
PT-VME141	68030/EC030	25	—	1-8	80	2 32-bit	22 serial, 1 parallel, 2 Ethernet, 1 SCSI	32-bit EPAK	$1,836
PT-VME151	68040/EC040	25	in CPU	1-8	80	2 32-bit	22 serial, 1 parallel, 2 Ethernet, 1 SCSI	32-bit EPAK	$2,316
RadiSys 19545 NW Von Neumann Dr, Beaverton, OR 97006 (800) 950-0044									**Circle 308**
EPC-3	80386SX	16	i387SX	1-4	—	2 16-bit, 4 8-bit	2 serial, 1 parallel, VGA graphics, keyboard	1 EXMbus slot	$2,980
EPC-4	80386	25	i387	4-16	—	2 16-bit, 4 8-bit	2 serial, 1 parallel	2 EXMbus slots	$3,995
EPC-5	80486	25 or 33	In CPU	4- 16	—	2 16-bit, 4 8-bit	2 serial, 1 parallel	2 EXMbus slots	$5,995
EPC-6	80386SX	20	i387SX	1- 4	—	2 16-bit, 4 8-bit	2 serial, 7 segment display	1 EXMbus slot	$1,995
Radstone Technology 20 Craig Rd, Montvale, NJ 07645 (201) 391-2899									**Circle 309**
CPU-3A	68030	25	68882	4	55	2 32-bit	2 RS-423	VSB	$7,300
CPU-20	68020	20	68882	5	70	2 32-bit	2 RS-232	—	$6,530
CPU-40	68040	25	In CPU	10	40	2 32-bit	2 RS-423	MXbus mezzanine expansion bus	$12,500
68-33	68030	50	68882	5	20	2 32-bit	2 RS-232/422	VSB and APEX	$3,220
68-41	68040/020	40/20	In CPU	36	80	5 32-bit	4 RS-232/422/485	VSB and APEX	$4,995

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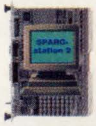

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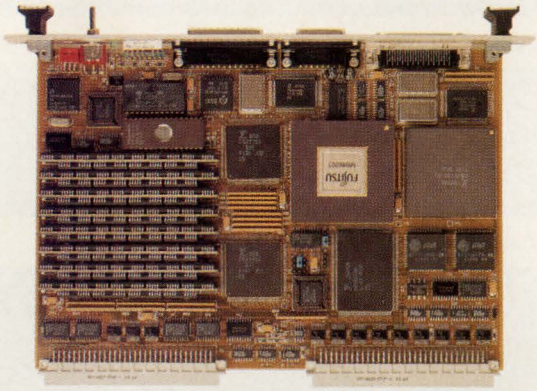

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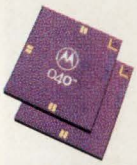
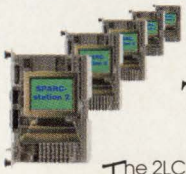


2 040 x 2 =28.5

With 28.5 Mips of integer performance, the 40 MHz SPARC MPU is more than twice as fast as the 68040. A larger 64KB cache and combined MPU/FPU put the SPARCcard 2LC in a class of its own.

64/32 64-Bit Architecture

The SPARCard is the only SPARC VME SBC built on the MBus, Sun's sophisticated 64-bit local bus. Used in the SPARCserver 600 MP Series, the MBus offers 64-bit paths to internal devices and memory for *fast* system throughput. Advanced ASICs designed specifically for the MBus guarantee performance and reliability.



The Future

The 2LC is just the beginning. Themis is producing an entire family of SPARC 2-based products for every embedded application, including those requiring SBus modules. For more information contact Themis Computer, the sole source for VME SPARCstation 2 performance.

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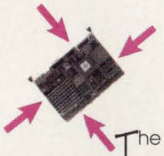
We're partnered with SunSoft, a division of Sun Microsystems and developer of Solaris, Sun's newest operating system. So we guarantee full SunOS compatibility including: SunOS 4.1.1, Open Look, Open Windows, and ONC/NFS. All Sun application software and development tools run on a SPARCard without modification.



5 Fully Loaded

The SPARCard 2LC is a complete system on a card. Everything's on-board, including: 8-32 Mbytes DRAM, Ethernet, SCSI, VME interface, Open Boot PROM, Non-volatile SRAM, and two Serial Channels. Its MBus/VMEbus Controller has data FIFOs and hardware DMA for blazing VME performance.

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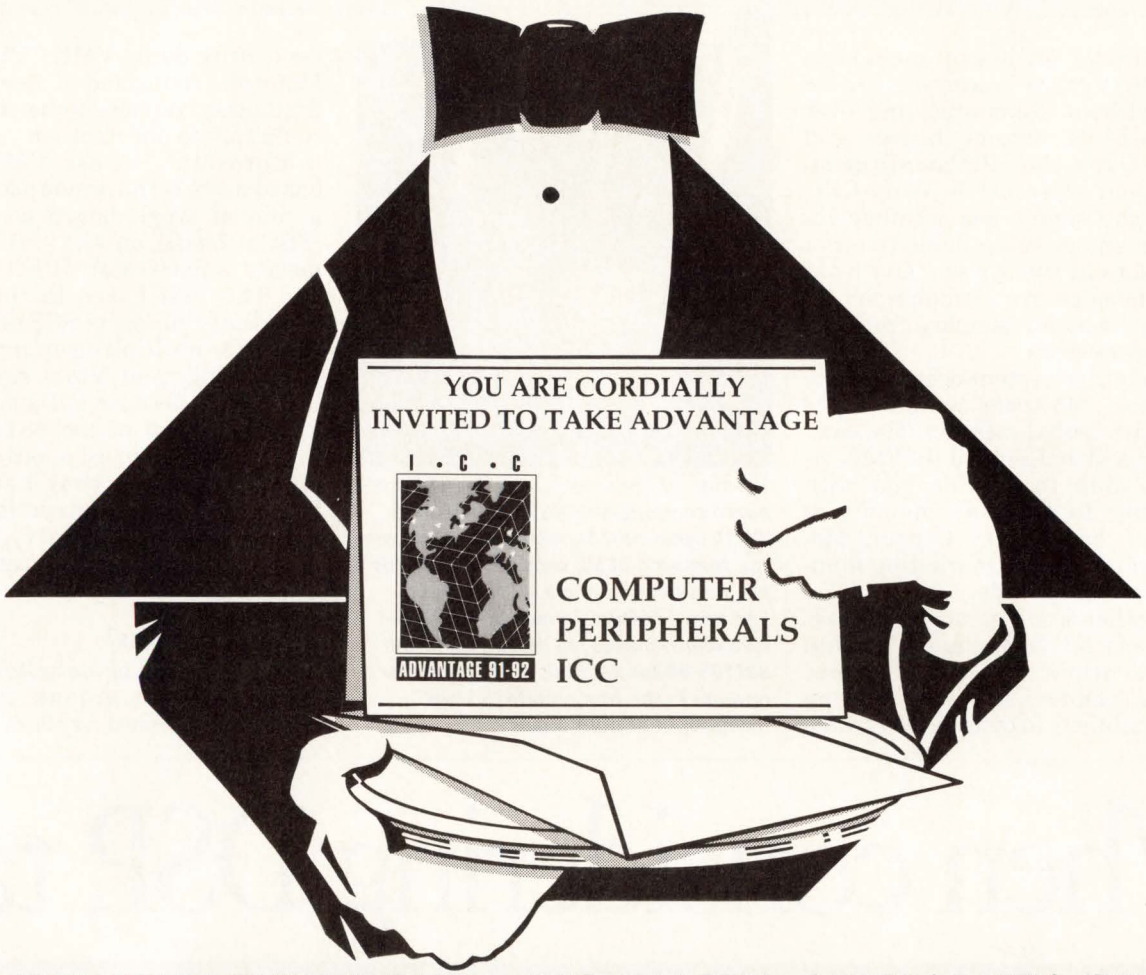
38610 Gieres, France
Phone 33 1 76 59 60 61, Fax 33 1 76 63 00 30

CIRCLE NO. 72

Model	CPU(s)	CPU clock speed (MHz)	Math coprocessor	Memory (Mbytes)	Memory speed (ns)	DMA channels (no. and width)	I/O ports (no. and type)	On-board interboard expansion	Price
Radstone Technology 20 Craig Rd, Montvale, NJ 07645 (201) 391-2899									**Circle 309**
68-42	68040/020	40/20	In CPU	36	80	4 32-bit	4 RS-232/422/485	APEX	$4,595
RISQ Modular Systems 39899 Balentine Dr, Ste 200, Newark, CA 94560 (510) 490-0732									**Circle 310**
RISQengine/3e	R3000A	25	R3010A	8-32	400	4 32-bit	2 RS-232/423, SCSI, Ethernet	VSB	$8,495
RISQengine/5e	R3052E	25-40	R3010A option	2 - 32	175	4 32-bit	2 RS-232/423, SCSI, Ethernet, custom I/O	RISQbus	$2,995
SBE 2400 Bisso Ln, Concord, CA 94520 (800) 347-2666 (510) 680-7722									**Circle 311**
VPU-25	68020	25	68882	1-4	160	—	2 multiprotocol serial ports	1 or 2 Green-Spring modules	$1,380
VPU-30	68030	25	68882	4-8	160	—	1 SCSI, 2 multiprotocol serial ports	—	$2,430
Synergy Microsystems 179 Calle Magdalena, Encinitas, CA 92024 (619) 753-2191									**Circle 312**
SV20	68020	12- 25	68882	1-16	80	On modules	4 RS-232/422	EZ bus	$1,395 - $5,280
SV30	68030	25, 33, 50	68882	1-16	70	On modules	4 RS-232/422	EZ bus	$1,995 - $6,430
SV400	68040	25 or 33	68882	2-32	70	On modules	4 RS-232/422	EZ bus	$2,395 - $6,390
Tadpole Technology 8310 Capital of Texas Hwy N, Austin, TX 78731 (800) 232-6656									**Circle 313**
TP-34V	68030	20 or 33	Optional	4 to 32	80	4 32-bit	1 Ethernet, 2 SCSI, 6 serial	—	$4,400
TP-881V	88100 (up to 8)	20 or 33	In CPU	8-128	80	—	1 Ethernet, 2 dual SCSI 2, 4 serial	M bus, VSB	$9,200
TP-IGCV	68020	20	Optional	1-8	100	On VIC	2 serial, 1 mouse, Ethernet	—	$4,850



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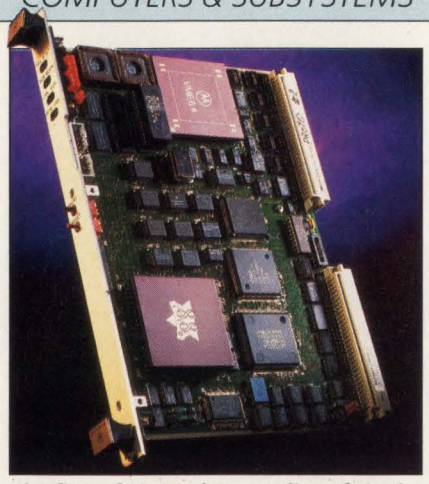
CIRCLE NO. 75

COMPUTERS & SUBSYSTEMS

while large on-board memories mean that more processing can be done without communicating over the VMEbus, outside boards still need to access the CPU board's memory. When selecting a VME CPU board, you should ask whether on-board memory is available to other processors in the system, and what methodologies are available for accessing on-board memory from off-board processors.

To let other system boards talk to its board, Motorola configures its CPU with global memory. The company has also designed its VME interface chip to provide you with flexibility in the way memory is mapped, says Jerry Gipper, Motorola product line marketing manager for VME boards.

The other trend in memory access is support for D64, the 64-bit data mode for transfers across VMEbus. Several vendors are now offering this capability. To test the D64 transfer feature on its VME CPU board, Motorola connected a few boards from other vendors to be sure they could talk to one another.



The first of Motorola's new line of single-board computers (SBCs) is based on its 88110 symmetric superscalar RISC processor, featuring SCSI2 support, multiple users, networking, and a VSB interface. The board features a memory architecture which makes maximum use of the 88110's 64-bit data bus and lets memory operate in the burst mode to keep throughput at peak levels.

Motorola's latest VME CPU board news is the announcement of a line of single-board computers (SBCs) based on the 88110 symmetric superscalar RISC processor. The first board in the series reportedly supports SCSI2 peripheral I/O, multiple-user interfaces, networking, and VME subsystem bus (VSB). Because of the high performance level of the 88110 chip, the board features a burst-mode memory scheme that keeps the 88110 fed with instructions and data. The board's memory array is designed to take advantage of the 88110's 64-bit data bus.

Who's the boss?

Because the rest of the system is typically designed around the CPU board, CPU board vendors are the

When considering DSP, take

first to hear demands for increased sophistication—especially for greater system controller capability. In the past, many system controller functions—so-called slot "1" functions—were considered optional on a CPU board. Today, designers are unwilling to dedicate multiple slots to various functions and would rather have them all on the CPU board.

Review controller capabilities

When evaluating a VME CPU board, AP Labs' Davis suggests looking carefully at its system controller capabilities. Can it be a master? Can it arbitrate masters in the system? What different scenarios of arbitration does it support? (There are three available within VME—some only do round-robin, some do priority-based and round-robin, and some do only daisy chain.) Knowing how configurable the system interface is helps figure out who's going to be the boss in the system.

Any board that has a VIC chip has the potential for being the slot 1 system controller board. The VIC chip can be set up to use the full range of system controller functions. While CPU vendor Radstone Technology (Montvale, NJ) uses the VIC chip on its boards, it also has another system control feature on its commercial boards. "To address the needs of multiprocessing applications, we use an ID switch on our boards which the software can read," says Joel Silverman, marketing manager for commercial products at Radstone. "This lets you remove a non-system-controller board from slot 2, toggle its switch to the slot 1 setting and put it in slot 1. The system software will then know that it needs to boot from that board as the system controller."

For its military CPU boards, Radstone offers a similar feature, except that it uses the backplane to configure the board. "Once you have a military board in an application, you may have multiple [units] of the same board within a system," says Douglas H. Patterson, marketing manager of military products. "To cut down on logistics costs and spares, the backplane actually determines which board is the slot 1 master through a set of ID pins. You unplug one board from slot 2, plug it into slot 1 and automatically know that it's going to be the slot 1 arbiter."

Reflecting the view of many VME board vendors, Gipper generally sees fewer compatibility problems these days. "Compatibility issues aren't nearly as bad as they used to be," he says. "Especially now that vendors use ASICs so they can standardize across several designs. Even if it's wrong, at least it will be consistently wrong. Now it's more an issue of dealing with new features as they are added to VMEbus, or with features that were never tested because the capability wasn't there—such as DMA and block transfer." ■

INTEGRATED CIRCUITS

Sample-and-hold includes on-board output multiplexer

The Datel MSH-840MC is a four-channel simultaneous sample-and-hold (S/H) device that includes an on-board multiplexer packaged in a 32-pin TDIP (thin DIP) package.

Datel claims the part breaks some of the classic rules of S/H architectural design. A typical S/H circuit design trade-off is that as device speed increases, the part loses accuracy—signal loss (or droop) at the S/H output stage is caused by the slow discharge of the hold capacitor. Datel claims to have circumvented such problems with a novel architectural design in both the S/H and multiplexer sections of its product. The MSH-840MC can acquire a 10-V step to 0.01 percent accuracy in just 775 ns, including the time taken to multiplex the signals on-chip.

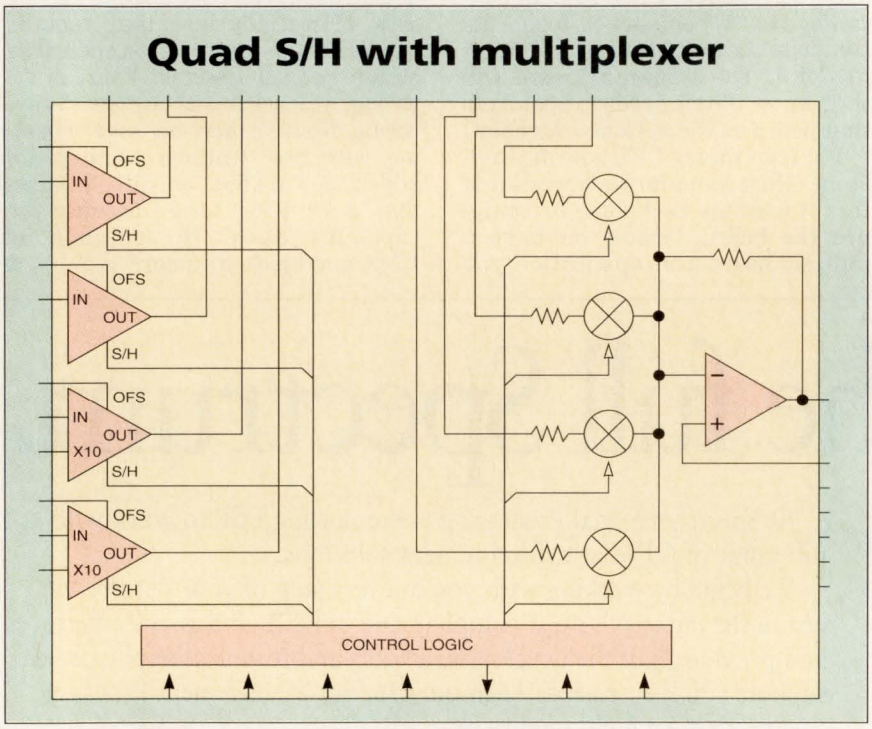
While it may be possible to obtain similar speed and accuracy with competing parts, the resulting designs would be much larger and the power consumption higher. "If you look at the speeds of sample-and-holds, a single 12-bit 200-ns sample-and-hold costs anywhere from $150 to $180. We have effectively taken four of those sample-and-holds, plus a multiplexer, and still have obtained a speed of 775 ns at a cost of less than $250—an order of magnitude improvement," says Bob Leonard, Datel's MSH-840MC product marketing manager. Applications for such a device include phased sonar arrays and the correlation of signals acquired from multiple receiver channels.

In addition to the speed and accuracy of the S/H circuitry, Datel's breakthrough multiplexer architecture lets the company break some previous speed barriers for multiplexers. "Right now, for 0.01 percent accuracy (which is effectively 12 bits), the fastest competitive stand-alone multiplexer in the market has a settling time of 600 ns to 0.01 percent accuracy," adds Leonard.

The MSH-840MC can operate in two modes: scan mode and single-channel sampling mode. The scan mode lets you sample up to four channels at the same time. In the single-channel mode you can randomly select a particular channel for digitization by an external analog-to-digital converter. In either mode, logic is also provided to set all the S/Hs either to the sample or hold mode; this can be done simultaneously or individually. The logic which lets you put all the S/Hs into a single mode is normally achieved on such devices through external glue logic. With the Datel chip, however, it's done internally to the device.

Traditionally, the performance of such devices has been measured in two ways: statically or dynamically. While the offset error, gain, linearity, and transfer accuracy may be tested with a dc input, designers often use very high frequency signals in the 100- to 500-kHz range in actual implementations. As a result, they require some indication of the part's performance in high slewing input conditions—parameters gained by the measurement of the total harmonic distortion of the device. The dynamic specifications of the MSH-840MC include a harmonic distortion of –70 dB for a 500-kHz input frequency, a slew rate of 45 V/µs and a small signal bandwidth of 13 MHz.

The part operates up to a ±10-V input range and has a maximum nonlinearity of ±0.01 percent over the full operating range. A 10-MΩ input impedance avoids the need for costly input buffers that are required for some sample-and-holds. Two operating temperature range models are available: a commercial 0° to +70°C part and a military –55° to +125°C part. — *Dave Wilson*



The MSH-840MC is a quad sample-and-hold device with an acquisition time of 775 ns. It contains a four-channel multiplexer that lets you select S/H outputs individually.

MSH-840MC at a glance

- Four-channel simultaneous sample-and-hold device
- Internal four-channel multiplexer
- 775-ns acquisition time
- 10-V step to 0.01 percent (including multiplexer) accuracy
- Consumes only 2.25 W

Datel
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Mansfield, MA 02048
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Circle 352

INTEGRATED CIRCUITS

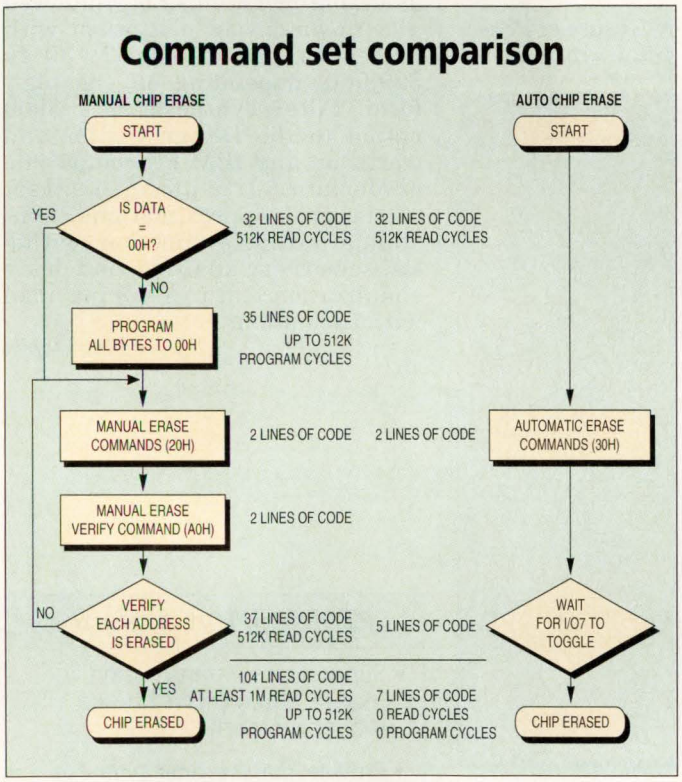
Block erase capabilities come in a flash

With this month's introduction of a 4-Mbit flash memory device, Hitachi America (Brisbane, CA) claims to have brought the capabilities of block erasure to these devices for the first time. In a 512k × 8 configuration, the company's HN28F4001 is divided into 32 blocks of 16 kbytes. You can erase the entire chip randomly, one block at a time or multiple blocks simultaneously.

According to Sean Pitonak, product marketing engineer at Hitachi, the device's organization was determined by two important parameters: customer input and the economics of the marketplace. On the customer side, a 16-kbyte block size is attractive to both flash memory card designers building alternatives to floppy disks and designers who may use the device as an alternative to EPROMs in PC BIOS designs.

From a chip designer's perspective, as the number of blocks increases, more transistors must be added to the die, increasing the cost. Thirty-two blocks was deemed to be an optimum size for the price point the company was trying to reach.

The product adheres to the JEDEC Standard Flash Command Set. The command set defines both manual and automatic commands for programming, chip erase and block erase, but leaves the chip manufacturer to define the size of the block. These automatic commands let you issue only one set of commands to program, chip erase or block erase without a verify algorithm, giving you a reduced software interface to the device.



There's a big difference in the number of lines of code you need to write when you use the Hitachi flash memory in automatic versus manual mode.

In the manual mode, the processor first has to read the flash to determine if it's erased. If it hasn't been, the processor has to prewrite and erase the flash, then verify the erasure by going back to read each byte. Automatic commands, on the other hand, free the processor of the need to control the flash, eliminating about 100 lines of code. "A pretty significant amount of processor overhead gets eliminated by using the automatic mode—we feel that's a real nice feature of the part," says Pitonak.

Flash automatically erases

In the automatic block erase mode, the flash prewrites, erases and verifies itself through status polling after the automatic erase starts. When only one byte of data is programmed, programming completion is verified by polling the data line after the automatic programming starts.

Pitonak says these programming methodologies mimic those already used in the EEPROM world, so that users migrating to flash from EEPROM will be familiar with them. "In operation, the processor simply sends out a command and waits for one bit to come back to verify the state of the flash," he says. This eliminates the processor's need to keep track of code overhead, and frees the system bus to carry out other operations.

Chip erase time is typically one second and byte programming is typically 10 µs/byte. Endurance is a minimum of 10,000 erase/write cycles, and versions with maximum access times of 120, 150 and 200 ns are offered. Typical power dissipation is 30 mA. Standby power dissipation is a maximum of 20 µA. The part is available in a variety of configurations. They include an 8 × 20-mm TSOP-Type 1 (Thin Small Outline Package). Also available are a 32-pin plastic DIP and a 32-pin plastic SOP. The device is sampling this month at $49 for a quantity of 1,000.

The pinout of Hitachi's new device is the same as that of earlier parts, providing a migration path for designers who may already be using 1-Mbit or 2-Mbit flash devices. Currently, however, the Hitachi 4-Mbit device doesn't meet a JEDEC standard—but only because there isn't one for flash with density above 2 Mbits. Even so, Hitachi expects many vendors to follow its pinout in the near future. *— Dave Wilson*

HN28F4001 at a glance

- 4-Mbit flash memory
- Supports block erase
- 10,000 erase/write cycle endurance
- 120-, 150-, 200-ns access times offered
- 30-mA active power dissipation

Hitachi America
Semiconductor and IC Division
2000 Sierra Point Pkwy
MS-080
Brisbane, CA 94005
(800) 448-2244

Circle 351

CAE/CAD TOOLS

Simulator supports transmission line models and filter synthesis

Version 5.1 of the PSpice circuit simulator from MicroSim (Irvine, CA) offers two new features—the ability to model lossy transmission lines based on the distributed model approach and support for the synthesis of passive filters. The first feature lets you simulate transmission line behavior affected by attenuation and dispersion—properties that are especially troublesome in high-speed circuits.

According to MicroSim, using the distributed rather than the traditional lumped model approach lets PSpice simulate lossy transmission lines in significantly less time, while producing a more accurate approximation of the line's behavior. The distributed model simulates a continuous line specified by electrical length and the resistance, inductance, capacitance, and conductance distributed along its entire length. The line's behavior is computed from this data using impulse responses.

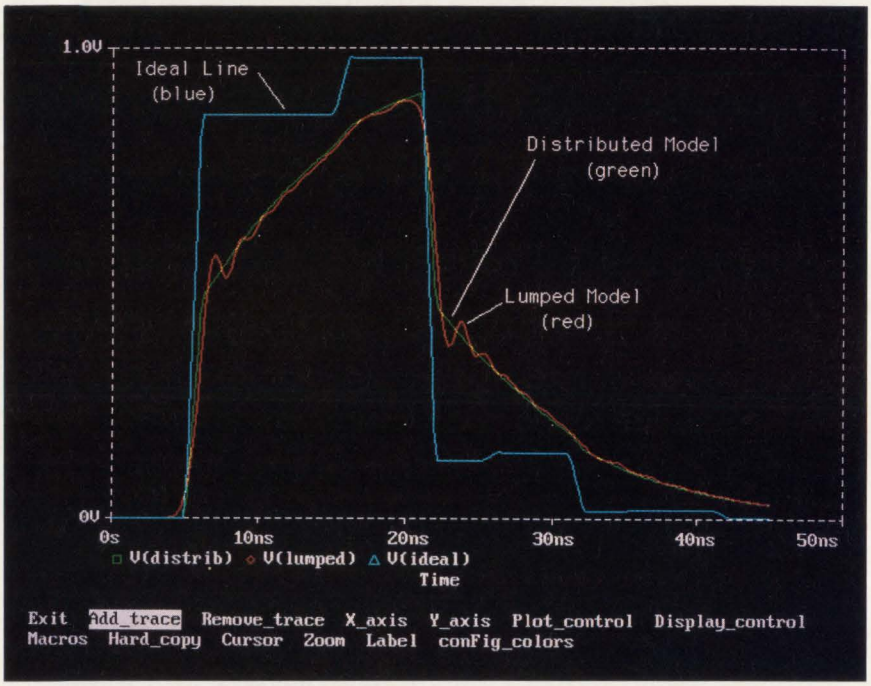
This technique avoids the overhead introduced by the lumped model approach, which describes the lossy line as a string of line segments where each segment is modeled with discrete passive components. The lumped model approach also produces oscillations at points where abrupt changes occur in the signal traveling along the transmission line. In PSpice, these frequency artifacts are eliminated by modeling lossy lines as continuous lines.

The second new feature of PSpice 5.1, the passive filter synthesis capability, lets you compute and evaluate inductor and capacitor values by selecting either minimum inductor or capacitor configurations. A Preference Screen guides you through design specification and configures the filter synthesis for specific applications. Filter specification can be customized to accept stop band properties or filter order, while band pass and band reject filter specifications can include upper and lower bounds or center frequency and bandwidth. Suitable default frequency units (Hz through GHz) can be specified, as can filter type—continuous or sampled-data.

In addition to gain, phase and group delay, the enhanced Bode plots submenu lets you examine linearized phase and phase delay. The Bode plots, as well as step response and impulse response plots, provide a cursor for zooming and displaying plot values numerically.

PSpice is an integrated member of MicroSim's Design Center analog and digital circuit design environment. The Design Center is available on a number of windowed and unwindowed platforms, with prices ranging from $2,450 to $29,000, depending on the platform. Filter synthesis is a $900 option to the Design Center and works on any IBM PC-compatible or Macintosh II platform. A full set of classical approximations, nonstandard transfer function synthesis, sensitivity analysis, and delay equalization features are included with the option.

—Mike Donlin



PSpice Version 5.1 supports lossy transmission line models based on the distributed model approach. In this comparison of a distributed model and a lumped model to the ideal signal, the distributed model eliminates frequency artifacts by representing lossy lines as continuous signals.

PSpice 5.1 at a glance

- Supports lossy transmission line models based on distributed model approach
- Provides passive filter synthesis capability
- Evaluates inductor and capacitor values of filters by selecting either minimum inductor or capacitor configurations
- Lossy transmission line modeling capability is available now as part of the Design Center—an analog and digital circuit design environment
- Filter synthesis is a $900 option

MicroSim
20 Fairbanks
Irvine, CA 92718
(714) 770-3022
Circle 354

CAE/CAD TOOLS

Simulator histograms ease timing analysis

High-speed ASICs and PCBs pose a number of challenges to circuit simulators. One of the most formidable is predicting dynamic or worst-case timing hazards across a circuit to find the worst possible delay combinations. Start-up Nextwave Design Automation (Mountain View, CA) has brought new thinking to the timing analysis problem with its Verilog-based simulator, Epilog.

The tool is an event-driven logic simulator with two timing modes: Epilog Min/Max and Epilog Histogram. What sets Nextwave's simulator apart from other event-driven tools is its histogram approach, which uses actual component and interconnect delay distributions propagating through a design to produce accurate delay histograms for each internal node and signal.

"The histogram capability brings a level of intelligence and analysis to the task that other simulators don't offer," says Hal Daseking, president of Nextwave. "Simulators that don't see a range of min/max values miss errors because of the production variations that cause delays such as interconnect anomalies, heat or cold effects and component manufacturing variances. Dynamic timing verifiers can take a range of variances into consideration, but they can give pessimistic results if they just tally up a list of every possible timing violation."

Fine-tuning the analysis

Epilog identifies the most likely hazards instead of searching through many random timing problems. The five-segment histogram represents the distribution of delays for each node and finds hazards common to digital designs through timing detectors built into models or placed on design nodes to produce a hazard report. You can select hazards by their probability, signal name or other parameters.

The approach does exact some penalty compared to traditional min/max simulators, because it requires more CPU power to analyze hazards. According to Nextwave, this penalty is only 10 to 15 percent.

The other mode for the simulator, Epilog Min/Max, is a traditional dynamic worst-case timing analyzer. It offers common ambiguity removal, a feature that traces signals backward to minimize pessimism caused by shared delays in reconverging signals. "Though common ambiguity removal is essential, it simply isn't enough," Daseking points out. "In that approach the simulator carries around two values—minimum and maximum—that refer to the delays of each gate. Because no weight is assigned to either value, the tool assigns equal values and probabilities. Because it continuously adds these values together, they accumulate and generate a lot of false errors."

Epilog is available now for $45,000. It operates on Sun workstations, though ports to other Unix systems are under development.

— Mike Donlin

Epilog at a glance

- Verilog-based logic simulator with two modes: Epilog Histogram and Epilog Min/Max
- Epilog Histogram uses timing detectors to generate timing hazard report
- Detectors can be built into models or placed on design nodes
- Five-segment histogram can filter out portions of a delay range falling below a given probability
- Available now on Sun workstations for $45,000

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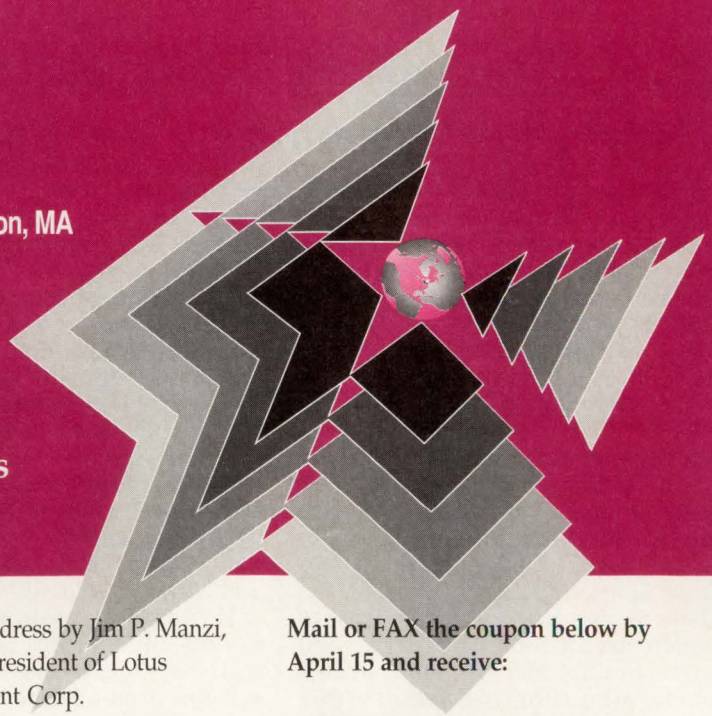

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CIRCLE NO. 77

SOFTWARE & DEVELOPMENT TOOLS

Automated software testing for window-based systems

Computer-aided software testing (CAST) is a method for automating regression testing of today's complex, window-based applications, be they running under MS-Windows, OS-2 or Unix/X Windows. Ferret, a new testing system by Tiburon Systems (San Jose, CA), uses a capture/playback scheme to let you analyze testing requirements, design tests, capture and playback user activity, produce bug reports, and assess software product maturity.

Ferret is entirely nonintrusive. It runs on a personal computer and connects to the system under test via an interconnect unit that taps into the target system's keyboard, mouse and serial I/O lines—and to the display by way of a scan converter.

All activity and its results on the target system can be monitored and recorded. This includes snapshots of the target's screens, with annotation. The graphics analysis monitor (GAM), part of the Ferret hardware, compares expected test results to actual display differences down to the individual pixel.

Capture/playback at the core

The heart of Ferret is its capture/playback software, which records all user keyboard and mouse actions and their results, as well as screen results, and time-stamps them. These actions can be played back to the target system or used in the construction of more elaborate test suites. Test scripts can be constructed from monitored and captured user activity, as well as from requirements imported from a CASE environment.

The test engineer uses a spreadsheet tool to construct test cases on matrices from the requirements. Using the matrices and a test control language, you can "teach" Ferret each test. Then you can enhance testing with repeatable loops for an exhaustive exercise of the program—up to 24 hours. In case of a crash of the target system, Ferret can be programmed to reset and restart, dial a phone number or otherwise alert the test engineer.

Additional aids

Ferret includes Microsoft Word to aid in analysis of requirements documents, prepare bug reports and do general word processing. It also includes Microsoft Excel for the design of electronic test matrices. Each testable requirement is laid out in a row and each test case in a column. This permits easy organization of tests into groups.

Another third-party package, the Owl Hypertext Guide, is used to link requirements text via buttons to the test matrices, scripts, results, and bug reports. This lets you link together all the information needed to analyze a given problem in a way that's self-documenting and self-organizing.

The final module is the maturity prediction software, which lets you define an initial desired quality level, estimate the time for the test phase and monitor the effectiveness of testing.

Ferret will be available for shipping in March of 1992. The system, which includes the five software packages and four hardware subsystems (PC, GAM, cable interface box, and scan converter) and is priced at $26,450. *— Tom Williams*

Ferret at a glance

- Nonintrusive testing captures user activity and target response
- Lets you build user activity into test suites and automate exhaustive testing
- Interfaces to target via target keyboard, mouse and monitor
- Pixel-level comparison of displays is supported
- Runs on 80386 PC workstation under Windows 3.0
- Includes standard software packages for word processing and Hypertext document organization

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Circle 355

COMPUTERS & SUBSYSTEMS

National releases protocol controller

National Semiconductor (Santa Clara, CA) has released the DS3805 protocol controller chip it's been working on with Newbridge (Kanata, Ontario) over the past several months. The product will round out National's Futurebus+ chip family, which includes handshake, arbitration and latching transceivers and an arbiter IC. Newbridge will also market the controller.

National is behind Signetics (Sunnyvale, CA), its largest competitor in the Futurebus+ market, in announcing a protocol controller chip. "We wanted to wait until the Futurebus+ specification was firmly nailed down before we committed to developing any silicon," says National product manager Phil Hughes. He adds that it was worth the wait because the company was able to closely tailor the chip to the needs of a large majority of users.

Compelled mode only

Because the specification isn't nailed down tightly enough to include the faster packet-mode transfer mechanism, National has stayed with the compelled transfer mode for its Futurebus+ protocol controller. "The Standard Bus Architecture Committee of the IEEE (formerly the Futurebus+ subcommittee) is currently finalizing the faster protocol, and when it does," says Hughes, "we will be there with the right silicon."

The DS3805 controller monitors and handles all handshake signals required for Futurebus+ transactions and can serve either as master or slave. It can deal with connected as well as split transactions, but not with cache-coherent transactions. (Additional external logic is required to help the DS3805 perform cache-coherent operations.) The chip's logic also includes all internal FIFOs and decoding logic, along with address regeneration for the retries and block-length mismatches.

The chip includes its own internal direct memory access controller and Futurebus+ programmable registers. The latter let you use the chip effectively in all applications—from simple I/O boards through cache-coherent single-board computers, using either RISC or CISC processors.

The protocol controller also contains reset logic that monitors the local and Futurebus+ reset signals and register commands. It generates the appropriate reset events to these external signals, as well as to internal events such as transaction timeouts.

Protocol transactions

The DS3805 provides a generic 32-bit local interface that converts whatever protocol is used on the local bus of the module into Futurebus+-like information and simple address and data strobes with acknowledges. If called for, the chip will convert 32-bit local transactions into 64-bit Futurebus+ transactions by packing data and using an address-extension register. The 64-bit address decoding and unpacking provisions are used to convert Futurebus+ transactions into 32-bit local transactions. Only the lower 32 bits of the address are carried through.

The internal read/write registers are accessed through the 32-bit local interface, either directly or via a Futurebus+ access. In this way the local address decoder can reflect to the on-chip registers, letting the board's logic use additional registers directly. The registers are used to tailor the operation of the IC to a particular application. But, at power-up time, the chip shows default values for all parameters, letting it be accessed as a slave.

Bells and whistles

National's new interface chip has all the logic for both the Futurebus+ interface and a flexible interface for most local buses, from a simple peripheral bus to any of the most recent CPU architectures. Split and locked transactions are supported on both local and Futurebus+ interfaces to permit tightly coupled multiprocessing both on the board and across the backplane. The internal logic supports burst transactions from one to 64 transfers, with unlimited length allowed for connected transactions.

The busy/retry circuitry provides the ability to break a burst transaction into multiple subbursts of a particular length—of 16 or 32 bits, for example—to let specific slave modules or a local bus manage. This permits each module on the backplane to operate with the most efficient length for its local bus and for the Futurebus+ itself.

The chip supports a full 32-bit local and 64-bit Futurebus+ address and data path and connects directly with standard Futurebus+ transceivers. Expansion of the address to 64 bits, if required, is managed by programming an internal address extension register to create a 64-bit Futurebus+ address.

Since the chip doesn't directly support full cache coherency, it's primarily designed as a Profile B chip, though most of the hooks are included to let it operate as a Profile A controller. According to Hughes, National intentionally took this approach because the company found in working with designers that, for the immediate future, the largest number of systems—and board-level products—will be looking for a Profile B controller.

— Warren Andrews

DS3805 at a glance

- Fully compatible with IEEE-896.1 Futurebus+
- Low-power CMOS
- 32-bit local bus interface
- 64-bit Futurebus+ data and address available
- Supports split and locked functions
- Parity on all command lines
- Incorporates FIFOs and logic to decouple Futurebus+ for local bus
- IEEE-1149.1 JTAG testability port

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Circle 358

ASICs & ASIC DESIGN TOOLS

ASIC designers gain GaAs arrays with 10K, 20K usable gates

To extend the price and performance benefits of its 0.6-µm GaAs technology to the majority of ASIC designs, Vitesse Semiconductor (Camarillo, CA) has just added 20,000- and 40,000-gate arrays to the higher-density members of its FX GaAs gate array family. Like their 100,000-, 200,000- and 350,000-gate Si siblings, the new arrays have a sea-of-gates architecture with four-layer metal routing.

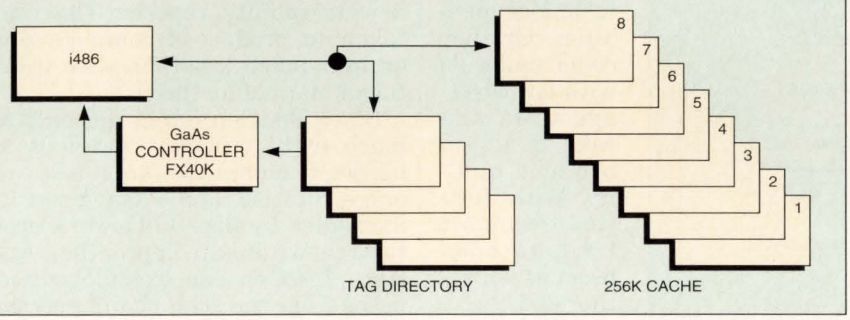
The FX20K (10,000 usable gates) and FX40K (20,000 usable gates) offer up to four times the speed performance available in competing silicon BiCMOS arrays. A typical two-input NOR gate has a worst-case delay of 60 ps unloaded, while dissipating only 0.18 mW of power. That performance yields a speed-power product of 11 fJ, significantly better than silicon BiCMOS at approximately 25 fJ at 100 MHz, or silicon ECL at about 50 fJ.

Competitive performance

"For applications above 150 MHz, there is really nowhere else to find the kind of performance you get with FX," says Vitesse director of ASIC products Ray Milano. "Even at slower speeds—between 80 and 150 MHz, for instance—FX is very competitive with silicon BiCMOS, both in terms of power consumption and price. By adding the smaller arrays to the family, we have substantially increased the base of applications that FX can cover."

More than 50 percent utilization of the FX20K and FX40K gate arrays is possible through a custom masterslice option where you can incorporate fully custom logic into the base array. You may also elect to embed megacells such as RAM and register files into one of the base FX arrays. To speed the design cycle for custom RAM blocks, Vitesse supports RAM compiler technology. Moreover, you can minimize skew of clock signals by using an optimized clock distribution scheme developed for each array in the family. Signal interfaces are configurable to ECL, TTL or mixed ECL/TTL signal levels.

Second-level cache control using the FX40K



This block diagram shows a cache controller scheme for a 50-MHz i486 using the Vitesse VGFX40K GaAs gate array and commodity SRAM for the tag directory and for the cache itself. Since the speed of the GaAs controller is high (5 ns pin-to-pin), users can achieve zero-wait-state performance with 12-ns tag directory RAM in a 50-MHz system or 10-ns RAM in a 66-MHz system.

Lower pin-to-pin delays

With I/O delays of less than 3 ns, the FX20K and FX40K can achieve pin-to-pin delays of less than 5 ns. By implementing critical cache control functions such as tag comparison with these arrays, you can eliminate unnecessary wait states in the operation of high-speed RISC and CISC processors. What's more, you can significantly reduce overall system cost by using inexpensive commodity SRAM for tag or cache functions, since the FX gate arrays can make up the difference in the timing margin. Vitesse claims the FX20K and FX40K contain enough resources to implement even the most sophisticated cache control schemes, such as multiprocessor, set-associative or write-back compatibility.

With internal flip-flop toggle rates exceeding 1 GHz and input receivers and output drivers capable of bandwidths in excess of 1 GHz, the FX20K and FX40K are well suited for implementing complex DSP algorithms such as infinite or finite impulse response filters and fast Fourier transforms, crosspoint or crossbar functions which route data streams in excess of 300 MHz but require low power dissipation.

Package options for the FX20K include a 52-pin ceramic LCC and a 132-pin ceramic LCC or PGA. The FX40K is available in a 184-pin ceramic PGA. You can design FX arrays with Mentor and Cadence/Valid schematic capture and logic simulation tools, Synopsys synthesis and Teradyne's Lasar simulator.

The FX20K and FX40K are available now with nonrecurring engineering expenses ranging from $70,000 to $120,000 and production prices ranging from 0.5 to 1.25¢ per utilized gate. —*Barbara Tuck Egan*

FX20K & FX40K at a glance

- 0.6-µm GaAs manufacturing technology
- 10,000 and 20,000 usable gates
- Worst-case delay of 60 ps unloaded for typical 2-input NOR gate
- Speed-power product of 11 fJ
- I/O delays less than 3 ns, pin-to-pin delays less than 5 ns
- Flip-flop toggle rates exceeding 1 GHz

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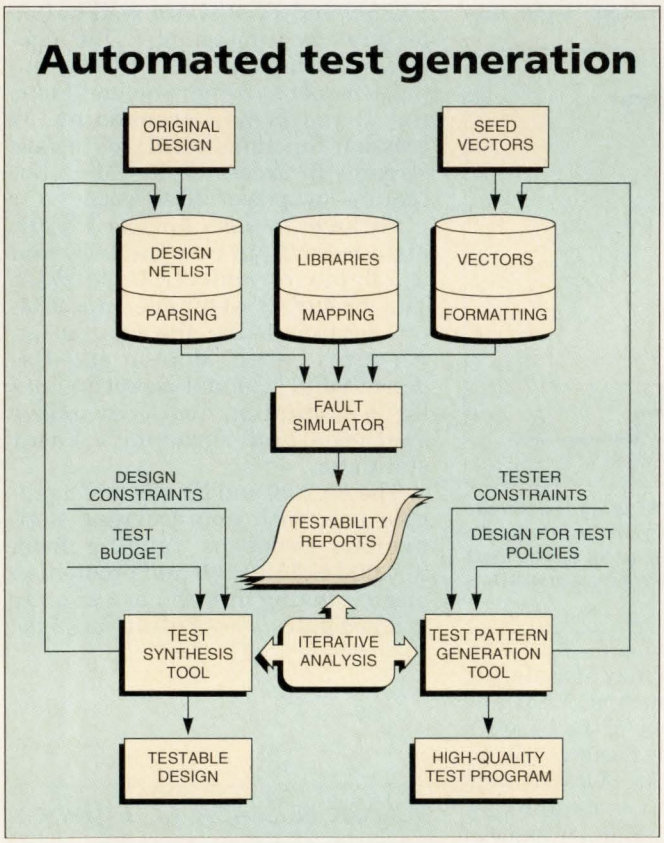
ASICs & ASIC DESIGN TOOLS

Partial-scan sequential ATPG tool handles complex ASICs

TestGen from Sunrise Test Systems (Sunnyvale, CA) is a tool for partial-scan sequential automated test pattern generation (ATPG) that accommodates the full range of circuit types—including combinational and sequential logic, and synchronous as well as asynchronous circuits. TestGen integrates a test vector generator, fault simulator and test synthesis tool. For low- and moderate-complexity ASICs, Sunrise offers a version of TestGen that works only with gate-level designs and prequalified libraries. For complex ASICs and full-custom ICs, a second version accommodates transistor-level descriptions and supports custom libraries.

Unlike traditional full-scan methodologies, which require a large number of test circuits to be built into the chip, TestGen places no restriction on the design and does not compromise chip size and performance. "In the past, chip designers had a no-win choice," says Jean-Pierre Braun, vice-president of marketing and engineering at Sunrise. "They could opt for the high fault coverage of the full-scan approach, with all its size, cost and performance penalties. Or they could make do with low-coverage tests and take a hit on product quality. With TestGen they don't have to compromise on either end."



If testability reports from TestGen's fault simulator indicate coverage that's less than acceptable, you can use the test vector generator to create additional vectors or the test synthesis tool to selectively insert scan points.

TestGen is a back-end tool, for use after a preliminary chip design is completed. It requires only a netlist from standard CAE tools such as those from Cadence, Mentor, LSI Logic, and Toshiba.

The fault simulator in TestGen issues a testability report detailing fault coverage provided by functional vectors. If the testability report shows fault coverage that's less than acceptable, you can use TestGen's test vector generator to create additional vectors for increased coverage. But if there's a lack of either controllability or observability, it may be impossible for vectors to turn up faults unless the circuit itself is altered. For that reason, the fault simulator also issues a structural analysis of the circuit's testability, describing faults that may be undetectable because of problems with controllability and observability.

If hard-to-test structures are found, you can use the test synthesis tool to insert scan points into the circuit. To avoid any speed penalty, you can exclude performance-critical logic blocks, paths or gates from scan insertion. The output of the test synthesis tool is a new netlist, automatically modified to include the scan circuits.

Shorter programming time

The test generation process is iterative and until target coverage has been reached, you can continue feeding vectors from the ATPG tool and new netlists from the test synthesis tool back into the fault simulator for new testability reports. The time taken to produce a complete program is much less than with traditional manual methods.

Since TestGen integrates only as much extra circuitry and I/Os as needed to obtain the target test coverage, Sunrise claims its use results in smaller die sizes and lower silicon costs than full-scan approaches. And since TestGen can exclude critical paths from the scan chain, you can minimize the effect of the software on device speed.

TestGen runs on Unix workstations from Hewlett-Packard and Sun. Custom TestGen, for use with custom ICs and complex ASICs, is priced at $160,000. ASIC TestGen, for use with most ASICs, is priced at $95,000. Both are available now.

—Barbara Tuck Egan

TestGen at a glance

- Handles combinational and sequential (synchronous and asynchronous) logic
- Selectively inserts scannable circuits
- Performance-critical paths can be excluded from scan chain
- Accepts netlists and libraries from major CAD tools
- Usable for low- and high-complexity ASICs as well as full-custom ICs

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Sunnyvale, CA 94086
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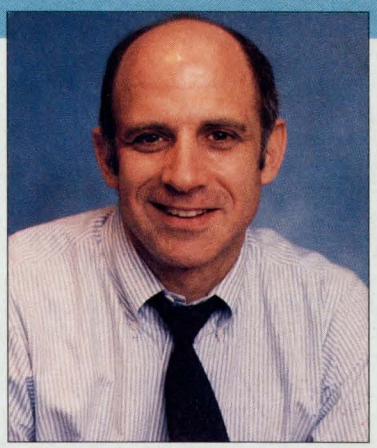
Circle 357



CAE tools for analog: just interesting or essential?

It wasn't long ago that hard-core analog designers took great pleasure in bad-mouthing the available CAE tools. Analog design—and any serious mixed-signal design that pays careful attention to analog—requires a different toolset than digital design. And, in terms of utility, the tools for analog and mixed-signal design have followed strictly digital tools by a good three to five years. Consequently, the promotional handles put out by analog tool vendors often got a negative response from influential critics. National Semiconductor's analog guru, Bob Pease, has written that simulation can't replace careful component selection and breadboarding, and Linear Technology's Jim Williams has said "don't get me started."

But the once-venomous tone has now changed into something considerably more conciliatory. Jim Williams admits he's "exploring ways to use what these guys have." He said recently that the experienced designer will most likely use multiple tricks—including CAE tools. "The really good technologist is aware of a spectrum of solutions," he says.

There are several factors driving the acceptance of analog design tools. First, there's a perceptible change in ease of use. Second, simulation—the real bugaboo of analog design—is getting faster and less painful. This is a direct result of improvements in simulation algorithms, the penetration of behavioral modeling techniques and the use of more powerful desktop computers. There's also a subtle change in the way analog designers think about their work. In a word, analog design is becoming *more abstract*. It's this acceptance of a higher level of abstraction that's creating a favorable environment for analog tools.

Better hit rates

While analog toolsets aren't as horrendous as the worst critics have made out, they've hardly been as wonderful as the trade show demos would have you believe. For analog design tools, though I'd argue the overall "hit rate" is getting better. Much better.

First, there's improvement in graphics and ease of use. This is most noticeable for PC-based systems, which are getting the lion's share of design tool development. Those of us who've breadboarded circuits with soldering pencils and Global Specialties clip blocks, or who've tweaked Spice decks to run on an IBM 3033, may express a certain amount of cynicism about the utility of desktop analog tools. But one should never underestimate the ease-of-use factor, especially when it comes to equipping a department of young engineers. These tools have made a transition from "interesting" to "essential," while remaining "fun to use."

The ViewSim/SD simulator of Viewlogic Systems (Marlborough, MA) and the Design Center of MicroSim (Irvine, CA), for example, have graphical front ends which interface seamlessly with a Spice-based mixed-mode simulator. One version of Design Center takes advantage of the Microsoft Windows 3.0 environment to display PSpice-generated waveforms—analog and digital—in windows on the same screen with the schematic.

PSpice, because it was one of the earliest to use the PC as its platform, has the largest installed base of any of the Spice-based analog simulators—over 15,000 copies. Improvements to the graphical front end can't do anything but elevate the popularity of the tool, which now runs on Apple Macs, DECstations and Suns, as well as PCs.

Viewlogic, similarly, has built a tight coupling between schematic entry and simulation. You enter all simulation parameters on the schematic itself, and invoke the ViewSim/SD simulator with some clicks of a mouse pointer. (The schematic editor couples with PSpice and HSpice, as well as ViewSim.)

Viewlogic product marketing manager Karen Wills agrees analog design tools have traditionally lagged behind digital design tools in terms of sophistication—especially in their ability to manipulate hierarchical blocks with thousands of transistors. Viewlogic has nonetheless managed to incorporate a number of ease-of-use features for traditional analog designers—and the growing number of digital designers who, because of mixed-signal requirements, are now performing analog design.

Chief among these features is what Wills calls "context sensitivity," the program's ability to anticipate the circuit designer's next move. It's features like these that have given Viewlogic tools an installed base

in excess of 11,000 seats, digital as well as analog.

With each of these tools, the once-annoying transitions from schematic to simulation are now easier to make. This transition once required you to wait, sometimes for several minutes, while the computer made a translation from the graphical format of a circuit schematic to the netlist format of a Spice simulator. Even then, you often had to go back into the Spice netlist to rearrange things so the simulator would run properly. But now the netlist compilation runs so fast and smoothly that the process is typically invisible to the user.

Part of the speed of the process is due to 386- and 486-based PCs which approach workstation performance; part of it's due to tool vendors' efforts to tightly integrate schematic and simulator. The fact that Viewlogic and MicroSim tools run on 386-based PCs lets analog designers try out circuit ideas at their desks, without a Unix network and workstation.

Automated model generation

As *Computer Design* senior editor Mike Donlin pointed out recently (see "Mixed-signal board designers resist the siren call of simulation," Nov. 1991, p. 84), the use of board-level simulation will depend entirely on the availability of component models. This factor will make the difference between simulation or breadboarding on the PCB level.

Without decent op amp models, for example, the Bob Peases of this world are confronted with a very lopsided choice. You can spend a half-hour wiring together some resistors, capacitors and op amps—a big $1.38-worth of parts—and take bench measurements with a signal generator and oscilloscope. Or, you can spend the better part of a day writing a Spice model for your favorite op amp, and pray that it works with your simulator. Says Jerry Brown, MicroSim's director of software development, "Designers are very interested in simulation—but, if they don't have models, they breadboard."

Spice model generation is actually not as painful as it's tedious and time-consuming. Its simplicity or its accessibility results because it describes a *physical structure* based on electrical nodes. The model developer visualizes the nodes as a set of points—A, B and C, or 1, 2 and 3—and describes the physical entities that reside between two points—for example, resistors, capacitors, diodes, and transistor terminals. He or she then assigns some sort of value to the components—for example, ohms or nanofarads.

V1, in the listing below, is an idealized buffer—a voltage amplifier with a gain of 1. It resides between nodes 2 and 0 (ground). R2 is a 150-kΩ resistor residing between 2 and 0.

```
1 V     0  0 1.
2 R     1  0 10.
3 R1    1  0 15.K
4 C3    1  2 10.n
5 R2    2  0 150.K
6 V1    2  0 1.
7 R     3  0 10.
```

The problem with this type of node description is that you must pay careful attention to all types of nonlinear circuit elements if you want the simulation to be accurate. As a result, the idealized op amp buffer model must be replaced with a network of transistor models; and the idealized transistor model must be replaced with a network of resistive, capacitive, inductive, and nonlinear elements. A single transistor model, then, can consist of as many as 38 nodal components, each of which will be used as values in the matrix calculations the simulator performs to determine the voltage and current at every node with a given set of input conditions. In short, you don't want to spend a lot of time writing Spice models unless you're well compensated for doing it.

Spice models more accessible

Fortunately, Spice models are becoming more accessible, thanks to a number of factors. First, tool vendors are very diligent about providing usable models with their simulators. MicroSim, for example, provides model libraries—over 5,700 parts—with its PSpice simulator. Similarly, analog IC vendors, such as Analog Devices' PMI Division (Santa Clara, CA), are offering usable Spice models for their parts. While these models are not as detailed at the nodal level, they depict the behavior of the device within range of its data sheet parameters.

A second factor is current-generation compilers and modelers that are making it easier to create new models for packaged parts. Zeelan Technology (Beaverton, OR), for example, last fall introduced a parameter extraction system that rapidly builds detailed behavioral models of packaged components. The heart of the system is a component "measurement mainframe"—a dc-to-4GHz stimulus-response capture system—that gathers data on any prepackaged analog device.

Curve-fitting software, in turn, converts the captured data into a behavioral model. Using a "Z-deconvolution" curve-fitting technique, the generator will provide a model in Laplace form which easily supports behavioral modelers such as Saber from Analogy (Beaverton, OR). The system will extract Boyl models and parameters, as well as ASCII files. It will support Spice directly in its next generation.

Because these models are compiled from data extracted from actual parts, they provide a much more detailed description of device behavior than the generic parts models available through distributors. Because of its sophistication, Zeelan's model building system is best used by systems companies with strong commitments to board-level simulation, as well as by IC vendors under pressure to characterize their newest parts and provide precisely detailed models.

New compilers help out

New compilers, meanwhile, make it easier for you to build your own models by entering specific parameters to a generic symbol on a graphical screen. The computer then does the work of converting the symbol into a simulator model. One of the most promising of

these new compilers is DesignStar, a graphical front end for Analogy's Saber simulator.

Less of a "simulator" than a "modeler," Saber takes an entirely different approach than Spice to the process of describing analog behavior. Where Spice is wedded to electrical nodes, Saber describes the behavior of component blocks *as a whole*. It would be an oversimplification to suggest that Saber works "top down" while Spice works "bottom up," but that may be the best way of understanding these simulators.

If Spice calculates the voltages and currents at each node of a circuit at any instant in time, the only way the entire circuit can be described is as a summation of all the nodal activity. Saber, in contrast, finds and applies a set of equations which best describes the activity of the circuit as a whole. The result is much shorter computer run times than Spice, much more utility in simulating large circuit blocks such as ASICs and much more success in pairing digital with analog activity in a mixed-signal simulation.

A problem for Saber has been the process of generating behavioral models, which has you working in a high-level, C-like language—something of a "stretch" for most analog designers. The DesignStar compiler practically eliminates this problem by giving you a graphical front end in which you can enter transfer functions, circuit parameters and other data. The model is then automatically generated.

It's here that the entire analog design process comes to a crossroads. Up to now, the analog designer has worked with very *physical* things—resistors, capacitors, transistors, and op amps. Whether you breadboard or simulate, the process is the same. You select components, wire them up and see how they work together. With behavioral modeling, you're looking at a level of abstraction that digital designers are just starting to get comfortable with. Like the digital designer working in VHDL, you must deal with modeling a circuit function which has no physical analog.

High-level hardware description languages (HDLs) such as Cadence's Verilog and VHDL make it possible to describe a digital circuit without regarding how it's implemented. Since digital behavior is described in 1s and 0s and clock cycles, in principle it's possible to describe a digital system that's totally independent of the implementation technology. The same description can apply to a highly integrated CMOS ASIC, or a board full of 7400-series logic. A behavioral-level analog modeling language such as Analogy's Mast—the C-like language utilized to build Saber models—or an analog equivalent of VHDL will make it possible to describe an analog or mixed-signal system without reference to the components in the circuit.

This is new territory for analog engineers, who've typically been more closely tied to structural descriptions than digital designers. The stage is set, in fact, for "analog emulation technology," the ability to implement analog functions with largely digital means.

But this is the point at which traditional analog designers begin to balk. "You can use a million transistors on a chip to beat a problem into submission," says Jim Williams, "as opposed to thinking 'what is the problem?' and 'how do you solve it?' " With design modularity (the by-product of high-level design methodologies), says Williams, "elegance in design is no longer the primary goal."

Implementing analog filters

An extraordinary contrast between traditional analog and the newer CAE-driven design styles can be seen in the means of implementing analog signal filters. A reasonable analog filter can be implemented cheaply with a fistful of resistors, capacitors and op amps. Though the filter functions will never be very steep, a clever analog designer can make the system work as well as it needs to. A digital signal processor, in contrast, will provide a much steeper, much more precise filter function than almost any combination of analog parts. The DSP solution, however, is typically more costly in money, silicon and programming time.

There's a new CAE tool which dramatically closes the gap between these differing design styles. The Sproclab development system from Star Semiconductor (Warren, NJ) offers a graphical, easy-to-use environment for specifying filter functions. You can specify filter parameters on a menu on a PC screen and visualize the actual waveform it will create. You can then use the software to compile code for a specially-developed DSP chip—the Sprocchip. The development system will automatically download the developed code directly to the Sprocchip.

The breakthrough for analog designers here is in the pairing of easy-to-use tools with specific hardware. No matter what level of abstraction you choose to work at, you always have a structure element that will reliably implement your design.

I suspect that analog design tools which remain close to circuit structure—for example, schematic entry packages integrated with Spice-based simulators—will be more popular in the near term than tools which approach analog design from a behavioral-level perspective. These behavioral-level tools, however, will increase in popularity as designers take on more digitally-based mixed-signal ASIC projects and recognize the utility of describing large circuit blocks with a high-level language construct. We'll also see a greater proliferation of analog emulation techniques, and a gradual "changing of the guard." Dave Fullagar, vice-president of R&D for Maxim Integrated Products (Sunnyvale, CA), couldn't disagree more. "Tools may be the 'wave of the future,' " he says, "but they can't replace 10 years of design experience—the novice user still gets ground loops."

Stephan Ohr is president of Indian Forest Research, and publisher/editor of the monthly newsletter, Mixed Signals.

INTERNATIONAL DESIGN ENGINEERING & ASIC EXPOSITION 92

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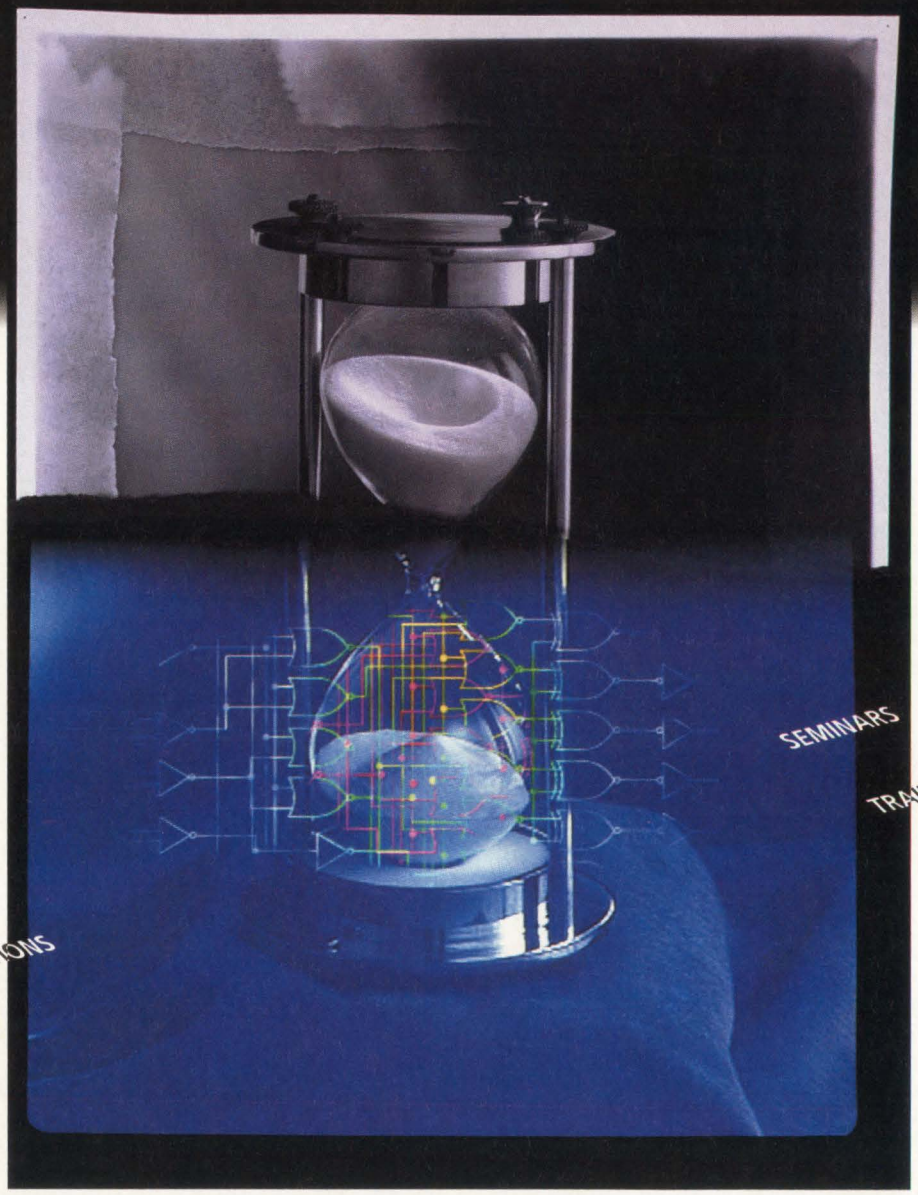

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Specialized PLD and FPGA tools

When designing with programmable logic devices (PLDs) and field-programmable gate arrays (FPGAs), you basically have two choices. You can go with a development environment from a third-party vendor or obtain proprietary development systems from the manufacturer of the specific parts you want to use. Both choices have merits and drawbacks.

There was a time when all PLDs were provided by a few companies. They were fusible link, bipolar and sum-of-products parts which transformed Boolean source files into JEDEC fusemaps for programming. Today, hundreds of different parts are available from dozens of manufacturers, and the technology has moved from bipolar to CMOS, BiCMOS, ECL, and GaAs. Also of importance now is the fact that fusible-link one-time programmable parts have been joined by EEPROM and flash parts, as well as fusing-link and RAM-based programming technologies.

Most important, though, is the fact that modern PLDs include many proprietary architectures for multilevel logic implementations and encompass more recent FPGA characteristics. FPGA architectures vary more, and making the right choice can set the tone for the entire project.

Know it all

If you didn't have to perform any other tasks, it might be possible to know in detail the architectures, quirks and subtleties of every part. But no one today can be expected to know every part in any sort of depth. That's why it's important to make the proper choice when selecting design automation tools for PLD and FPGA devices.

Third-party vendors are useful because they don't limit you to a specific manufacturer's parts. Generic logic can be designed and captured in various formats, such as schematic capture, Boolean language, truth tables, state machine syntax, VHDL, and even waveform capture. This is beneficial in that different designs lend themselves to different design input techniques. A decoder may be simpler to enter in truth table format, for example, while a sequencer may lend itself to state machine or even schematic entry. This is also often a matter of preference and different designers will choose different input formats, even for the same design.

With third-party support tools it's also important that you need to master only one software. When designing with various chips from different manufacturers, a third-party tool will let you design within a single environment, rather that having to obtain, load, configure, learn, and run each company's proprietary tool. Instead of having to load and run a program, and then exit it and repeat the sequence with a different program, with one program run you can load, compile and save one design, then load, compile and save another one. While it may seem to be a trivial benefit that the operational aspects of running a program as well as the specific syntaxes of source files are uniform in format, in practice it's not.

Doing it "their" way

Almost every program, third-party as well as proprietary, has a slightly different syntax and notation format for Boolean input. One may require a slash (/) to indicate the NOT value for a signal, while another may require an asterisk (*) and still another may call for an exclamation point (!). One may require a semicolon at the end of each line, and another may have the line end with just a carriage return.

When moving from tool to tool, it's easy to inadvertently use the wrong syntax, and so waste time going through the text editing and compiling tasks several times. This situation holds true for commonly supported input techniques such as Boolean and truth table formats, as well as for a tool's proprietary formats, such as state machine and high-level language support.

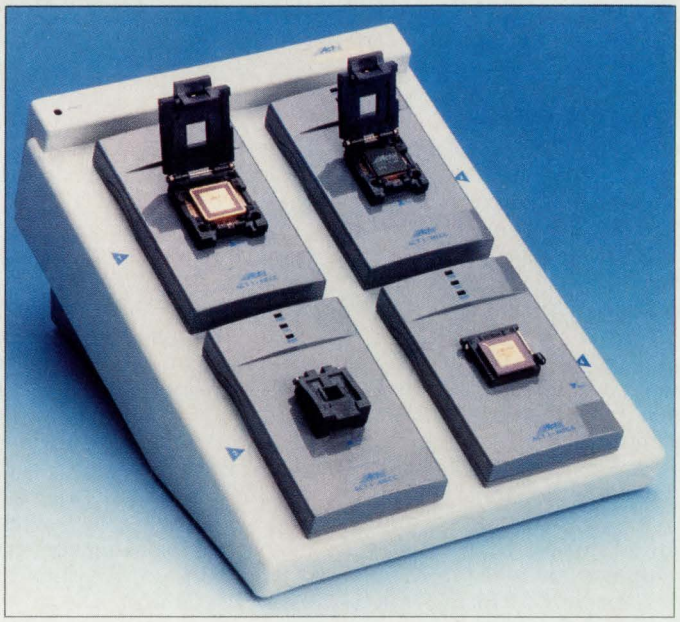
A great benefit of third-party PLD and FPGA design systems is the ability they give you to aim at devices you want to implement the design in and the way they let you make software recommendations. Many of today's third-party PLD and FPGA design programs provide automated or semi-automated device selection and even device partitioning. This relieves you

of the burden of having to be intimately familiar with every part's architecture, characteristics, quirks, and subtleties. What's more, more recent third-party software even lets you input weighted criteria for automated device selection, permitting the software to find the cheapest, or fastest, or smallest, or lowest power (or any combination of the above) solution to specific design requirements.

Does flexibility offset price?

While third-party PLD and FPGA packages can cost $5,000 or more for PC platforms, they tend to provide a flexible environment in which to experiment with "what-if" scenarios, so you can arrive at the optimum choice of parts for a given design. In addition, the ability to partition a design into chip sets further enhances flexibility, since smaller and cheaper parts can be used where PC board space isn't a design criterion.

But not everyone needs a general-purpose program for PLD and FPGA design. Many times a company focuses on one or two device manufacturer's parts, when a broad product line can satisfy all its PLD and FPGA requirements. In this case, the need to support other manufacturer's parts is eliminated and may even be undesirable.



The Actel FPGA utilizes a fusing-link technology to achieve highly dense parts. A dedicated programmer is available through Actel as part of its development system.

For those of you who aren't limited to a few manufacturer's parts, third-party tools may fall short in another area. In many such cases the device manufacturer is the only source for immediate support of a newly introduced part. Third-party tools may lag behind device manufacturers by several months when it comes to supporting new devices. Also, nobody knows the architecture of a part better than the device manufacturer.

This means that the device manufacturer's software will almost always do a better job of allocating internal device resources than will a third-party tool. This is especially true of FPGAs, whose architectures are so specific and variable that it's nearly impossible for an independent third-party company to intimately know every part.

Device fitters supplied by device manufacturers to third-party software vendors are starting to alleviate this problem. Still a rather new arrangement, when it matures it could mean that third-party tools can be as responsive to new parts as the manufacturer's own tools. Until then, the manufacturer's tools are still the only way to get immediate and comprehensive support for the latest parts.

Captive on the move

Traditionally, device manufacturers have provided low-cost—or even free—software to aid both novice and experienced PLD designers with design transformation into JEDEC code for device programmers. This proprietary software can only be used to design with the parent company's parts, even though in most cases it includes translators that convert other companies' designs into its format.

While many manufacturers still offer low-cost software for this purpose, the trend has been toward more expensive, but still proprietary, software. The days of free software haven't quite come to an end, but cutting-edge designers who want to take advantage of the latest parts may now have to pay for proprietary development systems from device manufacturers that are as, or even more, expensive than good general-purpose third-party PLD and FPGA development systems.

On the surface, this may seem like a disincentive for designers to use a specific company's parts. You will find, however, that device manufacturers' software has grown from simple Boolean translators to full-blown and comprehensive design environments for design capture, optimization, reduction, factoring, functional simulation, timing verification, test pattern generation, fault analysis, programming interface, and hard copy documentation support.

In addition, many of today's newer FPGAs can't be programmed on standard device programmers. Either there are too many pins or you just don't have the flexibility to tackle the specific algorithms needed to program the part. As a result, many of the device manufacturers' proprietary development systems include a dedicated programmer and interface to your computer, driving the price even higher for these narrow, but powerful, solutions.

A related issue is the expense of the PC. It used to be that a bare-bones PC could easily handle PLD designs. Now many programs, both third-party and proprietary, require 386- and 486-based machines with large hard drives, deep memory (4 to 16 Mbytes), VGA displays, mouse, printer, serial and parallel

ports, and even specific operating environments such as Windows. On top of that, you may be required to obtain other third-party software for schematic capture and netlist generation. This can add another $1,000 to $5,000 to the cost of obtaining and using these superparts.

And, as if this wasn't enough, third-party debug aids such as emulators and debuggers are often recommended, even when using a company's proprietary tool. These aids come in very handy when initially testing your design. Some advanced parts are one-time-programmable, meaning that every design and test iteration could cost $100 or so. If many designs are planned, an emulator could pay for itself, especially if a brute-force engineer is doing the design.

The full spectrum

In the world of PLD and FPGA development systems from device manufacturers, the entire spectrum is covered. Free and low-cost software is still available from most manufacturers, but it generally supports small devices only, such as sum-of-product architectured parts. This software is intended to work well with various third-party programmers, and is generally limited to equation-based input with limited simulation (if any).

Large parts and proprietary FPGA architectures require more costly development hardware and software, but these tools are now as streamlined and efficient to operate as any third-party development package. Most companies offer a comprehensive design environment, with schematic, equation, high-level language, and even waveform support. In addition, better simulators are coming with these more costly development systems.

What's really nice is that modern proprietary development software is now fully integrating with popular third-party tools. Within a single design environment, engineers can use preferred schematic capture programs, text editors and other user-defined tools and utilities that can integrate into the environment rather that run from outside it. This can dramatically improve throughput and reduce human-introduced errors such as file I/O and program invocation switches.

Jon Gabay is a freelance editor with extensive design experience. He has written for all of the specialized CAE/CAD publications at one time or another, including High Performance Systems, Engineering Workstations *and, most recently,* Design Automation.

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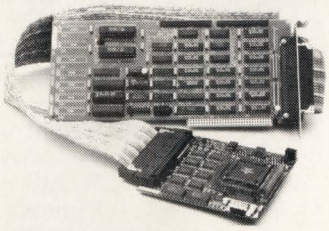

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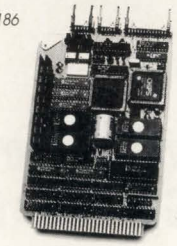

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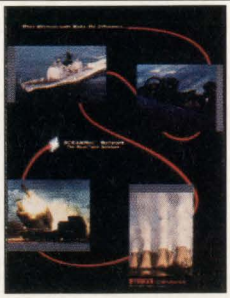

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Connor-Winfield Corp. announces literature on a new line of high frequency ECL Logic clock oscillators. The ECLB Series oscillator covers the high frequency range of 8 MHz-360 MHz. AVAILABLE NOW IN A 14-PIN DIP. Literature for a double DIP version with frequencies to 500 MHz is also available. Frequencies to 90 MHz are now available with Voltage Control function (model EV53 series). Contact Barney Ill for details.

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Package	:	14-pin DIP
Frequency	:	8 MHz to 360 MHz
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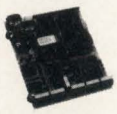

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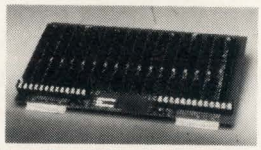

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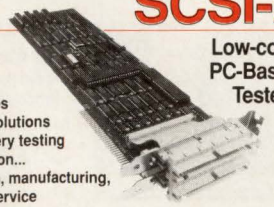

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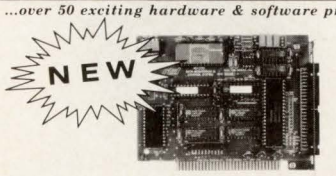

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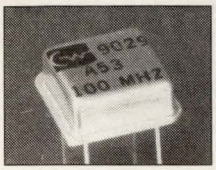

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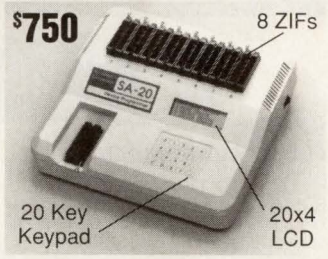

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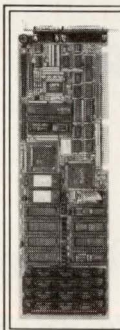

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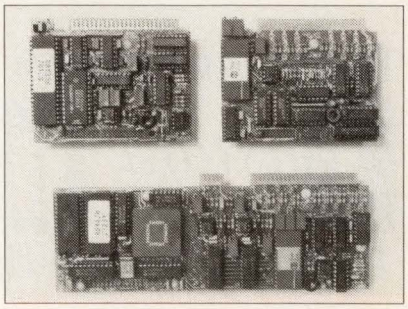

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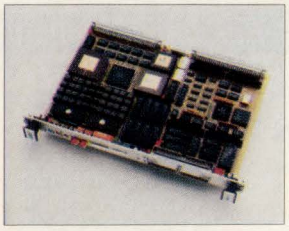

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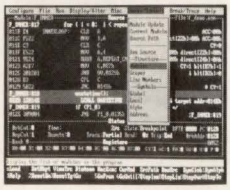

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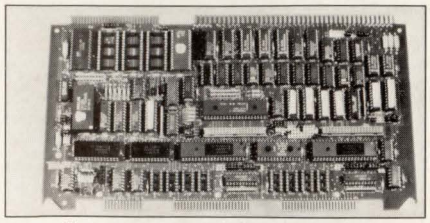

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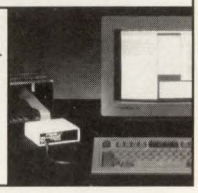

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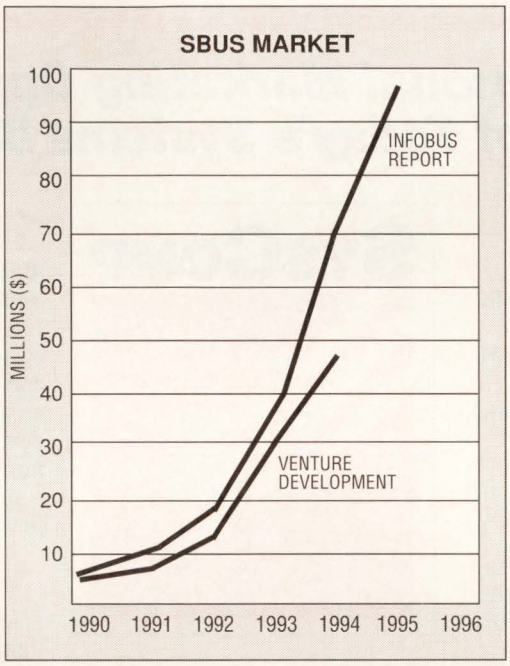

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CIRCLE NO. 92

Call for Papers

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SysComp International is an intensive 3-day systems-oriented conference and exhibition, providing an opportunity for presentations on a wide variety of OEM system and subsystem topics in both hardware and software. **SysComp International** is intended to bridge the information gap between passive/discrete component shows such as Wescon, and VAR/VAD/end-user exhibitions such as Comdex. The applications-oriented, **SysComp International** Technical Program is targeted at hardware and software designers, and OEM integrators, working in a variety of industries—military and avionics, computer/computer peripherals, industrial control, robotics and automation, and consumer electronics.

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Acceptance of proposed presentations will be made by May 1, 1992. A complete copy of the presentation, including all visuals and graphics, will be required no later than **September 1, 1992**.

For more information, or to submit a proposal, contact:

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CIRCLE NO. 89

LETTERS, COVERS & OTHER DIVERSIONS

What happened? When we started our Cryptic Cover Contest back in December, we received more than a hundred responses deciphering the rebus writing on the cover. January's cover, on the other hand, generated only a handful of responses. Perhaps the rebus writing was easier for readers to get their teeth into than the subtleties in our multimedia cover. In any case, here's what we were thinking about. The big guy on the right in the blue trunks is Big Blue, or IBM, being ganged up on by Microsoft—with all the $$$—and DEC—in the person of Ken Olsen (topped with a pilgrim's hat). The wrestler in pink represents Apple and is in pink because Pink is the name of the new operating system from the Apple/IBM joint venture. Note also the blue and white touches on Pink's tights. Sun is, of course, represented by the high-flying wrestler and Hewlett-Packard by the wrestler just entering the fray.

Here is my interpretation of your January cover: Sun is flying high while HP is on the ropes. Microsoft is claiming a victory and Big Blue (IBM) is watching as it's a turkey shoot for the bucks in the multimedia contest. Please keep the puzzles coming.

Cris Drakiotes
CR Bard USCI Division
Fitswilliam, NH

Like the cover! Big Blue bullying Apple and Microsoft, HP entering the ring, Sun above our heads but maybe not for long. And someone gleefully wearing pink. I didn't get that one but I'm looking forward to your next issue so I can find out. Liked the editorial. Applies all over North America.

James Partanen
Resource Manager
Matheson Communications
Waterloo, Ont, Canada

Excellent article on multimedia standards.

Ralph Merrill
Department Chairman
Utah Valley College
Orem, UT

I'm not sure what the deadline for your rebus writing contest is but I just picked up the December issue today. Your editorial was very interesting. Subconciously, I knew your magazine had a different feel to it but I had never conciously thought about what that difference was. I feel there is a need for both types of magazines and I am glad that Computer Design is there to fill the need for a *technology* magazine.

Ross A. Osborn
Naval Air Development Center
Warminster, PA

As I read your editorial in the Janaury issue, an article in the morning paper kept running through my mind. I am enclosing a copy of the article. The big U.S. companies are downsizing in the U.S., but are expanding elsewhere. It seems as if they are purposely trying to reduce the standard of living in the U.S.

K.E. Davies
San Diego, CA

Thanks for the clipping. The article was entitled "Free-trade follies" and here's what it said:

"The 'Big Three' U.S. automakers all announced a bad year during 1991. But General Motors, Ford and Chrysler all say they boosted production at their Mexican plants, hiring extra Mexican help, and have increased exports to the United States....Just last month, GM announced it would close 21 U.S. plants and eliminate some 74,000 U.S. jobs. On January 15, GM announced it will begin making trucks in communist China. Apparently, Chairman Robert Stempel thinks that what's good for GM is good for Red China."

It's remarkable how much political claptrap starts with claims like, "We need someone to stop the political claptrap," as in your January editorial. Your observation that there are fewer American products for sale every Christmas is probably true, but to leap from that to advocating more government involvement in research, use of more taxpayer money on a failed "educational" system, unilateral disarmament, and protectionism is an astonishing transition. Has it escaped your notice that, for example, the military (which accounts for only a fourth of our federal budget and uses at least some of its money to produce American-made products) is the only part of governemnt whose budget allocation actually has been cut in the last half century?

You imply that more vigorous action on the part of government is in order. Yet, for fifty years our governments have gotten steadily more powerful and intrusive in the marketplace. The result, in your own words, has been a loss of "the kind of jobs that count most." One sign of insanity is to repeat actions, expecting different results.

We do *not* need "leadership" who will "get down to business" of further intrusion in the operations of American industries, or of disarming us. We *do* need governemt at all levels to stop interfering in the marketplace; to release us from the burden of government gone wild; to *leave us alone* to do business!

Chuck Kriel, Ph.D.
Boeing
Wichita, KS

THIS MONTH'S COVER: *This month's cover should be a breeze. The Special Report is about debugging 32-bit processors, so what could be more appropriate than bugs on the cover. There are several bugs represented in the illustration and the contest is to properly identify the specific bugs. There also are a couple of other ideas, as well as a specific product, represented in the illustration. Happy hunting.*

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NOVEMBER Wescon, Autofact	• Designing for testability	• Mezzanine bus strategies • Advances in datacom ICs	• Emulators	• Robotics and automation	
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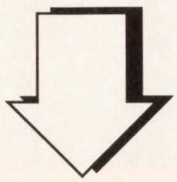

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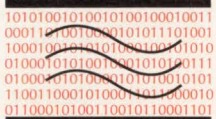

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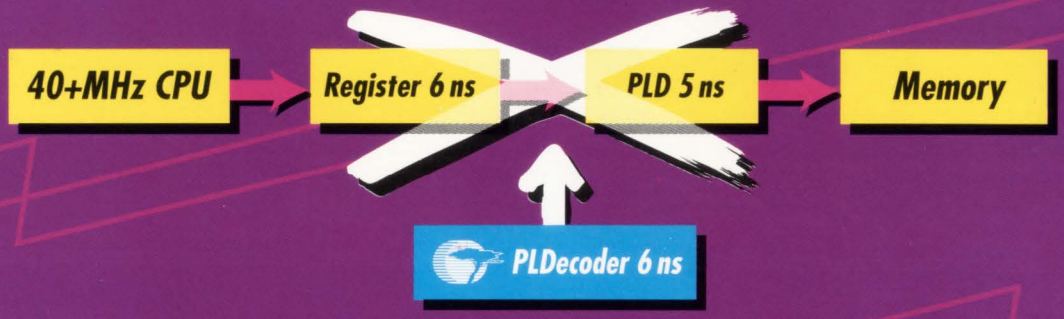

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