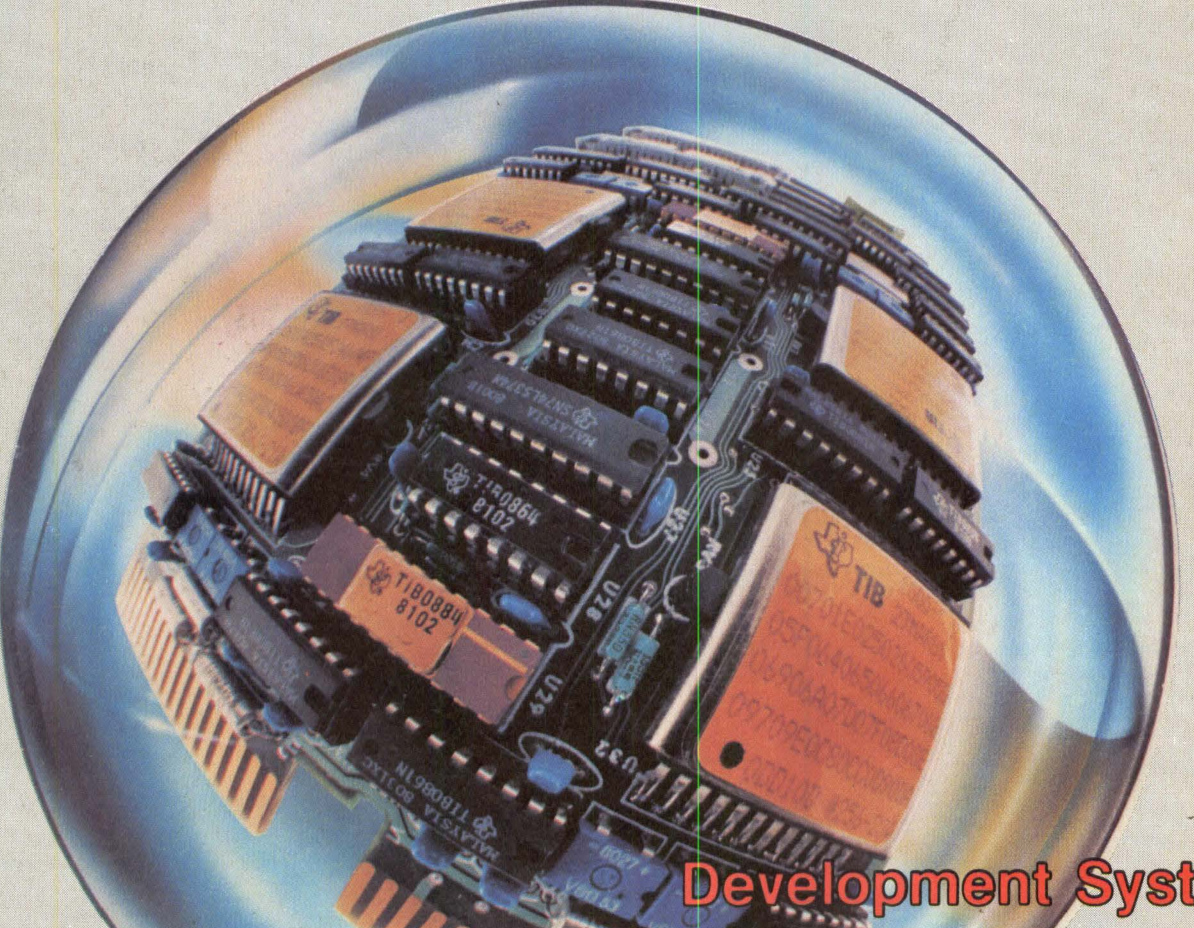
VOLUME 11, NO. 6 JUNE 1981

Digital Design

Computers • Peripherals • Systems

Bubble Memory Storage



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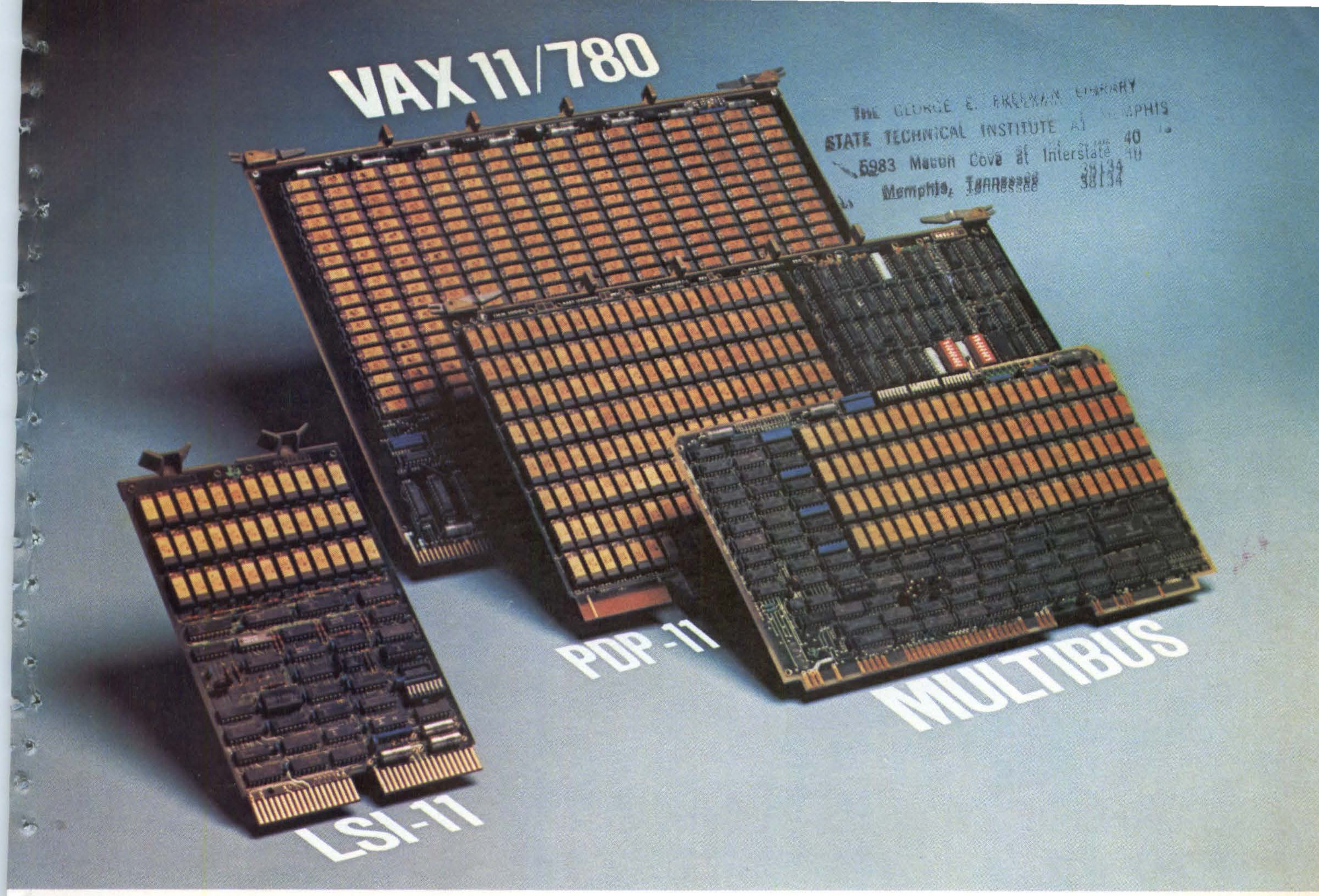

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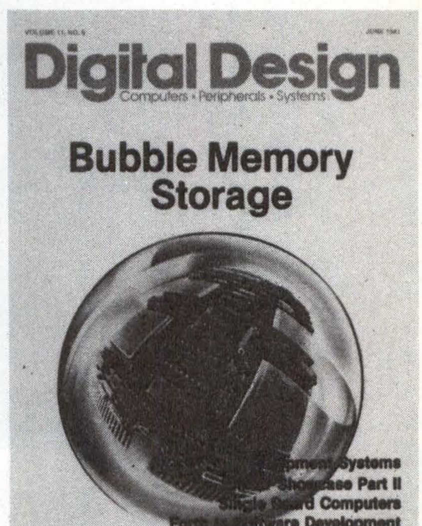
Departments



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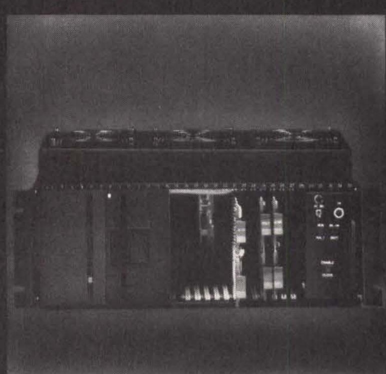

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Letters

printer controllers

Dear Editor:

The article "Printer Controllers: How to Choose Them" (March 1981) claims "The RS-232C is generally good for up to 50′," which is incorrect. A properly-designed cable will allow standard RS-232C transmission over far greater distances. At 9600 baud, for example, 500′ should be quite practicable. We have designed (under subcontract to Butler Computer) such cables to run through electrical utility ducts (an electrically-noisy environment) from the 7th to the 21st floors of the Eaton Centre in Toronto. They are over 350′ long and to the best of my knowledge have been running at 9600 baud five days a week for over three years now, without a single transmission error.

As for serial interfaces with buffer-ready monitor circuits, our standard CASLIs (Character-Asynchronous Serial Line Interfaces) have that feature.

Terry Rowe
MIRA Electronics Ltd.,
Microcomputer Systems Div.,
Box 2145, Station B
Scarborough, Ontario
Canada M1N 2E5

not a monopoly

Dear Editor:

As a foreign engineer in US industry, I am surprised at letters directed against aliens. They are unaware that technology and intelligence are not US monopolies. Immigrants come to the US in search of a better life, and most work for it. US engineers who seek guaranteed job security and salary are looking for handouts.

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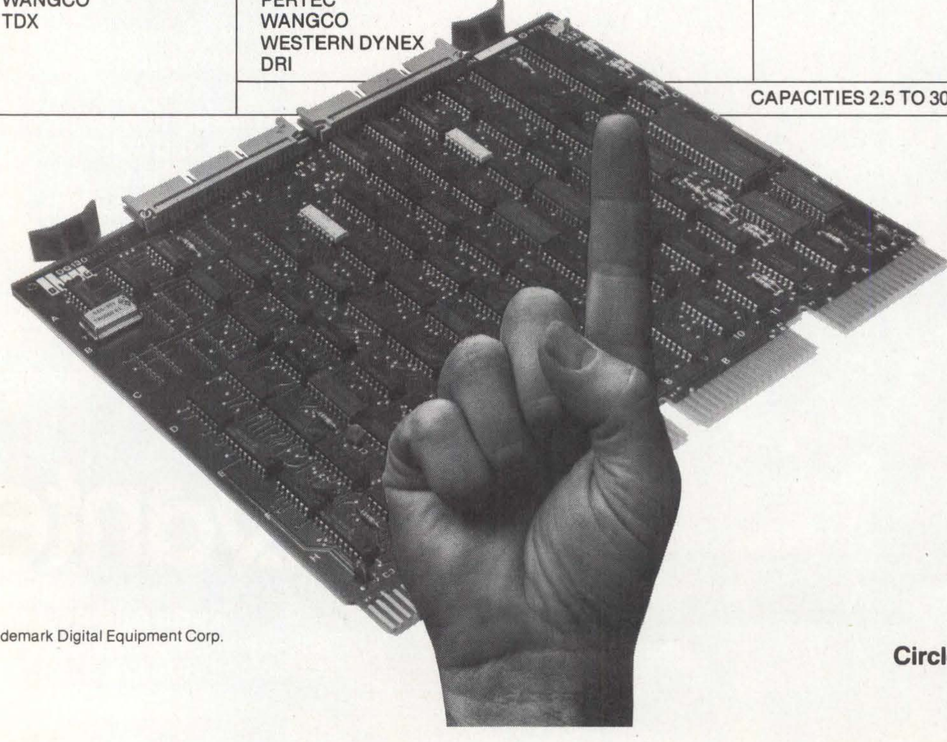

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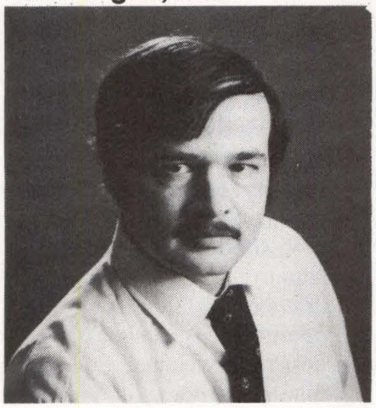
Speakout

Keys To Quality

Paul Snigier, *Editor*



Japan, offering rock and salt water (neither highly marketable), was forced in the 1960s and 1970s to go after high value-added products — cameras, autos, tankers, motorbikes, TVs and transistor radios. In the 1970s, with price escalations and shortages striking raw materials and fuel, Japan recognized this long-term trend would hurt Japan. With an astute understanding of market share, and able to await long-term payoffs, Japan prepared for a major transition to semiconductors and computers. For Japan, success in computers is vital: failure to successfully establish and maintain a sizeable market share will lead to the ultimate demise of Japan as a commercial power. Survival is a strong motivator.

Why does Japan succeed? Much has been written about Japanese quality, their "Quality Circles," tariffs, worker loyalty, lack of unions, benevolent corporate attitude to workers, tariffs, etc. Although these are factors, they are only portions of the overall picture. It is the Japanese approach that accounts for their success. Too little is written about it.

In a 1973 book, "Management: Tasks, Responsibilities, Practices" (Harper & Row), Peter Drucker described how these quality assurance and other tactics fitted into a far bigger picture or strategy. Success lies in the way the Japanese make decisions.

According to Drucker, no nation on earth has a standardized approach to decision making — except the Japanese, resulting in very effective decisions. American managers can't understand how the Japanese approach can reach any decision, never mind an effective one (much like the bumble bee which, according to laws of aerodynamics, cannot fly). But the Japanese success, claims Drucker, is proof of how wrong we are. Drucker, who studied the Japanese versus American approaches, discovered some interesting things.

Most Americans cannot understand how a Japanese executive can be so adamantly opposed to a major decision, and three years later will enthusiastically support it. It makes sense only when we understand that "making decisions" are different things to Americans and Japanese. We emphasize "the answer" to a question, and all our management decision-making books offer systematic aproaches to getting an answer. But, to the Japanese, "defining or understanding the question" is the key to decision-making. They begin by first deciding if there is a need for a decision and what the decision is all about. No discussion is made of what the answer might be! Thus, people are not forced to hurt egos and take sides, and creativity-killing rudeness is avoided. Creativity is encouraged, put-downs are discouraged, and there is less one-upsmanship. They discover what the decision will be about, not what it should be. This step takes time, frustrating Americans, who feel they're getting the runaround. Every month new groups come to start (it seems) "negotiations" anew, with each new group knowing zero. (This means the Japanese are taking things seriously.) Endless discussions go on. They involve people who will eventually carry out the agreement process, and it becomes clear what approaches each group will take.

It is finally referred to the "appropriate (high-level) people" for a decision. Since everyone was sold before the decision, the answer surprises no one. Now, things move very fast — too fast for the American partners, who are left gasping at the speed and who cannot provide the information and decisions in time. The Japanese — who understand American management as little as we do theirs — complain bitterly about American incompetance and procrastination. For the Japanese, no time is wasted politicking and "selling" the decision (and avoiding sabotage and sandbagging).

The Japanese would not even begin by discussing a proposal for a joint venture from a U.S. firm. In one such case Drucker investigated, the Japanese began with the question: "Should we change our firm's direction?" After much discussion, they agreed, then decided to get out of older businesses and start new ones (the joint U.S venture was to fit in with this new strategy). Until the concensus for change was made, not once did they (even privately) discuss the joint venture or its terms! But here in the U.S., task forces and long-range planning groups come up with recommendations and commit themselves to one alternative. They choose an answer, then document it. Japanese do not commit themselves to a recommendation until they've fully defined the question, examined all alternatives and arrived at a consensus. They are less likely to become prisoners of preconceived answers. Opinions are encouraged, and face-saving encourages a more honest examination of alternatives. The American approach forces antagonisms and aggression, and supresses creativity. The Japanese approach,

Speakout

ironically, and unknown to the Japanese, incorporates certain qualities of different management creative thinking techniques pioneered by ADL, Bill Gordon, Synectics and others.

Creative thinking (CT) techniques used in management meetings minimize the ego defense mechanisms of participants. Unlike most meetings run in the U.S. (which become CT-killing environments), CT techniques are carefully designed to minimize or avoid grandstanding, defense of one's ideas (simply because they're yours), one-upsmanship, put-downs (no matter how subtle), ego clashes and win-lose situations. By its nature, American industry fosters a subtle disrespect for others' ideas, power plays, unwillingness to take chances, domineering, premature jumping at the most obvious solutions, and general confusion.

America is not improving the productivity of its decision-making process; in fact, American industry's decision-making capability is worsening. It's certainly no secret that American management techniques and U.S. executives are not as well-respected overseas or sought after, like a decade ago. And now, the situation is worsening, and our response is to copycat Japanese "Quality Circles."

Can we tailor the Japanese methods to American behavior? Or will such a plan fail, as suggested by many Japanese experts familiar with both cultures? They suggest that the American worker, with his aggressive lack of respect for fellow workers, and mutual lack of loyalty between him and his firm, can never truly adapt the Japanese approach. If significantly modified, however, could it then help us? Many firms now claim they're adopting such holistic approaches to quality assurance (it's also good for P.R. and advertising). But when the history books are written in 1995, will the Japanese methods have beaten us? Will grafting or modifying the Japanese way ever achieve the same incredible money-making results for us that it does for the Japanese? Time will tell. But the signs aren't reassuring: already, they've invaded the mainframe and personal computer fields, and are hell-bent on closing the software gap. For the American computer industry, the warning signs are growing. Stormy sailing lies ahead.

"Faraday Solar Generator" Uses Single-Chip Microcomputers

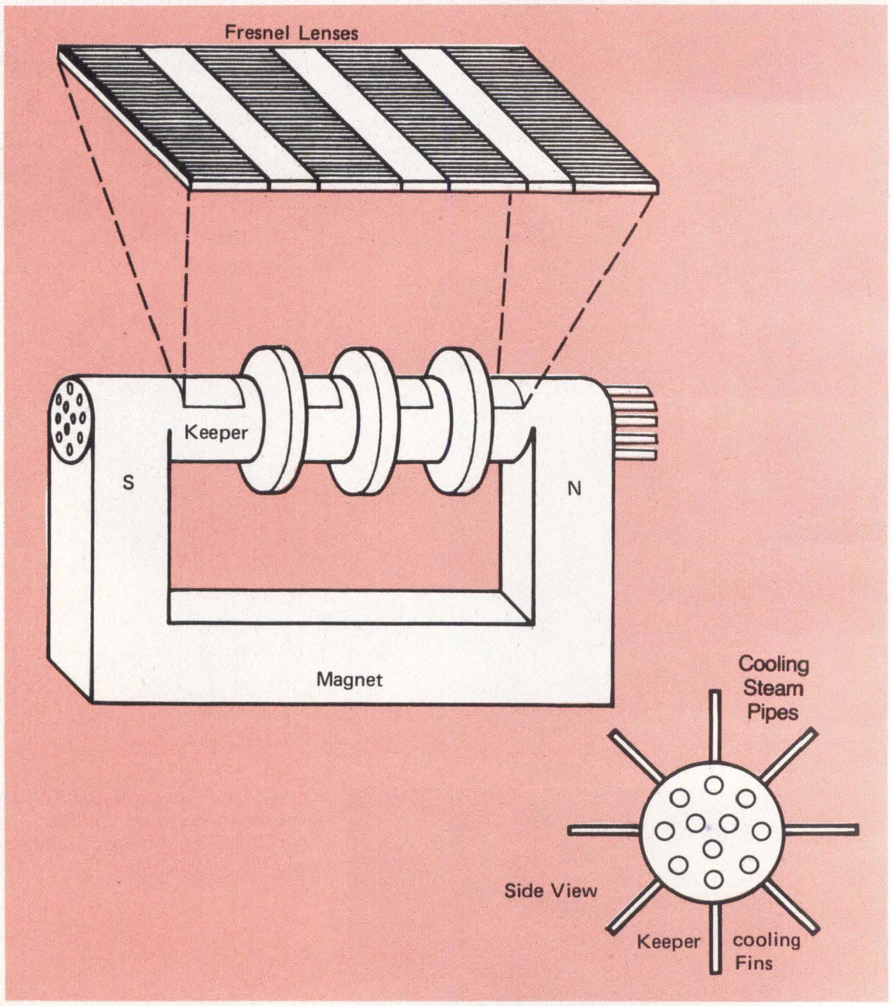
A μC-controlled, solar generator, the "Faraday Solar Generator" (FSG), invented by the author, converts solar energy by focusing solar rays onto an iron "keeper" bar in a magnetic circuit. By turning the solar rays on and off, heated domains in the keeper bar alternately randomize and align, thus creating a magnetic field that alternately moves outward and then collapses, cutting a coil's conductors to induce emf and current flow. Indirect conversion solar converters or Faraday Solar Motors (FSM), also developed, use similar principles.

This thermo-magnetic generator is not limited to solar energy, but could function in a coal-fired unit or nuclear reactor. It is possible that in a nuclear reactor, it would eliminate complexity, improve safety and reduce radioactive waste; conversion from heat to electricity is more direct than many present methods.

based on Faraday's Laws

This solar thermo-magnetic generator (and solar motor) is based on two basic laws: (1) a varying magnetic field induces voltage in a conductor, and (2) magnetic materials such as soft iron lose their capability to conduct a magnetic field when sufficiently heated. If an iron keeper bar (across a horseshoe magnet, for example) is conducting a magnetic field (completing the magnetic circuit), and if a solar collector (such as a Fresnel lens, parabolic mirror, etc.) is focused on the keeper bar, it heats up. Upon reaching about 670°C or so (if soft iron), the magnetic field relocates itself due to the sudden disalignment of the domains; flux lines move outward quickly. When the flux lines cut through a conductor (coil), the lines induce a transient in this nearby coil.

By thermally cycling (heating and slightly cooling) such a magnetic conductor or keeper — which need not be a solid bar (but may be a plasma, gas or fluid) — then a continuous emf pulse train is generated in the coil. When the field collapses again, a transient pulse in the opposite direction is induced. By



Faraday Solar Generator focuses rays to heat soft iron keeper, causing magnetic domain disalignment and rapid outward flux line movement, which cuts coils. Next, steam burst through keeper pipes lowers keeper temperature, causing domain realignment and flux collapse, inducing a negative counter emf pulse. A mechanical or electrosensitive shutter for the Fresnel lenses is not mandatory.

properly phasing a number of these serially and/or parallel-connected solar generators, and adjusting their magnitude, (and with suitable filtering), a system could generate any desired waveform.

geometry: key to efficiency

Efficiency is improved through optical and physical geometries by: (1) rapid application and removal of intense solar heat, (2) more rapid orientation and deorientation of domains (perhaps with improved materials), (3) rapid heating and cooling of the bar(s) and (4) optimum cutting of conductors by collapsing and expanding flux lines.

Application and removal of solar heat may be physical, although this requires mechanical movement, introducing inefficiencies and lowering reliability. Non-mechanical means, chiefly electronic and chemical, involve schemes such as transluscent sheets that become alternately transparent and opaque with minute voltage. In such a case, shutter action need not be a total on-off (i.e., total opaqueness). The keeper's temperature variation need not be great — just enough to randomize and then align the domains and no more.

Rapid bar heating/cooling can be accomplished by optimizing heat sinks, vapor mist cooling, cooling fans, proper shading, thinner bar ("keeper"), etc. For more rapid cooling, a series of pipes could be spaced throughout the iron "keeper" or bar. Vapor or steam passing in bursts through the pipes would lower the temperature briefly for domain alignment.

Waveforms. Since transient surges alternate in both directions, any desired waveshape may be approximated by varying the magnitude and phase of several connected solar energy generators and properly timing SCRs in certain SCR networks. For more complex systems, a μP would provide control. Current and voltage requirements can be met by parallel and/or series connection of the generators.

Or, to prevent impulse waveforms and to smooth out the waveform, one portion of the tube or ring would be thicker. The domains would randomize (or re-orient, if cooling) on the thinner side first and rapidly move to the thicker portion, creating an inherently-longer waveform.

Frequency. Maximum attainable frequency is not known, but I suspect at least 8 to 15 cps is possible. This is variable and depends on incident solar radiation, optical geometry, cooling scheme, physical configuration and other factors. Also, a tradeoff (inverse relationship, but not linear) also occurs between frequency versus flux: the more length in the randomized domain ("gap") that opens, the longer will be the magnetic flux lines and the greater their expanding (and collapsing) movement.

To open up (heat) as much of the bar as possible, a maximum length must be heated quickly, uniformly and simultaneously.

Unfortunately (all other factors being equal), this is at the expense of a lower frequency. An upper limit of the "gap's" length or size is set by several influences, of which unavoidable heat losses (which increase more than linearly) are the most significant limiting factor. "Healing time" (reorientation of the domains) will not be the obstacle; "heating time" becomes the worst obstacle for larger "gaps."

Microcomputer control

A single generator or motor will not need μC control; thermo-magnetic feedback controls are fine. But, for generator banks, magnitude and phasing control become too complex and variable. A μP would monitor variables such as incident solar radiation, temperature in and within the iron and coils, and compare this with statistical data (overcast skies) which would be monitored continuously. Other tasks include firing of SCR networks for magnitude and phase control of the output waveform(s), control of cooling cycle time, and rate at which coolant (steam) is shot through pipes in the "keeper," thus optimizing the opening and closing of the magnetic circuit and maximizing the movement of flux lines through the coils. It must detect and compensate for sudden or gradual system characteristic changes due to material degradation or aging, load changes, and other parameter variations.

Numerous control tasks involved, it seems, might lend itself to shared (and independently operating) multiprocessors, with shared architectures, such as National's new COP 2440 4-bit μC family. The 2440 avoids slow system throughput, interprocessor data transfers and complex task scheduling. It offers parallel processing with direct memory accessing (per processor) and saves memory. Processors intercommunicate via common memory. They share clocks and internal buses; instruction decode, steering and gating, and arithmetic logic. Status registers are separate. Each processor accesses I/O and common memory, and alternately fetches PC-addressed instructions.

Faraday solar motors

Direct conversion linear and reciprocating "Faraday Solar Motors," also invented by the author, use Faraday's laws. Potential energy is alternately stored in a spring (either in compression and/or tension — but probably in tension), in raising a weight (in the form of a roller on an incline or vertical weight), compressed air, flywheel, etc. For example, a soft-iron "bar" (connected to a spring, weight or other potential energy storage device) cools and the magnet pulls the bar or keeper in, converting kinetic to potential energy. Movement need not be restricted to solid iron keepers; certain liquids or gases can be moved directly, although with lowered efficiency.

Different configurations exist; here is one I constructed. Gravity pulls a horizontal lever down. Next, the keeper (attached to the lever) cools; the magnet pulls the soft-iron keeper up, closing the magnetic circuit (directly into the path of the focal point of a Fresnel lens), thus heating the keeper and randomizing the keeper domains. This breaks the magnetic circuit, causing the lever to fall down (and out of the focal point), whereupon it cools and the cycle repeats.

Rotary-motion Faraday Solar Motors would have magnetic "poles" that "switch" on and off when thermally cycled by coming out of and into the shadow(s) of solar "shields." No "shutter" is needed, creating a simpler design than the linear motor. RPM would be depressingly low, and a flywheel to develop angular momentum would be needed in most applications.

Impracticality and low reliability rule out most potential energy storage systems (such as springs). This may be circumvented by push-pull action, with two linear Faraday Solar Motors linked in opposition; they are alternately active and passive. Or, several linear-action motors could be connected to a crankshaft, eliminating the need for a potential-energy storage mechanism.

Key to a linear action solar motor, as with rotary motion, is the feedback servomechanism. This may include, but is not limited to, a shutter control of the Fresnel (or other) focusing device.

efficiency

Semiconductor solar cells should prove cheaper for most applications than my

Technology Trends

Faraday Solar Generator; which, in turn, is more efficient than the Faraday Solar Motor. Finally, rotary-action Faraday Solar Motors provide greater inherent efficiencies than rotary solar motors. Whether Faraday Solar Motors are practical, remains to be seen.

Paul Snigier, *Editor*

Magnetic Field Controls Optical Shutters

Anatoli Larkin, Corresponding Member of the USSR Academy of Sciences, Edward Nagayev, Doctor of Science (Physics and Mathematics), and David Khmelnitsky, Candidate of Science (Physics and Mathematics), have discovered the phenomenon of heterophase autolocalization of conductivity electrons in semiconductors. This discovery, confirmed by Swiss and U.S. researchers, makes possible new instruments. In some instruments, magnetic properties can be controlled with electrical fields and illumination; in others, optical and electrical properties with magnetic fields and varying temperature. It is possible to design optical shutters to let through or stop light beams of certain frequencies and open or close them by weak magnetic fields.

"Electrons are usually evenly distributed in the crystal," says Prof. Edward Nagayev. "But it is not always so. In magnetic and ferroelectric semiconductors, electrons group into clusters in certain regions of the crystal under certain conditions, and form a kind of drop scattered throughout the crystal. It is significant, for properties of crystals inside the drops differ from those outside the drops."

In-between the drops lies electron-free space. In that case, the crystal is incapable of conducting electric current and becomes an insulator. But it regains conductivity once these drops are destroyed or increased in size until they contact each other and their number increases.

Remote Terminals

England. US electronic firms are currently being wooed to England through a lucrative program of government grants and financial incentives to open manufacturing operations in the County of Merseyside which also includes the port city of Liverpool. The area where the Mersey River empties into the Irish Sea is located in the northwestern portion of the country. Merseyside is the heart of a home market of about 57 million people and a reachable European market of some 360 million. Low land and labor costs, plus good transport facilities (by land and sea) have helped attract present industry to Merseyside. The official incentives being offered to US firms (and others): 1) Special government grants up to 22% of new manufacturing investment. 2) A 100% capital allowance to any firm investing more than $12,200 in buildings and more than $1,200 in each new machine. 3) Factories can be purchased over a period of 15 years at a fixed rate of interest. 4) If rented, factory-sites can be obtained up to two years rent free. 5) Grants of $45 per week for each new employee for up to 26 weeks. (Available only to smaller firms employing less than 200 people.) 6) Tax allowances to help write off cost of capital expenditures. 7) Additional central Government Grants available to offset some of the costs of plants, machinery and buildings. Another advantage offered prospective companies is lower wages in the area. A 1978 international table showed the following dollars-per-hour wage scale: UK, $3.47; France, $4.48; Japan, $4.66; USA, $6.58; Germany FR, $6.71. Contact US reps Thomas H. Miner & Associates, Inc., 135 South La Salle Street, Chicago, IL 60603 . . . . **Germany.** November 4 to 6 1981 are the dates in Cologne for the International Trade Exhibition for Telecommunications. "You need to be at the fair," say the organizers, "to meet face-to-face the potential users from industry, administration and science and win them as customers." Interested? Write to Erwin Schafer, Messe-und Ausstellungs, Ges. m.b.H. Koln, Postfach 21 07 60. D-5000 Koln 21 . . . . **Canada.** National Semiconductors Ltd., in Montreal, (no connection with National Semiconductor Corp in the U.S.) is changing its name to Silonex, Inc. The Canadian company makes optoelectronic components . . . . **Sweden.** Facit Data Products Co., of Stockholm, has signed an agreement with Computervision Corp., to deliver paper tape equipment for the European CAD/CAM market . . . . **Ireland.** PC-board production is so good in Northern Ireland that manufacturers are expanding their plants. Latest to announce is Andus Electronics which is now building its second factory here. Andus Electronics had its origins in West Berlin . . . . **Denmark.** Handelsbanken in Copenhagen is installing $2 million worth of Racal Milgo data communications equipment. New modems will link branches to main office. The modems will operate at 9600 baud. The previous link operated at a 4800 baud rate . . . . **Japan.** This country's exports to the US are declining. Latest figures show that in Oct. 1980, the value of shipments was 12% lower than in the month of September. The October value was about $23 million. In November, 1980, the value again fell to $20 million . . . . **Switzerland.** "Telecom 83" is the fourth in a series of quadrennial World Telecommunications Exhibits. (Oct. 26-Nov. 1, 1983, in Geneva.) Purpose of the exhibits: keep telecommunications administrations, companies, organizations and the entire telecommunications industry informed on the latest advances in telecommunications techniques. Contact: Telecom 83, International Telecommunication Union, Place des Nations, CH-1211 Geneva 20, Switzerland . . . . **Republic of China.** The Tatung Company of Taiwan is buying Decca Radio Co., a division of Racal Electronics, Ltd. The selling price is $2.25 million . . . . **The Netherlands.** N V Phillips Co., of Eindhoven, has unveiled a new stepper motor. Other stepper motors, says the company, offer ony a limited range of step angles (because of the way the stator is wound). Phillips' new technology has ring coils which offer an almost unlimited choice of step angles, a better performance, and a very high torque-to-volume ratio . . . . **Norway.** Travel in the Scandinavian countries is being made easier. Two thousand terminals are being placed in airline, train and bus terminals, hotels, motels, travel agencies, etc.

High Speed Controller Development

Steve Drucker

MNEMONIC DEFINITIONS *
(Used to define symbolic language)

Loop: EQU H#D; Test loop end, jump to loop beginning if fall,
POP STK if pass.
Cont: EQU H#E; Continue
Push: EQU H#4; Push current address +1 on stack.

INSTRUCTION DEFINITIONS * (Used to define subinstruction format)

```
SEQ: DEF 4VH#E, 1VB#0, 3X, 8VX, 16X
         |      |      |   |     |
         |      |      |   |     Reserved for ALU
         |      |      |   Bit branch address, no default
         |      |      ALU Flags
         |      Register load, default value O
         Sequencer instruction, default value E (continue)
```

ASSEMBLY INSTRUCTIONS (User program based on above definitions)

Seq Push: Set up hold
Seq Loop: Hold at current address until inpug arrives

OBJECT CODE

0100 0XXX XXXX XXXX XXXX XXXX XXXX XXXX
1101 0XXX XXXX XXXX XXXX XXXX XXXX XXXX
* Partial definitions from Step Demo System, 2910 based

Figure 1: Example of TMA use.

Winchester disk technology and high speed serial communication links such as the Ethernet are but two of the areas that have fuelled the recent growth in high speed controller requirements. In the past, high speed interface design employed MSI. Due to design complexity and availability of inexpensive programmable logic blocks, design philosophies are changing. The 2910 Sequencer and 2901 ALU of 8X300 now form the starting place for most controller designs. Furthermore, hybrid monolithic MOS and bipolar interfaces are becoming commonplace; the MOS processor provides required intelligence and bipolar controllers provide the high-speed signal-handling capability. Whether this approach or one which is solely based on high speed microcode is taken, you must cope with a whole new set of development problems: language design, program design, system architecture and program system debug.

Most are familiar with MOS Development Systems and produce at least one design using them. The monolithic processor design problem is conceptually simple: pick the processor and peripheral chips that satisfy the throughput requirements and structure the software design approach to handle the desired tasks. With current in-circuit processor emulators, a design based on a standard 8-bit processor is easily debugged. The designer working on a custom high speed controller has additional problems to consider: (1) What sort of controller architecture will provide for today's throughput requirements and tomorrow's upgrade while minimizing cost? (2) How will this custom design be developed, debugged and tested in a real time operating environment?

In an ideal world the preceding two questions are independent. Unfortunately, in the real world, they are not. If only very simple development techniques can be employed, then the architecture chosen will be designed to minimize development at the expense of overall design time, cost and flexibility.

What is necessary for development? Basically the same things that are required for MOS processor development; a way to: generate machine code, try the generated code,

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modify the code, control the target machine and monitor the target machine.

The complicating factors are speed, 100-250ns for complete instruction and architecture that will be unique and variable from project to project. The instruction sets will be different for every project. For small projects, an expense of $20,000 or more for development aids cannot be justified. The designer is forced to make as much use of existing equipment as possible. However, he must still get the job done on schedule.

generating machine code

The designer who elects not to use an assembler to generate machine code is courting trouble. True, a 100-line program can be hand coded from assembly language to machine code — but it's tedious, error prone and provides hard-to-upgrade code. Worse yet is a program written in machine code directly, leaving no documentation trail for others to make code modifications. Any additions require a complete new program to be written once the originator leaves.

Avoid these problems; use a good assembler. Let's examine our TMA, (Transportable Meta Assembler). It can be installed on an Intel or Futuredata Development System, a CPM-based μC, a mini or in-house timesharing network. With it, a designer can generate an assembler customized for his controller architecture. The instruction set, symbolic names, variable default values and constant values can all be defined. **Figure 1** gives an example of TMA useage for program definition. Once this definition is complete, the TMA becomes a standard two-pass assembler providing cross reference tables, error messages, source and object listings. By using an assembler on existing in-house equipment, you obtain both machine code and a readable, commented assembly listing which can be modified to add additional capability.

trying the program

It is easier to test a controller design in speed mode than it is to slow it down. With non-real operation, critical timing paths can't be checked and the operating environment must be simulated, a design task in itself. The difficulty of slow-speed checkout plus the control work width, rules out directly using a MOS Development System. Basically, you have three choices: burning PROMs, building a RAM array or adding to existing development tools. The PROM approach is simple but costly. Engineering time during debug goes up dramatically due to an inability to easily modify the code to find or patch problems. A simple change requires pulling the PROMs, editing the code, reassembling, burning new PROMs and reinserting them into the breadboard. It also forces the designer to spend time determining when to change code versus leaving problem code for future modification. If the bad code interacts with something that is bug-free, time is wasted looking for a problem that has already been found.

Building a RAM array to which the code can be downloaded is a better approach. However, this also has pitfalls: a means of loading the RAM array must be found, the decision on whether to incorporate an editor must be decided, and finally, determination must be made on how far to carry the design concept; i.e., should the RAM be part of the breadboard and therefore non-transportable to prototypes or must an interconnect be designed? Companies which spend design time up-front, end up with useful self-built equipment (if it is properly documented). The very design that goes into the RAM array potentially lengthens the development time and increases engineering costs without adding capability to the end product. Furthermore, the RAM array is only part of the design; a control panel is also necessary.

Adding high speed microcode capability to an existing development system or computer provides a cost effective solution to trying the code and also allows future upgrade. A system like the STEP-CCI, Computer Controlled Instrument, is one example of such an approach **(Figure 2).** It comes with a driver listing for an Intel or Futuredata and can be used with any programmable system with RS-232 serial ports system. This system provides 32 Kbits of high speed memory (which can be expanded to 1152 Kbits), editor and preprogrammed RS-232 links for connection to the host system. The memory is designed to interconnect to the target machine

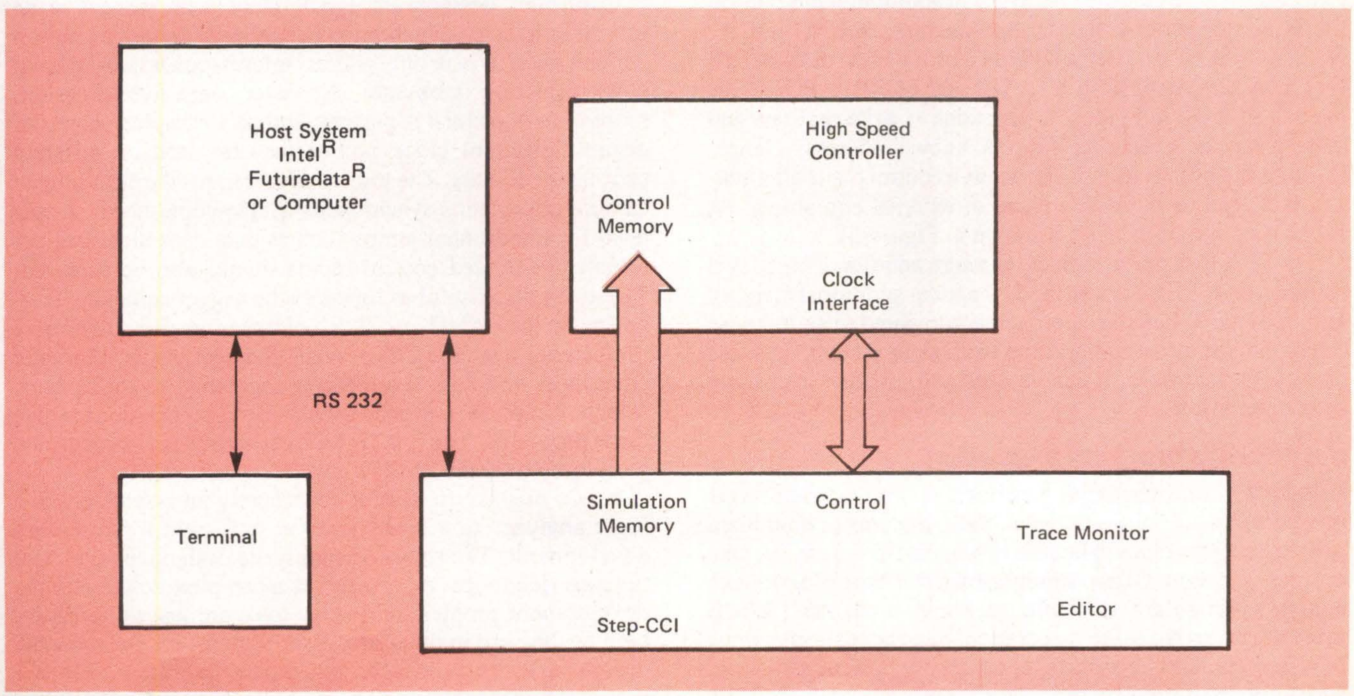

Figure 2: System Interconnect

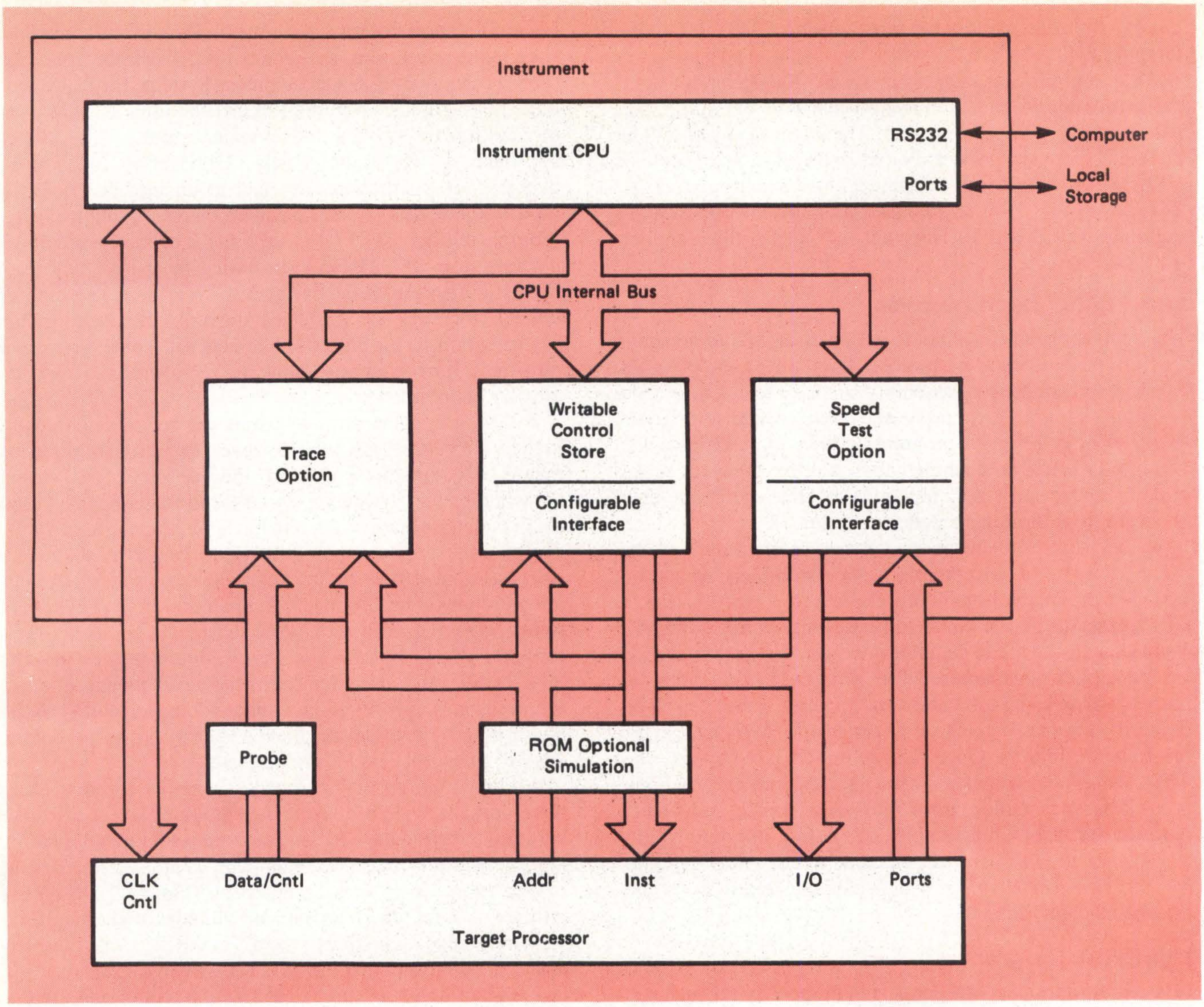

Figure 3: Step CCI

to replace PROM during checkout. In addition, it has built-in facilities to control the target machine: RUN, HALT, NSTEP, HALT on BREAKPOINT or EVENT, EXAMINE INTERNAL MACHINE STATE, and FORCE. FORCE is used to execute individual instructions to write registers and start program execution from a known address. Hence, through the host system it can act as a control panel eliminating the need to build this piece of external equipment. (A block diagram of the CCI is shown in **Figure 3**).

The CCI can be customized through additional high level routines on the host system and by adding additional memory and options. When this approach is compared to an in-house development effort to build the equivalent system, it is less costly. Furthermore, it can be used and justified over more than one project.

monitoring program execution

Effective design checkout requires a way to monitor target program execution. Sometimes, the symptoms of a problem provide enough clues to be able to pinpoint the cause and take corrective action. Often, simultaneous real-time events make analysis particularly difficult. At a minimum, the TRACE must not affect the system operation, must be real-time, must have a sufficiently good trigger capability for fault isolation. Most good second generation logic analyzers such as CCI's TRACE have this capability.

Controller designs are synchronous with respect to an internal clock so synchronous capture is desirable, but on which clock? Where only address information is being traced, clock selection is obvious. However, on a hybrid design, more than one clock is present, and on a complex controller design, different clock phases may be used on different processor sections. The logic analyzer needs the capability to capture information synchronous with multiple clocks. Inputs used for conditional jumps such as data dependent and externally generated control inputs should also be captured. These are also useful as inputs to the trigger equation. Triggering on the "AND" or "OR" of these signals helps resolve timing conflicts. The CCI provides 5 trigger inputs, 12 trigger equations, and dual level trigger capability, event counter, selective capture, and programmable trigger position to solve these problems. The full TRACE capability can be set up and monitored over the RS-232 link.

It is a mistake to assume that merely an assembler, or a logic analyzer or a RAM array is suffficient for controller development. The rigors of high speed design, complex real time service loops, etc., mandate a complete solution to the development problem. Effective tools are just as necessary here as they are in other processor designs if a maintainable design is to be produced. Equipment like the STEP-CCI provides the means to add high power development capability to exisiting development systems at a reasonable cost. D

FORTH "Breaks The Ice" In Software Development

Bob Kimball

FORTH provides a general, compact, but very powerful core of constructs for handling arithmetic, logic, data structures, mass storage interface, editing and assembling. You can modify, delete, or add to these constructs as the problem at hand demands because FORTH is an extensible language. It is also a multi-level language: without any linking operation, high-level FORTH "words" or modular programs can invoke low-level FORTH words. Because of its multi-level nature, programs can be written in high level language and easily optimized by coding a few critical words in low-level FORTH, which executes at full machine speed.

interactive development simplifies work

It is a completely interactive language: you start with simple FORTH routines ("words") and test them as they are typed at the terminal. Testing to see what has happened to date is easy because FORTH makes explicit use of a push-down data stack for parameter passing and temporary storage. To see if a definition is working properly, you examine stack contents by simply typing the word ., (or "dot,") which prints the top stack value on the VDT screen. You can test all modules simply by invoking them from the VDT keyboard with reasonable arguments on the stack, and then check the results. There is no requirement for any special test program or "harness" to do this interactive testing.

Interactivity will be a principal tool for use throughout the development process, as you check out more and more complex routines when they are written. Interactivity encourages modular program design. You write interchangeable parts, or fundamental words which can be used in a variety of situations, somewhat like subroutines without the call and return statements. The result is top-down program design and bottom-up coding, an efficient and structured approach.

The use of the data stack leads naturally to postfix notation. Therefore, words expect their arguments to be on the stack before operation takes place.

block

As for handling of mass storage, in polyFORTH, mass storage is organized into 1024-byte blocks. Using the FORTH EDITOR, a block may be listed on the terminal screen. It will appear as 16 lines of 64 characters each. Your compiled and tested definitions will be edited onto a block, usually on floppy disk, for permanent storage. Blocks can be transferred into program memory by LOAD commands for execution-time use, either explicitly by typing LOAD followed by carriage return, or from an application load block with load commands for all of the blocks containing application definitions edited onto it.

As in a natural language, words are the building blocks of FORTH. A high level word is created or defined by following this format when typing at the terminal:

```
: NAME  names of previously defined words  ;
```

Colon and semicolon are pre-defined FORTH words which begin and end compilation of a new high level word. A new word is added to the top of your "dictionary" when it is compiled. The dictionary is a linked list of all the words defined so far residing in RAM. A word you define is resident in the dictionary just like the supplied words OR, +, and :. To compile your newly defined word, a text interpreter compiles the addresses of the previously defined words in the dictionary space of the new word. At run-time, a fast address interpreter executes the code at each word's address and jumps to the address of the next word invoked in the definition until the routine compiled by semicolon is encountered, which terminates that word's execution.

Low level FORTH words can be defined and added to the dictionary just like high level words by typing:

```
CODE NAME  assembler mnemonic instructions  NEXT
```

Code definitions would normally be used for interrupts, I/Os and operations where speed is a critical factor. Only these low level words are machine dependent, and since most FORTH applications are written mostly in high level FORTH, a high degree of transportability of programs can be achieved.

With this basic summary of FORTH's implementation, we will approach a development problem to illustrate the differences between FORTH and more traditional development approaches. In this problem, the target applications will be built around a single board computer.

developing on target

For some classes of application, an existing SBC would be a logical choice. Now normally, the programmer is committed to an expensive development system like the MDS 235 in the case of an 80/10 target, and would either use assembly

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language or some high level language linked to assembly sub-programs and probably an in-circuit emulator. With FORTH, the development system in this case *is* the target because there is a FORTH which will reside on the 80/10's PROMs with some help from a disk. The 80/10 has a serial port so we can add a terminal. Because it is a standard multi-bus board, we can add a floppy disk controller and drives. And we can outboard RAM for developing the original program. Right away, we have saved a lot of hardware alone. The SBC 80/10 with the peripherals noted may cost typically about $5K; compare this to a $15K MDS 235 development system.

The initial phase of software development in FORTH may be spent at your desk, but it won't be the writing of your entire application program. FORTH encourages top-down design with bottom-up coding.

For the sake of brevity, as an example, consider this very simple task: we have a cryogenic environment and a μP must sample the temperature and decide whether to let in another burst of liquid nitrogen. Visualize the overall process as a sequence which goes SAMPLE COMPARE CHECK in an infinite loop. A sensor transmits an analog signal through an A/D converter to our μP in the SAMPLE segment, then in COMPARE, the digitized temperature reading is compared with a digital representation of the desired temperature entered via a front panel. CHECK periodically takes the results of the comparison and opens the liquid nitrogen valve if necessary for a specified duration.

To go from the top down, we follow each of the three functions to its most basic operations. In this example, we will trace CHECK to its roots. CHECK will have to open and close the liquid nitrogen valve, time the duration of the opening, and periodically scan the results of COMPARE to decide whether or not to open the valve. A top-down tree for CHECK might go like this:

CHECK → CYCLE → OPEN or CLOSE. OPEN and CLOSE represent the lowest level of operation in CHECK. This is where we will start the bottom-up coding process. Assuming the 80/10 target, and port 1 as the output controlling the valve, we would write:

CODE OPEN 1 # A MOV NEXT and A1 OUT NEXT
CODE CLOSE 0 # A MOV NEXT A1 OUT NEXT

These code definitions make use of 8080 assembler mnemonics, and directly route either a 1 or a 0 to port 1. We can debug these routines by connecting our electromechanically controlled valve to the output port and simply observing the proper operation. Or, we could put any kind of hardware, like an LED for example on the port, if target hardware is yet unavailable. Or, we could write a short routine to store port value in a RAM location which can be dumped at a later time.

From the primitive operations defined at the outset of development, FORTH's extensibility will enable creation of more sophisticated routines. For example, suppose our control operation specifies that the valve be opened and then closed after 100ms. With the words OPEN and CLOSE already defined, we can now define the word CYCLE which will satisfy the desired function. We suppose for now that the decision rule will be that the valve opens if CYCLE finds a 1 on the data stack, and remains shut if a 0 is on the stack. The word CYCLE could be defined like this:

: CYCLE IF OPEN THEN 100 MS CLOSE ;

The colon begins compilation of the high level word CYCLE. IF is a logical operator which branches to OPEN if a nonzero number is found on the stack, or to THEN if zero is found. If there was a nonzero number on the stack, OPEN would be executed at run time, followed by a branch to THEN, a 100-ms delay and then execution of CLOSE. If zero had been on the stack, at execution CYCLE would have performed only a 100-ms delay and the CLOSE routine.

CYCLE illustrates the free intermixing of high and low level FORTH. No special linking was required as the CODE definitions OPEN and CLOSE are compiled in the same dictionary as high level words like CYCLE. So it is easy to write high level definitions using low level words.

To complete this bottom-up coding sequence, we can easily perform a CYCLE every second with CHECK:

: CHECK BEGIN 900 MS DUP 2 < IF CYCLE AGAIN DROP ;

At execution time, CHECK will set up an infinite loop with the structure BEGIN. . .IF. . .AGAIN. The 900-ms delay, the duplication of the top stack parameter (DUP), and the placement of 2 on the stack will be executed at least once. If the duplicated number which we presume to be on the stack prior to execution of CHECK is less than 2, then the IF branches to CYCLE.

The comparison between the number on the stack and 2 left only a truth value of 1 or 0 on the stack. When the IF executed, it destroyed this truth value. We DUPed the original parameter on the stack so that cycle would still have a parameter on the stack for its IF. After CYCLE, AGAIN jumps back to 900 MS and another pass is made through the loop. The loop terminates when the parameter on the top of the stack prior to CHECK is greater than 2. In this way, the loop will keep going as long as CHECK finds truth values on the stack. If at power down another FORTH module left a 5 on the stack, CHECK would terminate the loop and the valve would be in the closed position.

The simplicity of FORTH software development makes for a conspicuous absence of things like breakpoints. When you have 100 lines of source code and a problem somewhere between line 1 and line 100, the philosophy of breakpoints can be justified; but in a one-line FORTH definition, it is much easier to correct a mistake by testing interactively before editing it into your program on disk. For the case of the SBC target, in FORTH there is no need for ICE or its attendant time lags in talking to the monitor, then the debugger, then the emulator — each with its own set of commands and protocols. FORTH's extreme modularity will save you a lot of detective work.

When a FORTH program is correct on the host in a RAM environment, it can be burned into PROM for stand-alone operation. PolyFORTH includes Target Compiler software which facilitates the transition. The target compilation generates executable code for the target. In doing this, headers for all the application vocabulary words may be dropped. Headers are used in the host system to provide random word access which may or may not be of use in the final application. Another characteristic of target compilation is to include in the target vocabulary only those FORTH words that will be needed for program execution. Thus FORTH's extreme compactness is further enhanced for fitting programs into limited object hardware memory.

Target compilation involves several operations which we will discuss briefly. The first stop of the compilation is to create an application load block on disk. The application load block will transfer all of the blocks containing your application definitions from disk to program memory. The next step is to write a target load block which will load a "nucleus" or subset of FORTH, with all the words needed to run the application program on the target, then the target compiler, the application itself, and finally a block you write containing definitions for an initialization routine in low level code to bring the application up at power-on time.

When you have finished editing the target load block, all object code for the application will be on disk. At this point you can dump, burn PROMs, or do whatever you wish. Then the program can be tried on the object hardware and evaluated. Because all of the application is loaded from a single block, it is simple to revise or add to the application. We can edit definitions on disk and can add new ones to the application blocks until the system operates as desired.

The target compiling process has a degree of difficulty related to the memory in the target. Less RAM means more restrictions. For example, we would be careful to locate any arrays in the RAM portion of memory, and simple look-up tables could be placed in ROM. Nor could we store into CONSTANTS which are also in ROM.

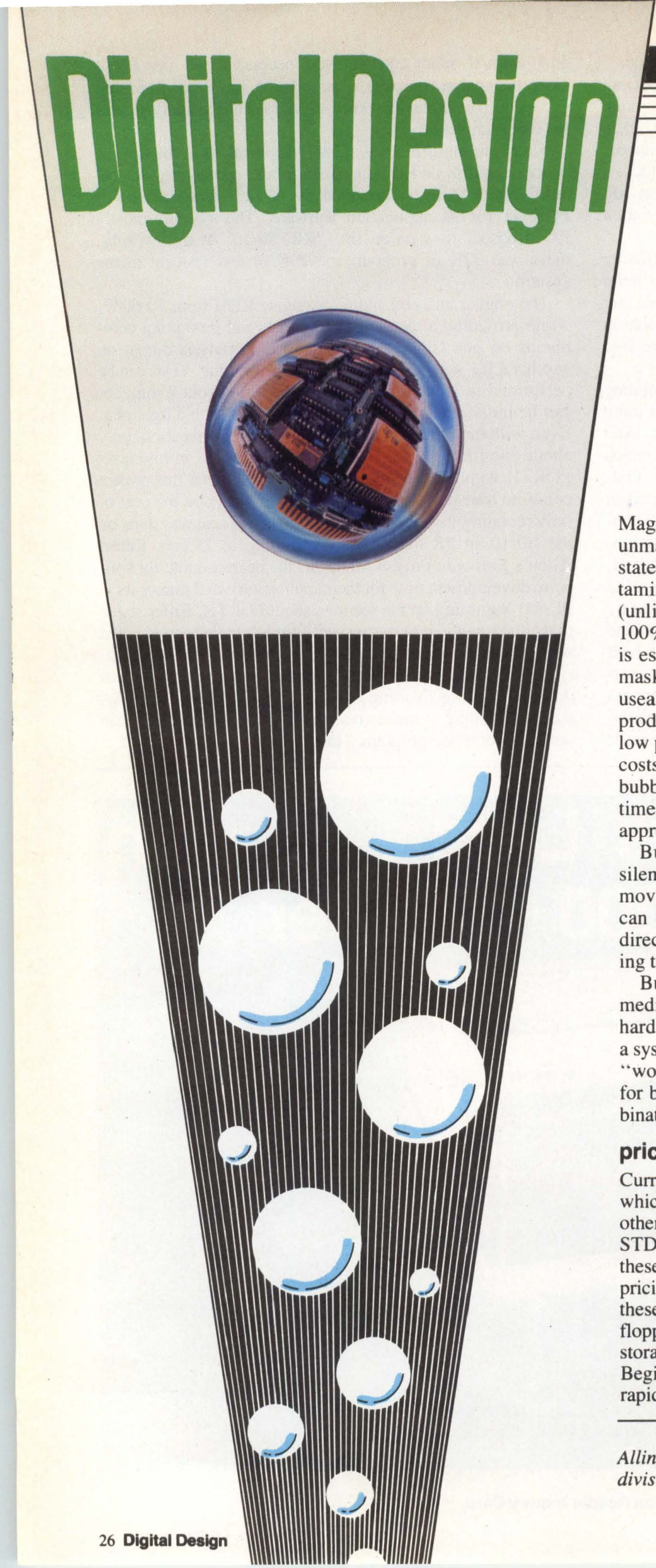
In the experience of FORTH users, the target compiling process represents only a slight discontinuity which is more than compensated for by savings in development time. And like any process, target compiling has a learning curve which makes the second target compilation much easier than the first.

We have gone from start to finish for software developed on a single board computer target; we might draw several conclusions. First, we were able to take advantage of some substantial hardware savings before we ever got started. Second, we saved a lot of time during primary development by being able to interactively perform a top-down design achieved by bottom-up coding. Third, we were able to easily combine different levels of FORTH to help us develop faster with high level constructs and preserve flexibility and run-time optimality with low level code. Fourth, we turned our application into a ROM environment with the Target Compiler. If we had to make small changes in the finished program, we didn't sweat; and, even if major changes were necessary, we didn't lose sleep because a complete recompilation and PROM burning cycle could be done in minutes — not the hours usually needed for other languages.

There are many real case history applications in the field of process control and data acquisition and processing. A new auto engine analyzer designed by Allen Testproducts used FORTH for its application software. The system, mostly ROM-based, runs on an Intel SBC 80/10. At this writing, there was 32K of program and 20K of text resident in the system.

The engine analyzer monitors engine RPM from 50-6000, while providing a menu of test routines and prompting commands on one CRT to the operator and analysis output on another CRT with simultaneous off-line printing. Tests can be performed in an automatic sequence taking about 7 min., or can be individually selected by the operator with a light pen. Even with the critical real-time nature of the application, only about one-fourth of the application was written in low level FORTH with the rest in high level, meaning that this project could be transported to a faster CPU if desired at the cost of only recoding low level words. All development was done on the 80/10 in 18 manweeks. According to Dennis Rufer, Allen's Software Project Manager, the nearest quote for software development time for their application was 2 manyears in PL/M! Summing up his feelings about FORTH, Rufer stated that "the engine analyzer project couldn't have been handled with any other language."

An EE conversant in Postfix notation can give up the usual duties of linking, sorting out mistakes like needles in haystacks, patching to make code work, and waiting to try again with a recompiled program. D



Bubble Memory

Alling C. Foreman

Magnetic bubble memory has several operational advantages unmatched by other mass storage. First, bubbles are a solid-state medium; no moving parts wear out or become contaminated with dirt, dust or smoke. Second, bubble-memory (unlike silicon-based RAM) is a magnetic technology and is 100% non-volatile, just like disk and tape. Third, the device is essentially a simple chip to make, because only a single mask step is required, and because it need not be perfect to be useable at specified capacity. This combination of simplified production and ability to use imperfect chips promises very low per-bit pricing in the immediate future, with parallel low costs for systems built around the bubble devices. Fourth, bubble memory is much faster than floppy disks, with access times similar to those of hard disks, and transfer rates approaching megabit-per-second levels.

Bubble memory also promises very high storage density, silent operation, and low power consumption compared to moving-media systems. And lastly, bubble memory systems can be entirely constructed on PC boards that can plug directly into the bus structure of a computer system, eliminating the need for additional chassis and power supplies.

Bubble memory can also be used as a removable storage medium. But for removable bulk storage, floppy disks and hard disk cartridges will be far more economical. Therefore, a system which employs bubble memory for high-performance "working" mass storage, combined with a floppy disk drive for back-up and data archiving may offer the optimum combination of mass-storage features for many applications.

price trends

Currently, complete bubble memory systems are available which can be plugged directly into DEC LSI-11s, Intel (and other) MULTIBUS systems, S-100 systems, T.I. 9900s, STD-bus machines and others. Small-quantity pricing for these systems is currently in the area of \$25/Kbyte, with pricing approaching \$11/Kbyte in OEM quantities. Even at these prices, bubble memory systems are competitive with floppys for systems requiring only a modest amount of mass storage, as is often the case in the process control field. Beginning this summer, prices will drop rapidly due to rapidly-maturing chip production processes and competition.

Alling C. Foreman is Chief Engineer, of Bubbl-Tec, a division of PC/M Corporation, Dublin, California

Mass Storage for Microcomputers

bubbles vs floppies

Frequently cost comparisons are made between bubble systems and floppy-disk systems, since both offer low-cost mass-storage with moderate capacity. While bubble systems offer operational advantages over floppy systems, like faster, quieter and more reliable operation, lower power consumption and smaller physical size, the floppy offers the convenience of a low-cost removable storage medium.

When comparing the cost of bubble versus floppy storage, one must consider the variables of time (since bubble prices promise to drop rapidly), production quantity, and total required storage capacity.

Both the bubble system and the floppy system require a fixed initial cost to allow storage of the first byte. In the case of the floppy, this initial cost is for chassis, power supply and controller electronics. In the case of a plug-in bubble system, the fixed cost is spent for power supply and controller circuitry. Although fixed costs depend on several variables, it is reasonable to say that the fixed cost of a floppy system today is roughly \$350 to \$900 as delivered, depending on quantity. For the bubble system, a support chassis is not required and power supply requirements are reduced, so the fixed costs might be closer to \$250 to \$750, again depending on quantity.

This difference in fixed costs between the two systems is significant, and gives bubbles a slight edge, mainly due to the fact that the bubble system does not require a separate housing, and is less power hungry.

A major difference between bubbles and floppies can arise, however, as increments of storage are added to the fixed initial cost. Since bubbles are solid-state devices, it is practical to add storage in very small increments, perhaps as small as 32 Kbytes. Currently this cost increment will be in the area of \$300 to \$500. By the end of 1984, this figure is likely to be in the area of \$50 to \$80.

Floppy systems, on the other hand, require a complete electromechanical drive in order to achieve the first increment

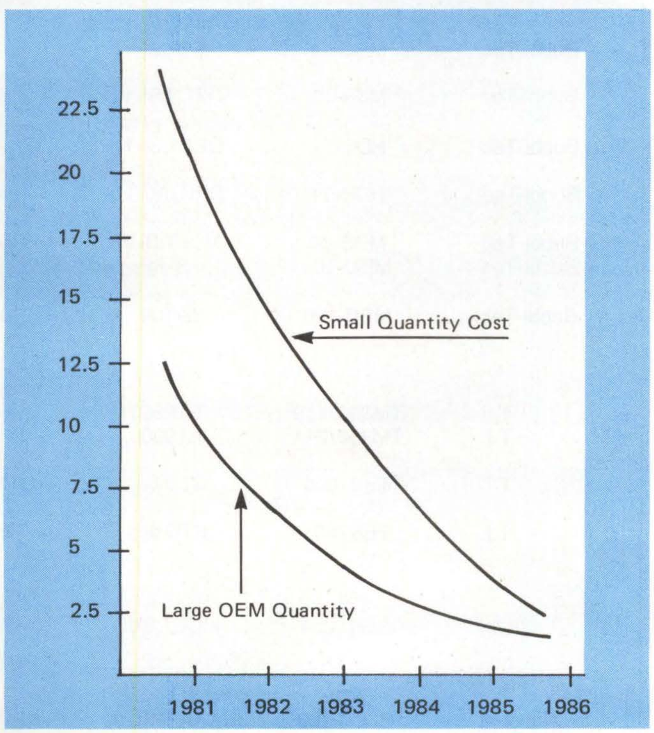


Figure 1: Small and OEM-quantity price projections for bubble memory systems.

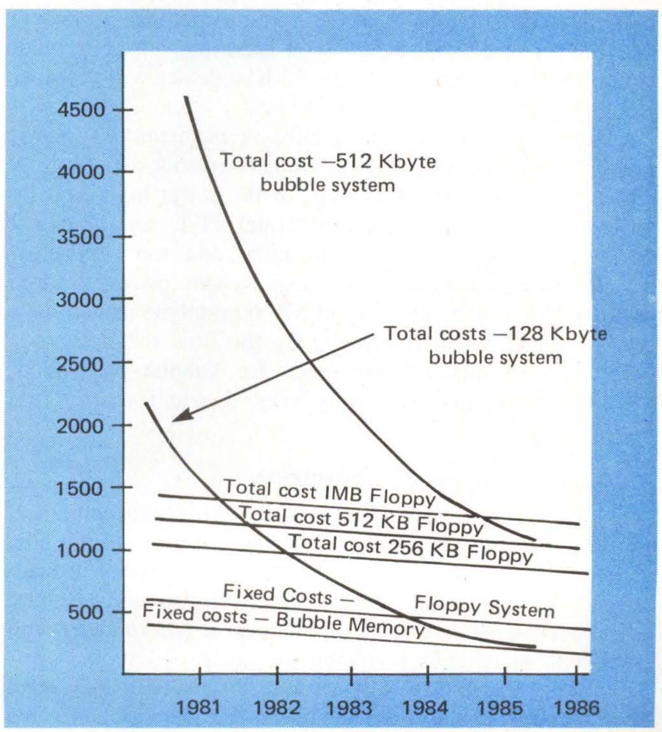
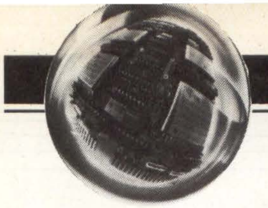


Figure 2: Price comparison for bubble memory system vs floppy disk considering total storage capacity



MANUFACTURER	TYPE #	CAPACITY	ACCESS TIME
Texas Instr.	TIB0203	92 Kbits	4 ms
Texas Instr.	TIB0500	512 Kibs	11.2 ms
Texas Instr.	TIB1000	1 Mbit	11.2 ms
National	NBM-2256	256 Kbits	7 ms
National	NBM-2011	1 Mbit	11.2 ms
Intel	7110	1 Mbit	40 ms
Fujitsu	FBM31DB	64 Kbit	370 ms
Fujitsu	FBM32DA	64 Kbit	4.5 ms
Fujitsu	FBM43DA	256 Kbit	6 ms

Figure 3: Currently available bubble memory devices.

of storage. The cost of the drive will be in the range of $275 to $500, depending on capacity and quantity.

Thus, the very smallest complete bubble system may have a total cost that is little more than its fixed intitial cost. The cost of the first floppy drive, however, will have a significant impact on the total floppy system cost. As a result, small bubble systems will be quite economical. The cost advantage of the floppy system will be seen as the storage requirement exceeds, say, 1 Mbyte. As time goes on, the cross-over point, at which total bubble system costs exceed those of the floppy, will move to larger and larger total storage capacity.

It is, of course, important to remember that price comparisons of bubbles vs floppies is valid only for those applications where the great operational advantages of bubbles (speed, reliability, storage density, quiet and low power operation, etc.) are without value. Probably in the greatest number of applications, the competitive advantages of bubble memory will make it worth a significant added cost.

currently available bubble-memory

A listing of announced bubble memory devices would list the T.I. 92-Kbit bubble device as the first successful production device; it currently still is the design being produced in highest volume, and at the lowest per-bit cost. For small mass-storage systems, the T.I. 92K device will continue to be the most economical for some time into the future. T.I. offers this device with a complete set of specialized silicon support devices (coil drivers, function drivers, etc.) to ease the engineer's circuit-design task.

It is the 1-Mbit device, however, that will soon take over center-stage in the bubble-memory market. This high-capacity device, offered by several manufacturers, provides enough storage capacity in just one package (128 Kbytes) to satisfy many small-system requirements. And prices for this device will decrease rapidly over the coming months, ultimately reaching a level well below 0.01 cents per bit. (For small amounts of storage, though, the 92-Kbit device will probably continue to offer the lowest per-bit cost.)

A summary of currently-available bubble memory systems, ready to plug into existing computer systems, would grow dramatically over the next year, as the newer high-capacity bubble devices announced by Intel, T.I. and National Semiconductor are applied to more and more systems. Competitive pressures will cause system prices to drop rapidly. Now is the time for OEMs to prototype new designs incorporating bubble-memory. By the time the designer's bubble-based products are ready for volume production, bubble-system prices will likely be less than half what they are today.

designing-in bubble memory

The easiest way to add bubble memory into existing computers is simply to plug board-level systems directly into the bus. Current products work this way. The LSI-11 bubble system offered by Bubbl-Tec, for example, incorporates an entire DEC-compatible controller on one dual-height module, with 46K-byte increments of bubble storage on additional dual-height modules call BUBBL-PAC's. The BUBBL-PAC's get their control signals from the controller via a ribbon cable which can daisy-chain from one BUBBL-PAC to the next. Since the BUBBL-PAC's do not make use of the Q-bus signals, they can alternatively be mounted in a separate housing if desired.

The larger MULTIBUS systems incorporate the controller on the same board with the bubble devices. Other systems for the STD-bus and S-100 bus, like the LSI-11 system, use the separate controller approach.

With most of the board-level systems you can remove a bubble-memory module without loss of stored data. Therefore, data can be moved from one machine to another, or one module can be replaced with another containing different data. Compared to floppies, however, bubble memory is obviously an expensive removable storage medium. In special applications, though, the removal capability of bubbles can be valuable despite the expense involved. An example might be moving data from a data-acquisition system to a larger computer for data reduction. One manufacturer, Fujitsu, has designed a small removable bubble "cassette" module to facilitate off-line storage.

The alternative to ready-to-operate bubble memory is to design a custom system for the application at hand.

MANUFACTURER	MODEL #	FOR MICROCOMPUTER	BUBBLE DEVICE
Bubbl-Tec	MBC-11	DEC LSI-11	—
Bubbl-Tec	MBB-11	DEC LSI-11	TIB0203
Bubbl-Tec	HDC-11	DEC LSI-11	—
Bubbl-Tec	HDB-11	DEC LSI-11	TIB1000
Bubbl-Tec	MBB-80	MULTIBUS	TIB0203
Bubbl-Tec	MBC-100	S-11	—
Bubbl-Tec	MBB-100	S-100	TIB0203
T.II	TM990/219	T.I 9900	TIB0203
T.I.	TM990/211	T.I 9900	TIB1000
T.I.	TBB7090	STD bus	TIB0203
T.I.	TBB7091	STD bus	TIB0203
Intel	SBC0254	MULTIBUS	7110
National	BLC-9250	MULTIBUS	NBM-2256
National	BLC-9101	MULTIBUS	NBM-2256

Figure 4: Currently available board-level bubble-memory systems.

DATA RATE	ARCHITECTURE	PACKAGE	REMARKS
50 Kb/s	major/minor loop	14-pin	
100 Kb/s	block relpicate	24-pin	Half of TIB1000
200 Kb/s	block replicate	24-pin	2-track device
100 Kb/s	block replicate	16-pin	
100 Kb/s	block replicate	16-pin	
100 Kb/s	block replicate	20-pin	Larger package
100 Kb/s	single loop	18-pin	Also available incassette form
50 Kb/s	major/minor loop	18-pin	
100 Kb/s	block replicate	20-pin	

performance characteristics

Since the operation of a bubble memory system resembles the operation of a disk storage system, there are several terms normally used to characterize the performance of a disk system that can also be applied to bubble memory. These include seek time, access time, transfer rate and error rate.

In a disk system, the seek time is normally taken to mean the time it takes to move the R/W head to the track where the relevant data is located. In the bubble system, the minor loops must be rotated until they are in position to transfer or "replicate" the bubble domains from the minor loops to the major loop or the R/W tracks. Thus, the seek time for a bubble memory device is dependent upon the number of bit positions or "pages" in the minor loops and the bubble shift rate. Most current bubble devices are designed to be shifted at a 100 KHz rate. Depending upon the architecture of the bubble memory device, the minor loops typically contain from 64 to 4096 bit positions, or pages. Thus, worst-case seek times can be calculated by multiplying the number of pages by 10 μs, resulting in seek times between 6.4 and 41 ms. Average seek times will be half of these worst-case figures.

STORAGE CAPACITY	APPROX COST	REMARKS
—	$ 460	RX01-compatible controller
46 Kbytes	900	BUBBL-PAC for use with MBC-11
—	950	RX02-compatible controller
512 Kbytes	6500	BUBBL-PAC for use with HDC-11
92 Kbytes	1800	
—	460	DMA-type controller module
46 Kbytes	900	BUBBL-PAC for use with MBC-100
46 Kbytes	1250	T.I. 9900 system bus
128 Kbytes	3145	Uses 1-Mbit bubble device
11.5 Kbytes	615	Controller plus one bubble device
46 Kbytes	1150	Expansion board; use with TBB7090
128 Kbytes	3500	Board expandable to 512 Kbytes
32 Kbytes	1750	Single 256-Kbit bubble device
128 Kbytes	3500	Four 256-Kbit bubble device

The average seek time for a typical floppy disk is close to 400 ms, and over 50 ms for a typical hard disk. Thus, the seek times for a bubble system will better a floppy by as much as two orders of magnitude, and a hard disk by perhaps a factor of five to eight.

The access time for disk drives includes the seek time previously discussed, any required head settling time, and the rotational latency of the disk drive. For a bubble system, the access time includes the seek time and the time required to shift the read track or minor loop so that the first bit of data is under the read detector. It typically takes about 100 shifts or 1 ms to move the read data to the detector. This read track shift time is fixed by the bubble device design. Thus bubble access time can be calculated by adding about 1 ms to the calculated seek time.

The rotational latency alone for a typical hard disk averages over 7 ms; 50 ms for a floppy. The result is that bubble systems can provide total access times 25 to 100 times faster than most disk systems.

The effective transfer rate at which data is moved between the bubble devices and the host computer is dependent primarily on the bubble shift rate, and how many bubble devices are active at a single time. When bubble devices are operated serially (i.e., only one device accessed at a time), the effective transfer rate may be as low as the bubble shift rate (and perhaps lower if the controller operation requires it). When bubble devices are operated in parallel, however, the transfer rate can easily exceed the bubble shift rate, by a factor equal (at most) to the number of devices operating in parallel. Some of the 1-Mbit bubble devices have two parallel sets of read and write tracks, allowing transfer to/from a single device at close to 200 Kbits/sec. When four of these devices are operated in parallel, as in Bubbl-Tec's HDC/HDB-11 system for LSI-11s, the peak transfer rate is close to 800 Kbits/sec. This compares favorably with the 250 Kbit/sec transfer rate of a typical floppy. Operation at the 2.5 Mbit transfer rate of typical hard disks would require many more bubble devices operating in parallel, however.

As in disk systems, both soft and hard errors can be defined for a bubble memory system. A soft error is said to occur when a bit is read incorrectly during a single read operation, but is read correctly on a subsequent operation. A hard error is said to occur when a bit is read incorrectly during several consecutive read operations. Tests of bubble devices by their manufacturers have shown soft error rates of 10^{-9} (that is, one bit error in 1,000,000,000 bits) to be typical. Hard error rates of 10^{-12} are also probably typical for bubble devices. The corresponding typical error data for floppy disks is similar to that for bubbles, assuming use of a high-quality diskette in good condition.

Because bubble errors are primarily single-bit errors, they are usually easily detectable (and then correctable) by using standard error detection procedures, such as CRC checks. Several bubble device manufacturers are already including error detection and correction logic built into some of the specialized silicon support devices they are providing with their bubble devices. When error correction logic is provided in the bubble memory system, it is at least theoretically possible to achieve overall system error rates of 10^{-16} to 10^{-20} One of the very most effective soft-error correction schemes is simply to re-read the erroneous data.

Our experience with bubble devices shows them to be

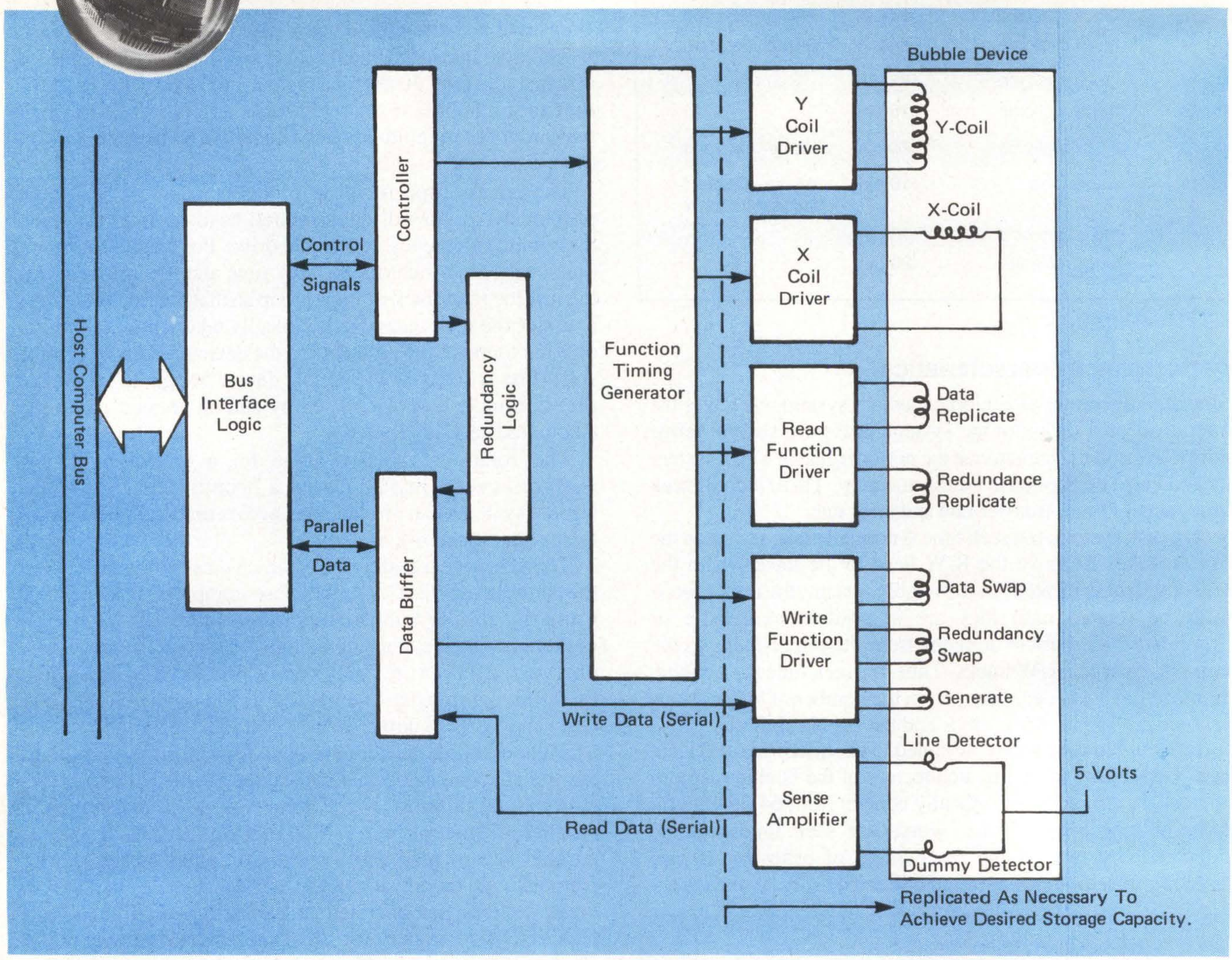


Figure 5: Typical block diagram for bubble-memory mass-storage system.

highly reliable in actual field operation. Although field failures of bubble systems delivered to date have occurred, they have predominantly been due to failure of semiconductors other than the bubble devices. The only failures so far have been caused either by catastrophic failure of other components in the system, or by attempted improper operation of the system.

system design

The design of a bubble-memory system is much more complex than is design of memory systems using other forms of solid-state memory. Relatively few external control signals are required by most semiconductor memory devices, and the signals that are required are often not particularly critical in either amplitude or timing. Bubble devices, on the other hand, require many control signals with relatively precise timing and amplitude requirements. Thus, bubble systems can involve a great deal of support logic to generate the many control signals required by the bubble devices.

Fortunately, most of the bubble device manufacturers are producing specialized silicon support circuits which simplify the designer's task by performing many of the functions which involve the most critical control signals. The availability of these specialized support devices is probably essential to the popularization of bubble memory. Without them as many as 10 or 12 additional discrete semiconductors and/or integrated circuit packages may be required to support each bubble device, and this extra component count may have a negative effect on overall system reliability.

Even with the typical specialized support devices, however, there are still several design areas which need the designer's detailed attention. These will be discussed below, after a brief overview of the basic components of a typical bubble-memory system.

A typical bubble-memory mass-storage system for a small computer consists of an interface to the host computer's bus, a controller to produce the necessary control-signal enables, a data buffer, redundancy logic for bad-loop definition and error detection, a function timing generator to control the sequencing and duration of the control pulses required during each bubble shift cycle, function drivers to produce control pulses of the proper amplitude, coil drivers to energize the bubble-shifting coils, and sense amplifiers to detect the presence or absence of a bubble at specific points in the bubble-access cycle.

The characteristics of the interface to the host will primarily be determined by the requirements of the system bus. The interface protocol should be designed to minimize the load placed on the host computer. Another important consideration is to minimize the software required to integrate the bubble system into the host's operating system.

(continued on page 33)

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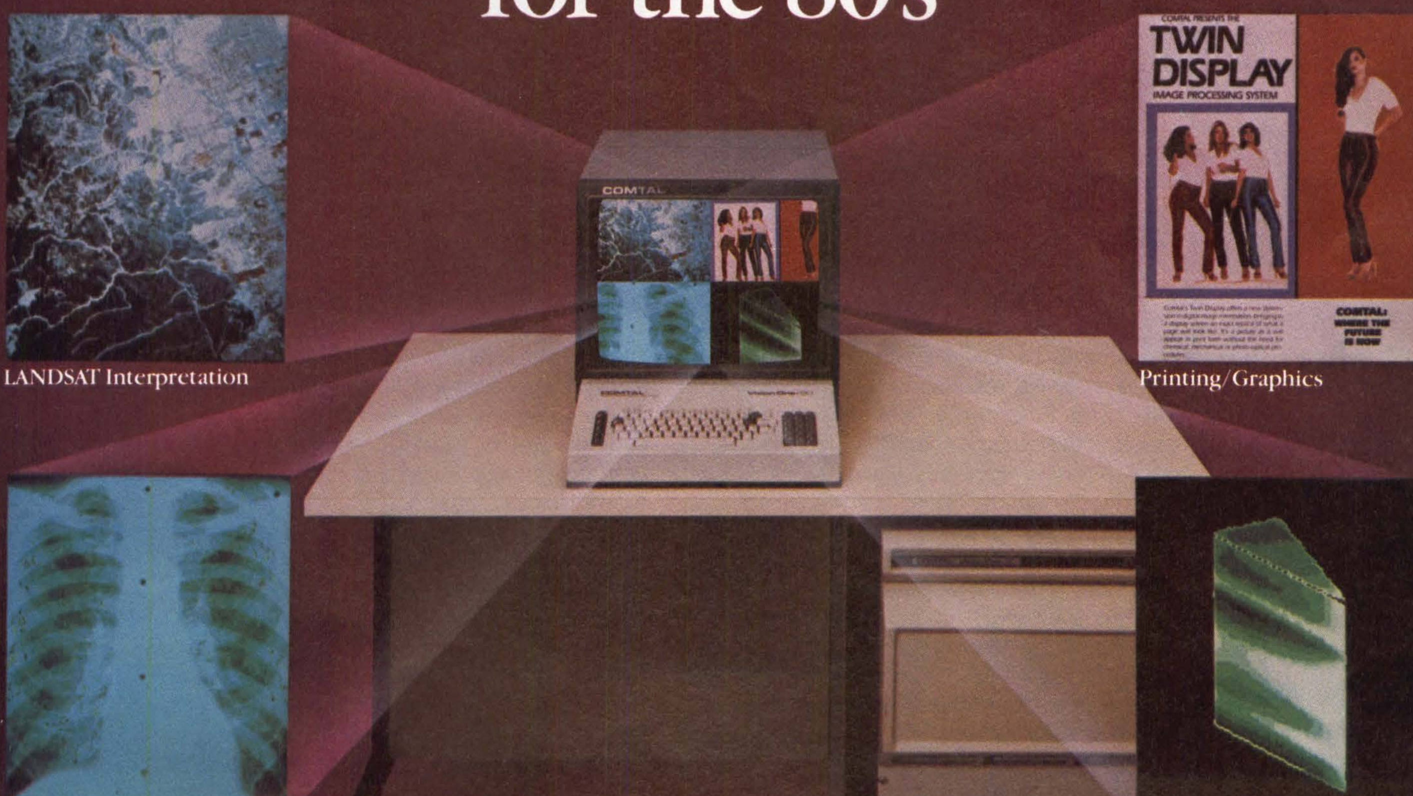

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Bubble Device Basics

All bubble devices to date have a non-magnetic garnet substrate onto which is deposited a thin film of magnetic garnet compound. "Bubbles" exist in the thin film — small cylindrical magnetic domains or islands of a given polarity (say North) floating in a sea of opposite polarity (South). A small permanent magnet, included in the device package, magnetically biases the device so that only proper-sized bubbles exist that are easily generated and erased by small current pulses. Bubbles are organized and forced to "march" in unison by magnetic fields generated by currents in two orthogonal coils wrapped around the garnet chip, and by a copper/aluminum conductor pattern which is deposited on the thin magnetic film. Brief current pulses in specially-placed loops etched into the conductor pattern allow new bubbles to be generated, old bubbles to be erased ("annihilated"), bubbles to be "replicated" into two new bubbles, bubbles to be transferred or "swapped" from one loop to another, and the presence or absence of a bubble at a given position and time to be detected.

Bubble devices are similar to shift registers in operation. A few devices, like Fujitsu's FBM31CA, are actually organized like a single long shift register, with all bubbles arranged in a loop which passes by a single write loop or "head" at one point, and a single read head at another point. The advantage of this architecture is design simplicity. The disadvantages are that the worst-case access time is long (740 ms for the FBM31DB), and that the single loop must contain no defects if proper operation is to be achieved.

To improve access time, a major-loop, minor-loop design is usually chosen. In this case the data is normally stored in a few hundred minor loops which have no direct connection between them. Each minor loop typically contains between a few hundred and a few thousand bubbles, depending on the device. To read data, one bubble from each minor loop is transferred in parallel to a major loop. The major loop is then shifted under the read head to read relevant data. Conversely, to write data, the major loop is shifted under the generate coil and the coil is pulsed at the appropriate times to produce bubbles where data is to be stored. The major loop is then rotated around until the "page" of data is properly aligned with the minor loops, and a transfer from major to minor loops is effected.

Not all minor loops need be operational. If a few extra loops are designed in, some minor loops can be defective and still meet the capacity specification. To transfer data from the minor loops to the major loop, and vice versa, the first method (exemplified by the TIB0203 92K-bit device) a destructive transfer operation moves the bubbles from the minor loops to the major loop. As the bubbles are moved around the major loop, they are either erased by a special "annihilate" coil which preceeds the generate coil for write operations, or replicated (split into two bubbles) for read operations. In the read operation, one of the bubbles is routed under the read head, and the other continues around the major loop until it is in position to be transferred back into the minor loops. This type of operation can be described as a "read-restore" operation.

More recent bubble designs are employing a "block-replicate" capability. In this case, parallel data transfer from minor to major loops is non-destructive. These devices also employ separate R/W major loops, actually called "tracks", since the loop is not really complete. Data transfer from the write track to the minor loops is called a "swap" operation. Some newer devices have pairs of R/W tracks which may be operated in parallel to increase throughput.

There are two major advantages of the block-replicate architecture over the read-restore method. First, the effective transfer rate can be improved because data does not have to be shifted around the major loop to be restored after each read operation. Second, the system is vulnerable to a loss of power for much briefer periods of time because operations can be aborted without needing to restore the data into the minor loops. D

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One way to accomplish these goals is to emulate an existing mass-storage system which is already a part of the computer's mass-storage heirarchy. Several of the systems offered by Bubbl-Tec, for example, employ controllers that emulate existing floppy disks.

Another important consideration in bus interface design is the form of transfer that will take place between bubble memory and the host system's RAM memory structure. For systems where only one bubble device is to be accessed at a time, the major constraint on performance will be the transfer rate of the bubble device. In this case, programmed I/O or interrupt-driven transfers are normally best, because the extra logic required for DMA operation will not produce a significant increase in overall performance.

In a system where several bubble devices are operated in parallel, on the other hand, the transfer rate to the host computer may be the limiting factor. In this case, DMA

High-Performance Bubble-Memory System

The HDC-11 and HDB-11 are plug-in memory modules for the LSI-11. HDC-11 BUBBL-BOARD is a DMA-type bubble-memory controller which emulates DEC's RX02 double-density floppy-disk system, and simultaneously provides improved performance. The controller can address up to 8 Mbytes of bubble memory and is software transparent to the DY floppy-disk handlers and utilities. The HDB-11 BUBBL-PAC module contains four 1-Mbit bubble devices, providing 512 Kbytes on a single dual-height PC module. Up to 16 HDB-11s are controlled by a single HDC-11. One HDC-11 and two HDB-11 modules provide the same storage capacity as a complete RX02 dual-drive, double-density floppy-disk system. And with the bubble system, operating speed is increased, less space is required, reliability is enhanced, less power is consumed, and operation is

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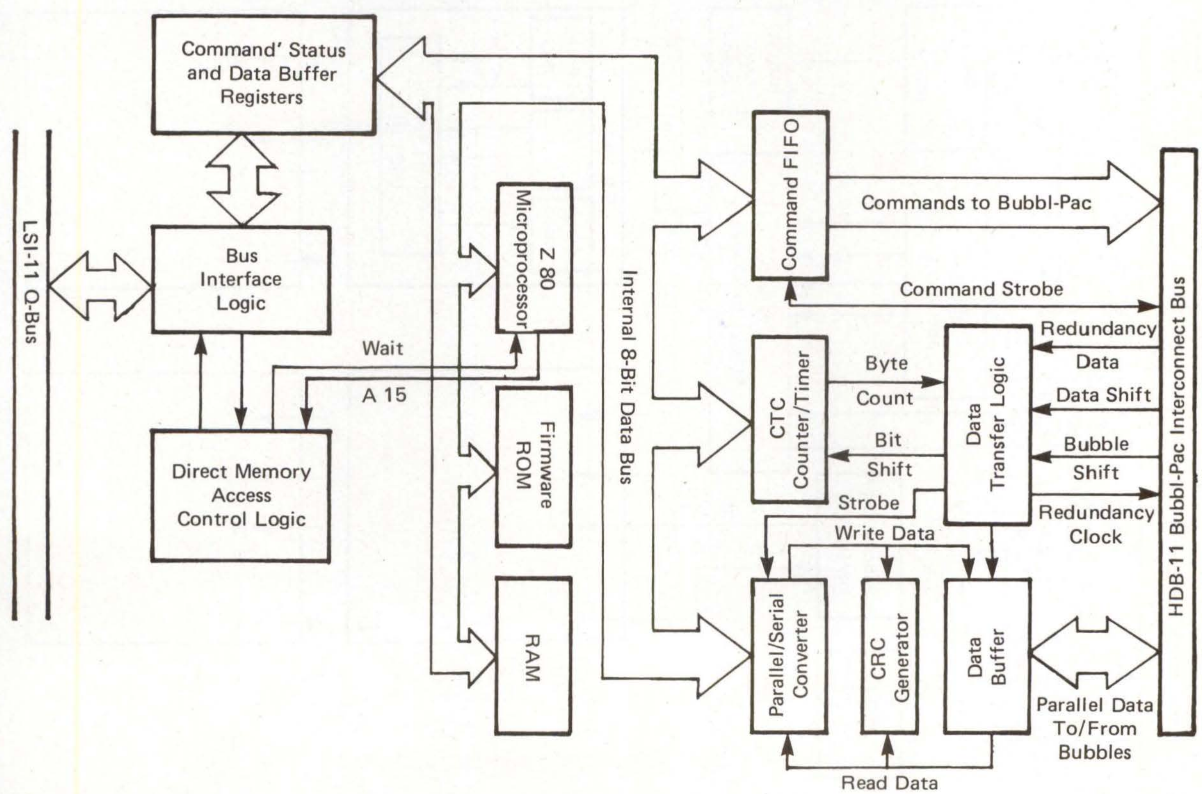
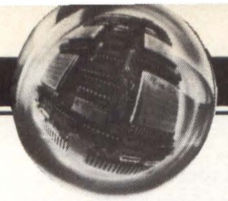


Figure B: Typical block-replicate device-schematic



opertion should be considered if speed of operation is to be maximized.

The controller function must provide the appropriate enable signals to allow control signals to be generated by the various support circuitry at the appropriate times during read, write, and bubble-shift operations. Often the controller function can be simplified by using an LSI controller supplied by the bubble device manufacturer. Where it is desired to make the ultimate user's task as simple as possible, however, it may be necessary to provide custom controller logic in order to implement the desired protocol. A microprocessor can often be used to provide most of the required controller functions.

An example of the latter approach is our HDC-11 bubble-memory controller for LSI-11 microcomputers. In this controller a Z80-CPU microprocessor and Z80-CTC counter-timer device are used to implement most of the controller functions. Th CTC device counts bubble shift pulses to determine when the Z80-CPU should load new control words into a bubble command buffer. It also counts data bits being clocked into a serial/parallel data converter required for parallel operation of the bubble devices, and tells the Z80-CPU when to load or unload a one-byte data buffer.

Data buffer design is related to the redundancy logic design. Each bubble device is accessed in a serial data mode. Thus, the data buffer must perform a parallel-to-serial conversion

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completely quiet.

Because the four TIB1000 bubble devices on each HDB-11 module are operated in parallel, the performance of the bubble system compares very favorably with that of a corresponding floppy system. Each TIB1000 has two data tracks, and bubbles are shifted on each at a rate of 100 KHz. Thus, peak transfer rates close to 800 Kbits/sec are achieved between the bubble devices and the HDC-11 controller, compared to a corresponding 500 Kbits/sec for the floppy system. Furthermore, the average access time for the bubble system is only 11.2 ms, compared to about 300 ms for the floppy. As a result, the bubble system will complete an entire data transfer before the floppy has even found the data on the diskette.

The Z80-based HDC-11 controller is quiescent in a wait loop until a command is received from the host LSI-11 CPU. When the LSI-11 writes a word into the controller's command register, the Z80 interprets the command and performs the requested function. If the command is to fill or empty the data buffer, the Z80 initiates a DMA operation to transfer data between the LSI-11 memory and the controller's scratchpad. If the

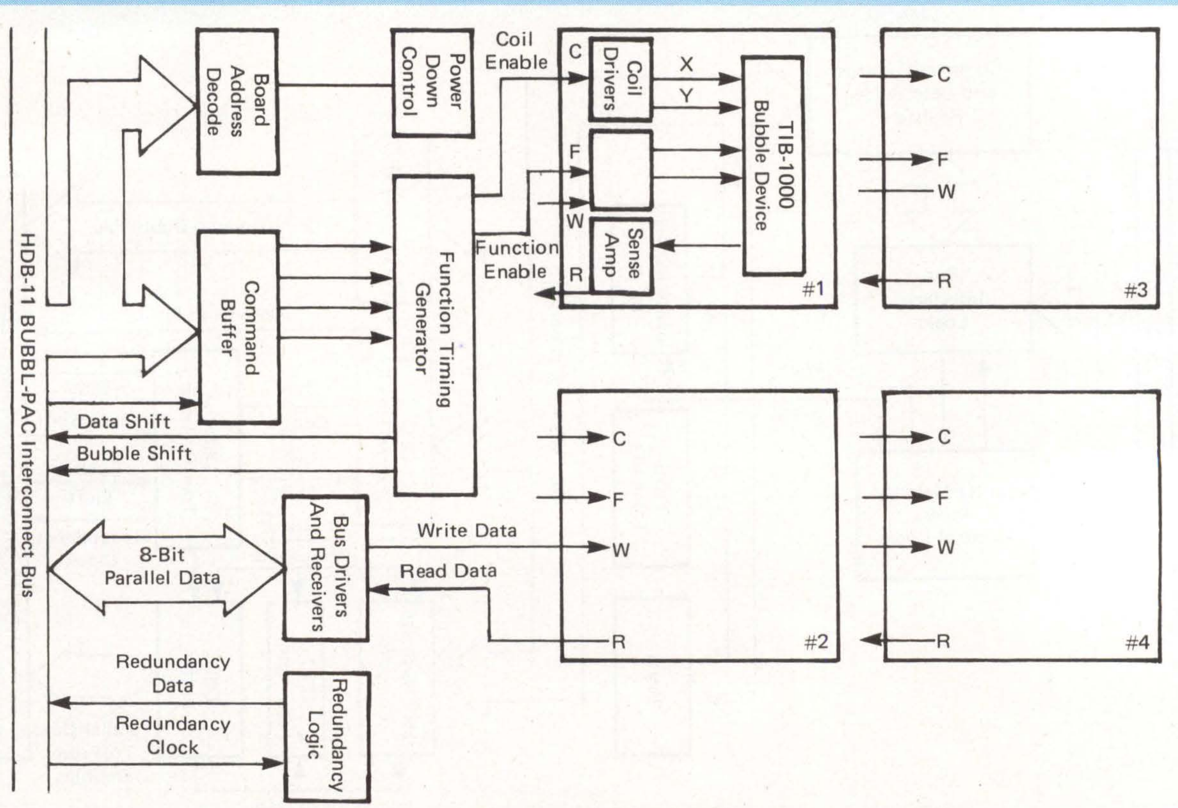

Figure BB: HDB-11 Bubbl-Pac Block Diagram

for write operations, and a serial-to-parallel conversion for read operations. The redundancy logic insures that no bubbles are created in bad loops (identified by the manufacturer during his device testing process). Thus, clock pulses to the shift register in the parallel/serial converter must be inhibited whenever the bubble loops have been shifted to a position where a defective loop is available to be written into or read from. This requires that the serial/parallel converter be unique for each bubble device, since the bad-loop information for each is unique.

Two different methods are widely used to store the information concerning the bad loops in each bubble device. One technique is to store the information in a PROM whose address bits are generated by a counter which is stepped at the

High-Performance Bubble-Memory System

command is to write a sector into bubble memory, the Z80 requests a track and sector address, converts this address information into a bubble-memory page address, and then transfers the data to a special data buffer before it is written into the bubble devices.

Because each bubble device contains bad loops that must not be used, the write-data must be conditioned by redundancy logic to prevent writing bubbles into defective loops. This is accomplished during the transfer of data from the scratchpad to the bubble buffer memory. The data is loaded into a shift register by the Z80 and serially shifted out at a 1 MHz rate. A PROM on the addressed HDB-11 contains a zero at each address corresponding to a bad loop in a bubble device, and is accessed synchronously with the bubble shifting. When a zero is encountered in the PROM, the logic inhibits the shift pulse and writes a zero into the buffer memory at that location.

After the data has been transferred to the buffer memory, the Z80 issues commands to the module to shift the bubble devices the required number of bit positions to access the appropriate page of stored data. Commands are sent to the module via a FIFO memory. A command from the FIFO is loaded into a command register on the module each time a bubble-shift counter overflows. The shift counter is stepped by pulses produced at the 100KHz bubble shift rate by the Function Timing Generator on the HDB-11. The number of shifts between overflows of the counter is programmed by the Z80 in preset register contained in a counter/timer device on the HDC-11 controller.

A read operation is the converse of the write operation. The Z80 obtains a track and sector address, converts it to a bubble page address, reads the data into the data buffer from the bubble device, removes redundant bits, transfers the data to scratchpad memory, and awaits an empty-buffer command from the host.

Each TIB1000 page stores 34 bytes of data. Because eight pages are transferred in parallel, an entire 256-byte sector can be transferred in a single bubble-access operation. Addressing and error-detection checkwords are stored in the extra 16 bytes not needed for data. D bubble loop shift rate. Another is to store the bad loop information in a special "boot loop" in the bubble device itself. The boot loop is read by the controller during power-up and the information is then stored in a small RAM device. Each technique has its advantages and disadvantages, and both require about the same amount of controller logic to implement. The boot loop usually requires that the designer employ the unique support chips provided by the bubble device manufacturer, since these chips include the logic required to read the boot loop. The boot loop also has the disadvantage that a separate RAM device must usually be provided for every bubble device, or a single RAM must be re-loaded whenever a new bubble device is about to be accessed. On the other hand, the PROM-stored redundancy information technique has the disadvantage of requiring a special PROM-programming operation for each bubble system during the manufacturing sequence.

The Function Timing Generator provides the control pulse sequencing and duration. It is typically implemented with a counter stepped at a 4 to 16 MHz rate, a ROM, an output latch and associated enable gating. The device receives enable signals from the controller to determine which pulses are to be produced during the bubble shift cycle. In some cases the Function Timing Generator may be built directly into the controller device.

Coil Drivers provide the controlled currents to the orthogonal coils in the bubble devices which are required to shift the magnetic bubbles around their respective loops. Control signals are received from the Function Timing Generator with correct phasing to turn the Coil Drivers on and off with appropriate timing. The Coil Drivers provide a voltage step with a fixed amplitude which is integrated by the coils to provide a current ramp with peak value on the order of 400 to 800 mA. The driver outputs are clamped by Schottky diode bridges to prevent voltage excursions beyond the upper and lower power supply rails.

PC board layout of the high-current coil-drive circuitry is important, to insure that excessive noise is not created in the control-logic and bubble-sense functions.

The Function Driver(s) supporting each bubble device provide the precise current pulses required by the various R/W coils in each device. In some cases these currents are even varied in amplitude by temperature compensation to account for the fact that the optimum bubble-generation current decreases at higher device temperatures. The timing for each read and write pulse is received via TTL-level pulses from the Function Timing Generator. As in the case of the coil-drive circuitry, close attention must be paid to board layout to avoid noise caused by high-amplitude circulating currents.

The most critical element in the bubble-support circuitry, the sense amplifier, receives differential inputs from "live" and "dummy" bubble-sense loops in the bubble device. The sense amp must have high common-mode rejection (CMR) because it must detect signals with only a few mV of amplitude, when operating close to the high-current circuitry required to shift, write and read bubbles. The amplifier usually consists essentially of a comparator and output latch. The comparator output, strobed into the latch at a precise time in the bubble cycle, determines the presence or absence of a bubble under the "live" read loop.

Physical layout of the bubble-sense circuitry is critical to overall bubble-memory system performance. Careful routing of all low-level signals is required if the best system error-rate performance is to be achieved. Shielding of the sense amplifier inputs may also be required to avoid the possible effects of external noise pulses.

system-level design considerations

At the system level, designing bubble-system power supply and power-fail detection circuitry is crucial to overall system performance. High peak currents of precise amplitudes must be present during bubble-shifting operations. If the power supplies are out of tolerance, the coil drivers may not produce sufficient energy to completely shift the bubbles to their next position, and the phasing may be incorrect for proper bubble detection.

If the bubbles are shifted while the power supplies are not stable during power-up or power-down, bubble device data may become scrambled. In the case of a read-restore type bubble device, data must be restored in the minor loops after a read operation. If the major loop is not correctly aligned because of insufficient energy in the drive coil, data may be inadvertently transferred into bad loops, thus creating hard errors that can only be eliminated by erasing the entire device with a calibrated external permanent magnet.

To eliminate the possibility of scrambled data during power-up and power-down, support circuits must be disabled during periods when power supplies are not stable. The controller must be given adequate warning of an impending DC power failure so that the current operation can be completed or aborted before the power supplies go out of tolerance. This warning is normally given by a special circuit which monitors the AC power line and asserts a power-fail signal if a missing AC cycle is detected. Power supply design must assure that DC power will remain within tolerance for a period of time on the order of 1 to 15 ms after loss of AC power.

testing bubble memory systems

Since one main reason for using bubble memory is to achieve the high reliability expected of solid-state mass storage, each system must be thoroughly tested to assure weeding out weak components. Diagnostic software should be run at the temperature extremes expected in normal system operation to certify the bubble devices. Operation at the extremes of the specified power-supply levels should also be tested. Burn-in and temperature cycling is also advisable to assure high system reliability.

Each bubble device type is most likely to make errors in the presence of unique "worst-case" data patterns. Diagnostic software employed in testing memory systems should take advantage of this information to quickly find bad devices. D

Circle 19 on Reader Inquiry Card

Single Board Computer Microsystems

Charles Brabant

How do you protect investments in tooling-up to achieve greater speed and efficiency in developing μP — driven products? Both goals involve capital outlay and engineering cost considerations, intermixed with subjective perceptions.

representative example

In developing products using MCS-80, -85, -86, Z80, MCS-48 and other families, remember that over 20,000 Intellec development systems are installed — mostly MDS-800 models and Series II. The former supports a plug-in CRT display and keyboard terminal and floppy disk drives alongside other computer peripheral equipment and such specialized μP tools as PROM programmers. Series II is packaged differently, with an integral CRT and single density diskette drive housed with electronics. Other separate, stackable cabinets house the add-on dual floppy and hard disk drives needed in advanced development work. Due to this popularity, many ancilliary manufacturers make Multibus compatible products, largely with board-level, general purpose SBC implementation. Such microsystem products have an endless list of applications and expansion possibilities, in which Intel's Multibus standard is a de facto Common Denominator between SBC-type and development systems, irrespective of the type or the source of the CPU chip and its related companion devices. Added to this commonality of bus structure is the economic reality that thousands of 8- and 16-bit SBC and development systems are linked together and integrated vertically via the Multibus into Intel's Microsystem 80, up through to the 432 micromainframe processor family. Although this move was anticipated by industrial microsystems users, it will impact other economy sectors.

Charles Brabant is Technical Marketing Manager for Zendex Corp., 6680 Sierra Lane, Dublin, CA 94566

multibus

Here are many of the technical-use aspects of the Multibus spec. It has . . .

- been in use for over five years in SBC and development system products
- become an IEEE proposed standard (796) for industrial and commercial use
- well defined interface characteristics (pins, signals, protocols and waveforms)
- modular expandability to meet a wide range of application requirements
- a data rate of up to 5 million words/sec i.e., a high performance rating
- compatibility with 8- or 16-bit transfers, with both present in the same system
- direct addressing up to 1 MB which is being extended to 16 MB and beyond
- a backplane with connector pin assignments grouped for adequate power, bus control, address, interrupt and data signals. Memory & I/O have independent address spaces.
- compatibility with multiple board multi-master and multi-slave combinations
- over 70 manufacturers currently producing Multibus products and systems
- flexibility and low risk in using low-cost expansion products available off-the-shelf.

Selecting Multibus rests on its interfacing hardware features with compatibility both upwards and downwards to satisfy present and future development needs. Use of the bus can be scaled to the project using a modular building block approach both for tooling and for operations. This is not only suited for engineering design and development service, but also for production, field and repair depot servicing and in assembling new systems for sale with a common bus structure and communication links.

implementation

For this example, a design with clean short bus wiring, low capacitive loading and immunity to noise would be ideal. We recently announced such a backplane in its nine-slot cardcage. ZX-609 incorporates Multibus access parallel priority resolution circuitry mounted on sockets on the PCB, thus eliminating need for hanging TTL encoder/decoder in the air or for placing these chips on otherwise valuable baseboard real estate, replicated needlessly several times over in SBC baseboards. Removing IC chips from their sockets permits either parallel resolution technique on-board the SBC baseboard or implementation of a serial or daisy chain technique for resolving bus access contention. At maximum transfer rates, the latter is limited to three masters because of propagation delays in the serial chain. Also, empirical observations indicate that nine slots may be optimal with respect to reflected noise on Multibus. Underestimating system expansion needs in development systems is usually costly. At least one system with a triple independent bus structure which includes the Multibus provides a 14-slot capacity. Other systems commonly provide 8 slots, usually by interconnecting two modules of 4 slots. In considering the assortment of design aids and development tools, such as in-circuit-emulators, that can be plugged into the development system, nine is a useful number. If the cardcage is full, a handy, quick-fix Multibus extender socket for these systems plugs into the last slot of an otherwise full cardcage, adding one more baseboard card on the Multibus.

software

Unless one wishes to jump right into the "user-friendly," menu driven, sophisticated generation of software support — which currently is still expensive in comparison to utilitarian, assembly language and industry-standard DOS — the choices are either ISIS, the Intel System Implementation Supervisor or CP/M 2.2 OS from Digital Research Inc. for 8-bit μCs, which will serve well with the starter development system. Each has its attendant editors, assemblers, linking, loading and other utilities and myriad high level languages for creating new computer applications programs. Programmers spend about 80% of their development time using the editor program. A critical assessment of both the editor and the OS, particularly with respect to file handling efficiency, may be important to the user. For the purposes of this article, however, suffice it to say that selection of the most efficient software development system support package remains largely subjective, despite the wide disparity in the initial cost in licensing fees for such packages. A total life-cycle cost analysis and performance studies of various product offerings will reveal comparison criteria. Apply them to your individual circumstances.

If you are a novice software user, investigate before investing heavily in software (and hardware) over which you have little or no control. Is this overcautious? Perhaps. Don't take it as a blanket indictment of the many fine sophisticated software systems offerings. It takes time to learn software intimately. In approaching μP software and hardware for the first time, there is no substitute for building up knowledge step-by-step of the subject and its peculiar tools, as well as for keeping up to date.

"Has adequate analysis and planning preceded the decision to acquire a development system? Is it efficient for designing and developing μP-based products? No matter which choice you make, it pays to shop around. Finally, if a capital equipment budget is not there, leasing and rental opportunities can expand your options. **D**

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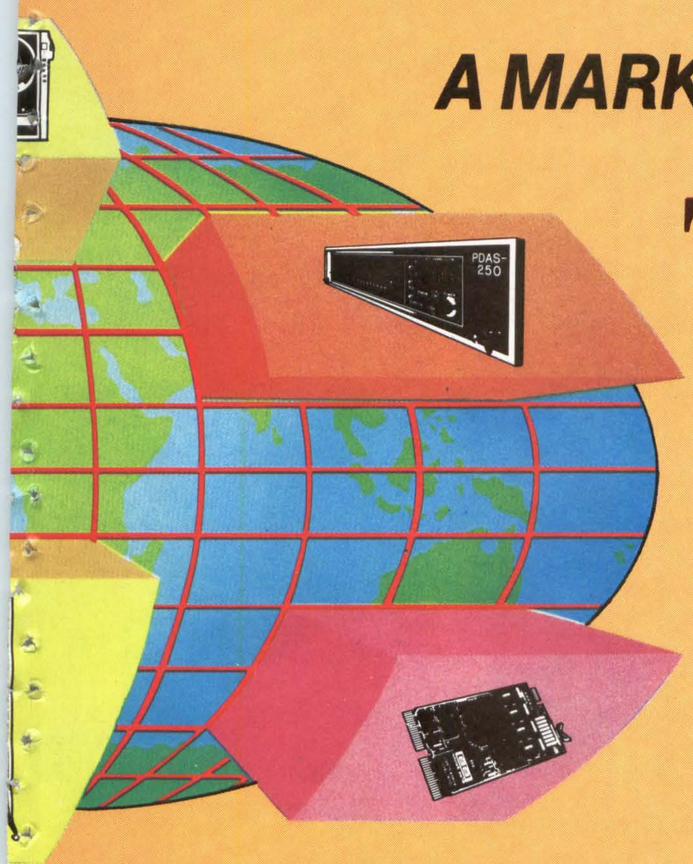

A MARKETING FORUM for CEMs

This exposition is dedicated to the proposition that the unprecedented growth and expansion in the use of computers for all kinds of applications will continue at an exponential rate. No one company can solve everyone's applications problems; no one company can supply everyone's needs for complete systems, add-ons, peripherals and software.

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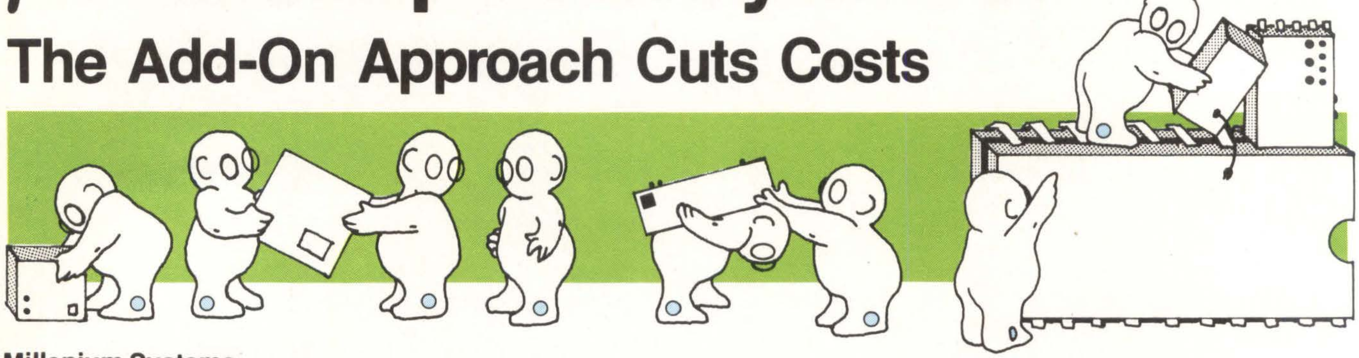
μP Development Systems:

The Add-On Approach Cuts Costs



Millenium Systems

Next-generation development systems, though universal and multi-user oriented, are costly. An alternative approach exists by which such networks can be assembled economically around a commonly used minicomputer.

Universal development systems are costly. But there is a solution: existing single-user development systems can be expanded into universal systems with a limited multi-user capability. And minicomputers, with multi-user operating systems and resources, can be turned into universal, multi-user development systems. Often, the user can make these transformations at a fraction of the cost of the bundled systems through an add-on approach to system expansion.

The integration process is straightforward enough, and can be quite effective. Unfortunately, today's more-sophisticated μP-based systems require the attention and talents of both hardware and software specialists. As you know, it is common to see two separate teams working in parallel on a single project, with each member of each team requiring the use of the resources of the development system at one time or another. But a single-user system supports only one user at a time. Thus, addition of support capability really means additional development systems, with a concomitant large overlap of development capability. Yet still, all of the resources of a given system will be tied up when any one of its features is in use.

multi-user networks

Tektronix and Millennium made an early attempt to remedy single-user system's problems with their 8001 and 8002 development labs. The 8002 was the first universal development system, but it was still a single-user system. The 8001, however, was developed as a stand-alone, in-circuit emulator and could be down-loaded from the 8002 software development system. So, software developed on the 8002 could be transmitted to the 8001 for execution and debug, and the 8002 was then free for further software development work.

The later universal, multi-user development networks — as from GenRad and Hewlett-Packard — are a major evolutionary step beyond Tektronix's earlier efforts. They provide shared central resources, which reduce the need to duplicate costly system parts such as mass-storage, memory, and printers; they provide software development stations for source entry, editing, and assembly; and they provide hardware development stations, which include in-circuit emulation for hardware debug and hardware/software integration.

Each such development station provides the capabilities of a single-user development system, but at a total cost that can be less than the cost of an equivalent number of single-user systems. And the networks provide universal support for the most popular μPs, with both cross assemblers and in-circuit emulation.

But development networks are sold bundled and so the total system's price can be quite high, even though the potential cost per station is moderate. Still, if the user wishes to start with only a single development station, his entry price will be significantly higher.

the add-on alternative

The common theme underlying both the single-user system and the multi-user network is that each calls on a general-purpose computer for basic software development. Thus, if a user has either a single-user development system or a minicomputer, he has the start of a universal, multi-user development network. And he can build one that will compete favorably with those offered by the instrumentation suppliers, but with one additional feature — it will be affordable.

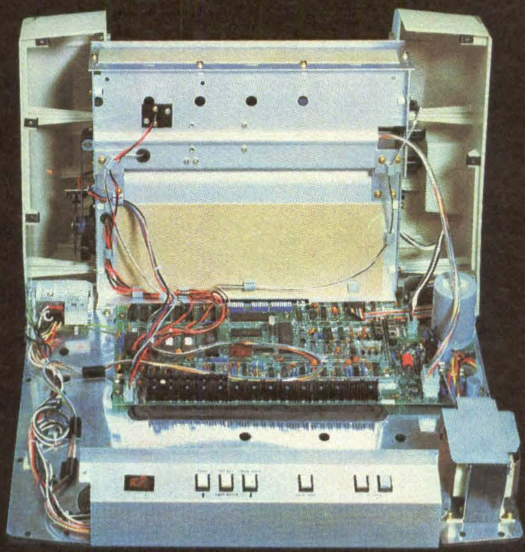
Now, the elements of a general-purpose computer system that are common to development systems are the computer itself, the terminal, mass storage, text editor, and file manager — these are the elements needed for source entry and editing. They are unique neither to a particular μP nor to the μP development support in general.

Translation of source code to object code, however, does require a cross assembler that supports the target μP; actually, a cross software package is needed. A reasonable package for today's product needs includes a relocatable macro cross assembler, a linking loader, a formatter (to put the linked program into a format that can be sent to an in-circuit emulator), and a communications link driver for communications with the in-circuit emulator. By adding this software to a general-purpose computer, the user can develop his applica-

Subsidiary of American Microsystems, Inc. 19050 Pruneridge Ave., Cupertino, CA 95014

Illustrated by Jacky Brill

Say Ahh...



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tions software from concept, through assembly, to linked modules ready for execution and debug.

add-on in-circuit emulation

Debugging requires a controlled environment. While the just-developed software and the hardware prototype could be combined, the probability of their operating properly together is essentially nil. And the task of identifying and correcting the bugs is monumental; it increases with increasing system complexity, and at a faster rate.

The best debug solution is an add-on in-circuit emulator. It provides a way to debug new software as far as possible before being run on unproven hardware. It also can show that the new hardware does operate to at least some degree, before it is integrated with the application software. Furthermore, the in-circuit emulator provides a point in the debug process where one element, the μP kernel, can be assumed to operate properly. And, from the in-circuit emulator, the debug process can extend into the hardware or software. In-circuit emulation provides control and monitoring of the program flow; it vastly improves debug capability via user-directed stimulus and response.

Unfortunately, very few companies offer add-on in-circuit emulation units, even though this approach to development systems is economically and technically attractive. We are the major supplier,so we will use our MicroSystem Emulator (μSE) and MicroSystem Designer (μSD) as examples of add-on in-circuit emulators.

Remember that the initial debugging of either hardware or software doesn't usually require the full capabilities of a software development system or an integration station. The major requirements are for an "intelligent front panel" — to monitor and control prototype systems operations — and RAM program memory, for the entering and execution of short driver programs. The MSD provides these basic functions in a very low-cost instrument. In addition, because its I/O resources are available to the program being debugged, the MSD eases software debug sans prototype.

The final integration of hardware and software, however, does require the resources of a software development system, as well as an in-circuit emulation instrument with expanded capabilities — real-time trace, complex trigger and breakpoint definitions, etc. The μSE provides such support in a full hardware/software development station.

integration via add-on in-circuit emulation

The μSE permits applications programs to be downloaded into its program memory from a software development system; they are then executed within the prototype hardware. Once debugged in this mode, the program can be moved into the prototype system itself for execution. This is done by burning PROMs that plug into sockets within the prototype hardware; the program then executes from the PROMs, but is still under control of the μSE. Alternatively, the user can map the μSE's emulation memory over the memory space of the prototype system, and control program execution from μSE memory.

In such a configuration, the host computer stores the application software prior to integration, edits source code when software bugs are found, and reassembles the program. It also links, formats, and downloads application programs to the μSE for execution and debug. But the μSE controls the actual program debug. Thus, if desired, the link between the host computer and the μSE can be broken after the downloading. The link can be reestablished whenever subsequent editing is required.

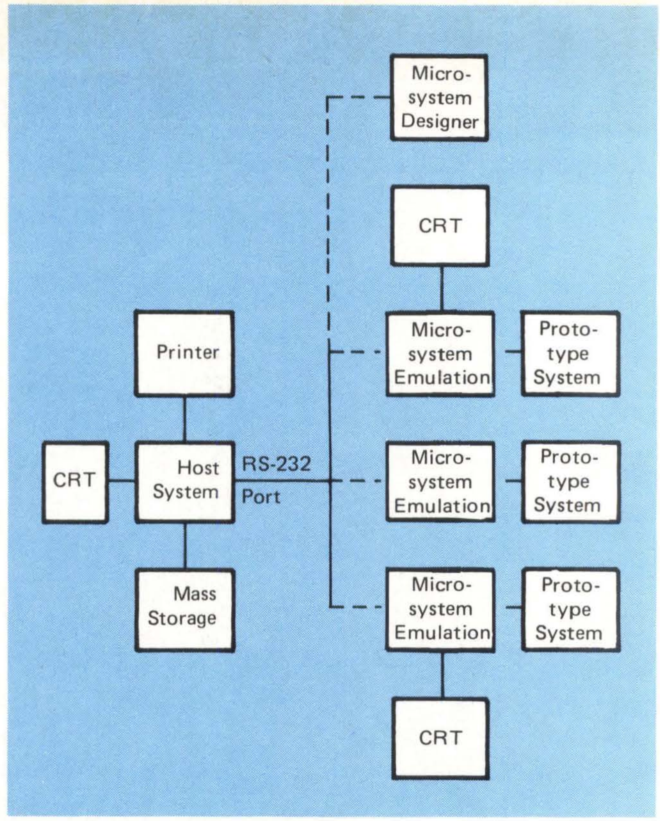


Figure 1: The host system — originally a single-user, dedicated development system — has here been expanded to a multi-user, universal system through add-ons, and, if desired a MicroSystem Designer. The configuration makes use of the host's resident development software, but requires the addition of a cross package. The host's resident operating system can support only one CRT terminal, so only one software development station is possible. Multiple hardware development stations are possible, however, because of the stand-alone capabilities of the MicroSystems Emulators. The RS-232C link is needed only to transmit programs to the Emulator. Once the programs are sent, the link can be broken.

from single-user to multi-user

With these things in mind, we can describe the conversion of a single-user minicomputer — or a single-user development system — into a multi-user development. If the single-user development system happens to be dedicated, the conversion will turn it into a multi-user universal system.

Let's consider a dedicated single-user development system that's been expanded to a universal development system; the resident single-user operating system supports only one CRT terminal, so only one software development station is possible. Multiple hardware development stations are possible, however, because of the stand-alone capability of the μSE units.

Software development makes use of the host system's resident text editor, file manager, and mass storage. Remember, to translate from source to object codes, link application program modules, and download programs to the μSE for execution and debug, a cross software package must be added. (Millennium, among others, offers such a package for most major μPs. Some are written in Fortran, and these can be installed on a minicomputer having a Fortran compiler; others are written in the native language of popular minicomputers and development systems.)

Hardware development is normally done through in-circuit emulation with stand-alone μSEs. If programs are required, they are transmitted from the host system to the μSE via an RS-232C serial port: the μSE is connected and the program transmitted after which the μSE may be disconnected.

System integration — again using in-circuit emulation — requires both the software development station and a μSE. In one integration procedure, the μSE is connected to the host system's RS-232C port, and remains connected throughout the integration process. In this case, software changes are made quickly, using the host's editor and assembler, and checked out immediately in the μSE/prototype hardware.

In a second integration procedure, software is downloaded to the μSE, then the link is broken. Integration proceeds with the μSE operating in a stand-alone mode, with temporary patches made to correct software bugs. When patching becomes difficult to manage, the host system can edit and reassemble the program. The RS-232C link is reestablished, the program downloaded, and the link broken again.

Of the two integration procedures, the first is more productive for a single task, but the second may be more productive when several tasks are involved. The first is, in effect, a single-user system; the second is a limited, multi-user system. The latter allows software development to proceed on the host and hardware development to proceed on stand-alone μSEs, while system integration proceeds on other μSEs. A potential disadvantage is that operations on the single-user host must be interrupted whenever editing and downloading are needed. Further, changes in application software take somewhat longer to make.

from multi-user mini to multi-user development system

If the host system supports multiple users and multiple ports, it needn't be interrupted; a typical configuration would be a Digital Equipment Corporation PDP-11 or LSI-11, with an RSX-11 operating system. Such a system has characteristics almost identical to those of a bundled development network — except for price. A software development station is simply a CRT terminal, so stations can be added to this network for less than $1,000 each. With the addition of a μSD, the

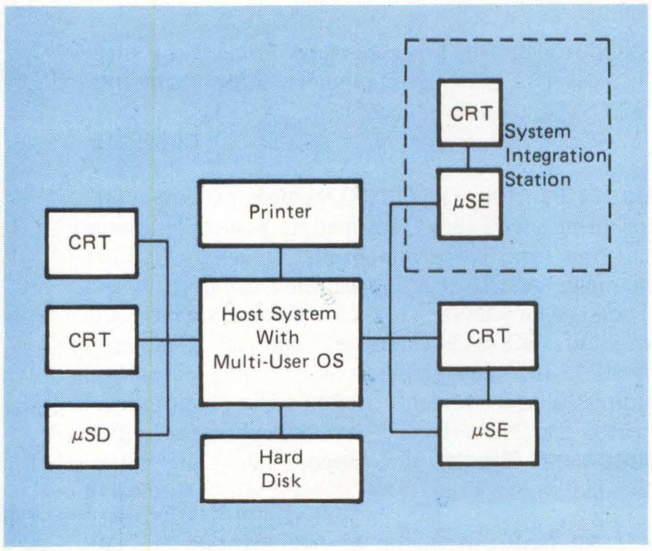


Figure 2: This is a full capability, user-created, multi-user, universal development system. The host system is a mini that can support multiple ports and multiple users — a PDP-11 or LSI-11, for example. Here, a software station is simply a CRT terminal; a hardware station is either a MicroSystem Designer (μSD) or MicroSystem Emulator (μSE), which may or may not be connected to the network. The system integration station is merely an Emulator and a CRT terminal on a common RS-232C port. The power of such a system is essentially identical to that of a bundled network — yet offers a significant economic advantage over the commercial system.

software can execute and debug developed code in a target environment.

A hardware development station is simply a μSE or μSD, which may or may not be connected to the network, while a system integration station is a CRT terminal and a μSE sharing a common RS-232C port. And the total number of stations supportable depends only upon the capabilities of the host system.

Moreover, the development functions possible at each station are, in essence, identical to those for a single-user system, except that they will all operate simultaneously.

Assume a host system can support four RS-232 ports under a multi-user operating system. When converted, it can support four software development stations, or four system integration stations (remember, each port can support both a CRT and a μSE), or any combination; and a software development station becomes a system integration station simply by the addition of a μSE. Thus, there is a tremendous amount of flexibility in this configuration.

Now, the cross software that operates on the single-user system is also applicable to the multi-user network. It's simply placed under the control of the multi-user operating system so that any software development station can access it. Source code entry, editing, assembly, formatting, and downloading are done in the same way as on a single-user system, but at each station independently.

The power of such a system may encourage ambitious projects. So the host system's resources must be adequate to handle peak demands. Thus, consider a hard disk for mass memory, rather than floppies; and perhaps add internal RAM to reduce the need for overlays. Of course, a minicomputer is designed for upgrade, and so is easily expandable to support growing needs.

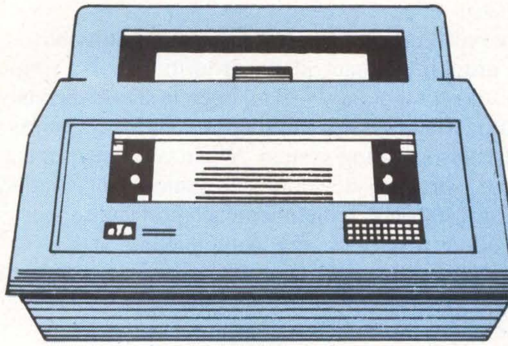
cost savings

What are the comparative costs for a bundled, multi-user network and one user-created through add-ons? Consider a typical configuration: central resources, two software development stations and two hardware/software development/system-integration stations.

Prices do vary somewhat between instrumentation suppliers; but central resources and one software development staton will cost $20,000, typically. A second software development station will add $11,000; hardware/software stations, $18,000 each. The bundled network, exclusive of cross software, totals $66,000.

An equivalent, user-created, add-on system will need four CRT terminals and two μSEs. Assuming that no terminals are available on the host system, four CRT terminals will cost $4,000 (actually they will cost less than $1,000 each). A μSE, including one emulator module, costs about $7,000, so two will add $14,000. To add code execution capability to one software station requires a μSD with a personality module, at only $2,000. Thus, the total cost to build a four-station development network from an existing mini is about $20,000. This does not include cross software, or any upgrading to the host system.

Suppose, however, that it's necessary to buy everything — the add-ons and the host system. A typical system would be an LSI-11/23 and a 10MB hard disk, RSX-11 operating system, and Fortran. Such a system will cost about $30,000. Adding this to the $20,000 above gives a total cost of $50,000 — very reasonable, when compared to the bundled system. And for the money, you get not only a multi-user, universal development system that is easily and economically expandable, but a general-purpose computer system capable of many other data processing tasks as well. **D**



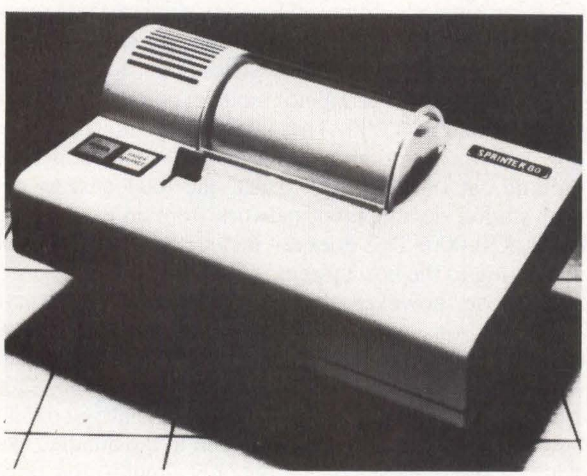
Printer Showcase Part II

Part II of the Printer Showcase is a continuation from the March 1981 issue of Digital Design. A representative model from each company is described. Additional models are available from most manufacturers. The second part of this Showcase lists Printer Components, Mechanisms, Controllers, Supplies, etc. Circle numbers on "Reader Inquiry Card" to get more information from the company. If your company manufactures printers or printer components, and is not listed here or in the March 1981 issue, let us know so we can include you in future listings. Write to Showcase Editor, Digital Design, 1050 Commonwealth Ave., Boston, MA 02215.

Printers

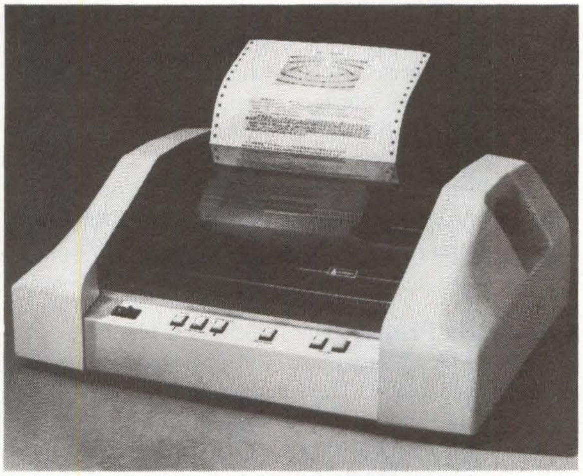
Dot Matrix Thermal Printer. The Sprinter 80 is a compact, 80 column, 5×8 dot matrix unit featuring user selectable parallel or RS232 serial interface, 8 selectable baud rates from 110 to 9600 bps, selectable character or graphics mode and software controllable print speeds from 2 to 4 lps. Using 560 × n matrix, up to 240 full 80 character lpm are possible. 96 character ASCII, roll and fan fold paper feed. Primarily for small business and personal computers. **Alphacom Inc,** 2323 S. Bascom Ave, Campbell, CA 95008.

Circle 215.



Matrix Printer. The GP300 includes maximum 300 cps print speed in a 9×9 matrix. Switch selectable baud rate from 300 to 9600 baud. Character set is a 141 character ASCII, U&L case (includes foreign and special characters). Gothic and data quality sets standard. RS-232 interface, optional Centronics parallel. Includes graphics and plotting capability, bidirectional movement, friction paper feed (optional tractor and sheet feeder) and 380 chacacter FIFO. **Amperex Electronic Corp,** 230 Duffy Ave, Hicksville, NY 11802. **Circle 216**

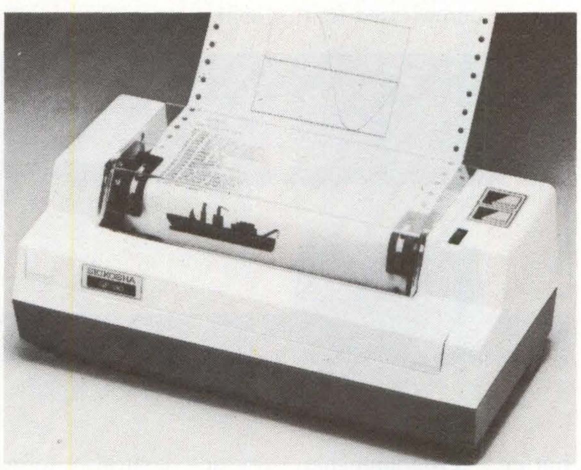
80/132 Column Serial Matrix Printer. The DP-9000 grafixPLUS printer includes a universal interface providing RS-232C, current loop and parallel interfacing. 96 character ASCII with descenders and underlining. Bidirectional up to 200 cps. High density graphics. 700 character FIFO storage buffer, optional 2K buffer. Selectable baud rates from 50 to 9600.



Anadex Inc, 9825 DeSoto Ave, Chatsworth, CA 91311. **Circle 217**

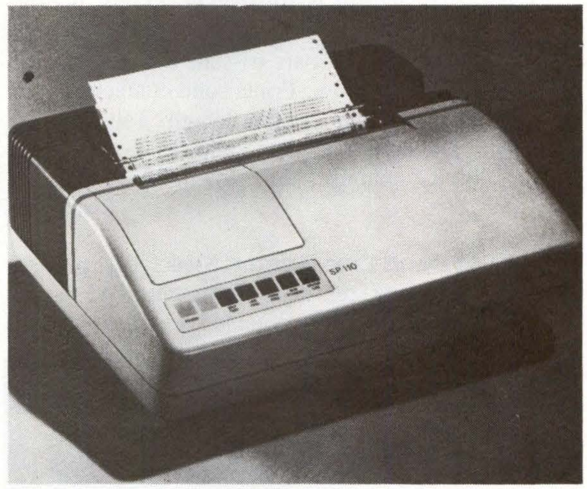
Ink Jet Printer. The quiet AJ 650 uses a drop-on-demand method of applying ink in a precise dot matrix. Switchable 80 char/line to 132 char/line with single or double spacing, 6 or 8 lpi. Under computer control it prints extended characters, boldface and U&L case. Bidirectional at 180 or 210 cps. 96 character ASCII. **Anderson Jacobson Inc,** 521 Charcot Ave, San Jose, CA 95131. **Circle 218**

Impact Printer. The GP-80M uses a single rugged print hammer to print both alphanumerics and graphics. Features include ASCII U&L case character



sets, 80 columns with 12 cpi, adjustable tractor feed, 3 copy reproduction, Centronics parallel interface. Optional interfaces include RS-232C, serial TTL, 20 mA current loop, IEEE 488, plus interfaces for most small computers. Print speed is 30 cps in a 5×7 dot matrix. Designed for the OEM and the personal and small business markets. **Axiom Corp,** 1014 Griswold Ave, San Fernando, CA 91340. **Circle 219**

Serial Printer. The SP110, for general purpose and telecommunications use, includes bidirectional printing at 90 cps, up to 136 char/line, character-mode operation, a 7×9 character matrix with descenders and underlining, condensed and expanded fonts, alternate and optional national character sets, and programmable horizontal and vertical tabbing. Prints 96



character ASCII and APL. RS-232C or Centronics interface. **Burroughs OEM Marketing,** Burroughs Place, Detroit, MI 48232. **Circle 220**

Alphanumeric Printers. The P2010 with RS-232C interface and the P2020 with IEEE 488 interface, feature two color, 31 column printout with mixed characters, 7×7 dot matrix and integral paper feed. Print rate is 2.4 lps, 64 character ASCII, 31 char/line in black and red. **Canon Business Machines,** 3191 Red Hill Ave, Costa Mesa, CA 92626. **Circle 221**

Electrosensitive Matrix Printer. The 912 series employ a 9×12 matrix with 225 cps, 170 lpm print speed. From 110 to 4800 baud. 96 character ASCII with optional Foreign character sets. Friction paper feed. Memory includes 256 bytes standard, 2K bytes optional. The 912-S uses an RS-232 serial interface; the 912-P, an IEEE 488 parallel; and the 912-GPP a Centronics parallel interface. A graphics only model, the 912-GO, is also available. **Comprint Inc,** 340 E. Middlefield Rd, Mountain View, CA 94043. **Circle 222**

Single Part Form Printer. The 708-0033 prints a 2″ wide, continuous fanfold ticket of variable length. Speed is 20 col/sec. This rotating drum impact printer with fully formed characters employs an integral ticket cutter and provisions for color stripping or logo stamping. OCR or bar code characters are available. **Computer Terminal Systems,** 65 S. Service Rd, Plainview, NY 11803. **Circle 223**

Checkprint Systems. These systems print checks and other MICR documents on a special computer driven printer under software control. Variety of throughput speeds and options. **Data Card Corp,** Troy Div, 2331 S. Pullman St, Santa Ana, CA 92705. **Circle 224**

Universal Interface Printer. The 722UA accepts 20 mA loop, RS-232, ANS/IEEE 488 and a BCD input. All interface lines are tri-state but may be hard wired active high or low. Prints solid characters at up to 2400 lpm, 22 character line length. Table or rack mounting. **Datadyne Corp,** Valley Forge Corporate Center, 960 Rittenhouse, Norristown, PA 19403. **Circle 225**

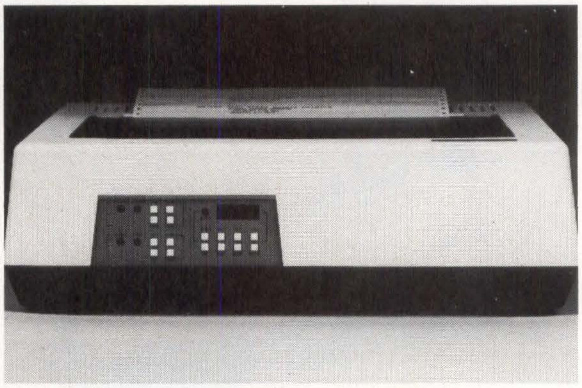
1200 LPM Band Line Printer. Model 3121 prints at 1200 lpm or at 600 lpm, for draft-quality WP output with an optional switch selectable speed feature. This

132 column unit includes over 40 digital display symbols, a low-cost spool ribbon system, a full line buffer, below 65 dBA noise level, operator interchangeable 48, 64, 94 and 128 character bands, and vertical and horizontal paper adjustment. The 3121 offers high speed and durability with the flexibility and low-cost of band printers. Options include 136 columns, cassette ribbon and ribbon re-inking system, forms length selection switch or direct access VFU, an 8 or 12 channel electronic VFU tape reader and numerous font options. **Data Printer Corp,** 99 Middlesex St, Malden, MA 02148. **Circle 226**

Band Line Printers. The B-900 prints at 900 lpm. A 64 character ASCII set is standard with optional, user specified character sets available. Features Dataproducts parallel interface, optional long line, paper puller feed, bit-slice μP control and line buffer memory. The B-1500 prints at 1500 lpm, 48 character set standard, up to 96 characters available. Includes the same features of the B-900. **Dataproducts Corp,** 6200 Canoga Ave, Woodland Hills, CA 91365. **Circle 227**

Dot Matrix Printer. The IPS-5000-C featurers open-ended DMA architecture for potentially unlimited memory expansion. The standard unit contains 12K of EPROM and 4K of RAM. Standard features include 165 cps at 10 cpi, 285 cps at 17.2 cpi, selectable print styles, control panel, self-test, hex trace, graphics, programmable VFU, horizontal tabs, 500 character FIFO buffer and 6 or 8 lpi spacing. Options include expandable buffers and international character sets. 80 and 136 column versions available. **Dataroyal Inc,** 235 Main Dunstable Rd, Nashua, NH 03061. **Circle 228**

Dot Matrix Impact Printer. The DS180 utilizes 180 cps bidirectional printing in a 9×7 matrix. Includes 96 character ASCII, 132 column line at 10 cpi. Adjustable tractors handle 3-15" wide, up to 6 part forms. Interfaces are RS-232, 20 mA current loop and Centronics compatible. Baud rates from 110 to 9600, tractor paper feed, 1000 character printer buffer and non-volatile memory for format retention are standard. Options include compressed font, graphics capability and 2K



buffer. Programmable keypad controls forms handling. **Datasouth Computer Corp,** 4740 Dwight Evans Rd, Charlotte, NC 28210. **Circle 229**

Miniature Thermal Printers. The APP-20-1 is a 20 column, alphanumeric, panel-mouted unit. It prints 96 character ASCII (U&L case) at 1.2 lps on a 5×7 dot matrix. Parallel data input, built in AC or DC power supply, μP control of printing and stepper motor.

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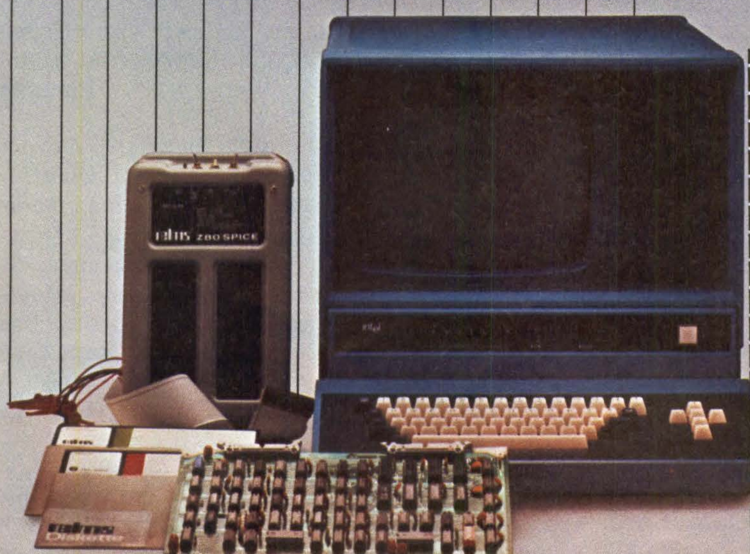

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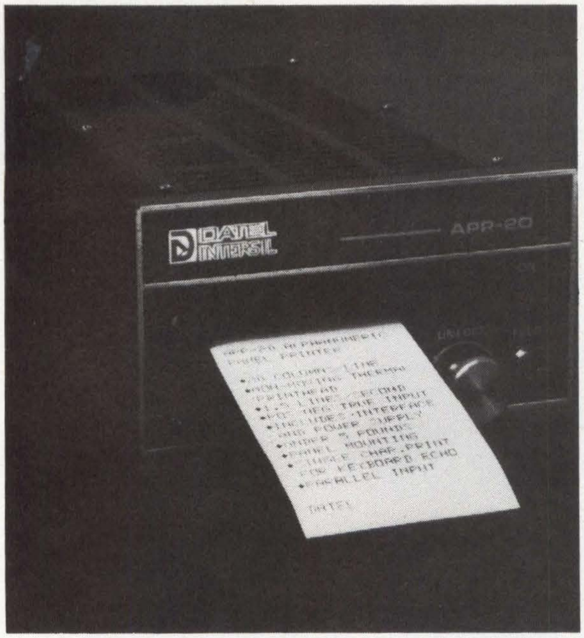


Features inverted or extra-height character printing, single character and keyboard echo printing. Accommodates 2.31" wide thermal paper at 20 col/line. The APP-20-2 is a serial input version which can accept RS-232C or 4-20 mA serial data inputs. It also includes a one line internal buffer. Both measure approx. 4"W × 3"H × 9"D. A 48 column version is also available. **Datel-Intersil,** 11 Cabot Blvd, Mansfield, MA 02048. **Circle 230**

Serial Matrix Printer. The 6541-04 interfaces with IBM systems. Speed is 150 cps with a 96 character ASCII, optional character sets available. Includes bidirectional movement, tractor paper feed and buffer memory. **Decision Data Computer Corp,** 100 Witmer Rd, Horsham, PA 19044. **Circle 231**

Daisy Wheel Printer. Model 630 uses either a metal or plastic print wheel interchangeably. Over 100 different type styles in 88, 92 or 96 characters available. Fully strappable power supply for domestic and international applications. Bidirectional printing from 32 to 40 cps. Variety of paper handling options. **Diablo Systems Inc,** a Xerox Co, 24500 Industrial Blvd, Hayward, CA 94545. **Circle 232**

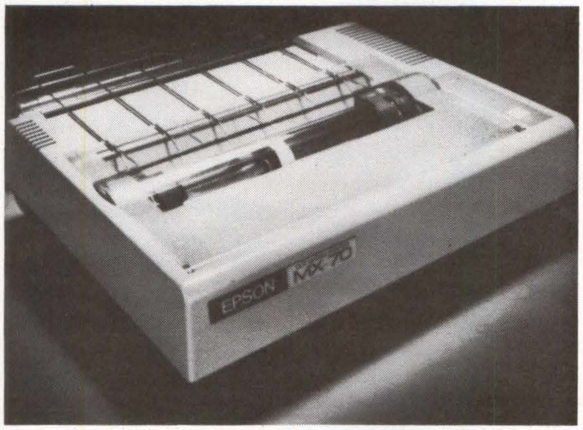
Band Type Line Printers. The 3000/3001 series print at speeds from 150 to 900 lpm. Supplied with a 64 character ASCII, optional 48, 96 and 128 character sets. Interfaces to a range of minicomputers including DEC, DG, HP and P-E. The units are μP controlled and include tractor paper feed, a one line buffer and versatile forms handling. **Digital Associates Corp,** 1039 E. Main St, Stamford, CT 06902. **Circle 233**

132 Column Smart Printer. The LA120-RA is a bidirectional, 180 cps unit that seeks the shortest print path and skips white space. Features include full duplex, half duplex, 14 baud rates, 8 split baud rates, 8 horizontal fonts, 6 vertical line selections and sets tabs/margins. Includes pedestal mount, non-volatile memory, RS-232C interface, field service, documentation and training. Options include 20 mA loop,

4K RCV buffer, APL and European character sets. **Digital Equipment Corp,** 1 Iron Way, MR2-2/M67, Marlboro, MA 01752. **Circle 234**

Dot Matrix Impact Printer. The 7000+ provides either a single width font of 40 columns at 12 char/in., or 20 columns at 6 char/in with a double font. It prints on regular paper with widths of 0.750" to 3.875" at a speed of 1.25 lps. Options include 64 columns at 19.2 char/in; 32 columns at 12 char/in; interface cables for serial RS-232, IEEE, current loop or parallel. Baud rates from 110 to 1200 baud. **Eaton Corp,** Count Control/Systems Div, 901 S. 12th St, Watertown, WI 53094. **Circle 235**

Dot Matrix Impact Printer. This low-cost unit, the MX-70, prints unidirectionally at 80 cps with a user-defined choice of 40 (double-width characters) or 80 column printing. It features a disposable printhead and



provides top-of-form recognition, programmable line feed and form lengths, a self-test mode and adjustable tractor feed. It also features GRAFTRAX II, a high resolution function for bit image graphics. **Epson America Inc,** 23844 Hawthorne Blvd, Torrance, CA 90505. **Circle 236**

High-Speed Matrix Printers. The OSP/120 and 130 models have a 600 cps print rate for draft or DP output, and up to 150 cps for letter quality output. They provide graphics, multi-font storage, fully formed characters and OCR printing and labeling in one machine. Features include versatile forms handling and automatic cut sheet feed, manual feed and tractor feed in one mechanism. Character size flexibility, graphics and plotting are printed on plain paper. **Florida Data Corp,** 600 D John Rodes Blvd, Melbourne, FL 32935. **Circle 237**

Matrix Printer. The TermiNet 2120 is a 1200 baud, multi-μP-based unit that prints at 120 cps. Size in a compact 22″ × 18-1/2″ × 5-1/2″ and weighs 24 lbs. APL/ASCII keyboard. Produces original and two copies. Paper slew rate is 5 ips. **General Electric Co,** Waynesboro, VA 22980 **Circle 238**

Impact Dot Matrix Ticket Printer. The AO 542 stores individual tickets in an internal hopper and automatically feeds them on a print command. A reprint feed slot allows printing additional information. Its full 80 character width allows printing a full CRT screen onto a ticket. Features include bidirectional printing, 120 cps speed, full 96 U&L case ASCII character set, underlining, double width print on software command, μP control, RS-232C serial, 20 mA current loop serial and ASCII 8 bit parallel interface, 8 baud rates from 110 to 9600 and a 480 character buffer expandable to 1920 characters. Choice of ballistic or conventional 9 needle print heads. **Hecon Corp,** 31 Park Rd, Tinton Falls, NJ 07724. **Circle 239**

Serial Matrix Printer. The Model 500 is a 9×9 matrix printer with 150 cps speed and up to 136 column output. Baud rate is switch selectable from 110 to 9600. Either manual selection or software control of most functions. Includes 96 character ASCII, bidirectional movement, tractor paper feed, and up to 3.4K buffer. Additional features include 10, 12 or 16.5 char/in. and 6 or 8 lpi; double width printing; vertical format control, vertical tabbing; subscripts and superscripts; descenders and underlining; and serial or parallel interface. Options include alternate character set, communication interface, auxilary control panel and expandable input buffer. **Infoscribe Inc,** 2720 S. Croddy Way, Santa Ana, CA 92704. **Circle 240**

Daisy Wheel Printer. The 40 cps Starwriter utilizes an RS-232C EIA communications interface. Offers all performance features of the 25 cps and 45 cps Starwriter models. Employs a 96 character print wheel to

produce letter-quality printing on 3 copies with either 136 or 163 columns. Compatible with sheet feeders, handles forms up to 15″ wide, includes self-test, programmable VFU and front panel indicator lamps for paper, select and power status. **C. Itoh Electronics Inc,** 5301 Beethoven St, Los Angeles, CA 90066. **Circle 241**

Serial Dot Matrix Printer. The Model 310 employs a 7×9 matrix with optional 9×9 and 9×12 matrix. Speed is 180 cps, 120 lpm with 80 char/line. It uses a 96 character ASCII with Foreign language and special character sets available. Baud rate is 75-9600 baud; EIA-RS-232C/CCITT interface. Other features include bidirectional movement, pin feed tractor paper feed, μP control and memory up to 16K ROM. Business graphics capability available. **Lear Siegler Inc,** Data Products Div, 714 N. Brookhurst St, Anaheim, CA 92803. **Circle 242**

Impact Line Belt Printer. The Quiet 300 features a 300 lpm print speed and switchable serial/parallel interface. It includes up to 9600 baud rate, 64 or 96 character ASCII, tractor paper feed and 1K memory optional to 4K. Interfaces include RS-232C, 20 mA, Centronics parallel, DEC LA-180. **Local Data,** 2701 Toledo St, Torrance, CA 90503. **Circle 243**

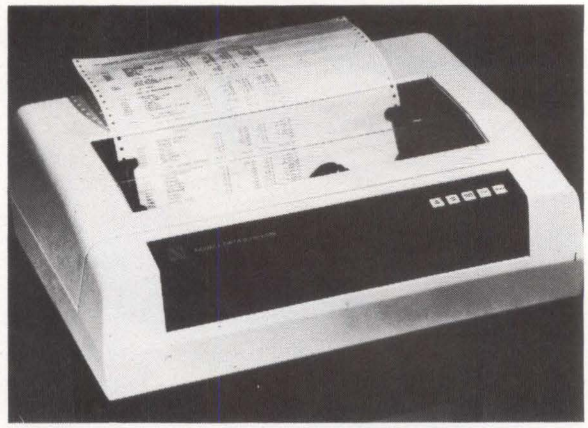
Dual Function Serial Printer. The T-1805 produces word processing letter quality characters via a 40×18 matrix at 50 cps. It can also be used in a data processing mode using a single pass 7×9 matrix for a speed of 200 cps with bidirectional printing. Proportional spacing of characters is available. Includes a low 53 dBA noise level and tractor paper feed. **Mannesmann Tally,** 8301 S. 180th, Kent, WA 98031. **Circle 244**

Alphanumeric Thermal Printer. The 20 column MAP-20S is a compact 4.5″W × 2.75″H × 7″D unit complete with μP control circuits, buffers, drivers, UART and AC power supply. It prints full 96 ASCII characters, U&L case at 115 lpm, maximum of 240 lpm. OEM programming features include print direction, buffer mode, character size, vertical and horizontal tab, backspace, carriage return and line feed. Pin-selectable data rates from 75 to 9600 baud; RS-232C and 20 mA loop interfaces. **Memodyne Corp,** 220 Reservoir St, Needham Heights, MA 02194. **Circle 245**

165 CPS Matrix Printer. Model 5126 employs a 7×9 matrix; 110, 300 or 1200 baud rate; 96 character ASCII; RS-232 serial interface; bidirectional movement; and adjustable tractor paper feed. Other features include graphics and plotting capability, 132 character buffer, host control with keyboard and parallel interface models available, μP controlled, program controlled electronic form length selection and expanded print capability. **Microdata Corp,** 17481 Red Hill Ave, Irvine, CA 92713. **Circle 246**

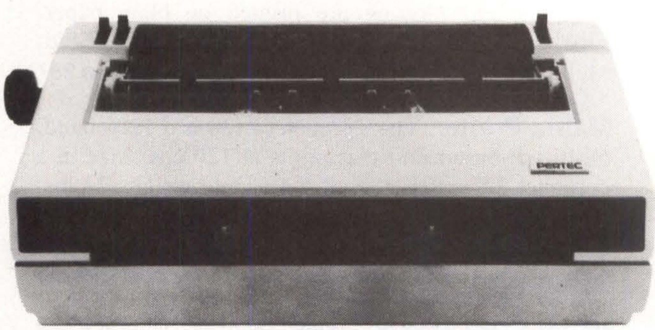
Impact Matrix Printer. Model 88G has 100 cps bi- or unidirectional printing, full U&L case 96 character ASCII, 7×7 matrix and line formats of 80, 96 or 132 columns/line. Double wide characters are software selectable. Stepper motor driven paper feed with 16 selectable form lengths. μP controlled interface accepts RS-232C data at up to 1200 baud or TTL level parallel data. Options include dot addressable graphics mode, 9600 baud, 20 mA current loop, IEEE/parallel interface adapter and 2K buffer. **Micro Peripherals Inc,** 4426 S. Century Dr, Salt Lake City, UT 84107. **Circle 247**

Dot Matrix Printer. The fully programmable Image 800 has a 150 cps print speed with a 136 column



output. Programmable functions include 6 different sizes of condensed and expanded print, variable line spacing, subscripts and superscripts, selection of 2 character sets and a programmable VFU. Includes ballistic printhead, 9×9 matrix, RS-232C or Centronics parallel interface, data rate from 110 to 9600 baud, combination of stepper motor and dual tractor paper feed and 300 character buffer expandable to 3300 characters. **Novell Data Systems,** 1170 N. Industrial Park Dr, Orem, UT 84057. **Circle 248**

Daisy Wheel Printer. The Stylist 360 is a serial, fully formed character printer with a 100 character ASCII, U&L case, symbols, proportional and OCR



type styles. Speed is 17 cps with bidirectional logic seeking. Includes automatic paper loading and alignment, modular design for easy servicing, μP control, 1024-bit buffer, below 60 dBA noise level. Available in a variety of character sizes, fonts, languages and spacing. **Pertec,** Peripherals Div, PO Box 2198, Chatsworth, CA 91311. **Circle 249**

Variable Speed Line Printer. This multi-application unit, the Taskmaster MVP2, includes operator or computer selectable print speeds of 80 lpm for correspondence quality output, 150 lpm for data processing and 200 lpm for compressed character printing.

Includes self-driven hammer shuttle mechanism with integrated linear motor. Ohter features include 60 dBA noise level, 6 part forms, business graphics, plotting, forms generation, labeling, OCR, bar codes, double-

height printing, underlining. Optional foreign, special and expanded character sets, manual forms length selector and RS-232C interface. Available in second quarter 1981. **Printronix Inc,** 17421 Derian Ave, Irvine, CA 92713. **Circle 250**

Ticket Printer. The Model 1180 employs a 5×7 matrix, has a 1100 cps print speed, selectable 50-19.2K baud rate and a 96 character ASCII. RS-232C or parallel interface. Uses 2″ wide electrosensitive paper with automatic cutter. Other features include μP control, 4K memory, friction paper feed and optional graphics capability. **SCI Systems Inc,** PO Box 1000, Huntsville, AL 35807. **Circle 251**

Ink Jet Printer. The PT80i, with a 9×12 matrix, has a speed of 270 cps. Baud rate is 300 to 9600 baud. A 128 character set supplied with optional sets available. Interfaces include RS-232, parallel and 20 mA. Other features include graphics or plotting capability, bidirectional movement, 1K memory and pin, tractor and friction paper feed. Available in RO and KSR configurations. **Siemens Corp,** 240 E. Palais Rd, Anaheim, CA 92805. **Circle 252**

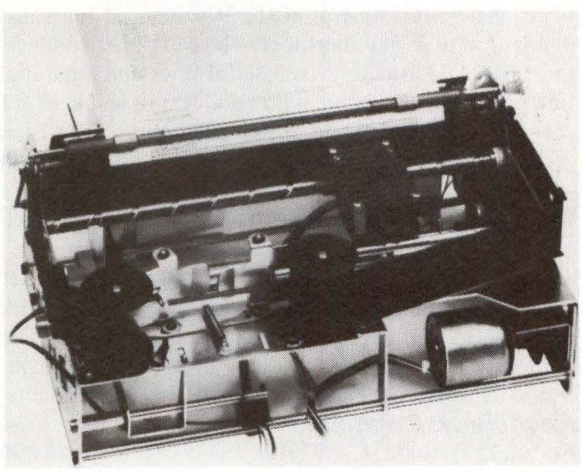
Compact Dot Matrix Printer. The SP-314 features 12V DC operation allowing independence from power lines, buffered 40 column impact printing on 4.25″ paper, RS-232 serial and parallel inputs, crystal controlled baud rate selectable from 110 to 9600 baud, 96 character ASCII set plus double width characters and a self-test routine. Includes graphic capabilities, 2 lps print speed and rugged design. **Syntest Corp,** 169 Millham St, Marlboro, MA 01752. **Circle 253**

Matrix Line Printers. Model 150 prints at 150 lpm and is field upgradable to 300 lpm. The Model 300 prints at 300 lpm and features Non-Stop-Printing. Both feature 9×7 matrix or 9×9 for characters with descenders, selectable 110-9600 baud rate, 96 character ASCII, compressed print mode, optional character sets, serial RS-232C and parallel interfaces, dual μP control, and a 7 line buffer memory. A graphics mode is also included with a 60 × 72 dots/in. plot density. Full forms control. **Trilog Inc,** 17391 Murphy Ave, Irvine, CA 92714. **Circle 254**

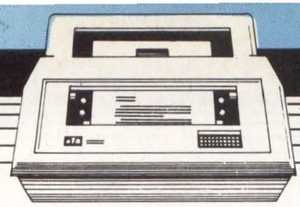
Thermal or Electrosensitive Printers. The 6410/6420 has a 64 cps print speed, 110/300 baud rate, 64 character ASCII, optional double font character set, and serial RS-232C, 20 mA loop or 8 bit Bus interface. Also includes pressure paper feed, μP control and 32 character buffer. **United Systems Corp,** 918 Woodley Rd, Dayton OH 45403. **Circle 255**

Daisy Wheel Printers. The V300 series includes a 25 cps and 45 cps model. Both are impact printers which product letter quality printing using a 96 character print wheel. They accommodate paper widths to 15″ and print up to 136 columns. Centronics parallel or RS-232C interface. Baud rates from 300 to 2400. A programmable VFU allows selection of form length up to 66 lines with top-of-form and VT justification. **Vista Computer Co,** 1317 E. Edinger Ave, Santa Ana, CA 92705. **Circle 256**

Dot Matrix Printers. Model 820 is a split platen journal/receipt printer. Model 840 is a slip/document 40 column printer. Model 850 is a 51 column journal printer. Model 880 is an 80-96 column journal printer.



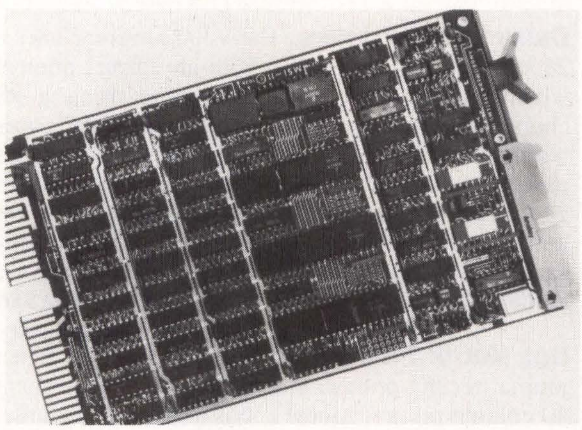
All are alphanumeric bidirectional units with a 150 cps print speed. Needle array permits a wide variety of characters and fonts. Heavey duty construction and 100% duty cycle. **Westrex OEM Products,** 1140 Bloomfield Ave, W. Caldwell, NJ 07006. **Circle 257**



Printer Components

Graphics Board. This plug-in board, the OMNI 810 Graphics, contains 4K ROM and 4K RAM and allows the TI 810 RO printer to perform graphics plotting and user-programmed special character printing. Provides hard copy from Raster Scan data systems, as well as 150 cps character printing. User may utilize two plot modes and may define his own 75 character software font for custom uses such as foreign languages, descenders, scientific symbols, bar code, etc. **Analog Technology Corp,** 15859 E. Edna Place, Irwindale, CA 91706. **Circle 258**

LSI-11/Q-Bus Interface Cards. The LPI 11 series connects the LSI-11/Q-Bus to the DEC LA180 printer, all Centronics style interfaces and Diablo 1200 & 1300



parallel daisywheel printers. The MSI 11 series connects the LSI-11/Q-Bus to 1, 2 or 4 serial lines and printers with serial interfaces. The MSI 11-P connects the LSI-11/Q-Bus to 2 or 3 serial lines and a parallel line printer. Compatible with DEC RT-11 and RSX-11 software. **Andromeda Systems, Inc,** 9000 Eton Ave, Canoga Park, CA 91304. **Circle 259**

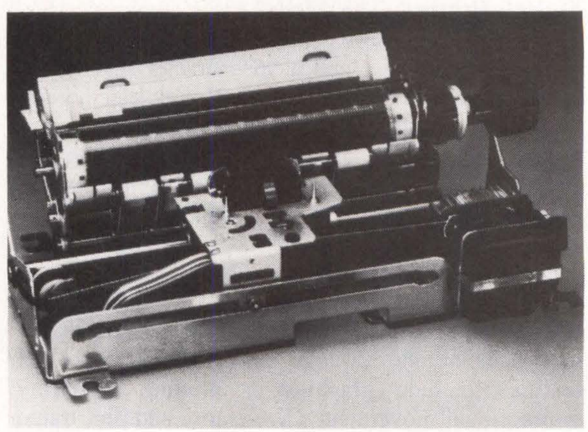
Printer Controllers. The IF-11/9700, a μP-driven controller, attaches to the DEC PDP-11 and emulates an IBM System/370 Selector or Byte Multiplexer Channel. Principal use is operation of the Xerox 9700 high-speed multi-font printer from the PDP-11. The company also markets a wide variety of other mainframe interfaces and DEC system attachments. **Associated Computer Consultants,** 228 E. Cota St, Santa Barbara, CA 93101. **Circle 260**

TI Multiplexers. These boards for the TI 990 Series computers control 7 or 15 terminals or printers (RS-232 type). They feature independent fully programmable baud rates for each channel and for input and output on each channel, 2 sensible control lines for each channel (RTS & DTR), one controllable output line for each channel (CTS), and independently programmable stop bit, parity bit and data bits for each channel. **Axis Inc,** 4706 B Ruffner St, San Diego, CA 92111. **Circle 261**

Controllers and Interfaces. Line printers with complete "add-on" line for the plug compatible marketplace. Develops unique interfaces and controllers for most mainframes and minicomputers including DEC, HP, IBM, Burroughs, Control Data, TI, DG, Interdata, etc. **BDS Corp.** 1120 Crane St, Menlo Park, CA 94025. **Circle 262**

Printer Parts. Full array of precision parts for computer line printers including daisy print wheels, continuous print bands, encoders, timing devices, gimbal springs and flexible circuits. Custom designs available. **Buckbee-Mears Co,** (BMC), Micro Products Div, 245 East 6th St, St. Paul, MN 55101. **Circle 263**

Printer Mechanism. The PM 114 is an impact dot-matrix mechanism featuring 3-way forms handling which accommodates forms including pinfeed, roll



paper and cut sheets. Includes bidirectional printing, 90 cps print speed and front or rear feed. **Burroughs OEM Marketing,** Burroughs Place, Detroit, MI 48232. **Circle 264**

DC Commercial Motors. Uses in high-speed serial and line printers. DC permanent magnet servo motors designed for direct drive servo systems. Applications include printer carriage drives and office copiers. Stepper motors provide torque in discrete steps in response to excitation pulses from a controller or driver. Applications are ribbon feed, paper advances and car-

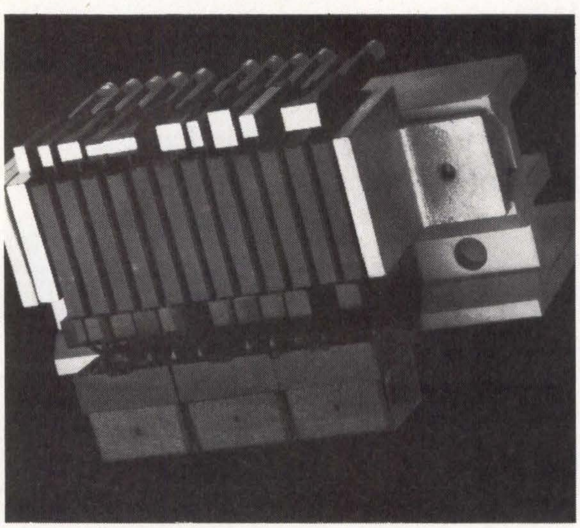
riage drives. **Clifton Precision,** Div. of Litton Systems, Marple at Broadway Ave, Clifton Heights, PA 19018. **Circle 265**

Thermal Dot Matrix Mechanism. The Q160 employs a 5×9 dot matrix font on 7×11 dot character cell. Speed is 160 cps, 128 character ASCII with U&L case, over and underscore, descenders. APL and foreign fonts optional plus a 512 × 512 or 1024 × 512 plotting option. Other features include bidirectional movement, friction paper feed, 80 and 132 column format and RS232 and 20 mA interfaces. **Computer Devices Inc,** 25 North Ave, Burlington, MA 01803. **Circle 266**

DEC Line Printer Controllers. The LPC 11, LPC L11 and LPC 8 provide an interface to a variety of line printers for the PDP-11, LSI-11 and PDP-8 families of processors. Accepts LA 180, Centronics or Data Products. **Computer Extension Systems Inc,** 17511 El Camino Real, Houston, TX 77058. **Circle 267**

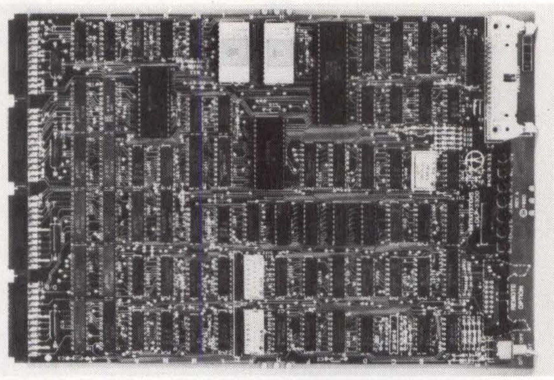
Line Printer Mechanism. The DMI-40, a 40 column, 12VDC mechanism, has a 9×7 matrix and will print any size font or graphics using customers electronic drive circuitry. With optional DMI-40E electronic driver board, it will print 96 character ASCII code (parallel and serial, RS-232 inputs) in 5×7 matrix font. **Data Machines International Inc,** Ghent Square, Bath, OH 44210. **Circle 268**

Custom Hammerbanks. Designed and manufactured to particular customer specifications. The number of columns, column spacing, effective mass, impact



energy, contact time, tip size and shape, drive current, flight time, flight distance, and mounting can be specified to provide optimum performance. Typical life of over 100 million characters per hammer. **Dataproducts Corp,** 6200 Canoga Ave, Woodland Hills, CA 91365. **Circle 269**

Line Printer Controllers. A variety of controllers that connect DG Nova or Eclipse, DEC Unibus or Q-Bus, and IBM Series/1 to any Centronics or Dataproducts interface printer. All share certain common



features: self-test which verifies controller, cable and printer operations and assists in printer system troubleshooting; all cables are interchangeable with other Datasystem controllers; all addressing and interface options are DIP switch selectable with no trace cutting or jumpering required; all are software transparent. **Datsystems Corp,** a Wespercorp Subsidiary, 8716 Production Ave, San Diego, CA 92121. **Circle 270**

Interfaces and Supplies. Interface products in the CS series are compatible with most personal, mini and mainframe computers. A complete line of wheels, ribbons and supplies as well as depot and field service capabilities. Interfaces are RS-232, Centronics 8-bit parallel, IEEE-488 Commodore, HP-85 and Datapoint parallel. **Data Wholesale Corp,** 700 Whitney St, San Leandro, CA 94577. **Circle 271**

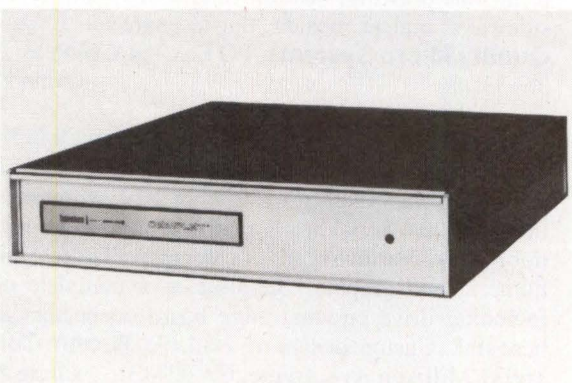
Impact Matrix Printheads. Complete line of printheads from 7 and 9-wire to 18-wire twin row; 42-wire, 6-row; and OCR versions. Range from 1 KHz to 2 KHz. Custom designs available. **DH Associates,** 754 N. Pastoria, Sunnyvale, CA 94086. **Circle 272**

Dot Matrix Impact Mechanism. The Model 410 is a journal or receipt printer with a 5×7 matrix. Speed is 3 lps. Includes 96 character ASCII, baud rate software selectable to 1200 baud, bidirectional movement and friction paper feed. Optional tractor paper feed, supply and rewind, low paper sensor and document edge sensor. **Eaton Printer Products,** Technical Research Park, Riverton, WY 82501. **Circle 273**

Thermal Printheads. The DM20100 is a medium speed 20 column printhead for printing 5×7 dot matrix characters at 2-4 character lps. Text/datalogging applications. Allows multiplexed operation. The SM 20100 is a high-speed 20 column printhead for outputting mini/micro developmental systems at up to 1600 text lpm. The DM 10101 is a medium speed 2" graphics printhead. Up to 20 dot lps, 4 character lps. Multiplexed operation. The LM152 is a high-speed 3" graphics printhead with 2.5 ips chart speed, 800 lpm text speed. The DLP110 is a 10 dot print/plot flying head. Used at 30-60 cps in printer/plotters and in EKG strip recordings. **Gulton Industries Inc,** Hybrid Microcircuit Dept, 212 Durham Ave, Metuchen, NJ 08840. **Circle 274**

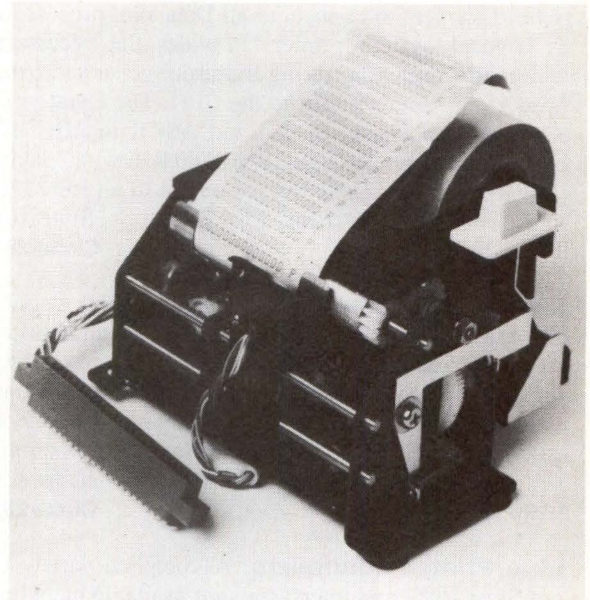
Printer/Plotter Mechanism. Microplot 80 prints full 80 column, matches CRT display line for line. Uses a thermal fixed head, thick film design. Plots data and prints grid on scale, annotates data with alphanumerics and prints alphanumeric text with X&Y axis orientation. Programmable 9 data line graphics interface, individual dot addressing, enhanced vector plotting. Full 96 character ASCII, double height, double density characters, programmable tabs. **Gulton Industries Inc,** Measurement & Control Systems, Gulton Industrial Park, E. Greenwich, RI 02818. **Circle 275**

Electrostatic Plotter Interface and Controller. EPIC is a vector-to-raster converter for electrostatic plotter/printers. It looks like a local async serial RS-232C compatible terminal to the host and can receive



and transmit serial data at up to 19.2K baud. EPIC has a serial output port available and utility plotting software routines. It works with the host to establish a proper speed to plot the data. **Houston Instrument,** One Houston Sq, Austin, TX 78753. **Circle 276**

Electrosensitive Printer Mechanisms/Subsystems. These mechanisms provide dot matrix printing as well as graphic versions. From hand held versions to panel as well as desk or bench operations. A variety of features including tear bar, paper advance, paper roll mount, paper release; either 12, 16, 21 or 40 columns;



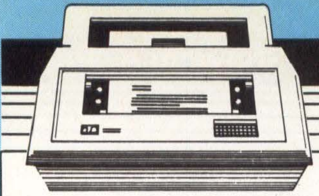
from 3 to 5.5 lps speed; paper widths of 1.4", 2.25", 4.75"; and serial or parallel interfacing. Uses include archival data recording data logging and scientific notation type equipment. **Hycom Inc,** 16841 Armstrong Ave, Irvine, CA 92714. **Circle 277**

HASP Workstation. Used with Printronix P300/P600 printers, the HASP-PX allows attachment of from 1 to 8 Printronix printers to a single box with all EBCDIC to ASCII and serial to parallel conversion handled internally. Multiple input and/or output devices may operate simultaneously. Optional ports can be configured for a variety of devices. Supports 7 user-selectable data rates of 300 to 19,200 Hz on any of the serial ports. **KMW Systems Corp,** 8307 Highway 71 West, Austin, TX 78735. **Circle 278**

Sprocket Drum Assemblies. For graphic recordings or pinters, these sprockets and drums are available for paper with perforation pitches of 1/6", 5 mm, 1/4", 3/8", 1/2" and special sizes. Parts available as stock components or made on special order. **LaVezzi Machine Works Inc,** 900 N. Larch Ave, Elmhurst, IL 60126 **Circle 279**

Shaft Position Encoders. These electromechanical devices provide an efficient method of digitizing the variable properties of a rotating shaft. Applications include any device which requires monitoring angular or linear positions, speed regulation or amount of rotation. **Litton Encoder Div,** 20745 Nordhoff St, Chatsworth, CA 91311. **Circle 280**

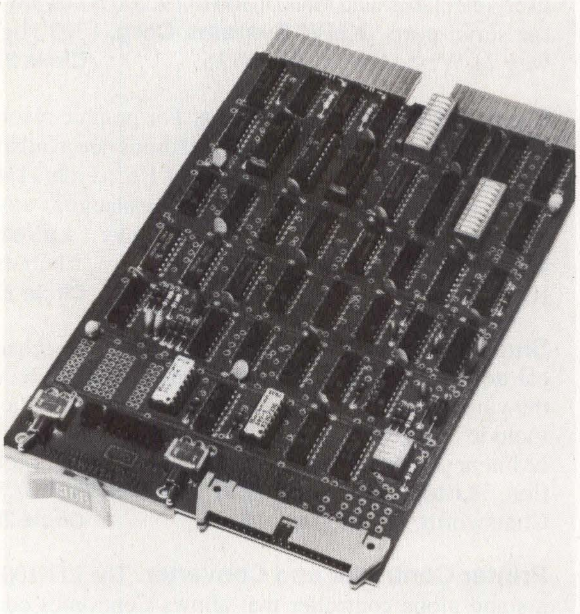
Printer Controller and Converter. The LD-100 is a stand alone controller that allows Centronics com-



patible printers to connect to all Datapoint processors as a local system printer. Provides the necessary address decoding, buffering and strobe generator to the printer and printer status to the CPU. The DataLynx/3780 is an async to bisync and ASCII to EBCDIC converter that emulates an IBM 3780 RJE with 2 async ports, one for I/O and one for output to an RS-232C line printer. **Local Data,** 2701Toledo St, Suite 706 Torrance, CA 90503. **Circle 281**

Line Printer Controller. Compatible with Perkin-Elmer computers and interfaces printers with industry standard Centronics, Dataproducts, or Data Printer interfaces. Compatible with diagnostics and operating systems. Printer speed to 500 kB/sec, switch selectable addressing, 1/2 standard bus load, 1/2 mounting slot. **Macrolink,** 1150 E. Stanford Ct, Anaheim, CA 92805. **Circle 282**

Line Printer Controllers. A complete variety of configurations and interfacing are available including DEC, PE, Centronics, Dataproducts, GE TermiNet, Houston Instrument, Printronix, Control Data, Mannesmann Tally, Okidata, Data Printer, IBM etc. Various models are compatible with RT-11, RSX-11, VMS, IAS, RSTS, RTS, RDOS, AOS and DOS operating systems. Various features include four level interrupt, loop features, LEDs to give visual indication of data lines, DIP switch selectable addressing and interrupt vectors, cables, optional long line differential drivers-receivers, special PROMS to allow block character printing, barcode, plotting and other graphics, and Printest — a complete self-testing capability which verifies that the interface circuitry of the printer and controller are operating correctly and that the interconnecting cable is not damaged. **MDB Systems Inc,** 1995 N. Batavia St, Orange, CA 92665. **Circle 283**



Terminal-To-Printer Interfaces. Designed for use with MSI portable data entry terminals, Model 77-435 provides a direct interface with Radio Shack's Quick Printer II. Model 77-428 is a versatile RS-232 interface module which plugs into an MSI terminal and can operate as a local interface to transfer data between the terminal and host computer, acoustic coupler or printer/teletype. **MSI Data Corp,** 340 Fischer Ave, Costa Mesa, CA 92626. **Circle 284**

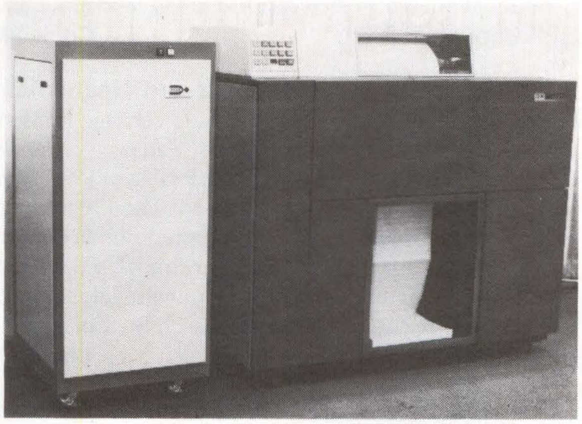
Forms Feed Tractors and Assemblies. Variety of forms tractors for Daisywheel printers; tractor feeds for Teleprinters. Quality components XACTRON forms tractors for all computer printers, paper motion monitors, shafts, specialty gears, clutches, bushings, rollers, standard and custom forms handling assemblies. **Precision Handling Devices Inc,** 63 S. Main St, Assonet, MA 02702. **Circle 285**

Printer Controller. The Magnum 3000 transforms the Printronix P150, P300 and P600 printer/plotter into an in-house labeling and barcoding system capable of forms generation. Completely transparent to host computer. Features on this 9×12" circuit card include large character generation both U&L case, compressed print, line drawing, box drawing, forms drawing, and sideways and/or upside down character rotation. **Quality Micro Systems,** PO Box 1644, Mobile, AL 36633. **Circle 286**

Thermal Printheads. Thick film line and thin film serial printheads for use in non-impact printers. Line printheads vary in print width from 2-10" with varying dot densities. Serial heads available in 1×7 and 1×24 dot matrix. Various types of cabling available. Alphanumeric and graphic. Supplied as a complete unit including drive circuits, edge board connectors and heat sink. Custom designing available. **R. ohm Corp,** 16931 Milliken Ave, Irvine, CA 92713. **Circle 287**

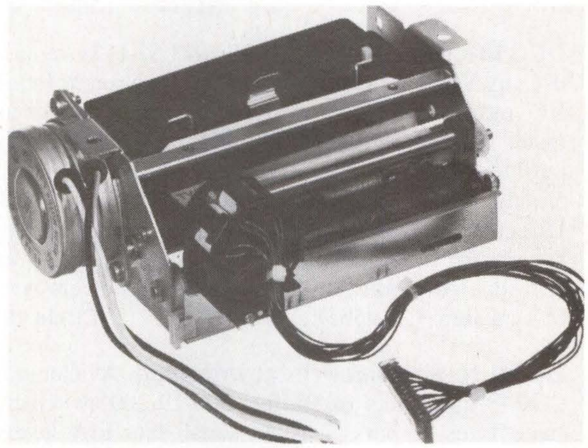
Graphics Board. The Graphic II circuit board converts a DECwriter terminal to a plotter. A total of 1320 × 792 dots are addressable. Features multiple character sets, vector graphics, superscipts and subscripts, VT-100 graphics compatibility, boldface and doublewidth type, tabs, forms control and bidirectional paper feed. **Selanar Corp,** 2403 De La Cruz Blvd, Santa Clara, CA 95050. **Circle 288**

Printer Controller. The S1403 allows the IBM 1403 family of printers to operate on non-IBM computers plus IBM Series/1, 360/370 and 1130 computers.

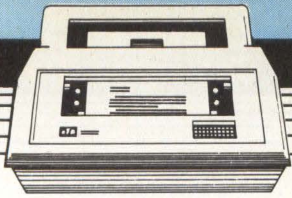


Interfaces to DEC, Burroughs, Univac, Prime, Sigma, HP, CDC, etc. Optional ROM and single to 3 phase conversion available. **Spur Products Corp,** 1904 Centinela Ave, Los Angeles, CA 90025. **Circle 289**

Dot Matrix Impact Mechanisms and Printheads. The GPM-40A, -B and -C are 40 column mechanisms. Speeds are 60 lpm and 120 lpm, print width is 3.33″, ribbon cartridge. The GPM-80-A and -B are 80 column mechanisms for Personal and small business printers, OEM, mini and micro computers and stand alone printers. 60 lpm throughput, 8″ print width. Sync or stepper motor line feed. The VERS/ECON-7 and -9 are 7 or 9 wire dot matrix impact



printheads with 150 cps print speed. **Two-Day Corp,** (TDC), 203 E. Main St, Riverton, WY 82501. **Circle 290**



Matrix Printhead. The Mark IV WP is a 9 needle head for correspondence quality printing. Produces standard matrix style printing or high quality fonts such as elite by ROM change. 500 million character life. **Universal MicroPrinters Inc,** PO Box 313, Shelton, CT 06484. **Circle 291**

DEC Interface. Model 125 allows LSI-11 systems to use any Versatec electrostatic plotter or printer/plotter, I/O multiplexer, hard copy controller or vector-to-raster converter. Electrically and mechanically compatible with PDP-11/03, -11/23 and LSI-11/2, -11/23 and the LP-11 line printer driver. Operates under DEC Direct Program Control or DMA. Provides for printing speeds to 1000 lpm and plotting speeds to 34 sq. ft./min. **Versatec,** a Xerox Co, 2805 Bowers Ave, Santa Clara, CA 95051. **Circle 292**

Serial to Parallel Printer Interface. Available in 0-2048 characters of Buffer, 300-19,200 switchable baud rates. Input — async serial data EIA levels. Output — parallel TTL Centronics printer compatible. Self-test and mounting. Optional self-powered. IEEE model available. **Via West Inc,** 2739 W. Palm Lane, Phoenix, AZ 85009. **Circle 293**

Dot Matrix Impact Printhead and Mechanism. The 129 printhead is used for wide carriage printers, plotters or special purpose printers. Can print on labels, tickets. User determines font. Special symbols or foreign languages. 110 cps print speed. The 130 mechanism includes paper handling, blue/red ribbon control, 110 cps, and 41, 34 or 18 char/line. Used in cash registers, calculators, bank terminals, etc. **Victor Data Products,** 3900 N. Rockwell St, Chicago, IL 60618. **Circle 294**

Printer Interface. The ZBX-349 interfaces Intel and Zendex single board computers with SBX module jacks to a Centronics type parallel interface. Includes 6′ cable with connectors, 5V only operation, occupies one port I/O address, automatic data latch and strobe. Accomplishes all hardware interfacing needed when an SBC system is integrated with a line printer. **Zendex Corp,** 6680 Sierra Lane, Dublin, CA 94566. **Circle 295**

Innovative Design

Letter-Quality RO Daisywheel Data Terminal

Bringing letter-quality and RO data terminal versatility to WP and computer users, Qume's "Sprint 9" is a significant development in daisywheel printing. Its "Direct Drive" mechanism promises greater print accuracy and system reliability.

The steel cable and pulley drive in other daisywheel terminals was replaced by the "MicroDrive" carriage mechanism; it uses a custom-designed DuPont KEVLAR belt to position the printer for each strike. The belt is pretty tough. Our editors decided to see just how tough this thin belt was. After measuring a sample band (at slightly over a 3/8″ width), we made a 1/4″ cut in it perpendicular to the edge; and, after repeatedly trying to tear the severely damaged belt in two with our full force, we couldn't do it. Due to its construction, it's unlikely this belt will stretch with age.

But why give up the steel cable? Without the cable and multiple-pulley system used in other terminals, there is considerably less tension on the printer chassis and greater tolerance for service adjustment, and everything lasts longer.

Extensive life tests demonstrate a MTBF much better than other daisywheel terminals. This means a longer period between service calls.

Sprint 9 has both old and new features, having incorporated those proven successful in the earlier models. It has 30% fewer parts, since PCBs were reduced from four to three, the supply moved inside the cover and service access simplified. Improved ribbon handling with new "Clean Hands" Quickload cartridge system and "multistrike IV" ribbon cartridge permits 375,000 characters. As for noise pollution, critical in today's new markets, acoustic noise level was reduced to 65 dBA, max. It is less vulnerable to static electricity. Automatic proportional spacing is switch selectable. It has a "Hot Zone" automatic carriage return. Exterior styling is contemporary, with controls on the front.

Using the industry standard RS-232C interface, it plugs directly into most minis and provides all current WP functions. Print speeds include 45 CPS and 55 CPS. Its superset of the Sprint 5 command set has enhancements such as automatic "Logic Seeking" bi-directional printing.

To avoid being a single-source company, Qume second-sources itself, with equal and separate manufacturing operations in San Jose, CA and Humacao, Puerto Rico. Sprint 9 is compatible with Qume supplies, 94-plus plastic printwheels and complete selection of ribbon cartridges and other accessories.

All Sprint 3 and 5 models will continue to be available and receive full manufacturing support.

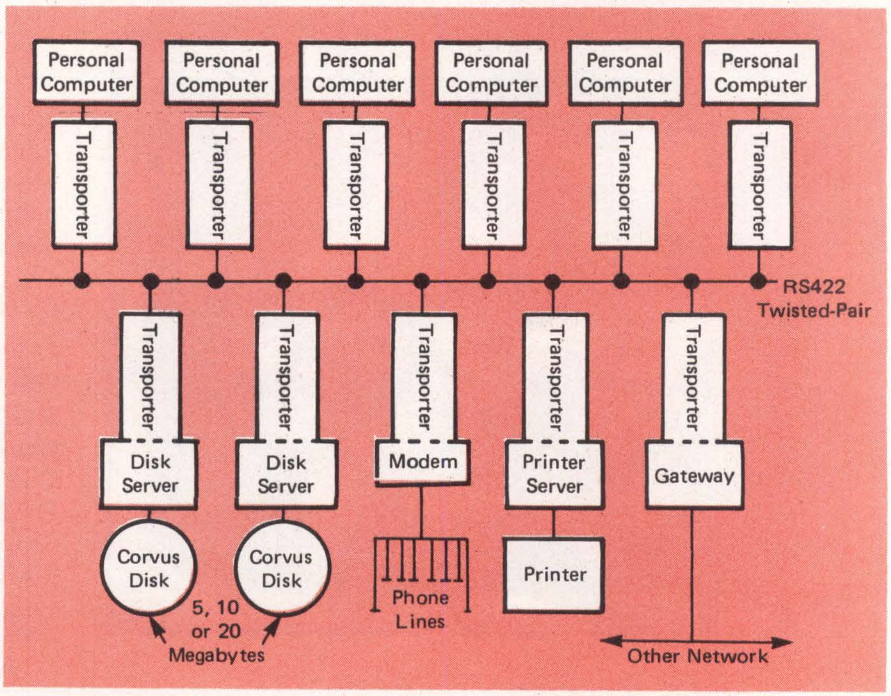
— Paul Snigier

Qume Corp, 2350 Qume Dr, San Jose, CA 95131. **Circle 199**

Low Cost Local Network Interconnects 64μCs

Opening one door to the office of the future is Corvus' Omninet, an efficient one-megabaud network that utilizes low-cost RS-422 shielded twisted pair cable in lieu of more costly and bulky coax. The network interconnects up to 64 μCs and peripherals in a 4,000≥ serial link. Maximum message size is variable, up to 2KB.This carrier-sense-300multiple-access (CSMA) network, similar in concept to Ethernet-type networks, is priced at a fraction of their predicted prices.

Omninet permits sharing of mass



storage and printers and two to 64 computers; it is easily expandable as needs grow and simple to install (screwdrivers and pliers).

System intelligence is centered around the Omninet transporter — a Corvus-designed interface with a Motorola 6801, custom Omninet gate array and support components. The transporter interfaces directly to the μC or peripheral on any network node and provides the transfer of error-free, variable-length messages with no software intervention required by the sending or receiving μC. Thus, total network management is provided to users without a costly network control processor.

Omninet works with Constellation software, providing up to 80 million bytes of shared storage. Omninet, available for the Apple II, Onyx C8000 and LSI-II, connects to any existing Corvus peripheral, including the 5-, 10- and 20-MB Winchesters, Mirror or Constellation. Future transporters will include Apple III, Tandy TRS-80, any S-100 Bus computer, Atari, Commodore, Altos and others. It will provide gateways to Ethernet, SNA and other available networking next year.

Omninet transporter units are $495 for the Apple and S-100 Bus computers; $750 for the DEC LSI-II; and $650 for the Onyx C8000. The disk server for Corvus Winchester disks retails for $990.

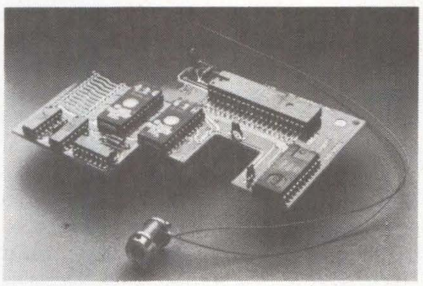
Corvus Systems, Inc, 2029 O'Toole Ave, San Jose, CA **Circle 198**

Enhancement Extends TI Terminal Capacity 70%

Many smaller electronics firms have left peripheral manufacturing to the big guys. Instead, they're focusing their energy on producing enhancements for already-established popular peripherals. Since original product manufacturers are generally unwilling to cooperate with such endeavors, companies concentrating on product enhancements must engage in rear-view engineering: analyzing the existing product, finding what potentially-popular option it lacks, and designing that option so that a user can easily retrofit his peripheral.

Texprint, a new company specializing in product enhancements, decided the TI "Silent 700" series of printing terminals would be their first product's target. Their TXP 136 converts an 80-column TI Silent 700 into a 136-column printer, and may be installed with only a small screwdriver (provided the user is mechanically inclined, adds Texprint president Joel Novak). Aside from squeezing 70% more data onto a page, the option creates more readable type, claims the manufacturer.

"The TXP 136 had some unique design problems, because we had to be adaptable to a product that was first manufactured in 1976 and is still being



manufactured," explains Novak. "So we had to be adaptable to a number of vintage TI terminals, to allow the same basic module to go into any unit."

Texprint's modification is a two-step process consisting of changing TI's motor pulley and cable, and replacing a socketed μP with a small PC board.

Without TI's aid, Texprint had a difficult time designing the option. "We had to figure out not only what they did, but why they did it, because we had to be sure in our design not only that we function correctly," says Novak, "but that we don't overstress any of the parts of the machine, nor use them in a fashion that they weren't really intended to be for. We want to make sure that the machine is as reliable as it was before we modified it."

According to Novak, TI actually has much to gain from the enhancement. "It extends the life of their product. Many of these people have them on lease, so for a relatively small amount of additional money, distributors take a product that's maybe four or five years old, rejuvenate it, and then put it back on lease for another two or three years."

TXP 136 costs $375 in quantities of one (OEM discounts available) and is available from Texprint or most TI terminal distributors. Delivery is 15 days ARO.

— Bob Hirshon

Texprint, Inc, 8 Blanchard Rd, Burlington, MA 01801. **Circle 200**

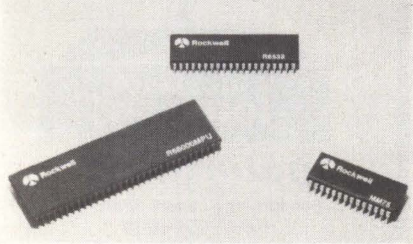
New Products

TEXT-TO-SPEECH SYNTHESIZER makes "talking" a practical reality for personal computers. Used on any computer with an RS-232C interface, TYPE-'N-TALK permits the hobbyist to type an unlimited combination of English words and

phrases on the keyboard. Words can be spoken simultaneously as they are typed, or a 750 character buffer will hold the words until the user prompts the computer to speak them in entire phrases or sentences. The computer can verbally take the user through a complex routine. Used as a teaching aid, it can tell students when and why they correctly answered a question. TYPE-'N-TALK is $345. **Vodex,** a Votrax Co, 500 Stephenson Hwy, Troy, MI 48084.
Circle 190

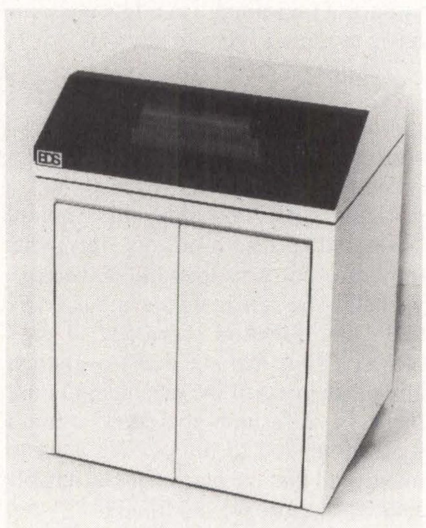
MULTIBUS CONVERTERS. The Series 5400 Intel 8056/8086 Multibus compatible synchro-to-digital (S/D) and digital-to-synchro (D/S) system consists of a standard Intel size PC that incorporates all interface logic. It can be configured with either a multi-purpose two-speed (36:1/18:1) S/D; or any combination of three 16 bit S/D or D/S converters. **Transmagnetics, Inc.,** 210 Adams Blvd, Farmingdale, NY 11735.
Circle 202

R68000 16-BIT CPU. The device is the first in the R68000 16-bit family which addresses up to 16 MB of memory, has over 1000 total instructions and can process 8, 16, or 32-bit data. The R68000 CPU is being sampled now in 4 and 6 MHz versions, with an 8 MHz version scheduled. Additional devices which will be available in the 68000



family include an intelligent peripheral controller (68120), a memory management unit (68451), and a DMA controller (68450). **Rockwell International,** Electronic Devices Div, 3310 Miraloma Ave, Anaheim, CA 92803 **Circle 205**

900 LPM BAND PRINTER incorporates diagnostic routines and a dual-digit status display that lets operators pinpoint and correct minor problems. The display also indicates malfunctions such as character-read errors, vertical format unit faults and others. This 132-column printer operates at 1100 lpm with a 48-character set, 900 lpm with a 64-character set and 672 lpm with a 96-character set. Bands are easily exhanged by the operator. Horizontal print format is 10 cpi with vertical format switch selectable at 6 or 8 lpi. Noise levels are less than 60dB. Handles fan-folded paper forms from 3″ to

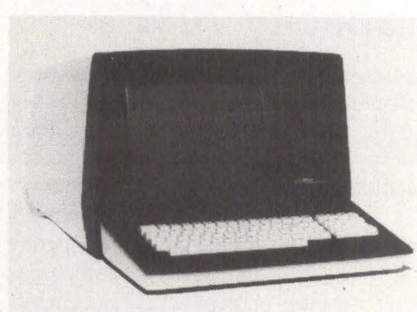


16″ wide with up to 6 parts. The BDS 900 is $11,600 ea; interfaces and controllers from $3500 to $6500. **BDS Corp,** 1120 Crane St, Menlo Park, CA 94025. **Circle 145**

RFI SEMINARS. For those who want to learn more about FCC's Radio Frequency Interference (RFI) regulations for computers, R&B Enterprises offers two one-day seminars. One seminar deals with the regulations themselves: background, terms and definitions, labeling, test methods and facilities. The second seminar concentrates on design methods for controlling RFI, including system grounding, shielding, filtering, conductive coating and composite applications. Each seminar costs $225, ten days in advance ($250 at the door). Fee includes luncheon, coffee breaks, course notes and copies of subject documents. Seminars run from 9am to 4:30pm, and will be held in Los Angeles on June 23-24 and in San Francisco on June 25-26. For more information, contact Leonard Levin, **R&B Enterprises,** PO Box 328, Plymouth Meeting, PA 19462. Phone (215) 828-6236. **Inquire Direct**

MULTI-TASK SYSTEM. This operating system supports PASCAL and "C" language compilers on the MC68000-driven CGC 7900 color graphic computer. IDRIS is a general purpose operating system which includes an assembler and text editor. The operating system is $2,000, language compilers are $1,000 each. The CGC 7900 provides high-resolution color graphics, the power and speed of the 68000 CPU and the optional capacity for a 10MB Winchester hard disk drive and dual double-density flexible disk drives in one integrated cabinet. Base prices start at $19,995. **Chromatics,** 2558 Mountain Industrial Blvd, Tucker, GA 30084. **Circle 133**

IBM 2740/3767 DISPLAY. This display terminal provides 3270-type features and application-program access to IBM 2740- and 3767-type keyboard printer terminals. Current 2740 and 3767 users can avoid the substantial investment in programming, equipment and additional leased lines normally necessary to provide remote users with 3270-type terminal capability. A slave printer may be attached to the display to print data selectively from the screen. The μP-based display features a 12″ diagonal screen with 24 80-character lines. The 25th line is an operator and terminal status line. Most existing 3270-type application programs can be interfaced with the CTi 2000 over 2740/3767 communication lines by

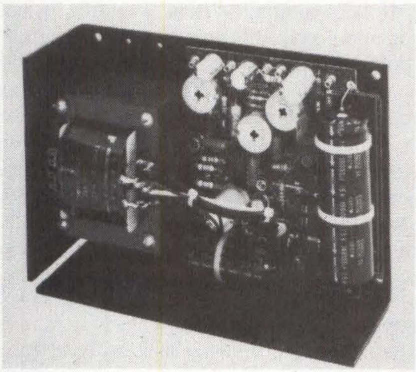


using a special software translator module. The CTi 2000 is $2,500. The software translator interface is $7,500. **Custom Terminals Inc.,** Box 19906, Raleigh, NC 27619. **Circle 201**

64K RAMS. In a standard 16 pin DIP package with access times of 150 and 200 ns, the MB8264 quadruples memory system capacities without adding space or sacrificing speed. Features include: TTL compatibility; 248 mW active- and 28 mW standby power; single +5V supply, ± 10% tolerance; 128 refresh cycles/2 msec; and hidden refresh. **Fujitsu Microelectronics,** 2945 Oakmead Village Court, Santa Clara, CA 95051.

Circle 207

HARD DISK POWER SUPPLIES. These linear μP power supplies offer outputs of 5V at a current of 5A, 9 to 15V with a current of 1.0A and the third produces 5 to 15V at



0.3A. Designed for high volume OEM micro-based systems applications, Model TBB512 is low cost and features current limit/foldback for continuous overload protection and built-in overvoltage protection on all 5V outputs when the unit is set at 6.2±4V. The TBB512 incorporates a built-in OVP, dual 115/230 VAC input for both domestic and foreign operation and a −12V output that can be selected to −5V for different ROM and I/O circuitry. **Microcomputer Power, Inc.,** 2272 Calle de Luna, Santa Clara, CA 95050. **Circle 191**

IEEE-488 BUS EXTENDER gives virtually unlimited range for IEEE-488 Bus systems. The Extender converts parallel Bus data to serial form for high-speed transmission; up to 4,000′ with twisted-pair cable and over unlimited distances using modems and telephone lines. A second Bus Extender at the other end reconverts the serial data to parallel Bus data. With twisted-pair cabling,

the Model 4886 transmission link is fully duplex, allowing data to flow in both directions simultaneously. In a multi-drop operation, up to 31 remote sites can communicate, at one time, with the controller. $1,295. **ICS Electronics Corp,** 1620 Zanker Rd, San Jose, CA 95112. **Circle 177**

NEW BOOK. "The Distributed System Environment Some Practical Approaches" by Grayce M. Booth, 245 pgs. Drawing on her experience with distributed systems, Booth covers the subject with lucid comparisons of the actual approaches taken by major vendors of both general-purpose machines and minicomputers. She covers: terminology clarifying inconsistent and often contradictory vendor usage; features of seven existing systems and one hypothetical new system; advantages and disadvantages of current state of the arts systems; data base structures; networking structures; architectural principles common to all systems/networks; strategies for functional distribution; selecting components — when to use minis/micros and when to use larger machines; design techniques for the communications networks — including a summary of trends in public data networks in the U.S. and major European and Asian countries; system design — a step by step guide; and managerial and operational control. The emphasis throughout is on practical vs. theoretical information and the characteristics of real systems that you can use in day to day problem solving. $21.95. **McGraw-Hill,** 1221 Avenue of the Americas, New York, NY 10020. **Inquire Direct**

New Products

CACHE/DISK SYSTEM provides significant response time improvements for large-scale Series 1100 users. Data that is frequently accessed is held (cached) in semiconductor memory and can be transferred to the host system without waiting for the seek and latency time of disk drives. The 5057 Processor provides full control over the operation of the Cache/Disk System that functions as an I/O peripheral system attached to the 1100/60 and 1100/80 word channels. Indexing, searching, buffering, storage management, staging and destaging of data to and from disk to Cache memory, along with extensive error

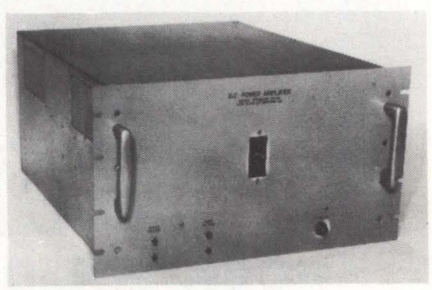
recovery, are part of the 5057 capability. The 7053 Storage Unit utilizes 16K RAM solid state memory elements for a capacity of 917,504 words of fast access data. The 7053 can be configured as a Cache memory or as a Solid State Disk. The Cache/Disk System allows for fewer disk drives to satisfy storage capacity requirements. \$104,700 for the 5057 Processor; \$137,534 for the 7053 Storage Unit. Lease prices also available. Delivery in December 1981. **Sperry Univac,** Box 500, Blue Bell, PA 19424. **Circle 195**

BOOK REVIEW. "Introduction to Computer Design and Implementation" by S.I. Ahmad and K.T. Fung, 268 pgs. If you're a physicist, electrical or mechanical engineer just entering the field of computer design, you may find this book to be of assistance. Since the development of microcomputers it is no longer feasible to separate the study of computer hardware and software. That's an approach the authors take. Including essential aspects of both as an introductory approach for beginning systems designers, the authors start with the design of simple combinational and sequential circuits, proceed to the subsystem level and then discuss the control unit, the arithmetic-logic unit, the memory unit, and I/O units. Written as a text for a first course in the subject, the book doesn't assume any prior knowledge and for that reason may be used as a self-study program. \$19.95. **Computer Science Press Inc.,** 11 Taft Ct., Rockville, MD 20850. **Inquire Direct**

FIBER OPTIC SCANNER CATALOG contains detailed specifications for over 100 configurations of fiber optic scanners for industrial, laboratory, and OEM applications. Lengths up to 72" and diameters from 0.027 to 0.125" are available. Both bifurcated units for reflective operation and straight light pipes are completely described. Models are available up to 1200°F (660°C). **Dolan-Jenner Ind, Inc.,** Box 1020, Woburn, MA 01801. **Circle 169**

LARGE SCREEN OPTION, on the DT80 Series, is a 14" screen that can display larger characters for improved readability in the 132-column mode. Particularly useful for systems development and any application using wide screen format because the larger screen eliminates the need to use a printer in order to see forms that are 132-columns wide. The DT80/114, the 14" version of Datamedia's DEC VT 100 emulator, is \$1840. DT80/314, the larger-screen version of their 132-column terminal, provides features of the VT 100, \$1540. The DT80/514 offers VT 100 features to the APL market, \$1985. Qty discounts available. **Datamedia Corp,** 7401 Central Hwy, Pennsauken, NJ 08109. **Circle 170**

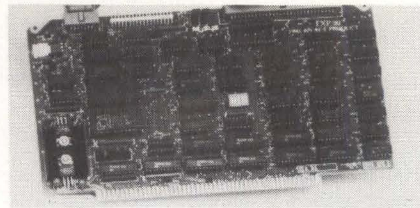
3000W DC POWER AMPLIFIER. The maximum output voltage is ±95V DC at a current of ±32A. High frequency response of 4,000 Hz, low output impedance of less than 0.1 ohm and the complete elimination of cross over distortion makes it useful in



Antenna Drives, Industrial Controllers, Computer Tape Transports and other high performance servos. The Model 980-27 linear amplifier is completely free of R.F. noise. **Control Technology Co,** 41-16 29th St, Long Island City, NY 11101. **Circle 139**

RDS-500 DISK REPLACEMENT. This all-electronic nonrotating disk replacement for Raytheon RDS-500 Computers uses a micro-programmed controller and RAM to operate via the DIO and DMA bus. The unit has two programmable modes of operation: an extended instruction mode suited for special array processing, and a disk emulation mode, emulating a 64 track × 128 sectors/track × 47 words/sector fixed head disk. The Megastore 500 Chassis will accommodate from 1 to 4 pairs of Megastore modules, offering from 1 to 4 MB of storage capacity. \$17,650 for 1MB, OEM discounts available, 90 days ARO. **Ampex Corp,** 200 N. Nash St, El Segundo, CA 90245. **Circle 131**

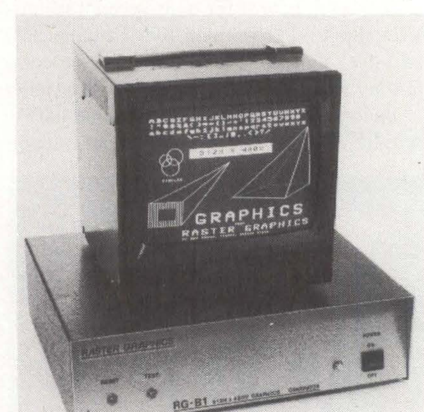
MP/M FOR S-100 BUS. This expansion board enhances the networking capability of the NET/80 single board slave processor. NET/80 contains a Z80A CPU, 64kB of RAM and an RS232 serial port for the local



console The new EXP/80 adds features for a data processing network master to run the MP/M operating system. Features include an additional console port, priority interrupt control, real time clock, serial or parallel printer support and IEEE S-100 bus master capability (as permanent master) for accessing disk controllers or other peripherals over the S-100 bus. EXP/80 may be used as either the master or as part of a slave. \$295. **MuSYS Corp,** 1451 Irvine Blvd., Suite 11, Tustin, CA 92680. **Circle 151**

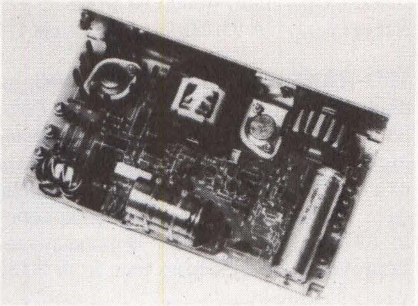
5-1/4" WINCHESTER DISK was developed for high reliability, easy system integration, reduced size and low cost. Packaged in the same size as an industry-standard minifloppy, the disk can store up to 6.38MB unformatted. Average access time is 170 ms, data is transferred at 5 Mbits/sec. The unit includes a spindle mechanism, a stepper motor and a head assembly with 4 R/W heads. Drive electronics are located on two PC boards mounted underneath the disk. Features an integral fail-safe brake mechanism to insure head/disk reliability. (\$1490). **Texas Instruments, Inc.,** Box 202145 H-574, Dallas, TX 75220. **Circle 158**

GRAPHICS GENERATOR. The RG-B1 512H × 480V Graphics Generator adds graphics capability to any computer via its RS-232 port. This stand alone unit accepts



high level commands from a host computer and displays text and graphics on a standard 525 line TV monitor. Includes point to point draw, circles, reverse video, variable size ASCII characters, selective erase, and rectangular fill. \$1,450. **Raster Graphics,** Box 23334, Tigard, OR 97223. **Circle 184**

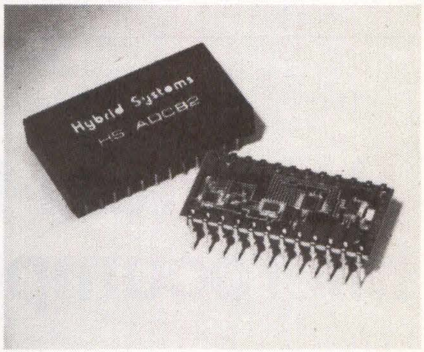
5V, 20A POWER SUPPLY. This open-frame switching power supply is the first of a family of 100W models. It is suitable for a line range of 90 to 135 VAC or 180 to 270 VAC selectable, and a line frequency of between 47 and 440 Hz. Efficiency is over 72% at full load, 115 or 230 VAC and 25°C. Model S5-20 is on a single PC board. Options include a power fail warning signal, DC input and a pre-load device. It incorporates the Univerter design, a feed-forward, pulse width modulated inverter using only one switch transistor. It requires fewer parts, for a higher efficiency, longer MTBF and improved reliability. **Adtech Power,** 1621 South Sinclair, Anaheim, CA 92806. **Circle 129**



2D HARDCOPY GRAPHICS. This software package provides users with the capability to plot cartesian, parametric and polar equations as well as data points. Full axes labeling and scaling are provided for either linear or logarithmic plotting. Shaded bar graphs are also included. CURVE is written in Basic and drives any of Houston Instrument's HIPLOT Plotters from an Apple, TRS-80, Pet or North Star computer. It also drives the new Japanese-made WATANABE plotter. **West Coast Consultants,** 1775 Lincoln Blvd, Tracy, CA 95376. **Circle 206**

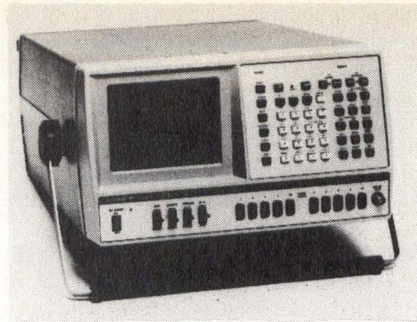
NEW PROGRAMMING LANGUAGE. The Department of Defense (DOD) in an effort to reduce some of its costs, developed the ADA programming language. Ada is an effort to standardize programming for imbedded systems in DOD. It will replace other DOD-approved languages; increase reuseability of software from project to project; and increase transferability of the environment including programmers, debugging tools and methods of documentation. It is expected to become as well known as COBOL or FORTRAN. This language was developed through coordination of the military departments and agencies of DOD. A Reference Manual for the Ada Programming Language, stock number 008-000-00354-8, is $5.50. Orders must be accompanied by check or money order and sent to Superintendent of Documents, U.S. Government Printing Office, Dept. 50, Washington, D.C. 20402. **Inquire Direct**

SECOND SOURCE DAC'S/ADC'S. The monolithic HS7541 is a version of the AD7541, a CMOS 12-bit multiplying DAC. It is built with a high density CMOS and CrSi process that yields 12-bit linearity without laser trimming, eliminating a costly step while improving stability and reliability. Specifications include TTL and CMOS compatible inputs, reference input up to ±25V, and a current output settling in 1μSec. Comes in an 18 pin plastic DIP or a ceramic 18 pin side braze DIP for various temperature ranges. From $16 to $45 (100 qty). The HS ADC82 is a second source to the BB ADC82 AG, with identical function and pin connection. Improvements include power consumption reduced by 35% to 650mW thus lowering the internal temperature and improving stability; and, the power supply voltage range has been widened to include operation at ±12V supplies. HS ADC82 is an 8-bit ADC which converts in 2.8 μSecs. Packaged in a 24 pin DIP; $69 (1 - 9), $48 (100). **Hybrid Systems Corp,** 22 Linnell Circle, Billerica, MA 01821. **Circle 193**



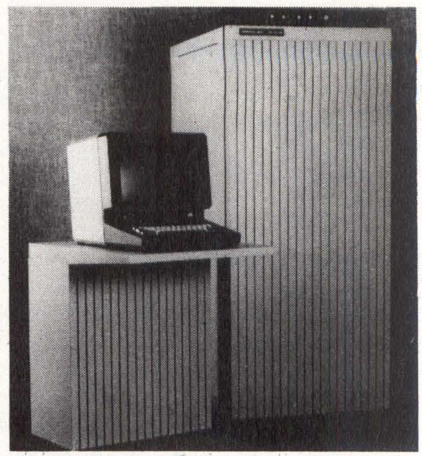
New Products

LOGIC ANALYZER allows viewing digital data transitions at speeds not previously possible. Model K500-D features a 500-MHz clocking rate and can record analog signals at bandwidths to 100 MHz. Narrow noise pulses, or glitches, transitions and other events can be captured and sampled every 2ns. Both analog and digital information may be displayed simultaneously. The K500-D is a μP-based test



system with an interactive keyboard and display. It is compatible with the IEE-488 GPIB so it can be used in fully automated testing applications. Other features include 2K words of solid-state memory, active high performance probes for each of the 8 channels, self-test routines and, for compactness and light weight, a switching power supply instead of a linear supply. Up to 8 timing channels may be recorded and viewed simultaneously, or the scroll mode used to record an 8 channel timing diagram one signal at a time. $22,625. **Gould Inc.,** Biomation Operation, 4600 Old Ironsides Dr, Santa Clara, CA 95050. **Circle 174**

MID-RANGE 32-BIT SUPERMINI includes full 32-bit architecture; 8MB DMA bandwidth; 8 DMA ports for interfacing high speed devices such as tapes and disks; 4 external priority interrupt levels, supporting over 1000 devices; and memory expansion to 8MB. Cache memory is standard and improves memory access time from 500ns

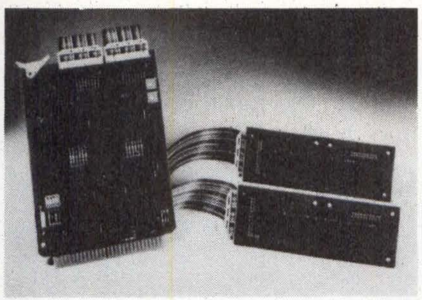


to 340ns. Reliability features include hardware error logger, ECC memory, power fail/automatic restart, processor self test, and the capability for remote diagnostics. Model 3230 is $46,789 (qty 15) for a processor with 512 kB MOS memory, a Model 550 system console, real-time clock, cache memory, and battery back-up. **Perkin-Elmer,** Computer Systems Div, 2 Crescent Place, Oceanport, NJ 07757.
Circle 188

LINEAR FEEL KEYBOARD. The Butterfly switch, the first Key Tronic capacitive keyboard with linear feel, is a solid-state keyboard that uses the same electronics as their tactile design. Includes N-key rollover at no extra charge and the same double shot molded keytops with over 20,000 legends and over 300 shapes. **Key Tronic Corp,** Box 14687, Spokane, WA 99214. **Circle 147**

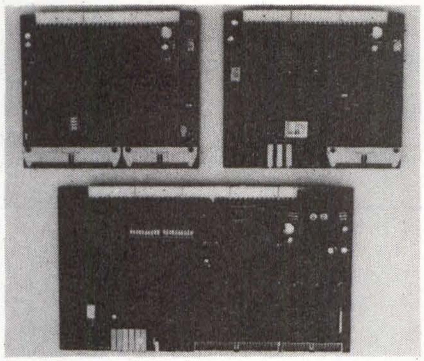
VAX 256KB ADD-IN. This single-board add-in memory for VAX-11/780 features full ECC compatibility and uses 16K dynamic RAMs organized as 32K by 72 bits to provide 256 kB. The VA-780 is a direct replacement for DEC's M8210 main memory board and is both hardware and software compatible with the host VAX-11/780 memory controller, which determines operating speeds. From $1900. **Cambex Corp,** 360 Second Ave, Waltham, MA 02154. **Circle 134**

HEX DISPLAY CONTROLLER. This STD Bus compatible I/O mapped card is designed for automatic decoding, driving, and multiplexing information. It displays up to 12 digits of hexadecimal information on a



remote display up to 6′ away. The 7911/HDC operates as write only memory and occupies 16 I/O mapped address locations. A decimal only version, the 7911/DDC, has special symbol displays and individual digit blanking. A LED support board, the 7911/HDA, consists of six .5″ LED displays that are directly compatible with either the HDC or DDC. The Hex Display Controller is from $190 to $133 (100). **Matrix Corp,** 1639 Green St, Raleigh, NC 27603. **Circle 148**

FLOPPY DISK CONTROLLER BOARDS. The DMA Disk Controller uses high speed DMA for data transfers to and from system memory. It supports any combination of drives: 8″ and 5″; single and double headed; single and double track (48 and 96 tpi); single and double density; up to 4 drives total. It features both a phase-locked loop data separator and adjustable write precompensation. It can be used in 6809 systems running at 1, 1.5, and 2 MHz. ($548). Other controller boards are also available for the SS 50 bus and 6809/6800 systems that support various combinations of drives; from



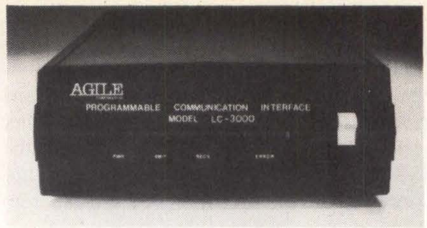
$226 to $348. **Gimix, Inc.,** 1337 W. 37th Place, Chicago, IL 60609. **Circle 187**

TEMPERATURE MEASUREMENT. The 1981 Temperature Measurement Handbook and Catalog contains over 10,000 instruments and accessories in 360 pgs. New instruments featured include a line of hand-held thermocouple and RTD digital thermometers; retractable, insulated thermocouple amd RTD wire; severe-duty assembly heads; ceramic/inconel insulated wires; and easy-grip miniature and ultra miniature hypodermic thermocouple probes. The book also contains reference tables for Thermocouples, Material Characteristics, Conversion Charts and Thermometry Fixed Points. **Omega Engineering, Inc.,** One Omega Dr, Box 4047, Stamford, CT 06907. **Circle 153**

INTELLIGENT VERSAMODEM is compatible with a variety of personal computers and the Bell Standard 103 protocol. It is also FCC registered for direct connection. Applications include store-and-forward message routing, remote database access, off-hours automatic polling, computer/terminal networking, remote computer diagnostics and CPT-TWX network nodes. Enables full automatic dialing and auto-answer capability controlled through an

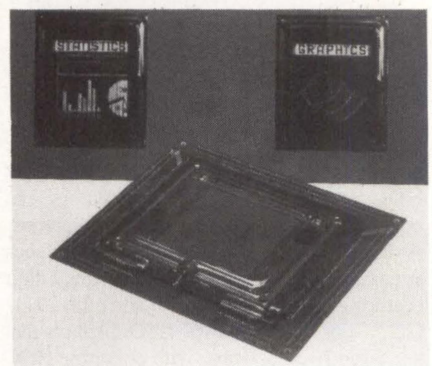
RS232 interface. Data rate is preset to 300 baud. Model 1084 VersaModem is $299, OEM qty discounts available. **Bizcomp, Corp,** Box 7498 Menlo Park, CA 94025. **Circle 132**

HP COMMUNICATION INTERFACE allows users of Hewlett-Packard MTS 3000 software to attach any RS232C peripheral to HP's MTS 3000 sync communication line. Satisfies local and remote computing requirements for any system using MTS 3000 software. The LC-3000 allows linking an HP-3000 communications line running MTS 3000 with a variety of otherwise non-compatible peripheral devices. The unit is a



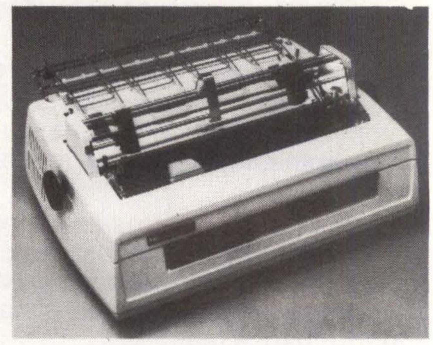
standalone μP-controlled protocol translator and line speed converter. It is plug compatible with the 20mA MTS 3000 HP current loop and offers HP modified bisync compatibility. LC-3000 also includes a 4000-byte receive buffer, a 256-byte transmit buffer, a power-up memory integrity check and operation in a transparency mode for line monitoring. $2000. **Agile Corp,** 1050 Stewart Dr, Sunnyvale, CA 94086. **Circle 164**

HIGH-RESOLUTION DISPLAY is capable of displaying a wide variety of complex subject matter including special symbols, geometric patterns, graphics, block and cursive alphanumerics, contin-



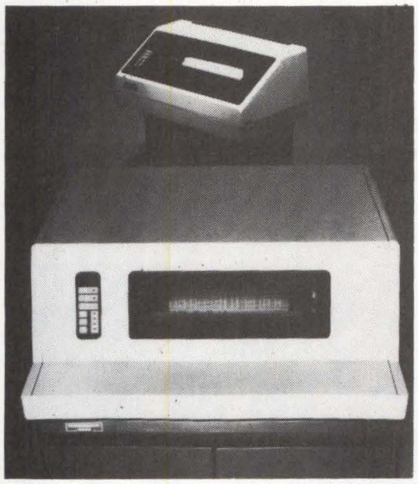
uously scrolling images and lighted areas. The "itron" square format DM128×128C 128 by 128 dot matrix display panel features a double-matrix interconnection structure to maximize the brightness output and enhance clarity. The fluorescent dot matrix has a 3" sq. active area. Each dot in the closely spaced matrix is individually addressable. **Noritake Electronics, Inc.,** 22410 Hawthorne Blvd, Torrance, CA 90505. **Circle 196**

LETTER-QUALITY PRINTERS. The Spinwriter 7700 Series consists of 7 models that provide letter-quality printing at speeds up to 55 cps. They use 27% fewer parts than the previous 5500 Series, and feature new electrical and mechanical advancements that reduce traditional ownership costs. These include single-board electronics, a compact one-piece universal power supply, and new digital control techniques for improved print quality. Intended for sale either as mechanisms to major computer and office automation equipment manufacturers



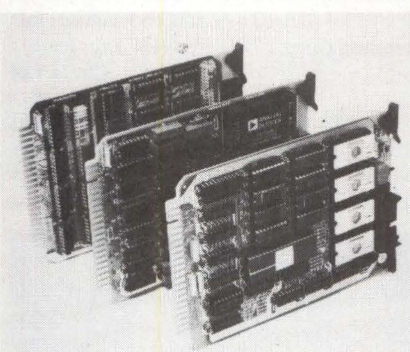
or as fully packaged terminals. The MTBF of the 7700 Series should exceed 2,500 hours. A wide variety of functions and options are available. Quantity-100 prices for OEM mechanisms start at $1,254; terminal models begin at $2,170. **NEC Information Systems, Inc.,** 5 Militia Dr, Lexington, MA 02173. **Circle 152**

600 LPM BAND PRINTER is plug-compatible with DEC, DG and IBM systems. The LP Series includes a standard pedestal-mounted unit with open paper path, and a totally enclosed office quiet version. Both models feature a printer mounted operator activated self-test capability, built-in μP electronics, and 600 lpm speed. They also



include a choice of 48, 64, 96 and 128 character set print bands, paper jam and paper-out sensors, and a long life ribbon cassette. **Centronics Data Computer Corp,** Hudson, NH 03051. **Circle 173**

MODULASONE BOARDS. These 3 modules are fully compatible with the 6802- and 6809-based ModulasOne family of microcomputer modules. Employing a 6802, Module 1020 gives the user a mix of RAM and EPROM, customarily 4K RAM and 8K EPROM. ($260). With the Module 1310 interface board, 32 I/O lines of 2 PIAs can be arranged as all inputs, all outputs, or any combination of inputs and outputs in increments of 4 lines. ($215). Module 1620 is a dual DAC which converts digital signals



within the computer to 4-20mA current signals for industrial applications outside the computer. ($470). All are compact 4-1/2" × 6-1/2" modules. **Adaptive Science Corp,** 4700 San Pablo Ave, Emeryville, CA 94608. **Circle 130**

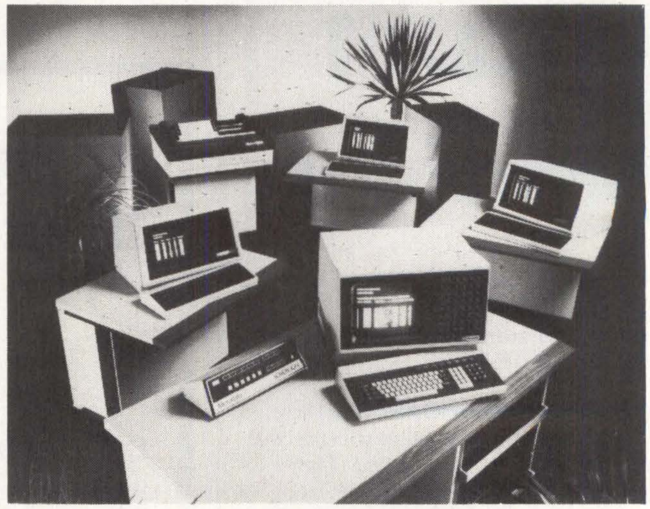
DG-6053 REPLACEMENT will execute all of the commands of the Nova Dasher 6053 except blinking and underlining. Additional features include user or host programmable function keys, line graphs, smooth scroll, user-settable clock and a bidirectional printer port. Each function key can be programmed with any combination of up to 48 characters, codes or graphic symbols and can be chained to simplify operation. The GT-100/D is $1595, qty. discounts available. **General Terminal Corp,** 14831 Franklin Ave, Tustin, CA 92680. **Circle 144**

DG SCREEN-DRIVER-EDITOR, with graphics capabilities, offers users of DG Dasher Terminals a capable and inexpensive screen-driver to create, display and edit data right on the screen. ASCII data is stored in compacted format, saving storage space. Forms are stored as a record on disk file and may be recalled for change at any time. A language linking system allows any given form to be called by as many programs as desired. A C-RITE form requires a single subroutine call, with a change in form rarely requiring a change in the calling program. It allows full cursor control and is completely compatible with most operating systems or languages. C-RITE is sold with either the ASSEMBLER, FORTRAN or BASIC interface for $500. **Country Programmers International, Inc.,** Holiday Inn Drive, White River Junction, VT 05001. **Circle 168**

New Products

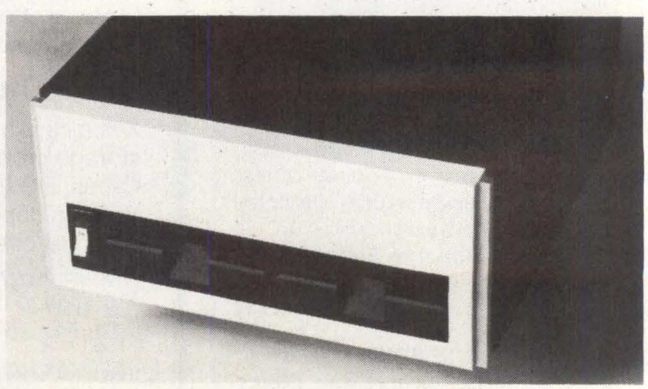
NEW HARD DISK SYSTEM. File controller III, is designed to interface with up to eight widely-accepted Ontel OP-1 Display Computer systems each with its own Disk Controller III to the File Controller III, which in turn interfaces up to two CDC 9448-96 Phoenix 96 MB hard disk drives. Each OP-1 now has access to any disk drive with priorities assigned by the File Controller III. **Ontel Corp.** 250 Crossways Park Dr., Woodbury, NY 11797. **Circle 162**

MULTI-FUNCTION DDP SYSTEM features modular architecture. Expansion is accomplished by adding separate intelligent application processors. All programmable computing elements in a SOVEREIGN system are interconnected by the DataWay which provide high speed data access and data transport between the



system's computers, the operating software and data base stored on disc. Small to large system configurations are available. A medium SOVEREIGN system may consist of 248 kB of processing power, fifteen 520 character CRT's for data entry, three 2000 character intelligent Processing Terminals for supervisory control, local processing and concurrent communications, 20 MB of on-line disc storage, a 45 ips 9 TK 800 bpi tape drive, one 165 cps printer, and one 300 lpm printer. This configuration has a purchase price of $124,150, a monthly lease of $2,440 for 60-months and includes full training and support. **Microdata Corp,** 17481 Red Hill Ave, Irvine, CA 92714. **Circle 135**

5-1/4" MINI-FLOPPY. A compact desktop model, the SCORPIO is targeted at the first time user market. The system is packaged with a DEC LSI-11/2 CPU, 64 kB of memory, serial I/O port, and two double sided, double density mini floppy disk drives. It has a

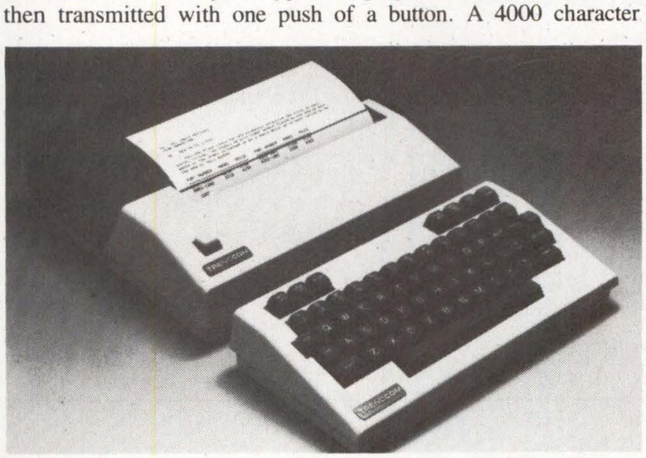


stepping rate 10 times faster than previous mini-floppy systems, is both small and low cost, and provides 1.8 MB of disk storage. **General Robotics Corp,** 57 N. Main Street, Hartford, WI 53027. **Circle 181**

BLOCK-MODE DISPLAY. Format mode, supporting protected and unprotected fields, and the optional line drawing character set enable users to build screen forms that match existing paper forms. Four standard display enhancements include reverse video, underlining, blinking and half-bright. Standard memory accommodates up to two full pages of 80-character lines. Direct screen copy is available with the optional thermal printer. Operates in block, line-

modify and character modes, with full-duplex async data communications. Computer connections are via RS-232-C interface, with an optional 20mA current loop. The HP 2622A display terminal is $2,075. Integral thermal printer is $1,210, the line-drawing character set is $105. **Hewlett-Packard Co** 1507 Page Mill Rd., Palo Alto, CA 94304. **Circle 203**

DESKTOP TELEPRINTERS plug into any standard telephone jack, combines ease of use, quiet operation, and compact size with low cost. Offered in two models, with 40 and 80 cpl. Messages can be transmitted as they are typed, or prepared off-line, edited and then transmitted with one push of a button. A 4000 character



memory stores the message for easy editing. The teleprinters will automatically print messages sent over a regular telephone line from another teleprinter or a computer operating at 110, 200, 300 Baud. Auto answer and answer back features are included. They automatically answer the phone with a programmable identification line of up to 40-characters which verifies that the correct number has been reached. $595 and $695 for the RO models 400 and 800 Teleprinters. Plugging in a model 600 Intelligent Keyboard ($295) converts either teleprinter into an automatic Send/Receive communications terminal. **Trendcom,** 480 Oakmead Pkwy, Sunnyvale, CA 94086. **Circle 159**

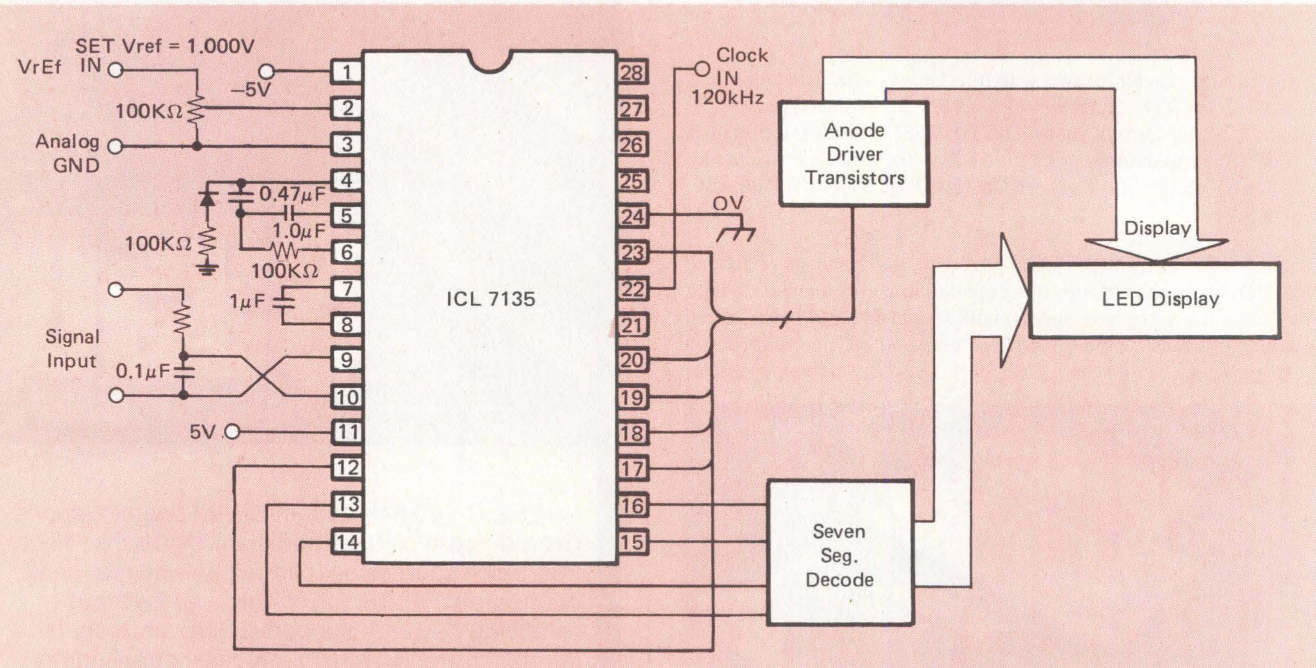
One-Chip ±4-1/2 Digit CMOS ADC Drives LED Display

Add a few standard components, clock and a MUX BCD-to-7 segment decoder/driver and you get a complete visual display DVM/DPM or digital scale, etc. The 7135 was used to drive a LED display as shown. The only critical component required for high accuracy was the external reference.

CMOS precision single-chip ±4½-digit A/D converter ICL7135, has accuracy guaranteed to ±1 count over its entire ±20,000 count range, for ±2.0000V full scale reading. It combines analog and digital circuitry on the same chip and uses proven auto-zeroed dual-slope integration technique conversion to provide high rejection of noise, AC signals and make component selection and clock frequency non-critical.

Performance has auto-zeroed offset to less than 10μV, zero drift of 0.5μV/°C (not including external reference), differential linearity of 0.01 LSB, input bias current of 1pA and roll-over error of 1 count. It has true differential input, true polarity at zero count for precise null detection, and true ratiometric operation. Over and under-range signals are provided for auto-ranging, and visual indication of an over-range condition is accomplished with a blinking display. Outputs are TTL compatible; six auxiliary I/Os exist for interfacing to UARTs or μPs.

Intersil, Inc.
10710 North Tantau Ave.
Cupertino, CA



ICL 7135 one chip ± 4 1/2 digit CMOS A/D converter drives LED display.

Try Speech Synthesizers For Simple Applications

TI's Speak & Spell, circa 1978, is an excellently-designed and implemented "toy" with a vocabulary of approximately 300 words (including alphabet, numbers and phrases). Voice quality generally is good, although some words are not very clear ("ocean" sounds like "unction"). The TI synthesizer components are only becoming available recently, so that it largely served to whet the appetite of developers of μP systems.

Most speech synthesis ICs and boards feature sample vocabularies to allow potential users to evaluate performance and develop prototype equipment. ICs and boards are expensive in small quantities, but will drop quickly. Developing specialised vocabularies for specific applications is typically $250 per word or more.

If you wish to use speech synthesis devices in limited quantities, expect difficulties; sample vocabularies offered by various manufacturers might suit a few applications, but are inadequate where your application requires specialised vocabularies. The only alternative for limited applications is for you to create your own vocabularies using phoenetic synthesizers, such as the Votrax SC-01 [5]. Still, much work could be involved, with voice quality not likely to equal that of expertly developed vocabularies.

A solution for limited applications would be for synthesizer manufacturers to offer ROMs containing specialised vocabularies, such as for instrumentation and WP. Since 100 words, properly selected, would satisfy most applications within a general area, cost to the limited-use OEM would not exceeed the sample vocabularies currently available. Such ROMs at a reasonable price would accelerate introduction of μP applications employing speech synthesis in general, since value of speech output would be proven to end users and would gain general acceptance in systems of limited production (scientific and technical instruments, etc).

National Semiconductor's DT1050 Digitalker synthesizer, discussed in February's "Designers' Guide To Speech Synthesis" (pp. 53 - 57), has a speech processor (SPC) and two, 4-kB ROMs which contain a sample vocabulary of 135 words (including alphabet and numbers sufficient to count up to a billion), two tones, five periods of silence and the phrase "This is Digitalker." The author used an MC6802 μP circuit with 2716 EPROM, for exercising Digitalker.

This design can be simplified further by eliminating the 74LS244 buffers. The INTR output from the SPC can be inverted and used to interrupt the MC6802 via the NMI input. The SPC will safely interface to the MC6802, although the clock input to SPC is not TTL compatible and must be pulled up to +12 V.

Digitalker software is simple: sentences are constructed by equating Digitalker codes to their equivalent word and then using the words, rather than codes, to create the spoken sentence.

Digitalker's vocabulary is inadequate for all but very simple applications. For example, if you use Digitalker for a speaking clock, it is impossible to have a spoken calendar in the clock. And, vocabulary is almost sufficient to construct a speaking multimeter — except that "ohm" is lacking. This is disappointing. How can an OEM make a convincing demonstration

```
;               DIGITALKER EXERCISE ROUTINE
;
TALK_REG        EQU         2000H           ;START AND SAY WORD
WAIT_REG        EQU         4000H           ;b7=0 IS WAIT
;
PAUSE           EQU         71
;
                ORG         0F800H
SENTENCE:
                FCB         PAUSE
                FCB         OH,PAUSE,HI
                FCB         PAUSE,PAUSE,PAUSE,PAUSE,PAUSE
                FCB         THE,POUND,IS,TWO,DOLLAR,SS
                FCB         AND,THIRTY,TWO,CENT,SS
                FCB         PAUSE,PAUSE,PAUSE,PAUSE,PAUSE
                FCB         SIX,MILLION,TWO,HUNDRED,THOUSAND
                FCB         KILO,METER,SS
                FCB         PAUSE,PAUSE,PAUSE,PAUSE,PAUSE
                FCB         NINE,TIME,SS,NINE,EQUAL,SS,EIGHTY,ONE
                FCB         PAUSE,PAUSE,PAUSE,PAUSE,PAUSE
                FCB         THE,WEIGHT,IS,THREE,POINT
                FCB         TWO,FIVE,CENTI,GRAM,SS
                FCB         PAUSE,PAUSE,PAUSE,PAUSE,PAUSE
                FCB         PLEASE,STOP,PAUSE,IT,IS,TIME,FOR,TEA
                FCB         PAUSE,PAUSE,PAUSE,PAUSE,PAUSE
                FCB         THE,TIME,IS,PAUSE,TWENTY,ONE,HOUR,SS
                FCB         THIRTY,EIGHT,MINUTE,SS
                FCB         PAUSE,PAUSE,PAUSE,PAUSE,PAUSE
                FCB         CHECK,FUEL,FLOW,PAUSE,IT,IS,TOO,LOW
                FCB         YOU,ARE,IN,DANGER
                FCB         255
;
PROGRAM:
                LDS         #127            ;SET UP STACK
;
                LDX         #SENTENCE
                BSR         SAY_SENTENCE
;
SAY_ALL         CLRA                        ;SAY ALL WORDS IN VOCABULARY
LOOP_ALL        BSR         SAY_WORD        ;SAY WORD CODE IN ACCA
                INCA
                CMPA        #144
                BNE         LOOP_ALL
;
;
                BRA         PROGRAM
;
;
SAY_WORD:
                PSHB
                STAA        TALK_REG        ;LOAD WORD INTO DIGITALKER
WAIT_SPEECH     LDAB        WAIT_REG        ;WAIT UNTIL WORD IS SAID
                BPL         WAIT_SPEECH
                PULB
                RTS
;
SAY_SENTENCE:
                LDAA        X               ;SPEAK CODES UP TO 255
                CMPA        #255
                BEQ         SAY_SENTENCE_END
                BSR         SAY_WORD
                INX                         ;MOVE TO NEXT ONE
```

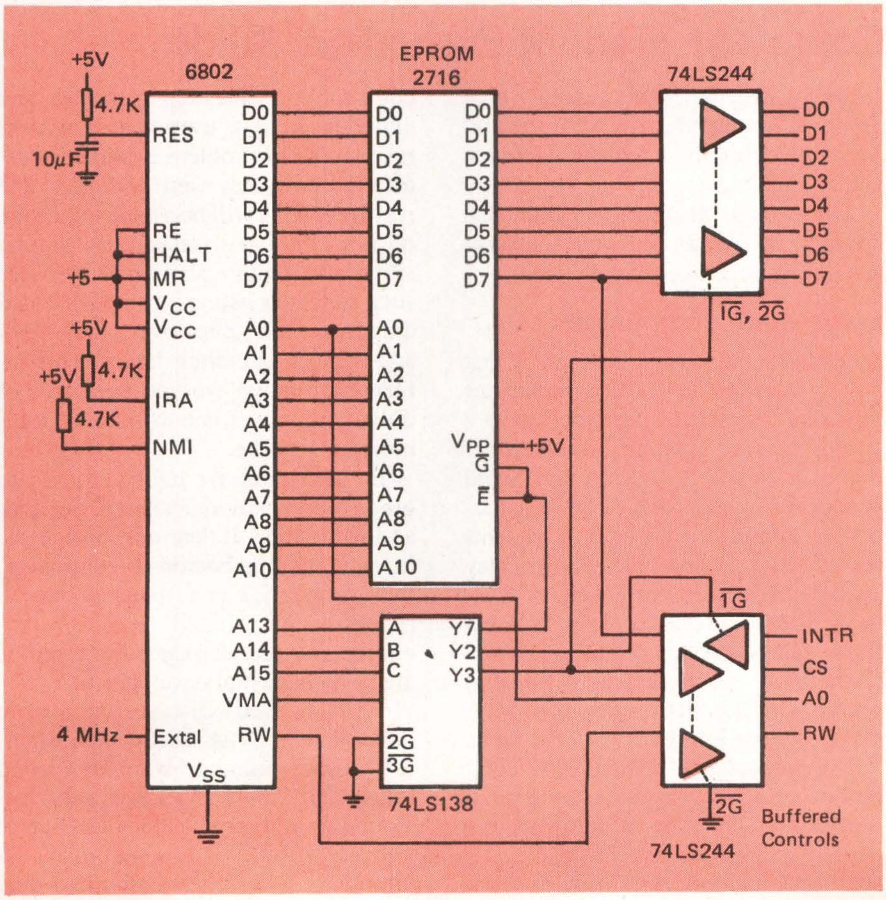


Figure 1: Diagram of the national Semiconductor DT 1050 Synthesizer.

of how powerful an addition that voice output can be?

Other than sample vocabulary limitations, Digitalker is convenient to interface and program. The SPC chip's need for non-TTL level voltage and clock is a minor nuisance. Some audio output filtering is necessary, but need not be elaborate. Voice quality is good, although sentences constructed from individual words often sound artificial because of improper inflection.

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Reading RG6 2AX, England

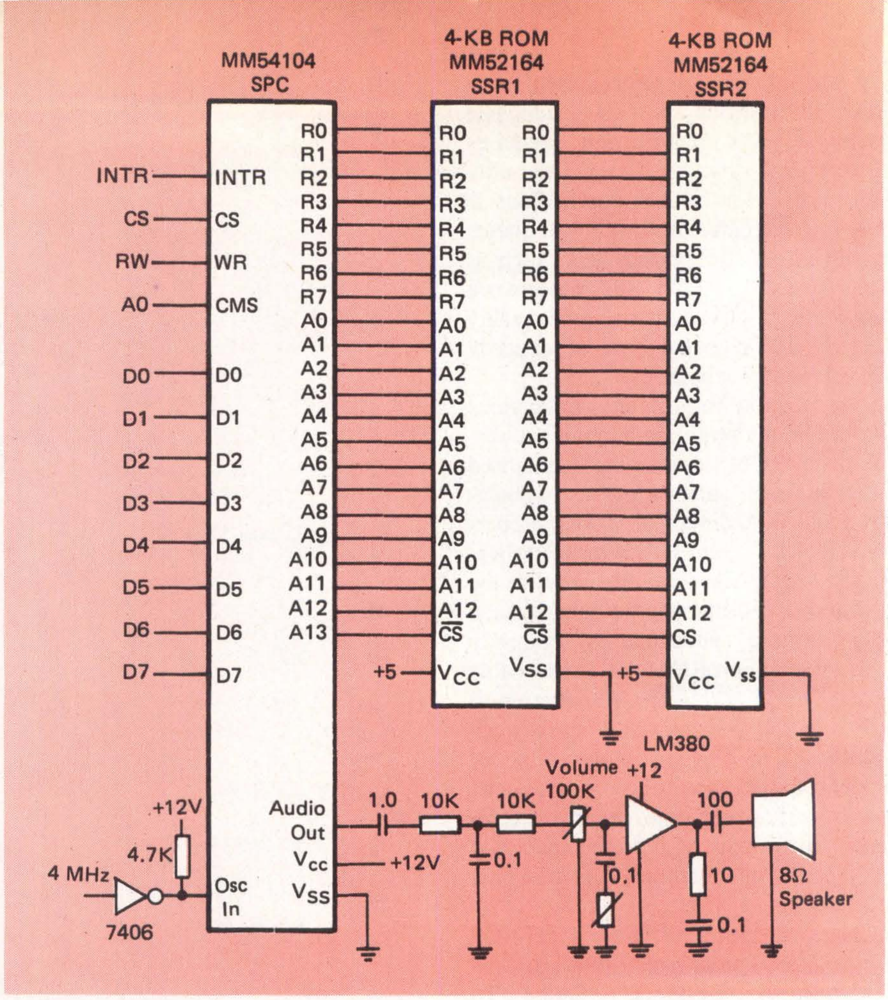

Figure 2: Micropocessor circuit for exercising the Speech Synthesizer.

Computer Product Evaluation Guide

In today's market, determining which computer product best fits your specific needs is an involved process. Here are some guidelines.

Three considerations include the product, cost/value ratio and company. Weighting depends on application.

investigate companies

Investigate only those companies that have manufactured such computer products for several years and have a strong market position. Do consider manufacturers, however, that build products aimed specifically at a particular application. Limiting systems reviewed lessens the chance a firm may drop a product line or go out of business. The company should have direct field sales, service and application engineers — complimented (ideally) with a solid distributor network. Multiple response improves response time.

Do not judge a company by competitor input; all companies have problems at some time. Comments are usually inaccurate and misleading. If such information does disturb you, confront your sales rep or another user experienced in its use and analyze their responses. In problem evaluation, determine how they were addressed and resolved. This will be a good indication of how they will respond in similar situations. Inquire about other services such as ladder listings, computer-aided diagnostic assistance over phone lines and service operating hours. This information may save you thousands of dollars in downtime costs and technician assistance.

Beyond their reputation, look into other products manufactured, services and warranties. If their only business is in, say, add-in boards or controllers, they probably can respond to special requests, and should have a better-engineered product since more profits are reinvested into development.

Will you need assistance with system development? Ask about applications assistance, training, warranty period (parts and labor) and associated cost. Training and applications assistance policies differ. For some manufacturers, these services cost more than hardware; in others, it's free. Warranty periods may vary from 90 days to 18 months and may not include labor.

cost/value ratio

Do not measure cost in dollars. Develop a personal cost/value (feature) ratio by determining base features needed to meet specific needs (number of I/O, memory, etc.). Determine their costs and compare system prices.

Next, evaluate enhancements included with the base cost as standard, but not immediately necessary. They could be math functions, diagnostics or free training. Although initially these extra features may be unimportant, experience shows that once these features are understood, their uses and your needs expand exponentially. Since this could reduce future expansion costs of a system by 50 - 75%, establish a features list which includes solutions to every control problem you ever experienced; and, determine what the unit offers as options (and costs) to achieve these limits.

Remaining potential costs are for

hidden requirements. Some controller systems lack individually-fused outputs and may need special loading to prevent intermittent on/off cycling of I/O. Other systems require isolation or ferroresonant transformers to nullify line transients. Since these and other "special service" costs are not in a quote, include such costs into systems requiring such peripherals.

the product

While evaluating system cost, appraise the product. First, is it large enough to fit your needs? Determine memory size, discrete I/O limits and analog I/O limits. In evaluating memory size, do not ask how many "words" are available; a "word" in the PC industry lacks a standard definition. The best memory size criteria is how many "bytes" are available, and in turn, how many bytes are required per contact, per timer and any special functions. Most manufacturers use CMOS memory — not core or EPROM. CMOS, which yields low-cost, high-speed logic-solving, is easily alterable. Core is expensive; in a system over 16Kbytes (8K 16-bit words), logic solving time is prohibitive. EPROM is fast, but for a program change, it is a frustrating, time-consuming process.

Besides memory type, determine how system logic is solved. The best one has all special functions written in micro-code and resident in the PC's main processor. These special codes may include such functions as table-to-register moves, PID, "get status", ASCII, "bit manipulation", "bit compare" and others. Such features eliminate the need for data to be transmitted from one memory to another. Data transmission lengthens logic solving time, increases user logic and programming time, and loses data during transmission.

Most suppliers, having more than one product, offer a variety of units and communications systems. All must be compatible with the communications network and, if possible, the same programmer and tape loader. Although often not considered a major evaluation factor, I/O could also be reviewed; check available types, current and voltage capabilites and cycle times. If I/O capabilities are important, their specs may be important in overall system response.

Two controller products to consider are programmer and tape loader. Using a CRT programmer, the easiest method available, should permit you to program in a "free format" and allow systems control and monitoring. Free formatting is the "unrestricted" use of nested branches, timers and special functions. Ability to disable logic and force it to an active state and control/monitor the system saves hours of set up and troubleshooting time. It is a must.

Some CRT's can make tapes of your logic. Try to purchase a system with a one-package programmer and tape loader to save money and increase functionality. Investigate enhancements and alternatives to programming systems. An example of an alternative is LED/numerical key pads which permit disabling I/O (as with the CRT) and also allow remote limit-setting of timers and counters.

Don't select a system on price alone; it could limit your expansion capabilities. But if cost is a major factor, measure the true cost and consider services and training.

Arne L. Watland
Gould Inc., Modicon Div.
Troy, MI

DEC-wise

A DEC-compatible directory was launched in our January issue. It was the first such concentrated discourse in any computer-aligned magazine.

The subject matter proved so popular that we are running, in the July issue, more material. There'll be more information on the **whys** and **hows** of DEC compatibility. And there'll be some interesting comments on the whole subject itself, showing why computer compatibility is becoming an important part of *Digital Design's* editorial direction. Look for us in July.

Input-Output

Have you got something to say and no place to say it?

Write us, your comments and suggestions are always welcome.

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