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VOL. 12
NO. 3

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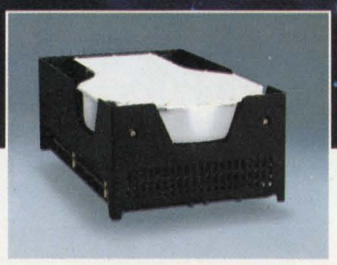

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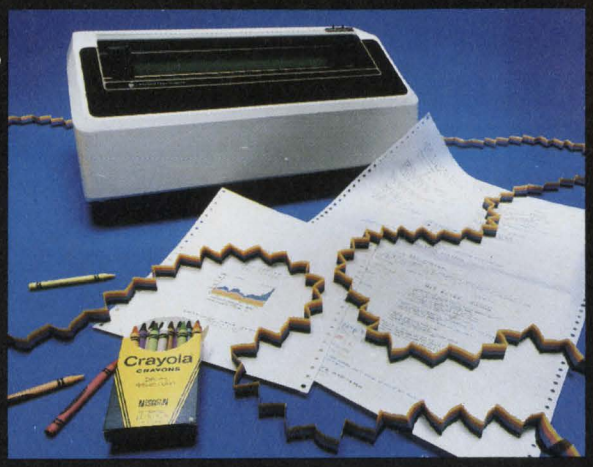

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MARCH 1982
VOL. 12, NO. 3

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Postmaster, send address correction to Morgan-Grampian Publishing Company, 1050 Commonwealth Avenue, Boston, MA 02215. 2nd class postage paid at Boston, MA and additional mailing offices.

COMPUTERS/SYSTEMS

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Because dot-matrix printers use the same fundamental technique to present graphic data as CRTs, and because they now offer increased speed and resolution, they've become ideal low-cost graphic hard copy devices.

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Now that dot matrix printers produce copy sharp enough for office use, they must conform to the noise restrictions imposed by the office environment.

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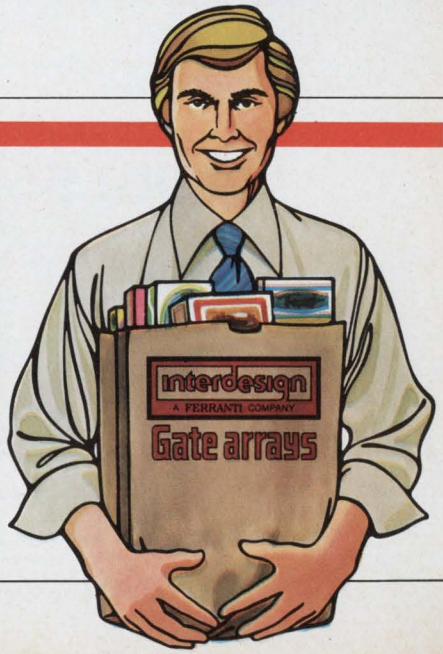

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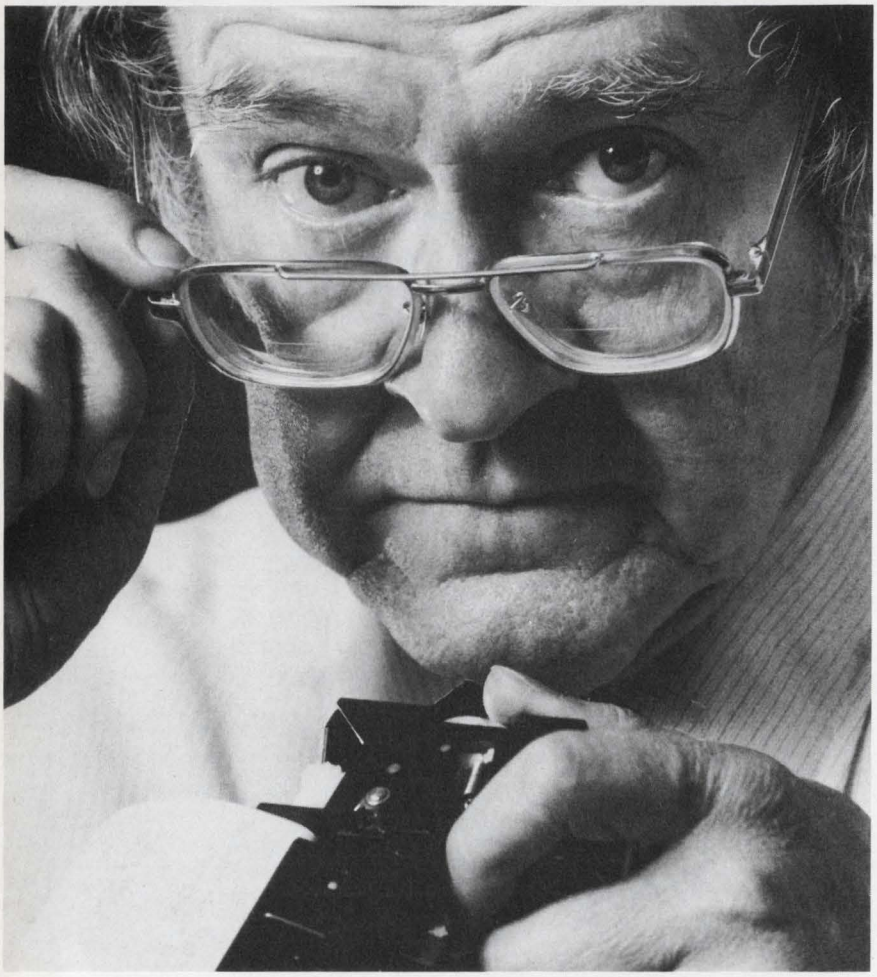
Check Out Our Printers



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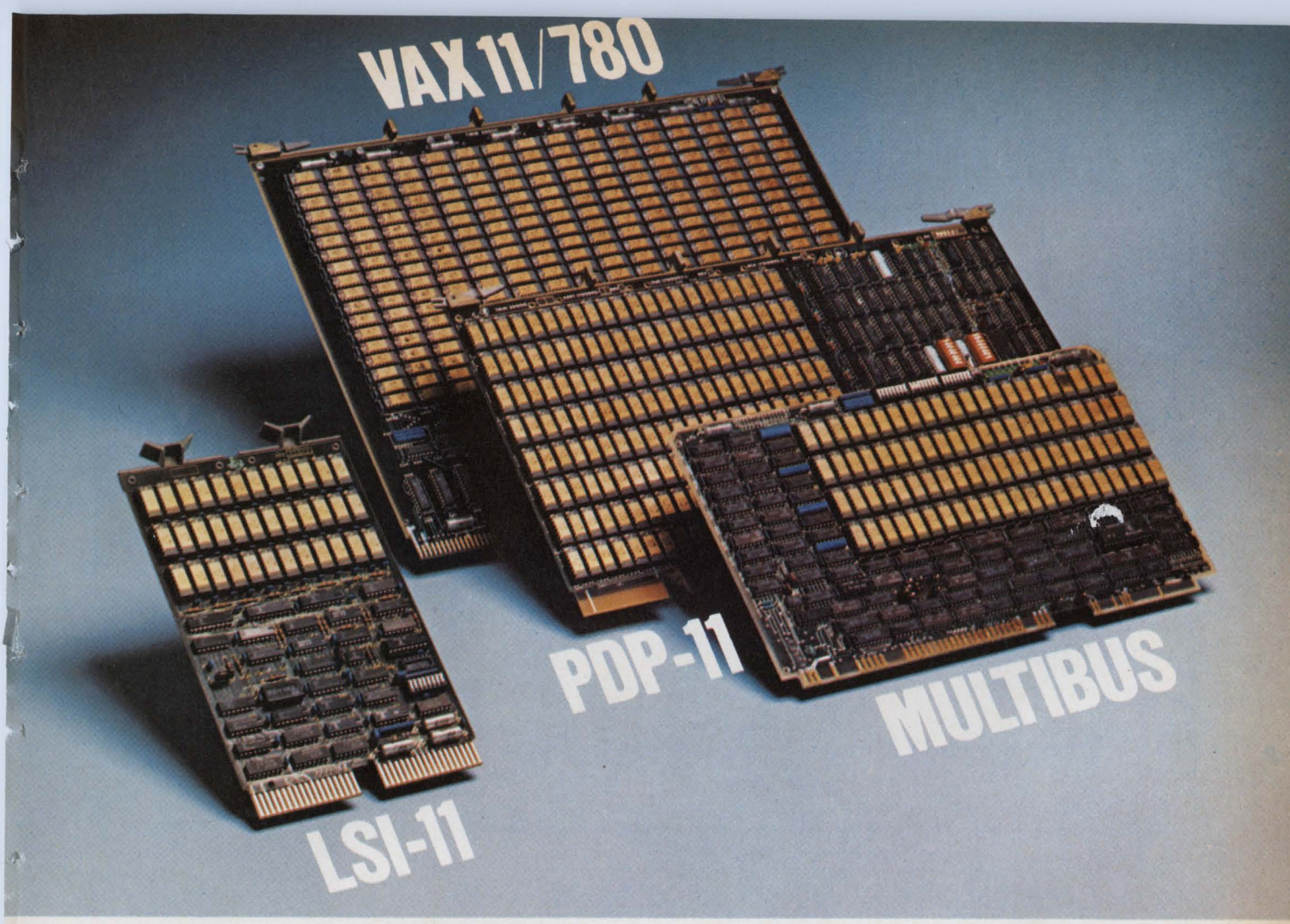
ISSN 0147-9245

Published monthly and copyright © 1982 by Morgan-Grampian Publishing Company, 1050 Commonwealth Avenue, Boston, MA 02215. Second class postage paid at Boston, MA and additional mailing offices.



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PDP-11†	TMM20000[2]		X	X	X	X		X
VAX†	TMM30000					X	X	X
Multibus‡	TMM40010[2]	X	X		X	X		

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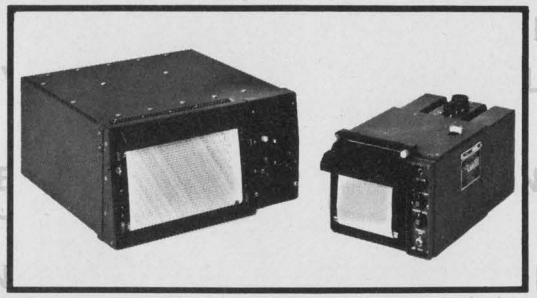
The Track Record That Says It All . . .



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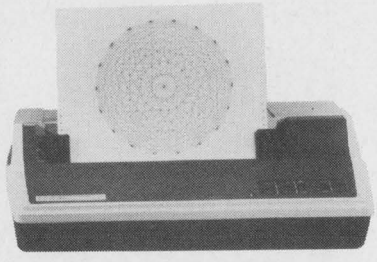

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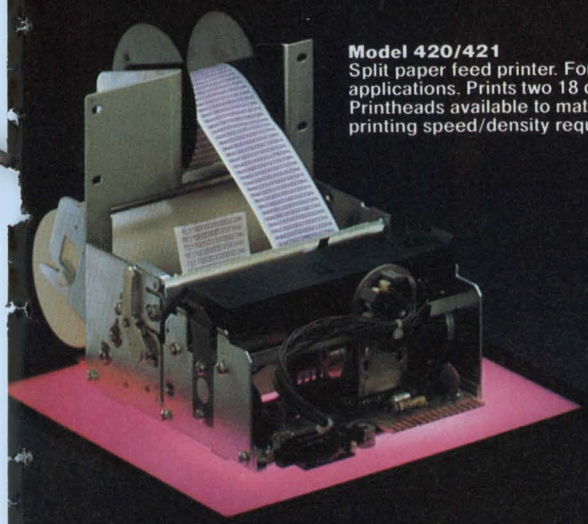

Model 420/421
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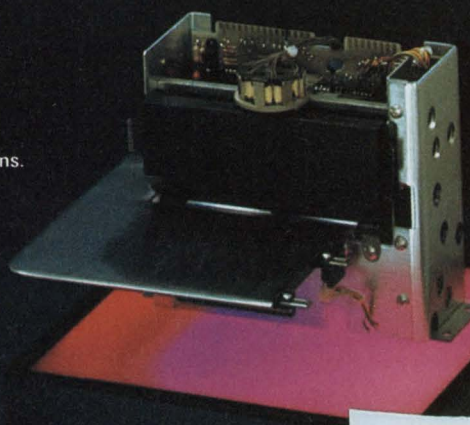

Model M-400
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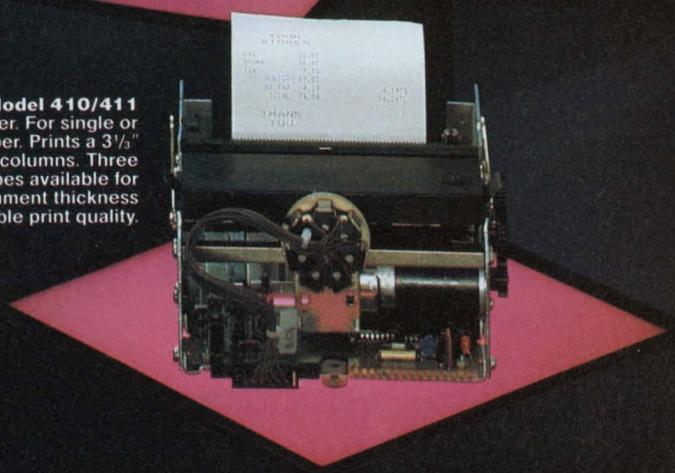

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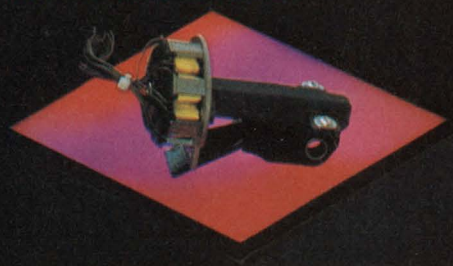

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Letters

Fig-FORTH Foul-Up

Dear Editor:

We here at Blue Sky were overjoyed to see our fig-FORTH product for the Ohio Scientific computer systems get exposure in your magazine (*FORTH Directory*, January, 1982). However, there was one small error in the listing. The price as quoted in your directory is $875. The correct price is $75 each. It seems that somewhere along the line, the $ got interpreted as an 8 and thus the error. Needless to say, most OSI users will take one look at the price quoted in your directory and disregard our product without a second thought. We feel (of course) that we have the best product available for OSI users, and would appreciate it if in some way you could make this known to your readers.

Steve McIntosh
Blue Sky Products
729 East Willow Street
Signal Hill, CA 90806

Operating Systems

Dear Editor:

As much as I found Peter Wolochow's article "Microcomputer Operating System Trends" (Dec. 81) good reading, appreciating only too well the problems of comparing operating systems, I was a little disappointed to note the disservice he did for the non-Intel operating systems by improperly allocating "no"s in his comparison table. Perhaps this was due to not realizing that different operating systems provide the same features, but not necessarily the the same names for them. For example, both RSX-11M and MTOS-86 provide packet transmit/receive primitives which are mailboxes by another name. Indeed UNIX's pipes might fall into the "yes" category under mailboxes. Also, UNIX does manage interrupts and perform asynchronous I/O and is both multiprogramming and multitasking — with alterable priorities. Others more experienced in some of the other operating systems listed may well argue against some of the other "no"s also.

Alex D. France,
Jubilee House
120 Blyth Road
Hayes, Middx. UB3 1DL
England

Fiber Optical Noise Reduction

Dear Editor:

Mr. Kalbach's recent article, "Designer's Guide to Noise Suppression" in your January 1982 issue was very informative and helpful. One of the most powerful techniques of avoiding noise and grounding problems is the use of optical fiber transmission. The all-dielectric cable is immune to noise pickup and it also does not radiate EMI. Since each end of a fiber optic link can be totally isolated from ground, its common-mode noise rejection is excellent.

The points Mr. Kalbach's article referred to should be implemented wherever possible. Even with a fiber optic link, noise can be introduced into the electronics by way of the power supplies. By taking advantage of fiber optic technology together with good engineering practice referred to in this article, system noise problems can be eliminated.

Neil P. Albaugh
Burr-Brown
Box 11400
Tucson, AZ 85734

Editorial Noise Reduction

Dear Editor:

Your editors deserve credit for doing what I believe to be a first-rate job on condensing my technical paper and still leaving essentials. I have already received a number of comments from readers who have expressed interest in the subject and the possibility of my doing some consulting in that technical area. Other responses were from past associates who, like myself, have "retired" and cannot seem to stay out of the business. Thank you again.

J.F. Kalbach
920 Alto Pine Dr.
Altadena, CA 91001

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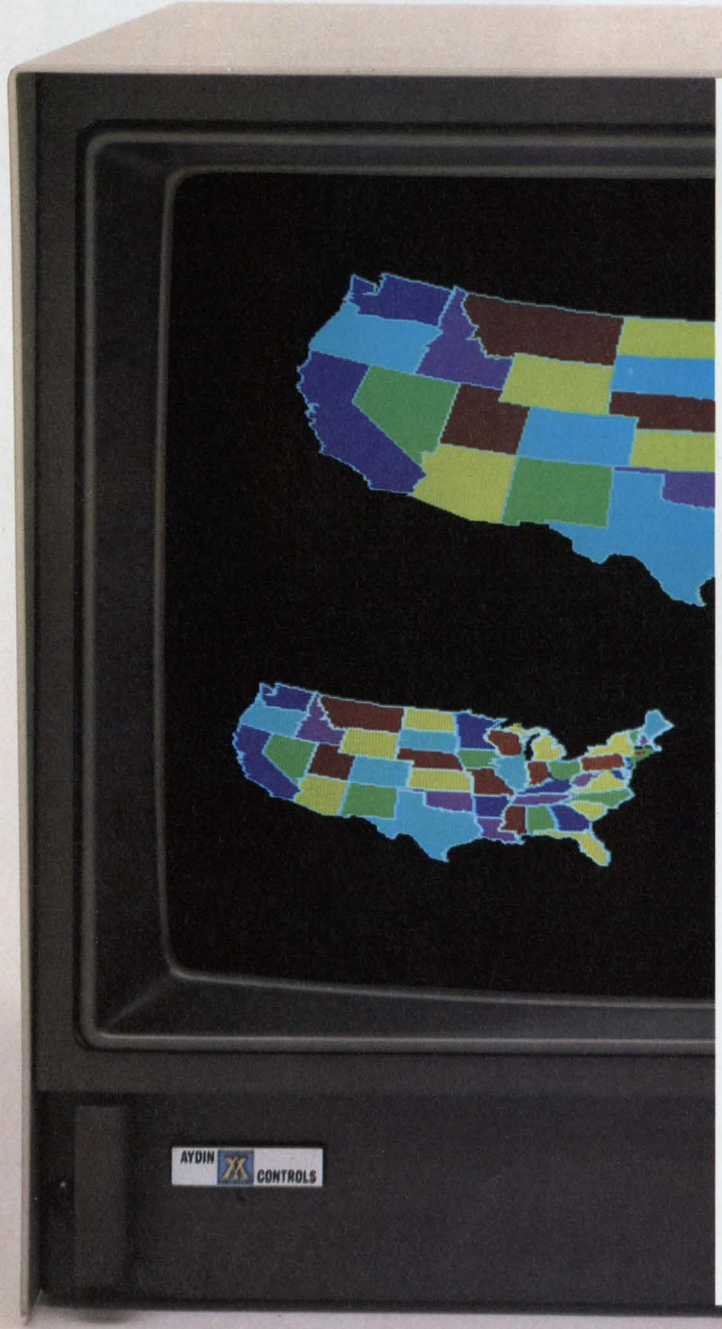
Aydin Patriot™ Color Monitors

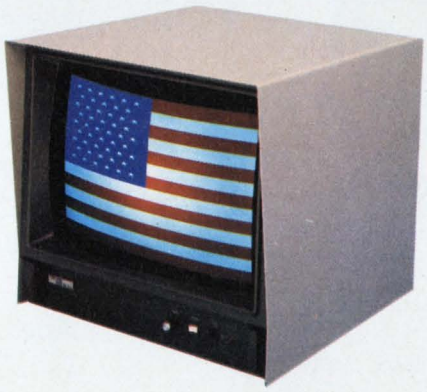
Aydin Controls introduces its American-made, in-line gun, high resolution Patriot Series of Color Monitors.



Aydin Controls, a leader in high resolution color display terminals, now manufactures Patriot™, its own in-line gun series of color monitors. The Patriot series will supplement Aydin's well known family of delta and in-line gun monitors.

Patriot's 13-inch Model 8810 and 19-inch Model 8830 both offer the latest state-of-the-art features plus all of the advantages of American technology and manufacturing. Patriot features high video bandwidth, wide horizontal line rates, fixed convergence, excellent high voltage regulation, modular construction, analog or TTL inputs and rack mountability. The Patriot Series can be customized to fit special needs.

Patriot monitors provide outstanding performance at an attractive price coupled with an 18-month OEM warranty; off-the-shelf availability; quick delivery of spare parts; and fast, reliable service. For more information contact Aydin Controls, 414 Commerce Drive, Fort Washington, PA 19034. Tel: 215-542-7800 (TWX 510-661-0518).



AYDIN CONTROLS

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Calendar

April 4-7

Southeastcon '82 (IEEE et al.) Destin, FL. Contact: Carolyn C. Schauble, U.F. Graduate Engineering Center, PO Box 1918, Eglin Air Force Base, FL 32542; (904) 882-5614.

April 6-8

Fifth International Symposium on Programming. Torino, Italy. Contact: S. Ronchi, ISI, C.M. D'Azeglio 42, 10125 Torino, Italy.

April 8-9

Automated Software Engineering Tools. San Francisco, CA. By Dr. Edward F. Miller. What software tools are available, how to best use them, where do you get "good" information about them. Contact: Gloria Kulbe, Software Research Assoc., Box 2432, San Francisco, CA 94126; (415) 957-1441.

April 13-14

Computer Network Performance Symposium. College Park, MD. Examines local networks, related technologies. Contact: Rebecca Hutchings, Honeywell Information Systems, MS1007, 7900 Westpark Dr., McLean, VA 22102; (703) 827-3982.

April 13-16

Software Project Management. Boston, MA. Develop and improve skills required to manage real-time micro and minicomputer-based projects. Also held in Washington, DC, May 18-21; and San Francisco, May 25-28. Contact: Ruth Dordick, Integrated Computer Systems, 3304 Pico Blvd., Box 5339, Santa Monica, CA 90405; (213) 450-2060.

April 13-16

Sixth European Meeting on Cybernetics and Systems Research. Vienna, Austria. Contact: Prof. Robert Trappl, Dept. of Medical Cybernetics, University of Vienna, Freyung 6/2, A-1010 Vienna, Austria.

April 14-16

14th Annual Southeastern Symposium on System Theory. Blacksburg, VA. Contact: Dr. Richard Claus, Dept. of EE, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061.

April 15-16

Software Quality Assurance Technology. San Francisco, CA. By Dr. Edward F. Miller. How, when, how much and with what effect should programs be tested to assure their quality. Contact: Gloria Kulbe, Software Research Assoc., Box 2432, San Francisco, CA 94126; (415) 957-1441.

April 18-22

Common-An IBM Computer Users Group. Miami Beach, FL. Over 130 sessions to keep the Data Processing Professional well informed and up-to-date on new developments. Contact: David G. Lister, COMMON - F82, 435 N. Michigan Ave., Chicago, IL 60611; (312) 644-0828.

April 19

Grounding Seminar/Workshops. Chicago, IL. Covers Effective Grounding of Electrical Systems and Equipment. Also held on Apr 19; May 18; June 15; Sept 21; Oct 12; Nov 16. Contact: Ecos Electronics Corp., 205 W. Harrison St., Oak Park, IL 60304; (312) 383-2505.

April 19-20

New Trends In Rapid IC Processing Techniques. Palo Alto, CA. Covers lasers, electron beams and incoherent sources. Also, **Materials Characterization For Ion Implantation.** Reviews techniques and their applications for process development, production control and yield improvement. Contact: Continuing Education in Engineering, Univ. of California Extension, 2223 Fulton St., Berkeley, CA 94720; (415) 642-4151.

April 19-21

ACM SIGSOFT Second Software Engineering Symposium. Columbia, MD. Contact: Dr. Marvin Zelkowitz, Dept. of Computer Science, University of Maryland, College Park, MD 20742.

April 19-21

All Electronics/ECIF Show. Barbican Centre, London. Contact: British Information Services, 845 Third Ave., New York, NY 10022; (212) 752-8400.

April 19-21

IFIP International Symposium on Local Computer Networks. Florence, Italy. Contact: Greg Hopkins, Ungermann-Bass, Inc., 6 New England Exec. Park, Suite 400, Burlington, MA 01803; (617) 273-5858.

April 19-22

International Conference on Computer Capacity Management. San Francisco, CA. Contact: Armond Inselberg, Institute for Software Engineering, 535 Middlefield Rd., Suite 200, Menlo Park, CA 94025; (415) 493-0300.

April 20-22

AUTOFACT. Mexico City, Mexico. Focuses on computer integrated manufacturing and the Automatic Factory. Also held in Singapore, July 20-22; and Philadelphia, Nov 8-11. Contact: Society of Manufacturing Engineers, One SME Dr., Box 930, Dearborn, MI 48128; (313) 271-1500.

April 20-23

Hands-On Microprocessor Troubleshooting. Washington, DC. Learn practical troubleshooting techniques. Also held in Philadelphia, April 27-30; and San Francisco, May 11-14. Contact: Ruth Dordick, Integrated Computer Systems, 3304 Pico Blvd., Box 5339, Santa Monica, CA 90405; (213) 450-2060.

April 21-28

Hanover Fair '82. Hanover, West Germany. Contact: Hanover Fairs Information Center, PO Box 338, Whitehouse, NJ 08888; (201) 534-9044.

April 22-23

13th Annual Pittsburgh Conference on Modeling and Simulation (IEEE et al.). Pittsburgh, PA. Contact: William G. Vogt, Modeling and Simulation Conference, 348 Benedum Engineering Hall, University of Pittsburgh, Pittsburgh, PA 15261.

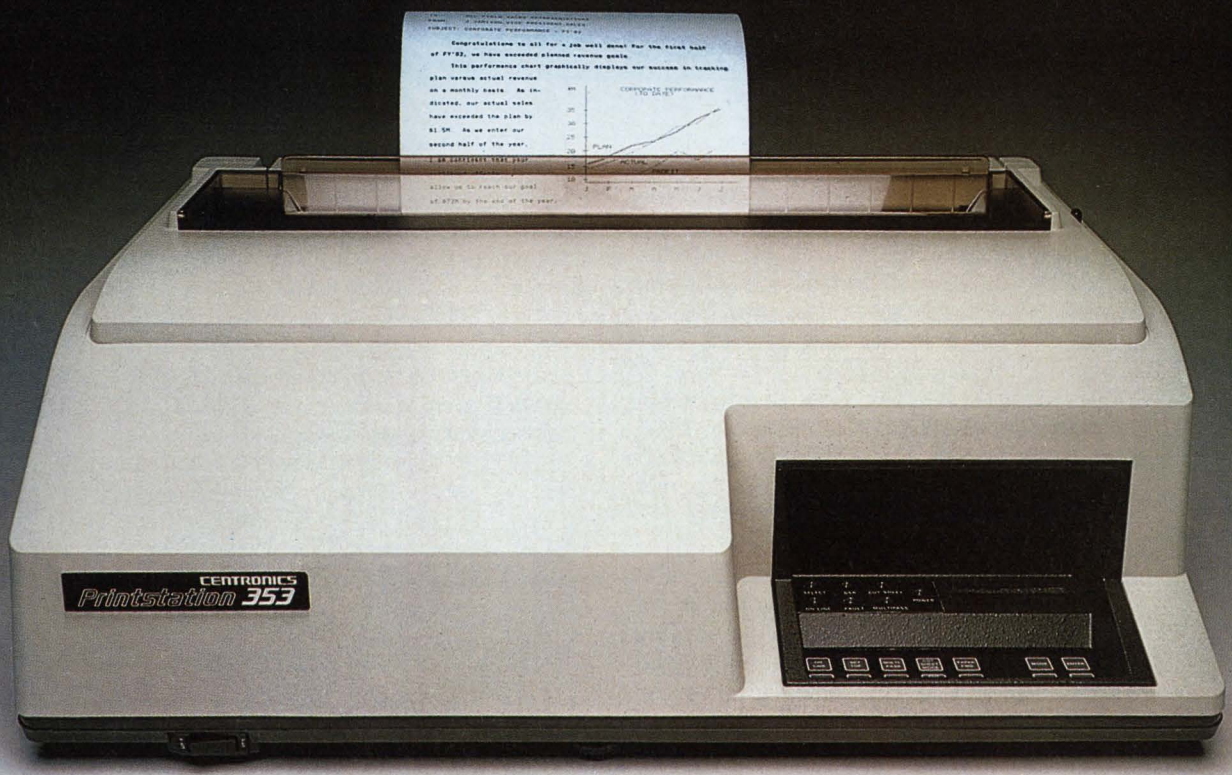
April 26-29

Ninth Annual International Symposium on Computer Architecture. Austin, TX. Contact: Computer Architecture, PO Box 639, Silver Spring, MD 20901; (301) 589-3386.

April 27-29

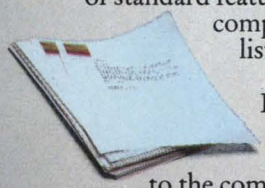
INFO/Manufacturing 82. Chicago, IL. Covers entire spectrum of information systems for manufacturing companies. Contact: Clapp & Poliak Inc, 245 Park Ave., New York, NY 10167; (212) 661-8410.

THE PRINTSTATION 350. ITS BEAUTY IS MORE THAN SKIN DEEP.



THE MULTIFUNCTION PRINTER WITH UNMATCHED PAPER HANDLING CAPABILITY.

If all you look at is the handsome, office-styled cover you'll miss the real beauty of its functionality, its revolutionary paper handling design and its list of standard features that even competitors' "options" lists can't match.



Centronics' new Printstation 350 is truly the "one-printer solution to the complete range of data processing, business processing, and word processing printing needs".

SEMI-AUTOMATIC PAPER HANDLING... FAN-FOLD, MULTI-PART FORMS, AND CUT SHEET loaded instantly and switched rapidly. In fact the Printstation 350 can be loaded with cut sheets faster and easier than a typewriter.

LETTER QUALITY PRINTING, a word processor's dream... using multipass technique for high resolution, high density characters.

PIN-ADDRESSABLE GRAPHICS PLUS "NO-WASTE" DEMAND DOCUMENT REMOVAL deliver true business processing capabilities.

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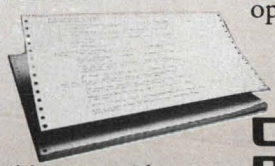

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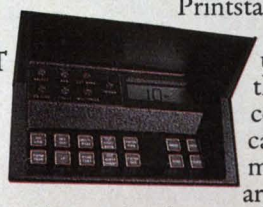
So don't judge a printer by its cover especially when it's one of the Printstation 350 family. Because underneath there's a unique collection of capabilities, mechanical architecture, and electronics that provide a level of versatility we call PRINTSTATION PROCESSING. But if beauty is in the eye of the beholder, you should behold the Printstation 350 in operation. For more information or a demonstration, contact us today.



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News Update

RCA, Philips And Signetics Sign Agreement

RCA, Philips and Signetics have signed a design and development agreement for an advanced new family of high speed CMOS logic chips under which each will be an alternate source for approximately 180 new circuits. The new devices are expected to start becoming available in the second half of 1982. Both RCA and Philips have previous experience in CMOS technology: RCA Labs in Princeton, NJ, pioneered the CMOS concept in 1961, and in 1968 Philips Research Labs in Eindhoven, The Netherlands, contributed the isolation technique known as LOCOS (local oxidation of silicon).

The agreement covers common design rules and the exchange of tapes for computerized mask generation so that the companies can alternate source each others' circuits. The new types will use compatible advanced 3-micron CMOS technology and processes, so that circuits developed by either company can be processed easily at their respective wafer fabrication centers in Europe and the United States.

Minicomputer Technology Purchased By E-H International

Minicomputer Technology (MCT), a privately held corporation, has been purchased by E-H International, Inc. for $600,000. MCT will continue operations in Palo Alto, CA under its own name, as a wholly-owned, but autonomous subsidiary of E-H. MiniComputer Technology manufactures and markets a full line of single-board disk drive controllers for Digital Equipment Corporation, Data General and Perkin-Elmer minicomputers. Founded in 1973, the company's 1981 sales approached $4 million.

Rockwell To Second Source CMOS Process

Rockwell International has disclosed that its Electronic Devices Division is holding discussions with a number of US and Japanese semiconductor firms to secure a second source for an advanced CMOS process. Charles V. Kovac, vice president of marketing and business development, said his firm has developed a CMOS process in its Microelectronics Research and Development Center, and plans to put this process into production during 1982 in its Newport Beach factory. To assure second-source capability to support its marketing efforts, the division is investigating the compatibility and producibility of CMOS processes now being used by other firms in the US and abroad with the objective of negotiating a production licensing agreement. The division is directing its CMOS processing plans at the production of μP, μC and specialized communications devices, Kovac said. In response to questions about a report published in Japan, Kovac confirmed that Sharp Corp., Osaka, Japan is among firms with which discussions are in progress, but "in no way concluded," and declined to name other firms.

Mostek Establishes Array Logic Dept.

Mostek has announced a further expansion of its semiconductor product base by establishing an Array Logic Product department to offer semicustom logic circuits to the commercial market. The new group will have responsibility for the design, production and marketing of circuits based on gate array technology developed by the United Technologies Microelectronics Center in Colorado Springs, Colorado. Department manager Lynn Reed said the group will be offering a broad line of arrays using up to 4,000 gates. First products are scheduled for mid-1982. The commercial gate arrays will use double-level metal silicon-gate CMOS processing with 3-micron geometries. The devices will be offered in a variety of packages depending on customer requirements, including standard DIPs and leadless chip carriers.

Zilog And Litton Enter Ada Agreement

Zilog and Litton Systems' Data Systems Division have agreed in principle to cooperate on a program to convert the Ada programming language to run on Zilog's 16-bit System 8000 and to generate code for the Z8000 μP family. Zilog President Manny Fernandez and Leon Bloom, Litton's director of advanced Army and Air Force Programs, said the agreement will be formalized during the next several weeks. The program will involve the develop-

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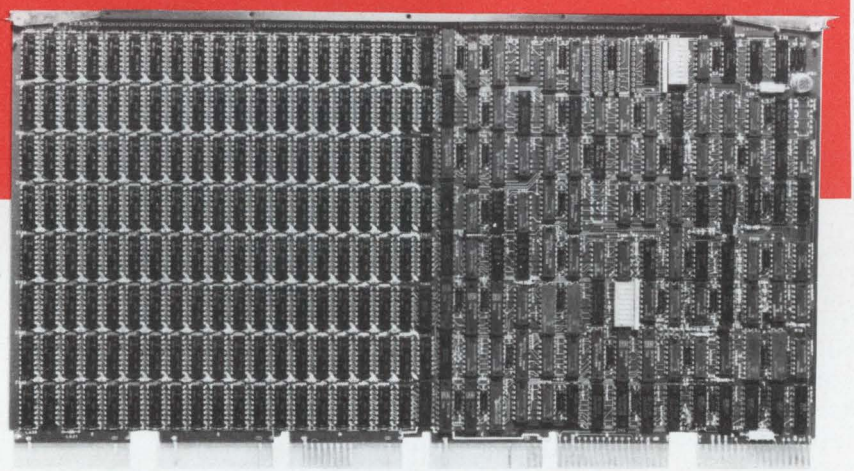

FROM THE LEADER

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The chart provides a glimpse at the industry-pacesetting family of DEC-compatible semi add-ins. Circle the reader service number below or, better yet, call us today at 609-799-0071, and we'll give you a close-up look at the products that have made us the leader.

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LSI-11	DR-215S	dual	256 KB
LSI-11	DR-113S	quad	256 KB
LSI-11	DR-213S	quad	1.0 MB
PDP®-11	DR-114S	hex	256 KB
PDP-11	DR-114SP	hex	256 KB
PDP-11	DR-214SP	hex	1.0 MB
PDP-11	DR-144S	hex	256 KB
PDP-11	DR-244S	hex	4.0 MB
VAX®-11/750 PDP-11/70	DR-175S	hex	256 KB
VAX-11/780	DR-178S	extended hex	512 KB
DECSYSTEM 2020®	DR-120S	extended hex	512 KB
PDP-8/A	DR-118S	quint	128 K x 12

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Dataram also provides core add-ins, core and semiconductor add-ons, memory system units, memory management, and a wide range of memory-related accessories for DEC users.

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News Update

ment of an Ada compiler for Zilog's 16-bit μPs: the Z8001 (segmented memory addressing version), Z8002 (non-segmented version), and Z8003 (segmented version supporting virtual memory). The System 8000 will be used as the host computer system for developing the compiler, which will be submitted to the Department of Defense for certification.

Beckman Merges With SmithKline

Beckman Instruments and SmithKline Corp. have approved a definitive merger agreement providing for Beckman to become a wholly-owned subsidiary of the new company named SmithKline Beckman Corp. The agreement requires approval by shareholders of both companies. The companies have scheduled special shareholder meetings on March 4 for SmithKline in Philadelphia, and Beckman in Fullerton, CA.

Fujitsu Slashes Prices Of Bubble Memories

Brisk worldwide sales of bubble memory cassettes and devices have enabled Fujitsu to reduce prices on 256K bit memories by 20%, according to Fred Bihler, senior vice president of Fujitsu's Component Div.

"We are able to make these price reductions because bubble memory sales have reached our forecasts. Although other manufacturers dropped out of this field, we believe that there is an even stronger demand to come," he said, adding "we foresee more price reductions in the near future as the market continues to grow". Currently volume applications include data logging, portable terminals, point of sale terminals, personal computers, machine tool controls and electric typewriters.

Scientific Calculations Introduces Microelectronic Design System

Scientific Calculations has announced the MicroElectronics Design System, a product targeted at both MOS and Bipolar markets that, according to the company, enhances productivity for all design approaches including hand-crafted, cell-based, and gate array. The system is a turnkey product which is intended to be used for all phases of the implementation of an IC from the completion of logic definition, through generation of data tapes for photomask production. It supports, as an integral part of the system, automatic placement and routing, structured design, auto-interactive editing, and central data management via a data base management system. The system includes a new graphics-editing capability which includes dynamic pan and zoom features coupled with Multi-Viewport color graphics presentation.

TI Sales Up But Income Down

Texas Instruments has reported that its net sales billed for the year 1981 were $4206 million, an increase of 3% over 1980. Net income was $108.5 million, down 49% from 1980. Earnings per share were $4.62, compared with $9.22 in 1980. Income before provision for taxes as a percentage of net sales billed was 4.2% in 1981, compared with 9.3% in 1980. TI Chairman Mark Shepherd, Jr., and President J. Fred Bucy said in the report:

The principal reasons for the decline were adverse results in semiconductors and distributed computing, along with the effect of weaker international currencies. Pretax earnings also reflect costs of $36.6 million associated with the product phaseouts and employment reductions announced in the second quarter of 1981.

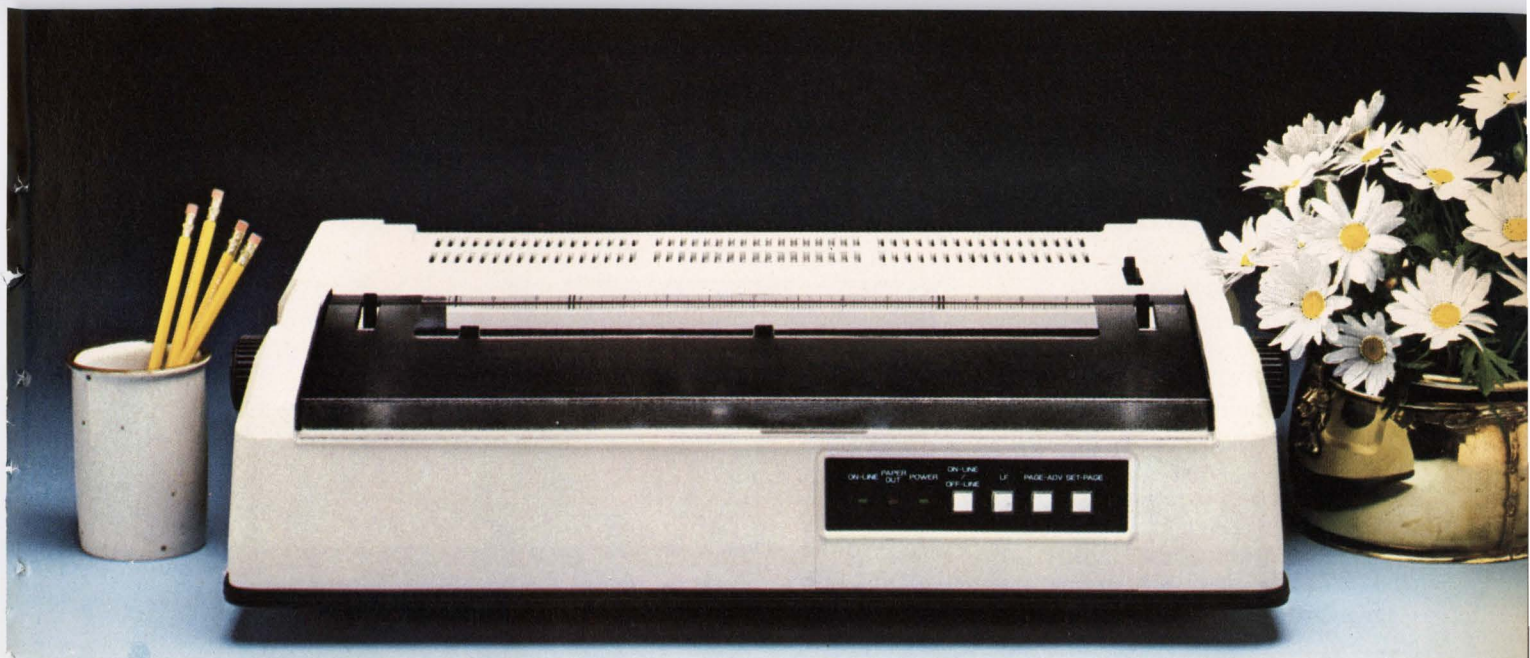
UCSD p-System To Be Available On IBM Personal Computer

SofTech Microsystems has announced that IBM has joined a long list of major hardware manufacturers, including Texas Instruments, Ohio Scientific, Zenith, Philips, and Commodore, who have chosen to distribute the UCSD p-System, an operating system which provides advanced software development facilities as well as high-performance execution options.

Orcatech Launches US Operation

Orcatech, a Canadian-based manufacturer of computer graphic systems for the design engineering marketplace, has opened a sales and service office in the United States. Located at Ocean Park Blvd. in Santa Monica, CA, the new facility will establish a sales and service network in the American market as well as a support organization for those companies who have purchased the Orcatech Graphic Computer System.

According to Orcatech's President, David Pearson: "California was chosen because of proximity to the aerospace, semiconductor and computer graphics industries. Many of our major customers are located there, and if you want to compete effectively in this new and growing field, where better to be than right on the doorsteps of your competitors".



C. Itoh's new *F-10 Printmaster* Daisywheel printer is the compact beauty you can easily get attached to. Just look at what you get:

1. Small footprint, low-profile design (only 6" high) fits easily into your system.
2. Downloading wheel and impact sequences allow use of a variety of unique wheels and permit OEM's to tune the printer to specific needs.
3. Comes in two Shannon-text-rated speeds. 40 CPS and 55 CPS.
4. Industry-standard parallel or RS 232-C interfaces and ETX/ACK, XON/XOFF protocols provide maximum OEM flexibility and installation ease.
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7. Field proven, firmware intensive technology for increased reliability.
8. Cast aluminum base plate with high quality metal parts provide lasting dependability.
9. Low-noise operation is ideal for office environment.
10. Choice of friction feed or bidirectional tractor feed for precise print positioning of tabular and graphics data.
11. Uses industry-standard wheels and ribbon cartridges available from multiple sources at low prices.
12. Universal power supply is standard and allows worldwide power source compatibility.
13. FCC approved and under 50 lbs. in weight for fast shipments and sales.
14. Easy-to-load wheels with tested and proven method of wheel support (spring loaded with positive detent).

We could go on. But quite frankly, once you see Printmaster perform, you'll never look at another Daisy.

Printmaster is fully backed by C. Itoh's warranty and complete support organization. Contact C. Itoh Electronics, Inc. 5301 Beethoven St., Los Angeles, CA 90066 (213) 306-6700.

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Silicone Shields Chips From Alpha Radiation

Soft error mechanisms in integrated circuit memories caused by alpha-particle radiation were first reported in 1978.

The particles are emitted by uranium and thorium decay sequence radioactive isotopes present as trace materials used in packages for the circuit. Although the amount of these radioactive elements is only in part per million range, the activity is high enough to affect memory cells. There are three conceivable ways to alleviate this problem:
(1) Reduce the activity level of the packaging materials (2) Redesign the circuit to reduce device sensitivity, or (3) Shield the chip surface with a material that will stop the alpha particles.

One company, Western Electric, Allentown, shields static RAMs from alpha-particle radiation with a 2-mil coating of Dow Corning 3-6550 silicone dispersant.

Tests conducted by Bell Labs, Allentown, confirmed that the silicone material met the basic requirements for shielding the static RAM circuits from alpha radiation. These include: No adverse effect on circuit reliability, low alpha activity and compatibility with packaging materials and processes.

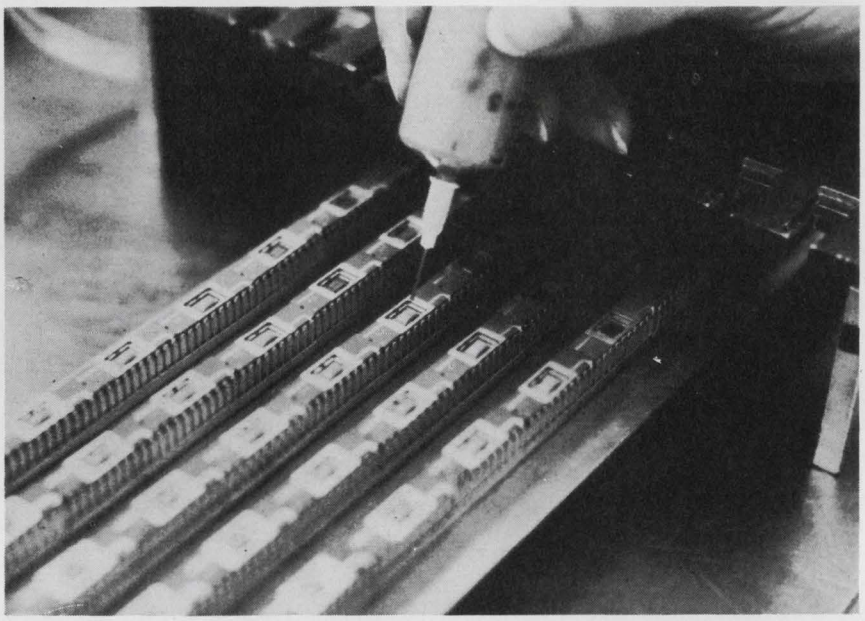

Figure 1: A syringe is used to apply liquid silicone RTV to shield static RAMs from alpha radiation.

The Dow-Corning 3-6550 dispersion coating is applied to the memory chips in the last step before hermetic sealing. It is applied manually using a time controlled, pneumatically activated syringe. The syringe holds 30 cc of liquid silicone RTV, enough to coat 2400 static 4K RAMs.

Prior to coating, the devices are cleaned by degreasing in fluorocarbon solvent vapor and liquid. Coated chips are placed in air for two hours to initiate cure and to permit the solvent to escape. The coating is then fully cured in a batch oven for six to eight hours at 120°C and 35% relative humidity.

Florida Hosts Southcon/82

Southcon/82, Florida's first major high-technology electronics exhibition and convention, will be held in Orlando on March 22-25. It will attract over 10,000 electronics professionals from the Southeast and elsewhere.

Featured will be products and systems of over 250 regional and national manufacturers, reps and distributors in 470 exhibit booths at the Sheraton Twin Towers and Hyatt Orlando hotels. A 20-session Professional Program at the Holiday Inn on International Dr. will detail electronics in the Southeast.

Southcon/82 will also feature five special-fee workshops at the Holiday Inn.

Frequent complimentary shuttle buses will link all Southcon/82 locations and connect with the simultaneous IEEE Computer Society's Tutorial Week East/82 held at the Orlando Marriott Hotel, close to the Professional Program's site at the Holiday Inn.

Southcon/82 will also operate bus service to the meeting from Cocoa Beach (Cape Canaveral), Melbourne and Tampa/St. Petersburg/ Clearwater each day.

The evening of opening day will be devoted to a two-hour informal get-together for attending professionals. The All-Industry Reception will include refreshments and entertainment.

The rapidly expanding base of high-technology in the Southeast has dictated the direction of Southcon's Professional Program — designed to explore leading-edge developments in the traditional and emerging disciplines of the region.

The area's predominance in space and space flight technology will be reflected in the sessions. But there will be plenty of attention devoted to data communications, micros, navigation, logic array and the μP.

The 20 two-hour sessions, at the Holiday Inn on International Drive, will be presented in three time blocks daily, starting at 9:30

a.m., 1 p.m. and 4 p.m. Topics will include explorations of industrial robotics, control applications on microcomputers, VLSI advances in digital signal processing, image processing, speech recognition and synthesis, developments in EHF SATCOM fiber-optic data links, fiber-optic communication systems, developments in programmable logic, gate array approaches of circuit design, local networking developments and data communication integrated circuits.

The numbers of exhibitors and their featured products at Southcon/82 reflects the diversity and scope of the Southeastern electronics industry, not only in the quality and range of manufacturing but in the size and varying fields of endeavor.

More than 250 exhibitors including United Technologies, Gould and Texas Instruments will occupy 470 exhibit booths at the Sheraton Twin Towers and Hyatt Orlando hotels. In each location the exhibit areas will be approximately the same size and similarly divided into four product categories. The categories are: mini- and micro-computers, EDP peripherals and data communications; instrumentation, control systems and test equipment; components, microelectronics and fiber-optics; production and packaging equipment.

Foundry Size Grows

During 1981, the custom IC business saw the emergence of the Silicon Foundry. Small and large IC producers joined the custom circuit parade to offer any company the option of designing its own IC and having these produced in a silicon foundry.

Foundries, custom ICs and gate arrays are not new concepts — all were born in previous recessions. Bad times for IC makers create excess capacity. Putting that excess capacity to work is very important to semi manufacturers. As the economy improves, the excess capacity disappears as standard product production increases. Good-by excess capacity, good-by custom production.

A new sign of hope developed during the past year: a large number of start-up companies were formed to do design or production of custom and gate array devices. Hopefully, these companies will be on hand after the recovery predicted this year.

National Semiconductor seems to be one of the large producers interested in future custom/foundry

THE
ZENDEX ZX-907
BUS TRACER
Monitors Multibus* Operation

The ZX-907 represents a major advancement in Multibus development tools. This processor-based board, in conjunction with an external CRT, interprets Multibus events by monitoring address, data and control lines. The on-board memory will store up to 1024 bus events. The interpreted results are displayed on the CRT in the form of action, memory or I/O location, and data.

- 40 bit wide trace
- 1024 Bus Cycle Storage in on-board RAM
- On-board 8085A-2 Processor
- Menu driven software trace control
- Breakpoint can be preset on Address = , <, >
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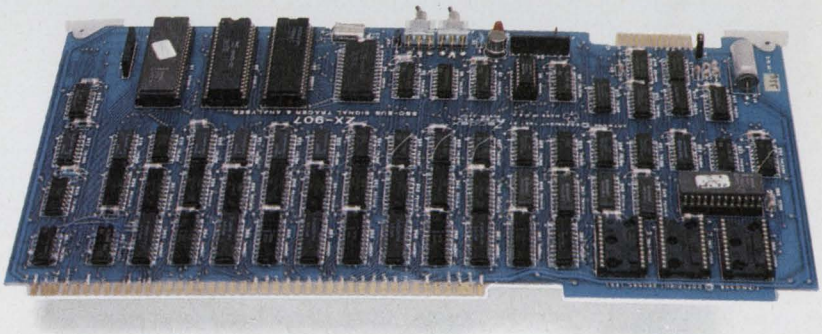

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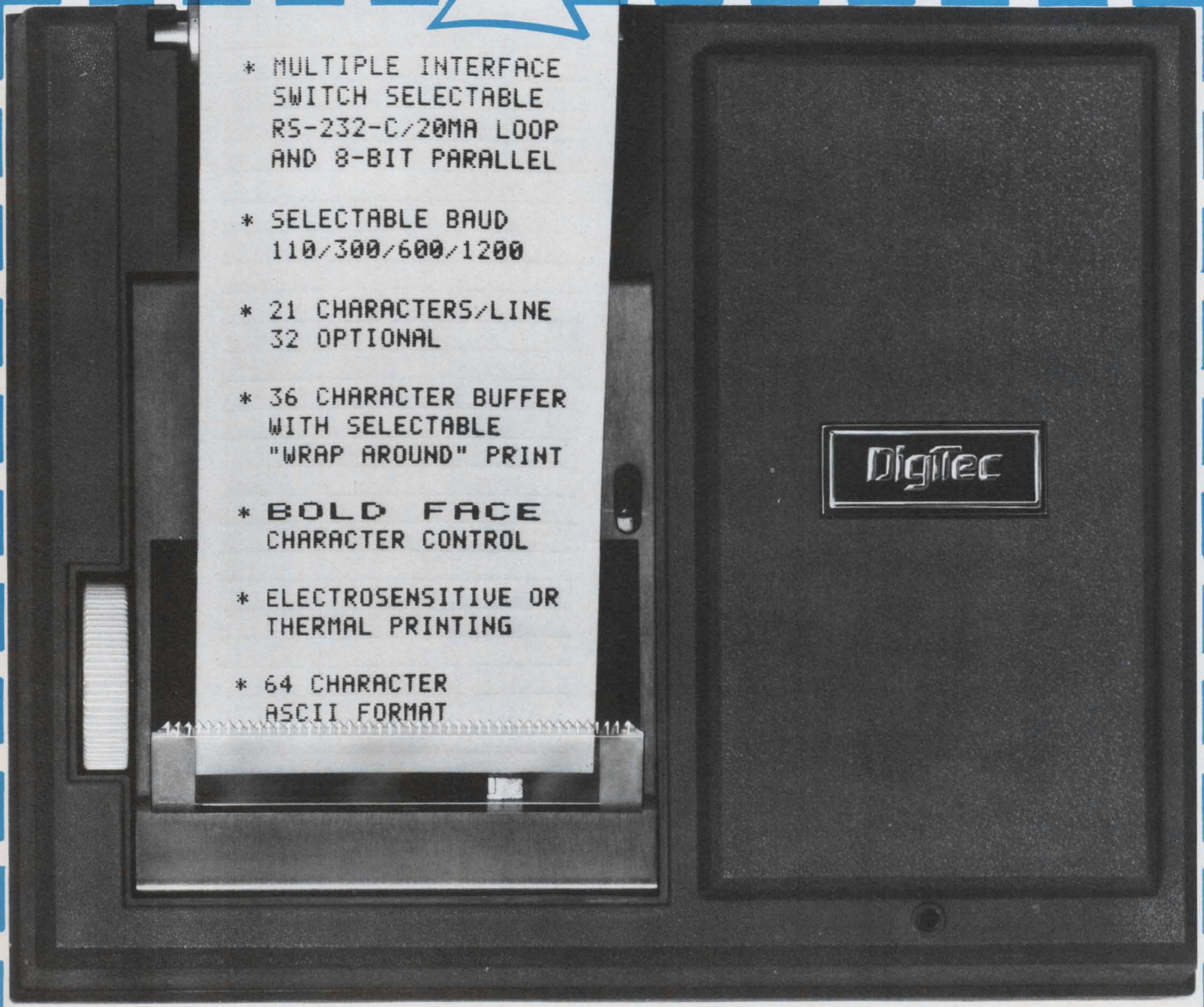

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business. In December, they opened a 5″ ROM and Custom/Foundry wafer fabrication line that they claim will increase National's total NMOS ROM and foundry capacity by 150%. That means a total capacity of 20,000 wafer starts every four weeks or 10,000,000 ROM or custom circuits manufactured every four weeks. That's a lot of chips, and NSC claims that they will accept custom orders for as little as $50,000 using custom tooling.

National's new $8 million automated wafer fab line includes computer control of all fabrication processes, μP-controlled furnaces, laser-controlled auto-align printers and automactic inspection. NCS's investment is based on a custom market that they claim has exceeded $300 million and will to $1billion by 1985. That's a compounded growth rate of 32%.

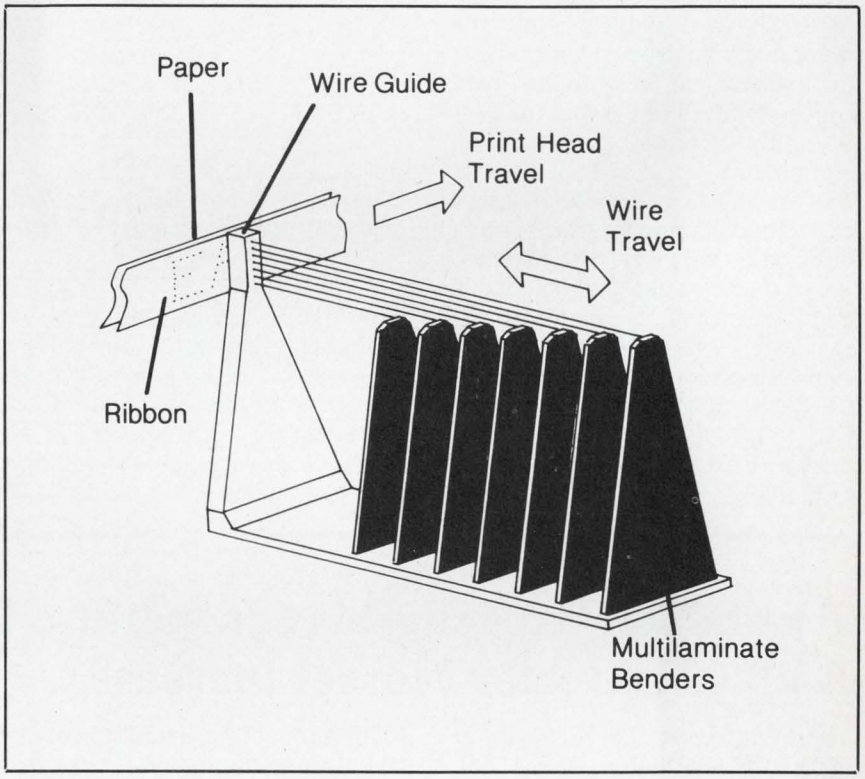
With the silicon foundry concept, the customer or circuit user owns the tooling (data base tapes, design, photomasks etc.), while the IC manufacturer supplies wafer, die, or packaged parts. The IC user retains his proprietary design. This gives the user many design and production options. Should capacity become a problem the user can move his tooling to a producer with excess capacity.

In the case of National's new foundry, users will be able to run advanced geometry designs; 3μ design rules are now available compared to 5μ offered by much of the industry. National expects to advance to 2μ design rules in the very near future.

Perhaps as this recession fades, the custom and foundry business will stay bright. For some users the custom design approach is critical to producing the end product. Hopefully, National and all of the other foundries will be around for a long time. If not, there may be more in-house production start-up at the major equipment manufacturers. Foundries have a definite place in the business. A lot of IC users have invested in tooling. It will be very interesting to watch the future of the foundry. —*Groves*

Piezoelectric Print Head

Dot matrix printers provide moderate print quality by repetitively launching dot-producing wires against an inked ribbon as the print head travels across the page. Usually, a vertical row of seven wires is used. These wires can be launched up to 1000 times each second and create close to 200 characters per second if the character width is five dots.



Piezoelectric print heads run cooler and quieter than standard print heads. They also provide higher quality, according to Pieco Electric Products (Cambridge, MA), because the print wires are held, rather than hammered, against the ribbon (standard ballistic print wires can also be used with piezoelectric drivers).

The main problem with conventional heads is that solenoid wire drivers generate a lot of heat. This limits the launch rate and the number of solenoids that can be packed into available space. Designers pushing these limits often end up with reliability problems.

Recently developed printer heads from Piezo Electric Products, Inc. (Cambridge, MA), using piezoelectric drivers don't have this problem. Seven piezoelectric drivers generate less than one watt of heat in the head and can continuously operate at over 200 characters per second while remaining at room temperature.

The cool operation and low cost of piezoelectrics mean that more drivers can be put in the printer. Extra drivers can be used to improve either print quality or printing speed. Piezoelectric drivers are also quieter then solenoids.

Piezoelectric drivers are multilaminate benders specifically designed for the job. Unlike solenoid drivers, which usually strike the wires and bounce them off the ribbon, the benders are attached to the wires and push them against the ribbon. This permits control of the time the wire holds the ribbon against the paper. Longer times improve print because more ink soaks into the paper.

EDP User Expenditures To Double Over Next Five Years

During the past seven years or so, EDP user expenditures on data communications, including both line charges and equipment, has increased 22% annually on average. According to a new market study, that growth rate will be maintained throughout most of the decade, with user budgets at $6.4 billion in 1981 to approximately double in size to $12.5 billion by 1985.

Data communications will account for an increasing proportion of EDP user budgets while the market will be driven by increasing deployment of distributed data processing techniques and the proliferation of remote data terminal equipment.

The analysis of service offerings and their economics turns up a dazzling variety of choices. Beyond the traditional telephone companies and Western Union, there are eleven new common carriers, along with two more satellite-based carriers already approved by the FCC, and scheduled to be operational before the mid-1980s.

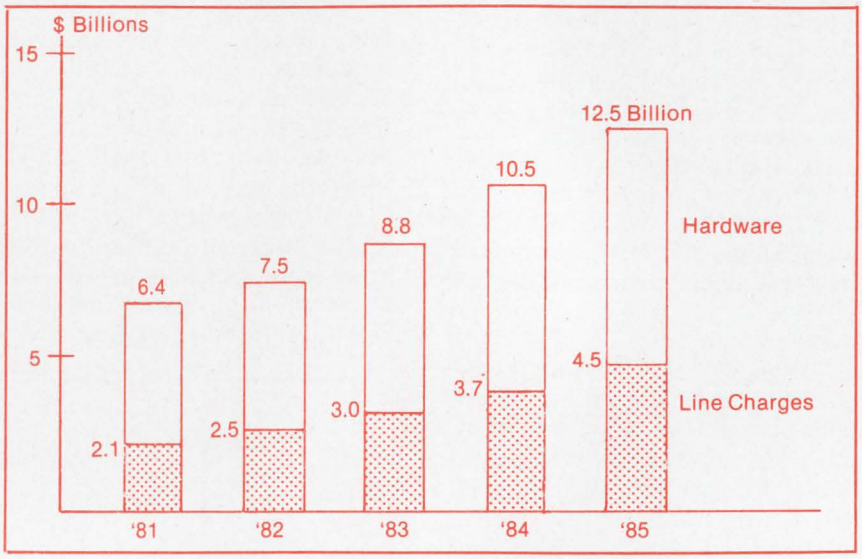


Figure 1: Data communications markets, based upon EDP user budgets (source: Frost & Sullivan, Inc.).

All such services will gain importance in the future. In addition, Videotext/Teletext developments will have an unpredictable impact.

Hardware expenditures associated with such services will also rise by as much as three times over the next five years. A similar gain will occur for local on-site networks as well as a substantial increase for network switching node controllers. For further info, contact Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038.

Production Capacity May Jeopardize Billion Dollar Converter Market Increase

The unprecedented growth in market demand for ADCs and DACs could well be thwarted by the industry's failure to sufficiently expand production capacity. In a new market study on the converter industry, Venture Development Corporation (Wellesley, MA) estimates that the market for ADCs and DACs will grow 33.9% per year over the 1981 to 1986 period.

Parts shortages could be particularly severe in certain high growth monolithic and hybrid product segments. While the demand for hybrid ADCs will expand at a 35% per year annual rate, monolithic converter markets will be even more dynamic. Consumption of monolithic DACs will rise at a 39% annual rate, exceeded only by the astounding 46% per year growth in monolithic ADCs.

Maurice Klapfish, Manager of VDC's Instrumentation Division, observed that the expected fourfold increase in data converter consumption over the next five years cannot be achieved by the mere addition of people and machinery. Massive expansions of factory floor space will also be necessary.

Despite a number of facility expansion programs currently under construction, product shortfalls may still occur. The rapid market growth in conjunction with the several years required to plan and implement a new facility require that subsequent facilities must be planned for, even before present projects come on-line.

Attention to facilities management will be especially critical in the monolithic converter segment where the 1986 demand will be six times larger than at present.

The failure of the data conversion component industry to adequately expand production capacity to meet the rapidly growing demand could permanently alter the future course of the business. Most certainly, major production shortfalls will trigger a surge of new supplier start-ups, as occurred in the early 1970s. Once attracted to the data converter business, the awesome resources of the world's leading semiconductor manufacturers could dwarf the efforts of the present industry leaders.

Increased captive production is another likely consequence of restricted parts availability. Stretched out lead times and unreliable deliveries would force equipment manufacturers to devise in-house solutions to μP interfacing problems. Should this occur, the traditional converter manufacturers might find it impossible to recapture lost business.

Mr. Klapfish further added that the escalating demand for ADCs and DACs is well documented and quite independent of converter availability. Equipment designers concur that the inherent need for analog μP interfacing will be satisfied either through open market purchases, or by in-house fabrication using more elemental circuit functions. For more info: Venture Development Corp, One Washington St, Wellesley, MA.

Disk Drive Market Prospects Dimmed By Optical Disk

The Winchester disk drive market will be threatened as early as 1984 by the optical disk, according to a report released by International Resource Development Inc. Although the rigid disk drive market is now experiencing very strong growth, particularly at the very low and very high ends, these Winchester market segments will be subject to heavy competitive inroads by optical disk-based peripheral storage systems during the second half of this decade. The spectacular price/performance advantages offered by optical disk-based systems will allow them to take command of two-thirds of the 1992 market for business system disk peripheral sales in the U.S.

The key attractions of optical disk storage technologies center upon low cost, extremely high storage capacities and compactness, according to the report. A 12″ optical disk can store 2G bytes of information, based on existing technology. Evaluation disks are already available from a small California firm called Drexler Technology at a cost of $3,000 to $4,000 per disk but Drexler is prepared to price initial quantities of production-run disks at $100, and prices of $10 per disk are foreseen when production is in full scale by 1984.

The potential for storage of 1M byte of information at such low costs poses a serious threat to familiar forms of disk storage. For example, Winchester and floppy disk prices are $12 and $7.50 per Mbyte respectively. Even if recent trends in price declines for these technologies continue through 1984, they will still remain above optical disks' projected levels.

As with most radical developments, the advent of the optical disk has been met with some caution and, the report counsels, further technical refinements are needed. At the same time, significant advances have been made in the area of lasers which are crucial to the recording and reading of data on the disks. Companies such as Hitachi and RCA have assumed leadership positions in the development of semiconductor diode lasers. Similarly, work on alternative media types is progressing, e.g., thin metal films like tellurium and its alloys (Philips, RCA), dye polymer films (Kodak), electrophotographic (Harris) and metal-impregnated (Drexler), such that archival storage lives and recording densities can be further improved.

Two frequently cited impediments to optical disk storage — lack of erasability, and relatively high error rates for data storage — are regarded as temporary drawbacks by the IRD researchers. The vast quantities of storage space offered by these disks will permit data to be rewritten or new data to be added, thus sidestepping these problems. These characteristics will also have little adverse effect on application areas such as image and video storage which are expected to grow dramatically during the latter half of the decade. Further details are available from IRD at 30 High St., Norwalk, CT 06851.

TYPE OF MEDIA	QUANTITY NEEDED	COST OF MEDIA
Magnetic Disk	80 200MB Disk Packs	$40,000
Computer Compatible Tape	90 Tapes (2,400 ′, 6250bpi, 8-track)	1,350
High Density Magnetic Tape	2,400 ′ of 2″ Tape	100
Optical Disk	One 12″ Disk	10*
*Projected		

Figure 1: Quantities required for storing 10^{11} bits of information in alternative storage media (source: International Resource Development, Inc.).

Thick Films From PR

The DuPont Company has announced plans to construct a new facility to produce thick film electronic materials at Manati, Puerto Rico. The plant, which is expected to be completed during the summer of 1983, will be owned and operated by a new wholly owned subsidiary, DuPont Electronic Materials. The project includes construction of a 39,000-square-foot manufacturing and warehouse building and installation of state-of-the-art production and quality control equipment at a nine-acre site adjacent to DuPont's Caribe Biochemicals facility.

Agency Aids Import-Damaged Manufacturers

If your company has been hurt financially or technically by foreign competitors, there is a U.S. Department of Commerce program that can provide some help. Under this program, authorized by the Trade Act of 1974, an American manufacturer damaged by the import influxes can obtain technical assistance in areas such as marketing, engineering and production to help make it competitive again.

Import-damaged manufacturers can also obtain financial assistance of up to $1 million in direct government loans. An additional $3 million in government guaranteed loans can be provided for working capital, fixed assets or other company needs in many cases. Companies with sales in the $1 million to $50 million-range, with 25 to 300 employees are favored under the program; however, smaller and larger firms may qualify for some aid.

Two types of assistance are available. One is "technical assistance", for which the government pays up to 75% of the cost of helping business solve technical, marketing and financial problems. A second type is "financial assistance", for which the program provides loan guarantees or direct loans for new capital equipment and facilities. Very favorable interest rates can be obtained in many cases with the loan guarantees — in some cases 25-year loans are available.

Outside consultants' fees can be paid under the Trade Assistance program for technical advice. In the western states, for example, the Trade Assistance program is administered under a grant to the University of Southern California. USC is able to provide a wide range of technical, financial, and marketing consulting services.

Eleven Trade Adjustment Assistance Centers (TAAC) were established to serve the 50 States, Puerto Rico and the Virgin Islands. Information is available from the regional TAAC or from the Office of Trade Adjustment Assistance, International Trade Administration, U.S. Department of Commerce, Washington, DC 20230. Tel: (202) 377-5005.

A similar U.S. Department of Labor program is available to provide benefits to workers who have been laid off or put on part-time employment because of imports. Information on this separately administered program is available from the U.S. Department of Labor, Office Trade Adjustment Assistance, Washington, DC 20213. Tel: (202) 376-6896.

— Groves

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The full standard ASCII 96 character set, with descenders and underlining of all upper and lower case letters, is printed bi-directionally, with up to 5 crisp copies, at speeds up to 200 CPS. Models DP-9500 and DP-9501 offer 132/158/176 and 132/165/198/220 columns respectively. Print densities are switch- or data-source selectable from 10 to 16.7 characters/inch. All characters can be printed double-width under communications command.

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Standard in all models are the three ASCII compatible interfaces (Parallel, RS-232-C, and Current Loop). Also standard is a sophisticated communications interface to control Vertical Spacing, Form Length and Width, Skip-Over Perforation, Auto Line Feed, X-On/Off, and full point-to-point communications.

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Beyond the built-in performance of the grafixPLUS series printers, the engineered-in quality and support are equally important. The result? Approval of both UL and FCC, Class A; operating noise levels under 65dbA; and a nationwide service organization second to none.

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A Precise Real Time Clock

As μCs are being used more frequently in data analysis and in control applications, it is becoming increasingly important for the computer to know the actual time an event took place. To do this, the computer must have access to a real time clock — an internal or external device that keeps track of the time in hours, minutes, seconds, etc. This article describes the construction and interfacing of an accurate, remote real time clock with a μC system that required an accuracy of a hundredth of a second.

A Simple Clock

A very simple real time clock can be constructed which uses the line voltage to supply a short pulse which interrupts the μP. Most μPs have one or more pins that can interrupt the processor which can then go to an area of memory that services the interrupt. The program residing there would cause memory locations to be updated. The time is then determined by examining those memory locations and decoding the values (it is also possible to decode the information at interrupt before storing in the memory locations, but that uses much more processor time). Such a clock can measure to the nearest tenth of a second with an accuracy dependent on AC power frequency. This type of clock is quite adequate for most applications but not when a precise time (or time interval) is required that is relatively short (few seconds) or when the power system is unreliable.

More Precise Versions

A real time clock which is more precise can be built along two lines. One is to continue with an interrupt system but use a quartz oscillator to generate the interrupt signals. To obtain high precision (small time intervals), a larger and larger percentage of the processor's time is devoted to time measurement as the frequency of interruptions increases. To avoid wasting valuable processor time, a non-interrupt, real time clock was designed and interfaced. This device can keep track of the time and inform the computer only when requested. A non-interrupt clock once required external memory to keep track of the time. However, with the new LSI clock chips available, one cannot only construct a very precise clock but also do it very easily. The design presented below satisfies three requirements: 0.01 second resolution, ease of interfacing to the μC through 8 bit parallel ports and high accuracy.

Number	Segments lit abcdefg	Condensed code abefg	Decimal	Hex (converted)
0	xxxxxx	11110	30	F0
1	xx	01000	8	40
2	xx xx x	11101	29	E8
3	xxxx x	11001	25	C8
4	xx xx	01011	11	58
5	x xx xx	10011	19	98
6	x xxxxx	10111	23	B8
7	xxx	11000	24	C0
8	xxxxxxx	11111	31	F8
9	xxxx xx	11011	27	D8

Table 1: Numbers, their seven segment LED code, and the five segments ("condensed code") needed to uniquely determine them; the decimal equivalent of this latter, condensed code also appears. The decimal equivalent must be multiplied by 8 (2^3) and converted to hex for comparing to the information coming to the computer from the clock (see Figure 2). This converted hex code appears last. See Figure 1 for segment labeling.

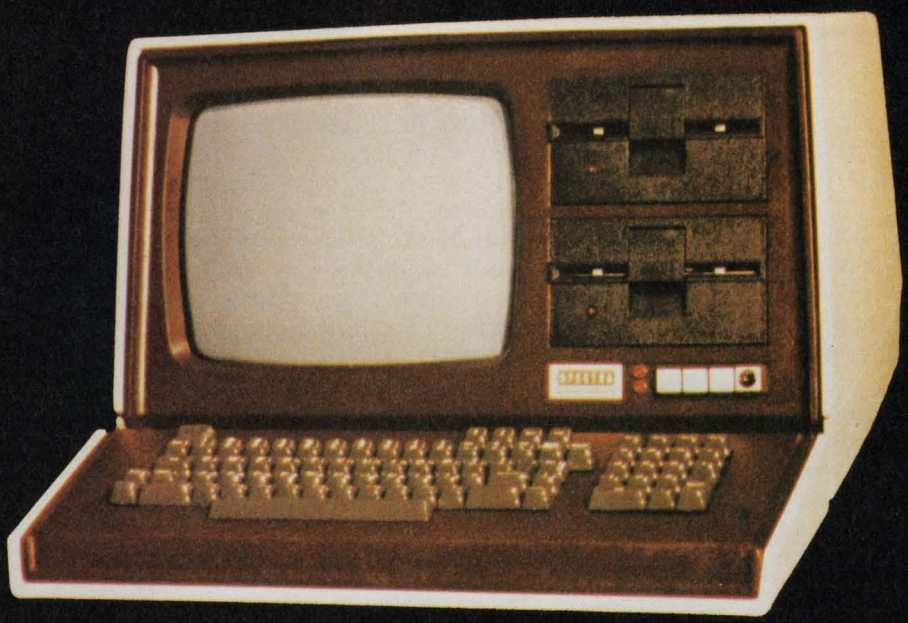
Inputs								Outputs		
1 H	2 10M	3 M	4 10S	5 S	6 S/10	7 S/100	8 10H	C	B	A
							0	1	1	1
						0	1	0	0	0
					0	1	1	0	0	1
				0	1	1	1	0	1	0
			0	1	1	1	1	0	1	1
		0	1	1	1	1	1	1	0	0
	0	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	0

Table 2: Logic for a 1 of 8 priority encoder (74147). A low (0) to one of eight inputs (each corresponding to a digit in the "display") can be encoded to 3 bits on the output. Blanks in the input indicate either a high (1) or low may exist.

Clock Design

An Intersil 7045 was chosen since it afforded convenient interfacing

THE SPECTRA ADVANTAGE



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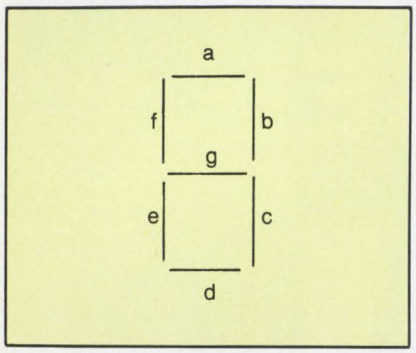

Figure 1: A seven segment LED digit and the normal labeling of the segments.

with several attractive options. This chip was built for stopwatch applications yet would accurately keep track of the time through 24 hours with a resolution of 0.01 seconds. It stores the time internally as hours, minutes, seconds and hundredths of a second. A very attractive feature was the "split" mode which allowed the output from the chip (the display) to freeze while the clock continued to measure the time. Thus one could read the digits without affecting the timing accuracy.

The CMOS clock chip can run on 5V and does not require a special power supply. The chip needs two input lines: one for reset and another for start/stop (this for the "display" in the split mode). The output of the chip is designed to go to a multiplexed seven segment, eight digit common cathode LED display. This means fifteen lines are needed to see the time on a display. However, many of these lines carry redundant information and it was possible to reduce the number of output lines to eight without losing any information. The eight output lines from the clock chip and the two input lines to the chip can share the same 8 bit parallel port, but, for simplicity and because two lines were free in another 8 bit port, this design uses two lines from one 8 bit port as input and eight lines from another as output from the chip.

A multiplexed display requires a high to each of the appropriate segments and a low to the cathode of that digit so that the segments light in the digit correctly (see **Figure 1** for segment code). Each digit is lit individually, but this occurs so fast that the eye would see all eight digits of the display lit at once. The width of each pulse to the display from the clock chip is about 0.1ms. The digits are lit in the following order: .01 sec, 10 hr, 1 sec, 10 min, 10 sec, 1 min, .1 sec, and 1 hr. All eight digits can thus be read in .8ms, which is much less than the clock's 10ms resolution.

The code for a seven segment display appears in **Table 1;** only five (a,b,e,f and g) of the seven segments are needed to uniquely specify the number. Since each digit is lit sequentially, the digit corresponding to the segments is determined by sensing which digit line is low. For example, when the time is 16:22:40.53 (hours: minutes: seconds), then, when the ten second digit would go low, the segments b,(c),f and g would go high to give a display of 4.

Instead of looking at each of the eight digit lines to see which is low, one can use a priority encoder (74147) to give a three bit output (2^3) indicating to which of the eight digit lines is low **(Table 2).** Thus, the seven segment lines have been reduced to five and the eight digit lines have been reduced to three resulting in one byte (for 8 bit processors) that contains the value of a particular digit. Eight bytes are required to fully specify the time.

Address Data	Assembled Code	Address Data	Assembled Code
BE00 08	PHP	BE51 2907	AND #$07
BE01 A207	LCX #$07	BE53 CDF6BF	CMP $BFF6
BE03 A900	LDA #$00	BE56 F0F6	BEQ $BE4E
BE05 9DF7BF	STA $BFF7,X	BE58 60	RTS
BE08 CA	DEX	BE59 A000	LDY #$00
BE09 D0FA	BNE $BE05	BE5B ADF5BF	LDA $BFF5
BE0B AD0EC7	LDA $C70E	BE5E 29F8	AND #$F8
BE0E 2907	AND #$07	BE60 C9F0	CMP #$F0
BE10 D0F9	BNE $BE0B	BE62 F029	BEQ $BE8D
BE12 A20A	LDX #$0A		
BE14 204ABE	JSR $BE4A	BE64 C8	INY
BE17 AD0EC7	LDA $C70E	BE65 C940	CMP #$40
BE1A 8DF5BF	STA $BFF5	BE67 F024	BEQ $BE8D
BE1D 2907	AND #$07	BE69 C8	INY
BE1F D0EA	BNE $BE0B	BE6A C9E8	CMP #$E8
BE21 ADF5BF	LDA $BFF5	BE6C F01F	BEQ $BE8D
BE24 A200	LDX #$00	BE6E C8	INY
BE26 2059BE	JSR $BE59	BE6F C9C8	CMP #$C8
BE29 8EF6BF	STX $BFF6	BE71 F01A	BEQ $BE8D
BE2C 204EBE	JSR $BE4E	BE73 C8	INY
BE2F A20A	LDX #$0A	BE74 C958	CMP #$58
BE31 204ABE	JSR $BE4A	BE76 F015	BEQ $BE8D
BE34 AD0EC7	LDA $C70E	BE78 C8	INY
		BE79 C998	CMP #$98
BE37 8DF5BF	STA $BFF5	BE7B F010	BEQ $BE8D
BE3A 2907	AND #$07	BE7D C8	INY
BE3C AA	TAX	BE7E C9B8	CMP #$B8
BE3D 8DF6BF	STA $BFF6	BE80 F00B	BEQ $BE8D
BE40 2059BE	JSR $BE59	BE82 C8	INY
BE43 8A	TXA	BE83 C9C0	CMP #$C0
BE44 2907	AND #$07	BE85 F006	BEQ $BE8D
BE46 D0E4	BNE $BE2C	BE87 C8	INY
BE48 28	PLP	BE88 C9F8	CMP #$F8
BE49 60	RTS		
BE4A CA	DEX	BE8A F001	BEQ $BE8D
BE4B D0FD	BNE $BE4A	BE8C C8	INY
BE4D 60	RTS	BE8D 98	TYA
BE4E AD0EC7	LDA $C70E	BE8E 9DF7BF	STA $BFF7,X
		BE91 60	RTS

Table 3: Machine Language subroutine to read and decode the data from the real clock. A Flow Chart is shown in Figure 3. All values are hexidecimal and are for the 6502 microprocessor. The # symbol refers to an immediate command and the $ symbol preceeds a number in hexidecimal. The starting address is BE00.

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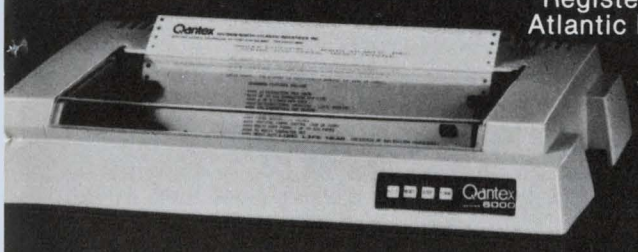

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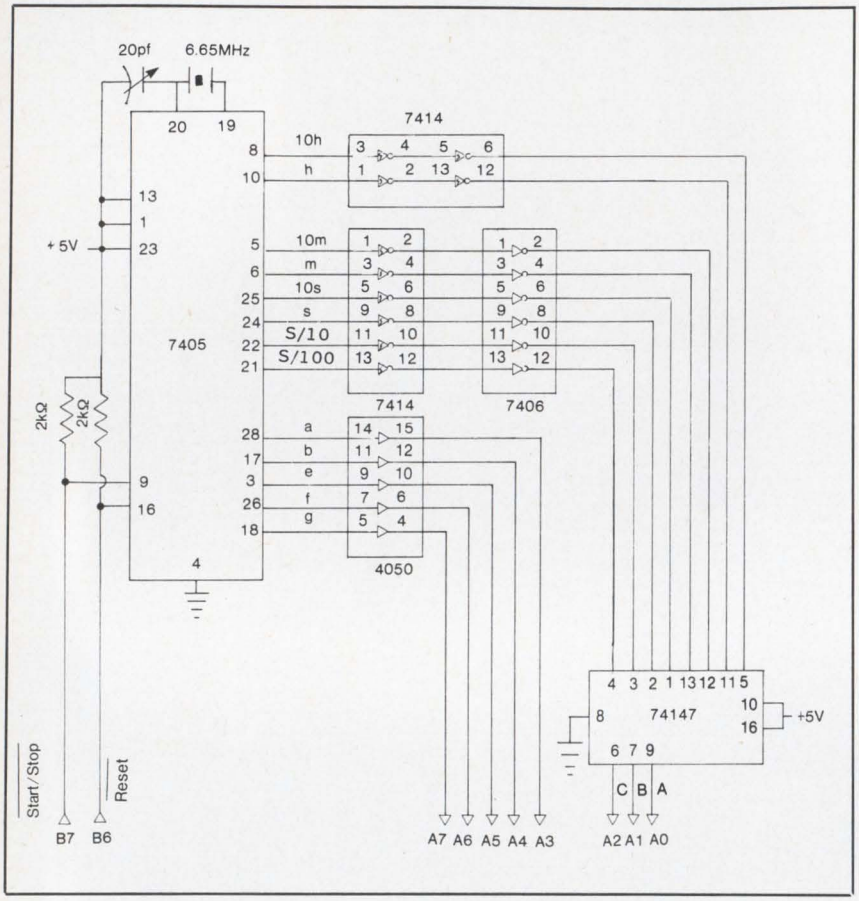

Figure 2: Electrical schematic for a non-interrupt, remote, real time clock. An Intersil ICM7045IPI stopwatch clock chip is used allowing eight digit accuracy: .01 sec (S/100) to 10 hr (10 HR) in a 24 hour format. Schmidt triggers (7414) and a 4050 are used to bring the 7405 signals to TTL levels. The priority encoder (74147) determines which digit (s, 10s, etc.) corresponds to the segment data presented to the computer. By reading eight consecutive values, the time is determined.

The remaining chips bring the logic pulses from the clock chip to TTL levels. The 7405 does not provide sufficiently distinct output voltage levels to drive the 74147. A Schmidt trigger (7414) performs this task but inverts the signal in the process. An inverter (7406) follows the 7414 and provides the correct logic levels for the 74147. The 4050 is a CMOS to TTL driver. The complete schematic is shown in **Figure 2.** the 20 pF variable capacitor connected to the crystal can be varied to provide accurate time. An accurate frequency meter can be connected to one of the outputs of the 7414 (i.e. pin 2) and the capacitor varied for a period of 1.25 msec; this will provide an accuracy of 1 second/week.

```
1     REM THIS IS MICROSOFT BASIC ON OHIO SCIENTIFIC C4PMF
100   POKE 8955,0: POKE 8956, 190: POKE 8960, 189: REM SET LOCATION OF USR (X)
1100  REM SUBROUTINE FOR TIME
1110  R = PEEK (50954) AND 56: REM RECALL CURRENT VALUES ON THIS PORT
1120  POKE 50954, 192 + R: POKE 50954, 64 + R: REM UPDATE "DISPLAY"
1130  X = USR(X): REM CALL MACHINE LANGUAGE SUBROUTINE
1140  FOR L = 0 TO 7
1150  T(L) = PEEK (49143 + L): REM PULL VALUES OF TIME DIGITS FROM MEMORY
1160  NEXTL
1170  REM T(0) CONTAINS S/100 VALUE, T(1) CONTAINS S/10 VALUE, ETC.
1180  RETURN
```

Table 4: A BASIC program to read the current time from the clock. The program assumes the clock has already been reset and may have been started. The start/stop line is toggled in lines 1110 and 1120 by outputting to the clock by way of the port located at 50954_{10}. The machine language routine (Table 3) is accessed at 1130 and retrieves the values from memory and stores them in an array T(L). From this array one can readily form the time in hours, minutes and seconds. A test can be added to change dates and months.

Procedure And Software

In order to use this real time clock, the reset line is brought momentarily low; the first negative slope on the Start/Stop (abbreviated S/S) line starts the time. If the S/S line is brought high and then low, the "display" then freezes while the clock chip continues timing. The computer can read this time by a machine language program (**Table 3**; the multiplexed output from the clock is too fast for most BASICs.) Each time the S/S line is brought high and then low, the "display" is updated to the current time. Thus, in use, the computer toggles the S/S line and goes to the machine language subroutine that reads the time digits. The computer does this only when it needs to know the current time.

In our application, the computer utilizing this real time clock does data acquisition and control using the BASIC language. BASIC can transfer to a machine language routine and back again. Our computer uses a 6502 μP so that the machine language subroutine in Table 3 is specific for this processor. The program has the processor read the parallel port (configured as memory location 50958_{10} or $C70E_{16}$) and decode the information to determine the value for each digit. This value is stored in a table in memory where the 0.01 sec digit's value is located in 49143_{10} ($BFF7_{16}$), the 0.1 sec digit's value is in location 49144_{10} ($BFF8_{16}$) and so on. A flow chart of the program is shown in **Figure 3** and will allow a corresponding routine to be written for other μPs. The portion of the BASIC program that calls the machine language routine is shown in **Table 4.**

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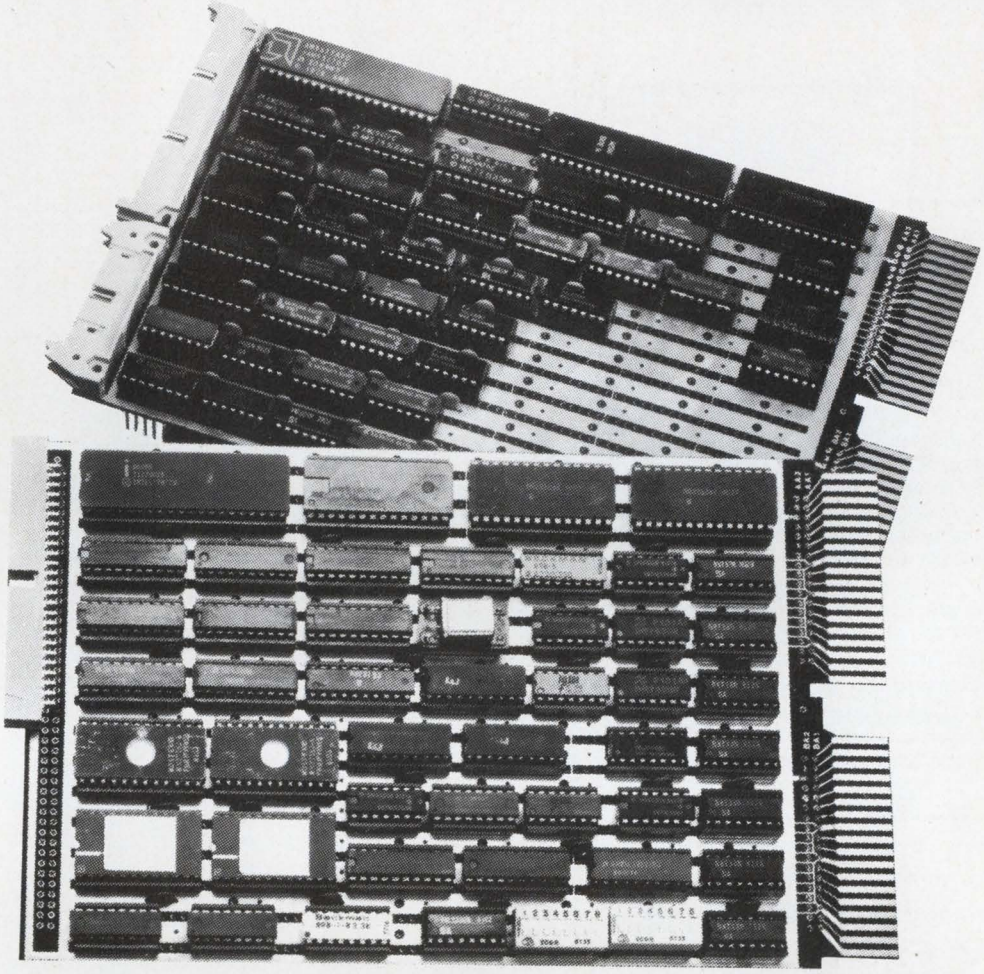

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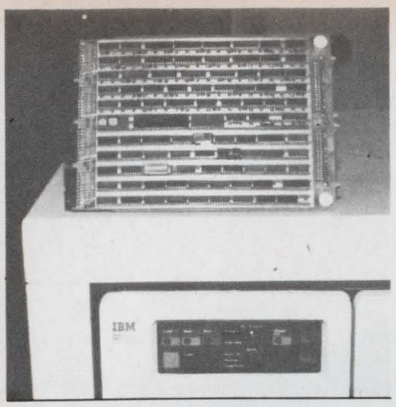

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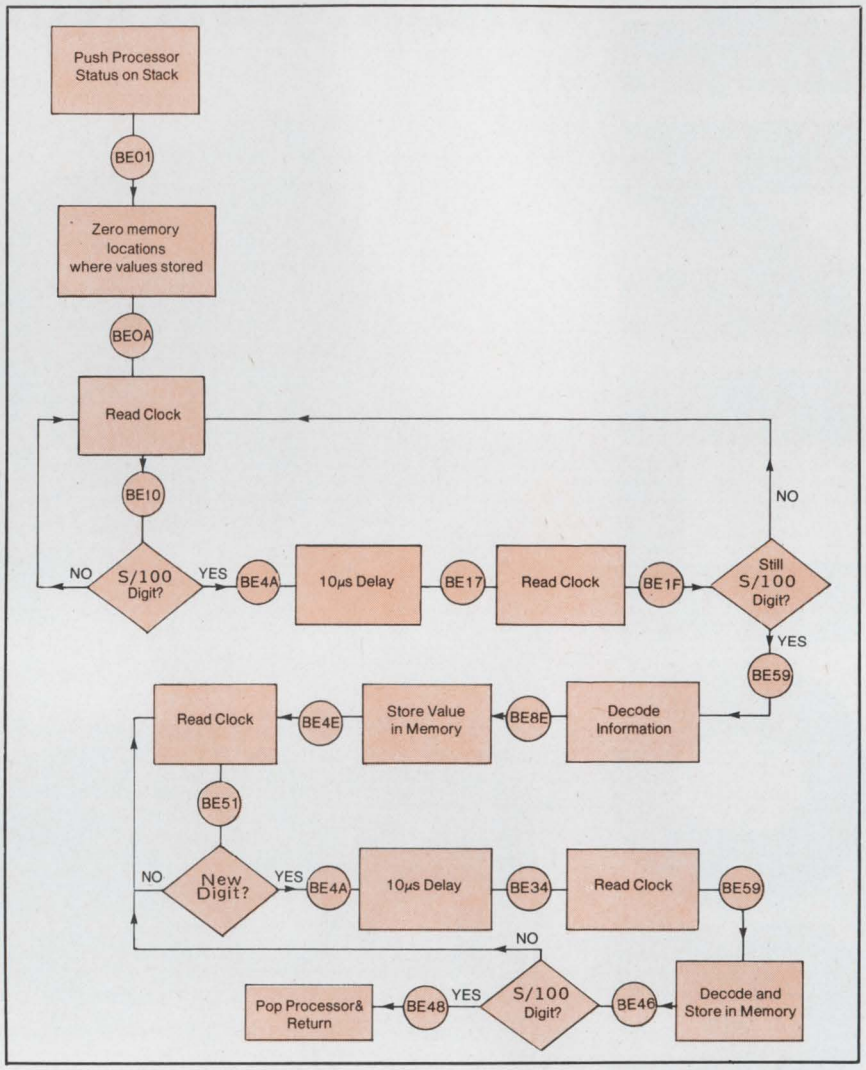


Figure 3: Flow Chart of the machine language subroutine that reads the parallel input port connected to the real time clock. The routine decodes the information in the 8 bit word and determines the value of the digit and stores that in a corresponding memory location. The Hex memory locations of the instructions in Table 3 are shown adjacent to each box. The first loop finds the .01s (S/100) digit (the 10μs delay insures stable voltage levels) while the second loop waits for the next digit, and decodes and stores it. This continues until the S/100 digit appears again. The time to read and store all eight digits can vary from 0.8ms to 1.5ms depending on which digit is being output by the clock when this subroutine begins.

The parameter T(L) contains the time with T(0) having the value of the S/100 digit and T(7) having the value of the 10 hour digit.

The real time clock has been working very well for the last six months. It makes efficient use of the processor's time, yet allows high resolution in timing. Successive timings as short as 180ms can be done using BASIC while timings of 0.01sec (resolution of the clock) are possible using only machine language. The six chips needed to construct this clock make it inexpensive and easy to construct. The interface to the computer is straightforward and allows μCs to access the current time for calculations or recording events.

Finally, I'd like to express my appreciation to Research Corporation for funding the research which led, in part, to this design.

D.T. Jacobs, Dept. of Physics, The College of Wooster, Wooster, OH 44696.

The Three Printing Modes Of Low-Cost Dot-Matrix Printers

by Joseph A. King

Incorporation of electronic memory, and electromechanical advances are vastly expanding the capability of the low-to-moderate cost dot-matrix printer. From a somewhat noisy, relatively slow device for the sole task of data processing output a decade ago, this class of printers has been enhanced to perform three major functions in a single machine—data processing, word processing, and graphics. The sophisticated package is available at about the cost of a single printer for each of the three functions previously. It provides an important new output alternative for the computer systems designer, integrator and user.

Joseph A. King is Peripherals Product Specialist for Anadex, Inc, Chatsworth, CA.

Data processing, word processing and graphics are now performed in a single inexpensive machine.

Anatomy Of The Printer

Five major elements make up new triple-function dot-matrix printers. The functional block diagram (**Figure 1**) illustrates the operating relationship between the elements:

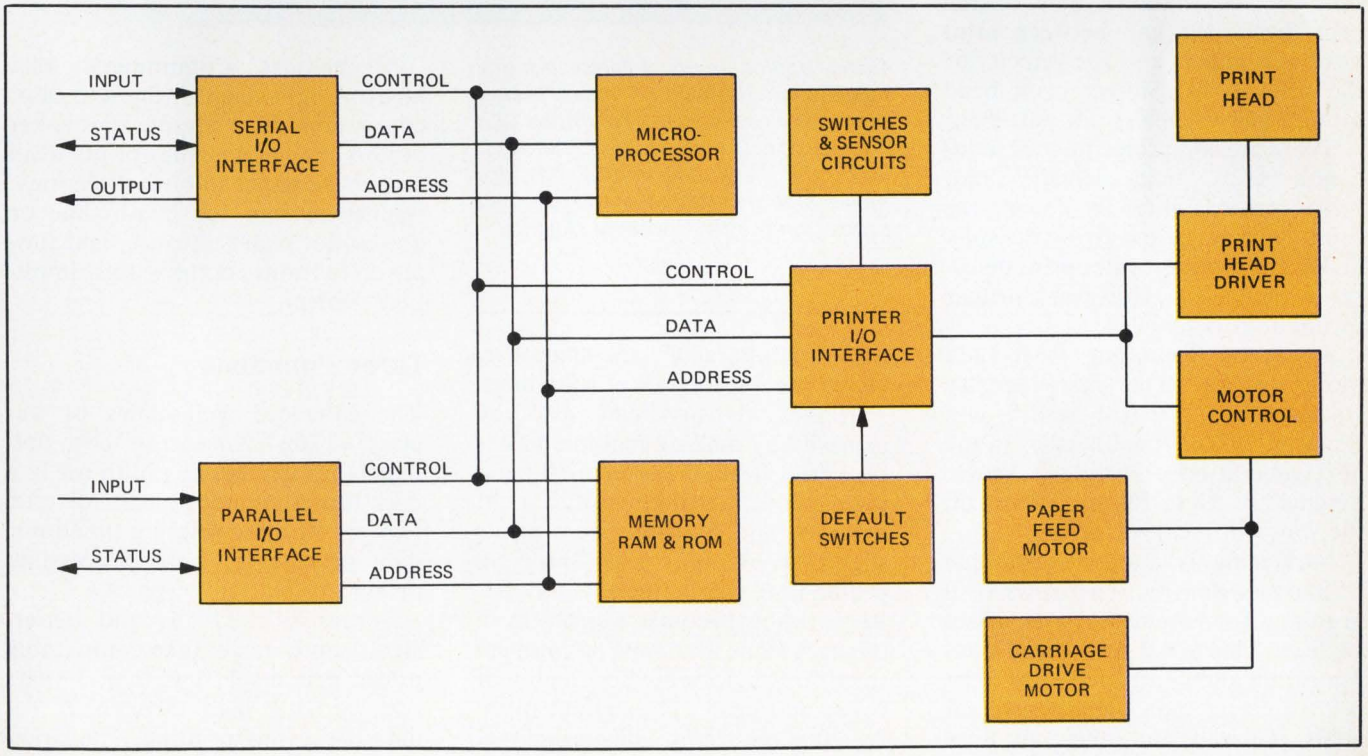
Data Receipt Element: Receives and converts, as required, incoming data into a format useable by the μP for storage and later printing.

Data Storage Element: Buffer capacities range from 1000 characters upward. For a simple, single-mode alphanumeric printer, a minimum of 1000 characters of buffer storage is desirable. For graphics and correspondence printing, storage of 2000 to 20,000 characters can be required to store look-up tables for special character sets and graphic symbols.

Control Element: The μP performs a number of functions simultaneously:

- Timing of data receipt, data storage, and print functions.
- Logic decisions. For example, a single instruction will be accepted. The μP then logically performs a

Figure 1: Functional block diagram of a typical μP-controlled dot-matrix printer.



series of actions in the printers.
- Status of horizontal and vertical positions on the paper.
- Receipt of next instruction.

Print Head Element: The printing needles, encased in the print head, are driven by small electromagnetic solenoids. The needles are actuated in synchronization with head and paper movement, causing one or more dots to be printed. In a 9-needle print head, for example, seven dots are printed vertically to form the backbone of the letter "B." In the next strobe, only the first, fourth, and seventh needles are printed, forming the top, middle, and bottom shape of the "B" form. Up to 13 or 14 strobes may be required to print the full image. In most printers, the bottom two needles are used for lower-case descenders or for underlining.

When the solenoid strikes the end of a needle, the needle flies forward in a ballistic, guided trajectory, and strikes the paper in "free flight." This minimizes wear on the end of the needle. A finite amount of time is required from application of current to the solenoid, causing the needle to fly forward, make contact and rebound; and for the solenoid field to collapse for the next pulse. Hence, dot density becomes a function of the characteristics of the print head, the gap between print head and paper, and the velocity of the print head. Slower print head motion allows denser dot patterns.

There are several techniques to increase print head density, and, hence, print quality. By slowing the print head down and firing the solenoids at a constant rate, print density is increased. However, printer throughput is reduced.

A second technique is to add more needles. The first industry standard of 7 vertical needles was replaced by 9 vertical needles in the next generation of printers. Newer designs are using 18, and others on the way will incorporate 24.

Interlacing is another technique to increase density. Two rows of 9 needles, for example, are offset slightly. This 9 x 2 print head configuration allows adjacent dots to be printed closer than one dot interval apart. Curved and diagonal lines within a character are smoother, giving the appearance of solid lines.

Higher density can also be achieved by making multiple passes of a print head. After the first pass, the paper is moved vertically a slight amount, and a second pass prints slightly overlapping dots. This is repeated until the character is formed. Registration becomes a problem in this technique and must be compensated for by accurate positioning of paper and head. Throughput (print speed) is reduced by this technique.

Cover photo: In its graphics printing mode, a moving-head dot-matrix printer produces a two-dimensional display of a 3-dimensional mathematical function. The print head and ribbon cartridge moves bidirectionally across a page and prints "on the fly," without stopping.

Mechanical Components Element: A lightweight frame and case, continuous drive motors or stepper motors to move the print head across the paper in both directions, stepper motors for line-by-line or dot-by-dot paper advance, and simple drive trains comprise this simplified element.

Three Functions

The enhanced capabilities of this class of low-to-moderate cost dot-matrix printer can be put to use in a desk-top computer system for one, two, or all three printing functions: data processing, word processing, or high-resolution graphics.

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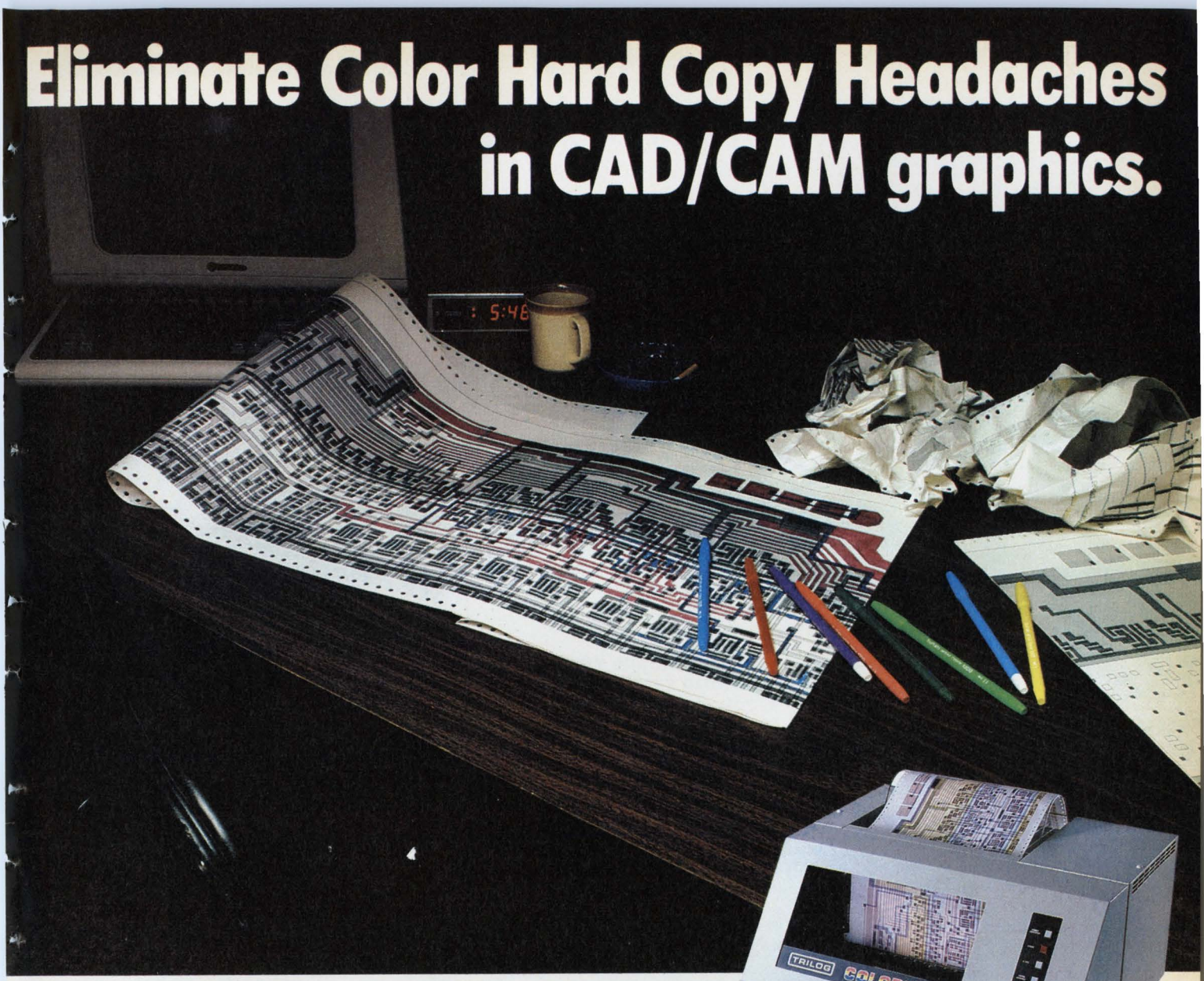

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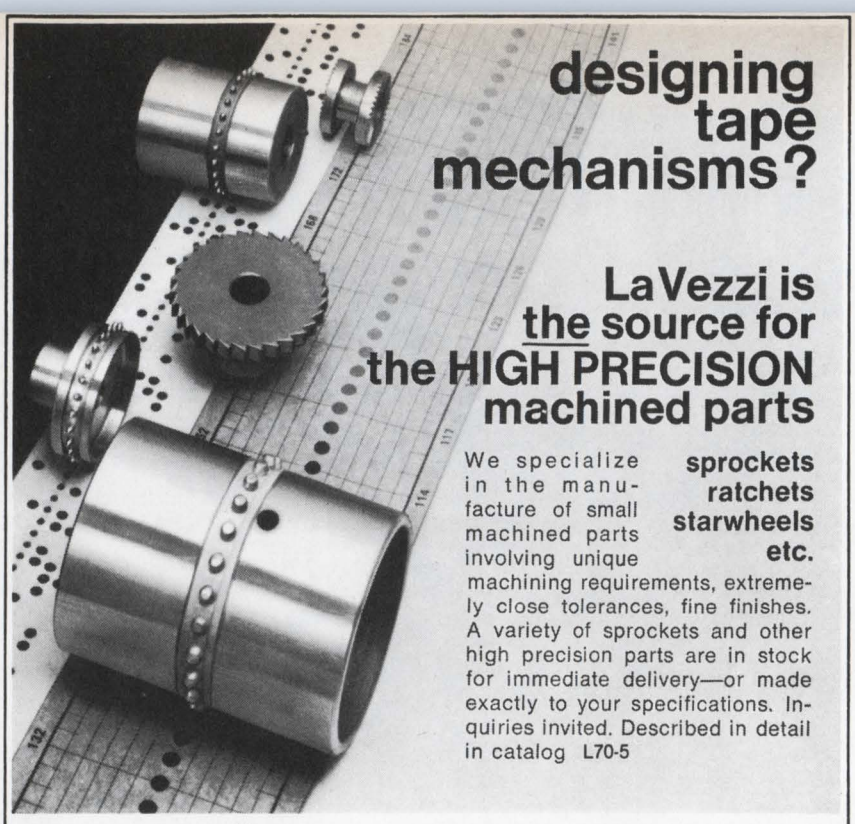

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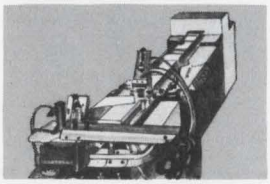

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Three Printing Modes

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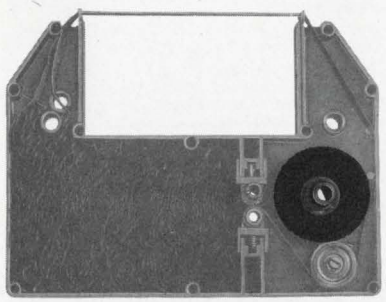

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The Technique Of Graphic Printing

by Joseph A. King

In the conventional use of small computer systems — whether in engineering, education, or business — information is stored and manipulated, then printed in traditional alphanumeric, tabular form. Technological advances, however, are providing an exciting, new dimension to computer output — the graphic display of this data. Improvements have been made in the resolution of both color and black-and-white CRT displays. Low-cost memory devices have been developed. These have been combined with sophisticated software that can manipulate and present data pictorially. Graphic output has thus become a practical reality for even the most modest computer budget.

Growing use of CRT-based graphics has spawned the need for hard copy printout, since CRT terminals can't be picked up and carried to the next office, a duction of sophisticated, high-resolution graphics—gives designers and integrators a new range of applications. Resolution, previously a limiting factor in achieving perceived print quality, has been sharply enhanced in the newest printers. In fact, most printers now achieve a resolution higher than that of the average CRT (and in some cases, double). And a growing range of graphic software packages and drives are becoming available for use on these low-cost dot-matrix printers.

Some of the major applications that are now taking root are:

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0 0	1 0	2 0	3 0	4 0	5 0	6 0	7 0
0 1	1 1	2 1	3 1	4 1	5 1	6 1	7 1
0 2	1 2	2 2	3 2	4 2	5 2	6 2	7 2
0 3	1 3	2 3	3 3	4 3	5 3	6 3	7 3
0 4	1 4	2 4	3 4	4 4	5 4	6 4	7 4
0 5	1 5	2 5	3 5	4 5	5 5	6 5	7 5
0 6	1 6	2 6	3 6	4 6	5 6	6 6	7 6
0 7	1 7	2 7	3 7	4 7	5 7	6 7	7 7

Figure 1: A typical CRT memory map-to-printer graphics byte relationship. Shaded column on left represents the 8-bit byte transferred by computer for printing in a vertical row by the printer.

Continued on pg. 42

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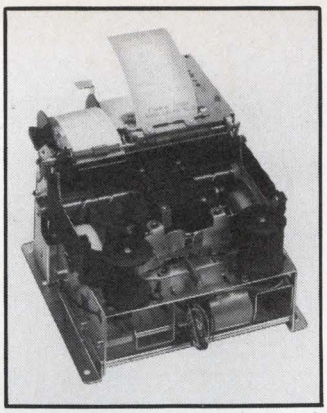

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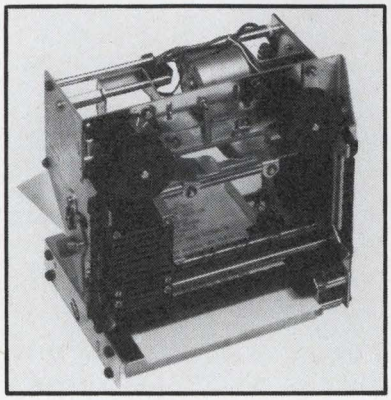

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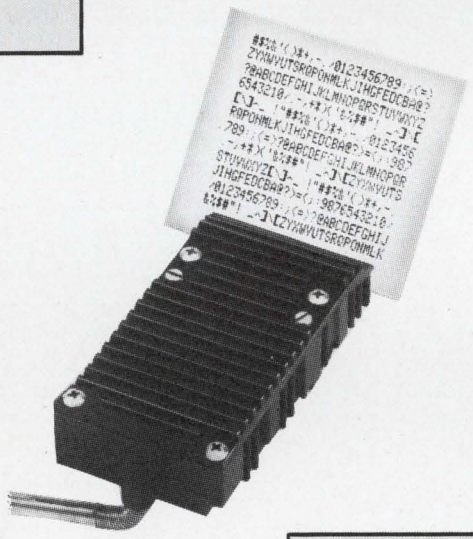

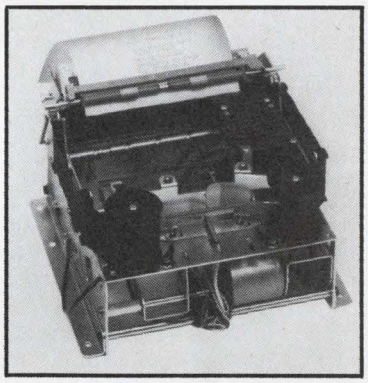

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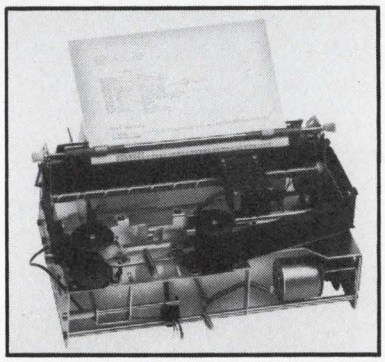

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Graphic Printing

continued from pg. 40

client's plant, the boardroom, or a classroom. Continuous line plotters and similar devices are capable of producing hard copy, but are relatively slow and expensive. Moreover, a plotter normally performs a dedicated function only. There is a new and practical solution: Hard copy generated on the newer dot matrix printers. These printers are versatile, multipurpose machines that offer dot-addressable graphics as an alternative mode. Because the same fundamental technique is used to present data graphically, the dot matrix printer is ideal for generating printed copy from CRT graphics. In fact, dot-addressable printers are more graphically versatile than CRTs. Like plotters, the amount and shape of information that can be presented on a dot matrix printer is limited only by the width and length of the paper supply and the programmer's imagination.

The technique for supplying graphic data to a dot-addressable printer varies slightly from printer to printer, but the basic concept is the same. The 8 bits in a data byte transferred from a computer represent from 1 to 8 vertical dots to be printed or not printed. Usually the "1" bit represents a dot to be printed and the "0" bit represents a dot to be omitted. The next byte defines the dot pattern of the next vertical column of dots and so on across the paper until that horizontal pass of the print head is completed. A byte, or series of bytes, then provides instructions to the printer to move the paper to the next position and the next horizontal pass is begun.

The method of generating data in a form useable by the printer varies according to the form of the data base. For example, if the data is simply a transfer from the graphic presentation on the CRT, and there is no concern for the difference in aspect ratios of the two devices, a simple dot-for-dot transfer is possible. A byte from the 1 or 0 values of the first dots of successive video scans is composed and transferred to the printer. This is repeated for the next horizontal CRT dot position until the first pass is completed. The paper is moved and the location of the sample is shifted down one byte increment. The process is repeated until the complete CRT display has been printed.

When generating graphics output directly from the data base, the process becomes more complex. The techniques are essentially identical to those used for generating the original CRT graphics. The data base is scanned and a bit map is generated in memory. The bit map has a one-to-one correspondence to the possible dot positions on the paper. Each dot location is represented by a unique address in the map. The memory is then scanned and the graphic bytes are generated for output to the printer. If the entire picture is bit mapped before outputting to the printer, a large block of memory must be reserved. An alternate technique would be to generate a bit map for only one pass of the printhead. After outputting the data to the printer, a new map is then generated for the next pass.

Another technique is the use of look-up shape tables. This is similar to the technique used to generate characters in normal alphanumeric printing, however, the shape table is contained within the printer. The printer's firmware interprets the incoming data and makes the conversion. In graphic printing, the computer's data base would be scanned. The matching shape from the look-up table would then be transmitted to the printer much in the same way as in the bit map technique. Computer memory requirements for this method can exceed that of bit mapping. Shapes which are not required for a particular presentation are contained in the look-up table. This is offset by the probability of multiple uses of the same shape.

Printers with dot-addressable graphics are becoming the norm and are available from a few hundred dollars to several thousand. Their capabilities vary from block-shaped graphics to extremely accurate and high-resolution dot graphics. Presently, there are only a few dot-addressable color printers available. Color displays must by necessity be presented in hard copy by gray scale patterns. However, with the recent advances in color CRT displays, moderately priced color printers will become available in the near future to match the advances in CRT display technology.

scanned to form the composite data byte to the printer. Also, as the accompanying story on the technique of graphic printing points out, CRT raster graphics must usually be transferred in 6 to 8 video-line bursts for most printers.

Presentation of Engineering and Mathematical Data: A two-dimensional presentation of three-dimensional algorithms is a sophisticated graphics application. In a computer-assisted design application, a 3-D display of a new part designed from a data base can be printed.

Special Character Sets: Practically any desired shape can be created on a dot addressable matrix printer. These images include type fonts, ranging from cursive script to original faces. Logotypes, headings, and labels can be generated. Special character sets can be printed in a range of sizes, from condensed to page-high-and-wide dimensions.

Complex charts, graphs and tables can be printed.

Business Operations Data: Complex charts, graphs, and tables can be intermixed with text and printed.

Even as the new, triple-mode device begins to enter the marketplace, more technological developments promise to expand the capabilities of this class of printer even further. For example, color printing is making an entry-level impact in the marketplace, and should experience major improvements in color selection, resolution, and consistency. □

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Putting The Lid On Printer Noise

by Bob Hirshon

Recent advances in print head technology and on-board intelligence now allow dot matrix printers to produce near letter-quality type. But now that printers perform well enough to be considered for office applications, they must conform to new constraints imposed by an environment for which they were never intended. One of these constraints is acoustic noise.

Ambient noise levels in an office with no one speaking measure about 55dB to 60dB. Conversation can boost that up to 65dB (an increase of 3dB means a doubling of actual noise). If you add machinery producing sound levels over 75dB, that conversation comes to an abrupt halt — research indicates that this is the level at which speech is interrupted. When one considers that many impact printers operate at 75dB, it's easy to see why they are often unwelcome in office environments.

One answer to this printer noise problem is isolation of the printer in a sound-damping enclosure. Gates Acoustinet (Santa Rosa, CA) is one of several companies that make enclosures specifically for this purpose. Called "Sound Controllers", they can decrease emitted noise levels more than 10dB. On the negative side, however, sound-proof enclosures may impede user access to the printer, even as they impede the escape of printer noise. One consideration in the use of these enclosures, then, is how frequently the hard copy needs to be accessed.

Printer manufacturers are coming up with ways of their own to combat printer noise. Basically, they have two choices: they can either redesign the electro-mechanics of the printer so it produces less noise from the start, or they can try to prevent noise from escaping the printer case.

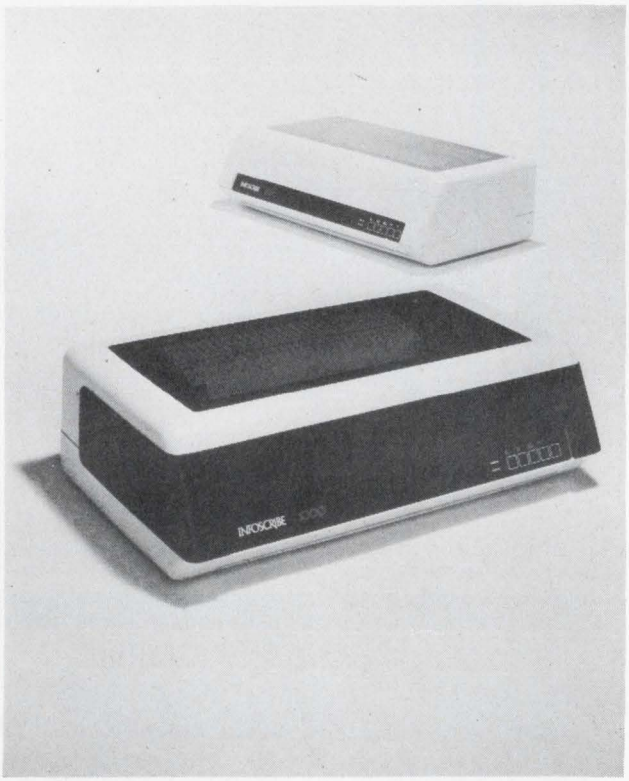
When electro-mechanical redesign is the chosen route, printer motors are prime targets. Motors used for printhead and paper positioning are major culprits in printer noise problems. Dataroyal, when designing their IPS-500 printers, simply replaced solenoids, clutches, and cams with quieter stepper motors, thereby reducing internal noise considerably. Infoscribe, in the design of their model 1000, quieted things down even further by using a closed loop servo system.

Prevention of printer noise transmission can follow several routes: materials choice, cabinet design, and proper use of sound-damping materials all can produce dramatic results.

Judicious choice of materials can silence printers by absorbing rather than transmitting noise. For example, since regular steel tends to vibrate and amplify noise, Dataroyal uses vibration-resistant extruded metal for their mechanism housing. In addition, their case is a tough, sound-resistant polycarbonate plastic.

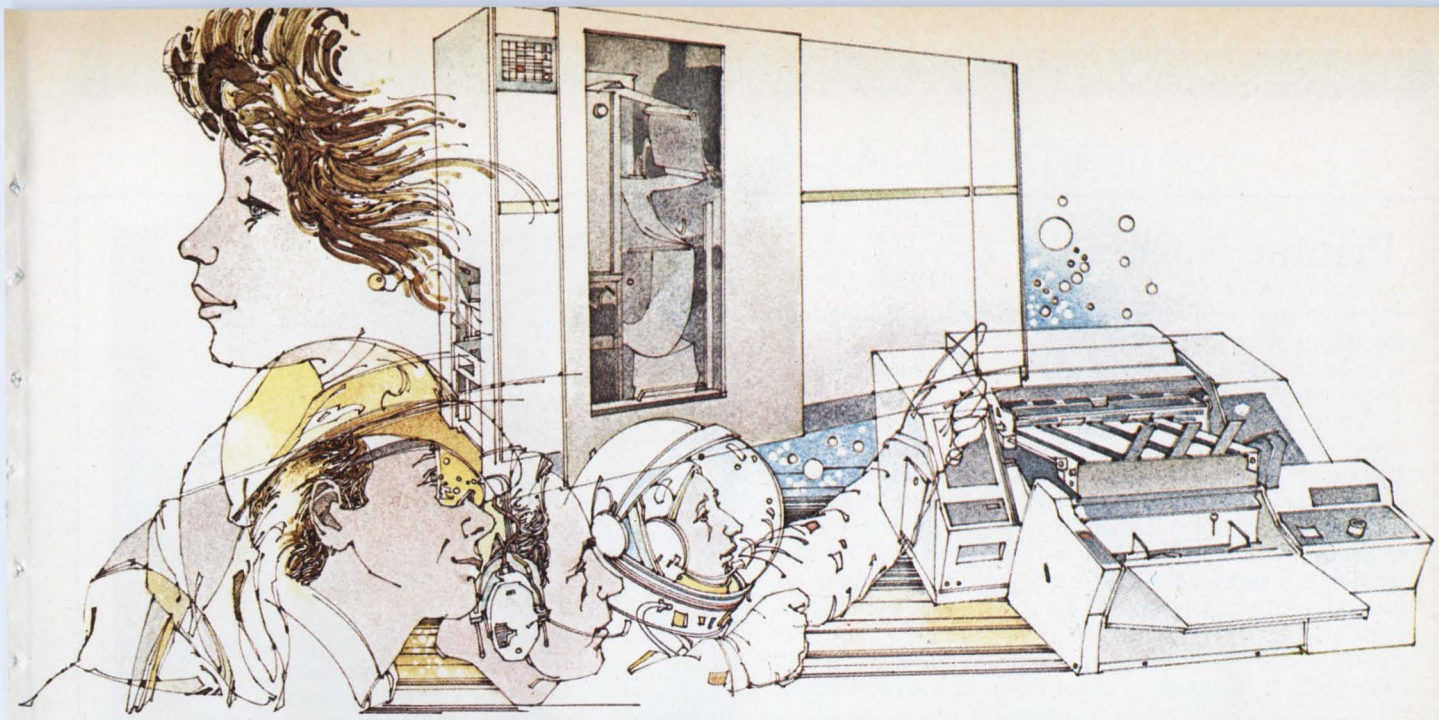
Thoughtful cabinet design can also reduce noise. Gaps and holes in a printer's case, for instance, provide ports through which noise can escape. Consequently, Infoscribe made several changes in their case to eliminate openings where possible, and to locate those that were absolutely necessary where they would raise noise levels the least (**Figure 1**). For example, because paper transmits considerable amounts of noise, the model 1000 has a rear paper exit, lowering noise levels in front of the machine. In addition, they seal their cabinet with an S-type overlap, trapping sound inside the case. Conventional switches require enclosure holes, so Infoscribe replaced them with membrane switches. Finally, where knobs were absolutely necessary (for adjustment purposes), they were located within the case, making them less accessible, but making the printer tighter and quieter.

Figure 1: Tight case design contributes to this printer's low noise emission levels. Note membrane switches that eliminate the holes associated with conventional switches.



Using sound damping materials is perhaps the easiest and most effective way to make large reductions in printer noise. Dataroyal uses a material made by Specialty Composites Corp (Newark, DE) called Tufcote Noise Damper (TND) which consists of a damping pad combined with acoustical foam. Damping pads alone (Ted-Pads) are affixed to the base of the cabinet and applied to the platen and other metal surfaces that vibrate and transmit noise. TND is used throughout the interior of the chassis and cabinet, and optionally at the paper entrance and exit (**Figure 2**).

Continued on pg. 46



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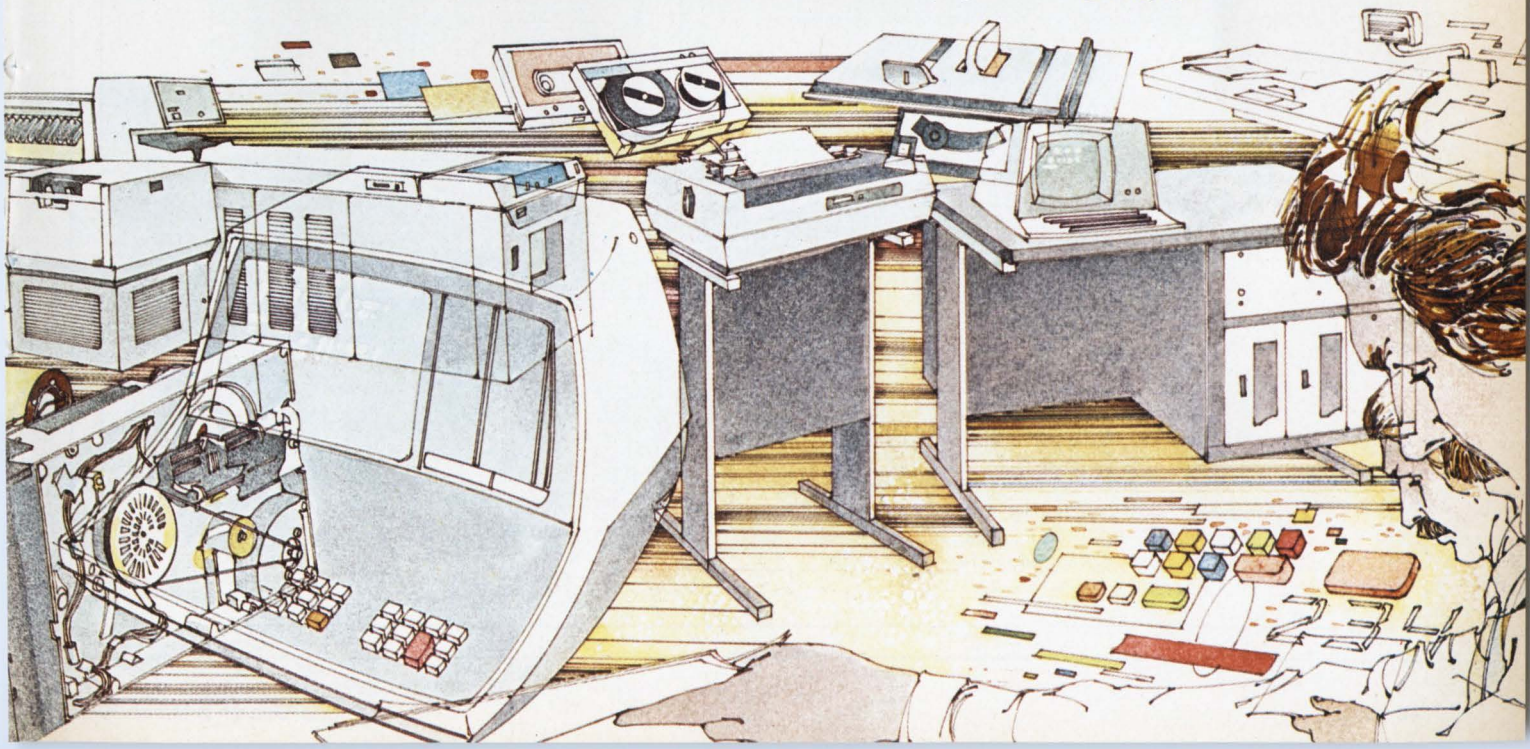


Printer Noise

Continued from pg. 44

Infoscribe similarly uses Soundfoam (Soundcoat Co, Santa Ana, CA) to line their model 1000, and this is a large factor contributing to their low noise levels of under 54dB (**Figure 3**).

While quiet printers have a marketing edge over other printers in America, they may enjoy a market of their own in Europe; strict European noise emission standards (especially German VDE) propose maximum noise levels of 55dB. Laser and ink jet printers already operate at these low levels, but are more costly than impact printers and don't produce multiple copies. As a result, impact printer manufacturers who can design a printer to meet European noise emission requirements without boosting costs to laser/ink jet levels may soon enjoy sales in a lucrative, exclusive market.

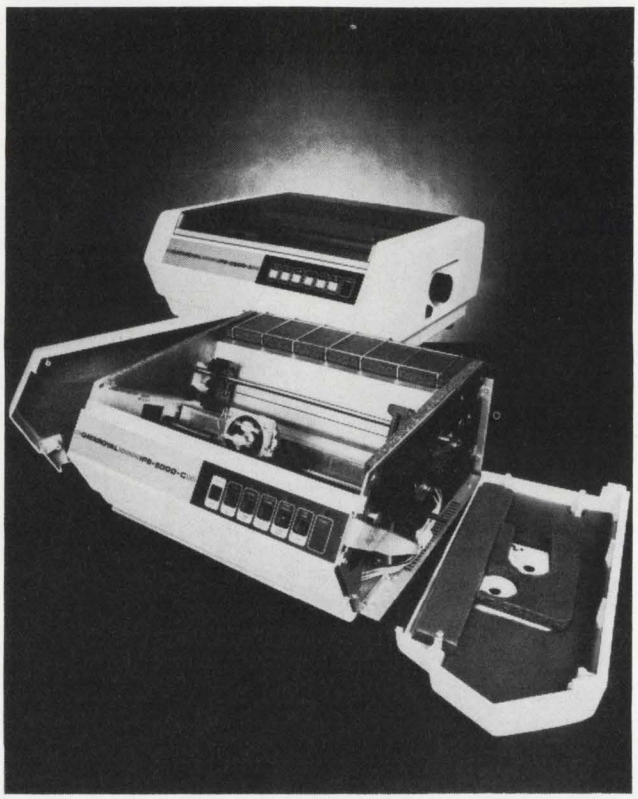
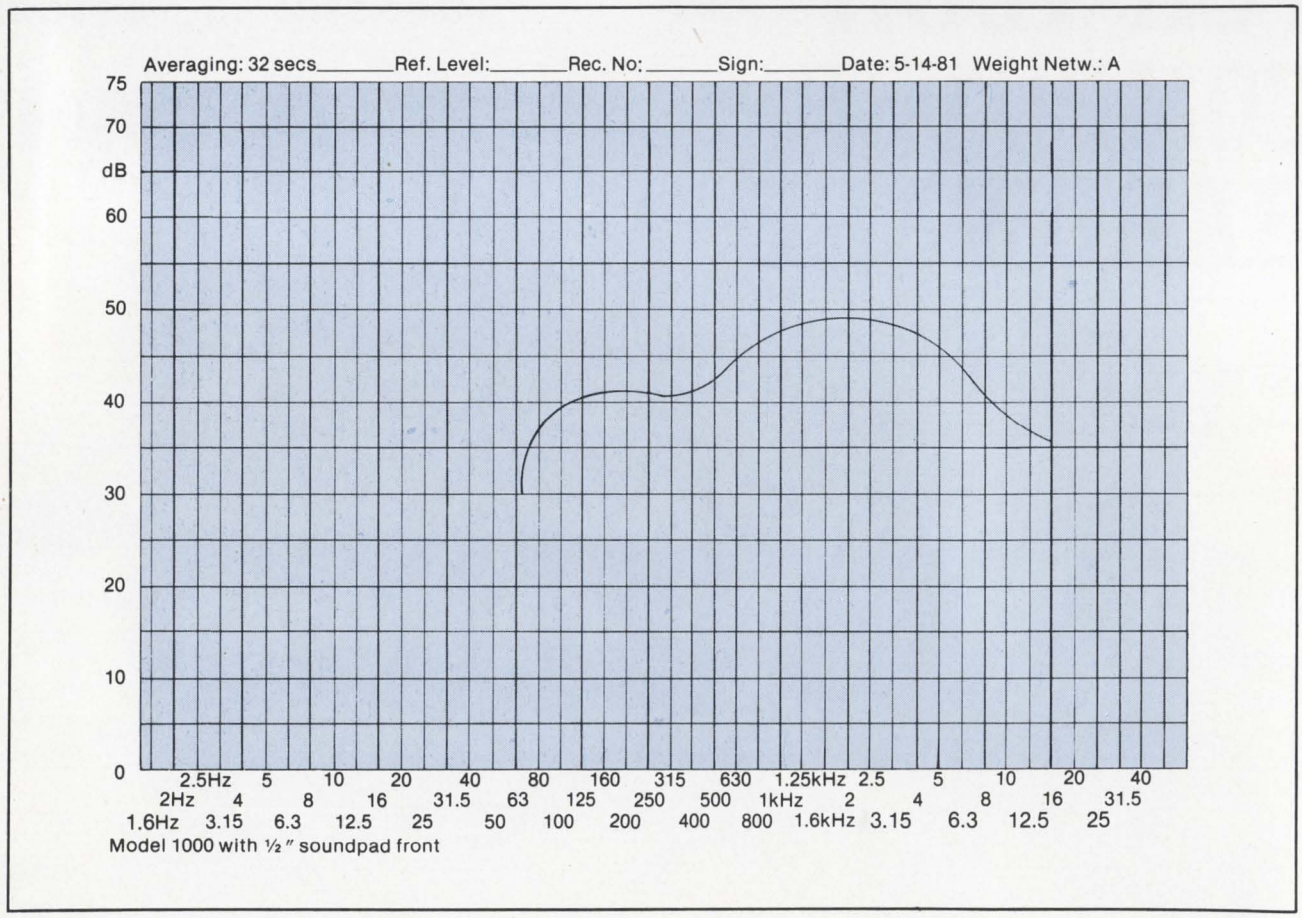


Figure 2: To achieve quiet operation, picture on right shows how die-cut parts of Tufcote Noise Damper are placed in strategic locations throughout this serial impact printer.

Figure 3: Based on testing using the Acoustical Society's ANSI S1.29-1979 (ASA 29-1979) specifications, this graph shows Model 1000's noise output over individual octave band levels from 63Hz to 16 KHz. The printer was ultimately rated at 53.9dBA.



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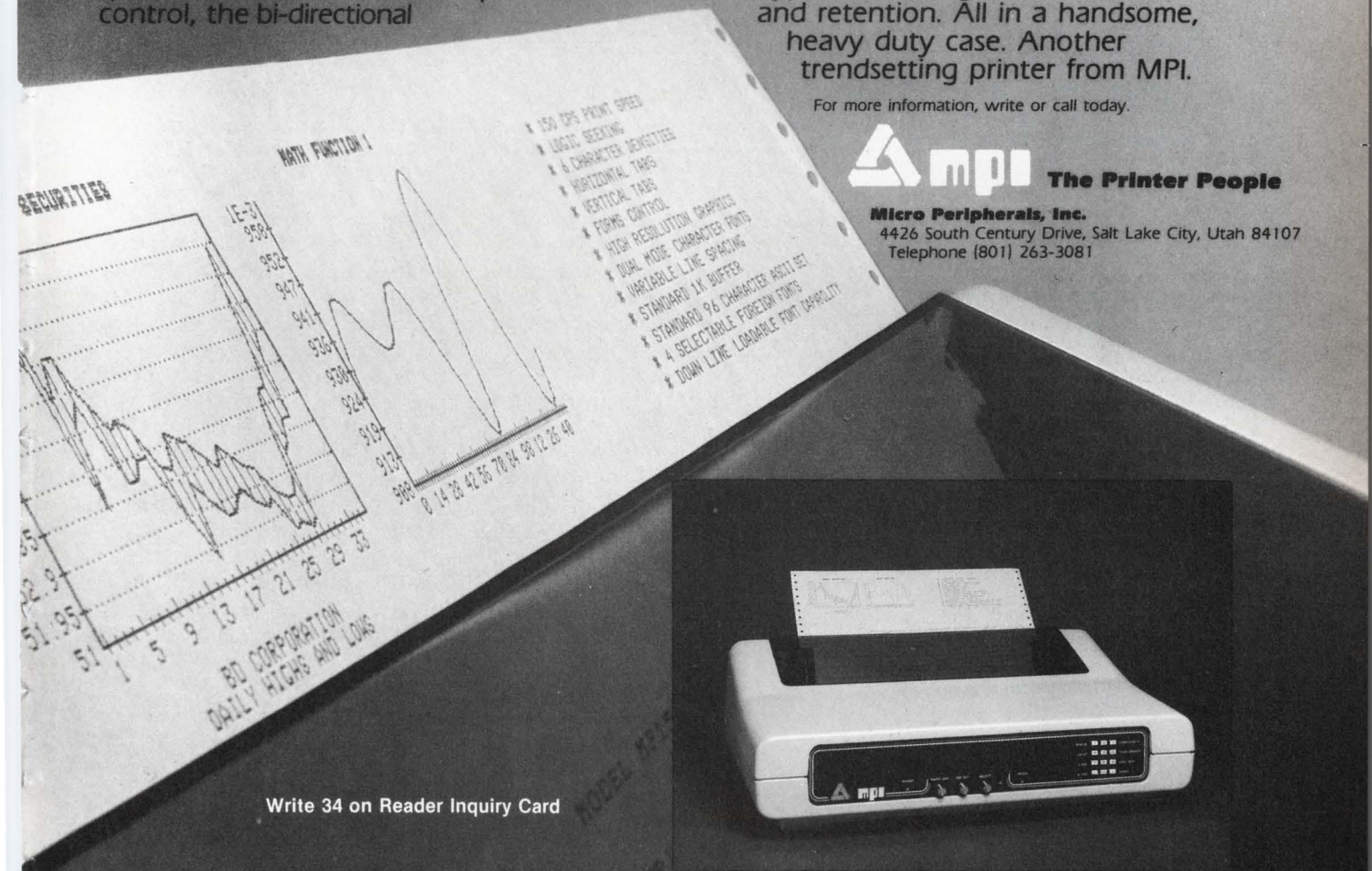

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Peripheral Controllers: New Trade-Offs For 1982

by Bill Groves

Driven by the recession of the past year, many semiconductor producers are announcing or planning to announce new controller products that will make your job easier. A lot of careful planning and design has been going on during 1981 — now the pay off is at hand.

Trade-offs in controller selection have been quite simple in the past. If you selected a μP system you had to find devices that would play with that particular processor. That meant that control and access to the peripherals was time and performance dependent on the μP. The number of devices available to support each processor family and its second sources probably numbers several hundred. They will also be with us for a long time to come. For a large percentage of applications they do the job well.

The new twists for this year are smarter approaches to peripheral control, much better performance, and more efforts to standardize interfaces. In all, the designer beginning to think about a new peripheral controller system has many more and better options.

High Performance Controllers

High data rates are not new, but trying to keep a total system running at a nominal data rate of a few MB has been a very challenging problem. The 2901 Bit Slice was one of the only solutions to the high data rate problem. It is a 16-bit machine so it was not easy to use in an 8-bit control application. It also required a large number of support chips to turn it into an operational peripheral controller. A dozen or more added devices were not uncommon. In 16-bit applications, it is still untouchable — at least for now.

If you are designing a peripheral controller of any type, 1982 looks like it will be the best year yet for better, smarter, and cheaper control solutions.

In 1980 Signetics introduced the 8X300 family of μcontroller chips. These filled many of the high speed applications, but they did not offer the really high performance needed for new technologies like hard disk controllers. The 8X300 bipolar TTL chips have found many applications as floppy, CRT, printer, etc. controllers. The 8X300 μcontroller brought a lot of smarts to the world of peripheral control.

Now Signetics has bettered their own system. In late January, they announced the 8X305 μcontroller family. This looks like one of the more interesting high speed μcontrollers yet to emerge. Homework has been done on the new 8X305 and the lights are still burning in Sunnyvale.

Basically the 8X305 is a low power Schottky TTL 8-bit μcontroller family featuring a 200 nsec cycle time (25% faster than the 8X300 series). It has an expanded instruction set and seven additional registers to improve overall throughput. The 8X305 μcontroller is supported by 12 additional devices (**Figure 3**) to control and interface with almost any type of peripheral. All are scheduled for full availability by the end of 1982; many are available now. Seven of these support chips are new and five are previously announced 8X300 series parts that are fully compatible with the 8X305 family.

Instant Second Source

A three-bus architecture allows fetching, decoding, and execution of a 16-bit instruction every 200 ns. Top speed is 5 MB/sec., and that makes it the fastest stand-alone, byte-oriented μcontroller yet announced. To make things even more interesting, Signetics has announced this family and AMD as an alternate source at the same time. With AMD coming on stream later in 1982, the 8X305 series has added second source advantages.

During the 200 ns cycle the 8X305 can fetch an instruction from the instructor bus and decode that instruction. Then it executes the instruction, including fetching data from the I/O bus, latching, rotating, masking, performing an ALU operation, shifting, merging, and returning it to the I/O bus. It also computes the next instruction address and places it on the instruction bus within the 200 ns cycle.

Development Systems Available

This device family is fully supported with the American Automation EZ-PRO, a self-contained development system with in-circuit emulation

Bill Groves is **Digital Design's** *West Coast Technical Editor. Operating out of the Campbell, CA Office. Bill can be reached at (408) 371-9620.*

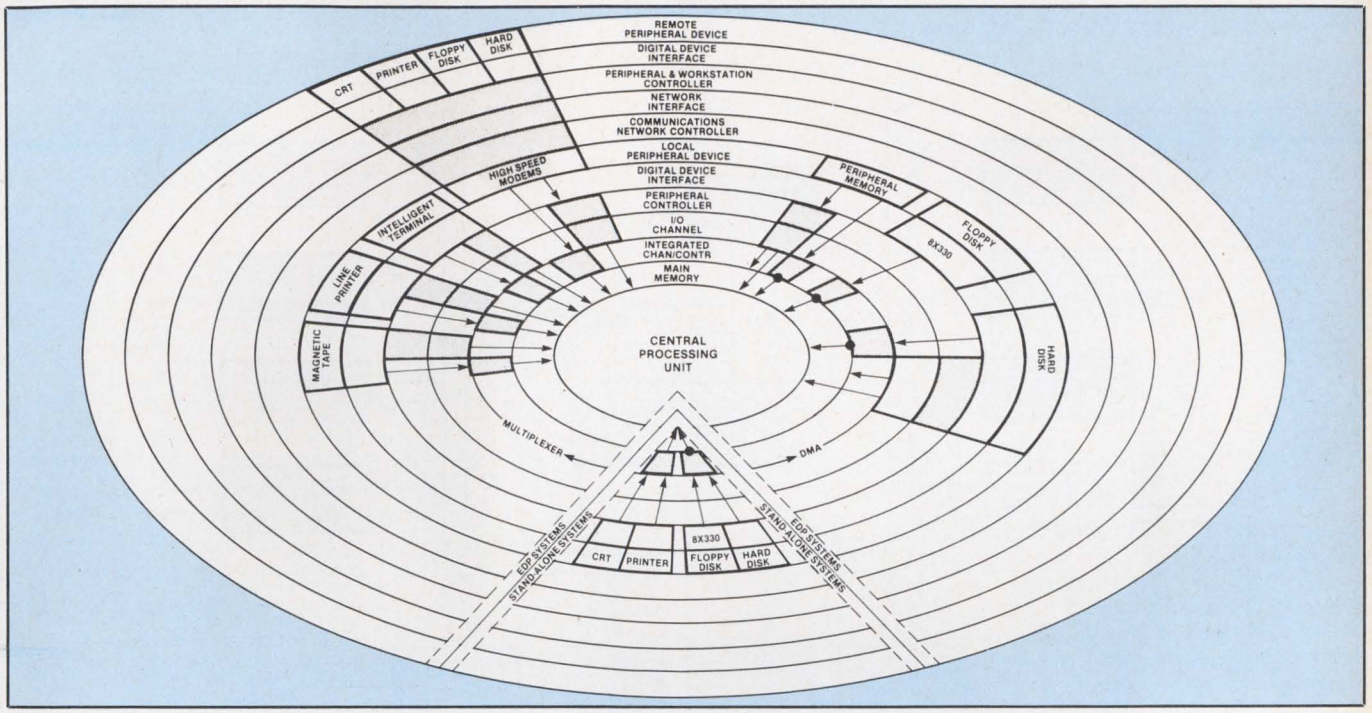

Figure 1: Peripherals and their control are a major segment of the computer world. This chart's rings indicate the size of the peripheral marketplace with the outer rings accounting for the largest portions of the market. Signetics prepared the chart to show applications for its new 8X305 μcontroller family, but it also indicates with the shaded areas all of the one-byte wide applications. The Stand Alone Systems wedge on the ellipse should become the dominant section of the chart in 5 years or so. By far, peripheral control will become a more dominant element of system design as the number of stand alone systems and remote peripherals begin to grow dramatically. Dedicated μP controllers appear to be the solution to many complex peripheral control problems — freeing host computers for more important tasks.

capabilities. Several general purpose computer programs are available to cross-assemble the 8X305 system on other computers and it is fully supported with documentation and training aids.

More peripherals can be controlled at higher speeds, and peripheral types can be interchanged with relative ease. Since the 8X305 can handle data rates up to 5 MB wide it should be able to fit most controller applications through the mid 1980s and probably well beyond. And the 8X305 series is not limited to peripheral control applications; it has obvious advantages for other uses, such as data compression, real-time process control, industrial controllers, and even smart robots. Signetics also plans to offer a military-qualified device in the future for real-time signal processing and digital filtering applications.

Obviously, the 8X305 is a very significant product and it should get a lot of attention for high-speed peripheral control applications. It has little competition now; it has a second source; and it is priced low. The 8X305 chip is going to be available in the second quarter of 1982 and in 100 piece quantities it is expected to sell for $25. The 8X330 floppy disk controller is available now for about $30.

Getting It Together

Sixteen bit μC systems based on the Motorola MC 68000 have been using mainly the Motorola Versabus interconnect structure. Now Motorola, Mostek and Signetics have formed an alliance to standardize some of the technical aspects of the bus interconnects (Mostek and Signetics are alternate sources for the 68000 processor).

Late in 1981, all three companies agreed to use the VME Bus. Based on the European bus standard, DIN 41612 and DIN 41494, it sets mechanical standards for printed circuit boards and backplanes. Also standardized is the DIN type pin and plug style of connector (**Figure 4**). Motorola will also continue to offer Versabus as well.

The VME Bus

Four levels of Bus Arbitration with Bus Busy and Bus Clear control signals permit sharing of the VME bus by multiple processors. In addition, a separate serial link is provided independent of the parallel boards. This permits optimum utilization of the bus bandwidth in a multiple processor system.

An indivisible Read/Modify/Write cycle also permits use of semaphores required for multiple processors to synchronize to each other, or to lock out other processors.

In addition, the seven levels of interrupts may be centralized or distributed among the multiple processors. Asynchronous timing of the bus permits processors, memories, and peripherals of varying speeds to reside in the same system. This permits future upgrading of the processors without changing the peri-

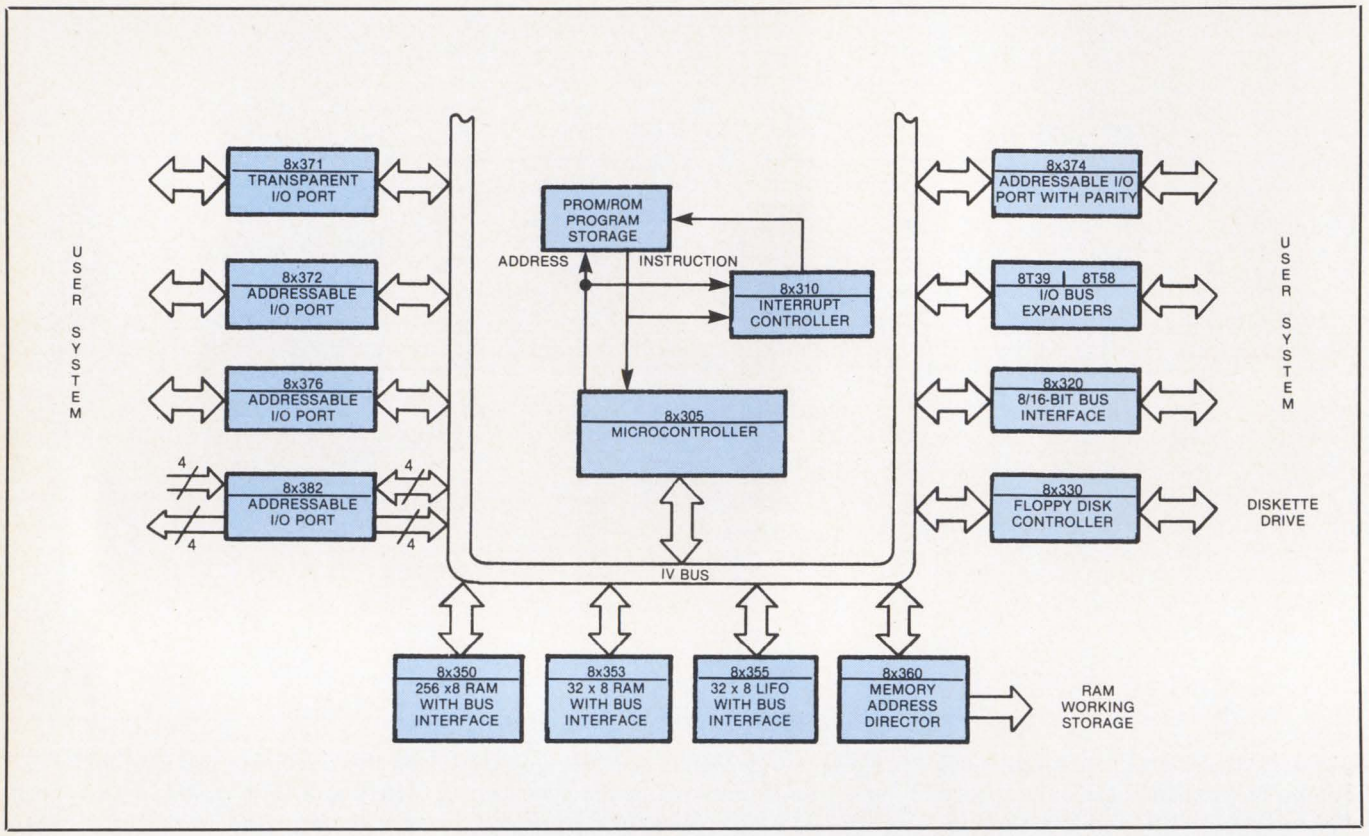

Figure 2: Signetics 8X305 controller system is the first byte-wide controller introduced in the high speed range (200 ns cycle time). It offers a choice of I/O and controller ICs.

pherals or memories. The proposed IEEE standard P896 bus, however, has many of the features of the VME structure with most differences being in the electrical specifications. P896 (Future bus) does propose to use the Eurocard and DIN type connectors of the VME bus.

Multibus from Intel and Q-Bus from DEC both use edge connectors and different PC board sizes. Also both of these bus structures are limited to a 16-bit data width.

Closer to Standards

Peripheral control would be a much easier task if the interconnects were standardized, but that may be a lot farther away than we would like. A least there is some movement in the direction of bus standards. Both VME and IEEE P896 are able to expand in the future; this is not the

8X300 FAMILY OF INTEGRATED CIRCUITS

Part Number	Product Description
8X305	Microcontroller - 200 ns processor for I/O and data control
(1) 8X310	Interrupt Controller - 3 prioritized interrupts with 4-level stack
* 8X320	Bus Interface Array - 2-port RAM for 8/16 bit mailbox interfacing
* 8X330	Floppy Disk Controller - 1Mb/sec data rate, programmable, ECC support
* 8X350	Bipolar RAM - 256X8 high-speed memory with bus interface
(2) 8X360	Memory Address Director - 16-bit address controller for working storage
8X371	Transparent I/O Port - 8-bit bidirectional
8X372	Addressable I/O Port - 8-bit bidirectional, synchronous
(3) 8X374	Addressable I/O Port - 8-bit bidirectional, synchronous, with parity
8X376	Addressable I/O Port - 8-bit bidirectional, asynchronous
8X382	Addressable I/O Port - 4-in/4-out
* 8T39	Addressable Bus Expander - High-drive bus driver
* 8T58	Transparent Bus Expander - High-drive bus driver

* = Part has previously been announced, but is fully supportive of the new generation Microcontroller.
1, 2, 3 = These circuits will be available near the end of the first, second and third quarter, 1982, respectively.

Figure 3: The devices announced by Signetics show the range of control options designed to support the 8X305 processor. A few of the devices are compatible with the 8X300 as well. By the end of 1982, the family should be fully available from both Signetics and AMD. Board level offerings are also coming.

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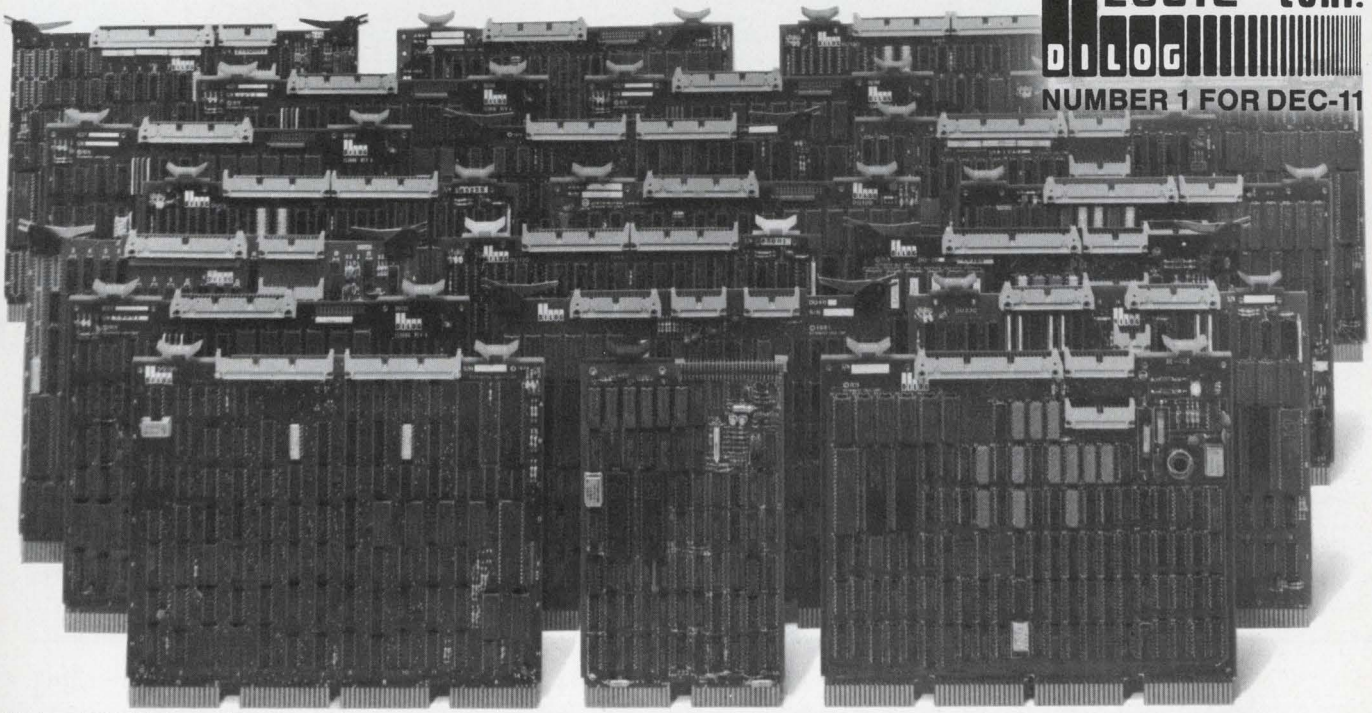

*Trademark Digital Equipment Corp.

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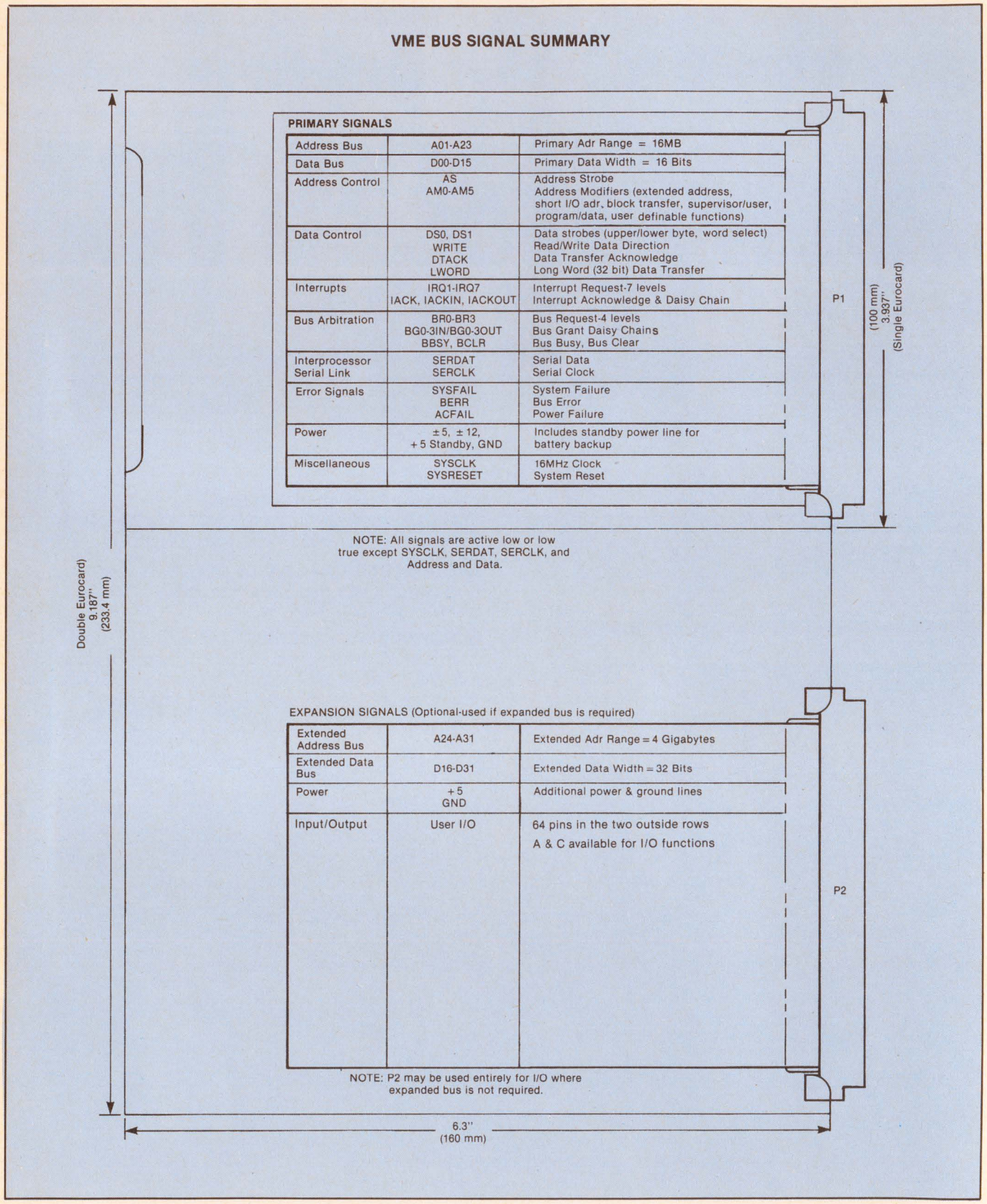

Figure 4: VME Bus Standards are being adopted by Motorala, Signetics, and Mostek for the 68000 processor. This European driven standard has many advantages and room for expansion. It is a serious consideration for export products, and will be offered by all three companies along with the Versabus for the 68000.

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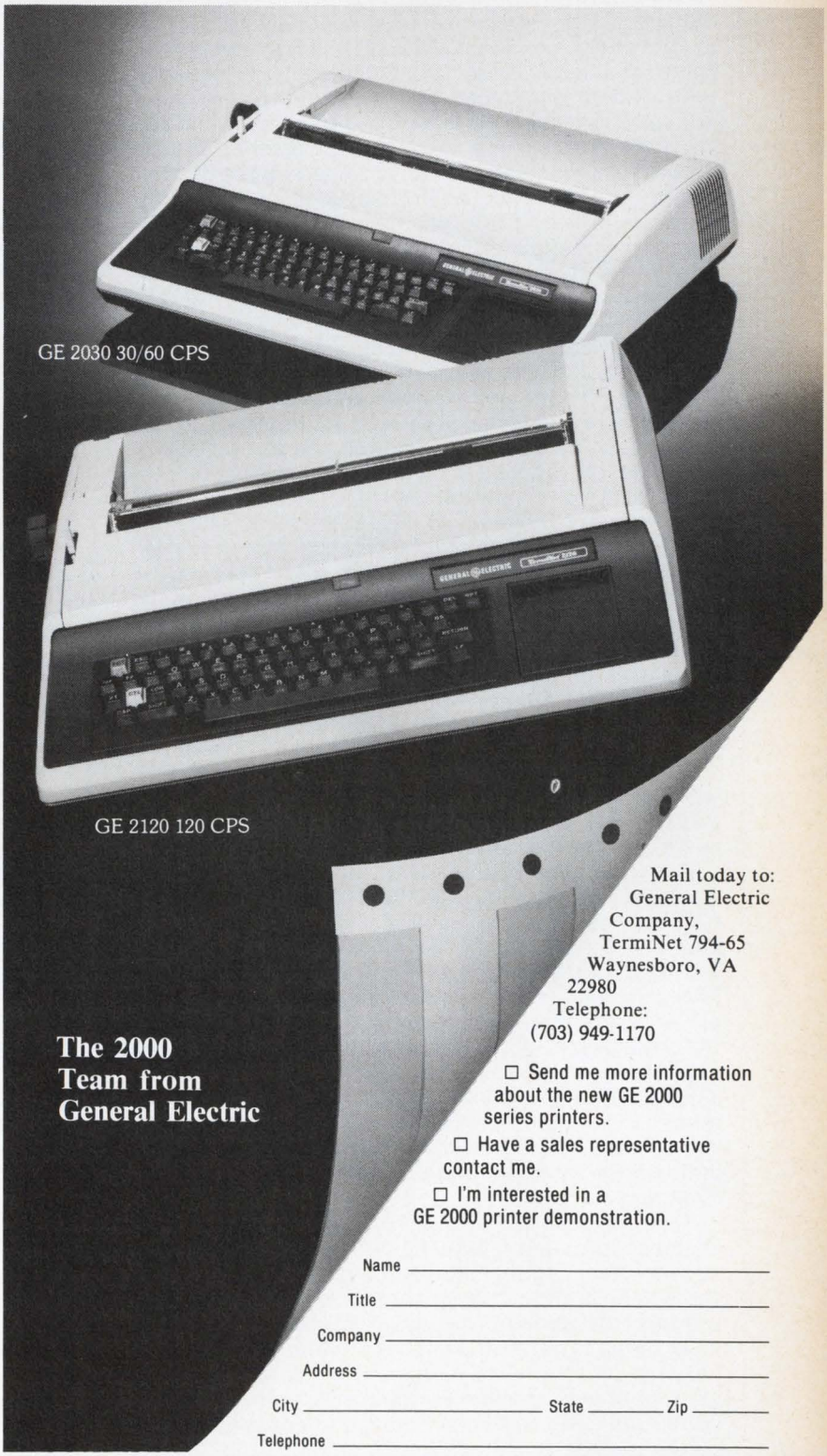

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Slave Processors Reduce Software Overhead

Designers of μP based systems which are required to control a large number of peripheral devices such as daisy wheel printers, stepper motors and seven-segment displays may often find that the speed of their system is reduced by the amount of peripheral software that the CPU is required to execute. To alleviate this problem Intel will introduce a series of slave processors which are designed to handle the detailed hardware control and interfacing and to reduce the software overhead from the host processor to a command level instruction from the CPU. Slave processors consist of two major groups of peripheral components; universal peripheral interfaces (UPIs) and functionally dedicated processors.

UPI devices are in essence user-programmable single-chip μCs with on-board ROM, RAM, CPU, timers/counters I/O ports and a slave interface to the system CPU. After the user has programmed the device to perform a specific peripheral function, the central CPU of the system is reduced to command the peripheral controller using less instructions than it would have done had it interfaced directly to the peripheral device. Thus the UPI can be used to offload detailed hardware interfacing and also reduce software overhead for the CPU. Because the UPI does not act as a bus master on the host CPU bus, contention and arbitration problems are avoided.

The second group of slave processors are functionally dedicated. This group includes components which process data sent by the host CPU for printer control, math and floating point calculations. Essentially these devices implement hardware functions that were previously done via software routines. This is designed to increase performance, reduce software overhead and free up the processor for other tasks.

Two examples of peripheral interface that will be available from Intel include the 8042/8742 UPI and the 8295 dot matrix printer controller. The 8042/8742 is an 8-bit μC with 2K words of program memory and 128 words of data memory on-chip. Two 8-bit I/O ports are available and individual port lines can function as either inputs or outputs under software control.

The 8042/8742 UPI is an extension of Intel's 8041AH/8741A UPI which has 1K x 8 program memory and 64KB of RAM. The company has chosen to extend its range of peripheral controllers so that the 8042/8742 can be used in applications such as controlling 80 column and daisy wheel printers where additional ROM, RAM and performance are needed.

The Intel 8295 dot matrix printer controller falls into the second category of a functionally dedicated processor. Providing the detailed hardware interfacing to the solenoid and motor drivers for dot matrix impact printers, the device provides an interface to the LRC 7040 series of dot matrix impact printers. The chip may be used in a serial or parallel communication mode with the host processor. Furthermore, it provides internal buffering up to 40 characters and contains a 7 x 7 matrix character generator accommodating the 64 standard ASCII characters.

Where the designer's peripheral interface circuit is required to interface via a serial link to a distant computer (for example if printer to printer interactions need to take place over long distances) a remote universal peripheral interface (RUPI) can be used. The RUPI has a similar function to the UPI except that it also features a serial communication interface. This interface is transparent to the on-chip CPU which allows additional CPU processing power for local control tasks.

To be introduced this year by Intel, the RUPI can be used as shown in *Figure 1*. On the CPU side the RUPI

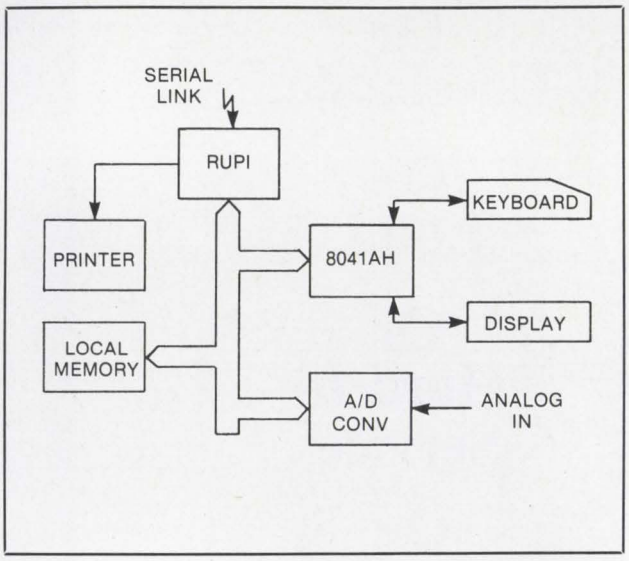


Figure 1: The remote universal peripheral interface (RUPI) permits peripherals like printers, keyboards, tape drives, or floppy disks to be placed physically separate from the master CPU.

provides a high level or synchronous data link control (HDLC/SDLC) interface. On the subsystem side it generates a local bus for standard Intel peripherals. So, in addition to controlling communications with the host CPU, the RUPI can support significant peripheral control. The RUPI implements a hardware subset of the SDLC protocol, relieving the system of acknowledgement, error checking and retransmission request duties. Information field data is delivered to the on-board RAM with no CPU overhead (auto-mode). Full SDLC (and other protocols) can be implemented with CPU intervention (non-auto-mode).

The RUPI has 4K x 8 ROM or EPROM memory, 192 x 8 RAM data memory (enough RAM to buffer communication data and hold local variables), two timers, two external interrupts, 32 I/O lines and a 1μs CPU/Boolean processor that has add/subtract/multiply/divide capabilities. The CPU can address 64K bytes of both external and data memory. —*Wilson*

case with Multibus and Q-Bus. The IEEE standard is only proposed at this point, and the choice of VME for the 68000 series may result in more changes before it is formally accepted. Obviously, Motorola and Signetics/Phillips have a vested interest in the European and World markets, but their choice of VME is not solely based on their European connectors. It looks good.

68K Gets Better Support

Early in March 1982, the 68000 μP suppliers plan to announce some significant high performance peripherals and data communication products. Motorola is planning to produce a board level, Versa Module VM-40, Video Color Graphics Controller. This 512 by 512 device will supply composite color to drive standard color monitors. Motorola claims that it will produce a resolution of 8 shades per dot.

Suppliers plan to announce high performance peripherals and data communications products.

At the same time Motorola's alternate source on the 68000, Signetics will be announcing a similar or identical color video controller that they plan to deliver early in 1983. A dual multiplexed data communications device, a hard disk controller with phase locked loops, a single channel DMA controller, and a dual UART are the other products

COMPARISON OF THE VME BUS TO OTHER 16 and 32-BIT BUSSES

	VME Bus	Multibus[1]	Q-Bus[2]	IEEE P896[3]
Bus Type	Asynchronous Non Multiplexed	Asynchronous Non Multiplexed	Asynchronous Multiplexed	Asynchronous Multiplexed
Address Width	24 Standard 32 Expanded	20 Standard 24 Expanded	16 Standard 18 Expanded	32 Standard
Data Width	8, 16, 32	8, 16	8, 16	8, 16, 32
Board Size	DBL 160x233.4 mm = 37344 mm² SGL 160x100 mm = 16000 mm² (Standard Eurocard)	171.5x304.8 mm = 52273 mm²	214x263.4 mm = 56368 mm² 214 x 147.3 mm = 31522 mm²	Any Eurocard
Connector Type	Pin & Socket	Edge	Edge	Pin & Socket
No. of Pins on Primary/Secondary Connector	96/96	86/60	38	64 or 96 on either
Power	+5, ±12, +5 Standby	+5, ±12	+5, ±12, +5 +12	+5
Interrupt Levels	7	8	4	None (uses serial bus or write into CPU card)
Arbitration Levels	4	1	1	32
Multiprocessor?	Yes	Yes	No(Master/Slave)	Yes(including System Supervisor)
Error Signals	AC Fail, System Fail, Bus Error	None	DC Power OK Power OK	ECC on bus, error result field
Special Cycles	Read/Modify/Write Block Transfer Access Privilege Lvls.	Lock	Refresh Read/Modify/Write Event Interrupt	Read/Modify/Write, Block Transfer, Split Cycle, Event Cycle
Extendable Modes For Future	Yes(Address Modifiers)	No	No	Yes(Command Field)
Separate Serial Bus	Yes	No	No	Yes

[1]Multibus is a trademark of Intel Corporation
[2]Q-Bus is a trademark of Digital Equipment Corporation
[3]IEEE P896 was previously known as "Futurebus" and is still in definition by the IEEE P896 committee-therefore, some of these features may be subject to change.

Figure 5: VME and the other popular buses show that only VME and the proposed IEEE P896 spec have expansion capabilities. Missing from this chart are a few other popular buses like Motorola's own Versabus; it, however, is very similar to the VME structure.

System Features						
Feature Description	**Signetics Chip Set**	**Motorola MC6845**	**Intel 8275-NO DMA**	**Intel 8275-DMA**	**SMC CRT5027**	**National DP8350**
Second Source	None Announced	Hitachi Rockwell Synertek	NEC UPD 3301[1]	NED UPD 3301[1]	TI Solid State Scientific	None Announced
Power Supplies Required	+5 ±12	+5 ±12	+5 ±12	+5 ±12	+5 ±12	+5 ±12
System Configuration	Line Buffer Transparent Shared RAM Independent	RAM[2]	Internal Line Buffer	Internal Line Buffer	Line Buffer or RAM	Line Buffer or RAM
Cursor Readable Writable Incrementable	 Yes Yes Yes	 Yes Yes No	 No Yes No	 No Yes No	 Yes Yes No	 No Yes No
Cursor Size Blink	Prog.	Prog.	Location Only	Location Only	Prog.	Fixed
Light Pen Register	Yes 14 Bits	Yes 14 Bits	Yes	Yes	Additional External Hardware	Additional External Hardware
Horizontal Timing Control Front Porch Width Back Porch	 Yes Yes Yes	 Yes Yes Yes	 Only Total Retrace Time[4]	 Only Total Retrace Time[4]	 Yes Yes Yes	 Mask Mask Mask
Vertical Timing Control Front Porch Width Back Porch	 Yes 3 Scan Lines Yes	 Yes 16 Scan Lines Yes	 Only Total Retrace Time[4]	 Only Total Retrace Time[4]	 Yes 3 Scan Lines Yes	 Mask Mask Mask
Composite Sync Available	Yes	No[3]	No[3]	No[3]	Yes Non-Interlace Only	Yes
Interlace	Yes 2 Modes	Yes 2 Modes	No	No	Yes	No
External DMA Required	No	No	No	Yes	No	No
Addressing Method	Linear	Linear	Row/Column	Row/Column	Row/Column	Linear
Addressing Limits	14 Bits O-16K	14 Bits O-16K	Controlled By External Circuitry	Controlled By External Circuitry	8-Column 6-Row O-8K	12 bits O-4K
Number of Displayable Characters	128 ASCII Plus 64 Graphics	128 ASCII Plus 37 Graphics	128 ASCII Plus 11 Graphics[3]	128 ASCII Plus 11 Graphics[3]	128 ASCII Graphics with External Circuits	64 ASCII

Figure 6: CRT controllers available now offer a very wide range of operating performance. The trends are for smarter CRT control with greater improvements in color graphics. Here a few of the monochrome controller offerings are compared.

Feature Description	Signetics Chip Set	Motorola MC6845	Intel 8275-NO DMA	Intel 8275-DMA	SMC CRT5027	National DP8350
Thin Graphics	Yes	No	Yes	Yes	Yes	No
Dots Per Character (Max.)	12	10	10	10	9	16
Characters Per Row	1-256	1-256	1-80	1-80	20-132	5-110 Mask
Scan Lines Per Row	1-16	1-32	1-16	1-16	1-16	1-16 Mask
Rows Per Screen	1-128	1-128	1-64	1-64	1-64	1-64 Mask
Character Rate	4MHz	2.5MHz	3.1MHz	3.1MHz	4MHz(Typ.)	2.5MHz(Typ.)
Blink Attribute	Yes	No[3]	Yes	Yes	Yes	No[3]
Reverse Video Attribute	Yes	No[3]	Yes	Yes	Yes	No[3]
Highlight Attribute	Yes	No[3]	Yes	Yes	Yes	No[3]
Blank Attribute	Yes	No[3]	No[5]	No[6]	Yes	No[3]
Underline Attribute	Yes	No[3]	Yes	Yes	Yes	No[3]
Graphics Attribute	Yes	No[3]	See Thin Graphics	See Thin Graphics	No[3]	No[3]
Processor Overhead Required for Terminal	Minimal	Minimal	Extensive	High	Minimal	Minimal
50Hz/60Hz Operation	Software	Software	Software	Software	Software	Software
Number of Keys	80[6]	64	64	64	88	90
Auto Repeat	Internal	Software	Software	Software	Software	Software
Rollover Modes	Internal 4 Modes	Software	Software	Software	Internal 2 Modes	Internal 2 Modes
Type of Key-boards Utilized	Static or Capacitive Non-Encoded	Static Non-Encoded	Static Non-Encoded	Static or Capacitive Non-Encoded	Static Non-Encoded	Static Non-Encoded
Audio Alarm	Yes	External Hardware	External Hardware	External Hardware	External Hardware	External Hardware
Split Screen Capabilities	Internal Simple Timing	No	Software	Software	No	Internal Critical Timing

Note 1: UPD 3301 is a pin for pin enhanced version.
Note 2: Bi-Phase synchronization-requires 300-350ns RAM.
Note 3: External hardware required to implement.
Note 4: For individual control-external hardware.
Note 5: General purpose attribute could supply this attribute.
Note 6: 128 if 74LS151 is used instead of 74LS159

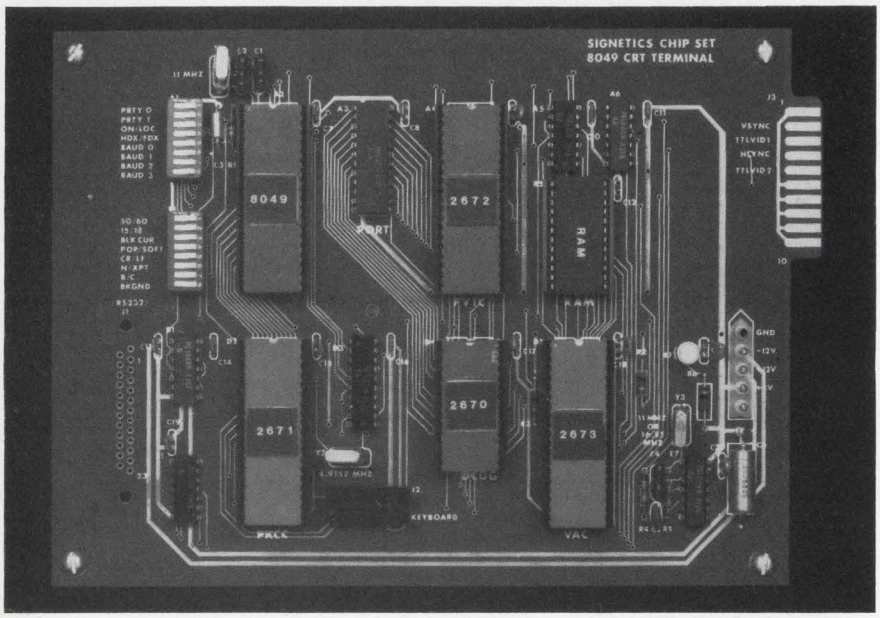


Figure 7: Four new CRT controller chips from Signetics combined with an SC 8049 μC chip produce a single board controller. With a non-encoded electromechanical or capacitive keyboard and a raster-scan CRT monitor, a low-cost smart monochrome display can be built. It will perform smooth-scroll, thin-line and block graphics, interlaced or non-interlaced operation, variable cursor, composite or separate sync, reverse video, highlight, underline, autorepeat keyboard, four rollover modes and an audio alarm.

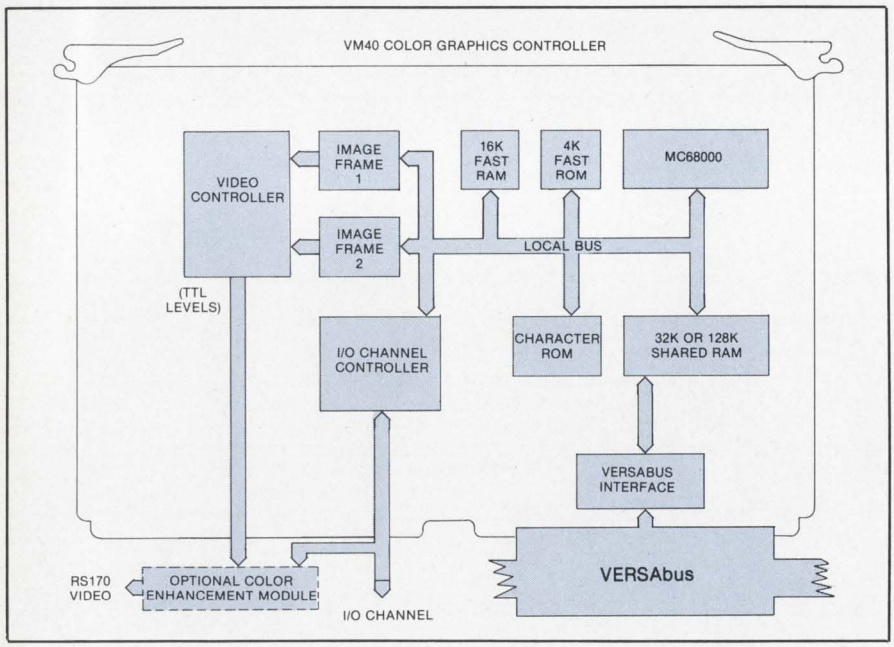


Figure 8: Using a dedicated 68000 μP this new controller VM-40 Versamodule frees the host processor of time consuming color graphics functions. It provides a screen pixel density of 512 by 512 or 512 by 384 on a standard interlaced monitor. It provides a μs pixel update rate and produces 8 basic colors with 400 shading areas. Character size is programmable and location is addressable to the pixel position. Special display algorithms and characters may be entered to shared RAM from system tasks. It also has socketed ROM/EPROM for user-tailorable display processing algorithms and character/symbol tables. This board level module should go a long way to improving color graphics.

Signetics (and most likely Mostek and Motorola) will announce.

This interesting technical exchange between Motorola, Mostek, and Signetics is the first time that three IC makers have agreed on standard devices to such an extent. It should simplify the tasks of selection and design for any users of the 68000 processor. Since the three companies claim the agreement is only at the technical level, it should keep the price and delivery end of the market operating as competitively as ever. They have moved toward standards for interconnection and now toward similar products. More technical cooperation agreements like this would help.

What You See— Isn't What You Get

At Rockwell they have developed a single chip controller with its own ROM, RAM, and timer on the chip. To a host computer this 6500/41 chip looks like a peripheral interface adapter, but it can control a wide range of peripherals. It has three 8-bit I/O ports and one 7-bit port. A 16-bit center timer, 64-bits of RAM and 1.5K bits of programmable ROM reside on the chips. It acts as a host interface for the 6500/6800/68000 μPs with a synchronous mode bus. With software control and swing timing it can also be made to work with the 8080 or the Z80 bus. Several other variations of this device are available with different I/O ports and varying amounts of on chip memory.

A new floppy controller, Rockwell's 6565, works with double sided minis or 8-inch floppy disks. Up to 3 disk drives can be controlled and interfaced to 6500/6800/68000 bus lines. Available late in 1982, this floppy controller also offers a mask programmable section of 1, 2, or 3 bus lines. It too can be made to interface with the 8080.

In its 6500 series, Rockwell is also offering an actuator motor control device for floppy drive head acceleration algorithms. It is a ROM code programmable device that has a wide range of motor control applications, from floppies to sewing machines. Rockwell is developing

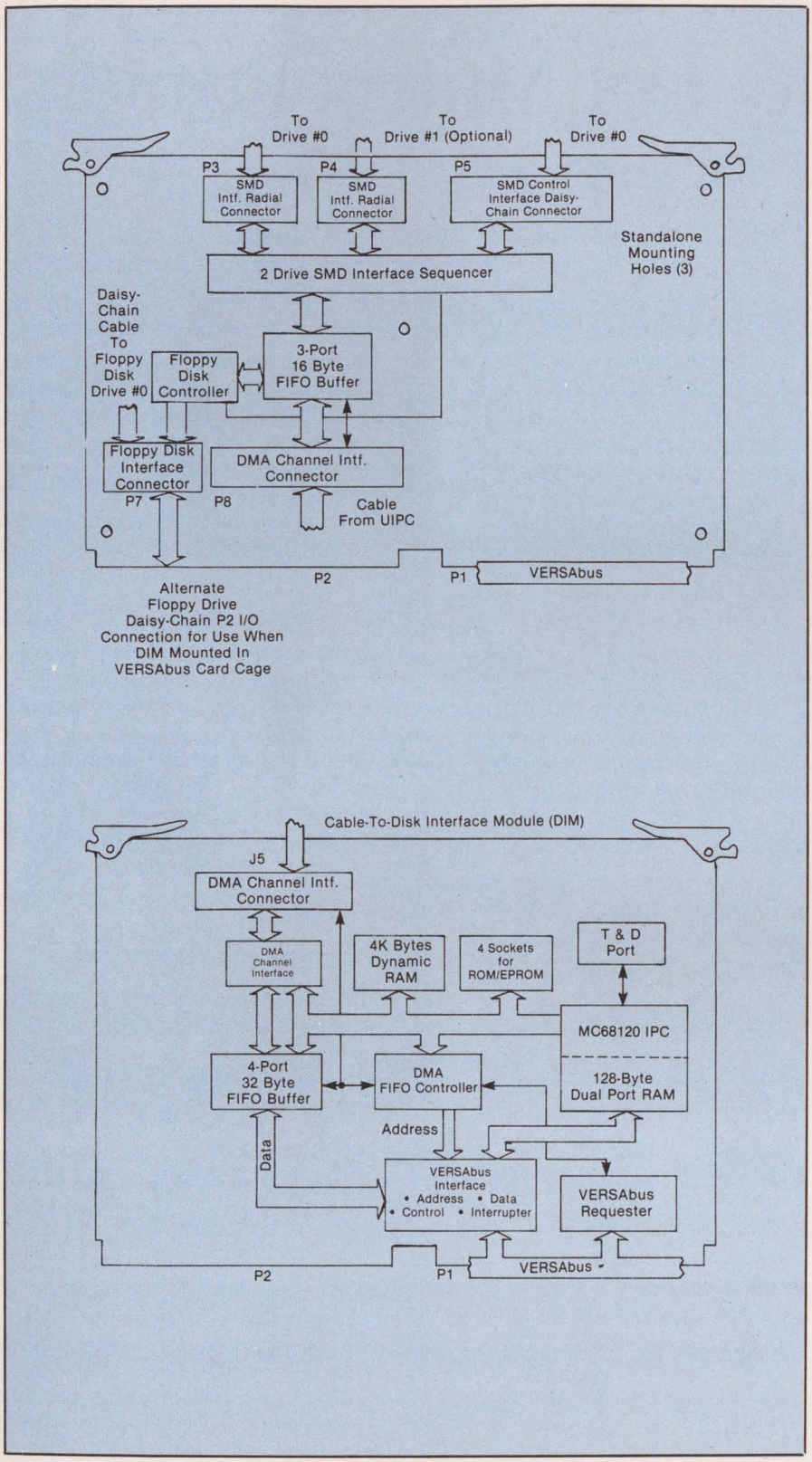


Figure 9: For disk control, Motorola offers several options in its Versa module line. The most interesting is the two-board VM 21 Universal disk controller and interface module. It provides SMD interface for 14 currently qualified drive types, including storage, cartridge, mini and lark module types of drives. Motorola also produces a VM 20 floppy controller board capable of interfacing up to 4 double-sided or single density floppy drives.

some interesting products, most of which are also compatible with the 68K processor. For a long time Rockwell has concentrated on custom and semi-custom business, but they now appear ready to serve more general purpose applications — perhaps with some unique offerings.

CRT Controllers Getting Better

This year should see the introduction of several significant advances in CRT controllers. In general they will get smarter and will be able to do more interesting things in color. Products now available come mainly from National, SMC, Intel, Motorola, Rockwell, Signetucs, TI, and Japan. **Figure 6** attempts to compare the current offerings, but it is not complete.

The new CRT color controllers should add another dimension to graphics display, and these are the devices that should be watched very carefully as they are introduced.

Controller Trade-Offs

Like any design problem, peripheral control is loaded with tradeoffs. If you are using a specific type of μP your choices are limited to what that system is capable of accepting. There are many moves towards more universal chips and boards, but the processor and its bus structure dictate most of the constraints.

With micro control of peripherals and a larger computer system, the options now becoming available will make the flexibility of both the peripherals and the controllers much better.

This recession may have produced some real advances in control devices. As the recession appears to fade (we hope!) the product introductions are beginning. 1982 should be a year that sees major advances in products and some real movement to standardization of interfaces. In this article, we have shown some of the latest peripheral control devices; many have no doubt been overlooked, but we hope to report, in future articles, on every new type of controller device or board as it is introduced. □

Letter Quality Dot Matrix Printers

Dot matrix printers with the ability to print letter quality characters pose a threat to the daisywheel market. Although they still don't have the exact character representation of fully formed character printers, many of the dot matrix printers in this Showcase come very close.

The current technology for letter quality dot matrix printing is accomplished by a multipass technique. This combines incremental vertical motion of the paper with multiple passes (commonly 2 to 4) of the printhead over the print line, interleaving a dot pattern to create solid print characters. Other methods to increase the character quality are double-density printing and proportional spacing.

A problem with the multipass method is that when you pass over a line several times, print speed may be reduced to that of a daisywheel, thereby producing a character at the same speed with slightly lesser quality. However, dot matrix technology offers several advantages that fully formed character printers cannot. These include: flexibility of character size plus graphics to provide output of any size or shape (characters, labels, graphs, charts, or other images which can be generated from a computer on a CRT); electronically changeable character fonts which eliminates changing of print elements such as bands or print wheels; and the ability to print at much higher speeds for applications where letter quality is not required.

"Quality" is a relative term that differs according to personal preference. Just as when judging works of art, preference often comes down to "I know what I like" — so it applies to "letter quality." The units described in this Showcase have applications requiring: (near) letter quality, correspondence quality and word processing output. Many of them produce copy so close to fully formed character units that it's hard to tell the difference; again, it's a personal judgement.

For this Showcase we tried to limit our selections to models providing output for word processing and business applications, and for the most part omitted units whose main purpose is to provide graphics output or plotting capabilities. Many more units are available that produce "good" or "high resolution" characters. Descriptions of these can be found each month in the New Products section of *Digital Design*.

VARIETY OF FONTS

The GP300 is an 18 needle (9 X 9 interlaced) dot matrix printer designed to bridge the gap between dot matrix and daisywheel printers required in office workstation requirements. It is capable of printing a variety of fonts under electronic control and has a full set of options available. Specs include: 132 char/line at 12 cpi; up to 7 fonts available in ROM or RAM addressable; RS-232C compatible; platen or tractor feed, front feed and single sheet handler available. Advantages include complete control by computer command, high quality printing, fast speed and paper handling options. The unit can also reproduce letterhead quality company logos, charts and fixed graphics; and, will also produce optical wand readable bar codes, OCR-A and OCR-B characters. Centronics parallel interface is available. $3165 OEM; $2685, 100 qty. **Amperex Electronic Corp,** 230 Duffy Ave, Hicksville, NY 11802.

Write 300

FLEXIBLE PAPER HANDLING

The WP6000 utilizes an 18 wire, continuous duty print head coupled with a high speed, bidirectional logic seeking, multiple μP controlled servo system. It prints in the correspondence mode at 150 cps and at 500 cps in data processing mode. Multiple resident character fonts as well as optional downloading of other fonts from a host computer are provided along with proportional spacing and text justification. Paper handling includes both bottom and rear loading of continuous roll or fan fold stock up to 15.6″ wide using friction or optional tractor feed systems. In addition, top loading of single sheets may be done manually or an automatic single or dual sheet feeder may be added. Complete forms control and programmable vertical and horizontal tabs are included. Other features include high density graphics and parallel plus serial RS-232C interfaces. The WP6000 is $2895. **Anadex Inc,** 9825 De Soto Ave, Chatsworth, CA 91311.

Write 301

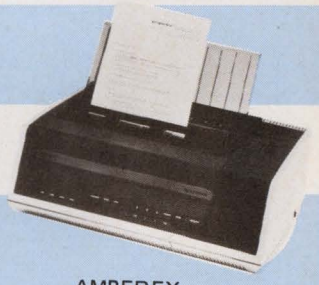
Letter quality dot matrix printers pose a threat to the daisywheel market.

LETTER QUALITY CONVERSION BOARD

Letter quality print can now be generated on the TI 810 RO printer equipped with the Graphics 810, Model 190-L plug-in conversion board and a substitute high-resolution paper advance motor. The 190-L allows the user to select between 6 typefaces, including 3 letter-quality fonts, which can be combined within the same line. The paper advance motor (shipped with the board) provides the dot addressibility of 240 X 288 dots/in. Text centering or justification, font and pitch selection are performed by simple escape command sequences. Proportional spacing is either automatic or WP controllable. The 190-L makes the TI 810 a multi-mode printer with high-speed draft copy capability, selectable letter quality fonts, a 95 character software font, a high speed plotting mode, commandable expansion and printing of barcode and block characters. A 3000 character print buffer and X-on, X-off protocol facilitate its use on many systems. (For information on the TI 810 printer contact Texas Instruments, Houston, TX.) **Analog Technology Corp**, 15859 E. Edna Place, Irwindale, CA 91706. **Write 302**

FULL FORMS HANDLING CAPABILITY

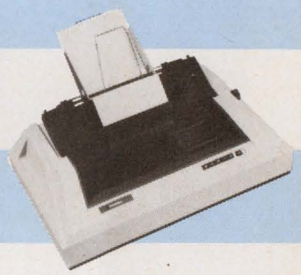
The Printstation 350 Series offers all the functions required to perform the varied applications within the office environment, in a single unit. Standard features include paper handling flexibility to accommodate cut-sheet, fan-fold and immediate tear-off forms. Its modular design incorporates fewer moving parts with an operator replaceable print head and a 10 million character ribbon cartridge. Eight resident character sets are included along with 110 or 220V operation for international usage together with switchable serial/parallel interfaces. Additional standard features include pin-addressable graphics, 200 cps print speed for data processing, 50 cps for correspondence quality printing, self-test/diagnostics and bidirectional logic seeking. Model 353 additionally includes an operator-programmable control panel for feature selection and the capability of accepting a user defined character set via the host computer. The Printstation 353 is $2495 (single unit end-user); OEM discounts available. **Centronics Data Computer Corp**, Hudson, NH 03051. **Write 303**



AMPEREX

NEWLY DEVELOPED PRINTHEAD

The bidirectional logic-seeking M-100 matrix printer provides 140 cps performance using a 9 X 9 matrix representation of all alphanumeric characters. With the newly developed vertical column 14-wire printhead, the unit produces high resolution output, combined with raster graphics capability as an option, for applications ranging from business to word processing systems. Specs include: 56 1pm at 132 char/line and 86 1pm at 80 char/line throughput; 10 ips paper slew speed; 128 character set (96 ASCII plus 32 commonly used international characters); printing format of 132 columns, 6 1pi (std.), 6 or 8 1pi (opt.); character spacing of 10 and 5 cpi (std.), 16.7 cpi (opt.); and plotting format option with dot density 70H X 84V, 1320 dots/raster maximum. Interfaces include Dataproducts parallel, serial (RS-232, 20 mA current loop), Centronics compatible. Options include programmable character generator, graphics, block letters, bar codes, proportional spacing, condensed print (16.7 cpi), tape-controlled vertical format unit. The newly developed printhead provides true descenders for all lower case letters, as well as real subscripts and superscripts for scientific notation, and true underlining at any position in the output. The unit can also print solid black areas. The M-100 is $2700; under $2000 in OEM qty 100. **Dataproducts Corp**, 6200 Canoga Ave, PO Box 746, Woodland Hills, CA 91365. **Write 304**



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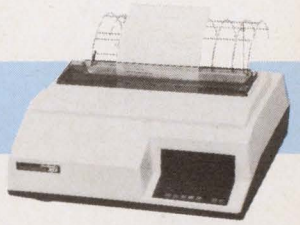

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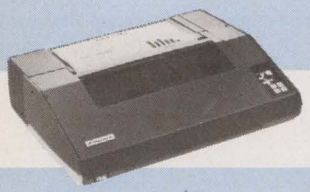
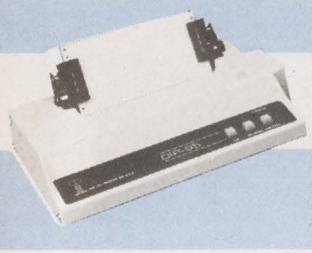
5983 Macon Cove at Interstate 40
Memphis, Tennessee 38134



DATAPRODUCTS

SWITCH-SELECTABLE DUAL-MODE

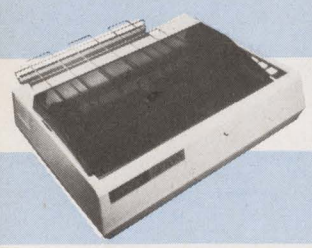
The DIP-95 has two basic switch-selectable printing modes. The DP mode uses a 9 X 9 matrix font, and the correspondence mode uses an 11 X 9 font. Under program control the user can specify 6 different character sizes and one or two pass printing. Features include bidirectional printing, both tractor and friction paper feed, continuous-loop ribbon cartridge, variable line density and continuous form length control. Its high resolution dot addressable graphic capability can provide plotting, printing CRT screen graphics, drawing illustrations and special effect symbols. Telecommunications capability include standard baud rate up to 9600, parallel and serial RS-232C transmission control, as well as X-on/X-off, and standard 1K FIFO character buffer or an optional 2K buffer. With a full 96 character ASCII set, the unit is capable of both upper and lower case printing at 40, 48, 66, 80, 96 or 132 char/line on 8-½" wide paper. Paper feed is at 5 1ps. The DIP-95 is $929; $625 in OEM qty 100. **DIP Inc**, 745 Atlantic Ave, Boston, MA 02111. **Write 305**



DIP

VARIETY OF PRINTING STYLES

The MX-80F/T is a dual mode (draft/correspondence quality) printer featuring dozens of type styles and plotter-like bit image graphics as standard. It offers both tractor and friction feed allowing printing on almost any type of paper. The unit prints a full set of characters at 80 cps, bidirectional, and incorporates a logical seeking function. A user-defined choice of 40, 80, 66 or 132 columns is provided in a total of 12 distinct printing character modes including 5, 8.25, 10 and 16.5 cpi in standard, double printing and emphasized printing. Other features include: full 96-character ASCII with descenders; 64 block characters; printing sizes of normal, normal expanded, compressed, compressed expanded; single sheet, roll or fan-fold paper handling; self-test mode; disposable print head; and full forms handling. Interfaces include Centronics-style 8-bit parallel; optional RS-232, IEEE488. The MX-80F/T is $745; qty pricing avail. **Epson America Inc**, 3415 Kashiwa St, Torrance, CA 90505. **Write 306**



EPSON AMERICA

PROPORTIONAL SPACE PRINTING

The 4542 Flex Hammer printer features an extensive character repertoire as standard and can also print pictures, staple diagrams, large size characters, curves, etc. For letter quality printout, a proportional space printing version is available. Different printing modes such as grey scale and scanning are software controlled by means of escape sequences. Speed is 260 cps at 10 cpi, up to 535 cps in proportional spacing mode. Other features include: black or red printing; noise below 65 dB; bidirectional; bar code, variable size characters as well as normal and proportional print graphic charts; elongated characters; underlining; high speed tabulation and carriage return; justified right margin; and internal self-test. Interface includes RS-232C, IEEE488, and Centronics. $5000. **Facit Inc**, 66 Field Point Rd, Greenwich, CT 06830. **Write 307**

THREE PAPER HANDLING MODES

The OSP 120 and 130 offer a Triple Paper Path that provides automatic cut sheet feed, hand feed and multi-part form tractor feed in one mechanism. For DP applications, print speed is 600 cps; correspondence quality printing is 150 cps; and, WP high resolution letter quality print speed is 100 cps. Self-test and diagnostic display are included. The units have three printing methods: fonts stored in the printer, downline load fonts, and graphics. Specs include: up to 6-part forms; programmable horizontal pitch; incremental horizontal character positioning; vertical and horizontal tabbing; internal diagnostics; and serial RS-232 interface, Diablo 1650 or 630 software compatible. Among the options are: expanded font memory, downline load font capability, Centronics parallel interface and graphics. The OSP 130 is $4100; $2600 in 100 qty. **Florida Data Corp**, 600 D John Rodes Blvd, Melbourne, FL 32935. **Write 308**

LOW-NOISE PERFORMANCE

For office environments, the Infoscribe 1000 has a noise level of 54 dbA. Speed is up to 200 cps (100 cps correspondence quality) and up to 136 column output with no duty cycle limitations. High throughput is achieved with high-speed paper movement with vertical tabbing, plus bidirectional printing with logic seeking in both directions. DP quality printing is produced at 10, 12, or 16.5 cpi; correspondence quality characters or

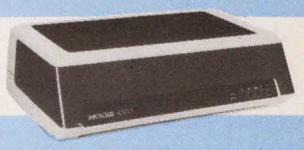
double-density printing at 10 cpi. Double-wide printing, as well as subscripts and superscripts, may be produced in any selected pitch. In graphics mode resolution is 72 X 72 dots/in. The printer stores a standard ASCII 96 character set in ROM together with an alternate character set. An additional character set may be downloaded from the host CPU into an expanded buffer. Options include programmable character set, 3K input buffer, special character sets, and auxiliary control panel. The Infoscribe 1000 is $1825. **Infoscribe Inc,** 2720 S. Croddy Way, Santa Ana, CA 92704. **Write 309**

MODULAR CAPABILITY

The Prism Series are modular, field-upgradable units with add-on options that allow configuration to a wide range of applications. The basic 80 column version yields correspondence quality print in an overlapping 24 X 9 dot matrix. Printing bidirectionally at up to 150 cps for proportionally spaced characters, Prism allows for character densities of 10, 12 or 16.8 cpi, plus double-width characters. Standard features include: enhanced (bold) text printing; automatic text justification; programmable horizontal and vertical tabbing; reverse paper feed; character positioning of 1/120th of an inch; ASCII U/L case 96 character set; and up to 4 different 96 character sets residing within the printer. The unit has true logic seeking lookahead capability, a high-speed slew, and RS-232C serial interface as well as Centronics-compatible parallel interface. Serial transmission rates from 300 to 9600 baud are switch selectable. An important option is Prism Color, a color-printing capability for graphics and text. Other optims include automatic cut sheet feeder. Dot Plot graphics for raster graphics from CRT screens, and Sprint Mode for high-speed output in excess of 200 cps. The Prism 80 (80 column) is $899. **Integral Data Systems Inc.,** Milford, NH 03055. **Write 310**

15.5″ PAPER WIDTHS

The Pro/Writer II accommodates up to 15-½″ paper widths with up to 231 columns. A 9 X N matrix produces consistent correspondence quality printing. The unit has a 120 cps print speed with logic seeking, bidirectional and quick-cancel printing. Five alphabets with 8 character sizes (two proportionately spaced) are available along with a high resolution graphics mode. Other features include incremental printing to allow intermixed fonts on one line, variable form length, 6-channel electronic VFU, automatic vertical and horizontal tabbing, built-in bidirectional tractor and roll feed, and 3 kB buffer. Industry standard parallel or serial (RS-232C) interfacing includes X/On, X/Off protocols. Under $1000; OEM qty discounts available. **C. Itoh Electronics Inc,** 5301 Beethoven St, Los Angeles, CA 90066. **Write 311**



INFOSCRIBE

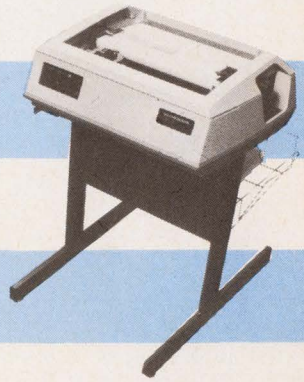
MULTI-FONT CAPABILITY

The Dual-Mode 200 features multi-font capability for both WP and DP quality output as well as high resolution graphics. Tractor feed and friction feed provide universal forms handling. DP speeds range from 165 to 250 cps; letter mode speeds range from 42 to 70 cps. Over 25 different fonts are available including italics, proportionally spaced, OCR-A, APL, bar code, greek/math and foreign. Up to 6 font selections may be stored in ROM and interchanged while printing. Specs include: 1 user defined font in RAM; graphics resolution of 60H X 72V and 120H X 144V; 512 byte buffer; 15″ carriage; front, bottom and top paper loading; programmable format control; daisywheel control code compatible (Qume and Diablo); bidirectional, logic seeking; lower case with descenders; underlining; expanded characters; downloadable character sets; horizontal and vertical tabs; RS-232C serial and Centronics parallel interface; and optional buffer expansion to 6.5K RAM. The Dual-Mode 200 is $2995; $1995 in 100 qty. **Malibu Electronics Corp,** 2301 Townsgate Rd, Westlake Village, CA 91361. **Write 312**

MALIBU ELECTRONICS

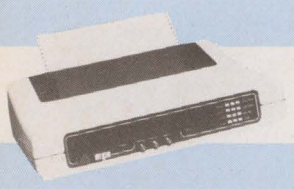
HIGH DENSITY CHARACTER MATRIX

The MT 1800 has a high density character matrix for 50 cps quality correspondence printing. Under command it uses a conventional matrix for DP printing at 200 cps. Specs include: bidirectional, logic seeking; accelerated head slew at 480 cps over blanks; 132 column; double width characters; operator replaceable printhead; 6 or 8 lpi vertical spacing; 96 character ASCII plus 6 foreign sequences; forms length select switch; 2



MANNESMANN TALLY

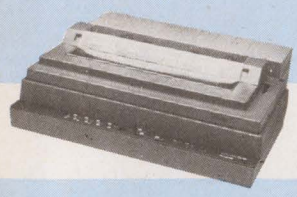
channel VFU; 53 dbA noise level; cartridge ribbon; and upper and lower tractors. Centronics or RS-232 interfaces are standard, with optional Dataproducts, IEEE 488 or current loop. Available options include short form quick tear, automatic front feed device, bottom forms load and universal power supply. The MT 1800 is $1995. **Mannesmann Tally Corp**, 8301 S. 180th St, Kent, WA 98031. **Write 313**



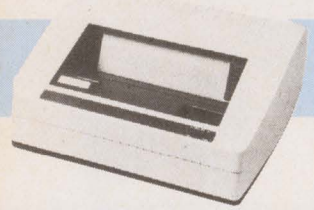
MPI

WIDE CARRIAGE PRINTER

The MP150G has a bidirectional, logic seeking, 150 cps printhead that is rated for continuous duty with an expected lifetime of over 100 million characters. Other characteristics include descenders and underlining, 136 char/line at 10 cpi, or up to 226 columns by selecting 12 or 17 cpi density. Double wide characters can be software selected in any of the character densities for a total of 6 different cpi densities. A 7 X 9 matrix font is used for high speed data printing, an 11 X 9 serif style font is used for high quality correspondence printout. A standard 96 character USASCII set with 4 strap selectable foreign fonts are standard. Special fonts may be downline loaded into RAM or permanently located in ROM. Dot addressable graphics capability is included for plotting, printing of screen graphics, drawing illustrations and producing special characters; 4 horizontal dot densities are selectable. A tractor paper feed accepts forms from 3″ to 15″. Specs include: 8 selectable form lengths, and skipover-perforation; horizontal tabbing; 10 channel VFU; 1K buffer expandable to 8K; and Centronics type interface. An optional RS-232C serial interface accepts data at any of 7 strappable baud rates up to 9600 and supports both X-ON/X-OFF and ETX/STX protocols. An IEEE-488 bus interface is also optional. The MP 150 is $1095; OEM qty discounts are available. **MPI**, 4426 S. Century Dr, Salt Lake City, UT 84107. **Write 314**



OLIVETTI



PRINTRONIX

SHORT-LINE SEEKING LOGIC

The Microline 84 prints bidirectional at 200 cps and features short-line seeking logic to maximize throughput. It also prints charts, illustrations, forms and graphs in addition to text on 16″ wide forms or paper. A standard Dot-Addressable Graphics package enables the ML 84 to reproduce what has been displayed on a CRT screen. Its 9-pin stored energy print head has a life expectancy of 200 million characters. Correspondence-quality printing is possible in the enhanced and emphasized print modes. Six program selectable character sizes are built into the printer which has 224 column print capability in the condensed character mode. Other specs include tractor and friction feeds; parallel Centronics-compatible or RS232 interfaces, IEEE 488-compatible interface optional; U/L case characters with descenders plus underlining; condensed printing; full 96 character ASCII; double-width characters and block graphics; print buffers; and no duty cycle limitations. **Okidata Corp**, 111 Gaither Dr, Mt. Laurel, NJ 08054. **Write 315**

TWO BIDIRECTIONAL PRINTING MODES

The DM 80/180 prints 16 X 32 letter quality characters at up to 80 cps in a single pass. In the conventional mode, 8 X 7 dot matrix characters are printed at 180 cps. The printer has all the capabilities of a standard word processing printer such as proportional spacing and automatic sheet feeding, and also features a 2 digit display for a full range of self-diagnostics. The unit is μP controlled for bidirectional print with shortest path seeking and high speed skip over blank fields. A wide range of fonts are available in 94 printable characters. By an optional expandable memory, the user can create his own character fonts. Interface is RS-232C/CCITT V24 serial interface or current loop. Four methods of tabulation are possible: normal horizontal tab, addressed horizontal tab to any print position, high resolution horizontal skip and relative horizontal tab. Line spacing characteristics include vertical spacing definition of 1/264″, choice of 3 line spacing standards available to define intrinsic vertical pitch, 5 selectable multipliers of the intrinsic pitch (set manually or automatically by the host), automatically controllable forward and reverse half-line space, and high plotting capability. Print modes include normal, underlined and elongated character. The DM 80/180 is $3470; $1760 in 500 qty. **Olivetti OPE**, 505 White Plains Rd, Tarrytown, NY 10591. **Write 316**

OPERATOR- AND COMPUTER-SELECTABLE MODES/SPEEDS

The Taskmaster/MVP is suited to small business/multi-task operations, distributed data networks, and heavy-duty industrial uses. Lightweight and office-quiet, it provides single-unit versatility for high quality alphanumeric printing, data representation graphics, OCR and bar codes, and multi-part forms. Printing speeds can be computer- or operator-selected at 80 lpm for graphics and correspondence quality, at 150 lpm for DP output, or at 200 lpm for compressed printing. The MVP features internal diagnostics, test pattern printout and programmable configuration. Specs include: vertical format of 6 or 8 lpi; 96 ASCII character set; upper case font matrix; lower case with descenders; plot mode density of 100 X 100 dots/in (80 lpm), 60 X 75 dots/in (150 lpm), 50 X 50 dots/in (200 lpm); double high characters plus underlining; adjustable tractor paper feed; full forms controls; and Centronics interface. Options include RS-232C/Current loop, Dataproducts, high-speed parallel interfaces; expanded, custom character sets; memory expansion; and downline loadable font. The MVP is $3995; qty discounts available. **Printronix Inc**, 17421 Derian Ave, PO Box 19559, Irvine, CA 92713. **Write 317**

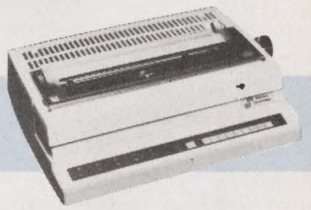
FOUR MODES OF OPERATION

The 7030 includes advanced design to allow operation in 4 different modes and perform functions previously associated with a word processor, such as right hand justification and proportional spacing. The unit incorporates a machine reporting function to allow an operator to determine the operating parameters of the printing system. Speeds are 180 cps for draft copy, 150 cps for compose copy, 75 cps for memo quality, and 37 cps for letter quality. All fonts have ASCII versions as well as 7 European versions resident. Fonts include Trend, APL, Emphasis, General Scientific, Cubic, Script, OCR-A, Courier and Italics. Graphics resolution is 72 and 144 dots/in vertical, and 144 dots/in horizontal. Other features include: bold and in-line over-printing; optional non-volatile (EAROM) escape code buffer; serial and parallel interfaces; up to 19,200 baud, odd, even or no parity; tractor feed standard; settable tabs and margins; and, variable line spacing. The 7030 is $1900; $1350 in quantity. **Qantex Div**, North Atlantic Industries Inc, 60 Plant Ave, Hauppauge, NY 11788. **Write 318**

INFINITE MATRIX

The S700 prints at 32 to 58 cps in letter quality mode that is comparable to daisywheel printing; at 65 to 195 cps in correspondence quality mode; and at 130 to 390 cps for draft quality. It contains one font pack with two fonts, usually a draft and a letter quality font. Five additional packs for a total of 12 fonts may be optionally inserted. Over 100 different fonts are available including domestic and most foreign alphabets, proportionally spaced character sets, special graphics and a user defined font. Commands inserted in the text to be printed and executed by the printer (rather than the host) give the user total control over the layout: top, bottom, left and right margins, line lengths and spacing, identing, tab settings and justification, centering, bolding, underlining and automatic switching between character sets, typestyles, speeds and quality level. Specs include: printhead with average life of over 500 million characters; fonts available for 6, 8, 10, 12, 15, 16.5, and 18 cpi; 6 and 8 lpi; cut sheet, fan fold or continuous roll of plain paper up to 14.7″ wide; 2048 byte input data buffer; tractor feed, single bin cut sheet feeder and dual bin cut sheet feeder; and, RS-232C serial, Centronics-type parallel, Diablo, Qume and custom designed interfaces. **Sanders Technology**, Box 1226, Nashua, NH 03061. **Write 319**

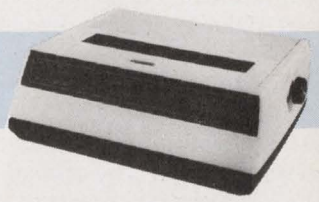
QANTEX



SANDERS

IBM COMPATIBLE

The 287D attaches to Telex's 276 Control Unit or IBM's 3274/3276 Cluster Controller as well as to the IBM 4331/4341 Processors. The bidirectional unit prints at 150 cps with an optional operator selectable high resolution print feature providing near letter quality printing at 75 cps. Printout is at 10 cpi with 6 or 8 lpi spacing. Features include choice of ASCII-B or EBCDIC character sets, U/L case, underscore and Serial Character String operations under SNA/SDLC. Character buffers of 960 and 1920 are standard; 2560, 3440 and 3564 buffers are optional. The unit has a friction platen, with bottom and top forms feeding. An optional pinfeed and forms tractor allow the use of perforated forms in widths from 3 to 15″. The 287D is $5150. **Telex Computer Products Inc**, 6422 E. 41st St, Tulsa, OK 74135. **Write 320**



TELEX

Floppy Disks Vs. Winchesters: The Battle Looms

by Paul Snigier

Small and removeable Winchesters and alternative forms of backup threaten the future of floppy disks.

Technology and competition in floppy disks are changing. Since its beginning in 1973, the OEM floppy disk industry has been characterized by small startup companies getting a foothold and then selling out to larger firms. Recently, however, the new entrants have been primarily foreign firms penetrating the American market in a variety of ways.

Many industry participants anticipate a "squeeze" in the low end of the OEM floppy market. This projected squeeze will be due to increased competition from foreign competitors, combined with a tendency toward backward integration into captive production by customers with large-unit requirements.

But competitive and technological changes are now coming from new developments that threaten the very floppy disk drive itself. Shortly, these changes will drastically alter the ballgame. Some industry observers even suggest that upcoming developments could foreshadow the decline and even demise of the floppy disk. These developments are the emergence of the 3.25" Winchester, removeable Winchesters, new and reliable storage backup, standardization, simplicity of use and growing ease of integration. Dramatic Winchester capacity growth continues unabated. These developments have already frozen the floppy disk from upward growth. The very inherent qualities of the floppy disk drive, as dictated by the laws of physics, seal its fate.

But some floppy fans prognosticate that the (so-called) 3" floppy, as pioneered by Sony, Maxell and others, will do well in desktop computers, small business and personal computers and word processors — once upcoming second-generation 3" floppies increase capacities. In any event, the floppy is becoming a mature product and technology. This niche could be the floppy's last pocket of resistance.

The tumultuous changes in the technology jungle, of course, extend well beyond floppies to Winchesters, where we've already seen: the 8" Winchester stumble (and not merely due to poor standardization) against the 5.25" Winchester; rapid errosion of the low end of the 14" Winchester; the yet-to-materialize but very definite upcoming threat of R/W optical disks; and other drastic changes. The death of the floppy disk drive is a certainty; the question is not one of how or why, but one of when and how suddenly.

In the short-term, however, floppy makers are not alarmed; although floppy disk drives will begin to be displaced from some applications by newer technologies with superior price/performance — in particular low-cost hard disks — erosion in floppies' functional market share will be more than offset by expanded production of μP-based systems until 1984. After that, it's downhill for the floppy disk drive.

Selection Criteria

What should you look for in selecting floppy disk drive systems? We've covered these criteria exhaustively in previous articles but, basically, it boils down to the following.

First, decide if you want to buy a complete system with drive, interfacing and control electronics. If so, your work is easy: you will connect the units directly to a micro or terminal via an RS-232C or 20mA current loop connector. However,

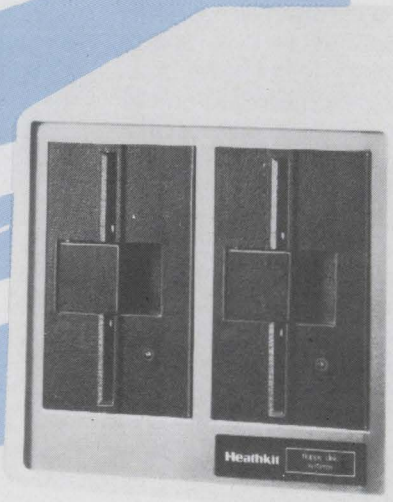


Figure 1: The 5.25" diskettes, such as this Heath H-37, 640-kB / diskette floppy system, have found increased use in small business computer OEM designs.

Figure 2: With second-generation, larger-capacity 3" diskettes, many word processors and desktop/personal business computers (such as this IBM unit) will switch from the 5.25" floppy disk drives.

should you (as a large OEM) buy mechanical drive and R/W heads alone, you may wind up providing the electronics; and if you're a large OEM, you will most likely buy drives with on-board electronics to control head movement, stop and start disk contact, and raise the 1mV R/W head's signal to 5V.

Second, decide on the disk type. Do you want an 8" or 5.25" disk? As a rule of thumb, minifloppy systems only offer 40% of standard-size floppy useable data storage (but at 70% of the price) and take up a lot less space.

Third, determine your memory capacity needs, differentiating between useable and absolute storage. For example, although a typical single-sided single-density 8" floppy stores 400 Kbytes, a portion is used for formatting or memory organization.

Specifically, look for these factors in your evaluation: capacity, cost/bit, environmental needs, future system needs, warranty (from shipping or installation date?), reliability and maintainability, service (on site? local service center? spare parts?), data transfer rate, interface, physical size, multiple vendors and training (on site?).

With this behind us, let's look at a sampling of some newly introduced floppy disk drives. This sampling does not constitute an endorsement of the products listed; rather, it offers you a starting point. Although we obviously don't suggest that you rely primarily or solely upon this or any other listing published in any magazine (brevity precludes comprehensiveness), we do strongly recommend that you obtain product coverage manuals and directories from Datapro (Delran, NJ), GML (Framingham, MA) and the many other excellent organizations that specialize in gathering and publishing such data. This should begin your search, even then, and not constitute it.

The **ACS8000-6** is a mag tape floppy system combining hard and flexible disk storage with a magnetic tape backup unit (MTU). The system includes a Data Electronics ¼" "Funnel" cartridge tape drive, with Shugart 8" floppy and 14" Winchester hard disk drives. It supports 1-4 users simultaneously. The MTU includes a 450 ft. tape cartridge with 17MB of storage capacity. R/W is performed on 4 tracks at 30 ips. The drive searches at 90 ips in either direction and packing density is 6400 bpi. The ACS8000-6 is $12,650; OEM discounts available; delivery 90 days ARO. **Altos Computer Systems,** 2360 Bering Dr., San Jose, CA 95131.

A new series of mini-floppy drives are compact mechanical-only versions of the 6106/6108 disk drives. **Model 6107** is a single-headed version; the **6109**, a doublehead mechanical drive. With dimensions of 2.1" x 5.75" x 7.5" these units occupy ⅓ less space than other available drives. For full compatibility, they are also offered with an optional "industry-standard" sized (3.75" high) front panel, allowing mechanical interchangeability in existing systems. Optional software-controllable door interlock and sensors and connectors permit system customization and versatility. **BASF Systems Corp**, Crosby Dr., Bedford, MA 01730.

A dual-sided, double-density floppy disk subsystem for the Scout Naked Mini 4/04 computers, has a formatted-data capacity of 1 MB per drive. Full software support includes the 10S4 driver, ISOLITE (self-test) diagnostic and autoload diagnostic formatter. The subsystem includes a universal floppy disk controller, a single Scout board that interfaces with the Scout I/O bus, rack-mountable chassis with power supply, and cables. Diagnostic/formatter software enables the user to format diskettes with sequential sectoring for both single and double density. $3950. **Computer Automation, Inc.**, 2181 Dupont Dr., Irvine, CA 92713.

A double-sided, double-density diskette drive for Data-point 1800 dispersed processors can store over 2 MB of data. Four dual drive units can be configured with an 1800 for over 8 MB of storage. **The 1413** includes a dual diskette drive with internal controller. A 256 byte buffer in the diskette controller is randomly accessible by the processor and provides access to stored data.

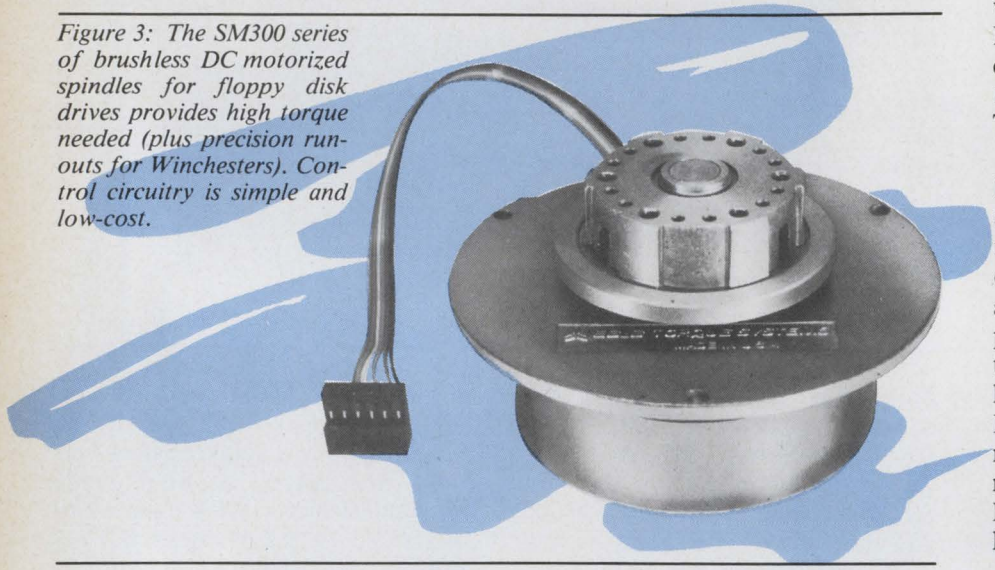


Figure 3: The SM300 series of brushless DC motorized spindles for floppy disk drives provides high torque needed (plus precision runouts for Winchesters). Control circuitry is simple and low-cost.

The 1812, with 64K user memory and the 1413 diskette drive, is $12,770; the 1814, with 120K user memory and a 1413 diskette drive, is $14,070. Add-on 1413 diskette drive modules are $5,795. **Datapoint Corp**, 9725 Datapoint Dr., San Antonio, TX 78284.

A series of economical brushless DC motorized spindles meets Winchester and floppy disk drive needs. The SM300 series provides high torque needed by floppy drives and precision runouts necessary for Winchesters. The brushless DC motor design produces a full 360° of torque for smooth starting from any position and for minimizing instantaneous speed variation. It has an optional magnetic exclusion seal, which is compatible with a class 100 environment as required for Winchesters. Models available for 5¼" and 8" drives. Control circuitry is simple and inexpensive. Only two power devices are required for high-speed Winchesters, the Hall device within the motor furnishes the speed signal; for floppies, a separate, higher-resolution reference is required. **EG&G Torque Systems**, 36 Arlington St., Watertown, MA 02172.

A new flexible disk system, for DEC LSI 11/02 and 11/23 based μCs, holds up to 1MB of on-line random storage on each of 2 diskettes. A single dual wide controller contains an on-board bootstrap. Housed in a 5¼" rack mount chassis, the dual-drive is available in the single-sided **800-1** version with capacity of 1MB ($3295), or the double-sided **800-2** with capacity of 2MB ($3995). **General Digital Industries, Inc**, 500 Wynn Dr., Huntsville, AL 35805.

The **megafloppy 1117 family** includes two single and two double-sided drives using 96 or 100 tpi double track recording technologies. Increased storage capacity was achieved by increasing data recording density from 6,000 bpi to 12,000 bpi using MFM recording techniques. Model 1117 provides 6ms track-to-track positioning speed with 600,000 bps data transfer rates, and also provides full compatibility with industry standard interfaces. Double sided models provide 2.175 and 2.025 MB of formatted storage at 100 and 96 tpi, respectively; single-sided versions offer 1.2 and 1.1125 MB. **Micropolis Corp**, 21329 Nordhoff St., Chatsworth, CA 91311.

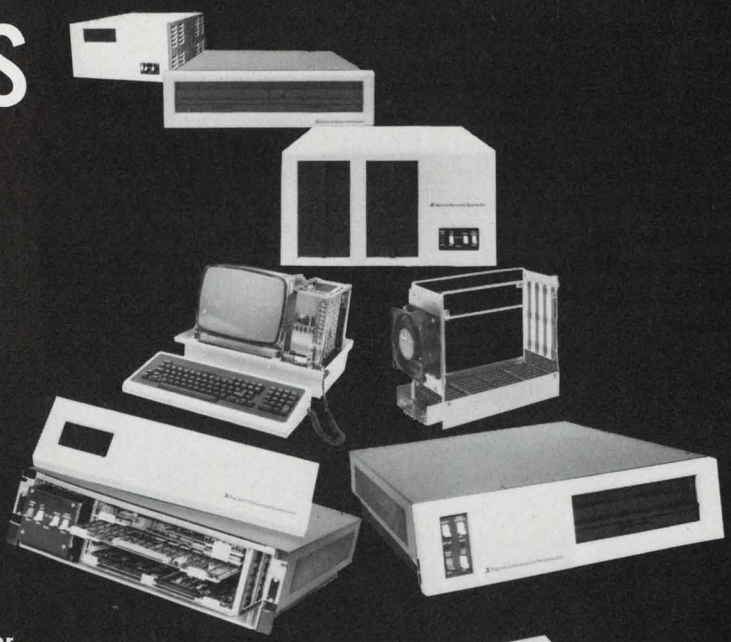
More capacity, faster performance and full software support make the Micro-Sci 5¼" floppy disk drive an alternative to 8" floppy drives — with a 5¼" size and price. Each **A-70** disk drive stores 286 KB, a full 12% increase over the 256 KB found in 8" floppies. A longer, two-piece clutch means accurate diskette registration and less media distortion. A steel band positioner provides faster head positioning and gives the A-70 about half the seek time of an 8" drive. Full software support provided with each drive includes compatibility with DOS 3.3, Pascal and CP/M. First drives are priced at $699; second drives are $599. **Micro-Sci**, 17742 Irvine Blvd., Suite 205, Tustin, CA 92680.

A new dual-sided flexible disk head assembly has adjustable upper arm, improving media interchange reliability for systems with track densities of 96 tpi and greater. It is adjustable to within 50μin. as compared to the industry-wide required tolerance for 96 tpi head-zero-to-head-one alignment of 200μin. Drives using this head assembly do not require modification: simply replace the existing head assembly. **Nortronics Co**, 8101 Tenth Ave. N., Minneapolis, MN 55427.

A new series of double-sided, dual density floppy disk subsystems store up to 1MB of data on a single floppy diskette. Both controllers can support 2 floppy disk drives for a maximum capacity of 2MB. The PM-ZS31 is used with the PDP-11. The single, quad-wide microprogrammed controller is software transparent to DEC operating systems and it is pin-to-pin, signal, and power compatible with both Plessey and DEC Unibus SPC backplanes. **The PM-XSV31** consists of a single dual-wide controller board and a choice of one or two floppy disk drives, designed for use with the LSI-11. **Plessey Peripheral Systems**, 1691 Browning Ave., Irvine, CA 92714.

Intended for the DDP user with limited storage requirements, the **PTS/1220** offers up to 4.1MB on 4 daisy-chained drives. The direct-access data storage devices use removable 8" diskettes. The processor's drive uses a two-sided, double-density, flexible diskette with a recording density of 6,816 bpi and a formatted capacity of 1.025MB. Track-to-track access time is 3ms.

ENCLOSURES and MODULES for LSI-11 SERIES SYSTEMS



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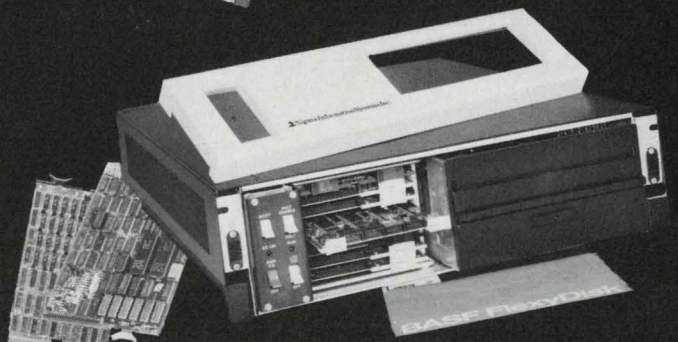

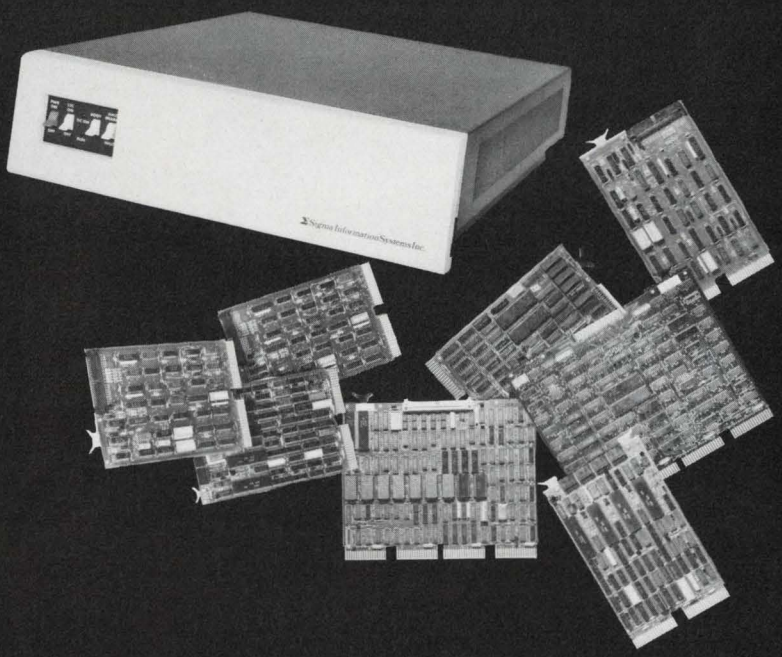

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Maxell Proposes 3″ Floppy Standard

Hitachi Maxell, Hitachi and Matsushita have made a joint announcement of the establishment of a technical standard for a new compact floppy disk (80mm wide by 100mm long by 5mm thick) that will be used in disk drive systems that are compatible and interchangeable with conventional floppy disk drives. The capacity of this new disk is 125K bytes for the single sided, single density version and 500K bytes for the double sided, double density type.

All three companies, Hitachi Maxell, Hitachi and Matsushita will join in proposing this new standard to disk and computer hardware manufacturers. Mr. Ted Ozawa, Vice President, Special Products Division, Maxell stated: "We believe that this new standard for a 3″ compact floppy disk will be adopted by many computer hardware manufacturers and we expect that various disk drives using this new 3″ disk will begin to appear in the marketplace toward the latter part of 1982. The high capacity of this 3″ disk is the result of an ongoing intensive R&D program in floppy disk technology and will result in both hardware and magnetic media economies for the public."

This announcement comes only a short time after the announcement by Maxell of their super high density 5¼″ floppy disk, which is capable of almost 5MB of storage capacity.

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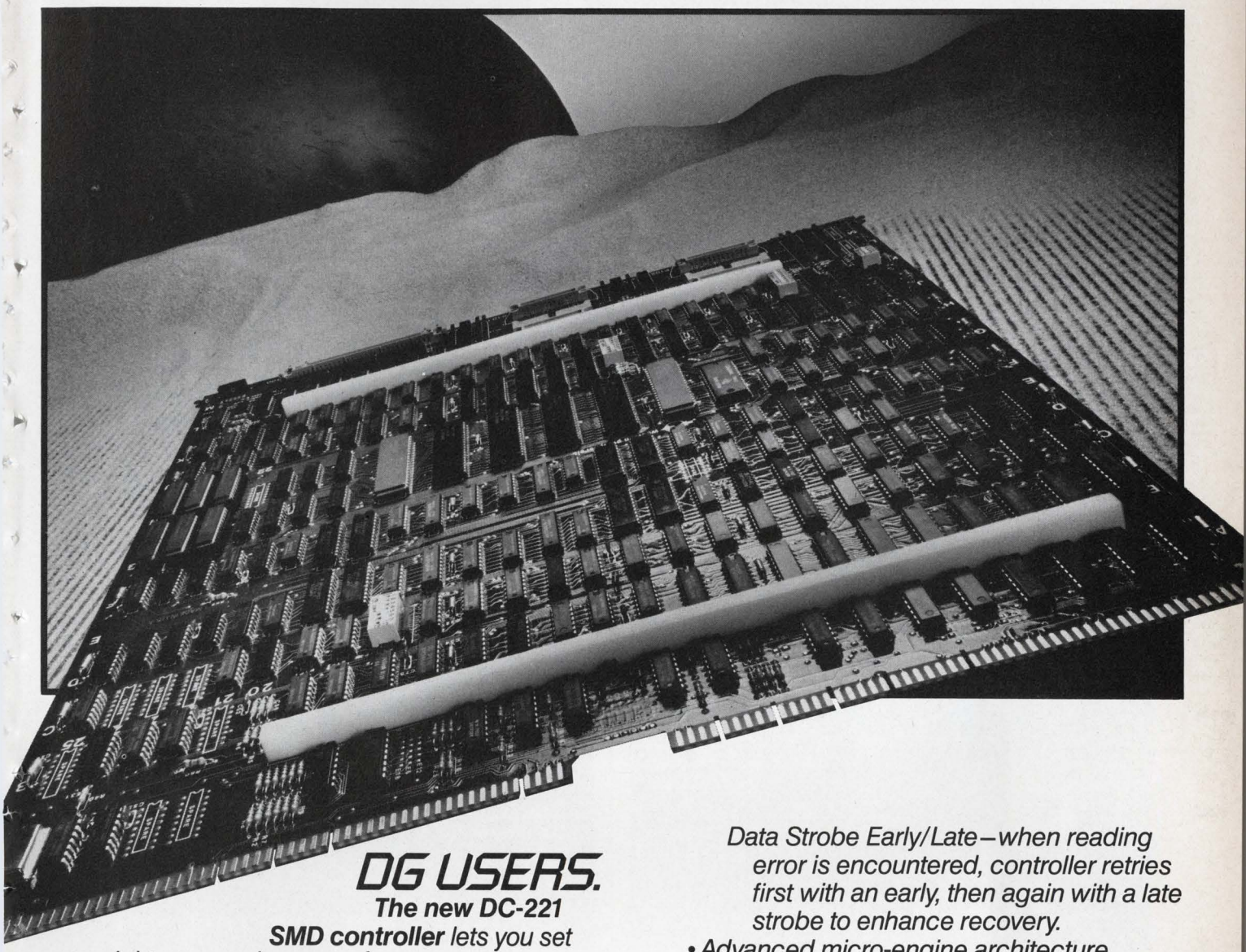

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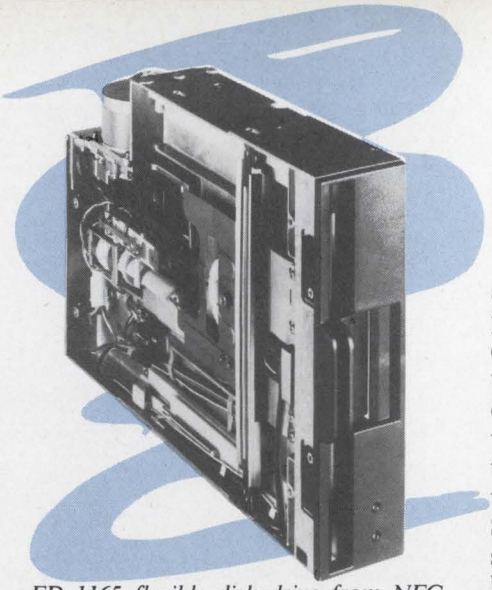
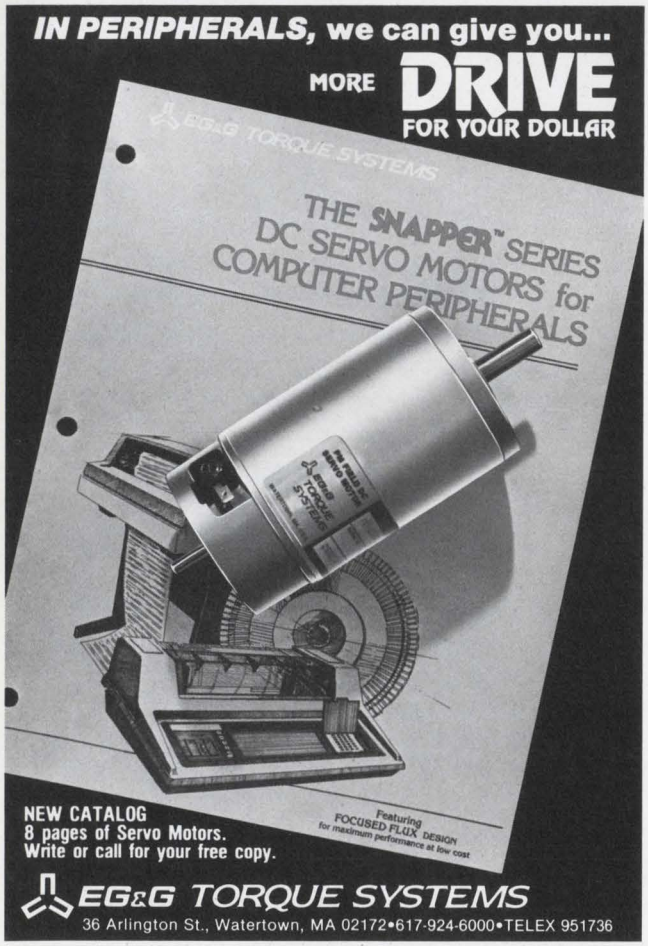
Model 3831 field upgrade diskette system with controller, adapter, expansion chassis and first 1.025MB diskette drive, cables and software is $4100: **Models 3832** and **3834**, field or factory installed drives are $1650; **Model 3833** diskette expansion chassis and 1.025MB drive is $2850. **Raytheon Data Systems**, 1415 Boston-Providence Tpke, Norwood, MA 02062.

RX02 compatible floppy disk systems for PDP-11, LSI-11 and VAX/Unibus computers may be configured with two single-sided or double-sided disk drives. It is hardware, software and format compatible with DEC's RX02 and RT-11, RSX-11M and VAX/VMS software. **The FWT0100/FWT1100** series may be upgraded to Winchester plus floppy system for storage to over 35MB. The Winchester also offers 5 times faster access and over 10 times faster data transfer throughput. IBM 3740 single density and IBM 2/2D double density formats are also supported. Floppy only systems are $3900; an 8.9MB Winchester plus 1MB floppy system starts at $6900; OEM discounts available. **Scientific Micro Systems Inc**, 777 E. Middlefield Rd., Mountain View, CA 94043.



FD 1165 flexible disk drive from NFC Information Systems, Inc. is half the height of conventional 8-inch drives, uses a controlled head loading mechanism, and has an unformatted capacity of 1.6 Mbytes.

At 96 tpi, **SA410** (single-sided) and **SA460** (double-sided) minifloppy drives feature unformatted capacities of 500KB and 1MB, respectively, using double-density recording. Both incorporate helical cam v-groove lead screws for head positioning (not band or disk positioners) for improved access time. Single-point ball follower in the screw eliminates hysteresis (backlash) and minimizes friction. Both use fast-starting DC spindle motors instead of head-loading solenoids, allowing drives to be shut down when not in use to avoid the problems of head and media wear and damage caused by solenoid-controlled head loading. SA410, $325; SA460 $400 (100). **Shugart Associates**, 475 Oakmead Parkway, Sunnyvale, CA 94086. □



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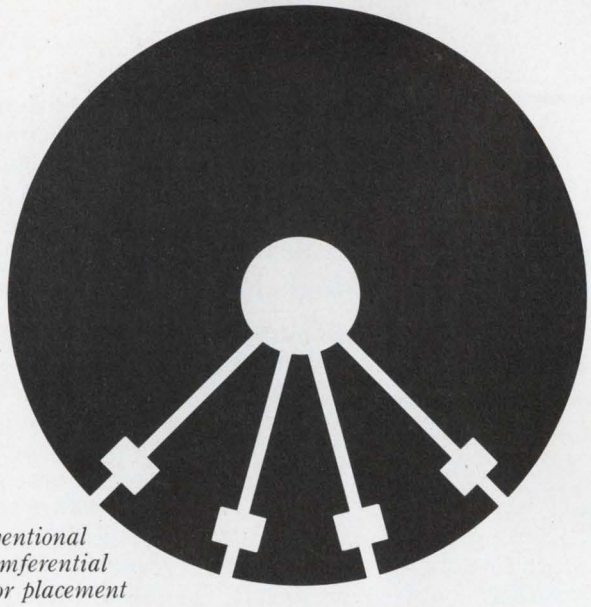
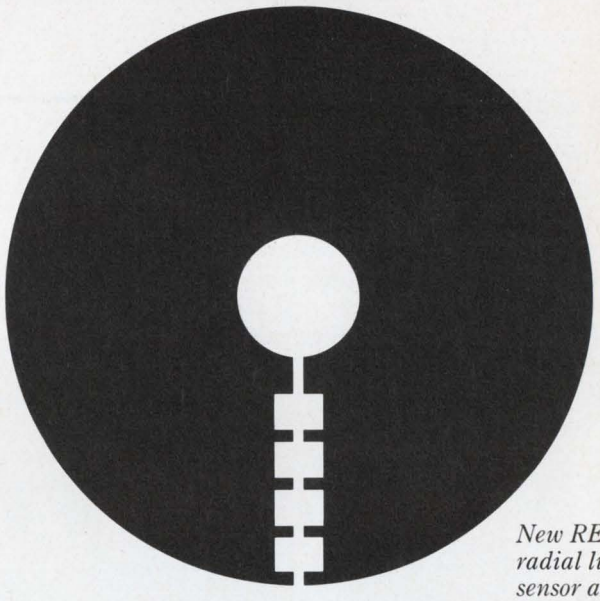


Conventional circumferential sensor placement



New RENCO radial line sensor array

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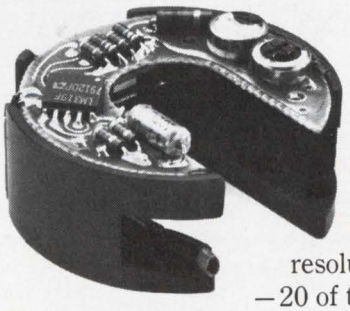

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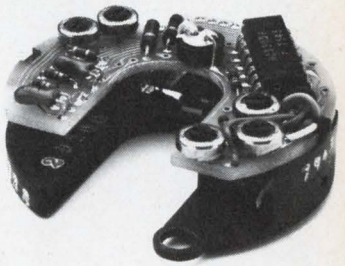

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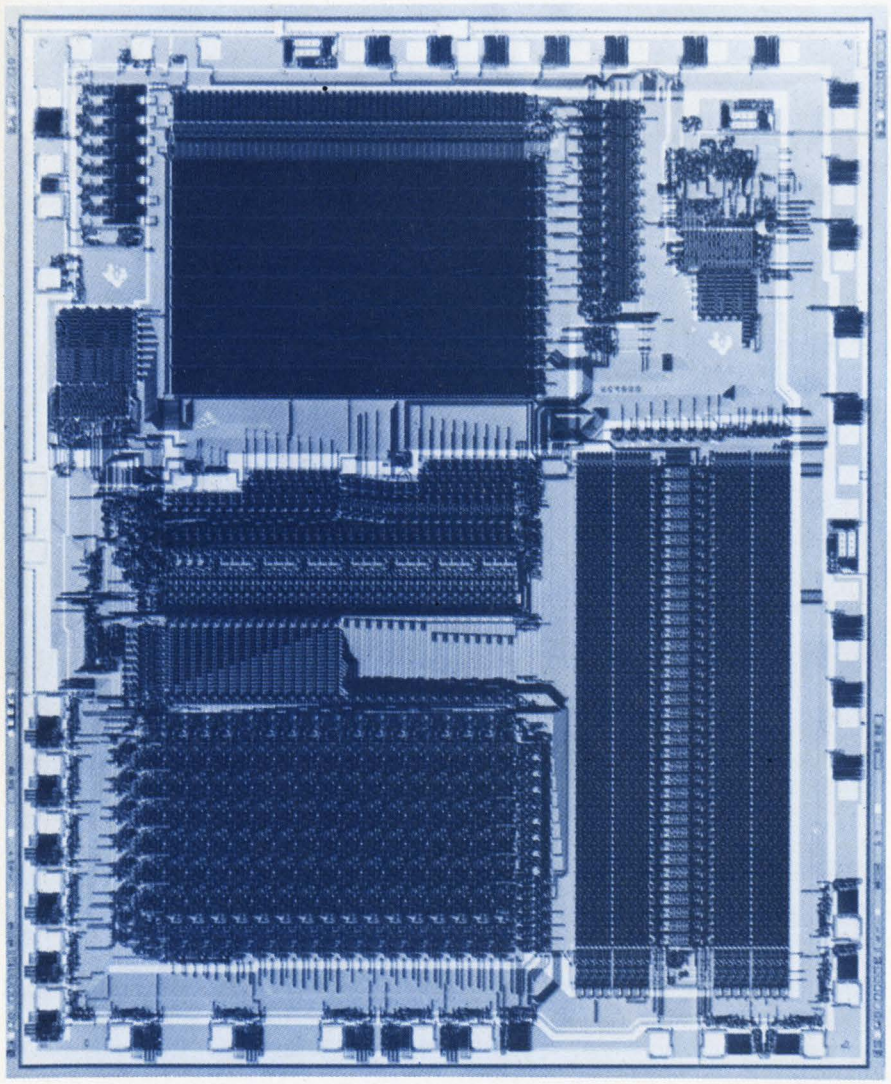
ISSCC '82: State Of The Art In Solid State

by David Wilson

ISSCC '82 marked an important milestone in the years' calendar. Many of the latest gains achieved in solid state technology were to be found here, and the reader can be certain that many devices that were discussed will find their way onto board and into system designs in the near future.

μC's gain number crunching capabilities and find applications in voice recognition.



The conference was broken down into sixteen sessions covering such diverse subjects as digital signal processors, dynamic and static RAMs, and device modeling and characterization.

Digital Signal Processors

Chaired by Mr. P.J. Verhofstadt of Fairchild, Santa Clara, this session revealed a 2 μ CMOS/LSI 32-point Fast Fourier Transform Processor from TRW, and a single-chip single signal processor for a digital Modem (9600 or 14400 bps) from Matsushita Electronics, Japan.

Mr. E.R. Caudel, Texas Instruments, Houston, described a new high performance μC, the TMS 320, which is capable of implementing a variety of complex digital signal processing systems. The device has a comprehensive μP instruction set which makes it also applicable in a wide range of general computing and high speed control applications (**Figure 1**).

The heart of the processor is a high speed, arithmetic unit containing 32-bit ALU, 0-16 bit shifter, 16 x 16 bit signed multiplier and 32-bit accumulator. The device is configured to support two modes of program store operation. The first configuration, the TMS 320M10, uses on-chip program ROM for single-chip high volume applications. A combination of internal ROM (1.5K words) and external program memory (2.5K words) is

Figure 1: TMS 320 from TI. The device has a single accumulator Harvard type architecture that allows full overlapping of the instruction fetch and execution, due to data and program residing in separate address space. Instructions have been provided that connect the two spaces together.

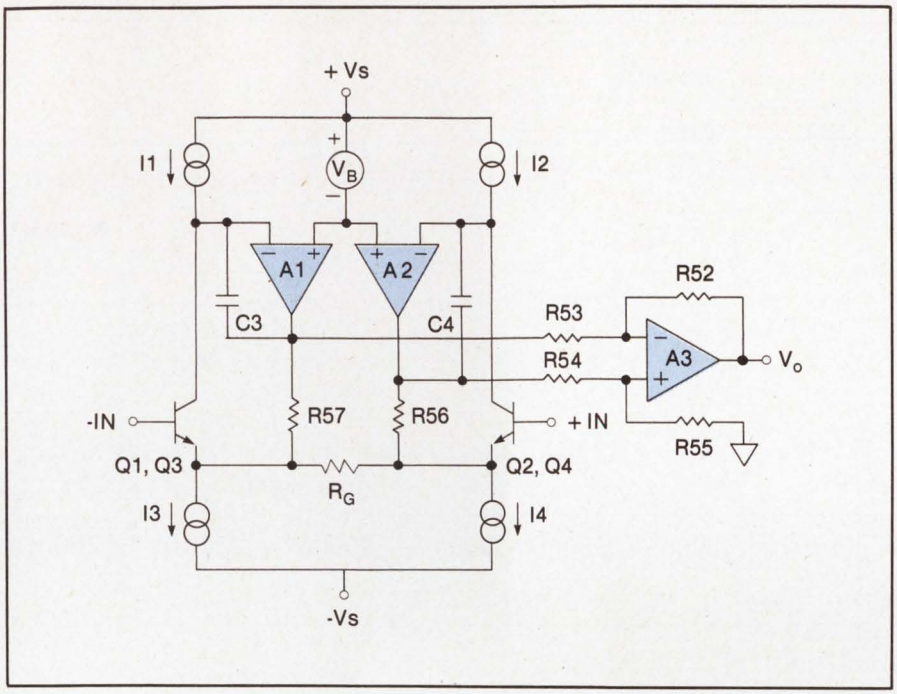


Figure 2: Simplified representation of the Analog Devices amp. Errors that cannot be adjusted by automatic zeroing and scale factor adjust are reduced to new lows.

also allowed which could be useful in systems with fixed Kernal routines and various application system configurations. A second mode, the TMS 32010, supports 4096 words of external program memory and completely suppresses the internal ROM.

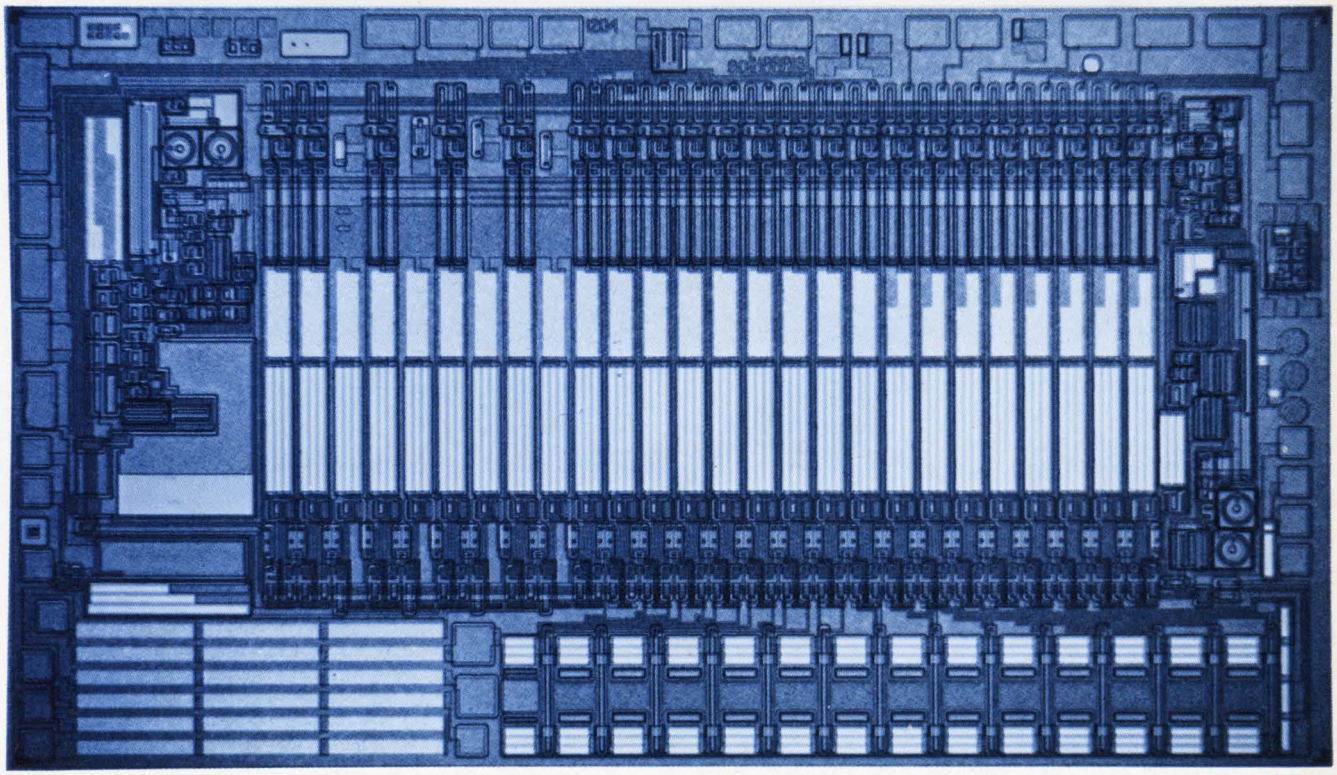
This mode allows a user program to reside in external 4K memory and development system software to reside in on-chip program ROM. Thus, the device not only supports self emulation, but can also be used as its own development system. The external program memory interface runs at the same speed as internal ROM, thus allowing real-time development and execution of user programs.

The device is packaged in a 40-pin DIL pack, dissipating 950mW typically. The maximum clock frequency is 20MHz for an instruction rate of 5 million instructions per sec. Several test modes are incorporated to aid production testing and yield analysis. The processor, data memory, and on-chip ROM can all be isolated for purposes of testing and reliability analysis.

To date, Mr. Caudel said that the device had demonstrated the capability for performing LPC analysis and connected speech recognition with a 25 word vocabulary.

In 1978, Mr. Frederick Ware began the development of CMOS/SOS floating point processor circuits at HP. At the ISSCC he spoke of a set of processors recently completed by HP's computer systems division. There are three processors in

Figure 3: Harris 16-bit monolithic DAC.



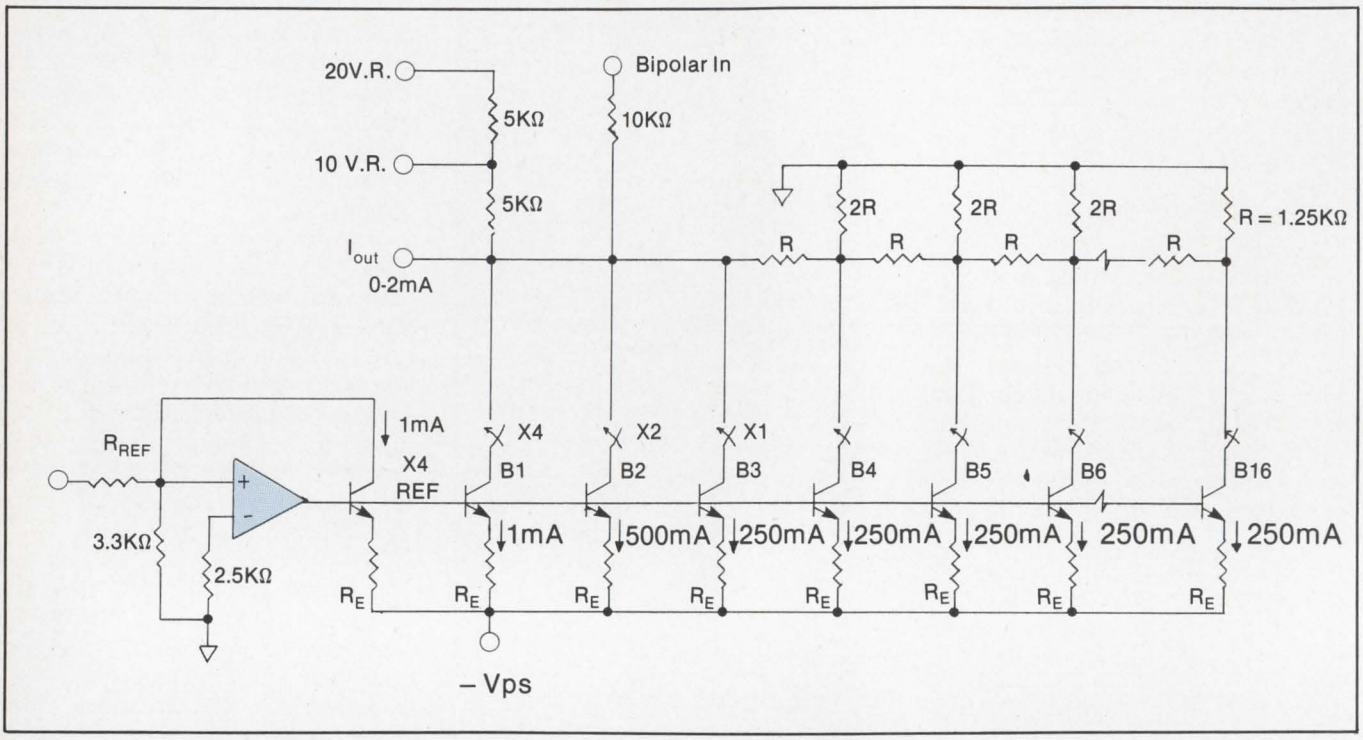


Figure 4: Basic configuration of Harris DAC. The process used for the circuit contains complementary, bipolar transistors and buried zener diodes in a dielectrically isolated structure.

the set: an add/subtract chip, a multiply chip and a divide chip; these three handle the 32-bit and 64 floating point and 32-bit fixed point data types of the HP1000 minicomputer. The chip set is placed in parallel to the primary data path of the CPU and controlled by a microprogram. The add and multiply chips can perform 32-bit scalar operations in about 750ns when used in a high performance configuration. This figure does not include system-dependent overhead time for instruction dispatching and data accessing.

It is also possible to operate multiple chip sets in an interleaved manner, and thereby create a pipelined processor capable of executing vector (many operation) instructions in the minicomputer systems. The add and multiply chips are able to overlap operations, and each provides a 32-bit processing bandwidth of two MFLOP's (millions of floating point operations per second). Three interleaved chips will saturate the data bandwidth of a bus set (six MFLOPs), but multiple bus sets may be pipelined for additional throughput.

Mr. Ware concluded with the applications of the chip set that included signal and image processing, graphics processing and linear system decomposition.

Data Acquisition & Conversion

With the advent of low cost 12 bit data conversion systems, the need to extend the true instrumentation amplifier (in-amp) function to this realm is evident. Scott Wurcer,

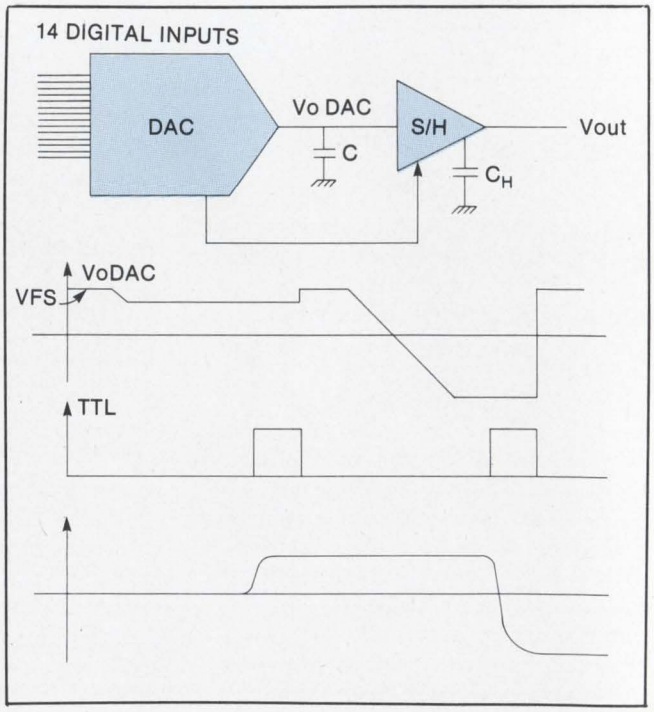


Figure 5: Signetics 2-chip converter employing two precision ratioed current sources and an external capacitor.

Analog Devices, Wilmington, described a completely self-contained systems level amplifier designed to address this need.

He claimed that errors that cannot be eliminated by automatic zeroing and scale factor adjust, such as nonlinearity, noise, and settling time, are reduced to new low levels.

Figure 2 is a simplified representation of the new amplifier. Feedback will keep the collector currents of Q1, Q2, Q3, and Q4 constant and, as a result, the input voltage is impressed across RG. Since the unity gain subtractor (A3, and R52 to R54) amplifies the difference between the outputs of A_1 and A_2, Vo is the differential portion of the input voltage times the programmed gain. Three pin selectable RGs are provided for gains of 10,100, and 1000. R52, R53, R54, and R55 are laser trimmed to ratio match within +.01%, this insures over 80 dB attenuation of common mode signals and unity gain accuracy of +.02%. The RG terminals are brought out to enable the user to select any gain between 1 and 1000.

This configuration might also be recognized as a classical three amplifier in-amp (A_1, A_2, A_3) preceded by a preamp. As RG is reduced to increase closed-loop (programmed) gain, the transconductance of the input preamp increases asymptotically to the transconductance of the input transistors (-2000μmhos). This has three important advantages. First, this approach allows the circuit to achieve an open loop gain of 3×10^8 at a programmed gain of 1000, thus reducing gain related errors to a negligible 30ppm. Second, the gain bandwidth product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors.

The demand for low-cost high-accuracy D/A converters continues to grow, especially with recent developments made in digital recording of audio signals. Realizing this demand via monolithic ICs is obviously the most cost effective method, but for 16 bit accuracies, the related process requirements have been difficult to achieve. Linda Trythall, Harris Semiconductor, illustrated a monolithic circuit that utilizes a conventional configuration with special layout techniques to reduce the process demands. The initial accuracy achieved approaches that of very expensive hybrid modules while the accuracy over wide temperature ranges surpasses anything presently available on the market.

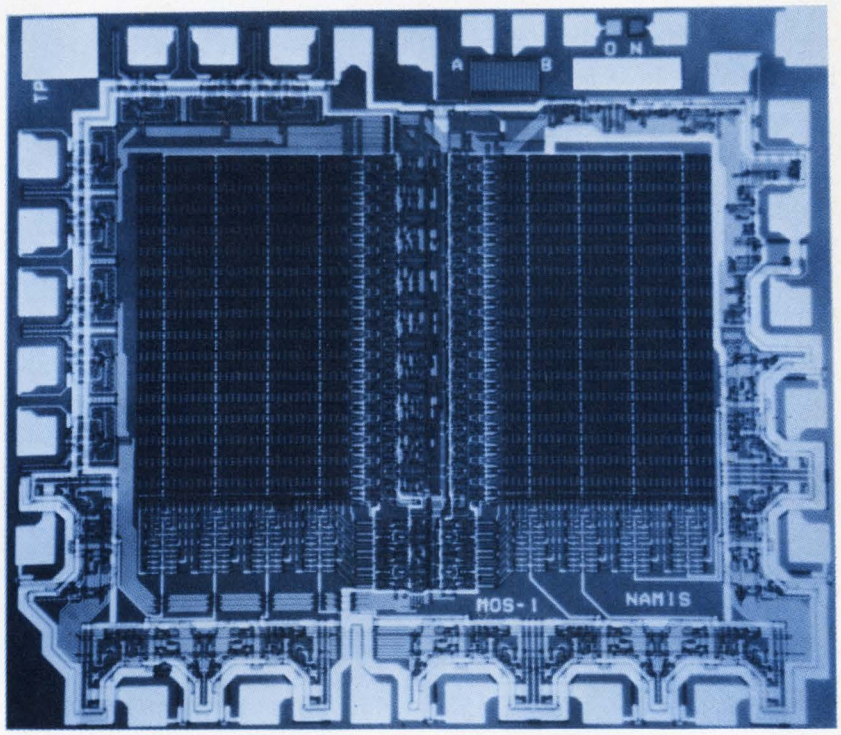


Figure 6: Fujitsu's 2Kb EAROM claims data retention characteristics superior to MNOS devices.

32-bit system design approach from HP requires concentration on packaging.

This circuit is a laser trimmed 16 bit accurate monolithic D/A converter fabricated with a bipolar DI process (**Figure 3**). It has 16 parallel inputs using straight binary format and has a 0-2mA current output with onboard range resistors. The basic configuration seen in **Figure 4** consists of binary weighted current cells accurately controlled via a servo amplifier in conjunction with the reference resistor. The initial accuracy is set by trimming the NiCr emitter resistors of the current sinks while the circuit is in an active mode. The bit weights are adjusted with respect to each other so as to remove all initial component match errors simultaneously.

The performance of the DAC is summarized in **Table 1.** The limitation of the circuit's accuracy is largely dominated by drift over life. The specification shown in Table 1 for accuracy drifts are the one sigma standard deviations on a group of high grade units. The selection of these high grade units was made based on accuracy drift after 168 hours of burn-in.

Ms. L. Trythall concluded that greater understanding of the mech-

Table 1 Performance Specifications

Resolution	16 bits
Unipolar Offset @ 25°C	± ½ LSB
0° - 70°C	± .2ppm of FSR/°C
Integral Nonlinearity @ 25°C	± ½ LSB or ± .0008%
0° - 70°C	± 1 LSB or ± .0015%
Differential Nonlinearity @ 25°C	± ½ LSB or ± .0008%
0° - 70°C	Monotonic or ± .3ppm/°C
Settling Time (Full Scale Transition) Current settling to ± .003%	1μsec
Noise at Output RMS ± 1σ 10Hz to 1MHz	⅓ LSB
Drift over 1000 hr @ 125°C	
Unipolar Offset (± 1σ)	± 10μV or ± 1ppm/1000 hr
Diff. Lin. (± 1σ)	± 80μV or ± 8ppm/1000 hr
Power Supply Sensitivities	
Gain	85dB or .8ppm/%
Differential Linearity	95dB or .3ppm/%
Power Dissipation	450mW

anism of the long term accuracy drifts may eventually lead to higher accuracy converters.

Applications in the newly emerging home digital-audio playback field were also addressed by Bill Mack, Signetics, who spoke of the market necessity for 14 to 16-bit D/A converters.

In particular, he spoke of a new two chip converter, a dual ramp D/A and a precision sample and hold amplifier. **Figure 5** shows the basic operation. The analog output voltage Vodac is first reset to full scale V (FS). The DAC then supplies a current to the capacitor C to ramp the output voltage, the duration of the ramp being digitally controlled by the input code. When the ramp is completed, the S/H acquires the analog output voltage.

One significant feature of the converter design, Mr. Mack said, is a current divider circuit which achieves a ratio accuracy between two currents of 0.003%. This accuracy is implemented by a special purpose R-2R ladder configuration with a low offset, drift and bias current op-amp to control termination voltages. To eliminate offsets due to die attach stress in the op-amp, the op-amp is electrically trimmable through the digital inputs by shorting zener diodes after packaging. The fast growth of the μP market in recent years has resulted in an increasingly growing interest in fast, non-volatile electrically erasable memories. The requirements set by the μP-based systems include:

- Nonvolatility
- On-board erasability
- Bit/byte erasability
- Short erasure time

The widely-accepted ultraviolet erasable EPROMS fail to meet the last three of the above requirements. Their erasure normally requires the removal of the component from the board and its exposure for approximately 20 minutes to an ultra-violet light, resulting in erasure of the whole memory content-chip erase.

To meet the above new requirements, two distinctively different EEPROM technologies have been developed:

1. **MNOS technology,** in which electrons are stored at the interface of a stacked oxide-nitride structure, which form the gate isolation of the memory device.
2. **Floating gate technology**, in which electrons are stored in a floating layer deposited between two thermal oxide layers.

Dr. G. Yaron described a 16K thin oxide-floating gate EEPROM, that appears to be National Semiconductor's answer to Intel's 2816. The part features three high voltage operating modes: byte write and byte erase in which the content of a single byte can be altered within 10msec and a chip erase mode in which the whole chip can be erased within 10msec. A low voltage standby mode reduces worst case current consumption from 70mA in the active mode to 10mA in the standby mode. An on-chip thin oxide protection is provided by an internal pulse shape generator which generates minimum thin oxide stress pulse from an external 21VDC signal. A chip write and a threshold bit mapping testing feature covering a cycling testing spectrum ranging from zero to well over 10^5 assures tight reliability screening. A retention of well over 10 years is assured by reading at reduced voltages generated on-chip and by unique thin oxide properties providing I-V characteristics with a slope of less than 1 decade/.7V.

Continuing the theme of non-volatility, Shinpei Hijiya, Fujitsu Labs, Japan, covered the development of a single 15V supply 2Kb EAROM arranged as 256/8b words. Writing and erasing are done by raising Vpp to 15V for 10ms (**Figure 6**).

Mr. Hijiya claimed that this voltage was exceptionally low when compared to other MNOS approaches (25V) or tunneling oxide approaches (17V, 21V). For the write/erase endurance, the threshhold window remains beyond 10^4 cycles, and even after 10^4 cycles, non-volatile data retention of more than 10 years at 150°C is obtained.

EEPROMs gear up for low-voltage programming capability.

Contradicting previous thought, Ronald M. Fisher from Harris Semiconductor described a 64K PROM fabricated using a lateral thin film fuse link. The circuit follows the generic scheme employed by Harris on all of their

bipolar PROMS. The device is arranged 8K x 8 with 4 bits on either side of the row decoder. A double wide row decode arrangement had to be created in order to properly match up a new matrix cell.

Because of smaller cell sizes, the 64K device was achievable in a die size of 5.09mm x 7.3mm with a shrink of the chip coming shortly. Extension of this technology, according to Mr. Fisher, implies that a 128K PROM will also be possible using a lateral fuse element. The part is packaged in a 24 pin 600 mil DIP and conforms to the JEDEC pinout. The part consumes a maximum of 190mA of Icc at 5.5V, 75% less power than the four 16K PROMs it replaces, while having typical access times of 45ns.

At last year's ISSCC, the topic of redundancy was in the forefront of discussion. This year, Alan Folmsbee, Intel, brought the subject up again with reference to a 128K EPROM. The device active area of 23mm² is large enough to benefit significantly from redundancy, he said. The device is organized as 16K bytes of regular storage plus an additional 128 bytes of redundant storage. The redundant storage is contained in four extra rows of 32 bytes each. If a defective bit or row is found, a redundant row is activated to replace it by memory tester software control of signals to the standard 28 pins.

The circuit which is central to the redundancy system is shown in **Figure 7** and is referred to as a CAM (Content Addressable Memory). 36 CAMs are used to program the 4 redundant row decoders to respond to the addresses of any row. Each X address of each redundant row has one CAM. The memory element in the CAM is a polysilicon fuse link. The fuse resistance is changed from about 200 Ohms to an open circuit by applying a high voltage pulse train to the fuse. The pulse train can only be applied if the Repair Mode signal (RM1) and the row address signal (AX) are both at low levels. The Redundant Row decoder is a NOR gate with output RN1. Depending on whether or not the fuse in a CAM is blown, AX or $\overline{AX}$ is input to the NOR gate, thereby permanently coding the redundant row to the address of the row to be replaced.

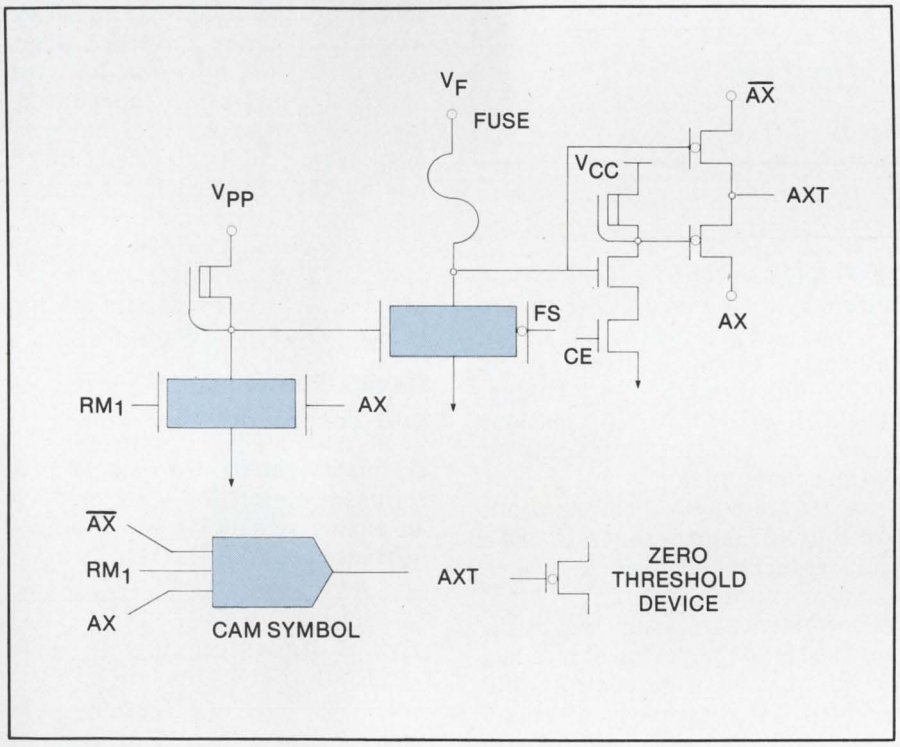


Figure 7: Content addressable memory from Intel.

Circuits For μP Based Systems

Today floppy disks are very popularly used in small data processing systems such as personal computers, minicomputers and terminals. Because floppy disk recording density is low, existing floppy disk controller devices are required to handle serial data at the rate of only up to 500K bits/sec. and detect errors by the simple cyclic redundancy check. But recently, small-size hard disks, namely Winchester disks, are obtaining growing popularity in small data processing systems due to their larger storage capacity and good cost performance. Very high recording density of modern hard disks requires the controller device to execute very high speed data transfer and also to facilitate high-level error detection and correction operations. Probability of data error increases with the higher recording density. Moreover, defects in recording media that are only a minor concern at lower recording densities can become a serious cause of hard errors at the higher recording densities of Winchester disks.

With this in mind, Mr. T. Ohtsuka, NEC, described a single-chip HDC that handles high speed data transfer of up to 1.5 MB/sec. between the host system and one of up to 8 Winchester disks connectable to itself. It performs high-level error detection with hardware implementation of the Fire code while handling high speed serial data of up to 12 Mbits/sec., facilitating easy correction of errors by the host system.

As shown in **Figure 8**, the HDC is composed of two major functional blocks, the on-chip 8-bit parallel processor and the format controller. The on-chip processor governs overall functions of the device including control of the format controller. Various operations of the HDC are instructed by 15 different commands. Each command is initiated by a multi-byte transfer from the host system. The on-chip processor interprets the command that is fully specified by multiple bytes, and loads internal execution program for that command into RAM of the format controller so that the device

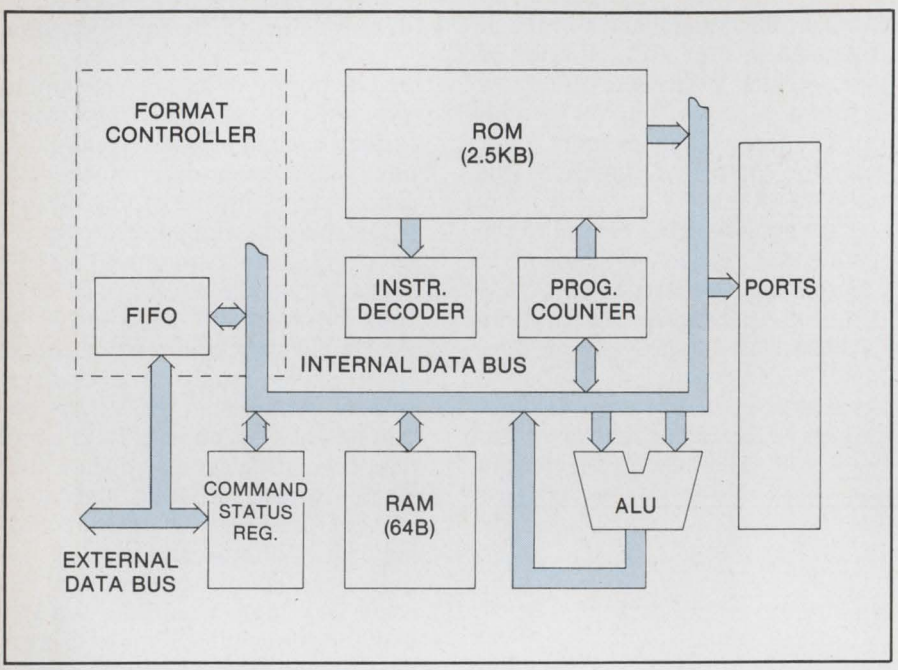


Figure 8: Major functional blocks of the NEC HDC.

will perform the operation specified by the command. After execution of a command, a multi-byte of information can be sent back to the host system to indicate operation result status. The on-chip processor facilitates this interchange of multi-byte information between the HDC and the host system. Since the HDC is designed such that any hard load of special function or high speed operation is eliminated from the on-chip processor, a standard 8-bit μP architecture is adopted to this portion.

The format controller reads data from and writes data onto a disk according to the specified track format, executing MFM decoding/encoding, precompensation, serial-to-parallel/parallel-to-serial conversion, address mark detection/writing and error location and pattern detection. The format controller contains a microprogram processor and other functional blocks necessary to implement an efficient high speed operation. Serial-to-parallel and parallel-to-serial data conversion takes place in the Serial-to-parallel/Parallel-to-serial Register (SPR) in synchronization with the Winchester disk operation timings.

Maintaining full software compatibility with previous devices (the 9900 and the 9995) and increasing throughput by a factor of from 3 to 14, was the goal behind the design of a new 16 bit μP from TI, the 99000, discussed by Karl Guttag. The IC has demonstrated a machine state rate and memory cycle of greater than 7MHz.

A 256 state by 152 bit microcode word ROM controls the CPU, and a data reduction method, known as Compressed Control ROM (CCROM) was used to reduce the physical ROM requirement by a factor of 4. The wide control word enabled faster execution of microcode and reduced the need for random logic or PLA's; the performance of the microcode is demonstrated by a signed 16 bit divide in 34 cycles (4.9μs), a signed 16 bit multiply in 25 cycles (3.6μs) and an interrupt context switch in only 13 cycles (1.9μs). For high usage instructions, Mr. Guttag said, special hardware was added to speed execution; for example, a memory-to-memory move or a conditional jump requires as little as 3 cycles (0.42μs).

Still on the theme of μP systems, Mr. Dana Seccombe of HP's desktop division, sketched the design of a fully integrated 32-bit VLSI processing system, focusing on the memory subsystem. This high performance design implemented in MOS technology made special system and circuit design tradeoffs to preserve high throughput. These include special packaging, clock generation, and system protocols which play to the strength of MOS VLSI.

The system consists of the following VLSI chips: a 32-bit CPU, an I/O processor, a memory controller, a 128K bit RAM, a 64K bit ROM, and a clock generator chip, all fabricated in a 1 micron NMOS double-layer-metal technology. The IC chips are directly mounted on a special printed circuit-like substrate with a copper core and teflon interlayer dielectrics, providing low cost packaging, and a low capacitance, low inductance electrical environment. These chips can be assembled into a tightly coupled 32-bit processing system with multiple CPU, I/O, and memory processors, operating at a bus transfer rate of 36 MB/sec. A block diagram of the system is shown in **Figure 9.**

Device Structures and Technology

A binary-analog correlator performs the correlation, C(t), between an analog signal S(t) and a binary reference code R(n):

$$c(t) = \sum_{n=0}^{N-1} R(n)\ S[t-(N-n)\triangle t] \quad (1)$$

where S[t-(N-n) $\triangle$ t] are sequential samples of the analog signal. In operation, the device samples the analog signal, performs the multiply-add indicated in the equation, and performs the required shift of the reference code with respect to the signal, thereby performing the correlation between a received analog signal and a locally generated reference code. The design goal of the GE Schenectady team headed by William Engeler was to integrate a dual 128-bit correlator on a single chip dissipating less than 0.5 watt while achieving operation from $-55°C$ to $+125°C$.

This design employs a moving reference architecture where charge

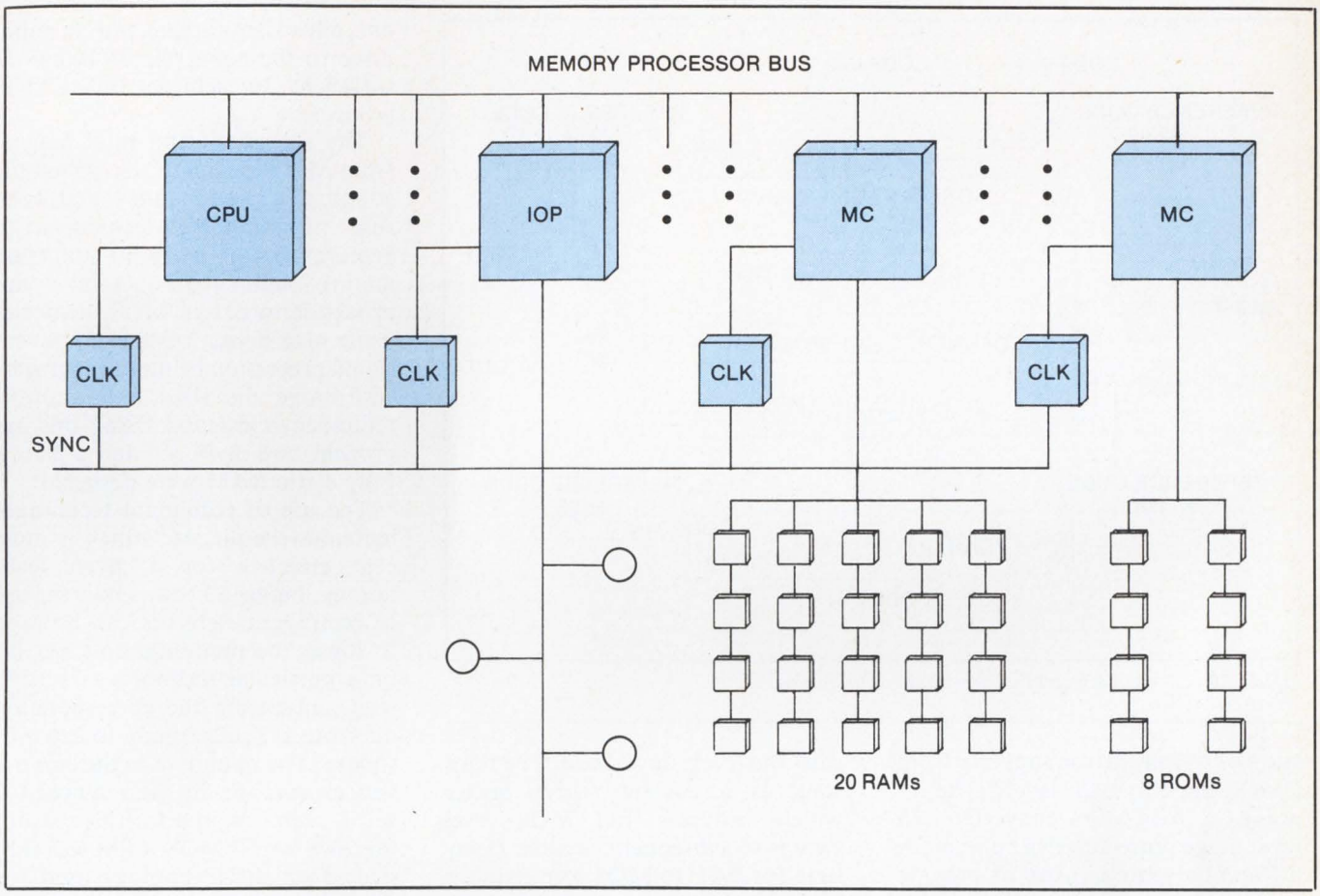


Figure 9: System block diagram of HP's VLSI system features special packaging, clock generation and system protocols.

packets corresponding to samples of the analog signal are stored in individual correlation cells and are transferred back and forth in these cells under control of a binary reference code which is shifted through a CCD register. The summation indicated in the above equation is achieved by detecting the signal charge on a single output electrode which overlies all cells in the correlator.

The overall chip architecture shown schematically in **Figure 10** is designed for computing the correlation between a single reference code and the in-phase and quadrature components of a complex signal. A photomicrograph of the dual 128 bit correlator chip, which measures 128 x 277 mils, is shown in **Figure 11.**

The circuit was designed to perform a true binary-analog correlation. That is, the analog signal sample is multiplied either by +1 or −1. It should be noted that a trilevel correlation, where the analog signal is multiplied by either +1, 0 or −1, is easily accomplished with this correlation cell. The multiplication by zero is achieved by not transferring the charge in the correlation cell. The zero can therefore be represented in the CCD by either a one followed by a one or a zero followed by a zero.

Correlator achieves broad operating range while dissipating low power.

Static RAMs

The session on static RAMs appeared to be dominated by Intel Corp., whose authors presented three papers covering both NMOS and CMOS technologies.

The 4K x 1 ECL compatible static RAM discussed by Edwin Hudson is designed to be directly compatible with industry standard 4K bipolar ECL memories. Consequently, the chip select pin is used to provide a fast output enable capability. Access time from chip select is typically 10ns, and the device has a current dissipation of 150mA when operated at the nominal supply voltage of −5.2V.

The overall circuit block diagram is shown in **Figure 12.** Internally, the memory uses normal MOS circuits and voltage swings. An input buffer converts from ECL levels to CMOS levels for each input signal,

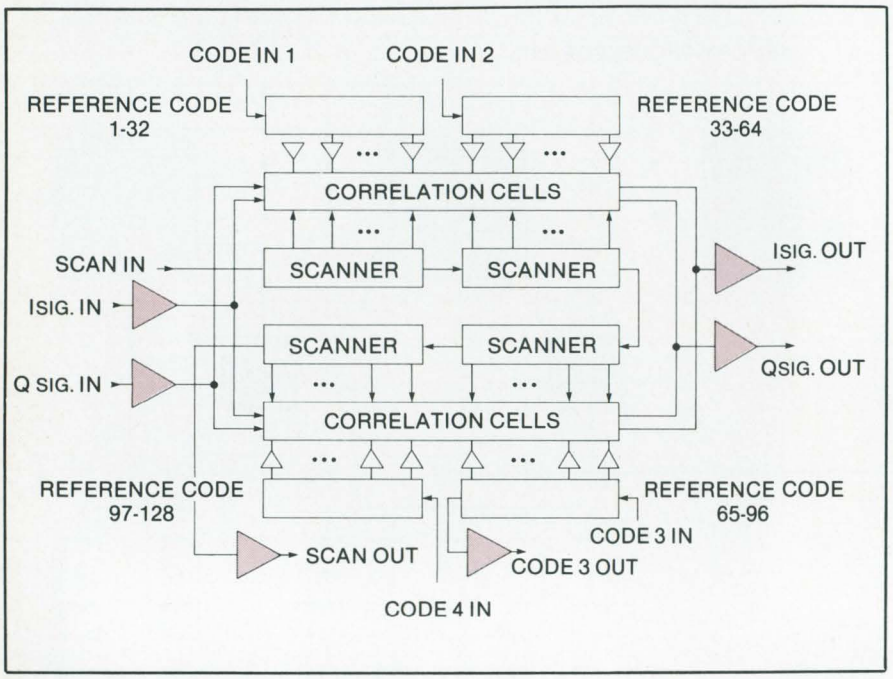


Figure 10: General Electric's correlator architecture.

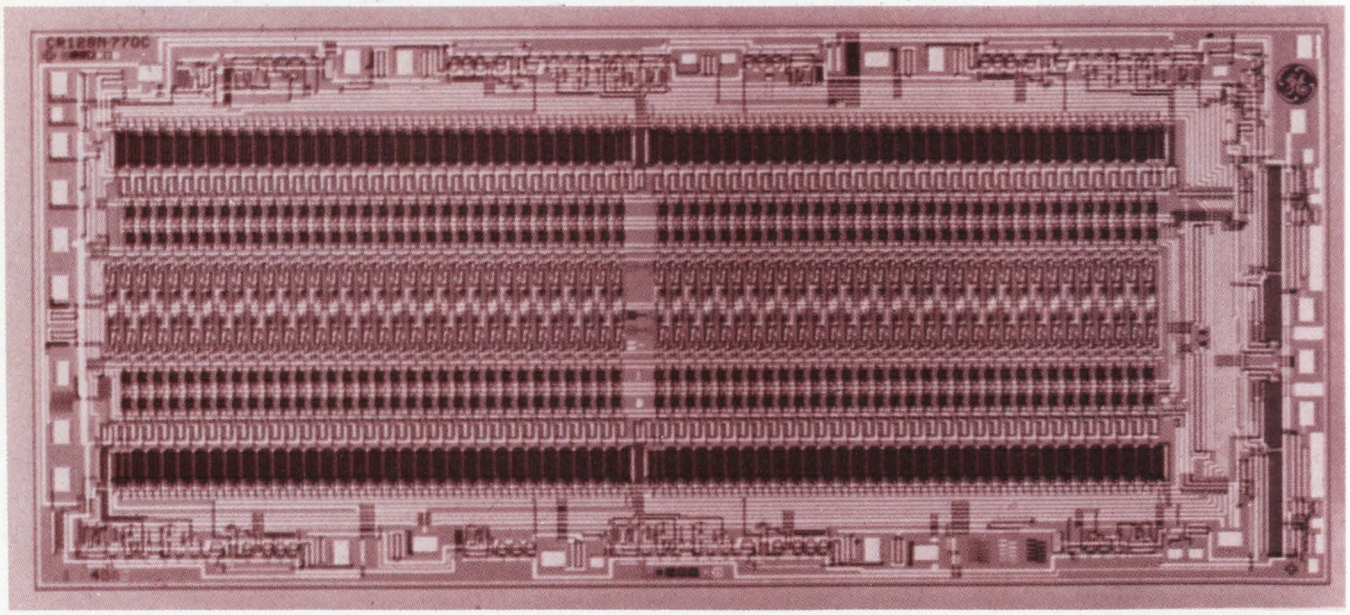
and the output driver converts from CMOS back to ECL levels. The input ECL to CMOS converter is a three stage sense amplifier circuit. A differential pair is used to provide an initial voltage gain and a comparison to the proper switch point reference voltage. Cross coupled N channel devices in the second stage provide additional gain and also shift the levels downward. The third stage is a current mirror buffer which provides full MOS level swings to subsequent circuits. Delay time for ECL to MOS conversion is typically 4ns. To achieve this high speed conversion, 65% of the total chip power has been allocated to the 15 input converters. Input stage offset is typically 40mV or less, from one pin to any other, and an input drive to the converter of 100mV is sufficient to achieve full CMOS levels.

The second of the Intel papers, from Mr. R.J. Smith, described the coupling of redundancy and laser fuse programming techniques to achieve memory array bit counts on mature technologies. Intel's approach is to design MOS memories using 4μm design rules and conventional projection printer lithography with large die sizes and multiple redundant elements. Using this approach, both a 4K x 8 and a 2K x 8 fully static RAM were designed.

The use of redundant techniques increases the die size which is most cost effective for a given technology. **Figure 13** shows how the use of redundant elements can be used to lower the minimum cost per bit on a particular technology by 62% while increasing the corresponding die from 153 mils square to 226 mils square. The minimum in the curve is very close to the die size required for a 16K memory, and for this reason, the 2048 x 8 bit MOS RAM was fabricated on the technology used for this illustration.

Laser techniques for programming fuses and encoding spare elements were chosen for these circuits because they offer several advan-

Figure 11: GE correlator-believed to be the first that has been operated from −55°C to +125°C.



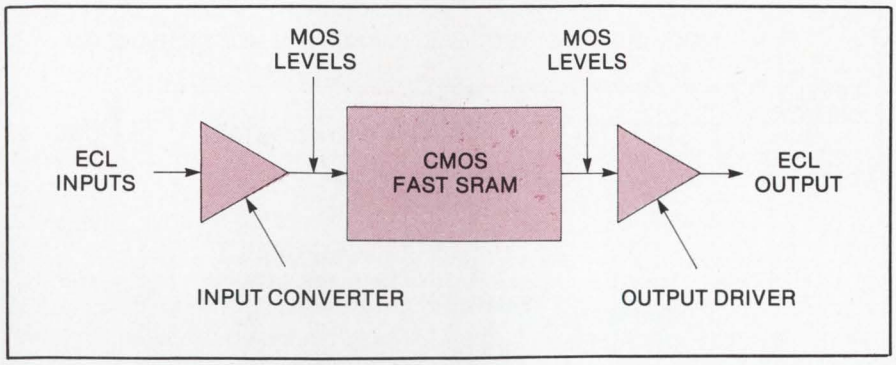
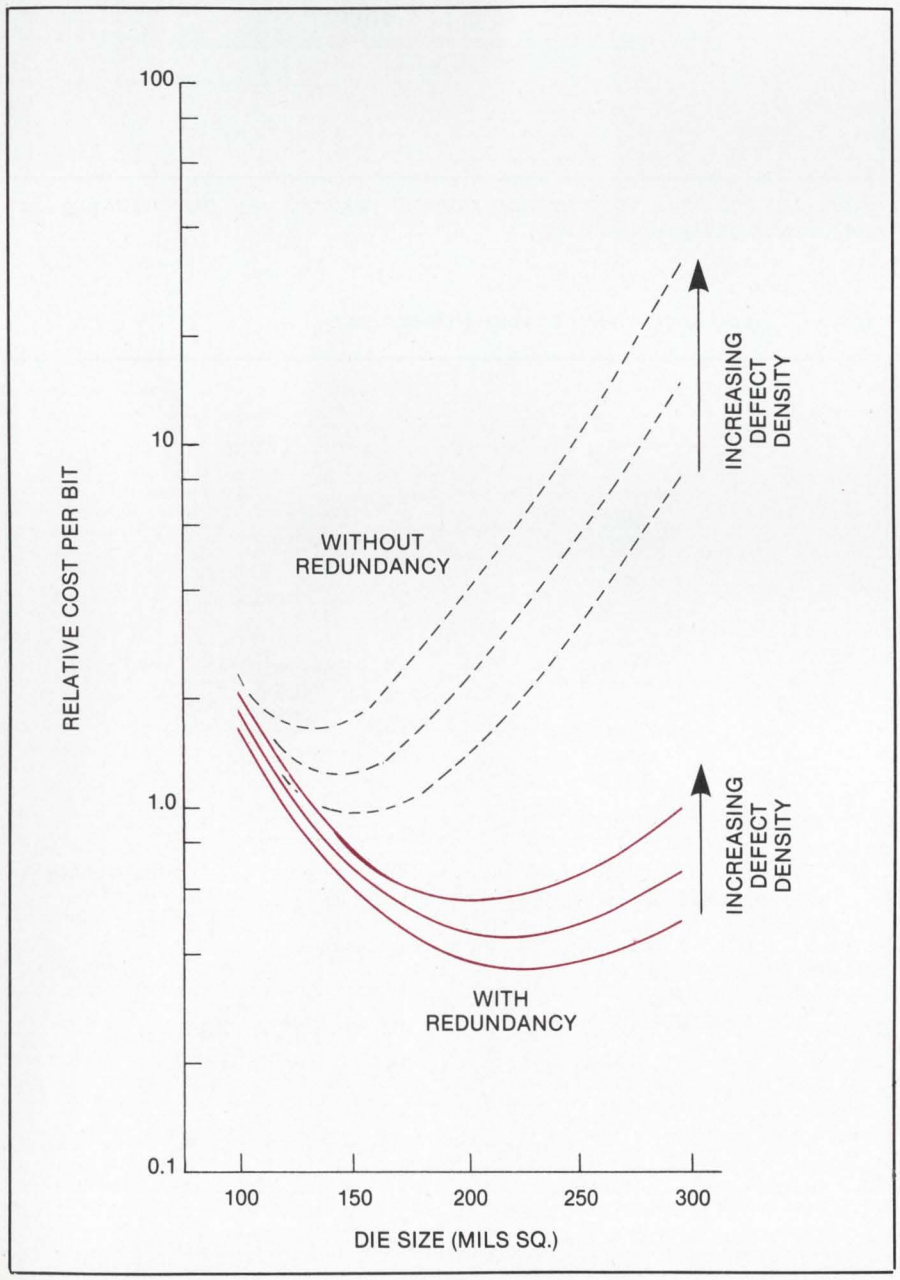


Figure 12: Circuit block diagram from Intel. Internally the memory uses normal MOS circuits and voltage swings.

Figure 13: Using redundant elements to lower cost per bit.



tages. For example, laser blown fuses can be added as part of active circuitry in series with signal paths, which allows greater design flexibility and reduces circuit device count; no high voltages or extra pads are required to blow fuses; laser techniques reduce the amount of non-repairable chip real estate; and finally, greater fuse programming flexibility allows fuse selectability of special optional circuit features.

Lastly, Anne V. Ebel, also from Intel, spoke of a 16K x 1 bit static RAM generated as the yield and development model for a double-poly NMOS technology. In addition a 64K bit static RAM was designed, with the implementation of redundancy for yield enhancement. The 64K device is organized as an 8K x 8 bit RAM with the array split into two planes of 130 columns by 260 rows. (Including the redundant elements separated by a common row decoder.) Both devices are TTL compatible and fully-static with a single 5V power supply. The 8K x 8 RAM has common I/O pins and fits in a standard 28 pin package, while the 16K x 1 RAM has separate I/O pins and fits in a 20-pin package.

From Japan, Kenji Anami of the Mitsubishi Electric Corp. outlined a new 16K static RAM. 16K NMOS static RAMs with a typical access time of less than 50ns have long been required for improvement of system performance; however, several 16K RAMs have been reported that suffer from a high operating and standby power consumption, according to Mr. Anami.

He went on to describe an NMOS 16K x 1 fully static RAM that boasted 35ns access time, 275mW operating power and 22.5mW standby power. In conclusion, he added that the low operating power and small chip size allow the RAM to be molded in a low-cost plastic 20-pin package.

Speech Processing

Headed by Mr. Brodersen, University of California, the speech processing session presented a dynamic array of new developments. For Texas Instruments, Japan, Mr. Takashi Takamizawa presented a

Voice chip allows the use of lower voice digitization rate while providing real-time operation.

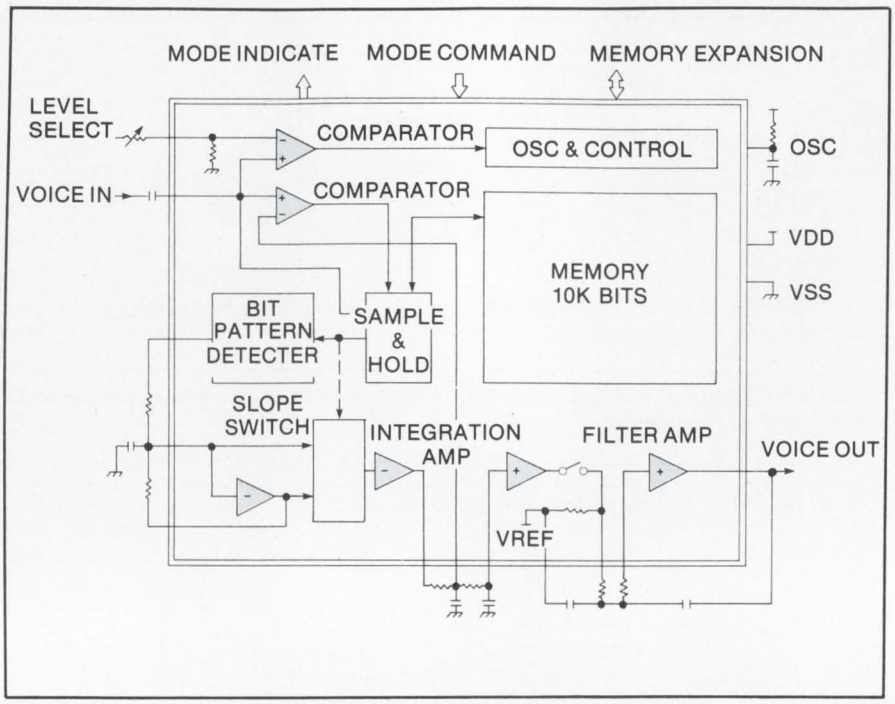


Figure 14: This voice recorder chip from TI performs real time recording and reproduction of the human voice.

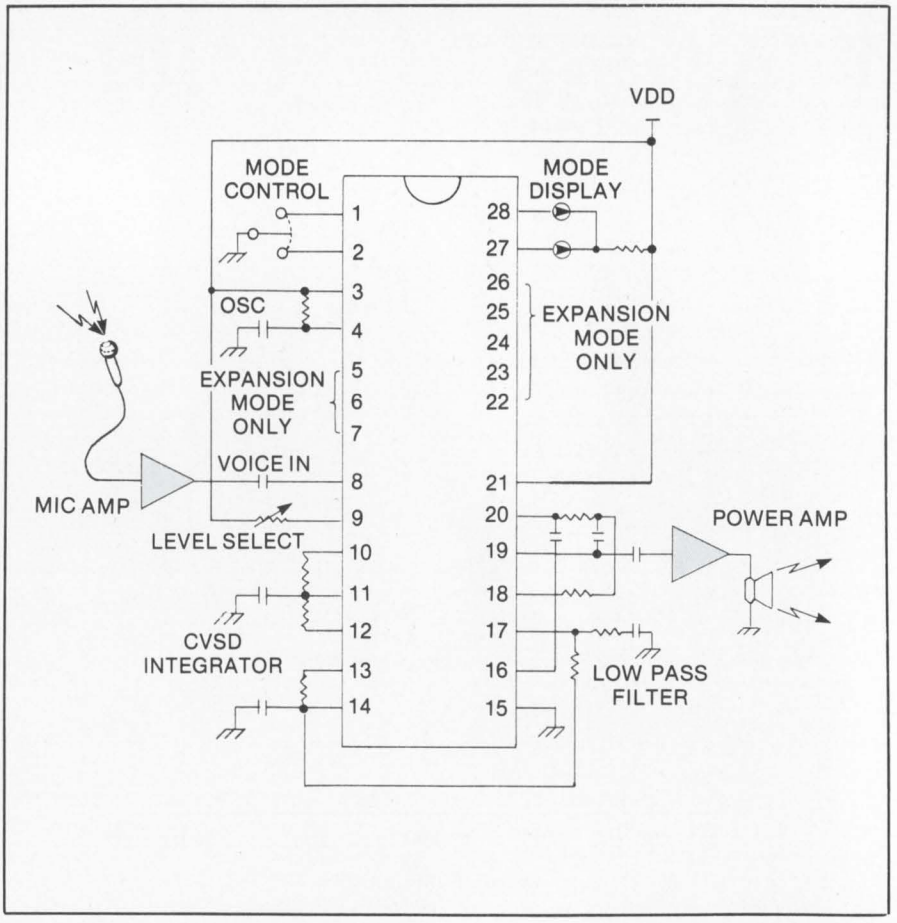
monolithic voice recorder performing real time recording and reproduction of the human voice.

To realize on-chip integration, voice digitization is achieved by continuously-variable-slope delta modulation (CVSD). This technique allows the use of a lower voice digitization rate (VDR) as compared to other wave-form reconstruction methods, while still providing real time operation, as opposed to analysis/synthesis methods such as linear predictive coding.

The chip consists of 10K bits dynamic memory, four operational amplifiers, two comparators, a delta modulator and control circuits as shown in **Figure 14**, and is fabricated by low cost metal gate PMOS technology to ensure high manufacturing yields and reliability. In order to achieve a minimal chip size, a unique dynamic shift register bit composed of three minimum size transistors with only three bus lines (data, address, ground) was developed.

A typical application circuit is shown in **Figure 15**. Reproduced voice wave forms are compared with the original input where the VDR frequency is varied from 4KHz to 12KHz. For longer recording times, the device is equipped with a memory expansion mode and can operate either as a master chip or as a slave chip defined by the mode control pin.

Figure 15: Application circuit for voice recorder chip.



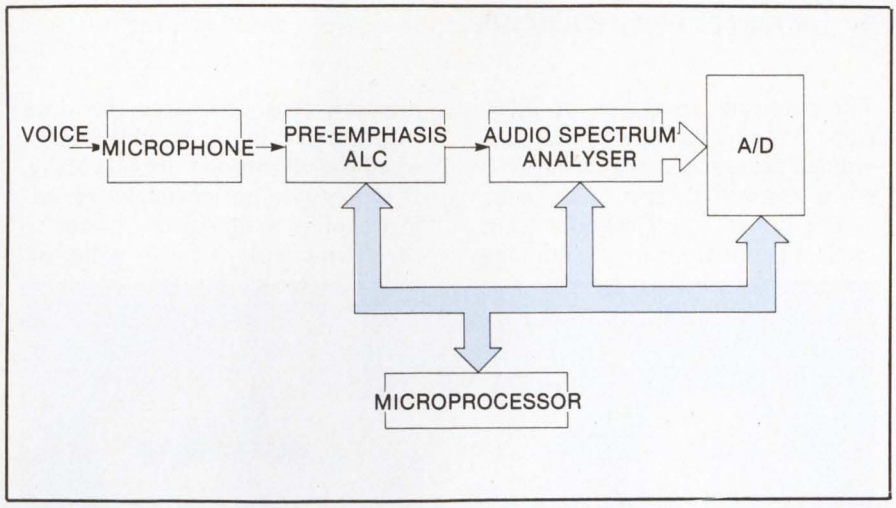


Figure 16: Analyzer of voice recognition systems.

A functional block diagram of the analyzer section of a typical speech-recognition system is shown in **Figure 16.** After a voice signal is frequency-emphasized and level-adjusted, it is applied to a spectrum-analyzer chip. The outputs of the chip represent the corresponding amplitudes of the frequency components of the incoming voice signal over sixteen predefined bands of a filter bank. The amplitude outputs can then be externally digitized, encoded, compressed and compared with a set of reference data. A variety of algorithms can be used to determine the similarity to this data, thus achieving recognition. Mr. Lyon Lin detailed such a monolithic audio spectrum analyzer chip built at EG & G Reticon, CA.

On chip, the extraction of amplitudes corresponding to each channel are accomplished by passing the signal through sixteen parallel channels; each contains a second-order Butterworth band-pass filter (BPF), a precision half-wave rectifier, and a second-order Butterworth low-pass filter. The device was designed to operate with a ±10V power supply and the chip draws about 35mA.

Dynamic time warping is an established technique for time alignment and comparison of speech segments in speech recognition. Backing up a series of articles on the subject (Proc. IEEE Conf. Acoustics, speech & signal processing, March 30, 1981; Proc. IEEE 8th Annual Symposium on Computer Architecture, May 12-14, Minnesota, 1981), Neil Weste, David Burn and Bryan Ackland described a simple programmable processing element **(Figure 17)** which, when configured in a systolic array, performs the task of comparing unknown utterances against a dictionary of references at least two orders of magnitude faster than conventional processing techniques. The processor architecture consists of a 16-bit register/arithmetic LOGIC unit (RALU), a RAM microcode store, a Control section and some single bit data routing circuitry. The RALU uses two 16-bit operated buses and a result bus. The control store consists of a 32-bit by 32 word static RAM. RAM microcode controls data pathways, arithmetic operations and register addressing. Special arithmetic functions include minimum value, absolute value, iterative multiplication and a logarithm multiplication.

Concluding, Mr. Weste cited a typical speech recognition problem consisting of performing a sum-of-product and logarithm calculation on a 9-D LPC feature vector. Assuming a microcycle of 180ns, each unknown reference word comparison will require 41ns. This is equivalent to a recognition rate of 25,000 words per second. Existing systems, he said, only deal with 50 to 100 words per second.

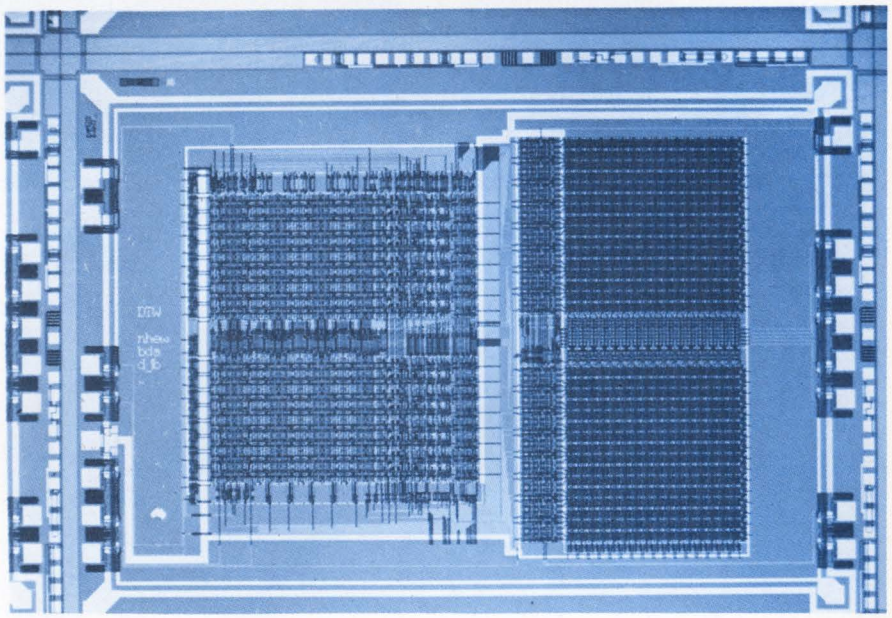


Figure 17: Bell Labs' processing element, believed to be the first for computation on an array basis.

Further Details

For further details about the Technical Digest for the ISSCC, write to Lewis Winner, 301 Almeria, Coral Gables, FL 33134.

Two Pen Plotter Scales Down Technology

To eliminate the problems associated with heavy moving arms and paper transport drums and belts, the designers of the new HP7470 graphics plotter have incorporated what they call a micro-grip drive system, a technique first proven last year with the HP7580A 8-pen color drafting plotter.

Micro-grip drive involves moving the drawing medium in one direction (the x-axis) while the drawing pen travels in the second direction (the y-axis). The drive consists of two rotating metal grit wheels that hold each edge of the drawing medium firmly against a hard rubber pinch wheel.

To enable a continuous record to be made of pen location, an optical encoder has been designed onto the two DC motors that drive the x and y axis.

The encoder consists of an LED source, a 500 slit encoder disk attached to the motor shaft, a phase plate and a photodiode detector. The resulting resolution of 2,000 steps per revolution helps to provide an accuracy in distance traveled by either the paper or the pen.

The optical shaft encoder feeds back its position to a summing junction that compares the data with the plotting program processed by the μP through the gate array. If the two do not correlate, an adjustment is made in the power to the driving motor. **Write 201**

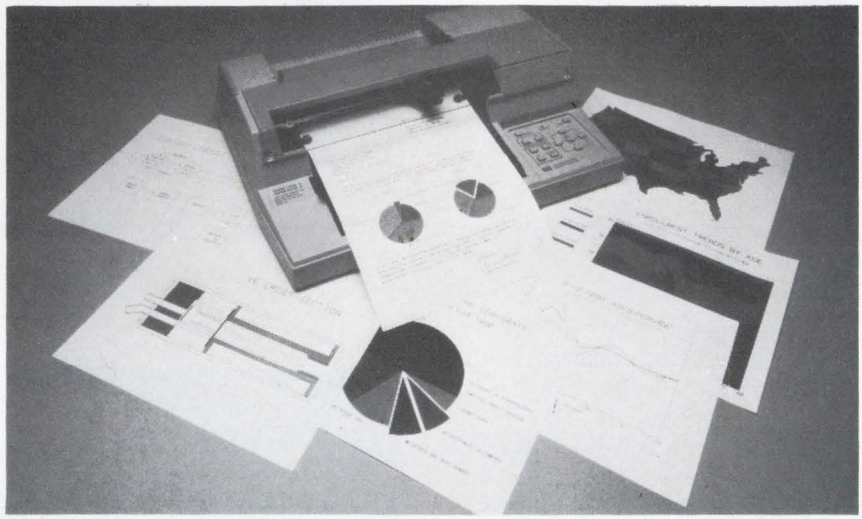


Figure 1: The HP7470 pen plotter can be connected to a variety of computers to produce high-quality business and technical graphics on overhead transparency film and paper.

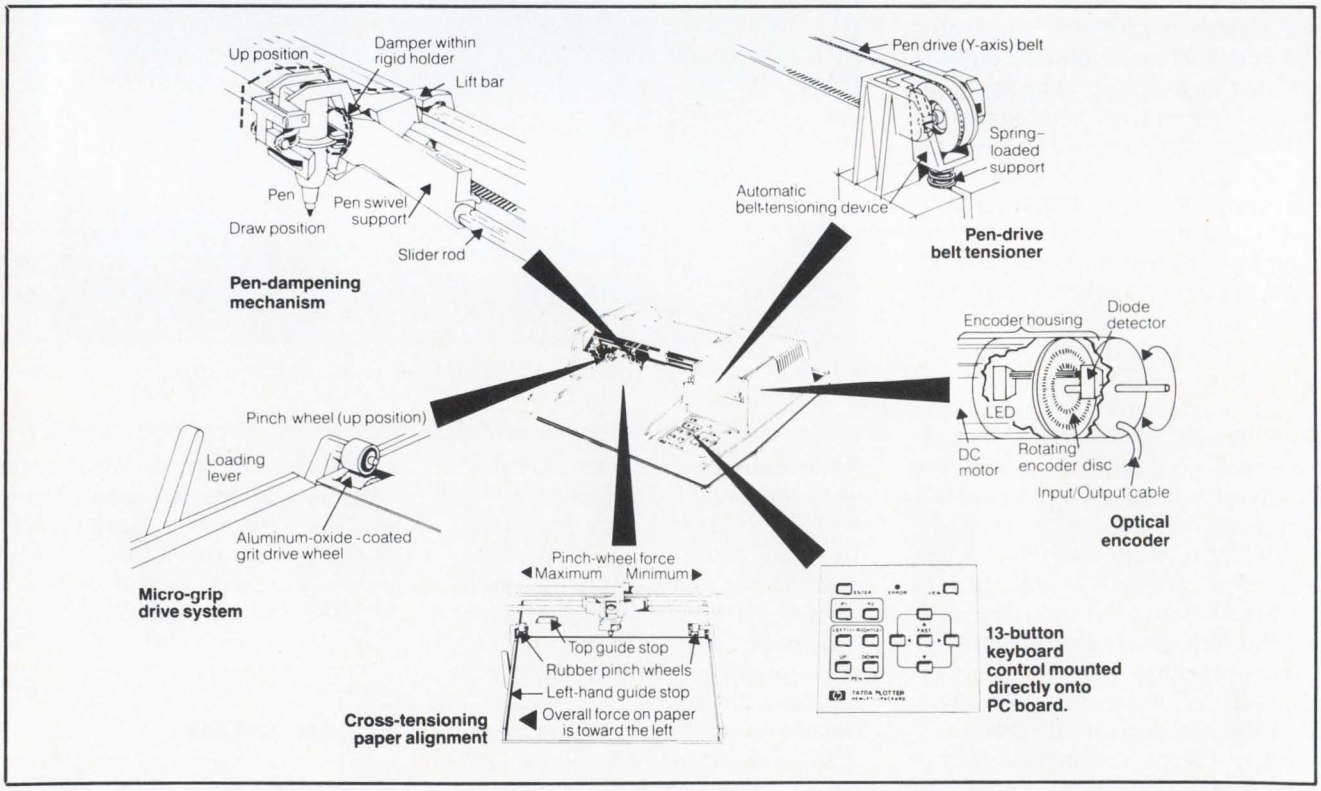


Figure 2: The HP7470 plotter incorporates a number of innovative ideas to match the speed and accuracy of larger more expensive plotters.

Ethernet Family Allows Direct Computer Connection To LAN

Projected annual sales in the local area network marketplace are due to reach $3.2 billion by the end of the decade, according to Interlan, a designer and manufacturer of local area network products.

Interlan has targeted three primary markets: office communications, operations communications and facilities management. Initial study has indicated that specific application areas like CAD/CAM, factory data collection, financial flow, sophisticated text editing and text processing may be the innovative fields in the application of local area network technology.

The company is developing controller boards and software for the Ethernet and the IEEE Standard 802 local area networks. These products allow PDP-11, VAX-11, LSI-11 and Multibus-based computers to be connected through a local network. Network protocol-specific circuitry is packaged on a universal board that may be combined with bus-interface boards for Unibus, Q-bus or Multibus to form a complete controller, or offered separately for users who wish to integrate into their own system. This universal board, the NM1O, performs the specified data link and physical channel functions permitting 10Mbit/sec data communications to take place between stations separated by 2500 meters.

The NI1010 and the NI2010 are the Unibus and the Q-bus, Ethernet controller boards, respectively. By way of example we will look at the NI1010 Unibus board in some detail. As shown in **Figure 1**, the board, when attached to a transceiver unit, provides VAX-11 or Unibus-based PDP-11 a complete connection onto the Ethernet local area network.

Within the Data Link Layer the NI1010 performs the specified Ethernet transmitter processes of Transmit Data Encapsulation and Transmit Link Management, and the Ethernet receiver processes of Receive Data Decapsulation and Receive Link Management.

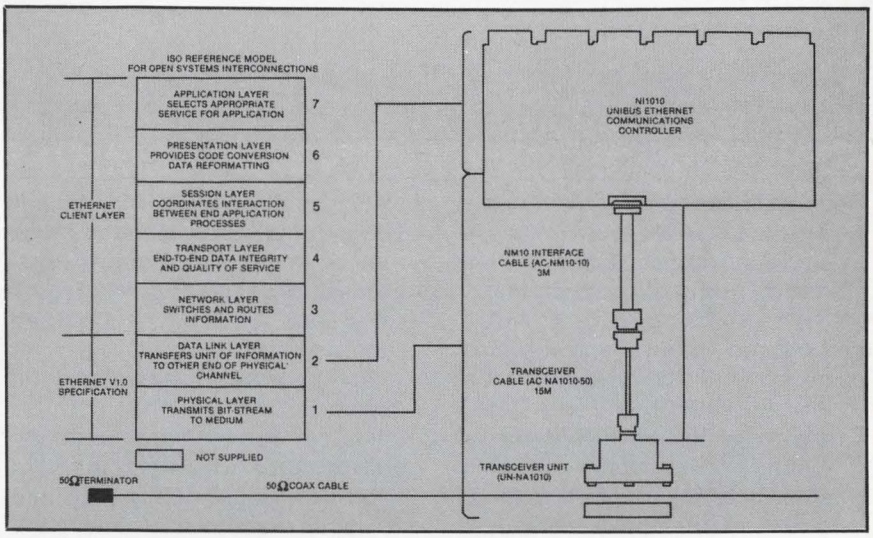


Figure 1. Ethernet Architecture and Implementation

Transmit Data Encapsulation

Figure 2 shows the Ethernet Frame Format for packet transmissions over the coaxial cable physical channel. For receive synchronization purposes, the frame is preceeded with a 64-bit preamble sequence and terminated with a minimum interframe spacing period of 9.6μ secs.

The Destination Address field specifies the station(s) for which the frame is intended. The address value provided by the user may be either: 1) the physical address of a particular station on the network; 2) a multicast-group address associated with one or more stations; or 3) the broadcast address for simultaneous transmission to all stations on the network. The first bit of the Destination Address distinguishes a physical address from a multicast address (0 = physical, 1 = multicast). For broadcast transmissions an all one-bit pattern is used.

The Source Address field specifies the physical address of the transmitting station. To eliminate the possibility of an addressing ambiguity on a network, associated with each NI1010 is a unique 48-bit physical address value assigned to it at the time of manufacture. On transmission, the NI1010 inserts this value into the Source Address field.

The Type field is specified by the user for use by high level network protocols. It specifies to the receiving station(s) how the content of the Data field is to be interpreted.

The Data field may contain a variable number of data bytes ranging from a minimum of 46 bytes to a maximum of 1500 bytes. The NI1010 accepts less than 46 bytes from the user by automatically inserting null characters to complete a 46-byte minimum frame size.

The Frame Check Sequence (FCS) field contains a 32-bit cycle redundancy check (CRC) value generated by the NI1010 during transmission.

Transmit Link Management

The NI1010 performs all Ethernet Transmit Link Management functions required to successfully deliver a frame onto the network. These functions include:

- Carrier Deference; the NI1010 monitors the physical channel and defers its transmission should the channel be busy carrying other traffic.
- Collision Detection; once the NI1010 has finished deferring to the passing traffic on the network, it proceeds with its own transmission. In the event that

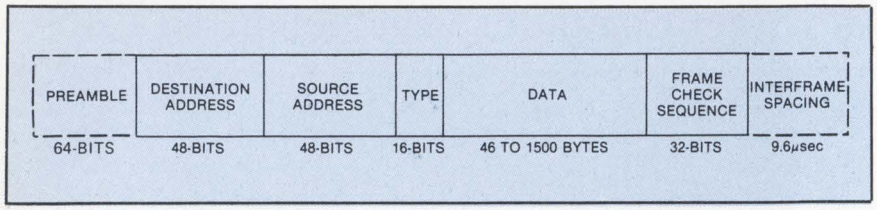


Figure 2. Ethernet Frame Format

another station simultaneously began a transmission, a "collision" occurs. The NI1010 detects this event and terminates its transmission attempt.

- Collision Backoff and Retransmission; when a transmission attempt has been terminated due to a collision, the NI1010 attempts its transmission again after delaying a short random period of time. The scheduling of the retransmission is determined by the Ethernet process called "truncated binary exponential backoff". The NI1010 reports an error should it be unable to deliver its frame onto the network after 16 transmission attempts.

Receive Data Decapsulation

When not transmitting a frame the NI1010 continuously listens to the traffic being carried on the network. After synchronizing to the preamble sequence of a frame on the network, the NI1010 processes the Destination Address field through its address filter logic to determine whether or not the incoming frame is intended for it. The NI1010 controller will only accept a frame from the network with a Destination Address value that either:

1) matches the physical address of the NI1010 board itself;
2) contains the broadcast address; or
3) matches one of the 63 multicast-group logical addresses which the user may assign to the board.

The NI1010 performs high speed multicast-group address recognition. Whenever a multicast-group logical address is received on the network, the NI1010 converts the frame's 48-bit Destination Address field into a 6-bit table entry pointer through the application of a many-to-few mapping called "hashing." It uses the resulting pointer to look into a table of valid multicast-group addresses to see if the received address is one that the station should accept.

For network management and diagnosis, the NI1010 may be operated in a "promiscuous" receive mode which permits it to bypass the address filter logic and accept all undamaged frames passing on the network.

The NI1010 validates the integrity of a received frame by regenerating the 32-bit CRC value on the received bit stream and comparing it against the CRC value found in the frame's Frame Check Sequence field.

Since collisions are a normal occurrence in the Ethernet's CSMA/CD link management process, the NI1010 receiver filters out collision fragments from valid frames.

Ethernet Physical Layer Functions

Within the Ethernet Physical Layer, the NI1010 performs the electrical and procedural specifications required for interfacing to a transceiver unit. Transmissions and receptions take place at a 10Mbits/sec data rate under half-duplex operation.

During transmission the NI1010's physical channel functions include:

- Generating the 64-bit preamble sequence for all receivers on the network to synchronize on;
- Parallel to serial conversion of the frame;
- Calculating a 32-bit CRC value and inserting it into the Frame Check Sequence field:
- Generating a self-synchronizing serial bit stream Manchester encoding of the data; and
- Providing proper channel access by detecting carrier from another station's frame transmission and sensing the collision presence signal from the transceiver unit.

The NI1010's physical channel functions during reception include:

- Manchester decoding the incoming bit stream into a data stream and a clock stream;
- Synchronizing to, and removal of, the preamble sequence; and
- Parallel to serial conversion of the frame.

Serving to buffer the system from the unpredictable interarrival times characteristic of network traffic, the board has a FIFO (first-in, first-out) memory which can store up to 16 Kbytes of received frames. Because of this front-end buffering, few time-critical service requirements are imposed on the host Unibus system.

For transmission, the NI1010 has a 2 Kbyte Transmit FIFO which permits the host to perform a one-time transfer of a frame.

All data block transfers between the NI1010 and Unibus memory are performed under the control of an onboard DMA controller. To maximize system performance during reception, the controller allows the user to preload up to sixteen different memory buffer address and byte count values for DMA of received frames.

Diagnostic Features

Mounted on the edge of the board are four network state LED indicators which provide a visual indication of whether or not the user's station is communicating onto the network. For a comprehensive station diagnosis, the user can exercise the NI1010's communication facilities in either internal and external data loopback mode; making it possible to detect and isolate a fault to the coaxial cable, transceiver unit, transceiver cable, or the NI1010 board itself.

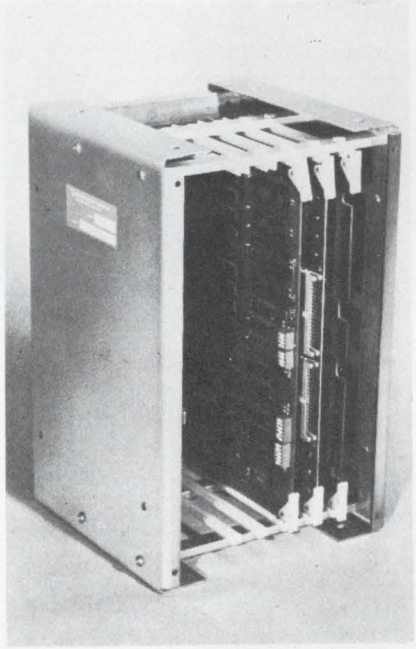
On power-up, the NI1010 performs a confidence test of the onboard memories, register and data paths. A LED indicator shows the pass/fail operational state of the board.

Write 202

MOTION PROFILE COMPUTER

Controls DC Servo Motor Drive Systems

Designed for OEM use with N/C machine tools, robotic assemblies and other positioning systems using DC servo drives, the Model MPC-1000 can store and control pre-programmed profiles, in one, two or three axes of motion. The standard unit controls position to an accuracy of 0.36° (or better, when high resolution encoders are used), and handles speeds up to



5000 RPM and accelerations to 30,000 RAD/sec². It can be accessed through any terminal keyboard and utilizes internal, plug-in PROM's that can be pre-programmed by the user with appropriate motion profile data. Several options are available to adapt the MPC-1000 to specific operating requirements. These include additional memory capacity, thumbwheel input software for manual selection of specific stored motion profiles, RAM memory with battery back-up, and other accessories. **EG & G Torque Systems**, 36 Arlington St, Watertown, MA 02172. **Write 194**

ACCESS UTILITY

For CP/M-80 Compatible 8080/Z80 Operating Systems

ZAP80, a powerful menu-driven disk/diskette access utility for SB-80 and other CP/M-80-compatible 8080/Z80 operating systems, automatically allows direct file viewing and patching by actual memory address. Especially designed for experienced users, this system includes extensive file utility servicing to access and patch file sectors, compare files and more. **Lifeboat Associates**, 1651 Third Ave., New York, NY 10028. **Write 222**

μP OPTION

Allows VT100 To Run CP/M Personal Computing Software

The VT18X gives the VT100 two distinct identities. Users can either use the VT100 as an I/O device to a computer system or, by pressing a single key, run stand-alone personal computing applications under CP/M. It includes a Z80-based μP module with 65,536 characters of internal memory, for mounting inside the VT100 cabinet, a dual mini-floppy (5-¼″) disk drive with 160,000 characters of data and program storage, connecting cables, user guide and documentation, and a diagnostic disk to check system performance. A second dual mini-floppy disk drive can be added for $1275. CP/M software license and documentation is $250. Also available are several software packages running

under CP/M developed by independent software distributors. These include WP, mailing list, financial modeling and statistical packages, and communications to external data base sources. The μP option is $2400. **Digital Equipment Corp**, Maynard, MA 01754. **Write 184**

DATA ENTRY SOFTWARE

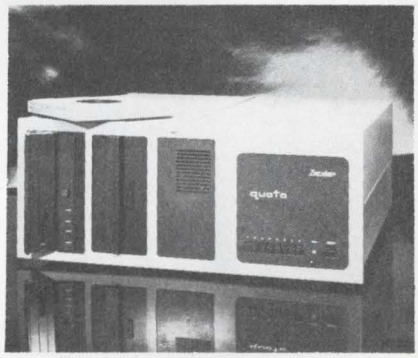
Strengthens 1600 Line In Distributed DP

KEYPLUS is an easy to use formatted data entry package allowing Harris 1600 users to increase operator productivity through advanced features such as conditional logic and branching, extended accumulator processing and ineligible field indication. With one system, a user can now execute remote or local batch processing, remote host interaction, local data base interaction, user-written applications in interactive COBOL and high-speed data entry routines. KEYPLUS may be operated on both local or remote stations attached to a 1600 processor. $65/month lease; $2860 object license fee. **Harris Corp.**, Data Comm Div., 16001 Dallas Pkwy., Dallas, TX 75240. **Write 221**

μC SYSTEM FAMILY

Flexible Configurations Of Up To 30.5MB Storage

The Multibus compatible Series 900, is an 8085A-2/8088 based turnkey system with CP/M compatibility, and off-the-shelf availability. The basic configuration provides 64K resident dynamic RAM for the 8085-based System 935.



This is expandable to 320K for multi-user environments. The 8088-based System 938 is provided with 192 kB of RAM, expandable to the full 1MB capability of the 8088 via on-board circuitry. Both systems have 4K ROM (2732A), and 11MB (unformatted) on-line storage. The storage subsystem incorporates two Shugart SA801R floppy drives, and an SA1004 8″ fixed Winchester hard disk. The System 955/958, with 20.5MB on-line storage, incorporates a single floppy and fixed Winchester, with an additional 10MB removable Winchester. The System 965/968 provides 20MB fixed, and 10MB removable hard disk storage, via a Data Peripherals DP-100 Lynx disk drive. If floppy drives are needed, Model 710/720 extender chassis can be integrated as part of the system. An 8086 CPU, Ethernet capabilities, and data communications applications will be developed for the Series 900. From $14,500 to $28,230; 1 yr. warranty. **Quota Systems Div**, Zendex Corp, 6680 Sierra Lane, Dublin, CA 94566. **Write 185**

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32MB MULTISHARE SYSTEM

Supports Up To 5 Workstations

The 5032 MultiShare features a 6 MHz Z-80B processor which speeds up processing time by 15 to 25% over a 4 MHz system, and RAM memory expanded to 128K which provides 56K per terminal for user applications and still leaves room for a new and extended version of a CP/M operating system. Extended CP/M capabilities are print spooling, a feature which permits simultaneous data entry and printing, thus adding to the 5032's multitasking capabilities. With its time-sharing capabilities, different applications can be performed simultaneously by up to 5 operators at locations up to 100' from the central processor. A serial and a parallel printer can be supported and operated simultaneously. It is equipped with standard Vector software and optional Memorite III WP and ExecuPlan II financial modeling software packages. It also utilizes a 32MB 8" Winchester hard disk. An integral 630 kB floppy disk provides compatibility with programs and data from other floppy disk Vector microcomputers. Basic configuration starts at $13,995. **Vector Graphic Inc,** 500 N. Ventu Park Rd., Thousand Oaks, CA 91320. **Write 233**

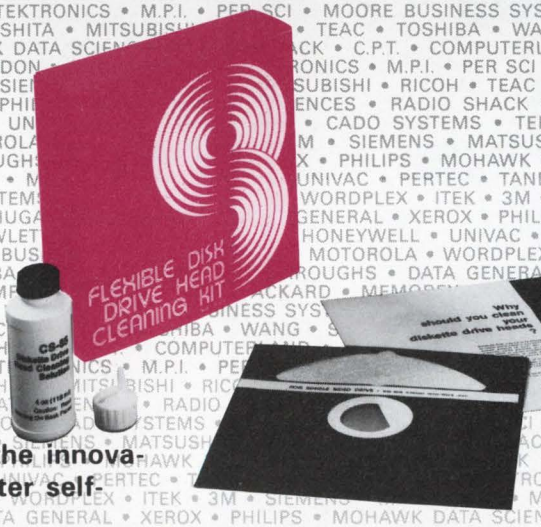
COLOR CAD SYSTEM

Designed For Development Of VLSI Circuits

The GS1220 is a color version of the Avera system, a desktop stand alone CAD system that provides the circuit

designer or engineer with an interactive workstation for electronics drafting and schematic capture. The system incorporates a powerful comprehensive graphics editor and a flexible data structure. A wide range of command modifiers makes available hundreds of options for maximum flexibility and precise specification of necessary operations. The data structure of the system has been optimized for hierarchical design and features a unique associative capability offering increased flexibility through having various items associated with one another. This allows the designer to, among other things, nest cells within cells up to 16 levels. The GS1220 incorporates a 488 x 668 pixel color display, of which 464 x 464 are devoted to the graphics area. The rest of the display is devoted to menu boxes, an on-line reference guide, and the user response area. The display is refreshed at 30Hz interlaced and uses long persistence phosphors. The screen features two color tables; hardware-controlled area fill; outline color control; overlap control; dominant color; and, background color control. It utilizes 8 basic colors and combines these to provide a total of 256 shades. $55,250. **Avera**, 200 Technology Circle, Scotts Valley, CA 95066. **Write 205**

WHAT HEAD CLEANING KIT DO THESE COMPANIES RECOMMEND?



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DIGITAL OUTPUT MODULE

Provides 16 Discrete Drivers

The DMS221 is a 16-bit digital output module that provides an interface between low-level μP circuitry and high power peripheral loads in industrial control applications. The 16 discrete outputs have open-collector drivers, each capable of sinking 100mA continuous or 500mA peak, and are able to sustain voltages up to +50VDC. Packaged in a small (2.50" x 2.00" x 0.375"), rugged epoxy encapsulated module, it is compatible with the COLUMBUS component level μP bus. This enables the DMS221 to be connected to all popular 8-bit or 16-bit μPs with a minimum of additional components. The logic control circuitry is CMOS, giving high noise immunity and low power consumption. Independently addressable 8-bit input latches and 3-state buffers provide ease of interface to μPs that can output only an 8-bit byte. The wide range of the logic supply voltage (+4V to +12V) permits direct TTL or CMOS compatibility on the COLUMBUS data bus and control lines. **DI-AN Micro Systems Ltd.**, Mersey House, Battersea Rd., Heaton Mersey, Stockport, Cheshire. SK43EA. UK. **Write 234**

EMULATION SYSTEM

Supports 8- And 16-Bit μP's

The universal emulator incorporates a standard mainframe with plug-in control cards and pods which tailor the

unit to specific μP families. It supports Zilog's Z-8001; support is also planned for other 8- and 16-bit devices: 68000, 8086, 8088, Z-80B, 6800, 6802, 6809, 8080, 8085 and 8048. Communicating via two RS-232 ports, the Satellite Emulator can hook up to a user's present development system, minicomputer or automatic test system. Thus it upgrades existing equipment with more sophisticated hardware/software integration and debug capabilities, and supports new μP design starts. For stand alone operation the emulator, coupled with any ASCII CRT terminal, accepts software programs developed on the user's host system. Then, while debugging is being performed on the emulator, the host is free for other complex design tasks. From $6400 to $9500. **Applied Microsystems Corp.**, 11003 - 118th Place NE, Kirkland, WA 98033.

Write 230

RS-232 LINE TESTER

Pinpoints Transmission Difficulties

The pocket-size device connects between the user's equipment and the communication line to differentiate 12 different signals. Interface pins can be cross-patched with the tester's connection jumper wires to test and correct problems. It will cut repair cost by pinpointing transmission difficulties

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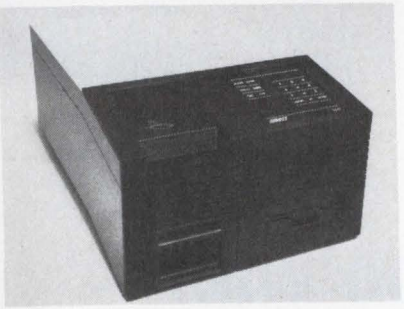
before a technician is called by determining whether the modem, computer or transmission line is at fault, which signals are in error, and what system modifications should be made. It features a supplementary power supply from two 1.5W penlight batteries to eliminate errors caused by power drain. An EIA/CCITT conversion chart is included. The RS-232 I/O Tester is $199 (1); $185 (2-4); $175 (4+). **Inmac**, Dept. 34, 2465 Augustine Dr., Santa Clara, CA 95051. **Write 227**

DISKETTE COPIERS

Combine Industrial To Personal Diskette Copying With Office Flexibility

Both the 5208 and 5248 automatic desktop units are designed for duplicating and verifying single- and double-sided 5-¼", 48 tpi diskettes in an operator-selectable quantity from one to 999 copies. An automatic accept-reject output stacker is common to both. The 5208 performs as a peripheral subsystem, and is compatible with personal and business computers via an RS232 serial interface. Because it is under host computer control and user command, software integrity is maintained by the host. The 5248 is a stand alone



copying system for both single and/or double sided diskettes encoded in "known" formats in single and/or double density. Optional intelligence may be added to the system with Specific Personality Modules. Custom personality modules are also available. Under $10,000 for the 5208, approx $13,000 for the 5248; qty discounts avail. **Media Systems Technology**, 17991 Fitch Ave., Irvine, CA 92714.

Write 238

PRINTING SYSTEM

40 CPS Printing For IBM 34/38 Minis

The letter quality printing system consists of a BDS LQ40 printer and a Model IPI-34 interface housed in the LQ40. The bidirectional printer has 132 column spacing with 10 cpi, 158 columns with 12 cpi, or 198 columns with 15 cpi. Character spacing is switch selectable. Maximum form width is 16.0" with up to 6 part forms. Vertical spacing, under program control, is variable in 0.021" increments. Carriage speed is 400 ms for 132 columns, paper feed speed is 4 ips. The printer accepts interchangeable plastic and metal print wheels to provide a wide variety of fonts and languages. Options include a pin-feed platen, unidirectional and bidirectional tractor feed, single- and double-tray sheet feed, and a dual envelope tray. The LQ40 printer and interface is $4695. **BDS Corp.**, 115 Independence Dr., Menlo Park, CA 94025.

Write 232

WHEN SPEED IS OF THE ESSENCE... OUR MODEL 130 COUPLER IS FASTER THAN EVER!

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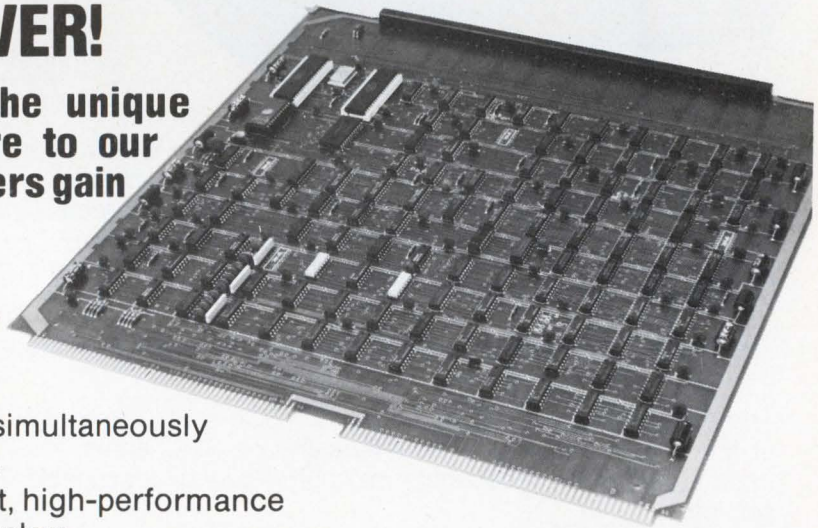

No software modifications are necessary with the Model 130 Magnetic Tape Coupler.

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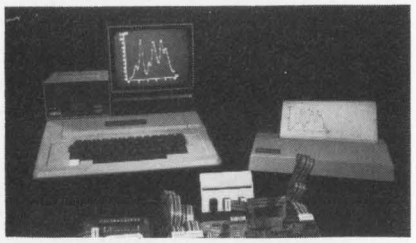
212A-COMPATIBLE MODEMS

Full Duplex Operation Over Dial-Up Lines



The MT212A is a dual-speed 1200 and 300 bps replacement for the Bell 212A. The MT212D is a 1200 bps-only version with full 212A compatibility. They are available in stand-alone and rack-mounted configurations, and provide originating and automatic answering capability. Voice to Data transferring is accomplished with a push button on the modem chassis, eliminating the need for special 502 exclusion key phones and adaptors. For originating applications, the user's telephone set can be connected directly to the modem, and the modem can be connected to the phone line using either RJ11 or RJ45 modular connections. The MT212A is $850, the MT212D is $695. **Multi-Tech Systems Inc.**, 82 Second Ave., SE, New Brighton, MN 55112. **Write 236**

The Hecon with the Hopper.

The Hecon A0542 impact dot matrix ticket printer with hopper feed. Load up to 75 tickets in the easily accessible hopper. When you are ready to print, the A0542 automatically feeds, prints and transports the ticket for removal. You can even reinsert a ticket for additional printing thru the unique reprint feed slot.

The highly visible Time and Date feature is standard and can be printed with a single command.

The A0542 can print the 96 character ASCII set bidirectionally at 120 characters per second. The standard print head is rated at 200 Million characters minimum for long, dependable service.

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8" WINCHESTER DRIVES

Support Multi-Station Business And WP Systems

Featuring ANSI interface, the TrakStar is available with 33, 67 and 84MB capacity. The D-8033 records on 476 tpi, the 8066 and 8084 on 952 tpi, with all three recording at 8200 bpi. They have an average positioning time of 45 ms, and a data transfer rate of 8.5 Mbits/sec. The voice coil rotary head positioner provides a single cylinder move time under 10 ms, including settling time, 80 ms full stroke and random access (average) time of 45 ms. The closed loop servo system offers high track accuracy. The positioner is provided with automatic head retraction to a dedicated landing zone when power is turned off or inadvertently lost. Under $2000 in OEM qty. **Pertec Computer Corp.**, Peripherals Div., 21111 Erwin St., Woodland Hills, CA 91367. **Write 240**

DIGITABLET

Enhanced By Many New Programs

New features of the #2400 tablet digitizer in the software area include data flagging, cursor control that allows the user to output data to the host in engineering units while controlling cursor position on a graphics screen, data formatting and preparation, downloading of all digitizer operation parameters including operating mode, menu function & dimension and prompts, and digitizer/host interaction and communication including menuing, data input and status request. It also features a menu area that can also be used as normal working space, and a dual I/O port for two simultaneous interfaces. **Numonics**, 734 Pine St., Philadelphia, PA 19106. **Write 228**

UNINTERRUPTIBLE DC SUPPLY

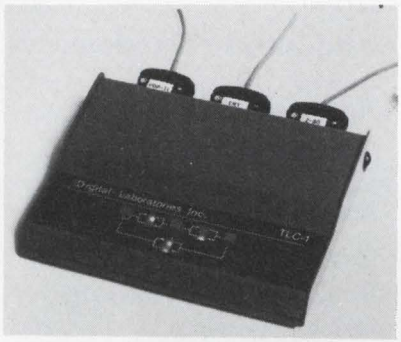
For Winchester Disk Based Computer Systems

The EHV-150 provides glitch free transfer to onboard battery power in the event of AC line loss. The onboard battery pack allows holdup times of 8 minutes to 1.5 hours depending on load. Longer holdup times are available with the optional battery pack. Standard outputs are 5V at 25A and 24V at 9A. Also included are 3 other fully regulated outputs tailored to specific user requirements. Total available power is 400 W. TTL compatible signals indicate battery failure, AC line loss, low battery and overtemperature conditions. The EHV-150 includes delayed shutdown and startup logic and occupies 5¼ " of space in a standard 19" rack. OEM price $875. **EHV Systems Inc,** Terminal Rd, Setauket, NY 11733. **Write 218**

3 PORT DATA SWITCH

Features 63 Connection Arrangements

For routing data between 3 RS232C ports in any combination, the TLC-1, a self-contained unit with push button control and LED displays, operates through CMOS logic circuits rather than mechanical contacts. 63 communication arrangements are possible, compared with the two of an "AB" mechanical port switcher. For example, the TLC-1 allows transmitted and received data to be switched separately creating a "port splitting" feature that allows one terminal to move data between two computers. Existing software such as line editors can be used in conjunction with port splitting. Six control bits, each indicated with a LED, direct the data movement between the TLC-1's ports. Each bit, activated by push buttons, connects one port's transmitter to another's receiver. $245 (1-4). **Digital Laboratories Inc,** 600 Pleasant St, Watertown, MA 02172. **Write 217**



CMOS 4K STATIC RAM

Pin-For-Pin Replacement For The Harris HM6504 RAM

The MP6504 has a true standby supply current value of only 1μA and while in the idle or non-switching state the value is only 40μA. It has a 4096x1 memory configuration, a 250ns access time, interfaces with a number of μP's and is pin-compatible with the industry standard 6504. Each device is powered from a single +5V supply. Data is retained even when power drops to as low as 2V. The absolute maximum voltage of 7V allows for 4, fully- charged, 1.5V batteries in portable product applications. Inputs and output are fully TTL compatible. A tri-state output and on-chip address registers allow easy interfacing with μP-based designs. 100-piece price for the MP6504 is $6.25 (18-pin plastic). **Micro Power Systems,** 3100 Alfred St, Santa Clara, CA 95050. **Write 226**

Looking for an easy-to-integrate, economical print mechanism?

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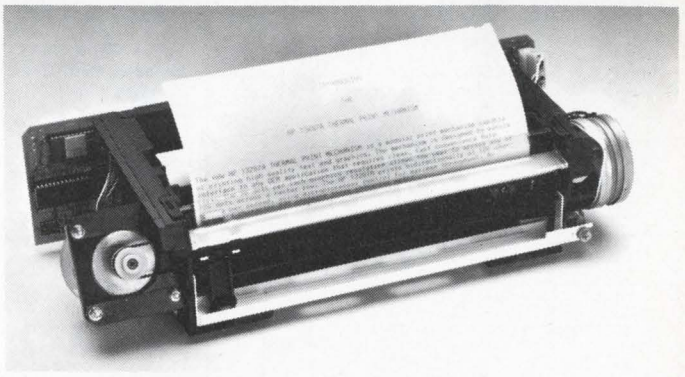

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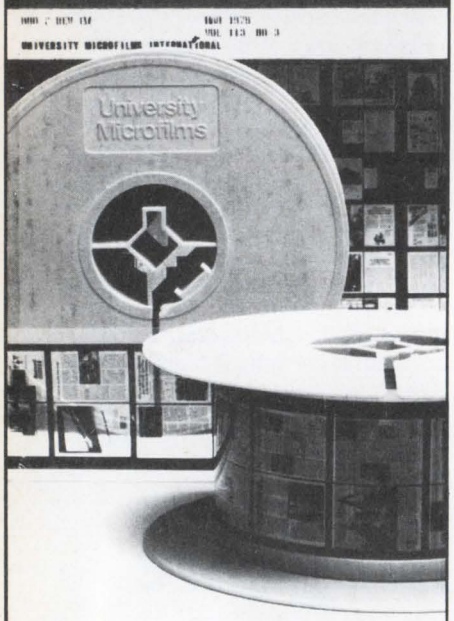

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City _____

State _____ Zip _____

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Dept. P.R.
Ann Arbor, Mi. 48106
U.S.A.

30-32 Mortimer Street
Dept. P.R.
London W1N 7RA
England

Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

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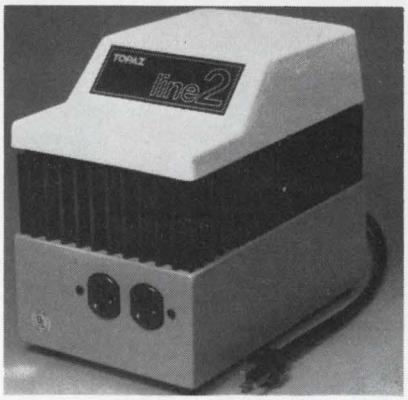
POWER CONDITIONERS

For Small Business Applications

Line 2 Power Conditioners are available in power ratings from 400 VA to 2000 VA and give small business computers complete protection against power line noise, voltage sags and surges — even brownouts. These self-contained, portable units combine the noise suppressing capabilities of an Ultra-Isolator with the voltage regulation properties of an AC Line Regulator. Together these features provide protection against costly power-related problems such as computer memory losses, program errors, system malfunctions and downtime. The Line 2 simply plugs into the existing 120V outlet to eliminate the need for expensive fixed-wire installation. They feature excellent dynamic regulation, low output impedance, one-cycle response time and energy-saving 94% efficiency. **Topaz Electronics Div,** 9192 Topaz Way, San Diego, CA 92123. **Write 244**



TOUCH PEN SYSTEM

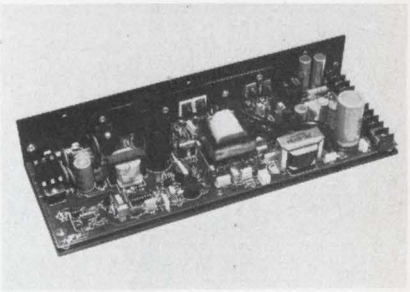
Interactive Device For Video Displays

The touch pen is a μP-based, stylus operated, transparent, graphical interface allowing simpler and faster interaction with the host processor by bypassing the keyboard. It can make a touch sensitive target out of every character the terminal can display. Features include: menu selection and medium resolution graphics standard (up to 256 points on each axis); high resolution graphics optional; can be used on flat or curved displays; can be used with rear projection; and, almost any size display may be used, from 5″ CRT to 3′ x 4′ projection displays. **Sun-Flex Co. Inc,** 20 Pimentel Court, Novato, CA 94947. **Write 242**

150W SWITCHERS

For Use With 8″ Winchester Drives

The NW150 switching power supplies feature 24V main output capability with



post regulated auxiliary outputs in an industry standard outline configuration. Features include built-in line filtering and soft start circuitry; 115/230 VAC input capability; fully regulated adjustable auxiliary outputs; LSI control circuitry; and built in remote sense on the 24V main output. The unit is designed to meet UL, CSA, and VDE requirements. Overall size is 13.6″ x 4.9″ x 2.5″. $292 (1-9); $216 (100-249). **National Power Technology,** 2111 Howell Ave, Anaheim, CA 92806. **Write 241**

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DEC

DEC 1200 BAUD PRINTERS

LA120-AA	EIA, KSR, Keyboard Only	$1,995
LA120-BA	EIA, Keyboard & Keypad, KSR	2,075
LA120-RA	Receive Only	1,795

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SCHERER'S MINI COMPUTER MART

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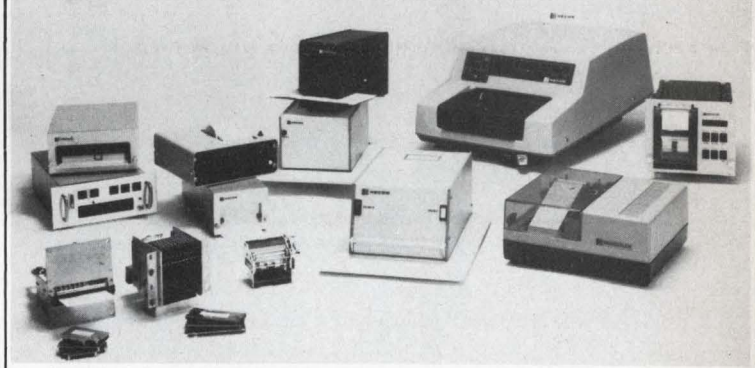
Write 54 on Reader Inquiry Card

The Little Printer That Didn't.



A technician anxiously approaches the test rack early on a Monday morning. Sipping his first cup of coffee, he looks expectantly at the tape for the results of the test run over the weekend. Blank. Eyes widening, he presses the "print" button. Silence. Frantically, he searches for a reason. Then he spots it. The printer . . . is not a Hecon.

Hecon has built quality printers that you can depend on for over a decade. We can supply Impact Dot Matrix, Thermal, Electrosensitive, and Modular Impact units. From one column to eighty columns. You can specify complete printers or OEM mechanisms. We also design and build custom units.

So the choice is yours—a printer that won't or a Hecon that will.

It's got to be good. It's a Hecon. 890 HECON®

Hecon Corporation, 31 Park Road, Tinton Falls, NJ 07724
• (201) 542-9200

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1982 NATIONAL COMPUTER CONFERENCE

JUNE 7-10 ★ ASTRODOMAIN ★ HOUSTON, TEXAS

"ADVANCING PROFESSIONALISM"

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★ The conference that has progressed in quality each year since its inception.

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Monday—Thursday, 9:00 am to 8:00 pm (EST)
Friday, 9 am until 6:00 pm.

In Rhode Island and outside the Continental U.S., call 401-884-9500.

64K DYNAMIC RAM

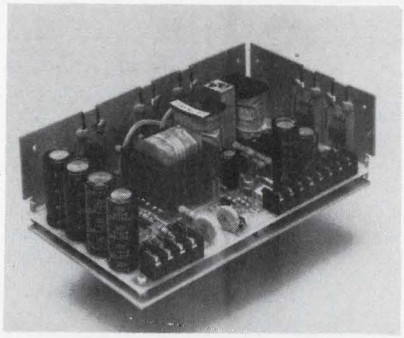
Second Generation DRAM

The MCM6664A and MCM6665A offer improved performance and high reliability at lower cost. This new generation device preserves the ASR (Address Strobe Ratios) of $t_{RAC}/t_{CAC}=2$, which provides a $t_{CAC}=t_{RCD}$ specification. Two systems performance advantages gained with an ASR = 2 include: the extended t_{RCD} provides additional switching time for the high capacitive load on the column address drivers; and, reduced t_{CAC} provides for faster page mode operation. This part also offers industry standard soft error performance of 0.1% per 1000 hours, improved row access time, lower input capacitance, wider operating margins, and exceptional tolerance to Vcc slew. From $19.40 to $63.60 (100+ qty). **Motorola,** MOS Integrated Circuits Div, 3501 Ed Bluestein Blvd, Austin, TX 78721. **Write 178**

SWITCHING POWER SUPPLIES

Single And Triple Output Models

Econoflex open-frame power supplies have dual inputs at 110VAC ±20% and 220VAC ±20%, 47-440 Hz; thus, they are suitable for use in equipment for world markets. Inrush current is limited to 15A peak at 110VAC and 30A peak at 220VAC line voltages. All outputs are fully regulated and floating, and incorporate short-circuit and overload protection.



The main output is adjustable over a ±10% voltage range. Remote sensing is standard, over-voltage protection is optional. Regulation for the worst case of full input voltage and 5-100% load change is typically 0.2%; ripple and noise are 0.5% RMS max. From $80 to $200 in qty. **Gould Inc,** Instruments Div, 35129 Curtis Blvd, Eastlake, OH 44094. **Write 220**

MAG TAPE CONTROLLER

Interfaces Up To Two Kennedy 6450 Drives to LSI-11

This μP-based, single board ¼" 3M Cartridge magnetic tape controller provides interface for one or two Kennedy 6450 ¼" DE300 type cartridge tape drives with up to 17MB (each) data storage, for backup use with LSI-11, 11/2 and 11/23 computers. Model DQ330 is compatible with DEC TM-11 and TS-03 software drivers in RT-11 and RSX-11 operating systems. In operation it handles read after write Serpentine head drives and includes a diagnostic routine and automatic self-test which causes on-board diagnostics to run each time the Q-bus is initialized. An integral LED provides indication to insure protection of critical data base transfer. The controller also includes operator convenience features, FIFO buffer for DMA latency, and memory addressing to 128K words. Performance includes 30 ips R/W speed, 6400 bpi format densities and 192,000 bps data transfer rate. $1436 (qty 50). **Dilog,** (Distributed Logic Corp), 12800 Garden Grove Blvd, Garden Grove, CA 92643. **Write 216**

DEC

DEC CRT'S

VT101-AA	EIA, Non Upgradeable	$ 995
VT131-AA	w/AVO, PCO, & Screen Editing	1,575
VT100-AA	EIA	1,375
VT132-AA	AVO, Screen Editing	1,450

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Itching . . . for a Thermal Printer?

Don't Scratch Your Head!

Don't scratch your printhead, that is. Only the Hecon A0550 Thermal Printers lift the printhead away from the paper during paper advance. This unique feature reduces unnecessary wear and extends printhead life to a minimum of 4 million lines at 2 lines per second.

Designed for long term reliability, the A0550 uses cast parts for consistent and dependable operation. Even the rubber roller uses an exclusive compound to ensure accurate paper position and superior print quality.

Available in 20 or 40 column versions, you can specify desktop complete units or OEM mechanisms. Two copy thermal paper is also available.

If thermal is the way you go, don't scratch your head—make Hecon your destination!

It's got to be good. It's a Hecon. 890 HECON

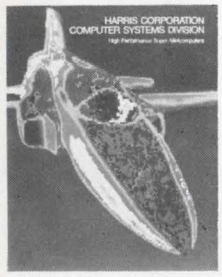
Hecon Corporation, 31 Park Road, Tinton Falls, NJ 07724
• (201) 542-9200

Write 51 on Reader Inquiry Card

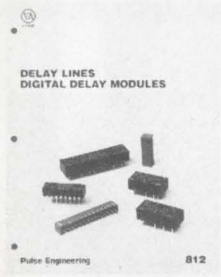
New Literature

Disk Storage Subsystem. This application note provides specific instructions for configuring an HP Series 80 personal computer with the MSC-9800H 5-1/4" hard disk subsystem in conjunction with other HP peripheral devices such as the HP-82901 5-1/4" floppy disk subsystem. It gives hints and examples on using the MSC subsystem for applications programs as well as procedures for backing up important programs and data from hard disk to mini-floppy disk. Application Note, 4 pp.
Microcomputer Systems **Write 250**

Lock-In Amplifiers. These fully programmable sine-wave responding instruments are of interest to anyone measuring intensities and phase shifts of weak signals — particularly those overwhelmed by noise. The brochure highlights Models 5205 (single phase) and 5206 (two phase) as the first commercial lock-ins to offer full computer control. "Your Computer... our Lock-In," brochure, 4 pp.
EG&G Princeton **Write 251**

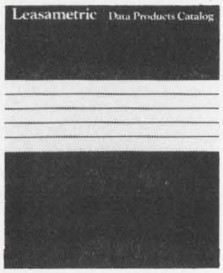


Super-Minicomputer Line. The brochure contains separate sections on each of the Harris virtual memory computer systems — from the H80 to the H800. An in-depth chart provides an overview of all Harris models and pertinent data about each, including throughput rates, performance measurements and maximum number of interactive terminal users supported. Brochure, 10 pp.
Harris Computer Systems **Write 252**



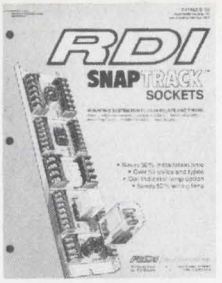
Delay Lines And Digital Delay Modules. Included are product descriptions, schematic diagrams, electrical specifications and a product selection guide. Also, high-performance and standard digital delay modules, dynamic RAM timing modules, 14 and 16 pin DIP delay lines and 7 and 14 single-in-line delay lines all for use in memory systems and other digital circuits. Catalog #812, 16 pp.
Pulse Engineering **Write 253**

Data Conversion Products. Describes 37 new products including technical data and specs for analog-to-digital, digital-to-analog, synchro-to-digital, and resolver-to-digital converters. Other products include data bus products, sample/hold and track/hold amplifiers, control transformers, industrial products and synchro instruments. Catalog, 8 pp.
ILC Data Device **Write 254**



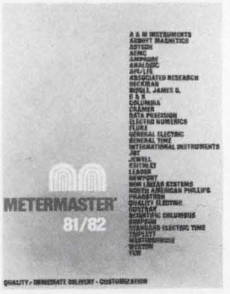
Data Products. Features data terminals, μP test and development systems and telecommunications equipment from major companies for rent or lease. Most items are available within 24 hours from 5 inventory centers located in the US and Canada. The 64 pp. catalog lists short technical descriptions and rental rates for each product.
Leasametric **Write 256**

Snaptrack Sockets. Describes over 60 relay socket assemblies and accessories. Instead of two fasteners per socket, the Snaptrack system requires only two fasteners per foot of track. Features a series of miniature socket assemblies, edge card connectors, 16 pin DIP socket assemblies, fuse blocks and new relay bails. Catalog 102, 12 pp.
RDI/Reed Devices **Write 255**



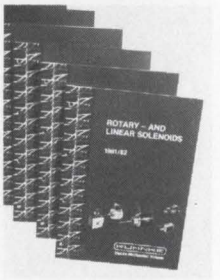
Series 90 PROM Programmer. Featuring the M910A Control Unit, the brochure describes the new RS-232C communications option which allows the M910A to be used with development systems and computers. It contains a list of 450 devices that can be programmed with the M910A, and describes the new gang personality modules that simultaneously program 8 PROM's for any family of 5V MOS devices. M910 brochure, 24 pp.
Pro-Log **Write 261**

Test And Measurement Equipment. Complete specs on thousands of instruments from 36 leading manufacturers. A single reference book for instrument, maintenance, test and field engineers and buyers. Includes multimeters, panel meters, oscilloscopes, frequency meters and counters, relays, printers, recorders, insulation testers, etc. Catalog, 432 pp.
Metermaster **Write 258**

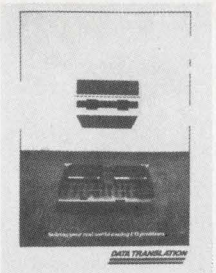


2800μC Family. Software enhancements such as the capability to boot from any drive, including the hard disk, and extensive error recovery are fully described. The systems are easily expanded for multiple users by adding MP/M or OASIS operating systems and additional serial I/O and memory. Brochure, 6 pp.
Systems Group **Write 259**

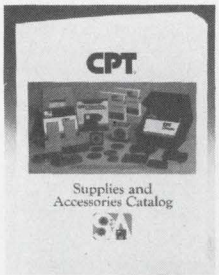
Rotary Solenoids. The technical catalog describes H. Kuhnke's complete line of rotary solenoids. Full technical information is provided on torque, voltage and options offered. A separate price sheet is enclosed. 50 pp.
H. Kuhnke **Write 260**



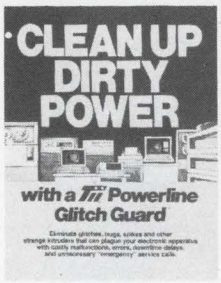
Packaging/Connection System. The system allows the use of high lead-count μP's and peripheral integrated circuits on an economical two-sided board. The 64-lead QUIP (quad in-line package) is described in this bulletin and illustrated with diagrams, spec charts and photos. A graph shows its low thermal resistance and a table lists other environmental test results.
3M **Write 267**



Analog I/O Systems. Full technical specs for data acquisition products ranging from modular subsystems to fully integrated μC based data acquisition systems are presented. Organized by product category, each section begins with a Quick Selection Guide followed by detailed technical specs on each product. Application sections are also included. Catalog, 288 pp.
Data Translation **Write 262**



WP Supplies And Accessories. Includes photos and descriptions of supplies such as printwheels, ribbons and diskettes for the CPT product line of WP systems and printers. Included are accessories such as anti-static floor mats, filing systems for storing and filing floppy disks, and a disk drive head-cleaning kit. Catalog, 12 pp.
CPT **Write 263**



Glitch Guard. Describes this series of powerline conditioning equipment that cleans up powerline surge, noise, lightning effects, spikes and other transients. Included in the line of devices and fault detection units are UPS, isolation devices, plug-in powerline outlet protection and items with line cords and Glitch Guards for direct installation into equipment. Brochure GG-11-81.
TII Electronics Div. **Write 264**

Display Products. The complete line of Cherry Gas Discharge Displays and Display Systems is included with application data and specs for the line of standard display panels, special custom format display panels, alphanumeric display systems and modular interactive alphanumeric display systems. Catalog CE-987, 16 pp.
Cherry Electrical Products **Write 265**

Switch Digest. Covers manual electromechanical switches and contains dimensional photographs, specifications, ordering procedures and catalog numbers for standard items including toggle, rocker, push-button, rotary and keylock switches. Catalog, 24 pp.
Crouse-Hinds **Write 257**

DC Power Boards. Presents integrated DC power boards for 48V and 24A systems of 200-400A capacities. They feature the Meter and Alarm Panel (MAP), a module which integrates all metering, alarm and control functions into a signal panel. Discussion includes a general description, design feature benefits and a concise listing of Warren's standard interchangeable elements. Publication No. 5PB-200/ 400-011.
Warren Communications **Write 266**

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DEC DEC 300 BAUD PRINTERS

LA34-AA	EIA w/Forms	$ 875
LA34-RA	EIA, Receive Only	850
LA38-GA	EIA, KP & Tractor	1,000
LA38-HA	EIA, KP, Tractor & Stand	1,100
LA38-AA	EIA, KP, Forms & Tractor	1,150

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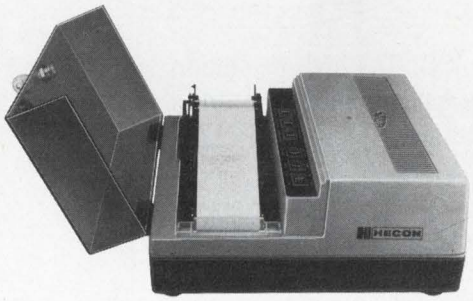

The sound of Hecon's GO687 Electrosensitive Tape Printer.

Reliable.
The only moving part is the paper feed. A unique, fixed 100 wire printhead produces a full 20 characters per line. No shuttle mechanism to fail. No ink cartridges or ribbons to replace. Lots of dependable printing.

Legible.
The 64 character ASCII set is produced in a unique 5 x 14 matrix pattern. Crisp, clear characters line after line at 5 lines per second.

Versatile.
Available versions are desktop, wallmount, and rackmount complete units or OEM mechanisms. A model for every application.

Reliability, legibility, versatility—all you ever needed in a Tape printer. Available now in the GO687.

It's got to be good. It's a Hecon. HECON®

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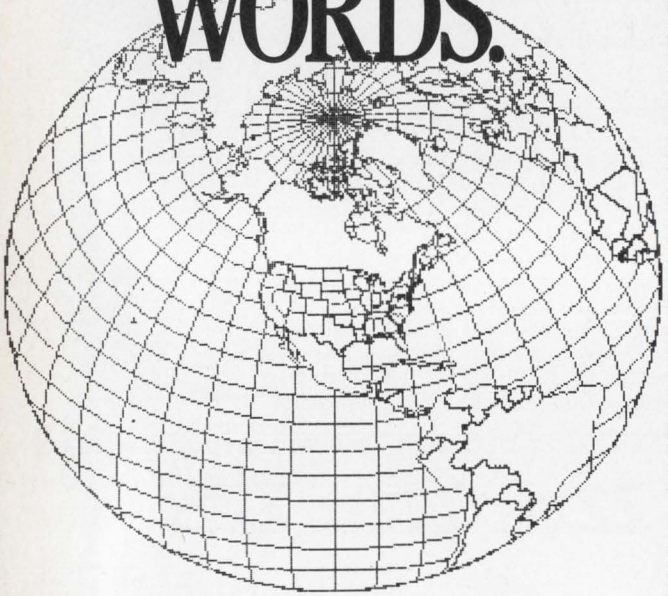
SOMETIMES, A PICTURE IS WORTH A THOUSAND WORDS.



Q160 from CDI. The high-resolution thermal graphics printer the world's been waiting for.

Standard Features:

160 cps. high speed, bidirectional printing
5 x 10 alpha-numeric dot matrix characters
Upper & lower case, true descenders
80/132 column printing
Software/switch-selectable functions

Optional Features:

High resolution (512/1024 per line), dot addressable graphics
Custom or dual fonts
APL font
Serial interface
Also available in receive only terminal

For more information on the Model Q160 graphics printer and the Model 2100 receive only terminal, call Richard H. Leeman, OEM Product Manager, at (800) 225-1229. (In Massachusetts call (617) 273-1550). Computer Devices, Inc., 25 North Avenue, Burlington, MA 01803.

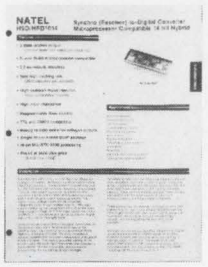
We travel in the best companies.

COMPUTER DEVICES INC.

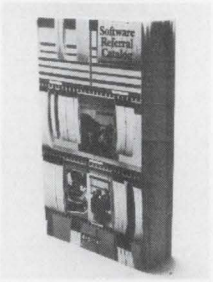
Write 37 on Reader Inquiry Card

New Literature

Compatible Products. The Ordering Guide/Price List, with information on over 100 DEC LSI-11 compatible products as well as Intel, DG, Unibus and Omnibus related products, contains product descriptions with current pricing information on completely packaged industrial process control systems, analog I/O boards that plug directly into the DEC LSI-11 and other bus backplanes, system enclosures, compatible floppy disk and Winchester hard disk mass storage systems and CRT terminals.
ADAC **Write 269**



14-Bit Hybrid S/D Converter. Describes the HSD1014 μP-compatible, 14-bit S/D converter which is packaged in a 36 pin DDIP hybrid. In addition to normal features, description, specs and ordering information, the data sheet provides applications, process and testing information. Data sheet, 12 pp.
Natel Engineering **Write 270**



Software Referral Catalog. This catalog for DECsystem -10 and -20 mainframe computer users is divided into two sections. The first lists commercially available software and is classified into applications from Accounting to Utilities; the second describes packages available from DECUS (Digital Equipment Computer Users Society). Each description includes abstract, sources and systems required. 368 pp.
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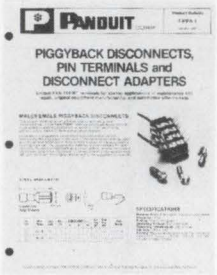

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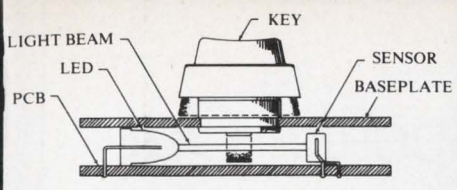

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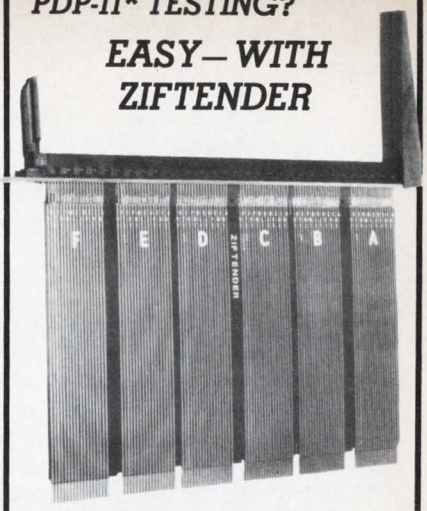

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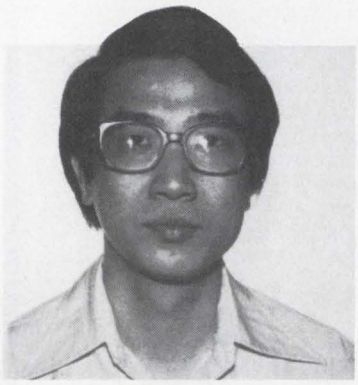
A Foreign-Born Engineer Speaks Out

by *Hing-Kai Chan*
Sandy, Utah



Some engineers doubt that an engineering shortage exists; others claim that US companies, taking advantage of foreign born engineers' (FBE's) need to be employed to gain residency in the US, offer them salaries substantially lower than the normal US market rate to obtain cheap talent without the dilemma of raising the salary scale to attract engineers. As an FBE myself, I wish to offer some viewpoints on the subject.

After reading many engineer-wanted ads, I believe the shortage exists but is not critical. I asked the Immigration and Naturalization Service in Washington, DC for the latest figures on approval for FBE residency. The most recent figure for 1978 shows that 6,700 engineers were admitted in 1978. Since the immigration regulation and quota is unchanged since the Johnson administration, this figure should increase only slightly for each of the last two years. However, with over 60,000 engineering graduates in the US by 1981, the additional FBEs admitted yearly is significant.

Unfortunately, I cannot link these two facts to the low salary scale. According to three independent salary surveys conducted by the Bureau of Labor Statistics, NSPE and IEEE, the median engineering salary for 1981 exceeded $35,000. Entry-level engineers start between $21,000 and $26,000.

FBEs without higher immigration preference (not related to US citizens or immigrants) must first apply for labor certificates to gain residency. US Department of Labor guidelines for hiring foreign workers state that it is illegal for US companies to: (1) hire FBEs if American engineers are available and (2) offer FBEs salaries significantly below the US market rate. Most companies comply with the law.

No statistics show how many FBEs are hired at lower salary scales, and most allegations are circumstantial. For example, another magazine's editor mentioned a recent ad placed by the Employment Division of the Oregon Dept. of Human resources that asked for an electronic/software engineer with a BS/MS in electronics or computer science and three to five years experience with real-time computerized process control, familiarity with Intel equipment and microprocessors, and be willing to work any schedule and travel out of state. The salary was $17,700. This editor called the salary "obscene" and said it was intended for FBEs. With the recent local government's tight budget, the salary seems reasonable. Perhaps the ad was placed without market research. If an FBE worked here over three years, he would establish residency; and, with those qualifications, would be earning twice as much!

A recent IEEE survey (*The Institute,* Oct. 1981) asked engineers if they knew alien engineers hired at salaries below what US engineers would receive for the same job. Of 212 replies, 46 said yes. So, although it's true that a few unethical incidents of hiring FBEs are true, we cannot justify that FBEs cause low salary scales.

Many engineers are dissatisfied with the present salary scale because they are not earning more. Since most are employees, they cannot adjust their own income as medical doctors and plumbers do. And, existing engineering societies like IEEE rarely represent engineers' best interests. So, without any bargaining power or representation, they must settle for their present salary scales. Many engineers also feel that job satisfaction is more important than salary reward. As long as they are willing to work unpaid overtime and be used as techs or aides, they deserve to be hurt. Maybe one day people will realize that engineers are well-trained professionals who deserve more recognition and reward.

Your comments are welcome: If you agree or disagree with this viewpoint (or anything in these pages), please write us a letter. On occasion, we would like to publish different viewpoints from our readers on this page. Whether you agree or disagree, we look forward to hearing from you. If you feel that there isn't enough time, we understand; could you then simply provide us some feedback? One way might be to take this (or future) Viewpoint pages and circle those statements that you agree with and underline those that you disagree with — perhaps adding some marginal notes — and then mail it or a photocopy to us. Best wishes and thank you. The Editor.

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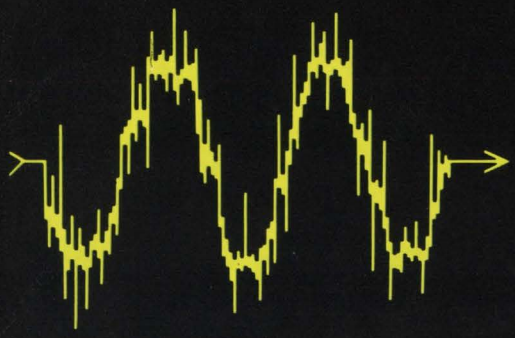

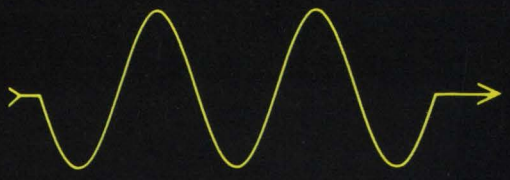

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