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DESIGNER'S GUIDE: MAKING THE TRANSITION TO SEMI-CUSTOM ICs

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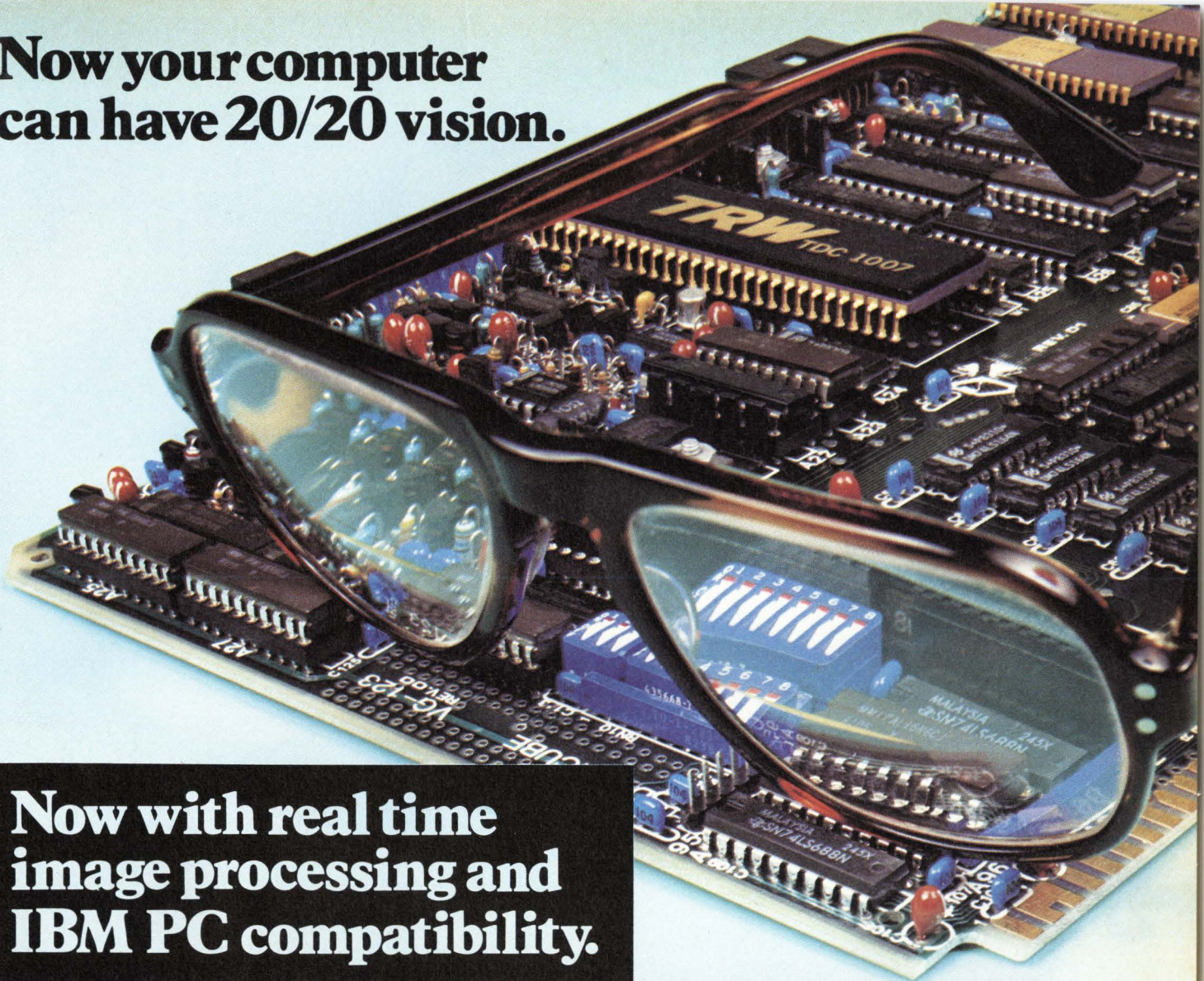
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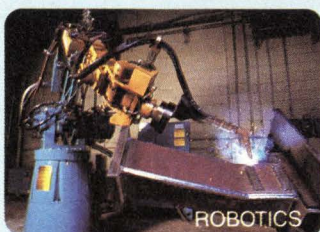
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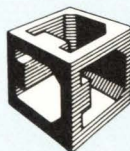
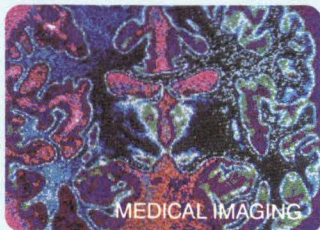
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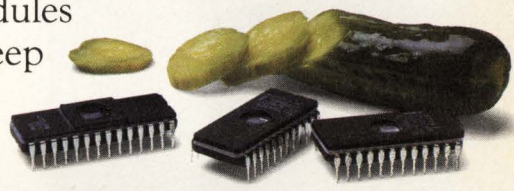
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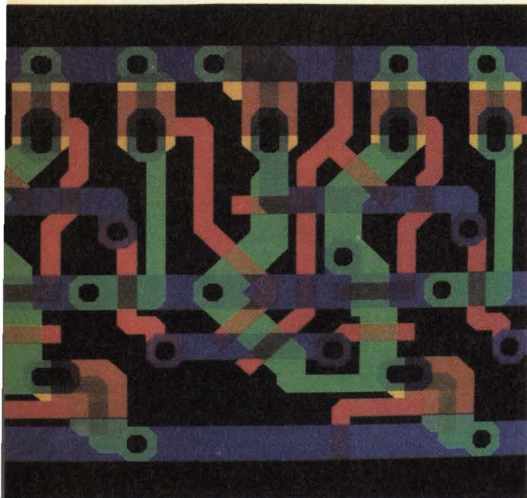
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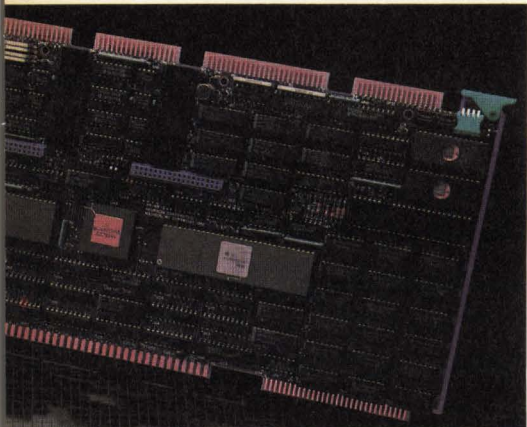
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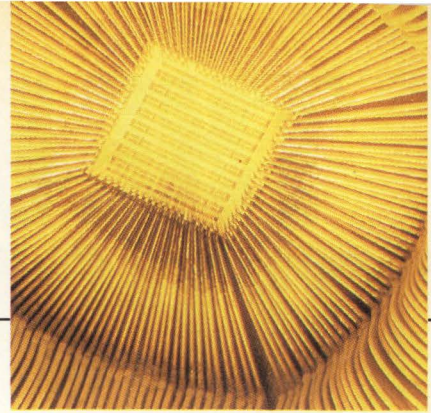
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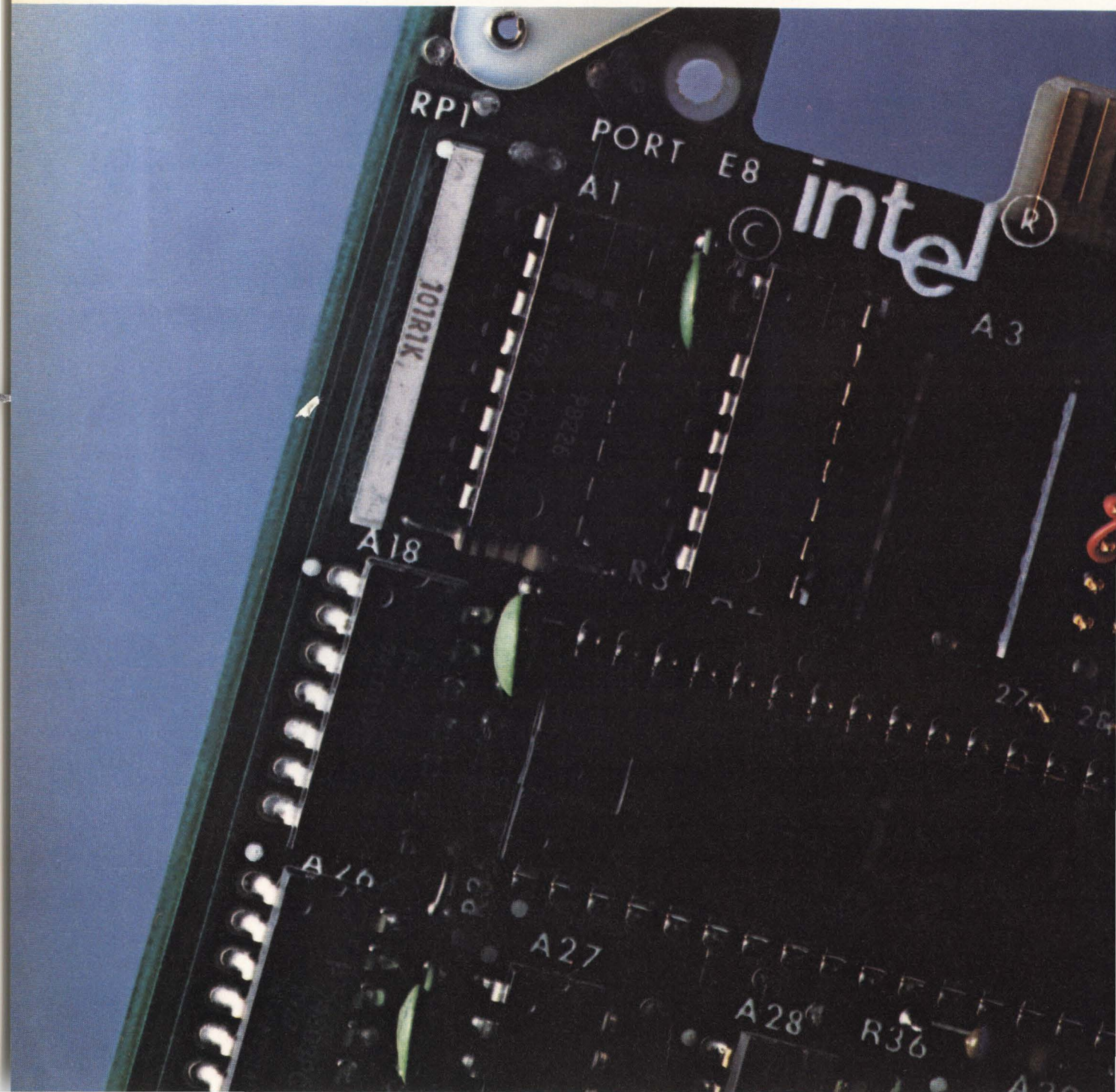
by James R. Coyle

One major market for displays is control industries whose product performs constant monitoring and management of a process.

ON THE COVER

Cover photo courtesy Gould AMI Semiconductors Inc. The three wafers in the background depict the improvement in fabrication process technology. Larger wafers offer increased yields, yet it is important to consider the transition from 3" to 5" wafers when assessing the yield. The chips in the foreground illustrate the wide variation of packaging for chips.

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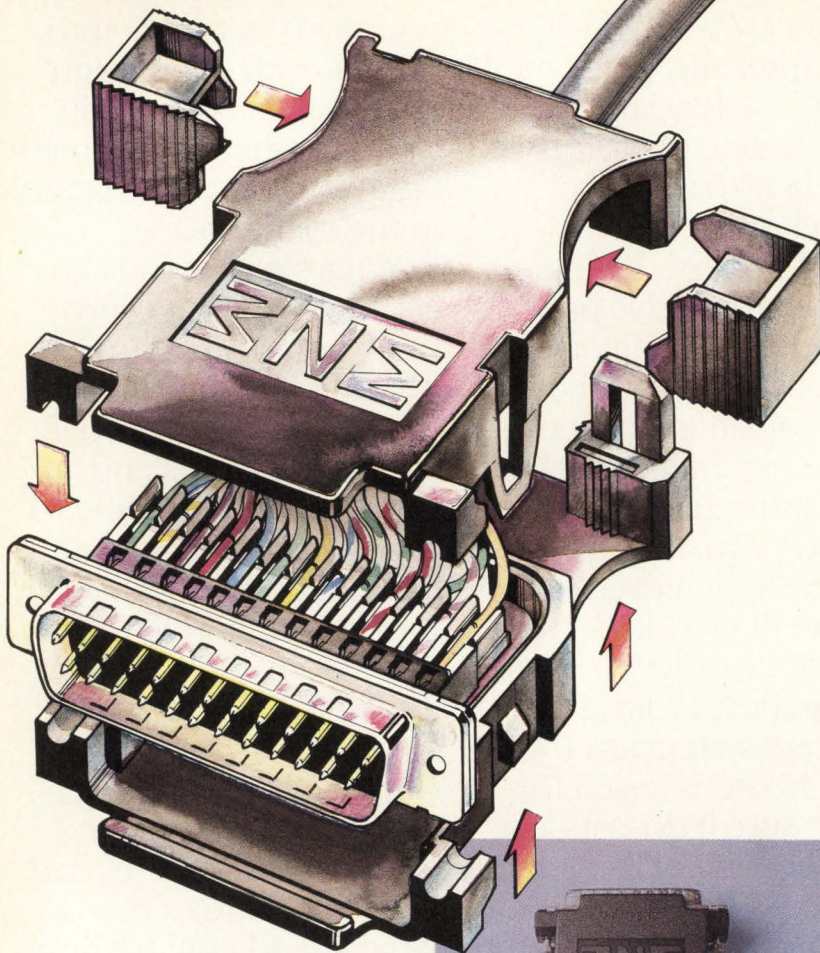
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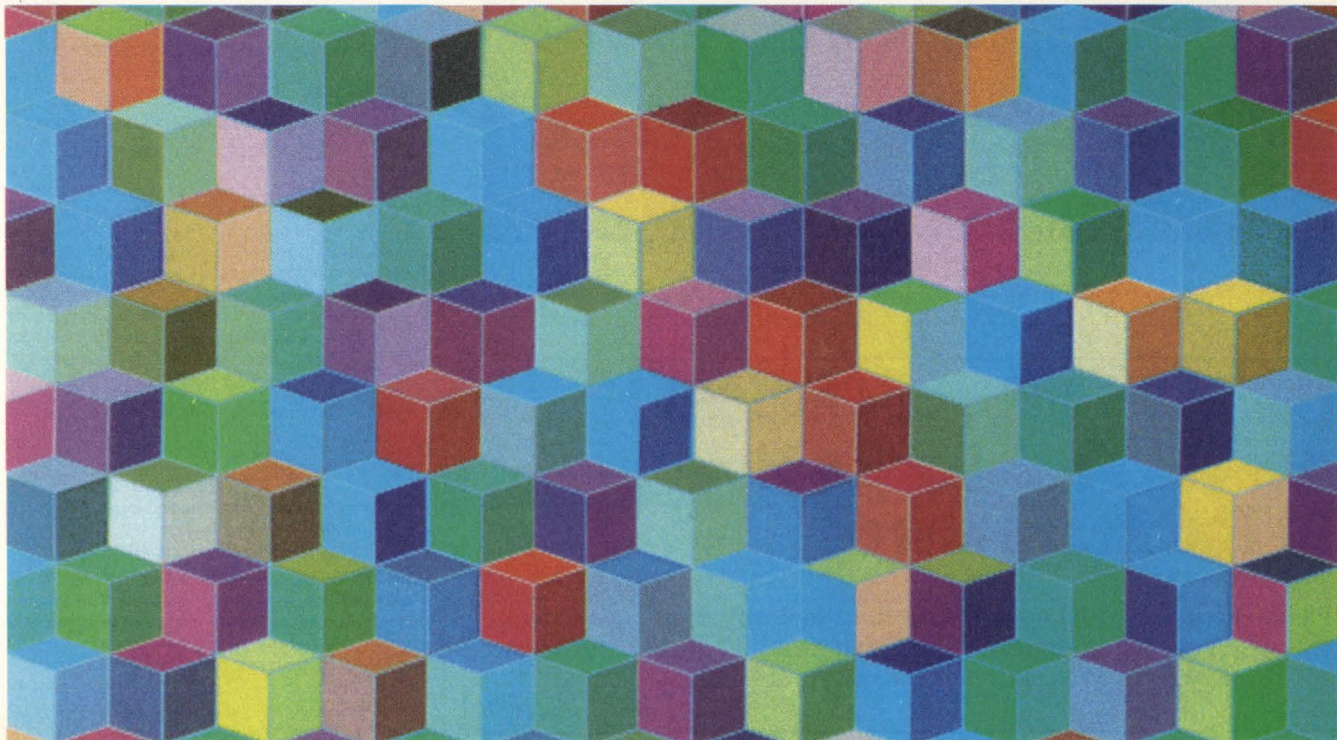
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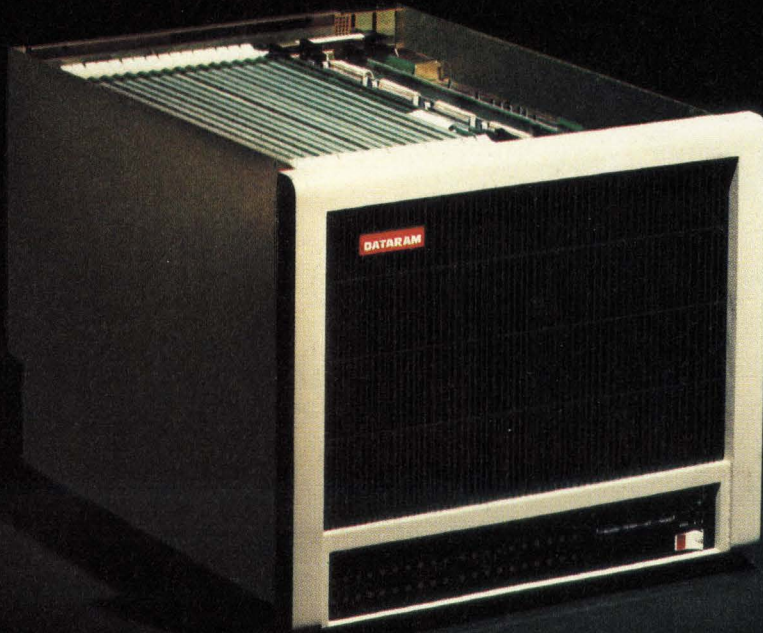
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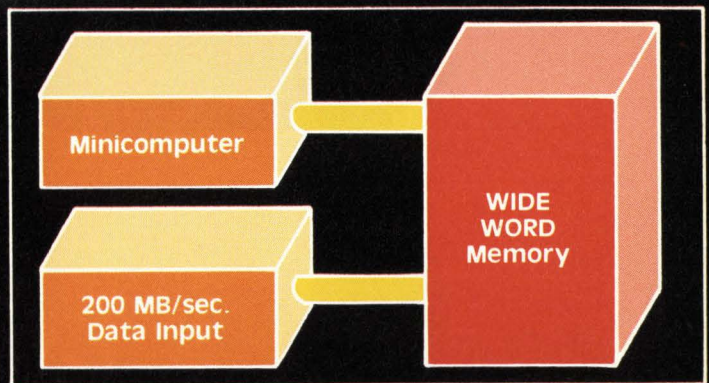
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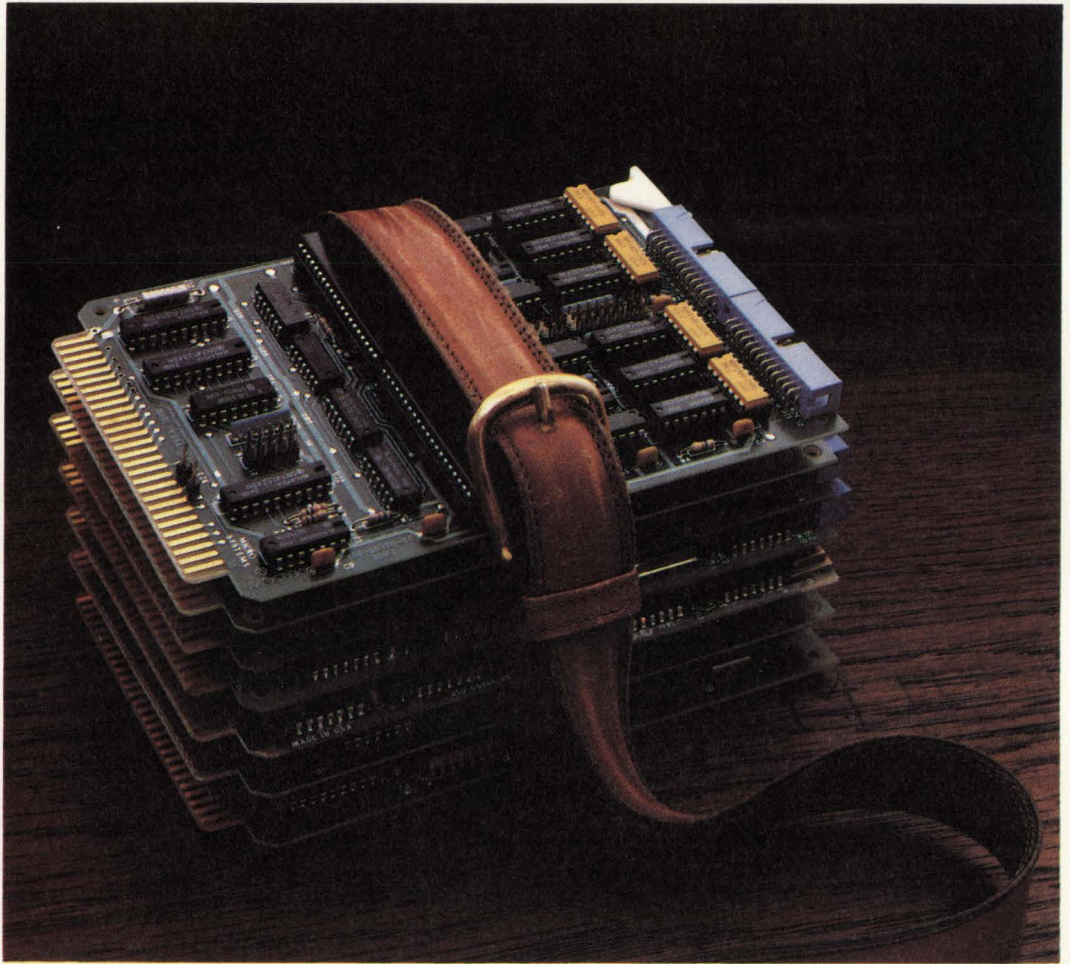
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‘A concern of mine is what impact the rising potential for ineffective protectionism may have on our industry.’

EDITOR'S COMMENT

This summer's trade conferences have shown the tremendous vitality of our industry and underscored the international nature of the current competition for technology. Exhibit floors display a greater share of technology from Japanese manufacturers vying with that of US manufacturers. We also see more concern expressed about the effects of Japanese technology on American industry and what responsive action should be taken. One cannot help but feel that the chorus of voices, either of indifference or of panic, should be more directed. There should, at the least, be critics or an audience that would react to the concerns being raised.

An obvious corollary to this observation is that the United States is the only Western nation without a cabinet level representative for the information industries of computer, electronics and telecommunications. It is also one of the few nations with no formal industrial policy regarding those same industries. There are, nevertheless, efforts by industry and the administration to shape legislation or regulation that will affect the information industries.

A concern of mine is what impact the rising potential for ineffective protectionism may have on our industry. The growing strength of demands for protection of the electronics industry against the "dumping" of products by Japanese manufacturers may be as futile as import duties and quotas on automobiles, steel, and textiles. An even worse possibility is that the end affect will be the same as in those older, smokestack industries, causing artificially high prices, inflation, and rewarding the inefficient.

The call for reciprocal agreements has become increasingly shrill. A recent article by Lionel H. Olmer, a Department of Commerce Undersecretary, in *Business Week* (May 14) is one of those rare efforts by an administration to enter the public record with a statement of policy. The article is circumspect, but at one point the author notes that imports will fall in 1984 as a result of enforcing US trade laws. The point in case is steel, an industry where the competition is all but over. The clear implication is that electronics can suffer as well.

Forced protectionism would be unfortunate because Japan is, among other things, our best trading partner, the most effective proponent of our way of life in the Pacific Rim area, and the honored competition that keeps US designers and engineers looking at the horizon for better solutions to technological problems. There is an unreasonable expectation that this will always be so. In the final analysis, a pragmatic Japan could sell its technology more easily to the resource-rich Soviet Union. Our experience with the Common Market countries and the oil pipe-

line cooperation with the Soviets shows how economics can overcome political orientation.

We often forget that despite the economic, industrial, and technological prowess of Japan, it has become a latter day equivalent of Great Britain at its colonial and trade peak. More importantly, the Japanese see this analogy, and due to the instability of the Pacific region, intend to insure that their influence does not suddenly erode. With its geographic isolation, Japan can ill afford to become a pawn in the volatile politics of the Far East. Its lack of mineral resources, fuel, food resources, its aging population, and minimal easily inhabited land require that it establish a trade-based economy.

The Japanese microelectronics industry, unlike the consumer electronics industry, shows little sign of abandoning its market share. One response to the challenge has been to analyze their reasons for success. Recognition of the multi-disciplinary scientific research that encourages microelectronics has produced efforts on the state and national level to encourage industry and academia to share resources and research. Industry has learned that it must form political committees that can shape legislation and regulation to its benefit. Further, if US industry is to remain at the forefront, the investment of capital must be higher than that associated with traditional industries. Similarly, the industry recognizes that its capital investment in plant and production facilities must be turned over much more quickly in order to remain competitive. The most encouraging responses have been industry efforts to form research cooperatives such as the Semiconductor Research Consortium and the Microelectronics and Computer Technology Consortium.

Another response has been for larger American firms to acquire semiconductor manufacturers. The rationale, at least in part, is that the economies of scale, vertical integration, and faster start-up time will enhance their capability. Examples include IBM's acquisition of 10% of Intel shares, Honeywell's acquisition of Synertek, GE's purchase of Intersil, Gould of AMI, Philips of Signetics and Schlumberger of Fairchild.

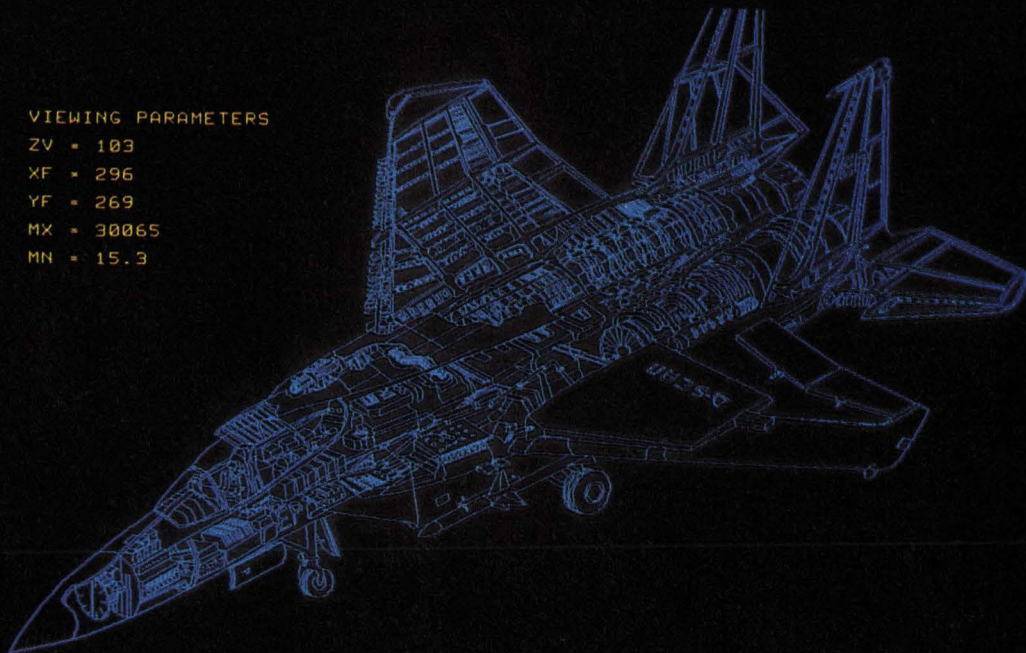
The results, with few exceptions, have not brought about the vertical integration typical of NEC, Fujitsu, or Mitsubishi. Again, there is a dissimilar Japanese result from a similar effort: Fujitsu's investment in Amdahl, NEC and Toshiba's construction of US semiconductor fabrication facilities, Hitachi's support of National Advanced Systems, Mitsubishi of Leading Edge and Sperry, Espon support of IBM and Sony of Hewlett-Packard and Tektronix.

In many cases, the more bellicose advocates of trade controls not only have the most to lose in terms of market share, but often lose sight of the potential benefits of joint cooperation or competition. These benefits relate to the integration of microelectronics into society, and the benefits that sharing of technologies can bring towards making life better for larger portions of the world's population.

Jerry Borrell, Editor-in-Chief

VIEWING PARAMETERS

ZV = 103
XF = 296
YF = 269
MX = 30065
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


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MCC Buys Symbolics' Systems

The Microelectronics and Computer Technology Corp. (MCC) recently bought 40 symbolic processing systems from Symbolics, Inc. In excess of \$3 million, the sale was the largest single order in Symbolics' three-year history. MCC is an Austin, Texas-based consortium of electronics and computer companies including RCA, Honeywell, and Control Data. MCC will be using the Symbolics systems for artificial intelligence research, VLSI/CAD, software technology (higher-level language research), human interface research, and database design.

2020 CAD/CAM Contract

Ramtek Corp. has signed a contract with Calma Company to provide colorgraphics computer terminals for use in Calma CAD/CAM systems. Ramtek expects its sales to Calma under the agreement to be at least \$20 million over a period of several years. Calma's new graphics terminals are based on Ramtek's 2020 series, an advanced technology product for interactive 2-D and 3-D design, including shaded solid models. The announcement follows a recent multi-million dollar OEM agreement between Ramtek and Control Data for CAD/CAM terminal products.

Codex Modems For RCA Network

Codex Corp. (Mansfield, MA) has signed one of its largest contracts to date, a 3-year agreement with RCA Cylix Communications Network, Inc., for up to 8,000 of Codex's new 2640 modems. RCA Cylix is a satellite-based, value-added data communications network for transaction-oriented applications, which became a wholly-owned subsidiary of RCA Communications, Inc. in 1982. The Codex 2600 Series modems are the first to utilize the Motorola 68000 microprocessor as a controller and a Codex-developed custom VLSI signal processing chip set. The Codex Model 2640 provides RCA Cylix with advanced network control capabilities, including transparent monitoring of line conditions and self-testing. RCA Cylix plans to use the 2640 in its public network, currently serving users across the continental United States.

Advances In High-Density Diskettes

BASF Systems Corporation is taking orders for the newest generation of floppy disks, the 5.25", high-density diskette. BASF first exhibited samples of this 5.25" diskette at the Fall Comdex, and is now making them available to drive manufacturers. A new coating technology allows BASF's 5.25" high-density floppy to store up to 1.6 Mbytes, or 60% more than the conventional 5.25" 96 TPI floppy. BASF is one of the qualified vendors for YE-Data's YD-380T disk drive. BASF is currently developing a 3.3-Mbyte 5.25" high-density diskette, and will make that product available when the new generation drives enter the market.



Optoelectronic Division Begins Production

National Semiconductor's Optoelectronics Division has begun production at its new plant in Rensselaer Technology Park (Albany, NY). National consolidated all of its optoelectronics operations into this one plant after acquiring Xciton Corporation in June of 1982. This new facility will enable National to put in place an advanced statistical quality control program designed to further enhance the quality of its components. National will be expanding the product line in intelligent displays and higher performance infrared devices and fiber optics.

Floating Point Ups Lattice Investment

Floating Point Systems Inc. has recently increased its investment in Lattice Semiconductor Corp. by \$2.5 million. As part of the agreement, Floating Point Systems (FPS) may purchase up to one-tenth of Lattice's wafer-fabrication capacity for its high-speed computer products, which require the kind of high-performance CMOS (complementary-MOS) chips that Lattice plans to manufacture. FPS will also be given access to Lattice's proprietary VLSI (very large-scale integrated) circuit design techniques, and assist Lattice in the definition and design of standard products, including digital signal processing circuits.



Orcatech, Draper Labs Development

Orcatech Inc. and The Charles Stark Draper Laboratory (CSDL) has signed a development agreement for delivery of standalone computer-aided design software on Orcatech graphic workstations, addressing the application area of mechanical design. CSDL has for the past decade been developing sophisticated CAD tools in support of their design and engineering activities on a wide variety of military and commercial projects. The CAD package developed by Draper Laboratory, referred to as ICAD—Integrated Computer-Aided Design—has been in use for 10 years. Under the Orcatech/CSDL agreement, Orcatech has worldwide marketing rights and projects its initial product offering to be available in the 3rd quarter of 1984.

Tape Drives Take ECC Approach

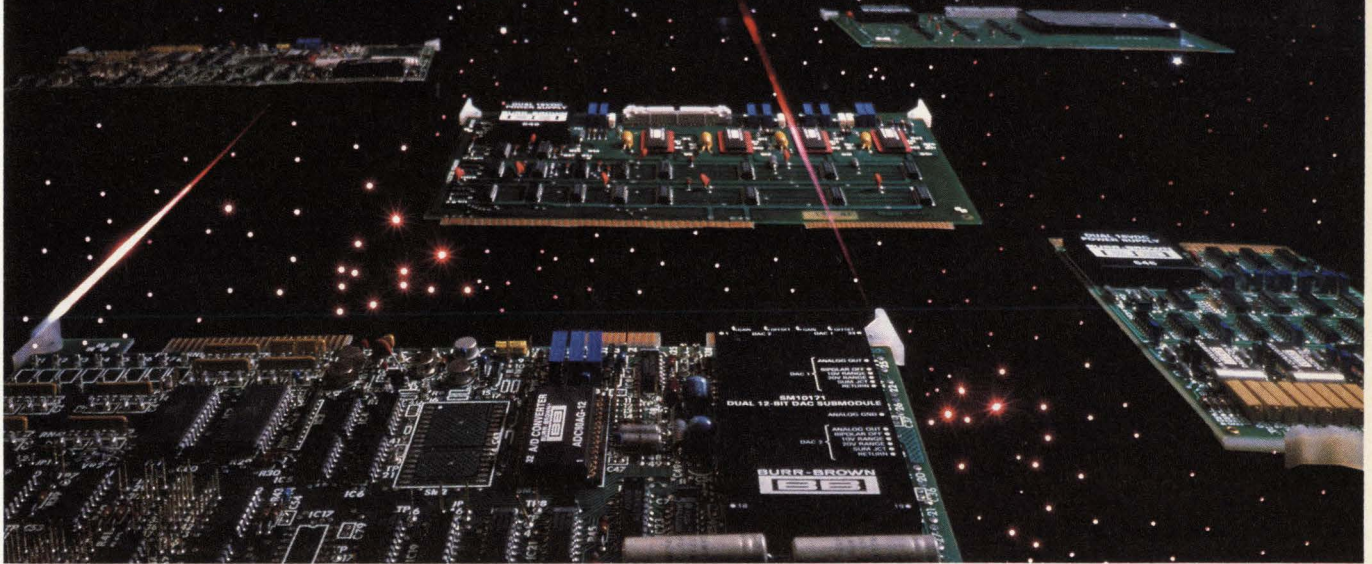
A 120 Mbyte class of quarter-inch cartridge tape drives utilizing error correction code (ECC) for enhanced data reliability will be defined and proposed as a worldwide standard by the Working Group for Quarter-Inch Cartridge Drive Compatibility (QIC). The QIC-50 format will provide read compatibility with current 4-track and 9-track cartridges which utilize the QIC-24 recording format. It is expected that the present QIC-02 formatted and QIC-36 basic interfaces will be adapted to accommodate QIC-50 devices.



Artificial Intelligence For Lotus

Lotus Development Corporation, producer and marketer of the 1-2-3™ and Symphony™ programs for desktop and portable computers, signed a licensing agreement with Prelude Development Corporation, a startup artificial intelligence software firm. Under the agreement, Prelude, which was founded by a former Lotus employee, will license artificial intelligence (AI) software technology to Lotus. Lotus plans to market products incorporating the technology in 18 to 24 months. The company will develop a family of productivity products based on intelligent databases to be introduced in Spring 1985.

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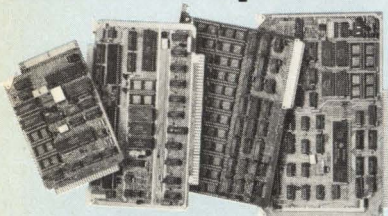
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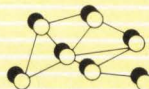
Representatives' inquiries are welcomed.

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UPDATE

LAN Marketing Agreement



Interlan, Inc., a supplier of Ethernet local area network system products, and Data General Corporation have entered into a marketing agreement which will provide users of ECLIPSE MV/Family™ systems operating under AOS/VS the ability to connect Data General's XODIAC™ network to an Ethernet/IEEE 802.3 local area network. Under the terms of the agreement Interlan will provide Ethernet Communication Controllers for connecting Data General ECLIPSE MV/Family systems to Ethernet and Data General Corporation will provide the driver software for use with AOS/VS software and AOS/VS XODIAC software.

Eaton Acquires Bunker Ramo

Eaton Corporation (Cleveland, OH) has acquired the Bunker Ramo Electronic Systems Division (Westlake, CA) from Allied Corporation, including all of the Division's businesses with the exception of the antisubmarine warfare product line. The Division will become part of Eaton's Defense and Electronics Group and will continue to operate under its current management. The Bunker Ramo Electronics Systems Division will add capability to Eaton's role as a supplier of C³I (Command, Control, Communications, and Intelligence Systems) to the Government. The purchase price was not disclosed.

Federal Emergency Management Systems

Burroughs Corporation's subsidiary, System Development Corporation, has been chosen by Harris Corporation of Melbourne, Florida, to furnish mobile message switch and message management subsystem for its Direction, Control and Warning Communications Systems (DCWCS) contract from the Federal Emergency Management Agency (FEMA). The initial \$9 million subcontract to the Custom Products Group of System Development Corporation (SDC), a Burroughs Company, calls for construction and delivery of four sheltered mobile DCWS units. Each unit contains Burroughs TEMPEST-qualified and Electro-Magnetic Pulse (EMP)-hardened medium computer systems and

microcomputer workstations. "TEMPEST" is a security design designation that allows electronic equipment to be protected from compromising emanations. "EMP-hardened" protects both hardware and software from the transient shock of a nuclear blast. Over the next five years, the contract is expected to exceed \$30 million.

Trident II Displays

Sanders Associates, Inc. has been awarded a \$10 million subcontract by Sperry Systems Management, to provide Auxiliary Display Terminal (ADT) equipment for the U.S. Navy's Trident II navigation subsystem development program. The ADT's will provide the keyboard entry and display capability for monitoring the Trident II's navigation subsystem performance and will also be used during maintenance and training operations. The ADT is an adaptation of Sanders recently developed MILIGRAPHIC Display System, a militarized intelligent raster graphic display terminal with dual microprocessors, derived from Sanders/CalComp VISTAGRAPHIC™ displays.

Daisy To Offer Zymos Libraries



ZyMOS Corp. will adapt its ZyP standard-cell libraries for use with Daisy workstations, while Daisy will provide ZyMOS with training, application assistance and hardware and software to develop the Daisy-compatible ZyP libraries. This agreement marks the first time that ZyP libraries will be available for a workstation. The libraries, available for both 5- and 3-micron CMOS technologies, are predefined standard logic functions that are used to design ICs. Each library includes more than 100 of the most often used digital functions.

Plessey Reorganizes

In a move to be more responsive to its business opportunities, Plessey Peripheral Systems, Inc. has restructured its divisional management organization and is combining its Computer Systems, Computer Products and Distributor Products Divisions. Under the new management structure, activities previously directed by separate division personnel will be consolidated into corporate-wide functional groups, including manufacturing, sales and marketing, finance, administration, engineering and service departments.

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WASHINGTON REPORT

by Anne A. Armstrong

IBM Asks For Stop On Counterfeit Imports

As part of an increasingly vigorous program to protect its products against unauthorized use, IBM Corp. has asked the Customs Service for help in stopping the importation of counterfeit copies of more than 70 IBM products. To support the request for special protection, IBM has registered copyrights of operating systems, applications programs and printed materials with the Washington enforcement branch of the Customs Service.

Apple Computer enlisted Customs aid last year to try and stop the flood of counterfeit Apples from the Far East. Agents did win indictments recently in Philadelphia against a group importing fake Apples from Taiwan. However, several Taiwanese companies have begun importing computers without ROM to get around the court ruling that it is the ROM which is protected. Customs agents, backed by an International Trade Commission ruling, have been seizing the ROM-less Apples as they enter the country, but the legal issues are muddy and may have to be resolved in court.

IBM will not say how serious its problem with counterfeits is.

Deficit Emerges In Japanese Computer Trade

Commerce Department figures indicate that imports of data processing equipment from Japan jumped sharply from \$274 million in 1982 to \$819 million in 1983. Imports of subassemblies and parts were up 65.5% from \$433 million in 1982 to \$708 million in 1983. Meanwhile, exports of the same type of equipment to Japan increased only slightly, leaving the United States with a trade deficit of nearly \$700 million.

The figures show an increasing dependence by U.S. OEM manufacturers on Japanese, lower-priced, volume parts, according to Computer and Business Equipment Manufacturers Association President, Vico E. Henriques. They also show it is easier to get into the U.S. market than into the Japanese counterpart, said Henriques. Despite continued effort by U.S. firms, Japan remains the only world market where U.S. computer equipment has a nega-

tive trade balance.

The trade situation with Japan has been the subject of several high level talks with Japanese officials, however, industry officials see little prospect for change in the near future.

Pentagon Wins Right To Review Exports

President Reagan has decided to give the Defense Department the right to review export license requests for computer equipment destined for more than a dozen non-Communist countries. The Pentagon already has the review right for computers bound for Communist countries, but several shipments to non-Communist countries have been diverted to Eastern Bloc locations. The new authority amounts to veto power over the shipment of a wide range of materials including semiconductor manufacturing equipment, laser technology, and many types of computers.

Although the decision is seen as a victory for DOD and a sign of tighter export controls, the President included two checks in the system: the formal licensing procedure remains at the Commerce Department and a time limit has been put on DOD's review process so licenses cannot be held up indefinitely.

DOD To Curb Software Exports

At a recent meeting of the CoCom countries, which include NATO allies and Japan, the United States urged that software be included on the list of equipment and materials that cannot be shipped to the Soviet Union and would require special licenses before exporting to Western countries.

Administration officials are concerned that certain software that was written for commercial uses can also be used for military purposes. Real-time software systems are high on the list to be included. Certain computer-aided design and manufacturing systems and a host of computer languages, including ADA, C, Pascal, and UNIX, are also reportedly on the list to require special licensing procedures.

Pushing the new restrictions is Assistant Secretary of Defense for International Security Policy, Richard N. Perle,

who recently demonstrated for a Senate hearing that an Apple computer could be programmed to help select battlefield targets.

The last time restrictions on software were proposed, CoCom voted them down, but the current administration strongly believes that something must be done to stop the transfer of technology to Soviet bloc countries. Pressure to include software will be higher this time.

State Software Protection Bills Pending

As numerous computer crime, chip and software protection bills languish in an election-year Congress, several parties are turning attention to the state legislatures in an effort to get some legislation passed.

The Videotex Industry Association is taking its case for stopping unauthorized access to its computer systems to the states first, before even approaching Congress. VIA officials see little chance of any federal legislation in the near future and believe that some state action is possible.

Vault Corporation of Westlake, CA, is leading an effort to get software anti-piracy legislation introduced in all 50 states. So far, legislation has been introduced in Louisiana and a sponsor has announced a bill will be filed in California shortly. Sponsors say that illegal software copying costs publishers as much as \$700 million each year.

The Louisiana and California bills, which are similar, attempt to make the copying a contract issue, enforcement of which falls into a well-defined area of the law.

C-3 Wins Navy Contract

Less than a month after debarment proceedings brought against it by the Army were dropped, C-3 Inc., of Reston, VA has won two Navy contracts totalling some \$89 million dollars. The first contract, worth more than \$69 million, calls for C-3 to provide 200 small computers and maintenance. The second, valued at \$20 million, is a maintenance contract for the Navy's series of Perkin-Elmer 3200 computers. C-3 currently has the maintenance contract for those computers.

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However.

As soon as you try to transfer the data generated by your engineers to the design stage (not to mention manufacturing) you'll find you have a problem. Because none of the systems are fully compatible with each other. Engineering can't get along with Design. Design can't get along with Manufacturing. And vice versa. Worse still, when the systems can't get along, neither can the people using them. So instead of state-of-the-art, you end up with something akin to a state of war.

The solution, of course, is to work with one company that can handle the entire project from beginning to end. A company with a full range of modular systems for every stage of every electronic design project. All fully integrated around a common data base.

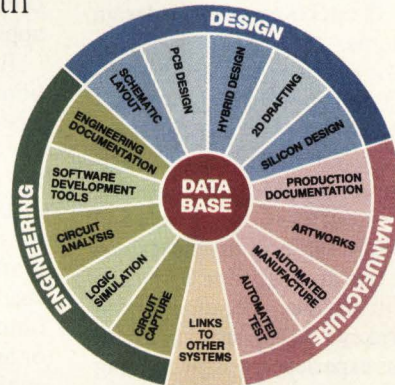
That company is Racal-Redac.

With Racal-Redac, you can solve today's problems without creating new problems for yourself tomorrow. Because all the system modules were designed to work together, and grow with you as your needs grow.

Read that last paragraph again. We at Racal-Redac are talking about a range of complete, totally integrated systems which work for you through every stage of the design cycle.

Only unlike other companies, what we're talking about isn't a vague promise for the future. Racal-Redac systems are already hard at work right now in over 1,000 electronics companies around the world. Any one of which we will be happy to discuss in considerable detail.

Just clip your business card to this ad. Or write. Or call. But don't wait for someone else to work it out. Because the alternative to integration is disintegration.



Finally, a totally integrated capability for electronics.

RACAL-REDAC
 Linking Concept to Product

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Functions Linked By Integrated CAD Services

One of the hottest areas of technology development is that of industrial implementation of computer technology. Among these implementations are applications of computer aided design, computer aided manufacturing, and computer aided engineering. Mechanical CAD systems are being developed at a rate similar to that in the electronic area; the field being dominated by Computervision, Applicon, Intergraph, and IBM because they offer systems in both mechanical and electronic applications. There is also a wide knowledge of the firms that build the workstations or computer graphic display systems that are the heart of the CAD system because of our coverage of the design of such systems.

There is, however, a much less significant understanding of several manufacturers who have a long history of working with design, manufacturing, and engineering disciplines. Most notable are manufacturers such as Control Data and McAuto. While the origins and experience of the two are disparate both have similarities in that they offer timesharing services, turnkey CAD systems, and have a tremendous experience with integrating CAD in industrial processes.

McAuto is the computer services division of the McDonnell Douglas Corporation. The company has, and continues to benefit from, the exposure of the parent firm to solving sophisticated engineering

One of McAuto's strengths in mechanical CAD is its development of a B-rep type solid modeler. The system is capable of both wire frame and rendered surfaces.

Unigraphics II from McAuto operates on a variety of terminal configurations supported by Genisco, Tektronix, and Megatek.



problems with computers in the design and construction of aircraft. McAuto sales appear less substantial in CAD than the firms mentioned above, but much like the case with Control Data, this belies the work that both McAuto and its parent company achieves in broader fields or the experience that the company brings to the application of CAD to industry.

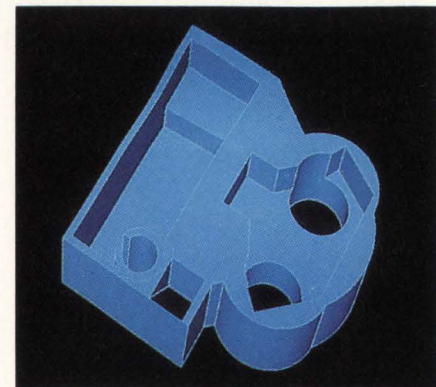
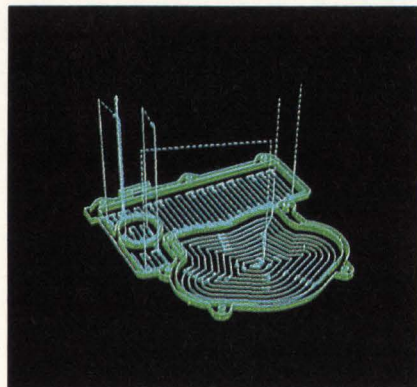
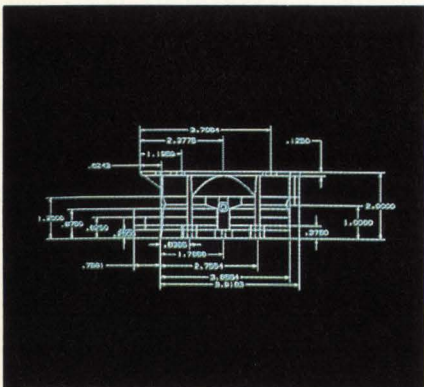
To a certain extent the power and functionality of CAD systems is measured against the graphics capabilities of a workstation. This is one of the causes of the recent controversy regarding CAD systems that offer solid modeling capabilities. The crux of this issue is that many graphics functions such as 3D capacity, shaded images, and dynamics may have limited application to many of the design or analytic tasks associated with design engineering today. More basic issues include techniques for storage and management of data bases, the interaction of CAD/CAM/CAE functions, and the interface of computer systems to integrated manufacturing processes.

The efforts by manufacturers such as Computervision in their announcements last fall about joint work with IBM is to develop strength in areas such as those above. McAuto's announcements seek to show that they, among others, already

have the type of integrated manufacturing and industrial experience discussed here. The company has recently released Unigraphics II which represents a substantial step towards integrating many design and engineering functions. While many manufacturers are at least partially successful in linking drafting, engineering, and manufacturing, other functions which make up the concept of computer integrated manufacturing are not as well developed. McAuto rightly points out that database management, communications, programming support, and management/business activities must all be supported. However, there are very few manufacturers who can afford to implement this comprehensive a solution, particularly as its introduction is tied to existing capital investments such as plants. Even the conceptual description of such comprehensive solutions as presented by Hewlett-Packard, Control Data, or IBM presents the planner with an almost overwhelming number of ideas to assimilate.

However, those firms who are able to offer their experience with integrating CAD in industrial processes may have a significant lead.

— Borrell
Write 241



**SUDDENLY
THE TAPE
CONTROLLER
IS
OBSOLETE.**

SPECTRA LOGIC

Metheus Expands Product Line

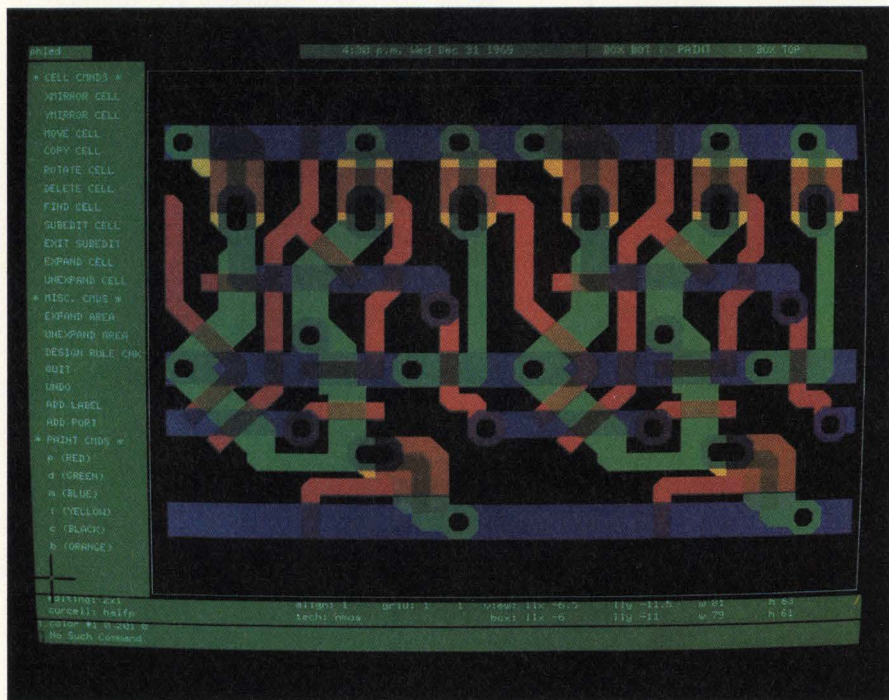
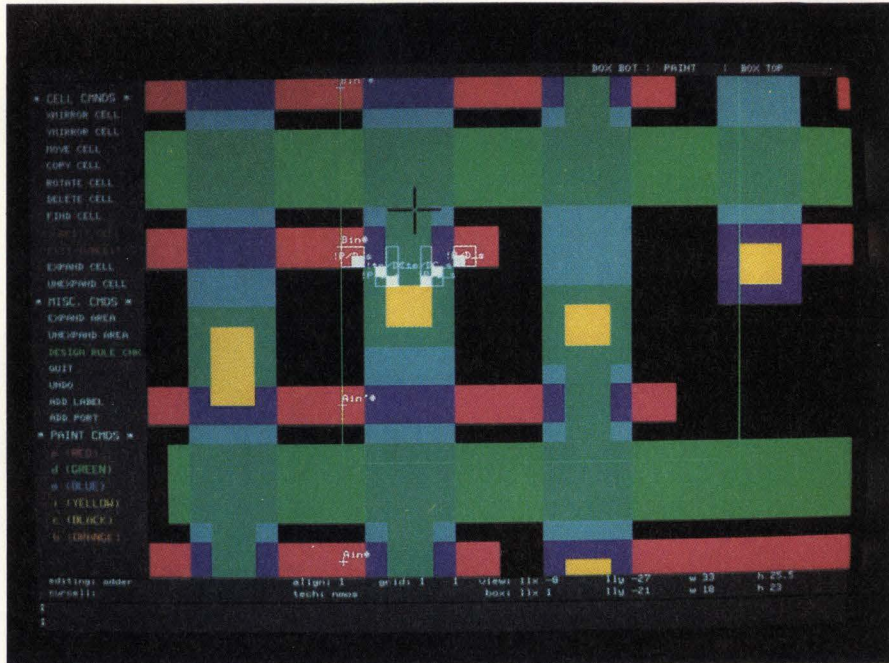
Metheus, the Hillsboro, Oregon-based developer of graphics display processors, recently announced several products for its graphics workstation. The announcements indicate that the firm not only intends to compete for OEM markets in computer graphics but will be competitive with firms such as Daisy and Mentor for electronic CAD systems. The company has incorporated seven software systems into its product line: UNIX software development, graphics development, schematic design, logic design, printed circuit boards, full custom IC design, and gate array design. A basic configuration of the system with UNIX, graphics, and schematic design capabilities will cost under \$40,000. In a configuration called the "Logic Design System" the product supports the schematic design, HILO fault and functional simulations, SPICE circuit simulation, and standard cell libraries for products from AMI, IMP, and SMC.

The company is somewhat unique in that it is one of the few workstation vendors that develop not only graphics processors and workstations, but are also willing to offer turnkey CAD systems in the electronic CAD field. The Apollo processors have been selected by the majority of electronic design station makers to date. Since its founding in 1981 by a group of talented engineers from Tektronix, Metheus has consistently surprised many observers with its growth. It has recently begun construction of a large new facility to support the manufacture of products for its OEM such as Hewlett-Packard, PERQ, Sigma Design, and CII Bull.

While the company is privately owned, a third round of venture financing has provided a total of almost \$15 million in the last three years. While the company notes that its workstations have potential application in many fields, their drive for products in electronic CAD have shown what many analysts of the CAD field are beginning to feel; that mechanical CAD is being supplanted in terms of systems sold by electronic CAD applications. It cites a Dataquest Report, for example, that shows significantly less growth in traditional CAD markets. Many will question whether its citation of a Strategic Inc. report that shows full custom will experience faster growth than standard cells or gate arrays is accurate.

— Borrell
Write 242

Top: The Metheus Full Custom Design System. Center: The lay-out editor allows on-line design rules. Bottom: 45°-angle geometry lay-out capability.



HOW TO DOUBLE YOUR CONTROL WITHOUT DOUBLING YOUR CONTROLLER.

If your plans for controlling disk and tape drives call for two boards and two CPU slots, you can now cut your plans in half.

And use the SPECTRA 25 LSI-11 emulating multifunction controller instead. You'll get all the control of separate disk and tape boards in just half the space. Half the slots. Half the spares. While using less power.

SPECTRA 25 is the smarter way to handle SMD/Winchester and 1/2-inch tape drives, and it's the first and only multifunction controller designed for DEC Q-BUS® computers.

Its block-mode data transfer capability can increase your throughput by up to 50%. And it performs Error Correction Code (ECC) independently of the operating system. All 32 bits worth.

SPECTRA 25 fully emulates DEC's RM02/5 and RM80 disk subsystems, and TS11 tape subsystem. It can run two SMD disk drives and four tape drives, in any combination. Plus an E²PROM lets you easily reconfigure while the controller is in your system.

But SPECTRA 25 puts something else in your system, too: proven reliability. Because you're working with half as many parts and pre-tested ICs.

You're also working with excellent documentation that's regularly updated. And the most comprehensive one year warranty in the industry. All backed by responsive nationwide service.



SPECTRA 25 is the multifunction controller that doubles your control. And your advantage on the competition.

Before you look at Emulex or Dilog, consider the SPECTRA 25 from Spectra Logic.

It could be all the controller you'll ever need. For further information on our expanding family of controllers for DEC Q-BUS and UNIBUS® computers, call or write us today.

	SPECTRA 15*/ SPECTRA 25	SPECTRA 111*/ SPECTRA 121	SPECTRA 12*/ SPECTRA 21
BUS	Q-BUS (Block-mode)	UNIBUS	UNIBUS
Disk Emulation	RM02/05, RM80, RP06 (2 drives)	RM02/05, RM80, RP06 (4 drives)	RK06/07 (4 drives)
Tape Emulation	TS11 (4 drives)	TS11 (4 drives)	TS11, TM11 (4, 8 drives)
Disk Transfer Rate (SMD)	2.0MB/sec	2.0MB/sec	2.0MB/sec
Configurable On-Line	Yes	Yes	No
*Single function disk controller			

Spectra Logic Corporation, 1227 Innsbruck Drive, Sunnyvale, CA 94089, (408) 744-0930, TWX 910-339-9566, TELEX 172524 SPL SUVL. International Sales Office: Belgium (32) (2) 5134892.

SPECTRA LOGIC

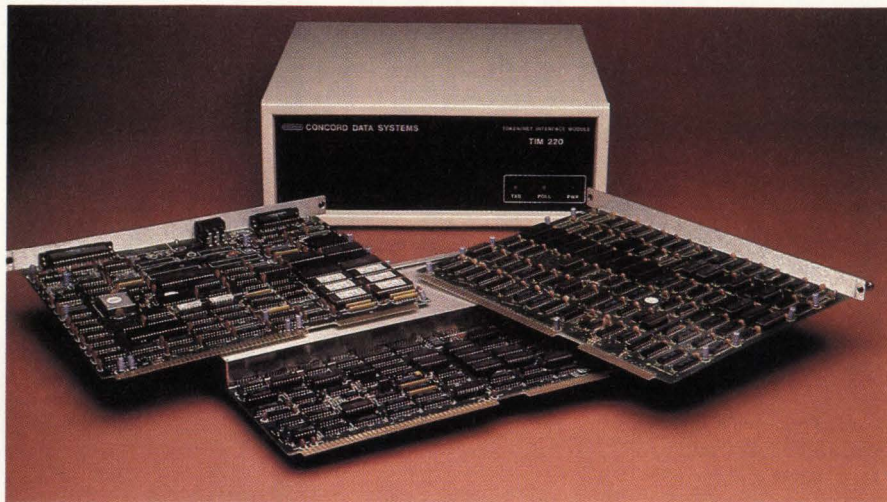
The Multifunction Controller Company.

NBS Networks NCC Exhibitors

The National Bureau of Standards, General Motors and Boeing booths at the National Computer Conference (NCC) will be the site of a 13-vendor demonstration of a business-type network connecting equipment from DEC, Intel, Hewlett-Packard, Charles River Data, ACC, Honeywell, ICL and NCR. GM's industrial application network will link 13 devices from IBM, Allen Bradley, DEC, Gould Modicon, Hewlett-Packard and Motorola with Concord Data Systems equipment. Both systems will use standard NBS network protocols to allow file transfer applications across the network between any of the machines.

The two networks show how the ISO Open Systems Interconnect layered protocol (**Figure 1**) works, with this variety of vendors' computers linked for applications across networks with different access methods and physical topologies. Though the NBS protocols run with all of the various operating systems intact, the firms involved have invested the time and effort to develop the networking software to intercommunicate. Even the biggest companies are backing network standards here.

One network, in the GM-sponsored booth, follows the IEEE 802.4 token passing bus scheme over CATV cable for OSI layers one and two. The adjacent Boeing booth will show IEEE 802.3 CSMA/CD Ethernet-like baseband physical and link layers. Using NBS-standard



Concord Data Systems Token/Net Interface Module, the TIM 220.

transport layer protocol and a file transfer package at the seventh layer, the two networks allow applications resident on one machine to be displayed and manipulated on any other on the net. All of the participants have passed NBS tests for meeting their network standards.

It is significant that the booth organizers are major computer and networking end-users. General Motors has been active in promoting network standards in industry, and have chosen the 802.4 token bus architecture for their MAP system. Broadband and token passing are key features for factory automation systems, as

the multiple channels of broadband allow video and other services on one cable (many large industrial plants already have broadband cable installed) and token passing assures each device on the network a maximum access time to the bus, regardless of the loading. All of the networking is provided for the booth by Concord Data Systems, currently the only 802.4 compatible broadband network supplier.

In addition to the file transfer application running on both networks, the GM system will show process control across the network. Status and control information on a paint process and a robot in the booth will be accessible by any of the 13 devices connected.

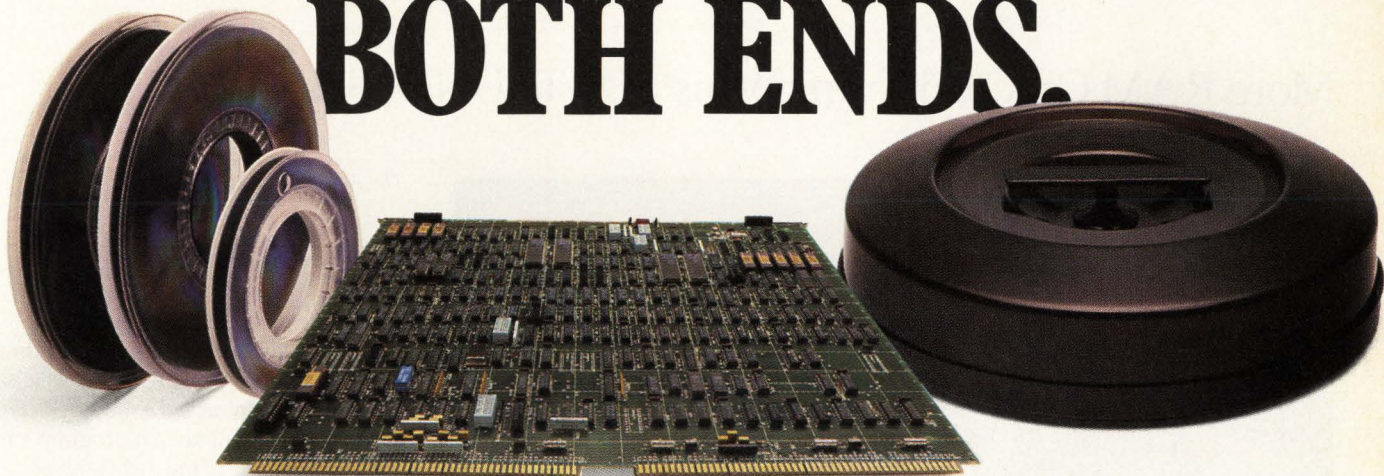
The CSMA/CD access method used in the second booth is well developed, as the IEEE standardization similar to the Ethernet scheme developed by Xerox, DEC and Intel several years ago. Three types of files will be transferable by this net: ASCII text, binary files and graphics formatted files. Three of the systems in this group use the UNIX operating system, and Charles River Data is using boards, from ACC, since both support the standard but only supplied one part or the other.

To allow all of the different equipment

Level 7 Application Layer	User interface into the network. Proposed are electronic mail, file transfer, virtual terminal services.
Level 6 Presentation Layer	Data formatting and translation for application use. Conversion utilities like compression, encryption and file formatting.
Level 5 Session Layer	For local and remote connection. Buffering, queuing and insulation of higher levels from physical location of processes.
Level 4 Transport Layer	Packet formation and flow control. End-to-end integrity of data assured.
Level 3 Network Layer	Data link routing. Uses only the links needed. X.25 Level 3, for example.
Level 2 Data Link Layer	Procedures for electrical interface control. Includes logical link layer. IEEE 802.3, 802.4, 802.5.
Level 1 Physical Layer	Electrical, mechanical, functional and procedural specification for connections. IEEE 802.2.

Figure 1: The seven layer ISO Open Systems Interconnect (OSI) model. Each higher layer uses and depends on the layers below.

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Looking at disk and tape control for Data General? You're probably looking at two separate controller boards. Which is one too many.

Spectra Logic multifunction controllers offer all the control you need, on just a single board. They're the smarter way to handle SMD/Winchester and 1/2-inch tape drives, because they've got you covered from both ends. But they do it in half the space and half the slots. Using half the power. And you're stocking half the spares.

So now buying separate boards for disk and tape makes no more sense than buying separate radios for AM and FM.

Our expanding family of Data General controllers offers you the performance you're looking for. We'll give you both ends for DG's NOVA® and ECLIPSE®/MV computers. And emulate DG's series of 6060 or 6160 disks and 6020 tape subsystems under RDOS, AOS, IRIS®, and BLIS/COBOL® without modifying your operating system.

But we'll also give you something extra: proven reliability. Because you're working with half as many parts and pre-tested ICs. Plus total FCC compliance and compatibility with DG's new hardened chassis.

You're also working with excellent documentation that's regularly updated. And the most comprehensive one year warranty in the industry. All backed by responsive nationwide service.

Spectra Logic. Our multifunction controllers double your control. And give you an advantage on the competition.

Look into Spectra Logic multifunction controllers for Data General computers. They could be all the control you'll ever need.

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	SPECTRA 17*/ SPECTRA 27	SPECTRA 110*/ SPECTRA 120	SPECTRA 10*/ SPECTRA 20
BUS (Disk)	Burst Multiplexor Channel	Data Channel	Data Channel
Disk Emulation	606X, 6122, 6160, 6161 (4 drives)	606X, 6122, 6160, 6061 (4 drives)	606X (4 drives)
Tape Emulation (Data Channel)	6021	6021	6021
Operating Systems (without OS patches)	RDOS, AOS/VS	RDOS, AOS	RDOS
Disk Transfer Rate (SMD)	2.0MB/sec	2.0MB/sec	2.0MB/sec
Supports FCC Chassis	Yes	Yes	No
*Single function disk controller			

Spectra Logic Corporation, 1227 Innsbruck Drive, Sunnyvale, CA 94089, (408) 744-0930, TWX 910-339-9566, TELEX 172524 SPL SUVL. International Sales Office: Belgium (32) (2) 5134892.

SPECTRA LOGIC

The Multifunction Controller Company.

on each net not only to hook into the bus but also communicate on the application level, the OSI transport layer four is written for each operating system. This requires no changes to any of the operating systems; the file transfer layer seven application is written on top of NBS pseudo layers five and six and the standard trans-

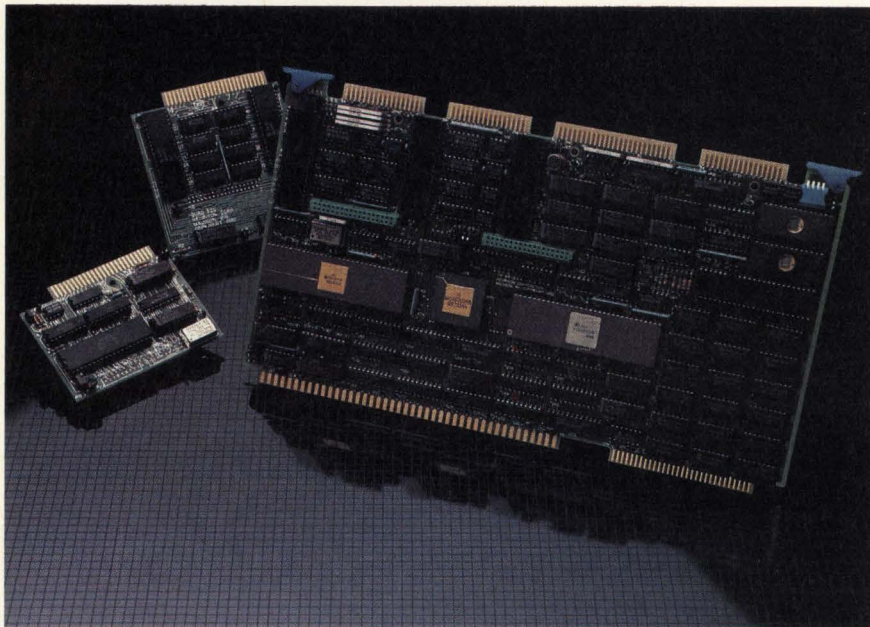
port layer. And though the physical and link levels for intervendor networking have been established in several forms for some years, the standard higher level protocols that truly allow applications to run across LAN links are being demonstrated for the first time with such a broad base of support.

With the backing of both computer and communications vendors and large-volume end-users, LANs based on the OSI model will soon become readily available, for true transparent local communications between any vendors' machines.

—Pingry
Write 231

DEPARTMENTS/Systems

More RAM On Card Transforms SBC To UNIX System



The HK68 with iSBX modules.

By adding more RAM on card, Heurikon Corp. (Madison, WI) has transformed its HK68 single board computer into a complete single board UNIX system, the HK68A. With the added dimension of 512 Kbytes or 1 Mbyte of RAM, the HK68A supports UNIX System III and V with drivers for Ethernet, SDLC/HDLC and floating point processors. Other possible operating systems include CP/M-68K, PolyFORTH, and Regulus.

Feature design is based on the MC68000. A quad channel MC68450 DMA controller has been included on the HK68A. The MC68450 is a 4-channel, 16-bit access controller with internal 32-bit addressing, byte, word, or long transfers, programmable priorities, vectored interrupt support, and both chained and unchained operational support. Conse-

quently, data transfers never tie up the MC68000 MPU.

The HK68 provides an MC68451 segmented memory management unit with logical to physical address translation and segment sizes of 256 bytes to 16 Mbytes.

The HK68 may be configured to include 512 Kbytes of dual access RAM accessible by the Multibus. A single DRAM controller chip makes the hardware memory refresh transparent to the MPU.

In accordance with IEEE-796 specifications, the HK68 interfaces directly to the Multibus with 16-bit data path and 24-bit addressing. Master/slave and multimaster modes are supported. An on-board byte-swap buffer allows the HK68 to interface easily with 8-bit peripherals and CPUs. The HK68 can support both Motorola and Intel data bus conventions

via hardware or software control.

An exclusive on-board watchdog timer is provided to prevent lengthy accesses from locking up on-card facilities. This HK68 feature will keep a program running under some of the most unexpected conditions.

Four serial ports are provided on the HK68 via two Z8530 (SCC) serial communication controllers. Each port has a separate software controlled baud rate generator, and all four ports support asynchronous or synchronous communications including IBM BiSync, HDLC, IBM SDLC, as well as others.

An 8-bit port with control signals is provided for interface to various hard disk controllers such as the Western Digital WD1001; the PRIAM Smart controllers; and the 1400-type controllers (SASI) available from several manufacturers. The port will support controllers for both 5 1/4" and 8" drives including the Xebec S1410. The port may also be configured to support the SASI standard as defined by Shugart.

Numerous systems and applications software packages are available, as well as system expansion cards and packaging. Twin Intel iSBX compatible expansion connectors reside on the HK68. These connectors allow any of the numerous existing plug-in modules to be used on the HK68 for various I/O expansion.

This specific array of features may make the Heurikon HK68 the only single board UNIX system available on the Multibus.

—Hanrahan
Write 235

Fingertip control

FLUKE 1722A INSTRUMENT CONTROLLER

Can make the difference
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Touch Here

The Fluke 1722A Instrument Controller

Of course, the biggest difference is 1722A touch-sensitivity. It will make your system truly user-friendly. And that sells systems!

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Designing the 1722A into your system is no problem. It's fully integrated and features a high-performance micro-computer, graphics display, 400K disk drive, complete software packages, plus RS-232-C and IEEE-488 I/O ports.

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Panel or rack mountable, the 1722A fits right into your OEM system.

get Fluke support. You're working with a multinational corporation and worldwide service organization.

The 1722A Instrument Controller is available, on an OEM basis, in as few as

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Consider the 1722A in your next development. It will make your OEM system easier to build, to sell, to use, and to support. That's a big difference!

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Write 12 on Reader Inquiry Card

THOMAS EDISON DIDN'T
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INVENT THE LIGHT BULB. MAKE IT WORK.

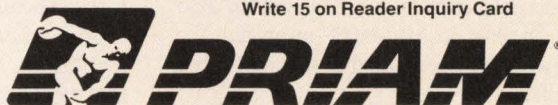
Fifty years before Edison, people were taking the air out of glass tubes, sending in current and hoping the filament would glow.

But in 1879, Edison attacked the bigger problem of how to distribute the electricity. So that by developing the power grid first, he was able to determine the precise combination of carbon rod, vacuum, voltage and current that his lamp would demand.

At Priam, we build our disc drives with a similar focus—on your system's requirements, and on your production schedule. It's a commitment that has made us the leading U.S. manufacturer of high-performance, high-quality 8" voice-coil Winchester—from 35 to 500MB. A commitment we're now making to our new 86MB 5¼" drives as well. It's why we provide total, industry-standard interface support, including ST412, ANSI, SMD, SCSI, IPI-3, and our own Priam interfaces. And it's why we've just opened a new, automated production facility, one of the largest and most modern in the OEM world.

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Merlin Brings Magic To Graphic Systems

Each summer during the computer graphics conferences, landmark announcements are made for both hardware and software. This June, Megatek, the San Diego-based manufacturer of computer graphics systems, has announced such a system. The Merlin 9200 series of multiprocessor based graphics display systems is worth this type of recognition because it incorporates features that indicate the advancement of graphics systems design and provides the benchmark against which other high performance systems manufacturers must compete. Last summer, for example, Ramtek announced its 2020, another multiprocessor display system which established performance benchmarks for speed. The tug-of-war for recognition of the system with the greatest horsepower continues with the Merlin announcement. An important distinction in this announcement is that it unites functions which until now were found only on different manufacturers' systems.

Architecturally the system is similar to earlier dual bus Megatek designs, with additions in database management software and systems communications. The former is presented as having special advantages in applications such as solid modeling in that complex geometric shapes can be stored in an efficient manner.

Rather than compete with other graphics systems manufacturers for display resolution and refresh rates, Megatek has developed a unique approach to displays which it has named "pixel phasing" (patent applied for). There will be some confusion about classifying the approach as either raster or vector, but the company notes in its technical documentation that it is calligraphic. The display provides a window of 1280×980 pixels into a virtual screen of 3072×2304 with a 60 Hz non-interlaced monitor. The display also introduces a 16-bit matrix approach for hardware anti-aliasing that is remarkably effective.

The performance characteristics, however, that affect industry's overall perception of "state-of-the-art" include features such as translucent displays, XYZ clipping, Gouraud or Phong shading, surface



The MERLIN 9200 multiprocessor-based display system.

texturing and patterning, mesh generation, and depth cueing (which includes both object brightness and perspective). While all of the high performance display system, manufacturers vie for recognition of their dynamic capabilities, pixel write time, and refresh rates, there is notably little competition for performance in both rendering and speed.

While the system retains the dual processor-memory bus approach to system architecture, common to high performance systems from Ramtek, Jupiter, Ikonas, and others, it has added other features. The user may decide, for example, to implement either Gouraud or Phong techniques for shading and light source that most others perform in software. Use of a 16-bit Z buffer brings the company into competition with the high performance geometry engines from Lexidata, GTI, and Raster Technologies. The use of Z plane memory not only enhances ren-

dering functions, but is used for 3D functions such as clipping and transformations. Finally, the announcement indicates the firm's willingness to continue development of its own software.

The overall effect of Merlin is to continue the impetus of dividing the system into discrete functional units: display processor, geometry processor, frame buffer, and CPU. Other processes which are taxed in systems with high levels of performance include data handling for high speed video and input/output handling where supplementary processors are being applied. As manufacturers enhance performance in each of these areas, the OEM is confronted with demands by users for what they perceive to be the basic features; this in turn makes the graphics systems industry one of the fastest changing areas of computer technology.

— Borrell
Write 239

DIGI-PAD® WORKS WHERE YOU WORK

DIGI-PAD digitizer tablets perform in the real world. They won't quit over spilled coffee! They are unaffected by dirt, graphite, moisture, or perspiration on the tablet. And DIGI-PADs are insensitive to acoustic noise, magnets, vibration, or pressure. In fact, DIGI-PADs will work in almost any environment you will. That's because they use our reliable absolute electromagnetic sensing technology. And GTCO is the largest producer of digitizers using electromagnetic technology.

Most other digitizers are not as tolerant as a DIGI-PAD. So make sure that the digitizer you choose won't fail or require adjustments because of heavy use or environmental factors.

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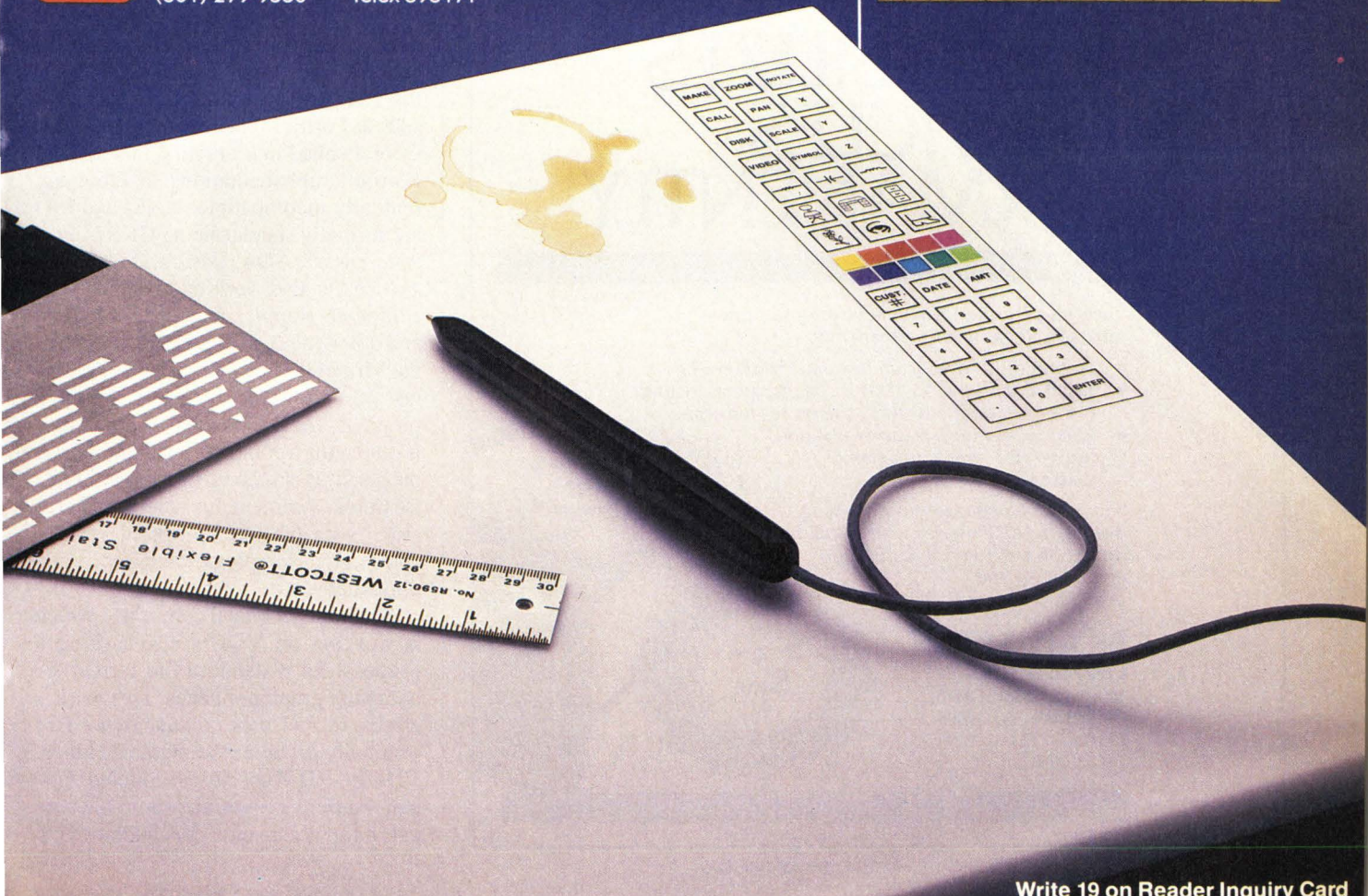
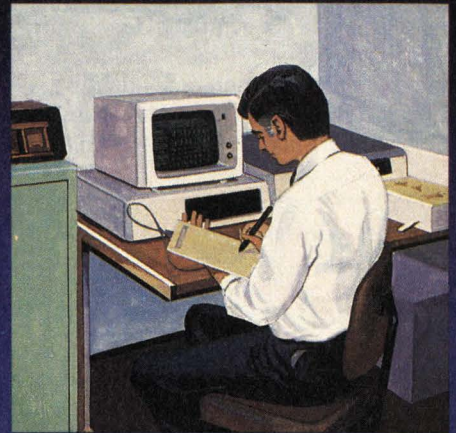
DIGI-PADs are available in sizes from 6" x 6" to 42" x 60", all using the same patented electromagnetic technology. They have been field proven in military, industrial, technical, business, and educational environments. DIGI-PAD is compatible with nearly all computers, from PC to mainframe. Most models are in stock for quick delivery and all comply with pertinent EMI and safety standards.

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The Status Of Computer Graphics Standards

Most early efforts to standardize computer graphics concentrated on software interfaces. Now, software standards are nearing final adoption, and attention is turning toward hardware standards, as well as extensions and improvements to the software standards.

The Association for Computing Machinery (ACM) developed a proposal in the 1970's called the "Core System." It was a collection of functions which could be implemented as subroutines in a programming language like Fortran. Several vendors produced software packages purporting to follow the Core proposal, and some manufacturers even put Core functionality into firmware in intelligent graphics terminals.

In 1979, the American National Standards Institute set up a technical committee named "X3H3," with the goal of turning Core into an American National Standard. In the same year, ISO established a committee to work on graphics standards called "TC97/SC5/WG2". For the next four years, American vendors and users of computer graphics sent roughly 50

experts to three and four meetings a year to contribute to the effort, and to protect the interests of their institutions and companies. Progress was substantially slower than anticipated.

Meanwhile, the ISO committee members were principally Europeans with just a few delegates from ANSI in the USA. With less substantial investment to protect, this group worked to refine and adopt a proposal which originated in Germany; the Graphical Kernel System (GKS). GKS is now a Draft International Standard (DIS 7942). The final letter ballot on GKS was held in December, and all of the "NO" votes have now been resolved. The final letter ballot did instigate a number of editorial changes to the GKS document, when these have been approved, (the French translation is available) GKS will become an International Standard (IS). Meanwhile, ANSI has undertaken to adopt GKS as an American National Standard. ANSI has published GKS as draft proposed American National Standard X3.124, and is currently in a stage known as "public

comment phase," in which any member of the public may order a copy, study the proposal, and submit comments and suggestions for the ANSI technical committee to process. This period will end on July 1, 1984. Support for the proposal on the technical committee is high. There was only one "NO" vote on GKS; the ACM special interest group on computer graphics (SIGGRAPH), the group which originally wrote the Core proposal.

The Core proposal and the GKS proposal are similar. One difference is that Core addresses 3-Dimensional computer graphics as well as the 2-Dimensional graphics addressed by GKS. Today, an ISO project is underway in the Netherlands to extend GKS from 2-D to 3-D. Initial working papers from the group doing the work look promising, and a draft will be circulated at the next meeting to be held in June 1984 in France. The 3D-GKS proposal even solves a serious technical flaw in Core 3-D graphics, the inability to deal with high performance 3-D displays capable of performing real-time perspective rotations.

Both the GKS and the Core proposals are abstract descriptions of what functions should be available to an applications program. Neither specifies what the names of the functions should be, or how their data is to be passed back and forth. To make such a specification is to "bind" the standard to a particular language, such as Fortran. The lack of bindings for Core resulted in a situation in which all Fortran implementations of Core are mutually incompatible. ANSI and ISO are formally standardizing GKS in Fortran, Pascal, ADA, Basic and C.

ANSI is also working to standardize computer graphics terminals, plotters, and other devices. This effort, known as the Virtual Device Interface proposal, is not yet as fully-developed as the GKS proposal. Today, the technical committee is reviewing a complete draft of the VDI proposal. It is scheduled to be available for public comment this winter. It shares much with the GKS proposal such as common terminology, functions, and philosophy.

The same technical committee which is working on VDI is also writing a proposal for a standard file format for computer graphics images. This work is closely related to the commands used for originally creating the picture. Hence, VDI and VDM are closely coupled. One major difference is that a picture file does not have commands for interactivity.

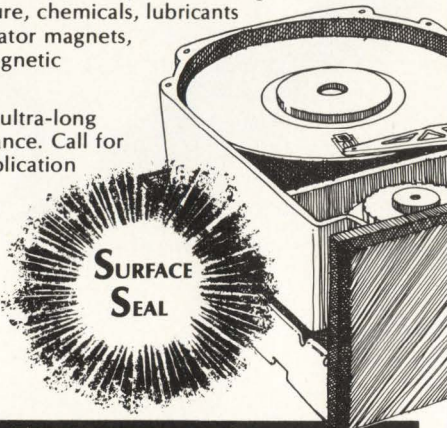
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Those commands are a part of VDI but not VDM. The VDM is more mature than the VDI and is now available for public comment, just as is GKS.

While GKS standardizes the interface between application programs and graphics software, it does not standardize all of the functions which are desirable for computer graphics. One particular area omitted from GKS (and Core) is hierarchical pictures. In a hierarchy, objects contain other objects, which may in turn contain still other objects. This is an important part of the design process, and unfortunately neither GKS nor Core address hierarchy very well. Another group within ANSI is working on the Programmer's Hierarchical Interactive Graphics System (PHIGS). Logically, it is an extension of the functions standardized by GKS including a richer tool-set for graphics. This proposal is still in the draft stage, and is scheduled for public comment this winter. One important issue facing PHIGS is compatibility with GKS. Al-

though PHIGS shares many GKS terms and functions, the current PHIGS proposal is not compatible in that application programs written to work with GKS software would not be able to use PHIGS software directly.

There are other standards which relate to computer graphics. For example, the NAPLPS, or North American Presentation Level Protocol Syntax, has been adopted simultaneously in Canada and the US. It provides a common standard for the communication and display of information via videotex networks. It is not a general-purpose computer graphics interface, but is intended to support activities like browsing through "electronic catalogs" in one's own home.

Initial Graphics Exchange Standard (IGES), adopted as ANSI Y14.26M, is a standard format for exchanging computer graphics design databases between different design systems. Note that it standardizes designs format, not pictures. It is easily confused with VDM, but is

really quite different. Designs are much more than pictures, containing materials specifications, tolerances, and other types of data.

If you would like to review drafts of standards under development, the proper way and time is to review them during the official public comment phase. Standards relating to computers are handled by Technical Committee X3. For more information, write to: X3 Secretariat/CBEMA, 311 1st Street NW, Washington DC, 20001.

If you know the document you want, enclose a check to cover copy and mailing charges (\$35.00 for X3.124, dpANS GKS, \$20.00 for X3.122, dpANS VDM), and a self-addressed mailing label. In order to review documents before they reach public comment phase, such as VDI and PHIGS, the best way is to become an active member on the committee doing the work.

— Dave Straayer, Tektronix,
Wilsonville, OR

DEPARTMENTS/Memory

DRAMs Go CMOS

CMOS technology provides many solutions to the problems traditionally associated with NMOS, and brings with it many coherent advantages. Currently, the density and speed of CMOS is chasing that of NMOS, and in addition it provides a reduction of device power consumption that lowers system power requirements by allowing less costly power supplies. Device reliability problems are more easily solved, and in addition, a cooler die can help solve some VLSI packaging problems, particularly in high reliability plastic packaging.

CMOS 64K dynamic RAMs are expected to open a number of new markets for dynamic RAMs, including portable and personal instruments and new kinds of graphics terminals and displays. The 51C64 and 51C65 are the first members of a new family from Intel, bringing the companies CHMOS technology to fabricate DRAMs.

In the active mode of operation, these devices have significantly lower power consumption than their NMOS counterparts. In addition, because of reduced internal clocking made possible with the

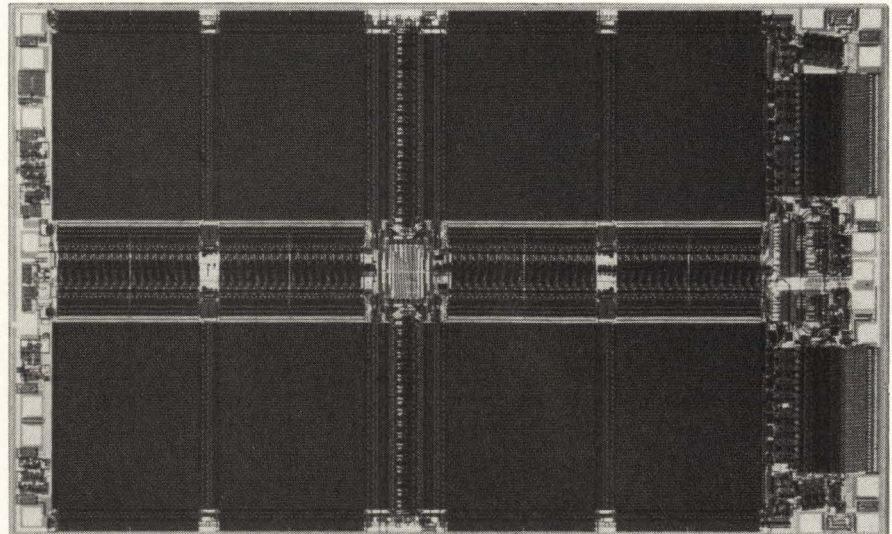


Photo micrograph of Intel's 51C64, 64k x 1 CHMOS Dynamic RAM.

CHMOS design, the current transients on the system power buses during active cycles are less severe, a feature that helps to reduce noise and decoupling requirements.

The greatest power savings of CHMOS occur in the standby mode. Here, the cur-

rent drain is only a function of internal leakage paths and consequently, is very low. The low-power version of the CHMOS DRAM (51C64L or 51C65L) has a standby current in the microampere range.

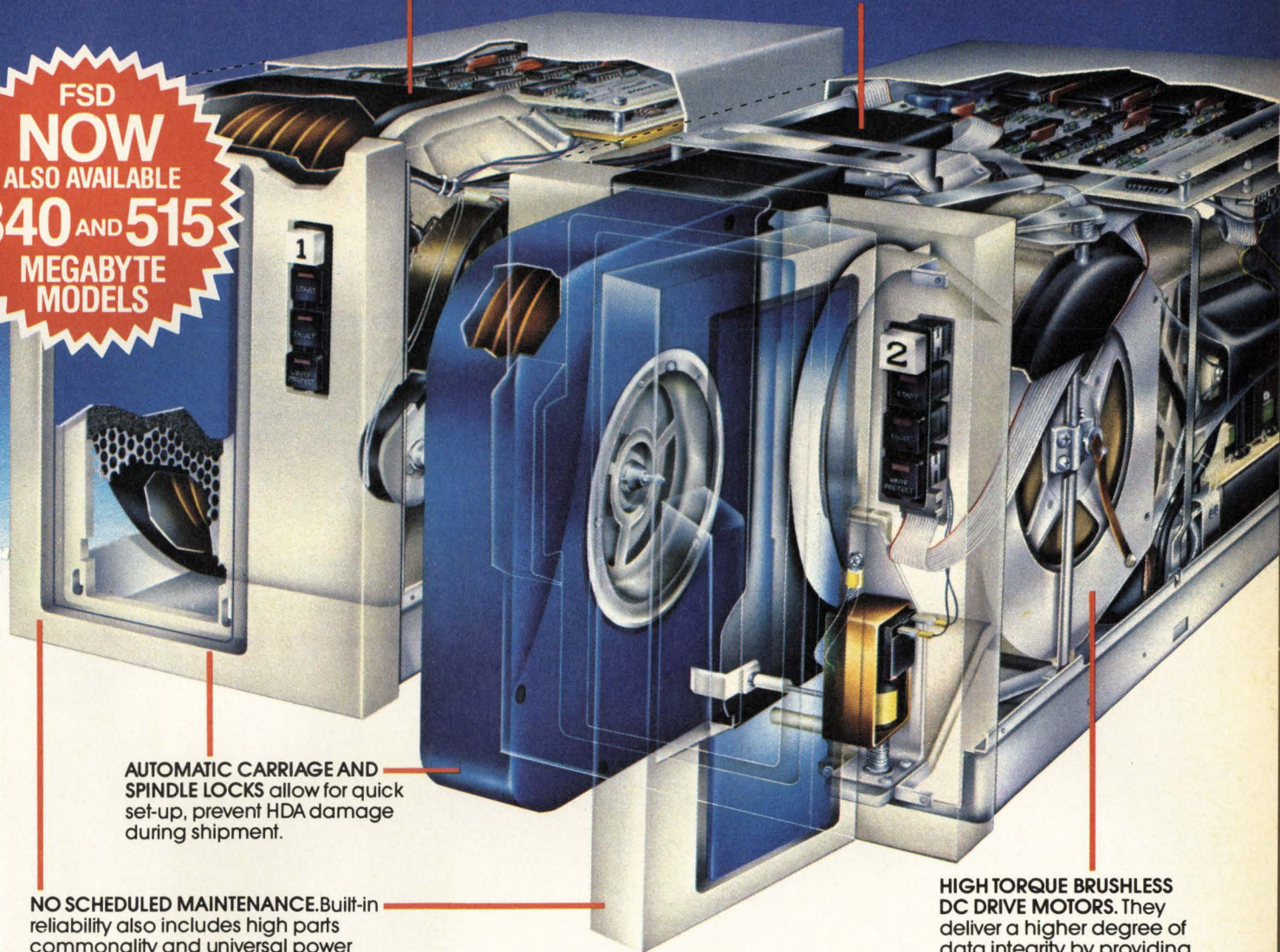
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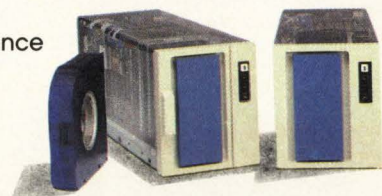
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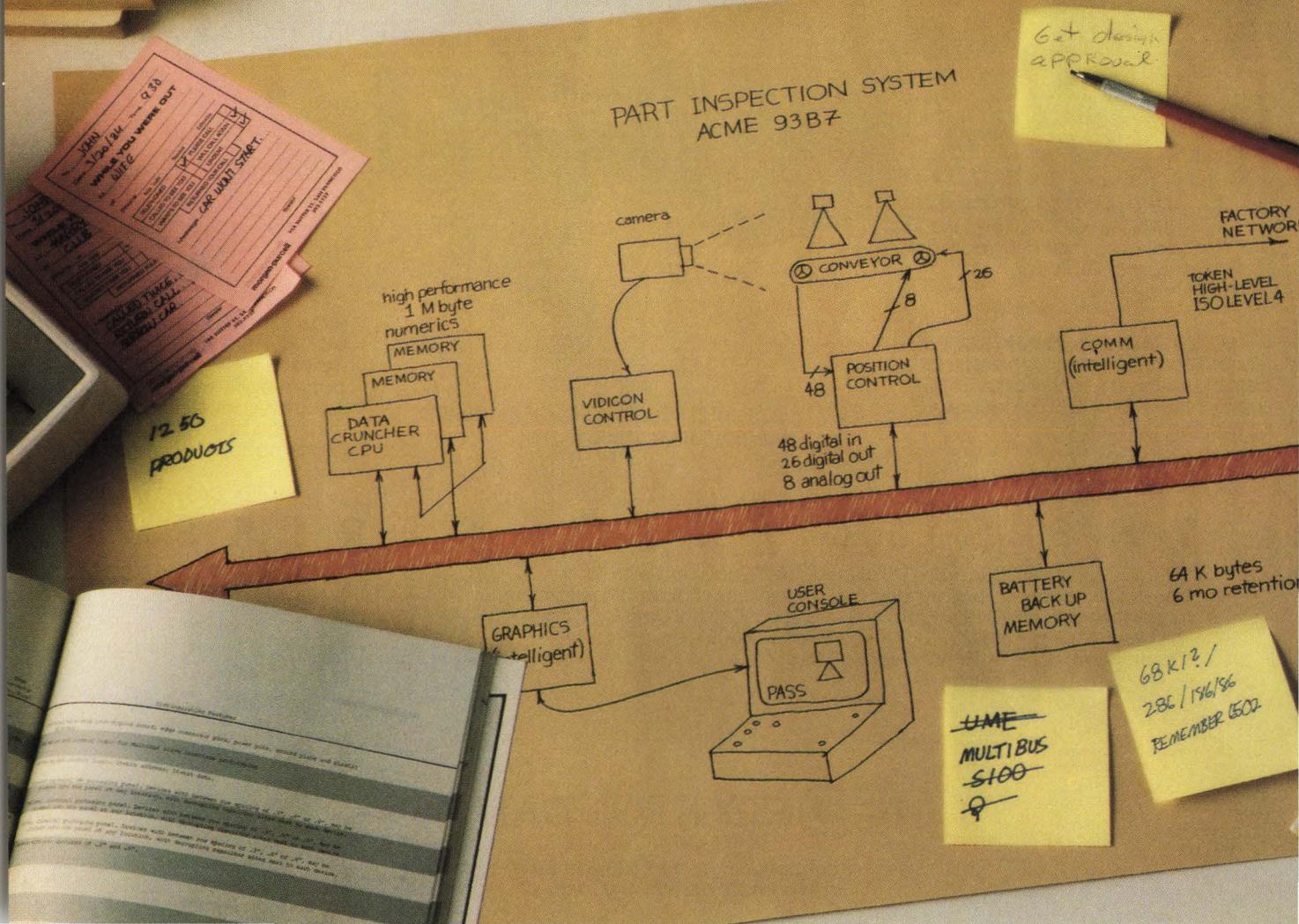
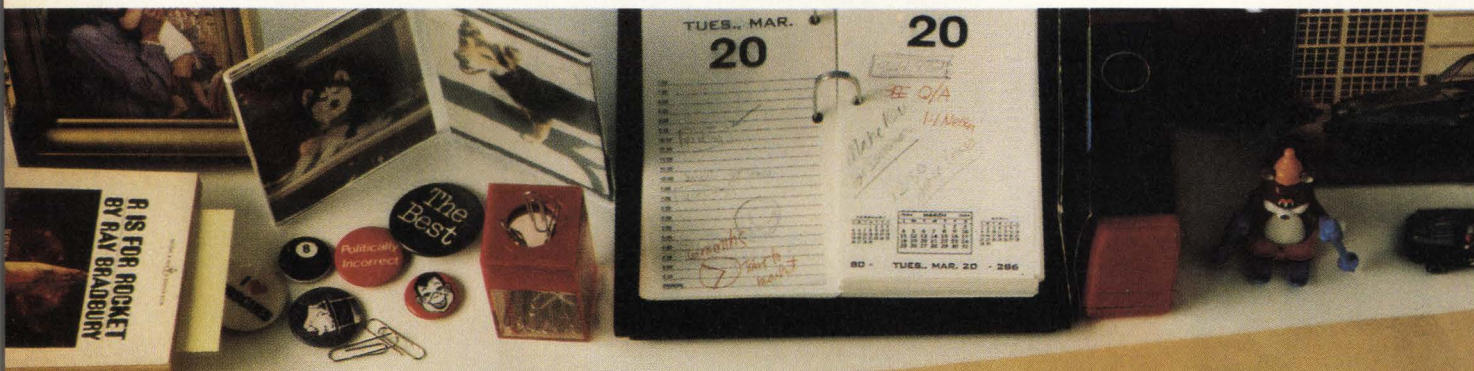


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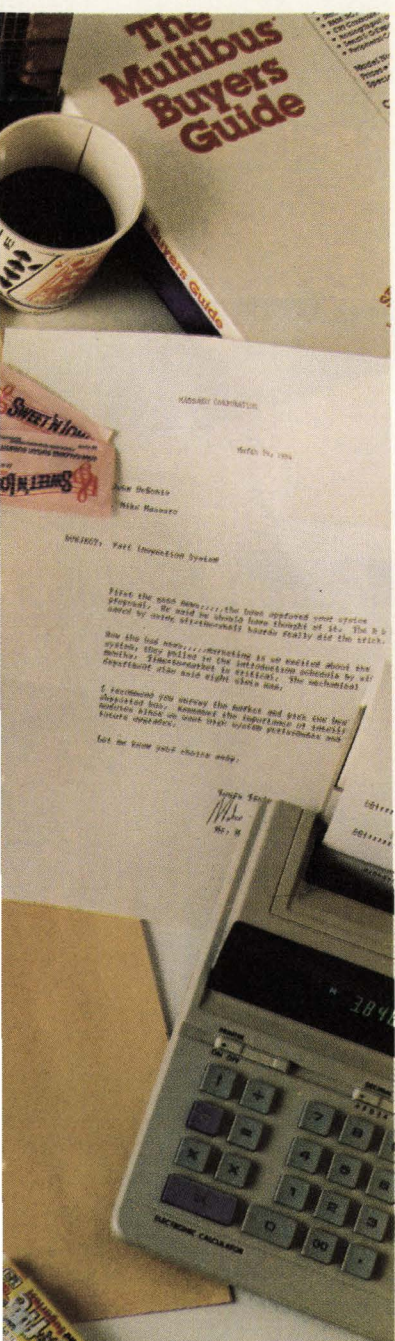
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two new methods of gaining access to data; Ripplemode (51C64) and Static Column Mode (51C65). The Ripplemode operation provides the ability to randomly read or write any series of bits within a single row at minimum cycle time of 65 ns. Ripplemode operation is particularly useful for graphics applications. Static column mode offers equivalent high performance and essentially makes the dynamic RAM act in a manner similar to a static RAM, and permits all 256 bits within a device row to be accessed at a data rate potentially faster than Ripplemode.

Three article reprints are currently available from Intel to help the systems

engineer with his designs: "CHMOS DRAMs in Graphics Applications, AP: 172," "Systems Implications of CHMOS Dynamic RAMs, AR: 311," and "Static

Column Architecture in CHMOS Dynamic RAMs - A Graphics Memory Solution, AR 312." - *Wilson Write 238*

FEATURES FOR TODAY'S APPLICATIONS

Application Need	CHMOS DRAM Feature	Benefit
■ High Serial/Random Bandwidth (e.g. graphics, array and signal processors).	Ripplemode™ or Static Column Mode.	Cycle Times As Low As 65nsec.
■ Low Power For Portable Instruments and Computers	CHMOS DRAM Technology and Extended Refresh.	DRAM Density With The Standby Currents Of CMOS SRAM.
■ Fast "Usable" Speed	Flow Through Column Latch and Fast Precharge.	Wide T _{RCD} Window and Fast Cycle Times.

DEPARTMENTS/Peripherals

High Speed Printer Uses Magnetic Drum

To date there have been only two types of high speed non-impact printers: electrostatic (Xerographic) or electro-optical (laser). Both types, which are capable of printing thousands of lines per minute, use a photosensitive drum which records a latent electrostatic image. These sophisticated devices have traditionally suffered from the same problems, notably unpredictable drum life. They have histories of frequent maintenance, and are sensitive to humidity. Laser printers tend to print large black areas non-uniformly. In addition, both types may require special paper. In some cases, suppliers of high speed printers base their prices on the volume of pages printed each month, in order to help defray the increased maintenance costs which accompany higher printing volumes.

Cynthia Peripherals Corp. (Sunnyvale, CA) uses a new technology, magnetic perpendicular printing, to avoid these problems while reducing costs. The MP60 series printer uses a 100mm diameter magnetic drum rotating at a constant speed of 12.5 in/sec. The drum is first demagnetized, then magnetically recorded by the printing station, consisting of 3360 recording heads with a resolution of 240 x 240 dots/in. Unlike most magnetic recording, in which the magnetic flux is recorded longitudinally between two pole pieces of equal size, the MP60 series uses one small pole piece and one of large size a significant distance away. The large



The MP6090 uses magnetic perpendicular printing with a 100 mm diameter magnetic drum rotating at a constant speed of 12.5 in/sec.

pole piece acts as a flux return in which the flux is distributed over an area of such size that it does not materially affect the magnetization of the drum. All recording

is done at the small pole, where the magnetic flux is perpendicular to the surface of the drum; hence the term "perpendicular recording."

The lean, mean plotting machine from Houston Instrument

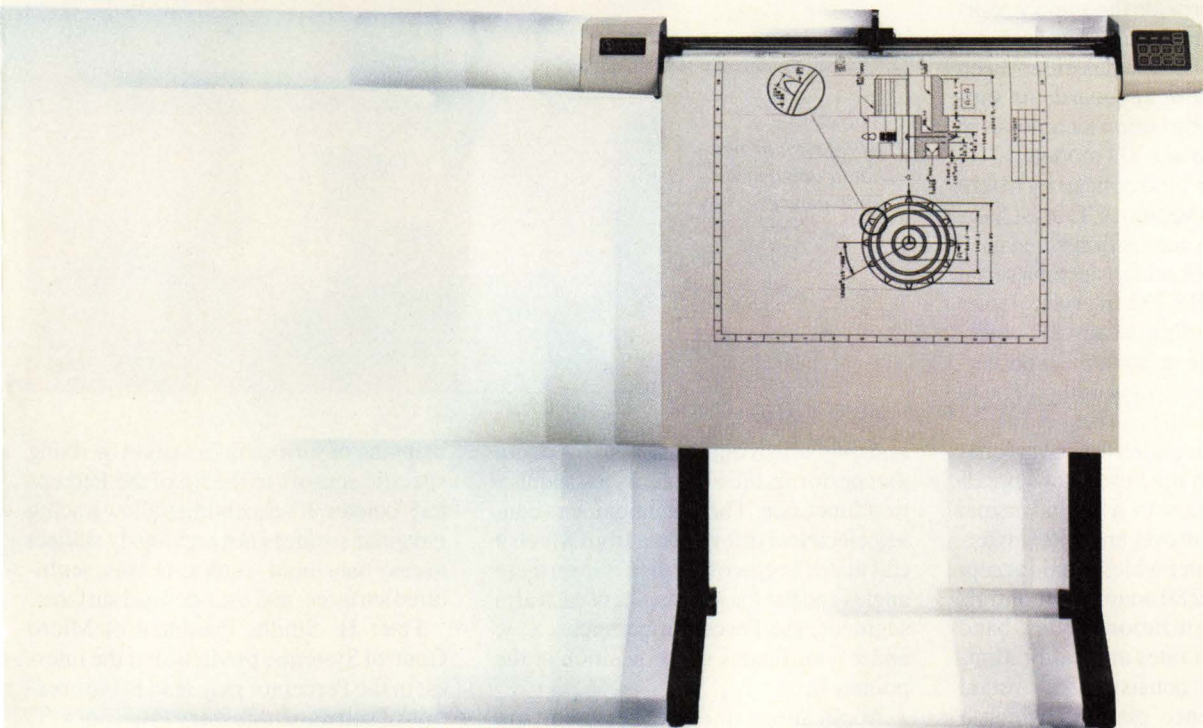
Houston Instrument's brand new servo driven DMP-51 is the fastest drum plotter we've designed to date. This superb plotter offers a pen speed of up to 22 inches/second; programmable accelerations, and a pen-on-paper resolution of 1/1000 of an inch! That means you'll turn out quality 17" x 22" and 22" x 34" drawings a lot faster, increasing your firm's productivity and profitability.

Now, for more good news. The DMP-51, priced at \$4,495*, is as fast as other plotters costing three times more. At that price, you can afford to put a DMP-51 at individual drafting work stations.

This is the professional plotter that meets the needs—and the budgets—of all companies, large or small.

The DMP-51 is intelligent, too. The DMP-51 can execute complex graphics operations from the simplest commands. A mechanical/architectural version, the DMP-52, with its 18" x 24" and 24" x 36" paper size, is available for the same price from Houston Instrument.

So, watch our new plotter in action . . . it won't take much time to realize it's the best buy for your money. For the name, address and phone number of your nearest dealer or distributor, write Houston Instrument, 8500 Cameron Rd., Austin, Texas, 78753. You can also call 1-800-531-5205 or 1-512-835-0900 (Texas residents). In Europe, contact Houston Instrument Belgium NV, Rochesterlaan 6, 8240 Gistel, Belgium. Tel: 059-27-74-45. Tlx: 846-81399.



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The recording process is repeated over successive regions as the drum rotates. The dot configurations produce a latent magnetic matrix forming an image of the page to be printed. The result can comprise any combination of alphanumerics or graphics.

After the magnetized regions have passed through the toning station, dry magnetic ink particles adhere to the drum. The ink toner is a single component consisting of thermoplastic resin particles ranging in size from 10 to 50 microns, enclosing several submicron magnetic fillers. The single component toner provides a consistent and predictable image. The image is developed by pressing the toner against the drum with a wedge. The image is then transferred onto plain paper by means of a pressure roller. The friction and rolling process is mechanical, and as a result does not suffer from humidity problems as does Xerography. The remaining toner is scraped away and the process begins again.

The magnetic process offers several

significant advantages, notably 10-million-page drum life and 8500-hour recording head module life. The heads are accessible for cleaning by the operator, reducing service calls.

The MP6090 is capable of printing 88 pages (6000 lines) per minute at a resolution of 240×240 dots per inch using conventional fan fold paper. Four sets of 96 characters each can be rotated to four positions. Character pitch is user-selectable, and may be mixed within a page. The unit includes complete mechanical and electrical diagnostics. An optional floppy disk drive allows storage of font libraries and development of a library of electronic forms. The on-board buffer stores 12K characters and can be expanded to 24K. The printer is manufactured in France by Cynthia's parent company, the Bull Group.

For automatic checkwriting, mass mailing, billing and similar uses where fast, reliable high volume printing is a must, the Cynthia MP6090 provides an attractive alternative.

—MacNicol

MP-6090 Specifications At A Glance

Speed: 68 8½" × 11" pages/min or 6000 lpm at 8 lpi.

Resolution: 240 dots/in vertical or horizontal.

Character Pitch: 6, 8, 10, 12, 15 or 20 chars/in, user selectable, mixable within a page.

Character Rotation: 90, 180 or 270 degrees.

Buffer: 12,000 characters, 24,000 optional.

Character Set Capacity: 512 characters, user selectable.

Bused Control Lines: 48.

Enable Lines: seven per module, ten modules.

Control Current: 70 ma.

Control Time: 4 microsec.

Price: Under \$50,000.

Write 233

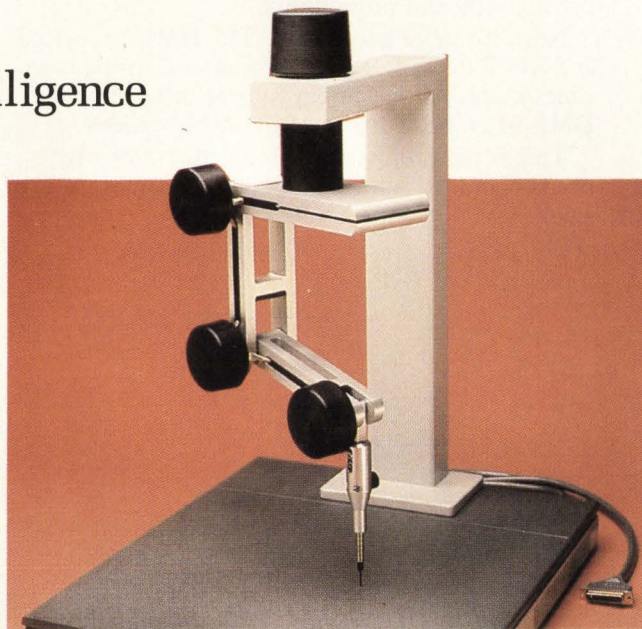
3D Digitizing With On-Board Intelligence

Until recently, computer graphics users have relied upon various 2-dimensional input devices to provide the x and y coordinates of a point in a 2-dimensional space. The z coordinate has either been entered through the keyboard, or supplied through construction techniques in software to arrive at a 3D model.

"The Perceptor", introduced by Micro Control Systems (Vernon, CT) at NCGA, performs 3D data acquisition when used with any computer which accepts serial input through an RS-232 interface. Users can interactively digitize any 3D object however irregular its surface. The Perceptor can interface to any computer and in order to achieve this, an on-board processor (Z80A) was added to convert analog readings from the Perceptor's precision potentiometers to a digital signal which could be sent over an RS-232 interface to any computer which would accept serial input. The Z80 board also controls four different digitization modes, baud rates, digitization rates and calibration.

The Perceptor consists of a ground aluminum reference plate on which a frame is mounted and to which a precision-machined digitizing arm is attached. Beneath the referenced plate is a metal

The Perceptor brings 3D data acquisition to input devices.



housing which encloses a circuit board that performs the electrical data acquisition functions. The potentiometers convey electrical information from which it calculates angles of rotation. Given these angles and the known lengths of each arm segment, the Perceptor computes x, y, and z coordinates of the position of the pointer tip.

Applications for the Perceptor are widespread, ranging from interactive 3D CAD, to contour analysis of virtually any object, to medical applications, or field

mapping of various information by fixing specific sensors to the tip of the Perceptor's pointer. Its capabilities allow tracing irregular surfaces not previously subject to easy data input, such as curves, sculptured surfaces, and user-defined surfaces.

Peter H. Smith, President of Micro Control Systems, predicts that the interest in the Perceptor may lead to the creation of software necessary to accept x, y, and z coordinate data, where only x and y exist now.

—Hanrahan
Write 244

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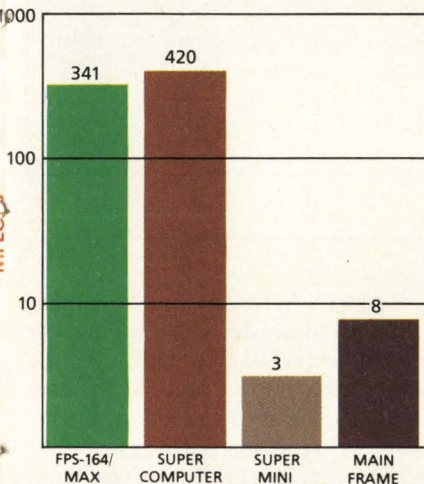
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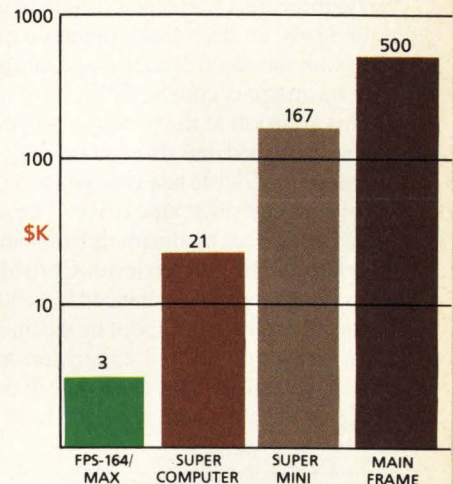
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Number of Independent Processors	1
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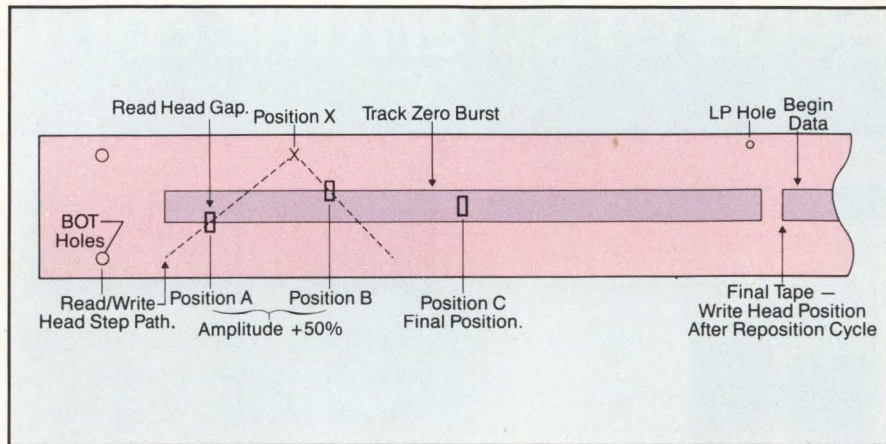
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Track Zero Sensing Streamer Enhances Tape Interchangeability

Higher track densities (9 to 16 tracks) in today's 1/4" streaming cartridge tape drives mean correspondingly smaller track sizes than those in older, lower track density devices. While low density tapes (typically four-track) have track widths of about 25 mils, track width in high density tapes may drop to as little as six to eight mils. While normal tape wander of about two to three mils is acceptable with larger track sizes, in high track density tapes such wander could reduce signal amplitude by an unacceptable 50%.

This solution to the problem borrows from established disk drive technology to reference read/write heads to data in a 1/4" streaming cartridge tape drive. The approach enhances media interchangeability and reliable data retrieval. Cartridge interchangeability is enhanced by reducing problems brought about by mechanical tolerances, thermal expansion and possible misalignment due to age of cartridge or drive. Referencing the head to



Zero Track Sensing Process.

the data reduces the amount of signal reduction introduced by normal tape wander, thus improving data integrity and retrieval.

The figure shows how the drive design

of Wangtek's Series 5000E Streaming Cartridge utilizes the zero track burst at the beginning of the tape to reference the read/write heads to the data under microprocessor control. In operation, a firmware program running out of an Intel 8749 micro directs the reading of the tape, from the beginning tape holes (BOT), and steps the head across the tape, storing the zero track burst signal amplitude. The micro notes the head position where the amplitude is 50% (position A), and continues to move the head until the amplitude is zero (position X). The head is then stepped back down, while the tape continues to be read, until the signal amplitude is again 50% (position B). The micro records this position. The read/write head is then positioned at a point half way between positions A and B (position C).

According to Richard Lewis, director, streaming tape engineering at Wangtech, Simi Valley, CA, solving the problem of streamer cartridge interchangeability and data integrity will enhance streamer cartridge acceptance, and open the way for even higher density recording. "We feel it is no longer acceptable to design units that look for data where it is supposed to be by simply measuring from the edge of tape." Apparently the Quarter Inch Cartridge Committee agrees; the approach outlined here will be a part of the QICC-24 specification, according to Lewis. Production units Wangtech's 5000 E (E for enhanced with the use of this head positioning approach) are now becoming available.

—Cashman
Write 236

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Silicon Software Components Require No Modification

The acceptance of advanced 16-bit microprocessors may have been somewhat slowed by the high cost of writing operating system software. Programmers developing "real-time" applications for embedded 16-bit microprocessors have found that as much as 60% of their time is spent designing and writing the operating system.

Hunter and Ready Inc. (Palo Alto, CA) have developed a family of products offering a new approach to software integration. The company produces operating systems based on "silicon software" components that can be put to work with virtually no modification. A silicon software component is basically an executable version of a microprocessor program designed so that it can be shipped like a VLSI component, usually in a PROM. The methodology permits the same component to operate completely unchanged on all board-level microcomputers that use the same microprocessor.

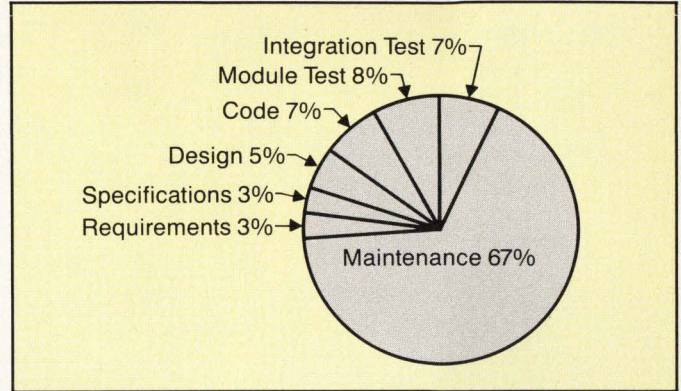
"Silicon software" was coined to describe code frozen in silicon and cannot be modified by the user anymore than the microcode of the 68000 will be modified by the user.

Hunter & Ready has recently announced FMX and IOX, two components that simplify the development of real-time operating system software for applications such as industrial process control, analytical medical instruments and telephone switching devices. Designers are provided with a standard operating kernel that can be used without modification on all board-level microcomputers that share the same microprocessor. With FMX and IOX, programmers of real-time operating system software no longer have to write source code for file management or I/O functions. Six months to one man-year may be shaved off development time.

Both devices work in tandem with the Versatile Real-Time Executive (VRTX), an operating system kernel that can be used without modification to control applications based on Intel's 8086, 8080 or Motorola's MC68000.

Previously, off-the-shelf operating systems had to be modified at the source code level to be functional. Hunter & Ready created standard components that could be linked together like large scale integrated circuits so that designers don't

Software maintenance costs are significantly greater than software development costs. Maintenance represents between 60% and 70% of the total software costs, with development accounting for only 30% to 40%. (source: Zelkowitz, Prentice-Hall, 1979)



have to reinvent operating systems for each new product.

Typical operating system software packages are characterized by board-level dependencies. The VRTX offers the same operating system kernel can be used without modification on any board-level

microcomputer that uses the same microprocessor.

The potential for industry is that the VRTX and the FMX and IOX software components can drastically reduce the expense of getting new microprocessor-based products to market. —Hanrahan

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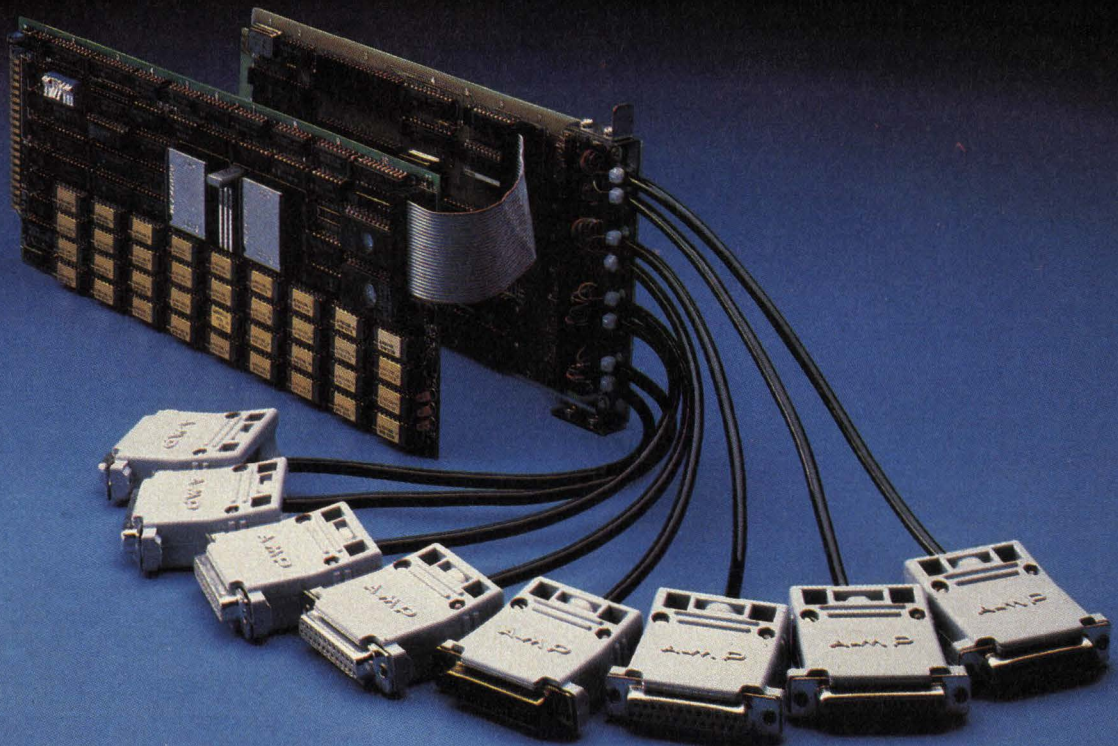
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Multiple Bus Structures And Custom Chips Increase Multiuser System Performance

by Andrea Coville,
New Products Editor

Multiuser systems encompass an area so broad that more than a hundred manufacturers offer systems for a multi-user environment. These computers range from mini-based systems to single microprocessor systems to multi-microprocessor systems. Rather than discuss the architectural variations in these three categories, this review will focus on one segment, the single microprocessor-based small system.

Minicomputer Roots

When looking at multiuser systems today, it is important to look at the architecture of minicomputers to discover which of their features small systems emulate.

Architecturally, a VAX 11/780, which has a 32-bit CPU, is a good example of a minicomputer from which microcomputers have drawn certain portions of their designs. The VAX processor can directly address four billion bytes of virtual address space and includes memory management hardware, 16 32-bit general registers and 32 priority interrupt levels.

Figure 1: The Series 9 from Molecular Computer is a multiuser system based on a proprietary LAN-in-a-box architecture and n/STAR network operating system.

In multiuser systems, memory management allocates large amounts of memory space to each user and is responsible for protecting tasks from each other.

In a minicomputer system cache memory reduces the effective memory access time for the CPU by providing high speed data access that stores frequently refer-



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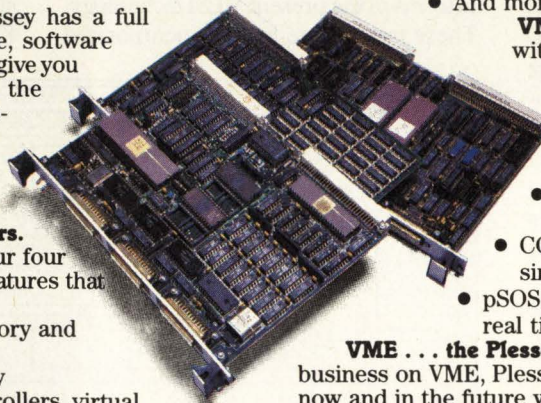
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When looking at multiuser systems today, it is important to look at the architectures of minicomputers to discover which of their features small systems emulate.

enced items like addresses, data and instructions. The implementation of cache significantly boosts performance in multiuser designs.

In both minicomputers and microcomputers, a bus is the primary interface to disk drives, tape transports and peripherals. Conventional controllers and their associated interfaces have become bottlenecks to systems' performance. In the minicomputer environment, this has led to proprietary schemes of partitioning systems intelligence. Similarly, several new I/O bus structures have been introduced in microprocessor-based systems to enhance throughput.

The disparity among minicomputer operating systems is due in part to their individual histories and hardware configurations. This is not the case with microprocessor-based small systems, where operating system software is fairly standard among models; MP/M, Concurrent CP/M-86, MS-DOS, CP/M and different implementations of UNIX are the most common. Many improvements have been made on UNIX software to produce its current versions. UNIX has been designed around certain common problems in multiuser environments such as extensive disk activity and memory management, which require hardware as well as software solutions. In summary, certain architectural features of minicomputers are reflected in micro-based multiuser systems.

Multiuser Architectures

Three different architectural approaches have been used to define multiuser systems. While this review is based on only the single microprocessor design, a brief look at all three is of historical value.

One group is the systems based on 16-

bit minicomputers. These designs are typified by large language, application and software bases, reliable software and upgrade paths. These systems require space and electricity, but can use fast bipolar devices.

Single microprocessor-based systems have 8/16, 16, and 16/32-bit microprocessors which are manufactured by Motorola, Intel, Zilog, and National Semiconductor. These systems utilize memory management, cache, communications and I/O support.

Multi-processor based systems utilize local area networks or disk servers to link workstations to users. All users have some degree of processing power and share disk storage and printers. According to Rohit Kumbhani, Manager of CPUs and Systems at Harris Corporation, "a multi-microprocessor system provides the simplest way of getting higher performance from the same pieces of hardware. The technology is at a stage where, in order to double or triple performance, you have to design a whole new technology."

Bus Structures

Future bus structures of microprocessor-based multiuser systems will incorporate several features to compete as lower cost-high performance solutions for multiple-user environments. These include high bandwidth and a high level of message passing support.

Standard bus structures have limitations in terms of the present VLSI technology. These buses were initially incorporated

into microprocessor systems for I/O expansion, greater memory addressing and enhanced multiprocessing support. However, the need in multiuser systems for higher speed execution and I/O have brought about several design changes.

One of these is the development of the add-on bus, which allows a single board computer (SBC) to communicate to a memory card without tying up the main bus. In some multiuser systems which include multiple SBCs, there may not be enough space on the CPU board for memory. A single system bus does not have the bandwidth to adequately handle execution, DMA and interprocessor communication. For memory intensive multiuser systems, designs call for an approach that can move the execution off the system bus, freeing it for DMA and interprocessor communication and a separate high bandwidth bus to support memory.

Multiuser, multiprocessing architectures are evolving into two areas. One is a loosely coupled architecture in which several microprocessors are linked together over a high speed bus, and each has its own memory. The other is a tightly coupled architecture where each of several microprocessors can access the common global memory.

An example of this tightly coupled scheme is the Poly 8/16 from Polymorphic Systems, which is a master-slave S-100 system where a single Z-80 master processor performs all system related I/O requests, communicating with 8086-based slave processor cards over the bus at 500 Kbytes/sec. Slave processors run Con-

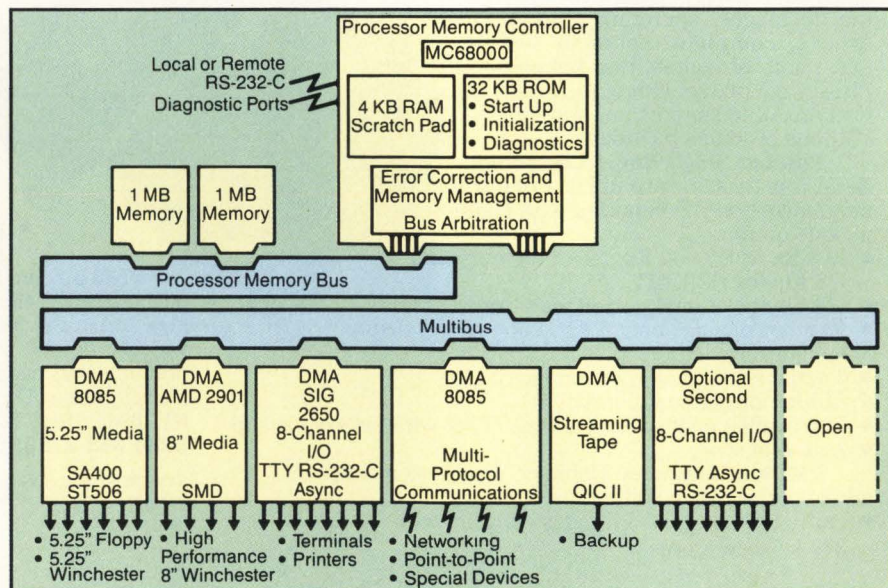
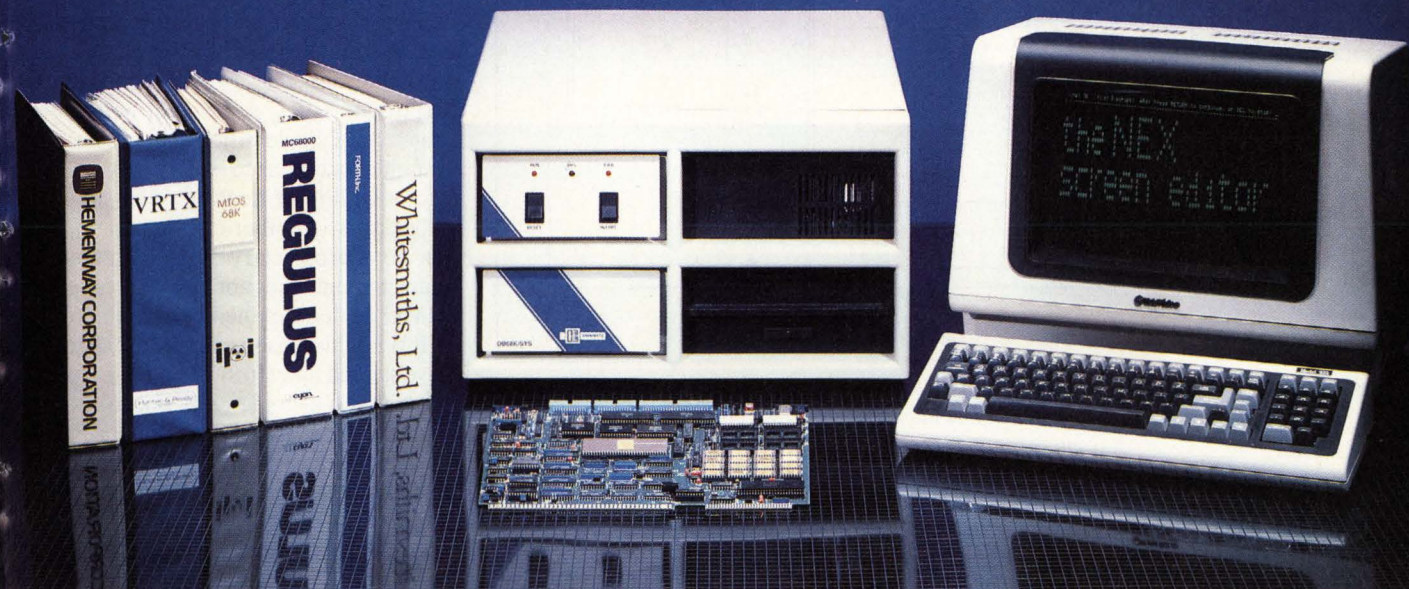


Figure 2: This diagram illustrates the architecture of the Tower 1632 from NCR Systems. The Multibus-compatible controllers used to control the communications links and peripherals are multiple device, industry standard modules.

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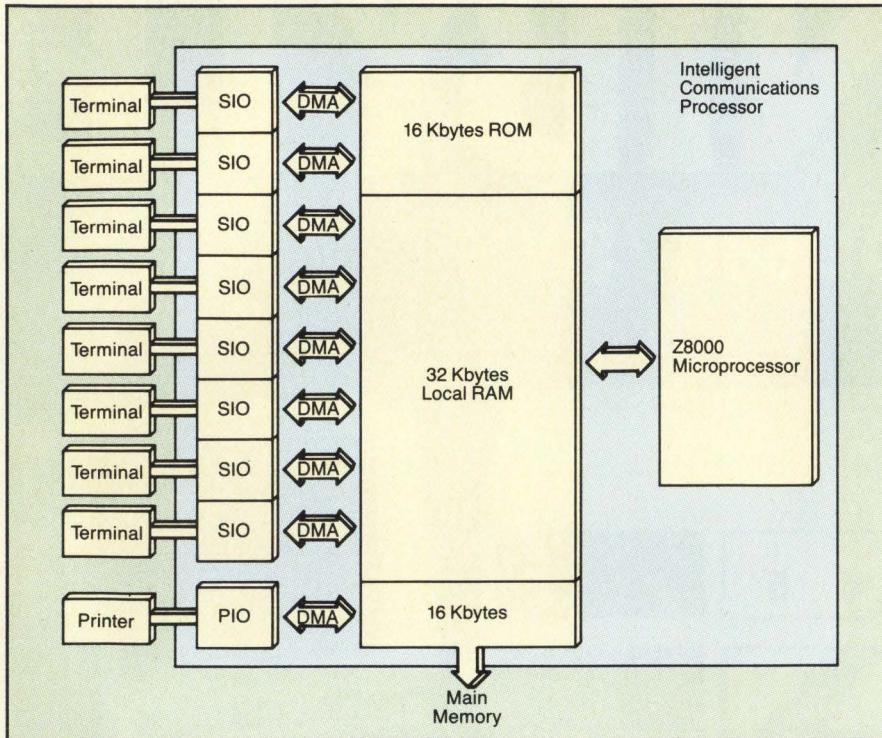


Figure 3: Block diagram of the intelligent communications processor from Plexus, a 16-bit microcomputer which is dedicated to memory management.

current CP/M86 which caches programs for each user at the user card. The master service processor contains 64 Kbytes RAM and caches disk requests using an LRU algorithm. This board contains an on-board DMA controller. Slave cards, based on Intel's 8086, include a 2-channel DMA controller, three 16-bit counter-timers, and an interrupt controller in addition to an 8 MHz 8086.

Boards in multiuser systems are now being tailored for particular purposes. This modular design approach breaks systems down into processing, mass storage, communications and graphics functions. In these particular modules, data movement is kept to a minimum, and real-time data is confined to a local environment.

CPUs For Different Designs

Microprocessor-based multiuser systems are based around several microprocessor chips such as those manufactured by Motorola, National Semiconductor, Intel and Zilog. Small system manufacturers have selected different devices according to their systems design needs. The most commonly asked question about the latest microprocessors relates to the software portability across a vendor's product line, an important consideration, since most small system designs depend heavily on the next generation

microprocessor as it becomes available from the IC houses.

The latest generation of microprocessors not only incorporates pipelined architectures, but has on-chip functions that make them almost indistinguishable from minicomputer architectures. These may include on-chip instruction and data caches, memory management, memory protection and virtual memory support.

The memory management capabilities of the Zilog Z8216 are useful in multiuser systems. This chip has a memory man-

agement unit, cache memory, four 16-bit counter-timers, a serial port and four channels of DMA control as well as a dynamic RAM refresh controller. The memory manager coordinates the 16 Mbyte address space of the processor by using two sets of 16-page descriptor registers. These registers contain 12 bits of address information and 4 bits of attribute information. For multiuser systems requiring a high degree of memory management, this processor is a logical choice.

Both the functionality that the IC vendor has placed on the single microprocessor and the peripheral devices that are available for that processor become important issues. A designer building a system for the scientific environment, for example, may wish to make extensive use of availability of floating point support processors. Another design may incorporate a proprietary form of memory management and not use the on-chip MMU device supplied by the vendor.

It is for this reason that some IC houses have steered away from the "greater functionality on a single chip" approach for high-end processors. They anticipate that certain designs would not benefit from this method. Speed and performance benefits not directly related to bringing co-processing functionality (such as MMU or FPU) on-chip relate more to caching instructions and/or data for speed, an approach that has been implemented at the board level for some time.

Charles River Data Systems, for example, developed one of the first designs to incorporate cache memory. The use of cache in this particular design dramatically increased system operating speed because it dedicated a high speed memory to the exclusive use of the local CPU.

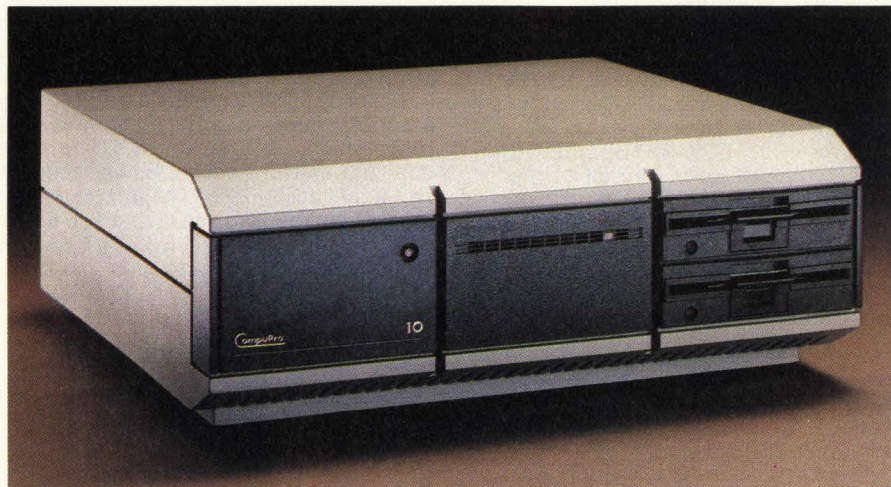


Figure 4: The CompuPro 10 is a multiprocessor, multiuser system whose architecture includes an 8088 CPU and four Z-80B processors.

Memory

The designer of a microprocessor-based system has two basic types of devices available to implement a random access read/write memory; static or dynamic RAM. Dynamic RAMs have four times the density of static RAMs. This means that four times as many bytes of memory can be placed on the same board space. Also, the cost of DRAMs is about one fourth that of SRAMs. On the other hand, SRAMs do not require the complex support functions of the DRAMs, such as address multiplexing and refreshing.

Multiuser systems use either of these memories, depending on their individual criteria of performance, power consumption, density and cost. When considering cost alone, cost of design time is directly proportional to design complexity. For example, SRAMs require less design-time than DRAMs because there is no refresh circuitry to consider. Conversely, the DRAM provides the lowest cost per bit because of its higher packing density.

I/O

The methods by which a multiuser system manufacturer implements I/O is an important consideration because additional I/O tasks significantly slow down the CPU by using large portions of the bus bandwidth otherwise available for CPU tasks. A traditional solution is to offload tasks for the system processor to a disk controller. In this arrangement, the processor specifies disk control and command parameters to the controller, which include the selection of recording density and specification of disk formatting information. The processor also sends commands to the controller. Most LSI controllers receive commands and parameters by means of the processor's I/O instructions.

In addition to the I/O interface, the controller provides data transfer between memory and the disk drive. This data transfer may be implemented by one of two methods: one, direct processor intervention in the transfer, and two, by interfacing disk controller to a Direct Memory Access (DMA) controller.

The I/O controller has traditionally been one of the main computer system's bottlenecks by failing to optimize system access time to data or the system's throughput rate. One solution to this has come from newer I/O bus structures with enhancements over older interfaces.

The disconnect/reconnect function of the SCSI bus allows a computer system to



Figure 5: A microprocessor-based multiuser system from Callan Data Systems that utilizes memory management, cache, communications, and I/O support.

access time, resulting in up to five times the system I/O performance.

Software

As mentioned earlier, software is an important issue with microprocessor-based multiuser system designs. According to Molecular Computer, who manufacture the Series 9 Multiuser Computer System, the broad acceptance of the IBM PC has curtailed a rapid shift from 8-bit CP/M based hardware and software to 16-bit applications.

Additional considerations include a particular system's ability to efficiently share data among users, provide economical expansion and maintain consistent performance as processor demands increase or as users are added to the system.

Because microcomputer operating systems are evolving to encompass developmental and target application purposes into one system, operating systems will

run concurrent I/O tasks by handling multiple seeks and reads/writes with the I/O bus disconnected, reconnecting only when a drive has data ready to be read or written. This function allows controllers to complete tasks in the most efficient order, regardless of the order they were received, thereby increasing the efficiency and speed of I/O transfers. This dramatically decreases multiple drive

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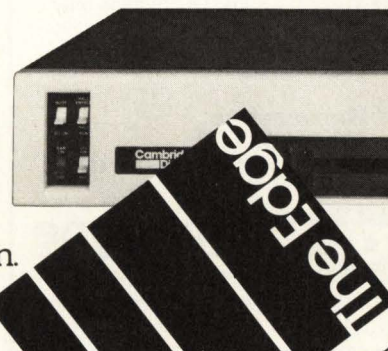
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change to accommodate modularity and ease of configurability as well as evolutionary growth and standardization in languages, networks, and operating systems themselves. The last two items are needed to provide protection of a firm's software investment, including the option to move toward silicon software.

According to Buddy Frank, Director of Public Relations at Sage, manufacturers of the Sage II and IV 68000-based systems, "more UNIX and UNIX-like operating systems will appear. Also a trend to exploring multiuser versions of other operating systems such as CP/M. There will be a trend toward increasing amounts of RAM (up to 3 Mbytes) and storage approaching the half gigabyte range to allow more effective use of satellite work stations on a central microcomputer with a large memory."

The choice of operating system and movement of microprocessor chips to integrated silicon technology will motivate the advance of micro-based multiuser systems. There is a trend toward multiple micro-based systems, which are attractive because of their ability to provide higher performance from inexpensive hardware. Multiple bus structures, the implementation of cache memory and the use of several I/O processors are becoming important considerations in multiuser designs. □

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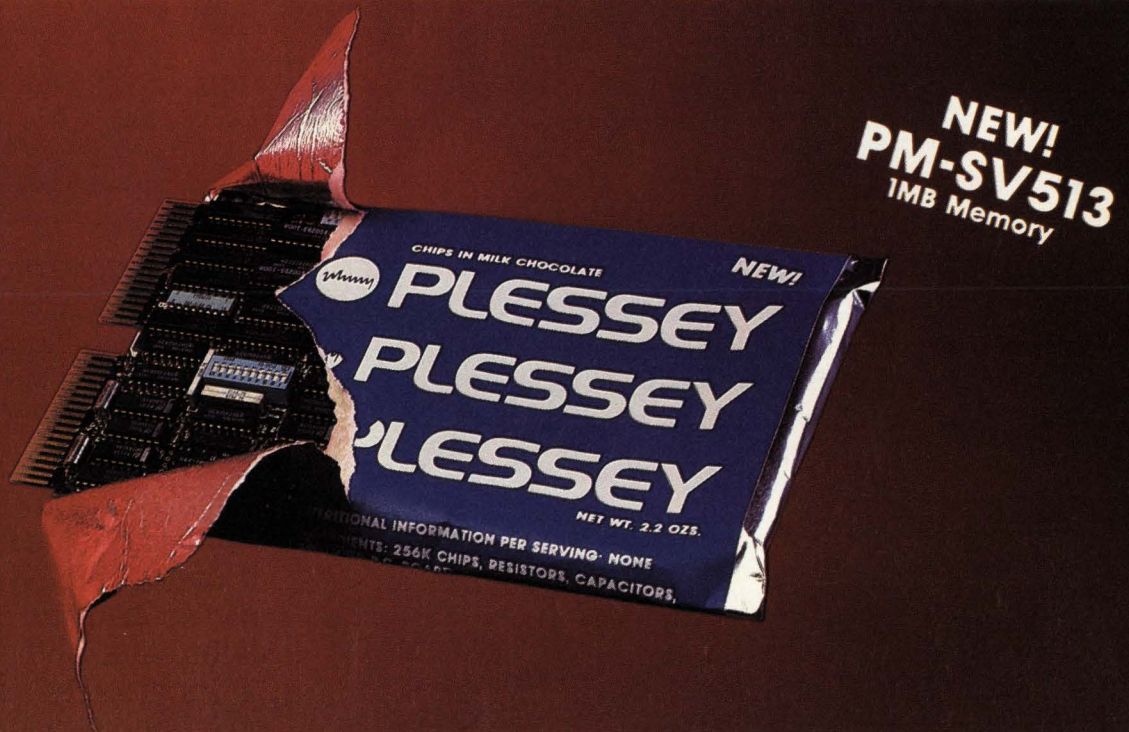
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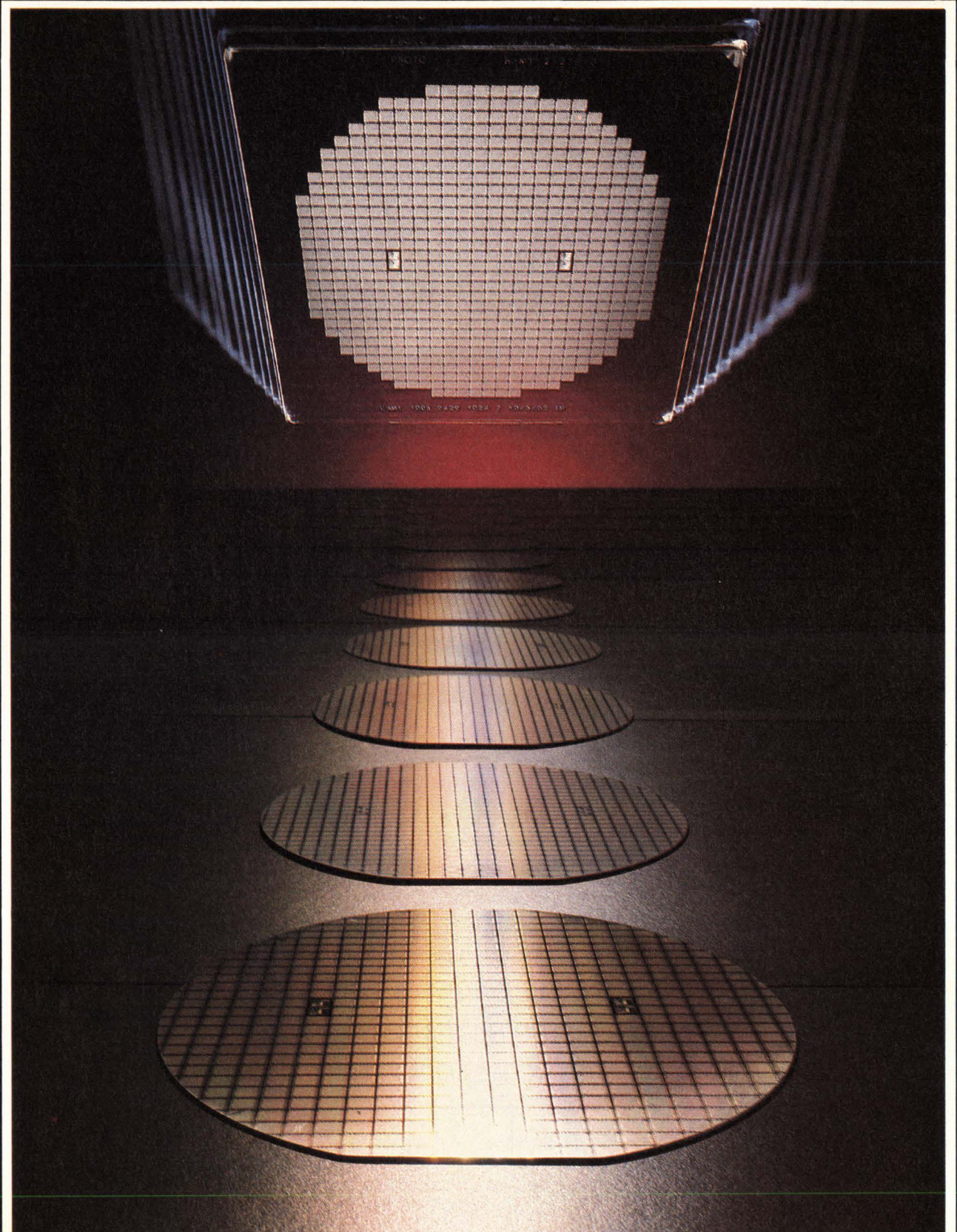
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Designer's Guide Series SEMI-CUSTOM ICs



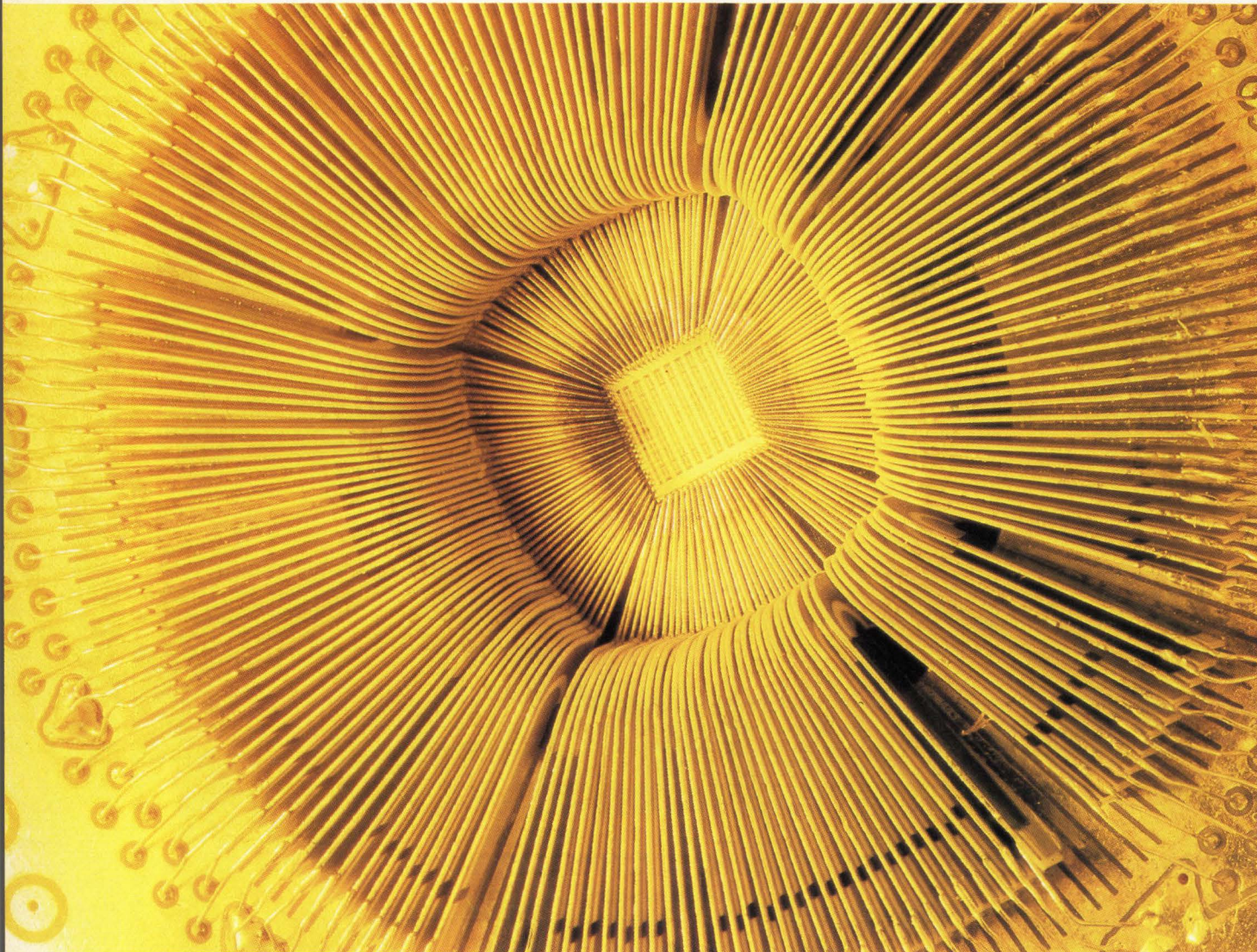


Photo courtesy Fairchild, Gate Array Division

Designer's Guide To Semi-Custom ICs

by Ron Collett,
Technical Editor

The economic advantages of using semi-custom ICs will eventually force most equipment manufacturers presently designing with off-the-shelf parts to switch to this newer technology. Semi-custom ICs lower a system's overall cost since they drastically reduce the number of chips, PC boards, wires, connectors and overall assembly costs associated with standard IC (i.e. using standard

The number of IC vendors in this industry continues to grow, and choosing the right one is essential to the success of the design.

Custom".)

In most cases, entire systems cannot be implemented using semi-custom parts, but certainly many of the SSI/MSI/LSI

TTL parts) designs. In turn, systems that use this VLSI technology also have increased performance, higher reliability and lower power dissipation. Proprietary design protection is an added benefit of this fast growing methodology. (For definition of semi-custom, see box entitled "Defining Semi-

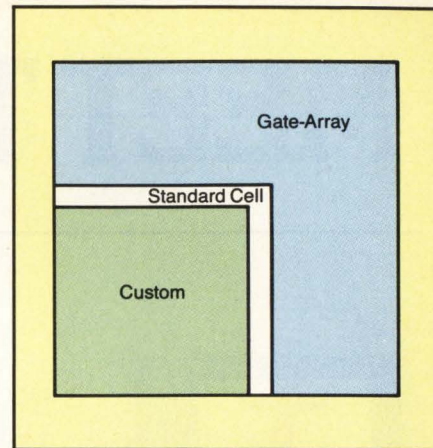
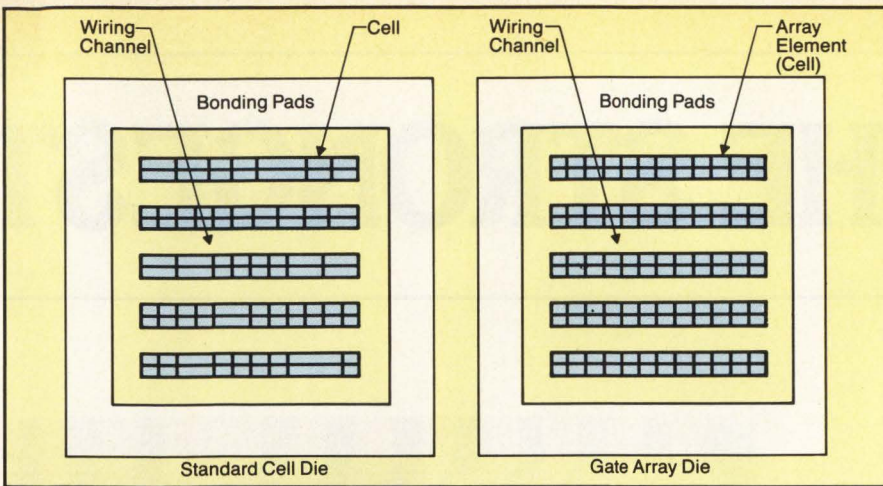


Figure 1: Standard cells have fixed heights and variable widths whereas both dimensions are fixed on gate arrays. When defining a logic function on a gate array, a complete cell must be accessed regardless of whether all the transistors within the cell are used. Standard cell designs require customization of all masks which results in 100% transistor utilization.

Figure 2: Shown is a relative comparison of die size between full custom and semi-custom ICs.

devices now available can be integrated. Until recently, semi-custom design has meant the integration of random logic ("glue chips"). However, large macro cells such as ALUs, multipliers and memory can reside on a gate array or a standard cell chip. Larger macros such as microprocessor cores primarily exist in standard cell libraries, and most likely will not immediately find their way onto gate arrays.

Manufacturers are making the transition from standard ICs to semi-custom devices both for replacing the SSI/MSI chips of an existing product, and for designing a new product. Semi-custom VLSI is usually driven by the demand for decreased size, cost reduction and improved performance. Shortages and long delivery times (sometimes from 26 to 40 weeks) for standard TTL parts also contributes to the increased demand for semi-custom chips. In contrast, typical gate array turn around times range from eight to 16 weeks while standard cell devices usually take 20 to 30 weeks.

Whether upgrading an existing product or initiating a new design, choosing a vendor is the most important step in making the transition from standard ICs to semi-custom. At last count, there were between 70 and 100 semi-custom IC vendors. Picking the right one can mean the difference between faulty parts delivered late and working parts delivered on time. Since most products have a market window, late parts can mean a delayed product entry, which obviously causes profit losses.

Unlike systems built using off-the-shelf chips, semi-custom designs require close interaction between the product manufacturer and the IC vendor. A semi-custom project leaves the system architect with much less control over the design's implementation; in most cases, from 50 to 80% of the design cycle will ride in the hands of the semi-custom IC supplier. The exact percentage varies from one design case to another as well as between different vendors.

Standard Cell Or Gate Array

Until recently, most semi-custom IC vendors supplied either gate arrays or standard cells, but few offered both. This has begun to change, and an increasing number of gate array vendors now provide standard cells as well. Of the multitude that presently offer just gate arrays, many plan to introduce standard cell libraries in the future. Working with a vendor that has both (or plans to offer both) gives the system architect greater design

implementation flexibility. For instance, present designs may require a gate array, but future projects could demand a standard cell approach. Since each vendor has a particular design methodology, switching from one to another may require learning a completely different design approach.

In general, high I/O requirements, high gate count and large volume quantities dictate the use of a standard cell. Unfortunately, it is impossible to choose the best solution without weighing many technical and economic considerations.

Standard cell designs cost more to develop initially, and closely resemble a full custom chip since each mask is customized. Standard cells have fixed heights but can have any variation in length. Gate arrays, on the other hand, have fixed rows of transistors in which all the cells are the same dimension (Figure 1). Consequently, defining a logic function from these transistors requires that the entire cell be accessed, regardless of whether all of the transistors will be used.

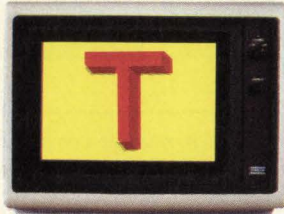
Standard cell designs use all of the transistors on the chip. In most instances, this more efficient use of the silicon leads to a smaller and consequently cheaper die when compared to a gate array (Figure 2). However, since each standard cell design has its own unique set of masks (usually eight to 12), the development cycle costs more.

On the other hand, all of the masks of a gate array are fixed except the interconnect levels and the level defining the vias (connections between levels). With approximately 85% of the array predefined, only the last 15% need be customized, for generally less expensive development cycles. Lower costs and shorter development cycles make gate arrays a good risk management strategy. For example, if a product has yet to be introduced to the market, the system architect may then further integrate the system using standard cells. This risk management plan minimizes financial losses if the product is not as successful as originally anticipated. If the product does turn out to be a market success, the initial gate array expenditure will be absorbed over the sheer volume of the product.

Choosing A Vendor

With such a large selection of semi-custom vendors, the choice can be overwhelming. Most vendors can deliver good parts on time, but the potential customer must cull those few vendors that cannot. Assessing the technical requirements of the circuit and

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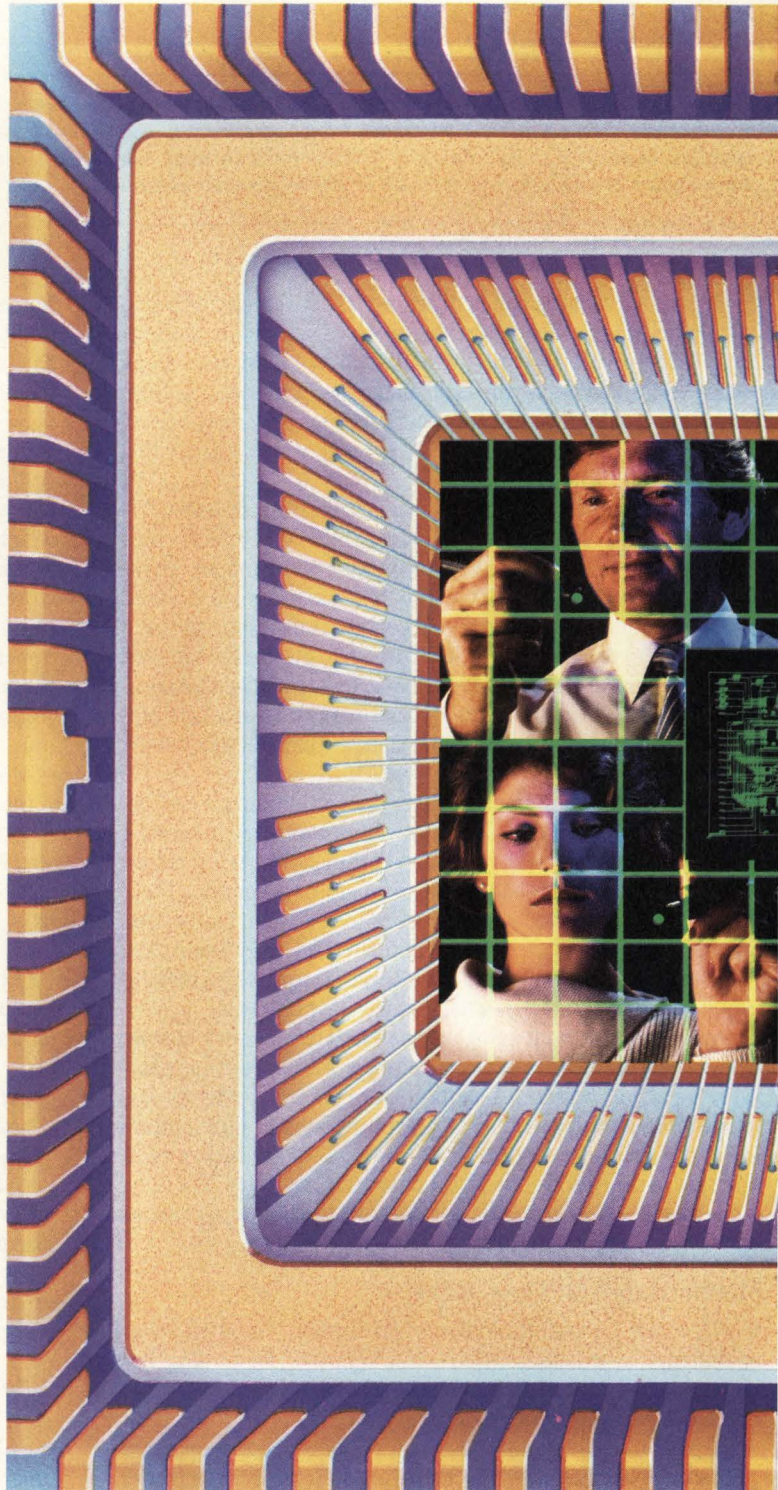
TECHNOLOGY	GATE LENGTH	PROP DELAY TIME*	GATE COUNT
STD CMOS	3.6 μ	7.0 ns	700-3900
H CMOS	2.8 μ	5.0 ns	440-3900
VH CMOS	2.3 μ	2.5 ns	2600-8000

*2-Input NAND Gate, F/O = 2

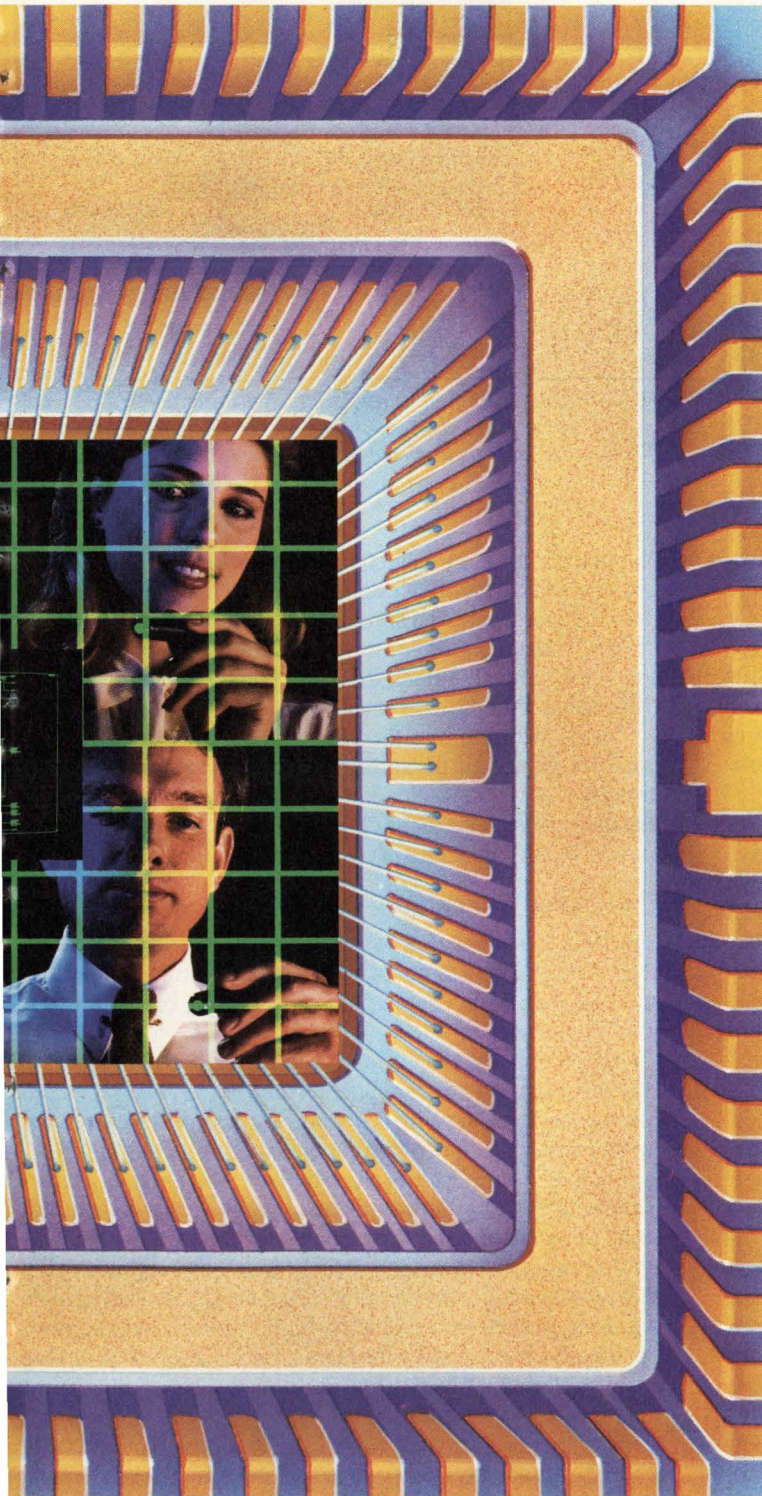
BIPOLAR

TECHNOLOGY	PROP DELAY TIME*	GATE COUNT	POWER DISSIPATION PER GATE
LSTTL	1.8 ns	500	2.3 mW
LSTTL	1.9 ns	240-1100	0.8 mW
LSTTL	0.95 ns	2000	0.65 mW

*3-Input NAND Gate, F/O = 1



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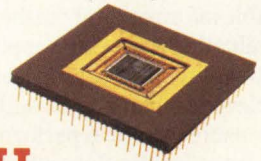
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performing an economic analysis similar to the risk management strategy is the first step to choosing the best approach to integration.

Presently, most vendors do not offer both gate arrays and standard cells, so some can be immediately eliminated if one approach is best for the particular application. When implementing high speed (greater than 35 MHz) complex designs (over 4000 gates), the selection of vendors is reduced because many do not have the advanced process technology necessary to fabricate these chips.

Speeds up to 25 MHz are becoming widely available in CMOS, and higher rates using this revitalized technology are possible, but only from a limited number of vendors. In most cases, a bipolar technology such as TTL or ECL will be a better choice for higher performance applications. As fabrication process improves and sub 1-micron (effective) geometries are reached, CMOS will battle bipolar performance. Currently, 2-micron (drawn) gate widths with double layer interconnect metalization represent the "state of the art" in CMOS gate arrays. With double layer metal, the interconnections between macrocells (i.e. gates, flip-flops, etc.) are made using two layers of metal separated by a layer of oxide. With several layers available for metal interconnections, more transistors can be integrated onto the die.

When speaking of gate widths, it is important to note whether a vendor refers to this dimension as "drawn" or "effective." The drawn value represents the gate size as sketched on the mask; this is larger than the effective value, which represents the actual dimension on the die. The drawn value is larger than the effective value, so when comparing technologies among vendors be sure that both dimensions are given. Since smaller transistor gate widths mean higher performance, the vendor's fabrication process capabilities can be partially evaluated by this dimension.

Inquiring about a vendor's yield percentage is another way to evaluate the fabrication capabilities, although this is often proprietary information. This figure expresses the number of "good" die versus faulty die on a wafer. Most of the time, vendors with high yields will not hesitate to reveal these figures.

Whether or not a semi-custom vendor fabricates their own wafers is another consideration. In the case of gate arrays, most vendors perform the metalization, but not all do the actual wafer fabrication. Those that fabricate their own wafers are not necessarily better than those that buy the wafers from outside sources. The latter vendors are dependent upon the wafer suppliers for quality and quantity, whereas those with their own wafer fabrication line are in complete control of the manufacturing process. For long term, large volume commitments, most industry experts consider it mandatory to have a wafer fab line.

After weeding out those vendors on the basis of technological capabilities, the next stage involves verifying the vendor's credentials. Speaking with previous customers can provide invaluable information about the vendor's merits or shortcomings.

Evaluating a test chip supplied from the vendor is one of the best ways to check the propagation delays, set-up and hold times and electrical parameters outlined in the timing specification. To measure electrical performance, a test chip need only have a few gates and flip-flops which are chained together. Some vendors will offer this outright while others may comply upon request.

Since the delay of a CMOS gate is directly dependent on its

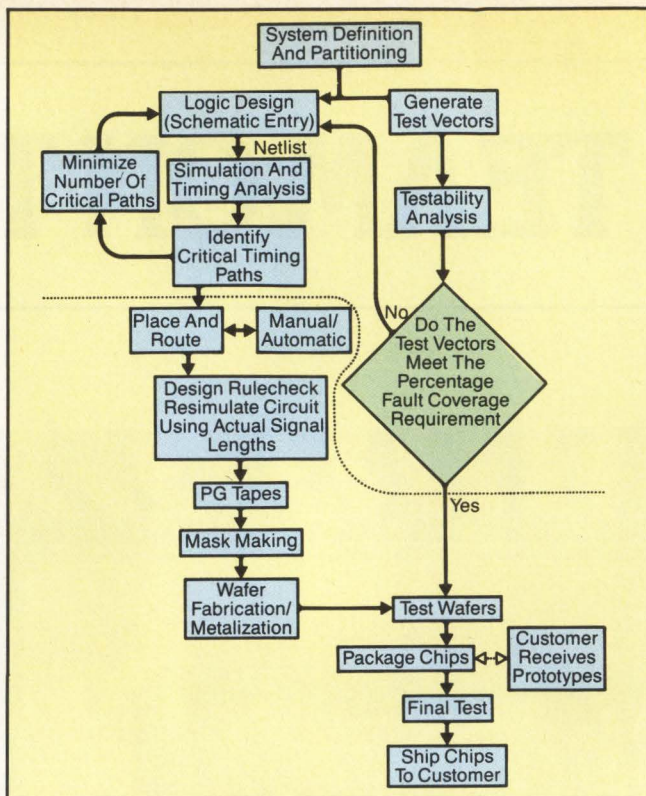


Figure 3: This flowchart illustrates the typical design cycle for a semi-custom chip. Most vendors encourage customers to perform many of the front-end tasks including test vector generation.

output load, make sure that the size of the load (i.e. number of gates) is indicated when evaluating gate delay specifications from the data sheet. And similar to working with standard ICs, use the "maximum" or "minimum" values for a given parameter—not "typical" values. In short, verify that the vendor's chips agree with the data sheet.

Finally, insuring that the chip will function as promised should be outlined in the agreement between the vendor and the customer. A written statement from the vendor guaranteeing that the performance of the chip will match the computer simulation should be mandatory when negotiating an agreement.

The Analog Dilemma

Interfacing to the analog world is one of the most important aspects of systems design. In addition, integrating both analog and digital on a single chip poses a stumbling block for most semi-custom vendors.

High performance analog or mixed analog/digital designs are available from just a few suppliers. However, most vendors can combine digital logic with lower performance analog circuitry such as simple op-amps and comparators. As one would expect, purely linear semi-custom chips deliver much higher performance than hybrids but are not up to the speed and resolution found in many dedicated standard analog ICs. Variations in voltage requirements between the analog and digital sections of the chip present a major problem for mixed arrays because smaller transistor geometries do not allow higher voltages. In addition, electrically characterizing the huge number of different analog circuits in terms of function and performance has stymied most vendors.

For higher performance mixed applications, standard cells offer a better solution than gate arrays since all mask layers are accessible. Comparing the analog functional libraries among

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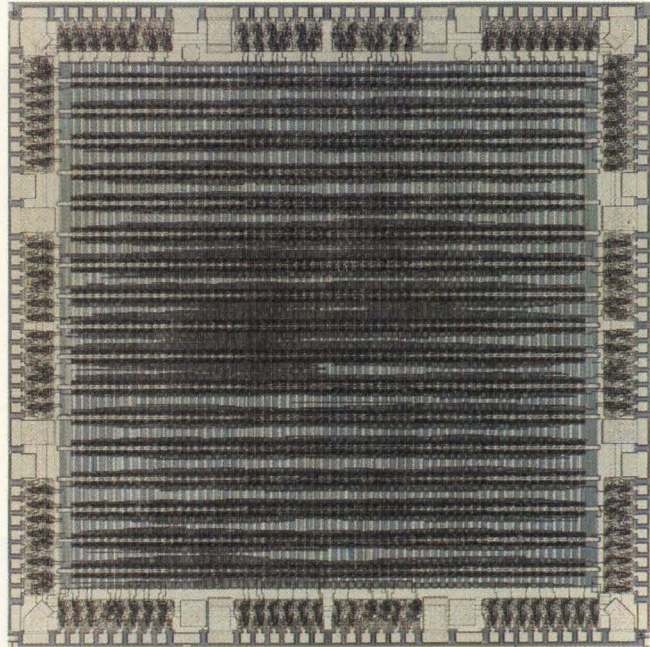
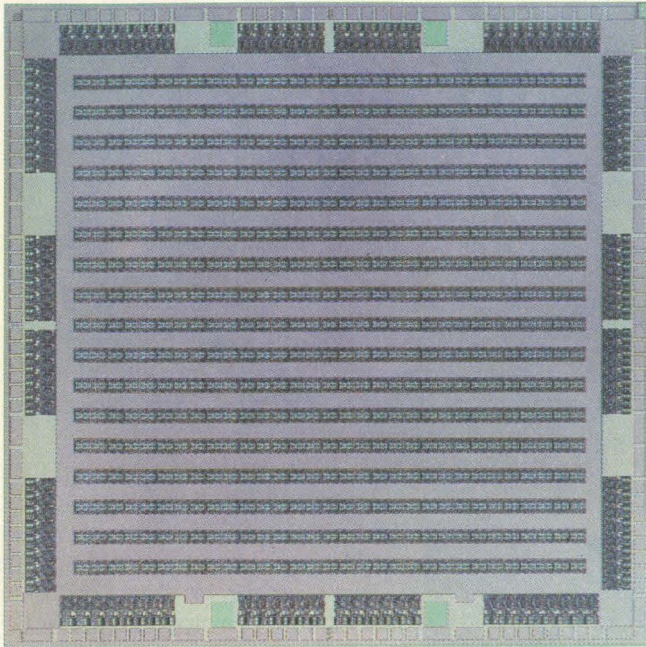


Figure 4: Fujitsu Microelectronics' B2000 Bipolar, 2000 gate array, before and after metalization.

vendors is one of the most important criteria for mixed or high performance circuits supporting present and future designs.

The lack of analog computer simulation tools, however, makes semi-custom linear design much different from its digital counterpart. Small sections of analog circuitry can be simulated using a SPICE type simulator, but for the most part, the computational demands require excessive computer horsepower. For this reason, breadboarding remains the primary method to verify large linear designs. This leads to longer design cycles (20 to 30 weeks), higher costs and an increased level of design complexity.

With analog designs, technical problems are more likely to be encountered, so the vendor should be willing to devote engineering expertise to your design. It is also vital that you completely understand all aspects of your design. For example, investigate the various phenomena that occur when powering up the circuits and evaluate particular nodes for critical voltage levels and timing requirements. It is impossible to address all the possibilities, but with the vendor's help, most pitfalls can be avoided.

CAD Tools

Workstations most definitely have a place in the design cycle of semi-custom ICs. However, a hasty decision to purchase one can prove uneconomical. Before investing \$40,000 to \$120,000 in a workstation, evaluate the extent to which they can facilitate your semi-custom design. This can only be accomplished by getting some experience in semi-custom design.

In theory, workstations are designed to increase an engineer's efficiency and productivity. Purchasing one single-user workstation for several engineers can be counterproductive. The ideal situation would provide each system architect with a workstation connected to a large host. Schematic capture, net list generation and smaller logic simulations would be done locally at the workstation with larger simulations running on the host.

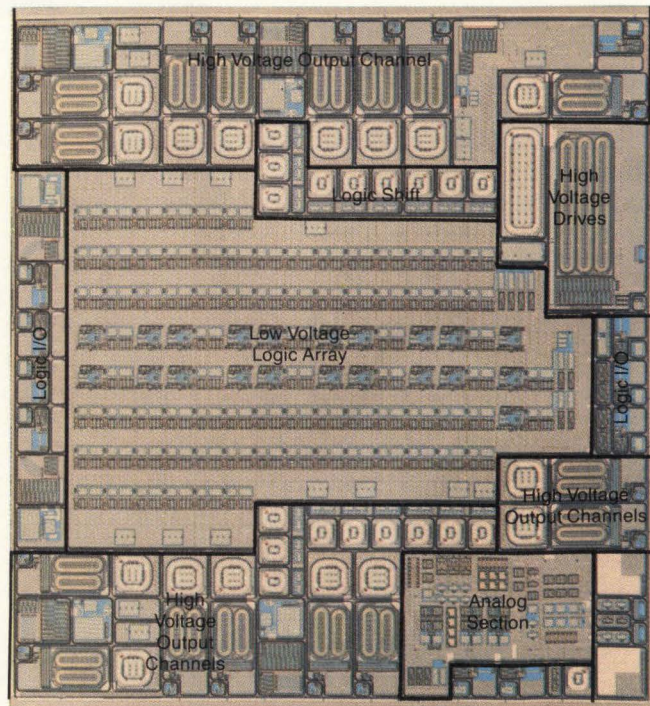


Figure 5: The Telmos TML5002 high voltage gate array provides analog and digital capabilities. The array has 16 200V/10mA push-pull output stages which operate under the control of 300 gates of uncommitted CMOS logic.

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ISO-2B	540	48	58
ISO-2C	720	54	64
ISO-2D	960	62	72
ISO-2E	1200	68	78
ISO-2F	1500	76	86
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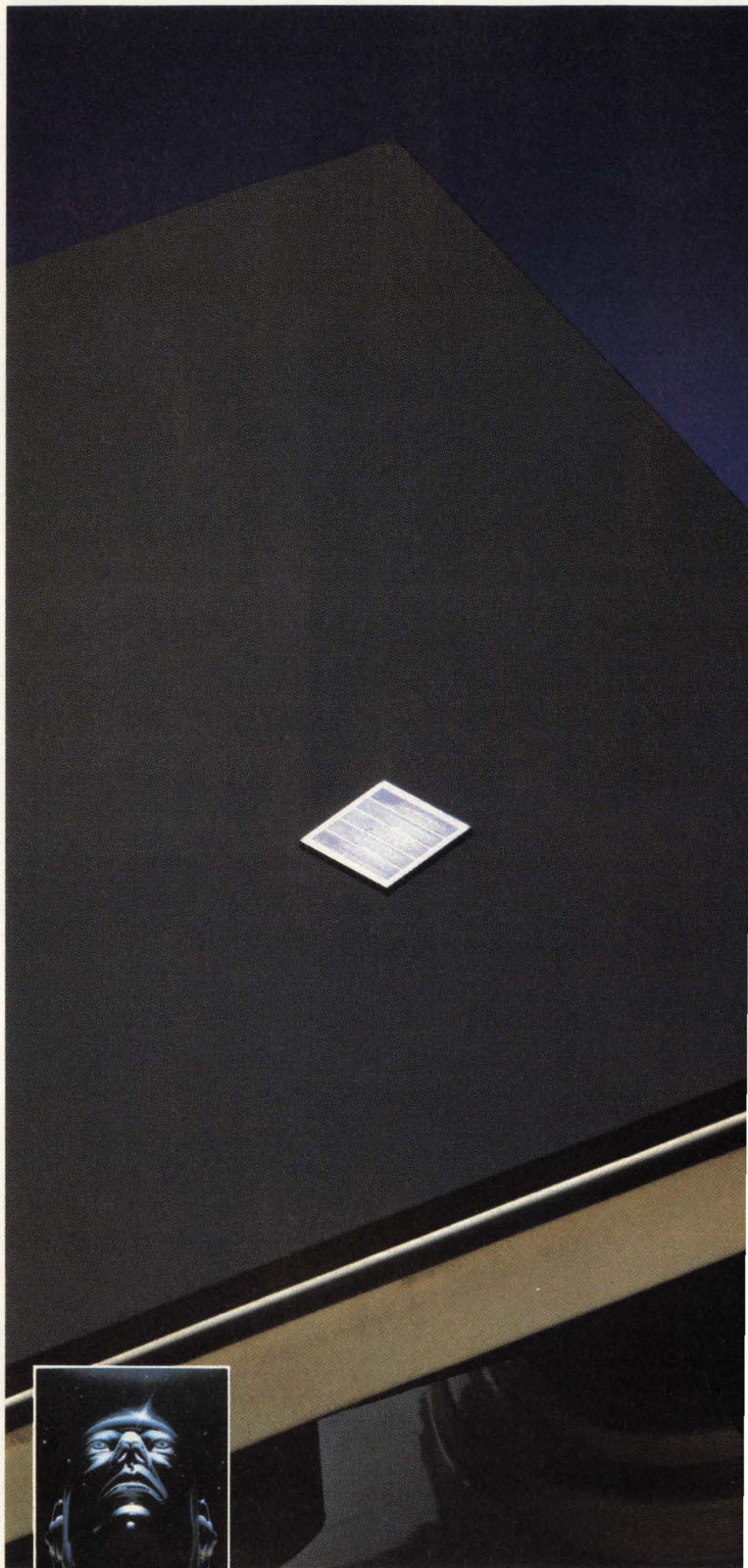
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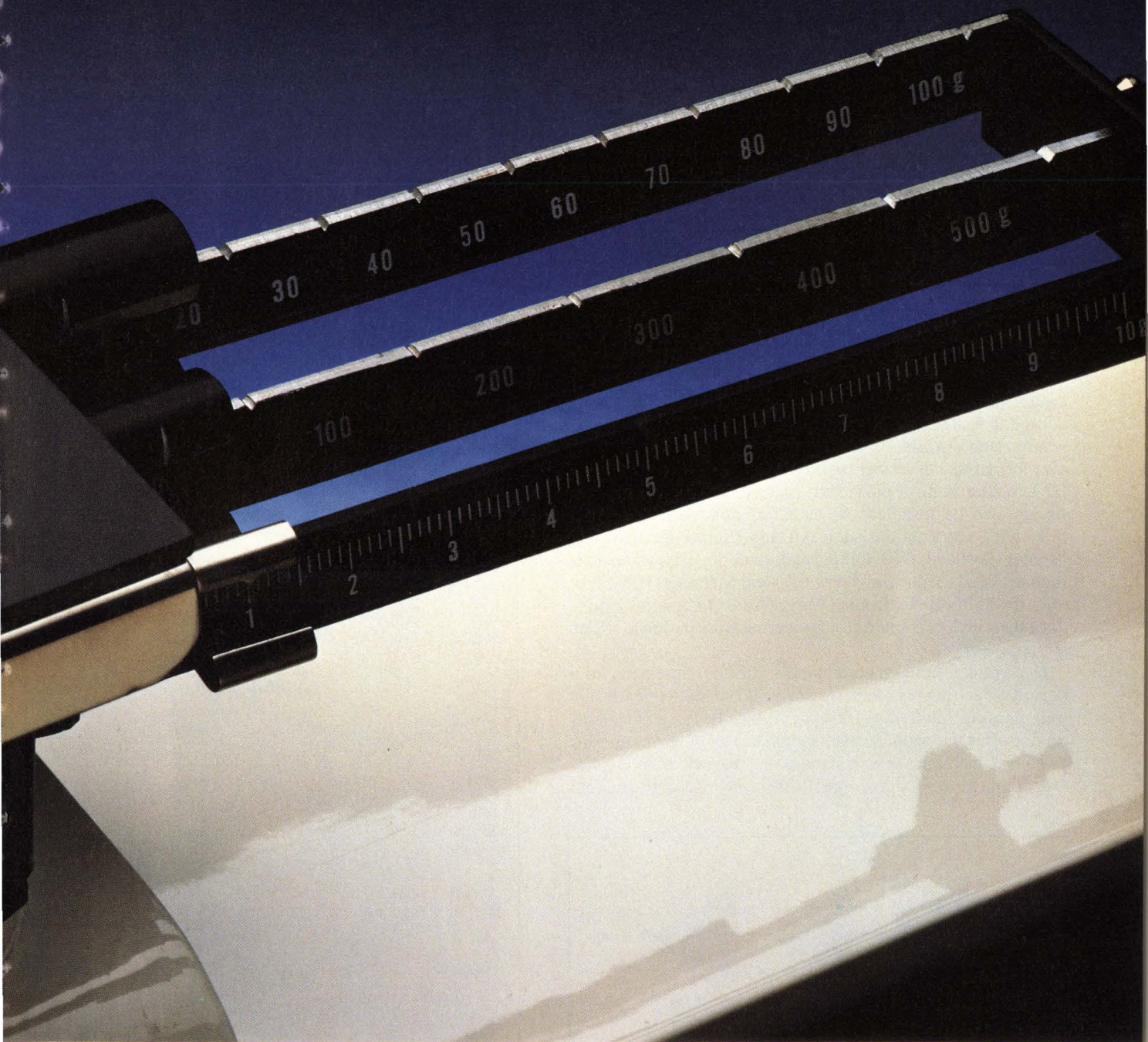
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Defining Semi-Custom

Digital Design includes both gate array and standard cell ICs under the definition of semi-custom. This view is based on the similarities between gate arrays and standard cells as well as the differences in design procedures between semi-custom and full custom chips. Undoubtedly, semi-custom and full custom methodologies continue to get closer to each other, and the differences become subtle. However, until they are in fact the same, we must differentiate between the two. When full custom designs are automatic and do not require the IC designer to define the transistors, perform the layout and make the interconnections, then semi-custom and full custom will merge into a single discipline.

System architects designing semi-custom chips use predefined macro functions from a library. *Digital Design* views full custom designs as those that do not allow an engineer to call upon predefined libraries of functions. In addition, with semi-custom methodologies, most of these functional macrocells are automatically laid out and interconnected by computer. Conversely, full custom designs require that the IC designer draw and interconnect each transistor on the chip.

Most experts contend that gate arrays belong in the semi-custom category. Whether standard cells belong in this category, however, tends to create some argument. Since each of the masks are

customized for standard cell and full custom methodologies, some argue that these should be put in the same category.

Though there is no doubt that all of the masks are customized, this definition does little to serve those performing the design. Methodologies that allow the system architect to use automatic placement and routing of predefined cells should be separate from those that use predominantly manual techniques. If one were to base the definition of application-specific integrated circuits (ASIC) on the customization of the masks, then there would be no difference between designs that are handcrafted and those that are semi-automated.

This is the most costly solution and is only recommended when many semi-custom designs will be undertaken.

A common misconception among newcomers to semi-custom design involves netlist (i.e. the description of the circuit components and the interconnects) compatibility between IC vendors and workstation vendors. Each IC vendor has a particular format that describes their macro library, so if you own a CAD/CAE system or plan to buy one, be sure that the vendor's library can be installed. Most IC vendors support several third party workstations such as Daisy (Sunnyvale, CA) and Mentor (Portland, OR). Other vendor-supported workstations include Valid (Mountain View, CA) and Metheus (Hillsboro, OR). In addition, Tektronix (Wilsonville, OR) plans to introduce their own version of an engineering workstation to stiffen the competition.

Designing a semi-custom chip for the first time calls for a period of "getting your feet wet." Most IC vendors offer design training and CAD/CAE workshops. Typically, IC vendors' tools do not offer the sophisticated schematic capture or superior graphics capabilities of workstations, but they will allow the system architect to get the design off the drawing board and into

silicon. It is often forgotten that CAD/CAE should allow the system architect to concentrate on the circuit rather than the tools.

Slight differences in design procedures exist between using "off-the-shelf" parts and semi-custom libraries. Most system architects presently tailor standard ICs to meet their needs. For example, designing a 7-bit counter would require using an 8-bit counter and rendering the eighth bit (flip-flop) inactive. Semi-

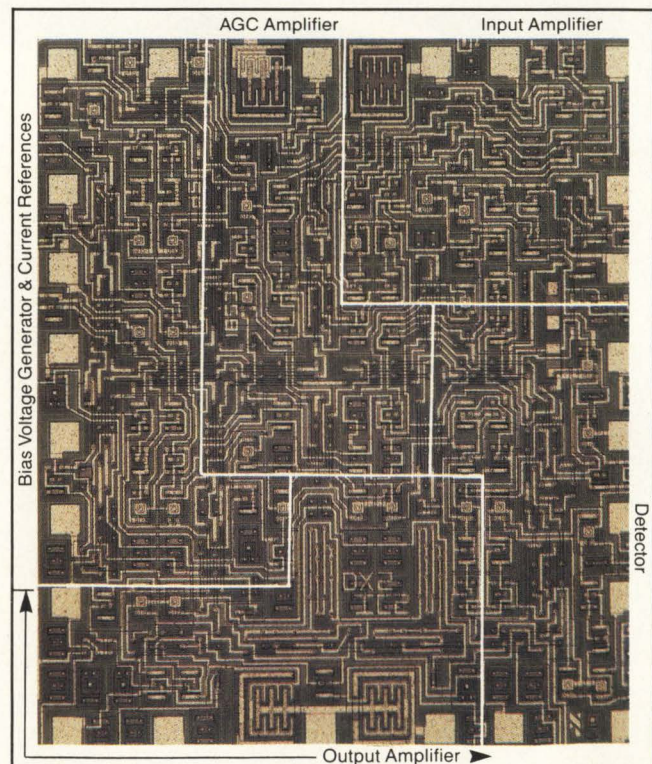
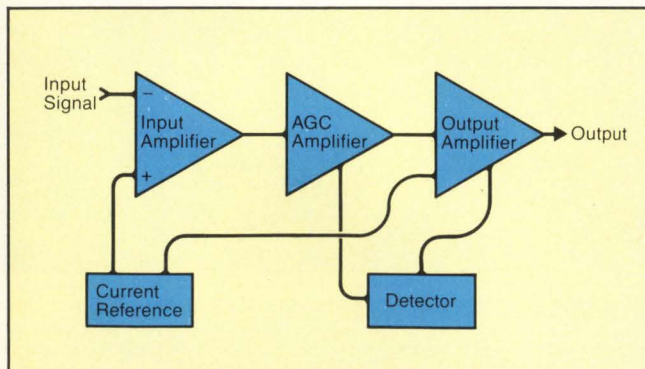


Figure 6: A completely analog array from EXAR Integrated Systems with the corresponding block diagram.

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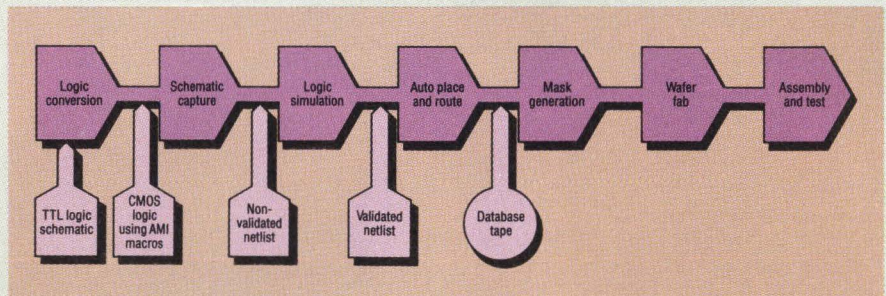
Get out of the gate faster with AMI gate arrays.

AMI gate arrays—in 5-micron single-metal, 3-micron single- and double-metal, and 2-micron* double-metal CMOS—are predesigned, prefabricated circuits. They're processed through all but the final "mask" layers which give the circuit its personality. All that needs to be done is design the personalized mask layers to your specifications. Then your circuit is ready for manufacture and delivery—in weeks, not months.

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Finally, you can simply provide us with your database tape. The adjacent chart illustrates all your options.

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We can ship your AMI gate arrays as quickly as 4 to 6 weeks from pattern verification. Compare that to 24 weeks and more for TTL circuits.

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Netlist

Netlist



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Figure 7: The SCALDstar integrated VLSI logic and layout design system for custom and semi-custom design.

custom designs are built on a more primitive level, and in this case would require the architect to build the 7-bit counter using seven flip-flops. Some vendors ease the task by offering libraries with many different variations of the same function. For instance, a vendor may have a 4-bit, 6-bit and 8-bit counter in the library in addition to the basic flip-flops.

Since minimizing the number of gates in a system is one of the reasons for switching to semi-custom, system architects must understand how to design at the gate and flip-flop levels. Most engineers are accustomed to designing at higher levels, so portions of the vendors' training courses are often devoted to reacquainting the individual to designing logic with primitives.

Design centers are a popular alternative for designers inexperienced with semi-custom. These facilities, usually located in major cities, are an extension of the vendor's plant, with CAD tools, access to the vendor's host computer, training courses and general engineering resources. After completing the design training, the system architect can work at the circuit design using the tools at the design center. Leasing a line to the vendor's host computer is another alternative. This is often preferred for experienced semi-custom designers since it allows the customer to do the design work at his own facilities.

High Performance Gate Array In SMS Computer System

A high performance CMOS gate array plays a key role in providing the unique levels of mass storage performance and overall system integration provided by the Scientific Micro Systems' SMS 1000 Model 40 computer system. The array integrates a large portion of the disk controller data path, allowing the system to support a wide variety of disk drives in a broad range of data rates. It also allows a complete set of system support functions to be integrated with the storage controller on a single plug-in board. This integration reduces cost, space and power to levels not available using other techniques.

Previous SMS designs relied on PALs and PROMs as the only mechanisms for customizing circuitry. These programmable components provided a reduction in package count, board space, and power, compared to standard logic while maintaining in-house design control and multiple vendor sources. The Model 40 designers realized, however, that they would be unable to provide the data rate capability and system compaction they wanted without progressing to higher integration levels. A survey was undertaken to find a quality vendor and then to find a component in their

line which provided a good solution to the integration problem. To minimize risk, the array had to be in production already. To encourage regular communication, the vendor needed to be close geographically. They also needed to provide good CAD tools and training since the Model 40 array required high speed and complexity despite the fact that this was SMS' first custom design. The survey narrowed the choice of vendors and also proved that, at the moderate volume levels anticipated, gate array technology was the most cost effective solution when compared with either standard cell or fully custom alternatives.

In parallel with the vendor survey, SMS engineers determined the portion of the controller circuitry to integrate. An iterative design process considered potential array sizes against the specific functions to be included while considering the limitations imposed by cost and the number of package I/O pins available. The array finally chosen has 3200 gates. In the SMS version, the functions it provides would take over 30 SSI/MSI ICs to implement, ignoring the array's higher data rate and flexible interface capabilities.

Once the vendor and array were chosen and the functional design completed, about five months were spent on the internal design of the SMS array version. This effort cost substantially more in both time and expense for computer simulation than had been originally anticipated by either SMS or the vendor.

The inaccurate estimates seem to be primarily a result of the heavy speed and functional requirements placed on the circuit. These approached the basic limitations of the array, causing greatly increased design and simulation efforts to optimize the internal circuit to improve performance. Less aggressive performance requirements would have reduced the cost significantly. In addition, continuous enhancement by the vendor's training and CAD tools would make this development less costly today.

When the design was complete, prototype arrays were produced in approximately 10 weeks. This array, and the Model 40 is now beginning full production.

—Daniel A. Dawson, Director of Product Planning, Scientific Micro Systems, Mountain View, CA

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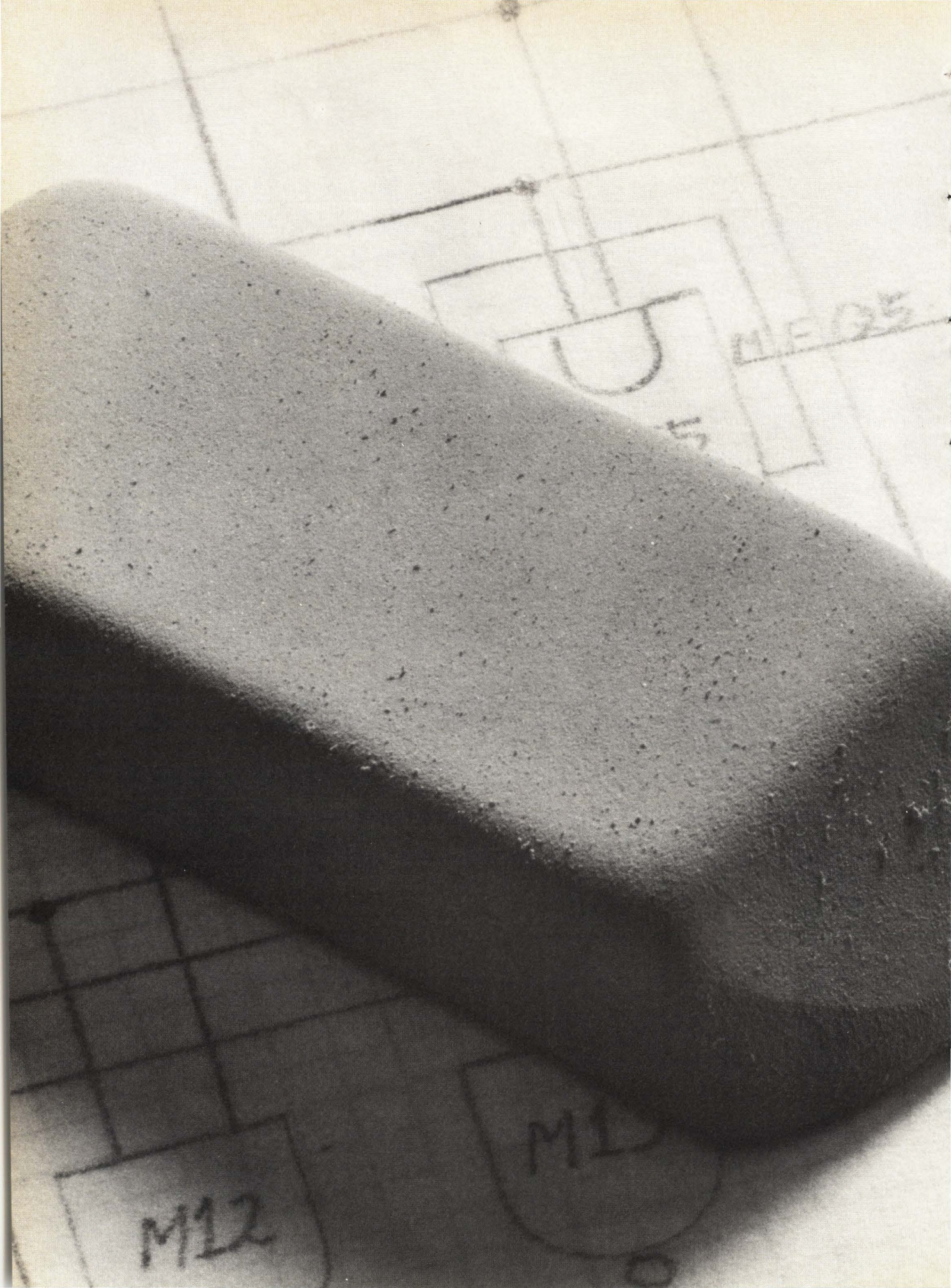
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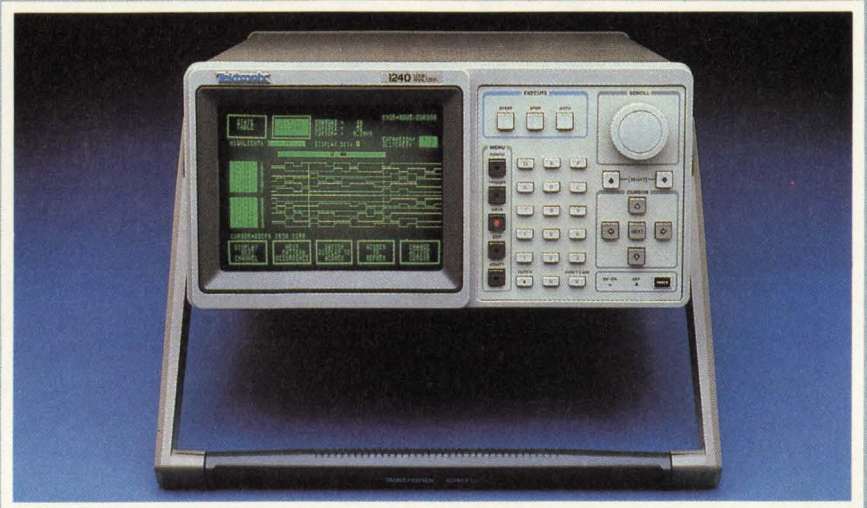
Designing A Logic Analyzer With A Gate Array

The model 1240 logic analyzer from Tektronix was designed for up to 72 channels running as fast as 50 MHz. The unit has 14 levels of triggering with counters, timers duration filters and glitch detection down to 5 nsec. These capabilities, coupled with the physical size constraint of the box, forced integration of many of SSI/MSI parts. Using a gate array, all of the necessary circuitry fit on the 18 channel acquisition card without sacrificing any features.

Hybrids were too expensive and neither the time nor resources were available to undertake a full custom design. To achieve very high performance, a bipolar gate array was chosen, since there were no standard cell bipolar libraries available. Using a 600 gate equivalent array, the space required was reduced by 75%.

The selection of the particular gate array was based on several factors. The cost of the actual part when in production as well as the development costs were quite reasonable. In addition, the CAD tools were readily available and met the needs of the design team.

Design, development and testing took about five months. One of the reasons for the lengthy cycle was that several redesign iterations were needed to utilize 100% of the cells on the array. It also re-



The Tektronix 1240 logic analyzer.

quired ten different placement schemes and manual graphic editing to successfully route the design. However, if 100% cell utilization had not been required, it would not have been necessary to perform so many iterations.

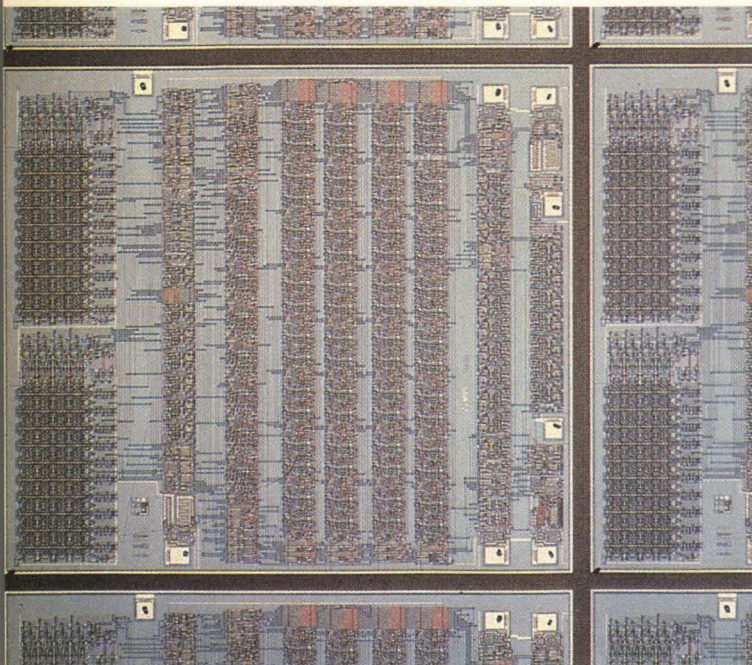
One of the areas where semi-custom design has improved is the CAD/CAE. At the time of this design, there were no schematic capture tools, and the auto-

place and route programs were not as good as they are now.

Lack of AC testing on the part of the vendor was one of the areas that needed improvement. We recommend investigating how well a vendor tests the chips when they come off the fab line.

—Ron Jackson, Tektronix Design Automation Division

Write 301

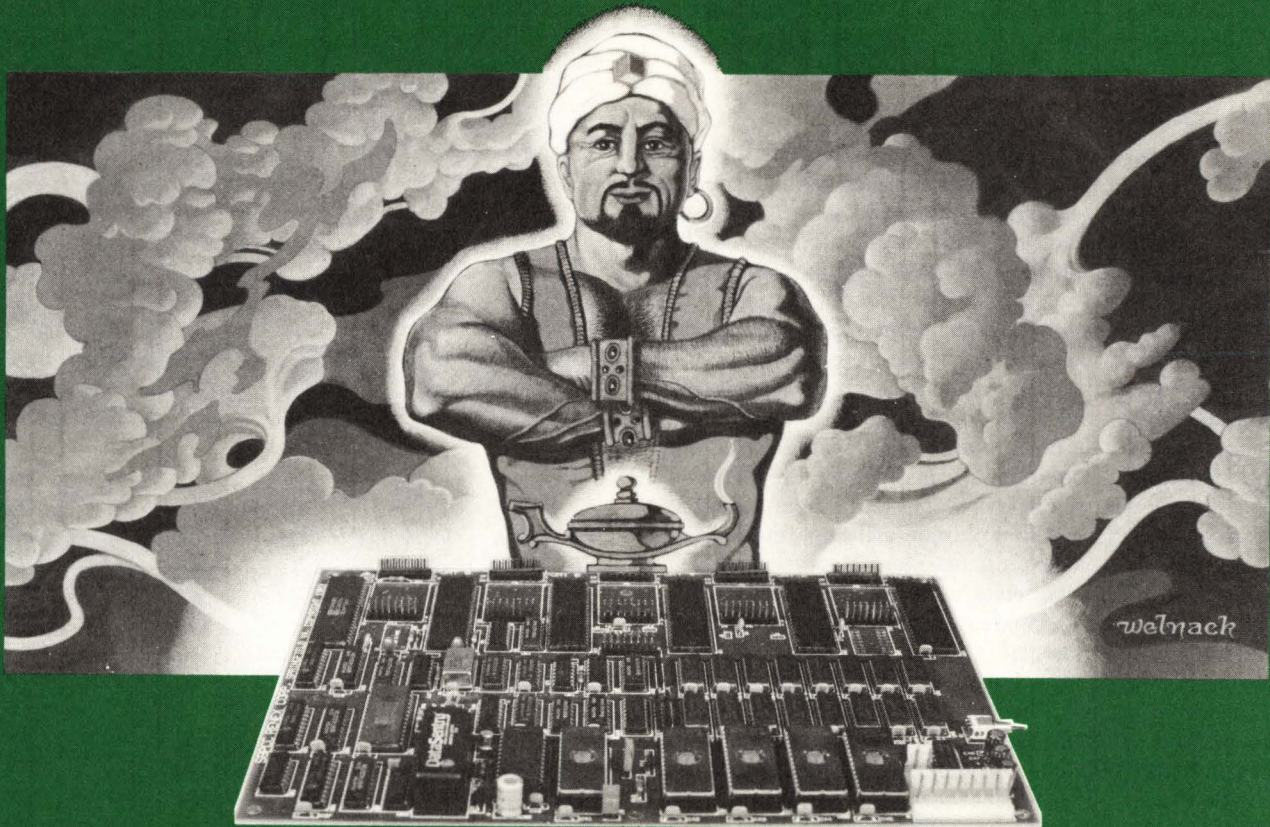


The logic simulator is the most important tool in semi-custom design. Over 50 percent of the chip design revolves around simulating the operation of the circuit, generating the test vectors and performing the fault analysis. Each vendor has a simulator which usually runs on a host such as a DEC VAX or IBM mainframe due to the tremendous computational requirements of large logic simulations. Most third party workstations offer simulation capability but do not have the horsepower to perform large simulations quickly. A large simulation running on the VAX might take 25 minutes while the same simulation running on a workstation could take four hours.

Using an efficient, user-friendly simulator will facilitate semi-custom design. The simulator's efficiency is directly tied to the cost of running a simulation; the more CPU time the job takes, the greater the cost. In most cases, the system architect will be required to simulate the circuit many times. A reasonable estimate of computer charges would be \$20,000 per design, dependent upon the size of the circuit, the number of simulation iterations and the architect's familiarity with the simulator.

Figure 8: A standard cell die designed by ZyMos Corp. includes a block of RAM.

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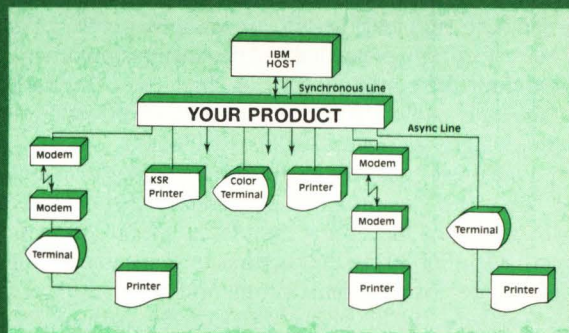


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The ability to set breakpoints in the simulation can influence the time as well as the cost of the simulation. Breakpoints are predefined times where the simulation stops and lets the architect examine the results. If a problem is identified then, it can be rectified immediately without waiting for the entire simulation to be completed. This saves time and money since circuit simulations need not be repeated each time a small problem is encountered.

Vendor Libraries

Most vendors offer several different libraries based on functional performance. These libraries are often characterized by the gate width. In most instances, the vendor first introduces the 5-micron library, then the 3-micron and most recently the 2-micron. But often, not all of the macro functions in recent libraries have been characterized or tested, since it requires much time and effort to benchmark each function. Some vendors let customers do the evaluation to expedite the process.

If performance is critical throughout the circuit, it may be advantageous to seek out a vendor in whose library the performance of most of the macros has been verified. In any event, potential customers should inquire about the number of components which have been 100 percent tested and characterized.

Macro models in the library must describe how the function performs when laid out on the actual chip. Therefore, it is critical to evaluate the parameters in the model. For example, CMOS delays are load dependent and must be characterized in the model. Other parameters include: intrinsic delays, setup/hold times, temperature sensitivities, input voltage sensitivities, fan-in/fan-out and power dissipation. Not all libraries and simulators take all of these parameters into consideration, so it is beneficial to investigate the model descriptions as well as the simulator.

Cost Estimation And The Design Cycle

Non-recurring engineering (NRE) costs are directly related to the process technology needed and the design complexity, and do not include the computer time or chip costs. Typical NRE costs for a gate array range from \$5,000 to \$75,000 while standard cell designs go from \$20,000 to \$150,000.

To reduce these costs, the customer should perform as much of the front end design work as possible. Front end tasks include: designing the circuit, simulating the circuit, generating a netlist (preferably in the vendor's format), generating test vectors and performing fault simulation. The less work the vendor has to do, the lower the NRE cost. In addition, system architects that do much of the design themselves better appreciate the various subtleties of the circuit as well as how the chip will function when placed in the system.

Interfacing to a vendor can occur at different stages of the design cycle (Figure 3). Some suppliers will accept a functional block diagram while others require a simulation and netlist. Some vendors will allow the customer to perform placement and routing of the circuit, which involves assigning the macro locations on the chip and then connecting the wires between these functions. This is typically performed automatically by complex software programs and is referred to as "auto place and route." These programs usually do a good job and typically complete 90% on the first pass. The remaining interconnections are then completed by the system architect.

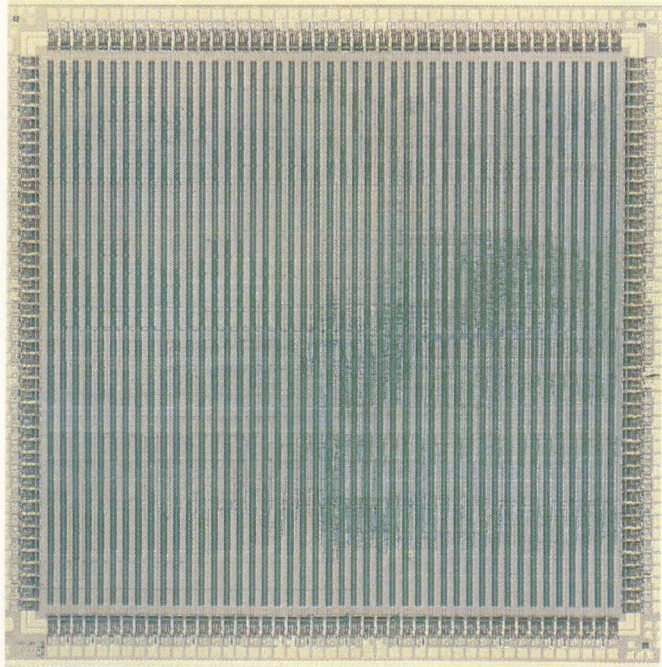
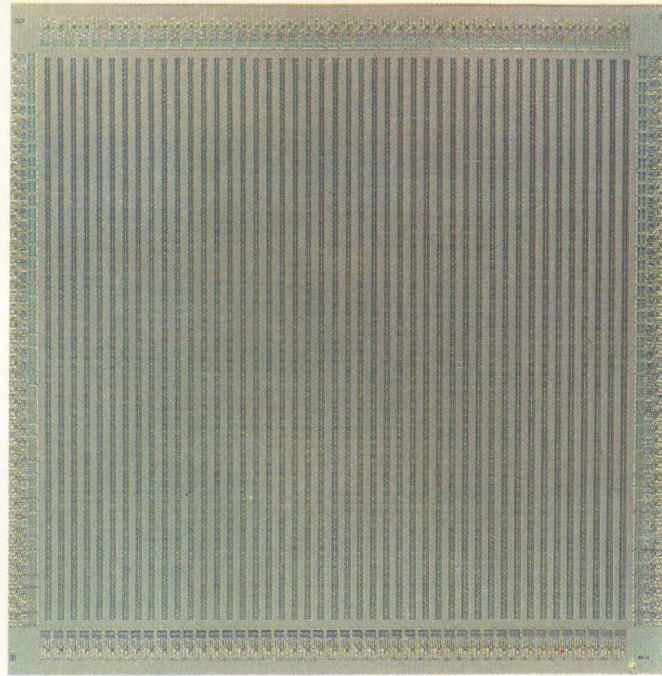


Figure 9: An 8000 gate CMOS array before and after metalization.

Manually routing the interconnections can be extremely time consuming, so there is a tremendous effort underway to enhance the capabilities of these software programs.

In many cases, manual placement and routing is unavoidable. For example, critical timing paths should be laid out manually since auto place and route programs cannot discriminate between critical and non-critical paths. The customer must identify these critical areas and bring them to the vendor's attention. In any event, vendors can usually handle the design process better after the point of circuit simulation. This is an especially good rule for inexperienced semi-custom designers. Once the customer acquires some experience, he will be in a

Allowing extra time to perform a semi-custom design is something that most vendors strongly recommend.

better position to judge how much design responsibility to assume.

The next stage in the design cycle involves the transformation of the symbolic layout data into pattern generated (PG) tapes that allow the creation of masks. Seldom does the customer get involved in this stage of the design cycle, though some vendors will accept PG tapes from a customer. Once the masks are created, a few prototypes are tested and sent to the customer for verification.

Testing these VLSI chips requires sophisticated automatic test equipment (ATE). Even with the most sophisticated fabrication process, vendors are not viable suppliers if they cannot adequately test the chips after fabrication. The cost of sophisticated ATE ranges from \$200,000 to one million dollars, and vendors who cut costs by superficially testing their chips should be avoided. Potential customers should evaluate the amount of emphasis a vendor places on quality assurance and testing.

Conclusion

As with any emerging design methodology, certain voids exist. The greatest gap that currently plagues the semi-custom industry are standards to allow the transfer of chip data from the customer to the vendor. Whether the customer has a netlist, the symbolic layout data or even the PG tapes, there is no guarantee that the vendor can directly use this data to build a chip. Presently, there is little compatibility among IC vendors. There is also a lack of data compatibility between workstation manufacturers and IC vendors which further complicates the problem. Industry experts have joined together and formed committees to define and adopt a data transfer standard. Whether a final standard can be agreed upon remains to be seen.

Another area that requires an in-depth study is whether a vendor has an agreement with another vendor to second-source fabricate chips. Without a second source, the customer must rely on a single vendor. As a worst case scenario, what can a customer do if the vendor goes out of business or his fabrication facilities are destroyed through a natural disaster? The customer may be left with masks, PG tapes, layout data, a netlist or test programs that are incompatible with other vendor's facilities. As with off-the-shelf parts, most designers would not buy ICs that are available from a single vendor.

Comparing each stage of the design cycle between vendors before the actual design begins and verifying that an alternate source can duplicate the procedure is insurance that schematics can be turned into reliable working chips. If there are differences, inquire about additional costs that may be necessary to bridge the incompatibilities. For example, transferring PG tapes from the primary to the secondary source may require building new masks at additional cost to the customer. In this instance, the customer may wish to have ownership of the masks. How-

ever, this can also be a problem because slight variations in fabrication facilities may require slightly different masks, thus ownership would be useless. Since there are many subtle differences in the various second source agreements between vendors, it is up to the customer to investigate the details of their vendor's second source agreement at the outset.

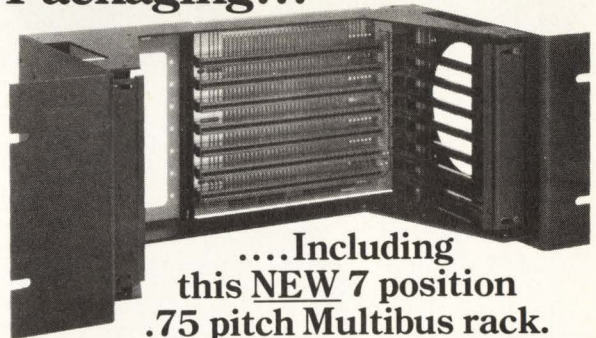
Allowing extra time to perform a semi-custom design is something that most vendors strongly recommend. When customers are quoted a certain turn-around time, this does not take into account any design oversights that may cause an iteration in the design cycle. It also overlooks the extra time the customer may need to fully check for any oversights by either the vendor or system architect. Allowing extra time for the first semi-custom design is almost mandatory.

Finally, some vendors offer more customer assistance than others, and although this is an important consideration it should be weighted accordingly. In most cases, such assistance is only necessary for the first few semi-custom designs. After that, the customer can design chips with less help from the vendor. □

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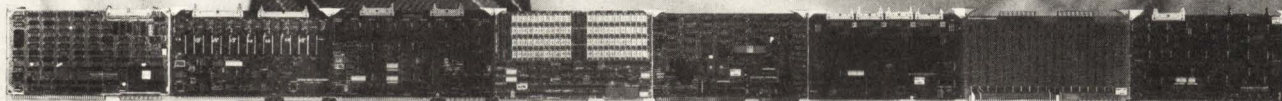
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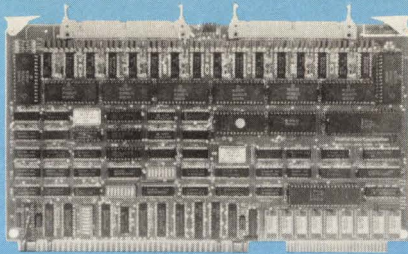
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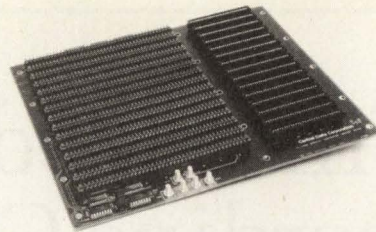
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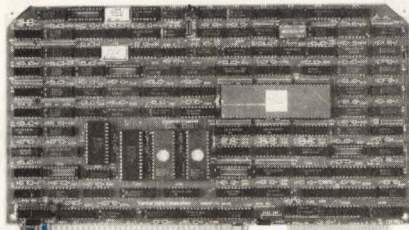


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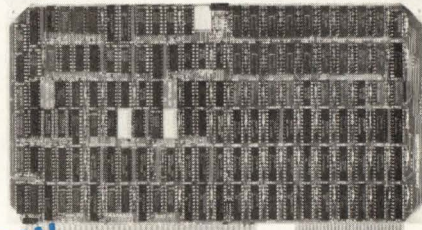
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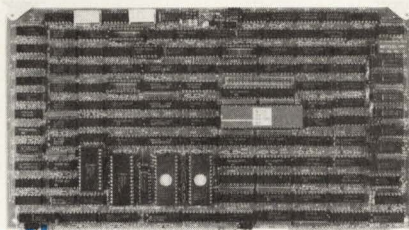
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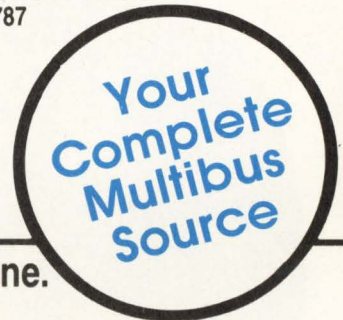
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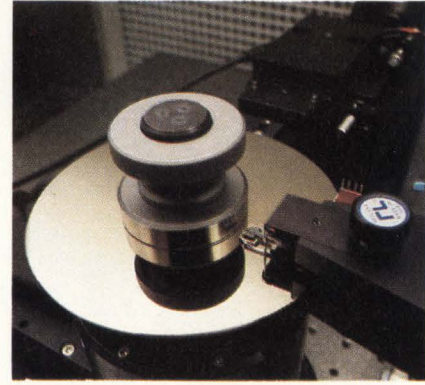
by Julie Pingry, Editor

Although magnetics is one of the older disciplines used in current computer systems, very intense developments are bringing about huge increases in the amount magnetic recording devices can store. As with any technology that has been used for many years, magnetic data recording on particulate ferric oxide has enough foothold in companies' development labs to allow it to progress competitively with other technologies. At least for some time, improvements in oxide media will provide a refined storage vehicle to compete with all comers, notably

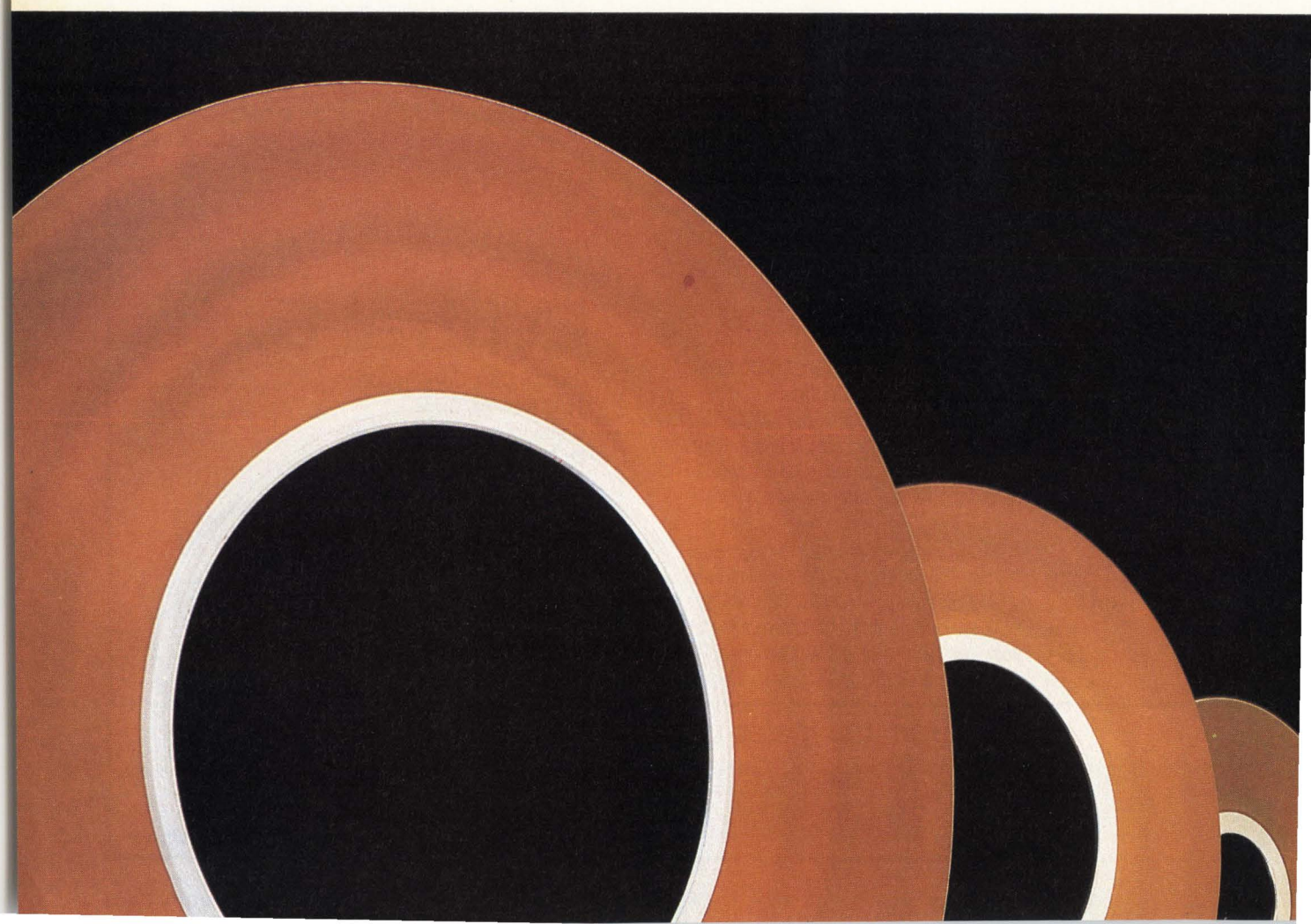
metallic "thin film" surfaces.

In both particulate oxide and metallic media, specific advances and twists on the standard media and techniques are in the works that offer densities up to an order of magnitude greater than the most advanced disks now available. But perhaps the most visible increase in magnetic storage capacity is promised by perpendicular or vertical recording.

Refinements in materials and processes for manufacture are providing substantial increases in media capacity, as well. Magnetic surfaces like those used for the sub-four inch "microflopies" have a stronger magnetism, or coercivity (see



Above: Testing a metal thin film disk at Information Memories Corp. Below: photo courtesy Memorex.



Advances in media and techniques offer densities up to a magnitude greater than the most advanced disks now available.

"The Language of Magnetic Recording" box); this allows smaller magnetic areas to be read accurately and thus more information to fit onto a magnetic surface. Special media that are isotropic (see box) also provide opportunities to pack information more tightly. Combinations of mechanical features, like crossing floppy surfaces with rigid substrates and using cartridges improve overall performances.

How much data can be stored on a surface magnetically, whether on a tape, floppy or rigid disk, depends on how densely magnetic areas are recorded. Density is defined both by the number of magnetic flux changes or reversals in an inch, often the same as bits per inch (fcpi, frpi, bpi) and by the tracks per inch (tpi) across the media. Products with higher densities are coming onto the market now, and all of the technologies under development have characteristics that will allow even higher bit density recording as relationships between the media and drive heads, read/write channels and electronics improve.

Advanced Oxide

Particulate ferric oxide is the standard medium for magnetic data storage, and has been for some years. There are currently several particulate surfaces that provide improvements over the capacity of 300 Oersted (see box) media, and are just being introduced into the market.

Thickness of the magnetic surface plays a role in its performance. Ideally, the full depth of the surface is recorded so that, even without an erase head, a track can be overwritten with no residual noise on the new data. With 300-350 Oersted media, the coating has been getting thinner to allow a relatively weak signal to record all of the way through the surface. Theoretically, a surface as thin as 10 to 15 microinches could be applied, but with particles that are about four by 20 microinches, the deposition process would

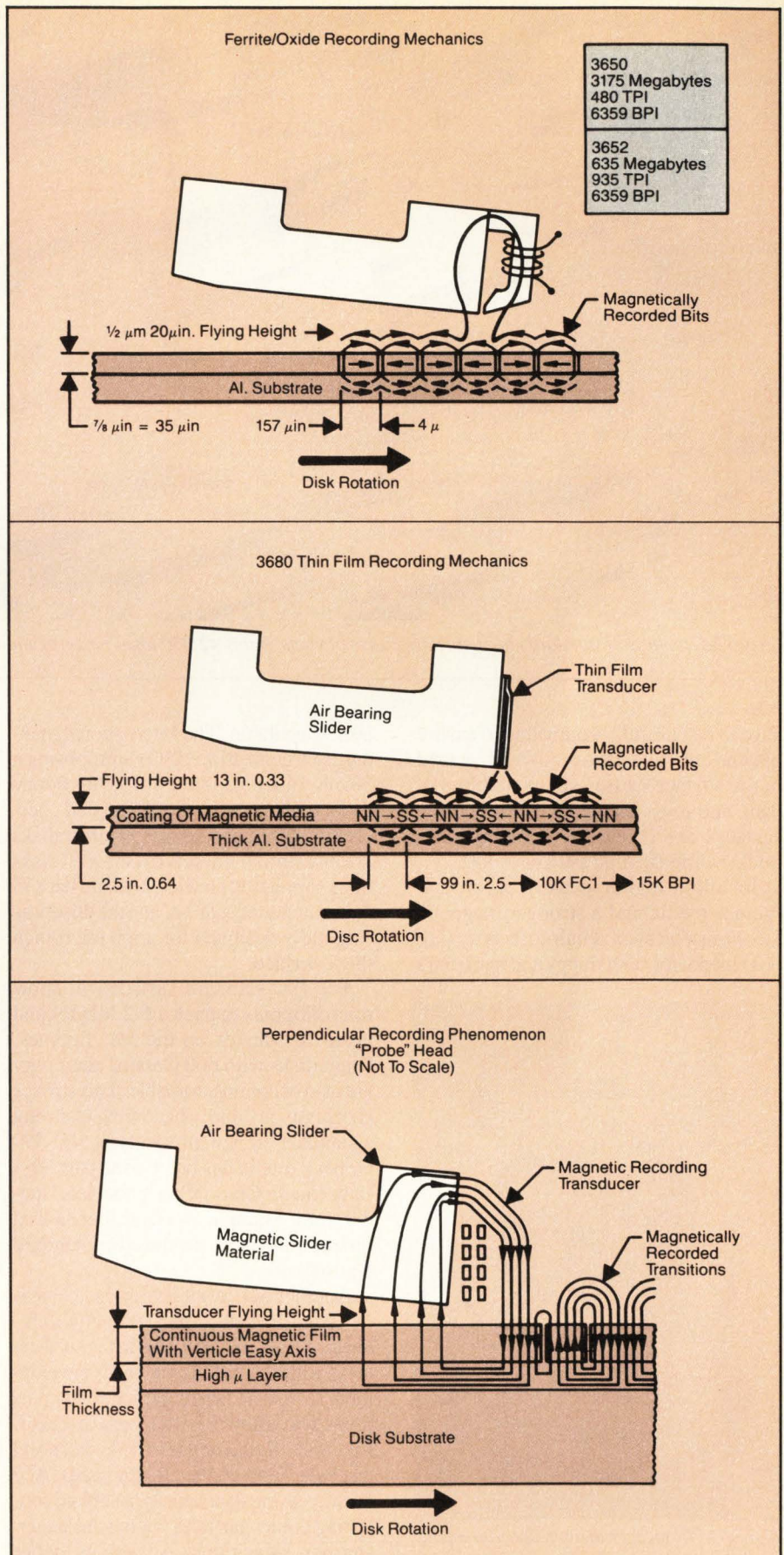


Figure 1: The three main magnetic recording technologies: ferric oxide, thin-film metal heads and media and perpendicular recording, as illustrated by Memorex rigid disk systems; the same techniques can be used on floppy disks.



Figure 2: The bias of standard magnetic particles is obvious in this 42,050 times magnification from 3M.

have to be carefully controlled to ensure that the entire surface is covered. A void in the surface causes errors and loss of data, and most standard rigid recording surfaces are about 30-40 microinches thick, while flexible are about 100.

To allow higher density recording, thinner media and a stronger magnetic force must be used. High coercivity (see box) media for both floppy and hard disks

is now available. The International Standards Organization (ISO) is proposing a 50 microinch standard surface for floppy disks with a nominal 600 Oersted coercivity. Although the microflop disks are of a similar coercivity, the 3½" disks Sony supplies to Hewlett-Packard have 75 microinches of coating, and the drive was originally designed for a 100 microinch thick surface.

The ISO standard surface will allow microflop disks to pack 1.6-2 Mbytes and up to 10 Mbytes on the 5¼" floppies. Rigid disks with 600 Oersted coercivity are also becoming available. This surface coercivity is rapidly becoming as strong a standard in new products as 300-350 Oersted media has been in the past. Dysan's (Santa Clara, CA) "chocolate" medium, for example, is a Cobalt-enhanced ferric oxide that is produced on standard equipment.

Another way to achieve higher capacities is with smaller particles. Audio recording uses fine particles in the surface, and similar materials are under development for use in data recording. Finer particles will allow a better surface finish, for closer flying heads in rigid disks and less wear from contact floppy heads. And for increasing data density, a surface consisting of tiny particles has much cleaner, sharper transitions as well as better chances of covering an entire surface with a thinner coating.

Still another particulate media that has

greatly increased information carrying capacity is isotropic. The basic anisotropy (see box) of particulate ferric oxide floppy disks is shown in the directional particles as in **Figure 2**.

Uneven expansion due to heat and humidity changes are a major problem for anisotropic substrates; since the surface does have an orientation, changes in the medium are not consistent across the face of a disk, causing problems for interchanging disks, overwriting and later reading. These factors limit track density of floppies to 96 tpi.

Several factors in increasing particulate surface recording density are combined in certain new media. The Isomax medium from Kodak's Spin Physics (San Diego, CA) is not only isotropic (with a squareness of .85, as compared to 0.67 for the URH II Medium from Dysan — see box) but also use a very small, 0.2 micron long particle at a nominal coercivity of 790 Oersteds. The particle's diameter is nearly as large as the length, with a ratio of 2 or 2.5:1, compared to 5 or 6:1 for standard media particles, and three axes of magnetization allow good recording either vertically or longitudinally. Kodak uses Isomax at 192 tpi. In Kodak's lab, 120,000 fpci linear density has been demonstrated.

Another solution appears to be the stretch surface recording (SSR) technique from 3M (Saint Paul, MN). This disk scheme is a cross between floppy

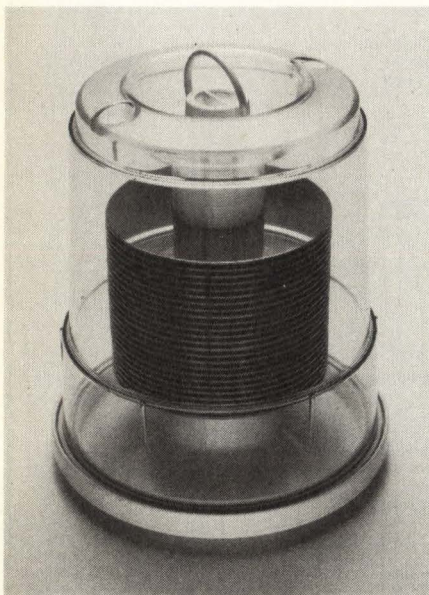


Figure 3. To protect their metal-film media from contaminants, Information Memories has developed sealed containers with inert gas to maintain Class 100 clean room conditions during shipping.

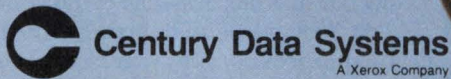
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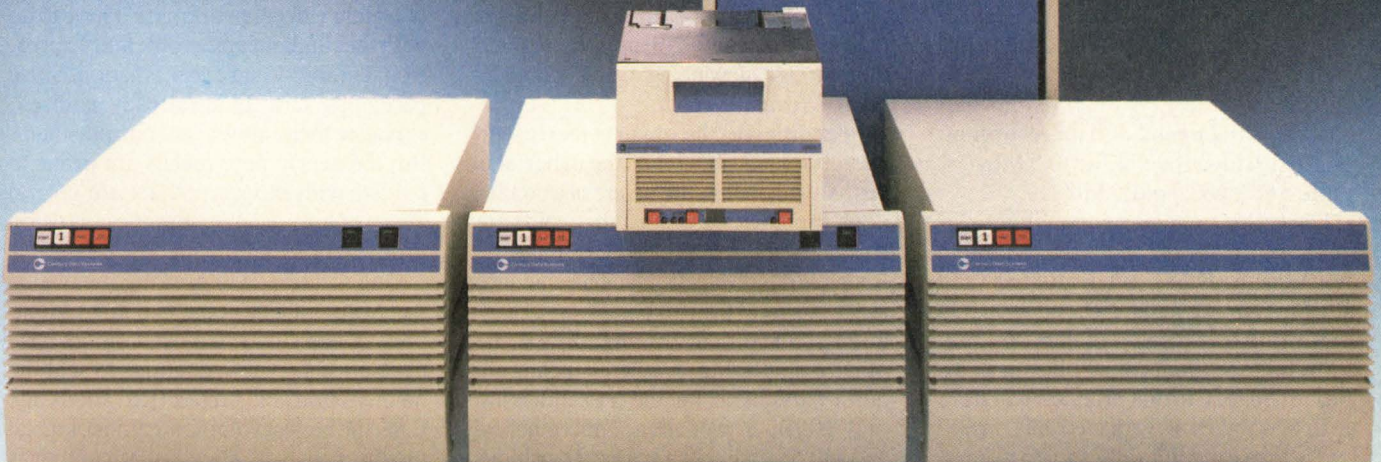
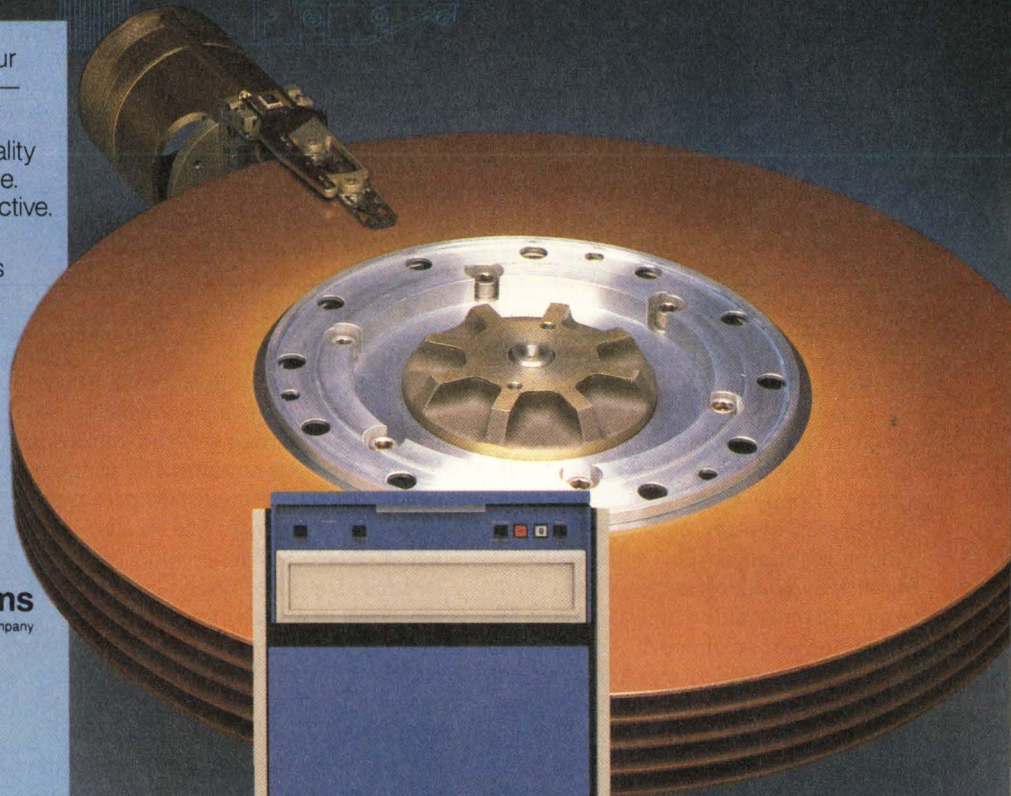
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The Language Of Magnetic Recording

Since it is based on the science of magnetics, and not electronics, data recording and storage use terms otherwise unfamiliar in computer literature. The terms defined here are just those used in this article; the field uses many more.

Anisotropy: disuniformity; for magnetic surfaces, it refers to the directional magnetic and physical bias created by the stick-shaped particles, the long dimension of which generally has a specific orientation.

bpi (bits per inch): linear density measure dependent on encoding scheme; bpi may or may not be equivalent to **fcpi** or **frpi** (see below).

Coercivity: the value of the opposing magnetic intensity that must be applied to a material magnetized to saturation to remove the residual magnetism; how strongly a magnetic surface holds its charge; measured in **Oersted**. Higher numbers mean that the material is more difficult to demagnetize.

fcpi, frpi (flux changes per inch, flux reversals per inch): interchangeable specifications for linear bit density; read heads sense transitions in the magnetic field from one direction of magnetization to the other.

Isotropic: having the same characteristics (mainly mag-

netic, here) in all directions; physical isotropy is important for floppy disks, to ensure that expansion due to humidity and temperature is even in all directions; see also **anisotropy**.

Microinch: One millionth of an inch, used here since disk sizes are also in English measure; 1 microinch = 25.4 nm or 0.0254 microns.

Oersted: the intensity of a magnetic field in a vacuum in which a unit magnetic pole experiences a mechanical force of one dyne in the direction of the field; a measure of **coercivity**.

Serpentine recording: a method of recording on tapes in which tracks are recorded in alternate directions, i.e. track one is recorded left to right, track two right to left, track three left to right, and so on; this speeds reading and writing because no rewinds are required to access all tracks.

Squareness: ratio between the ability of a surface to be magnetized and its maximum flux density; higher squareness media provide a more accurate record of the magnetizing field applied during recording.

tpi (tracks per inch): measure of how tightly packed the concentric rings of magnetically recorded information are on a disk surface.

and rigid, using 600 Oersted floppy-type recording material stretched across a rigid substrate. With this combination, the uneven expansion effects of temperature and humidity changes on the 60 microinch floppy material are minimized, but the non-contact read/write style of a floppy is retained. This scheme uses a modified Winchester head, and both fixed and removable drives using the SSR technology are planned.

Stabilizing a flexible disk with a rigid substrate for higher capacity is also possible without attaching the two materials. Iomega makes use of air pressure created by disk rotation to stabilize a flexible media about 100 microinches above a stable surface. The head is not in contact with the medium, but flies at about 10 microinches, allowing high density data to be read accurately. With servo information, 18,000 fcpi and 300 tpi recording, the 8" cartridges pack 10 or 10.5 Mbytes, while 5 1/4" disks hold 5 Mbytes.

The move to higher coercivity material has also spread to tapes; 3M offers cartridge tapes in two coercivities, and though both are now recorded at 10,000 frpi, using the stronger of the two could allow huge amounts of storage on a single cartridge. Current products can store up to 67 Mbytes of formatted data on 600 feet of tape, and within five or six years, as much as one or two Gbytes could be held by a single tape cartridge. With IBM's Del Oro cartridge announcement,

tape use will no doubt be an issue again. Although the specs will not be public until next year, it appears IBM is using a chromium dioxide surface with non-contacting heads. The same amount of information can be stored in a single tape package as on a stack of floppies. And because of the nature of tape, still more information can be packed into the finished space without the use of new technologies.

Metallic Surfaces

A natural way to enhance the magnetic properties of a surface is to increase the portion of the material that is magnetizable. Ferric oxide surfaces are only 40% magnetizable; the other 60% of the surface is a plastic binder material. Surfaces that are about 99% metal, often called thin film, are now being manufactured by several firms.

In addition to the obvious increase in coercivity possible when the material is virtually all metal, the nature of a continuous film coating is such that voids are less common, even in very thin layers. Refinements on electroplating techniques are only one of the two basic ways of producing a metallic recording surface; the other is sputtering. Sputtered metals are quasi-particulate, but the crystallines are only 0.05 micron or about 2 microinches, and still provide much sharper transitions than particulate oxides.

Metal media also is less noisy than oxide media by a factor of 10 at relatively

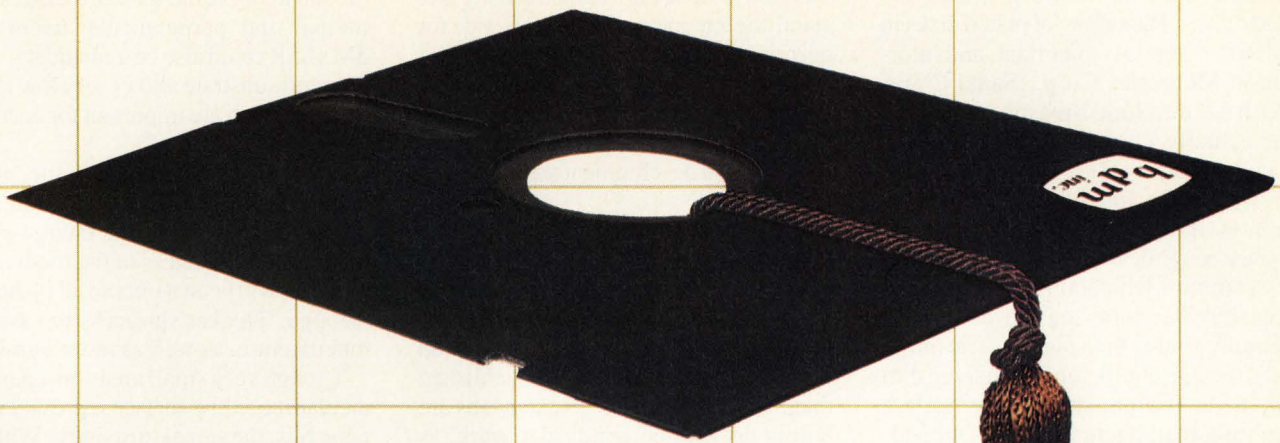
low density. The work in thin film metallic media is fueled by the theoretical potential of 200,000 fcpi and more, and one of the main reasons that so little metal media is in use is its short supply.

State-of-the-art commercial metal media is usually a very thin film — on the order of 3 microinches — and 600-675 Oersted coercivity is used. In addition to the two methods of deposition used, several metals have been used. Most surfaces are now Cobalt/Nickel/Phosphorus alloys. All of the variations in metallic surfaces are the mark of a very young technology, and they cause a lack of not only standardization, but interchangeability.

Other factors in the slow introduction of metal media onto the market have to do with the fundamental problems of corrosion, durability and contamination. Since particulate surfaces are already oxidized, exposure to the air will not corrode them. But the nearly pure metals are prone to oxidize with exposure; there are several views of how to cope with the corrosion problem of metal media.

One solution is to coat the metal surface with a thin protective coating. Memorex (Santa Clara, CA) and others have developed very thin coatings to seal the medium from air. Ampex (Redwood City, CA), the largest volume supplier of metal media, however, claims that coating is not necessary.

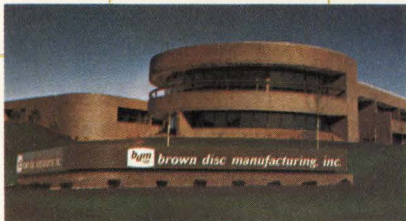
Contamination can be deadly between head and medium when the surface is



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soft, as pure metals tend to be. For some time, metal media will be most suited to fixed drives. Packaging of plated disks in sealed containers is important, and Information Memories Corp. (Santa Clara, CA) have developed plastic containers that actually contain Class 100 clean room air (Figure 3).

Keeping the manufacturing process clean is also a challenge with plating. Surface roughness and defects are much less common with sputtered metal surfaces, but the sputtering process is considerably slower than plating. The initial investment in equipment for making thin film media is high, and there are delays in getting manufacturing lines shipped. But in the long run, metal surfaces may not be more expensive to produce.

Thin film metal may also be an important surface for tapes; though it has not been perfected for data recording, the work with metal audio tapes shows some possibilities. With Cobalt-Nickel surfaces, tapes will have similar storage capacities to optical disks, according to 3M. Metal tapes may even have a greater potential capacity than optical disks.

The very nature of an all-metal surface for magnetic recording allows tiny areas to carry enough signal to be read with little noise. Demand for thin film metal recording media is large; the many companies (estimated at 30 or more) making metal media are only just gearing up, and though each is finding different solutions to the problems of metal surfaces, more drives will appear using metal instead of oxide this year.

Perpendicular Recording

Since magnetized sectors are much thin-

ner than they are long, yet another way to increase surface information density is to stand the magnetic charges on end, for perpendicular or vertical recording. This idea was put forward by Professor S. Iwasaki of Japan in a paper at the 1976 Inter-mag conference and has the attention of research and development teams in many companies.

Both floppy and rigid disks can be recorded vertically, and the potential is so great that new companies like Lanx (San Jose, CA) for rigid and Vertimag (Minneapolis, MN) for floppy media production have been formed. Large, established magnetic media firms' research labs are humming with perpendicular work, as well: 3M, Memorex and Control Data's Magnetic Peripherals Inc. (Minneapolis, MN) all see a rosy future for the technique. MPI have licensed Lanx technology for rigid disks and are also developing flexible media. One thing these efforts are showing is that media, heads, read/write channels and electronics are very closely tied. Vertimag will market entire drives, though they had originally hoped to use Shugart (Sunnyvale, CA) drives with their media and modified heads; CDC's MPI is also making heads against their original wishes and plans to produce only media.

The two main compounds for perpendicular recording media are Barium Ferrite and Cobalt Chromium. Current development is mostly in sputtered Cobalt Chromium, but vertical recording could also be applied to other media. That possibility is strong with the three-axis, unoriented isotropic particles like Spin Physics' Isomax. And though the technology for vertical recording is not yet com-

mercial, Isomax advertising points out the suitability of the surface to both longitudinal and perpendicular recording. 3M's SSR could also be a candidate, since the rigid substrate allows very low flying heights which are important for accuracy (Figure 4).

One major difference in the media needed for this technique is that it need not be so thin. With the charge going through the thickness of the media, it is much less difficult to record all of the way through. Thicker surfaces are easier to manufacture, as well as more durable.

Though very small areas on a perpendicular recording surface represent magnetic bits, the signals are sharp. With the magnet poles away from the next one with like charge, none of the demagnetization and deforming of the surface found in longitudinal recording takes place (Figure 1).

The original scheme for vertical recording uses two heads and needs access to both sides of the medium (Figure 5). Several companies are developing methods for recording perpendicularly without accessing two sides of the disk. The head for vertical recording is a design challenge even for the original two-sided design. To accurately read such small bits of charge a thinner main pole tip is necessary; the limit is because too thin a pole cannot write all of the way through the medium. The direct contact of the head with the metal medium requires extreme care in cleanliness and the possibility exists for wear problems in flexible disks.

Several of the perpendicular recording media being developed use a permalloy layer under the magnetics, but as with

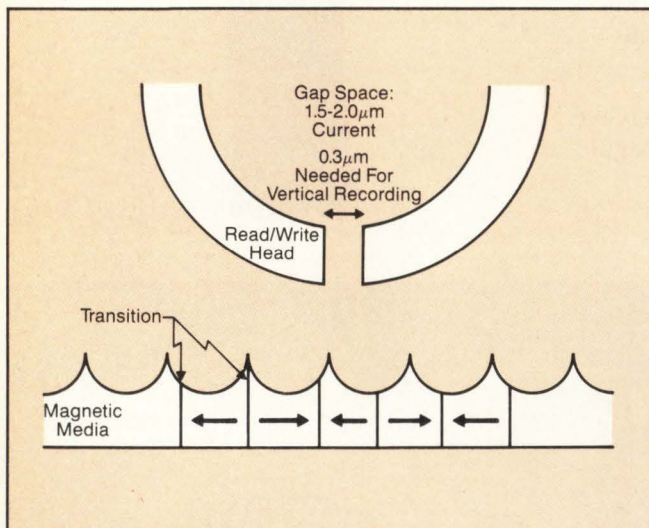


Figure 4: As the magnetized areas get smaller, surface finish and head gap size become critical, as shown here for rigid surface recording.

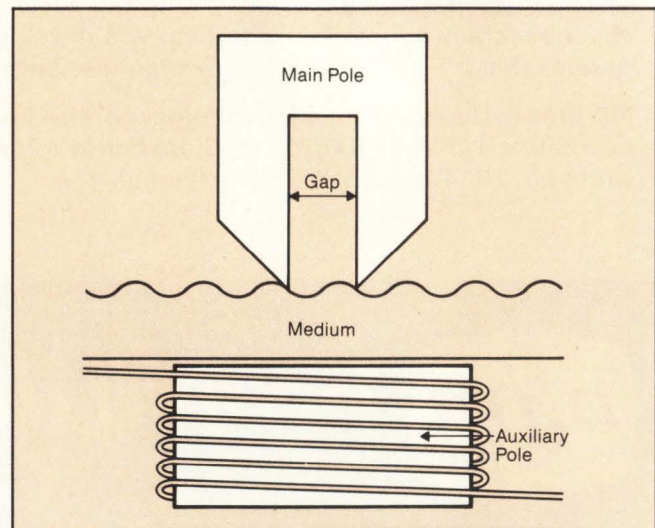


Figure 5: Iwasaki's scheme for vertical recording on flexible media uses a pole on either side of the surface.

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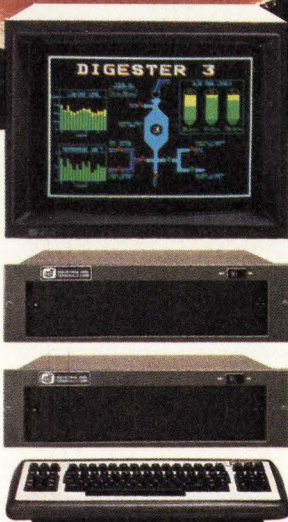
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Data Rate (kb/s)	500	500	500	500	3464	5000	500	500
Connector	50		50	34		ST506	50	50
Positioning	open loop	open loop	reference track	embedded servo	open loop	embedded servo	reference track	reference track

Table 1: Capacities and parameters of current 5¼" floppy disk drives, compiled by Amlyn.

coatings for thin film, there are different camps. And since it is a metal surface, the same questions of wear and corrosion apply; some manufacturers are providing a protective overcoat. The sputtering process used to produce a surface very smooth, free from defects and magnetizable normal to the disk surface is slow, and the equipment is in such demand that delivery is not prompt.

As in **Figure 4**, smoothness is very important with such small points of the magnet available to read. So the same advantage in packing information onto a disk puts burdens on the system. Vertimag's floppy uses only 192 tpi, but with 30,000 fpci, over 5 Mbytes will fit on a 5¼" disk. With increased track densities, the potential of a floppy with 10 Mbytes on it is well within reach.

With rigid disks, the stability of the medium allows track densities of 960 tpi on current Lanx disks. The 20,000 fpci combines for a huge amount of storage per disk, and although eventually probe heads instead of ring heads used on longitudinal recording may be available, Lanx chose to make a medium that can be used with a Winchester head. With the 3380 head at the same flying height as over a standard 3380, the initial capacity increase is about a factor of two.

Using existing heads, channels, or electronics has been a goal of many of the new recording schemes. Initially, the ability to use existing drive parts will help ease these techniques into the commercial market. But to take full advantage of the capacities of vertical recording, current transfer rates of five or 10 Mbits/sec are not adequate. The alternative of slowing down rotation speed is not desirable, because access times would be signifi-

cantly longer. Perpendicular recording on floppies can use Winchester interfaces to achieve system throughput nearing read/write speed. Rigid disks at this high density, however, will only be used to their fullest when new channels and interfaces are developed.

Though there is great interest in perpendicular recording in drive houses, until some methods are proven, it may continue to be a field of vertical work, with medium, heads, channels and drives all created in close cooperation. There is little doubt that perpendicular recording will soon provide huge amounts of storage on traditional size and shape disks, but the question is which of the several methods of achieving that will be most commercially attractive.

Capacities

All of the advances in magnetic recording surfaces allow multiple Mbytes on a 5¼" disk. Current capabilities and potential densities of various media vary greatly, however. And the medium itself is by no means the only factor in capacity. Available 5¼" flexible products, listed in **Table 1** compiled by Amlyn, show several parameters that go into overall capacity. Iomega drives using Verbatim media make use of servo, fast rotation and a cartridge format, for high range floppy recording. As hard disk backup, the 3.2 and 3.3 Mbyte disks fill the 1:3 ratio for a 10 Mbyte drive like the PC/XT's Winchester.

Conventional particulate ferric oxide media with 600 Oersted coercivity like that produced for flexible disks by Brown Disc, Dysan and Memorex can hold 20,000 fpci, though initial products are at lower bit densities. And some feel that

there is opportunity for yet another generation of coercivity left in oxide media, the prospect for as much as 20 Mbytes on a floppy.

With isotropic particles, 30,000 fpci is in range, and Kodak's prototype packs 28,000. Even at standard floppy track density of 96 per inch, 2½ Mbytes per side can be recorded on a 5¼" disk. In the lab, Isomax has reached bit densities of as much as 120,000 fpci.

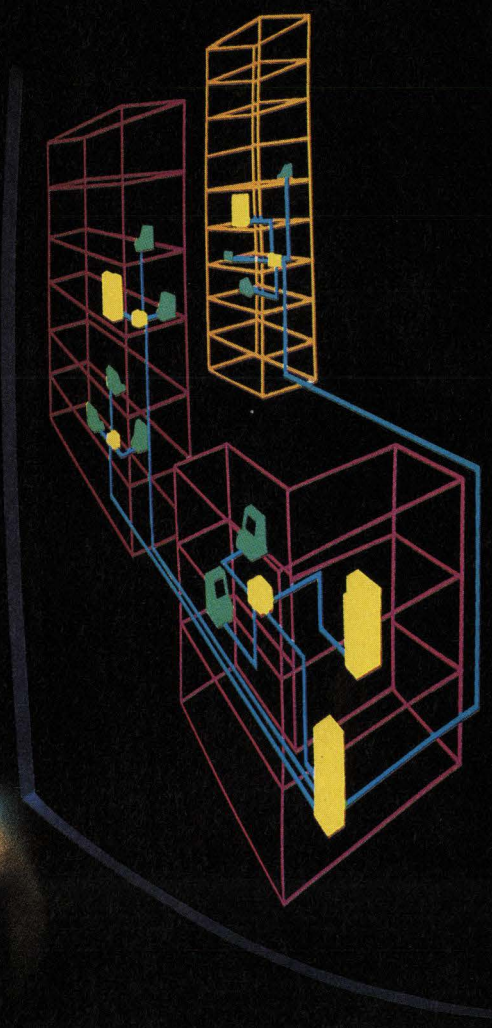
Sputtered thin film surfaces for metal floppies are now often 300 Oersted, but with 600 Oersted, very high densities are possible. In the lab, 3½" disks have as much as 6.2 Mbytes, and there is promise for increases throughout a decade with thin film, as the materials and processes are refined.

By decreasing the overall "floppiness," schemes like 3M's SSR allow as much as 200 tpi for removable and 345 tpi for fixed disks. Prototypes can pack 5 Mbytes per side, without servo assist. 3M foresees 35-50 Mbytes per disk, using as much as 728 tpi and 20,400 fpci, and with thin film surfaces and/or vertical, perhaps even higher linear bit densities in the package.

Capacities of rigid disks will increase tremendously, too. About 10-15,000 fpci is the maximum from conventional media, and it is being used at nearly that now. Several sources are gearing up for 600 Oersted surface production. These allow 960 tpi, for 10 Mbytes formatted capacity per disk. In the lab, linear densities of as much as 36,000 fpci have been demonstrated with "chocolate" media.

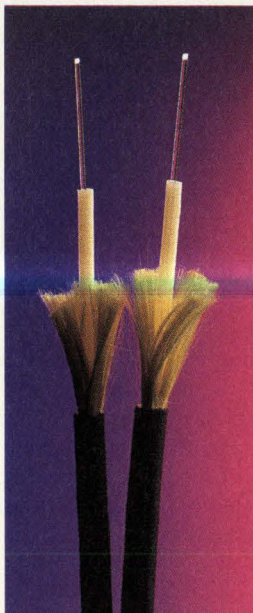
Plated or vacuum deposited metal film media are in great demand to increase capacities of disks, and the supply right now is not near demand. Ampex is the

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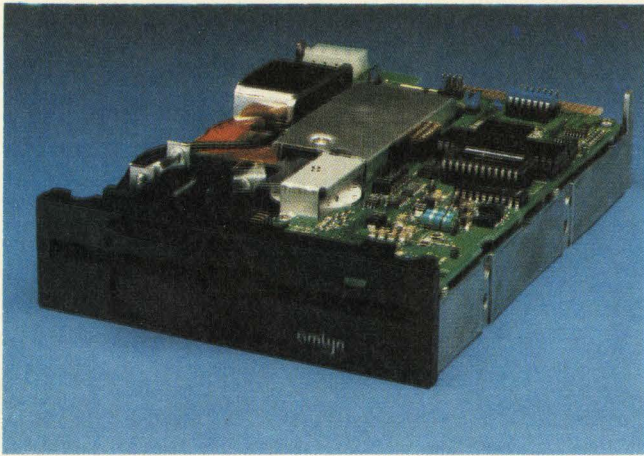


Figure 6: Amlyn's floppy disk drives use closed-loop servo positioning to double the track density.

only volume producer, but others are planning to ship more than evaluation quantities over the next year. Most drives use thin film surfaces to record about 15,000 frpi, but Ampex claims that their uncoated disks can record to 180,000 frpi. With an embedded servo, Cynthia Peripheral (Sunnyvale, CA) packs 13 Mbytes fixed and 13 Mbytes removable on 5 1/4" disks. Sealed, fixed drives will improve reliability by lowering defects and allow denser recording.

Perpendicular recording will increase capacities of both floppy and hard disks by several times. Initial Lanx rigid disks can handle 30,000 fcpi at 960 tpi; Vertimag's flexible disks are being introduced at 30,000 fcpi, as well, but 192 tpi. Memorex sees a 16 times improvement left in magnetic media with vertical; 200,000 fcpi and 900 tpi would move densities into a different range.

And not to forget the old storage styles, tape is also advancing with improved magnetic surfaces. Cartridges hold 60-100 Mbytes today, and within five or six years, will probably hold one to two Gbytes with higher coercivity. Besides their backup and archive functions, tapes in cartridge form are very transportable and reliable. 3M reports about one uncorrectable error in 39 cartridges, and with serpentine recording schemes (see box) and sectoring, access times are closing in on floppy disks.

Of course, access times of floppies or any disk are related to disk size. A huge movement toward 5 1/4" disks is evident in both flexible and rigid, and it would appear that the 8" disk will be viewed as mainly an interim product. The vast quantities of information now stored on 5 1/4" disks will no doubt not be converted to another size. Companies like Xidex (Mountain View, CA) make 8" and 5 1/4" disks, and are moving into the 3 1/2" mar-

ket under license to Sony.

The activity in sub-four inch diskettes has drawn huge attention, and there are some advantages to this new size. Flexible media have the problem of stability and temperature and humidity sensitivity. With smaller surfaces for these environmental factors to affect, the potential for error is somewhat reduced. In addition, the new diskettes are more portable, for use with mobile computers. But the portable computer market is still relatively small and many never reach huge proportions.

The increased stability and schemes like a rigid hub and spring-loaded sleeve opening allow microfloppies to be recorded more densely than 5 1/4" disks. Since all of the sub-four inch disks use 600 Oersted media, they have capacities roughly equal to minifloppies. Still, there is no clear indication that a large portion of the 5 1/4" business will be lost to smaller disks.

Future Recording

With technologies developing now, it is entirely conceivable that a 5 1/4" magnetic surface will hold 15 Mbytes per side, vertically recorded. These disks could go into an eight-platter drive, for 250 Mbytes total storage in a small package. The increasing sophistication of software with artificial intelligence and multiple user capabilities will create more places that need large data storage capacities. A central node in a network and central sites will always use as much storage as is available.

Providing many times the storage capacities now available through thin film media and heads, as well as vertical recording and the other special configurations of media will require changes throughout storage systems. Right now, a 10 Mbit/sec transfer rate is being stan-

darized, but these technologies could make use of 15. Similarly, servo or other positioning methods will be required for very dense surfaces to be used interchangeably, channels and heads will need to be optimized for smaller magnetic areas and more care may need to be taken to keep contaminants away from the tightly packed surface and lower head-to-disk flying heights.

The challenge may be greatest for flexible media, as its main advantage to date has been low cost. Now, there is a desire for twice the capacity for only about 10% more cost. So some of the technologically sound solutions to packing more data onto floppies may not be made into products.

Advances in media may provide opportunities for VLSI for new standard speeds and configurations. Once this scale of integration can be used on these new storage systems, prices will drop and the new high capacity drives will be able to compete in price with those already on the market. The finer scale and more sensitive equipment may also provide increased markets for companies making alignment disks and drive and disk test equipment like Dymek (San Jose, CA), Dysan, with their test diskettes, and Applied Circuit Technology (Anaheim, CA).

Demands created by the density of the new magnetic recording technologies, like error correction and servo positioning schemes are only part of the story. Users will also want to continue using the old storage systems and disks they already have, so backward compatibility like that seen in Amlyn and Drivetec high density systems that can read both old and new diskettes will be important.

Technological advances in many aspects of magnetic recording media will provide alternatives for extremely large storage capacity in small spaces. Initially, products that can make use of existing head, channel and drive technology may have an advantage. But over the long term, changes will probably come about in every part of disk and tape drives to support each of the schemes that can provide both economy and capacities. □

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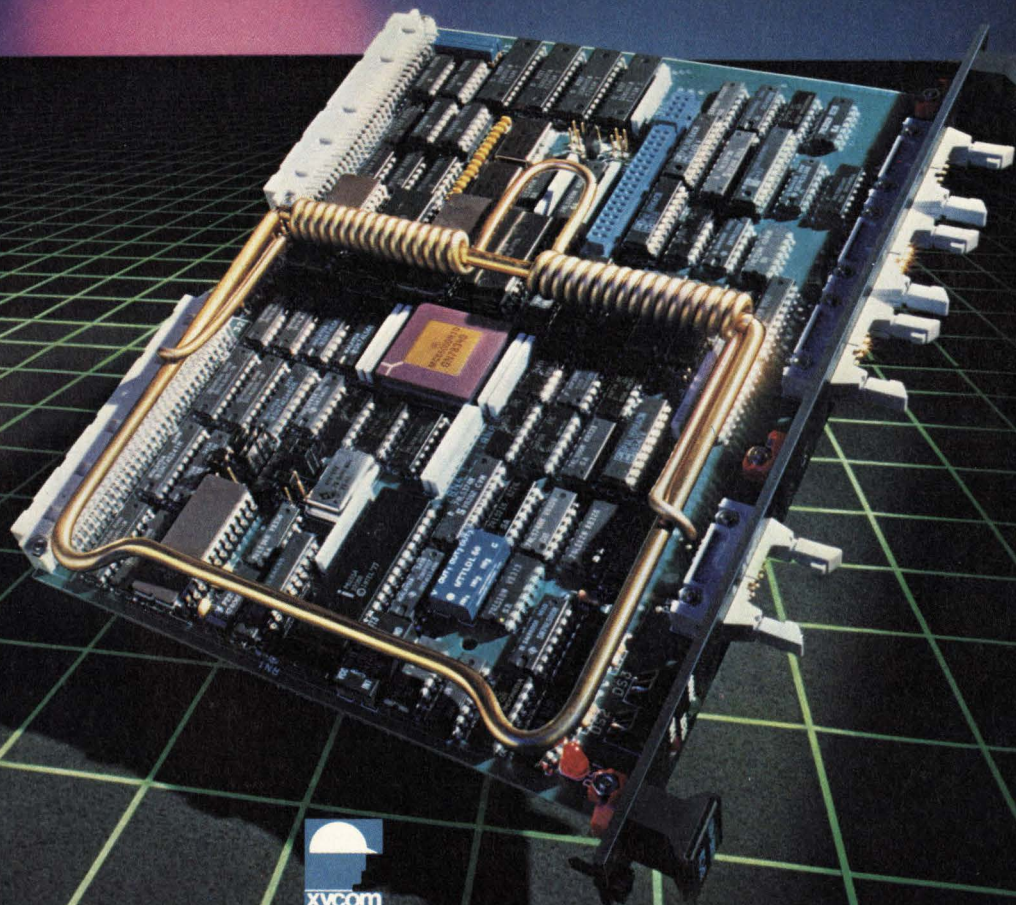
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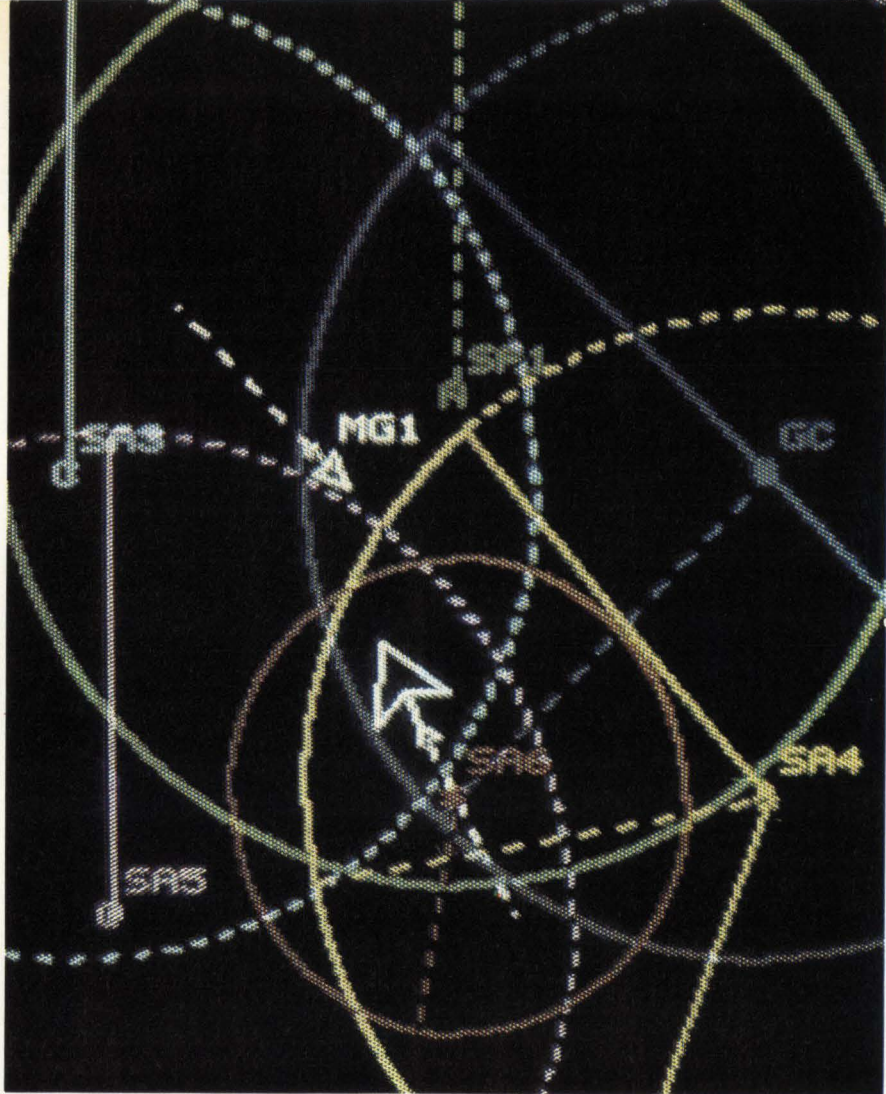
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Right: Training simulator from Litton's Applied Technology Division alerts air crews they are being illuminated by hostile radar, permitting pilots to take electronic countermeasures.

Below: The Excellon XL-5 machines are used at Northrop's Defense Systems Division to prepare circuit boards for airborne electronic countermeasures systems.



Defense Electronics And Industry Synergism

by M.R. Hanrahan
Departments Editor
Megan Niels, Research Assistant

The scope of military electronics is broadening as the push for advancement creates collaborative efforts between commercial enterprise, university research, and the Department of Defense (DoD). It is estimated that approximately 40% of all EEs are involved in commercial defense labs or defense research projects. The Reagan Administration's Strategic Defense Initiative (SDI), with a \$2 billion R&D budget, is expected to funnel funds into the electronics industry at an unprecedented rate. Those companies

manufacturing high-speed, high-capacity computers using parallel processing stand to benefit greatly from continued DoD support of programs such as VHSIC (Very High-Scale Integrated Circuits) and Gallium Arsenide research. If Congress approves the 13% budgeted raise in DoD spending levels, more than \$35 billion of military electronics business will open up.

VHSIC Origins

The VHSIC program was established on the premise that high-throughput signal processing VLSI would meet defense reliability and environmental requirements. The original goal was to run a

pilot-line of processors containing 250,000 gates, operating at clock speeds of at least 25 MHz, and performing several million to several billion operations per second. The processor chips were to perform with a functional throughput rate of 10^{13} gate-Hz/cm² at a .5 micron size. This technology, when inserted into existing military hardware would withstand radiation up to 10^{11} rads/cm². Built-in testing at the chip level was incremental to the program's success. Speed and circuit density were to be obtained by scaling down ICs, reducing channel length and oxide thickness, decreasing supply voltage, and developing new types of system architecture and software.

MIL-STD-883.



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The overall goal of machine intelligence will be supported by developments in key areas of artificial intelligence, GaAs-based systems, and signal processing.

Phase I VHSIC contractors were bidding for work in the areas of NMOS, bulk CMOS, CMOS on SOS, and bipolar technologies for the design and fabrication of chips for application-specific military systems. The original VHSIC contracts were bid on by IBM, Texas Instruments, Honeywell, TRW, Hughes, and Westinghouse. Each contractor manufactured a different brassboard for insertion into existing military hardware, and each developed a unique approach to developing the VLSI circuit. The NMOS development has been undertaken by IBM, while Texas Instruments will use NMOS for memory devices and Schottky TTL for signal processing. Honeywell is researching dielectrically isolated bipolar technology and TRW is working with triple-diffusion bipolar and p-well CMOS. CMOS in SOS (sapphire) research has been undertaken by Hughes. Westinghouse devices will be based on bulk CMOS technology. Phase II of the VHSIC program should see the attainment of submicrometer geometries packing 100,000 gates per chip at throughput of 10^{13} gate-Hz/cm². Bidders on Phase I have been joined by RCA Government Systems Division, and E-Systems (a Western Electric subsidiary).

Maintaining VHSIC

Funding for the VHSIC program has remained at the '84 budget level of \$120 million as transitional difficulties from lab to actual weapon system are occurring. The VHSIC goal of a 1.25 micron silicon chip is expected to increase computing power 100-fold. Program expenditures include more funding for CAD tools and capability testing with hopes for a .5 micron chip by the late 1980s. DoD standardization will attempt to address the denser chips' susceptibility to EMP (Electromagnetic Pulse) and radioactivity in the military environment.

Signal processing, deemed "the greatest challenge to the electronics industry" by Dr. Leo Young, a DoD Research Di-

rector, is heavily dependent on VHSIC work in high speed parallel processing. NASA has designed the MPP (Massively Parallel Processor) which consists of 16,384-bit processing elements in a 128 × 128-bit configuration. Nanosecond speeds are obtained for the real-time operation required for radar and image processing applications.

The DoD's ambition for the VHSIC program is for its use as an incremental building block in the next generation of weapons and communications systems based on state-of-the-art microprocessors and supercomputers. High-density complex silicon devices and superfast radiation-hardened gallium arsenide ICs are expected to fill the military's high-performance requirements.

GaAs: DoD's Protégé

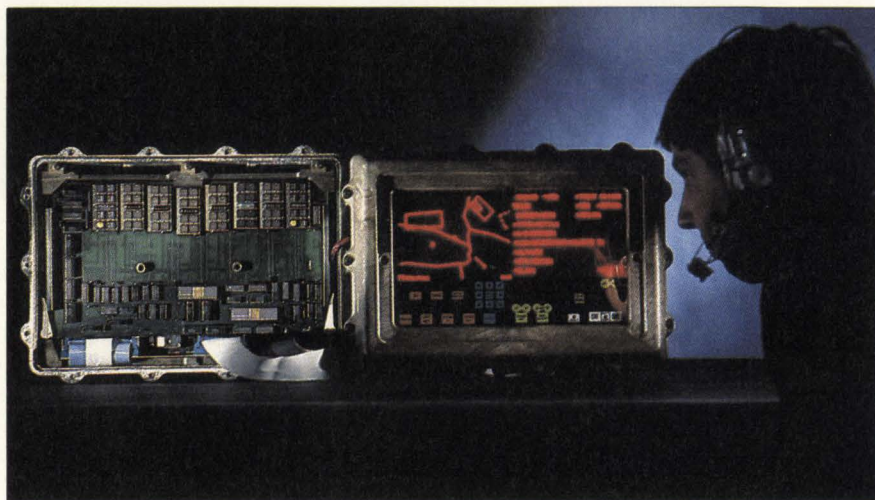
Its promise of very high speed and potential for size reduction in fabrication has positioned gallium arsenide ICs as the basis for future military weapons. As the once-futuristic substance becomes commercially acceptable, development of GaAs as the alternative to silicon accelerates. One of the primary characteris-

tics considered when choosing materials for circuit design are electron mobility and insulation. GaAs offers an electron mobility about four to five times faster than that of silicon. The electrons can be moved at higher speeds and lower voltages than silicon. In weaponry that demands tremendous amounts of energy, these factors are critical.

Because of gallium arsenide's insulating properties, the switching time between devices is extremely fast. The capacitance is lower with gallium arsenide circuits when attempting to run signals over a substrate. The need for special insulating designs is eliminated and superfluous interaction between devices is minimized. The rugged military environment requires these characteristics when meeting the need for maintainability and availability in the battlefield.

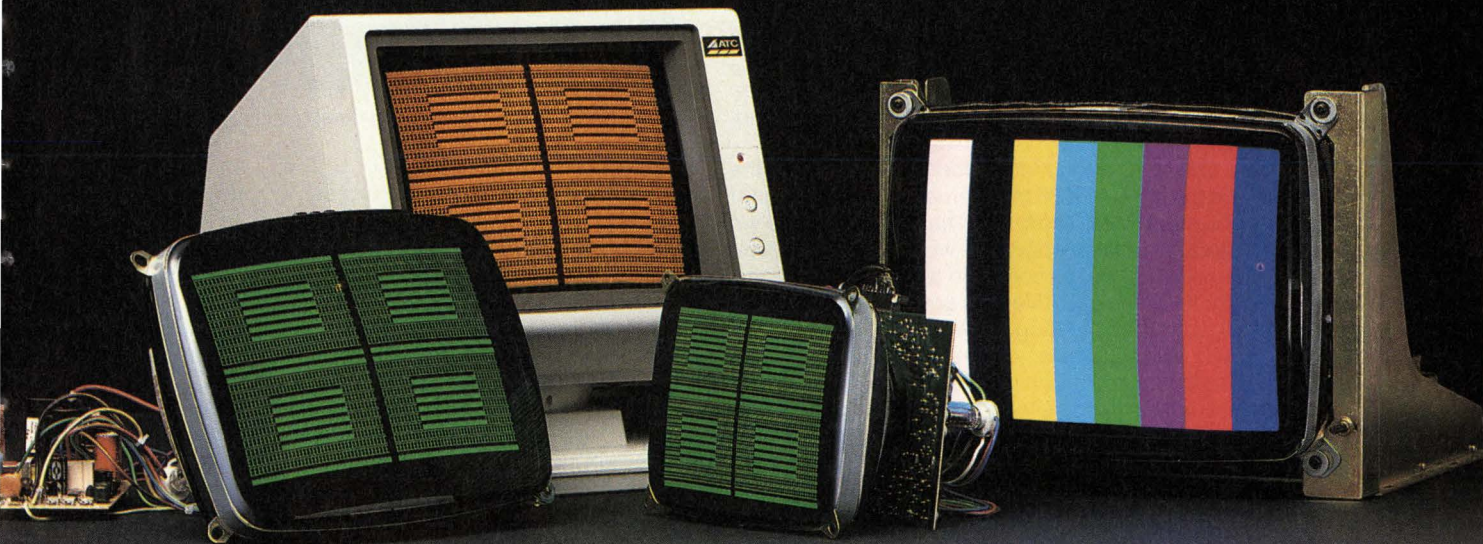
Commercial/Defense Synergism

H. Warren Cooper, Manager of Solid State Systems at Westinghouse's Defense and Electronic Systems Center described the "Commercial/Defense Synergism" occurring in GaAs technology at the IEEE Conference On Technology Policy earlier this year. Planned military applications of GaAs include airborne and ground radar systems, instrument landing systems, satellite communications, expendable jammers, channelized receivers and various forms of electronic warfare. DoD's DARPA (Defense Advanced Research Project Agency) has based its Advanced On-Board Signal Processor on GaAs where it will be used in conjunction with the Air Force in a Strategic and Tactical Array module for space-based radar systems. The Multi-



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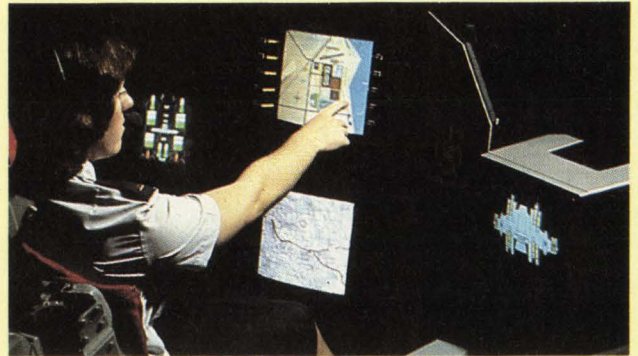
With the advent of integrated electronics displays in advanced cockpit design, the role of dynamic mockups is becoming increasingly important. The human factors researcher can now evaluate dynamic computer-generated formats and real-time interactive control methods in preliminary crew station design phases.

Microcomputer Applications of Graphics And Interactive Communication (MAGIC), being developed by the Air Force's Flight Dynamics Laboratory, is a simulation device of a single-seat, generic "cockpit" currently being used to test integration of voice control and pictorial formats technology. Voice control will allow the pilot to command certain aircraft functions with the use of voice alone (no hands), and pictorial formats provide the capability to combine and present information from a number of sensors to the pilot in a simple, easy-to-understand format.

At the core of MAGIC are four microcomputers based on the S-100 bus and the Intel iAPX 86 microprocessor with a total of 1.4 Mbytes of system RAM. The MAGIC hardware is controlled by a highly modular software package written in Pascal. The speed of Pascal MT-86 makes coding in assembler unnecessary except for the interrupt driven I/O drivers which must interact directly with the operating system.

The flexibility of MAGIC as an evaluation tool is further enhanced by a software design which allows certain sections of the software, such as the logic tree, to be changed simply by modifying a data file rather than changing any of the code itself.

Both manual and voice mode interface can be used with either conventional, menu-driven (branching) logic or the less-conventional tailored logic to interact with the aircraft. The



The MAGIC Cockpit tests the integration of voice controls and image formatting.

voice response mode is being examined to determine under what conditions it is more effective than the manual response mode using multifunction control switches.

MAGIC provides expandable graphic capability, dedicating a specific processor entirely to graphics. It is possible to expand and upgrade graphic capability by simply adding circuit boards which increase the number of bit planes and colors which can be displayed at one time. Videodisc images such as terrain maps, status, systems status, engine status, emergency procedures, and tactical situation displays can be displayed "as is" or overlaid with dynamic images generated by the graphics processor.

beam Integrated Solid State program undertaken jointly by NASA and the Navy is also built on GaAs technology. NASA has also developed a 20 to 30 GHz satellite communications link using GaAs devices. The overall potential of GaAs lies in its capability for ultra high-speed A/D conversion at the multi-bit level.

The commercial follow-up on the DoD GaAs initiative has been slow, due to concerns as to the feasibility of GaAs. In comparing cost, the silicon wafer is \$1.00/in² or about \$6.00 per wafer. GaAs is \$30.00/in² or approximately \$300 per wafer. Most of its value as an IC is in its processing and packaging, not in the raw material. DoD is planning on costs to come down, as they did with silicon, when GaAs becomes more readily available.

GaAs Technology

In evaluating the transition from silicon to GaAs, certain GaAs characteristics may be questionable for military environments. GaAs is brittle and tends to be a

poor thermal conductor. Unlike silicon, GaAs is composed of two elements which may behave differently under the same environmental conditions. GaAs has no native oxide and is inherently less available than silicon.

Successful digital and analog circuits fabricated in GaAs MESFETS (Metal-gate Schottky Field Effect Transistor) hold the most promise for the military production environment. Depletion-mode MESFET devices have larger current drive capacity, a larger logic voltage and faster operating speeds. They do consume more power and are limited to medium-scale integration levels, yet may soon achieve large-scale integration densities. The depletion-mode device is less risky to construct because of its simplicity. It normally exists in an "on" state, indicating that current is flowing through it. Consequently, the device requires higher voltages for operation.

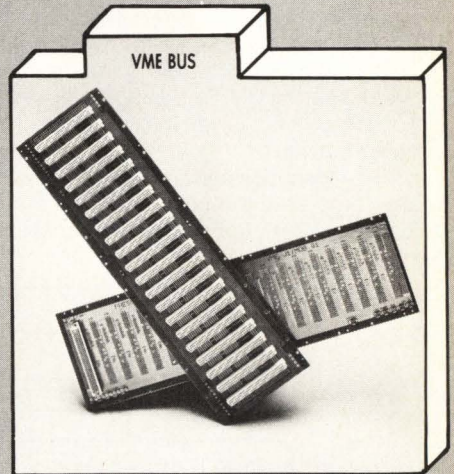
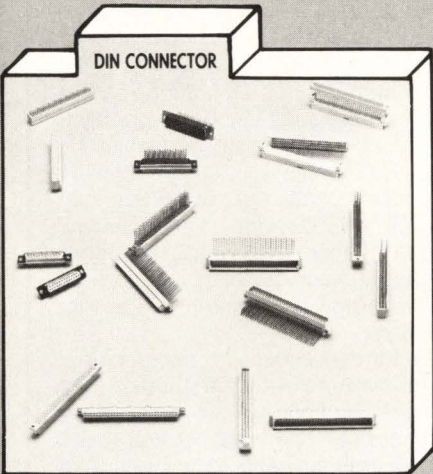
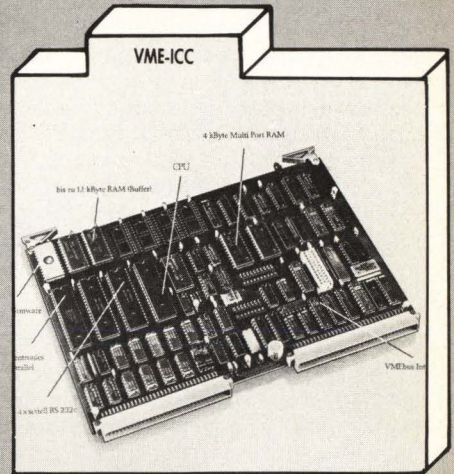
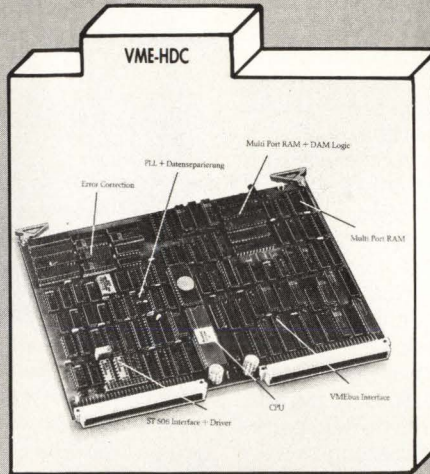
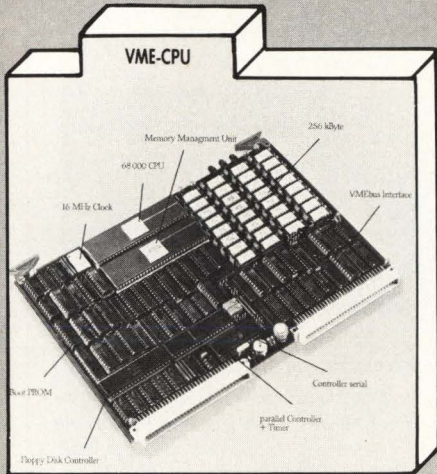
Enhancement-mode GaAs devices are more precise, yet more complicated to fabricate. The enhancement-mode de-

vice normally exists in an "off" state, as in typical silicon circuits. Less power and voltage swing is required to operate enhancement-mode GaAs circuits, thus making the job of cooling a computer system much easier. Enhancement-mode GaAs FETs have achieved LSI levels and are very near VLSI levels.

DARPA has been accepting proposals on GaAs gate array development for use in communications systems and weaponry. Private industry has been called upon to develop up to 10,000 cell gate arrays for a DARPA pilot program. DARPA's Advanced On-Board Signal Processor will require a radiation-hardened 4000-gate array. In response, Texas Instruments began by designing a 1000-gate array in a bipolar GaAs process.

In the area of memory, GaAs ICs are used to develop kilobit static RAMs for applications in space surveillance and those that require radiation hardening. GaAs ICs are also employed in high-level signal digitization at a multi-bit level resolution. Gigasample/sec analog-to-

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Adapting Commercial ICs To Military Requirements

Commercial integrated circuits have matured out of the original developmental devices of the '60s (which only the military could afford) to the point where production quantities of advanced integrated circuits are available for less than \$1.

Failures may be inconvenient in a commercial application, or a financial burden in industrial applications. Only after the technologically advanced commercial part has been demonstrated to be reliable in the commercial application, can it be applied to military or other high-reliability applications. Military integrated circuits feature tighter levels of quality control and traceability, extended operating temperature range, and environmentally secure (hermetic) packaging. All of these add to unit cost but should significantly increase the expected reliability. This is usually done without any change to the basic integrated circuit chip.

As shown in the Typical Product Flow, a single batch process produces both commercial and military integrated circuit wafers. Those wafers exhibiting the required characteristics for low and high-temperature operation, and with tighter electrical limits, are sorted out for military end-use. All IC die are visually inspected for mechanical defects with military parts being inspected to tighter limits. Hermetic packaging for military uses includes extensive environmental testing to ensure high reliability. Improved confidence in the reliability can then be obtained by burning in the IC. This is done by operating the device at a higher than normal temperature to cause any "weak links" to fail. Recently, because of warranty costs and brand reputation, even inexpensive commercial ICs are often being burned in.

Final testing is performed to assure that only quality parts are shipped to the customer. Commercial devices may be tested at room temperature only. Military devices are also

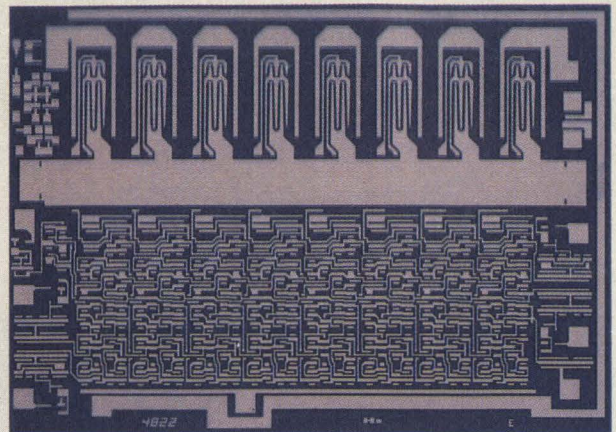


Figure 2: Example of Sprague BiMOS monolithic integrated circuit illustrating very-low power MOS logic ("smart" functions) combined with high-power "muscle" functions. This device is an 8-bit serial input, parallel output latched peripheral power driver. Each output is rated to 100 V and 500 mA for driving LED displays, incandescent lamps, thermal printheads, relays, solenoids, or other power loads.

tested at high and low limit temperatures. Depending on specific customer requirements, many combinations of operating temperature, package, reliability level, etc. are generally available.

Military hermetic integrated circuits are not without cost, however. The increased unit price is obvious. Not so obvious are the performance trade-offs. Increased operating temperature is obtained at increased leakage currents and, perhaps of most importance with today's power ICs, allowable package power dissipation is reduced.

Digital logic and low-level linear circuits are often designed for maximum efficiency (minimum power) and there is minimum difference in operation between the plastic package and the hermetic devices at normal operating temperatures. Modern "muscle" chips are now being used in commercial applications which both control significant amounts of power (> 1000 W) and must also dissipate power. In these applications, the standard hermetic device must be used at a reduced output power rating in order to obtain even a reasonable expected lifetime. Recently, because of increased required power ratings, monolithic integrated circuits have become available in flange-mount hermetic TO-3 cans for improved power dissipation in military and high-reliability applications.

Each end application has a unique set of operating conditions, design objectives, and user requirements. It is important that the designer understand the differences and trade-offs between the various levels of integrated circuits.

Consumer applications must use lowest-cost and sometimes "state-of-the-art" technologies, while commercial service requires low-cost components with reasonable life under reasonable working conditions. Military applications usually require hermetic integrated circuits for operation under severe environmental stress with high reliability, maintaining life support systems which require the highest reliability available. — F. Raymond Dewey, Sprague Electric Co., Integrated Circuit Operations, Worcester, MA

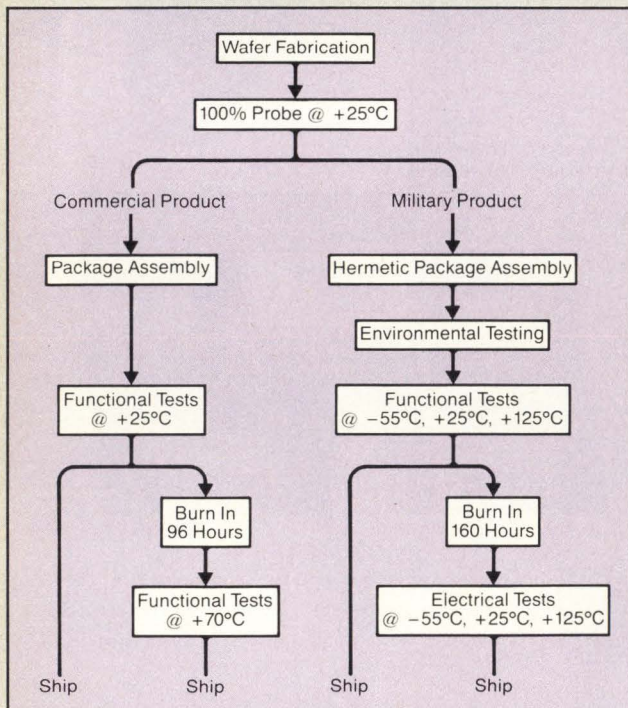


Figure 1: Simplified IC Product Flow showing four basic levels of reliability.

Write 243

digital and digital-to-analog converters are being developed by many aerospace and electronic instrument companies.

Ultimately, GaAs will offer the military electronics industry ICs capable of ultra-high speed, lower power dissipation, the ability to operate over a wide temperature range and resistance to radiation.

Strategic Computing

Advances in supercomputers have, in effect, been driven by the need for sophisticated weapons design. Issues common to all involved in supercomputer development are access problems, building the next generation, and artificial intelligence. These issues are of particular concern to the military electronics industry, as the need exists to create computers which magnify the power of strategic and tactical weapons. Defense systems must control a series of complex machinery in relatively abnormal operating environments.

Robert S. Cooper, Director of DARPA, cites three areas of development in supercomputers that will evolve. Exceedingly fast signal processors will assess imagery and real-time image understanding necessitated by advanced weaponry. Symbolic processors used as processing overlay for semantic memory will contain human knowledge allowing systems to operate autonomously. And general purpose processors will manipulate symbols, ideas, and concepts.

DARPA's Strategic Computing Program has been described by Cooper as "long and arduous" with a slated 7-10 years for mature technology to be incorporated into weapon systems. The overall goal of high-performance machine intelligence will be supported by key areas of development. Expert systems will code and mechanize practical knowledge, as well as application-specific knowledge. Artificial intelligence will facilitate speech recognition, machine vision, and natural language commands. System development environments will be characterized by simplification of rapid system prototyping and experimental refinement. Computer architectures will be enhanced by methods for using concurrence in parallel systems.

Current DARPA projects span a spectrum of performance requirements. Autonomous systems requiring human capabilities to sense, reason, plan and navigate are being built into cruise missiles, advanced undersea vehicles, and land vehicles, such as tanks. Autonomous

systems will interpret current solar and situational information to determine necessary actions for the vehicles under their control. "Pilot's Associates" are systems that would collaborate with and assist a pilot by responding to spoken commands, executing orders by drawing on specific aircraft, sensor, and tactical knowledge stored in memory. A large amount of computational power is necessary to activate surveillance sensors; interpret radar, optical and electronic intelligence; and prepare appropriate weapon systems. Battle management systems will allow military commanders to interface with weapons systems through natural language commands.

DARPA's work on high-level programming languages fostered ADA, the standardized defense language. DARPA plans at the device level may produce fabrication techniques that will allow VLSI circuits to be produced with a 3-D structure, in which circuits are placed on top of one another. Radical improvements in packing densities may be attained.

Conclusion

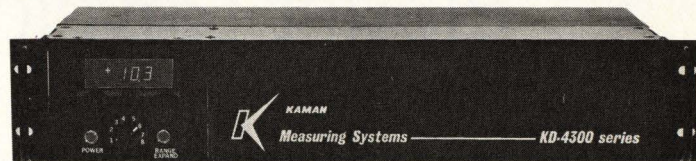
As the battlefield becomes more diffuse

and dynamic, the model of future warfare will lie in the sophistication of its electronics. Agencies such as DARPA are funding research whose results are incorporated into the fifth-generation project—artificial intelligence, parallel computing, speech understanding, and natural language programming. The Commercial-Defense support of GaAs technology has gained momentum as evidenced by Cray Research's decision to base the next CRAY on GaAs ICs. Advances in integrated opto-electronics and mosaic infrared processes will allow "staring" not scanning surveillance. The requirement of expert systems will gradually upgrade intelligence sensors, voice recognition, distributed data processing, and large data storage capabilities offering easy access. □

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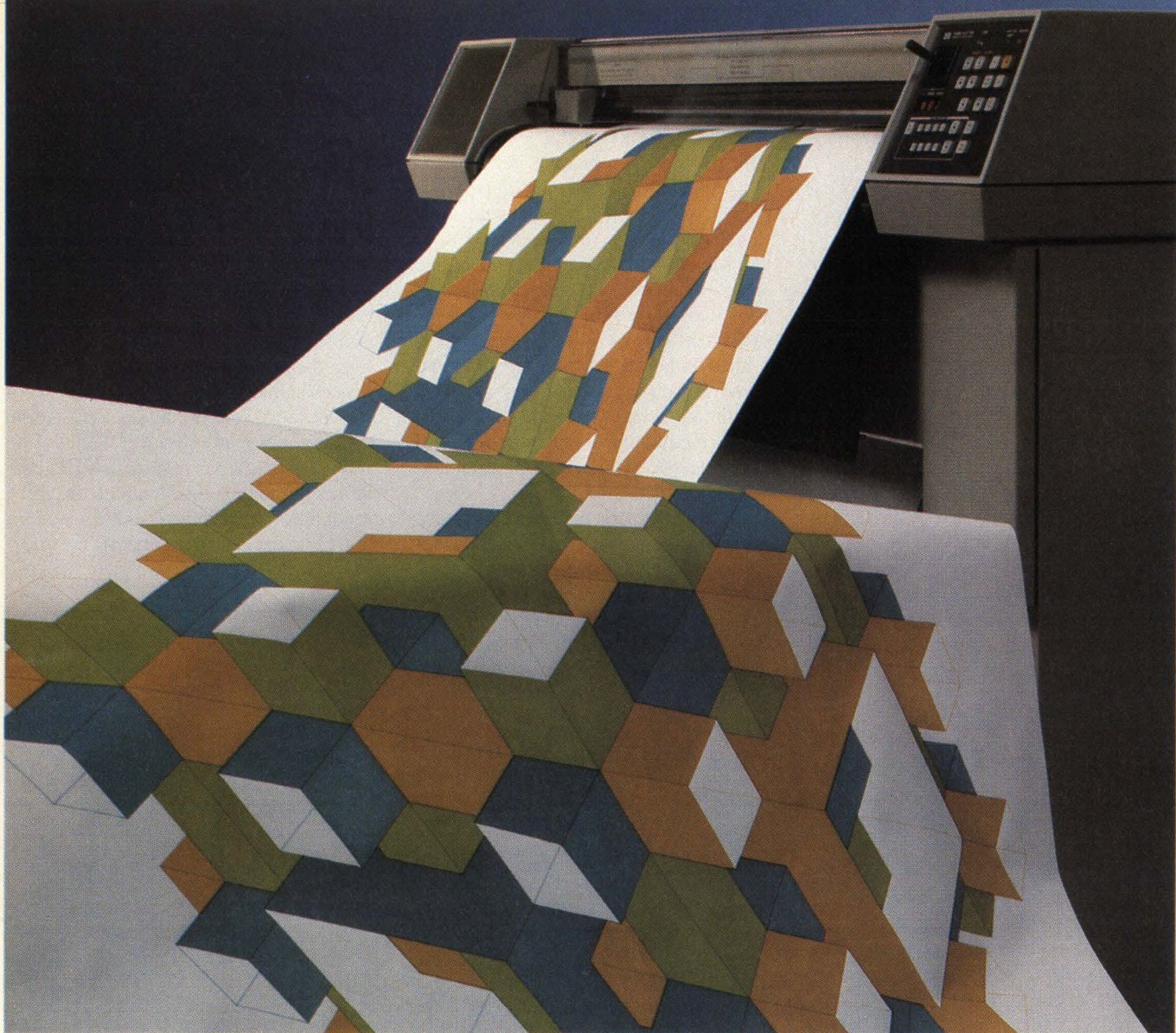


Photo courtesy Hewlett-Packard

Electrostatic and Vector Plotter Developments

by Michael Cashman,
West Coast Technical Editor

Everyone who is even remotely familiar with the computer industry knows that tremendous advances continue to be made in electronics and semiconductors, the brains and hearts of today's systems. Unfortunately, these advances tend to push developments in other important sectors of systems design somewhat into the shadows.

One such sector is the electromechani-

cal aspect of systems design, and no other device has seen more impressive progress in recent years than the graphics plotter. Clear advances have been made in simplifying designs, cutting component counts, upping performance and reliability, and making them easier to use, all while prices have moved downwards. The result is that the plotter today with the same performance attributes (plus improved reliability), costs a small percentage of what it cost 10 or even five years ago. There were no pen plotters

available for under \$1,000 five years ago; now there is a good selection, primarily for business graphics applications. Engineering-oriented units that cost upwards of \$20,000 five years ago today sell for closer to \$5,000, and top-of-the-line plotters with greater speed, accuracy and reliability are more readily available than at any time in the past. The trend is clear, the engineering community cannot do without graphics plotters, and the business systems user is increasingly willing to pay for graphics output.

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While significant improvements in performance, price, reliability, and user friendliness can be seen in all shapes and sizes, industry sizzle is clearly concentrated at the low end.

Applications Dictate Technology Choice

This article will focus on recent developments and approaches in the two most common graphics plotter technologies: vector and raster. Other evolving technologies, including ink jet, thermal transfer and others, will be the subject of an upcoming Advanced Technology Series in the July issue.

Before describing recent technological developments, vector and raster plotter technologies need to be defined, and something said about their suitability for various applications along general lines.

Vector plotters, pioneered more than 25 years ago by the company that now calls itself CalComp, are still the most common type of device. These devices generate drawings a line at a time by using servo motors to move ink pen(s) across the drawing medium (most often paper).

Raster plotters, by contrast, plot an entire raster of information across a given plotter width simultaneously, which means that plotter speed is more a function of paper movement speed than of plot complexity.

In general, vector plotters tend to provide higher throughput performance for relatively simple to somewhat complex plots, have better resolution and accuracy, and are somewhat less expensive than raster plotters. On the other hand, raster plotters can create extremely complex plots in minutes that cannot be created on a vector plotter in many hours. Fortunately, both the vector and raster plotter manufacturers are working toward minimizing the disadvantages and maxi-

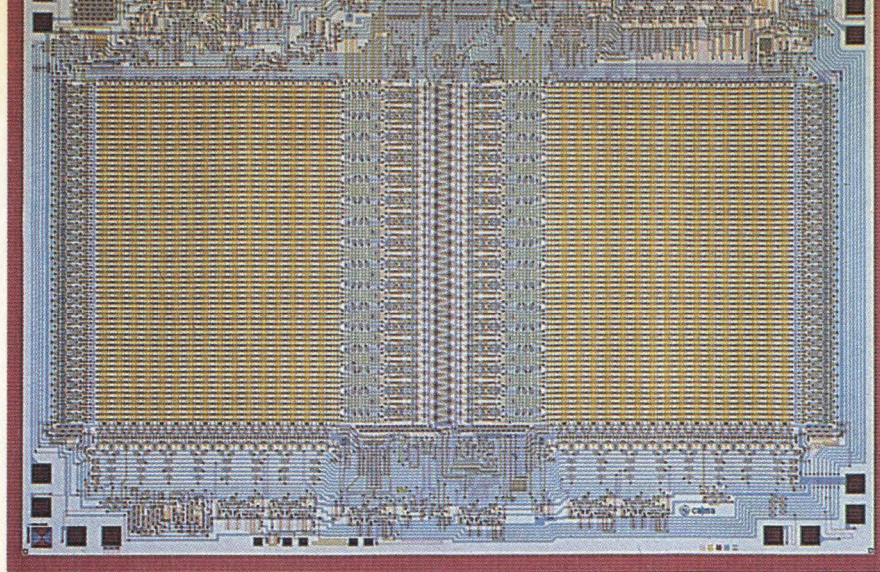


Figure 1: Circuit layouts with up to 30 million elements are easily plotted using electrostatic plotters, such as those produced by Versatec.

mizing the advantages of their respective products. Let us examine some recent efforts in these directions.

Flagship Of The Fleet

The Versatec color electrostatic plotter is acknowledged by direct (other electrostatic) and somewhat indirect (raster) manufacturers as an impressive achievement. Now approaching one year after first delivery, it is still state-of-the-art for the industry. It can generate a full color E-size drawing 34" x 44" that is dry, odorless and ready to use in eight minutes with a resolution of 40,000 points-per-square-inch.

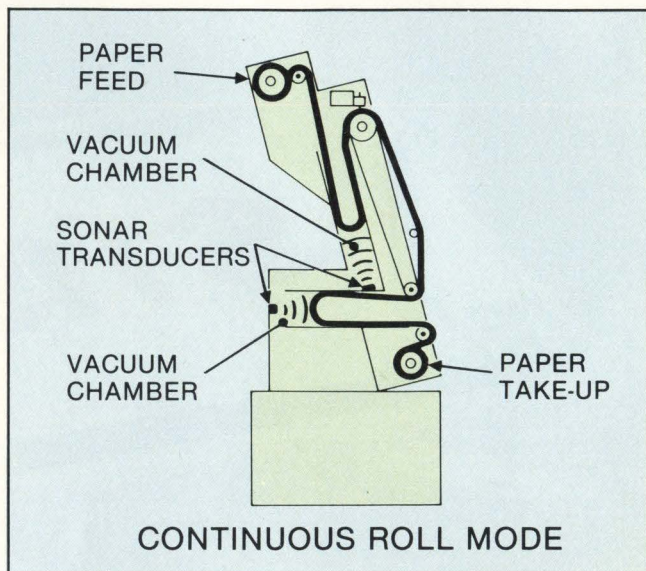
An interesting aspect regarding this plotter is how closely it is related to the black and white electrostatics that preceded it, according to Product Manager

Barbara J. O'Connell. "The electrostatic engineering community knew it was possible to get color plots by simply using different toners. The problem that needed to be solved was one of color registration for acceptable quality."

Versatec engineers solved this problem by having the plotter generate a series of rectangular marks (the internal jargon is railroad tracks) along the edge of the paper from beginning to end of plot during the first pass. The next three color passes reference these marks. Constant monitoring of the railroad track references causes subtle paper position changes.

Versatec, part of Xerox, claims to be exceeding sales forecasts for this plotter, priced at \$98,000 but with OEM discounts. It is said to be selling particularly well in CAD (especially circuit design)

Figure 2: CalComp equipped the 1070 Series Plotters with mini-sized sonar sensors at the base of the vacuum columns to determine when the paper loop in the column is too long or too short to act as a proper "buffer."



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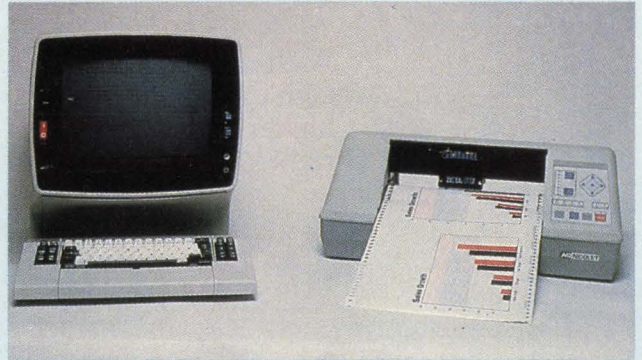
Plotter Offers Graphics Update For IBM Users

The ZETA 887 plotter from Nicolet Zeta Corp. (Concord, CA), provides IBM users with enhanced color graphics. This eight-pen, high-speed drum plotter can plot on paper, vellum, high quality glossy bond and clear inking film for overhead transparencies. Unattended plotting is done using roll or fan-fold paper.

The plotter connects directly to an IBM 3274 or 3276 cluster controller in a BSC or SNA/SDLC network via coaxial cable. It can plot EBCDIC or ASCII plot files downloaded from an IBM host computer and can operate on-line, off-line or remotely via communications lines.

Two 16-bit integral microprocessors provide on-board intelligence. The ZETA 887 is also supported by a wide range of software packages.

Write 300



The ZETA 887 and IBM cluster controller.

and for use in geophysical exploration. Several semiconductor houses which use this plotter were contacted and were impressed with the plotter; both with its technological achievement and the price. They claim the color capability greatly facilitates the optical checkout of circuit paths, so Versatec's claim that one semiconductor house discovered an error in a circuit plot that had defied detection for a year seems reasonable.

Versatec's O'Connell is sanguine about the future of color electrostatic devices in particular. "The trend is toward greater

complexity. The CAD industry today is generating plots containing from eight to 20 million elements, (Figure 1) and the demand will soon be for the capability to handle 40 million. The color electrostatic type plotter seems the only reasonable choice when talking about designs of this magnitude. Our research indicates that 85% of CAD and geophysical users want color plotting."

The acceptability of the Versatec color electrostatic is being watched closely by traditional competitors. A spokesman at Benson (which acquired Varian's electrostatic printer plotter operation) implied that Versatec may not have this market to itself for long. "Give Versatec credit; that machine is a breakthrough product, but it's still a 200 dots-per-inch machine. Potential customers are telling us that they need 400 points-per-inch, and they want it at one-third the price of the Versatec product. I think you'll see a product like that in the near future."

Electrostatic Plotters

It may be that electrostatic plotters will always be more expensive than vector plotters, but their developers have not yet given up on the challenge. A way to lower the printing head costs of the machines is still being sought. If these products are to overcome their accuracy inferiority to vector plotters, more writing heads must be used, and heads make up a considerable portion of overall systems costs. One vendor stated that advances in robotics

may lead to significant reductions in the costs associated with manufacturing of plotter heads.

Versatec has also introduced 400 dots-per-inch capability in its new 7000 Series monochrome plotters. It operates at 4 ips and is rated at a maximum accumulated horizontal and vertical plot error of $\pm .15\%$. Quantity one for the 7436 is \$44,000 with first shipments slated for this month.

Another nagging problem mentioned by the electrostatic manufacturers was that of paper. Paper has water content that can and does vary, and not necessarily evenly or along the X and Y dimensions, or by batch. Versatec says that it now recommends a conditioned atmosphere like that of a DP center for its color electrostatic plotter. Benson states that it is constantly working with the paper manufacturers on paper quality improvements. (It should also be noted that there are problems with film stretching, for the same fundamental reason.)

Both major electrostatic plotter vendors cited the potential for microprocessors and decreasing memory costs to decrease vector to raster conversion costs.

Vector Plotters

While electrostatic plotters continue to make tremendous advances, it is a fact that the great majority of images to be plotted are not as complex as those which electrostatics can plot with ease. The greater accuracy of vector devices, coupled with low cost units quite suitable for business and some scientific uses, help explain why many times more vector plot-

(continued on p. 119)



Figure 3: The Hewlett-Packard 7550A may be the first plotter to break the 4G acceleration standard.



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PRODUCT INDEX

To help you find the products that you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

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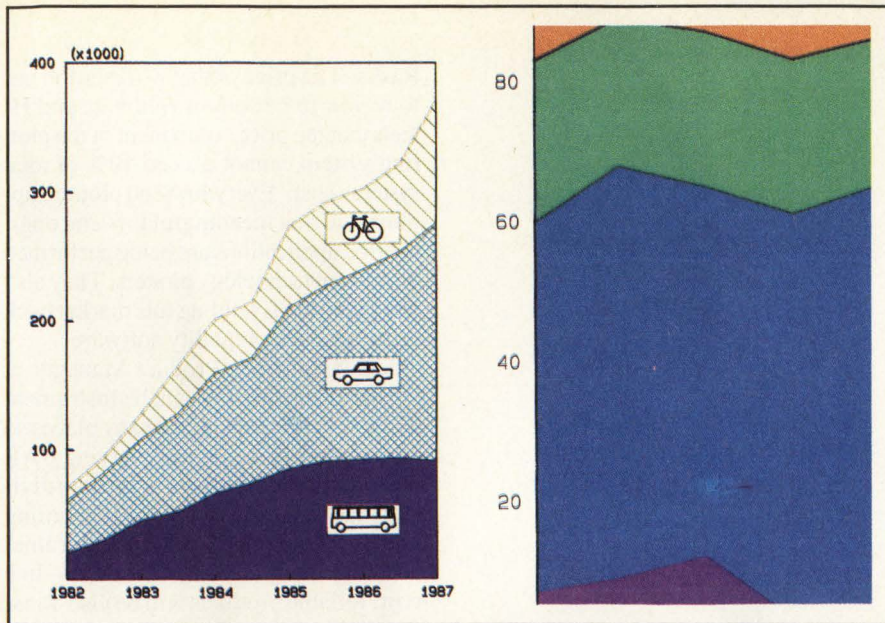


Figure 4: These original plots were generated on the Hewlett-Packard 7550A.

(continued from p. 112)

ters are being sold today than electrostatic devices. Clearly, the vector plotter engineers have not been standing still.

The High-Accuracy, Engineering Oriented Marketplace

This is the marketplace that was pioneered by a company that started out as California Computer Products more than 25 years ago. As in most viable marketplaces, customer demands for additional capabilities caused separate product lines to evolve, which is also true for other vendors. Though it offers low-cost business graphics devices, CalComp, now part of Sanders, still focuses heavily on the high-accuracy engineering-oriented marketplace. Here is an example of how customer requirements can lead to a product that increases the competitiveness of the vendor through the use of innovative engineering approaches.

Market research told CalComp that 30% of its users felt restricted in having to choose between a cut sheet plotter and a continuous-roll plotter. The toughest technical problem facing the engineers in developing what would become the 1070 series of combination cutsheet/continuous-roll plotters was accurate paper tracking. One aspect of the problem was solved by borrowing the grit wheel approach taken by Hewlett-Packard several years ago for products oriented toward this same marketplace. The solution of another aspect of the problem is a little more intriguing.

Conventional continuous roll plotters use optical sensors in the vacuum columns to determine when the paper loop in the column is too long or too short to act as a proper "buffer." When the sensor determines that one of these conditions exists, it activates servo motors to feed to take-up paper as needed. The design of the combination cutsheet/continuous-roll plotter required a shortened paper path that was insufficient to serve as a buffer. Optical sensors simply couldn't determine the length of the paper loop quickly or accurately enough.

The solution to this problem came from, of all places, the Polaroid SX70 camera, which uses sonar as the basis of its automatic focus feature. Sonar sensors were installed at the bases of the two vacuum columns (Figure 2). Not only did this approach solve the remainder of the paper tracking problem, the sonar sensors have the additional advantage of not being affected by differences in the opacity of different plotting media. As a bonus, the sonar sensors are cheaper and are said to be more reliable than their optical predecessors. Both Nicolet Zeta and Hewlett-Packard have introduced combination cutsheet/continuous-roll plotters into their respective product offerings.

This serendipitous engineering solution fits in nicely with what OEMs are demanding, says Trevor J. Lee, the 107 X Product Manager at CalComp. "OEMs are demanding more simple devices.

They want no more sophistication than that which is absolutely required to provide the performance level required." This was an observation made by most vendors interviewed.

Both CalComp and Nicolet Zeta said that users and OEMs are demanding a greater number of connectivity possibilities for their products. "Customers want the accuracy of these high-performance products, but increasingly they want to tie them into resource sharing networks," according to Bill Manos, Product Manager at Nicolet Zeta. This quickly turns into a software protocol problem that these vendors are moving to solve by expanding their involvement with software.

Hewlett-Packard invaded the high-performance engineering-oriented marketplace several years ago and is very competitive with a complete vector plotter line. The grit wheel paper guiding approach taken by H-P with its 7580 line strongly motivated the competition.

As a complement to the 7580 product line, H-P has just introduced a particularly interesting product. The 7550A (Figure 3) is a desktop eight-pen 11" x 17" device with 31.5 ips performance and 6G acceleration. This plotter may be the first with automatic cut-sheet paper feed, and is almost certainly the first unit capable of generating up to 99 copies automatically and unattended (Figure 4). While these capabilities sound like the features of a business plotter, H-P feels that the 7550A will find use in a large number of CAD and other engineering applications. The quantity one price of \$3,900 makes this product a strong contender for engineering workstation duty. The interfaces are HP-IB (IEEE-488) and RS-232-C/CCITT V.24.

Both H-P and CalComp say that the trend toward easier to use, relatively high-performance, high-accuracy devices will be the key that unlocks a potentially large but virtually dormant market. Almost everyone assumes that almost all architectural firms of any significant size use graphics plotters routinely. The plotter vendors say otherwise. "When the price falls below \$15,000 for a user friendly product that doesn't require a dedicated on-site guru to run it, that market will take off," says Bryan Butler, a Retail Sales Development Manager at H-P.

The Low-End Marketplace

Color electrostatics and high performance vector plotters may be intellectually

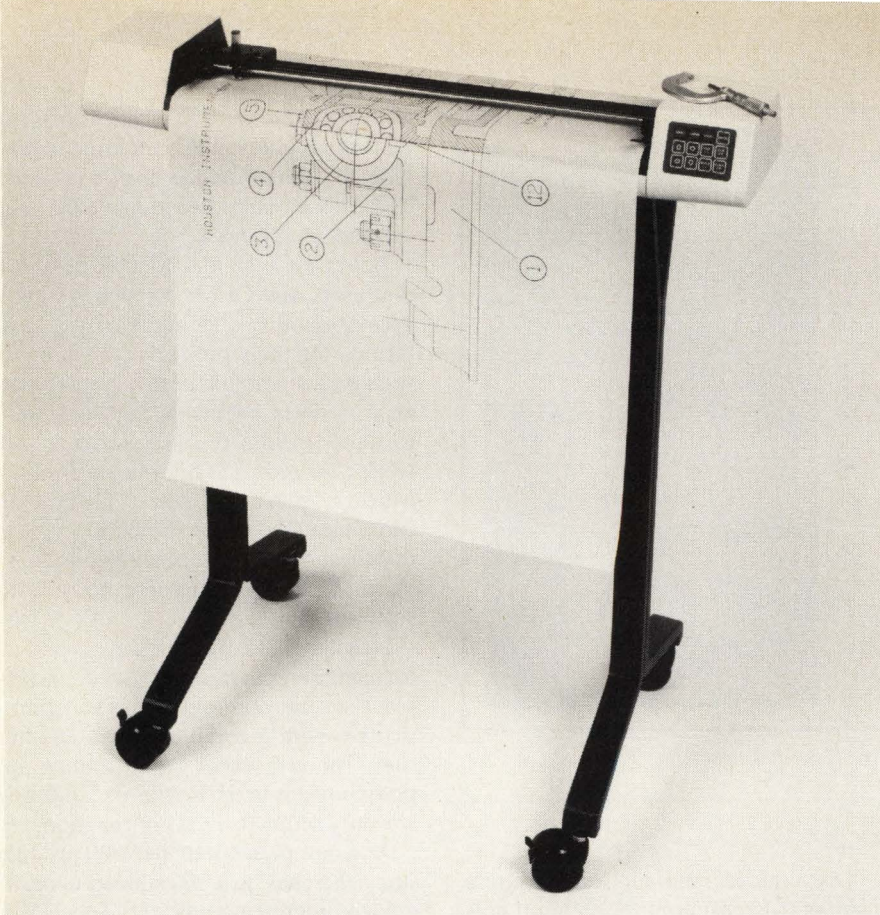


Figure 5: The Houston Instrument DMP-51 features 22 IPS performance, 4G acceleration, 26 Kbyte of built-in intelligence, and a resolution of .001".

fascinating, but it's the "bottom lines" vendors with products costing less than \$5,000 (and sometimes under \$1,000) which seem to be having the most fun these days (Figure 5). Inside Hewlett-Packard's Rancho Bernardo (near San Diego) plotter manufacturing facility can be seen hundreds of low-cost plotters ready for shipment.

Reduced Parts Counts

"The 'secret' to offering low-cost, reliable products that a vendor can proudly put its name on lies in reducing part counts," say H-P's Bryan Butler and James J. Raska, Products Manager at Houston Instrument. An example of this given by H-P is that its 7470 two-pen graphics plotter contains only one-fourth the number of parts of its immediate predecessor. When these types of reductions can be made, features that were previously limited to higher-priced/higher-performance products tend to migrate downward. This would include user-friendly software and features like pen capping, etc. For example, the aforementioned H-P 7470 features a one-piece platen, a one-piece pen carriage, and requires no manufacturing or field adjustments. Designing for low-

power consumption makes it possible to do without a fan, for example.

Houston Instrument's Raska sees the importance of parts count reductions in another way. "In this hotly contested low-end marketplace, an hour of manufacturing time can defeat one's best efforts. It's not enough to design the product with a lower parts count, it has to be designed from the outset to be as easy and quick to manufacture as possible."

New types of products often necessitate new manufacturing and testing methods as well. H-P, for example, has gone to "strife testing" its low-end products. Strife testing is applied to components during the design process and selected units coming off the manufacturing line are required to cycle through 0°-100° C "desert to arctic" conditions.

Toward The Engineering Workstation

Is there a place for a relatively inexpensive and relatively low-performance on plotter on the evolving engineering workstation? Every vendor interviewed said yes, but some vendors think that low-end means a \$10,000 plotter. "That isn't what we're seeing," says Houston Instrument's

Raska. The price of that workstation has to be low to be sold in volumes, and HI feels that the price component of the plotting system cannot exceed 50% of total systems cost." Every low-end plotter supplier said that meaningful low-end engineering applications are being performed on current technology plotters. They also feel that what is holding this market back is the absence of quality software.

Jack Campbell, Product Manager at Western Graphtec (Watanabe Instrument Corp.), states that his company places so much importance on the evolving CAE market that it has formed a separate division. He sees the product really coming into its own in the 1985-1986 timeframe, and that companies without very low cost, reliable products will be also-rans.

The Software Problem


Finally, the software aspects of the graphics plotter market must be addressed. "Systems end users are hungry for color graphics. They have them on their system CRTs; they seem unwilling to go to non-color for the hardcopy," says Western Graphtec's Campbell. "It is the sophisticated information processing software packages that are selling the plotters, packages like Lotus 1.2.3 and Context MBA. It's up to the plotter vendors to ensure that these package developers are supplied with the software drivers for individual devices." As usual, the Europeans were cited by several vendors for pushing standardization efforts.

Western Graphtec's Campbell feels that much has to be done before the plotter becomes anywhere near as popular as the system printer. "Stores, for example, don't like to stock plotters, and sales personnel don't like to demonstrate them. These products are intimately tied into the software capabilities of systems, and sales people say they don't have the time to learn the packages. But I feel this must and will change."

The constant improvement in design and engineering of graphics plotters in all performance categories will assist in this effort. □

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Photo courtesy Stratus Computer

New Architectural Designs Push Fault-Tolerance Into The Market

by Dave Wilson,
Senior Technical Editor

Although the concept of fault-tolerance has only recently attracted wide publicity, the idea has been around since the design of the first computer system. Many people believe that the ENIAC was the first stored computer built in the U.S., but its predecessor, the BINAC, was designed specifically with high reliability in mind. Built with continuous checking of two identical processors, its purpose was to carry out ballistic calculations for the

military. Unfortunately for its designers, the individual processors used for the BINAC were built with vacuum tube and relay technology and each of them had a mean time between failure of seven minutes. Although this design was not very practical, it does indicate an early recognition of the need for reliability. Today's fault-tolerant machines may be divided up between those that are suited for the commercial or business environment and those that are used in industrial environments such as process control.

On-Line Systems Market

The majority of the recent introductions have been aimed at the on-line systems marketplace. This market has emerged as one of the largest and fastest growing segments of the computer industry. There is a trend to move away from batch processing to on-line, interactive processing, particularly in applications that consist of numerous transactions that must be processed quickly and accurately. This trend is fueled by the needs of many businesses to improve profitability in the face

of inflation and increased competition in their markets.

The needs of this on-line transaction processing market place a unique set of demands on the computer systems architect, since transaction processing applications have characteristics that distinguish them from other types of computing, such as small computational tasks. One critical requirement is computer systems reliability. Users who need continuous and instantaneous access to large information files typically need it 100% of the time. Any system failure, no matter how brief, can result in serious financial losses and organizational chaos. Because continuous availability is important to on-line systems customers, another requirement is for on-line maintenance. Systems must be serviced or parts replaced while processing continues. A third critical need in the on-line environment is for data integrity, both in the individual

Today's fault-tolerant machines may be divided between those suited for the commercial or business environment and those used in industrial environments.

transactions and throughout the network that is frequently part of an on-line processing system.

To meet the demands of the above criteria, many designers have proposed and implemented advanced forms of multiprocessor systems. One notable feature of some machines includes dynamic load balancing across a number of processing elements. This sort of architecture, although expensive by present day small-systems standards, will inevitably emerge at the low-end, endorsing many analysts' claims that by 1990 fault-tolerance will be everywhere.

Unfortunately, in the UNIX world, this implies rewriting the operating system kernel to support a number of processors working concurrently. However, the obvious advantage of being able to add processing power incrementally to a system (irrespective of the fault-tolerant issues) is undoubtedly the driving force behind many current designs.

Take, for example, the recent announcement from start-up Flexible Computer Corporation (Dallas, TX) who plan deliveries of their Flex/32 system by next year. Able to support up to 10 32-bit NSC 32032 microprocessors operating concurrently the system will be targeted towards OEMs with real-time applications.

Sources of Downtime

There are many sources of system downtime. The figures given in **Table 1** for typical sources of unscheduled downtime for transaction processing systems were derived from a paper presented by Stephen Jones of Synapse at the 26th IEEE Computer Society International Conference in 1983. The exact numbers vary widely among installations due to differences in hardware, maintenance, software, and operations.

From these figures, it is apparent that downtime related solely to the CPU is extremely low. Furthermore, it may seem

Software	30%
Human Error	20%
CPU	15%
Other Hardware	25%
Environmental	5%
Other	5%

Table 1: Sources of system downtime.

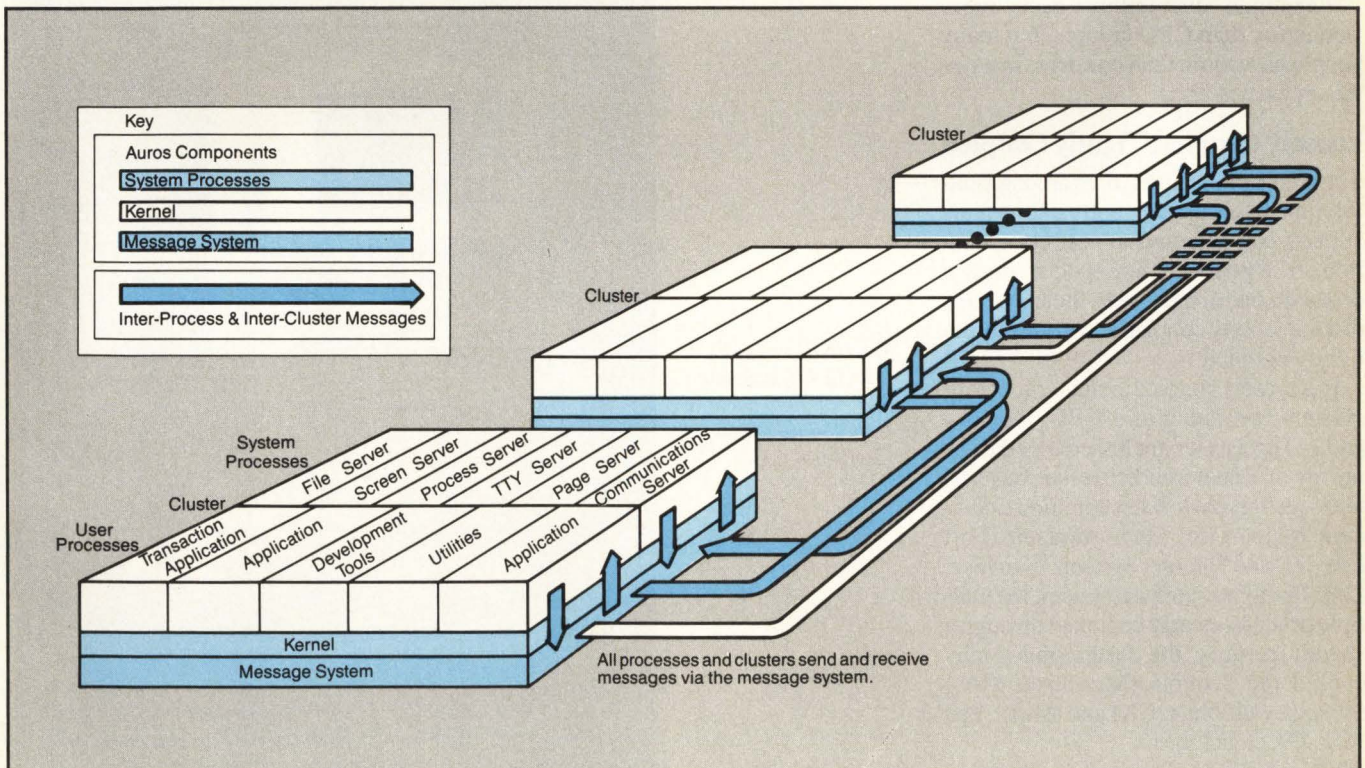


Figure 1: AUROS Interprocess and Intercluster Communication.

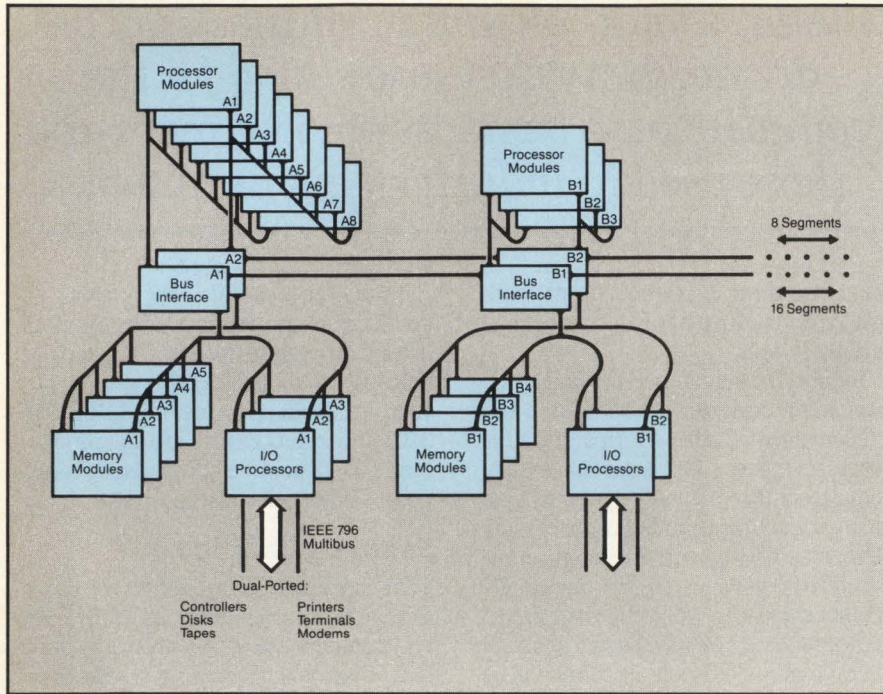


Figure 2: Architecture of the Sequoia Computer.

strange that many designs go to such lengths to back up the CPU in case of failure. It must be realized, however, that the issues of fault-tolerance are related less towards *what* piece of a system fails most often, but towards the *cost* (in time and money) to the user should that piece fail. For example, disk failures occur more frequently than CPU failures, but many people have more than one drive in a system anyway.

Loosely Coupled/Tightly Coupled

The architectural differences among fault-tolerant machines currently on the market defy any attempts at neat classification. It is possible, however, to draw a broad distinction between those systems that are loosely coupled and those that are tightly coupled.

In a loosely coupled system, processor clusters consisting of a CPU, memory and I/O processor are linked together by means of a dual interprocessor bus system—an approach that is common to Tandem (Cupertino, CA), Auragen (Fort Lee, NJ) and Tolerant Systems (San Jose, CA). In a tightly coupled system, the multiple processors may be linked through a shared memory, the design philosophy behind the Sequoia (Marlboro, MA), Synapse (Milpitas, CA) and Arete (San Jose, CA) machines.

Loosely coupled systems do not incorporate redundancy at the CPU level. In-

stead, each processor is kept in communication with the others across the dual interprocessor bus. If one processor fails, its workload is taken over by the remaining processors.

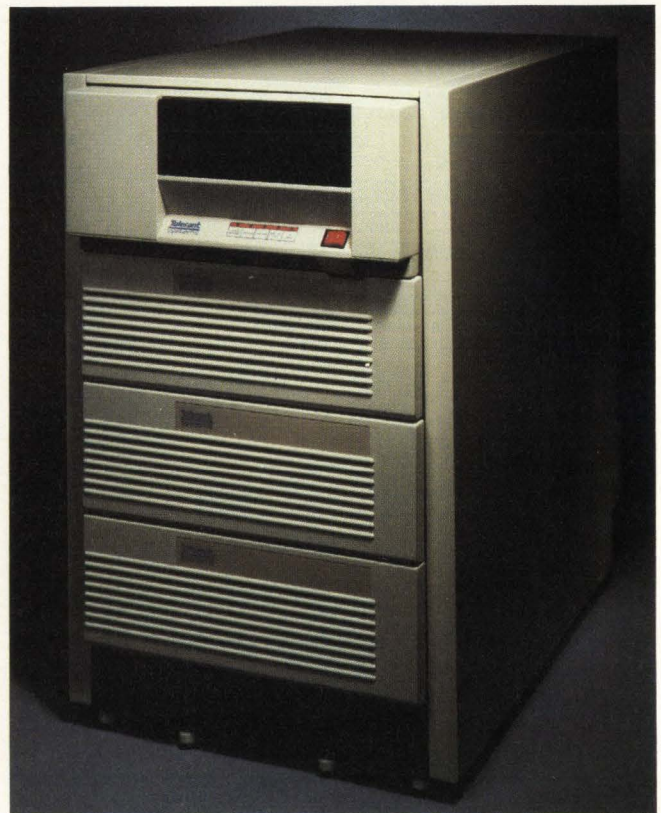
The entry-level Auragen system has

two processor clusters. Each cluster consists of an executive processor module, a word processor module and a 1 Mbyte memory module. A processor cluster can be expanded to contain up to four disk/tape processor modules, a maximum of four communications processors and up to 8 Mbytes of memory. A copy of the operating system, in Auragen's case AUROS (compatible with UNIX System III) runs in the executive processor of each cluster. The message system, which is part of AUROS, automatically creates a backup copy of every executing program. The backup does not execute, it simply receives and saves messages sent by the message system. These messages contain the same information that was sent to the executing primary process. If the primary fails, the backup can recreate and continue the work of the primary by processing its stored messages.

The message system also ensures that when a backup process begins executing, it does not resend any messages already sent by the primary. In this way, the backup hardware can do productive work during normal operation, because the message system only uses a minimal amount of system resources to manage messages for backup processes.

Spreading the workload over several processors so that multiple instruction and I/O processing operations can be

The UNIX-based Eternity 32-bit supermini fault-tolerant machine from Tolerant Systems (San Jose, CA).





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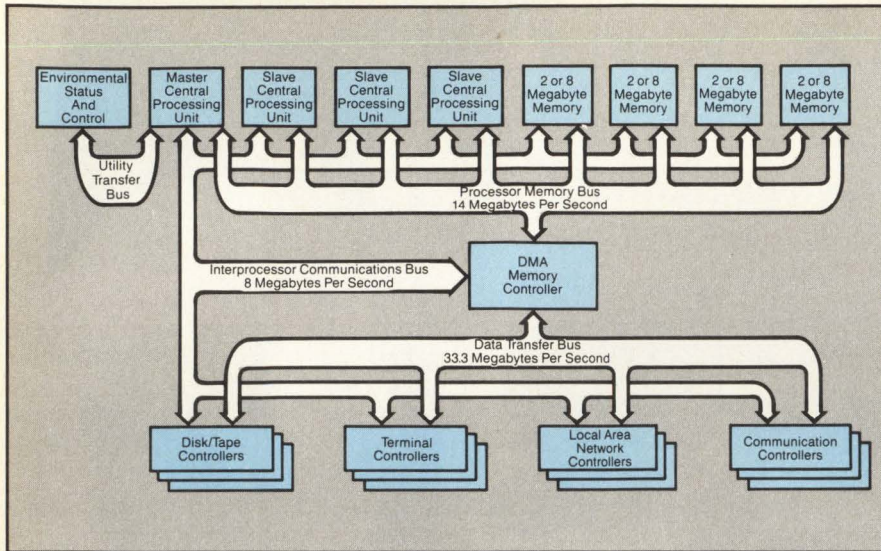


Figure 3: Systems Block Diagram of the Arete 1000 machine.

performed concurrently is also the rationale behind the Tandem design. Like Auragen, the operating system (in Tandem's case Guardian) is distributed across all the processors in the system. The Guardian operating system provides continuous operation through the operation of fault-tolerant process pairs. The primary process is the active program. The backup process is a passive copy of the primary process and resides in a different processor. Before performing any critical functions such as updating a database, the primary sends its backup process a checkpoint message. The message contains the data and processor status information the backup needs to complete the function should a failure occur.

The second class of modularly expandable multiprocessor systems link the processors together through a shared memory. This design approach is possibly the method best suited for load balancing, because at any given instant in time at almost no cost to the user, a program can be moved from one cluster to another. This is in contrast to the loosely coupled architecture where a program is committed to a cluster and to move it, the entire memory must be copied from one cluster to another.

The drawbacks of the shared memory approach include contention for the re-

source by a number of processors and the fact that memory becomes a single point of failure in the system. One way around the contention problem is to locate a cache memory in front of the CPU. In the Arete 1000 system, for example, each CPU has its own 4 Kbyte cache memory. This allows the CPU to run faster and since many memory accesses come from the cache, traffic across the processor memory bus is greatly reduced.

The recognition that not all data are required by all of the processors and their executing programs, led Synapse to improve the typical cache write-through technique. In a write-through operation, any write to a local cache results in the updating of main memory at the time of

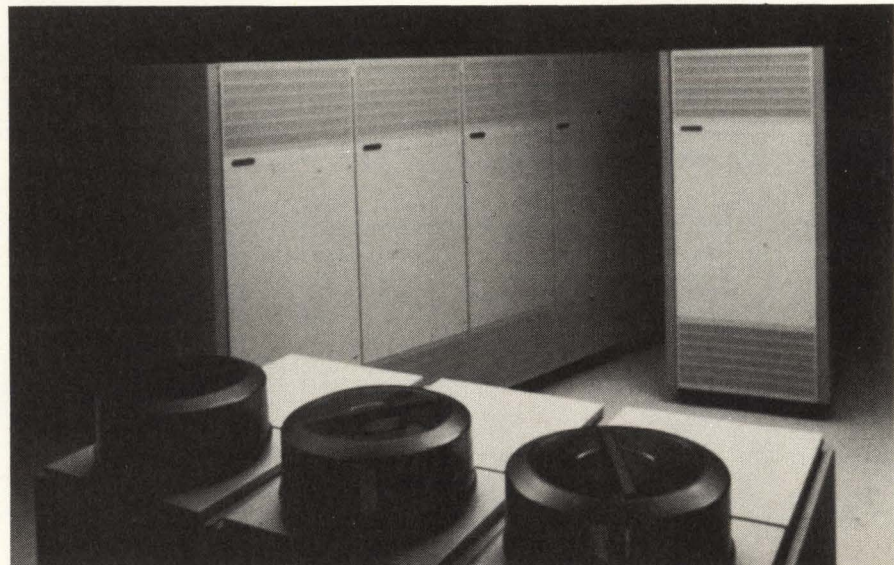
the write. Synapse uses a proprietary method to reduce the write-through traffic by assigning a usage mode to words contained in cache and main memory. If the mode dictates that there is no need to perform write-through because of the local usage nature of the data the main memory copy is not updated, resulting in a significant decrease in main-memory system usage.

By use of unique partitioning of the memory in a design, shared main storage as a single point of failure can be minimized. On the IPL 4480 machine from IPL Systems (Waltham, MA) main storage is partitioned into 16 independent storage modules, each with two parts. Either part can fail without affecting the other part and any storage module can fail without affecting the others. Moreover, in the event of a storage module failure, the operator can bring on line the active spare module without waiting for the field engineer.

Unique Architecture

Although it also uses a tightly coupled approach the design methodology adopted by Stratus Computer (Natick, MA) is unique in the fault-tolerant marketplace. The Stratus CPU system component, for example, contains two sets of identical circuitry that perform every operation. The system component is itself duplicated and the two operate in parallel. If the checking logic detects a component malfunction, the failed board is automatically removed from service before erroneous processing occurs or before data is corrupted.

In the original member of the Stratus/32 family, the FT 200, the CPU *itself* is



One of the latest entries into the fault-tolerant market is from Sequoia Systems (Marlboro, MA).

comprised of two 68000's, because information placed on a single 68000's stack is not sufficient for the same processor to recover from bus faults, although a second processor can do so. Both of the latest Stratus designs, the XA400 and the XA600, make use of the 68010 which permits the design of a complete single processor virtual memory system. To the user, of course, the FT200 machine effectively has only one processor, while the XA400 employs four and the XA600 six. In the XA models each logical, independent processor is capable of running a different program.

Some unique features of the XA600 include a standard hardware arithmetic processor that is located on the boards with the 68010 that processes commercial instructions and provides IEEE floating point operations. It has been microcoded to handle commercial arithmetic and trigonometric functions. Each XA600 processor is accelerated by a dedicated high-speed cache. Stratus claims that the largest performance benefits derived from the cache will be done to programs with compact, frequently used data items and small instruction loops.

Conclusion

Aside from the architectural merits of a particular design, there are some important issues critical to the understanding of which market is most appropriate for a particular fault-tolerant vendor. For example, is it possible to automatically add a new processor and get that much incremental system performance without manual load balancing, file splitting or comprehensive returning? Can high database performance be achieved without sacrificing the ease-of-use demonstrated by the newer database technologies, i.e. relational DBMS? Does the user have to specifically code database integrity and system recovery scenarios? Does the fault-tolerant vendor provide application development tools that significantly accelerate development of systems within a particular target industry?

In five years all computer systems will have a degree of fault-tolerance. Newer vendors must bring a great deal more to the marketplace than fault-tolerance itself to achieve staying power.

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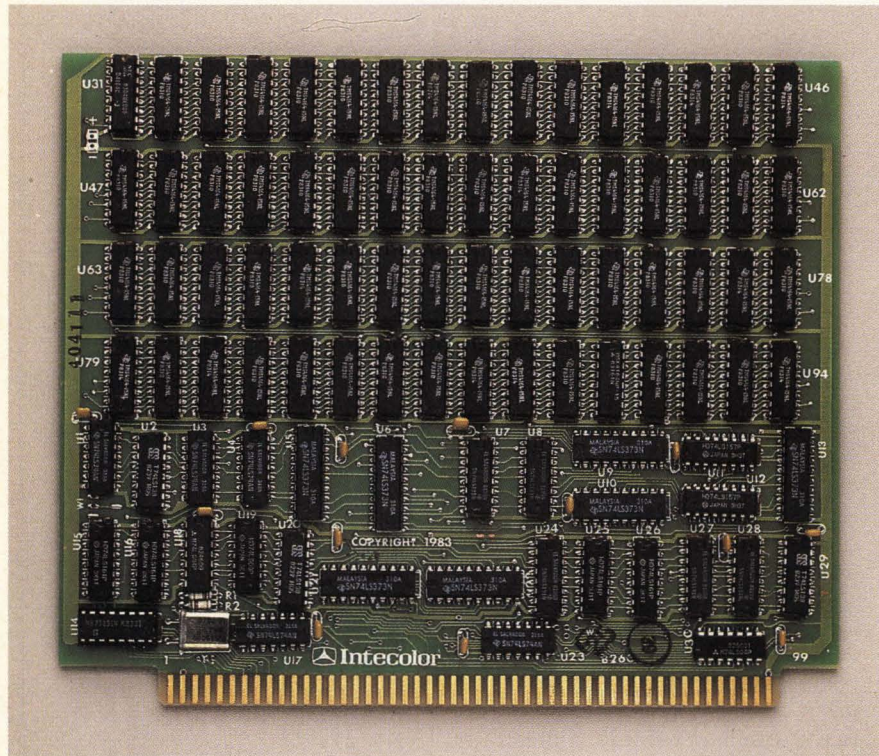
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Making Fast Faster: The Design Of A Small Graphics System Enhancement



by James R. Coyle

It is widely accepted that color terminals are important because they permit more information to be displayed and understood by an operator than monochrome terminals. One major market for displays is control industries whose product performs constant monitoring and management of a process.

In process control, taking immediate action when a chemical interaction starts going astray can save a lot of money. Though color terminals became popular in the early 1970s, the market wanted terminals to handle information faster, with a way to put up a new screen in less than two seconds. As one of the first to bring color terminals to the marketplace, Intecolor had a large share of the control market. With an installed base of more than

The FastScreen board RAM disk improves screen redraw for Intecolor's 8001 series color graphics terminals as much as three times.

25,000 model 8001G color terminals that could be used even more effectively if faster screen updates were possible, a search began for ways to speed up the 8001 series.

Technology For Speed

At about the same time that the control market needed faster color terminals, RAM disks were invented. The RAM disk is a disk drive emulator that solves the problem of wear and tear suffered by mechanical disk drives. Unlike conven-

A new board designed to speed up terminals with a large installed base is worth the effort in meeting users' demands.

tional disk drives, it also is relatively immune to extreme temperatures, dirt and vibration. It uses additional computer memory as a temporary storage area for information. Its major advantage is its ability to speed up access to information.

When implementing RAM disk technology in Intecolor products was first considered, the only available design was for the S-100 bus, with the complete system fitting on one 5"×10" card. The 8001 terminals used 6"×8" circuit boards. Redesigning the layout to fit on the smaller board was the most difficult part of the development of Intecolor's RAM disk. This problem was compounded by a need for additional features to make the system really useful to the control industry.

The original RAM disk design being converted to a smaller card was based on the Z80 microprocessor. The 8001 series used the 8080A, and in light of the large installed base of 8001G color terminals, the RAM disk itself, as well as the board it was mounted on, had to be completely redesigned.

James R. Coyle is manager of marketing services for Intecolor. Prior to joining Intecolor in 1977, he worked for Factory Mutual Engineering. He holds a BS degree in electrical engineering from Florida University.

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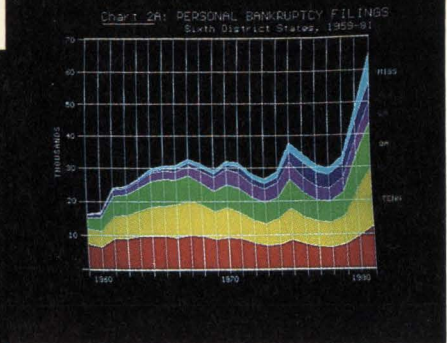
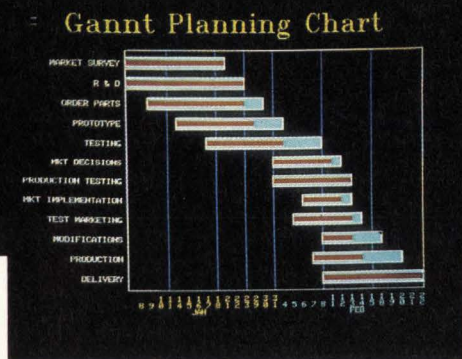
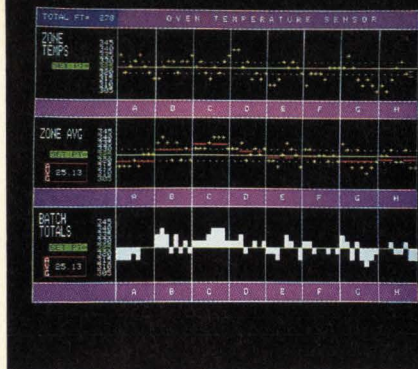
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Circuit Details

The complete design includes a 512 Kbytes dynamic type read/write memory (RAM), a set of programmable counters which generate the memory's addresses and a control system that coordinates all the functions involved in memory operation, including the periodic recharging or refreshing of the memory's storage cells required for the maintenance of its data.

The memory is organized as eight banks of 64K eight-bit registers. Each bank has eight type 4164-15 integrated circuits. The 4164-15 contains 65,536 storage cells whose organization can be represented as a two dimensional matrix having 256 rows and 256 columns. An eight-bit address is required to single out a row; another eight-bit address is required to single out a column. So, a total of 16 bits are required to address a single cell.

The 16-bit cell address is furnished to the 4164's eight address terminals as two successive bytes. The first byte is accompanied by a strobe signal that enables the chip's row address decoder. The row address strobe remains present while the second byte is furnished. This byte is accompanied by a second strobe signal which enables its column address decoder. Data is read or written while the column address strobe is present, according to the state of the chip's write enable line.

A bank of 64K eight-bit registers is formed by connecting the address, strobe and write enable terminals of eight 4164s in parallel and forming two eight-line data buses with the read and write lines from each chip. Accordingly, a 16-bit address picks eight cells (one in each chip) simultaneously.

The complete array of eight banks is formed by tying the address and data buses of each bank in parallel. In addition, the row address strobe and write enable lines to each bank are effectively in parallel.

The memory's read data bus is routed

to the inputs of an octal latch, and the outputs of this latch are connected to the Intecolor system data bus. The memory's write data bus is tied to the outputs of another octal latch. Latches are enabled at the proper times by signals from the control circuitry.

The main address counter consists of four latches connected in cascade. This counter provides a 19-bit memory address for each read or write operation. The lower 16 bits of the address single out a register in any bank by specifying a row and a column. The upper three bits single out the proper 64K bank by determining which is to receive a column address strobe.

Prior to reading or writing a block of data, this counter is loaded with a starting address by the system processor in a series of three I/O write operations.

Three examples of output from the Intecolor FastScreen.

When reading or writing, the counter is incremented by the master column address strobe at the end of each read or write operation. A continuous sequence of memory addresses is produced corresponding in length to the number of bytes being read or written.

A crystal controlled oscillator functions as the RAM disk's timebase generator. The oscillator's output (9.619 MHz) is buffered and inverted, providing clock signals for a frequency divider/pulse counter and gating signals for a decoder. Output from the counter is used directly to clock refresh.

The refresh clock signal marks the limits of the RAM disk's basic operating cycle. This cycle occupies a total of 64 periods of the clock oscillator, about 6.4

Intecolor's 8001 series color graphics terminal showing a typical screen display.



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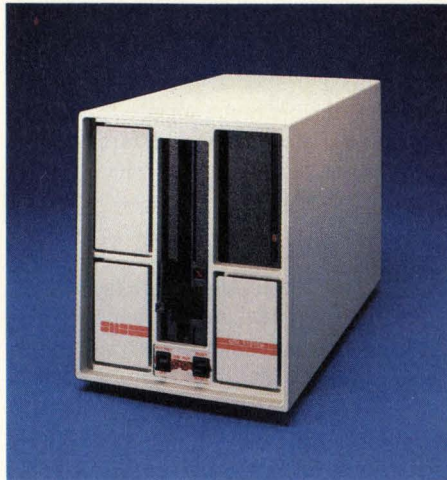
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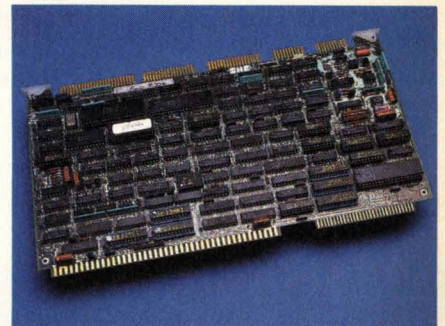
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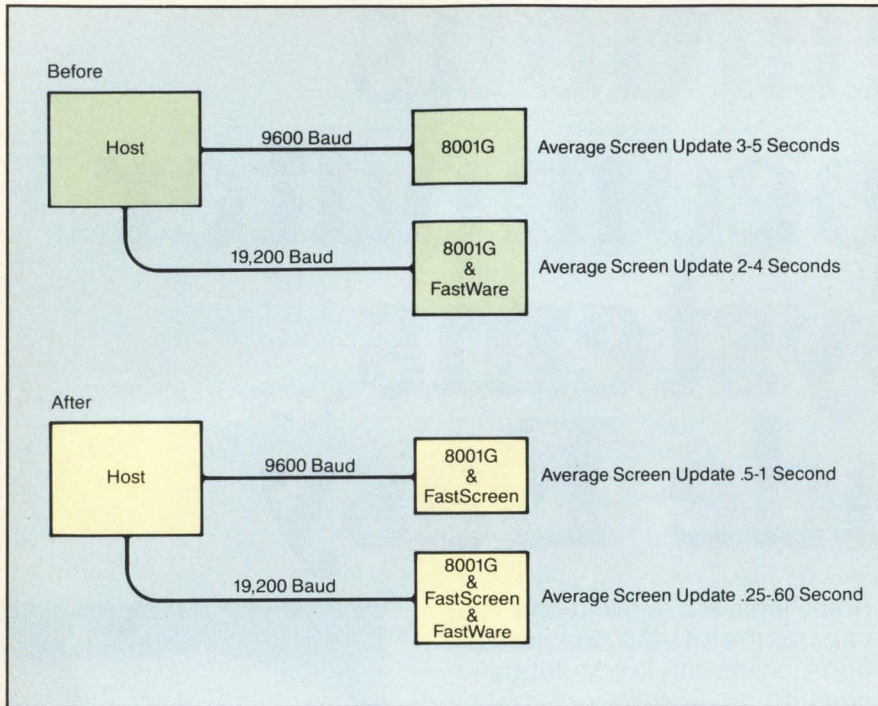


Figure 1: The FastWare driver and FastScreen board combination allows normal G operation of 8001G terminals at 19,200 baud, while the standard G unit operates at 9600 baud.

microseconds. The first eight of these periods are devoted to memory refresh. The remaining 56 periods are available for response to a memory service request by the CPU. Response to a service request involves the generation of a complete set of control signals and occupies between eight and 16 clock periods, depending on the timing of the request relative to the RAM disk's internal functions.

A refresh operation begins about every 6.4 microseconds. A service request involves the issuance of the RAM-disk's data port address and the activation of the system I/O read or write line.

Because the RAM disk's operation is asynchronous with respect to that of the

system CPU, special provision had to be made to insure that a service request by the CPU does not interfere with a memory refresh operation which may be in progress when the request is received.

A Circuit Problem

The completed circuit board has 95 ICs and 15 miscellaneous components on a 48 square inch board. As a result of the complexity of the circuits and the relative compactness of the circuit board, the new card had a problem with increased noise. It showed up as a number of bits of information being dropped intermittently.

The 74SI38 integrated chip was chosen to keep the design simple and compact. It had to function as a bank select and column address select driver.

An important problem resulted from the fact that the 74SI38 drives several complex signals to a total of 64 different 4164 RAM chips over a large part of the board. We had to check the rise and fall time and the noise level to each input of the 64 4164s. The magnitude of the noise problem became clear with the use of diagnostic software to detect the lost information.

Another example of FastScreen's color graphics capabilities.

One approach to solving the problem was to minimize the trace runs to each of the RAM chips. We had to be especially careful of the long runs, avoiding routing them near other signals that generated noise, such as the memory read/write lines. These traces needed more foil to lower overall impedance as seen by the driving chip. The lower impedance, in turn, lowers induced noise to the driven chip.

High quality Rogers flat-type capacitors are inserted beneath the 4164 RAM chips. Since they are flat, they help reduce noise on the power supply bus near each RAM chip. With the capacitors mounted so close to the 4164, noise pickup is reduced to almost zero.

One goal was to avoid going to a four-layer board, which would triple board costs. An engineering time and cost investment was made up front to save costs in the long run. The results of extensive testing, showed that this up-front design strategy avoided the need for a four-layer board.

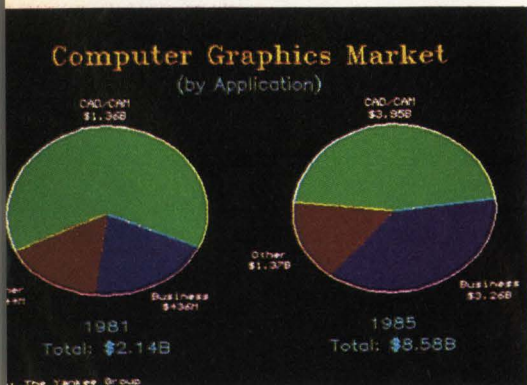
The Driver Problem

The remaining problem was writing the software driver that enabled the RAM disk to talk with screen RAM at a fast rate. To produce screen updates in less than a second, the data transmission rate had to be improved. Information needed to be exchanged at 40 Kbytes per second rather than 9,600 baud that most control applications were using.

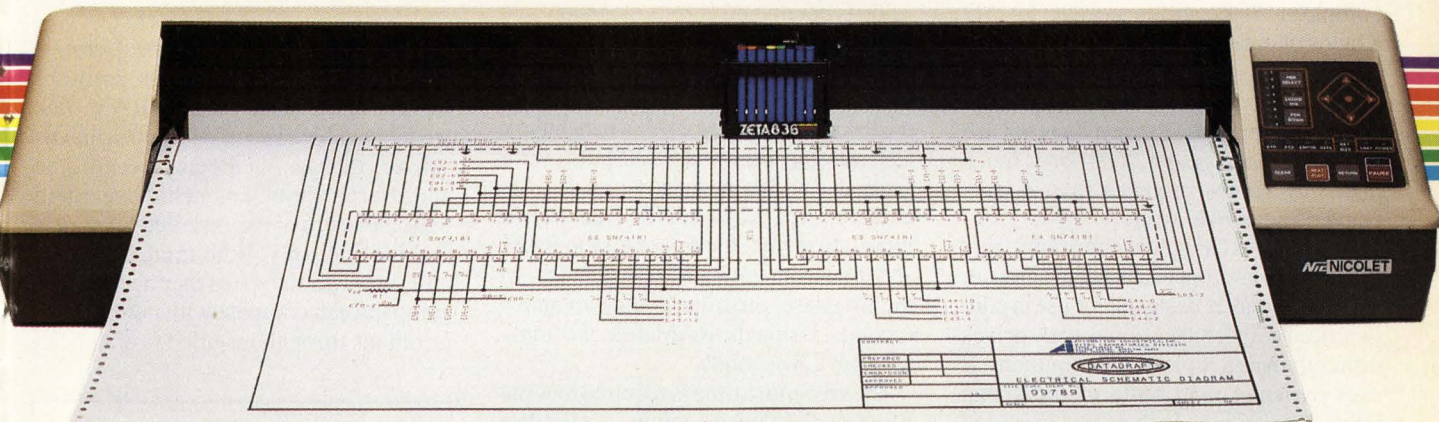
Since the 8080A, unlike the Z80, does not have block move and other micro-coded instructions, in-line coding techniques with multiple fetches and writes were necessary to prevent loop delays from slowing the driver considerably. Using in-line coding, 40 Kbytes per second can be transferred from the terminal screen to the RAM disk. To achieve such a fast update speed, an extremely critical look at the driver's control program was needed to minimize the amount of code executed for any given operation.

An 8080 emulator showed the section of the code on which the processor was spending most of its time. Time was allocated on that basis, economizing the code and maximizing information throughput. The software driver for the 8080A RAM disk is called FastWare (Figure 1).

A special program was written for a host to test the driver as to whether those design changes produced the desired effects. Eight different versions of the driver were developed before the amount of code began to increase. This was the



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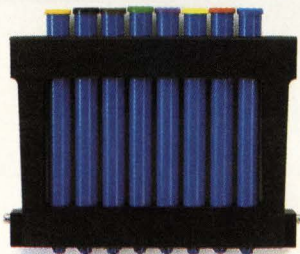


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point at which the incremental cost of improving the code exceeded the benefit from improving it.

RAM Disk Advantage

This RAM disk is a fully electronic disk drive emulator, designed for use in an Intecolor 8000 series terminal or desktop computer. It provides storage for 512 Kbytes of data, a capacity roughly equivalent to that of a conventional 8" floppy disk recorded on one side with double density techniques. Since it does not use mechanical equipment, it responds much faster to access requests than does a conventional disk drive.

As one board inside the terminal, this device provides speed and convenience. The RAM disk is designed for use in conjunction with conventional disk drives rather than as a replacement for them. It uses dynamic read/write memory that holds data only as long as it is provided with power. Consequently, as a storage device, it does not provide the permanence of a floppy disk and requires that information to be saved is backed up on either flexible or hard disk. This is not a problem for most process control users

since they usually have their computers and terminals on uninterruptable power systems.

Such backups need to be used only at the beginning and ending of an operating session. While a program is running, data can be transferred quickly between the RAM disk and system memory as needed.

Tests conducted at Intecolor show that data transfers from the RAM disk to memory are about three times faster than transfers from a double density, 8" floppy disk drive (**Figure 2**). In a benchmark test, a floppy disk and a RAM disk were formatted and then loaded with a data file containing 50 Kbytes. This file was then moved first from the floppy disk to RAM and then from the RAM disk to RAM. In the first case, the transfer took about 8.8 seconds. Using the RAM disk, the transfer took 2.8 seconds.

Clearly, more time is required to write data to a disk than is required to read data from it. In the case of the RAM disk, reading and writing are accomplished in about the same time. In other words, the RAM disk advantage over disk drives is obvious in transfers from memory to storage.

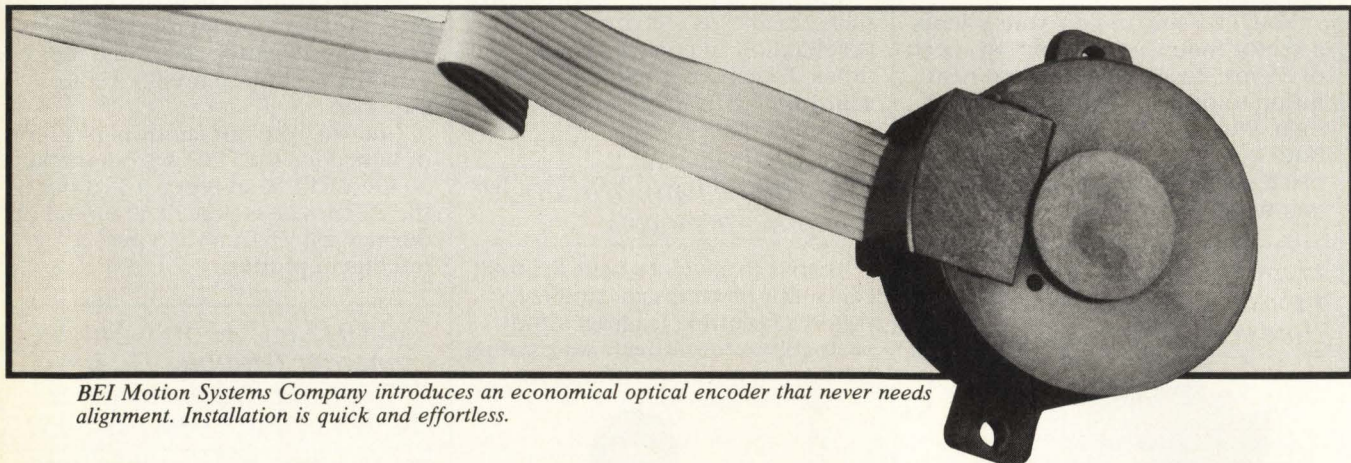
Designing on Demand

The single board addition to a color terminal line, dubbed FastScreen, has increased the performance of the 8001 series considerably. All of the people already using the 8001G terminals can put up even complex new screens in less than a second with the addition of this RAM disk board.

Changing the size and form factor of the board, microprocessor and software drivers to optimize existing RAM disk technology for a specific line of terminals was a challenge. But the engineering time and effort in development has benefitted both the users of the installed terminals and the company. With minimal added cost, users get the speed they need, so the company can compete with newer color terminals through installed products. □

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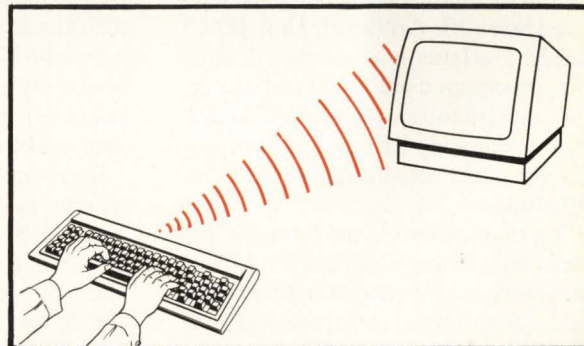
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New Members Join Superminicomputer Families

A range of new superminicomputers were introduced this spring to fill out the product lines of Digital Equipment Corp. (Maynard, MA), Gould SEL, Harris (both of Ft. Lauderdale, FL) and Wang (Lowell, MA) near the time AT&T (New York, NY) announced their first computers. Harris' 60 adds to the low end of their line, while the DEC VAX-11/785, Gould Concept 32/97 and Wang VS 300 are the most powerful of their respective super-mini families. AT&T introduced two 3B5s for lower and three 3B20s for higher end systems. One of the main features of all of the new systems is their compatibility with a family of minicomputers.

Communications, cache memory and a combination of LSI and VLSI with bipolar-type logic are some issues mentioned by several of the announcements, including price/performance ratios.

At the lower price range, Harris' 60 (Figure 1) is aimed at up to 32-user distributed or networked computing and entry-level users. A single precision Whetstone speed of 0.85 MIPS is achieved by a two-card CPU operating under VOS with a 6 Mbyte main memory card and a communications controller. The unit contains an 80 Mbyte Winchester and 23 Mbyte 1/4" tape drive; memory uses 256K RAM chips to fit memory plus error detection/correction and diagnostics on one board. The basic compact system costs \$69,500. Options include cache memory and Integrated Scientific Arithmetic Unit (ISAU) boards. The latter is a hardware floating point processor using VLSI and gate arrays to keep it to a single board. Communications include RJE and 3270 emulation and X.25 networking for CPU-to-CPU links.

Communications in the form of a network and RJE are important for AT&T's computers, as well. Speed and capability similar to the Harris 60 are provided by the AT&T 3B5/100 and 200, designed for up to 60 users. These use the WE 32000 chip as CPU, for speeds of 0.63 MIPS for the 100 and 0.8 MIPS for the 200. An 8 Kbyte cache is standard, in addition to the 8 Mbyte main memory. Peripheral storage is in larger increments than the Harris system, with 160 Mbytes unformatted per fixed drive and 48 Mbytes per removable, as well as streaming tape backup. Though the footprint of these is larger



Figure 1: The Harris 60 superminicomputer supports multiple CAE graphic display systems and other design peripheral equipment.

than the VLSI-intensive Harris 60 and the peripherals are not internal, the system provides modularity, and the disk units can be stacked on the main cabinet. Typical list for the 100 is \$57,000 and the 200 runs about \$73,000. All AT&T computers run UNIX, of course, and though the family is new, UNIX's popularity makes it likely that a strong body of software will be available for these machines.

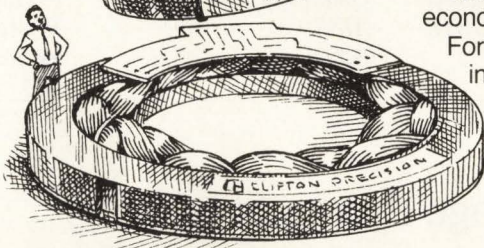
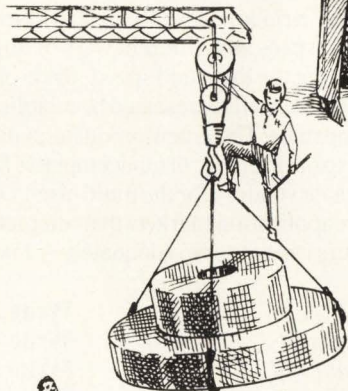
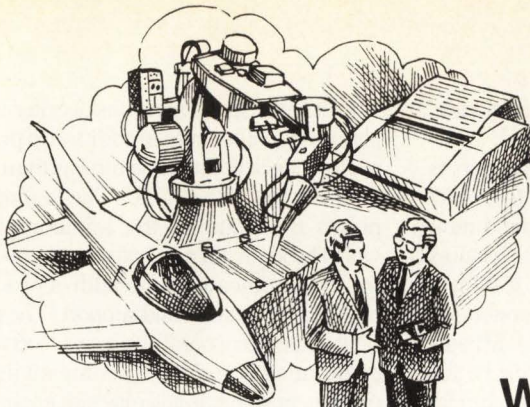
Harris and AT&T have compared these systems to DEC's VAX-11/750. Meanwhile, DEC was introducing a new VAX for the high end of their line, the 11/785. The new system shortens 11/780 cycle time by one-third, to 133 nsecs, and uses Schottky logic for higher-speed switching. Other enhancements over the 780 include 48 rather than 16 Kbytes of console memory, four times the cache space — 32 Kbytes — and RAM instead of ROM-based microcode. DEC touts the 785 performance as 50 to 70% better than the 780, and a field upgrade package is available for the myriad 11/780 users. The basic 785 includes 2 Mbytes memory and the CPU under VMS for \$195,000; with

options like the FP785 floating point accelerator in the same timing and technology as the CPU for \$14,000, storage and communications options, a system can range to \$399,000. Like software and peripherals, communications are common to the VAX family, including DECnet, Ethernet and gateway packages. DEC's ULTRIX-32 version of UNIX will also run on the 785.

An even faster cycle time than DEC's — 120 nsecs — is used in Wang's VS300, which has 32 Kbytes of cache, like the 785. A pipelined processor, intelligent I/O and communications controllers and memory management allow Wang to claim speeds three times that of their VS 100. Dedicated microprocessors in the I/O systems free the CPU from processes like disk and telecommunications links. The basic VS 300 cost of \$170,000 includes 4 Mbytes main memory, console workstation, serial I/O controller and assembler, and enhanced VS O.S. software, and will be available early next year. Wang's machines are known for data processing, office automation and interactive

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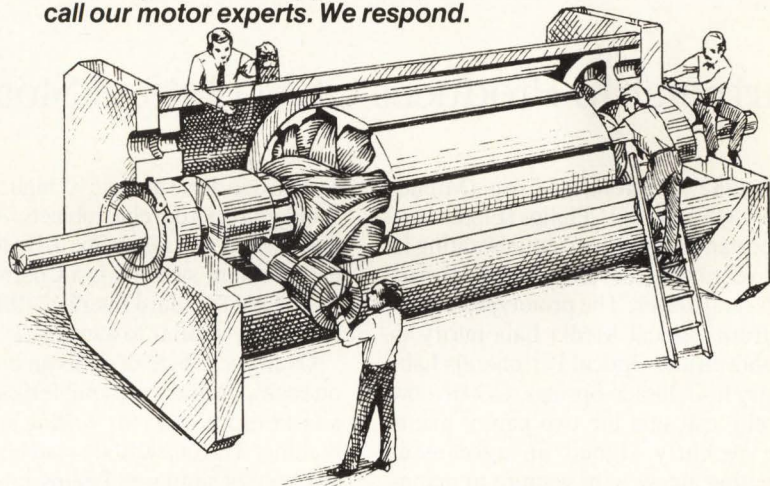
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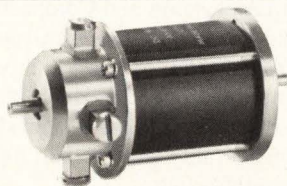
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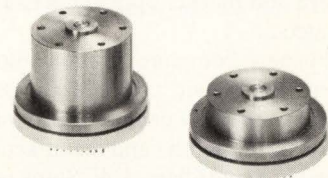
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Write 88

Write 89

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For General Information Write 91

transactions. This system supports up to 192 workstations and printers, with enhancements for more planned. To serve engineering and scientific markets, an optional hardware floating point accelerator increases performance.

AT&T's 3B20 line includes up to 12 Mbytes main memory with an 8 Kbytes cache, DMA and distributed I/O intelligence. Storage is dual ported removable 300 Mbyte and fixed 675 Mbyte drives. An interesting feature of all of the AT&T computers is that they require no air conditioning or raised floors, a special advantage for entry-level minicomputer users. Other AT&T strong points are diagnostics, error recovery and other reliability insurance devices, as well as the popular UNIX O.S. The basic model 3B20S costs \$230,000, and the 20A upgraded system costs \$330,000 to incorporate parallel CPU and memory. A special dual-CPU version of UNIX optimizes the performance of the 3B20A, providing nearly a doubling of 20S performance. The third 3B20 system is a

totally redundant fault-tolerant computer, in which modules are duplicated.

The fastest of these new computers is Gould's Concept 32/97, ranging from 4.67 MIPS to cover 10 MIPS with maximum options. They 97 line includes the features of other Concept models plus 16 Mbyte task addressing. The basic model 32/9705 includes a single CPU, 4 Mbytes main memory and 32 Kbytes cache for \$245,000. Field-installable enhancement modules include a multiply accelerator and an Internal Processing Unit (IPU) additional processor, which, when combined, give a reported 10.08 MIPS Whetstone benchmark. Another module option is Shadow Memory; one to three of these 128 Kbyte units can be added for applications that cannot afford cache misses, but need to run at the cache rate. The 97 uses 10K ECL logic and hardware memory management for full 16 Mbyte addressing by any of multiple tasks. The system runs under Gould's MPX-32 real-time O.S., and they also offer a UNIX-compatible UTX/32 program.

DEC released suggestions of criteria for choosing a supermini in addition to price/performance at the same time as their announcement of the 11/785. The four other points the giant of the minicomputer world brought out are: software, networking/communications, breadth of product offering and service and support. The particular memory configurations, software environments and family compatibilities of these new machines may suit each system to various needs. Though all have different specs and different ways of implementing the logic and speed, these other points are well represented by established companies. These new products continue to expand the range of minicomputers from reliable vendors for the multi-user, complex application markets that microcomputers cannot serve adequately. —Pingry

DEC
Harris
Gould SEL
AT&T
Wang

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Write 249

Partnership Produces OEM Optical Storage Products

Since 1982, Control Data Corp. (Minneapolis, MN) and N.V. Philips (Eindhoven, Netherlands) have been collaborating in joint ventures to develop optical storage media and drives. The prototypes of media from Optical Media Laboratory in Eindhoven and Optical Peripherals Laboratory in Colorado Springs, CO are now in field test, and the two parent giants have recently signed an agreement launching a new joint venture to manufacture and market optical data storage products.

The new company, Optical Storage International, will continue to use the two labs for R&D under the new name, but the headquarters and manufacturing will be in Santa Clara, CA. Some media manufacturing will probably take place at a Philips plant in Blackburn, U.K. Amyl Ahola, currently VP of CDC's Magnetic Peripherals' Santa Clara Disk Division, has been named CEO for the new venture.

Unlike the storage libraries announced by Storage Technology and Panasonic, the initial products will be single 12" disks in

a cartridge drive about 5 1/4" high, to fit in standard racks or relay cabinets. Another feature that will allow this drive to be integrated into systems is a Control Data Intelligent Standard Interface (ISI) to the computer, similar to a magnetic drive.

Over one Gbyte of data can be stored on each side of the removable disks, with a laser diode used for writing and later reading. The laser diode read head uses technology similar to Philips' inventions used in Laservision and Compact Disc digital audio players. As with all current optical storage, the system is archival, or write-once read-only thereafter. But data stored optically with this system should have considerably greater than 10 years lifetime on the disk.

Two tempered glass substrates with a thin separating air layer are bonded to make the recording disk itself. For protection and ease in handling, the disks are permanently encased in a cartridge that is inserted into the drive. Though only one side of the disk can be read at a time, the disk never leaves the cartridge. The entire drive, including power supply,

error-correction circuitry and drive electronics are included in the 5 1/4" high package.

The capability to store Gbytes in computer accessible format in a single slim package is especially attractive for central storage facilities. Fields like medicine and geophysical exploration that generate screens of information so complex as to exhaust traditional magnetic storage systems are a prime market for such optical drives.

As was pointed out at the press announcement in New York and Eindhoven, a single 12" platter will hold as much as 25 file drawers. The system is designed to replace paper, microfilm, magnetic tape reels and photographic files. As a permanent storage method, these early optical storage devices may not replace the refined magnetic and semiconductor memory integral to systems, but ventures with the backing of such large firms hold promise for optical storage to become a vital new industry.

—Pingry

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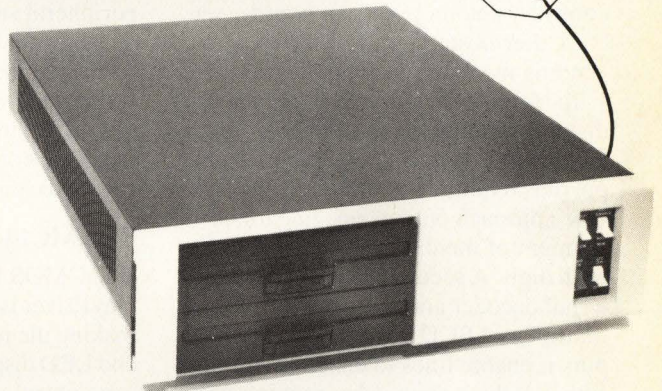
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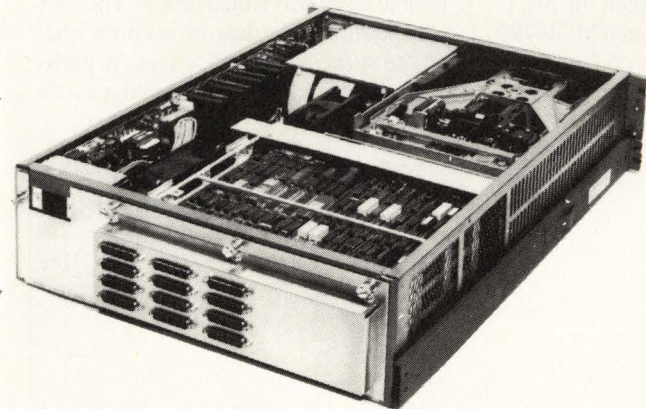
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CMOS Display Drivers Interface Serially To Microcomputers

The pervasiveness of the microprocessor was due to the increased number of system functions that could be performed in a cost effective manner with a given number of silicon chips. This pervasiveness now continues as the ROM, EPROM, RAM and I/O functions are integrated onto the CPU chip.

Cost effectiveness of the new applications for single chip microcomputers may be still measured by the number of functions performed by the number of chips but also by the number of pins required. Package size and number of pins is an important factor in product cost.

Many applications require a digital display output to act as human interface communicating system data or status. Some applications requiring display outputs include: test instruments, industrial controls, automobile dash boards, set-back thermostats, medical instruments, vending machines, and appliances.

To increase system cost effectiveness, display multiplexing techniques were employed to reduce the number of output pins required for multidigit displays. One approach outputs one line for each segment of the digit plus an enable for each digit. A second method uses an external decoder and outputs four lines of multiplexed BCD or HEXadecimal data plus n enable lines to enable 2^m digits. Either of these approaches requires considerable program space and execution

time to provide the display update at a multiplex rate fast enough to avoid flicker. This reduces the processor throughput performance.

Newly introduced CMOS display decoder drivers use a serial bus type of interface to greatly reduce the number of I/O pins. More importantly they unburden the processor from the multiplex service task and also greatly reduce the number of program (ROM or EPROM) bytes required to support the display function.

In this article the software described takes advantage of two powerful bit manipulation instructions available in the 6805 single chip microcomputers (Bit Clear or Bit Set), to implement the serial interface. Recently developed microcomputers of the 6805 family include a peripheral serial port (SPI) to simplify data transfer between chips, and also interchip connections, using its three wire interface. The task of the software in the case of SPI interface is reduced even further, and is only limited to load a data register, indicating that a transfer is required.

The MC14499

The CMOS MC14499 multiplexed display driver is one of the devices aimed at making the interface between the MCU and LED display easier. Each MC14499 can control up to 4 digits of 7 segment LED display plus a decimal point. This

requires only three lines from the microcomputer (MCU): Enable (EN); Data (D); and, Clock (C) inputs.

The multiplexing of the digits is performed internally while the scanner frequency is determined by an on-chip oscillator. The oscillator frequency is determined by a single external capacitor (C_{OSC}). An external oscillator signal may also be used within the recommended range of 200 to 800 Hz to avoid flicker and digit overlap. Also included are a BCD to 7 segment decoder and output drivers to the led display. A divide-by-four counter provides for nonoverlapping scanner waveforms corresponding to the four digits. The digit output buffers are short circuit protected CMOS devices.

Circuit Operation

The MC14499 accepts a 20-bit serial data input, 16-bit for the four digits (BCD format), plus 4-bit for the decimal point selection. The input sequence is the decimal point code (4-bit) followed by the four digits with the most significant digit first.

A typical application of the MC14499 is shown in **Figure 2**. The device is connected to 3 I/O lines of Port A on a 6805 microcomputer. In order to enter data, the Enable input (EN) must be low. The sample and shift of the data are accomplished on the successive clock edges (negative or trailing edge). Data is loaded from the

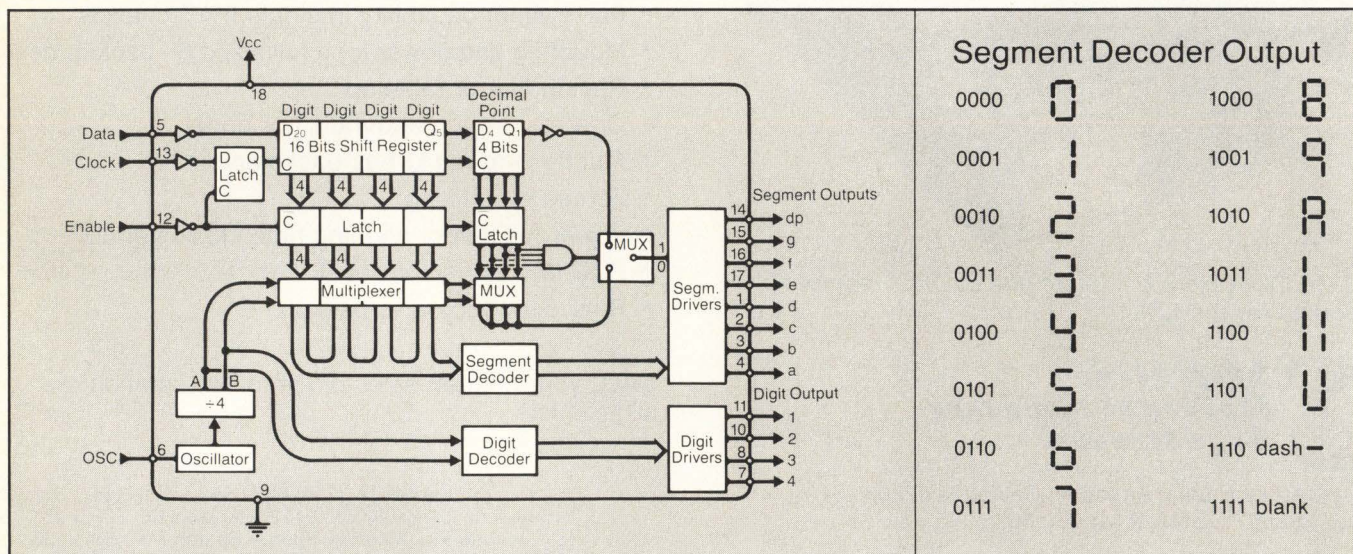


Figure 1: Block diagram of MC14499 Display Driver.

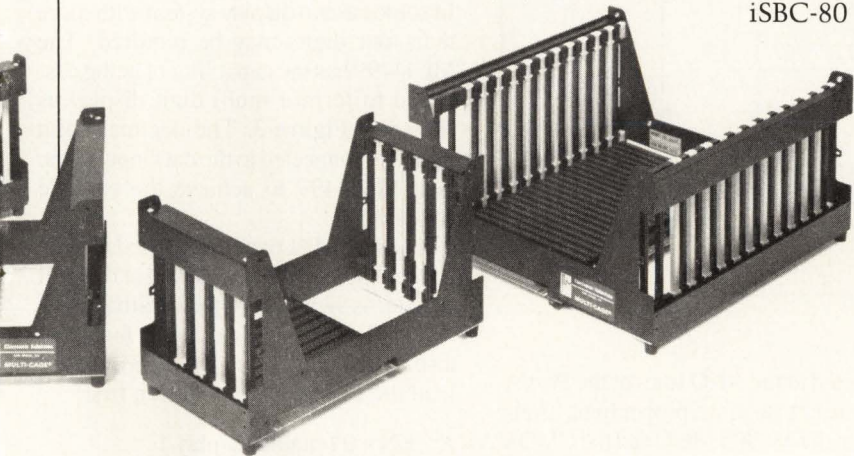
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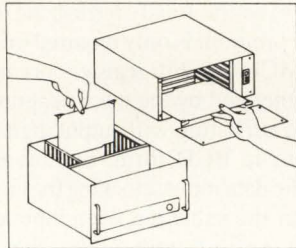
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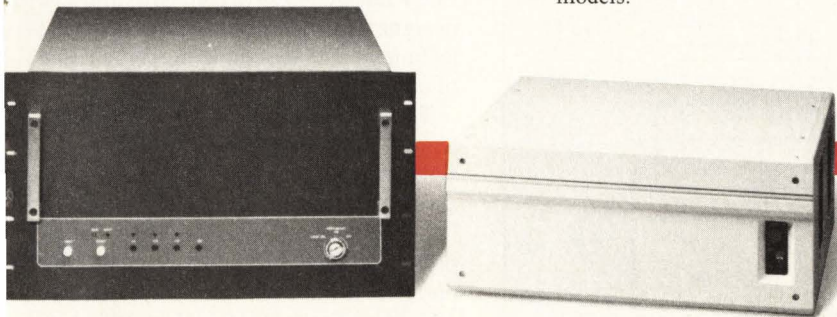


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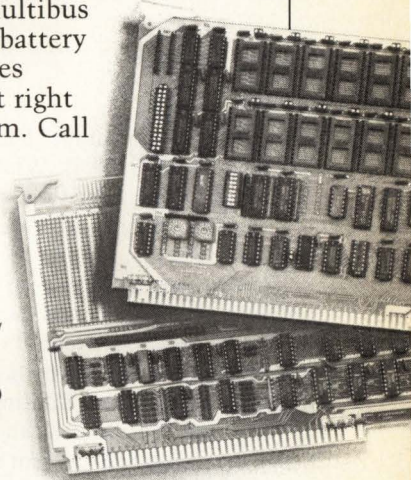


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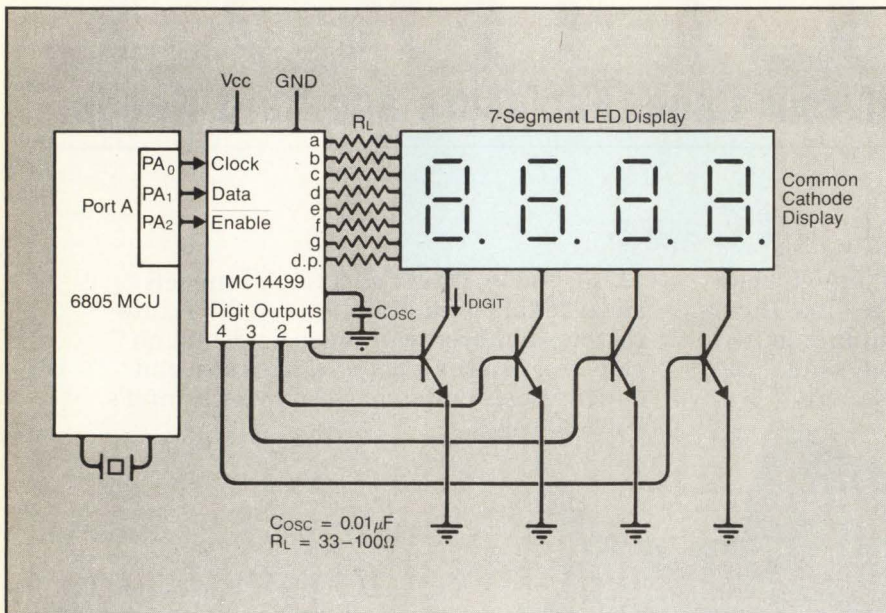


Figure 2: A typical application of the MC14499.

shift register into parallel latched when EN goes high ($\overline{EN} + 1$). While the shift register is being loaded the previous data is held in the latches and presented to the decoder circuitry.

If the decimal point is used the system requires 20 clock pulses to load data, otherwise only 16 are required. Because the segment and decimal point drivers are internal, only current limiting resistors are required. The values can be chosen based upon segment current (I_{seg}), specified by the display manufacturer.

External transistors or digit drivers, such as the MC1413, are required to handle the digit current. Pull-up resistors are

connected to the 3 I/O lines of the Port A in the order to achieve proper logic levels between the M6805 MCU and the CMOS MC14499.

It is a short simple program to output four digits since the M6805 MCU is not required to continuously refresh the display. The program is only required to update the MC14499 shift register once new data is generated by the main program.

A program listing will output digit information, in BCD form, one bit at a time, to the data input, clocking the clock input after the value has been inputted. The Enable (\overline{EN}) input, allows the designer to disable the MC14499 in some

cases, and use the Data and Clock lines for other purposes. It is possible to have several MC14499 chips connected together where a multiple display system is required and control each display independently, using Enable as a chip select line. The program shown reads the packed BCD data stored in two bytes of RAM, and then outputs the data in serial form. A similar programming scheme can be used with the MC6805 MCU or the MC68HC11.

Cascading the MC14499

In some cases a display system with more than four digits may be required. The MC14499 has the capability of being cascaded to form a multi-digit display as shown in Figure 3. The decimal point output is connected to the data input of the next MC14499 to achieve the cascade scheme.

If a binary 1111 pattern is loaded into the decimal point latch, the output of the shift register is switched to the decimal point driver. Therefore, to cascade n four digit display drivers, a setup is used which will load the 1111 cascading pattern first:

- $\overline{EN} = 0$ (enable display.)
- Load 20-bit, the first four bits being 1, using 20 clock pulses.
- $\overline{EN} = 1$, to load the latch.
- Repeat steps a thru c ($n-1$) times.
- $(n \times 20)$ bits can be loaded into m circuits, with 1111 as a decimal pattern to continue cascading.

Driving LCD Displays

For low power applications the combination of a CMOS driver and a CMOS microcomputer such as the MC146805, will be the proper choice to control a LCD display. The MC144117 is fully compatible with MC14499 driver. This allows a designer to use an identical interface technique without changing a single line of code in the program.

The MC144117 will drive the LCD display in a duplex scheme providing the AC signals to the two backplanes and also the associated waveforms to the segments.

Decoder drivers in CMOS technology provide a simple interface to microcomputers and multiple digit displays. The serial interface scheme allows effective utilization of the MCU I/O lines.

Daniel Artusi, Motorola Semiconductor Products Sector, Phoenix, AZ

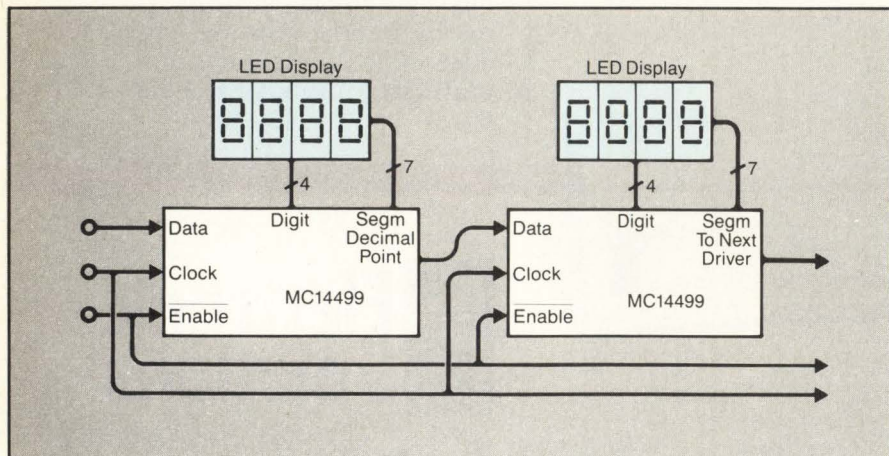
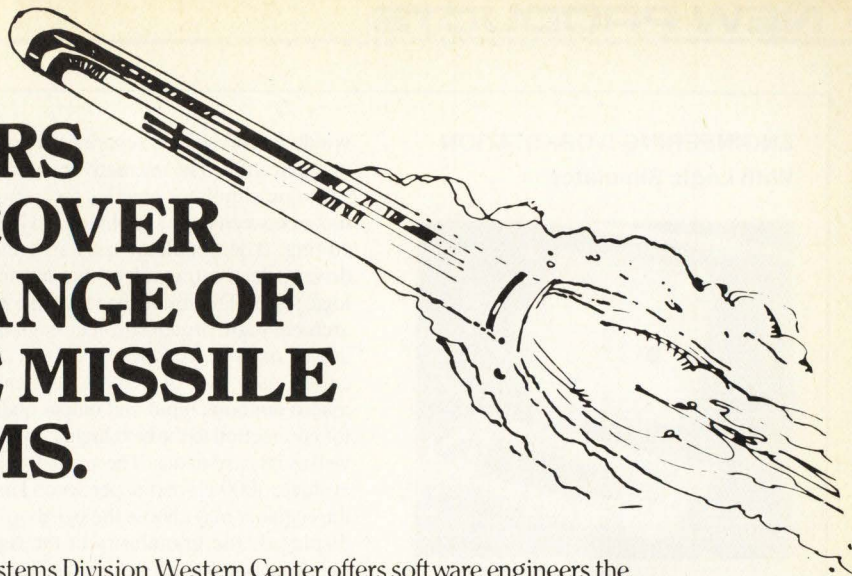


Figure 3: Cascading MC14499.

AVIONICS SOFTWARE ENGINEERING

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SIMULATION SOFTWARE — realtime simulation of avionics systems. Realtime, FORTRAN experience required; experience with MIL-STDs and Harris computer hosted simulation software preferred.

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ENGINEERING WORKSTATION With Logic Simulator

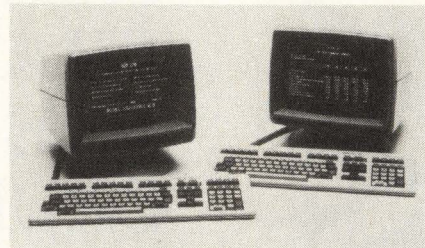


The Expert workstation from Versatec displays multiple windows on a 1024 × 808 pixel CRT. Each

window represents a separate user task or application. The interactive hierarchical logic simulator enables the user to move between logic simulation and logic editing. The simulator uses an event-driven selective trace algorithm and nine logic states. The simulator supports hierarchical logic organization through the use of macros. A logic model is conceived as a tree of macros, and each macro contains input and output nodes for connection to the next higher level as well as internal nodes. The simulator can evaluate 1000 elements per second and the engineer may choose the signals to be displayed, the granularity of the time axis, and options for debugging the design. Subwindows provide access to commands and parameters. **Versatec, Santa Clara, CA Write 131**

DISPLAY TERMINAL

DEC Compatible



The ADM 220 is a video display terminal which is ANSI X3.64 standard and compatible with DEC VT220, VT100 and the VT52 terminals. The terminal has a 80 or 132 column × 24 line display, split screen, and editing capabilities. Options include a 14" display and multiple-page memory. **Learn Siegler, Anaheim, CA Write 132**

CAE SOFTWARE

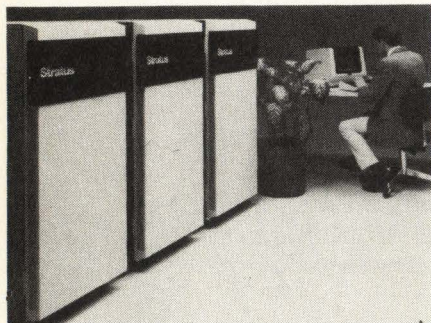
For VAX Systems



CAE Worksystem is software which runs under either the VAX/VMS or Berkeley UNIX 4.2 operating systems. The software provides a multiuser distributed database, allowing a design project to be partitioned into multiple segments. It is a user interface with hierarchical command menus, pop-up menus and multiple overlapping viewpoints. The software includes a schematic capture package, a set of database extraction tools and the ability to be interfaced with a variety of VAX machines. Price is \$45,000. **CAE Systems, Sunnyvale, CA Write 137**

FAULT - TOLERANT COMPUTERS

Based on Multiprocessor CPUs



The XA 400 and XA 600 are software compatible with the Stratus/32 continuous processing system. The XA 400 CPU employs four logical, independent Motorola 68010 processors, each capable of running a different program. The XA 600 uses six logical, independent 68010s, each accelerated by dedicated cache memory and a hardware arithmetic processor. The arithmetic processor provides commercial and decimal arithmetic in addition to IEEE double precision floating point. Price is \$185,000 (XA 400) and \$270,000 (XA 600). **Stratus, Natick, MA Write 127**

MULTI-USER SYSTEM

Supports Seven Users

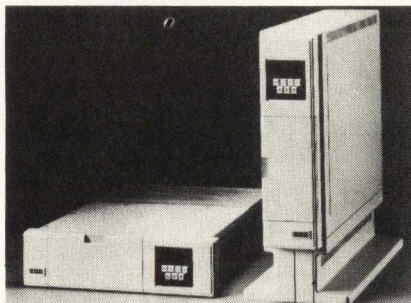


The Mark 2T is a multi-user minicomputer system which employs bit-slice technology, with a high-speed microsequencer, to effect a 600 nsec instruc-

tion time, and a 200 nsec RAM access time. The Mark 2T supports seven users. Price is \$10,000. **Point 4 Data Corp., Irvine, CA Write 130**

MICROCOMPUTER SYSTEM

Q-Bus Compatible



The SMS 1000 Model 40 is a Q-bus compatible, Winchester-based microcomputer system that runs all system and application software developed for LSI-11/23 or LSI-11/73 CPUs. The system incorporates a foundation module which integrates the mass storage device controller, two serial communication ports, backplane circuitry, and the support monitor subsystem on one board. The system is available with 2.5 Mbytes of main memory and two serial communication ports are standard. Price starts at \$5,800. **Scientific Micro Systems, Mt. View, CA Write 134**

LOGIC DESIGN SIMULATOR

Mainframe-Based

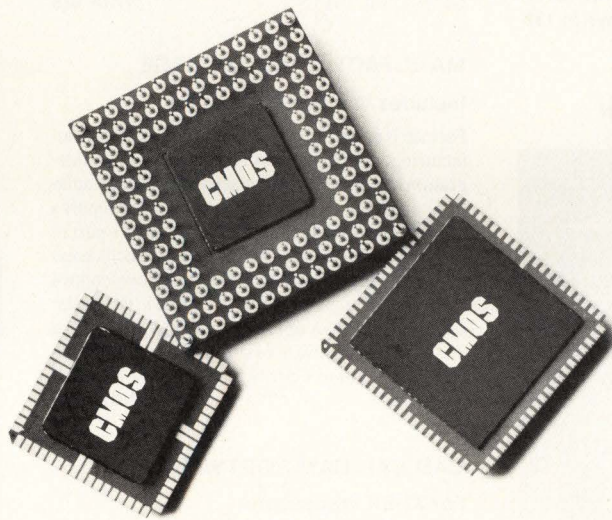
The GenRad HILO-2 High Speed Universal Logic Design Simulator is designed for the CAE 2000 on Apollo based computer-aided-engineering workstation. The device has applications in IC and PC board design, design verification, structural and functional modeling, detailed timing analysis, fast fault simulation, and test validation. Price is \$15,000-\$20,000. **CAE Systems, Sunnyvale, CA Write 143**

IMAGING WORKSTATION

512 × 480 Resolution

The 32-bit DELTApro imaging workstation has a display resolution of 512 × 480 pixels. The DELTApro combines a color raster display, a 5 Megaflop array processor and a 32-bit minicomputer with a shared 8 Mbyte memory as well as MEDICL, an imaging language. Applications include medical imaging, planetary geology, commercial printing, and earth satellite resources. **CDA, Waltham, MA Write 144**

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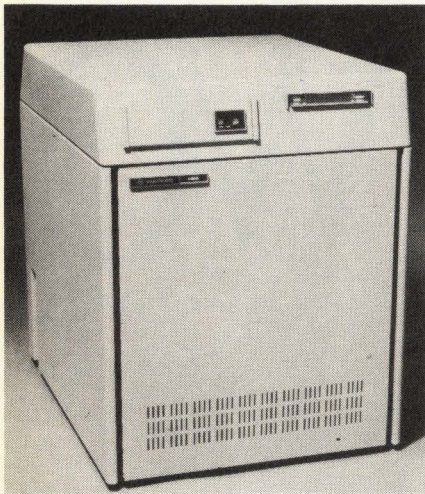
For further information on any of our advanced CMOS gate arrays, contact Fairchild Gate Array Division, 1801 McCarthy Blvd., Milpitas, CA 95035, (408) 942-2672.

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Write 92 on Reader Inquiry Card

SUPER-MINICOMPUTER

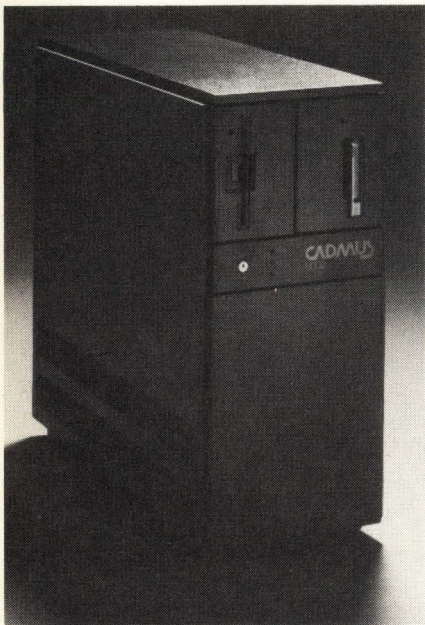
Supports 32 Users



The HARRIS 60 is a 1 MIPS super-minicomputer which handles multi-user applications. Supporting 32 interactive users, the HARRIS 60 can perform decision support, CAD and software development applications at the same time. The Harris 60 has both a cache memory and floating point processor option. The basic system includes a two-board CPU, communications controller, 80 Mbyte 8" Winchester drive, 23 Mbyte 1/4" cartridge tape drive, operator communications terminal and the VOS operating system. Price starts at \$69,500. **Harris**, Ft. Lauderdale, FL **Write 136**

FILE SERVER

Uses Ethernet Or Proprietary LAN

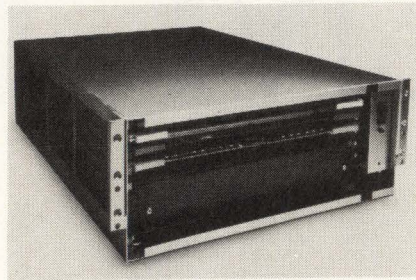


The 9740 diskless computational node and 9760 unison server are additions to the Cadmus 9000 line of distributed system models. Configured as either file servers or diskless nodes, the systems are designed for use with Ethernet or Cadmus' proprietary fiber-optic LAN. The 9740 includes an MC68010

CPU, 1 Mbyte dual port RAM, and an Ethernet controller and transceiver units. The CADMUS 9760 is built around the same basic configuration. Price is \$8,900 (9740) and \$45,900 (9760). **Cadmus**, Lowell, MA **Write 129**

RACKMOUNT TERMINALS

For Process Control



The 6210 series of rackmount terminals includes one color alphanumeric terminal, and two color terminals which combine alphanumeric and graphics. The R6210/01, features VT100 terminal emulation and meets ANSI 3.64 Standards. The R6210/21 has R6210/01 terminal features, and adds an overlay with four planes of bit-mapped graphics at 640 x 480 resolution. The R6210/11, has the same attributes as the R6210/21 in graphics mode. An optional display mode combines three planes of graphics overlaid with either one plane of alphanumeric or blink. Prices for the systems are: R6210/01, \$3,495; R6210/11, \$3,995; R6210/21, \$4,995. **Ramtek**, Santa Clara, CA **Write 128**

MANUFACTURING PACKAGE

Includes Variance Calculation

Forman is an application software product for manufacturing, which includes real-time planning, integration of material and capacity plans and simulation capabilities. The system can plan and report a manufacturer's subcontract operations as a part of the production process. Other features include expanded variance calculation, shop floor control reporting and customer order interface to the master schedule. Forman operates on the IBM 43XX or 30XX series hardware or on any System/370 compatible computer. **Formation**, Mt. Laurel, NJ **Write 138**

CAD/CAE/CAM SOFTWARE

For 32-Bit Processors

Unigraphics II is an interactive graphics software package designed for 32-bit processors. The software has an associative data base that links information and automates the dimensioning of drawings and machine product geometries. Unigraphics II has Fortran-based post-processors, file management capabilities, drafting protocols and multisurface machining. **McDonnell Douglas**, St. Louis, MO **Write 142**

BRIEFCASE-SIZED COMPUTER

With Multiple Windows

The Consultant is a briefcase-sized computer designed for use as a portable or desktop unit. It has a multi-windowing capability and an integrated soft-

ware package. The computer has an 8 x 40 bit-mapped LCD display, and 32K of non-volatile RAM, expandable to 64K. ROM memory is 64K. Mass data storage is provided by a recorder, which is supported by a TOS. Each tape can store 128 Kbytes of data. Price is \$995. **Sord Computer**, New York, NY **Write 140**

TURNKEY SYSTEM

With Laser Printer



The OPS-2000 is a bundled turnkey system which includes a 32-bit Motorola 68010 microprocessor-based workstation, a laser printer, graphics controller, and integrated software. The workstation has two Mbytes of main memory, a bit-mapped screen with 900 x 1152 resolution and a mouse. Minimum disk storage consists of a 42 Mbyte Winchester disk drive and a 20 Mbyte streaming cartridge tape drive. **Interleaf**, Cambridge, MA **Write 133**

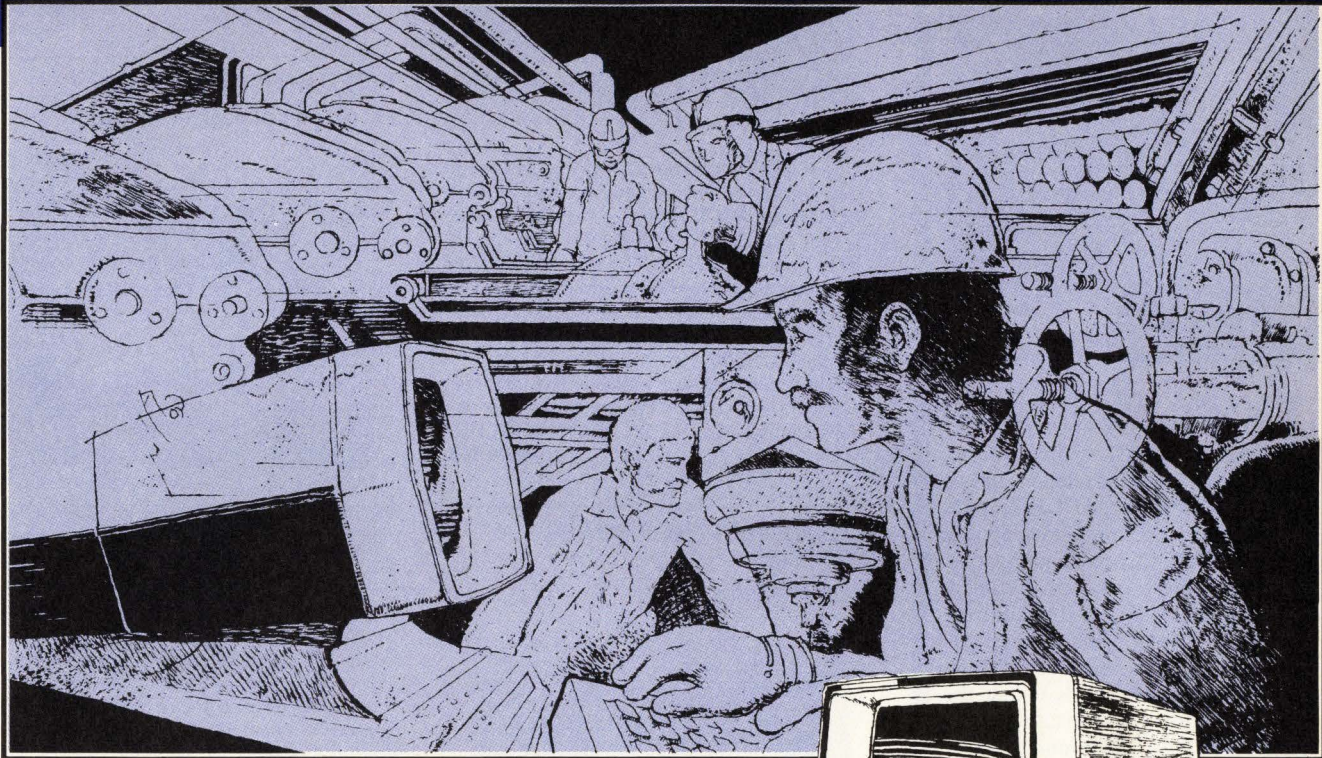
TEST SYSTEM

For VLSI



The 2720 Performance Test System tests and diagnoses bus-structured digital VLSI printed circuit boards at their operating speeds in their native system environment. The 2720 test system may be interconnected to the unit under test in one of two configurations; a bed-of-nails fixture or clipped directly. The 2720 includes memory emulation interface modules, and a 68000 microprocessor with 1.5 Mbytes of memory. System software is a high-level test language executed on UNIX. Price is \$105,000. **GenRad**, Concord, MA **Write 126**

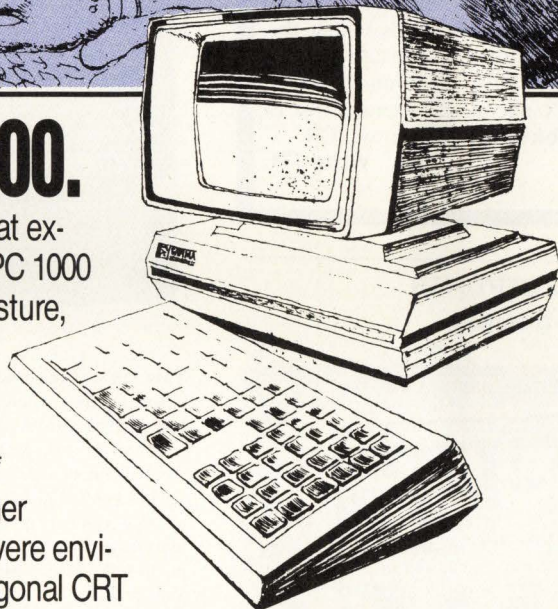
THE SEVERE ENVIRONMENT VIDEO TERMINAL:



THE GPC 1000.

Designed with sealed, airtight enclosures that exceed NEMA 4X and 6P requirements, the GPC 1000 survives in environments where dirt, oil, moisture, heat, corrosives and airborne contaminants are the enemy. Its durable rugged design incorporates advanced technical specifications with smart ergonomics. DEC* compatible, the GPC 1000 outleagues all other video terminals in its ability to perform in severe environments with features like a sealed 14" diagonal CRT with protective anti-glare filter; separate monitor, control unit and keyboard for optional bench top, wall, shelf or ceiling positioning; true bi-directional auxiliary port for two way communications—and much more—all backed with our one year warranty.

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*reg. TM-Digital Equipment Corporation emulates VT100 with AVO

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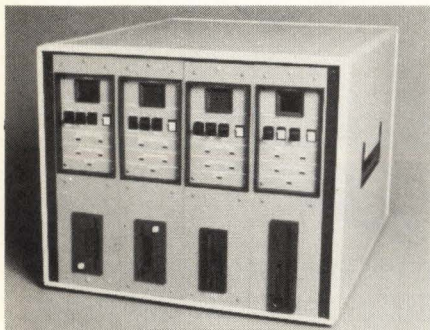
DIGITAL ANALYSIS SYSTEM For VLSI Verification And Test



The DAS 9100 Digital Analysis System from Tektronix is software for VLSI verification and test. It creates a coupled relationship between the DAS 9100 and DEC's VAX host to implement chip test capability. The DAS 9100/VAX combination acts as a test and verification system that interfaces with other VAX-based engineering tools, such as logic simulators. Hardware test functions are performed by modular instrument cards within the DAS mainframe, which in turn is interfaced to a VAX computer running under the UNIX operating system. Price is \$1,000. **Tektronix**, Beaverton, OR.

Write 171

DISKETTE CERTIFIER For Floppy Diskettes



The Model MDC-350 is a four-slot manual diskette certifier for sub-5 1/4" and 5 1/4" floppy diskettes. The certifier detects media defects in high density floppy diskettes in the range of 10,000 bits/in for both sub-5 1/4" and 5 1/4" sizes. Missing Pulse Errors and Extra Pulse Errors can be detected in disks with different formats, number of sides, and recording densities. The drives, available for user selection, in the Model MDC-350 are: a single-sided Sony 3.5" drive, a Tabor 3.25" drive, a half-height Drivetec 5.25" drive, and an Amlyn 5.25" drive. Price is \$40,000. **Certel Inc.**, Fremont, CA **Write 145**

DISPLAY SYSTEM

16-Character



The DPI6B 16-character display system is an upgraded electrical and mechanical replacement for the Burroughs SSD-1000-0041 and -0061 self-scan display. The DPI6B's nominal display brightness is 200 ft L and power is 3 W. A jumper option selects data entry from left-to-right or right-to-left. The blue-green vacuum fluorescent 5x7 dot matrix characters measure 0.35 H x 0.25 W" and are readable at distances of 25 to 30 ft. Characters are loaded on an 8-bit parallel interface, while scan and refresh are handled by an on-board microprocessor with on-chip memory. Price is \$300. **Atron**, Toledo, OH

Write 147

UNINTERRUPTIBLE POWER SYSTEMS

Portable Model

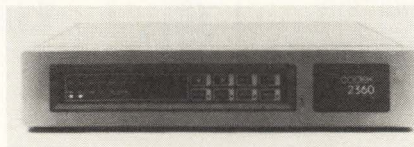


This 1.0kVA power system uses two separate DC power supplies to power the inverter and charge the battery. The 750 VA Mini-UPS is a portable, plug-in unit which is designed to protect small electronics from all potential AC power line problems, including blackouts. The Mini-UPS regulates output voltage to ± 3 percent of nominal, input frequency fluctuations of up to ± 160 Hz are regulated at the output to ± 0.5 percent Hz. **Sola Electric**, Elk Grove Village, IL

Write 148

MODEM

14.4 KBPS



The Codex 2360 is a 14.4 Kbps modem which uses the combined implementation of a custom VLSI signal processing chip set, Motorola 68000 microprocessor and Trellis Coded Modulation scheme. The

modem's control panel enables the operator to configure, monitor and test the modem. Diagnostic tests include modem check, digital loopback, terminal loopback and self-test. The control panel monitors five CQMS line parameters, including error probability readout. **Codex**, Mansfield, MA

Write 156

VIDEO CAPTURE SYSTEM

For Graphics/Image Processing

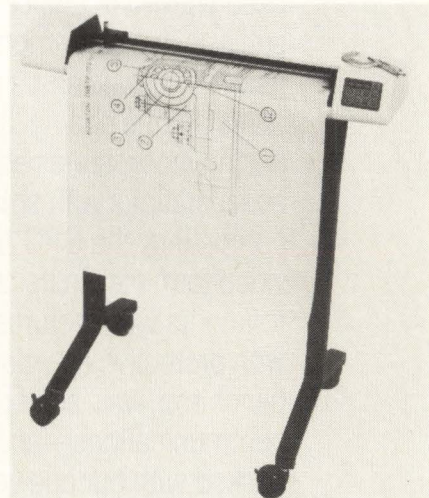


The PC-Eye Series 1000 is an IBM PC-compatible video capture system, designed for applications such as graphics/image processing. The interface board occupies one IBM PC or XT expansion slot. Users can capture video images at 8 frames per second, which may be digitized with 1 or 2 bits of intensity for the IBM graphics adapter or with 4 bits of intensity for other compatible graphics adapter boards. The image is transferred at 1 Mbyte/sec. Successive frames may be captured and stored for post-processing. Price is \$500. **Chorus Data Systems**, Hollis, NH

Write 153

HIGH SPEED PLOTTER

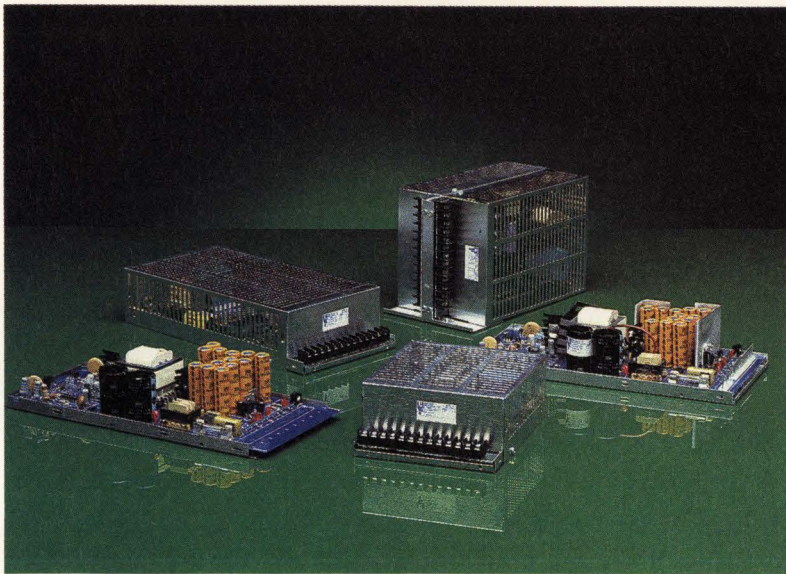
Produces C- and D- Sized Drawings



The DMP-51 plotter produces C or D-size drawings at speeds of 22 in/sec with 4G acceleration and a resolution of .001 inches. The plotter has 26,000 bytes of built-in intelligence and is compatible with existing DM/PL software programs. Both the DMP-51 and a mechanical/architectural version, the DMP-52, with its 18" x 24" and 24" x 36" paper size, are priced at \$4,495. **Houston Instrument**, Austin, TX

Write 150

Rx FOR RELIABLE POWER



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Rx FOR HEALTH

INSTALLMENT FIVE



By Lawrence Lee, MD

Dr. Lee is a leading Southern California Internist, specializing in cardiology. He is a co-founder and board chairman of LH Research, Inc. This column is presented as a public service for better understanding of topical medical problems and possible solutions.

HERPES!

SIMPLE PRECAUTIONS

Our last four columns have generated a great deal of mail from concerned individuals. One of the most often asked questions comes from young couples concerned with the effects of this disease on their ability to have healthy children.

They express a desire to start a family, but are fearful that a known (or possibly unknown) herpes infection may harm their child. Should they go ahead with their plans?

The answer is YES. You may have children so long as you take precautions. If either the father or the mother has had herpes, they should know that the infection cannot be transmitted to the child by blood — only by direct contact. If a parent suspects herpes, certain steps can be taken starting about two weeks before delivery. Diagnosis should be undertaken ten to 14 days before birth, and specimens of the vaginal secretions taken two to three times during this period. If positive, a Caesarian section should be performed to prevent the newborn from infection. If this precaution is not undertaken, and the newborn does come in contact with the infection during delivery, it could result in eventual disability or even death. The simple precautions covered above can help prevent this.

In earlier columns, we discussed the fact that Herpes Simplex Type I (HSV-1) most commonly infects mucous membranes of the mouth, the skin around the lips and mouth, the eyes, and other skin areas above the waist; while Simplex Type II (HSV-2) usually infects the genitalia, rectal area and other skin areas below the waist. These areas of infection by both types hold true in a majority of cases. However, we are seeing a minor amount of infections in which HSV-1 is found below the waist — probably attributed to the changing sexual habits of our present society.

We've seen much concern expressed by individuals who have HSV-1 and are afraid of spreading it to other members of their family. The wisest approach is to avoid close contact (kissing, touching sores, etc.) while the infected person has skin or mucous membrane lesions. ACYCLOVIR has not been approved for treating HSV-1 at this time, although it is being used experimentally. It can be administered intravenously, topically or orally. While it appears more effective intravenously, more clinical trials will have to be performed until the best treatment is known, or if and when the FDA approves this drug for general use.

In the meantime, my best advice is to take the simple precautions I have discussed, and practice good personal hygiene. Open discussion between parent and child may also be helpful in understanding and dealing with such diseases in contemporary society, and provide that ounce of prevention that could make the difference.



The Power Supplier.

This is the fifth in a series of columns by Dr. Lee on medical subjects of current interest, although perhaps not fully understood, by the public. If you have a question, please write Dr. Lee at LH Research, Tustin, CA 92680.

DATA DISPLAY

CAD/CAM Applications

The Model 15DD977 15" raster-scan monochrome CRT data display. Available with composite video and TTL input, its applications include CAD/CAM, graphics, photo reproduction and display of alphanumeric data. Features include 1000 line horizontal resolution, 30 MHz video bandwidth and horizontal scanning frequency of 15.75 KHz. **Audio-ronics**, North Hollywood, CA **Write 146**

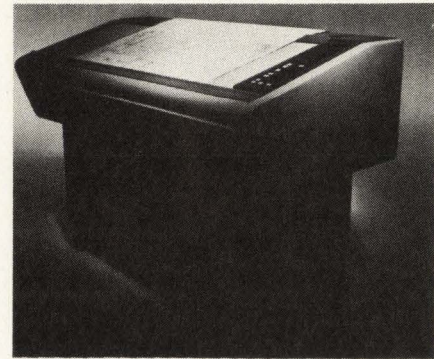
DOT MATRIX PRINTER

120 CPS

The Wide Carriage Imagewriter dot matrix printer is compatible with Apple II and Apple III personal computers. The Imagewriter prints in a 7 x 9 dot matrix at a rate of 120 cps. Featured are eight character fonts and variable resolution, pitch and line spacing. The printer uses friction-feed or adjustable-width pin-feed tractors. Price is \$595. **Apple**, Cupertino, CA **Write 163**

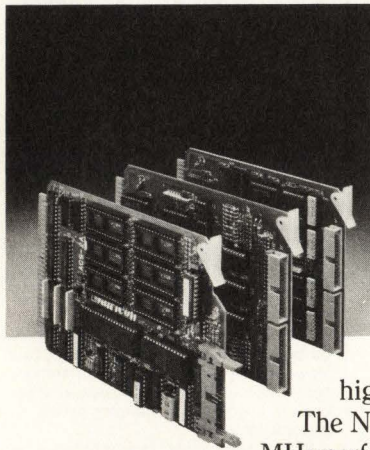
ELECTROSTATIC PLOTTERS

With Raster Data Translator



The Versatec 7000 series electrostatic plotters, available in 36" and 44" media widths, plot at 400 points per inch. Using a raster data translator, they accept data at half resolution. Adjustable plot speed control permits operator or host computer to set speed from 1/8 ips to rated speed. Maximum accumulated error of a plot is $\pm 0.15\%$, horizontal and vertical. Other features include rear-loading twin roll media supply spools, diagnostic keypad/display, darkness control/display, line enhancement, mirror imaging, and reverse imaging. Price is \$47,200. **Versatec**, Santa Clara, CA **Write 165**

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Write 41 on Reader Inquiry Card

POWER CONDITIONER

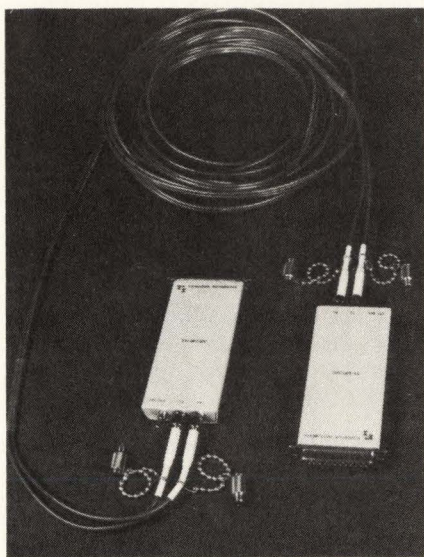
Operates In Forward Transfer Mode



The 800VA is a sine wave UPS operating in the forward transfer mode. On loss of utility power, or if the A.C. line voltage drops too low, a transfer switch places the load on the inverter which is powered by internal batteries. On restoration of utility power or when the A.C. line returns to proper levels, the load is retransferred back to the A.C. line. While operating on the A.C. line the load is protected from line noise or spikes by power conditioning circuitry. Price is \$890. **Nova Electric**, Nutley, NJ **Write 157**

FIBER OPTIC LINK

Duplex Asynchronous Operation



The FI-DP232C fiber optic link has full RS-232C features. The design requires a standard RS-232 source, and operating power is derived from the transmit data. A complete link consists of two modems, mounted to the two ends of a customer specified length of cable. The link is available in lengths of 10, 20, 50, 100, 200, 500, 1000 and 2000 meters. It is EMI /RFI immune and has full duplex asynchronous operation from 75 bits to 20 Kb/s.

Foundation Instruments, Dexter, NY
Write 160

1/4" TAPE SUBSYSTEM

For Micro/PDP-11

The DSD StacPac provides hard disk back-up to DEC's Micro/PDP-11 and other Q-bus based systems. The tape subsystem provides software distribution, system boot, diagnostics load and existing data base upgrade in a footprint of 14" by 16.25". Based on the backplane DSD 8120 dual-wide controller, the subsystem emulates DEC's TSV05/TS-11 tape subsystems, and employs a start/stop tape for use of all DEC back-up utilities. Price is \$3,495.

Data Systems Design, San Jose, CA
Write 172

SYNCHRONOUS DATA UNITS

Interface to DDS Networks



The DSU 500 Series of synchronous data service units permit users to access Digital Data Service net-

works. The units have combination data service/channel service units and can interface on-premise data terminal equipment directly to DDS networks. The 500 Series is DDS-compatible in signaling characteristics, timing, format, and has the ability to respond to DDS control signals. Network transparent, the series operates in full or half duplex modes and at switch-selectable data rates of 2400, 4800 and 9600 bits per second or fixed data rates of 56K bits per second. Price is \$850-\$1,050. **Racal-Milgo, Miami, FL**
Write 164

DISK AND TAPE CONTROLLERS

For Data General's 6160 Series

The Spectra 120 is single-board SMD disk and 1/2" tape controller which emulates DG controllers when using 80 or 16 Mbyte drives. The controller attaches four removable pack or Winchester disk drives and eight formatted 1/2" start-stop or phase encoded and GCR streaming tape drives. It supports transfer rates of 2 MB/second disk and 800 KB/second tape. **Spectralogic, Sunnyvale, CA**
Write 180

**The Most STD-Z80
Power You Can Buy.
Available Now As
A Total System
From
Datricon.**



The STD-Z80 System is built around our powerful new 6MHz ACS-80 board. With MMU addressing, 256K 16K paged memory, 2 serial ports, CTC, bitwise memory and

APU. Compliments include the Z80-DR256 RAM board and the Z80-IFDC — the most intelligent Floppy Disk Controller on the bus. With its own Z-80, the IFDC DMA's anywhere in 256K memory and supports mixed drive types from 3.5 to 8".

The new Z80-SIO4 with quad RS232/422 serial ports and the Z80-PIO3 with 48 channels of open-collector I/O complete the system. And we offer software too. CP/M and SPHERE.

So don't be constrained. Call us now to arrange evaluations.



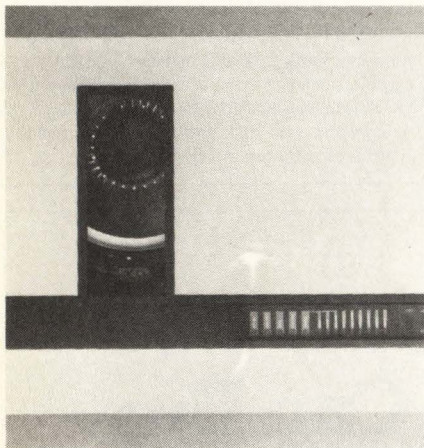
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Lake Oswego, Oregon 97034
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WEST: (503) 636-7671 • CENTRAL: (214) 991-7422 • EAST: (210) 747-2060

Write 42 on Reader Inquiry Card

TAPE SUBSYSTEM

Start/Stop Or Streaming Mode



The 2920 PE/GCR Tape Subsystem can be used in either a 50 ips start/stop or in 100 ips streaming mode. In stop/start mode, the 2920 has a 5 msec average access time. When operated in streaming mode, the 2920 has a 20 msec nominal access time and a 50 msec repositioning time. An optional Per-tec compatible tape interface facilitates 6250 bpi upgrades to older systems. Price in quantities of 100 is \$6540. **Storage Technology**, Louisville, CO

Write 179

5.25" WINCHESTER DISK DRIVES

IBM-XT Compatible

The Micro-Magnum II/II and Micro-Magnum IIR are 5.25" Winchester disk drives with an 11Mbyte formatted cartridge. The II/II provides an additional 11 Mbyte of formatted storage on a single fixed drive. The drives have a track density of 908 tpi and operate at 9254 bpi. The Micro-Magnum II/II drive is priced at \$1,525, in quantities of 1,000 and the Micro-magnum IIR drive, in the same quantities is \$1,190. **DMA Systems**, Goleta, CA

Write 217

LASER DATA TRANSFER SYSTEM

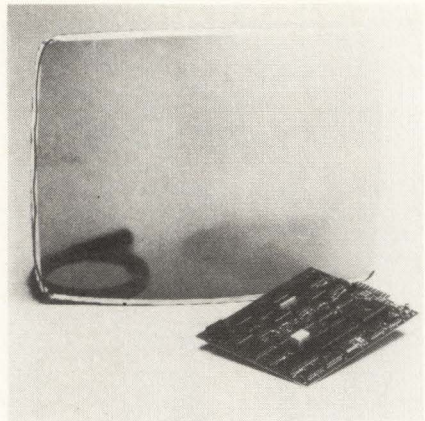
Synchronous And Asynchronous

The Laser Data Transfer System is an optical modem for bi-directional transfer of data between two devices equipped with an RS 232 Serial Interface. It permits synchronous transfer rates of 76.8K Baud and asynchronous speeds of 19.2K Baud. When used with a multiplexer, the system can provide data transfer for 16 asynchronous lines. Data links do not necessitate cabling for routine communications between buildings and remote stations and can be adapted to voice data transfer. **Rothe Development**, San Antonio, TX

Write 182

DIGITIZED TOUCH PANEL

Provide X-Y Coordinate Output



The TK-1000 Series of digitized X-Y touch panels are designed in capacitance technology which allows human touch to be detected on a transparent glass sensor. This method of touch detection provides an X-Y coordinate output with 100 part resolution when a person touches the tempered glass faceplate. The unit consists of a faceplate, a 5" x 7" touch controller board, interconnecting cables and mounting hardware. Available in 12", 13" and 15" sizes, price is \$585 in quantities of 100. High volume discounts are available. **Interactive Systems**, Newtonville, MA

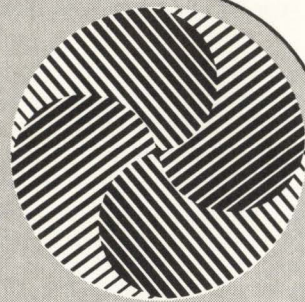
Write 181

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Write 95 on Reader Inquiry Card

TWO-GIGABYTE PUSSYCATS...

One lean controller. Capable of taming up to four big, fast disks—making them look like a roomful of RM05 pussycats. Over two gigabytes of formatted on-line capacity—without changing a line of your VAX-11/750 or 780 software. It's the new Emulex SC7000, the most powerful—and versatile—disk controller ever developed. A single-board controller that can handle any mix of old and new SMD-interface drives: fixed or removable, 80 to 825 Mbytes per spindle, with standard or high-speed transfer rates of 1.8 Mbytes per second.

BEYOND ALL LOGIC...

You can map your physical disk surface into any combination of up to eight "logical" DEC drives (RM03, RM05 or RM08). Completely transparent, of course, to your VMS or UNIX software, application programs and subsystem diagnostics. But you can also break through these logical barriers and take full advantage of the new generation of higher density, higher performance drives. Host-readable SC7000 configurations allow you to write your own custom, self-configuring device drivers for non-standard disk capacities, cylinders, tracks and sectors per track.

TWO OF A KIND...

The new SC7000 disk controller is also a perfect match for the recently announced tri-density (GCR/PE/NRZI) Emulex TC7000 tape coupler. Together they give you almost unlimited mass-storage flexibility. With maximum throughput benefits and minimum parts inventories. Both single-board controllers can be plugged directly into any available Comet Memory Interconnect (CMI) slots in your VAX-11/750 backplane. Or the same boards (with different switch settings) can be loaded into an Emulex V-Master chassis plugged into the terminator slot of your VAX-11/780 Synchronous Backplane Interconnect (SBI) bus.

CATCHING THE CACHE BUS...

Similar high-throughput features apply to another new Emulex product—the SC72 disk controller for PDP-11/70 CPUs. Again, a proprietary bipolar microprocessor architecture supports disk transfer rates of 1.8 Mbytes per second. Again, too, the SC72 gives you a direct backplane interface—via the PDP-11/70 cache bus—for high-speed DMA transfers between the host and any combination of up to four physical SMD drives or eight "logical" drives. All completely transparent to your PDP-11 software. But with a host of OEM and end-user conveniences: priority-level jumpers, 14-sector data buffer to minimize late data delays, switch settings for interrupt vector, address range and up to 32 combinations of pre-defined disk configurations.

Write 64 on Reader Inquiry Card



3545 Harbor Blvd., P.O. Box 6725
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Toll-free (800) 854-7112, in Calif. (714) 662-5600.

AC POWER SOURCE

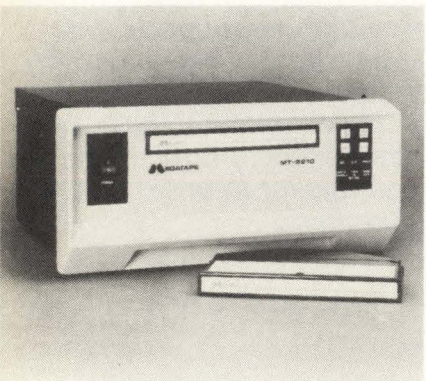
Verifies Output Voltage



The KB Series AC power source provides independent verification of operating output voltage, frequencies, currents, and phase relationships. Measurements are reported on a front panel fluorescent display and watchdog functions are carried out by self-diagnostic circuits that make reports via the display and host interface. Programming is done by the keyboard or host computer and allows for incrementing and decrementing of the output values with user definable resolution. Military programming requirements are met. **Behlman Engineering**, Carpinteria, CA **Write 161**

STREAMING TAPE DRIVES

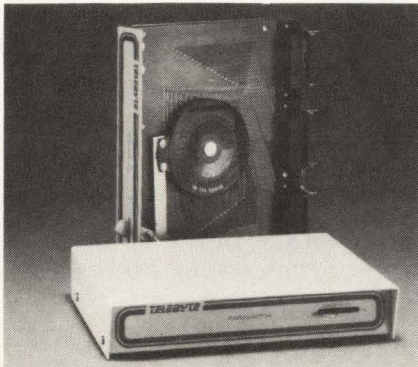
500 Mbyte



The MT-2000 family consists of two 500 Mbyte streaming tape drives which use a book-sized cartridge of 1/2" wide magnetic recording tape. The MT-2210 and MT-2220 drives operate in a 200 or 500 ips streaming mode and a 50 ips start-stop mode. The data transfer rate at 200 ips is 240 Kbytes/sec. When operating at 200 ips, they can back up 500 Mbytes in 36 minutes. A 24-track, bit-serial, serpentine format is used with a packing density of 9,600 bpi. Data is encoded into a 4/5 GCR format. **MegaTape**, Duarte, CA **Write 174**

CENTRONICS INTERFACE SELECTOR

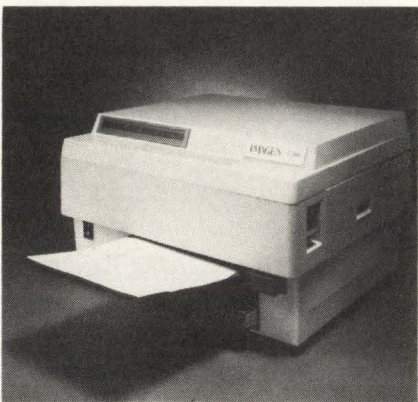
Allows Daisywheel Access



The Model 311 Paraswitch connects two Centronics parallel ports to a master port. With Paraswitch computers can share one printer, or one computer can access either of two printers; a dot matrix or a letter quality daisy wheel. The Paraswitch switches 36 signal leads used in the Centronics connector which is accomplished by a rotary switch that provides 36 form C contacts. Price, in quantities of 100, is \$156. **Telebyte**, Halesite, NY **Write 158**

TEXT AND GRAPHICS LASER PRINTER

Desktop Configuration



The Imagen 8/300 is a desktop, nonimpact page printer with a speed of eight pages per minute at a resolution of 300 dpi. The printer works with many host computers running UNIX and using document composition systems such as troff, TeX and Scribe. The 8/300 emulates daisy wheel and line printers and Tektronix 4014. Price \$9,950. **Imagen**, Mountain View, CA **Write 167**

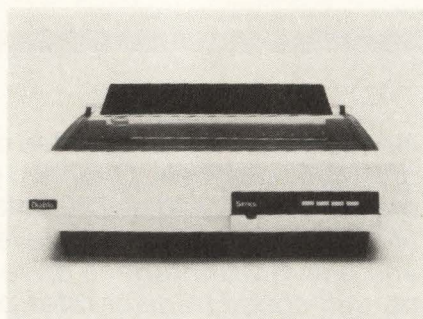
LINE PRINTER

For Text And Graphics

The P1351 line printer has the capability for down loadable fonts, letter quality text, and high resolution graphics. The 132-column P1351 produces letter-quality work at 100 cps and dot-addressable graphics at a density of 180 by 180 dpi. The P1351 has a condensed print mode that allows for 226-column formats, accommodating large spreadsheets and saving paper during large data dumps. **Toshiba**, Tustin, CA **Write 173**

DAISYWHEEL PRINTER

Operates At 30 To 40 CPS



The Series 36 daisywheel printer is designed to operate at 30 to 40 cps. Its all purpose interface includes RS 232 C, IEEE 488, and Centronics. A 12 bit parallel interface is also available. The Series 36 has automated printwheel recognition plus a control panel that allows unattended operation. Price is \$1,595. **Diablo Systems**, Fremont, CA **Write 169**

COMMUNICATIONS PROCESSOR

Supports All Formatting Capabilities



The MC-80/602 communications processor emulates an IBM 3271, 3274-51C, 3276 and models 1 and 2 communications controllers. The device converts a KSR device or asynchronous ASCII host into an IBM 3277-1, 3277-2, 3278-2 terminal communicating with the IBM host using the EBCDIC BSC protocol. Full screen mapping is performed by the MC-80/602 and data displayed on the KSR terminal is the same as an IBM 3277/3278 display station. All screen formatting capabilities are supported. Price is \$1,650. **Innovative Electronics**, Miami, FL **Write 155**

FIRMWARE ENHANCEMENT

Supports File Sharing

The Option 660 is a firmware enhancement for Series 3000 Winchester disk subsystems to support file sharing among two or three HP-computers. The firmware resides in the series 3000 disk controller that arbitrates the use of a common data storage area in the hard disk. Each computer requests access to that area through its own port. Connection to the hard-disk subsystem is by standard HP-IB cables. No additional hardware is needed as long as the distance from the computer to its disk port is 20 meters or less. Price is \$480. **Bering Industries**, Fremont, CA **Write 154**

At Last! A Communications Processor For DEC Computers That You Can Program

The Simpact ICP1600 Intelligent Communications Processor can off-load your host system because it's versatile enough to handle the toughest communications tasks and is code compatible with VAX and PDP-11s.

Use your host system utilities and our software toolkit to create your custom protocols, or let our communications specialists help you develop them. X.25 software is available from Simpact now, and more standard packages are on the way. For under \$5,000, the ICP1600 is the most cost-effective communications processor available today.

256 Kbytes on-board memory to store downloaded programs and buffer data

High-speed DMA transfers with host processor

Eight programmable, serial communications ports (expandable to 20) support multiple asynchronous and synchronous protocols at speeds up to 612 Kbaud

15 Kbytes PROM contains Boot Loader, Self-Test routines and Debugging firmware

DEC MICRO/T-11 processor engine executes the PDP-11 instruction set

Single hex-size card plugs into any UNIBUS slot*

*Q-Bus version available soon.

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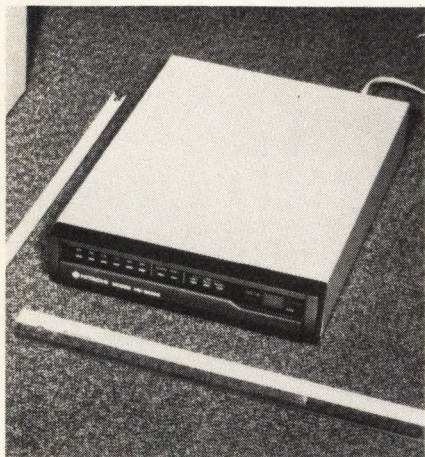
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MULTIPOINT MODEMS

For Signal Processing Applications



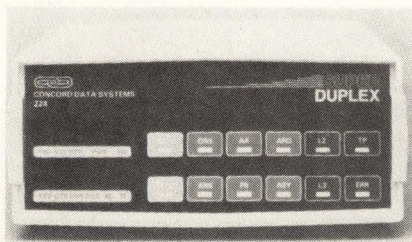
Models HD9600FP (9600 bps) and HD4800 (4800 bps) are point-to-point and multipoint modems, which are used in both dial-up and leased-line networks. All four modems are implemented with single processors and general purpose micro processors which perform functions such as scrambling/descrambling, modulation/demodulation, encod-

ing/decoding, filtering, equalization and timing recovering. **Hitachi Denshi**, Woodbury, NY

Write 219

AUTODIAL MODEM

With Statistical Multiplexing



The CDS 224 is a 2400bps full duplex modem equipped with a statistical multiplexor. Designed for interactive and batch traffic, the CDS 224 is compatible with CCITT recommendations, and is available in an international model. The modem's statistical multiplexor provides three RS-232 ports. The CDS 224 can detect if a remote modem is a Bell 212A-type, and will adapt its speed and modulation accordingly. Price is \$1,695 and quantity discounts are available. **Concord Data Systems**, Waltham, MA

Write 216

KEYBOARD PHONE SOFTWARE

IBM PC-Compatible

Dial-A-Dex is IBM PC and PC compatible support software for the keyboard phone. Features are mail merger, call usage reporting and a note pad area. Additional software is available for dBase, Alpha Micro, MarketFax, and UNIX users. The keyboard phone consolidates all telephone functions at the keyboard of the personal computer or terminal and connects to an RS-232 port of the computer or terminal. Price is \$199. **Voad Systems**, Los Angeles, CA

Write 149

ROBOTIC SYSTEM

2.5 Second Placement Time

The CHAD ECA 101 robot system inserts nonstandard components into a PC board. The system can handle parts from 0 to 1½" and place them in .05" spacing between components. The average time for placement is 2½ seconds from grip to release, with a repeatability of .001". System includes end effector, robot, software and base. Price is \$60,000. **Chad Industries**, Orange, CA

Write 178

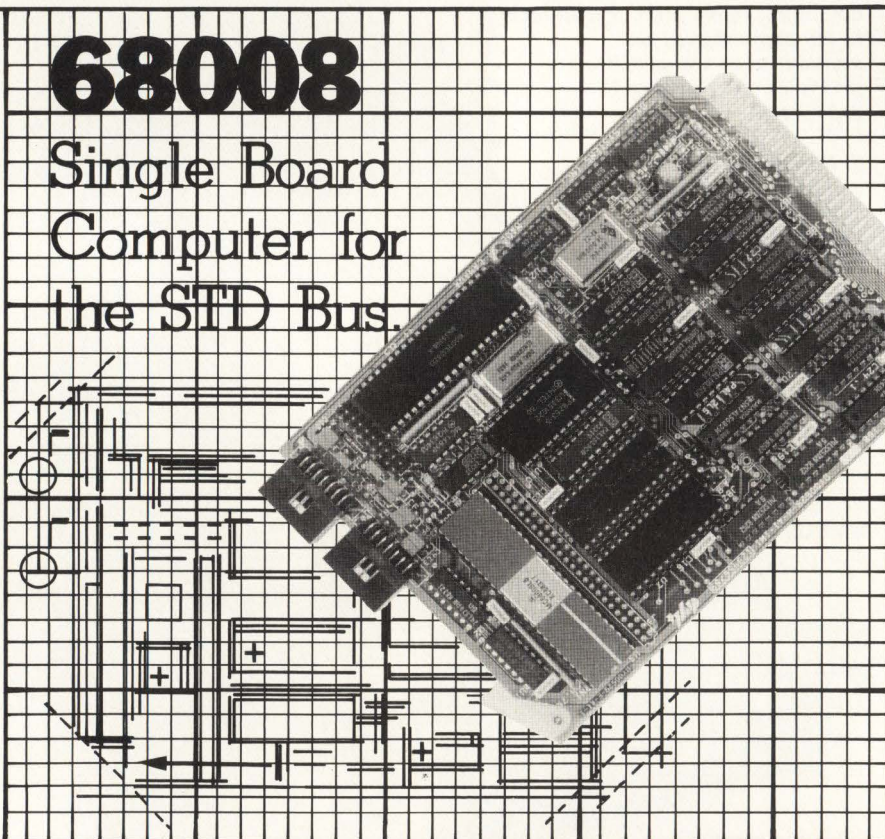
Part of the complete family of DY-4 STD cards, the DSTD-168 offers many unique features resulting in reduced overall cost to the system designer. The card supports dynamic refresh compatible with Z80 transparent refresh thus allowing use of high density quarter megabyte memory cards (DSTD-328). The DSTD-168 supports popular Z80 peripheral chips.

- 68008 CPU (68000 software compatible)
- Two RS-232C serial channels
- Two independent baud-rate generators
- Two 28-pin bytewise sockets for RAM/EPROM/ROM
- 8, 10, 12.5 MHz versions
- Full 1M Byte addressing
- S/W controlled shadow on-board memory
- Three counter-timer channels

DY-4 Systems offers a comprehensive line of STDbus cards, including processor, I/O, memory and peripheral controller capabilities, based on Z80, 8088 and 68008 processors.

68008

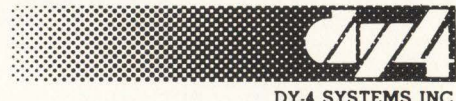
Single Board Computer for the STD Bus.



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888 Lady Ellen Place
Ottawa, Ontario, Canada
K1Z 5M1
(613) 728-3711

U.S. Sales Office
1475 S. Bascom Ave.
Suite 202
Campbell CA, 95008
(408) 377-9822

European Office
Solbakken 48, DK-8450,
Hammel, Denmark
(06) 96-3624,
TLK 60938, (Dendy DK)



Write 82 on Reader Inquiry Card

THERMOELECTRIC HEAT PUMPS

For Cooling Diode Lasers

Device performance is assured by the high quality polycrystalline bismuth telluride manufactured by Varo. The product line of thermoelectric heat pumps from Varo Semiconductor includes both single and multiple stage devices. The devices have a cooling capability range of -94°C to 27°C . Customer support includes thermal analyses, heat pumps designed to meet special requirements, system packaging services, and special power supplies. **Varo Semiconductor**, Garland, TX

Write 152

MASS STORAGE DEVICE

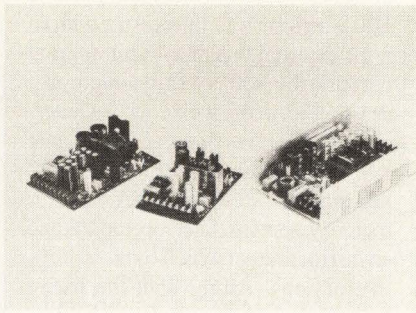
Additional Space For Internal Controllers

The Discovery 1604 Storage Array permits configurations between half-height floppies and full-height Winchester hard disks, and accommodates four $5\frac{1}{4}$ " Winchesters plus four minifloppies or superminifloppies. A power sequencer powers up the Winchesters sequentially, and space for two internal controllers is provided. The Discovery 1604 is available in desktop or rackmount versions. Price is \$3,700 - \$6,075. **Action Computer**, Pasadena, CA

Write 166

POWER SUPPLIES

Telecommunications Applications



This series of switcher lines contain 34 models ranging from 40 to 250 w for applications in instrumentation and control systems, telecommunications and small computer systems. The newest 12 models are output devices and meet VDE, IEC, and UL requirements. VDE-approved components are used where required, as are the appropriate safety spacings and insulation systems. The emission limits of FCC Docket 10780 Class A, and VDE 0871/6.78 Class A are also met. **Power-One**, Camarillo, CA

Write 177

DISTRIBUTED CONTROL SYSTEM

For Industrial Process Control

The distributed control system designed for industrial process control, merges KineticSystems' hard-

ware with Aim industrial software packages. Based on CAMAC interface standard, the system has applications in factory automation, temperature monitoring, and automated testing. Fiber-optic transmission is over a 5 Mbit data highway and permits 62 remote stations. **KineticSystems**, Lockport, IL.

Write 170

STATISTICAL MULTIPLEXER

With Modular Firmware



The TC-500 intelligent statistical multiplexer includes the FlexPak, modular firmware card. FlexPak allows users to field upgrade their units with ComDesign software releases. The enclosure can be configured from 4 to 32 channels. It has network monitoring, statistics gathering, and diagnostics. Options include a supervisory port, synchronous channels, and integral 4800 or 9600 bps modem. Price is \$1,700. **ComDesign**, Santa Barbara, CA.

Write 168

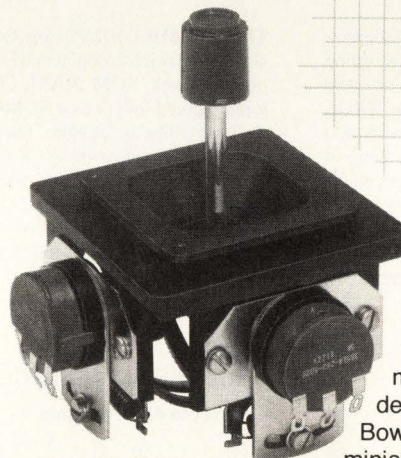
6502 64K COMPUTER-CONTROLLER

The model 83-230 single board computer has 55K of dynamic RAM, up to 8K of EPROM, four parallel ports, 1 serial RS232 port, and four timers. This 4.5" X 6.5" computer uses the 44 pin AIM bus. This computer was designed to be used as an industrial controller. A 2716 monitor EPROM is available for \$19.95. Bare board for \$49.95 or assembled and tested for \$299.95.

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Reliable & Versatile



MJ Series

You have reliable performance and custom design versatility with Bowmar's MJ Series miniature joysticks.

Standard benefits include: • All metal functional and structural parts • Replaceable potentiometers • Proportional rate control • Simplified field repairs.

Add to this Bowmar's long-term leadership in design and production. Choose MJ Series joysticks for a variety of your needs. Contact us today.

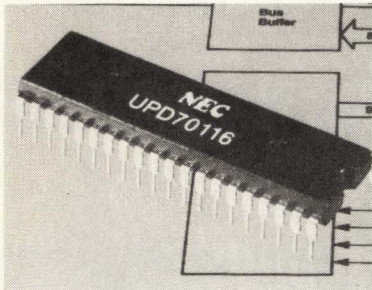


BOWMAR INSTRUMENT CORPORATION/Aerospace Division
8000 Bluffton Rd. • Fort Wayne, IN 46809 • 219/747-3121

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PROPRIETARY MICROPROCESSORS

16-Bit Dual Data Bus Structure

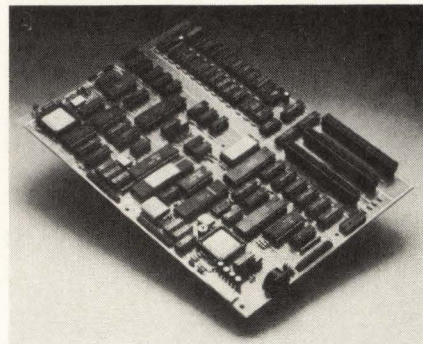


The V-Series from NEC is a group of high-performance proprietary microprocessors

designed in CMOS technology. The V20 is an 8-bit microprocessor with an 8-bit external bus and 16-bit internal bus, and the V30 is a 16-bit microprocessor with a 16-bit external and internal bus. Features of the series include a 16-bit dual data bus structure for the internal bus, dedicated hardware for memory access related operations and an instruction set which consists of 101 instructions. Along with the native operation mode, an emulation mode is available. With standby functions, clock supply to the majority of circuits is stopped, and power consumption in standby is reduced. Prices are \$75-\$90. **NEC**, Mountain View, CA

Write 215

MICRO-CPU PC Compatible

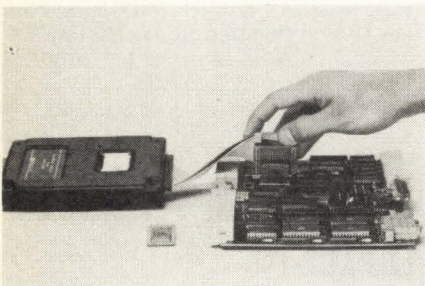


The FE Model 6410 series of micro-CPU's are IBM-PC compatible and have the option of a floppy disk controller and/or monochrome video display controller integrated on the CPU board. The 2-layer boards include 64K or 128K of parity checked RAM, 32K of EPROM space, parallel printer port, serial port, IBM PC compatible keyboard port and three IBM PC compatible expansion slots. BIOS software included in the EPROM supports PC-DOS, MS-DOS, CP/M 86 and Concurrent CP/M. Price is \$275. **Faraday Electronics**, Palo Alto, CA

Write 211

TRACE MODULE

For Analysis of 80186-Based Systems

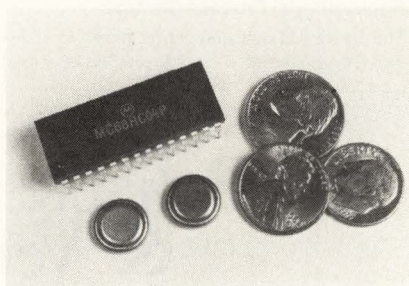


The TMDA 80186 subsystem is designed for analysis of the Intel iAPX 186 by tracing and recording microprocessor bus activity at the machine-cycle level and displaying it in mnemonics. The TMDA 80186 is used with Dolch's LAM 4850A and 64300 logic analyzers, and connects into the pod inputs of those instruments. It connects to the system under test through a plug-in cable and a buffer probe that houses the iAPX 186 microprocessor chip in a leadless chip carrier. Price is \$3,800. **Dolch Logic Instruments**, San Jose, CA

Write 214

HCMOS MICROCOMPUTER

8-Bit Architecture



The MC68HC04P2/P3 are two HCMOS 8-bit single chip microcomputers which contain a CPU, on-chip clock, ROM, RAM, I/O, and timer. Features include low power HCMOS, stop and wait modes and 8-bit architecture. The MC68HC04P2/P3 are pin compatible with the MC6804P2 and contain 32 to 128 bytes RAM. The microcomputers have memory mapped I/O and 1024 to 2048 bytes user ROM. The devices have options such as 20 bidirectional I/O lines with TTL or TTL/CMOS interfaces. **Motorola**, Austin, TX

Write 208

CMOS MULTIPLIER

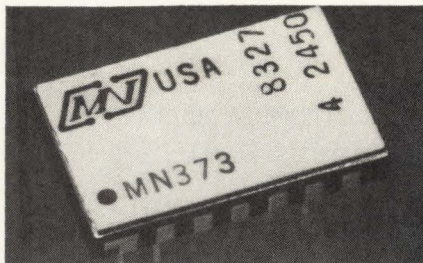
16 x 16-Bit

Bipolar performance at CMOS power requirements is how the MPY-16MI 16 x 16-bit parallel multiplier will be marketed. The device is a two's complement, unsigned magnitude or mixed mode device. It is pin-for-pin compatible with TRW's MPY-16HJ. Multiply time is 170 ns and power consumption is 150 mw at 5 volts. **International Microcircuits, Inc.**, Santa Clara, CA

Write 190

TRACK/HOLD AMPLIFIER

10 μSec Acquisition Time



The MN373 is a high-resolution, track-hold amplifier which is compatible with DIP packaged 14-16 bit A/D converters. Dynamic specifications include 10μsec maximum acquisition time, 1 ns aperture jitter, and 400kHz small-signal bandwidth. MN373's $\pm 0.25\mu\text{V}/\mu\text{sec}$ maximum output droop rate enables the device to hold signals to the 14-bit level for up to 2.4msec and to the 16-bit level for up to 600μsec. Packaged in a 14-pin, ceramic dual-in-line, the MN373 is TTL compatible. **Micro Networks**, Worcester, MA

Write 210

DISK DATA SEPARATOR

MFM Decoding

The DP8460 is a monolithic disk data separator chip which incorporates on-board PLL control circuitry. The chip is designed to be implemented in either the disk drive or disk controller section of the disk system. The DP8460 is designed for 3.5", 5.25", 8", and 14" hard disk drives, high density floppy disk drives, and optical disk drives. Features include MFM decoding, the ability to detect an MFM missing clock and 2-to-15 Mbit/sec data rates. In addition the separator has a power consumption of 500 mw, max and 300 mw typical. In quantities of 100 to 999, price is \$25.75. **National Semiconductor**, Santa Clara, GA

Write 191

ETHERNET INTERFACE

Connects 48 Terminals

The CS/I-HSM high-speed multiplexed host interface system is a front-end processor connecting 48 terminal sessions from other nodes on an Ethernet LAN to a VAX over a single high-speed serial line. It consists of Bridge's Communications Server/1 (CS/I) network interface system incorporating a HSM interface card linked via a single RS422 cable to Bridge's hex-size Unibus host adaptor board inside the VAX. The CS/I-HSM may be located up to 500 meters away from the host system. Price is \$16,500. **Bridge Communications**, Cupertino, CA

Write 188



ARTIFICIAL INTELLIGENCE

and Advanced Computer Technology

CONFERENCE/EXHIBITION

April 30, May 1-2, 1985 • Long Beach Convention Center • Long Beach, California

*Focussing on commercial and industrial applications
of Artificial Intelligence*

Extensive Technical Program

The far-ranging technical program is under the direction of Dr. Murray Teitell, Chairman of the Department of Computer and Information Sciences, Northrop University, Inglewood, California. The most recent trends and developments in AI will be covered, including:

- Knowledge Information Processing Systems
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- Expert System Development Systems
- Expert Systems
- Computer Vision

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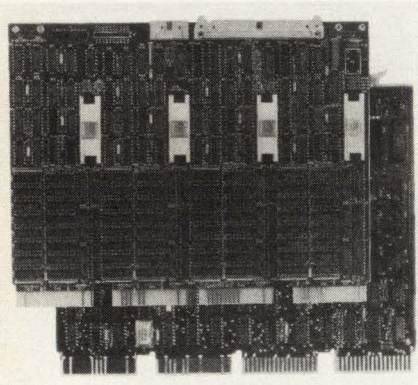
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GRAPHICS CONTROLLER

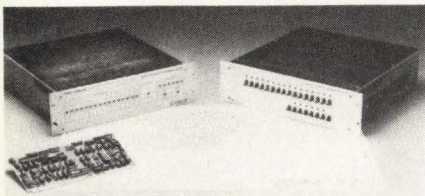
For DEC LSI-11 Bus



The GC-20 Graphics Controller is designed for use with high resolution monitors on DEC LSI-11 mini-computers. The controller consists of two standard DEC quad boards: the GI-20 graphics interface board and the RM-20 refresh memory board. It generates a 1024 × 1024 interlaced image and emulates the Tektronix 4010, 4014, and 4065 terminals. Operating in either a programmed I/O or a DMA mode, it uses an on-board 68000 microprocessor and is supported by a 128 Kbyte scratchpad RAM and a 128 Kbyte EPROM firmware set. **Dataram**, Cranbury, NJ **Write 207**

INTERFACE

For Multibus-Compatible Computers

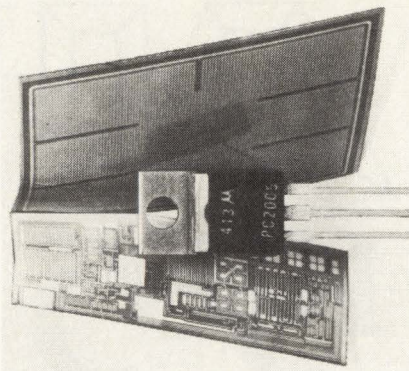


The GM796-4 is designed for coupling data conversion systems to Multibus-compatible computers. This interface features four data ports and a data transfer rate of 250K words/sec. The maximum addressing capability is one Mbyte. Operational features include DMA and programmed I/O modes. The GM796-4 may be controlled by 8 bit or 16 bit CPU's in the bus master. Functionally, the interface is a smart type device that has nine hardware/software operating modes; bus control, bus data, bus address, interrupt circuit, I/O decode, status, DMA control, and input and output circuits. Price is \$2,950. **Preston Scientific**, Costa Mesa, CA **Write 193**

PROTECTION CIRCUIT

Operates At 15 Amps

The MPC2005 is Motorola's first SMARTpower II device, a technology that combines high-speed CMOS logic and high-current TMOS vertical power structuring on a single chip. Capable of discharging capacitors with peak currents of 150 amps, the MPC2005 can operate at up to 15 amps of continuous anode current. When voltage exceeds 6.2V, or the junction temperature rises over 125°C, the



device trips and removes voltage from the system. In quantities of 100 price is \$4.50. **Motorola Semiconductor Products Inc.**, Phoenix, AZ **Write 205**

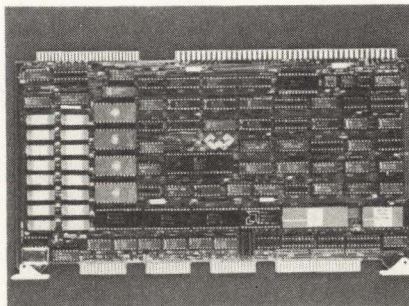
CMOS CONTROLLER

For NMOS, CMOS DRAMs

The 82C03 peripheral chip from Intel controls and refreshes arrays of NMOS or CMOS 64K bit dynamic RAMs in microcomputer systems and on memory expansion boards. The 82C03 is pin and function compatible with Intel's bipolar 8202A and 8203. The 82C03 performs multiplexing of row/column memory addresses, generation of strobes used by RAMs to latch their addresses internally and initiation and control of memory refresh cycles. It also provides arbitration between simultaneous requests for memory access and refresh and acknowledgement to the system CPU when memory-access cycles begin. Price is \$35 in 100-piece quantities. **Intel Corp.**, Santa Clara, CA **Write 192**

SINGLE BOARD COMPUTERS

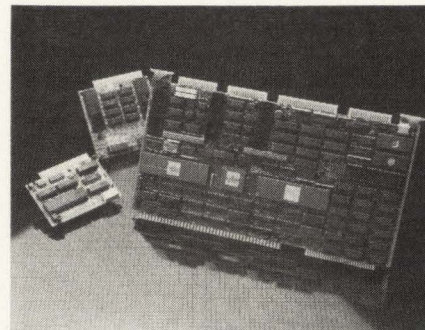
Multibus-Compatible



The MSC 8017 and MSC 8014 are two Multibus-compatible single-board computers based on the 6MHz Z80B processor. Each board provides 128K of dynamic RAM controlled by four memory maps. Both SBCs feature 24-bit address recognition, programmable I/O configurations for multitasking applications, parallel and serial I/O ports, eight-level interrupts and sockets for 32K of EPROM. The MSC 8017 provides three programmable parallel ports (24 lines), and the MSC 8014 has one serial port and six parallel ports (48 lines). Price is \$1,116 in single quantities and \$781 in OEM quantities of 50 to 99. **Monolithic Systems**, Englewood, CO **Write 196**

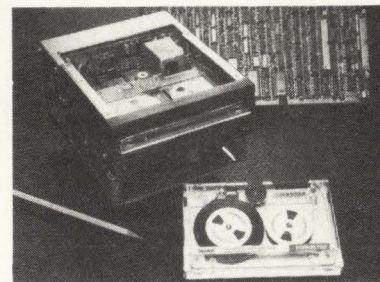
SINGLE BOARD UNIX SYSTEM

1 Mbyte RAM



The HK68A single board UNIX system has 512 Kbyte or 1 Mbyte of RAM and includes Winchester and tape I/F, and eight serial ports. The board has two iSBX I/O expansion plugs, quad channel DMA, MMU, 32Kbytes of EPROM, user programmable LEDs and dipswitches, as well as three programmable 16-bit counter/timer channels. Heurikon supports UNIX System III and V with drivers for Ethernet, SDLC/HDLC, and floating point processors. **Heurikon Corp.**, Madison, WI **Write 209**

Erratum



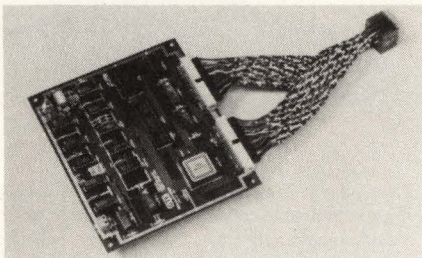
The photo accompanying the department article, "Disk Backup Saves Space and Power" on p. 28 of *Digital Design's* March 1984 issue is incorrect. The correct photo (above) shows 3M Corporation's HCD-75 Data Cartridge System with SCSI interface.

In the April issue of *Digital Design*, the ad for HDL Research Labs on page 64 had an incorrect phone number. Their correct number is 713-896-8582.

In the April 1984 feature "Inputting Graphics by Digitizer," the Micro Control Systems 3-D digitizing system is incorrectly referred to as electromagnetic. The system is actually electromechanical.

EVALUATION SYSTEM

Provides In-Circuit Emulation

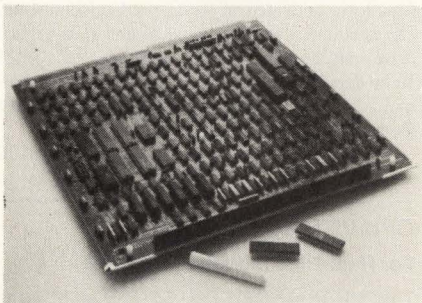


The G65DS-150 evaluation system is for designers who want to use the G65SC150 communications terminal unit in their products. The CTU is a single-chip CMOS microcomputer that merges modem and line-signaling capabilities with the intelligence and programmability of a 65SC02 microprocessor. The evaluation system provides real-time in-circuit emulation and program for the CMOS CTU when used with a 6500-series microprocessor development system. **GTE Microcircuits**, Tempe, AZ

Write 213

DISK AND TAPE CONTROLLER

Data General-Compatible



The ZDF-1 is a dual function controller which is compatible with DG's Nova/Eclipse Series mini-computers and has emulation of DG 6060, 6061, 6067 and 6122, 6160, 6161 disk subsystems and DG tape subsystems 6021 and 6125. The ZDF-1 runs under RDOS and AOS operating systems. Up to four disk drives and eight tape drives are controlled by functionally dedicated microprocessors. Data transfer rates of 2 Mbyte on disk drives and 1 Mbyte on tape drives are supported. Price is \$4,195. **Zetaco**, Eden Prairie, MN

Write 212

10 MHz COMPUTER BOARD

Multibus Compatible

The Am97/8605/010 is a plug-in and software compatible upgrade for the Intel iSBC 86/05. The board features serial and parallel ports, three counter/timers, 8K static RAM, sockets for 64K of EPROM, an interrupt controller, and three SBX connectors. The SBX connectors enable a variety of SBX modules to be plugged into the connectors to change the board's functionality for meeting specific applications. In quantities of one to nine, price is \$1,995. **Advanced Micro Devices, Inc.**, Sunnyvale, CA.

Write 203

INSTRUMENTATION CONTROL

For VMEbus Computers

The GPIB-1014 computer interface allows users to implement VMEbus computers as general instrumentation system controllers. The interface can be used as an IEEE-488 Talker, Listener, or Controller.

It supports normal and extended talker and listener, serial and parallel poll, service request and remote programming functions. The GPIB-1014 uses a Hitachi HD68450 LSI DMA controller with a DMA data transfer rate of 500 Kbytes/sec. The interface has 24 bit addressing and programmable selection of the Address Modifier Codes. Price is \$1,295. **National Instruments**, Austin, TX

Write 201

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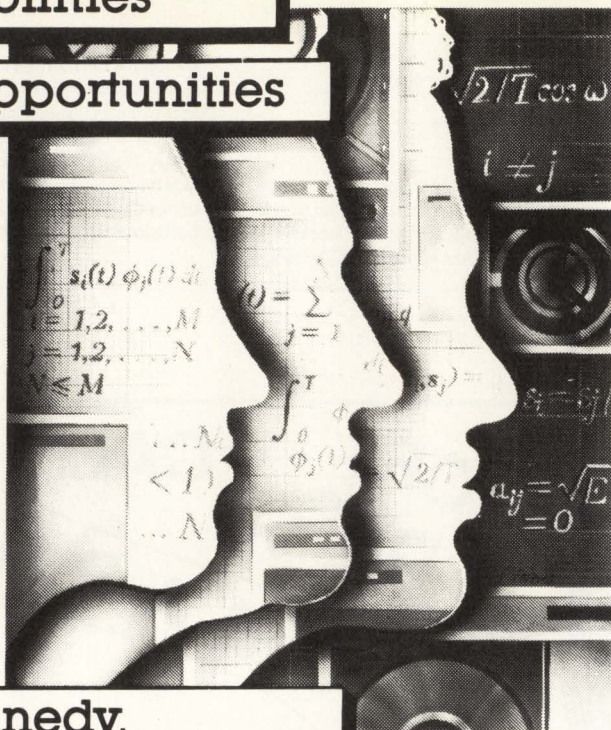
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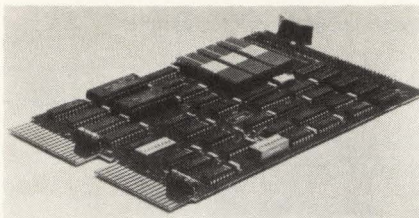


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CONTROL BOARD

18 Counting Modes, 16 Interrupts



The Codar M-Timer is a counting module that has 15 programmable counter/timers and 16 levels of user-definable interrupts. Designed for real-time data acquisition and industrial control applications, the M-Timer is implemented on a dual-wide LSI-II module, and is compatible with DEC LSI-II processors and the Micro-VAX I, as well as 68000 Q-Bus systems. The timer uses three Am9513 timing controllers and two Am9519A interrupt controller circuits. Each Am9513 contains five 16-bit counters. Price is \$875. **Codar Technology, Longmont, CO**
Write 197

DISK CONTROLLER

Q-Bus Compatible

The PM-DCV12 provides DEC RL02 emulation when used with SMD-interface Amcodyne 7110 cartridge disk drives. Memory addressing is 18- or 22-pin direct, with 32-bit error checking. A self-test function is activated on power-on. Each controller can accommodate one physical and four logical drive units. It accommodates sector capacities of 128 16-bit data words, and a formatted subsystem maximum capacity of 42 Mbytes. Price is \$1,950. **Plessey Peripheral Systems, Inc., Irvine, CA**
Write 195

CPU VME BOARDS

For Real-Time Industries Control

The CPU-1B and CPU-2 are CPU boards based on the 68000 microprocessor and the VMEbus. The CPU-1B board is a SMD based on the 68000 16/32-bit microprocessor, and available with an 8 MHz or 10 MHz processor unit. It has memory options of 128 Kbytes or 512 Kbytes of local dynamic RAM. The CPU-2 is designed for applications in real-time industrial control. It can be supplied with the 68000 or the 68010 and is available with an 8 or 10 MHz processor unit, has buyer-selectable dynamic RAM configurations. Prices are \$1,295 (CPU-1B) and \$1,795 (CPU-2). **Force, Santa Clara, CA**
Write 186

SMD DISK CONTROLLER

80186-Based

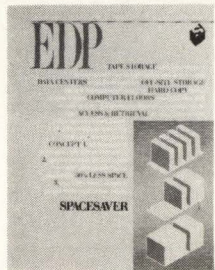
The CH-5643 controller handles four disk drives and conforms to the SMD interface. The controller has unrestricted 24 bit addressing with an 8 or 16 bit data bus and serial or parallel priority is standard. Defective mapping and transparent alternate selection of either tracks or sectors and an automatic dump and restore capability are included. The CH-5643 is based on the Intel 80816 bit microprocessor. The controller contains 16 Kbytes of PROM, 32 Kbytes of static RAM and a high speed sequencer. **Symbicon, Amherst, N.H.**
Write 189



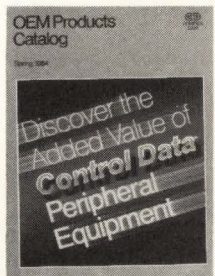
STD Bus Catalog. This 12-page catalog from Applied Micro Technology details STD Bus board and systems level products. Functions discussed are processor, memory, I/O, special function and video. Separate categories on its line of mainframes, disk subsystems, integrated systems, software and cables are included.
Applied Micro Technology Write 266



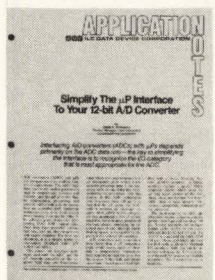
Instrumentation Catalog. This 36-page catalog from Honeywell Test Instruments Division describes their instrumentation product line. The catalog covers six groups; oscillographic recorders, imaging recorders, signal conditioning units, magnetic tape systems, industrial systems and special products. Photographs and descriptions are included.
Honeywell Write 252



High Density Storage Brochure. This 8-page brochure from Spacesaver Corp. covers high-density mobile storage systems in the EDP environment. The brochure provides information, graphics and system design for storage, including magnetic disk packs/cartridges, computer printouts, microfilm/microfiche, magnetic tapes and other related media.
Spacesaver Corp. Write 265



OEM Products Catalog. This 36-page catalog of peripheral equipment from Control Data contains information and specification charts for its flexible, 3 1/2", 5 1/4", 8" cartridge, and module family disk drives; intelligent standard interface; and 1/4" cartridge and 1/2" streaming tape drives. Covered are thin film heads, metallic media, vertical recording and automated material handling and manufacturing.
Control Data Write 270

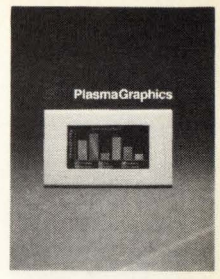


A/D Converters Application Note. This six-page application note from ILC Data Device Corp. discusses techniques for interfacing A/D converters with microprocessors for different data rates. The note points out that the key factor in simplifying the interface is to recognize the I/O category that is most appropriate for the ADC. It presents a study of interfacing the 12-bit ADC having conversion rates in the popular categories between 2 us and 100 us.
DDC Write 269

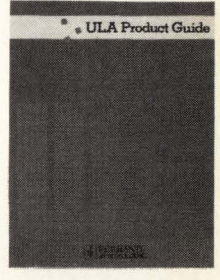


RG Chip Resistors Bulletin. This 4-page bulletin from the Resistive Products Division of TRW offers product specifications for its line of RG chip resistors. The bulletin includes performance data such as characteristics, limits, and test methods. Tape packaging specifications, ordering information, and color band identification is furnished through illustrations. Photograph and outline drawings which provide dimensional information are also included.
TRW Write 263

Plasma Display Brochure. This brochure from Plasma Graphics describes its 120 flat panel display. Features are self scan with memory, a 480 x 250 pixel matrix with 40 drives and 137 driver-to-panel interconnections. Also included are photos and a specification chart.
Plasma Graphics Write 267



Semiconductor Product Guide. This 16-page guide describes the ULA family of bipolar arrays from Ferranti Electronics. The family comprises gate arrays for systems of 100 to 10,000 gates, digilin arrays combining digital and linear functions on the same chip, and linear arrays. Descriptions include diagrams and specification charts. A separate price sheet is attached.
Ferranti Write 273



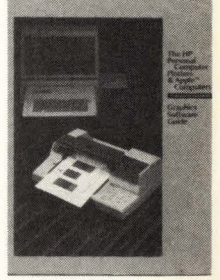
Keypads/Membranes Switches Brochure. This four-page brochure from Mantex Corp. describes products for designers and buyers of membrane keyboards and switches. Various construction and options are featured, such as tactile feel, PC board construction, embossing, associated microelectronics, complete assemblies and stock switches for prototype use.
Mantex Write 257



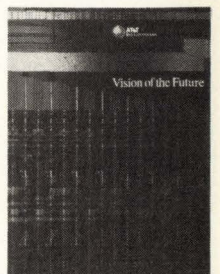
Electronic Materials Catalog. This 10-page catalog from Electro-Science Laboratories describes thick film materials cermet conductors, and resistors and dielectrics. Materials for surface mounting include solder pastes and organic adhesives, and the catalog also lists materials for packaging, hybrid circuits, flexible circuits, pc boards, optoelectronics, sensors and high frequency applications.
Electro-Science Write 255

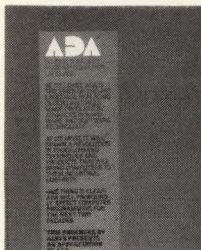


Graphics Software Guide. This guide from Hewlett-Packard Co. describes eight graphics-software packages, which enables Apple personal-computer users to produce charts and graphs on HP 7470A and HP 7475A graphics plotters. Each data sheet has a description of the software package, sample plots to illustrate the graphics capability, a list of hardware requirements and ordering information with the suggested retail price. Information on connecting the HP graphics plotters to the Apple IIe and Apple III is also provided.
Hewlett-Packard Write 253



Future Technology Report. This 48-page book from AT&T Bell Laboratories looks at the expanding power and availability of technology. Some of the topics discussed are selection and storage of information by intelligent machines, use of speech to operate machines, continued increase in the intelligence of microelectronic chips, fiber's capacity to carry more information, and advances in software systems that control computer equipment.
AT&T Write 272

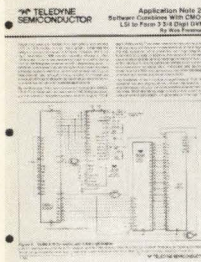




ADA Brochure. This 16-page brochure Alsys, Inc., discusses ANSI standard ADA computer language. It includes the history of the language's development, benefits of its use, and reasons for its probable adoption in both military and non-military applications.

Alsys

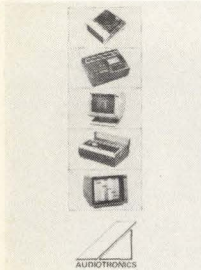
Write 254



DVM Application Note. This application note from Teledyne Semiconductor outlines a software and CMOS LSI combination that forms a 3 3/4 digit DVM. Application note 22 (AN-22) describes how a system's measurement range can be expanded by combining a 13-bit, microprocessor compatible CMOS LSI A/D converter with software and a CMOS display driver. The system can operate at speeds of up to 30 readings per second and allows interface functions to be performed by one LSI microprocessor interface chip.

Teledyne

Write 260



Audiovisual and Video Product Catalog. This 12-page catalog from Audiotronics Corp. describes its line of ATC computer and data monitors, CCTV video monitors, multi-image programmers, tape recorders, Tutorette audiocard readers and programs, record players, headphones, listening systems and accessories. Also contained are photos, specifications and prices.

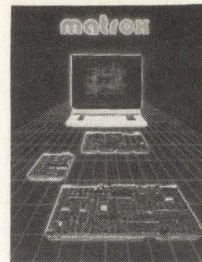
Audiotronics

Write 250

Boards and Systems Catalog. This 16-section catalog from Matrox Electronic Systems describes its line of boards, card cages, color monitors, keyboards, color graphics terminals and systems. Data provided includes descriptions, technical specifications, block diagrams, eight application notes and ordering information.

Matrox

Write 271



Trace Control Application Note. This ten-page application note from Gould, Inc., Design & Test Systems Division, describes its Trace Control feature developed for the K105-D logic analyzer. The note explains how Trace Control operates using a command language that permits which samples to save and those to disregard.

Gould

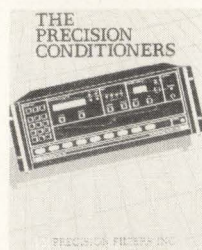
Write 259



Signal Conditioner Catalog. This 16-page summary catalog from Precision Filters, describes the company's line of electronic signal conditioners. Characteristics of ultra-high performance filter systems, frequency band translators, amplifiers and preamplifiers are described. The catalog offers system option and filter selection guides, and features comparison tables for gain ranging amplifier systems.

Precision Filters

Write 251



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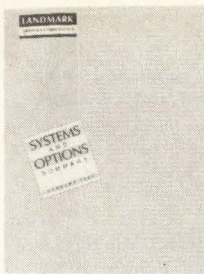
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- * Minimum four years on-hand digital experience on micro-mini computers, peripherals, data acquisition systems, micro-processor controlled test instruments
- * Trouble-shooting and repair capability to component level
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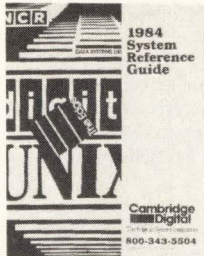
**University of Petroleum & Minerals
Houston Office
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Department 189
Houston, Texas 77057**



Systems and Options Summary Document. This document from Landmark Graphics Corp. is a Systems and Options Summary which describes three workstation configurations. Also described are options, third-party software, terms and conditions of sale, field support services, environmental requirements, and maintenance requirements.

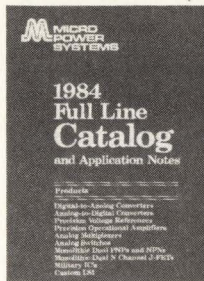
Landmark

Write 261



System Reference Guide. This sixty-page product catalog from Cambridge Digital Systems describes the company's DEC, NCR and UNIX-compatible systems and software. Chapters cover areas such as DEC and UNIX operating systems and layered products; fully integrated Q-bus, Uni-bus and Multibus systems and components; mass storage and tape drive subsystems; terminals and printers; and hardware and software support services. System configurations are described.

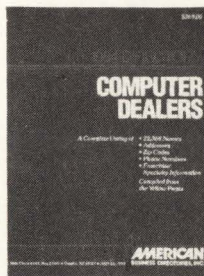
Cambridge Digital Systems Write 278



Product Catalog. This B/W catalog from Micro Power Systems contains nine sections of microcircuit product information for 1984. Products discussed are converters, D/A and A/D; precision operational amplifiers, analog switches and multiplexers and custom LSI. Diagrams, specifications charts, application notes and ordering information are also included.

Micro Power Systems

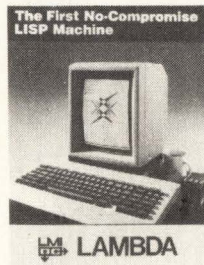
Write 264



Computer Dealers Directory. This Directory from American Business Directories, Inc. lists business names, addresses, zip codes, telephone numbers and franchise information for 22,368 computer dealers. Information, compiled from the Yellow Pages of telephone directories, is organized alphabetically by state and city.

American Business Directories

Write 277



LME Lambda Brochure. This 8-page brochure from LISP Machine Inc. describes the LMI Lambda computer and the software supplied with it. The LMI Lambda is a next-generation machine that can be configured with LISP and UNIX co-processors in a high-speed, multi-processor bus, enabling the two processors to execute concurrently.

LISP Machine

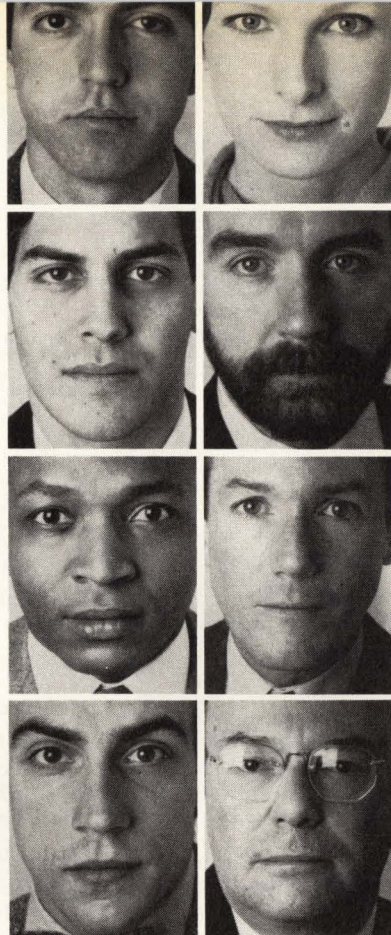
Write 276



Computer Supplies Catalog. This 82-page catalog and buyer's guide from Inmac lists over 2,500 computer-related supplies and accessories. Products include disks, ribbons, print wheels, paper, glare screens for video terminals and cables. Product descriptions feature photos, specifications and pricing information.

Inmac

Write 262



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Mini/Micro

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July 3-5

The European Computer Communications Conference & Exhibition. London, England. Contact: Online Conference Inc., Suite 1190, 2 Penn Plaza, New York, NY 10121. (212) 279-8890.

July 9-11

EUROSAM '84. Cambridge, England. Contact: Richard Jenks, T.J. Watson Research Lab., PO Box 218, Yorktown Heights, NY 10598. (914) 945-1233.

July 9-12

1984 National Computer Conference. Las Vegas, NV. Contact: AFIPS, PO Box 9658, Arlington, VA 22209. (703) 558-3613.

July 10-13

Database Management Systems - Mini, Micro and Distributed Applications Course. San Diego, CA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

July 11-15

The National Symposium and Workshop on Optical Platforms/Exhibit. Huntsville, Alabama. Contact: SPIE, PO Box 10, Bellingham, WA 98287. (206) 676-3290.

July 17-20

Designing with 16-Bit Micros Course. Washington, D.C. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

July 23-25

1984 Summer Computer Simulation Conference. Boston, MA. Contact: Dr. William D. Wade, Wade Engineering, PO Box 849, Huntington, NY 11743. (506) 271-6073.

July 23-27

1984 Joint International Symposium and Exhibition on Medical Images and Icons. Arlington, VA. Contact: Symposium on Medical Images, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

July 23-27

SIGGRAPH '84. Minneapolis, MN. Contact: Richard Mueller, Control Data Corp., PO Box 0, Mail Zone HQC02D, Minneapolis, MN 44330. (612) 853-5615.

July 24-27

Digital Image Processing Course. Washington, D.C. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

July 30-August 2

7th International Conference on Pattern Recognition. Montreal, Canada. Contact: ICPR Secretariat, 3450 University St., Montreal, Que., Canada H3A 2A7. (514) 392-6744.

July 31-August 3

Database Management Systems - Mini, Micro & Distributed Applications. Washington, D.C. Contact: Integrated Computer Systems, PO

Box 45405, Los Angeles, CA 90045. (213) 417-8888.

August 6-8

Personal Computers in Business and Government - The Micro-Mainframe Connection. Washington, D.C. Contact: National Institute for Management Research, PO Box 3727, Santa Monica, CA 90403. (213) 450-0500.

August 14-16

Database Administration and Data Resource Development. Boston, MA. Contact: Software Institute of America, Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

August 19-24

28th Annual International Technical Symposium on Optical and Electro-Optical Engineering/Instrument Display. San Diego, CA. Contact: SPIE, PO Box 10, Bellingham, WA 98227. (206) 676-3290.

September 16-20

Compeon Fall '84. Arlington, VA. Contact: Compeon Fall '84, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

September 26-28

Eurocon '84, Sixth Conference on Electro-technics: Computers in Communication and Control (IEEE et al.). Tokyo, Japan. Contact: F. Harashima, Institute of Industrial Science, University of Tokyo, Roppongi, Minato-ku, Tokyo, 106 Japan. Tele. 03-402-6231.

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