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NOVEMBER 12, 1987

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Special show preview: Wescon/87

Interface a real-time clock chip to a host computer

Minicartridge tape drives

Use a fast 16-bit DAC in a CD player

ISDN stirs up a storm of telecomm-IC activity

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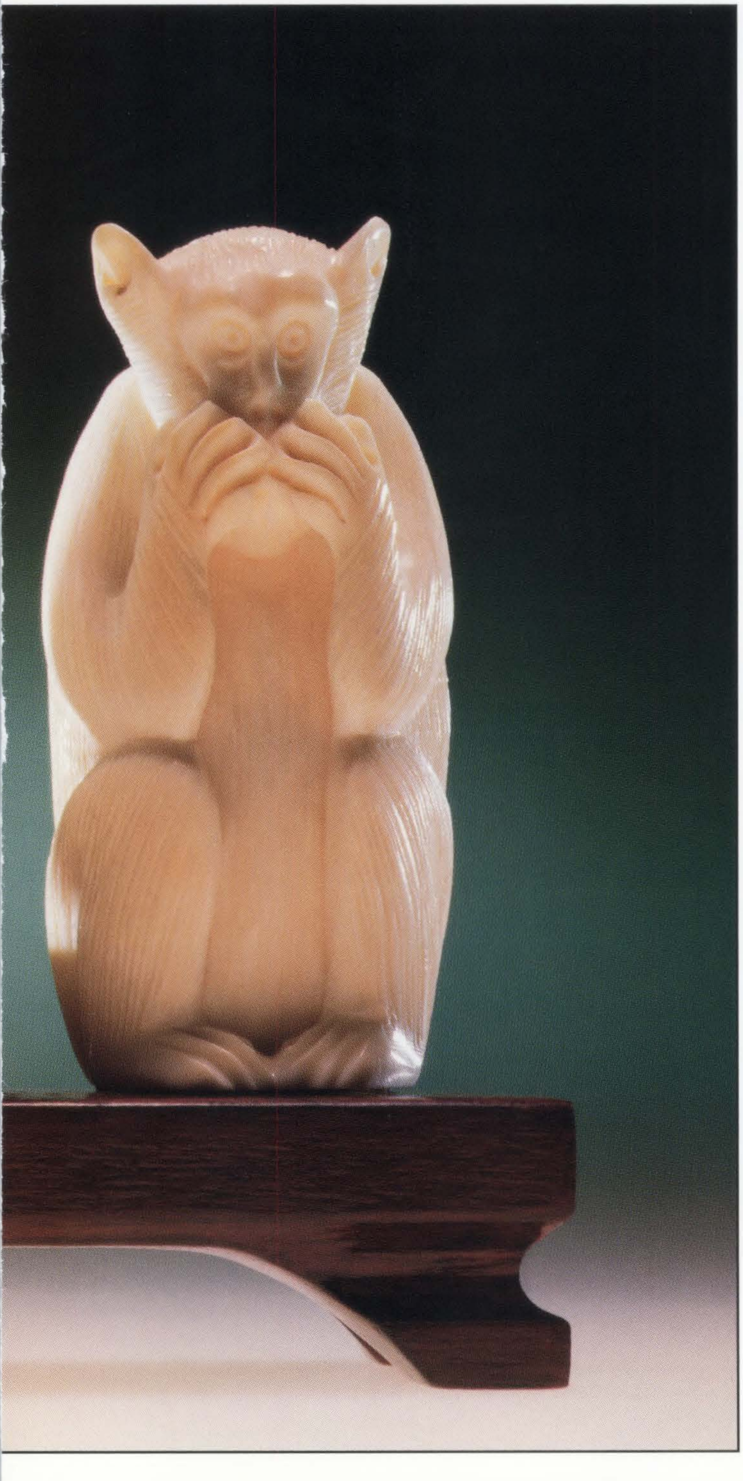

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CIRCLE NO 306

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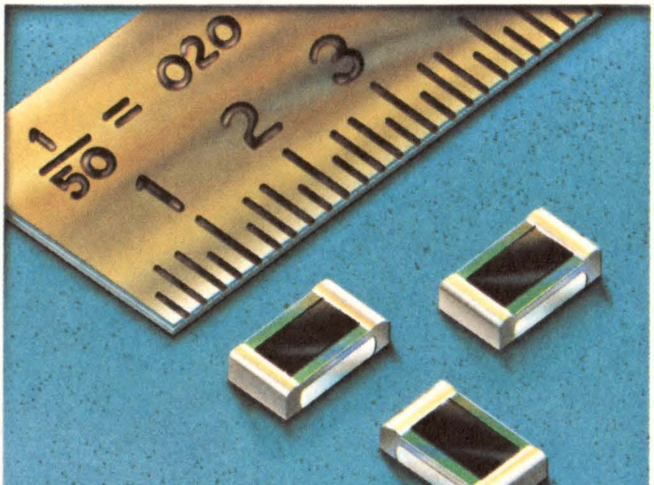

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For complete information: **402-371-0080**

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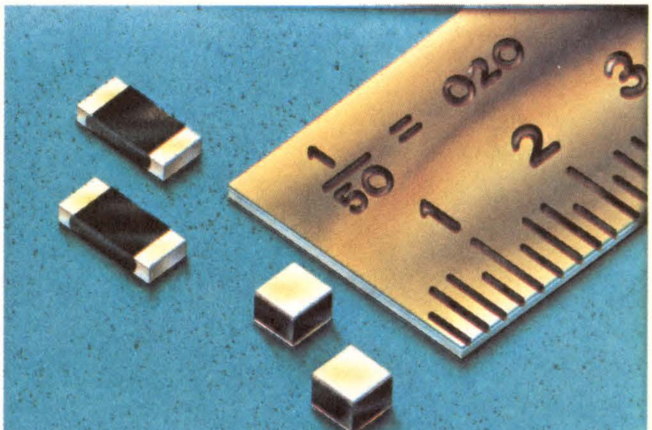

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SPECIFICATIONS

FREQ. RANGE	dc-4.6 GHz	
INSERT. LOSS (db)	typ	max
dc-200MHz	0.9	1.1
200-1000MHz	1.0	1.3
1-4.6GHz	1.3	1.7
ISOLATION (dB)	typ	min
dc-200MHz	60	50
200-1000MHz	45	40
1-4.6GHz	30	23
VSWR (typ)	1.3:1	
SW. SPEED (nsec)		
rise or fall time	2(typ)	
MAX RF INPUT (dBm)		
up to 500MHz	+17	
above 500MHz	+27	
CONTROL VOLT.	-8V on, OV off	
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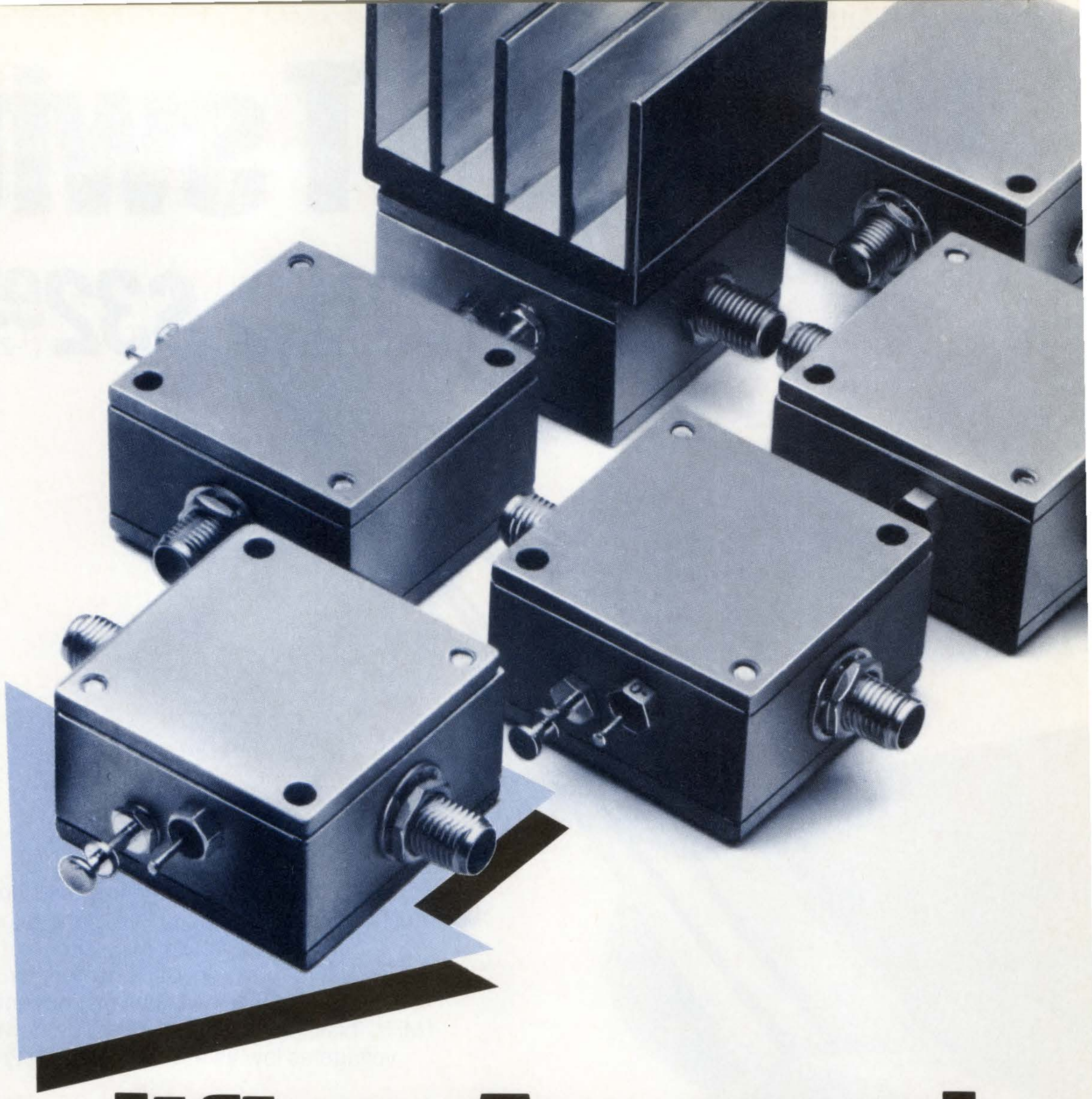
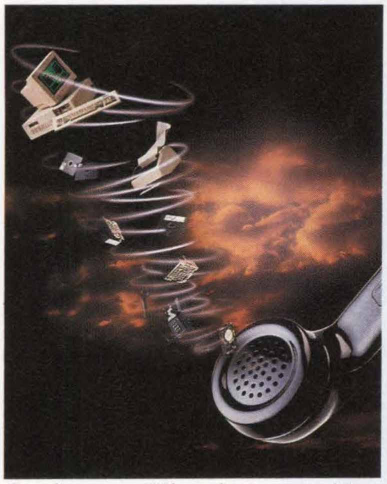


EDN

Volume 32, Number 23 November 12, 1987

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *When the Integrated Services Digital Network becomes a reality, the world telephone network will be exclusively digital. This transformation will create a whirlwind of business for suppliers of telecomm equipment. See pg 118. (Photo courtesy Intel Corp)*

DESIGN FEATURES

Continued on page 7

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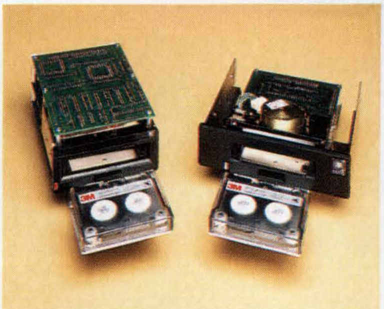

The capacity and access times of minicartridge tape drives continue to increase, but the peripherals' drive interfaces and data formats are still incompatible, and the market remains highly volatile (pg 63).

DESIGN FEATURES *(Continued)*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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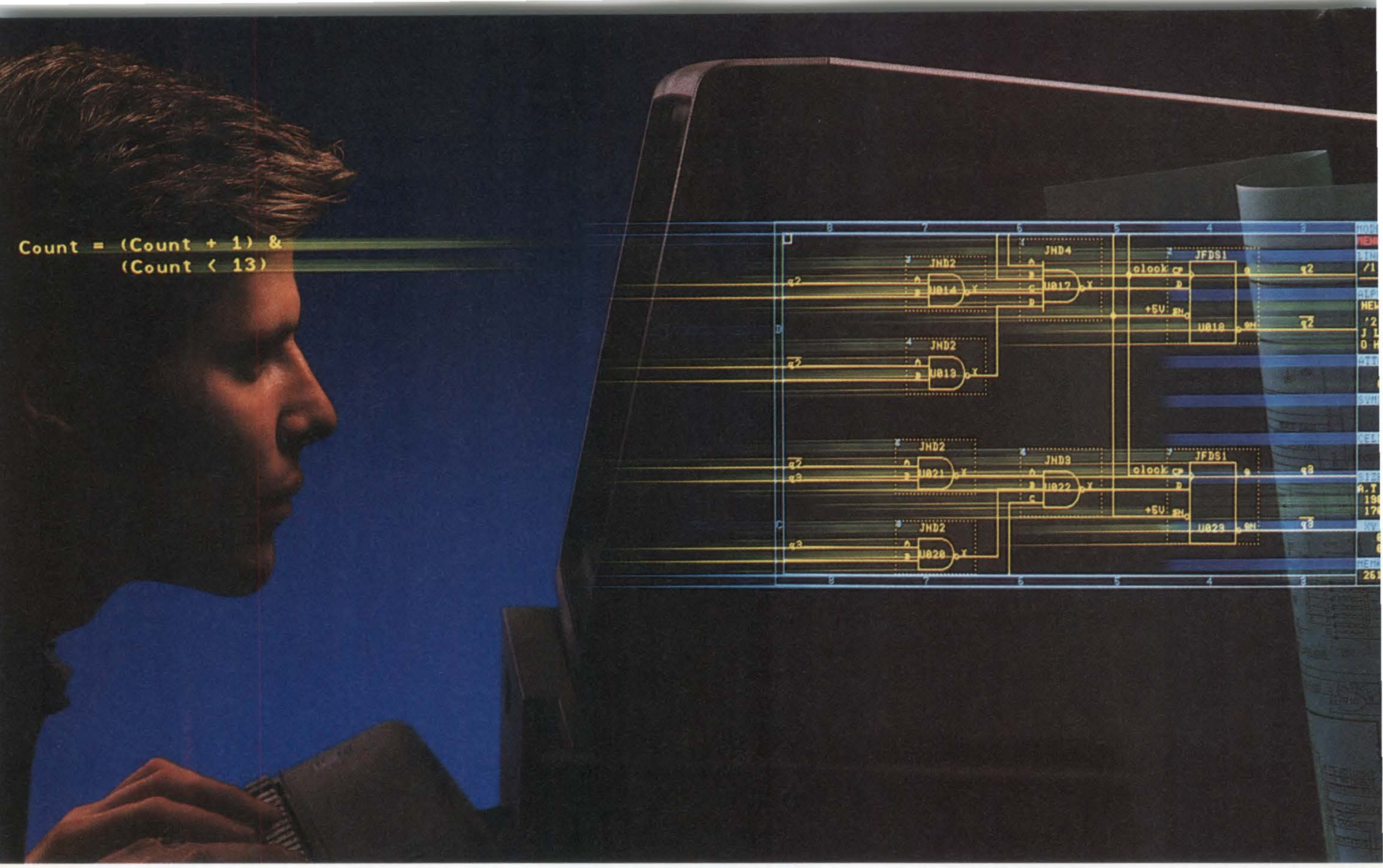

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Continued from page 7

EDITORIAL 57

Although purchasing Fairchild leaves National with expanded markets, it's worth looking at other aspects of the deal.

NEW PRODUCTS

PROFESSIONAL ISSUES 411

Software developers tussle over the "look and feel" issue.—*Richard Beutel, Washington, DC*

LOOKING AHEAD 429

UPS shipments to grow at 20% per annum. . .Color enriches hard-copy-output markets.

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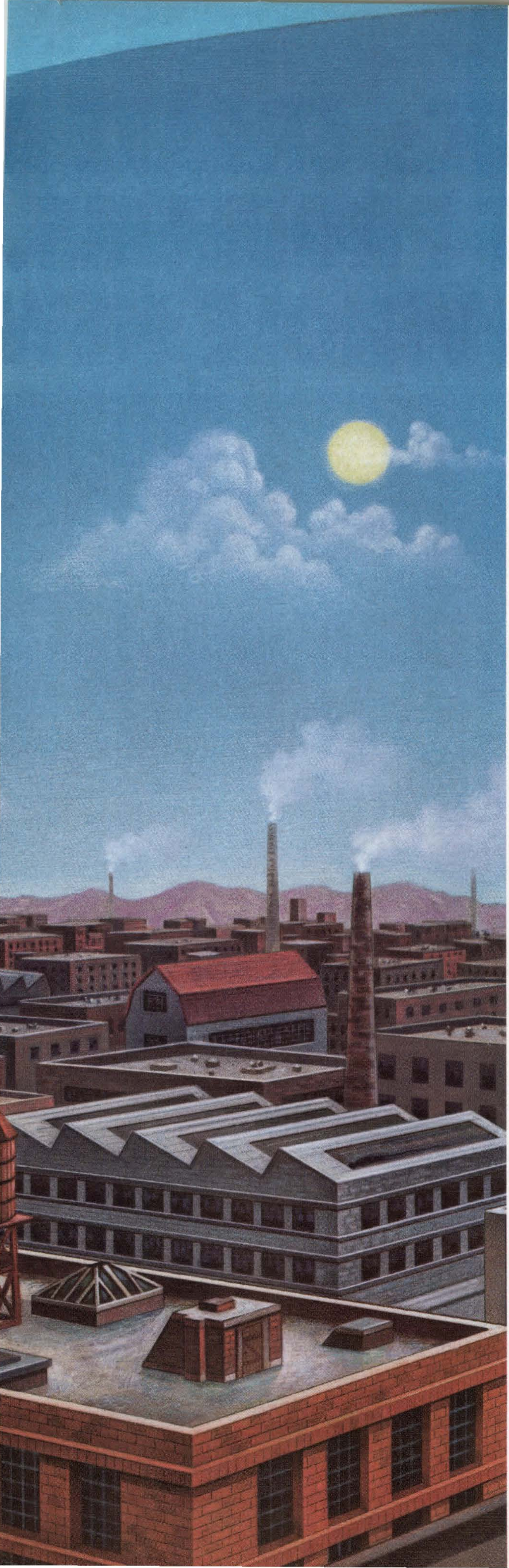

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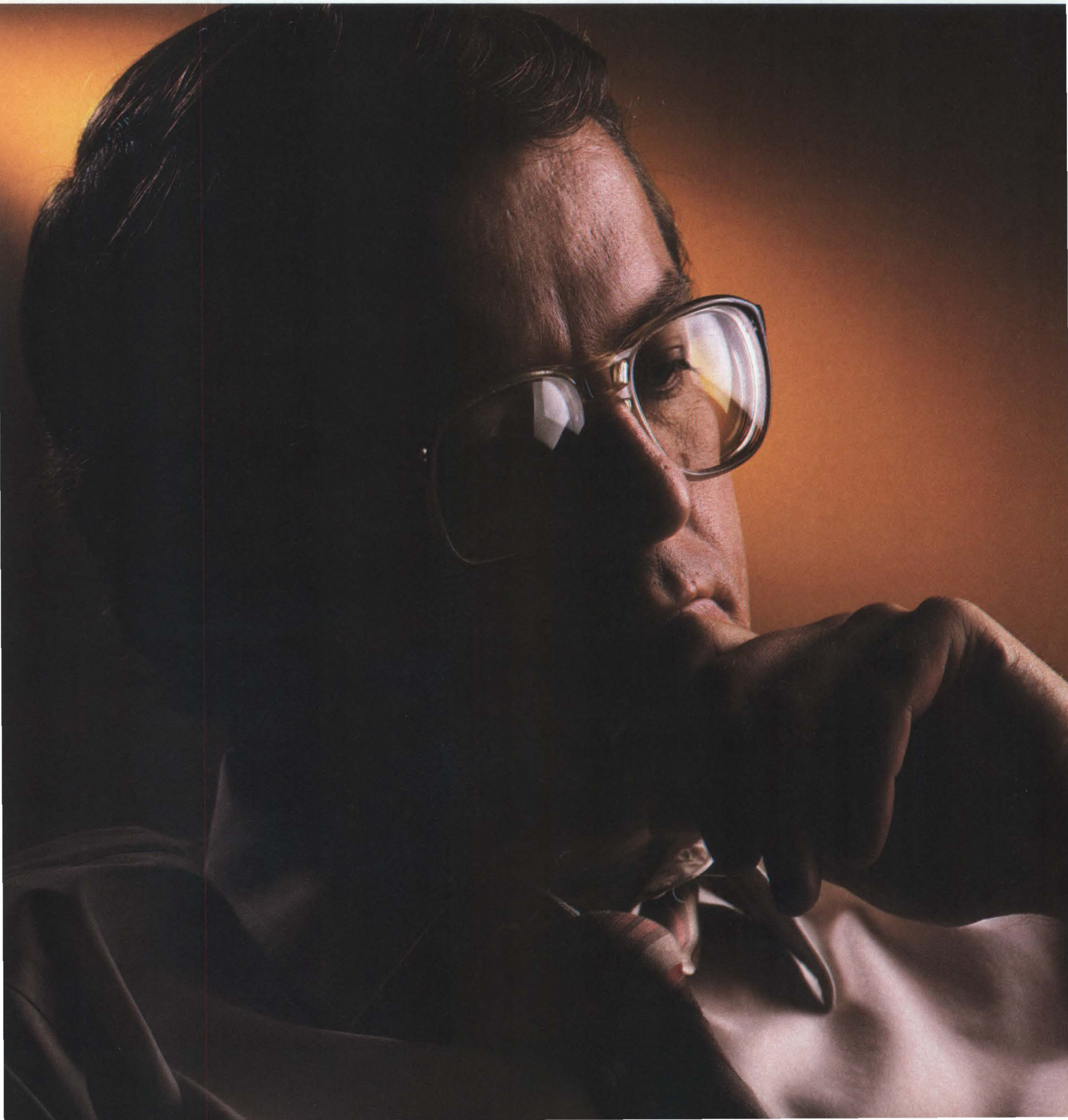
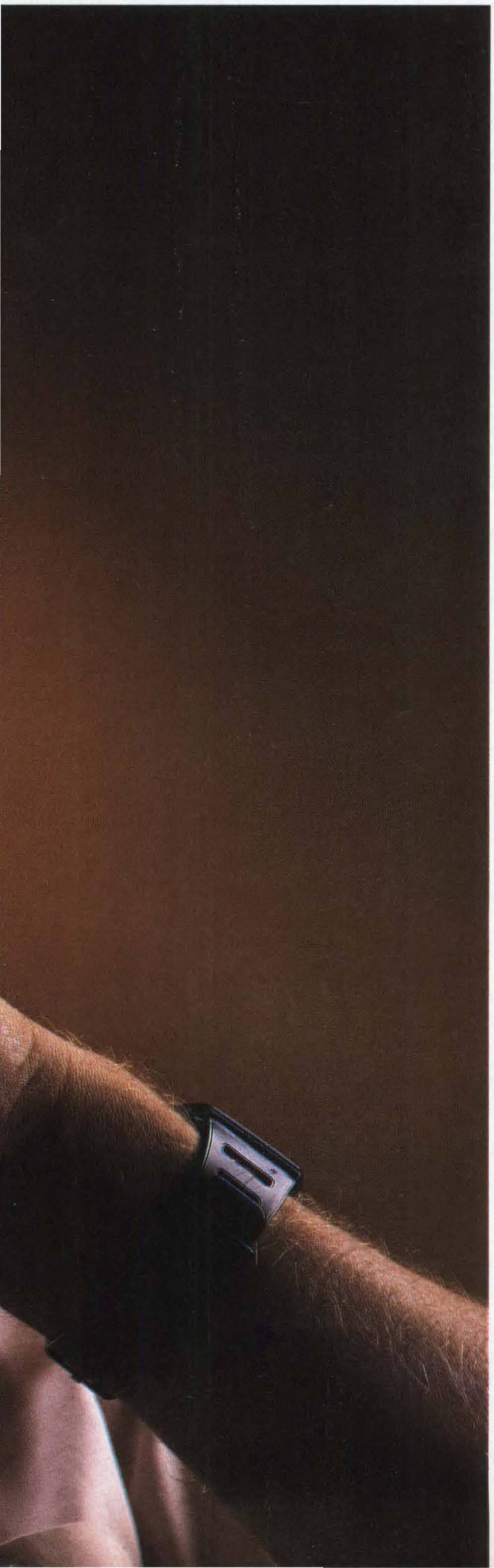
CIRCLE NO 227

"ASICs CREATE A
SET OF TEST PROBLEMS.
WE NEED A WHOLE NEW



WHOLE NEW DOESN'T THAT MEAN TEST STRATEGY?"



IT SURE DOES.

It's easy to see that the tremendous potential of ASICs has only just begun to be tapped. What's not so evident is the fact that developing these unique ASIC devices carries with it some unprecedented test problems. Problems that traditional test approaches and traditional ATE simply are not equipped to handle.

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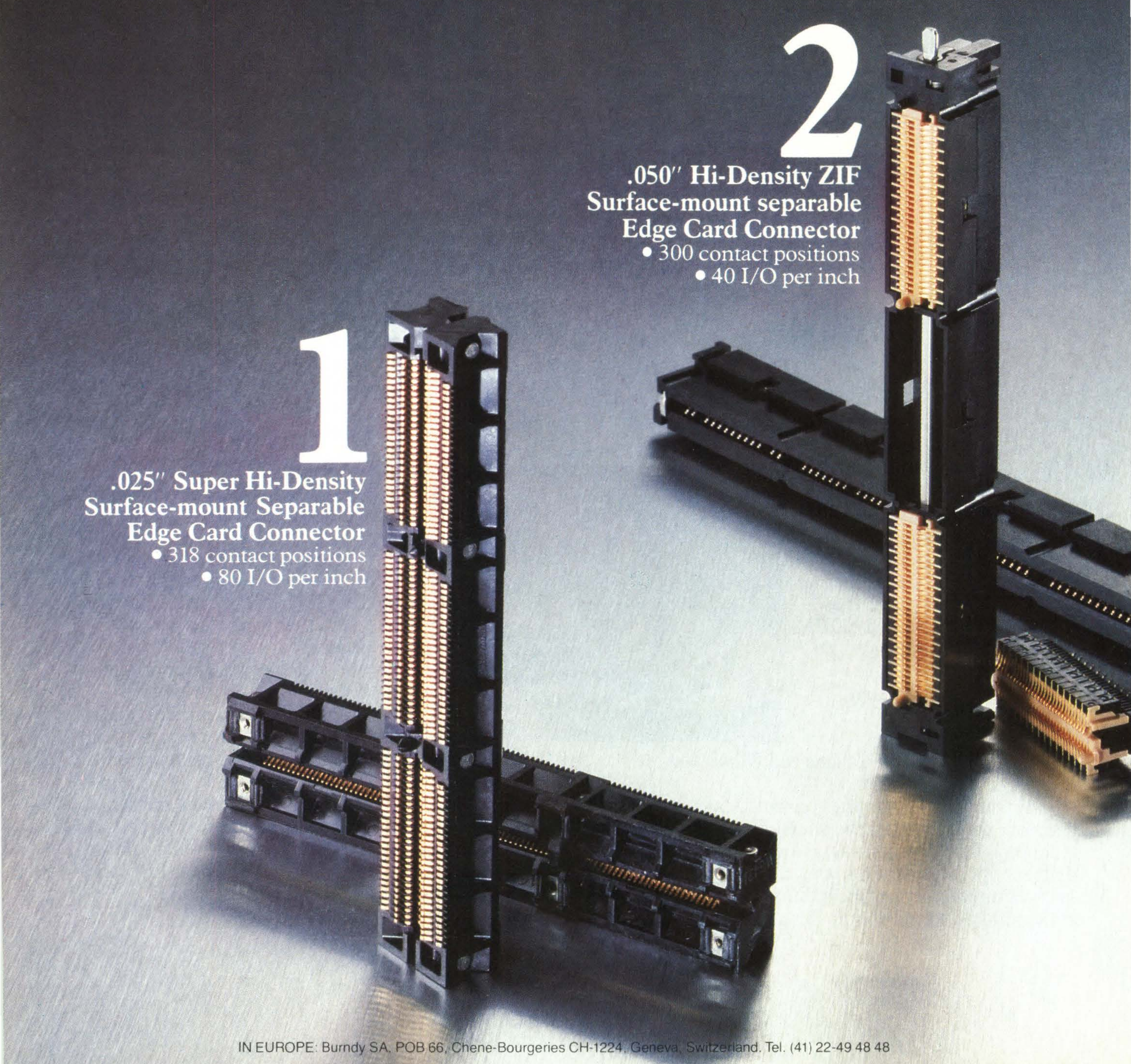

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NEWS BREAKS

EDITED BY JOANNE CLAY

8-BIT ADC AND 12-BIT DAC OFFER FAST CONVERSION SPEEDS

The TKAD20C from Tektronix Inc (Beaverton, OR, (503) 627-2515) combines an 8-bit ADC with a track-and-hold circuit, allowing you to sample a 125-MHz waveform at 250M samples/sec with 7-bit accuracy, including the effects of harmonic distortion, noise, and aperture jitter. Its 50Ω input impedance and 3-pF input capacitance allow the device to follow high-speed signals. The digital outputs are available as 8 bits at 250 MHz or 16 bits at 125 MHz. The device comes in an 84-pin ceramic package and costs $750 (100). The TKDA20H, also from Tektronix, is a 12-bit DAC with a settling time under 30 nsec. This device features complementary voltage and current outputs for applications requiring negative as well as positive signal values. You can also use the TKDA20H as a multiplying DAC for signals as high as 10 MHz. $500 (100).—Doug Conner

CMOS MICROPROGRAMMABLE μP OPERATES ON 145 mW

Although the CMOS SN74ACT29116 from Texas Instruments (Dallas, TX, (800) 232-3200) has the same pinout and functions as AMD's 29116 microprogrammable μP, the TI device operates at a 100-nsec cycle time with a mere 145 mW instead of the 2.8W consumed by the bipolar 29116. In addition, the processor features a 30-μW standby mode. If you need a little more speed, consider using the -1 version, which features an 85-nsec cycle time. The SN74ACT29116 and SN74ACT29116-1 cost $50.40 and $62.50, respectively.—Steven H Leibson

FAST, HIGH-CAPACITY HARD-DISK DRIVE INCLUDES ESDI OR SCSI

Miniscribe (Longmont, CO, (303) 651-6000) has jumped into the high-performance, hard-disk-drive market with its 9000 Series 5¼-in. drives. The first two products in the series, the ESDI versions of the 9230 and the 9380, store 203M bytes and 338M bytes, respectively; the corresponding SCSI versions store 207M and 347M bytes. Both drives feature a 16-msec average access time and a 30,000-hour MTBF rating. The clamshell casting common to all drives in the series makes robotic assembly easier. The 9230 and 9380 cost $1400 and $1900 (1000), respectively.—Steven H Leibson

ELECTRONIC TIMER LETS YOU PRESET INTERVAL FOR SOFTWARE USE

To prohibit unauthorized use of your software program, yet allow potential customers to try or lease the program, consider using the DS1207 Electronic TimeKey from Dallas Semiconductor (Dallas, TX, (214) 450-0400). The TimeKey contains a self-erasing memory that you can set to expire from one day to two years after the end user first accesses data from its memory. A microchip in the TimeKey contains critical data that's necessary to run your disk-based application program. The TimeKey plugs into the DS1255 KeyRing, which, in turn, plugs into the parallel port of the customer's IBM PC or compatible computer; it doesn't interfere with normal printer operation. The TimeKey costs $10 (100).—J D Mosley

SINGLE-CHIP GRAPHICS CONTROLLER EMULATES EGA

The GC201 multimode graphics controller from G-2 Inc (Milpitas, CA, (408) 943-0224) incorporates most of the circuitry required to implement a graphics subsystem that emulates IBM's Enhanced Graphics Adapter (EGA) for the PC, as well as IBM's Color Graphics Adapter (CGA) and Monochrome Display Adapter (MDA), and Hercules Computer Technology's Monochrome Graphics Card. To create a complete EGA subsystem with the chip, you need only add video RAM, a BIOS EPROM, and a 74LS244. The IC costs $31 (10,000). The company offers a $149 evaluation kit consisting of an EGA card (for the IBM PC) that has a GC201 on board.—Steven H Leibson

NEWS BREAKS

PC-BASED AUTOROUTER EMPLOYS THREE ROUTING ALGORITHMS

Pathfinder, an IBM PC-based pc-board design system from Bishop Graphics (Westlake Village, CA, (818) 991-2600), features an autorouter that uses the same three routing algorithms used in high-end autorouters. The algorithms—probe, exhaustive search, and rip up and reroute—are user-selectable. In addition, the autorouter offers true first-time (or nonchamfered) 45° routing. To use the autorouter, you need the company's proprietary, 68000-based coprocessor board. You can route boards of as many as 16 layers on a 25- or 12-mil grid, so you can squeeze as many as three 6¼-mil traces between DIP leads. The Pathfinder software sells for $1995; the standard autorouter software, with a 1M-byte, 8-MHz coprocessor board, costs $2995. The XL autorouter version, which has seven times the speed of the standard autorouter, is based on a 4M-byte, 25-MHz coprocessor board; it costs $5995.—Margery S Conner

SPEEDY, 5¼-IN. WORM DRIVE STORES 654M BYTES

Featuring a 75-msec average access time and a 1.5-msec track-to-track seek time, the 5¼-in., full-height Laserdrive 510 WORM (write-once, read-many) optical disk drive from Laser Magnetic Storage (LMS, Colorado Springs, CO, (303) 593-7900) can place 327M bytes on one side of its ANSI-compatible cartridge. Thus, the $95, dual-sided cartridge stores 654M bytes. The drive, which costs $2880, sustains a transfer rate of 600k bytes/sec over its SCSI interface, and it can support a 1.5M-byte/sec burst rate from its 64k-byte buffer. LMS selected sampled-servo WORM recording for the drive; the company claims this approach allowed it to integrate the drive's electronics with the optics more easily, to relax design specifications for some components, and to create a self-calibrating design.—Steven H Leibson

LOW-POWER TRACK/HOLD AMPLIFIER OFFERS 1-μSEC ACQUISITION

Requiring half the power that other 12-bit track-and-hold amplifiers need, the CS3112 from Crystal Semiconductor (Austin, TX, (512) 445-7222) dissipates a maximum of 200 mW. Using a RAM-based calibration scheme that automatically limits all internal dynamic and dc errors to less than 700 μV, the CS3112 maintains 12-bit accuracy throughout its operating life. Its on-chip hold capacitors confine droop to 0.001 μV/μsec. The device limits aperture jitter to 100 psec. Prices start at $8.90 (100); sample quantities are currently available from stock.—J D Mosley

CUSTOM-POWER-SUPPLY VENDOR UNVEILS FOUR STANDARD MODELS

After years of designing and supplying custom power supplies, the Components Group of Zenith Electronics Corp (Glenview, IL, (312) 391-8700) has jumped into the standard-power-supply market with four switch-mode offerings. The ZSP-40, -250, -300, and -400 supply 40, 250, 300, and 400W, respectively, and cost $45, $340, $355, and $405, respectively. The three larger power supplies feature onboard filtering designed to meet VDE 0871/Class B requirements and FCC Part J EMI requirements, and the ZSP-40 meets Class A specifications. They also feature four isolated outputs with magnetic-amplifier regulation on the three auxiliary outputs. You can adjust the primary output on the larger supplies from 4.5 to 5.5V; two of the auxiliary outputs supply 10 to 15.5V, and the fourth output furnishes 4.75 to 5.25V. The ZSP-40 has three fixed supply voltages of 5V and ±12V. All supplies satisfy UL/CSA/IEC 380 and VDE 0806 safety requirements.—Steven H Leibson

CHIP SET CARRIES ISDN ON EXISTING SUBSCRIBER LINES

By using adaptive-filter DSP techniques to perform echo cancellation at each end of a telephone line, the PCB2390 chip set from Philips's Elcoma Div (Eindhoven, The Netherlands, TLX 51573; Signetics Corp, Sunnyvale, CA, (408) 991-4571) allows existing 2-wire subscriber wiring to carry ISDN (Integrated Services Digital Network) information over distances as great as 8 km.

The chip set allows for full-duplex transmission of two 64k-bps B channels of encoded voice or data and a 16k-bps D channel of signaling and low-speed data. It complies fully with the West German PTT's U_{KO} specification for the CCITT U interface. In addition to its U interface, the chip set has an industry-standard IOM (ISDN-oriented modular) interface to connect it to circuits that implement other CCITT interface points. The 2-chip CMOS implementation of the PCB2390 currently costs around $80, but its price is expected to fall to $50 by the end of 1988. A single-chip version is under development.—Peter Harold

PLASTIC CONSTRUCTION PROVIDES LOW-COST PGA PACKAGES

Manufactured from pc-board laminates with conventional pc-board technology, plastic pin-grid array packages from Tectonic Products Ltd (Wokingham, UK, TLX 847569) provide a low-cost alternative to ceramic types. The 100-pin package currently costs around £5, but its price is expected to fall to around £2.5 (10,000) within two years. By employing multilayer interconnect patterns and buried vias, the company has already prototyped packages with as many as 300 pins.

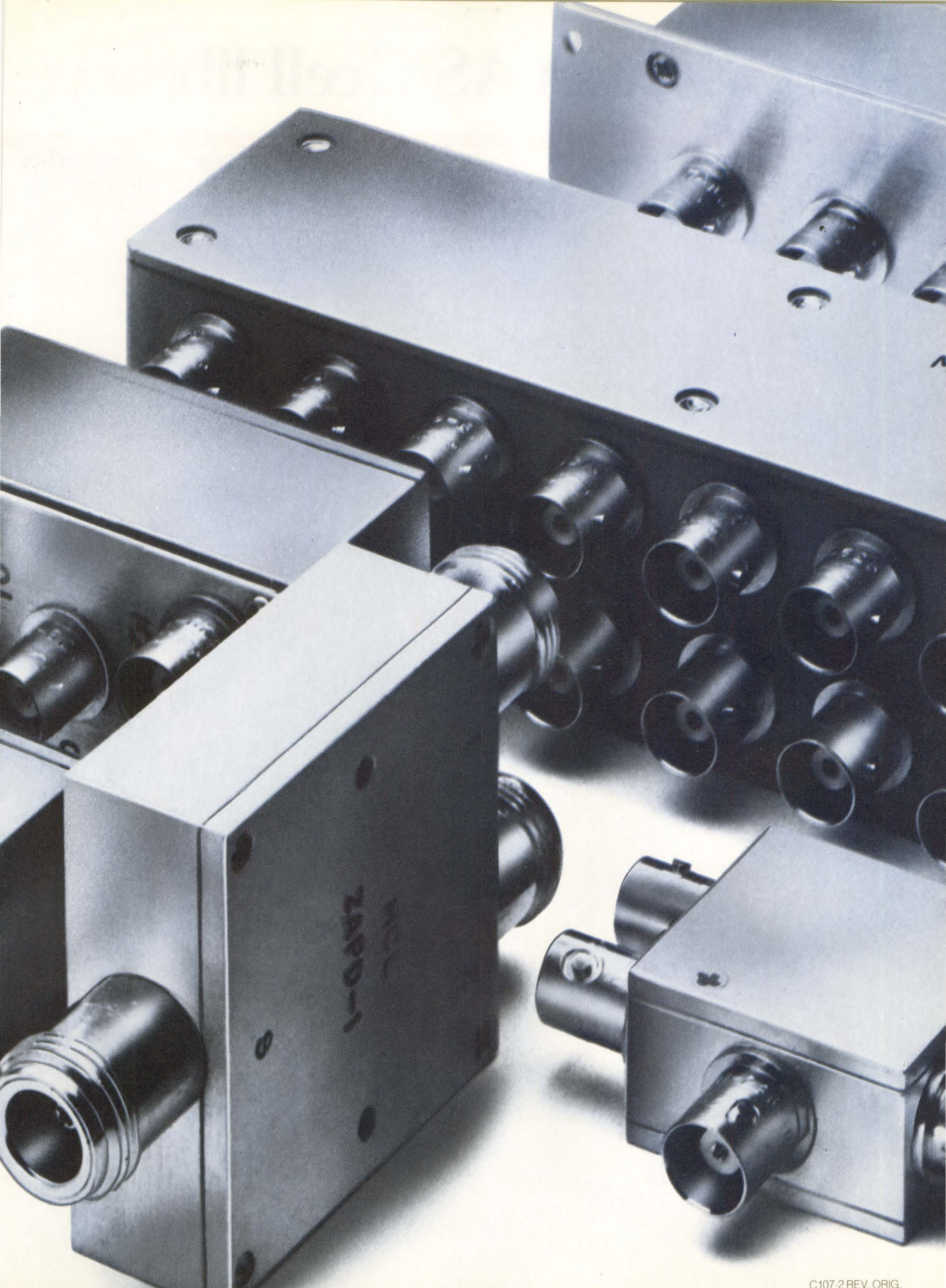
In addition to providing a standard range of packages that are plug-compatible with ceramic PGAs, the company can also provide custom versions. For example, you can order a PGA with pins mounted underneath the semiconductor die; this arrangement allows you to use the entire undersurface of the package for the device's pinout. You can also order a package that incorporates heat sinks.—Peter Harold

32-BIT PERSONAL COMPUTER RUNS JAPANESE OS/2, MS-DOS 3.1

The 80386-based PC-98XL2 personal computer recently introduced by NEC is the first to run the Japanese-language version of Microsoft's OS/2 operating system. The computer also runs MS-DOS version 3.1, and it's compatible with the company's PC-9800 Series. The system has 1.5M bytes of user memory, and it offers a 5.25k-byte dual-port graphics RAM; a 40M-byte, 5¼-in. hard-disk drive; and two 1M-byte, 5¼-in. floppy-disk drives. It sells for ¥988,000 or $6914.—Joanne Clay

OPTICAL TRANSMISSION MODULE OPERATES AT 2G BPS

Hitachi has introduced an optical transmission module that operates at 2G bps. The module incorporates a semiconductor laser and has a gallium-arsenide (GaAs) drive circuit. Samples of two versions are currently available. One model uses a Fabry-Perot-type laser to transmit over a distance as great as 30 km; it costs $4414. The other uses a distributed-feedback laser, which allows it to send information over more than 40 km; it sells for $8483.—Joanne Clay



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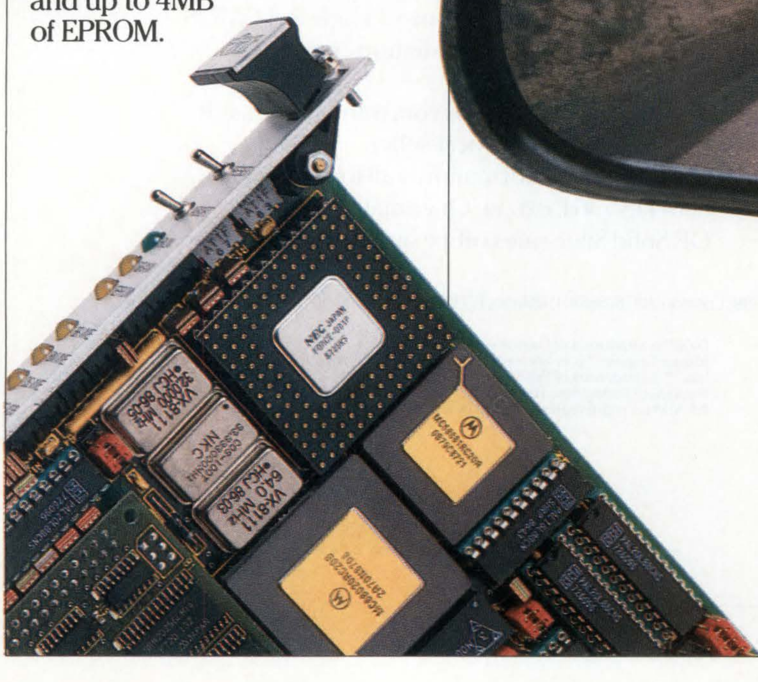

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ZERO-WAIT-STATE SRAM	1MB
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EEs can use their talents in nonmilitary endeavors

I write in response to the anonymous letter in the August 20 issue of EDN, in which the writer bemoans the sorry history of his engineering career—nine layoffs in 29 years, frequent relocations, no retirement equity, and inefficient use of his time. He concludes that he would not advise anyone to choose engineering as a career.

The writer views engineering first as a way to make money and second as a potentially challenging position. He disdains one who works "with a nonprofit foundation or social-service organization, no matter how useful and needed it is, unless the social work is more important to him than income is." The product of his work, and its potential benefits or damage to society, is irrelevant to him. The writer's problem is with military engineering, not engineering in general.

What kind of profession have we become? Have our values deteriorated to the point that money is all-important? If designing instruments for war is the most lucrative job, do we choose that—and then complain because the Pentagon dole is occasionally erratic? If that is engineering, then I am ashamed to be an engineer.

Our nation—indeed, the entire human species—is faced with mammoth problems. In health care, housing, nutrition, transportation, energy, communications, education, and other areas, engineering can be of enormous help toward improving our quality of life. Yet our government pours a million dollars a minute into machinery for death. America's economy and industrial infrastructure are collapsing; half our engineers and technicians work for the military, while our consumer electronics, cars, steel, and other products can't compete on the world market. If that anonymous correspondent hasn't been as successful as he would like in getting his piece of that torrent, perhaps he should be putting his skills to better use.

At the least, he should understand those who use their time and talents to help their fellow humans. Not all of us are single-minded enough to pursue our economic security as part of the most deadly war machine the world has ever seen, regardless of the consequences.

Charles Scheiner
President
Peaceful Systems
White Plains, NY

Check your math

Thank you for the September 3 publication of my article "Low-cost

Text continued on pg 38

TEK UNIX-BASED WORKSTATIONS

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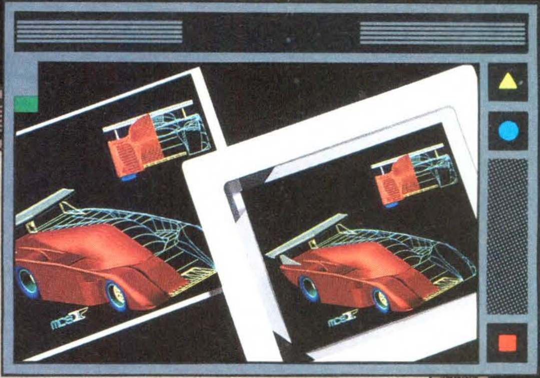

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CIRCLE NO 211

quad op amps boost circuit performance" (pg 213). An error appears in that article on pg 215 in the last three lines of the second paragraph. What twice appears there as $\sqrt{2}$ should be $1/\sqrt{2}$.

Jerald Graeme
Burr-Brown Corp
Tucson, AZ

Gate-array update

Please make the following corrections to EDN's gate-array directory, which begins on pg 134 of the June 25 issue. The address given on pg 185 for Motorola Inc is incorrect. The current address is Motorola Inc, ASIC Div, 1300 N Alma School Rd, Chandler, AZ 85018; phone (602) 821-4426.

Further, the Motorola entry in the table of MOS digital arrays (pg 146) lists some old information. The CMOS gate arrays currently available are the HCA62A00 Series. The company no longer makes 3-μm CMOS gate arrays.

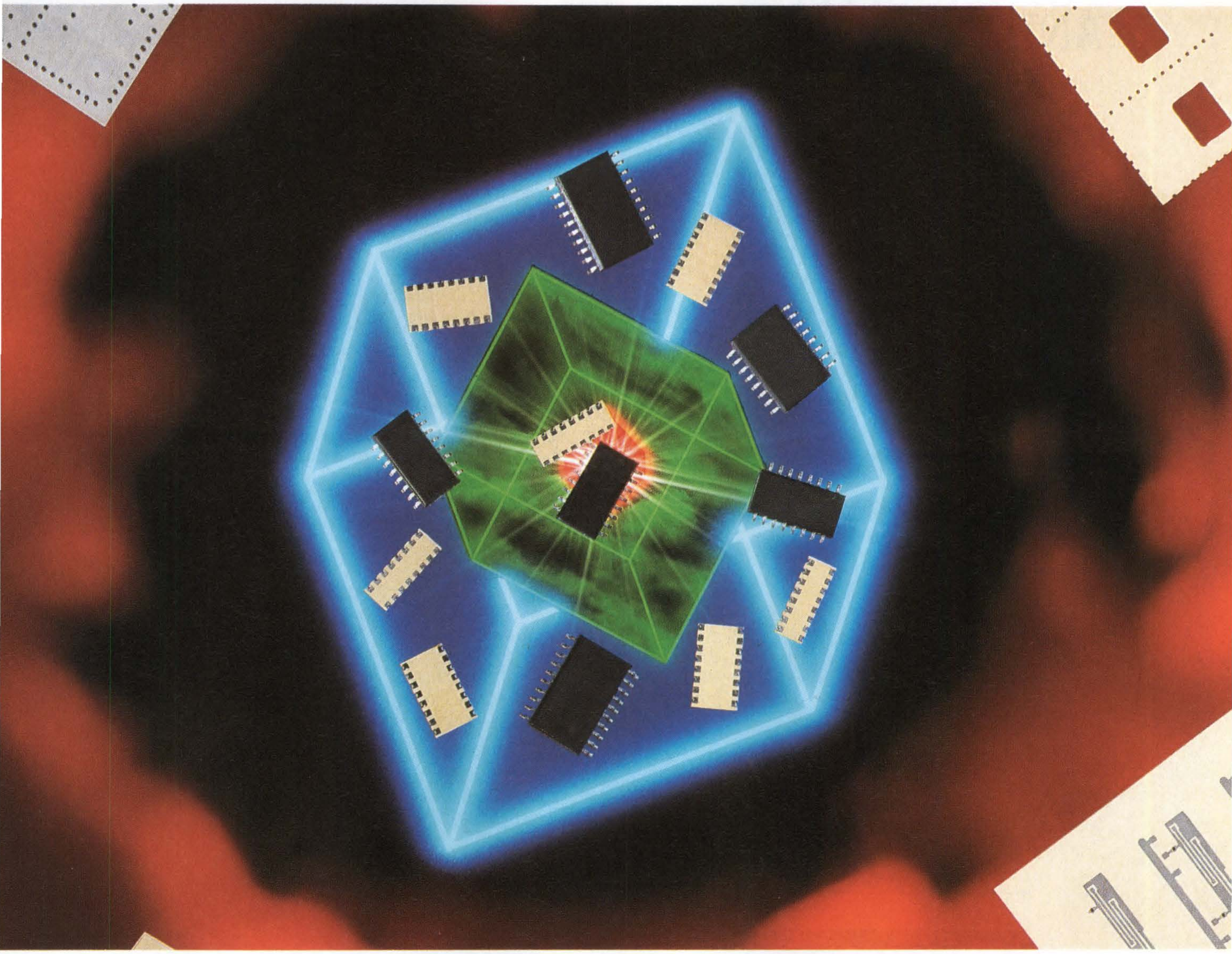
Correction

The Technology Update entitled "Automatic test generators for PLDs clean up your logic designs" lists an incorrect address for Structured Design Inc. The company's current address is 333 Cobalt Way, Suite 107, Sunnyvale, CA 94086; phone (408) 736-2191.

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

NEW CIRCUIT TECHNOLOGY.



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CIRCLE NO 210

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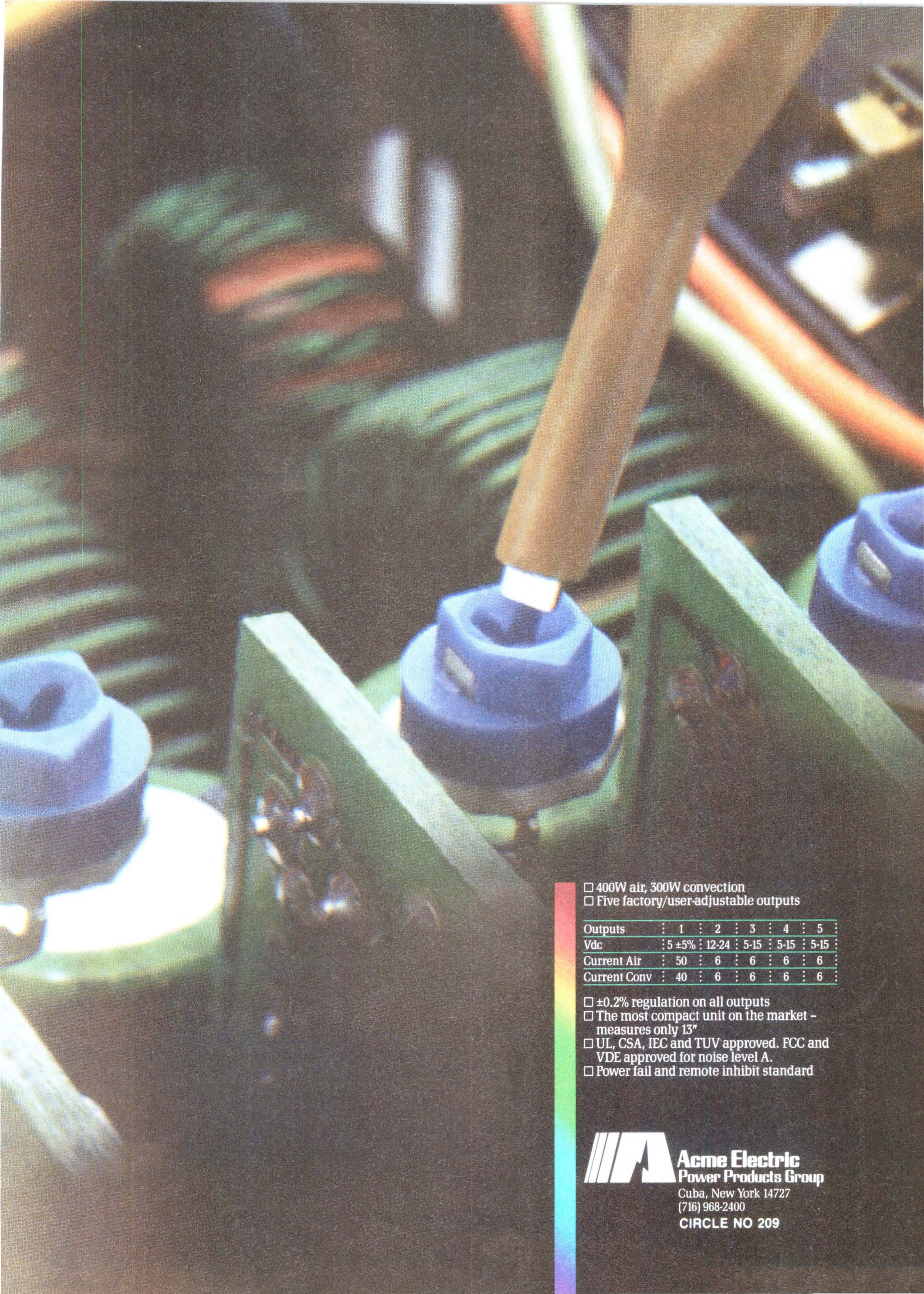
□ 400W air, 300W convection
□ Five factory/user-adjustable outputs

Outputs	1	2	3	4	5
Vdc	5 ±5%	12-24	5-15	5-15	5-15
Current Air	50	6	6	6	6
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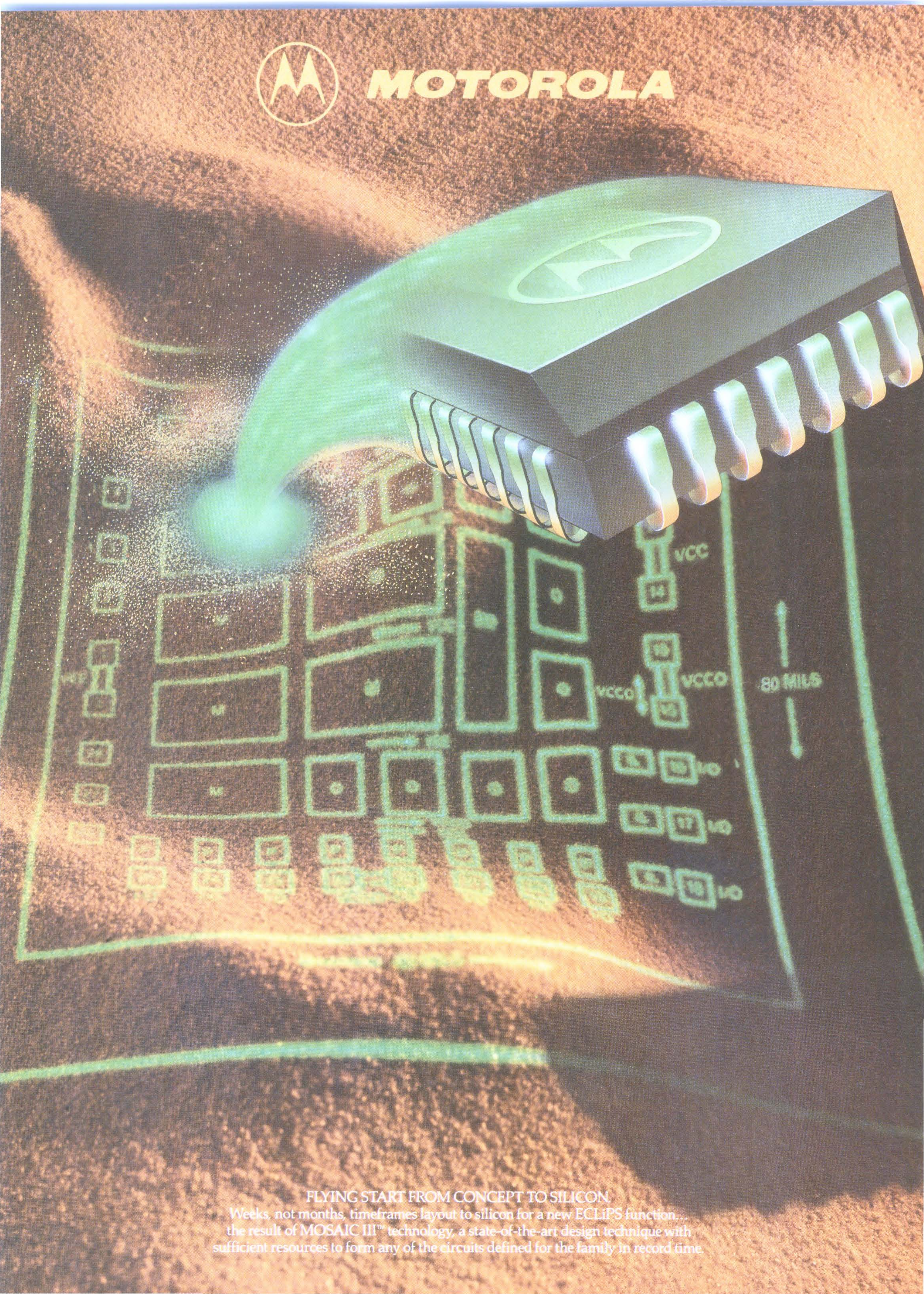
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Speed-ns Gate-tpd (typ.)	0.33	1.0	0.75/0.95*
F-F Toggle MHz (min.)	600	250	350
Pwr Dissipation mW/gate	35/32**	35	44/40**
Speed-Power Product-pJ	11.5/10.5**	35	42/30**
Edge Speed Tr, Tf-ns	0.5	1.0	0.7

* Flat/DIP package
** V_{EE}=-5.2V/-4.5V

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MC10/ MC100	Function	Features	Output Type	General Sampling
E111	1:9 Differential Clock Driver	Low Skew, Enable, Vbb	Diff.	Now
E142	9-Bit Shift Register, 500MHz	Async. Reset	SE	4Q 87
E155	6-Bit 2:1 Mux-Latch	Common Enable, Reset	SE	4Q 87
E143	9-Bit Hold Register, 500MHz	Async. Reset	SE	1Q 88
E336	3-Bit Registered Cutoff Bus XVCR	25 ohm Cut off Outputs	SE	1Q 88
E151	6-Bit D Register	Common CLK, Reset	Diff.	1Q 88
E167	6-Bit 2:1 Mux-Register	Common CLK, Reset	SE	1Q 88
E158	5-Bit 2:1 Multiplexer	Common Select	Diff.	1Q 88
E154	5-Bit 2:1 Mux-Latch	Common Enable, Reset	Diff.	1Q 88
E131	4-Bit D Flip-Flop	Individual CLK, Reset	Diff.	2Q 88
E171	3-Bit 4:1 Multiplexer	Split Select	Diff.	2Q 88
E156	3-Bit 4:1 Mux-Latch	Common Enable, Reset	Diff.	2Q 88
E160	12-Bit Parity Generator/Checker	Register-Shiftable	Diff.	2Q 88
E451	6-Bit D Register, Diff. Data & Clk Inputs	Vbb, Common Reset	SE	2Q 88

All resets are asynchronous. Diff. = Differential, SE = Single Ended.

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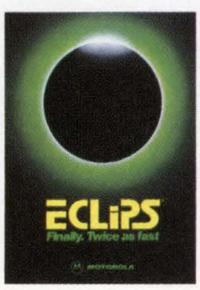

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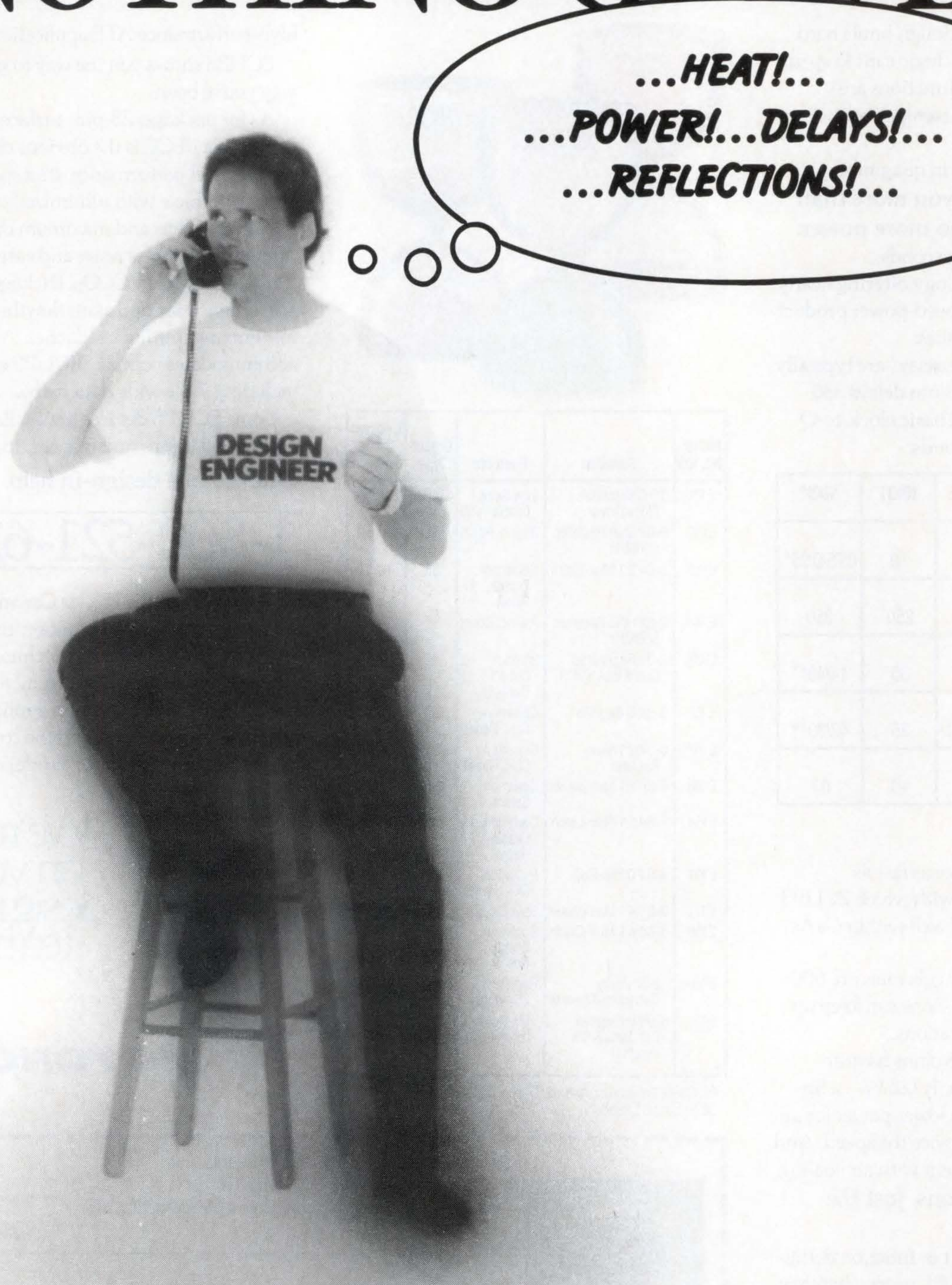

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Advanced SMT Design Techniques (short course), San Jose, CA. Surface Mount Technology Plus, 1786 Technology Dr, San Jose, CA 95110. (408) 943-0196. November 16 to 17.

Designing Signal Processors with DSP and Bit-Slice Chips (short course), Anaheim, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. November 17 to 20.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Norfolk, VA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. November 17 to 20.

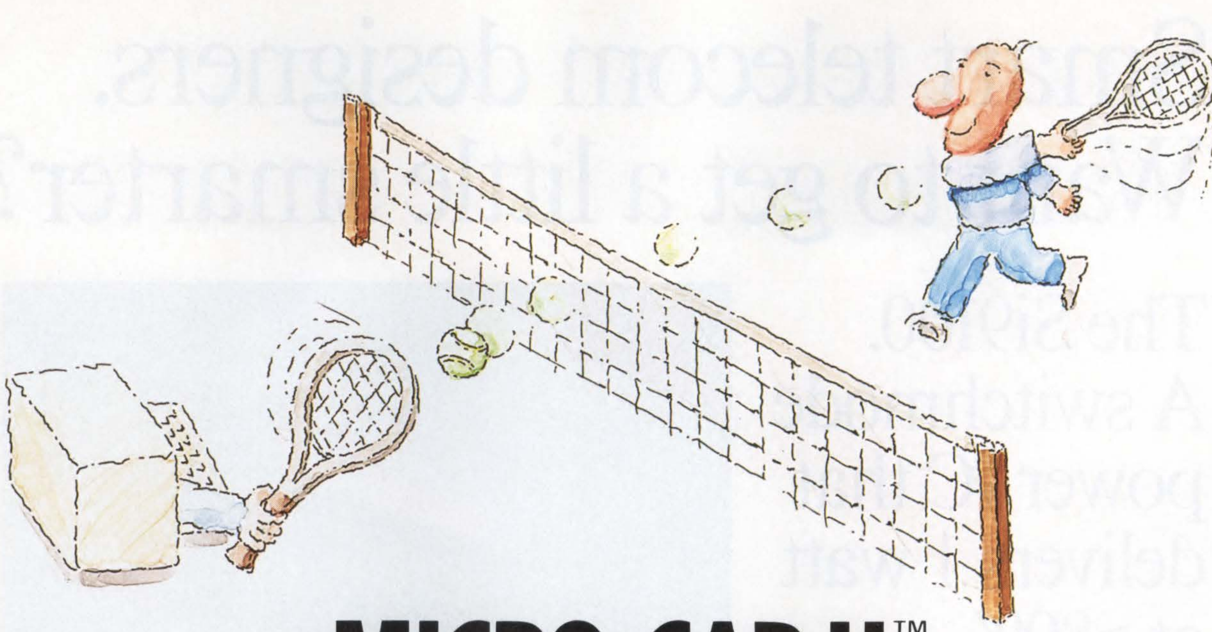
9th Interservice/Industry Training Systems Conference, Washington, DC. Ralph Nelson, ADPA, Rosslyn Center, Suite 900, 1700 N Moore St, Arlington, VA 22209. (703) 522-1820. November 30 to December 2.

Hands-On Graphics Programming Using GKS/VDI Tools, Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. December 1 to 4.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Oklahoma City, OK. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. December 1 to 4.

IEEE International Electron Device Meeting (IEDM), Washington, DC. Courtesy Associates, 655 15th St NW, Suite 300, Washington, DC 20005. (202) 347-5900. December 6 to 9.

Lasers '87, Lake Tahoe, NV. Society for Optical and Quantum Electronics, Box 245, McLean, VA 22101. (703) 642-5835. December 7 to 11.



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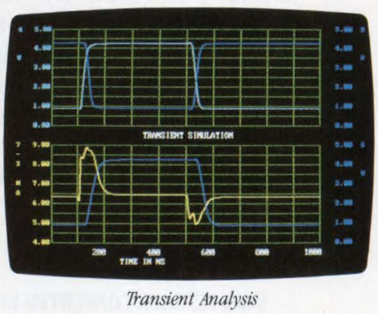
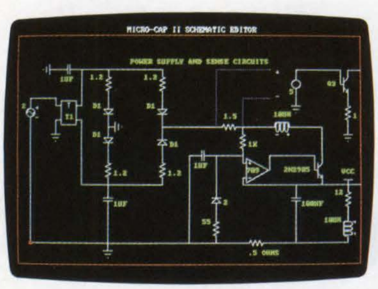


Transient Analysis



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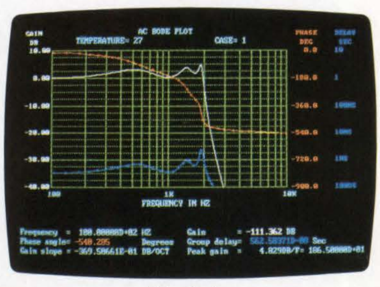

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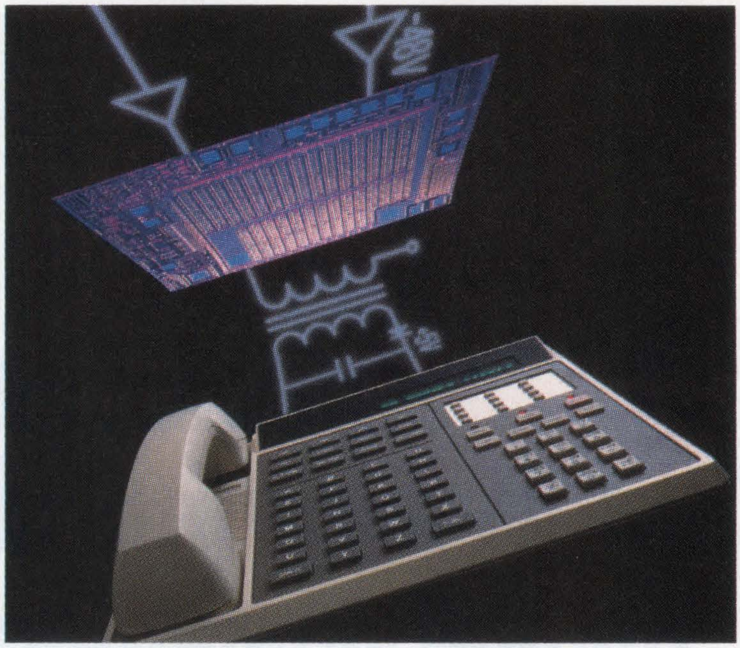

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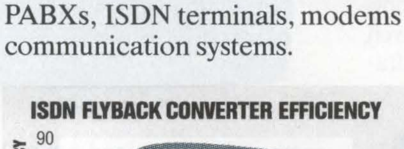

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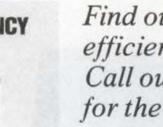

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Third Annual Battery Conference on Applications and Advances, Long Beach, CA. Cecile Duong, Department of Electrical Engineering, California State University at Long Beach, 1250 Bellflower Blvd, Long Beach, CA 90840. (213) 498-4605. January 12 to 14.

Modern Electronic Packaging (seminar), Orlando, FL. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. February 9 to 11.

Unix Technical Conference, Dallas, TX. Usenix Conference Office, Box 385, Sunset Beach, CA 90742. (213) 592-1381. February 9 to 12.

Compcon Spring (33rd IEEE Computer Society International Conference), San Francisco, CA. Hasan AlKhatib, Dept of EECS, Santa Clara University, Santa Clara, CA 95053. (408) 927-1818. February 29 to March 4.

Modern Electronic Packaging (seminar), Torrance, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. March 16 to 18.

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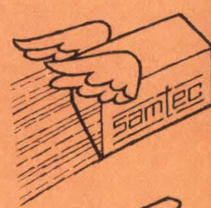

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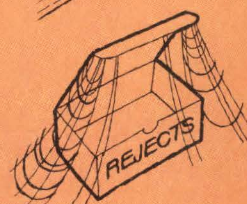

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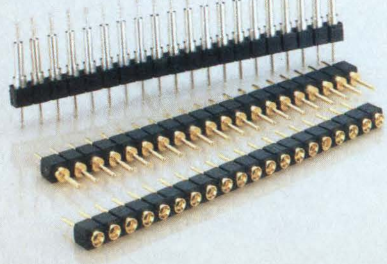

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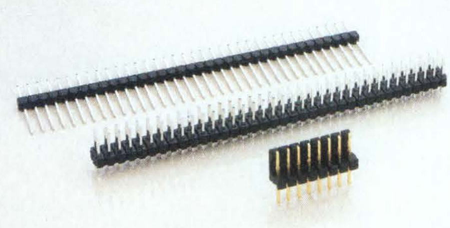

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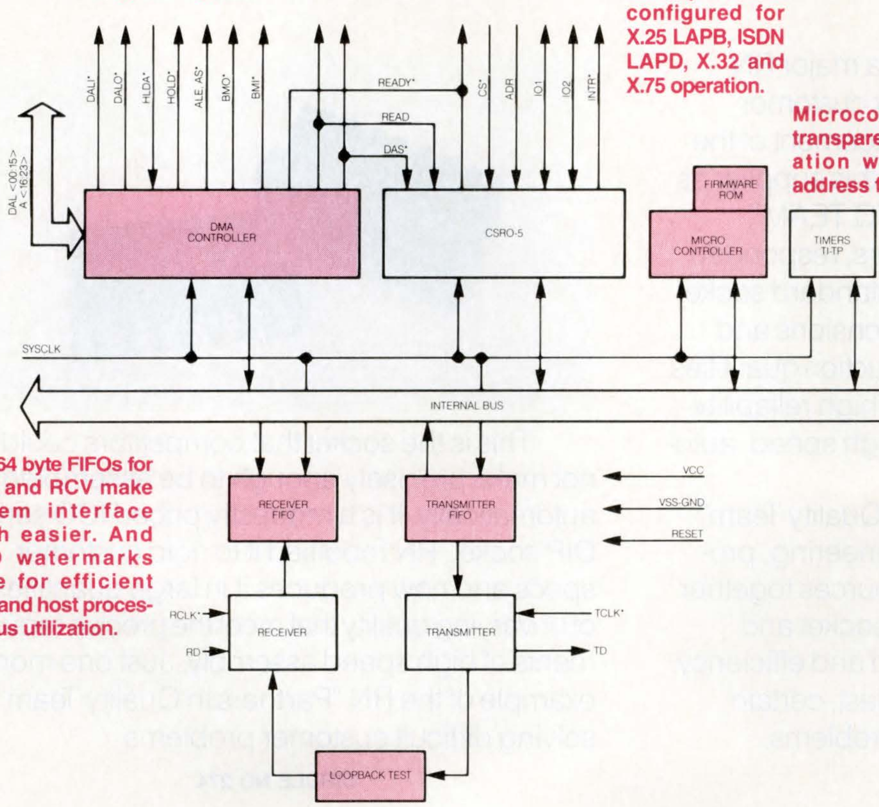

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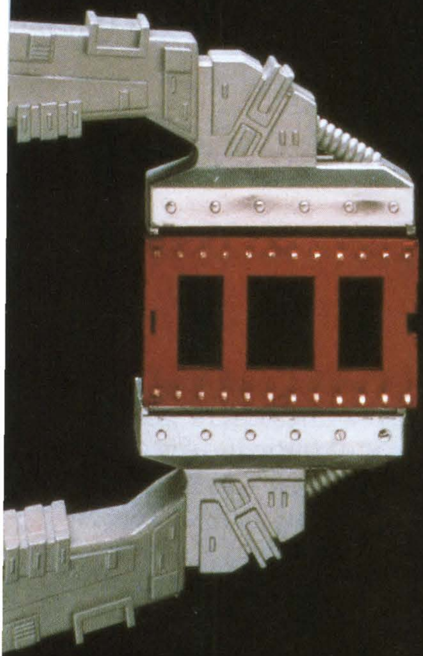

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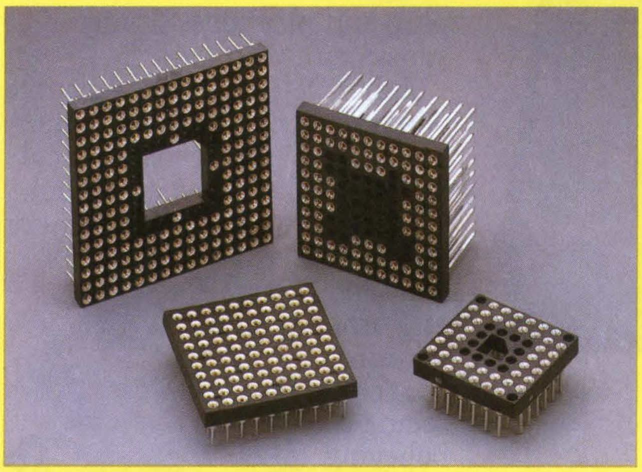

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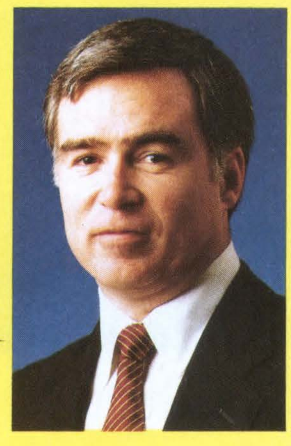

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EDITORIAL

Who won, who lost?

In the weeks past, semiconductor-industry observers and analysts have been discussing the merits of National Semiconductor's purchase of Fairchild Semiconductor Corp. They've also been mourning the loss of Fairchild as one of the industry's entrepreneurial incubators. Instead of simply touting National as a big, revitalized semiconductor supplier, it's worth looking critically at some of the real winners and losers in the transaction.

Clearly Schlumberger was a loser—it never realized a profit from Fairchild after purchasing it for $425 million in 1979. In 1986, Fujitsu offered Schlumberger between $200 and $250 million for 80% of Fairchild. But the deal fell through because of concerns on the part of the Department of Defense and individuals in the US semiconductor industry about foreign—that is, Japanese—ownership of critical technology. It was convenient to forget that Schlumberger was a foreign company, too. In the end, Schlumberger exchanged $122 million of National's stock for Fairchild.

Don Brooks, Fairchild's president, and other top management also lost. They and Citicorp Venture Capital offered $225 million in a leveraged-buyout package that Schlumberger turned down without room for further negotiations. Brooks and Citicorp thought they could turn Fairchild into a profitable venture by next year. But they never got a chance to try. Perhaps they'll find another company that will use their skills. It's doubtful they'll fit into National's plans.

Intergraph, which uses the Fairchild Clipper μP in its InterPro 32C workstation, may be in a toss-up situation. It recently negotiated to buy the Clipper line from National for $10 million, thus protecting its supply of the μP chips. However, because the company is its own best customer, Intergraph may be reluctant to depart from Clipper-based technology when the market demands it.

Finally, National Semiconductor's situation appears to be a tossup, too. Keep in mind that National had net losses in three of its last five years and that its semiconductor sector lost $129 million for the fiscal year that ended in May. It's true that National's acquisition of Fairchild boosts its position on the scale of military, bipolar, and analog semiconductor manufacturers. However, combining two money-losing companies may yield only a larger money-losing business. To be successful, the company will have to turn itself around quickly. As National's Peter Sprague said to *Business Week*, "Otherwise, paying $122 million for the opportunity to lose $10 million a month isn't such a hot deal."

Jon Titus

Jon Titus
Editor

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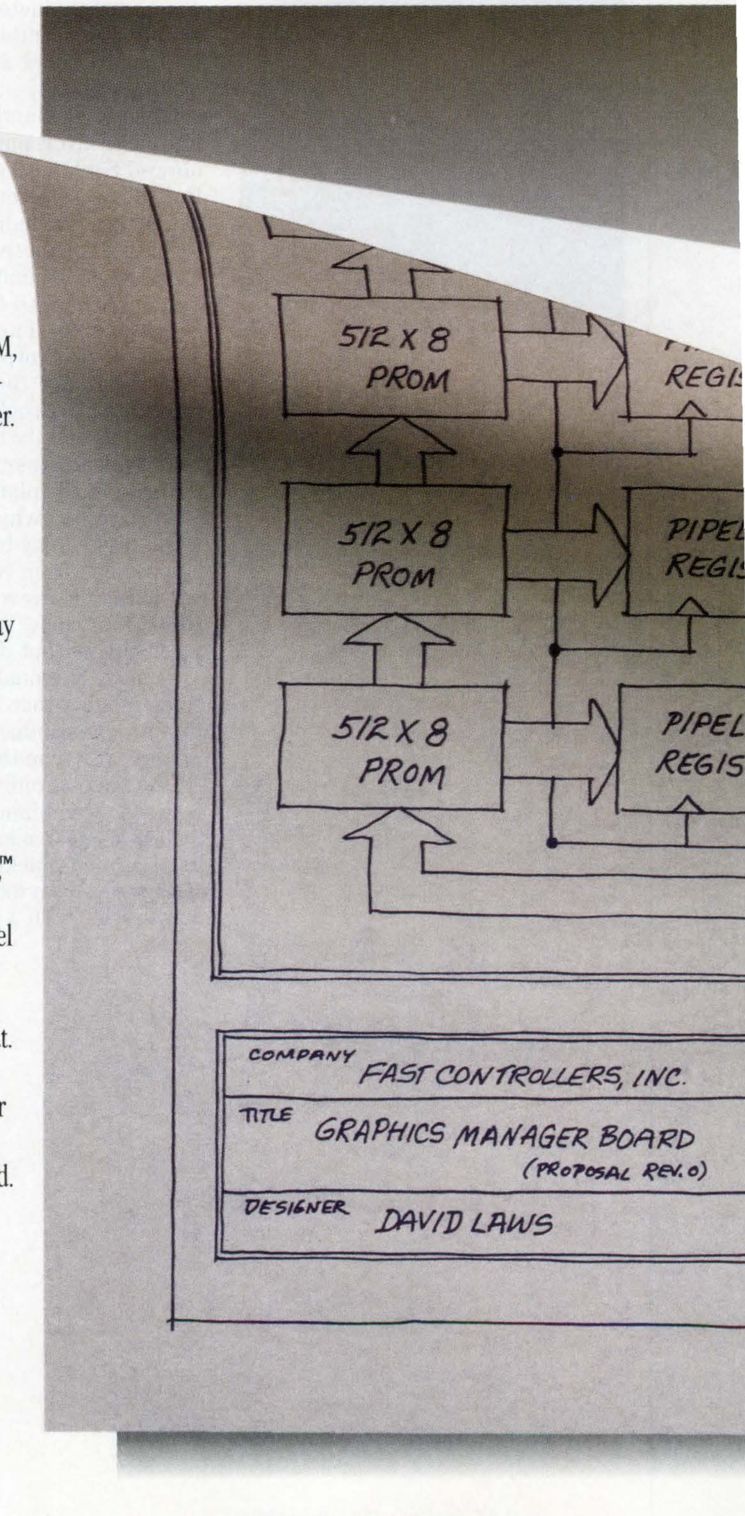

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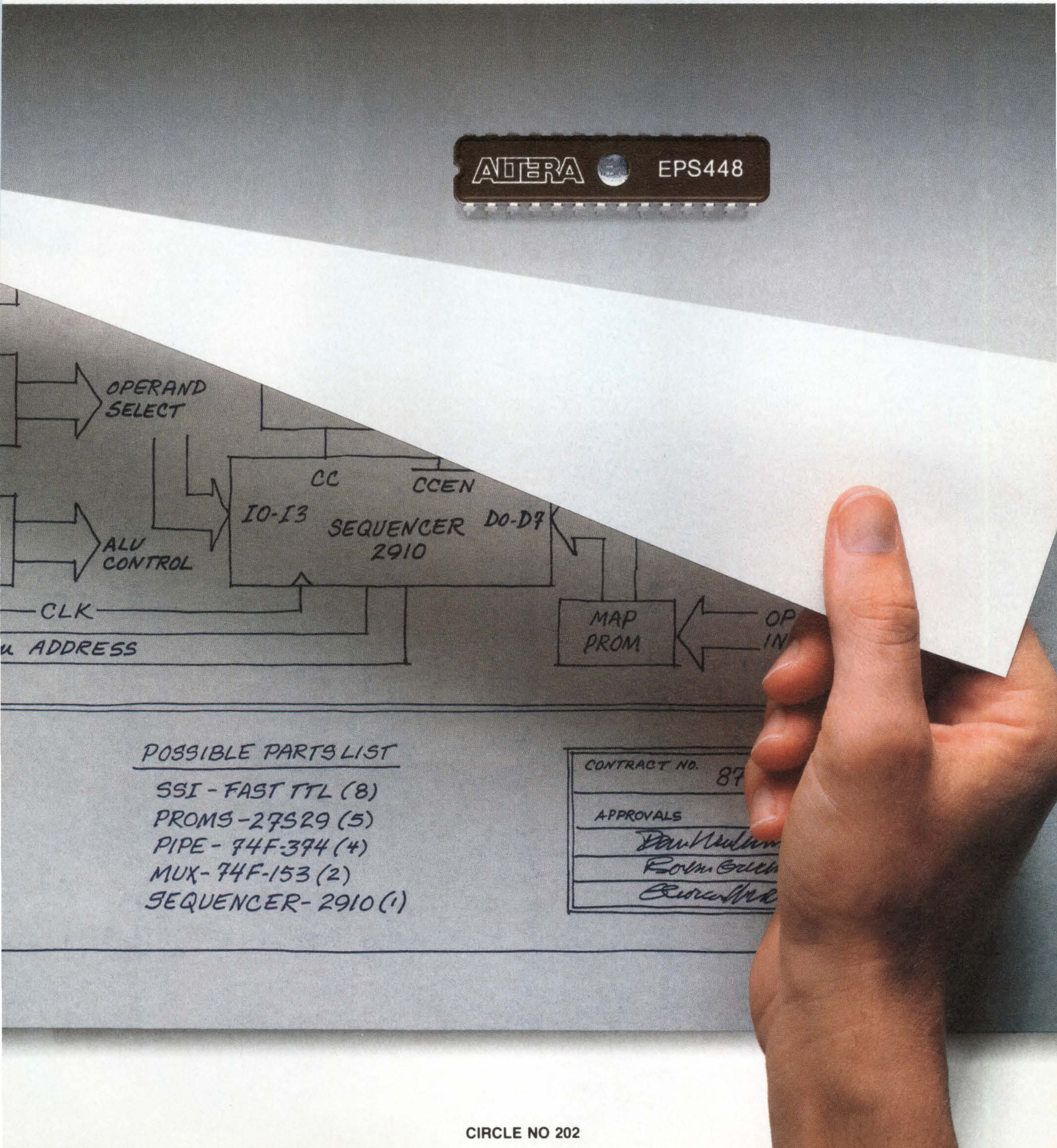

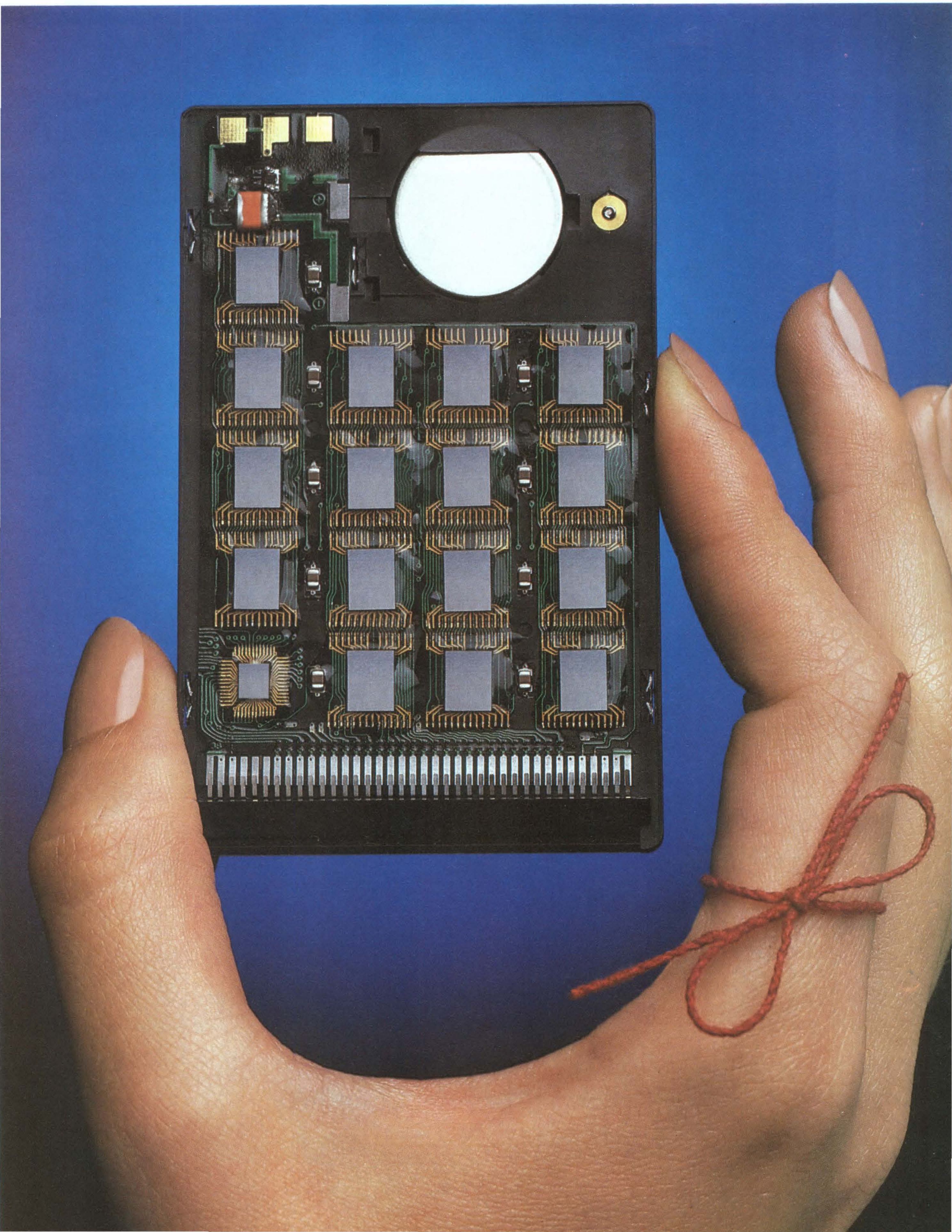

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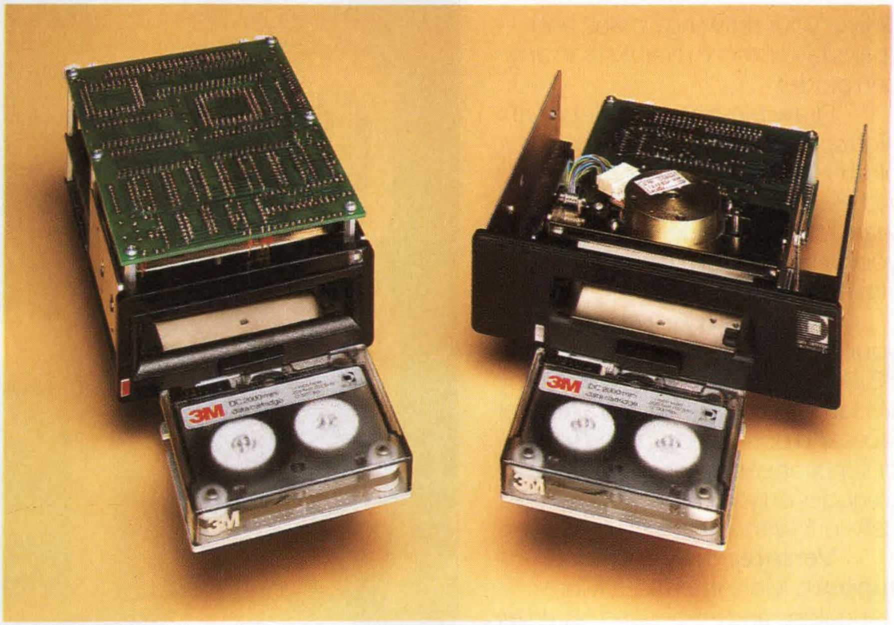
CIRCLE NO 200

Interface and data format dictate your choice of a minicartridge tape drive

Maury Wright, *Regional Editor*

Most tape-drive manufacturers and their customers agree for now on the appropriate medium and capacity for low-end secondary-storage applications: A number of manufacturers offer 40M-byte drives based on the 3M DC 2000 or DEI (San Diego, CA) Microtape 2000 minicartridge, which use ¼-in. tape. The vendors have yet to agree, however, on a standard drive interface or data format. You can choose from four incompatible combinations of drive interface and data format from a number of different vendors. The drive manufacturers soon plan to boost minicartridge-drive capacities to 80M to 120M bytes, but, again, you can expect a choice of three or more incompatible products.



*By offering both **floppy-interface and QIC-100** models in 3½- and 5¼-in. form factors, 3M targets its MCD-40 tape-drive offerings at both low-end single-user systems and more-powerful systems that use the SCSI I/O bus.*

Like floppy-disk drives, tape drives are secondary-storage devices; they perform such tasks as backup of primary-storage devices (hard-disk drives), data or software distribution, and data or software transfer. In most small-computer applications—the primary use for minicartridge drives—minicartridges are used strictly for backing up hard disks. In those applications, the different interfaces and data formats aren't important. The end users won't need tape drives that can read data cartridges recorded on other computers; they'll use the drives simply to back up their own data.

But in a small but important percentage of applications, minicartridges are used for software or data distribution and transfer. If you're building a system for such an application, you can appreciate the need for an industry-wide standard interface and data format for tape drives.

Unfortunately, no standard yet exists for minicartridge drives. One major reason why minicartridges aren't standardized is that IBM hasn't yet endorsed a particular minicartridge product. The secondary-storage standards that do exist—those for open-reel and floppy-disk drives—are the direct result of IBM's choice. Until IBM chooses a sub-4-in. tape drive, you can expect the market for minicartridge data-storage peripherals to remain highly volatile.

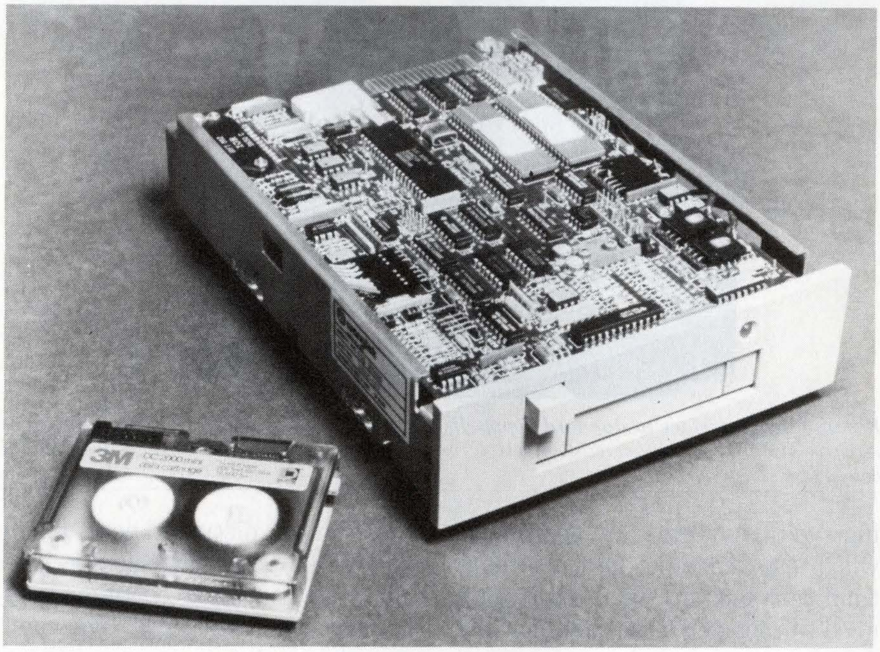
Tape capacity matches disk's

For backup applications, tape-drive manufacturers strive to offer products that match the capacity and form factor of hard-disk drives. DC 2000-type minicartridges have proved to be an ideal backup medium for low-end systems. Minicartridge drives fit into the 3½-in. disk-drive form factor, and manufacturers also offer the drives with half-height, 5¼-in. mounting frames. The drives' 40M-byte capacity matches the hard-disk capacity currently popular in personal-computer applications.

The 40M-byte capacity will also serve other small business systems and even low-end engineering workstations. Minicartridge-drive manufacturers plan to boost the capacity of their drives to keep pace with the higher-capacity hard-disk drives used in business systems. In fact, future minicartridge drives will store more than 100M bytes, and they may even suit low-end minicomputer and mainstream engineering-workstation applications.

Among the 40M-byte minicartridge-drive choices are products from Irwin Magnetic Systems. The products' format is proprietary, but it's in wide use: Irwin was the first company to offer minicartridge tape drives for secondary storage and has sold more minicartridge tape


Ken's Pharmacy



***An error-corrected hard-error rate of 1 bit in 10^{11}** characterizes Wangtek's FAD-3500 tape drive. This error rate exceeds the hard-error rates of typical Winchester drives.*

drives than any other company. In fact, before 3M introduced the DC 2000 (¼-in. tape) cartridge, Irwin offered drives for the DC 1000 (0.15-in. tape) cartridge.

Although Irwin still offers drives for the DC 1000 cartridge, its customers choose the DC 2000 product for almost all new designs. For the DC 2000 cartridge, the company offers the 20M-byte Model 120/220 and 40M-byte Model 145/245 drives; they cost $499 and $699, respectively.

QIC supports two standards

Unlike the proprietary Irwin drives, all the other available minicartridge drives evolved from the Working Group for Quarter Inch Cartridge Drive Compatibility (QIC). QIC (pronounced "quick") is a group of manufacturers that promotes standard formats and interfaces for tape drives. The QIC group couldn't agree on a single type of tape drive for minicartridges, but it did settle on two: QIC-40 and QIC-100. Drive manufacturers currently offer devices that meet both specifications.

Four QIC-40 tape drives are currently available: Alloy Computer Products' APT-40/Q, Archive's XL, Mountain Computer's TD4000, and Wangtek's FAD-3500. Each of the QIC-40 drive manufacturers quotes a price around $250 (1000) for its product. All the QIC-40 drives are very much alike, probably more so than any other data-storage product in history. Your choice among them would probably depend on nothing more significant than your bargaining abilities.

A similar drive is 3M's MCD-40/FITD. Although its format originally evolved from the QIC-40 effort, it's different enough from QIC-40 to qualify as a separate format. The drive costs $280 (1000).

Three manufacturers currently offer QIC-100 minicartridge tape drives. Tallgrass Technologies, the company that developed the QIC-100 tape format (Tallgrass originally called it PC/T), offers the MCD40 SCSI-3.5 for $375 (1000). Braemar markets the Qicbac 350S at $410 (1000). The 3M MCD-400 series QIC-100 drive sells for $420 (1000).

Interface dictates cost

In choosing a drive strictly for backup applications, you need to consider only the cost and performance characteristics of the various offerings. In minicartridge tape drives, the drive interface dictates the price and performance characteristics.

The Irwin, the 3M MCD-40/FITD, and the QIC-40 drives all interface to a standard SA-450/475 floppy-disk-drive controller such as the one on the IBM PC. Because that interface is simple, the floppy-interface drives cost less than any of the currently available QIC-100 drives, each of which includes an intelligent Small Computer System Interface (SCSI) controller (the QIC-100 standard, however, doesn't specify a particular controller interface).

The floppy-interface drives also save you money because they don't require a special interface; they connect to the floppy-disk-drive controller that's already present in most system designs. In contrast, to interface a QIC-100 drive to many low-end systems, you must add a SCSI host adapter, thereby increasing the cost of the system.

The QIC-100 drives, however, transfer data faster than the floppy-interface drives do. Minicartridge drives that interface to a floppy-disk-drive controller are limited to the transfer rate of that controller—250k bps for 360k-byte controllers and 500k bps for 1.2M-byte controllers. The transfer rate of a QIC-100 product is limited only by the drive's recording density and tape speed: The SCSI bus can handle 1.5M-byte/sec asynchronous transfers and 4M-byte/sec synchronous transfers.

Tape speed affects data rate

The Braemar and Tallgrass QIC-100 drives transfer data at 750k bps, and the 3M drive transfers data at 600k bps. All three drives feature 10,000-bpi recording densities, but the Braemar and Tallgrass drives spec a 75-ips tape speed, and the 3M product has a 60-ips tape speed. The faster transfer rate of the Braemar and Tallgrass drives results in faster backup operations and faster tape-format operations. The particular driver-software implementation you write determines the exact effect that the transfer rate will have on backup or format time.

Stan Miller, market development manager for 3M, points out other factors that might affect your choice between floppy-interface and QIC-100 drives. Miller claims that floppy-interface drives best suit applications in single-user systems, such as personal computers running MS-DOS. A floppy-interface drive wouldn't be a good idea for a multiuser system both because of the slow transfer rate and because the system CPU must interact with the floppy-disk-drive controller on all tape operations.

Drives suit network server

The more-expensive SCSI controller on QIC-100 drives better suits the products to multiuser or network server applications, according to Miller. Because QIC-100 uses a SCSI controller, it won't substantially slow your system's performance: The SCSI controller permits data transfers directly from tape to hard disk or hard disk to tape. SCSI also supports multithreading (multitasking) in the I/O subsystem.

As a system designer or value-added reseller, when you're choosing how to implement secondary storage in a system you must consider the needs of your entire potential customer base. If you're designing your system for customers who'll use the tape drive for more than just backup purposes, you'll need to consider more than just the drive's price and performance specs. For instance, your customers may want to use their cartridges to transfer data among systems, or your company or independent software developers may decide to distribute software or data on tape cartridges.

Because they interface to standard floppy-disk-drive controllers, *QIC-40 tape drives such as Archive's Model XL prove cost-effective for implementing backup storage in personal computers.*

For applications entailing data distribution or transfer, you must also consider the format a tape drive uses to write data onto a cartridge. The drive's ability or inability to interchange data with other drives may override cost and performance considerations.

The 40M-byte Irwin tape drive stores data on 20 tracks at a recording density of 10,000 bpi. Unlike the other vendors discussed here, Irwin employs a tape format that specifies that a servo signal be embedded between each data block. The company claims that the servo scheme improves the tape drive's track-following characteristic. The drive's specification lists an error-corrected hard-error rate of 1 bit in 10^{11}.

Because Irwin uses a proprietary data format, its drives can't read cartridges written by drives from any other manufacturer. The drives do, however, offer "downward compatibility" with all tape drives Irwin has offered. Downward compatibility means that a certain drive can read a cartridge written on an Irwin drive of equal or lesser capacity. In fact, the DC 2000-based drives can even read DC 1000 cartridges.

The QIC-40 drives also store data

Longer tape boosts cartridge capacity

You can increase a cartridge-tape drive's capacity by using a cartridge with a longer tape. DEI (San Diego, CA) offers cartridges that allow users to increase their drives' storage capacity by as much as 70%. The company's Gold Plus XL line of full-size ¼-in. tape cartridges includes models with 750 and 1000 ft of tape instead of the standard 600 ft. The Gold Microtape 2000 XL cartridge holds 300 ft rather than the standard 205 ft of tape found in minicartridges.

A 40M-byte QIC-40, QIC-100, or Irwin minicartridge tape drive can store 60M bytes on the $35 Microtape 2000 300XL cartridge. The $55.50/$59 Gold Plus 750XL/1000XL series can store 100M to 500M bytes when used with cartridge drives capable of storing 60M to 300M bytes on 600-ft cartridges.

DEI claims its patented Equithane belt design is responsible for the reliability and data integrity of the longer-tape cartridges. The company also uses a new plated-particle media formulation in the cartridges; the formulation allows for thinner tape, so more tape can fit into the cartridge.

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at 10,000 bpi on 20 tracks. The standard specifies that the drives employ a Reed-Solomon error-correction code (ECC), which results in a hard-error rate of 1 bit in 10^{14}. The 3M floppy-interface drive stores data at 8621 bpi on 24 tracks and has a hard-error rate of 1 bit in 10^{12}.

QIC-40 specifies file format

What's more important, the QIC-40 specification not only dictates a data format but also defines a file format and common-command set. The data files recorded on a cartridge by a QIC-40 drive can therefore be read on any other QIC-40 drive, regardless of the tape-drive manufacturer, computer type, or operating system. Theoretically, the QIC-40 manufacturers say, only one in 300,000 cartridges will prove unreadable on a drive from any manufacturer.

The QIC-40 standard is the first cartridge-tape standard to achieve such interchangeability. Not even the widely used QIC-24 drives (full-size DC 600 cartridges) feature data-file compatibility. As a matter of fact, Alloy claims that its drive can read cartridges written by certain models of Irwin drives.

The QIC-100 standard fails to provide such file interchangeability. The drives record data at 10,000 bpi on 24 tracks. Their exclusive-OR ECC scheme results in a hard-error rate of 1 bit in 10^{12}, but also requires that ECC data blocks occupy 50% (overhead) of the capacity of real data blocks.

Despite the lack of a defined file format, Apple Computer (Cupertino, CA) has created a de facto file format for the QIC-100 drives by offering 3M QIC-100 drives as backup-storage options for the Macintosh. Both Braemar and Tallgrass products, which third-party subsystem houses offer to Macintosh users, can read cartridges recorded by the 3M QIC-100 drive.

Drives offer powerful format

QIC-100 is a potentially more powerful format than the QIC-40, 3M, or Irwin formats. Although all of the minicartridge products can randomly access any data on a cartridge, the QIC-100 products can typically access a file in 9 sec. The QIC-100 format also lends itself to selective updating of the files on a tape.

The floppy-disk-drive controller also affects the format on floppy-interface tape drives because the controllers support only MFM (modified frequency modulation) encoding. Manufacturers supply the QIC-100 drives with group-code-recording (GCR) encoding.

Minicartridge-drive manufacturers would all like to increase their drives' capacities, and the QIC-100 combination of GCR encoding and SCSI controller will probably provide the simplest upgrade path of all the offerings. The SCSI bus will handle an increase in data rate as the bit density is increased on the drive. And GCR encoding allows for the increase in recording density.

New designs not yet defined

For now, the only way to increase a QIC minicartridge drive's capacity—which is limited only by that of the cartridge—is to use a longer-tape cartridge (see **box,** "Longer tape boosts cartridge capacity"). Unfortunately, the QIC group remains undecided on the format or interface type to use in a drive that holds 80M bytes or more. Certain factions within the group would simply like to offer an 80M-byte version of the QIC-40 product. The 80M-byte product would still use a floppy-disk-drive interface and would maintain downward compatibility with QIC-40 drives. Other group members would like to move immediately to a higher-performance product.

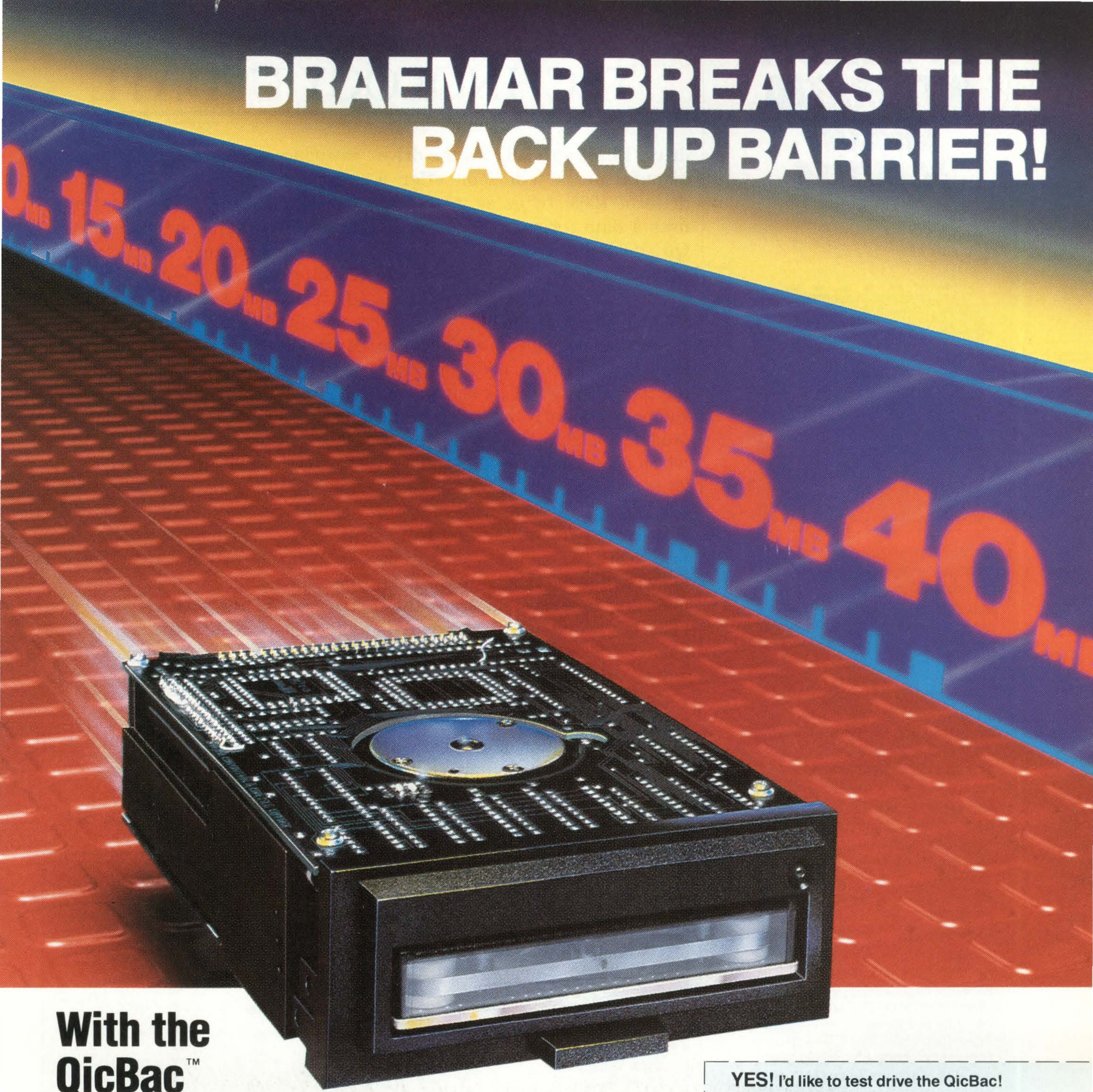
Lee Elizer, president of Peripheral Strategies Inc (a Santa Barbara, CA, research firm) is one of those who believes the next product will be an 80M-byte floppy-interface

US company forms Asian alliance

Companies from Asia haven't generally been successful in selling low-end data-storage peripherals on the US market. The large Asian companies, however, have vast engineering and manufacturing experience in tape recording and drive mechanisms. California Peripherals Corp, or Caliper (Torrance, CA), has formed a strategic alliance with Nakamichi Corp (Kodaira, Japan) to tap such resources and quickly enter this competitive US market.

Although Caliper made a late entrance to the market for DC 600-based tape-cartridge drives, the company now offers 60M-, 120M-, and 150M-byte drives, and will soon offer 300M-byte products. Nakamichi engineered and is building the drives for Caliper. Caliper was among the first companies to introduce a drive that used the 3480 ½-in. tape cartridge in a drive that met the HI/TC standard, which was developed by HI/TC, a group of manufacturers similar to QIC.

The Caliper/Nakamichi team is preparing to cooperate on other products as well. You can expect Caliper to introduce a minicartridge drive when the QIC committee clears up some confusion over future standards. The company will probably also be a leader in 4-mm-tape digital-data-cartridge drives. Nakamichi is making 4-mm-tape audio drives now.



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drive. Elizer also believes the drive manufacturers will soon offer a drive of 100M bytes or more that uses a data format similar to the QIC-150/300 DC 600 drives, and a SCSI controller.

Capacities move ahead

Irwin, meanwhile, doesn't have to consult anyone else before increasing the capacities of its drives. The company recently introduced the Model 165/265 64M-byte drive, which records data at 13,200 bpi on 24 tracks and sells for $899. Irwin also plans to ship a drive of more than 100M bytes in the first half of next year. The company believes an embedded-servo tape format will be necessary to achieve such capacities. (The QIC committee, however, is not considering a servo scheme for any new drives it specifies.)

Both Irwin drives will use a floppy-disk-drive interface, and both will offer the option of working with 750k-bps floppy-disk-drive controllers, which are currently being designed. The company also plans to introduce a SCSI-controller product next year.

Also on the horizon are 4-mm-tape digital-data-cartridge drives. The drives will use helical-scan-recording technology and the same drive mechanism and head developed for the digital audio-tape industry. The drives may provide Asian companies with an inroad into the small-tape-drive market (see **box,** "US company forms Asian alliance"). Although they'll be the same size as the minicartridge drives—so they'll fit into the same 3½-in. form factor—they will store more than 1G byte. The 4-mm-tape drives may be available within a year, but it'll take longer for the price to drop to the level of the minicartridge; you can expect to see the 4-mm-tape drives offered at a reasonable price by 1990. **EDN**

Article Interest Quotient
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For more information . . .

For more information on the minicartridge tape drives discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

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Irwin Magnetic Systems Inc
2101 Commonwealth Blvd
Ann Arbor, MI 48105
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Mountain Computer Inc
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Scotts Valley, CA 95066
(408) 438-6650
TWX 910-598-4504
Circle No 725

Tallgrass Technologies Inc
11100 W 82nd St
Overland Park, KS 66214
(913) 492-6002
TLX 437121
Circle No 726

3M Co
Magnetic Media Div
Building 223-5N, 3M Center
St Paul, MN 55144
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Wangtek Inc
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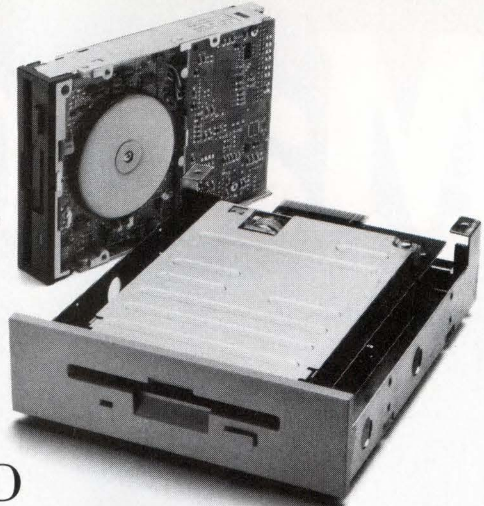

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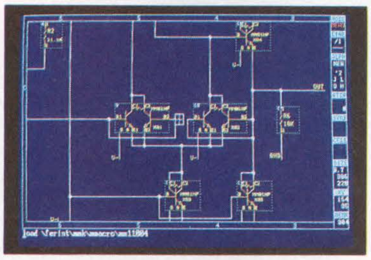

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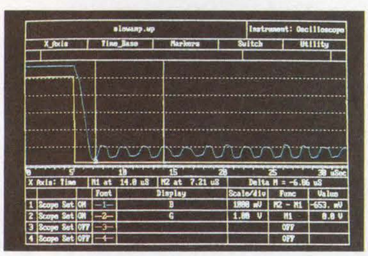

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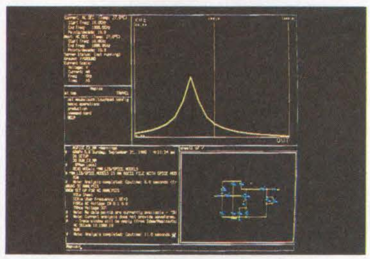

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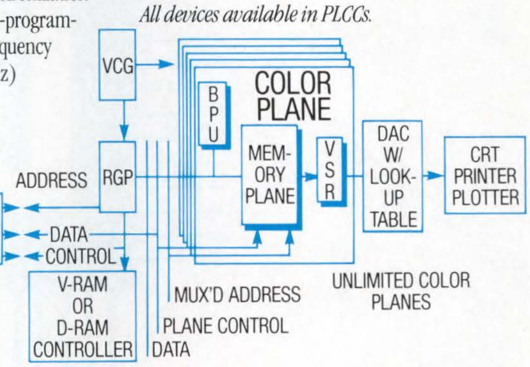

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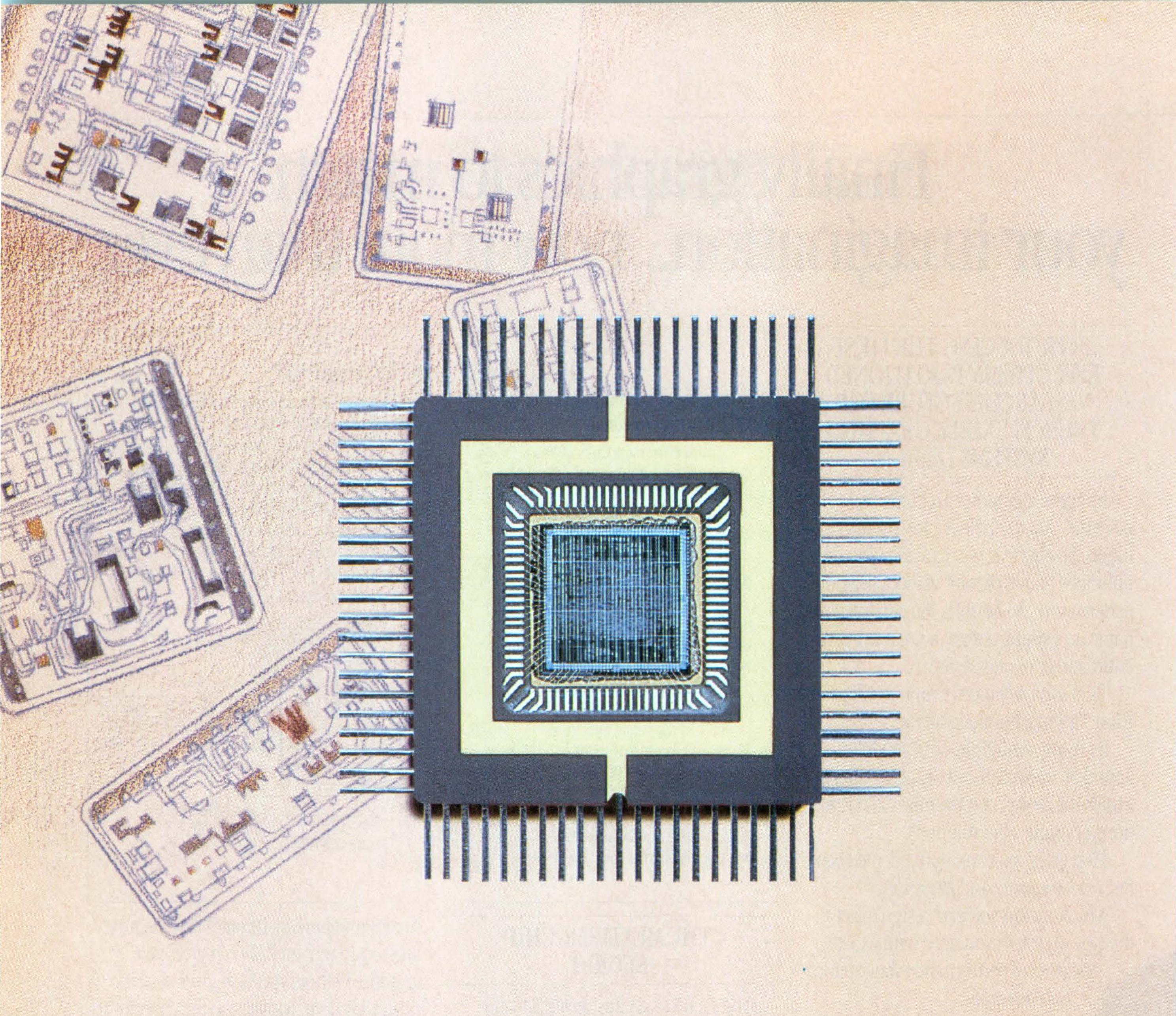

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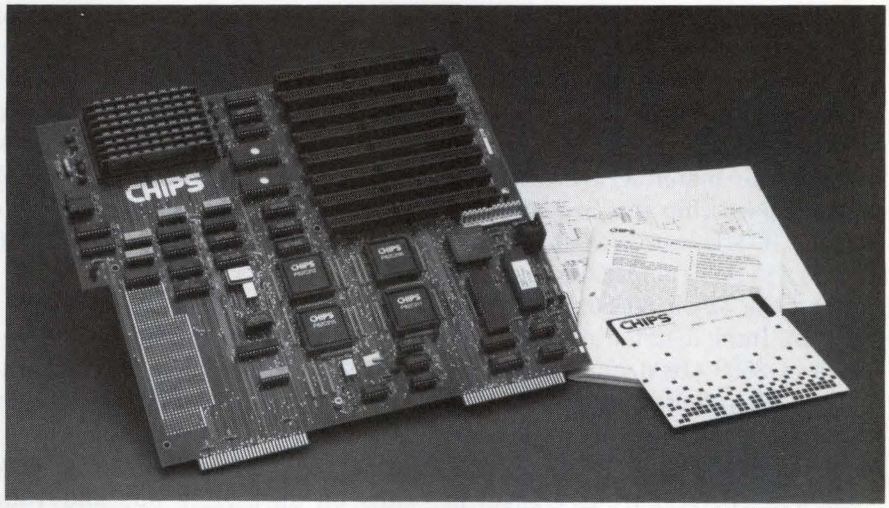
Chip sets for PC/AT compatibles support faster μPs and shrink board size

Margery S Conner,
Regional Editor

Using a chip set that provides the basic nonmemory functions of an IBM PC/AT mother board, you can build a board for your system that is less than half the size of IBM's version. Generally, the only additional ICs necessary are the μP, keyboard controller, and buffer chips. In all, the total number of chips required is well below that of IBM's 110, along with a corresponding reduction in power (**Table 1**). All of the chip sets available support speeds faster than that of IBM's PC/AT; the differences among them depend mainly on whether or not they offer more capabilities than the IBM PC/AT mother board.

In general, chip sets for PC/AT compatibles fall into two categories: straight implementations of the IBM PC/AT mother board, with all of its faults and virtues; and new chip sets that implement the PC/AT's capabilities and incorporate some non-PC/AT features as well, such as fast mode-switch, extended memory, and shadow RAM. The new chip sets are available from Chips and Technologies Inc (CTI), Faraday, and Zymos; VLSI Technology, G2, and Logicstar sell the straight-implementation chip sets.

The number of extra nonmemory ICs required to implement a mother board varies, depending on the chip set. Logicstar's SL600X chip set needs 36; Zymos's Poach/ATFB requires one. Note the attendant prices, though: The Logicstar chip set sells for $44 in low volumes, whereas the Zymos chip set costs almost twice that in OEM quantities ($75). If board space isn't a major consideration in your application, you may be better off with the less-expensive set. No matter which chip set you choose, however, you still achieve a total IC count well below that of IBM's PC/AT.



***Most manufacturers will supply** a chip-set evaluation board so that you can test a chip set before you buy. Chips and Technologies' CS8221 fits in the same form factor as the IBM mother board.*

Power requirements are reduced

The chip sets also offer the opportunity to reduce your system power requirement. Make sure, though, that the manufacturer hasn't eliminated a capability of the PC/AT that's vital to your design in its zeal to reduce space and power. Faraday's FE3600 chip set, for example, doesn't contain a clock/calendar circuit; if you need one, you'll have to add a chip like Dallas Semiconductor's (Dallas, TX) DS1287 Real-Time Clock Plus RAM, which contains a battery and support circuitry.

CTI departs from its previous chip set's architecture, which incorporated bipolar bus drivers (as does the PC/AT) by going to an all-CMOS design. The CS8221 contains the control circuitry to add a bidirectional driver if your application requires more than the CMOS chip set's 8-mA drive capability.

VLSI Technology's VL82C(PC/AT) chip set has a CMOS address- and data-bus buffer chip that can supply as much as 20 mA. If you need more current, you can add a bidirectional bus driver, but the chip set doesn't have the integral control circuitry for one, and therefore you'll need more chips than the 16 listed in **Table 1.** Study the data sheets, and if they don't provide enough detailed information, ask the manufacturer which IC each individual chip replaces.

Processor speeds are faster

Systems based on these chip sets offer faster speeds and reduced board size. The simplest way to gain a speed advantage over IBM's 8-MHz PC/AT is to raise the processor clock speed. All of the chip sets support 8-, 10-, and 12-MHz clock rates for the 80286. Further, CTI's CS8221, Faraday's FE3600, G2's GC(PC/AT), and Zymos's Poach/ATFB can also operate with

AMD's 16-MHz 80286. CTI and Faraday both stress that their chip sets will be able to support AMD's 80286s operating faster than 16 MHz as these μPs become available. You should remember, however, that Intel has named AMD in a lawsuit over the 80286, and it's possible that its production will be held up.

It's already a certainty, however, that the 80386 has a long lead time and a high price, and this is the reason the manufacturers of the higher-speed chip sets are supporting the 16-MHz 80286 as an alternative to a PC/AT compatible designed around the 32-bit 80386. Early this fall, an Intel distributor quoted a price of $599 (1000) for the 80386, but wouldn't quote delivery: At that time, the vendor had been allocated only 165 of the chips for the southwestern US. Apparently Intel is selling all it can make of these chips to companies like IBM and Compaq, who are buying in very large quantities. All in all, you may be better off choosing a higher-speed 80286-based design; all the chip sets support 10- and 12-MHz systems, and so you have a fallback if your 16-MHz 80286 encounters availability problems.

Both the straight implementations and the newer offerings operate at faster processor speeds than the IBM PC/AT's 80286, but you should be aware of the limitations of the add-in cards you need to use on the system bus. Most add-in-board manufacturers will only guarantee a board's compatibility with the clock frequencies in the standard IBM PC/AT. You may have problems running your system bus at 12 or 16 MHz.

CTI and Faraday have schemes for slowing the system bus to accommodate the slower cards. Faraday's chip set slows the bus only for accesses to slower add-in boards. If you have an add-in board that only runs on an 8-MHz bus and your system bus is running at the μP's 16-MHz clock frequency, the chip set slows the system bus to 8 MHz to let the μP access the slow board. When the board access is complete, the chip set returns to 16-MHz operation. This speed change is made under software control; therefore, your system's program must be written so that it takes the slow speeds of the peripherals into account.

The CTI chip set gives you the option of completely segregating the μP bus from the system bus: You can run the μP bus asynchronously to the system bus. You can select from three possible sources for the system bus clock—the μP clock, the μP clock divided by 2, or an external source. For instance, if you want to run the μP clock at 16 MHz, you have a choice of running the system bus clock at the full 16 MHz, using the chip set's internal divide-by-2 circuitry to obtain a system bus clock of 8 MHz, or using an external clock source to generate a, say, 12-MHz rate.

Bus schemes: pro and con

The disadvantage to CTI's scheme is that the system bus speed is constrained by the speed of the slowest add-in card on the bus. Its advantage over Faraday's scheme is

TABLE 1—REPRESENTATIVE CHIP SETS FOR 80286-BASED PC/AT COMPATIBLES

MANUFACTURER	CHIP SET	NUMBER OF CHIPS/SET	MAXIMUM μP CLOCK (MHz)	ADDITIONAL CHIPS NEEDED (EXCLUDING RAM)	MAXIMUM RAM (BYTES)	ON-CHIP BUS DRIVE CURRENT	CHIP-SET PRICE
CHIPS AND TECHNOLOGIES (CTI)	CS8221	4 (82C211, 212, 215, 206)	16	24	8M (LIM EMS)	8 mA	12 MHz: $108.90 (100) 16 MHz: $136.80 (100)
FARADAY	FE3600	4 (FE3001, 3010, 3021, 3031)	16	6	8M (LIM EMS)	24 mA	$95 (10,000)
G2	GC(PC/AT)	3 (1 GC101 AND 2 GC102s)	16	10	1M	24 mA	$78 (10,000)
LOGICSTAR	SL600X	5 (SL6001, 6002, 6003, 6004, 6005)	12	36	1M	24 mA (BUS DRIVER ICs ARE BIPOLAR; LOGIC ICs ARE CMOS)	$44 (100)
VLSI TECHNOLOGY	VL82C(PC/AT)	5 (VL82C100, 101, 102, 103, 104)	12	16	640k	20 mA	$68.85 (10,000)
ZYMOS	POACH/ATFB	6 (P7, 8, 10, 11, 12, 13)	16	1	16M (LIM EMS 4.0)	20 mA	UNDER $75 (1000)

*THIS PRICE ALSO INCLUDES A GRAPHICS CONTROLLER AND A DISK CONTROLLER.

that you don't need any special programming to exploit it.

In general, if your system's add-in boards will be accessed frequently and will also be constrained by a bus speed that's lower than the μP clock, the CTI scheme may be the best, particularly if your software doesn't take slower peripherals into account. If most of your system's add-in boards can operate at the μP speed with only occasional accesses to slower add-in boards, and you know that the software is capable of allowing for slower peripherals, Faraday's scheme may be better.

As stated earlier, the newer chip sets from CTI, Faraday, and Zymos offer more than just faster processor speeds; they provide fast mode-switching, shadow RAM, and extended-memory support. These chip sets accelerate the 80286's mode-switching ability by copying the way IBM speeded up its Model 50/60 PS/2.

Whenever an IBM PC/AT switches between the real-address mode (which is the mode the 8088/8086 programs use) and the pro-

EVALUATION BOARD PRICE	COMMENTS
$2450	CHIP SET DOES NOT INCLUDE BUS DRIVERS. ADD EXTERNAL DRIVERS FOR >8-mA CAPABILITY.
$1095*	SAMPLES WILL BE AVAILABLE IN 4TH QTR.
$699	SAMPLES WILL BE AVAILABLE IN 4TH QTR.
NONE	PIN-FOR-PIN COMPATIBLE WITH CTI's OLDER 82CS220.
$2000	
UNDER $1500	SAMPLES WILL BE AVAILABLE IN 1ST QTR OF 1988 (12-MHz SAMPLES WILL BE AVAILABLE IN 4TH QTR 1987).

***Chip sets such as the** GC(PC/AT) from G2 can squeeze the functions of an IBM PC/AT-compatible mother board into as few as three ICs.*

tected virtual-address mode (which gives you access to the 80286's 16M bytes of memory), the system has to be reset. Because IBM reset the PC/AT's μP through the 8042 keyboard controller, the 8042's delay in recognizing reset commands means mode switching takes about 90 μsec, a costly time penalty.

In the Model 50/60, IBM set up a port for resets, which reduces the mode-switch time to 1 μsec. Note that this reset is transparent to the software; if you have a memory-resident program such as Sidekick, for example, it remains in RAM after a mode switch.

Fast μP speeds affect memory accesses as well as bus timing. Remember that a fast processor can drive up system cost if you must use correspondingly fast memory to support it. The 80286 inserts clock cycles, or wait states, within its machine cycle while it's waiting for a slow device (like a 120-nsec dynamic RAM) to return the ready line high. During wait states, the 286 does nothing. You've probably seen the ads for 10- and 12-MHz PC/AT clones that mention in fine print (if at all) that the RAM requires three wait states—nullifying the processor's speed advantage.

Paged architecture's available

CTI uses a paged/interleaved memory architecture to enable fast response from slow 120-nsec dynamic RAM in a fast 12-MHz system. The 80286 memory architecture is set up in pages. Normally, you use one word to specify the page and the next word to specify the location within the page. Because most memory accesses are sequential, CTI's interleaving scheme prefetches the next memory location and assumes it will be within the same page, thus saving the fetch operation of the page word.

As a consequence, if the next memory location that the RAM requires is in the same page, no additional wait states are necessary. If it isn't in the same page and the RAS signal is high, there's one wait state for a read memory access and one for a write memory access. If it isn't in the same page and the RAS signal is low, there are three wait states for a read operation and two for a write operation. CTI claims that, in the course of using a common program like Lotus 1-2-3, you'll find the average number of hits and misses in prefetching the next address yields an effective wait state of 0.7. Keep in mind, however, that one wait state is always required for a memory-write operation—the 0.7 figure refers to the *average* number of wait states. Although you can use 120-nsec dynamic RAM with CTI's chip set to achieve the 0.7 effective wait states, you need to use the more-expensive 100-nsec dynamic RAMs with 16-MHz systems.

Shadow RAM speeds BIOS

A PC/AT compatible's basic input/output system (BIOS) is stored in ROM, which can be slower than the slowest dynamic RAM. (The BIOS assigns interrupts to the interrupt vector table, handles keyboard communications, and generally performs basic functions that must be present for the disk operating system to communicate with the hardware.) At the faster μP speeds, the BIOS PROM access times force the μP to insert additional wait states. By transferring the BIOS software from ROM into fast RAM (shadow RAM) at power-on, you speed BIOS execution time. Instead of accessing the slow ROM, the CPU obtains BIOS instructions from the fast shadow RAM. All three of the newer chip sets offer the shadow-RAM feature.

Faraday's chip set also lets you access the 8-bit BIOS instructions as 16-bit words. Note that the ability to operate with 16-bit words instead of 8-bit bytes doesn't automatically double the BIOS software's execution speed, because most of the BIOS-related hardware, such as the EGA (enhanced graphics adapter) operates on an 8-bit bus.

IBM has copyrighted its BIOS, and thus your computer will require a set of compatible BIOS software routines from a third party. The most popular BIOS ROMs are Phoenix's (Norwood, MA) and Award's (Los Gatos, CA). These BIOS routines are fully compatible with IBM's, so most of the clone manufacturers use them. No major complaints have been reported. Faraday is the only chip-set manufacturer that has developed its own BIOS.

Although CTI's previous chip sets could use IBM's own BIOS PROM, the CS8221 doesn't because of the extensive μP register setup that must occur before the BIOS is loaded. CTI provides the register setup software that you have to load prior to loading the BIOS into the shadow RAM. Phoenix expects to have these setups incorporated into its BIOS by the next quarter.

CTI's, Faraday's, and Zymos's chip sets increase their memory size over a standard IBM PC/AT by

For more information . . .

For more information on the chip sets discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Chips and Technologies Inc
521 Cottonwood Dr
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G2 Inc
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VLSI Technology Inc
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(602) 893-8574
Circle No 733

Faraday Electronics Inc
749 N Mary Ave
Sunnyvale, CA 94086
(408) 749-1900
TLX 706738
Circle No 730

Logicstar Inc
4160-B Technology Dr
Fremont, CA 94538
(415) 651-2796
TWX 510-601-1813
Circle No 732

Zymos Corp
477 N Matilda Ave
Sunnyvale,CA 94086
(408) 730-5400
TWX 910-339-9530
Circle No 734

using some version of the Lotus-Intel-Microsoft extended-memory scheme (LIM EMS) **(Ref 1).** The LIM EMS standard supports a system RAM to a maximum of 8M bytes; CTI and Faraday implement this version. Zymos implements LIM EMS 4.0, which supports a system RAM of 16M bytes max.

If none of the chip sets discussed here exactly suits your application, consider customization, either at the chip or board level. A chip-set manufacturer's ability to offer versions customized for your applications varies, depending on the background of the manufacturer. VLSI Technology and Zymos both stress their ability to easily customize the basic chip sets; both companies started in the ASIC business.

Customizing a chip set provides several advantages. Your product is no longer based on a commodity chip set available to your competition; plus, you can optimize the product for your particular application. However, the disadvantages may be stronger. For example, because your product isn't an off-the-shelf item, longer turnaround times are likely.

CTI, the first vendor to offer PC/AT replacement chips, has only lately begun to mention that it can provide customized versions of its chips. However, it recommends them only for high-volume (25,000 to 50,000) applications.

Faraday, like CTI, lacks a background in custom ASIC services and gives little encouragement to its customers to customize. Instead, the company takes advantage of the extensive SMT board facilities of its parent company, Western Digital, and recommends that you customize the support circuitry surrounding the chip set.

Before you decide on an off-the-shelf chip set vs a custom design, you may want to try an evaluation board, which all of the chip-set manufacturers offer. Rather than commit to any chip set without verifying how it will perform with your software, you can test the chip set on a PC bus-based board. **Table 1** lists prices. **EDN**

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Vertical Sensitivity	2 mV/div	2 mV/div	2 mV/div	2 mV/div	2 mV/div
Trigger Frequency	500 MHz	500 MHz	500 MHz	500 MHz	250 MHz
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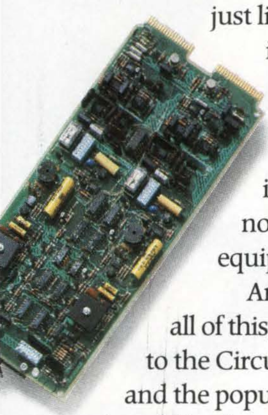

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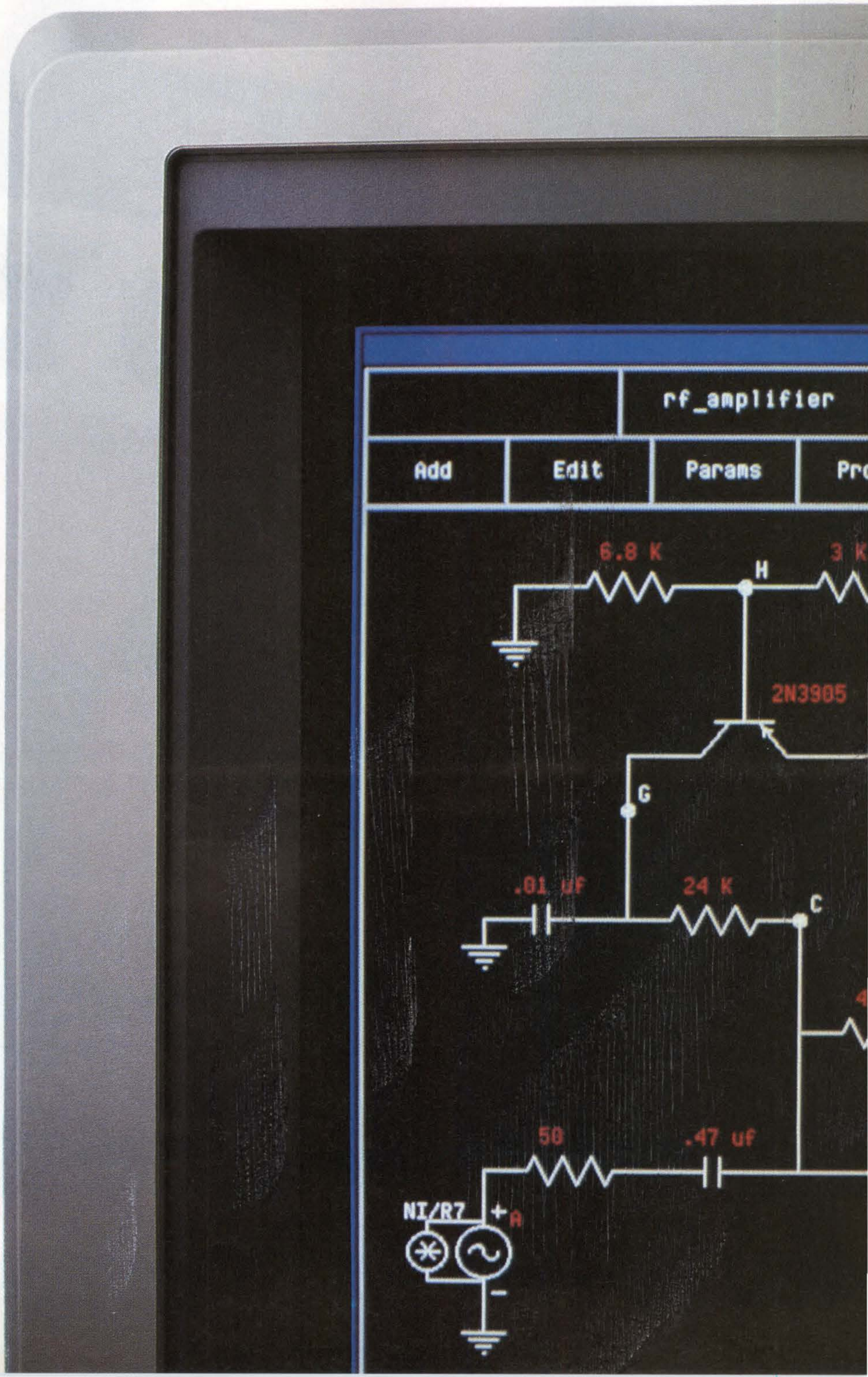

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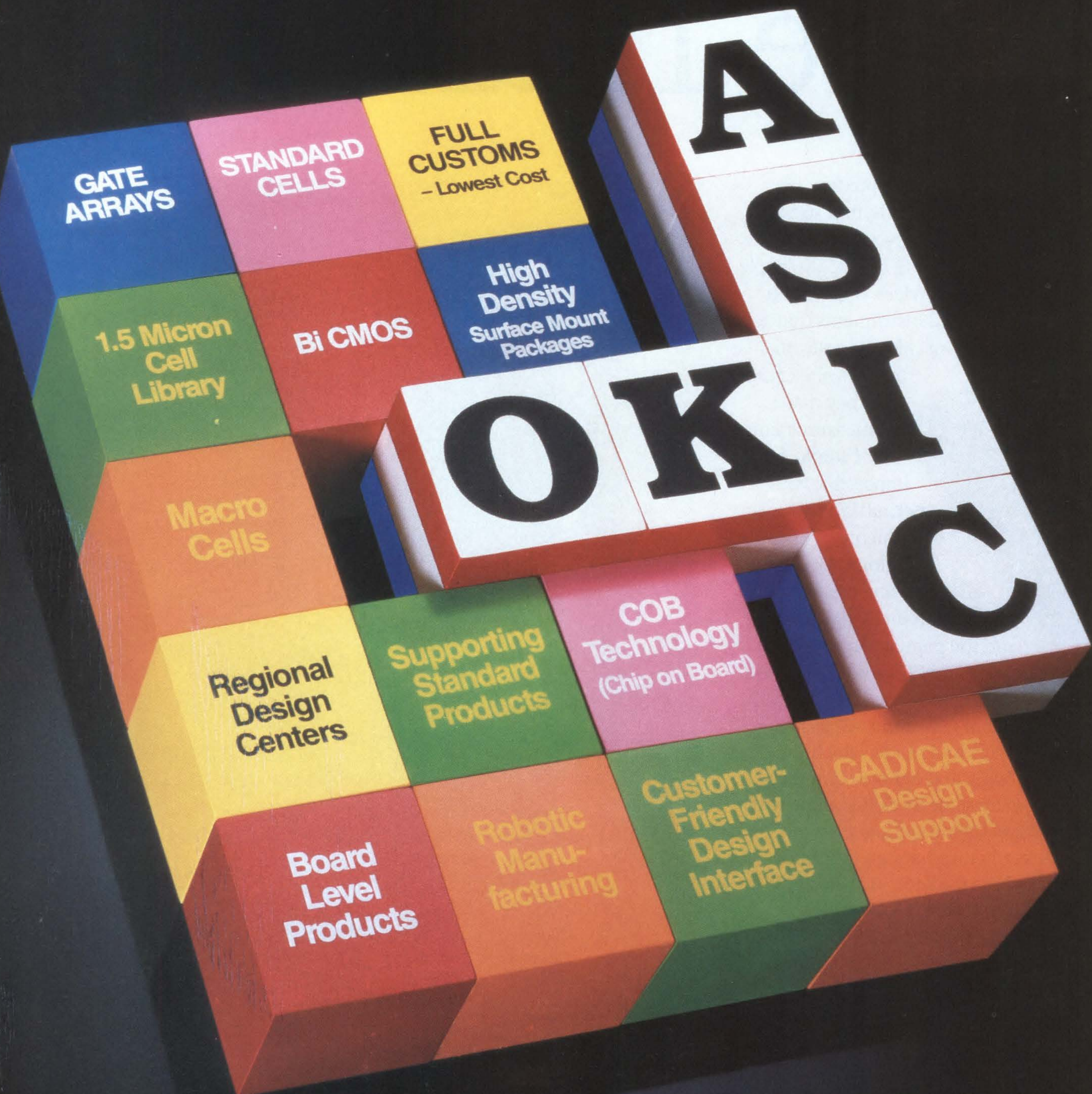

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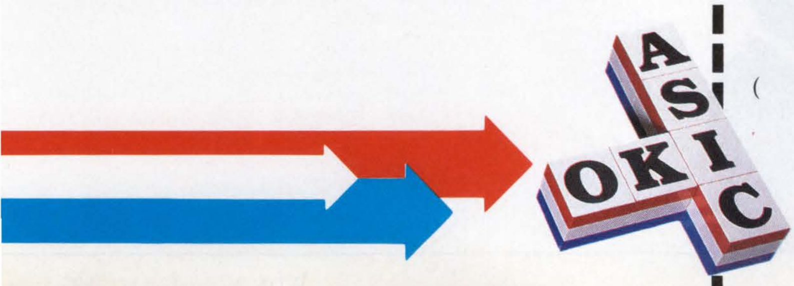

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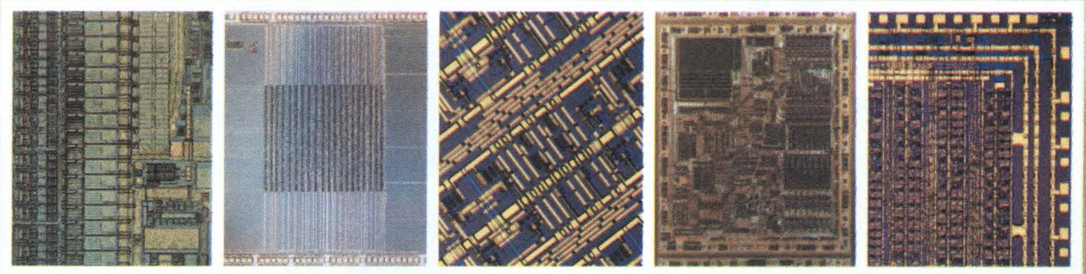

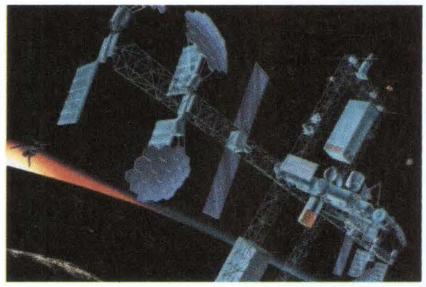

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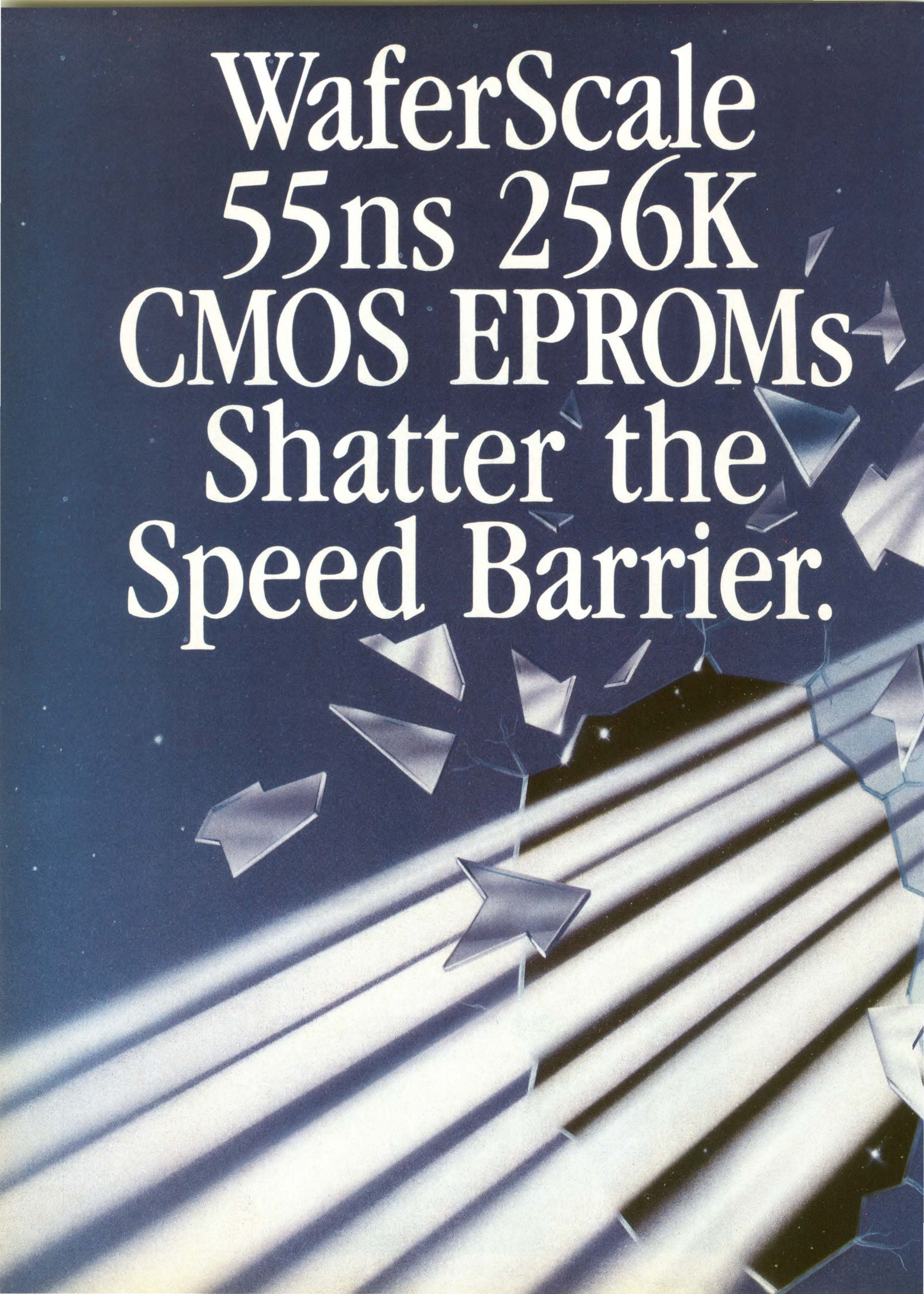
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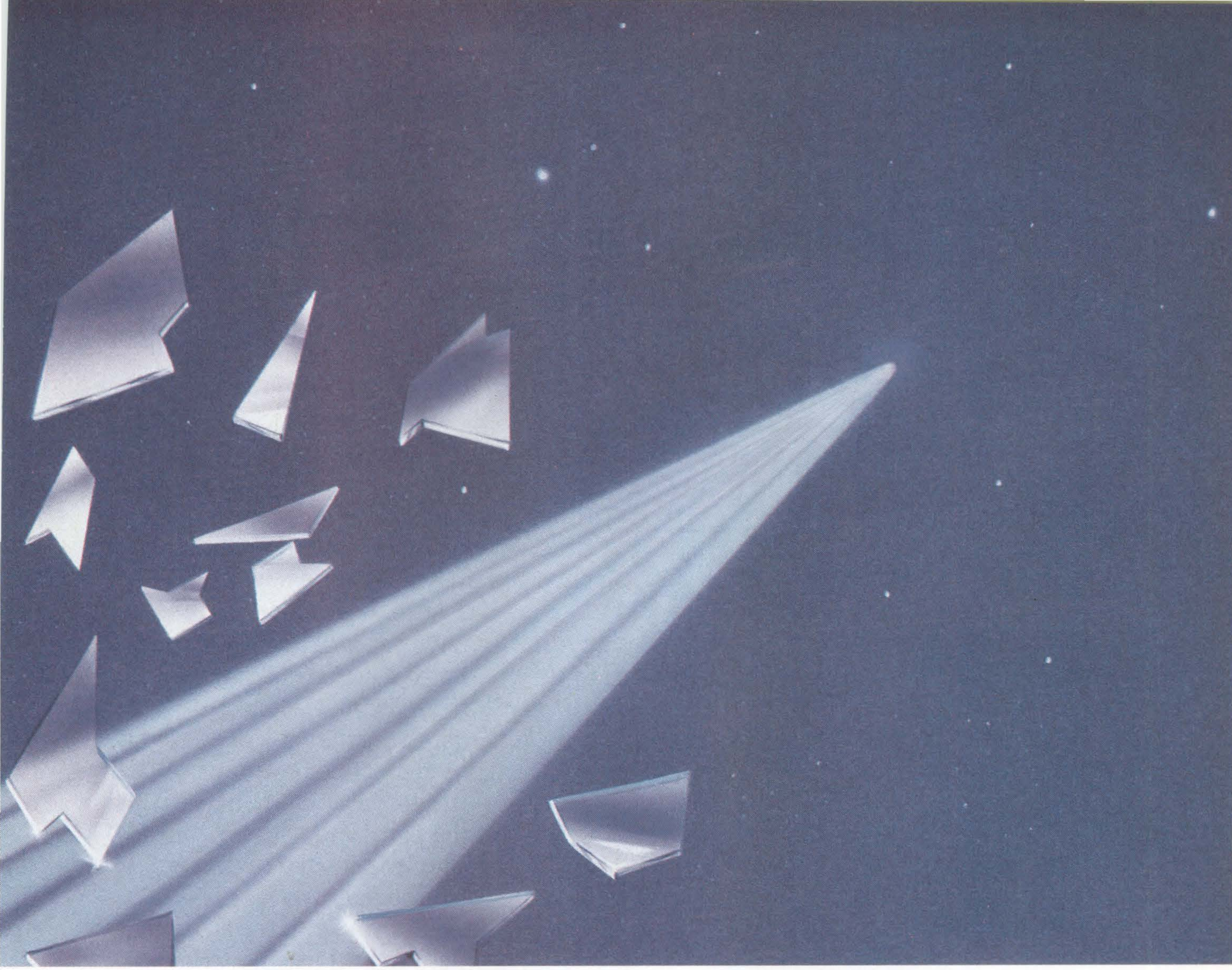

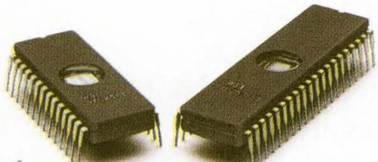

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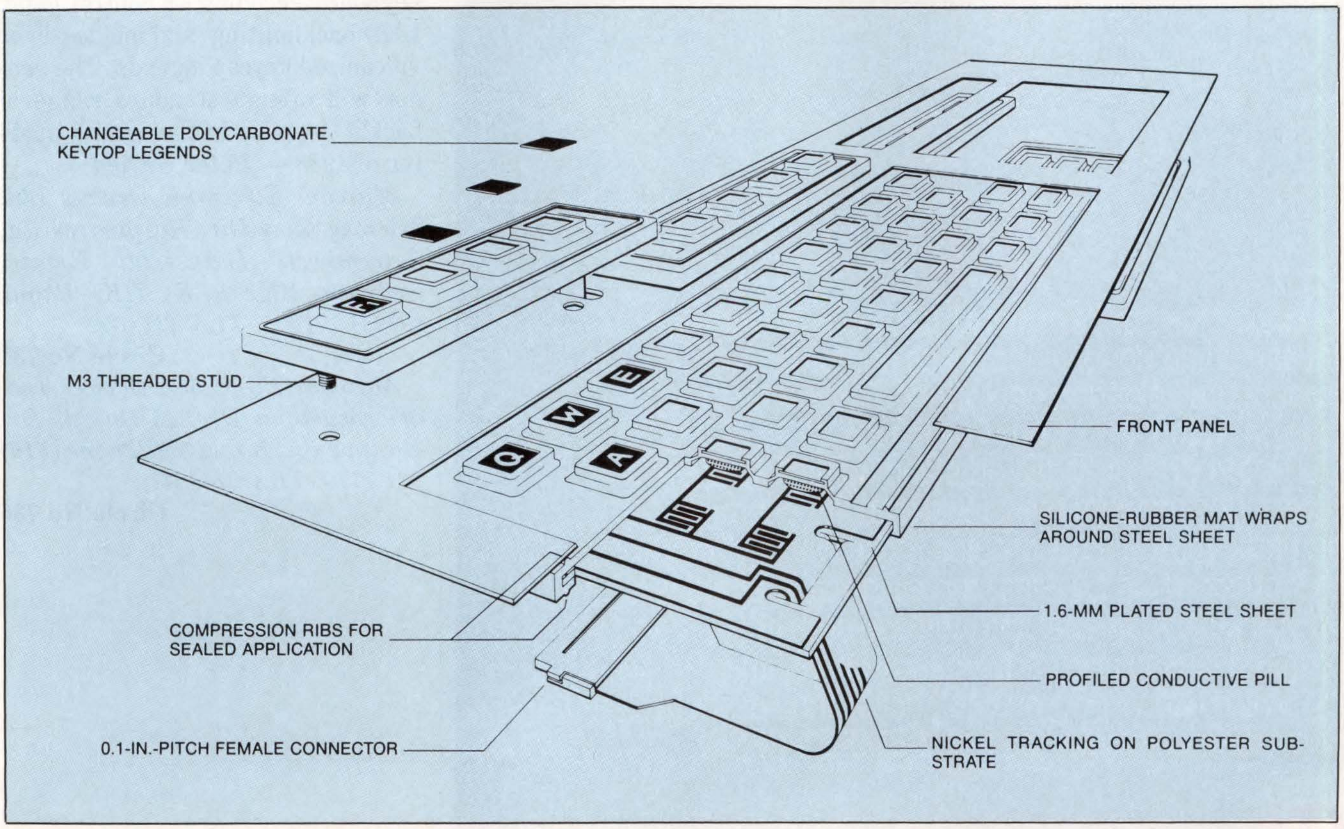
The keyboards incorporate a 1-piece silicone-rubber molding that is profiled, providing raised keys. Because they're self-supporting, both laterally and vertically, these raised keys don't require the rigid keyswitch housings often found in other conductive-rubber keyboards. As a result, the keyboards have no cracks or crevices that can harbor dust and dirt, and you can clean them by scrubbing them down. The silicone-rubber molding fits over a metal backplate that also supports a plastic film on which the switch-contact traces are printed. The plastic film also provides a flexible leadout for connections to the switch matrix; the leadout is terminated in a 0.1-in.-pitch connector.

When you press a key, the silicone-rubber molding deforms to provide 1.4 mm of switch travel, as well as tactile feedback. Conductive-rubber inserts molded into the silicone-rubber provide the moving switch contacts. The keyboard retains its tactile feedback and switch-contact performance even if you strike the keys hard or off-center.

The switches have a maximum contact bounce of 5 msec and a maximum contact resistance of 200Ω. You can operate them at voltages as high as 24V dc and at currents as high as 50 mA. The force required to operate each key is typically 1.16 oz (160g). The vendor claims the keyswitches have a typical lifetime of 2 million operations without noticeable fatiguing of the silicone



While retaining tactile feedback and positive key travel, *the self-supporting keys of the SF62000-Input conductive-rubber keyboards eliminate the need for rigid switch housings. As a result, the keyboards have no cracks or crevices to harbor dust and dirt, and you can scrub them down.*

rubber or unacceptable degradation of switch performance. In addition, the keyboards operate over −55 to +125°C, so they're suitable for use in military equipment.

The keyboards are available with gray, black, or brown silicone-rubber moldings and a range of interchangeable keycap inserts with alphanumeric or symbolic legends. When you use the integral threaded mounting studs to mount one of these keyboards on a front panel, a lip around the edge of the silicone-rubber molding provides an environmental seal between the keyboard and the front panel.

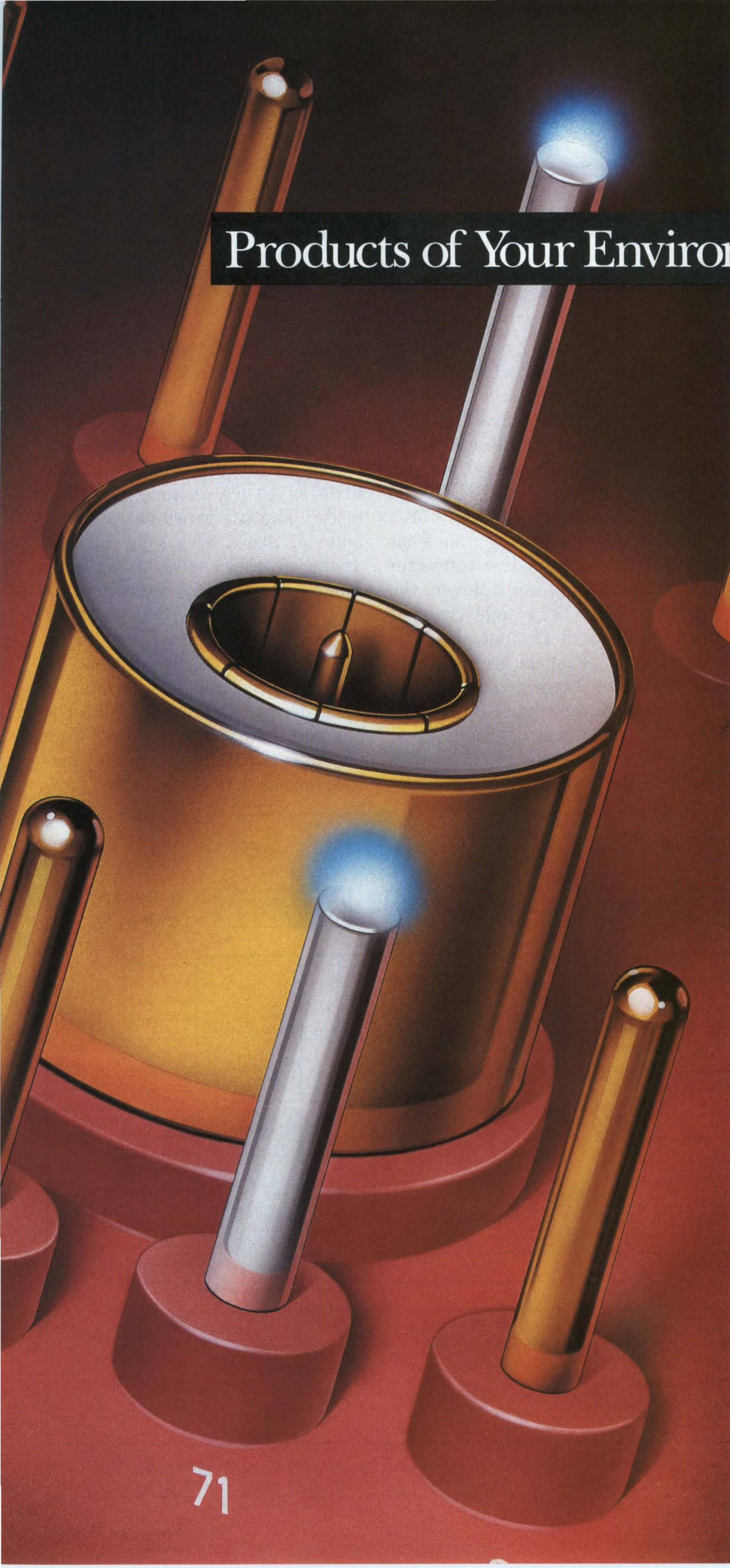
You can also mount the keyboards alongside one another to create more complex switch panels. The SF62000-Input keyboards, which were developed in conjunction with Keymat Technology Ltd (London, UK), range in price from $24 for the 4-key keypad to $75 for the qwerty keyboard. You can order custom keyboards that incorporate integral keyboard encoding or control logic, LED backlighting, and molded-in or vulcanized keycap legends. The vendor will offer a standard range of backlit keypads in the second quarter of 1988.— ***Peter Harold***

Marconi Electronic Devices Ltd, Microsystems Div, Hargreaves Rd, Groundwell Industrial Estate, Swindon SN2 5BE, UK. Phone (0793) 727005. TLX 444460.

Circle No 735

Marconi Electronic Devices Inc, Microsystems Div, 45 Davids Dr, Hauppauge, NY 11788. Phone (516) 231-7710. TLX 275801.

Circle No 736



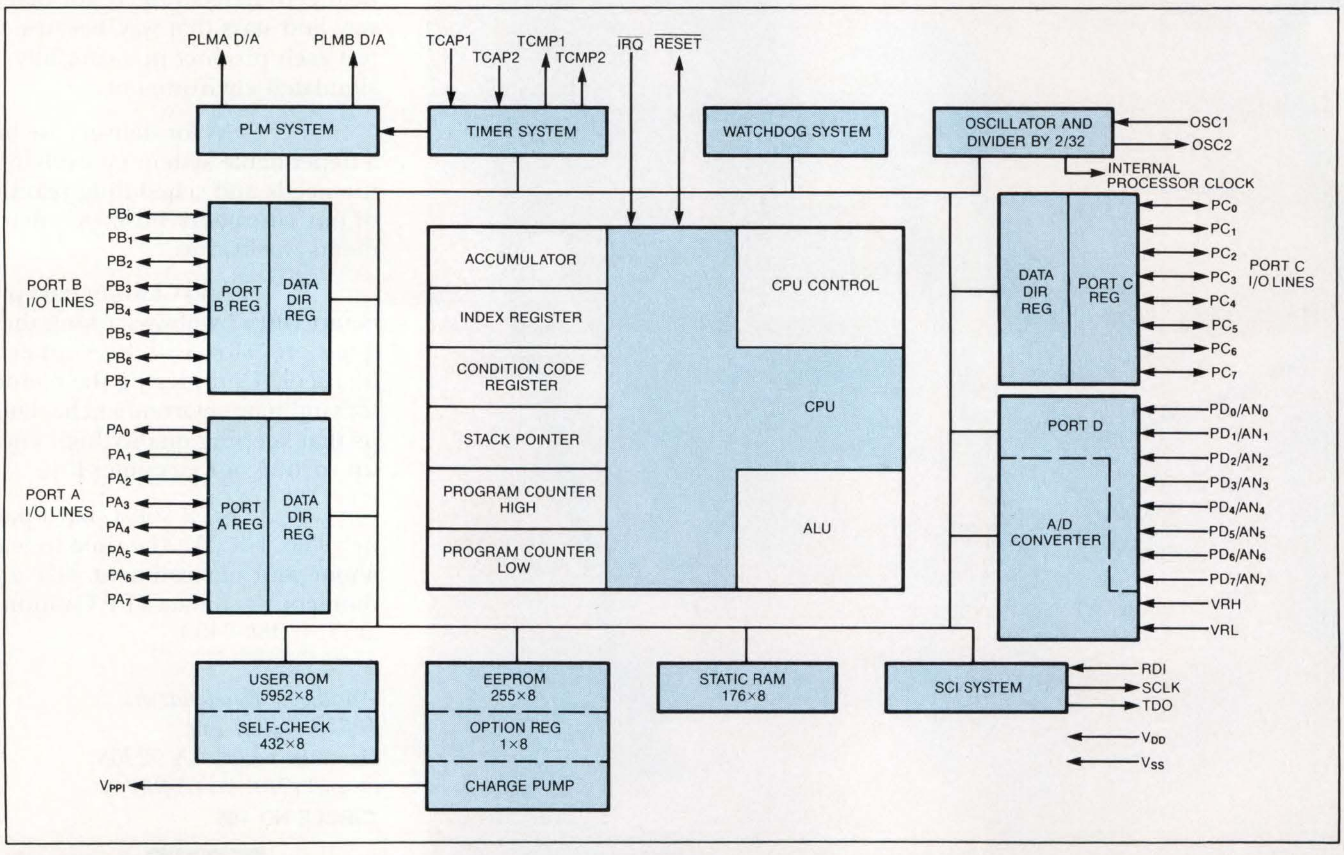
High-speed CMOS 8-bit μC provides on-chip ADC and nonvolatile EEPROM

You can think of the MC68HC05B6 as an upgraded version of an MC68HC05C4. The manufacturer of this 8-bit, single-chip μC took the CPU core of an MC68HC05C4 and added an 8-channel A/D converter, two pulse-length-modulation (PLM) systems, 1792 additional bytes of ROM, eight more bidirectional I/O lines, a serial communications interface (SCI) that allows you to select a separate baud rate for the transmitter and receiver, a software-selectable Slow Mode, and a software-programmable external interrupt.

If you need more EEPROM, you can order the MC68HC805B6, a version that provides 6k bytes of EEPROM and no ROM. If you don't require EEPROM, you can select the MC68HC05B4, which has 4k bytes of ROM.

The on-chip A/D converter is the key feature that lets these B-series μCs bridge the functional gap between the low-end MC68HC05C4 and the memory-laden MC-68HC11A8. Comprising an 8-bit successive-approximation converter and a 16-channel multiplexer, the A/D converter links eight channels to the μC's Port D input pins. The other eight channels are dedicated to internal reference points for test functions. Rather than being driven by the heavily loaded system-power supply lines, two dedicated pins supply the converter's reference voltage to prevent any degradation of conversion accuracy.

The static design of these B-series devices lets you operate at frequencies as low as dc, thus reducing the chip's power consumption to as little as 10 μA in the μC's Stop mode. The μC consumes a maximum of 9 mA of supply current during normal operation. In Slow Mode, its current consumption drops to 2 mA. When you select the Slow Mode function, you add an extra divide-by-16 circuit between the chip's oscillator and its internal clock driver, thereby dropping the bus speed to 16 times slower than nominal—a particularly useful feature for use with the μC's two pow-



The MC68HC05B6 1-chip μC is an upgraded version of the MC68HC05C4; *it includes an on-chip A/D converter, 256 bytes of EEPROM, and bidirectional I/O for synchronous and asynchronous communication.*

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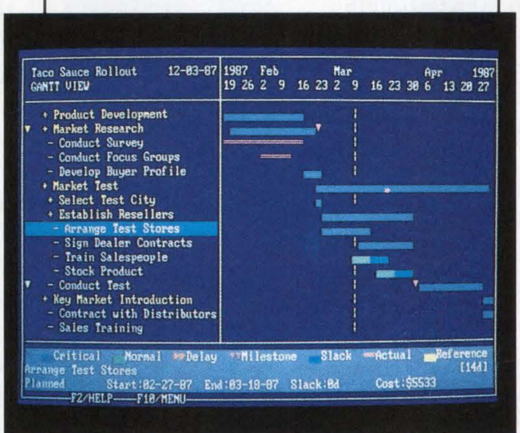

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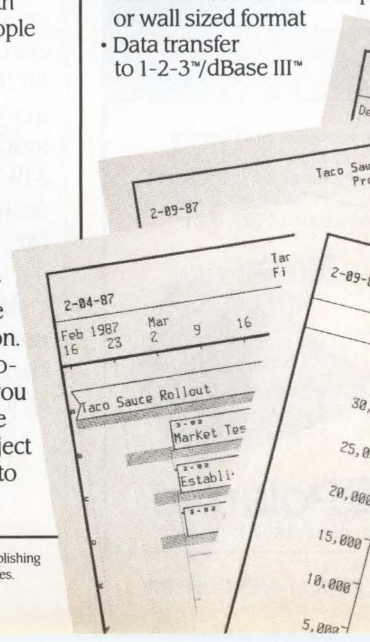

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CIRCLE NO 185

er-saving standby modes (Stop and Wait), during which current consumption can drop to 10 μA.

The on-chip, full-duplex, asynchronous SCI comes with a standard NRZ format and a variety of baud rates. Although the SCI's transmitter and receiver are functionally independent and have separate baud-rate generators, they share a common baud-rate prescaler and data format. You can execute software commands to select from one of 32 different baud rates; for each transmit baud rate there are eight possible receive baud rates. The SCI's advance-error-detection feature can spot noise at 1/16th the time that it takes 1 bit to pass through the SCI. The SCI also lets you implement transmitter clocks without altering the regular transmit or receive functions.

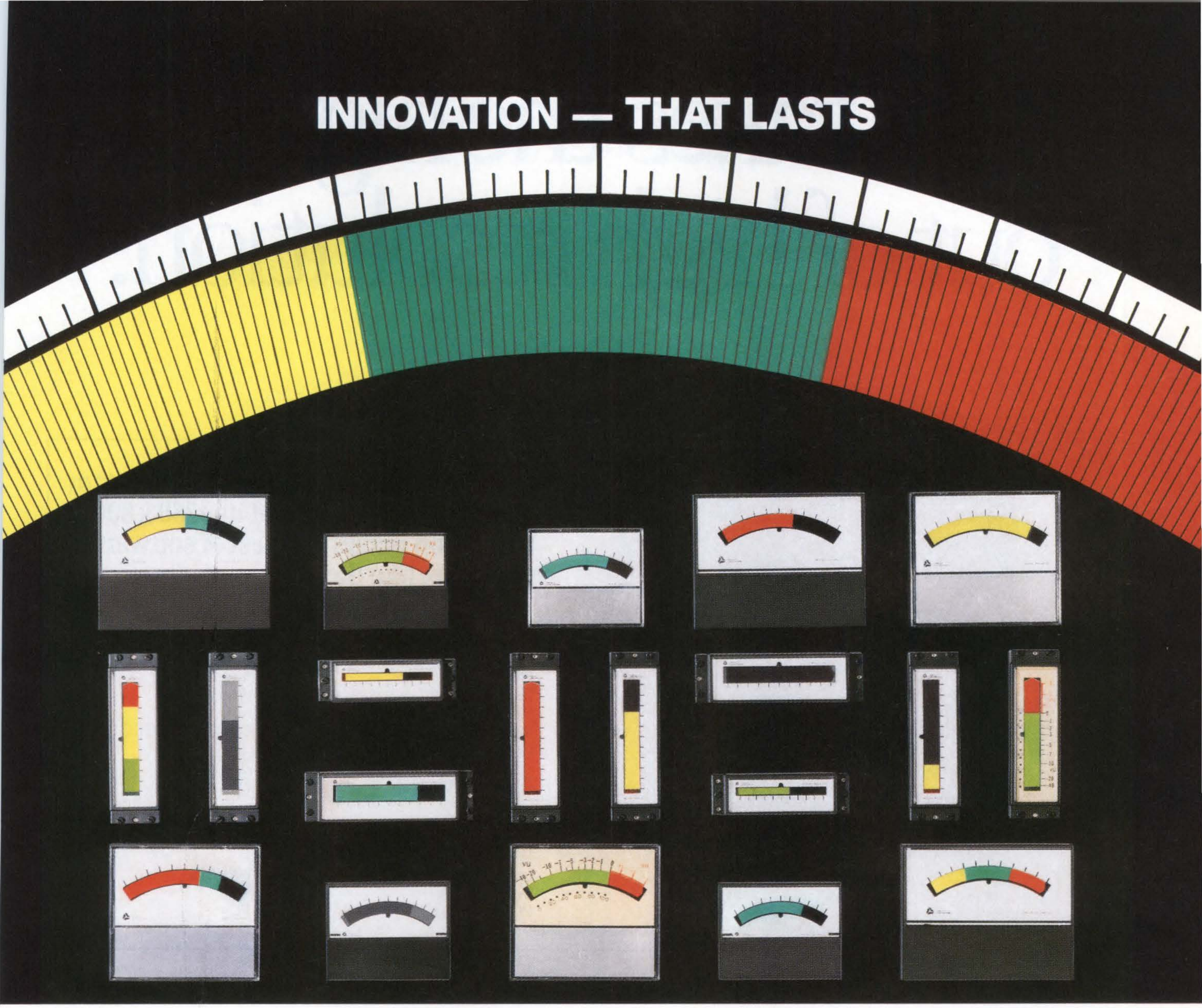
The MC68HC05B6 comes with 176 bytes of RAM, 5952 bytes of ROM, 256 bytes of byte-erasable EEPROM, 32 bidirectional I/O lines, a 16-bit timer, a watchdog counter, a crystal oscillator, a single 3 to 6V supply, and an external reset pin. Its software features include an 8×8 unsigned multiply instruction, addressing modes with indexed addressing for tables, and memory-mapped I/O. Its software is upwardly compatible with software for the MC146805 CMOS μC family.

Housed in either a 52-pin PLCC or a 48-pin DIP, the MC68HC05B6 costs $4.90 (OEM qty). The MC68HC05B4 sells for $4 (OEM qty), and the MC68HC805B6 is available in limited quantities for $49.50. For $500, you can order evaluation modules of the MC68HC05B6 for development support.

—J D Mosley

Motorola Inc, 6501 William Cannon Dr W, Mail Drop OE39, Austin, TX 78735. Phone local sales office.

Circle No 737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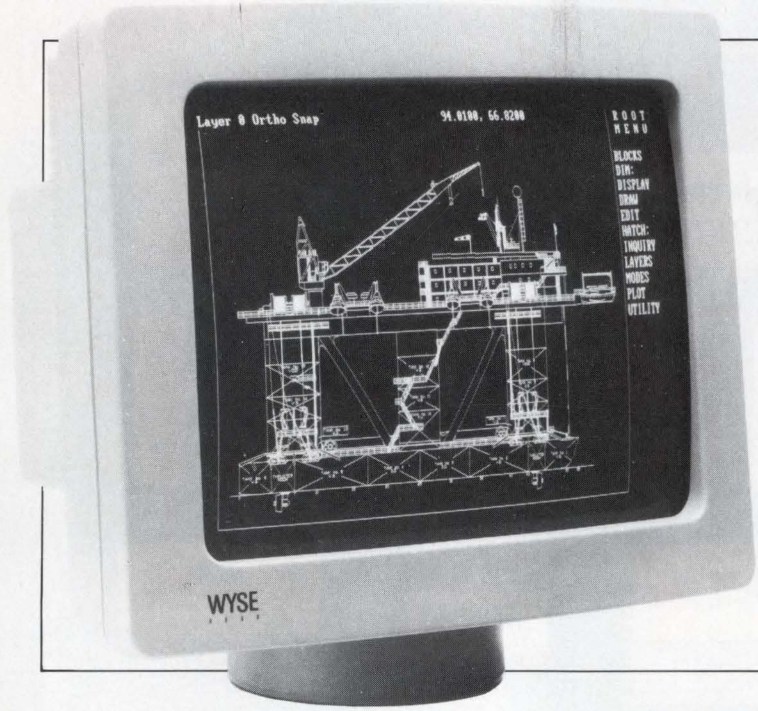

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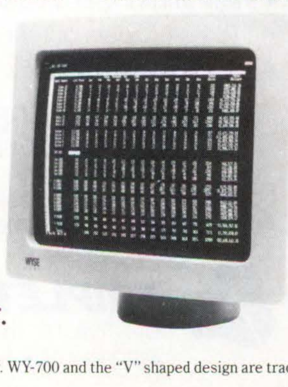
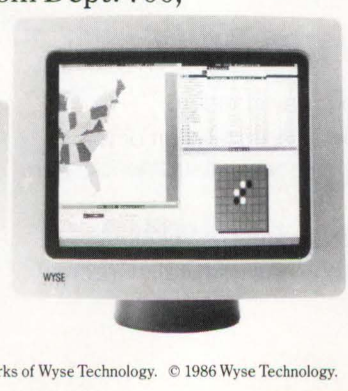




Your next destination:

READERS' CHOICE

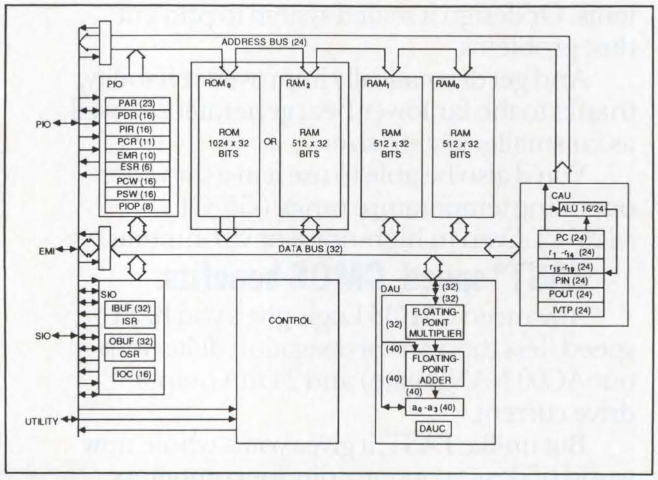
Of all the new products covered in EDN's **September 3, 1987,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **September 3, 1987,** issue.

▲ EEPROM PROGRAMMER

You can control the Writer-RX single-socket (28-pin) EEPROM programmer with a nonintelligent terminal or an IBM PC (pg 279).
Bytek Corp.
Circle No 602

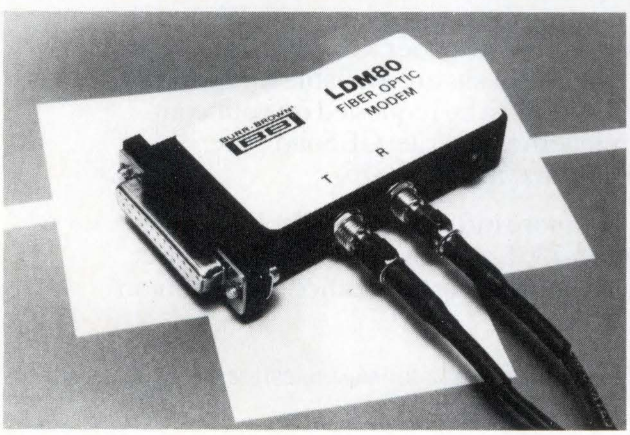
ANSWERING MACHINE

The CAM turns any IBM PC/XT, PC/AT, or compatible PC into a smart telephone-answering machine. Using its onboard μP, the board digitizes the caller's voice and stores it on the computer's hard disk (pg 259).
The Complete PC Inc.
Circle No 604



▲ CMOS DSP IC

The Model WE DSP32C CMOS floating-point digital signal processor (DSP), which features cycle times as low as 80 nsec, is targeted at high-performance applications such as graphics, telecommunications, image processing, high-speed control, and speech processing (pg 99).
AT&T Technology Systems.
Circle No 603



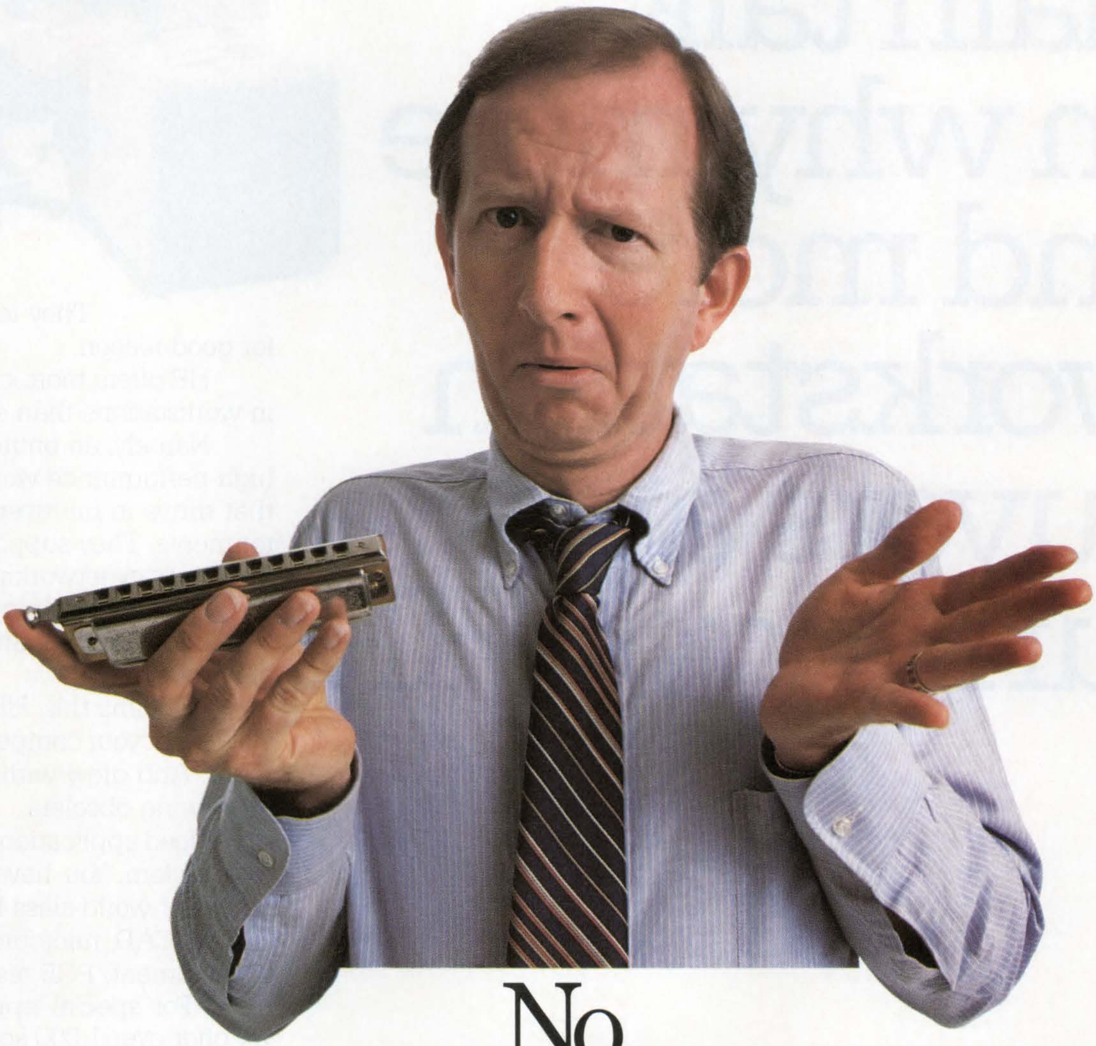
▲ OPTICAL MODEM

The LDM80 fiber-optic modem is completely powered by the host RS-232C port signals and requires no external power-supply connection (pg 264).
Burr-Brown Corp.
Circle No 605

C COMPILER

Turbo C is a C editor, compiler, and linker that runs on the IBM PC and compatibles. It conforms to the Kernighan/Ritchie and proposed ANSI standards (pg 286).
Borland International.
Circle No 601

You've made power supplies smaller, lighter and quieter with a harmonica?



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Division of Valor Electronics, Inc.

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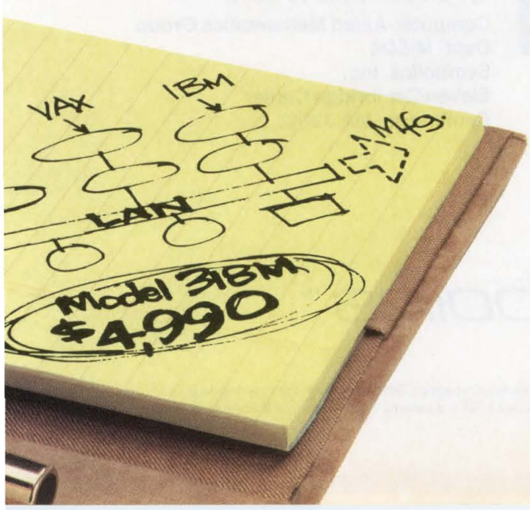

HEWLETT PACKARD

CIRCLE NO 102

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LEADTIME INDEX

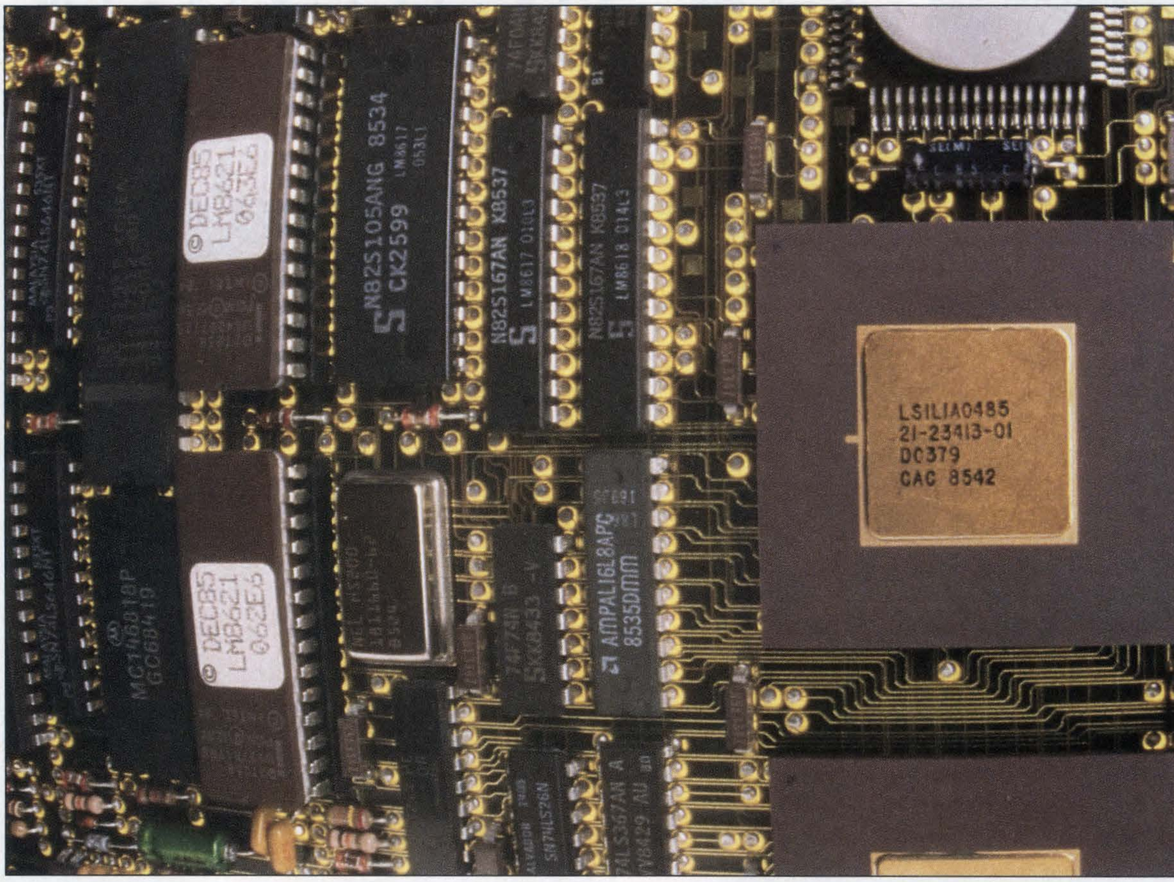
Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	12	63	12	13	0	10.5	8.6
Pot-Core	0	14	43	29	14	0	12.0	9.7
Laminate (power)	0	27	47	26	0	0	8.7	9.2
CONNECTORS								
Military panel	0	0	100	0	0	0	8.0	9.9
Flat/Cable	19	25	50	6	0	0	5.7	5.0
Multi-pin circular	20	20	40	20	0	0	6.9	6.6
PC (2-piece)	0	40	50	10	0	0	6.8	5.8
RF/Coaxial	20	54	13	13	0	0	4.7	5.6
Socket	27	50	18	5	0	0	3.7	4.1
Terminal blocks	11	61	22	6	0	0	4.5	4.3
Edge card	0	62	31	7	0	0	5.5	7.0
D-Subminiature	6	50	38	6	0	0	5.5	6.4
Rack & panel	0	33	34	33	0	0	8.8	8.9
Power	0	12	75	13	0	0	8.3	5.7
PRINTED CIRCUIT BOARDS								
Single-sided	6	47	41	6	0	0	5.6	5.3
Double-sided	4	28	60	8	0	0	6.9	7.0
Multi-layer	0	18	65	17	0	0	8.4	9.3
Prototype	0	77	23	0	0	0	4.2	4.1
RESISTORS								
Carbon film	45	17	31	7	0	0	4.1	3.7
Carbon composition	44	12	32	12	0	0	4.8	3.3
Metal film	27	32	32	9	0	0	4.9	4.1
Metal oxide	7	43	43	7	0	0	5.8	6.0
Wirewound	19	25	25	25	6	0	8.2	7.2
Potentiometers	13	33	37	17	0	0	6.6	4.5
Networks	18	29	35	18	0	0	6.4	6.3
FUSES	59	27	5	9	0	0	2.6	4.2
SWITCHES								
Pushbutton	20	35	40	5	0	0	5.0	6.4
Rotary	5	48	42	5	0	0	5.6	6.2
Rocker	7	50	36	7	0	0	5.5	6.4
Thumbwheel	12	29	41	18	0	0	6.9	9.3
Snap action	18	27	37	18	0	0	6.5	7.0
Momentary	13	40	40	7	0	0	5.4	7.1
Dual in-line	0	33	50	17	0	0	7.6	6.9
WIRE AND CABLE								
Coaxial	17	44	28	11	0	0	5.3	4.3
Flat ribbon	11	56	33	0	0	0	4.3	5.1
Multiconductor	13	47	33	7	0	0	5.1	6.2
Hookup	30	44	22	4	0	0	3.7	2.8
Wire wrap	15	54	23	8	0	0	4.7	2.3
Power cords	33	29	29	9	0	0	4.5	6.0
POWER SUPPLIES								
Switcher	0	0	55	36	9	0	12.3	6.2
Linear	0	39	22	39	0	0	9.0	6.7
CIRCUIT BREAKERS	29	14	36	14	7	0	7.3	5.6
HEAT SINKS	19	33	43	5	0	0	5.2	4.8
RELAYS								
General purpose	9	48	38	5	0	0	5.2	4.4
PC board	6	30	30	34	0	0	8.7	7.7

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
Dry reed	11	22	56	11	0	0	6.8	8.0
Mercury	13	13	37	37	0	0	9.2	7.5
Solid state	0	50	30	20	0	0	7.0	7.5
DISCRETE SEMICONDUCTORS								
Diode	30	17	27	23	3	0	7.1	4.8
Zener	23	23	31	19	4	0	7.1	5.4
Thyristor	0	25	25	50	0	0	10.5	8.0
Small signal transistor	20	20	15	45	0	0	8.8	7.5
MOSFET	13	31	25	31	0	0	7.8	7.9
Power, bipolar	0	40	20	40	0	0	9.0	8.4
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	10	15	35	40	0	0	9.5	8.4
CMOS	13	23	41	23	0	0	7.5	6.4
TTL	12	44	19	25	0	0	6.7	6.0
LS	19	33	19	29	0	0	7.0	6.1
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	9	27	35	27	0	0	8.0	8.2
OP amplifier	14	33	33	20	0	0	6.8	7.9
Voltage regulator	12	41	35	12	0	0	5.9	5.8
MEMORY CIRCUITS								
RAM 16k	10	20	50	20	0	0	7.7	7.7
RAM 64k	13	27	33	20	0	7	8.6	7.1
RAM 256k	0	34	25	33	8	0	10.3	8.7
RAM 1M-bit	0	9	27	46	18	0	14.1	10.0
ROM/PROM	7	27	33	33	0	0	8.6	7.1
EPROM 64k	7	33	13	40	7	0	10.0	7.7
EPROM 256k	6	25	31	38	0	0	9.1	8.8
EPROM 1M-bit	0	11	44	45	0	0	10.8	8.3
EEPROM 16k	0	33	34	33	0	0	8.8	8.5
EEPROM 64k	11	11	44	34	0	0	9.1	8.0
DISPLAYS								
Panel meters	25	25	25	25	0	0	6.6	9.9
Fluorescent	0	14	29	57	0	0	11.6	12.5
Incandescent	0	33	34	33	0	0	8.8	8.6
LED	27	27	27	19	0	0	6.0	7.5
Liquid crystal	0	0	50	38	12	0	13.0	9.7
MICROPROCESSOR ICs								
8-bit	6	22	39	33	0	0	8.9	6.8
16-bit	8	23	46	23	0	0	8.0	8.3
32-bit	0	15	23	54	8	0	12.6	12.5
FUNCTION PACKAGES								
Amplifier	10	20	30	40	0	0	9.2	9.4
Converter, analog to digital	0	37	27	36	0	0	8.9	9.3
Converter, digital to analog	0	45	22	33	0	0	8.3	8.6
LINE FILTERS		43	29	14	14	0	9.4	7.9
CAPACITORS								
Ceramic monolithic	21	29	38	8	4	0	6.2	4.8
Ceramic disc	23	35	15	23	4	0	6.8	4.7
Film	25	20	35	15	5	0	7.0	5.0
Aluminum electrolytic	23	27	19	27	4	0	7.5	5.5
Tantalum	19	39	19	19	4	0	6.7	5.6
INDUCTORS	0	50	34	8	0	8	8.0	6.3

Source: *Electronics Purchasing* magazine's survey of buyers

If you're not finding Gate Array, Advanced Schottky, and SMT faults, maybe the fault lies with your tester.



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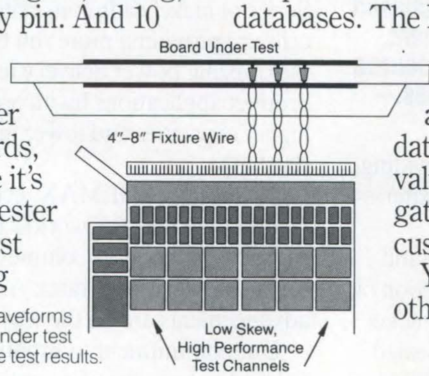
Most importantly, the L210i delivers 95% or greater fault coverage on VLSI boards, in just 1–2 months. Because it's the first and only in-circuit tester that handles the three biggest problems in in-circuit testing today.



The L210i delivers waveforms accurately at the board under test for repeatable test results.

Test ASIC's ASAP.

One of the biggest problems for in-circuit testers today is ASIC's. If they detect ASIC faults at all, it's only because you've spent weeks and weeks programming them.

Not so with the L210i. It has a unique VLSI device tester architecture. So you can use patterns from device design and test databases. The L210i's translators convert patterns quickly.

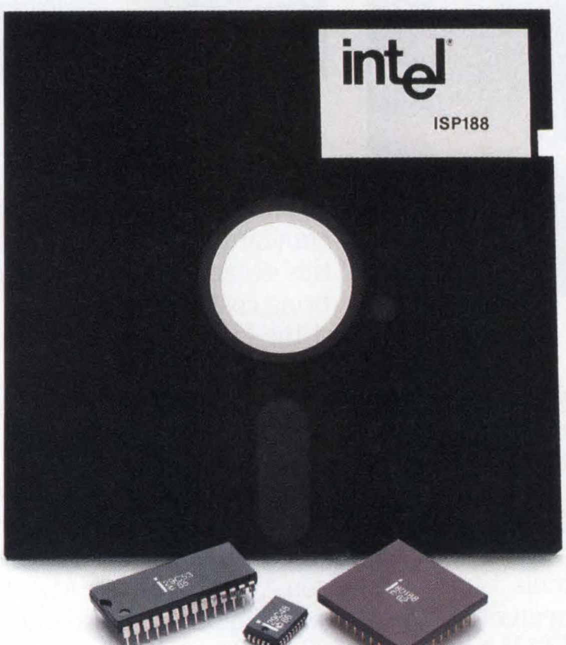
Plus, the L210i stores and processes lengthy test data efficiently. So you save valuable time in testing gate arrays and other semi-custom devices.

You won't find that in any other in-circuit tester.

CIRCLE NO 112

TO THE MILLIONS OF WORDS THAT HAVE BEEN WRITTEN ABOUT ISDN, WE'D LIKE TO ADD A NEW ONE.

COMPLETE.



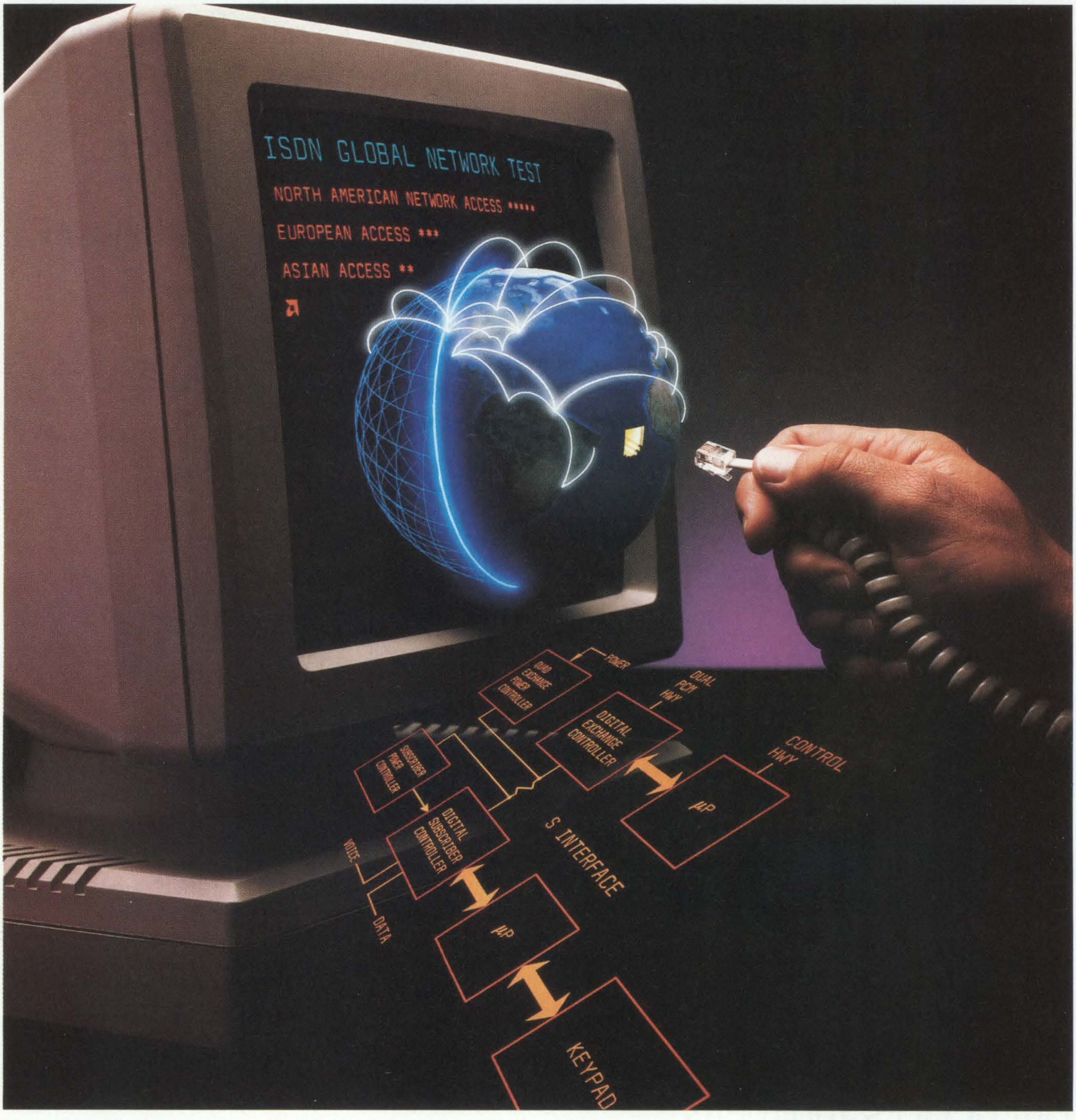
For years, you've read about the incredible new products you can design when ISDN becomes a reality. And now, you can stop waiting and finally get started. Because our 29C53 ISDN Kit delivers what most people have only been writing about. A complete ISDN solution.

There's our 29C53 "S" Transceiver, which transmits and receives data at the ISDN basic rate of 192 kbps. And fully implements Open Systems Interconnection (OSI) Layer 1. There's our programmable 29C48 Voice Conversion Chip. And our 80188 CPU, which performs protocol processing.

But that's just the beginning. What really puts you ahead is our ISP188 software, which completes OSI layers 2 and 3.

SPECIAL REPORT

Integrated Services Digital Network



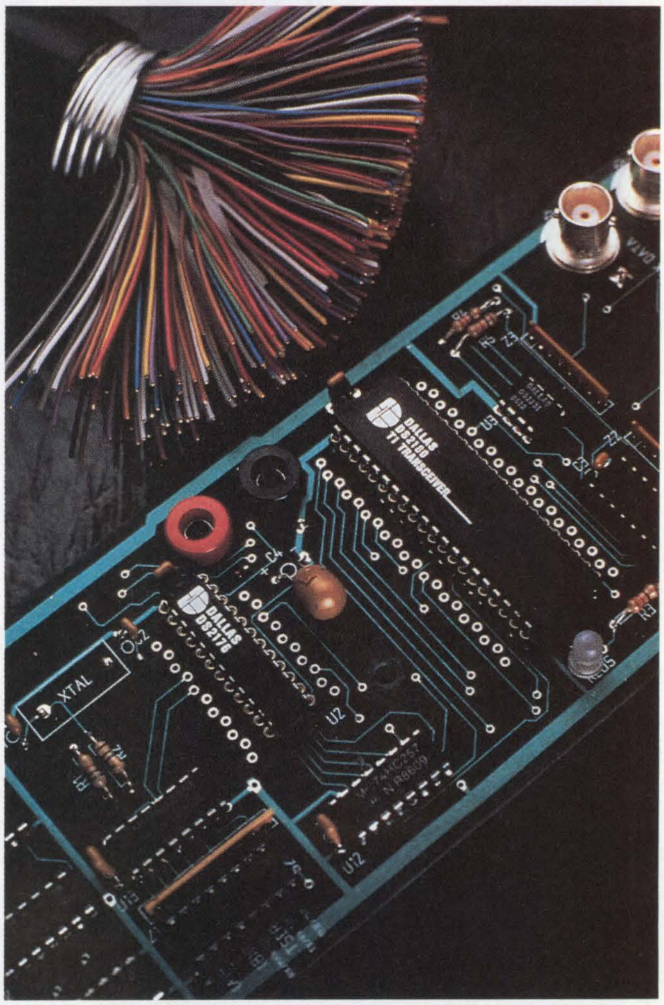
The Integrated Services Digital Network (ISDN) stands poised to transform the world's telecomm network into an all-digital system. The demand for ISDN equipment, which combines telephone and data-communications functions, may create the next boom market in electronics. ISDN services will be available by 1990.

KEEPING AMERICA COMPETITIVE

Steven H Leibson, *Regional Editor*

Since early in this decade, two major telecommunications standards organizations have struggled to develop specifications for converting the world telephone network to all-digital operation while preserving the network's largest inanimate asset. That asset—an installed base of copper wiring that girdles the planet—is worth an estimated $300 billion. CCITT (the International Consultative Committee for Telegraphy and Telephony) published the initial ISDN standards in 1984; Committee T1 of the US-based Exchange Carriers Standards Association added some refinements (see **box,** "The ISDN interface standards"). Conversion to the Integrated Services Digital Network (ISDN) will reduce the global telecommunications network's overall operating costs while drastically improving its ability to carry voice and digital traffic.

Billions of dollars worth of electronic equipment, including modems and T1 multiplexers, is currently needed to cajole today's antiquated analog telephone systems into carrying digital information. This equipment will soon become obsolete. The additional services made available by ISDN will create a demand for new equipment that combines voice and digital communications functions. For these reasons, many semiconductor vendors view ISDN telecommunications as the next big market for electronic products.



A T1 digital-carrier line replaces several *individual subscriber lines. An ISDN T1 link carries twenty-three 64k-bps B channels and one 64k-bps D channel in each direction. (Photo courtesy Dallas Semiconductor)*

Phone companies won't await customer demand

Surprisingly, customer demand isn't the major reason why the phone companies intend to convert to ISDN. The major reason is the high cost of operating the world's communications network. The companies that stand to benefit from the implementation of ISDN include not only the regional Bell operating companies (RBOCs), which operate a substantial part of the US telephone network, but also the non-RBOC network operators such as GTE and the long-distance network operators such as US Sprint. Because they provide a wide variety of special services, these companies spend a lot of money to plan, install, and maintain the existing telecommunications system.

A Bell Communications Research (Bellcore, Livingston, NJ) survey conducted a few years ago showed that RBOCs offered 150 different special communications

Text continued on pg 122

One plug provides unified voice and data access *to the global telecommunications network through ISDN (left). Because ISDN puts voice and high-speed-data access on one network, it will make current telecomm equipment obsolete and open vast markets for new products. (Concept and photography by Paul Ambrose Studios; photo courtesy Advanced Micro Devices)*

The ISDN interface standards

The CCITT published its initial recommendations for ISDN basic-access services in 1984 in the *Red Book* of I Series recommendations. CCITT's reference model for ISDN basic access appears in **Fig A**. Basic access (also called the "S0 reference point" in the CCITT recommendations) operates bidirectionally at 192k bps. That rate includes two 64k-bps channels that can carry either voice or data (these channels are called "bearer" channels B1 and B2); a 16k-bps data channel (the D channel) used for network signaling and control (or call establishment and dialing), telemetry, or user packet data; and 48k bps of channel overhead for framing and error detection. Voice transmissions can use either of the B channels; the CPE negotiates B-channel usage with the switch each time it initiates a call.

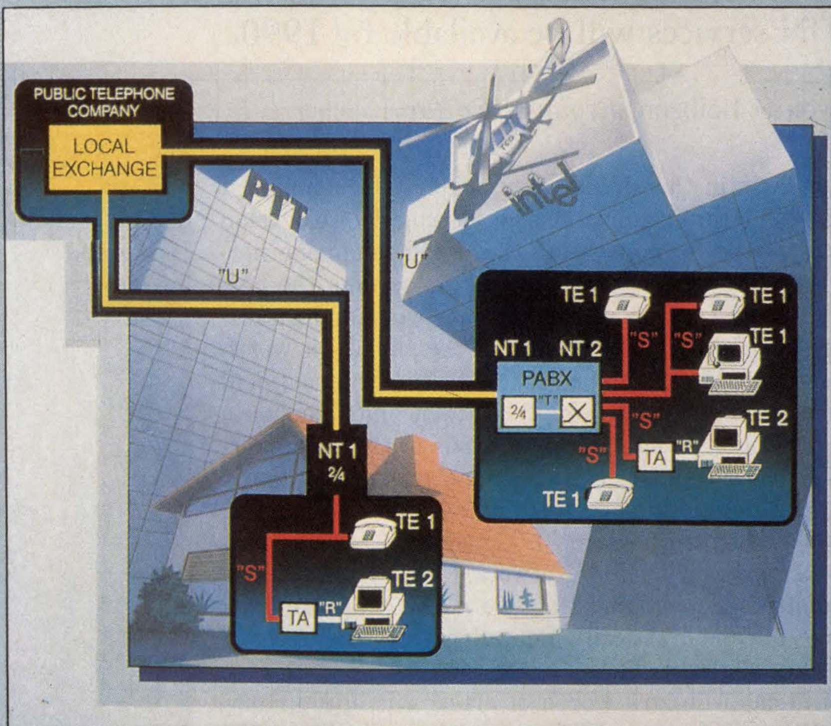


***Fig A—CCITT's reference model for ISDN subscriber lines** includes the undefined U interface (in yellow), which links the CO switch with the network terminator (NT) on the customer's premises, and the S interface (in red), which links an NT with the ISDN terminal equipment (TE). (Photo courtesy Intel Corp)*

"U" meant "undefined"

The ISDN standard defines four reference points: the R, S, T, and U interfaces. Starting at the CO switch, the U-interface link transports the B and D channels from the CO to the customer's premises. The U interface uses only one twisted-wire pair to link the CO with the NT1 box; this metallic link already exits between COs and customers. This transport was originally called the U interface in CCITT documents because it was undefined so that it could accommodate the different needs of various countries.

The national governments of the European countries own and operate the telephone systems, so the CCITT left the U-interface definition to them. In the post-divestiture US, however, network operators own the wires only as far as the network termination (the NT1 box in **Fig A**), making the need for a standard interface to the NT1 box more acute. Bellcore proposed a basic-access standard, the Digital Subscriber Line, for the US market at a Technology Requirements Industry Forum in St Louis on July 21, 1987; the organization has since published these requirements as Technical Advisory TA-TSY-000393.

An NT1 box such as the one depicted in **Fig A** terminates the U interface and transforms it into the 4-wire S or T interface. Electrically, the S and T interfaces are identical, but the protocols used over them vary slightly. The T interface exists only to link NT2 boxes (essentially ISDN PABXs) to the NT1 box. The S interface uses two twisted-wire pairs to carry access traffic. One pair carries signals from the NT1 box to the ISDN terminal equipment (TE1); the other pair carries signals back from the terminal equipment to the NT1.

A terminal adapter (TA) transforms S-interface traffic into the R format, which allows non-ISDN terminals (TE2) to

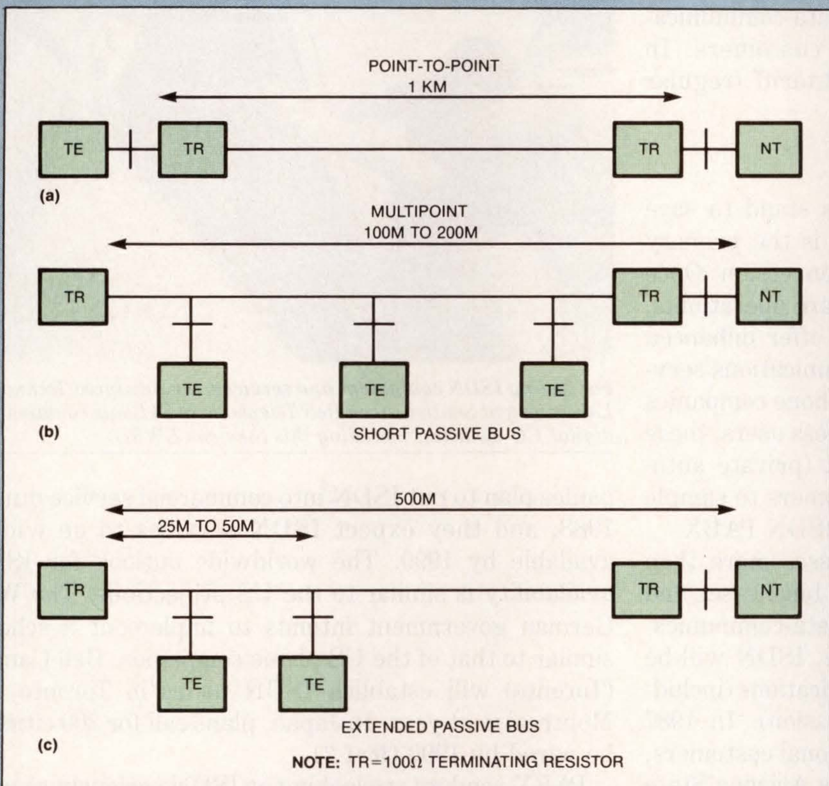


***Fig B—Wiring for an ISDN S interface (S bus)** can assume one of three topologies: a simple point-to-point configuration that's generally limited to 1 km **(a)**, a short passive bus that allows terminal equipment to be distributed evenly along the bus **(b)**, or an extended passive bus that clusters terminal equipment at one end and supports longer runs than the short-bus topology does **(c)**.*

connect to the digital network. The R format is nothing more than the good old RS-232C interface. CCITT recommendations I.460, I.461, I.462, and I.463 and ECMA (European Computer Manufacturers Association) recommendation 102 specify how non-ISDN-terminal data rates can be rate-adapted to an ISDN B channel. Bellcore has developed an adaptive rate-multiplexing scheme and offers a technology-transfer package for licensing, with and without patent rights.

S-interface topologies accommodate point-to-point and point-to-multipoint operation. CCITT's recommendation for the interface doesn't specify a maximum length for these configurations but does mandate a maximum signal loss of 6 dB or less, which usually limits practical cable lengths to those shown in **Fig B**. Note the two multipoint configurations: the short passive bus that allows TEs to be placed along the entire S bus, and the extended passive bus that allows longer cable runs but limits TE placement to a cluster at the end of the cable. Because of its multipoint capability, the ISDN's S interface is often called the S bus.

The S bus's multipoint topology doesn't allow you to use additional telephones on one S line as extension phones for a conversation. ISDN doesn't provide for extension phones because no standard exists for merging B-channel data from multiple sources. The bus architecture does allow additional equipment to make use of the second B channel while the conversation occurs, however, so it would permit two people to talk to each other while transferring data between their terminals.

ISDN defines only the first three layers of the ISO communications model. Layer 1, the physical layer, includes the definitions of the R, S, and T interfaces in CCITT recommendation I.430. ISDN defines the B channel as a clear data channel and provides only layer 1 services when transporting data over a B channel. The user's terminal equipment and software must supply the upper OSI layers as needed.

Recommendations I.440/Q.920 and I.441/Q.921 define ISDN's layer 2, the D-channel link-access procedure (dubbed LAPD), which is a functional superset of the LAPB (link-access procedure, balanced) used for X.25 communications. Layer 3, the network layer and the top of the ISDN model, defines call-setup and clear-down procedures; it resides in CCITT recommendations I.450/Q.930 and I.451/Q.931.

Billions of dollars worth of electronic equipment is currently needed to cajole today's analog telephone systems into carrying digital information.

services across the US (**Ref 1**). ISDN promises to reduce that number to one. ISDN will also reduce the cost of special services—particularly data-communications services—to phone companies' customers. In ISDN, most services will be standard-tariff (regular price) items.

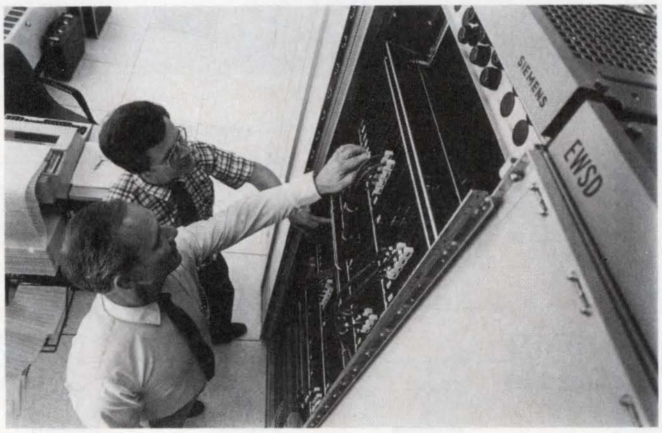
Businesses are the primary targets

The money the telephone companies stand to save from this reduction in special services is the primary economic incentive driving the ISDN conversion. Once the ISDN central office (CO) switches are operational, the telephone companies will start to offer enhanced data services in addition to voice-communications services. ISDN CO switches will allow the phone companies to offer Centrex ISDN services to business users; these services will simulate an ISDN PABX (private automatic branch exchange) and allow customers to sample ISDN services without purchasing an ISDN PABX.

The phone companies target businesses more than they do residential customers, because businesses and institutions are the primary users of data-communications services. In the immediate future, ISDN will be useful mainly for intracompany communications (including voice, data, and facsimile transmission). In 1987 several interested business and institutional customers, including Tenneco, Shell Oil, AT&T, the Arizona State Government, and McDonald's participated with telephone companies in conducting ISDN field trials. In addition, the US government is currently soliciting proposals for a project called the Federal Telecommunications System 2000 (FTS 2000), which will revamp the government's communications, relying heavily on ISDN services and equipment.

An ISDN lab for testing products

As an adjunct to the field trials, Southwestern Bell Telephone established an Advanced Technology Laboratory at its offices in St Louis, MO, to assist customers in selecting and testing ISDN services and equipment. The lab contains four digital CO switches: an AT&T 5ESS, a Northern Telecom (Concord, NH) DMS-100, an Ericsson (Stockholm, Sweden) AXE-10, and a Siemens EWSD. Manufacturers of ISDN customer premises equipment (CPE) can also schedule time in Southwestern Bell's Advanced Technology lab to test their products' compatibility with the various CO switches. The lab has controlled-access areas to protect customer and vendor secrecy.



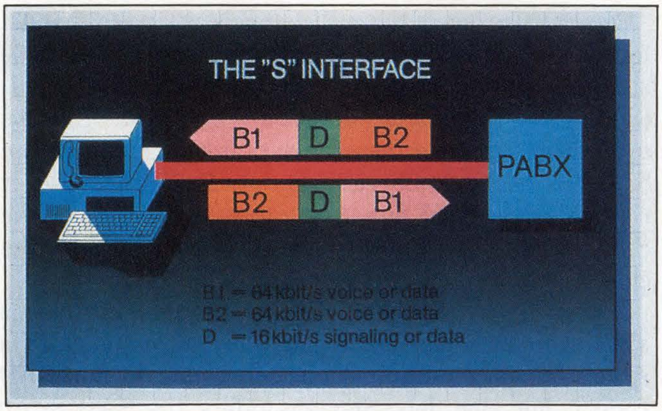
For testing ISDN equipment and services, *the Advanced Technology Laboratory at Southwestern Bell Telephone in St Louis contains four digital CO switches, including this Siemens EWSD.*

After the field-trial experiences, the telephone companies plan to put ISDN into commercial service during 1988, and they expect ISDN services to be widely available by 1990. The worldwide outlook for ISDN availability is similar to the US projections. The West German government intends to implement a scheme similar to that of the US phone companies. Bell Canada (Toronto) will establish ISDN nodes in Toronto and Montreal next year. In Japan, plans call for 200 cities to be wired by 1990 (**Ref 2**).

PABX vendors are looking at ISDN seriously as well. PABXs must eventually connect to the public networks, which will shortly offer ISDN access protocols. In addition, ISDN promises to afford PABX vendors the chance to make more of an impact on the data-communications market. Though PABX manufacturers have offered voice/data systems in the past, vendors used proprietary transmission methods, so any one customer was generally limited to terminal equipment from the same PABX vendor. These days, however, users have a lot of sophistication, garnered from the experience of purchasing PCs: They now expect and demand a mix-and-match marketplace for equipment of all kinds, including telecommunications products. ISDN's standard interfaces will make such interchangeability practical.

Primary rate means wide bandwidth

ISDN's basic-access rate provides for 64k bps of voice and 64k bps of data transport in both directions. Because of that limited bandwidth, PABXs aren't likely to use just the basic-access rate for transport to CO switches. PABX designers plan to use the higher-speed, primary-access rate as well. ISDN's primary-



***The ISDN S interface carries data at a 144k-bps rate** in both directions simultaneously; the rate is allocated to two 64k-bps B channels (B1 and B2) and a 16k-bps D channel in each direction. (Photo courtesy Intel Corp)*

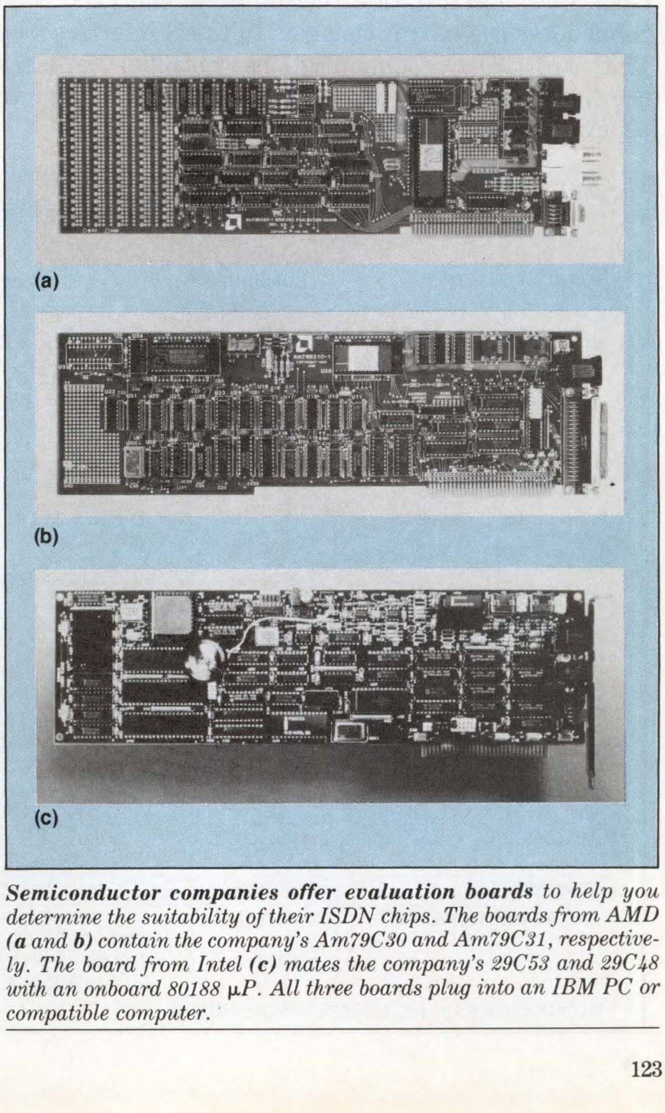
access rate employs a technology already in common use: the digital carrier. In Europe, the primary-rate digital carrier operates at 2.048M bps and is called CEPT (Conference of European Post Telecommunications); in North America, the primary-rate digital carrier operates at 1.544M bps and is called T1. In CCITT's ISDN terminology, these primary rates are called the S1 and S2 reference points, respectively.

A T1 carrier supplies bidirectional 23B+D service: twenty-three 64k-bps B channels and one 64k-bps D channel. CEPT accommodates thirty 64k-bps B channels and two 64k-bps D channels in each direction (30B+2D). Note that the primary-rate D channel has a wider bandwidth than the basic-access D channel does. PABX manufacturers already apply the T1 carrier for digital communications, in the digital multiplexed interface (DMI) format, to several brands of mainframes and minicomputers. Because they already have the T1 technology, PABX manufacturers will find it relatively easy to overlay ISDN on the existing T1 transport mechanism.

Although many business users will appreciate the jump from the meager 1200- or 2400-bps data rate permitted by today's phone system to ISDN's 64k-bps rate, some forward-thinking network planners already foresee the time when certain data-communications applications, such as CAD and CAE graphics, will need the entire primary-rate bandwidth. This so-called hyperchannel use of the T1 and the CEPT digital carriers will support 1.536M- and 1.920M-bps data rates, respectively. One manufacturer already offers a protocol controller that can operate at hyperchannel rates: Motorola's MC68606 multilink, LAPD (D-channel link-access procedure) protocol controller, which has a built-in DMA controller.

The current ISDN products from semiconductor vendors include ICs for primary-rate applications and for ISDN's S interface. Because CCITT did not define a U-interface standard and because Bellcore was still soliciting industry comments on its proposal for this basic-access transport as recently as September 30 of this year, chip manufacturers guess that U-interface chips for the US market won't appear until the second half of 1988.

Table 1 lists some of the available primary-rate devices, including line drivers and receivers, encoder/decoders, and protocol controllers. Although many of these products were designed for non-ISDN, digital-carrier applications, they work equally well in ISDN designs.



(a)

(b)

(c)

***Semiconductor companies offer evaluation boards** to help you determine the suitability of their ISDN chips. The boards from AMD **(a and b)** contain the company's Am79C30 and Am79C31, respectively. The board from Intel **(c)** mates the company's 29C53 and 29C48 with an onboard 80188 μP. All three boards plug into an IBM PC or compatible computer.*

Network providers currently offer 150 different special services; ISDN promises to reduce that number to one.

You can find many more chips for ISDN's S interface than for the U interface, for two major reasons. First, until this year, the S interface was the only ISDN physical-layer standard that companies could develop products for; it was the only one defined adequately. Second, most of the high-volume CPE (such as telephones, workstations, printers, and facsimile machines) will attach to the S bus. **Table 2** lists several representative S-interface ICs.

Although no ISDN CPE designs have yet reached the market in volume, some semiconductor companies have already introduced second-generation ISDN chips. For example, Siemens first introduced its 2-chip PEB 2070/2080 set for S-interface applications. The two devices interconnect by means of Siemens' proprietary IOM (ISDN-Oriented Modular) serial data bus, which operates at 512 kHz and has two unidirectional data lines, a clock line, and a data-direction line. The PEB 2080 S-bus interface circuit connects to the S interface; the PEB 2070 ISDN communications controller performs the LAPD processing and splits the two B channels into separate data streams.

You can use one of these B channels as a voice channel by connecting a codec, such as the company's PEB 2060 signal-processing codec filter, to the PEB 2070's SLD (Subscriber-Line Datalink) port. The serial SLD bus uses three wires to transfer data between chips. The SLD bus has one bidirectional data line; otherwise, it resembles the IOM bus. You can assign either of the S-interface's B channels to the SLD port through the chip's serial-port control register.

For B-channel data applications, the PEB 2070 has a synchronous serial port that you can connect to a synchronous communications controller (or non-SLD codec). For that job, Siemens offers the SAB 82520 high-level serial communications controller. You must use a synchronous chip, not an asynchronous serial controller, to couple to the PEB 2070's serial ports. The serial communications controller provides a FIFO buffer, which allows the μP a reasonable data-transfer latency between the S interface and upper ISO protocol layers for user-data transport over ISDN networks.

The PEB 2070 will also transfer B-channel data to and from the S interface through its μP interface

TABLE 1—REPRESENTATIVE PRIMARY-RATE ICs

MANUFACTURER	PART NUMBER	PART NAME	FUNCTION	PRIMARY-RATE INTERFACE	PRICE*
AT&T	L1046	PCM TRANSCEIVER	ENCODER/DECODER, LINE INTERFACE	T1	$26 (1000)
DALLAS SEMICONDUCTOR	DS2175	T1/CEPT ELASTIC STORE	TRANSMIT BUFFER	T1/CEPT	$10
	DS2176	T1 RECEIVE BUFFER	RECEIVE BUFFER	T1/CEPT	$10
	DS2180	T1 TRANSCEIVER	ENCODER/DECODER	T1	$23
	DS2181	CEPT TRANSCEIVER	ENCODER/DECODER	CEPT	$23
	DS2186	RECEIVE LINE INTERFACE	LINE RECEIVER	T1/CEPT	$8
	DS2187	TRANSMIT LINE INTERFACE	LINE DRIVER	T1/CEPT	$8
EXAR	XR-T5650	PCM LINE RECEIVER	LINE RECEIVER, CLOCK RECOVERY	T1/CEPT	$5.83
	XR-T5683	PCM LINE INTERFACE	TRANSMITTER/RECEIVER, CLOCK RECOVERY	T1/CEPT	$5.21
	XR-T5670	B8ZS/AMI TRANSCODER	ENCODER/DECODER	T1	$4.43
	XR-T5675	DUAL LINE DRIVER	LINE DRIVER	T1/CEPT	$1.60
GOULD	S8975	DS1/T1 TRUNK INTERFACE	TRANSMITTER/RECEIVER	T1	$17.10
MITEL	MH89760	T1/DS1 TRUNK INTERFACE	TRANSMITTER/RECEIVER, CLOCK RECOVERY	T1	$55
	MH89790	CEPT TRUNK INTERFACE	TRANSMITTER/RECEIVER, CLOCK RECOVERY	CEPT	$68
	MT8976	T1/ESF TRUNK INTERFACE	TRANSMITTER/RECEIVER	T1	$25.56
	MT8979	CEPT TRUNK INTERFACE	TRANSMITTER/RECEIVER	CEPT	$35
MOTOROLA	MC68606	MULTI-LINK LAPD CONTROLLER	HDLC CONTROLLER	T1/CEPT	$100 (SAMPLE)
ROCKWELL	R8070	T1/CEPT PCM TRANSCEIVER	TRANSMITTER/RECEIVER	T1/CEPT	$22
TEXAS INSTRUMENTS	TCM2202/2222	AMI/HDB3 ENCODER/DECODER	ENCODER/DECODER	T1/CEPT	$11.60
	TCM2203	EQUIPMENT LINE INTERFACE	LINE DRIVER/RECEIVER CLOCK RECOVERY	T1/CEPT	$11.60

*IN QUANTITIES OF 100, EXCEPT WHERE NOTED

TABLE 2—REPRESENTATIVE ISDN S-INTERFACE ICs

MANUFACTURER	PART NUMBER	PART NAME	FUNCTION	PRICE
ADVANCED MICRO DEVICES	AM79C30A	DIGITAL SUBSCRIBER CONTROLLER	S-INTERFACE, D-CHANNEL PROCESSOR, CODEC, FILTER, DTMF DIALER, RINGER	$33.25 (100)
	AM79C31A	DIGITAL EXCHANGE CONTROLLER	S INTERFACE TO PCM HIGHWAY CONVERTER	$20 (100)
	AM79C312A	DIGITAL EXCHANGE CONTROLLER	79C31A WITHOUT DATA-LINK CONTROLLER	$18 (100)
	AM79C32	ISDN DATA CONTROLLER	DATA-ONLY VERSION OF 79C30	$20 (100)
	AM79C401	INTEGRATED DATA PROTOCOL CONTROLLER	LAPB/LAPD LOGICAL-LINK CONTROL	<$30 (100)
AT&T	T7250	UNITE	S-INTERFACE, D-CHANNEL PROCESSOR	$16 (1000)
INTEL	29C48	VOICE CONVERSION CHIP	CODEC, FILTER	$6 (10,000)
	2952	LINE CARD CONTROLLER	CONTROLS EIGHT 29C53s	$9.50 (10,000)
	29C53	DIGITAL LOOP CONTROLLER	S-INTERFACE, D-CHANNEL PROCESSOR	$12.70 (10,000)
	83C152	UNIVERSAL COMMUNICATIONS CONTROLLER	μC WITH HDLC CONTROLLER	$25 (10,000)
MITEL	MT8994	DIGITAL TELEPHONE CHIP	μ-LAW CODEC, FILTER, DTMF DIALER, RINGER	$17.15 (1000)
	MT8995	DIGITAL TELEPHONE CHIP	A-LAW CODEC, FILTER, DTMF DIALER, RINGER	$17.15 (1000)
	MT8930	SUBSCRIBER NETWORK INTERFACE	S-INTERFACE, D-CHANNEL PROCESSOR	$16 (1000)
	MT8952B	HDLC PROTOCOL CONTROLLER	HDLC CONTROLLER	$8 (1000)
MOTOROLA	MC145474	S/T INTERFACE TRANSCEIVER	S INTERFACE	$12 (10,000)
	MC145488	DUAL DATA-LINK CONTROLLER	DUAL HDLC CONTROLLER	$16 (10,000)
	MC145503	FILTERED CODEC	CODEC, FILTER	$4.50 (10,000)
SIEMENS	PEB 2060	SIGNAL PROCESSING CODEC FILTER	CODEC, FILTER	$12.80 (1000)
	PEB 2070	ISDN COMMUNICATIONS CONTROLLER	D-CHANNEL CONTROLLER	$13.60 (1000)
	PEB 2080	S-BUS INTERFACE CIRCUIT	S INTERFACE	$13.60 (1000)
	PEB 2085	ISDN SUBSCRIBER ACCESS CONTROLLER	COMBINES PEB 2070 AND PEB 2080	$24 (1000)
	SAB 82520	SERIAL COMMUNICATIONS CONTROLLER	DUAL HDLC CONTROLLER	$17.60 (1000)

without requiring the help of a communications controller. However, because the PEB 2070 provides no FIFO buffering for B-channel data, the μP will have to operate in a tight loop to catch the data as it flies by. Siemens combines the functions of the PEB 2070 and PEB 2080 in its second-generation device, the PEB 2085 ISDN subscriber-access controller.

Intel uses the SLD bus to interconnect its 29C53 digital loop controller with its 29C48 voice-conversion chip. The 29C53 incorporates the S interface and the D-channel processor, and it can be operated through either its μP or SLD ports. The 29C53 operates at either the NT or TE end of the S interface. The ability to control the device through the SLD port is especially useful for PABX line-card applications, because it minimizes the required amount of interconnection on the line card. Intel's 2952 line-card controller operates eight 29C53s but still fits in a 40-pin package: It uses eight of the pin-efficient SLD ports to control the digital loop controllers.

For B-channel data applications, you can use any USART, linking it to the 29C53's SLD port with some glue logic. However, Intel offers a more integrated solution: the 83C152 universal communications controller. Based on an 80C51 μC core, the 83C152 also contains a 2-channel DMA controller; two counter/timers; an 8k-byte ROM; 256 bytes of RAM; and the "global serial channel," a 2-channel, multiprotocol, serial communications controller.

The 83C152's communications controller handles both HDLC, which is an appropriate protocol for ISDN applications, and CSMA/CD (carrier-sense, multiple access with collision detection), which is the protocol employed by Ethernet LANs. Such a design can use the core 80C51's asynchronous serial port to provide an R interface for an external data terminal.

Mitel employs a proprietary, 2.048M-bps, 4-wire ST serial bus to connect devices to its MT8930 subscriber-network interface circuit. The MT8930 contains an S interface plus the D-channel controller. When combined with an MT8930, the company's MT8994/8995 digital telephone ICs incorporate the codec, filter, speakerphone circuits, DTMF generator, and tone ringer you need to build a complete ISDN telephone.

The MT8994's codec employs a μ-law encoder for North American applications; the MT8995's codec has an A-law encoder for European use. The devices are pin compatible, so you can use one pc board for products sold on both sides of the Atlantic ocean. Mitel's MT8952B adds HDLC formatting for B-channel data applications and connects directly to the ST bus.

The Am79C30 digital subscriber controller IC from Advanced Micro Devices (AMD) has no serial bus to connect to other devices in the family, because it contains all the basic functions necessary to build an integrated ISDN voice/data workstation. A digital signal processor on the chip implements the codec, filter, DTMF tone generator, and tone ringer. The device provides D-channel processing and supplies the B data channel through a serial port for protocol processing.

ISDN will also reduce the cost of special services—particularly data-communications services—to RBOC customers.

Makers of competing multichip products claim that ISDN is still in its infancy and that it's too soon to offer a cost-effective, single-chip, S-interface controller. Ron Ruebusch, director of marketing for AMD's Communications Products Div, strongly disagrees. Ruebusch points out that AMD chose DSP for implementing analog functions on the Am79C30 because that choice allows designers to use AMD's standard, 1.6-μm, CS11 digital-IC process. Traditional codec-IC design, he says, uses switched-capacitor filters built with analog-IC processes. Existing codecs also require ±5V power supplies, however, so they're poor candidates for incorporation in an all-digital ISDN controller chip. Most digital-IC processes won't accommodate 10V analog circuitry and digital circuitry on the same device.

Modularity vs integration

Another charge that competing vendors level at AMD's 1-chip approach is that it lacks modularity—even if you don't need all the chip's features, you still have to pay for them. Ruebusch admits that the DSP section of the Am79C30 is expensive, consuming about 30% of the die. However, AMD also offers the Am79C32 ISDN data controller, which incorporates all of the Am79C30's features except the DSP features. The chip is useful for data-only applications such as ISDN printers or facsimile machines, and it costs approximately 30% less than the Am79C30. In addition, the company has planned another two generations of refinements to its standard process; the refinements will allow for smaller device geometries. Because the Am79C30 uses this standard process, Ruebusch expects that the company will ultimately shrink the Am79C30's die to 40% of its current size, reducing the device's cost as ISDN usage grows.

Further, in the short term, it's not the chip cost but the development cost that is customers' greatest concern, Ruebusch says. His customers estimate that

Manufacturers of ISDN ICs

For more information on ISDN ICs, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Advanced Micro Devices
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Sunnyvale, CA 94088
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TLX 346306
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(800) 372-2447
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Exar Corp
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Gould Inc
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Intel Corp
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Centre Électronique
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44075 Nantes Cedex, France
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Kanata, Ontario K2K 1X5
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Zentralstelle für Information
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8000 Munich 1, West Germany
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TLX 5210025
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Siemens Components Inc
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Iselin, NJ 08803
(201) 321-4842
Circle No 715

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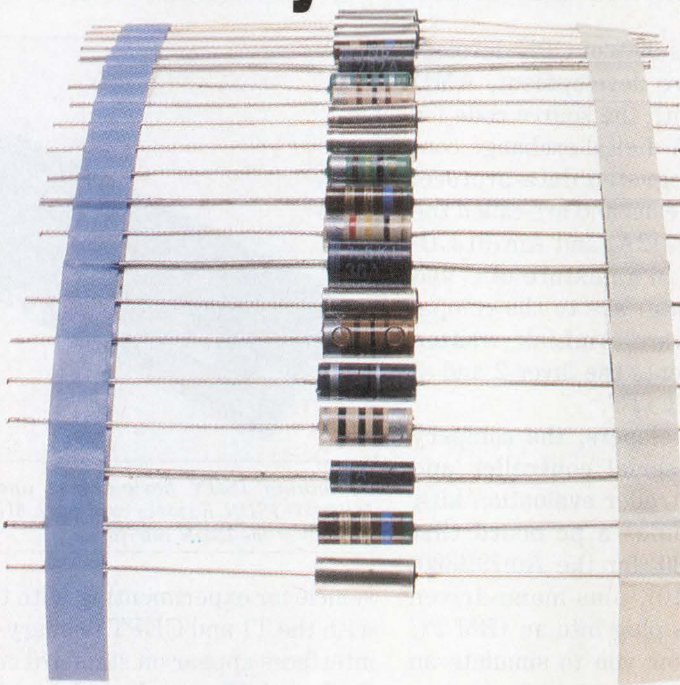

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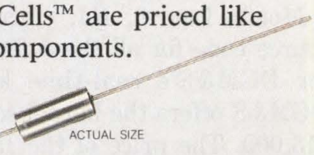

For more information, call us at 301-296-7000.

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The telephone companies plan to put ISDN into commercial service during 1988 and expect ISDN services to be widely available by 1990.

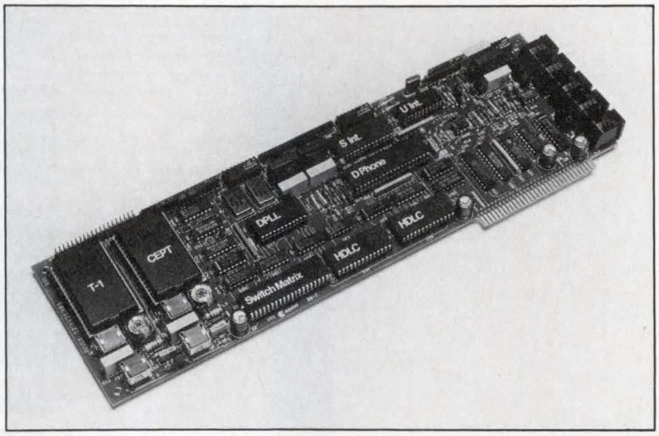
software development represents 90% of CPE development cost. As an aid to software development, AMD offers low-level device drivers with the source code for the Am79C30/32, the Am79C31A digital exchange controller, and the Am79C401 integrated data-protocol controller. The drivers cost $125 each and are called the Am79LLD30/32, Am79LLD31A/312A, and Am79LLD-401. AMD's drivers are written in a mixture of C and 8088 assembly code, and they interface to the company's $850 AmLink protocol software. AmLink, written entirely in Microsoft C, implements the layer-2 and -3 LAPD recommendations from CCITT.

As a further aid to CPE developers, the company offers the Am79B300 digital serial controller and Am79B310 digital exchange controller evaluation kits. Each kit costs $1250 and includes a pc board that incorporates either the Am79C30 (for the Am79B300) or Am79C31 (for the Am79B310), plus menu-driven evaluation software. The boards plug into an IBM PC or compatible computer and allow you to simulate an ISDN line card and workstation by using one or two PCs.

Intel also offers software support for its ISDN components. The ISP188 software package implements layers 2 and 3 of the ISDN protocol and includes layer-1 drivers for the company's 29C53 digital loop controller, 29C48 voice-conversion chip, and 82530 serial communications controller. AT&T has tested the ISP188's call-establishment protocol and found it to be compatible with the 5ESS switch. At this early stage of ISDN development, the switch manufacturers have yet to create a unified protocol for call establishment; each vendor's CO switch currently requires a different protocol.

The software included in the $20,000 ISP188 package was written by DGM&S Communications Technology, a Mount Laurel, NJ, consulting firm. Intel includes source code for all the software in the package except for DGM&S's real-time kernel for the 80188 μP. DGM&S offers the kernel source code for an additional $15,000. The price of the ISP188 also includes two pc boards that plug into an IBM PC or compatible computer (each board contains a 29C48, a 29C53, and an 80188 μP), diagnostic software, two days of training, and unlimited incorporation rights for the object code.

Mitel's $1500 MB89000 ISDN Express card places 12 of the company's ISDN components on one PC-compatible board. The menu-driven software supplied with the card gives you access to the data, control, and status registers on each IC. The Express card provides a vehicle for experimenting with the S interface as well as with the T1 and CEPT primary-rate interfaces. All line interfaces appear on standard connectors at the back of the board. The product also includes two of the company's MT8952 HDLC protocol controllers and a digital crosspoint switch.



Combining ISDN basic-access and primary-rate chips, *the MB89000 ISDN Express card from Mitel allows you to experiment with all of the ISDN interfaces.*

Products like the Mitel Express card and the other development boards from Intel and AMD can help you familiarize yourself with ISDN concepts. Because phone companies are rapidly implementing ISDN facilities in the global telecomm network, it's a good idea to look now at how ISDN will fit into your general product line. The availability of ISDN chips will make it easier for you to integrate ISDN interfaces in virtually all the computer equipment you're designing. Both the impending availability of ISDN services and the current availability of ISDN chips promise to make ISDN a commercial reality by the end of the decade. **EDN**

References

1. Carpenter, J B, "ISDN—The Promise," *ISDN User*, Volume 1, Number 1, June 1987.
2. Pandhi, Sushil N, "The universal data connection," *IEEE Spectrum*, July 1987.

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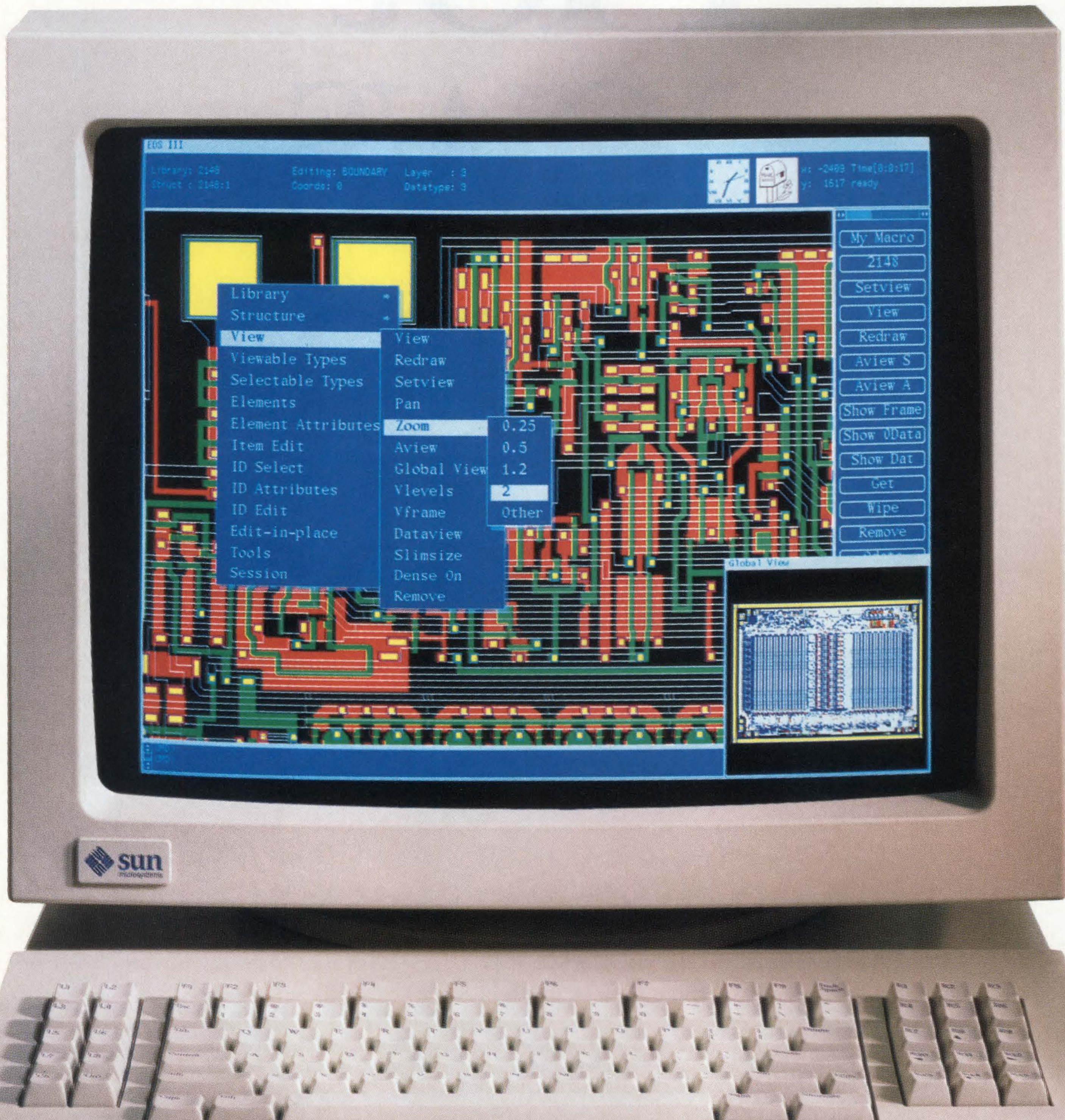

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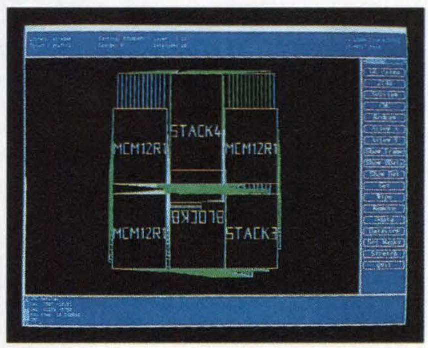

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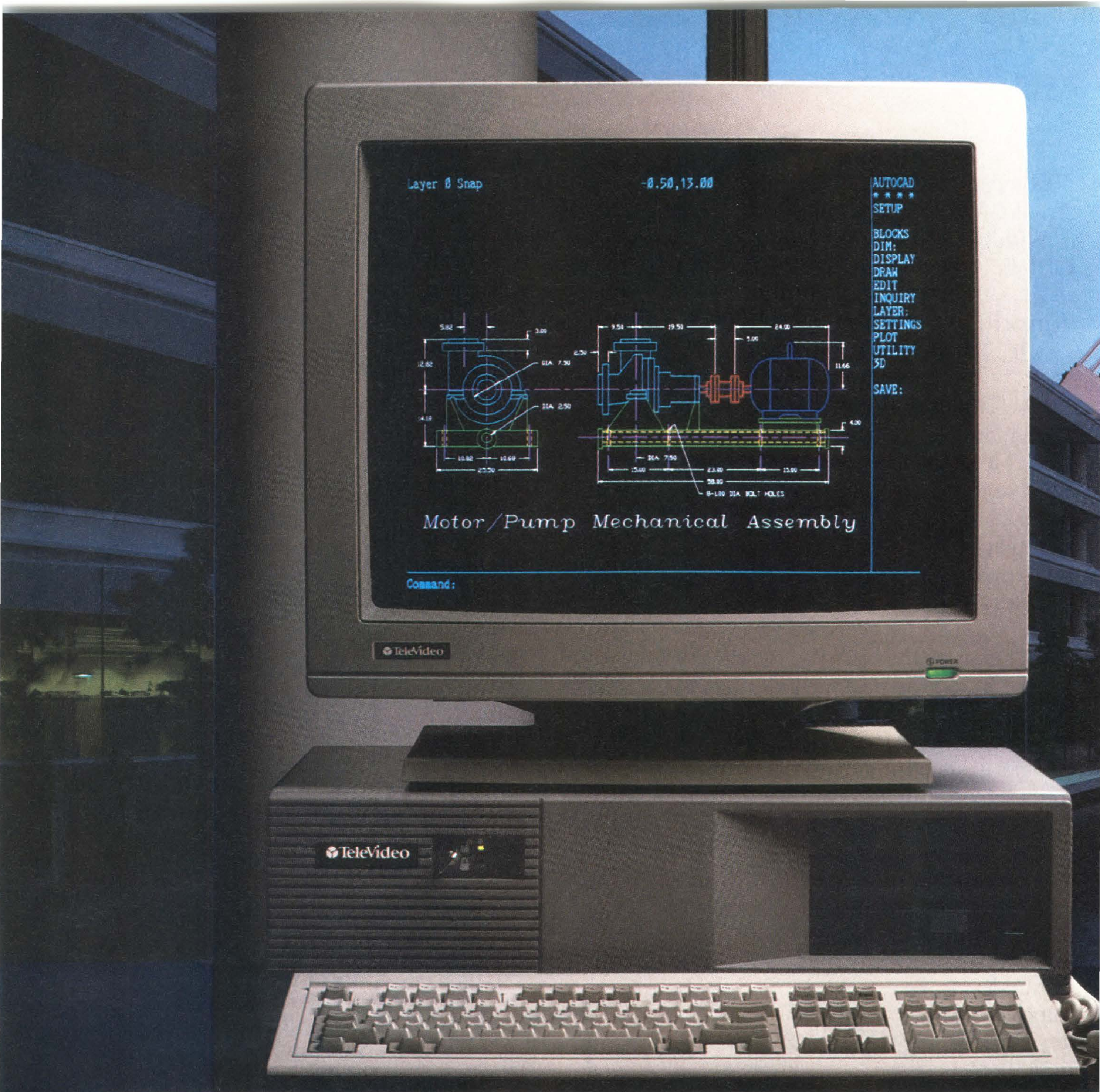

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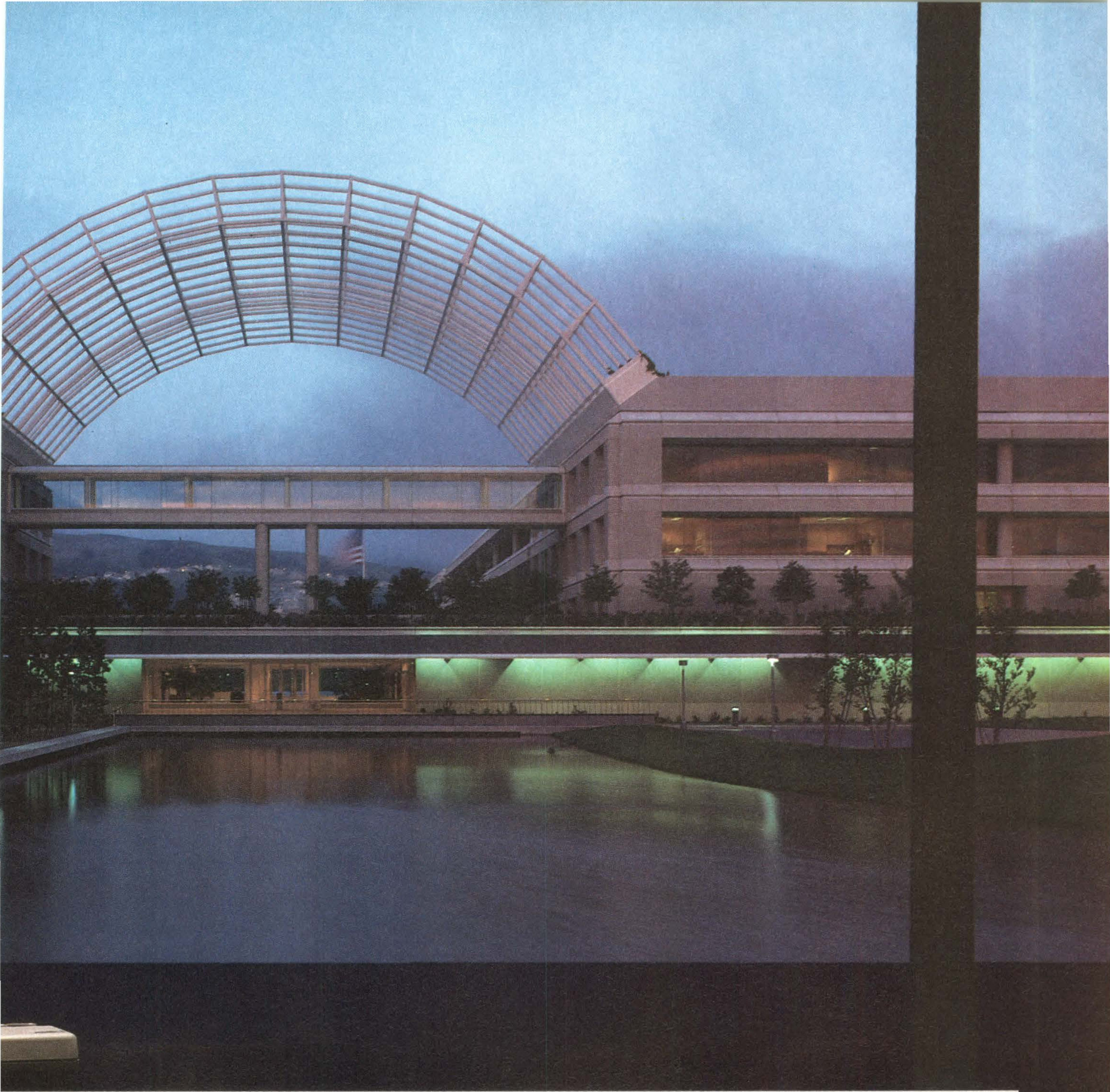

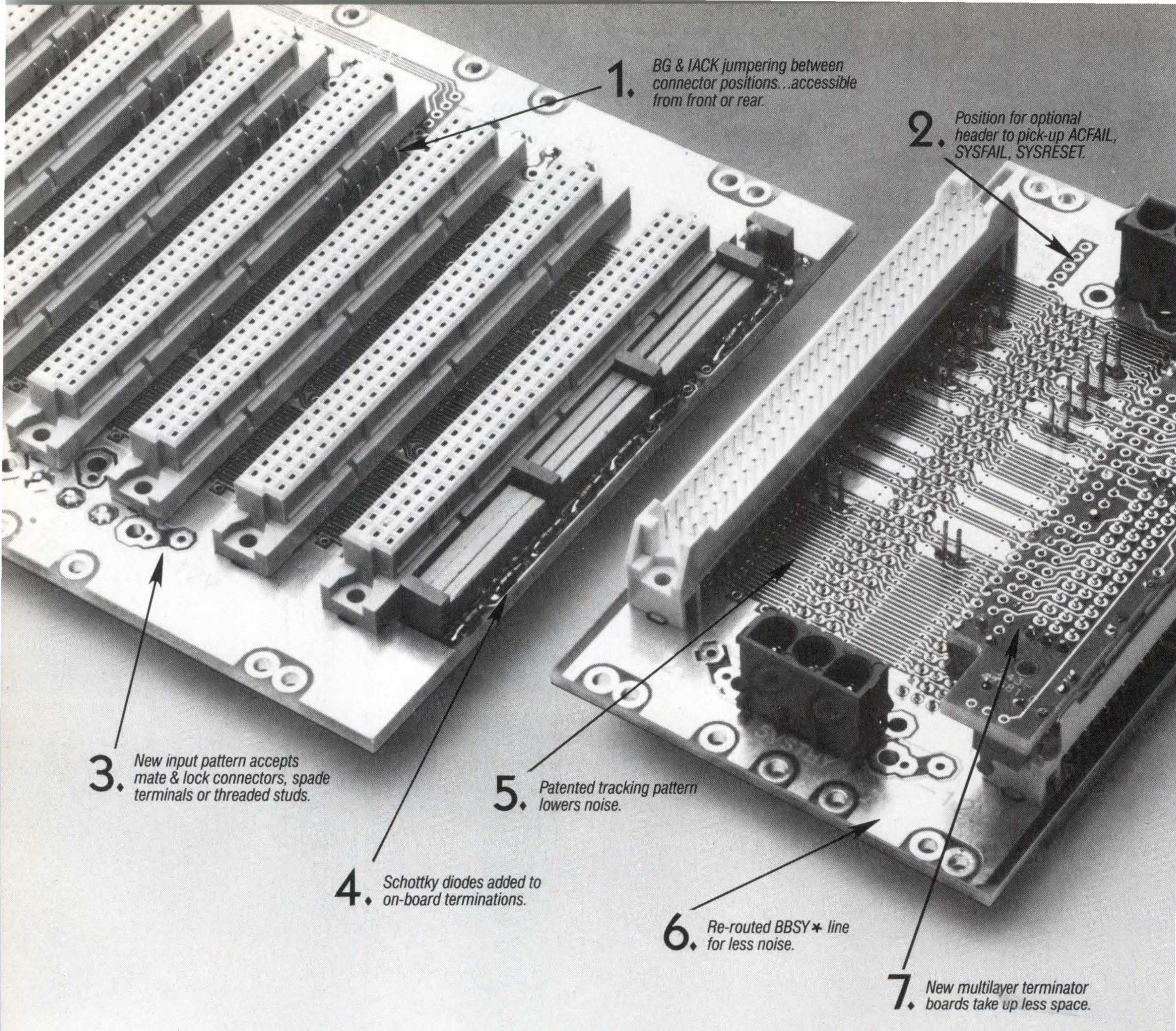

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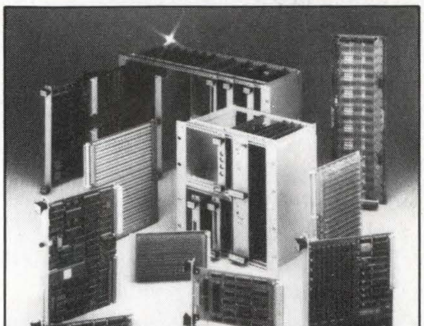

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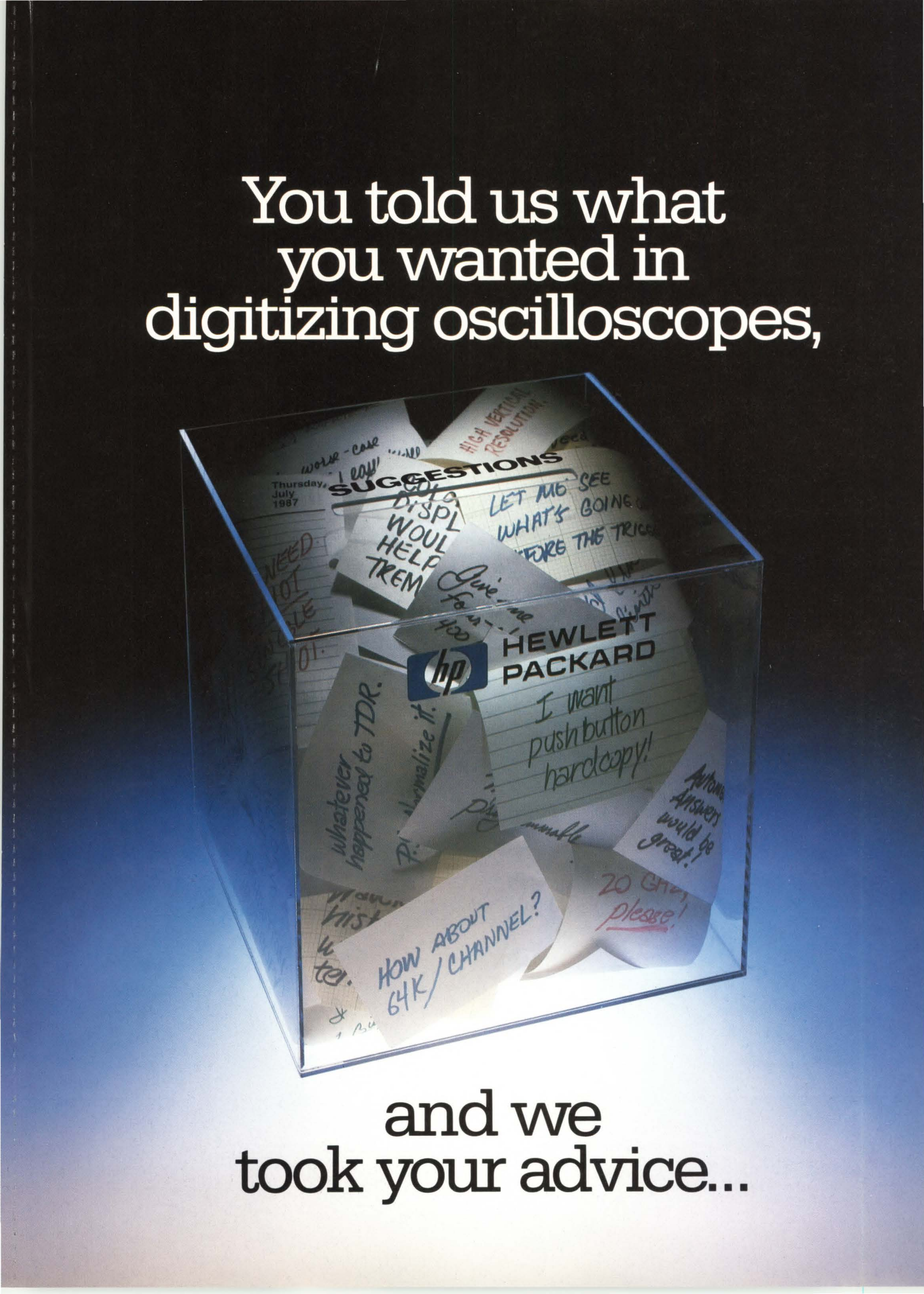

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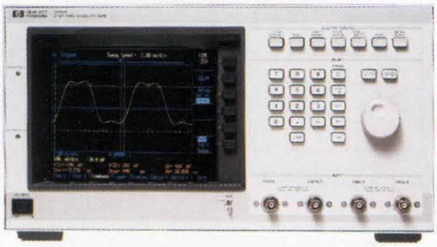

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S.S. bandwidth	250 MHz
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Resolution	8 bit to 25 MHz, 7 bit to 100 MHz, 6 bit to 250 MHz
Sensitivity	1 mV/div to 5 V/div
Coupling	ac, dc; 50 Ohm & 1 MOhm
HORIZONTAL:	
Digitizing rate (max)	1 GSa/sec
Resolution	10 psec
Pre-trigger viewing	YES
MEMORY:	
Acquisition/chan	8k
Waveform storage	2 pixel, 4 rep wfm, 4 ss wfm
Nonvolatile instrument setups	10

HP 54112D $22,900.00*

VERTICAL:	
Rep. bandwidth	100 MHz
S.S. bandwidth	100 MHz
Inputs	4 chan & 1 trig
Resolution	6 bit to 100 MHz
Sensitivity	5 mV/div to 5 V/div
Coupling	ac, dc; 50 Ohm & 1 MOhm
HORIZONTAL:	
Digitizing rate (max)	400 MSa/sec
Resolution	40 psec
Pre-trigger viewing	YES
MEMORY:	
Acquisition/chan	64k
Waveform storage	2 pixel, 4 rep wfm, 4 ss wfm
Nonvolatile instrument setups:	10

HP 54120T $27,850.00**

VERTICAL:	
Rep. bandwidth	20 GHz
S.S. bandwidth	NO
Risetime	17.5 psec
Accuracy	0.4%
Inputs	4 chan & 1 trig
Resolution	12 bits
Sensitivity	1 mV/div to 80 mV/div
Coupling	50 Ohm
HORIZONTAL:	
Accuracy	10 psec
Resolution	0.25 psec
Pre-trigger viewing	NO
Range	10 psec/div-1 s/div
MEMORY:	
Acquisition/chan	0.5k
Waveform storage	2 pixel (volatile), 4 rep wfm (nonvolatile)
Nonvolatile instrument setups:	10
TDR	
Pulse source	
Amplitude	0-200 mV
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Flatness	1%
Normalization	YES
Waveform histograms	YES

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Wescon/87

Wescon's 3-day professional program will provide you with practical technical information you can use immediately. Special exhibits and sessions on the business of electronics will help put it all in focus.

Dan Strassberg, *Associate Editor*

"Lights! Camera! Action!" Although the phrase sounds more appropriate to show biz than to electronics, it aptly describes the theme of this year's edition of the electronics industry's oldest trade show. Wescon/87, which will take place November 17 through 19 at San Francisco's Moscone Center, Civic Auditorium, and Brooks Hall, will turn the spotlight on electronics in entertainment and broadcasting.

Keynote address will spotlight the Olympics

The keynote address, by Charles A Steinberg, board chairman of Ampex Corp, will take you behind the scenes of the Olympic games that have been held since 1964. The address, at 12:00 noon on Tuesday in the Meridien Hotel ($25 admission), will illustrate electronics' role in putting television viewers in a front-row seat for the games. Following Mr Steinberg's talk, the Wescon Business Conference entitled "The State of the Entertainment Electronics Business" ($30, or $50 in combination with the keynote luncheon), will feature talks by Joseph Roizan, president of Tegal Consultants; William Jasper, president of Dolby Labs; R Bland McCartha, director of marketing for Ampex's AVS Div; and Russ Coughlin, TV editorial commentator.

Picking up on the electronics in entertainment theme will be a new feature at Wescon—the Electronics Theater. Located in the Civic Auditorium and open free of charge to all Wescon attendees, it will offer a combination of show-and-tell sessions, computer graphics from ACM/Siggraph, and video films. On each of the three show days at 9:00 AM, the Electronic Theater will present a session exploring applications of leading-edge technologies. On Tuesday, "Television and Special Event Communication—the Concept and How it Can Help You" will explain how multichannel party-line intercom systems not only coordinate entertainment events, but also play roles in aerospace and industry. Wednesday's session, "Computer Graphics Animation," will start with a historical perspective of the field and then discuss the state of the industry today and look at its future. Thursday's theme, "Digital Signal Processing for Television Broadcast," will inform you about the operations needed to generate and manipulate TV signals, as well as trends in videotape recording.

From 2:30 to 4:30 each afternoon, the Electronic Theater will present selections from the "1986 ACM/Siggraph Convention Video Review." Organized by Stephen Keith, ACM/Siggraph local-groups coordinator, the show will provide outstanding examples of computer graphics. During lunch, the Electronic Theater will show short subjects.

Special exhibit dazzles with sights, sounds

A special exhibit will feature the hardware that helps create the sights and sounds of today's electronics world. Among the products on display will be a 1-in. videotape recorder and the ADO (Ampex Digital Optics) special-effects device from Ampex Corp (Redwood City, CA). You will also be able to listen to the Emulator II computer-based digital music synthesizer from E-Mu Systems (Scotts Valley, CA). The exhibit will showcase video-digitizing equipment and a mobile broadcast van.

In addition to static displays, you will be able to see videotapes of avionics, engineering-design, and graphics-modeling systems from Robert Bosch Corp and Evans and Sutherland, both of Salt Lake City, UT. The free exhibit, to be located in the Civic Auditorium, will be open during regular show hours.

Conference turns toward business

Although Wescon won't officially open until Tuesday, a 2-part conference will take place Monday at the Meridien ($55 including luncheon, for morning or afternoon sessions; $80 for all day). The conference will

WESCON/87 TECHNICAL-SESSION PROGRAM

		BALLROOM F	BALLROOM G	BALLROOM H	MERIDIEN HOTEL (SAUTERNES BALLROOM I, II, III)
TUESDAY, NOVEMBER 17	9:00 AM TO 11:00 AM	(1) MICROCONTROLLERS MAKE THE 8- TO 16-BIT TRANSITION	(2) SOFTWARE VALIDATION AND VERIFICATION	(3) DEBUGGING AND INTEGRATION OF EMBEDDED SYSTEMS: CURRENT ISSUES	
	12:30 PM TO 2:30 PM	(4) THE 32-BIT RISC VS CISC CONTROVERSY	(5) NEW CAD TOOLS INTEGRATE PLDs, GATE ARRAYS, AND STANDARD CELLS	(6) MODERN METHODS IN DIGITAL SIGNAL PROCESSING	
	3:00 PM TO 5:00 PM	(7) NEW WAVE OF HIGH-PERFORMANCE VLSI PERIPHERAL CHIPS	(8) PC BASED CAD—COMPUTER-AIDED DESIGN OR COMPUTER-AIDED DISASTER? A USER'S PERSPECTIVE	(9) HIGH-VOLUME MICROWAVE APPLICATIONS	
WEDNESDAY, NOVEMBER 18	9:00 AM TO 11:00 AM	(10) PLDs. . . ARE THEY A DESIGN STEPPING STONE OR DO THEY OFFER LONG-TERM DESIGN AND MANUFACTURING SOLUTIONS?	(11) PHOTOVOLTAIC TECHNOLOGY AND SYSTEMS FOR THE 1990s	(12) ADVANCES IN BUS INTERFACE	(13) ELECTRONICS BUSINESS IN CANADA
	12:30 PM TO 2:30 PM	(14) QUICK-TURN ASICs; AN ELIXIR FOR SHORT PRODUCT LIFE CYCLES	(15) MICROPROCESSOR TECHNOLOGY AND APPLICATIONS FOR POWER SYSTEMS; DATA ACQUISITION AND CONTROL	(16) A FACTORY-FLOOR PERSPECTIVE OF COMPETITIVE BUS STRUCTURES	(17) NEW TECHNOLOGY—PROTECTING IT AND PROTECTING YOURSELF FROM IT
	3:00 PM TO 5:00 PM	(18) APPLICATION-SPECIFIC PLDs—A NEW THRUST	(19) PERSONAL-COMPUTER-BASED DATA ACQUISITION AND CONTROL	(20) SERVICES, ISSUES, AND TECHNOLOGY IN THE REALIZATION OF INTEGRATED SERVICES DIGITAL NETWORK (ISDN)	(21) BENEFITS OF ASIC DESIGN CENTERS
THURSDAY, NOVEMBER 19	9:00 AM TO 11:00 AM	(22) PROGRAMMING MICROCONTROLLERS —NEW SOFTWARE ENVIRONMENTS	(23) THERMAL CONSIDERATIONS IN SURFACE-MOUNT TECHNOLOGY	(24) SILICON SENSOR AND MICROSTRUCTURE TECHNOLOGY	
	12:30 PM TO 2:30 PM	(25) CMOS CORE PROCESSORS—THE KEY TO HIGH-PERFORMANCE ASIC	(26) POWER CONVERSION	(27) REAL-TIME MULTIPROCESSING TECHNOLOGIES	
	3:00 PM TO 5:00 PM	(28) HIGH INTEGRATION TECHNOLOGY FOR PERSONAL-COMPUTER DESIGN	(29) FLAT-PANEL TECHNOLOGY—"THE MEMBRANE ALTERNATIVE"	(30) LOW-POWER GaAs GATE ARRAYS—ALTERNATIVE TO HIGH-POWER ECL ARRAYS IN HIGH-SPEED SYSTEM DESIGN	

NOTE: ALL SESSIONS WILL BE HELD IN THE MOSCONE CONVENTION CENTER UNLESS OTHERWISE NOTED.

explore methods of doing business domestically and internationally. In the 8:30 AM to 12:00 noon session, speakers Richard Holton, a professor at the University of California at Berkeley; Zhang Zhidong, China Electronics Import/Export Commission; Lee Ting, Hewlett-Packard; Nancy Kuo, Finnigan Corp; and Robert Yahng, Baker and McKenzie will explore "Doing Business in the Pacific Rim." During the 12:00 noon to 2:00 PM luncheon, Joan M McEntee, deputy assistant secretary for trade development at the US Department of Commerce, will present an overview of the Reagan Administration's trade policies for the Pacific Rim. The 2:00 to 5:00 PM session, "Going to Market in the Domestic US," will feature talks by John Haskell, marketing consultant, and Marshall Cox of Western Microtechnology Inc.

On Wednesday at the Meridien, conferences ($20 each) related to the business rather than the technical side of electronics will continue. From 9:00 AM to 12:00 noon, you will be able to obtain "An Insider's View of J-I-T: a Purchasing Perspective" with Bruce Harvey and Michael Saenz of HP, Gordon Beattie of Northern Telecom, and Dennis Ryan of Unisys. Those who want to invest in electronics securities should attend "Investing in Electronics: Venture Capital and Public Stocks" from 2:00 to 5:00 PM, with Michael Murphy and Lissa Morganthaler of *California Technology Stock Letter*.

Interest in cryogenics, which not too long ago had dropped to near absolute zero, has heated up recently with the development of higher-temperature superconducting materials. You will get an informed look at the future of this technology on Thursday at the Meridien. There, a panel comprising Professor M Beasley, Stanford University; Professor T Van Duzer, UC Berkeley; Arnold Silve, TRW Space and Technology Group; and Dr Ferdinand Bedard, US Department of Defense will discuss "Superconductor Electronics and the New High Temperature Materials." This session is free to all registered attendees.

Technical program addresses nuts and bolts

If all the sessions on business, applications, and crystal-ball-gazing leave you hungry for new products and technology you can use, you should consider attending a 3-day technical program. It addresses the nuts and bolts of electronics, focusing on the impact of the evolving technologies on the way engineers do their jobs. Virtually all technical sessions will be held in the Moscone Convention Center, and you won't have to pay extra to attend them. Sessions run from 9:00 to 11:00 AM, 12:30 to 2:30 PM, and 3:00 to 5:00 PM.

On Tuesday, you'll be able to choose from three sessions each on high-performance VLSI, software-applications tools, and system solutions. On Wednesday, several sessions will focus on PLDs; three more will highlight power systems; and three others will cover data acquisition and control. You'll also be able to attend sessions on bus interfaces, metastability, and ISDN. On Thursday, Wescon attendees will find three sessions on new-generation single-chip µPs, as well as

Transportation and show details

As in most other large cities, parking in San Francisco is a hassle. Therefore, Wescon officials recommend that, if you must drive to the city, you park at Candlestick Park. It is close to the Bayshore Freeway—well away from downtown—at the Southeast corner of the city. Parking there costs $3, and shuttle buses will run frequently to and from Wescon. You *must* remove your car from Candlestick by 6:45 PM. If you take the BART (Bay Area Rapid Transit), the Civic Center stop is the most convenient to the Civic Auditorium and Brooks Hall. Powell Street is the stop for Moscone Center. If you travel by bus, take the 21 Hayes or 19 Polk for Brooks Hall and Civic Auditorium; take 15 Kearney or 30 Stockton for Moscone Center. The bus costs $0.75, and drivers will not make change for you.

Registration (for those who have not preregistered) costs $10 at the door. It admits you to both the exhibits and the professional program. As previously mentioned, your registration also admits you to the Electronic Theater and the special panel on superconductivity.

As you look through EDN's Wescon product section, you can map out a strategy for covering booths that interest you. To do this, it's helpful to know that booths numbered 3999 or lower are in the Moscone Center, 4000 through 4999 are in Brooks Hall, and 5000 through 5999 are in the Civic Auditorium.

sessions on SMT, flat-panel switches, silicon sensors, real-time programming, and GaAs devices.

Session 3 will cover debugging of integrated systems, and **Session 4** will shed light on the merits of 32-bit RISC and CISC architectures. Speakers at **Session 2** will address the problem of software verification. **Session 22** will cover programming single-chip μPs, and **Session 27** will guide you through the mine field of real-time programming for multiple CPUs. The title tells the story of **Session 8:** "PC-Based CAD—Computer-Aided Design or Computer-Aided Disaster? A User's Perspective."

Programmable logic devices will star in **Session 10,** which poses the question: "PLDs . . . Are They a Design Stepping Stone or Do They Offer Long-Term Design and Manufacturing Solutions?" **Session 18,** titled "Application-Specific PLDs—A New Thrust," will cover the impact of programmability in application-specific devices.

Cool SMT issue will surface

EDN readers who followed Steve Leibson's recent 5-part, hands-on SMT series may want to attend **Session 23**—"Thermal Considerations in Surface-Mount Technology." The session will address the double-edged problem of SMT boards, which take up less space, yet dissipate the same amount of power as their predecessors that use through-hole mounted components. The session will explain how to keep SMT boards cool, thus avoiding high failure rates.

The ubiquitous MS-DOS-based personal computer and the Apple Macintosh will star in another session. Because both machines offer a wealth of low-cost software tools and applications software, PC-based data acquisition and control has become more intriguing. But, until recently, designers have had to overcome significant problems with these systems to achieve adequate performance. **Session 19,** "Personal-Computer-Based Data Acquisition and Control," will highlight products for implementing low-cost control systems that take advantage of the economical computational capability of PCs. **EDN**

Products begin on pg 151

Article Interest Quotient (Circle One)
High 497 Medium 498 Low 499

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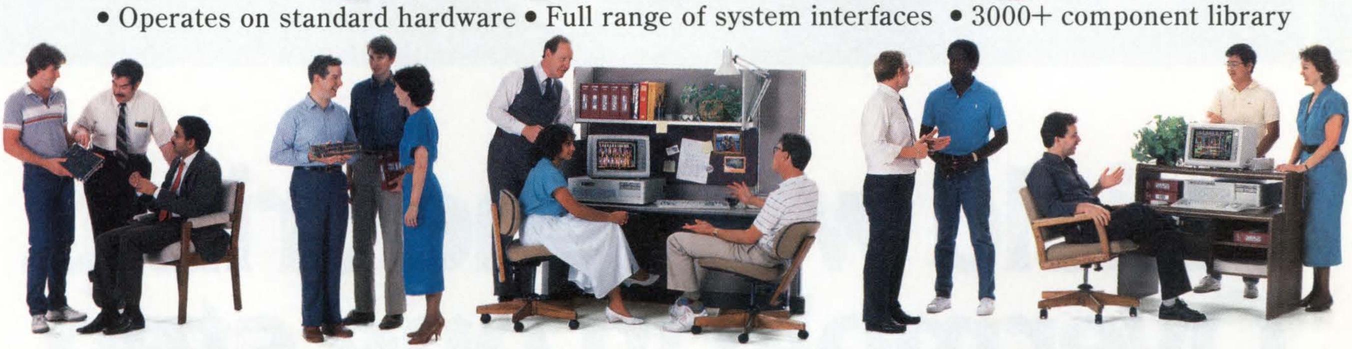

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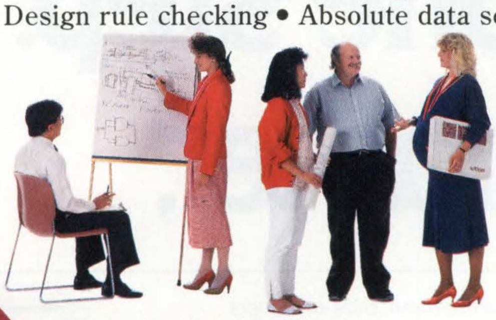

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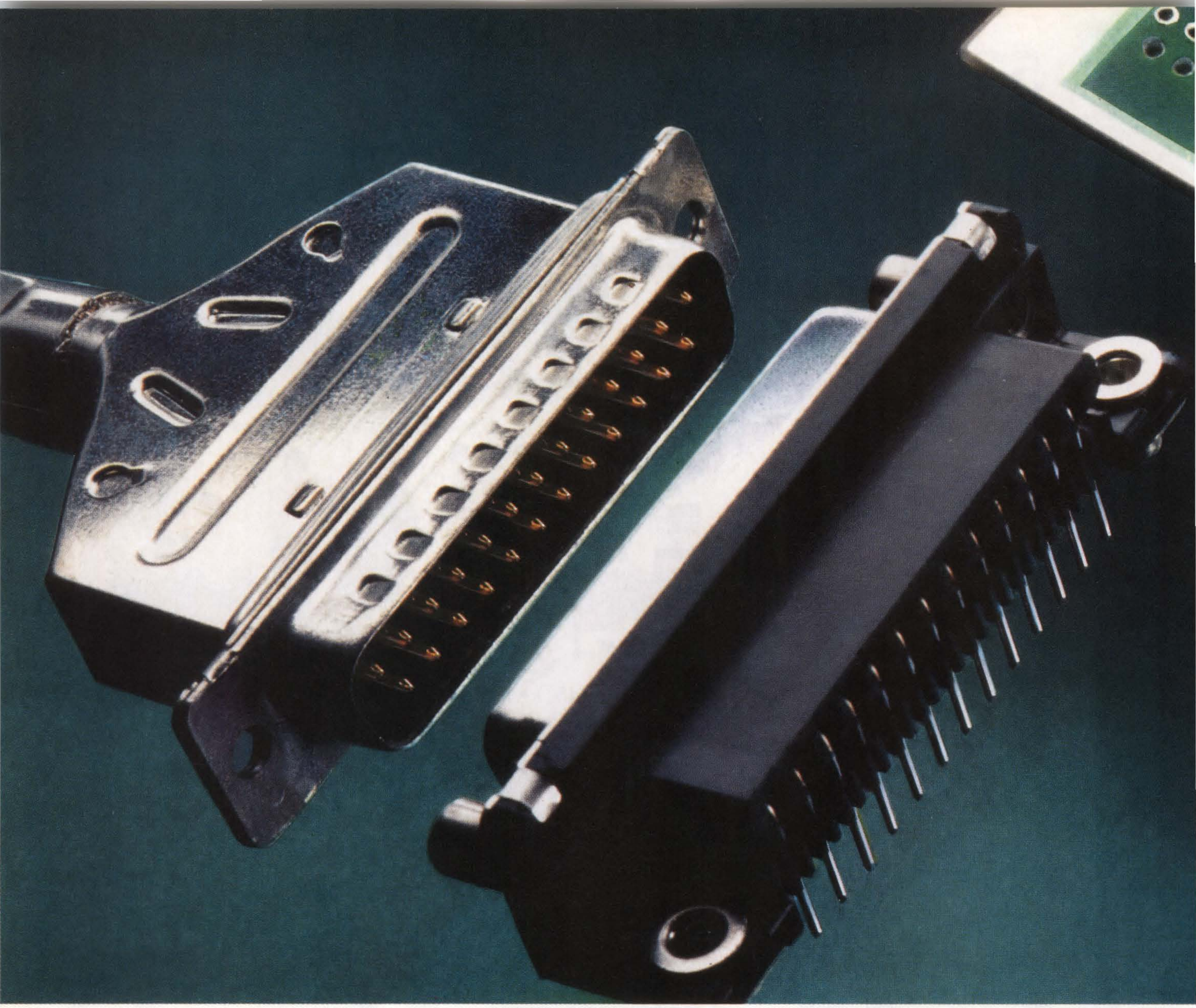

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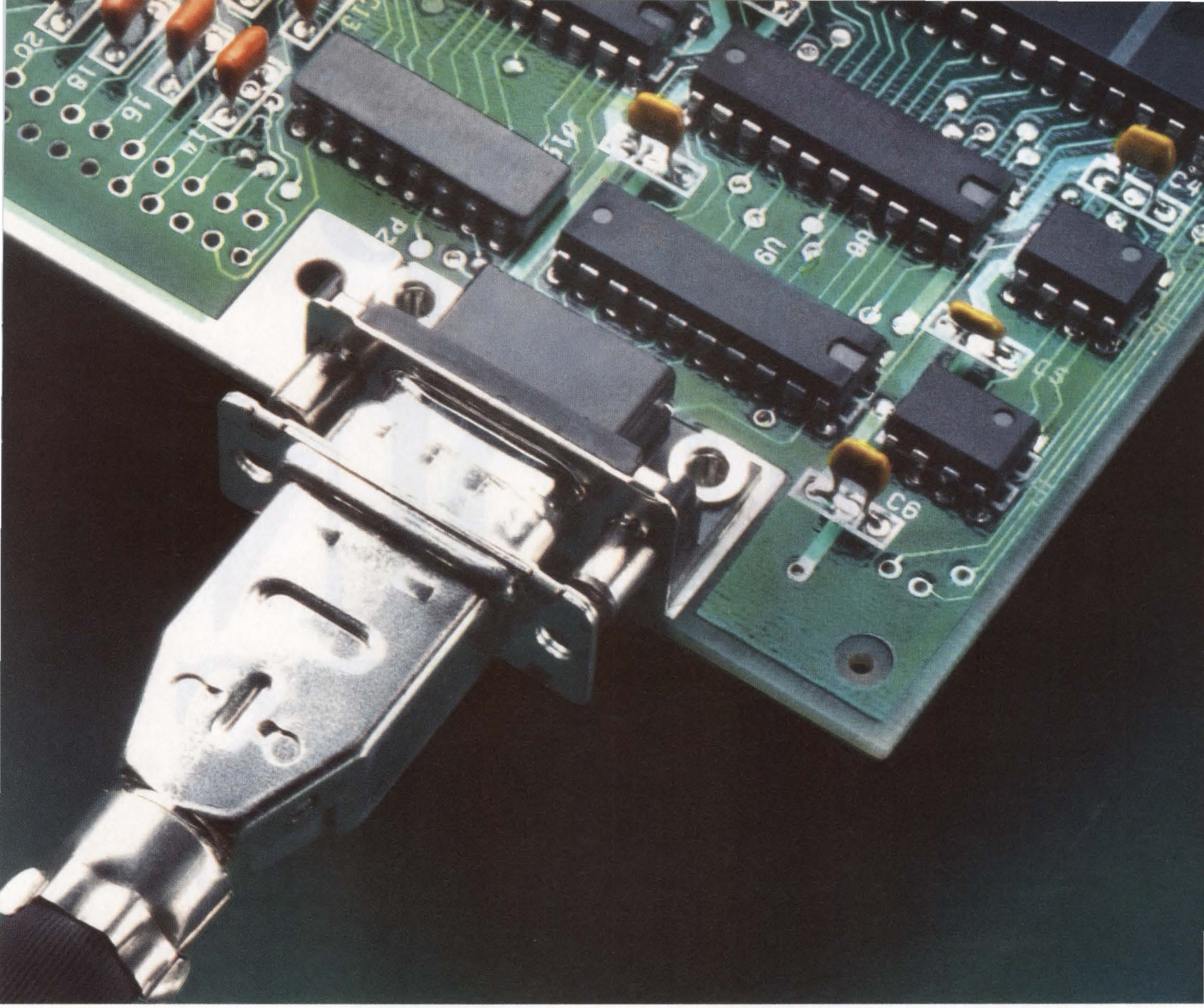

One step shielding/overmold kits save time and free up resources. Kits are available with solder, crimp/snap, and mass insulation displacement AMPLIMITE contacts.

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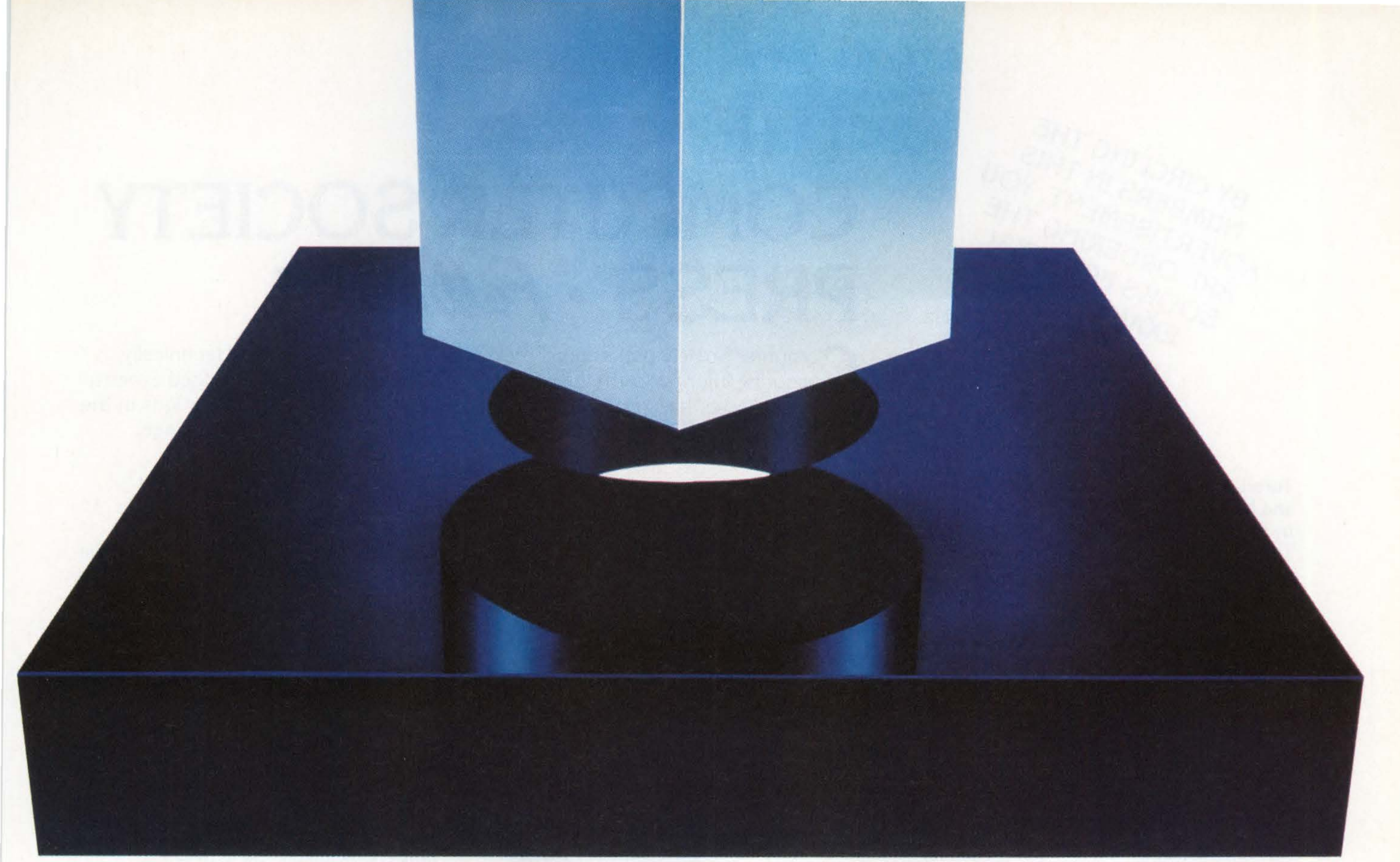

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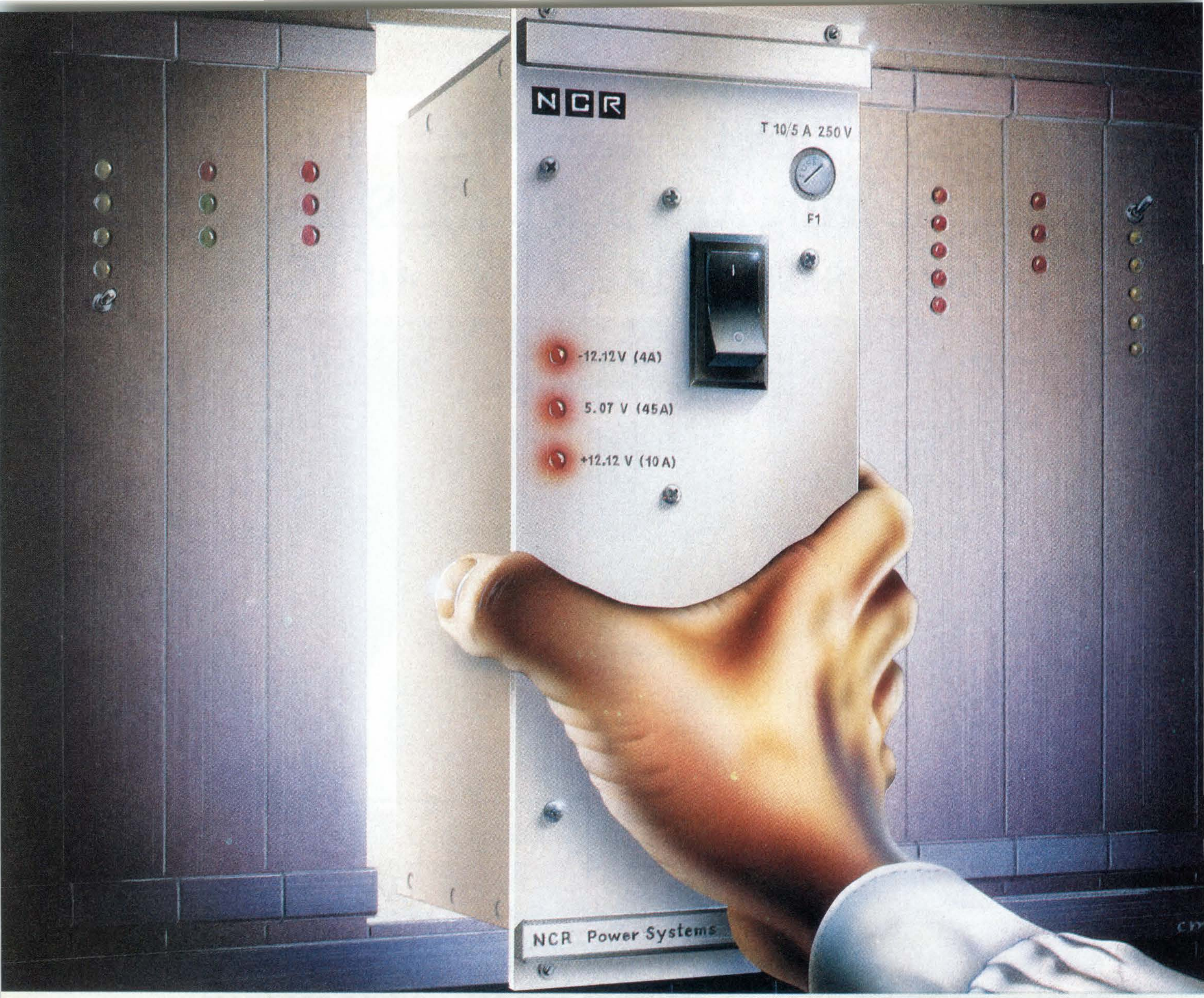

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Switching frequency is 80 kHz, and the unit has protection against overvoltage, overcurrent, and input surges. It meets the stringent safety and EMI requirements established by UL, CSA and TUV (VDE). Packaging complies with the Eurocard standards defined in DIN-41494 and IEC-297 for plug-in attachment to the motherboard. Precise (±0.4%) line and load regulation and 75% efficiency make the unit ideal for data communications and processing applications.

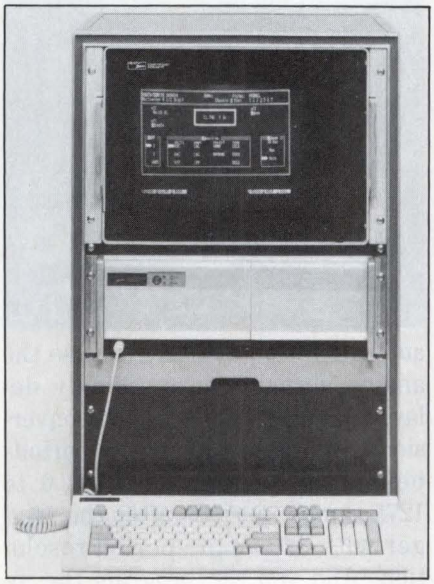
Standard units can be modified by NCR for precise conformance to customer requirements.

For detailed specifications and price quotation, contact NCR Power Systems, 3200 Lake Emma Road, Lake Mary, FL 32746; Telephone 800/327-7612 or in Florida, call 305/323-9250.

SEE US AT WESCON: BOOTHS 150 & 152

NCR

Industrial instrument system runs all MS-DOS-based software



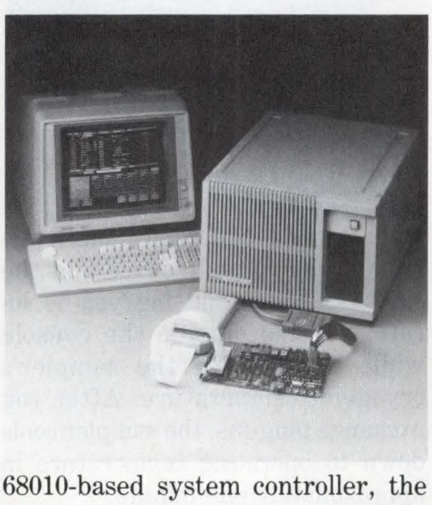
The SW-3020 computer-based instrument system works with a universal counter, a digital multimeter, an oscillator, a programmable dc power supply with three floating outputs, a function generator, and a module in which you can build prototype instruments of your own design. These modules accept optional plug-in front panels and conform to the height, length, and electrical specs of the IBM PC bus; however, they are thicker than standard PC expansion cards. They plug into and receive power from the vendor's expansion chassis.

To control the modules, you can use the vendor's SW-3000, a rack-mountable IBM PC/AT-compatible computer. In its standard configuration, this machine features 512k bytes of RAM, a 1.2M-byte floppy-disk drive, a 20M-byte hard disk, serial and parallel I/O ports, six open expansion slots, and a video adapter that supports Hercules graphics, MDA (monochrome display adapter), CGA (color graphics adapter), EGA (enhanced graphics adapter), and VGA (video graphics array) modes. For a video display, you can use the SW-3010, a 13-in. EGA monitor. The system runs all MS-DOS-based software and can also operate under the vendor's VIOS (versatile instrument operating software). System with computer, monitor, instrument chassis, chassis-interface cards and cables, instrument software, and calibration software, $8100; instrument modules, $1045 to $1490; instrument panels, $140 to $155.

Heath/Zenith, Computer-Based Instruments, Hilltop Rd, St Joseph, MI 49085. Phone (616) 982-3200. Booth No 2709.

Circle No 650

Logic-analysis system handles 160 channels at 2 GHz



You can configure the DAS 9200 logic analyzer to acquire 540 channels of data at 20 MHz with a 32k-bit-deep RAM in each channel, 432 channels at 200 MHz with 4k bits of RAM per channel, or 160 channels at 2 GHz with 8k bits of RAM per channel. When using the device as a stimulus source, you can equip it with 1008 channels capable of 50-MHz operation with 8k bits of RAM behind each pin.

One to four rack-mountable, 8-slot enclosures can house the system. Each has a built-in power supply, which can furnish 90W per card slot. The first enclosure houses the 68010-based system controller, the floppy-disk drive, and the hard disk. Specialized probing subsystems provide the interface to the unit under test.

Some of the functions performed include 200-MHz triggering, clock qualification, counting, timing, and recognition of edges and inter-module events. You can purchase hardware options that support testing of systems-based μPs with buses as wide as 32 bits. $11,425 to $150,000. Delivery, four to 16 weeks ARO.

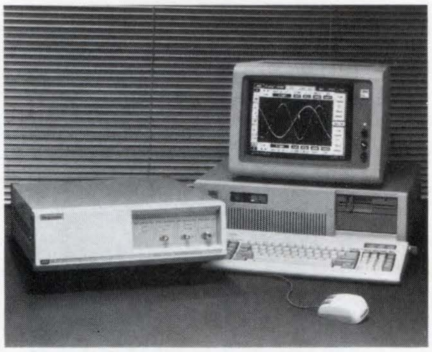
Tektronix Inc, Box 12132, Portland, OR 97212. Phone (800) 245-2036; in OR, (503) 231-1220. Booth Nos 2217, 2219, 2221, 2223.

Circle No 653

10-bit digitizer samples with 3-psec-rms aperture-width jitter

The Model 3000 waveform digitizer converts analog signals as high as 350 MHz into 10-bit digital words. It samples every nanosecond (1 GHz) or at any of eight intervals, the longest of which is 505 nsec. Using a 350-MHz sine-wave input, you get a spurious-response-free dynamic range greater than 50 dB typ, the equivalent of more than 8 bits. During the conversion of a 5-MHz signal, the S/N ratio improves to 57 dB.

You can communicate with the unit via its internal RS-232C interface and can store 1k word of sampled data in its memory. You can select dc or ac coupling (−3 dB below 10 kHz); program the full-scale sensitivity from 400 mV to 8V in five steps; and subtract input offsets of ± full scale (±5V max) in 256 programmable steps. The unit has



autocalibration ability. Because the analog signal is intentionally delayed, you can in effect start conversions from 0- to 992-sample periods before the trigger, or from 0 to 127k-sample periods after the trigger with 32-sample-period resolution. And you can program the internal trigger level over the full-scale signal range in 256 steps and the external trigger level over a ±2V range in the same number of steps.

Using the vendor's software, you can connect your dedicated IBM PC or compatible to as many as eight digitizers. The computer can then control programmable functions; store and display the digitized data; and perform FFT, phase, and power-spectrum calculations. Another digitizer, the Model 3100, provides a built-in μP-based IEEE-488 interface. You must supply your own software in order to control this instrument. Model 3000, $29,500; Model 3100, $31,500. Delivery, 60 days ARO.

Sequence Inc, 60 E Plumeria Dr, San Jose, CA 95134. Phone (408) 943-9707. Booth Nos 2749 and 2751.

Circle No 651

Superconductive sampler gives digital oscilloscope a 70-GHz bandwidth

The 70-GHz vertical bandwidth, 5-psec rise time, and 50-μV sensitivity of the PSP-1000 picosecond signal processor enable you to make measurements on the fastest circuits. Waveforms and associated messages appear on a 455×576-pixel, 13-in. color display.

The speed of this digital sampling oscilloscope derives from its use of Josephson-junction samplers operating at liquid-helium temperatures; the unit's 52×26.5×28-in. console houses all cryogenic-cooling support hardware. Plug-ins contain the samplers; you can get single- and dual-channel TDR (time-domain-reflectometer) and oscilloscope plug-ins. An optional module extender lets

you minimize the cable length between your signal source and the samplers by permitting you to locate plug-ins outside the console while maintaining the sampler's cryogenic temperature. After you exchange plug-ins, the sampler cools down to operating temperature in approximately one minute.

When ordering oscilloscope plug-ins, you can specify ±10, 100, or 1000 mV max full-scale vertical sensitivity. The plug-ins' dynamic range equals 46 dB at a 1:1 S/N ratio. You can select 1024, 512, 256, or 128 data points per waveform and can build the picture on screen by summing 256 or 1024 samples/data point. Sweep speeds range from 5 psec/div to 1 nsec/div; you can display as much as 30 psec of pretrigger signal. The built-in nonvolatile memory stores nine waveforms and their horizontal and vertical setups. Mainframe, $120,000; plug-ins, $30,000 each.

Hypres Inc, 500 Executive Blvd, Elmsford, NY 10523. Phone (914) 592-1190. Booth No 5040.

Circle No 652

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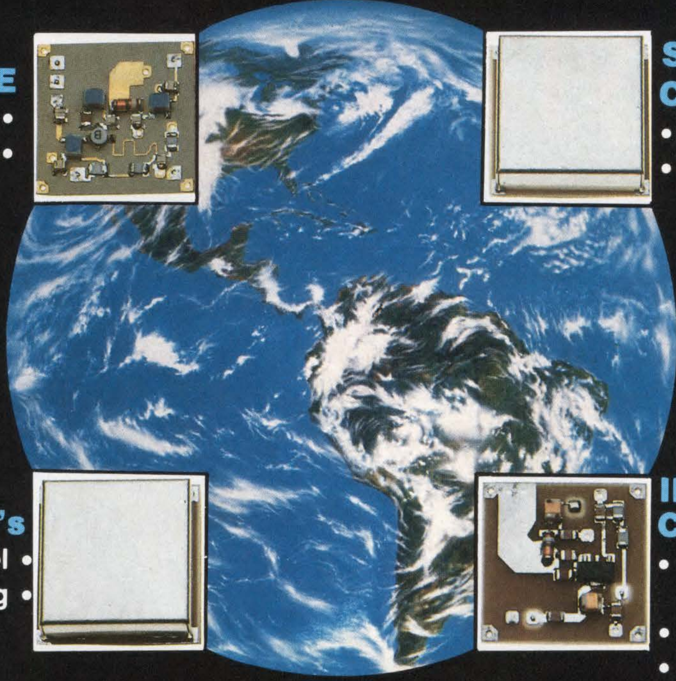

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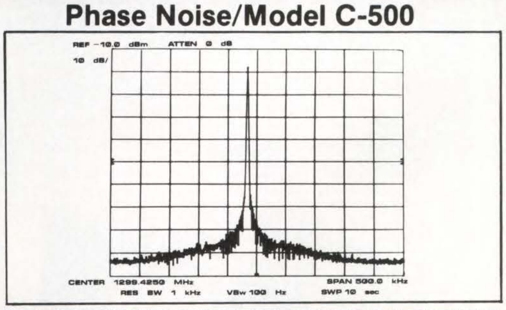

Z-Communications designs and manufactures Voltage Controlled Oscillators (VCO's), Synthesizers and RF-Modular products for the broad spectrum of applications ranging from Satellite Communications, Cellular Phones, CATV Industry, Instrumentation to RF-Modem LAN applications and many others with unique expertise in frequency ranges from MHz to 3GHz and to 22GHz respectively.
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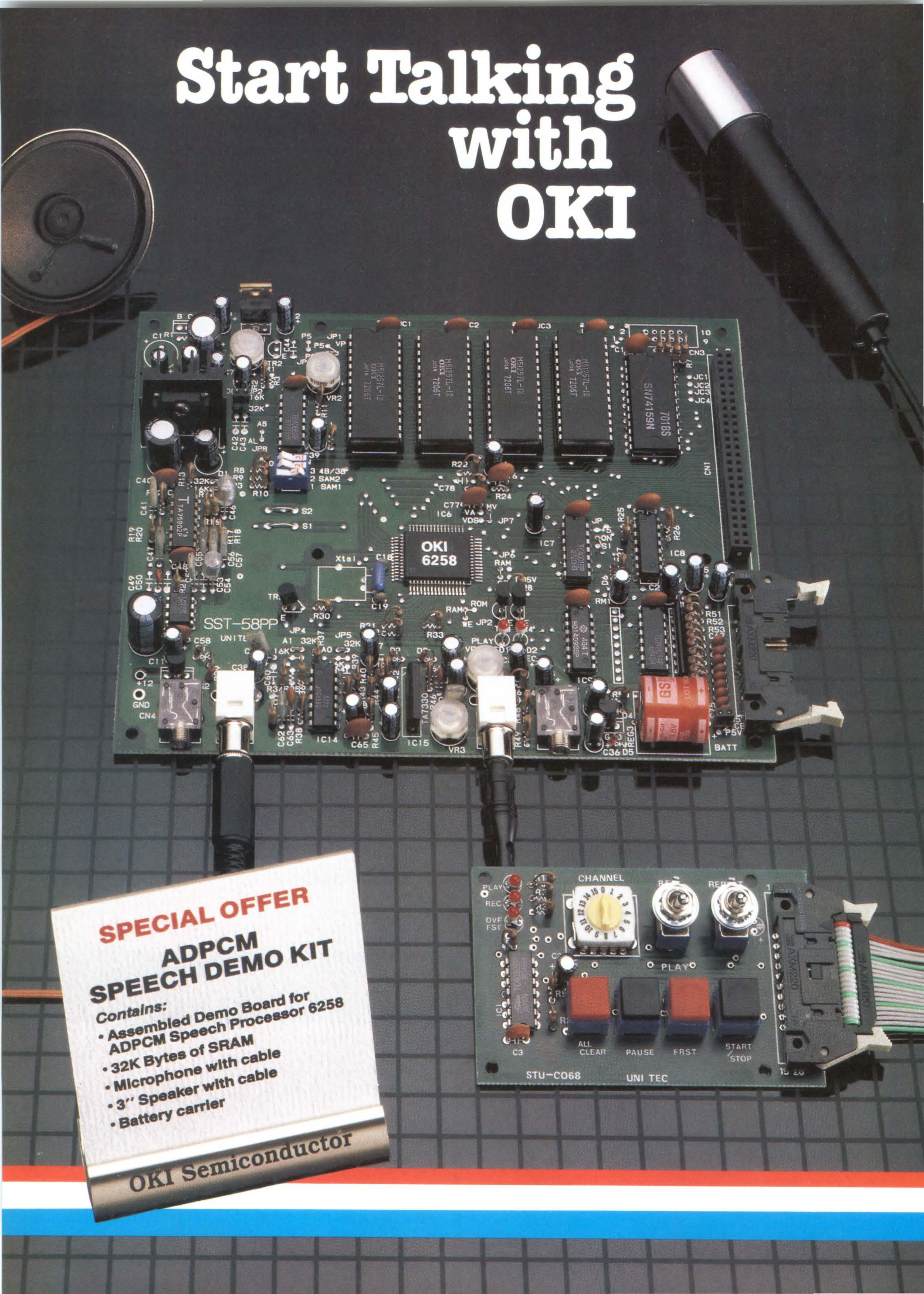
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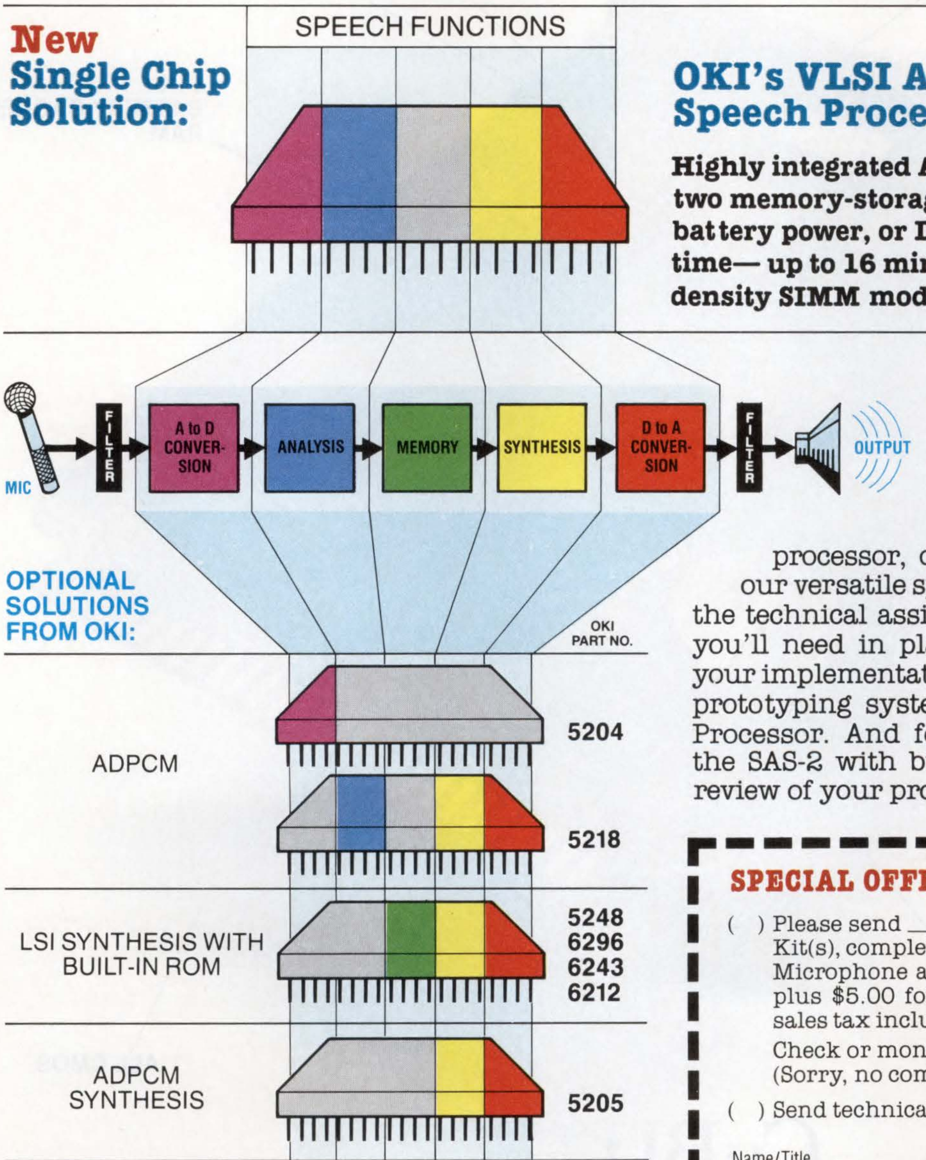

OKI's VLSI ADPCM Speech Processor 6258.

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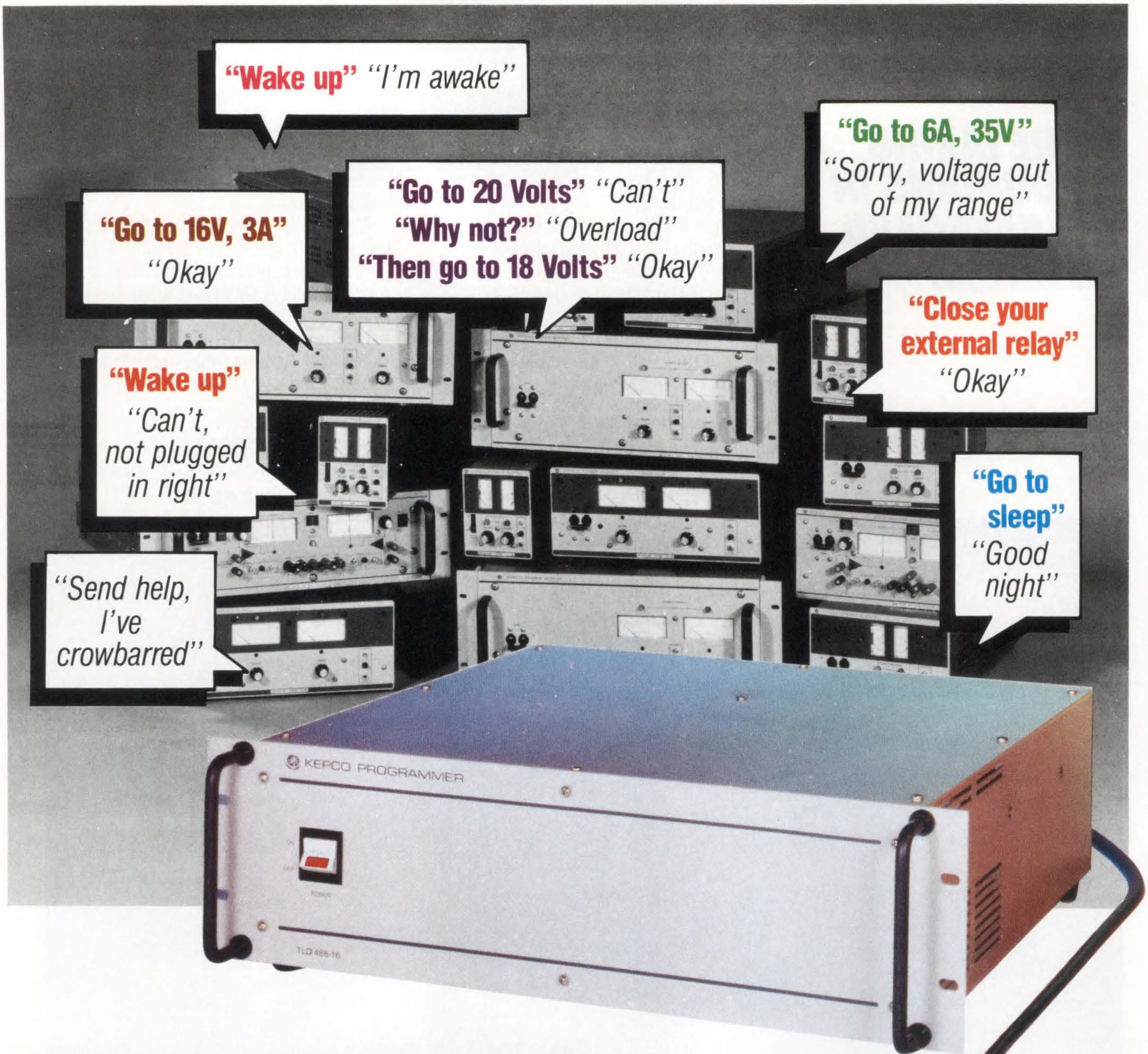

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CIRCLE NO 242

EUROCARD 68000 μCs

The Gescomp 8300-M has an 8-MHz 68000 μP, 512k bytes of RAM, and two 1M-byte 3½-in. floppy-disk drives. Its big brother, the 8340-P/HF, features a 16.7-MHz 68020 μP, a 68881 arithmetic coprocessor, a 3½-in. floppy-disk drive, and a 40M-byte hard disk. Both systems use the Eurocard board format and the G-64 bus. The typical system configuration leaves eight backplane slots free for boards of your choice. You supply the operator interface, an alphanumeric terminal; you can also add graphics controller boards that permit 640×480- or 1024×1024-pixel displays employing 256 colors from a palette of 262,144.

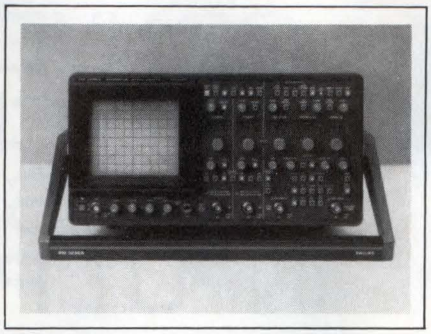
The systems run under the OS-9 operating system, which, with the appropriate library, can run programs written in C and intended to run under Unix. OS-9's memory requirements are low enough that you can put a version of it into ROM and thereby create a diskless system. The vendor's proprietary LAN allows 50 systems to communicate over 3000 ft of coaxial cable at 800k bps. $3995.

Gespac Inc, 50 W Hoover Ave, Mesa, AZ 85202. Phone (602) 962-5559. TLX 386575. Booth Nos 5607 and 5609.

Circle No 654

400-MHz SCOPE

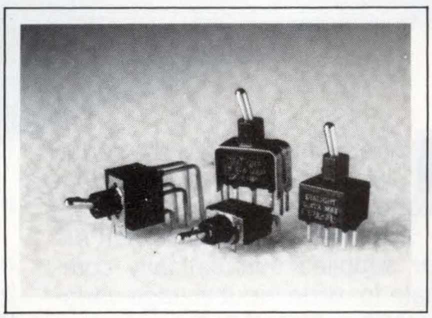
The PM 3296A provides a 900-psec rise time and a 4-div/nsec writing rate. You can position cursors to obtain an alphanumeric display of amplitude, time, frequency, and



ratio, and can also view scope settings. By using the trigger-level readout, you can set the scope to trigger only on events whose amplitude exceeds a predetermined limit. You can set sensitivity from 1 mV/div to 5V/div and can choose between 1-MΩ and 50Ω input impedance. An autoset function picks the channel to be displayed, adjusts the vertical position, and sets the voltage range, sweep speed, and trigger functions. The nonvolatile memory can store 75 front-panel settings. You can recall any setting by using an IR remote-control unit, or you can control the scope via the IEEE-488 bus. 400-MHz scope, $6000; 200-MHz version, $5000.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 426-0361; in WA, (206) 347-6100. TLX 185102. Booth No 2517.

Circle No 655



SEALED SWITCHES

Because 578 Series switches are sealed, you can subject them to wave soldering and cleaning, thus avoiding the cost of a postwave hand-soldering operation. You can choose either wire-wrapping or wave-soldering terminal styles, and you can select either sustained- or momentary-contact spdt and dpdt versions, with or without support brackets for vertical or horizontal mounting. You can specify silver contacts for 120V ac or 28V dc circuits where you switch 1A currents, or gold contacts for lower-power applications (0.4 VA max at 20V ac or dc). $1.77 (1000).

Dialight Corp, 1913 Atlantic Ave, Manasquan, NJ 08736. Phone (201) 223-9400. Booth Nos 1552, 1554, 1556, and 1558.

Circle No 656

PC AND PS/2 CAD

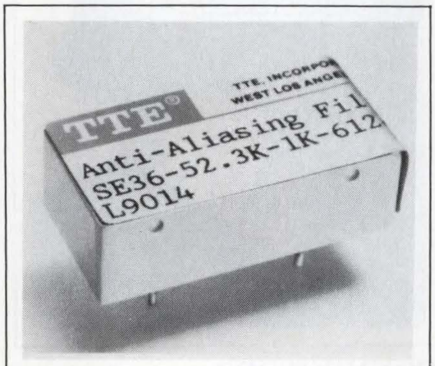
HiWire schematic-capture software lets you enter pc-board schematics on an IBM PS/2 or on a CGA- (color graphics adapter) or EGA- (enhanced graphics adapter) equipped IBM PC, PC/XT, PC/AT, or compatible. When you're finished, you can use SmartWork layout software to place the components on the board. The layout software's autorouter can route many of the conductors, and you can interactively route the remaining traces. While drawing schematics, you can move, rotate, mirror, copy, or delete objects. You can create your own libraries or select parts from TTL, CMOS, μP, memory, and discrete-component libraries.

You can design single- and double-sided boards and add a silkscreen. You can choose 12-, 16-, or 20-mil trace widths with 15-, 17-, or 19-mil min spacing, or you can select wide conductors in multiples of 50 mils. The programs are key-disk copy protected, but you can get backups that can be copied to load

onto your hard disk. HiWire and SmartWork, $895 each.

Wintek Corp, 1801 South St, Lafayette, IN 47904. Phone (800) 742-6809; in IN, (317) 742-8428. TLX 709079. Booth No 2044.

Circle No 657

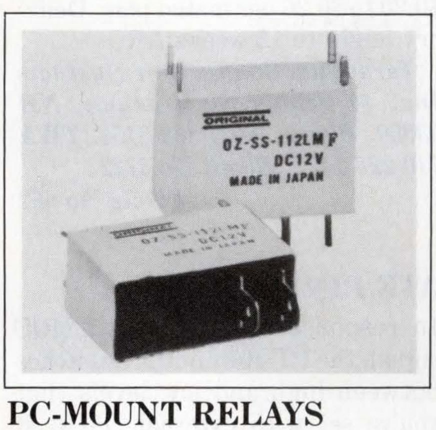


ANTIALIAS FILTERS

SE Series filters come in two case sizes—0.4×0.6×1.2 in. and 1.2×1.2×0.5 in. You can specify lowpass cutoff frequencies from 10 kHz to 20 MHz. The filters provide a dynamic range of at least 80 dB. A 0.4×0.6×1.2-in. unit that has a 20-kHz cutoff frequency and introduces 60-dB attenuation at 27 kHz (attenuation vs frequency is >120 dB/octave at 1.35 cutoff frequency) costs $130.

TTE Inc, 2233 S Barry Ave, West Los Angeles, CA 90064. Phone (213) 478-8224. Booth No 4600.

Circle No 659



PC-MOUNT RELAYS

You can solder the OZF Series relay to your pc board where it occupies 0.496×1.14 in. and picks up the coil-drive signal. On the opposite surface of the relay's 0.799-in.-high package, you'll find standard 0.187-in. quick-connect terminals tied to the silver cadmium oxide spst contacts. This arrangement facilitates field wiring in automotive, appliance, and process-control applications. The relay can switch 20A at 120V ac or 28V dc, and it can handle a ½-hp load.

When employed to switch the full rated load, the relay has a 100,000-operation life expectancy; when used for light-duty switching, it has a 5,000,000-operation life expectancy. The device is insulated to withstand 5 kV ac between coil and contacts; it can survive 10-kV surges. You can specify standard or high sensitivity at coil ratings of 3 to 48V dc. Delivery, eight to 12 weeks ARO. $2.15 (1000).

Original Electric Manufacturing Co Inc, 123B Lincoln Blvd, Middlesex, NJ 08846. Phone (201) 271-5770. Booth No 5613.

Circle No 658

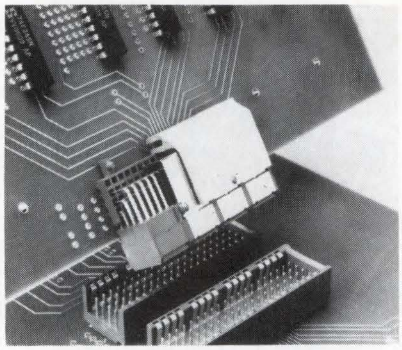
INLETS

TRON primary power inlets let you combine in one unit the functions of several ac-power-control components, including an ac-input connector, a line-voltage-selector switch, one or two fuse holders, and a power on/off switch. You can choose solderable or 0.187-in. quick-connect terminals and snap-in or flange-mount units. The units meet CEE-22 requirements and have the approval of various North American and European regulatory agencies.

After installing an inlet in your product, you can choose between 0.25×1.25-in. (North American standard) or 5×20-mm (European standard) fuses; just before shipping your product, you can insert fuses and a cord set, and set the line voltage so as to conform to the requirements of the country of destination. For a snap-in-mount inlet with quick-connect terminals, a dual-line-voltage selector, and a single fuse holder, $5.46 (1000).

Cooper Industries, Bussmann Div, Box 14460, St Louis, MO 63178. Phone (314) 394-2877. Booth Nos 1637, 1639, 1641, and 1643.

Circle No 660



CONNECTORS

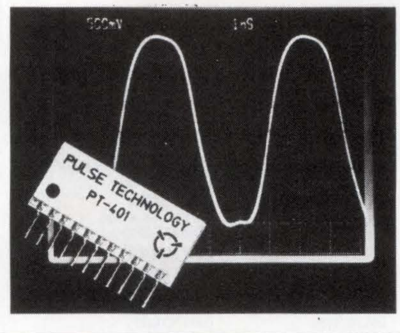
High Density Plus Two connectors, for mating pc boards with backplanes, add two rows of ground contacts to the four rows of signal connections offered in the vendor's earlier High Density Plus line. Because a ground line usually accompanies a high-speed signal, the new connectors enable the use of many more of their contacts for signals. The insulator's modular design lets you place many connectors end to end along the length of your boards. You can place other members of this product family on your card edge to bring high-current power-supply buses onto your board and to provide polarization and guidance. $0.20 to $0.26 per mated pair. Delivery, eight to 12 weeks ARO.

Teradyne Connection Systems Inc, 44 Simon St, Nashua, NH 03060. Phone (603) 889-5156. TWX 710-228-1431. Booth No 5722.

Circle No 662

ATE PIN DRIVER

In response to a TTL or CMOS signal, the PT-401's output switches between high and low levels that you've set with external DACs. If your drive is produced by ECL, you must supply a logic-level shifter. You can switch the output level from

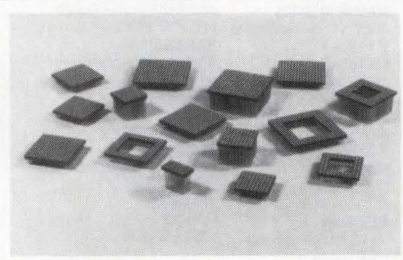


−5 to +10V or make it assume a high-impedance state. Operating with a 3V swing and a 50Ω load, the device can switch at 200-MHz max and can achieve rise and fall times of 1.35 nsec. The vendor also specifies the device to handle high-impedance loads. The device's 11-pin SIP measures 1.2×0.55×0.12 in.

You can mount the unit's companion module, the PT-412 buffer, beside or in line with it. The buffer obtains power from loosely regulated supplies. It buffers the two DAC outputs and provides the regulated ±5V needed by the PT-401. To null the offsets that the buffer can add to the DAC levels, you connect external resistors to the provided terminals. PT-401, $208; PT-412, $25. Delivery, eight weeks ARO.

Pulse Instruments, 1234 Francisco St, Torrance, CA 90502. Phone (213) 515-5330. Booth No 2629.

Circle No 661



PGA SOCKETS

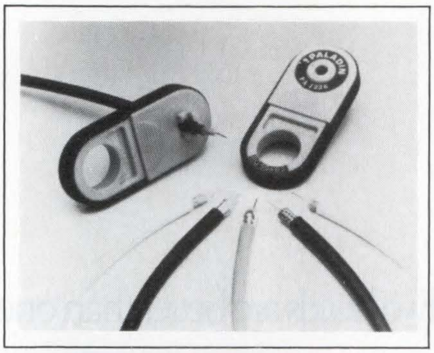
P Series sockets are molded from glass-filled polyester that has a 94V-0 UL flammability rating. Grid sizes range from 7×7 to 18×18 contacts. A 4-finger contact provides an average mating force of 2.3 oz/pin. The vendor also supplies PGA sock-

CIRCLE NO 240

ets that have glass-epoxy insulators. A molded socket with 68 solder-tail contacts and gold-over-tin plating, $3.25 (100).

Electronic Molding Corp, 96 Mill St, Woonsocket, RI 02895. Phone (401) 769-3800. TWX 710-387-1350. Booth Nos 1223 and 1225.

Circle No 663



WIRE STRIPPER

The Toggle coaxial cable stripper employs a toggling blade system to remove braid and dielectric quickly, accurately, and repeatedly. The 3-in.-long, 1.25-oz tool can handle 1-, 2-, and 3-level stripping. It's available in six sizes that handle RG58, RG59, RA62AU, RG6, 8281, and RG8/11 video cable. The vendor will build custom units for other cable types. $24.95.

Paladin Corp, 3543 Old Conejo Rd #102, Newbury Park, CA 91320. Phone (805) 499-0318. TWX 910-494-2799. Booth Nos 2304 and 2306.

Circle No 664

MIXED CONNECTOR

This cylindrical connector mixes fluid/pneumatic, high-voltage, standard, and coaxial contacts. The unit has four 50Ω coaxial contacts, two 5-kV working-voltage contacts rated to carry 4A each, eight 22-AWG standard contacts, and four 145-psi fluid/pneumatic contacts, three of which have a 1.3-mm ID and one of which has a 1.6-mm ID. The unit has an ASTM C385 brass shell and Peek dielectric, and is guaranteed to survive 5000 mate/unmate cycles. $266.24 (500). Delivery, 20 weeks ARO.

Lemo USA Inc, Box 11488, Santa Rosa, CA 95406. Phone (707) 578-8811. TLX 340933. Booth Nos 1621 and 1623.

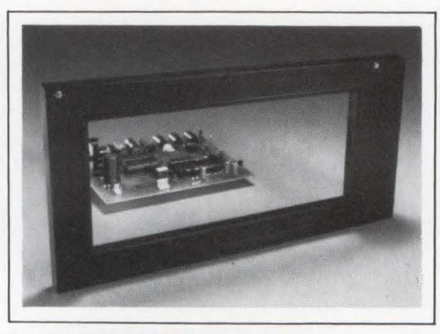
Circle No 665

MEMBRANE PANELS

You can have this line of touch-sensitive panels made to your specifications, with single or multiple switches in sizes from 1 in^2 to 5 ft^2. The vendor prints overlays using close-tolerance silk-screen or photoresist/etching processes. You can specify the actuation force and can purchase embossed, shielded, or backlit panels, as well as units with LED indicators. A unit with 50 tactile-feedback keys, five colors, a numeric-display window, an aluminized Mylar EMI shield, a metal backplate, and a connector at the end of a 6-in. tail, $30 (1000). Delivery, eight to 10 weeks ARO.

The Hall Co, 420 E Water St, Urbana, OH 43078. Phone (513) 652-1376. Booth No 5604.

Circle No 667



TOUCHSCREENS

You can mount Cyclops ES Series touchscreens over your display, or you can purchase them preattached

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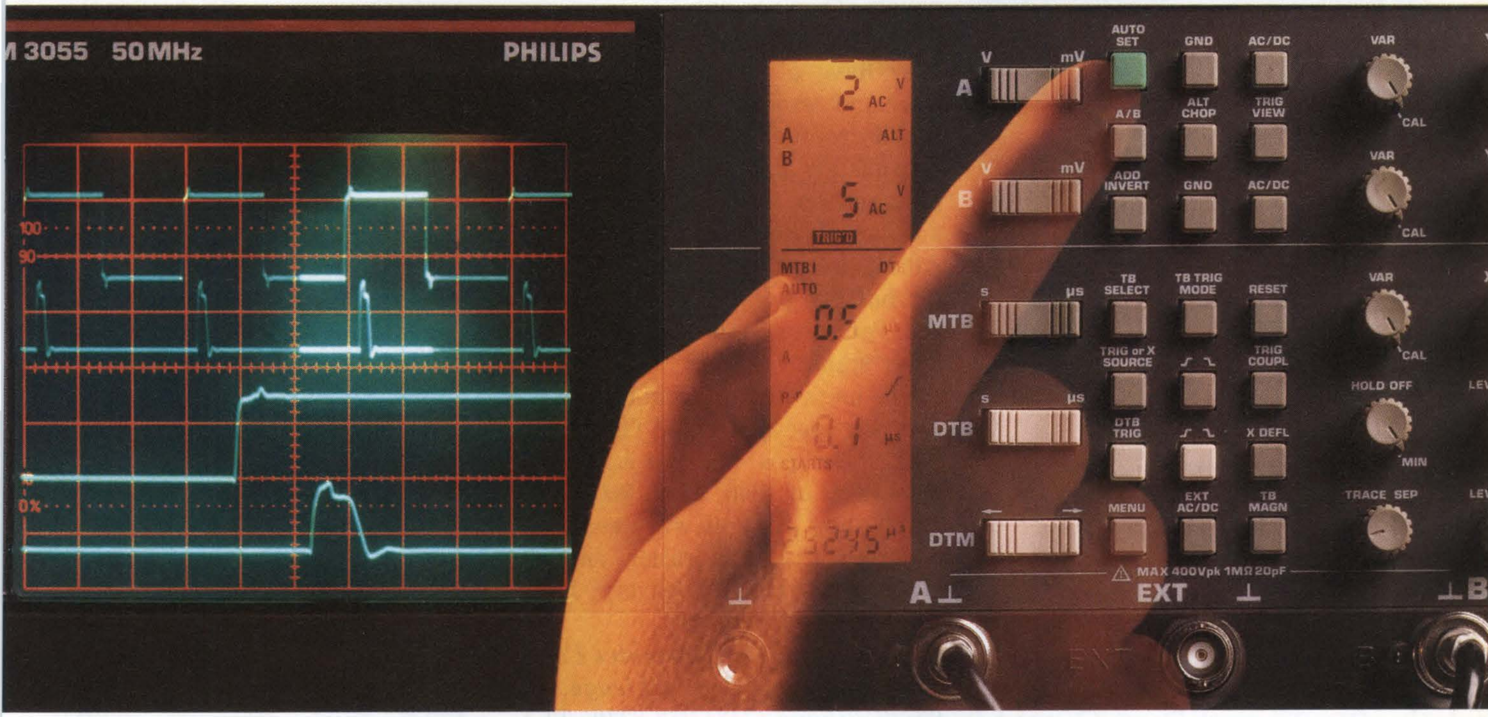

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For about what you'd pay for the next-best scope you get innovative engineering that's more productive and easier to use. You get plug-in modularity and IC microelectronics for reliability you've never seen in this class before. Plus, for a limited time, you get a no-risk, no-questions-asked, 30-day money-back guarantee. So why wait any longer?

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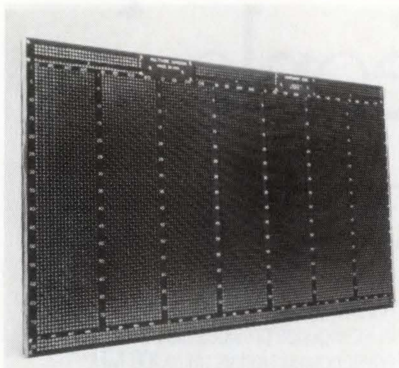
CIRCLE NO 238

to 640×200-pixel twisted-nematic LCD, electroluminescent, or plasma panels. They use one LED and one CCD sensor to cover a 4×9-in. area; they have a response-time of 50 msec and resolution to 100×70. The touchscreen frame protrudes approximately 0.75 in. from the display screen. The LED, detector, and associated electronics draw <0.5W from 12 and 5V dc supplies; for battery-powered applications, the vendor supplies a unit with lower standby power.

The units operate from 0 to 50°C. You can specify serial-TTL or RS-232C interfaces, and you can select data rates of 1200, 4800, 9600, and 19,200 bps. Six software routines facilitate setup, calibration, and operation. $115 (5000). Delivery, six to eight weeks ARO.

Wells-Gardner Electronics Corp, 2701 N Kildare Ave, Chicago, IL 60639. Phone (312) 252-8220. TLX 253286. Booth No 812.

Circle No 666



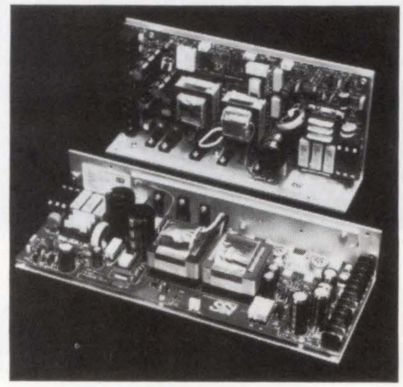
PROTOTYPING PANELS

Protoboard Series prototyping panels offer closely controlled characteristic impedance, thereby optimizing the high-frequency performance of your circuits. If you provide an X-Y coordinate net list with your order, the vendor will ship you a 100% electrically tested wired board within 10 days ARO. If you supply wiring data as a schematic or as a symbolic net list, delivery takes longer.

The vendor's Multiwire process uses 4-mil-diameter (38-AWG) wire to fabricate the boards. You can mount them in your card cage on the same centers as etched circuit boards; they have no surface wires to obstruct component access. To achieve the 10-day turnaround, you must use one of the vendor's six pretooled board formats, which include five Mupac types and a Multibus I compatible. $485 to $1700.

Multiwire/East, 250 Miller Pl, Hicksville, NY 11801. Phone (516) 933-8300. Booth No 2059.

Circle No 668



DC/DC CONVERTERS

The SQC125 dc/dc converter delivers 125W from a 2.5×5×10.5-in. package, and the SQC180 delivers 180W from a 2.5×5×13.5-in. package. You can allow the input to vary from 42 to 60V dc—the range you need to drive the supply from a 48V-nominal bank of lead acid cells. You specify triple or quadruple outputs at either power rating. In the 125W unit, the main output produces 5V at 20A; in the 180W unit, the main output (5V) supplies 35A. The secondary outputs source 5A at 12, 15, or 24V, depending on your specification.

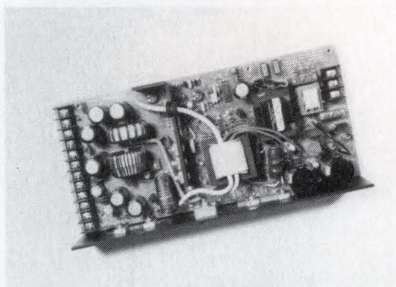
Built-in protection prevents short circuits from damaging individual outputs; overvoltage protection safeguards the load if the supply malfunctions. Though both devices can deliver rated output power continuously at an ambient temperature of 50°C and can supply 50% of their rated power at 70°C, don't try

CIRCLE NO 235

to draw maximum current from all outputs at once; that would exceed the overall power ratings. Both devices have line filtering to minimize the ripple current your primary dc source must furnish; shielded power transformers minimize the injection of switching spikes into your load. SQC125, $180; SQC180, $231 (100). Delivery, three to six weeks ARO.

Switching Systems International, Box 1599, Placentia, CA 92670. Phone (714) 966-0909. Booth Nos 455 and 457.

Circle No 669



AC/DC SWITCHERS

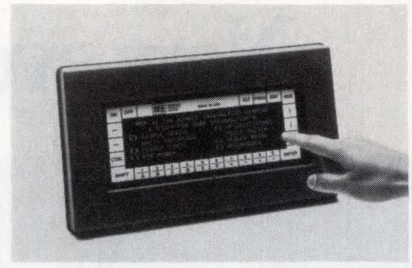
The EM160, EM200, and EM350 open-frame switching supplies produce continuous outputs of 130, 200, and 300W and transient-peak outputs of 160, 250, and 350W, respectively. The multiple-output units are designed to meet international safety specs and are currently undergoing certification testing. $1/W (OEM qty). Delivery, stock to 10 weeks ARO.

Elpac Power Systems, 3131 S Standard Ave, Santa Ana, CA 92705. Phone (714) 979-4440. Booth No 928.

Circle No 670

VF TOUCHSCREEN

The 4283-01 PEP (peripheral entry panel) combines a 6-line×40-character vacuum-fluorescent (VF) display with an IR touchscreen. You can set up as many as 969 separate touch-sensitive areas on the panel. Although the touchscreen uses infrared sensors, it won't trigger on ambient light or even direct sun-



light. Its touch-sensitive areas extend beyond the display's periphery, so you can set up additional fixed-function switch locations outside the display and designate them with legends, which the vendor will silk-screen onto the touchscreen frame as an option.

The touchscreen's VF display has 5-mm-high characters; under software control, its brightness can be set at three levels to 185 fL max. The unit includes 8k bytes of battery-backed CMOS RAM, which you can use to store as many as 127 "canned" messages. The device operates from a 5V supply. The onboard μP controls all functions, including built-in diagnostics and host-computer communications, via a port that you can configure for RS-232C or RS-422 interfaces. $800 (100).

IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556. Booth Nos 1230, 1232, and 1234.

Circle No 671

OPTOISOLATORS

The MOC3081 Series optoisolators combine a GaAs LED with a monolithic circuit that integrates a photodetector, a line-voltage zero-crossing detector, and a triac driver capable of holding off 800V and guaranteed not to trigger with a 600V/μsec dV/dt (1500V/μsec typ). The devices' 6-pin miniature DIPs can withstand over 7500V between input and output. Their 800V triac drivers can tolerate over 100V more than the p-p voltage on a 240V ac line. You can choose among devices with 5-, 10-, or 15-mA trigger currents at a 100-μsec trigger-pulse

Text continued on pg 177

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Resolution to 1μV dc, 10μA dc, 1mΩ		Resolution to 100nV dc, 1μA dc, 100μΩ	
One-year specifications and warranty		Two-year specifications and warranty	
8840A	$795	8842A	$995
8840A-09 with AC True RMS	$990	8842A-09 with AC True RMS	$1,245
8840A-05K IEEE-488 Field Kit	$170	8842A-05K IEEE-488 Field Kit	$170

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* Patent pending

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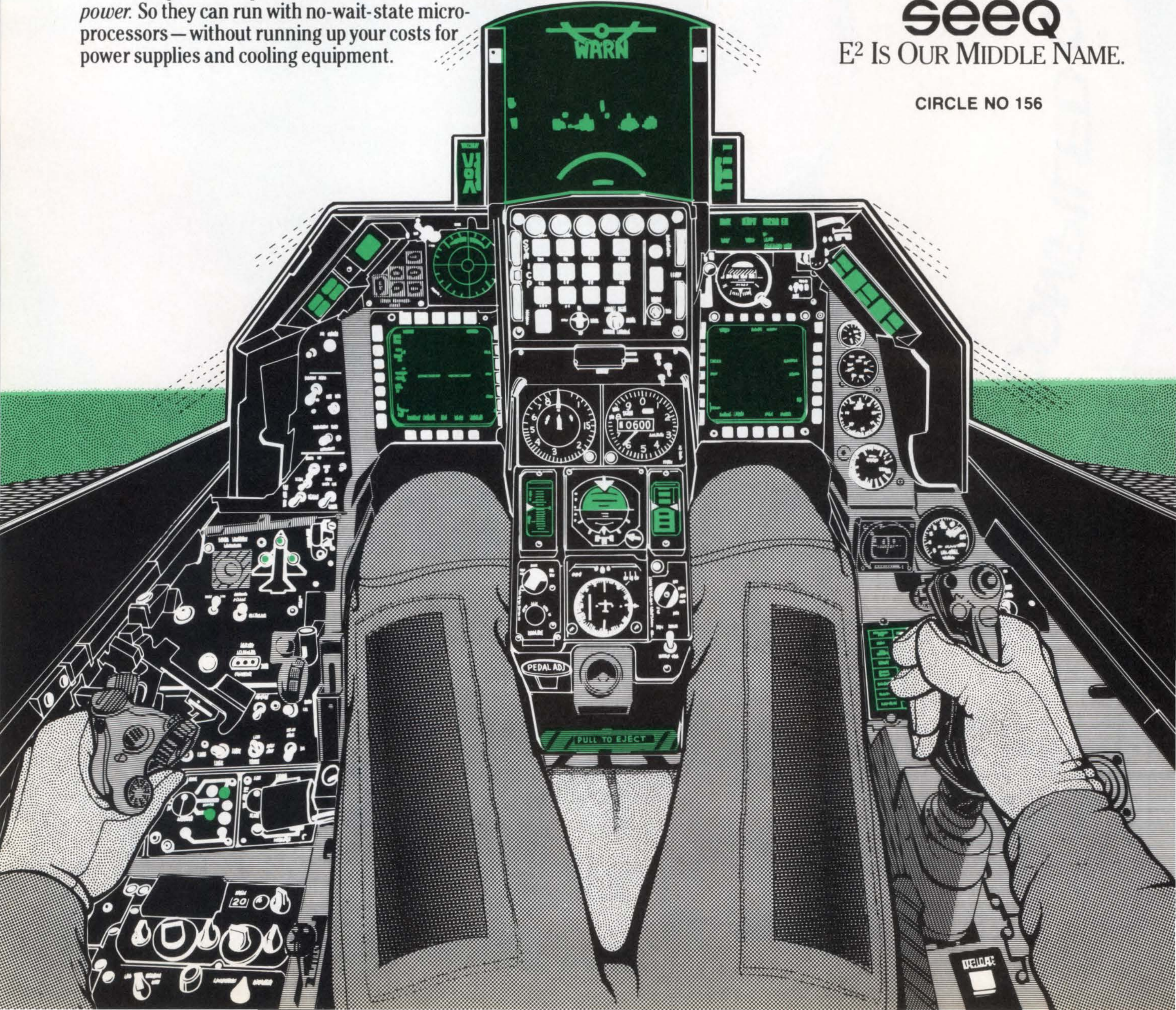

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width. With 15-mA trigger current, \$1.54 (1000). Samples available from stock. Delivery of production quantities, stock to eight weeks ARO.

Motorola Inc, Semiconductor Products Sector, Box 52073, Phoenix, AZ 85072. Phone (602) 244-3818. Booth No 652.

Circle No 672

CONTROLLER

If you design control systems, the CDI-Ladder lets you employ an STD Bus-based approach to building your hardware without forcing you to learn an unfamiliar programming language. Using a standard relay-logic language, you can develop programs for the Z80-based process controller on an IBM PC or compatible. The hardware includes a 6-slot card cage that houses the CPU board and an integral power supply. In the remaining slots, you can add DACs, an ADC, and the vendor's math coprocessor and analog and digital I/O cards. When you've filled the first cage, you can add 2- to 24-slot cages housing additional cards until you've expanded your system to 416 analog and 1152 digital I/O points. A fully loaded system handles 40 PID (proportional-integral-differential) loops and 32 stepper drums. \$1195.

Computer Dynamics, 107 S Main St, Greer, SC 29651. Phone (803) 877-8700. Booth No 5708.

Circle No 673

MACINTOSH CAD

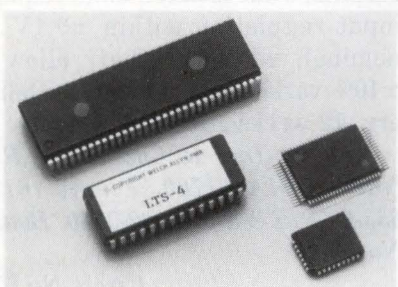
If you have a 512k-byte Apple Macintosh or a Macintosh II, you can use Professional System software to capture pc-board schematics, place components, and automatically route many of the traces. The program handles boards as large as 32×32 in. with surface or through-hole-mounted components and as many as 16 layers. It even simulates the operation of your circuit and displays the results in a screen window. You use a command file to

specify routing parameters.

When determining where to place a trace, the router will compare the relative cost of using buried vias as opposed to thinner traces or smaller spacing between traces. The program can drive pen plotters, laser printers, and dot-matrix printers. It can produce files that drive a Gerber plotter. If you are laying out double-sided boards, you can send your output files to the program's vendor, who will ship you prototypes in three days; if you are designing multilayer boards, the vendor can generate photoplots from your files. Professional Layout, $1500; Schematic Capture and Autorouter, $700 each.

Douglas Electronics, 718 Marina Blvd, San Leandro, CA 94577. Phone (415) 483-8770. Booth Nos 911 and 913.

Circle No 674



BAR-CODE DECODER

The LTS-4 bar-code decoder chip set simplifies the task of designing bar-code-reading capabilities into your product. It consists of a processor and a PROM. You can connect any of 10 input devices to the processor—five lasers, three contact sensors, a machine-mounted slot reader, and a machine-mounted noncontact sensor. The set's software handles nine symbologies, so you can make your product meet the requirements of several customers without modifying the hardware. Its minimum laser-scan time of a bar-code element is 22 μsec; when used for hand scanning of high-density codes, it can operate at 2 to 50 ips. You can choose surface-mount or through-hole packages. Four packages are available: the SMT processor in an 80-pin flat pack; the SMT PROM in a 32-pin PLCC; the leaded processor in a 64-pin shrink DIP; and the leaded PROM in a 28-pin DIP. $118.

Welch Allyn Inc, Box 187, Skaneateles Falls, NY 13153. Phone (315) 685 8351. TLX 325435. Booth No 538.

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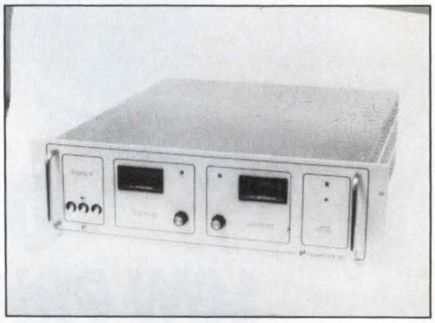

POWER SUPPLY

The 4600 power supply produces 5 kW of regulated dc in a 5.25×19.5×20.25-in. rack-mountable package. You can specify single-output voltage to 60V; lower-voltage versions produce current to 500A. You can connect the outputs in series or parallel and can use any unit as a master or a slave. The remotely programmable units provide rated power at ambient temperatures to 50°C. The output voltage and current are regulated to within 0.1% of their maximum; at fixed line, load, and temperature, the output varies no more than 0.05%/8 hours. The ripple is 15 mV rms. $2700.

Power Ten Inc, 486 Mercury Dr, Sunnyvale, CA 94086. Phone (408) 738-5959. Booth No 2754.

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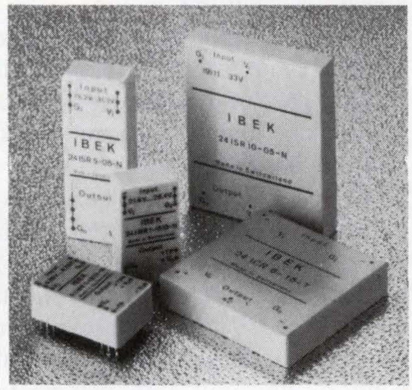
IBEK Series encapsulated dc/dc converters and ISR Series switching regulators conform to industry-standard package configurations and provide single and multiple regulated outputs. You can get units with or without ohmic input/output



isolation; that draw power from dc sources of 5, 12, 15, 24, 28, or 48V; and that produce one, two, or three outputs.

The two families include units with output power ratings from 1 to 10W; the operating temperature range on some models extends from −40 to +85°C without derating. Nonisolated switching regulator modules meet specifications with inputs from 4 to 33V higher than their outputs; some isolated units require input regulation within ±0.1V of nominal, whereas others allow a ±10% variation. $44 to $111. Delivery, 12 weeks ARO (OEM qty).

Melcher Inc, 10 Cochituate Rd, Natick, MA 01760. Phone (617) 653-9979. TWX 510-100-3830. Booth No 5550.

Circle No 676

RGB RAM/DAC

The monolithic CMOS/TTL-compatible RGBDAC3405S incorporates three 4-bit DACs, three 4-bit-wide×32-nibble-deep static RAMs, an internal temperature-compensated voltage reference, and all the control logic required for a full graphics/color-monitor interface. The device gives you control over output enable, multiplex address, and overlay features, as well as control over black, white, and sync levels. You can use it to produce signals that conform to EIA standards 170 and 343. Each DAC output can drive a 75Ω coaxial cable terminated at both ends; 32 colors are available at a 60-MHz pixel rate. The devices

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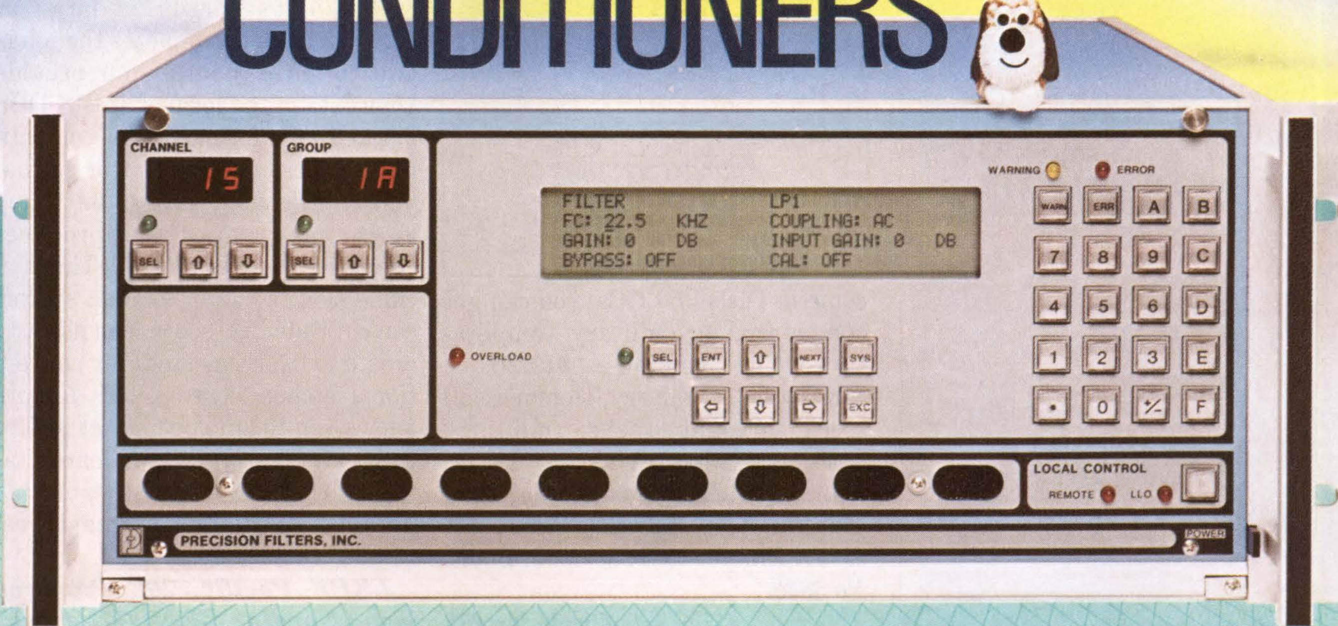

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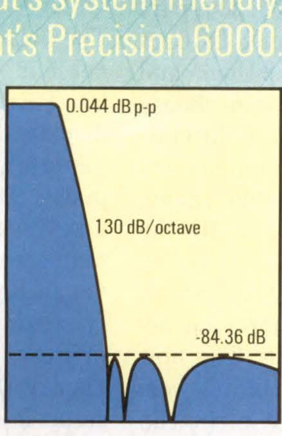

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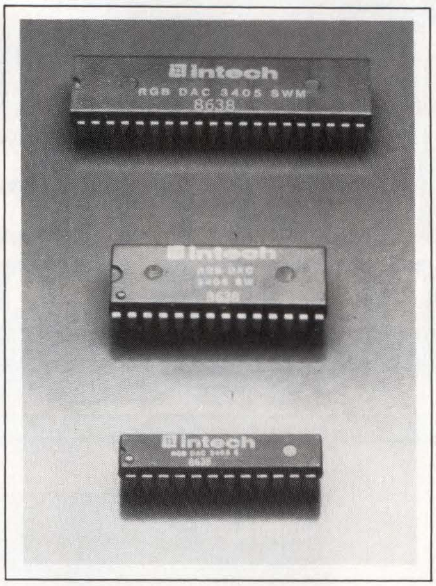


come in DIPs or LCCs; you can get commercial or military temperature-range versions. $19.20 to $73.25 (100). Delivery, (commercial) stock to eight weeks; (military) stock to 12 weeks ARO.

Intech Advanced Analog, 2270 Martin Ave, Santa Clara, CA 95050. Phone (408) 988-4930. Booth No 5630.

Circle No 678

A/D CONVERTER

In a single 40-pin hybrid DIP, the ADC-00300 combines a 12-bit ADC and a track/hold amplifier. The part uses a custom monolithic DAC, a discrete op amp, and both thick- and thin-film resistors. You can choose among nine unipolar and bipolar input ranges. The maximum linearity error is 0.05% of full-scale range; the minimum S/N ratio is 65 dB; the harmonics are at least 68 dB below full scale. You need only furnish an encode command to trigger an acquisition/conversion cycle. The unit operates from −55 to +125°C; versions are available that meet the requirements of MIL-STD-883. From $750. Delivery, eight to 12 weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324. Booth Nos 721 and 723.

Circle No 679

PROTOFAB SYSTEM

The ColorCam system lets you manufacture small quantities of double-sided PC boards using the manufacturer's dry-etch method. Part of the system is an X-Y machine tool that routes the board to your outline, drills holes, and removes copper from the laminate by milling. This tool handles boards as large as 16.5×15 in. and completes the job in two to three hours. You provide your data in the form of an MS-DOS database file formatted for compatibility with a Gerber plotter so that you can do your layout with any CAD program that produces Gerber-compatible files. The machine tool in the ColorCam system can cut Rubylith, so you can use it to create artwork masters for conventional etched boards. This feature allows you to employ one set of files to create the prototype boards, as well as the artwork masters used to obtain production quantities. $10,000 to $30,000.

LKPF Pacific, 20C Pamaron Way, Novato, CA 94947. Phone (415) 883-1717. TLX 470875. Booth Nos 1925 and 1927.

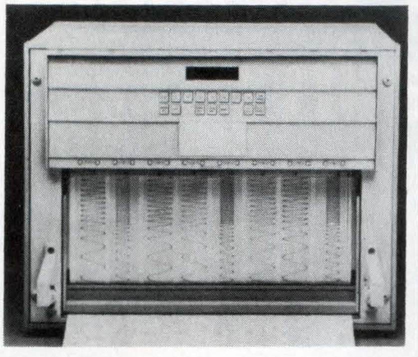
Circle No 680

CONTROLLER

The C220 board allows electroluminescent and plasma panels to emulate DEC's VT220 terminal. You can display 25 lines of 80-column text on panels with 512×256 or 640×200 pixels. The board provides ports for a keyboard and a printer, and communicates with the host computer via an RS-232C port. Menus simplify setting up terminal, keyboard, printer, communications, and tab display parameters; you store your setup in onboard nonvolatile RAM. Four character sets reside in ROM; you can define four additional sets. $595 (100).

Digital Electronics Corp, 31047 Genstar Rd, Hayward, CA 94544. Phone (415) 471-4700. TLX 172073. Booth No 1340.

Circle No 681



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The 3000 Series oscillographs employ a pressurized ink-writing system and can provide four colors in one recorder. You can get recorders with one to eight channels; other features include a <4-msec rise time and <0.35% nonlinearity. A direct-entry keypad allows you to enter text to annotate the recordings; the recorder prints text between the channels.

The oscillographs have 21 fixed-chart speeds from 500 mm/sec to 5×10^{-6} m/sec. In addition, the stepper-motor chart drive allows you to select intermediate speeds. One of the plug-in preamplifiers is remotely programmable. You can specify a recording system that is fully remote controlled via either RS-232C or IEEE-488 ports. Two-channel version, $3600; 8-channel version, $10,000. Delivery, 30 to 60 days ARO.

Gould Inc, Recording Systems Div, 3631 Perkins Ave, Cleveland, OH 44114. Phone (216) 361-3315. Booth No 2327.

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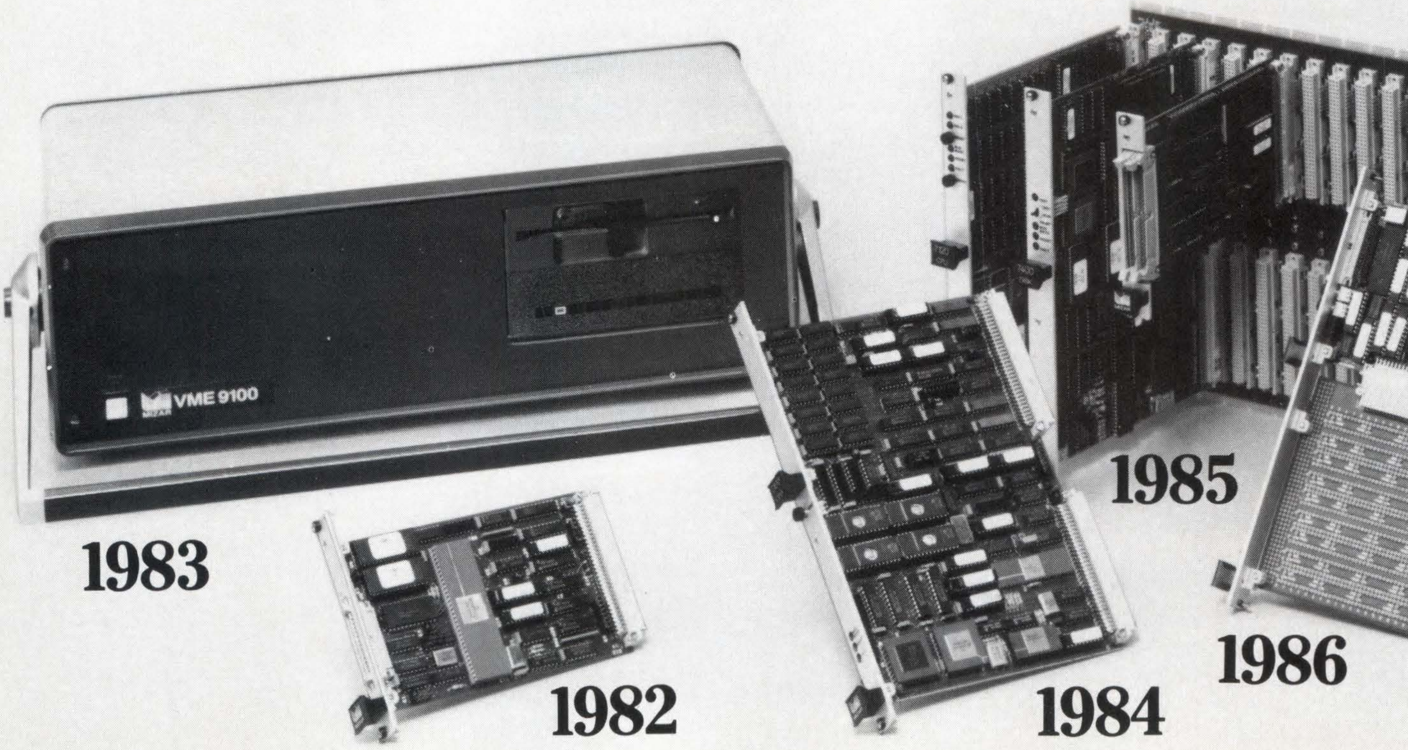

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1985—Mizar introduces the first VME development system with double- and single-height cards. The Mizar 9500 made it possible for designers to pay for only as much capacity as they actually needed. Additional design freedom stemmed from the system's expansion slot enabling designers to add their own custom features to the system.

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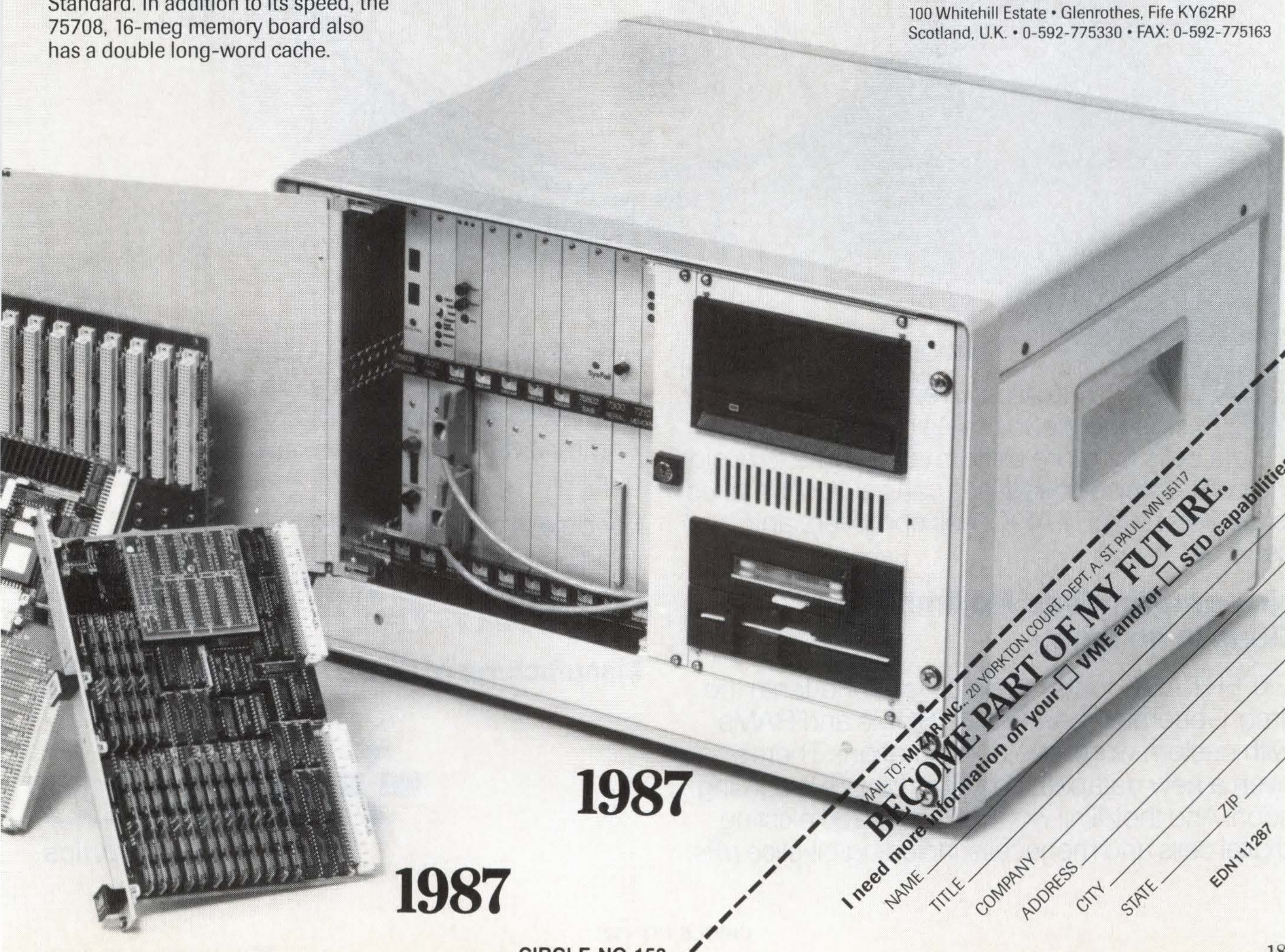

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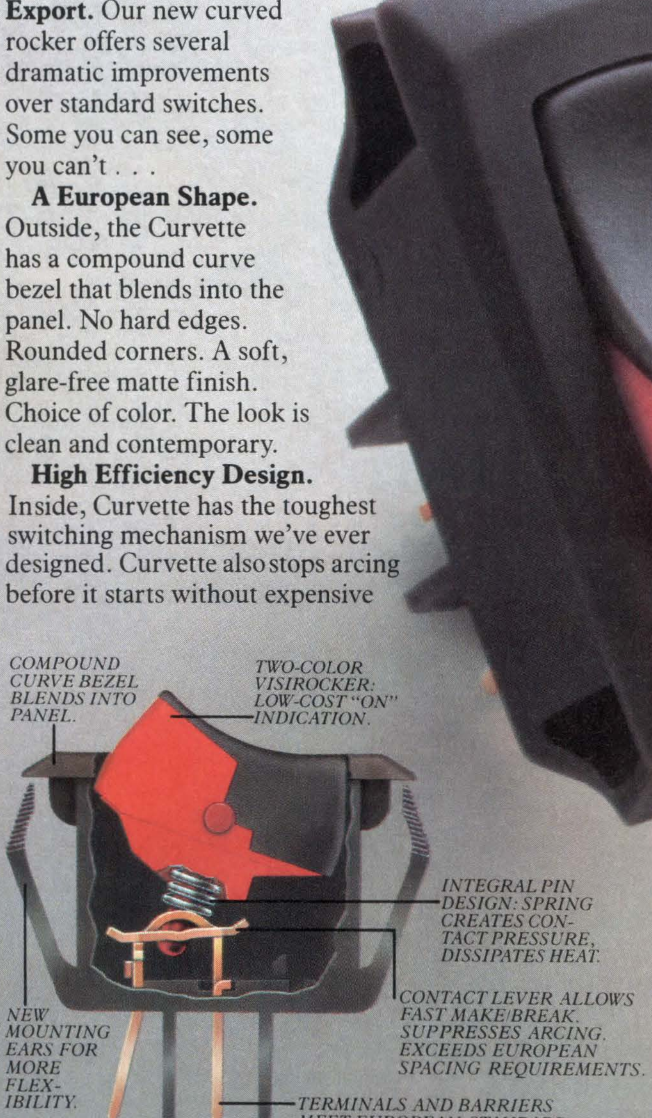

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INNOVATION BY DESIGN

Designer's Guide to Switching Power Supplies Part 1

Regulator IC speeds design of switching power supplies

In part 1 of this 2-part series, you'll learn about simple switching regulators and a technique for stabilizing switching-supply feedback loops. Part 2, scheduled for the November 26th issue, will pick up where this article leaves off and delve into more complex, isolated switching power supplies.

Jim Williams, *Linear Technology Corp*

Switching power supplies are among the most difficult circuits to design. Mysterious operational modes; sudden, seemingly inexplicable failures; peculiar regulation characteristics; and just plain explosions are common occurrences. Diodes conduct the wrong way. Things get hot that shouldn't. Capacitors act like resistors, fuses don't blow, and transistors do. The output is at ground, and the ground terminal shows volts of noise.

In addition, there's the regulator's feedback loop, sampled in nature and replete with uncertain phase shifts. And of course everything varies with line and load conditions. A glance through conference proceedings and available literature yields either an undigestible store of mathematics or absurdly coy and simple little block diagrams that make everything look *so* easy.

Most engineers who need switching supplies don't require 98.2% efficiency or 100W/in^3. They aren't trying to get tenure, and they don't care about inventing a new type of circuit. What they do want are concepts directly applicable to the construction of working circuits that use readily available parts.

Standard parts ease startup

The circuits in this article employ standard, off-the-shelf magnetics exclusively, because most of the problems with switching power supplies center on the inductive components. The standard-magnetics approach almost certainly precludes precisely optimized performance and may horrify some veteran switching-supply designers, but it also eliminates inductor-construction uncertainties, saves time, and greatly increases your chances of getting a design running. A functional circuit is much easier to work with—and get enthusiastic about—than the smoking carcass of a decimated breadboard. Although the characteristics of standard inductors aren't optimal, it's easier to evaluate the performance of a working circuit on an oscilloscope than to guess why you don't see anything at all.

Also, once your circuit is running, you can obtain an optimized version of the standard product from the inductor manufacturer. Generally, the manufacturer can more easily modify its standard product than start from scratch. The process of communicating and translating circuit-performance requirements into inductor-construction details is tricky. Using standard products

Most engineers who want switching supplies don't need 98.2% efficiency or 100W/in³.

as a starting point accelerates the dialogue and minimizes the number of iterations required for satisfactory results. Besides, the standard product will often suffice.

Strictly speaking, it makes more sense to design an inductor to meet circuit requirements than to fashion a circuit around a standard inductor. Deliberately ignoring this point complicated the author's work considerably, but will hopefully simplify the reader's. (**Ref 1** discusses inductor design theory.)

Start with a basic flyback supply

Fig 1 shows a basic flyback supply using the LT1070 switching-regulator IC (see **box,** "Switching supply improves duty-cycle control" for details of the LT1070.) The circuit converts a 5V input to a 12V output. **Fig 2** shows the voltage (trace A) and current (trace B) waveforms at the IC's V_{SW} pin.

The V_{SW} output is the collector of a common-emitter npn transistor and pulls current through the 100-μH inductor. The LT1070's internal oscillator sets the circuit's 40-kHz repetition rate. During the time V_{SW} is low, the current flow through the inductor induces a magnetic field around the inductor. The amount of energy stored in this field is a function of the current level, how long the current flows, and the windings of the inductor and its core material. Control of the duty cycle of the V_{SW}'s base drive forces a constant 12V output.

It's useful to think of the inductor as a bucket and the current flow as water pouring into it. The bucket's capacity—corresponding to the inductor's saturation limitations—sets the ultimate limit on energy storage.

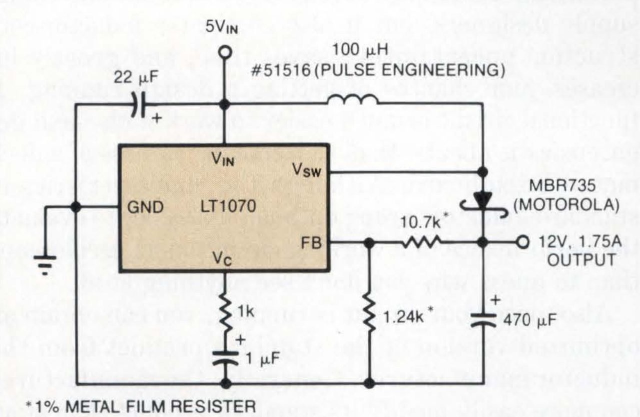
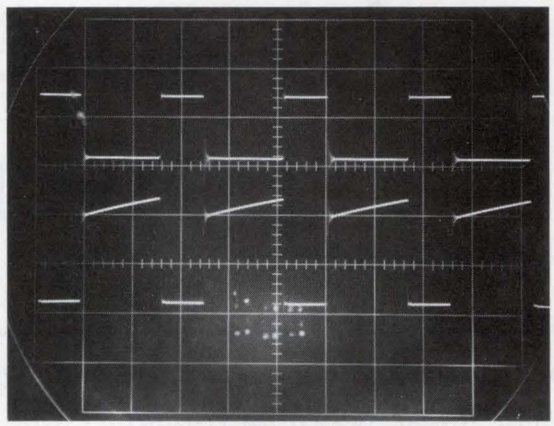


*Fig 1—**This basic flyback supply converts** a 5V input to a 12V output.*

The applied voltage and the inductance of the wire limits the amount of energy that you can put into an inductor in a given time. The core characteristics limit the amount of energy that the inductor can store without saturating.

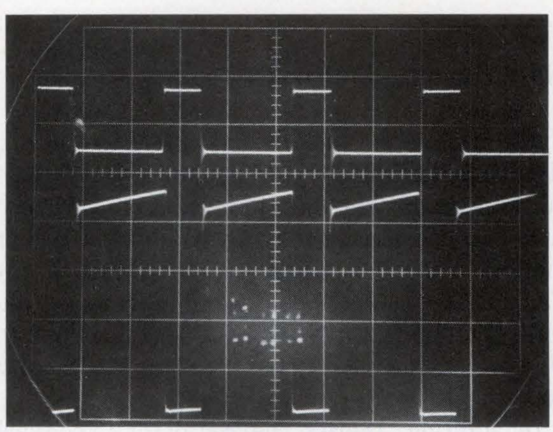
If the inductor is in a feedback loop, such as in **Fig 1,** then changing load demands will control the energy put into the inductor. **Fig 3** shows what happens when the

Text continued on pg 198



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	10 μSEC/DIV
B	1A/DIV	10 μSEC/DIV

*Fig 2—**Trace A is the voltage,** and trace B is the current waveform at the V_{SW} pin of the IC in **Fig 1**.*



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	10 μSEC/DIV
B	1A/DIV	10 μSEC/DIV

*Fig 3—**This photo is the result of the same setup as Fig 2,** but shows what happens when the output demand doubles. In this case, the duty cycle doesn't change appreciably, but current doubles.*

Switching supply improves duty-cycle control

The LT1070 from Linear Technology (Milpitas, CA) is a current-mode switching supply, which means that the switch current, rather than the output voltage, directly controls the switch's duty cycle. The switch **(Fig A)** turns on at the start of each oscillator cycle, and turns off when the switch current reaches a predetermined level. A voltage-sensing error amplifier sets the current-trip level, which thereby controls the output voltage.

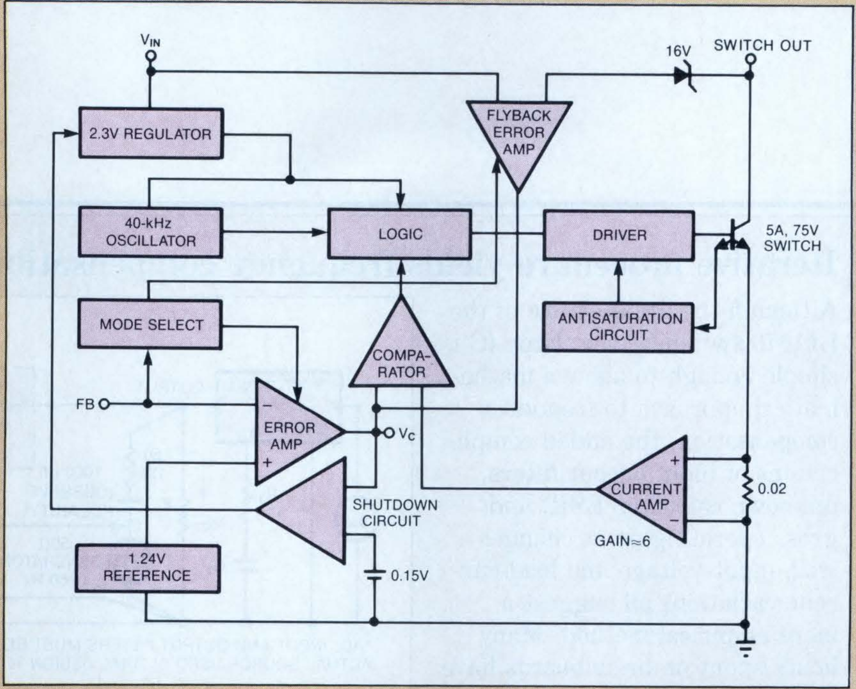


***Fig A—The LT1070 is a current-mode,** switching-regulator IC in which the switch current directly controls the switch's duty cycle.*

This technique has several advantages. First, it responds immediately to input-voltage variations, unlike ordinary switching power supplies, which have notoriously poor line-transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy-storage inductor. This lack of phase shift greatly simplifies closed-loop frequency compensation under widely varying input-voltage or output-load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output-overload or short-circuit conditions.

A low-dropout internal regulator provides a 2.3V supply for all of the LT1070's internal circuitry. The low-dropout design allows the supply voltage to vary from 3 to 6V with virtually no change in device performance. A 40-kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisaturation circuitry detects the onset of saturation in the power switch and instantaneously adjusts driver current to limit switch saturation. This limiting minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The error amplifier's negative input is brought out for output-voltage sensing. This feedback (FB) pin has a second function; when an external resistor pulls it low, it programs the LT1070 to disconnect the main error-amplifier output and connects the output of the flyback amplifier to the comparator's input. The LT1070 then regulates the value of the flyback pulse with respect to the supply voltage.

This flyback pulse is directly proportional to the output voltage in the traditional transformer-coupled, flyback-topology supply. By regulating the amplitude of the flyback pulse, you can regulate the output voltage with no direct connection between input and output. The output is fully floating to the maximum breakdown voltage of the transformer's windings. You can easily obtain multiple floating outputs with additional windings. A delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. The pin (V_C) has four functions. You can use it for frequency compensation, current-limiting adjustment, soft-starting, and total regulator shutdown. During normal regulator operation, the pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current).

The error amplifiers are current-output (g_M) types, so you can externally clamp the V_C pin's voltage to adjust the current limit. Likewise, a capacitor-coupled external clamp provides the soft-start function.

The switch duty cycle goes to zero if the V_C pin gets pulled to ground through a diode, which places the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown—with only 50-μA supply current required for biasing the shutdown circuitry.

Iterative procedure yields frequency compensation

Although the architecture of the LT1070 switching-regulator IC is simple enough to allow a mathematical approach to frequency compensation, the added complications of input/output filters, unknown capacitor ESR, and gross operating-point changes with input-voltage and load-current variations all suggest a more empirical method. Many hours spent on breadboards have shown that the simplest way to optimize the LT1070's frequency compensation is to use transient-response techniques (and resistor and capacitor decade boxes).

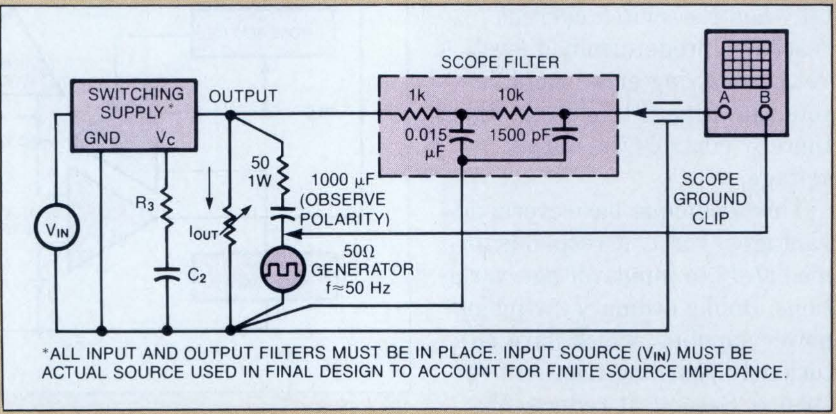


***Fig A—You can use this setup** to couple a load variation into the output of a switching supply and to observe the waveform of the supply's response to the load variation. Typically you set the amplitude of the generator's output to 5V p-p to generate a 100-mA p-p load variation.*

You can inject a transient signal into a switching supply in many ways, but the preferred method is to ac-couple a load variation into the supply's output. This technique avoids the injection-point loading problems that arise if you try to inject a transient into some internal node of the supply, and it is applicable to all switching topologies. The only change necessary may be an amplitude adjustment to maintain small-signal conditions.

Fig A shows a setup using this technique and a function generator with a 50Ω output impedance, coupled through a 50Ω/1000-pF series RC network to the supply's output. The generator frequency is noncritical, but a good starting point is 50 Hz. Lower frequencies can cause an annoying, blinking scope display, and higher frequencies may not allow sufficient settling time for the output transient. Typically you set the amplitude of the generator's output to 5V p-p to generate a 100-mA p-p load variation.

For lightly loaded outputs (I_{OUT}<100 mA), this initial level can prove too high for small-signal response. If the positive- and negative-transition settling waveforms differ from each other significantly, you should reduce the amplitude. The actual amplitude is not particularly important because the shape of the resulting supply-output waveform is what indicates loop stability.

A 2-pole oscilloscope filter (f=10 kHz) blocks the switching frequencies. You need this filter because regulators without additional LC output filters have switching-frequency signals at their outputs, which may have much higher amplitude than the low-frequency settling waveform to be studied. The filter frequency is high enough to pass the settling waveform with no distortion. You should connect the scope and generator exactly as shown in **Fig A** to prevent ground-loop errors. Connecting the channel B probe to the generator, with the ground clip connected to exactly the same place as the channel A ground, synchronizes the oscilloscope.

You shouldn't use the sync output of the generator to synchronize the scope because of ground-loop errors. You may also have to isolate either the generator or the oscilloscope from its third-wire (earth-ground) power-plug connection to prevent ground-loop errors in the scope display. Connecting the channel A probe tip to exactly the same point as the probe's ground clip reveals ground-loop errors; any activity on channel A while it's shorted indicates a ground-loop problem.

Once you've made the proper setup, finding the optimal value for the frequency-compensation network is fairly straightforward. Initially, you make C_2

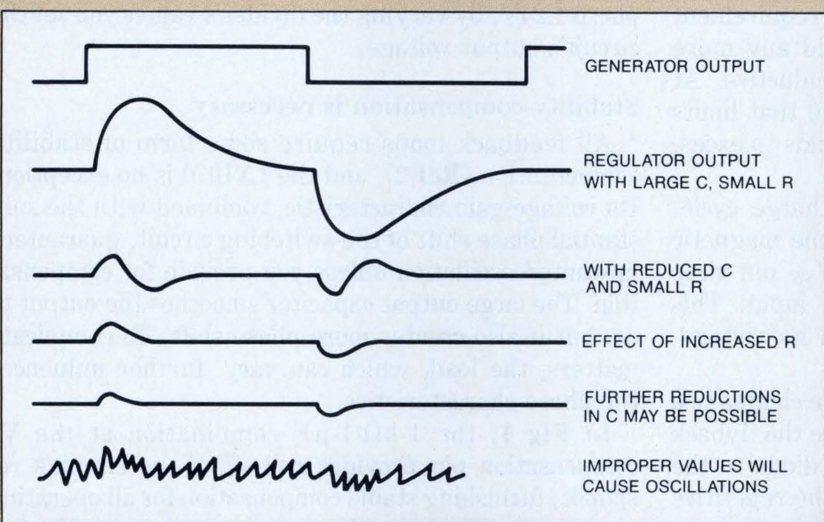


Fig B—Using the setup in Fig A, *you should be able to optimize the compensation-network component values in accordance with the wave shapes shown here.*

binations of input voltage and load current. The simplest way to accomplish this goal is to apply minimum and maximum load currents—and several intermediate load currents. At each load-current level, vary the input voltage from minimum to maximum while observing the settling waveform.

These additional "worst-case" experiments are definitely necessary. Switching supplies, unlike linear supplies, have large shifts in loop gain and phase with changes in operating conditions. If you expect large temperature variations for the supply, you should also make stability checks at the temperature extremes. Significant temperature variations in any of several key component parameters can affect stability—in particular, input and output capacitor values, their ESRs, and inductor permeability.

The LT1070's parametric variations also require some consideration. The error amplifier g_M affects loop stability as does the transfer function of the V_C pin voltage vs switch current (listed as transconductance in the device's data sheet). For modest temperature variations, conservative overdamping under worst-case temperature conditions is usually sufficient to guarantee adequate stability at all temperatures. Note that, if you include external amplifiers or other active devices in the feedback loop, you must include their effects when stabilizing the loop.

large (≥2 μF), and R_3 small (~1 kΩ). This compensation nearly always ensures that the supply will be stable enough to begin working.

Next, if the supply's output waveform is overdamped (see the waveforms in **Fig B**), you reduce the value of C_2 in steps of about 2:1 until the response becomes slightly underdamped. Next, you increase R_3 in steps of 2:1 to introduce a loop zero. This zero will normally improve damping and allow you to reduce the value of C_2 further. Shifting back and forth between R_3 and C_2 variations will allow you to quickly find the optimal values for these components.

If the supply's response is underdamped with the initial large value of C_2, you should increase R_3 immediately and try larger values for C_2. Increasing R_3 will normally bring about the overdamped starting condition for further iterations.

Just what do "optimal values" for R_3 and C_2 really mean? Normally they mean the smallest value for C_2 and the largest value for R_3 that will still guarantee no loop oscillations and that will result in loop settling that is as rapid as possible. The reason behind this criterion is that it minimizes the variations in output voltage due to input-ripple voltages and output-load transients.

A switching supply that is grossly overdamped will never oscillate, but it may have unacceptably large output transients following sudden changes in input voltage or output loading. It can also suffer from excessive overshoot problems during start-up or short-circuit recovery.

To guarantee acceptable loop stability under all conditions, you should check the final values chosen for R_3 and C_2 for all com-

The circuits employ a switching-regulator IC and only standard, off-the-shelf magnetics.

output demand doubles. In this case, the duty cycle doesn't change much, but current doubles.

This current doubling requires the inductor to store more energy. If it can't meet the storage requirement —that is, if it saturates and cannot hold any more magnetic flux—then it will cease to be inductive. At this point, the resistance of the wire is all that limits current flow. The current then rapidly builds to excessive and destructive values.

At the end of each inductor current-charge cycle, current flow in the inductor ceases, and the magnetic field around it abruptly collapses. The V_{SW} pin rises rapidly to a voltage higher than the 5V input. This "flyback" action gives the regulator both its voltage-boost characteristics and its name.

In this circuit, the flyback pulse's voltage clamps to a level just above the output voltage, because the flyback pulse gets steered through the Schottky diode to the output. The 470-μF capacitor integrates the repetitive flyback pulses, providing the circuit's dc output.

The feedback pin (FB) samples this output via the 10.7-kΩ/1.24-kΩ divider. The LT1070 compares the feedback-pin voltage to its internal 1.24V reference and controls the V_{SW} pin's duty cycle, closing the feedback loop. Because the LT1070 is trying to force its feedback pin to 1.24V, by varying the divider's values you set the circuit's output voltage.

Stability compensation is necessary

All feedback loops require some form of stability compensation (**Ref 2**), and the LT1070 is no exception. Its voltage-gain characteristic, combined with the substantial phase shift of the switching circuit, guarantees unwanted oscillation unless you provide for compensation. The large output capacitor smoothes the output to dc, but it also creates more phase shift. To complicate matters, the load, which can vary, further influences the phase characteristics.

In **Fig 1**, the 1-kΩ/1-μF combination at the V_C compensation pin provides roll-off of the circuit's response, furnishing stable compensation for all operating conditions. (See **box**, "Iterative procedure yields frequency compensation" for details and suggestions for achieving stability in switching-regulator loops.)

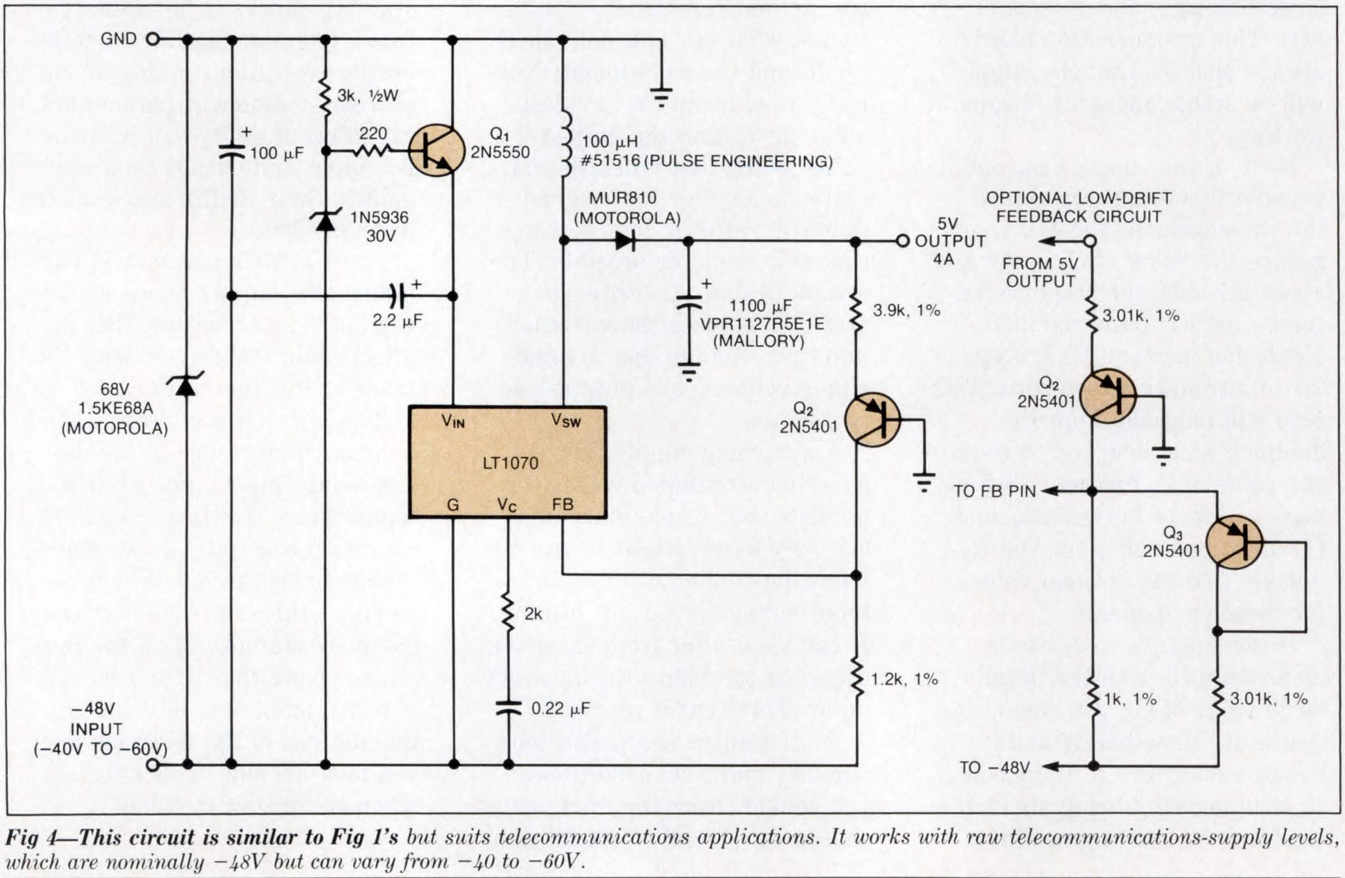


Fig 4—This circuit is similar to Fig 1's *but suits telecommunications applications. It works with raw telecommunications-supply levels, which are nominally −48V but can vary from −40 to −60V.*

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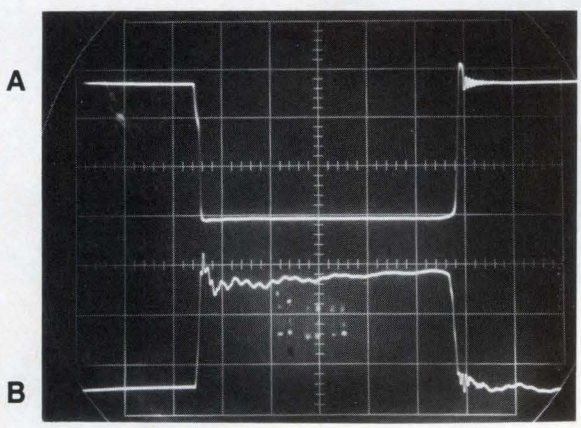
The majority of the problems you'll encounter with switching supplies involves their inductive components.

As innocent as **Fig 1** appears, odd and seemingly inexplicable problems will arise. Note that the ground connection appears at the ground pin, as opposed to its normal location at the bottom of the diagram. This unconventional location is deliberate because you must make the supply- and load-return connections at the GND pin. You musn't allow the high-speed, high-current returns from the output transistor's emitter (the "other end" of the V_{SW} pin) to mix with the small currents of the output divider or the V_C pin. Such mixing can promote poor regulation, unstable operation, or outright oscillation.

The 22-μF bypass capacitor ensures clean local power for the LT1070, even during the fast, high-current drain periods when V_{SW} turns on. The bypass capacitor should have good high-frequency characteristics (a tantalum or aluminum type, for example, paralleled by a disc-ceramic type).

Flyback supply for telecommunications

Fig 4's circuit is operationally similar to **Fig 1**'s, but is suitable for telecommunications applications. A raw telecommunications supply is nominally −48V, but can vary from −40 to −60V. Although the chip's V_{SW} pin can handle this voltage range, the V_{IN} pin requires protection (V_{MAX}=60V). Q_1 and the 30V zener diode serve this purpose, dropping the input voltage to about −17V at the V_{IN} pin under all line conditions.



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	500 nSEC/DIV
B	2A/DIV	500 nSEC/DIV

Fig 5—Trace A is the voltage, *and trace B is the current at the V_{SW} pin of the circuit in* ***Fig 4****. The ripples in the current trace are due to a nonoptimal breadboard layout. Inductor ringing during turn-off (trace A) is characteristic of flyback configurations.*

Here, the "top" of the inductor is at ground, and the ground pin is at −48V. The feedback pin senses with respect to the ground pin, so the circuit needs a level shift from the 5V output. Q_2 accomplishes this function and introduces only −2-mV/°C drift. This drift is normally not objectionable in a logic power supply, but you can compensate for it with an appropriately scaled diode-resistor combination across the 1.2-kΩ resistor.

Frequency compensation is similar to that of **Fig 1.** Note that a low ESR (equivalent series resistance) capacitor provides less phase shift, permitting faster loop response because of a reduced compensation time constant. The 68V zener diode clamps and absorbs excessive line transients that might otherwise damage the LT1070 (V_{SW} is 75V max).

Fig 5 shows operation waveforms for **Fig 4**'s V_{SW} pin. Trace A is the voltage, and trace B is the current. Switching characteristics are fast and clean. The ripples in the current trace are due to nonoptimal breadboard layout (ground as I say, not as I do). Inductor ringing during turn-off (trace A) is characteristic of flyback configurations. **EDN**

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

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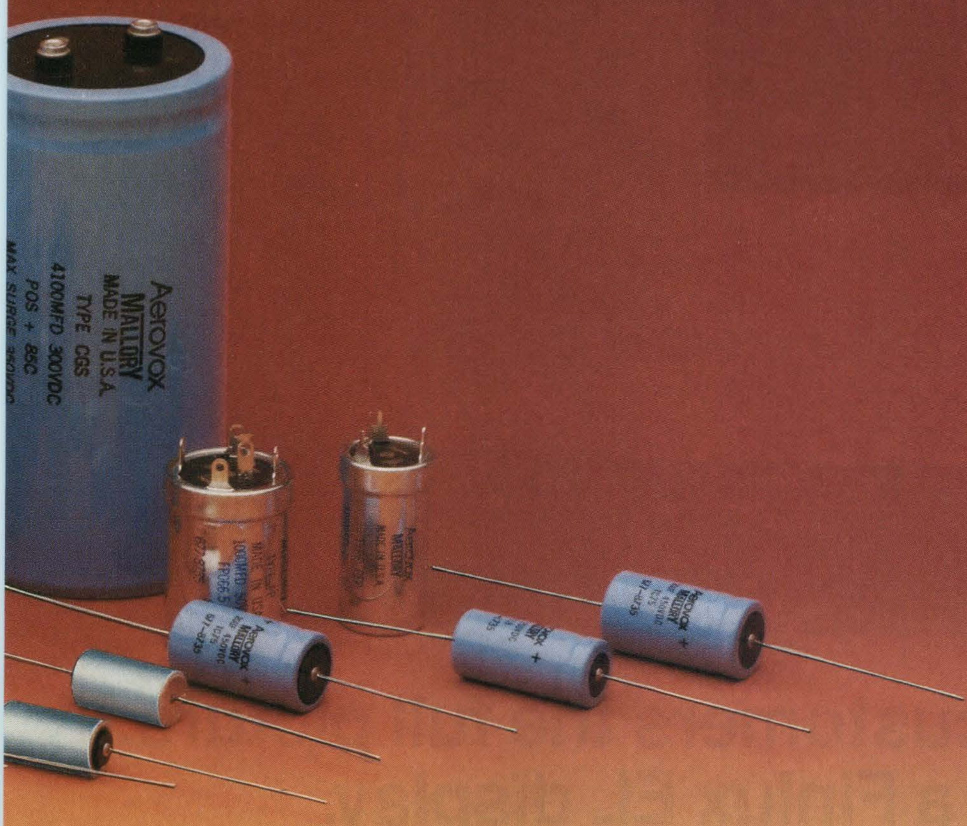

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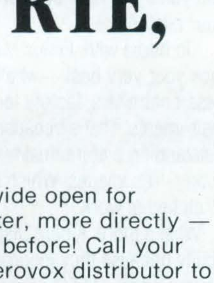

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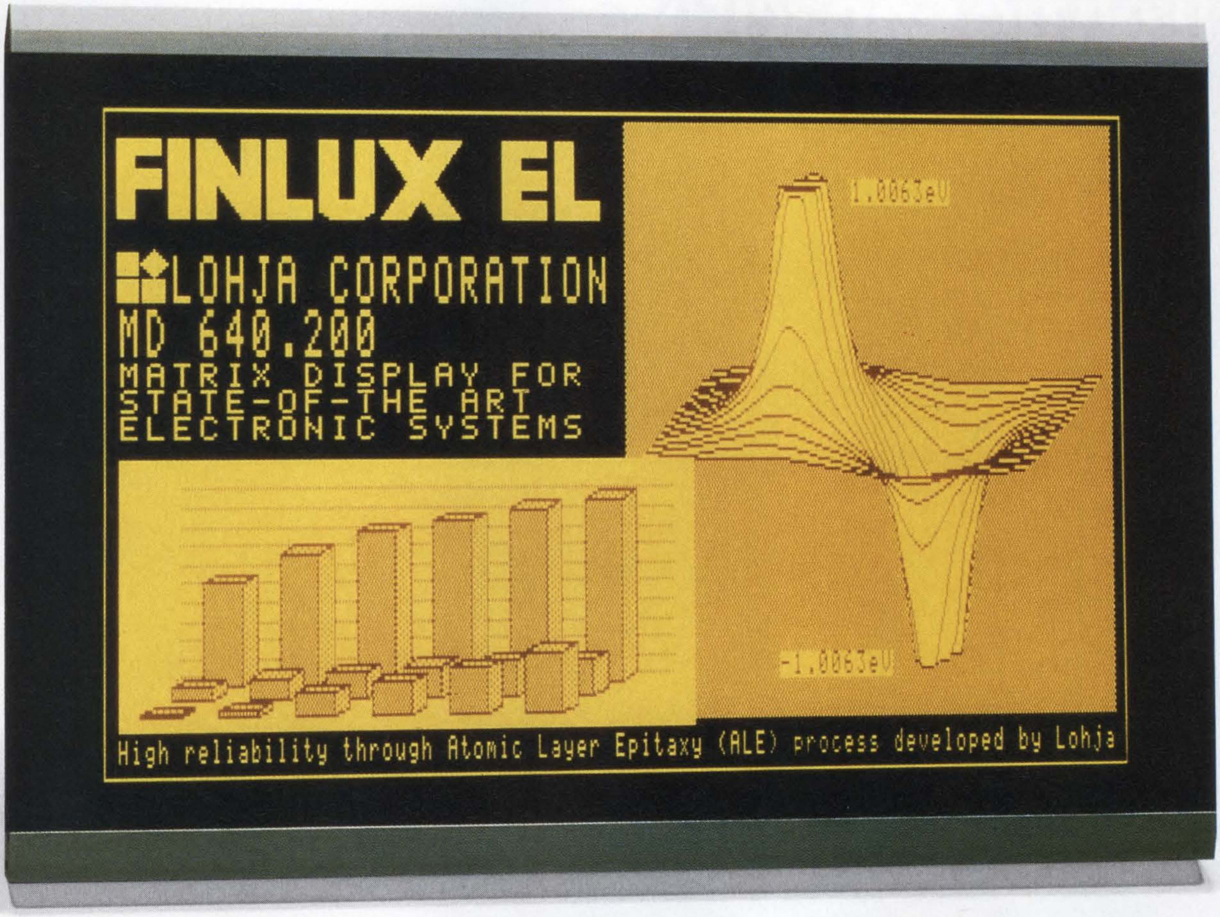

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Interface a real-time clock chip to the IBM PC or Apple II

Modern real-time clock (RTC) chips are sophisticated, highly stable devices that require very few external components. RTC chips are easy to use, but to obtain their highest accuracy you must take care both in board layout and in your choice of a timebase crystal.

Adnan Khan, *GE Solid State* and
Mark Alexander, *GE/Intersil*

Real-time clock (RTC) chips have evolved from expensive, no-frills, power-hungry timekeepers into inexpensive, sophisticated, low-power coprocessors that provide many more capabilities than just basic timekeeping. Most personal computers now include a clock chip that automatically updates the system's real-time clock/calendar and can start any system or application program at specific times, which can be hours, days, or months apart. You don't need many components to interface a modern RTC chip to other devices or to a host computer such as an IBM PC or an Apple II. However, you'll need to select these components carefully to obtain the best frequency and temperature stability and to ensure that the clock chip switches reliably between the main power supply and the backup battery.

The combination of an RTC chip and an 8-bit microcontroller (**Fig 1**) illustrates most of the capabilities of a modern RTC and shows the design aspects that need the most attention. The circuit depicts a world-time alarm clock that can display the time for any zone and can switch to and from daylight-savings time. You could implement a real-time process controller with this circuit by using one of the I/O ports on the μC to drive an alarm buzzer, a relay, a solenoid valve, or a triac.

The areas of this circuit that prove most troublesome to design are the oscillator circuitry, the battery-backup scheme, and the layout of the pc board on which you mount the clock chip. The ICM7170 used in **Fig 1**'s circuit is typical of many other available clock chips in these respects. (For additional information on the chip, see **box**, "The ICM7170 real-time clock," pg 212).

In **Fig 1**'s circuit, the oscillator's frequency stability determines both the long- and short-term accuracy of the clock, and depends primarily on the phase-changing properties of the feedback network. For high stability, you'd generally use a quartz crystal or a tuning-fork-type crystal as the feedback element, but to select the right crystal you need some understanding of the oscillator. Some modern RTCs let you choose among several frequencies for the crystal, but most chips use a 32.768-kHz tuning-fork-type crystal as the timebase generator. These crystals have the advantage of being very inexpensive—but they do present some tradeoffs.

A modern RTC chip with the proper crystal can keep accurate time to within 0.5 sec/month over a wide temperature range.

First, because oscillator current rises as the series resistance of the feedback network increases, it's good design practice to select a crystal that has a low series resistance. Unfortunately, the tuning-fork crystals have a rather high series resistance—typically around 45 kΩ. Further, tuning-fork crystals have a rather poor temperature/frequency curve **(Fig 2a)**. Their frequency drift with temperature is typically −0.038 ppm/°C, and mechanical vibration can also cause considerable frequency drift. Thus, the tuning-fork crystals are best suited to those applications in which the equipment experiences only minor temperature changes and little mechanical shock or vibration.

If the RTC in your design will be exposed to a wide range of temperatures, you'll need to use an AT- or SC-cut crystal. When used at frequencies over 1 MHz,

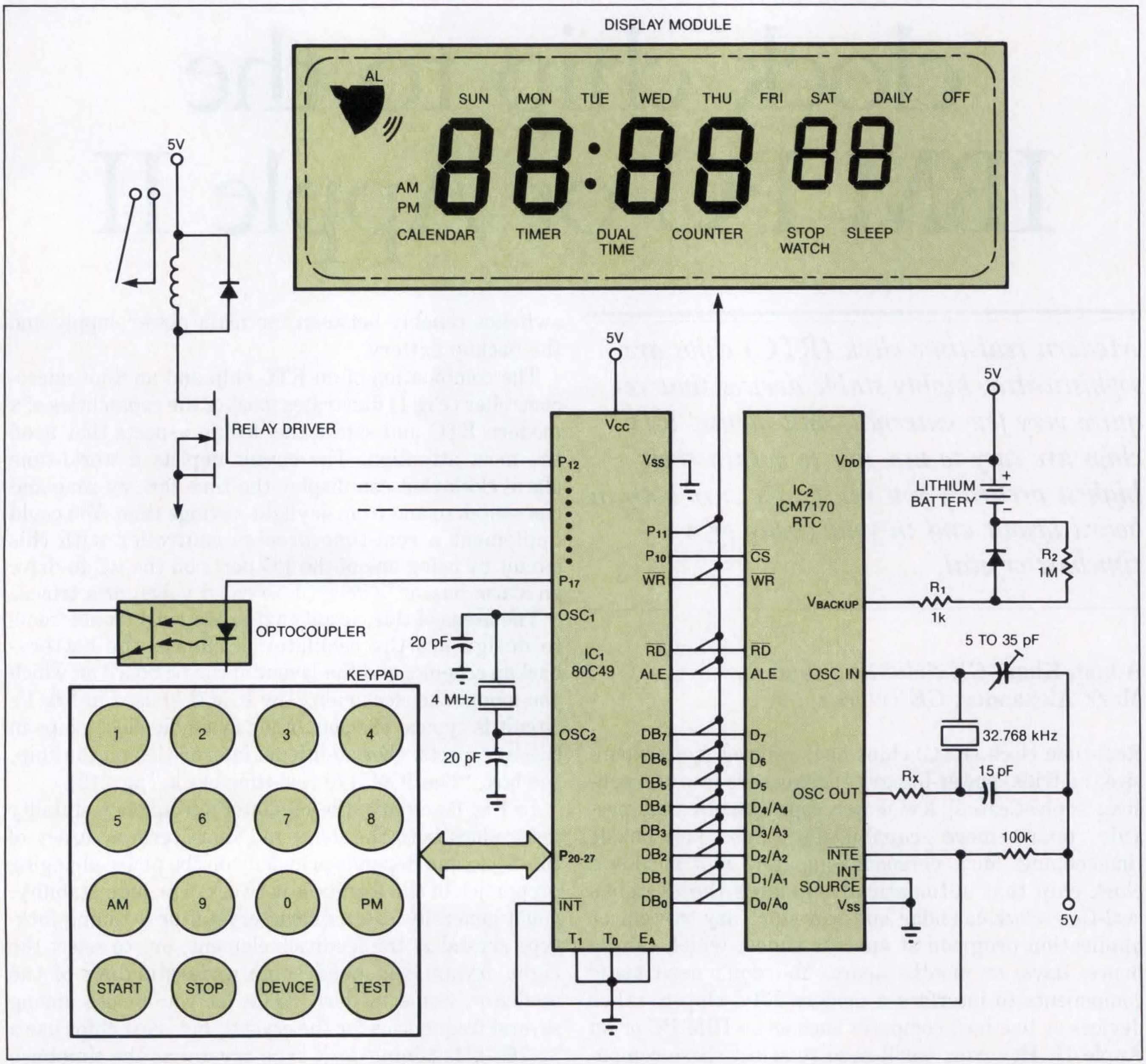
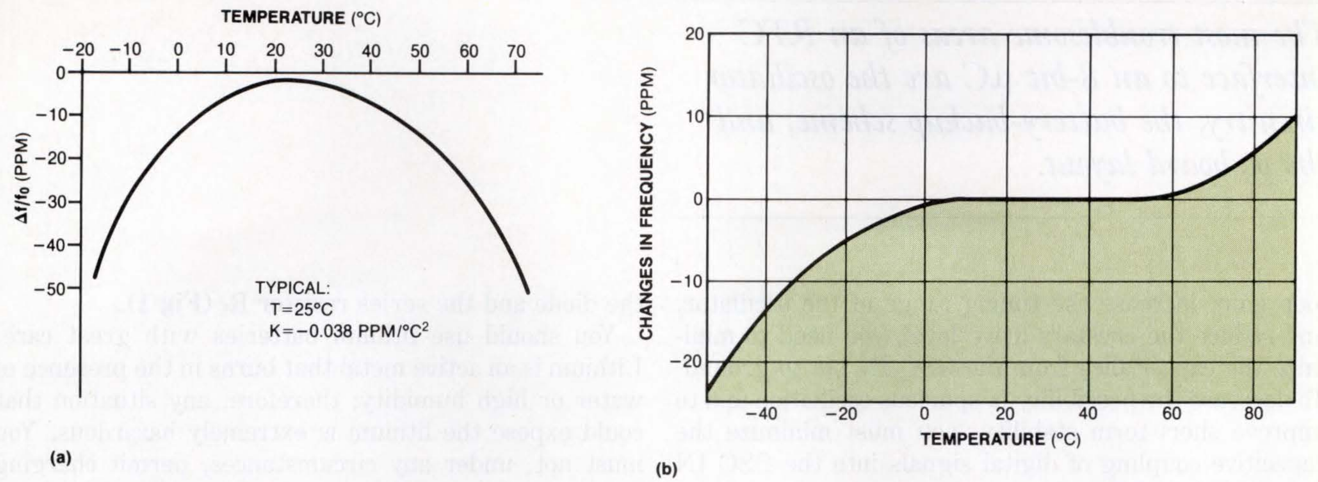
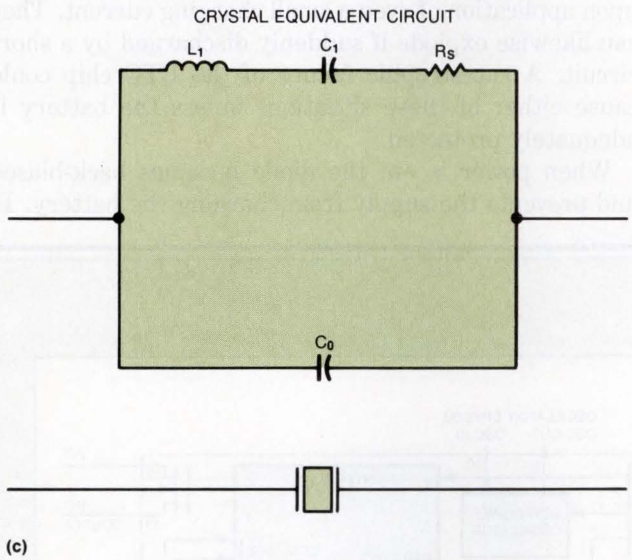


Fig 1—You can combine a modern real-time clock chip with an 8-bit μC *to implement a universal timer/process controller. You can use ports $P_{12\text{-}17}$ of the μC to drive a variety of alarms and peripheral devices.*





f_{OSC}	4.194304 MHz	1.048576 MHz	32.768 kHz
R_S (MAX)	75Ω	700Ω	50 kΩ
C_0 (MAX)	7 pF	5 pF	17 pF
C_1	0.012 pF	0.008 pF	0.003 pF
Q	50k	35k	30k

Fig 2—It's important to choose the right crystal for an RTC timebase. *Wide variations of temperature cause the frequency of a tuning-fork-type crystal to drift **(a)**. An SC-cut crystal is stable over a much wider temperature range **(b)**. The characteristics of various crystal types are shown in **(c)**.*

these crystals are rugged and have excellent temperature stability. An SC-cut, third-overtone-type crystal will have a temperature coefficient of less than 1×10^{-7}/°C on each side of the turnover temperature **(Fig 2b)**. A crystal of this type, with a frequency of 4.194304 MHz, will admirably suit an RTC circuit and, after a few months at a constant temperature, will exhibit an aging rate of only one part in 10^7 per month, or less.

Almost every currently available RTC chip uses a Pierce oscillator as its internal timebase generator. Pierce oscillators typically draw 1 to 80 μA, and they're convenient because you can easily fine-tune their frequency with a trimmer capacitor, and because their oscillation stops (rather than going wild) in the event of a crystal failure.

Although most crystals are capable of dissipating as much as 150 μW, it's considered good design practice to limit the drive to the crystal to 75 μW. For an overtone crystal, you should limit the drive even further, to about 30 μW. It's also good practice to limit the drive to a 32.768-kHz tuning-fork crystal by inserting a series resistor of 200 to 300 kΩ (R_X, **Fig 1**). Most clock oscillators operate from a supply of 3 to 5V, and because crystals of this type have a high internal series resistance, the oscillator current can easily rise to a value that will damage the crystal.

To obtain optimum performance from a Pierce oscillator, you should lay out the circuit board very carefully. In general, you should treat the oscillator as a high-frequency circuit, and use the standard techniques of avoiding parallel and long traces: That is, you should use ground traces between signal traces to reduce cross-coupling, and you should keep components well separated to avoid coupling between component bodies.

The following points are especially important. To increase loop gain, reduce start-up time, and increase short-term stability, you must minimize the capacitance across the traces that run between the crystal and the OSC IN and OSC OUT pins of the RTC. To increase

The most troublesome areas of an RTC interface to an 8-bit µC are the oscillator circuitry, the battery-backup scheme, and the pc-board layout.

loop gain, increase the tuning range of the oscillator, and reduce the crystal's drive level, you need to minimize the capacitance from the OSC IN pin to ground. To decrease the possibility of spurious oscillation and to improve short-term stability, you must minimize the capacitive coupling of digital signals into the OSC IN terminal of the RTC. Finally, if you use a crystal series resistor, you must isolate it to reduce parasitic charges flowing into the oscillator input circuit.

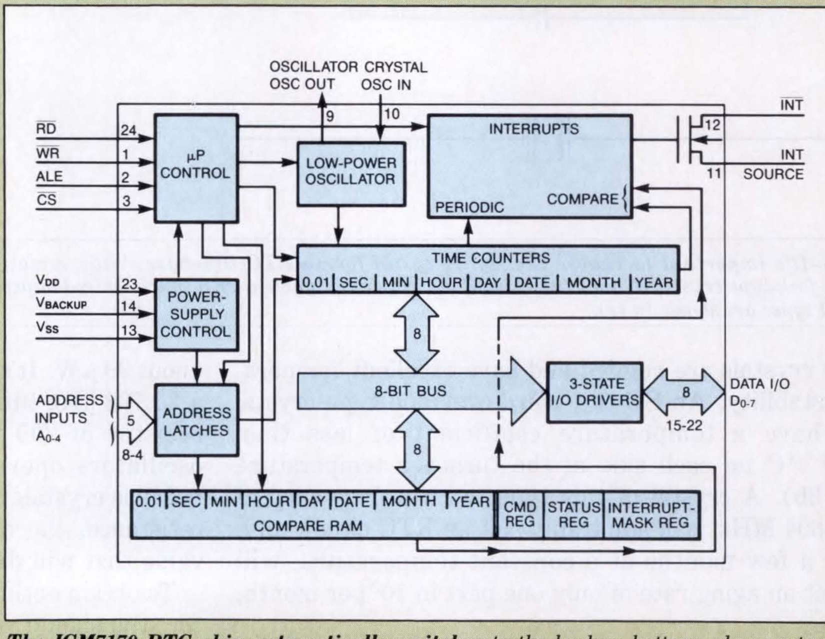
RTC chips vary as to the battery-backup circuits they require. The ICM7170 requires only three external components: a 3V lithium battery, a diode, and a resistor. For temporary operation, the battery alone would be sufficient, but to meet UL safety requirements, you must protect the lithium battery by adding the diode and the series resistor R_1 **(Fig 1)**.

You should use lithium batteries with great care. Lithium is an active metal that burns in the presence of water or high humidity; therefore, any situation that could expose the lithium is extremely hazardous. You must not, under any circumstances, permit charging current to flow into the battery—lithium batteries have been known to explode or release dangerous materials upon application of even a small charging current. They can likewise explode if suddenly discharged by a short circuit. A catastrophic failure of the RTC chip could cause either of these situations unless the battery is adequately protected.

When power is on, the diode becomes back-biased and prevents the supply from charging the battery. In

The ICM7170 real-time clock

The ICM7170 real-time clock (RTC) from Intersil is a µP-compatible peripheral chip fabricated in a 4-µm, P-well, silicon-gate CMOS process. The chip uses an 8-bit bidirectional bus for I/O operations, and it provides time and date data in binary format, which reduces the amount of software processing that the host system must perform. The RTC has a built-in data latch, and its access time is short; valid data appears on the I/O pins no more than 250 nsec after the falling edge of the $\overline{RD}$ strobe.



***The ICM7170 RTC chip automatically switches** to the backup battery when system power is turned off. The RTC can generate periodic interrupts as well as an alarm interrupt.*

The internal data latch is extremely important, because it eliminates the possibility of reading invalid time data. (This possibility is always present in RTCs that don't have a data latch.) When the CPU reads the 1/100-sec latch, the RTC strobes data from all the counters into the other sections of the latch and holds it there indefinitely until the CPU again reads the 1/100-sec latch. If the RTC time-base generator tries to update the 1/100-sec counter during the read operation, the 100-Hz clock transition is delayed until the read operation is terminated, when the update can propagate through the counters without affecting the data read by the CPU.

The ICM7170 keeps track of time intervals ranging from 1/100 sec to several years. It records hours in either 12- or 24-hour format; you can change from one the event that the RTC chip breaks down and creates a short circuit, the resistor will limit the discharge current to a safe value. In some circumstances you may need to connect a second resistor (R_2) across the diode. This resistor, which should have a value of 1 to 2 MΩ, will provide sufficient leakage current for the RTC chip to overcome any leakage over the board from the V_{SS} trace to the V_{BACKUP} trace and pin.

It's easy to create a clock board that will plug into an expansion slot of an IBM PC or compatible computer. You can mount the components on a blank prototyping board and wire-wrap the connections. The associated software could be merely a simple routine that polls the clock and reads the time into a RAM buffer; alternatively, it could be an interrupt-service routine that is periodically triggered by the RTC's 1-sec interrupt-request line.

Fig 3 shows the interface circuit. You'll need only four logic chips and a few resistor packs to implement the support circuitry. With any RTC chip, however, you should use only chips in the 74HCT or 74LS families, whose outputs have slow rise and fall times. Chips of the 74S, 74AC, and 74F families have very fast rise and fall times that produce EMI noise and ground bounce, and may cause spurious operation of the RTC.

IC_1 is an address comparator that compares the setting of DIP switches S_{1-4} with the address presented on lines A_{5-8} to determine the base port address of the clock board. Address lines A_{0-4} are buffered by IC_2, the bidirectional data lines are buffered by IC_5, and IC_4

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format to the other at any time without affecting the integrity of the hours data. The calendar section provides data for the day of the week, date, month, and year. All the counters are separately addressable, and you set or read their contents by enabling each in turn. Although complete date and time data occupies eight bytes, only 43 of the 64 bits are needed to represent all possible valid date/time values. The RTC holds the unused bits at logical zero during a read operation and ignores them during a write operation.

The RTC also contains eight additional registers that hold alarm data. An internal comparator compares the data you preset into the alarm registers with the current values in the real-time registers. When the comparator detects an exact match, it generates an interrupt request. You can program the alarm circuits to generate periodic interrupt requests at intervals ranging from $\frac{1}{100}$ sec to years, or you can program it to generate an alarm at a specific time.

The timebase generator is a Pierce crystal oscillator equipped with an active feedback resistor and a voltage regulator. The regulator output is typically 1.8V for 32-kHz operation. This low voltage yields several advantages: First, the change in the oscillator's output voltage is negligible for variations in V_{CC} from 2.0 to 5.0V; second, switching from system power to backup power (or vice versa) does not compromise the oscillator's stability; third, the backup-battery voltage can be as low as 1.9V; and fourth, there's no danger of overdriving the crystal, whether the chip is operating from system power or from backup power. You can use crystal frequencies of 32.768 kHz, 1.048576 MHz, 2.097152 MHz, or 4.194304 MHz. If you use a 32.768-kHz crystal that does not have a high Q factor, you may not have to use a series resistor.

The RTC's built-in automatic battery-switchover circuit allows you to operate the chip in backup mode merely by adding an external battery, such as a CR2325 lithium/manganese dioxide battery. However, for safety's sake, when you use a lithium battery you should always place a diode and a limiting resistor in series with it. The switchover circuit switches the ICM7170's internal ground bus from the V_{SS} pin to the V_{BACKUP} pin whenever the system's power-supply voltage drops below that of the battery. On standby power, the chip draws only 2 μA when operating with a 32.768-kHz crystal, and you'll get approximately 40,000 hours (4½ years) of operation from an 80-mAhr lithium battery. Whenever the voltage from the V_{SS} pin to the V_{BACKUP} pin drops below 1.0V, the internal logic disables all I/O operations, thereby providing additional protection for the counter data during power-supply transitions.

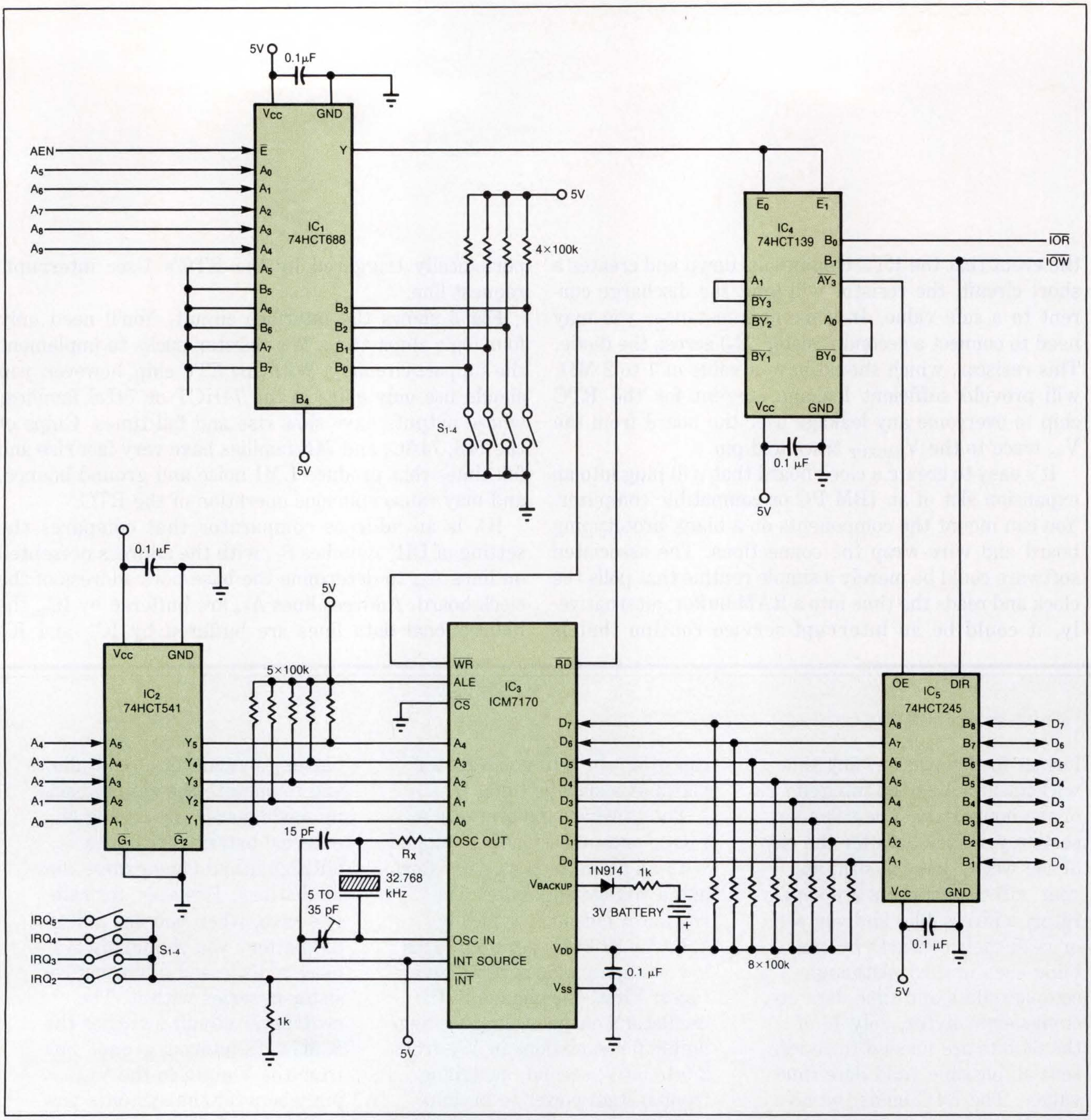


*Fig 3—**You need only four 74HCT support chips** and a few discrete parts to construct an interface between the ICM7170 RTC chip and an IBM PC. Buffers isolate the RTC from the PC bus except during I/O operations specifically addressed to the RTC.*

generates the control signals that the RTC requires. It may seem unusual to decode the PC's $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ lines to generate the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals needed by the RTC and to control bidirectional bus transceiver IC_5, but there's a good reason for doing so. If a bus fault or a PC malfunction should ever drive $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ low simultaneously, the decoder will not respond; therefore, the malfunction won't cause the RTC to perform unwanted or erroneous operations. The data transceiver is enabled only by valid I/O operations addressed to the clock board.

Another slightly unusual feature of **Fig 3**'s circuit is that the $\overline{\text{CS}}$ line of the RTC is permanently grounded to enable the chip. This procedure reduces the chip's active power consumption. The procedure is permissible because the $\overline{\text{CS}}$ signal is internally OR-combined with the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals to generate the internal read and write strobes.

The PC's interrupt controller requires an active-high signal, whereas the $\overline{\text{INT}}$ output of the RTC is active-low; you can obtain an interrupt-request signal of the correct polarity by using the internal output transistor of the interrupt generator as a source follower, and by connecting an external pulldown resistor to the $\overline{\text{INT}}$ line. **Fig 3** shows the connections that achieve this configuration and yield an interrupt request of the correct polarity for the PC.

The battery-backup circuit is extremely simple. In its

The oscillator circuit and board layout can affect the accuracy and stability of a real-time clock.

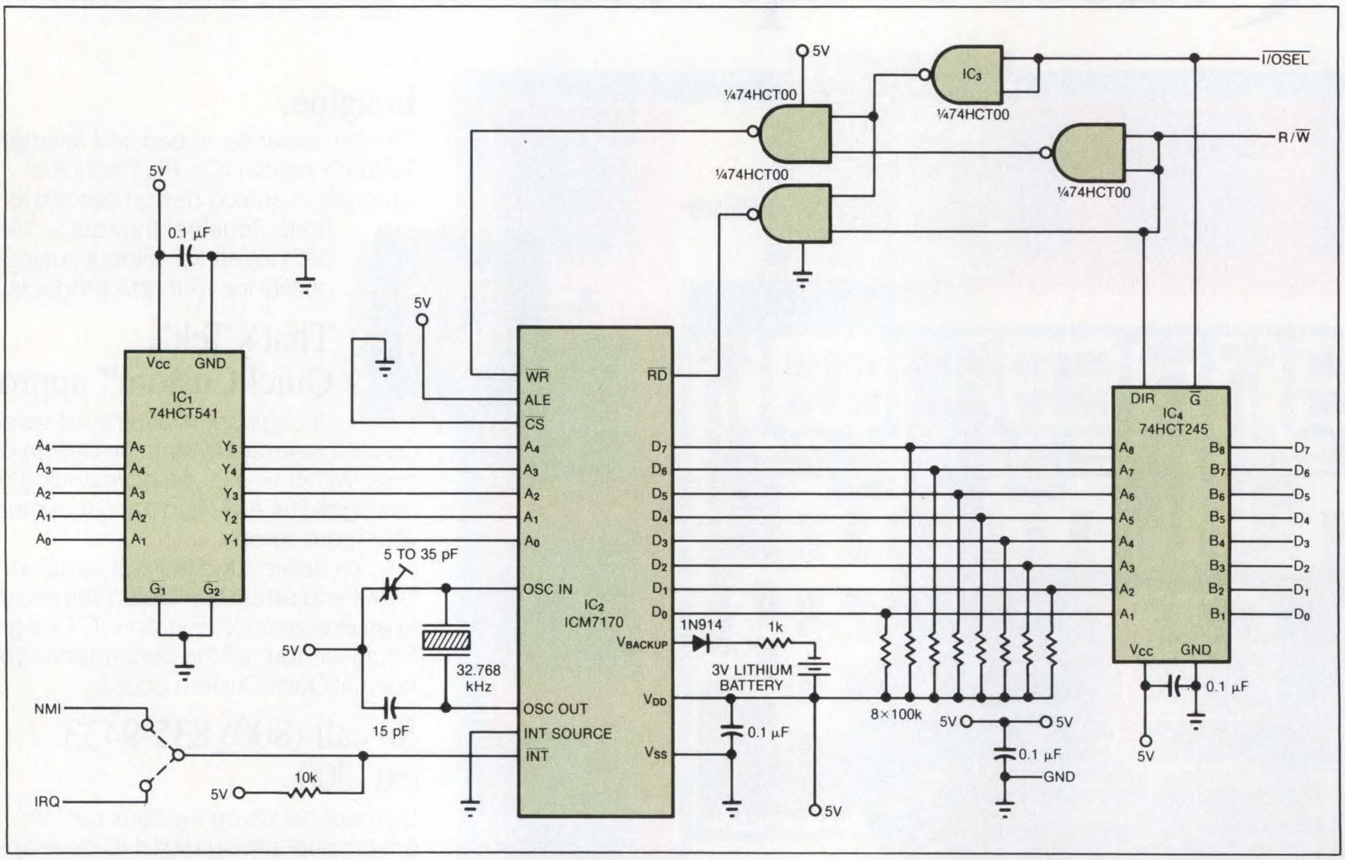


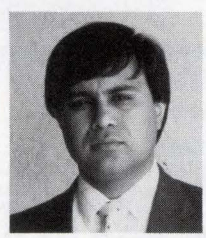
***Fig 4—Interfacing an RTC to an Apple II is extremely simple** because Apple expansion slots have unique base addresses; you don't need to perform any address decoding.*

simplest form, it needs only an external battery. If you select a lithium battery, however, you should add a protective diode and resistor in series with the battery to meet UL safety requirements. A CR2325-type battery will provide approximately 10 years of service in backup mode.

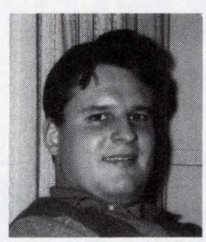
Fig 4 shows a very simple RTC interface for Apple II machines. The Apple II computers are very different from the IBM PC family in that each expansion slot has a fixed, unique base address. Thus, it's not necessary to decode the upper address lines, because the decoding is done for you on the mother board.

As in the IBM PC interface, the $\overline{\text{CS}}$ line is permanently grounded to enable the RTC. However, the RTC's $\overline{\text{RD}}$ and $\overline{\text{WR}}$ lines are gated not only with the R/$\overline{\text{W}}$ bus signal, which selects either a read or a write operation, but also with the $\overline{\text{I/OSEL}}$ bus signal. This arrangement provides approximately 250 nsec of setup time between the time at which the address lines become stable and the falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$, which initiates the operation. **EDN**

Authors' biographies



Adnan S Khan is a field application engineer at GE's Solid State Sales Div (Santa Ana, CA). He holds a BSET degree from Northrop University and is a member of the IEEE. In his spare time, Adnan enjoys music, model aircraft, and operating a ham radio station (N6HSI).



Mark Alexander was employed at GE/Intersil in Cupertino, CA, when he coauthored this article. He currently works as an analog-circuit-design engineer at Attain Inc (Milpitas, CA). He holds a BSEE from the University of Toronto, Canada. In his spare time, he enjoys designing and constructing audio equipment, cooking, and skiing both on water and on snow.

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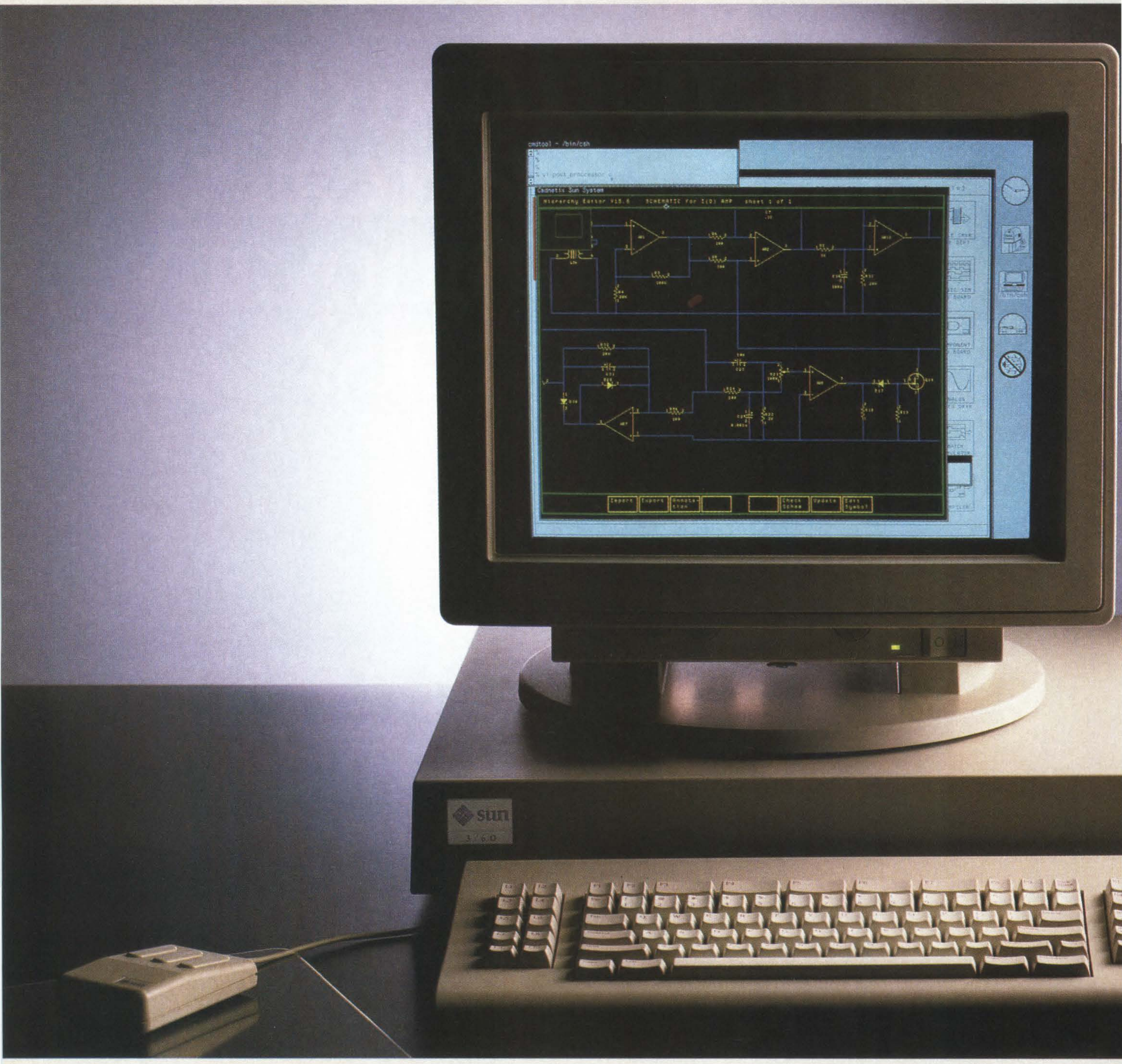

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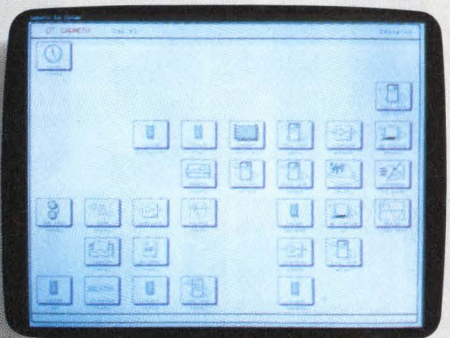

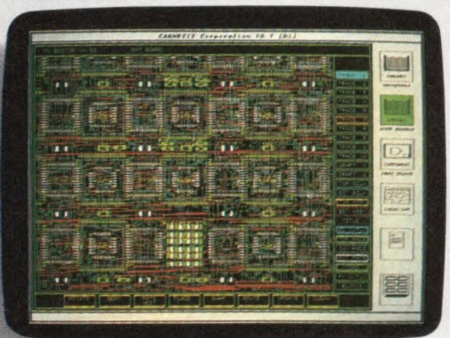

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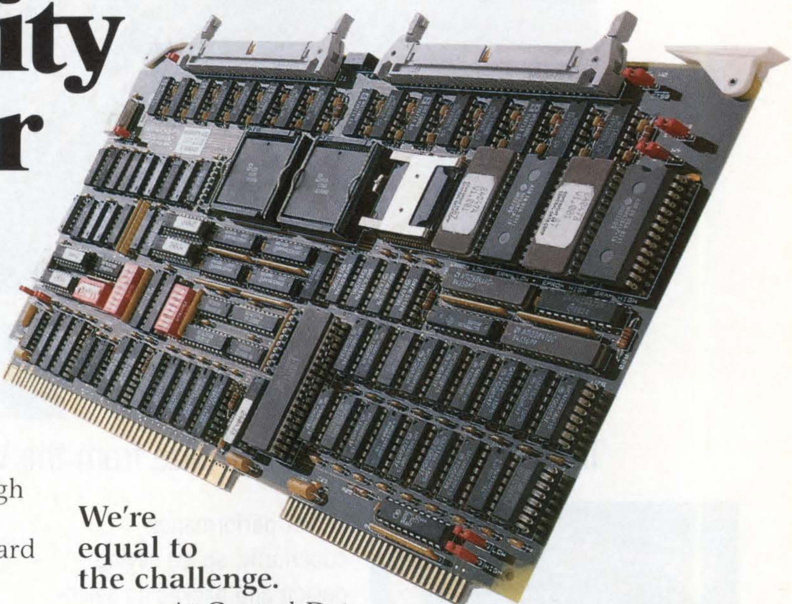

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CD-player design requires an accurate 16-bit D/A converter

You can greatly simplify the design of a compact-disk player by using a high-speed, serial input DAC that has low noise and low harmonic distortion. The high-speed feature permits you to use oversampling techniques in your system; the serial-input capability improves the CD player's reliability.

Frederick J Highton, *Burr-Brown Corp*

To process the digital output of a compact disk (CD), a CD player requires a D/A converter that has low noise, low harmonic distortion, and high conversion speed. A DAC that operates at high speed allows for oversampling of the digital stream and greatly eases your circuit-design requirements. You can also simplify your CD-player design if that high-speed DAC also accepts serial input.

Compact-disk recorders employ linear pulse-code-modulation (PCM) techniques to sample the audio signal at a rate of 44.1 kHz and store the resulting output on a CD as a 16-bit word. A 16-bit resolution is equivalent to a signal-to-noise ratio of 98 dB—a performance that is all but impossible for conventional record or tape players.

When a disk is played back, the player retrieves from the disk the digital words that represent the audio content. The CD player checks the words, corrects any errors in them, and assembles them into a serial data stream that represents the alternate left- and right-channel signals.

Many systems demultiplex the information into 16-bit parallel outputs that correspond to a particular left- or right-channel sample. The 16 bits representing the analog amplitude of the sample are simultaneously fed into a DAC, which transforms the digital word into an output-voltage level. Thus, the DAC is the heart of the signal-reproduction process and the key element in determining sound quality. All the care taken in the original recording, and any error correction, is wasted if the DAC does not faithfully reconstruct the original sound signal. To design a good compact-disk player, therefore, you must use an accurate 16-bit monolithic DAC.

In a CD player, the digital information stream extracted from the disk combines alternate left- and right-channel samples. If you're designing a lower-end system, you'll probably choose to multiplex the DAC between channels. In such a design, the DAC must respond fast enough to provide two clean outputs during one sampling period. The DAC's output is multiplexed by an external switching circuit; the output then goes through a deglitching circuit between the left- and right-channel filters.

Fig 1 shows the interface circuitry you need to

Compact-disk recording samples the audio signal at 44.1 kHz and stores it as a 16-bit word; this resolution yields a 98-dB S/N ratio.

connect an existing LSI control circuit, the PCM56P DAC, and the left- and right-channel integrate-and-hold circuits. The control circuit (a Sony CXD-1130Q) operates at a clock frequency of 4.23 MHz and includes a 2× oversampling filter. The single serial output contains data that is decoded by the DAC and multiplexed to the appropriate channel by means of FET switches. The FET switches are driven by signals from the LSI circuit's APTR and APTL terminals.

High-end design uses a DAC for each channel

If you're designing a high-end system, you'll want to employ separate DACs for each channel, using support circuitry to steer the digital input to the appropriate DAC. Although it isn't the most inexpensive scheme, this arrangement provides the maximum degree of channel separation.

Fig 2 illustrates this type of configuration. The setup provides a separate DAC for each channel and includes deglitching circuits in the form of FET switches in series with the S/H amplifiers. The latch-enable output (CO4) generates the control signals. To prevent a switching race, the inverters introduce a delay. Because of the low glitch energy of the DACs, you may not need deglitching circuitry; in that case, you can also dispense with the delay circuit.

You can use a DAC such as the PCM56P in systems that employ separate DACs for each channel as well as in those that use one DAC multiplexed between channels. The PCM56P operates to 4× oversampling frequencies in either of these modes, and the glitch energy is small enough to preclude the need for a deglitcher in many applications. Its digital feedthrough is minimal, and its combined analog and digital noise is typically less than 6 μV over a 20-kHz bandwidth (see **box,** "The PCM56P D/A converter").

Digital filter removes extraneous frequencies

In any sampled-data system, you must band-limit the input signal to prevent aliasing. You must also filter the sampled output waveform in a similar fashion to eliminate those frequencies inserted by the sampling operation. Because you desire the dynamic range of the system to be greater than 90 dB, your system must

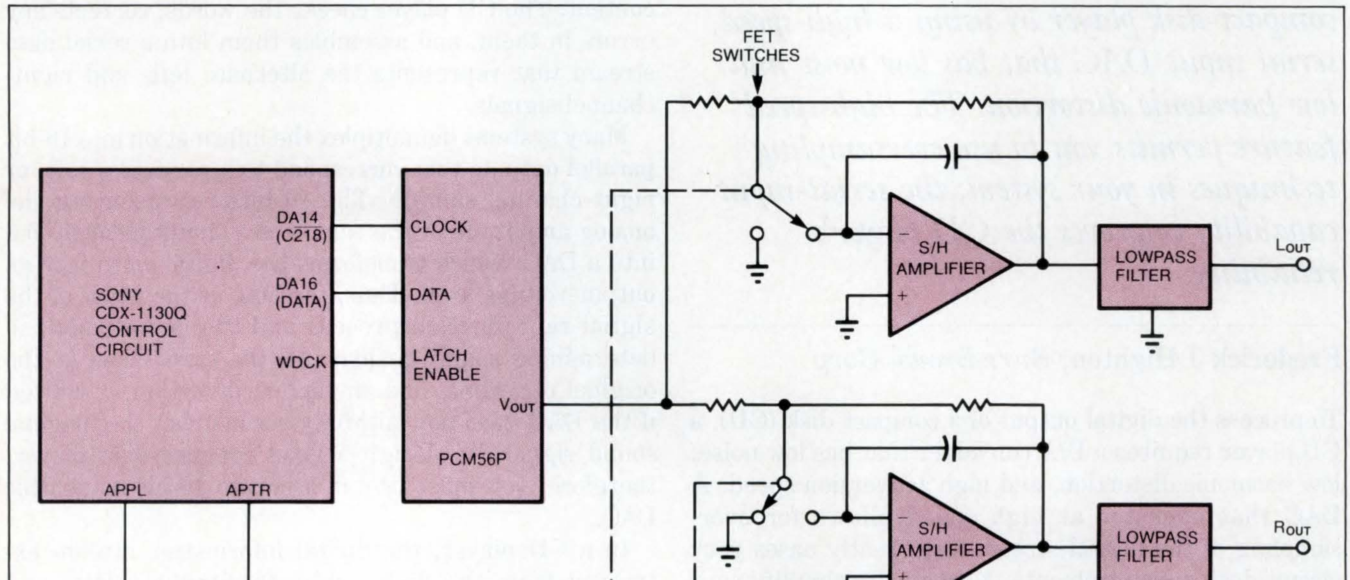


Fig 1—This CD-player design uses a single DAC for both channels. *The control circuit operates at a clock frequency of 4.23 MHz and includes a 2× oversampling filter. The single serial output sends data that is decoded by the DAC and multiplexed to the appropriate channel by FET switches.*

attenuate these extraneous frequencies by at least that amount. To achieve this degree of attenuation in a single octave (22 to 44 kHz), you need to use a multipole analog filter. Such a filter is expensive, difficult to build, and invariably introduces distortion of both amplitude and phase.

One way to overcome this problem is to turn to digital filtering. Although digital-filtering circuitry is very complex, you can easily obtain it in an economical, off-the-shelf LSI circuit. Digital filtering increases the sampling frequency by a factor of two or four. This increase effectively removes the frequency bands centered around the original sampling frequency and also removes the harmonically related components as high as the new oversampled frequency. You apply digital filtering to the digital word before the D/A conversion takes place.

After conversion and deglitching, a modest amount of filtering will remove the remaining oversampling frequency components. For example, if your design has 4× oversampling, a simple, third-order, lowpass filter is sufficient. In addition to reducing the size and cost of your system, digital filtering will also reduce the signal's phase distortion and improve its transient response. One disadvantage of the process is that it increases the DAC's speed requirements—the DAC must now operate at a greatly increased sample rate.

When changing from one output signal to another, a DAC takes a finite time to reach and settle to the new value. In many DACs, this change is accompanied by a large voltage spike called a glitch. Your CD-player system will need to employ a sample-and-hold (S/H) circuit that acts as a deglitcher, removing these spikes as well as the possibly erroneous output associated with

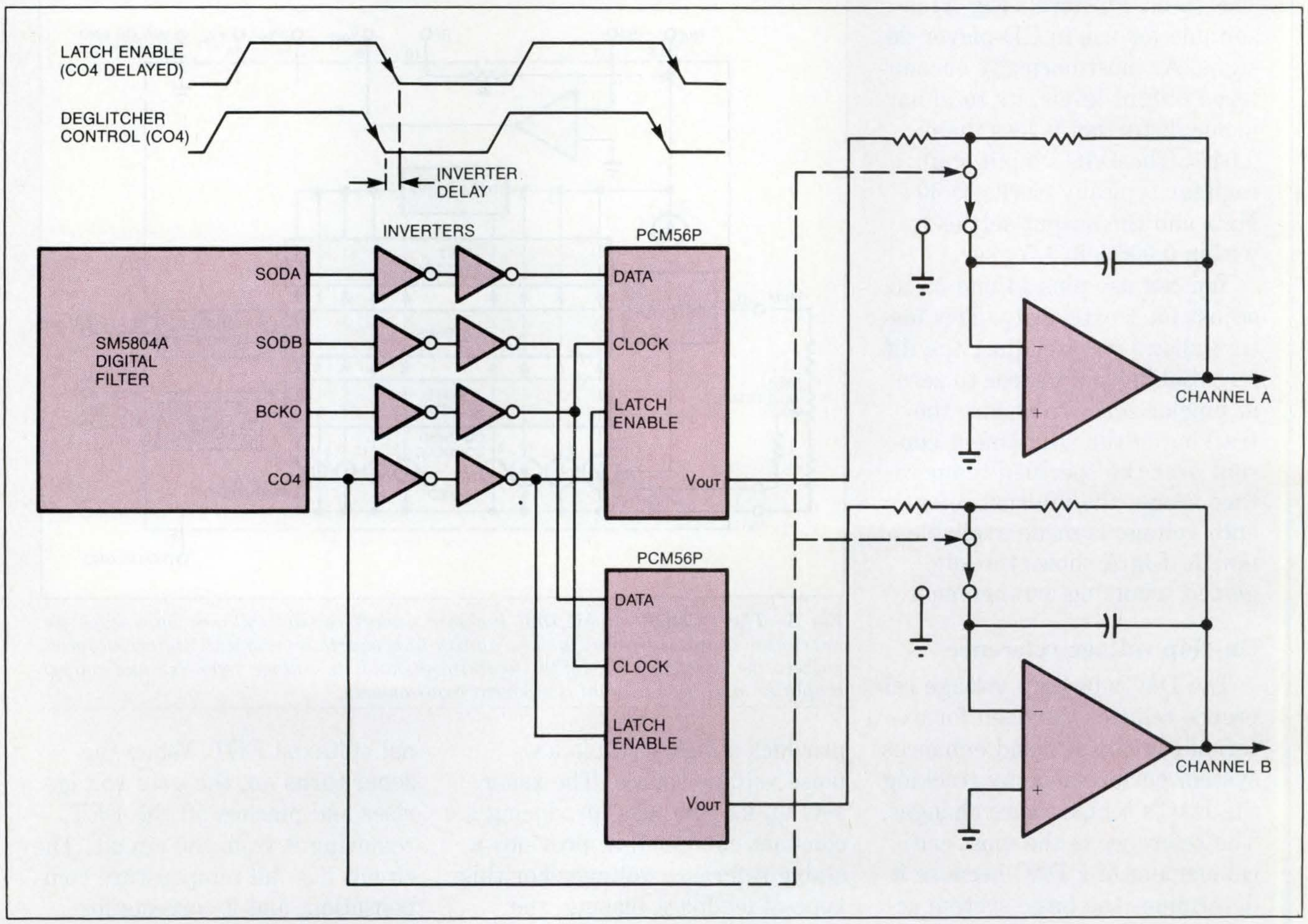


*Fig 2—**This high-end CD-player design provides separate DACs** for each channel. The digital filter's left- and right-channel outputs operate at 4× oversampling frequencies. This scheme employs deglitching circuits, and the control signal is generated from the CO4 latch-enable output.*

The DAC's function is to reconstruct the digital information on the CD as an exact replica of the original analog signal.

the DAC's change of state. The timing of the S/H circuit is such that it samples the DAC's output only after it settles to the new value. During the period of the DAC's output glitch, the deglitcher operates in the hold mode and prevents the disturbance from coupling to the output. After deglitching, the audio signal (now a pulse-amplitude-modulated wave) passes through a smoothing filter that removes all traces of the sampling frequency and its associated harmonics, thus providing a faithful reproduction of the original audio waveform.

As previously stated, many DACs give rise to a large voltage spike at the instant they change output levels. The cause of this spike is often the reference-element voltage, which fluctuates with the switching of the bit currents. If this voltage spike varies with the digital code, as is usually the case, the output of the filter will contain extraneous information. This code-dependent information will interact with the audio signal and cause distortion. To prevent this interaction, you can employ an S/H circuit. If your design uses only one DAC, the S/H circuit also functions as the demultiplexer. If your design uses separate DACs for each channel, you must follow each channel with its own deglitching circuit.

The DAC's function is to reconstruct the digital information as an exact replica of the analog informa-

The PCM56P D/A converter

The 16-bit PCM56P **(Fig A)** is suitable for use in CD-player designs. At most normally encountered output levels, its total harmonic distortion is less than 0.04%. The DAC's input shift register typically clocks to 30 MHz and the output settles to within 0.006% in 1.5 μsec.

You can use pins 14 and 15 to adjust bit 1 externally. This feature allows you to adjust the differential-linearity error to zero at bipolar zero. To ensure the tracking of the adjustment current over the specified temperature range, the internal reference voltage is made available at pin 15. **Fig A** shows the suggested trimming arrangement.

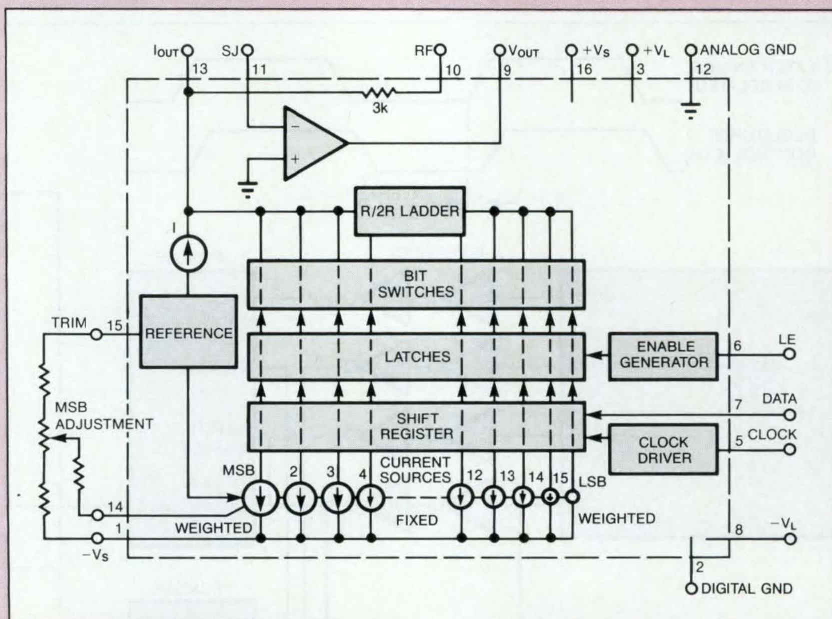


***Fig A—The PCM56P 16-bit DAC** includes a shift register followed by a latch for maximum loading flexibility. The ability to separate analog and digital supplies reduces the possibility of digital feedthrough, and its voltage reference and output amplifier minimize external component requirements.*

On-chip voltage reference

The DAC's on-chip voltage reference reduces the need for external components and enhances system performance by tracking the DAC's temperature changes. The reference is the most critical element of a DAC because it determines the basic system accuracy. A buried zener diode is the heart of the reference; it provides a highly stable low-noise voltage source. The zener sets up its own bias, producing a constant current that provides a stable reference voltage. For this type of feedback biasing, the DAC requires a start-up circuit, which is provided by an n-channel epitaxial FET. When the zener turns on, the gate voltage rises and pinches off the FET, removing it from the circuit. The circuit has full temperature compensation, and it corrects for drift in both V_{BE} and H_{FE}.

The input shift register, which

tion used to record the digital samples. Assuming that the recording process was accurate and that any digital-word corruption during storage and retrieval has been corrected, the fidelity of the entire reconstruction process depends on the performance of the DAC.

Traditionally, the most important specifications for DACs are the gain error, offset error, and integral and differential linearity. For industrial applications, these specifications are adequate to describe a DAC's expected performance. For audio applications, however, rigorous specifications of gain error and offset error are not important. Gain error merely appears as a small change in sound volume, which the listener can control. Offset error gives rise to a dc offset voltage, which capacitive coupling removes.

Instead of considering gain error and offset error in CD-player design, you must pay attention to a number of new specifications. A DAC's total harmonic distortion (THD) spec, for example, is very closely related to its linearity. This relationship is expressed by the equation

$$\mathrm{THD}=\frac{e_{RMS}}{E_{RMS}}=\frac{\sqrt{1/n\sum_{i=1}^{n}[E_L(i)+E_Q(i)]^2}}{E_{RMS}}\times 100\%,$$

where E_{RMS} is the rms input signal level, e_{RMS} is the

employs differential current-mode logic (CML), consists of a straightforward arrangement that is more efficient than the traditional ECL construction because it couples the master/slave functions. The result is a saving of two transistors per stage—a significant saving because the circuit uses 16 such stages. To prevent the latch circuit's emitter-coupled input transistors from saturating, the circuit employs level shifting, which takes place only between the three logic inputs and the shift register and latch circuits.

The chip uses a single cross-coupled latch that occupies minimum area but requires a narrow pulse to operate correctly. Commonly available LSI circuits don't generate such a pulse, so the DAC generates it on chip.

Enable pulse generator

The DAC's enable pulse generator consists of a D-type flip-flop with a constant logical one at its input. An external latch-enable control signal clocks the flip-flop and resets it with the next occurring positive clock edge. The circuit achieves the reset function by gating the clock pulse with the enable output. The output amplifier and driver stage ensure the fast operation of the 16 latches that are tied to the enable output.

The DAC includes a differentially connected, lateral pnp-transistor pair that converts the input logic signal to a current that is returned to the negative supply rail. The pair operates at clock frequencies in excess of 30 MHz.

The clock driver must supply the 16 master/slave shift-register stages. This requirement represents a much heavier load than that applied to the enable output, and it places much greater demands on the driver. The driver circuit acts in push-pull mode at the clock rail outputs. Any capacitance on the clock lines, therefore, is driven by the total available current.

The arrangement of bit currents in the DAC is such that the three most significant bits use binary-weighted current sources, the next nine bits use equal current sources that are binary-weighted through an R/2R ladder network, and the least significant bits use emitter division of a single current source. Differential switching helps to make the bit switches' turn-on and turn-off times equal, which considerably reduces glitch energy. The chip minimizes digital feedthrough by using differential circuitry for all clock signals and data signals throughout the shift-register and latch stages.

Output amplifier

The DAC's output amplifier is a typical op-amp structure that uses a phase splitter to drive an all-npn output stage. It produces the 3V (peak) audio-output level required for CD-player systems. The amplifier has a typical open-loop gain of 90 dB and a unity-gain bandwidth in excess of 4 MHz. The amplifier can drive 8-mA load currents. It gives the DAC an overall settling time of 1.5 μsec for an output-voltage change of 6V.

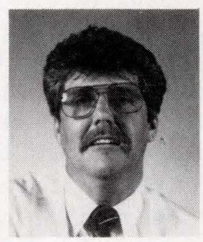
error level compared to the input, n is the number of samples in one cycle, $E_L(i)$ is the linearity error at a specific sampling point, and $E_Q(i)$ is the quantization error at that sampling point.

Because the error of a particular digital code is a unique summation of bit errors, PCM DACs usually specify THD that's measured with digitally coded sine waves of differing amplitudes; this specification gives a much clearer indication of the DAC's actual performance.

The DAC you use in a CD-player design must satisfy some very demanding specifications. For example, to achieve the extremely low levels of harmonic distortion that the industry has become accustomed to, you must use a DAC that has at least 14-bit accuracy and 15-bit monotonicity, and the serial-input function must not compromise linearity or noise performance. To accommodate 4× oversampling and the simultaneous multiplexing between channels, the DAC must handle clock speeds in excess of 8.5 MHz and have fast-settling characteristics. Because of these higher speeds, your CD-player system will probably need a deglitcher with a shorter time constant, so the DAC you choose should also have sufficient output-drive-current capability.

EDN

Author's biography



Fred Highton is the design manager for PCM products at Burr-Brown's Advanced Products Div (Tucson, AZ). Prior to joining Burr-Brown about two years ago, he worked with the GE Mobile Radio Div in Virginia. He has also worked at Plessey Co. Fred is a graduate of the Northampton College of Technology and the Lanchester College of Technology, both in the UK. He is a member of the IEE (UK). In his spare time, Fred enjoys hiking.

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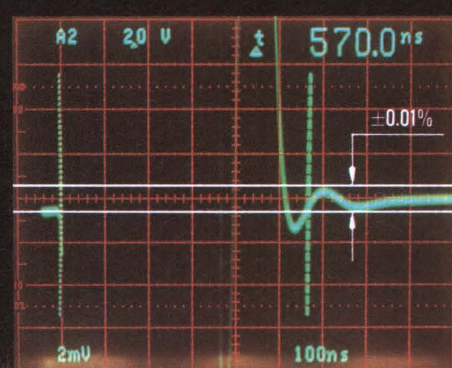
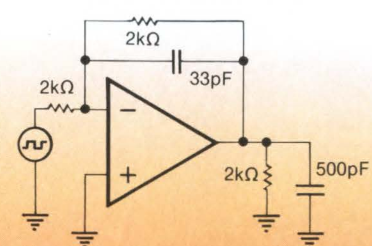


Output Settling Time



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Digital signal-synthesis tools model real-world environments

High-speed digital signal synthesizers can generate test signals that exhibit varying degrees of distortion and noise. The flexibility and repeatability that the digital tools offer can help you test electronic systems ranging from magnetic disk drives to television receivers.

Karen Kafadar, *Hewlett-Packard Co*

Digital signal synthesis can serve as a powerful tool in electronic-system test applications. The technique allows you to define a variety of waveforms in software; you then download the data to a waveform synthesizer to generate the corresponding real-life signals that you can use to characterize the equipment under test.

Noise—a characteristic of any operating environment—is of particular importance in test applications, and a waveform synthesizer's ability to generate quantifiable noise allows accurate determination of the performance margins of a system under test. In contrast, noise generation by other methods (for example, by noise diodes or resistors) is often difficult to characterize or is not repeatable, making accurate, consistent test results difficult to obtain.

One system that employs digital signal synthesis is the HP8770 arbitrary waveform synthesizer, or AWS, which works in conjunction with a computer running the WGL waveform-generation language (see **box,** "A look at an arbitrary waveform synthesizer"). The HP8770 can implement an algorithm for generating nearly Gaussian noise.

A waveform-synthesis example

As an example of how the AWS and WGL generate a digitally synthesized waveform, consider a pulse waveform with the following characteristics:

- 40-nsec rise time (0 to 100%)
- 200-nsec pulse width (at 100%)
- 56-nsec fall time (100% to 0)
- 2-μsec period.

Because the AWS spaces waveform points 8 nsec apart (which corresponds to a 125-MHz rate), the pulse train requires 2 μsec/8 nsec=250 points: The rise time requires 40 nsec/8 nsec=5 points; the pulse width requires 200 nsec/8 nsec=25 points; the fall time requires 56 nsec/8 nsec=7 points; and the rest of the points are zeros. The points are generated in WGL by using straight segments and are stored in a macro where they can be called repeatedly.

Noise can be added to this signal by calling a simple WGL command labeled NOISE. This command generates a noise waveform whose points are independent and whose amplitudes are uniformly distributed. An

Digital synthesis tools can produce test signals with varying degrees of noise, distortion, or signal variations similar to those encountered in real-world environments.

A look at an arbitrary waveform synthesizer

The HP8770S arbitrary waveform synthesizer (AWS) uses digital signal synthesis to create waveforms in the frequency range of dc to 50 MHz. Digital data is created on a computer running a Waveform Generation Language (WGL) and downloaded to the synthesizer. Used together, WGL and the AWS can produce test signals with varying degrees of noise, distortion, or signal variations similar to those encountered in real-world environments.

A simplified block diagram of the HP8770S AWS system is shown in **Fig A**. The first step is the design of a waveform in computer software, which here is depicted as WGL running on an HP9000 Series 200 or Series 300 computer. (**Table A** lists some WGL commands.)

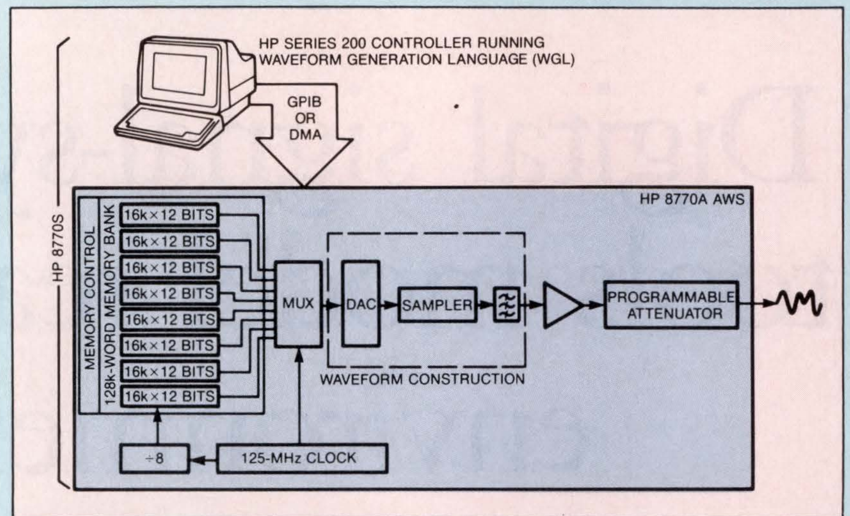


Fig A—In this arbitrary-waveform-synthesis system, *the AWS is interfaced to an HP Series 200 controller running WGL.*

Next, the waveform data is downloaded into the 128k-word AWS memory, which is partitioned into eight sections of 16k 12-bit words. A multiplexer selects one word at a time from each of the sections and sends them to a 12-bit DAC, which yields 0.024% amplitude resolution. The DAC can generate samples at a 125-MHz rate (eight samples every 64 nsec).

The DAC is followed by a sampler, which smooths the transitions between samples, and by an anti-aliasing filter, which eliminates power beyond 50 MHz. An amplifier raises the smoothed output level to a ±1V level (more amplifiers may be added for higher output levels). Finally, a programmable output attenuator scales the waveform's amplitude to power levels ranging from +10 to −100 dBm.

The DAC's 125-MHz sampling rate allows it to run through the entire 128k-word memory in less than 1.05 msec. However, a memory sequencer allows repetition of packets, or sections of memory, thus permitting generation of waveforms of durations much longer than one millisecond.

TABLE A—REPRESENTATIVE COMMANDS OF THE WAVEFORM GENERATION LANGUAGE

COMMAND	OPERATION
CTX	SET CONTEXT OF WAVEFORM
DEFINE	CREATE NEW WGL COMMAND DEFINITION
DOWNLOAD	STORE COMPUTED WAVEFORM DATA INTO AWS MEMORY
FDOMAIN	OPERATE IN FREQUENCY DOMAIN
FREQ	DETERMINE PARAMETERS FOR SINE WAVE
GO	GENERATE WAVEFORM IN AWS
HZ	CONVERT SPECIFIED FREQUENCY INTO HERTZ
LOAD	FILL ALL ELEMENTS OF WORKING WAVE WITH SPECIFIED VALUE
NOISE	FILL ALL ELEMENTS OF WORKING WAVE WITH UNIFORM NOISE [−1, 1]
NORM	SCALE WORKING WAVE TO [−1, 1]
PACKET	DEFINE PACKET WITH WAVEFORM NAME AND NUMBER OF REPETITIONS
PI	CONSTANT 3.1415926536
RAMP	CREATES A RAMP (LINE) FROM −1 TO 1 IN PRESENT WINDOW
STORE	STORE WAVEFORM (A, B, C, D, E)
TDOMAIN	OPERATE IN TIME DOMAIN
TOBD	CONVERT DECIBEL VALUE TO LINEAR VALUE
TOLIN	CONVERT LINEAR VALUE TO DECIBELS
TOTIME	CONVERTS A TIME DOMAIN SIGNAL TO THE FREQUENCY DOMAIN
TOFREQ	CONVERTS A FREQUENCY DOMAIN SIGNAL TO THE TIME DOMAIN
WINDOW	SELECT PORTIONS OF ENTIRE WAVEFORM FOR MANIPULATION
X Y	EXCHANGES WAVEFORMS IN CURRENT AND AUXILIARY LOCATIONS

NOTE: THE COMMANDS EMULATE THOSE OF A CALCULATOR USING RPN.

oscilloscope recording of the pulsed train along with additive noise generated by the NOISE model is shown in **Fig 1**. The WGL command TOFREQ computes the amplitude and phase spectra required for frequency analysis. **Fig 2** shows the amplitude spectrum of the pulse train and the additive noise when the amplitude spectrum is downloaded to a spectrum analyzer.

An algorithm for generating nearly Gaussian noise

Although the noise components of the **Fig 1** waveform are easy to generate using a single WGL command, the added noise has uniformly distributed ordinates, and observation of **Fig 2** shows that the noise power spectrum is not flat—rather, it contains discrete components of variable amplitude. These components are related to the sequence length of the pseudorandom code used to generate the noise. In this case, the sequence length is 2000 pseudorandom words, which are generated every 8 nsec, thereby producing periodic spectra every 62.5 kHz (the inverse of 16 μsec).

In contrast, consider the desirable properties of a digitally synthesized noise waveform for test applications. First, the waveform should have a nearly flat power spectrum. The theoretical power (or amplitude) spectrum of an infinitely long and continuous noise waveform is constant—that characteristic defines white noise **(Ref 1)**, and such a waveform permits rapid detection of nonlinearities in system response. Unfortunately, the length of digitally synthesized waveforms is limited by memory, and such waveforms aren't continuous because of sampling. Further, aliasing, waveform repetition, and computational Fourier transformation result in a discrete spectrum. Nevertheless, an algorithm that simulates white noise should account for these realities and produce a power spectrum that's as nearly constant as is feasible.

Second, the noise waveform should exhibit zero autocorrelation for all nonzero time shifts. If a waveform is truly noisy, then knowledge of its value at any time point provides no information whatsoever about its value at any other time point. Such a waveform is said to be uncorrelated with itself (except at zero time shift, for which the correlation is, of course, one); white noise has this property. Because any digitally synthesized signal is necessarily discrete and periodic (it is repeated many times), the autocorrelation will also be periodic, taking the value 1 at time shifts that are integral multiples of the length of the sequence. For all other time shifts, the autocorrelation function should be zero.

Third, the desirable waveform should have Gaussian distributed ordinates. A Gaussian waveform has the property that the joint distribution of any set of waveform values is Gaussian.

Fourth, the waveform should be easy to implement in software; the algorithm should not be computationally intensive.

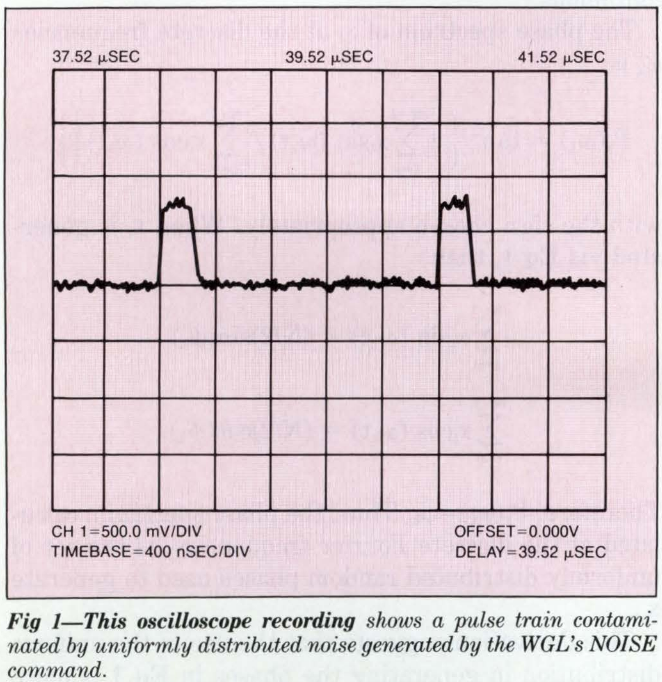


Fig 1—This oscilloscope recording *shows a pulse train contaminated by uniformly distributed noise generated by the WGL's NOISE command.*

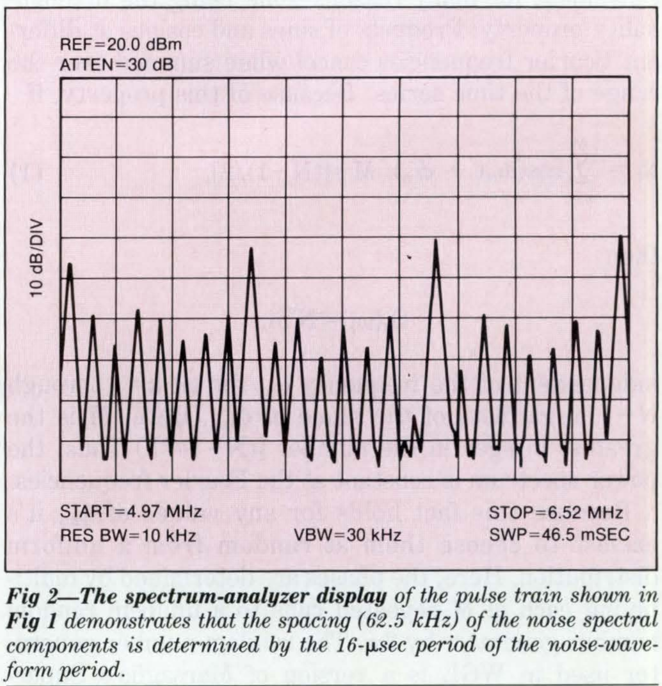


Fig 2—The spectrum-analyzer display *of the pulse train shown in* ***Fig 1*** *demonstrates that the spacing (62.5 kHz) of the noise spectral components is determined by the 16-μsec period of the noise-waveform period.*

When one sequence of 2048 samples is used to generate noise, the difference between the actual and the theoretical Gaussian distribution is less than 5%.

The first and third properties jointly define Gaussian noise, which is representative of noise found in typical operating environments. It's possible to develop an algorithm in WGL that generates a noise waveform that is more nearly Gaussian than is the one that results from the NOISE command. Although the algorithm (which is derived in the following paragraphs) requires more than one WGL command to generate Gaussian noise, it is still easily implemented and can be stored in a macro for repeated use.

Derivation of the noise algorithm

If x_t represents a series of N noise-waveform samples taken at intervals of t=0, 1, 2, . . . , N−1, the discrete Fourier transform of these samples is defined by:

$$J(\omega) = \sum_{t=0}^{N-1} x(t)e^{-j\omega t}.$$

The power spectrum of x_t is denoted by $S_x(\omega)$, where

$$S_x(\omega) = |J(\omega)|^2,$$

and the phase spectrum is denoted by $P_x(\omega)$. Note that the amplitude spectrum is the square root of $S_x(\omega)$.

Typically, the power spectrum is computed at a discrete set of frequencies. The set of frequencies denoted by $\omega_k=2\pi k/N$ for k=0, 1, 2, . . . , N-1 is convenient for many reasons—one being the orthogonality property: Products of sines and cosines at different Fourier frequencies cancel when summed over the range of the time series. Because of this property, if

$$x_t = \sum_{m=1}^{M} \cos(\omega_m t + \phi_m),\ M=[(N-1)/2], \tag{1}$$

then

$$S_x(\omega_k)=N^2/4,$$

independent of the frequency ω_k, for all k=1 through N−1, regardless of the value of ϕ_m. (Here, M is the greatest integer in the number [(N−1)/2].) Thus, the power spectrum is constant at the Fourier frequencies.

Because this fact holds for any values of ϕ_m, it's easiest to choose them at random from a uniform distribution. Here, the phases are determined by multiplying each of M repeated calls to a uniform random number generator by 2π. The random-number generator used in WGL is a version of Marsaglia's Super-Duper generator (**Ref 2,** pg 500).

Illustrating the constancy of the power spectrum of x_t defined in **Eq 1** is easiest in complex exponential notation. Because $\cos\theta=(e^{j\theta}+e^{-j\theta})/2$, then

$$J(\omega_k) = \sum_{t=0}^{N-1}\sum_{m=1}^{M} e^{j(\omega_m t+\phi_m)}e^{-j\omega_k t}$$

$$= \sum_{m=1}^{M} e^{j\phi_m}\sum_{t=0}^{N-1} e^{j(\omega_m-\omega_k)t}$$

$$= \begin{cases} 0 \text{ for } m\neq k \\ (N/2)e^{j\phi_k} \text{ for } m=k, \text{ not 0 or } N/2. \end{cases}$$

Hence,

$$|J(\omega_k)|^2 = \frac{N^2}{4}.$$

(The values m=k=0 or N/2 aren't possible because they don't fall within the defined range m=1 to [(N-1)/2].) Because the waveform is periodic—x_t repeats many times—its power spectrum is discrete; that is, spectral lines of power are nonzero at frequency spacing 1/N, where N is the length of the nonrepeating segment of the waveform. These spectral lines are all of equal height, and as N approaches infinity, they become closer, thus making the power spectrum more nearly continuous.

The phase spectrum of x_t at the discrete frequencies ω_k is

$$P_x(\omega_k) = \tan^{-1}\left\{ \pm\sum_{t=0}^{N-1} x_t\sin(\omega_k t) \Big/ \left|\sum_{t=0}^{N-1} x_t\cos(\omega_k t)\right| \right\},$$

with the sign chosen appropriately. When x_t is generated via **Eq 1,** then

$$\sum_{t=0}^{N-1} x_t\sin(\omega_k t) = (N/2)\sin(\phi_k)$$

$$\sum_{t=0}^{N-1} x_t\cos(\omega_k t) = (N/2)\cos(\phi_k).$$

Therefore, $P_x(\omega_k)=\phi_k$. Thus, the phase spectrum, calculated at the discrete Fourier frequencies, is the set of uniformly distributed random phases used to generate x_t.

This derivation suggests that the use of the uniform distribution in generating the phases in **Eq 1** is more than merely convenient, because the distribution of the phase-spectrum ordinates for a truly stationary Gaussian signal is uniform (**Ref 3**). (This fact is a consequence of the computations, not a defining property of Gaussian white noise.) Because x_t as generated by **Eq 1** is discrete (that is, N is finite), its distribution is Gaussian only asymptotically (that is, it is Gaussian only at N equals infinity). Nonetheless, when **Eq 1** uses uniformly distributed phases on the interval $[0, 2\pi]$, the phases are recovered exactly, so the distribution of the phase spectrum for x_t agrees with that for Gaussian white noise.

The autocorrelation function for the series of x_t samples is

$$\rho(k) = \mathrm{cor}\{x_t, x_{t+k}\} = \mathrm{ave}\{x_t x_{t+k}\}/\mathrm{var}\{x_t\}.$$

When x_t is generated by **Eq 1,** it can be shown that

$$\mathrm{ave}\{x_t x_{t+k}\} = \sum_{m=1}^{M} \cos(\omega_m k)/2, \quad M-[(N=1)/2],$$

and so

$$\rho(k) = \begin{cases} 1 \text{ for } k = 0, N, 2N, \ldots \\ -1/M \text{ for } k \text{ even (not } 0, N, 2N, \ldots) \\ 0 \text{ for } k \text{ odd.} \end{cases}$$

Note that as N approaches infinity, $\rho(k)$ approaches 0 for all values of k except $k=0$, therefore satisfying the property that a waveform should exhibit zero autocorrelation for all nonzero time shifts. Because the signal is in discrete time at the synthesizer stage, its autocorrelation function is essentially zero at nonzero time shifts up to the length of the sequence. The antialiasing filter after the D/A conversion creates a continuous time signal and, for large N, is unlikely to alter appreciably the autocorrelation beyond a few time shifts. Thus, the waveform has negligible autocorrelation and most likely can't be distinguished in practice from random sequences.

As a result of choosing pseudorandom phases for x_t in **Eq 1,** the value of x_t becomes the sum of independent random quantities and, therefore, has a nearly Gaussian probability distribution. This is due to the Central Limit theorem, so called because of its central importance in probability theory. When ϕ_m is uniformly distributed between 0 an 2π, $\cos(\omega_m t+\phi_m)$ has a probability distribution that is far from Gaussian. Yet,

$$\mathrm{ave}\{\cos(\omega_m t + \phi_m)\} = (2\pi)^{-1}\int_0^{2\pi} \cos(\omega_m t + \phi_m)d\phi_m = 0$$

$$\mathrm{var}\{\cos(\omega_m t + \phi_m)\} = (2\pi)^{-1}\int_0^{2\pi} \cos^2(\omega_m t + \phi_m)d\phi_m = 1/2.$$

The Central Limit theorem states that the sum of the $M=[(N-1)/2]$ independent terms (that is, x_t) has a distribution that is nearly Gaussian with a mean of zero and a variance M/2. This result is asymptotic; the approximation improves as N increases. If x_t is multiplied by $2/\sqrt{N-2}$ when N is even and by $2/\sqrt{N-1}$ when N is odd, x_t is normalized to have a unit variance, and thus a unit root mean square.

How close to a Gaussian distribution is the actual distribution of x_t when generated via **Eq 1**? The Berry-Esseen theorem (**Ref 4,** pg 300) gives an upper bound on the difference between the actual probability distribution and the corresponding theoretical Gaussian probability distribution. For a normalized random sequence of length 2048 generated by **Eq 1,** the differences between the actual and the Gaussian distributions never exceed 3%; the Berry-Esseen upper bound is 5%.

Generating nearly Gaussian noise in WGL

Evaluation of x_t via **Eq 1** is very slow, because each time point requires $M=[(N-1)/2]$ cosine evaluations. However, x_t may be recognized as the result of an inverse Fourier transform, for which an FFT algorithm is appropriate (**Ref 3,** chapter 4). Using WGL, in the frequency domain with full scale set to 1, a constant is loaded into the magnitude vector, and the phase vector is filled with uniform noise. (Because most uniform

TABLE 1—WGL COMMANDS FOR GENERATING A WHITE-NOISE WAVEFORM

COMMAND	OPERATION
FDOMAIN	TRANSFER TO FREQUENCY DOMAIN
2049 CTX	CONTEXT OF WAVEFORM USES N+1 POINTS
1.0 LOAD	LOAD ONES IN THE FIRST (AMPLITUDE) VECTOR
0 0 STOREIN	LOAD 0 IN THE 0TH POSITION (DC COMPONENT)
X Y	INTERCHANGE: AMPLITUDE WITH PHASE
NOISE PI*	LOAD PHASE VECTOR WITH NOISE SCALED BETWEEN $-\pi$ AND $+\pi$
X Y	INTERCHANGE: PHASE WITH AMPLITUDE
TOTIME	GO TO THE TIME DOMAIN (INVERSE FFT)
DOWNLOAD	DOWNLOAD SEQUENCE INTO AWS MEMORY
GO	GENERATE WAVEFORM WITH AWS

A nearly Gaussian noise model is easy to generate using a few commands.

random number generators are on the interval [0, 1], the output must be scaled to the interval [0, 2π], or, equivalently, [$-\pi$, π].) Transforming to the time domain gives the inverse Fourier transform, using an FFT routine if N is a power of 2, or by direct computation (discrete Fourier transform) if it is not. Clearly, lengths that are powers of two are advantageous for generating Gaussian white-noise waveforms for purposes of computational speed.

The samples are then converted to the time domain via an inverse FFT. To generate a sequence length of 2048 samples, the commands listed in **Table 1** can be executed interactively or stored in a macro. (**Fig 3** illustrates the resulting waveform.) The sequence re-

TABLE 2—WGL MACROS FOR GENERATING A TEST WAVEFORM

WGL COMMAND: 0 20 9 11 10 SIGNOISE

MACRO SIGNOISE: AVG SNR f_{LOWER} f_{UPPER} CFREQ SIGNOISE

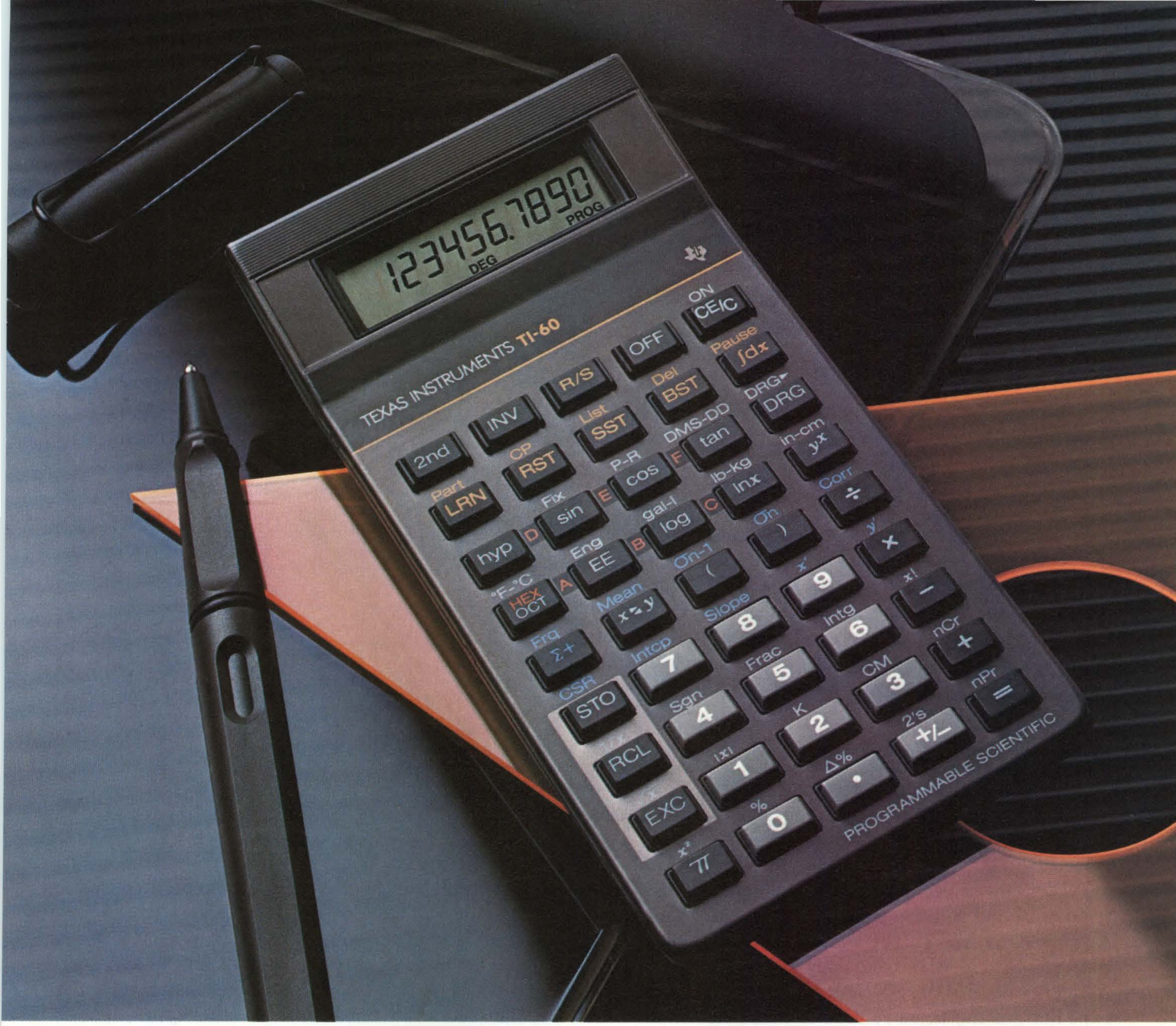
GENERATE A WAVEFORM SIGNAL+NOISE, WHERE THE CARRIER FREQUENCY OF THE SIGNAL IS CFREQ, AND THE NOISE, CONCENTRATED IN BANDWIDTH BETWEEN f_{LOWER} AND f_{UPPER}, HAS MEAN AVG AND SIGNAL-TO-NOISE RATIO WITH THE SIGNAL SNR.

COMMAND	RESULT
DEFINE SIGNOISE	MACRO DEFINITION
STORE CFREQ DOWN STORE FUPPER DOWN STORE FLOWER DOWN STORE SNR DOWN STORE AVG	STORE MACRO ARGUMENTS IN STACK
8193 CTX FDOMAIN	MAX CONTEXT IN FREQUENCY DOMAIN
125E6 4/CLOCK	IMPROVE FREQUENCY RESOLUTION
FLOWER 15.625/8193* INT STORE W1	VECTOR ELEMENT FOR f_{LOWER}
FUPPER 15.625/8193* INT STORE W2	VECTOR ELEMENT FOR f_{UPPER}
CFREQ 15.625/8193* INT STORE WC	VECTOR ELEMENT FOR CFREQ
2 SQRT INV SNR TOLIN/STORE RMS	CALCULATE RMS_{NOISE}
GWN	CALL MACRO GWN
2 SQRT INV?	CALCULATES RMS OF SINE WAVE
RAMP PI WC**SIN? STORE X	SIGNAL AT CFREQ, STORED AS WAVEFORM X
SQ SUM SIZE MAX SWAP/SQRT?	CALCULATES ACTUAL SIGNAL-TO-NOISE RATIO
X A +?	ADD NOISE TO SIGNAL AND DISPLAY
"TEMP;AUTO"S DOWNLOAD	DOWNLOAD WAVEFORM FROM FILE TEMP, AUTO SCALE, INTO AWS MEMORY
"INT;4"S AWSCLOCK	
GO	GENERATE WAVEFORM WITH AWS
END	

MACRO GWN:

GENERATE A GAUSSIAN WHITE NOISE WAVEFORM, MEAN AVG AND ROOT MEAN SQUARE RMS, IN THE WINDOW CORRESPONDING TO ELEMENTS OF THE FREQUENCY ARRAY BETWEEN W_1 AND W_2.

COMMAND	RESULT
DEFINE GWN	MACRO DEFINITION
0 LOAD XY 0 LOAD	CLEAR PHASE AND AMPLITUDE VECTORS
W1 W2 WINDOW	OPERATE ON ELEMENTS W_1 TO W_2 ONLY
NOISE PI*	GENERATE UNIF [$-\pi$, π] RANDOM PHASES
XY	CHANGE FROM PHASE TO AMPLITUDE VECTOR
AVG 0 STOREIN	LOAD AVG IN DC COMPONENT
W2 W1-2/SQRT INV RMS* LOAD	MULTIPLY WAVEFORM SO ROOT MEAN SQUARE=RMS
FULL?	DISPLAY GWN WAVEFORM
TOTIME ERASE STORE A	WAVEFORM IN TIME DOMAIN STORED AS A
AVG-SQ SUM SIZE MAX SWAP/SQRT?	CALCULATE, DISPLAY ACTUAL RMS OF WAVEFORM
A?	DISPLAY WAVEFORM
END	



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TEXAS INSTRUMENTS

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One algorithm relies on the Central Limit theorem to produce noise that has a nearly Gaussian probability distribution.

peats approximately every 16 μsec, which corresponds to 2048×8 nsec. The macro can be modified to generate Gaussian noise with a specified mean and standard deviation (rms_{NOISE}) by multiplying the waveform by $2(rms_{NOISE})/\sqrt{N-2}$ and loading the mean value for the dc component of the spectrum.

Generating real-world test signals and noise

The AWS provides a flexible tool for testing electronic devices such as receivers. One such test is to subject the receiver to a test signal that is contaminated with noise. When the noise is modeled by a source that has a flat power spectrum, the signal and noise test waveform can be used to measure signal degradation and nonlinearities in the receiver's power spectrum. A convenient method for specifying the amount of noise is the signal-to-noise ratio (SNR):

$$SNR = rms_{SIGNAL}/rms_{NOISE},$$

where rms_{SIGNAL} is the root mean square of the test signal and rms_{NOISE} is the standard deviation of the noise.

Table 2 describes a macro that generates a 10-MHz test signal and additive noise using the noise algorithm expressed by **Eq 1.** The noise has a 0 mean and is confined to a 2-MHz frequency band about a center frequency of 10 MHz. An SNR of 20 dB is specified. An expedient of the noise routine is that noise levels and bandwidths are easily altered. **Fig 4** shows a spectrum-analyzer display of the test waveform generated by the AWS.

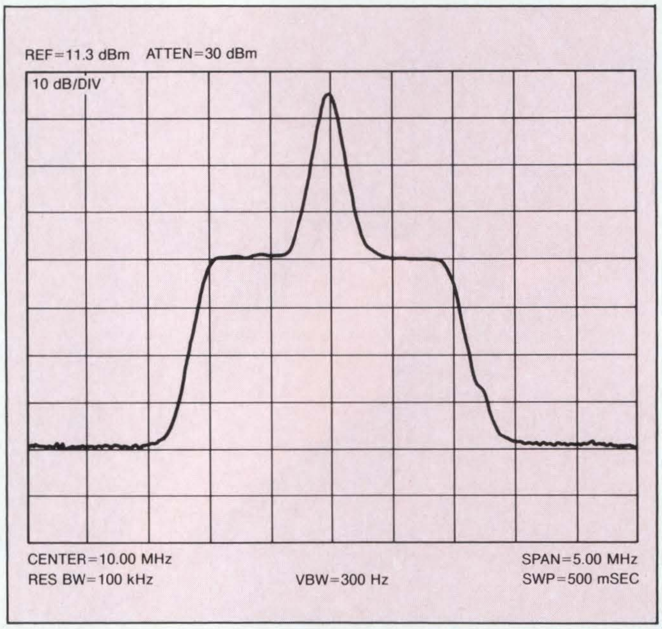

Fig 4—This spectrum-analyzer display *shows a 10-MHz test signal contaminated with noise that is bandlimited to 2 MHz. The noise has a nearly Gaussian distribution with an SNR of 20 dB.*

Under some circumstances, the use of a pseudorandom noise waveform might not be appropriate. Tests on certain electronic devices may involve not only Gaussian white noise, but also other types, such as 1/*f* noise or thermal noise. In such cases, a waveform

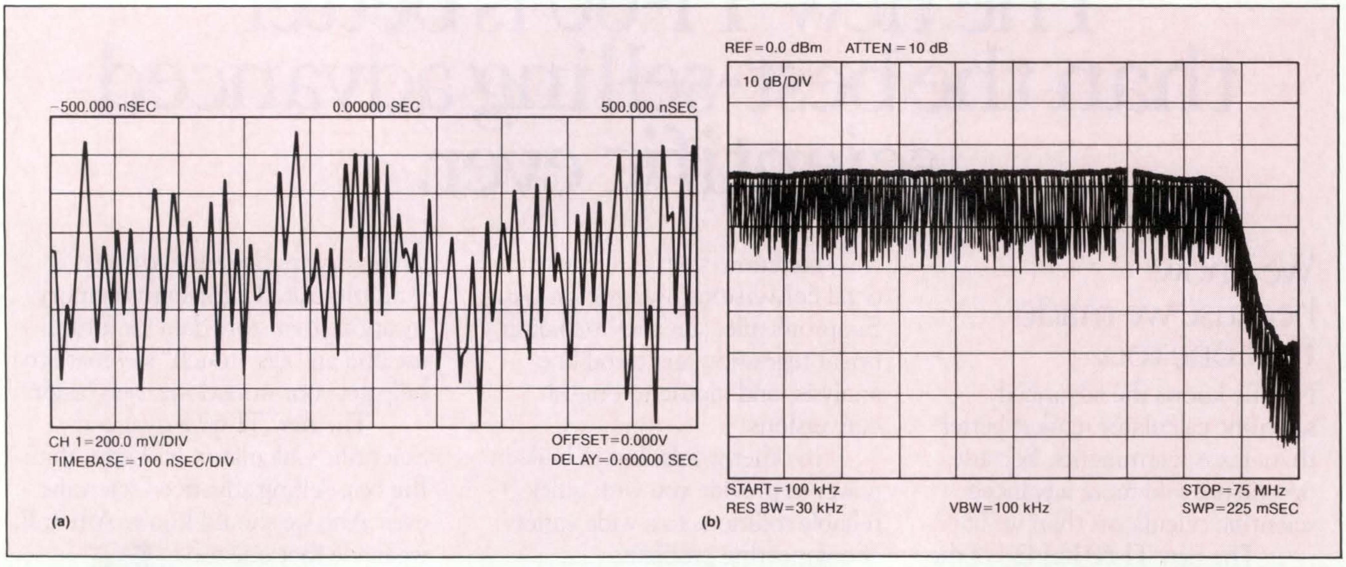

Fig 3—The WGL commands *listed in* ***Table 1*** *yield the signal that is illustrated by these oscilloscope* ***(a)*** *and spectrum-analyzer* ***(b)*** *displays.*

that most closely resembles the waveform of concern should be devised. However, for general test applications, the computer-generated Gaussian waveform will be suitable. **EDN**

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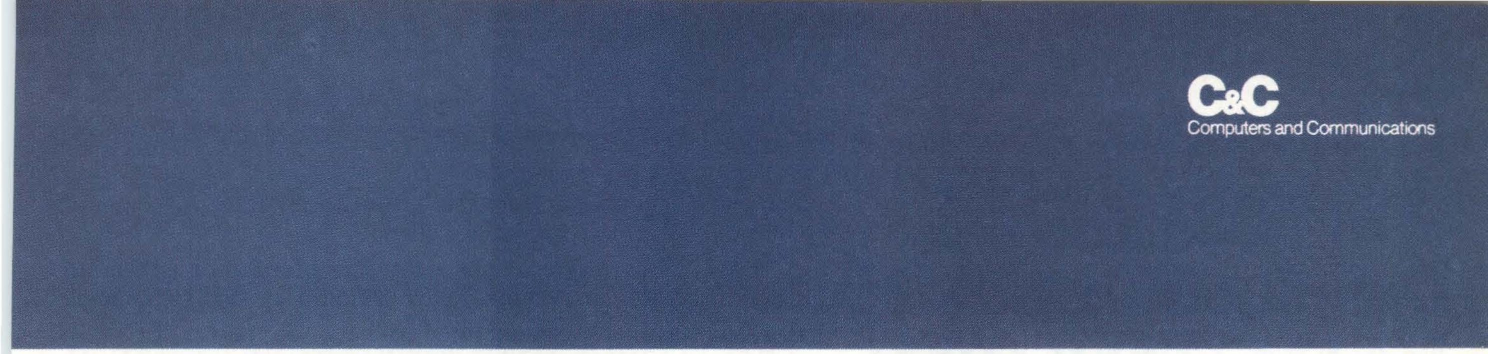

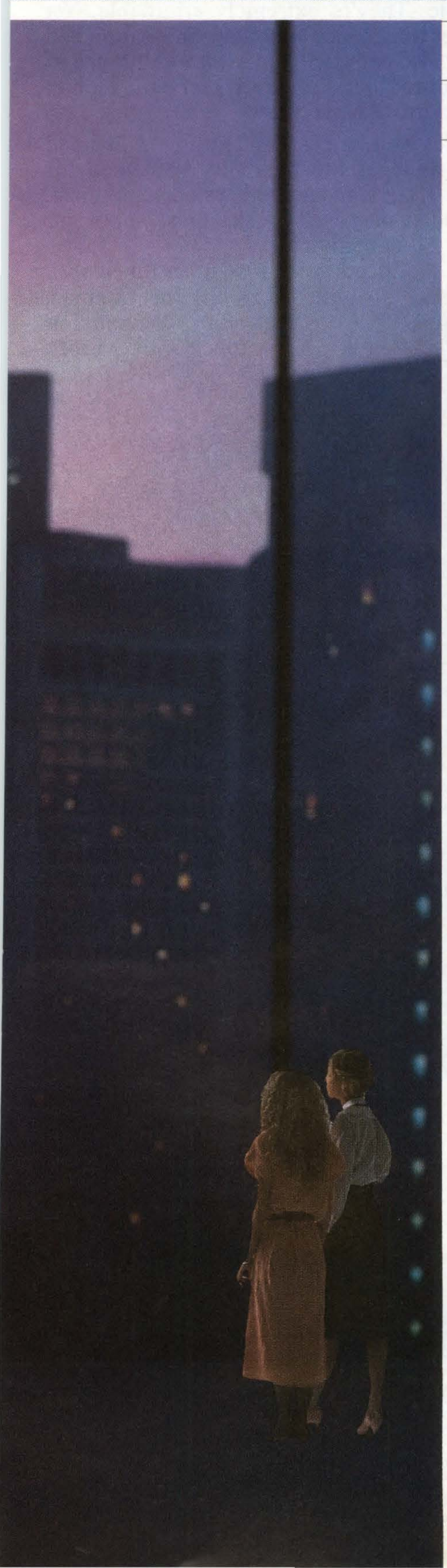

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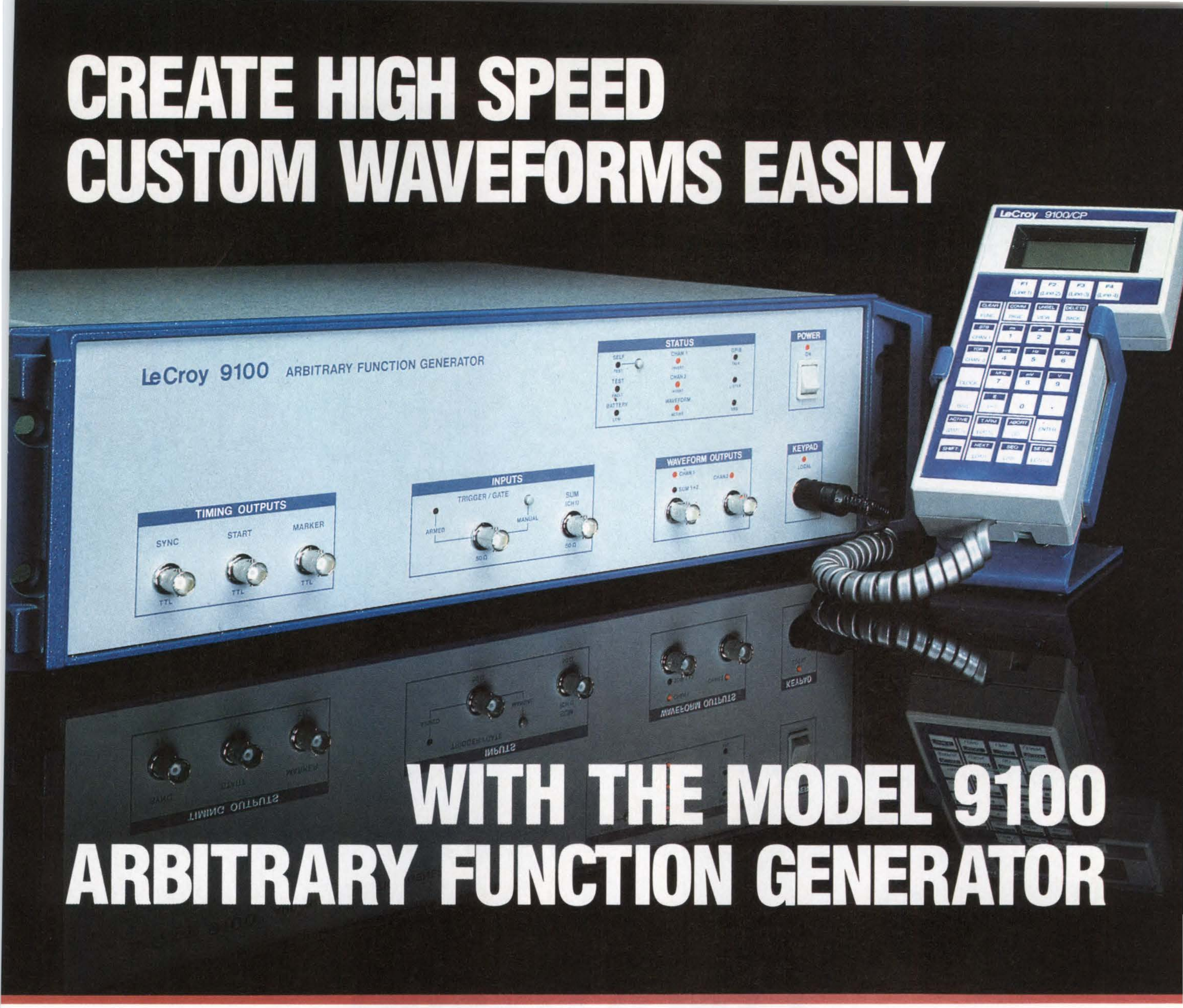

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Switcher power densities change filter-capacitor needs

The drive for high power densities in switch-mode power supplies is dramatically increasing the switching frequency in the units. This frequency increase now puts severe limitations on the output filter capacitor's electrical parameters and how it is physically mounted in the circuit.

John Maxwell, *AVX Corp*

High-frequency switch-mode power supplies place tremendous restrictions on output filter capacitors, and traditional capacitor-selection criteria no longer apply. Today, capacitors must handle high ripple current (which equates to low series resistance) and have an inductance that approaches 0 nH. The capacitors must be truly surface mountable and available in configurations that can be integrated into transmission lines to further reduce inductance. In short, the higher frequencies have changed the whole selection process.

Parameter requirements have changed

Historically, switch-mode power-supply (SMPS) designers have concentrated on a capacitor's ESR (equivalent series resistance) parameter to reduce output ripple voltage. To meet the low ESR requirement, designers would use 10 to 1000 times the supply design's minimum required capacitance and essentially ignore ESL (equivalent series inductance), considering it to be insignificant because of the large capacitance. Because switching frequencies have moved to 1 MHz and beyond, this situation has changed.

ESR no longer dominates output filter ripple and noise voltage performance—ESL is now the limiting factor. For most high-frequency SMPSs, total output filter inductance requirements will equal 1 nH or less, which will force designers to use surface-mount components to eliminate most component inductance.

Traditional filter-capacitor technologies cannot meet this need for low ESL. Electrolytic capacitors are not suitable for surface mounting because the electrolyte boils at the reflow-solder temperatures, and aluminum reacts violently with vapor-phase soldering fluids. Tantalum capacitors have high values of ESR, and even the surface-mount configurations have excessive ESL. In addition, if you fail to take handling precautions, reflow soldering accelerates a failure mode in surface-mountable tantalum capacitors, which causes ESR to increase with time. Tantalum and electrolytic capacitors have another problem—their intrinsically high ESR and ESL dramatically reduces the capacitance value at high frequency.

Film capacitors are not a viable alternative for today's SMPS designs either, because the polymers used

Traditional selection criteria no longer apply for output filter capacitors in today's switch-mode power supplies.

as dielectrics melt at solder reflow temperatures. Multilayer ceramic (MLC) capacitors are the only viable choice for very-high-frequency SMPS output filters.

Power density makes a big difference

Traditional MLC capacitors have very high values of ESL and ESR, so they are only viable for low-density supplies. These devices are not designed to minimize ESL and ESR; instead, they fill a need in commercial and military markets, where they are typically used for filtering or decoupling. To serve as output filter capacitors in high-frequency, high-power, switch-mode power supplies, capacitors must be designed to minimize ESL and ESR and to maximize ripple-current capability.

It's important to develop guidelines that establish practical limits of minimum required capacitance and maximum values of ESL and ESR for output filter capacitors. By their very nature, most SMPSs have high ripple currents (**Fig 1**). This ripple current (for a simple LC output filter) is typical for a forward or flyback converter. Alternate designs will have different but similar current waveforms and filter requirements.

The ripple current shown in **Fig 1** generates a ripple voltage that is a function of capacitance value, ESR, and ESL. ESL is the major culprit in high-frequency switching power supplies because of the high di/dt at the current inflection points. Increases in frequency or ripple (load) current proportionally increases di/dt and noise, because V=Ldi/dt (where L is the output filter inductance, di/dt is the rate of change of current with respect to time, and V is the voltage spike amplitude).

An order of magnitude increase in operating frequency or load current decreases the maximum allowable ESL by the same amount. As designers continue to increase switching frequencies and load currents to improve power densities, they must incorporate the output filter capacitor into a transmission-line structure to cancel its inductance. Designers are also taking switching frequencies above 10 MHz, which will force the output filter into cavities and new configurations to further reduce filter inductance.

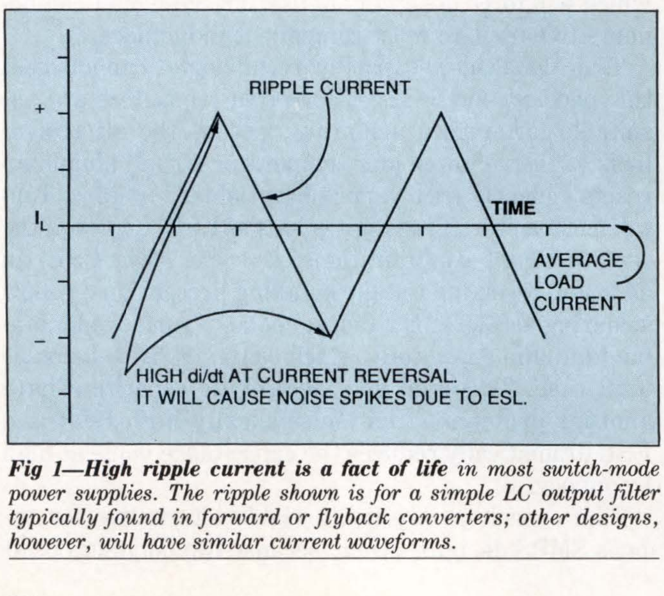

Fig 1—High ripple current is a fact of life in most switch-mode power supplies. The ripple shown is for a simple LC output filter typically found in forward or flyback converters; other designs, however, will have similar current waveforms.

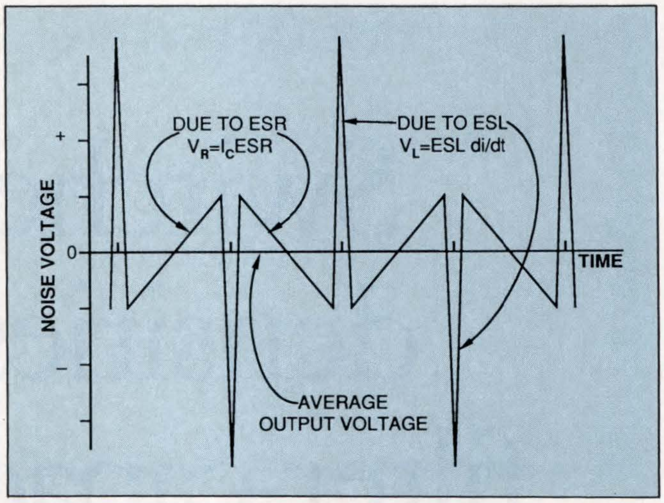

Fig 2—To establish practical limits for ESL, ESR, and C_{MIN}, derive each value by assuming that the other two make no contribution to output ripple and noise.

You can establish practical limits for ESR_{MAX}, ESL_{MAX}, and minimum output filter capacitance (C_{MIN}) by analyzing the current waveform in **Fig 2**. You can derive each limit by assuming that the other two parameters make no contribution to output ripple and noise. For example, you calculate the values of C_{MIN} by assuming that all ripple is due to the capacitance. In practice, it's best to increase the capacitor's value to minimize its contribution to output ripple. In some cases, you'll need much more capacitance to stabilize the power-supply control loop. In these instances, you should use a lower-value, high-performance output filter capacitor in parallel with a higher-value tantalum or electrolytic capacitor to provide loop stability.

Surface-mount techniques provide the answer

For very-high-frequency SMPSs that operate at 1 MHz and higher, maximum total inductance values will be in the 1- to 2-nH range, so you'll have to surface-mount components and RF layout techniques. However, don't assume that you can locate a few capacitors along with transistors, diodes, resistors, and inductors on a substrate that has a ground plane everywhere and expect the circuit to work reliably.

Practical size limitations prohibit you from directly mounting MLC chips larger than 2225 types (0.22×0.25 in.) directly on a substrate. Even 1812-type (0.18×0.12 in.) chip capacitors will have solder joint failures due to mechanical fatigue after about 1500 0 to 85°C thermal cycles on FR-4 substrates, and about 3000 −55 to +125°C cycles on alumina substrates. This fatigue is due to the difference between the CTE (coefficient of thermal expansion) between MLCs and the substrate materials used in hybrids and surface-mount assemblies. These substrate materials have a wide range of CTEs (**Table 1**).

This CTE difference translates into mechanical stress that's due to the linear displacement between substrate and component. Linear displacement is a function of ΔCTE ($CTE_{SUB}-CTE_{COMP}$) and the overall length of the component. Even with a small Δ, long components or substrates will have large linear displacements, which will cause high stress (and fatigue) in the solder joints after a few temperature cycles.

You must use lead frames on larger capacitor sizes (greater than 2225 types) to minimize mechanical stress on the solder joints during temperature cycling—a normal operating condition for power supplies. Failing solder joints increase both ESL and ESR, which increases ripple, noise, and heat, and accelerates failure.

You also have to use effective dams on the solder lands to ensure that molten solder does not migrate from the land during the reflow operation. Such a migration can lead to opens or weak solder joints. Because of stringent inductance requirements, you cannot use low-frequency layout techniques (such as necked-down conductors) for high-frequency output filters.

Adding lead frames has a small impact on component inductance, but this is the price you have to pay for reliable operation over temperature. **Fig 3** shows typical lead-frame inductance increases for two lead-standoff distances vs the number of leads along one side of capacitors that are specifically designed for switching power supplies that operate at 1 MHz or above. Actual inductance will be somewhat less because the lead frames flare out from the lead where they attach to the capacitor body. **EDN**

TABLE 1—CTEs OF TYPICAL COMPONENTS AND SUBSTRATES

MATERIAL	CTE (PPM/°C)
ALLOY 42	5.3
ALUMINA	≈7
BARIUM TITANTE CAPACITOR BODY	9.5-11.5
COPPER	17.6
COPPER CLAD INVAR	6-7
FILLED EPOXY RESIN	18-25
FR4/G-10 PC BOARD (X,Y)	≈18
NICKEL OR STEEL	15
POLYIMIDE/GLASS PC BOARD (X,Y)	≈12
POLYIMIDE/KEVLAR PC BOARD (X,Y)	≈7
TANTALUM	6.5
TIN LEAD ALLOYS	≈27

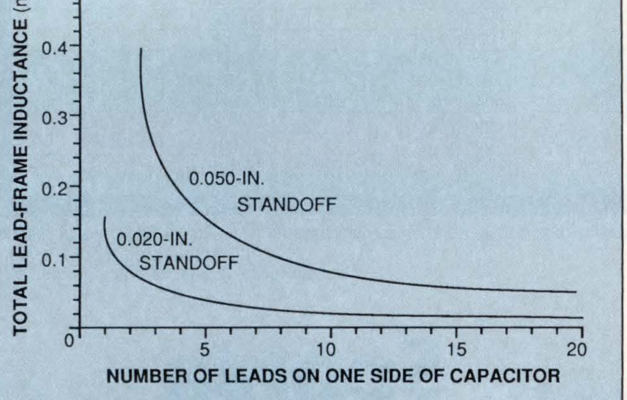

Fig 3—Adding lead frames has a small impact *on component inductance, but that's the price you have to pay for reliable operation over temperature.*

Author's biography

John Maxwell is a new product development manager at AVX Corp (Colorado Springs, CO). In this position, he coordinates market and technical requirements for new electronic ceramics, with an emphasis on surface-mountable devices. John holds BSEE and MSEE degrees from Oklahoma State University. In his spare time, he is involved in competitive pistol shooting, and he collects machine guns.

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	MC68HC11	DIP48P	○	
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	HD6301X/6303X, HD63701X	SDIP64P	○	
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	HD6305U/V, HD63705V	DIP40P	○	
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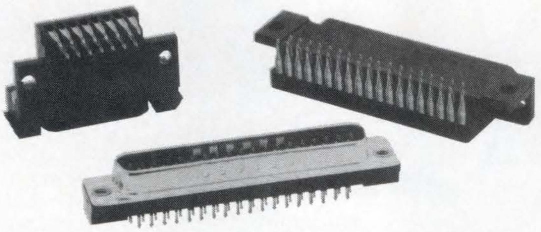

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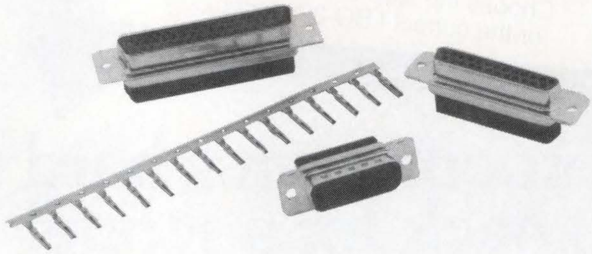

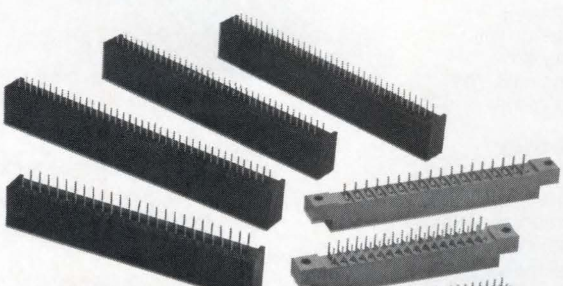

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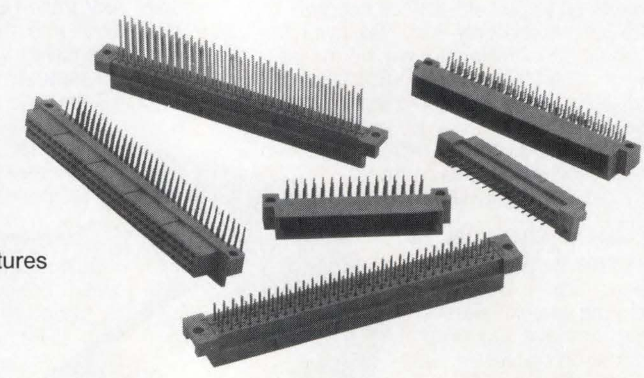

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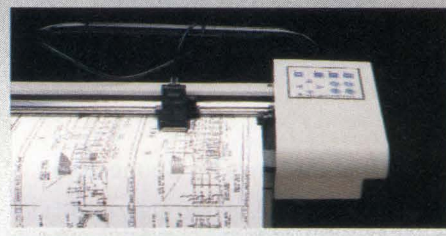

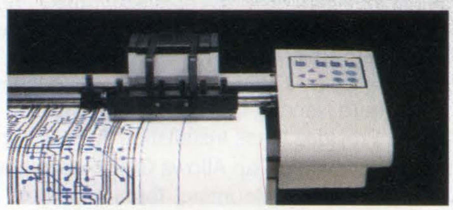

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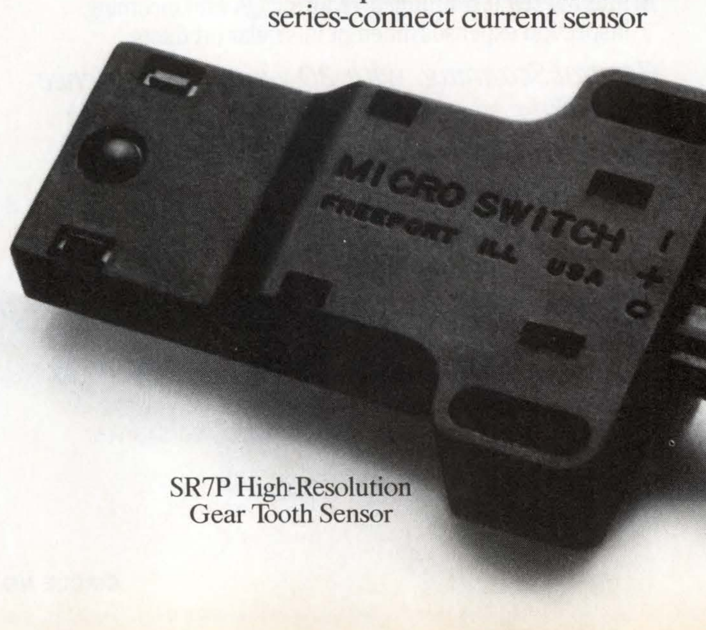
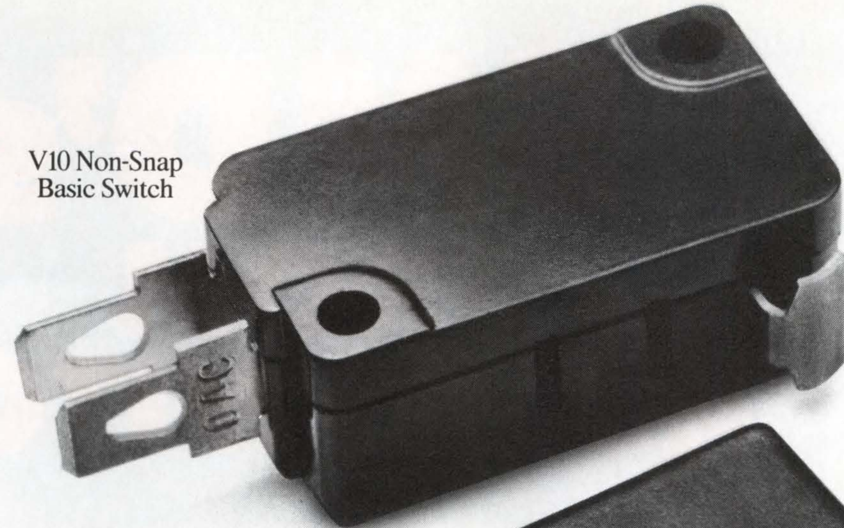


SR7P High-Resolution Gear Tooth Sensor



V10 Non-Snap
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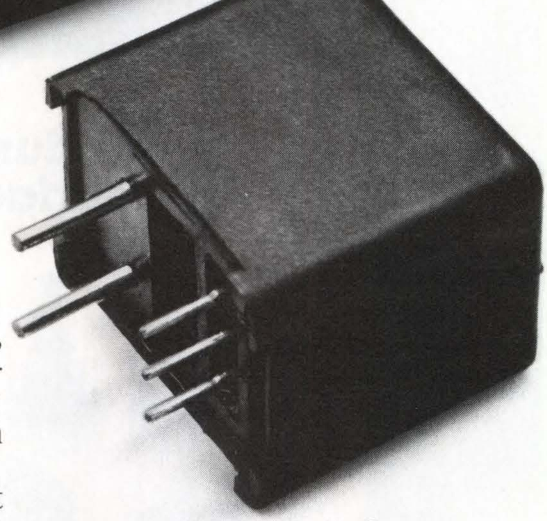

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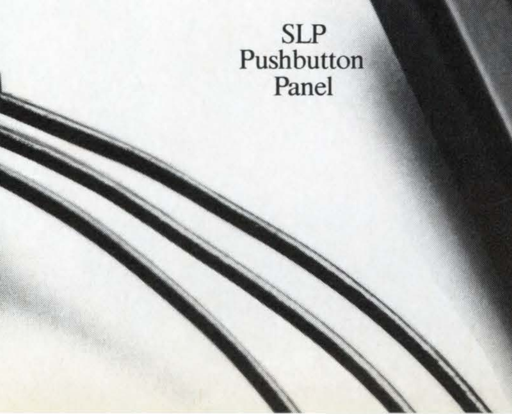

SLP
Pushbutton
Panel

Alternative computer architectures reduce bottlenecks

The Von Neumann architecture is no longer the architectural mainstay of the computer world. Although pipelining techniques improve upon a Von Neumann machine's performance, combining pipelining with one of the newer architectures or topologies will prove to be far more effective.

James W Hess, *Ohmeda*

For decades, the Von Neumann architecture has dominated the computer field, but an architecture of this type doesn't permit parallel processing. Today's computers need to operate in parallel to avoid bottlenecks and to achieve the higher rates of performance that future applications will undoubtedly call for.

Fig 1a illustrates a traditional SISD (single instruction, single data stream) Von Neumann CPU. The program counter keeps track of where the computer is in the program. To initiate an instruction cycle, the CPU places the address in the program counter on the address bus via the address buffer. The instruction latch latches the instruction returned by the memory. The decode and control logic decodes the instruction and generates the control signals, which effect the instruction execution.

After the instruction fetching and decoding is complete, the CPU sends out the address of the first data operand needed for the instruction, which it has stored in an internal register (**Fig 1b**). The CPU also stores the operand returned by the memory within an internal register. Next, it presents the address of the second operand through the address buffer. This address can be a part of the instruction itself, or it may also reside in an internal register.

Once both operands are in the possession of the CPU, it performs the instruction and temporarily stores the result of the operation in an internal register. The CPU then retrieves the storage address for the resultant from another internal register and places that address on the address bus, finally storing the result off-chip. It places the next instruction's address on the address bus, and the next instruction cycle begins.

A pipelined computer reduces bottlenecks

Computers with a Von Neumann architecture are prone to bottlenecks because a single bus handles the fetching of both instructions and data. In the example in **Fig 1**, assuming all data operands are stored in memory, a single instruction requires a total of 10 machine cycles.

Computer manufacturers have devised several methods of alleviating this bottleneck. One popular approach is pipelining. Generally, during the execution of an instruction, the CPU has to perform several operations that require several hardware sections. Actually the CPU can perform some of these operations at the same time, overlapping sections of different instructions.

Pipelined computers are very similar to Von Neumann machines except for the simple addition of latches between the functional blocks.

Pipelined computers are machines designed to execute different portions of different instructions at the same time. They are very similar to Von Neumann machines except for the simple addition of latches between the functional blocks (**Fig 2a**). When a computer latches a signal as the signal leaves a functional block, that functional block is then free for the next instruction to use. At the same time, the next functional block can operate on the latched signal.

A pipelined computer fetches its instruction and data

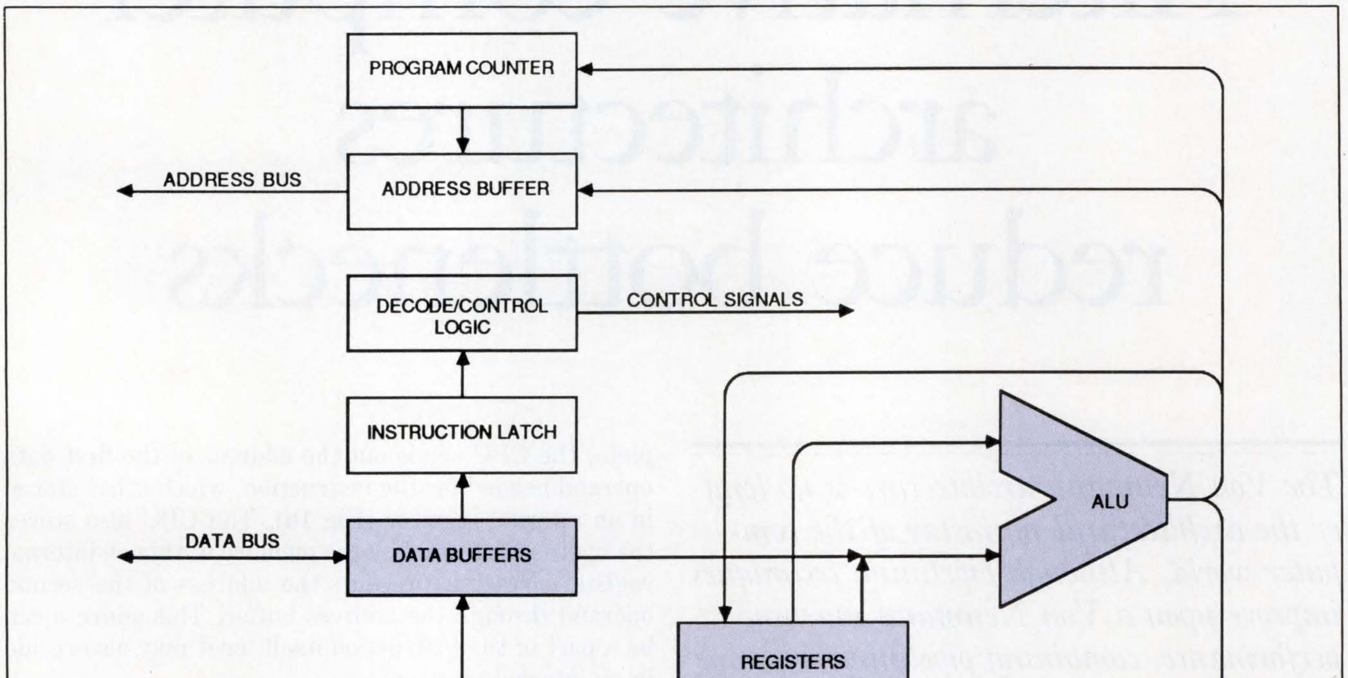

Fig 1—In a typical Von Neumann configuration (a), *the ALU has input paths from the registers and data buffers and feedback from the ALU output. In **b**—an illustration of the flow of instruction and data information for two instructions, A and B,—note that instruction A has to be complete before the next instruction, B, is even fetched.*

sequentially the way a Von Neumann computer does, but as it executes the first instruction, it also fetches the next instruction. This overlap between instruction fetching and execution allows the CPU to effectively fetch the next instruction using a "free" clock cycle. Also, while the CPU is executing the first instruction, it decodes the next instruction, eliminating the decode machine cycle of the second instruction. In this example, the pipelined computer requires seven cycles instead of the 10 that the Von Neumann computer in Fig 1

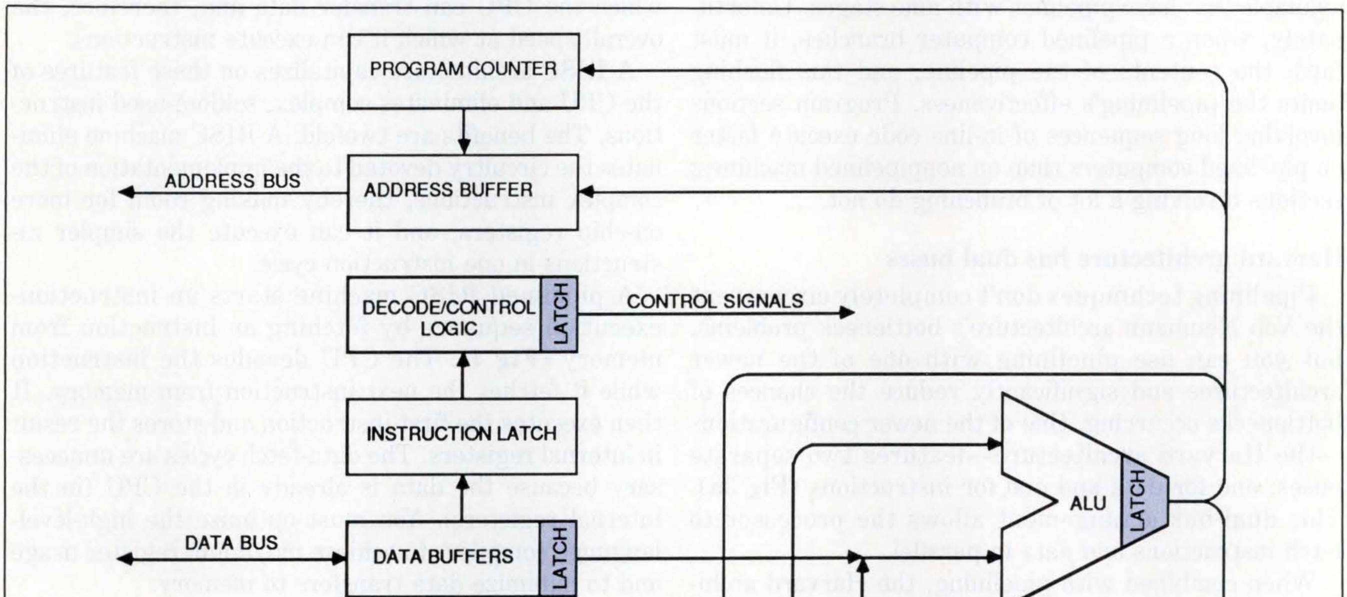

***Fig 2—To increase the throughput of a Von Neumann machine,** you can add latches to the control signals, data buffers, and ALU output (a). The latches allow the CPU to overlap the execution of an instruction with the fetch of the next instruction, which you can see in b's 3-instruction sequence.*

The Harvard architecture features two separate buses: one for data and one for instructions.

needs; it is also 1.4 times faster than the Von Neumann machine.

The simple computer illustrated in **Fig 2** is a 2-stage pipelined machine: It can perform operations on portions of two instructions at a time. Computers are available that have pipelines with nine stages. Unfortunately, when a pipelined computer branches, it must flush the contents of the pipeline, and this flushing limits the pipelining's effectiveness. Program sections involving long sequences of in-line code execute faster on pipelined computers than on nonpipelined machines; sections involving a lot of branching do not.

Harvard architecture has dual buses

Pipelining techniques don't completely circumvent the Von Neumann architecture's bottleneck problems, but you can use pipelining with one of the newer architectures and significantly reduce the chances of bottlenecks occurring. One of the newer configurations —the Harvard architecture—features two separate buses: one for data and one for instructions **(Fig 3a)**. This dual-bus arrangement allows the processor to fetch instructions and data in parallel.

When combined with pipelining, the Harvard architecture allows very efficient use of the computer hardware. A Harvard machine with two data buses and an instruction bus starts an instruction cycle by fetching an instruction **(Fig 3b)**. After decoding the instruction, the CPU fetches both data operands at the same time, one from each memory. It then executes the instruction and begins the next instruction fetch. As the CPU writes the results of the operation to one of the data memories, it simultaneously decodes the next instruction. In the ideal case, this instruction sequence requires five cycles instead of the Von Neumann computer's 10—a 100% improvement in execution speed.

A computer based on the Harvard architecture is an SISD machine like a traditional Von Neumann computer, but programming differences do exist. If a Harvard machine employs two separate memories for data storage, a programmer must make sure that separate operands for the same 2-operand instruction are stored in different data memories—otherwise the machine won't be able to take advantage of its parallelism.

RISC machine has more on-chip registers

The more internal registers the CPU has for data storage, the faster it can execute instructions; similar instructions that operate from main memory take much longer. Access times for on-chip registers are typically much shorter than those for main memory. In addition, a CPU often has separate read and write buses for the internal registers (resembling a Harvard machine in this respect), thus allowing multiple register accesses simultaneously. These features increase the speed at which the CPU can transfer data and, therefore, the overall speed at which it can execute instructions.

A RISC architecture capitalizes on these features of the CPU and eliminates complex, seldom-used instructions. The benefits are twofold: A RISC machine eliminates the circuitry devoted to the implementation of the complex instructions, thereby making room for more on-chip registers, and it can execute the simpler instructions in one instruction cycle.

A pipelined RISC machine starts an instruction-execution sequence by fetching an instruction from memory **(Fig 4)**. The CPU decodes the instruction while it fetches the next instruction from memory. It then executes the first instruction and stores the result in internal registers. The data-fetch cycles are unnecessary because the data is already in the CPU (in the internal registers). You must optimize the high-level-language compilers to achieve maximum register usage and to minimize data transfers to memory.

Topologies point the way

Although an improvement, RISC machines are still less than perfect. Like the architectures discussed previously, they use the SISD topology, executing a single instruction and processing a single piece of data at a time. The SISD topology limits processing power. Manufacturers are coping with this limitation by turning to interconnected multiprocessor systems—loosely coupled, networked topologies, tightly coupled systolic-array topologies, and MIMD (multiple instruction, multiple data stream) topologies.

A cluster of microcomputers linked together over a local-area network is an example of a very loosely coupled topology. In spite of the links, this topology is still basically an SISD type. Several computers linked together over a LAN can run different programs for different users concurrently, effectively providing a larger, faster computer, but this grouping of computers doesn't provide any performance advantage when it's operating on a single large program.

One example of a loosely coupled computer system is a master-processor-based system, in which the master processor sends commands to many slave processors operating independently of one another. Many robot systems use this type of topology. The master computer determines which motions each joint in a robot's arm should make and sends the appropriate commands to the processors controlling the individual joints. In a sense, all the processors in the system are operating on the same program, but the master processor directs the program flow.

At the other end of the spectrum are tightly coupled topologies. Rather than link processors loosely through

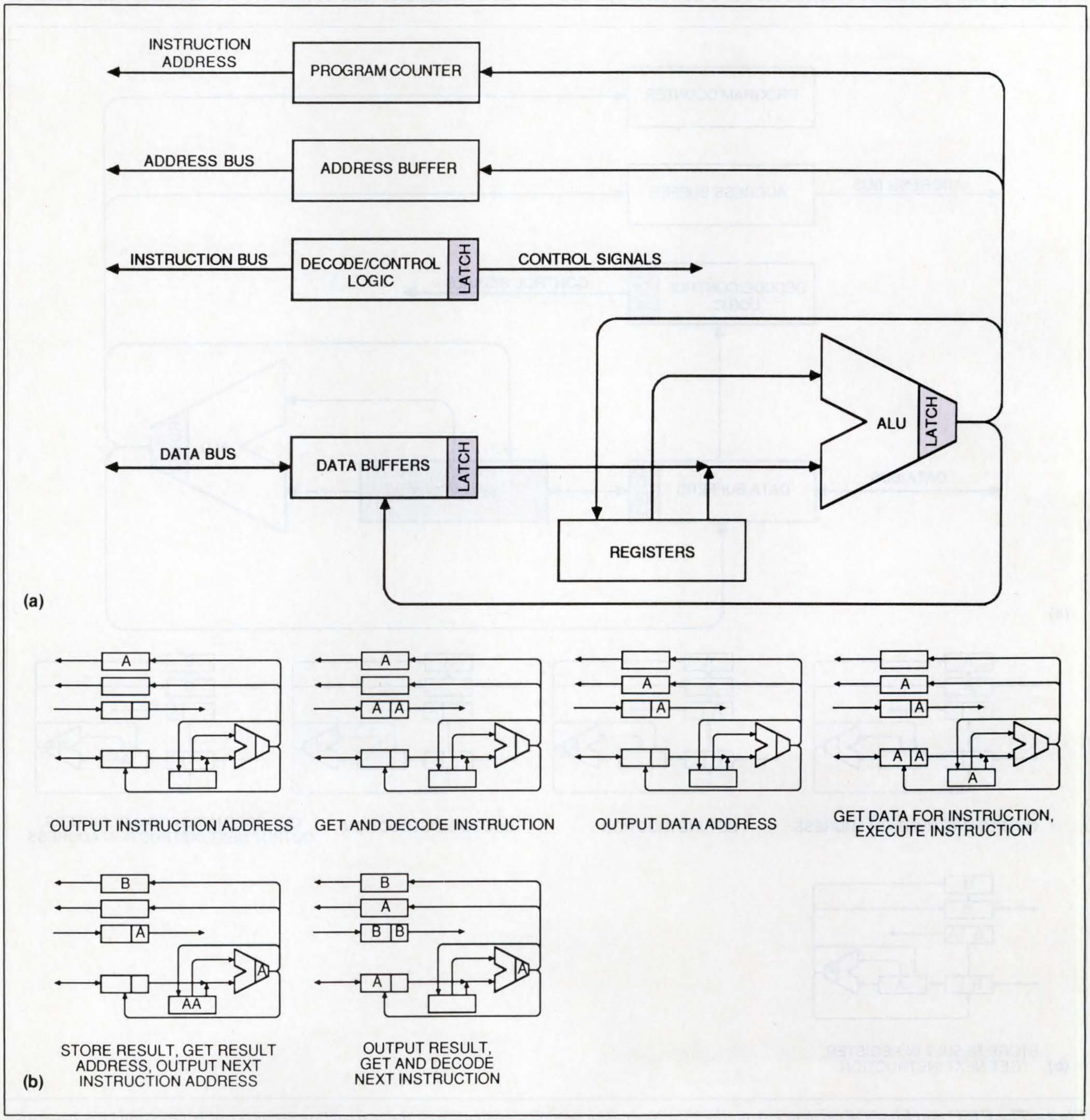

Fig 3—A pipelined Harvard processor, *in addition to providing latches for pipelined operation, comes with both an instruction bus and a data bus, allowing some degree of parallel operation.*

A RISC machine eliminates the circuitry needed to implement complex instructions, and it can execute the simpler instructions in one instruction cycle.

a network or other similar fashion, a systolic array groups individual processors, which are designed to operate in parallel on a program. An instruction cycle for a systolic array begins like that of any SISD computer; the processor fetches an instruction from the instruction memory. After the instruction is decoded, however, several or all of the processors in the array operate in parallel on the data required for instruction execution.

In contrast to the relatively straightforward task of

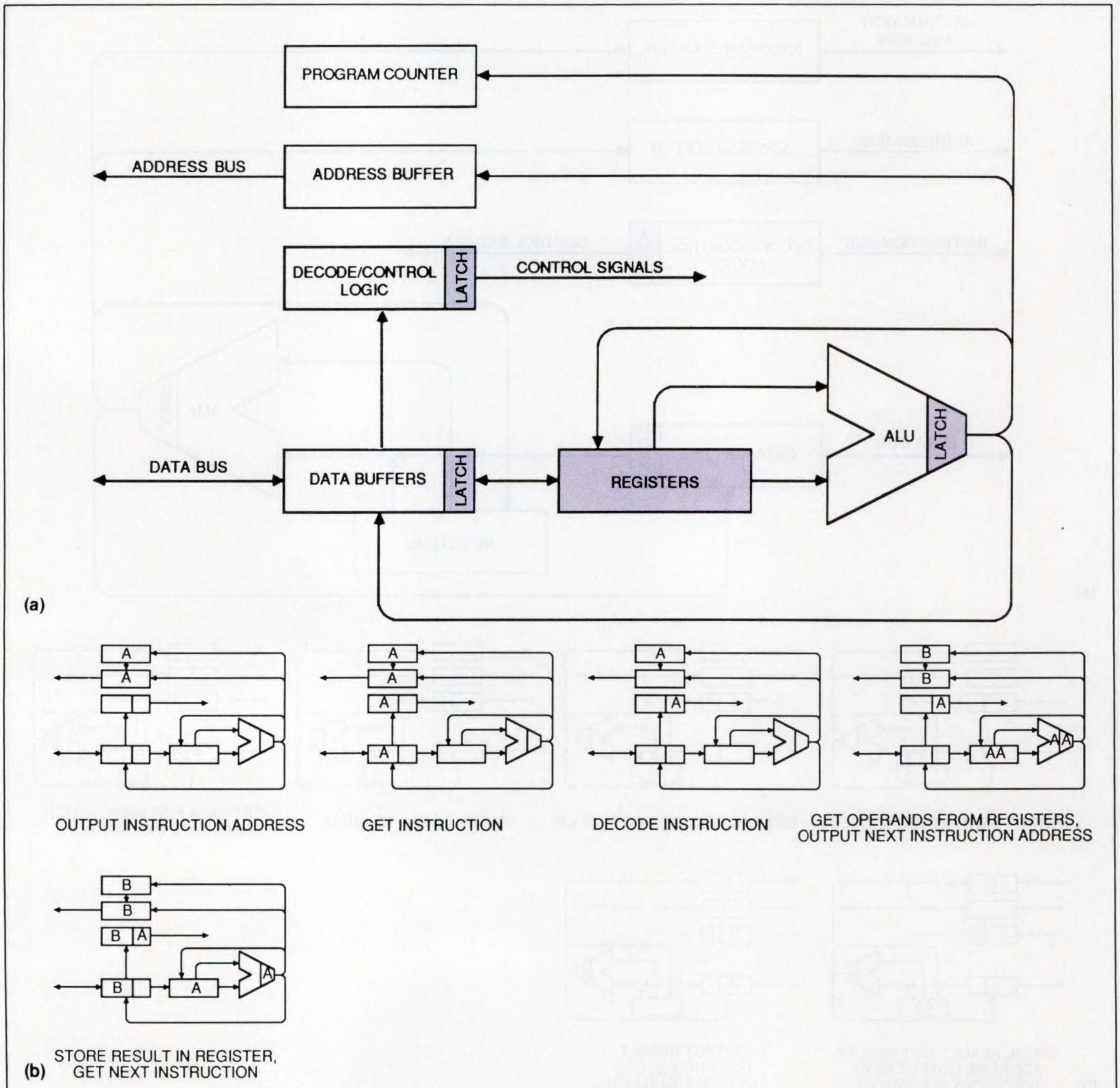

***Fig 4—The RISC machine's divergence** from the Von Neumann model is evident from the instruction sequence of **b**. Operands are generally available in on-chip registers **(a)** and results are stored there as well, resulting in better performance because of the faster accesses afforded by the on-chip registers.*

Code must match topology

Although higher-level languages are available for systolic-array processors, a programmer must write code that will run in parallel on the array's processors to take full advantage of the array's architecture. Specifically, a programmer must adapt sequential algorithms for parallel processing.

For example, if an array of processors is working on a problem such as

C=cosine(A)+sine(B),

the programmer might break the procedure up into three procedures, each running on a separate machine:

1) D=cosine(A),
2) E=sine(B),
3) C=D+E.

Procedure 3 must positively ensure that the first two procedures are complete before the third procedure begins.

One way to convert from sequential to parallel operation is to employ data-flow principles in the computer architecture. **Fig A** shows the three basic functional blocks of a data-flow computer. Tagged data flows from the execution unit to the associative memory. The I/O system monitors this flow for output data and inserts input data into the data stream. Data flows from the associative memory to the execution unit.

A cell in the associative-memory block contains an instruction latch, several data latches, a tag latch, and comparators. Each tag comparator monitors the data stream that flows into the associative memory. When a data tag flows by that matches the value of a tag comparator, the comparator signals the data latch, which then latches the data. The comparator also signals the instruction that this bit of data is available for processing.

When all the data necessary for this instruction is latched and available, the instruction and its data travel to the execution unit. The execution unit then operates on the data, tags the result, and inserts the tagged result into the data flow.

The data-flow approach makes programs parallel on an instruction-by-instruction basis. When an instruction has all the data it requires, the data travels to the execution unit; there is no predetermined instruction sequence. Multiple-execution units can execute multiple instructions simultaneously, just as long as the required data is available for the instruction.

Debugging these complex programs is significantly more difficult than debugging programs running on a single processor. Consider the following scenario, for instance. If a program is running on a sequential machine, and variable E is incorrect when procedure 3 accesses it, the programmer simply examines E in each procedure that ran before procedure 3 until he finds the cause for the incorrect value. In a processor array, however, the programmer has to examine all of the currently active and previously active processes to determine which process changed the variable to an incorrect one.

In some programs, many different processes may be capable of changing E, all of which run in parallel. The programmer must examine all of these processes and their interactions to determine where the error occurred. If the programmer steps through the procedure on one processor, the problem may disappear because part of the program would be executing at a slower rate than the rest of the program. This lack of concurrency compounds the difficulty of the debugging task. You can't simply look back in the program to find the code that is responsible for the error, as you can with a strictly sequential machine.

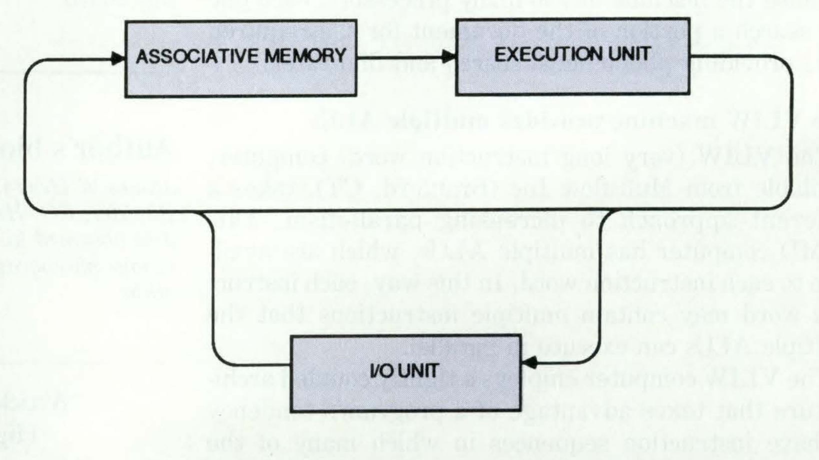

Fig A—Three basic units characterize a data-flow architecture: the execution unit, associative memory, and I/O unit (a). In the representation of the associative memory's internal organization (b), each instruction and each bit of data has a tag associated with it. After the comparator gathers all the data with the help of the tags, the instruction and data are all sent to the execution unit.

A systolic array groups individual processors, which are designed to operate in parallel on a program.

programming other types of processors, programming a systolic array is complicated (see **box,** "Code must match topology"). Because all the processors in the machine are executing the same instruction, a programmer must carefully route the data so that each instruction applies to all the data in the machine. This difficulty limits the systolic array to specialized applications. Such processors find use mostly in scientific and engineering work, especially in signal processing, image processing, and matrix operations; all of these involve repeated multiplication and addition.

An example of a commercially available machine that uses a systolic-array topology is the Connection Machine from Thinking Machines (Boston, MA). The Connection Machine's 65,536 single-bit processors are connected in a 16-dimensional hypercube configuration. Each single-bit processor has 4k bits of memory, and communications hardware allows message passing between any two processors. The tightly coupled architecture allows a programmer to dynamically configure the machine to suit the particular application that's running.

According to the manufacturer, the Connection Machine can process 2- and 3-dimensional images 1000 times faster than more conventional computers of the same complexity. A valuable business application for such a machine is searching for text in document files. Because the machine has so many processors, each one can search a portion of the document for the required text, providing phenomenal search and find rates.

The VLIW machine provides multiple ALUs

The VLIW (very long instruction word) computer, available from Multiflow Inc (Branford, CT), takes a different approach to increasing parallelism. This MIMD computer has multiple ALUs, which are available to each instruction word. In this way, each instruction word may contain multiple instructions that the multiple ALUs can execute in parallel.

The VLIW computer employs a tightly coupled architecture that takes advantage of a program's tendency to have instruction sequences in which many of the instructions aren't directly dependent on each other. For example, the equation

$$A=\text{sine}(B)+\text{cosine}(C)$$

requires that the transcendental functions sine(B) and cosine(C) operate first, before the addition. Because the data necessary for these two operations (sine(B) and cosine(c)) is independent, the two operations can run simultaneously.

Sophisticated compilers running on the VLIW machine partition programs, written in conventional languages such as C, into operational chunks that the separate ALUs can then execute. Program development for the VLIW computer is essentially the same as for traditional SISD computers, providing that the applications programmers use the high-level languages that the manufacturers supply.

A final example of a commercially available machine with a highly parallel topology is BBN's (Cambridge, MA) Butterfly. An array of MC68000 processors connect in a switching-system topology similar to the butterfly configuration that fast Fourier transforms use for moving data.

The Butterfly can have as many as 256 processors, each with its own memory and I/O. Each processor can directly access all the memory in the system: Each accesses local memory conventionally but performs remote-memory accesses using packet-switching techniques. A processor serializes off-board memory-read requests and then sends the address and read status to a switch. The switch sends the information to either the next switch or the addressed board. When a board receives a packet, it responds by getting the data from its memory, serializing it, and sending it to the requesting board. **EDN**

Author's biography

James W Hess is a research engineer with Ohmeda in Boulder, CO. He adapts existing products for use by OEMs. Jim obtained his BSE degree from Walla Walla College and enjoys photography and working in preteen and early-teen clubs.

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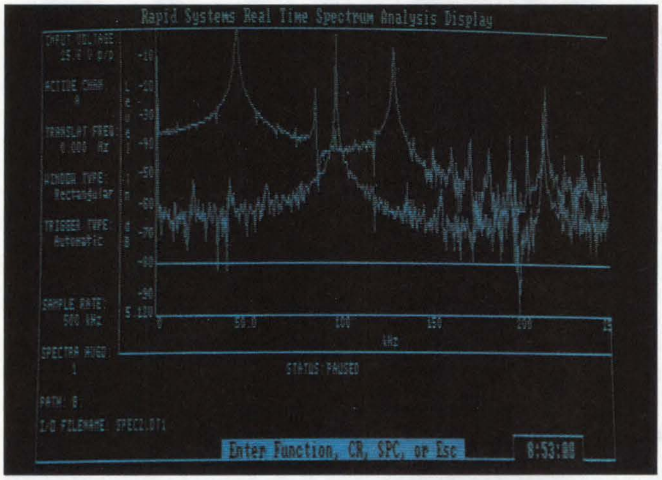

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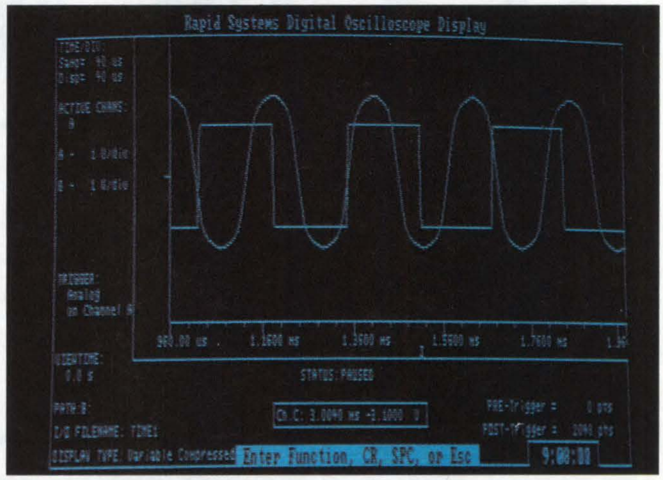

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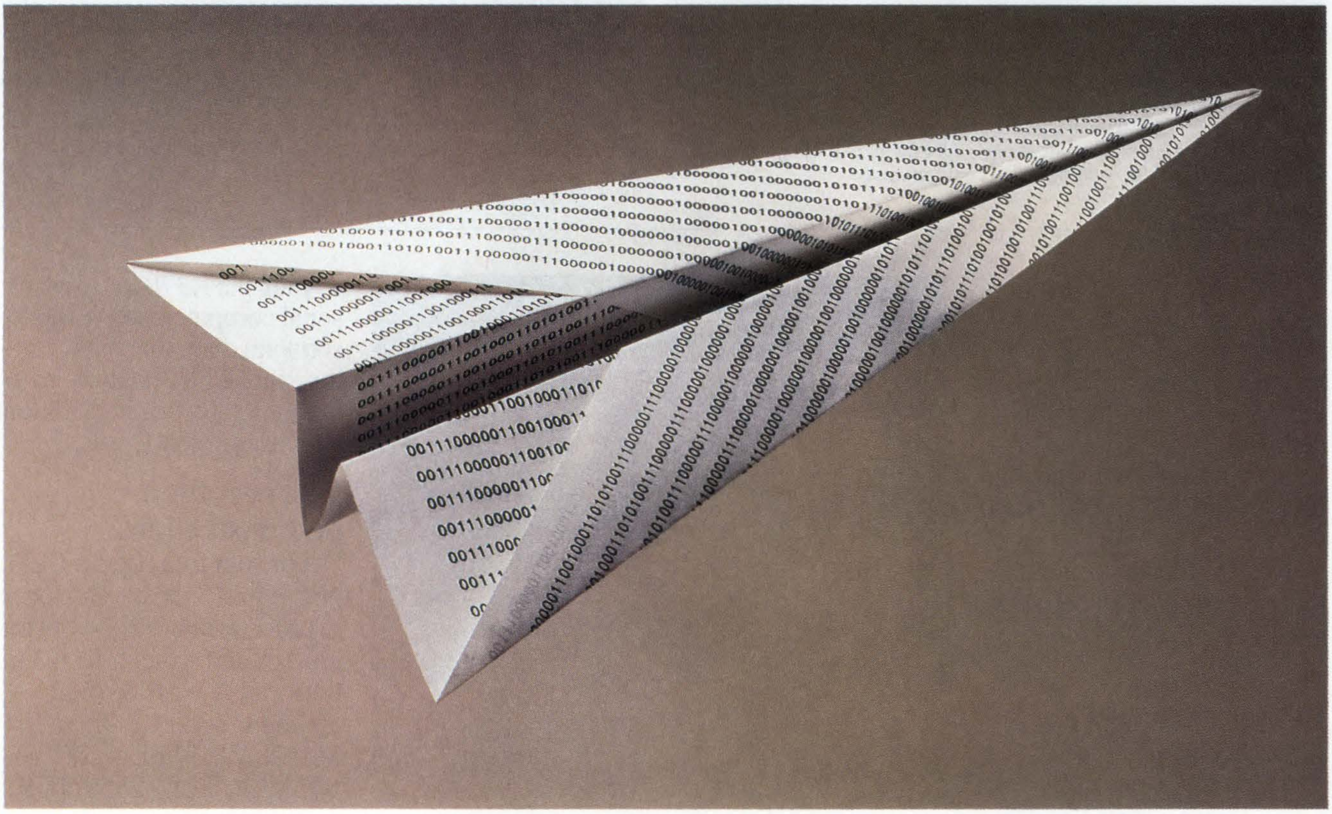

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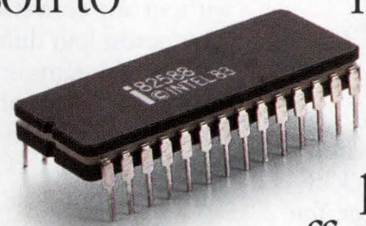

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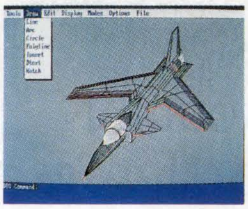

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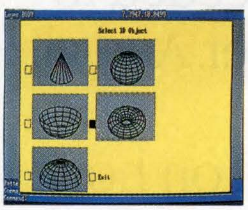

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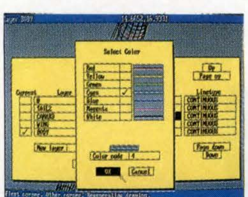

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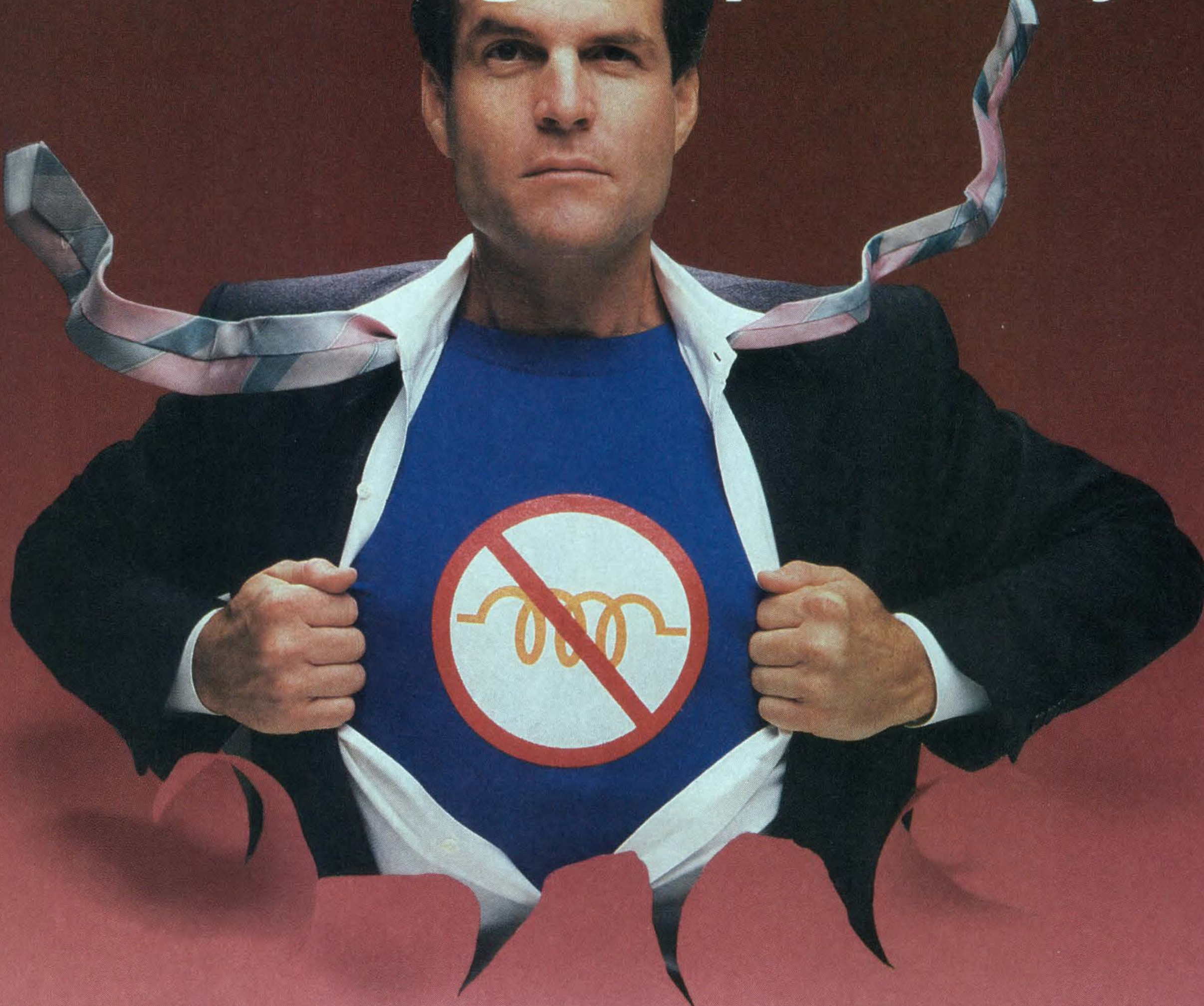

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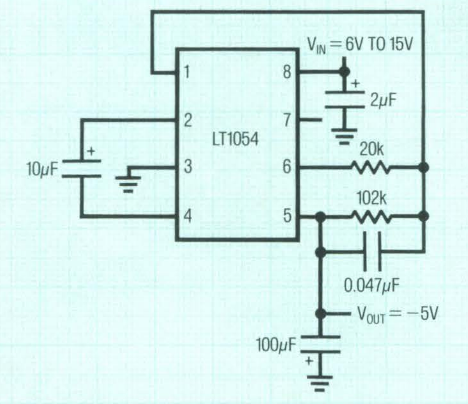

The LT1054 is ideal for use in a wide variety of applications where a supply voltage is needed that is either higher, lower, or of a different polarity than what is available.

LT1054 is pin-compatible with switched capacitor voltage converters such as LTC1044 and ICL7660, and it comes in 8-pin plastic or ceramic DIP configurations. Military versions are also available.

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DESIGN IDEAS

EDITED BY TARLTON FLEMING

Transmission gate improves clock driver

Terje Kvinge
EB NERA, Bergen, Norway

Data latches within a CMOS digital IC require biphase clock signals (OUT and $\overline{\text{OUT}}$ in **Fig 1**) whose nearly simultaneous transitions are unaffected by the output load. The basic circuit shown in **Fig 2a,** for example, has outputs separated by a time interval of one gate delay **(Fig 3).** This circuit's increasing time skew vs load can cause false latching.

You can eliminate the load-variable time skew by adding a third inverter gate **(Fig 2b),** but the outputs of this circuit also remain separated by a 1-delay interval. (Adding a noninverting buffer to **Fig 1a's** $\overline{\text{OUT}}$ output doesn't solve the problem. The noninverting buffer—two inverters in cascade—has a 2-gate delay, which again causes a 1-gate delay between the driver's outputs.)

The optimum driver circuit **(Fig 2c)** has a forced (permanently on) transmission gate in the signal path. Delay through the transmission gate is more than half that of an inverter, resulting in less than one-half of a gate delay between the clock-driver outputs.

Because the transmission gate is bidirectional, its output signals can feed back to the input and disrupt the clock driver's operation. To avoid this problem, drive the circuit with an inverter or an AND gate—never with a flip-flop or an OR gate. (Higher carrier mobility gives an n-channel transistor better drive capability than that of a p-channel transistor. Because OR gates have two p-channel transistors in series (vs the AND gate's two in parallel), an OR gate has a lower noise margin and slower low-to-high transitions.) **EDN**

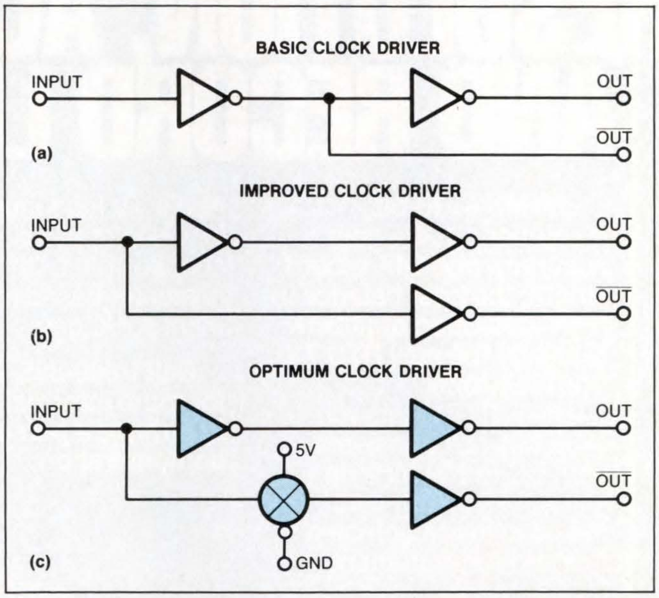

*Fig 2—**These are alternative circuit configurations** for a biphase clock driver. Output skew for these digital CMOS circuits is illustrated in **Fig 3**.*

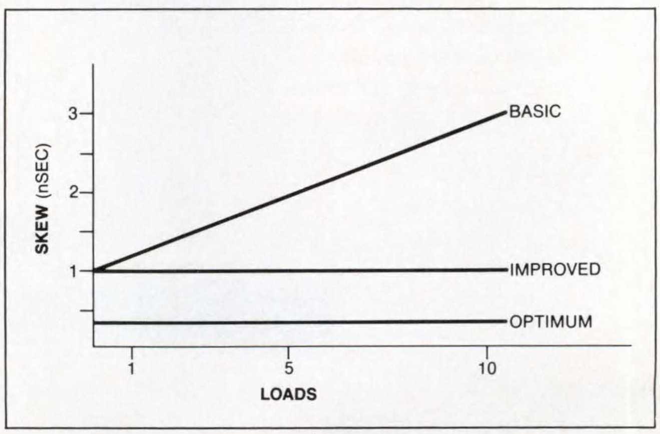

*Fig 3—**This graph of output load vs output time skew** shows that **Fig 2c's** optimum circuit exhibits skew that is small and independent of load.*

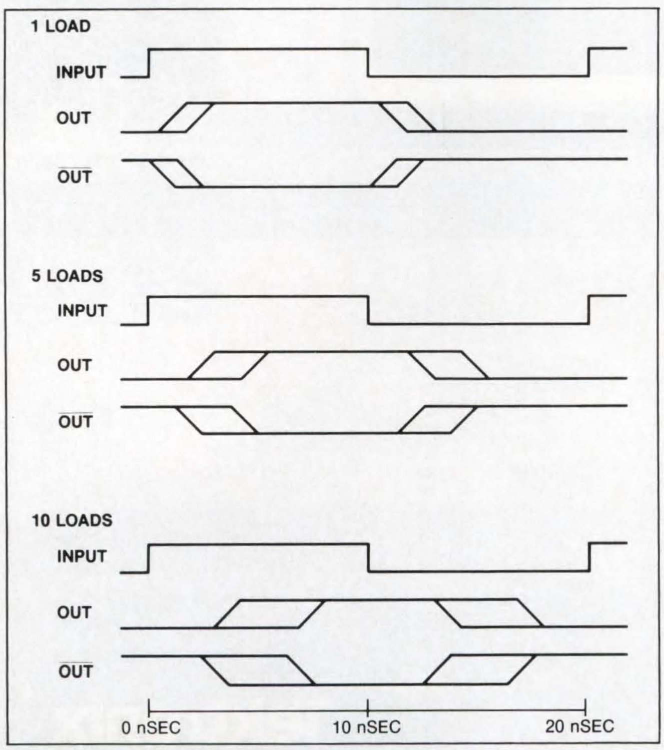

*Fig 1—**These waveforms show the effect of loading** on the optimum clock driver circuit of **Fig 2c**.*

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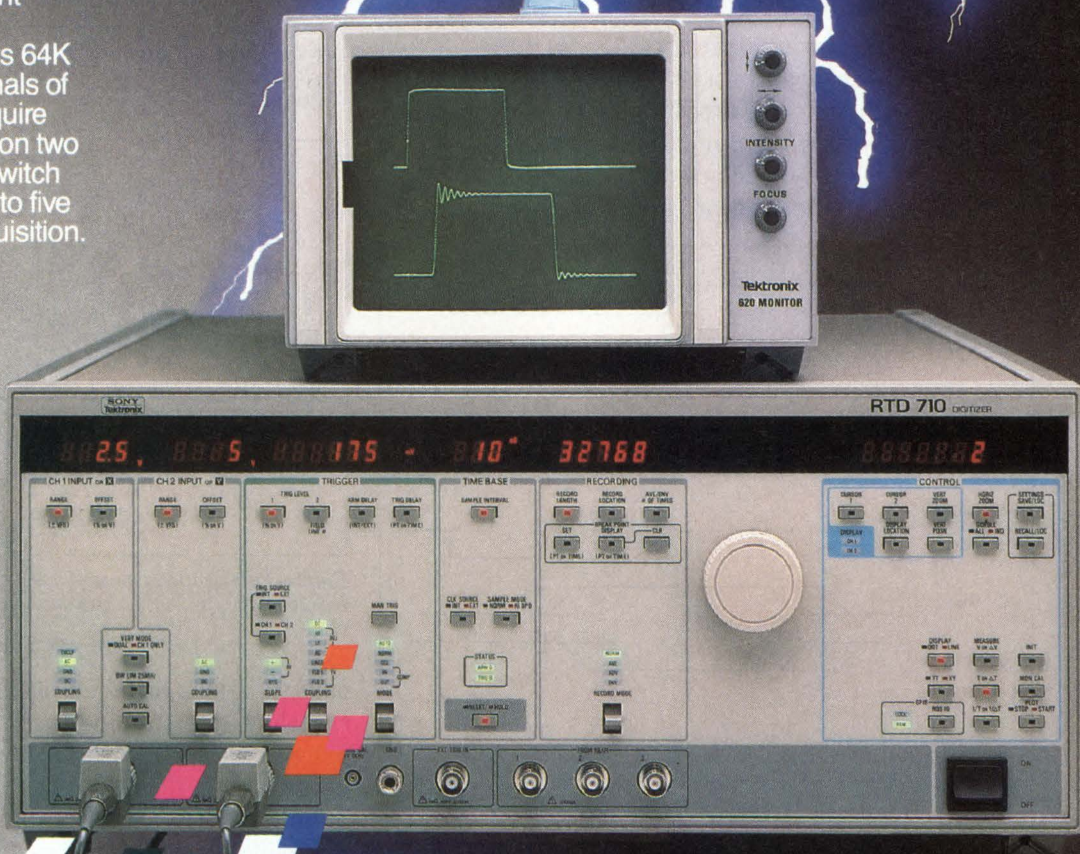

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Op-amp current mirror drives load current

Sandro Centro
University of Padova, Padova, Italy

In the programmable pulse-width generator shown in **Fig 1**, a general-purpose op-amp current mirror (R_2, R_3, and IC_2) allows a current-output D/A converter to deliver current (I_L) to a load. The load in this case is the timing capacitor of the one-shot multivibrator IC_3.

The circuit's output pulse width is a linear function of the digital input D, within accuracy limits imposed by the components used. You must set a minimum value for I_L to assure operation of the one-shot, either by grounding some D/A-converter inputs, as shown, or by adding a resistor in parallel with C_1. **EDN**

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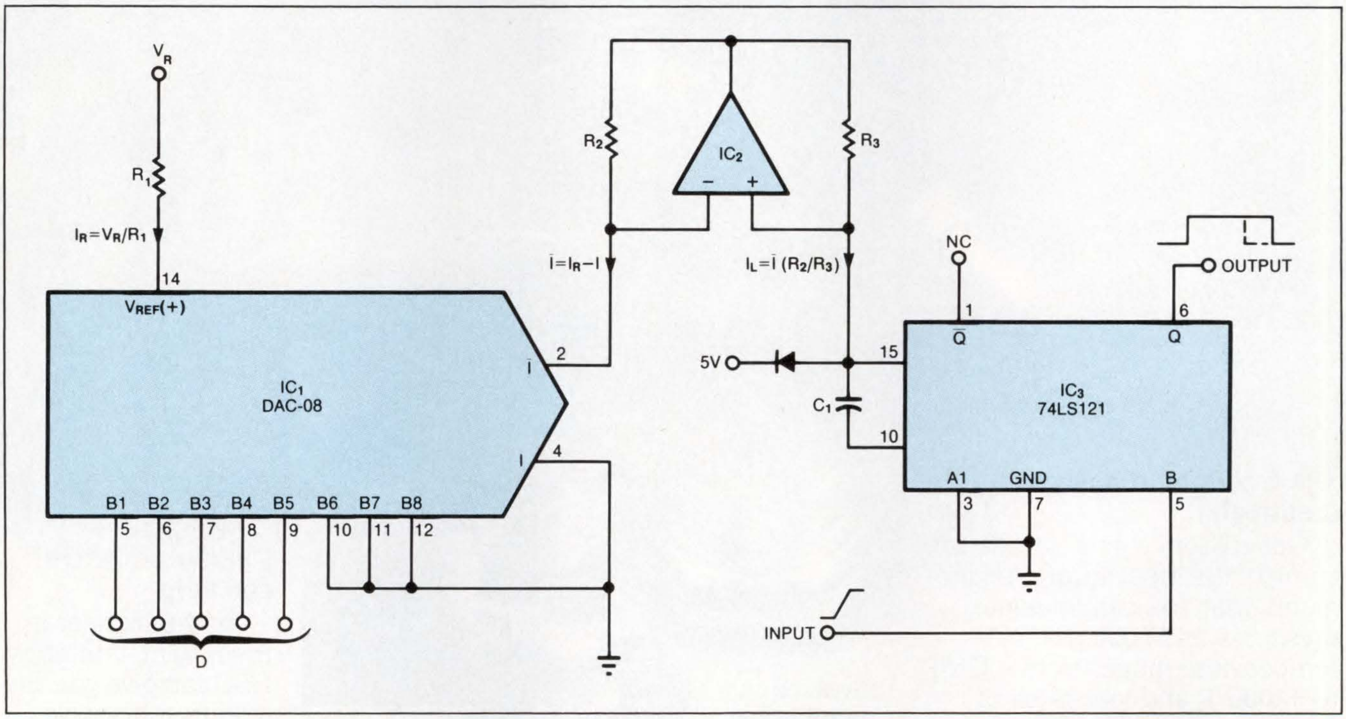

*Fig 1—**Op amp IC_2 mirrors the D/A converter's** output current to the timing capacitor of one-shot IC_3, providing digital control of the one-shot's output pulse width.*

Phase shifter uses digital techniques

Albert Helfrick
Dowty RFL Industries, Boonton, NJ

The **Fig 1** circuit produces a digitally selected phase difference between two sine waves of equal amplitude and frequency (outputs A and B). You set a discrete phase increment by selecting one or more of the quantities 2, 4, 8, 16, 32, 64, and 128° (coarse setting) plus one or more of the quantities 1, ½, ¼, and ⅛° (fine setting). The circuit creates these outputs by first generating a precise phase relationship between two square waves and then filtering each to remove all but the fundamental frequency component.

Because the switched-capacitor filters are sampled-

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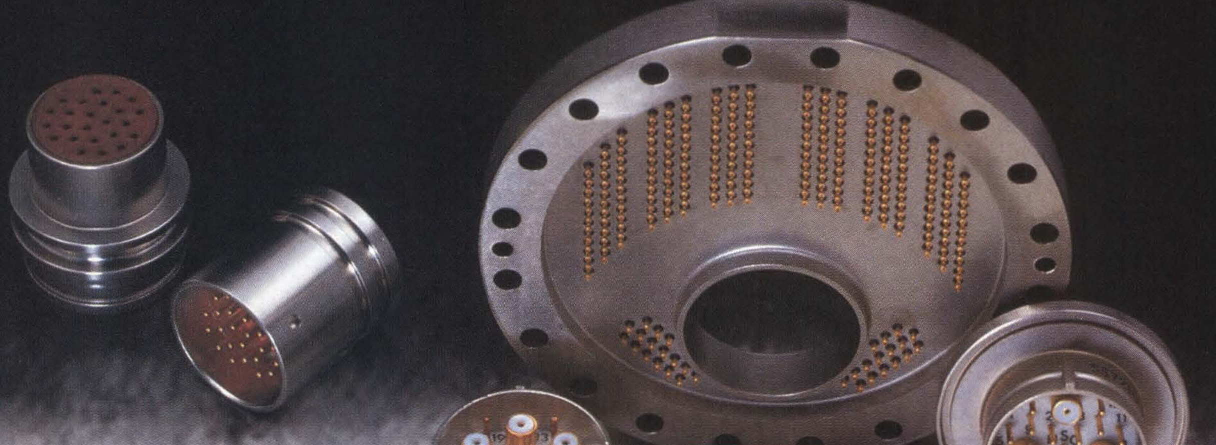

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data devices (IC_5 and IC_6), they can't recognize phase increments equivalent to a time interval less than the filter's clock period. For the circuit shown, this period equals the output period divided by 180, or 2° in terms of phase. (The filter chips—6th-order, lowpass Butterworth types—internally fix the ratio of clock-to-cutoff frequency at 100. The cutoff frequency is 1.8 times the filter's input frequency, so the clock-to-input ratio is 180.)

You establish the 2° coarse-phase resolution by providing an input clock frequency 2880 times the desired f_{OUT}. Counter IC_1 then divides this input by 16, producing the $180f_{OUT}$ system-clock signal.

To obtain finer resolution (below 2°), the 4-bit, presettable counter IC_2 lets you introduce a phase difference between the filters' clock signals. This method provides ⅛, ¼, ½, and 1° phase increments; for finer resolution you could substitute an analog approach for introducing the phase.

The sinusoidal filtered-square-wave outputs A and B have low distortion (about −60-dB THD) and well-defined characteristics of frequency and phase. You must add lowpass filters to the A and B outputs, however (not shown); without filtering, the outputs exhibit about −25-dB THD. Each filter chip includes two uncommitted op amps for constructing the lowpass filters. EDN

To Vote For This Design, Circle No 749

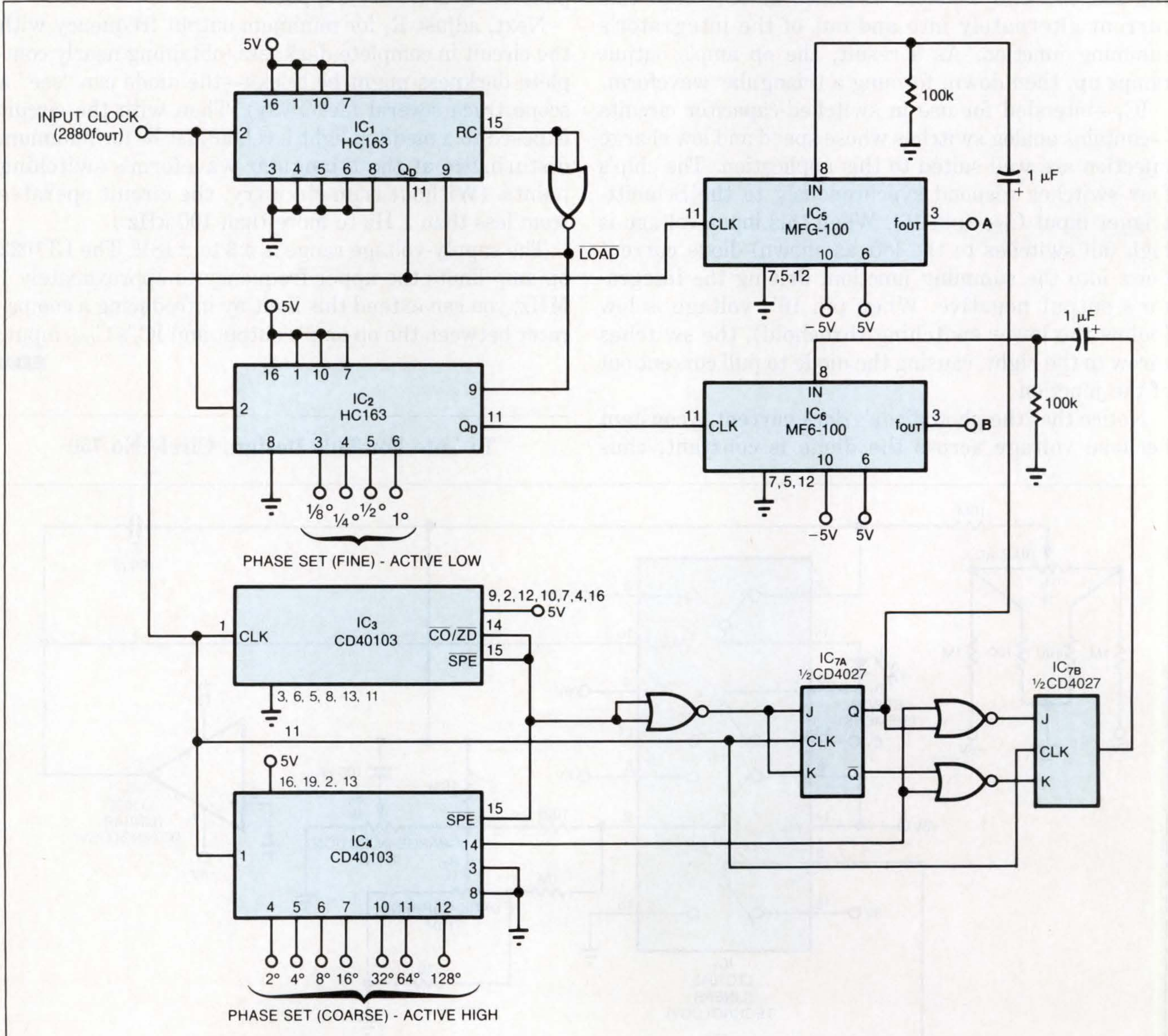

__Fig 1—By extracting the fundamental components__ from two digitally synthesized square waves, this circuit produces two constant-amplitude sine waves with a programmable phase difference.

Current-to-frequency converter spans 140 dB

Steven E Sarns
Vesta Technology Inc, Wheatridge, CO

The circuit of **Fig 1** converts a photodiode's current into frequency, producing an output that ranges from 0.1 Hz to 1 MHz. Conversion is reasonably linear from below 0.1 Hz to 100 kHz; it becomes nonlinear above 100 kHz.

Capacitor C_1 and the op amp form an integrator. Ambient light induces current flow in the photodiode D_1, and the two topmost switches in IC_1 route this current alternately into and out of the integrator's summing junction. As a result, the op amp's output ramps up, then down, forming a triangular waveform.

IC_1—intended for use in switched-capacitor circuits—contains analog switches whose speed and low charge injection are well suited to this application. The chip's four switches respond synchronously to the Schmitt-trigger input C_{OSC} (pin 16). When this input voltage is high (all switches to the left as shown) diode current flows into the summing junction, driving the integrator's output negative. When pin 16's voltage is low (below the lower switching threshold), the switches throw to the right, causing the diode to pull current out of the junction.

Notice that the photodiode's dark current is constant because voltage across the diode is constant, thus allowing cancellation via the R_2 trim network. R_3 lets you compensate for charge injection in the switches, and the R_1 network lets you trim the error due to bias current at the op amp's inverting input. The lower switch provides a TTL-compatible output.

To calibrate the circuit, replace the ±6V supplies with ±100-μV sources and replace the photodiode with a 10-MΩ resistor. Adjust R_1 for a symmetrical triangular output from the integrator, and then reinstall the photodiode and ±6V supplies.

Next, adjust R_2 for minimum output frequency with the circuit in complete darkness (obtaining nearly complete darkness might be tricky—the diode can "see" a scope trace several feet away). Then with the circuit exposed to a medium light level, adjust R_3 for minimum disturbance at the triangular waveform's switching points. (Without trim circuitry, the circuit operates from less than 1 Hz to more than 100 kHz.)

The supply-voltage range is ±3 to ±18V. The LT1022 op amp limits the upper frequency to approximately 1 MHz; you can extend this limit by introducing a comparator between the op amp's output and IC_1's C_{OSC} input.

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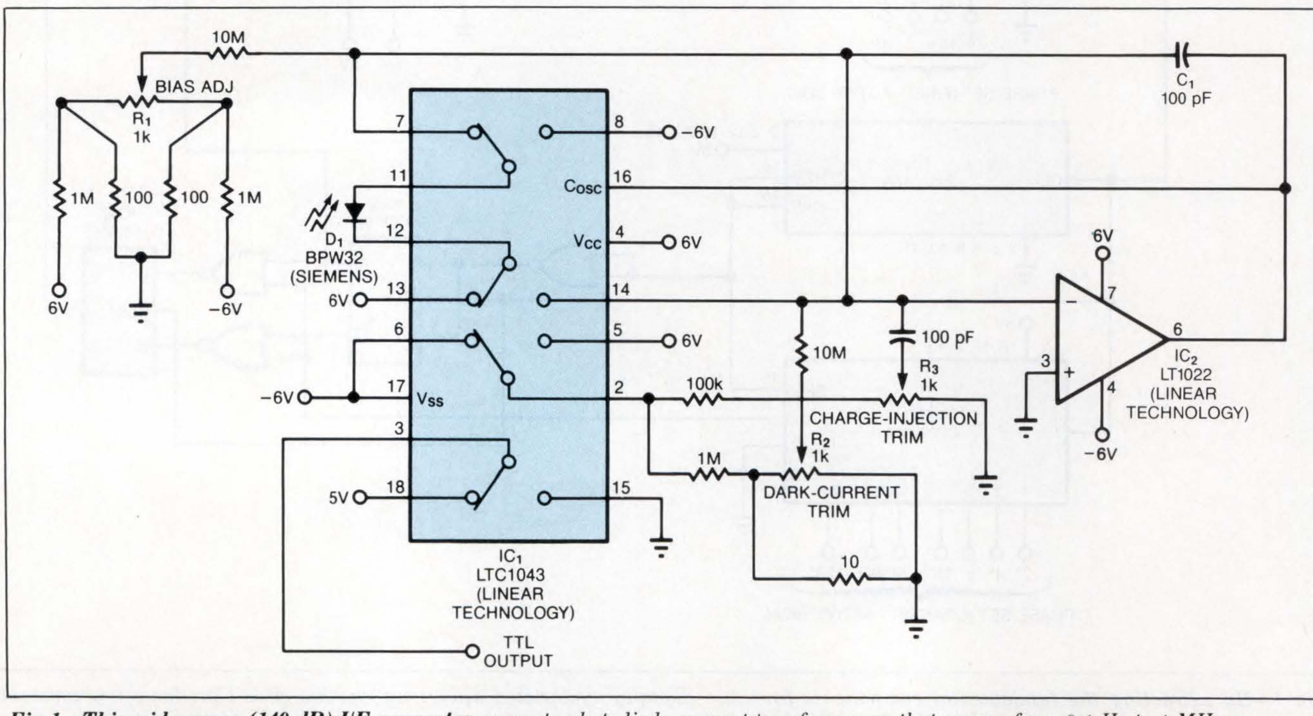

Fig 1—This wide-range (140-dB) I/F converter *converts photodiode current to a frequency that ranges from 0.1 Hz to 1 MHz.*

Step-up converter produces 5V from 1.5V

Gerald Grady
Maxim Integrated Products, Sunnyvale, CA

You can produce a regulated 5V output from a 1.5V battery cell by using the step-up dc/dc-converter circuit shown in **Fig 1.** The circuit can operate with V_S as low as 1V, but it requires at least 1.5V to start. The output can deliver 100 mA when V_S is 1.5V or 1.7A at 70% minimum efficiency when V_S is 3V.

Supply voltage for the switching regulator IC_1 appears first at pin 4 (start-up mode) and then at its own V_{OUT} terminal, pin 5. The chip includes an oscillator, bandgap reference, three voltage comparators, a catch diode, and associated control circuitry. An internal MOSFET lets you implement low-power applications; higher power calls for an external device: Q_1 in **Fig 1.** The on-chip oscillator provides a 55-kHz square-wave drive to both the internal and external MOSFET.

When Q_1 turns off, current through inductor L_2 drives the drain-node voltage higher. Similarly, current through L_1 drives the voltage at pin 5 higher when the internal MOSFET turns off. This action generates two independent voltages, each higher than V_S. Q_1 and L_2 generate sufficient overhead voltage to enable the regulator chip to produce a regulated 5V output, and the internally generated voltage ensures adequate gate drive to Q_1. The internal voltage, clamped by the 10V zener diode D_3, ranges from 10V (turn-on) to 15V (normal operation). Q_1's resulting $R_{DS(ON)}$ is only 0.085Ω.

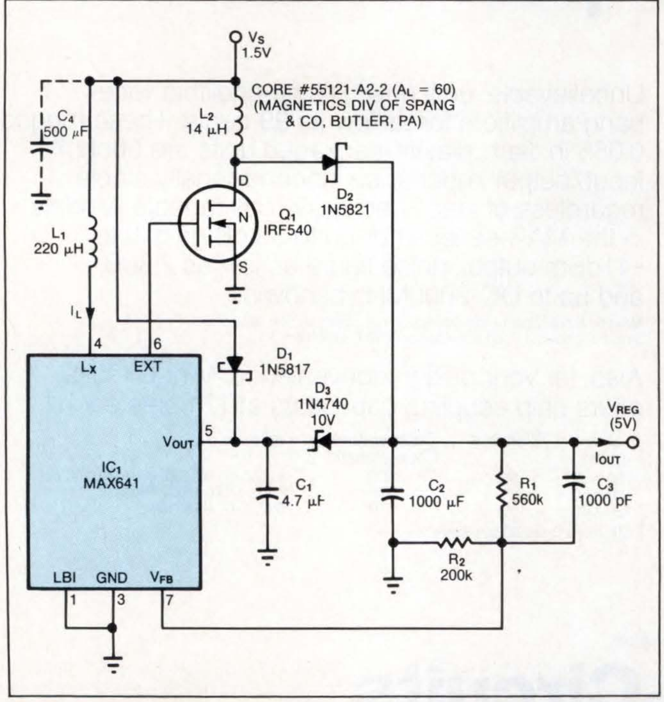

***Fig 1—This switching-regulator circuit** converts a dc input (as low as 1.5V) to a higher regulated value—to 5V, for example.*

TABLE 1—OBTAINABLE VALUES OF I_{OUT} MAX

V_S	L_2		
	14 µH	27 µH	50 µH
1.5V	105 mA	48 mA	30 mA
2.0V	220 mA	95 mA	60 mA
2.5V	390 mA	160 mA	100 mA
3.0V	1.75A	1.5A	1.25A

Resistors R_1 and R_2 determine the regulated output level. For V_{REG} outputs other than 5V, set

$$R_1 = R_2\left(\frac{V_{OUT}}{1.31} - 1\right).$$

You choose an R_2 value in the range from 10 kΩ to 10 MΩ.

For low values of V_S, losses in the internal and external diodes and the Q_1 inductor sharply limit the maximum output current. The following design equations let you determine component values while calculating this current. First, Q_1 must be able to handle the peak current I_{PK} of inductor L_2:

$$I_{PK} = V_S t_{ON}/L_2,$$

where $t_{ON} = 0.55/f_{OSC}$. For this circuit, then, $I_{PK} = 1.07A$.

The circuit loss V_{LOSS} is

$$V_{LOSS} = I_{PK}(R_{DS(ON)} + 2R_{L_2}) + V_{D_2},$$

where R_{L2} is the dc resistance of L_2 and V_{D2} is the forward voltage drop of D_2. For this circuit, $V_{LOSS} = 0.56V$. The output current is

$$I_{OUT} = \frac{0.5 L_2 I_{PK}^2 f_{OSC}}{V_{REG} - (V_S - V_{LOSS}) - I_{L_1}}.$$

Therefore, $I_{OUT} = 103$ mA for the circuit shown. **Table 1** shows the output currents you can obtain for various values of V_S and L_2. The corresponding conversion efficiencies range from 70 to 85%. **EDN**

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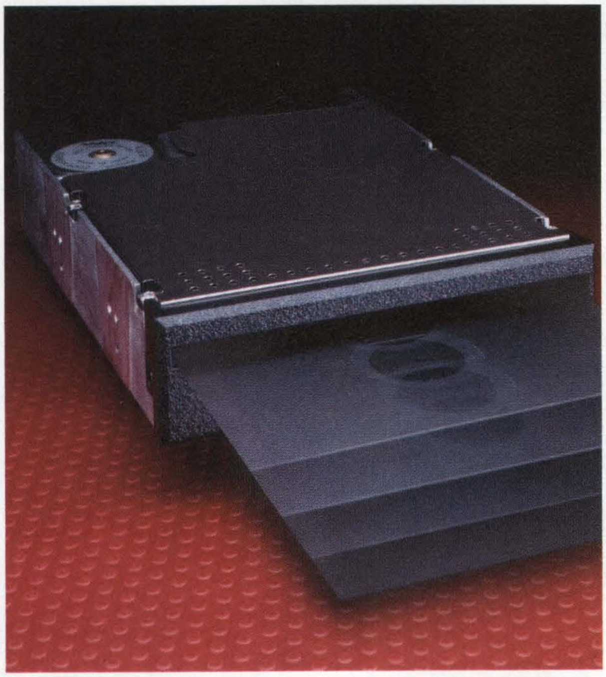

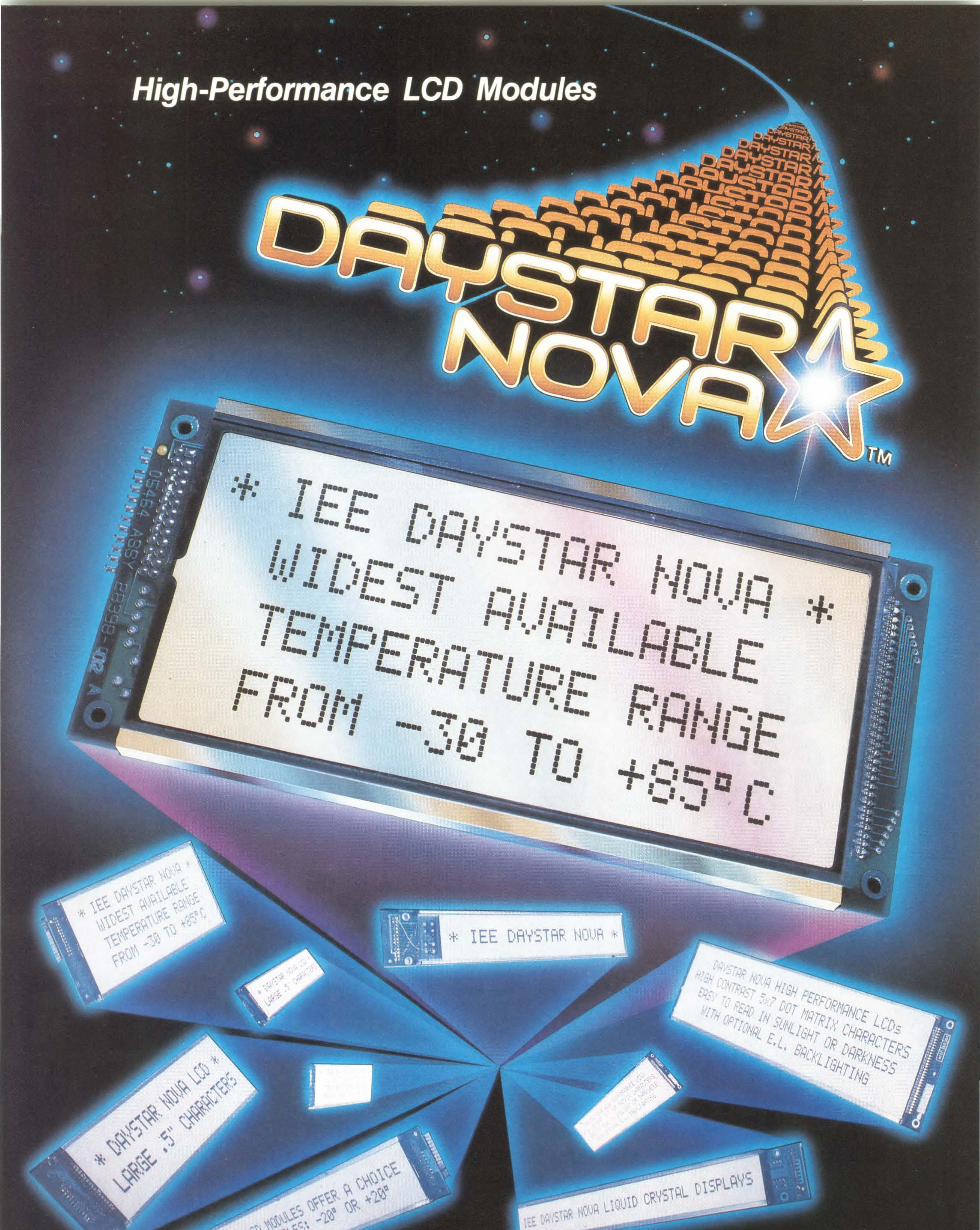
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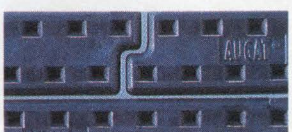

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CIRCLE NO 146

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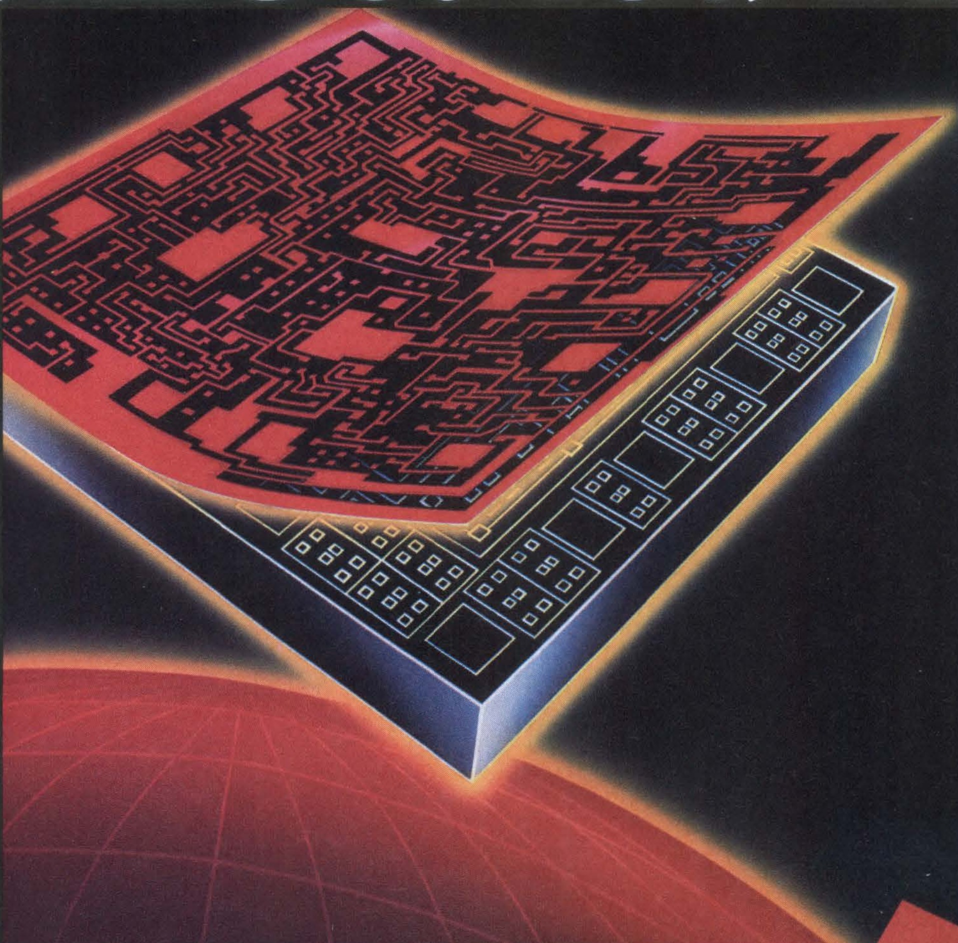

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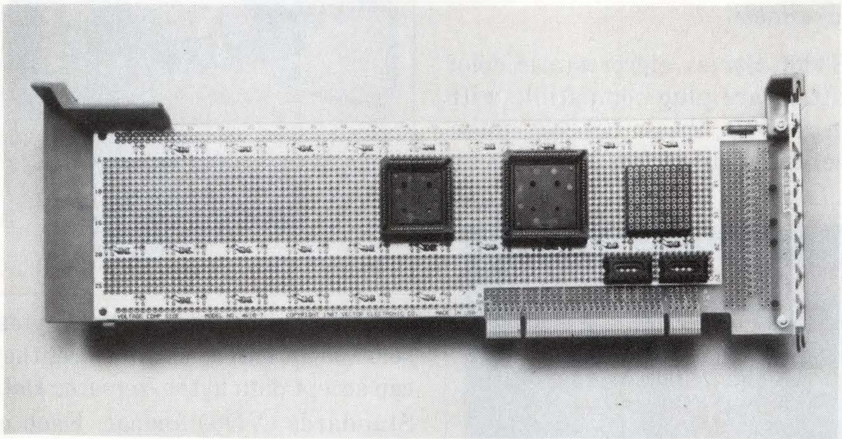
CIRCLE NO 147

COMPUTERS & PERIPHERALS



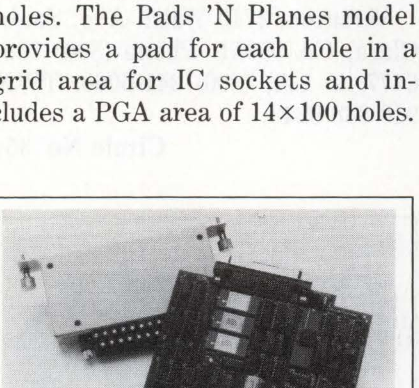
PROTOTYPE BOARDS

- *For high-speed logic designs on the PS/2 Models 50, 60, and 80*
- *Have ground and power planes for surface-mount capacitors*

Two prototype boards are available for the IBM PS/2 Models 50, 60, and 80 computers and for Micro Channel architecture. The Vectorbord plus model has socket pins and two pin-grid arrays (PGAs) with 21×25 holes. The Pads 'N Planes model provides a pad for each hole in a grid area for IC sockets and includes a PGA area of 14×100 holes. Each board holds 79 16-pin DIPs, 32 or 24 SMD capacitors, and a 33-μF capacitor. The boards have solder tin/lead-coated circuitry, 2-oz power and ground planes, and etched hole-marking legends. Dedicated holes are provided for voltage and ground terminals. Both boards feature transition pin areas for the bus edge connector and for a D-subminiature connector in the I/O area. $69 to $450.

Vector Electronic Co, 12460 Gladstone Ave, Sylmar, CA 91342. Phone (818) 365-9661. TLX 269303.

Circle No 351



A/D CONVERTER

- *32-channel single-ended capacity*
- *Operates at a 200-kHz throughput rate*

The AD300 board-level A/D converter for the HP 9000 Series 200/300 workstations provides multiple-channel data acquisition that accommodates 32 single-ended analog inputs or 16 differential analog inputs. It operates at a 200-kHz throughput rate and provides 12-bit resolution. A μP controls all onboard operations, thus reducing program control by the host HP computer; a 64k-byte FIFO eases the processing load further. Using an onboard channel sequencer, the board can store as many as 2048 states, each with its own channel, mode, and gain specifications. This operation allows many different types of measurements to be made without interaction by the host computer. A digital output port lets you program as much as 8 bits of data to control external instruments or circuitry. Two external trigger lines provide voltage-level triggering and a rising-edge trigger. The board uses the HP GPIO protocol for programming and supports Basic, Pascal, and HP-UX operating environments. $1900.

Infotek Systems, 1045 S East St, Anaheim, CA 92805. Phone (714) 956-9300.

Circle No 352

SWITCH/CONCENTRATOR

- *Packet switching for as many as 16 X.25 data links*
- *As many as four links can operate at speeds to 64k bps*

The Smart Net 3700 Switch/Concentrator provides a backbone for the company's wide-area network products. It uses an 80286 16-bit μP with 250k bytes of memory to switch more than 100 packets/sec and provide line concentration. It can handle as many as 16 X.25 data links. As many as four of these links can operate at speeds to 64k bps with soft-configured V.35 or RS-232C termination. Using Smart-View, a PC/AT-based SmartNet network management system, you can centralize network management. The resident system-management service allows you to configure operating parameters, update routing tables, perform diagnostics, monitor performance, and retrieve statistics locally or remotely from any point on the packet data network. The unit can route calls based on the content of the called address field and the call-user-data field. The unit is available with two or four 64k-bps X.25 links and four, eight, or 12 medium-speed links. With two 64k-bps and 4 medium-speed X.25 links, $6400.

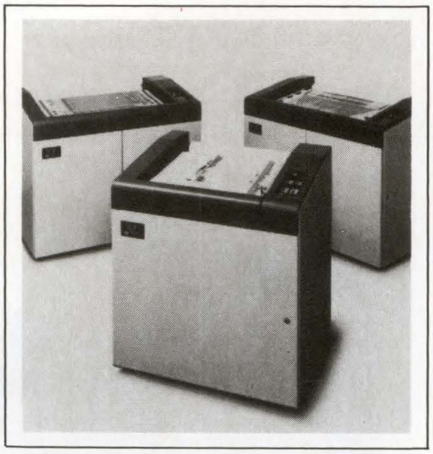
PCI Inc, 26630 Agoura Rd, Calabasas, CA 91302. Phone (818) 880-5704.

Circle No 353

COLOR PLOTTERS

- *Capable of 38.4k-byte/sec transfer rate*
- *200- or 400-point/in. resolution available*

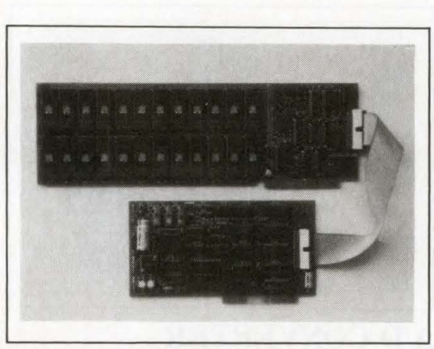
VS3000 Series electrostatic color plotters are plug compatible with pen plotters. Via an RS-232C interface, the plotters can accept vector



data at transfer rates to 38.4k bytes/sec. Via a Centronics interface, they can accept data in the Versatec Data Standards (VDS) format. Each of the units has a controller that includes 4M bytes of RAM for vector memory. For large vector plots, 55M-byte and 140M-byte disks are optional. The plotters are available in 200- and 400-point/in. resolution with 24-, 36-, and 44-in. media widths. With 200-point/in. resolution: VS3224, $45,000; VS3236, $55,000; VS3244, $65,000. With 400-point/in. resolution: VS3424, $55,000; VS3436, $65,000; VS3444, $75,000.

Versatec, 2710 Walsh Ave, Santa Clara, CA 95051. Phone (800) 538-6477; in CA, (800) 341-6060. TWX 910-338-0243.

Circle No 354



SILICON DISK

- *Plugs into an IBM PC, PC/XT, or PC/AT*
- *Provides 3M bytes of program storage*

Intended to reduce the disk-access delays associated with CAD/CAM

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Keithley Instruments Inc., 28775 Aurora Road, Cleveland, Ohio, 44139▲(216) 248-0400▲

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CIRCLE NO 296

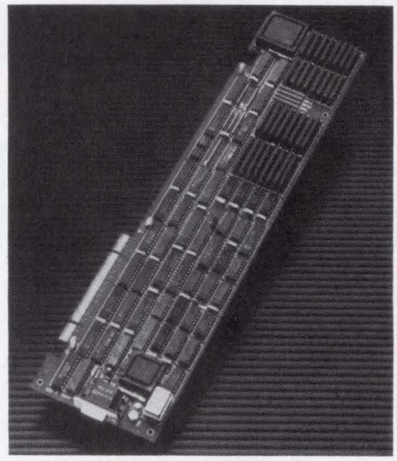
software packages that have to access large amounts of disk-based program memory, this EPROM silicon disk accommodates as much as 3M bytes of EPROM. The board occupies one expansion slot in an IBM PC, PC/XT, PC/AT, or compatible computer; you can install as many as four boards in the computer. Designed using 1M-bit CMOS EPROMs, the board has a maximum power requirement of 2W. Once installed, the silicon disk appears to the operating system as a normal disk drive. To transfer programs to the silicon disk, you plug a programming module into the PC to provide the necessary programming voltages and programming algorithms for the EPROMs. After programming, you can remove the programming module from the personal computer. A silicon disk fully loaded with EPROMs costs £999; the programming module costs £299.

Micro Control Systems Ltd, Electron House, Bridge Street, Sandiacre, Nottingham NG10 5BA, UK. Phone (0602) 391204. TLX 265871.

Circle No 355

GRAPHICS CONTROLLER

- *IBM PS/2 board displays 16 colors*
- *Uses the Hitachi ACRTC graphics μP*



The Artist 10/16, a graphics controller board for the IBM PS/2, can display 16 colors with either 1024×768-pixel noninterlaced resolution or 1024×1024-pixel interlaced resolution. It contains 1M bytes of video RAM for graphics memory and uses the Hitachi ACRTC graphics μP. It features a 4096-color palette, variable scan rates from 15 to 50 kHz, 65,000-vector/sec drawing rates, an 8- or 16-bit bus interface, and compatibility with GEM and VDI standards. The board allows you to zoom to 30 levels and thus provides a virtual window of 16000×12000 pixels. In an AutoCAD environment, a bird's-eye-view feature gives you a close look at the portion of a drawing you're working on. Optionally, you can see four different views of an image simultaneously. A fast-erase feature lets you erase any portion of a draw-

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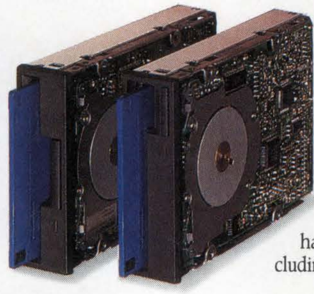

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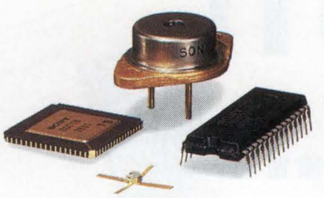

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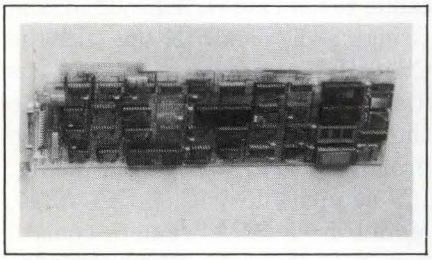
Spokane (509) 924-4410
WI Waukesha (414) 542-5352

CIRCLE NO 294

ing. When used with NEC's MultiSync XL, the board works with VGA (video graphics array) graphics. $2995.

Control Systems Inc, Box 64750, St Paul, MN 55164. Phone (612) 631-7800. TLX 756601.

Circle No 356



ADD-IN BOARD

- *Provides PCs with X.25 communications capability*
- *Includes software for a PAD and for SNA/3270 emulation*

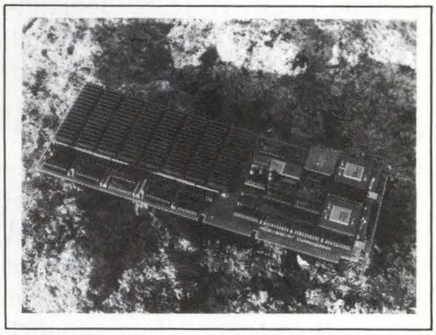
The SICC-PC add-in board provides IBM PC, PC/XT, PC/AT, and compatible computers with an X.25 network communications interface. The software that accompanies the board includes an MS-DOS driver and application software. The application software includes a PAD (packet assembler/disassembler), which allows you to communicate with remote hosts that implement CCITT X.28, X.29, and X.3 Recommendations. It also includes SNA/3270 emulation for communication with IBM mainframes. The board occupies one expansion slot in a personal computer and has an onboard Z80A CPU and PROM/dynamic-RAM options with respective memory capacities of 16k/48k, 32k/32k, and 48k/16k bytes. The serial interface, which you can adapt to physical layer interfaces such as X.21 and V24, is supported by a DMA capability. The serial port operates at 19,200 baud max. DM 2950 (including software).

Stollmann GmbH, Max-Brauer-Allee 81, 2000 Hamburg 50, West Germany. Phone (040) 3890030. Teletex (17) 403226.

Circle No 357

COPROCESSOR BOARD

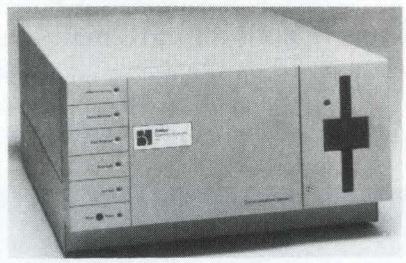
- *Has a 32382 demand-paged MMU*
- *Coprocessor operates at 15 MHz*



The 332/AT is a coprocessor board for the IBM PC/AT and compatibles and is based on the 32-bit NS32332 µP. It operates at 15 MHz with as much as 4M bytes of no-wait-state dynamic RAM. A 32382 demand-paged MMU (memory management unit) allows full use of the 32-bit virtual-address space. Other features include bus-master capability, access to the entire PC/AT-bus address space, two 16-bit counter/timers, and software and bidirectional hardware interrupts. A 32081 or 32381 floating-point processor is optional. Operating-system support includes AEON5.3, VRTX, and stand-alone access to all DOS and BIOS functions. The AEON5 operating system is an enhanced version of Unix System V.3 for the Series 32000. Languages available for AEON5 include C, Pascal, Fortran, Lisp, Basic, and Assembler. The onboard RAM has a burst-mode bandwidth of 24M bytes/sec for fetching op codes and reading data and 15M bytes/sec for writing data. With a 1M-byte RAM, $1995 (OEM qty).

Aeon Technologies Inc, 90 S Wadsworth Blvd, Suite 105-481, Lakewood, CO 80266. Phone (303) 986-3599.

Circle No 358



SNA GATEWAY

- *Allows you to share 48 hosts*
- *Uses an MC68020 32-bit μP*

The Server/1-SNA (System Network Architecture) is an enhanced version of the company's CS/1-SNA gateway unit. It lets IBM PCs and compatibles, 3270-type displays, and ASCII terminals and printers operate in an IBM 3270 SNA environment. This version utilizes an MC68020 μP that allows network devices to share as many as 48 host sessions. It also supports both the TCP/IP (Transmission Control Protocol/Internet Protocol) and the XNS (Xerox Network Systems) protocol sets. The unit works with three LAN types: Ethernet (IEEE-802.3), using coaxial or fiber-optic cable; token ring (IEEE-802.5); and Bridge Broadband (5M-bps with the CSMA/CD access mechanism). Thus it allows TCP/IP networks access to the SNA environment over the broadband and token-ring media. It's compatible with IBM's 3274, Model 51C SNA remote-control unit. $10,500, plus a $1000 software fee. A $5000 hardware and software upgrade kit is also available.

Bridge Communications Inc, 2081 Stierlin Rd, Mountain View, CA 94043. Phone (415) 969-4400. TLX 176544.

Circle No 359

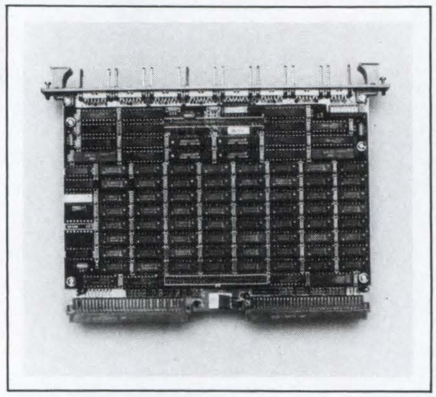
DISPLAY CONTROLLERS

- *1600×1280×8-bit resolution*
- *256 colors from a palette of 16.2 million*

The UDC-803 Series color-display controllers supports 60-Hz noninterlaced monitors. These IBM PC/AT-compatible, high-resolution, bit-mapped devices can produce 1600×1280×8- or 4-bit pixel resolution with a choice of 256 colors from a palette of 16.2 million. The controllers use the 82786 graphics coprocessor and 4M bytes of video RAM to produce polygons, line drawings, and bit-block transfers at speeds as high as 2.5 million pixels/sec. The 3M-byte RAM is dual ported for fast host access. The boards have a video bandwidth of 180 MHz and provide an RS-343 (monochrome or color) video output with composite or separate sync. They also feature a 32-bit external standard VSB (VME system bus) processor; pan and scroll registers; and variable display formats. AutoCAD and ImagePro-2000 software drivers are optional. The 8-bit version, $4995; the 4-bit version, $3995.

Univision Technologies, 12 Cambridge St, Burlington, MA 01803. Phone (617) 273-5388. TLX 988755.

Circle No 360



VIDEO STORAGE

- *VME module stores as much as 8 million pixels*
- *Eight interleaved modules can examine 8192×8192×8-bit image*

You use the MegaStore-8 VME module with the MaxVideo family of real-time image and digital-signal-processing boards. It can store as much as 8 million pixels as large, high-resolution individual images measuring 2048×4096×8 bits, or it can store as many as 32 standard-sized (512×512×8-bit) images. Within a MaxVideo subsystem, the module exchanges data with other MaxVideo modules via the MaxBus. The board has two independent address generators, (one for the read port and one for the write port), which expand MaxVideo's ability to focus processing on regions of interest. The board performs video read and write zooms of 2×, 4×, and 8× magnification. Eight modules can be interleaved to examine an

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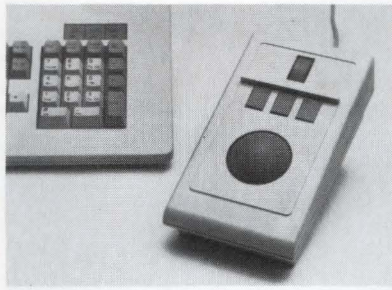
8192×8192×8-bit image frame. A VME port with an A32, D32 interface is accessible as one 8M-byte block or as a ½M-byte page that is switchable to any one of 16 blocks. The board has six MaxBus ports (two outputs, two input/outputs, and two inputs) that transfer data at a 10M-byte/sec rate. $11,950.

Datacube Inc, 4 Dearborn Rd, Peabody, MA 01960. Phone (617) 535-6644.

Circle No 361

POINTING DEVICE

- *Allows input of 2- and 3-axis data via an RS-232C interface*
- *Offers resolution to 200 points/in. for x, y, and z axes*



The FastTrap is a 2- or 3-axis pointing device that offers an alternative to a mouse for entering data into a computer. In addition to functioning in a proprietary 3-axis operating mode, it can emulate existing 2-D mice such as Microsoft's serial mouse. It features a 200-point/in.-resolution trackball for x- and y-axis inputs, a 200-point/in. Trackwheel for z-axis input, three input buttons, and an RS-232C interface. The software driver runs with MS-DOS or PC-DOS versions 2.0 and higher, and it supports systems equipped with an MDA (monochrome display adapter), a CGA, an EGA, or a Hercules graphics adapter. A keyboard emulator program allows the pointing device to work with many software packages that don't directly support pointing devices. The device has a low-power CMOS design and is compatible with all systems that support RS-232C communications. Its work-surface footprint is smaller than the clear area required by a mouse. $149.

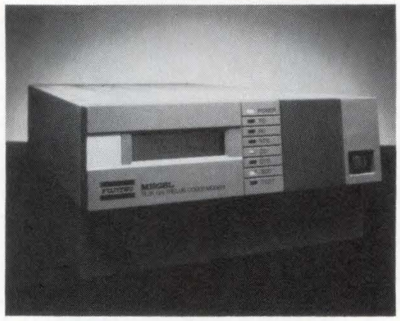
Microspeed Inc, 5307 Randall Pl, Fremont, CA 94538. Phone (415) 490-1403.

Circle No 362

19,200-BPS MODEM

- *For use over D1-conditioned leased lines*
- *Uses 16-state, 8-dimensional Trellis-code modulation*

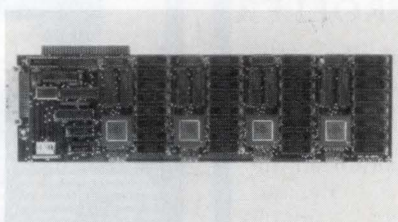
The M1928L 2-port synchronous modem features data-transmission rates of 19,200, 16,800, 14,400, 12,000, and 9600 bps. It uses 16-state, 8-dimensional Trellis coding to ensure operation over D1-conditioned leased lines. It has an adap-



tive equalizer that automatically reduces or increases the transmission rate in response to the quality of the line conditions. It has an integral 2-channel multiplexer that allows it to emulate the operation of two 9600-bps modems, thus eliminating the need for another leased line. The modem has eight loopbacks and a built-in bit-error-rate tester for fault isolation. An LCD shows local and remote strapping, diagnostics, and operating conditions. $4495.

Fujitsu America Inc, 3055 Orchard Dr, San Jose, CA 95134. Phone (800) 422-4878; in CA, (408) 432-0460. FAX (408) 432-1318.

Circle No 363



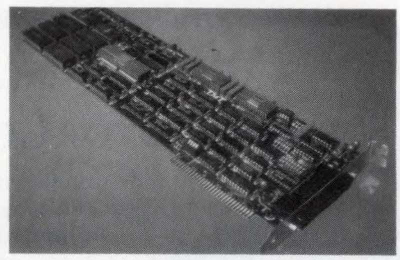
TRANSPUTER BOARD

- *Plugs into an IBM PC to provide four transputers*
- *Supports transputer development software*

The Fast4 board occupies one expansion slot in an IBM PC, PC/XT, PC/AT, or compatible and provides four 32-bit T414 transputers or T800-20 floating-point transputers, thus increasing the PC's processing power to 40 MIPS. You can also use the board as a stand-alone system or as part of a larger transputer system. Each of the transputers has 1M bytes of RAM. You can select one of the transputers to operate as a separate transputer subsystem, or you can use it to control the other three transputers. This control mode allows you to run software (the Inmos transputer development system software, for example) on one transputer, downloading code to the other three transputers and supervising their error recovery. In addition to supporting this type of software, the board supports program development in Fortran, Pascal, and C. The four transputers on the board are connected by transputer links into a square. Also, two transputer links from each transputer are accessible externally so that you can link multiple boards into a range of topologies. £4400.

Quintek Ltd, Southfield House, 2 Southfield Rd, Westbury-on-Trym, Bristol BS9 3BH, UK. Phone (0272) 628196. TLX 449683.

Circle No 364



MOTION CONTROLLER

- *Based on the 8096 16-bit μC*
- *Provides a turnkey system for 1- or 2-axis motion control*

The Amadeus-96 is a single-board motion controller for the IBM PC, PC/XT, PC/AT, and compatible computers. It is based on the 8096 16-bit μC and provides a turnkey system for 1- or 2-axis motion control. The only additional hardware required for closed-loop control is the power amplifier and the mechanical system, which are interfaced through a 37-pin rear-panel connector. Feedback can be read from shaft encoders, tachometers, and limit switches. The board can actuate the motor with analog signals or

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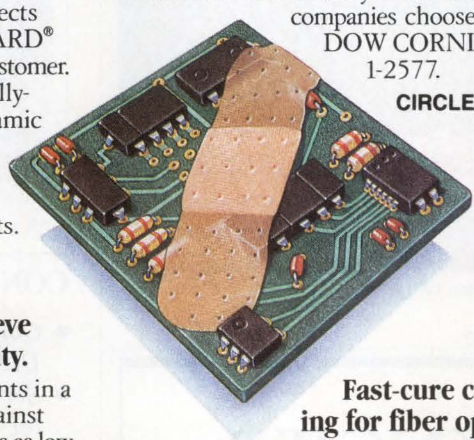

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Write Department 7013, Midland, MI 48686-0994.

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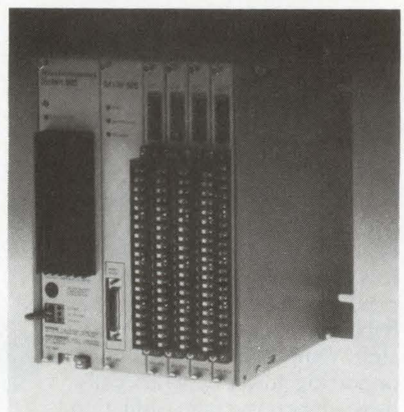
digital PWM signals. Hardware features include an 8096 CPU running at 12 MHz; 48k bytes of RAM; 8k bytes of ROM; two incremental quadrature decoders; a watchdog timer; four input channels for 10-bit A/D conversion; two output channels for 12-bit D/A conversion; and address decoding for as many as eight boards. Software features include an 8096-based operating system providing drivers for all onboard devices; implementation of multiple sample rates; real-time software that performs 1- or 2-axis data acquisition and control; and support of Intel's C96, PLM96, and ASM96 languages. $2000.

Integrated Motions Inc, 1299 N First St, San Jose, CA 95112. Phone (408) 279-6465.

Circle No 365



CONTROLLER FAMILY

- *Conforms to UL, CSA, VDE, DIN, and IEC standards*
- *Series consists of CPU controller and I/O modules*

The Series 505 control system is UL listed, CSA certified, and meets applicable DIN, VDE, and IEC requirements. It consists of four versions of the Model 525 CPU and a range of I/O modules. The four CPUs have memory sizes of 2k-, 4k-, 8k-, and 12k words of relay-ladder-logic (RLL) memory. Programs are stored in battery-backed CMOS RAM, EPROM, or EEPROM. The

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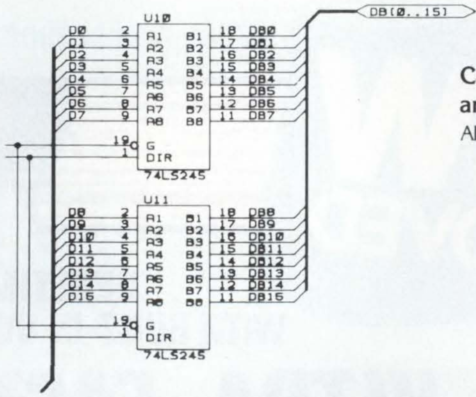

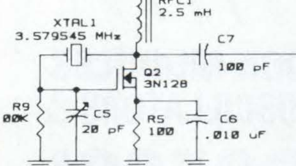

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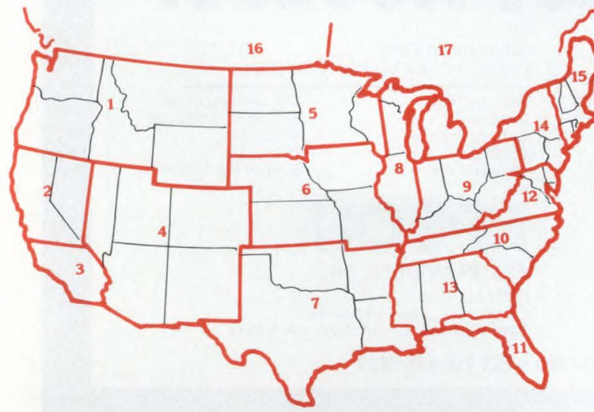

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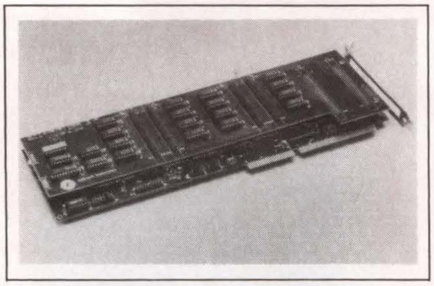
8-, 16-, and 32-point versions of the I/O modules achieve the following packaging densities: As many as 128 I/O points in a 10.5×8.0-in. area and as many as 512 I/O points in a 10.5×19.0-in. area. Twenty-seven I/O modules for ac and dc voltages and currents are available for operation with pushbuttons, limit switches, proximity switches, lights, or solenoids. Four analog modules monitor and control pressure, temperature, flow, or position by converting analog inputs to 10-bit digital words for processing. Programs are developed using the company's TISoft software. 2k-word Model 525 CPU, $745; 4k-word version, $1958; 8k-word version, $3548; 12k-word version, $5261; I/O modules, from $219.

Texas Instruments Inc, Data Systems Group, Box 809063, Dallas, TX 75380. Phone (800) 527-3500.

Circle No 366



NTDS BOARD SET

- *Has NATO STANAG 4146 parallel interface*
- *Simulates the operation of AN/UYK Series computers*

The NT1632FS AT/NTDS adapter board and the ANW1632 daughter board comprise a 2-board set that simulates the Navy Tactical Data System (NTDS) interface. The set is also compatible with the NATO Standard Agreement (STANAG) 4146 parallel data interface. These interfaces are common to the data distribution networks fitted on most US and Allied surface ships. The board set can be used in the IBM PC, PC/XT, PC/AT, Zenith 248 computers or with a 286/386 system. The interface hardware and software simulates the operation of the AN/UYK Series computers. The board set provides full-duplex communications by handling Type A (NTDS slow=160k bytes/sec), Type B (NTDS fast=1M bytes/sec), and Type C (NTDS fast ANEW=1M byte/secs) I/O channels using differential I/O drivers and receivers. Full-duplex 8-, 16-, 24-, or 32-bit-wide parallel-word transfers optimize communication with computers or peripherals. The source code for I/O drivers is included in Microsoft Pascal, Turbo Pascal, and C languages. $3250.

Sabtech Industries Inc, 4091 E La Palma Ave, Unit P, Anaheim, CA 92807. Phone (714) 630-9335.

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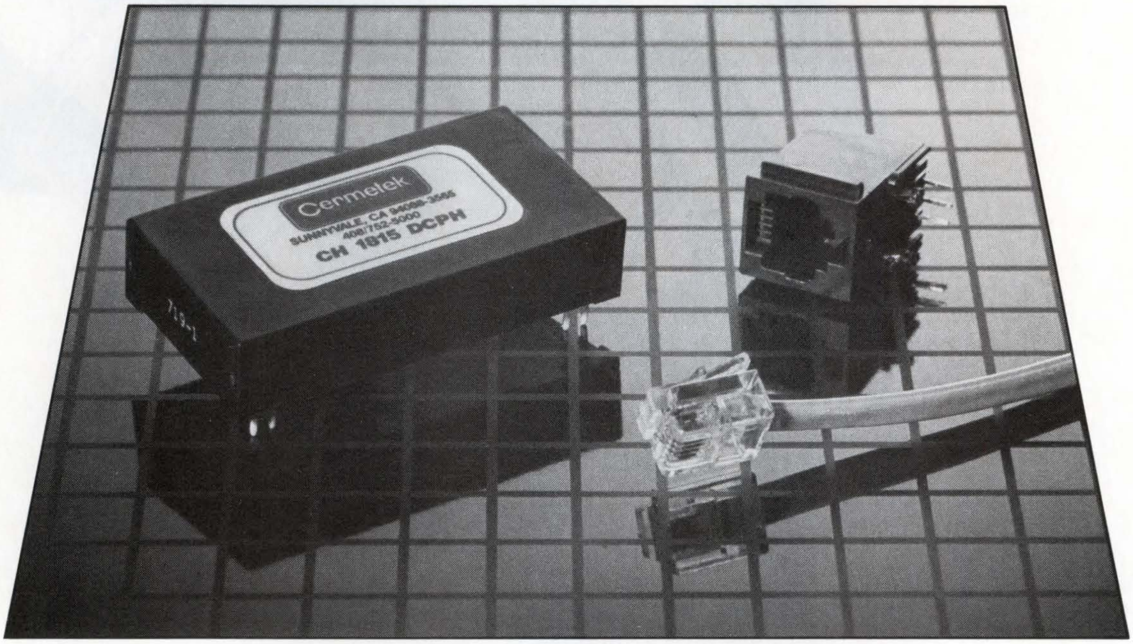

THE PROBLEM

Products that connect directly to the telephone line must be registered:

- ☐ FCC in the United States
- ☐ DOC in Canada
- ☐ BABT in the United Kingdom
  by telephone authority in most other countries

This means first understanding and interpreting local requirements, then conducting tests to meet these requirements and finally obtaining approvals.

Needless to say, this can be an involved and time-consuming process taking as much as 12 months to complete.

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Other telephone line interfaces are designed for international operation—CH1814/CH1828, ultra small size—CH1815 or high volume/low cost—CH1812A/1813

And all are compatible with today's modem components. Cermetek provides application notes, design assistance and help with registration. Write or call us for more information.

Phone Line Interface Components

Features	CH1810A	CH1811	CH1812A/ CH1813	CH1814	CH1815	CH1828
Countries for use	U.S. Canada	U.S. Canada	U.S. Canada	Inter-nat'l	U.S. Canada	Inter-nat'l British
Pre-Registered	FCC Part 68	FCC Part 68	Conforms FCC	British Pending	Conforms FCC	Regis-tered
Surge and High Voltage Protection	Yes	Yes	Yes	Yes	Yes	Yes
Isolation	1KV	1KV	1KV	1.5KV	1KV	4KV
Ring Detect and ON/OFF Hook Control	Yes	Yes	Yes	Yes	Yes	Yes
Phone Hook Switch Detect	—	—	1813	—	—	—
2- to 4-wire Conversion	Yes	Yes	NO	NO	NO	Yes
Data and voice	Data	Both	Data	Data	Data	Data
Size (in.) L W H	2.2 x 2 x .7	2.2 x 2 x .7	2.1 x 1.1 x .6	2.1 x 1.1 x .6	2.1 x 1.1 x .45	3.4 x 3.4 x .77
Power	+12V 275mW	+5V 100mW	Inter-Face Driven	Inter-Face Driven	Inter-Face Driven	+12V — 700mW

Cermetek microelectronics

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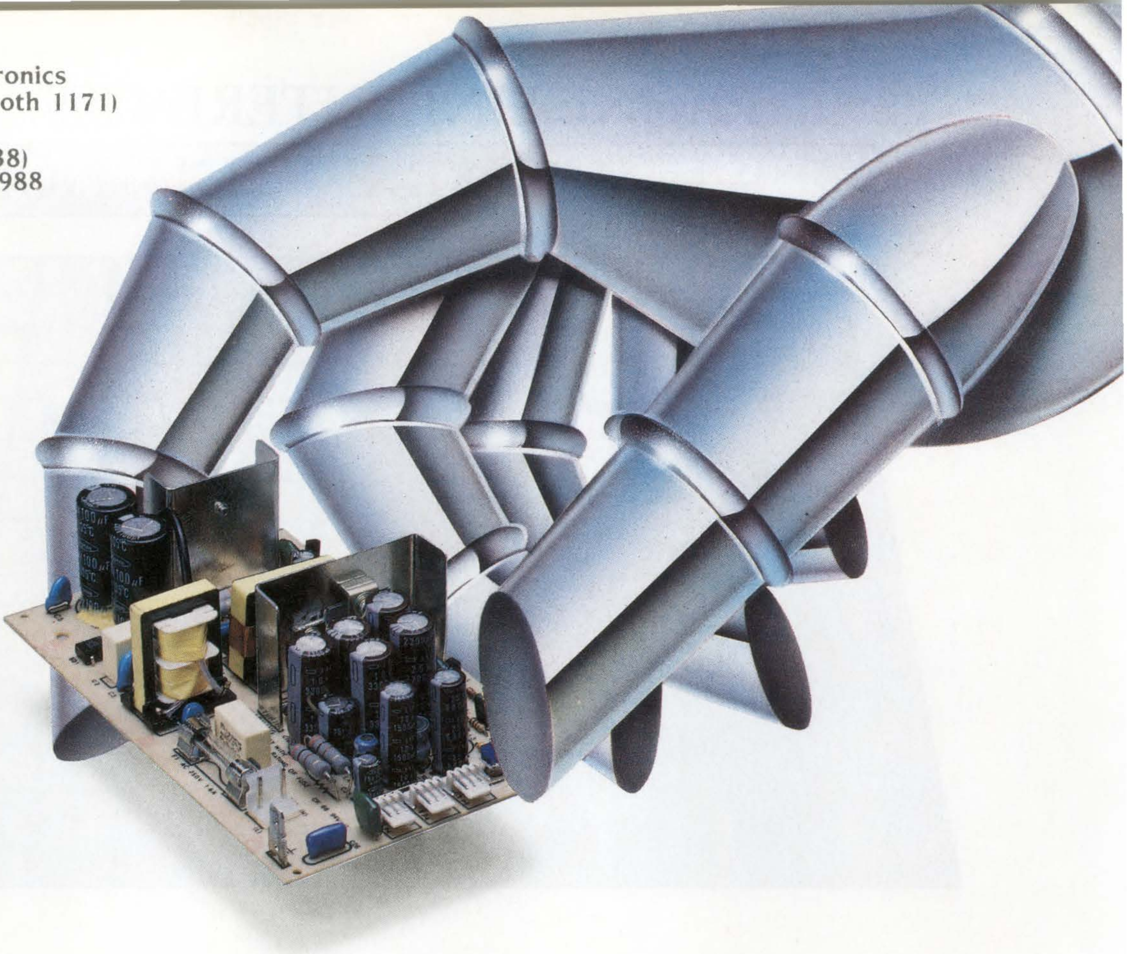

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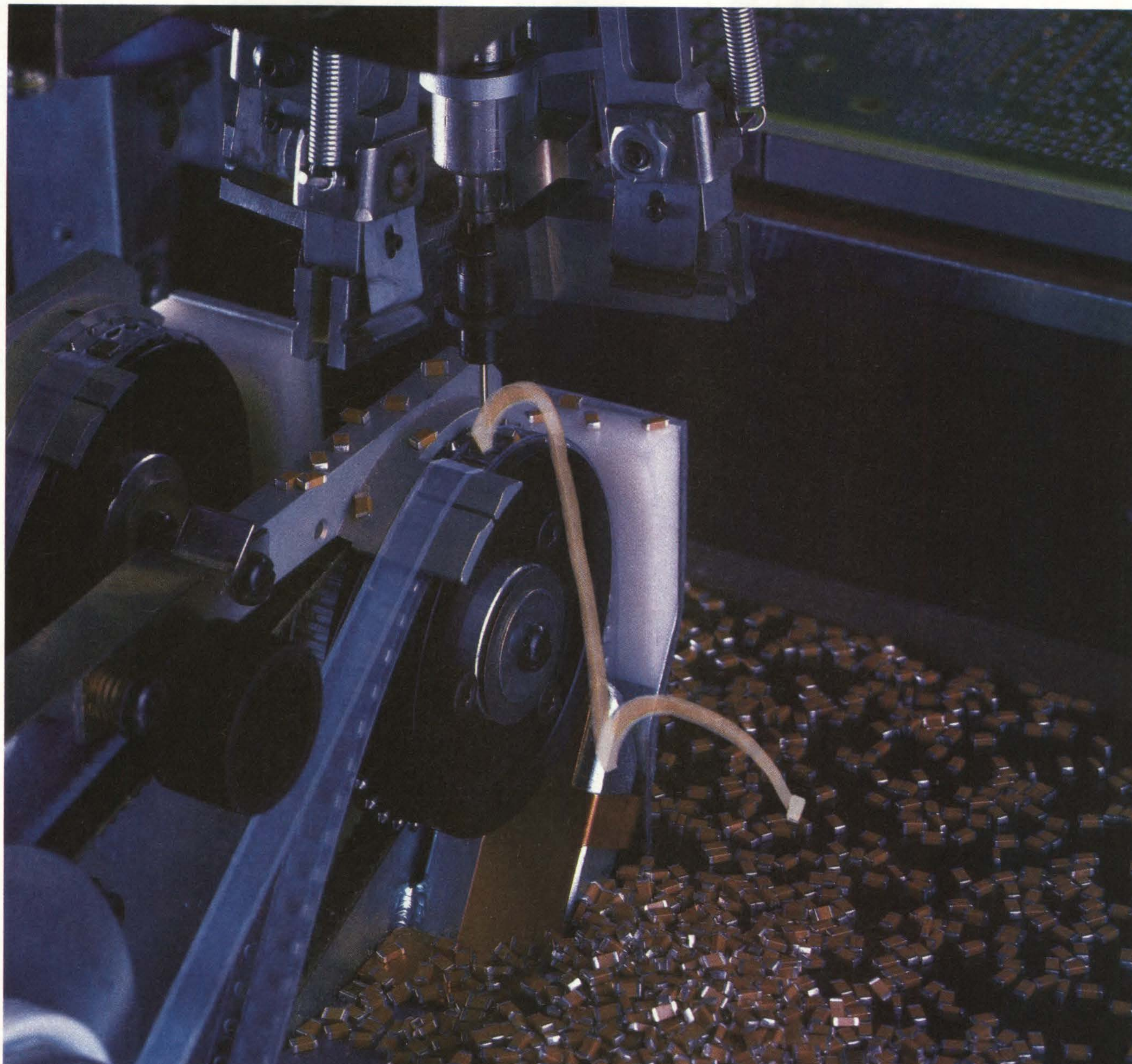

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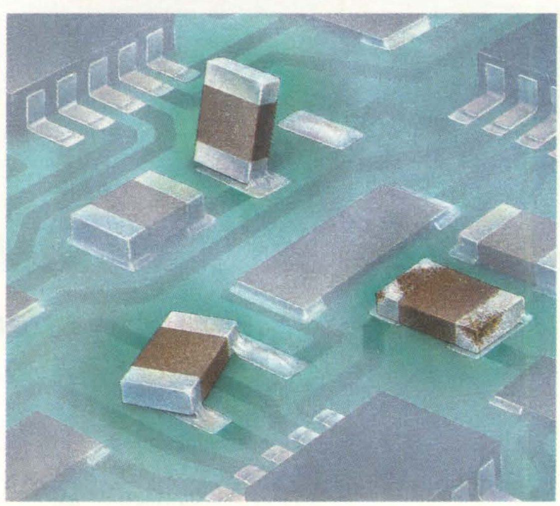

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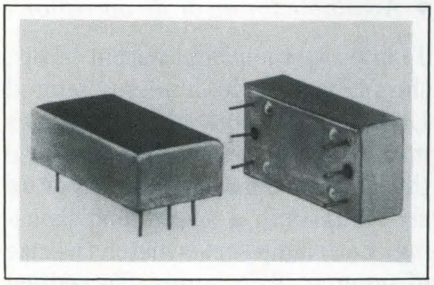


FILTERS

- *Are matched in pairs*
- *Have 60-dB min spurious response*

These filters, which are phase/amplitude matched in pairs, have a nominal frequency of 21.4 MHz and a 3-dB bandwidth of ±150 kHz min. Their initial offset has a 10° matching phase and a 1-dB amplitude. The devices also offer ±120-kHz matching phase of 2° and amplitude of 0.5 dB. Their spurious response equals 60 dB min, and insertion loss equals 10 dB max. The filters, which operate over −20 to +85°C, have 50Ω source and load impedance. Typical package size equals 1.8×0.6×0.52 in. $650.

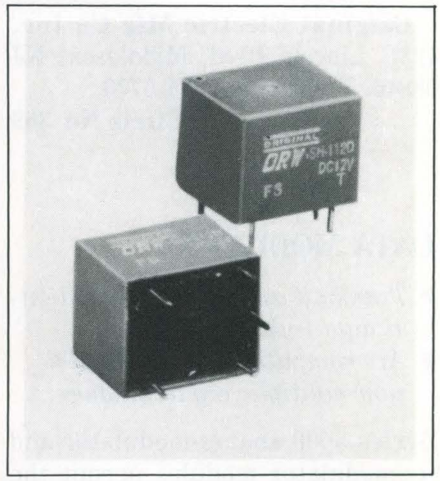
Piezo Technology Inc, Box 7859, Orlando, FL 32854. Phone (305) 298-2000. TWX 810-850-4136.

Circle No 368

RELAYS

- *Designed for general-purpose applications*
- *Available in spst and spdt contact arrangements*

ORW Series 5A relays are designed for general-purpose applications, such as process control and telecom-



munications, that require a high contact rating in a small package. The units are sealed to accommodate wave soldering during pc-board processing operations. When switching 5A loads, the relays have a 100,000-operation life expectancy.

The devices are available with spst and spdt contact configurations. $1.09 (1000). Delivery, eight to 10 weeks ARO.

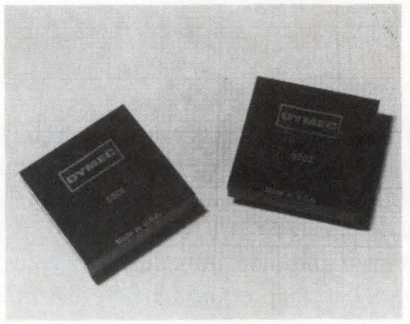
Original Electric Mfg Co Inc, 123B Lincoln Blvd, Middlesex, NJ 08846. Phone (201) 271-5770.

Circle No 369

DATA MODULES

- *Transmit analog data over digital data links*
- *Are compatible with time-division multiplexing techniques*

Series 5500 analog-modulator and -demodulator modules permit the transmission of precision analog information over digital data links. The modulator (Model 5501) accepts a ±1V, 500-kHz-bandwidth input signal and produces a 4- to 5-MHz TTL pulse train, which you can multiplex with other TTL data streams



for transmission over a digital data link. The demodulator (Model 5502) accepts a TTL carrier signal and produces a ±2V or 0 to 4V output signal. If you employ a lowpass filter with a 1-MHz cutoff frequency, the overall link bandwidth equals dc to 500 kHz. Model 5501, $144 (25); Model 5502, $165 (25). Delivery, stock to six weeks ARO.

Dymec Inc, 8 Lowell Ave, Winchester, MA 01890. Phone (800) 225-1151; in MA, (617) 729-7870. TWX 710-348-6596.

Circle No 370

LAMPS

- *Incorporate six LEDs for increased brightness*
- *Available for ac or dc operation*

To improve their light output levels, the MF206 Series midget-flanged LED lamps and MG206 Series midget-grooved LED lamps utilize thick-film technology to incorporate six LEDs into a single lamp housing. Both lamp series match the size of popular T1¾ lamps. To reduce their overall current requirement, the six LEDs are connected in series, with integral resistors that provide 18 to 48V operation. Alternatively, you can obtain versions of the lamps with the LEDs arranged in two parallel arms, with each arm containing three LEDs. In addition to providing a level of redundancy in the event of one arm failing, this arrangement allows operation from supplies as low as 5V. Versions with the LEDs arranged for ac operation

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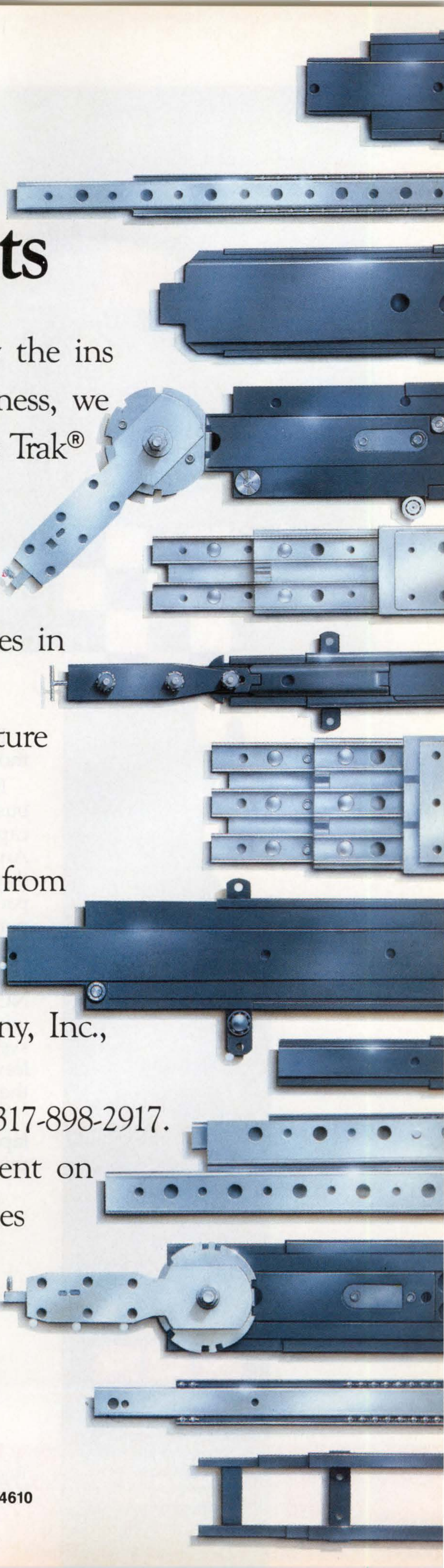

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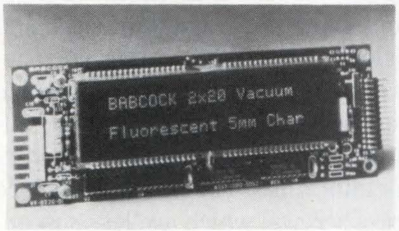
CIRCLE NO 311

are also available. £2.72.

Marl International Ltd, Ulverston, Cumbria LA12 7RY, UK. Phone (0229) 52430. TLX 65100.

Circle No 371



VF DISPLAY MODULE

- *Can be filtered to complement front-panel design*
- *Includes drive, refresh, and control electronics*

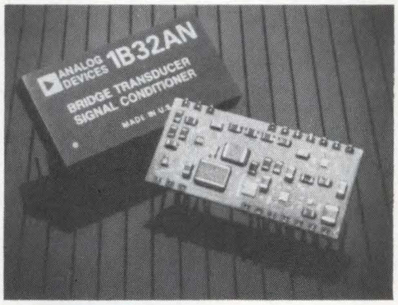
The VF-0220-01 is a 2-line×20-character vacuum-fluorescent-display subsystem. Its 0.2-in. dot-matrix viewing area presents 40 characters in a tight footprint. You can filter the blue-green display to blue, green, aqua, or yellow to complement front-panel design. The module contains display drive, refresh, and control electronics. The device operates from 5V; its dc/dc converter provides all additional operating voltages. A μP controller offers editing functions such as blinking characters and horizontal scrolling. $148 (100). Delivery, stock to 12 weeks ARO.

Babcock Display Products Inc, 1051 S East St, Anaheim, CA 92805. Phone (714) 491-5121. TLX 249646.

Circle No 372

SIGNAL CONDITIONER

- *Has ±0.005% max nonlinearity*
- *Direct transducer interface has no external parts*



The 1B32 hybrid signal conditioner offers ±2 μV/°C max offset voltage and ±6 ppm/°C gain drift. Nonlinearity equals ±0.005% max and common-mode rejection equals 140 dB min. The device provides pin-selectable gains of 333.3V/V and 500V/V for 2 mV/V and 3 mV/V load cells. Additional features include a direct transducer interface with no external parts and a remote sensing interface with 6-wire load cells. To optimize performance, you can program the transducer's preset excitation from 4 to 15V at 100 mA. The integral 3-pole lowpass filter offers a 60-dB/decade roll-off from 4 Hz, which reduces common-mode noise and improves the system's signal-to-noise ratio. The device has an operating range of −25 to +85°C. $52 (100). Delivery, stock to six weeks ARO.

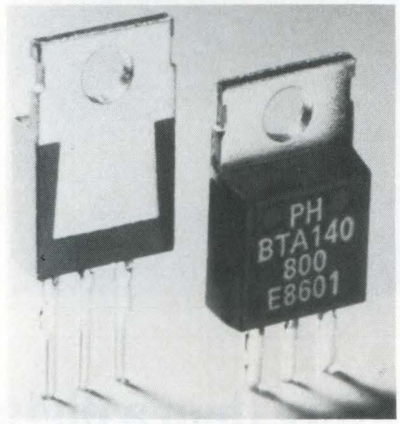
Analog Devices Inc, Box 9106, Norwood, MA 02062. Phone (617) 461-3643. TLX 174059.

Circle No 373

TRIACS

- *Feature a 25A on-state current rating*
- *Have a 35-mA min gate current*

BTA 140 Series glass-passivated triacs have an on-state current handling capability of 25A rms. The devices are designed for use in applications that require high bidirectional transient- and blocking-voltage capability, and they feature a 200A surge-current rating in 60-Hz systems. The units have a 35-mA min gate-current triggering requirement. You can order them rated for 500, 600, or 800V. They come housed in encapsulated TO-220 packages. For 500V types, $1.20 (10,000). Delivery, 12 weeks ARO.



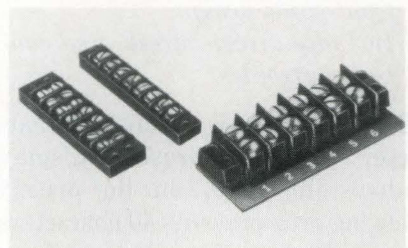
Amperex Electronic Corp, George Washington Hwy, Smithfield, RI 02917. Phone (401) 232-0500.

Circle No 374

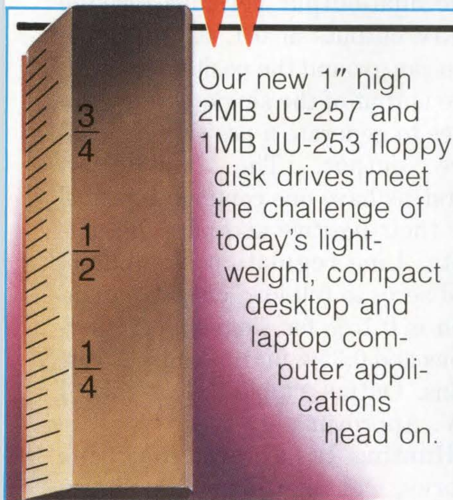
TERMINAL BLOCKS

- *Are UL recognized*
- *Have optional flame-retardant marker strips for identification*

These UL-recognized terminal blocks for cable-to-cable applications come in a variety of sizes and styles. The units have barriers between the terminals to maximize electrical ratings and to provide additional protection against accidental shorting. The blocks feature brass screws, which are less susceptible to corrosion from moisture. Options include flame-retardant marker strips for identifying the



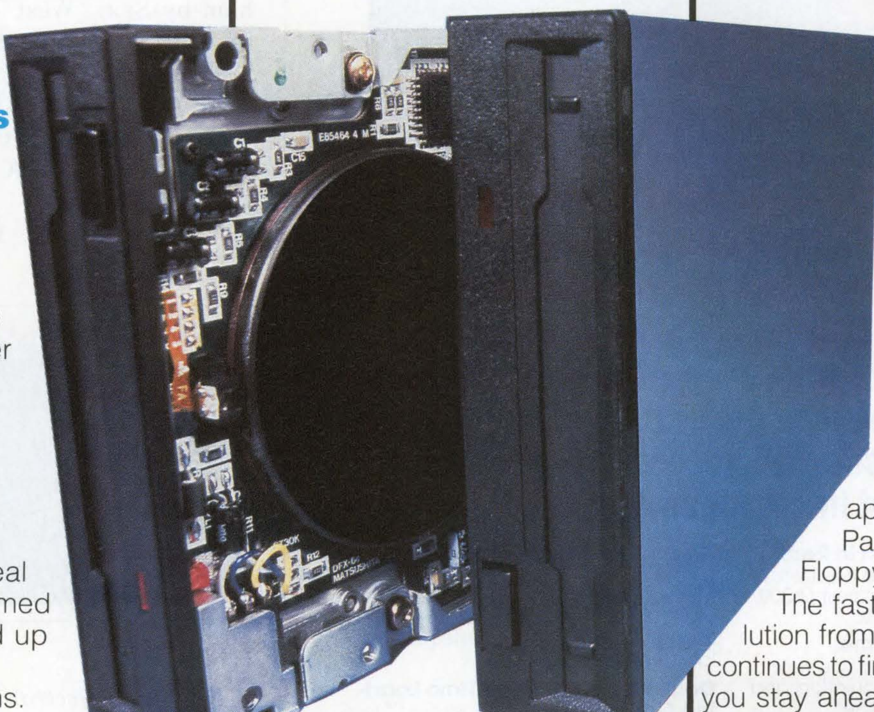
To stay ahead of the pack you've got to be fast, smart and *small.*



"Our new 1″ high 2MB JU-257 and 1MB JU-253 floppy disk drives meet the challenge of today's lightweight, compact desktop and laptop computer applications head on.

Panasonic® 3½″ Floppy Disk Drives.

1MB
2MB



There's more here than meets the eye.
For all of their performance, our 3½″ disk drives are just 1″ high. They're 50 grams lighter than 32mm models. And they consume a mere 6.5 watts of power. All of which makes them ideal for today's slimmed down, lightened up portable and desktop systems.

Speed is just the beginning.
With some 3½″ disk drives, you can count on standard track-to-track access time of 6 msec. With ours, you can cut that in half – to a blazing 3 msec. Right now, nothing in their class is faster.

It pays to think big.
When you need capacity, the JU-257 gives you plenty. It reads and writes both 1 and 2MB (unformatted) floppy disks. But if that's more than you want, the JU-253 will handle floppy disks up to 1MB.

There's more. For compatibility, a standard TTL interface is built right in. Both size and power consumption are reduced from 32mm drives. And it's even possible for our drives to be used in some CMOS applications.

Panasonic 3½″ Floppy Disk Drives.

The fast, smart, small solution from the company that continues to find new ways to help you stay ahead of the pack.

For more information, contact: Panasonic Industrial Company, Memory Systems Division, 1600 McCandless Drive, Milpitas, CA 95035. (408) 262-2200. Or call any Hamilton-Avnet location at 1-800-228-7886.

Panasonic
Industrial Company

terminal positions. The terminal blocks are currently undergoing CSA (Canadian Standards Association) certification testing. $0.46 to $10.17 (1000).

TRW Electronic Components Group, 1501 Morse Ave, Elk Grove Village, IL 60007. Phone (312) 981-6000.

Circle No 375

POWER SUPPLIES

- *Provide 5, 12, 24, or ±15V outputs*
- *Are suitable for chassis or pc-board mounting*

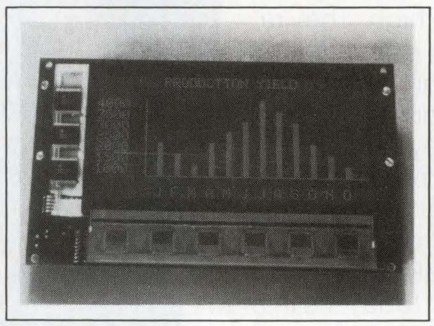
Minivolt miniature power supplies measure 90×64×32 mm and are suitable for chassis or pc-board mounting. They operate from 110/230V line inputs. Single-output versions provide a 5V output at 0.5, 1.0, 1.5, 2.0, or 2.5A; a 12V output at 1.2A; or a 24V output at 0.6A. The dual-output versions provide ±15V outputs at 0.1, 0.2, or 0.5A. You can ground the positive or negative output of the single-output supplies to generate a positive or negative output. The dual-output versions have one common terminal for their positive and negative outputs. Line regulation is ±0.05%, and zero- to full-load output regulation is 0.15% for single-output versions and 0.35% for dual-output versions. Output ripple is less than 1 mV. Approximately £100.

Hunting Hivolt Ltd, Riverbank Works, Old Shoreham Rd, Shoreham-by-Sea, West Sussex BN4 5FL, UK. Phone (0273) 454511. TLX 87466.

Circle No 376

Hunting Hivolt, 1008 W 9th Ave, King of Prussia, PA 19406. Phone (215) 265-7462.

Circle No 377



DISPLAY

- *Has drive electronics and a µP-based controller*
- *Operates in either serial or parallel modes*

The 192-column×88-row Model APD-192GO88-1 graphics display has drive electronics and a µP-based controller. The display, which you can program to operate in serial or parallel mode, furnishes refresh memory, character generation, and control logic. The unit uses 1- or 2-byte commands to simplify code generation while accomplishing

side view
(actual size)

With a Planar light-emitting electroluminescent flat panel display, you could use the rest of this space for anything you like. Call either 503-690-1100 or 503-690-1102, or write for a brochure:
PLANAR SYSTEMS, INC.
1400 N.W. Compton Drive
Beaverton, Oregon 97006.

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CIRCLE NO 267

WHEN YOU HAVE THE FACTS— YOU'LL KNOW THERE IS NO COMPETITION

Introducing the Venable 350—A New Generation Design Tool For Frequency Response Analysis, Synthesis, Modeling and Testing of Power Supply and Servo Control Loops.

The Venable 350. It's a highly flexible, computer-based 0.0001 Hz to 1.0 MHz frequency response analyzer. It allows you to quickly and precisely measure and document the frequency characteristics of any component or system. Competitively priced with other uncompromising analyzers, it truly offers a quantum leap forward in performance and design capability.

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The 350 maximizes your engineering creativity. And it's a real workhorse in a test environment. But there's so much to the Venable 350 it can't be covered in one page. Why not contact Venable Industries today. After all, if you don't—how do you know your competition won't? **Venable Industries,** 3555 Lomita Blvd., Torrance, CA 90505. Outside CA **(800) 262-2522.** Inside CA **(213) 539-2522.** Fax: (213) 539-4139.

VENABLE INDUSTRIES,INC.

V E N A B L E

CIRCLE NO 266

tasks such as scrolling or line and character insertion. A 4k×8-bit EPROM generates 256 characters—128 US ASCII characters and 128 block-graphics characters. The vendor will program alternate character sets for you, or you can program them yourself. You can also order a version that will directly interface with CRT controllers. $699 (100).

Dale Electronics Inc, 2064 12th Ave, Columbus, NB 68601. Phone (402) 564-3131.

Circle No 378

TRIMMERS

- *Withstand soldering to 300°C*
- *Are compatible with major pick-and-place equipment*

Model 3314 surface-mount trimmers withstand 300°C soldering temperatures. Designed to minimize board real-estate requirements, the units measure 4.45×4.45×2.55 mm. They

are compatible with all major pick-and-place equipment. The devices have standard resistance values from 10Ω to 2 MΩ and a contact-resistance variation of 1%. You can specify either J-hook or gull-wing lead configurations. The trimmers meet EIA standard 481 and come in 12-mm embossed tape on 7-in. diameter reels. $1.09 (1000). Delivery, 12 weeks ARO.

Bourns Inc, 1200 Columbia Ave, Riverside, CA 92507. Phone (714) 781-5500. TLX 676423.

Circle No 379

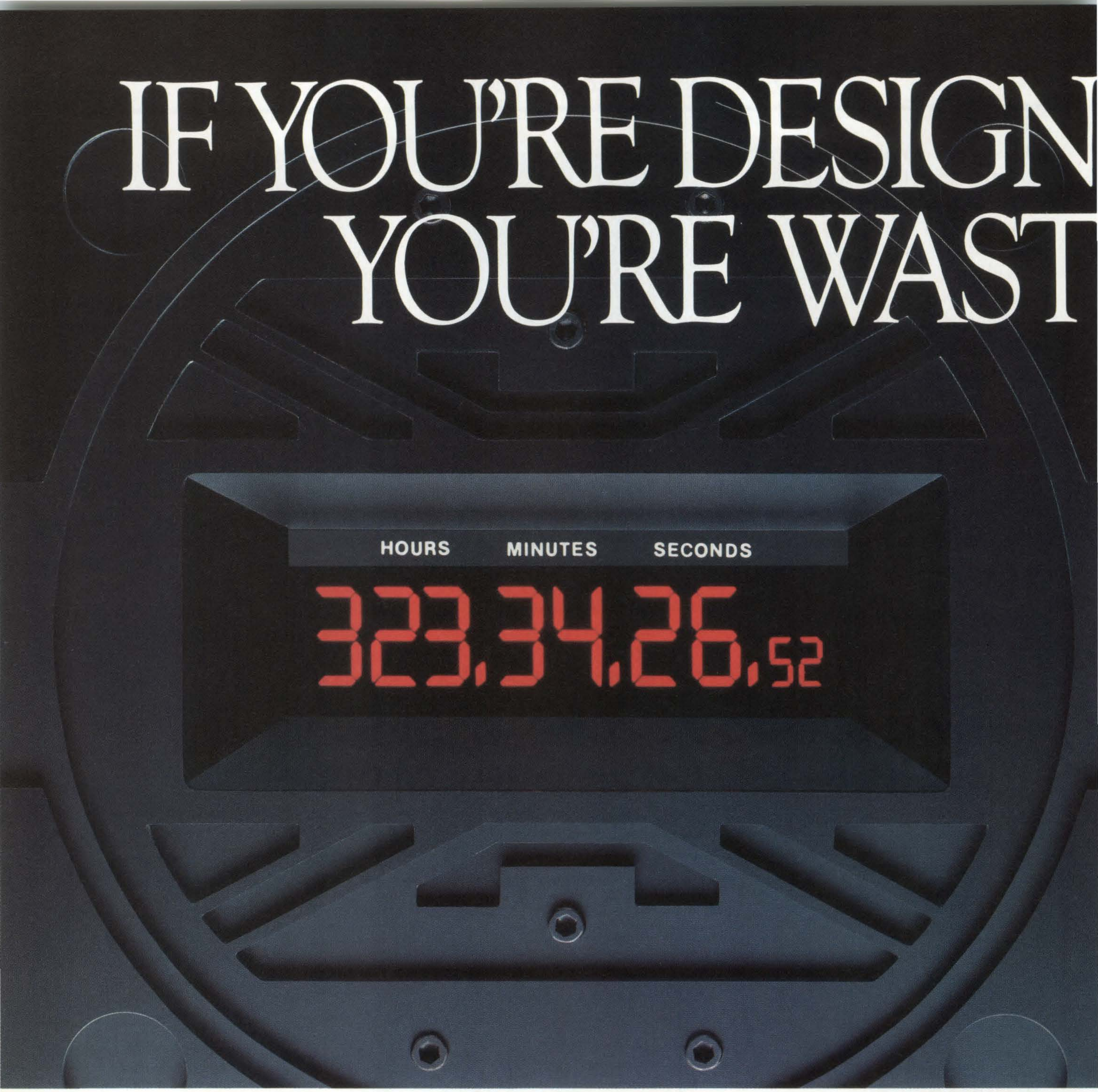
LED LAMPS

- *Replace T1-size filament lamps*
- *Available in five colors*

Operating from 15 to 28V dc supplies, LSMF125 Series T1-sized LED lamps are direct replacements for filament-bulb types. Compared to filament-bulb lamps, they offer high reliability, less heat generation, and lower power consumption. The lens incorporated into the lamp provides even illumination over its entire area, and an integral resistor controls the lamps' operating current. The T1-sized flanged lamp housing is 3.5 mm in diameter and 11 mm in length. The lamps are available with red, orange, amber, yellow, or green illumination. £2.97.

Marl International Ltd, Ulverston, Cumbria LA12 7RY, UK. Phone (0229) 52430. TLX 65100.

Circle No 380



Until now, if you wanted to put 50,000 gates on one chip, you usually had to put them in one at a time. You had to put in three months work. And you had to put your launch date into a holding pattern.

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Announcing the only compilers that take you to gate arrays and cells. Fast.

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ING YOUR TIME.

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We'll show you a good time.

To find out how much time you can save, call us for a free stopwatch.

VLSI TECHNOLOGY, INC.

CIRCLE NO 265

INTEGRATED CIRCUITS

DUAL OP AMP

- *Rail-to-rail operation for both input and output signals*
- *Features low-voltage and low-power operation*

The Si-Gate CMOS ALD-2701 is a dual op amp that allows the input and output signal levels to extend to the supply-voltage rails. For a single 5V supply, for example, the input and output voltage ranges are 0 to 5V. The parameters are specified at 5V, but you can use a 2 to 12V single supply or dual supplies of ±1 to ±6V. The maximum supply current for each op amp is 250 μA. The device has a unity-gain bandwidth of 0.7 MHz and a slew rate of 0.7V/μsec. Each amplifier can drive capacitive loads to 100 pF and remain unity-gain stable. The part is available in a plastic or ceramic DIP or in die form. In an 8-pin plastic DIP, it costs $0.89 (10,000).

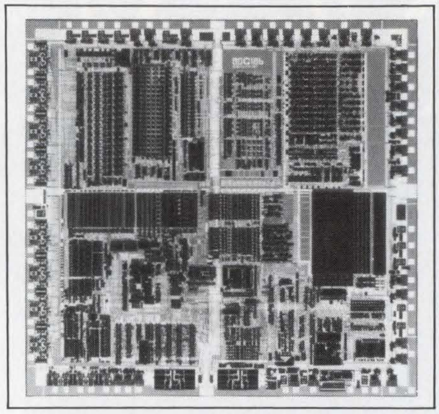
Advanced Linear Devices Inc, 1030 W Maude Ave, Suite 501, Sunnyvale, CA 94086. Phone (408) 720-8737. TWX 510-100-6588.

Circle No 381

12.5-MHz μP

- *Designed for embedded-control applications*
- *Offers multimode operation*

The 80C186 μP is an improved version of the original 80186 suitable for embedded-control applications and industrial and office automation. The μP is currently available in a 12.5-MHz version; a 16-MHz version is scheduled for the first



quarter of 1988. The device operates in several modes, including an HMOS-based 80186-compatible mode, a high-impedance test mode for in-circuit testing, and an enhanced mode with dynamic-RAM refresh and power-save logic. The dynamic-RAM-refresh controller is programmable to automatically generate refresh cycles every 18 to 512 clock periods. The system software development tools are the same as those for the 8086 and 80186. In a 68-pin plastic or ceramic LCC or ceramic PGA (pin-grid array) package, $18 (1000).

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (800) 548-4725.

Circle No 382

80286 µP

- *Offers performance nearly equivalent to 80386 systems*
- *Supports OS-2 and Microsoft Windows*

The 16-MHz 80286-16 µP speeds performance by 28% over its 12.5-MHz predecessor and provides a system performance more than twice that of an IBM PC/AT. Benchmark tests on an 80286-16 PC/AT

compatible indicate a performance equivalent to current 80386 PC/AT compatibles. An 80286-16-based system supports the OS-2 operating system as well as graphics environments such as Microsoft Windows. You can use the µP in the IBM PC/AT and compatibles, communications controllers, and engineering workstations. 68-pin LCC, $150; PGA (pin-grid-array) package, $175 (100).

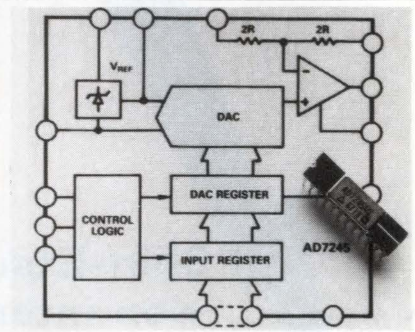
Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 982-7445.

Circle No 383

CMOS 12-BIT DACs

- *Include an on-chip output amplifier*
- *Provide an on-chip voltage reference*

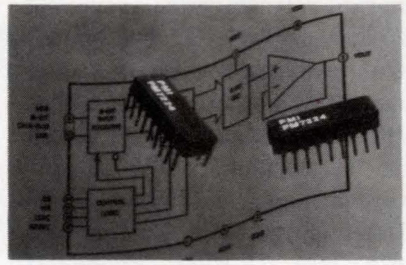
The AD7245 and the AD7248 D/A converters each include an on-chip amplifier and a voltage reference. A merged bipolar/CMOS fabrication process combines precision linear functions with high-speed digital logic. The settling time is 5 µsec. Both DACs operate from either a single or dual 15V supply and dissi-



pate 135 mW max. The AD7245 accepts data in a 12-bit format, and the AD7248 provides an 8+4-bit interface for use with 8-bit buses. Both devices incorporate high-speed logic (80 nsec) for direct interfacing with most μPs. They also include on-chip interface logic and a double-buffered latch structure for simultaneous update in multiple-DAC systems. The manufacturer guarantees monotonicity over three temperature ranges: 0 to 70°C (J grade); −25 to +85°C (A grade); and −55 to +125°C (S grade). Either device (J grade), $9.85 (100).

Analog Devices, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577.

Circle No 384



8-BIT CMOS DAC

- *Microprocessor compatible with double-buffered data inputs*
- *Guaranteed monotonicity*

Offered as an improved version, the PM-7224 is a multiplying 8-bit, voltage-output, CMOS D/A converter that features an internal amplifier capable of sourcing 5 mA and driving a 3300-pF load. The 8-bit registers have double-buffered inputs, allowing the simultaneous updating of multiple DACs in a system. Double buffering also minimizes the possibility of digital glitches appearing at the output. The PM-7224 contains a reset pin that functions as a zero override for DAC reset during power-up or for periodic calibration. The device operates with either a dual (15V, −5V) or a single (5 to 15V) supply. Commercial grade, $3.96; military 883 device, $27.84 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 310-371-9541.

Circle No 385

INTEGRATING ADCs

- *Provide 3¾-digit, high-resolution outputs*
- *Operating supply current is 100 μA*

The MAX133 and MAX134 are low-power CMOS integrating A/D converters that provide 3¾-digit, high-resolution outputs. When operating from 9V supplies, the ADCs draw a supply current of 100 μA (25 μA in standby mode). The devices also provide seven input channels, on-board switches for range and mode

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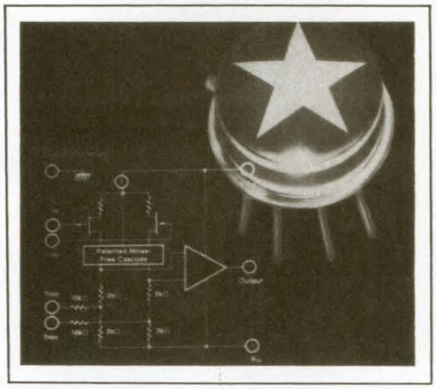
CIRCLE NO 264

selection, signal resolution to 10 μV, and μP interface circuitry. Their conversion rate is 20 readings/sec. Combining an external resistive attenuator with the μP-controlled range switches allows signal measurements over a range of five decades. Mode-selection switches, also under μP control, switch between voltage and current (either ac or dc) and ohms. Both devices offer a normal-mode rejection of at least 80 dB at line frequencies. The MAX133 has a multiplexed address/data bus that reduces the number of I/O lines for interfacing to 4-bit μPs. The MAX134 has a separate 4-bit bidirectional data bus and three address inputs that simplify interfacing to 8-bit μPs. 40-pin plastic DIP, \$11; 44-pin plastic chip carrier, \$12.10 (100).

Maxim Integrated Products, 510 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 386



MILITARY OP AMP

- *MIL-STD-883B processing*
- *Low noise, high open-loop gain, and high CMRR*

For military and high-reliability systems, the OPA111/883B offers precision performance and radiation hardness. The device is manufactured in production facilities certified by the Defense Electronics Supply Center for MIL-STD-976A monolithic circuits. Circuit-design techniques and low-noise processing result in a noise floor of 8 nV/$\sqrt{\text{Hz}}$ at 10 kHz, and dielectric isolation makes possible the low bias current of 2 pA. The device also features low offset voltage and low drift. \$27 (100).

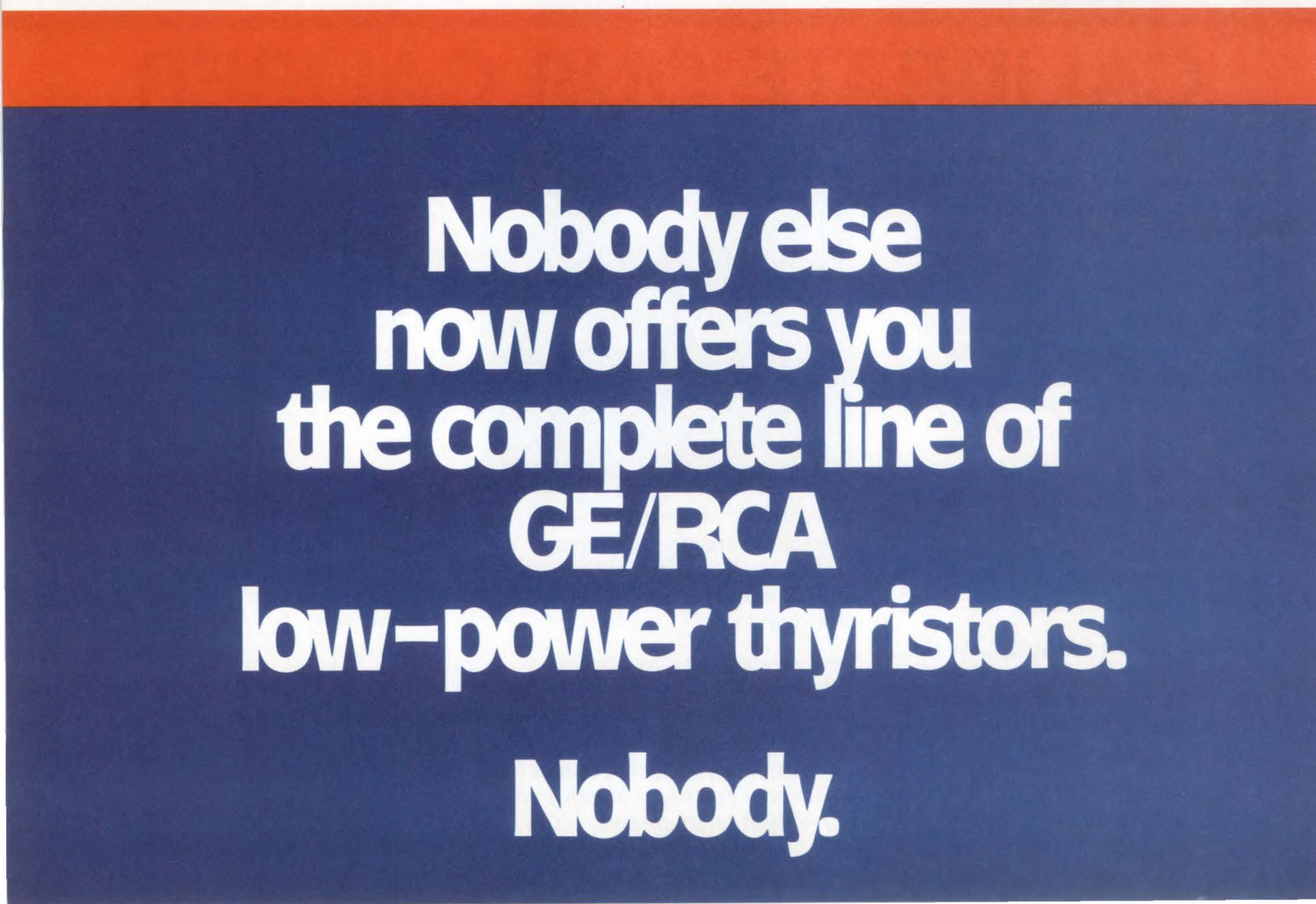
Burr-Brown, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

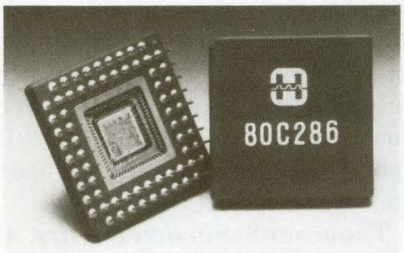
Circle No 387

CMOS 80286 μP

- *Specs a maximum 12.5-MHz clock rate*
- *Reduces power 60% compared to NMOS 80286*

The static CMOS 80C286-12 μP has a maximum clock rate of 12.5 MHz and a worst-case supply current of 20 mA/MHz. For the 12.5-MHz operating frequency, the 20-mA/MHz rating yields a power reduction of approximately 60% compared to the NMOS 80286 version and ap-





proximately 40% compared to the 80L286. The μP is compatible with the NMOS 80286 and includes multitasking support capability and on-chip memory-management circuitry. Operating in the static mode, an 80C286-based system can realize as much as a 90% power savings by stopping the system clock or reducing the operating frequency. The device has a minimum frequency of dc, which is the same dc-to-maximum-frequency range as for the 80C86 and 80C88. Using an 80C286 as the host, you can add static, software-compatible 80C86 and 80C88 satellite processors and have complete control over power, operating frequency, and throughput. $125 to $170 (100).

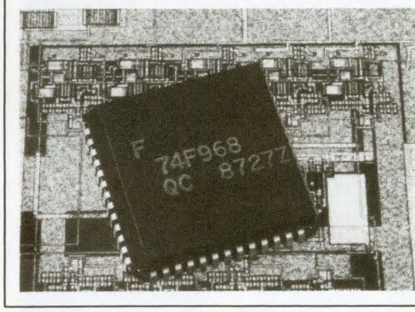
Harris Corp, Semiconductor Sector, Box 883, Melbourne, FL 32901. Phone (305) 724-7418.

Circle No 388

RAM CONTROLLER

- *Dedicated controller for 1M-bit dynamic RAMs*
- *Fast LSI II process means low propagation delay*

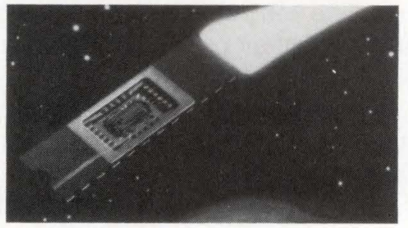
The 52-pin 74F968 provides row- and column-address multiplexing, refresh-address generation, and bank selection for as many as four banks of 16k-, 64k-, 256k-, or 1M-bit dynamic RAMs. It has two 10-bit address latches and two 10-bit counters for row- and column-address generation during refresh. A 2-bit bank-select latch switches two high-order address bits to select one of



the four RAS (row address select) and CAS (column address select) outputs. The typical current drain is 265 mA. The unit eliminates the need for multiple controllers for the same function. It is functionally equivalent to the 2968 dynamic-RAM controller, but addresses four times the memory-array size and directly drives as many as 88 dynamic RAMs. In a plastic LCC, $30 (100).

Fairchild Semiconductor Corp, 333 Western Ave, South Portland, ME 04106. Phone (800) 554-4443.

Circle No 389



FAST 12-BIT DAC

- *35-nsec settling time to within ±0.025% of full scale*
- *±½-LSB max integral linearity error*

The AD568 is built using a proprietary complementary bipolar-process technology that combines high-speed npn and pnp transistors on the same chip to achieve high-speed switching and current steering. The chip includes an accurate buried-zener reference and a variable threshold adjust for TTL or CMOS logic compatibility. Typical applications for the AD568 are waveform generation and video graphics displays; it is also suitable as a building block in high-speed and high-resolution successive-approximation A/D converters. Depending on grade and temperature range, \$35 to \$108 (100).

Analog Devices, Literature Ctr, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TWX 710-394-6577. TLX 174059.

Circle No 390

STATIC RAM/CALENDAR

- *Includes 11-year battery backup*
- *Has on-chip power-fail detection*

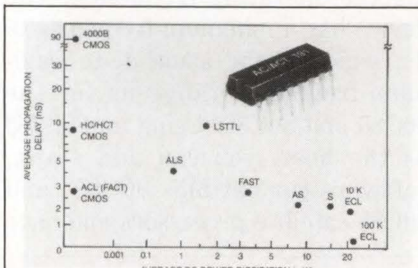
The MK48T02/12 is a 2k×8-bit CMOS static RAM that also incorporates a real-time clock/calendar, quartz crystal, and lithium battery in its 24-pin JEDEC-standard DIP package. The RAM is available in various speed versions with access times ranging from 120 to 250 nsec. The clock/calendar provides a 24-hour clock and calendar information with leap-year correction as BCD format data. Its lithium carbon monofluoride battery has a worst-case life of 45 years at 55°C or 11 years at 70°C. To ensure data integrity, on-chip circuitry automatically deselects the RAM during power-down conditions. The MK48T02/12 operates from a 5V supply and operates over 0 to 70°C. \$19 (1000).

Thomson Semiconducteurs, 45 Ave de l'Europe, 78140 Velizy, France. Phone (1) 39469719. TLX 204780.

Circle No 391

Thomson Components-Mostek Corp, 1310 Electronics Dr, Carrollton, TX 75006. Phone (214) 466-6000. TLX 730643.

Circle No 392



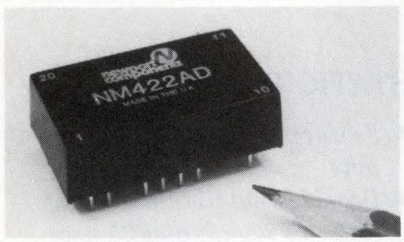
BINARY COUNTERS

- *Presettable, synchronous 4-bit up/down counters*
- *Advanced CMOS logic ensures high speed and low power*

You can asynchronously preset the CD54/74AC/ACT191 ACL (advanced CMOS logic) counters to a desired number, but counting up or down occurs synchronously. A single up/down pin determines the direction of the count. The counters are incremented or decremented synchronously on the low-to-high transition of the input clock. When the count-enable (CE) pin is high, no counting occurs and the count remains at its previous value. Each counter provides two pins for cascading devices. The terminal-count (TC) pin, which is low during counting, goes high for one clock cycle to indicate either an overflow or underflow. You can use this output for look-ahead-carry operations in high-speed cascaded applications. When the TC pin goes high, it triggers the ripple-clock (RC) pin, which goes low and remains so for the low-level portion of the clock pulse. This output is also suitable for look-ahead-carry operations. The counters' performance and drive parameters match the parameters of bipolar Fast parts. The maximum propagation delay from an input clock pulse to data output is 13.8 nsec for the AC models and 14.8 nsec for the ACT models. Both versions can sink and source 24-mA drive currents; the maximum clock frequency is 65 MHz. An industrial-temperature-range counter in a 16-pin plastic DIP costs $3.05 (100).

GE Solid State, Rte 202, Somerville, NJ 08876. Phone (201) 685-6562.

INQUIRE DIRECT



INTERFACE MODULE

- *Implements two full-duplex RS-232C to RS-422A links*
- *Operates from one 5V supply*

Providing a direct interface between RS-232C and RS-422A serial data links, the NM422AD pc-board-mounting interface module allows you to convert between RS-232C and RS-422A without the need for multirail power supplies or dc/dc converters. The module has sufficient drivers and receivers to provide two full-duplex links. It operates from a single 5V supply and typically consumes 300 mW of power. The NM422AD is housed in a DIP package with a 17×30-mm footprint and a height of 9 mm; pins are on a 0.1-in. pitch with 0.5-in. pin-row spacing. It has an operating temperature range of 0 to 70°C. $18 (1000).

Newport Components Ltd, Tanners Drive, Blakelands North, Milton Keynes MK14 5NA, UK. Phone (0908) 615232. TLX 825621.

Circle No 394

TRANSCEIVER ICs

- *Support star and bus topologies*
- *Interface between the LAN cable and the controller*

The XR-T82515/T82C516 StarLAN transceiver chip set performs all interface functions between the LAN cable and the LAN controller in accordance with IEEE specifications. The chip set is compatible with the Intel 82586 and 82588 communication controllers. A proprietary on-chip adaptive hybrid provides 100% collision detection by automatically adapting to the cable impedance and sense-level changes on the cable. The chip set features Manchester encoding/decoding, transmit waveshaping, a receive filter, a carrier energy detector, and jabber-control functions. Using 24-AWG twisted-pair cable, you can use the chip set with 1600-ft cable lengths (14 dB attenuation) in the bus configuration and 2400-ft cable lengths (20 dB attenuation) in the star configuration. The worst-case S/N ratio is 3 dB, which provides a bit-error rate of more than 10^{-8}. In a plastic DIP or a plastic LCC, $17.50 (1000).

Exar Corp, Box 49007, San Jose, CA 95161. Phone (408) 434-6400. TWX 910-339-9233.

Circle No 395

REGULATOR ICs

- *Have separate regulator outputs for battery-backed circuitry*
- *Generate µP reset signals*

To simplify the design of systems that require battery backup of certain circuitry, the SGS L4901, L4902, L4903, and L4904 voltage regulators have two separate 5V regulator outputs, one of which specifies a leakage current of less than 1 μA. This low-leakage regulator section also has a quiescent input current drain of only 0.6 mA, suiting it for operation with battery supplies. The second 5V output is suitable for driving circuitry that doesn't require backup. The devices also generate a μP reset signal during power-up, after brief supply interruptions, or when the output to the battery-backed section of a circuit falls below a safe value (4.9V typ). You can control the reset-period timing with one external capacitor. The L4901 and L4902 are housed in 7-lead Heptawatt plastic packages; each provides a 5V/0.3A output for battery-backed circuitry and a 5V/0.4A output for other circuitry. The L4901 has separate inputs for the two regulator sections, whereas the L4902 has a common regulator input. The L4903's and L4904's outputs are rated at 5V/0.1A; both devices have separate inputs to their two regulator sections. They are housed in 8-pin miniature DIPs and have TTL/CMOS-compatible disable inputs that control the outputs not designed for battery-backed circuitry. All four models have input overvoltage protection (to 60V) and output short-circuit and thermal-overload protection. The price is around $3 (100).

SGS Microelettronica SpA, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

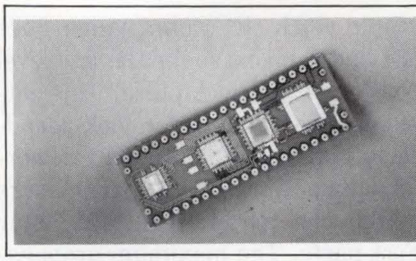
Circle No 396

SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 397

CMOS MODULE

- *System on a substrate*
- *Suitable for process control or data acquisition*



The EDI6F87C31-8PC CMOS μPak is targeted for process-control or data-acquisition applications where space is at a premium. The CMOS hybrid contains an 80C31 microcontroller, an 8k×8-bit static RAM, an 8k×8-bit ultraviolet EPROM, and a proprietary logic-control unit. The epoxy-encapsulated, chip-on-board assembly yields a cost reduction of greater than 30% when compared to the price of the same device in a ceramic module. Device samples are available now; full production is scheduled for the first quarter of 1988. $100 (100).

Electronic Designs Inc, 42 South Street, Hopkinton, MA 01748. Phone (617) 435-2341. TLX 948004.

Circle No 398

STATIC RAMs

- *Features TTL inputs and outputs*
- *Provides maximum address times of 20, 25, and 35 nsec*

These two BiCMOS static RAMs, the SSM2148 and SSM2149 1k×4-bit devices, are available with maximum address times of 20, 25, and 35 nsec. They are replacements for Cypress's CY7C148 and CY7C149 and other equivalent parts, and are designed for use as high-speed cache buffers in minicomputers and graphics workstations. The devices have TTL inputs and outputs, and they are enclosed in 18-pin ceramic DIPs. Both parts have an operating power of 250 mW. The SSM2148 has an automatic power-down feature and draws 50-mW standby; the SSM2149 has a power-down mode that dissipates 110 mW when deselected. $8.55 to $11.95 (100).

Saratoga Semiconductor, 10500 Ridgeview Ct, Cupertino, CA 95014. Phone (408) 973-0945.

Circle No 399

New low price

Score a Whole In One

Score the MS-DOS-Compatible System On a Chip from NEC

Now you can score on your next round of systems designs *and* parlay your MS-DOS investment. Simply use our CMOS V25™ Whole in One™ — the new 16-bit microcomputer on a chip from NEC.

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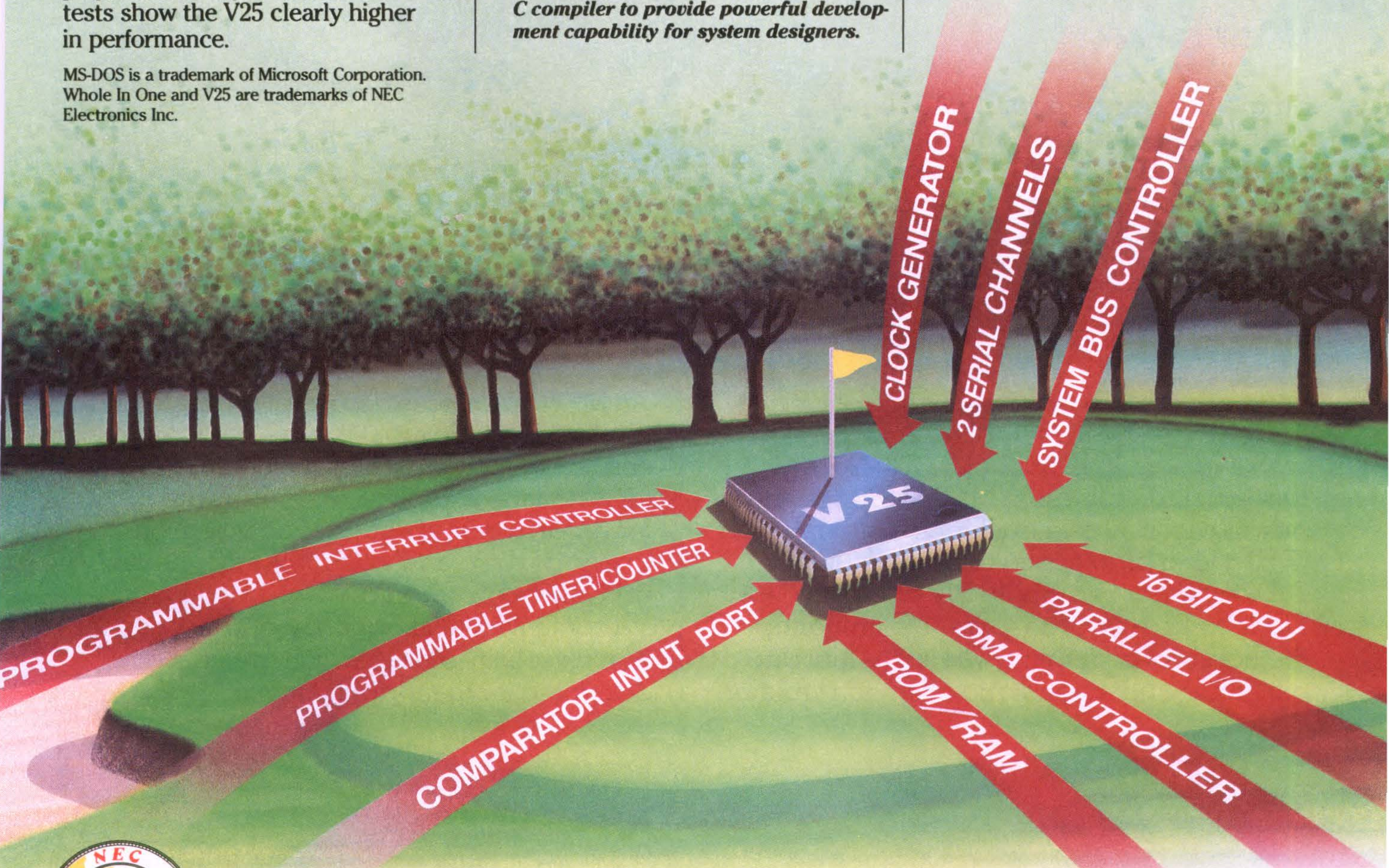
NEC Electronics Inc.
401 Ellis Street, P.O. Box 7241
Mountain View, CA 94039



NEC WHOLE·IN·ONE V25

The V25 is now on distributor shelves for immediate delivery

NEC

CIRCLE NO 263

FFT-TESTED 12-16 BIT SAMPLING A/D's

MIL-STD-1772 CERTIFIED

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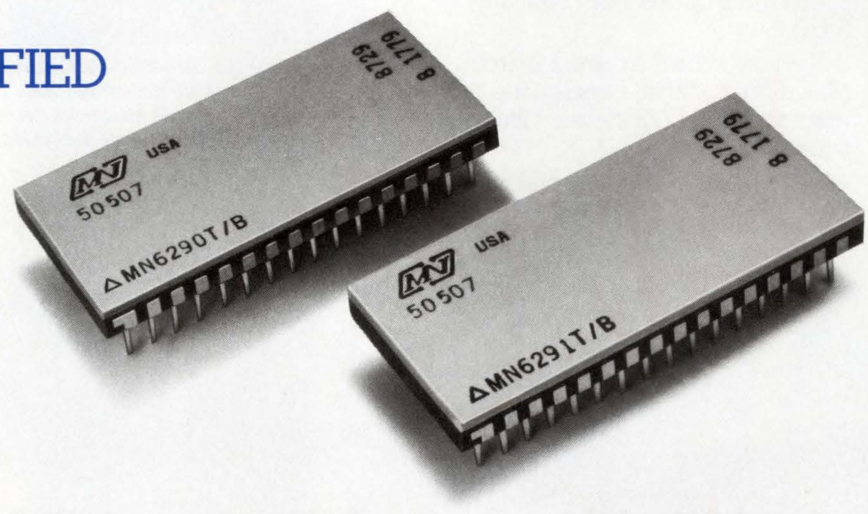
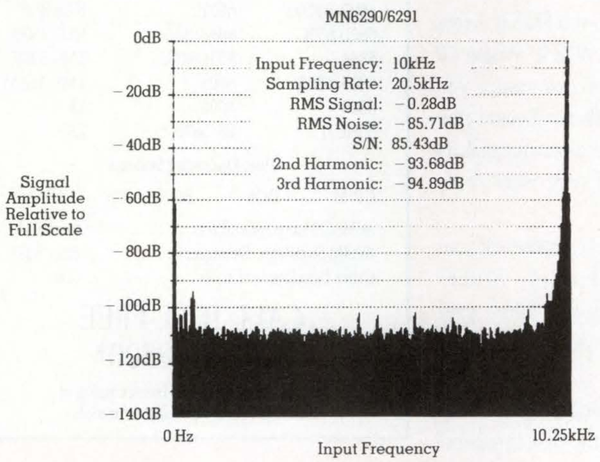
  MN6231/6232: 50kHz 12 Bits
  MN6227/6228: 33kHz 12 Bits
MIL-STD-883 Screening

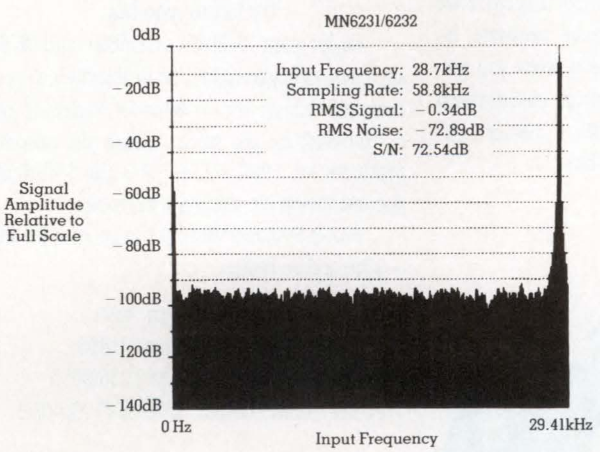


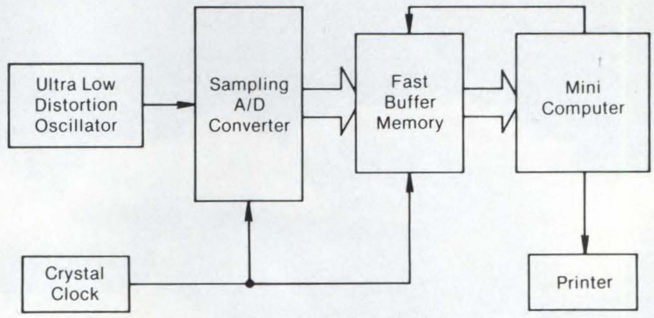
For you, we've expanded our line of FFT-tested, high-speed, sampling A/D converters with two new 16-bit models: MN6290 and MN6291. Like our entire MN6000 Series, these new devices mate a track-and-hold amplifier (T/H) with a high-speed, high-resolution, A/D converter in a single DIP package. The T/H is completely transparent, eliminating the hassle of evaluating T/H specs that are difficult to understand and often don't relate.

All MN6000 devices accurately sample and digitize dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). They are ideal for radar, sonar, spectrum and vibration analysis, voice and signature recognition, and other contemporary DSP applications. All come with full frequency-domain performance specifications, which are critical to designing for these applications.

Micro Networks was the first to apply FFT testing to A/D converters. We recognized that this would be the key to specifying A/D's for emerging DSP applications. In our frequency-domain testing, sampling A/D's operate in a manner that simulates a digital spectrum analyzer with a known low-distortion input signal. The output spectra yield precise, practical measurements of signal level, noise level, signal-to-noise ratio, harmonic distortion, and input bandwidth, giving you the performance specifications you need to design to your application. Our testing clearly demonstrates the ability of our MN6000 Series devices to maintain near-ideal signal-to-noise ratios independent of increasing analog input frequencies.







Frequency-Domain Testing of A/D Converters

All MN6000 Series devices are packaged in standard ceramic DIP's and are available fully specified for −55°C to +125°C with MIL-STD-883 screening. 12-bit models contain full 8 or 16-bit μP interfaces. Select the device that best meets your design requirements.

Part Number	Input Range	Minimum Sampling Rate	Minimum Input Bandwidth (Note 1)	SNR (Note 2)	Harmonics
12-Bit Resolution					
MN6227	10V	33kHz	16.5kHz	70dB	−80dB
MN6228	20V	33kHz	16.5kHz	70dB	−80dB
MN6231	10V	50kHz	25kHz	70dB	−80dB
MN6232	20V	50kHz	25kHz	70dB	−80dB
16-Bit Resolution					
MN6290	10V	20kHz	10kHz	84dB	−88dB
MN6291	20V	20kHz	10kHz	84dB	−88dB

1. Input bandwidth for which SNR and harmonic specs are guaranteed when sampling at the minimum guaranteed rate.
2. Signal-to-noise ratio (r.m.s. to r.m.s.) with full-scale (0dB) input.

For detailed information on MN6290/6291 or other high-speed sampling A/D's in our expanding line, send for our comprehensive data sheets. For rapid response, call Russ Mullet at Ext. 208.

Micro Networks
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Worcester, Massachusetts 01606
(617) 852-5400

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CIRCLE NO 262

KEEP TIME

Keeping track of human time hasn't been easy for computer systems.
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The SmartWatch DS1216 and DS1216E from Dallas Semiconductor keeps and reports precise time of day, date and hour, down to the one hundredth of a second. With the SmartWatch, all electronic transactions can be accurately time documented without manual entry.

The SmartWatch is well designed and easy to use. A CMOS timekeeping circuit embedded in a JEDEC Bytewide 28 pin DIP Socket saves you a boards worth of real estate. And no hardware design modification is necessary to make your existing systems keeptime.

The DS1216 and 1216E circuitry and self contained energy source do more than maintain calendar time. They convert any CMOS RAM into a nonvolatile memory when mated to a socket or an EPROM. And the memory transfers are not restricted by the presence of the time keeping function.

SmartWatch: a design whose time has come.

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CIRCLE NO 260

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CYPRESS
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VTI
16V8, 20V8
EEPLDS

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77153 HPL

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DIP, PLCC EPLD

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TEST & MEASUREMENT INSTRUMENTS

COMPONENT TESTER

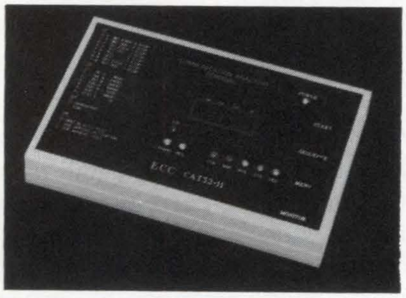
- *Tests digital and linear ICs*
- *Has 16-bit ADC and an rms-to-dc converter*

The SZ-M3000 benchtop tester is used mainly for incoming inspection and tests digital and linear ICs. It can supply 600V or 50A to the device under test and can test SSI/MSI logic devices (CMOS and TTL), op amps, A/D and D/A converters, diodes, transistors, SCRs, triacs, optoisolators, resistors, inductors, capacitors, and passive-component networks. An HP310 68010-based workstation with a 14-in. graphics display, an ink-jet printer, 2M bytes of RAM, a 710k-byte floppy-disk drive, a 20M-byte hard-disk drive, an RS-232C port, and an IEEE-488 port provides control, programmer and operator interface, and report generation. You can program the test limits for many devices using menus; a Pascal-based language allows you to write programs for other parts. A 12-way multiplexer enables you to rapidly switch the 16-bit voltmeter from device pin to device pin; an S/H amplifier allows the voltmeter to accurately digitize time-varying signals. In addition to the meter, standard instrumentation includes a low-current I-to-V converter for leakage measurements; nine programmable voltage sources; three fixed-voltage sources; a bidirectional current source; a 16-bit-resolution time-measurement unit; a pattern generator; a programmable sine-wave generator; a ramp generator; a 32-bit serial-to-parallel converter; 16 digital I/O lines; a voltage standard; and an automatic calibration unit. You can add automatic device handlers and a crosspoint matrix. $75,000. Delivery, 90 days ARO.

SemiTech International, 100 Fifth St, Boston, MA 02129. Phone (617) 242-5222. TWX 650-291-1632.

Circle No 400

CIRCLE NO 74



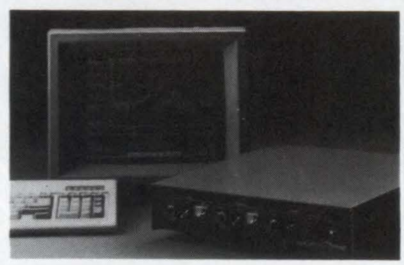
PORT ANALYZER

- *Automatically identifies RS-232C port to be tested*
- *Indicates data rate, format, start/stop control mode*

You can use the 2-lb, 6×9×2-in., 68000-based CAT-32 communications analysis terminal in a standalone mode or with a terminal you provide. After you connect it to a port to be tested and push a single button, the analyzer automatically sequences through all the normal RS-232C conditions that can make the port echo received data; it then identifies data rate, data bits/character, parity (even, odd or none), number of stop bits, and type of handshake. The unit also indicates X-On and X-Off conditions, whether the DCD (data carrier detect) line is used, and the activity on the TXD (transmitted data) and RXD (received data) lines. While testing, it dynamically interchanges TXD- and RXD-line function. You can use a menu-driven manual mode to gain tighter control over the analysis process—for example, when the protocol uses nonstandard characters for X-On or X-Off. For interactive debugging, the unit gives you access to a firmware-resident monitor that provides single-step execution and breakpointing. $1495. Delivery, 90 days ARO.

ECC, ATE Instruments Div, 4650 Cedar Ridge Pl, Oceanside, CA 92056. Phone (619) 434-2026.

Circle No 401



ANALYZER/SCOPE

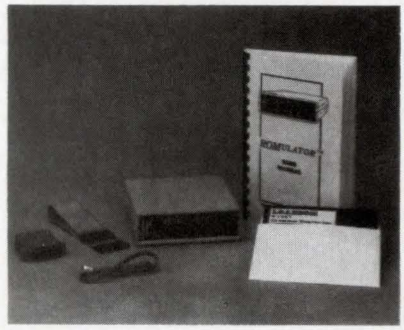
- *Displays waveform and spectrum simultaneously*
- *Uses IBM PC, PC/XT, PC/AT or compatible computer*

The R370 is a combination spectrum analyzer/digital oscilloscope. It works with an MS-DOS-based IBM PC, PC/XT, PC/AT, or a compatible computer having 5¼-in. disk drives, at least 512k bytes of RAM, CGA (color graphics adapter) graphics, and a CGA-compatible color or mon-

ochrome monitor. It enables your computer to act as both a spectrum analyzer and a digital scope capable of simultaneously sampling two channels at a rate of 20M samples/sec. Using this device, you can display a waveform on the same screen as its spectrum in real time. The unit offers selectable 50Ω or 1 MΩ input impedance, sensitivity adjustable from 1 mV to 50V/div, automatic calibration, an internal or external trigger, pretriggering and post-triggering, a 64k-byte buffer for each channel (128k bytes optional), manual or automatic disk storage and retrieval of acquired data, and X-Y display capability. The spectrum analyzer handles frequencies of 10 MHz and below, executes a 1024-point FFT in 60 msec, allows you to average as many as 64 spectra, performs post-averaging on data streams as long as 64k bytes, and displays data with either linear or log scaling. $4495.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98013. Phone (206) 547-8311. TLX 265017.

Circle No 402



ROM EMULATOR

- *Modifies ROM code during debug while power is on*
- *Emulates one to eight ROMs*

The Romulator in-circuit ROM emulator measures 5.08×5.25×1.5 in. It receives power from a 5V supply in your system and connects to the target-ROM sockets via DIP cables; another cable connects it to a host-computer RS-232C port. During debug, you can modify ROM code without turning off your system. The emulator comes with software for downloading data from the host. Models are available in 256k- and 512k-bit sizes. Both emulate low-capacity 24- and 28-pin parts. The units can be configured to emulate one or two ROMs, and you can interconnect multiple units to emulate larger ROM arrays. Where multiple ROMs in a system contain identical data, you can load their emulators simultaneously. An optional nonvolatility feature preserves data in the simulated ROMs when power is shut down. $400 to $1100.

Grammar Engine Inc, 1021 Tipton Ct, Westerville, OH 43081. Phone (614) 882-6366.

Circle No 403

SCSI TESTER

- *Supports device-specific commands*
- *Permits evaluation of as many as seven DUTs*

The Model 512 SCSI tester runs on an 8-MHz 80186 μP, 1M byte of RAM, and menu-driven, MS-DOS-based software. It allows you to send single commands or groups of commands to the device under test (DUT). You need no knowledge of programming languages to set up test sequences and to store them on a floppy disk in the tester's disk drive. The software supports the connection of as many as seven DUTs and their testing in a user-defined sequence. The unit requires a user-supplied alphanumeric terminal for operation and can provide as much as 45W dc to power the DUT. $2995.

AVA Instrumentation Inc, 8010 Highway 9, Ben Lomond, CA 95005. Phone (408) 336-2281. TWX 510-100-7906.

Circle No 404

GENERATOR UPGRADE

- *Supplies redesigned front panel*
- *Adds more IEEE-488 programming commands*

The HP 86606A retrofit program upgrades the HP 8660D synthesized signal generator with new front-panel and programming functions. The IEEE-488 interface, previously an option, is standard on the upgraded version. The retrofit adds this interface to units that lack it and replaces the older optional interface on units equipped with it. The commands are a superset of the earlier vocabulary, so software that operates older generators will continue to work after the retrofit. The retrofit replaces the existing power supply with one that operates from 50 to 400 Hz, substitutes redesigned attenuators in the RF plug-ins, and provides a new timebase equivalent

CIRCLE NO 77

to the former optional high-stability timebase. Retrofit, $7500; new generator, $14,000; plug-ins $700 to $9900. Delivery, six weeks ARO.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 405

80286 TEST POD

- *Interfaces with pin-grid-array and LCC sockets*
- *Adapter clips onto soldered-in LCCs*

The 80286 interface pod works with the vendor's 9000 Series microsystem troubleshooter and 9100A digital test system. You can use it to write data to or read data from any location that the μP can address. The pod is clocked by the UUT (unit under test) clock signal; you can supply clocks at frequencies from 4 to 25 MHz without adding wait states. You can set hardware breakpoints as an optional means of terminating a Run UUT operation, and 8k bytes of overlay RAM can replace the UUT memory. Six quick-test modes are built-in, as are protection against improper voltages on the UUT pins and self tests to verify pod operation and UUT-cable continuity. $2995. Delivery, eight weeks ARO.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 426-0361; in WA, (206) 347-6100. TWX 910-445-2943. TLX 185102.

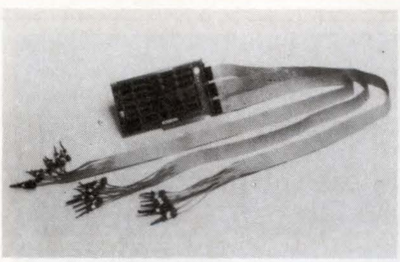
Circle No 406

LOGIC ANALYZER

- *Plugs into IBM PC I/O bus*
- *Handles 24 50-MHz TTL signals*

The PC-29 logic analyzer is a half-sized I/O card for the IBM PC, PC/XT, PC/AT, and 100%-compatible computers equipped with CGA (color graphics adapter), EGA (enhanced graphics adapter) or Hercules display adapters and at least 256k bytes of RAM. Minijack-equipped input cables plug directly into the rear of the card with no external pod; they can be disconnected without opening up the computer. With the card installed, the computer can function as a 24-chan-

TEST & MEASUREMENT INSTRUMENTS



nel logic analyzer with 1k samples of memory for each channel. If you need only six channels, you can configure the analyzer to store 4k samples/channel. You can set the internal clock to any of eight frequencies from 25 kHz to 50 MHz, or you can supply an external clock at a frequency as high as 25 MHz and trigger on the rising or falling edge. You can begin the data display from 64 to 960 clock periods before or after the trigger point. $749.

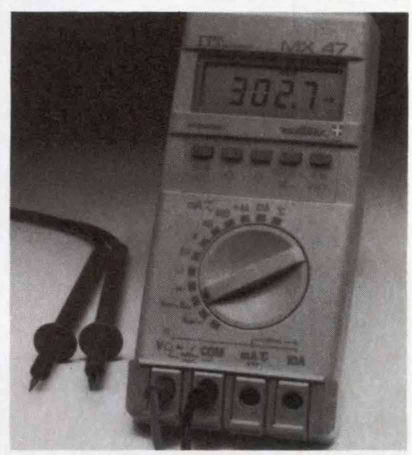
El Toro Systems, 23702-B Birtcher Dr, El Toro, CA 92630. Phone (714) 770-1474. TWX 910-240-7216.

Circle No 407

DMMs

- *Provide a full range of 4000 counts*
- *Include an analog peak-hold facility*

Ruggedized to withstand field-service use, the MX40 Series handheld autoranging DMMs withstand shock and vibration to MIL-T-28800C levels. Several models have sealed cases that are waterproof to MIL-T-28800A requirements. They feature a full range count of 4000, allowing you to measure, for example, 400 to 0.1V resolution. Autoranging or manual ranging is provided for dc-voltage, ac-voltage, and resistance measurement. Autoranging on the dc- or ac-voltage function extends down to the 400-mV range. In addition, an analog peak-hold facility provides peak-hold acquisition time of 5 msec typ. Current measurement ranges for ac or dc current extend from 400 μA to



10A and are fully protected on all ranges. Typical voltage drop in the meter for current measurement is 500 mV. Basic dc accuracy ranges from 0.7 to 0.1% depending on the model. The top-of-the-line model—the MX47—includes rms measurement on ac voltage and current, and ac or ac and dc coupling. You can also use the MX47 with K-type thermocouples to provide a direct readout of temperatures as high as 400°C. All models conform to IEC348 class 2 safety standards and have input leads that you can lock into the instrument. £89 to £179.

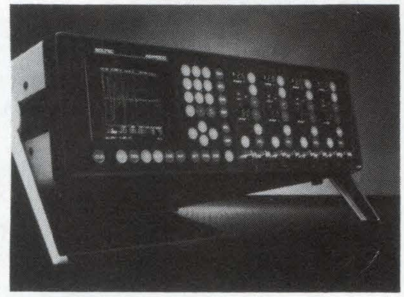
ITT Instruments, 346 Edinburgh Ave, Slough, Berkshire SL1 4TU, UK. Phone (0753) 824131. TLX 849808.

Circle No 408

TRANSIENT RECORDER

- *Has dual-timebase*
- *Accepts a variety of plug-ins*

The ADA1000 is a portable, 2- to 12-channel transient-waveform recorder. The dual-timebase instrument's mainframe accepts a variety of plug-in sampling modules. The fastest module records at 20M samples/sec with 10-bit resolution; the slowest provides 12-bit resolution. Each has a 64k-sample memory. You can chain or partition all of the modules' memories to achieve record sizes ranging from 512 samples to 0.75 megasamples. The instrument's plug-ins have programmable input amplifiers and can operate under software control. The instrument comes with RS-232C and IEEE-488 interfaces. It has direct outputs for X/Y plotters and matrix printers. $13,275. Delivery, 30 to 60 days ARO.



Soltec Corp, Sol Vista Park, San Fernando, CA 91340. Phone (800) 423-2344; in CA, (818) 365-0800.

Circle No 409

INDUCTOR CHECKER

- *Measures chokes, coils, and transformers*
- *Broad range of voltage, current, and frequency stimuli*

The 3240 analyzes chokes, coils, and transformers. It measures L, C, R, D, Q, Z, dc-resistance, phase-angle, and transformer-turns ratio. It generates excitation signals ranging in frequency from 20 Hz to 300 kHz, and it applies constant-voltage stimuli ranging from 10 mV to 5V rms or constant-current from 1 to 100 mA rms. DC-bias currents from 1 mA to

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• one of the first VLSI design and production centres to be AQAP 1* approved in Europe.
1987 : first with 64K CMOS SRAM 1.2. microns and soon first with a CMOS process at 0.8. micron.

(*) AQAP1: allied quality assurance publication level 1.

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Tél.: 30.60.70.00

Matra Design Semiconductor
2840-100 San Tomas Expressway
Santa Clara CA 95051
USA
Tél.: 408/986-9000

Italy, Milano 2.4984586 • Sweden, Stockholm 08-7348390 • UK, London 344-485757 • Germany, München 89-31900550 • Far East, Hong Kong 5-8327993.

dp industries

1A are also available. The instrument's overall accuracy is 0.1%. It accepts 4-wire measurement setups, and it stores lead-nulling correction factors in nonvolatile memory. $8400.

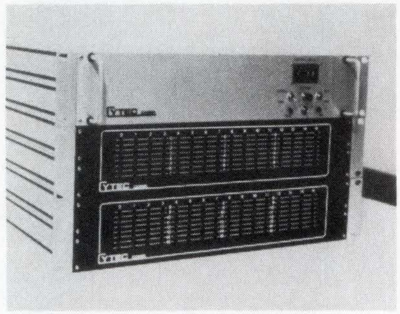
Wayne Kerr Inc, 600 W Cummings Park, Woburn, MA 01801. Phone (617) 938-8390. TLX 6817257.

Circle No 410

ANALOG MATRIX

- *Coax, low-voltage, and high-voltage switches*
- *Expands to 4096 2-pole crosspoints*

The Mesa Series matrix expansion systems handle voltages from 1 μV to 1 kV, 2A currents, and RF signals at frequencies as high as 100 MHz. The system consists of a 3½-in. rack-mountable control mainframe and as many as 32 3½-in. rack-mountable expansion chassis,



each accommodating from one to 16 plug-in cards; each card contains eight 2-pole crosspoints for a maximum of 4096 crosspoints. The crosspoints can be a mixture of coax, low-voltage and high-voltage types. The control options include an RS-232C, an IEEE-488, or a 16-bit-parallel bus. Configured with IEEE-488 and 128 double-pole low-level channels, $3200.

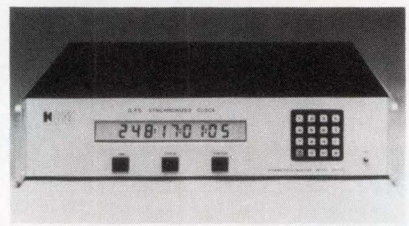
Cytec Corp, 2555 Baird Rd, Penfield, NY 14526. Phone (716) 381-4740.

Circle No 411

RECEIVER/CLOCK

- *Receives timing sync from Navstar satellite system*
- *Time codes traceable to UTC/USNO within ±200 nsec*

The GPS-DC synchronized clock receives signals transmitted by any satellite in the Navstar GPS (global positioning system), which will be fully operational in the early 1990s. The clock generates 1-, 5-, and 10-MHz square waves, IRIG-B time codes, and a 1-Hz reference pulse. You can use an alternate time reference when the Navstar satellites are not in view. The unit includes an RS-232C interface. It can be pow-



ered from a 110 or 220V ac line or from 10 to 40V dc. Optional functions include IRIG-E and -H time codes, and parallel-BCD and IEEE-488 interfaces. $15,500. Delivery, 90 days ARO.

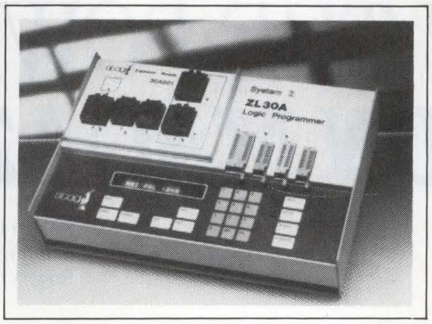
Kinemetrics/TrueTime, 3243 Santa Rosa Ave, Santa Rosa, CA 95407. Phone (707) 528-1230. TLX 176687.

Circle No 412

PLD ADAPTER

- *Extends programmer capabilities to SMDs*
- *Handles SMD versions of 750 DIP devices*

The 30A0001 expansion module allows the vendor's ZL30A programmer to handle the SMD equivalents of all DIP parts it can program. Included are PAL, IFL (integrated fuse logic), EPLD (erasable programmable logic device), and GAL



(generic array logic) devices. $600.

Stag Microsystems, 1600 Wyatt Dr, Santa Clara, CA 95054. Phone (800) 227-8836; in CA, (408) 988-1118. TWX 910-339-9607

Circle No 413

VLSI TESTER

- *Configurable with 352 bidirectional pins*
- *Clocks at 50 MHz with ±1.5-nsec skew*

The 64-channel STM5200 digital VLSI test system measures 21×24×16 in., not including the IBM PC/AT-compatible test system controller. It backs each pin with memory for 64,000 test vectors and can automatically adjust time skew to ±1.5 nsec at 25 MHz on all clocks with the device under test in place. The test-cycle rate is continuously adjustable from 200 kHz to 50 MHz with 0.25% accuracy. Among the data formats is a double-return-to-zero pattern that allows pulses to appear at twice the data rate. This format makes it possible to test at 50 MHz without pairing drivers behind one pin—the full pin count is available when testing at 50 MHz. The system can also perform dc parametric testing and measure device voltage-level sensitivity. A 32-channel configuration, $39,500. Delivery, eight weeks ARO.

Cadic Inc, 1725 SW 167th Pl, Beaverton, OR 97006. Phone (503) 645-2222.

Circle No 414

"I'M A TRUE BELIEVER IN THE POWER OF **EDN MAGAZINE.**"

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Manager, Marketing Communications
Rogers Corporation

Bob Sanders is a pro at marketing materials and components for Rogers Corporation, a worldwide leader with divisions from Connecticut to Arizona. To do the best job, he uses EDN magazine.

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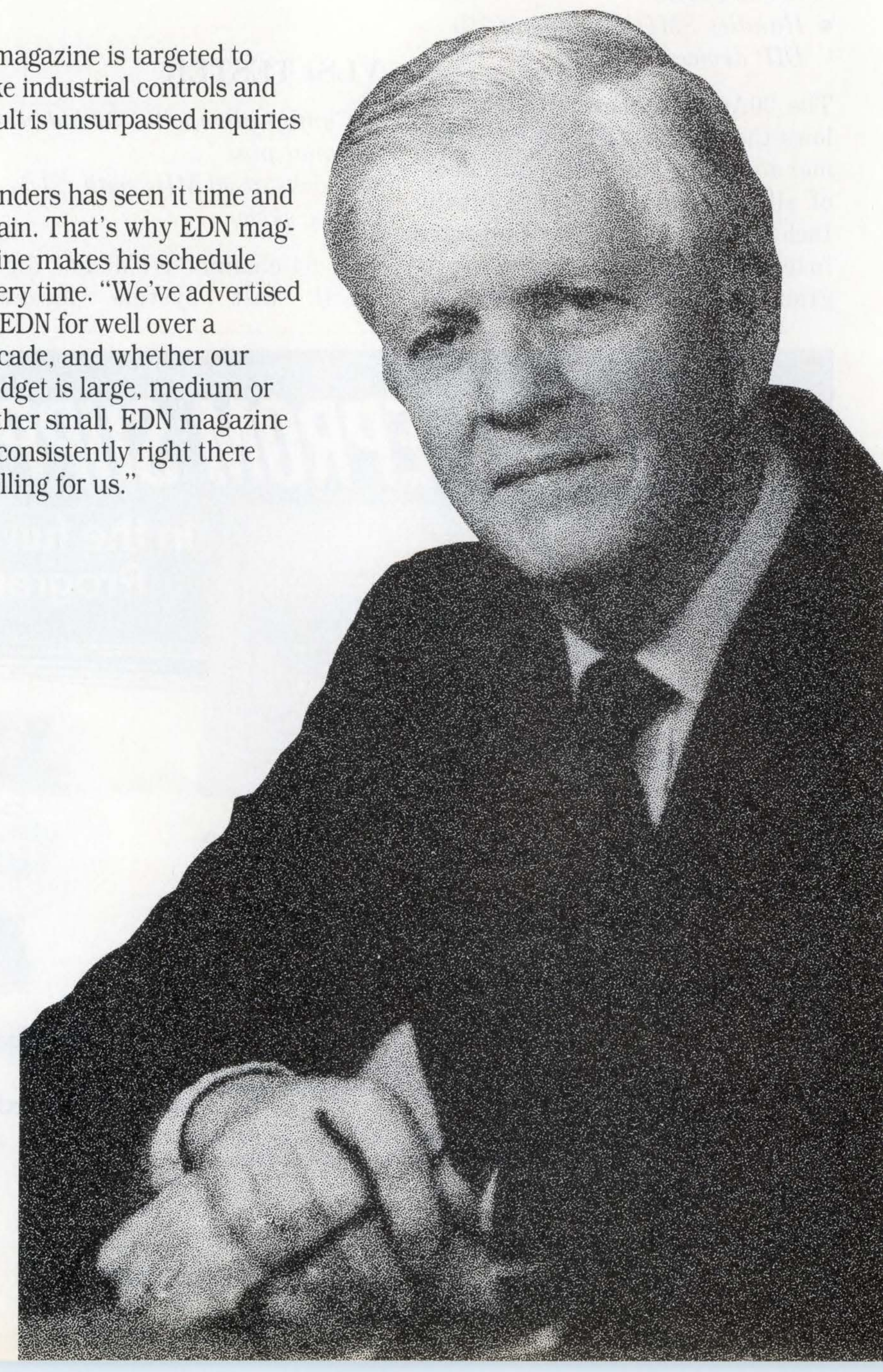

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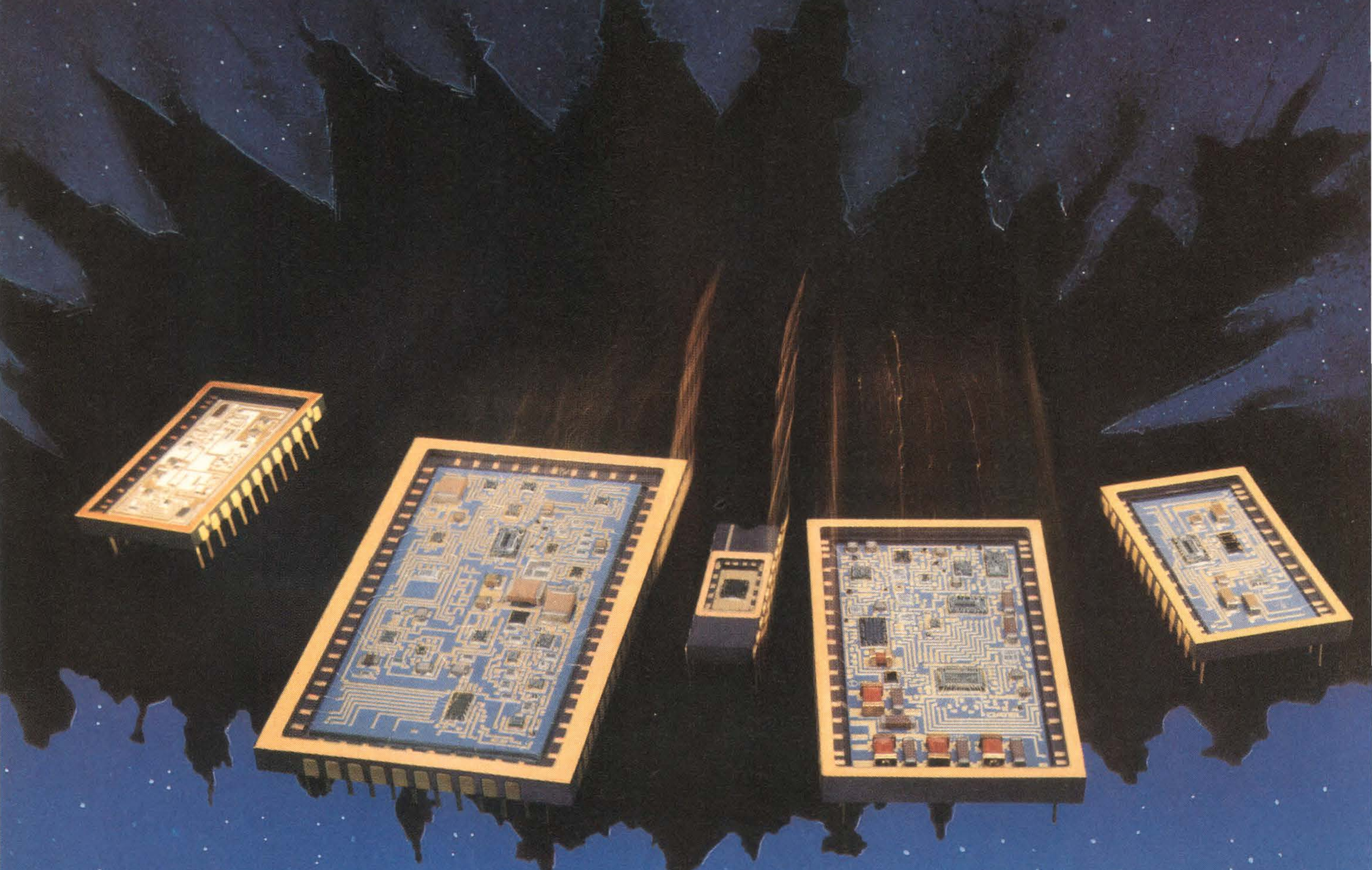

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CAE & SOFTWARE DEVELOPMENT TOOLS

DISK UTILITY

- *Provides data security by writing to two drives at once*
- *Can work with four 32M-byte partitions per drive*

The Me2 software package provides fault-tolerant operation for IBM PCs and compatibles acting as stand-alone computers or as network file servers. The software intercepts all disk read and write requests, and writes all data to two hard-disk drives simultaneously. This "shadowed-pairing" operation is transparent; the pair appears as a single drive to the computer during normal operations. If a read or write request results in an error in one drive, the software automatically switches to the data file in the second drive and notifies you of the failure. You then have the option of continuing your transaction, of using the second drive only, or of suspending operation until the malfunction in the first drive has been repaired. The software provides a 9-level log-in password system and keeps detailed records of all log-in activities. To run Me2, you need a machine equipped with DOS version 3.1 or higher. The software is compatible with both CSMA/CD (carrier sense multiple access/collision detection) and token-ring network architectures. Stand-alone version, $385; network file server version, $1285.

Atlantic Microsystems Inc, 8A Industrial Way, Salem, NH 03079. Phone (603) 898-2221.

Circle No 415

OS FOR 80386

- *Runs on 8088-, 8086-, 80286- or 80386-based machines*
- *Provides file-sharing and user-security features*

PC-MOS/386 version 1.02 is a multitasking, multiuser operating system for 8088-, 8086-, 80286-, and 80386-based computers, and it takes advantage of all the 80386's features. Those features specific to the 80386

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CPU are isolated in a single system-driver file used only when an 80386 is present in the system. Systems based on the other chips in the family can use the extended-memory facilities of the OS, provided that the systems include extended-memory hardware. The OS provides software tools that let you assign 640k bytes of RAM to each task or user, including "ill-behaved" tasks that write directly to video hardware. You can also run multiple tasks in systems that don't have extended-memory-management hardware, but you are then limited to a total of 640k bytes (minus system overhead) for all tasks. Single-user version, $195; 5-user version, $595; 25-user version, $995.

The Software Link Inc, 3577 Parkway Lane, Atlanta, GA 30092. Phone (404) 448-5465. TWX 4996147.

Circle No 416

TEST GENERATOR

- *Generates high-coverage test vectors for all types of PLDs*
- *Comes with a model library of 50 commonly used parts*

The automatic test-generator program Anvil ATG runs on IBM PC/XTs, PC/ATs, or on any compatible with 640k bytes of RAM and a hard disk with 4M bytes of available storage. The package consists of an event-driven, time-based simulator, a concurrent fault simulator, a general-purpose automatic test-vector generator, and utility programs. The software is menu-driven, but you can bypass the menus if you want a series of jobs to run in batch mode without operator attention. According to the vendor, the program typically achieves 90 to 100% fault detection, even on highly sequential designs, such as state machines. The faults considered include stuck-at-0 and stuck-at-1 logic elements and incomplete or improperly blown fuses. So as not to obscure true-fault coverage, the program removes from consideration undetectable faults that derive from redundancy or unused circuitry. $4950.

Anvil Software, 369 Massachusetts Ave, Suite 192, Arlington, MA 02174. Phone (617) 641-3861.

Circle No 417

GRAPHICS CONVERTER

- *Lets you add color to Macintosh graphics*
- *Converts Macintosh graphics to DEC's Regis or Sixel formats*

Reggie is a software package for the Macintosh that converts MacDraw, MacPaint, and Clipboard images to DEC's Regis (object-oriented) or Sixel (bit-mapped) formats so that the converted images can be imported into applications that run on a DEC host. In addition, the program allows you to add color to each object of a MacDraw document. You can also use the program to convert Macintosh CAE-program images into a form suitable for processing on a DEC host workstation. $99.

White Pine Software Inc, Box 1108, Amherst, NH 03031. Phone (603) 886-9050. TWX 650-288-7627.

Circle No 418

MODEM SOFTWARE

- *Works with Hayes AT-compatible modems*
- *Provides built-in automatic dialing directory*

Anchor-Talk is a simple telecommunications program that you can use on an IBM PC or compatible equipped with the vendor's modems; you can also use the program with other vendors' internal or external modems, provided the modems employ the Hayes AT command set. The program allows you to create a built-in dialing directory; when you select an item, the modem dials the number automatically. You can use the Xmodem or Xmodem/CRC protocols to transfer files between your machine and any host

that can also use these protocols. If you communicate with a public-service host that doesn't use Xmodem, you can employ the XON/XOFF protocol for file transfer in either direction. $29.95.

Anchor Automation, 20675 Bahama St, Chatsworth, CA 91311. Phone (818) 998-6100.

Circle No 419

NETWORKING OS

- *Conforms to System V Interface Definition*
- *Operates with an Ethernet TCP/IP network*

Venix 2.3 is a real-time version of Unix that runs on the HP Vectra Plus, the Compaq Deskpro 386, and IBM PC/ATs and compatibles. The enhanced OS can now use an 80386-based machine's protected mode. It also works with machines that are connected to an Ethernet network and that use TCP/IP (Transmission Control Protocol/Internet Protocol). The OS conforms to the AT&T System V Interface Definition and has passed the System V Verification Suite instituted by AT&T to test for compliance with System V standards. The system's features include support for the IBM Enhanced Graphics Adapter board and for AT&T 80286 executable binary programs in common object file format; thus, programs written for AT&T's 6300 Plus μC will run under Venix 2.3 without recompilation. Improved memory management, a more efficiently coded kernel, an extended-buffer cache, and a 1024-byte block file system combine to provide quick responses when you run demanding multiuser, multitasking application programs. The software includes a large-memory-model C compiler. A 2-user system, $600; after December 31, 1987, $990.

VenturCom Inc, 215 First St, Cambridge, MA 02142. Phone (617) 661-1230.

Circle No 420

TEXT FORMATTER

- *Operates with the HP LaserJet or compatible printers*
- *Comes in CP/M and MS-DOS versions*

MagicFont is an addition to the MagicSeries text-formatting tools, which allow you to create logos and symbols in many sizes or styles for use with a standard CP/M or MS-DOS word processor and an HP LaserJet or compatible printer. MagicPrint, the series' basic formatting tool, provides true proportional spacing, automatic footnoting, multiple-column printing, automatic chapter/section numbering, widow/orphan control, and table-of-contents generation on a variety of printers. Adding MagicFont lets you employ all laser-printer functions; you can use your printer's standard fonts or download disk-resident fonts and create headings and drop letters of 72 points or more. You can mix different type sizes, styles, and symbols within a line, or even within a word, without disrupting the margins and justification. The other tools in the series are MagicBind, which includes MagicPrint and provides mail-merge facilities, and MagicIndex, which includes MagicBind and provides automatic multitier document indexing facilities. MagicFont, $59; MagicPrint, $99; MagicBind, $149; MagicIndex, $199.

Computer EdiType Systems, 509 Cathedral Pkwy, Suite 10A, New York, NY 10025. Phone (212) 222-8148.

Circle No 421

MULTITASKING WITH C

- *Library provides basic functions for multitasking*
- *Lets you handle multiple users or devices as independent tasks*

Multi-C is a library of C-language functions that you can link to a program to convert the program into a number of time-independent tasks.

The library contains task-scheduling, time-scheduling, and intertask-communication functions. When you create a task, you call a function that creates both a structure that controls execution of the task and a separate stack area that lets the task behave as an independent program. When a task must wait for an event, other functions save its current state on the stack and restore the state when the scheduler returns control to the task. The scheduling functions are nonpreemptive and give control to the "ready" task with the highest priority; if several ready tasks have the same priority, they are scheduled on a round-robin basis. Companion products include Multi-Comm, a communications library; Multi-Windows, a screen-management library; and Multi-Forms, a data-entry and -display library. All run on an IBM PC or compatible, and various versions work with Microsoft, Datalight, Lattice, and Turbo-C compilers. Multi-C, Multi-Comm, Multi-Forms, $149 each; Multi-Windows, $295.

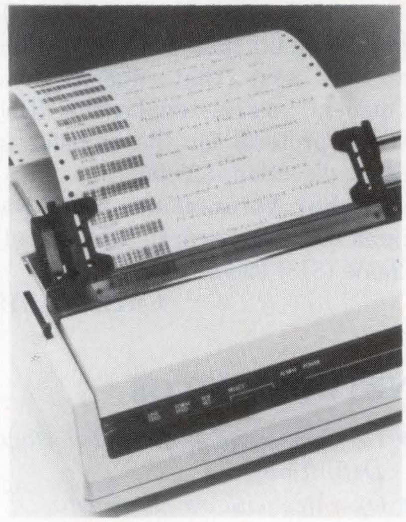
Cytek Inc, 805 Turnpike St, North Andover, MA 01845. Phone (617) 687-8086.

Circle No 422

BAR-CODE SOFTWARE

- *Can use a dot-matrix or laser printer to print bar codes*
- *Obtains data from a dBASE III Plus file*

dBarcode runs on an IBM PC or compatible and prints Code 3 of 9, Code 2 of 5, or UPC Version A bar codes that correspond to part numbers or other numerical information that you've stored in a dBASE database. You can adjust the bar and space widths to suit various bar-code readers, and you can also adjust the bar-code height and vertical spacing. You can print multiple columns of bar codes (on labels, for example), or you can print descriptive text alongside each bar code. The package includes Barprint, a



utility that allows you to set code height and spacing and to then enter data from the keyboard. You can configure the program to use either an HP LaserJet printer or any dot-matrix printer that is compatible with the IBM Graphics Printer. $99.

Timekeeping Systems Inc, 12434 Cedar Rd, Cleveland, OH 44106. Phone (216) 229-2575.

Circle No 423

FILTER-DESIGN TOOLS

- *Help you design high-frequency distributed lowpass filters*
- *Handle coaxial, stripline, and microstrip filters*

Three new programs in the vendor's MSAfilter product group allow you to design distributed lowpass filters in coaxial form (CXLPF), stripline form (SLLPF), or microstrip form (MSLPF). Each program performs a design synthesis of the electrical circuit, synthesis of the distributed circuit, and frequency analysis of either the standard or the dual filter design. The programs are interactive, and you can change the topology and physical dimensions of the filter and quickly determine the effect of such changes on the filter's response. You can also perform tolerance studies on the design to determine the critical parameters. The programs run on IBM PCs or compatibles with at least 256k bytes of RAM and one double-sided floppy-disk drive. Each program comes on a 5¼-in. floppy disk and is accompanied by a backup copy; versions for hard-disk installation are available. $495 each.

Microwave Software Applications Inc, Box 1736, Norcross, GA 30091. Phone (404) 441-9193.

Circle No 424

PROCESS ANALYZER

- *Lets you analyze and fine-tune process-control loops*
- *Provides time-response, frequency-response, and Bode plots*

The ProcessPlus process-control analysis and tuning software package runs on an IBM PC or compatible with 512k bytes of RAM, at least one floppy-disk drive, and DOS 2.1 or higher. A math coprocessor is recommended but not required. The program identifies your process from test data that you enter, and it lets you select a proportional-integral-differential (PID) controller from three categories (interacting, noninteracting, or parallel) and 10 industrial PID algorithms. The program then generates graphs of step or ramped setpoint changes, or either of two types of load-disturbance plots, or any of three different types of frequency-response plots. The program offers extensive on-line help screens and uses a simulation model that lets you simulate any combination of dead time: as many as seven lags in series, integration, lead action, inverse response, and underdamped or overdamped processes. You can see the results of changing loop parameters and can compare the operation of different manufacturers' controllers. $750; outside the US and Canada, $825.

Gerry Engineering Software, 13310 W Red Coat Dr, Lockport, IL 60441. Phone (312) 257-5950.

Circle No 425

NETWORK ANALYZER

- *Monitors Ethernet or ProNet-10 traffic*
- *Lets you screen out all but the packets of interest to you*

The LANWatch software network analyzer monitors traffic on an Ethernet network, captures packets as they pass, and stores them for later examination. The software runs on IBM PCs and compatibles, and it is compatible with various Ethernet boards by Excelan, Micom, and 3Com. In display mode, the program captures successive packets passing over the Ethernet, stores them in a buffer, and displays one line of information about each packet on the screen. The buffer holds as many as 254 packets. When the buffer fills up, the program discards the oldest packets to make room for new ones; however, by setting a software switch, you can make the program store all the packets to a disk file and thus allow for histories of more than 254 packets. The display mode provides filters that allow you to select for display only the packets of interest to you. If you want filter specifications not provided by the filters supplied with the program, you can write a C function, compile it with Microsoft C, and link it to LANWatch; the documentation includes examples of how to write filters. The examine mode lets you browse through packets stored in the buffer and examine the contents of individual packets in detail. $1200.

FTP Software Inc, Box 150, Kendall Sq Stn, Boston, MA 02142. Phone (617) 868-4878.

Circle No 426

OS FOR HD64180

- *Provides a large operating space for CP/M-compatible programs*
- *Operates with floppy-, hard-, or RAM-disk storage*

The Hyperspace Z-System operating system for computers based on the Hitachi HD64180 or Zilog Z280 μPs lets you run all application programs written for CP/M 2.2. The software consists of ZRDOS 2.0 (a replacement for the CP/M BDOS); a sample BIOS for the HD64180; and ZCPR 3.3, a package that provides extended command-processing features including conditional branching, a batch processor, a shell subsystem, multilevel directories, named directories, a path-searching feature, and extensive on-line help. A file-maintenance utility lets you use a single command to tag multiple files for viewing, copying, erasing, and other operations. The Unerase utility permits you to reclaim erased files. You can use the menu subsystem to create and run menus that automate many housekeeping functions and isolate nontechnical users from the OS, but yet grant these users full access to the application programs and OS functions that they need. Because the HD64180 and Z280 CPUs both have a large memory-address space, you can place many of the ZRDOS modules outside the normal 64k-byte CP/M address space. This feature enlarges the memory space avail-

VF Technology... The Bright Decision

Futaba, a world leading manufacturer of vacuum fluorescent displays, offers a wide assortment of *display tubes* in many sizes and formats. Also, Futaba offers *display modules* with all the electronics required to refresh the display and easily interface with the host system.

GRAPHIC DISPLAY

Both front glass phosphor, which provides maximum viewing angle and uniform surface appearance, and conventional back glass phosphor, with optimum brightness and software dimming capabilities, are available. All Futaba graphics modules offer complete drive electronics, bit mapped control with a DC/DC converter. All active components are surface mounted onto a single board.

DOT MATRIX MODULES

Utilizing Futaba's dot matrix displays, a completely intelligent line of "dot modules" is available. Each includes all drive, power supply and microprocessor components surface mounted onto a single board. Surface mounted technology results in higher reliability and allows for a smaller overall package and lower cost. All dot modules require only a 5V DC power source and can accept parallel or 8 possible serial baud rates.

GRAPHIC DISPLAYS/MODULES

Futaba Display	Futaba Module	Pixels (Row X Char.)	Brightness (FT-L)	Module Dimensions (in.)
GP1005B	GP1005B03	128X64	400	7.28X3.35X1.77
GP1006B	GP1006B04	256X64	200	9.84X3.35X1.77
GP1009B	GP1009B03	240X64	200	6.2X2.76X1.57
GP1010B	GP1010B01	176X16	200	7.32X2.16X1.70
GP1002C	GP1002C02	320X240	100*	7.10X6.30X1.60
GP1004B	GP1004B03	640X400	30	9.65X7.28X1.85

*Different Versions Available

DOT MATRIX DISPLAYS/MODULES

Futaba Display	Futaba Module	Char. X Row	Dot Format	Char. Ht. (in.)	Module Dimensions (in.)
20SD01Z	M20SD01	20X1	5X7	0.200	6.3X1.97X.75
20SD42Z	M20SD42	20X1	5X12	0.344	7.1X2.16X.88
40SD02Z	M40SD02	40X1	5X7	0.200	9.45X2.16X.88
40SD42Z	M40SD42	40X1	5X12	0.344	9.45X2.16X.88
202SD03Z	M202SD03	20X2	5X7	0.200	6.7X2.56X.90
402SD04Z	M402SD04	40X2	5X7	0.200	10.43X2.56X.90

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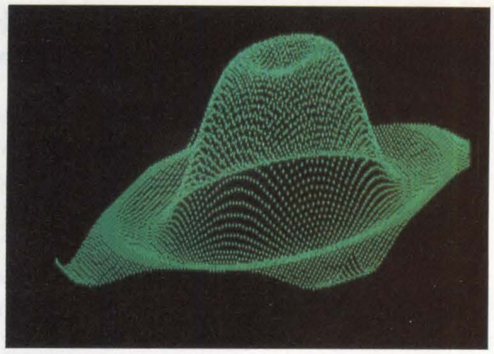

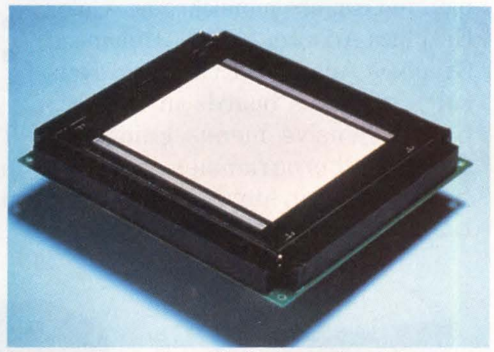

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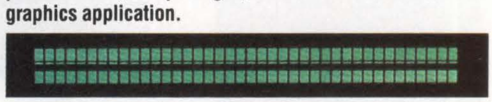
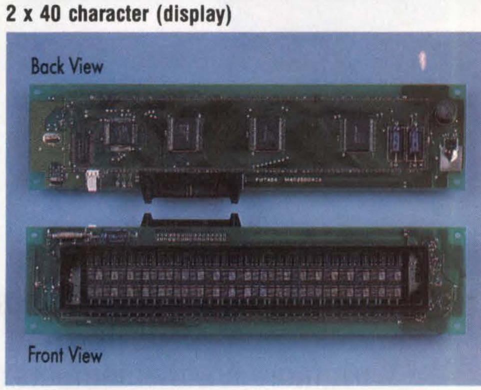


2 x 40 character (display)



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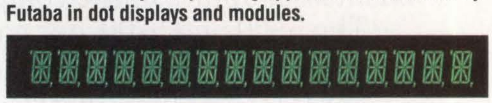

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FTG Data Systems, Box 615,

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Process Software Corp, Box 746, Amherst, MA 01004. Phone (413) 549-6994. TLX 517891.

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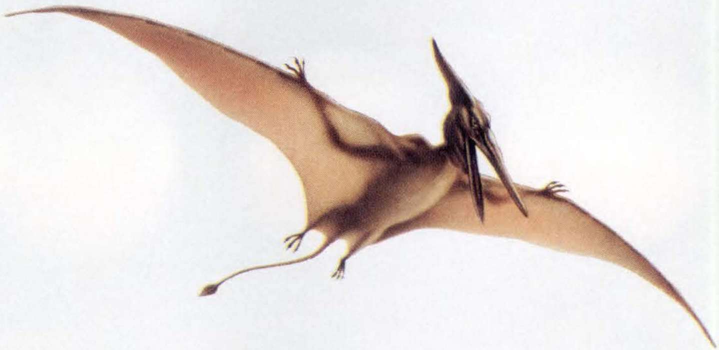

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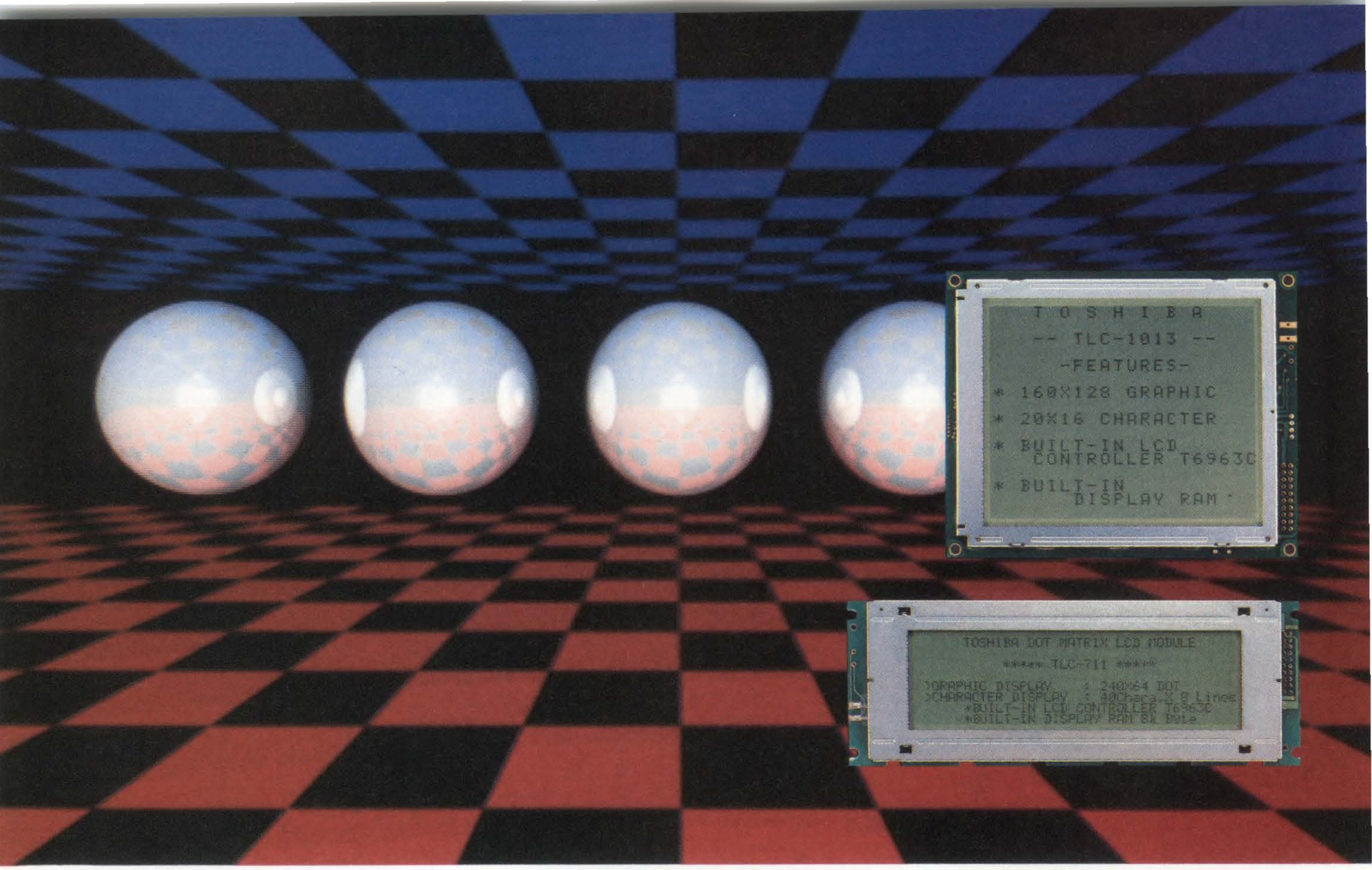

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TLC-731	16 × 4	87.0 × 60.0 × 12.0
TLC-501	20 × 2	116.0 × 37.0 × 12.5
TLC-721	20 × 4	98.0 × 60.0 × 12.0
TLC-691	24 × 1	126.0 × 36.0 × 12.0
TLC-771	24 × 2	118.0 × 36.0 × 12.0
TLC-601	40 × 1	182.0 × 33.5 × 13.0
TLC-591	40 × 2	182.0 × 33.5 × 13.0
TLC-1001	40 × 4	221.0 × 76.0 × 12.5

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TLC-682	160 × 64	125.0 × 50.0 × 18.0	T6963C
TLC-711A	240 × 64	180.0 × 65.0 × 12.0	T6963C
TLC-1013	160 × 128	129.0 × 104.5 × 14.0	T6963C
TLC-1091	240 × 128	241.0 × 125.3 × 12.0	T6963C
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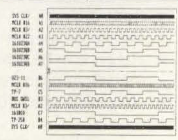

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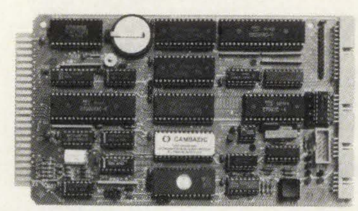

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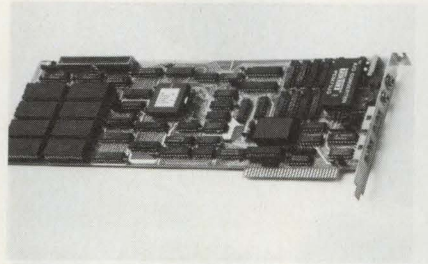

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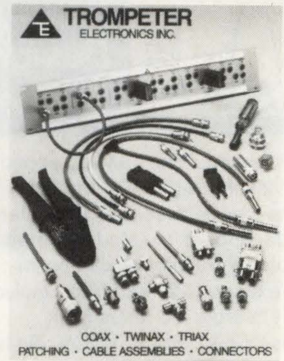

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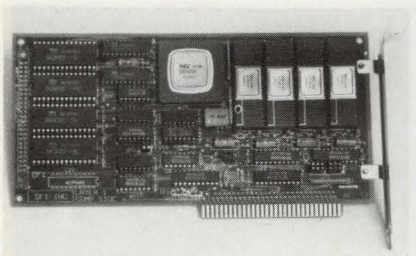

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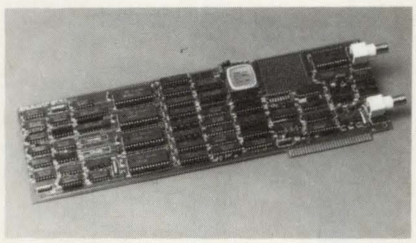

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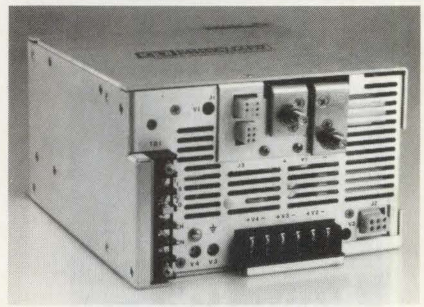

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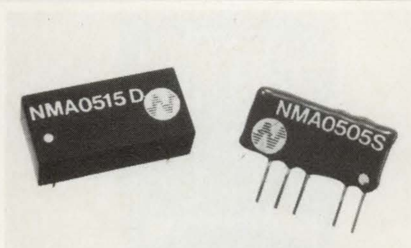

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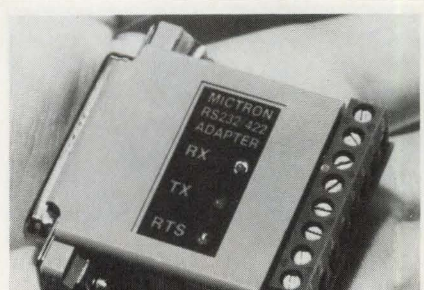

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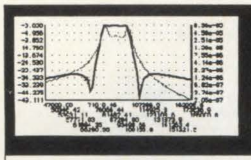

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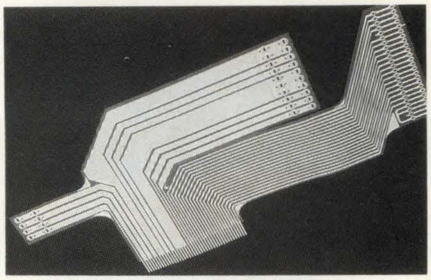

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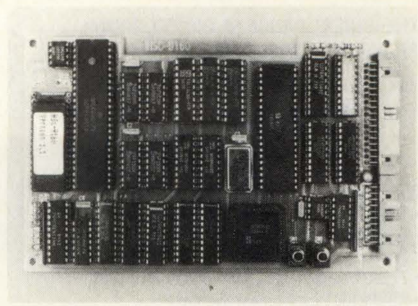

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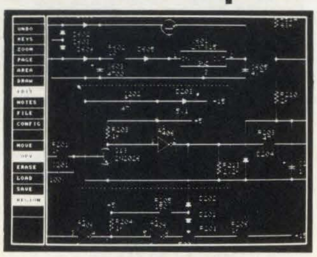

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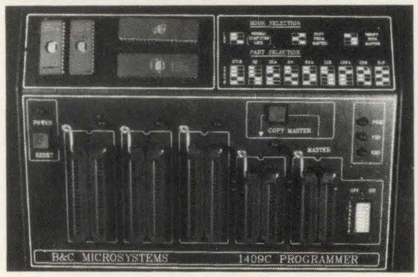

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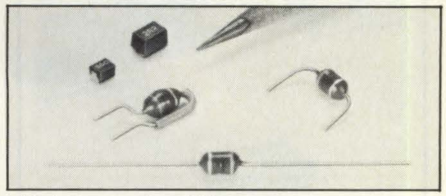

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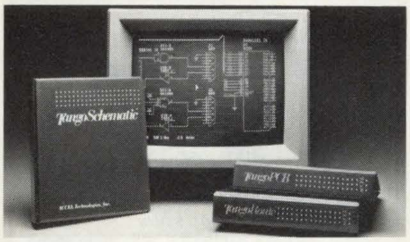

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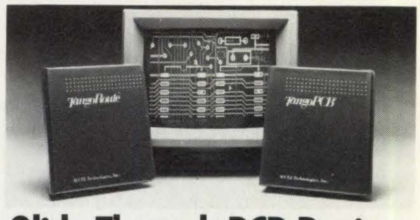

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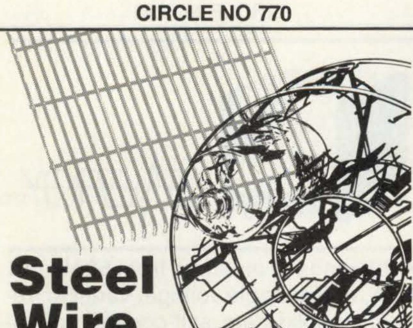

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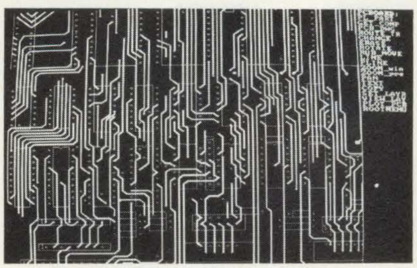

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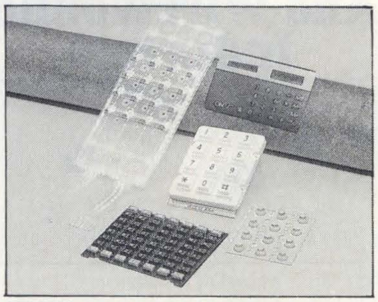

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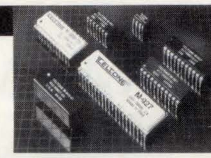

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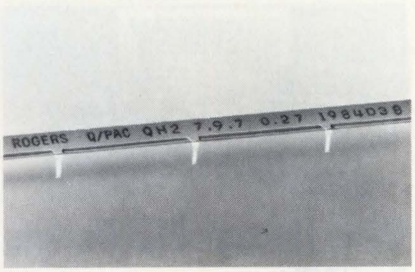

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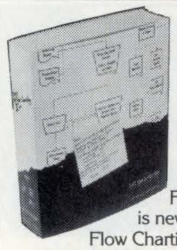

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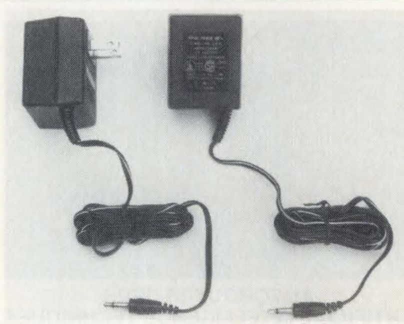

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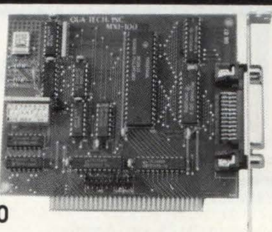

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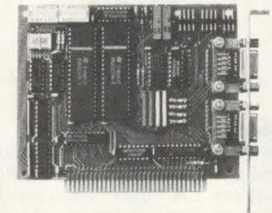

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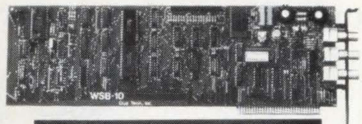

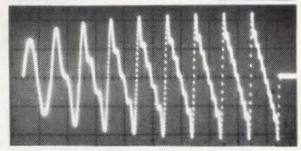

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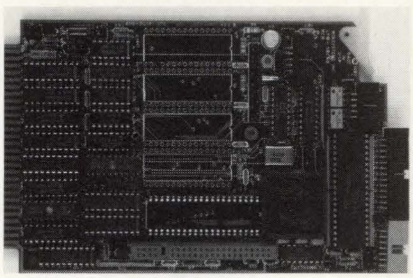

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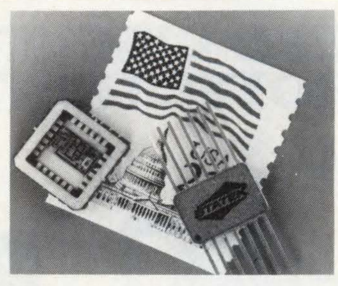

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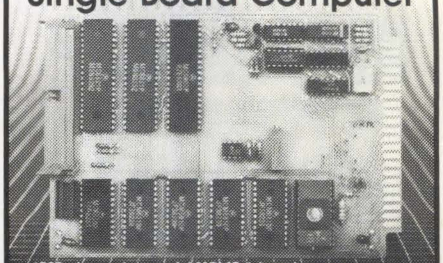

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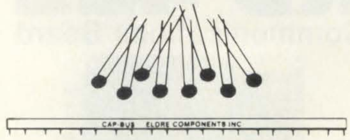

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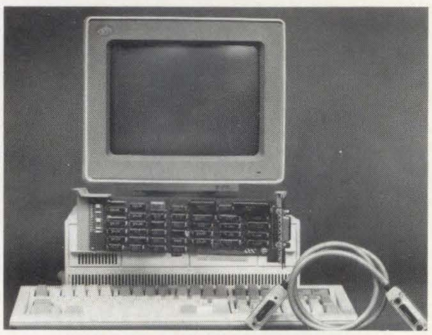

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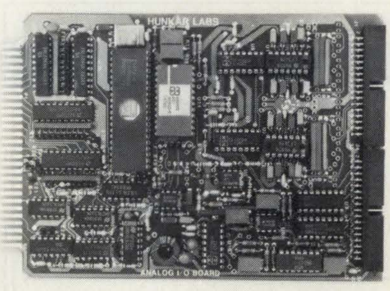

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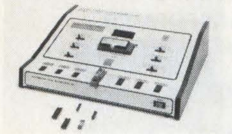

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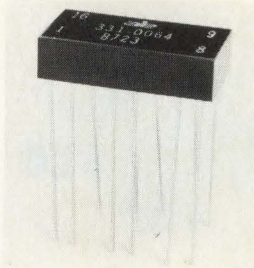

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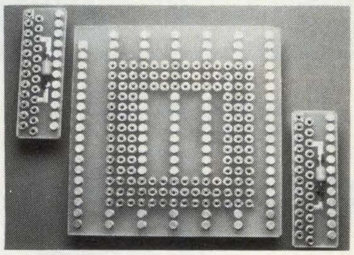

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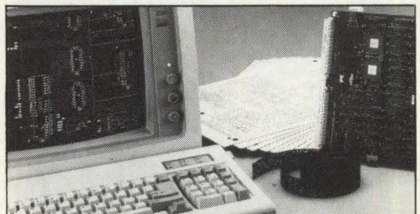

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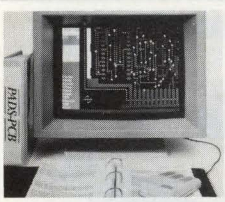

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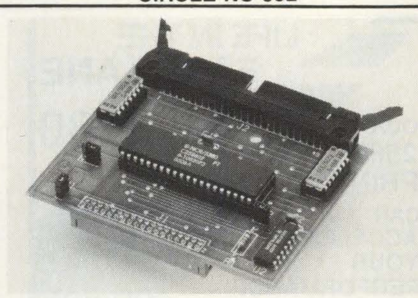

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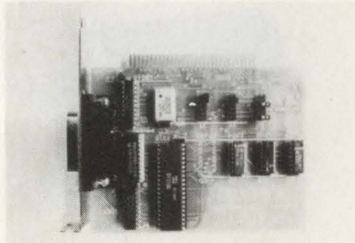

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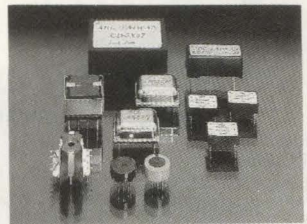

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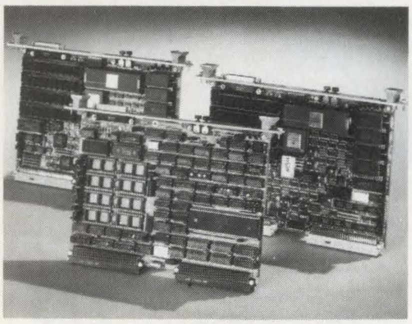

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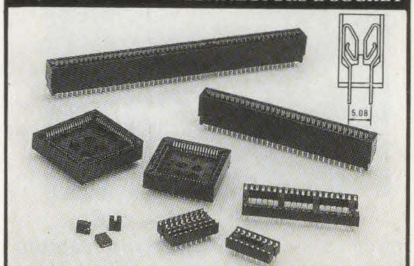

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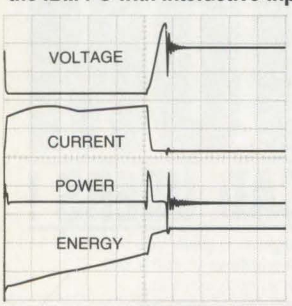

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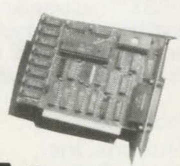

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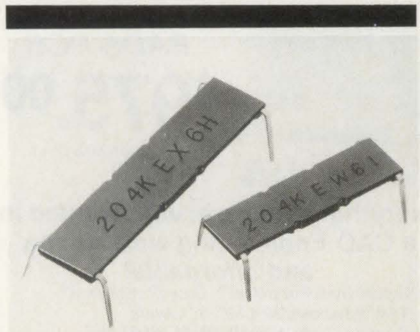

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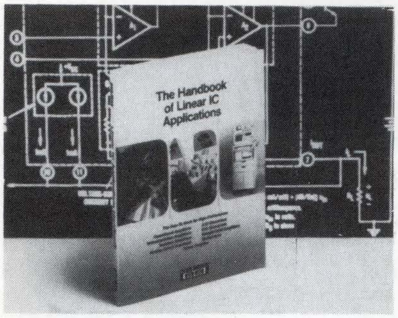

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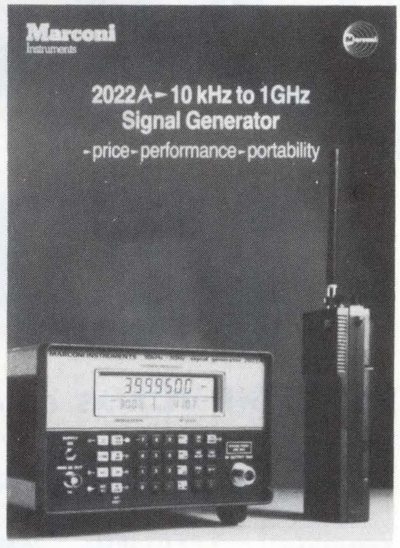
Signal generator specs

This 8-pg, 4-color brochure outlines the features of the Model 2022A signal generator. It examines the product's specification improvements, which include lower noise; an FM noise of only 7 Hz that improves S/N ratio; lower carrier distortion; dB improvement for critical measurements on wideband devices; and lower FM distortion. The pamphlet



lists the 2022A's operational features including nonvolatile memory, computer control, RF output, simple calibration, and automatic monitoring.

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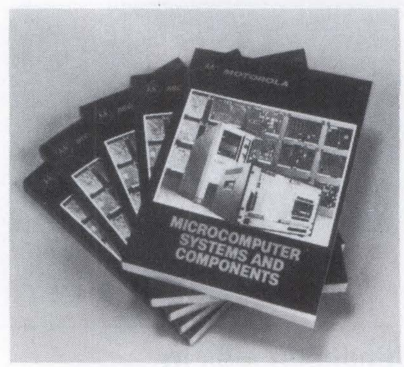
LITERATURE



Data book describes μC systems

The 628-pg, second-edition *Microcomputer Systems and Components* data book contains technical descriptions of more than 345 products. It's categorized by systems, boards, software, and documentation. Each section has its own table of contents and index. A 44-pg bus-specification summary explains architectures of the VME Bus, VSB bus, I/O channel bus, as well as other specifications of the company's product line. Request Literature DLI27/D. $4.75.

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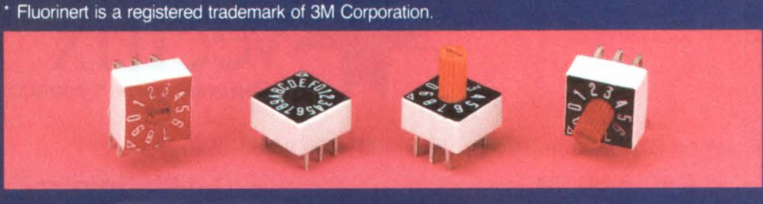

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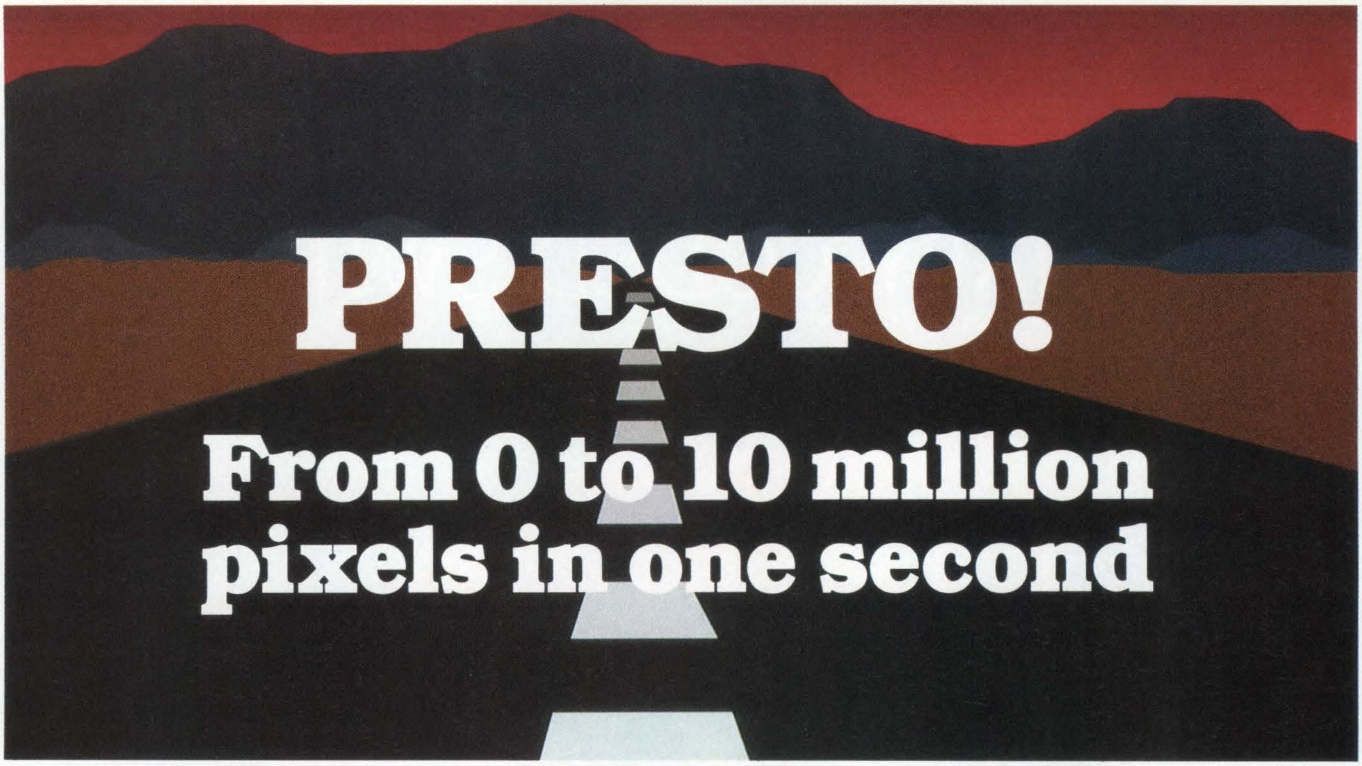

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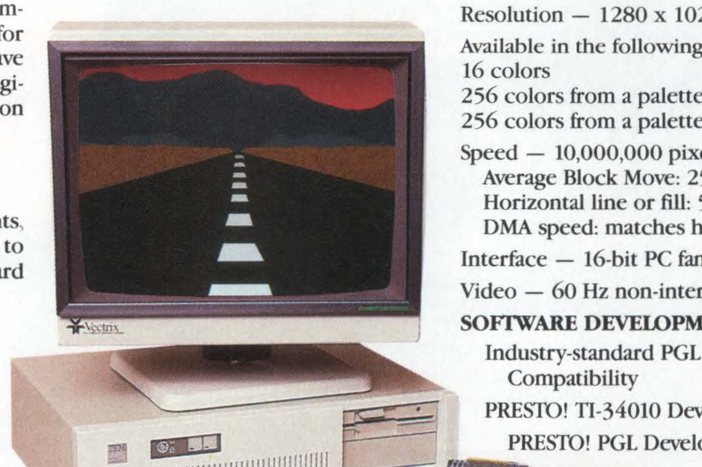

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16 colors
256 colors from a palette of 4096
256 colors from a palette of 16.8 million

Speed — 10,000,000 pixels per second
Average Block Move: 25 million bits/second
Horizontal line or fill: 50 million bits/second
DMA speed: matches host bus speed

Interface — 16-bit PC family

Video — 60 Hz non-interlaced

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PRESTO! PGL Developer Toolkit

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CIRCLE NO 304

concepts and includes a recommended panel layout for the maximum use of raw materials.

Dynacircuits Inc, 11230 Addison St, Franklin Park, IL 60131.

Circle No 435

Test and measurement instruments categorized

This 16-pg catalog on test and measurement instrumentation outlines performance features, applications, and specifications for 22 instruments. The products featured include digital multimeters, data-acquisition and logging instruments, dynamic analysis and vibration equipment, and communications test sets.

Solartron Instruments, 2 Westchester Plaza, Elmsford, NY 10523.

Circle No 436

Bus products described

Everything for the EXORbus is a 6-pg product guide that provides information on a family of EXORbus-compatible boards, modules, and accessories. It features a product overview on 6800/6809 μP modules that are suitable for use in systems dedicated to production automation, process control, data acquisition, and materials testing. Other sections deal with processor modules, memory modules, I/O modules, microcomputer systems,

enclosures, and packaging and accessories.

Creative Micro Systems, 3822 Cerritos Ave, Los Alamitos, CA 90720.

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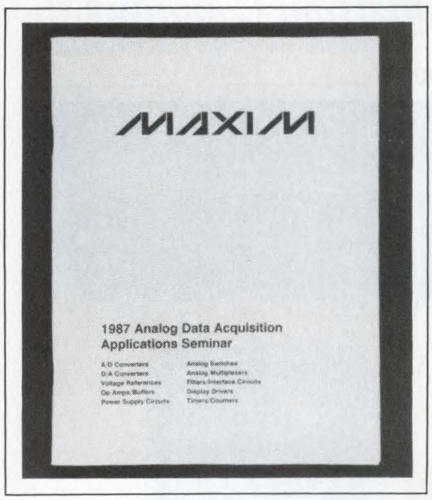

Catalog lists data-acquisition devices

The *1987 Analog Data Acquisition Applications Seminar* covers a wide range of products. They include CMOS data converters, video amplifiers, multiplexers, low-power dc/dc converters, switched capacitor filters, op amps, and μP support devices. This handbook also discusses product reliability and surface-mount packaging.

Maxim Integrated Products, Customer Service Dept, 510 N Pastoria Ave, Sunnyvale, CA 94086.

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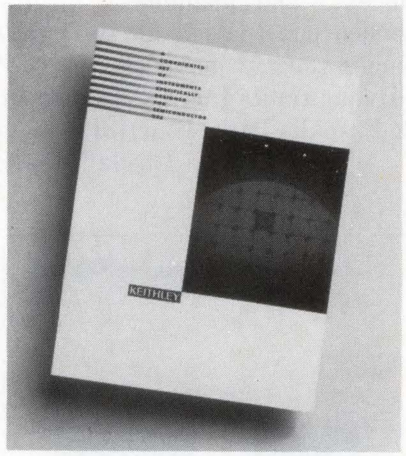

Tutorial pamphlet for semiconductor testing

The 4-color, 12-pg brochure, *A Coordinated Set of Instruments Specifically Designed for Semiconductor Use,* describes how to use instruments to make semiconductor measurements. The publication is a combination of tutorial and product descriptions. It explains techniques such as low-level measurements, capacitance-voltage tests, resistance and electromigration studies, and Hall-effect measurements. It also explains how to use specialized instruments, electrometers, switch systems, picoammeters, and capacitance-voltage instruments.

Keithley Instruments Inc, 28775 Aurora Rd, Solon, OH 44139.

Circle No 439

Instrument catalog

This 32-pg catalog covers the company's line of products for industrial and laboratory test and measurement applications. Products highlighted include handheld thermometers, temperature controls, panel meters, calibration equipment, temperature loggers, IR thermometers, thermocouples, RTDs, and handheld probes. Also included are humidity instruments, anemometers, digital voltmeters, temperature baths, pH meters, oxygen analyzers, and tachometers. Also listed are multifunction instruments that can measure several different parameters by using plug-in modules and sensors; the listing describes each product, giving its operating specifications and price.

Owen Instruments Inc, Box 2193, Provo, UT 84603.

Circle No 440

Catalog of VME Bus products

This 4-color, 16-pg catalog highlights the manufacturer's VME Bus boards, systems, and software. The short-form catalog covers systems and packaging, multiprocessing ready development/target systems, CPUs, multiprocessing engines, system resources, single-board computers, memory, analog I/O and DSP devices, displays, special-function products, and packaging and peripherals.

Ironics Inc, 798 Cascadilla St, Ithaca, NY 14850.

Circle No 441

Data sheet explains DSP software

This 4-pg publication presents the manufacturer's DSPlay software package that allows you to use an IBM PC, PC/XT, PC/AT, or a compatible computer as a DSP workstation. It discusses the program's use of functional block diagrams as its language for program development and documentation. It also describes the library of block functions, such as correlation, signal source, filter, window, and FFT. Also included are performance specifications, hardware and software requirements, and options.

Burr-Brown, Box 11400, Tucson, AZ 85734.

Circle No 442

App note deals with CMOS analog switches

The 4-pg application note, *ADG201A/202A and ADG221/222 Performance with Reduced Power Supplies*, discusses applications for four monolithic CMOS analog switches, including their use in 12V disk drives and ±12V PC applications. The note also explains the variation in switch characteristics over the 10 to 15V single- or dual-power supply range; it contains 17 graphs that show all relevant performance curves. The note discusses leakage currents, digital input trigger levels, and switch timing. Other sections include dynamic characteristics, charge injection, and power-supply current.

Analog Devices, Literature Ctr, 70 Shawmut Rd, Canton, MA 02021.

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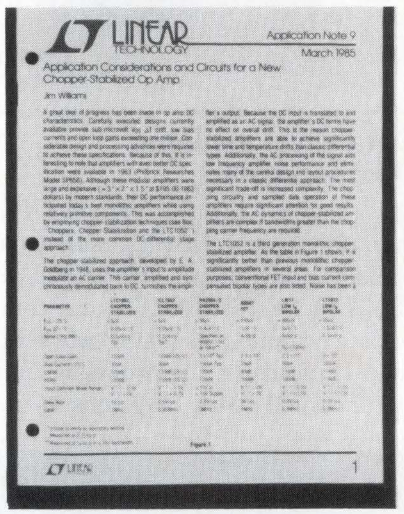
LINEAR TECHNOLOGY — Application Note 9 — March 1985

Application Considerations and Circuits for a New Chopper-Stabilized Op Amp

Jim Williams

App note on op amp

The 20-pg application note, *Application Considerations and Circuits for a New Chopper-Stabilized Op Amp* (AN9), describes the chopper-stabilized approach, which uses the amplifier's input to amplitude-modulate an ac carrier. The note provides a schematic of a tested circuit for a dc- to 1-Hz noise test circuit, as well as schematics for other tested circuits.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

Circle No 444

Connector booklet

This 8-pg short-form catalog provides descriptions and specifications for the company's varied line of connectors. The products covered include rectangular, circular, and flat-ribbon-cable connectors; circuit-board and edge-card connectors; modular interconnections; IC and zero-insertion-force sockets; and single-mode and multimode fiber-optic connectors.

JAE Electronics Inc, 1901 E Carnegie Ave, Suite A, Santa Ana, CA 92705.

Circle No 445

Booklet summarizes features of spectrum analyzer

The 16-pg, 4-color brochure, *400-MHz Spectrum Analyzer 2382*, illustrates Model 2382's RF design and details specifications. A section on measurement problems shows you how to speed up measurements at a single frequency; how to display demodulated FM; and how to get permanent records of tests.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401.

Circle No 446

Brochure presents IR pyroelectric detectors

This 6-pg data note, *Introduction to Infrared Pyroelectric Detectors*, describes the basics of lithium tantalate pyroelectric detectors. Three introductory topics are entitled "When to Use Infrared," "Beyond Photodiodes," and "Pyroelectrics are Practical." Other topics discussed include electrical considerations and laser applications.

Eltec Instruments Inc, Box 9610, Daytona Beach, FL 32020.

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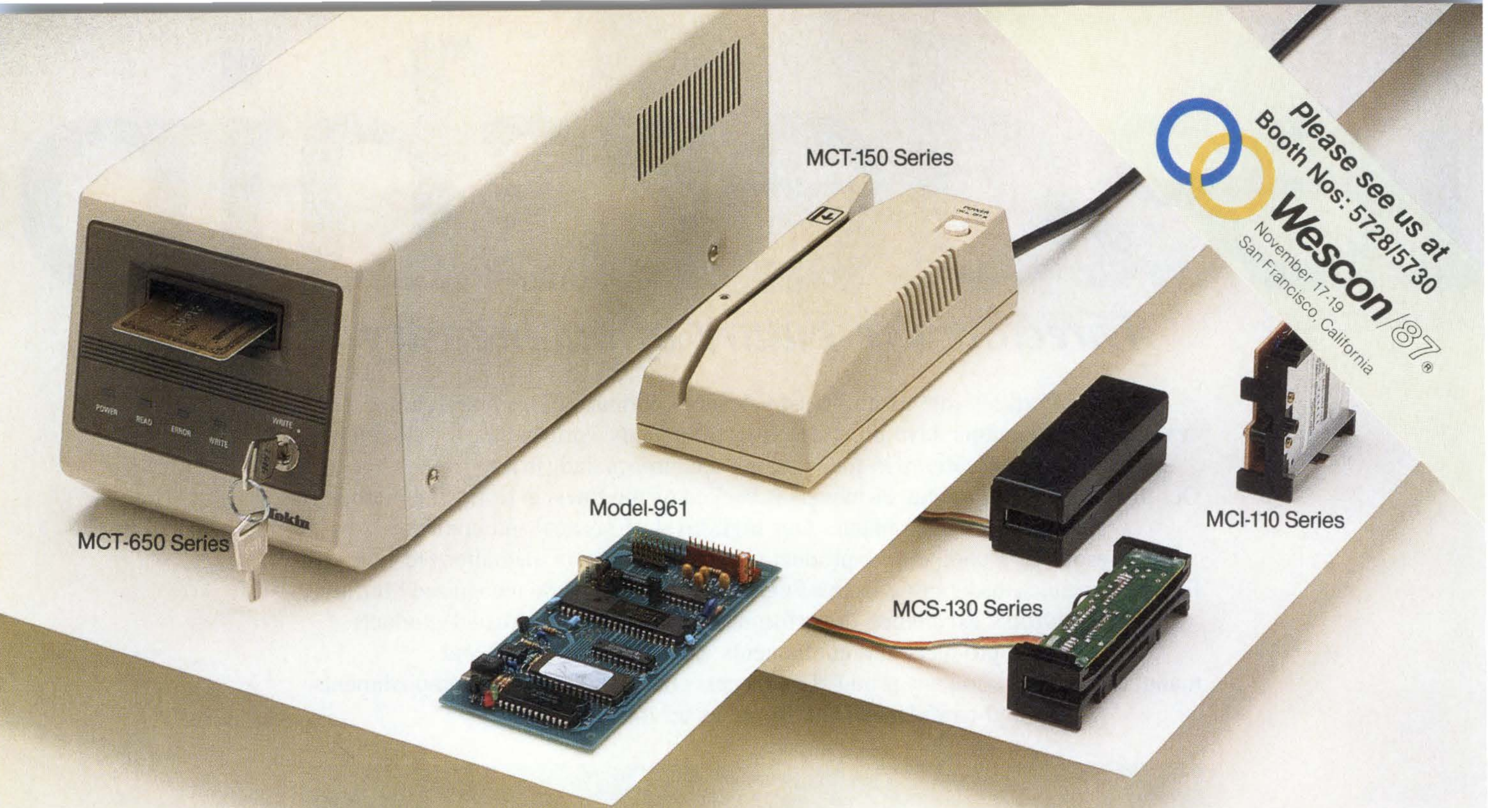

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	MCT-650 Series	MCT-150 Series	Model-961 Interface Module
Communication standards	Standard EIA, RS232C		
Communication mode	Start-stop synchronization, full duplex (half duplex)	Start-stop synchronization, full duplex	Start-stop synchronization, full duplex (half duplex)
Transmission speed (baud)	1,200/2,400/4,800/9,600	1,200	600/1,200/2,400/4,800/9,600/19,200/38,400
Communication format	Start bit 1 Data bit 8 Parity (even) 1 Stop bit 1		Start bit 1 Data bit 7 Parity (odd) 1 Stop bit 1 (User selectable)
Card driving system	Motorized	Manual	—
Performance	Read/write	Read only	
Power supply	117V AC		+5V DC, +8~12V DC

Applicable Magnetic Card

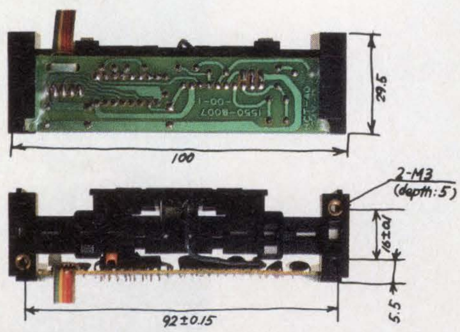
Units	Card Standard	Dimensions (mm)
MCI-111	ISO, track 2	24×61×65
MCI-112	ISO, track 1	
MCI-113	ISO, track 3	

Units	Card Standard	Dimensions (mm)
MCS-131(E)	ISO, track 2	27×29.5×100 (32.5×32×100)
MCS-132(E)	ISO, track 1	
MCS-133(E)	ISO, track 3	
MCS-135(E)	ISO, track 1 and 2	
MCS-136(E)	ISO, track 1 and 2	

*(E): With cover

Shapes and Dimensions

MCS-135, 136



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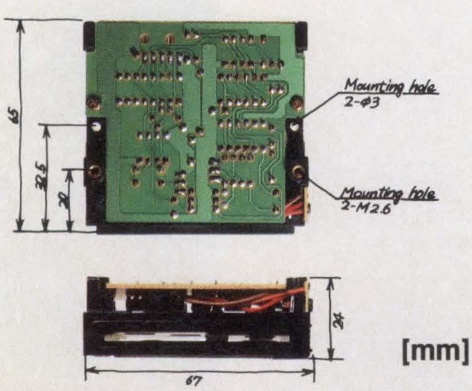

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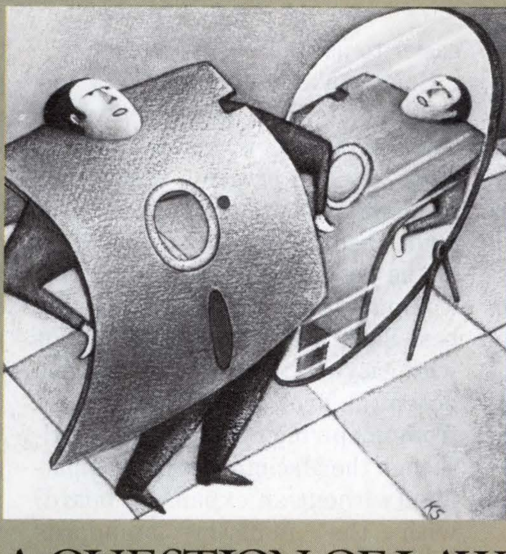
Kris Stevenson

A QUESTION OF LAW

Software developers tussle over the "look and feel" issue

Richard Beutel, *Washington, DC*

It's said that imitation is the sincerest form of flattery. If recent events in the software industry are any indication, however, imitation often results in a lawsuit.

Several lawsuits in the news over the past year indicate a new legal basis for software developers' attacks on so-called clone software—software that imitates or adopts the user interface of another software product. Formerly, only the algorithms of software programs were considered subject to copyright, the law's traditional protector of creative works. Now some software makers are saying that copyright should also extend to a program's user interface. According to these companies, the user interface gives a program a distinctive "look and feel" and to copy that is to copy an essential part of the program.

The idea that a program's "look and feel" are copyrightable and subject to court protection has startled the computer-law community. In copyright suits that involved the screen displays of video games, the courts had ruled that a screen had to show originality and artistic expression in order to be protected. Data elements such as menu options weren't considered creative in nature and were therefore denied the protection of copyright. Most computer-law specialists expected this reasoning to apply to software programs as well.

The earliest hint that it might not apply came in the fall of 1986, when a court ruled that Unison World had infringed on the menu-screen copyright of Broderbund Software's Print Shop package. This was the first court decision in which copyright protection was interpreted to apply to the user interface. Previously, the courts had held that only the software program's algorithm was truly creative and thus copyrightable.

The idea that a program's "look and feel" are copyrightable has startled the computer-law community.

Lotus grabs headlines

Then in January, Lotus Development Corp (Cambridge, MA) filed suit against Paperback Software International (Berkeley, CA) and Mosaic Software (Cambridge, MA), two companies whose spreadsheets, it claimed, copied the user interface of its own best-selling product, Lotus 1-2-3. Lotus's suit has attracted a lot of attention for two reasons. One reason is that Lotus is much bigger than either Paperback or Mosaic, which has led some industry observers to wonder if the suit is merely an anticompetitive tactic.

The other reason for the suit's notoriety are the ramifications for the software market should Lotus win. Critics believe that a Lotus victory will discourage programmers from trying to improve existing products. These critics claim that clone products hold down costs and are the result of evolution, not plagiarism. Supporters of the company's position, however, contend that a decision in its favor will lead to more, rather than fewer, creative programs.

Lotus drew additional attention in April when it was sued by SAPC Inc. As Software Arts, SAPC had created the VisiCalc spreadsheet and then sold it to Lotus; ironically, it sued Lotus on the grounds that 1-2-3 copies VisiCalc commands, screen displays, and keystrokes.

Later that same month, Digital Communications Associates successfully sued SoftKlone of Tallahasee, FL, for infringing on the status screen of its popular communications package, Crosstalk. In a ruling that surprised the legal community, a Georgia court affirmed that Mirror, SoftKlone's spreadsheet package, infringed on Digital Communications' copyright.

Ease of use is crucial

The issue of a product's look and feel is growing in importance because changing software-market demographics have made ease of use an increasingly expensive and critical aspect of product development.

The days when customers accepted awkward and hard-to-use products are long gone. Command-driven user interfaces require the memorization of arcane, often unwieldy command strings. Ashton Tate's dBase III, the best-selling database-management program for IBM-compatible PCs, once had this sort of cumbersome interface, but has since been modified to include cross-screen menus that make it easier to use.

Such conveniences are very important. Many of today's software users have little technical training. They expect a program to use simple, straightforward terms that will guide them through its procedures.

The phenomenal success of Apple Computer's Macintosh computers best illustrates the public's delight with easy-to-use products—and the potential profits that can result from inspiring that delight. Although the Macintosh is not compatible (without an expansion board) with the industry standards MS-DOS and PC-DOS, its playful, icon-based user interface has made it a success.

As a result of the huge customer base that awaits easy-to-use products, software makers are beginning to consider their icon-driven commands, mouse functions, and pull-down menus as key features. The desire to protect their products' user interfaces—as well as their investment in those products and their market share—is what has led them to court.

Spotting a ready market

The large following of an established product is particularly attractive to clone makers. The user community has already invested the time needed to become familiar with such a product. Lotus 1-2-3, with its distinctive menu system, and Crosstalk, a telecommunications package, are examples of products that are so widely used they've become de facto industry standards.

In addition to capitalizing on the large user base of de facto standards, clone makers avoid the high costs associated with the research and development of an easy-to-use system. Software is designed to run on a machine, not to be "used" by an individual. Making it easy to use constitutes yet another time-consuming and expensive task.

Because clone makers dodge such development costs, they can offer their products at greatly reduced prices. Lotus 1-2-3, for example, sells for $495, as it has since its 1982 introduction. Mosaic Software's Twin, on the other hand, retails for $75.

Judges who've addressed the look-and-feel issue have disagreed on what, if any, aspects of a display are copyrightable. Different jurisdictions have put forth different opinions. However, it seems clear that a company deemed to have appropriated another company's creative user interface will incur penalties.

In light of the recent suits, the best advice for new-product developers is to refrain from using distinctive, easily recognizable features of another product's user interface. Certainly, a company should refrain from employing a name that capitalizes on a product's similarity to another product—like Mirror or Twin—because a judge may interpret such a name as a less than subtle admission that a product has been copied.

Where the line will be drawn regarding these issues is unclear and likely to remain so for some time. The final decision might be left to the Supreme Court. But one thing is certain: The look-and-feel issue has been added to the list of concerns that software makers must address when trying to develop a competitive and successful new product. **EDN**

Author's biography

Richard Beutel is an attorney with Abrams, Westermeier, and Goldberg, a Washington, DC, computer-law firm specializing in software law. Prior to joining the firm, he practiced law for two years in Silicon Valley. Beutel earned a JD at Georgetown University Law Center (Washington, DC) and a BA at Pomona College (Claremont, CA).

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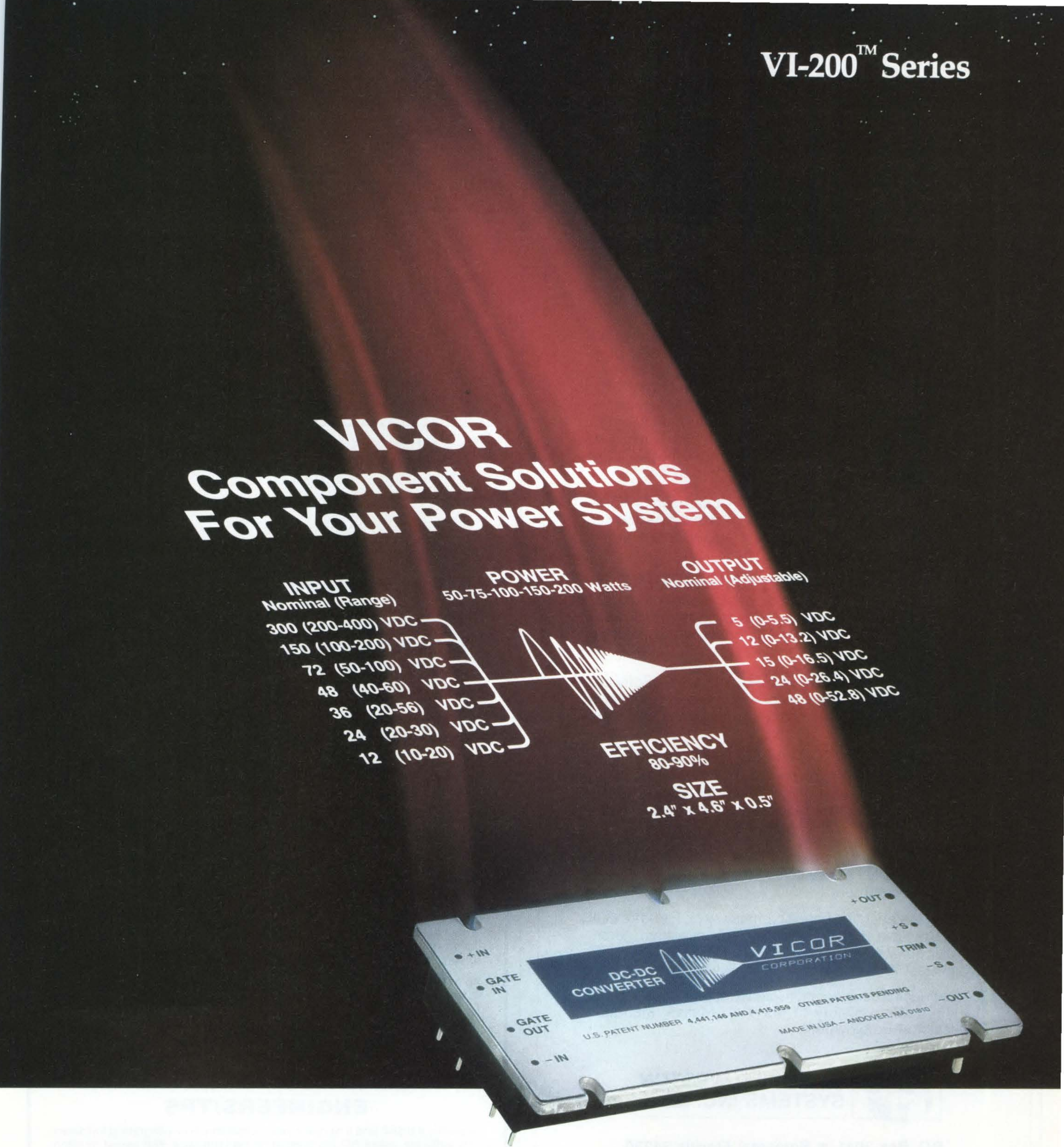

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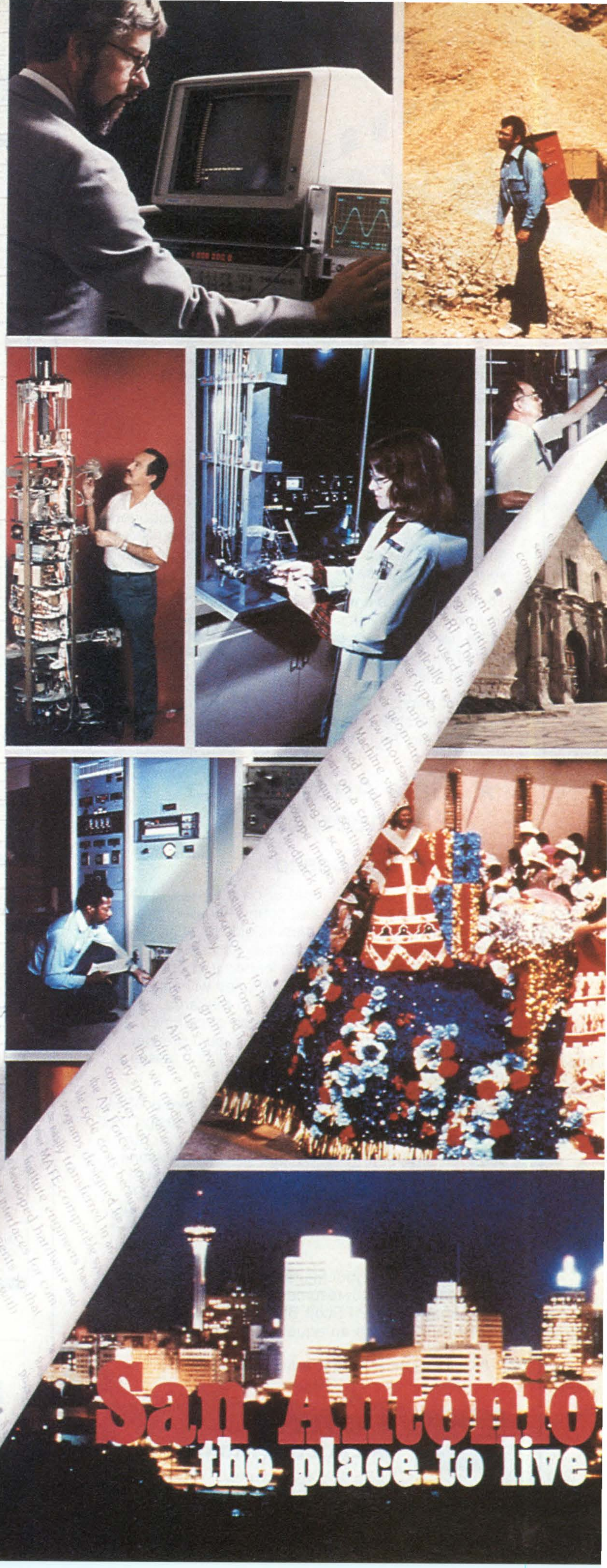

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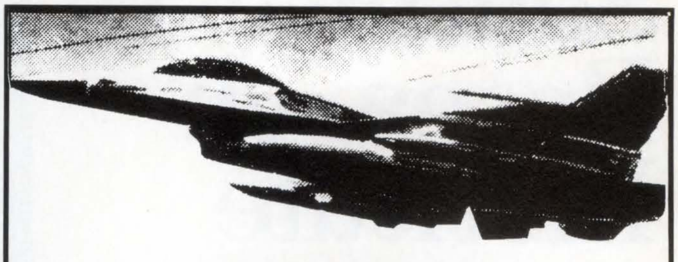

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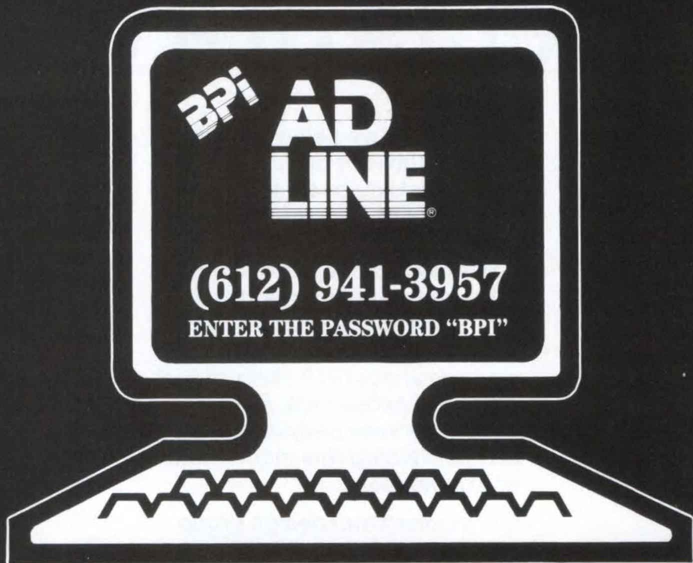

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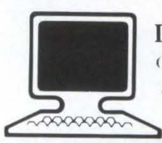

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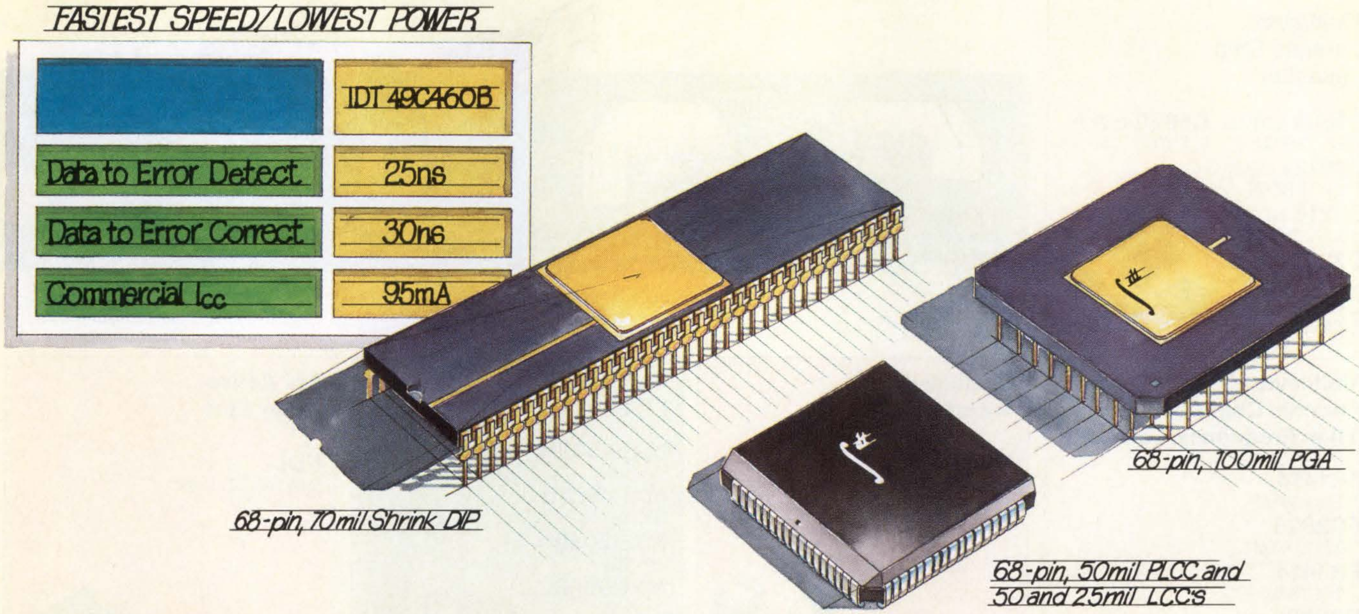
World's Fastest

32-bit CMOS EDC

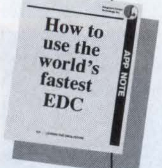
25ns | DETECT TIME



IDT49C460B: fastest speed, lowest power 32-bit EDC.

Your memories are getting bigger and with that comes higher error rates. Use the new, faster IDT49C460B to enhance data integrity. It corrects all single-bit errors, detects all double and some triple-bit errors.

Replaces 2960s. You can easily upgrade existing 2960 systems with the IDT49C460B because both devices use the same Hamming code. Your design benefits from faster speed, improved power consumption and a 3-to-1 reduction in chip count. Byte writes, byte operations and diagnostics are included.



Faster than bipolar. The IDT49C460B detects an error in 25ns and corrects in 30ns. Nothing is faster.

Lowest power. The only 32-bit EDC in CMOS consumes just 95mA commercial. Now you can get EDC faster than the fastest bipolar but with CMOS power.

Cascades to 64 bits. Only IDT offers you a simple, two chip solution for 64-bit EDC. (The TI632 cannot be cascaded to 64-bits; while the Am2960 approach requires 14 devices.)

16-Bit EDC

	IDT39C60A	IDT39C60-1	IDT39C60
Data to error detect	20ns	25ns	32ns
Data to error correct	30ns	52ns	65ns
Commercial I_{CC}	85mA	85mA	85mA

Speed leadership in 16-bit EDC.

We also make a family of 16-bit CMOS EDCs. All are 2960 pin compatible with improved output drive while consuming only 1/4 the power.

The IDT39C60A is unquestionably the highest performance TTL compatible CMOS 16-bit EDC in the world. And more than just some "specs on paper," it's *available now—in volume.*

The IDT39C60-1 and IDT39C60 are equal in speed to the 2960-1 and 2960.

Packages. ☐ 48-pin plastic and ceramic DIPs. ☐ 52-pin PLCC/LCCs.

Cascadable. Up to 64 bits.

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Contact our local representative, call **1-800-IDT-CMOS**, or fill in the bingo for a copy of our *Data Sheet* and our *Application Note* explaining how to use 16- or 32-bit EDC.

Also ask for our *Product Selector Guide* on CEMOS™ **MICROSLICE™** (bit-slice microprocessor products), **Subsystems, Memory Interface Logic, Digital Signal Processing Circuits** (multipliers and MACs), **Data Conversion Products, E²PROMs** and one of the fastest, broadest lines of **Static RAMs** in the world (including the biggest, fastest families of **FIFOs** and **Dual Ports**).

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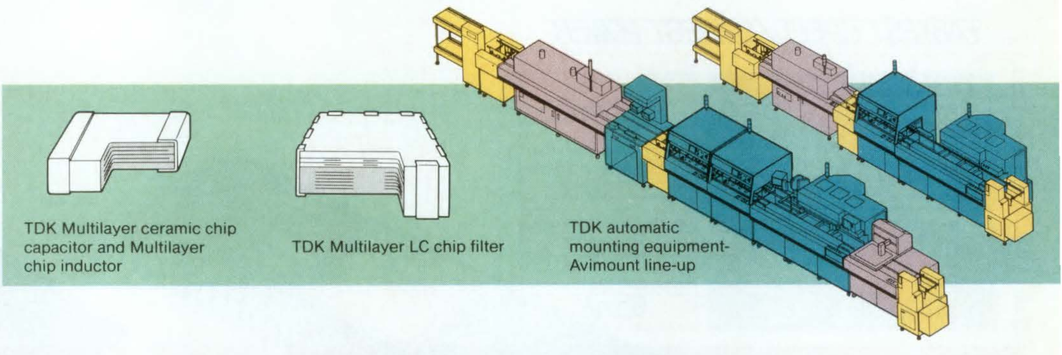
As boards are getting thinner, TDK is helping that diet succeed by providing a variety of extra-slim surface mountable components. Nourished by TDK's expertise in ferrite and ceramic materials, these miniaturized components feed on TDK—developed multi-layerization and multi-functionalism. How do we know the exact needs of high-quality automated board production? Well, a fair share of the world's automatic mounting equipment—the Avimount series—comes from TDK.

Multilayer Ceramic Chip Capacitor

C1608 (CC0603)
C: 0.5~22,000pF
C2012 (CC0805)
C: 0.5~100,000pF
C3216 (CC1206)
C: 0.5~220,000pF
C3225 (CC1210)
C: 750~470,000pF
C4532 (CC1812)
C: 2,400pF~1μF
C5650 (CC2220)
C: 5,100pF~1.5μF



TDK Multilayer ceramic chip capacitor and Multilayer chip inductor

TDK Multilayer LC chip filter

TDK automatic mounting equipment-Avimount line-up

Multilayer Ceramic Chip Capacitor (High Frequency, Low Loss)

FC1414
C: 0.5~3,300pF
FC2828
C: 0.5~22,000pF
FR1414
C: 0.5~3,300pF
FR2828
C: 0.5~22,000pF

Multilayer Chip Transformer

MTT4532
L: 10~200μH

Multilayer Chip LC Filter

MXF4532H
HPF (Tuner)
MXF4532B
BPF (FM radio)
MXB5050B
BPF (VCR)
MXB5050L
LPF (VCR)
MXB5050D
Delay Line (VCR)

A variety of characteristics are available.
Please specify when ordering.

SM Active Delay Line

FDL
Delay time: 20~75 nsec.

Leadless Inductor (Wound Chip Inductor)

NL322522
L: 0.01~220μH
NL453232
L: 1.0~1,000μH
NL565050
L: 1,200~10,000μH
NLF453232
L: 1.0~1,000μH
(Shielded Inductor)

Multilayer Chip IFT

MIA4532
F: 455, 459, 464kHz
MIF4532
F: 10.7MHz

Multilayer Chip Capacitor Network

MCN7575
TC: CH, 1~100pF (10 capacitors)
SL, 10~1,000pF (10 capacitors)

Class II, 100~470,000pF (10 capacitors)

SM Transformer/ Inductor

EE5
ER9.5
ER11
T2

A variety of characteristics are available.
Please specify when ordering.

Multilayer Chip Inductor

MLF3216
L: 0.047~33μH
MLF3225
L: 39~220μH

Multilayer Chip LC Trap

MXT4532
F: fo ±2%

Ferrite Chip Beads

CB201209
Zo: 7, 10, 11Ω
CB321611
Zo: 19, 26, 31Ω
CB322513
Zo: 31, 52, 60Ω
CB453215
Zo: 70, 120, 125Ω

SM Step-up Inductor (Piezoelectric Buzzer)

OL3.3 x 1.6
OL3.3 x 2.1

Inductance values are representative, please specify value when ordering.

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CIRCLE NO 298

LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG

UPS shipments to grow at 20% per annum

Clean, consistent ac power from public sources is no longer a workable assumption for many applications, particularly as more sensitive electronic systems and equipment become available for commercial and industrial uses. Power irregularities cause havoc in all kinds of situations from interruptions in crucial services to malfunctions of basic equipment. Although power irregularities are typically associated with public power supplies, the failures of internal power-distribution networks can just as easily cause power disturbances. And these disturbances can spread throughout the internal network of a facility.

Venture Development Corp (Natick, MA) has found that these two sources of disruption—the unpredictability of external power sources and the intrinsic difficulties of internal distribution of power—will create a demand of about 20% annually for uninterruptible power supplies (UPSs) through 1991. Assessed at $649.4 million in 1987, the US shipments of UPSs should exceed $1.3 billion by 1991.

VDC concludes that other options —dedicated lines, shielded isolation transformers, line-voltage regulators, line-power conditioners, and motor generators—cannot protect a critical load from virtually all the potential commercial power-source problems as reliably as UPSs can. On-line UPSs now dominate US shipments, but the demand for off-line sources of the same nature will expand during the next few years.

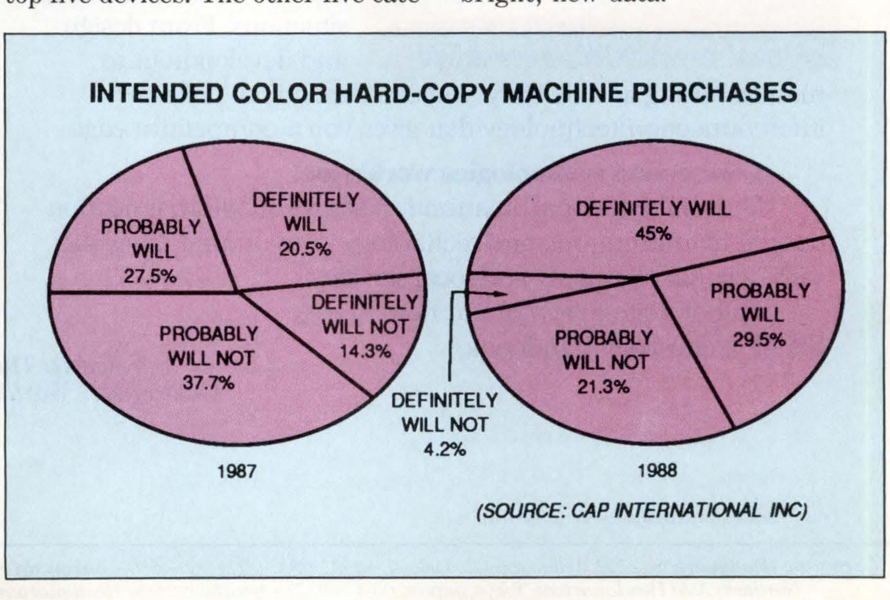
Color enriches hard-copy-output markets

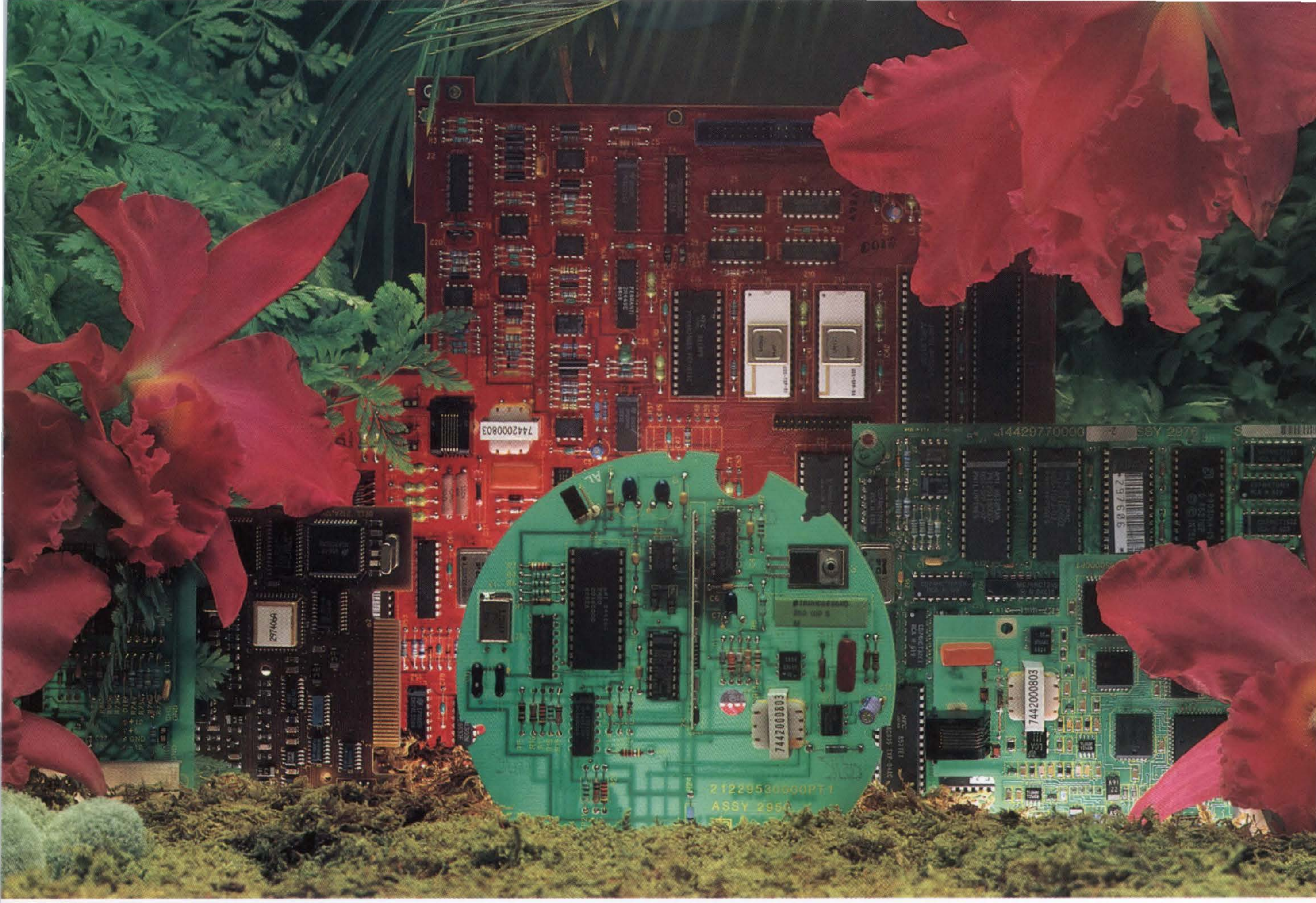
Color begets more color. The rise in color-monitor use, the proliferation of color software packages, and the availability of better performance for less money have together created a dramatic increase in the desire for color hard copy, according to CAP International Inc (Marshfield, MA). In fact, American commercial concerns are now willing to pay for color in surprising numbers.

A survey conducted by CAP found that, when asked whether they intended to purchase machines to produce color hard copy, 48% of the respondents either expressed a definite intention to buy (20.5%) or their probable intention to buy (27.5%) color-printing equipment by year's end. By the end of 1988, CAP predicts the total number of users who at least intend to buy will swell to 75%. The various sorts of commercial organizations surveyed ranged from CAD/CAM companies to businesses that use slide presentations to serve their clients.

CAP defines a color hard-copy machine as one capable of producing three or more full colors without manual intervention. Pen plotters lead the top five processes that users believe to be most useful for their needs. Increasing in popularity are laser printers, which users rate second in desirability; in diminishing order of interest, ink-jet printers, electrostatic plotters, and dot-matrix printers round out the top five devices. The other five categories in descending rate of popularity are electrophotographic copiers, film recorders, photographic copiers, thermal-transfer printers, and thermal-transfer copiers.

Color options for hard copy might present users with a somewhat happy quandary: On the one hand, the improved vividness of presentation, the addition of a mode for providing more data within the same picture, and the sheer visual pleasure of color will enhance hard-copy applications in a multitude of ways. But if one picture can be worth ten thousand bytes, that same picture with ten or twenty hues could need a megabyte RAM operating at several MIPS to decipher it in a reasonable amount of time. Graphics are designed to be experienced primarily visually—not verbally. "The complexity of multifunctioning elements can sometimes turn data graphics into visual puzzles, cryptographical mysteries for the viewer to decode," warns Edward Tufte in *The Visual Display of Quantitative Information* (Graphics Press, Cheshire, CT, 1983, pg 153). Users may need more help learning about restraint with their new color-palette freedom than about actually generating their bright, new data.





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Non-standard modem functions are another specialty of the house. For example, UDS engineers have already designed and delivered a hand-held RF modem operating at 4800 bps!

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