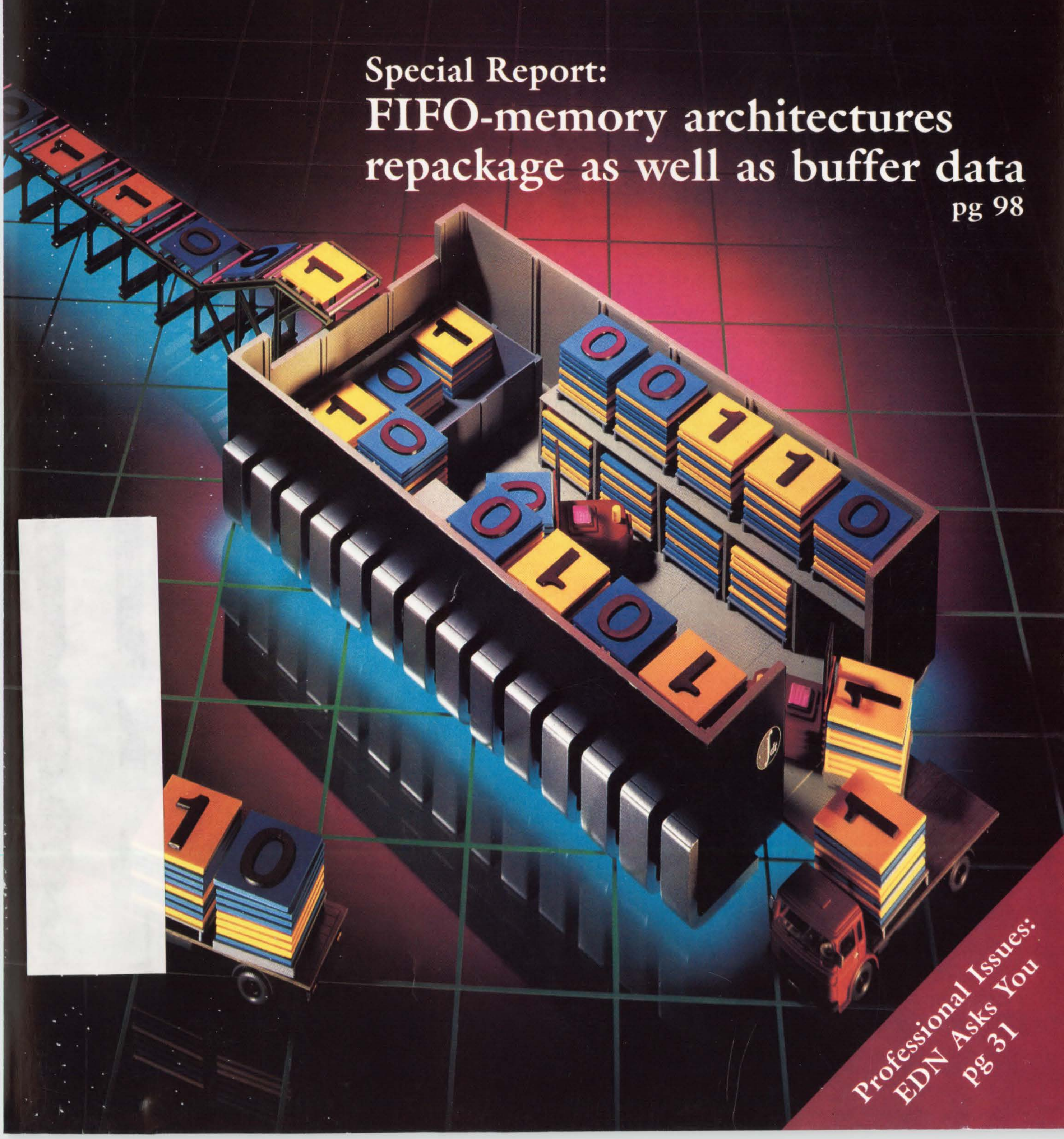
A CAHNERS PUBLICATION JANUARY 21, 1991

EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Special Report: FIFO-memory architectures repackage as well as buffer data

pg 98

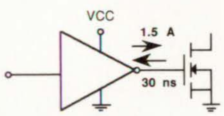
Professional Issues: EDN Asks You pg 31

Lead, follow, or get out of the way.

Presenting the three rules of BiCMOS design.

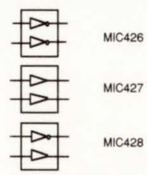
Now, one family drives all FETs.

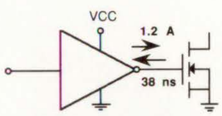
High Speed, High Current Low Side MOSFET Drivers



Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

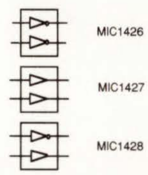
MIC426/7/8 (Original)
- 30 nS into 1000 pF
- 4.5 V to 18 V supply
- 1.5 A peak output
- 6 Ω output impedance
- Available in surface mount packages

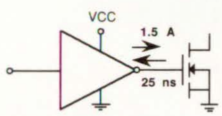




Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

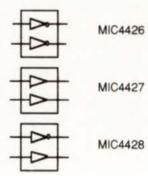
MIC1426/7/8 (Low Cost)
- Low cost predriver
- 38 nS into 1000 pF
- 4.75 V to 16 V supply
- 1.2 A peak output
- 8 Ω output impedance
- Available in surface mount packages

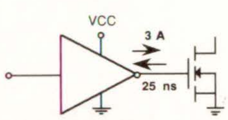




Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

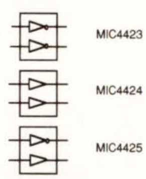
MIC4426/7/8 (Protected)
- Latch-up protected
- 25 nS into 1000 pF
- 4.5 V to 18 V supply
- 1.5 A peak output
- 7 Ω output impedance
- Withstands 5 V negative swing
- Available in surface mount and high temperature packages

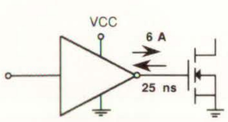




Drives a hex 4 - hex 5 size MOSFET; 6000 pF to 12000 pF.

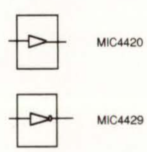
MIC4423/4/5 (High Current)
- Latch-up protected
- 25 nS into 1800 pF
- 4.5 V to 18 V supply
- 3 A peak output
- 3.5 Ω output impedance
- Withstands 5 V negative swing
- Available in surface mount packages

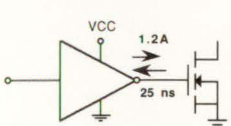




Drives a hex 6 - hex 7 size MOSFET ; 15000 pFto 16000 pF

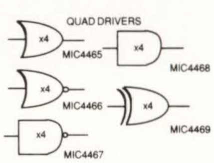
MIC4420/4429 (Singles)
- Latch-up protected
- 25 nS into 10,000 pF
- 4.5 V to 18 V supply
- 6 A peak output
- 2.5 Ω output impedance
- Withstands 5 V negative swing
- Available in surface mount packages



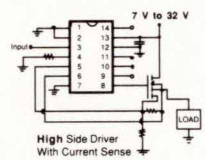


Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF

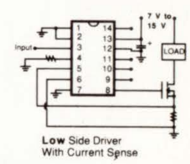
MIC4465/6/7/8/9 (Quad)
- Latch-up protected
- 25 nS into 470 pF
- 4.5 V to 18 V supply
- 1.2 A peak output
- Available in surface mount packages
- Five logic choices

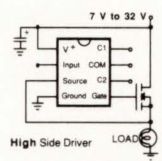


High Side, Protected MOSFET Drivers

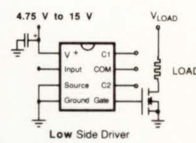


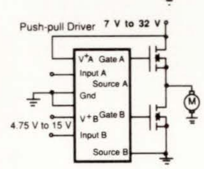
MIC5010
- Full Featured predriver
- Optional speed up caps
- 7 V to 32 V supply
- Internal charge pump
- 60 μS into 1 nF
- Over current sensing
- Fault flag output
- Surface mount packages
- Dynamic sensing threshold



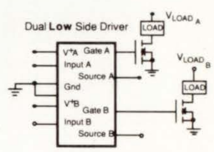


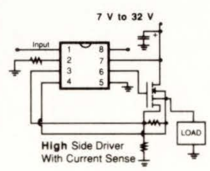
MIC5011
- Minimum parts count
- Optional speed up caps
- 4.75 V to 32 V supply
- Internal charge pump
- 60 μS into 1 nF
- Surface mount packages



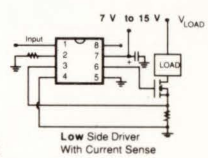


MIC5012
- Dual predriver
- Provides high and low side
- 4.75 V to 32 V supply
- Internal charge pump
- 60 μS into 1 nF
- Surface mount packages





MIC5013
- Over current sensing
- 7 V to 32 V supply
- Fault flag output
- Internal charge pump
- 60 μS into 1 nF
- Surface mount packages
- Dynamic sensing threshold



Choose from the widest selection of MOSFET predrivers in the industry. Whether your specification requires ultrafast low side driving, overcurrent protected high side driving, or overcurrent protected low side driving of 1 Amp to 100 Amp MOSFETs, we can supply the right product from our family of CMOS drivers to reliably meet your needs. For details contact: Micrel Semiconductor, 560 Oakmead Parkway, Sunnyvale, CA 94086. Or call (408) 245-2500.

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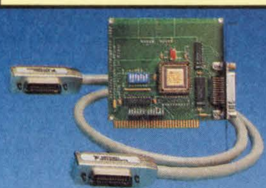
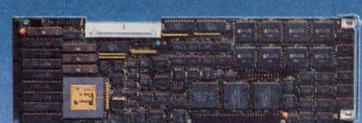
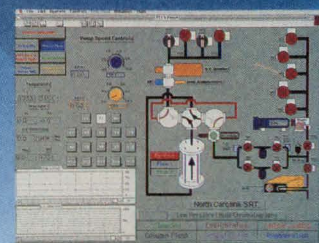
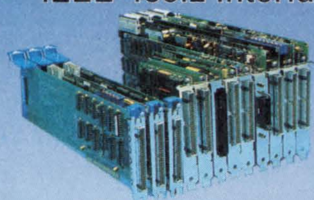
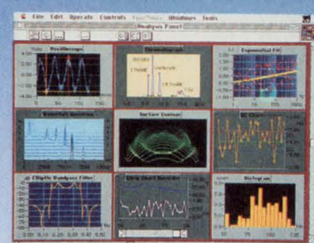
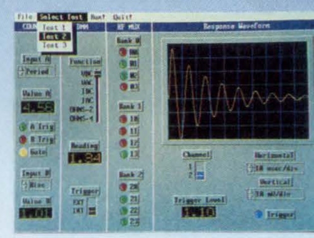

IEEE-488.2 Interfaces


DSP Hardware


LabVIEW 2
Graphical User Interface

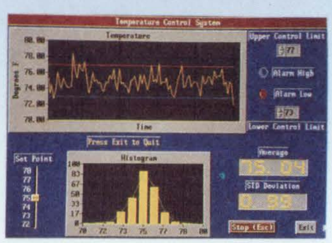

Plug-in Data Acquisition


Macintosh Analysis Software

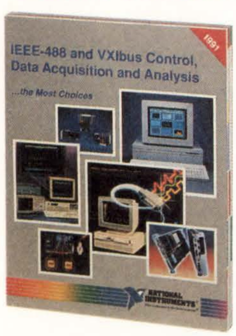

LabWindows 2.0
Graphical User Interface


VXI
Controllers


Software
for RS-232
Instruments


DOS-Based Analysis Software

And Here Are Two Great Ways to Learn More About Your Choices!



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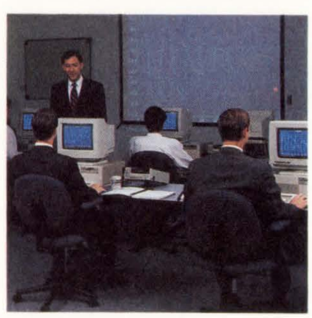

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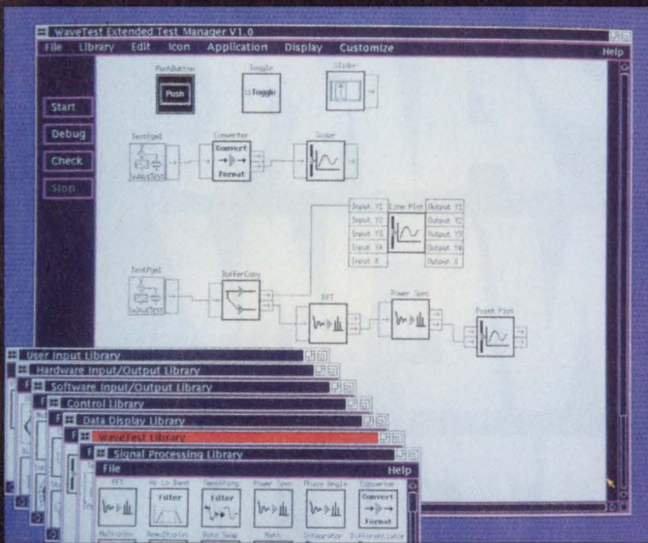
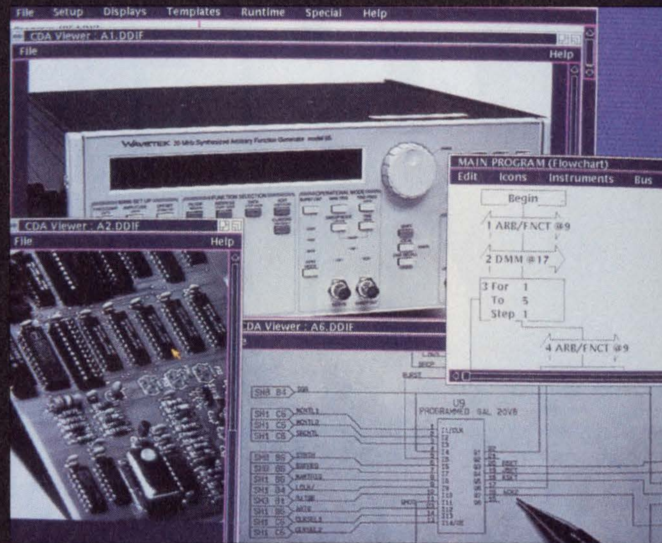


Just select and move icons to build a complete ATE test and data management program.



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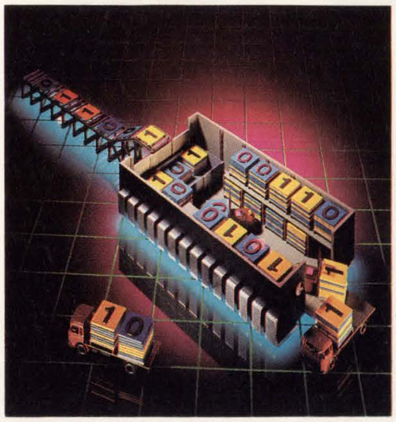
Volume 36, Number 2 January 21, 1991
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: Certain features of first-in, first-out (FIFO) memories make them ideal buffers for the data flowing between devices operating at different rates. Read about it in our Special Report on pg 98. (Photo courtesy Integrated Device Technology; photography by Mel Lindstrom; model maker, Evan Ormondroyd)

Continued on page 7

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Continued from page 5

***Today vendors offer an assortment** of servo-motor controller boards for the ISA bus (pg 61).*

EDITORS' CHOICE

DESIGN IDEAS

EDITORIAL

Continued on page 9

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Continued from page 7

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January 21, 1991

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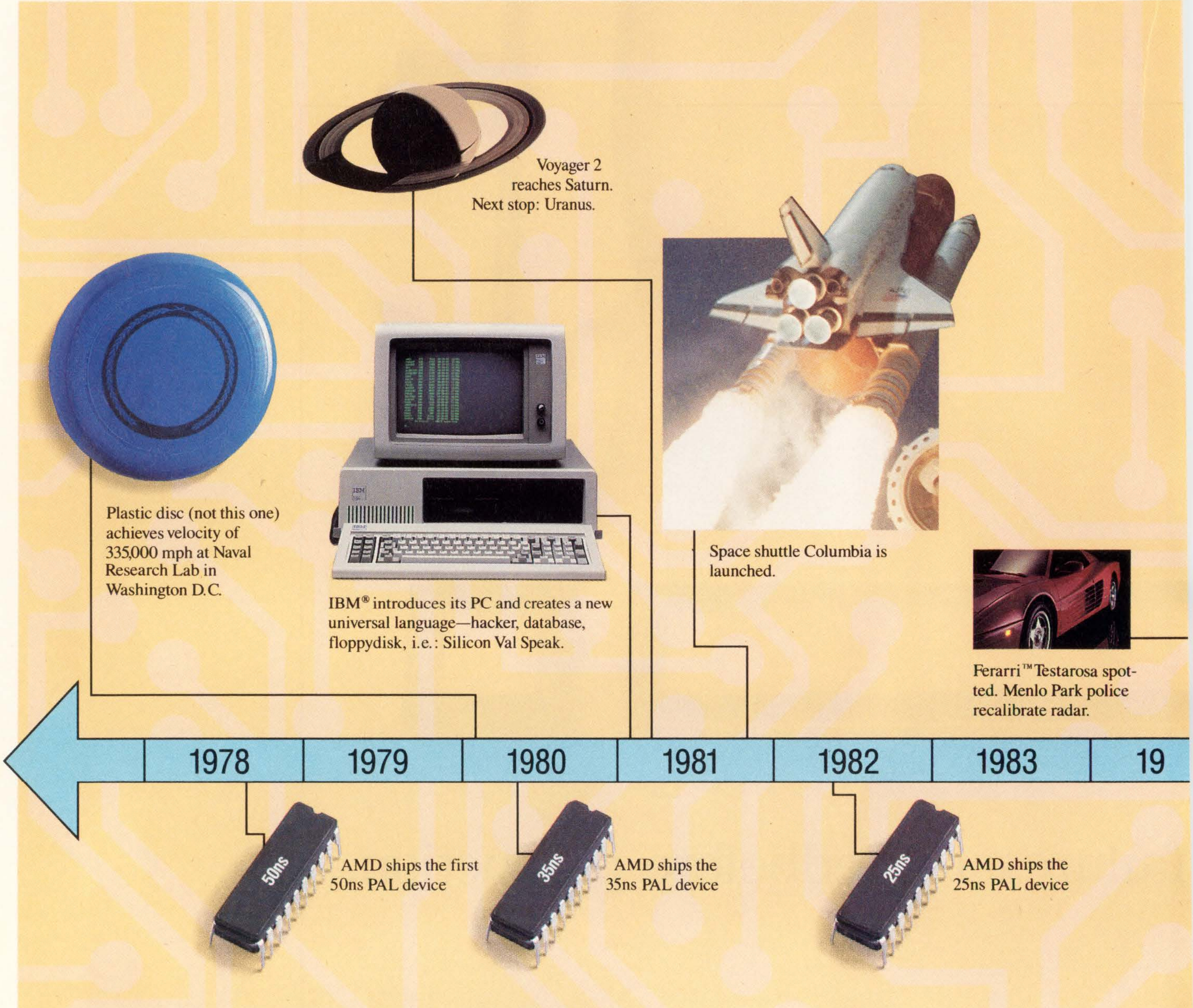

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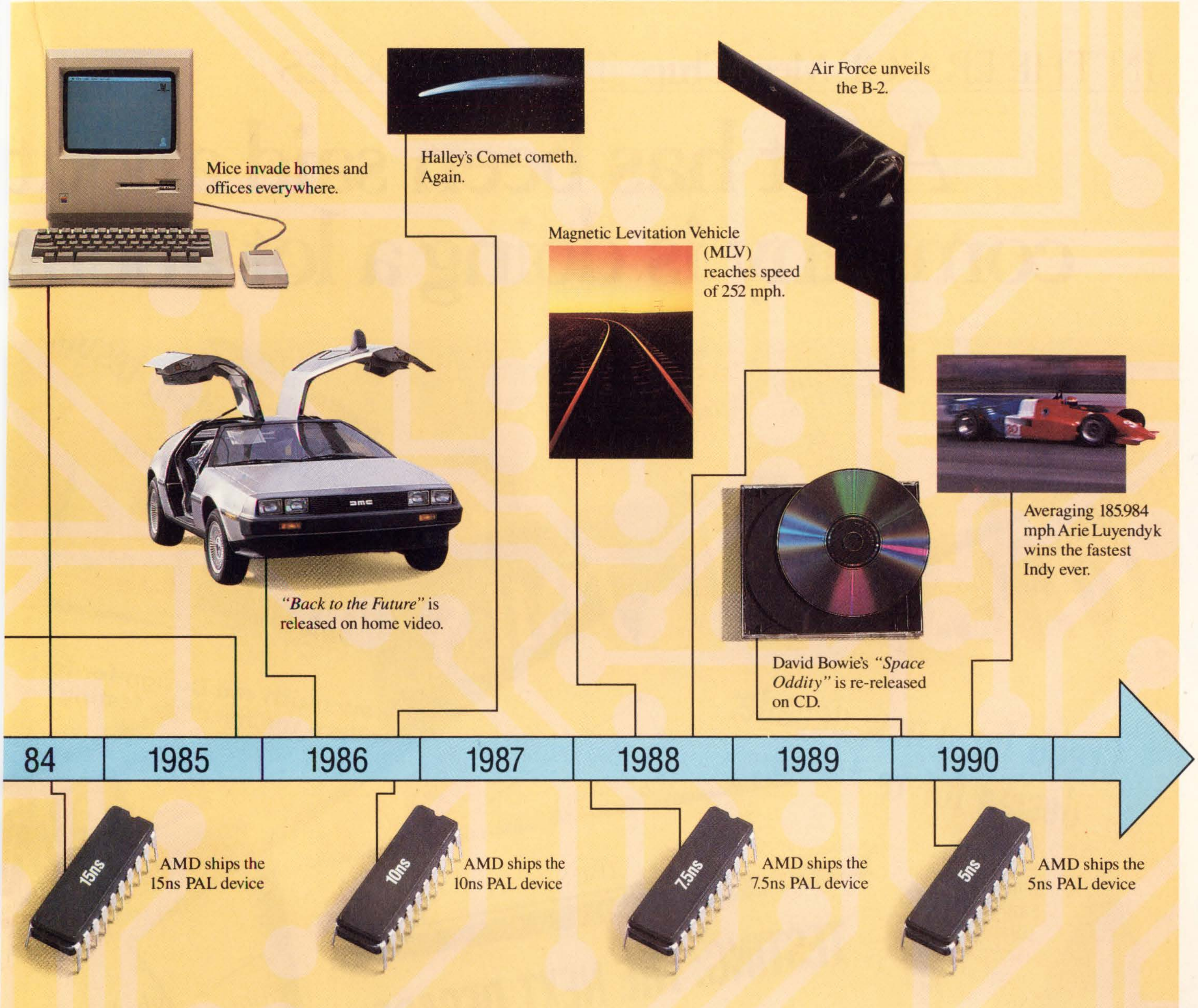

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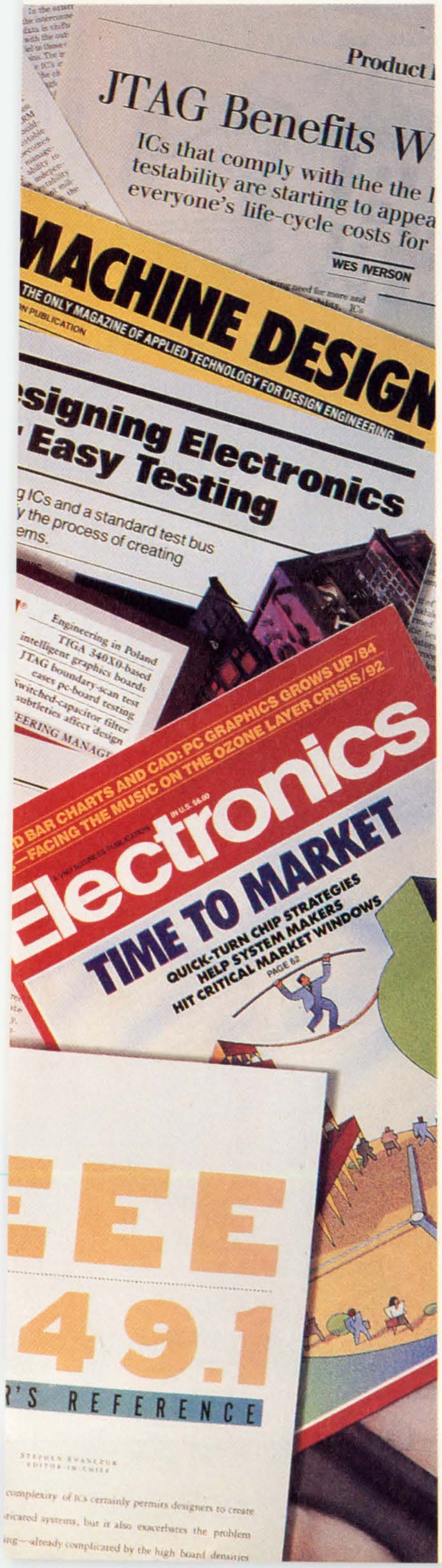
testability, but only one it. Texas Instruments.



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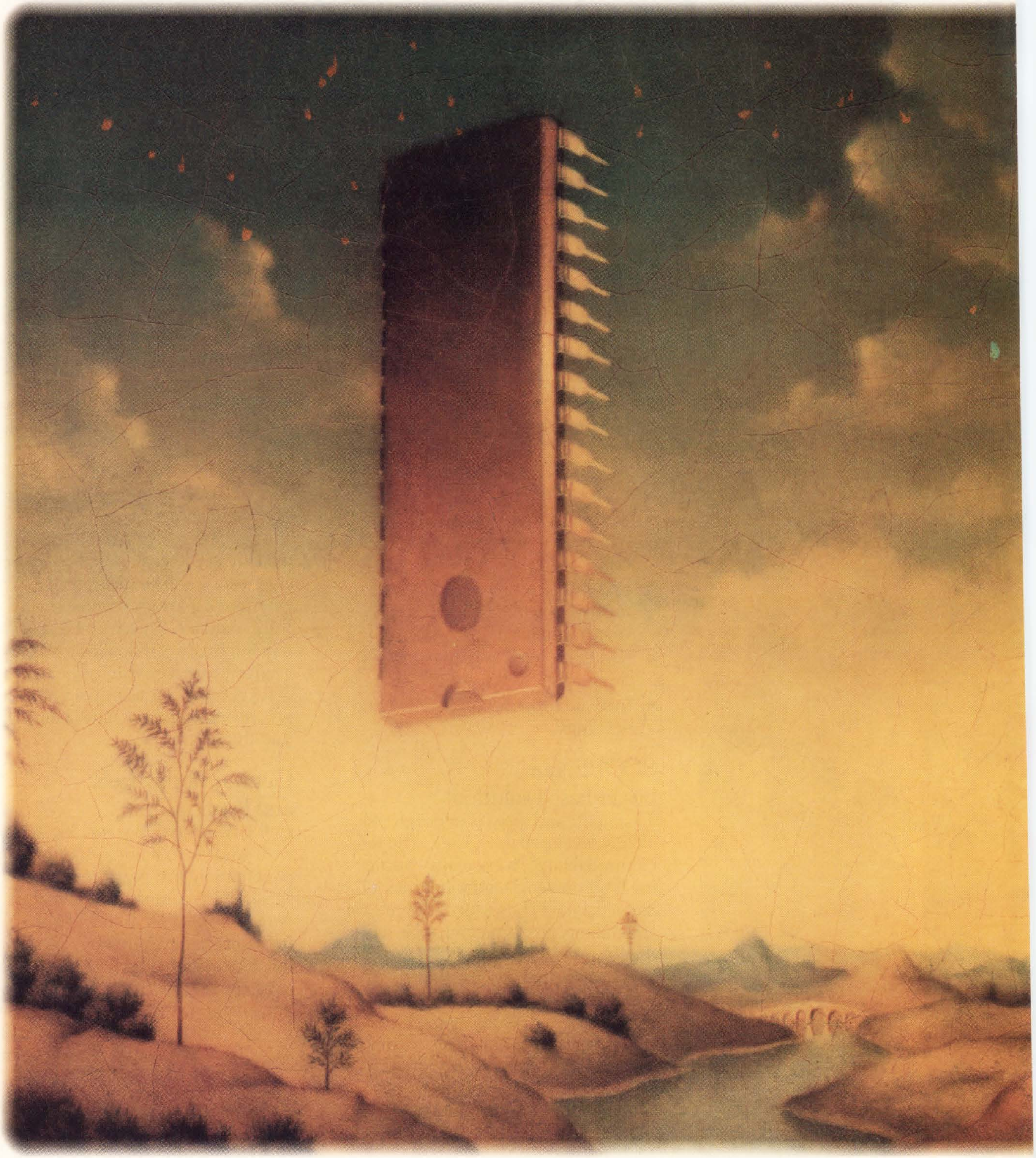

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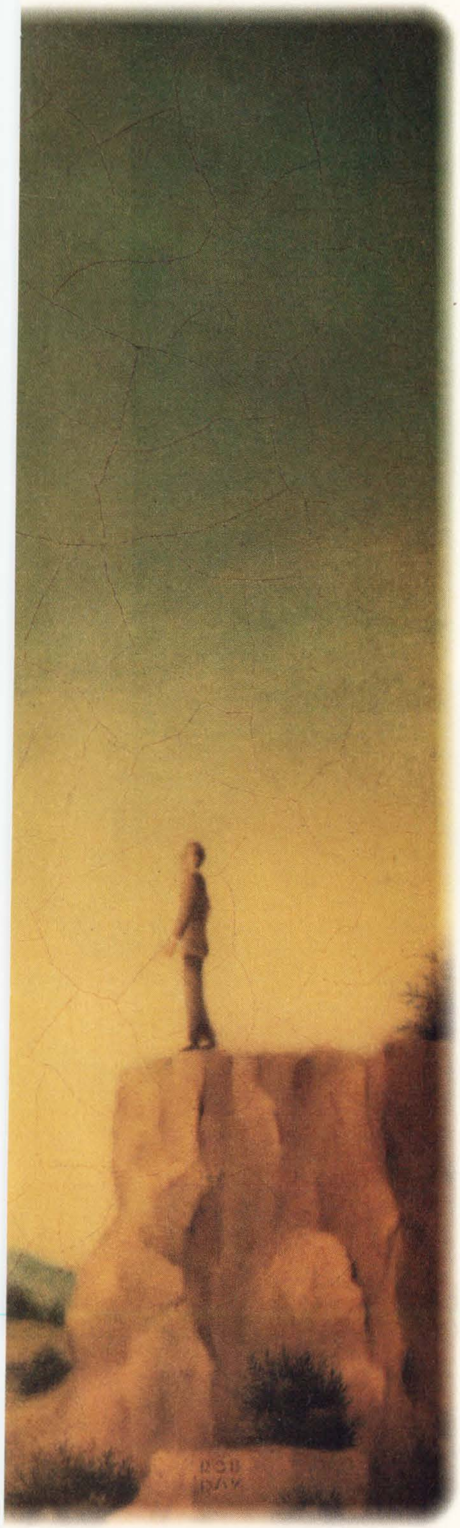

The recently introduced Samsung 1-meg SRAMs have a transistor count of 6.6 million.

In a day and age when makers of advanced microprocessors take understandable pride in the 1 million transistors on their chips, we think it's forgivable for us to be proud of the vastly greater number on these SRAMs.

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We offer the 1-meg slow SRAM in several speeds, several power ratings, and several package types. We're currently developing the part in the revolutionary TSOP packaging.

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After all, the best way to contemplate the 6.6 million transistors on the part, is to get your hands on one.

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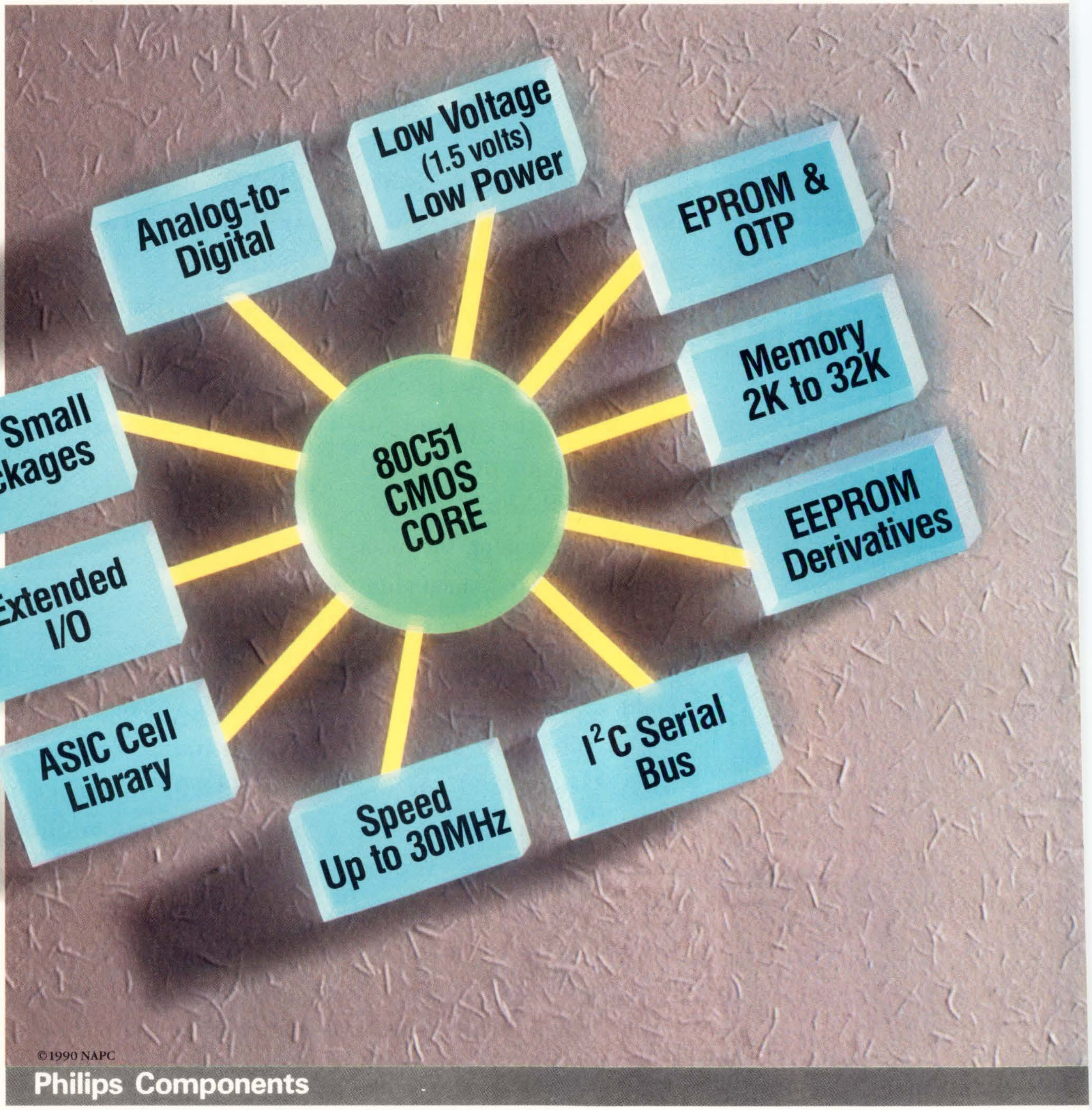

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EDITED BY SUSAN ROSE

TTL 80-MHz CLOCK-DRIVER IC DISTRIBUTES 20 SIGNAL COPIES

Silicon Connection Corp's SC3501 driver IC outputs 20 TTL-compatible clock signals with frequencies as high as 80 MHz. You can use the BiCMOS chip to handle clock distribution throughout an entire high-speed-CPU board design. The clock-driver IC requires, as input, a signal of double the desired primary output frequency. The IC has three groups of outputs. The first group consists of 10 outputs that operate at the primary output frequency. You can set the second group, which has five outputs, to be identical to the primary outputs or to operate at one-half of the primary output frequency. Likewise, you can set the third group, which also has five outputs, to a choice of one-half or one-fourth of the primary output frequency. The $17 (1000) IC comes in a 52-pin quad flatpack and is available now. Silicon Connections Corp, San Diego, CA, (619) 535-0442, FAX (619) 535-1635.—Maury Wright

GET FASTER SOFTWARE VIA SPARE HARDWARE

The complexity of design problems multiplies faster than the improvements in CPU horsepower. In contrast, some important tasks, such as schematic capture and hardware-description-language-model creation, are hardly compute intensive and waste precious MIPS when done on a workstation. Fortunately, EDA tool vendors are learning how to distribute a compute-intensive problem on system resources that might have power to spare.

Analogy (analog simulation), ISS and Mentor (IC layout and verification), Quickturn (IC emulation), Valid (analog simulation), and Vantage (VHDL model compilation) have recently introduced EDA software that breaks problems into smaller pieces and spreads them out among available network resources. All of the tools let you control which resources can be used; some offer failure-recovery methods. In addition to seeing more such distributed-processing tools in the near future, look for dynamic distribution capabilities, which can determine individual resource loading and capability and redistribute their tasks based on changing system usage. Analogy, Beaverton, OR, (503) 626-9700, FAX (503) 643-3361; ISS, Research Triangle Park, NC, (919) 361-5814, FAX (919) 361-2019. Mentor Graphics, Beaverton, OR, (503) 626-7000, FAX (503) 646-7881; Quickturn Systems, Mountain View, CA, (415) 967-3300, FAX (415) 967-3199; Valid, San Jose, CA, (408) 432-9400, FAX (408) 432-9430; Vantage Analysis Systems, Fremont, CA, (415) 659-0901, FAX (415) 659-0129.
—Michael C Markowitz

DATA-ACQUISITION MODULES CONFORM TO IEEE-488.2, SCPI

System 23 from Philips is a range of modules that includes a switching matrix, low-level and coaxial cable scanners, and digital I/O. The 19-in. half-rack enclosures let you stack modules and automatically interlink units both mechanically and electrically. The PM 2301 interface module ($1500) forms the base unit for the stack and houses a power supply sufficient for six switching modules. Also within the module is an IEEE-488.2 interface, which uses Standard Commands for Programmable Instrumentation (SCPI). The module has four external programmable bidirectional trigger lines for synchronizing system events. Triggers conform to VXIbus trigger protocol, enabling you to link the modules directly to a VXIbus system. The PM 2301 daisy chains power, triggers, and internal system communications up the stack to the other modules. It also provides a direct interface to the company's existing range of System 21 products. Other modules include the PM 2320 ($1250) 8×4 or 16×2 switch matrix; the PM 2321 ($1450) low-level scanner with a switching speed of 500 channels/sec on 10 4-wire channels; and the PM 2330 ($1650) 16-bit digital I/O interface with a 32k word-buffer memory. A front-panel connector on each of the switching modules links to the PM 2390 ($500) portable display unit for local status verification and control. Philips, Eindhoven, The Netherlands, (40) 788620, FAX (40) 788256.—Brian Kerridge

OVEN-CONTROLLED CRYSTAL OSCILLATOR IS 1.46 IN.^{3}

Raltron achieves the TF-65010-B's 1.46 in.^{3} size by eliminating the oven enclosure and wrapping the resistance wire heater directly around the crystal. The oven-controlled crystal oscillator stability is $\pm 2 \times 10^{-7}$ for temperatures from −20 to +70°C. Steady-state power requirements are 3W, and the device stabilizes in two minutes. The $65 (10,000) oscillator is available in frequencies from 1 to 20 MHz. Raltron, Miami, FL, (305) 593-6033, FAX (305) 594-3973.—Doug Conner

MANUFACTURER BETS $80.51 THAT ITS ICE IS BEST

Metalink is offering an incentive to try its Ice Master in-circuit emulator (ICE): If you decide that the emulator's windowed user-interface and hardware isn't what you need, the company will refund the purchase price, plus an $80.51 "evaluation fee" for your trouble.

The emulator's trace buffer uses a forward- or backward-searching scheme to locate any label, source line number, or address during debugging. During disassembly, a code window displays the contents of memory locations, registers, and any directional changes in the control flow. The emulator's 115k-bps RS-232C link lets you download most programs in less than 3 sec. Pricing for the emulator starts at $1495. Device-specific, interchangeable probe cards sell from $345. The company also has free demo disks. Metalink Corp, Chandler, AZ, (800) 638-2423, FAX (602) 926-1198.—J D Mosley

POPULAR PLD PICKS UP SPEED

Cypress Semiconductor's high-speed versions of the 22V10 PLD have propagation delays of 7.5 nsec max and 190-mA supply currents. The company uses ECL circuitry for the speed-critical paths within the chip and CMOS for the control logic. The devices come in either a 24-pin DIP or a 28-pin plastic leaded chip carrier (PLCC). The PAL22V10C PLCC costs $30 (100), and the PAL22VP10 DIP costs $39.45. Cypress Semiconductor, San Jose, CA, (408) 943-2600, FAX (408) 943-2796.
—Richard A Quinnell

UNIX-BASED CAE TOOLS DON'T HAVE TO BE EXPENSIVE

Phase Three Logic's $995 Capfast runs on SPARCstations, providing a cost-effective alternative to the thousands of dollars needed for Unix-workstation-based schematic-capture packages. The schematic editor has hierarchical capabilities that let you create and use symbols. It also has an on-line electrical-rules checker, an interactive simulation grapher, and interfaces to Spice, Hilo, Susie, Actel, and Xilinx software packages. The package uses an ASCII file format; the software's database is compatible with the company's IBM PC schematic editor. An optional EDIF 2 0 0 translator is available to provide an interface to Mentor, Cadence, and Valid tools. Phase Three Logic, Beaverton, OR, (503) 645-0313, FAX (503) 645-0207.—Michael C Markowitz


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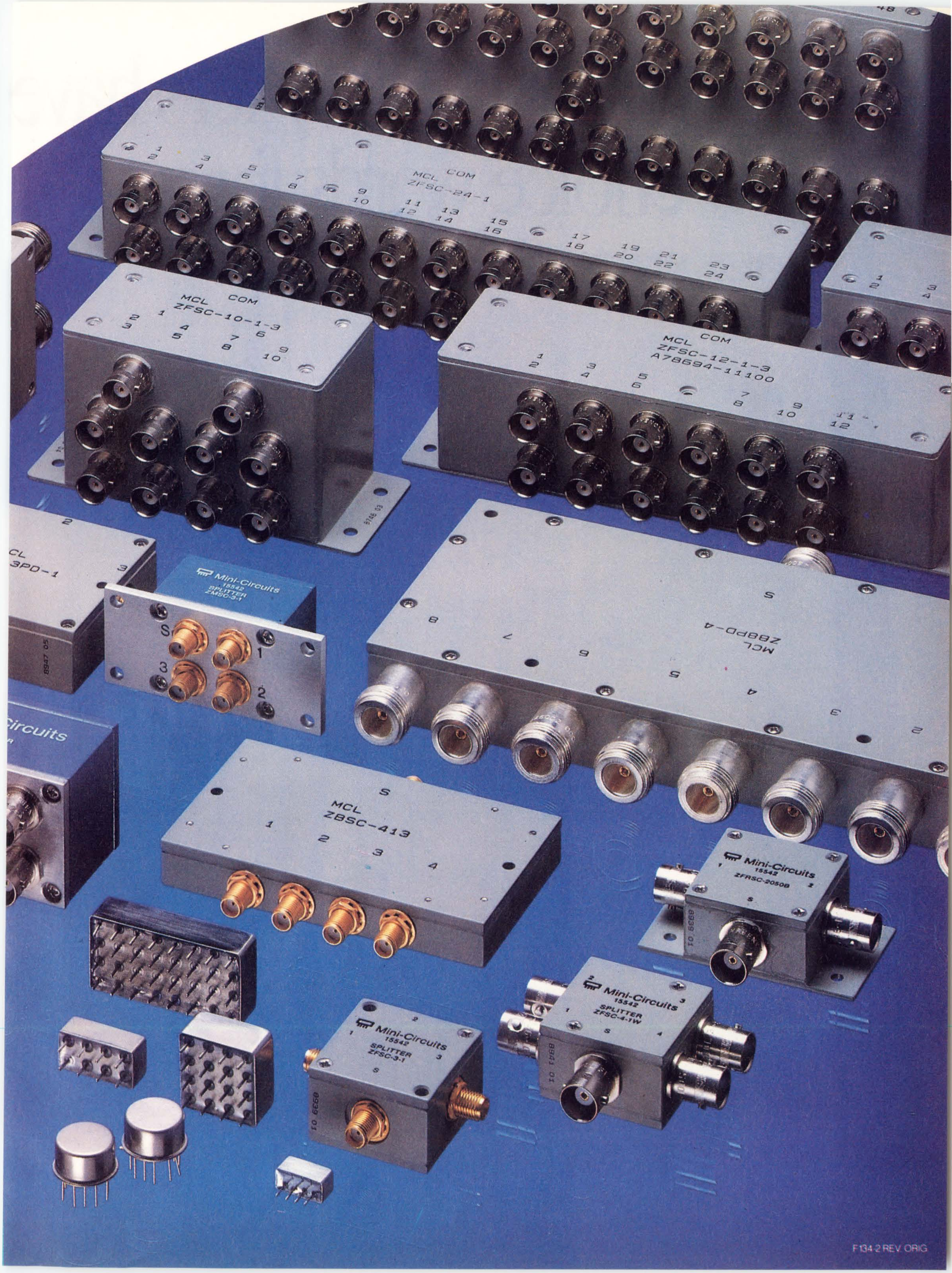

F134-2 REV. ORIG

Recently, our customers have a few choice words for us.

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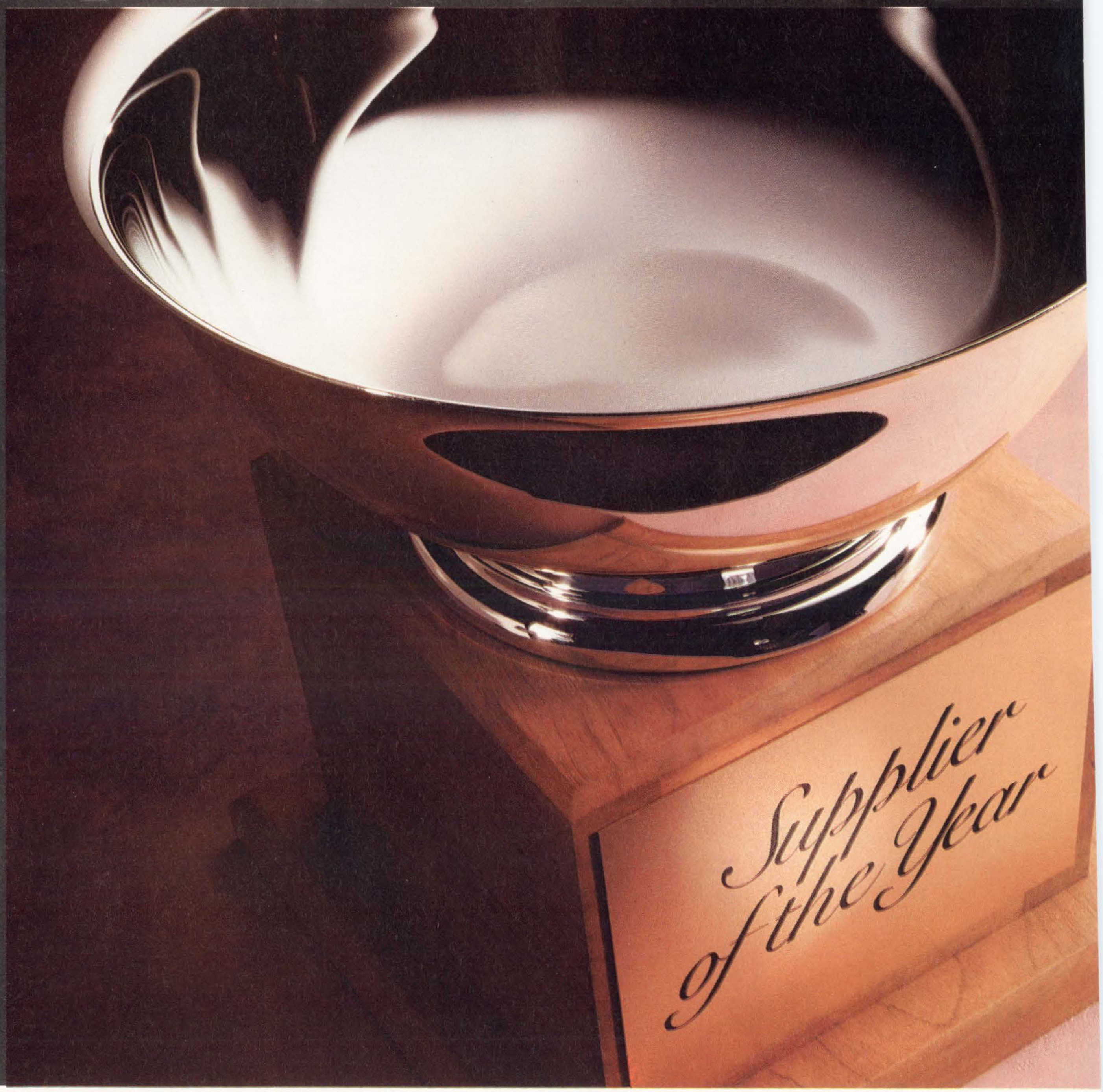

had

For years Seagate has been best-known as the volume producer of disc storage products. But our reputation as solely a manufacturing powerhouse is beginning to change.

H N O L O G Y

In the past several months Seagate has received three Disc Drive Supplier of the Year awards from some of our valued OEM customers. In every case, the commendations have been earned not just for supplying quality products, but for providing superior customer service.

ICL, Britain's leading information technology company, honored us with their Vendor Award Citation for being responsive to their flexibility of delivery and cost of ownership requirements. In addition, our Wren drives exceeded their stringent reliability and "plug-and-play" criteria.

Olivetti, the Italian computer company, awarded us their Quality Award for Customer Satisfaction for the same reasons. By meeting Just-in-Time delivery schedules, listening to the customer, exchanging data from the field and providing training and support, we have helped Olivetti provide superior products and service to their customers.

Most recently, AT&T's Oklahoma City Works presented Seagate with its 1990 "Partner in Excellence" award during their Quality Month observance. Once again, Seagate was selected for its ability to meet AT&T's high standards of quality, delivery, service, cost and technical support.

So while Seagate is still the first name in disc drives, we're making quite a name for ourselves in quality and customer service, as well. To learn more about the benefits of a partnership with Seagate, call us at 800-468-DISC, or 408-438-6550.

And to our customers, we offer a couple of choice words of our own: Thank you.

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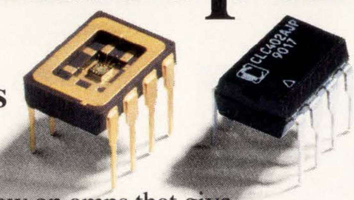

14-bit, 25ns settling keeps up with fast converters.

Here are two new op amps that give you big design margins on fast, high-resolution A/D and D/A converters. The new 175MHz CLC402 and 150MHz CLC502 have extremely fast settling to 0.0025% accuracy. Plus a low 1.6mV max. offset. And, the CLC502 gives you output voltage clamping to protect downstream circuits from damaging or saturating signals. That's a lot of good news for your high-speed, high-accuracy converter designs.

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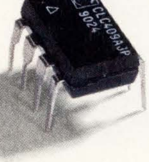

350MHz BW with low distortion drives flash A/Ds.

At last, there's a wide-bandwidth op amp with extremely low distortion for your flash A/D converters. The new 350MHz CLC409 is spec'd at a low -65/-72dBc, 2nd/3rd harmonic distortion (20MHz, 100 ohms, $2V_{p\text{-}p}$). And it does it without burning much power. Dissipation is a low 142mW at ±5V. Add to that its low input noise and you have an ideal driver for today's fast 6- to 10-bit flash A/D converters.

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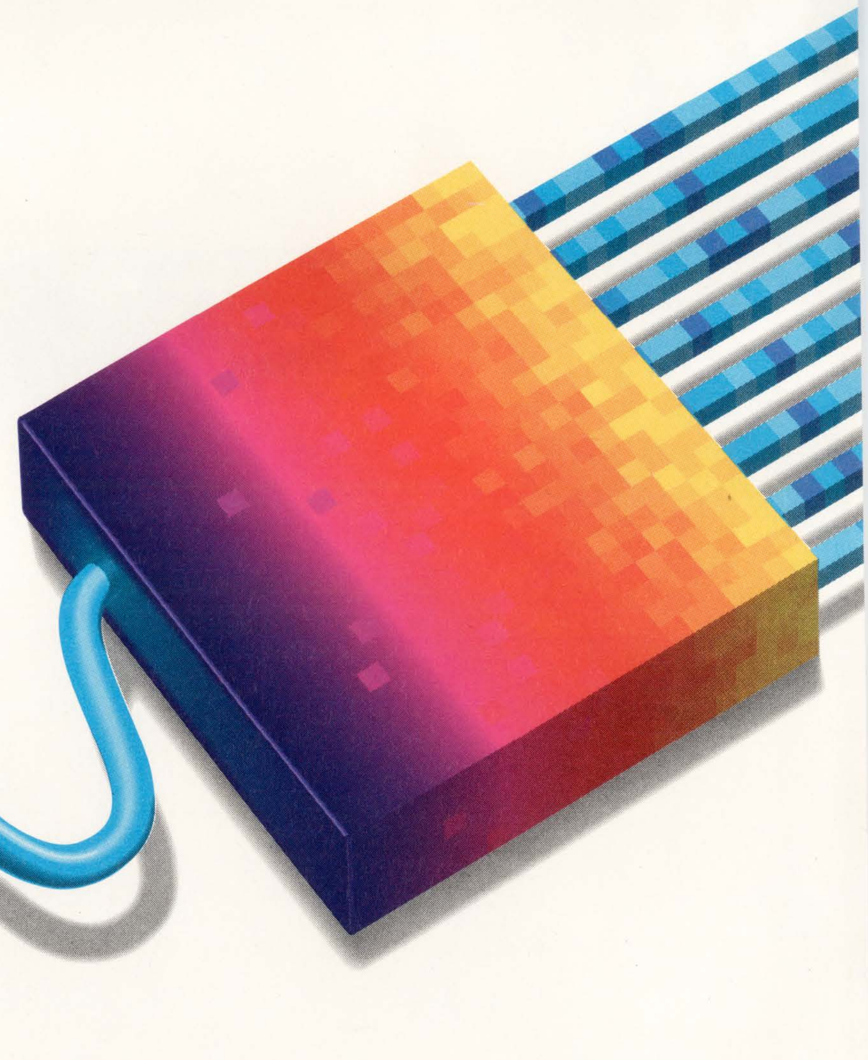

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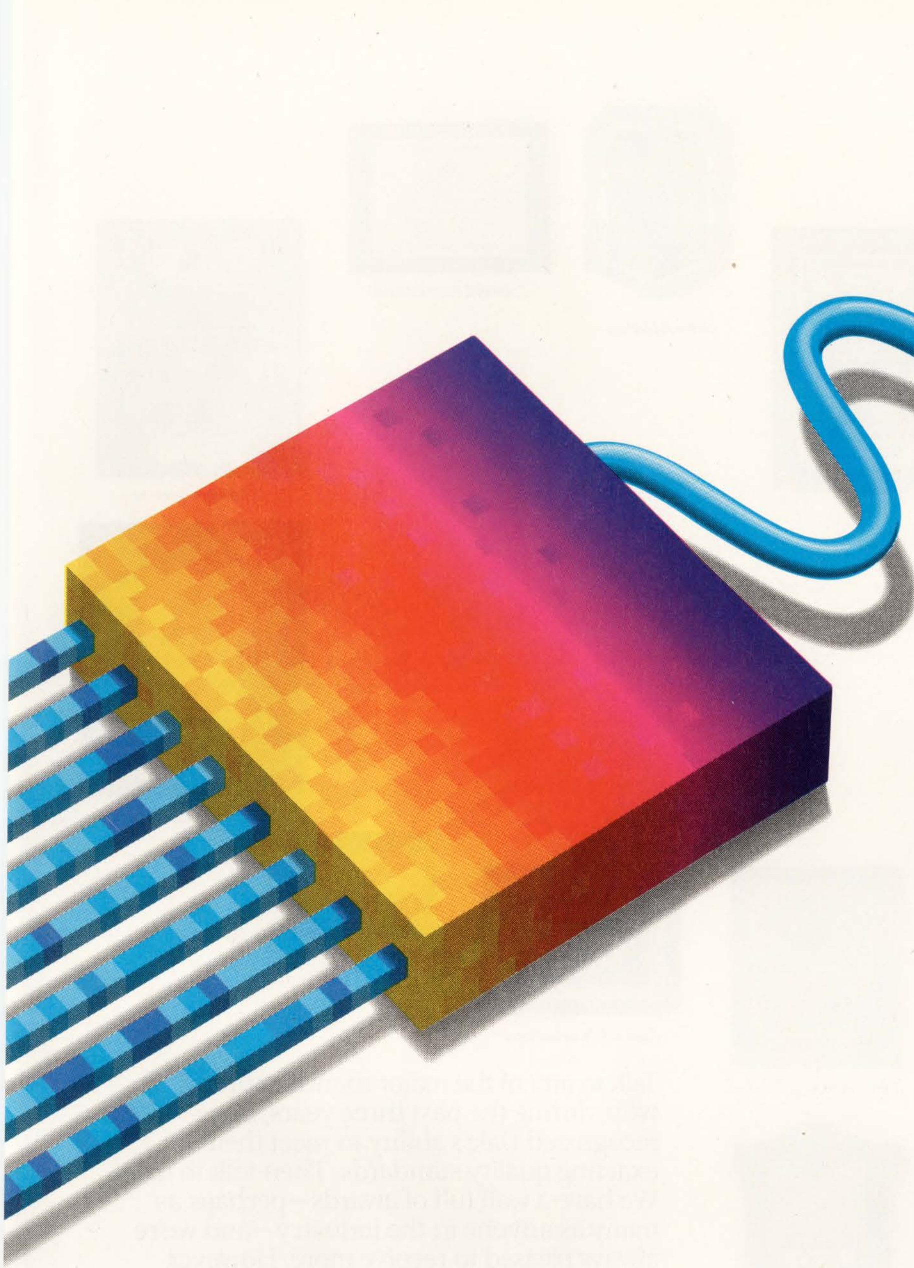

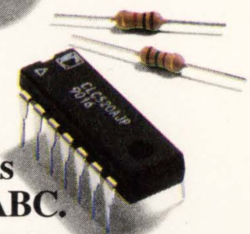

Now, high-speed AGC is easier than ABC.

Take the new CLC520, add ±5V and two resistors, and you have a total high-speed AGC solution for fast converter applications. 160MHz small-signal and 100MHz gain-control bandwidth—with a 40dB range from max. gain—give you a very flexible solution in a single 14-pin DIP.

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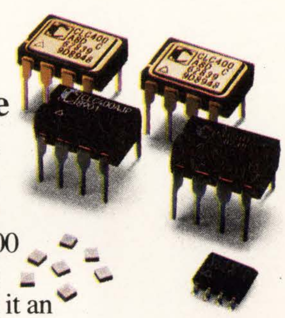

High performance at low gains.

Optimized for a gain of +2, the 200MHz CLC400 has 10ns settling to 0.1%, making it an ideal data converter driver. Its excellent gain flatness makes it great for video applications too. And it's priced at just $5.95* (1000s).

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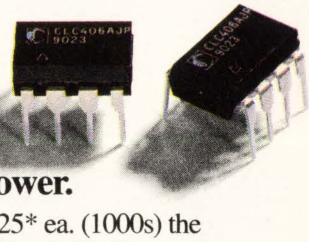

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For only $4.25* ea. (1000s) the CLC406 provides 160MHz small-signal bandwidth ($2V_{p-p}$) at only 50mW power dissipation (±5V). It's your low-cost answer for remote-site applications, video systems, or driving/buffering fast data converters.

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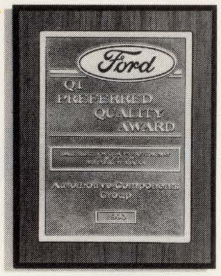

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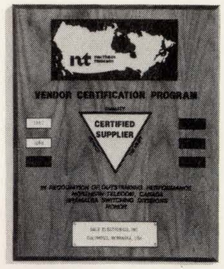
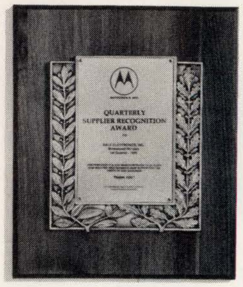


Northern Telecom



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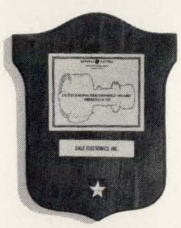

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CIRCLE NO. 161

Don't count TTL out yet

Jon Titus's ringing of the death knell for TTL (EDN, October 25, 1990, pg 53) is both premature and unfair. Premature, because there are still people out there who design with TTL and CMOS. (Why wasn't this family included in the eulogy?) Unfair, because not everyone reading EDN can be state of the art.

Many companies are just not financially situated to jump into programmable logic. Or maybe they just don't need the sophisticated functions made possible by PLDs and FPGAs. Jon states that "computer circuit boards today are teeming with PLDs." That is undeniable; however, not everybody is at the leading edge of building computers.

I took some comfort in the header, "Editorial" at the beginning of Jon's comments. This header implies opinion, and opinions vary. For example, I recently read an article that referred to the 8051 as "venerable," implying "past its prime." However, another stated that 8-bit microcontrollers such as the 8051 are very much in demand and will be in new designs well past the year 2000. I'm certainly glad to hear that; my company is just announcing the second generation of a product that uses a venerable 8051. What is it? An in-circuit tester for the very TTL (and CMOS) devices that Jon claims is at death's door.

Gerry Volk
Technical Writer
B&K Precision Test Instruments
Chicago, IL

Comparing execution efficiency of Ada vs C

As a proficient Ada programmer, I read Charles Small's excellent article "Adopting Ada is first step to code reuse" (EDN, August 20, 1990, pg 71) with great interest. As a proficient C programmer, however, I found the article to be flawed with respect to its view of programming C. In the box, "Ada features promote code reuse," Charles states: ". . . A C library, for example, would need separate versions of a ring-buffer library routine to handle characters, fixed-point numbers, and floating-point numbers. Ada could handle any of these data types with a single ring-buffer generic."

This statement is patently false. In terms of pure execution efficiency, C is actually superior to Ada in that a ring-buffer software library (to follow the given example) could be (and has been) created in C. C would use the same code to manipulate all three types, as well as any other types the programmer cared to use.

By way of contrast, Ada's generic facility creates a template that will most likely be implemented in such a way that the entire set of routines is copied for the new data type rather than being reused. The C code is thus more reusable than the corresponding Ada code.

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If you would welcome a follow-up phone call by an EDN editor, please give your name and phone number. This information will not be shared with anyone else.

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This is actually an implementation issue rather than a language issue. One can visualize an Ada "macro" compiler that would create code as efficient in terms of both space and time as C's, or possibly a little better. Consider, for example, that subroutines imported in the instantiation

```
generic
    type ITEM_TYPE is private;
    with function "<" (LEFT,RIGHT :
        in ITEM_TYPE) return BOOLEAN;
package . . .
```

could be known to be in-line, via a pragma, at compile time, obviating an external call. This is not unique to Ada, however. C++ also implements an in-line mechanism known as compile time.

The advantage (if you choose to call it one) that Ada offers is that when instantiated (an ugly, sanctimonious word), the routines are tied to a specific data type in an unambiguous way, preventing unintentional or malicious abuse of the routines within the scope of the fleshed-out generic. (As always, what the programmer does outside the scope of the generic is quite another matter.)

James B Crigler
Orlando, FL

(Ed Note: Certainly you can write an all-purpose routine that will handle any conceivable type of input. Such a routine will, I think, inevitably be larger, slower, and more complex than one written or "instantiated" to handle just one type of input.

I've used a programming construct similar to the generic, and I've found that its use led to cleaner code and clearer concepts than writing individual versions of similar routines.

Using any particular language does not guarantee good programs. Small's "Second Law of Programming" states that you can write a bad program in any language.)

Usable used equipment lets him continue working

I was interested in Jon Titus's editorial, "Praise the PC and pass the Windows" (EDN, October 11, 1990, pg 49) because it relates to the matter I need help with. Like all Americans, I'm concerned about the economy, maybe even more so, because I'm disabled with multiple sclerosis. I'm an independent volunteer with Civil Defense, American Red Cross, United Way, Bright Hope Foundation, National Multiple Sclerosis Society, and several other organizations.

My area of expertise is communications and computers. Because I'm not paid, I must rely on the generosity of companies that are willing to contribute the used equipment I need to continue doing this volunteer work. I don't need "new" equipment—just equipment that's complete and operational—or that can be easily repaired. The following equipment would help me do a variety of jobs, such as upkeep of databases, word processing, number crunching, and other informational services:

- A 20M-byte and 100M-byte or higher or a 120M-byte disk
- Color VGA or EGA monitor and card
- Full-page or hand scanner
- Laser printer and accessories
- Sola electric copier
- Tape backup system (100M byte)
- Laptop computer
- Fax machine
- LAN equipment
- Burr-Brown plotter and accessories
- High-speed modem (2400 baud up)
- Macintosh computer and software
- Computers as workstations on a LAN
- Old computer equipment for parts.

Intel, US Robotics, Miniscribe, Western Digital, Hercules, and Borland are companies that have already helped me. I'll be glad to answer any questions you may have. You can reach me after 12:00 CST at (601) 684-9550, or you can write to me.

John T Statham
1506 Sheila Dr
McComb, MS 39648

Corrections and new address

The caption for the photo at the bottom of page 55 (EDN, December 20, 1990) discusses the VHDL textual output of a software tool. In the last sentence, "VHDL" is used without "the," creating the impression that VHDL isn't yet suitable for logic synthesis. VHDL *is* suitable for logic synthesis, but this particular tool's VHDL output is not. The last sentence should read: "Unfortunately, the VHDL isn't yet suitable for logic synthesis."

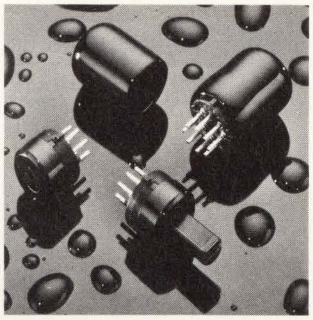
The photo at the bottom of page 57 is a screen shot of Mentor Graphic's Design Consultant, not of Synopsys' VHDL Compiler, as the caption suggests.

CAD Language Systems Inc, listed in the Manufacturers List (pg 58), has a new address:
15245 Shady Grove Rd
Suite 310
Rockville, MD 20850
(301) 963-5200
FAX (301) 963-1511

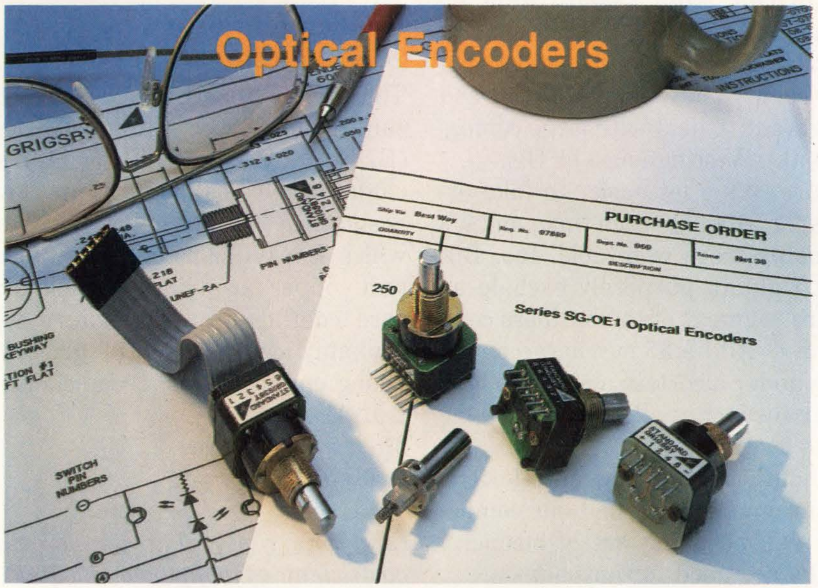
Problems of ordering parts for small companies

As president of a small electronics company, I face many obstacles. The biggest one nowadays seems to be distributors' lack of willingness to sell small quantities of parts to companies like mine. We don't buy vast quantities of parts, but our projects do require us to buy parts and to receive them in a reasonable period of time. We've been finding that most of the distributors have started adding not just minimum

Gold Terminals Extend TO-5 Switch Life. Gold-plated terminals, handling resistive loads of 500 mA/125 VAC, extend the life of Standard Grigsby's TO-5 rotary switch to an 5000 cycles (typ.). These compact switches mount easily into standard TO-5 transistor sockets or PC boards for wave soldering. Screwdriver or knob actuation available. 45° throw with 8 positions max. Positive detent switching action is standard. Contact pin surface is sealed and an optional boot is available to seal the shaft. Price: $1.39 in 10,000-piece lots. Delivery: 4 weeks. Contact Standard Grigsby, Inc., 88 N. Dugan Rd., Sugar Grove, IL 60554-0890. 708/556-4200 FAX 708/556-4216.



CIRCLE NO. 162



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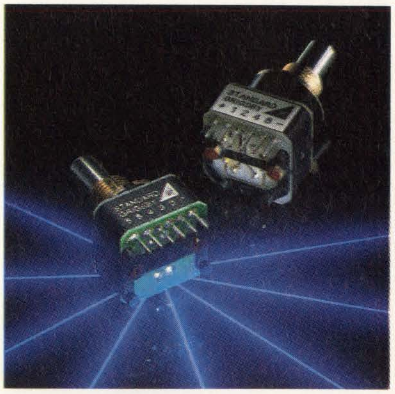
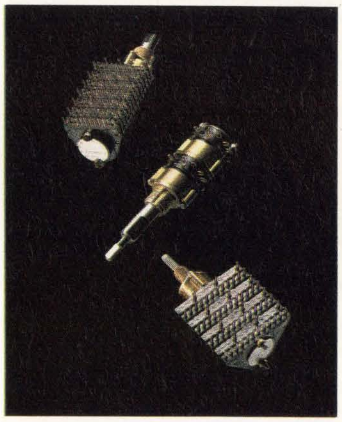


Choose Binary Or Gray Coded. Sugar Grove, IL—Binary and Gray coded optical encoders are available from Standard Grigsby, Inc. Ideal for use in robotics, medical instrumentation, communications, computer peripherals and avionics, the 16-position encoder is available with integral cable or connector. Users may specify custom shaft lengths and diameters.

Priced at $29.10 each in 100-piece lots, the encoders are available in 6 weeks. Standard Grigsby, Inc., 88 N. Dugan Road, Sugar Grove, Illinois 60554-0890. 708/556-4200 FAX 708/556-4216.

CIRCLE NO. 164



Multi-deck, Multi-options. Sugar Grove, IL—Standard Grigsby's multi-deck rotary switches offer reliability and long life, and retrofit other manufacturers. Measuring approximately 1/2" in diameter, the switches are available with PC or solder lug terminations, fixed or adjustable stops; 30° or 36° indexing angles; commercial or military finishes.

Priced at $4.50 each in lots of 500, the switches are available in 6 to 8 weeks. For more information, contact Standard Grigsby, Inc., 88 N. Dugan Road, Sugar Grove, IL 60554-0890. 708/556-4200 FAX 708/556-4216.

CIRCLE NO. 165

SIGNALS & NOISE

orders, but excessive minimum orders. We've seen the minimum orders go from $0 to $25 to $50, and now some companies require minimum orders of $200.

In addition to this, some distributors have a minimum line order of $25 or $50, or even as high as $200. The purpose of a distributor, at least in the past, was to buy parts from the manufacturers in large quantities and resell them in smaller quantities to the general population. Most of these distributors seem to have forgotten this and only want to deal with large companies like Westinghouse or GE.

Sure, it's a lot easier to take orders for $100,000 each time, and it's probably more profitable, too. But is it right to purposely exclude an entire segment of the business community? Add a $5 surcharge on orders under a certain amount to help cover costs. But allow us to buy the parts that we need for our designs. Without these parts, our designs cannot go forward, and our companies will be going out of business. That's not good for anyone.

When we place orders with these companies, something invariably gets confused at the distributor's end. We request that an in-stock item be delivered a week from the order date, but the week comes and goes, and the part has not arrived. We check back with the distributor, and lo and behold, the part has never been shipped. This is not an isolated incident, but occurs close to 80 or 90% of the times we order parts from places like Hamilton/Avnet, Arrow, and Marshall. For the past year, we have tried and tried to get proper service and respect from the parts distributors; we spend about $3000 a year on parts.

The only parts distributor that gives us good service is Digi-Key in Thief River Falls, MN. They have everything we've ever ordered in stock, have shipped when they say it's going to be shipped, all at an acceptable cost. If there are any other "Digi-Keys" out there, please let me know because we will start buying parts from you, too, and I will spread the word among the small-business community.

Scott B Rosenthal
Microsol Corp
6851 Oak Hall Lane, Suite 201
Columbia, MD 21045

Reader fears for young engineers, et al

The article "Thermal charging circuits safely boost NiCd batteries" (EDN, May 24, 1990, pg 147) includes a box called "Create low-resistance shunts with wire" in which Jim Williams fails to mention that copper has a horrible temperature coefficient. This failure will probably cause a lot of grief for young engineers and technicians.

L R Morse
Martin Marietta
Orlando, FL

(Author's reply: The temperature coefficient of copper is 0.39%/°C. Over an operating range of 30°C ± 40°C (reasonably generous for NiCd), the battery charge current variation will be about 16% due to shunt valve shift. This seems reasonable considering the other variables involved. Additionally, what variation there is contributes a negative slope to the charging current vs temperature and is perhaps useful. So, while I don't recommend copper shunts for DVM reference circuitry, they seem adequate for NiCd charging purposes. I hope this clears up any confusion.)

It's time for a new declaration of independence

I've observed the events in Iraq and Kuwait with great concern. The leader of the Iraqi government, one of the most vicious modern terrorists, is convinced he can get away with his invasion because of the in-

HMI development systems do it all!

HMI provides complete development systems—in-circuit emulator, window driven source level debugger and software performance analyzer—that address all aspects of the microprocessor system design cycle, from prototype to production:

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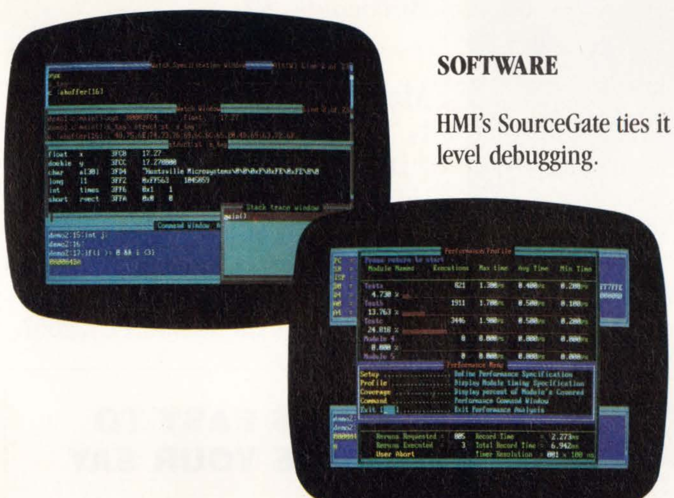

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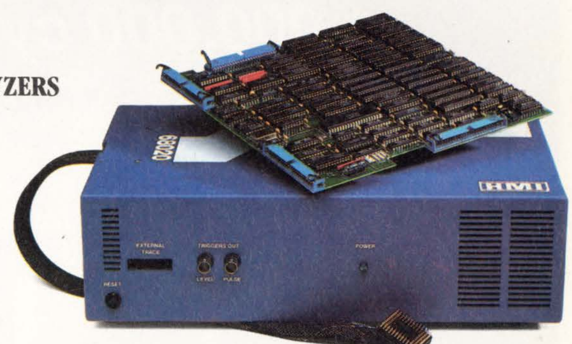

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Performance Analysis Features:

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68008	68332	DS5000
68010	68340	8096/80196 Family
68020	6809/6809E	8085
68030	68HC11 including F1 and D3	64180/Z180
	68HC001	Z80

HMI

CIRCLE NO. 92

satiable American craving for oil. And he knows we are loathe to give up this craving, seeing that we have learned nothing from the gas lines of the early '70s.

Even though the US makes up less than 20% of the global population, we consume 40% of the world's gasoline. Figures published by the Environmental Defense Fund indicate that the Germans and Japanese use half as much energy per capita as Americans do.

Something is also wrong with the way the US wastes talent and energy. Let us encourage the thousands of first-rate, but unemployed, engineers across the country to join forces in developing cheaper, efficient, mass-producible solar cars, mass transportation, and heating panels. I think taxpayers would be more inclined to pay for this effort than to bail out corrupt bankers.

If we do not eliminate our crippling dependence on oil, the alternatives are continued air pollution, more price gouging from our own companies, more disastrous oil spills, and even more vulnerability to terrorist dictators in the Middle East who have us right where it hurts.

Is there really any choice? Ask an engineer!

Russ Hodge
Portsmouth, RI

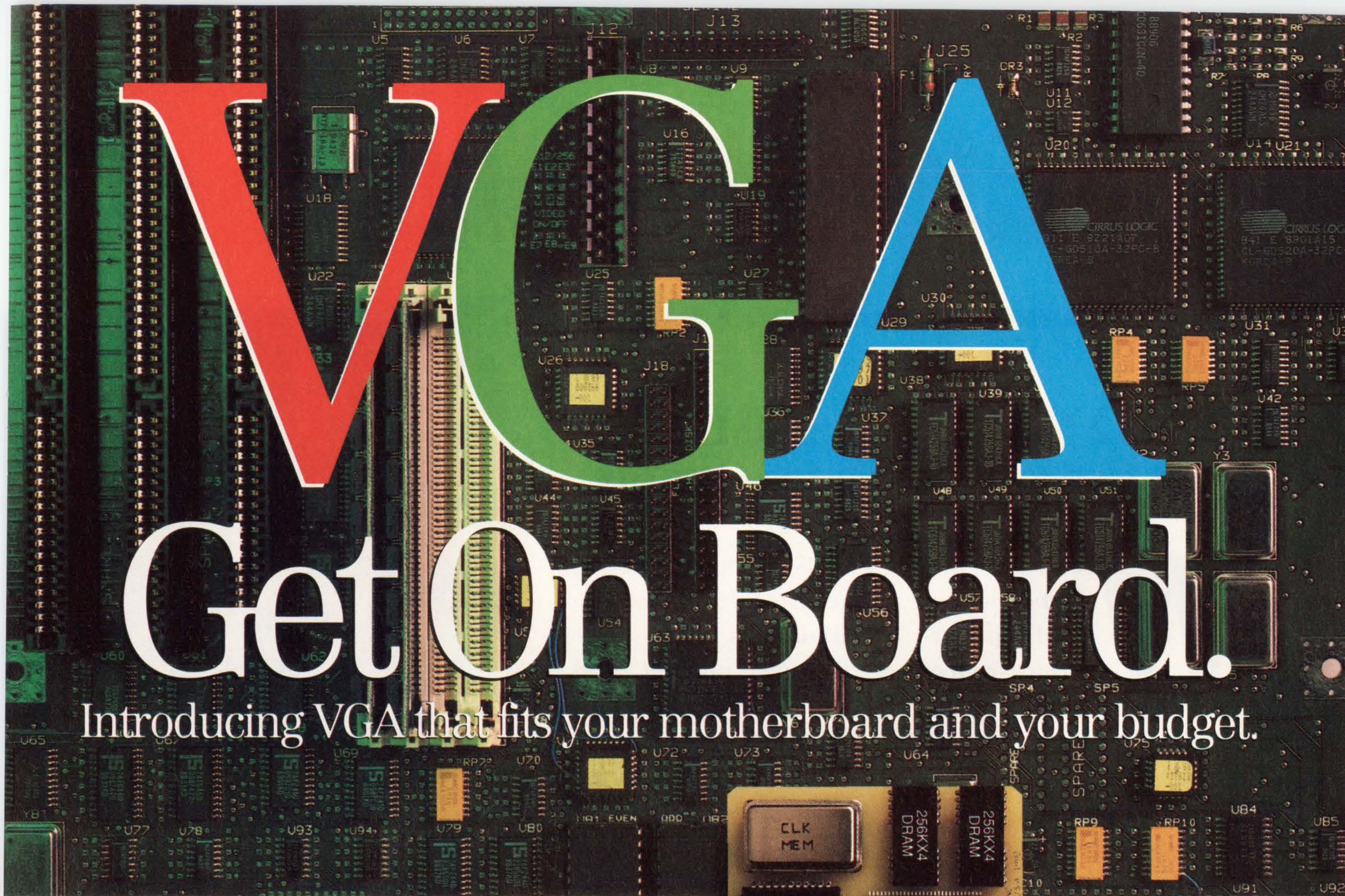
Mea culpa

In the October 11, 1990, issue of EDN, pg 261, we unfortunately called Spectronics Corp's UV eraser, a μV eraser. We regret the error. You can contact Spectronics at (516) 333-4840 for further information about the Model PC-2200A.

IT'S EASY TO HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps or less modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 2400, 8N1 in shorthand.

EDN



To put VGA graphics on your motherboard, you need a cost-efficient, highly integrated, powerful solution that uses minimal board space. You need the new CL-GD5320 Enhanced VGA-Compatible Graphics Chip from Cirrus Logic.

Use it to incorporate full 16-bit or 8-bit VGA into low-cost personal computers. You only need two industry standard 256K x 4 DRAMs and as few as five other ICs. Whatever memory speed you select — 80ns, 100ns, or 120ns — you'll get a complete VGA display system with greater performance than systems using a more expensive solution with 64K x 4 DRAMs.

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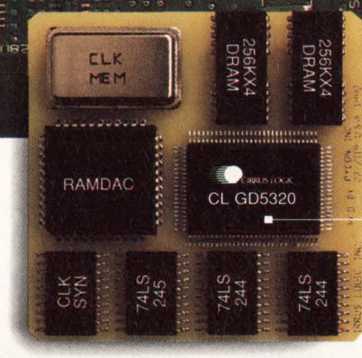

This full 16-bit CL-GD5320 lets you implement 16-bit or 8-bit VGA capabilities on your motherboard with as few as 5 other chips and two 256K x 4 DRAMs. Get a complete solution that saves time, space, power, and expense. You still get all the speed, features and flexibility you're looking for.

You can also pick a ready-to-use solution that's right for you. Anything from a chip with full BIOS, drivers, utilities, user's manual, and documentation — to a complete manufacturing kit including everything you need to quickly move into high-volume production.

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For many other PC, workstation, printer, and computer-related companies, Oki is simply "the preferred SIMM supplier." Our modules are favored for their superior quality levels. For their low power features and variety of configurations and heights. And for their range of packaging options—such as our ultrathin TSOP for memory cards. Plus our new manufacturing facility in Tualatin, Oregon supports fast, full custom SIMM capabilities.

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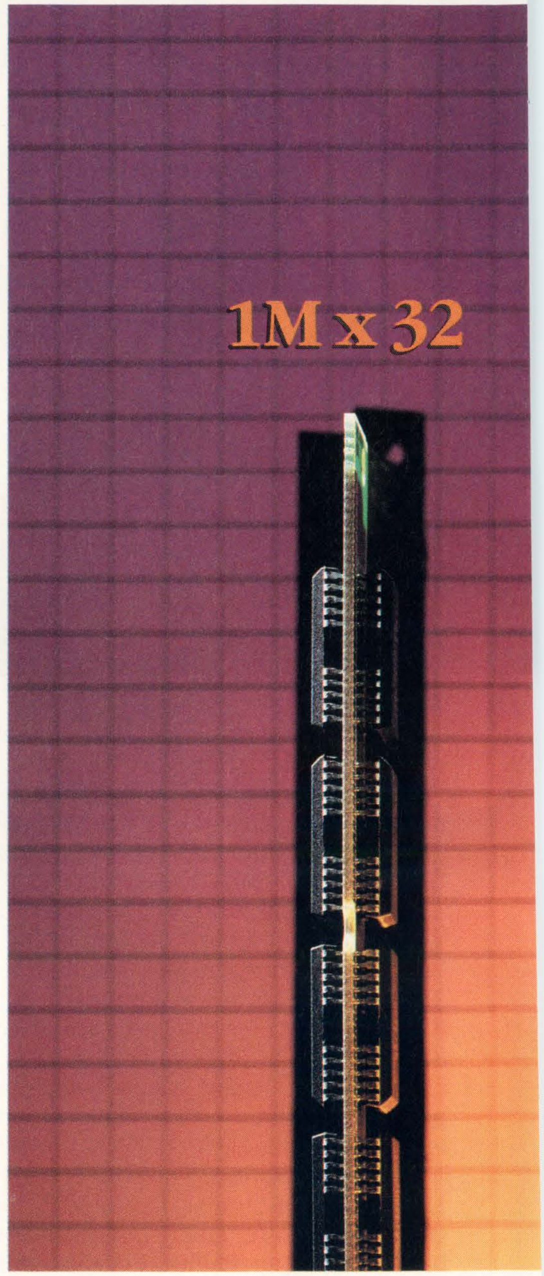

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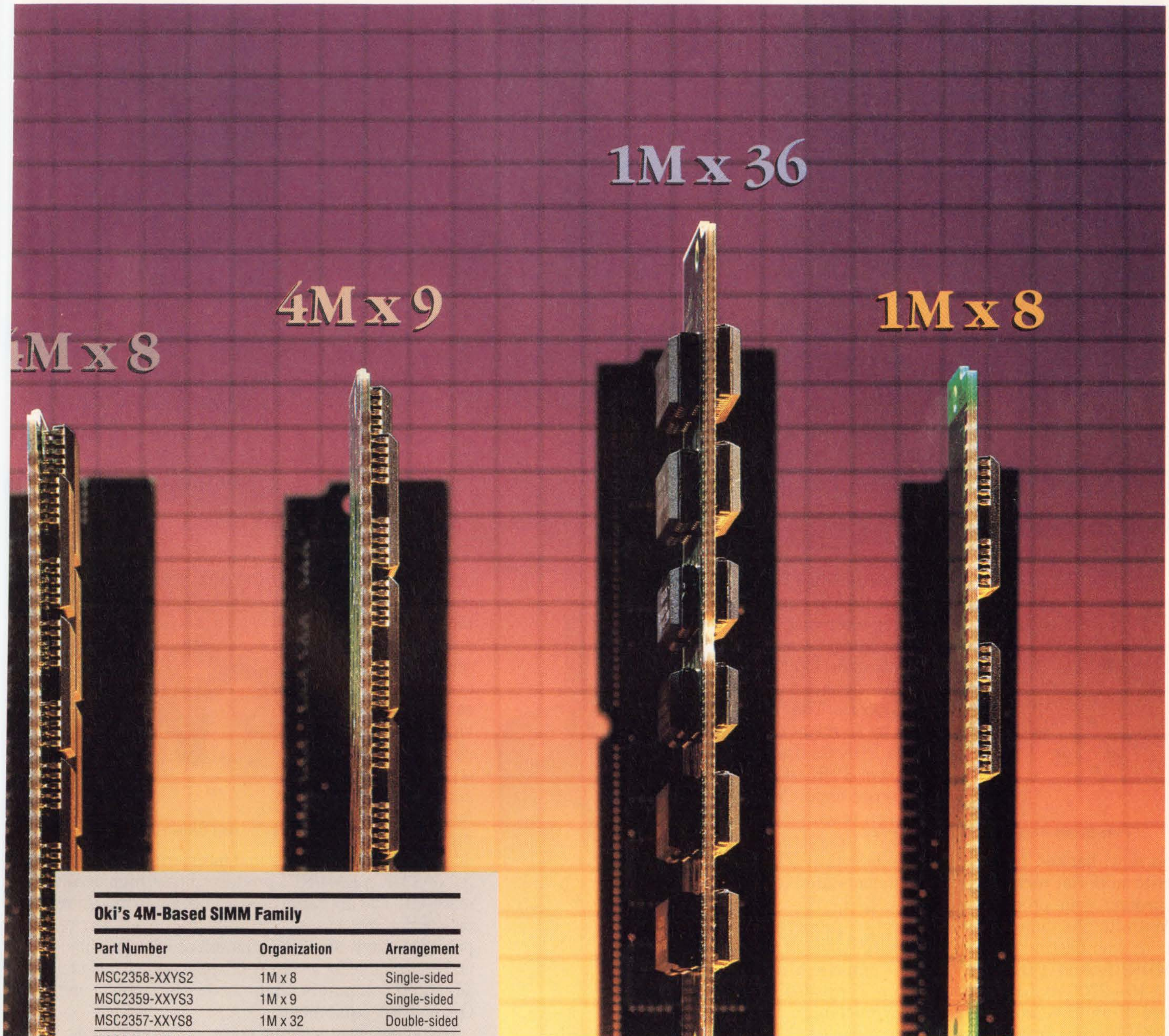

Oki's 4M-Based SIMM Family

Part Number	Organization	Arrangement
MSC2358-XXYS2	1M x 8	Single-sided
MSC2359-XXYS3	1M x 9	Single-sided
MSC2357-XXYS8	1M x 32	Double-sided
MSC2361-XXYS8	1M x 32	Single-sided
MSC2355-XXYS12	1M x 36	Double-sided
MSC2360-XXYS12	1M x 36	Single-sided
MSC2353A-80YS10	1M x 40	Single-sided
MSC2362-XXYS16	2M x 32	Double-sided
MSC2356-XXYS24	2M x 36	Double-sided
MSC2352A-80YS20	2M x 40	Double-sided
MSC2341-XXYS8	4M x 8	Single-sided
MSC2340-XXYS9	4M x 9	Single-sided

All the above listed SIMMs operate in fast page mode.
Speed options (XX) include:
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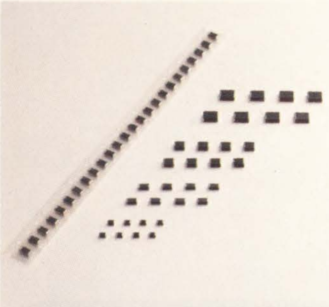
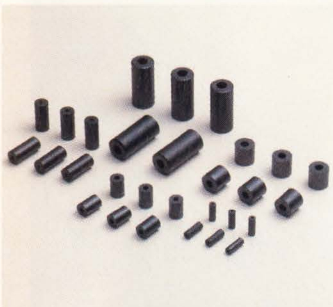
80 = 80ns (^{t}RAC) 20ns (^{t}CAC)

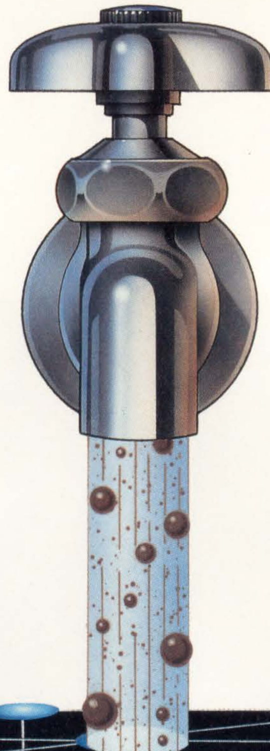
OKI
Semiconductor

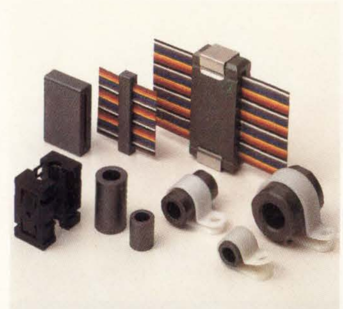
785 North Mary Avenue
Sunnyvale, CA 94086-2909

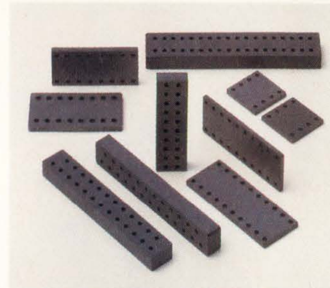
CIRCLE NO. 89


Ferrite Chip EMI Suppressors, ACB Series

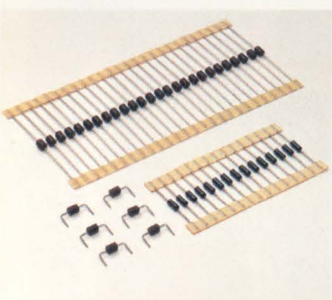

Ferrite Bead Cores, BB Series




Ferrite EMI Suppressors for cables


EMI Suppression Multi-hole Substrates for ICs and Connectors

TDK Ferrite Technology Blocks out EMI/RFI


Ferrite Beads Axial-lead taped type

Ferrite Core for EMI/RFI:
For electronic equipment electromagnetic interference is a major concern. That's why so many turn to TDK for assistance. TDK, the ferrite expert has been researching EMI for years. And now, backed by the full complement of TDK ferrite material technology, our products are ready to protect your products from EMI/RFI.

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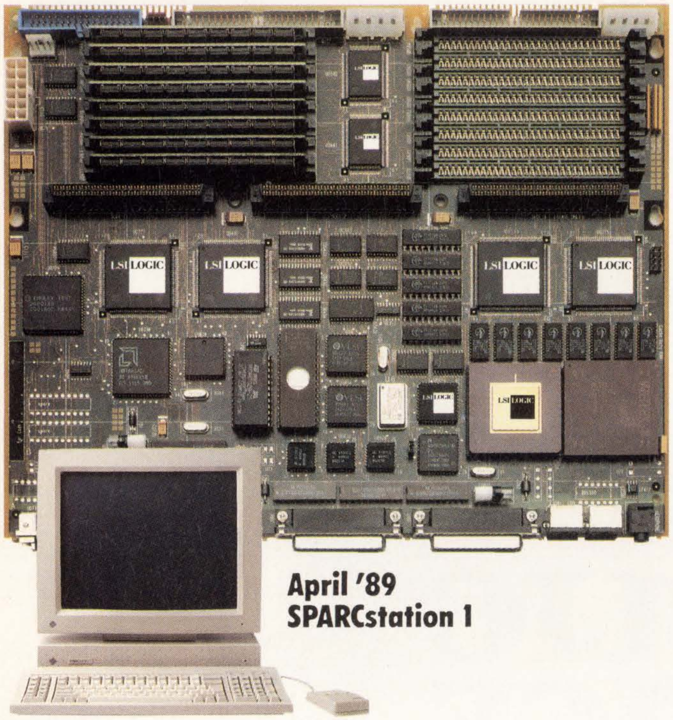
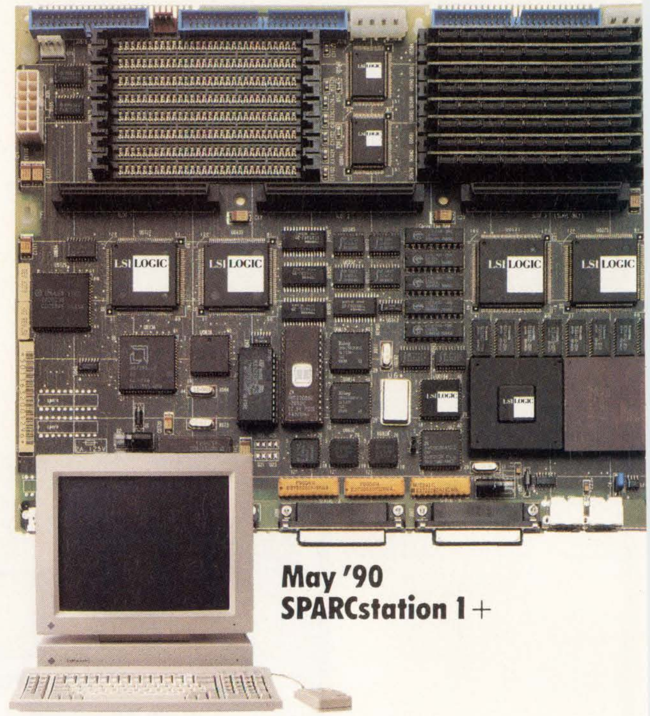
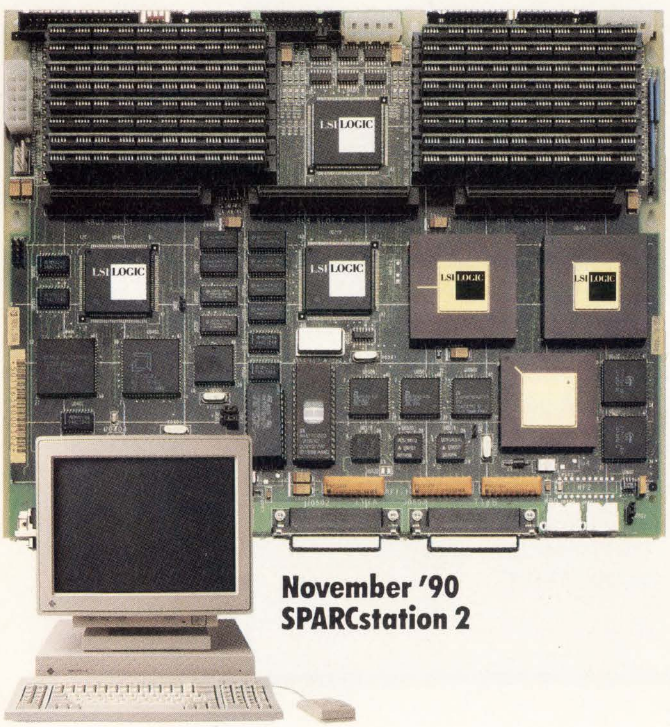


April '89
SPARCstation 1

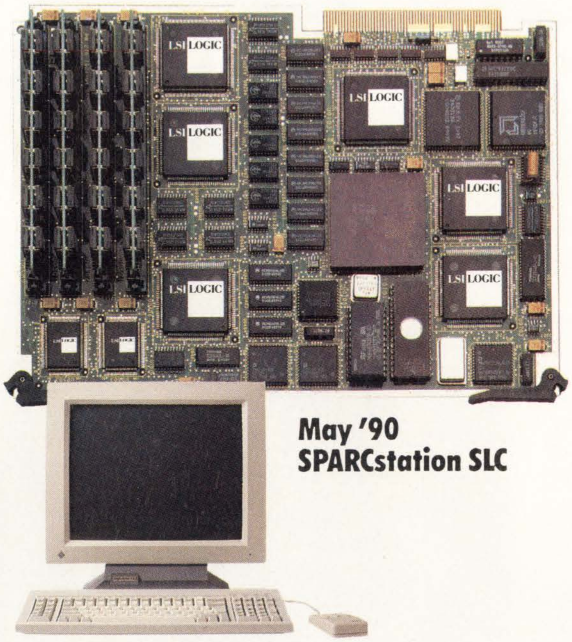


May '90
SPARCstation 1+

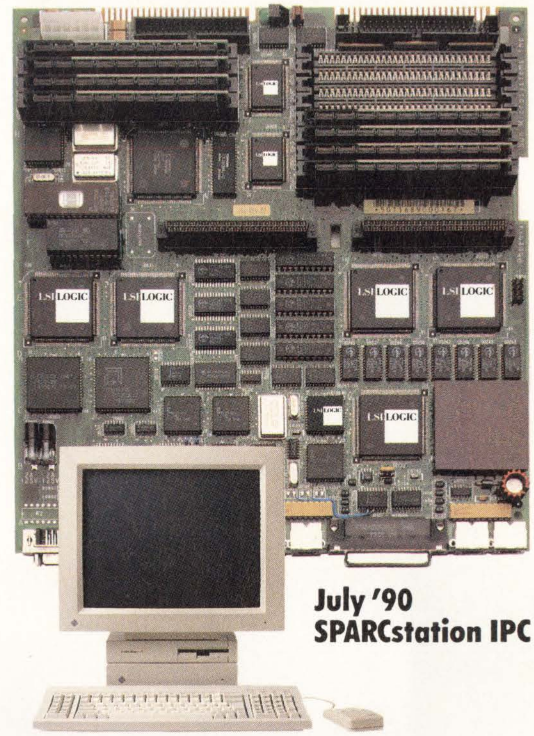


November '90
SPARCstation 2

LSI HA ANOTH



May '90
SPARCstation SLC



July '90
SPARCstation IPC

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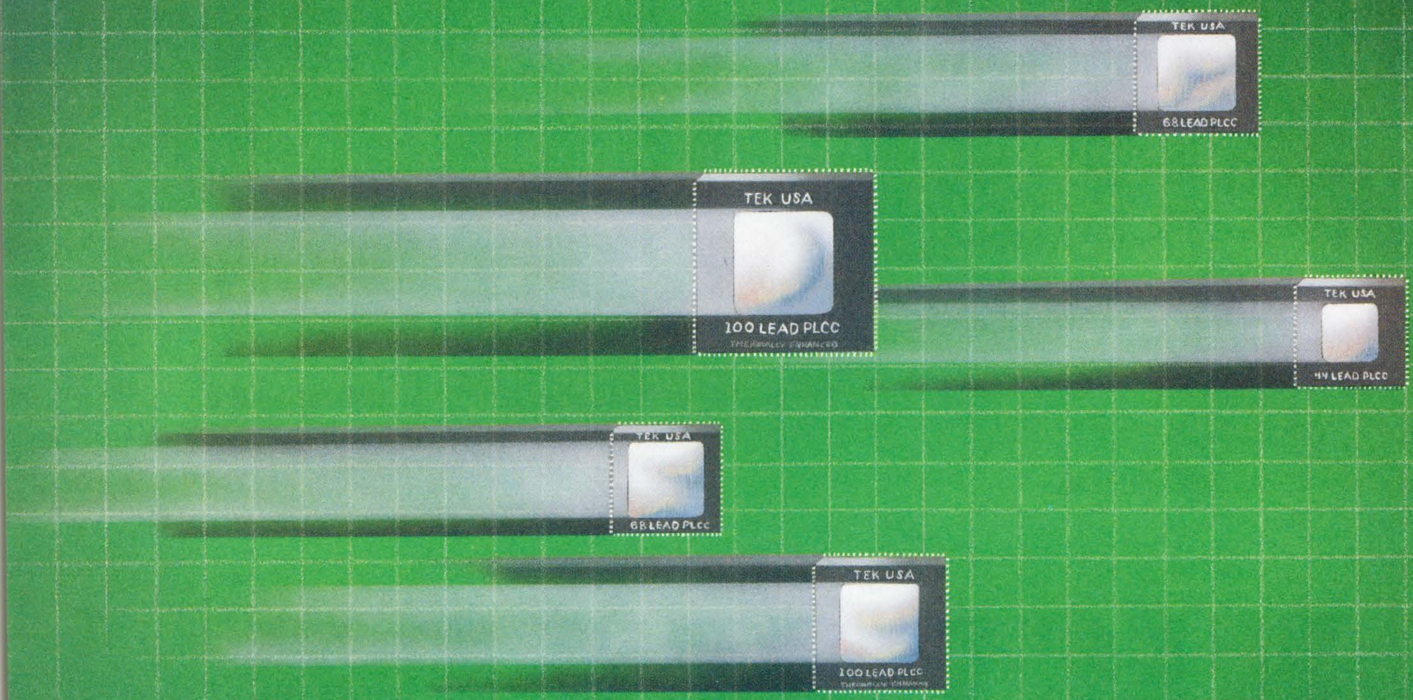
ACROSS THE BOARD

CIRCLE NO. 84

When Time Is Money ...

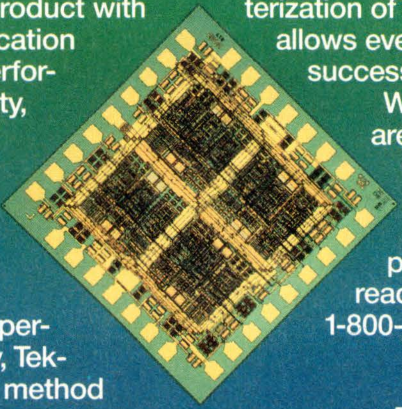
Tektronix QuickCustom™ ASICs



Tektronix' QuickCustom ASICs make it easy for you to create your own analog designs fast. And error free.

Our high speed QuickCustom family of bipolar products, together with Tek's QuickCustom design system, help ensure that your design works right the first time, reducing development time and cutting costs.

◆ Tektronix QuickChips™ help you move from concept to finished product with minimum design and fabrication time. ◆ For even higher performance and greater flexibility, the Tektronix QuickTile™ design method offers standard building blocks for fast implementation of analog and mixed signal functions. ◆ And finally for optimum performance and functionality, Tektronix' Full Custom design method is also available.



All three QuickCustom products provide convenient access to our high performance bipolar process (f_T = 8.5 GHz and $LV_{CEO} \geq 8$ V) with Schottky diodes, JFETs, NiCr resistors, and PNPs. Typical applications include high speed data converters, L-Band amplifiers and mixers, and low noise transducer amplifiers. Our advanced QuickCustom design system, which includes complete CAD tools, thorough characterization of all devices, and support, allows even the first time user to successfully complete the design.

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CIRCLE NO. 87

ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

Have you been stumped by a design problem for so long that you don't know who to turn to? Are you having trouble locating parts? Finding companies? Can't interpret a spec sheet? Ask EDN.

This department will serve as a forum to solve nagging problems and answer difficult questions. EDN's editors will provide the solutions. If we can't solve a problem, we'll find an expert who can, or we'll print your letter and ask your peers for help. We can't answer every question, but we'll try to publish the ones that will help you most in your job.

Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or, send us a letter on EDN's bulletin-board system. You can reach us at (617) 558-4241 and leave a letter in the /ask_edn Special Interest Group.

More missing parts

I would like to ask a question to which I have still not found an answer. My company is searching for a special National Semiconductor microprocessor called the TMP with part ID NS405-A12. Unfortunately, the part is no longer in production, but we need a batch of 30 to 50 working units to solve a tricky service situation. We would appreciate your help in this matter.
Christer Berg
Technical Director
BEON Data AB
Sollentuna, Sweden

If any reader knows of a source of these parts, please contact Ask EDN.

Reader offers advice

In the October 1, 1990, issue of EDN, David Fors of the Naval Weapons Center in China Lake, CA, requested a vendor for an IRIG/B converter. I would suggest he try sending out an urgent data request through the Government Industries Data Exchange Program (GIDEP). Most large companies, including military IC manufacturers, have a GIDEP representative.
Mark Monroe
Grumman Corp
Bethpage, NY

Desperate for debounce circuit

I am desperate for a debounce circuit that will work from an existing pushbutton switch circuit and will be electrically resettable after time-out, preferably without a clock.
Gary Lawrenson
President
Lawrence Electronics Co
Seattle, WA

EDN Editor Jon Titus and Senior Editor Charles H Small reply: "The problem logic designers have with mechanical switches is that the switches emit a series of pulses every time you change their state. This phenomenon, called switch bounce, is inherent in the springy mechanical parts of the switch.

To debounce a switch, you can take one of two tacks: filtering out the switch bounce as though it were high-frequency noise or inserting a latch in your switch-sensing path that will recognize only the first pulse from a bouncing switch.

Consult these standard reference works for debounce circuits: *The 555 Timer Applications Sourcebook*, by Howard M Berlin; and *The 555 Timer Cookbook* and *The IC Timer Cookbook*, both by Walter G Jung. All three books are published by Howard W Sams & Co, Indianapolis, IN 40206. National Semiconductor has excellent application notes that can also help.

Database is defunct

I can't locate Videolog Communications (Norwalk, CT)—they aren't at their published phone number. The company offered Videolog, a database of information on more than 500,000 semiconductors. Can you find out what happened to them?
Dave Kukuk
Telecommunications Technology
Milpitas, CA

Videolog Communications was acquired by Schweber in 1986 or 1987, says Special Projects Editor Gary Legg. Schweber renamed the Videolog information service, but it never really took off. Cahners CAPS, a CD-ROM-based database, provides the same information retrieval capabilities that Videolog did, plus many more. In fact, Schweber is now a CAPS customer. CAPS resides on your workstation or PC, whereas Videolog was accessed via modem. For more information on CAPS, contact

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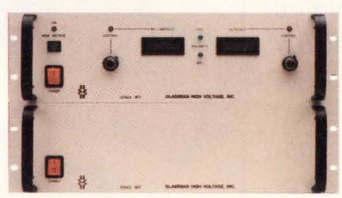

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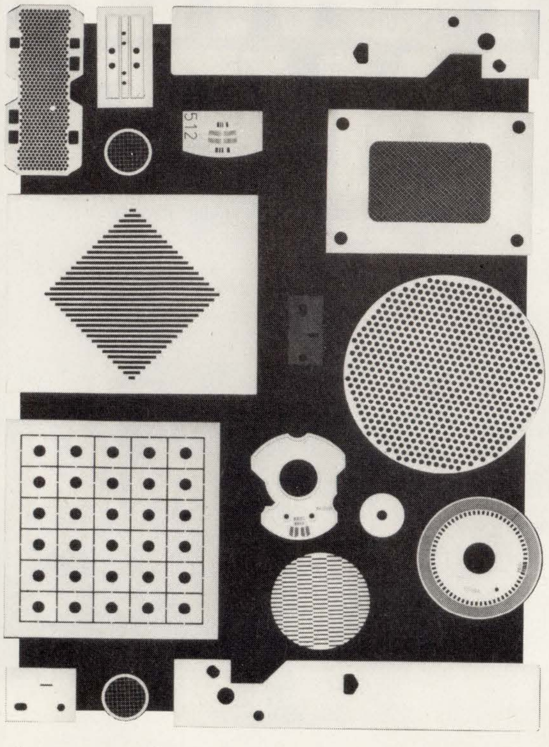

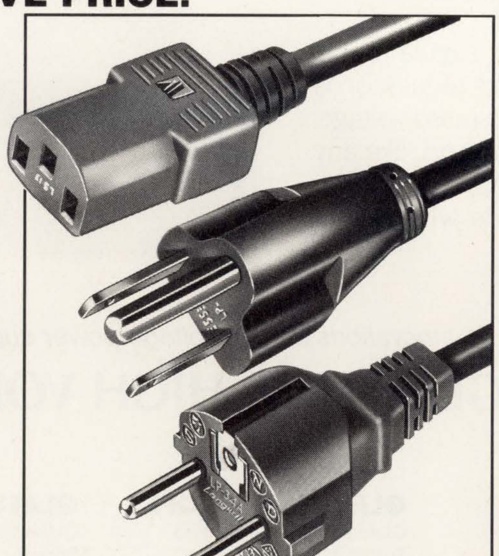

CALENDAR

1991 Mathematica Conference, San Francisco, CA. Maury Kendall, Wolfram Research Inc, 100 Trade Center Dr, Champaign, IL 61820. (217) 398-0700. FAX (217) 398-0747. January 12 to 15.

Managing Concurrent Engineering, Los Angeles, CA. Joan Hill, USC School of Business Administration, Los Angeles, CA 90089. (213) 740-6411; (213) 740-5219. January 13 to 15.

Applications of Unix Utilities (short course), Seattle, WA. Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155. (206) 527-3385. FAX (206) 527-2806. January 15.

VXIbus User Group Meeting, Anaheim, CA. Sandy Garza, National Instruments, 6504 Bridge Point Pkwy, Austin, TX 78730. (800) 433-3488. (512) 794-5435. FAX (512) 794-5569. January 17.

Information Services Seminar (ISS), Newport Beach, CA. Terry Burke, SEMI Membership Services, 805 E Middlefield Rd, Mountain View, CA 94043. (415) 940-6901. January 21 to 23.

Winter 1991 UNIX Technical Conference, Dallas, TX. Usenix Association, 22672 Lambert St, Suite 613, El Toro, CA 92630. (714) 588-8649. FAX (714) 588-9706. January 21 to 25.

1991 Reliability and Maintainability Symposium and Exhibits, Orlando, FL. F Peter, Dayton T Brown Inc, Church St, Bohemia, NY 11716. (516) 589-6204. January 29 to 31.

Learn Test In The 1990s (short course series), Silicon Valley, CA. ATE Solutions Inc, 2820 Townsgate Rd, Suite 202, Westlake Village, CA 91361. (805) 373-1477. FAX (805) 373-1979. February 4 to 9.

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CXK581001P	128K x 8	70/85	DIP 600 mil	L
CXK581001M	128K x 8	70/85	SOP 525 mil	L
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The OEM Computer Technology Conference and Expo for Systems Design and Integration, Anaheim, CA. American Electronics Association, 5201 Great America Pkwy, Santa Clara, CA 95054. (503) 359-5873. FAX (503) 357-3839. February 11 to 13.

7th Annual IEEE Semiconductor Temperature and Thermal Management Symposium, Phoenix, AZ. Paul Wesling, IEEE, 12250 Saraglen Dr, Saratoga, CA 95070. February 12 to 14.

International Conference on Artificial Intelligence, Miami Beach, FL. CAIA '91, IEEE Computer Society, 1730 Massachusetts Ave NW, Washington, DC 20036. (202) 371-1013. February 24 to 28.

NEPCON West '91, National Electronic Packaging and Production Conference, Anaheim, CA. Cahners Exposition Group, 1350 E Touhy Ave, Des Plaines, IL 60018. (708) 299-9311. FAX (708) 635-1571. February 24 to 28.

European Design Automation Conference Amsterdam, The Netherlands. Professor Jochen Jess, Eindhoven University Technology, Box 513, 5600 MB Eindhoven, The Netherlands. (Phone) 31-40-47-3353. February 25 to 28.

SQL (Structured Query Language): A Hands-On Workshop, Seattle, WA. Learning Tree International, Box 45028, Los Angeles, CA 90045. (800) 421-8166; in Canada, (800) 267-1824; in CA, (213) 417-9700. March 12 to 15.

Advanced Research in VLSI Conference, University of California, Santa Cruz, CA. Kevin Karplus or Jean McKnight, Computer Engineering, UCSC, Santa Cruz, CA 95064. (408) 459-2303. March 25 to 27.

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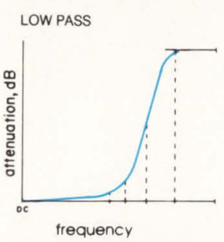
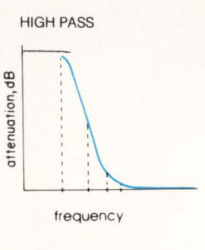


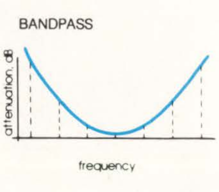
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz



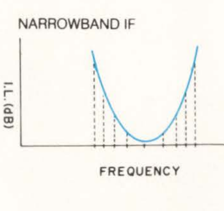
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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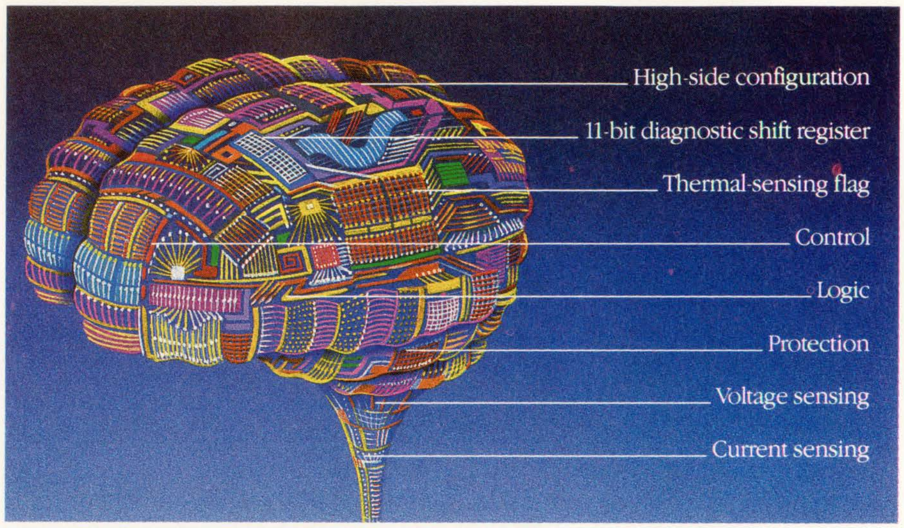

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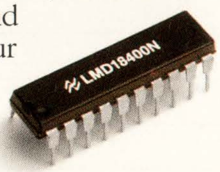

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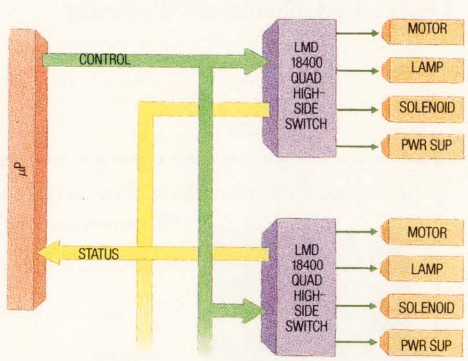

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EDITORIAL

Support your local test engineer

As a design engineer, you should know that testing the products you design is *your* responsibility . . . not somebody else's. In most companies, though, when it comes to product testing, design engineers aren't alone. Test engineering is becoming more important and increasingly complements design engineering.

In the field of test development, the US electronics industry is gradually emerging from the dark ages. Design engineers used to satisfy themselves that a design worked, then they would lob it over the proverbial wall separating design from test. There, it would land like a bombshell, ready to "explode" among the test engineers.

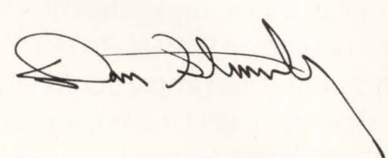
Many companies now use a design-and-test partnership. Sometimes this partnership is an uneasy one. Design engineers, accustomed to ruling the technical roost, grudgingly accept test engineers as members of the product design team—albeit inferior ones. They then often rail at the constraints the test engineers try to place on designs to ensure testability.

When developing a product's test strategy, it isn't important which type of engineer is chosen as the senior partner—test engineers and design engineers can be equally effective. A good design engineer knows the product better than the test engineer does, whereas a good test engineer knows the capabilities of test equipment and test-department personnel better. Moreover, the test engineer is a pragmatist who understands—in ways few design engineers care to—what approaches the company will accept.

When management hands out kudos for a product design, the design engineers usually receive the accolades (and occasionally the bonuses). The test engineer is lucky to receive recognition from his or her supervisor and peers. Now there *is* a way to recognize unsung heroes of test engineering: John Fluke Mfg Co is sponsoring a test-engineer award to be presented at the International Test Conference, which will be held in Nashville, TN from Oct 28 to Nov 1, 1991. Three finalists will be selected, and each will receive a plaque. The grand-prize winner will receive a $1000 award, or Fluke will donate $1000 to an organization of the winner's choice. The person who nominates the winner will receive $250.

To obtain nomination forms, write to John Fluke Mfg Co Inc, Test Engineer Awards, Box C9090, MS 250C, Everett, WA 98206. You can also send your request for nomination forms by FAX to (206) 356-5962. You must submit your completed nomination forms by the August 15, 1991 deadline.

We hope you work with a test engineer who you think should win. If you think your company doesn't have such a person, you ought to ask yourself why not. Think about what you and your colleagues can do to change the situation. There's a good chance that the problem has more to do with organizational attitudes than with a lack of talent. Challenge yourselves: If you work at it, in a year or two your problem could be that you have too many candidates. If so, whether or not your nominee receives a plaque or a check, your company will be a winner.



Dan Strassberg
Associate Editor

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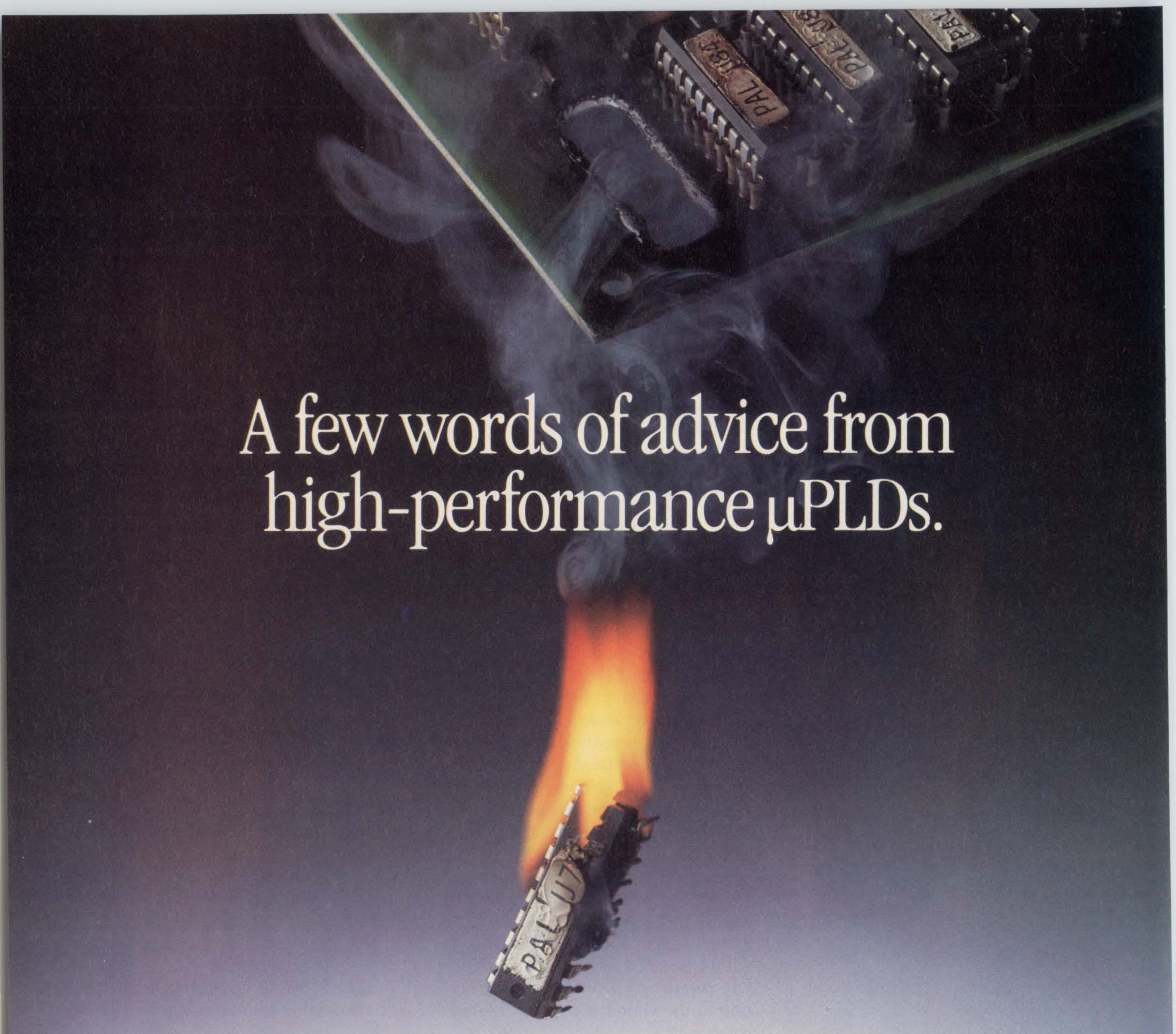

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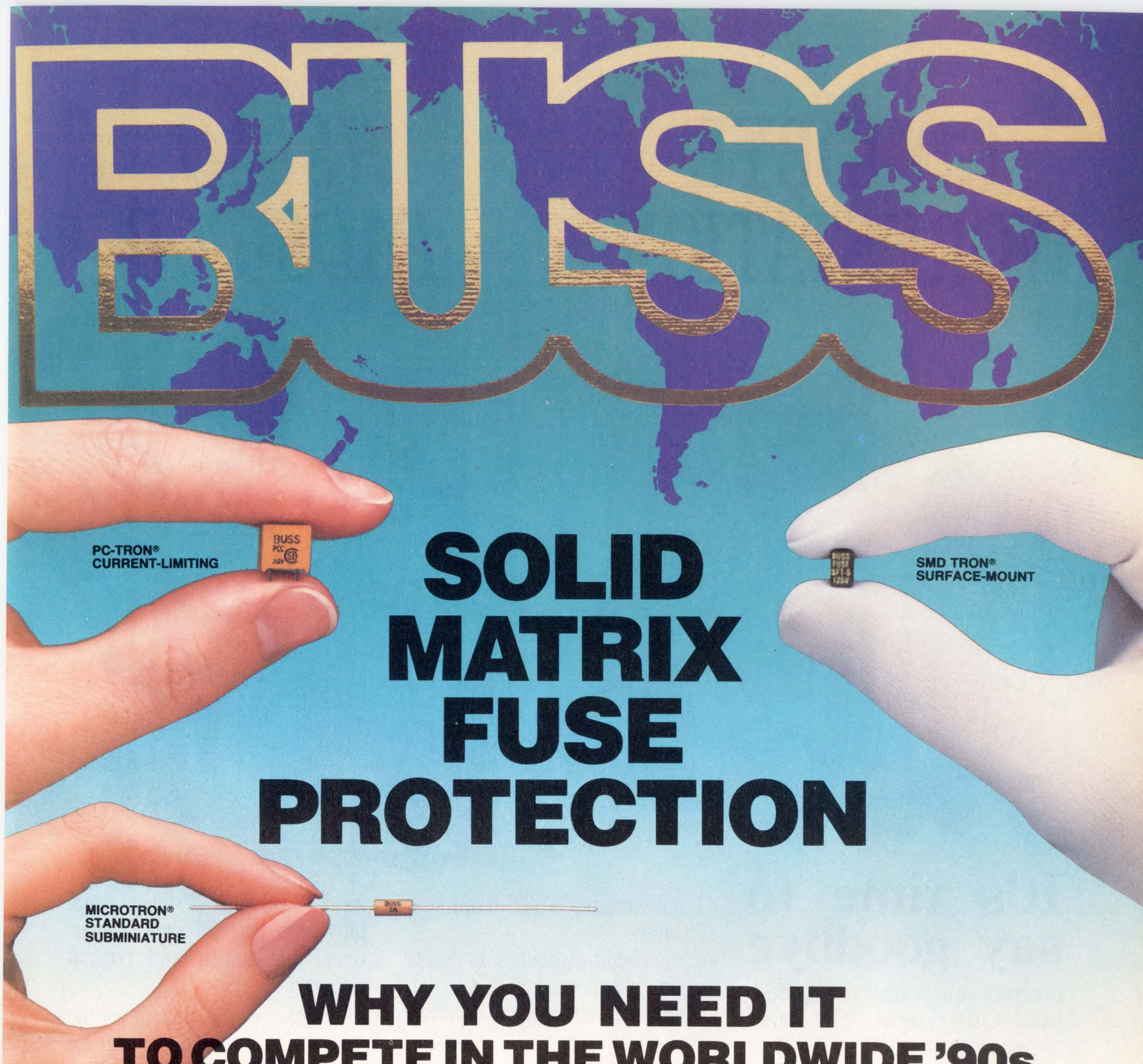

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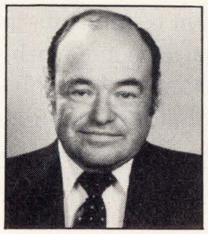
SERVO-MOTOR CONTROLLER BOARDS

Boards refine the art of servo control



Modular control boards and user-friendly software let system designers control sophisticated motions.

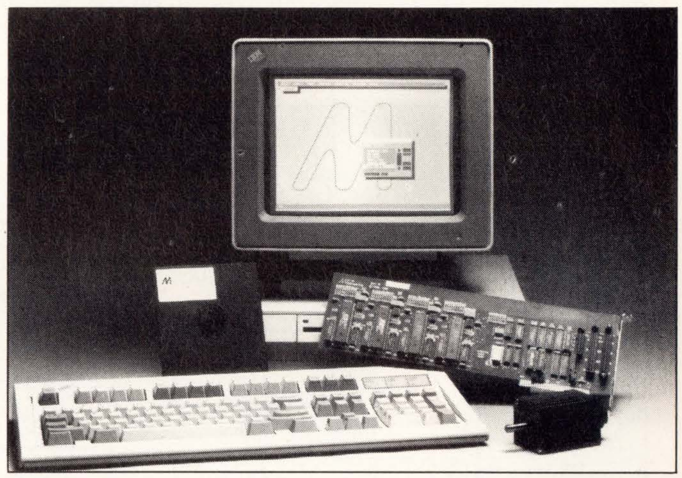
John Gallant,
Associate Editor

Designing a servo-motor control system is easier than it used to be. In the past, designers had to juggle such factors as loop stability, power-amplifier design, mechanical coupling, and a good knowledge of control theory to get such a system to work effectively. The need to control multiple axes in a synchronized movement complicated the task even further.

Today, vendors offer an assortment of servo-motor controller boards for computers and stand-alone applications. (This article concentrates on boards for the ISA bus, but most of the vendors offer boards with the same features and more for other bus architectures.) These boards make servo-control systems more modular. In many instances, you can build a multiaxis servo system by purchasing motors containing incremental encoders, power amplifiers, and one of these boards to complete the necessary hardware. The development software tools supplied with the boards let you optimize loop performance and synchronize motion on multiple axes.

You can expect a motor-control board to have a commercial motor-control IC, an ASIC, a μP, or a DSP chip performing the servo-loop control functions. The chips accept quadrature feedback signals from an encoder and have registers for storing motor commands and motion profiles. To drive the external power amplifier, the boards use either a dc output signal from a D/A converter or a sign-magnitude PWM signal.

In addition, the boards have dedicated digital I/O ports for inputs from limit switches, index pulses, and loop-status outputs. They also have user-definable digital I/O lines for programmable-logic controller signals that are synchronized to the motor's position. The digital lines are usually optoisolated to reduce noise. Some boards have watchdog timers that monitor the servo loop's operation and generate interrupts under emergency conditions.



Many boards employ commercially available motor-control ICs. *The MC series of boards from Motion Engineering employs a Hewlett-Packard HCTL-1000 that receives instructions directly from the ISA bus host computer.*

Technology 80 Inc offers servo-motor control boards for ISA bus, VMEbus, STD bus, and stand-alone applications. The boards employ a Hewlett-Packard HCTL-1000 or a National Semiconductor LM628 or LM629 motor-control IC for each axis of control. (See **box,** "Anatomy of two motor-control ICs," for a description of how these devices work). The 5638 and 5639 8-bit ISA bus boards utilize the LM628 and LM629 ICs, respectively. The boards can control one, two, or three axes of movement. The 5638 features a 12-bit DAC that provides a ±10V dc motor command. The 5639 has an optoisolated, 8-bit, sign-magnitude PWM output signal. The boards provide optically isolated inputs for quadrature signals from an incremental encoder. The maximum encoder rate is 1×10^6 counts/sec.

Twenty-three software commands let you control many loop functions via the host's keyboard. For example, you can command the boards to change the 16-bit coefficients of a proportional, integral, and differential (PID) loop filter while the motor is in motion, which compensates for changing load conditions. You can also specify and execute trapezoidal motion profiles and monitor the motor's status during a move.

The boards can update the digital data in the servo loop in a minimum of 256 μsec; a watchdog timer can disable the motor and issue an interrupt to the host. Eight digital inputs and eight digital outputs can input data from relays or switches and output data to solenoids or displays. An extra onboard quadrature decoder can operate as a master decoder to synchronize the velocity and position of multiple motors.

The boards come with a library of more than 70 assembly-language routines that are compatible with

Anatomy of two motor-control ICs

The heart of all servo-motor controller boards is a motor-control IC. Vendors employ a single μP, a custom ASIC in combination with a μP, a DSP IC, or a commercially available IC. Hewlett-Packard's HCTL-1000 and National Semiconductor's LM628 and LM629 are the most popular commercially available motor-control ICs.

The HCTL-1000 (**Fig A**) is a 40-pin NMOS device

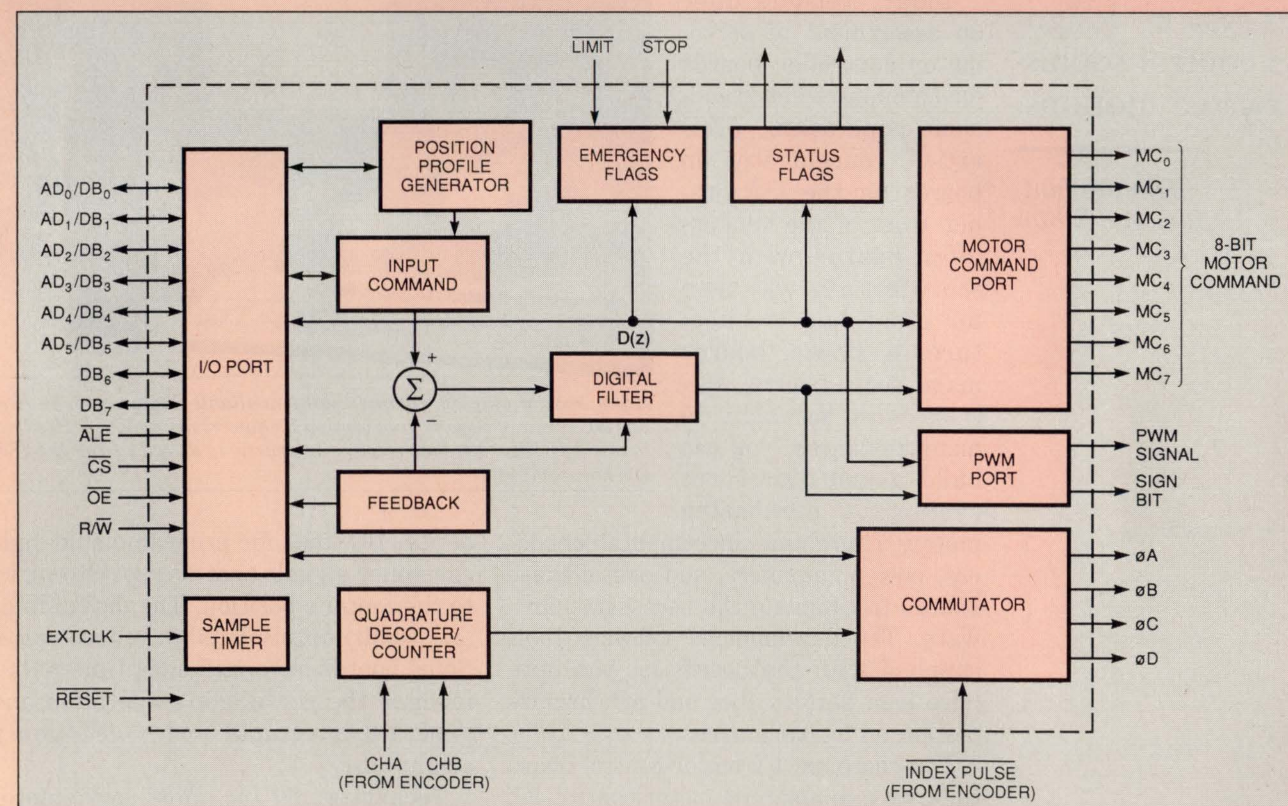


Fig A—Commercial motor-control ICs can perform all of the functions *needed to control a servo motor. Hewlett-Packard's HCTL-100 decodes quadrature encoder signals; provides a loop filter; delivers parallel, PWM, and phase-commutated motor commands; and includes an interface to a μP.*

Microsoft's C, Quick C, and Quick Basic. The routines come with the source code, so users can modify them.

IC commutates four phases

The MC-03 from Mektronix Technology Inc is another 3-axis motor-controller board for the 8-bit ISA bus. The board employs three Hewlett-Packard HCTL-1100 motor-control ICs, which are enhanced versions of the HCTL-1000. The board has a proportional derivative (PD) loop filter and provides both a ±5V dc signal and an 8-bit sign-magnitude PWM output signal. It also provides phase-sequenced commutator output signals for controlling 3- and 4-phase motors.

The board has 12 user-definable digital I/O lines and a port that can connect to an oscilloscope for monitoring the loop step response. The IC's command registers communicate directly with the host CPU and occupy eight bytes of a computer's I/O address space. The board comes with a library of Microsoft C, Turbo Pascal, and Quick Basic software routines. An Exerciser program lets you execute motor commands from the keyboard or a text file.

An optional numerical-control development package lets you rotate the motor at a constant velocity (also called jogging) as well as detect a specific motor position (homing) under keyboard control. The package conforms to the EIA RS-2740 standard for machine tool operation. A menu system lets the operator edit, simulate, and run programs, as well as linearly interpolate the position of a 3-axis move

---

for controlling dc, brushless dc, and stepper motors. (The HCTL-1100 is a lower-power CMOS version.) The IC has a bidirectional 8-bit multiplexed address and data bus that interfaces to a host μP. The HCTL-1000 accepts two quadrature signals from an incremental shaft encoder at a maximum rate of 300 kHz. The IC internally decodes the four transitions of the encoder clock cycle to provide an encoder resolution of 1.2×10^6 counts/sec. The IC then increments or decrements a 24-bit counter using the encoder counts to decode the motor's position. An internal commutator uses the encoder signals and an index pulse to select the correct phase sequence for commutating 2-, 3-, or 4-phase motors.

The HCTL-1000 generates the servo-control loop's position-error signal by comparing the motor's 24-bit decoded position with a command position located in an internal 24-bit register. The error signal feeds a programmable digital filter that has the following transfer function:

$$D(z)=K\,\frac{z-A}{z+B},$$

where K, A, and B are programmable constants. This first-order lead filter provides proportional and derivative (PD) compensation for closed-loop stability. You can program the minimum servo update time between 64 and 2048 μsec. The loop filter has an 8-bit parallel output, which drives an external D/A converter, and an 8-bit sign-magnitude PWM signal. The IC also has two inputs, which permit emergency interruptions.

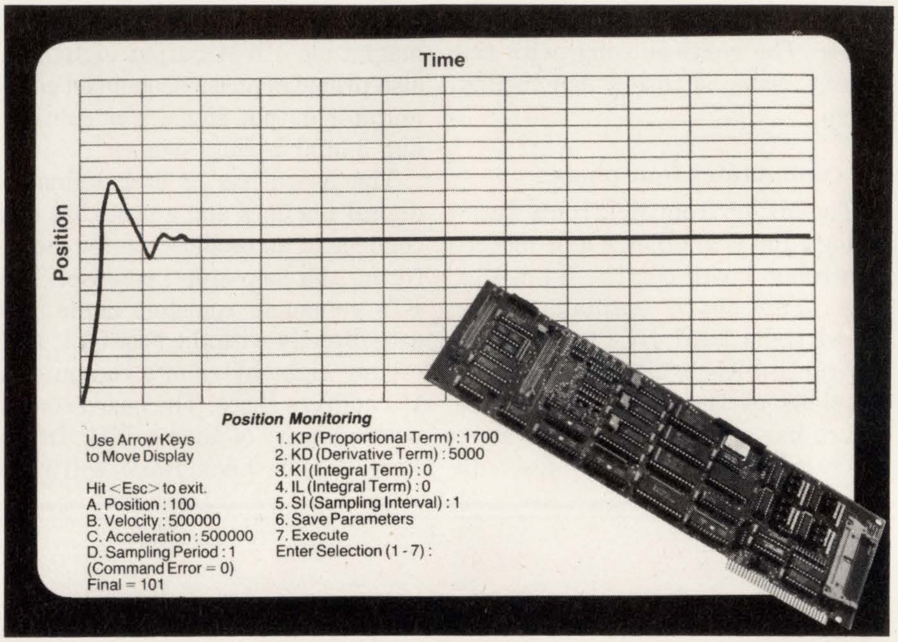
National Semiconductor's LM628 and LM629 are 28-pin NMOS devices that also accept two quadrature signals and an index pulse from an incremental encoder. The chips decode a maximum of 1×10^6 counts/sec from the quadrature signals and accumulate the counts with a 32-bit counter. Both chips create a position-loop error signal by comparing the 32-bit feedback-position register with a 32-bit command position register. The error signal drives a programmable digital filter that provides proportional, integral, and derivative (PID) compensation. The output of the LM628's filter is an 8-bit parallel port for driving an external D/A converter. The LM629 provides an 8-bit sign-magnitude PWM signal for driving H switches. Both chips have an 8-bit data bus that interfaces to a host μP.

You can program both the Hewlett-Packard and National Semiconductor motor-control ICs to generate motion profiles. The HCTL-1000 has four motion-control modes. The modes let you position the motor using point-to-point position moves or a trapezoidal position profile in which changes between motor positions occur at a specified linear velocity. The chip also has a trapezoidal velocity-profile mode, which enables the motor to change speeds at a specified linear acceleration. The LM628 and LM629 have trapezoidal velocity- and position-profile modes only. Both chips create velocity feedback by taking the derivative of the data in the feedback-position registers.

Servo-motor controller boards

and circularly interpolate the rotation angle of two motors in a 2-D plane.

Motion Engineering Inc manufactures 1-, 2-, 3-, and 4-axis motor-control boards that utilize the HCTL-1000 motor-control IC for both the 8-bit ISA bus and stand-alone applications. The MCS series of boards uses the host computer's CPU to transfer data to the IC's command registers. The registers map into the host memory address space, so read and write times are less than 3 μsec. The boards have a PD loop filter, generate analog or PWM motor-command signals, and provide phase commutation for stepper and brushless servo motors. The boards have limit and emergency-stop switch inputs, status output signals, and 12 bits of user-defined digital I/O.



Motor-control boards come with software *to optimize servo-performance. The software for Technology 80 Inc's 5638 ISA bus board lets you observe the loop step response while you adjust the coefficients for a PID loop filter.*

Each board comes with the Quick Script developers kit. The software, which is written in the HPGL graphics language, lets you create a plot file using AutoCAD and convert the file to motion control. You can create different motion profiles by reading a series of *n* points from a disk file as fast as 1024/*n* points/sec and executing point-to-point position moves. A jogging function lets you control motor speed using the + and − keys. Other software functions include changing register settings on the fly, 2-axis circular interpolation, and 4-axis profile contouring.

A μP for flexibility

Many vendors say commercial ICs limit the flexibility of a servo system. Creonics Inc, for example, employs a custom ASIC, the CX2216, and either an 80C186 or an 8031H μP to control the servo loop. The company offers motion-controller boards for the ISA bus, Multibus I and II, VMEbus, STD bus, and stand-alone applications.

The CX2216 ASIC can decode quadrature 1×10^6-count/sec signals from two incremental encoders using a 32-bit counter. It then delivers two 12-bit sign-magnitude PWM output motor-command signals. The μP calculates the servo-loop parameters in software and provides the interface to the host-computer bus. The μP also calculates the coefficients for a PID filter for loop compensation and provides a velocity feedforward signal, which helps the loop response follow a velocity command.

Creonics's IBM PC Motion Control Card (MCC) for the 8-bit ISA bus controls two axes of motion. The board features an 80C186 μP, a 256-byte dual-port RAM interface to the host, a 66×10^6-to-1 velocity range, a 2×10^9-to-1 acceleration range, 1-msec servo-update time, optical isolation for encoder and digital I/O lines, a CPU watchdog, and a ±10V dc and 12-bit sign-magnitude PWM motor command. The board occupies eight bytes in the host's I/O space and can operate in interrupt or polled mode.

The board has options that let you electronically adjust the gear ratio between two synchronized motors. Another option permits two motors to generate CAM waveforms. The board's software allows direct access to the board using peek and poke instructions. An optional library has 50 motion routines and is written in Microsoft C version 5.0. The routines handle all the commands to the board and come with source code for user modification.

A watchdog lends an eye

Galil's boards also perform motor-control functions using a custom ASIC and a dedicated μP. The company offers boards for the ISA bus, VMEbus, Multibus I, STD bus, and stand-alone applications based on the 68008 μP. The DMC-600 controls one, two, or three axes on an 8-bit ISA bus. The μP provides PID filtering and an acceleration feedforward signal that reduces the loop following error during accelerated moves. You can store com-

Table 1—ISA bus boards for servo-motor control

Vendor	Board name	Motor controllers	Number of axes	Position count range (bits)	Min servo update time (μsec)	Max encoder edge rate (counts/sec)	Motion profiles*	User digital I/O	Motor command	Loop filter‡	Price	Comments
Creonics	IBM PC MCC	8C186 CX2216	2	32	1000	1×10^6	1, 2, 3	4 inputs, 1 output per axis	$\pm$10V dc or PWM (12 bit)	PID; velocity feed forward	$2190	I/O mapped (8 bytes); electronic gearing and electronic cam optional
Delta Tau Data Systems	PMAC	DSP56001	4 or 8	24	50 to 500	10×10^6	1, 2, 3, 4, 5, 6, 7	20 inputs, 8 outputs	$\pm$10V dc (16 bit), 2-phase commutator (16 bit)	PID; velocity and acceleration feed forward	$2998 (4 axes)	Optional pole-placement algorithm; cubic-trajectory algorithm; and handwheel encoder
	SMCC	78312	2	24	480	1×10^6	1, 2, 3, 4, 5, 6, 7	7 inputs, 5 outputs	$\pm$10V dc (9 bits); 2-phase commutator; 11-bit PWM	PID; velocity and acceleration feed forward	$1679	Optional cubic-trajectory algorithm; RS232C port, 8-bit parallel port
Galil	DMC-600	68008 and an ASIC	1, 2, or 3	24	1000	2×10^6	1, 2, 3, 4, 5, 6, 7	8 outputs, 8 inputs	$\pm$10V dc (12 bit), 12-bit PWM	PID; acceleration feed forward	$895 (1 axis) $1995 (3 axes)	I/O mapped, 256-character FIFO buffer, 256k-byte RAM; 128k-byte EPROM
Mektronix Technology	MC-01	HCTL-1000	1	24	128	1.2×10^6	1, 2, 3	8-bit output, 4-bit input	$\pm$5V dc; PWM at 20 kHz with sign bit; 3- and 4-phase commutator	PD	$465	Optional hand wheel encoder; I/O mapped; optional machine tooling software
	MC-03	HCTL-1100	3	24	128	1.2×10^6	1, 2, 3	8-bit output, 4-bit input	$\pm$5V dc; PWM at 20 kHz with sign bit; 3- and 4-phase commutator	PD	$1065	Optional handwheel encoder; I/O mapped, optional machine tooling software
Motion Engineering	MC-Series	HCTL-1000	1, 2, 3, or 4	24	64 to 2048	1.2×10^6	1, 2, 3	8 inputs, 4 outputs (24 bits optional)	$\pm$10V dc (8 bits); 4-phase commutator 8-bit PWM	PD	$295 (1 axis) to $895 (4 axes)	Memory mapped
	MCS-Series	HCTL-1000	1, 2, 3, or 4	24	64 to 2048	1.2×10^6	1, 2, 3, 5, 6	8 inputs, 4 outputs (24 bits optional)	$\pm$10V dc (8 bits) 8-bit PWM; 4-phase commutator	PD	$495 (1 axis) to $1095 (4 axes)	AutoCAD to motion via HPGL poles; memory mapped
Technology 80 Inc	5638	LM628	1, 2, or 3	32	256	1×10^6	2, 3	8 inputs, 8 outputs	$\pm$10V dc (12 bits)	PID	$695 (1 axis) to $1350 (3 axes)	Watchdog, programmable timer, additional quadrature decoder
	5639	LM629	1, 2, or 3	32	256	1×10^6	2, 3	8 inputs, 8 outputs	8-bit PWM	PID	$695 (1 axis) to $1295 (3 axes)	Watchdog programmable timer, additional quadrature decoder
Whedco	3697	Z80	2	32	1000	1×10^6	1, 2, 3, 5, constant torque mode	2 outputs	$\pm$10V dc (12 bit)	PID, velocity feed forward	$895	I/O mapped (16 bytes); 7k-byte RAM, 8k-byte ROM
	3797	Z80	1	32	1000	1×10^6	1, 2, 3, 5, constant torque mode	2 outputs	$\pm$10V dc (12 bit)	PID, velocity feed forward	$655	I/O mapped (16 bytes); 7k-byte RAM 8k-byte ROM

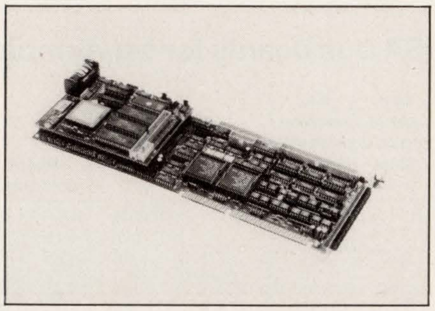
*Motion Profiles:
1. Point-to-point position, 2. Trapezoidal position, 3. Trapezoidal velocity, 4. Parabolic velocity, 5. Linear interpolation, 6. Circular Interpolation, 7. S-curve acceleration.

‡PD = proportional derivative; PID =proportional, integral, and derivative.

Servo-motor controller boards

mands and motion programs in the board's 256k-byte RAM. The board has a watchdog timer as well as a ±10V dc and a sign-magnitude PWM motor-command signal. The board maps into the computer's I/O address space and has a 256-byte FIFO buffer to receive data from the host.

The software supplied with the DMC-600 lets you create a variety of independent or coordinated motions using an ASCII instruction set. You can specify a linear segment of motion by specifying the ending X-Y coordinates of a vector. You designate an arc segment using a radius, an initial angle, and a travel angle. A contouring mode lets you generate position trajectories of almost any shape for all axes. The controller performs linear interpolation between specified points for smooth motion. You can also perform mathematical operations on the motion variables and change them while the program is executing.



For fast loop sampling times and complex motion profiles *for many axes, consider a board that uses a DSP chip for motion control. The PMAC boards for the ISA bus and VMEbus from Delta Tau Data Systems employ a DSP56001 IC. The boards can be daisy chained to synchronize as many as 128 axes and update the servo loop in as little as 50 μsec.*

Whedco uses a Z80 μP to perform motor-control functions and host communications. The company offers ISA bus, STD bus, and VMEbus motor-controller boards. The 3697 and the 3797 8-bit ISA bus boards have PID filtering and velocity feedforward to reduce the loop's following error during velocity moves. The boards have 7k bytes of memory in which you can store as many as 255 motion profiles. The boards occupy eight consecutive bytes in the host's I/O address space and have an 8k-byte ROM for the firmware. A 12-bit DAC produces a ±10V dc motor-command signal. The 3797 and 3697 have 14 and 28 user-definable digital I/O lines, respectively.

The boards use a long-term integration compensator when an analog velocity loop exists. The compensator eliminates dc offsets in the velocity loop; traditionally, a potentiometer in the loop amplifier tweaked these offsets. The board's command set lets you program the board for piece-wise-linear, soft-start and soft-stop acceleration as well as point-to-point position and trapezoidal velocity profiles. You can also adjust set points while the motor is moving. A torque-mode command executes a torque profile and can maintain a constant motor torque during changing load conditions.

A few vendors use DSP ICs for motor control when high-speed motion-parameter calculations are necessary. Although DSP chips were designed for audio and video applications, they have many features that make them ideal for motor control. Motorola's DSP56001 can prefetch an instruction, multiply two 24-bit numbers, perform a 56-bit addition, transfer two data words, and update two address pointers in a single instruction cycle. These features make the chip ideal for calculating a new position vector when multiplying a coordinate-transformation matrix by the current position vector.

Mektronix Inc employs an AT&T WE-DSP32 IC on its stand-alone AMC-12 motion controller board, which controls 12 axes simultaneously. Delta Tau Data Systems Inc employs a DSP56001 IC on its PMAC boards for the VMEbus and the ISA bus. The boards control as

For more information . . .

For more information on the servo-motor controller boards discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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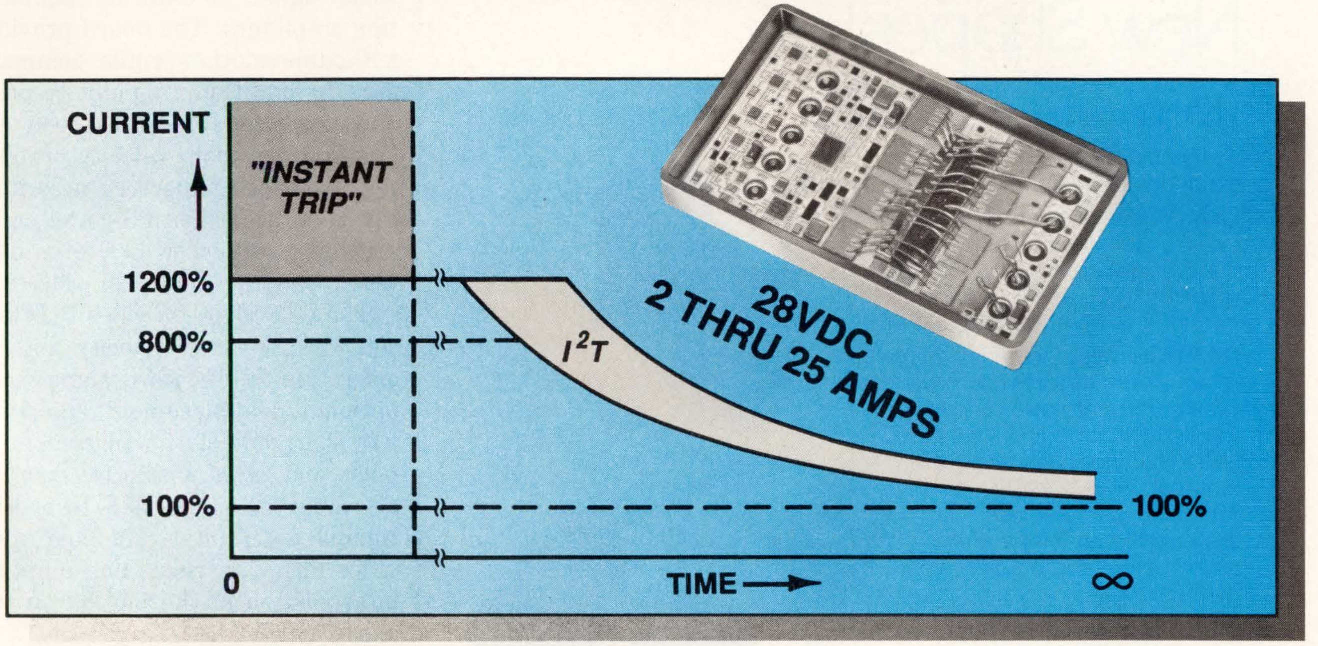

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Utilizing power MOSFET switches, these power controllers offer low "ON" resistance, low voltage drop, high "OFF" impedance, and low power dissipation. Built with power MOSFETs and custom monolithics many options such as I^2T trip curve tailoring, output rise and fall times, and a variety of custom current ranges are possible. They offer small size, low power, and high reliability, since there are no mechanical parts.

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The SSP-21110 series will operate over the full military temperature range from -55°C to +125°C. Military screening and optional packaging are available upon request. The SSP-21116, 270 Vdc, series, will be available before the end of the year.

Please contact Steve Friedman at (516) 567-5600 extension 381 for further information concerning the SSPC products. ❑

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many as eight axes simultaneously.

The PMAC-PC board for the ISA bus accepts signals from a quadrature incremental encoder at 10 counts/sec. It produces either a ±10V dc motor command with 16-bit resolution per axis or two sinusoidal signals for external commutation amplifiers. The board provides a flexible motion-profile command set. In addition to point-to-point and trapezoidal profiles, you can generate parabolic velocity profiles. A third-order trajectory algorithm can generate smooth S-curve acceleration profiles, which eliminate jerk terms in the motion profile.

The DSP56001 provides PID loop compensation and velocity and acceleration feedforward signals. An optional pole-placement algorithm lets you control the placement of poles and zeros within the loop. It also lets you access a 1- to 500-Hz tunable notch filter. The board provides linear, circular, and elliptical interpolation of the motion on two axes.

In addition to dedicated digital I/O lines for limit switches and homing commands, the board provides 20 digital inputs and 8 digital outputs, all of which are user definable. All digital lines are optoisolated. The programmable minimum servo-update time of 50 μsec to 1 msec lets you control the percentage of time the DSP chip uses to calculate loop parameters. You can daisy-chain as many as 16 boards to control 128 synchronized or independent axes.

Motor-control applications continue to grow in such fields as robotics, material handling, laser cutting, and camera controls. Modular motion-control boards along with user-friendly development tools ease the development of such systems.

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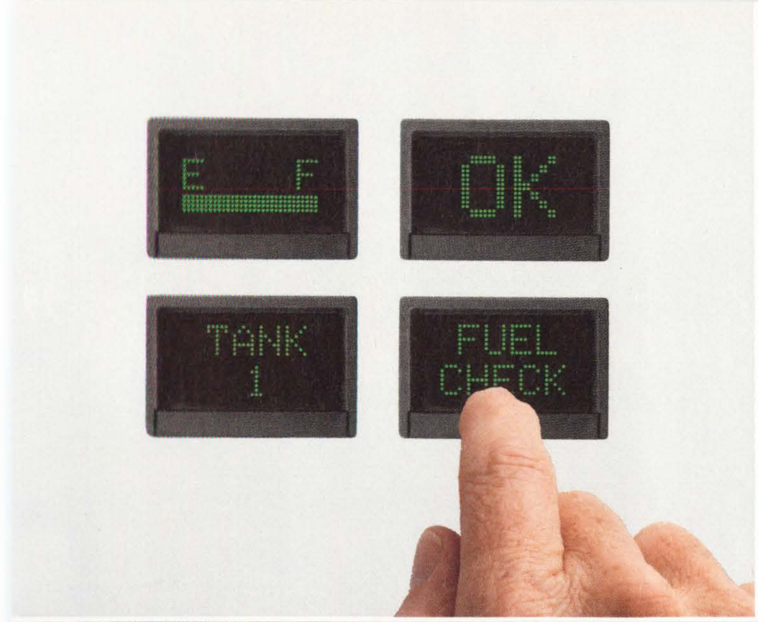

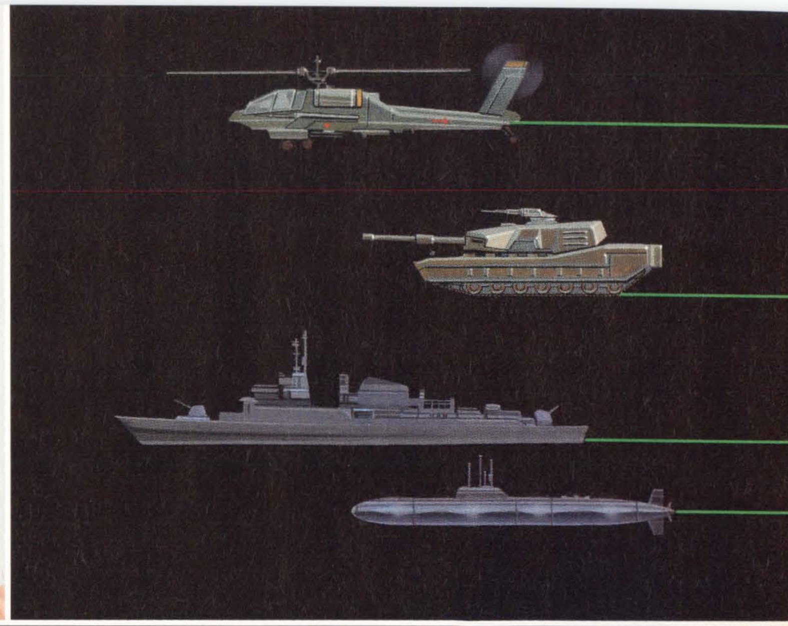

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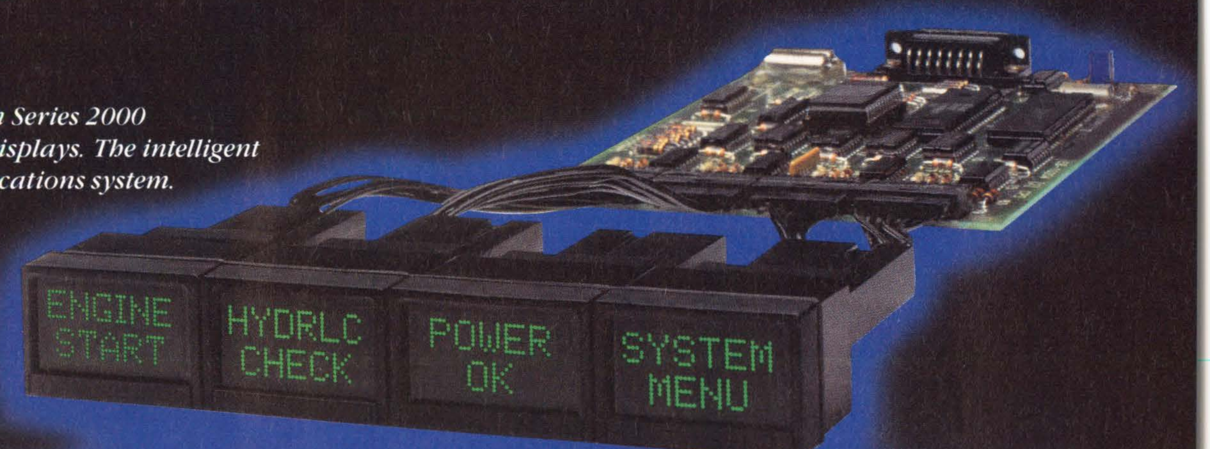

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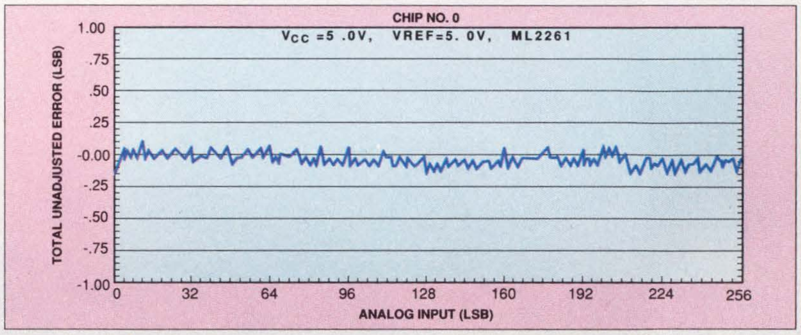

Built-in digital error correction delivers true 8-bit accuracy, with typical unadjusted error of less than ± ¼ LSB.

inputs can withstand at least 25 mA, you can achieve better latch-up immunity on analog inputs. The digital interface is also designed to keep up with the fastest microprocessors and appears as a memory location or I/O port to the microprocessor. In addition, no external clock is required and power dissipation is a mere 75 mW. All parameters are guaranteed over the supply tolerance and temperature range.

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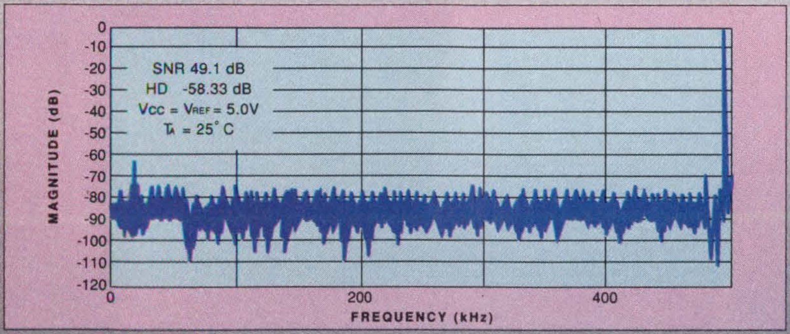
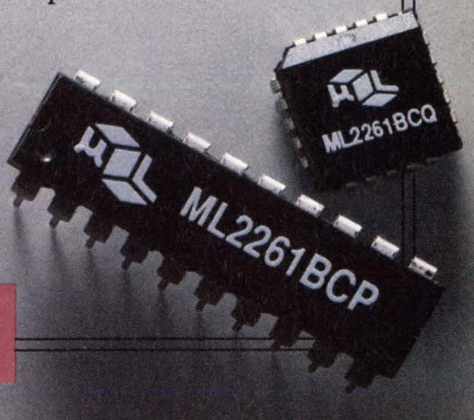
To find out more about how you can quickly convert your new product design to the ML2261, just call (408) 433-5200. Or write to: Micro Linear, Dept. TFA, 2092 Concourse Drive, San Jose, CA 95131. We'll send you all the specs. In a flash.



The ML2261 maintains ideal signal-to-noise ratios independent of increasing analog input frequencies to 500kHz.



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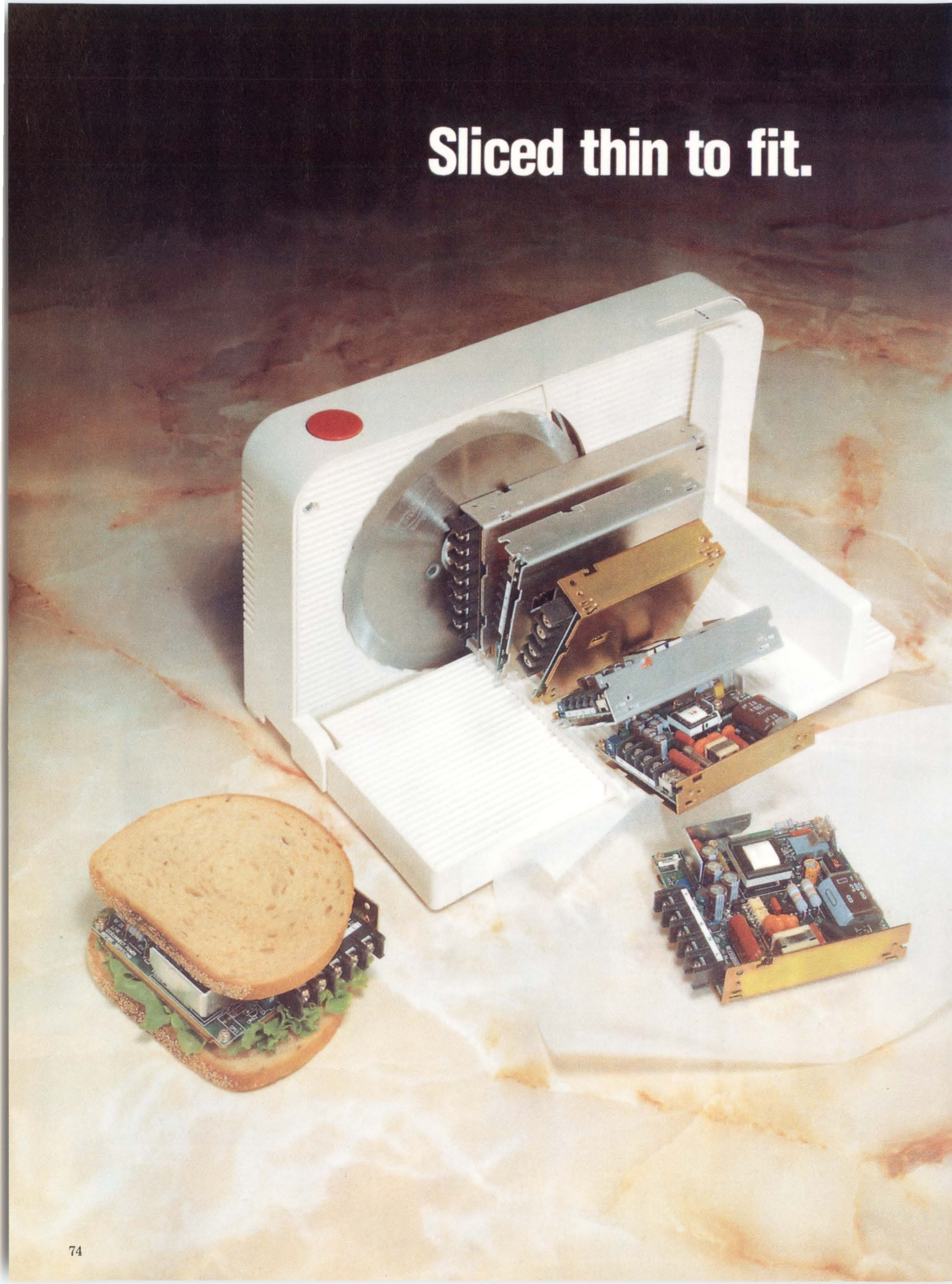
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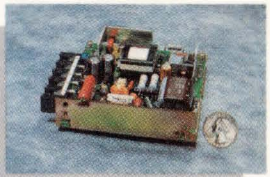

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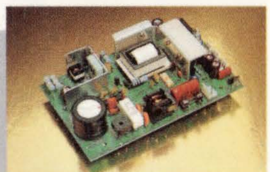
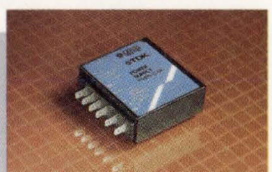


Series MRW

Triple output power supplies in the popular 100 X 160mm card size, MRW 150KV offer 35 Watts; MRW 160KV offer 50 Watts in the same footprint. Both feature a wide range (universal) input that accommodates 85-265V a-c. Built to the strict IEC 380/VDE 0806 standard, MRW have TÜV approval, as well as that of UL and CSA. MRW feature a built-in FCC Class B/VDE 0871 level B EMI filter. PC card design with optional metal enclosure. ***35W:*** *1.12 x 3.93 x 6.3 in.* ***50W:*** *1.5 x 3.93 x 6.3 in.*



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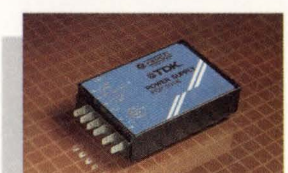

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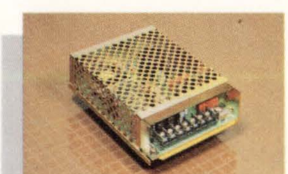
3W: *0.75 x 2.17 x 1.97 in.* ***10W:*** *0.75 x 2.17 x 3.15 in.*



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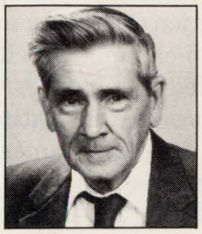
CIRCLE NO. 7

POWER HYBRID ICs

Multichip circuits satisfy special needs



Monolithic ICs and discrete power devices can't satisfy every need. For power applications requiring space-saving packaging, a hybrid circuit may be your best choice.

Dave Pryce, Associate Editor

Over the past few years, a number of monolithic-IC suppliers have expanded their catalog of standard parts to include devices that combine power capabilities with signal-processing or control functions. Such devices—often called "smart-power" ICs—provide space- and cost-saving benefits for many applications that previously used combinations of monolithic ICs and discrete power transistors. However, these single-chip devices are often out of their realm when confronted with high-power requirements or the special needs of certain motor-control and power-conversion applications. Where space is at a premium, a hybrid circuit may be your best choice.

Power hybrid ICs are available in a variety of circuit configurations, power capabilities, and packaging styles. Examples of available circuits include solid-state relays and circuit breakers, half-bridge and full-bridge drivers, 3-phase drivers, and dc/dc converters. (See **Table 1** for a representative list of power hybrid ICs.) Because of their specialized construction, hybrid ICs are often more expensive than equivalent combinations of monolithic ICs and discrete power devices. This higher cost is particularly true for military-grade hybrid ICs, which make up a large part of the mar-

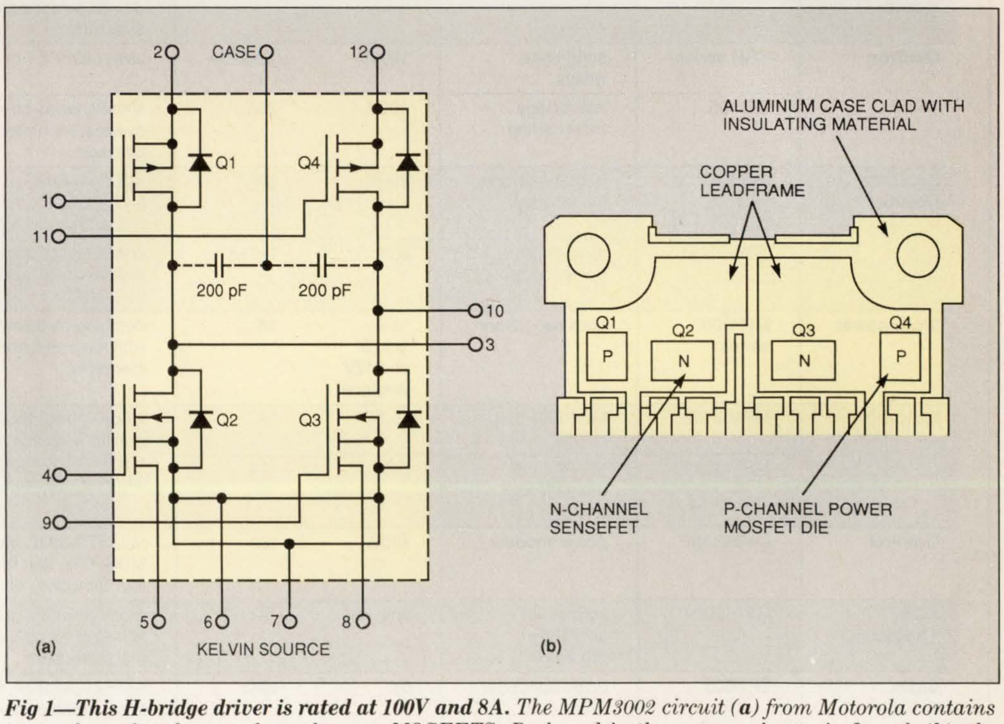


***Fig 1—This H-bridge driver is rated at 100V and 8A.** The MPM3002 circuit (**a**) from Motorola contains two n-channel and two p-channel power MOSFETS. Packaged in the company's 12-pin Icepak (**b**), the module has a power-handling capability of 62.5W.*

Power hybrid ICs

ket. Despite the cost, hybrid ICs have the redeeming characteristics of small size and the ability to combine specialized circuitry in a single package.

A key factor in obtaining these characteristics is the extensive use of chip-level and surface-mount components, including both active and passive types. Typically mounted on an alumina or beryllia substrate, such components minimize the size of the final package and allow flexibility in the design of the overall circuit.

A power hybrid IC can be as simple as a half-bridge driver or as complex as a dc/dc converter that contains all of the necessary active and passive devices, including magnetic components and filtering elements. Highly specialized hybrid ICs often contain dozens of components and can be quite elaborate.

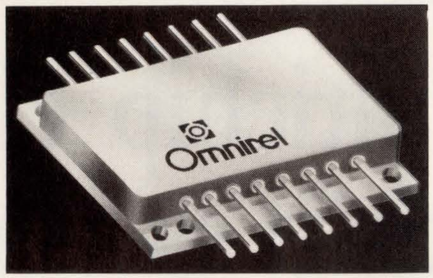


Fig 2—This 16-pin hermetically sealed package *is used for Omnirel's OM9011SF. The power hybrid IC contains four n-channel MOSFETS, four Schottky diodes, and four high-speed rectifiers.*

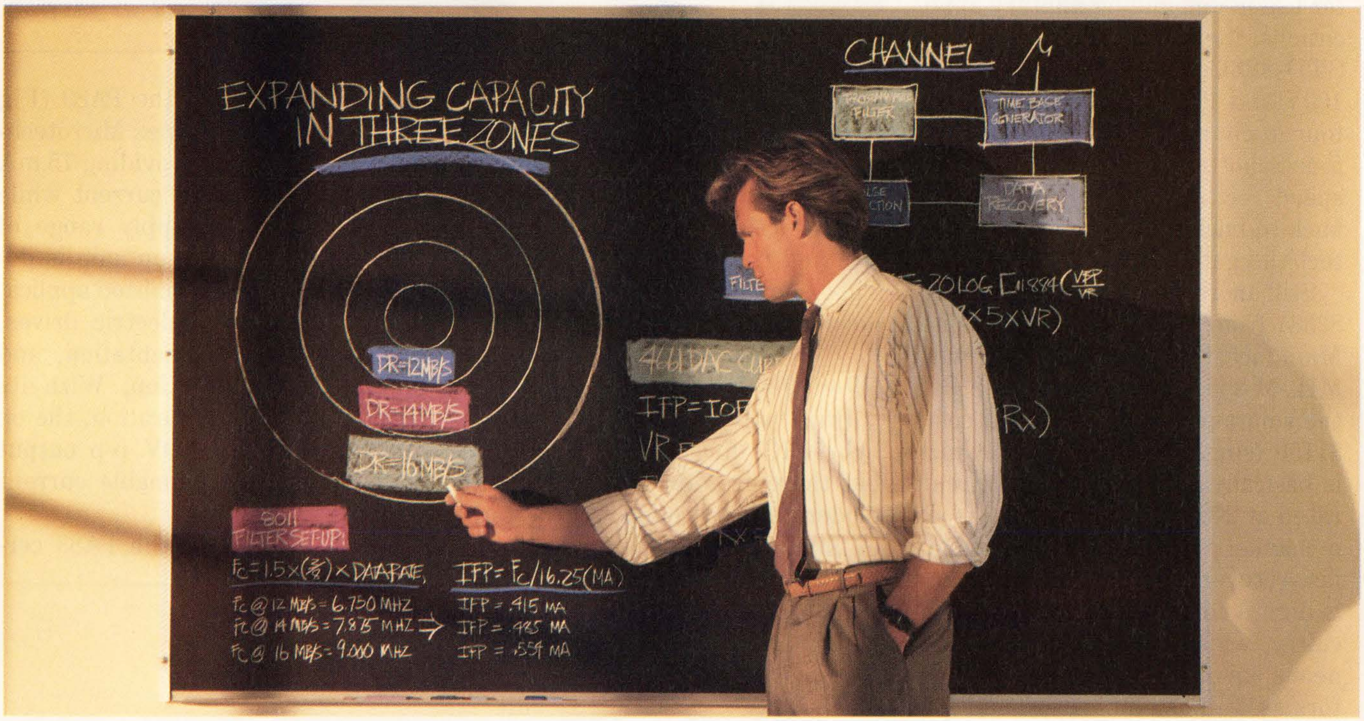
The MPM3002 H-bridge from Motorola is a good example of space-saving hybrid IC construction. Designed for applications such as servo motor drives, stepper-motor controls, and switching power supplies, the relatively simple IC contains four power MOSFETs with a total power capability of more than 60W. The upper legs of the circuit (**Fig 1a**) use p-channel devices, and the lower legs use Motorola's n-channel Sensefet devices, which feature a current-sensing Kelvin connection.

Packaged in Motorola's Icepak power module, the bridge circuit's construction (**Fig 1b**) consists of two n- and p-channel MOSFET pairs die-bonded to two separate copper leadframes. An insulating material isolates the leadframes from the aluminum case. The case, which has two mounting holes, provides heat-sinking capability for which Motorola provides detailed thermal data. Although deceivingly spartan in terms of its circuit complexity, the space savings afforded by the

Table 1—Representative power hybrid circuits

Company	Part number	Circuit type	Max ratings		Features	Cost
Apex u-tech	PA03	power op amp	75V,	30A	1 MHz gain-bandwidth product, 30 kHz power bandwidth, 8V/μsec slew rate.	$203.50 (100)
Gentron	SSR series	solid-state relays	1200V,	25–125A	uses MOSFET or IGBT switches	$13.88 to $58.92 (100)
	GS-105	half-bridge motor driver	400V,	25A	simultaneous-conduction lockout, overcurrent protection, isolated package.	$100 (50)
ILC Data Device	PWR-82331	3-phase bridge motor driver	200V,	30A	MIL-STD-883C process, six MOSFETs, six diodes, digital control, and protection circuitry.	$1150 (1–9)
	SSP-21110	solid-state power controller	28V,	2–25A	contains high-side MOSFET switch, driver, and isolated controller	from $255 (100)
Modupower	MP7000 series	buck regulators	15V, also 5 and 12V versions	1A	combines 5-terminal regulator with magnetic and filtering elements.	$17 (100)
Motorola	MPM3002	MOSFET half-bridge	100V,	8A	Icepak power modules for single- and three-phase motor drive. Used with company's MCxxxx series of control ICs	$9.57 (100)
	MPM3003	MOSFET 3-phase bridge circuit	60V,	10A		$14.08 (100)
Omnirel	OM9011SF	power module	100V,	18A	MIL-STD-883C process, four MOSFETs, four rectifiers, and four Schottkey diodes.	$781.40 (100)
SGS-Thomson	GS-R400V	step-down switching regulator	5 to 40V,	4A	programmable output voltage, soft-start, short-circuit, and thermal protection.	$24 (100)
Sipex	SP2805	dc/dc converter	5V,	10A	1-MHz operation, has input/output filters, transformer, switching transistor, and control	$1265 (100)

The universe is expanding.



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Power hybrid ICs

module's hybrid construction are obvious. The MPM3002, which costs $9.57 (100), typically replaces four TO-220-packaged MOSFETS, four diodes, four mica insulators, and a host of mounting hardware.

Somewhat more complex—and considerably more expensive—than the Motorola device, the OM9011SF from Omnirel comes in a 16-pin hermetically sealed metal package (**Fig 2**) and costs $781.40 (100). Designed for use in demanding military applications, the OM9011SF meets MIL-STD-883C standards. Rated at 100V and 18A, the module contains four n-channel power MOSFETs, four Schottky diodes and four high-speed rectifiers. Also included are back-to-back zener clamps that protect the gate of each MOSFET.

Still more complex is the PWR-82331 from ILC Data Device Corp. Manufactured in accordance with MIL-M-38510 and MIL-STD-883C, the smart-power motor driver costs $1150 (singles). The hybrid, which is basically a 3-phase bridge circuit rated at 200V and 30A, contains six n-channel power MOSFETS and six fast-recovery diodes. Also included is digital control and protection circuitry, which prevents the simultaneous conduction of in-line transistors as well as eliminating multiple upper- and lower-leg conduction. Additionally, an external shutdown input provides fast turn-off of the 3-phase bridge. **Fig 3** illustrates the space-saving advantages of the PWR-82331's chip-level hybrid construction.

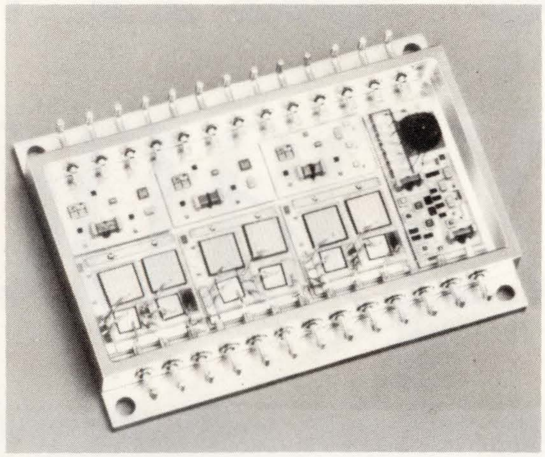


Fig 3—This 3-phase, smart-power motor driver *from ILC Data Device Corp meets MIL-STD-883C standards. In addition to digital control and protection circuitry, the hybrid IC contains six n-channel MOSFETs and six fast-recovery diodes.*

Although high-powered bridge circuits for use in motor-control applications are natural candidates for hybrid construction, power hybrid ICs take many other forms. For example, Gentron offers a line of solid-state relays that use a MOSFET or an IGBT (insulated-gate bipolar transistor) as the switching element. ILC Data Devices' makes a power controller, which contains a high-side MOSFET switch along with an isolated control circuit. Sipex has a 1-MHz dc/dc converter that contains all the necessary active and passive components. SGS-Thomson offers a complete step-down switching regulator.

Op amp satisfies special needs

Price and functionality of power hybrid ICs fluctuates dramatically, but there are devices that are both moderate in price and offer a range of functions. One of the most noteworthy examples is the PA89 (**Fig 4**), an op amp from Apex Microtechnology. Capable of providing 75 mA of continuous output current while operating over a supply range of ±75 to ±600V, the op amp is designed for use in specialized applications such as piezoelectric drives, high-voltage instrumentation, and electrostatic deflection. With its output-bridge configuration, the op amp provides a 1000V p-p output signal with programmable current limiting.

At $310.50 (100), the PA89 cer-

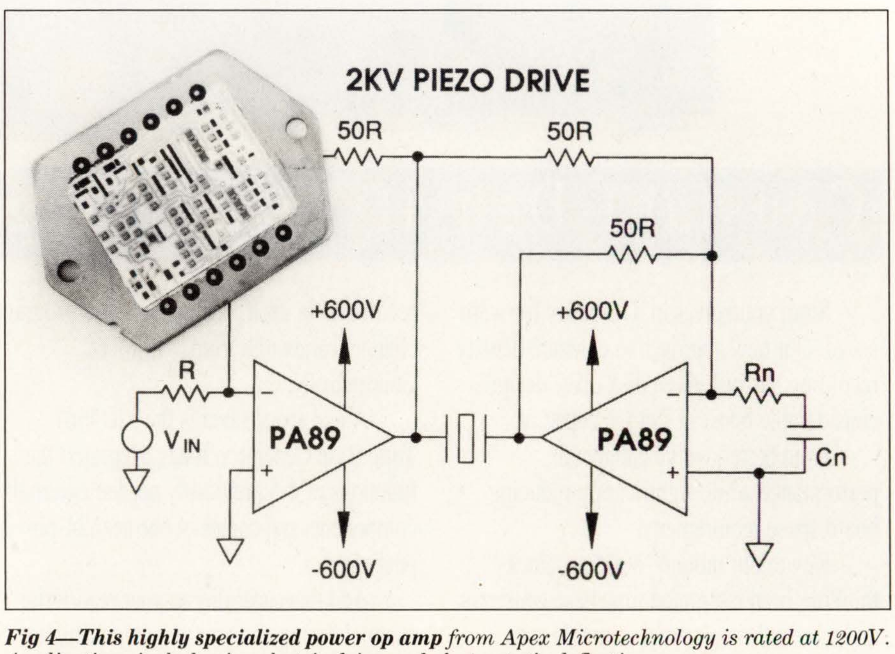
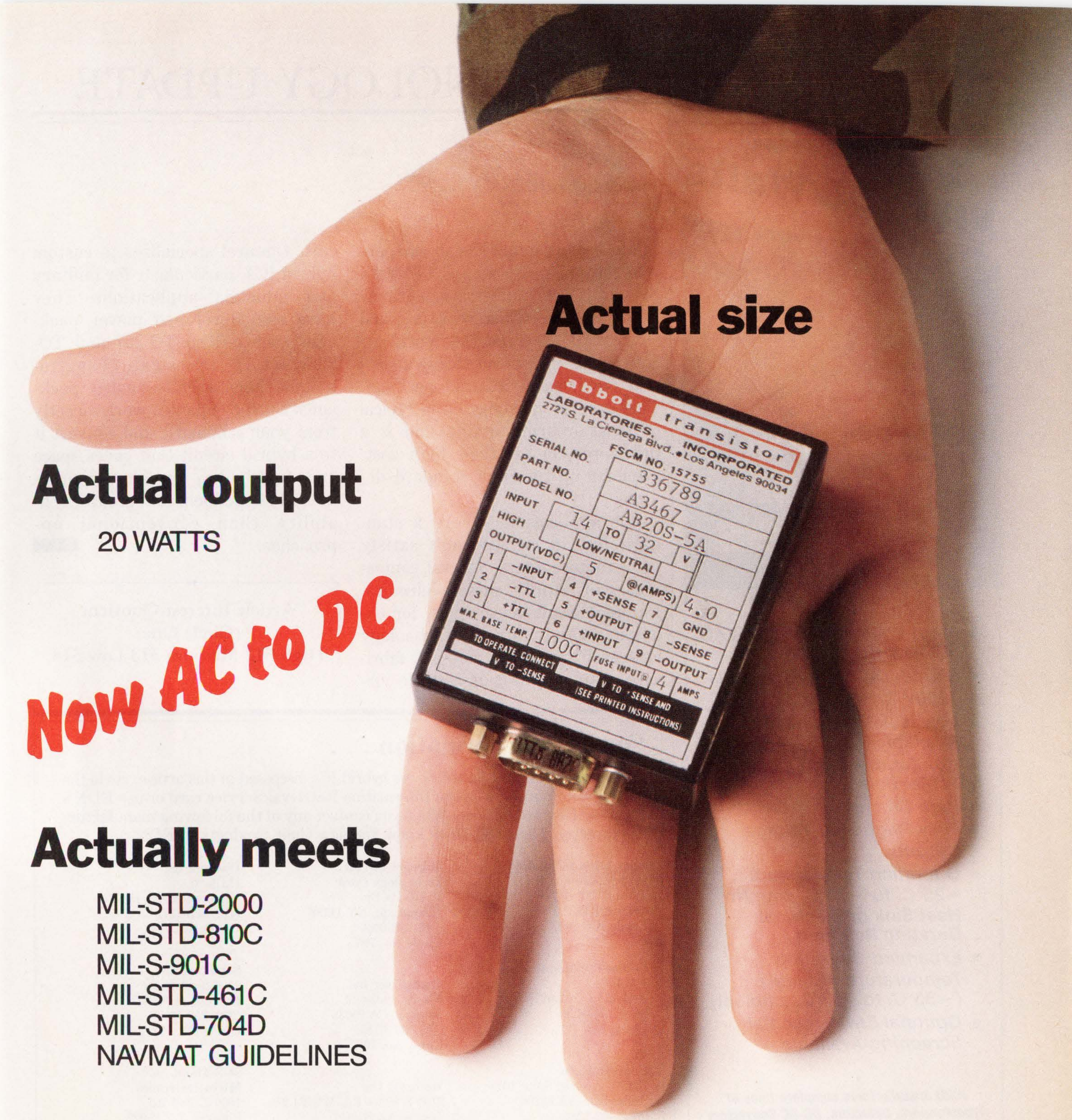


Fig 4—This highly specialized power op amp *from Apex Microtechnology is rated at 1200V. Applications include piezoelectric drive and electrostatic deflection.*



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Power hybrid ICs

tainly doesn't qualify as an inexpensive jelly-bean op amp. Utilizing a beryllia (BeO) substrate, ceramic capacitors, thick-film resistors, and semiconductor chips, the hybrid circuit comes in a hermetically sealed and electrically isolated package. This type of construction is typical of most hybrid circuits and is a prime reason for their high cost, even for off-the-shelf standard devices.

For applications where a standard hybrid circuit can't satisfy your requirements, several companies can supply custom circuits. Philips Circuit Assemblies, for example, has a number of technology choices from which they can fabricate your application-specific circuit. Omnirel specializes in custom hybrid ICs, particularly for military and industrial applications. They have also developed power packages such as the TO-257 and TO-258, which are small, easy-to-mount, hermetically sealed packages. Such companies work directly from your schematic and convert it to a hybrid circuit that saves space and usually has superior environmental ruggedness and greater reliability than conventional approaches. **EDN**

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For more information . . .

For more information on the power hybrid ICs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the fol lowing manufacturers directly, please let them know you saw their products in EDN.

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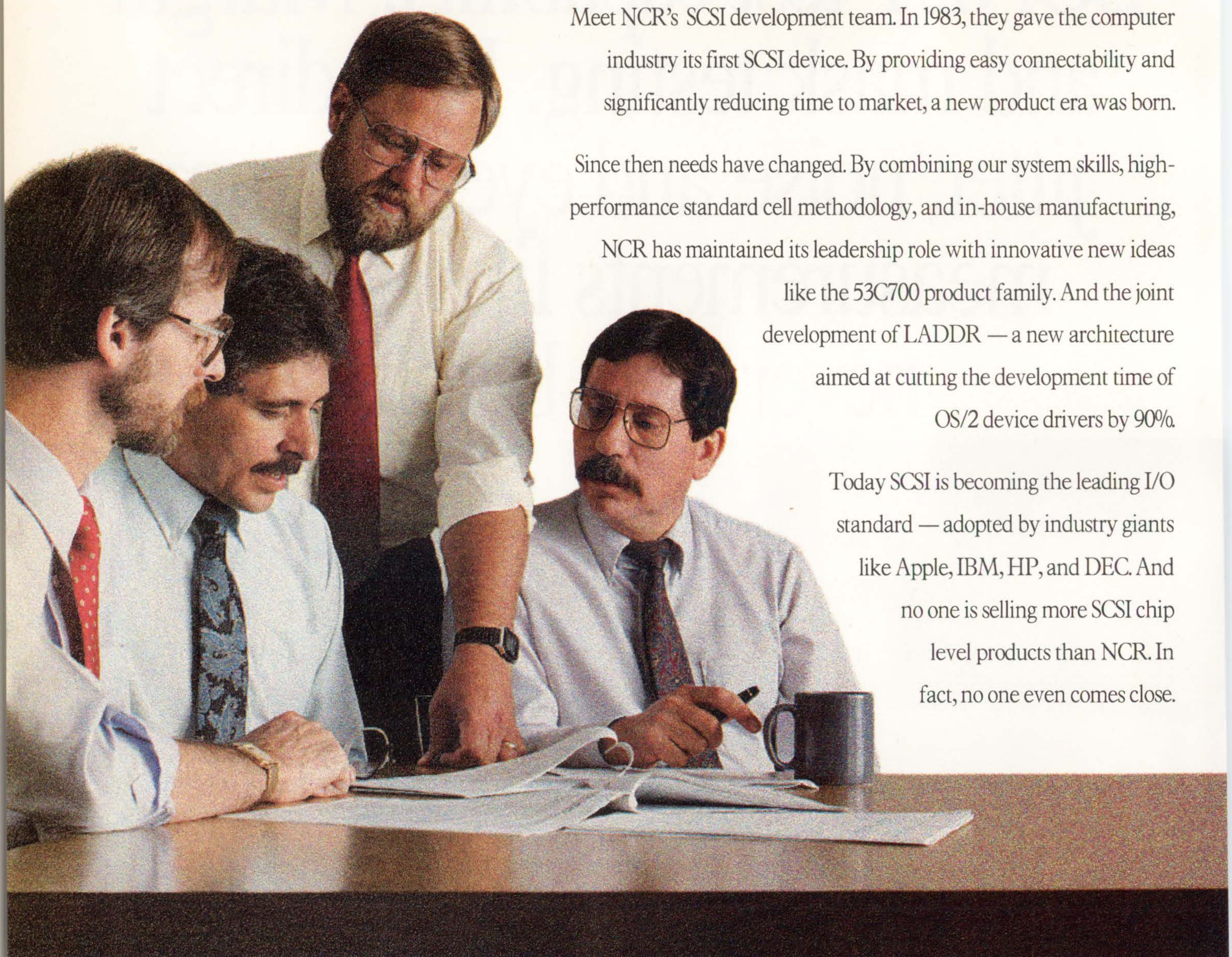
Since then needs have changed. By combining our system skills, high-performance standard cell methodology, and in-house manufacturing, NCR has maintained its leadership role with innovative new ideas like the 53C700 product family. And the joint development of LADDR — a new architecture aimed at cutting the development time of OS/2 device drivers by 90%.

Today SCSI is becoming the leading I/O standard — adopted by industry giants like Apple, IBM, HP, and DEC. And no one is selling more SCSI chip level products than NCR. In fact, no one even comes close.



Part of the NCR SCSI Development Team: (left to right)
Jerry Armstrong, Sr.Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI ProductManager.

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Here's another.

The NCR 53C700 SCSI I/O Processor… So good, *Electronic Design* named it the product of the year.

"You can't tell a good SCSI chip just by looking at it…" and according to Electronic Design, NCR's 53C700 is the best there is.

The only third generation SCSI device on the market today, it concentrates all the functions of an intelligent SCSI adapter board on a single, smart and extremely fast, chip… for about 15% of the cost.

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And now the NCR 53C710!

For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

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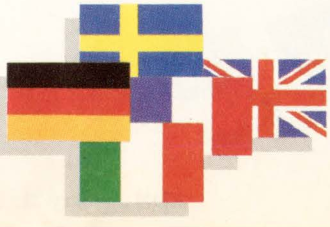
Creating value

CIRCLE NO. 14



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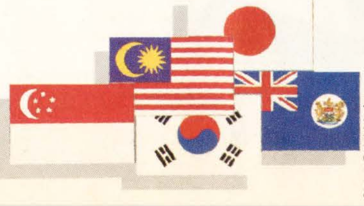

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CIRCLE NO. 4

SHOW PREVIEW

Futurebus+ nabs center stage at Buscon

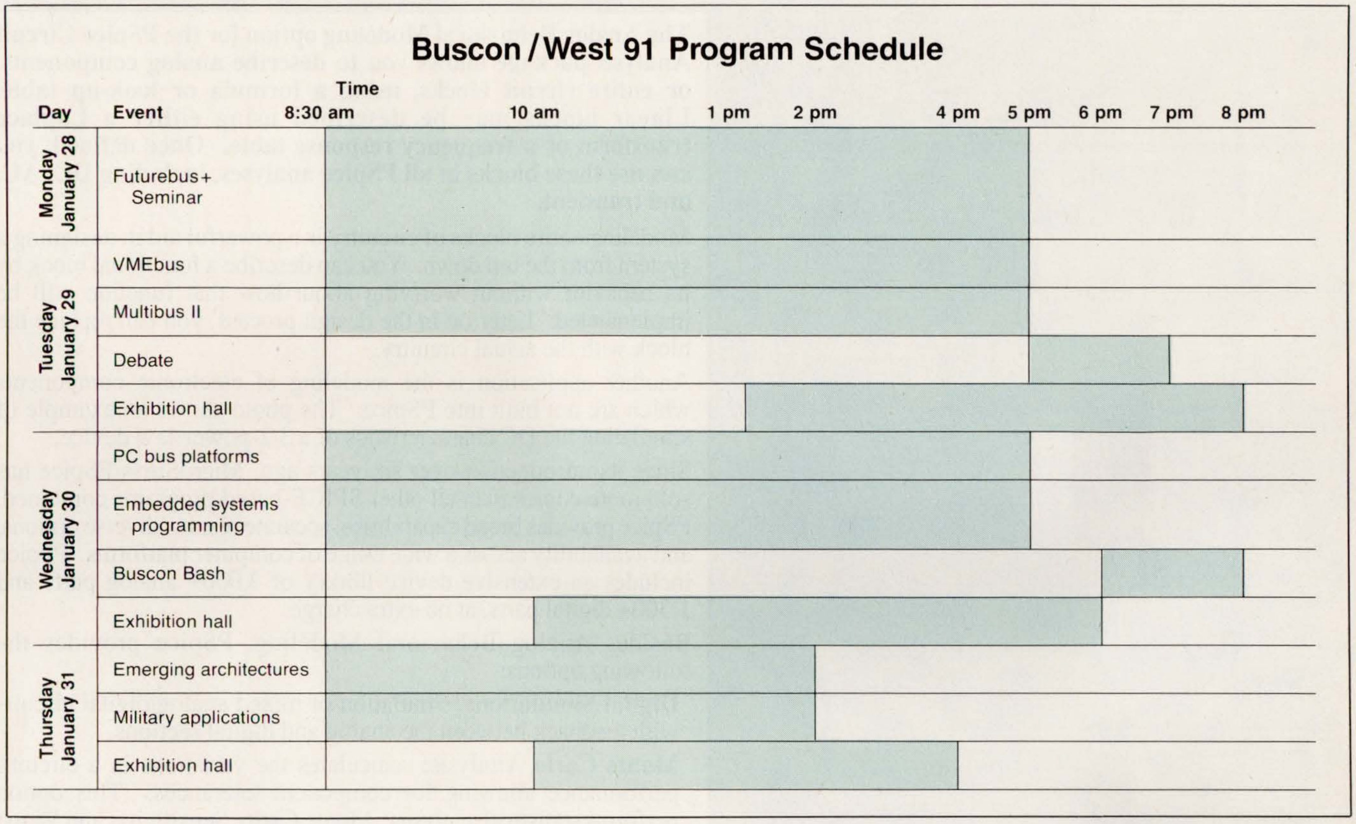
Susan Rose, *Associate Editor*

Like last year, Buscon/West 91 will take place at the Santa Clara Convention Center in Santa Clara, CA. This conference, which brings engineers up to date on bus technology and architecture, will employ the same format used at Buscon/East in Marlborough, MA, last October—that is, the seminars are tightly focused to offer in-depth analysis of each topic. The conference organizers have also extended the hours that the exhibition floor will be open. The show starts on Tuesday, January 29 at 2 pm and runs until Thursday, January 31 at 4 pm. Approximately 70 companies will exhibit their products, including buses, chips, and ports.

The growing importance of Futurebus+ has merited it special attention at this year's show. To avoid conflict with other seminars, a special 1-day Futurebus+ seminar will be held on Monday, January 28—the day before the official opening of the show. The session will examine the new technology and its incorporation into existing applications. Bridging VME and Multibus II to Futurebus+ will also be discussed. (For more information on Futurebus+, see EDN's Special Report in the October 1, 1990, issue.)

The remaining seminars focus on all aspects of a particular technology to give attendees a complete overview. Seminars on Tuesday and Wednesday will last from 8:30 am to 5 pm; Thursday's seminars will last from 8:30 am to 2 pm. The full-day seminars are grouped into morning and afternoon sessions with a lunch break around noon. Both preregistration and on-site registration are available for the seminars.

Tuesday's seminars will cover VMEbus and Multibus II. The VMEbus seminar will review the architecture and theory, then explore the directions the technology will follow. Seminar speakers will also present the comparative advantages of VME as opposed to other buses. The Multibus II seminars will fo-



cus on the capabilities, applications, and performance enhancements of this architecture.

Wednesday's seminars will cover PC bus platforms and embedded systems programming. Bus architectures are the primary topic of the PC bus platforms seminar. In addition to a discussion of ISA, EISA, and MCA, the seminar will look at development environments for the IBM PC and compatible computers. The embedded systems programming seminar will discuss how you can save time and effort in real-time operating-system design. The afternoon session deals with system performance and various development tools that you can use.

Thursday's half-day seminars will cover emerging bus architectures and military applications. Workstation development will be the main focus of the architecture seminar, which will highlight Turbochannel, Sbus, and other buses. The military applications seminar will give attendees a look at what type of applications the military currently needs and what its future requirements may be.

In addition to the seminar schedule, companies are exhibiting their products all three days. The show floor is open until 8 pm Tuesday night so that seminar attendees will have enough time to tour the exhibits. On Tuesday from 5 to 7 pm, you can attend a real-time operating-systems debate, which will focus on trends in the 386 real-time area.

Buscon participants can attend a party on Wednesday night. The Buscon Bash will be held at the Doubletree Hotel from 6 to 8 pm. At the party, the winner of the Buscon Industry Achievement Award will be announced. Your Buscon/West 91 badge is the admission ticket.

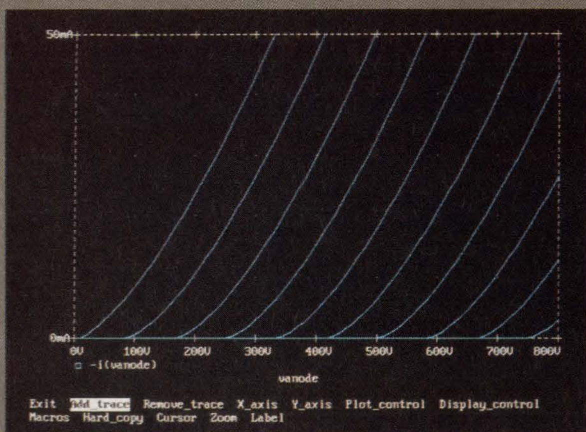
For more information on Buscon/West 91, you can contact Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856. Phone (203) 852-0500; FAX (203) 857-4075. **EDN**

Article Interest Quotient
(Circle One)
High 515 Medium 516 Low 517

PSpice

MicroSim Corporation

The Standard for Circuit Simulation



I-V curves of a triode vacuum tube

Analog Behavioral Modeling

The Analog Behavioral Modeling option for the PSpice Circuit Analysis package allows you to describe analog components, or entire circuit blocks, using a formula or look-up table. Linear blocks may be described using either a Laplace transform or a frequency response table. Once defined, you can use these blocks in all PSpice analyses, including DC, AC, and transient.

Modeling entire blocks of circuitry is a powerful aid in designing a system from the top down. You can describe a functional block by its behavior without worrying about how that function will be implemented. Later on in the design process, you can replace the block with the actual circuitry.

Another application is the modeling of electronic components which are not built into PSpice. The photo shows an example of simulating the DC characteristics of a 3/2-power-law device.

Since its introduction over six years ago, MicroSim's PSpice has sold more copies than all other SPICE-based programs combined. PSpice provides broad capabilities, accurate results, diverse options, and availability across a wide range of computer platforms. PSpice includes an extensive device library of 3,000+ analog parts and 1,300+ digital parts, at no extra charge.

Besides Analog Behavioral Modeling, PSpice provides the following options:

Digital Simulation: simulation of mixed analog/digital circuits with feedback between the analog and digital sections.

Monte Carlo Analysis: calculates the variations in a circuit's performance allowing for component tolerances. This option performs statistical analyses: Monte Carlo, Sensitivity, and Worst Case.

Probe: acts as a "software oscilloscope" to provide an interactive viewing and processing environment for simulation results (see photo).

Parts: is a parameter extraction program allowing the extraction of device model parameters from data sheet information.

PSpice is available on the PC (running DOS, Protected Mode DOS, or OS/2), Macintosh II , Sun 3, Sun 4, and SPARCstation, DECstation 2100, 3100, and 5000, and the VAX/VMS families.

In addition to the Circuit Analysis package, the PSpice family of products also contains the Circuit Synthesis package, which consists of our two filter synthesis products: Advanced Filter Designer and Standard Filter Designer. Filter Designer is an interactive design aid for synthesizing and analyzing active filters. Features include:

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Each copy of our Circuit Analysis and Circuit Synthesis programs comes with MicroSim's extensive product support. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022 or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

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Multibus II programmable logic board serves parallel-interface applications

Six Xilinx programmable gate arrays and 56 TTL transceivers make the MB2-PGA56T board compatible with many parallel interfaces. The Multibus II-compatible card serves applications that require a custom interface or quick turnaround time for the design of an interface card. Optionally, you can specify the board configured as a DEC DRllW-compatible interface capable of DMA transfers.

You can program the interface board to operate as a computer bus link in either DMA or repeater modes. Two of the boards connected back to back can link Multibus II systems. The board supports additional applications such as digital I/O with handshake sequence, counter input, incremental encoder input, and motor controller.

The MB2-PGA56T includes the Intel 82389 message-passing coprocessor IC, implementing full message-passing capability over Multibus II. The board supports 32M-byte/sec data transfers over the bus and includes a facility for interprocessor communications via interrupt message passing. Configuration and diagnostic routines also offer Multibus II interconnect-space compliance.

An 8086 μP controls local operation of the interface board, and the board includes as much as 128k-bytes of RAM and 128k-bytes of EPROM. Onboard firmware supports built-in self-test functions and includes power-up diagnostics. A front-panel LED provides board status information. The board also includes a serial port and two 40-pin flat-ribbon cable connectors.

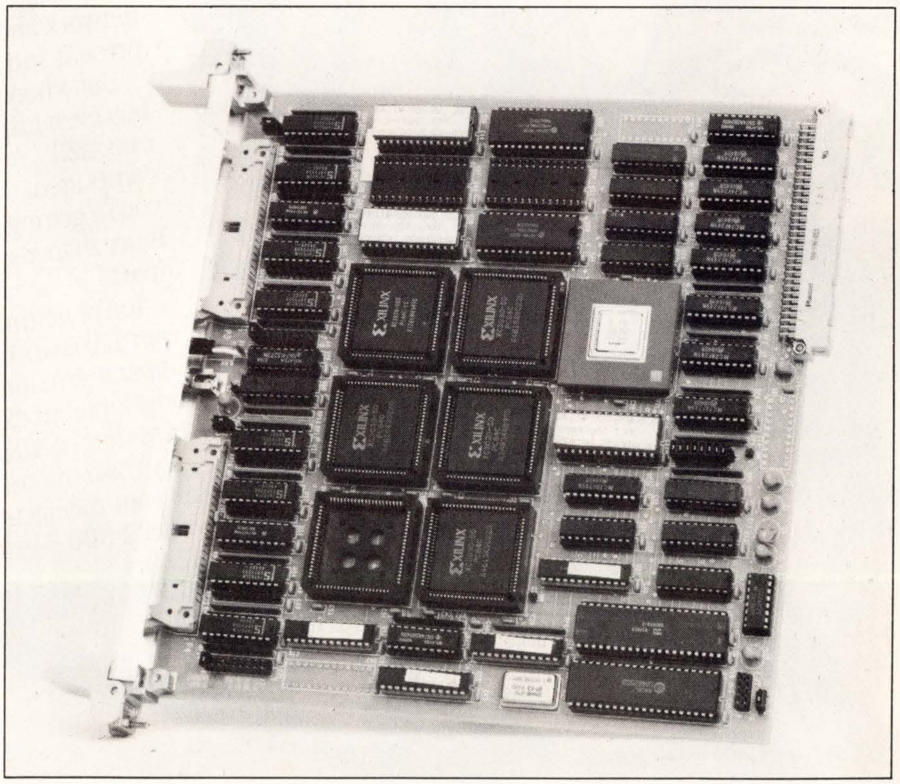
The board accommodates as many as six programmable gate arrays and will accept Xilinx 3020, 3030, or 3042 devices. The maximum configuration yields 864 control logic blocks; each block includes two D flip flops and a 32×2 look-up table. The μP initializes three of the arrays on power-up from onboard firmware. At any time, the controlling μP can program the three arrays that directly connect to the parallel-interface transceivers. The board stores as many as 10 different interface types and can select interface type on the fly under software control.

The board comes with examples of programmed configurations. Sample software and programmable gate-array schematic files are also available. You can buy a source-level debugger to control the board—via the serial port—during testing. A 50-MHz MB2-PGA56T-1 with one 3042 IC, two 3030 ICs, three 3020 ICs, and the optional DR11W software costs $2495.

—Maury Wright

General Standards Co, 8302A Whitesburg Dr, Huntsville, AL 35802. Phone (205) 880-8787. FAX (205) 880-8788.

Circle No. 730



Designing custom parallel interfaces *based on the MB2-PGA56T board simply requires you to program gate arrays. The Multibus II-compatible board includes a local 8086 μP, 128k bytes of RAM, and 128k bytes of EPROM.*

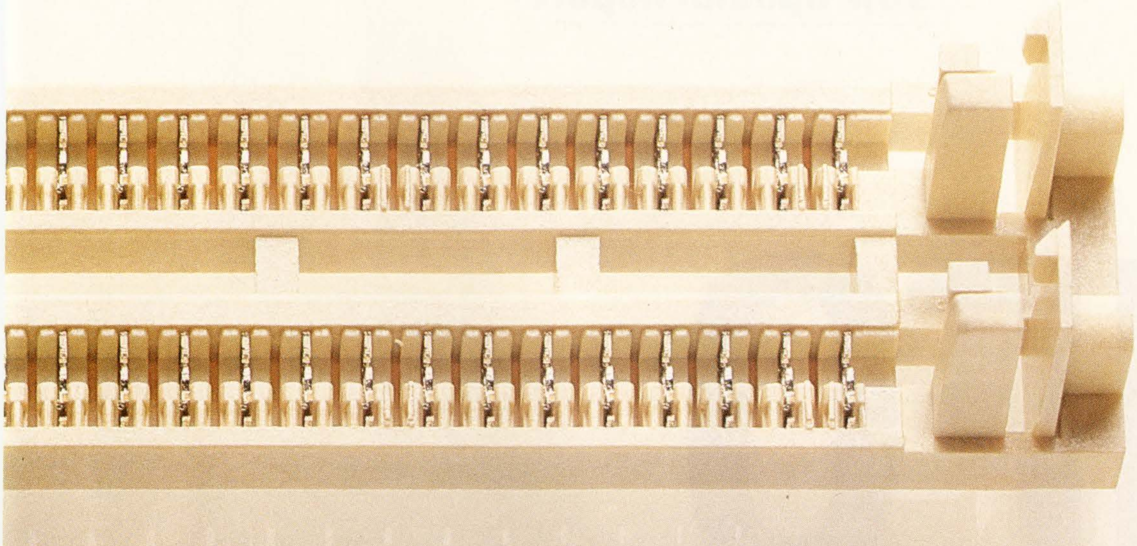
LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	11	11	67	11	0	0	7.3	6.4
Pot-Core	0	22	67	0	11	0	8.8	9.0
Laminate (power)	8	17	67	8	0	0	7.1	7.3
CONNECTORS								
Military panel	17	0	50	33	0	0	9.1	11.7
Flat/Cable	0	80	20	0	0	0	3.9	2.7
Multi-pin circular	13	13	37	37	0	0	9.0	6.9
PC (2-piece)	29	14	43	14	0	0	6.0	5.8
RF/Coaxial	43	29	14	14	0	0	4.1	7.1
Socket	42	17	33	8	0	0	4.3	4.0
Terminal blocks	18	45	37	0	0	0	4.3	5.5
Edge card	33	34	33	0	0	0	3.6	4.1
D-Subminiature	11	45	44	0	0	0	4.8	5.9
Rack & panel	13	38	49	0	0	0	5.0	6.5
Power	0	33	50	17	0	0	7.6	6.1
PRINTED CIRCUIT BOARDS								
Single sided	13	62	25	0	0	0	3.8	4.7
Double sided	0	64	36	0	0	0	4.7	5.0
Multi-layer	0	38	62	0	0	0	6.0	6.2
Prototype	10	70	20	0	0	0	3.6	2.6
RESISTORS								
Carbon film	50	25	25	0	0	0	2.7	4.2
Carbon composition	27	36	27	10	0	0	4.7	5.8
Metal film	33	33	25	9	0	0	4.3	2.6
Metal oxide	60	10	20	10	0	0	3.4	3.5
Wirewound	20	40	30	10	0	0	5.1	5.4
Potentiometers	21	43	21	15	0	0	5.2	5.2
Networks	31	30	31	8	0	0	4.6	3.9
FUSES	50	42	8	0	0	0	1.8	2.1
SWITCHES								
Pushbutton	27	27	36	10	0	0	5.2	5.2
Rotary	14	43	43	0	0	0	4.7	4.8
Rocker	13	49	38	0	0	0	4.5	4.6
Thumbwheel	0	38	49	13	0	0	7.0	5.1
Snap action	17	33	50	0	0	0	4.9	6.3
Momentary	0	60	40	0	0	0	4.9	4.9
Dual-in-line	20	20	60	0	0	0	5.3	5.6
WIRE AND CABLE								
Coaxial	44	44	12	0	0	0	2.2	4.2
Flat ribbon	27	55	18	0	0	0	3.0	3.1
Multiconductor	45	28	27	0	0	0	2.9	4.6
Hookup	60	30	10	0	0	0	1.6	3.2
Wirewrap	33	44	23	0	0	0	3.1	3.3
Power cords	27	36	27	10	0	0	4.7	5.5
POWER SUPPLIES								
Switcher	0	0	83	17	0	0	9.2	7.5
Linear	17	0	66	17	0	0	7.9	7.4
CIRCUIT BREAKERS	17	33	33	17	0	0	6.2	6.1
HEAT SINKS	38	37	25	0	0	0	3.1	4.9
BATTERIES								
Lithium coin cells	40	30	30	0	0	0	3.2	5.2
9V alkaline	33	33	17	17	0	0	4.9	2.5
Real-time clock back-up	40	20	40	0	0	0	3.7	6.4
RELAYS								
General purpose	11	45	44	0	0	0	4.8	5.2
PC board	13	49	38	0	0	0	4.5	4.9

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
Dry reed	13	37	37	13	0	0	6.0	6.5
Mercury	14	57	15	14	0	0	5.0	5.4
Solid state	22	23	22	33	0	0	7.5	8.7
DISCRETE SEMICONDUCTORS								
Diode	43	28	29	0	0	0	3.1	3.7
Zener	29	35	29	7	0	0	4.4	4.3
Thyristor	10	80	10	0	0	0	3.1	4.3
Small signal transistor	22	11	67	0	0	0	5.6	4.5
MOSFET	17	49	17	17	0	0	5.4	4.8
Power, bipolar	29	28	14	29	0	0	6.4	6.0
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	25	37	38	0	0	0	4.1	5.8
CMOS	27	45	28	0	0	0	3.5	4.8
TTL	44	33	23	0	0	0	2.8	4.3
LS	40	40	20	0	0	0	2.7	3.7
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	25	25	50	0	0	0	4.7	7.5
OP amplifier	27	37	36	0	0	0	3.9	5.0
Voltage regulator	27	37	36	0	0	0	3.9	5.3
MEMORY CIRCUITS								
DRAM 16K	33	34	33	0	0	0	3.6	7.0
DRAM 64K	33	34	33	0	0	0	3.6	6.3
DRAM 256K	0	71	29	0	0	0	4.4	4.3
DRAM 1M-bit	22	56	22	0	0	0	3.4	5.1
SRAM 4K × 4	0	60	40	0	0	0	4.9	8.4
SRAM 8K × 8	14	43	43	0	0	0	4.7	5.5
SRAM 2K × 8	25	37	38	0	0	0	4.1	6.6
ROM/PROM	14	43	43	0	0	0	4.7	7.6
EPROM 64K	14	43	43	0	0	0	4.7	5.4
EPROM 256K	29	29	42	0	0	0	4.2	5.6
EPROM 1M-bit	0	60	40	0	0	0	4.9	5.4
EEPROM 16K	0	40	60	0	0	0	5.9	7.5
EEPROM 64K	0	50	50	0	0	0	5.4	6.8
DISPLAYS								
Panel meters	20	40	40	0	0	0	4.3	4.3
Fluorescent	0	20	60	20	0	0	8.4	10.3
CRT 12-in. monochrome	0	33	50	17	0	0	7.6	8.7
LED	30	20	50	0	0	0	4.5	5.4
Liquid crystal	25	13	49	13	0	0	6.3	11.9
MICROPROCESSOR ICs								
8-bit	44	23	33	0	0	0	3.3	4.4
16-bit	20	40	40	0	0	0	4.3	5.6
32-bit	0	50	50	0	0	0	5.4	9.3
FUNCTION PACKAGES								
Amplifier	0	49	38	13	0	0	6.5	5.7
Converter, analog to digital	0	49	38	13	0	0	6.5	7.3
Converter, digital to analog	0	50	50	0	0	0	5.4	8.3
LINE FILTERS	0	14	86	0	0	0	7.2	6.2
CAPACITORS								
Ceramic monolithic	45	36	19	0	0	0	2.5	3.6
Ceramic disc	36	36	28	0	0	0	3.3	3.1
Film	40	20	30	10	0	0	4.5	4.4
Aluminum electrolytic	36	43	14	7	0	0	3.4	4.1
Tantalum	29	43	21	7	0	0	4.0	4.2
INDUCTORS	22	33	33	12	0	0	5.4	3.7

Source: Electronics Purchasing Magazine's survey of buyers.



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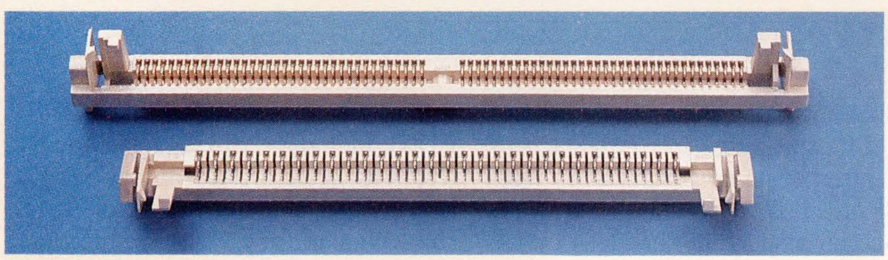

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AMP Interconnecting ideas

FIFO MEMORIES

Evolved from simple buffers, today's FIFO memories provide a link between channels with dissimilar data rates. They smooth over such mismatches as serial vs parallel format, differing bus widths, and speed variations in uni- or bidirectional data flow.

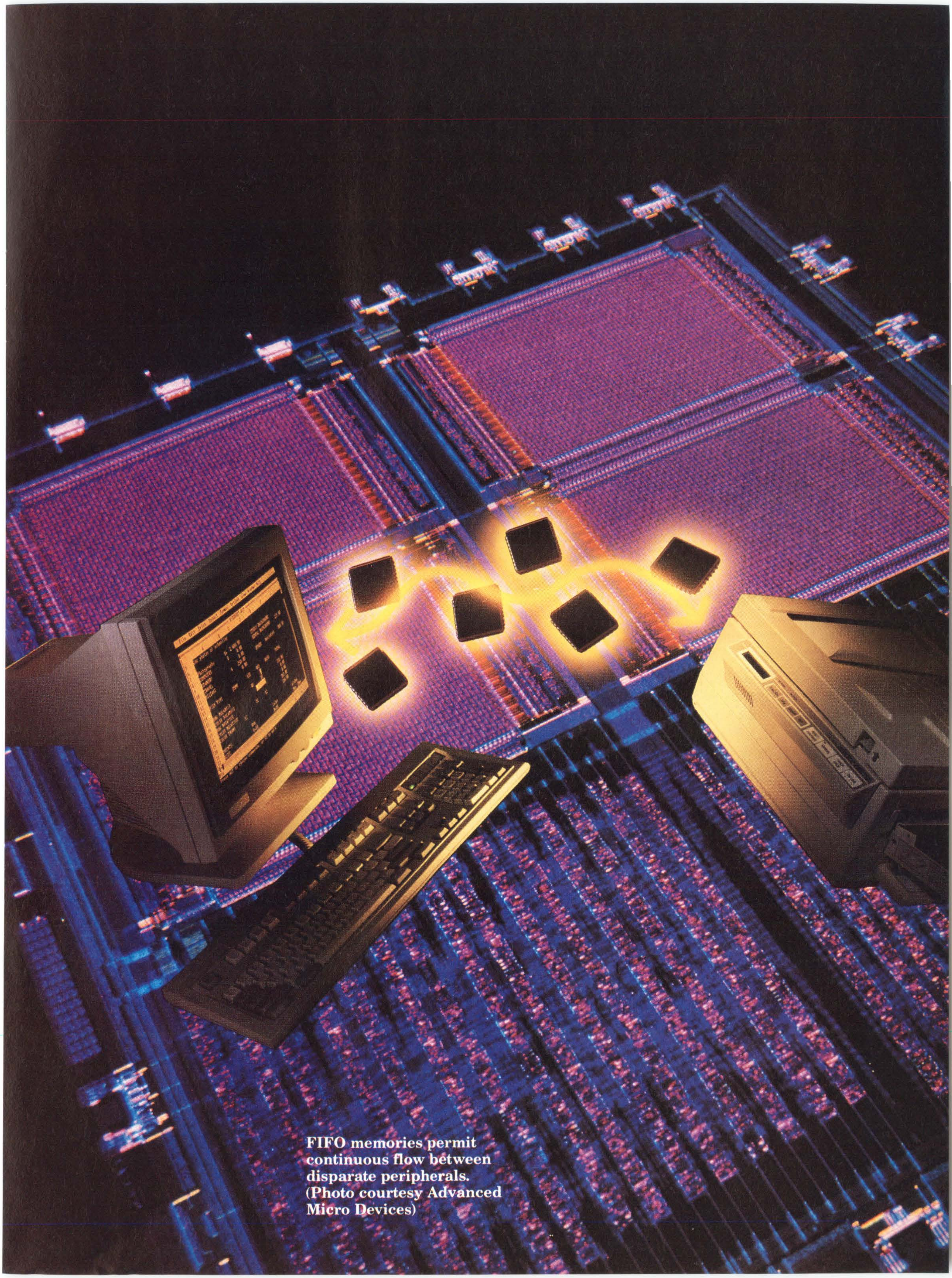
Richard A Quinnell,
Regional Editor

Connecting data buses that operate at different rates can exact a penalty in system performance by forcing one bus to wait for the other. You can avoid that time loss by using a first-in, first-out (FIFO) memory buffer between the two, even if the bus structures are different.

FIFO memories differ from conventional memories in that they don't use an address. You store and read data sequentially. FIFO memories are also dual-ported, accepting data from one port and presenting it to the other. These two features make FIFO memories an ideal buffer for the data flowing between devices operating at different rates.

The earliest FIFO memories had a register-based architecture. When you presented data to the FIFO memory, the device would ripple it through the memory's registers until the data reached one that was empty. The resulting "bubble-through" time slowed the memory's operation and added variability to its performance. These early memories also had a limited data capacity, typically 64×4 bits, and operated at speeds of a few megahertz.

Beginning in 1985, FIFO memories switched to a RAM-based architecture. (See **box**, "Anatomy of a FIFO memory.") These second-generation, RAM-based devices use pointers to keep track of data, eliminating bubble-through. Companies such as Plessey Semiconductor still produce register-based de-



FIFO memories permit continuous flow between disparate peripherals. (Photo courtesy Advanced Micro Devices)

Second-generation FIFO memories feature status flags that warn your system when memory is getting full.

vices, but most of today's FIFO memories are RAM-based, with devices such as the Cypress CY7C400 and Integrated Device Technology IDT72400 series ($8 to $10) replacing the low-density register-based parts. As RAM densities and speeds increased, so have the density and speed of FIFO memories. Devices such as the IDT7205 now hold as many as 8k words and operate with 30-nsec cycle times.

FIFO memories have also added a number of features that expand their utility. One feature that stems directly from the RAM-based architecture is the FIFO memory's ability to retransmit data. Because the data resides in RAM it remains after being read; only the pointer changes to show that the data is

Anatomy of a FIFO memory

The core of a FIFO memory is a RAM array (**Fig A**). Two counters provide address pointers to keep track of data in the array. The read and write pointers, as their names imply, show the next array location to be read from or written to. The array is dual-ported and the two counters are independently clockable, allowing you to read and write data simultaneously at differing rates.

Both counters initialize to 0 when the device resets, and they increment with each read or write pulse. The counters don't stop at the end of physical memory, however. When they reach their maximum value, they roll back to 0 and continue incrementing.

Each counter stops incrementing when it catches up to the other counter. When the read pointer catches the write pointer, you will have read the last word of new data; the FIFO memory is empty. When the write pointer catches the read pointer, the FIFO memory is full. The absolute value of the counters is irrelevant.

Flag logic monitors the difference between the two pointers and sets flags accordingly. When the pointers match, the logic asserts the empty- or full-flag as appropriate. When the difference between the pointers exceeds half the RAM array's depth, the logic asserts the half-full flag.

The expansion logic provides the means of daisy-chaining FIFO memories to achieve greater array depth. Depending on the state of the expansion input line (XI), the FIFO memory will act either as a single device or as part of a chain. A second line, first-load (FL), indicates which in the chain should first accept data following device reset.

When a FIFO memory in the chain is full, it pulses its expansion output signal (XO) during the write cycle to tell the next device in the chain to begin storing data. A device also pulses the XO if it is emptied during a read cycle, telling the next device to begin supplying data.

When wired in a circular chain (one device's XO connected to the next device's XI), the FIFO memories act as a single, large memory. A FIFO memory does not begin accepting data until the one before it in the chain is full and does not supply data until the one before it is empty. The region of valid data, then, rolls through the devices in the chain, much as it rolls through the array in a single device.

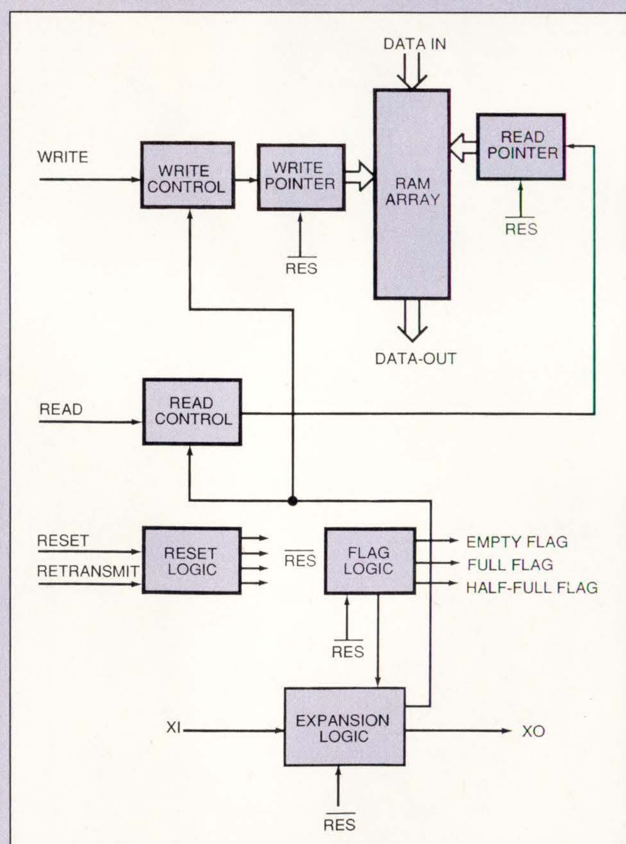
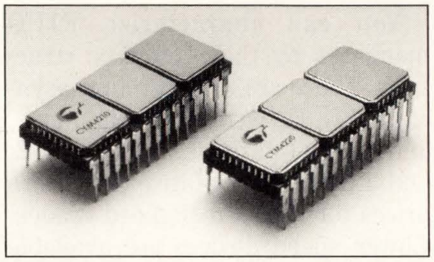


Fig A—Present-day FIFO memories are RAM-based, *using pointers to keep track of data. The RAM-based architecture eliminates the "bubble-through" time required by earlier register-based devices.*

no longer fresh. The retransmit feature allows you to reread that data on command by resetting the read pointer. The write pointer does not change.

If you're building a fault-tolerant system, you may want the ability to reread selected blocks of data. Unless you can empty and reset the FIFO memory between blocks, however, the retransmit feature won't help you. (See **box**, "Retransmit: the hidden flaw.") The IDT72510/20 series solves that problem by offering a reread feature. You mark the beginning of a data block you might want to reread by pulsing a control line before reading the data the first time. The reread command sets the read pointer back to the marked address, allowing you to reread the entire block regardless of the write pointer's location.



***If you just can't wait for high-density FIFO memory ICs**, Cypress Semiconductor's Multichip Technology division offers these 8k- and 16k-word-deep FIFO memory modules. The modules' pinouts are identical to the monolithic ICs that will eventually replace them.*

Another feature added by second-generation FIFO memories is the use of status flags. FIFO memories tell you when they're full or empty. High-speed and pipelined systems, however, may overflow the FIFO memory because they do not receive the flag in time to stop. The system may underflow for the same reason when emptying memory. Status flags give such systems warning that the FIFO memory is filling up. By monitoring the status flags you can begin corrective action before the FIFO memory reaches its limits.

There are three types of status flags: half-full, almost-full, and almost-empty. The simplest FIFO memories have a half-full flag, which asserts when the FIFO memory is filled beyond half capacity. If your system requires only a few write cycles to react and begin emptying the FIFO memory you can never use the FIFO memory's other half.

Retransmit: the hidden flaw

There is a catch to avoid when using a FIFO memory's retransmit feature. The RAM in a FIFO memory operates as a circular stack, as shown in **Fig A**. As you read from and write to the device, the pointers roll through the absolute address space. The retransmit command, however, sets the read pointer to the beginning of the address space, and you reread from there.

The problem comes when you read and write a sequence of data blocks. Reading data from the FIFO memory doesn't affect the write pointer. If you have read some of the FIFO memory's data, the write pointer will continue to advance beyond the end of physical memory, wrapping around to the beginning. The FIFO memory is only full when the two pointers meet; their absolute value is irrelevant.

Once the total number of words written to the FIFO memory exceeds its rated capacity, even though subsequent reads have kept the FIFO memory from filling, the retransmit command will return only the portion of the data that wrapped around. You can only prevent the wrap-around by resetting the FIFO memory, which clears both pointers.

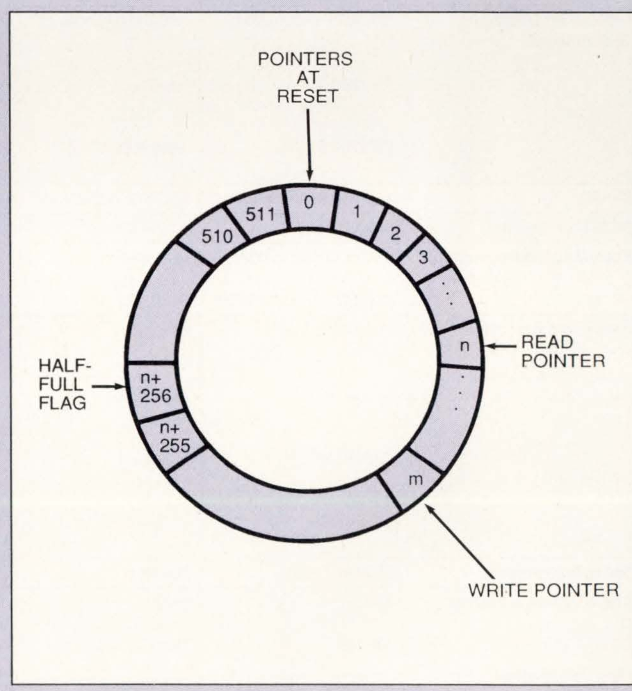


***Fig A—Operating as a circular stack**, the FIFO memory's pointers keep track of current data. Only 2 bytes remain in the FIFO memory, regardless of the write pointer's absolute value.*

Circuit noise accounts for more than half the problems designers experience when using FIFO memories. A 2-nsec glitch can disturb a FIFO memory's pointers.

The almost-full flag provides a better solution if your system can react to the flag before the memory fills completely. There is no standard definition for the almost-full flag. The flags assert themselves anywhere from ⅞ full to the full 7 bytes, depending on the device. Because the optimal placement of a status flag will vary with the system's data rates and reaction time, a number of devices now include programmable status flags.

You can characterize FIFO memories by their interface structure. There are three groups: asynchronous, clocked (or synchronous), and special-purpose. **Tables 1**, **2**, and **3** list representative parts with prices for the fastest speed grades. Lower speed devices are available at a lower cost for many product families.

The asynchronous FIFO memory is the most commonly available type. The general read/write timing for an asynchronous FIFO memory is shown in **Fig 1**. Although devices such as the Samsung KM75C03A offer cycle times as short as 20 nsec, asynchronous types become difficult to use at such high data rates.

For one thing, you must provide pulse shaping logic in order to minimize cycle time while meeting minimum read and write pulse widths. Further, it may be difficult to ensure that your circuit meets the device's data setup and hold

Table 1—Asynchronous FIFO memories

Company	Part Number	Organization	Minimum Access Time (nsec)	Minimum Cycle Time (nsec)	Flags	Special Features	Price (1000)
Advanced Micro Devices	Am4601	512×9	25	35	Programmable		$14.90
	Am7202A/03A/04A/05A	1k/2k/4k/8k×9	15	25	HF	Retransmit	$27–$79.40
Cypress Semiconductor	CY7C420/24/28/32	512/1k/2k/4k × 9	20	30	HF	Retransmit, Output enable	$15.55–$34.80 (100)
Dallas Semiconductor	DS2009	512×9	35	45	HF	Output enable	$5.15
	DS2010/11/12/13	1k/2k/4k/8k×9	50	65	HF	Output enable	$7.50–$31.50
Integrated Device Technology	IDT7200/01/02/03/04	256/512/1k/2k/4k×9	15	25	HF	Retransmit, Output enable	$5–$75
	IDT7205	8k×9	20	30	HF	Retransmit, Output enable	$90
	IDT72021/31/41	1k/2k/4k×9	25/35/35	35/45/45	HF, AEF	Retransmit, Output enable	$8–$40
Mosel	MS7200/01A/02A/03/04	256/512/1k/2k/4k×9	25	33	HF	Retransmit	$10.80–$23.80
SGS-Thompson	MK45H01/02/03	512/1k/2k×9	25	35	HF	Retransmit	$16.66–$30.98
Samsung Semiconductor	KM75C01A/02A/03A	512/1k/2k×9	15/25/12	25/35/20	HF	Retransmit	$15–$34
	KM75C101A/102A/103A	512/1k/2k×9	20	30	Programmable	Retransmit	$15–$34
Sharp Microelectronics	LH5481/91	64×8/9	N/A	28	HF	Retransmit, Output enable	$22.86
	LH5485/95	256×8/9	N/A	28	HF	Retransmit, Output enable	$34.29
	LH5496/97	512/1k×9	15	25	HF	Retransmit, Output enable	$20.28
	LH5498/99	2k/4k×9	20	30	HF	Retransmit, Output enable	$30–$51
Texas Instruments	SN74ACT7801	1k×18	15	22	Programmable	Output enable	$68
Vitelic Semiconductor	V61C01	512×9	35	45	HF	Retransmit	$11
	V61C02	1k×9	40	50	HF	Retransmit	$14

Flag Definitions:
HF = Half full
AE = Almost empty
AF = Almost full
AEF = Asserted if near empty or near full

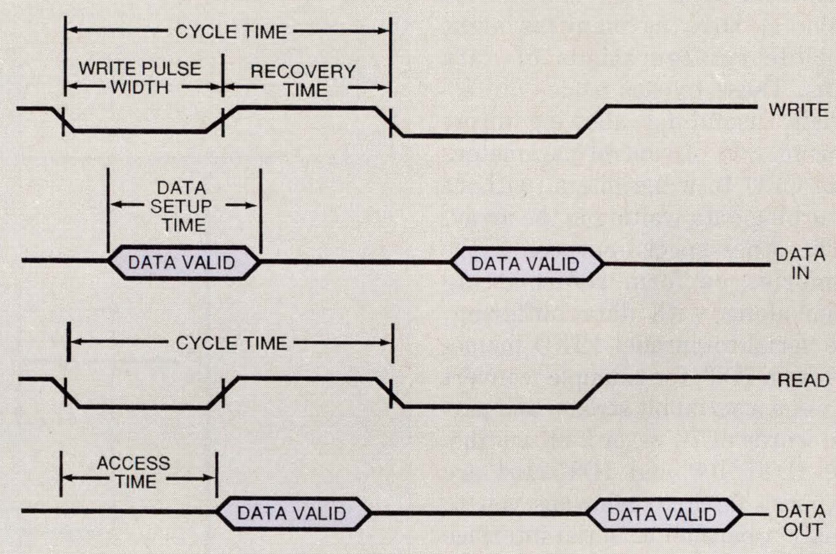
conditions. In the case of the KM75C03A, for example, the data setup time is 8 nsec, allowing only 4 nsec for new data to become available and stable between write pulses.

Synchronous design techniques simplify meeting such timing constraints at high speeds. Manufacturers, therefore, are now offering clocked FIFO memories with synchronous read/write interfaces. Such devices are best suited for high-speed systems and offer cycle times as low as 14 nsec. The term "synchronous" applies only to the nature of each port's I/O timing. The two ports of a clocked FIFO memory can still operate independently; each port has its own clock input pin.

Special-purpose FIFO memories are the third group. These devices offer an asynchronous I/O interface and tackle a variety of special applications. The most common member of the group is the bidirectional-FIFO memory.

Most FIFO memories are unidirectional; data flows in one port and out the other. Bidirectional-FIFO memories, on the other hand, allow you to read from or write to either port with equal ease. Most have two internal RAM arrays, one for each direction. An exception is the Cypress CY7C439, which only has one array. You can configure the CY7C439 to buffer data in either direction, but not simultaneously. The device allows you to send data in the opposite direction, either directly from port to port or latched in an on-chip register.

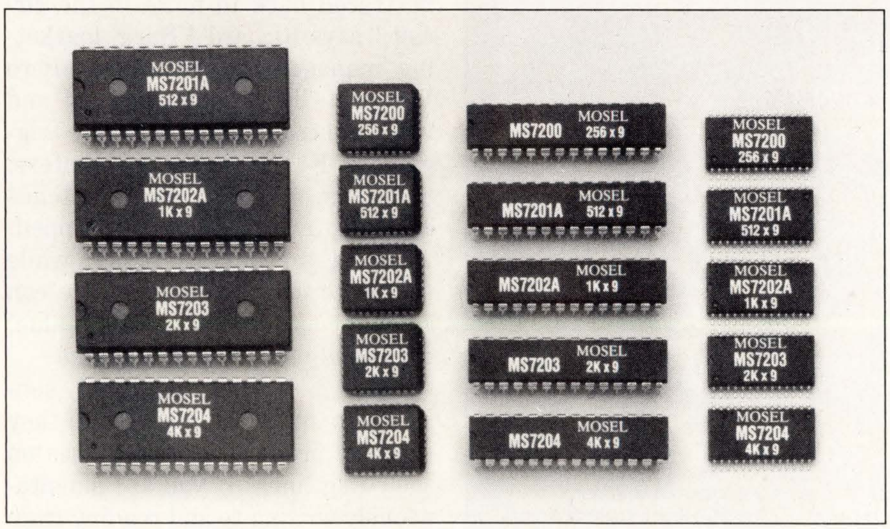
Many bidirectional FIFO memories have some form of bypass, a method for sending data from one port to another without passing through the RAM array. The de-



KM75CO3A TIMING

CYCLE TIME	20 nsec
WRITE PULSE WIDTH	12 nsec
DATA SETUP TIME	8 nsec
RECOVERY TIME	8 nsec
ACCESS TIME	12 nsec

Fig 1—Timing becomes critical at high speeds *when writing to asynchronous FIFO memories. The data setup time is nearly as long as the device's cycle time.*



FIFO memories come in a variety of package styles, *as this photo from Mosel Corp's family album shows. Most FIFO memory manufacturers offer both DIP and surface-mount package options.*

Daisy-chaining devices allow you to form deep FIFO memory buffers. You may pay a performance penalty, however.

vices from Texas Instruments, for example, have as many as eight possible configurations of data paths. These bypass modes are especially useful for allowing direct transmission of control parameters from CPU to a peripheral without disturbing data waiting in the array.

The other special-purpose FIFO memories perform reformatting tasks along with data buffering. The serial-to-parallel FIFO memories from IDT, for example, convert between a serial bit stream and parallel words of 7-, 8-, or 9-bit widths. The IDT72103 and IDT72104 are the most flexible, allowing you to specify a parallel or serial interface for either port.

The various FIFO memory structures promise to simplify the connection of virtually any two data buses. Following a few design guidelines will ensure that the devices fulfill that promise. The most important of these guidelines is noise control in the circuit.

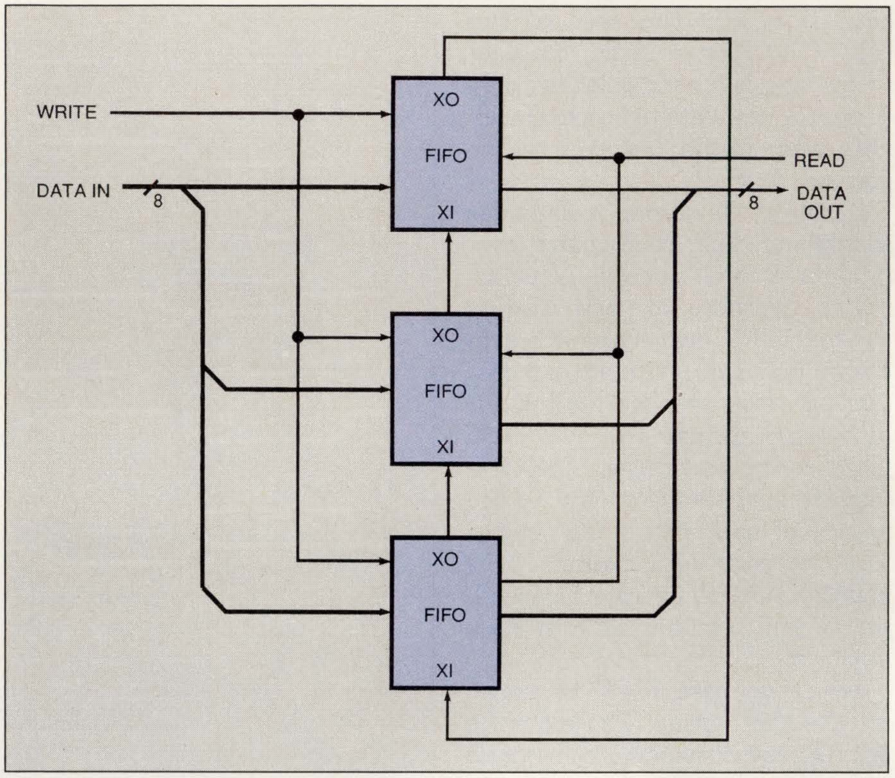


Fig 2—If you need to add more depth to your FIFO memory buffer *you'll have to connect the devices in a daisy chain as shown. Doing so, however, can exact a performance penalty and adds loading to the data buses.*

Table 2—Clocked FIFO memories

Company	Part No.	Organization	Minimum Cycle Time (nsec)	Flags	Special Features	Price (1000)
Cypress Semiconductor	CY7C441/43	512/2k×9	14	HF, AE, AF		$25.80
	CY7C451/53	512/2k×9	14	Programmable	A, B, C	$30
Integrated Device Technology	IDT72200/10	256/512×8	15	AE, AF (Note 1)	A	$12–$73
	IDT72201/11	256/512×9	15	Programmable	A	$12–$73
	IDT72215/25	512/1k×18	20	HF	A	$12–$73
	IDT72420	64×8	15	AE, AF (Note 1)	A	$12–$73
	IDT72421	64×9	15	Programmable	A	$12–$73
SGS-Thompson	MK4505	1k×5	25	HF, AE, AF (Note 2)	B	$35.28
Sharp Microelectronics	LH5492	4k×9	25	HF, AE, AF (Note 3)	A	$64.81

Notes:
1. Flags assert 7 words from empty/full
2. Flags assert 11 words from empty/full
3. Flags assert 8 words from empty/full

Flag Definitions:
HF = Half full
AE = Almost empty
AF = Almost full
AEF = Asserted if near empty or near full

Special Feature Definitions:
A = 3-state outputs
B = Expandable in depth
C = Built-in parity generation and checking

"Almost half of the problems users have with FIFO memories can be traced back to noise in the circuit," says Richard J Burg, marketing manager for Advanced Micro Devices. Glitches on the read and write control lines can falsely trigger the FIFO memory's counters, he notes. At best those glitches cause data to be added or skipped. At worst, a 1- or 2- nsec glitch while the write control line is active can set the counter to a random value, completely scrambling the data.

FIFO memories are not only sensitive to narrow pulses, but they can also produce narrow pulses on their flag lines. If you are simultaneously writing to and reading from an asynchronous FIFO memory, the device will assert a flag based on signals from one port and clear the flag based on the other. Depending on the relative timing of the two ports, the flag line may produce an arbitrarily small pulse. Using synchronous logic to sense and register the flag lines will avoid propagating these narrow pulses through your system.

Daisy-chaining deepens FIFO

If your design calls for a FIFO memory deeper than any available, you have several problems to overcome. You expand asynchronous FIFO memories in depth by daisy-chaining several devices together. **Fig 2** shows the wiring for depth expansion. When one device fills or empties, it produces a pulse on its output signal (XO) line to signal the next FIFO memory in the chain to take over. If you're running the FIFO memories at their full-rated speed, the delays inherent in generating XO may be enough to cause the next device in the chain to miss a read or write pulse during the handoff. Slowing down the data rate is the only solution.

Daisy chaining the FIFO memories carries other penalties. Each device in the chain connects to the input and output buses. The longer the chain, the greater the load presented by the FIFO memory. That loading could lower your system's speed even further. Finally, daisy chaining eliminates the half-full-flag and retransmit features.

Most currently available clocked FIFO memories are not expandable in depth. Two exceptions are the Cypress CY7C451 and the SGS-Thompson MK4505. The CY7C451 has expansion logic similar to that of asynchronous FIFO memories. The MK4505 has handshake signals that allow you wire the devices in cascade, then clock data through one FIFO memory into the next.

If you need both additional depth

Table 3—Special-purpose FIFO memories

Company	Part Number	Type	Organization (Note 1)	Minimum Access Time (nsec)	Minimum Cycle Time (nsec)	Flags	Special Features	Price (1000)
Advanced Micro Devices	Am4701	Bidirectional	2×512×8	35	45	Programmable	C	$22.30
Cypress Semiconductor	CY74C439	Bidirectional (half duplex)	2k×9	25	35	HF	C	$27 (100)
Integrated Device Technology	IDT72103/04	Configurable P/S	2k/4k×9	35	45	HF, AE, AF	B, D	$10–$38
	IDT72105/15/25	Parallel-to-serial	256/512/1k×16	15	25	HF, AE, AF	D, F	$10–$38
	IDT72131/41	Parallel-to-serial	2k/4k×9	35	45	HF, AE, AF	D, G	$10–$38
	IDT72132/42	Serial-to-parallel	2k/4k×9	35	45	HF, AE, AF	D, G	$10–$38
	IDT72510	Bus-matching	512×18 to 1k×9	35	45	Programmable	B, C, E, H	$35–$80
	IDT72520	Bus-matching	1k×18 to 2k×9	35	45	Programmable	B, C, E, H	$35–$80
	IDT72511	Bidirectional	2×512×18	35	45	Programmable	B, C, H	$35–$80
Mosel	MS72105/15	Parallel-to-serial	256/512×16	25	35	HF, AEF	D, F	$15–$20
Sharp Microelectronics	LH5420	Bidirectional	2×256×36		25	Programmable		$75
	LH5493	Parallel-to-serial	4k×9		25	HF, AE, AF		$62.86
	LH5494	Serial-to-parallel	4k×9		25	HF, AE, AF		$62.86
Texas Instruments	SN74ACT2235	Bidirectional	2×1k×9		25	Programmable	A	$52
	SN74ACT2236	Bidirectional	2×1k×9		25	Programmable	A	$52
	SN74ALS2238	Bidirectional	2×32×9	12.5	22.5	Programmable	A	$52

Notes:
1. Unless noted, devices expandable in width only
2. Serial FIFO memories clock at 50 MHz

Flag Definitions:
HF = Half full
AE = Almost empty
AF = Almost full
AEF = Asserted if near empty or near full

Special Feature Definitions:
A = 3-state outputs
B = Retransmit
C = Bypass path available
D = Expandable in depth
E = Build-in parity generation and checking
F = Programmable serial bit order
G = Programmable parallel word width
H = DMA interface

and full speeds, and don't want the design hassles, consider using a multichip module. Multichip Technology, a subsidiary of Cypress Semiconductor, offers FIFO memories as deep as 16k words in a DIP module. These modules foreshadow monolithic devices in development at Cypress, insuring that you can later replace the modules with ICs.

Of course, you could just wait for additional choices. Devices as large as 32k words deep are presently in development and will be available in 1991, as will clocked versions of special-purpose FIFO memories. **EDN**

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Manufacturers of FIFO memories

For more information on the FIFO memories described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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FAX (408) 982-7490
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Cypress Semiconductor
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San Jose, CA 95134
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4401 South Beltwood Pkwy
Dallas, TX 75244
(214) 450-0448
FAX (214) 450-0470
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Integrated Device Technology Inc
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Santa Clara, CA 95052
(408) 727-6116
FAX (408) 988-3029
Circle No. 653

Mosel Corp
914 W Maude Ave
Sunnyvale, CA 94086
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Multichip Technology
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FAX (408) 432-7049
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Carrollton, TX 75006
(214) 466-6000
TLX 730643
Circle No. 658

Sharp Electronics Corp
Microelectronics Div
Sharp Plaza
Mahwah, NJ 07430
(201) 529-8757
FAX (201) 512-2020
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Semiconductor Group
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Dallas, TX 75380
(800) 336-5236, ext 700
Circle No. 660

Vitelic Semiconductor
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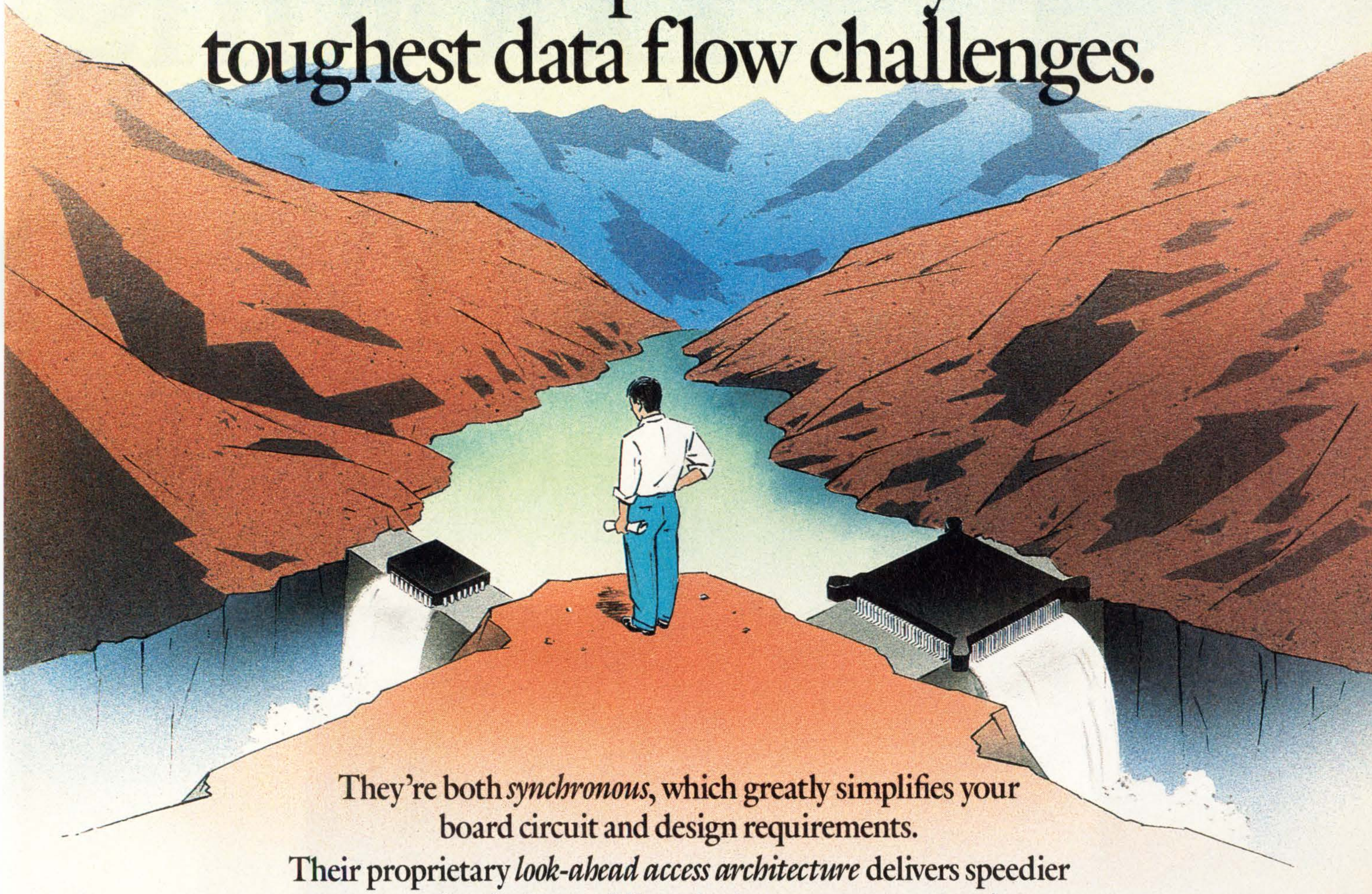
Two state-of-the-art FIFOs from Sharp to solve your toughest data flow challenges.



They're both *synchronous*, which greatly simplifies your board circuit and design requirements. Their proprietary *look-ahead access architecture* delivers speedier access and cycle times while reducing power consumption.

Introducing: The LH5492 4K x 9 Clocked FIFO.

Sharp's new LH5492 is a dual-port clocked FIFO, with a 4K x 9 configuration. The clocked interface is a significant enhancement in FIFO design over previous asynchronous parts. The clocked enables on the LH5492 eliminate the requirement to shape waveforms, resulting in simpler design tasks, and lower parts count.

Its high-speed clocked interface can be used directly with the typical 40%/60% duty cycle system clock. And a separate $\overline{OE}$ control signal provides independent control over output buffers.

The second enable pin on each part can be directly tied to the flags to simplify external logic requirements.

The LH5492 4K x 9 clocked FIFO comes in a 32-pin PLCC. It is available with access times of 20 ns, 25 ns and 35 ns, and cycle times of 25 ns, 35 ns and 50 ns, respectively.

Introducing: The LH5420 256 x 36 x 2 Bidirectional FIFO.

Sharp's new LH5420 is actually two 256 x 36-bit FIFOs in one. Operating in parallel but opposite directions to provide bidirectional data buffering that would normally require multiple independent devices.

Its 36-bit word width is an industry first. And ideal for interfacing with new generation higher-speed 32/36-bit and 64/72-bit microprocessors and buses. Moreover, a choice of 9, 18, or 36-bit word widths on Port B means efficient word width matching.

Programmable Almost Empty and Almost Full status flags on each port—in addition to Full, Half Full and Empty flags—allow you to either leave the flags set at their initialized setting of 8, or program them over the entire FIFO depth.

The LH5420 comes in a 132-pin plastic QFP package. It is available with access times of 15 ns, 20 ns and 25 ns, and cycle times of 25 ns, 30 ns and 35 ns, respectively.

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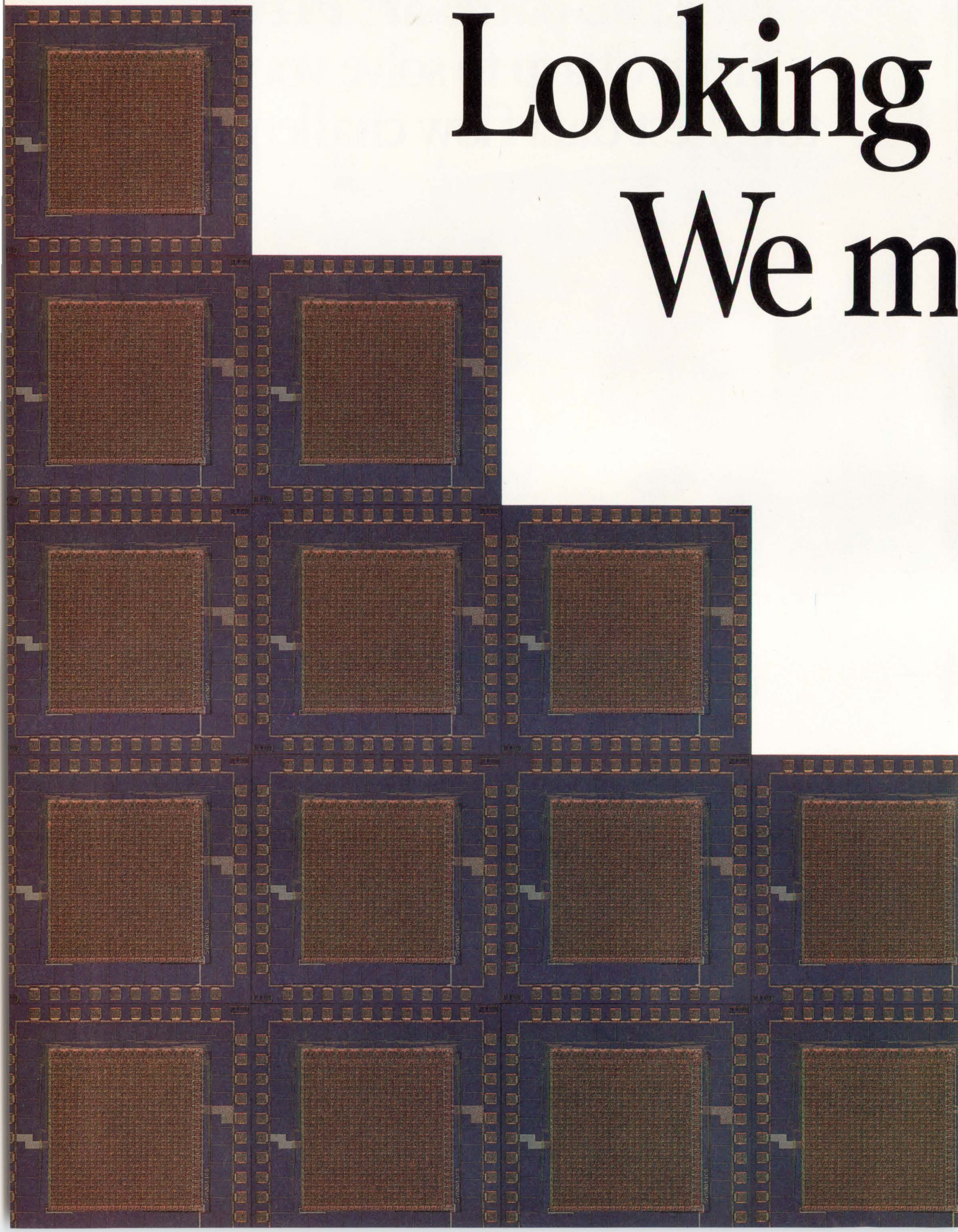

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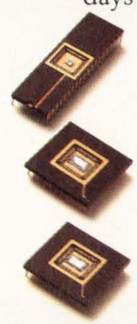

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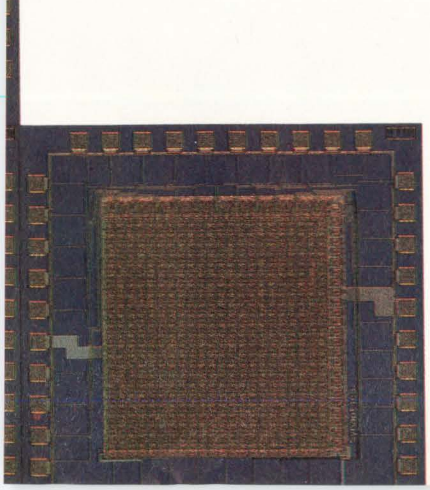

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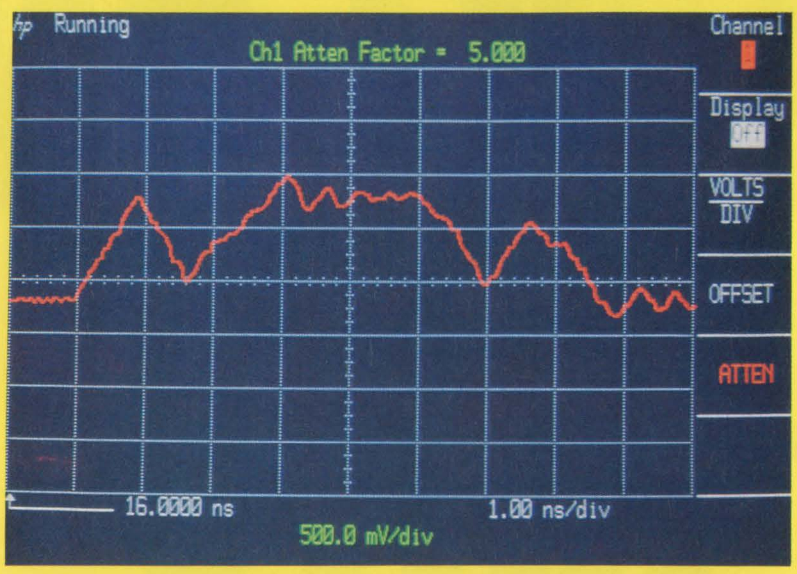

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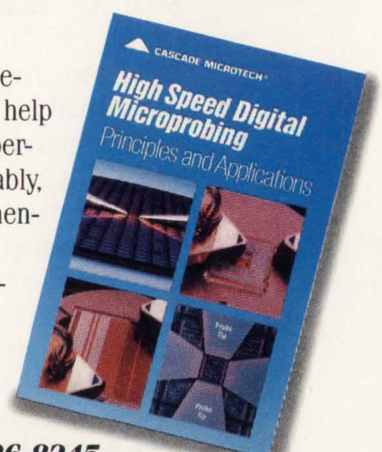

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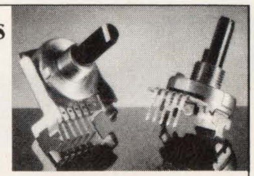

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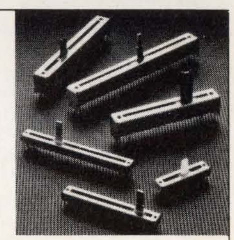

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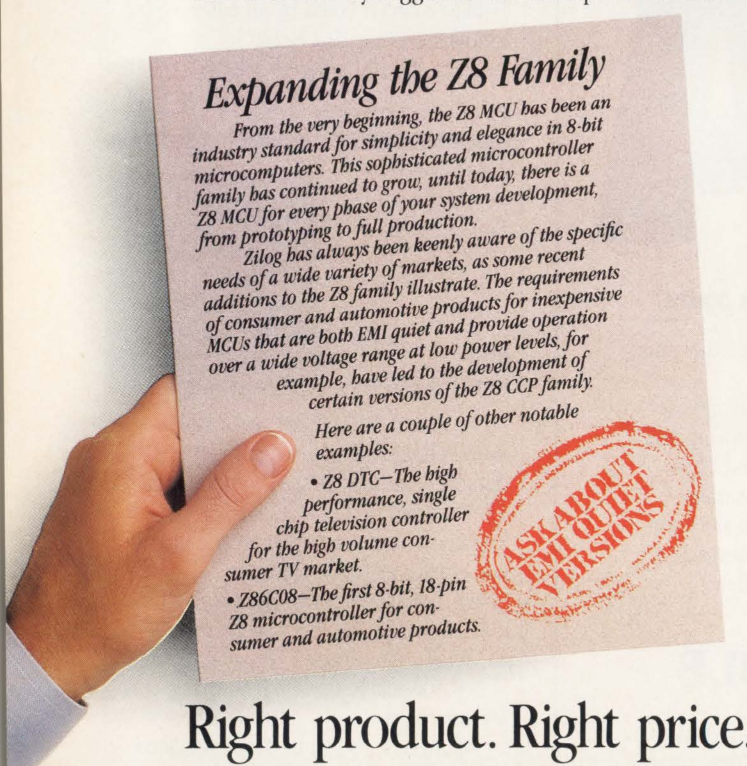

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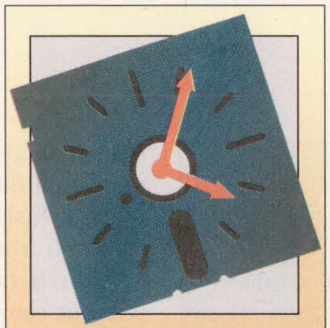

REAL-TIME PROGRAMMING PART 8

Message buffers and mailboxes

The discussion of task coordination methods continues in Part 8 of this series with an overview of how message buffers and mailboxes coordinate tasks in real-time applications. Parts 9 and 10 will discuss several other methods of task coordination.

David L Ripps, *Industrial Programming Inc*

You have already seen in the discussion of the overall organization of a real-time application that message passing is a fundamental method of coupling tasks (see pg 196 in Part 4 of this series, EDN, October 25, 1990). Normally, the coupling involves the passing of information, such as a packet of parameters for some work to be done, or the state of a job that is being performed in stages by a sequence of tasks. The coupling also involves coordination. For a receiver, this means the ability to wait for a message to arrive; for a sender, this means the ability to wait for a message to be received. Thus, even if the content of the message is empty (0 bytes long), message passing can still be used to coordinate the activity of tasks.

An event flag can also couple tasks, but with the information restricted to a single bit. In the limit, a message without content also carries a single bit of information: It is present at an exchange or not. Even so, coordination via event flags and messages is essentially different. When an event flag is set, all tasks that are waiting for that event continue, and the event flag still remains set for any tasks that come later to examine it. With a message, the task that receives it consumes it; if there are two tasks waiting for a message, only one continues while the other remains waiting.

In designing the OS, each message exchange could have been permanently tied to its parent task, as was done with the local event-flag group. Had this been done, sending a message to an exchange would have been tantamount to sending it to a designated receiving task. But such an arrangement is too limiting. Real-time applications often require the sharing of work among multiple, equivalent tasks. This sharing can be especially important if there are multiple processors in the system, so that separate pieces of work can be processed simultaneously. Load sharing can even be beneficial for single-processor systems when each piece of work may be suspended because of I/O or other inherent delays. (Recall **Fig 1**'s Rule B from Part 4 of this series EDN, October 25, 1990, pg 194: Try to keep the processor (or processors) always busy with productive work.)

Within the MTOS operating system, the arrangement for message passing is the analog of the bank queue with one line and (possibly) multiple servers. Each exchange is a separate object, distinct from the tasks that send and receive the messages. In principle, any task can send a message, and any task can receive a message. (Of course, application designers usually

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Only one task can receive a particular message. Other tasks waiting for messages must continue waiting.

impose task-level restrictions, but these are outside the operating system.) Thus, if two tasks can perform a given type of processing, each will seek the next available message from a common exchange. The message exchange is thus an implementation of the multiple producer/multiple consumer model of intertask communication (**Fig 1**).

Message exchange plays a central role in many real-time applications. As a result, MTOS-UX provides two different realizations of an exchange: a message buffer and a mailbox. The message buffer is the quickest and simplest mechanism for passing messages; the mailbox provides additional facilities.

A message buffer (MSB) is a place to which a message may be sent and from which a message may be received. The number of MSBs and the kinds of messages transferred are completely determined by the application; the OS imposes no restrictions of its own.

An MSB message is always the size of a single pointer variable (6 bytes for the 80386; 4 bytes for all of the others). Often the message is the address of a structure containing the parameters of some work to be done. However, the content of the message is not significant to the OS; the value is transferred without regard to its possible meaning.

A message buffer is a storage device; when there is no receiver immediately available, the 4- or 6-byte message is copied into the buffer. The maximum number of messages is specified when the buffer is created. A task that attempts to post a message to a full buffer is given a failure return value of **QUEFUL**. Similarly, when a task receives a message the 4 or 6 bytes are removed from storage.

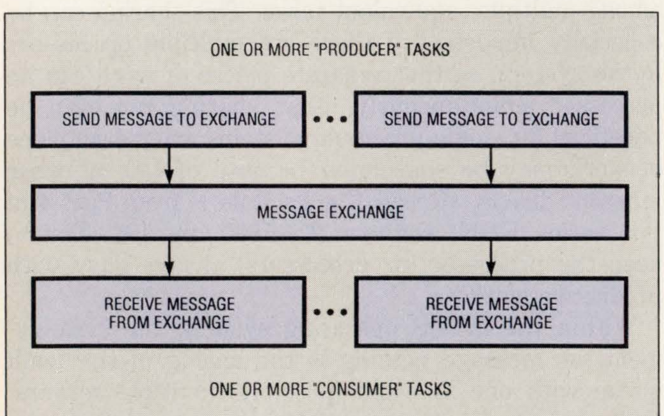

Fig 1—The message exchange—message buffers or mailboxes—allows multiple "producer" tasks to communicate with multiple "consumer" tasks.

After a task posts a message, it always continues without coordination. The only option at the send end is whether the message should be placed at the end of the buffer (FIFO) or at the beginning of the buffer (LIFO) in case there is no task already waiting to receive the message. An MSB message does not have a priority.

A task seeking a message at an empty MSB can either wait for the next message to arrive or continue and be notified that no message is currently available. These wait options enable tasks to coordinate their activities.

Typical use of a message buffer

As an illustration of the utility of message buffers, consider an application in which there are three tasks that produce blocks of parameters. Each block must be expanded into a formal report that is to be output to one of two identical printers. It is not important to specify the printer to be used for a given report. It is important, however, that a printer not be idle while a block of parameters is available.

Each producer task allocates a work area from a memory pool, builds a parameter block in the area, and then sends the address of the area as a message to a certain MSB (**Fig 2**). The producer does not wait for the message to be received and thus is immediately available to prepare the next block (**Fig 3**).

Two tasks do the report generation and printing. Each task executes the same re-entrant code, but has

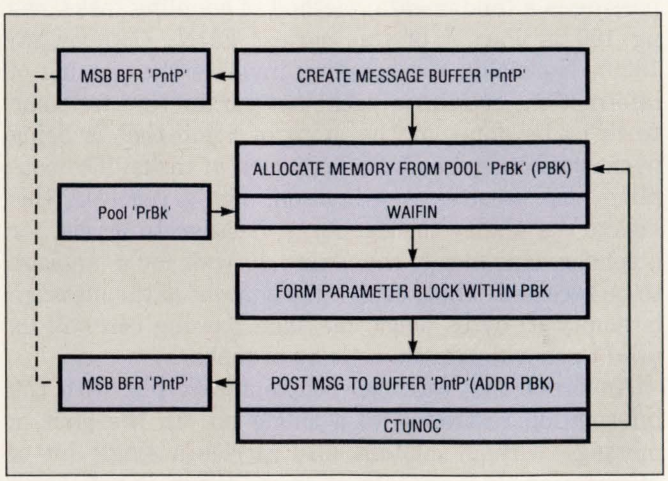

Fig 2—A typical producer task requests allocation of memory for a parameter block that will contain information the task needs to convey. The task waits (WAIFIN) for the OS to allocate the memory, then posts the parameter-block address to a message buffer and continues with no coordination (CTUNOC).

its own dedicated printer. A printer task seeks the address of a parameter block as a message from a common MSB. (If there is no message queued, the task waits.) When the printing is completed, the printer task deallocates the work area and then seeks the next message in an endless loop.

Thus, the MSB provides an orderly way to coordinate the producers and printers. Specifically, it allows the producer to send work to the next free printer, without knowing which one that is.

The parameter blocks need not all be of the same size or come from the same pool. Usually, they are not. Part of the parameter block can specify the length of the work area and the identity of the pool.

Creating a message buffer

A message buffer must be created before any task can use it. For a single-processor system, a typical create call is

```
#define MSBO 0x4D534230

long int msbid0;          /*identifier of message buffer 0*/

msbid0 = crmsb (MSB0,50L);
```

The first parameter is the key associated with the message buffer. It is the external name of the buffer. A 4-byte pattern unique among MSBs is required. The second parameter indicates the maximum number of messages that can be stored. The low-order 13 bits are used so that the highest value is 8191.

If an MSB with the given key does not already exist, it is created by this request. The only return values are the MSB identifier for success and **QUEFUL** or **BADPRM** for failure. The successful return value does not distinguish an MSB that already existed from one that was just created. An MSB is created empty.

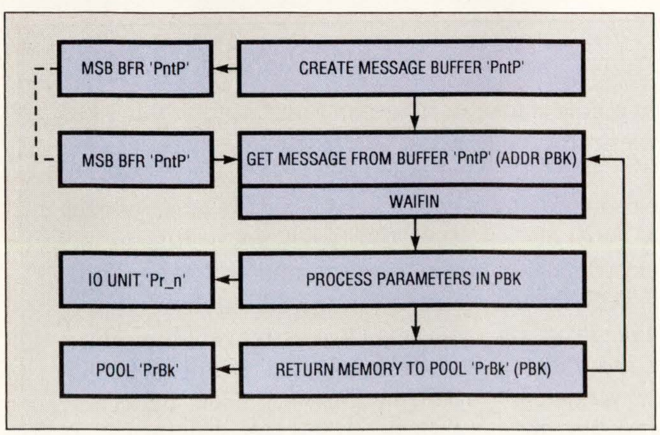

Fig 3—A typical consumer task receives the address of information (a parameter block) from a message buffer, then processes the information and returns the parameter-block area to a memory pool.

The buffer is created within a memory pool known as the Transient Program Area (TPA). For a single-processor system, there is only one TPA. For a multiprocessor system, there is one global TPA and one local TPA per processor. Thus, with a multiprocessor system the designer can specify the TPA by adding a term to the size parameter. The choices are **MSBGBL** (for a global buffer), **MSBLC0** (for a buffer local to processor 0), . . . , **MSBLCF** (for a buffer local to processor 15).

Some further calls are

```
#define MSB1 0x4D534231
#define MSB2 0x4D534232

long int msbid1,msbid2;  /*identifier of message buffers 1,2*/

msbid1 = crmsb (MSB1,MSBGBL+200);

if ((msbid2 = crmsb (MSB2,MSBLC2 + 500)) == QUEFUL) ...
```

A local message buffer must be created, used, and deleted on the processor specified in the second parameter of *crmsb*. The advantage of a local buffer is reduced traffic over the backplane. The advantage of a global buffer is universal access by all tasks.

The task that creates a message buffer automatically receives the identifier. Any C task that knows the key can also determine the identifier via

```
long int id2;

id2 = getmsb (MSB2);
```

Upon return, *id2* either has the identifier of the buffer with key **MSB2** or **BADPRM** if no such buffer exists.

Posting a message to a buffer

Once a task knows the identifier of a buffer, it may post messages to that buffer. If there is already an unfulfilled get-message request queued, the new message fulfills the request and unblocks the receiver. If there is no receiver immediately available, the message is stored (unless the buffer is full). In either case, the task that posted the message continues on.

Since a message buffer will store messages until they are claimed, it is important to control the manner in which storage occurs. Normally, a task posts a message to the *end* of a buffer. The request

```
putmse (msbid,msg);
```

posts a message contained in variable *msg* to the end of the buffer whose identifier is given by *msbid*. If all messages are posted this way, the buffer becomes a pure first-in, first-out storage device.

The task that receives a message "consumes" it. Event flags, on the other hand, are not consumed.

In some parts of an application, last in, first out (LIFO) might be more desirable. For example, the printing of error messages sometimes needs this rule. The request to post a message to the beginning of the buffer is

```
putmsb (msbid,msg);
```

You are free to mix both types of requests, even within a given buffer: Send most messages to the end, but occasionally force a highly important message into the front of the queue. Both posting functions return **NOERR** for success, **BADPRM** if the target is not a message buffer, or **QUEFUL** if storage is needed but the buffer is full.

Note that the message-buffer facility has been designed primarily for speed. Thus, there are no provisions for message priority or coordination at the send end. Applications needing these features can find them in the mailbox services.

Getting a message from a buffer

The OS provides a pair of C functions to get a message from a buffer.

```
long int msbid;        /*identifier of MSB*/
long int *msg;         /*message*/
long int result;       /*result of request*/

result = getmsw (msbid,&msg);

result = getmsn (msbid,&msg);
```

Parameter *msbid* must be the identifier of an MSB, otherwise *result* is **BADPRM**. The address of the variable to receive the message is given by the second parameter.

With the first function, the task will be blocked until a message is available. With the second, if no message is already queued, the return value is **MBEOF**. Thus, *getmsw* is get-a-message-with-wait and *getmsn* is get-a-message-with-no-wait. For *getmsw*, tasks waiting for a message are queued first-come, first-served. This seems to be a fair rule since it is hard to conceive of a case in which the receiving tasks are not all equivalent. There is no limit to the number of tasks that may be queued waiting for a message.

Deleting a message buffer

A message buffer may be deleted by invoking

```
result = dlmsb (msbid);
```

If *msbid* is not the identifier of a buffer, the function returns a failure value of **BADPRM**. The value for success is **NOERR**.

Usually, the MSB is not being used when it is deleted. However, if there are any queued messages or pending receive requests, then the buffer is marked "deletion pending," but it is not removed until activity ceases. New requests will still be honored while the buffer is awaiting deletion.

Achieving mutual exclusion

Commonly, tasks that share alterable data must be sure that access is limited to one task at a time. As you will see in Part 9 of this series, semaphores are the traditional mechanism to achieve the required exclusive access. Nevertheless, a message buffer can be a viable alternative. A buffer is created and then "primed" by sending it one dummy message. Thereafter, whenever a task needs access to the variables, it

Companion disk offer

All of the C examples in this series, plus applications of your own, can be run on a PC with a set of demonstration disks available from Industrial Programming Inc. The disks contain a full version of MTOS-UX for an IBM PC/AT or compatible. An application program is edited, compiled, linked, and loaded under MS-DOS. The MTOS-UX then takes over the hardware to execute the program in real time. At any time, you can enter a ctl/dlt command from the console to return control to MS-DOS.

The demonstrator requires an AT with a least 512k bytes of RAM and a hard disk with 2M bytes available for MTOS libraries and scratch storage. Program preparation requires the Microsoft C compiler/linker, version 5.0 or later. Microsoft tools are not included with the MTOS-UX demonstrator.

The demonstration version has all of the features and facilities of standard MTOS-UX. However, there is a limit of six of each type (six tasks, six mailboxes, six semaphores, and so forth). The disk set costs $25; unlimited versions are also available. For more details, call IPI at (800) 365-6867 or (516) 938-6600, or write to 100 Jericho Quadrangle, Jericho, NY 11753.

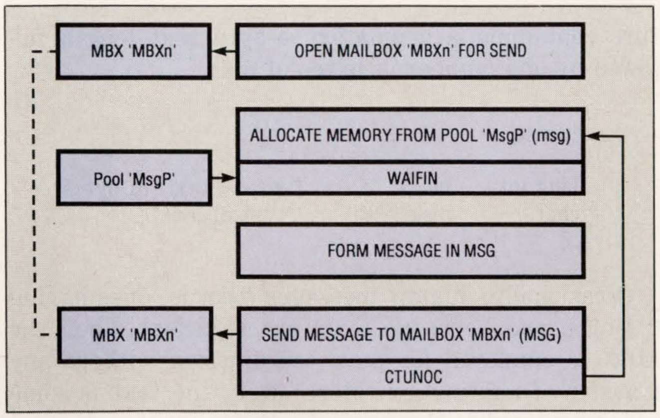

Fig 4—For mailbox communication, a typical producer task opens a mailbox in the "send" mode, then creates a message and sends the address of that message to the mailbox.

would request to receive that message, with wait. Since there is only one message, only one task at a time could proceed; all others queue up at the buffer. Sending the message back to the buffer enables the next task to proceed.

The idea is easily generalized for cases that can permit access by more than one task at a time. Suppose there are four independent and equivalent channels on a certain piece of equipment. Several tasks wish to use a channel, but do not care which one is provided. A buffer is created to handle the assignment of channels. The creating task initially fills the MSB with four messages, each containing a channel number (say, 0 to 3). Now a task waits for a message granting it permission to use one of the channels and eventually returns the message to release the channel to the next user.

Mailboxes vs message buffers

While message buffers are versatile enough to solve many problems that arise in real-time applications, there are often cases in which a stronger facility is required. MTOS-UX mailboxes provide full coordination at both the send and receive ends, arbitrary message length, unlimited queuing, and 256 levels of message priority.

As with a message buffer, a mailbox (MBX) is a place to which a message may be sent and from which a message may be received. The number of mailboxes and the kinds of messages transferred are completely up to the designer.

A mailbox message, however, can be a record containing any number of characters. The content of the record is not significant; the bytes are transferred as an unstructured string. Thus, a record may be a block of text to be processed, a set of data to be reduced, or even the address and length of "the real text or data," as stored in a memory pool.

A task receiving a mailbox message may specify an input buffer shorter than the incoming message. This is considered normal. The message is truncated, with the excess text discarded. In any case, receiving a message always "consumes" it, that is, removes it completely from the MBX.

After a task sends a message, it has the option of continuing or waiting until the message is received. Similarly, a task seeking a message at a mailbox that presently has no messages can either continue or wait for the next message to arrive. These wait options enable tasks to coordinate their activities.

MBX messages have a priority. If there is no receiver waiting, more important (higher-priority) messages are stored in a queue ahead of less important ones. For messages of equal priority, it's first in, first out (FIFO).

There is no corresponding priority for receivers. When a task waits for an MBX message, it's strictly first-come, first-served. It is assumed that all receivers are identical so that there is no need for priority ordering of the wait queue.

Although a mailbox is a storage device, it holds only the parameters of unfulfilled send or receive requests. The content of a message is not copied until a receiver is available, and then the transfer is made directly into the receiver's buffer. The sender may choose to dispatch a message and then continue without waiting for a task to receive it. Nevertheless, because there is no internal storage of text, the sender cannot alter the area containing the message until it is transferred to the receiver. **Fig 6** summarizes the differences between a message buffer and a mailbox.

Opening/creating a mailbox

A mailbox must be opened before it can be utilized. The open specifies both the external name (the usual 4-byte key) and the intended manner of access (the

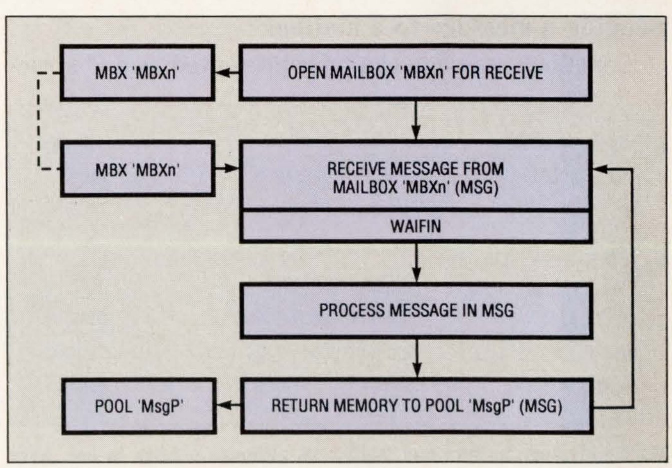

Fig 5—A typical consumer task receives a message from a mailbox and then returns the area where the message was stored to a memory pool.

> Message buffers are quick and simple. Mailboxes are more complicated and provide additional facilities.

"mode"). The mode is either **MBRCV** for receiving or **MBSND** for sending. A task may make both types of open (without any requirement for an intervening close) if it intends to both send and receive messages with the same target MBX:

```
#define MB03 0x4D423033

long int mb3id;          /*identifier of MBX 3*/

mb3id = opnmbx (MB03,MBRCV);

opnmbx (MB03,MBSND);
```

If a mailbox with the given key does not already exist, it is created by this request. The only return values are the MBX identifier for success and **QUEFUL** for failure. The return value does not distinguish a mailbox that already existed from one that was just created. A mailbox is created empty (no senders or receivers waiting).

Each time a mailbox is opened, a tally within the control data for the MBX is incremented, and each time the MBX is closed the tally is decremented. There are separate tallies for send and receive opens. However, the identity of the task making the request is not saved. As a result, it is not necessary for each task that uses a mailbox to have opened it. All that is required is that the current tally of opens minus closes be greater than zero for the corresponding mode.

Sending a message to a mailbox

A mailbox message can be represented as a C structure containing a mandatory 4-byte text length followed by any number of bytes of text.

```
struct msg
  {
    long int    msgs;        /*size of text, in bytes*/
    char        msgt[20];    /*typical text*/
  };
```

Occasionally, dummy messages (that is, ones having 0 length and hence no text) are sufficient when the MBX is employed for pure coordination without any transfer of information. More often, the text is some set of parameters, such as

```
struct msg
  {
    long int    msgs;         /*size of text, in bytes*/
    short int   mtyp;         /*type of msg*/
    long int    mprml[20];    /*parameter 1*/
       ...
  };
```

The simplest way to send a message to a mailbox is with no priority (0L) and wait-forever coordination (**WAIFIN**).

```
struct msg    msgl;      /*message*/
long int      result;    /*result of request*/

sndmbx (mb3id,&msgl,0L,&result,WAIFIN);
```

In this case, *mb3id* must point to a mailbox that has been opened for sending and not subsequently closed.

When a message priority is appropriate, it is entered as the third parameter.

```
sndmbx (mb3id,&msgl,100L,&result,WAIFIN);
```

For proper alignment, the priority must be a long word, even though the range is 0 to 255.

For coordination mode **WAIFIN**, *sndmbx* does not continue until the service is completed. Thus, *result* contains the same information as is returned by the request function itself. Possible values are **NOERR** for successful transfer of message, **BADPRM** for failure due to bad parameter, or **QUEFUL** for failure due to lack of internal resources. For other coordination modes, such as

```
long int     instat;     /*initial status of request*/

instat = sndmbx (mb3id,&msgl,100L,&result,CLEF0+100+MS);
```

sndmbx returns immediately with the initial status of the request (**NOERR**, **BADPRM**, or **QUEFUL**). When the service is completed, *result* contains the final status: **NOERR**, **BADPRM**, **QUEFUL**, or **TIMOUT**

MESSAGE BUFFER		MAILBOX
SIZE OF ADDRESS	LENGTH OF MESSAGE?	ANY
YES	STORES MESSAGE?	NO
YES	MAXIMUM NUMBER?	NO
NO	MESSAGE PRIORITY?	YES
NONE	COORDINATION FOR SEND?	GENERAL
WAIFIN	COORDINATION FOR RECEIVE?	GENERAL
FASTER	SPEED?	SLOWER

Fig 6—Message buffers and mailboxes, although similar in use, have different characteristics. Message buffers are versatile enough for many real-time applications; mailboxes offer additional features.

for failure due to not having a receiver within the specified maximum wait time.

You can take advantage of the deferred coordination modes, such as **CLEFn**, to do work while "waiting" for a message to be received. A typical sequence would be

```
sndmbx (mb3id,&msg1,100L,&result,CLEF0+100+MS);
...        /*do other work*/
waiefg (0L,EFOR+EF0,NOEND)  /*now wait for end of send*/;
if (result!= NOERR)
...        /*process error*/;
```

When sending a message to a mailbox, it is not necessary that any task currently have the box opened for receiving.

Receiving a message from a mailbox

The request to receive a message mirrors the one to send, except that there is no priority among the receivers. A typical receive sequence is

```
struct msg     rec1;                      /*received message*/
rec1.msgs = sizeof(struct msg) - 4;       /*set size*/
rcvmbx (mb3id,&rec1,&result,WAIFIN);
```

As with the send message, the first 4 bytes of a receive message are reserved for the size of the text. Often, the messages are of fixed size, so that the *msgs* component can be set initially and never change. When the size can vary, it is customary to set *msgs* to the largest possible value (and be sure the text portion is correspondingly large enough). The OS limits the actual transfer to the smaller of the size of the message text and the size of the receiving text area. The actual number of bytes transferred is stored in the first 4 bytes of the receiving area, overwriting the original maximum size. If the receiving area is longer than the message, the unused portion of the receiving area is not cleared. If the message is longer than the receiving area, the unused portion is discarded. Neither case is considered an error. A text length of 0 is valid and provides coordination without text transfer.

Coordination for *rcvmbx* is similar to that for *sndmbx*. One difference is that all receivers are assumed to have equal priority so that the wait queue is strictly FIFO. Another is that while no coordination (**CTUNOC**) is often appropriate when sending a message, it makes little sense when receiving one.

For example, receive up to 12 bytes into *rec1*—

```
rec1.msgs = 12;
```

with a maximum wait of 4 sec

```
rcvmbx (mb3id,&rec1,&result,WAIFIN+4+SEC);
```

without limit, but continue and set LEF 15 when done

```
rcvmbx (mb3id,&rec1,&result,CLEF15);
```

If there is a message available when the receive is issued, the function returns immediately with status **NOERR**. Otherwise, the task is expected to wait or not to wait as specified in the coordination qualifier. However, when the MBX is acting as a private conduit ("pipe") between tasks, it is important to be able to distinguish a mailbox that is temporarily empty from one that is permanently in that state. In the first case, it makes sense to wait for a message; in the second it does not. Toward this goal, when a receive request is made to an empty mailbox, the OS checks whether the MBX was once opened for sending and is currently not opened in that mode. In that special case, the receive request returns immediately with "at end of file" (**MBEOF**) status. In all other cases, an unfulfilled receive request is queued. This applies for all four basic coordination modes (**WAIFIN**, **CTUNOC**, **CLEFn**, and **CSIGn**).

Closing and deleting a mailbox

Very often a task that communicates via a mailbox is organized as an endless loop, as **Figs 4** and **5** show. For such tasks the mailbox exists for the entire life of the application. Nevertheless, there are provisions to close and to delete a mailbox, if need be. The functions

```
result = clsmbx (mb3id,MBSND);
result = clsmbx (mb3id,MBRCV);
```

close the given mailbox in the send and receive mode, respectively.

A valid close decrements the opens-remaining tally for the given mode. If the new tally is still 1 or more, the function returns **NOTFRE** to indicate that there are other opens still outstanding. If there are no more opens left for the given mode, the function returns **NOERR**.

The mailbox may be deleted by invoking

```
result = dlmbx (mb3id);
```

If the argument is not the identifier of a mailbox, the function returns a failure value of **BADPRM**. The value for success is **NOERR**.

Using a mailbox as a pipe

A pipe is a connection between two tasks, arranged so that the output of one task becomes the input to

After a task sends a message, it has the option of continuing or waiting until the message is received.

the other. Under Unix a pipe is implemented via the file system; under a real-time OS a pipe can be achieved using a mailbox. The following suggests one method to create a mailbox pipe. Many variations are possible.

A sender task (**S**) issues an *opnmbx* with mode **MBSND**. When **S** wishes to output some text, it issues *alloc* to obtain a pool area large enough to house the text. (Typically the area is larger than needed because of the granularity of a pool allocation.) The text is stored. **S** then posts a message containing the address and length of the allocated area to the pipe MBX. The priority is 0 so that messages proceed first in, first out. No-coordination is selected; **S** continues. When there is no more output, **S** closes the MBX.

A receiver task (**R**) issues a corresponding *opnmbx* with identical key and mode **MBRCV**. **R** seeks a message from the pipe MBX with unlimited wait. When **R** continues, it has either the address of the pool area or the **MBEOF** status. In the former case, it processes the text, deallocates the pool area, and then repeats the loop. In the latter case, it also closes the MBX to delete it.

Dangling references

The OS services to send and receive a message from a mailbox can be performed synchronously by choosing coordination mode **WAIFIN**. In this context, synchronously means that the requesting task does not continue running until the message is transferred. However, the OS also permits asynchronous communication via the deferred coordination modes **CSIGn** and **CLEFn** and the uncoordinated mode **CTUNOC**. With these last three asynchronous modes, the task continues to execute while the message transfer takes place.

In principle, a task that participates in asynchronous communication is free to execute any of its code, and thus may be at any point within its code space when the message is finally transferred. Therein lurks a danger: Unless this freedom is carefully controlled, there is significant potential for trouble.

A simple example can demonstrate the difficulty. A task enters a subprogram. Upon entry, it allocates some space for local variables, including a message buffer. The task builds a message in the buffer, sends the message to a mailbox with deferred coordination, performs other work, and then exits the subprogram. The exit code automatically reclaims the storage allocated for the local variables.

Usually there is no problem—by the time the other work is finished so is the transfer of the message. However, every so often the transfer is delayed so that the other work finishes first. In this case, while the message is waiting to be received, its memory is reallocated for other purposes. The OS cannot know that it is preserving an address that is no longer valid; when the receiver seeks a message, it gets whatever happens to be stored in the buffer at that moment. In general, preserving a pointer to a variable that no longer exists is known as a dangling reference. Among the candidates for a dangling reference are the receive buffer of *rcvmbx*, the runtime argument of *start*, the return argument of *exit* or *dltsk*, and the results buffer of any asynchronous service.

Several solutions are possible. The simplest is to always specify **WAIFIN** for a service that involves a local variable. Alternately, choose **CLEFn** but wait for the event flag to be set before exiting the scope of the local variable. (The scope of a variable is that portion of the code in which the variable exists.) Yet another alternative is to avoid local variables altogether by always utilizing static areas. That alternative, however, is often not convenient for dynamically composed messages. In these cases, you can avoid the troublesome automatic deallocation that occurs with local variables by having the sending task explicitly allocate the message area from a fixed block or common memory pool. A preamble or header within the message supplies the allocated address, plus the pool identification and allocation size, unless these are known by convention (**Fig 7**). The receiving task then does the deallocation.

In summary, message exchanges are a convenient way to connect tasks that feed information to each other. As with an event-flag group, a message ex-

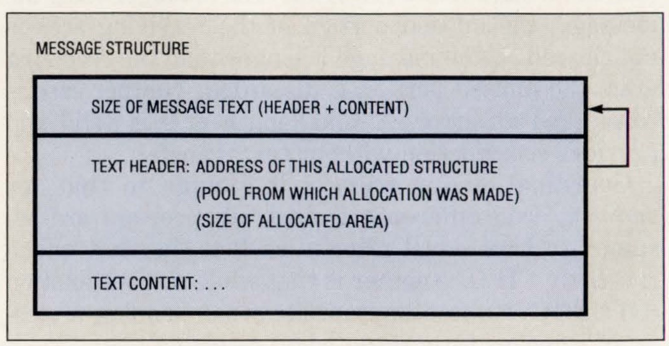

Fig 7—Avoid "dangling references" by having the sending task explicitly allocate a message area from a common memory pool. A message header or preamble supplies the address, plus the pool identification and allocation size.

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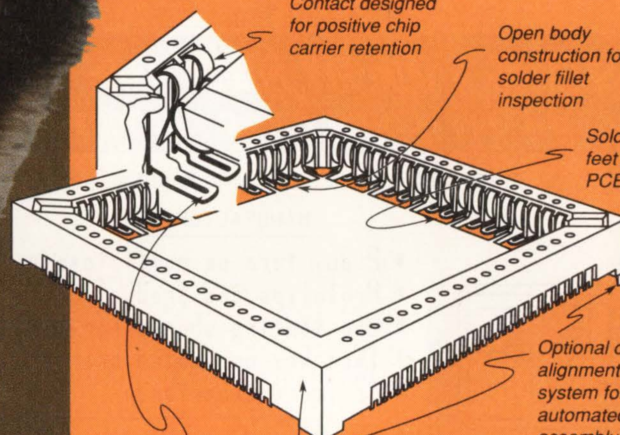

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SAMTEC, INC. • P.O. Box 1147 • New Albany, IN 47151-1147 USA • Phone 812-944-6733 • Fax 812-948-5047 • TWX 810-540-4095 • Telex 333-918 change is a freestanding object, separate from the tasks which use it. This permits any number of "producer" tasks to send messages to an exchange and any number of "consumer" tasks to receive them. Furthermore, the transfer of a message can be a point of coordination, with both the sender and the receiver waiting for the transfer.

Nevertheless, coordination based on message transfer is inherently different from coordination based on event flags. A task that receives a message removes it from the exchange. Thus, if two or more tasks are waiting for a message, only one gets it and the others continue to wait. (Recall that all waiting tasks continue when an event flag is set.)

Over the years, two different types of message exchange have evolved to permit the designer to opt for speed when complete generality is not needed. The first type, message buffers, are the faster of the two, but accept only messages that are the size of a pointer (4 or 6 bytes). These messages can have only two levels of urgency (ie, messages can be posted to either the front or the back of the queue.) Furthermore, the sender can only post a message without coordination, while a receiver can only coordinate using the equivalent of **WAIFIN** or **IMONLY**.

The second type of exchange is the mailbox. It is fully general. Messages can be of any length and can be assigned any of 256 levels of priority. All coordination modes and options are available to both the sender and receiver.

Part 9 of this series will discuss task coordination with semaphores and controlled shared variables. EDN

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In EDN's February 4, 1991, Special Report, Regional Editor Maury Wright will bring you up to date on the latest developments in the 3½-in.-drive area. The real-time programming series continues with part 9, which will examine semaphores and controlled shared variables.

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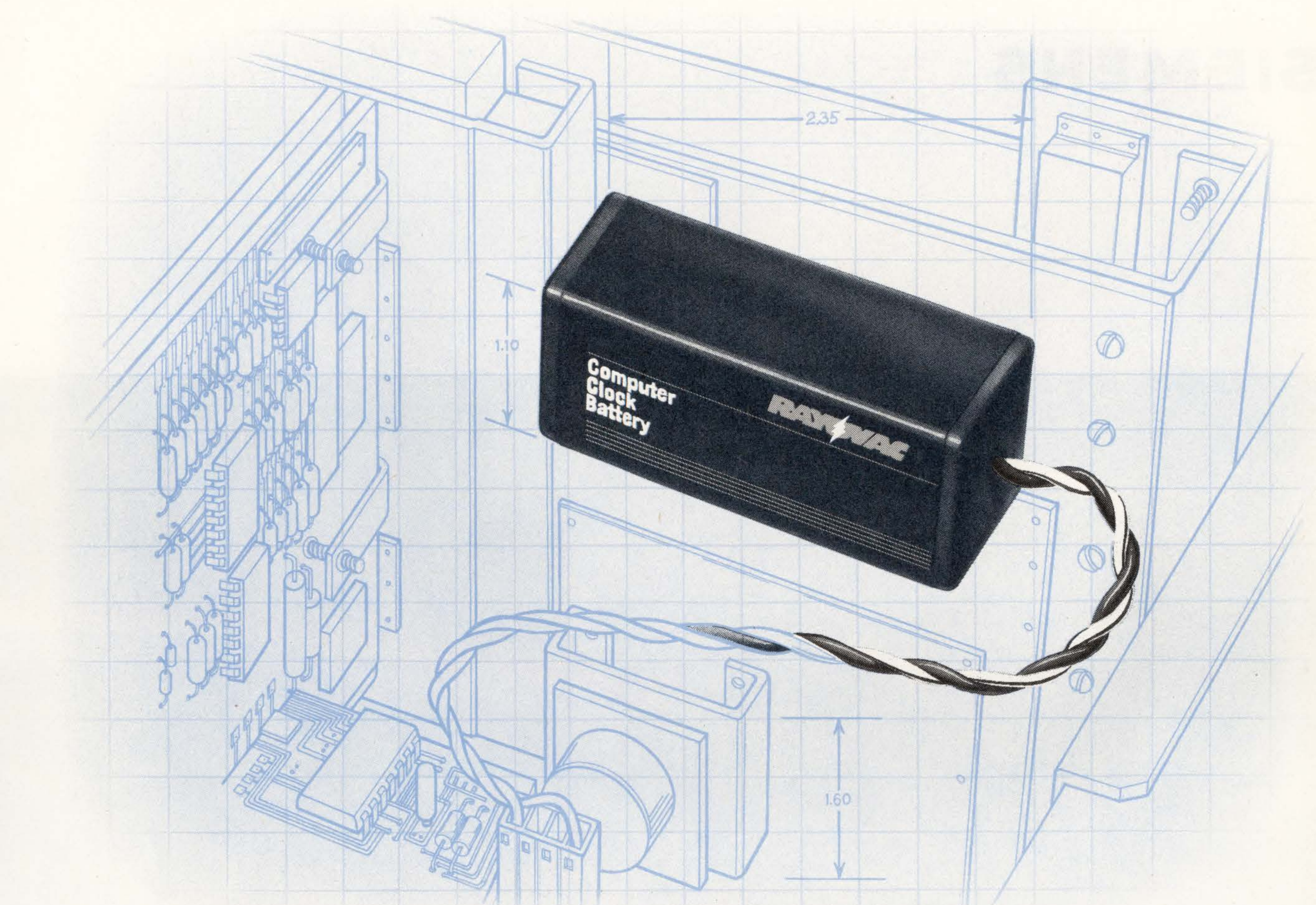

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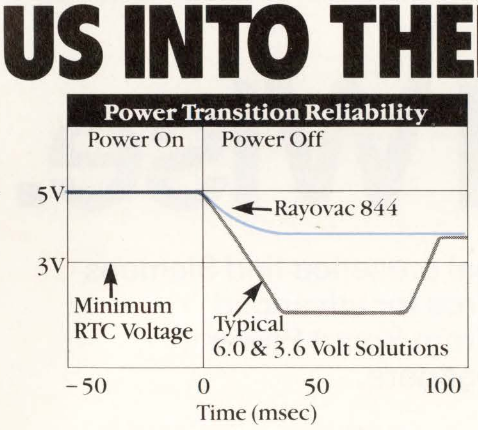

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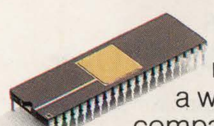

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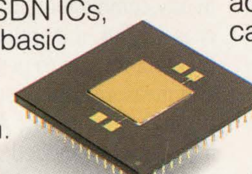

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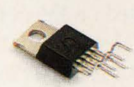

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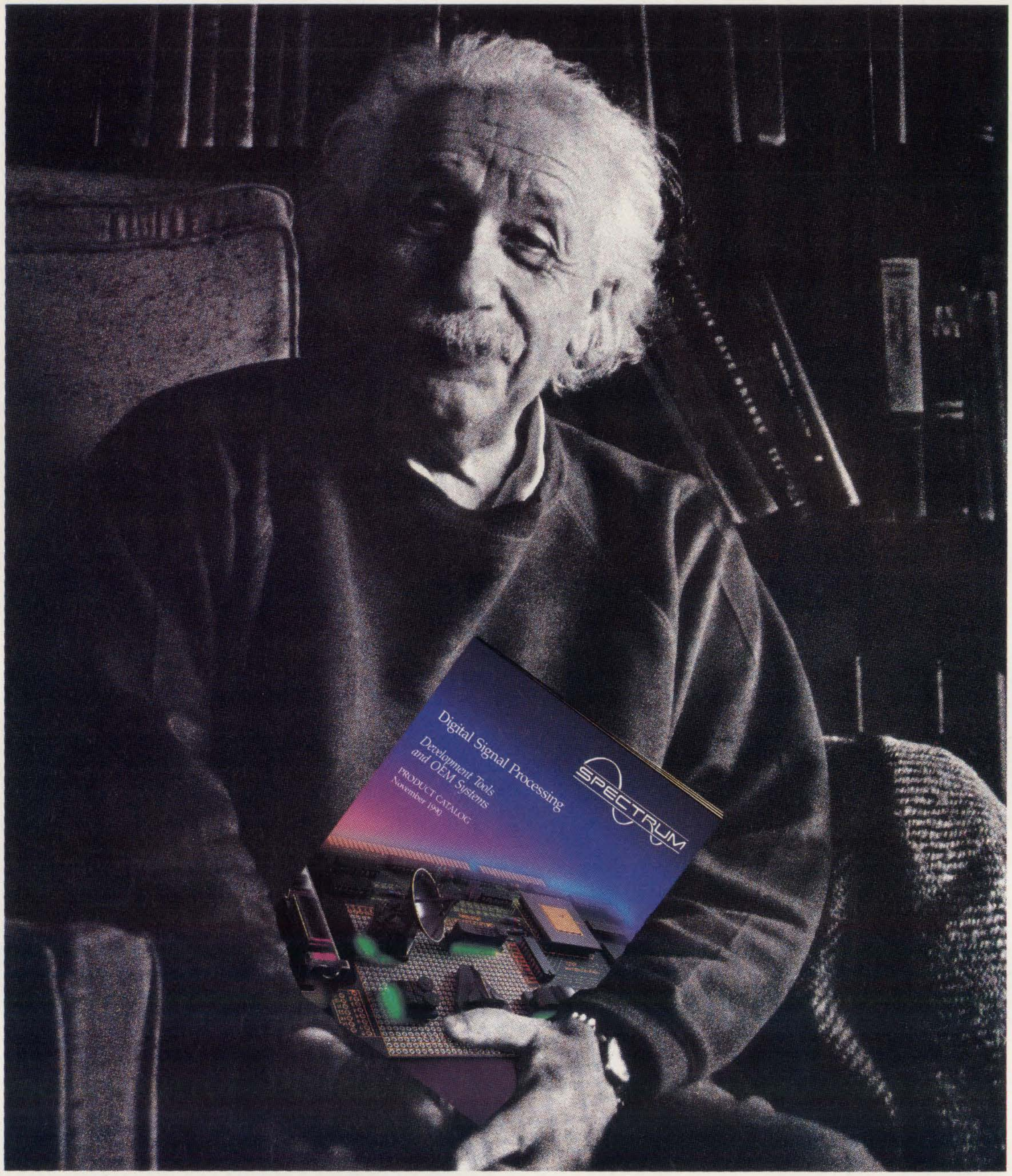

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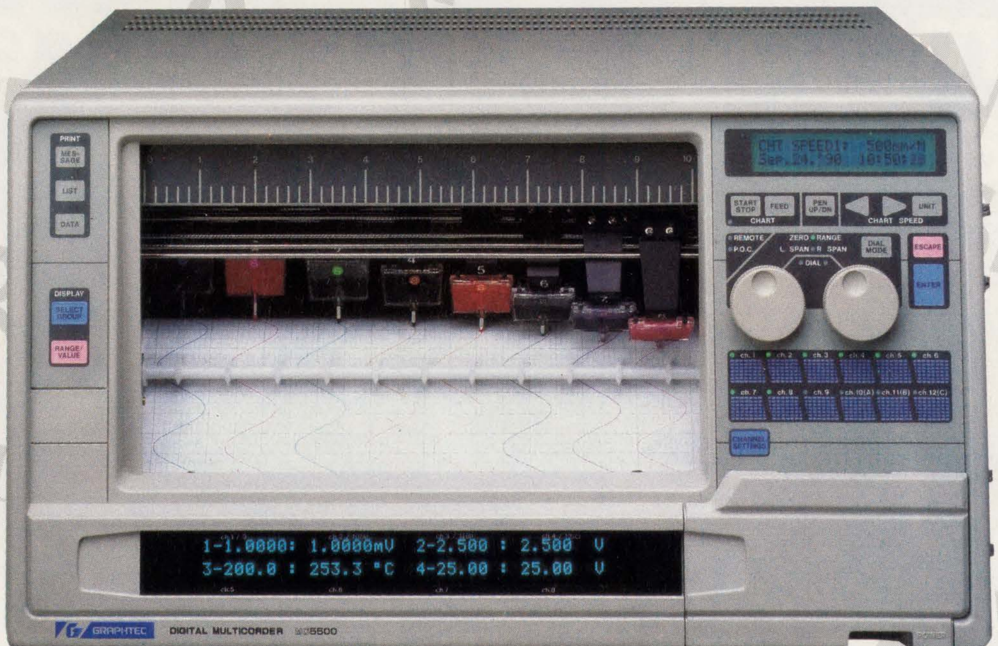

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CIRCLE NO. 28

DSP chips can produce random numbers using proven algorithm

You can use random-number sequences to test electronic components faster than more traditional methods allow. And a well-programmed DSP μP is one of the fastest ways to produce random-number sequences.

Paul Mennen, *Tektronix Inc*

If you incorporate mathematically proven methods into your programming, your DSP μP can generate reliable random-number sequences. Many of the properties of the "linear congruential sequence" method of random-number generation have been proven, making it an obvious choice. Without too much work you can translate this method from mathematical theory to general DSP-μP pseudocode to executable code for your DSP μP.

A random-number generator must satisfy two conflicting requirements. First, the generator must be able to repeat the same random sequence many times. This ability allows you to repeat a test exactly. It also helps, when averaging the results of several measurements in the time domain, to reduce the effects of external disturbances. The repeatability requirement is the easiest to meet because any computational algorithm will produce the same sequence every time you execute it if it begins with the same initial conditions.

Second, and almost opposite, the sequence must be truly random. A truly random sequence minimizes the effect of external disturbances by averaging many frequency-domain measurements. This requirement is impossible to satisfy with a deterministic computational device such as a digital signal-processing (DSP) chip. The best you can do is to make the sequence long enough so that it seldom repeats during a measurement. Consequently, the term for such sequences is "pseudorandom."

Usually you would want the numbers in the sequence uniformly distributed over the available range. In this case, however, a uniform distribution at the DAC input would produce a Gaussian distribution at the output because of the averaging effects of the DAC's smoothing filter. For frequency-response applications you should seek spectral flatness so that all frequencies can excite the DUT evenly.

Of the hundreds of methods in use for generating random sequences, perhaps the best known method is the "linear congruential sequence" (LCS) method. One advantage of the LCS is that mathematicians have been able to prove many of its properties. Such proofs reduce the amount of testing required and ensure well-characterized outputs.

The proven method explained

The defining equation for the LCS is

$$R' = (aR + c) \bmod m$$

where R is the random number, a and c are constants, and mod m signifies taking the remainder after divid-

Random noise speeds testing

Before the days of Fourier analyzers, engineers measured frequency response by exciting the system under test with a series of sine waves and measuring the system's output level at each excitation frequency. Random-noise excitation allows you to make the same measurement much faster. The idea is to excite the system with a signal having all frequencies of interest simultaneously instead of just one frequency at a time. You then compare the Fourier transforms of the input and output to generate a frequency-response plot.

Fig A shows a test setup for measuring the frequency response of an electrical network. **Fig B** shows the results from a test between 0 and 200 kHz using a Fourier analyzer. The analyzer computed the two spectra on the upper left and right from the Fourier transforms of Inputs 1 and 2, respectively. The lower trace is the resulting frequency-response curve. This measurement required 1.5 seconds. Repeating the measurement using the swept-sine technique yielded the same result (**Fig C**), but took 3 minutes.

ing by m (modulus). To use this simple algorithm, first you must pick a starting value for R, called "the seed." Then multiply R by a constant, add a different constant to the product, divide the sum by m, and assign the remainder resulting from this division to be the next value of R. Repeat these steps every time you require a new random number.

The numbers produced lie between 0 and $m-1$, and the sequence can not be longer than m (assuming that a, c, m, and the seed are positive). The number you choose for the seed is unimportant, but you must pick appropriate values for a, c, and m—not a trivial task. Make your choices to satisfy the following six criteria (where $n=\sqrt{m}$):

1. c and m are relatively prime.
2. $a-1$ is a multiple of every prime factor of m.
3. $a-1$ is a multiple of 4 if m is a multiple of 4.
4. a and c are both greater than n.
5. $a \div n$ (truncated) is a power of 2.
6. a mod n is less than $n \div 2$.

The first three criteria ensure that the algorithm's output will be a maximal-length sequence; that is, the sequence will hit all of the numbers between 0 and $m-1$, in random order, before repeating. (This result is provable, but that is beyond the scope of this article.) Criterion 4 ensures sufficient spectral flatness and distribution uniformity. Criteria 5 and 6 will simplify the computation without compromising the sequence's quality.

Computations for a specific DSP µP

You may want to use the AT&T WE-DSP16 because it is the only DSP µP fast enough to compute random numbers and interpolation filters in real time. These filters vary our Fourier analyzer's random-noise bandwidth because our analyzer's DAC's output rate and smoothing-filter bandwidth are fixed.

Note that choosing m to be a power of 2 simplifies computation because shifts can accomplish the division. The WE-DSP16 includes a 16-bit multiplier, so $m=2^{16}$ would be a logical choice. Assuming a maximal-length sequence and a 512-kHz output rate (required for a 200-kHz bandwidth), the sequence will repeat every 0.128 seconds ($65536 \div 512000$). Unfortunately, this sequence is too short for practical purposes. The next logical choice then is $m=2^{32}$, resulting in a sequence length of 2.33 hours (65536×0.128 seconds). This time is long enough to satisfy demanding test situations.

For this choice of m you need to do a 32-bit multiply. Like other fixed-point DSP chips, the DSP16 has only a 16-bit multiplier. Therefore the 32-bit multiply requires multiple-precision arithmetic, which complicates the code considerably. To formulate a multiple-precision algorithm, define a_{lo} and a_{hi} to be the lower and higher 16 bits of the constant a. Similarly, denote the two halves of the random number as R_{lo} and R_{hi}. Now the LCS algorithm, using multiple-precision arithmetic, becomes

$$R = c + a_{lo} * R_{lo} + ((a_{lo} * R_{hi} + a_{hi} * R_{lo} + \mathrm{zz}) << 16) \quad \mathbf{(1)}$$

where

$*$ multiplies two 16-bit numbers (32-bit result),
$+$ sums two 32-bit numbers,
$<<$ is a logical left-shift operation, and
$\mathrm{zz} = a_{lo}$ if R_{lo} is greater than 32768, or
$\mathrm{zz} = 0$ otherwise.

To see where this algorithm comes from, first look at the multiple-precision product of the 32-bit constant a and the 32-bit random number R. **Fig 1** shows this operation.

Because the remainder after dividing by 2^{32} *(m)* is simply the low-order half of the 64-bit product, you don't need to compute the high-order half. Thus you need save only the lower half of the second and third partials, and you don't need to compute the fourth partial at all. Because of criterion 5, a simple left shift computes the third partial, leaving only two required multiplications.

By now you should be able to verify **Eq 1**, except

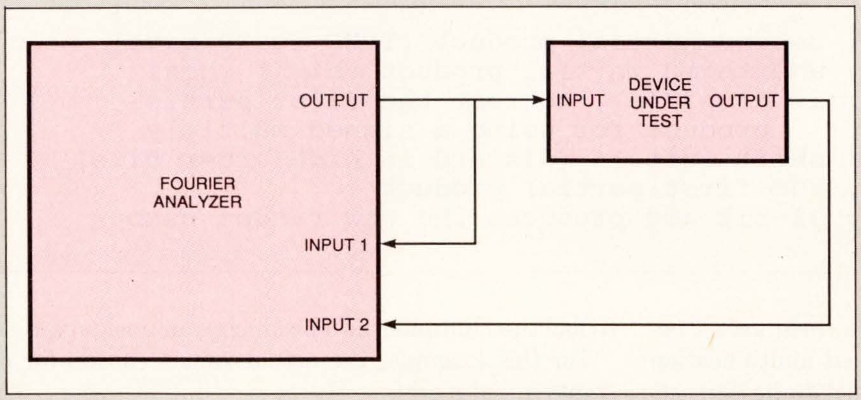

Fig A—A Fourier analyzer derives a frequency-response plot *from the Fourier transforms of the input and output waveforms of the device under test.*

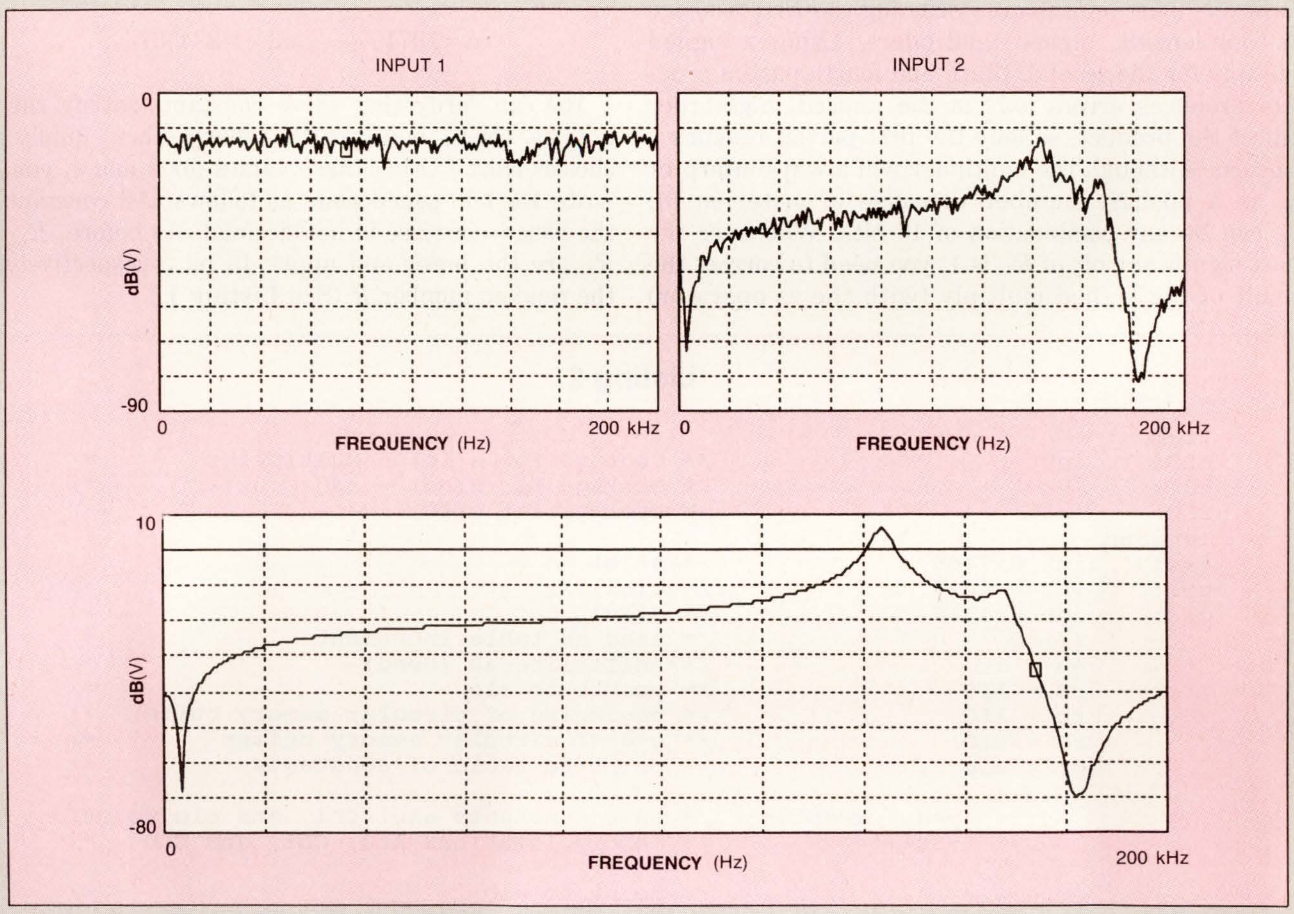

Fig B—A Fourier analyzer derived the lower frequency-response plot *from the upper two input and output waveforms.*

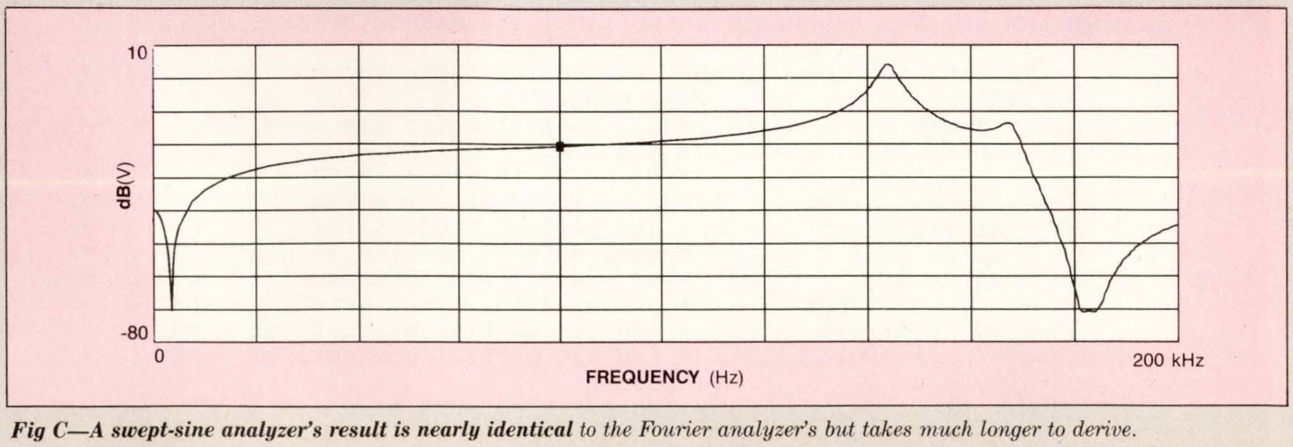

Fig C—A swept-sine analyzer's result is nearly identical *to the Fourier analyzer's but takes much longer to derive.*

Listing 1

```
TEMP=7465*Rhi          ; second partial product (TEMP is 32 bits)
TEMP=TEMP+Rlo<<4       ; add third partial product ahi=10 (hex)
if Rlo>7FFF            ; if Rlo>32767, correct the first partial
   TEMP=TEMP+7465      ;    product for using a signed multiply
TEMP=TEMP<<10          ; shift left 16 (discard 16 high-order bits)
TEMP=TEMP+7465*Rlo     ; add first partial product
R=TEMP+234567          ; 32-bit add produces the new random number
```

for the mysterious "zz" operator. This term arises because partial products require unsigned multiplication for the 64-bit multiple-precision product to be correct. However, most multipliers (including the DSP16's) are 2's-complement, signed multipliers. Using a signed multiply for the second, third, and fourth partial products produces errors only in the unused, high-order half of the product, so only the first partial remains a concern. Although the multiplier will always interpret a_{lo} as a positive number (because of criterion 6), R_{lo} can be any combination of 16 bits. Whenever the most significant bit of R_{lo} is 1, you need to correct the result of the signed multiply (with the zz operator) to fool the multiplier into producing an unsigned result.

For this example, the actual values chosen for constants a and c are:

$$a = 107465_{\text{HEX}} \text{ and } c = 234567_{\text{HEX}}$$

You can verify that these constants satisfy the six criteria. (Note, however, that many other equally fine choices exist.) Using these values for a and c, you can write **Eq 1** in psuedocode as follows. All constants in the psuedocode are in hexidecimal. As before, R_{lo} and R_{hi} are the lower and upper 16 bits, respectively, of the random number R.(See **Listing 1**.)

Listing 2

```
.ram
ALO:     int                        /* storage for a(lo) - Multiplier        */
CHI:     int                        /* storage for c(hi) - Add constant      */
CLO:     int                        /* storage for c(lo)                     */
.endram
alo:     int 0x7465                 /* a(lo)                                 */
chi:     int 0x0023                 /* c(hi)                                 */
clo:     int 0x4567                 /* c(lo)                                 */
         i = 0                      /* used as table increment               */
         a0 = i                     /* initialize a0 (seed)                  */
         r0 = ALO                   /* points to alo                         */
         rb = ALO                   /* beginning of circular memory buffer   */
         re = CLO                   /* end of circular memory buffer         */
         pt = alo                   /* point to table of constants           */
         do 3 {
                 y=a0  x=*pt++      /* save constants alo, chi, and clo to   */
                 *r0++ = x          /* memory locations ALO, CHI, and CLO    */
              }
         pt = alo                   /* point to alo                          */
         y=a0  x=*pt++i             /* x will always contain constant alo    */

/* NOW WE ARE SET UP, AND READY TO ROLL OUT THE RANDOM NUMBERS QUICKLY         */

do n {   /* Execute the loop in the instruction cache (needed for speed)    */
         y = a0                     /* y = Rhi                               */
         a1l = *r0++                /* a1l = alo (zz for Rlo >= 32768)       */
         a0 = a0 << 16              /* a0h = Rlo                             */
         if pl a1=a1<<16            /* clear zz if Rlo < 32768               */
         p=x*y  y=a0  x=*pt++i      /* p = alo * Rhi;  y = Rlo               */
         a1 = a1 + p                /* 2nd partial product + zz              */
         a1 = a1 << 16              /* save only 16 LS bits in a1h           */
         a0 = a0 << 4               /* a0 = ahi * Rlo (3rd partial product)  */
         p=x*y  y=a0  x=*pt++i      /* p = alo*Rlo;  yh = ahi*Rlo = 16*Rlo   */
         a0=a1+y  y =*r0++          /* add 3rd partial product, yh = cH      */
         a0=a0+p  yl=*r0++          /* add 1st partial product, yl = cL      */
         a0=a0+y                    /* add c                                 */
         pdx0 = a1                  /* output high part of R                 */
     }
```

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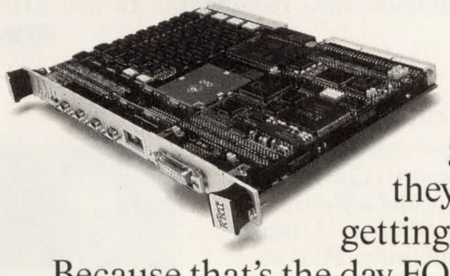

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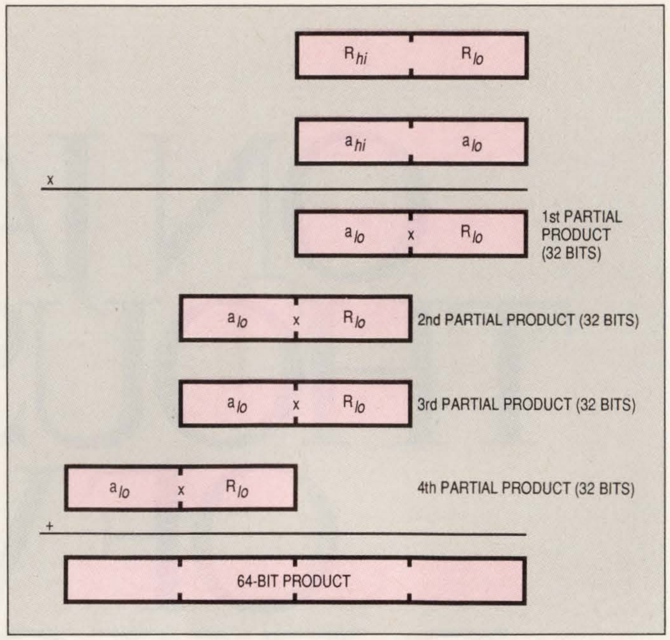
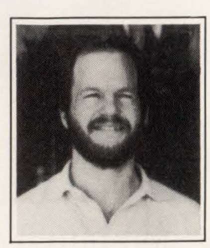


Fig 1—Computing a 64-bit product of two 32-bit numbers *with a 16-bit, 2's-complement multiplier complicates the algorithm.*

Listing 2 contains the AT&T WE-DSP16 code segment, which computes this LCS sequence. The **listing** is also available on the EDN BBS under the /freeware SIG (MS #236, (617) 558-4241,2400,8,N,1). The computations' order maximizes the number of parallel operations. Note that you have computed a 32-bit random number, but you only need 16 bits to send to the DAC. You should choose the upper 16 bits because they are more random than the lower half.

Generating each random number takes only 15 cycles. Therefore, if you were to use the fastest version of the DSP16A (25-nsec clock), and the DSP chip was doing nothing else, you could generate a new random number every 375 nsec. In our case however, the DSP chip has additional work. The LCS sequence must go through a series of digital interpolating filters to lower the bandwidth when required. The filters' output then goes to the output DAC at a fixed rate of 500k samples/sec, providing random-noise bandwidths to 200 kHz. **EDN**

Author's biography



Paul Mennen is a principal engineer for Tektronix, Campbell, CA. He has been doing hardware and software engineering for his firm's Signal Analysis Unit for the past six years. Paul obtained a BSEE from Rensselaer Polytechnic Institute and an MSEE from Stanford University. In his spare time, Paul enjoys aerobatic flying, flight instructing, hang gliding, unicycling, folk dancing, and playing the recorder.

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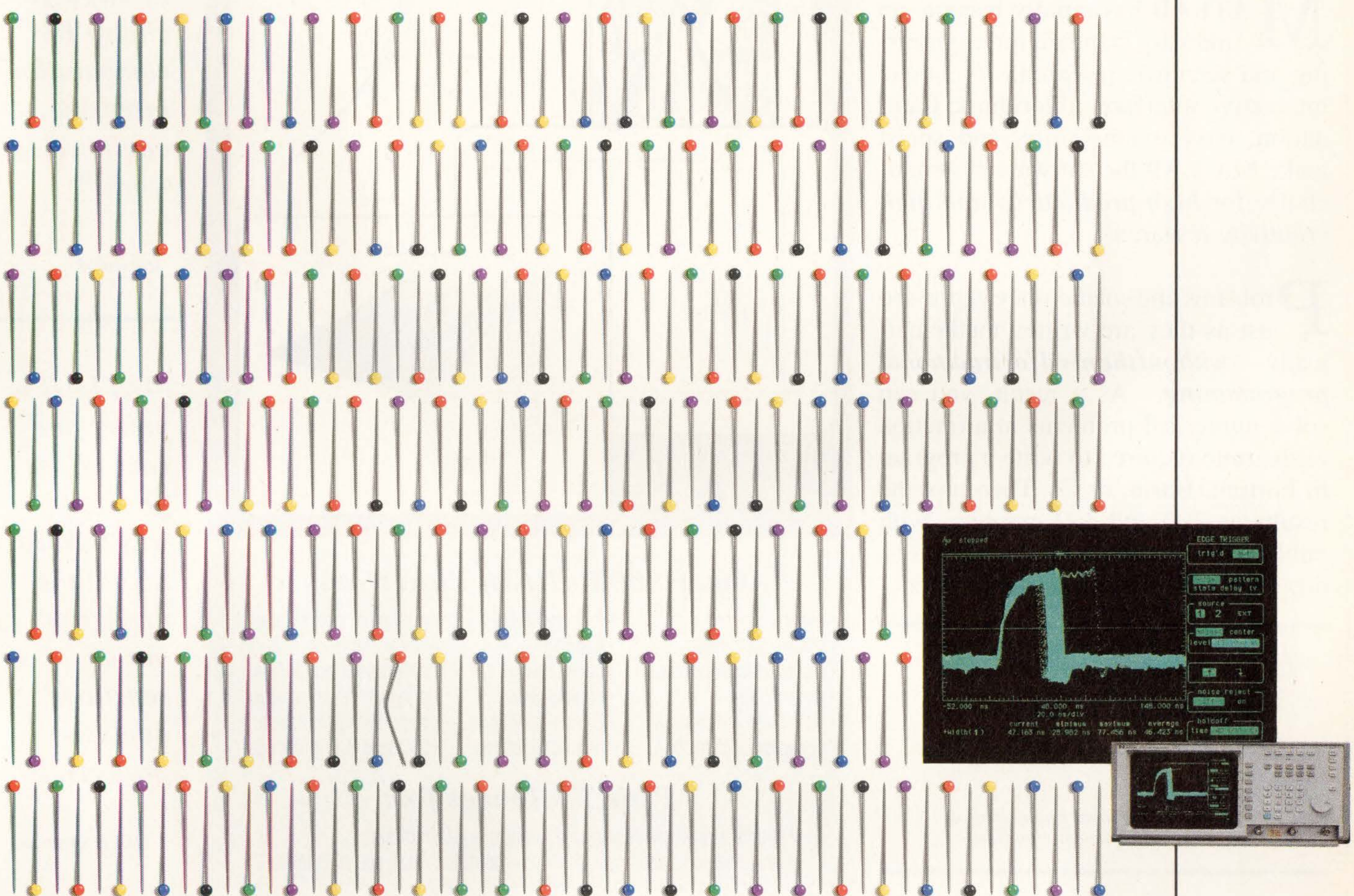

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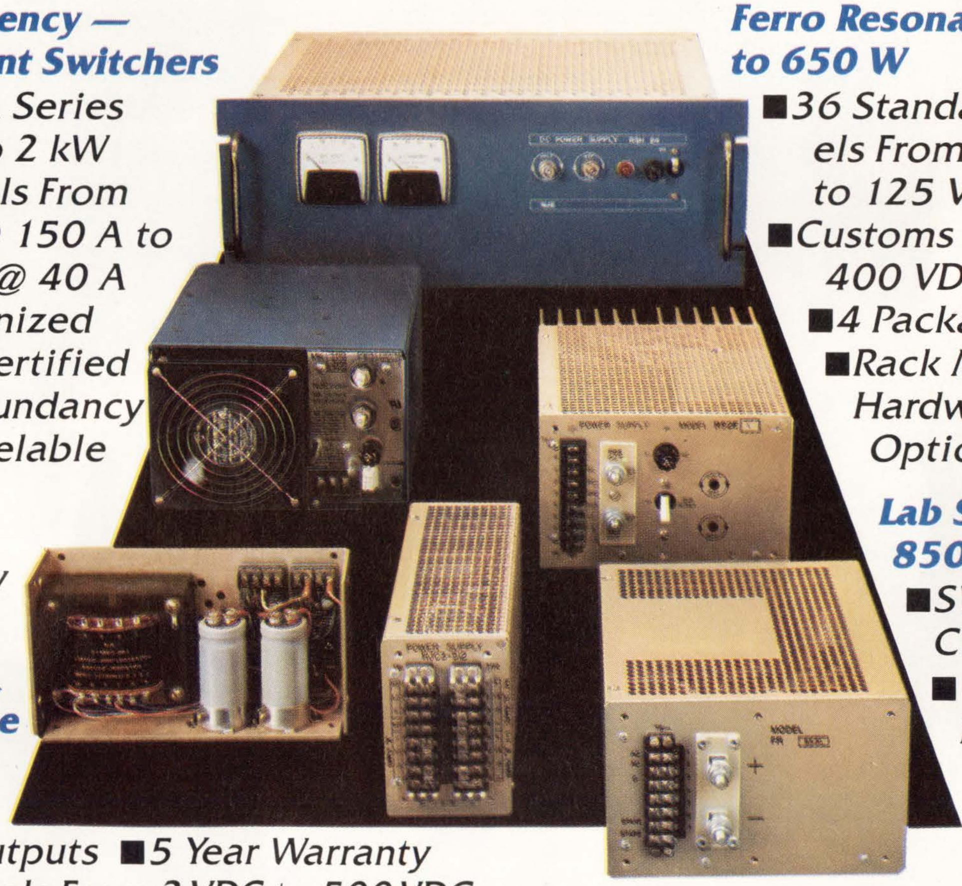

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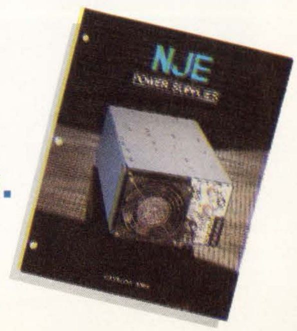

DESIGN IDEAS

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

Digital recorder speeds sampling rate

Lin Jun
Changchun University of Earth Sciences, Changchun, Jilin, Peoples Republic of China

When you use a μP to capture an analog signal digitized by an ADC, the maximum sampling speed is limited not only by the conversion rate of the ADC, but also by the instruction cycle of the μP. If the conversion rate of the ADC is 1 MHz or higher, the system sampling speed can't reach the ADC's potential maximum rate even by using popular DSPs. These systems must have a long sample interval to allow time for the μP to start a conversion, reach the converted result, and adjust the memory address pointer for the next sample: Sample rates above 1 MHz aren't practical. Storing the ADC's results directly in a static RAM (SRAM), followed by a transfer to the IBM PC under the control of external logic, lets your conversion take full advantage of the ADC's speed.

Fig 1 uses the AD7821 ADC with a 1-MHz sampling clock. The 1-MHz clock controls both the start of the conversion and the writing of data into an HM62818, a 128k × 8-bit SRAM. The 74HCT193 synchronous up/down counter drives the address bus of the SRAM.

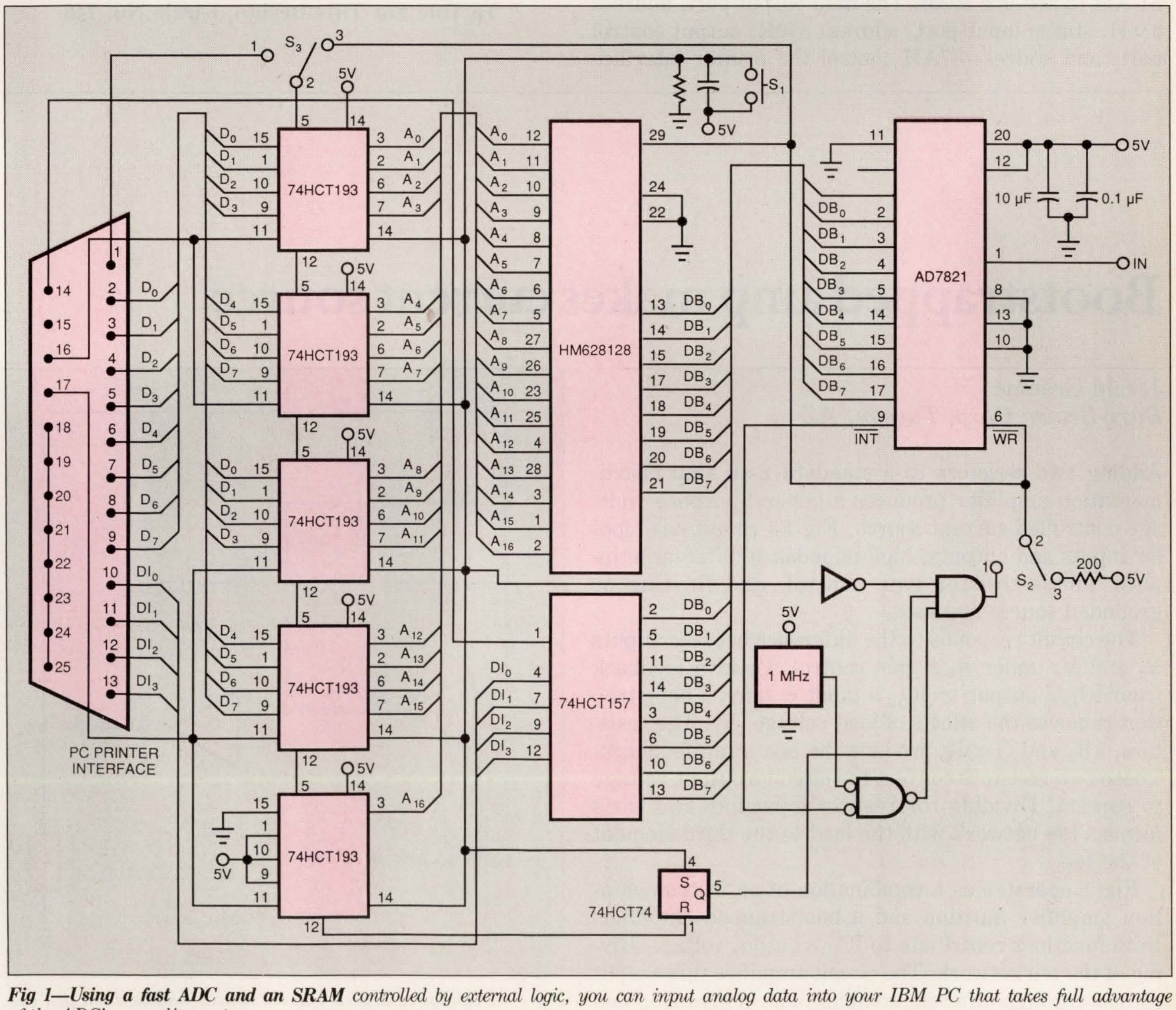

***Fig 1—Using a fast ADC and an SRAM** controlled by external logic, you can input analog data into your IBM PC that takes full advantage of the ADC's sampling rate.*

When S_2 and S_3 are in position 3, the circuit records a high-frequency signal. When the switches are in position 1, the circuit transfers data from the SRAM to the IBM PC through its parallel-printer port.

When you either switch the power on or press S_1 to clear the counter, the circuit samples the input signal at 1 MHz. The address of the SRAM increases automatically after each sample pulse until the carry out of the combined 17-bit counter clears the 74HCT74. **Fig 1**'s automatic address increasing circuit simplifies the block data transfer from the SRAM to the IBM PC. The five 74HCT193 counters generate 20-bit address lines, which can directly drive a 1-M byte memory space. The carry out indicates that the recording process is complete. The conversion result is stored starting with address 00001H.

Switching S_2 and S_3 to the other side forces the SRAM to act as a ROM. The data output port, address 378H, status input port, address 379H, output control port, and address 37AH control the printer interface of a standard IBM PC. You set the address counter's start address through ports 378H and 37AH, and then read the upper 4 bits and the lower 4 bits of the 1-byte through-port 379H by controlling the selection pin of the 74HCT157. This selection pin connects to bit 1 of the output control port. The SRAM address bus automatically increases if you program the control port 37AH properly. Because the circuit uses bits 4 through 7 of port 379H to read 4 bits each time, 1 byte is the result of combining every two 4-bits of data as follows:

- Shift 4 bits of the lower 4 bits to the right
- OR the upper 4 bits to get 1 byte
- XOR 88H to obtain the final result.

The last command is necessary because bit 7 of port 379H is inverted inside the IBM PC.
(EDN BBS /DI_SIG #928) **EDN**

To Vote For This Design, Circle No. 746

Bootstrapped amp makes current source

Jerald Graeme
Burr-Brown Corp, Tucson, AZ

Adding two resistors to a standard 2-op amp instrumentation amplifier produces a general-purpose, voltage-controlled current source. **Fig 1**'s circuit has bipolar inputs and outputs, high-impedance differential inputs, single-resistor gain control, and floating or grounded source and load.

The circuit responds to the difference between inputs V_1 and V_2 under R_G's gain control. Positive feedback from IC_{1B}'s output to IC_{1A}'s input creates a bootstrap that removes the effects of load voltage, V_L. The resistors, xR_2 and $(1\text{-}x)R_2$ produce the bootstrap feedback. These two resistors convert the circuit's output voltage to current. Dividing the resistor input into two parts forms a tee network with the load as the third element of the tee.

Fig 1 operates as a combination of an instrumentation amplifier function and a bootstrapped amplifier. Both functions contribute to IC_{1B}'s output voltage driving of the tee network. The circuit amplifies three input signals through different combinations of inverting and noninverting amplifiers. To input V_1, the circuit ap-

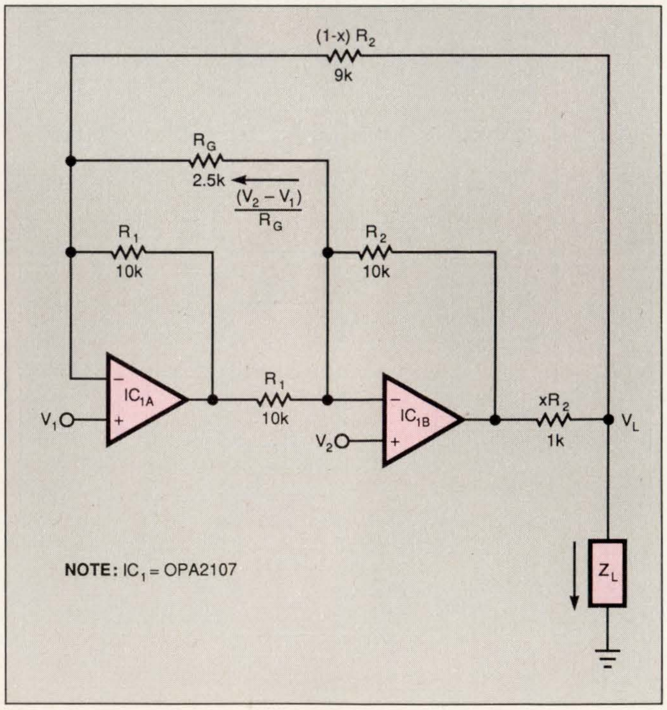

***Fig 1—A voltage-controlled current source results** when you combine an instrumentation-amplifier structure with bootstrap feedback.*

pears as a noninverting amplifier, IC_{1A}, followed by an inverting amplifier, IC_{1B}. Thus, the circuit amplifies and inverts V_1. Input V_2 has a net positive gain. Together, the two inputs produce a signal proportional to $V_2 - V_1$ at the output of IC_{1B}. The circuit boosts this output signal under R_G's control.

The bootstrap feedback adds to V_2's output voltage. The (1-x)R_2 resistor senses V_L to develop an added signal at IC_{1B}'s output. To V_L, the circuit appears as two inverting amplifiers in series for a net positive gain. This positive gain for V_L produces an IC_{2B} output that is in phase with the load voltage. This signal increases the net IC_{2B} output to cancel V_L dependent terms in the output current. The op amp's input offset voltage and input bias currents add to **Fig 1**'s theoretical output current equation.

Two other important characteristics of **Fig 1** are output impedance and output voltage compliance. Resistor values, resistor tolerances, and amplifier characteristics determine these parameters. At low frequencies, the circuit's output resistance would be extremely high except for the resistor mismatches. To ensure accurate bootstrap action, the two R_1 resistors must closely match, and the combined resistance of xR_2 and (1-x)R_2 must equal that of R_2. Only then will the bootstrap feedback accurately cancel the components of load current that are load-voltage dependent. Amplifier characteristics primarily determine voltage compliance. To maximize it, the circuit must place equal demands on the two amplifier outputs. Thus, R_1 and R_2 should be equal. **(EDN BBS /DI_SIG #929)** **EDN**

To Vote For This Design, Circle No. 747

High-side switches control 5V supply

Chuck Thurber and Illy King
Maxim Integrated Products, Sunnyvale, CA

High-side switches are useful for controlling supply voltages. They can lower the operating current in a portable system, for example, by turning off power to selected sections of the system during inactive periods. Three different circuits exhibit low on-resistance and low quiescent current. In each circuit, the 200-pF capacitor connected to pin 7 of IC_1 slows its internal oscillator to 100 Hz, reducing quiescent current in the overall circuit to approximately 10 μA.

Fig 1's switching device, a p-channel MOSFET power transistor, requires a V_{GS} of approximately 10V

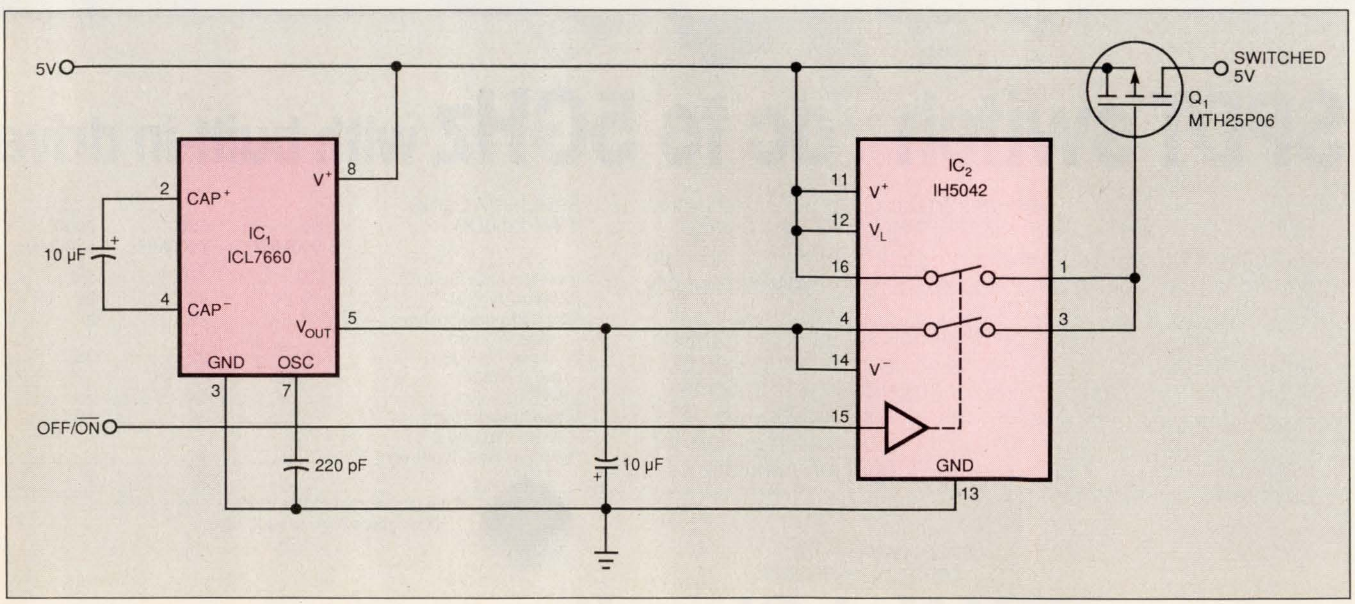

***Fig 1—This circuit provides 5V** under external control, exhibiting 100-mΩ on-resistance when on and 10 μA of quiescent current when off.*

to achieve a 100-mΩ on-resistance. By inverting 5V to −5V, the charge-pump voltage converter, IC_1, enables analog switch IC_2 to deliver the required 10V swing in response to on/off commands. **Fig 2**'s voltage converter generates 9.3V by driving a diode-capacitor voltage doubler. This higher voltage enables the analog switch to apply a 4.3V swing to the logic-level NMOS power transistor, Q_1. Q_1's channel is fully enhanced when V_{GS} equals 5V; the corresponding on-resistance is approximately 30 mΩ.

Fig 3's circuit uses a conventional NMOS switching transistor. When V_{GS} is equal to 10V, Q_1 exhibits a 30-mΩ on-resistance. With additional multiplier stages created by adding diodes and a capacitor to **Fig 2**, IC_1 and the multiplier stages generate 13.5V, enabling the analog switch to provide Q_1 with a V_{GS} of 8.5V. With this V_{GS}, the on resistance will be somewhat higher than 30 mΩ. **(EDN BBS /DI_SIG #927)** EDN

To Vote For This Design, Circle No. 748

Design Ideas continued on pg 160

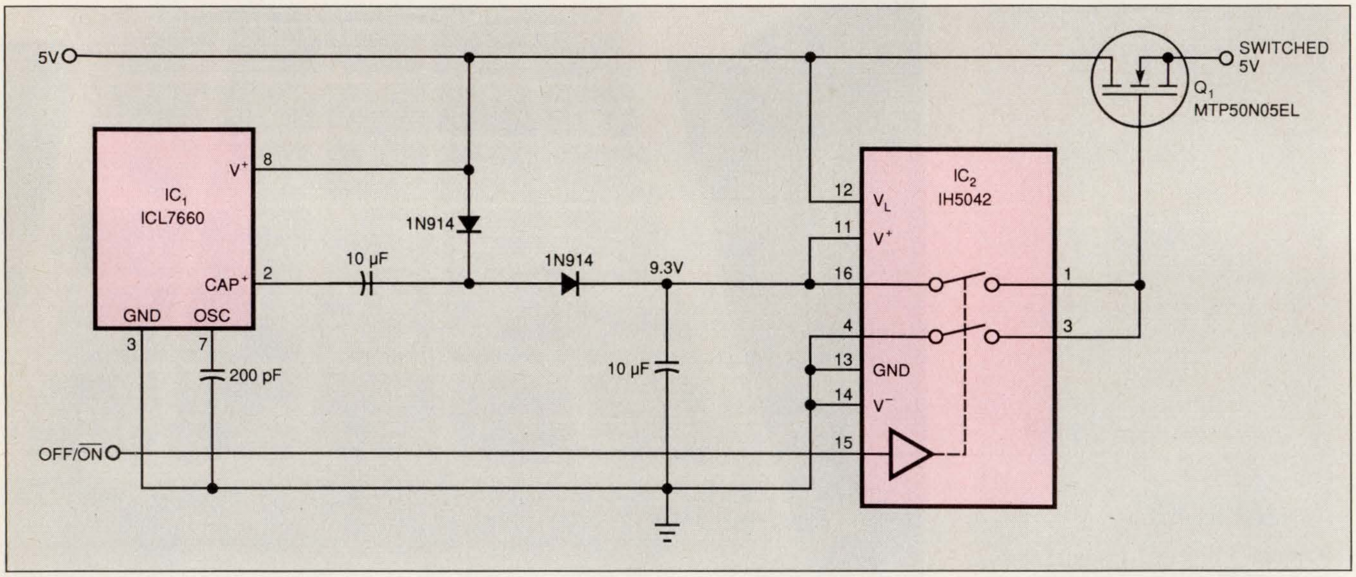

Fig 2—Employing a logic level n-channel MOSFET, *this circuit switches the 5V supply and exhibits a 30-mΩ on-resistance.*

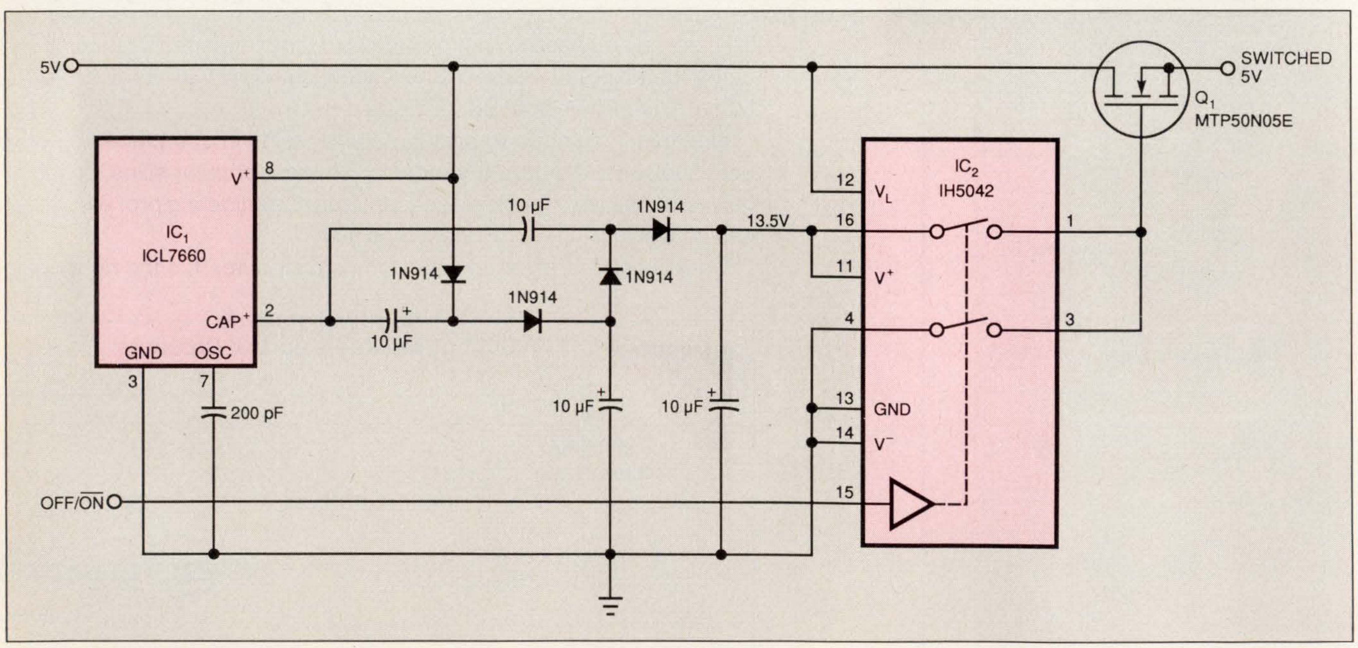

Fig 3—Additional stages in the voltage-multiplier section *of this high-side switch provide a higher gate voltage, allowing use of a conventional NMOS switching transistor.*

Number 43 in a series from Linear Technology Corporation January, 1991

DESIGN NOTES

LT1056 Improved JFET Op Amp Macromodel Slews Asymmetrically

Walt Jung

SPICE macromodels for op amps have been available for some time, for both bipolar[1,2] and JFET[3] input stage device types. Interestingly however, not much attention has been given in the models available to controlled slewing asymmetry. Dependent upon a given amplifier design topology, the large signal characteristics can have various degrees of slew rate (SR) asymmetry. It therefore makes sense to have models which emulate real IC parts in this regard.

A case in point is that of the available P-channel JFET input op amps, many which have a characteristic SR response which is asymmetrical. In fact, popular op amps with topologies like the original 355/356 types are intrinsically faster for negative going output swings than they are for positive. Similar comments apply to such related devices as the OP15, OP16, etc. Since this type of JFET device topology was introduced, the SR specified on the data sheet has typically been the **lower** of two dissimilar rates, i.e., the slower, **positive edge** SR. Thus, given an op amp with a typical SR spec of 14V/µs for positive going edges, the same amp will have a corresponding negative SR of about 28V/µs.

Ironically, this quite common JFET amplifier slewing characteristic has not been well modeled thus far. Most macromodels currently available simply do not address the asymmetric SR issue at all. Others have means of modeling it, but it is seldom found used.

A means of SR control was built into the original Boyle[1] model, and it addresses SR asymmetry for common mode (CM) signals by means of a common emitter (source) capacitor, CE (CS, for JFET amps). However, using this capacitor alone for a general SR symmetry control mechanism leaves something to be desired, as the resulting slopes are not consistent. LTC has implemented a new means of modeling SR asymmetry, shown in Figure 1.

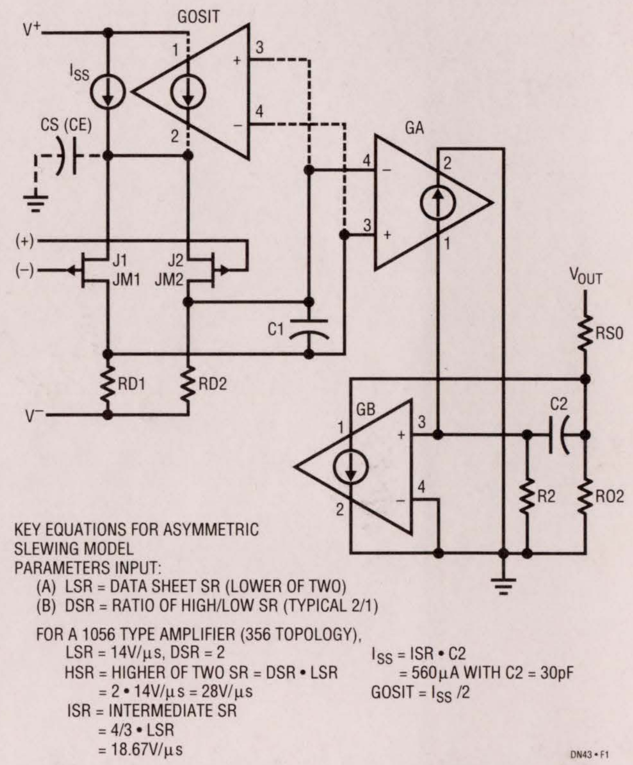

Figure 1. The LTC Asymmetric Slewing JFET Macromodel Has Little Additional Complexity, But Offers Controlled Slewing Response.

The circuit as shown here is a simplified Boyle type model with P-channel JFET input devices, J1 and J2. As this type (or similar input structure) of model is typically used, the SR is simply $I_{SS}/C2$, which is symmetrical when CS is zero. When the common source capacitor CS is added, the SR for CM signals can be adapted (corresponds to CE in the Boyle paper). Unfortunately, this strategy works best for CM amplifier inputs, and not as well for inverting inputs.

The LTC method of modeling asymmetrical SR employs an added VCCS (shown dotted), which dynamically modifies the total tail current available to J1/J2. This controlled source, "GOSIT," is driven by the differential output of J1/J2 and produces a current which adds to or subtracts from the fixed current, I_{SS}. The resulting current available to charge/discharge compensation cap C2 is thus higher for one slewing slope than it is for the opposite. This is true regardless of whether the amplifier is operating in an inverting or non-inverting input mode. As an option, CS can still be used for further control of slewing for CM inputs (shown dotted).

In generating a new macromodel with asymmetrical SR, the **lower** of the two slew rates is input from the data sheet. Also input is the **ratio** of the high-to-low SR. Algorithms in the program used by LTC then calculate an appropriate static value for I_{SS} and the gain of VCCS GOSIT, so that the proper slewing characteristic will be produced by the model.

A representative example op amp with these characteristics is the LT1056, a high performance op amp topologically much like the LF156-LF356 and OP-16 types (also produced by LTC, with corresponding macromodels available). Some sample lines of code taken directly from the LT1056 model released in version 2.0 of the LTC library are shown below. These are shown for both the asymmetric form as released, and for an (edited) symmetric case.

Actually, only one SPICE model element is added to produce the asymmetric SR as opposed to symmetric, and that is the VCCS GOSIT. The LT1056 example below produces SR of +14V/μs and −28V/μs.

```
**
C1   80  90  1.5000E-11
ISS  7   12  5.6000E-04
GOSIT  7 12 90  80  2.8000E-04
* intermediate
```

When the controlled source GOSIT is omitted, the model reverts to simple symmetric slewing, where the SR will be $\pm(I_{SS})$/C2. This is shown below, with I_{SS} adjusted for a (symmetric) SR of 14V/μs. Those lines of code edited are shown in **bold**.

```
**
C1  80  90  1.5000E-11
* for a (symmetric) SR of 14V/μs,
* iss = (1.4e7)*(3e-11) = 420μA
ISS  7  12  4.2000E-04
* comment out gosit with first column "*"
* GOSIT  7  12  90  80  2.8000E-04
* intermediate
```

The non-inverting mode waveforms of a typical SPICE run using the LT1056 macromodel and parallel lab results with an actual LT1056 device are shown in Figures 2A and 2B, respectively. As noted, there is quite reasonable correspondence between the two. A complete LT1056 model is contained on the LTC SPICE diskette.

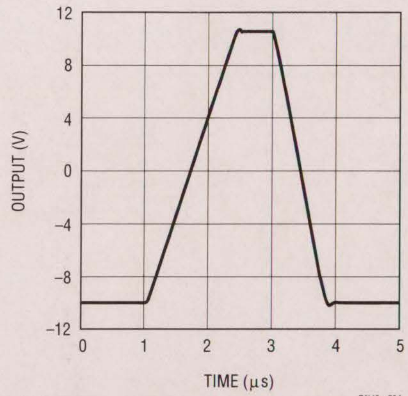

Figure 2A. LT1056 SR (+) Mode, Macromodel

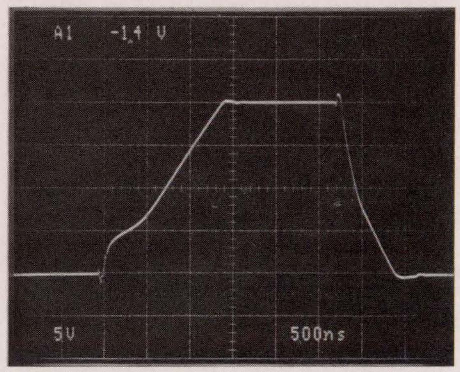

Figure 2B. LT1056 SR (+) Mode, Lab Photo

References

Available from LTC literature service, at (800) 637-5545 are copies of the latest LTC SPICE macromodel library on either a 5.25" or a 3.5" high density floppy diskette.

1. Boyle, G.R., Cohn, B.M., Pederson, D.O., Solomon, J.E., "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.

2. Solomon, J.E., "The Monolithic Op Amp: A Tutorial Study," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.

3. Krajewska, G., Holmes, F.E., "Macromodeling of FET/Bipolar Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-14, # 6, December 1979.

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CIRCLE NO. 101

NEC

Audio compressor splits the band

Richard Majestic
Voice of America, Washington, DC

The 2-band audio compressor amplifier in **Fig 1** features independently adjustable audio-signal compression ratios. The compression threshold is also adjustable. The design provides consistent and precise compression, with no threshold-level drift or compression-slope drift over time and temperature.

The input buffer, IC_1, limits step-function slewing voltages from passing to the following stage, and isolates the input source from the highpass and lowpass filters. Both filters are single pole and minimum phase, eliminating combing effects in the stop bands; they help compensate for compressor artifacts that occur when the circuit sums the two bands together in the output section. The output of the filters drive the input of an SSM-2120 dual-voltage-controlled amplifier/

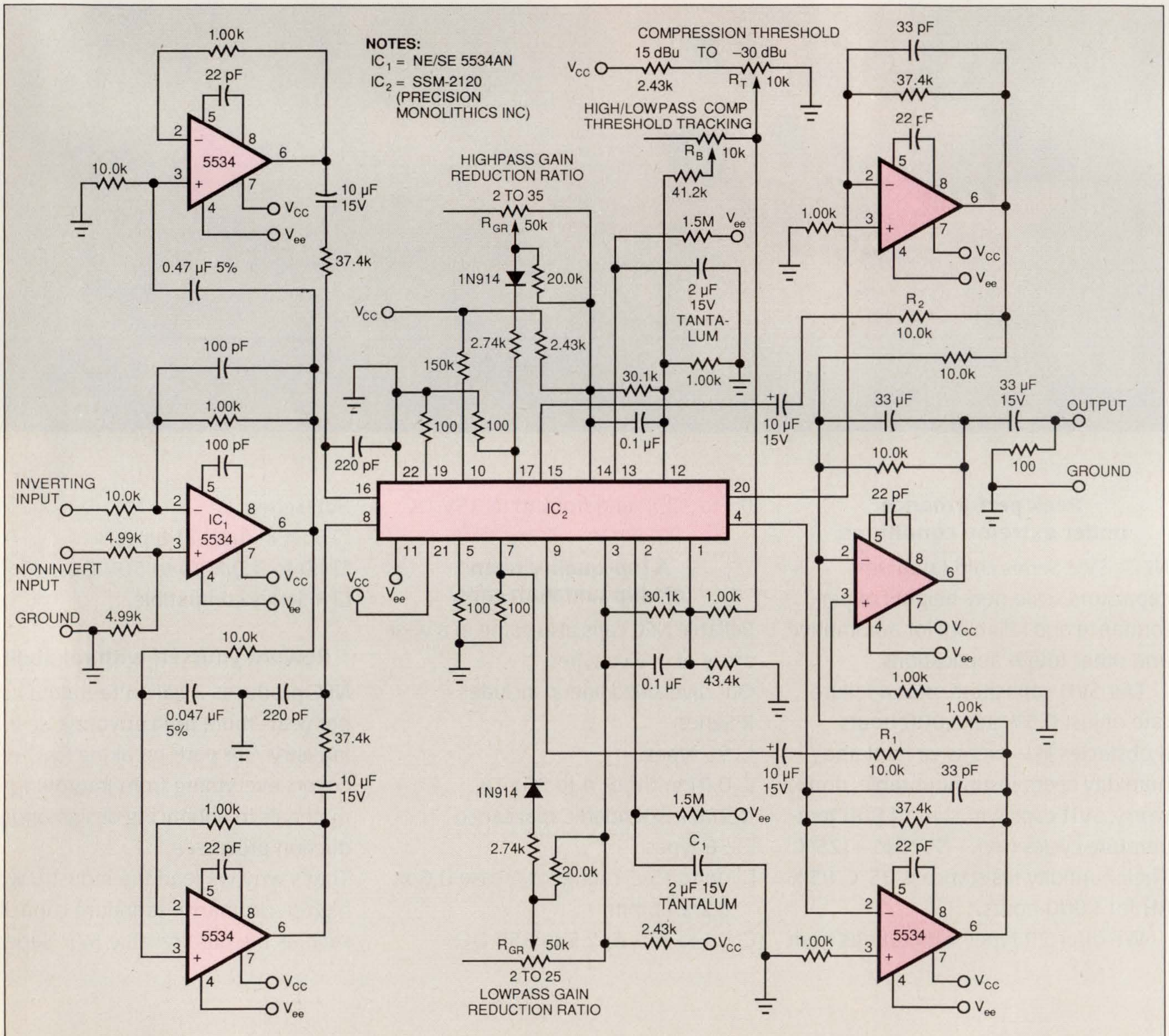


*Fig 1—**Two separate compression controls** allow you to adjust the gain of this audio-compressor circuit's highpass and lowpass sections over a range of 2 to 25.*

rectifier IC. This IC includes two full-wave rectifiers, level detectors, and voltage-controlled amplifiers. The voltage-controlled element and level detector have a dynamic range greater than 100 dB. The amplifier has a flat frequency range of 20 Hz to 20 kHz with typically less than 0.02% THD + noise, and 0.05% intermodulation distortion.

Two continuously variable gain-reduction controls, R_{GR}, within IC_2's control circuit provide independent adjustment of compression gain slopes. The gain-reduction rates are adjustable from 2 to 25 for both highpass and lowpass audio bands. The range of adjustment can produce anywhere from mild compression to severe limiter/clipper action. The control R_B helps balance the threshold amplitude between the two bands for tracking compressor dynamics.

The 10k input current-limiting resistors, R_1 and R_2, and the 2-μF integrator capacitors, C_1 and C_2, control the compressor attack time, which is approximately 20 msec. The 1.5M discharge resistor in the integrator circuit regulates the compression release rate. The recovery time constant is nearly linear because the discharge resistor current is relatively constant.
(EDN BBS /DI_SIG #926) EDN

To Vote For This Design, Circle No. 749

Calculator and IC simplify linearization

Robert S Villanucci
Wentworth Institute of Technology, Boston, MA

Using the HP-42S's curve-fitting software and a multifunction IC for analog computation simplifies thermocouple-linearization-circuitry design. **Fig 1** first cancels the cold-junction voltage, V_R, generated by the connection of the chromel-constantan thermocouple to a copper pc board by adding an opposing voltage, V_C. IC_1, a thermocouple cold-junction compensator, tracks ambient temperature and outputs at a temperature-dependent correction voltage, V_C, that has the same sensitivity as the cold-junction thermocouple. IC_2 amplifies the thermocouple's low-level signal by 100. R_2

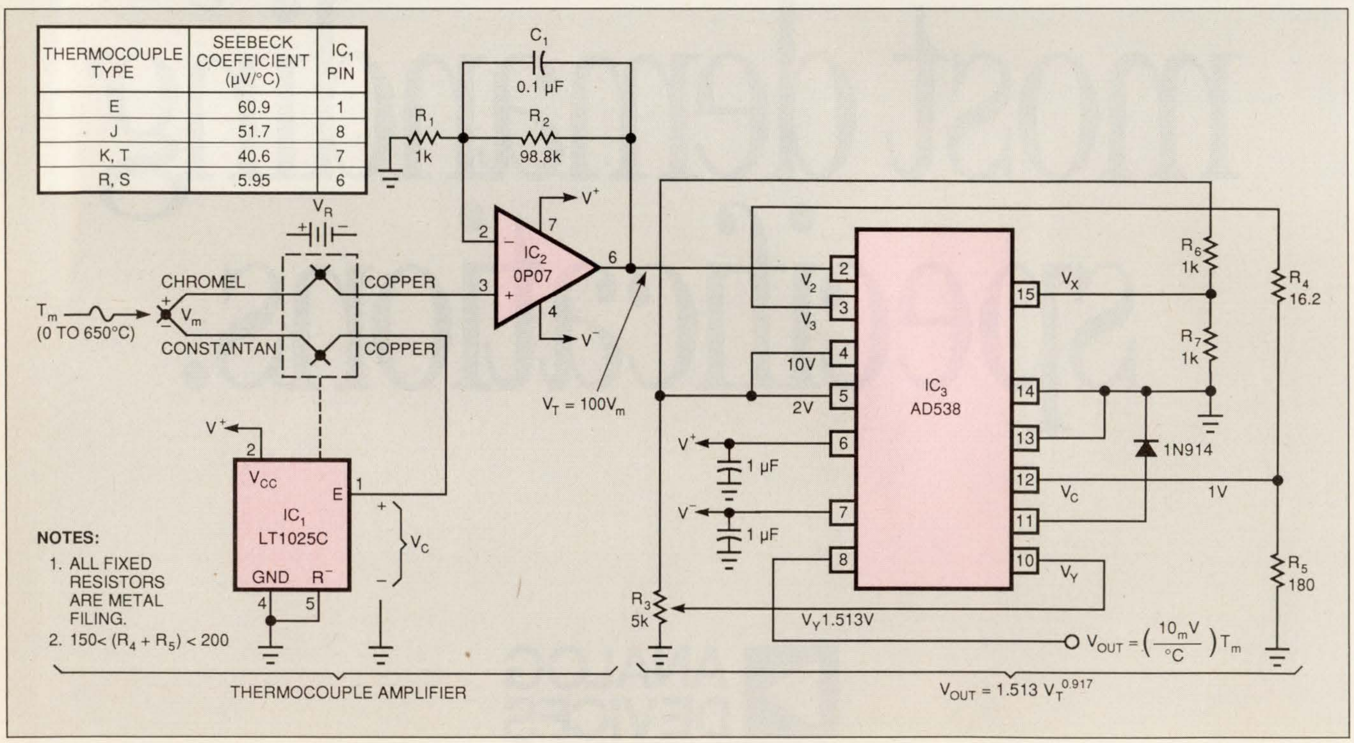
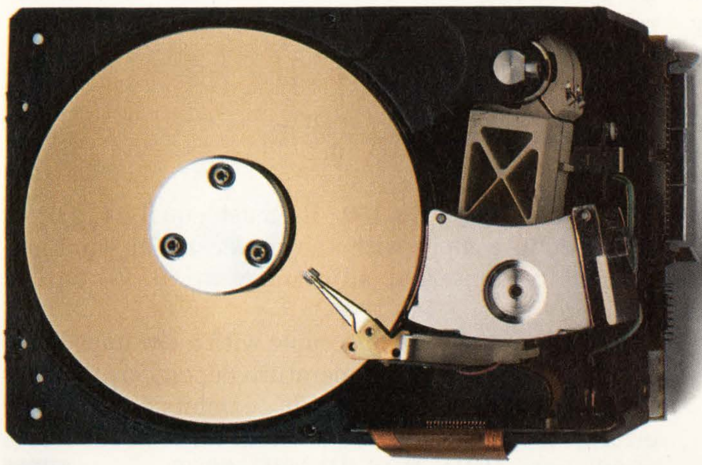


Fig 1—A ***cold-junction compensator, amplifier,*** *and a computational IC linearize a type-E thermocouple with the help of a calculator's curve-fitting algorithm.*

Faster.



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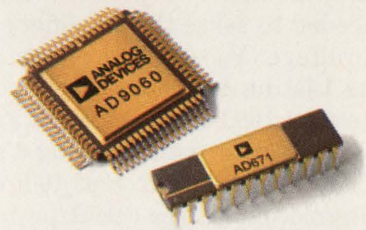

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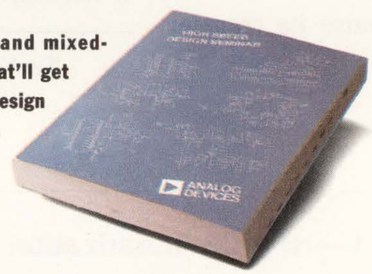

AD9712 – The only 12-bit, 100 MHz D/A converter on the market. Ideal for high-speed video and direct digital synthesis, its low glitch and low harmonics combine to deliver a spectrally pure output waveform.

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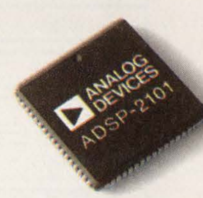

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CIRCLE NO. 103

and C_1 add a pole at about 16 Hz to filter power-frequency noise.

The HP-42S's curve-fitting software finds a mathematical model to describe the linearization circuitry needed to sense the amplifier's output (V_T) and output a voltage (V_{OUT}) with a system sensitivity of 10 mV/°C. As **Listing 1** indicates, you must set the calculator to its statistical mode and input a minimum of 13 separate V_T/V_{OUT} data pairs. **Listing 1**'s data points, which include a scaling factor of 100, correspond to a type-E thermocouple. The calculator uses standard regression techniques to select from its linear, exponential, logarithmic, and power models the one that best fits the data. The model that best describes **Listing 1**'s keystroke entries is the following power curve:

$$V_{OUT}=1.513V_T^{0.917}.$$

IC_3 can implement this function because its transfer function is

$$V_{OUT}=V_Y\left(\frac{V_Z}{V_X}\right)^m.$$

The exponent m can take any value from 0.2 to 5.0.

Fig 1 applies V_T to IC_3's V_Z input, and sets V_X to 1V by dividing down IC_3's 2V reference. To take the root of V_Z/V_X, R_5 and R_4 must have the following relationship.

$$R_4=\left(\frac{1-m}{m}\right)R_5.$$

Thus, with R_5 set to 180, R_4 must equal 16.2Ω. To scale IC_3 to comply with the power-model equation, R_3 requires external adjustment until V_Y equals 1.513V.

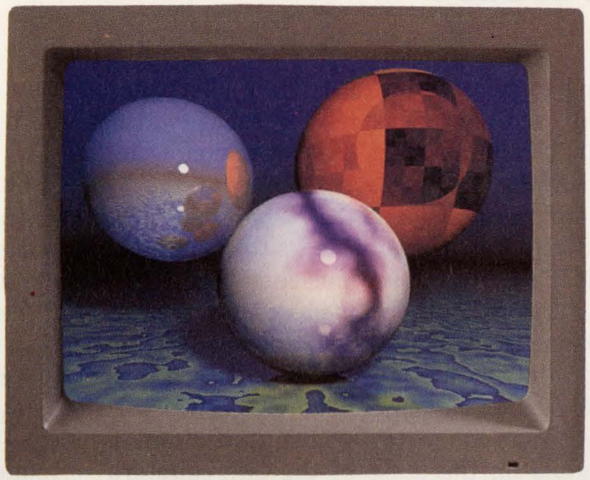
By replacing the thermocouple with a low impedance source to simulate its temperature dependent voltage, the output voltage at pin 8 of IC_3 exhibits a worst-case error at 600°C of 8.7°C (V_{OUT}=6.087V), or about 1.34% of full scale. (**EDN BBS /DI_SIG #930**) **EDN**

To Vote For This Design, Circle No. 750

Listing 1—HP-42S linearization keystrokes

SHIFT	STAT	▼	ALL Σ	EXIT	SELECT ALL SUMMATION REGISTERS
SHIFT	CLEAR	CL Σ			CLEAR SUMMATION REGISTERS
0.5	ENTER	0.3047	Σ+		
1.0	ENTER	0.6317	Σ+		
1.5	ENTER	0.9787	Σ+		
2.0	ENTER	1.3419	Σ+		
2.5	ENTER	1.7178	Σ+		
3.0	ENTER	2.1033	Σ+		MINIMUM OF 13 DATA PAIRS
3.5	ENTER	2.4961	Σ+		KEY IN V_{OUT} PRESS ENTER
4.0	ENTER	2.8943	Σ+		KEY IN 100 V_{m_1} PRESS Σ+
4.5	ENTER	3.2960	Σ+		
5.0	ENTER	3.6999	Σ+		
5.5	ENTER	4.1045	Σ+		
6.0	ENTER	4.5085	Σ+		
6.5	ENTER	4.9109	Σ+		
SHIFT	STAT	CFIT	MODEL	BEST	SELECT CURVE-FITTING MODEL THAT BEST FITS DATA
EXIT					RETURN TO CURVE FIT SUBMENU
SLOPE		X: 0.917			DATA RETURNED
INT		X: 1.513			DATA RETURNED

Better.



Picture this – a PC monitor that offers the same color and clarity as a high-end engineering workstation costing as much as 20 times more. Our pin-compatible RAM-DAC is literally redefining the low end of the PC monitor market.

Marball. Original image courtesy of University of California, Davis.

'Try, try again' is a costly way for manufacturers to find the best design solution. So to help our customers find answers to tricky problems the first time around, technical application engineers are just a phone call away. In some instances, they're even located right on the customer's premises.

After analyzing semiconductor suppliers, many of the leading oscilloscope and spectrum analyzer manufacturers chose Analog Devices for their mixed-signal components. One reason is our ability to deliver high performance at high levels of integration – for example, our AD640, which replaces a chain of discrete log-amps for higher accuracy.

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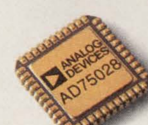

AD75028 – This custom ASIC passes the test for a top automatic test equipment manufacturer. Serving the function of 21 separate 12- and 8-bit D/A converters and providing on-chip static RAM, it also has seven channels of level setting (other monolithics only have four), and can automatically remove gain and offset errors.

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CIRCLE NO. 104

VFC rejects common-mode noise

Luchezar M Iliev
RDIA Scientific Instrument, Sofia, Bulgaria

The VFC (voltage-to-frequency converter) in **Fig 1** synchronizes its conversion periods to the cycling of the ac power line in a novel fashion. Such synchronizing helps the converter reject common-mode noise because much common-mode noise occurs at odd harmonics of the power-line frequency. Integrating over an even number of power-line cycles averages such noise out. Consequently, the 15-bit VFC achieves a 75-dB common-mode rejection ratio.

An extra winding on the converter's power-supply transformer applies a lowpass-filtered, power-line signal to IC_3. IC_3 and associated components form the power-line sinusoid into a train of short pulses occurring at each power-line zero crossing (waveform C in **Fig 2**). The pulses start the conversion cycle.

Synchronizing pulses start one of the two 14-bit counter/timers, IC_6 and IC_7, and then the other. A 32.768-kHz watch crystal clocks the timers. The timers output a pair of 0.5-sec pulses shifted in phase with respect to each other by one-half the period of the power-line frequency (waveforms A and B in **Fig 2**).

The 4-into-1 multiplexer, IC_2, passes one of three signals—either no signal, the V/F converter's output, or the V/F converter's output divided by two—depending on the state of the two counters' outputs (waveform F_{IN} in **Fig 2**).

To understand the point of this curious series of

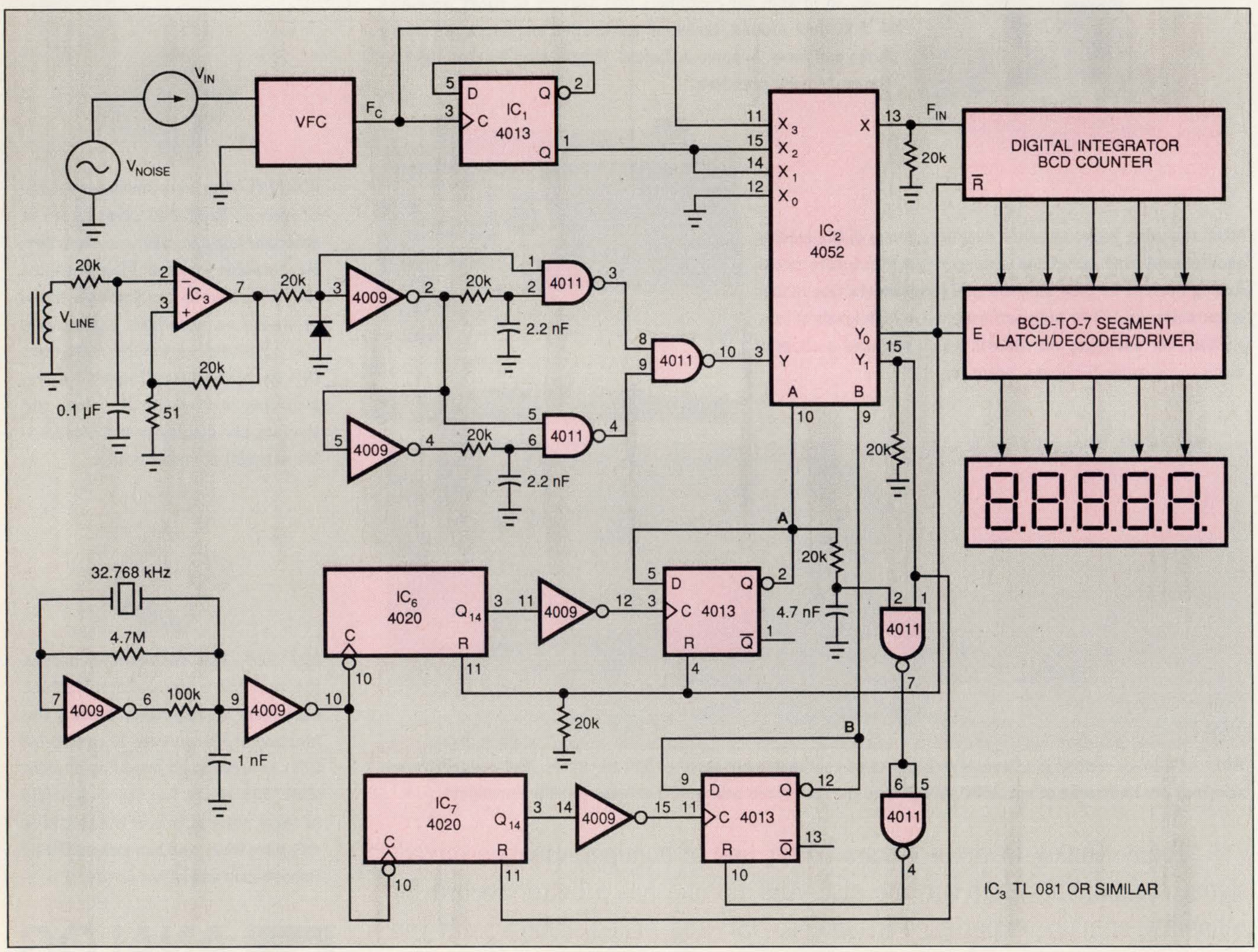

Fig 1—This circuit integrates the input signal *over a series of periods related to the power-line frequency to eliminate harmonic-related noise.*

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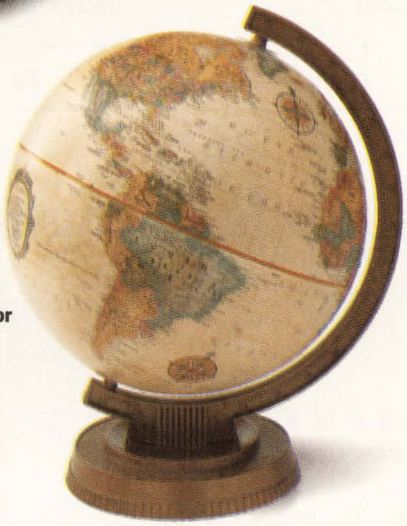
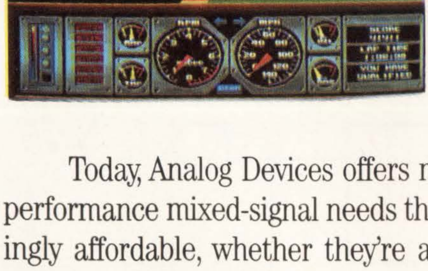


We're far from your local component boutique. Over half of our $540 million in revenues comes from international sales. And with manufacturing and stocking facilities on just about every continent, getting products to you quickly is a snap. Plus multiple manufacturing facilities allow us to take advantage of the right talent and processes for the job at hand.



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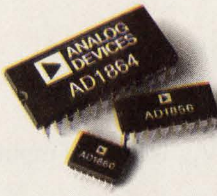

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CIRCLE NO. 105

integrations, first consider these three integrals:

$$w=\int_0^{T_1}\frac{1}{2}[V_{IN}+V_{NOISE}(t)]\,dt+\int_{T_1}^{T_0}[V_{IN}+V_{NOISE}(t)]\,dt+\int_{T_0}^{T_0+T_1}\frac{1}{2}[V_{IN}+V_{NOISE}(t)]\,dt.$$

where V_{IN} is the dc input signal to be measured. And

$$V_{NOISE}=\sum_{k=1}^{\infty}(a_k\cos k\,\omega_1 t+b_k\sin k\,\omega_1 t)$$

is the Fourier transformation of the line noise. The Fourier transformation of the first three integrals is

$$W=V_{IN}\,T_0-\sum_{k=1}^{\infty}\frac{c_k\,T_1}{2\pi k}[\cos\alpha_k-\cos_{\phi_k}+\cos(k\pi+\alpha_k)-\cos(k\pi+\phi_k)],$$

where

$$\alpha_k=\pi k\frac{T_0}{T_1}+\phi_k,$$

$$\phi_k=\arctan\frac{a_k}{b_k},\ \text{and}$$

$$c_k=\sqrt{a_k^2+b_k^2}\,.$$

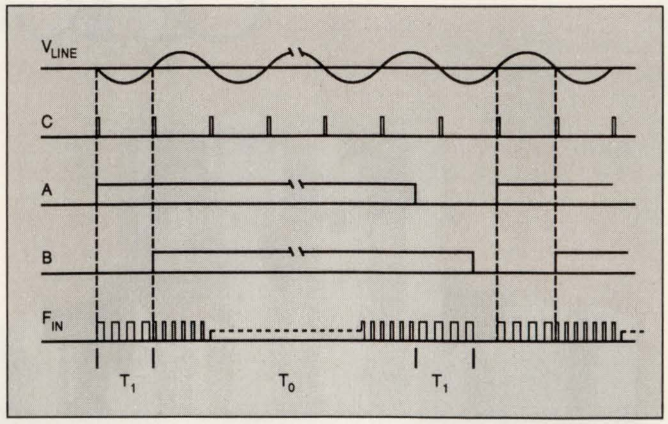


*Fig 2—**Depending on the state of the outputs** of a pair of counters, the circuit integrates (counts up) either the output of the V/F converter or the output of the V/F converter divided by two.*

An analysis of this solution reveals that the circuit's order of integration cancels all the odd harmonics of the power-line frequency, including the fundamental. Also note that you can shift the synchronizing signal, which kicks off the series of integrations in phase without decreasing the rejection effect.

(EDN BBS /DI_SIG #923) **EDN**

To Vote For This Design, Circle No. 848

SR flip-flop responds to edges

Ricardo O Rabinovich
Librascope Co, Glendale, CA

The edge-sensitive, set-reset flip-flop in **Fig 1** fills a gap in the discrete logic lineup. The circuit combines characteristics of an asynchronous, set-reset flip-flop and an edge-triggered JK flip-flop. It changes states on the leading edges of its inputs, but ignores the inputs' levels at all other times.

Inputs connect to the D flip-flops' CK (clock) inputs. The D flip-flops' D inputs actually function as negative-true qualifiers, $\overline{\text{SETEN}}$ and $\overline{\text{RESETEN}}$, for their respective inputs. The $\overline{\text{CLEAR}}$ clears the flip-flop.

Note that in operation, the outputs of both D flip-flops are normally high, going low only for brief periods after seeing an edge at their respective clock inputs. The classical, cross-coupled NAND gates following the D flip-flops actually latch the circuit's state.

(EDN BBS /DI_SIG #925) **EDN**

To Vote For This Design, Circle No. 849

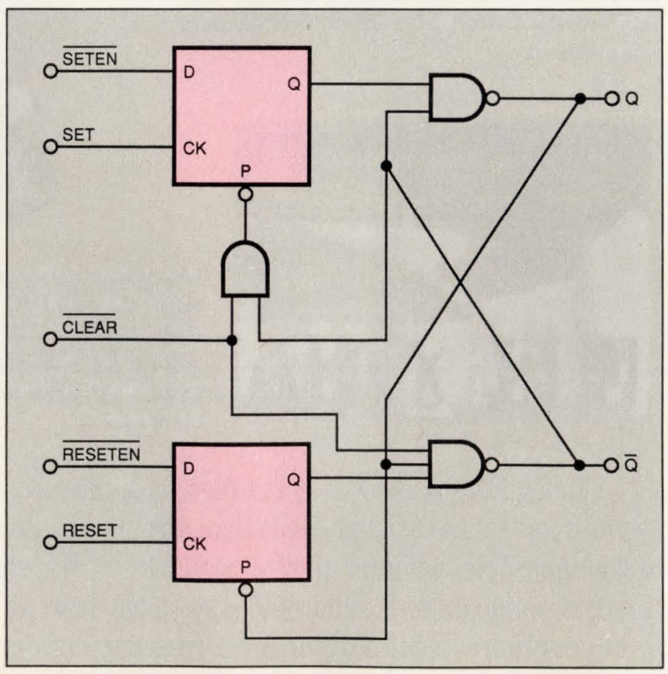
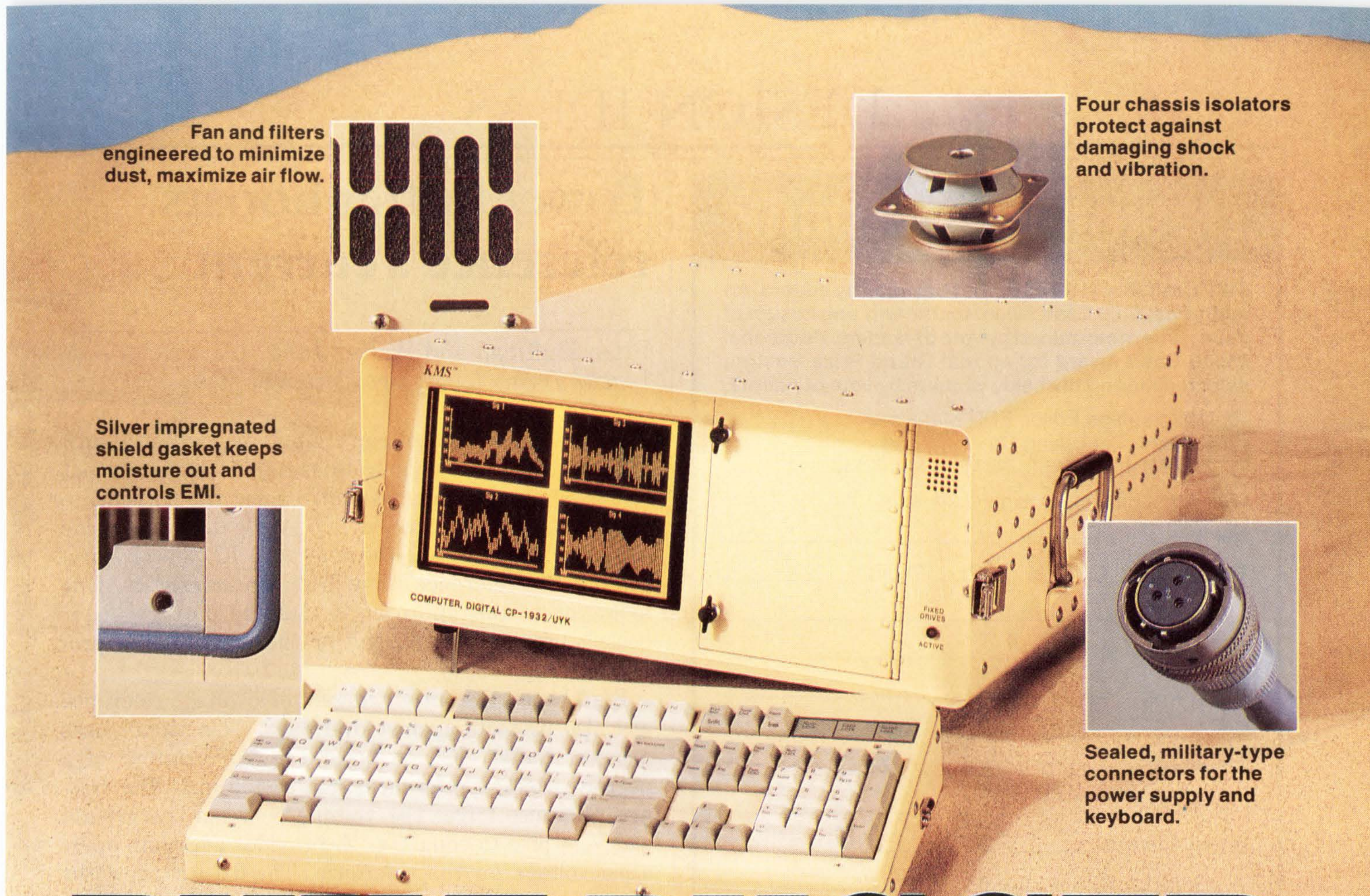


*Fig 1—**This circuit forms** an edge-triggered, set-reset flip-flop.*



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CIRCLE NO. 100

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ISSUE WINNER

The winning Design Idea for the October 11, 1990, issue is entitled "Hall sensor detects ground faults," submitted by V Lakshminarayanan of Centre for Development of Telematics (Bangalore, India).

The winning Design Idea for the October 25, 1990, issue is entitled "Three ICs produce pure sine waves," submitted by Bruce Saldinger of Maxim Integrated Products, Sunnyvale, CA.

Power buffer boosts reference's current

Brian Huffman and Walter Jung
Linear Technology Corp, Milpitas, CA

Most voltage references can't supply more than 10 mA of current, but many applications require higher output levels. Some approaches for increasing the current involve placing a pnp-transistor power gain stage inside a feedback loop around the reference IC, thereby preserving the reference's low-drift characteristics. One limitation to this approach is that the pnp transistor doesn't provide short-circuit or thermal-overload protection.

Fig 1 boosts the output current of a voltage reference and also protects against overloads. This circuit uses a power buffer, IC_1, to boost the $-5V$ output of a negative voltage reference, IC_2, to 100 mA. The voltage reference forces the voltage between the ground and V_{OUT} pins to equal 5V. Z_1 provides adequate operating voltage for the reference. The 0.1-μF capacitor across Z_1 filters noise generated by the Zener diode. R_1 and R_2 provide sufficient operating current for the reference and diode. The RC damper on the V_{IN} pin provides stable loop compensation for typical load conditions. The output may oscillate if you use low ESR capacitors. Therefore, use aluminum electrolytic or tantalum capacitors instead of ceramic or mylar.
(EDN BBS DI #907) EDN

To Vote For This Design, Circle No. 850

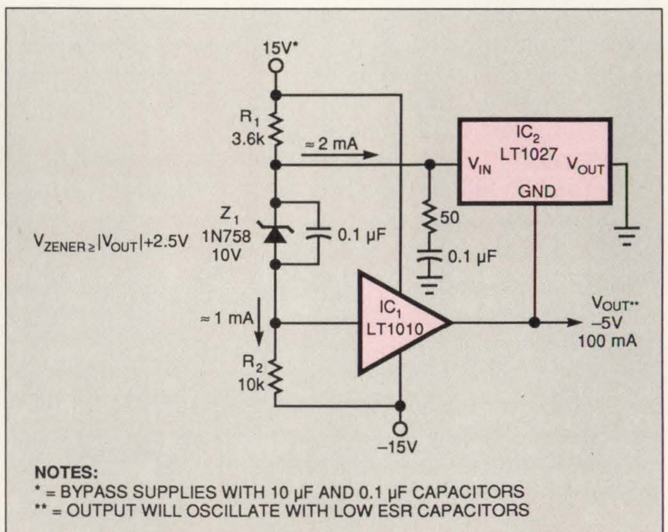

Fig 1—A power buffer, IC_1 in the feedback loop of a negative voltage reference, IC_2, boosts the reference's output current to 100 mA.

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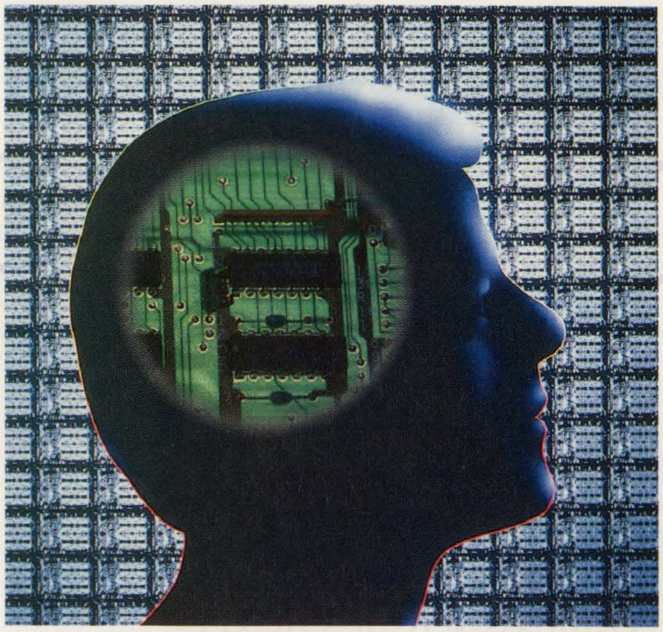

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When a system exceeds restrictions, designers are often forced to trade efficiency for acceptable EMC performance—with undesirable results. As a finished design is modified to accommodate necessary remedial shielding measures, weight and volume inevitably increase, and overall efficiency drops.

Planned EMC controls and testing during the design phase, on the other hand, not only help you maintain the integrity of the original design, but allow modifications in favor of greater system efficiency. In computer design, for example, EMC considerations such as selecting lower clock frequency, maintaining the smallest possible circuit layout areas, utilizing multi-layer boards, and minimizing the use of multiple shielding all contribute to optimum design efficiency.

The three EMC design techniques.

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TEL: 32-41-63-3021 FAX: 32-41-46-4862

Latin America, Middle East, except Israel: Beekman Laboratories, Inc., 914-472-6600; **Portugal:** Componenta Lda. 351-1-3621283; **Sweden:** LTG Marketing AB, 46-8-7039380; **Finland:** Euroshield OY, 358-38-50631; **Norway:** Feiring, 47-2-649070; **France:** Phytronic, 33-1-69-03-21-06; **UK:** Ramp Electronics, 44-703-260161; **Canada:** A.C.Simmonds & Sons, Ltd., 416-839-8041; **Switzerland, Austria, Liechtenstein:** KAB AG, 41-1-7342000; **Italy:** Sirces SRL, 39-2-57404962; **Israel:** Grand Central, Tech., 972-52-547520; **Germany:** Microscan GMBH, 49-89-964841; **Denmark:** SC Metric A/S, 45-42-804200; **Belgium, Luxembourg:** ACAL 32-2-720-5983; **Netherlands:** ACAL, 31-40-816565, Bodamer BVBA 32-2-452-3990; **South Africa** Connecta C.C., 27-11-4632240; **Spain:** Amitron Pasivos, 34-1-5420906; 34-3-4907494; **Turkey, Greece:** Oakdale Industrial Electronics Corp. 516-737-8013.

CIRCLE NO. 99

DESIGN IDEAS

FEEDBACK AND AMPLIFICATION

Reversed connections invert transfer function

The circuit schematic in "Commutating amp multiplies precisely," EDN, October 25, 1990, pg 203, /DI_SIG #900, has some errors. The published version, although functional, will produce an inverted transfer function: $V_{OUT} = -(V_X V_Y)/10$. First, you should ground pin 1 of the first AD630. Secondly, reverse the connections of pins 9 and 10 of the second AD630.

Moshe Gerstenhaber, product engineering manager
Analog Devices
804 Woburn St
Wilmington, MA 01887-3462
(617) 935-5565

Design Idea omits compass-sensor's maker

The Design Idea (DI #910), "Sensor and logic form digital compass" (EDN, December 6, 1990, pg 228), made it to print without identifying the circuit's key component, a Hall-effect sensor. The sensor's maker is: Dinsmore Instrument Co, Box 345, Flint, MI 48501, (313) 744-1330.

Semi maker agrees with Design Idea

I think that Tarlton Fleming's Design Idea, "Programmable amp provides arbitrary gain" (EDN, September 3, 1990, pg 174), is a very clever idea. Apparently National Semiconductor thought it was a clever idea also, as anyone can see from the data sheet for their LH0084.

Carl Spearow
Sundstrand Electronic Systems, 709-6
Box 7002
Rockford, IL 61125

EDN's bulletin board is on line

Call EDN's free bulletin board service (BBS) at (617) 558-4241 (1200/2400,8,N,1) and select /DI_SIG to get additional information or to comment on these Design Ideas.

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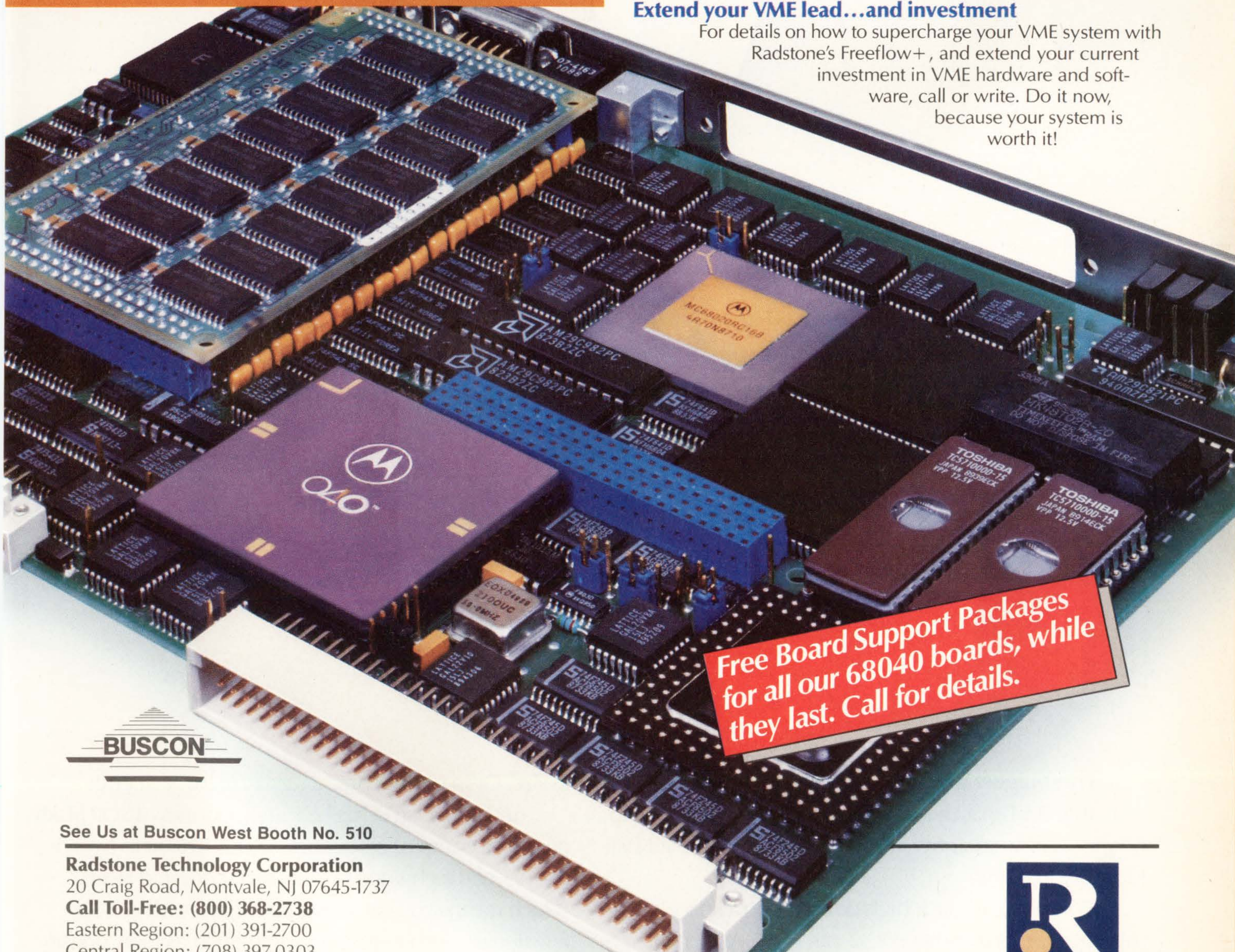

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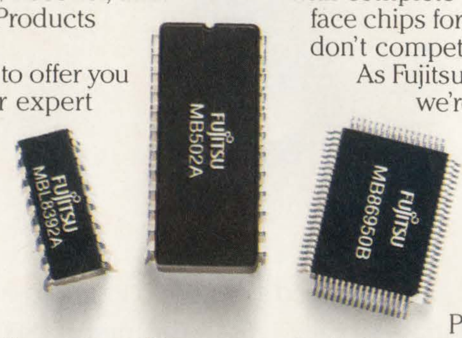

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NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

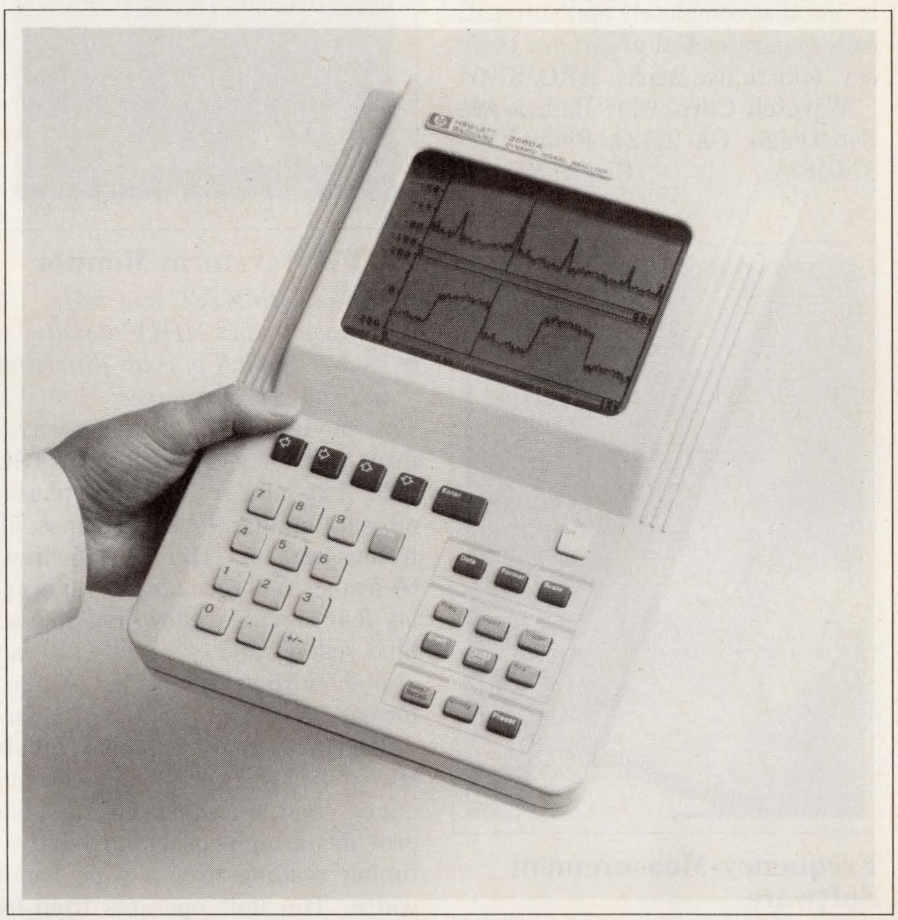
Notebook-Size FFT Analyzer

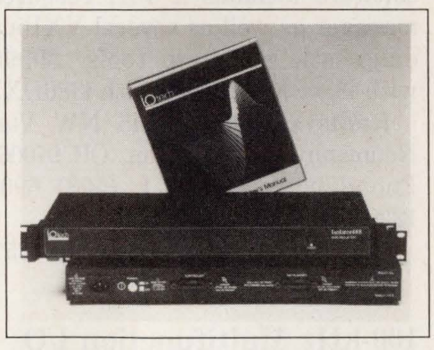
- *Covers dc to 40 kHz*
- *Provides 70-dB dynamic range and ±0.5 dB accuracy*

The HP 3560A FFT-based dynamic-signal analyzer weighs 7 lb and operates for 6 hours from internal batteries. It also operates from ac power and simultaneously recharges its batteries. An option lets it run and recharge from a 12V dc source. The unit processes signals with a frequency content of dc to 40 kHz. It has a dynamic range of 70 dB and an accuracy of ±0.5 dB. You can set up the display to resolve from 101 to 1601 lines. An RS-232C port sends plots directly to hardcopy graphics devices such as printers. The interface is compatible with the vendor's Laserjet and Quietjet printers as well as with units that support HPGL (Hewlett-Packard Graphics Language). $7500.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 351





IEEE-488 Bus Isolator

- *Provides 1500V isolation between instrument and bus grounds*
- *Does not occupy a bus address*

Isolator488 is a unit that you interpose between the IEEE-488 bus and an instrument connected to the bus. The unit provides 1500V of ohmic isolation between the ground system of the instrument and that of the bus. The isolation allows you to make some measurements you could not otherwise make; in other cases, it greatly increases measurement accuracy by reducing the effects of common-mode interference. The isolator is ac powered and does not occupy a bus address; from a data-transfer standpoint, it has no effect on the operation of the bus. You can configure the unit so that either or both of the IEEE-488 connectors on the rear panel (one is for bus input; the other for bus output) are isolated from power ground. $995.

IOtech Inc, 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093. TWX 650-282-0864.

Circle No. 352

Test-Development Software For DEC Workstations

- *Supports multiple users, multitasking, and networking*
- *Simultaneously controls IEEE-488 and VXIbus instruments*

Wavetest-XTM is software that helps test engineers develop procedures for instrument control, data acquisition, display, and analysis. The software runs on Digital Equipment Corp workstations under the Ultrix operating system. The host computers for the test setups are also DEC workstations. Supported instruments include units controlled via the IEEE-488 and VXI buses; you can use both types simultaneously. The software supports multitasking, multiple users, and networked CPUs. It provides a graphical user interface and allows plotting of data in real time. According to the vendor, the package is the only one that completely and automatically generates test programs. Delivery, four to five weeks, ARO. $7995.

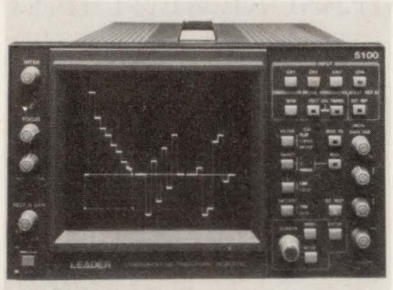
Wavetek Corp, 9045 Balboa Ave, San Diego, CA 92123. Phone (800) 874-4835. **Circle No. 353**

Frequency-Measurement Software

- *Works with vendor's 3052 DSP system*
- *Processes live and previously captured signals*

S2MG100 enhanced frequency-measurement software works with the vendor's 3052 digital signal-processing system. It improves the hardware's frequency-resolution capabilities by as much as 10 times. The software, which can operate on "live" data as the instrument captures it, or on previously recorded data, uses data from the signal processor's bank of 1024 digital filters. The system, which updates its spectral output every 200 μsec, has a span of 1 kHz to 10 MHz that you can center anywhere in a 10-MHz band. $5000.

Tektronix Inc, Box 4490, MS 38-386, Beaverton, OR 97076. Phone (503) 627-2589. **Circle No. 354**



HDTV Waveform Monitor

- *Works with NTSC and PAL composite and HDTV signals*
- *Vector display of color difference indicates chrominance*

The model 5100 television-waveform monitor lets you select NTSC (525 lines, 60 frames/sec), phase-alternating line (PAL) (625 lines, 50 frames/sec), or HDTV (1125 lines, 60 frames/sec) formats. It can overlay four signals: yellow, red-yellow, blue-yellow, and composite. It can also show three signals in "parade" format. A vector display of color-difference or red-green-blue signals lets you check component chrominance, and a "shark-fin" display provides a high-resolution relative-timing reading over a wide bandwidth. The unit operates from 90 to 250V ac sources or from 12V dc. $3800.

Leader Instruments Corp, 380 Oser Ave, Hauppauge, NY 11788. Phone (800) 645-5104; in NY, (516) 231-6900. **Circle No. 355**

SCSI Bus Analyzer/Emulator

- *Captures 32k 56-bit frames at 20 MHz*
- *Provides 15-level sequential triggering*

The OZ-201 SCSI bus emulator/analyzer can simultaneously act as a bus initiator and a target device. Thirty-three LEDs continuously display the bus status and data-communications activity. The instrument's 32k-frame buffer captures 56-bit-wide traces of bus activity either synchronously or asynchronously at speeds to 20 MHz. Sequential triggering has 15 levels with data qualification, phase skipping, and parity checking. An IBM PC/AT-compatible personal computer controls the emulator/analyzer. The instrument fits between the computer's monitor and its system unit. The computer displays the captured data in industry-standard mnemonics or in symbols that you define. $5995.

Biomation Inc, 19050 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 538-9320; in CA, (408) 988-6800. FAX (408) 988-1647. **Circle No. 356**

B-Size VXIbus Systems

- *Include 12-slot mainframe and slot-0 controller*
- *Provide choice of CPU*

The VXI-B series systems consist of a portable, 12-slot, B-size mainframe with power supply, a slot-0 controller, and a choice of two hard-disk-based CPU modules. One module employs a 25-MHz i386DX, and the other module uses a 16-MHz i386SX. Also included are MS-DOS, Windows/386, and the vendor's EPConnect/VXI software. This software includes a VXI resource manager as well as several VXIbus diagnostic software tools. $9995 with i386SX; $12,285 with i386DX.

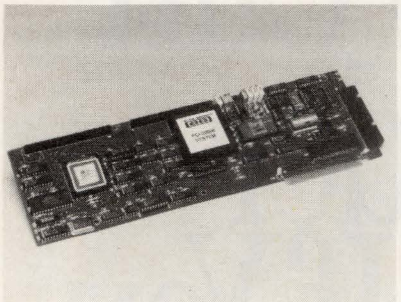
Radisys Corp, 19545 NW Von Neumann Dr, Beaverton, OR 97006. Phone (800) 950-0044; (503) 690-1229. FAX (503) 690-1228. **Circle No. 357**

100-kHz Multifunction I/O Board For IBM PC Bus

- *Includes analog inputs, digital I/O, counters, and timers*
- *Supports DMA operation*

The PCI-20098C-2 is a configurable, multifunction analog/digital I/O board for the IBM PC bus. The board provides 16 single-ended analog input channels (eight differential), 16 digital I/O channels, two

counter/timers, and a timebase/burst-rate generator. It operates in both DMA and interrupt-driven modes. Maximum sampling rate of the analog inputs is 100k samples/sec. You can program gains of 1,



10, 100, and 200. Each channel can have a different gain. Plug-in modules let you increase the channel capacity to 80 analog inputs, 80 digital I/O lines, or a combination of the two. A diagnostic software disk accompanies the board; the vendor offers software drivers for Basic, C, and Turbo Pascal. $995.

Burr Brown/Intelligent Instrumentation, 1141 W Grant Rd, MS131, Tucson, AZ 85705. Phone (602) 623-9801. FAX (602) 623-8965.

Circle No. 358

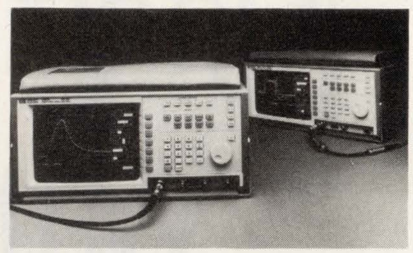
Floppy-Disk-Drive Test Software

- *Cleans drives and diagnoses faults*
- *For IBM PCs with 3½ and 5¼-in. drives and Macintosh models*

Generation 3.0 software tests floppy-disk drives to determine how accurately each head reads and writes. It then generates reports showing the accuracy. Based on the test results, it recommends either a routine or an extended head-cleaning procedure. The procedure incorporates a patented brush-like cleaning disk that scrubs the heads. The solvent for the cleaning process is distributed in a dispenser that resembles a felt-tipped pen. The software also performs a drive-speed test that displays rotational speed with a resolution of 0.01 rps. Versions are available for MS-DOS-based systems using 3½-in. and 5¼-in. drives and for the Apple Macintosh. $34.95 to $44.95.

Trackmate America Corp, 14577 S Bascom Ave, Los Gatos, CA 95032. Phone (408) 356-0795.

Circle No. 359



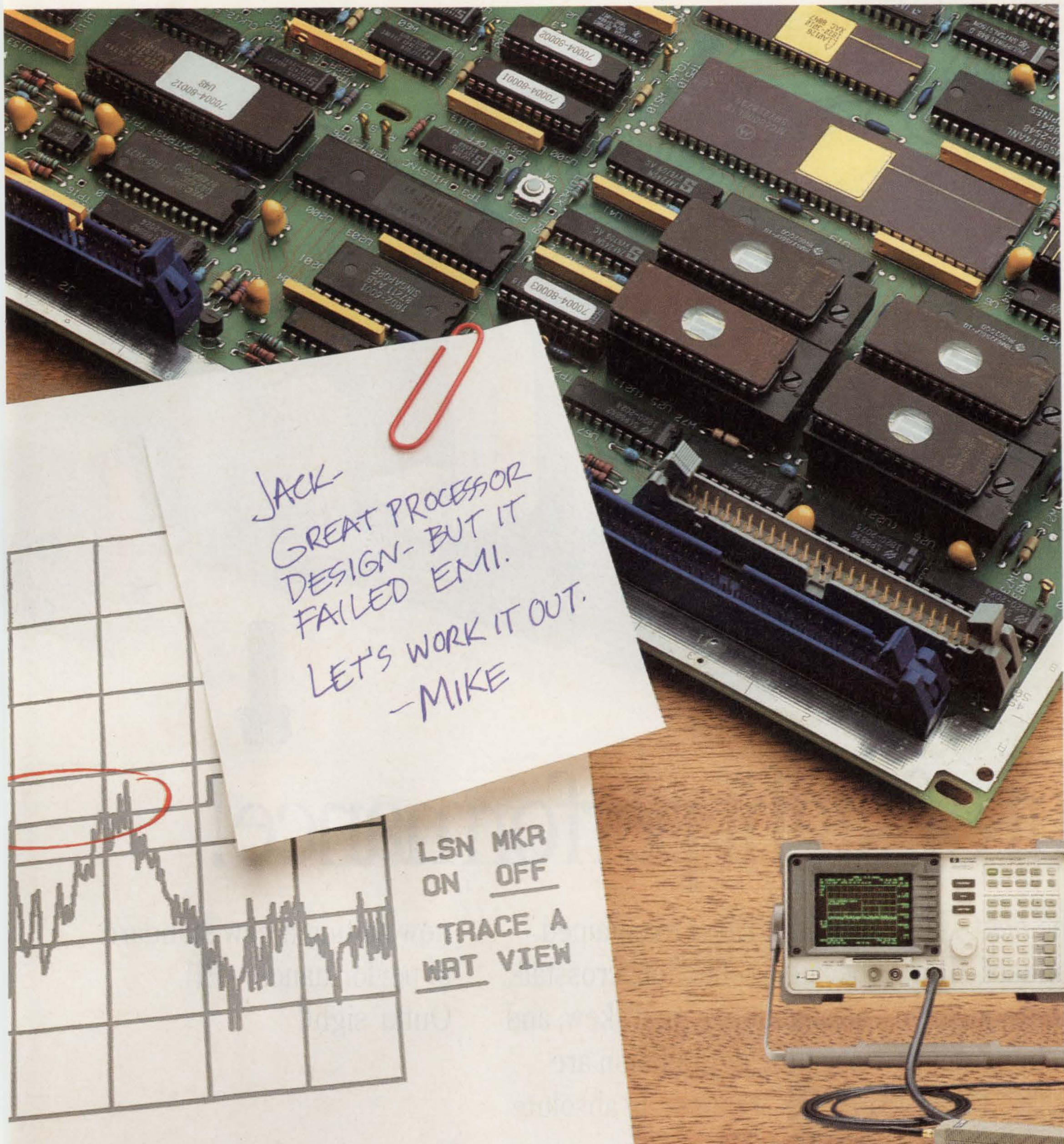
Telecom DSOs

- *Measure telecom pulse fidelity*
- *Store 16 masks in read-only memory*

When equipped with Option 001, the vendor's 54502A (2-channel, 400M sample/sec, real-time sampling) and 54503A (4-channel, 500-MHz bandwidth for repetitive signals only) digitizing oscilloscopes can make template measurements in accordance with ANSI, CCITT, and integrated-services digital network standards. The option adds a read-only memory containing 16 standard masks. The scope automatically aligns a waveform with the selected mask and determines the acceptability of the waveform by comparing it point-by-point to the mask. The scope then outputs failing waveforms for printing or plotting. The option adds $500 to the cost of the $6450 54502A or the $5450 54503A; you can add the option to existing instruments.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 360



Build EMC into your design now, and it won't be a problem later.

With all the new regulations surrounding electromagnetic compatibility (EMC), the best way to avoid costly delays is to locate problems as early as possible. Two new HP EMC solutions make that easy.

The HP 84100A Design Development Solution helps you correct problem areas at the design stage. It pinpoints hot spots on breadboards and prototypes using a spectrum analyzer with software memory cards that simplify troubleshooting.

The HP 84110A Pre-Production Solution gives you added confidence that your designs will pass compliance. It has all the analysis capability, software and accessories you need to uncover conducted and radiated emission problems before final EMI testing.

So, find out how to build EMC into your designs. For information about HP's full line of EMC solutions and design training programs, call **1-800-752-0900.*** Ask for **Ext. 1350,** and we'll send you our EMC Measurement Solutions fact kit.

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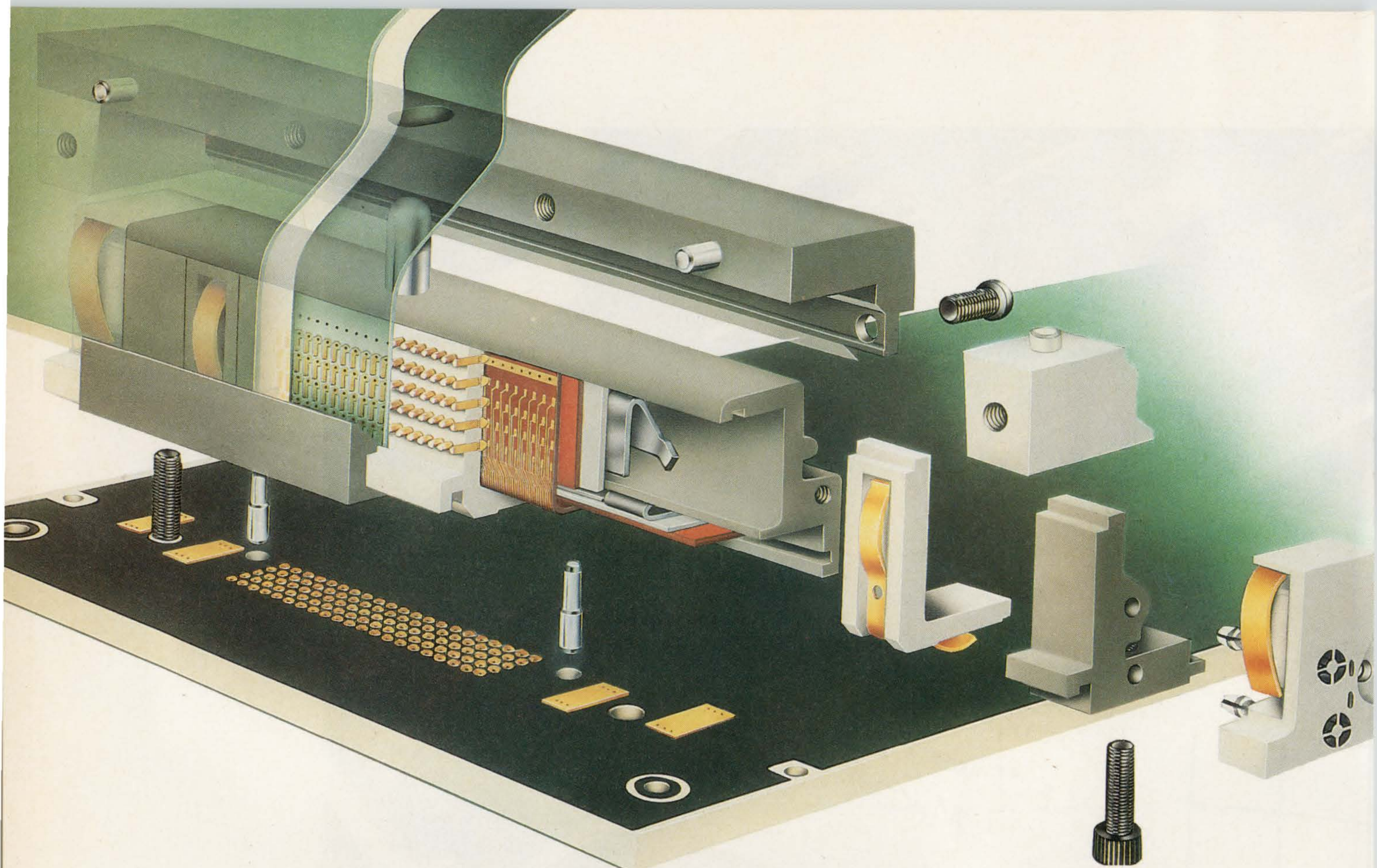
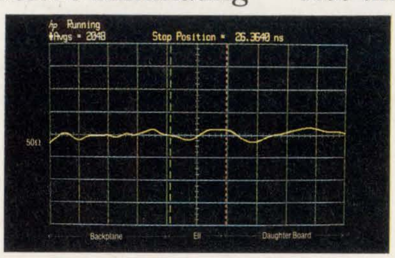
*In Canada, call 1-800-387-3867, Dept. 502

CIRCLE NO. 107



Out of sight performance!

Introducing the next generation interconnect, EII : transparent to high frequency signals, therefore eliminating connector induced signal distortion. Until now, the limiting factor for signal integrity in high speed electronic circuits has been the connector. The source may be matched to the load, but an impedance mismatch at the connector degrades performance. Signal integrity through EII is maintained because reflection, crosstalk, attenuation, signal skew, and rise-time degradation are reduced to absolute minimums.



EII achieves matched impedance of the connector to the backplane and daughter card.

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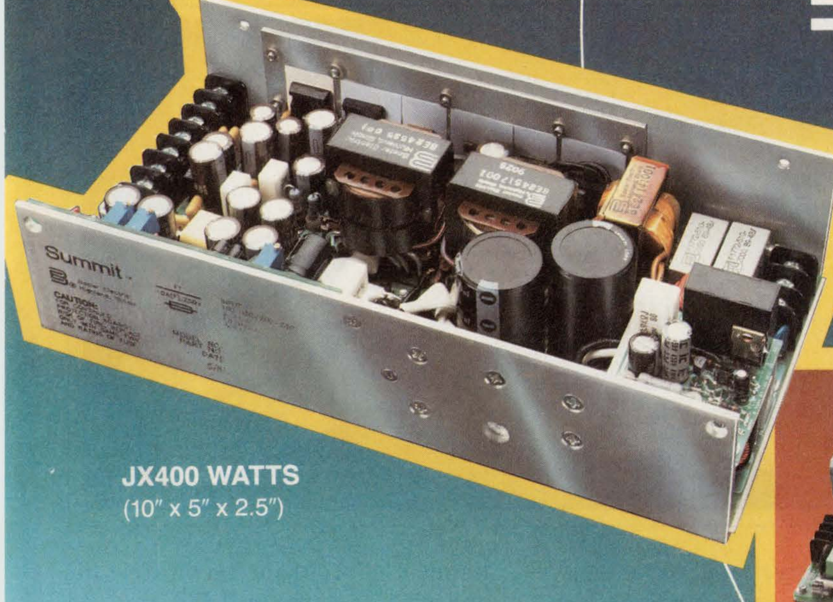

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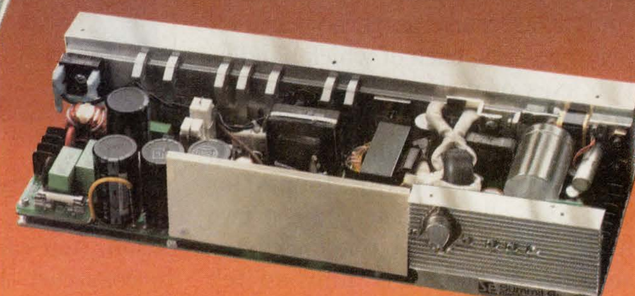
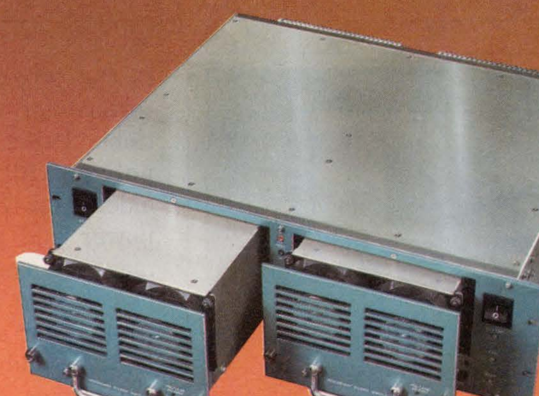


500/750 WATTS



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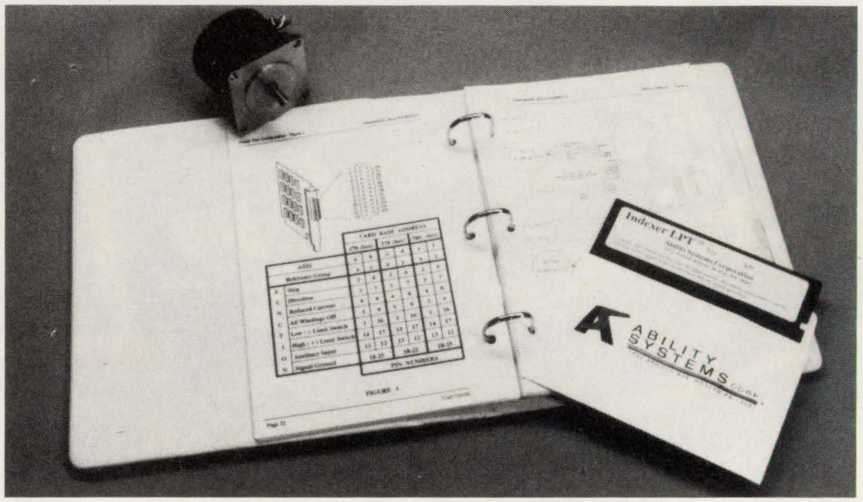
CIRCLE NO. 109

CAE & SOFTWARE DEVELOPMENT TOOLS

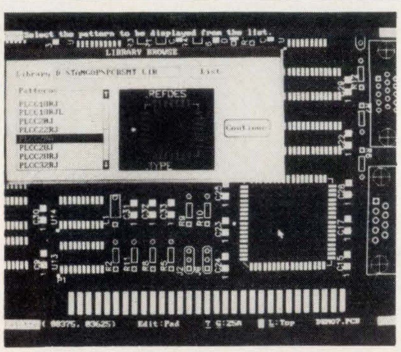
Stepping-Motor MS-DOS Driver

- *Uses a parallel-printer port to control a multiaxis motor*
- *Provides linear or circular interpolation and velocity control*



Indexer LPT version 2.0 is a motion-control subsystem that loads as an MS-DOS device driver. You can use it with most programming languages such as Basic, C, Pascal, and MS-DOS batch files. The driver can control as many as three parallel-printer ports, each of which handles two axes of motion. The TTL-level output signals for each axis are Step, Direction, Reduced Current, and All Windings Off. Inputs for each axis allow you to connect two limit switches and one auxiliary sensing device. Any limit-switch closure automatically arrests motion. Other features include linear interpolation in as many as six axes simultaneously, rapid traversal, velocity control, and circular interpolation. You can use any text editor to construct ASCII command files for use by an application program; each line contains one Indexer LPT command per line. A menu-driven diagnostic program facilitates installation of Indexer LPT, and its documentation includes many sample programs. $249.

Ability Systems Corp, 1422 Arnold Ave, Roslyn, PA 19001. Phone (215) 657-4338. **Circle No. 361**



PC-Board Design Tool

- *Manual, interactive, or automatic component placement*
- *Able to handle 23 layers, including 10 signal layers*

Tango-PCB version 2.0 provides component-placement assistance, allowing placement to be manual, interactive, or fully automatic. The program now can handle four more mid-layers, yielding a total of 23 layers, 10 of which can be signal layers. You can now define your own macros to give you rapid access to the program's Windows-like interface for frequently used functions. Other new features include polygon fill, which replaces the older area fill; the ability to edit power and ground planes, which makes it easier to lay out analog boards; the ability to create "was/is" lists for use in back-annotation; and the addition of TIGA, Orchid, and Genoa graphics to the list of printer drivers. Tango-Route version 2.0 can handle all of the enhancements to Tango-PCB; in addition, the program can use expanded memory so that the board size is limited only by the amount of expanded memory in your system. From $495 for a single entry-level module; a bundled, professional pc board and autoroute combination, $1695.

Accel Technologies Inc, 6825 Flanders Dr, San Diego, CA 92121. Phone (619) 554-1000. FAX (619) 554-1019. **Circle No. 362**

File Conversion Tool

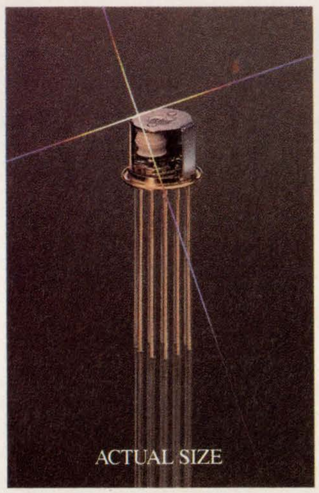
- *Lets SPARCstation read and write Macintosh and DOS files*
- *Works with 720k-byte or 1.44M-byte 3½-in. disks*

Common-Link is a file-transfer tool that runs on a Sun SPARCstation under SunOS release 4.1 or higher. It lets you transfer data files among SPARCstation, Macintosh, and IBM PC or compatible computers on a 3½-in. diskette. The tool can read MS-DOS files in 720k-byte double-density format or 1.44M-byte high-density format, and Macintosh files in 1.44M-byte high-density format, using the SPARCstation's built-in 1.44M-byte floppy-disk drive. You can also write SPARCstation files to a disk previously formatted by the target computer. If the transfer is between two versions of the same application program, the information is usable immediately, without further manipulation. If the creating application and the target appli-

TO-5 RELAY

The Unforgettable Maglatch TO-5

- Non-destructive memory
- Low power consumption
- Inherently bi-stable pulse operation
- CMOS compatible Centigrid® version



The Maglatch TO-5. It's a legend in its own time. The little magnetic latching relay that just won't forget. It can't. Because once you set it with a brief pulse of coil voltage, it simply stays in that state until reset. Even if the system loses power.

In applications where power drain is critical, the Maglatch TO-5 is unbeatable. Since no holding power is needed, it uses less energy than any other type of relay on the market.

The Maglatch's inherently low intercontact capacitance gives it high isolation and low insertion loss up through UHF, making it ideal for RF switching applications. And its tiny footprint makes it ideal for high density printed circuit boards.

The Maglatch TO-5 comes in commercial/industrial versions as well as military versions qualified to "L," "M" and "P" levels of MIL-R-39016. And now it comes in a CMOS compatible version as well. This version can be driven directly with CMOS level signals, with no outside amplification. That cuts down on the number of components and connections, for even greater system reliability.

The Maglatch TO-5. It's the world's smallest relay with indestructible memory. Call or write today for complete information.

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cation store data in different ways, you may need to perform further filtering or translation. Character-oriented (TTY) version, $150.

Pacific Micro, 201 San Antonio Circle, C250, Mountain View, CA 94040. Phone (800) 628-3475; in CA, (415) 948-6200. FAX (415) 948-6296.
Circle No. 363

Behavioral Entry System For FPGAs

- *Lets you design FPGAs using only Boolean descriptions*
- *Direct access to high-density FPGAs avoids partitioning*

Plustran Behavioral Entry System (BES) is an FPGA design tool that lets you design directly with ABEL, CUPL, PALASM, and other Boolean descriptions, enabling you to bypass the schematic-capture phase. If you have existing designs for PAL devices or PLDs, Plustran BES can accept the logic descriptions without modification, producing an efficient FPGA design that will reduce board space. The program runs on IBM PC/ATs and compatibles and Sun-3 or -4 Unix workstations. $475.

Plus Logic Inc, 1255 Parkmoor Ave, San Jose, CA 95126. Phone (408) 293-7587. FAX (408) 298-7587.
Circle No. 364

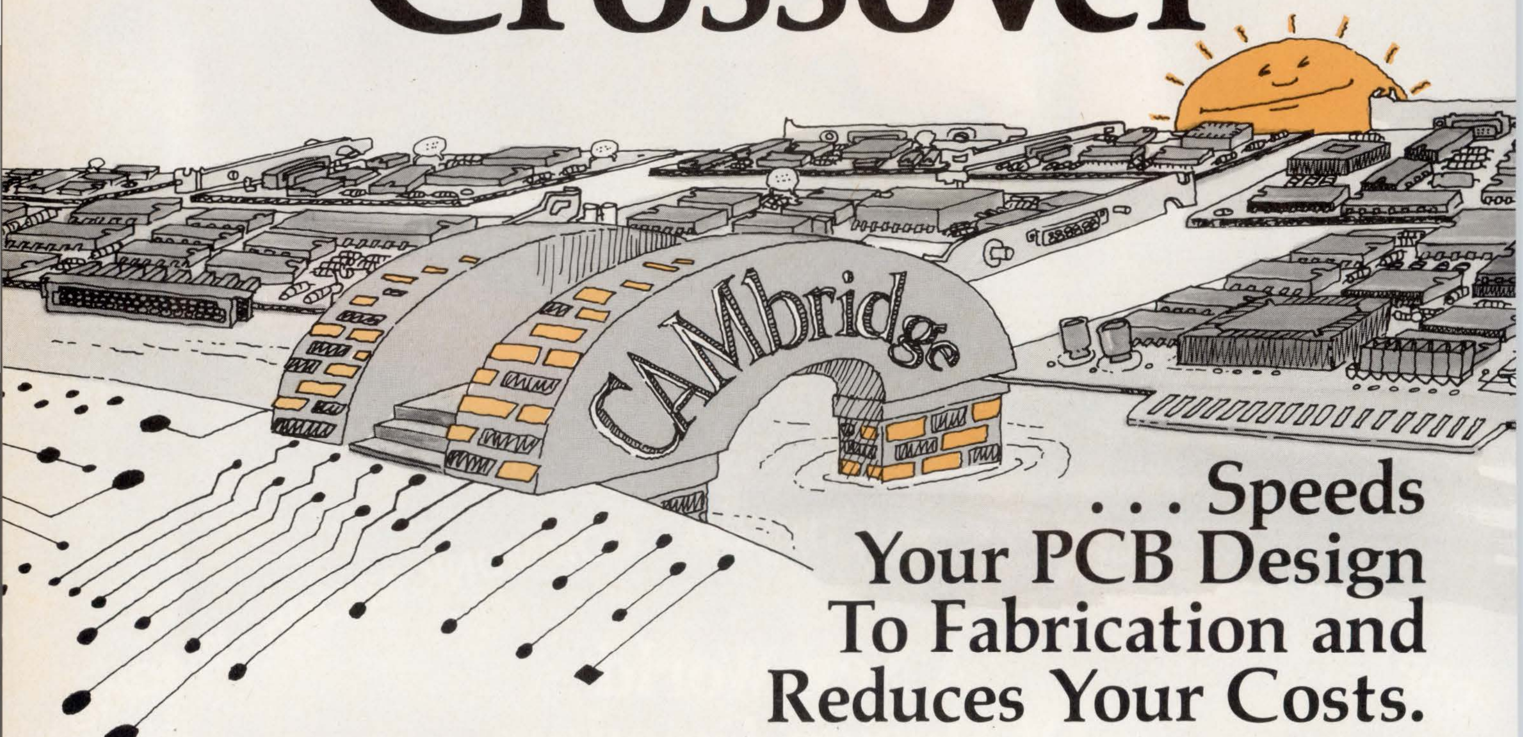
Translator Converts Force Files For 20 Simulators

- *Converts flat vector-stimulus files to other formats*
- *Handles high-level constructs found in Mentor Force files*

VTRAN is a program that loads the state/time information of simulation stimulus files and reformats the data for use by more than 20 widely used simulators. You can customize the format descriptors to describe both the input-data format and the output-data format. After loading the data, the program can perform some optional processing on the data before generating the output file. VTRAN works only on flat data files in tabular or script form; the XMENF module, however, works in conjunction with VTRAN. This translates and modifies Mentor Force files that contain high-level constructs such as DO macros, loops, and variables, which VTRAN is unable to handle alone. XMENF recognizes all of the Mentor syntax and commands that relate to the generation of simulation stimulus files. VTRAN, $2495; VTRAN with XMENF, $4995.

Source III Inc, 4960 Almaden Expressway, Suite 147, San Jose, CA 95118. Phone (408) 997-2575.
Circle No. 365

The CAMbridge Crossover



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Phone: (33) 1-46 04 30 47

CIRCLE NO. 108

NEW PRODUCTS

INTEGRATED CIRCUITS

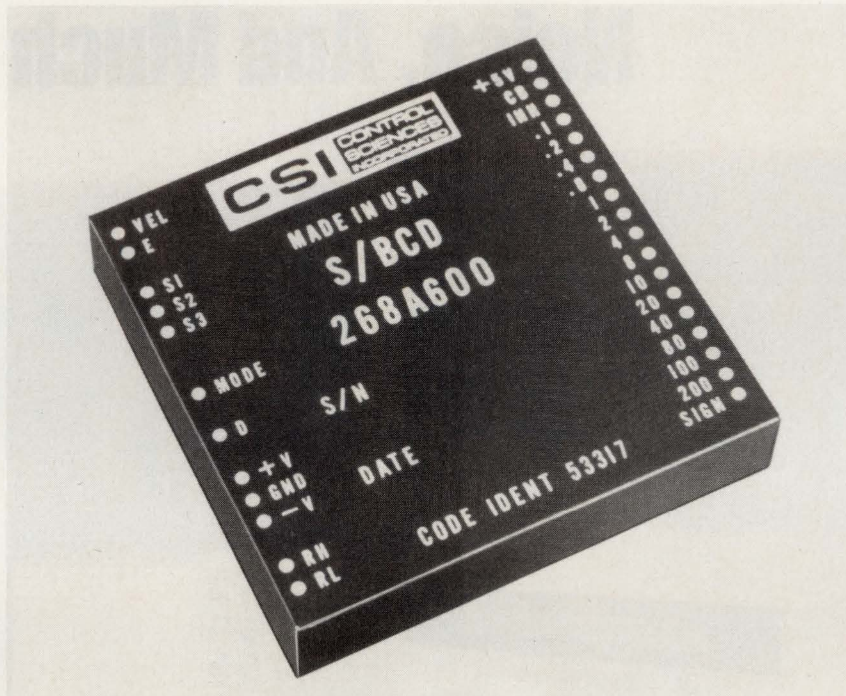
Synchro/Resolver To BCD Converter

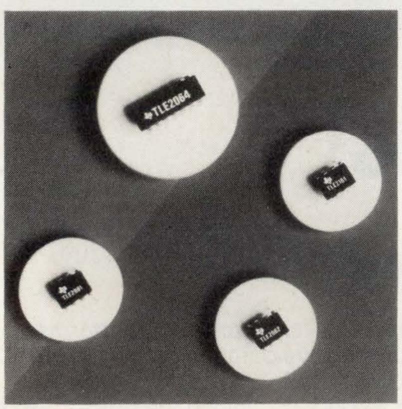
- *Accepts 3-wire synchro or 4-wire resolver inputs*
- *Package measures 2.0×2.0×0.4 in.*

The 268A600 series are small synchro/resolver-to-BCD converters. The device consumes <90 mW, using a ±5V supply. In addition to 3-wire synchro or 4-wire resolver inputs, the converter accepts 2 to $130V_{rms}$ line to line and 47- to 1200-Hz inputs. Outputs are 4-decade BCD angle plus sign, which you can pin-program for ranges of 0 to 359.9° or ±180°. The converter is available in either ±15V plus +5V or 5V-only versions. $375.

Control Sciences Inc, 9509 Vassar Ave, Chatsworth, CA 91311. Phone (818) 709-5510.

Circle No. 382





Precision Op Amps

- *Operate from supplies over the range of 3.5 to 22V*
- *Have an input offset voltage of 500 μV*

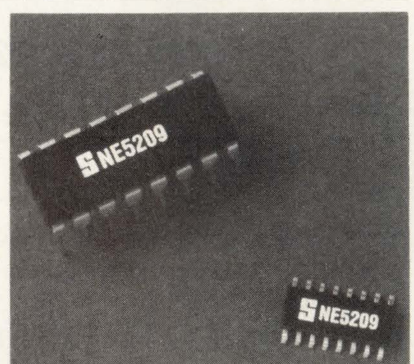
The TLE206x family of op amps and the TLE2161 decompensated op amp operate from dual supplies ranging from 7 to 44V. The 2061 single, 2062 dual, 2064 quad, and 2161 decompensated op amps can each drive 25 mA into a 100Ω load with 0.025% THD typ. The devices have slew rates of 3.4V/μsec typ and unity-gain bandwidths of 2.1 MHz typ. They are available in plastic and ceramic DIPs, small-outline ceramic LCCs, and metal cans. The op amps are also characterized for operation over commercial, industrial, and military temperature ranges. $0.92 to $2.05 (1000).

Texas Instruments Inc, Semiconductor Group, Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 700; in CA, (214) 996-6611, ext 700. **Circle No. 383**

Variable Gain Amplifier

- *Noise limited to 7 dB at maximum gain*
- *Internally compensated to allow for wideband operation*

The NE5209 amplifier offers gain out to 1.5 GHz. Using a control pin, you can adjust the gain of the amplifier over a 60-dB range. Noise increases 0.6 dB for each 1-dB gain drop. The device features a 1-kΩ high-impedance differential input and a 50Ω differential output and operates from one 5V dc supply. Available in DIPs or small-outline packages, the amplifiers operate

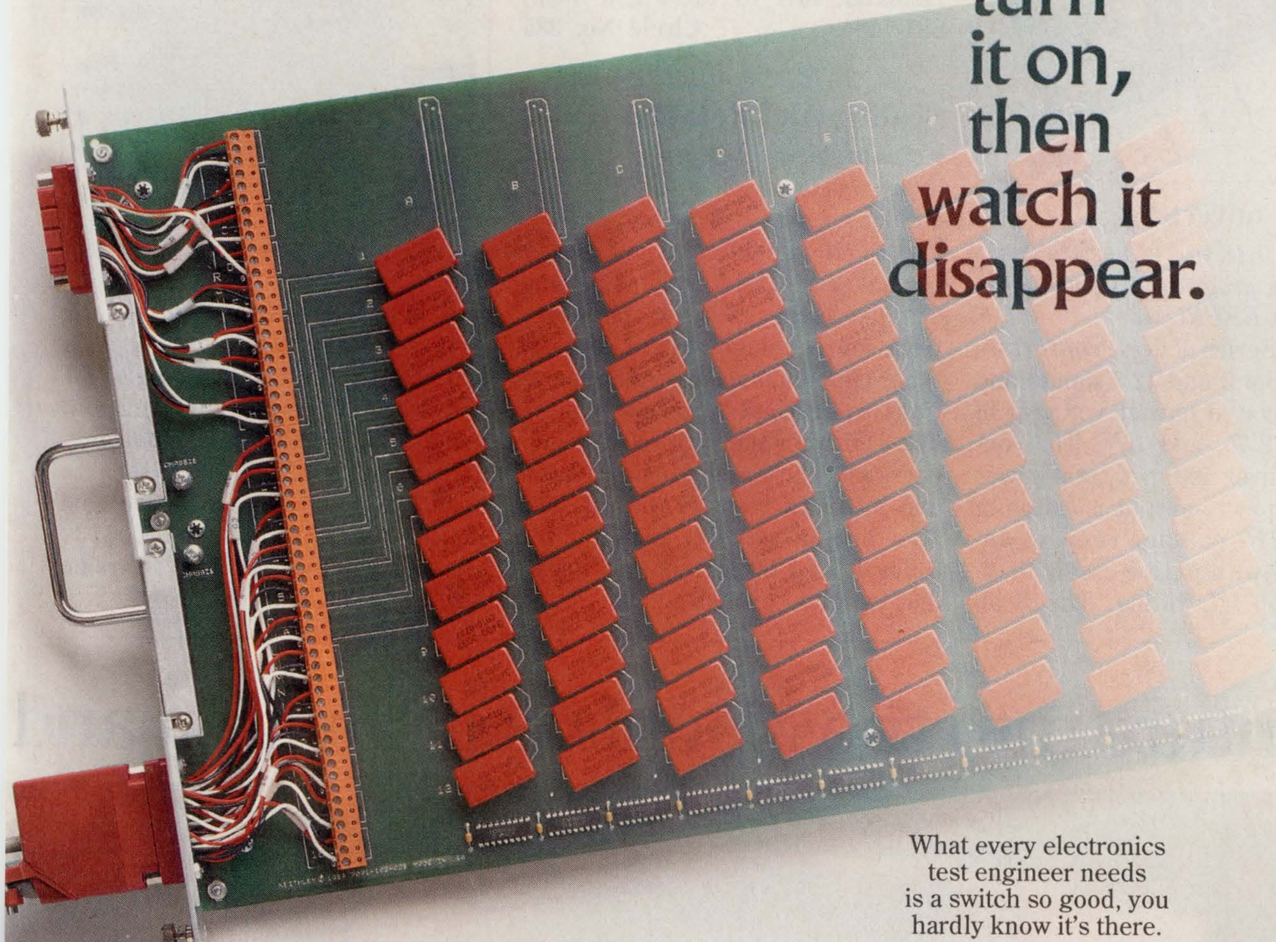


over commercial or industrial temperature ranges. Commercial version, $14.24 (100).

Philips Components/Signetics, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No. 384

Hook up a Keithley switch, turn it on, then watch it disappear.



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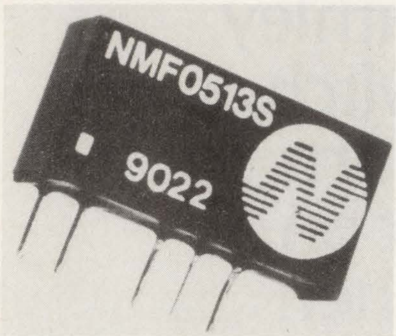
KEITHLEY INSTRUMENTS

CIRCLE NO. 113



DC/DC Converters

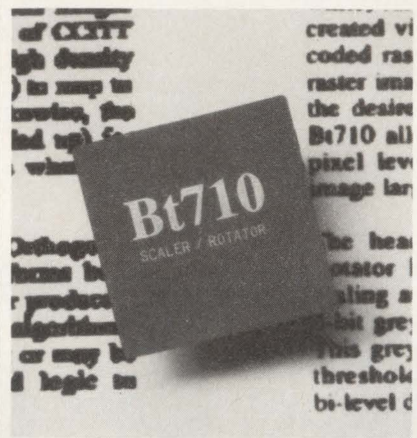
- *Require 0.18 in.² of board space*
- *Generate programming voltages for flash EEPROMs*

The NMF Series of dc/dc converters operate from 5 and 12V inputs and provide isolated output voltages of 5, 9, 12, 12.75, and 15V. The converters deliver 500 mW total power with an input-to-output isolation of 500V dc. The package is epoxy encapsulated with plastic casing, having a 94V-0 UL rating. The small converters operate over a 0 to 70° temperature range and don't require heat sinks. $12 (OEM qty).

International Power Sources Inc, 200 Butterfield Dr, Dept 8536, Ashland, MA 01721. Phone (508) 881-7434. **Circle No. 385**

Scaling And Rotation IC

- *Scales bilevel images to produce gray-scale result*
- *Scaling ranges from 6 to 750%*



The Bt710 image scaler and rotator IC has two DMA channels. One channel manages read operations from source image buffers, and the other channel manages write operations to destination image buffers. The DMA channels also provide address translation for image rotation and bit-block transfer (bitblt). The IC's output can be either 1 bit (bilevel) or 4 bit (gray). An on-chip look-up table provides image inversion, gamma correction, or mapping from 4-bit gray to 8-bit pixels. A software tool kit provides CCITT compression and decompression, image scaling, rotation, mirroring, and Boolean bitblt operations to destination buffers. Bt710 version in 132-pin pin-grid array, $132 (100); Bt710EVK IBM PC version under DOS and Windows 3.0,

$1990; Bt700SMA Macintosh version, $2490; Bt700SSA Sun workstation versions under Unix and X.11, $2990.

Brooktree Corp, 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. FAX (619) 452-1249. **Circle No. 386**

16-Bit Microcontroller

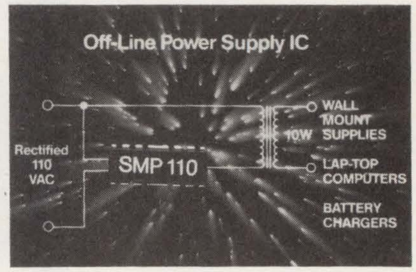
- *Source-code compatible with 68HC11*
- *Adds instructions to perform control-oriented DSP functions*

The 68HC16 adds three multiply instructions and two additional divide instructions to those of the 68HC11, its 8-bit sibling. In addition to these instructions, the HC16 offers new addressing modes and additional registers that allow the CPU to support high-level languages and perform some DSP functions. The microcontroller uses a modular design that surrounds the 16-bit CPU core with a queued serial module, a system integration module, a general-purpose 16-bit timer/counter, 1k byte of RAM, and a 10-bit, 8-channel ADC. The chip will be available in sample quantities in the second quarter of 1991. $25 (1000).

Motorola Inc, Microprocessor Products Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 891-2062. **Circle No. 387**

Power-Supply IC

- *Delivers as much as 10W from a rectified 120V ac input*
- *Contains both under- and overvoltage lockout circuits*

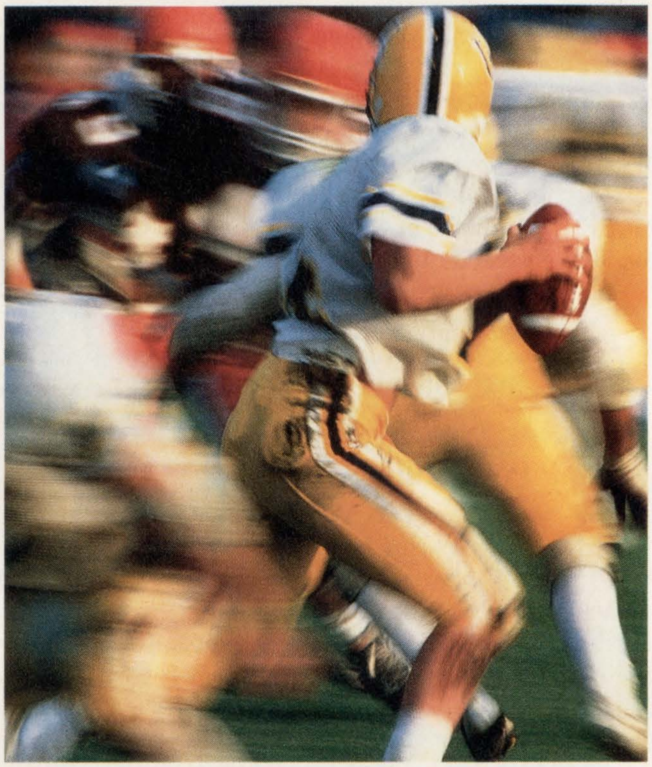


Accepting dc input voltages over the range of 36 to 200V, the SWP110 IC offers output voltage selection and supply isolation via an external output transformer. Without a heat sink, the chip can deliver 5W from a rectified 120V ac input; with a heat sink, it delivers 10W. An on-chip high-voltage PWM controller operates linearly from zero to the maximum pulse width. A preregulator circuit allows the chip to draw start-up power from the ac line. The chip has self-protection circuits for overvoltage, overcurrent, and thermal runaway. In a 16-pin plastic DIP, $2.36 (1000).

Power Integrations Inc, 411 Clyde Ave, Mountain View, CA 94043. Phone (415) 960-3572. FAX (415) 967-1608. **Circle No. 388**

CIRCLE NO. 182

TOKIN EMC SHUTOUT.



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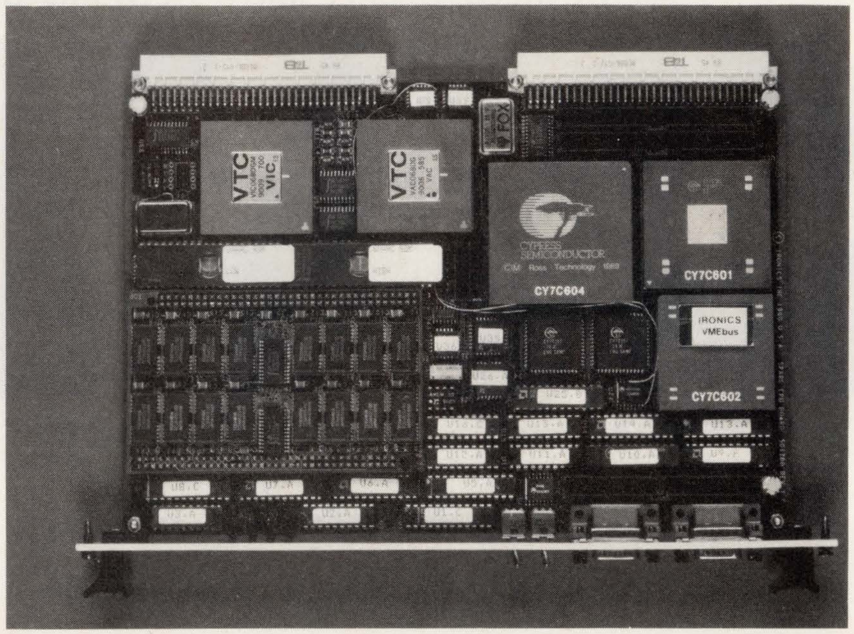
Tokin Europe GmbH
Knorrstr. 142, 8000 München 45, Germany
Phone: 089-311 10 66 Fax: 089-311 35 84

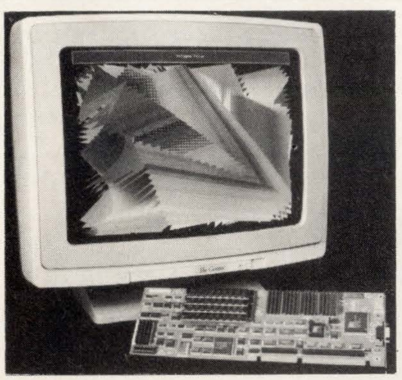
VMEbus Single-Board Computer

- *Uses 25-MHz SPARC chip and delivers 18 MIPS*
- *200M-byte/sec local bus gives CPU access to onboard RAM*

The IV-SPRC-25A single-board computer (SBC) for the VMEbus uses the Cypress Semiconductor 25-MHz SPARC chip set. Besides delivering 18 MIPS and 3.75M flops, the SBC can transfer data over the VMEbus at 30M bytes/sec. Its 200M-byte/sec local bus, the Mbus, gives the CPU access to the onboard RAM via a 64-bit data path. Other features are 64k bytes of cache RAM and either 4M or 16M bytes of dual-port dynamic RAM (DRAM), which has a 64-bit port to the Mbus and a 32-bit port to the VMEbus. A connector provides access to a variety of optional I/O daughter boards, which includes a VSB port, eight channels of serial I/O with DMA, and Ethernet or SCSI ports. The board runs on VxWorks, and compilers running on a Sun-4 workstation can directly download code to the board. Board with 4M bytes of DRAM, $6995; board with 16M bytes of DRAM, $9995.

Ironics Inc, 798 Cascadilla St, Ithaca, NY 14850. Phone (607) 277-4060. TLX 705742. **Circle No. 389**





Video-Controller Cards

- *Display 256 colors on monitors with 1280×1024 pixels*
- *Have 2M bytes of video RAM and 2M bytes of dynamic RAM*

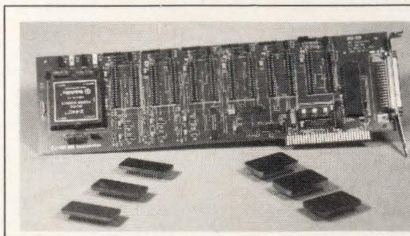
The Genius 1920C video controller drives multisynchronous monitors that have 1280×1024-pixel resolution and from 31- to 65-kHz horizontal scan frequencies. It contains TI's 34010 μP and comes standard with 2M bytes of video RAM and 2M bytes of dynamic RAM (DRAM); the latter is expandable to 16M bytes. Other features include a display of 256 colors from a palette of 16.7 million colors and a VGA pass-through mode. The board runs TI graphics-adapter applications and Microsoft's Windows 3.0. Drivers are available for AutoCAD, OrCAD, and Halo applications; the company is also developing drivers for Ventura, Wordperfect, and Pagemaker programs. The 1920G produces 256 shades of gray from a palette of 16.7 million. You can purchase the cards separately or with a choice of two monitors. 1920G, $2265; 1920C, $3195.

Micro Display Systems Inc, Box 455, Hastings, MN 55033. Phone (800) 437-7325; in MN, (612) 437-2233. FAX (612) 437-7325. TLX 4938623. **Circle No. 390**

Synchro/Resolver Board

- *Accommodates DDC's converters*
- *From one to six output channels*

The BBG-520 card for the 8-bit ISA bus converts digital signals to synchro/resolver outputs. It accommodates DDC's DSC-11520 or DRC-10520 and Natel's HDR2106 or HDR2116 converters. The cards have from one to six output channels that are jumper-programmable for resolver or synchro outputs when using the DSC-11520. Status



Analogic's DAS Family Outclasses the Competition

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MSDAS-12	12 Bits	200 kHz	$1495
LSDAS-12	12 Bits	100 kHz	$1195

**Single unit price. Quantity discounts available.*

For Applications Assistance, Call: David Wilson, Analogic Corporation, (800) 446-8936. For Sales Assistance, Call: Digital Distributors (800) 227-0349; In South Central USA: Norcom, Inc. (214) 386-4888; In Northeast USA: Trilogic (508) 658-3800

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- **High-speed DMA** for fast data acquisition
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CIRCLE NO. 116

registers provide built-in test functions from the converters. The unit's 12 bits of digital I/O allows it to drive external signals via software running on the host. From $1095.

BBG Inc, Box 954, Virginia Beach, VA 23451. Phone (804) 425-6615. **Circle No. 391**

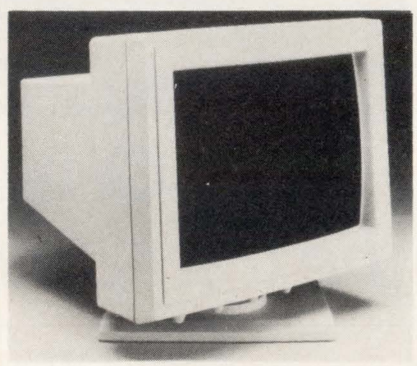
3½-In. Hard-Disk Drives

- *Available in 40M-, 80M-, and 105M-byte capacities*
- *Have <20-msec access times and are 1-in. high*

The SD-340/H, SD-380/H, and SD-3105 are 3½-in. hard-disk drives having 40M-, 80M-, and 105M-byte capacities, respectively. The drives' average access time is <20 msec, and they can transfer data at 1.5M bytes/sec. The drives use an index skew technique that offsets side 1 of a platter in respect to side 2. The index skew eliminates the delay when the drive head changes between platters, thus allowing faster track positioning. In addition, the rotational speed of the drives increases from 2400 rpm to 3600 rpm at 3600 rpm. The drives have either a SCSI-level 2 port or a standard IBM PC/AT interface. Shock-resistant mounting and an automatic head-locking feature protect against data loss when in transport. The MTBF is 30,000 hours. The drives can withstand nonoperational impacts as high as 70g. SD-340/H, $220; SD-380/H, $340; SD-3105, $400.

TEAC America Inc, 7733 Telegraph Rd, Montebello, CA 90640. Phone (213) 726-0303. FAX (213) 727-7621. TLX 677014.

Circle No. 392



Multiscan Color Monitor

- *Features 30- to 50-kHz horizontal scan rate*
- *Has 0.2-mm dot pitch and 1024 × 768 pixels*

The Model TE1791 17-in. multiscan color monitor features a flat nonglare screen that has sharp corner focusing. The analog monitor can track horizontal scan rates from 30 to 50 kHz and vertical scan rates from 45 to 100 Hz. The design utilizes Motorola's MC1381 multimode

C&C Computers and Communications

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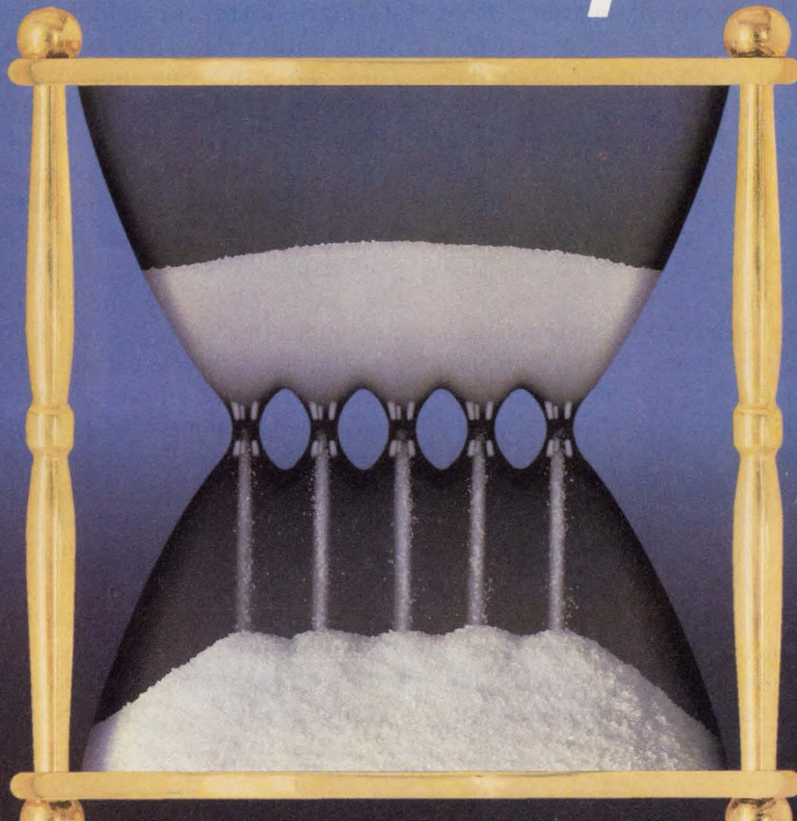

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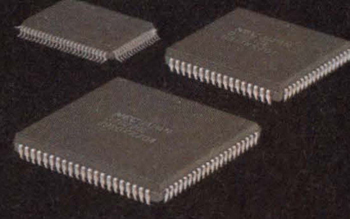
K Series

Embedded Control



NEC

CIRCLE NO. 117

monitor processor and a proprietary ASIC that reduces parts count and has a low power dissipation. Other features are a 119-in.^{2} of viewable area and a 0.26-mm dot pitch. The monitor meets the standards for VGA and Super VGA resolution and refreshes the noninterlaced 1024×768-pixel screen at a 60- to 70-Hz refresh rate. The monitor has a standard tilt/swivel base. $560 (OEM qty).

Teco Information Systems, 24 E Harbor Dr, Lake Zurich, IL 60047. Phone (708) 438-3998. FAX (708) 438-8061. **Circle No. 393**

Color Printer

- *Has 300-dpi resolution and prints Postscript files*
- *Uses an 80960 μP*

The Colorpoint PS desktop printer produces Postscript files. The printer uses an Intel 80960 μP for printing large image sizes. Two printer models make images on standard letter or tabloid-sized pages with a resolution of 300 dpi. They can also print supersize images with trimmed edges where the image runs off all four sides of a page. The letter-size printer produces a supersize image that is 8.53×13.0 in. The tabloid-size printer produces a super-size image that is 11.73×17.12 in. The five communication ports consist of Appletalk, Centronics parallel, RS-232C; and two SCSI ports. You can share the printer with several different computers. The printer's intelligent interface scans each port and begins printing the first available data. Letter-size, $6999; tabloid-size, $9999.

Seiko Instruments USA Inc, 1130 Ringwood Ct, San Jose, CA 95131. Phone (408) 922-5800. FAX (408) 922-5840. **Circle No. 394**

80386 Mother Board

- *Has a floppy and IDE hard-disk controller*
- *Has as much as 16M bytes of RAM*

The K386A-25/33, a baby-sized IBM PC/AT mother board, contains either a 25- or 33-MHz 80386 μP and a socket for either an 80387 or Weitek coprocessor. Its features include a floppy-disk controller, an IDE hard-disk controller, a parallel port, and two serial ports. You can populate the board's cache memory area with 32k bytes or a 128k bytes of static RAM with 25-nsec access time. The mother board has as much as 16M bytes of main memory with 80-nsec access times. It comes with the Phoenix BIOS; the AMI BIOS is optional. One 8-bit and five 16-bit expansion slots can operate at software-selectable speeds of 8 or 12 MHz. The board contains a real-time clock with battery, and it can run with OS/2, PC/DOS, MS/DOS, Unix, Xenix, Windows/386, Concurrent DOS, and Novell operating systems. $1100 (2 to 9).

Klever Computers Inc, 1028 W Maude Ave, Sunnyvale, CA 94086. Phone (408) 735-7723. FAX (408) 735-7724. **Circle No. 395**

VMEbus Chassis LAN

- *Connects as many as 16 chassis within 75 ft*
- *Data-transfer rate between chassis is 30M bytes/sec*

The PT-VME940 interconnects VMEbus chassis that are as far as 75 ft apart. The product can transfer data between chassis at a rate as fast as 30M bytes/sec. The interconnection scheme lets you integrate as many as 16 chassis in a parallel network. The configuration has from 2 to 16 VMEbus modules, each residing in a separate chassis. A module contains a 68020 μP to supervise data transfers and to execute network firmware. A high-speed FIFO buffer lets you transfer data over the VMEbus backplane at 60M bytes/sec, using the company's VME64 specification. The module comes with firmware that permits inter-chassis communications using peer-to-peer or master-slave modes. $2280/node (100).

Performance Technologies Inc, 435 W Commercial St, East Rochester, NY 14445. Phone (716) 586-6727. FAX (716) 586-6707. **Circle No. 396**

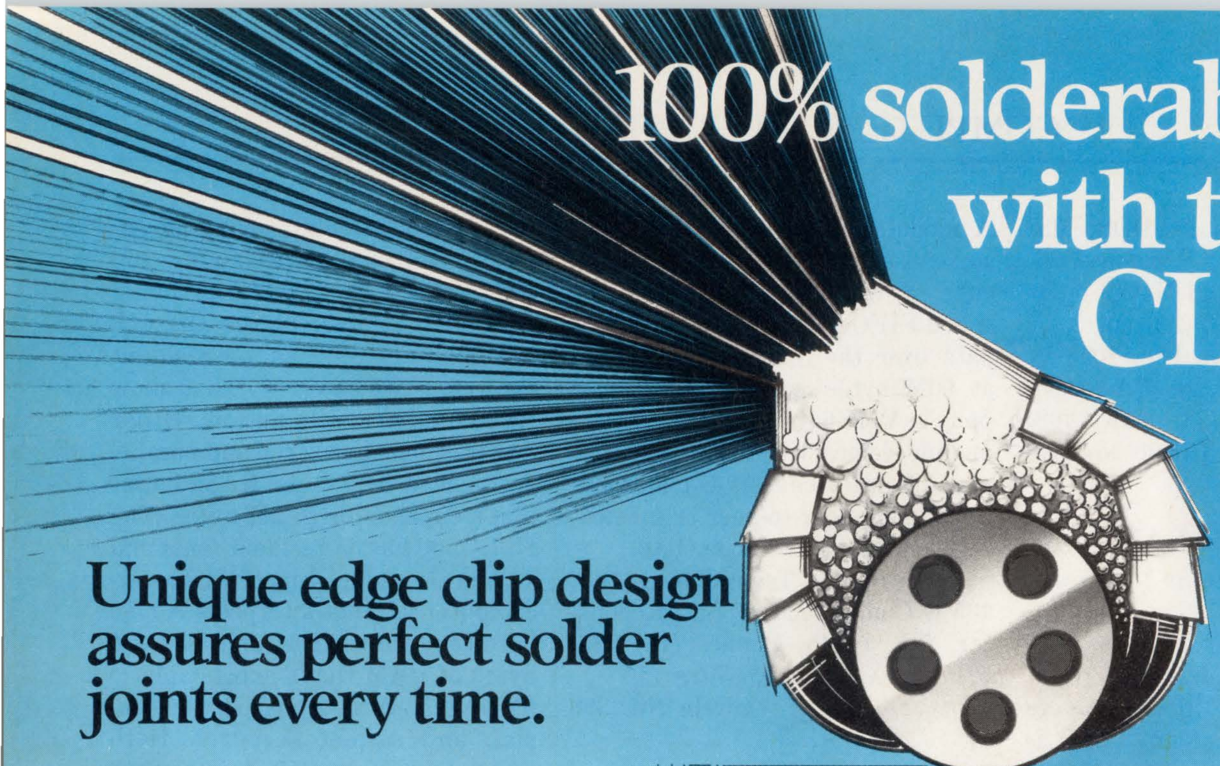
Laser Printers

- *Print at 6 pages/minute and have two card slots for fonts*
- *Have 1250-sheet paper tray and optional second tray*

The EPL-7000 personal laser printer and the EPL-7500 Postscript laser printer provide an engine speed of 6 pages/minute and two card slots for additional fonts. The EPL-7000 emulates the HP Laserjet IIP; it has 14 resident fonts and two card slots that allow HP-GL plotter emulation. Other features include a serial and parallel port and a 512k-byte RAM buffer that's expandable to 2M bytes. The EPL-7500 has 35 resident fonts and a Weitek reduced-instruction-set-computer μP that interprets Adobe Postscript files. The unit has 2M bytes of RAM that's expandable to 6M bytes. It also has parallel, serial, and Appletalk ports. Both printers have a 250-sheet paper tray. An additional 250-sheet paper tray is optional. EPL-7000, $1400; EPL-7500, $3500.

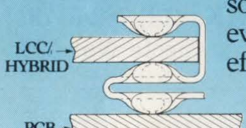
Epson America Inc, 2780 Lomita Blvd, Torrance, CA 90505. Phone (213) 782-5161. FAX (213) 782-5179. **Circle No. 397**

100% solderability with the CLAW

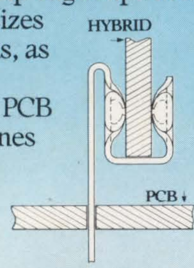


Unique edge clip design assures perfect solder joints every time.

NAS solder and flux bearing edge clips have proven to be the most effective way to overcome thermal mismatch between PCBs and high-density hybrids and chip carriers. Now, NAS has developed a unique "claw" grip design that assures 100% solderability and provides even greater assembly efficiency and economy.



"Claw" grip edge clips in a variety of sizes and designs, as well as different solder types, are offered for use with ceramics and PCB materials. Clips with .100 centerlines for both through-the-board and surface mounting of hybrids, and low profile clips with .050 centerlines for surface mounting LCCs are available. Both can be provided with an optional third solder preform for mounting clips to the devices and to the surface of the PCB with one reflow.



Fewer assembly steps. Dramatic reduction in rework. Lower overall costs. Increased product reliability. These are a few of the advantages of the new NAS "claw" grip solder and flux bearing edge clips—*the only interconnects that assure 100% solderability.*

For complete details and our new catalog, call or write NAS Electronics, 381 Park Street, Hackensack, NJ 07602. Tel. 201/343-3156. TWX: 710-582-3048. FAX: 201/343-4883.

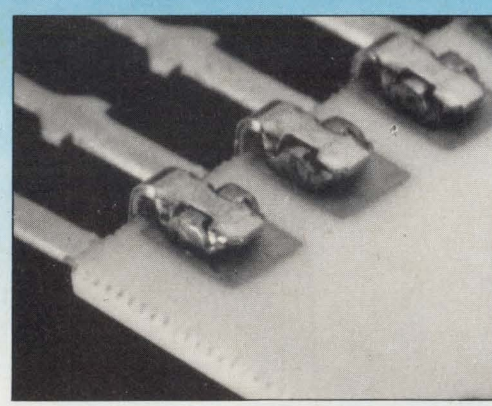
™ an Interplex Industries company

NAS ELECTRONICS

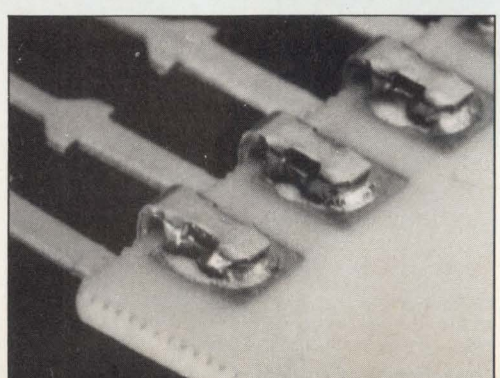
U.S. Patent 4,605,278. Other patents pending.

Direct contact between solder preforms and conductor pads produces wiping action as clips are attached.

Interference fit holds clips firmly in position for reflow. Top and bottom preforms are reflowed in one operation.

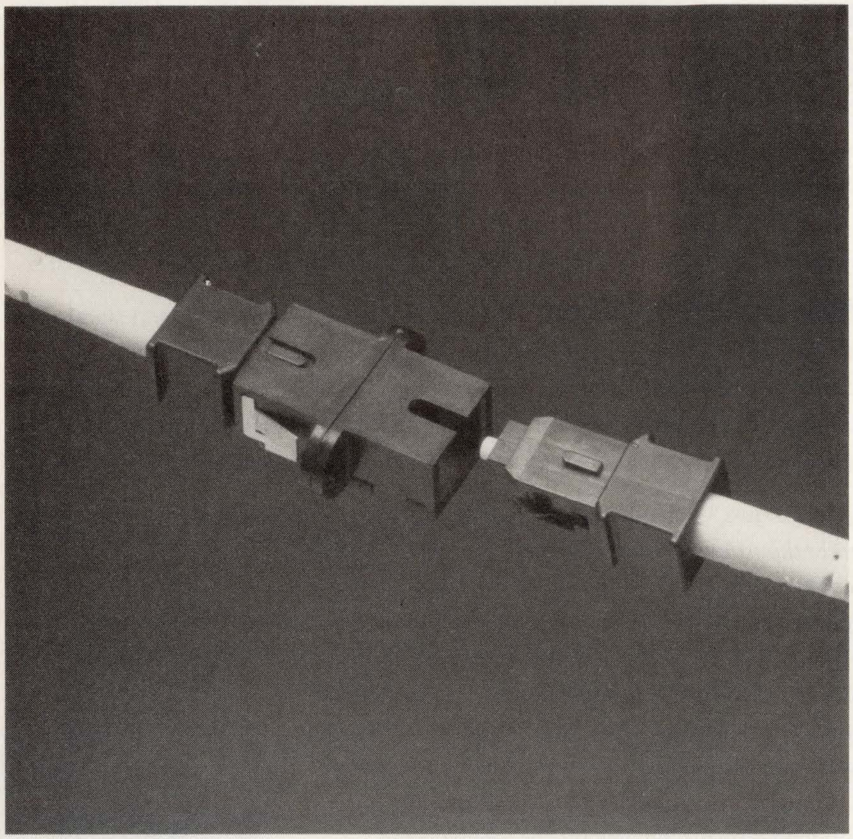


Precise amount of solder and the shape of the "claw" grip control solder flow without a solder stop. This assures perfect mechanical and electrical bonding without wicking or bridging.



Unretouched Macro Photography.

CIRCLE NO. 118



Fiber-Optic Connectors

- *Have 0.5-dB insertion loss*
- *Accommodate single- or multimode fibers*

You can terminate these SC fiber-optic connectors either in the factory or in the field. They feature a maximum insertion loss of 0.5 dB. The system includes connectors, coupling bushings, 100% pretested cable assemblies, pigtails, and wall-outlet plates. The units feature a pre-radiused ferrule, which allows you to polish the fiber end without using expensive equipment. The connectors accommodate either single mode or multimode fibers and are available in single- or dual-position versions. The units conform to the NTT SC design. Coupling receptacles are available to mate SC to SC, SC to ST, and SC to FC connectors. Single-mode version, $13.49/kit (500).

AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752.

Circle No. 374

Hybrid Voltmeters

- *Have $10^9\Omega$ input impedance*
- *Operate from a single supply*

DMH-30 Series 3½-digit hybrid voltmeters are available in commercial (PC) grade and extended temperature (MM) versions. Both designs feature full differential inputs with bipolar full-scale ranges of ±200 mV, ±2V, and ±20V dc. The high $10^9\Omega$ input impedance minimizes circuit loading. The meters operate from a 5V supply. Other features include user-selectable decimal-point placement, full autozero, auto-polarity changeover, underrange and overrange indication, a standby mode, test pin (all digits), external reference input for ratiometric measurements, 5V dc output pin for powering external circuitry, and a 1.23V reference output pin. Accuracy is 0.05%, and CMRR over dc to 60 Hz measures 86 dB. The operating range is 0 to 60°C and −40 to +75°C for PC and MM units, respectively. DMH-PC, $84; DMH-MM, $132.

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356. TLX 174388. **Circle No. 375**

DC/DC Converters

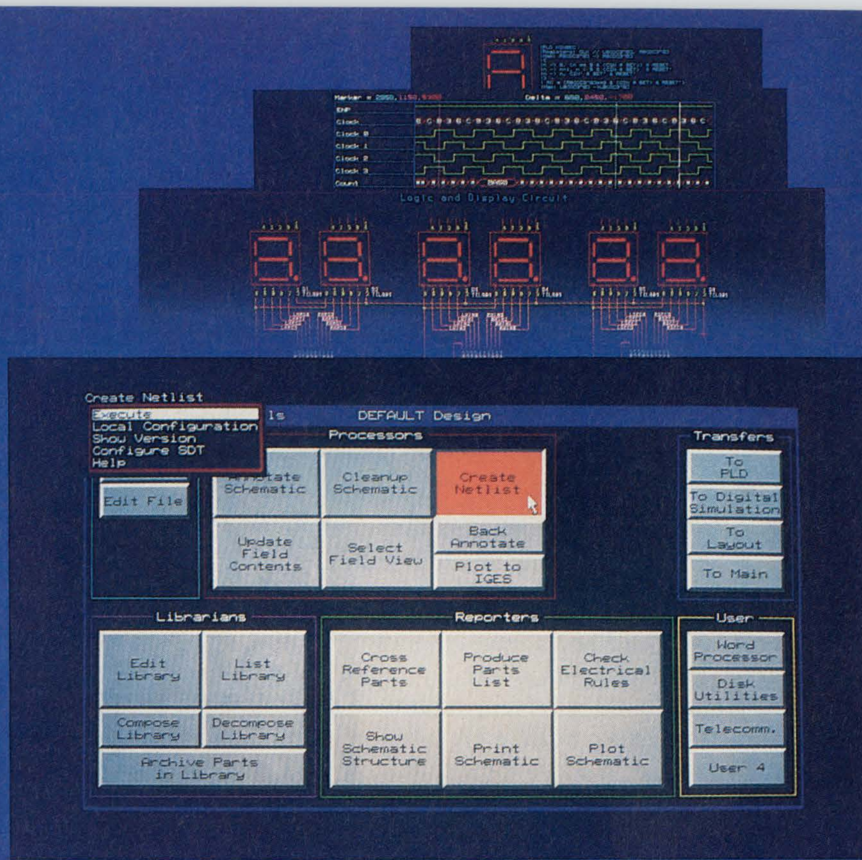
- *Deliver 25W*
- *Have an 82% efficiency*

Housed in a 3×3×0.4-in. package, NFC25 Series dc/dc converters provide 5 and ±12V outputs and deliver 25W—7W/in^3. The units have an 82% efficiency. A simple TTL signal can shut the outputs. An internal pi filter, combined with an external capacitor, attenuates input line noise below VDE0871 Limit B levels. Internal short-circuit protection guards against damage from load shorts, and overvoltage protection prevents damage from converter failure. The units operate at full power over a −25 to +70°C range. $77 (50).

Computer Products Inc, 3785 Spinnaker Ct, Fremont, CA 94538. Phone (415) 657-6700. FAX (415) 683-6452. **Circle No. 376**

OrCAD presents

Release IV



The limits are gone

OrCAD has introduced the greatest product upgrade in its history. Memory limits, design restrictions, even boundaries between products are all disappearing.

For years, OrCAD's competitors have been playing a game of catch-up. With the introduction of Release IV, the race is over. No one will match our price/performance ratio on these features:

- Schematic Parts Library has been increased to over 20,000 unique library parts
- Digital Simulation process has been speeded up by an order of magnitude
- Printed Circuit Board Layout package offers autoplacement and autorouting at no extra charge
- Expanded memory capabilities

Best of all, OrCAD introduces ESP

ESP is a graphical environment designed specifically for the electronic designer. Software tools appropriate for different stages in the design process are now linked together to form a seamless flow of information. This easy-to-use framework relieves the designer of time consuming tasks and the inconvenience of moving from one tool set to another. You can now spend more time productively designing.

For more information . . .

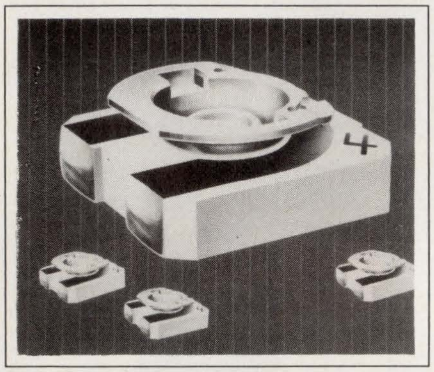
You need to know more about Release IV and all of the benefits OrCAD has to offer. Call the telephone number below and we'll send you a free demonstration disk.

OrCAD®

More designs from more designers

For more information, call (503) 690-9881

or write to OrCAD Sales Department, 3175 N.W. Aloclek Drive, Hillsboro, Oregon, 97124



Surface-Mount Trimmer

- *Saves pc-board space*
- *Resistance ranges to 1 MΩ*

The Model 3363 surface-mount trimmer satisfies both EIA and EIAJ standard board footprint and packaging requirements. Measuring only 3-mm square, the device saves valuable pc-board space and is compatible with pick and place equipment. Standard resistance values range from 100Ω to 1 MΩ, and maximum contact-resistance variation measures 5%. The trimmer has a special coating over the resistor element to protect it from harsh fluxes, soldering, and cleaning environments. The coating is permanent and requires no expensive secondary removal operations. The trimmer is packaged in an 8-mm embossed tape. From $0.395.

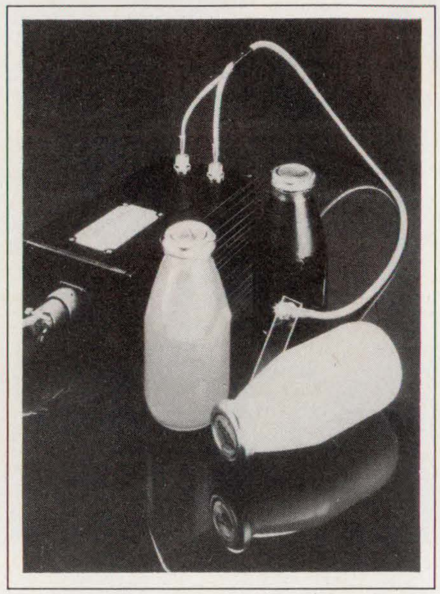
Bourns Inc, 1200 Columbia Ave, Riverside, CA 92507. Phone (714) 781-5500. TLX 676423.

Circle No. 377

Color-Recognition Sensor

- *Can memorize eight colors*
- *Has 2-in. sensing distance*

Capable of memorizing as many as eight colors, the CRS 300/301 sensor uses the total 400- to 800-nm visible light spectrum to characterize colors, not just color marks. You can place the fiber-optic sensing tip 0.1 to 2 in. from the target. In addition to the eight outputs for color definition, the unit has an output for self-diagnostics. The sensor output is either a sinking or sourcing signal (10.5 to 30V dc). You can configure the output simply by using onboard switches or menu-driven software. The unit features an RS-232C or RS-422 connection. A 10.5 to 30V, 47W power supply provides sensor operating power. Reverse-polarity protection is standard. Operating range spans 0 to 40°C. The rugged aluminum enclosure provides NEMA 1, 3, 4, 12, 13, IP65, and IP67 protection. $8000.



Micro Switch, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-6600.

Circle No. 378

Switching Power Supplies

- *Feature user-adjustable wide-range outputs*
- *Deliver 400W of power*

Series 2 400W switch-mode power supplies are available in single- and multiple-output versions. Single-output units deliver 5V at 50A. Multiple-output models have three or four outputs and provide a 5V/50A main output and 12V/15A, 12V/6A, 5V/6A or 24V/3.5A auxiliary outputs. User-adjustable output models are also available. These

Text continued on pg 214

A Look at Today... A Vision of Tomorrow

68040 VME
33 MHz 0-Wait-State

Your Vision of High Performance at an Affordable Price is Now Real!

With the OB68K/VME40™ you no longer have to compromise on performance or price in your VME embedded control application. We start by giving you a very basic board which includes:

- 25-33MHz 68040.
- (8) 28-pin RAM sockets for up to 256KB of dual access 0-wait-state static RAM (32KB standard).
- (8) 32-pin sockets for up to 8MB of ROM.
- (2) asynch RS232C serial ports.
- (16) lines of parallel I/O.

You can configure it with just the right amount of RAM and ROM you need. And you do not have to sacrifice features. Our Omnimodule™ modular I/O connector allows you to implement a wide variety of serial, parallel, SCSI, GPIB, analog, digital and other I/O options - all fitting into one slot. Other features include:

- VTC's VIC068 VME interface chip with arbiter, interrupter, mailbox and more.
- Terminal monitor/ debugger/diagnostic firmware program included.
- 2 year limited warranty.
- Worldwide availability.

All of this gives you a high performance board at a price you can afford with the features you need.

To learn more about our OB68K/VME40 contact our Marketing Manager, Pete Czuchra at 1-800-638-5022 or (708) 231-6880 in Illinois.

Omnimodules™

OMNIBYTE™

OMNIBYTE CORPORATION
245 W. Roosevelt Road
West Chicago, IL 60185-3790
Fax No. 708-231-7042
CALL TOLL FREE 1-800-638-5022
In IL 708-231-6880

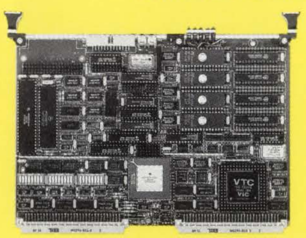
CIRCLE NO. 120

Our VME and Multibus Product Lines Stretch for Over 124 Miles

That's 854,738 uniquely configured boards to choose from and all from Omnibyte. You can choose from different processor types, RAM sizes, I/O options and other features to put together a board that gives you the features you need. With Omnibyte's quality, selection and 2 year limited warranty, you can count on finding exactly what your looking for.

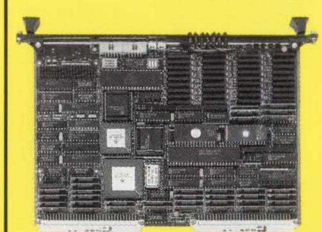
Here are just a few of the boards we offer:

OB68K/VME20™ VME SINGLE BOARD COMPUTER



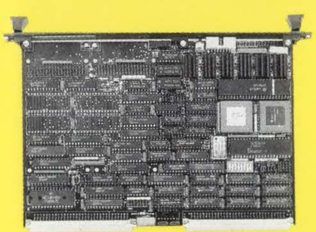
- 68020 16.66 - 33 MHz CPU
- (8) 28-pin RAM sockets for up to 265KB of dual-access zero-wait-state-static RAM
- (8) 32-pin sockets for up to 8MB of ROM, (4) sockets may be EEPROM
- (2) RS232C asynch serial ports
- (16) lines of parallel I/O
- (1) (OMNIMODULE socket for a wide variety of I/O (i.e. 2 serial ports, 20 parallel lines)
- VIC068 VME Interface Controller

OB68K/VSBC20™ VME SINGLE BOARD COMPUTER



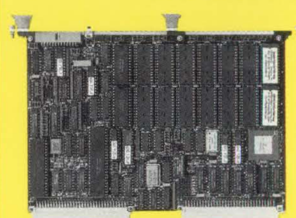
- 68020 16-33MHz, CPU
- 1-4 MB of dual-access, zero-wait-state DRAM with parity
- 68882 (optional)
- (2) 32-pin ROM sockets
- (2) RS232C serial ports
- (2) 8-bit parallel ports
- (1) OMNIMODULE socket for a wide variety of I/O (i.e. 2 serial ports, 20 parallel lines)
- 4 level bus arbiter (optional)

OB68K/VSBCI™ VME SINGLE BOARD COMPUTER



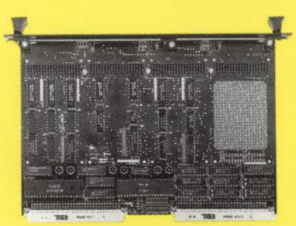
- 68000 12.5MHz 16/32 bit CPU
- 512KB of dual-access, zero-wait-state DRAM with parity
- (4) 28-pin ROM sockets
- (3) 16-bit counter/timers
- (2) Omnimodule™ I/O sockets for a wide variety of I/O (i.e. 4 serial ports, 40 parallel lines)
- DMA controller (optional)
- VME bus interrupt generator (optional)
- Optional 4 level bus arbiter
- Two year limited warranty

OB68K/VME1™ VME SINGLE BOARD COMPUTER



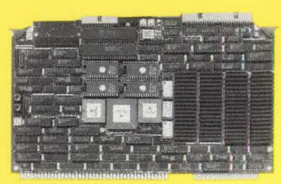
- 12.5 MHz 68000 CPU
- (8) pairs of 28-pin sockets for RAM or ROM
- (2) RS-232C serial ports
- (2) 8-bit parallel I/O ports
- System Controller

OB68K/VIO™ VME UNIVERSAL I/O BOARD



- (4) Omnimodule I/O sockets for a wide variety of I/O (i.e.8 serial ports, 80 parallel lines)
- One (1) interrupt per Omnimodule, two (2) optional

OB68K/MSBC30™ MULTIBUS I SINGLE BOARD COMPUTER



- 25-33 MHz 68030 CPU
- 4-32 MB dual access, zero-wait-state DRAM w/parity
- 68882 Math Co-Processor (optional)
- 2 channel DMA controller (optional)
- (2) RS232c sync/async serial ports
- (2) 8-bit parallel ports
- (1) OMNIMODULE™ socket
- (4) 32-pin ROM sockets

All our different configurations are built to give you the best in quality. And they are backed by our famous 2 year limited warranty. For more information call Pete Czuchra today. He'll help you pick the card you need.

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CIRCLE NO. 119

It takes experience to handle both limpness *and* flexibility.

Small, lightweight, flexible--these are the requirements we meet often. But *"limp as a noodle?"* An appetizing challenge.

Texas Instruments came to us for a complete interconnect system for a gyroscope controlled guidance system. Application-engineered to extremely demanding weight and space requirements, this dynamic system also must endure constant flexing.

At Precision Interconnect, we're working every day to meet requirements like these. We manufacture microminiature cables with conductors as small as 42 AWG and terminate them to our standard line of Micro-D and linear strip connectors with .050"(1.27mm) centerline spacing. Custom and nano strip connectors with .025"(.64mm) spacing can also be assembled.

Our expertise, increasing with each unique problem we solve, ensures that all critical components of your interconnect system are designed in, built in, and tested. We begin by discussing your specific interconnect system problems.

Maybe over lunch?

This ultra flexible harness for Texas Instruments terminates Nano Strip and Micro-D connectors to 43 conductors, 32 to 40 AWG.

PRECISION INTERCONNECT

16640 S.W. 72nd Avenue
Portland, OR 97224
(503)620-9400

Offices in San Francisco, Dallas, Wilmington, Düsseldorf and Tokyo.

CIRCLE NO. 166

units have a 5V/50A main output and auxiliary outputs of 12 to 15V at 15A, 5 to 15V at 6A, 2 to 6V at 6A, and 12 to 24V at 3.5A. Standard features include an internal dc fan, a 120/240V ac strappable input, an internal EMI filter, an input power-fail signal, a remote sense on outputs of 10A or more, overvoltage protection on all outputs, overtemperature shutdown, and soft start. All units comply with UL, FCC, CSA, and TUV safety and EMI specifications. From $362 to $491.

Qualidyne Systems Inc, 3055 Del Sol Blvd, San Diego, CA 92154. Phone (619) 575-1100. FAX (619) 429-1011. **Circle No. 379**

Board-Mount Transformers

- *Have a dual-bobbin construction*
- *Satisfy UL requirements*

Class 2 Series transformers are available in 12 pc-board and 5 chassis-mount versions. They feature dual-bobbin construction and a tailored insulating shroud. The transformers satisfy UL 1585 Class 2 requirements and comply with CSA safety and performance standards. The transformers are intended for 2.5 to 80V applications and feature 4000V rms primary and secondary isolation. The units are available in inherently limited or noninherently limited designs. The dual-bobbin design reduces capacitance and eliminates the need for an electrostatic shield. $6.75 to $18.94 (10).

Signal Transformer, 500 Bayview Ave, Inwood, NY 11696. Phone (516) 239-5777. FAX (516) 239-7208. **Circle No. 380**

PC-Board Connectors

- *Feature standoffs to facilitate cleaning operations*
- *Have gold plating*

Series 2400 pin strips feature a smooth bullet nose to minimize damage to sockets during insertion. Solder standoffs keep the connectors above the board to facilitate cleaning operations. The connectors are available in two lengths in single 40-contact-max or double 80-contact-max rows in straight or right-angle versions. You can break the units to match specific application needs. The units are side-by-side and end-to-end stackable and feature a choice of either 10- or 30-μin. gold plating. An optional retention feature holds the connectors in place in demanding applications. The pin strips are also available in plastic-tube packaging to accommodate robotic assembly systems. $0.03/pin (1000).

3M, Electronic Products Div, Box 2963, Austin, TX 78769. Phone (800) 225-5373; in TX, (512) 984-3897. **Circle No. 381**

CIRCLE NO. 167

For the first time! DC-DC converters that really check out.

MIL-STD-883 COMPLIANT

Insist on Interpoint.

It's official! The first high-density, low-profile, thick-film hybrid DC-DC converters that let you check off all the MIL-STD-883C, Method 5008, Class B requirements.

Work on your design, not the exceptions list. If you've ever had to justify a non-compliant part for a MIL-STD-883 design, you know about red tape. Now you can forget it. Interpoint's new MHF/883 DC-DC converters are fully compliant to MIL-STD-883C. No exceptions. No waivers. No apologies.

Premium performance. MHF/883 converters offer up to 12-watts output power, 84% efficiency, a 16 to 40 Vdc input range, single and dual outputs, constant frequency switching, and 10 mV typical output regulation. And they're small enough (1.5 x 1.1 x 0.36 inches) to leave plenty of room for the rest of your design.

More to come. The MHF/883 converters are the first in a series of compliant power products from Interpoint—the worldwide leader in high-reliability DC-DC converters and EMI filters.

Order our Prototyping Kit and see for yourself. You'll get a low-cost converter electrically equivalent to the compliant MHF/883—it's perfect for prototypes or design evaluation. Plus: our FREE Guide to Designing Distributed Power Systems, complete performance specifications and an MTBF Analysis Booklet. Call now: **1-800-822-8782, ext. 229.** In Europe: **44-276-26832.**

interpoint

MIL-STD-1772 QUALIFIED

10301 Willows Road P.O. Box 97005
Redmond, WA 98073-9705

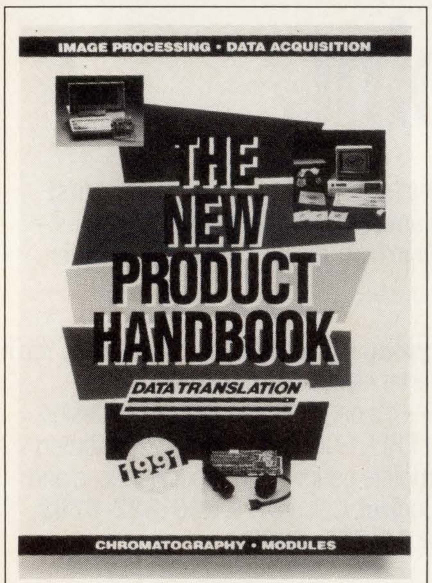
CIRCLE NO. 168

Data Book Deals With GaAs Integrated Circuits

The 1991 GaAs IC Data Book and Designer's Guide describes GaAs ICs, including the Picologic, NanoRAM, and NanoROM families; fiber-optic communications products; and SC10000 standard cell arrays. Also included is information about prototyping products, reliability, testing, and packaging. The publication describes seven new IC products. Also mentioned are chip sets for direct digital synthesis, PLL frequency synthesis, an 800-MHz pin driver for ATE (automatic test equipment) pin electronics applications, and a general-purpose line of high-speed digital logic functions. The designer's guide offers 14 application notes, including the use of the vendor's high-speed ICs, and information about thermal management and PN code generation.

Gigabit Logic, 1908 Oak Terrace Lane, Newbury Park, CA 91320.

Circle No. 366



Data Acquisition and Image Processing

Two handbooks provide comprehensive coverage of the vendor's products. *The New Product Handbook* describes data-acquisition, image-processing, and chromatography products for IBM PC and compatible computers, IBM PS/2, Macintosh II, and other microcomputers. This 275-pg catalog presents more than 300 products with data sheets, summary tables, tutorials, prices, and ordering information. The publication includes applications for hardware, software, and accessories for specific tasks. Color-coded tabs provide a quick reference to the products you're looking for. *The Source Handbook* lists the compatible software packages for each product in the product handbook. It also serves as a directory of worldwide hardware and services that are compatible with the vendor's products.

Data Translation, 100 Locke Dr, Marlboro, MA 01752.

Circle No. 367

How To Expand Generator Capability

The application guide, *More Function Generator Capability with Arbitrary Waveforms,* explains how to recreate waveforms captured with a digital storage oscilloscope on the PM5138 arbitrary waveform/function generator without any programming. Sample applications also show how to use the PM 3375. Other applications include bar-code reader testing, power-step-supply response, and testing a touch-tone DTMF signal.

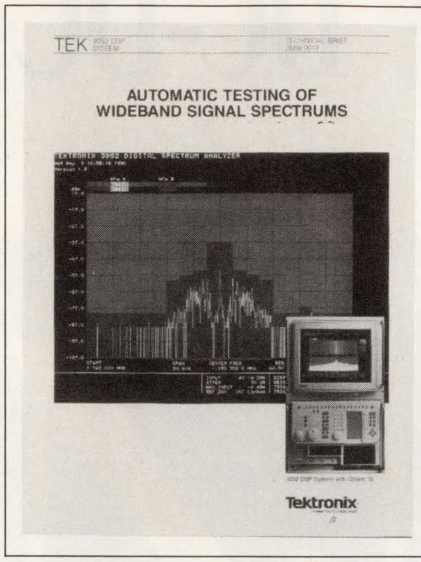
John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206.

Circle No. 368

Brochure Features DSP Solutions

This brochure covers the vendor's digital signal-processing products. The publication presents software for the product line, DSP processors for IBM PC and VME computers, and the vendor's analog I/O boards and systems.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. **Circle No. 369**



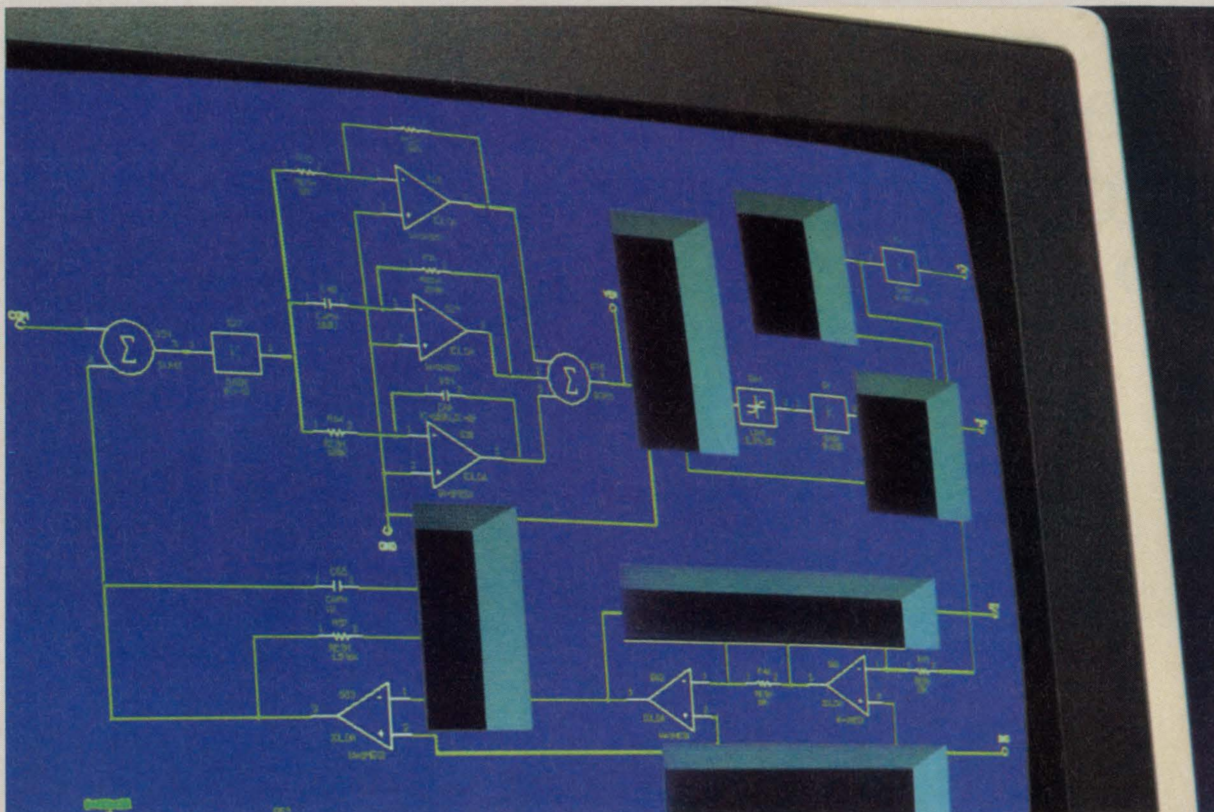
Article Discusses Testing Signal Spectrums

The technical note, *Automatic Testing of Wideband Signal Spectrums,* talks about the use of the vendor's 3052 DSP systems to test and compare with user-supplied limits as high as 5000 signal spectrums/sec. The publication gives an example of a program for setting spectral limits. The 6-pg note also mentions high-speed spectral testing and its value for applications where much testing is done in a short time.

Tektronix Federal Systems Inc, Box 4490, MS 38-386, Beaverton, OR 97076. **Circle No. 370**

IEEE-488 Hardware And Software Products

This 100-pg catalog lists IEEE-488 hardware and software products for test and measurement, research and development, quality assurance, and production applications. The publication features at least 70 products for IEEE test applications including several new products, such as the Power488 IEEE-488.2 controller and the Extender488/HS bus extender. The six product sections cover IBM PC/AT/386 and Micro Channel IEEE products; Macintosh IEEE products; Sun, DEC, and Next Workstation IEEE products; Serial/IEEE converters and



When it comes to analog design, Intergraph gives you the missing pieces.

Look closely at most analog design systems and you'll find something missing. Tools that don't exist.

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controllers; analog and digital I/O converters to IEEE; and IEEE Bus analyzers, extenders, buffers, converters, and expanders. Block diagrams, specifications, programming examples, and pricing round out the publication. Recent additions to the IEEE-488 Technical Review include tutorials for the IEEE-488.2/SCPI and the SCSI.

IOtech, 25971 Cannon Rd, Cleveland, OH 44146. **Circle No. 371**

Note Explains Waveform Simulation

Simulating Disk Drive Waveforms with LeCroy's Easywave Software and 9100 Series Arbitrary Function Generator (AN-06), explains how the software and generator solve waveform-generation problems. The note discusses creating simulated waveforms using waveform editing techniques and sequence files. Examples of complex operations, such as time-shifting a segment of waveform captured on a vendor DSO, are given in a hands-on, step-by-step presentation.

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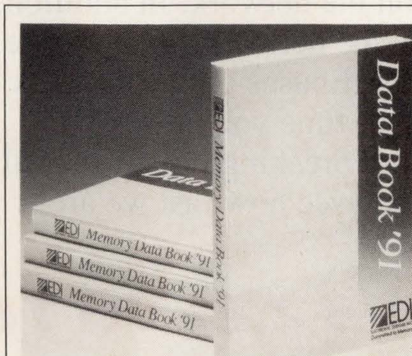

Publication Presents Memory Products

This 380-pg data book provides complete data on the vendor's standard memory products, including an expanded line of static RAMs, SRAM modules for commercial applications, and a preview of upcoming products. A summary lists part numbers with specifications such as speeds, current consumption, and package options. It also lists military products from the Defense Electronics Supply Center's Standardized Military Drawing Program and defines the vendor's reliability program. Indices to parts are arranged according to part numbers and function/density. Other features include a section of detailed package drawings and application notes.

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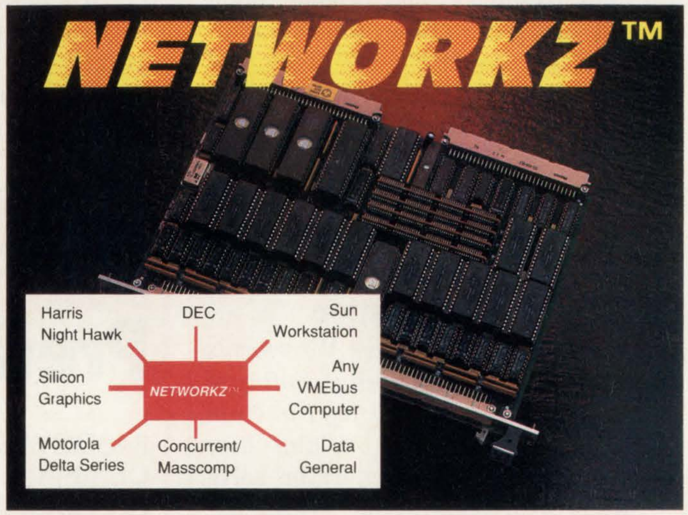

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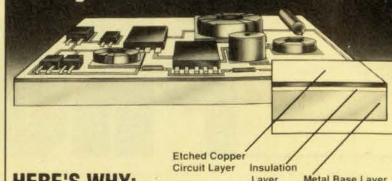

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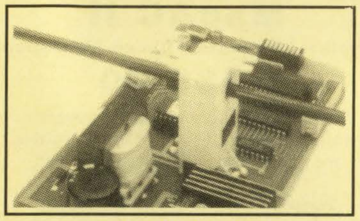

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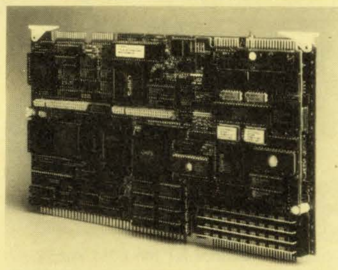

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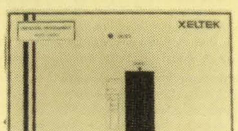

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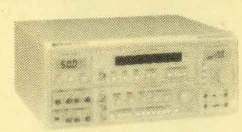

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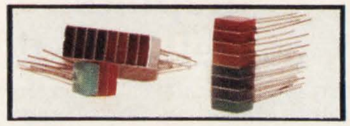

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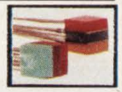

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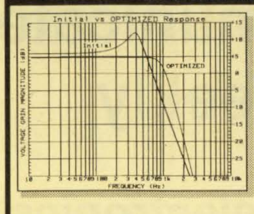

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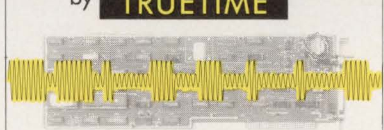

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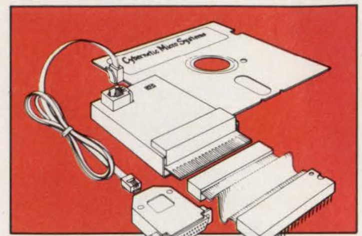

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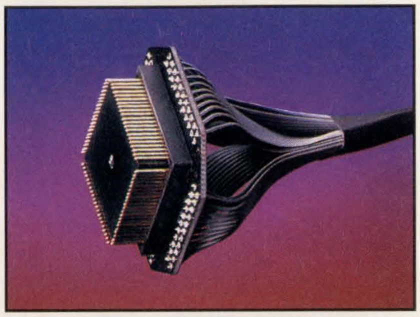

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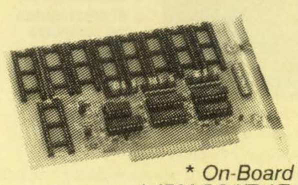

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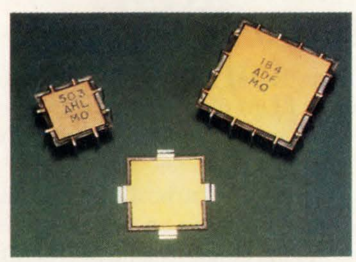

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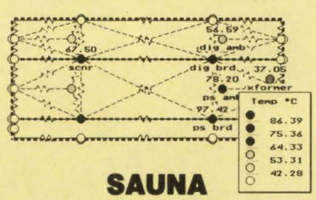

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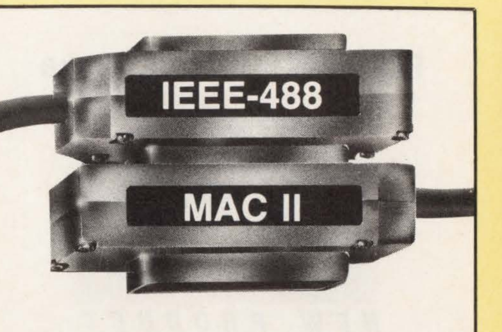

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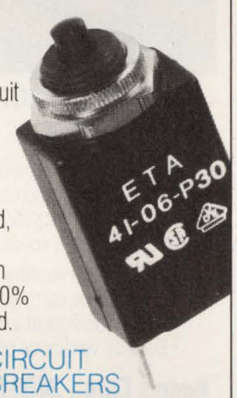

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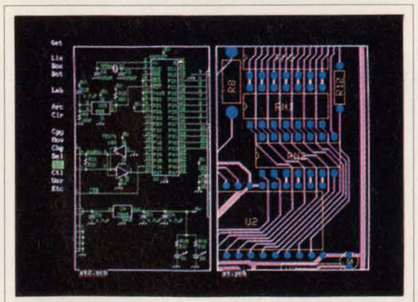

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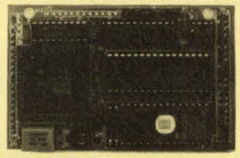

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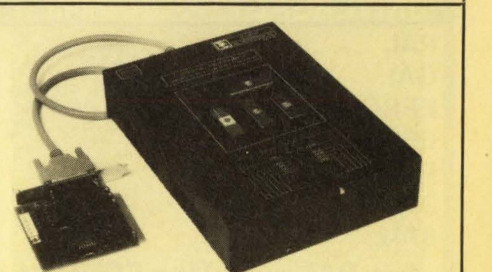

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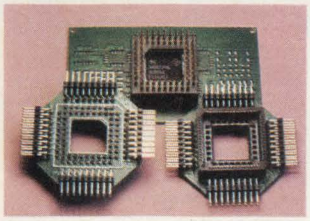

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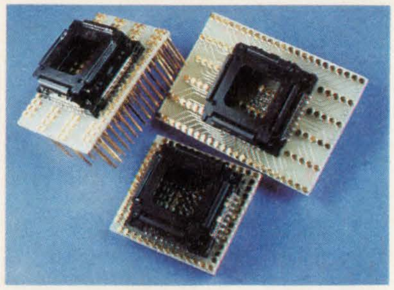

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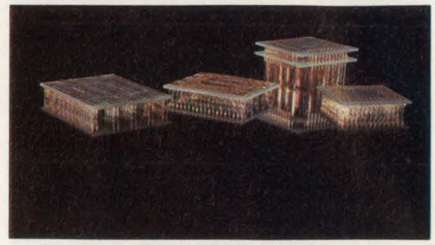

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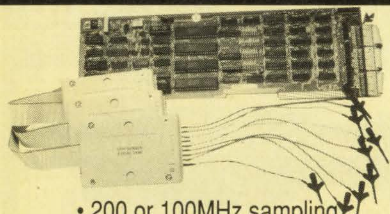

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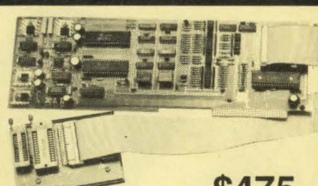

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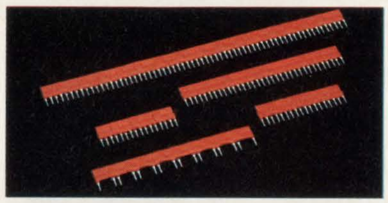

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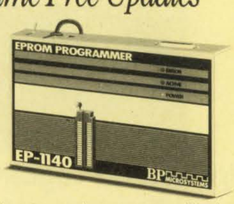

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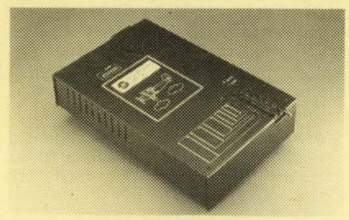

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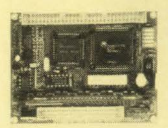

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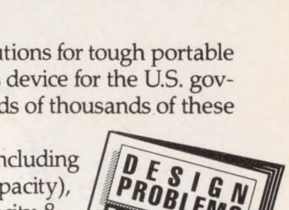

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CIRCLE NO. 172

The Job-

Unemployment among electrical engineers has not yet reached crisis proportions, but engineers who have been thrown back into the job market tell a different tale.

Julie Anne Schofield,
Associate Editor

You can't seem to get through a week's worth of newspapers these days without reading about another company's laying off tens or hundreds or even thousands of workers—including many engineers. Sometimes these announcements make the front page. At the same time, the help-wanted section of the Sunday paper continues to dwindle. Happy new year.

Companies recently making news with layoffs include Teradyne (Boston, MA), Texas Instruments Defense Systems & Electronics Group (Dallas, TX), Oracle Systems Corp (Redwood City, CA), National Semiconductor (Santa Clara, CA), VLSI Technology (San Jose, CA), Bull HN Information Systems (Billerica, MA), Mitre Corp (Bedford, MA), Digital

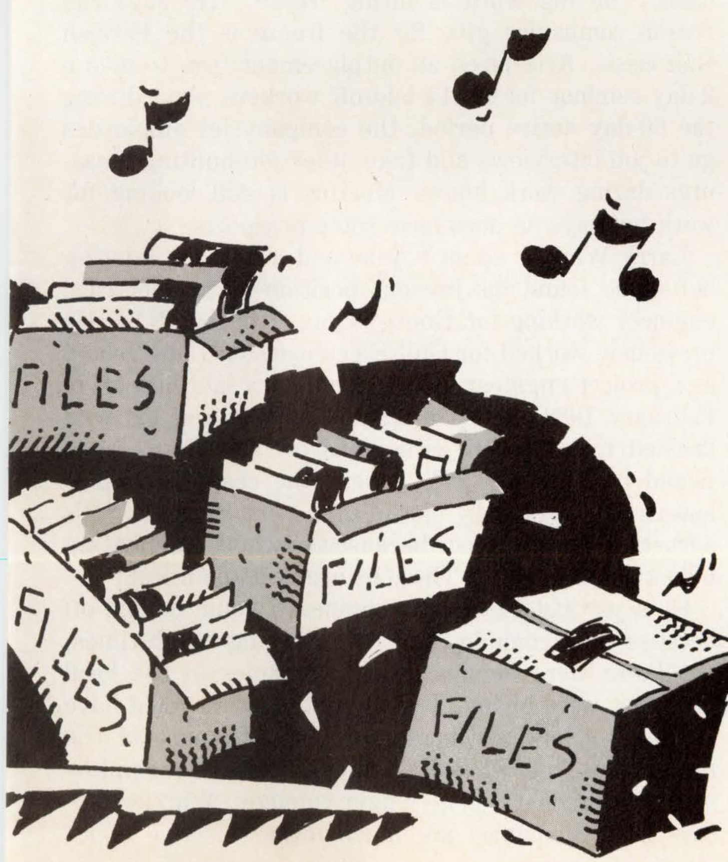
Illustrations by Jim Lambrenos

Hunting Blues

Equipment Corp, Data General (Westborough, MA), and General Dynamics (Fort Worth, TX). The list goes on. The companies vary in size. Some do defense work; some don't. Some are well-established firms that are "downsizing;" others are floundering startups.

No one factor is to blame for the increase in unemployment. Iraq's invasion of Kuwait exacerbated an already sluggish economy. Consumers concerned about the economy are wary of making big purchases, which affects commercial firms. Defense-budget cuts have forced many companies to cut their staffs, and, according to the Bureau of Labor Statistics, the paychecks of one in six electrical engineers depend on defense spending. How the situation in the Persian Gulf will affect defense cuts is still unclear.

Many of the layoffs are in regional pockets, according



to Robert A Rivers, editor of *The Engineering Manpower Newsletter*. Areas hardest hit include New England, Long Island, New Jersey, Texas, and the Silicon Valley. In his newsletter, Rivers says the jobless rate for electrical engineers was 2.2% in the third quarter of 1990, or approximately 12,000 electrical engineers. The rate usually hovers between 1 and 2%, says Rivers. The Bureau of Labor Statistics reported that the national unemployment rate in October was 5.7%.

Rivers expects electrical-engineering unemployment to increase in the first quarter of this year, "After the first quarter, things will start getting better. This is not a crisis situation, but it is a crisis for those people being eliminated." However, he is quick to point out that even his unemployment statistics are deceptively low. An engineer who takes a job with Sears is considered employed, even though that person has left the field—at least temporarily. His statistics also do not include engineers who took the early-retirement option.

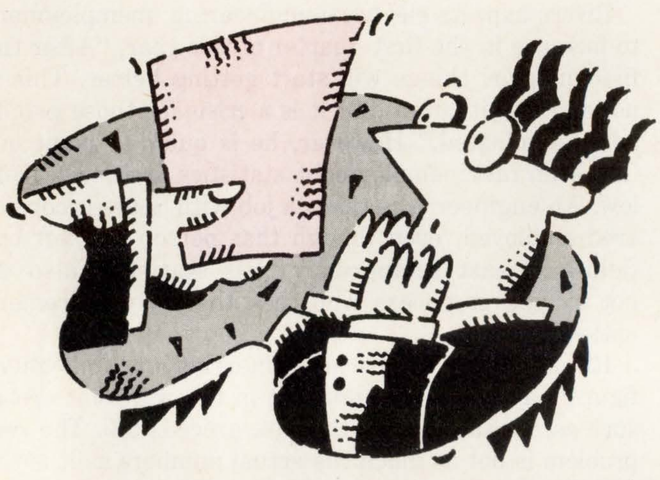
Rivers's 2.2% electrical-engineering unemployment figure may not seem high, but in the worst-hit areas, such as Massachusetts, the rate exceeds 5%. The real problem is not as much the actual numbers as it is the difficulty many unemployed electrical engineers have finding that next job. These difficulties go beyond out-of-date resumes, rusty interviewing skills, and the emotional turmoil common to all terminated workers—and the outplacement agencies companies hire do not address them.

Keeping up to date

A major problem for electrical engineers is that their field changes so rapidly. Computers and peripherals, communications equipment, and signal processing are all evolving, and keeping up to date is no easy matter. However, changing technology is not the only problem. "I hate to say it," says Joseph DeSalvo, chairman of the Career Activities Council of the IEEE-USA, "but we can become fat cats in a hurry. A young engineer graduates from a university, goes out and gets a good-paying job with good fringe benefits. The spouse has a job and is making reasonable money. They're making a lot of money and tend to forget about their goals and objectives in life." They don't think about their career future or consider what could happen 5, 10, or 15 years hence.

Engineers should think of themselves as products whose value will exist only as long as they keep their continuing education up to the state of the art, says DeSalvo. Otherwise, they will lose their value to present and prospective employers. He warns, "An engineer can become technically obsolete within a decade if he is not active."

Keeping up with his field didn't help James J Klinikowski. AT&T Bell Laboratories (Allentown, PA) laid him off from his position as a Member of Technical Staff in December of 1989. He holds 13 US patents and has published more than a dozen technical magazine articles. For the last eight years, he had been working in the NMOS and CMOS design of integrated-



circuit DSP chips. He says he has kept up to date with Unix, C, and CAD.

"No matter what angle you consider this situation from," Klinikowski says, "there is no justification for keeping a man from age 47 to 59 and then depriving him of the reason he worked there all those years—retirement. I missed it by 14 months."

In the three months he had before being removed from the payroll, Klinikowski was offered only one interview after 60 to 80 internal job inquiries. Because the job involved much travel as well as relocation, he couldn't consider it—his wife is disabled. Losing his job also meant losing paid life and medical insurance for himself and his wife, as well as losing his pension.

Klinikowski faces a number of obstacles in his search for an electrical-engineering job. First, he says that because AT&T is one of the most respected companies in the industry, prospective employers would be suspicious of a former member of technical staff saying he lost his job after 13 years of service in a corporate downsizing. He believes that companies are reluctant to hire older employees because medical-plan costs would greatly increase. Klinikowski also cites the many engineers who have opted for early retirement with a pension and full benefits as competition for scarce jobs, "These retirees are willing to work for almost nothing. Some just to keep busy. I have to compete against them in the job market."

Because he believes that finding a job that would satisfy his retirement-plan and medical-benefit needs would be impossible, Klinikowski hopes to secure design, consulting, technical-writing, or management work to support his wife and himself.

Softening the blow

Brad Morrow, 34, has more reason to be optimistic. Arix Computer Corp (Scottsdale, AZ) notified him in October 1990 that he would be laid off from his job as an engineering programming manager in 60 days. He got a generous severance package and says that since the notice, it would be four months until the money ran out.

He is looking everywhere for a job and says that he is willing to relocate, "The job market here is real tight. The big word is hiring freeze." He says the reason companies give for the freeze is the Persian Gulf crisis. Arix hired an outplacement firm to give a 2-day seminar for its 14 laid-off workers. And during the 60-day notice period, the company let employees go to job interviews and take other job-hunting measures during work hours. Morrow is still looking for work but says he does have some prospects.

Larry Winkler spent a year and a half job hunting before he found his present position as an electrical engineer working for Energy-Onix (Hudson, NY). He previously worked for Gull Electronics on Long Island as a project engineer, but the company laid him off in February 1988. After losing his job, he and his wife decided to go ahead with plans to move from Long Island to Kingston, NY, where the cost of living is lower. He occasionally picked up a consulting job. "It's a frustrating experience because the whole engineering industry is changing. The jobs aren't as plentiful."

He says that previously, engineers would be laid off because their company was experiencing rough times, but there were always other companies in the local area that were hiring. Three months later, you'd have another job and an increase in pay. Because of the regional pockets of electrical-engineering unemployment, this scenario is no longer common. Winkler also says that companies are much more selective about

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CIRCLE NO. 173

hiring now, "They're looking for someone who can fit right into a job, so you have to match it almost 100%." Companies can afford to be selective, he says, because of the glut of engineers. (Don't even mention the purported engineer shortage to an engineer—unemployed or otherwise—unless you're prepared for an earful.)

When asked if his age—50—hindered his job search, Winkler says, "Age and salary level go together. And whether you want to call it age discrimination or salary discrimination, I think that companies are bargain hunters. They'll pass over someone making a higher salary for someone making a lower salary."

Robert Bruce took early retirement at age 63 after his employer, AIL Systems, a division of Eaton Corp (Melville, NY), announced in the newspapers that it would lay off 800 of 3800 people. "I saw the writing on the wall for the whole aerospace sector as well as my company, and I took the early-retirement incentive." He retired September 28, 1990. (Most engineers interviewed for this article gave the exact date when they retired or were laid off.) He blames defense cuts for most of the layoffs, adding that the largest concentration of engineers in any identifiable industry is in defense and that electrical engineers constitute the largest portion of those engineers.

He believes that engineers are hit worse during economic recessions than other professionals because engineers depend on a growing economy for jobs. "When a company is cranking out the same old product line, they need only a couple of engineers. It's when companies undertake new developments that they really need engineers," says Bruce.

He's been looking for work since July but has been unable to find an engineering job. In the interim, he teaches electronics part-time in a trade school—a job he enjoys but which pays approximately half his former salary by the hour. Bruce continues to look for an engineering job but doesn't want to relocate, "I'm pessimistic. I know that I'll find one eventually if age discrimination is not an overwhelming factor. But I may have to ride out the recession on my retirement funds plus the part-time salary."

Many commercial firms are reluctant to hire former defense engineers because of the differing demands of the two types of work. Commercial projects are cost sensitive and don't always use state-of-the-art parts and equipment. Cost is not a primary concern in defense work, as are performance and using state-of-the-art technology. Also, many defense engineers become so specialized that employers are wary of hiring them for less-specialized work. Many employers don't look upon engineering skills as transferable.

Unemployment is especially bad among specific

demographic and engineering specialty groups. John Densler, consultant, and cochairman of the Boston IEEE Professional Activities Committee for Engineers, says that electrical engineers that have a particularly difficult time finding new engineering jobs are older engineers, hardware engineers, and former defense engineers. Older engineers face several problems when seeking engineering employment: They may not be as up to date as younger engineers; because of years of experience they command higher salaries; they require more expensive benefits; they may have become too specialized. Also, many who "choose" early retirement really have no choice. Given the choice between early retirement or being laid off with no benefits, many are forced to choose the lesser evil even when they cannot afford or have no desire to stop working. Hence James Klinikowski's worries about competing with retirees who may be willing to work for less.

Creating opportunities

Paths for electrical engineers to take to rejoin the work force certainly aren't clamoring for attention. But some people in the industry are working to offer good advice—and even some real help.

Bill Wilkes, a systems engineer who has worked in military fields since 1963, also saw the writing on the wall for older engineers and defense engineers. A little more than a year ago, he and psychologist/management consultant Diane Kramer started the nonprofit Center for Practical Solutions (CPS) in Hauppauge, NY, of which they are now the executive directors. The CPS has two goals: economic development and shoehorning older defense engineers into the commercial sector. It accomplishes these goals by linking technology professionals with entrepreneurs, accountants, marketing people, and lawyers to develop new businesses.

"Many older, displaced engineers will never have the opportunity to work in their field again," says

Wilkes, "Their best shot is to try to create enterprises of their own." The CPS also helps engineers develop unique working relationships with established companies. Wilkes says that older engineers still have valuable skills, and managers may want to retain them as consultants.

"Engineers have to move away from traditional employment situations because the jobs aren't there," Wilkes continues. Rather than chasing nonexistent jobs until the unemployment insurance runs out and the savings dwindle, he suggests that jobless engineers create opportunities for themselves. He says engineers can't leave finding employment up to politicians because politicians don't understand technology or engineers' needs. Companies are interested in surviving and cutting costs, he says, not placing laid-off engineers. He cofounded the CPS because a single engineer can't change the world alone.

The CPS operates on a shoestring budget in donated office space. Members, many of whom hold patents, meet Tuesday nights. Kramer says five project teams are currently working to become businesses. "Where there's a need, there's a niche. We find the niche and work with the project teams. When the teams are ready, they work with our business-development unit to launch them as businesses."

The technology areas in which the CPS would like to start project teams working include information processing, energy-efficient devices, aids for the elderly and handicapped, and telecommunications. It already has teams working in educational software and customized computer-manufacturing services with robotics and artificial intelligence—all fields that Kramer says can use defense engineers' talents. The first business the CPS developed is Innovations Development Corp, "It is a project-management company to take inventions and walk them through the manufacturing and marketing stages."

Take control

But few other groups exist that directly help electrical engineers get back to work. Thus, always being prepared for the possibility of losing your job is essential. Joseph DeSalvo says electrical engineers should take a more active role in their careers. "They know better than anyone else what their career goals and objectives in life are." He suggests that engineers establish short-, medium-, and long-term goals and take whatever steps are needed to achieve them.

John Densler also calls on engineers to be more savvy about their careers. "Don't go into areas where you don't get rewarded," he says. "Go into marketing or venture capital. But for God's sake, don't go into manufacturing." Manufacturing is the sector in which most electrical-engineering jobs are being cut.

When you're involuntarily unemployed, you've got three job-hunting choices. You can try to land another engineering job, you can take a job in another field, or you can go into business for yourself. You should first take some time to explore each option. Find out about the economic environment and employment prospects, and use that information to make your career decision. Once the outplacement services your former company provides end, you're on your own.

When returning to the job market, ultimately you have to rely on your own knowledge, your own imagination, and your own goals to find meaningful, paying work. However, don't forget the support of friends and family. You needn't feel cut off from the whole world when only your position has been cut. And if the job search gets to be too much, psychologists and psychiatrists are there to help. Many unemployed people become depressed; they may experience feelings of worthlessness, anxiety, and despair; sleeping or eating problems; or fatigue. If depression lasts more than two weeks, consider seeking professional help. EDN

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1991 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
Magazine Edition	Feb. 4	Jan. 9, '91	Computer Peripherals, ASICs/ CAE • CAE Software, Software Development
News Edition	Feb. 7	Jan. 18, '91	Imaging Boards & Coprocessors, Software**
Magazine Edition	Feb. 18	Jan. 24	Surface Mount Technology • CAE Engineering Software, Components, Analog Circuits, Bus Packaging/ Test & Measurement • Power Sources •
News Edition	Feb. 21	Feb. 1	Computer Peripherals, Graphics**, Regional Profile: Oregon & Washington State**
Magazine Edition	Mar. 1	Feb. 6	Communications Special Issue, ICs & Semiconductors, CAE • Computer Peripherals • Fiber Optics
News Edition	Mar. 7	Feb. 14	Special Supplement: State of Engineering • Medical Electronics**
Magazine Edition	Mar. 14	Feb. 21	Software Tools, Computer Architectures, Materials Technology, ICs & Semiconductors/Instrumentation Circuits
Magazine Edition	Mar. 14	Feb. 21	Software Engineering Special Issue, (To be polybagged with the March 14th Magazine Edition issue)
News Edition	Mar. 21	Mar. 1	CAE, Computer Buses**, Regional Profile: Alabama, Georgia, N. Carolina**
Magazine Edition	Mar. 28	Mar. 7	ICs & Semiconductors/ Microprocessors, Software • CAE • Computer Boards, Electro Preview Issue
News Edition	Apr. 4	Mar. 15	Optical Interconnects, Automotive Electronics**, Electro Show Issue
Magazine Edition	Apr. 11	Mar. 21	Power Sources, CAE/ASICs, Test & Measurement, Sensors, Electro Show Issue
News Edition	Apr. 18	Mar. 29	Distribution, Optics**, Regional Profile: No. California**
Magazine Edition	Apr. 25	Apr. 4	Computers & Peripherals Special Issue, Computers & Peripherals/ Memory Design, Data Storage Technology, ICs & Semiconductors, ASICs
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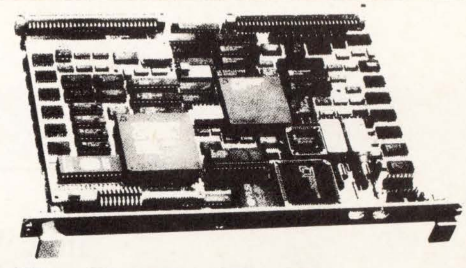

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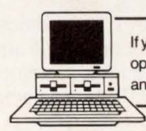

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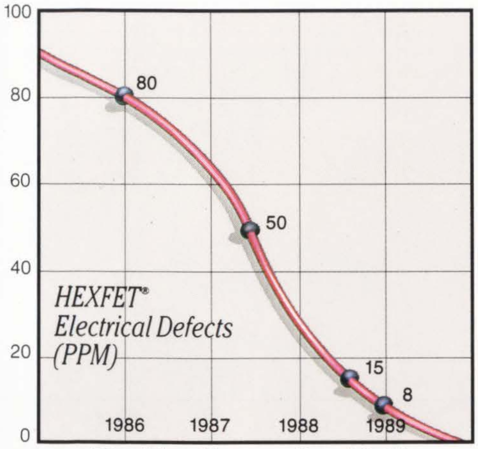

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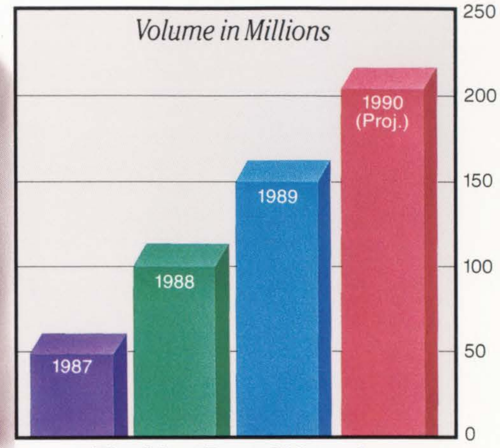

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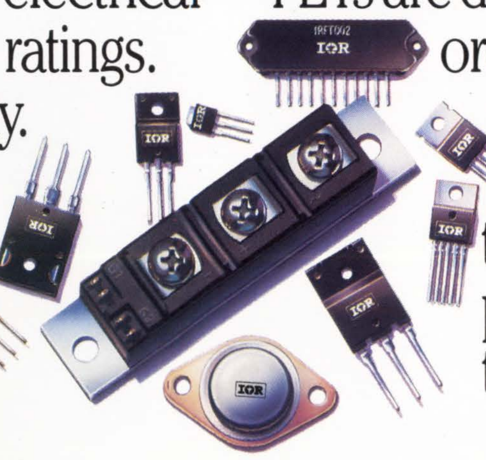

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