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# ElectronicDesign®

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

NOVEMBER 15, 1984


## COMPUTER-AIDED ENGINEERING

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**Language helps make designs testable**


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CIRCLE 131

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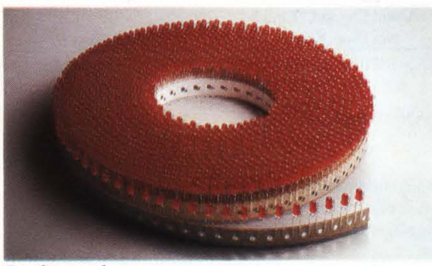

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ED 11/15/84

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CIRCLE 2

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# BEHIND THE COVER

Chips, boards, and boxes—the cover motifs—naturally suggest hardware, yet most of the articles in this issue's editorial package on computer-aided engineering are about software (p. 126). This apparent contradiction emphasizes the growing importance of software tools for hardware design—the almost universal reliance on CAE.

It was not always so. Mainframes, minicomputers, and even microcomputers were first designed by hand, much like bridges and airplanes. But while CAD for most mechanical devices is merely an efficiency tool, CAE has become a necessity for today's digital systems. In a way, it epitomizes the so-called second computer revolution, in which software dominates hardware.

A microcomputer pioneer once said: "We used to think that making as powerful a machine as the desktop computer would automatically generate endless applications in the home, the office, and the factory. Now we know better. The software must be in place first."

Right now, IC design is benefiting the most from CAE. Ultimately, chip designers may be able to feed the appropriate application software to a CAE system and have the best hardware for the job emerge from the foundry some days later. Before that vision becomes a reality, a major obstacle must be overcome—the lack of a uniform system of CAE languages.

Coming up with a uniform means of software communication is not likely to happen by itself. The Electronic Design Interchange Format (EDIF), a standard being proposed by a consortium of CAE manufacturers, is now ready for a vote, but it is not well-known. To wit, when a speaker at the International Conference on Computer Design was asked whether his hardware description language—the fifth introduced at that conference alone—would be compatible with EDIF, he replied, "What's EDIF?"

Obviously, communication among different CAE software systems is a necessity before IC design can be completely automated. Fortunately, suppliers of CAE software and hardware are laying the groundwork.

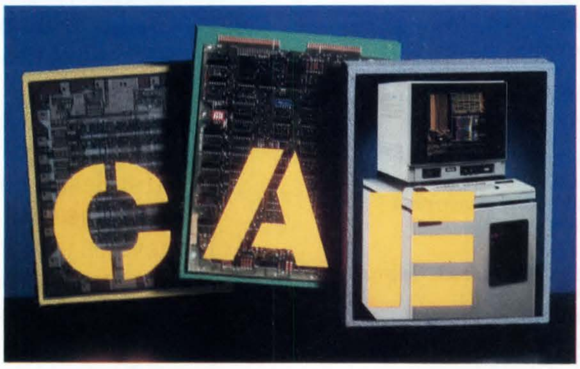
ElectronicDesign
November 15, 1984 • Vol. 32 No. 23

## DEPARTMENTS



## COMPUTER-AIDED ENGINEERING






### Design Entries



## TECHNOLOGY NEWS

## DESIGN ENTRIES



## NEW PRODUCTS



IN THE NEXT ISSUE

Technology Report: Testing VLSI circuits ... Personal Computer Series: Part 1 of a two-part survey ... Product Report: Focus on advanced logic ... Details on a high-density EPROM ... Conference Preview: IEDM.

Cover photograph by Ken Schroers

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# CONTENTS SPOTLIGHT

## Cover: Computer-aided engineering 126

As the methods and equipment for designing ICs become more sophisticated, engineers are naturally turning their sights toward application-specific ICs, single chips that can conceivably replace an entire circuit board. The Technology Report in this issue (p. 128) details the ways in which manufacturers of CAE software and turnkey systems are transforming digital system designers into IC specialists. The second part of the Technology Report, scheduled for the Dec. 13 issue, will cover the physical realization of application-specific ICs.

One of the most important CAE tools is the silicon compiler. One such package produces CMOS chips that typically reach 90% the density and 100% the performance of their handcrafted counterparts (p. 149). A second silicon compiler, this one designed for engineers with no hardware experience, works directly from a functional description of the chip (p. 187). Another setup directly links a CAE workstation to a pc board CAD system, yielding a cost-effective merger that follows a chip virtually from start to finish (p. 169). Finally, a testing software package bridges the gap between designing a circuit and writing the test programs for it (p. 207).

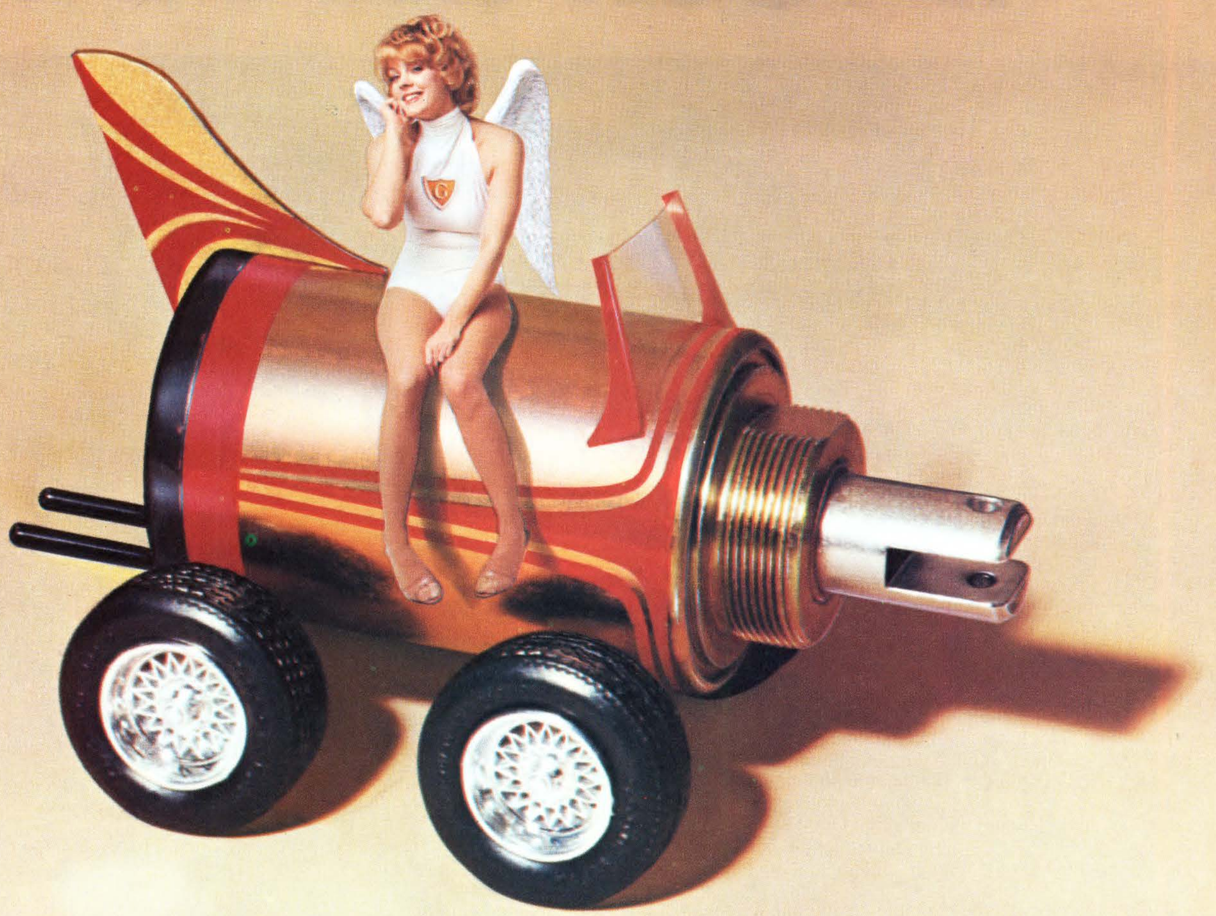
## Microprogrammable chip family 229

Taking a new approach, five VLSI chips extend the bit-slice concept to 32 bits while satisfying system designs that require cycle times of less than 100 ns. In fact, designers of microcoded systems can count on cycle times of 70 to 80 ns, using merely a handful of components. Following the introduction, two articles present an overview of the family (p. 230) and details on how to apply the math chips to jobs like fast Fourier transforms (p. 246).

## News Analysis 65

With Winchester disk drives expected to tip the bit-density scales at about 40,000 bpi by 1990, the industry is busily developing new materials for coating the disks themselves. Sputtered and plated thin films are emerging as the chief candidates, with sputtering holding an early lead.

# With 156,563 standard models...



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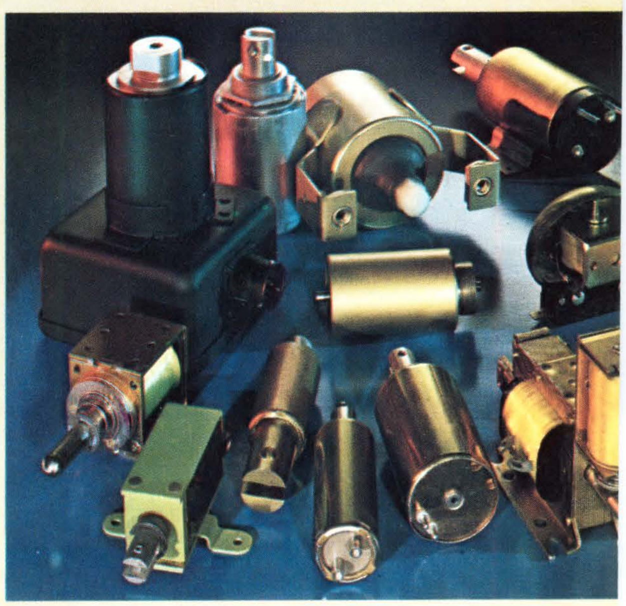

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CIRCLE 5

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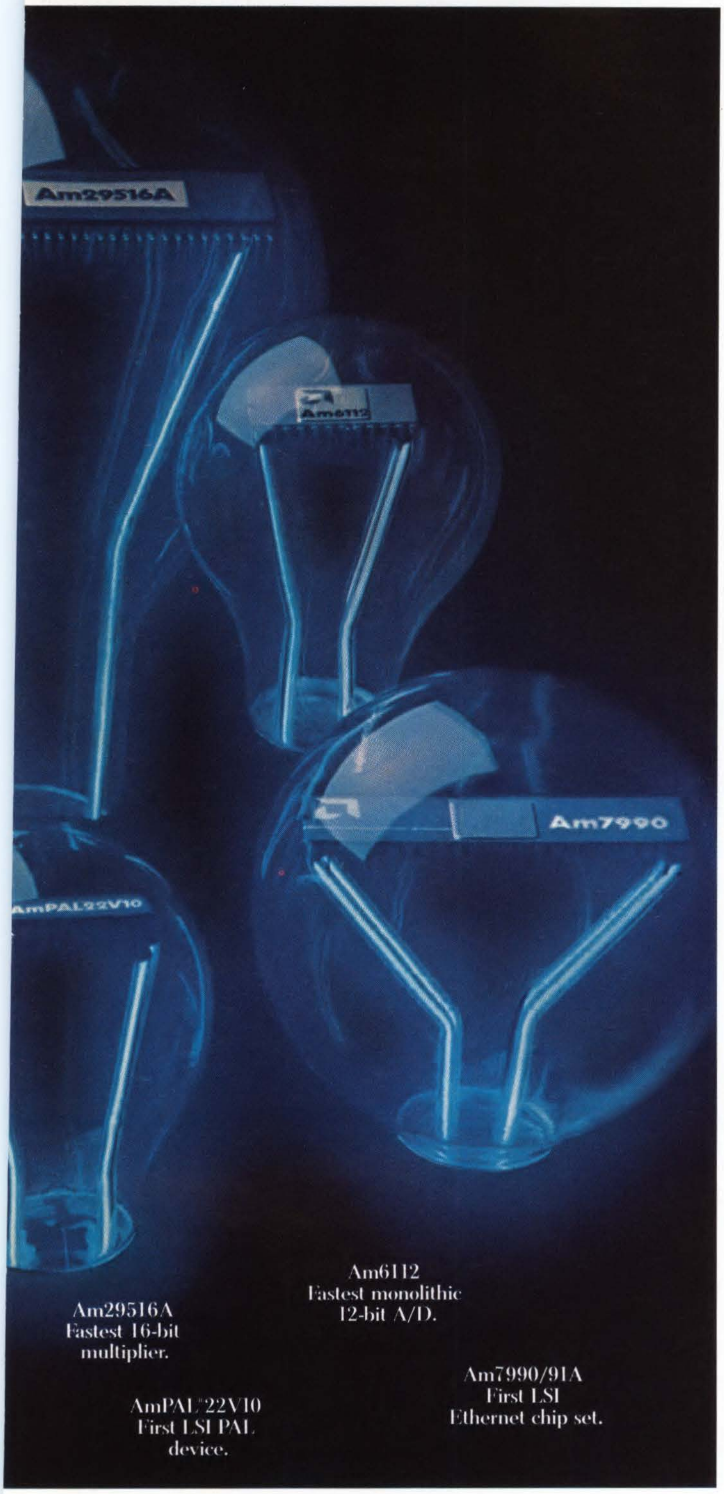


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CIRCLE 6


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CIRCLE 7

# ON REFLECTION

## For the record: Wiener on the invention of the loading coil

The human mind is a funny thing, at least mine is. I had completely forgotten about Norbert Wiener, Oliver Heaviside, and the great loading-coil scam until the name of Michael Pupin came up at a press conference. Then the long-buried images returned: Wiener, dripping wet, coming into the meeting room; the wet paper bag containing the sole existing copy of the manuscript; and Wiener, speaking without notes, casually giving us the keys to his *roman a clef*.

In the interest of completing the historical record, the facts are these. About 25 years ago, on a wet winter's night, Professor Norbert Wiener told a group of no more than 10 or 15 students at MIT the real story behind his just-completed novel, *The Tempter*.

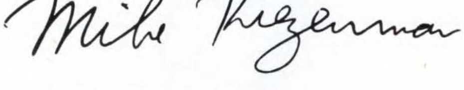
In the early days of long-distance telegraphy, signaling speed was limited by the distributed capacitance between the transmission line and ground. According to Wiener, English physicist Oliver Heaviside was the first person to recognize that and propose a workable solution—the placement of lumped series inductances at regular intervals along the line.

Since that technique could ultimately produce long-distance cables (including undersea cables) with vastly greater capacities for carrying information, it would save communications companies a great deal of money by reducing the number of cables necessary. The companies wanted permission to use Heaviside's idea, and one of them approached—or rather, tried to approach—Heaviside to make some sort of arrangement. But, as Wiener told us, Heaviside was such an eccentric that you couldn't make a deal with him. Not because he wanted too much money, but simply because he refused to negotiate at all.

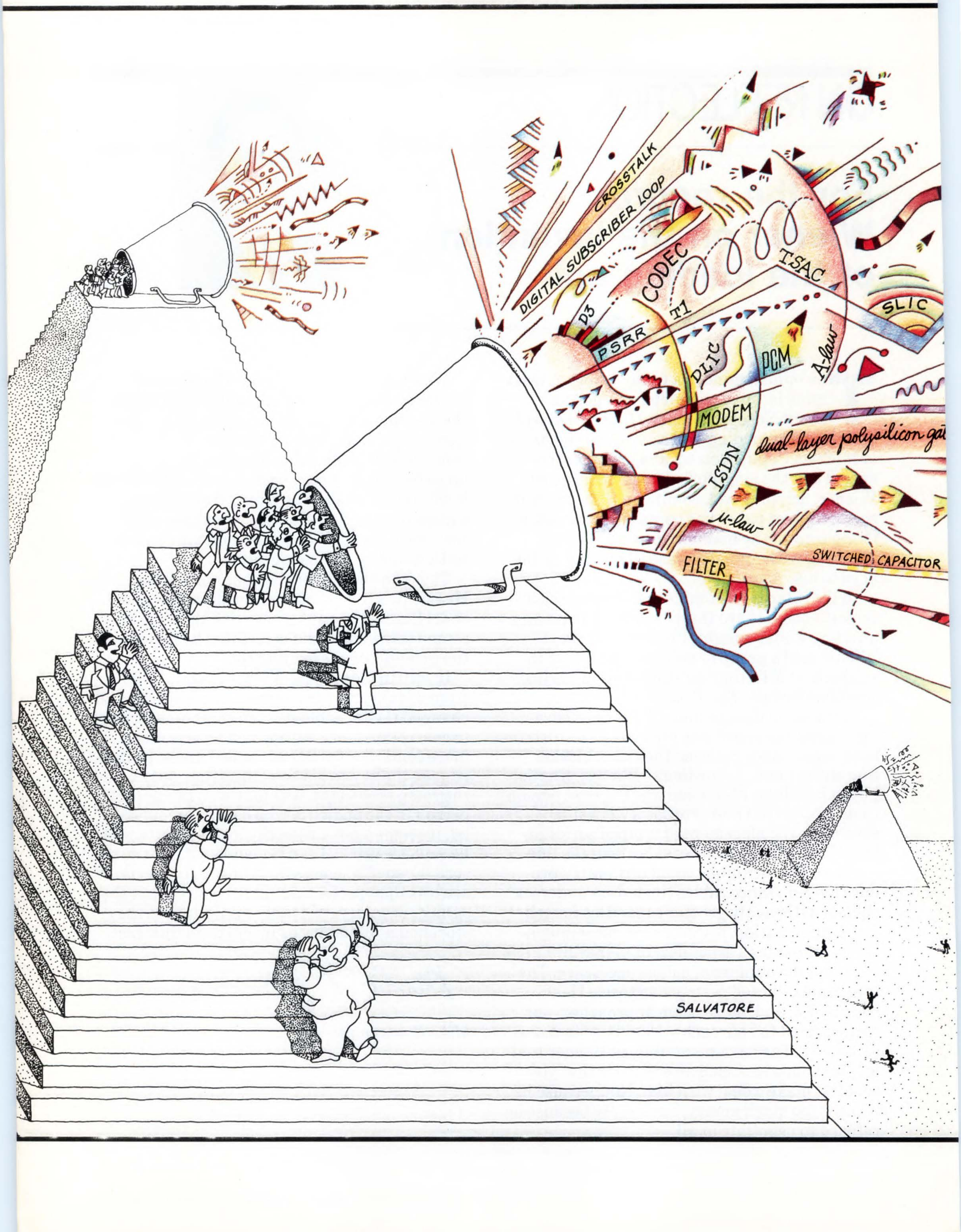
Well that just wouldn't do. The spurned company desperately wanted the right to use the loading-coil idea. So it conceived the stratagem of publicly buying the rights to the invention from a plausible inventor for a very large fee. Thus, it reasoned, no one would think it was trying to steal anything from anyone. If a dispute should ever arise over whose rights they were to sell, at least the company's good faith would be beyond question.

The man chosen for the honor of selling Heaviside's invention to the company was Michael Pupin. He went along with the idea, accepted the money, and is credited by history as the inventor of the loading coil.

In writing his novel, Wiener changed Pupin from a Hungarian immigrant to a Mexican and changed the technology from communications to control systems, with which he was much more comfortable. But as far as I know, he never gave the key to his book to anyone outside the room that night. As I may well be the only person in the audience who became a journalist, it seems a not-unworthy idea to relate what he said, as well as I can remember it, for the record. Even if Wiener's facts or my recollections are less than perfect, doing so ensures that the subject is not irretrievably committed to the storehouse of history as incontrovertible fact.



*Mike Riezenman*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CIRCLE 8

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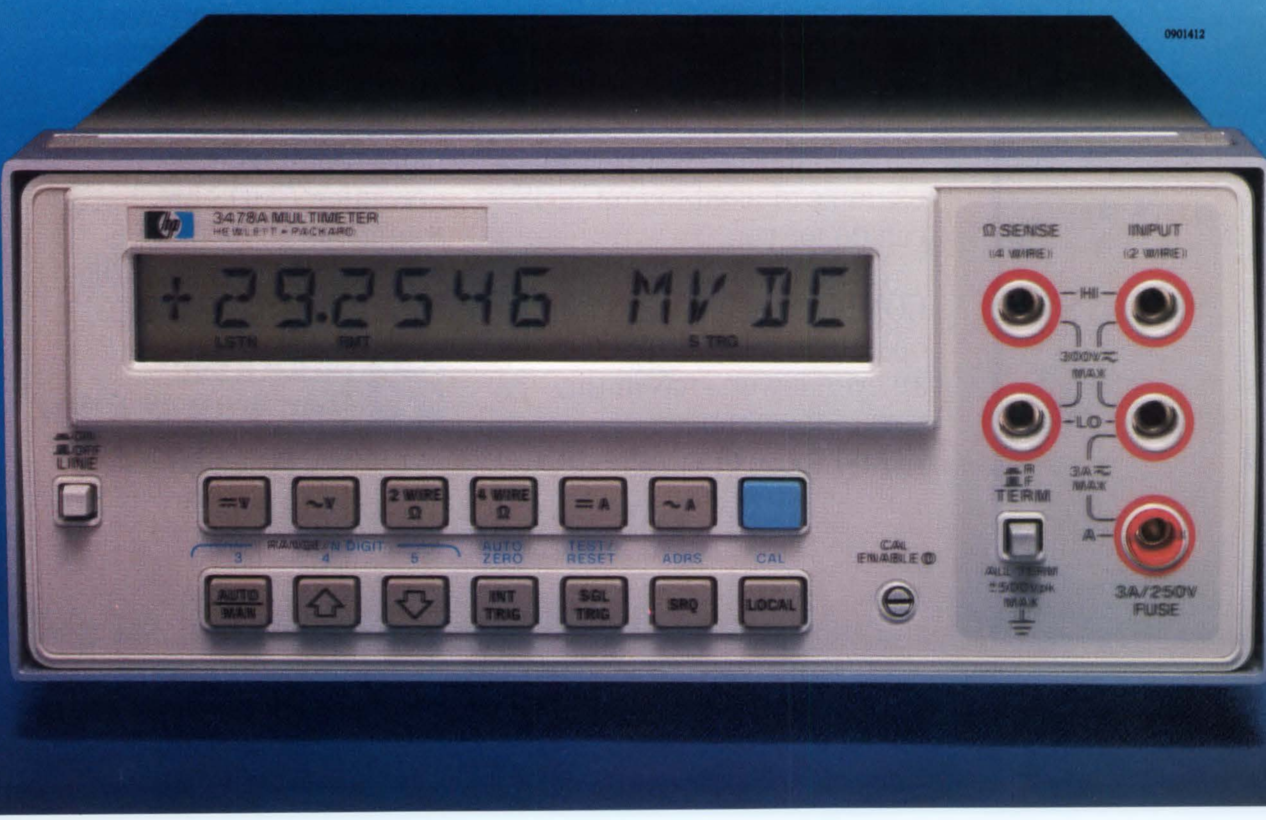

# READER FEEDBACK

## Futurebus: The opposite is true

I was surprised to see so many unlikely comments made about the Futurebus in a Viewpoint in your Sept. 20 issue ["Standard Buses May Yield to Proprietary Brethren and Self-Contained Boxes," p. 82].

The statement implying that the P896 Futurebus Working Group considers high performance and processor independence mutually exclusive is untrue. In fact, it considers the opposite to be true: Tie the bus to the protocol of a processor and you will limit the performance of the bus. Recent work on benchmarking the performance of the P896 protocol shows that, when specifying real parts, the bus has a maximum throughput of between 68.9 and 117.6 Mbytes/s (J. Theus and Paul Borrill, "An Advanced Communication Protocol for the Proposed IEEE 896 Futurebus," *IEEE Micro*, vol. 4, no. 4 [August 1984], pp. 42-56). I see no proprietary bus capable of even approaching these performance levels. Also, because the P896 protocol is completely processor-independent, further increases in performance will occur as technology improves.

But perhaps I am being a little unfair. P896 does, after all, have an elegant transceiver technology which solves the bus-driving problem (R. V. Balakrishnan, "The Proposed IEEE 896 Futurebus: A Solution to the Bus Driving Problem," *IEEE Micro*, vol. 4, no. 4 [August 1984], pp. 23-27). In addition, it has been designed more recently and with more consideration of diverse applications, more care for manufacturer independence, more prototyping, and more thought by more people than most proprietary bus designs.

More importantly, as every knowledgeable computer architect knows, the key is not the maximum performance of the bus, but rather capitalizing on the available performance in a real system. Multibus II employs an architectural method to preserve as much bandwidth as possible in a real system: It uses a message-passing protocol between processors, implemented in hardware to maximize system concurrency. P896 is also equipped with such facilities; it supports replicated shared memories, caches, and hooks to extend the protocol to higher-level messagelike protocols suitable for specialized systems.

**Paul L. Borrill**
Chairman, IEEE P896 and IEEE Multibus II Working Groups
University College—London
Dorking, England

## Corrections

*The New Products feature on Motorola's color video processors (Sept. 6, p. 306) contained two incorrect sentences and one misleading*

## READER FEEDBACK

*one. In the second paragraph, discussing the TDA-3333, the second and third sentences should have read:*

*"It targets video systems that can supply their own RGB matrix but that need a separate circuit to generate the R − Y (red minus luminance) and B − Y (blue minus luminance) signals. The chip also provides the color and tint controls."*

*The statement at the end of the description of the TDA3330 (the fourth paragraph) about a separate driver is true for all three chips. It should have said: "With this chip, all that is required are three video-output transistors to interface with the picture tube."*

*In addition, there were some mistakes in the block diagram: The block labeled "logic" is instead an input network; it should have produced the input to the color i-f filter; and the final outputs go on to the color video outputs.*

*The prices of Integrated Device Technology's CMOS FIFO chips were reversed in our Oct. 31 New Product story (p. 427). The price for the IDT7202 is $86 apiece and that of the IDT7201 $48 in 100-unit quantities.*

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Editor-in-Chief, Electronic Design, 10 Mulholland Drive, Hasbrouck Heights, N.J. 07604. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.

# The Hamburger Theory of CAE Workstations

Metheus-Computervision

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## THE CAE BUSINESS WELCOMES A WHOPPER.

On June 18, 1984, two companies joined forces in a way that will dramatically alter the business of computer-aided engineering. For good.

> "Among the big CAD/CAM companies entering the (CAE) fray... Computervision is a major threat.... The Little Three are competing so strenuously among themselves... they aren't focusing on the shadows in the hills."
>
> —*Fortune* Magazine, June 11, 1984

Metheus and Computervision formed a joint venture called, appropriately enough, Metheus-Computervision.

It combines the experience of Metheus, one of the original CAE pioneers, with the assets of Computervision, the worldwide leader in the giant CAD/CAM industry.

Metheus-Computervision now becomes the first CAE supplier with a mature product line backed by major resources. And we do mean major. Other CAE competitors are literally dwarfed by Computervision's financial strength, and by its worldwide service support. All of which are now behind MCV design tools.

Meanwhile, both companies will maintain operations separate from the joint venture. Computervision, of course, will continue its perennial leadership in the automated design and engineering industry. Metheus Corporation will specialize in high resolution graphics controllers and UNIX™ workstations. Interaction between the two original companies will give our CAE customers the best of both. With MCV, you can move smoothly across the spectrum into Computervision's CAD/CAM products, and still make just one phone call for service support.

## BYE-BYE, SMALL FRY?

A recent article in *Fortune* magazine described computer-aided engineering as an industry dominated by "The Little Three": Daisy, Mentor and Valid. Three good, but relatively small companies.

The article went on to note that the business is about to enter a new era—one in which a few giant companies could take the market away from the start-ups who pioneered it.

True to the *Fortune* prediction, the first giant has arrived. And not a moment too soon. Electronics companies have been hungry for the productivity that CAE can put on an engineer's desk. But lurking in the back of everyone's mind is a fear of getting locked into a supplier backed by relatively modest resources. A company that, gulp, might not be around in three years. So the strength of Computervision is a welcome addition.

Does that mean "The Little Three" are about to become extinct? Not necessarily. As *Fortune* pointed out, one or more could survive, and even thrive. But the ground rules are changing.

For the first time, there are CAE design tools with a big league company behind them. And there's now a combined resource that will be able to supply every CAE/CAD/CAM/CAT application your company could ever grow into.

Other big companies will undoubtedly follow. But it's not likely they'll have the kind of specialized expertise, and the proven experience, that's just become available from a company destined to be known as MCV.

METHEUS-COMPUTERVISION

*We use the same, beefy UNIX™ computer for every MCV workstation. Competitive hardware is inconsistent, and often, downright incompatible.*

# OUR RESOURCES VS. THEIR RESOURCES.

Metheus-Computervision. *If CAE companies were hamburgers, this is roughly what the combined resources of Metheus and Computervision would look like. Estimated annual sales (1984): Over $500 million. Total installed base: $1.5 billion. Total assets (1983): $349 million.*

Daisy. *Estimated annual sales (1984): $80 million. Total installed base: approximately $102 million. Total assets (1983): about $44 million.*

Mentor. *Estimated annual sales (1984): $80 million. Total installed base: approximately $108 million. Total assets (1983): about $24 million.*

Valid. *Estimated annual sales (1984): $48 million. Total installed base: approximately $67 million. Total assets (1983): about $43 million.*

*Sources for Daisy, Mentor and Valid financial and service information: corporate annual reports and widely available industry statistics.*

# MCV WORKSTATIONS ARE OPEN TO NEW ADDITIONS.

*MCV design tools are as easily upgradeable as this familiar example. Start with any workstation and simply add on.*

*"Want a cheeseburger? Just add cheese." Metheus-Computervision uses the same basic concept, for both software and performance upgrades.*

*Our extra ingredients aren't quite as inexpensive as these. But they're a lot less than the cost of a whole new workstation.*

# COMPETITIVE WORKSTATIONS ARE CLOSED TO THE IDEA.

*The typical competitive workstation is essentially a closed box. Or shall we say, a closed burger?*

*"Want to add cheese? Sorry, you'll have to buy a whole cheeseburger." That's roughly what happens with other workstations.*

*Starting over every time isn't too bad if you're talking hamburgers. If you're talking workstations, it's quite a bit to swallow.*

## THE FLEXIBILITY PRINCIPLE

# MAKE THE PRODUCT EASILY UPGRADEABLE.

### TASK OR PERFORMANCE UPGRADES: AS EASY AS ADDING CHEESE.

From the beginning, our workstations have been designed around a kind of "universal open box" concept. No matter which MCV workstation you start with, you can easily add task or performance upgrades as they come along.

By contrast, competitive workstations use what is known as the "closed box" approach. They do just fine with a single application area, like gate array or logic design. But if you hope to use those boxes for something other than the original task, good luck. The same is true for performance upgrades. You're pretty much stuck with whatever power your workstation started with. Since horsepower improvements have become a regular occurrence in the computer industry, a closed box can quickly become a white elephant.

For example, suppose a higher performance microprocessor comes along. With competitors, you either buy their latest workstation, or watch the world pass you by.

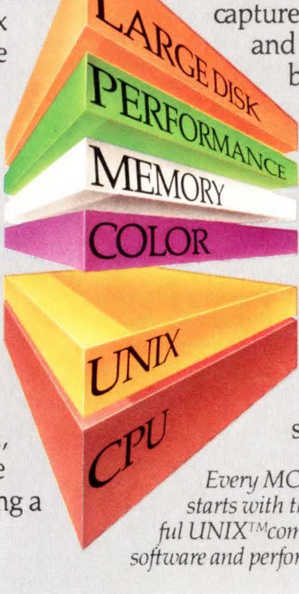
But if your workstation is from Metheus-Computervision, the situation is much more palatable. Instead of buying a whole new system, you make a simple board change, add the latest applicable software, and you're right up with the state of the art.

You can start as basic as you want. For example, let's say you begin with a Metheus-Computervision Schematic Entry system, for $39,900. Want to add complete full-custom design capability? Just buy our full-custom layout software and hardware upgrade package.

You now have the fastest, friendliest, most capable full-custom workstation you can get from anybody. In fact, it's just as good as buying a brand new MCV full-custom system.

And the added price? About $54,400. Considerably less than the roughly $145,000 extra you'd have to pay if you'd started with a Brand X schematic capture system and then had to buy a whole new workstation.

Want the same basic engine to do complete logic design? Just add MCV software and the hardware upgrade package for about $32,700. Somewhat better than spending $85,000 or more for a whole new logic design system.




*Every MCV workstation starts with the same, powerful UNIX™ computer. Just add software and performance options.*

### PRETTY SOON, EVERYBODY WILL BE TRYING IT.

The idea of an open, upwardly compatible workstation seems to have struck our competitors as a good idea. At least, it has recently.

"Fully upgradeable," they're starting to say.

Unfortunately, saying it is quite a bit easier than actually doing it. We suggest you ask a few, potentially embarrassing questions:

1) "If I buy this system from you today and want it to do (you name it) tomorrow, what exactly do I add? What will it cost? Will it work exactly as well as a new workstation?"

2) "Does all of your software run on all of your hardware? Easily? How about a demonstration?"

3) "What about performance upgrades? What are my options right now, and what do they cost? What kinds of upgrades will be available for this workstation in the future?"

These questions may cause your friendly workstation representative some momentary discomfort. But they'll help you avoid severe indigestion later on.

METHEUS-COMPUTERVISION

*tomatic Gate Array:*
*out $145,000.*

*Full-Custom: About $145,000.*

## ADD THE LETTUCE AND TOMATO: MCV LOGIC DESIGN SYSTEMS.

*Complete logic design and simulation capabilities for PCB or semi-custom and full-custom IC designs.*

• All the Schematic Entry software listed above, plus: • HILO-2™simulation. • Timing analysis. • Functional and gate level simulation. • Fault simulation. • Simulation waveform grapher. • Basic HILO symbol library. • TTL libraries (optional). • Automatic test generation (optional). • Symbol and simulation libraries for gate array and standard cell design (optional). • 8 bit planes. • 2 MB of memory. • 66 MB of disk storage. • RS-232, GPIB, RS-422 ports. • Support of Versatec and HP plotters.

## ADD THE BACON AND ONION: MCV SEMI-CUSTOM IC DESIGN SYSTEM.

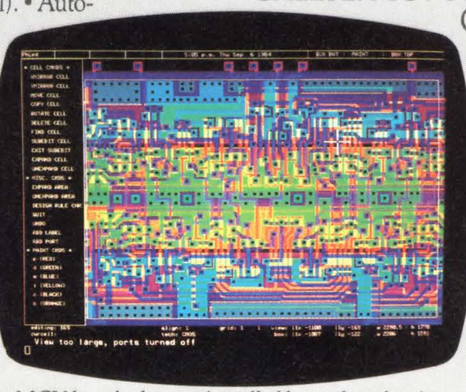
*Complete design, simulation and interface for gate array and standard cell IC design.*

• The Logic Design System, plus: • Symbol and simulation libraries for gate array and standard cell design. • Soon to be available: interfaces to Automated Place and Route Packages.

## ADD EXTRA PATTIES AND CHEESE: MCV FULL-CUSTOM DESIGN SYSTEM.

*Complete full-custom design, simulation and layout system.*

• The Logic Design System, plus: • 16 bit planes of graphics. • Technology independent layout editor. • Interactive design rule checker. • Physical layout to schematic netlist verification. • Functional gate level simulation with HILO-2. • Switch level simulation. • Circuit level simulation with SPICE. • 90° and 45° design supported. • Circuit extraction from physical layout. • Interfaces to GDS II Stream, CADDS 2/VLSI, Apple 860 and CIF.



*MCV has the largest installed base of production-tested, full-custom design workstations.*

## FOR THE REALLY BIG APPETITE: MCV CADDS 2/VLSI MULTI-USER LAYOUT SYSTEM.

*A powerful IC layout system with multi-user capability and technology independence.*

• Multi-user workstation system (four maximum). • Technology independent: Supports bipolar, MOS, Analog, Digital, Hybrid, GaAs, Microwave. • Schematic capture. • All angle layout. • Circles and arcs. • Interactive design rule checking. • Electrical rules checking. • Interfaces to GDS I, GDS II Stream, Apple 860. • Broad plotter support. • Integrated circuit programming language.

METHEUS-COMPUTERVISION

*mi-Custom Design*
*em (with color):*
*out $80,900.*

*MCV Full-Custom Design System (with color): About $89,000.*

*MCV CADDS-2/VSLI Multi-User Layout System: About $270,000.*

# THE TYPICAL COMPETITIVE MENU.

*Schematic Entry (monochrome): About $54,000.*

*Logic Design: About $85,000.*

*Semi-Au*
*Al*

## THE PRODUCT LINE PRINCIPLE

# OFFER SOMETHING FOR EVERYONE.

### THE BASIC BURGER: MCV GRAPHIC DEVELOPMENT SYSTEM.

*A powerful 32 bit dual processor computational engine with high resolution color graphics.*

• High resolution color graphics: 1024 x 768 pixel resolutions, 33hz interlaced, with 8 bit planes of graphics memory, upgradeable to 24 bit planes. • Dual 32 bit CPU with additional 32 bit Graphics Processor. • UNIX™ operating system with Berkeley extensions. • Battery backup for data protection. • True virtual memory. • 1 MB memory, upgradeable to 4 MB. • 33 MB disk storage, upgradeable to 66 MB. • 1 MB floppy disk. • 6 RS-232C ports for additional terminals. • 1 Versatec Printer/Plotter port. • Autodial 300 baud diagnostic modem. • Multibus. • Floating Point processor. • Programming languages include "C", with Fortran 77, Pascal and Lisp optional. • Ethernet™ • Full support for all Metheus-Computervision CAE software packages. • Optional mass storage up to 840 MB.

### ADD CHEESE: MCV SCHEMATIC ENTRY SYSTEM.

*Low cost basic design system for PCB and IC design applications.*

• 4 bit planes standard. • Multi-window. • Multi-page support. • Busses and bundles. • Off page connectors. • Drag or pre-position symbol entry. • Rubber band entry with automatic routing of signals. • User definable menus. • Versatile property attributes. • Supports functional, logic and circuit level designs. • Supports digital and analog design. • Adjustable text height and orientation. • User definable grid and snap. • Borders, titles and revision block support for A through D size drawings. • Industry standard netlist interface support.

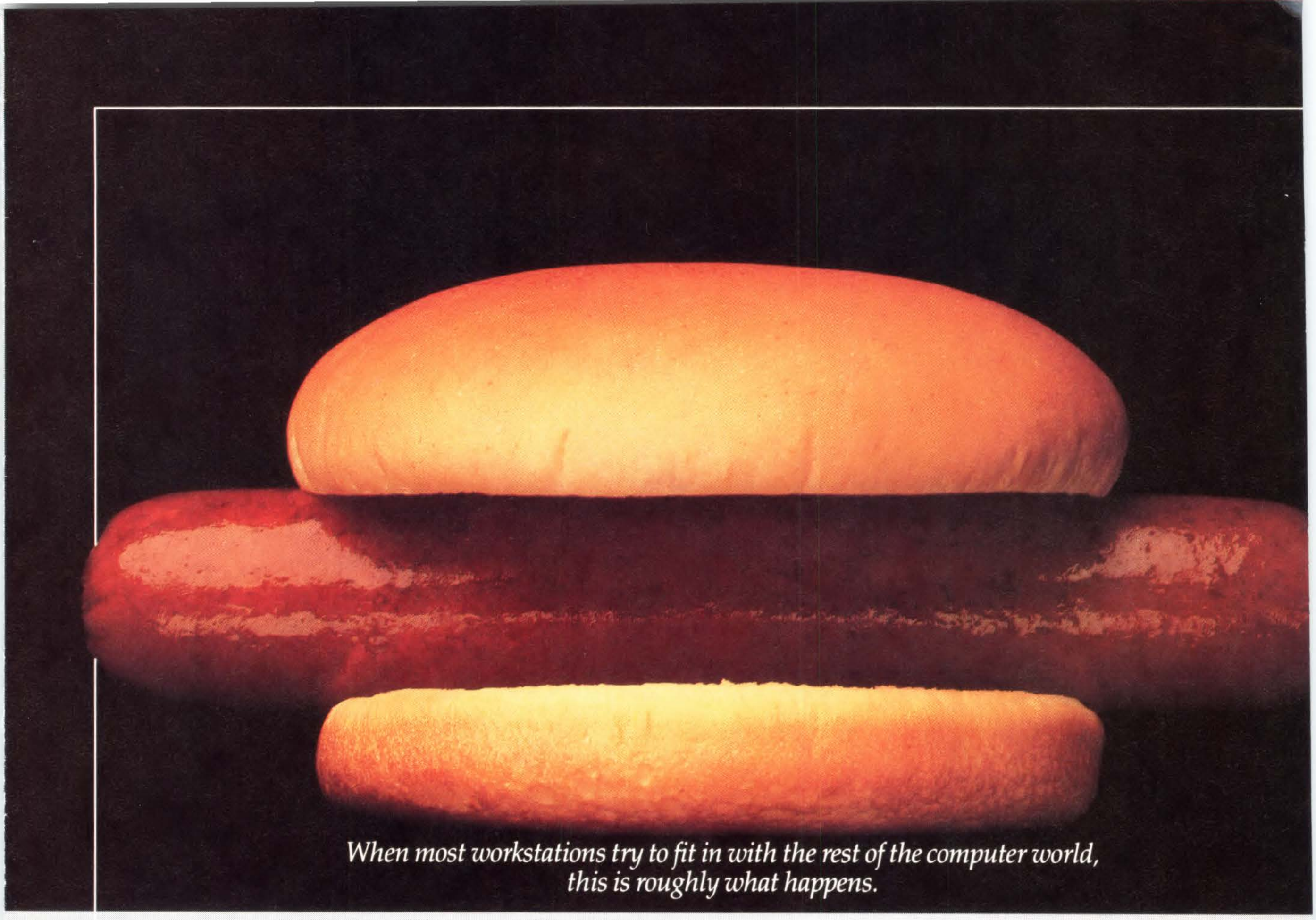
# THE METHEUS-COMPUTERVISION MENU.

*MCV Graphic Development System (with color): About $42,900.*

*MCV Schematic Entry System (with color): About $39,900.*

*MCV Logic Design System (with color): About $75,900.*

*MCV Se*
*Syst*
*A*



*When most workstations try to fit in with the rest of the computer world, this is roughly what happens.*

THE INTERFACE PRINCIPLE

# AVOID THE HAZARDS OF INCOMPATIBILITY.

## THE UNIQUE PROBLEMS OF BEING TOO UNIQUE.

A lot of engineering workstations have been designed as islands unto themselves. They do a fine job in isolation. But can they communicate with your mainframe?

The answer is usually no. The reason is that these workstations were designed around some rather unique standards: unique operating systems, unique networking, unique languages.

So they simply can't communicate well with the rest of the computer world. Which means, for example, you can't ship off a big number-crunching operation to the VAX,™ then get it back and continue on the workstation.

To solve the problem, one vendor offers you what they call a hardware accelerator. The price? They can get you into one for a mere $100,000 or so. In other words, they're asking you to pay the price for their workstation's inability to be compatible with the mainframe you've already paid for.

A lot to ask, we think.

## THE COMFORT OF WIDELY ACCEPTED STANDARDS.

From the beginning, we've built our workstations around the standards that are squarely in the center of the mainstream: UNIX,™ TCP/IP Ethernet,™ MC 68000's, HILO-2,™ SPICE, Multibus, Fortran, Pascal and C languages, and IEEE Floating Point, for example. A familiar bunch.

The benefits to you? We could go on and on.

For example: Ethernet allows you to use the power of your mainframe to do things like simulation. Just send the design to your VAX then back to the workstation. They all speak the same basic language.

Or take operating systems. Right now there are over

*Widely accepted standards allow for a much more efficient interface, as in the example above.*

400,000 engineers who earned their spurs on UNIX.

Which suggests it will be very easy to recruit and train engineers on a UNIX-based system. It also means that a wealth of UNIX software will run easily on your workstations.

Apollo-based marketers have tried to rectify the useability problems inherent in their AEGIS operating system by putting "UNIX-like" commands on top of the original system. A commendable step. But when it comes to custom-tweaking your system after it's installed, a true UNIX operating system will be a lot easier to deal with than one that's really an AEGIS system in disguise.

For any company that prefers the security of the mainstream, true UNIX is a pretty safe place to be. After all, how many AEGIS trade shows have you ever heard of?

## RING AROUND THE BUILDING?

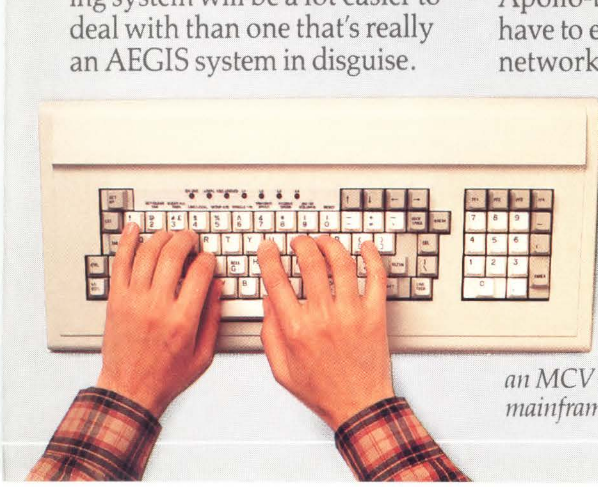
Another interesting issue is networking. Apollo-based workstations use the Cambridge ring network. It allows a circle of Apollo-based workstations to talk to each other.

What it doesn't do is communicate well with host computers like VAX or IBM. That will mean companies with Apollo-based workstations will have to eventually manage two networks: Ethernet and the ring network.

What will life be like under those conditions? You'll have two cables going around the building. You'll have the exciting challenge of cabling and managing two different sets of I/O lines.

Every time you buy a new computer, you'll have to decide which interface to use. Then you'll have the ongoing problem of managing two different interfaces for all your computers. When you try to go from one network to another, you're likely to face bandwidth discrepancies, which will cause a significant slowdown as you go through gateways, from one network to another.

But with an MCV workstation, you can take Ethernet to any of our other workstations, or to a VAX. As Ethernet becomes further enhanced, a Metheus-Computervision workstation will be able to take advantage of the refinements. So instead of your communications slowing down over the years, they'll keep getting faster.



*A few simple keystrokes can send your design from an MCV workstation to your mainframe. Thanks to Ethernet.*

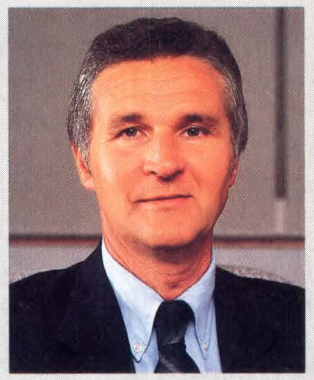
METHEUS-COMPUTERVISION

# THE PRINCIPALS BEHIND OUR PRINCIPLES.

For the foreseeable future, virtually all CAE competitors will be lacking at least one of the essential elements most customers are looking for: proven financial stability; proven, worldwide service backup; and a proven product.

But there is now a reassuring alternative to those companies: Metheus-Computervision.

*Jim Towne, President and CEO, Metheus-Computervision.*



*Jim Berrett, President and CEO, Computervision Corporation.*

Jim Towne, MCV President (and former President of Microsoft) puts it succinctly: "We can now beat the other CAE pioneers with our financial and service strength. And our experience beats the other big companies who are just getting into the market."

With this rather powerful combination, Metheus-Computervision will not be timid: "We have aggressive intentions for the electrical CAE marketplace," says Jim Berrett, Computervision President and CEO. "Our joint venture with Metheus makes an ideal fit."

But MCV represents more than just strong fundamentals and an aggressive marketing plan. We're a company that, from the beginning, has planned for the long haul. What we give you is faster total productivity, not just blinding speed on a few, isolated functions.

Of course, everybody promises you that. But the best way to judge promises is to see how well these companies have delivered in the past. Are they good long-term thinkers or just hard-charging marketers?

We suggest there's only one company that's been committed to a fully integrated, compatible, upgradeable line of design tools ever since the first news release. So maybe the company that's done the best job preparing for the future is the best company to spend the future with.

METHEUS-COMPUTERVISION



Metheus-CV, Inc., P. O. Box 959, Hillsboro, Oregon 97124. (503) 640-3311.

# ROCKWELL SEMICONDUCTOR TECHNOLOGY ACCELERATES DELIVERY OF CMOS ROMS.

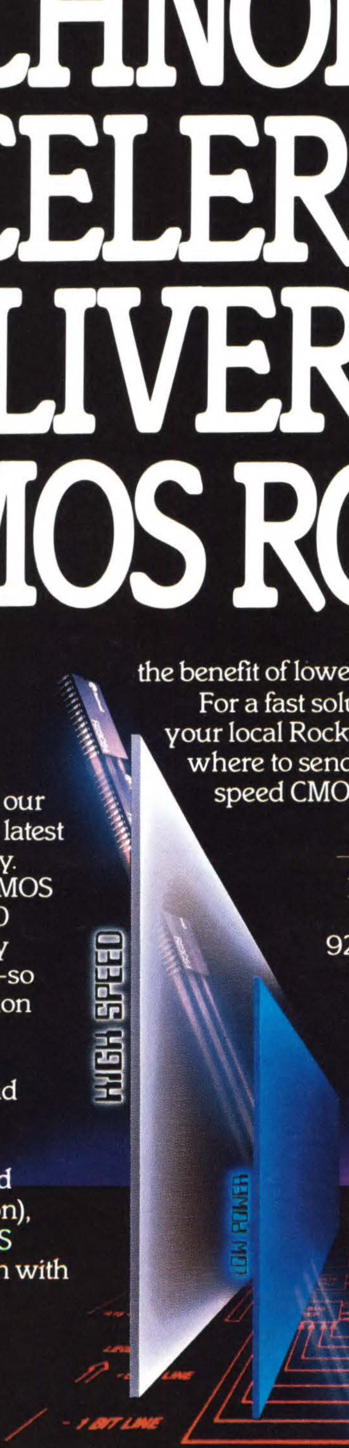
**Rockwell's R23C64 CMOS Static ROM is right on time for your portable equipment applications.**

Rockwell International is in production and accepting codes now for our R23C64 CMOS memory—one of the latest members of our CMOS product family.

This mask-programmable 64K CMOS ROM has an access time as fast as 150 ns, yet power dissipation is extremely low—10mW active, 50µW passive—so it's ideal for your low-power application requirements.

And with our 24-hour code-approval process and competitive lead times, you get high-speed CMOS without a lot of waiting.

In addition, the R23C64 is housed in a 28-pin JEDEC standard (B version), so it's pin-compatible with 64K CMOS EPROMs—allowing for easy transition with the benefit of lower power and higher speed.




For a fast solution to your low-power requirements, call your local Rockwell sales representative today. He'll tell you where to send codes and how to order low-power, high-speed CMOS memories now from—

**Rockwell Semiconductor Products Division**

Rockwell International, P.O. Box C, MS 501-300, Newport Beach, CA 92660. Call Toll Free (800) 854-8099. In California, (800) 422-4230.

**Rockwell International**

...where science gets down to business

CIRCLE 12

# U.S. MEETINGS

**Globecom '84, Nov. 26–29.** Atlanta Hilton Hotel, Atlanta, Ga. John Freight, Globecom '84, Scientific-Atlanta Inc., PO Box 105600, Atlanta, Ga. 30348; (404) 441-4800.

**30th Annual Conference on Magnetism and Magnetic Materials, Nov. 27–30.** Town and Country Hotel, San Diego, Calif. Ms. Diane Suiters, Courtesy Associates, 655 15th St. NW, Washington, D.C. 20005; (202) 347-5900.

**The Power Sources Conference, Nov. 27–29.** Sheraton-Boston Hotel and Hynes Auditorium, Boston, Mass. The Power Sources Conference Inc., 3970 Atlantic Ave., Suite 204, Long Beach, Calif. 90807; (213) 414-4412.

**Robots West, Nov. 27–30.** Anaheim Convention Center, Anaheim, Calif. Robot Institute of America, PO Box 1366, Dearborn, Mich. 48121; (313) 271-7800.

**Digital Avionics Systems Conference (6th DASC), Dec. 3–6.** Baltimore Convention Center, Baltimore, Md. AIAA, 1633 Broadway, N.Y. 10019; (212) 581-4300.

**Real-Time Systems Symposium, Dec. 4–6.** Hyatt Regency Hotel, Austin, Texas. Miroslaw Malek, Department of Electrical Engineering, University of Texas, Austin, Texas 78712; (512) 471-5704.

**Western Design Engineering Show, Dec. 4–6.** Moscone Center, San Francisco, Calif. Western Design Engineering Show, 999 Summer St., Stamford, Conn. 06905; (203) 964-8287.

**The First Conference on Artificial Intelligence Applications, Dec. 5–7.** Sheraton, Denver Tech Center, Denver, Colo. Conference on Aritificial Intelligence Applications, PO Box 639, Silver Spring, Md. 20901; (301) 389-8142.

**1984 IEEE International Electron Devices Society (IEDM), Dec. 9–12.** San Francisco Hilton and Towers, San Francisco, Calif. Melissa Widerkehr, Courtesy Associates Inc., 655 15th St. NW, Suite 300, Washington, D.C. 20005; (202) 347-5900.

**Computer Networking Symposium, Dec. 10–11.** Gaithersburg, Md. Robert Rosenthal, NBS, B226 Technology Building, Gaithersburg, Md. 20899; (301) 921-3516.

**Dexpo West '84, Dec. 11–14.** Disneyland Hotel, Anaheim, Calif. Expoconsul International Inc., 55 Princeton-Hightstown Road, Princeton Junction, N.J. 08550; (609) 799-1661.

**IEEE First International Conference on Office Automation, Dec. 17–19.** New Orleans Hilton, New Orleans, La. IEEE First International Conference on Office Automation, c/o Dr. Donald Kraft, Department of Computer Science, Louisiana State University, Baton Rouge, La. 70803; (504) 388-1495.

**1985 International Winter Consumer Electronics Show, Jan. 5–8.** Las Vegas, Nev. Dennis Corcoran, CES, 2001 Eye St. NW, Washington, D.C. 20006; (202) 457-8700.

**PC Fab Expo '85, Jan. 8–10.** Sheraton Twin Towers Hotel, Orlando, Fla. Julia Wilson, PMS Industries, 1790 Hembree Road, Alpharetta, Ga. 30201: (404) 475-1818.

**Automated Test Equipment West Conference (ATE), Jan. 14–17.** Anaheim Convention Center, Anaheim, Calif. Morgan-Grampian Expositions Group, 2 Park Ave., New York, N.Y. 10016; (212) 340-9780.

**1985 Measurement Science Conference, Jan. 17–18.** Marriott Hotel, Santa Clara, Calif. Darlene Diven, Lockheed Missiles and Space Co., PO Box 3504, Sunnyvale, Calif. 94088; (408) 756-0270.

**Uniform, Jan. 21–25.** Infomart, Dallas, Texas. Pemco, Inc., 2400 E. Devon Ave., Suite 205, Des Plaines, Ill. 60018; (800) 323-5155.

**1985 Society for Computer Simulation (SCS) Multiconference, Jan. 24–26.** Bahia Hotel, San Diego, Calif. SCS, PO Box 2228, La Jolla, Calif. 94038; (619) 459-3888.

**Communication Networks Conference and Exposition, Jan. 28–31.** Washington Convention Center, Washington, D.C. Louise Myerow, CW/Conference Management Group, 375 Cochituate Road, PO Box 880, Farmingham, Mass. 01701; (617) 879-0700 or (800) 225-4698.

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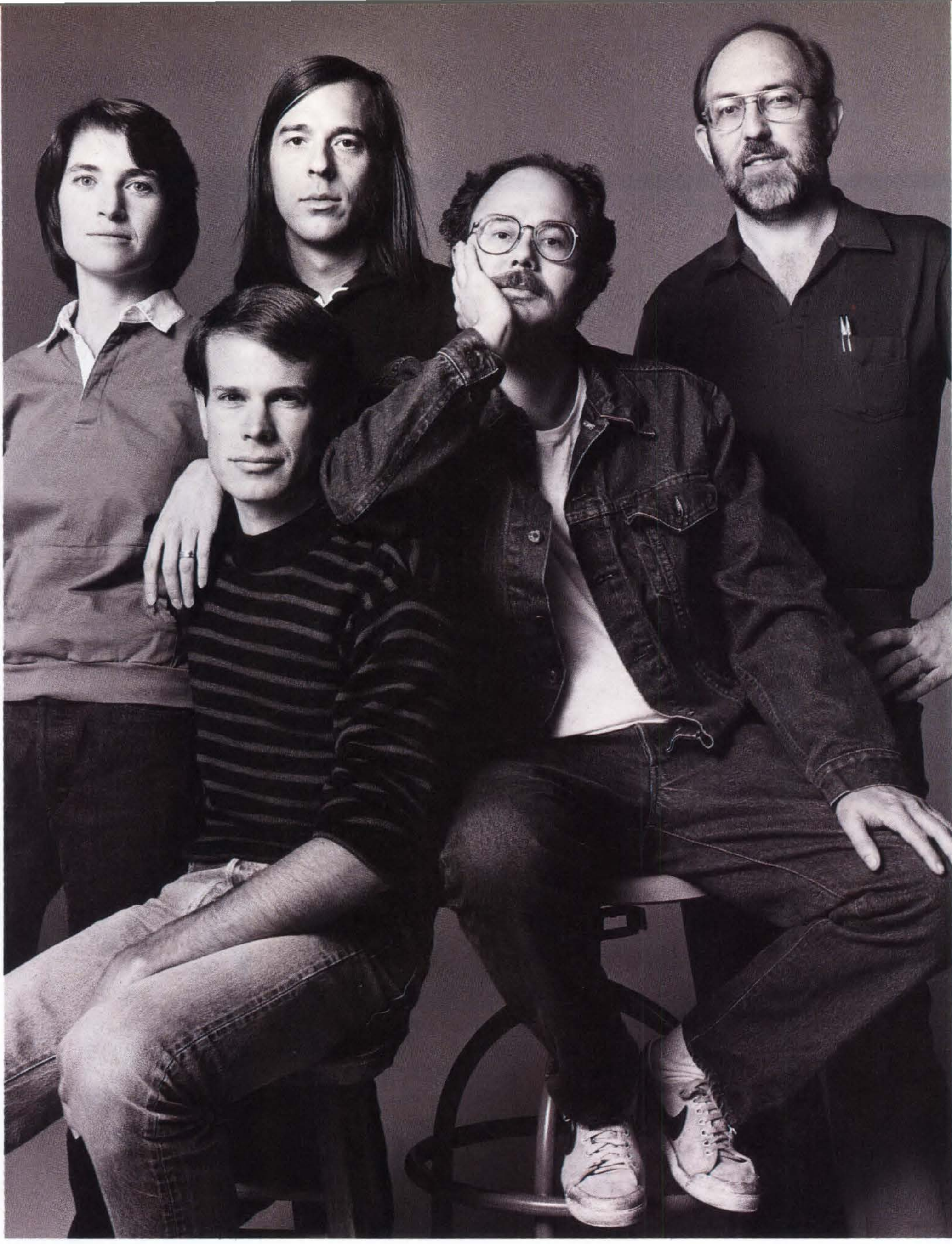


*The Pascal-2 system is available on Digital's VAX, MicroVAX; PDP-11/RSX, RSTS, RT-11, UNIX, TSX-Plus; and Professional Computer running P/OS, RT-11.*

# We put a lot of ourselves into Pascal-2. Put us to work on your VAX.

Everything we know about software development is built into Pascal-2. We created a straight-forward, robust compiler with rugged predictability that has already become a legend. Pascal-2 has proven its performance and its reliability in more than 2,000 installations in 36 countries.

## Pascal-2 on VAX

Now Pascal-2 can give you that same performance on the Digital Equipment Corporation's VAX, the premier software development computer system.

Pascal-2 provides the strength and flexibility essential for real utility in scientific, engineering, business, and industrial applications.

Using the advanced capabilities of this optimizing compiler, your development cycle will be shorter and your applications more efficient.

Pascal-2 is the only language compiler that provides a uniform development environment across the full line of Digital systems from the Professional 350 to the VAX. All versions of the compiler provide identical language features, with the same interface for the operating system and hardware, and the same set of language extensions.

## Portability

As a result, your application can be moved easily from one environment to another.

The Pascal-2 System Development Package for the Digital VAX and MicroVAX includes an optimizing Pascal compiler; an interactive, source-level Debugger; a Profiler that pinpoints execution bottlenecks; and other utilities to aid program development.

If you would like to put Pascal-2 to work on your VAX, call us at 1-800-874-8501.

**Oregon Software**

6915 S.W. Macadam Avenue
Portland, Oregon 97219



**CIRCLE 15**

## U.S. MEETINGS

*(continued from p. 29)*

**Mini/Micro West, Feb. 5–7.** Anaheim Hilton Exposition Center, Anaheim, Calif. Electronics Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

**Conference on Optical Fiber Communication(OFC '85), Feb. 11–13.** Town and Country Hotel, San Diego, Calif. Optical Society of America, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.

**IEEE International Solid-State Circuits Conference, Feb. 13–15.** New York Hilton Hotel, New York, N.Y. Lewis Winner, ISSCC, 301 Almeria, Coral Gables, Fla. 33134; (305) 446-8393.

**Integrated Machine Loading/Material Handling Systems Seminar, Feb. 19–21.** Holiday Inn Livonia-West, Detroit, Mich. John R. McEachran, SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, Ext. 382.

**Automated Design and Engineering for Electronics Conference and Exhibition (ADEE), Feb 26–28.** Anaheim Hilton and Towers, Anaheim, Calif. Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Ave., PO Box 5060, Des Plaines, Ill. 60018; (312) 299-9311.

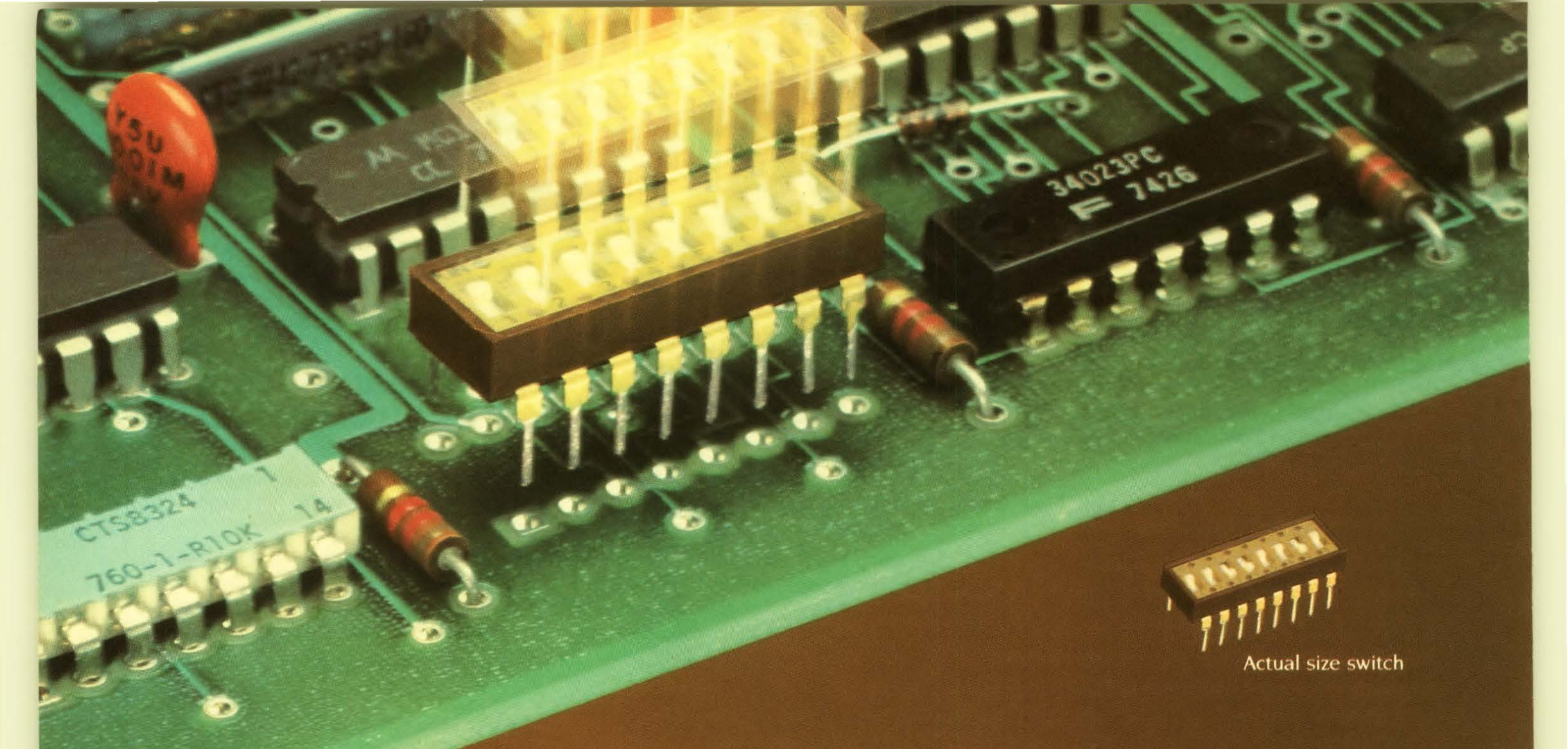
**American Institute for Design and Drafting (AIDD) Exposition, March 3–8.** Albert Thomas Convention Center, Houston, Texas. Philip Nowers, AIDD National Headquarters, 901 N. Washington St., Suite 509, Alexandria, Va. 22314; (703) 548-1263.

**Interface '85, March 4–7.** Georgia World Congress Center, Atlanta, Ga. The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

**Integrated Services Digital Networks Exposition (ISDN '85), March 6–8.** Bally's Park Place Casino Hotel, Atlantic City, N.J. Joan Barry, Information Gatekeepers Inc., 214 Harvard Ave., Boston, Mass. 02134; (617) 232-3111.

**Southcon '85 and Mini/Micro Southeast, March 5–7.** Georgia World Congress Center, Atlanta, Ga. Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

**Winter '85, March 13–15.** Hyatt Lake Tahoe, Incline Village, Nev. Optical Society of America, Picosecond Electronics and Optoelectronics Meeting, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.


Actual size switch

# New! CTS AUTO-DIP™ Switches for AUTOMATIC INSERTION!

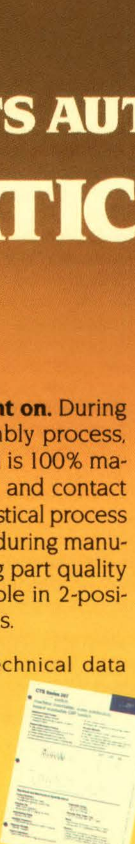
### You'll realize immediate cost savings in board production with the New CTS Series 207 AUTO-DIP™ Switch.

Because they are the same size as your IC's—these new Series 207 AUTO-DIP™ switches can be used in your automatic insertion equipment right along with IC's...without machine adjustment. You get economical high speed board production. You'll save significant board space as well! This new switch takes only 37% of the volume of a standard DIP switch allowing for closer board stacking and space savings.

**Wave solderable! Board washable!** The AUTO-DIP™ design eliminates bottom sealing. And, a lead frame housing construction with time-proven tape top seal keeps contaminants out of the switch through wave soldering and solvent or aqueous cleaning.

**Reliability you can count on.** During the fully automated assembly process, each Series 207 DIP Switch is 100% machine tested for continuity and contact resistance. In addition, statistical process control used in every step during manufacturing assures unvarying part quality and final reliability. Available in 2-position to 12-position switches.

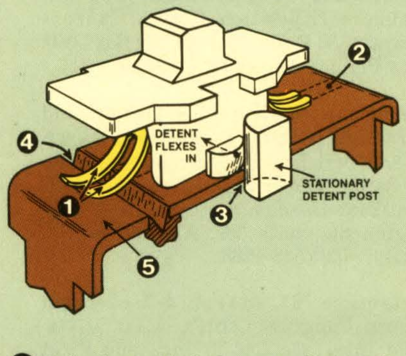
WRITE TODAY for full technical data on these new Series 207 AUTO-DIP™ switches.
Contact: CTS Corporation,*
Paso Robles Division,
Electromechanical Group,
500 Linne Road,
Paso Robles, CA 93446.
Phone: (805) 239-0427



*In Calif. dba CTS Electronics Corporation

**CIRCLE 17**

## Switch reliability that is the best ever!




1. Redundant gold inlaid contacts dramatically enhance contact reliability.
2. Positive wiping contacts assure low and consistent contact resistance. (.050" travel)
3. Detent function separated from contacts to optimize both designs.
4. Gold contacts never abraded or contaminated by sliding over polymer surfaces. Contacts never touch a nongold surface
5. No contactor deflection for the life of the switch. Constant contact force eliminates overstressing of contacts for greater reliability.

# CTS means Reliability

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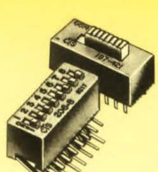
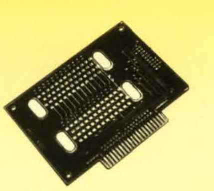


**Series 206RA & 197** Right angle and 4PDT slide actuated DIP switches.
Phone: (805) 238-0350
**CIRCLE 18**



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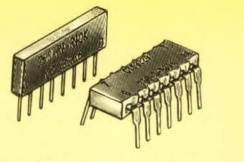
**CIRCLE 19**



**Series 750 & 760** Solid ceramic SIP and DIP resistor networks.
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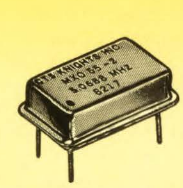
**CIRCLE 20**



**Series MX055** Low profile hybrid clock oscillators.
Phone: (815) 786-8411
**CIRCLE 21**

# PERSONALLY SPEAKING

## Now is the time for cutting back the length of the design cycle

The increasing complexity of circuits in silicon and the move toward application-specific VLSI chips deliver a message that is both loud and clear: Design times must be shortened. In some instances, the design cycle can stretch out as long as three years. And even though the latest engineering workstations often considerably curtail that cycle, there is still an urgent need for a unified data base that reaches from conception to the fully realized IC. What's more, today's techniques must be extensively revised to make the most of reusable circuit blocks that already exist as standard cells.

At present, the various phases of design—layout, simulation, and test pattern generation—work with separate data bases. Moving from one data base to another involves a time-consuming transition that is very error prone. In fact, translating the output of one program into another's input takes more time than running the entire program. Translation thus consumes a major portion of the design cycle, and the errors it introduces end up causing serious problems.

Data bases do exist that can be employed for design, but in most cases they are difficult to use, have low throughputs, and do not handle all of the attributes a designer must enter into a system.

A potential solution lies in using Lisp—the programming language of artificial intelligence—in conjunction with an advanced workstation. The language could define a set of specifications for, say, gate-level structures, timing behavior, and logic synthesis and possibly for laying out gate arrays and standard cells. Representations of the different aspects of the design process could be built into main memory as a single hierarchical data base, and all representations would check themselves against one another to ensure consistency.

Taking greater advantage of reusable circuit blocks in chip design also will truncate the overall design cycle. For years now, creating MOS devices with blocks of memory has been standard operating procedure. The time has come to turn to this approach when designing intrinsically more complex systems on a chip. Using standard cells over and over again will certainly simplify design and play a major role in boosting engineering productivity.

Further, reusable registers, ALUs, multiplexers, and core microprocessors—to name a few possibilities—make generating a test program far easier. The test vectors will already have been identified for a given block. From the test vectors for that or any other block, designers can extrapolate the test programs for the entire chip.

The handwriting is on the wall. Unless the design cycle is pruned back, engineering productivity will decline—a situation that is likely to get worse as devices grow more complex.



*Martin Gold*

# Our $2,000 CAD softwa

Task Force TIPS of Indiana needed to design an Automatic 50-350 GPM fire hose nozzle. They might have used a quarter million dollar computer-aided design system, but they used AutoCAD™ instead.

**Mainframe CAD capability at 5% of the price.**

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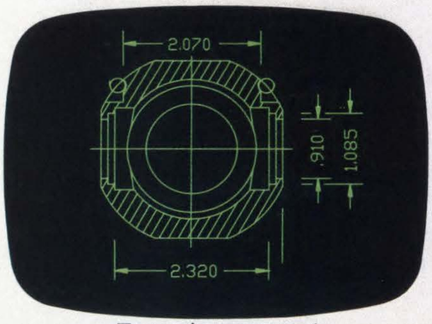
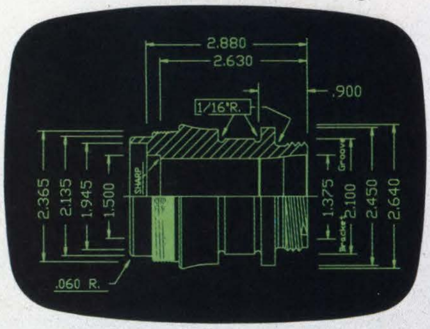



*Zoom in on a part to focus on the details*

*AutoCAD automatically dimensions distances and angles*




AutoCAD's editing facilities let you DRAW an object, ROTATE or SCALE it, DRAG it on the screen to any position, STORE it away in a parts library for recall in other drawings, FILL an area with any of our 38 defined patterns or your own, use an unlimited number of LAYERS like overlays in drafting, and automatically DIMENSION distances, angles, radii, and diameters with full ANSI standard dimensioning.

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The beauty of AutoCAD is that you need no prior knowledge of computers. Even if you've never seen a CAD system, you'll pick it up in a matter of days, and feel comfortable within a week.

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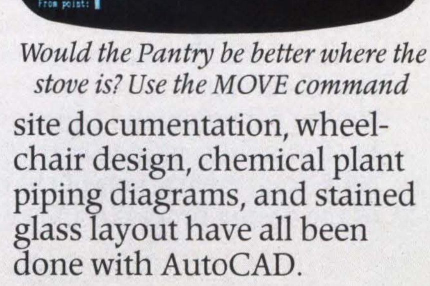
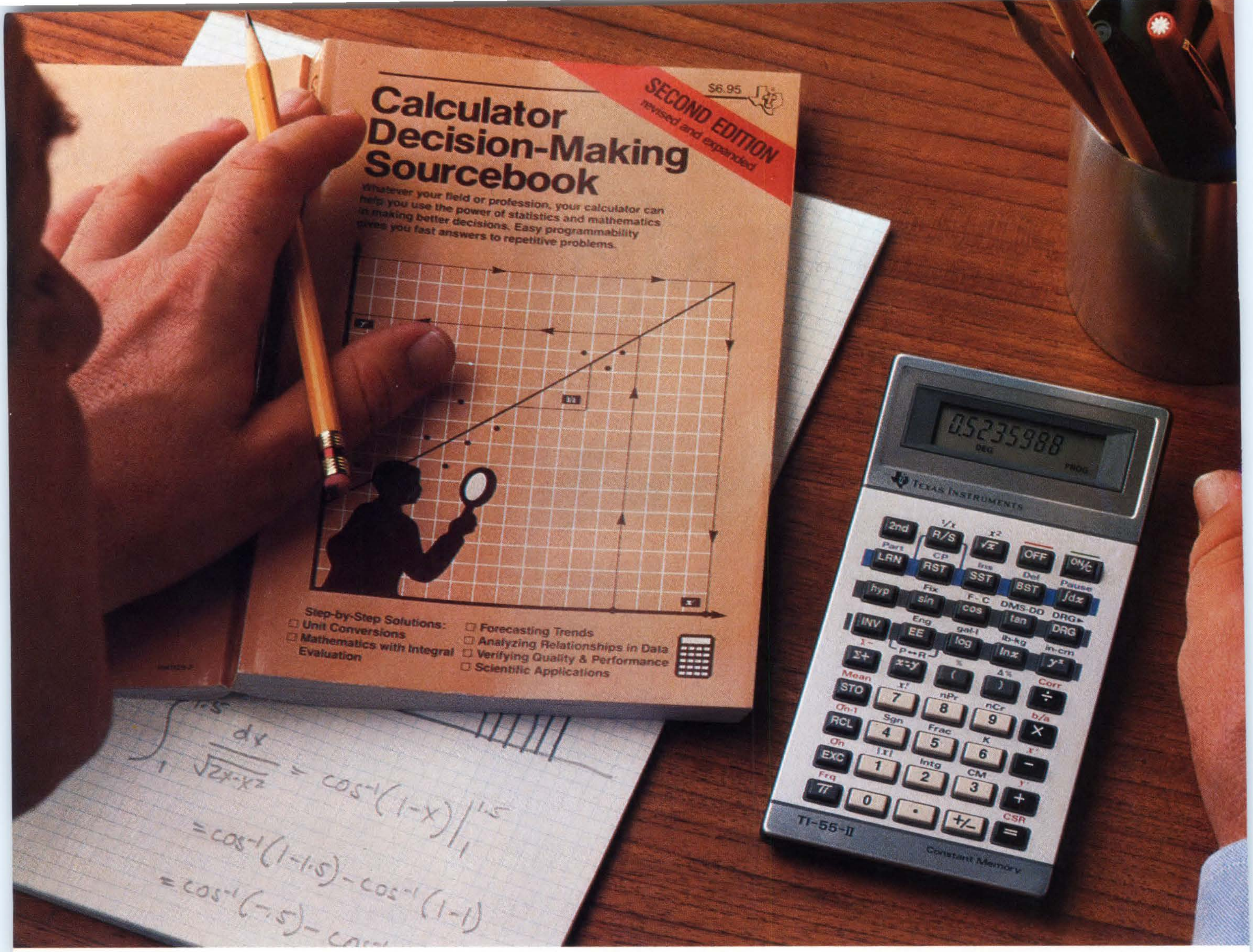
**Schematics, skyscrapers, and everything else.**

Since AutoCAD is general-purpose and user-customizable, it doesn't matter what type of drafting your work requires. Schematic design, building plans, PC board layout, archeological site documentation, wheelchair design, chemical plant piping diagrams, and stained glass layout have all been done with AutoCAD.




*Would the Pantry be better where the stove is? Use the MOVE command*

Architectural layout courtesy of Lansing Pugh, Architect  Solar Panel Assembly plot courtesy of Future Technology, Inc.




# How the TI-55-II makes short work of long problems.

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The TI-55-II also gives you enough programmability to eliminate a lot of repetitive key punching. Our Constant Memory™ keeps programs and data on tap, even when the calculator is turned off. So once you've entered a formula, you can simply put in the variables to get your solution. The Liquid Crystal Display shows your answers in standard, scientific or engineering notations — clearly and precisely.

We also help you get the most out of your calculator with the Calculator Decision-Making Sourcebook. It gives you step-by-step examples of the best techniques used for solving mathematical, scientific and statistical problems. And we've included a special section on how to program your TI-55-II.

So next time you're facing another time-consuming problem, cut it down to size with the TI-55-II.

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# NEWSPULSE

## Big ideas translate into high performance for VAX mini

Several design concepts usually reserved for large computer systems have been integrated in the VAX 8600 minicomputer, giving it more than four times the performance of the VAX-11/780. For instance, custom ECL gate arrays are partially responsible for a processor cycle time of 80 ns—2.5 times faster than the VAX-11/780. Second, four-stage pipelined processing reduces the number of cycles per instruction, and a 16-kbyte write-back cache cuts down on the time spent by the CPU accessing main memory. A floating-point accelerator and a dedicated memory bus further boost overall performance. According to Digital Equipment Corp. (Maynard, Mass.), a cluster of eight VAX 8600s equals the power of an IBM 3084 mainframe.

## Software halves test program development time

The link between designers and test engineers gets a lift from a software interface that translates the information gathered during circuit design into a test program, slashing the program development time by up to 50%. Engineers then use those programs for production tests or for debugging VLSI-based boards with guided probes. Jointly developed by Daisy Systems Corp. (Sunnyvale, Calif.) and Factron/Schlumberger (Billerica, Mass.), formerly Fairchild Subassembly Test Systems Division, the software enables Daisy workstation users to generate accurate simulation data—information that is critical to the test development process—and transfer it directly to Factron test equipment. The software interface package will be available next month.

## Processing scheme drops on-resistance for power MOSFETs

Fabricating power MOSFETs with the lowest drain-to-source on-resistance for a given unit area is the chief strength of a processing technique that has just come on the scene. Chips built with TMOS III, devised by Motorola Semiconductor Products Inc. (Phoenix, Ariz.), demonstrate an $R_{DS}$ (on) ranging from 0.08 to 0.10 Ω—roughly 20% better than industry standards. Further, the process packs 1 million cells/in.$^2$; typically, MOSFETs come in at about 400,000 cells/in.$^2$.

## Supercomputer's Cray-like architecture pays off in speed

Based on standard LSI circuits and semicustom CMOS gate arrays, a 64-bit supercomputer tackles about 60 million operations/s—about 25% the speed of a Cray 1 but at a tenth the cost. Much of that power is attributed to a vector-generating compiler and to the highly pipelined architecture, which itself is similar to the Cray 1's structure. The C-1 computer, which comes in at $500,000 or so, runs two compilers that optimize code for vector processing: a proprietary Fortran compiler running under Unix 4.2 BSD and a Fortran-77 compiler that works with VAX Fortran. The former one cuts run time significantly. The extensive CMOS circuitry permits an air-cooling scheme and allows the computer to take up only 7 ft$^2$ of floor space and dissipate only 3200 W.

**NEWSPULSE**

## Modeling language tackles four-state logic simulation

For the first time a behavioral modeling language will be able to work with four logic states—0,1,X, and three-state. Because the language, called Adlib, can propagate X or unknown states, it comes in handy for analyzing timing hazards and accurately simulating faults—two operations previously restricted to structural simulation models. Designed by Teradyne Inc. (Boston), the language creates a behavioral circuit that the company's Lasar-6 simulator can evaluate 30 to 50 times faster than it can the equivalent structural representation.

The modeling language is based on C, with hardware constructs added for parallel operations. From the behavioral circuit description, a compiler produces intermediate code that is then stored in the Lasar modeling library. During simulation and fault simulations, a special interpreter evaluates all behavioral segments of the simulation model.

The language, compiler, and interpreter all will be standard features of Lasar-6 by next spring. Adlib will also be accessible to Lasar-6 users who subscribe to Teradyne's software update service.

## CMOS successive-approximation register rivals bipolar speed

CMOS makes its impact in yet another chip, this time a successive-approximation register that carries all the storage and control circuitry needed for 12-bit successive-approximation analog-to-digital converters. The first CMOS equivalent of the bipolar 2504 register, it proves as fast as that chip but draws only 10 mA at 15 MHz and 8 $\mu$A on standby. Zytrex Inc. (Sunnyvale, Calif.) builds the CMOS chip with two metal interconnection layers and with metal gates. Besides its appropriateness for a-d converters, the chip can be put to work as a serial-to-parallel counter or as a ring counter for recursive algorithms.

## Surface-mounted packages continue to diversify

Driven by the considerable savings in board space, chip manufacturers of all types are increasingly turning their sights toward surface-mounted packages, both leaded and leadless. To wit, TRW Inc.'s Optoelectronics Division (El Segundo, Calif.) has developed some of the first surface-mounted optical couplers, each housed in a custom molded package 0.09 in. square and 0.07 in. high. Each component comprises a gallium arsenide LED and a silicon phototransistor, both coupled to a thick-film ceramic substrate.

Surface mounting is also moving into memories, primarily with the goal of trimming the board space of arrays. Mostek Corp. (Carrollton, Texas) is soon coming out with a 64-kbit dynamic RAM in a plastic leaded chip carrier that matches the footprint of a leadless ceramic carrier. As a result, it can substitute for ceramic packages. The plastic carrier conforms to the 18-lead JEDEC-approved outline—290 by 425 mils. Built with copper leadframes, it has excellent thermal properties.

## *Gould... Innovation and Quality in Logic Analyzers*

**The K105-D analyzer with Trace Control™ helps you find faults quickly and easily.**

For most engineers, the frustration is not in solving the problem. But in finding it.

Not anymore. Take the Gould K105-D logic analyzer. It can help you isolate errors and their causes quickly and easily. Because now you can capture and examine several possible cause areas with a single pass.

**Advanced program tracking and data capture.**

Flexibility is the key.

With 8 levels of Trace Control, you can follow every bend and turn in your program flow. No matter how complex. And capture widely-separated slices of code better than any other triggering method.

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This selective recording conserves memory. While it helps you get at the problem—and solve it—in less time than ever before.

**An analyzer that speaks your language.**

The K105-D speaks simple assembly language, not complex object code. Quite fluently, we might add.

With our disassembly modules for the 68000, 8086, 8080, 8085A and Z80® B microprocessors, you need only one analyzer for debugging most popular processors.

**Clear, concise pattern definitions.**

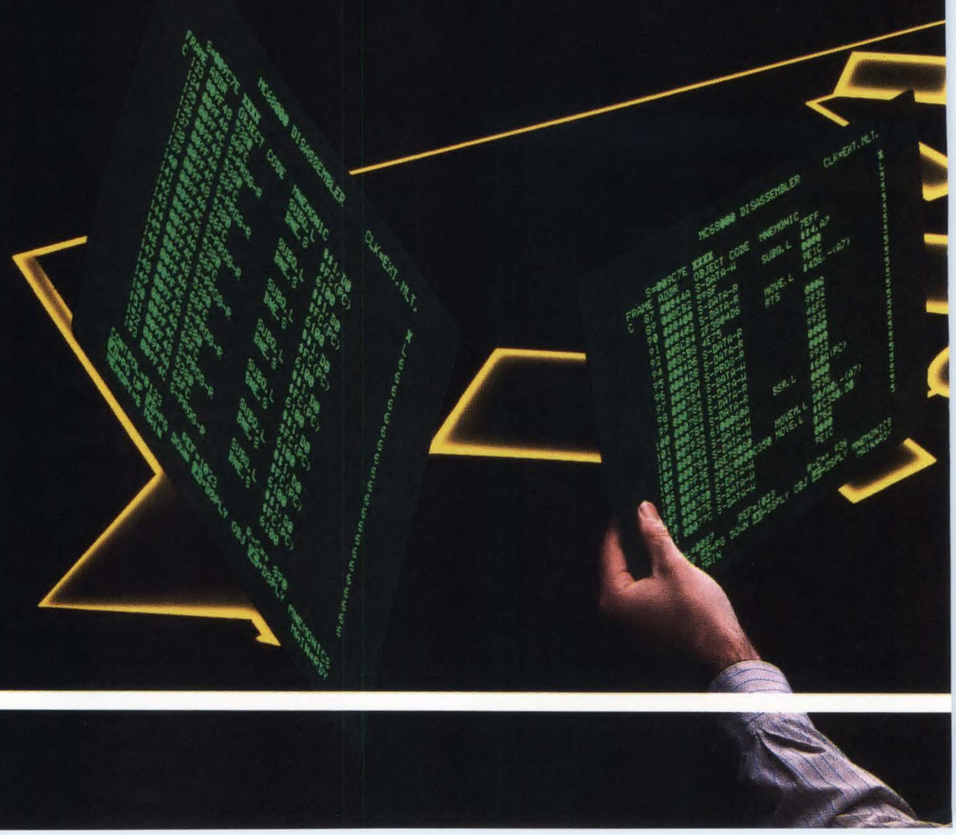
With the K105-D, you can define all your event patterns with symbolic labels. These labels can represent address locations, data values, fetched instructions or any control signal you're monitoring.

And since you create them, they're easier to understand and remember.

What's more, Trace Control uses English-like commands which make for shorter set-ups. Quicker comprehension. And a more productive engineer.

To make debugging even easier, add the optional dual floppy disk drive. With it, you can store up to 35 set-ups and associated recordings on a single diskette for instant recall.

# Now, capture up to 4 segments of complex program flow to pinpoint problems fast.



**You won't get caught in a loop.**

By using the K105-D's loop counter, you can follow a sequence of events for a specific number of iterations. Then stop at will.

It's a quick way for you to test the repeatability of a program function. And verify that your code is having the predicted effect.

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For the hard part (hardware/software integration), now there's a simpler solution. The K105-D's 100 MHz high speed link.

It's an extremely precise way to see how timing affects software execution. And vice-versa.

Again, for this task, Trace Control can help you track down hard-to-find faults. So you end up with a program that flows smoothly. Error free. In a fraction of the time it used to take.

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At Gould, we engineer every instrument to be clearly the best in its class.

So now with your insight and the K105-D analyzer, you can capture the problem. And solve it. Fast.

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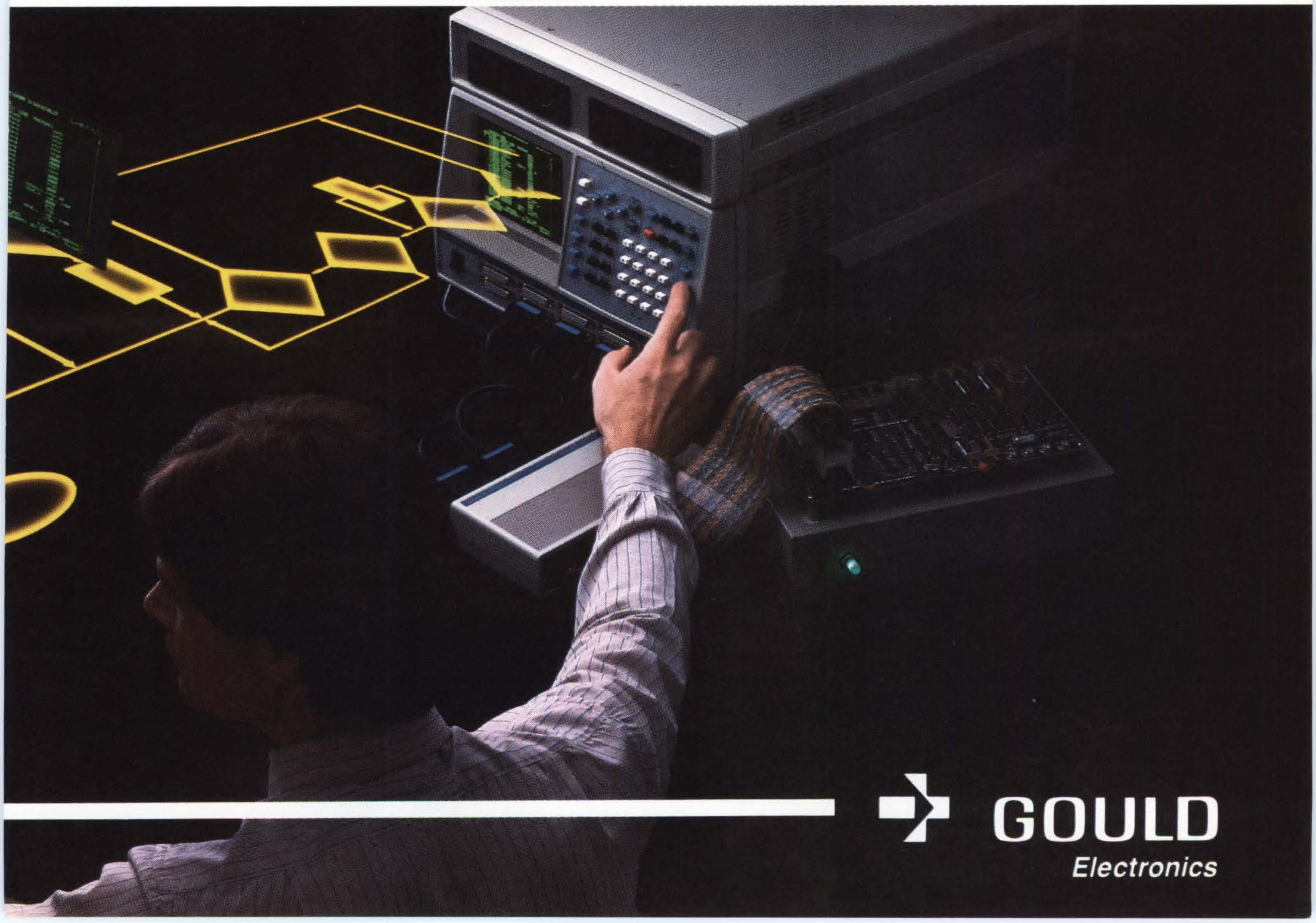
*The K105-D gives you two levels of HELP at the touch of a button. First, step-by-step operating instructions that appear along the bottom of the analyzer screen. Second, a menu that allows you to select more detailed "help" should you need it.*

 **CIRCLE 25**



# The HP 1630G Logic Analyzer for today's 16-bit designs.

# Hardware and software solutions design and test cycle.

With up to 65 channels of state analysis, the HP 1630G is the new standard for system design engineers working on complex new 16-bit microprocessor-based products. Plus, you can configure 8 of those lines for 100 MHz timing analysis to get a logic analyzer with investigative power and versatility for virtually all your needs.

## Three new software overview modes let you nonintrusively monitor software and hardware performance and interact in real time.

The HP 1630G significantly expands on the hardware and software performance capabilities already introduced in the HP 1630A/D family members. In addition to time histograms that show execution-time distribution, and label histograms that show address activity, the HP 1630G gives you three new modes: program flow, time positional, and linkage measurements. *Program flow measurement* lets you monitor program activity based strictly on opcode accesses. *Time positional measurement* lets you measure the number of occurrences of an event per unit time. *Linkage measurement* measures the relative frequency of the activity between specific modules.

## Time tagging gives you added insights into system functions.

In the state analysis mode, time tagging measures the time elapsed between each stored state. Make detailed absolute time measurements between states and known physical events. Or, use it to measure the total time from the trigger point to a particular state. Because time tagging is a single-pass activity, it is well-suited to helping you identify inline sections of code that take longer to execute than anticipated.

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HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

HP 1630D

HP 1630A

# throughout your 16-bit

### Floppy disc interface and popular 16-bit microprocessor support.

On-board non-volatile memory keeps one instrument setup and your current disassembler instantly available at power-up. For even greater storage, the HP 1630G features direct compatibility with a number of HP disc drives such as the HP 9121S/D (the HP 9121D is illustrated). In one convenient 3½″ floppy you can now store data, state listings, timing diagrams, alternate disassemblers, and instrument setup configurations. For added flexibility, the HP 1630G supports all popular 8-bit, as well as the following 16-bit microprocessors: 68008, 68000/68010, 8086, 8088, 80186/80188, 80286/80288, Z8001 and Z8002.

### Our HP 1630G upgrade kit protects your previous HP investment.

If you've already invested in an HP 1630A or HP 1630D, but you feel you need the added capabilities of the HP 1630G, an upgrade kit is available.

Compare the HP 1630G. At $12,100* it's even HP-IB programmable for fully automated measurements. To find out more about the HP 1630G or its companions, the HP 1630A/D, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

**CIRCLE 26**

*U.S.A. list price only.

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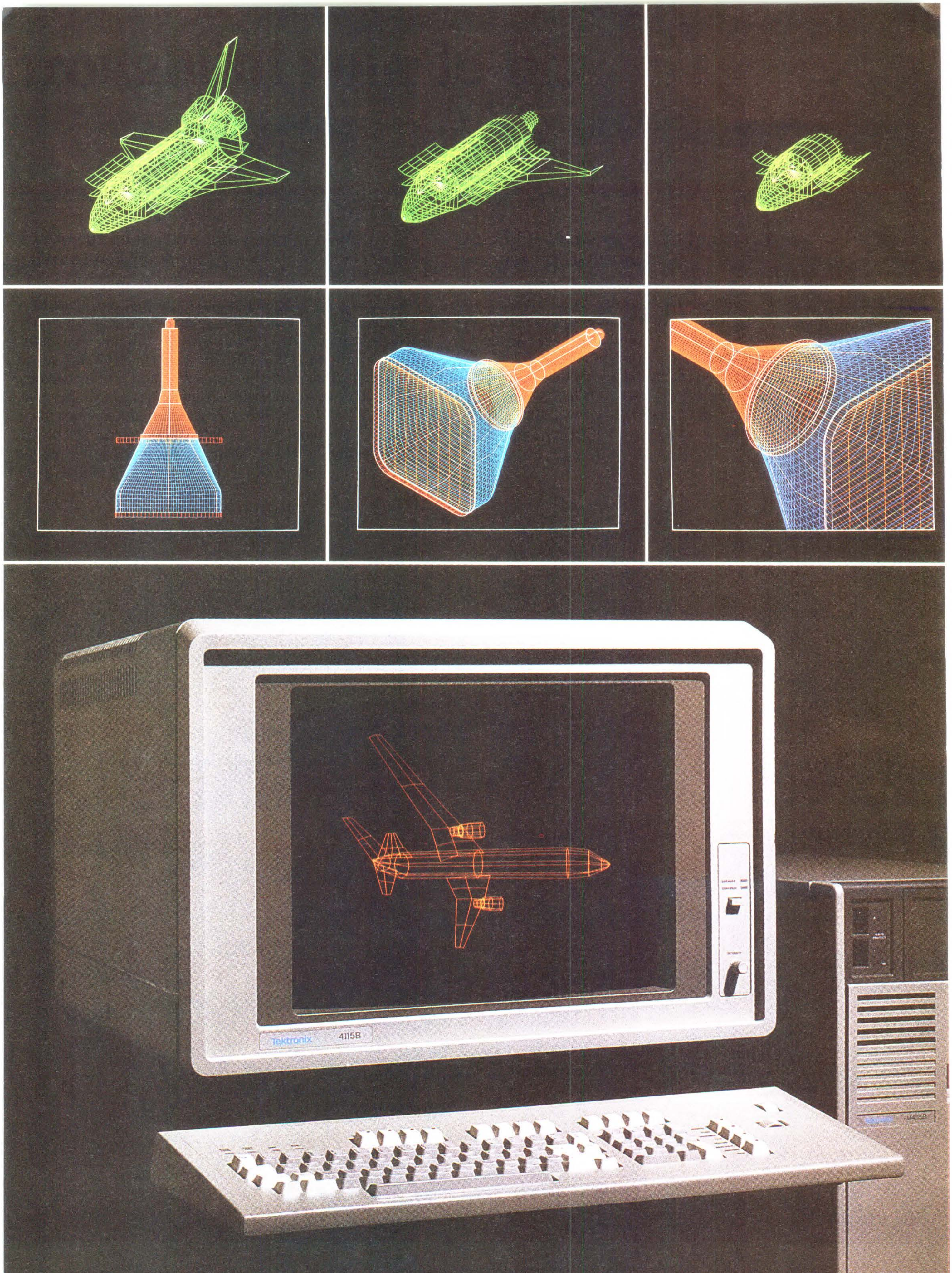
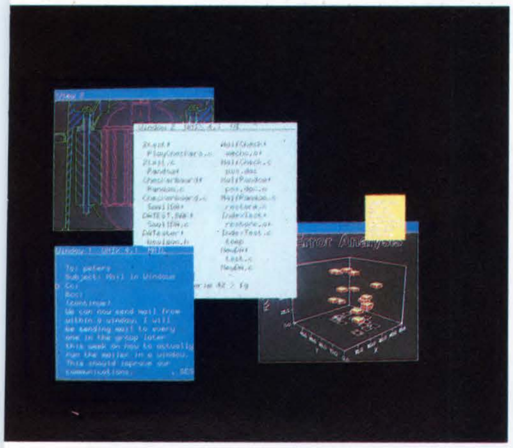

Tektronix
4115B
M4115B

# NOW TEK BRINGS YOU HIGH PRECISION 3-D FOR THE 4115B.

**Local control, real-life perspective and superb resolution bring high 3-D performance to the 4115B.** Known world-wide as the graphics standard, the 4115B is now even better—more powerful, more flexible, more productive because Tek has developed a complete 3-D wireframe enhancement package



Segment subroutines, segment editing, and friendly window management are all part of the new flexibility.

for the only terminal with patented AutoConvergence. And you can order it now for your new or existing 4115B.

No matter how complex your wireframe designs become, maximum resolution and true color will always be realized. Low eye fatigue and error minimization are benefits of the 4115B's superior clarity.

High resolution is matched by high interactivity. The 4115F58 enhancement is a user friendly 3-D tool that helps you build a productivity pathway to shaded surface modeling and the most advanced CAD applications.

**New processors, new firmware, new microcode, new keyboard with numeric pad provide powerful, yet well-known user methods that let you fully utilize all your existing 2-D commands.** And that means your current software and hardware investment is fully protected.

Users can actually mix 2-D and 3-D information on the screen at the same time... all with local zoom and pan. And while building 3-D data you'll maintain all standard 4115B functions for 2-D operation. Thus engineers working on one project can easily migrate to another or share terminals as needed for optimum productivity.

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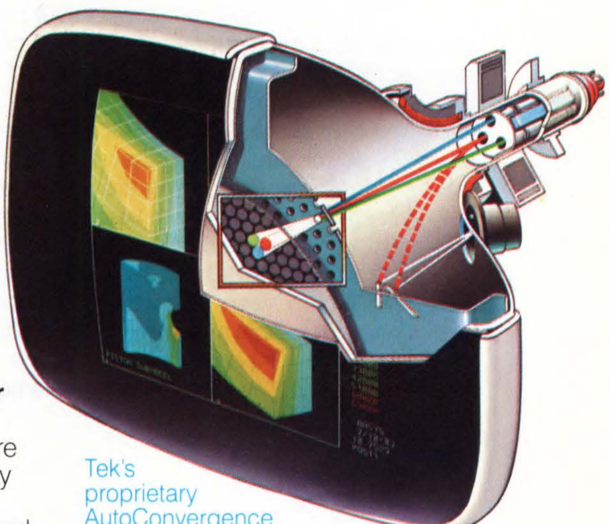
**Real-life perspective and true zoom and pan maximize**



Tek's proprietary AutoConvergence feature for the Tek 4115 achieves unmatched resolution.

**engineering precision achievable with previewing, intermediate views, and final part development.**

Whatever your application a few keystrokes are all that are required to fully manipulate viewing position. With 4115F58 you can rotate an object on horizontal, vertical or depth axes. Then with true zoom, pan and perspective you can view the displayed part, vehicle or system to see it just as you would in real life.

So if you want to start with the highest precision 3-D and work at your highest performance every day, call your Tek Sales Engineer. For literature or the location of your local Tek sales office, call toll-free 1-800-547-1512. In Oregon, 1-800-452-1877.

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CIRCLE 27

# THE SUCCESS OF YOUR MEMBRANE SWITCH DEPENDS ON ELECTRONIC RELIABILITY AND GRAPHICS EXCELLENCE.

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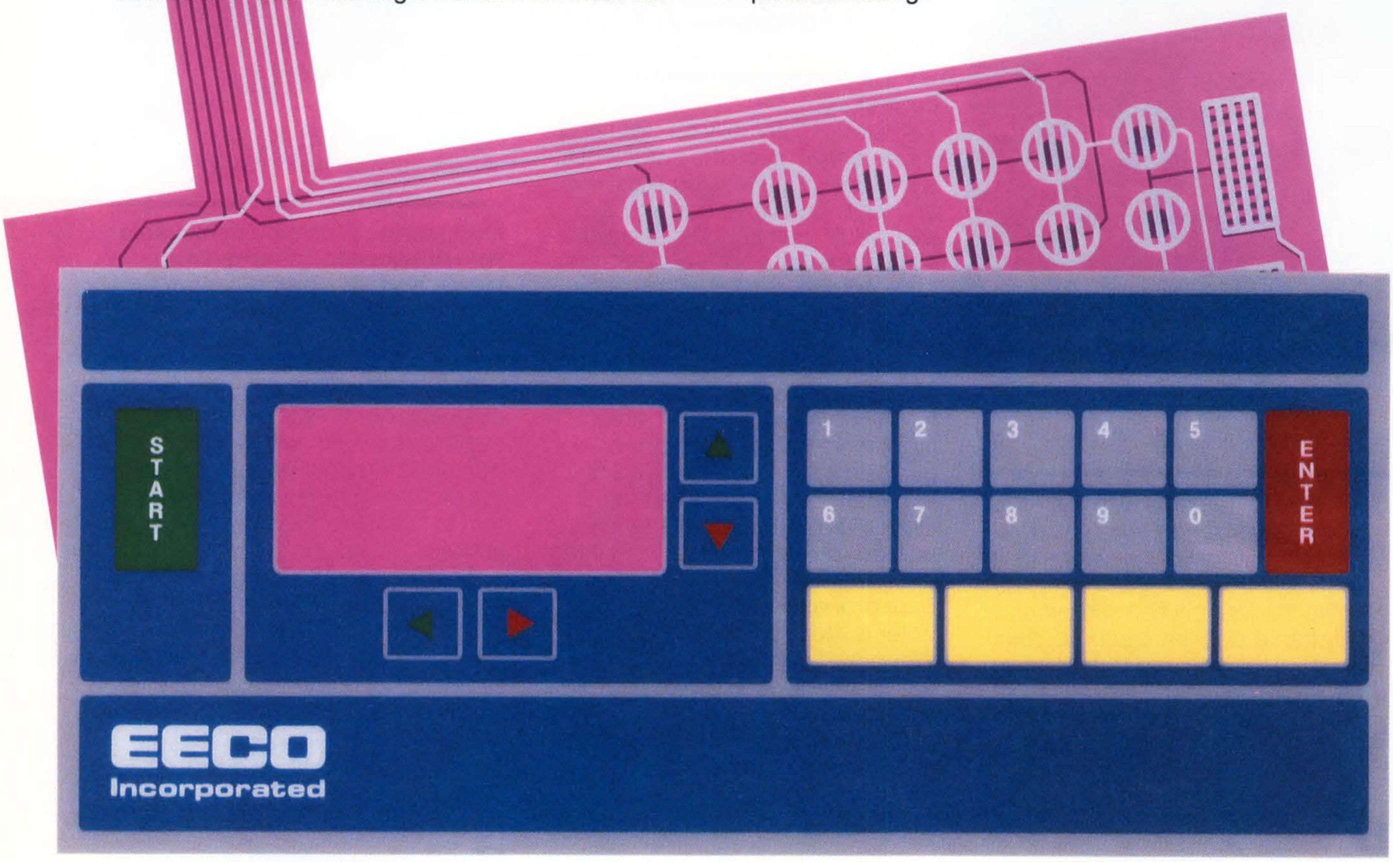
**Switch to EECO.** Your membrane switch panel is an electronic component. For over two decades, EECO has been an innovative leader in component technology, providing you with top performance thumbwheel and PCB mounted switches. We added the EECOflex® line to meet your demand for membrane switch panels from a true electronics manufacturer. Since 1977, we have been specified into rigorous medical and process control applications. Today our membranes are built entirely in-house for optimum control over processes and materials. Which guarantees the kind of quality that creates a quality image for your product. And business for your company.

**Rely on our circuitry.** EECOflex two-layer fully laminated switch circuits are screen printed on heat stabilized polyester. Conductors are always fully cured. Built-in shielding is available to block out EMI and ESD interference. State-of-the-art CAD equipment generates a prototype design with precision and speed —typically within 4 weeks after we receive your drawing. From prototype to final assembly, your EECOflex membrane's circuitry is built to work for you. Every time. And continue working. All switch elements are rated for an average lifetime of 5 million actuations.

**Look into our graphics.** You'll see bold, sharp, accurately registered overlays. Brilliant colors matched to individual lighting conditions. Take a closer look. At some of the most sophisticated graphics features in the membrane industry. Features like selective texturing for smooth integration of readout windows. Embossed key surround for definitive tactile location. A snap-dome contact system for tactile feedback to your operator. These and many more custom features add up to the visual appeal that sells your system. Up front.

**Give us your membrane design.** We'll implement it your way. EECO applications engineers work with you from Day One to make sure our membrane meets your toughest design criteria. A dependable, professional service organization assures on-time delivery and follow-up assistance. Design questions? No problem. We're only a phone call away with designer's guides, test results and specifications. Call us at (602) 272-5645, TWX 910-950-0196. Or write EECO Incorporated, Membrane Switch Operations, 2949 North 31st Avenue, Phoenix, Arizona 85017 for a product catalog.




CIRCLE 28

# NEWSFRONT

## Graphical Kernel System enters third dimension with 110 new subroutines

*The first 3D extensions add solids modeling to repertoire of Graphical Kernel System while retaining 2D compatibility.*

Programmers who must specify graphics calls for solids modeling, mechanical designs, and other types of three-dimensional imaging will soon be aided by the first 3D extensions to the Graphical Kernel System (GKS), which covers only two dimensions.

To create the third dimension, expressed as a "Z" coordinate, Saber Technology Corp. (San Jose, Calif.) adds approximately 110 subroutines to the 2D GKS structure (Fig. 1). As a result, programmers can build 3D images in software while still using most of the conventional 2D GKS rules. GKS has a leading position as a graphics standard and has even garnered the support of ANSI's X3H3.5 committee.

However, it has been limited to 2D drawing—virtually prohibiting any modeling of solids. Traditionally, programmers feared that adding a third dimension to GKS would create unnecessary complexity in the command structure.

**Stephan Ohr**

In working with 2D GKS, a programmer describes a graphic object in terms of global (real world) coordinates, which constitute the borders of the graphics display. The programmer can also specify hardware-independent logical input devices, which are not related to the coordinate structure of the display. GKS maps the logical inputs to actual physical locations and translates the global coordinates into hardware-dependent, normalized coordinates (those with a physical relationship to the CRT display).

### Step by step

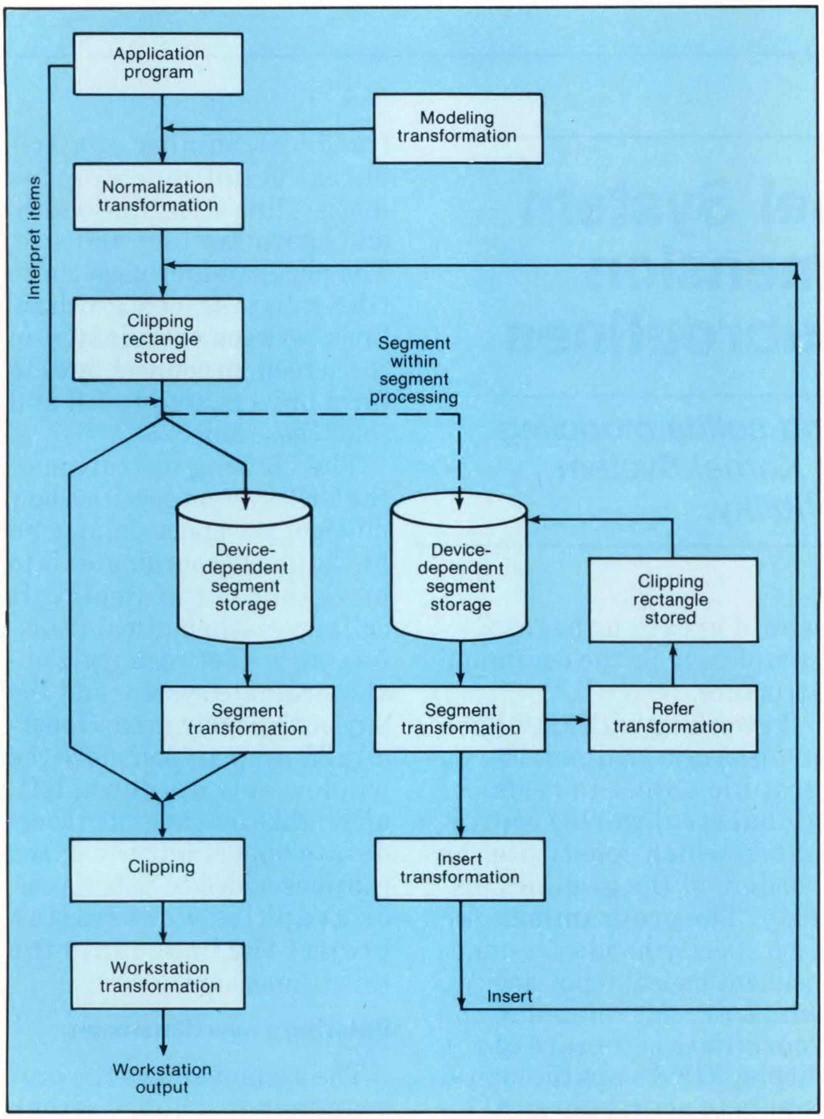
The programmer then defines the graphic characteristics of the object by attaching specific X and Y coordinates to calls to GKS primitives, which describe lines, segments, markers, text strings, and move operations. Primitives are further defined by a number of attributes including color, intensity, line style, line width, and character font and size. The programmer uses these GKS calls in sequence to draw lines between coordinates on the screen, to connect lines to form objects, and to fill and color those objects.

The viewing operation of the GKS system specifies how much of the space delineated by the global coordinates is to be visible on the display. It calls up mathematical transformations between the global coordinate system and the physical display area. Generally 2D systems can move the window only up, down, left, and right over the global coordinate space, but the extra routines added to Saber's color graphics workstation project the image into the third dimension.

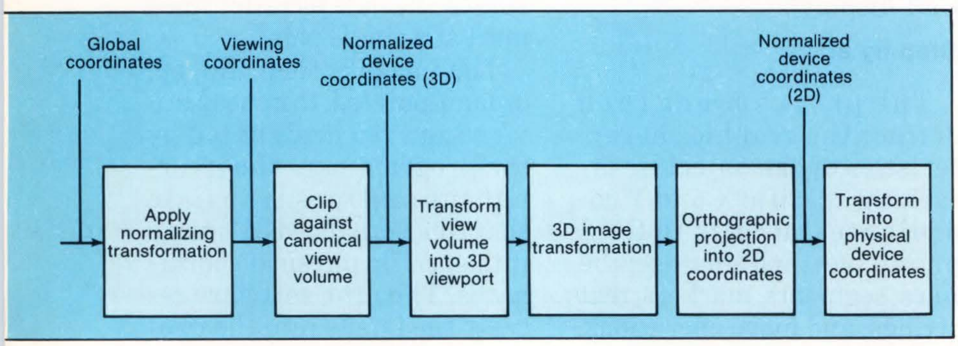
### Entering a new dimension

The system allows the programmer to choose either parallel or perspective projection. Parallel assumes all parts of the object are the same distance from the viewer, and perspective assumes that all parallel lines meet at a single point.

The image is then clipped, or manipulated, to appear in a viewing area designated by the programmer. The internal subroutines translate that conceptualized 3D image into specific physical coordinates. Then the software recasts the image into the two-dimensional equivalents of




**1. The 3D graphic's system created by Saber Technology provides extensions to the existing 2D system calls of the Graphical Kernel System. To implement a 3D coordinate system (X, Y, and Z) within a coordinate conversion structure geared for 2D operations, display-file segments are nested within display-file segments.**




the three-dimensional space, since the CRT is a two-dimensional medium (Fig. 2).

In addition, after a picture is drawn, GKS commands can pan, zoom, rotate, and perform other on-screen manipulations of the object. Included in Saber's 3D GKS system are routines which allow the drawn object to be rotated on any axis selected within the three-coordinate (X, Y and Z) system. The command structure acts, in effect, like a high-level language interpreter, offering the user a shorthand method of controlling on-screen displays without requiring that pixel addresses be entered bit by bit.

### Hardware makes it faster

While the routines for clipping and transformation are essentially software, Saber also offers a hardware accelerator whose internal matrix transformation processor can generate images as much as 100 times faster than straight software approaches.

The Saber approach draws from both the IDIGS document (developed in Europe as one approach to 3D drawing) and the American PHIGS (Programmer's Hierarchical Interactive Graphics Standard) specification, a proposal from the ANSI X3H3.1 committee.

**2. To view a 3D image (either on a parallel plane or in perspective) on the 2D CRT screen, coordinates of an object must be converted into normalized coordinates. The object is otherwise treated in software as having 3D properties.**

IEEE-488

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**NEWSFRONT**

## Electron microscope takes a peek at logic levels inside working IC

A new method for testing and verifying custom circuit designs puts the beam of a scanning electron microscope to work tracking and viewing electrical signals as they travel through an IC. The process, known as voltage contrast, was developed by scientists at Bell-Northern Research Ltd. (Ottawa, Ont., Canada). It employs the microscope's electron beam almost like a strobe light to photograph a circuit while it is operating.

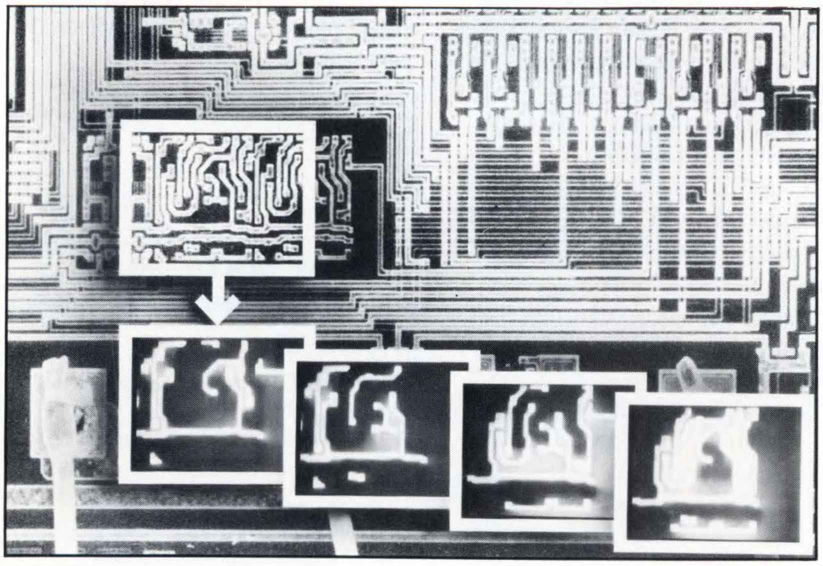
In the past, engineers have depended on mechanical circuit probes to examine chips for flaws. Such tools, however, can only test one or two points at a time. Voltage contrast, in comparison, allows large portions of a circuit to be checked all at once. Also, today's high-speed circuits sometimes use line widths as fine as 1 $\mu$m, which mechanical probes cannot handle.

#### On the right track

Specifically, the chip is placed in a scanning electron microscope whose beam is pulsed through the circuit —tracking the conductivity path of an electrical signal. As areas of the chip with different voltage levels are viewed, the device is photographed (see the figure).

If a particular part of the circuit under test is at a logical 1, it shows up as a bright area on the film. Differing voltages also appear as variations in intensity. The photos are then analyzed to check the conductivity path across the circuit, allowing designers to detect minute fabrication flaws.

The company is currently using the scheme to check custom IC designs for in-house use. *Carole Patton*



**Pulsing the beam from an electron microscope through an operating IC makes it possible to photograph the circuit as it cycles through four different logic states.**

## Streaming tape drive crosses OS and hardware barriers

A ¼-in. streaming tape drive uses a proprietary operating system that lets personal computer users transfer files between incompatible machines running under different operating systems without reformatting or rerecording the data. The drive's extensive error correction coding ensures integrity of data when tapes are used on different machines.

The key to the 4060 drive, developed by Tallgrass Technologies Corp. (Overland Park, Kans.), is the tape's operating system, called the tape management system, which is treated much like any other application program. It translates across many operating systems, currently MS-DOS, Unix, CP/M-86, and Macintosh.

Data from any of these operating systems is sent to the drive, where it is altered from the specific system's format to a proprietary format that remains constant for all of them. A controller board, based on a gate array, translates the proprietary

coding into the format of the target machine when data is read.

### Half-way splits

To ensure data integrity, the drive incorporates a 50% redundancy recording method. It splits data chunks into two blocks, then merges half of each block into a third. These blocks are separated on the tape by other data, which is similarly recorded. Using error correction algorithms, the operating system can reconstruct complete records even if two of the three blocks are erased or damaged.

The drive can transfer programs up to 60 Mbytes long —20 Mbytes longer than is possible with the QIC-24 standard—on 3M's popular ¼-in. cartridge. With that capacity it can carry Unix in its entirety, as well as large data bases.

The tape management system, written in C, has been recompiled for target machines to increase speed. OEMs incorporating the drive must add some call routines to begin backup sequences and other tasks that normally would not be included in a disk operating system.

*Terry Costlow*

## Buried isolation region speeds up silicon photodiode

An unusual structure that focuses on a buried isolation region has eliminated the slowness that plagues most p-i-n photodiodes. The process has produced a component that responds faster, reduces dark current (leakage), and operates at supply voltages as low as 4V—all in a fiber-optic communication systems operating at wavelengths of 800 to 900 nm.

Researchers at Bell Communication Research (Murray Hill, N.J.) incorporate a heavily doped $p^{++}$ buried layer—about 5 $\mu$m thick—with a standard moderately doped $p^{+}$ substrate, a p epitaxial layer, and a shallow $n^{+}$junction (Fig. 1). The structure traps minority photoelectrons in the substrate, contributing to the speedy transient response.

### Slow going

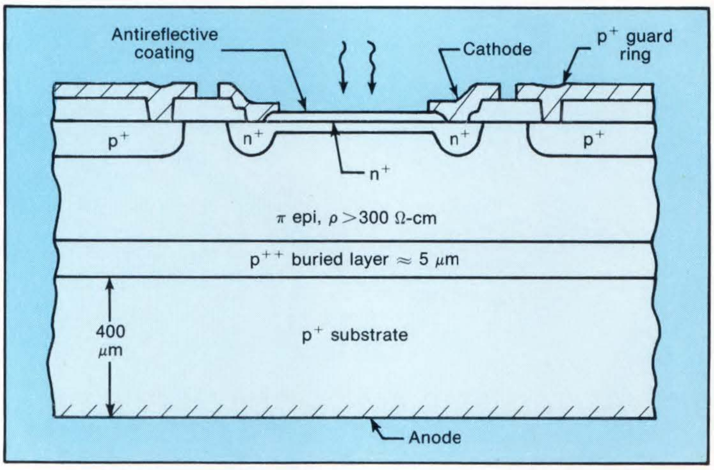
In photodiodes that use a thin epitaxial coating, the radiation generates photocarriers in the undepleted substrate. Those minority carriers slowly diffuse back to the depleted junction, thereby slowing the transient photoresponse. Though a thicker epitaxial layer could hasten the response of high-bit-rate systems, it causes the operating voltage to climb above 5 V, the standard level for TTL and CMOS circuitry.

In Bell's process, the doping gradient of the $p^{++}$-$p^{+}$ interface creates a built-in electric field that reflects the minority carriers back to the substrate and away from the depletion region of the junction. The interface of the $p^{++}$ and the epitaxial layer also improves speed, since it affords a built-in polarity that causes photoelectrons to drift into the depletion region and

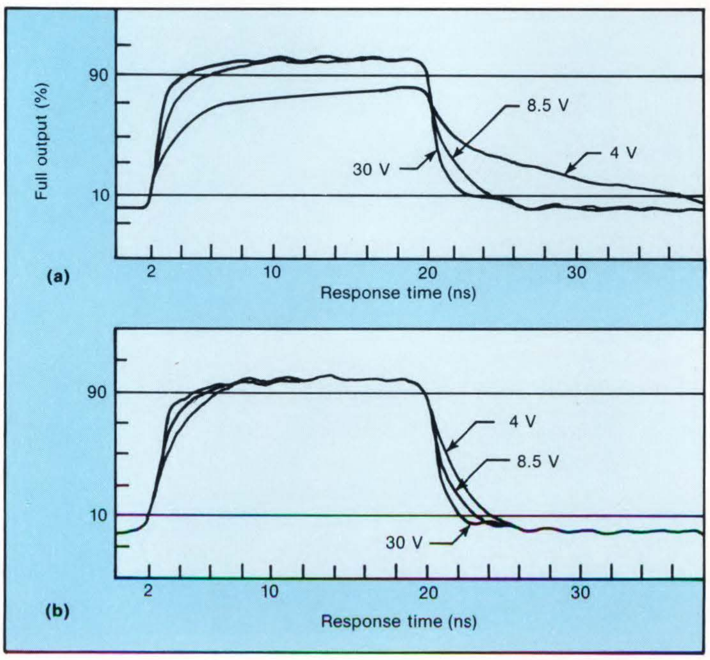
## NEWSFRONT

be collected.

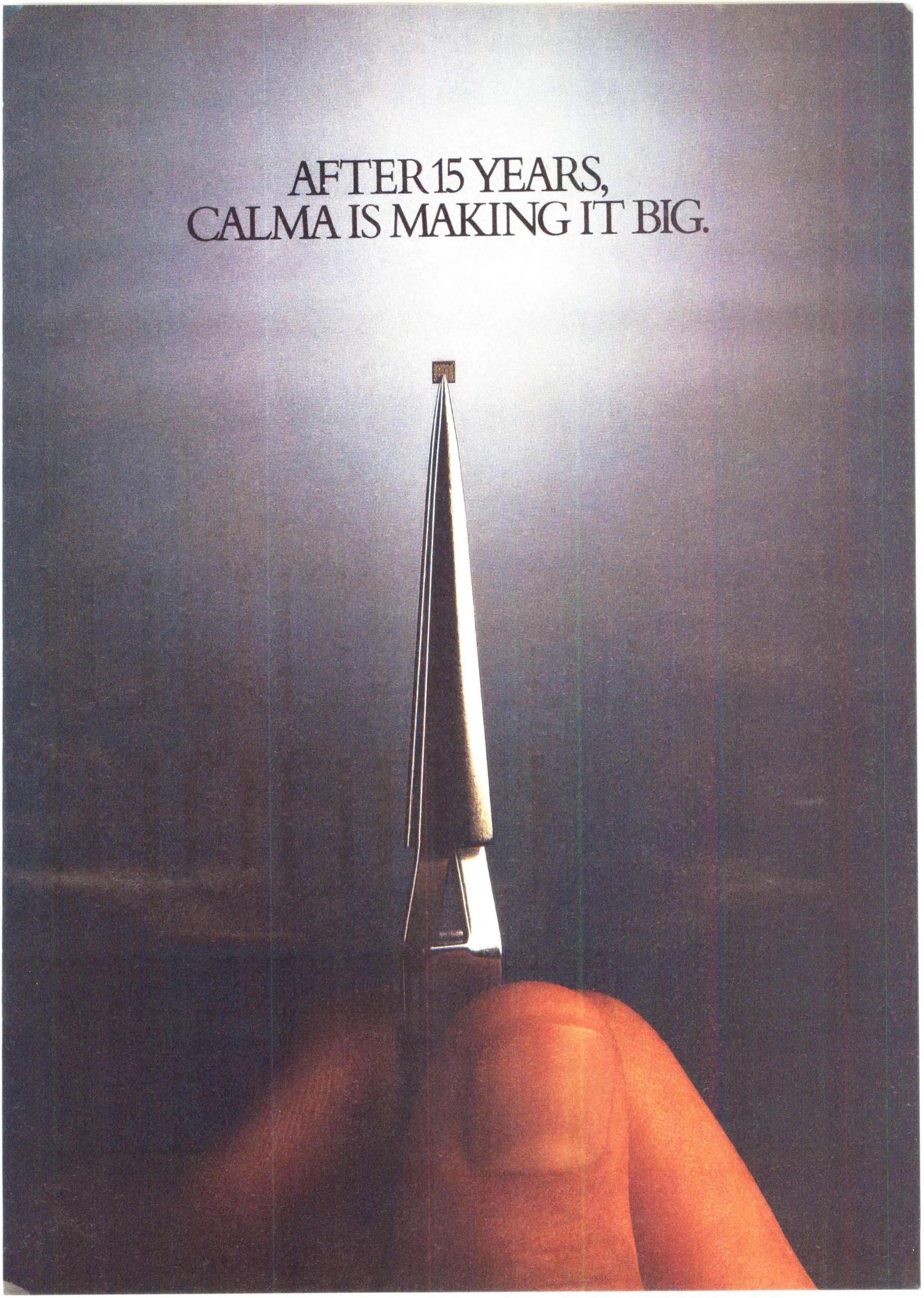
Dark currents fall as much as sixtyfold, since diffusion current generation occurs in the thin isolation layer (the buried $p^{++}$ region) rather than in the substrate. Devices fabricated in this process have demonstrated a 3-ns transient response at 4 V (Fig. 2). In contrast, the response of a conventional p-i-n photodiode trails off dramatically. *Warren Andrews*




**1. A Bell Communications process characterized largely by a heavily doped $p^{++}$ buried layer produces a faster photodiode with significantly lower dark current than conventional components.**




**2. A comparison between a conventional p-i-n photodiode (a) and Bell's experimental photodiode (b) reveals that the response time of the p-i-n diode falls off sharply, particularly at low supply voltages. In addition, it fails to reach 90% of full output even when operating at 4 V.**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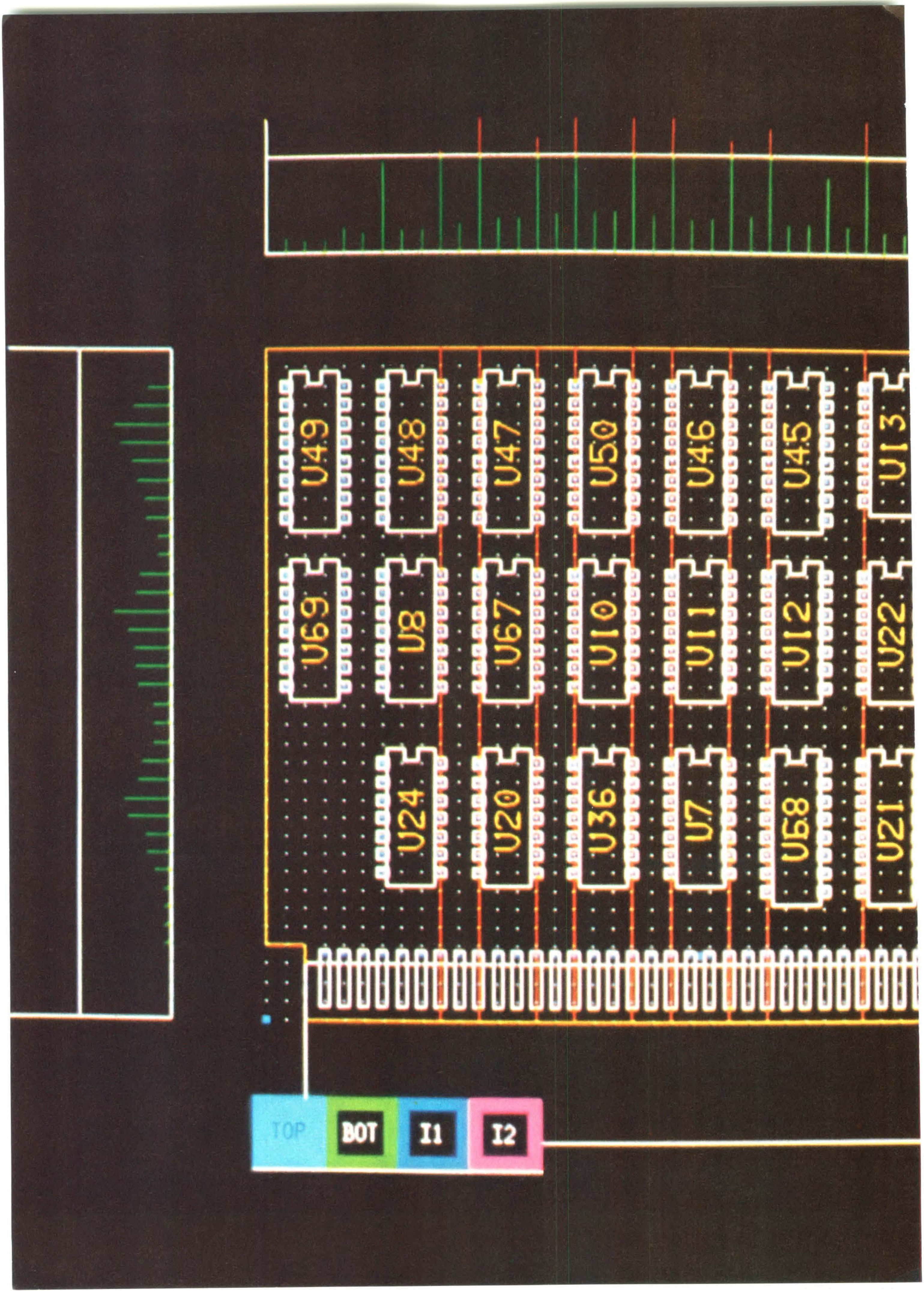

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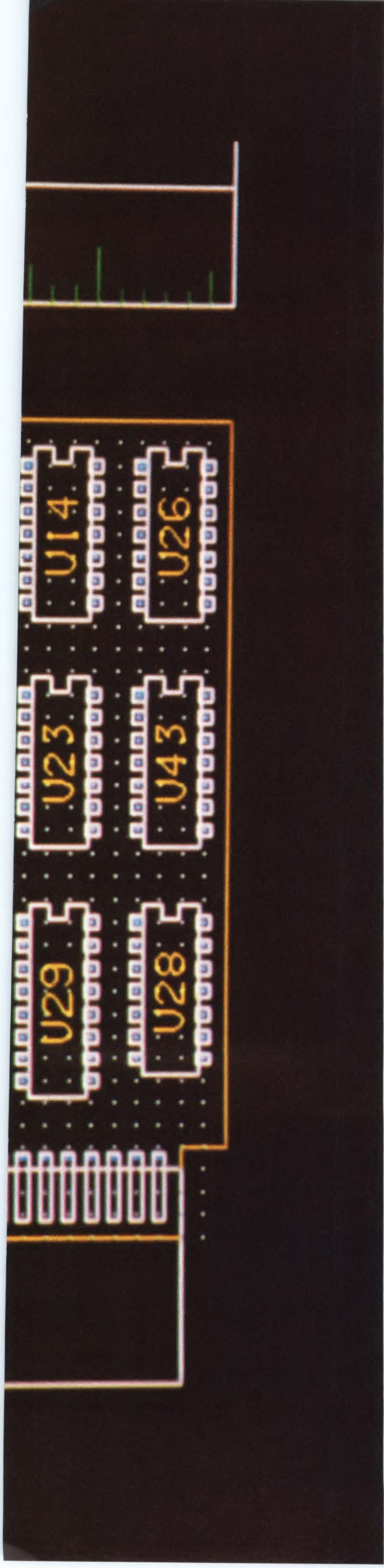


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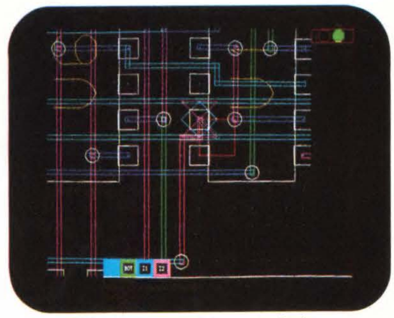
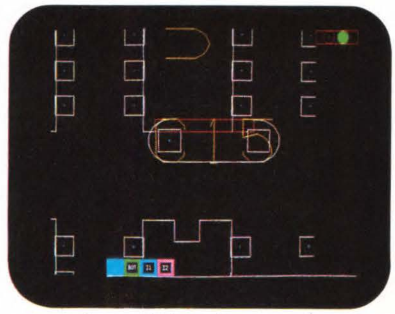


*Error lockout and dynamic checking.*



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**CIRCLE 32**

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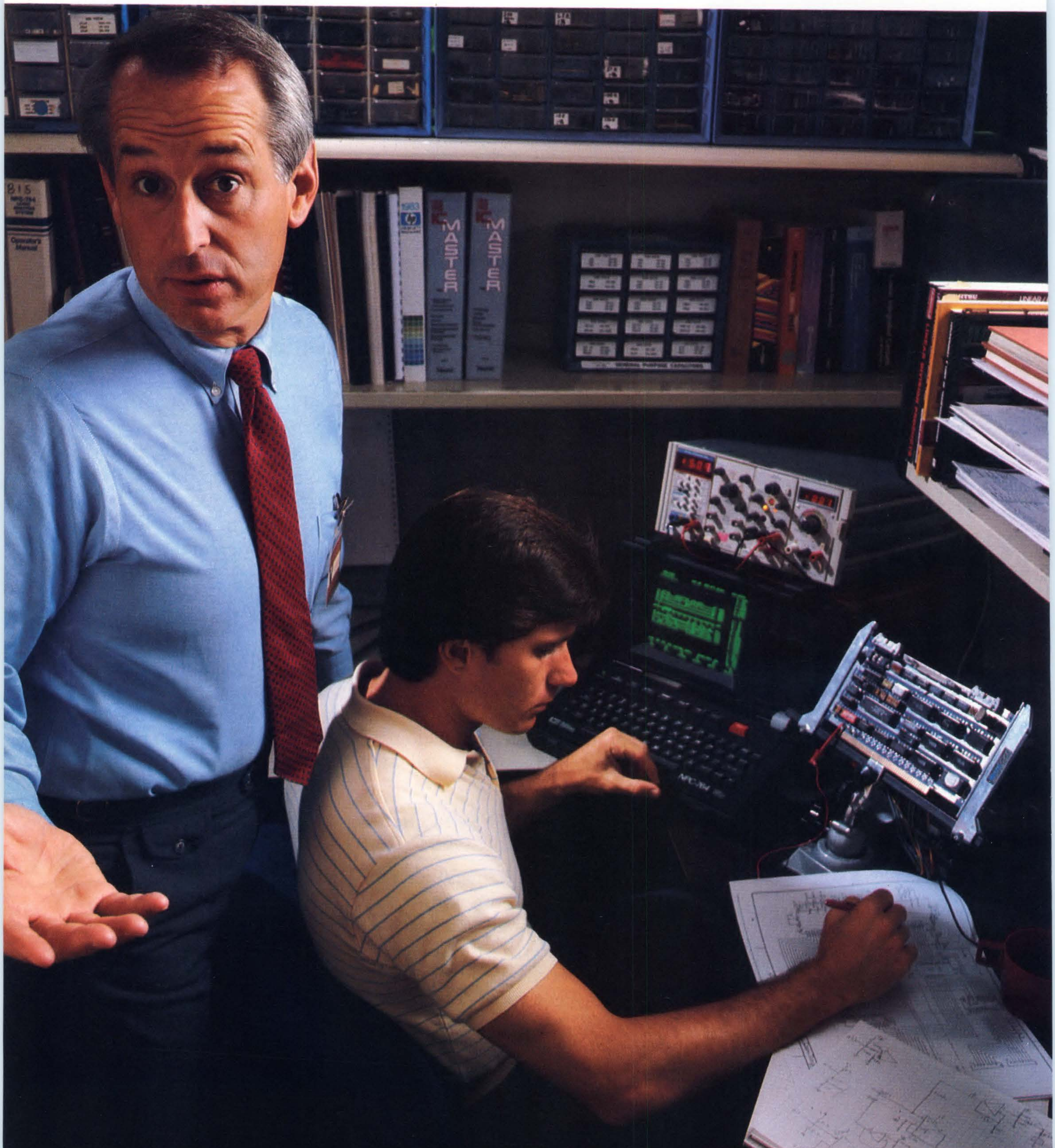

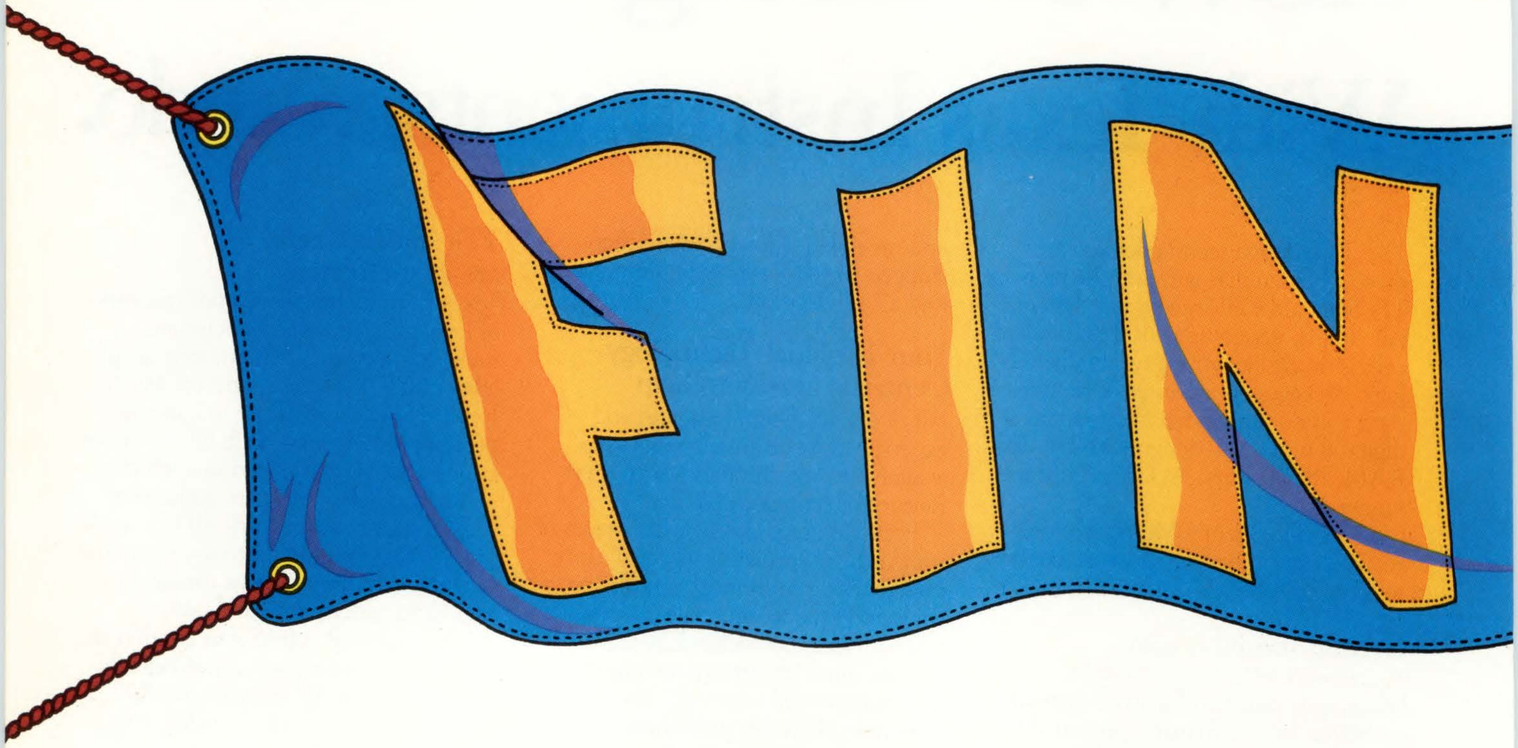
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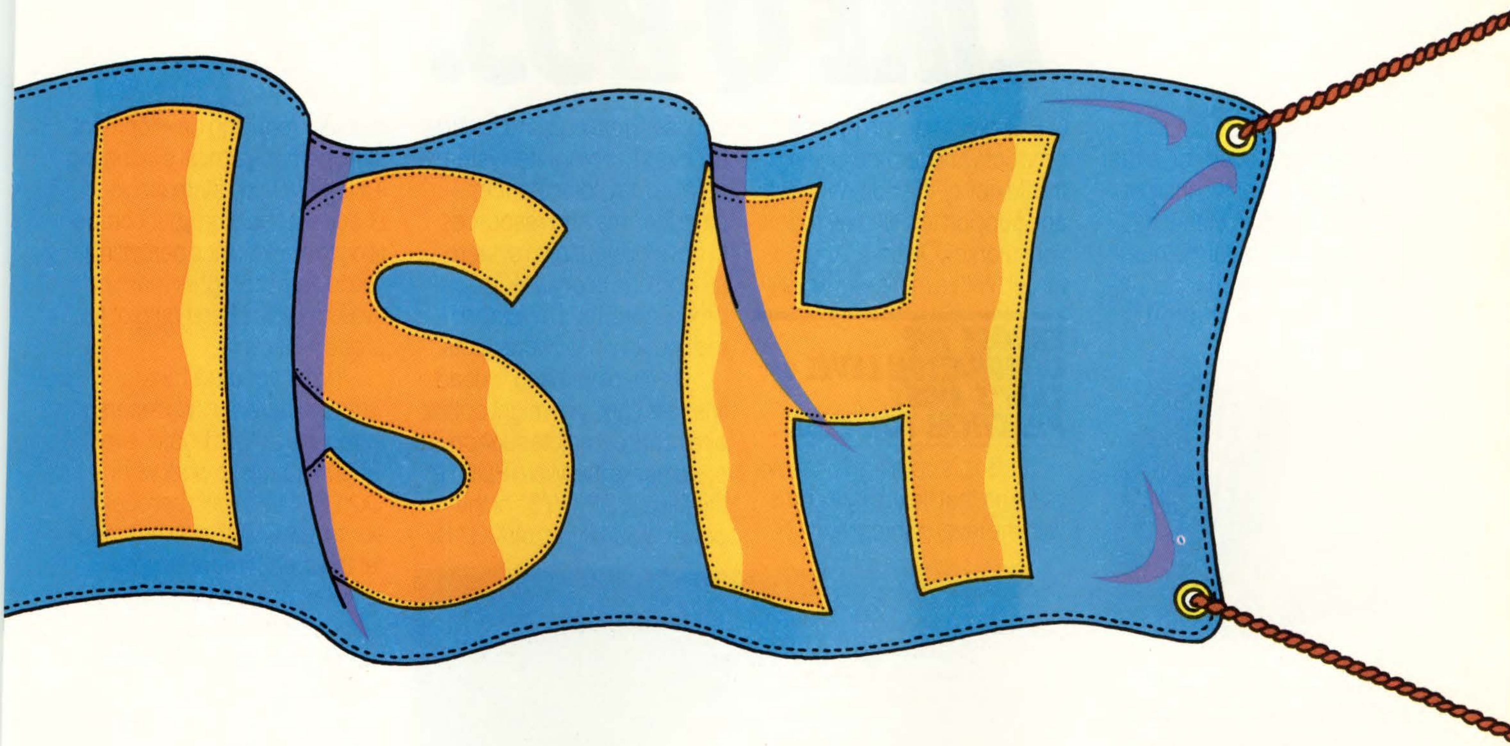


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CIRCLE 33

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We also understand the commitment you make when you select an architecture. And your need for support of that architecture. Not just from the manufacturer, but from third party sources as well.

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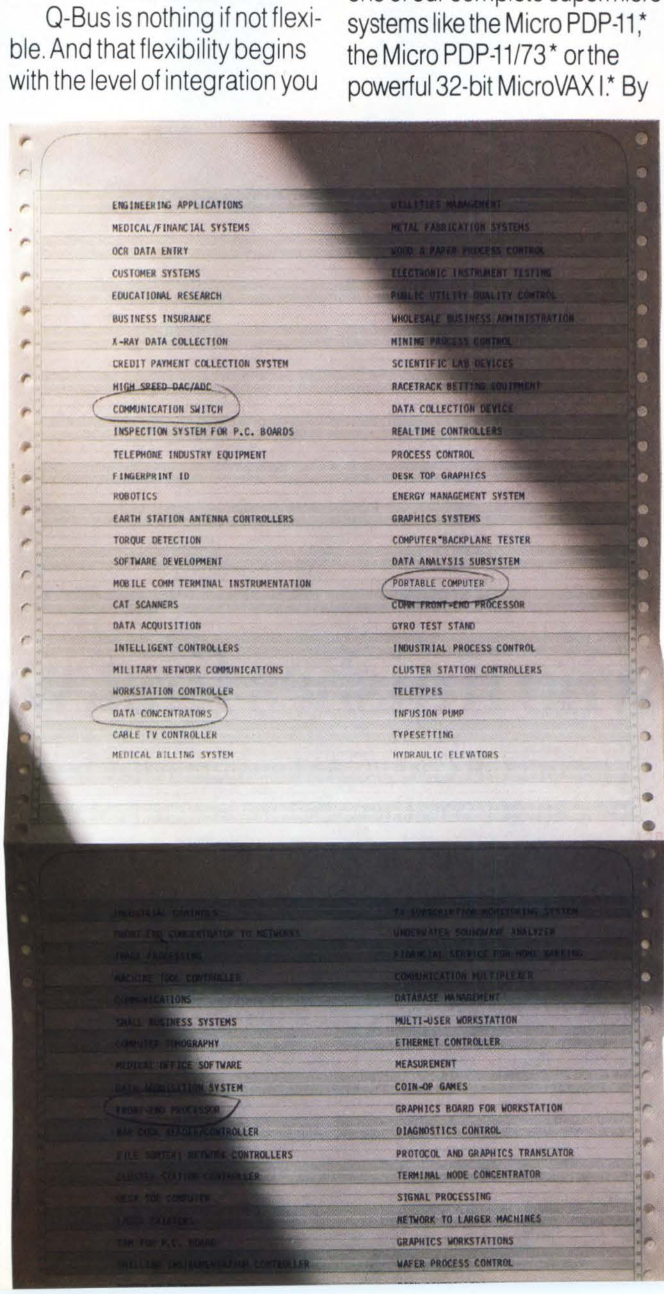


If your needs fall somewhere in between, we recently introduced three board level CPU products to work with. Our LSI-11/73* microprocessor, a new CMOS microcomputer that benchmark studies show exceeds the performance of a similarly configured MC68000* or NS16032* in most applications.

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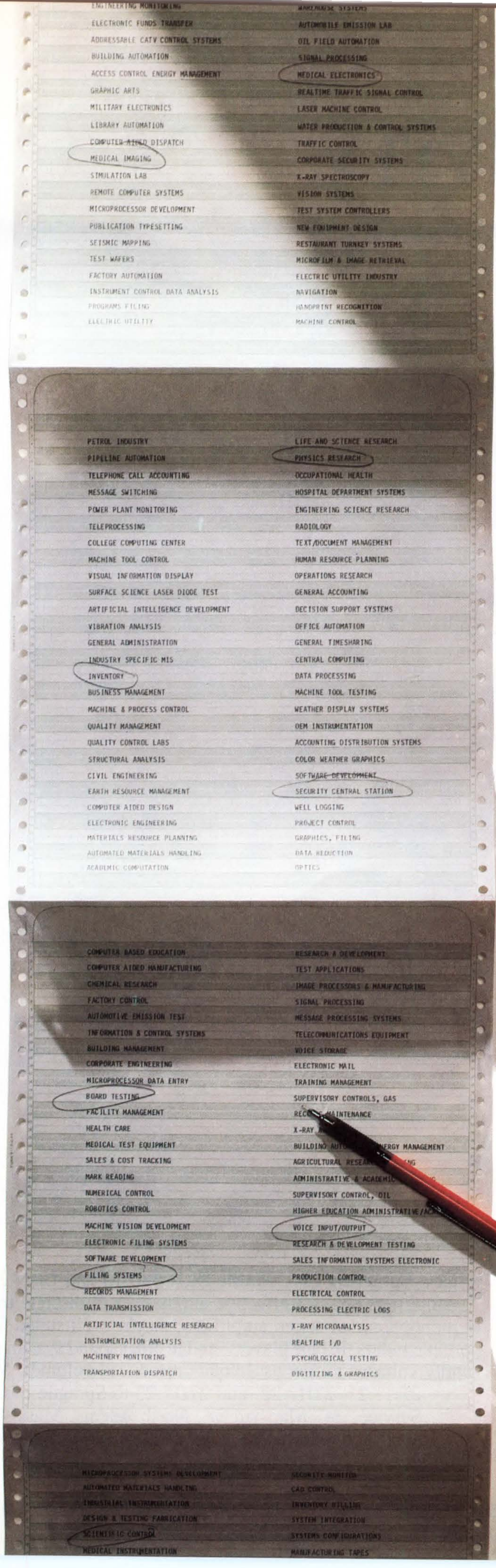


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# NEWS ANALYSIS

## Sputtering, plating vie for high bit densities on Winchester disks

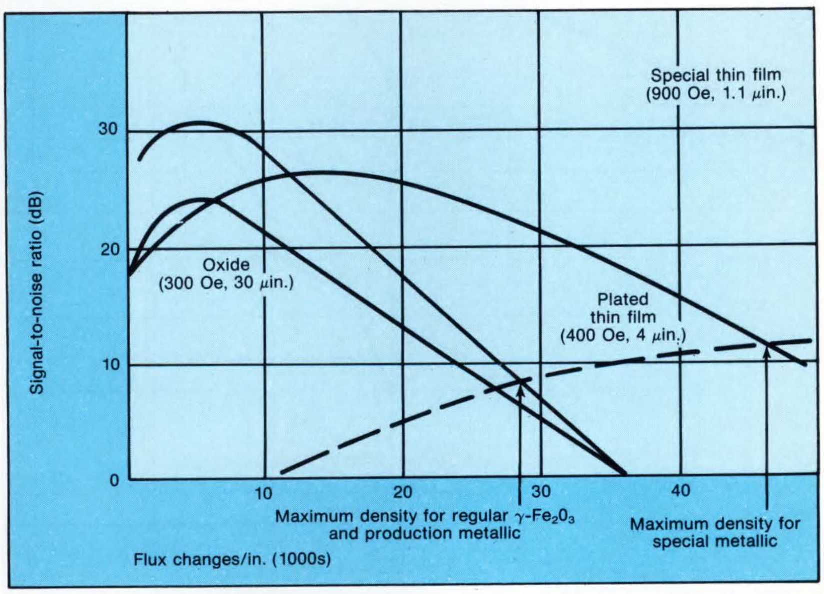
*Sputter-deposited magnetic coatings compete with plated media to replace today's gamma-ferric oxide in high-density disk drives.*

The evolution of high-density Winchester drives—complete with thin-film heads, encoding techniques, and servo tracking mechanisms—is fostering some dramatic changes in the way that magnetic disks are manufactured. Thin-film plating and sputtering techniques are now being developed to accommodate the higher bit and track densities anticipated before 1990—as much as 40,000 to 50,000 bpi and 2000 tpi.

In contrast to today's disk coatings, primarily gamma-ferric oxide, the new thin-film coatings will yield disks with higher bit densities, increased signal-to-noise ratios, and smoother surfaces (and thus lower flying heights). At the present time, particulate-oxide layers cannot handle recording densities greater than 18,000 to 20,000 flux changes/in. at 800 to 1000 tpi.

Sputtering and plating processes deposit magnetically sensitive thin films, made from cobalt alloys, onto the surface of a hard disk substrate. The disks perform well at extremely high densities (Fig. 1), and several companies have already produced some impressive figures. For instance, Applied Information Memories (Milpitas, Calif.) has applied its own sputtering technique to a 250-Mbyte 5¼-in. drive. Five disks together handle 18,534 flux changes/in. With 2,7 run-length-limited (RLL) code, that density effectively translates into 28,000 bpi.

Using plated thin film, Maxtor Corp. (San Jose, Calif.) has topped that with a 380-Mbyte, eight-platter drive that handles 22,000 flux changes/in. It, too, uses 2,7 RLL encoding to bring its effective bit density to over




**1. Even without reducing head-flying heights, solid metallic media (with 400 to 900 Oe coercivities and coating thicknesses of 4 to 1 μin.) will outperform iron oxide layers (with 300-Oe, 30-μin. coatings) at recording densities in excess of 18,000 or 20,000 flux changes/in. These projections assume a 1-mil track width (i.e., 1000 tpi).**

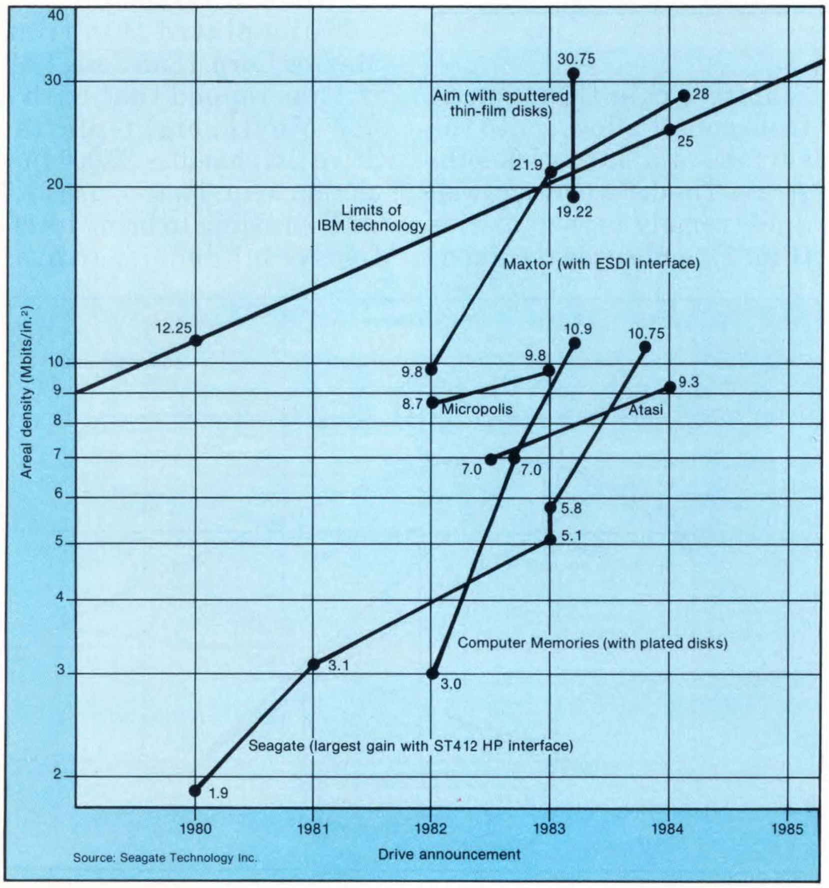
**Stephan Ohr**

30,000 bpi. In contrast, the packing density of a one-time record holder, the IBM 3380 14-in. Winchester drive, is only about 11,000 flux changes/in., for an areal density of 11 Mbits/in.$^2$ (Fig. 2).

**Limitations of oxide**

The recording technology for current commercial drives handles track densities of 1000 tpi and bit densities of 12,000 to 13,000 flux changes/in. With embedded servo tracking mechanisms, those figures jump to between 22,000 and 24,000 flux changes/in., and with advanced coding techniques, drives could possibly exceed 40,000 bpi (see the table, p. 68).

Currently, even with "enhanced" cobalt-doped oxide formulations, the particulate structure of the oxide coating rules against much higher bit densities. One of the major stumbling blocks is the signal-to-noise ratio, which falls rapidly as the disk surface area per recorded flux change decreases.




**2. High-performance disk drives have not followed the density projections of IBM, which for a long time set the standards for Winchester technology. The extremely steep development paths are a result of thin-film plating and sputtering, sophisticated interfaces, and frequently both.**

**Sputtering vs plating**

The question emerging now is which of the two newer thin-film deposition techniques—sputtering or plating—will have more to offer.

In the plating process, thin films are plated onto a disk's surface in an electrically or chemically active liquid solution. The film is typically a cobalt-phosphorus alloy that is deposited in a 3-$\mu$in.-thick layer. The alloy provides a coercivity on the order of 800 Oe and in some cases up to 1000 Oe.

The sputtering process, on the other hand, deposits magnetic layers and protective coatings molecule by molecule onto the surface of a disk in a vacuum chamber. Because it is a "dry" process, it offers better control over the material contamination that could cause defects than "wet" plating processes. It can alloy cobalt on a molecular level with a variety of other metals such as nickel, chromium, potassium, and even iron and its oxides. In theory, it can offer a wide selection of magnetic properties, including coercivities up to and above 1000 Oe. In its present state of infancy, the sputtering process can deposit uniform layers 3 $\mu$in. thick. However, experts predict that the process will soon be depositing layers a mere 1 $\mu$in. thick—estimated to be the ideal thickness for high-density

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longitudinal recording.

Sputtering processes vary from manufacturer to manufacturer, magnetic material to magnetic material, and substrate to substrate. Essentially, a molecularly active target material is bombarded by a high-energy source that strips away molecules. They are attracted to and come to rest on the charged surface of the disk substrate (Fig. 3). One variant of the sputtering process is bias sputtering, where the target and the disk substrate become highly charged cathode and anode elements in a chamber filled with argon or some other inert gas.

Another variant, rf sputtering bombards the target with microwave energy, stripping away molecules and directing them toward the disk. This process is particularly effective for sputter-coating plastic and other nonconductive substrates and suggests the possibility of both lower cost and potentially smoother surfaces. In addition, the lighter (lower density) materials may have less rotational inertia, making stopping and starting faster and perhaps reducing the demands placed on the drive motor.

### Better control

Compared with plating, sputter-deposited thin-films afford greater control over defect levels in the magnetic material itself. This becomes increasingly significant as bit densities rise, calling for an ultrapure media.

According to Domain Technology Inc. (Milpitas, Calif.), which is active in both plating and sputtering, the industry will typically tolerate only 6 to 12 noncatastrophic disk defects. The company expects that figure can be reduced to 4 or 5. The trick is that the number must remain constant as recording densities increase by a full order of magnitude.

Advocates believe that sputtering also gives more flexibility to the disk's magnetic properties. Thus manufacturers can better tailor disks to particular heads, thereby varying coercivity, flying heights, and data encoding schemes. In addition, they can use lightweight, nonmetallic substrates such as glass or plastic in place of the aluminum and aluminum alloys now being used.

### Smooth flying

Yet another key to increasing density is the flying height of the recording head, which is integrally related to the smoothness of the media surface. Backers of sputtering believe the surface smoothness required to move flying heights from their present 12 or 13 $\mu$in. down to 6 or 7 $\mu$in. can best be achieved with sputtering deposition. Further, to provide the even greater density advances anticipated toward the end of this decade—possibly as high as 300 Mbits/in.$^2$—flying heights will have to be reduced to about 4 $\mu$in. (Fig. 4). Current plating techniques chemically etch the substrate's nickel undercoat, producing a more adhesive surface that might not be smooth enough for 4-$\mu$in. flying heights.

Finally, the followers of sputtered disks believe it will

**Projected 5¼-in. disk drive capacities**

| Density (bpi) | Capacity (Mbytes) | Required technologies | Year of implementation |
|---|---|---|---|
| **Present interfaces** | | | |
| 10,000 | 75 | Ferrite heads and gamma ferric oxide medium | 1983 |
| **Interface changes** | | | |
| 15,000 | 112 | Advanced codes and enhanced oxide; thin-film heads and enhanced oxide; or thin-film medium | Late 1984-85 |
| 20,000 | 150 | Advanced codes, thin-film heads, and enhanced oxide; advanced codes and thin-film medium; or thin-film heads and thin-film medium | 1985-86 |
| 40,000 | 300 | Perpendicular recording | 1987-88 |

Note: A five-disk configuration and eight data surfaces at 980 tpi are assumed.

be the technology of choice for emerging vertical recording techniques and may even become the dominant manufacturing method for depositing light-sensitive coatings on optical disks.

**Too long?**

Critics, on the other hand, believe that sputtering techniques will require years of development before they will be available at reasonable cost in large production quantities. Furthermore, manufacturers still must cope with the same problems faced by plated disk makers: variations in delivered raw materials (substrates and magnetic materials). Claims of greater purity in the sputter deposition process simply may not be warranted.

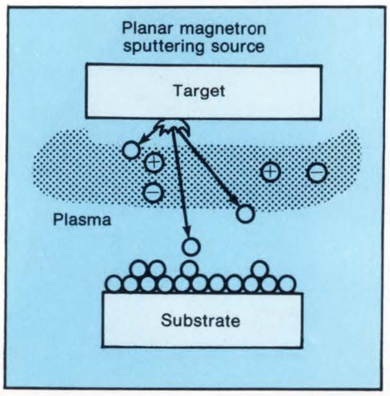
In addition, critics question whether what they characterize as marginal benefits will justify the costs of developing the process for volume manufacturing. For example, Maxtor feels that the full bit-packing potential of thin-film plating has not been reached. It says that parallel developments in sputtering and plating technology will continue to make plated disks look relatively attractive.

Others within the industry speculate that the sputtered disk facilities now emerging are the first buds of seeds planted more than two years ago, when the then immature disk drive industry believed that only sputtered coatings could achieve high density. Developments have demonstrated otherwise. In all likelihood, those new sources of sputtered disks will simply complement the supply of thin-film plated disks.

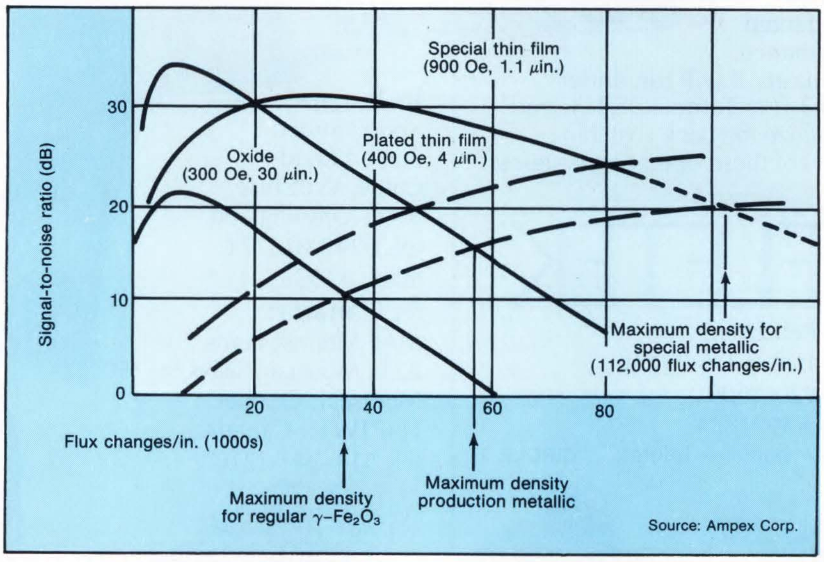
However, not everyone agrees. Currently a handful of small companies are rushing to get their sputtering equipment up and running and to get disks characterized well enough to get into the hands of drive makers.

**Already a reality**

Lin Data Corp. (Santa Clara, Calif.) and Applied Information Memories began shipping sample units earlier this year. Hot on their heels are Cyberdisk Inc. (Anaheim, Calif.), which hopes to produce the first prototypes later this year, and Domain Technology, which is aiming at early 1985. Cyberdisk and Domain agree that it may be years before the process is fine-tuned enough for volume production. With a lower profile, Nashua Corp. (Nashua, N.H.) declares its sputtering




**3. In the disk sputtering process, a target containing magnetic materials is bombarded by high-energy ions in a vacuum chamber containing an inert plasma gas. The magnetic material breaks off the target and is deposited—molecule by molecule—on the surface of a disk substrate.**




**4. With head-flying heights lowered to 4 μin., oxide layers have a limit of about 34,000 flux changes/in. with a 1-mil track width. Plated disks (400 to 600 Oe) will offer up to 55,000 flux changes/in. A 900-Oe special thin film might allow densities up to 112,000 flux changes/in.**

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## NEWS ANALYSIS

facility is strictly for internal experimentation.

Ampex Corp.'s Disk Media Group (San Jose, Calif.)—one of the leaders in plated disk technology—is hedging its bet and has quietly acquired and put into operation a West German-made (Laybold-Heraeus) sputtering machine for experimental use. Though Ampex maintains that the high-density potential of its own Alar plated media may not be reached for many years, it is mastering the sputtering process both as a technique for despositing the magnetic layer and as a means of coating the disks with carbon to protect them and to serve as a lubricant.

This carbon overcoat, some experts predict, may render the apparent argument between sputtering and plating academic. In addition to preventing "stickion" (a phenomenon in which two ultrasmooth surfaces inadvertently adhere to each other), the coat protects the disk from signal-level losses due to oxidation and from dropouts caused by glancing head abrasions.

The process has proved so successful in protecting disk surfaces that at least one drive manufacturer, Vertex Peripherals Inc. (San Jose, Calif.), has begun to store data in the disk space traditionally reserved as a landing zone for the head (during inactivity), assuming that the carbon will protect the data surface even when the head physically rests on it.

Although this overcoat approach calls for the heads to fly somewhat higher—currently precluding the possibility of 4-$\mu$in. flying heights—the benefits appear to outweigh the disadvantages. And, claim the stauncher supporters of sputter deposition, once disk manufacturers have mastered the carbon overcoat, it is only a matter of time before they master the sputtering of magnetic layers and thus gain the advantages of lower defect levels and smoother surfaces. □

# THE BIRTH OF THE ARRAY PROCESSOR AGE


Until now, array processors have filled an important, but restricted, niche in the computing world. Analogic's AP500 has changed that. Because of its unique combination of flexibility, performance, and reasonable cost, the AP500 opens a vast number of computationally-intensive problems to array-processing power.

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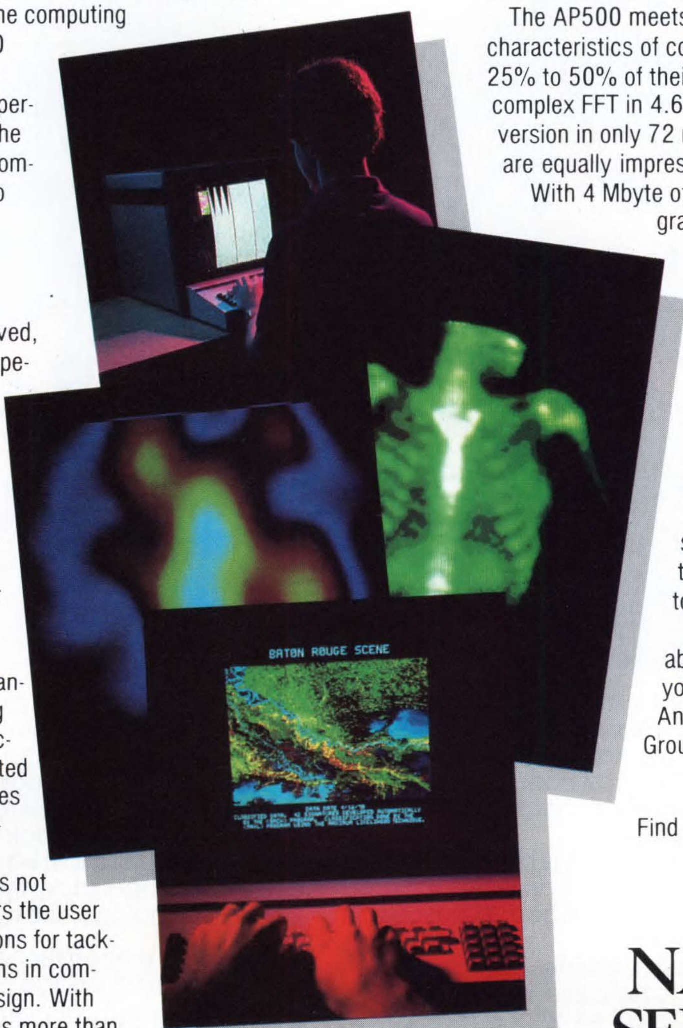


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**CIRCLE 42**

# SOLVING THE MYSTERY OF THE BLUE SKY PHENOMENON.

This is the 2nd in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.

In the microprocessor world, the "Blue Sky Phenomenon" refers to microprocessor development code crashes. The code simply and quite mysteriously disappears. The most common culprits are bugs. And the fact is, simple program bugs will crash most microcomputers.

The hosts for some of these bugs have famous names. What they all have in common is an absence of mechanism to protect against crashes. There is one exception.

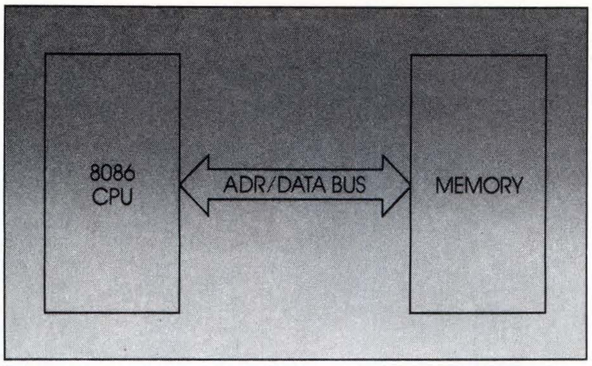
The Zilog Z8000® family provides comprehensive hardware protection to help create systems that are resistant to system crashes so common in primitive architectures. The Z8000 CPU is not only more reliable in this sense, but it's easier to learn how to use. Especially if you already know how to use the ubiquitous Z80® CPU.

## LOST IN THE WILD BLUE YONDER.

There is a technological reason why some microprocessors are so prone to corruption. It stems from the direct connection of the memory to the processor. Without any checking hardware between the processor and memory, the processor can change any area in its memory at will—without regard to the consequences. Such a lack of restrictions allows illegal operations such as changing program memory stack underflow (running the stack into the data area), and even modifying the code of the operating system. This lack of appropriate technology has two glaring results:

- Illegal operations cannot be detected before damage has occurred.
- Any damage to the program and data cannot be undone.

There are far-reaching implications for a lack of memory protection. Systems designed without it do not support multiple users, nor even UNIX™ very well. The simplest bug will crash the system. There is no protection and no recovery mechanism against even minor problems of access violations. The ability to handle more than one user is usually not allowed, or is strongly discouraged.

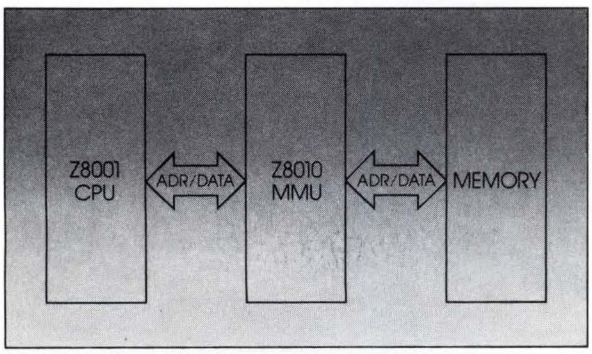



A typical Intel 8086-to-8088 configuration, the lack of memory checking hardware—the memory to the processor. The processor can change any area in its memory at will, without regard to the consequences. The result: illegal operations cannot be detected before damage has occurred; and any damage to the program and data cannot be undone.

## THE Z8000 CPU—THE FULL-PROTECTION MICROPROCESSOR.

Zilog's Z8000 CPU solves these problems by inserting a chip called the Z8010 MMU (memory management unit; available in paged or segmented versions) between the processor and memory. This chip normally passes addresses from the processor to the memories—checking each memory access for its address and type of operation as it occurs. If the MMU chip detects an illegal operation, or the use of an unauthorized address, it suppresses the illegal operation and interrupts the program. It passes control to the operating system. Once the program is stopped, the operating system can inspect, correct, or abort the program that caused the error. All with no wait states.

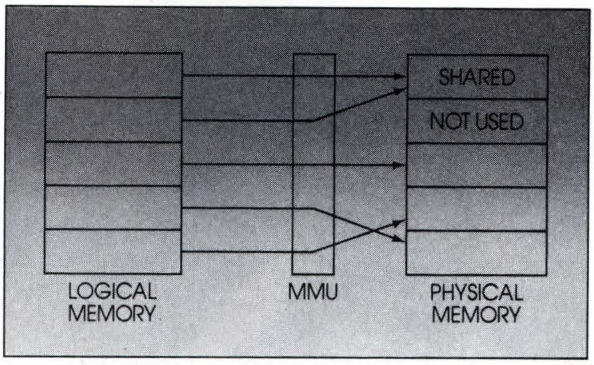
A system constructed with the Zilog MMU can allow many different programs to run without the fear that one program could entirely stop the rest or even corrupt the rest. But, the memory management hardware goes beyond providing protection. It also simplifies system implementation.




Zilog's configuration system prevents the Blue Sky Phenomenon by inserting a chip called the Z8010 Memory Management unit between the processor and memory.

## HIGH LEVEL LANGUAGES REQUIRE MEMORY MANAGEMENT.

One of the strengths of 16-bit microprocessors—and the Z8000 CPU in particular—is that they support high level languages such as C, PASCAL and FORTH. A goal of most users is to allow more than one of these high-level language programs to execute in the processor at the same time (multi-user/multi-tasking)—gaining more effective utilization of the computer. The challenge is to provide an architecture that allows a language compiler to produce code targeted to run at one address, but allows the actual placement at a different physical address. This mapping is known as logical to physical translation—a feature of the Z8010 MMU.




Zilog satisfies the common requirement for systems to share information with our MMU. The logical-to-physical translation capability allows more than one logical area to access a common physical area.

## SHARED MEMORY IN THE Z8000 CPU.

Another common requirement for systems is the need to share information. With Zilog's Z8010 MMU, the logical-to-physical translation capability allows more than one logical area to access a common physical area. When combined with the protection capabilities of the Zilog MMU, you can set up areas that can be common read-only while the same physical area could be read AND write when accessed under different conditions (operating system access).

For example, you could construct a process control system that posts status information into a common area. The central core of the system is allowed to read and write this common area. Application programs that need access to this information can read it through a totally different segment that is translated into the proper physical address—but with the provision that all access must be reads, not writes. If an application program were to run wild and attempt to corrupt the common area by writing into the read-only space, it would be intercepted before any write could occur.

The key benefit to using Zilog's MMU to implement shared memory is its flexibility to make multiple logical segments access a common physical area with all of the protection—or lack of protection—desired. All with no overhead per access. What's more, Zilog's MMU and other Z8000 devices are available from a host of reliable second sources.

Solving the problem of the "Blue Sky Phenomenon" is only one of the technological hallmarks of the Z8000 CPU. Others will be discussed in this continuing series of technical papers from Zilog, Pioneers of the Microworld. For details on the Z8000 CPU, call our Literature Hot Line at 800-272-6560.* Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.
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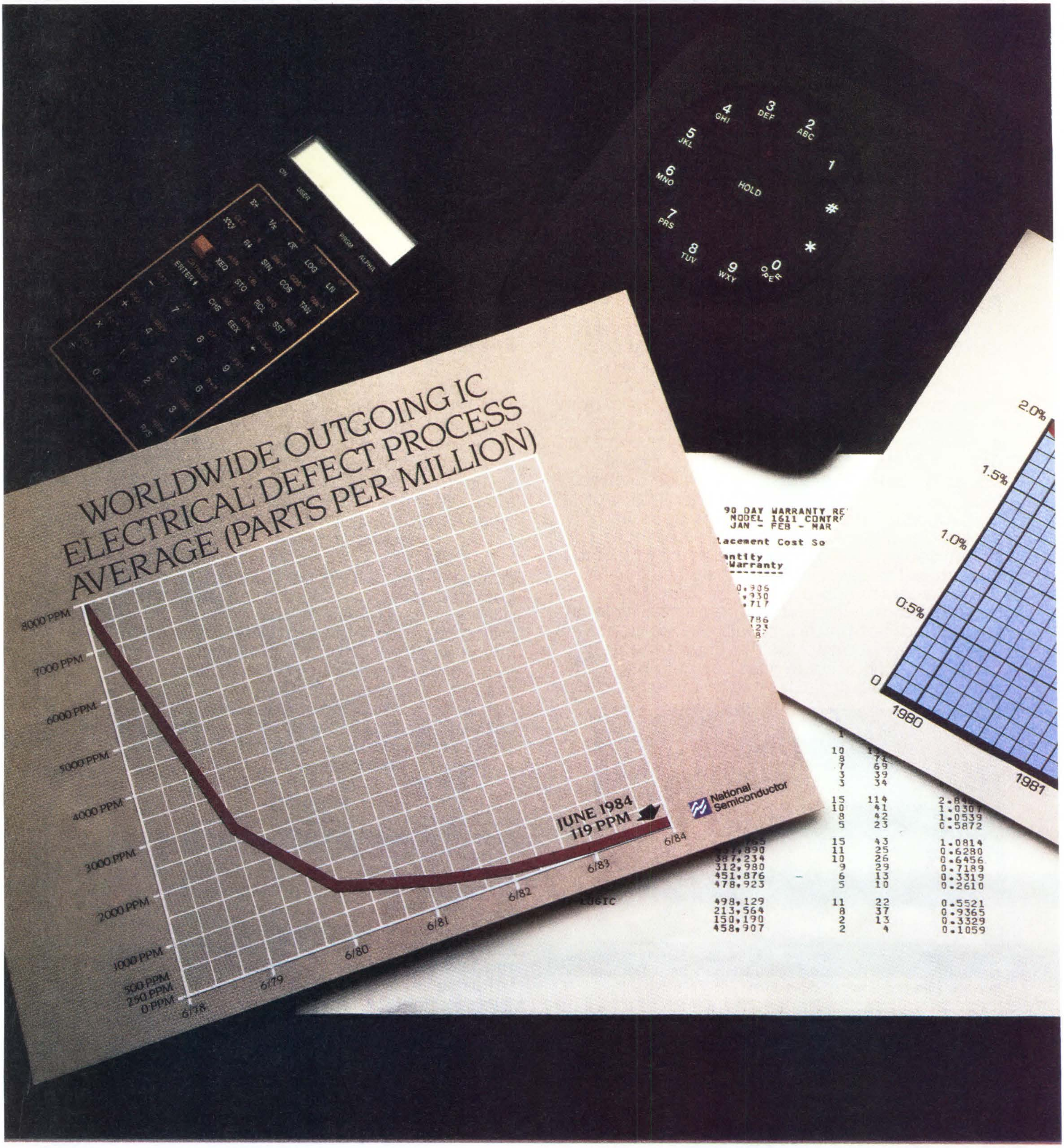


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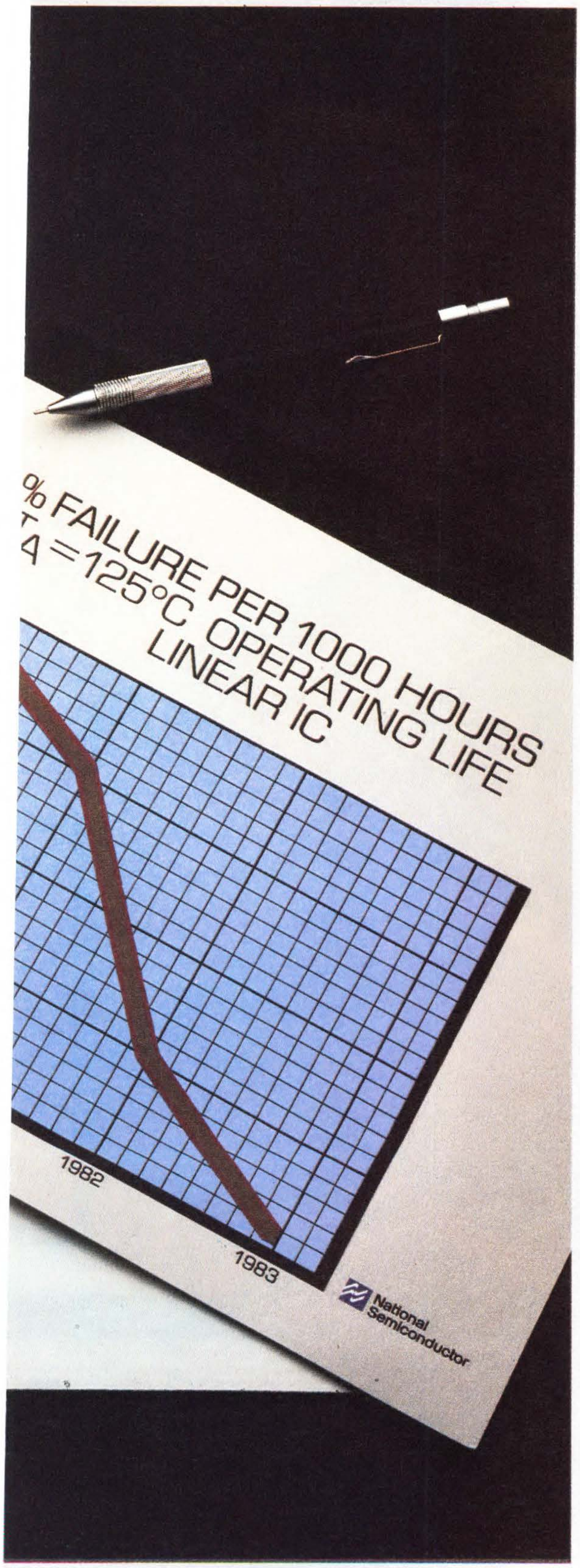


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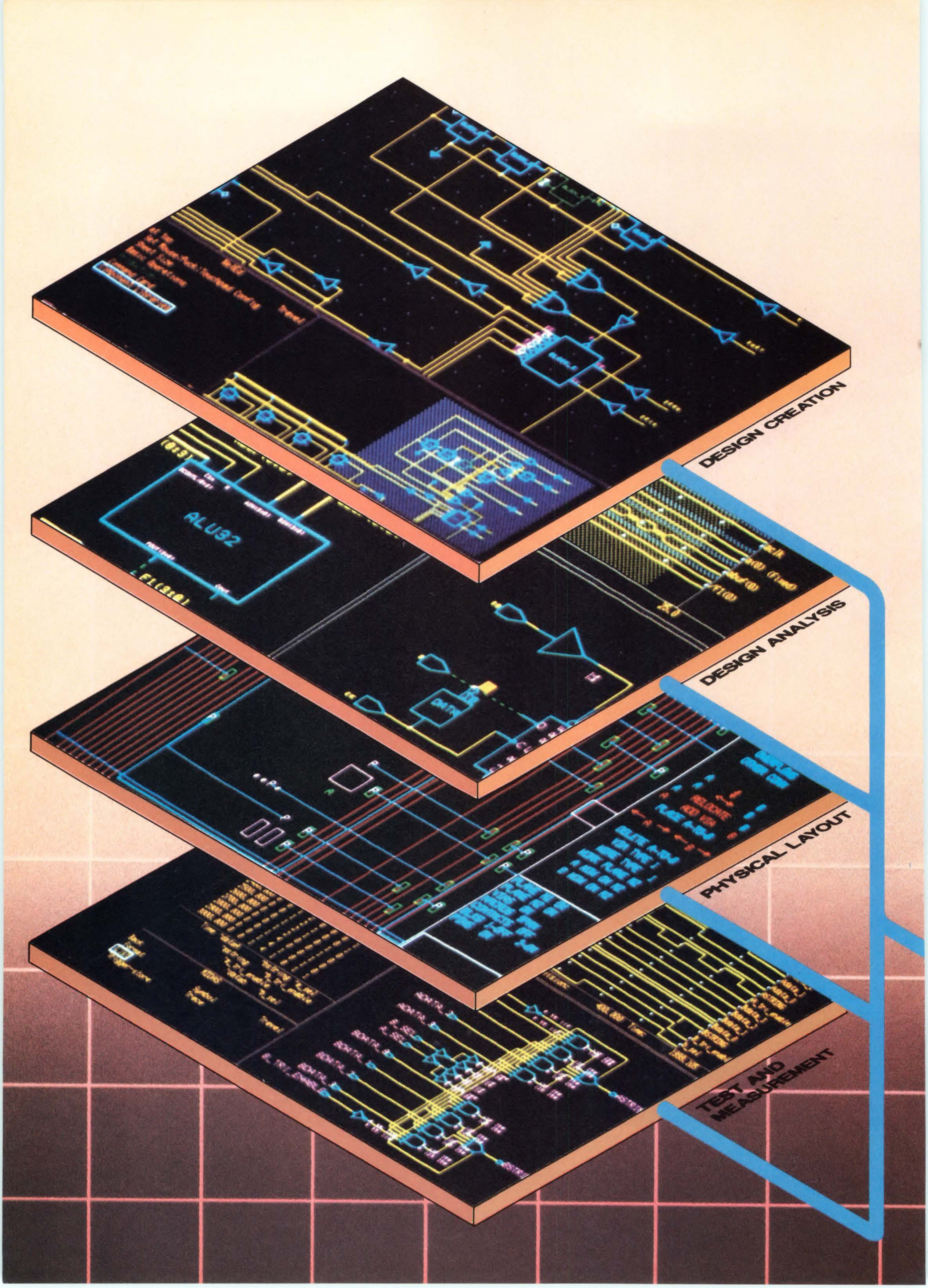
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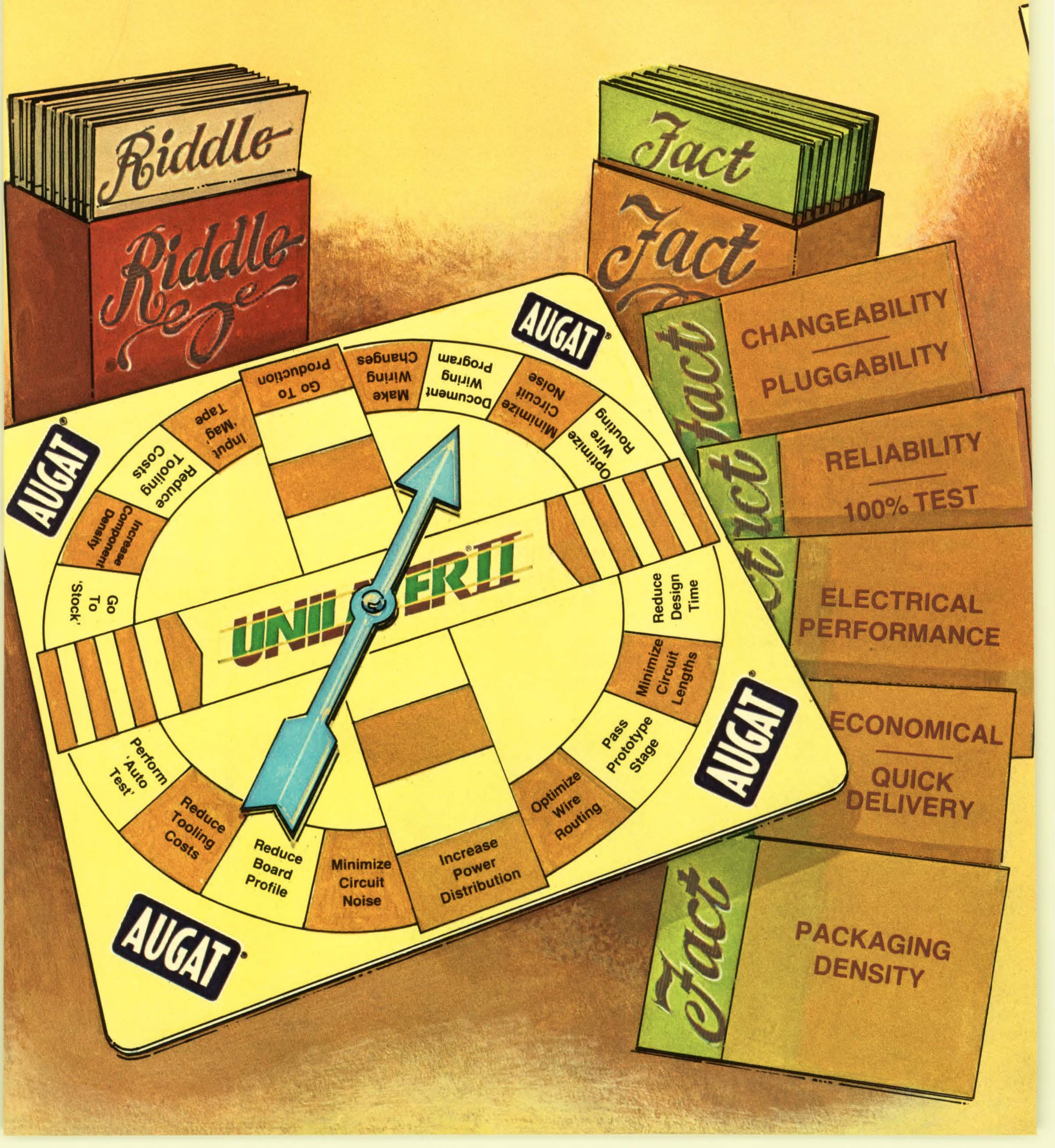

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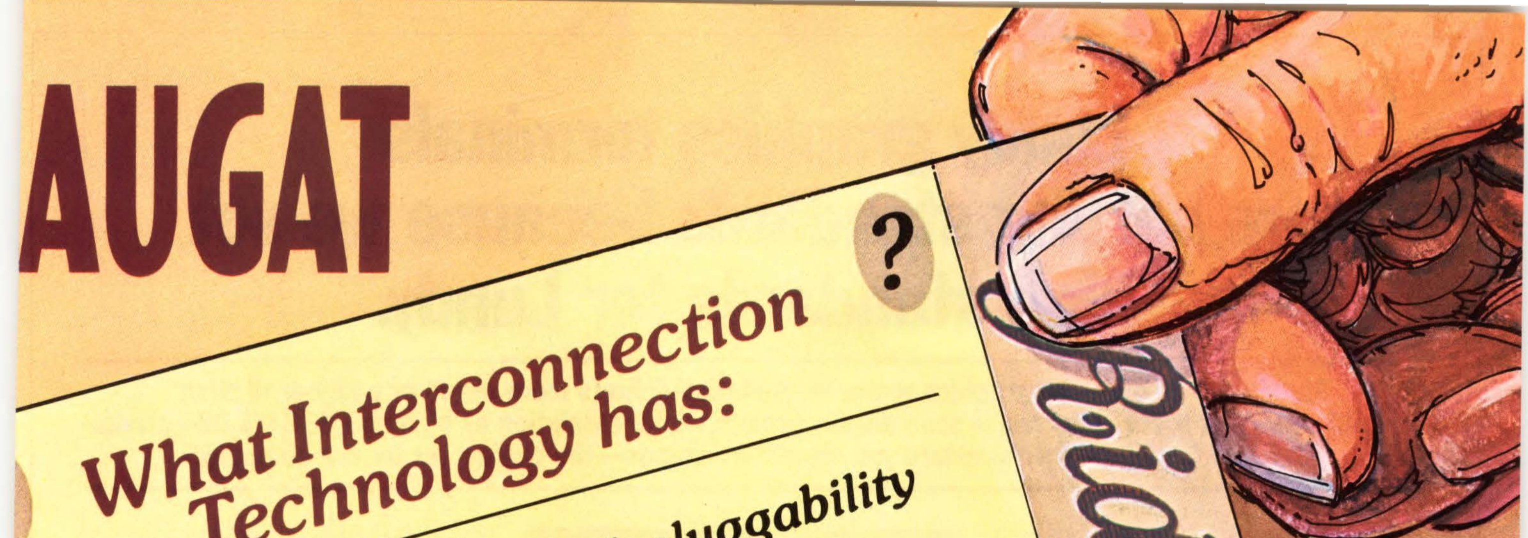


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# VIEWPOINT

# Better speech recognition means that computers must mimic the human brain

**Raymond Kurzweil**
President
Kurzweil Applied Intelligence
Waltham, Mass.

A year or so from now, Raymond Kurzweil's vision may well come true. A workstation subsystem will emerge that will enable users to run a word-processing program (or virtually any other software package) completely by voice—issuing commands and entering text. The system, which will recognize discrete words separated only by a slight pause, could tie into a PBX, letting several people log on and verbally enter their text.

The technology will draw on a number of artificial intelligence techniques that expressly mimic the human thought process. Though the system will be no more complex than other kinds of computers, its designer will have to know many subjects normally outside the area of computer science.

For example, building a natural-language processor —essential for this level of speech recognition—would require a basic understanding of how the human brain recognizes words. "But constructing a system that recognizes 10,000 words entails more than just understanding speech patterns," explains Kurzweil. "The machine would have to understand word sequence and linguistics."

"Some studies on auditory perception demonstrate how well or how poorly human beings understand speech when words are given to them in a sensible and a nonsensical order. In the latter case, auditory perception falls way down."

In other words, Kurzweil continues, people expect words to be presented in a certain order. Although the linguistical constraints of English are quite complex, he anticipates that computer systems will soon be able to "guess" the next word in a sentence. But to do that, the natural-language system must be parsing a sentence in real time as the text is verbally entered. Parsing looks at sentences in terms of syntactical structures, which specify, for instance, the noun and its modifier.

"That's how natural-language understanding works. You take a sentence, break it down into an internal representation, and extract the next level of meaning from it."

Even if a system can accurately predict the next word only from 300 or 400 possibilities out of a domain of 10,000 words, it still eases the burden of acoustic recognition," he says. "The fact is, we already have most of the necessary technology both soft-

**At 36, Raymond Kurzweil has an astonishing record in artifical intelligence. He has developed an optical scanner for the blind that can read any printed text aloud and is now working on a speech recognition system that will "understand" 10,000 words. Kurzweil is a graduate of the Massachusetts Institute of Technology.**

**Carole Patton**

ware and hardware, under our belt."

In the past the development of such intelligent speech recognizers has been hindered by a lack of appropriate parallel hardware and software. Both are vital, Kurzweil insists, since computational brute force is the major ingredient in many AI functions.

The traditional AI approach models systems and software after the human brain, a feat that has invited collaboration from researchers in other specialties (psychology, epistomology, and so forth). "The brain is highly parallel," Kurzweil says. "In human beings that parallelism makes up for the inherent slowness of nerve cells. We must replicate that parallel architecture in silicon."

To meet that demand, Kurzweil foresees "arrays of specialized subprocessors placed on a single chip, with each subprocessor tackling a particular computational action—like the steps involved in a fast Fourier transform or a logical inference."

In a short time, Kurzweil is confident that such systems will be integrated into data bases. "You'll be able to verbally ask your computer a complex question and get an immediate verbal answer.

"Looking a bit further ahead, these technologies might be applied to expert systems," he says. "But the fifth-generation computers will not be wide-ranging intellectuals. Rather, they will be 'idiot savants'—systems with extremely well-defined areas of expertise."

# Standard languages will give way to their adaptive kin

**Elizabeth Rather**

President
Forth Inc.
Hermosa Beach, Calif.

The second- and third-generation programming languages—Fortran, Cobol, Pascal, C, and Algol—are coming under attack from newer and more flexible languages like Lisp and Forth." So declares Elizabeth Rather. She gets right to the heart of the matter, emphasizing that "engineering software demands an adaptability to hardware and to special applications that is sadly lacking in the earlier, more structured languages."

**Ray Weiss**

The trends are quite clear. As more processors emerge, engendering greater numbers of applications, software systems must be rapidly developed for them. "What is obviously needed is a system that can shift easily among hosts, in turn allowing for effective interactive development." Older languages are too tightly defined and have led to a building-block approach to software development that depends on unwieldy discrete programs.

Counted among their ranks are operating systems, editors, compilers, link loaders, and debuggers—all large and complex programs that eat up a great deal of a computer's resources and overhead. "They are stand alone entities designed to handle all possible combinations of Data, Input and software processor state. But their complexity alone hampers software development and limits their transportability."

In contrast, Forth integrates a high-level language with development tools, utilities, and an operating system. Such integration allows software to be tailored to system needs. As an example, instead

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## VIEWPOINT

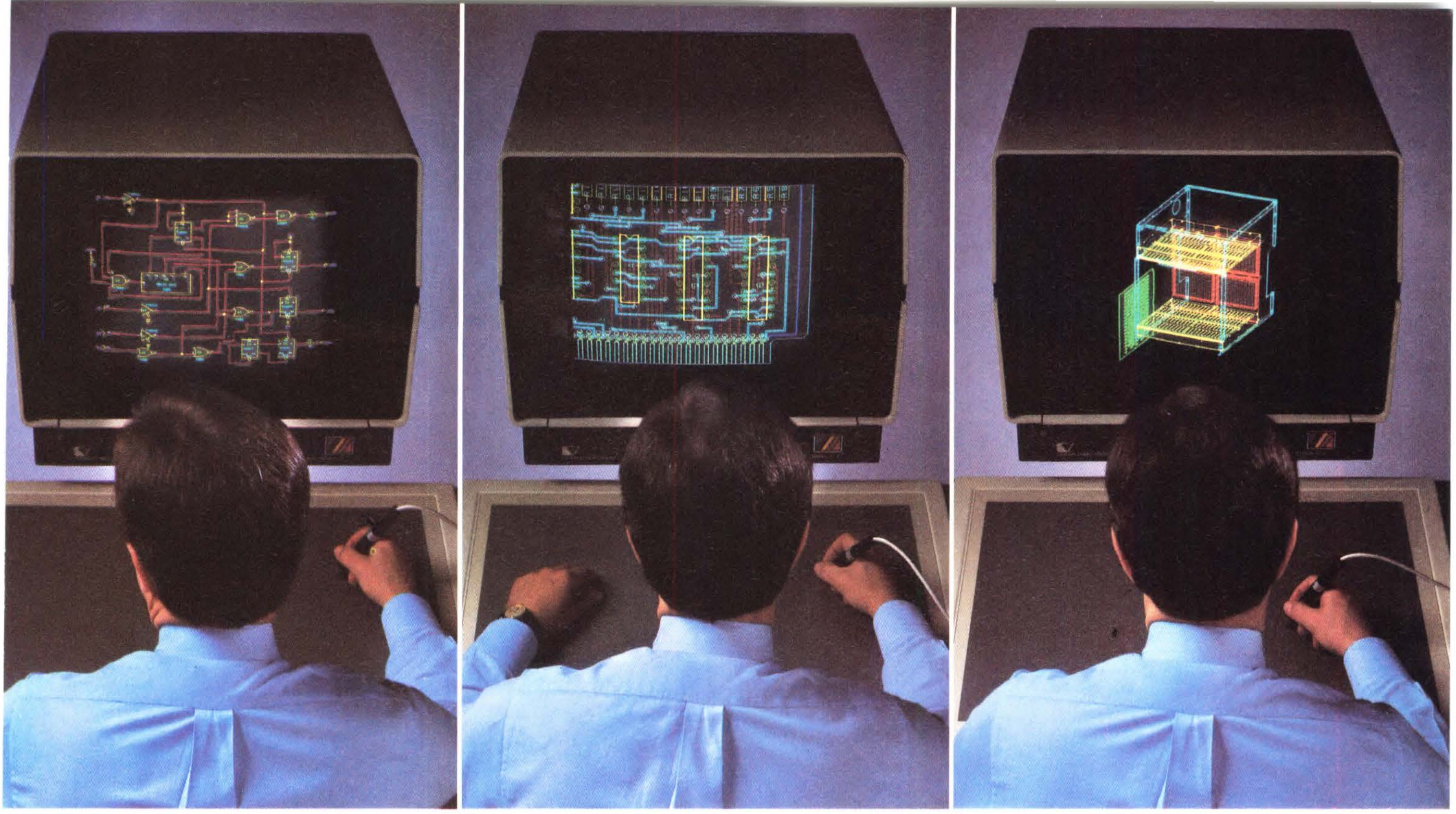
of considering the operating system as a fixed and static entity that can be moved to other hosts only with great expense and difficulty, an OS constructed in a language like Forth can be designed incorporating only those functions required by the target system, thus minimizing overhead.

"Adaptive languages," she explains, "start out with what we call a 'naked' computer. The language and particular software features are added as needed." That minimizes memory requirements, increases speed, and simplifies programming. For instance, a Forth system comprising a multitasking, multi-user operating system—complete with an interpreter-compiler and an assembler—can fit into only 8 kbytes of memory. Moreover, such software code can easily be moved from a development system with many resources to a target system.

"Forth will come into its own as 32-bit microprocessors become more common," Rather predicts. Already, Forth is available for the NCR 32-bit chip set as well as for Motorola's 68000 family.

"For applications like remote control, instrumentation, and data acquisition," she says, "the portability, compactness, and speed of adaptive languages will make them king of the hill."□

**Elizabeth Rather is the cofounder of Forth Inc. Before starting the company, she worked as a senior programmer for the National Radio Astronomy Observatory and the Kitt Peak National Observatory.**

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7912AD Programmable Digitizer

# The most familiar thing about waveform digitizers is the name on the best of them.

**At Tektronix, part of the job of making the best waveform digitizers in the world is making the world of waveform digitizing less formidable.**

Digital technology may simplify many kinds of measurements. But it does nothing to help you evaluate your own needs or to compare one waveform digitizer to another.

If you feel you're in unfamiliar territory, you'll find Tek a welcome landmark. For years, we've been building on our expertise in analog technology and microprocessor design to develop an extraordinarily diverse line of waveform digitizers... from manual operation to fully programmable, with frequency response from dc to 14 GHz for repetitive data, or dc to 500 MHz for single-shot measurements.

At the same time, we've developed the experience to get the right instrument into your hands.

**Of this you can be sure: a digitizer is no better than its interface with the analog world.** Tek digitizing instruments incorporate signal acquisition and conditioning capabilities that define the state of the art. No one offers greater accuracy and versatility for capturing such a wide range of signals.

**We'll show you features unique to digitizers—many unique to Tektronix—that are particularly suited to your signal capture and analysis needs.** Features like pretrigger viewing. Envelope mode for recording signal variations. Signal averaging, to minimize the effect of noise. Roll mode, for a continual view of incoming signals. Powerful storage, comparison and manipulation of signals. Signal processing, with digital readout of results. Up to 10-bit vertical resolution and many other high-performance characteristics.

Of course, waveform digitizers let you interface, via GPIB, to external data processing and output devices. Tek Standard Codes and Formats vastly simplifies the interfacing task, and assures consistent and compatible operation among all your GPIB instruments.

**Count on Tek to keep the digital world as familiar and friendly as you want it to be.** Whether you choose an evolution as simple as adding a digital plug-in to your existing Tek 7000 Series or 5000 Series mainframe, or as sophisticated as a complete Tek Signal Processing System, you'll find the waveform digitizing world well within Tek's domain.

**For a copy of Tek's Digital Storage Selection Guide, contact Tek or your local Tek sales representative.**

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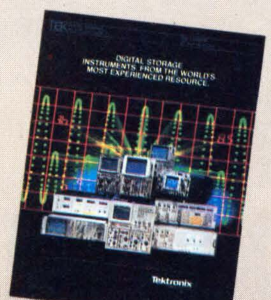


Tektronix
COMMITTED TO EXCELLENCE

CIRCLE 52

# "Who else could squeeze 512 analog input channels on 2 MULTIBUS™ boards? Or even 128 channels on one? We've done both."

Try this on for size.

Data Translation's new DT712 has 128 analog input channels. More than any other A/D board on the market. Add the DT713 to get 512 inputs.

Engineers faced with a lot of analog sensor inputs no longer have to add on a ton of extra boards for industrial process control applications.

Now all they need is one. Ours.

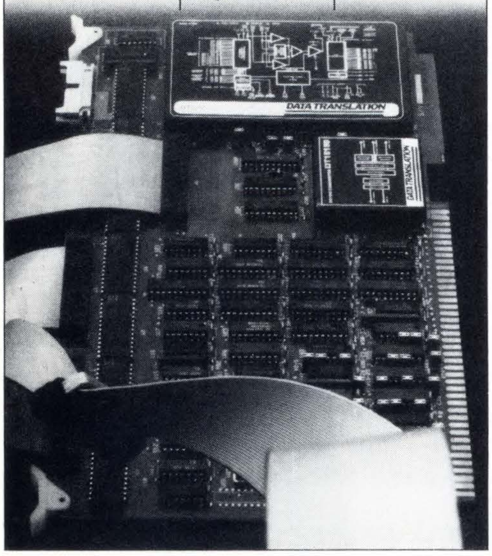
The DT712 is also extremely economical. With more channels, the cost per channel is at least a third less than anything the competition can offer.

Besides greater cost efficiency, the DT712 also includes multiple triggering and scanning schemes, and an on-board programmable clock. Plus, a unique screw terminal panel lets you enjoy easy installation of analog signals, and a very clean, noise-free cabling connection.

Fred Molinari, President

**DT712 SERIES A/D BOARD DESCRIPTION**

| MODEL | TYPE | MAX NUMBER OF CHANNELS |
|---|---|---|
| DT712 | High Level A/D | 128SE/64DI |
| DT712 + DT713 | High Level A/D Expanded | 512SE/256DI |
| DT714 | Low Level A/D | 64DI |
| DT714 + DT715 | Low Level A/D Expanded | 256DI |




The DT712 provides for up to 128 A/D channels on a single MULTIBUS board.

And the DT712 is compatible with the latest MULTIBUS interface... including 24-bit addressing and 16-bit data transfers.

So before you get into a tight spot, call Data Translation.

We've loosened up the input problem 512 ways.

**Call (617) 481-3700.**


See our 192 pg. new product supplement in Gold Book 1984, Vol. III, and our 336 pg. catalog/handbook in Gold Book 1983.

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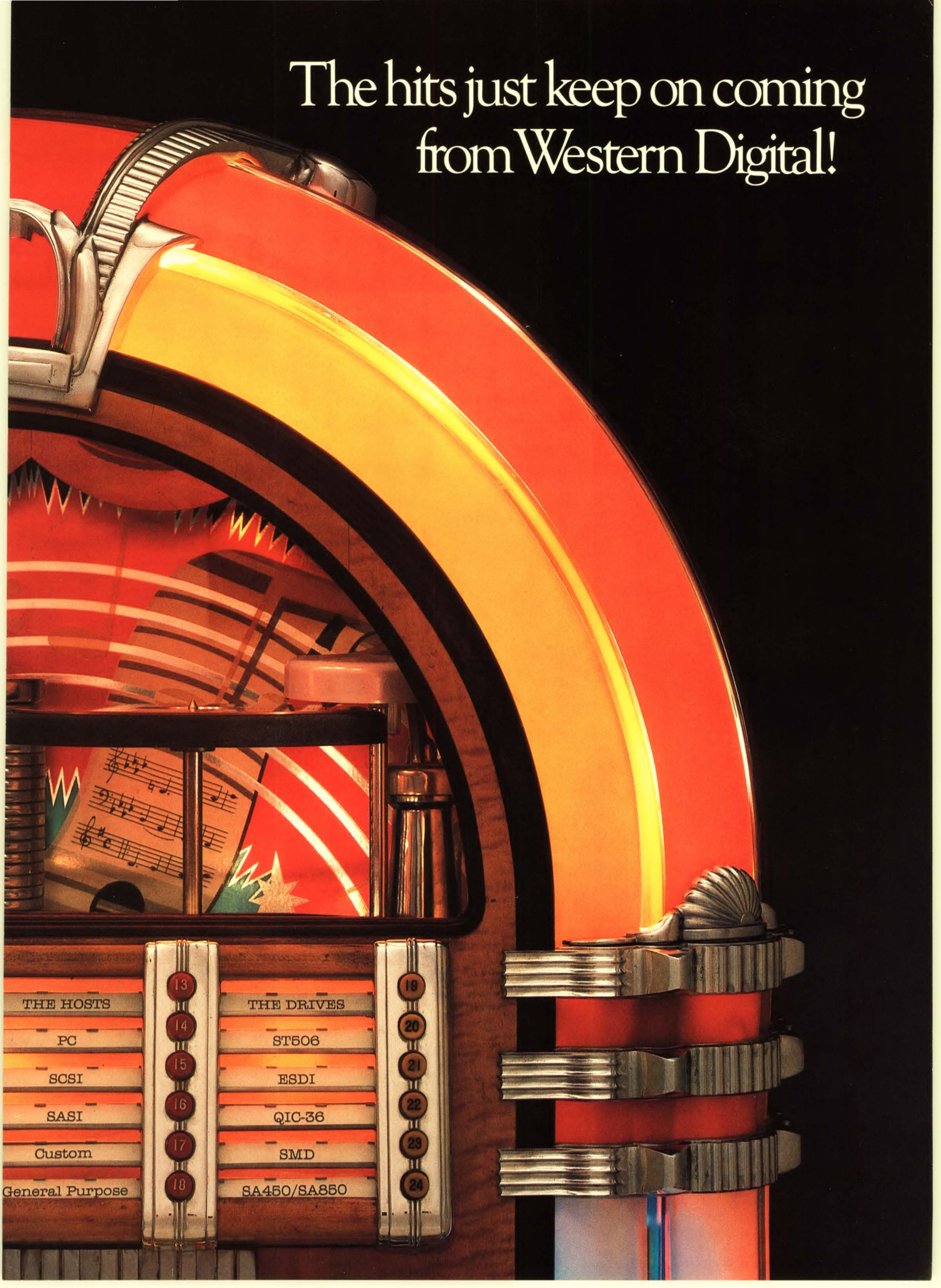
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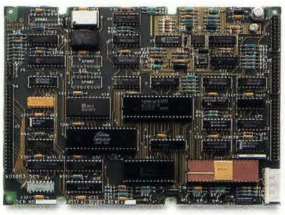
# Introducing the disk and tape

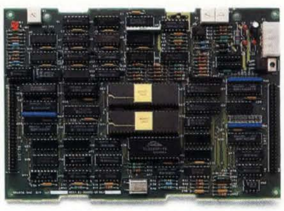

We're first with the most and latest with the greatest. And we've got a Jukebox full of new selections to speed and simplify your system design.


WD2010

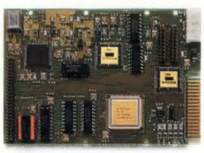

WD277X



WD1003-SCS



WD1036-SHD



WD1002S-SHD

Introducing WD2010, a new VLSI Winchester controller with ECC, auto correction and 2048-cylinder addressability.

Introducing WD1003-SCS, first of a new generation of high-performance board-level controllers. Based on the WD2010. And featuring a full SCSI interface for your multi-user systems.

Introducing WD1002S-SHD. VLSI, surface mount technology and special gate arrays have enabled us to pack a SASI:ST506 controller into a 3½″ form factor.

Introducing WD10C20, a VLSI self-adjusting data separator in CMOS.

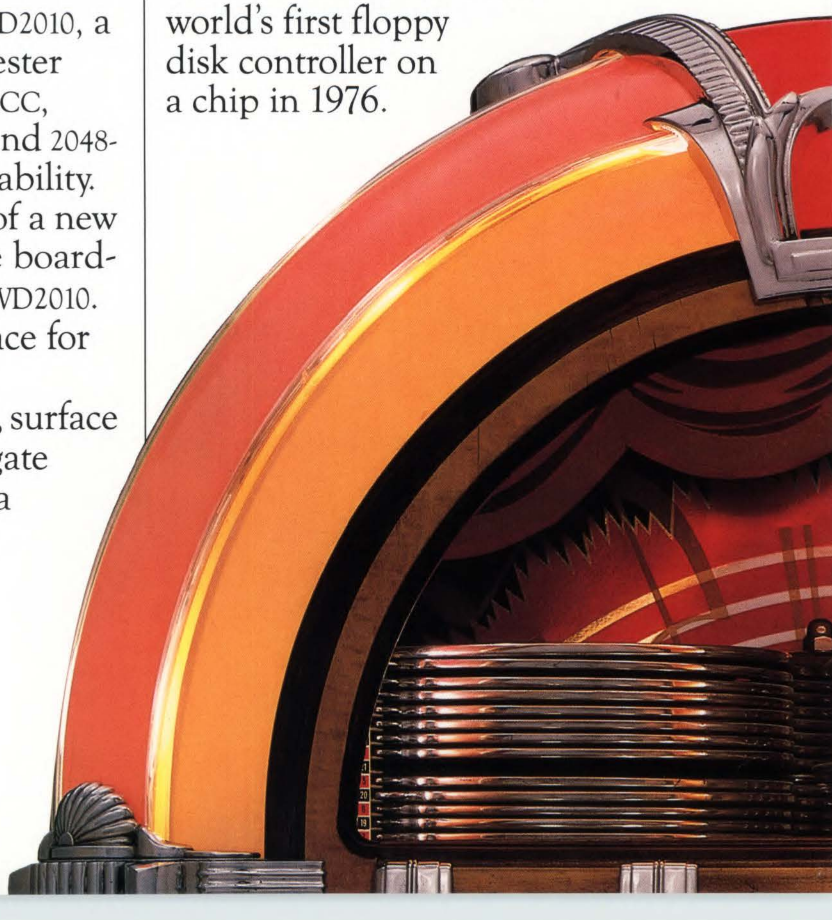
Introducing WD1036-SHD, a new SASI:QIC-36 tape controller. Based on our new WD2400 chip set. Sure to help make ¼″ streaming tape a chart-buster.


*Select one of our off-the-shelf controllers. Or have us customize one for you.*

Introducing WD277X, the newest generation floppy disk VLSI controller, with on-board analog data separation.

**Hits on silicon.**

We've been at the top of the charts since we introduced the world's first floppy disk controller on a chip in 1976.



# #1 hit parade of controllers.

Proprietary VLSI is still our most powerful advantage. It gives us the edge by enabling us to control the technology, cost and future of our products.

*Floppy, Winchester and ¼" tape — we've got controllers for all your storage needs.*

Today we're developing new VLSI at a rapid rate, achieving higher levels of integration, migrating into CMOS and shrinking into SMT packaging.

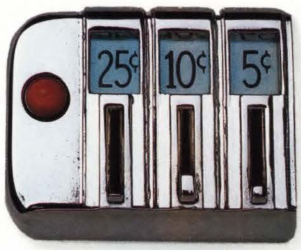
**We're playing your song.**

If our new product introductions don't give you precisely the *host:drive* combination you need, check our other selections.

Take our WD1002-WX2 board for example. PC compatible.

With a menu of options to match your system's personality. Plus room on board to add extra memory, data privacy or other unique features.

Or we can design and build a board just for you. Our CAD capability enables us to quickly adapt standard products to your custom needs. Our automated manufacturing capability gets you product in a hurry. Our worldwide Technology Centers and field engineering team speed system integration. And make you feel like dancing.



*We deliver cost-effective, applications-driven solutions with just the right set of features.*

**Punch our number.**

Call our Hit Parade Hotline, 714/863-7827, and we'll rush you details on all of our new floppy, Winchester and tape controllers. Better yet, drop by our booth #658 at COMDEX and see each of these important new products.

**WESTERN DIGITAL**
CORPORATION

## A FEW OF OUR STORAGE MANAGEMENT PRODUCTS

| | Part Number | Technical Information | Power Requirements | Package Size | Product Description |
|---|---|---|---|---|---|
| FLOPPY DISK CONTROLLER DEVICES | WD177X | Single chip | +5V | 28 pins | FD179X functionality with built-in digital data separator and write precompensation. |
| | FD179X | Single chip | +5V, +12V | 40 pins | Single/double density, IBM compatible. |
| | WD277X | Improved data separation | +5V | 40 pins | WD279X with improved data separator. |
| | WD279X | Integrated data separator | +5V | 40 pins | FD179X with built-in analog data separator and write precompensation, single/double density, and internal clock divide. |
| WINCHESTER DISK CONTROLLER DEVICES | WD1010 | 5MHz | +5V | 40 pins | 5.25″ and 8″ Winchester controller chip. |
| | WD1050 | Single chip | +5V | 68 pins | SMD controller. |
| | WD2010 | 5MHz | +5V | 40 pins | WD1010 with ECC. |
| WINCHESTER DISK SUPPORT DEVICES | WD10C20 | CMOS | +5V | 28 pins | Data separator, and write precompensation device compatible with the WD1010 and WD2010. |
| | WD1015 | Single chip | +5V | 40 pins | Winchester buffer manager control processor. |
| | WD11C00-13 | Single chip | +5V | 20 pins | ECC support device compatible with the WD1010. |
| WINCHESTER BOARD PRODUCTS | WD1002-05/HDO | Board | +5V | 5.75″X8″ | 5.25″ Winchester/floppy controller board with ECC. HDO Winchester only. |
| | WD1002-SAS | Board | +5V | 5.75″X8″ | WD1002 Winchester/floppy with SASI interface. |
| | WD1002-SHD | Board | +5V | 5.75″X8″ | WD1002-SASI interface – Winchester only. |
| | WD1002S-SHD | Board | +5V | 5.75″X4″ | 3.5″ form factor of 1002A-SHD. |
| | WD1002-WX2 | Board | +5V, −12V, +12V | 3.85″X13″ | WD1002 with IBM PC compatible interface – Winchester only. |
| | WD1003-SCS | Board | +5V | 5.75″X8″ | 5.25″ Winchester controller board with SCSI interface. |
| TAPE DRIVE CONTROLLER PRODUCTS | WD2401 | Single chip | +5V | 40 pins | Motion control & buffer manager |
| | WD24C02 | Single chip | +5V | 40 pins | Read/write formatter |
| | WD1036-SHD | Board | +5V, +12V | 5.5″X8″ | ¼″ tape controller (SASI:QIC-36) |
| | WD1036-WX2 | Board | +5V, +12V | 3.85″X13″ | ¼″ tape controller (IBM PC/XT:QIC-36) |

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The hits just keep on coming!

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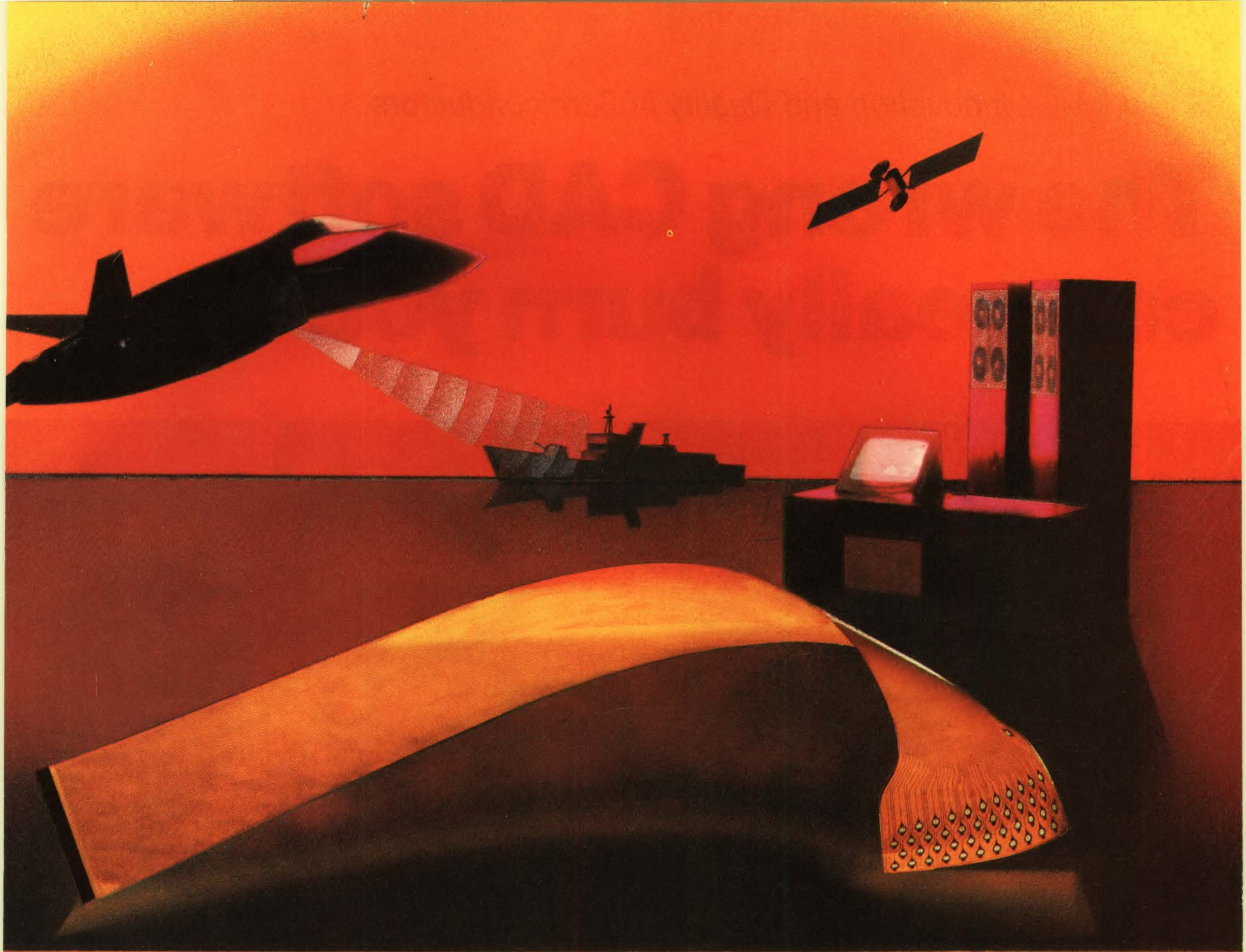

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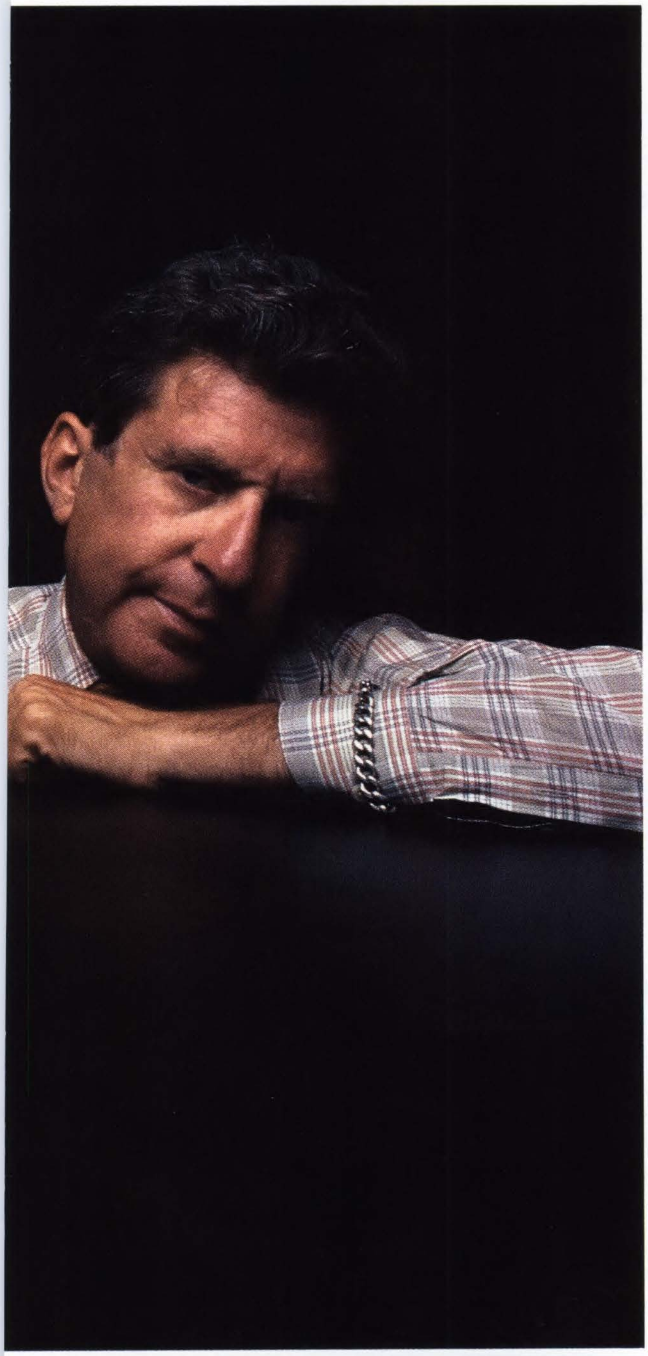

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# Tree-structured network realized in hardware sets 50,000 'talking'

*Among the first hardware-based networks to employ a tree structure is one that clips along at more than 160 Mbits/s.*

Though tree structures are deeply rooted in the software community, until recently they have not taken a firm hold in hardware. One of the first tree-structured networks implemented in hardware employs serial fiber-optic links to connect nodes and handles 50,000 users. Centrenet works with parallel packet-switched nodes to give an overall data throughput of better than 160 Mbit/s. At that speed, it clocks in as one of the fastest existing networks.

The system, from Manchester University (England), is organized into computing clusters, called starpoints, that may be located several kilometers apart. It uses non-return to zero inverted (NRZI) encoding. End-to-end handshaking on all links allows them to operate at different speeds, and the tree structure distributes the total bandwidth throughout the links and clusters so that every user is guaranteed a 10-Mbit/s link.

Each starpoint is a 16-port parallel switch with 15 downlinks and one uplink. The ports are housed on single boards (at the moment, a triple-height Eurocard, but this could be reduced fairly easily to a double-height card). Other boards act as interfaces to processors, to groups of terminals, or to interconnecting links. The cluster fits readily into a single standard rack.

**Mitch Beedie**

### Directing traffic

A cluster routes a packet from its source to destination according to a 4-bit address in the destination address field. At a node on the lowest (third) level of the hierarchy, packets are routed from port to port according to the values of the 4 least significant destination address bits. The 12 most significant address bits must correspond to the address of the node. If the MSBs do not match up, the packet is sent over an uplink to the next highest node.

At that point, bits 4 through 7 of the destination field are used to route the packet (again, as long as the remaining MSBs agree with the node's address). This configuration ensures that there is only one route between any two linked devices. It also makes certain that a packet travels the shortest distance possible—only as far up or down the hierarchy as is needed to reach its destination.

### The brains of the outfit

Routing between clusters is via a 72-bit parallel bus, and packets can be put into slots every 200 ns. Each starpoint is fitted out with a Z80-based network intelligence module. Among other duties, it takes care of initialization, error recovery, and polling. The uplink, downlinks, and intelligence module are polled round-robin style, using a 17-state counter. Each card receives a unique polling signal. The actual polling order is established by and can be changed by the intelligence module to yield adaptive polling.

A single port may transmit a packet every 2.5 $\mu$s, and transmissions may be overlapped, in turn establishing a data rate above the specified 160 Mbits/s. Most transmissions will connect two downlinks. If a downlink tries to access an uplink that is already in service, the transmitting link will continue in its attempt a specified number of

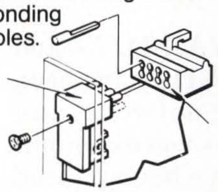
# The KM6 Subrack System will never be complete...

## The KM6 Subrack System has always been years ahead of its time

## 1981

### Polarising/PCB Mounting Bracket

Secured to front panel or direct to PCB. Mating half fitted to front of PCB guide during assembly. Polarisation by breaking spills and filling corres ponding holes.



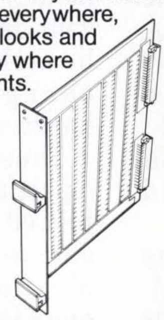
### Security PCB Retainer

Ensures PCB's stay electrically mated to connectors within sub rack. Easily assembled. Prevents PCB's becoming disengaged even in vibrative environments.

## 1982

### Front Panels

An increased variety of front panels for PCB mounting. Just look around . . . you'll notice them everywhere, good looks and quality where it counts.



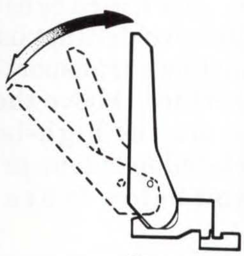
### Horizontal Mounting Kit

Horizontal Mounting Kit accommodates any size of PCB within width of card frame.

## 1983

### PCB Ejector/ Injector

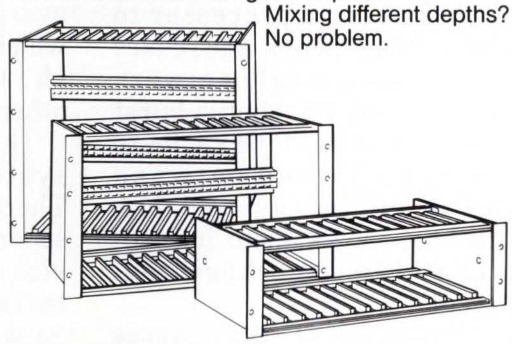
Unique saddle operated Injector/ Ejector means increase in number of connector contacts without difficulty of inserting and retracting PCB's from subrack. Unit operates within confines of subrack, utilising normal front panels, hinged or otherwise.



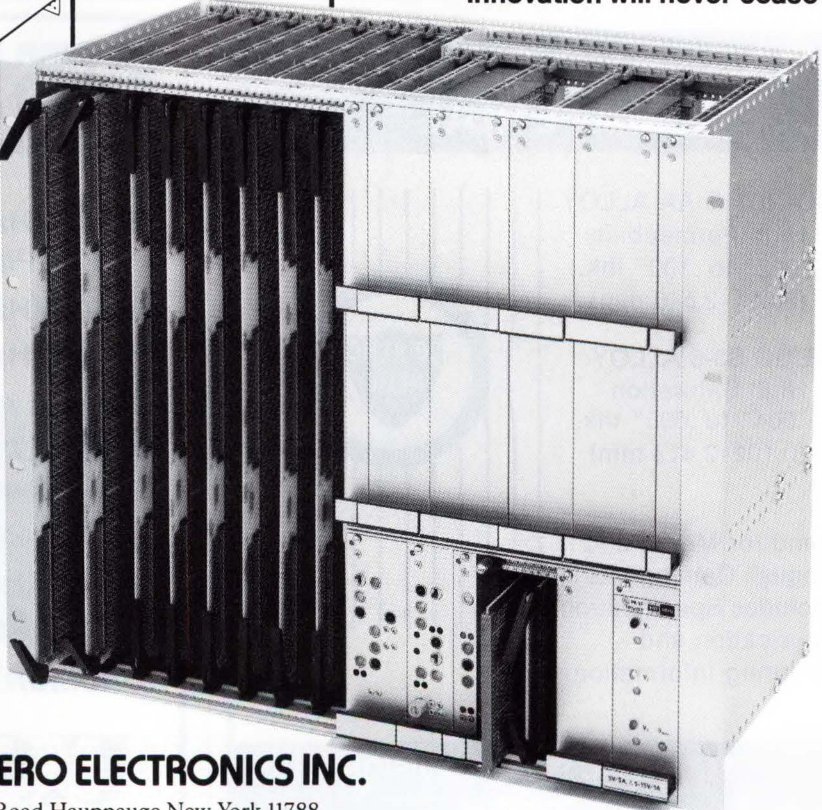
## 1984

### 9U KM6. Flexibility in Packaging Triple High Eurocards

Anticipating packaging needs has always been our strong point.
KM6 is now available in 9U heights for those who need the extra 'real estate' a triple high Eurocard offers.
Needless to say you can also mix single and double Eurocards along with triples.
Mixing different depths? No problem.



**It will never be complete because our programme of improvement and innovation will never cease . . .**



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**Leaders in packaging technology**

CIRCLE 56

## INTERNATIONAL NEWSFRONT

times. If it does not succeed, within a specified number of tries, an error is reported to the intelligence module, and the packet is discarded.

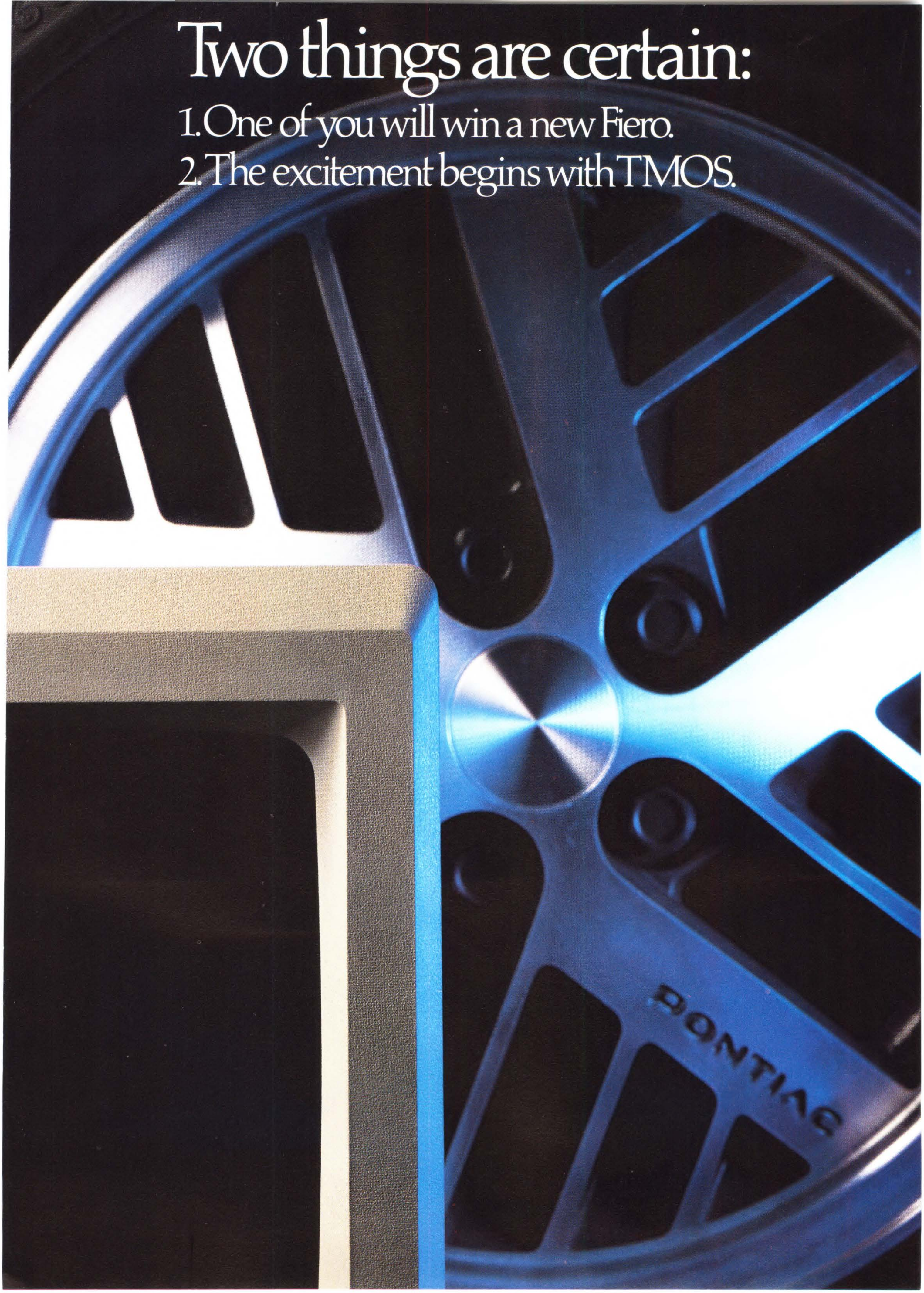
**Packing the packets**

Computers are hooked into the clusters by a so-called superport, which makes it possible for a processor to have 16 network addresses with just a single network connection. Further, a burst mode allows up to 64 kbytes to be transferred between superports—using DMA techniques—without individual end-to-end acknowledgments.

Every packet that passes through the system carries two 16-bit address fields—one for the transmitting, the other for the receiving station. They are followed by a 32-bit data field and an 8-bit control field. The last is mainly used for handshaking the packets across the network. A packet's overhead is thus 40 bits, giving the system an overall efficiency of 44.4%, which is comparable to that of the Cambridge Ring and other popular networks.

The protocols used in the system are hierarchical: There are two distinct bands separated by a transport service interface. Above the interface are the high-level, network-independent protocols, and below it are the network-dependent protocols. Such strict division permits the higher-level protocols (equivalent to layers 5 through 7 of the ISO's Open Systems Interconnection model) to be based on a single, well-defined interface and to be isolated from low-level changes in software and hardware.

Thus far a VAX-11/750 and a pair of PDP-11s have been joined to the network, and data as well as voice communications have been passed over it. Work currently is under way to build an Ethernet and an IEEE-488 interface, and, future capabilities call for the network to transmit video signals.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1. One of you will win a new Fiero.
2. The excitement begins with TMOS.
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Imagine a brilliant new 1985 Fiero SE by Pontiac in your garage.

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The stylish, sporty Fiero is the first mid-engine car in the world to use a space-frame chassis—a bold benchmark in automotive engineering. Its unique design concepts, gleaned from race-car designs, have caught on with everyone interested in advanced, mass-produced American cars.

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### Look how complete the line is.

Over 400 TMOS types comprise the broadest offering available.

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During October, November and December, we're guaranteeing you 10% off any other source's equivalent device quote or invoice.

Take any bona fide supplier's invoice or quote up to 30-days old to a Motorola factory representative and if it's for any of the 727 types we second-source, he'll duplicate the order and/or quote at 10% less. Guaranteed.

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**Five 3rd Prizes:** Macintosh Personal Computers plus up to $500 of software and accessories.

**Five Additional Prizes:** Macintosh Personal Computer plus up to $250 of software and accessories.

All entrants will receive the official TMOS Design Contest entry package of free TMOS Data Book, contest rules, free sample offer, brochure, price list, and a handy new TMOS slide-chart Selector Guide.

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Let the excitement build.

We're on your design-in team.



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**Please send me your Official TMOS Design Contest Entry Kit.** 211ED111584


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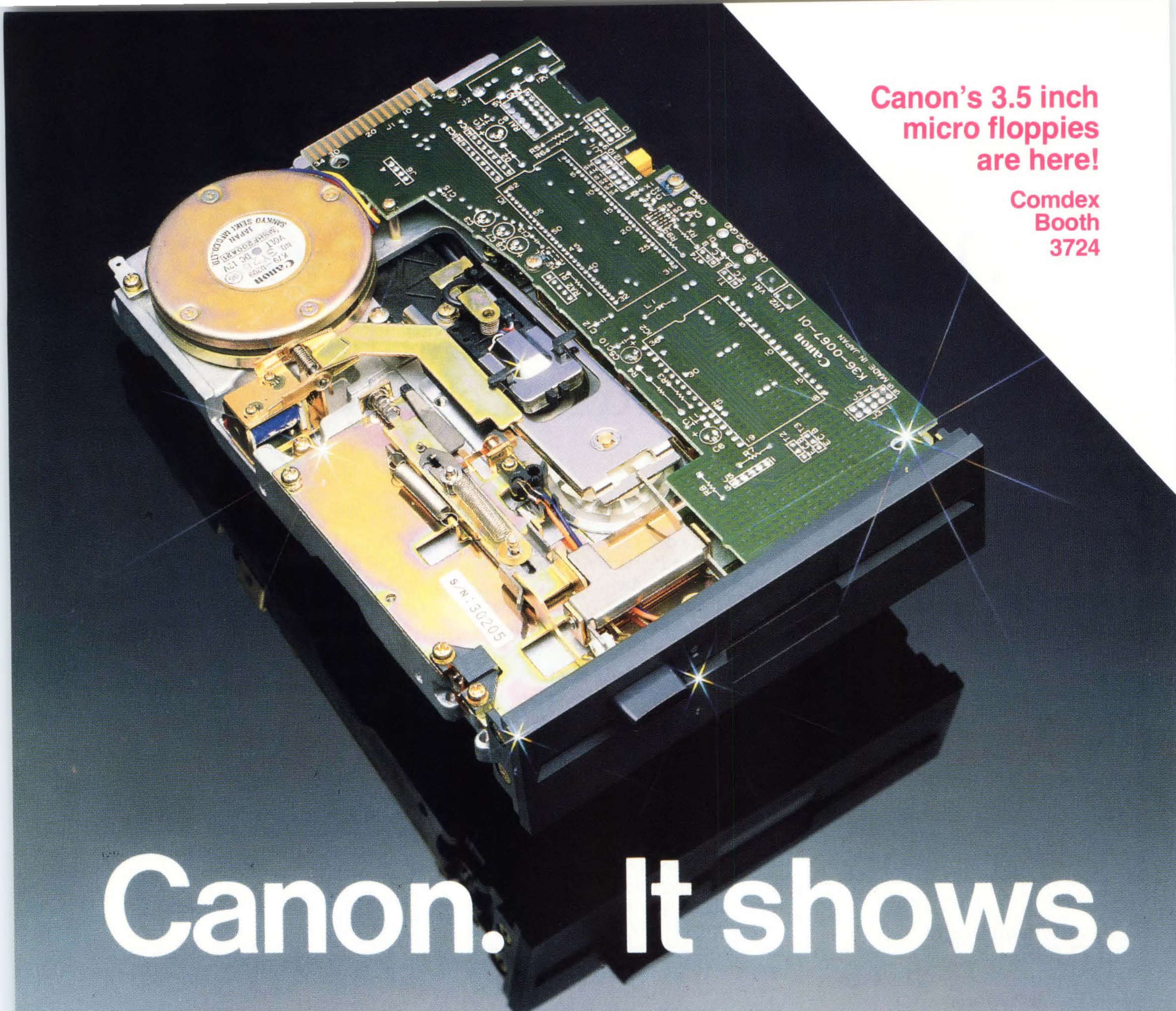
Title ____________________

Company ____________________

Address ____________________

City __________ State ______ Zip ______

Call me ( ) ____________________




One look at a Canon floppy disk drive — and hearing its silence while seeking — tells you it's made by masters in the art of designing and manufacturing ultraprecise miniature mechanisms.

A second look would reveal some unique features: Pushbutton clamping...disk is clamped — and ejected 10 to 20 mm — by pushing the same button, which is locked while the heads are loaded. Steel belt head positioning, for outstanding accuracy. Soft landing mechanism in the head loading system, and thin R/W heads (tested beyond 10 million taps), to minimize head and media wear.

Canon drives were designed originally for 96 TPI; the 48 TPI versions therefore have that added reliability.

| | |
|---|---|
| **Single Drives:** | MDD 221: 96 TPI, double sided/density, 1 Mbyte.*<br>MDD 211: 48 TPI, double sided/density, .5 Mbyte.* |
| **Dual Drives:** | MDD 423: 96 TPI, double sided/density, 2 Mbyte.<br>MDD 413: 48 TPI, double sided/density, 1 Mbyte. |

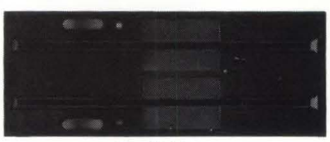
Let Lee Heller tell you more. Call him at (516) 488-6700, Ext. 4958. Or write to him at Canon U.S.A., Inc., Disk Drive Division, One Canon Plaza, Lake Success, NY 11042.

## Canon drives. More flexible up front.

Our drives are available with the bezels shown — or with no bezel at all, so that you can determine your own packaging design.


33.5 mm bezel


Standard half-height bezel


Dual drive:
Standard 2/3 height (57.5 mm) bezel


Dual drive:
Standard full height bezel

Canon

* *Recognized under the Component Program of Underwriters Laboratories Inc.*

CIRCLE 59

# INTERNATIONAL MEETINGS

**11th International Conference on Microelectronics, Nov. 13–15.** Congress Center, Munich, West Germany. Münchener Messe- und Ausstellungs GmbH, Knogressburo Mikroelektronik '84, Postfach 12 10 09, D-8000 Munich, 12 West Germany; (089) 51 07-371.

**China International Microelectronics/Computer Exhibition and Conference, Nov. 21–26.** Shanghai, People's Republic of China. Harry C. Lepinske, China International Microelectronics/Computer Exhibition and Conference, American Exhibition Services International Inc., PO Box 66373, O'Hare International Airport, Chicago, Ill. 60666; (312) 593-2462.

**International Spectrum Pacific, Nov. 21–23.** Centrepoint Exhibition and Conference Center, Sydney, Australia, Vic Sergie, IDBMA, PO Box 77, Gymea, NSW 2227, Australia; (02) 570-5505.

**The Northern Computer Fair, Nov. 22–24.** Belle Vue, Manchester, England. Reed Exhibitions, Surrey House, 1 Throwley Way, Sutton, Surrey, England; (01) 643-8040.

**Systemotronica '84, Nov. 22–30.** Moscow, USSR. Harry C. Lepinske, Systemotronica '84, American Exhibition Services International Airport, Chicago, Ill. 60666; (312) 593-2462.

**Computer China, Nov. 25–Dec. 1.** Xiamen Special Economic Zone, People's Republic of China. Kallman Associates, 5 Maple Court, Ridgewood, N.J. 07450; (201) 652-7070.

**International Spectrum Europe, Nov. 26–27.** Penta Heathrow Hotel, London, England. Chris Holman, IDBMA, PO Box 32, Northwood, Middx. HA6 1HZ, England.

**Transducer Tempcon '84, Nov. 27–29.** Harrogate Exhibition Centre, Yorks., England. Trident International Exhibitions Ltd., 21 Plymouth Road, Tavistock, Devon PL19 8AU; 0822 4671.

**Electronic Displays '84, Nov. 28–30.** Kensington Exhibition Centre, London, England. Networks Events Ltd., Printer Mews, Market Hill, Buckingham MK18 1JX, England; (0280) 815226.

**Conference on Computer-Aided Engineering, Dec. 10–12.** Univeristy of Warwick, Coventry, England. IEEE Conference Services Department, Savoy Place, London WC2R 0BL; (01) 240 1871.

**Fifth Generation and Supercomputers, Dec. 11–13.** Rotterdam, the Netherlands. Prof. R. P. van de Riet, Free Univeristy, Amsterdam, the Netherlands.

**Micro-Computer '85, Jan. 29–Feb. 3.** Frankfurt, West Germany. Philippe Hans, German American Chamber of Commerce, 666 5th Ave., New York, N.Y. 10103; (212) 974-8856.

**Middle East Electricity and Electronics Exhibition, Feb. 2–6.** Jeddah Expo Center, Kingdom of Saudi Arabia. Len Bennett, Logistics, 237 Park Ave., 21st floor, New York, N.Y. 10017; (212) 551-3530.

**AFIPS–Asia '84, Feb. 14–March. 2.** m.v. World Wide Expo, Tokyo, Osaka, Kitakyushu, Taipai, Hong Kong and Singapore. AFIPS, 1899 Preston White Drive, Reston, Va. 22091; (703) 620-8926.

**Autotech Hong Kong '85, March 7–8.** Hong Kong. Autotech Hong Kong '85, Hong Kong Productivity Center, 12th floor, World Commerce Center, 11 Canton Road, Tsimshatsui, Hong Kong; 3-7235656.

**Componentes Electronicos '85, March 12–15.** Mexico City, Mexico, March 19-22, Guadalajara, Jal., Mexico. Raquel Polo, United States Trade Center, Liverpool 31 Col., Juarez 06600, Mexico, D.F.; or PO Box 3087, Laredo, Texas 73044.

**The Scottish Computer Show and Conference, March 12–14.** Anderston Exhibition Centre, Albany Hotel and Holiday Inn Hotel, Glasgow, Scotland. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TWI 3SZ, England; (01) 891-5051.

# The Hitachi CMOS 6300 Family—8-Bit, Single-Chip Microcomputers

## The Real Performance Leader

The 63B01 offers you a powerful CPU and high-speed operation for systems requiring complex and fast data processing. Here's how it compares with the 80C51.

## Benchmark Study

| | Execution Time (μs) | | Code Efficiency | |
|---|---|---|---|---|
| | 63B01 | 8051/80C51 | 63B01 | 8051/80C51 |
| XTAL (MHz) | 8 | 12 | 8 | 12 |
| Instruction Cycle Time (μs) | 0.5 | 1 | 0.5 | 1 |
| **TASK** | | | | |
| Binary Multiply | 39 | 42 | 37 | 43 |
| Bit Manipulation | 6.5 | 6 | 8 | 8 |
| Logical Operations (AND/OR) | 7 | 3 | 11 | 6 |
| Nibble Comparison | 11 | 12 | 29 | 29 |
| Interrupt Processing | 11.5 | 21 | 1 | 19 |
| **TOTALS** | **75** | **84** | **86** | **105** |

Execution time for the 6301 ranges from 0.5 μs (2 MHz) to 1 μs (1 MHz) depending on the model, at a wide range of operation: Vcc = 3V to 6V. And an error-detecting function prevents illegal op-code and illegal addresses.

Other enhancements of the 6300 Family include upward source and object code compatibility with the HD6800 and bus compatibility with the MC6800 Family.

## All the Support You Need

Hitachi's comprehensive development support includes evaluation kits, emulators, prototyping devices, and cross-software packages running under CP/M on personal computers and under ISIS-II on Intel development systems.

The 63P01 offers piggyback flexibility, which lets you "fine tune" programming before committing to a final ROM code. All this development support is available now for you to start your design.

## Enviable Track Record

The 6301 has been in mass production for more than two years. Five million units are now the brains behind hand-held terminals, briefcase computers, printers, digital switches, phones, modems, and automotive spark control computers.

## Available in Quantity

If you need them now...in production quantities...you're in luck. The Hitachi 6300 Family offers immediate availability of the finest selection of single-chip microcomputers on the market today.

Why wait when you can have the finest 8-bit, single-chip microcomputers immediately. For complete design solutions, you can combine Hitachi's 6301 with our CMOS peripheral LSIs, CMOS ROMs, and CMOS RAMs for a total CMOS system.

So when you want deliveries, not just promises, call Hitachi. Ask your local Hitachi Representative or Distributor Sales Office about the CMOS Family of 8-bit, single-chip microcomputers.

**HD63B01**
4K Bytes of ROM, 128 Bytes of RAM
29 Parallel Input/Output Lines
Stop-Start Serial Communication Interface
16-Bit Timer
8 x 8 Multiply Instruction
Low Power Consumption Mode (60mW)
Sleep Mode (10mW), Standby Mode (10μW)
Instruction Cycle Time: 0.5μs
40-Pin Package

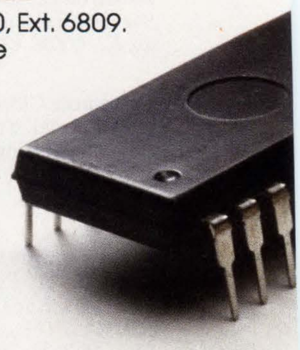
| Part No. | Architecture |
|---|---|
| HD6301, 63A01, 63B01 | Mask Programmable ROM On-Chip |
| HD6303 | External ROM |
| HD63P01 | Piggyback EPROM |

## FAST ACTION

To obtain product literature immediately,

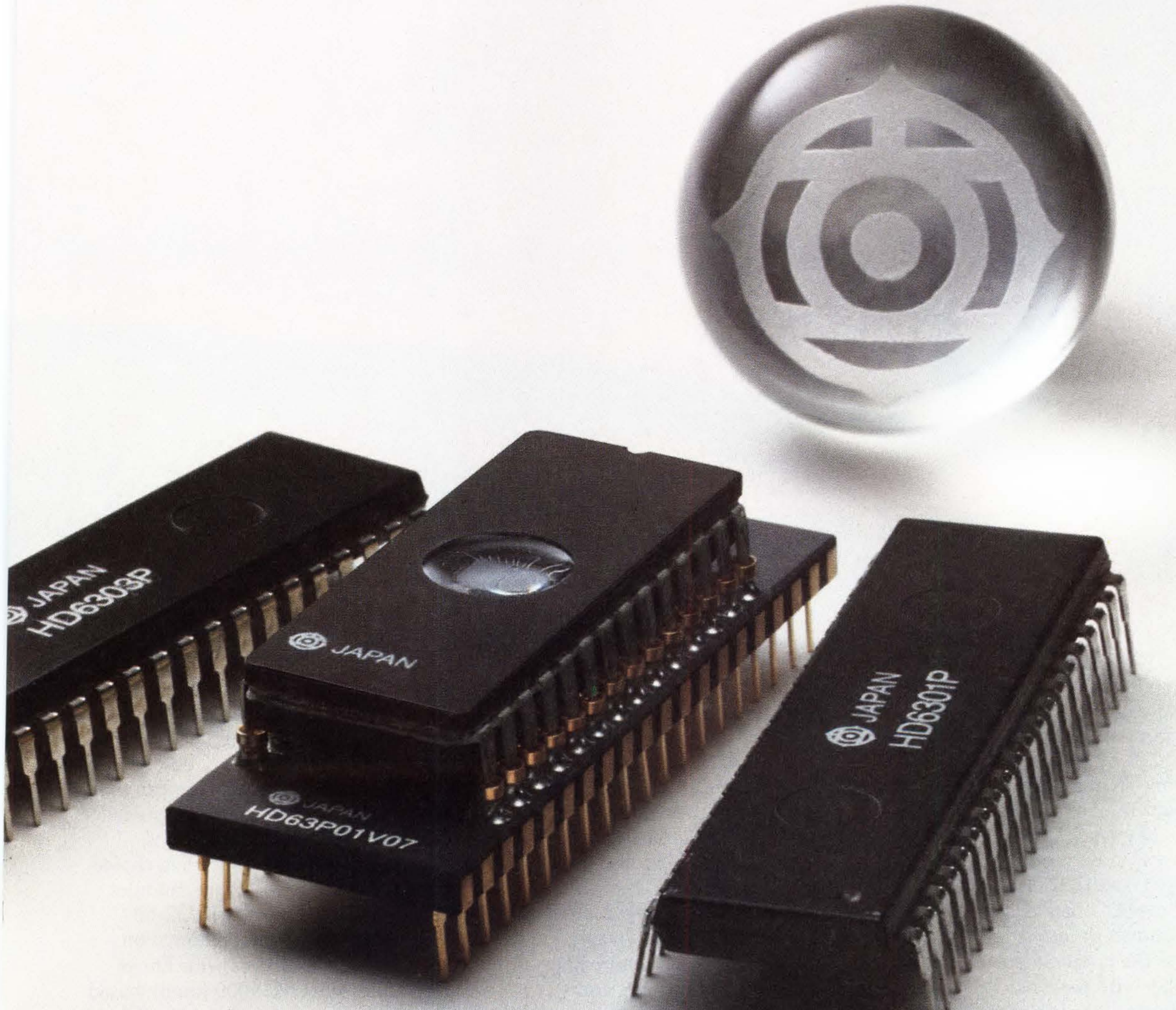
## CALL TOLL FREE

1-800-842-9000, Ext. 6809.
Ask for literature number 705.



**Hitachi America, Ltd.**
Semiconductor and IC Sales and Service Division
2210 O'Toole Avenue
San Jose, CA 95131
1-408/942-1500

# 6301 ≥ 80C51

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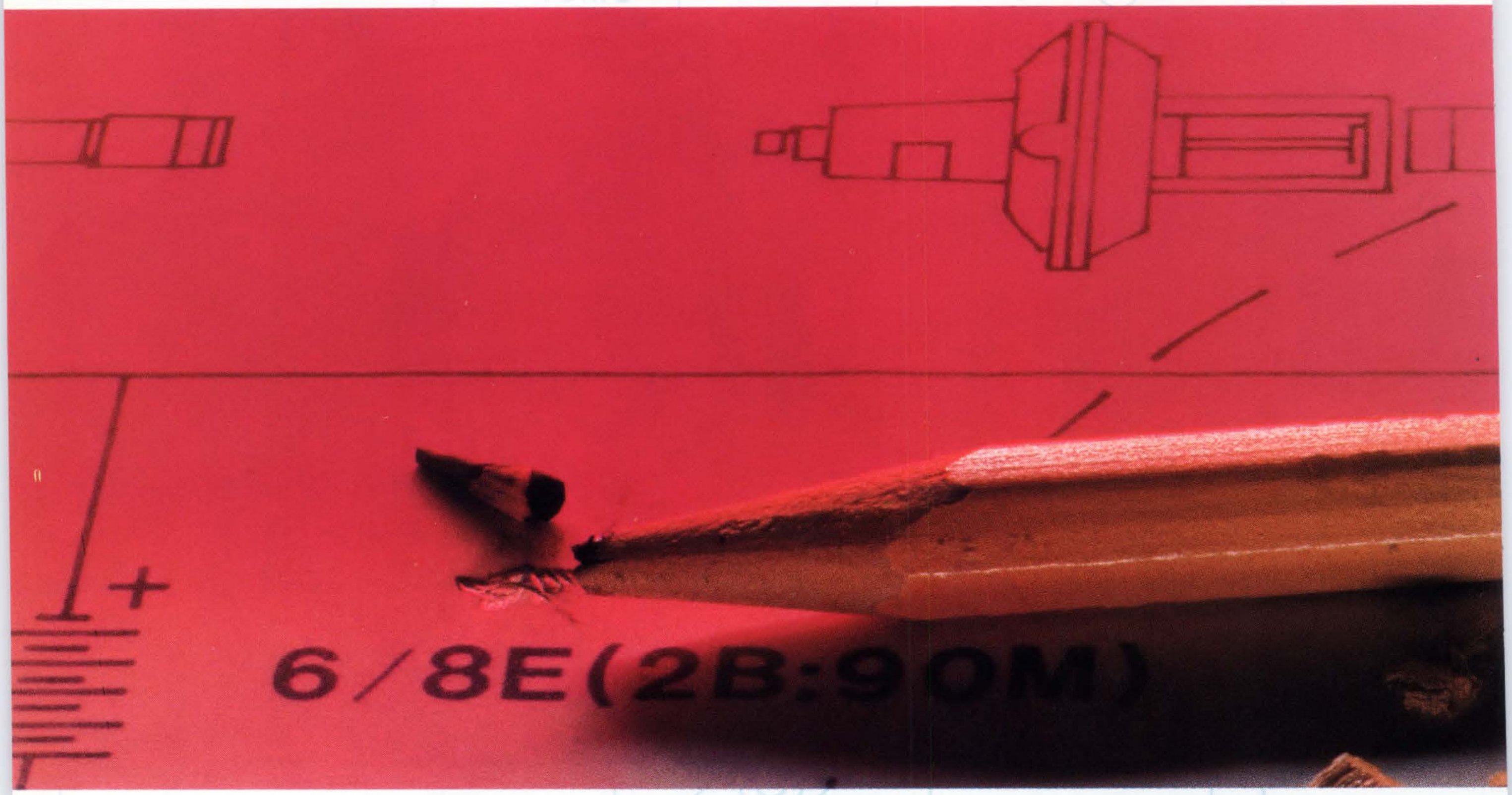
# MOTO

## Industrial automation systems are a



Designing complex industrial automation systems can drive you to great lengths in finding all the appropriate components. Call us now at 1-800-521-6274 and find out how one call to one source can help put all your semiconductor, board and box solutions within easy reach.

Whether you're working on robotics, pressure sensors, programmable controllers, computer numerical controls, data acquisition units, motor controls or industrial networks, Motorola is the broadest-line semiconductor supplier with the most advanced technologies and products for your industrial automation system needs.

**Start your design with silicon.**

Start with our complete line of 8-bit single-chip microcomputers road tested for hostile industrial environments by our long track record in automotive applications. Being bolted to the side of an automotive engine subject to heat, dirt and motion leaves no room for the weak of part.

With this history, you can match any speed or power requirement in your toughest industrial application by choosing from either our familiar HMOS or high-density HCMOS technologies. Our diverse M6800, M6804 and M6805 processor families include the MC1468705G2: the only CMOS MCU with on-board EPROM for additional user configurability.

The latest in our factory-proven line of 8-bit MCUs is the MC68HC11, which includes on-chip EEPROM. Its enhanced 6801 core provides the highest integration and fastest speeds in our entire line. And total bit manipulation gives complete control.

With bus speeds in the 2 MHz range and operating temperatures of −40 to +125° C the MC68HC11 will meet and withstand harsh factory applications.

Its powerful software control capability includes a comprehensive set of two serial ports, three timer functions, A/D conversion and parallel ports with full handshake capabilities that ease system integration.

**Integrated systems within your system.**

Many large industrial companies—with a number of plants and a variety of applications—have reduced the long term cost of support logistics and initial system development time by deciding on one standard board-level system. You can too.

Motorola's VMEsystem is designed especially for industrial applications.

It's the system designer's leading choice in providing high-performance modules and support products for 8/16/32-bit applications. For industrial automation needs, VMEsystem offers a wide line of VMEmodules from M68000 family-based processor, memory, controller and I/O channel modules to industrial I/O modules including A/D, D/A, sensing and switching.

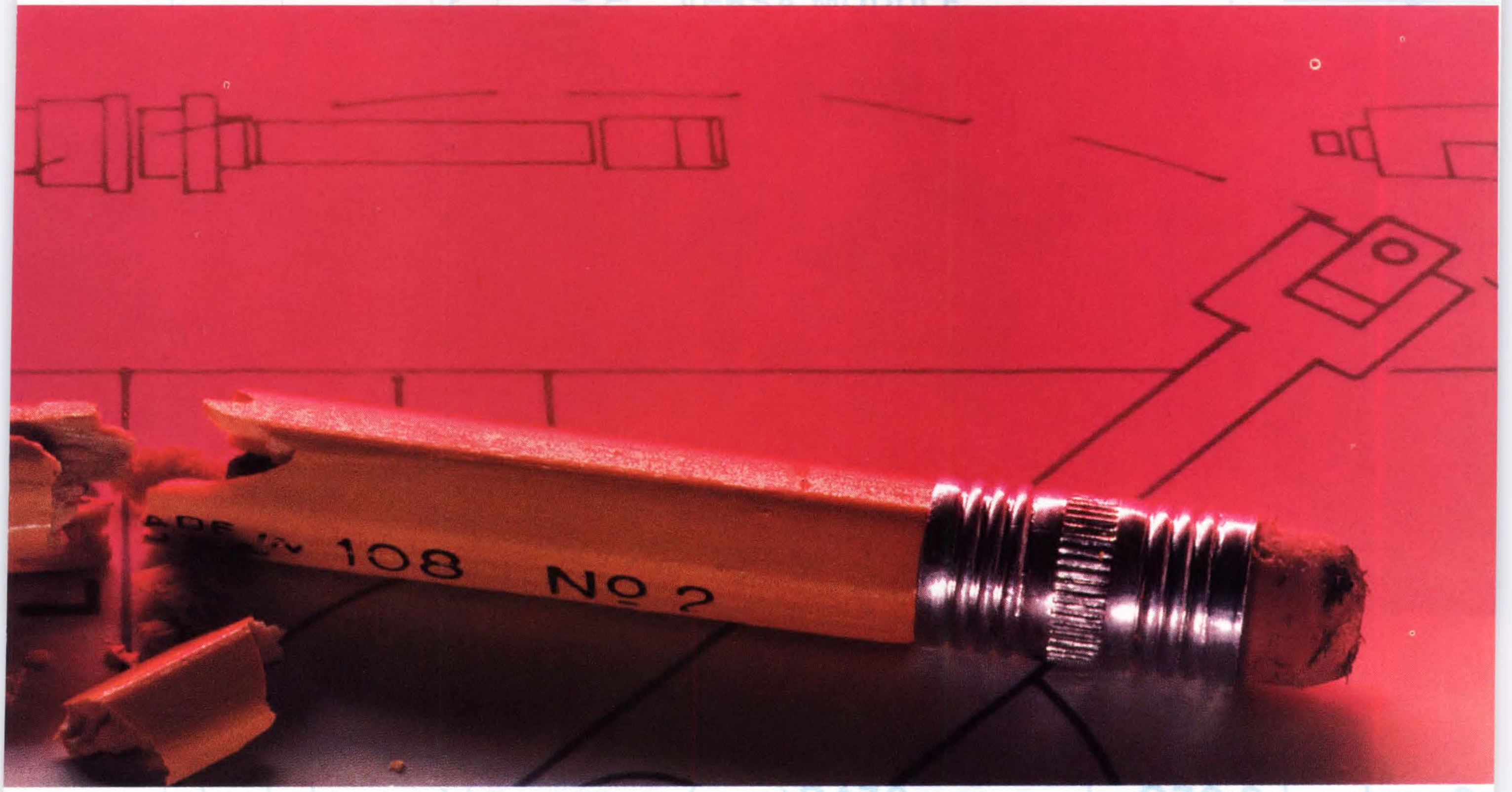
These modules can be incorporated into a VMEmodule system chassis or the VME/10 OEM microcomputer to meet a variety of demanding industrial applications and increase your flexibility.

You're not locked into product-specific manufacturing.

To better manage resources through data transfer and work station communication, the VME/10 OEM microcomputer can also be used as a data acquisition

# ROLA

## snap. Call now for design-in support.



station or a level two controller.

**Isolate power in your systems.**

To isolate power and control devices in an industrial setting, specify gallium arsenide infrared emitting diodes optically coupled to a detector/output device. Or, design your own slot configurations with our slotted optocouplers. Both provide the needed protection between power and control circuits.

When your design calls for isolating even up to 7500 volts between input and output, Motorola optoelectronic devices can meet the spec.

Surge hazards can also be controlled, by Motorola's MOSORB™ line of high-current surge protectors best suited for the precise protection of sensitive equipment even in the low voltage range.

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Our TMOS™ power MOSFET family is emerging as a design-in winner in power control, brushless DC motors and robotics due to its exceptional abilities to minimize switching losses and required heat sinking. Drive circuits become simpler. Size and weight of componentry shrinks. And your industrial automation system design becomes more energy efficient at a cost approaching that of bipolar devices.

Our SMARTpower™ power MOSFET family integrates both TMOS power and CMOS logic functions on a single chip. Our MPC100 and MPC2005 cost far less than equivalent discrete components, reduce layout space and have all the protection you need to virtually eliminate voltage faults and temperature excursions.

**Talk engineer to engineer.**

Motorola has tripled the number of application engineers it has throughout the U.S. and Canada.

Each has the expertise in emerging semiconductor technologies that can electrify your new industrial automation ideas. Call 1-800-521-6274 and discuss your applications. Any time between 9 A.M. East Coast and 5 P.M. West Coast time, weekdays. Toll free. Talk to our specialists. They'll discuss your applications and get you in touch with a field application engineer who'll in person describe in depth how Motorola products can cut your design time.

## 1-800-521-6274

Wait'll you hear what we have in store for your new design. Be it in industrial or office automation, voice/data communication, entertainment equipment or any other electronics-driven industry, we'll work with you at any level of chip, board or box integration through the industry's premier technical field organization.

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For all your semiconductor needs. Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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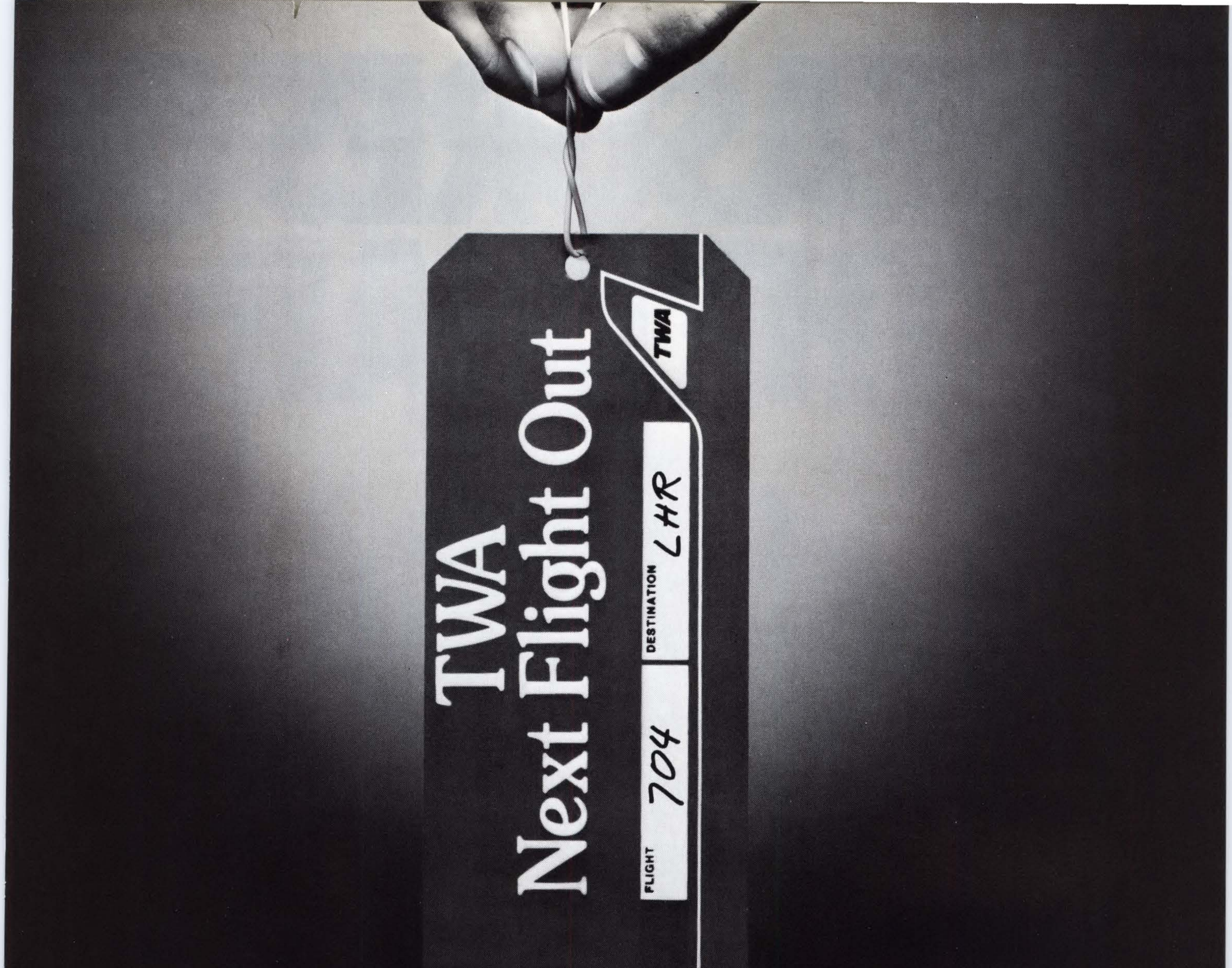


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CIRCLE 62

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# Preserve Your Time With Our Thermal Line

Your time is too important to waste. Once it's gone, it's gone. And that can be expensive. Western Graphtec helps you preserve your time and save money with its remarkable line of Mark VII high-speed, multi-channel oscillographs.

**Thermal Accuracy**

First, you save time by getting sharper, cleaner lines with our patented Mark VII Thermal Pen. Its microprocessor patented circuits sense chart speed, signal velocity, and ambient temperature, and automatically regulate the current that goes through the pen stylus. This guarantees you sharp, constant density, blot-proof, permanent presentations of charted data. No messy ink smears. No time-consuming clean-up. And no need to re-run your data. With Western Graphtec's Mark VII oscillographs you get it right the first time. And that saves you time.

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The Mark VII preserves your time in more ways than one. Its automatic Digital Annotation records the data and time for you, along with the record number and chart speed. So you never have to go back and waste time noting them yourself.

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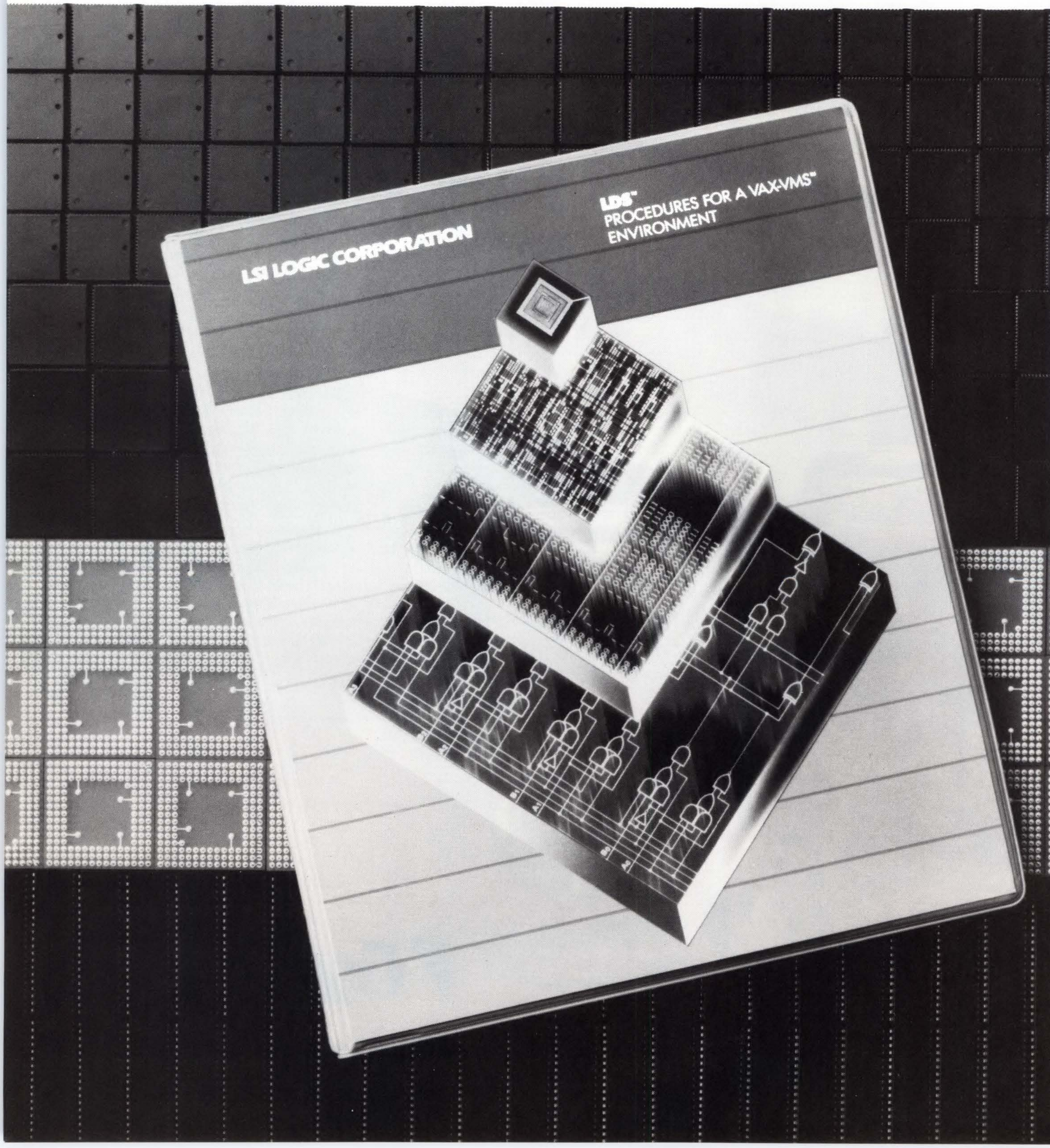
CIRCLE 64

# How to sim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LDS™
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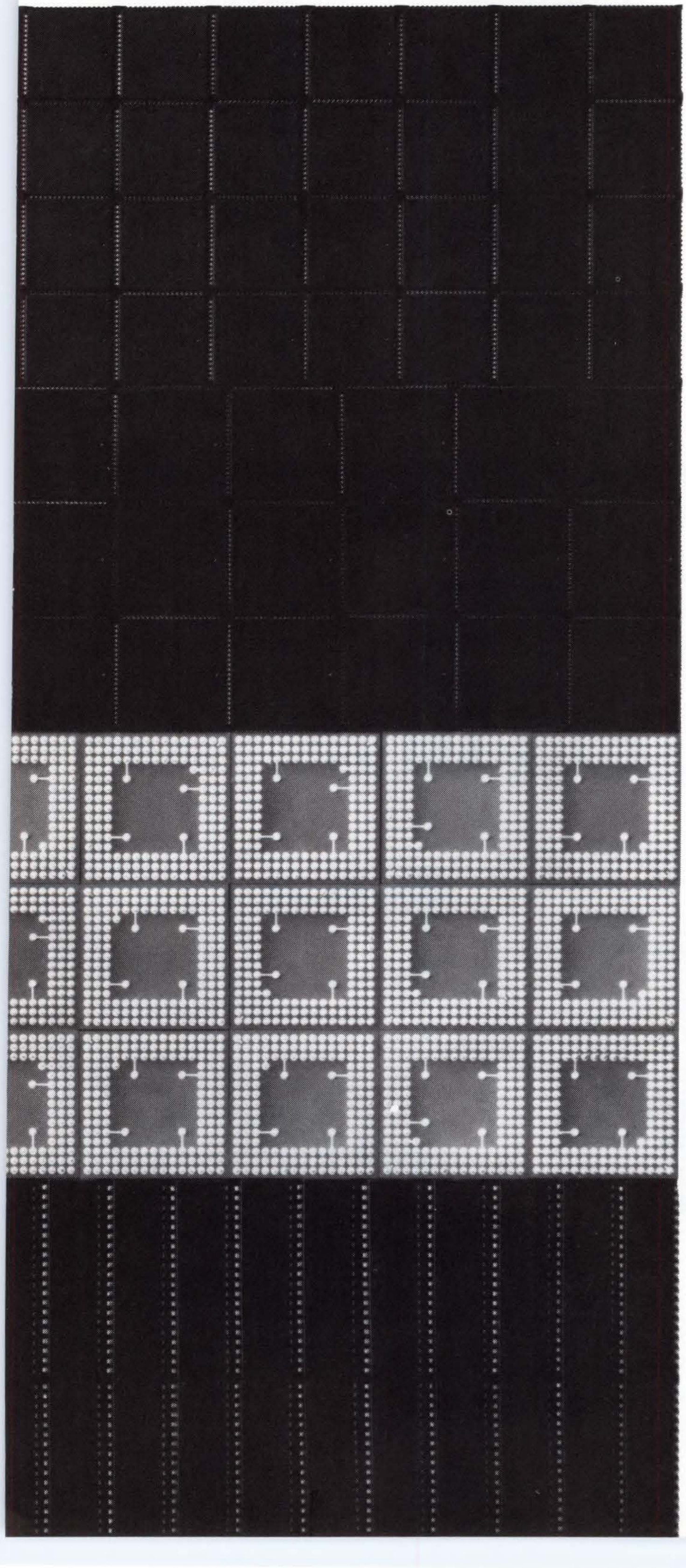
# ulate reality.



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Programs that let you describe, simulate, verify and test 2- and 3-micron HCMOS logic arrays on your VM/CMS, VAX-VMS or UNIX-based system.* So you can answer all the "what ifs" right at your desk, right away.

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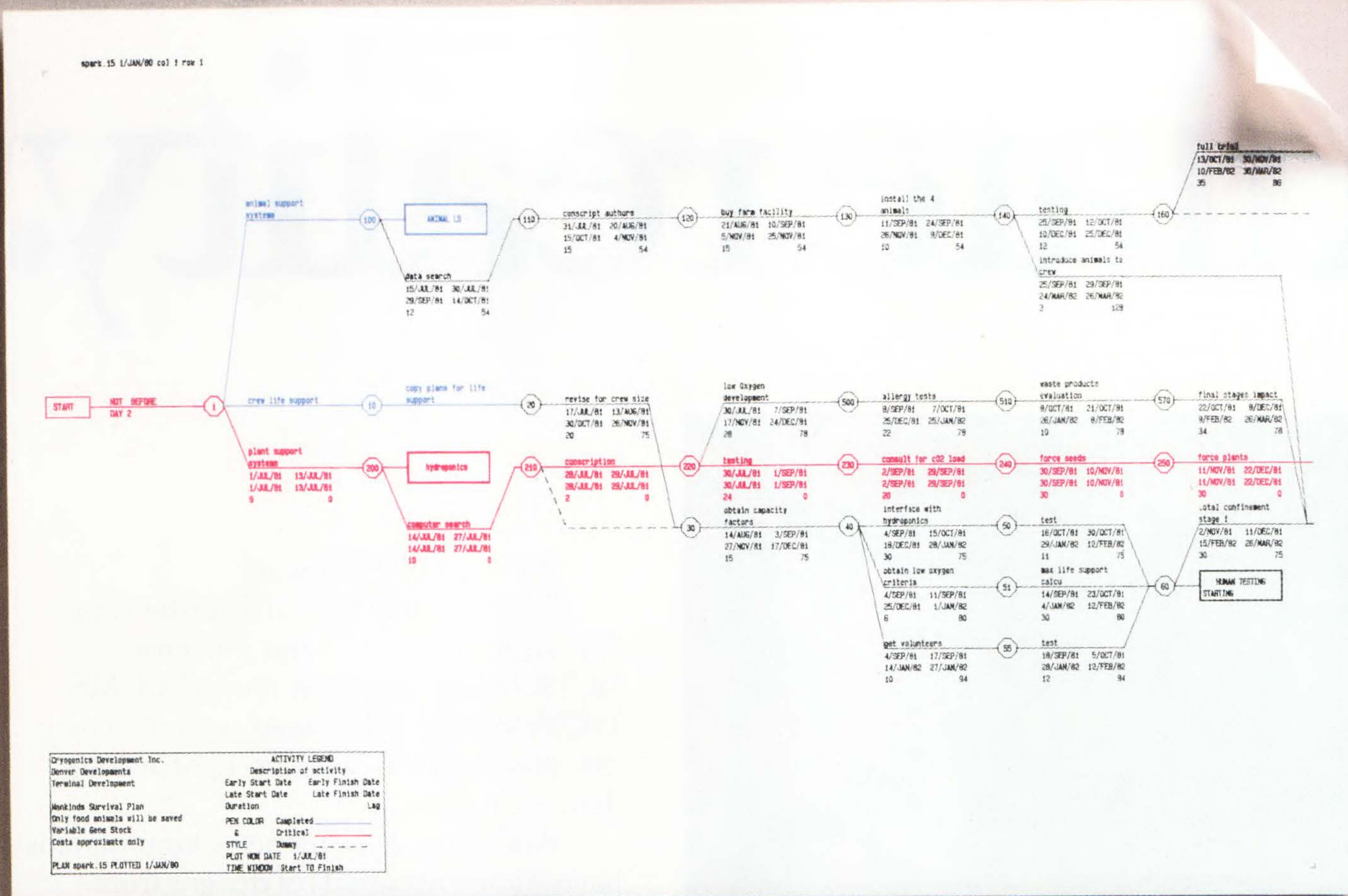
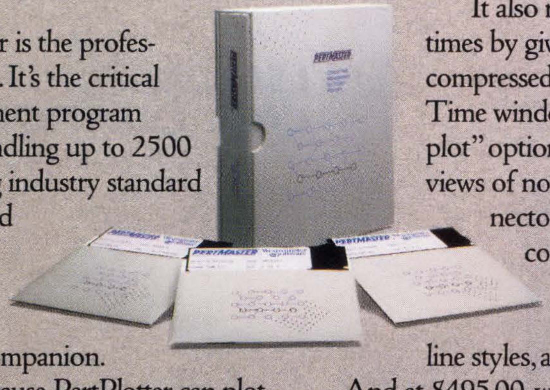
**CIRCLE 65**




# Tear along the plotted line.

And rip through deadlines in record time. With PertPlotter,™ the new network logic plotting program designed to complement Westminster's Pertmaster™ project management software.

Pertmaster is the professional's choice. It's the critical path management program capable of handling up to 2500 activities using industry standard notations. And Pertplotter is its logical extension and perfect companion.



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It also reduces plot times by giving you highly compressed logic diagrams. Time windowing. A "fast-plot" option for quick views of nodes and connectors. And full control of Title Block, activity data content, line styles, and much more.

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**PERTMASTER**™
by Westminster Software

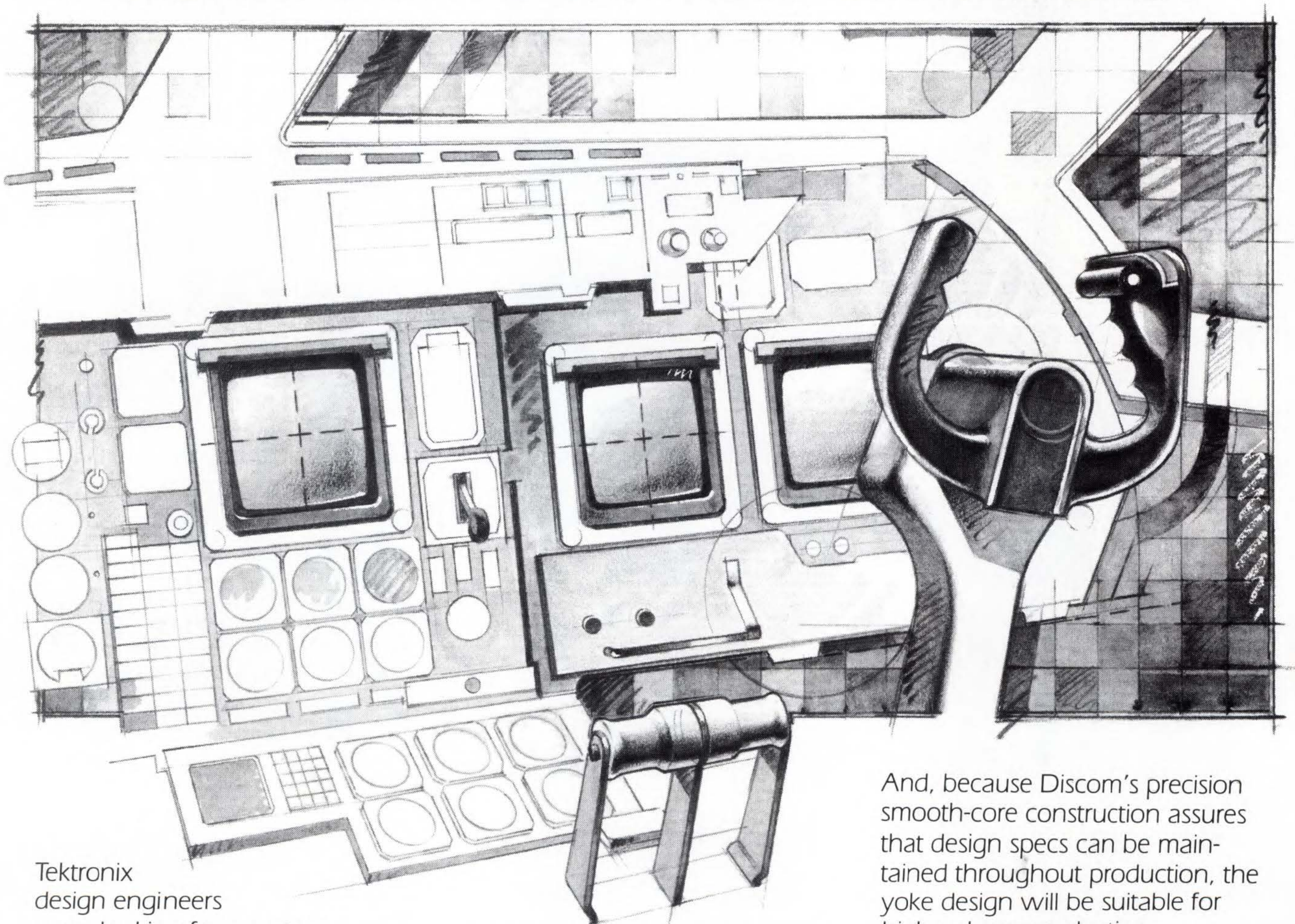
Westminster Software, Inc.
660 Hansen Way, Suite 2
Palo Alto, California 94304

**PertPlotter is compatible with the IBM™ PC graphics printer, most Epson™ and HP™ dot matrix printers and HP's 747X series pageplotters, with many more to follow. Pertmaster and PertPlotter are trademarks of Westminster Software, Inc.*

**CIRCLE 66**

THE CHALLENGE:

# Develop a self-converging color yoke capable of 0.3 mm convergence in extreme environmental conditions.



Tektronix design engineers were looking for a partner to participate in an R & D contract to develop a color CRT package for cockpit instrumentation. Convergence of better than 0.3 mm over the five- and six-inch flat screens would be difficult to achieve. And the temperature and vibration extremes of an aircraft cockpit would make it even more of a challenge.

So they turned to Discom. Tektronix knew Discom's thirteen-plus years of developing components that have continually raised the state-of-the-art in display technology would help them realize their objectives.

Discom's patented non-uniform conductor distribution process will enable Discom's engineers to develop a specially designed deflection yoke for these tough performance and environmental requirements. Then Discom's full-capability prototype lab can build prototypes for testing and evaluation.

And, because Discom's precision smooth-core construction assures that design specs can be maintained throughout production, the yoke design will be suitable for high volume production.

In avionics, as well as VDT's and large screen graphics, Discom is helping the world's largest electronics manufacturers meet their design challenges. And often saving them time and money in the process. Circle the number below on the reader response card, or call (617) 692-6000 and challenge Discom.

**Discom**

Display Components, Incorporated
334 Littleton Road
Westford, MA 01886

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CIRCLE 68

*Win Exciting Prizes!*

enter Mini-Circuits'

# Design Contest


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dual disk-drives, printer, software (word processing, spreadsheet and planner). A complete system ... **a $4,000 VALUE!***

**2-4-6 hr. VHS Videocassette Recorder**
3 speed, remote control, timer, electronic tuning ... including 6 tapes ... **a $500 VALUE!***

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*Value at time of press. All applicable taxes and duties are the sole responsibility of the winner.

F 93-A REV. ORIG.

# Design Contest

MICROWAVE JOURNAL OFFICIAL JUDGES

## It's Easy to Enter

Do you have a clever design idea or application involving IF/RF/microwave signal-processing components—mixers, power splitter/combiners, attenuators, RF transformers, directional couplers, amplifiers or RF switches? Or perhaps a versatile setup for testing them or a novel approach to enhance their performance.

If you have an original idea, enter Mini-Circuits Design Contest now. Type or legibly print your submissions. Start with a brief abstract describing the key point of your idea (cost saving, improved performance, simplified testing, etc.). List RF signal processing components used. Then proceed with the detailed explanation. Make schematics and block diagrams clear; include values of circuit components. Be sure to include performance data and curves; judges' scores will be based on content, multiplicity of products involved and thoroughness.

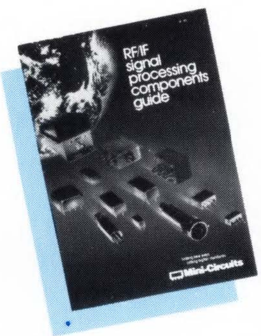
## Contest Rules

1. Submit as many entries as you wish.
2. Ideas should be original and non-proprietary.†
3. Entries will be judged by the editorial staff of Microwave Journal and their decisions will be final. The top 25 winning entries will be published in Microwave Journal.
4. All entries become the property of Mini-Circuits Laboratory and must be received by December 31, 1984.
5. Employees of Mini-Circuits Laboratory, Microwave Journal and their sales representatives, are not eligible.
6. Contest void where prohibited by law.
7. Make sure to include your business address and phone number. In addition, for non-U.S. entries, indicate AC power line voltage and frequency.
8. Send your entries to:
   Mini-Circuits' Design Contest
   P.O. Box 137
   Brooklyn, NY 11235

†Winners may be asked to sign an affidavit of eligibility & release.

## Good Luck, and Thanks.

The Mini-Circuits Design Contest, with its competitive excitement and fabulous prizes, is our way of thanking all of the designers worldwide whose staunch customer support has been responsible for our continuing growth.




### Free 64-page RF/IF Signal Processing Components Guide

For an up-to-date review of Mini-Circuits' IF/RF/Microwave product line, refer to EEM, EBG, Gold Book or Microwaves Directory. Or call/write our factory or any of our 45 worldwide sales offices for our 64-page RF Signal-Processing Components Guide.


### Free fact-filled Question/Answer Series on RF Signal-Processing Components

Since Mini-Circuits is the world's largest manufacturer of mixers and RF signal-processing components, it's natural for us to receive hundreds of questions from engineers on these products. How to test them, how to make the right selection, how to optimize a circuit design ... questions with answers not found in textbooks or reference manuals.

So we've put together a series of Q & A (question/answer) booklets on most-frequently asked questions on mixers, phase detectors and power splitter/combiners. They are loaded with application-oriented tips, ready to solve a problem you may be facing. The set is free ... just call or write us or any of our 45 worldwide sales representatives.

# EXAMPLE 1:

## Low-cost, high performance Image-Rejection Mixer.

**KEY COMPONENTS; mixers, power splitters.**

Many telecommunications systems require a mixer arrangement that delivers the desired IF and sharply rejects the other image frequency.

An effective, low-cost solution makes use of Mini-Circuits' TFM-2 mixers and it's 2-way, 0° PSC-2 and 2-way, 90° PSCQ-2-90 power splitter/combiners as shown in the diagram.

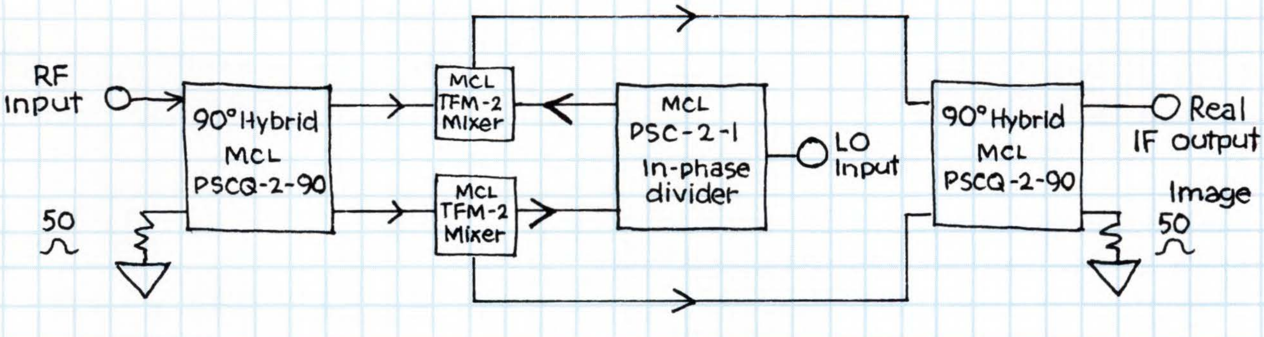
The key to an efficient image-rejection, such as shown in the block diagram, is the use of double-balanced mixers with well-matched amplitude and phase characteristics and high isolation. However, poor hybrid phase characteristics, differences in the output amplitudes of the hybrids and non-symmetrical external circuits will also reduce image-rejection performance. The effects on sideband suppression caused by unequal mixer amplitude and phase shift are shown in Tables 1 and 2.

Table 1
Amplitude Unbalance vs. A, dB

| Unbal, dB | A, dB |
|---|---|
| 0.3 | 35 |
| 0.9 | 27 |
| 1.5 | 22 |
| 2 | 13 |
| 3 | 15 |

Table 2
Phase Unbalance A, dB

| Phase Unbal, degree | A, dB |
|---|---|
| 3 | 33 |
| 9 | 22 |
| 15 | 18 |
| 20 | 15 |
| 30 | 12 |




JOSEPH CANTORE,
Engineering Dept.,
Alphaomega Corp.,
11 Madison Street
Key Biscayne, Florida 33149



F 93-C REV. ORIG.

send your entries to:

Mini-Circuits' Design Contest
P.O. Box 137,
Brooklyn, New York 11235

# EXAMPLE 2:

## Improving two-tone, third-order IM measurements.

### KEY COMPONENTS; power splitters, attenuators, amplifiers

Two-tone, third-order intermodulation (IM) expresses the degree of non-linearity of an amplifier or mixer. This parameter is generally not included on data sheets because it is dependent upon operating frequencies, terminating impedance and input levels; it must be measured under specific design performance conditions.

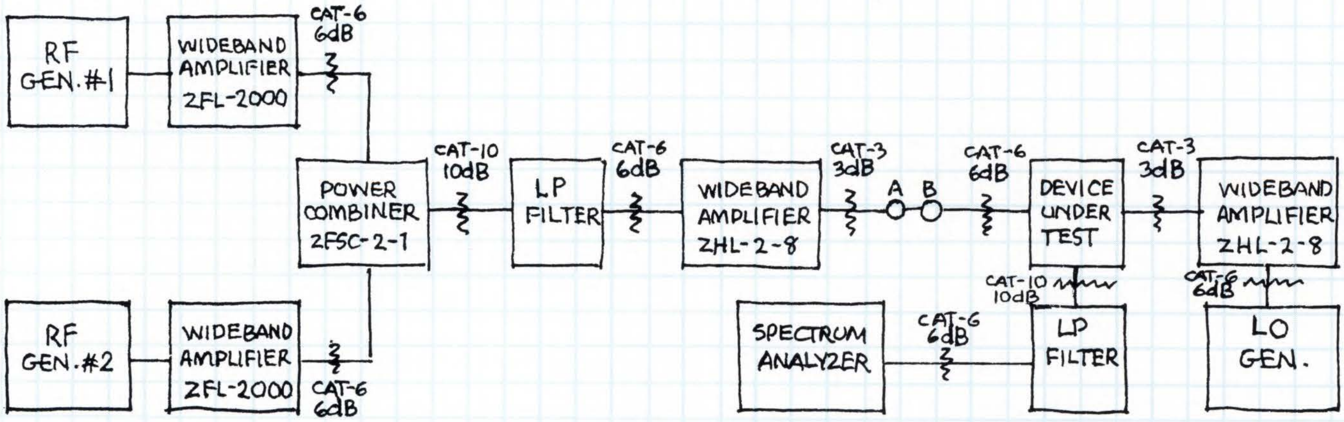
Two common errors in these measurements are (1) failure to provide adequate isolation between input signal generators and proper impedance matching and (2) insufficient filtering of the two input test signals.

A proper test setup for measuring two-tone, third order IM distortion is shown. Note the use of two amplifiers and 6dB pads for input generator isolation and proper 50 ohm matching. A practice of simply using a Tee-connector between generators developes mismatches, producing undesired harmonics which dramatically affect accuracy.

Two-tone, third-order IM distortion is only meaningful when the input levels to the device-under-test are defined.

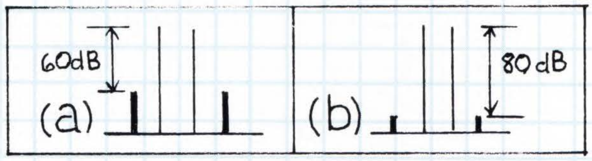
Examine the spectrum analyzer display for a ZAY-1 double-balanced mixer. Notice the significant difference in two-tone, third-order component with an input level of −10dBm for each tone (b) compared with 0 dBm input level for each tone (a).

Also, the amount of two-tone, third-order must be specified relative to either the RF input or desired IF output; the desired IF output is more meaningful.




GENERAL NOTES

1) All Mini-Circuits products have model numbers shown.
2) 0dBm input, A-B connected as shown
   −10dBm input, insert CAT-10, 10dB between A-B




0dBm input power — −10dBm input power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# NEWS FLASH



## Price breakthrough — switching power supplies

In the fiercely competitive switching power supply market, many companies have trouble meeting prevailing cost per watt pricing levels. Not so at POWER GENERAL, a Canton, MA. power systems manufacturer.

Quantity prices for a quad output, 100 watt, switching power supply, for example, have been cut to *less than 50¢/watt.* A wide variety of popular switching supplies, including 40, 50, and 70 watt, triple and quad output supplies, have been given similar price cuts.

This significant price reduction has been accomplished through new cost-effective designs and increased manufacturing efficiencies at no sacrifice in product quality, reliability or performance. All new open frame switching power supplies are designed to meet the most stringent international safety standards.

for more information circle 69

## Industry standard DC-DC converters offered

A full line of industry standard, 1 to 50 watt DC-DC converters is being offered by POWER GENERAL. These popular converter types are form-fit and functionally compatible with similar products available from manufacturers such as Power Products, Stevens Arnold, Datel, Reliability and Semiconductor Circuits.

Features such as wide input voltage ranges, remote on/off control, low output noise, electrostatic shielding, low profile cases, and input PI filters are offered. In some cases, the POWER GENERAL units will actually offer the user improved performance and availability at competitive prices.

for more information circle 70

## New AC-DC modules replace encapsulated versions

A new series of linear AC/DC modules features a unique, mechanical design. Offered by POWER GENERAL, a leading U.S. manufacturer of power conversion products, the 140/240 series convection cooled, metal cased supplies have an MTBF of 120,000 hours. These units are plug-in compatible with industry standard models available from Semiconductor Circuits, Power Products, Acopian and Datel.

Units are available with single outputs of 5, 12, 15 or 24 VDC and dual outputs of ±12 or ±15 VDC. All models are available for either P.C. board or chassis mount and are capable of series or parallel operation. The use of toroidal power transformers reduces radiated magnetic fields to a minimum. The 140/240 series is plug-in compatible with competing encapsulted units.

for more information circle 71

## Free handbooks offered on DC-DC's & SWITCHERS

Available free upon request, these new product handbooks include comprehensive data on Power General's full line of switching power supplies and DC-DC converters, including over 75 new products.

Power supply characteristics are presented in quick selection tables followed by complete engineering data on all models. Also included in each handbook is a glossary of terminology and tutorial information on DC-DC converters or switching power supply operation.

for more information circle 72

# Coming December 27... Our Designer's Reference Special Issue... The industry's only complete reference guide

*IN ADDITION, REPORTS COVERING:*

- CAE Software
- Data Communications

*NEXT IN OUR PERSONAL COMPUTER SERIES:*

## Personal Computer Report Card: A Reader Survey (Part 2)

# World-Class Components Update:

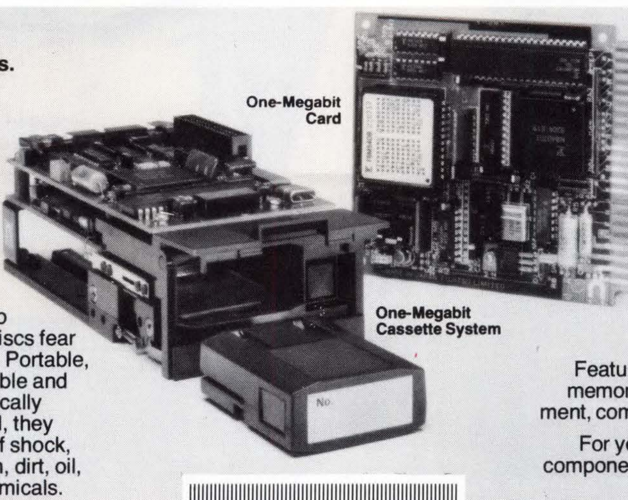
# CUSTOM BUBBLE MEMORIES

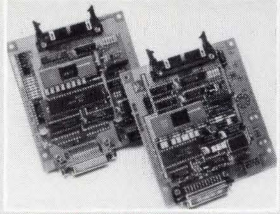
**Never has so much memory offered so many advantages in so many ways.**

Fujitsu's custom bubble memories offer maintenance-free operation, card expandability to 4 megabits, access time 4 times faster than competitive bubbles and 10 times faster than floppy discs, ambient temperatures from 0°C to +50°C (case temperatures from 0°C to +70°C) and a non-volatile memory that generates *without a seed bubble.*

What's more, tough Fujitsu cassettes go where discs fear to tread. Portable, detachable and magnetically shielded, they shrug off shock, vibration, dirt, oil, and chemicals.

And now, the new adapters shown in the inset interface the 1-megabit cassette and the 4-megabit card to both RS232C and GPIB (IEEE 488).



*Adapter FBM-A003 (left) interfaces with GPIB; Adapter FBM-A002 with RS232C.*

Also you can now order a 1-megabit, single power source (+5v) cassette system. This new unit has a built-in power-fail signal, which prevents loss of data in the memory. Its internal circuitry also provides for +12v and −12v power sources.

Finally, you can order a new 4″ x 4″ 1-megabit bubble memory card and card *kit.* The assembled card plugs into a standard card-edge connector.

Features like these make Fujitsu custom bubble memories ideal for test and measurement equipment, communication systems and data processing.

For years, Fujitsu has produced state-of-the-art components at competitive prices—components of uncompromised quality and reliability.

*For the best components at the best prices, choose Fujitsu.*

**FUJITSU**

CIRCLE 74

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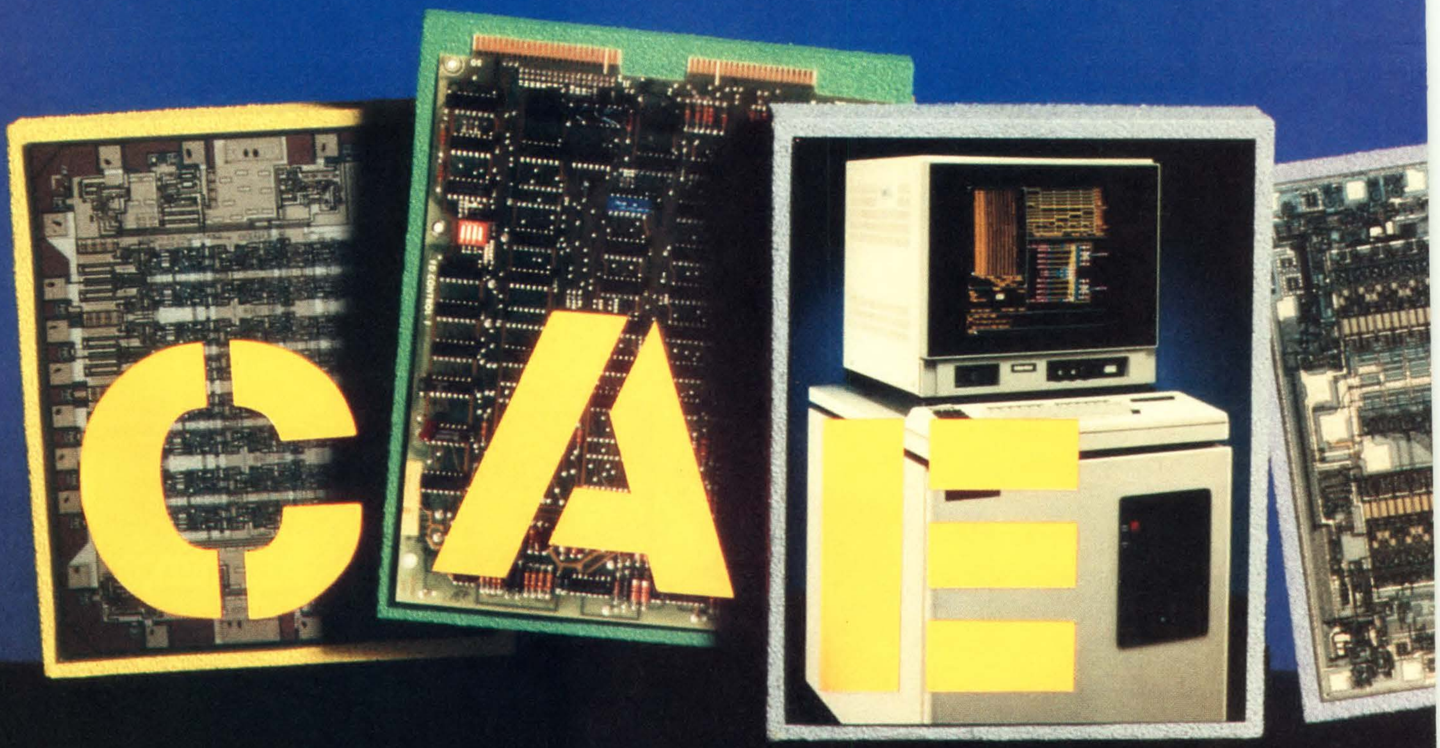
# COMPUTER-AIDED ENGINEERING

**In Greek mythology, Athena, the goddess of wisdom, leaped fully formed from Zeus's head without putting him through the pangs of childbirth. Something of his sense of triumph must buoy the system engineer seated at one of today's more advanced CAE workstations. He or she can express ideas for a chip in the sketchiest of block diagrams or even as mathematical outlines, and from them the machine will generate a complete design on a tape ready to be sent to a silicon foundry.**

**Today's CAE software is making its biggest strides in the area of simulation — the ability to model circuits accurately enough for their functions to be thoroughly tested and verified before they are cast in silicon or laid out on a printed circuit board. But in order to finish this long and complex task, some degree of accuracy always has to be traded off against speed. How the different software packages make such trade-offs is the main subject of the first part of the following Technology Report on CAE software.**

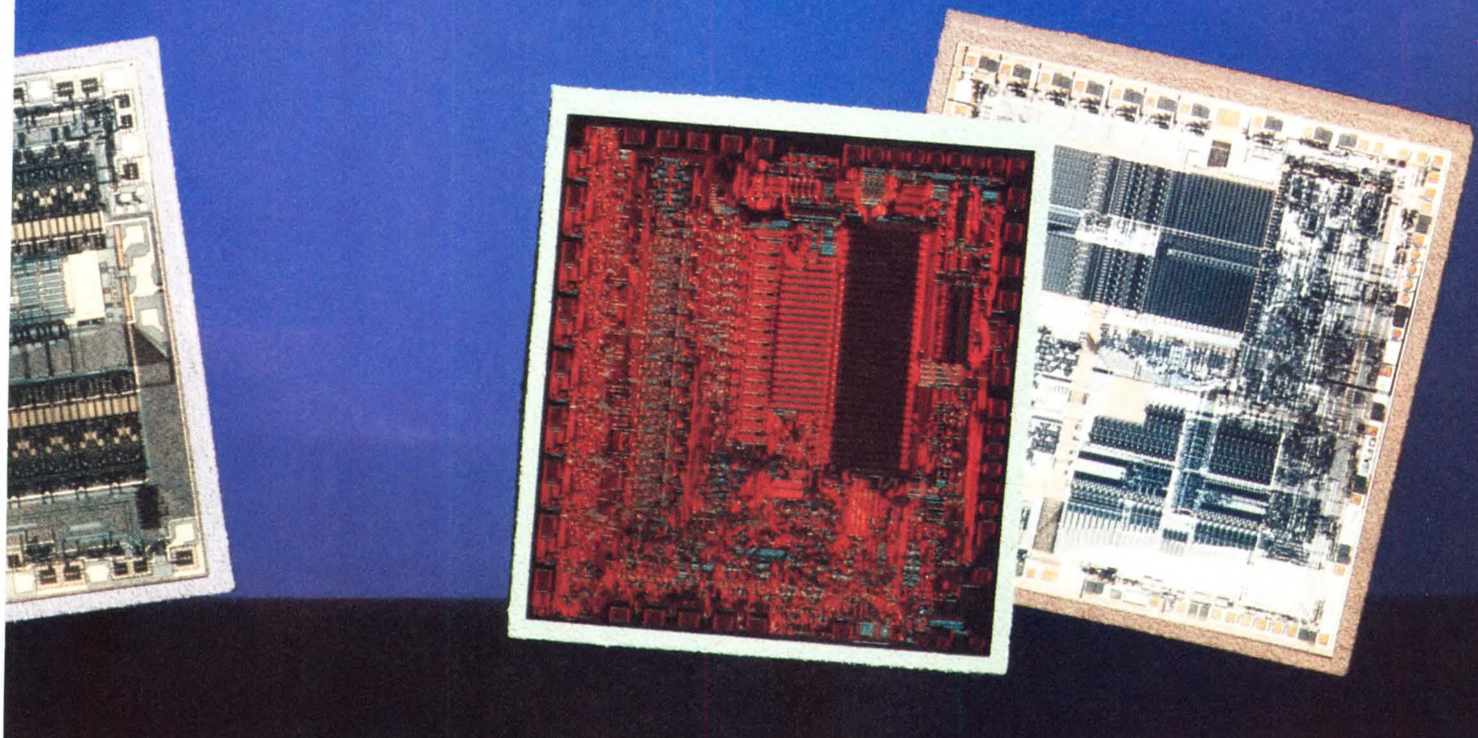
**The second and last part of the report will appear in the Dec. 13 issue and will cover the physical realization**



of application-specific ICs, including placement, routing, and design verification. Also discussed will be database systems, logic description standards, and the outlook for personal computers as hosts for CAE software.

Another major trend is toward integrating the various programs that design everything from application-specific chips down to the ultimate pc board layout. One of the design entries that follows describes a workstation for chip design and layout that links to another that develops pc boards. The board specifics are included in the simulation process. A second article homes in on the integration of a silicon compiler into a workstation capable of designing, simulating, and verifying VLSI chips.

Best of all, the languages in which engineers must talk about circuit design are becoming more appropriate to the task, as two further articles demonstrate. In one, a Lisp-like language is shown translating the functional specification for a circuit directly into hardware. Its user needs no familiarity with standard logic devices to develop a design. In the other, the described language encourages designers to incorporate into their circuits testability features that are comprehensible and helpful to the test engineer.



TECHNOLOGY REPORT

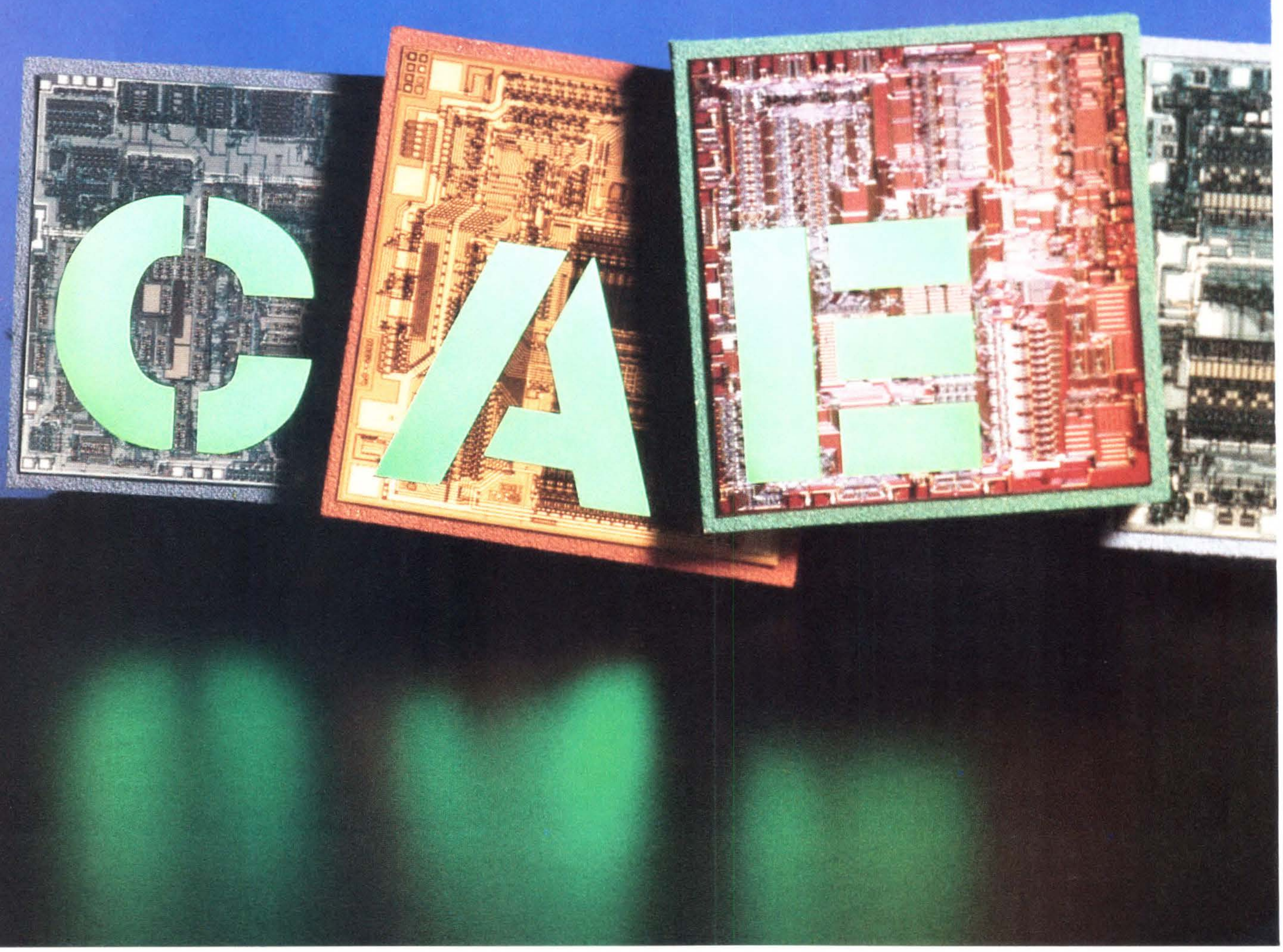
# Advances in software let system engineers take charge of IC design

This first of two Technology Reports surveying the field of integrated CAE software deals with electrical design — from capturing the circuit through simulating it. The second part, which will appear in the Dec. 13 issue, will cover the physical realization of application-specific including placement and design verification.

Over the past decade, the phrase "electronics industry" has come to be almost synonymous with digital signal processing and microcomputer-based automation. The typical digital circuit board carries a CPU plus RAM, ROM, and communications chips — all held together by glue logic. The last is usually implemented with standard TTL packages, often containing just a few logic gates.

There is a better way: the application-specific IC. And the forces of competition are making it even more attractive. Such devices can replace an entire circuit board with a single chip. The approach is already very popular for gate arrays, but software tools are advancing to the point that integrated circuits composed

Max Schindler



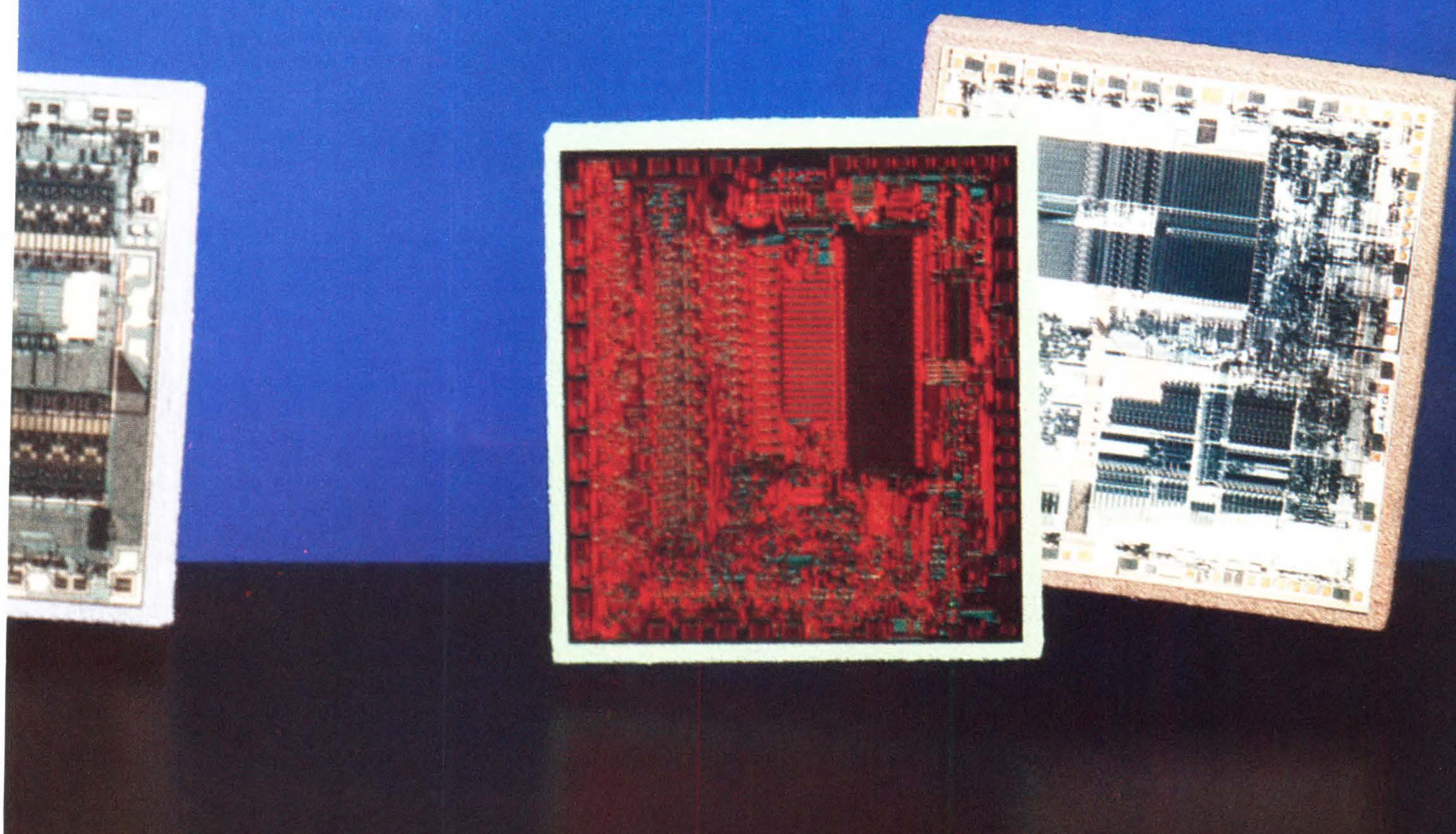
of standard cells — and even fully custom ICs — are becoming practical.

To bring about the application-specific IC revolution, manufacturers of CAE software and turnkey systems are attempting to convert an estimated 350,000 digital system designers into IC designers. At present, the second group is a rather exclusive club, with only a few thousand members. The tools needed to accomplish the transformation range from routines that handle automatic routing and placement (greatly simplifying designing gate arrays and standard cells) to silicon compilers (which convert a functional specification into a chip). Better data bases, testability analyzers, and design verification packages also improve the chances that a design will work on the first try.

None of these, though, compare in importance with digital and analog simulators. Indeed, every design relies on their accuracy. But accurate modeling consumes a great deal of CPU time; thus every CAE system must strike a balance between speed and accuracy.

Good software tools cut the cost of designing application-specific ICs to the point that the chips start to save money over TTL boards in quantities as low as a few thousand or even several hundred. The switch to ICs yields another bonus — radically reduced power consumption and faster execution. What's more, if CMOS is employed, a small unregulated power supply can often replace a large one, regulated to ±0.25 V.

Unlike the professional circuit designer, who knows how to apply and



link a broad spectrum of software tools to create logic and lay out chips, the system engineer turned IC designer requires an integrated tool set that produces correct results without the need for guesswork and for cumbersome file conversions.

Getting all the tools to accept a common data format is essential if the trend toward integrated CAE is to prevail. The efforts to create an Electronic Design Interchange Format (EDIF) could go a long way toward simplifying this chore. Nevertheless, to be truly integrated, tools must also conform to a consistent design philosophy. That characteristic is hard for the user to verify, even with a trial run.

Fortunately, the very essence of CAE integration is fairly easy to assess. Circuit design breaks down into two major phases, logic design and layout. Thus the user must simply make sure that the two are intimately connected (see "A Quick Pass through Integrated CAE," opposite). All too often, what passes for integration consists merely of a routine for translating between the logic and the layout data bases.

### Start at the beginning

The various approaches to integrated CAE can be most readily grasped by stepping through the process, beginning with logic definition and proceeding to chip production. Producing application-specific devices can start at a number of levels, ranging from capturing designs for

## A quick pass through integrated CAE

To appreciate the relationships among CAE tools that design application-specific ICs, system designers need a basic understanding of the design process. Usually a new system must be defined first at its functional level, either graphically or with a hardware description language (Fig. A). In a top-down approach, successive hierarchical decomposition into ever smaller modules follows, down to a level where components are accessible (Fig. B). At level 1 the CPU and RAM can be implemented by standard chips; at level 2, either a separate chip or a standard cell can be used for the a-d converter; finally, at level 3, the adder and latch are at hand as standard cells, but $G_1$ is represented at the gate level, and $X_3$ at the transistor level.

Because two of the "leaf" components (those that are not decomposed further) must be created from scratch, the designer switches to a bottom-up approach and lays out these functions by schematic capture. To create models for simulation at, say, the monitor level, the CAE system's analog simulator may be invoked for the selector, because this component is time-critical. The rather simple gate-level component can be modeled with standard delays, supplied by the CAE system's technology file.

If the simulator handles mixed logic representation, the whole monitor module can now be checked for proper functioning of its logic. If the simulator requires uniform (usually switch-level) representation, a tool that "flattens" the design must first be invoked. It converts functional descriptions (the a-d converter), gate-level descriptions (here, $G_1$) and cell-level descriptions (the adder and latch) into a uniform format, usually a net list plus logic and timing information.

Before committing the whole monitor subsystem to silicon, the complete control system should be simulated. If the CPU is a simple 4-bit controller chip, the CAE system's logic simulator should have no trouble handling its functional description—provided it is a mixed-mode simulator.

Before going on to generate a chip layout, system designers should plan to verify the timing of the whole system and analyze it for testability. In CAE systems, logic simulation is usually performed at the gate or the switch level (equivalent to a simplified transistor level), without considering timing. Only after the schematic is logically correct need timing verification be performed.

Because standard cells tend to consume less silicon than gate arrays, they work faster. In the example, one monitor is needed for every channel. Because silicon consumption determines how many channels can be handled by a single chip, a standard-cell design proves the best choice.

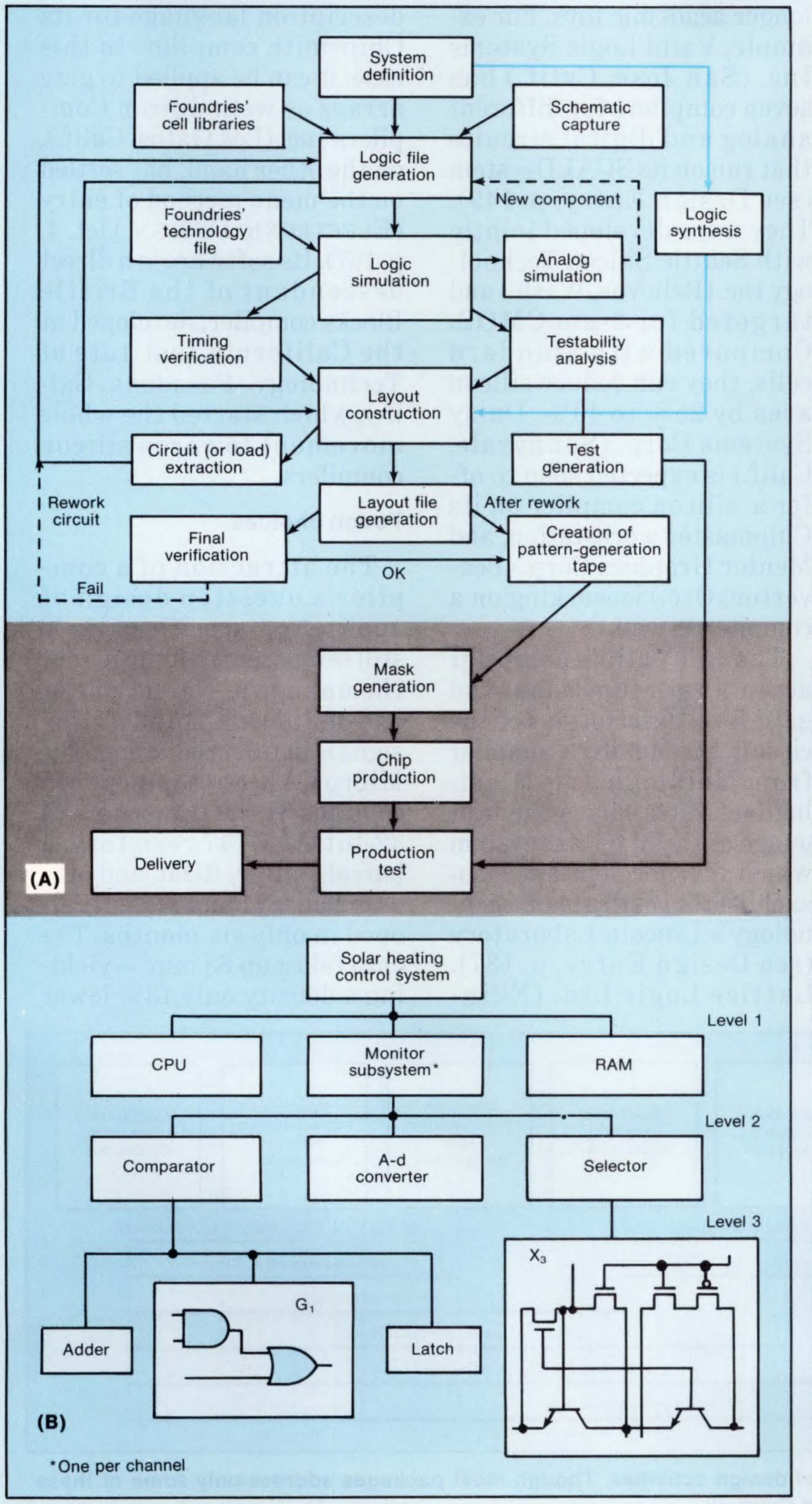
Although CAE systems differ widely in the way a logic circuit is converted to a physical layout, all need accurate models to avoid redesign. Most CAE systems extract timing information from the final physical layout, based on line length and capacitive loading. Some even reconstruct the whole circuit from the geometric mask information—a process usually called circuit extraction—and compare it with the circuit defined by the design data base.

If the design passes this last hurdle, a pattern-generation tape must be produced in one of several standard formats. All describe geometric shapes and can readily be translated from one into another.

Silicon compilation, which is now being added to some CAE systems, bypasses all steps between system definition and tape generation. As a result, silicon compilers may eventually become the main technique for designing application-specific chips.

While compiled chips may waste silicon, this may not matter if they can save a great deal of development time. However, silicon compilers have mostly been optimized for fairly standard circuits, whereas the prime purpose of application-specific designs is the replacement of nonstandard glue logic. On the other hand, random logic often adapts general-purpose microcomputers to specific applications, and a compiled processor could do away with the glue altogether.

new logic, to working with libraries of existing off-the-shelf chips and standard cells, to converting a board full of TTL packages into a single chip (Fig. 1).




In the first case, the user starts with what boils down to little more than an automated drafting system. Predefined geometric shapes (usually gates) are put on the screen and linked. The CAE system generates a data base, in the form of a net list that defines which pins are connected, and also stores the position of the circuit elements on the screen.

The second case closely resembles the first, except that here the user can pull predefined components from a library. For those employing pc boards, the components are separate packages; for designers of application-specific ICs, standard cells take the packages' place. A good example is the library of over 200 standard 3-$\mu$m CMOS cells from Texas Instruments Inc. (Dallas). It contains RAM, ALUs, decoders, adders, and analog cells like op amps.

### Just press the button

In the third case, the user starts with an existing board-level system. Because it is thoroughly defined, the ultimate CAE package would be one that converts the board to a chip at the push of one function key. Indeed, if the board has been designed on a CAE system equipped with a silicon compiler, that scenario would no longer be far-fetched.

A silicon compiler can be

visualized as consisting of a front end that handles logic synthesis and a back end that serves as a silicon assembler. Logic synthesis unites a host of tools that some would consider silicon compilers; others want to restrict that term to so-called ideal compilers, which perform the entire compilation process—from design capture through mask creation.

**Farewell, ivory towers**

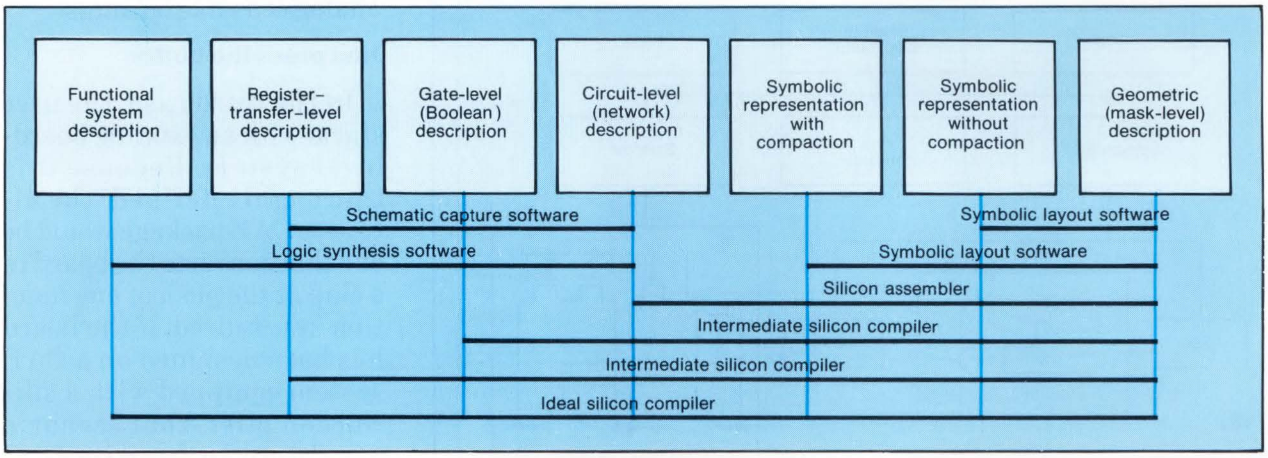
Some of the disagreement stems from the distinction between functional (behavioral) and structural (schematic) representations (Fig 2). The former describe what a system or subsystem does—usually in the form of a functional description language. The latter delineate implementations, either in schematic form or with hardware description languages. An ideal compiler transforms a functional description into a layout, but such descriptions are not widely used by system designers at this time.

Although they are still novelties, silicon compilers are no longer academic toys. For example, Valid Logic Systems Inc. (San Jose, Calif.) has seven compilers for different analog and digital circuits that run on its SCALDsystem (see Design Entry, p. 149). They were developed jointly with Seattle Silicon Technology Inc. (Bellevue, Wash.) and targeted for 3-$\mu$m CMOS. Compared with standard cells, they can reduce silicon area by 25% to 40%. Daisy Systems Corp. (Sunnyvale, Calif.) is expected soon to offer a silicon compiler on its Chipmaster workstation, and Mentor Graphics Corp. (Beaverton, Ore.) is working on a compiler as well.

Though Valid's compiler accepts both functional and gate-level descriptions of the circuit, the MetaSyn compiler from Metalogic Inc. (Cambridge, Mass.) uses the language of the MacPitts system which was developed at Massachusetts Institute of Technology's Lincoln Laboratory (see Design Entry, p. 187). Lattice Logic Ltd. (Edinburgh, Scotland) also favors a description language for its Chipsmith compiler. In this case, it can be applied to gate arrays as well. Silicon Compilers Inc. (Los Gatos, Calif.), on the other hand, has settled on the menu method of entry (ELECTRONIC DESIGN, Oct. 4, p. 167). Its software is a direct descendant of the Bristle Blocks compiler, developed at the California Institute of Technology (Pasadena, Calif.), which started the whole movement towards silicon compilers.

**Tough choices**

The attraction of a compiler's one-step design of application-specific chips is still tempered with the fear of the unknown. Nevertheless, one of Silicon Compilers' designs is in full production. The MicroVAX data-path chip contains 37,000 transistors (a 32-bit ALU, 47 resistors, a barrel shifter, ROM, and other circuitry) and was developed in only six months. The chip takes up 63 mm$^2$—yielding a density only 13% lower




**1. CAE software covers a wide range of design activities. Though most packages address only some of these tasks, an ideal silicon compiler tackles them all.**

than that of Intel's 80286. Digital Equipment Corp. (Maynard, Mass.) is now pursuing silicon compilation with an in-house effort, as are several other companies including Intel, Hewlett-Packard and Fairchild.

A silicon compiler fulfills the American ideal of a vertically integrated tool that shepherds a design from concept to chip. But the compiler's front end—which synthesizes the logic—may be better served by other design methods. For example, Japanese companies were quick to automate the time-consuming and error-prone layout effort. Nippon Telegraph and Telephone Corp. (Atsugi, Japan), for example, slashed the time usually associated with this task from 70 to 0.3 man-months. Typically 50 man-months are still required for circuit design. Through logic synthesis, this effort is expected to dwindle dramatically—to as little as 2 man-months. The functional design of the system has already been reduced from 40 to 10 man-months with the help of a simulator that accepts functional-level inputs.

One key factor in NTT's logic synthesis is circuit optimization, which eliminates single-input gates (except for inverters), redundant pass switches (by ORing equivalent signals), and redundant expressions created by previous synthesis steps. A technology conversion program, finally, optimizes the logic for the targeted approach—including TTL, ECL, and CMOS.

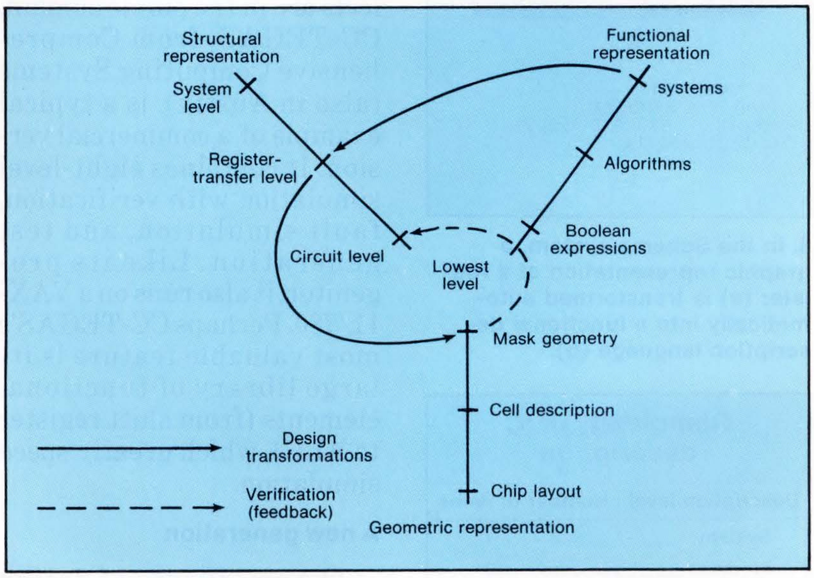
Hitachi Ltd. (Kokubunji, Japan), in contrast, takes technology limitations into account much earlier—at the register-transfer level. Signal polarity is already accounted for when a module is designed, thus producing more compact ICs. The experimental design software, from Fujitsu Ltd. (Kawasaki, Japan), even contains an expert system (currently with about 200 rules) to translate function diagrams into logic.

### Reaching out

The long-standing dispute between graphic and textual circuit description may have found a solution. At AT&T Bell Laboratories (Murray Hill, N.J.), the Schema design capture system prompts the user with a menu and then puts the selected primitive, say, a 4-bit register, on the screen (Fig. 3). The system then automatically translates the module into a hardware description language in FPDL (functional primitive-description language). This quality of representation permits both graphical connection of elements and symbolic manipulation.

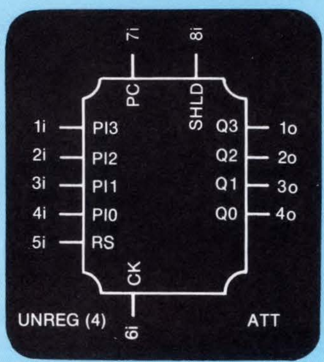
For example, the FPDL definitions could serve as input to another Bell development, the procedural layout generator. Standing about halfway between a silicon compiler and an assembler, this software package's CPU generator was employed in building the Plex microcomputer. Other generators can be specialized for UARTs, barrel shifters, or even memory. Silicon Design Laboratories (Basking Ridge, N.J.) is working on a commercial version of a similar tool set.

The layout generators are conceptually similar to Silicon Compilers' parameter-




**2. An IC can be represented in three ways. Functionally described systems could be transformed into a register-level network by one program and into mask geometry by another. A verification program can transform the latter back into circuit-level net lists, furnishing a feedback path.**

ized-cell compilers, although the latter appear capable of yielding more efficient layouts. One step closer to standard cells are the parameterized cells from VLSI Technology Inc. (Santa Clara, Calif.). A counter cell, for example, can be instantiated for any number of bits. Conceptually the two differ substantially, however. VTI's solution is generalized from standard cells, while Silicon Compilers' represents specialized silicon compilers.




(a)

```
CKTNAME:  ATT;
TYPE:     UNREG(4);
INPUTS:   CK, RS, PI [3:0], SHLD, PC
OUTPUTS:  Q [3:0]
```

(b)

**3. In the Schema system, a graphic representation of a register (a) is transformed automatically into a functional description language (b).**

**Complexity of IC description**

| Description level | Number of items |
|---|---|
| System | 1 |
| Modules | 10 |
| Cells | 1000 |
| Gates | 10,000 |
| Transistors | 30,000 |
| Geometries | 500,000 |

Whether a silicon compiler, conventional design, or anything in between is used—and whether the CAE system is or is not integrated—one piece of software is crucial: the simulator. As soon as a logic circuit exists on paper—or, more accurately, in a data base—it must be exercised. A logic simulator acts on paper logic in much the same way that a logic analyzer would for actual logic. The one exception is that the simulator's diagnosis depends entirely on the quality of the model.

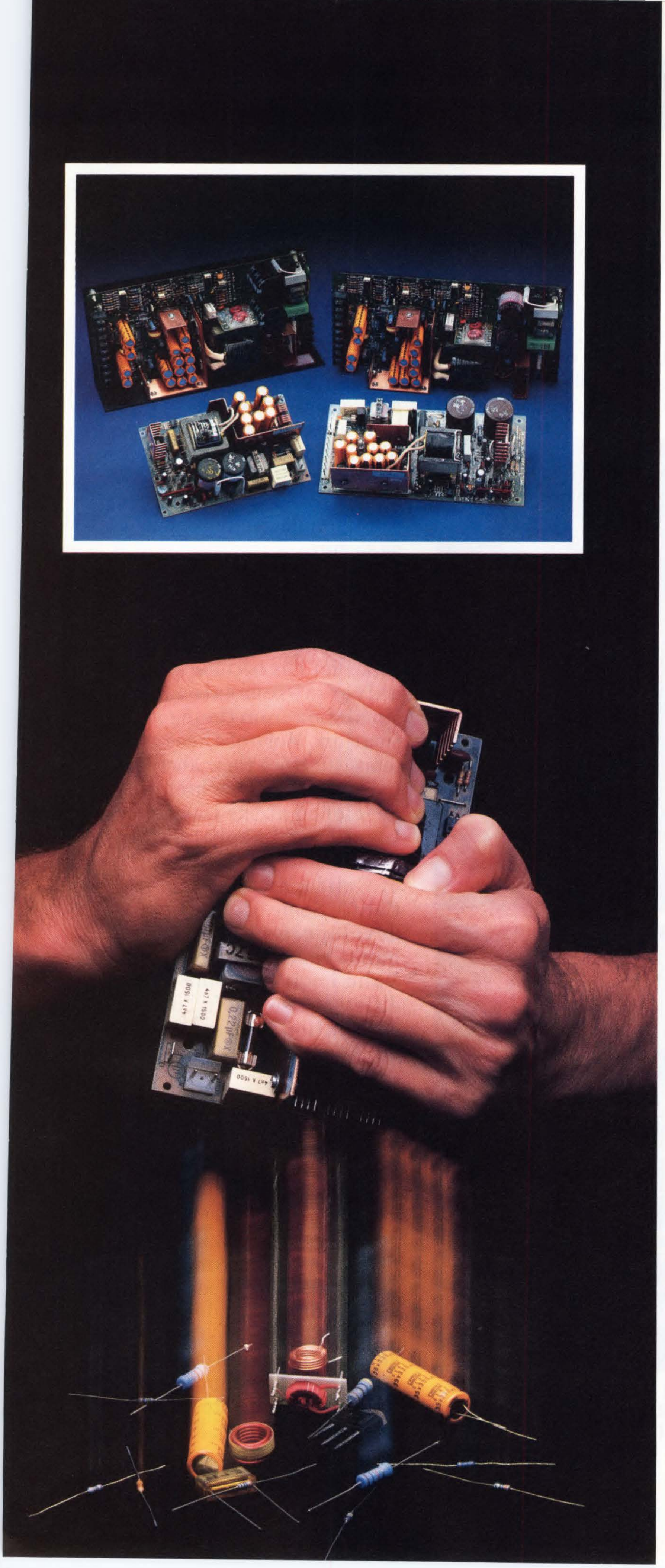
In the early days of design automation, TEGAS was the preferred simulator, running on a mainframe or superminicomputer like the VAX-11/780. A VAX-based integrated CAE system like TegaStation, from Calma Inc. (Austin, Texas), can afford to use that well-proven system. Although many TEGAS dialects are in the public domain, CC-TEGAS, from Comprehensive Computing Systems (also in Austin), is a typical example of a commercial version. It combines eight-level simulation with verification, fault simulation, and test generation. Like its progenitor, it also runs on a VAX-11/780. Perhaps CC-TEGAS's most valuable feature is its large library of functional elements (from shift register to ALU), which greatly speed simulation.

### A new generation

The emergence of design automation has spurred the creation of several new simulators that try to overcome TEGAS's biggest handicap—its slow speed. One solution is mixed-mode simulation, which works at the switch, gate, and functional level and is intrinsically more efficient than switch-level simulation (see the table). Hilo-2 devised by Cirrus Computers (Maidenhead, England) is now distributed in the U.S. by GenRad Inc. (Santa Clara, Calif.). The package has already found its way into several CAE systems including those from Metheus-Computervision (Hillsboro, Ore.) and CAE Systems Inc. (Sunnyvale, Calif.). Based on similar concepts, Cadat, from HHB-Softron (Mahwah, N.J.), is also making its way in the world, primarily because of its fault simulation features. It is now available on systems from Cadnetix Corp. (Boulder, Colo.), Mentor Graphics, and Via Systems.

### It's interactive

Most mixed-level simulators handle about 1000 to 2000 events (logic changes) every second, using a VAX-11/780. A new entry, Themis, equals this speed on a Prime 730 computer, for which it was developed. Functional components at the register transfer level can be defined in the TAD (Themis architectural design) language (Fig. 4, top). Themis stands out as a fully interactive simulator; any run can be stopped and restarted, even if changes are made to the simulated circuit or if it is incomplete. Furthermore, it permits as many as six different delays to be assigned to any gate output. Such flexibility is sorely



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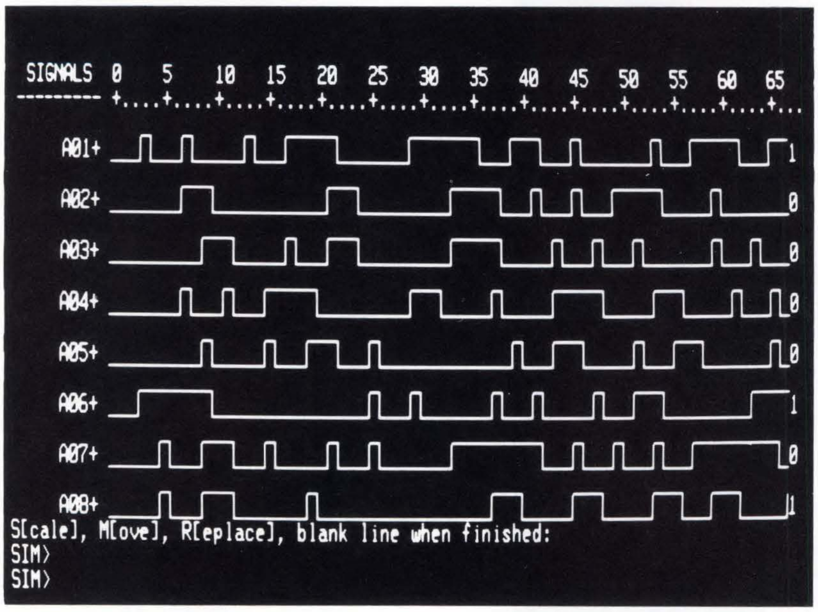
**Sierracin/Power Systems**

lacking in many simulators. What's more, the user can define probes anywhere in the circuit to analyze waveforms (Fig. 4, bottom).

Of all the system designers who will eventually work with application-specific chips, only a small fraction have access to a VAX. In fact, surveys have revealed that only about 10% are equipped to perform any logic or timing simulation at all. The remainder will have to make do with modest computer resources, such as those offered by workstations. Those tools are strained even by fairly small circuits. For example, a circuit with an 8-bit ripple counter, a 2-bit shift register, and some random logic—about 80 gates altogether—requires from 10 to 40 s to simulate on the major CAE workstations. On a system built around an IBM PC personal computer, the same simulation took as long as 45 min.

```
CREATE COMPONENT REG16
   ADD PINS
      DIN(0:15)  INPUT PASSIVE
      DOUT(0:15) OUTPUT
      CLK        INPUT CLOCK;
   ADD FUNCTION
      REGISTER
        REG[15:0];
   TAD
      IF CLK=+ THEN DO              /* LOAD MASTER ON RISING EDGE */
         REG=DIN(15:0)
         END
      ELSE DO                       /* LOAD SLAVE ON FALLING EDGE */
         DOUT(15:0)=REG
         END
   EXIT
   END FUNCTION
END COMPONENT
```




**4. For simulation with Themis, a component is described in a hardware language (top). The waveforms at arbitrarily selected nodes mimic those obtained with a logic analyzer (bottom).**

It is no wonder, then, that the CAE industry has expended a great deal of effort to speed up simulation. One tack that has become almost universal separates logic simulation from timing verification. Most of these systems can trace their ancestry back to SCALD, which was developed at the Lawrence Livermore Laboratory, an affiliate of the University of California (Livermore, Calif.). Some of its principal developers went on to enhance the original system. Valid Logic's version added different rise and fall delays, correlation between varied circuit events, and reconvergent fan-out.

By eliminating timing analysis, logic simulators have been sped up about threefold, assuming a nine-level logic model. In the beginning, SCALD and its counterparts worked with four levels: 0, 1, unknown, and high impedance. Today, most simulators have added from two to four signal strengths, so that uncertainties can be resolved—for example, when a line is connected to a 0 and a 1 at the same time. Most sys-

tems now offer from 9 to 16 logic states. Internally a larger number can be used, as in the Daisy Logician, which handles models tailored to specific foundries. Valid's 16 normal states are supplemented with 4 special cases, bringing the total to 20. Too many strengths, however, can lead to erroneous results.

### Perfect timing

Under SCALD, signal timing is calculated from the minimum and maximum propagation delays of all components and from the transmission line delays obtained from the physical configuration. SCALD associates a number of properties with each signal: stable (S) or changing (C), rising (R) or falling (F), and unknown (U). Established tables determine which properties apply to the outputs of different gates, depending on the properties of the inputs (Fig. 5).

Under SCALD, if a signal line were described as

CK.C0-4 & Z

it would indicate that the signal CK.C is high from time 0 to 4. An instruction, Z, tells the user that it refers to the time at which the output, rather than the input, of the gate changes.

In general, SCALD tries to verify timing once for every signal change; in some cases this can lead to overly pessimistic predictions concerning an output's stability. If, for example, two multiplexers with different delays operate in series, the timing verifier would calculate the worst-case timing without realizing that some combinations are impossible. Under these circumstances, the program's CASE construct can be invoked, analyzing the different alternatives in successive clock cycles. The current SCALD verifier samples a circuit every picosecond to reveal any hazard or instability.

### Step it up!

In spite of separating logic and timing analysis, requiring 100 to 500 ms for a gate (as implied by the 80-gate benchmark) and calling for about 500 to 1000 events/s (as defined by several manufacturers) make for agonizing delays as the circuit grows. Most CAE systems therefore are or soon will be equipped with hardware accelerators—additional processors for integer arithmetic. These speed the simulation dramatically. Daisy's Megalogician, which contains three such dedicated processors, runs 100 times faster than the Logician, which has none. For the ultimate in simulation speed, special-purpose computers like IBM's Logic simulation machine are needed. It zips through 1000 gates in about 1 ms, and NEC Corp.'s HAL (hardware logic), simulates 1.5 million gates in a 5-ms cycle.

One other parameter must not be overlooked when selecting simulation hardware—memory requirements. By and large, each gate consumes between 40 and 100 bytes of memory (not counting system overhead) for the simulation alone. Systems that cannot accommodate functional-level components must replace them with lower-level representations. Doing so results in huge storage and speed penalties. A modest 1000-gate circuit thus can easily consume a megabyte of RAM; for larger circuits, disk swapping may stall the simulation altogether.

### Gluing together models

A number of systems have evolved from a particular microprocessor, accumulating more and more glue logic with each enhancement. Even though application-specific ICs make sense as substitutes for the glue, they will rarely

| A ↓ / B → | 0 | 1 | S | C | R | F | U |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | S | C | R | F | U |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S | S | 1 | S | C | R | F | U |
| C | C | 1 | C | C | C | C | U |
| R | R | 1 | R | C | R | C | U |
| F | F | 1 | F | C | C | F | U |
| U | U | 1 | U | U | U | U | U |

**(a)**

| A ↓ / B → | 0 | 1 | S | C | R | F | U |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | S | C | R | F | U |
| S | 0 | S | S | C | R | F | U |
| C | 0 | C | C | C | C | C | U |
| R | 0 | R | R | C | R | C | U |
| F | 0 | F | F | C | C | F | U |
| U | 0 | U | U | U | U | U | U |

**(b)**

**5. SCALD derives signal shapes at a gate's output from those at the inputs: stable (S), changing (C), rising (R), falling (F), or unknown (U) as the truth tables for an OR gate (a) or an AND gate (b) show.**

be used to replace, say, an 8086. But to simulate the system, a high-level description of the CPU is certainly needed. The trouble is, nobody offers such a model, and designers certainly have no time to create one. Besides, a model of such complexity could slow the simulator to a crawl.

CAE manufacturers have risen to the challenge: Valid with its Realchip and Daisy with its PMX (physical modeling extension). The first permits as many as 64 components with up to 64 pins each to plug into an adapter board (A 114-pin 68020 has also been used). The simulator then feeds its signals into the actual devices and passes the outputs on to the simulated part of the circuitry.

When an application-specific chip becomes available, it too can be plugged into Realchip, enabling the designer to see how it stacks up against his model.

With all their limitations and pitfalls, logic simulators present an attractive candidate for elimination. A desirable alternative would be to prove mathematically that a circuit is correct. Research toward this end has come a long way, especially at Fairchild Laboratories (Palo Alto, Calif.). Verify, a program implemented in Prolog, accepts functional and structural descriptions of a component and determines whether the highest-level description agrees with the one derived from lower levels, all the way down to individual switches (i.e., idealized transistors).

The great advantage to this approach is that a component, once proven correct, need never be tested again. Consequently, the test effort grows only proportionally to the number of modules rather than exponentially or factorially. Individual modules are checked numerically and exhaustively if the number of test combinations is under 40; otherwise, algebraic simplification prevails.

One example, consisting of three multipliers and two adders (described with 400 Prolog statements), was broken down into 49 different types of modules. Eventually it was reduced to nearly 30,000 primitive parts, including over 18,000 transistors. It was proven correct in 10 minutes of CPU time on a DECsystem 2060, and the complete trace of the proof took up 4800 lines of output. The proof holds for all of the 134 million possible input patterns. No timing verification has yet been implemented, but that should not prove difficult.

### Analog—alive and well

If an application-specific IC contains analog components, to obtain exact digital models for digital circuits the system designer may have to resort to an analog simulator like Spice. Created originally at the University of California at Berkeley, Spice has evolved into many versions. Users of integrated CAE systems usually must be content with the one that the system handles, hoping that it achieves the requisite balance between accuracy and execution speed. If large circuits must be modeled, a system should be chosen that permits a Spice input file to be transmitted to a remote mainframe. By running Spice on a VAX, the Daisy user can speed a simulation three to six times. Mentor recommends carrying out MSpice runs either on a mainframe or on the most powerful Apollo node the designer has access to. But the company also furnishes a bridge for transferring the net list to QSpice, which runs on a floating-point array processor.

Naturally, analog simulation is essential for analog chips and for hybrid designs. For communications hardware, chips with switched-capacitor circuits, which also function like analog components, are popular. The Starcap system, from Silvar-Lisco (Menlo Park, Calif.), works with analog components and contains a special simulator for switched capacitors, Swap, for frequency-domain calculations of amplitude, phase, and group delay.

Analog designers can now get a dedicated workstation of their own from Analog Design Tools Inc. (also of Menlo Park). The 68000-based system (ELECTRONIC DESIGN, Aug. 9, p. 283) draws on a library of analog ICs and components and displays results in the time and frequency domain. Another useful tool is the Simon Simulator from Simon Software (San Jose, Calif.). It accepts Spice input files that contain as many as 10,000 transistors but works up to 20 times faster than Spice.□

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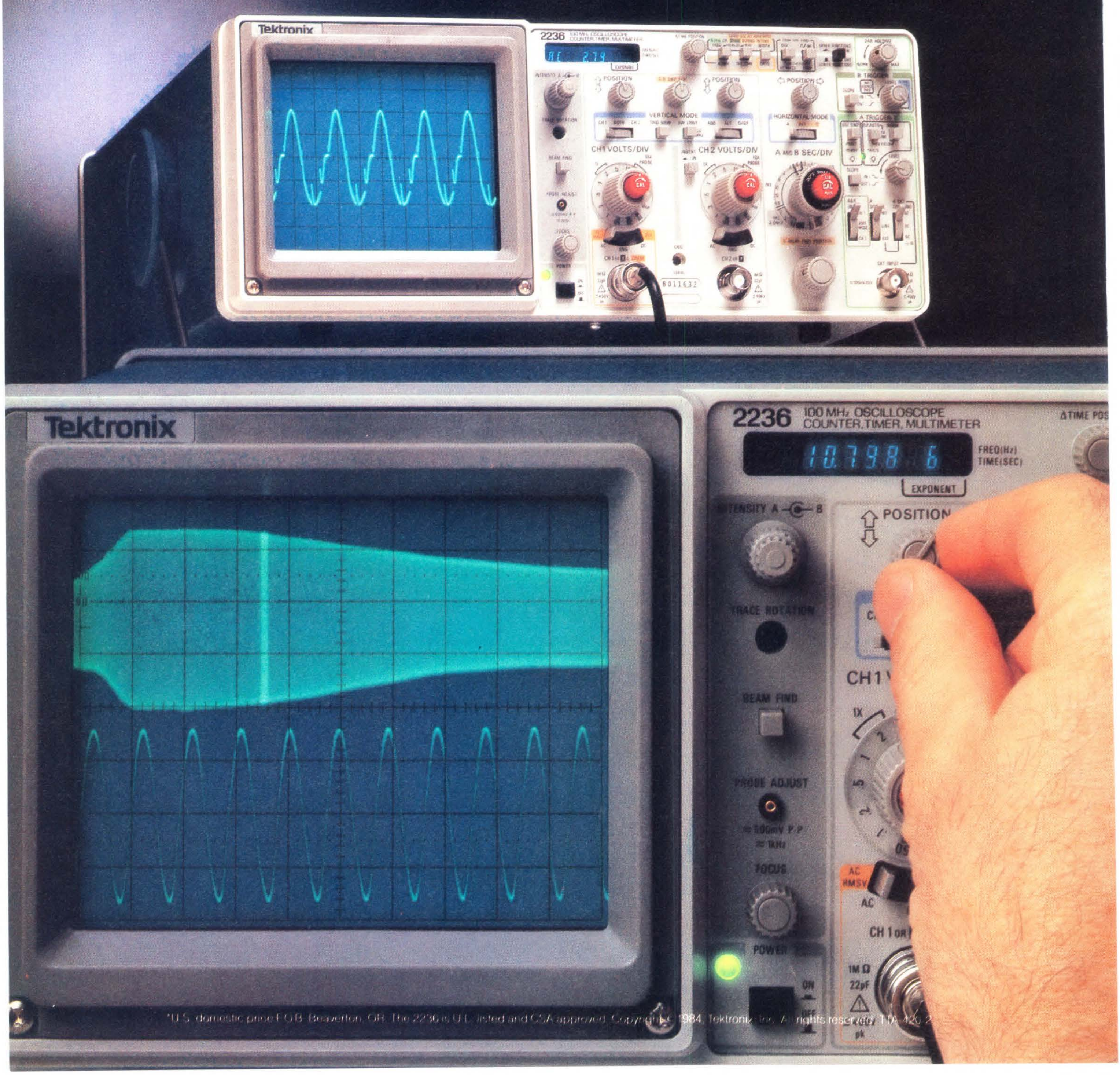

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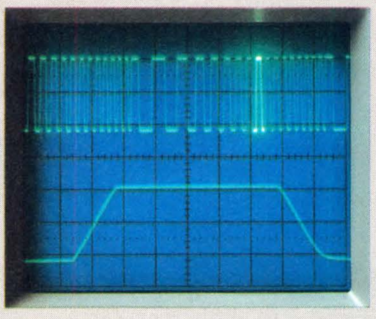
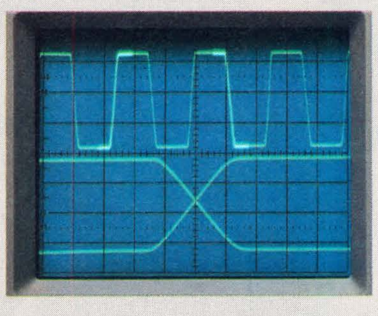


**Gated width measurement.** Pulse of interest is selected with the intensified zone. Both width and period measurements are made with up to 10 ps resolution.



**Delta time measurement.** Time between two intensified zones on the A sweep is measured with up to 50 ps accuracy.

**Left top: Ch 1 true RMS & DC volts measurements.** Made easily at the probe tip. (The 2236 adjusts automatically to 1X or 10X probes.) The 2236 includes relative reference capability for subtracting offsets.

**Left bottom: Gated frequency measurement.** Intensified zone brackets the period of interest by means of the delayed sweep, allowing easy frequency measurement on any specified portion of the waveform.

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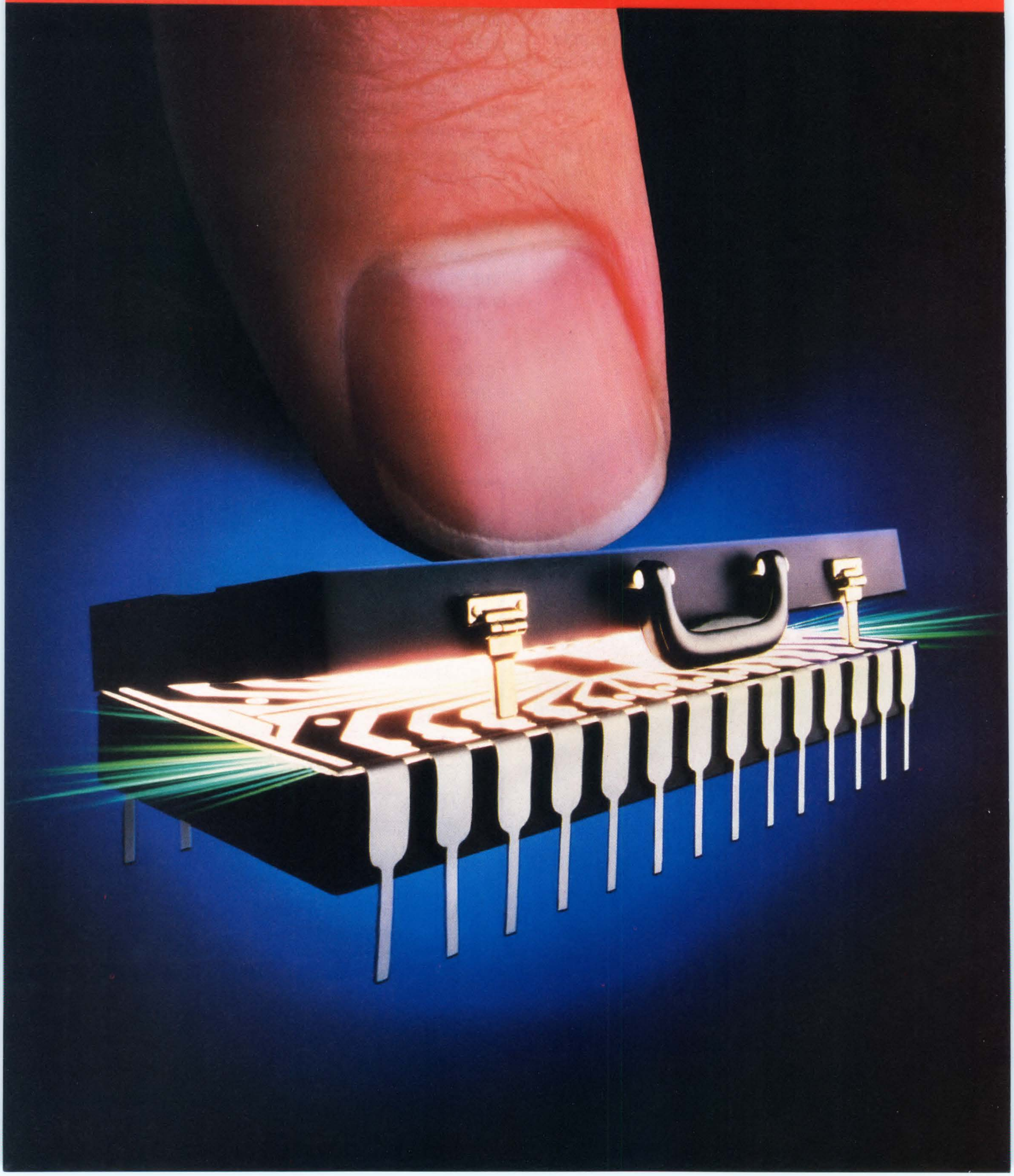

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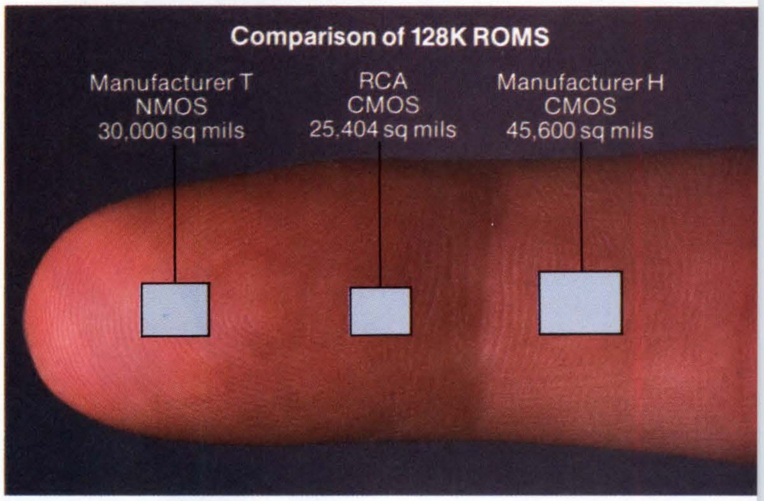


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# DESIGN ENTRY

# Silicon compiler teams with VLSI workstation to customize CMOS ICs

*A silicon compiler strengthens the muscle of a VLSI design station, letting system builders pack more punch into their application-specific chips.*

Using gate arrays and standard cells, system designers have been weaving their ideas into application-specific ICs. But when circuit density and performance are considered, those chips fall behind handcrafted circuits, which have been the sole domain of a few experienced designers and manufacturers with considerable resources.

The integration of silicon compilation software into an engineering workstation enables system designers to translate their projects into fully custom chips that approach the efficiency of handcrafted ones—without needing the IC expertise. Moreover, the workstation setup is an economical one, and the semiconductor technology to which the results apply is the popular CMOS process.

The chips, produced with a silicon compiler from Seattle Silicon Technology that runs on Valid Logic's SCALDsystem, typically reach 90% of the density and 100% of the performance of their manually customized counterparts. Furthermore, they are 25% to 40% smaller than comparable standard-cell designs and 50% to 70% smaller than gate arrays (see "Trading the Old for the New," p. 150).

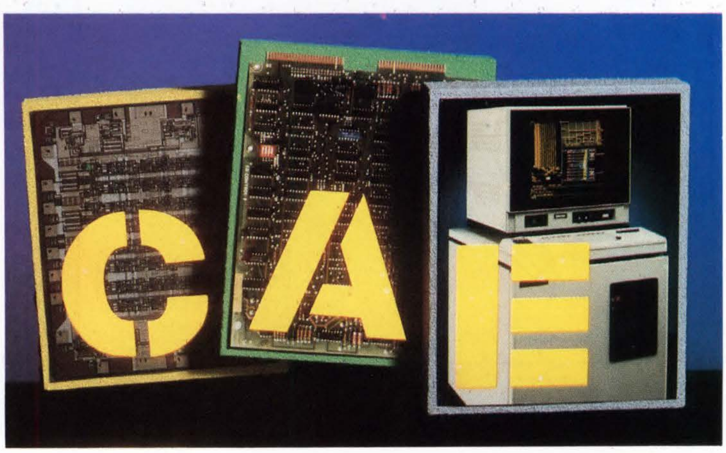
Silicon-compiled designs are also independent of any one set of design rules. As a result, an


**Benjamin Lee** and **Donald Ritzman**
Valid Logic Systems Inc.
**Warren Snapp**, Seattle Silicon Technology Inc.

*Last April Benjamin Lee joined Valid Logic in Palo Alto, Calif., bringing 16 years of IC experience to his position as CAD manager. Previously he helped invent Calma's Stick, the first dynamic symbolic layout software, and he designed the world's first bipolar fusible PROM.*

*Donald Ritzman joined Valid Logic last March as a product marketing manager for application-specific IC design tools. Before that he worked as the product marketing manager for Fairchild's high-performance ECL gate arrays. He holds a patent on a power supply designed with custom logic.*

*Warren Snapp is vice-president of engineering for Seattle Silicon in Bellevue, Wash. Before coming on board in February, he developed high-performance signal processors for Boeing and served as a senior architect of VHSIC activities for TRW's space and defense group.*

## CAE: CMOS silicon compiler

IC can easily be configured for numerous manufacturing sources. The user need only recompile a design once for each source. Such freedom lets designers immediately exploit the latest advances in processing technology.

### Climbing aboard the station

The silicon compiler software is the latest addition to a Unix-based VLSI design workstation equipped to build and completely validate circuits. With its built-in utilities, the workstation can edit graphics and layouts, verify timing, simulate logic, generate a net list, and check design and electrical rules.

A unique feature is the workstation's dual display: a monochromatic screen for capturing schematics, and a color screen for illustrating the physical layout of a chip. With two displays the designer can simultaneously observe the logical and physical aspects of the project.

Within the system the silicon compiler transforms information generated by the graphics editor into a format that resembles—as closely as possible—the physical layout of a handcrafted IC. And though users need not necessarily have vast design experience, if they do,

## Trading the old for the new

Designing an application-specific circuit means weighing the trade-offs among gate arrays, standard cells, handcrafted custom chips, and now silicon compilation. The pace at which electronics technology marches on demands a closer look at each.

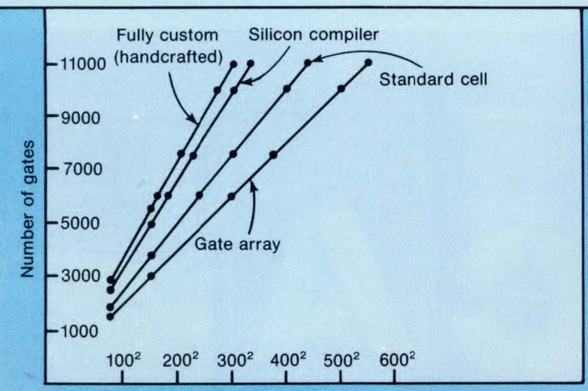
Gate arrays for years have been the most popular design element because of their modest design time (four to six months) and their relatively low development cost. But gate arrays are starting to encounter problems, since they pack only a small number of gates into a given area, typically about 10,000 gates over 450 square mils. Furthermore, the IC world pegs production cost to die size, a fact that places practical limits on a gate array's complexity. Nevertheless, gate arrays remain the technology of choice for designs containing fewer than 10,000 elements and for production runs of up to 50,000 units.

In comparison, standard cells are more versatile than gate arrays, since their highly optimized functional characteristics and layout ultimately create chips that squeeze more gates into less space. Furthermore, unlike preprocessed gate arrays, standard-cell wafers are processed only after the design is finalized.

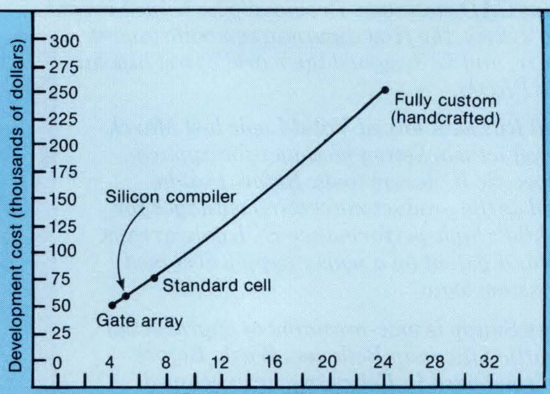
On the minus side, the design and fabrication techniques are more strenuous than for gate arrays and silicon-compiled chips, making their development time longer and their cost greater.

As systems grow larger and more complex, designs born of silicon compilers prove more economical. The custom nature of the technique results in dies that are smaller than those for gate arrays (Fig. A). Silicon-compiled circuits fall between gate arrays and standard cells in both development time and cost, even though their circuit densities surpass standard cells' by 25% to 40% (Fig. B).

Full appreciation of silicon compilation comes only through comparison with handcrafted chips. Research suggests that on the average, the gate density of compiled chips comes within 10% of handcrafted ones, but at one-fifth to one-tenth the overhead. Perhaps more important, silicon compilation requires no substantial design experience, a prerequisite for manually customized chips.



(A)



(B)

they can invoke the system's tools and manually modify the layout to maximize density.

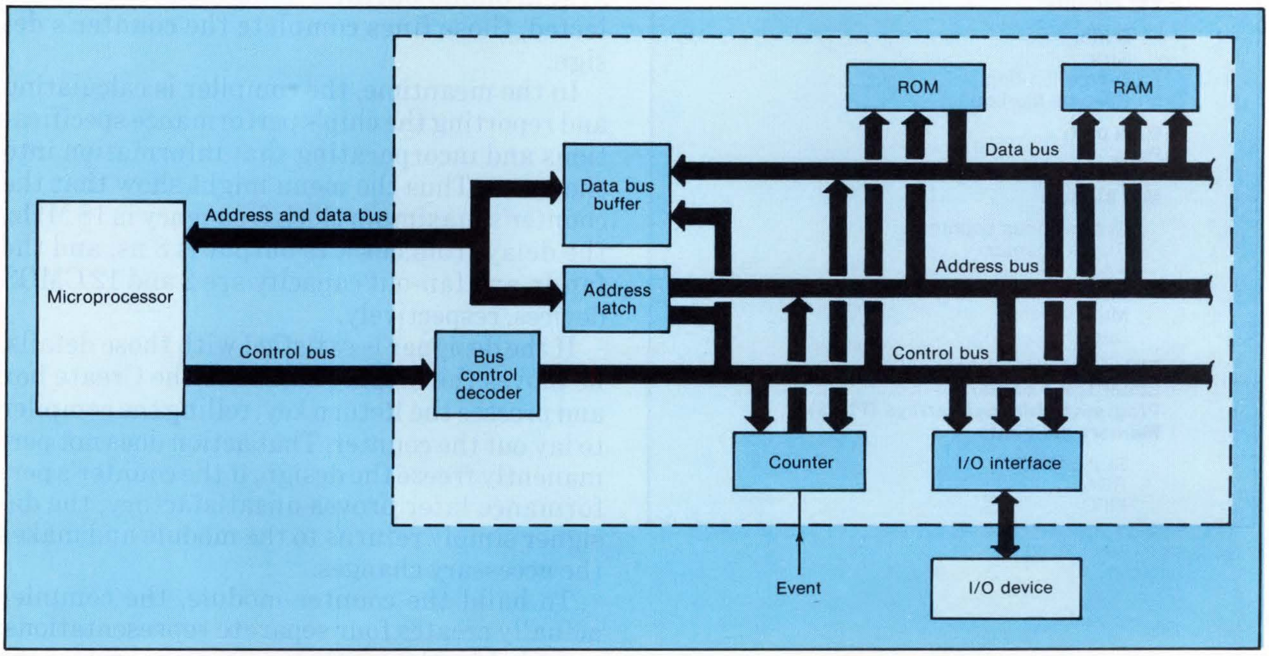
To illustrate the interaction of silicon compilation with the other workstation tools, consider a simple microprocessor-based system containing a program ROM and a data RAM, as well as a bus control decoder, a bidirectional data bus buffer, an address latch, an event counter, and an I/O interface (Fig. 1). Normally, a dozen or so MSI devices would make up the system, but they would eat up 20 or 30 square inches of board space. On the other hand, a considerable amount of production time and repair work could be saved if the system was built with a microprocessor and one custom chip, the latter developed with the workstation's compiler software.

For the first step, the graphics editor creates a detailed system block diagram. Some of the details should also be defined—the bus and control structure, for example, and some basic characteristics of each functional block, like bit width and fan-out.

### Decision time

After defining those details, the designer decides which compiler modules should be used to construct each functional block. As with standard logic, the modules span a full range of digital circuits and architectures (see the table, p. 152), all of which are accessed initially through a top-level menu.

There the designer is presented with the major compiler module groups—MSI circuits, programmable logic arrays, memory elements, data paths, and so on. Sharing the top-level menu is a box, labeled Rule Set, into which the designer inserts the design rules for compiling




**1. A simple microprocessor-controlled system built with a dozen or so MSI circuits takes up about 20 or 30 square inches of board area (inside dashed lines). Using a workstation-based CMOS silicon compiler, the same system can be reduced to a fully custom VLSI circuit that saves considerable space and power while cutting production and repair costs.**

the subsequent modules.

Assume that a designer wants to create a synchronous counter within the chip (Fig. 2). He first invokes the top-level menu by entering the compiler software's name (here, "Concorde") and then selects the MSI group by moving the cursor to that box and pressing the Return key. The MSI menu appears, offering several selections, among them the synchronous counter. When picked, another menu gives the designer several options for the counter's details.

Those options, unlike those of standard logic, gate arrays, and standard cells, place few constraints on a designer's imagination. For instance, a standard-cell counter has fixed features: counting mechanism (up, down, or both), number of bits, and fan-out. For a compiled counter, the user can customize nearly at will. He starts by giving the module's name—either a previous design (for modification) or a new design with a previously unassigned name. Next, he specifies the counter type—up or down or up and down—and finally the number of bits, any value from 2 to 99.

**Silicon compiler digital modules**

**SSI circuits**
- Buffer
- Strip
- D-type flip-flop
- RS-type flip-flop

**Data path**
**Pads**
**Programmable array logic (PAL) devices**
**MSI circuits**
- Synchronous counter
- Ripple counter
- Adder
- Shift register
- Multiplexer
- Decoder

**Flair ("folded" PLAs)**
**Elmer (glue chips)**
**Programmable logic arrays (PLAs)**
**Memory elements**
- Static RAM
- ROM
- FIFO

### Building a better buffer

Next is the buffer size, which determines the counter's fan-out capability by adjusting the size of its output transistor. A buffer size of 4×, for instance, produces a transistor that is four times larger than the default size and that can drive 12 CMOS loads.

The designer then has the option of adding enable, asynchronous preset and clear, and synchronous parallel-load inputs. Once selected, those lines complete the counter's design.

In the meantime, the compiler is calculating and reporting the chip's performance specifications and incorporating that information into the menu. Thus the menu might show that the counter's maximum clock frequency is 18 MHz, the delay from clock to output is 8 ns, and the fan-in and fan-out capacity are 2 and 12 CMOS devices, respectively.

If the designer is satisfied with those details, he moves the display cursor to the Create box and presses the Return key, telling the compiler to lay out the counter. That action does not permanently freeze the design; if the counter's performance later proves unsatisfactory, the designer simply returns to the module and makes the necessary changes.

To build the counter module, the compiler actually creates four separate representations: a symbol for the graphics editor, a model for the logic simulator, a footprint (that is, a boundary with connector points) for routing the counter's I/O connections, and the actual layout geometry. All four representations are stored in a data base, where they can be accessed by other workstation tools (Fig. 3).

The graphics editor uses the data to draw schematic symbols of each module constructed. The schematic, in turn, becomes the design data base, which along with the simulation model

## CAE: CMOS silicon compiler

verifies the design's logic and timing. In addition, each module's geometry and footprint become part of the layout data base, which is accessed by the silicon compiler's interconnection router.

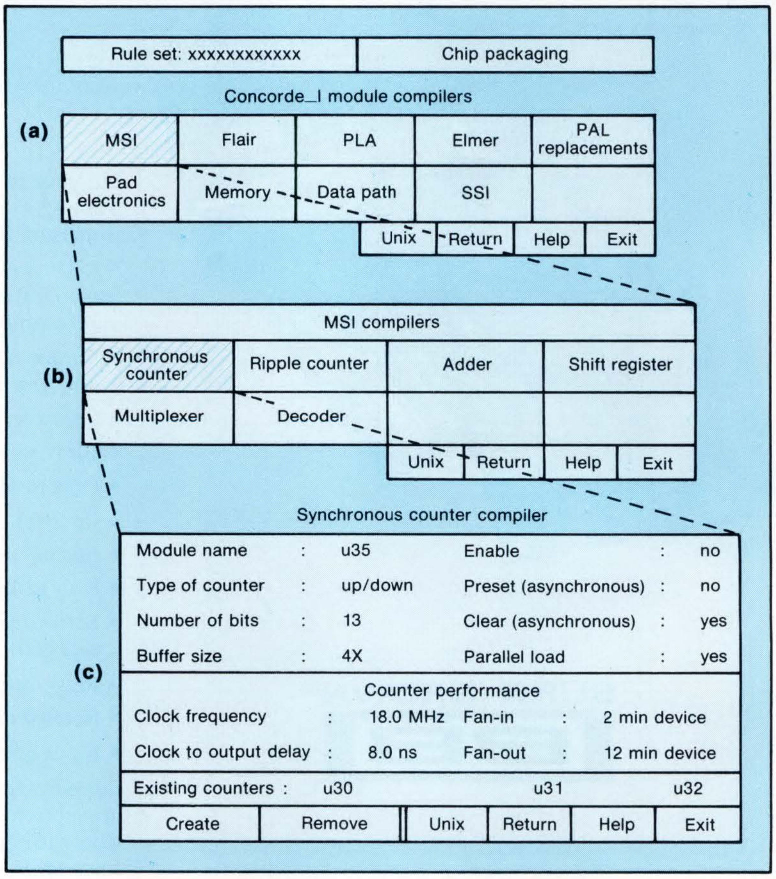
### Three-way routing

The designer can handle routing in three ways. First, it can be done automatically, on the basis of the schematic. This method invariably proves best for chips composed of only one module, since it involves only the pad electronics and the bonding pads. When several modules are involved, the designer can invoke an interactive symbolic router that selectively enhances the results of the automatic routing. Finally, experienced designers can use the workstation's layout editor to route the interconnections manually.

However achieved, routing clears the way for producing the actual chip, starting with the pattern-generation tape, which coincidentally is also one of the last steps for the workstation. The tape is turned over to the silicon foundry, which makes the production masks that are needed for the chip fabrication process.

### Test for success

With the newly produced chips in hand, the designer ironically faces one of the most difficult tasks of the entire process: testing the ICs against the original design. Again, the workstation helps cut through the problem. Using its good and faulty circuit simulator (called Lasar



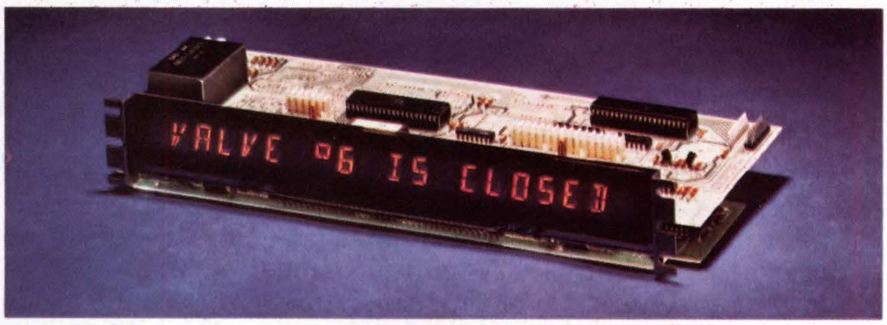

**2. To build a functional module, the silicon compiler starts with a top-level menu that the designer uses to select rules and the appropriate modules (a). Picking the MSI group from the first menu produces another menu that displays the assortment of MSI compiler modules (b). After the designer chooses synchronous counters, the compiler brings up yet another menu presenting the options and parameters for the counters (c).**

# *Programmable Controller Newsbrief*

# New PC display system reduces down-time, increases productivity

**F. A. Amendola**
Cherry Electrical Products Corp.
Waukegan, IL

## Cherry unit adds diagnostics and operator prompting in understandable printed messages to any programmable controller. Cost: less than $300



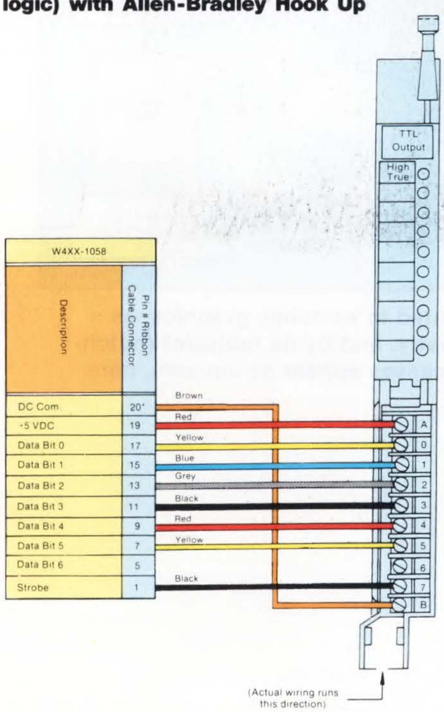

**Cherry No. W424-1058, 24 character display system complete with all on-board electronics.**

If your programmable controller is not equipped with a serial ASCII output port, you may not be realizing all of its potential productivity. In its present state it is unable to output information for operator prompting or provide diagnostic information in immediately understandable messages for your maintenance staff. Of course the information is being supplied by your PC, but in the form of signals or shut-offs or complicated codes.

The new Cherry display system literally adds literacy to any programmable controller with TTL output drivers, 5 VDC. Instead of using cumbersome look-up tables to translate output codes, your operator is given any of up to 64 messages of up to 32 characters each, spelled out on a bright, easy-to-read display panel. A flashing mode attracts attention to potential trouble such as slipping belts, stuck valves or overheating. Your operator is constantly and instantly supplied with pertinent, *understandable* information about all critical phases of production under your host system's control.

At a cost of less than $300 in OEM quantities this new unit compares with others costing over $1000. It is estimated that the addition of this Cherry display system to your host system will pay for itself in just a few months by decreasing frequency of down time, in improved maintenance and increased machine efficiency.

**Typical configuration (positive logic) with Allen-Bradley Hook Up**




## Easy to install—a complete message center

You just connect two color-coded cables (one power and one signal) and the Cherry unit is ready to take the PCs output drivers and provide output decoding of up to 64 easily programmable messages...anything from "BIN 4 EMPTY" to "ET PHONE HOME." No hardware changes or additions.

This new Cherry unit is a piece of straight-forward engineering consisting of complete on-board electronics and a flat gas discharge display panel of 24 half-inch high characters in bright orange easily readable in any ambience. (Longer messages may be scrolled.) Unit has built in capability for longer scrolled messages and a flashing mode.

**Sample Program (message: VALVE #6 IS CLOSED) Starting location HEX 000**

| HEX CODE | DESCRIPTION |
|---|---|
| 10 | Blank Display—all messages must start with this |
| 0A | Line Feed—clears display |
| 0D | Carriage Return—puts cursor to far left |
| 12 | Display Recall—turns on display |
| 56 | V |
| 41 | A |
| 4C | L |
| 56 | V |
| 45 | E |
| 20 | Space |
| 23 | # |
| 36 | 6 |
| 20 | Space |
| 49 | I |
| 53 | S |
| 20 | Space |
| 43 | C |
| 4C | L |
| 4F | O |
| 53 | S |
| 45 | E |
| 44 | D |
| 89 | All messages must end with this |

## Complete information and specs available

Cherry will send you an 8-page instruction booklet that includes typical connections to various PCs plus application notes on sample programs and ribbon cable connections and Hex Number Addresses for messages in user's EPROM. Send for it today.

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## CAE: CMOS silicon compiler

6), the workstation generates a test pattern that, running on a commercial automatic tester, can verify that the custom ICs work as planned.

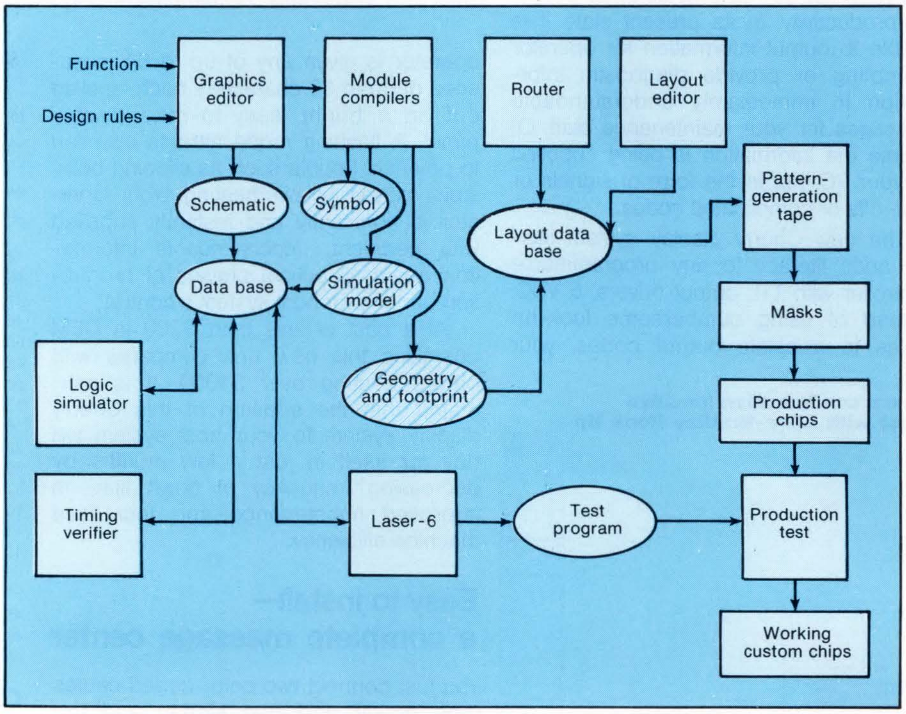
The multitude of functional modules is actually the silicon compiler's greatest resource for building dense, complex chips. With its 19 basic modules, the software gives designers a rich assortment (see the table again).

### A modular paradise

The SSI modules include a buffer, a strip, a D-type flip-flop, and an RS-type flip-flop. Of these, the first lets a designer create a customized buffer, tailor the number of its stages, and adjust the size ratios of its pull-up and pull-down transistors and of the transistors between its stages. The strip module generates rows of SSI cells such as two-, three-, or four-input NAND, NOR, OR, and XOR gates, as well as ordinary buffers and ones with three-state outputs. The modules for creating D- and RS-type flip-flops are self-explanatory but vary in terms of preset and clear controls, left- or right-side access, and drive capabilities.

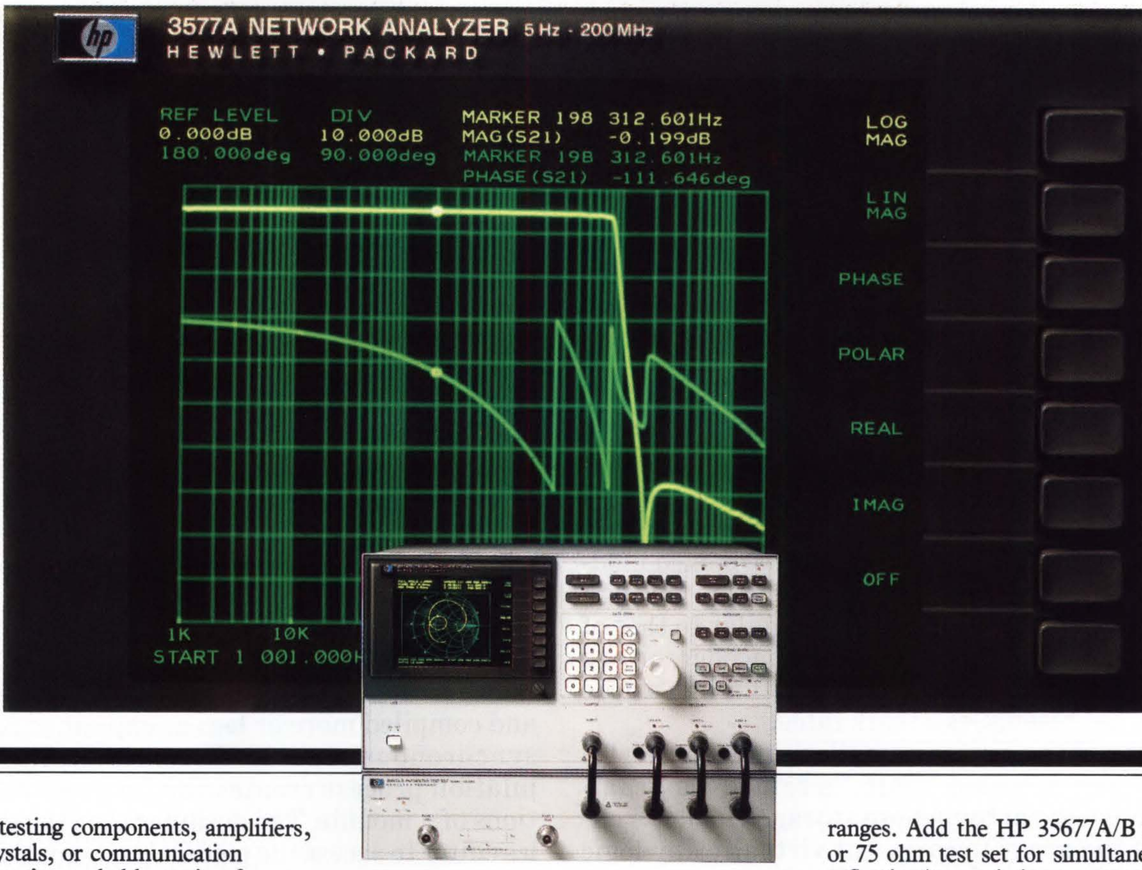
The data path module is a powerful tool for building columns of registers and logic blocks and then combining them with data buses. A specification language, not a menu, describes the data path module.

The designer can connect the custom chip to the outside world with the help of the pad module. As the user designs the pad electronics, the compiler indicates the module's physical size




**3. Once a module is compiled, it is represented in symbolic graphics, as a simulation module, in terms of layout geometry, and by its footprint (hatched ovals). In this operational summary, processes appear as squares, data as ovals, and hardware as rectangles.**

# Finally, high-performance network analysis from 5 Hz to 200 MHz ...for only $23,500*.

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**Filters.** Here's a major advance. For the first time, the HP 3577A lets you measure filters with 100 dB of stopband attenuation, and 0.001 Hz frequency setability. Ideal for crystal filters.

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and some of its electrical characteristics, such as static protection, propagation delay, and power consumption. For convenience, the compiler works with standard default pads as well.

Another compiler produces the CMOS equivalent of a programmable array logic (PAL) device, described in the format of PALASM, the PAL programming language. With this module, the user can design a PAL-only chip or add PAL circuitry to a larger chip. In addition, a standard PLA makes up another of the compiler's modules.

### Medium-scale selections

In the next group are six MSI modules that could be used to build a synchronous counter, a ripple counter, an adder, a shift register, a multiplexer, or a decoder. The details of each module (except for the decoder) are made through menu selections, in a manner similar to that of the synchronous counter. The decoder, on the other hand, defines its function through a code file that resembles a truth table.

One of the silicon compiler's most powerful modules is called "flair," a folded programmable logic array whose storage elements enable the array to carry out virtually any logic function. (The term "folded" refers to the space-saving layout of the actual chip, which interleaves the two major AND and OR arrays of the device.) Like the decoder module, flair functions are defined by a code file.

### Sticky situation

As its name suggests, the "elmer" compiler consists of the glue logic frequently used between large, complex elements. Essentially, it is both a router and a standard-cell compiler that works with SSI and MSI cells.

Finally, the last module group contains RAM, ROM, and FIFO registers. Like the MSI circuits, these are menu-driven, but unlike the others they can be laid out in a square, rectangular, or oblong floorplan for the final memory array. Memory arrays normally dominate the real estate on a custom chip; the compiler's ability to specify an array's shape helps the user optimize the chip space.

With the individual compiler modules now described in detail, the microprocessor-based system that served as the original example deserves a closer look (see Fig. 1 again). Recall that the construction phase starts with a block-level diagram that shows how a design will be partitioned. Here everything, save the microprocessor and the I/O device, is grouped into one custom chip.

Next, each block function is defined, and an appropriate module is selected to implement the function. For some of the functions—ROM, RAM, counter—the module choice is obvious. But, when several modules can serve the same purpose, the designers must make some decisions. For instance, the data bus buffers can be built with the strip, elmer, or PLA modules. Similarly, the address latch can be composed of D- or RS-type flip-flops or the flair PLA. Hardly a burden, the choice lets the designer make the most efficient use of the chip area or get the best performance.

### Building the base

The individual modules now must be defined and compiled more or less as explained for the synchronous counter. Essentially, the compilation process creates the four representations of a module. The designer uses the graphics editor to access the module's schematic symbol, and with an Add command and a puck (mouselike) positioning device, places the symbol on the monochromatic screen. A Wire command connects the separate modules to each other, as well as to any displayed symbols that represent devices retrieved from the workstation's device library. The resulting diagram becomes the design data base, on which subsequent steps draw to validate the design, generate the test program, and test the first parts.

With the diagram complete, the designer must confirm that the circuit, if built as displayed, will perform as intended. This step relies on the workstation's logic simulator. The compiler supplies the models of its modules. In addition, devices drawn from the workstation's library come with their own software models.

Extremely complex devices that are not in the library—say, a microprocessor—can be simulated through the workstation's hardware-based VLSI modeling scheme called Realchip (ELECTRONIC DESIGN, March 22, 1984, p. 167). That technique proves particularly important when the custom chip being developed

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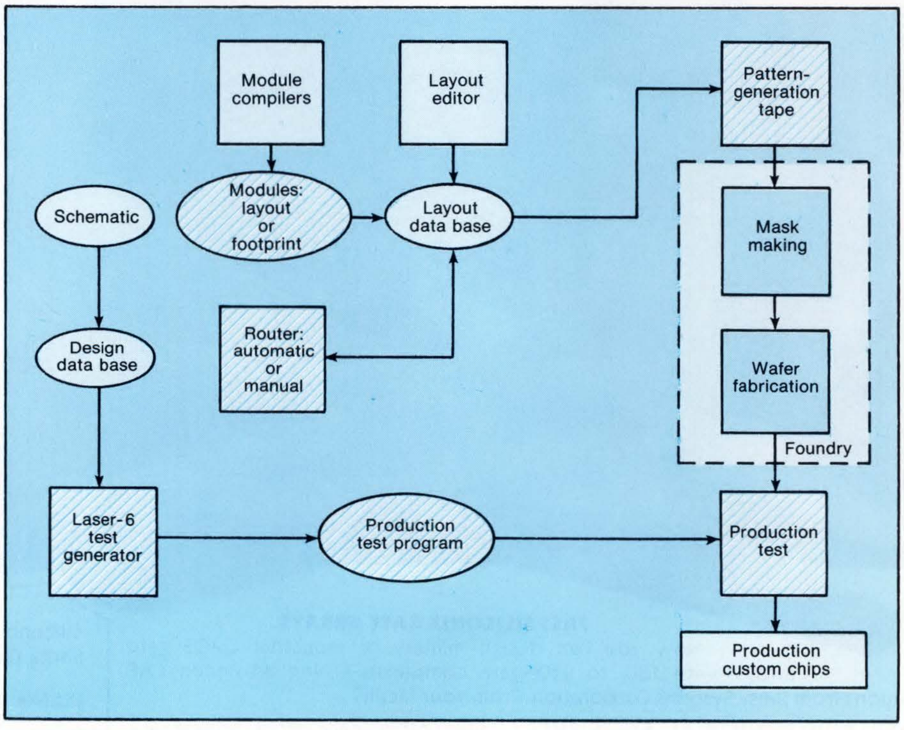
is part of a much larger and more complex system containing standard and custom VLSI devices. Moreover, the workstation can combine the hardware- and software-based models in the same simulation.

With all the circuit elements modeled, design verification proceeds interactively. The user supplies the stimuli, and the logic simulator responds by reporting the circuit's reaction. Should the circuit not act as expected, the user must return to the graphics editor and modify, recompile, and resimulate the circuit until it works as intended.

### Automatic arrangement

Once a design is verified, the workstation and compiler software perform most of the remaining steps automatically (Fig. 4). They place the modules and other circuit parts beside each other as they should appear on the chip, routing the interconnections between them, and creating the pattern-generation tape, with which the foundry produces the masks and eventually the custom chip.

As mentioned earlier, automatic routing, which draws on the original design data base to determine interconnectivity, is perfectly adequate for single-module chips. But for chips composed of more than one module, manual intervention is required for optimally placing and routing the circuit. Because fully manual routing demands an expertise in IC layout techniques beyond that of most system designers, another alternative lets users direct the placement of modules with the workstation's interactive symbolic router. Interconnections are left to software, which enforces the process design rules. In addition, the interactive router




**4. After a design has been validated, the workstation and compiler software tackle most of the remaining steps automatically. For instance, they place and route modules and their interconnections and generate a test program and pattern tape (hatched areas). As in Fig. 3, a square represents a process; an oval, data; a rectangle, hardware.**

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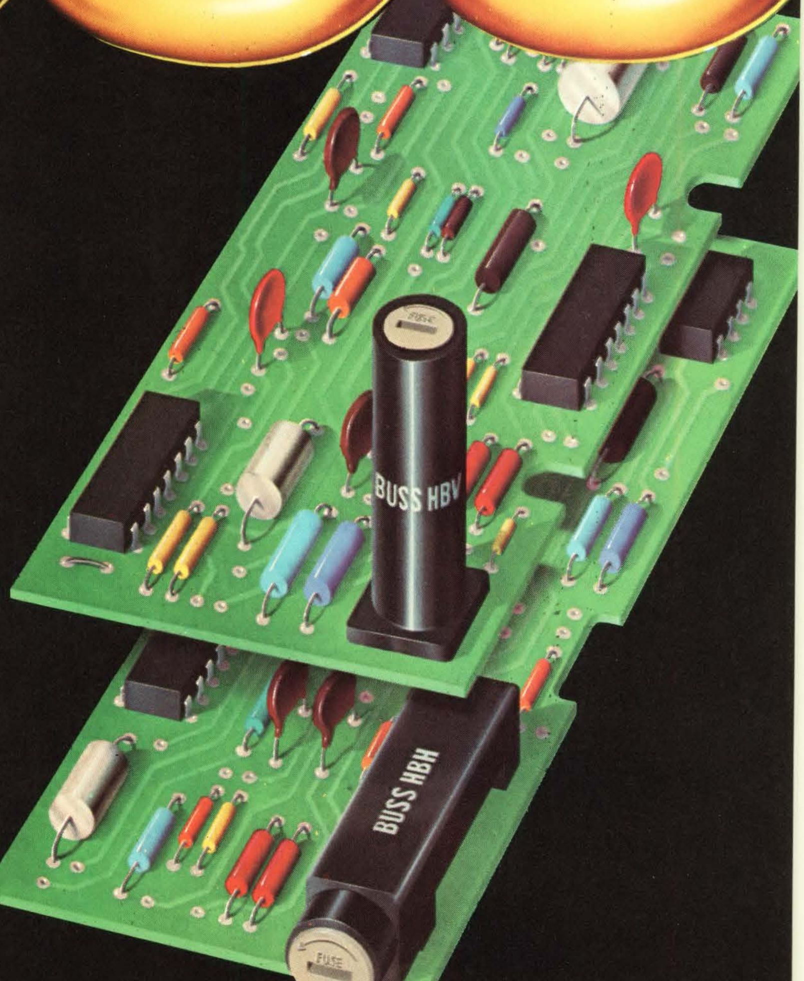
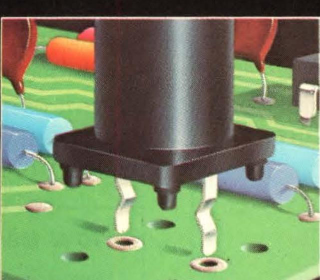



## New Buss International Fuseholder for PCBs stands up to the waves of automatic soldering.



Buss' new PCB - mountable International Fuseholder is making waves in the fuse business; it's the first to stand up against the rigors of high-speed production. Here's the up-to-the-minute answer for designers opting for the advantages of printed circuit boards. The Buss International Fuseholder meets both domestic and overseas requirements; it accepts both 5x20mm and 1/4 in.x1-1/4 in. fuses. Available in vertical and horizontal configurations. A kicked-leg design holds both types firmly to the board. They can't be vibrated off during wave soldering. The vertical version provides additional stability pins to secure it tightly during soldering. This Buss design is sensitive to all the exigencies of your manufacturing procedure. For example, an exclusive Buss feature prevents flux wicking. The Buss International Fuseholder for PCBs is designed to meet UL, CSA, VDE and SEMKO standards. For complete specifications phone your local Buss distributor today. Or call Bussmann Division, McGraw-Edison-Company, P.O. Box 14460, St. Louis, MO. 63178. Phone (314) 527-3877 for Order Service.

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## CAE: CMOS silicon compiler

enables the design to be recompiled without further manual intervention.

When routing is complete, the time comes to evaluate the effects of interconnection capacitance and other parameters on the circuit. The method, advisable at this point, resimulates the circuit to get a more accurate indication of how the actual hardware will perform.

### Fine-tuning the timing

If there is any doubt about performance, like timing tolerances that are particularly tight, the designer can simulate the timing at a higher degree of accuracy. Normally simulation at the module level assumes average timing values, but the workstation can also calculate delays at the switch (transistor) level and thus obtain a more precise timing picture. The designer invokes a workstation program that extracts the transistor connections from the gate-level layout.

Finally, for the ultimate timing analysis, the designer can turn to the Spice simulator. The designer wishing to invoke Spice has the choice of running it either on the workstation or externally.

Once all timing issues are resolved to the designer's satisfaction, the workstation produces a pattern-generation tape. If more than one silicon foundry will be fabricating the chip, the design is recompiled according to each foundry's design rules and a separate tape is created for each silicon maker.

Finally, with first silicon in hand, the designer tests the circuits again by creating a hardware model from the actual chips, using Realchip modeling. The stimulus test patterns that verified the software model are then applied to the actual hardware. If the hardware's response pattern matches that of the software model, the chips are working properly. Furthermore, the test vectors that verify the first silicon can be run later on automatic testing equipment to check for manufacturing flaws in production chips. □

| How useful? | Circle |
|---|---|
| Immediate design application | 541 |
| Within the next year | 542 |
| Not applicable | 543 |

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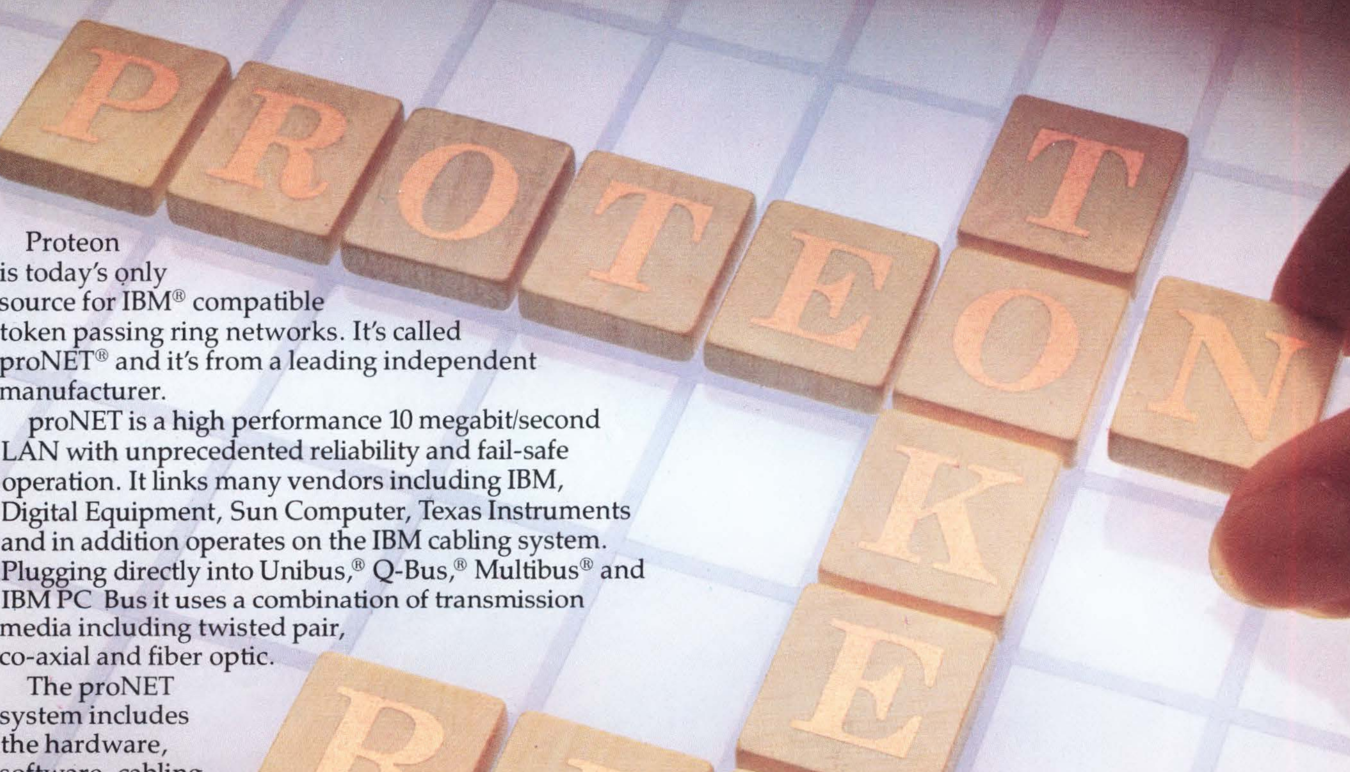


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# CAE workstation sets up direct connection to board design system

*Two workstations, sharing a data base, simulate the pc board as well as the circuitry it carries. Any change to one file updates the rest automatically.*

Computer-aided design and engineering tools have until recently been aimed primarily at the VLSI chip design process. For the board level of system design, however, simulation has not been considered a "must," because breadboarding is an economical method of debugging hardware design.

Nevertheless, a new CAE system makes it cost-effective for system designers to include pc board design in the simulation process. A full-function CAE workstation, the CDX-9200 develops and simulates a hierarchy of circuit schematics and semicustom IC designs. It then feeds that data to the CDX-5000 pc board CAD system, which in turn may send data back to it. Alternatively, all the software may be installed on a single workstation. Either way, simulation performed on an integrated electronic design system becomes a viable alternative to the time-consuming, manual procedure of breadboarding.

Closely coupling systems in this way eliminates the redundant manual entry that is required by present computerized tools. Design information is transferred automatically between schematic, simulator, and the pc board CAD system. Actual design is done interactively with a graphics editor and a mouse (see "Inside the CAE System," p. 170).

The CAE and CAD workstations use the same powerful relational data base for file management and storage. Such a data base makes fast work of manipulating large data structures. Moreover, the fact that logical and

**Stephen Gunther** and
**Victor E. Schoenberg**, Cadnetix Corp.

*Currently an applications engineer at Cadnetix in Boulder, Colo., Stephen Gunther formerly worked as a hardware designer at NCR Industrial Systems and as a designer of emulator and logic analyzer modules for field service testers at GenRad. He holds a BS in electrical engineering and in computer science from the University of Colorado.*

*Victor Schoenberg holds a BA in radio and television from San Diego State University and is now a senior technical writer at Cadnetix.*

physical data for both CAE and CAD applications is maintained in a common file structure means that the entire hierarchy of schematics is automatically updated any time a change is made at any one design level—that is, changes are transferred to levels preceding and following the current one. This forward and backward annotation, of course, improves the accuracy of schematics, pc board layouts, and production documentation.

The back-annotation capability allows every invocation of a component in a hierarchical design to be documented accurately. It enables, for example, pin- and gate-swapping changes occurring during board design to be automatically back-annotated to the schematic hierarchy. To do this, the system generates a unique back-annotation set, which lists reference designators and pin numbers for each invocation of a component in the schematic hierarchy. (A reference designator is a special identifier, one that is guaranteed to be unique

## Inside the CAE system

The CDX-9200 CAE workstation is a stand-alone system based on the 68010 processor, 1 Mbyte of main memory, a 35-Mbyte Winchester disk drive, and an 814-kbyte minifloppy, all in a single tabletop enclosure (see the figure). A 17-in. black and white CRT displays 1024 by 800 pixels. A color system is available with a 19-in. high-resolution monitor. A printer-plotter may be attached to the workstation, or an Ethernet hookup may acess a remote device, such as a pen plotter or dot-matrix printer, through a device and file server.

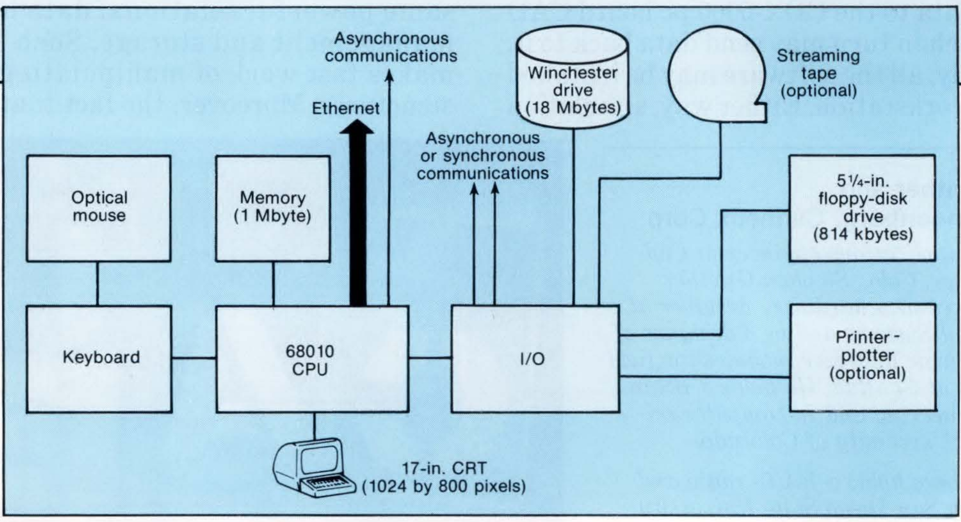
The Unix operating system serves as an alternative to the proprietary operating system, both of which have access to system hardware and design data bases. Based on the Berkeley 4.2 version, it has virtual memory and C and Pascal compilers.

A special subroutine library gives the user access to schematic data for postprocessing. As an alternative, users may generate an ASCII text file containing schematic net-list information.

The Ethernet package lets every workstation on the network share common files and output devices, such as plotters, printers, and tape drives. An output device connected to any workstation on the network can be driven by any other workstation, reducing the average peripheral cost per workstation by sharing devices among all users.

The file and peripheral servers use Winchester drives in 120- and 240-Mbyte versions. The file server acts as a common storage center for all systems on the network and can also service peripheral devices as shared resources. A magnetic tape drive holds archival data and acts as a backup.

The Ethernet option can transfer files to VAX computers running under VMS or Unix. In that way, an ASCII net list or a bill of materials can be transferred to the VAX for simulation, postprocessing, or materials management. Ethernet also gives users access to net list files, Gerber photoplot files, or simulation data.



within the hierarchy—for example, U31.)

Any back-annotation set generated for a particular invocation of a component is automatically displayed whenever that component's schematic is accessed by the user. A search function enables the user to locate a component by its reference designator. The user can modify that set at any point in the design process and be confident that the changes will be reflected in the pc board. When the schematic hierarchy is recompiled, the previously generated back-annotation sets are searched, so that real differences between the current schematic and the pc board can be distinguished. The fact that only the changes are actually recompiled speeds the process.

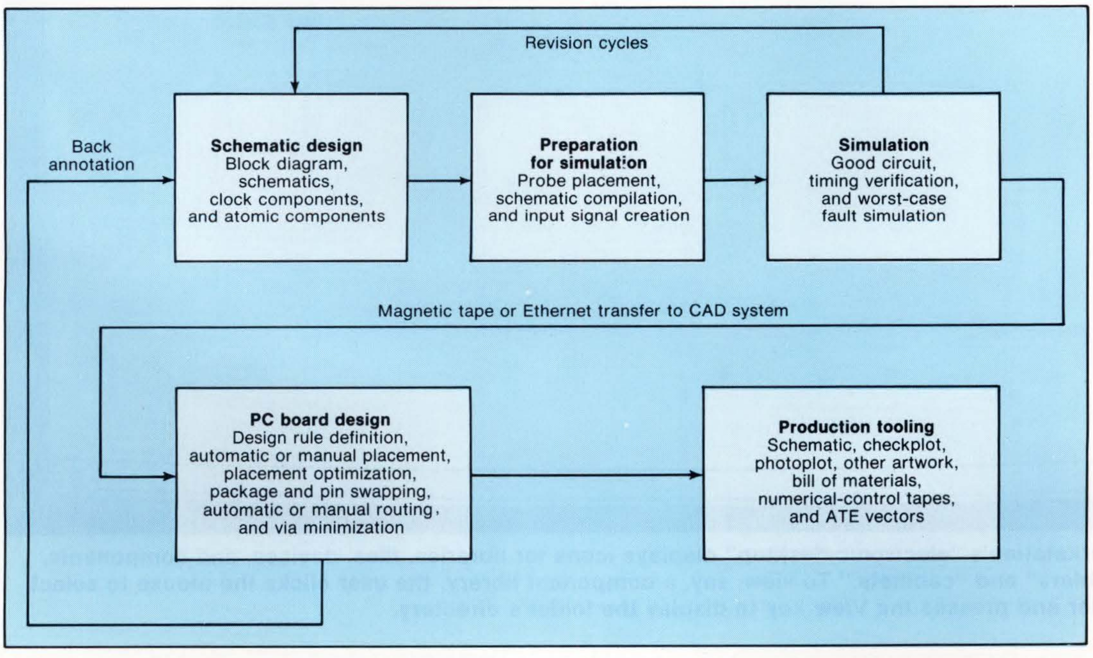
In the course of creating a schematic, the hierarchy of schematics below it can also be plotted. In addition, all possible back-annotation sets can be listed, permitting the user to select the one to be printed with the sheet. An option allows the user to plot the local signal names or to substitute names of the higher-level signals into which they are resolved. Also, the user can control the plotting of attribute strings associated with components and signals.

The process of design begins with schematic creation (Fig. 1). Any approach can be used—the design may be originated from the top down, the bottom up, or at any other point in the hierarchy. The system's comprehensive tools for graphically defining circuits apply to every level in the hierarchy, and the same user interface and editing techniques can create logic symbols, block components, schematics, and block diagrams.

**In the beginning**

The first screen displayed in a design session is the "electronic desktop," the work surface from which all operations are initiated and all resources are manipulated. Every file, library, device, and component is an object on the desktop, with a corresponding icon of intuitively obvious shape. Objects of the same type are generally kept together in file "folders" and "cabinets."

Most system functions are performed with one or two clicks of the mouse and by pressing a single key. For example, to view a component library, the user selects the file folder in which it resides, then presses the View key. This displays the directory for that folder (Fig. 2). The user can then select any object contained in it




**1. Two workstations sharing a relational data base incorporate the pc board design in the process of simulating an electronic circuit. The CDX-9000 CAE system handles the first three steps, producing input for the fourth step, performed by the CDX-5000 board CAD system.**

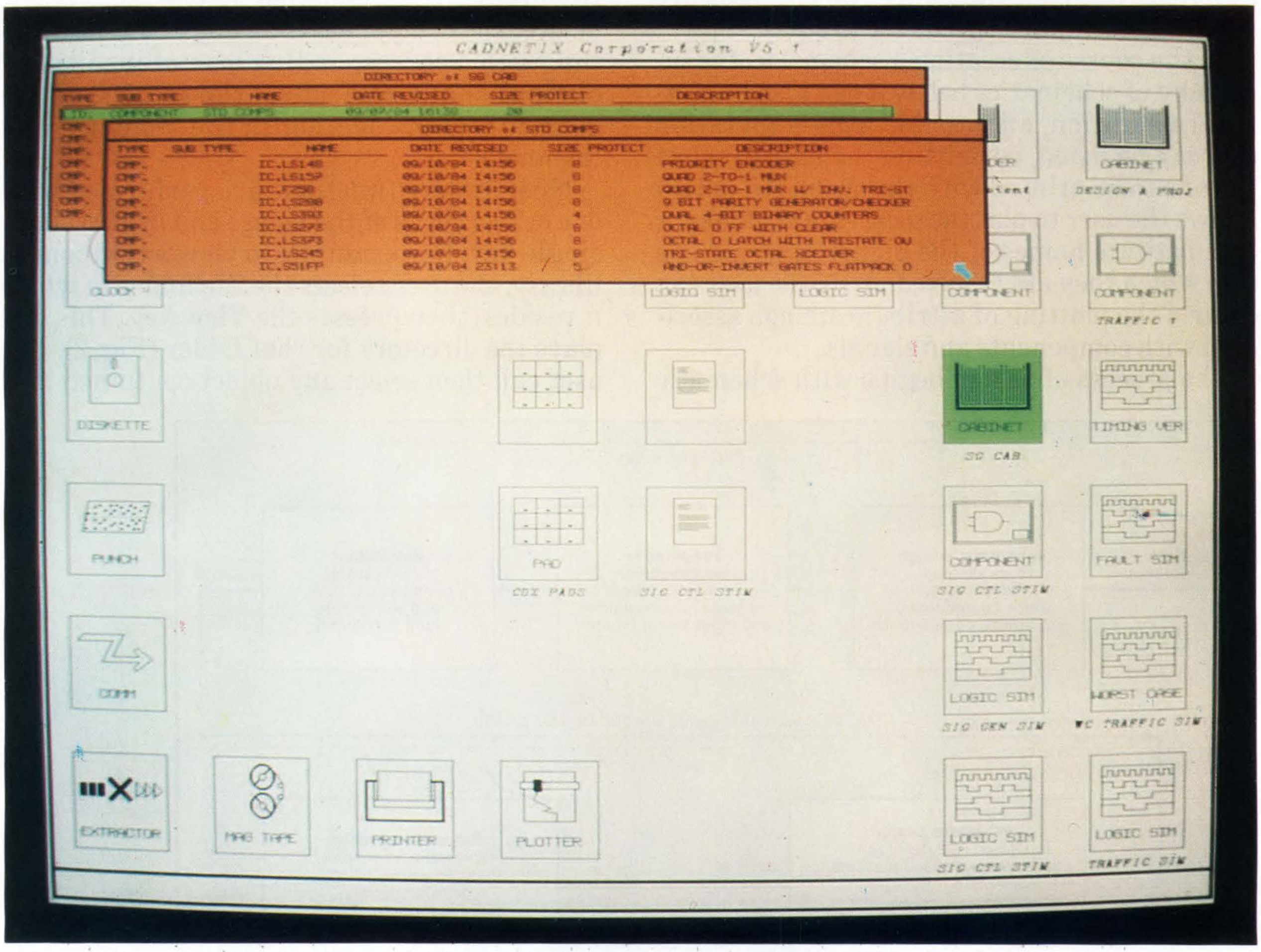
## CAE: Workstation duo

and, pressing View, open the file for editing.

The design of a simple traffic control system illustrates how the two workstations' CAE and CAD techniques mesh. A traffic control system has obvious analogies to industrial process-control systems but is simpler to describe. The designer begins with the top-level schematic—that is, a block design—of the basic modules, one each for controlling the light signal, the traffic signal, the main station, the crosswalk sensors, and the autoloop sensors (Fig. 3). These modules are created easily on the system by drawing lines with the mouse and typing text at the keyboard.

Each block is the symbol portion of a component object. A schematic exists for each of the five blocks in the top-level diagram. The designer traverses the hierarchy, to a lower level, by using the mouse to select the desired block symbol in the diagram, then pressing the View key. In this way, the schematic for controlling the traffic light is accessed (Fig. 4). Pressing the Close key returns the designer to the higher level.

Each component used in the schematic is first created in the symbol editor and stored in the component library. To create a logic symbol, such as a two-input NAND gate, the designer



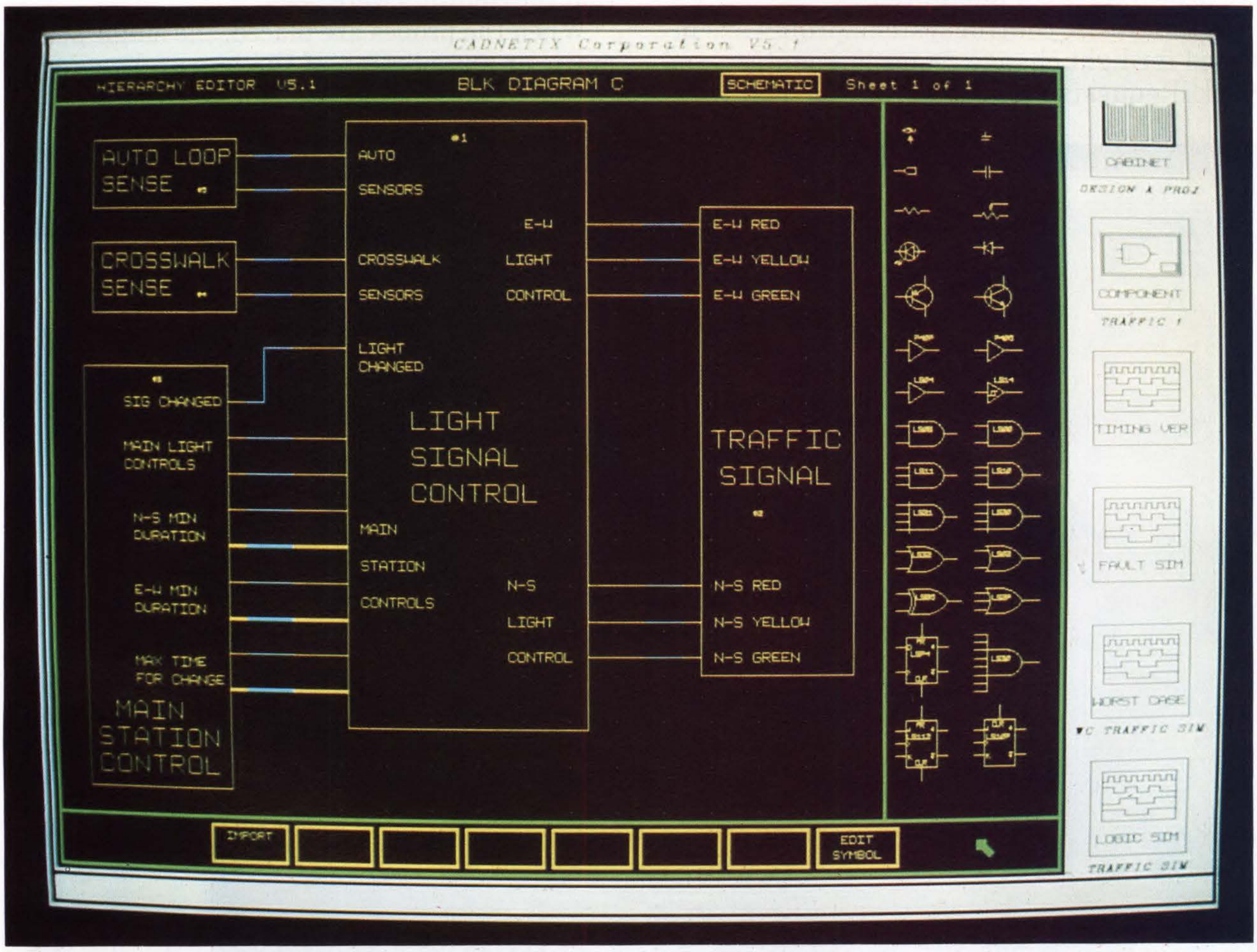

**2. The CAE workstation's "electronic desktop" displays icons for libraries, files, devices, and components, kept in file "folders" and "cabinets." To view, say, a component library, the user clicks the mouse to select the library folder and presses the View key to display the folder's directory.**

copies standard graphic elements (circles, arcs) and draws lines with the mouse. Then he calls up the component attributes form to enter the logical, physical, and cost attributes.

A graphics library contains user-defined board outlines, schematic sheet outlines, and other common elements. To draw the schematic, dedicated buttons on the mouse handle such jobs as moving components and creating signal connections. Action keys on the keyboard team up with the mouse functions to rotate components, automatically display alternative component representations, and search for and fetch components in the library.

Manipulation of components is quick and easy. For example, to search for a particular component, the designer places the cursor at the desired spot, then presses the Import key. A form appears that allows the designer to specify the component name. When Close is pressed, the workstation inserts the component in the schematic at the cursor location.

Components can be copied instantly from the Common Component Area on the right side of the screen, which contains representations of standard components. With the touch of a function key, components and their connections can be repeated automatically. As components are




3. A block diagram is the starting point of a CAE design. The user simply draws lines with a mouse and enters text through the keyboard to create the five modules of this traffic control system.

positioned and signals drawn, signal attributes can be set or modified by calling up the attribute form and entering values. No restrictions are placed on typing notational text. Here again complete backward and forward annotation ensures that all designs incorporate the most current version of components.

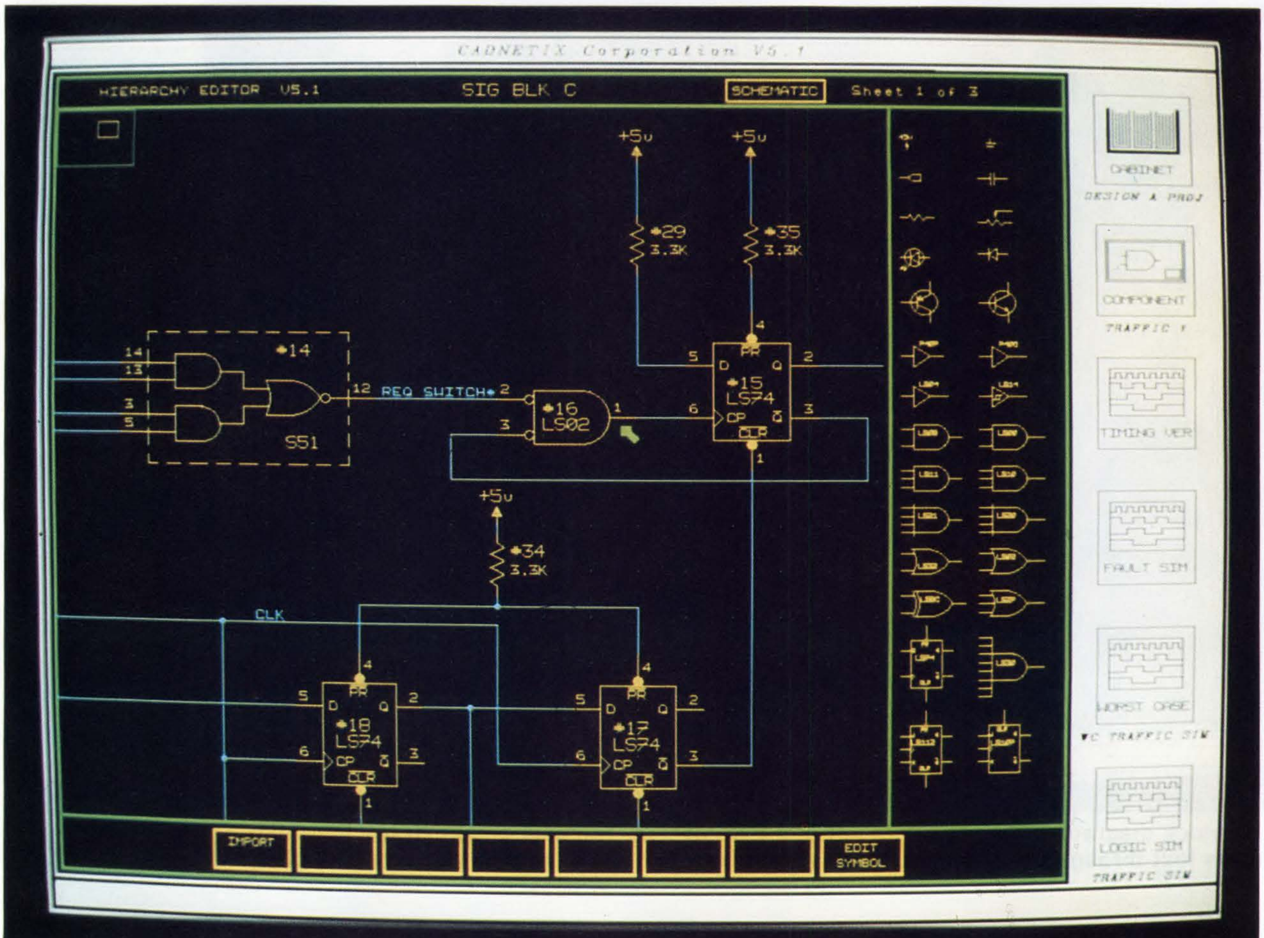
### Preparing for simulation

Schematics can be simulated either separately or with others. Starting with the light control module, the designer first inserts probes—through the same graphics editing steps that bring parts to the schematic—where signals are to be injected or monitored.

In the traffic control system, probes are inserted for light change requests, counters, and clock. Requests originate from the main station, the automatic loop sensors (placed in the pavement), and the crosswalk sensors (button-controlled). These requests are monitored in two directions, north-south and east-west. In addition, input probes are installed for counters that monitor the duration of yellow lights and for the clock.

Output probes are placed at signal-monitoring points (Fig. 5). In the example, probes check that the light change requests were generated, that requests to switch the light were generated, that the switching actually occurred, that all lights in both directions were the proper color at the appropriate times, and that the counters were reset.

When the probes are placed, the single schematic or any portion of the hierarchy can be compiled for simulation. This is a simple two-




**4. Before creating the schematic of the light signal control block of the traffic control system, the designer employs the symbol editor and the mouse to create each component and then accesses the attributes form to enter the component's logical, physical, and cost attributes.**

step operation on the desktop, in which a schematic object is associated with the simulation object. The mouse selects first the schematic object and then the signal object.

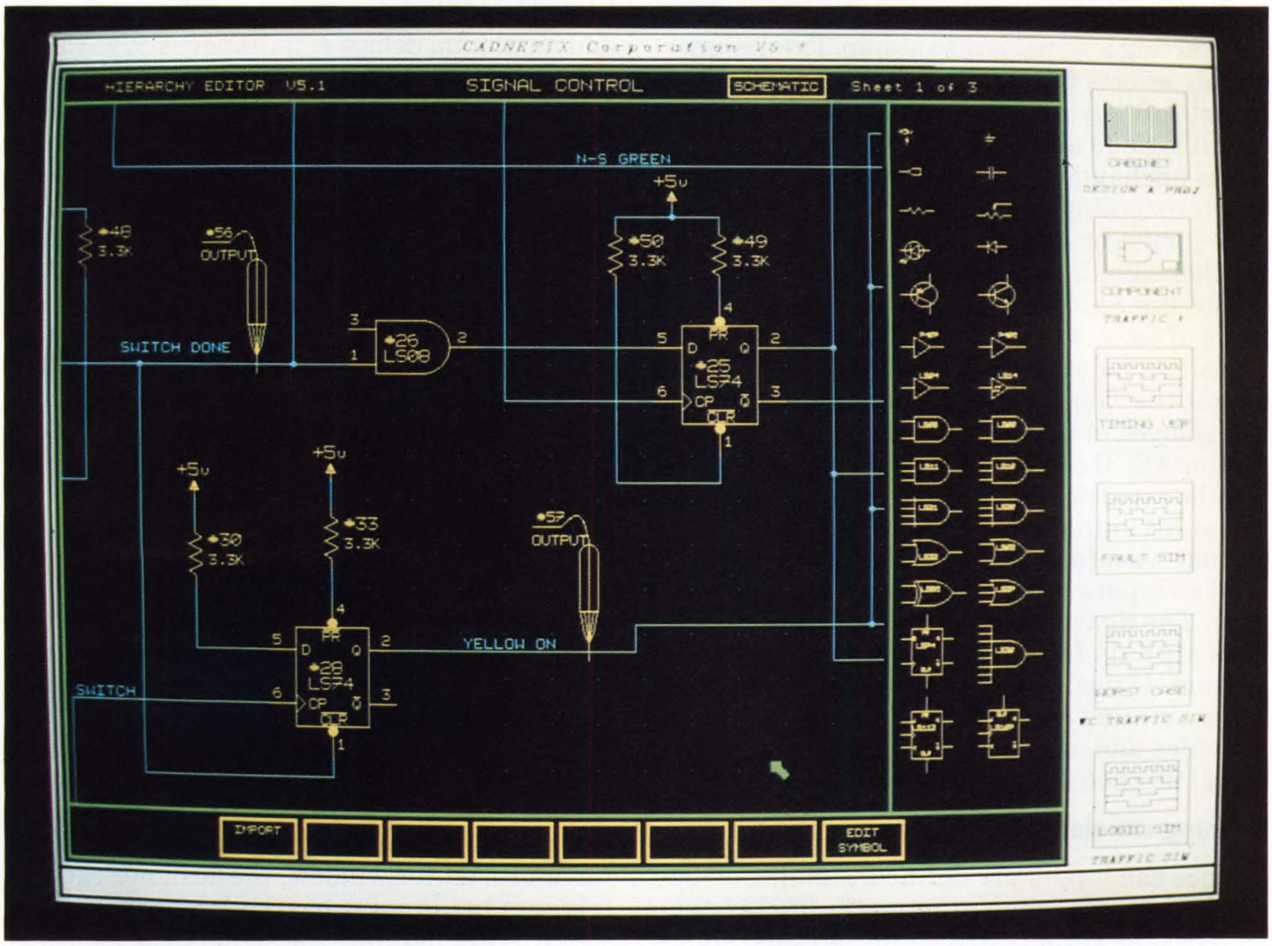
Schematic compilation may generate warnings or messages indicating errors. Once the errors are corrected, the user can view the signal object and begin defining the unique input signals required for the simulation run.

**Easy editing**

Viewing the signal object opens a window into the graphic waveform editor. Along the left side appear the names of I/O signals to which probes are attached in the schematic. The waveform display can be adjusted so that the schematic can be accessed concurrently in a second editing window. Simply positioning the cursor with the mouse makes it possible to edit in each window. As many as 20 signals show up in the window at once, while more than 2000 may be scrolled into view.

The mouse and soft keys greatly simplify the chore of defining input signals. Input signal names are underlined on the left side of the signal editor window; at the beginning of that area is a signal stub, which the user can grab with the mouse and extend to the right. Wherever a transition to a new signal state is desired, the user presses the soft key corresponding to the desired state—0, 1, X (unknown), or Z (high impedance). The states can be assigned different colors to make them easy to distinguish.

Various editing functions may be invoked to change signal definitions. For example, the designer may move a signal edge to the right,




**5. The first step in simulating a schematic is to put probes into those circuit locations at which signals are to be injected or monitored. The probe symbols are created by the usual graphics editing techniques. Here they monitor such events as the generation of requests to switch a traffic light.**

overwriting any transitions that are present. If the edge is moved back to the left, the overwritten transitions reappear. Another operation, dubbed extending, is a different setup in which the transitions to the right of the cursor advance ahead of it, while new edges can be inserted at the cursor location as it moves.

### Quick changes

Other editing functions operate on entire pulses. Pulses and sequences of pulses may be moved, repeated, inverted, copied, or deleted. The repeat function creates periodic pulses. For example, to create the clock, a 50-ns pulse sequence is drawn and selected with the mouse, then the Repeat soft key is pressed, causing a window to appear into which the designer enters the number of repetitions. In this way, arbitrarily long periodic sequences can be created by drawing just one cycle.

Inverting a signal is also a snap. The designer merely selects the signal name and presses the Invert soft key; the system substitutes logic 0s for all logic 1s and vice versa, leaving unknown levels unchanged. Other editing functions can clear everything to the right of the currently selected pulse or append one signal to the end of another signal.

The simulator also displays signal buses as pairs of lines, with vertical bars marking the transition points (edges). Between each pair of points, the value on the bus during that interval is displayed in binary, octal, decimal, hexadecimal, or ASCII code. At the user's option, the bus may be expanded into individual signal lines.

Not all signals need be created manually. Output waveforms can be edited and, in turn, used as inputs to any portion of the circuit design. The Search key enables the designer to find signals from any signal object in the system. If desired, text entry and command programming can be eliminated. The system provides added flexibility by allowing traditional methods of signal specification as well.

### Running simulation

Once the inputs are defined, simulation begins. Functional simulation on the 9200 system employs the kernel software of the Cadat simulator, originated by HHB-Softcon Inc. Cadat is fully integrated into the object-oriented user interface yielding the benefit of reduced training time. Yet the software uses the same primitives, and the process of modeling circuits is essentially the same. Circuit modeling draws on a library of more than 90 logic primitives, including 16 transistor models, ROMs, RAMs, ALUs, counters, and multiplexers, as well as standard gates and flip-flops.

The Cadat simulator works with 12 states, combining the three logic levels (low, high, and unknown) with four signal strengths (active, passive, floating, and indeterminate). Thus, it can accommodate complex VLSI chips and large transistor networks, as well as circuit board designs.

Functional simulation verifies the logical correctness of the circuit with typical rise and fall delays. In worst-case analysis, the devices are simulated with ranges of rise and fall delays. The signals propagate under minimum and maximum delays simultaneously, with the signal value during the interval of ambiguity considered unknown. Thus the simulator can determine how various devices would behave under worst-case specifications. (Timing verification will be available shortly, a type of simulation that resembles worst-case analysis, except that input signals may be specified as stable or changing rather than as exact values, so that the circuit may be tested for whole classes of input vectors.) The separate Cadat fault simulator is an optional software item for the CAE workstation. It grades a set of input test vectors for use with automatic test equipment.

### Viewing the output

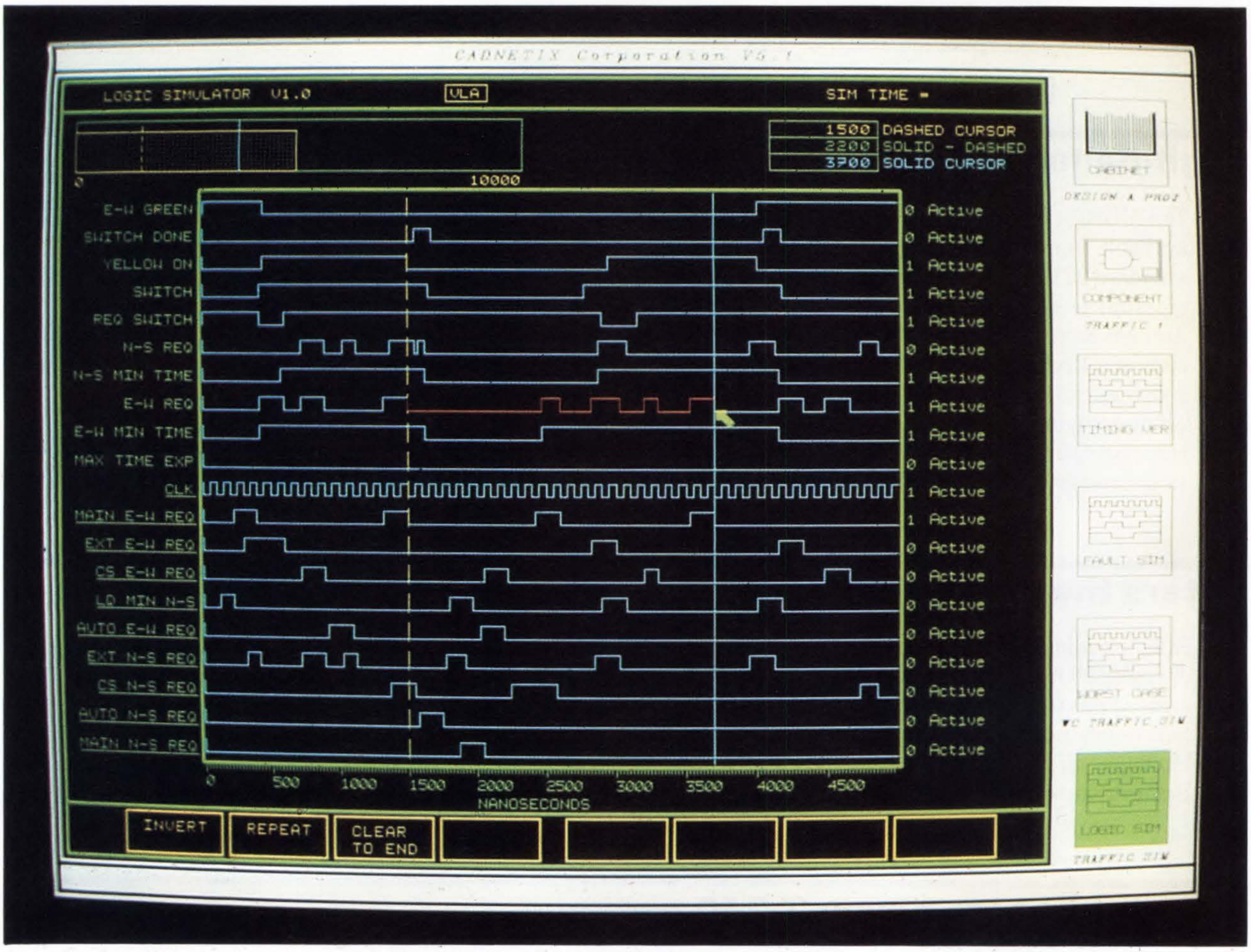
Following simulation, the output signals appear in the display's logic analyzer window, along with the previously defined input signals (Fig. 6). The simulator records as many signals as the user chooses—all signals in the schematic, all top-level signals, or only those to which output probes were attached in the schematic.

The postsimulation display incorporates the same user interface that creates input signals. In addition to zooming and panning within the waveform editor window, the designer can use triggers to pinpoint particular portions of a signal. After defining the signals, the logic levels, and the search time interval, the designer presses the Trigger key to initiate a search of

the signal store for the desired condition. If it is found, the system displays it in the window.

The system produces various reports in response to user requests, storing each report as a separate document accessible through the Reports soft key. The attributes feature is used to set report parameters. The reports cover:

- Minimum pulse width: The system checks for a minimum width (which the user defines) of pulses on selected signals, at the level and strength the user specifies. The report lists the signals and times when pulses too short in duration were detected.
- Setup and hold: The system checks the setup and hold characteristics of selected signals with respect to a reference signal. Signals that do not meet the specification are reported.
- Signal activity: Selected signal transitions are checked within the given time range, with the report indicating how many times each signal entered each possible state.
- Spikes: The system logs a spike whenever the simulator attempts to schedule two events within the propagation delay of a device.
- Bus contention: The system reports this if two devices attempt to drive one line with the same strength but different levels.
- Unknown signals: The system lists signals




**6. After simulation, the logic analyzer window displays both the previously defined input signals and the output signals of the simulated circuit wherever probed.**

with an unknown level or indeterminate strength at the end of simulation, which may indicate initialization problems or ambiguous circuit behavior.

- Pending events: Signals that have a change of state scheduled to follow the end of simulation are documented, to indicate possible circuit instabilities.

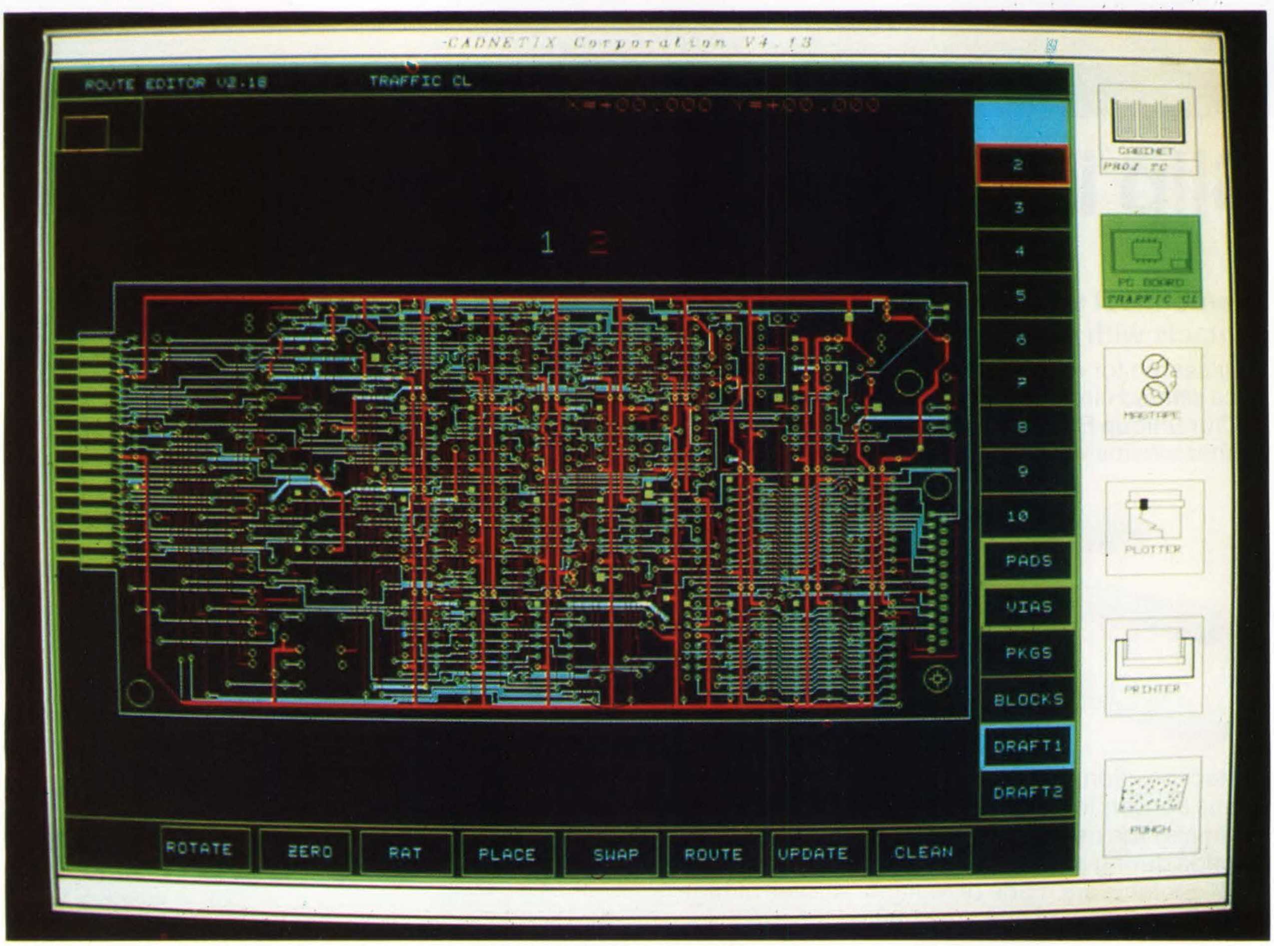
### From schematic to pc board

Either an Ethernet link or a magnetic tape can transmit finished designs to the CDX-5000 workstation. That comprehensive pc board design system incorporates automatic placement, placement optimization, routing, and via minimization (Fig. 7). Its editor lets the user control the layout process interactively. The user can specify the dimensions of the component and routing snap grids (down to 1-mil resolution), minimum trace clearance, routing trace width, and via shapes.

Up to 24 trace levels are at hand, along with a dozen drafting layers, six for generating artwork and six for defining pads, vias, packages, and blocks. The system also supports surface-mounted devices like chip carriers, small-outline ICs, and flat packs.

Generating a tape of the production tooling details of the board mask completes the process. Using the nine-track magnetic tape, the photoplotting supplier creates the artwork, and the design is ready for pc board fabrication.□

| **How useful?** | **Circle** |
|---|---|
| Immediate design application | 544 |
| Within the next year | 545 |
| Not applicable | 546 |




**7. An automatic feature optimizes the designer's original placement of components on the board. The automatic routing, followed by via minimization, results in a fully routed board.**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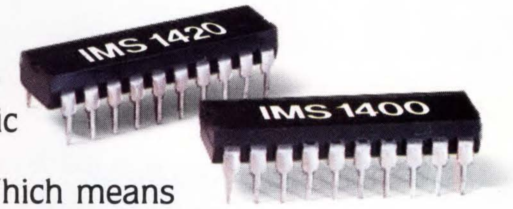


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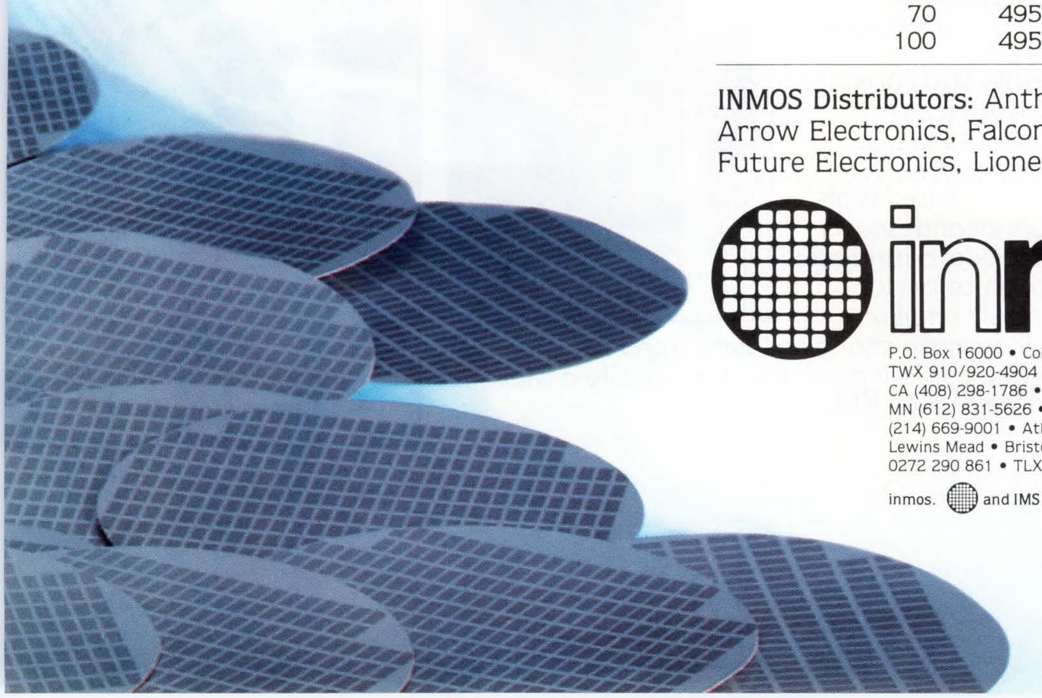

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|---|---|---|---|---|
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| | 45 | 660 | 110 | IMS1400-45 |
| | 55 | 660 | 110 | IMS1400-55 |
| | 70 | 495 | 83 | IMS1400-70L |
| | 100 | 495 | 83 | IMS1400-10L |
| 4Kx4 | 45 | 605 | 165 | IMS1420-45 |
| | 55 | 605 | 165 | IMS1420-55 |
| | 70 | 495 | 83 | IMS1420-70L |
| | 100 | 495 | 83 | IMS1420-10L |

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CIRCLE 94

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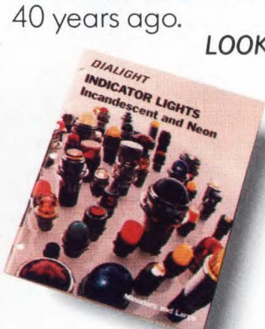


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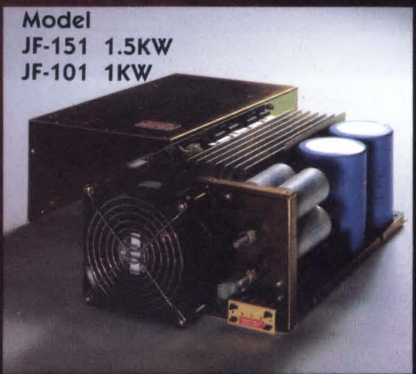
CIRCLE 95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CIRCLE 96

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# Silicon compiler demands no hardware expertise to fashion custom chips

*A functional language makes fast work of describing a custom processor. The compiler converts the description to an IC, and simulates its performance.*

Instant expertise in VLSI chip fabrication is the promise of all silicon compilers. Since they automate most time-consuming and difficult steps of IC development, they are beginning to make custom VLSI and other application-specific ICs a feasible option for the system engineer.

But the level of input that each silicon compiler accepts varies widely. One type generates masks from logic schematics produced on a workstation. Another is satisfied with input at the architectural, or block-diagram, level. A third kind—exemplified by MetaSyn—works directly from a functional description of the chip and hence requires absolutely no hardware experience (Fig. 1).

Anyone with moderate programming ability can use this compiler. As the product evolves, even someone not involved in the original design can easily modify that source specification to include enhancements. Moreover, the compiler contains a high-level simulator that lets the designer observe the device's internal operation and its interaction with a simulated environment.

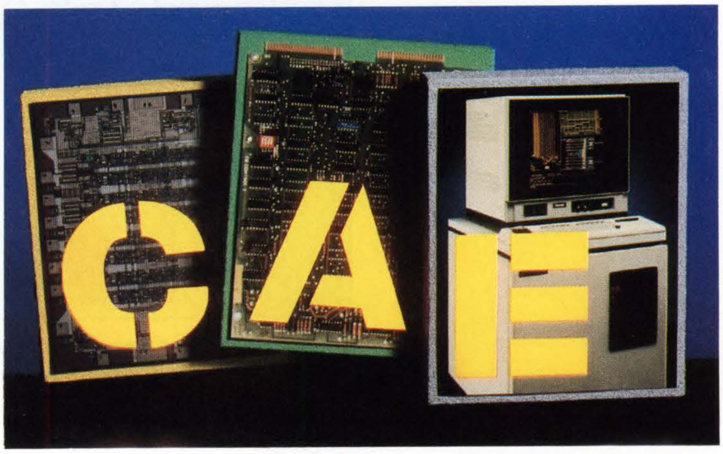
**Jay R. Southard**, MetaLogic Corp.

*Jay R. Southard is vice president and director of technical marketing at Metalogic in Cambridge, Mass. After receiving an MSEE from Stanford University, he worked as a systems designer for General Instrument and Charles Stark Draper Laboratories. Most recently he was a researcher at MIT's Lincoln Laboratory, where he was active in the conception and implementation of the MacPitts language and compiler, which became the basis for MetaSyn.*

The compiler is based on the MacPitts silicon compiler, developed at the Lincoln Laboratory of the Massachusetts Institute of Technology. It permits the description of systems in algorithmic terms rather than in the structural terms of the hardware engineer. To clarify the difference between the alternatives, consider the following algorithmic fragment:

$$a := a + b - c$$
$$r := r - a + d$$

In other words, first replace the value of a with



the result of a+b−c, and then replace the value of r with r − a + d. This function can have many possible structural representations (Fig. 2).

### Problem-oriented

The algorithmic approach is inherently less expensive to use than structural approaches. Thus it appeals to system designers who want to solve a system problem rather than create specific hardware; but it can upset hardware designers, because it does not permit them to specify and manipulate familiar hardware structures.

Theoretically the compiler cannot offer as great a variety of implementations as a hardware designer can. Practically, it solves nearly as many application problems, and of course, it does so in much less time and makes much more efficient use of silicon than do gate arrays and standard cells.

Although the MetaSyn specification for a chip is similar to a microprocessor program—especially for a bit-slice machine—it differs in several ways. Like a bit-slice microcode program, MetaSyn code may specify that several operations are to take place in the same clock cycle. The resulting parallelism clearly improves the algorithm's speed. Unlike microcode, however, a MetaSyn specification is not limited by some fixed, available hardware parallelism. Instead, the compiler automatically creates exactly the amount and kind of parallelism necessary to implement the designer's specification. This method also allows the algorithmic specification of such implementation techniques as pipelining.

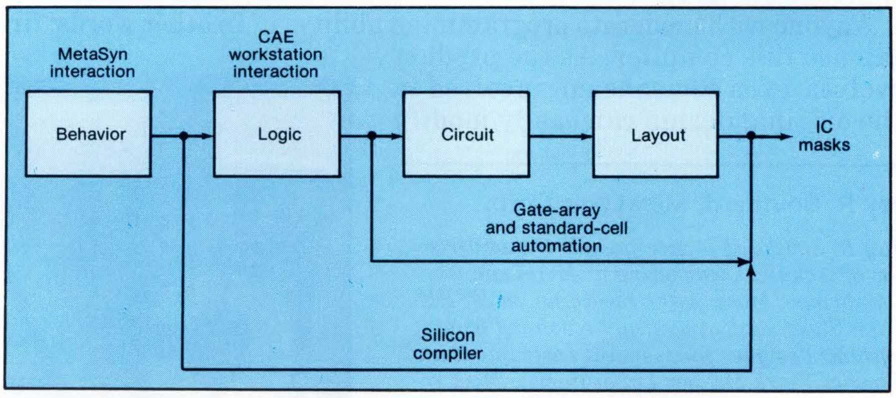
The new compiler goes a step beyond the way in which application programs are usually optimized. If a function's speed of execution is critical, it is usually coded in machine language. If it is even more critical and the computer has a writable control store, the function may be converted into microcode.The compiler goes beyond microcode. The application's critical algorithms need only be added to the processor's MetaSyn specification. The compiler then generates hardware that not only implements the old computer, but also the critical functions at a higher level of parallelism than available with microcode.

### Two kinds of simulation

Before synthesizing the IC layout, the new compiler's high-level simulator mimics the device's behavioral specification. For this purpose, the compiler uses two kinds of simulation: interactive input with execution monitoring and system-level simulation.

The user interface of the compiler's simulator consists of a set of windows that monitor the high-level elements of the design: registers, processes, labeled instruction states, I/O ports, and other elements. Because these are also the elements of the compiler's behavioral specification, it is a simple matter for the designer to observe these elements and to use a mouse to modify their values (Fig. 3).

For simulation of a chip design—say, a pro-

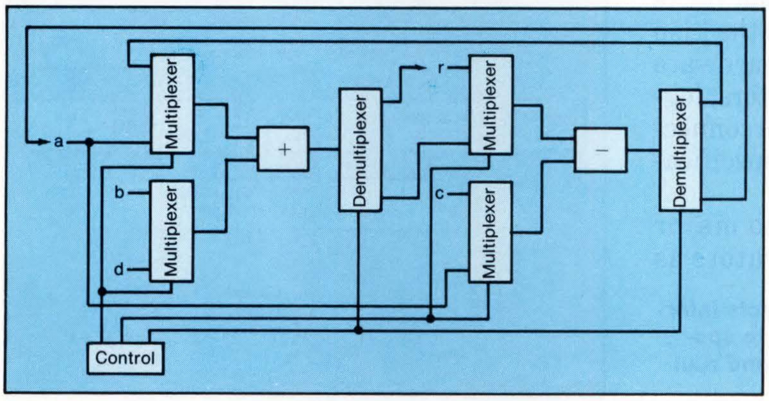



**1. The MetaSyn silicon compiler starts chip design a stage earlier than other CAE software. It translates algorithmic descriptions of circuit behavior—not block diagrams—into logic hardware and ultimately into masks for fabricating ICs.**

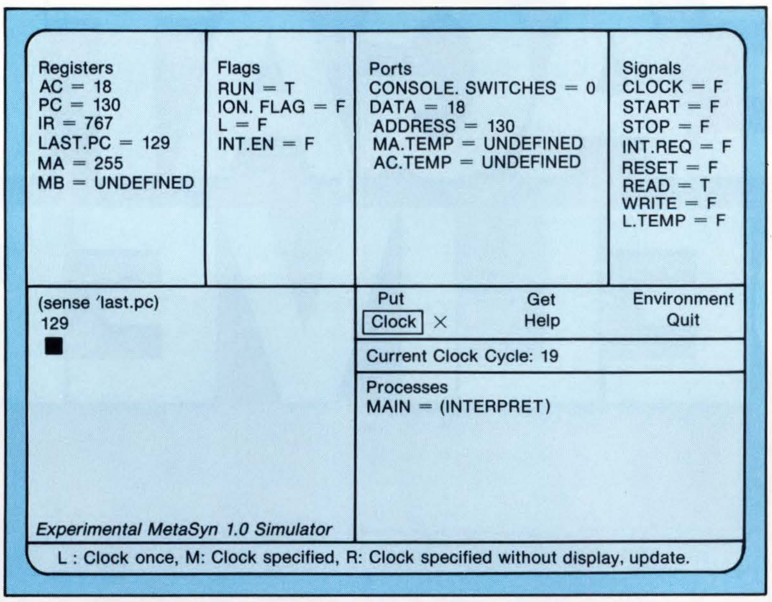
cessor—in the context of a complete system, the simulator creates several Lisp functions that can be used by other simulated system components to drive and sense the processor's ports and signals. This environment simulation thus deals with the same elements as the interactive simulator and the initial specification.

For example, the simulated processor can be connected to a simulated environment consisting largely of a memory that can contain a program for the simulated chip. The compiler simulates the processor and its environment concurrently, and the results can be monitored on the windows. Meanwhile interactive operation is simultaneously possible.

System-level simulation is also useful for control, signal-processing, and general system applications. In addition, the environment can




**2. This circuit stores five values (a, b, c, d, and r) in master-slave registers and then funnels them through the adder-subtractors selected by multiplexers under the direction of the control box. It is not immediately obvious, however, that this layout is one of the many structural equivalents of the algorithm** a:= a + b − c **and** r := r − a + d.




**3. During simulation the register contents, flags, ports, and other internal functions of the designed chip can be followed on the screen. The effects of changes to the description are displayed within a few minutes at most.**

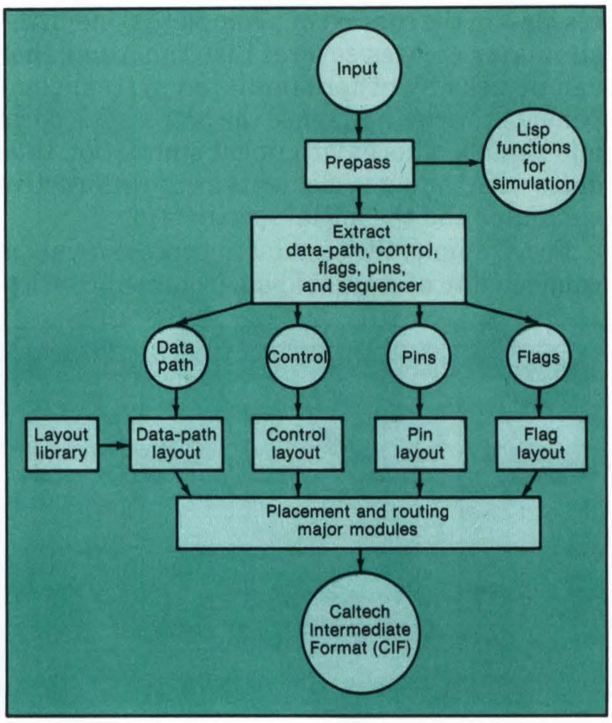
## CAE: Behavioral silicon compiler

produce a set of test vectors that mimic the environment, as well as the simulated chip, so that the chip, when fabricated, can be tested with standard automatic equipment.

### Inside the compiler

A silicon compiler is a complex piece of software (Fig. 4). The input "source" description goes first through a prepass stage that checks for syntax errors, expands macros, and if the simulation option is in force, produces the Lisp functions for the simulator. Then the hardware components—registers, integer operators, logic gates, flags or pads—and their interconnections are "extracted" from the source specification.

The components are grouped into major modules: registers and integer operators as




**4. From the user's input, the compiler extracts information related first to simulation and then to specific processor functions. After placement and routing, it produces a CIF tape.**

part of the data-path module, logic gates as part of the control module, and so forth. Next each group of components is laid out with data-path, control, flag, and pad module generators. Since most of the interconnections are between the components of a module—between the registers and the operators of the data path, for example—much of the routing has now been done. Finally, the major modules are placed and routed to create the final layout in CIF (Caltech Intermediate Format).

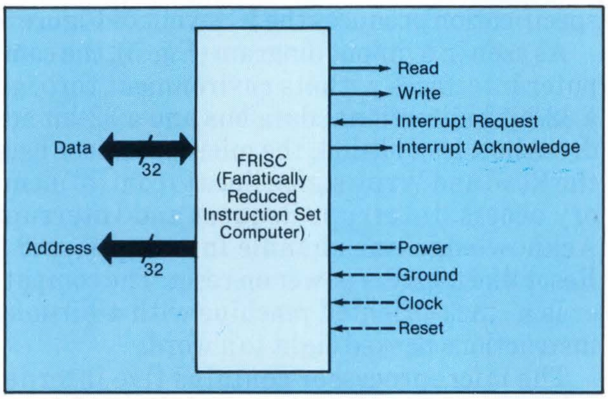
**Proof of the pudding**

Over the past few years more than 50 MacPitts and MetaSyn examples have been generated, ranging from simple counters and shifters to signal-processing chips, computer peripheral controllers, and such microprocessors as an 8080 and a PDP-8. Even a neural network simulator has been built from MacPitts-generated chips. For simplicity, consider a stripped-down, 32-bit microprocessor called FRISC (Fanatically Reduced Instruction Set Computer) as an example.

The FRISC processor is based on a flexible and simple instruction set. It is specified in little more than three pages of text. However, as will be shown, the basic FRISC processor can be easily tailored to special-purpose applications and algorithms. When compiled, the FRISC specification produces the IC layout of Figure 5.

As seen in a pinout diagram (Fig. 5), the computer interfaces with its environment through a 32-bit bidirectional data bus and a 32-bit address bus. In addition, the microprocessor uses the Read and Write signal lines to control memory access. Interrupt Request and Interrupt Acknowledge lines handle interrupts, and a Reset line triggers power on reset. The computer is a stack-oriented machine with 4-bit-long instructions packed eight to a word.

The microprocessor contains five internal registers, although, as in any stack machine, a FRISC programmer will not be able to access them directly. Specifically p is a program counter; s, a stack pointer; a, the top-of-stack cache; b, the next-on-stack cache; and i, an instruction register. The core processor implements a few simple instructions (see the table, opposite). Because of the flexibility of the compiler, it is easy to expand, reduce, or modify this minimal set of instructions.




**5. The 32-bit FRISC chip that MetaSyn will compile has two buses and eight other pins.**

To implement FRISC, a straightforward microcodelike sequence will be used. The code will be broken up into reset, instruction-fetch, instruction-decode, and instruction-execution sections.

### Back to state one

A MetaSyn machine with more than one instruction state must have a reset input signal that always returns the machine to its first instruction state. Thus Power On Reset (PRST) is the first state; it can be used to initialize the program counter (register p) with the data in memory location 0 and to initialize the stack pointer (register s) with the data in memory location 1. The state is defined as:

```
PRST
(par (setq address 0)(setq read t)(setq p data))
(par (setq address 1)(setq read t)(setq s data))
```

This code fragment specifies two clock cycles.

In the first cycle, the address port output is set to 0, the read signal is asserted (set to true), and the p register is set from the data port. In the second instruction cycle, the value in memory location 1 is accessed and read into register s.

The MetaSyn par instruction specifies that all three setq clauses operate in parallel in the same clock cycle.

The following code segment checks for an interrupt request, and if none is pending, loads

**FRISC instruction decoding**

| Instruction word* | Operation | Comment |
|---|---|---|
| 0000000000000000 | NOP | Instruction fetch |
| XXXXXXXXXXXX0001 | ADD | Add top-of-stack elements |
| XXXXXXXXXXXX0010 | INC | increment top-of-stack |
| XXXXXXXXXXXX0011 | PDSI | Push immediate data on stack |
| XXXXXXXXXXXX0100 | LTM | Load from memory onto stack |
| XXXXXXXXXXXX0101 | STM | Store into memory from stack |
| XXXXXXXXXXXX0110 | SUB | Subtract top-of-stack elements |
| XXXXXXXXXXXX0111 | SHFT | Shift top-of-stack right one bit |
| XXXXXXXXXXXX1000 | IF | Conditional jump |
| XXXXXXXXXXXX1001 | GO | Unconditional jump |
| XXXXXXXXXXXX1010 | CALL | Subroutine call |
| XXXXXXXXXXXX1011 | RET | Return from subroutine |

* X = don't care
Bits 0 to 15 are not shown; their value equals that of bits 16 to 27

instruction register i, with the data in the memory location addressed by register p:

```
instruction-fetch
(cond  (interrupt-request   (go interrupt))
       (t                   (setq address p)
                            (setq read t)
                            (setq i data)
                            (setq p (1+ p))))
```

In MetaSyn parlance, cond resembles a case statement. Each branch of cond is a subexpression, guarded by the first expression within each of the example's two branches. The remaining expressions within the branch are executed in parallel, but only if the guard is true and previous guards are false. Therefore, the first instruction state of instruction-fetch, cond checks the Interrupt Request signal and, if it is true, aborts the instruction fetch and goes to the MetaSyn instruction state labeled interrupt. In MetaSyn, (go . . .) causes an unconditional transfer of control within the MetaSyn specification. But if no interrupt is pending, instruction register i is read in from the memory location pointed to by the program counter, register p. In a single clock cycle, the address port is set to p, the read control signal is asserted, and the i register is set from the data port.

In addition, this instruction state also contains the clause (setq p (1+ p)), which uses the built-in MetaSyn operator 1+ to increment the program counter. Because p is a register, it can be used as the source for address during the current instruction state (as required by the memory access) and still be incremented in parallel, because it will not change its value until the end of the current clock cycle. The compiler can be counted on to produce enough buses so that p can be routed to both the increment operator and the address port in parallel.

### Case of the zero register

Now that an instruction resides in the i register, its four least significant bits must be decoded to pass control to the appropriate in-



struction execution subroutine (see the table, p. 193).

As the instruction in the four low-order bits is executed, it is shifted out of the i register. When that register equals zero, the current instruction word is exhausted, and a new one must be fetched. Thus the instruction-decode state must also check for the special case of the all-zero i register.

The instruction decode begins:

```
instruction-decode

(par (setq i (>>i 4 0))
     (cond ((=0 i) (go instruction-fetch))
           ((eq? i 1 (3 2 1 0 )) (call ADD))
           ((eq? i 2 (3 2 1 0 )) (call INC)
```

Naturally there are more instructions, but these suffice to demonstrate the basic implementation. The code first shifts the i register, so that at the beginning of the next instruction state the register's content will be replaced by the same word, shifted to the right by four places and filled from the left with zeros. (The right-most position of these zeros is the least significant bit.)

While shifting the i register for the next clock cycle, FRISC simultaneously executes the condition or cond statement that will actually decode the current instruction. Each of the guards within cond conducts a check for a different op code, but the op codes are all checked simultaneously.

The first guard specified is for the all-zero instruction. The clause (=0 i) uses the built-in =0 function, which then tests its integer argument (in this case, i). A Boolean value of true is returned if the integer equals zero; any other integer yields a false. If the value is true, the matching go expression is executed.

If i is not zero, the next guard tests the four low-order instruction bits, as specified by:

```
(eq? i 1 (3 2 1 0))
```

Again, eq? is a built-in function that takes a field of bits out of an integer (in this case, i) and compares the bits to another integer. A value of true results if the bits are equal and false if they are not. Thus this branch is executed only if the lowest four bits of i are equal to 1 (the op code for a FRISC ADD instruction).

If the branch is executed, control is transferred on the next clock cycle to the MetaSyn instruction state labeled ADD . Since this transfer comes about by means of a MetaSyn call instruction, the code at label ADD should end with a MetaSyn return instruction, in order to pass control to instruction-decode + 1 (the next state after instruction-decode).

If the low-order four bits are not 0001 but 0010, then the current FRISC instruction is INC, and control is dispatched to that instruction state, and so on.

#### Ready for execution

It is important to realize that the compiler automatically generates the hardware to implement the specified parallelism; no further guidance from the designer is needed.

To see how FRISC executes an instruction, consider how, for example, increment is coded:

```
INC
(par  (setq a (1+ a))
      (return))
```

The functions par and 1+ are already familiar. In this case, the latter is called upon to operate on the top-of-stack cache, a. Incidentally, this top-of-stack increment and the program counter increment can physically share the same hardware, since the two increments occur during different instruction states—but the compiler will worry about all that. Simultaneously with the top-of-stack increment, control returns to the instruction-decode + 1 state via the return operation.

Once the specification for the computer has been completed, the designer should simulate it interactively by setting and observing the processor's I/O pins, or by running a FRISC pro-



gram in a simulated memory. The test program to be used sums the elements of a vector containing the first six even integers.

### In the chips

All told, the FRISC project took less than a week, including the specification of about three pages of MetaSyn code and two pages for the system simulation program. But the manufacturability and size of the FRISC chip is also vital. Of course, chip size is very dependent on the fabrication technology. A safe, inexpensive, and conservative technology would be a 4-$\mu$m single-level metal NMOS process. In this case, the 10,000-transistor, 32-bit FRISC chip turns out to be 7.7 by 9.3 mm. By going to a 3-$\mu$m, single-level metal process, the size gets closer to 7 by 6 mm—easily producible. The compiler also supplies statistics and estimated power consumption.

The chip's density, as measured in transistors per square millimeter, may appear low, but that parameter is nearly irrelevant. Far more important is functional density. For example, ROM, PLAs, and random logic are, for many purposes, logically interchangeable. The ROM implementation has the best transistor density, while random logic provides the same function with the fewest transistors. Very likely (depending on the function implemented), the PLA will emerge with the best functionality per square millimeter. Similarly, FRISC—or any other design—should be measured by functional density.

### Build a better chip

One interesting aspect of a compiled chip like FRISC is the ease with which it can be converted into a 16-bit processor (or any multiple of 4 bits) by a change in just one number in the specification. For the 16-bit computer in the 4-$\mu$m single-level metal NMOS process, the size is 6.9 by 6.0 mm (Fig. 6).

Now that a FRISC prototype exists, it is time to think about improvements. For example, it might be good to overlap the processes for fetching, decoding, and executing instructions, thus implementing a form of pipelining. Alternatively, an application might suggest an addition to the FRISC instruction set. Designers often do this in microcoded processors by adding the new instruction to the microcode; however, the new instruction can use only the existing hardware resources. But when a new instruction is coded in MetaSyn, it may result in new, more suitable hardware for the new instruction. For example, an instruction to sum the elements in a vector could be included. Such an instruction might be called vector-sum . It takes as the vector's base address the data in the top-of-stack element. The next element will contain the length of the vector.

When vector-sum is completed, these two values are popped off the stack, and the sum is pushed on top of the stack. During execution of vector-sum, the a register serves as the current address in the vector, and b holds the vector's remaining count. No register is needed to hold each element as it comes in from memory, since FRISC can be made to add directly from the data port. To keep the running sum, however, a new register, called vs (for vector sum), becomes necessary.

#### Just add nine lines

To implement the vector-sum instruction, FRISC's instruction-decode section must be modified and new code added to the instruction-execution section. One way to implement the latter is:

```
vector-sum
   (cond (( = 0 b) (setq b vs)
                   (go pop))
         (t (setq b (1-b))
            (setq address a)
            (setq read t)
            (setq vs (+ vs data))
            (setq a (1+ a))
            (go vector-sum)))
```

The MetaSyn code for the instruction consists of a single instruction state. First the code checks for the end-of-loop condition—that is, whether all elements of the vector have been summed. This is done by means of an = 0 operator, as previously used in the instruction-decode section. If the summing has been completed, the result is placed on the stack, and the stack is cleaned up—in other words, the vector's start and length value are removed by a jump to the pop instruction code. Since that code ends with return, control returns to instruction-decode + 1.

If the sum is not completed, the memory location addressed by the a register is read while the current value of the vector length, stored in the b register, is simultaneously decremented via the built-in MetaSyn operator 1−. Contrary to what happens in a normal reading operation, the actual data from the memory is not stored, but is added to the value in vs, the running sum register. At the same time the current vector element address (in register a) is incremented for the next time through the loop. Again, because of the implied register timing, the value in the register will not change until the beginning of the next instruction state, so that address is maintained constant during the memory reading process. The final expression in this branch of cond sends control back to the vector-sum label for the next instruction state.

**A good trade**

When compiled, the 16-bit computer chip, complete with vector summing, measures 7.5 by 6.2 mm in area, or 12% larger than the original 16-bit FRISC. In return, it executes a vector sum more than 10 times faster than the old chip could—with software alone.

The redesign of FRISC involves one other cost—namely, the additional design time. In this case, the modification is so simple that it takes about 2 man-hours to modify the FRISC MetaSyn specification, create a vector-sum test program, and test the design using the MetaSyn simulator. Two more hours of compilation time is needed to produce the layout.

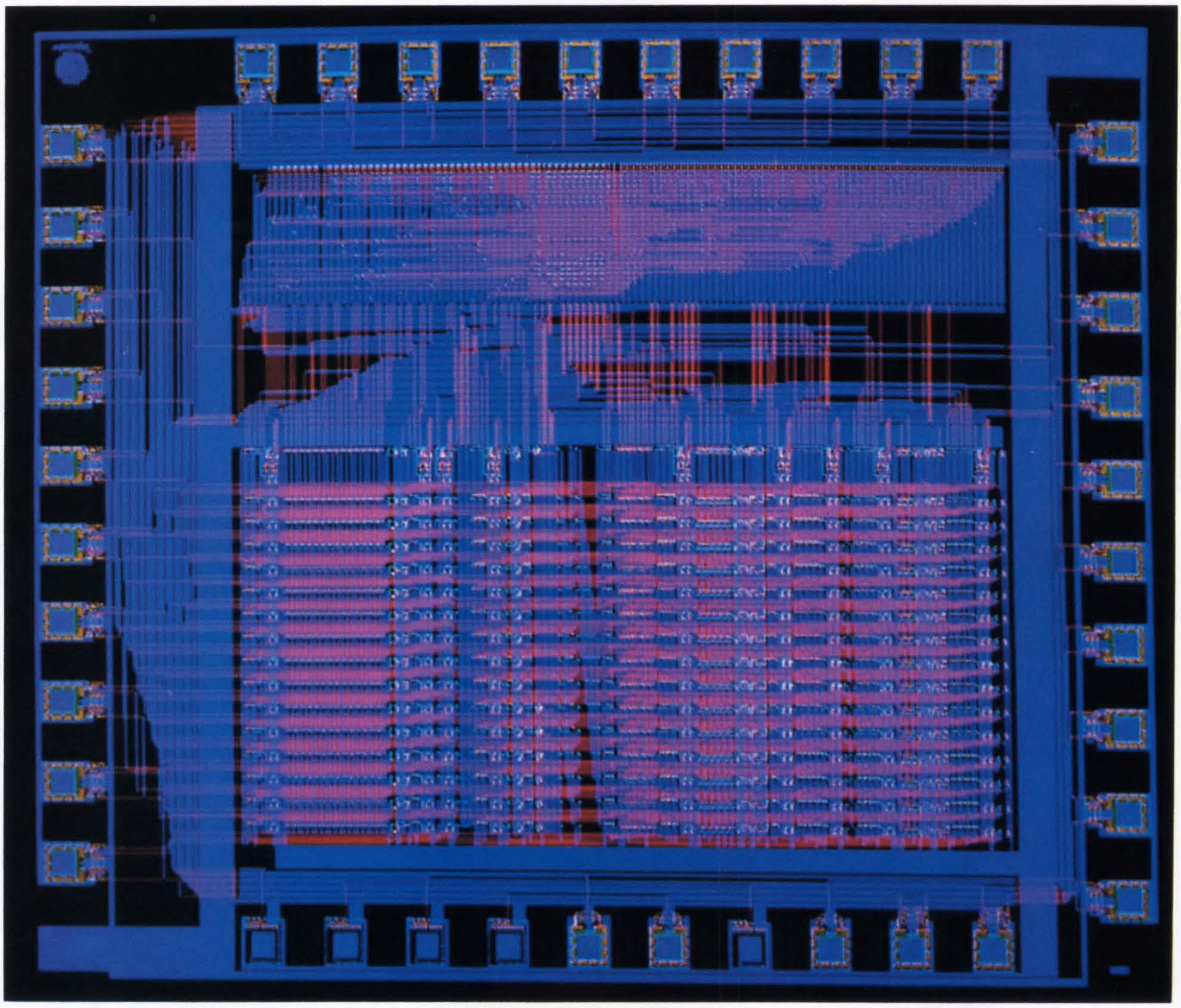
### Speedy compilation

Although the overall design time is most important, the compiler's actual CPU time is also of interest. There are two kinds of compilation time: the time from specification to interaction with the simulator, called "compilation to simulation," and the time to create the layout.

Compilation to simulation is very important, since it represents the innermost design loop. The largest designs compile to simulation in a few minutes, and the interactive response times are hardly affected by the size of the design.

As to layout time, small designs have compiled in a few minutes to half an hour; the largest designs, such as the FRISC chip, can take from two to four hours. These times apply to the August 1984 version of the MetaSyn compiler, running on a Symbolics 3600 Lisp machine with 474 Mbytes of disk storage and 1 Mword of semiconductor RAM.□





**6. A 16-bit version of the computer chip, ready for conversion to the CIF pattern-generation tape, has dimensions of 6.9 by 6 mm, based on a 4-$\mu$m single-metal NMOS process.**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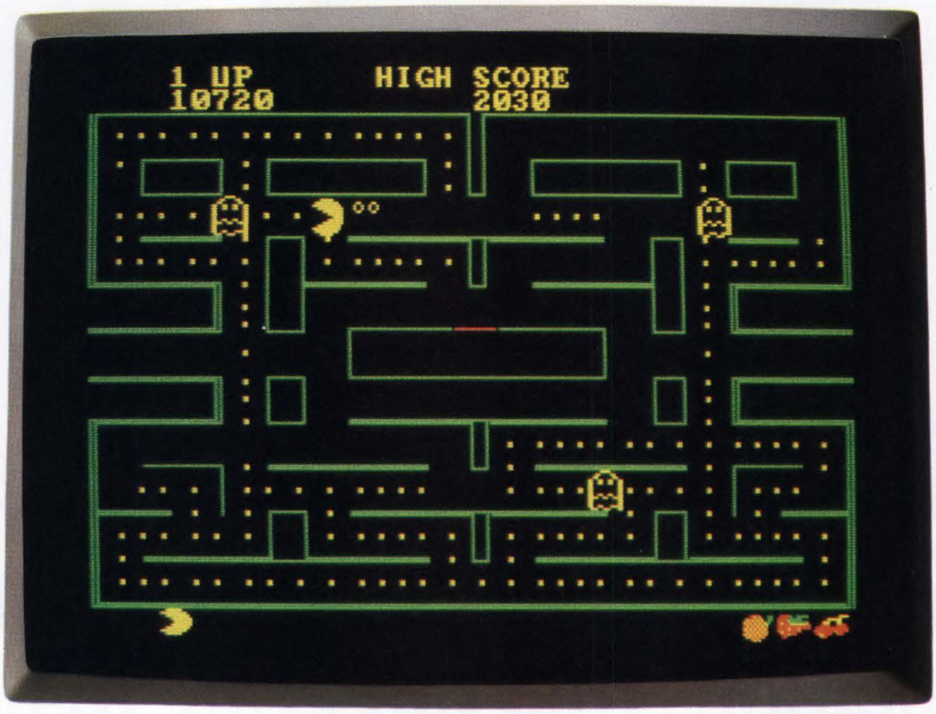


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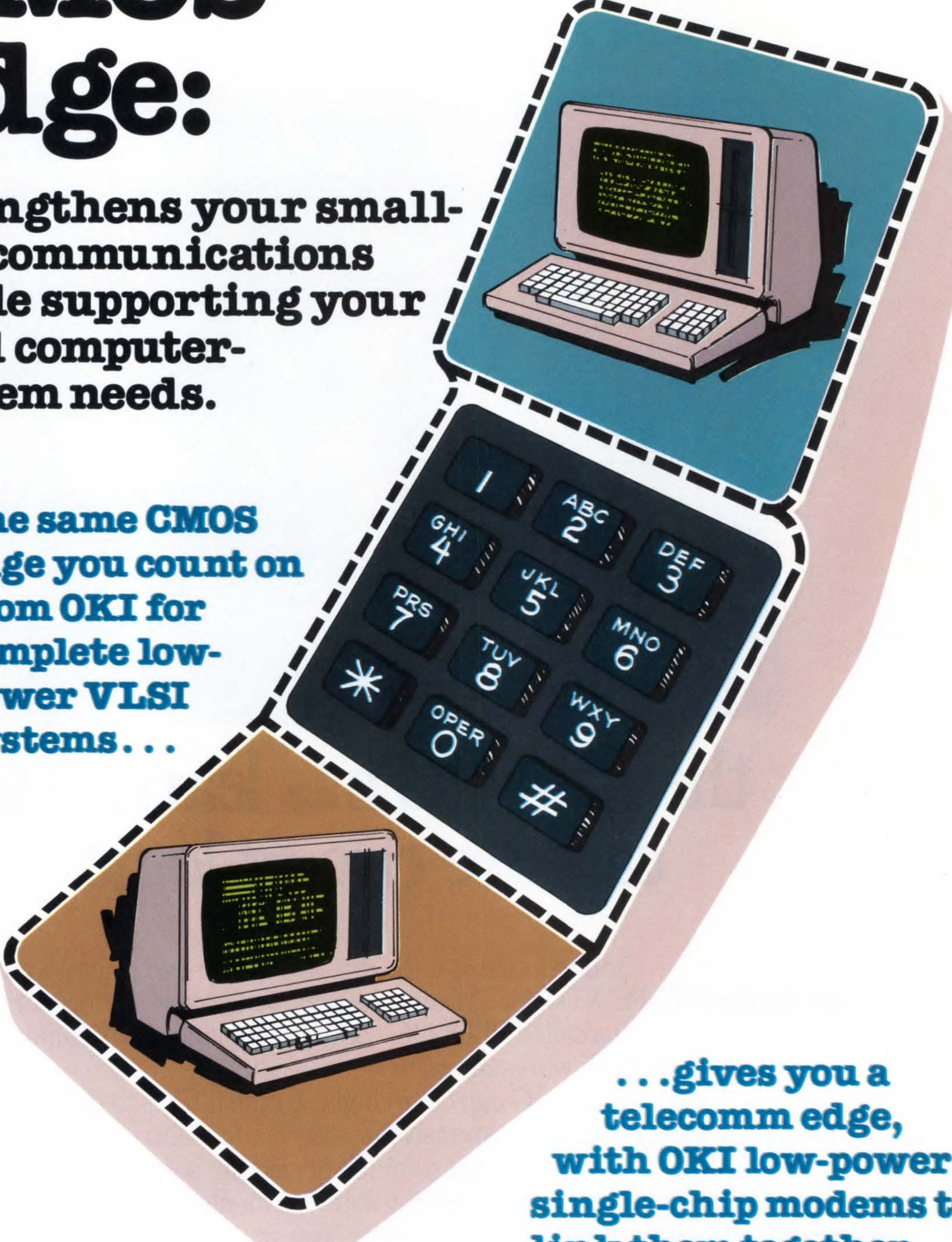


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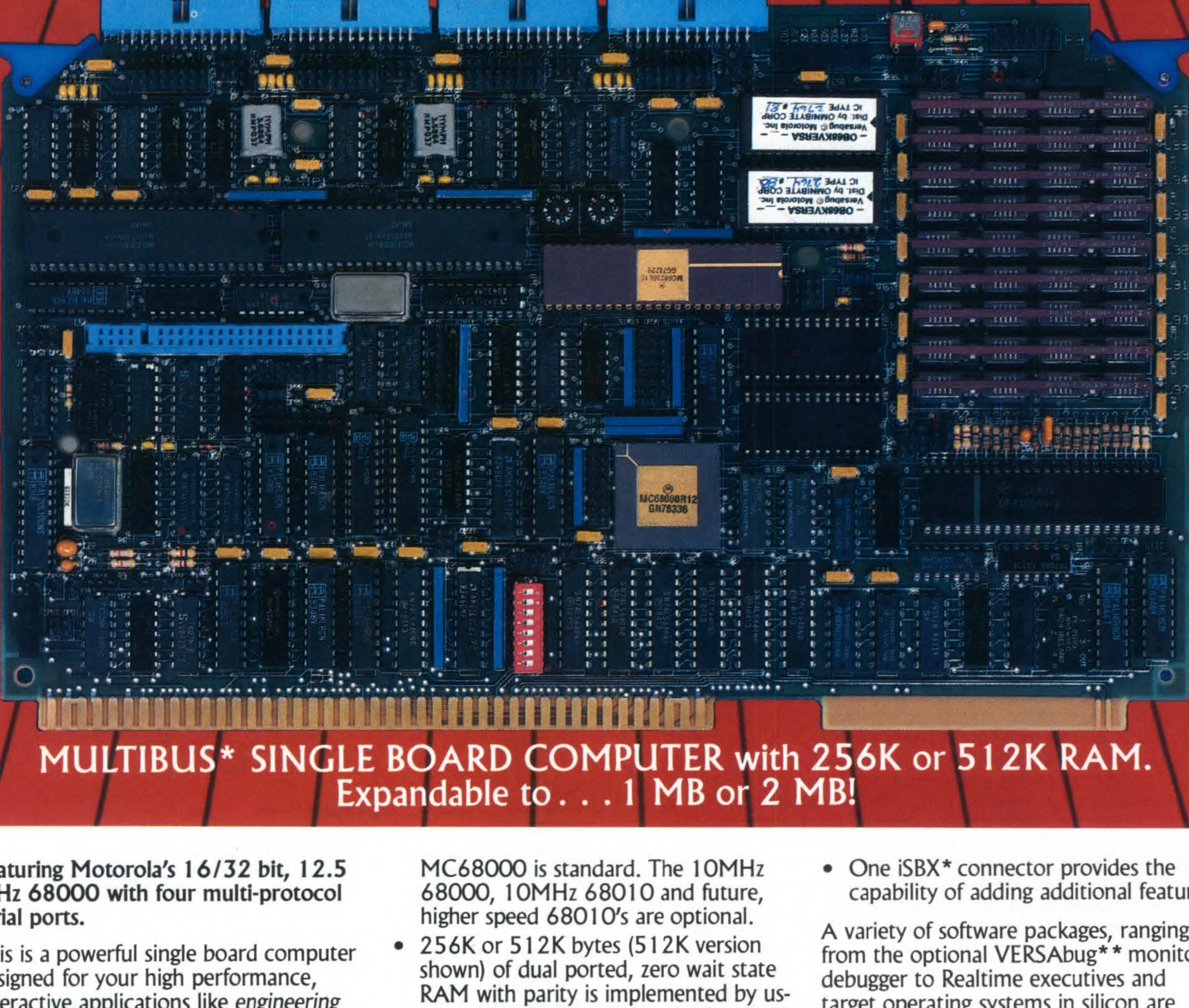

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# Software unites test program development with circuit design

*With tools that find simulator and tester limitations and suggest remedies, engineers can simultaneously design a VLSI circuit and generate test programs for it.*

Though high-level tester languages and advanced editing capabilities may simplify the jobs of design and test engineers, they tend to magnify the gap between creating a circuit and generating the test program for it. Identifying testing complications —such as timing complexities, initialization constraints, and a tester's physical limitations —requires detailed information that is rarely accessible to the test engineer. Furthermore, the information that might be available is usually obscured by postprocessing routines, which create test vectors by extracting only stimulus and response values from the simulation output.

In other words, the test engineer winds up with a set of test vectors that reveals little about the design itself. Moreover, some of those vectors prove invalid and are not discovered until the fabricated IC is placed in the tester.

To overcome these difficulties, a testing software package, dubbed VTItest, bridges the gap between designing a circuit and writing its test program. The software, which works with a test language called VTL, enables designers to develop a circuit and its test program simultaneously, notifying them in the early design stages of the tester-specific details that affect the circuit. Together these tools form an essential part of a graphically oriented VLSI design system that uses windows to access various design tools.

Through the test language, designers can create a file describing the physical characteristics, timing, stimuli patterns, and expected responses of a circuit under development. Then the remaining software translates the description into commands that run the simulation, verify the expected response, and store re-


**Ken Van Egmond,** VLSI Technology Inc.

*Ken Van Egmond has been with VLSI Technology in San Jose, Calif., for two years. As a design engineer, he developed the VTItest software and is closely involved with testing and testability issues. He holds a BS and a master's in EECS (electronic engineering and computer science) both from the University of California at Berkeley.*

quested response values predicted by the simulator (see the figure). Finally it generates a complete test program that includes all specifications for the timing generators, strobes, and registers; all pattern-loading, requested dc parametric, and summary test routines; and the test vectors needed to test the circuit functions.

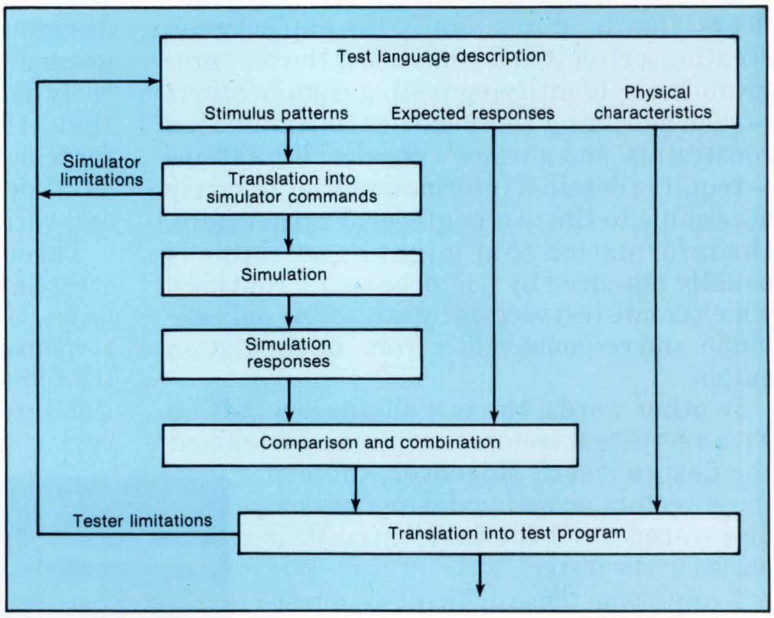
Besides merely identifying tester limitations associated with the test program—for instance, the number of accessible test pins or the placement of timing generators—the software suggests ways to work around them. In that way, engineers become familiar with both the problems and the solutions of testing, enhancing their ability to design testable circuits.

**Reaping the benefits**

Obviously, concurrently designing an IC and its test program means that engineers can make optimal design and testing trade-offs when difficulties arise. Because the circuit is still undergoing development, circuitry can be added to enhance the testing process. What's more, the circuit layout can be modified to enhance processing and testing for high-volume production.

The test vectors generated by the software have a 1:1 correspondence with the vectors used during simulation, so that the information normally lost duirng postprocessing is retained. And since the tester is no longer needed to develop the test program and initially debug it, it is available for production testing—a fact that obviously increases the tester's value.

To drive testers or simulators, the test software needs interface routines, which contain the simulator- or tester-specific information that enables the software to execute simulations and generate test programs. Moreover, the routines identify any portions of the test language description that cannot be executed




**With VTItest, designers can develop test programs while they are designing the circuit. The language takes into account both simulator and tester limitations, yielding a program that can be executed in the actual test environment.**

by the simulator or the tester. (Interface routines already have been written in Xidak's Mainsail for both VLSI Technology's simulator and Fairchild's Sentry Series 20, 10, and 7 testers.)

#### All in the definition

When developing an IC, designers can define the stimuli and the circuit's expected reaction through the test language, creating modules that describe aspects of the circuit's functions or dc test conditions. The resulting circuit description, which is independent of tester or simulator characteristics, is then combined with the tester-specific and simulator-specific interface routines.

Moreover, the circuit description contains the information needed for documenting and creating data sheets. Since that information actually drives the simulator and develops the test program, it always remains up-to-date. Furthermore, because all this design information is at hand when the circuit undergoes testing, test engineers can modify test programs without always calling in the design engineers.

Six types of modules are needed to create a complete test or simulation description. Designers use the first module, MAIN, both to describe the overall flow of the test or simulation and to initialize the test software for execution. The contents of MAIN declare the duration of a test or simulation cycle, select the required parameter modules, and specify their order of execution.

The physical characteristics of the IC are defined through the PINDEF (pin definition) module, which contains a declaration of the number of circuit pins and statements that the test software uses to identify pins during simulation or testing. Those pin-definition statements also specify a pin's type (for example, input, output, bidirectional, or power). In addition, the module may define the device type and state whether it is dynamic or static; if the device type is not specified, it is assumed to be static.

Minimum, nominal, and maximum timing parameters find their place in the TIMEPARAM module. Designers can test the circuit under different timing conditions by defining multiple modules and assigning each module its own identifier. Designers can thus vary the location of timing edges by selecting the appropriate module with MAIN.

A fourth module, EDGETIME, creates transition edges using the parameters defined by TIMEPARAM. Those edges indicate the point at which, say, an input pin should change value or an output pin should be checked for a particular value during a simulation or test cycle.

For example, creating a clock that remains at logic 0 for 80 ns, at logic 1 for 100 ns, and then repeats every 200 ns requires the definition of four edges. The first edge would be at 0 ns, the second at 80 ns, the third at 180 ns, and the fourth at 200 ns. The last edge defines the period of the cycle and also doubles as the duration declaration in MAIN.

#### Custom testing

For each test or simulation cycle, CYCLE modules describe the stimulus for input pins and the response for output pins. If parameter values are included within parentheses in the module heading, a variety of values can be placed on the circuit's pins. Each time the module is called, the appropriate values are passed to it. With FUNCTIONTEST modules, the designer partitions the test into functional blocks or initialization procedures, especially if the sections will be used more than once.

Three additional module types define dc parametric test conditions. The first, DCPARAM, sets the minimum and maximum measurement values, as well as the force (current or voltage) that creates them. If the designer does not yet know the appropriate values for the parametric tests, he or she may invoke the software's default values.

Next, the PINGROUP module defines identifiers that access groups of the IC's pins during testing. The designer tests the predefined dc parameters of a group of pins by assigning an identifier to it.

#### Helpful routines

Finally, the DCTEST module accesses predefined parametric routines, which demand that the design engineer initialize the circuit to the proper state and identify the pin group to be tested. Predefined routines measure, for instance, output voltage, input leakage current, and power pin leakage current. To set the test's measurement and forcing-function values, the declarations from the dc parameter module come into play.

The test language itself possesses all the power and flexibility needed to efficiently develop test programs. All variables and constants are 32-bit data values that may be manipulated on a bit-by-bit basis by an assortment of familiar operators, such as XOR, SHL (shift left), and SHR (shift right). Furthermore, the language's looping constructs present a compact means of conditionally executing a series of stimulus and response values. Additionally, since the various modules can essentially pass their parameters, the designer can alter the program—say, by inserting different stimulus and response values—without rewriting an entire test or simulation routine.

A good way to get a feel for the test language is to examine portions of a circuit description for a CRT controller, which generates the signals necessary to interface a digital system with a raster-scan CRT display. In that type of display, an electron beam starts on the left side of the CRT, quickly moves horizontally to the right, and returns to its original position. After each such scan, the beam moves down incrementally until it reaches the bottom of the CRT. At this point, one "frame" has been displayed. The beam is then reset to the upper-left corner, and the process repeats.

The PINDEF module specifies the physical characteristics of the circuit (Program 1). The

**Program 1. Physical characteristics and timing information**

```
PINDEF;          #  Defines the physical characteristics of the device
BEGIN
  DeviceName CRTcontrol;                #  Assigns a name to the device
  DeviceType Static;                    #  Declares the device type
  TestPins 40;                          #  Declares the number of pins

  Vss                :=  1,     Ground;  read_writeB     := 22,    Input;
  resetBar           :=  2,     Input;   enable          := 23,    Input;
  lightPenStr        :=  3,     Input;   register_sel    := 24,    Input;
  memoryAddr [13:0]  :=  17:4,  Output;  chipSelBar      := 25,    Input;
  display_time       :=  18,    Output;  dataBus [7:0]   := 26:33, Bidirection
  curs_display       :=  19,    Output;  rasterAddr [4:0] := 34:38, Output;
  Vcc                :=  20,    Power;   horiz_Sync      := 39,    Output;
  clock              :=  21,    Input;   vert_Sync       := 40,    Output;
END;

TIMEPARAM normal_time;                  #  Declares the timing parameters used by the
BEGIN                                   #  EDGETIME module to create transistion edges
  begin _cycle :=     0n,      5n,    10n;
  end_cycle    :=   480n,    500n,   520n;
END;

EDGETIME;   #  Creates transition edges within a cycle
BEGIN
  End_Of_Cycle  :=  end_cycle.nom;
  phase1        :=  begin_cycle.min;
  phase2        :=  end_cycle.nom/2;
  delayTime     :=  end_cycle.nom - 50n;
END;
```

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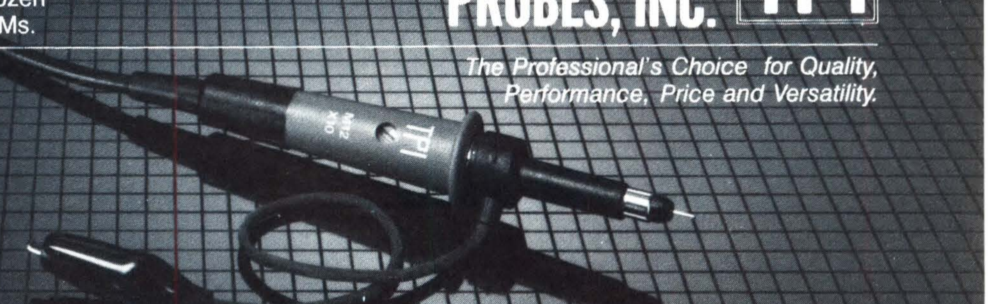

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## CAE: Testing software

first three statements assign the name CRTcontrol to the device, identify it as a static device, and spell out 40 circuit pins. The remaining statements take the basic form:

identifier {x:y} := pinList, pinType

where x:y optionally defines the most significant to least significant bits of a bus structure, PinList presents the positive integers declaring the pin configuration, and pinType labels the pin's type as input, output, bidirectional, power, ground, three-state, open-drain, open-source, or no connection. Although pin numbers are assigned arbitrarily, tester restrictions could force the designer to reassign the locations once the test program is generated. When a particular simulator or tester cannot handle all of the physical requirements, the software notifies the designer.

The program also shows the TIMEPARAM module, which defines the minimum, nominal, and maximum time parameters, and the EDGETIME module, which takes these parameters and creates transition edges for the CYCLE modules. The transition edges determine when the stimulus values are placed on the input pins and when the response values are verified during each simulation or test cycle.

Although only basic timing information appears in the program, designers are free to create as many transition edges as necessary to verify device timing completely. If a particular tester or simulator cannot execute all the transition edges, the software identifies the limitations and suggests a possible alternative.

The MAIN module partitions the simulation or testing of the CRT controller into a number of steps, thereby setting up a high-level view of the program flow (Program 2). The circuit is first initialized to a known state; afterward the horizontal and vertical registers, the cursor's start/stop and blinking functions, and the interlacing of sync and video modes are individually tested.

### Down to the nitty-gritty

The DURATION statement determines the length of the simulation or tester cycle, and normal-time selects the timing parameter module of the same name. Finally, the WRITE commands place remarks in the simulation or test program file, where they can be extremely valuable during simulation or test debugging. The identifiers (to the right in the program) call the FUNCTIONTEST or CYCLE modules that determine the flow of the simulation or test program. The identifiers also pass values to these modules during execution.

The FUNCTIONTEST modules further break down the simulation and testing stages in more detail, with some of the portions used more than once (Program 3). These modules are exe-

**Program 2. Simulation or test program flow**

```
MAIN;      #  Defines the simulation or test program flow
BEGIN
  DURATION End_Of_Cycle;  #  Set the period for the cycle
  normal_time;            #  Select the time parameters
  WRITE "Initialize all registers";                      Init_Reg;
  WRITE "Test the horizontal registers";                 Horiz_Test;
  WRITE "Test the cursor start/stop function";           Cursor_Test;
  WRITE "Test the vertical registers";                   Vert_Test;
  WRITE "Verify cursor blinks, 16 and 32 field rate";    Cursor_Blink;
  WRITE "Test interlace of sync and video modes";        Sync_Video;

END;
```

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CIRCLE 106

cuted when they are called by MAIN or by another FUNCTIONTEST module. Some of the modules contain WHILE or other looping constructs, which provide a means of conditionally executing a statement or group of statements.

Finally, the CYCLE modules apply stimuli and verify responses during a simulation or test cycle (Program 4). At various times during simulation or testing, parameters passed to these modules cause different values to be applied to particular pins. CYCLE statements in the modules specify whether the affected pin is being stimulated by the values (←) or whether the pin is generating the values (→).

When the test software is driving a simulator, each execution of a CYCLE module causes the values defined in that module to be applied to the pins at the appropriate transition edge time. The simulation runs until the next value or values are applied. At the specified transi-

**Program 3. Functional partitioning of tasks**

```
FUNCTIONTEST LoadReg ( dataSet, dataValue ) ;      #  Load the registers
BEGIN
  Variable tempVal, newVal ;
  IF dataSet THEN
    tempVal  := 0
  ELSE tempVal  := 1 ;
  write_Reg ( 0, 0, tempVal, 0, dataValue, X, X, X ) ;
  write_Reg ( 1, 0, tempVal, 0, dataValue, X, X, X ) ;
  write_Reg ( 0, 0, tempVal, 0, dataValue, X, X, X ) ;
END ;

FUNCTIONTEST Horiz_Test ;    #  Test the horizontal circuitry
BEGIN
  Variable instruct ;
  WHILE instruct < 7 DO
  BEGIN
    CASE instruct OF
    BEGIN
      [0]  BEGIN
             HorSync ( 'HA, 0 ) ;      #  Check horizontal sync with loc = A, width = 0
             Raster ('H1F) ;           #  Check raster address to 'H1F
           END ;
      [1]  BEGIN
             HorSync ('HA, 'HF) ;      #  Check Horizontal sync with loc = A, width = F
             MemAddr ('H3F) ;          #  Check memory address to 'H3F
           END ;
      [2]  HorSync ( 'H55, 'H5 ) ;     #  Check horizontal sync with loc = 55, width = 5
      [3]  HorSync ( 'HAA, 'HA ) ;     #  Check horizontal sync with loc = AA, width = A
      [4]  BEGIN
             HorSync ( 'HFF, 'H1 ) ;   #  Check horizontal sync with loc = FF, width = 1
             HorizReg ( ' HFF ) ;      #  Check horizntal total and display = FF
           END ;
      [5]  HorizReg ( 'HAA ) ;         #  Check horizontal total and display = AA
      [6]  HorizReg ('H55) ;           #  Check Horizontal total and display = 55
      [ ]  WRITE "Error—Invalid instruction executed";
    END ;
    instruct  := instruct + 1 ;
  END ;
END ;
```

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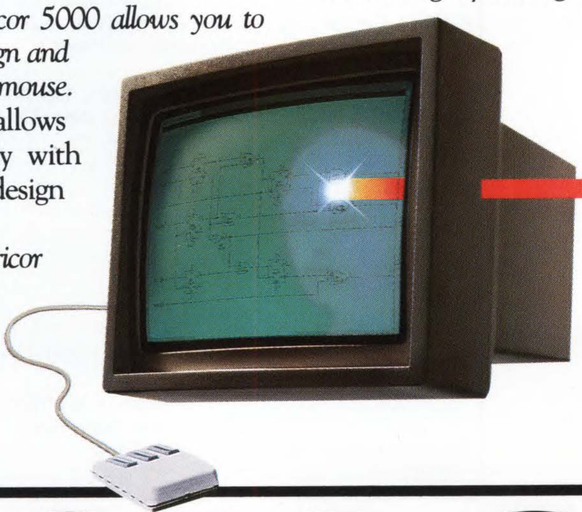
**CIRCLE 107**



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tion times, the expected response values are compared with the actual, and the requested response values are stored.

The transition edge at which pin values are entered or generated is specified by @time. If that is not specified, stimulus values are placed on the pin at the beginning of the cycle and responses are measured at the end of the cycle. When the response value is specified with a ?, the designer knows that the response value predicted by the simulator for that edge has been stored by the test software. When the software generates the test program, it combines the stored values with the expected response and stimulus values to create the test vectors.

### Considering the tester

As the software generates the test program, it draws on the stimulus and response values to select each pin's timing generators, strobes, and mask registers (which have tester-dependent characteristics and restrictions). The software assigns timing generators and strobes on the basis of value of the pin before the cycle starts, the number of transitions occurring on the pin during the cycle, and whether the pin is to be an input or an output during the cycle.

The selection of mask registers is determined by the state of the registers at the start of the cycle and by the pins that have been activated during the cycle. The appropriate values are inserted into a test vector, which is stored in a vector file with the register set or enable commands. Before storing the test vector, the software attempts to take advantage of any vector compaction capability of the tester.

After the test language is used to create the modules, the resulting description file is loaded into VTItest, which parses it and ensures that its syntax is correct. While parsing, the software creates a data base from the physical characteristics described in PINDEF and from the identifiers used throughout the circuit description. After a syntactically correct description has been loaded, the designer can begin simulating the circuit or generating the test program.□

| How useful? | Circle |
|---|---|
| Immediate design application | 550 |
| Within the next year | 551 |
| Not applicable | 552 |

**Program 4. Stimulus and expected response values**

```
CYCLE clockIt;        #  Clock the circuit
BEGIN
   clock <- 0 @ phase1, 1 @ phase2, 0 @ End_Of_Cycle;
END;

CYCLE write_reg ( enableVal, chipVal, regVal, readVal, dataVal, address,
                  horizPulse, vertPulse ) ;    #  Write the register
BEGIN
   clock          <-  0 @ phase1, 1 @ phase2, 0 @ End_Of_Cycle;
   MemoryAddr     ->  address @ delayTime;
   enable         <-  enableVal;
   chipSelBar     <-  chipVal;
   dataBus        <-  dataVal;
   horiz_Sync     ->  horizPulse;
   vert_Sync      ->  vertPulse;
   register_sel   <-  regVal;
   read_writeB    <-  readVal;
END;

CYCLE viewBus ( BusData ) ;      #  Verify the response values on the bus
BEGIN
   clock       <-  0 @ phase1, 1 @ phase2, 0 @ End_Of_Cycle;
   dataBus     ->  BusData @ delayTime;
   rasterAddr  ->  ? @ delayTime;
END;
```


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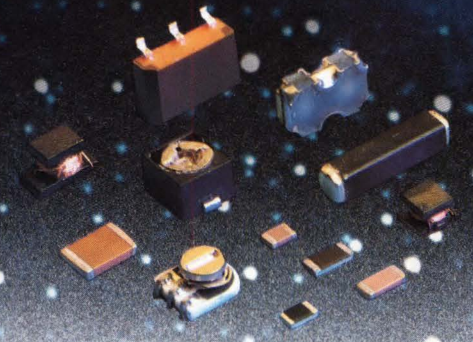

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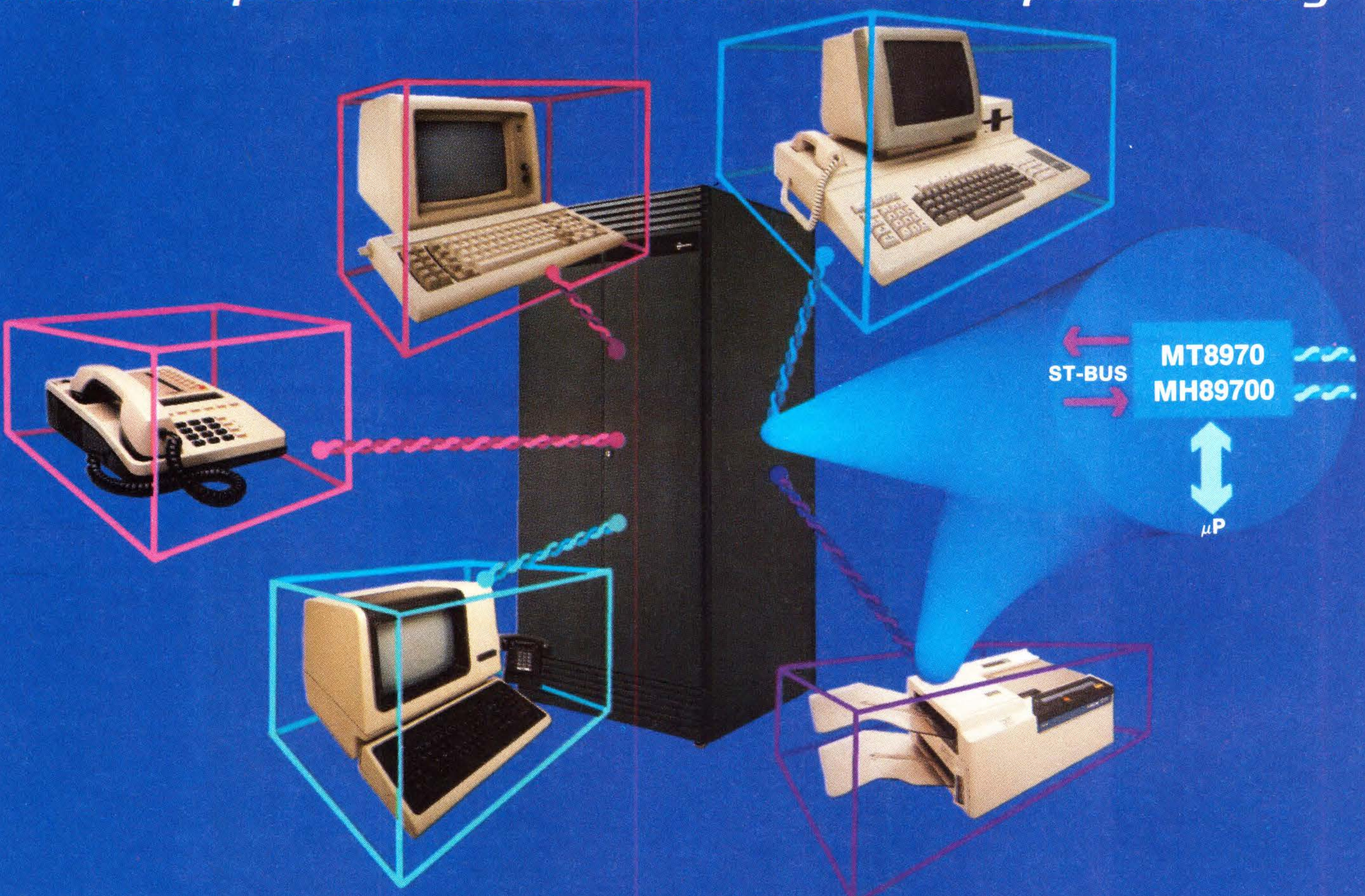


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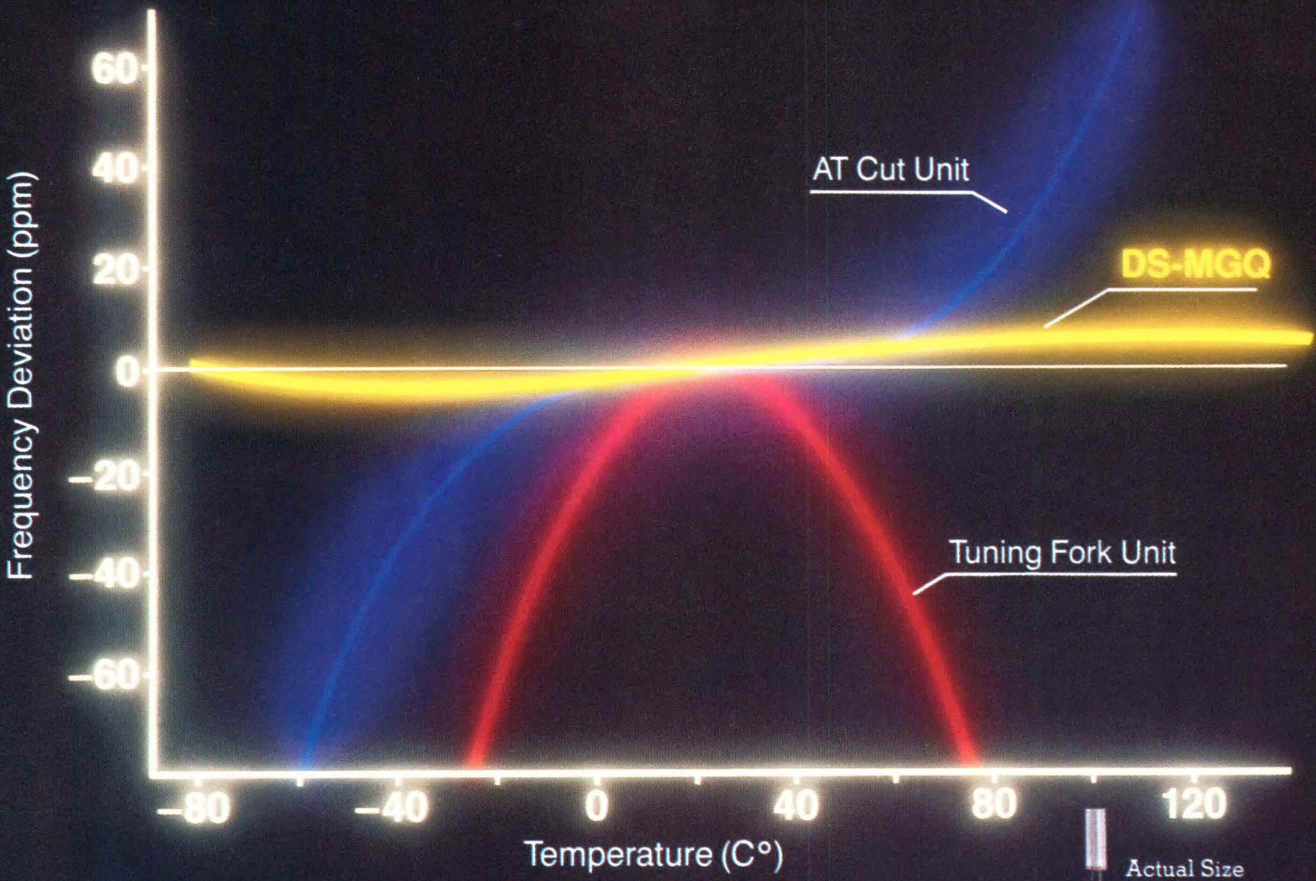


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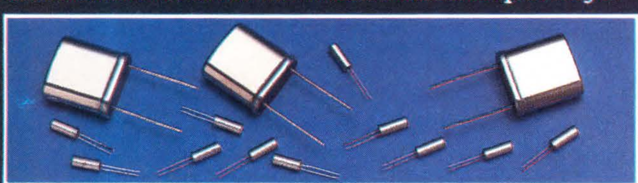

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|---|---|
| Frequency Range | 1.0 to 3.0 MHz |
| Load Capacitance | 10pf standard (other settings on request) |
| Quality Factor | 150,000 to 300,000* |
| Effective Series Resistance | 35Ω to 100Ω* |
| Frequency Temperature Stability (−30°C to +70°C) | ±5ppm to ±100ppm |
| Drive Level (Max) | 3 to 20μW* |
| Aging (First Year +25°C) | 1.0ppm (typical) |

*Depending on Frequency

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CIRCLE 115

# Microprogrammable chips blend top performance with 32-bit structures

*Broken down into 32-bit functional blocks instead of being sliced into multiple-bit sections, five VLSI bipolar chips match a supermini's speed.*

Designers of systems and subsystems for high-speed computation, intelligent peripheral control, and array and digital signal processing typically need higher performance than standard microcomputer parts can deliver. The required precision, speed, and virtual memory support has to some degree been supplied by dedicated VLSI components that are customized for particular applications. Yet an overwhelming need still remains for a set of building blocks that can bring extremely high performance to a large assortment of applications.

A new approach extends the bit-slice concept to 32 bits and also satisfies system designs that require cycle times of less than 100 ns. With a family of five VLSI chips, designers of microprogrammed systems can count on cycle times of 70 to 80 ns, using merely a handful of components. The building blocks for 32-bit systems functionally partition the chips and separate the register file from the rest of the data path.

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*As product planning manager for array processors at AMD, Bernard J. New is responsible for conceiving and defining arithmetic computing devices. The holder of a BSc (Hons) in electronic engineering from England's University of Birmingham, New has two patents on Am29500 products.*

The following two articles first explore the key members of the Am29300 family and then focus on a floating-point processor, which is the first chip scheduled for sampling. Details are given on how to use the chip and other devices in the series to build a fast Fourier transform computer, as well as more general-purpose digital signal-processing circuits.

The Am29300 family addresses the problem of fault detection through an interlocking checking scheme—parity and master-slave. Byte parity is generated, stored, and then checked on all data-path elements as a means of detecting interconnection failures. Moreover, to verify certain functions, the master-slave operating mode permits two units to be connected in parallel, with one unit actually handling the computation and the other checking the result cycle by cycle.

Detecting a fault triggers an interrupt at the microinstruction level. Unlike previous redundant schemes, no specialized software is required. Furthermore, communication among the redundant functional units causes no system degradation.

The five chips form a strong foundation for any system designer's work. For instance, a 16-bit sequencer can handle interrupts and traps at the microinstruction level. There is also a combined ALU and shifter that internally supports variable byte and bit fields. Together with the ALU-shifter chip, a true dual-port register file, organized as 64 words by 18 bits, can build a basic system. The register file, designed for simultaneous read and write accesses, is separated from the data-path elements, thereby avoiding the problem of addressing an internal register file differently from external memory. The benefits of that separation are uniform register addressing and unlimited depth expansion.

Two accelerator chips—a floating-point processor and a parallel multiplier—can be added to the basic system to raise the number of functions and cut processing time. The 32-by-32-bit parallel multiplier can, on successive cycles, expand to 64 by 64 or 128 by 128 bits, without help from external logic. For its part, the math chip can tackle single-cycle addition, multiplication, subtraction, and conversions—all in single-precision IEEE or DEC formats.

Because of functional partitioning, a three-bus flow-through architecture was chosen as the data path. For maximum bus accessibility, all data-path elements—the integer processor and the parallel multiplier, for example—share two operand and one result bus. The flow-through architecture not only transfers data extremely quickly but also avoids the complex timing control needed to turn around bidirectional buses. Above all, the simplicity of the three-bus architecture allows these components to be configured in a variety of ways to optimize micro-architectures for different jobs.

# Bipolar building blocks deliver supermini speed to microcoded systems

As CMOS processes start to encroach on the performance of bipolar circuits, bipolar technology is taking the next step to keep itself in the lead for the highest speed systems. A family of five bipolar VLSI computational circuits—fabricated with a scaled, ion-implanted, oxide-isolated process and three levels of metal interconnections for high density—provides a set of functionally partitioned microprogrammable VLSI building blocks for systems such as superminicomputers, digital signal processors, high-speed controllers, and many others. The modularity of the system functions ensures that the chips can meet the performance requirements of a general-purpose superminicomputer, as well as those of an image processor, which are radically different from each other.

Included in the family are three parts that form the core of a general-purpose microprogrammed system: a 32-bit arithmetic and logic unit (ALU), a 16-bit microprogram sequencer, and a 64-by-18 four-port, dual-access RAM. And, for systems that do a large number of multiplications or floating-point

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*Øle Moller is also a design engineer in AMD's product planning operation. He holds an MSEE from the Technical University of Denmark.*

*Another engineer in product planning, David Sorensen specializes in programmable processors. He holds a BSEE from Arizona State University.*

operations, two performance accelerators—a 32-by-32-bit multiplier and a 32-bit floating-point processor will be available to tie onto the buses (see Design Entry, p. 246).

The chips offer high performance, a flexible architecture, and microprogrammability, and even address the problem of fault detection for data integrity. These circuits can thus support an extremely fast microcycle—about 80 ns (projected). That high speed is the result of several design considerations: Each part is designed internally with emitter-coupled logic but has TTL-compatible inputs and outputs. Second, more power was allocated to the logic circuits used in the critical paths than for logic in the noncritical paths on each chip, to maximize the speed. Third, by integrating highly specialized logic on chip it is possible to execute very complex operations in a single cycle.

The microprogrammability of this chip set offers several benefits to the system designer. It provides a structured and systematic approach for implementing the control mechanism of the system, and like the bit slices, it allows the instruction set to be customized to suit the designer's application (see "Architectural Limitations of Bit Slices," opposite). And several versions of the initial design can be tested, or current designs can be enhanced simply by changing the microcode.

Thus, the functionally partitioned Am29300 family overcomes all of the performance penalties of bit-slice structures, while maintaining its ability to form a wide variety of architectures. Even though the chips are designed to work together as a family, each can also be used independently in an application that requires its unique capabilities.

#### Pipelines are out

The flexibility of the Am29300 family is largely due to a decision not to place pipeline stages within the functional blocks. Not including the pipeline registers inside incurs some off-chip delays. This is a small price to pay to allow system designers to optimize the pipeline structure for their individual needs. Moving the register file out of the functional block for the ALU also slows things down. At the same time it does not force a fixed register size on the user, enabling systems to be created with dedicated registers, register windows, or register banks—all with neither fixed depth nor width.

Additionally, the high level of integration helps eliminate the propagation delays often encountered when signals must go from chip to chip. The use of VLSI also results in fewer parts at the system level, which, in turn, conserves power (usually many watts in the case of bipolar systems) and board space. Lastly, a complete 32-bit solution is provided for applications that require increased precision for arithmetic operations, high memory bandwidth, and a

### Architectural limitations of bit slices

The limited performance of bit-slice circuits can be improved by increasing the width of the slices. That higher level of integration results in higher performance by reducing the number of off-chip delays while preserving the flexibility that has made bit-slice systems so attractive. However, as higher levels of integration become possible, two inherent problems with bit-slice architectures will limit their ultimate speed. The first involves the off-chip delays inherent in cascading. For example, the carry chain is usually the slowest path of an ALU. Breaking this chain between slices introduces off-chip delays into the critical path.

The second problem is that the functional needs of many systems do not slice well. Barrel shifters and prioritizers are especially difficult to cascade. Unfortunately, the ability to perform N-bit shifts and locate the position of leading 1s are of greatest importance in applications that require heavy number crunching and manipulation of data fields, such as image processing, graphics, database management, and controllers. These are precisely the applications whose need for speed forces the use of bit-slice devices. The system performance is compromised not only because these operations must be done bit by bit, but also because many high speed algorithms cannot be efficiently implemented.

## Microprogrammable 32-bit chips

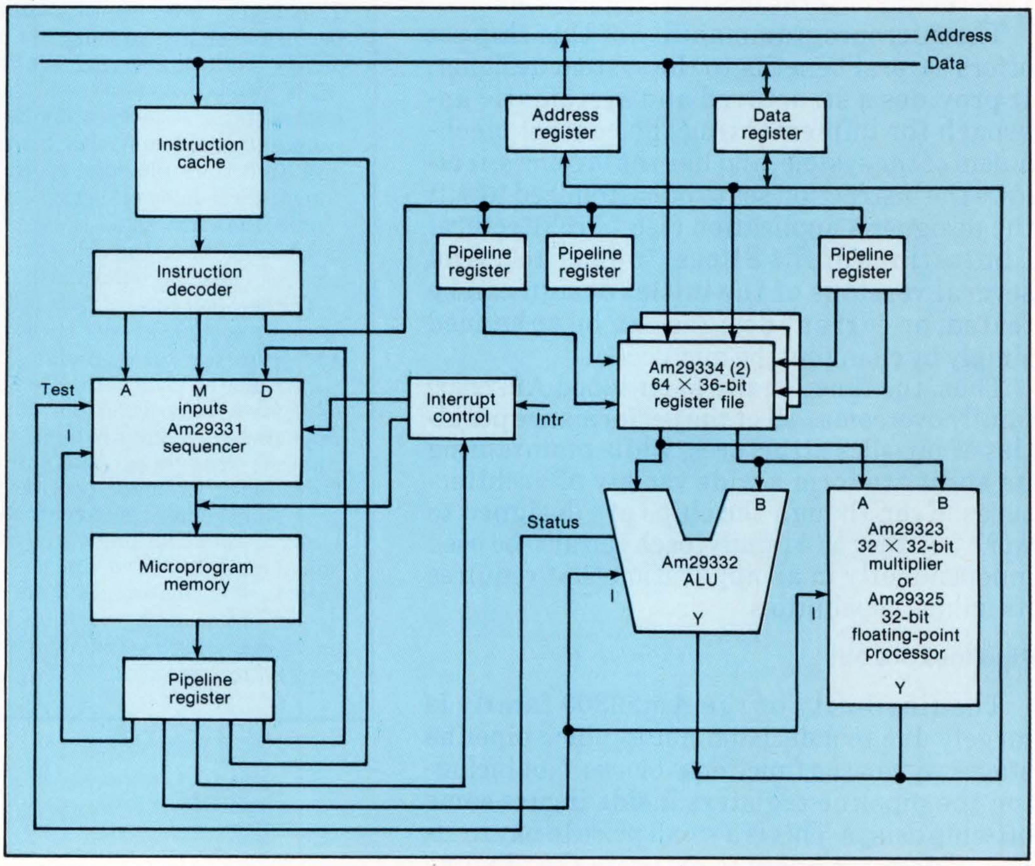
large addressing capability (4 billion bytes) to support virtual memory systems (Fig. 1).

The performance of a system depends, not just on its raw computing speed, but on its ability to respond to events such as interrupts and traps. For example, the Am29331 sequencer responds to both interrupts and traps at the microprogram level very quickly, and its response is completely transparent to the interrupted microroutine. Also, the Am29332 ALU indirectly supports the handling of these events by allowing its internal state to be saved or restored.

The Am29332, a noncascadable 32-bit-wide, ALU, provides fast number crunching, high data transfer rates, and powerful bit-manipulation capabilities. Intended to be used with the Am29334 dual-ported RAM, which serves as an external register file, the ALU has two 32-bit input buses (DA and DB) and one 32-bit output bus (Y).

Internally, the device has a 32-bit data path that interconnects its various functional blocks. These blocks include various shifters and multiplexers, a mask generator, a funnel shifter, the ALU proper, a priority encoder, a parity generator and checker, a master-slave comparator, and the status and Q registers (Fig. 2). The ALU proper has three 32-bit inputs: R, S and M. The R input comes from the funnel shifter, the M input from the mask generator, and the S input from a variety of sources —the DA or DB buses, status register, or the Q register.

The power and flexibility of the Am29332 comes partly from its ability to perform operations on various data types. It can operate on



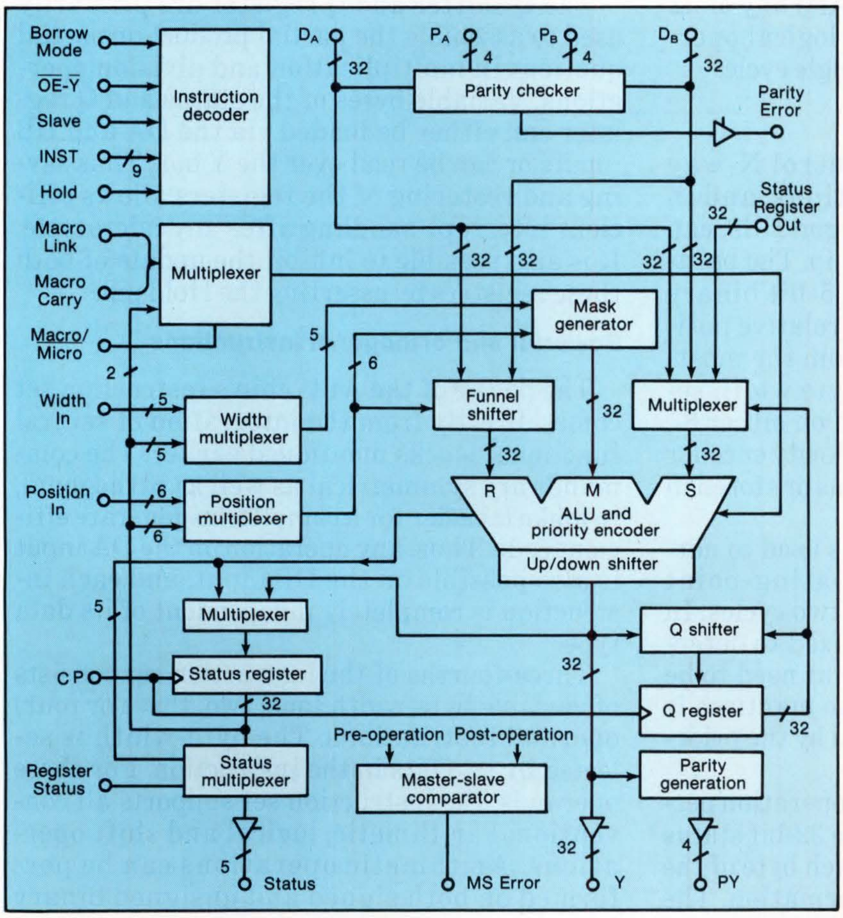

**1. A conventional CPU, built with Am29300 building blocks, forms the focal point of an extremely compact system that cycles as fast as 80 ns.**

variable bytes, variable-length bit fields, or single bits. This is made possible by the internal mask generator, which creates a 32-bit mask for each instruction (with no time overhead). The mask is used as an additional operand in each instruction to allow the operation on only selected data widths.

The type of mask generated depends on the type of instruction. For instructions that operate on variable bytes (1, 2, 3 or 4 bytes) the mask is a fence of 1s (bit 0 aligned) for all low-order selected bytes with a fence of 0s for all high-order unselected bytes. Instructions that operate on variable-length bit fields require a mask that is a string of contiguous 1s for all selected bit positions and 0s for all unselected bit positions. In cases where the field exceeds the 32-bit boundary, the mask does not wrap around, thus allowing operation on a contiguous field across a word boundary. For instructions that operate on a single bit, the mask is a 1 for the selected bit position and 0s for the other unselected bits.

For most single-operand instructions, the unselected bit positions pass the corresponding bits of the operand unmodified. For most two-operand instructions, the unselected bit positions pass the corresponding bits of the operand unmodified on the DB input. Thus, for two-operand instructions the mask allows the merging of two operands in a single cycle. In addition to being used internally, the mask can be sent out over the Y bus, permitting the generator to be used as a pattern generator for testing purposes.

To speed various mathematical and logical operations, many circuits have started to in-




**2. To connect its various internal functional blocks, the Am29332 ALU employs a 32-bit bus. Among the chip's major features are a 64-bit funnel shifter, parity checking and generation, and a basic 32-bit ALU that has three input ports. The processor also has three 32-bit ports through which it transfers data into and out of the chip.**

clude a barrel shifter, which has an N-bit input and an N-bit output. The barrel shifter would be used to shift or rotate the operand either up or down from 0 to N bits in a single cycle. Such high-speed shifting is very useful in operations such as the normalization of a mantissa for floating-point arithmetic or in applications in which the packing and unpacking of data are frequent operations.

However, a more useful circuit is a funnel shifter, which can be thought of as having two N-bit inputs and one N-bit output. Just such a circuit (with 32-bit-wide ports) was included on the 29332. The circuit can perform all the operations of a barrel shifter with capabilities extended to two operands instead of one. In addition, it can extract a 32-bit contiguous field across its two operands, a function very useful in several graphics applications. And any of its operations can be followed by a logical operation, with both completed in a single cycle.

### Setting the priorities

Prioritization, useful to control N-way branches, perform normalizations, and in graphic operations such as polygon fills, can readily be handled by the ALU chip. The built-in priority encoder sends out a 5-bit binary weighted code that signifies the relative position of the most-significant 1 from the most-significant bit position of the byte width selected. That allows prioritization on either 8-, 16-, 24-, or 32-bit operands. The priority encoder output can be passed on to the Y bus or stored in the status register.

If, for example, prioritization is used to normalize a mantissa during a floating-point arithmetic operation, it requires two cycles. In the first, the mantissa is prioritized to determine the number of leading 0s that need to be stripped off. In the next cycle, the mantissa is shifted up by the amount specified by the priority encoder output.

Relevant information for each operation performed by the chip is stored in the 32-bit status register after each microcycle. Each byte of the status word holds different information. The least-significant byte holds the position specifier. The next most-significant byte holds the width specifier and three other bits that are used to test the comparison of unsigned and signed operands. The next byte contains the Carry, Negative, Overflow, Link, Zero, M and S flags. The M flag stores the multiplier bit for multiply or the sign compare bit for signed division, and the S flag stores the sign of the partial remainder for unsigned division. The most significant byte stores the nibble carries for BCD operations.

The states of the Carry, Negative, Overflow, Link and Zero flags are available on the status pins, and the status multiplexer allows the user to select either the status of the previous instruction (register status) or the status of the current instruction (raw status) to appear on the status pins. The raw status could be used to update an external macro status register. This also allows branching at either the micro- or macro-level.

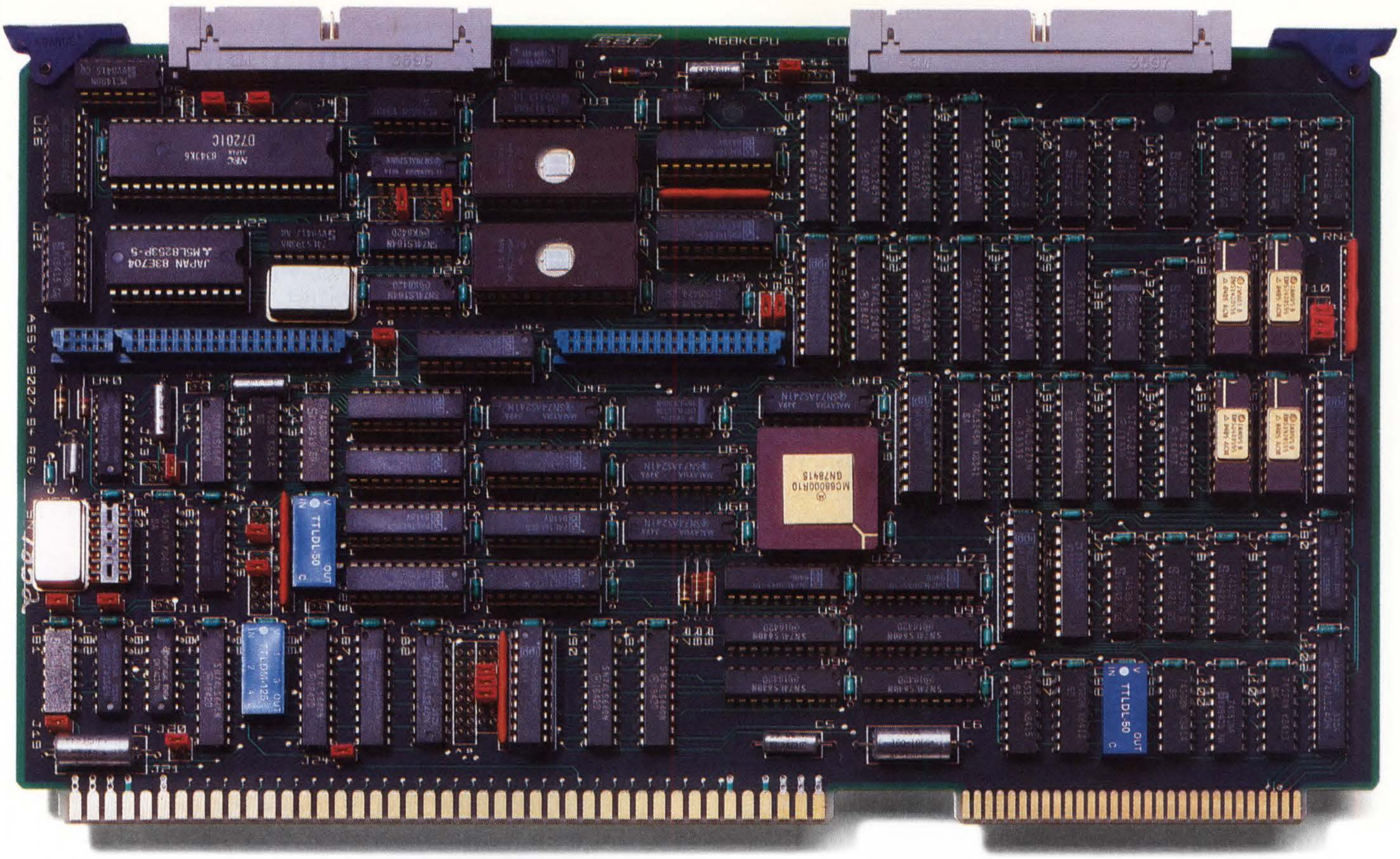
The Q shifter and Q register are primarily used to assemble the partial product or partial quotient in multiplication and division operations. Variable bytes of the status and Q register can either be loaded via the DA and DB inputs or can be read over the Y bus. Thus saving and restoring of the registers allows efficient interrupt handling after any microcycle. It is also possible to inhibit the update of both these registers by asserting the Hold pin.

### Powerful and orthogonal instructions

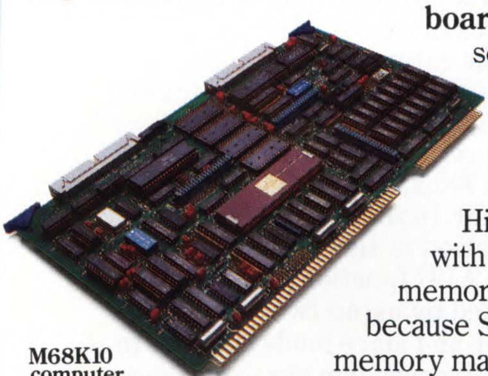
The power of the ALU chip's instruction set comes directly from the integration of several functional blocks mentioned earlier. The commands are symmetrical as well as orthogonal, to make it easier for a compiler to generate efficient code. Thus, any operation on the DA input is also possible on the DB input, and each instruction is completely independent of its data type.

Three-fourths of the instruction set consists of variable byte-width (one, two, three or four) operand instructions. The byte-width is selected by two bits in the instruction. For these operands, the instruction set supports all conventional arithmetic, logical and shift operations. Arithmetic operations can be performed on both signed and unsigned binary integers.

Additionally, the instruction set supports multiprecision arithmetic such as addition with carrying and subtraction with carrying or







M68K10 computer

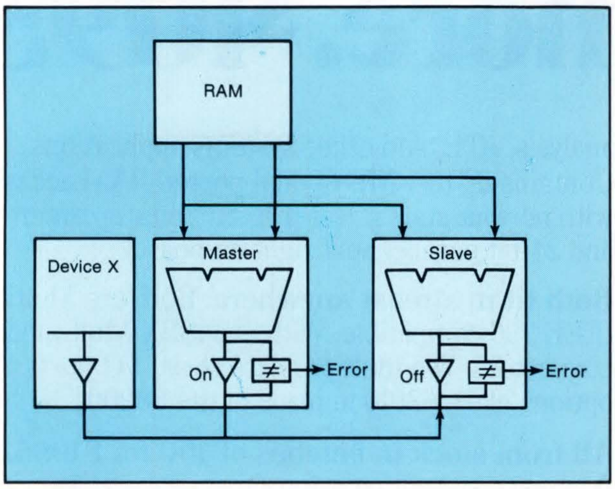
borrowing. For all subtract operations it provides the convenience of using borrowing instead of carrying by asserting the borrow pin. In this mode the carry flag is updated with the true Borrow. To allow efficient execution of macroinstructions the chip contains a Macro mode pin. When the chip asserts this pin, it allows the external Macro-Carry and Macro-Link bits instead of their microcounterparts to participate in the operation.

Instructions that execute algorithms for the multiplication and division of signed and unsigned integers are multiple cycles are also provided. For multiplication, the circuit supports the modified Booth algorithm, yielding two product bits in one cycle. Both single-precision and multiprecision division of signed and unsigned integers are supported at the rate of one quotient bit in every cycle.

Besides binary integers the instruction set provides basic arithmetic operations for binary-coded decimal (BCD) numbers. By operating directly on the decimal numbers created in most business applications, significant processing time is saved by eliminating the need to convert from binary to BCD and vice versa. Also, the round-off errors involved in converting from one base to the other are eliminated.

The last group of instructions was created to support variable-length bit fields (1 to 32) and single-bit operands. The position and width of the field can be specified by either the position and width inputs or by fields in the status register, thereby saving bits in the microcode. Most of the time, the position and width are determined dynamically. It is therefore difficult to supply them via the microinstructions. For single bit operations only the position specifier is needed.

Bit-manipulation instructions include setting, resetting, or extracting a single bit of the operand or the status register. Logical operations on either aligned or nonaligned fields in the two operands include OR, AND, NOT and XOR. In the case of nonaligned fields it is assumed that at least one of the fields is aligned to bit position 0. It is also possible to extract a field from one operand and insert it into another operand or extract a field across two operands.




**3. To help ensure system integrity, two Am29332 processors can be set for master and slave operation. Both chips perform the same operation in parallel, and any difference in their results is flagged as an error. The master also checks its internal result against the data on the output bus to make sure that no other device (such as device X) is turned on at the same time.**

### Enhancing system integrity

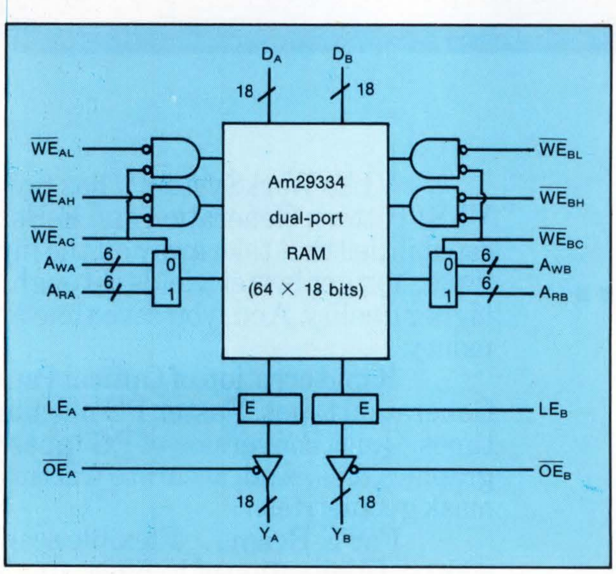
The growing need for data integrity has been addressed at both the system and the chip level by including hardware for fault detection. During calculations, byte-wide even parity is generated for the data result by the ALU and stored with the data in the external RAM. Byte-wide even parity is also checked at the ALU inputs and any error is flagged.

Even parity is specifically used to check for a floating TTL bus. Thus, all interchip connections are checked out. In addition, hardware for functional verification is also provided on the sequencer and the ALU functional verification can be implemented by using two similar devices in the master and slave mode (Fig. 3). In that setup, both chips perform the same operation, with any difference in their outputs being flagged as an error. The slave-mode chip's bidirectional buses operate in their input mode, allowing the master to compare its own internal result with that of the slave on every cycle. Additionally, the master checks the output bus to

## Microprogrammable 32-bit chips

make sure that no other device is turned on at the same time.

As mentioned earlier, the ALU architecture was designed to use an external register file. Keeping the file external to the chip permits the user to expand it to meet any system need. The Am29334, a high-speed 64-word-by-18-bit dual-access RAM, provides two independent data input ports and two independent data output ports (Fig. 4). Each port can be read from or written to using the separate inputs and outputs. The two accesses are independent except for the case when simultaneous write operations are done to the same word—in which case the result is undefined. The read address inputs and the write address inputs of each side are separate in order to save the cost and time delay of external multiplexing between a read address and a write address.




**4. The dual-access RAM serves as an external register file for the arithmetic processor chip. The Am29334 holds 64 words, each 18 bits long. Two chips are often connected to build a RAM block with four data outputs, two data inputs, and six address lines. Each port of the RAM can be independently accessed to read or write.**

The word width of 18 bits allows the RAM to store two bytes plus a parity bit for each. Each side has separate write enable for the lower and upper nine-bit bytes and a common write enable that also switches the address multiplexer. The actual write is delayed internally to allow the write address to set up internally before writing starts.

It is possible to build a RAM with four data outputs, two data inputs and six addresses by using two dual-access RAMs and on each side connecting the data input, write address and write enables of one RAM in parallel with the corresponding inputs of the other RAM. This expanded RAM may be used in concurrent processing applications in which an ALU and an adder (which generates the address) do their computations—this yields a result and an address in parallel. The two values can then be fed simultaneously to the multiport memory.

### The sequencer controls the show

The cycle time of the microprogrammed system is dependent on both the control path (i.e., sequencer and microprogram memory) and the data path (i.e., register file and ALU). Traditionally, the system bottleneck has been the control path, especially the ciritical paths associated with conditional branching. Special care has been taken in the design of the Am29300 family to balance control and data-path timing.

A key device contributing to the improved control-path timing is the Am29331 16-bit microprogram sequencer. It is designed for high speed, and that speed has been attained by the elimination of functions that would slow down the microaddress selection and by including the test logic and the test multiplexer in the sequencer (Fig. 5). As in most previous generation sequencers, the address register, the incrementer, the address multiplexer, the stack, and the counter are standard functions. The sequencer has multiway branch instructions that allow 1 of 16 consecutive addresses to be selected as the branch target in a single cycle.

The address register in most other sequencers is called a program counter, but this name is not correct if a strict definition is applied. In

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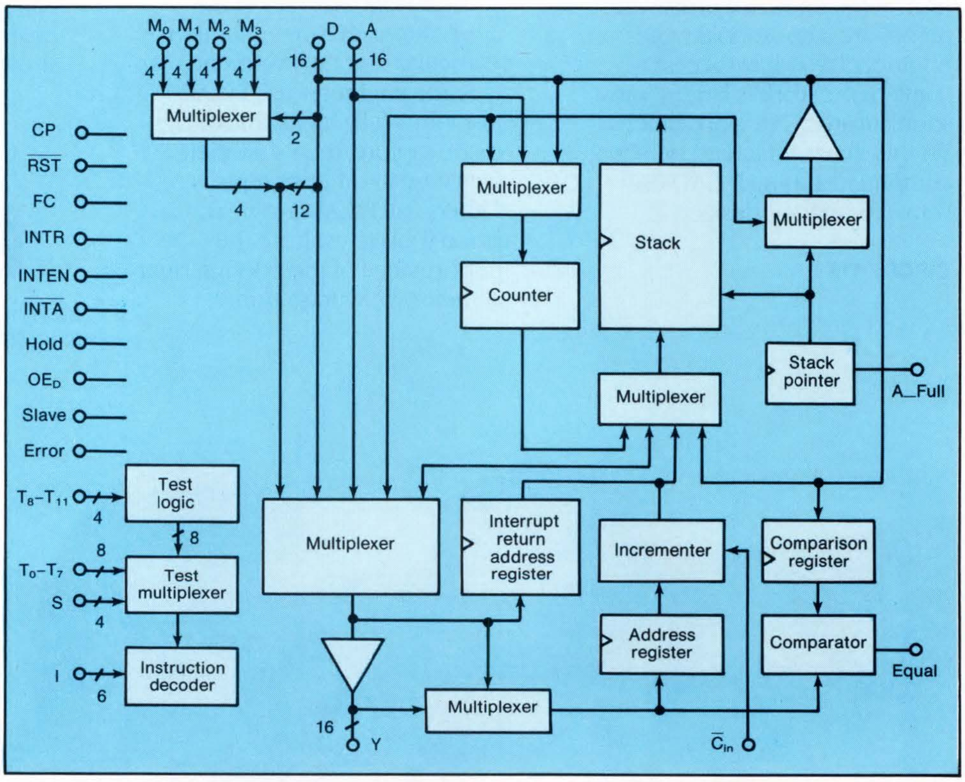
the Am29331, the incrementing counter is placed after the address register, which thus allows for the handling of traps. The stack stores return addresses, loop addresses and loop counts. It has 33 levels to permit the deep nesting of subroutines, loops and interrupts. An output, Almost Full (A-Full), indicates when 28 or more of the levels are in use.

Available for use in iterative loops, the counter can be loaded with an iteration count at the beginning of a loop, and the count is tested and then decremented at the end of the loop. The loop is terminated if the count is equal to one; otherwise a jump to the beginning of the loop is executed.

There are three buses that carry microaddresses. The bidirectional D bus can be connected to the pipeline register, providing branch addresses or loop counts, or used for two-way communication with the data processing part of the system. The A bus, called an alternate bus, can be connected to a mapping PROM to provide starting microaddresses for instructions in a computer. The Y bus sends out




**5. To aid in handling trap operations, the incrementer is placed after the address register in the Am29331 microsequencer. Additionally, the chip has a 16-bit address bus, which enables it to access up to 64 kwords of control memory and handle interrupts and multiple-path branches.**

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selected microaddresses to the microprogram memory and accepts interrupt or trap addresses if interrupt or trap is employed.

Four sets of 4-bit multiway inputs provide a simultaneous test capability of up to 4 bits. And, one way to use those inputs would be to decode mode bits in changing positions in macroinstructions. The four select lines select 1 of 16 tests to be used in conditional instructions. There are twelve test inputs. Four of these may be used for C (Carry), N (Negative), V (Overflow) and Z (Zero), generating internally the tests C+Z, $\overline{C}$ + Z, N XOR V, and N XOR V+Z, which are used for comparison of signed and unsigned numbers.

Relative addressing was the only somewhat useful function that was removed in order to maximize speed. The sequencer supports interrupts and traps with single-level pipelining, but may also be used with two levels of pipelining in the control path. It has a 16-bit-wide address path and cannot be cascaded, which thus limits the addressable memory depth to 64 kwords of microcode. That, however, is sufficient for the vast majority of applications—a typical computer, for instance, that has a microprogrammed instruction set, might use only about 1 to 2 kwords. However, for systems in which the microprogram is the sole program level, its size is generally larger.

#### Microprogram interrupts supported

The Am29331 sequencer supports interrupts at the microprogram level. Like polling, interrupts handle asynchronous events. However, polling requires explicit tests in the microprogram for events, thus leading to long response times, lower throughput, and larger microprograms. Interrupts, on the other hand, have a response time equal to the cycle time of the system (approximately 80 ns), measured from the Interrupt Request input (INTR). The sequencer accepts interrupts at every microinstruction boundary when the Interrupt Enable input (INTEN) is asserted.

An actual interrupt turns off the Y bus driver and asserts the Interrupt Acknowledge output (INTA), which should be used to enable an external interrupt address onto the Y bus, thus driving the microprogram memory. The interrupt also causes the interrupt return address to be saved on the stack; this permits nested interrupts to be handled (Fig. 6).

The Am29331 is also the first sequencer that can handle traps. A trap is an unexpected situation caused by the current microinstruction, which must be handled before the microinstruction completes and changes the state of the system. An attempt to read a word from memory across a word boundary in a single cycle is an example of such a situation. When a trap occurs, the current microinstruction must be aborted and re-executed after the execution of a trap routine, which will take corrective measures.

Execution of a trap requires that the sequencer ignore the current microinstruction and push the trap return address—the address of the ignored microinstruction—on the stack. The trap address must be transferred onto the Y bus at the same time. All this can be accomplished by disabling the carry-in to the incrementer ($\overline{C}_{in}$) and asserting the Force Continue input (FC) and the Interrupt Request input (INTR).

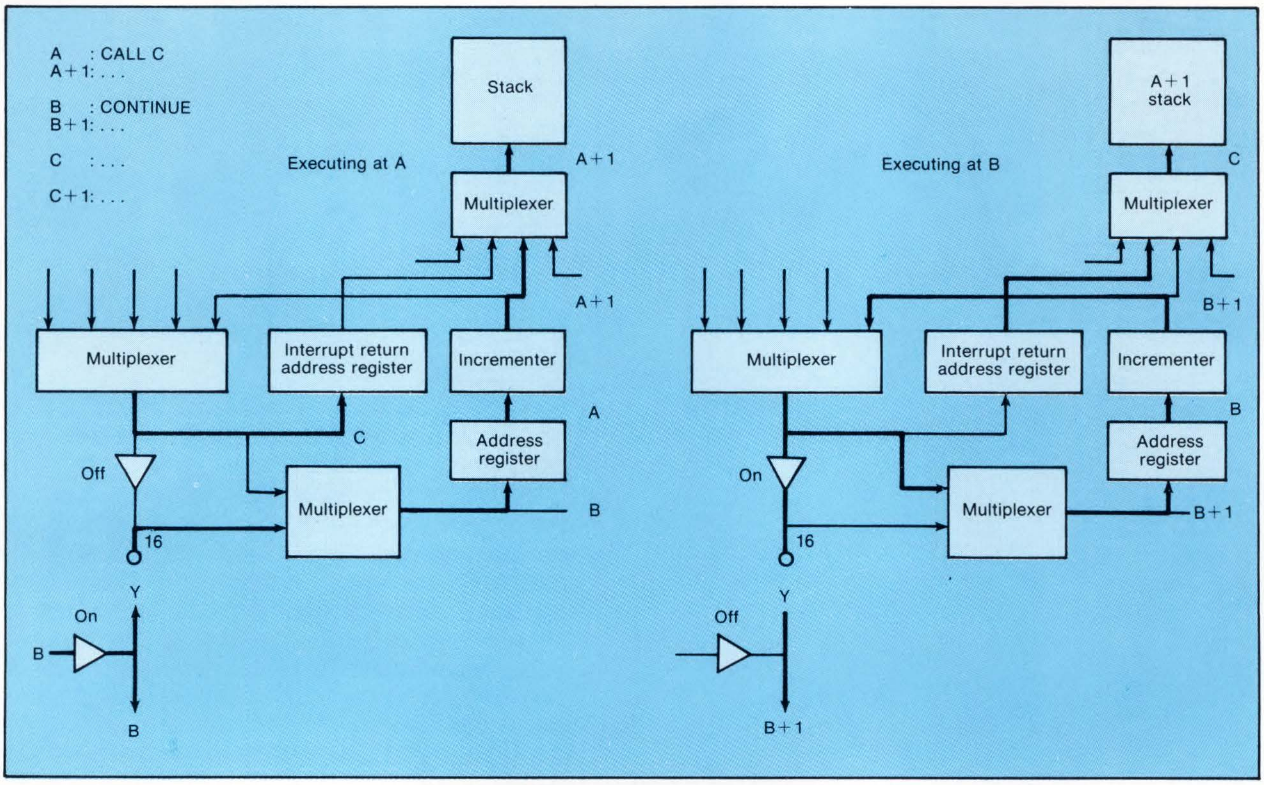
Also built into the sequencer is an address comparator, which allows detection of breakpoint in the microprogram. An output signal from the comparator indicates when the content of the comparator register is equal to the address on the Y bus. There is an instruction that loads the comparator register from the D bus and enables the comparator, which may later be disabled by another instruction.

Parallel microprocesses are useful when the system must deal with peripheral devices that are controlled at the microcode level. Normally only one processor is present and it must be time multiplexed between the concurrent operations that must be performed. When a process is suspended its private state must be saved, so that it can be restored when the process resumes execution. That, in turn, requires that the state of the sequencer be saved and restored, or each process must have its own sequencer that is active when the associated process is active. The first approach is the least expensive, but the second offers the advantage of shorter response time, because no time is spent on saving and restoring the state.

The Am29331 supports the first approach with its bidirectional D bus, through which the

entire state, with the exception of the comparator register, can be saved and restored. The sequencer also supports the multiple sequencer arrangement, in which the three-state Y buses from the sequencers are tied together driving a single microprogram memory. One of the sequencers is active, while the remaining sequencers are put on hold by asserting their Hold inputs. The Hold input disables most outputs (the D bus synchronously), disables the incrementer, and enables an internal Force Continue. This effectively detaches the sequencer from the system and preserves its state.

The sequencer has a 6-bit instruction input that is internally decoded to yield a set of 64 instructions. There are 16 basic branch instructions, each in an unconditional version, a conditional version, and a conditional version with complemented test. In addition there are 16 special instructions like Continue and Push C (push counter on stack). The branching instructions handle jumps, subroutines, various kinds of loops and exits out of loops, and FC actually overrides the instruction inputs with a continue




**6. Because it can accept interrupts at any microinstruction boundary, the sequencer responds faster than most other microprogrammed systems. For example, while the instruction at point A in memory is being executed, the sequencer is directed to point B. The only restriction on the programmer is that the first instruction of the interrupt routine cannot use the stack, since the interrupt return address is pushed onto it at the start of the procedure.**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The Am29331 is one of the few sequencers where the stack is accessible from outside through the bidirectional D bus. This indirectly allows access to the whole state of the sequencer except the comparator register. This is useful when testing the device, and during system debugging, in which, for example, the contents of the counter and the stack may be examined and altered. By including the troubleshooting instructions in the microcode, the sequencer may aid in debugging itself and the rest of the system. The access to the state is also useful for changing context or extending the stack outside.□

# Single-chip accelerators speed floating-point and binary computations

Complex multiplication or floating-point mathematical operations are frequently needed in most computer systems, but in many cases, not often enough to warrant the added cost of dedicating CPU hardware to the computational job. To speed up the calculations, many systems, though, allow for accelerator boards or boxes that can perform such operations at several megahertz speeds or more.

Already, many silicon designers have developed chips to simplify the design of such subsystems—16-bit parallel multipliers fabricated in bipolar, CMOS or NMOS processes, and single-chip or multichip floating-point processors made with CMOS or NMOS have been available for some time. However, they are low-performance solutions to the problem, or in some cases, have limited application since they are intended for highly pipelined systems.

Now, the ability to handle 32-bit binary multiplication or 32-bit floating-point multiplication, addition or subtraction can be added to a system with just a single chip. The Am29323 is a 32-bit parallel multiplier that accepts two 32-bit inputs and can deliver a 64-bit product in a single clock cycle of 80 ns. Alternatively, performing floating-point operations, the Am29325 accepts two 32-bit inputs and delivers a 32-bit result in less than 125 ns. It can operate with numbers represented in either the IEEE (P754) or Digital Equipment Corp. floating-point formats and can convert numbers from one format into the other.

Both chips are part of the just unveiled Am29300 series of 32-bit computational elements (Design Entry, p. 230). The multiplier is ideal for computer systems that do floating-point operations only infrequently but must often perform high-speed integer calculations such as those required in image manipulation. The floating-point processor enhances systems used for fast Fourier transform and scientific calculations. Systems could even contain both accelerators if a high-performance, general-

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purpose system were built (Fig. 1).

To speed the flow of data into and out of the chips, both circuits were designed with two 32-bit-wide input ports and one 32-bit output port. But the similarities end there, since the chips perform vastly different operations on the data. A fairly straightforward design, the multiplier uses a full Booth-encoded array to deliver a 64-bit product to the output register (Fig. 2). The output register feeds a multiplexer that sends the result, 32 bits at a time, to the output port.

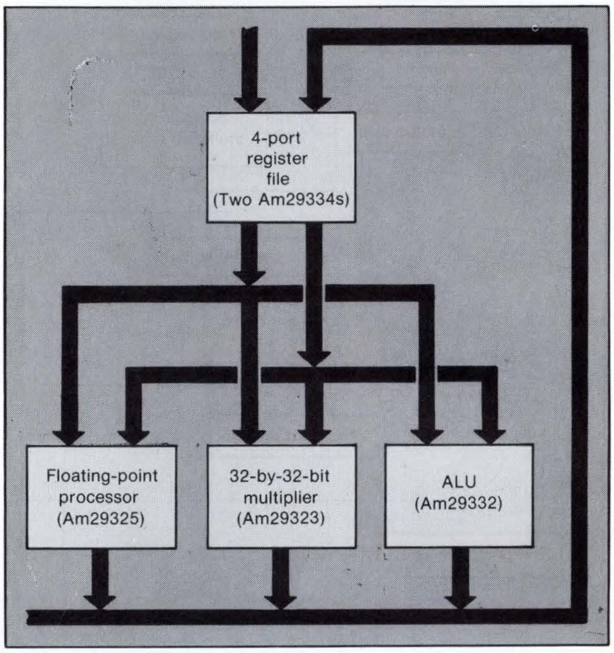
Double-precision operations can be done thanks to dual 32-bit input registers that are multiplexed into the multiplier array. A 67-bit partial-product adder allows new products to be summed with the contents of the output register. During this operation, the contents of the output register may be scaled by 32 bits, if necessary. Four partial products are formed and summed, and a temporary register assists in the scheduling of output transfers. The effective pipelining throughput in the double-precision mode is one 64-bit multiplication every four cycles. The accumulator can also support 96- and 128-bit multiplications. However, for such operations, input data must be repeatedly applied.

The input and output registers of the multiplier have independent control signals so that they can be optimally timed in pipelined systems. However, in unpipelined systems, the registers can independently be made "transparent" so that data encounters no delays when entering or leaving the chip. Like the other chips in the Am29300 family, the multiplier has parity checking and generating circuits to ensure system data integrity. And, the circuit offers a slave mode in addition to its normal mode—if two chips are tied together to operate in parallel with one set to operate in the slave mode, the circuits will generate an error flag if unequal results are obtained.

In the world of floating-point computations, several single-chip units, designed to be general-purpose math coprocessors for microprocessor systems have achieved close to microsecond operating speeds. However, to achieve higher throughput rates, several recently announced two-chip sets have cut that speed by a factor of 10, achieving data throughput rates of 10 MHz for pipelined operations. But, if operated in nonpipelined systems, these chips lose considerable speed—often by a factor or two or three—since data must ripple through the stages of pipeline registers.

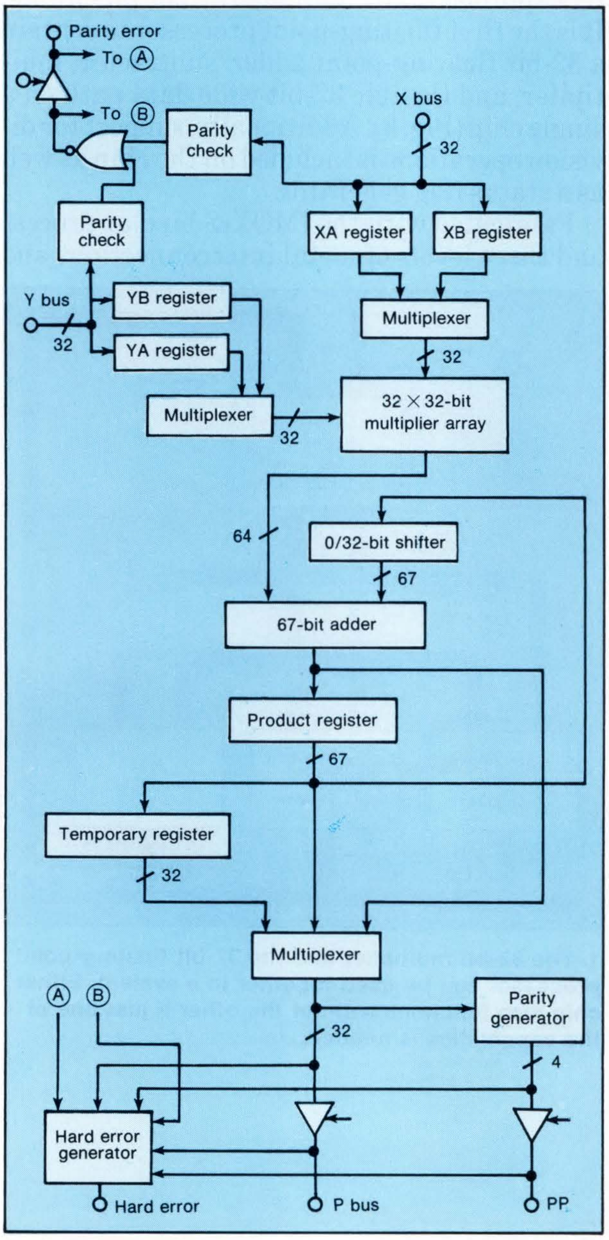
To cut the data delays, the Am29325 took a direct approach and eliminated all the pipelining. It is the first floating-point processor to contain a 32-bit floating-point adder/subtractor, multiplier, and flexible 32-bit wide data path on a single chip (Fig. 3). Additionally, support for division operations is included on the chip as well as a status flag generator.

Fabricated with the IMOX-S bipolar process and three levels of metal interconnections and




**1. The 32-bit multiplier and the 32-bit floating-point processor can be used together in a system. Either chip also functions without the other if just one of the capabilities is needed.**

housed in a 144-lead pin-grid-array package, the Am29325 can replace one to two boards of SSI and MSI logic typically used in general-purpose computers, array processors and graphics engines, to provide high-speed floating-point math capability. When used in concert, the on-chip functions will meet the computational and data-routing needs of these and many other applications.




**2. Surrounding the 32-by-32-bit multiplier array on the Am29323 are multipliers for the two 32-bit input buses, which permit 64-bit multiplications to be done in just four cycles. The multiplier checks parity on the input data and generates parity bits for the output result.**

Integrating these functions into a single device greatly reduces data routing problems and minimizes processing overhead that would otherwise be incurred when shuffling data on and off the chip. The internal data path is ideally suited for multiplication and accumulation, Newton-Raphson division, polynomial evaluation, and other often-used arithmetic sequences. Placing the data path on chip also dramatically reduces the number of ICs needed to interface the device to the rest of the system.

The three-port floating-point arithmetic unit at the chip's core can perform any of eight instructions in a single clock cycle. The absence of pipeline delay in the arithmetic unit means that the result of an operation is available for use as an input operand in the very next operation, a crucial feature when performing algorithms with tight feedback loops. Instructions and other operating modes are selected with dedicated input signals, an approach ideally suited to microprogrammed environments. The device easily interfaces with a variety of 16- and 32-bit systems using one of three programmable bus modes.

### Delving into the operation

At the heart of the arithmetic unit are a high-speed adder-subtracter, a 24-by-24-bit multiplier, an exponent processor, and other logic needed to implement the floating-point operations. Two input ports, R and S, provide operands for the instruction to be performed; the result appears on port F. One of eight instructions is selected by placing a 3-bit code on lines $I_0$, $I_1$, and $I_2$. The first three instructions—$R + S$, $R - S$, and $R \times S$—operate on both input operands; the remaining instructions need only one input operand.

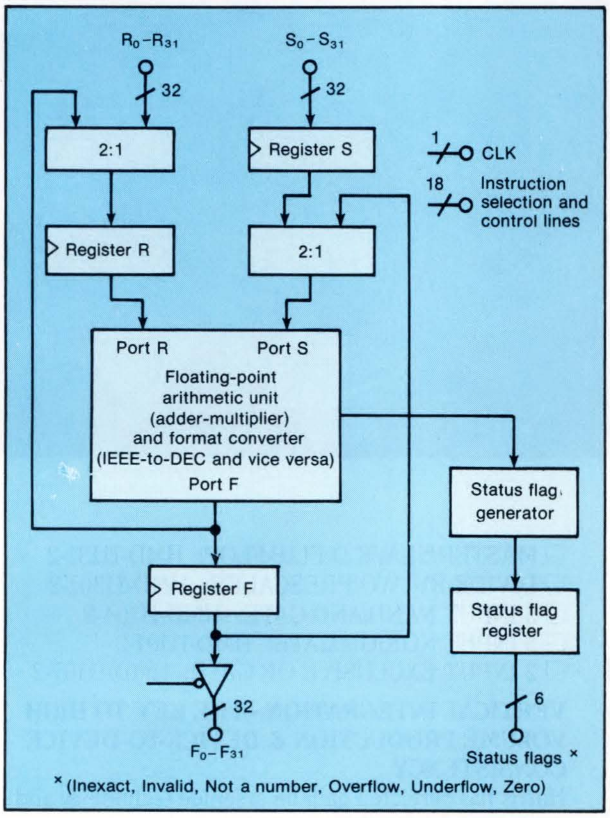
The fourth instruction, $2 - S$, forms the core of the Newton-Raphson division algorithm, in which the quotient A/B is calculated by first evaluating 1/B, then postmultiplying by A. The reciprocal value 1/B is derived by using an external lookup table to provide an approximation of 1/B; this approximation is refined using the iterative equation:

$$x_n = x_{n-1}(2 - Bx_{n-1}),$$



where $x_n$ is the nth approximation of 1/B.

Once B and the approximation of 1/B are loaded into the Am29325, the approximation is refined using a sequence of R × S and 2 − S instructions; no additional I/O operations are needed for reciprocal refinement. The remaining four instructions perform data format conversions. Instruction INT to FP converts a 32-bit, two's complement integer to floating-point form, useful when processing data initially generated in fixed-point format; conversion from floating point to integer format is handled by instruction FP to INT. Two other instructions convert between IEEE and DEC floating-point formats.




**3. Also using separate 32-bit buses for the inputs and output, the AM29325 floating-point processor handles either IEEE or DEC formatted data and can translate between formats, if necessary.**

The arithmetic unit recognizes two single-precision floating-point formats—the IEEE format as specified in proposed standard P754, draft 10.0, or the DEC format used in VAX minicomputers. The eight instructions can be performed using either format; the desired format is selected with the IEEE/DEC pin on the processor chip. The formats are broadly similar—each has an 8-bit biased exponent, a 24-bit significand comprising a 23-bit mantissa appended to an implied or "hidden" most-significant bit (MSB), and a sign bit.

There are, however, a number of subtle differences. The IEEE format has an exponent bias of 127 and a binary point placed to the right of the hidden bit, while the DEC format has an exponent bias of 128 and a binary point placed to the left of the hidden bit—these variances result in a slightly different range of representable values. Each format has its own set of operands reserved for special uses. The IEEE format reserves operands to represent non-numerical values (referred to as Not a Number, or NaN), $+\infty$, $-\infty$, and plus and minus 0; the DEC format reserves only two types of operands to represent non-numerical values and 0. In addition to format differences, there are a number of minor differences in the manner in which operands are handled during the course of a calculation. These differences are automatically accounted for when the desired format is selected.

### The need for rounding

When performing a floating-point operation, it is sometimes possible to generate a result whose value cannot be precisely expressed as a floating-point number. If, for example, the single-precision floating-point values $2^{23}$ and $2^{-1}$ are added, the infinitely precise result, $2^{23} + 2^{-1}$, cannot be represented exactly in the single-precision floating-point format. Some means, then, must be provided for mapping the infinitely precise result of a calculation to a representable floating point value. The arithmetic unit implements four IEEE-mandated

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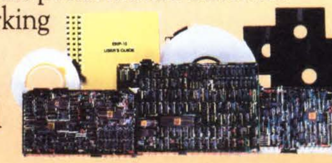

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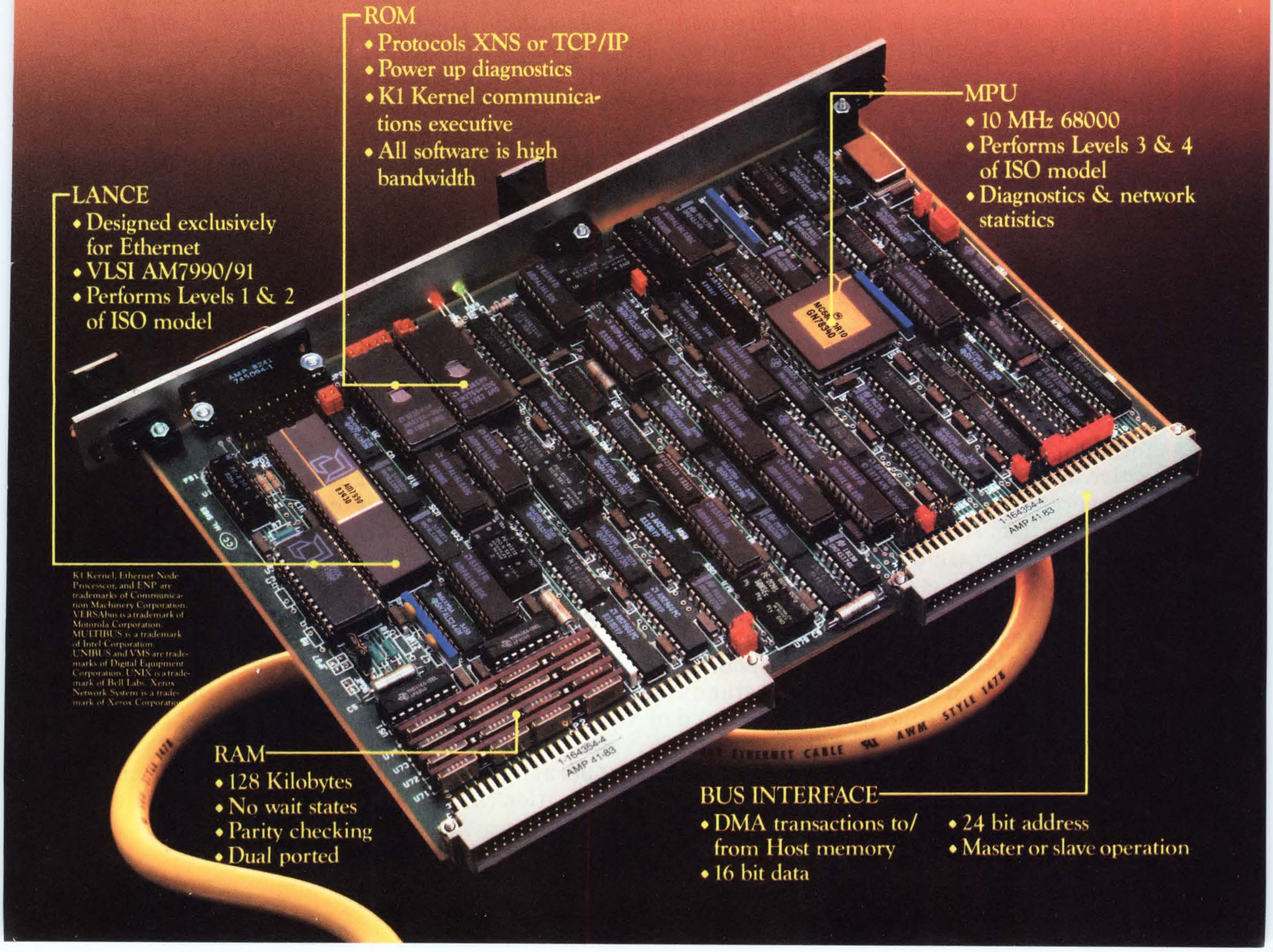

rounding modes to afford the user some flexibility when performing this mapping; the desired rounding mode is selected with signals $RND_0$-$RND_1$.

Of the four modes, the round-to-even mode is most often used; it maps the infinitely precise result of an operation to the closest representable floating-point value. The round-toward $-\infty$ mode maps to the nearest representable value less than or equal to the infinitely precise result; similarly, the round to $+\infty$ mode maps to the nearest value greater than or equal to the infinitely precise result. A fourth mode, Round toward zero, maps to the closest representation whose magnitude is less than or equal to that of the infinitely precise result. As one would expect, if the infinitely precise result of an operation is representable in the floating-point format, it passes through the rounding operating unchanged, regardless of rounding mode.

As the result of an operation, various status flags are set or reset by the status flag generator. Six flags are used to note the occurrence of overflow, underflow, zero, not-a-number, invalid, or inexact conditions. Because the flags are generated as the operation is performed, the user can greatly reduce processing overhead that would otherwise be needed to test the results of operations. The flags are fully decoded, minimizing the amount of hardware needed to interpret them.

### Flagging the status

Four of the status flags report exception conditions stipulated in IEEE standard P754. The Invalid flag indicates that an input operand or operands are invalid for the operation to be performed. The Underflow and Overflow flags are active when a result is too small or too large for the operation's destination format. The fourth exception flag, Inexact, tells the user that the result of an operation is not infinitely precise. Although these flags are primarily an adjunct to operation in the IEEE format, they also produce valid results when the DEC format is selected. The Am29325 generates two additional flags not provided for in the IEEE standard. Flags Zero and NaN identify zero-valued or nonnumerical results for both IEEE and DEC formats.

A floating-point processor whose arithmetic unit performs millions of operations per second can maintain that operating speed only if the correct operands can be routed to the arithmetic unit at that rate; if not, the specification is meaningless. To meet this crucial requirement, the core of the Am29325 is supported by a 32-bit data path comprising two input buses, a three-state output bus, and two data feedback paths. These data paths give the user the means to get the operands to where they are needed without devouring extra clock cycles.

Data enters through input buses $R_0$-$R_{31}$ and $S_0$-$S_{31}$; results exit through three-state output bus $F_0$-$F_{31}$. Each bus has a 32-bit edge-triggered register for data storage; data is stored on the rising edge of common clock input, CLK. An independent clock enable is provided for each register, so that new data can be clocked in or old data held; the clock enables are well-suited to a microprogrammed environment, and make the gating of clocks, always a risky business, unnecessary. The ability to clock or hold any register is a powerful tool for performing algorithms with conditional operations, or algorithms in which intermediate results must be delayed for one or more cycles before reentering the calculation.

In many applications,the internal registers will be used to store input and output operands; it is in this register-to-register mode that the chip shows its top speed. Some users, however, may wish to bypass one or more of the internal registers. The input and output registers can be made transparent independently using feedthrough controls FT0 and FT1. If all three registers are made transparent the device operates in a purely combinatorial "flow-through" mode. That mode, through, is somewhat slower than the register-to-register mode, but is useful in systems that need a register structure substantially different from that provided in the Am29325, or in systems where floating point operations must be concatenated with other combinatorial functions.

The two feedback data paths greatly simplify the task of moving data from one calculation to the next. One path routes data from the output of the arithmetic unit to a multiplexer at the input of register R; the multiplexer selects the operation result or $R_0$-$R_{31}$. The result of any operation can therefore be loaded into register


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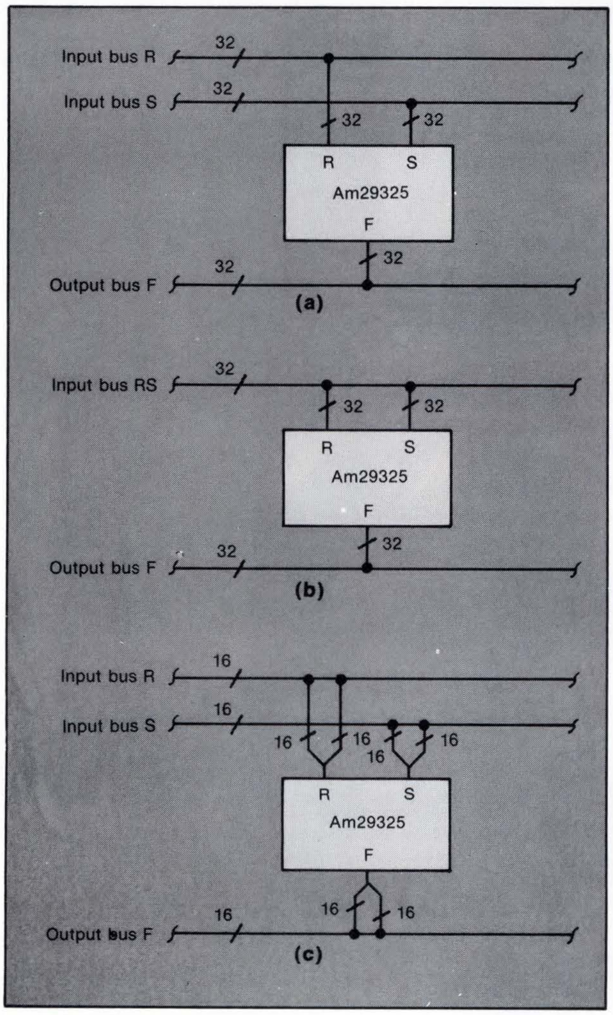
## 32-bit math accelerators

R, register F, or both. The second path feeds the output of register F to a multiplexer at the arithmetic unit's S port; the multiplexer selects either register S or register F as the port S input. This path effectively increases the number of commands—instruction R Plus S, for example, can also be performed as R Plus F.




**4. Three programmable I/O bus modes permit the floating-point processor to operate with dual 32-bit input buses (a), a single, shared 32-bit input bus (b), or even two 16-bit buses (c) so that it can easily connect to most 16-bit microprocessor systems.**

Thanks to the inclusion of three programmable I/O modes, the circuit readily interfaces with both 16- and 32-bit sytems. The most straightforward of these options is the 32-bit, two-input bus mode (Fig. 4a). The advantage of this mode is its high I/O bandwidth—no multiplexing of I/O buses is required, thus improving system speed and easing critical timing constraints. R and S operands are taken from their respective buses and clocked into the R and S registers on the rising edge of CLK; register F is also clocked on this transition.

Another choice sets up a 32-bit, single-input bus, in which both the R and S buses are connected to a single input bus (Fig. 4b). The R and S operands are multiplexed onto this bus by the host system; the R register clocks its operand on the rising edge of CLK, the S register on the falling edge. The S operand is double-buffered on chip, so that the new S operand is presented to the arithmetic unit on the rising edge of CLK. Operation of register F and the F bus is the same as in the 32-bit, two-input bus mode.

The last option has targeted 16-bit systems—a 16-bit, two-input bus mode (Fig. 4c). In this mode the R, S, and F buses are 16 bits wide; 32-bit operands are placed on the buses by time-multiplexing the 16 MSBs and LSBs of each data word. The LSBs of the R and S operands are double-buffered on chip, so that the complete 32-bit operands are presented to the arithmetic unit on the rising edge of CLK. Internal data paths and registers remain 32 bits wide, thus giving the 16-bit system designer the benefits of the simple interface and the speed of the wide internal data paths.

### Putting the part through its paces

Multiplication and accumulation—a combination of operations very commonly used in digital filtering, image processing, matrix manipulation, and many other applications—can readily show the capability of the floating-point processor. In such a combination of operations, N input terms $x_i$ are multiplied by constants $k_i$; the products are then added, producing the weighted sum:

$$s = \sum_{i=0}^{N-1} k_i \; x_i$$

To do this with the Am29325 is a simple two-step process, with two additional steps for ini-

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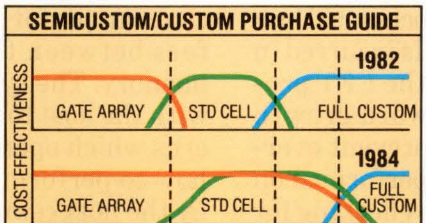


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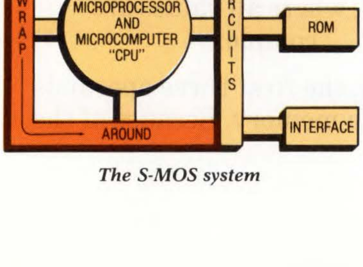


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tialization. In the first step data and coefficient values $x_0$ and $k_0$ are clocked into registers R and S. During step two the values $x_0$ and $k_0$ are multiplied and the product placed in register F; at the same time, data and coefficient values $x_1$ and $k_1$ are clocked into R and S. Third, values $x_1$ and $k_1$ are multiplied and the product placed in R. In step four, products $x_1k_1$ and $x_0k_0$ are added and the sum placed in F, and $x_2$ and $k_2$ are clocked into R and S.

The third and fourth steps are then repeated for as many iterations as needed to complete the operation. Once the part has been loaded with the first two sets of operands, the internal data path routes partial results to keep the arithmetic unit busy with a multiplication or addition every clock cycle; a new multiplication and accumulation is performed every two clock cycles. The partial results remain on-chip until the multiplication and accumulation is completed, thus eliminating I/O delays and the more complex programming that would result from having the adder and multiplier on separate chips.

### Some real applications

A more specific application for the Am29325 could be its use as the computational engine in a fast Fourier transform (FFT) processor. During a FFT operation, word growth is incurred in the butterfly calculation, and if the FFT processor uses integer arithmetic, word growth can cause a system overflow. To prevent overflow, a scaling operation must be performed on the data. The overhead involved in checking for word growth overflow and scaling of data can be avoided by using floating-point arithmetic. Floating-point provides not only greater dynamic range but in most cases also provides greater precision (24 bits of significance versus 16 bits in a typical integer system).

A powerful, low-cost system that executes FFTs can be built around the floating-point processor (Fig. 5). It consists of a floating-point arithmetic processing unit, a data and coefficient address generator, a data and address storage block, high-speed data and coefficient memories, a system controller, clock generator, and host interface. Input operands to the R port are fed from the data store, while data to the S port is fed from the coefficient memory. The result of an arithmetic operation may be stored back in the data memory. An exclusive-OR gate is also available to complement the sign of the result, effectively multiplying the operand on the F bus by −1. For most operations, intermediate results can be held within temporary registers in the floating-point unit; only the final result need be sent off chip.

The high-speed data memory is made up of RAMs, the coefficient memory of PROMs. The data memory can be loaded with data from the host or can store results that have been processed through the floating-point chip. Once all data or results have been stored, the data memory is ready for use in an operation, or for transfer back to the host system. The coefficient PROMs contains the sine and cosine data required for an FFT, while the data store holds frequently used operands.

During the calculation of a butterfly, the same operands must be used in several different cycles—and since the data store reduces the number of memory read operations required, it speeds up data access. As the butterfly sequence progresses, the appropriate address is available from the address store, which consists of two more multilevel pipelined registers.

The host interface consists of a DMA channel that can perform high-speed block data transfers between the host system and the data memory. The system controller communicates with the host to receive or transfer data. It governs which operations are to be performed and how to perform them. Instructions are issued by the host computer, via the host interface, to the system controller, and the system controller informs the host when the operation is done.

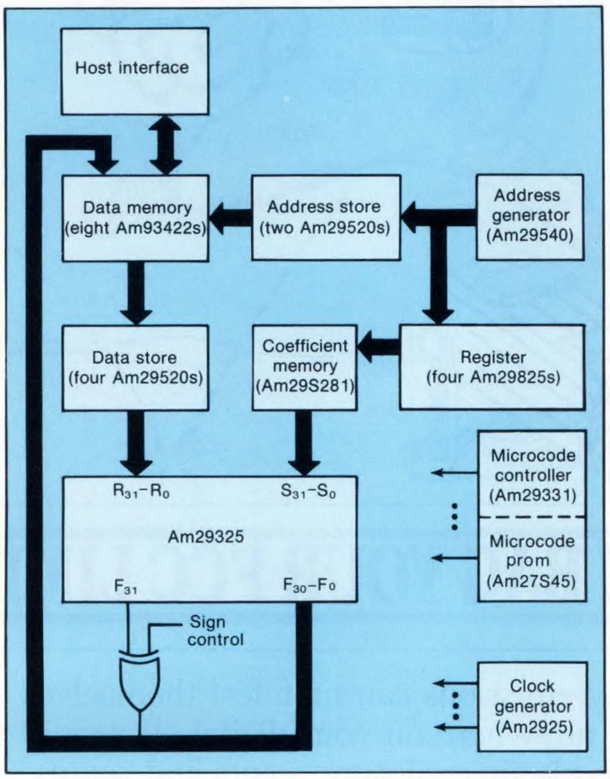
The system controller consists of an Am29331 or similar microsequencer, and a microcode program stored in registered PROMs. The system clock generator uses an Am2925. The architecture allows a ten-cycle butterfly FFT to be executed (see Fig. 5 again) using a radix-2 decimation-in-time (DIT) algorithm. The equations for a radix-2 DIT algorithm are:

$$A' = A + BW\ B'$$
$$B' = A - BW, \text{ where all values are complex}$$

In cycles 1, 2, and 3, the first three operands are read from the data memory. Because of the

overlapping butterflies, this read takes place while the previous butterfly is still being processed. In the following two cycles, data writes of the previous butterfly occur while the complex multiplications of (BW) are being performed. Cycle 6 reads in a new operand for the present butterfly and sums together the two products from the two previous cycles. In cycles 7 and 8, the real part of A′ and B′ is formed. In cycles 9 and 10, the real part of A′ and B′ is written to memory. Also, during these two cycles the other product pairs of (BW) are formed.

During cycles 11, 12, and 13, data for the next butterfly is read, and as part of cycles 12 and 13, the imaginary part of A′ and B′ is formed. In the following cycles the imaginary part of A′ and B′ is written to memory and processing of the next butterfly is initiated. The real and imaginary components of B′ have a negative sign, and can be corrected by complementing the sign. Counting the number of cycles from the first read or write of one butterfly to the next, it can be seen that a butterfly is computed every 10 cycles.




**5. To build a fast-Fourier transform processor that uses the floating-point processor as its heart requires only a few control chips and some memories. Use of the Am29540 and Am29332 LSI building blocks helps keep the circuitry simple.**

### The big system picture

Although the floating-point chip fits well in small systems, it is also easily incorporated in larger, more powerful configurations. In one such system, a high-speed, microprogrammed integer and floating-point processor can be readily tailored to implement signal processing, image processing, or graphics algorithms (Fig. 6). The processor consists of a two-level controller, data and coefficient memory, address generator, and arithmetic unit. These functional blocks are considerably more flexible than their counterparts in the simpler FFT system.

The controller is divided into two levels, or sections: program and microprogram. In the topmost or program section, an Am2910A microprogram controller addresses a program memory that contains high-level instructions, or macros. These macros implement building-block operations; a graphics processor, for example, might have macros called Translate and Rotate that move objects in three-dimensional space. Each macro would carry with it parameters relevant to its operation, such as memory pointers or iteration count.

The program section passes address-related parameters to the address generator, and passes the iteration count and the decoded microinstruction start address to the microprogram section of the controller; this section then provides cycle-by-cycle control of processor resources during the execution of a

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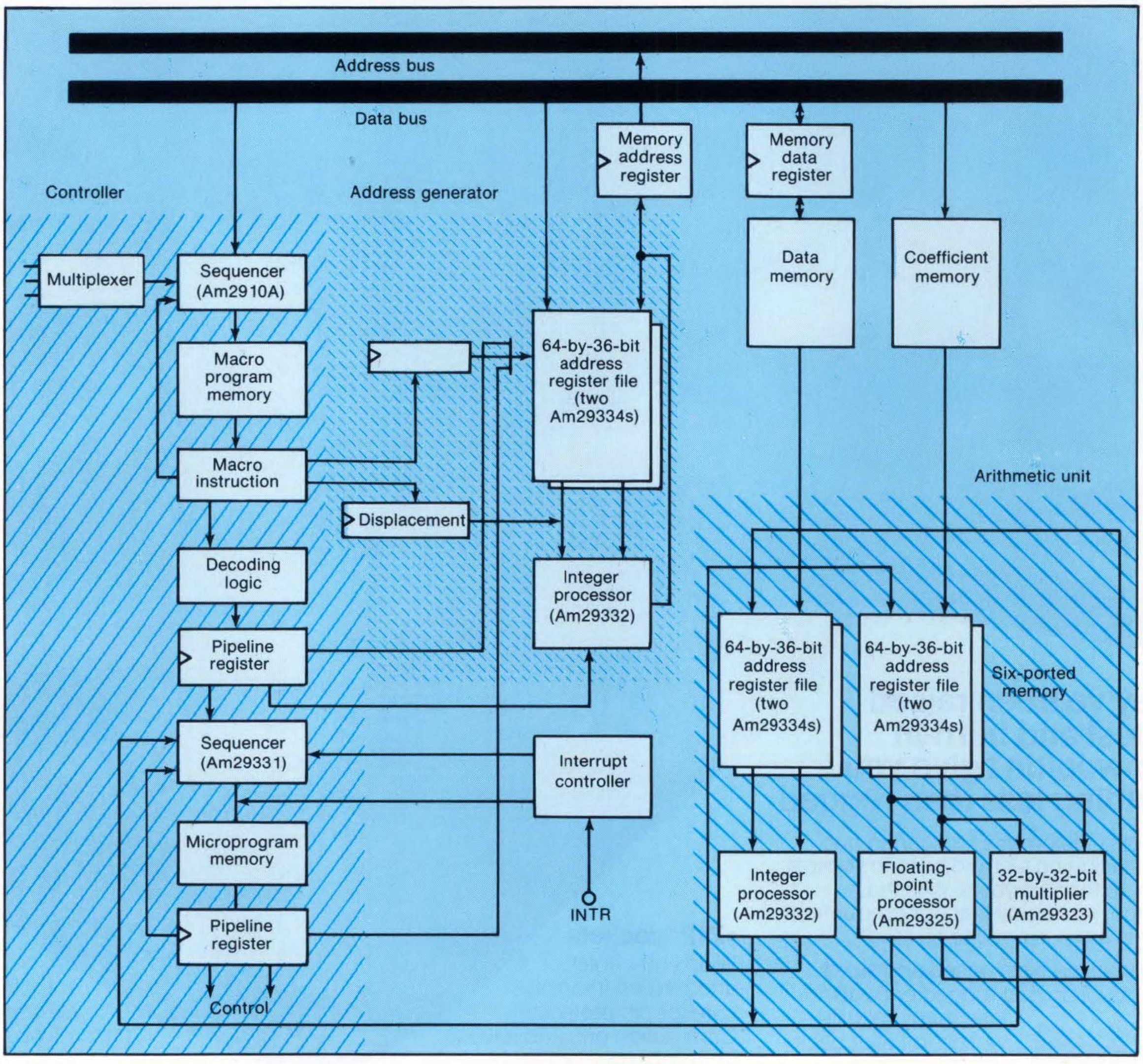
macro. The heart of the microprogam section is an Am29331 microprogram controller—it addresses a microcode memory, in which the microprogram sequence for each macro type is stored.

The microprogram controller was chosen for three reasons: first, it can address up to 64 kwords, which makes possible a deep microprogram memory that can store many operation sequences. Second, its high speed permits the use of slower, less expensive microprogram memory, a particularly important considera-




**6. A versatile, yet high-performance microprogrammable system can be built by including both the floating-point processor and the 32-bit multiplier into a system that uses the other Am29300 building blocks to form the control and address generation sections.**

**CIRCLE 128**

tion when the microprogram is large. And third, its micro-interrupt feature can be used to efficiently implement exception handling for arithmetic operations. By using interrupts for these exceptions, the overhead otherwise incurred in testing status flags can be greatly reduced.

The data and coefficient memories store input data, output data, and constants. In this application, data and coefficient memory have been separated from program memory. Sometimes referred to as a Harvard architecture, this approach increases throughput by allowing instruction fetch and operand fetch operations to proceed in parallel.

The address generator comprises a Am29332 ALU and two Am29334 register files. The register file stores up to sixty-four 32-bit base addresses and pointers. The Am29332 creates a 32-bit effective address from these bases and pointers, with the calculation assuming the forms:

base + pointer
base − pointer
base
or pointer

In addition, the Am29332 can perform mask, shift, and merge operations in a single cycle. This feature can be used to quickly calculate matrix addresses of the form:

$$a2^N + b,$$

where a and b are the row and column indices of the matrix element to be accessed. The combination of a 32-bit effective address and efficient matrix addressing makes this address generator particularly attractive for applications such as image processing, in which matrices must be plucked out of very large data arrays.

The arithmetic unit contains three arithmetic facilities—an Am29325 for floating-point operations, and the Am29332 and Am29323 for integer and logical operations. These devices accept data from a six-port register file made of four Am29334s. The register file has three purposes—it acts as a fast, temporary scratchpad for data, it routes data among arithmetic devices (the output of one arithmetic device can be written to the register file, and be used as an input operand by another such device during the following clock cycle), and it provides access to four data words every clock cycle, so that two or more arithmetic device can operate in parallel.

An example of this parallelism is integer multiplication-accumulation: because the Am29323 and the Am29332 receive operands independently, an integer product and sum can be calculated every clock cycle. The register file can then pass products from the Am29323 to the Am29332, for a throughput of one clock cycle per multiplication-accumulation.

Operation of the processor might be best understood by considering the execution of a typical macro. For graphics applications, one such macro is Translate, with which a set of points in three-dimensional space is moved in a given direction. The set of points is described by a list of vectors ($X_i$, $Y_i$, $Z_i$), while the translation is described by vector ($S_T$, $Y_T$, $Z_T$); each vector is stored in three contiguous data memory locations. Translation is performed by adding the translation vector to each entry in the vector list.

The translation process begins when the microprogram controllers encounters a Translate instruction in program memory. The Translate instruction is accompanied by three parameters: the start address of the translation vector, the start address of the vector list, and the number of vectors in the list. The first two parameters are passed to the address generator, the third to the iteration counter.

The microprogram section of the controller then assumes command, accessing the microcode for the Translate instruction. The microcode controls the address generator and arithmetic unit, specifying the operations needed to fetch each vector from the vector list, add the translation vector, and return the modified vector to the data memory. After all vectors in the list have been processed (as indicated by the iteration counter), control is returned to the Am2910A program sequencer, which then accesses the next macro from program memory. □

| **How useful?** | **Circle** |
|---|---|
| Immediate design application | 553 |
| Within the next year | 554 |
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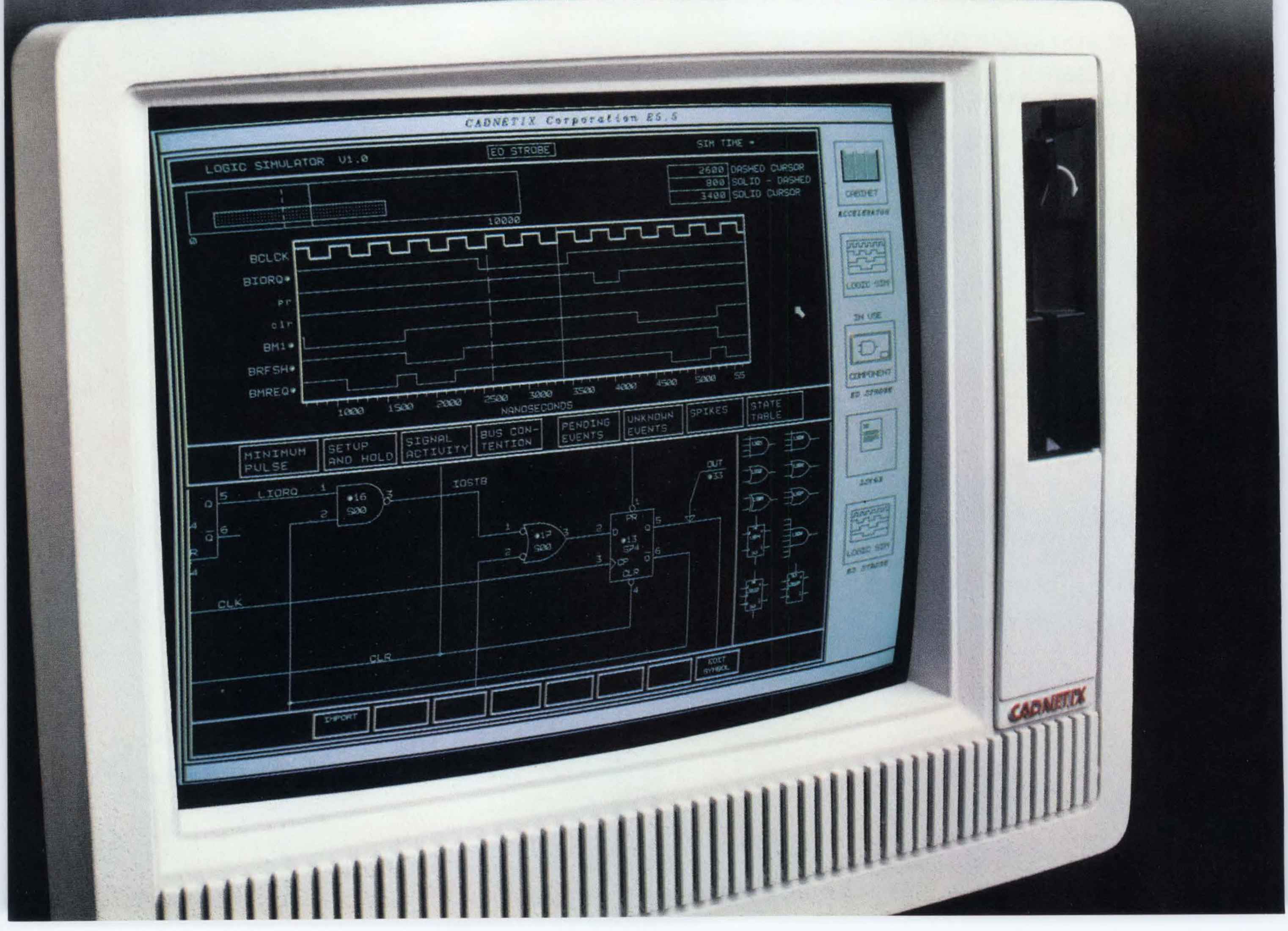

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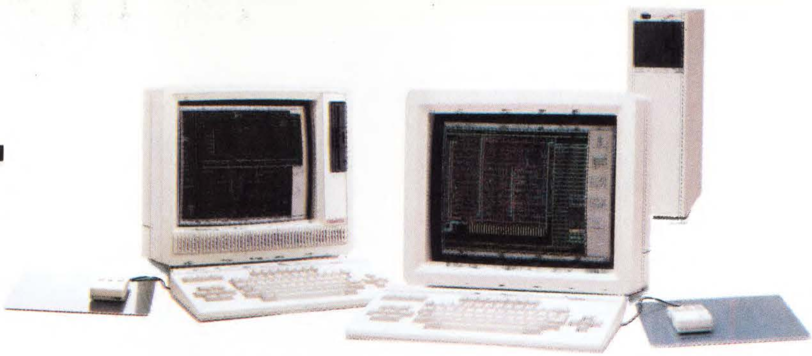

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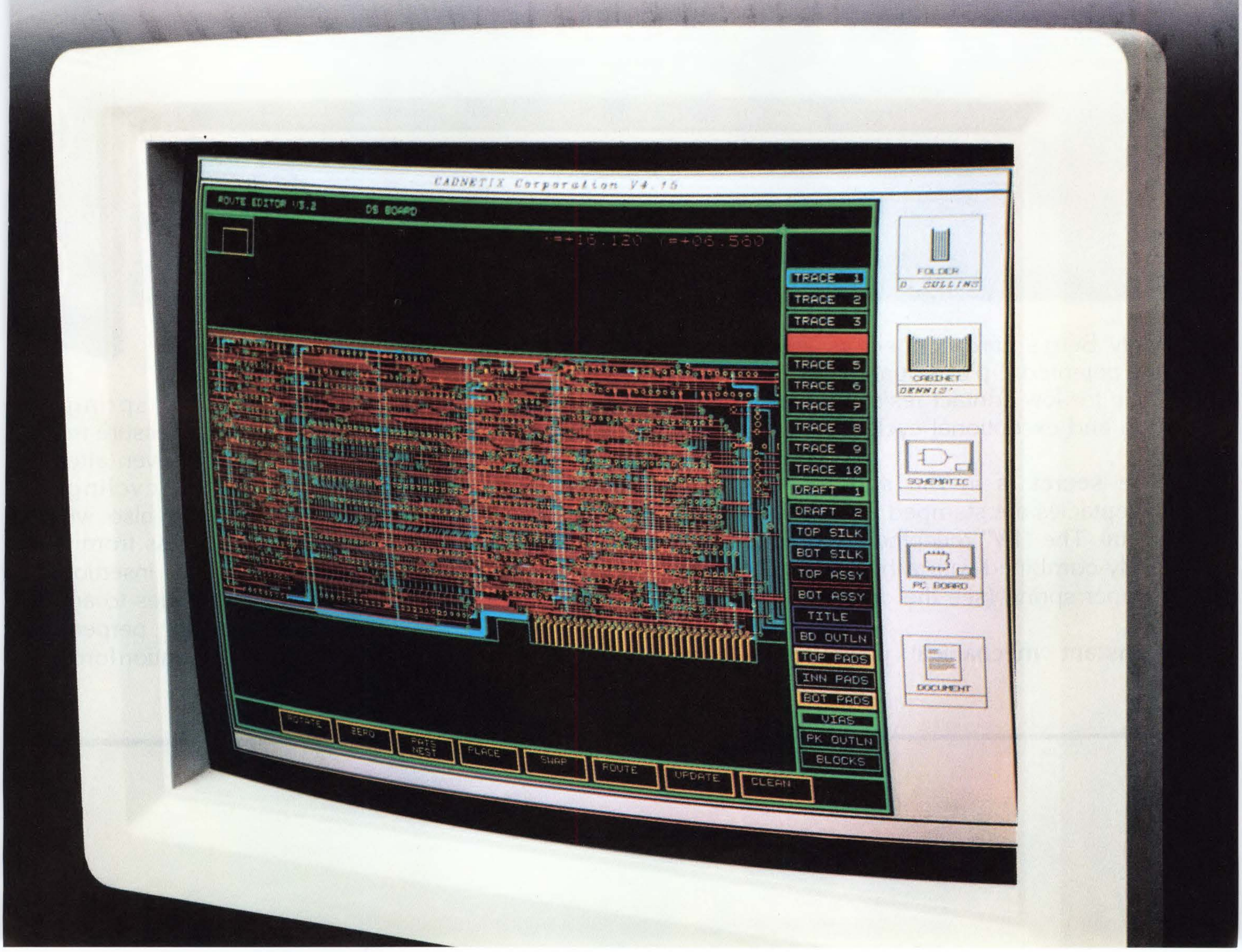

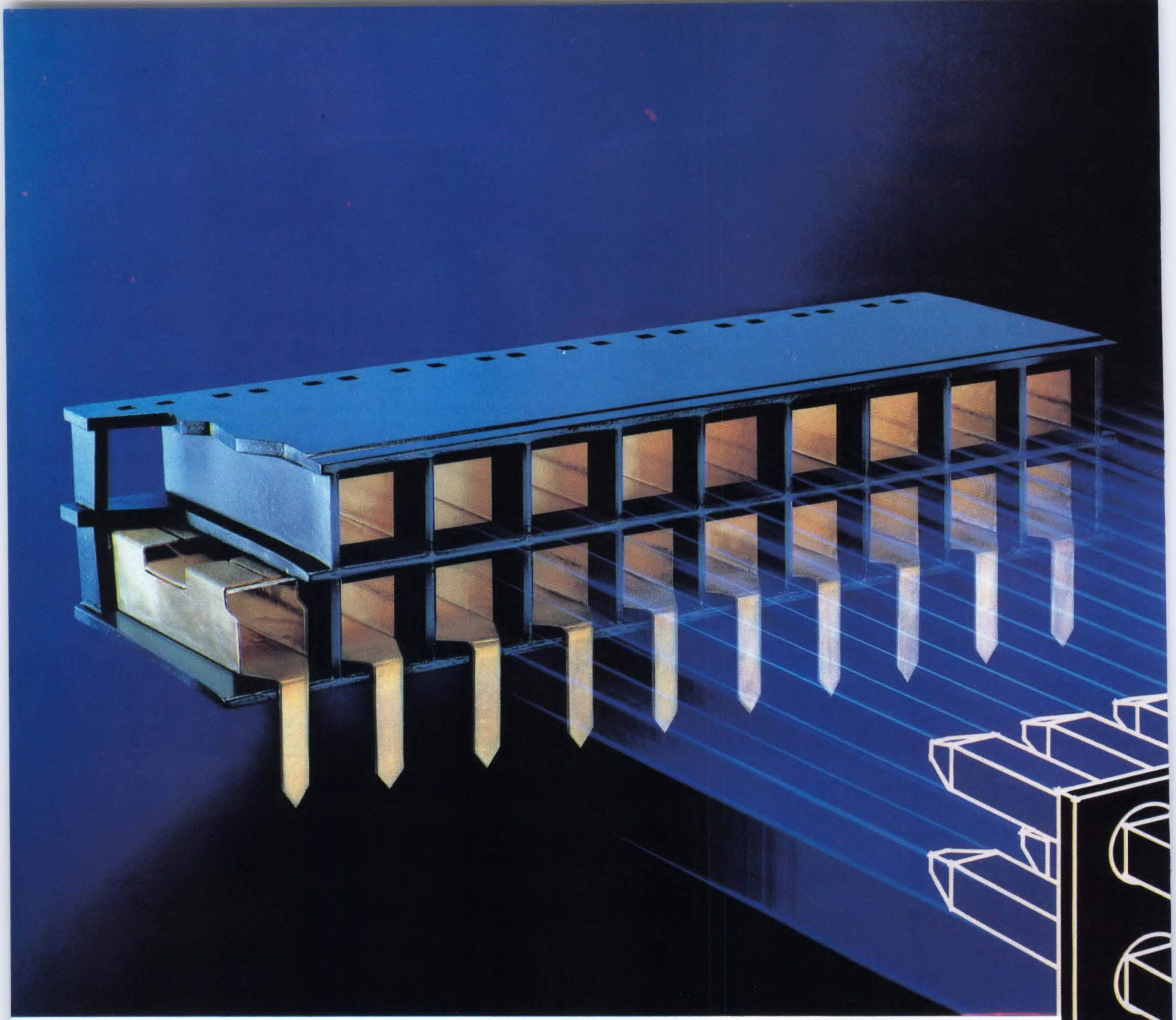

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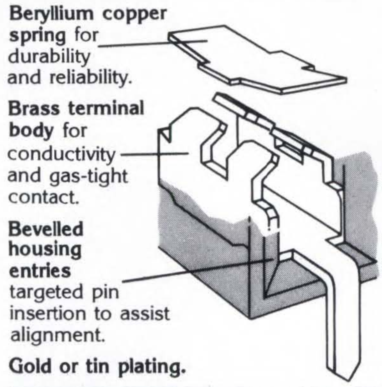


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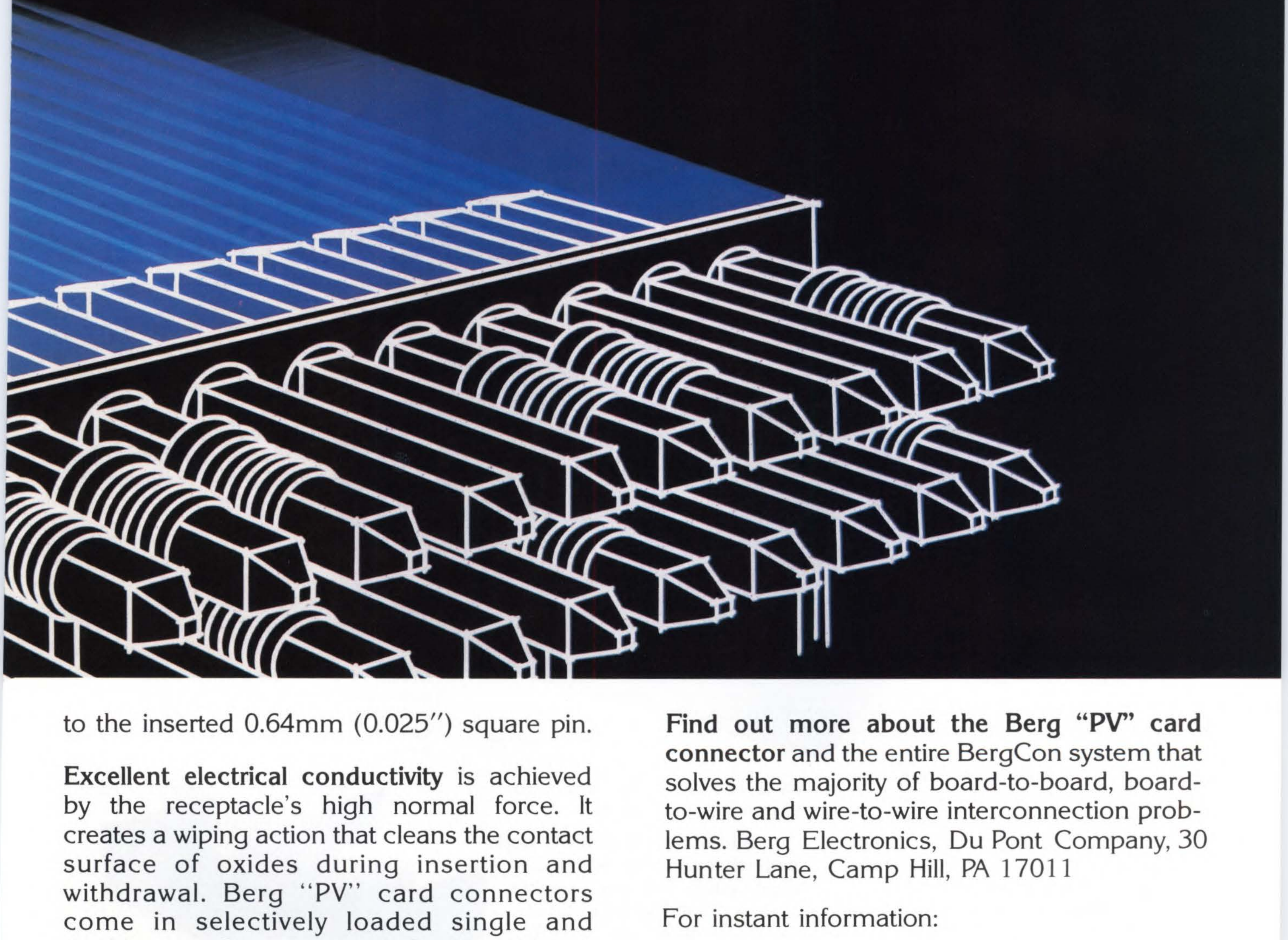

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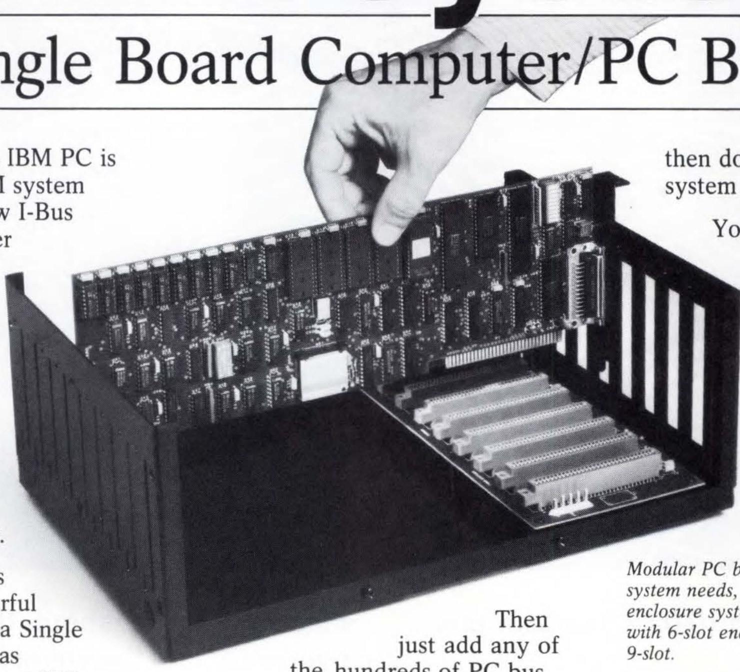

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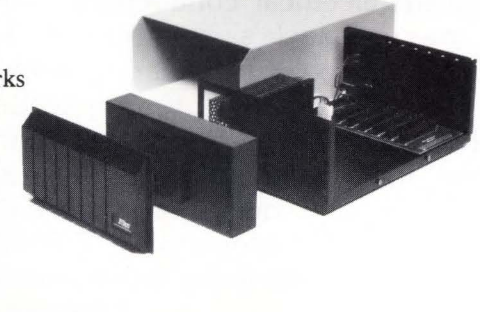

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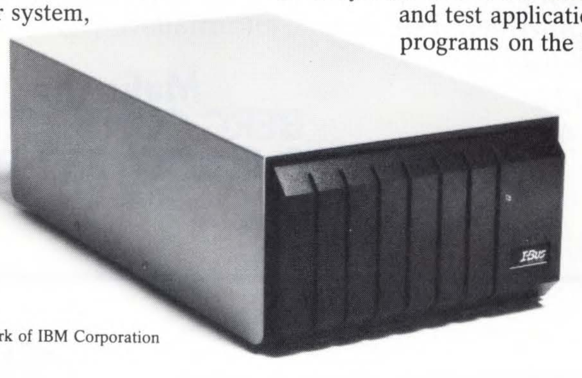

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# Highest-capacity 8-in. drive presents choice of interfaces

*A Winchester drive that stores 660 Mbytes is one of the first in its class to give designers the ability to work with both the SCSI and the SMD interface.*

The search for greater amounts of hard-disk storage goes inexorably on, always accompanied by the conflicting problems of holding disk size down and speeding up access time. Indeed, capacity becomes an increasingly urgent issue as supercomputers, which encompass multi-user systems, networking, computer-aided engineering, and artificial intelligence, continue to gain momentum.

But boosting memory is not enough; selecting an interface is also crucial. Low-performance ones like the ST506 are clearly inappropriate for high-performance applications. Instead, a designer must look for the intelligence delivered by the Small Computer Systems Interface (SCSI) or the up-and-coming second level of the Intelligent Peripherals Interface (IPI-2).

Although high capacity has historically been the domain of 14-in. disk drives, 8-in. Winchesters are making inroads into this territory. Certain to contribute to the 8-in. revolution is a seven-platter drive that stores up to 660.4 Mbytes (see ELECTRONIC DESIGN, Oct. 31, p. 356). It can be efficiently integrated into CAD/CAM workstations and fit into the slots intended for floppy disks. And it is fast: Access times average 18 ms and stay below 40 ms.

For systems integrators, the most welcome news may be that the 660.4-Mbyte MV600 and its companion the 331.8-Mbyte MV300 (see "Pushing Capacity to the Limit", below) are among the first drives in their class to allow a

**Clyde F. Czernek,** MegaVault Memories

*Clyde F. Czernek is the founder, director, and president of MegaVault Memories, Woodland Hills, Calif. Before starting the company in 1960, he was project management engineer at Borg Warner and acted as a consultant to IBM on hydraulic actuator systems for the first removable disk-pack drives. He went on to analyze and supervise the design and development of a rotary servo positioner for IBM's magnetic strip-tape memory system. His more than 30 years in the computer and electronics field make him one of the industry's leading experts in servo and actuator systems.*

### Pushing capacity to the limit

The MV300 records 331.8 Mbytes onto a standard 8-in. disk by organizing the data as 1266 cylinders, with 13 data tracks to a cylinder and 20,160 bytes on every track. Track density is 1000 tpi and the data density is 10,855 bpi. This configuration results in a 1.2-Mbyte/s transfer rate.

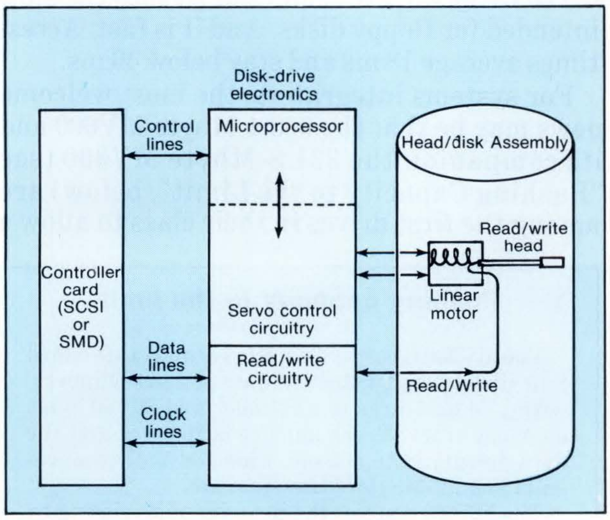
The MV600 doubles the capacity of its sibling by increasing both the number of cylinders and the bit density by 50%. The unit's linear head actuator was modified to pick up an additional 0.1 in. of stroke, thus increasing the number of available tracks.

The head-mounting mechanism was altered to squeeze the platters closer together, thus fitting more platters into the same-sized unit. Further, the head mount arranges the heads side by side. Beyond reducing the head profile by 0.2 in., arranging the heads in parallel permits reads and writes to be handled simultaneously at one location.

choice of either the intelligent SCSI or the standard Storage Module Device (SMD) interface. The latter enables a number of drives to be daisy-chained. (The pair will implement IPI-2 late in 1985.)

Changing interfaces is simply a matter of switching a single I/O board, one of the three boards in each unit. The other two are a microprocessor and servo controller and a read/write board. Which interface to choose depends on several factors, for each brings its own flavor to data transfers and other system characteristics.

For example, data transfers with intelligent interfaces are usually asynchronous, occurring in bursts. In such a system, there is generally a large memory buffer on the controller, residing between the host and the disk. On a typical write, for instance, the controller will wait until an entire sector of information has been transferred to it before it begins writing. Writing is timed by the controller to ensure that the data




**1. In an 8-in. disk drive, the three sets of lines between the controller board and the disk-drive electronics orchestrate the control, data, and clock signals. Using an SCSI controller, the host supplies high-level commands, and the controller addresses the disk as a series of logical addresses. With SMD, the controller must address specific cylinders, sectors, and head locations.**

is sent to the disk one sector at a time. The controller assumes the responsibility of dividing up the surface of a disk according to the number of data blocks. In contrast, a nonintelligent interface like SMD reads or writes the data at the same speed that it comes off or goes onto the surface of the disk. The controller does not have the option of slowing down or interrupting the data stream, since dividing the disk into sectors, as well as transfers, is managed by the host.

### One way or another

How data is stored on the disk is another way in which the interfaces differ. In a typical setup, the controller card mediates between the host and the disk-drive electronics. Three sets of lines from the controller position the head (the disks employed in the drives have a surface dedicated to servo head positioning data). The lines also manage passing data and clock information to and from the disk-drive electronics (Fig. 1).

Working with SCSI, the peripheral controller card identifies and oversees the tracks, sectors, and other physical spaces on the disk's surface. The SMD interface, on the other hand, leaves not only sectoring but managing tracks up to the host. Such factors make a substantial difference in the way a system designer addresses the relationship between a peripheral and the host.

Using SCSI, the designer need only be concerned with the logical address locations of the data. SMD demands an awareness of the physical sectors and the other divisions of the disk's surface.

### The long and short of it

Even with the trend toward offloading peripheral management tasks from the host, engineers must choose where to place the controller. At the host level, SCSI typically puts the controller within the drive, which simplifies both the hardware and the protocol required for the host to address the unit. At the same time, placing the controller there not only elevates the cost of the drive but also imposes specific limitations.

For one thing, SCSI stretches a much shorter cable between a host and a drive than does

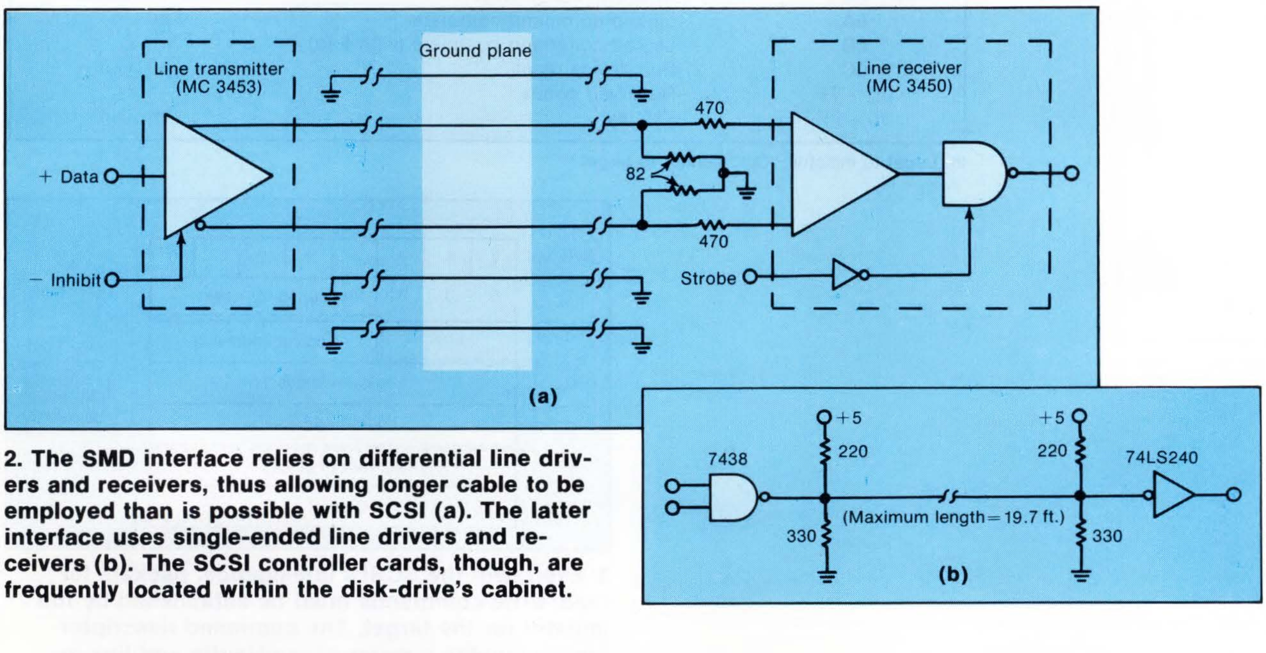
SMD. The latter allows for up to 100 ft of cable, with balanced differential cable connections for each parallel data line (Fig. 2a). SCSI, in contrast, employs cables roughly 20 ft long, due to the fact that the interface's drivers are typically single-ended open-collector transistors with 220/330 Ω terminations (Fig. 2b).

The SMD demands two connectors and two cables, one with 60 pins and one with 26 pins. The 60-pin cable carries all control functions, and the 26-pin line the clock and data signals. The SCSI, on the other hand, requires a single 50-pin header.

**Open to all**

SCSI rapidly emerged as a defacto industry standard and was ultimately formalized by ANSI as a specification for linking computers and their peripherals. It permits all types of storage units to be integrated simply into a system. In theory, the system designer need only write high-level commands to address a peripheral without worrying about the device-level interface. Such device-independence makes upgrading and substituting peripherals on the SCSI bus a relatively easy task. Further, the interface is structured so that all of its commands can be executed by a peripheral device while it is disconnected from the host. In practice, the engineer creates packets or command blocks for the SCSI controller to transfer to the drive.

On the device level, SCSI addresses disk sectors as logical blocks rather than as specific device cylinders or sectors. SCSI handles more than 4 billion blocks of data distributed among as many as eight drives. Adding a drive requires that the user be aware of the maximum block number that can be addressed. When the 660.4-Mbyte drive is used, the higher block numbers will probably be unfamiliar because of the record-breaking capacity of the unit. SCSI's Read Capacity and Format commands will aid in formatting the drive in such a way that its storage space can be fully employed, but the system integrator still has the job of arranging




**2. The SMD interface relies on differential line drivers and receivers, thus allowing longer cable to be employed than is possible with SCSI (a). The latter interface uses single-ended line drivers and receivers (b). The SCSI controller cards, though, are frequently located within the disk-drive's cabinet.**

data in packets for read/write transfers to and from the disk.

On an 8-in. drive, SCSI works by passing coded messages between the controller and the peripheral, with one playing an active role as the initiator and the other assuming the corresponding role of target. Among the most significant coded messages are those to disconnect or reconnect a storage unit with the bus. Also important are those that connect blocks or strings of data and those that indicate the status of the initiator and the target in the command execution process (see Table 1).

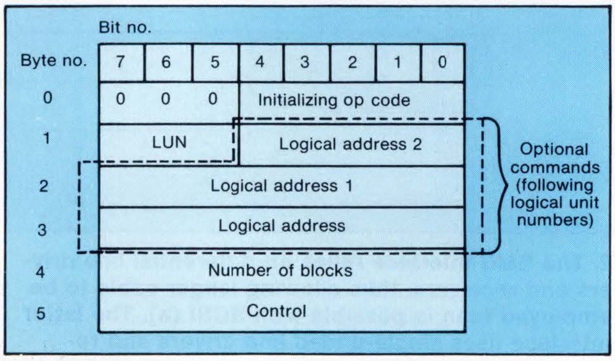
SCSI's nature is such that a seek is implied in every data transfer command. That is, if the read heads are not positioned over the correct cylinder, a seek is automatically initiated, starting at 0 and continuing until the desired block is found.

On the disk drives themselves, each block number represents a sector, and up to 256 sectors can be specified to be read with one com-

**Table 1. SCSI message codes used with 8-in. Winchesters**

| Code (Hex Values) | Description | Direction | |
|---|---|---|---|
| 00 | Command complete | In | |
| 01 | Extended message | In | Out |
| 02 | Save data pointer | In | |
| 03 | Restore pointers | In | |
| 04 | Disconnect | In | |
| 05 | Initiator detected error | | Out |
| 06 | Abort | | Out |
| 07 | Message reject | In | Out |
| 08 | No operation | | Out |
| 09 | Message parity error | | Out |
| 0A | Linked command complete | In | |
| 0B | Linked command complete (with flag) | In | |
| 0C | Bus device reset | | Out |
| 0D - 7F | Reserved codes | | |
| 80 - FF | Identify | In | Out |

In: target to initiator Out: initiator to target

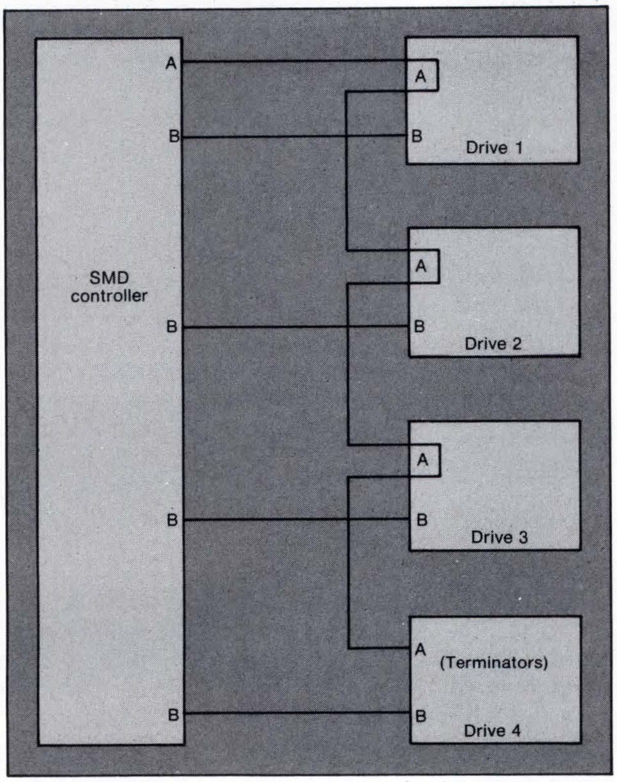



**3. Even with the SCSI's intelligence, packets for read/write commands must be established by the initiator for the target. The command descriptor block includes a series of read/write and link instructions sent to the peripheral and a logical address for that unit. The starting address of the data block to be transferred and the number of blocks involved are also indicated.**

mand. If the host asks for the next 256 logical blocks, starting at block 0, then the first 256 sectors will be transferred across the interface before any other commands are recognized.

### The chain of command

An I/O request to an SCSI device is initiated by first selecting the path from the initiator to the target and then passing a command descriptor block to the target (Fig. 3). The first byte of the block is the command operation code, and the remaining blocks specify, for example, the logical unit numbers (the peripheral devices being addressed), the block's starting address, the number of blocks to transfer, and the control byte.




**4. The SMD interface allows up to 16 drives to be daisy chained by joining them in parallel on control cable A. Separate data and clock cables are required between the controller and each drive.**

The operation code for SCSI (bits 7 through 0 on byte 00) allows for a total of 256 commands ($00_{16}$ to $FF_{16}$). The upper three bits of the operation code are termed group code. They describe one of the eight possible groups to which the command belongs. The lower five make up command code.

The group code (bits 7, 6 and 5 on byte 00) includes eight categories or groups of commands, listed from 0 to 7. Since three of these are reserved and two are designated as vendor-unique, only three (0, 1, and 5) are employed in most new SCSI drives. The group code merely signifies how many bytes there are in a command-descriptor block. Group 0 includes six-byte commands, while group 1 is made up of 10-byte commands. Group 5 consists of 12-byte commands.

### Command codes

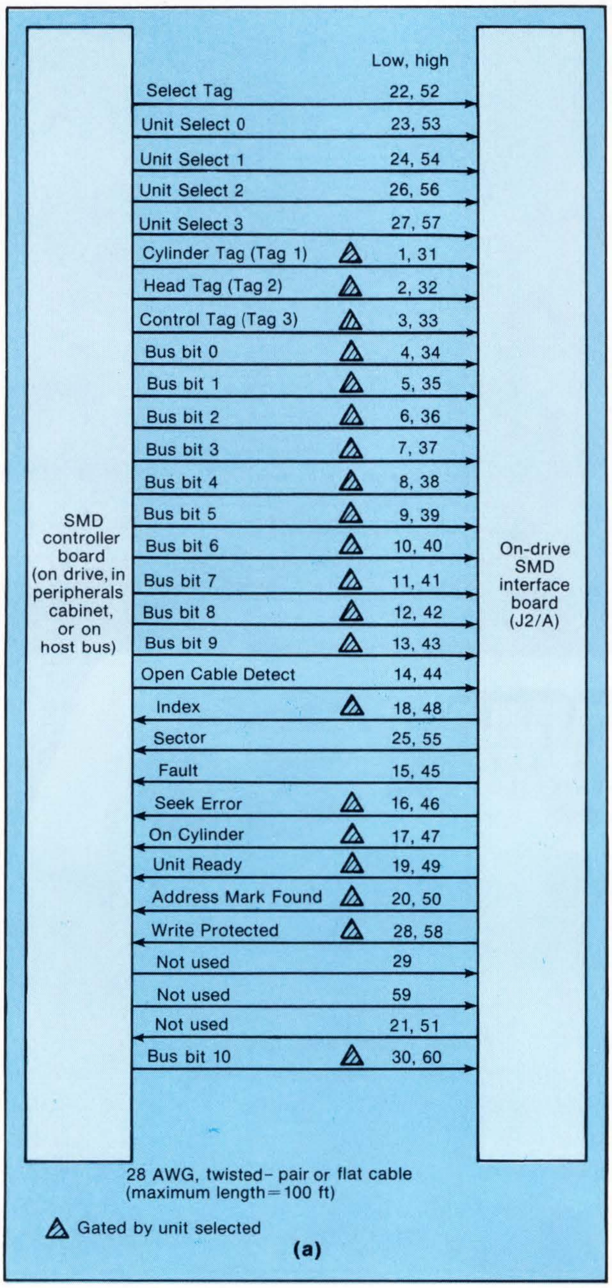
Bits 4 through 0 on byte 00 are the command codes for each SCSI group. They can be categorized as Standard (S) commands, those employed merely to meet the minimum requirement of the specification (Request, Sense Format, Read, and Write). Extended (E) commands include Inquiry and Special Format. The Optional (O) commands are implemented as defined. The Vendor Unique (V) commands (e.g., Copy, Rezero Unit, and Special Format) are specific to each drive. The Reserved (R) commands are not used now but will be defined for the SCSI specification at some time in the future.

Compared with SCSI, the SMD interface is relatively low level. For instance, it is up to the controlling device to identify the data sectors on the drive. SMD uses sector and index pulses (rather than logical addresses) to indicate the beginnings of a field, and sector marks are the reference points employed in seeking and reading data. On the disk drives, they are derived from the dedicated servo track and are continually transmitted back to the controller. The

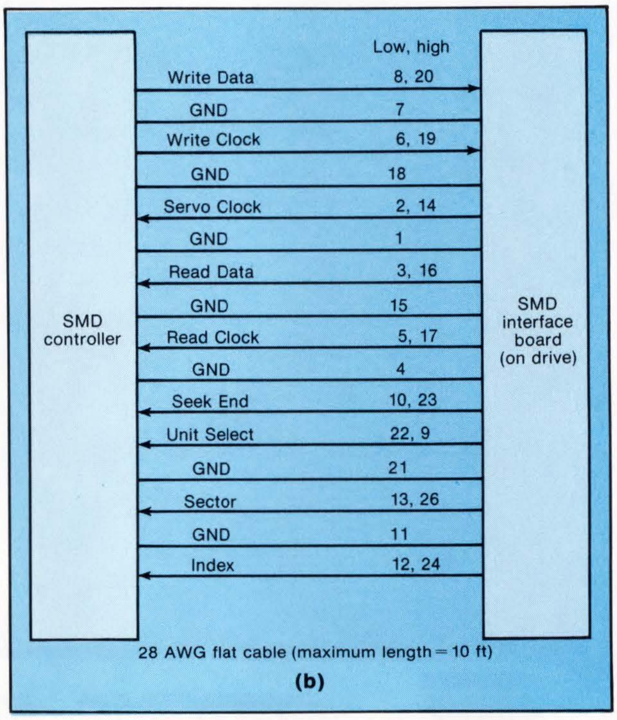
number of sector marks to a disk is always one fewer than the number of usable sectors, since the very first sector (0) following the index has no sector mark.

As many as sixteen drives can be daisy chained by linking them in parallel on control cable A. Separate B cables are thus required for each drive (Fig. 4). Those handle the drive selection functions and cue a particular drive as to whether it should be reading or writing data. The actual sector-addressing and tag control functions are handled by 11 lines of the A cable—bus bits 0 through 10. The termination resistors are installed in the last drive of the daisy chain.

The disk drives use only one A cable (for the control signals) and one B cable (for data). The first conforms to normal SMD signal timing and control functions (Fig. 5a). The second carries Read Data, Read Clock, Write Data, Write




**(a)**




**(b)**

**5. On the SMD interface, cable A furnishes the drive, cylinder, sector, and head addresses and control signals over a 10-bit control bus. It also carries tag lines and status lines (a). Cable B contains separate lines for writing data, for reading data, and for clocking these serial operations (b).**

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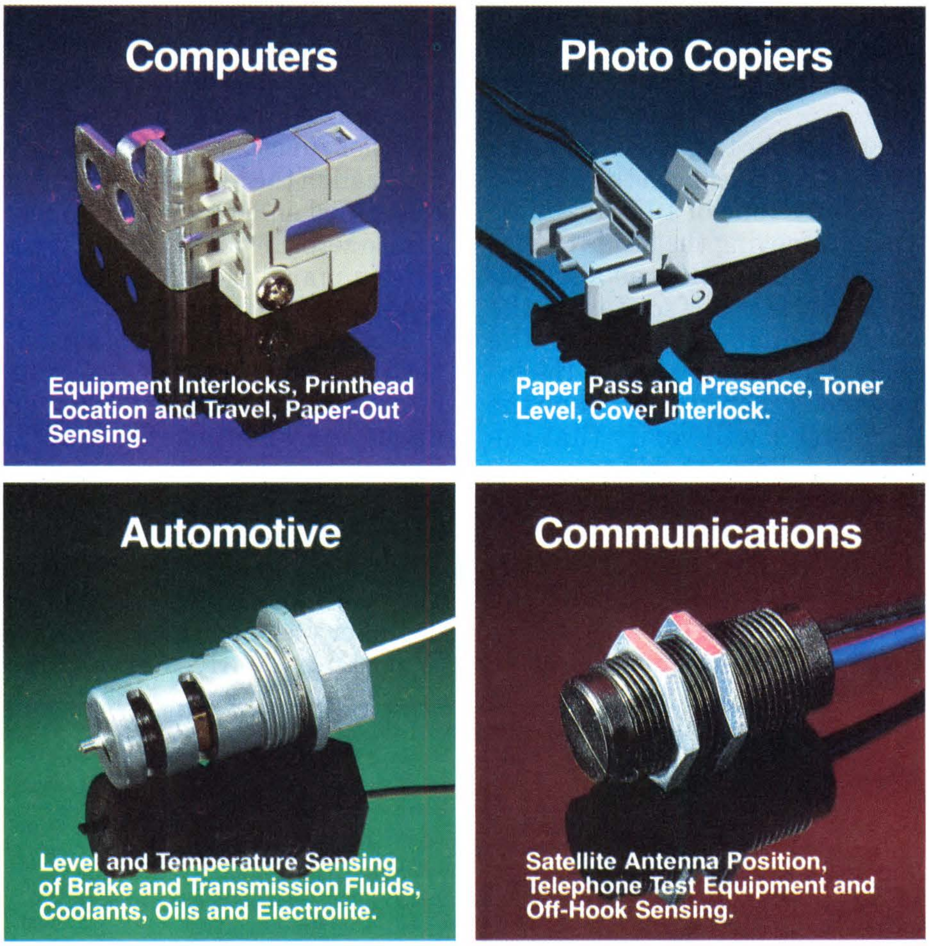


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**CIRCLE 139**

Clock, and Servo Clock control signals (Fig. 5b).

The A control table contains three qualifying tags that change the head address, handle disk seeks, or govern reads and writes in conjunction with the 11-bit control bus (see Table 2).

#### Tag, you're it

When tag 1 (the Cylinder tag) is asserted, the drive interprets the information on the bus as a 10-bit cylinder address (one of 1024 available cylinders) and begins moving the heads to that track. Unlike SCSI, which relies on a logical block address, the SMD interface forces the user to specify the cylinder locations on the drive. The cylinder address is placed on the interface bus lines and is then strobed in by the Cylinder tag. The drive will verify that the requested cylinder is valid and begin searching for it. The drive must be on the cylinder before the Cylinder tag is actually sent.

Similarly, tag 2 (the Head Selection tag) chooses one of up to 16 possible heads (the seven-platter drives work with 13 heads) with a 4-bit address furnished by four signals on cable A. When it is asserted, tag 3 (the Control tag) also indicates a read, write, or a seek over the 10-bit bus. In order to write, say, bus bit 0 is asserted to indicate a Write Gate. (At the same time, the write clock and write data signals are supplied on cable B.) Likewise, reading involves asserting bus bit 1.

Other functions, such as Positive Servo Offset, realign the head-positioning mechanism by a specified amount in order to recover lost data. It also zeros in on the center of a track and supplies a margin (that is, a test track) for the read/write electronics.

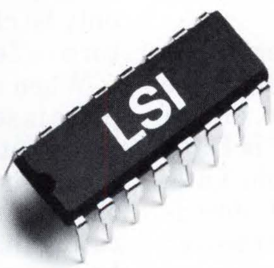
With the Control tag asserted, the drive interprets bus bit 0 as the Write Gate signal (which enables the write drivers on the disk drive), and bus bit 1 as the Read Gate (which activates the drive's phase-locked-loop. Bus bit 2 serves as the Positive Servo Offset and bus bit 3 as the Negative Servo Offset.

When the Positive Servo Offset signal is true, the positioner moves from the established On Cylinder position inward toward the spindle. When the Negative Servo Offset is true, the

**Table 2. Setting up the control line**

| | Tag 1 | Tag 2 | Tag 3 (asserted to bus) |
|---|---|---|---|
| Bus | Cylinder address | Head selection | Control selection |
| Bus 0 | Bit 0 | Bit 0 | Write Gate |
| Bus 1 | Bit 1 | Bit 1 | Read Gate |
| Bus 2 | Bit 2 | Bit 2 | Positive Servo Offset |
| Bus 3 | Bit 3 | Bit 3 | Negative Servo Offset |
| Bus 4 | Bit 4 | N.a. | Fault Clear |
| Bus 5 | Bit 5 | N.a. | Address Mark Enable |
| Bus 6 | Bit 6 | N.a. | Return to Zero |
| Bus 7 | Bit 7 | N.a. | Data Strobe Early |
| Bus 8 | Bit 8 | N.a. | Data Strobe Late |
| Bus 9 | Bit 9 | N.a. | N.a. |
| Bus 10 | Bit 10 | N.a. | N.a. |

# FAST ON ITS FEAT.

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CIRCLE 140

movement is in the opposite direction. Ordinarily, an On Cylinder status line indicates that the drive has positioned the heads over a track and is ready to read or to write. It goes false with any drive command that causes the head to move. The On Cylinder line also will go false for 2 ms when the Offset Command is received, to allow the head positioner to settle. Attempting to read or write in this position will set a Fault indicator on cable A. In addition to a Track Offset condition, the drive asserts the Fault line when there is a Write Fault or when the phase-locked loop was lost with the Write Gate asserted.

Bus bit 4 is the Fault Clear signal. This is a 100-ns pulse (minimum) that will cause the drive's Fault Status line to clear once the offending condition no longer exists.

Bus bit 5 is the Address Mark Enable signal. In conjunction with either the Write Gate or the Read Gate, it writes or recovers address marks. If used with the first, it creates an address mark by erasing a small section of data (about 4 $\mu$s). When used with the second, the address mark can be recovered by the read circuitry. When an address mark is recovered, the Address Mark Found signal is sent to the controller and the beginning of a data record is indicated.

Bus bit 6 is a reset, or Return to Zero. This 250-ns pulse causes the drive to recalibrate the heads to track zero, to select head zero, and to clear the Seek Error latch. Bus bit 7 is Data Strobe Early and bus bit 8 is Data Strobe Late: both cause the drive to modify its RLL-decoding timing slightly. The signals help recover marginal data.

### Along the line

Operating an SMD driver, consequently, can be viewed as an exchange of signals along cable A. The Unit Ready and Open Cable Detector signals, for instance, indicate that the drive is ready to seek, read, or write and that no fault is present. They also disable the interface in the event that the cable is disconnected or that power to the controller is lost. The actual data transfer, however, occurs on the serial data lines of cable B.

Bits 0 through 3 of the unit selection bus are used by the controller to indicate which of the 16 logical drives are to be selected when the Select tag goes true. There is a DIP switch on the drive's I/O board that allows their logical addressed to be defined.

The Select tag forces each drive on the SMD cable to compare the unit selection Bus Value Signal against its own Unit Select Switches. If the two match, the drive will be internally selected within 600 ns of the leading edge of the signal. The controller must keep the Unit Select high for the entire time the drive is selected. When the Select tag goes low, the drive is immediately disconnected.

The Index signal occurs once every revolution, and its leading edge is considered the beginning of sector zero. Typically, it is 2 $\mu$s long. The 256 sectors on the surface of the disk, and the Sector Pulse signals, are counted to supply data-address locations during seeks.

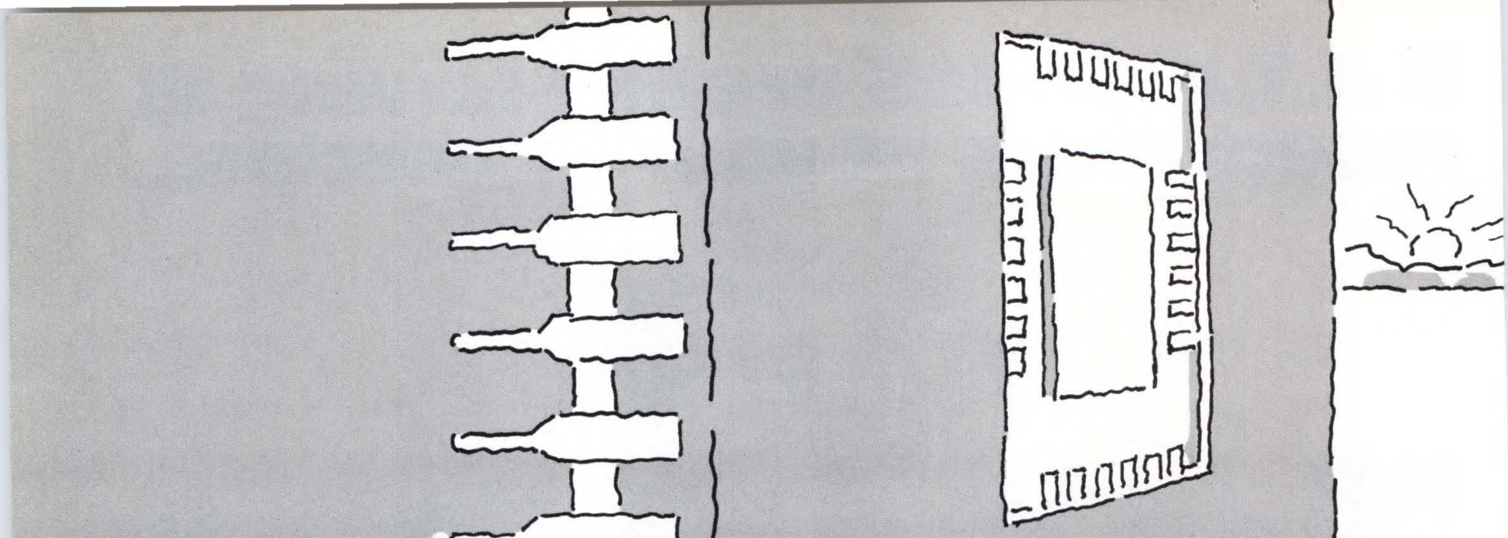
### Seek and ye shall find

If a Seek Error is indicated on cable A, then the controller either failed to complete a seek in 100 ms, the controller requested an illegal sector, or the drive electronics determined that the data heads were outside of the valid data area. A seek error is asserted within 100 ns of the leading edge of the Cylinder tag signal and can only be cleared by the controller issuing a Return to Zero command.

When a seek is successful, a 9-ns maximum pulse is sent, which is the Address Mark Found. It indicates that data will follow shortly on cable B. The drive sends it to the controller when the Control tag and Read Gate are true, indicating that a previously recorded address mark has been located. The Unit Selected line indicates that the drive is selected and is ready to receive a command from the controller.

Enabling a Write Protect inhibits writing under all conditions. That can be done with a jumper on the I/O board or with the external plug-in status monitor box. Combining On Cylinder or Seek Error with Seek End indicates that a seek has been terminated. □

| **How useful?** | **Circle** |
|---|---|
| Immediate design application | 556 |
| Within the next year | 557 |
| Not applicable | 558 |



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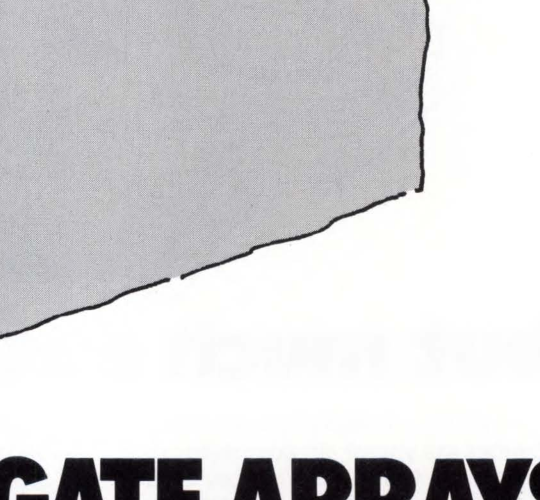


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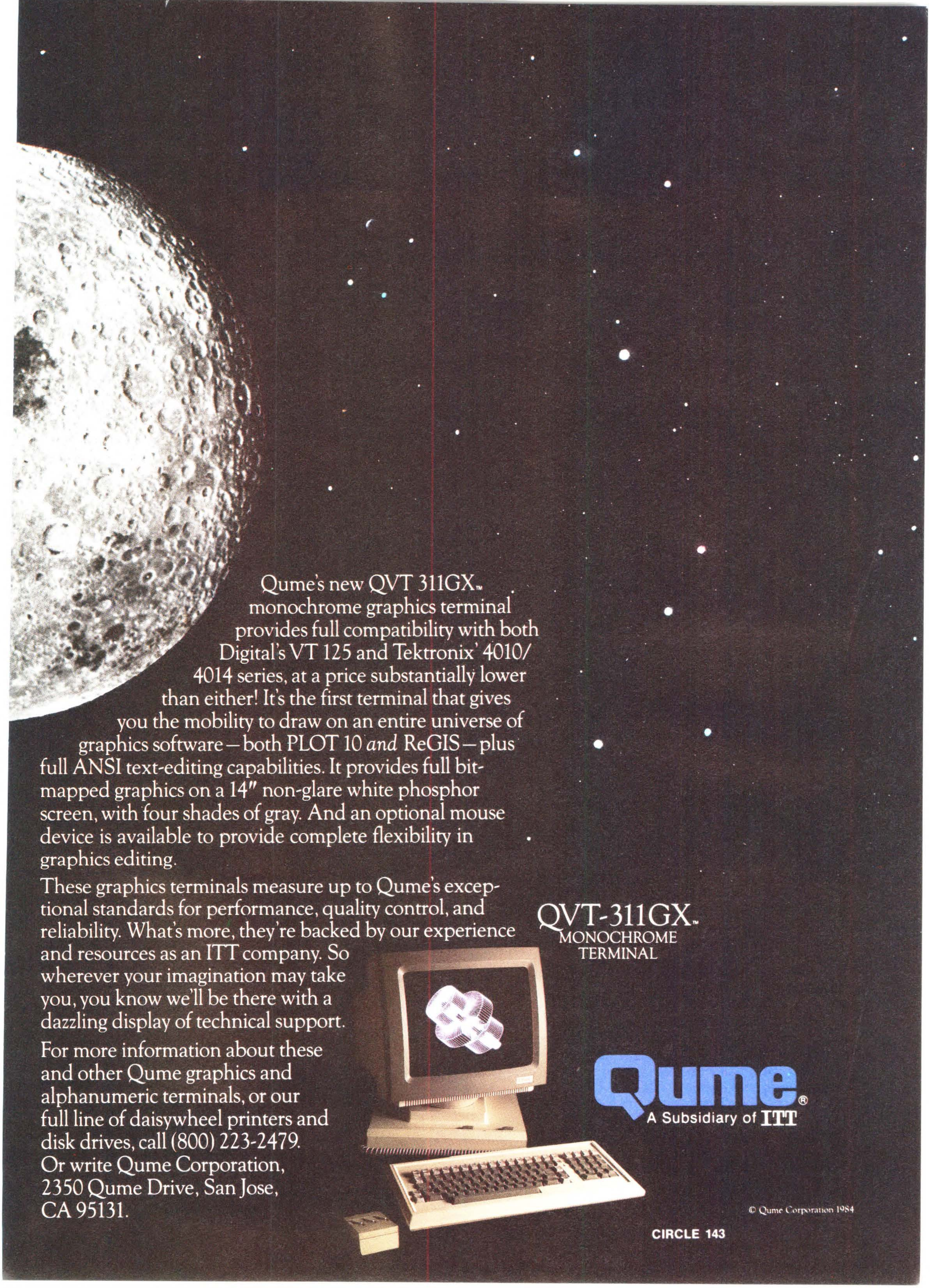
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CIRCLE 143

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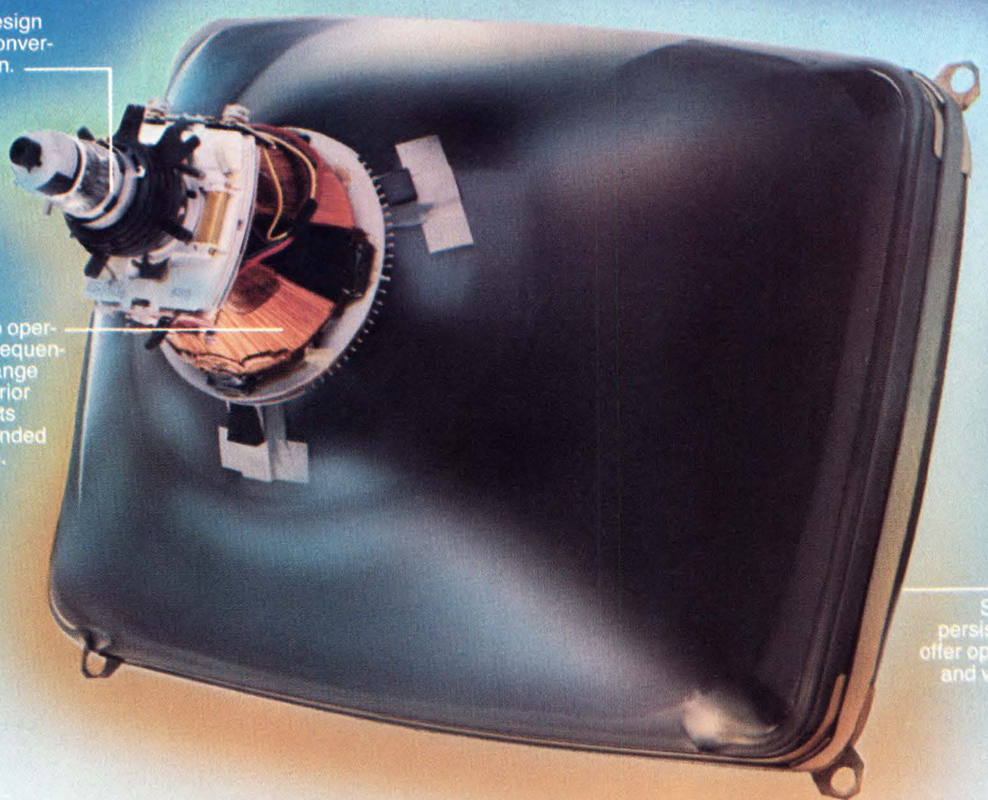


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|---|---|---|---|---|---|---|---|---|
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| | 12″ (11V) | | | | | 0.31 | 0.37 | 0.47 |
| | 14″ (13V) | | 0.2 | 0.31 | 0.25 | 0.31 | 0.4 | 0.4 |
| | 16″ (15V) | | | 0.31 | | 0.31 | | |
| | 20″ (19V) | 0.25 | 0.25 | 0.31 | | 0.31 | 0.44 | 0.56 |
| | 26″ (25V) | | | 0.37 | | | | |
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# Handling real-time images comes naturally to systolic array chip

*The internal memory and specialized algorithms of a systolic array IC cut the amount of hardware and boost the speed associated with image processing.*

*This is the second in a series focusing on the first commercial systolic array processor chip, developed by NCR Corp.'s Microelectronics Division in Fort Collins, Colo. The opening article was the Oct. 31 cover story (p. 207). Upcoming discussions will investigate the device's use in pattern recognition, data-base management, and as an associative processor.*

Until recently, real-time image processing has been a difficult task, calling for a large amount of hardware. Most high-performance systems comprise a frame buffer, which stores the incoming image; a high-speed, pipelined processor to carry out the needed algebraic manipulations; and a second buffer to retain the processed image. Although interleaved sequential memory accesses in such setups make it possible to load and unload the buffers rapidly, the bandwidth of the memory-processor bus limits throughput. Furthermore, some image-processing algorithms require several fetches for each pixel, further cutting into overall system speed.

**Wyndham Hannaway,** G.W. Hannaway & Assoc.
**Gary Shea,** Consultant
**William R. Bishop,** Consultant

*Wyndham Hannaway heads G.W. Hannaway & Associates, a technology consulting firm in Boulder, Colo., specializing in optics, image processing, and simulation. He helped create the boards for the systolic array and the algorithms for image processing.*

*Gary Shea is an independent consultant in image-processing software. He holds a BS in mathematics from the University of Colorado.*

*William R. Bishop is a consultant in image processing at G. W. Hannaway & Associates.*

The Geometric Arithmetic Parallel Processor (GAPP) chip overcomes these obstacles by supplying an array of 72 parallel bit-serial processor elements, each of which is fitted with 128 bits of RAM. This configuration lets system designers dedicate an individual processor element to every pixel. To cut costs, though, many systems could handle small groups of pixels or subimages serially, assigning more than one pixel to a processor element, or cell. In fact, the systolic array can be viewed as a combined frame buffer and processor, bringing a bit-mapped an image into its RAM, processing it, and then putting it back in RAM before sending it out. One example of the chip's prowess is its ability to store two images in its RAM and then deliver the difference between them. For design considerations, the monolithic array can also be considered a highly pipelined, parallel processor.

Since the chip departs substantially from the conventional von Neumann architecture, image-processing systems based on it must vary from the usual as well. To demonstrate these differences, it is necessary to briefly examine the traditional approaches. One, for instance, relies on a pipelined ALU, with separate frame buffers for input and output. Pipelining joins a series of processor elements to perform sequential arithmetic operations on a continuous data stream. The method is good with processors that range from bit-slice devices to supercomputers. Nonetheless, even the latter can perform only from 20 to 100 operations on each pixel to sustain a real-time rate of 10 megapixels/s, the rate of standard video systems.

The systolic array can drop into such an architecture (Fig. 1). With 32 of the chips joined together to create a grid of 48 by 48 processor elements totaling 2304 processors, up to 60 million pixels/s can be accepted, even with a gray-scale depth of 8 bits a pixel. Since data can be loaded over the chip's communication (CM) bus at the same time that it is processed, the grid array can operate at full speed at all times, chewing up 920 million macroinstructions every second. (A macroinstruction is defined here as an 8-bit addition that can be executed in 25 cycles, or 2.5 $\mu$s.) Linking together more chips further increases processing power.

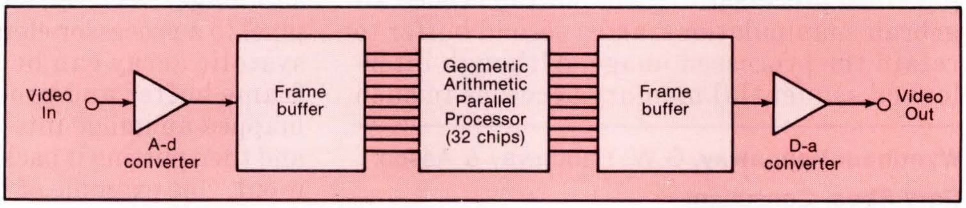
Despite its impressive speed, the architecture is not optimal for the systolic processor because data must be reformatted to work with the array. The chip works with information in the form of bit planes. As a result, an 8-bit number representing the pixels must first be reformatted as a bit plane. The first bit plane represents the least-significant bits. Once in the array, the whole plane is written to one location within the internal RAM of each processor element. The next seven bits must be loaded similarly, but such reformatting is too complex for most frame buffers.

### Shifting into first

To overcome this hurdle, a designer can turn to serial-to-parallel shift registers long enough to store one full video line (Fig. 2). During the horizontal retracing period of the television signal, the previous video line is shifted into the edge of systolic arrays, which can consist of any number of chips. The least significant bit of each pixel in the line is shifted into the bottom row of processor elements and written into RAM address 1. The next most significant bit is then shifted in and written to RAM address 2. The process continues until all eight bits of every pixel line have been loaded into RAM addresses 1 through 8 of the bottom row of processor elements.

Each RAM location of the block is read into the CM register before each shift into CM from the south (CM=CMS), so that the first video line is shifted up and written into the adjacent row of processor elements when the second line enters the bottom row of processor elements. Once the grid is filled, the same process occurs as the image is unloaded to the north and sent to the output video line buffer.

The line buffers can be designed with either shift registers or with systolic array devices. The latter approach enhances performance,




**1. A Geometric Arithmetic Parallel Processor can be substituted for traditional microprocessors in a pipelined architecture. The arrangement requires the memory to be very wide, and data to be reorganized. It is thus better to reconfigure the architecture to take advantage of the chip's properties.**

since these chips can compute while handling the serial-to-parallel shift. Regardless of whether systolic arrays are used, the chip's memory associated with each processor element allows it to simultaneously store up to 16 images of 8 bits each, obviating the need for frame buffers.

### Quicker than the eye

Once the architecture of the image-processing system is selected, the next concern is deciding on the number of systolic array chips (see "Welcoming Aboard the Systolic Array," p. 293). When speed is the primary concern, a one-to-one relationship between processor elements and pixels can be established. A block of 512 by 512 processor elements, made up of about 3700 chips, can perform 100 billion 8-bit additions a second. In the thirtieth of a second it takes to bring in a typical television frame, every cell can execute 13,333 8-bit additions or 333,333 primitive single-cycle instructions—for more than the number demanded by many real-time image-processing algorithms (see "Systolically Altered States," p. 294).

Thus instead of a simple 1:1 ratio between processor elements and pixels, a system might dedicate one element to a number of pixels and thus process data in the form of windows. When one window is completed, processing can begin on the next.

### Beat the clock

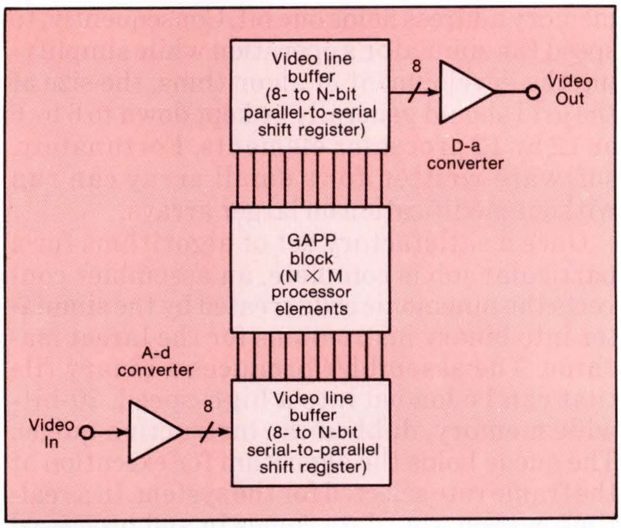
In a system involving a real-time algorithm, which does not require the use of previous image frames, the entire 512-by-512-pixel image need not be in the GAPP array all at once, thereby cutting the number of devices required. In a so-called neighborhood processing algorithm—one that determines the next value of a pixel by comparing it with the pixels surrounding it—a block of 24 by 516 processor elements, consisting of 172 systolic devices, can carry out 600 additions on every pixel while operating at 10 MHz—far more processing power than available with conventional architectures.

Since less hardware is used, the necessary program may be larger and more complex than that found in architectures devoting one processor cell to every pixel. Despite such differences, the algorithms share many attributes. In this set up, each pixel is stored in internal RAM, and although it might first appear that 128 bits of image data can be held in memory, the need to retain operands and intermediate results and to flag overflows reduces the chip's capacity somewhat. As in the first configuration, the number of systolic devices can be boosted or cut.

### A different point of view

Programming the systolic array is radically different from programming a traditional microprocessor. The first is a single-instruction, multiple-data path (SIMD) machine; the second, a single-instruction, single-data path (SISD) device. For that reason, code for an existing chip cannot simply be converted: Writing software for the systolic chip demands a new way of looking at both the task and the necessary algorithm.

To facilitate programming the systolic processor, a simulator that runs on personal computers has been created. Written in C, the software runs under Unix and operates NCR's PC-4 and on the IBM PC XT as well as on larger systems like the Digital Equipment PDP-11




**2. A video line buffer, which stores a full input line from the camera, can be made up of either shift registers or systolic array chips. The 128 bits of RAM included for each processor element in the GAPP block eliminate the need for frame buffers.**

and NCR's Tower 1632.

Although the advantages of simulating operation while the hardware is being designed are obvious, it must be noted that running the array program on a single-instruction, single-datapath computer will be very slow. A task executed as a single instruction on a systolic array will require at least $N^2$ operations when it runs on a conventional processor, where N equals the number of processor elements along one axis of the array.

Consider the addition of two 8-bit, 512-by-512-pixel images. A 10-MHz, 8-bit processor needs at least 1 second to do the job. As mentioned earlier, a grid of 512 processor elements could perform the same function in 25 cycles, or about 2.5 $\mu$s.

### Breaking with convention

Another factor that must be considered when the simulator runs on a traditional computer is the relationship between the memory and a processor. A conventional processor passes data between itself and memory. The systolic array, in contrast, has the aforementioned 128 bits of RAM associated with each cell, and every memory address holds one bit. Consequently, to speed the simulator's operation while simplifying the development of algorithms, the size of the grid should generally be kept down to 6 by 6 or 12 by 12 processor elements. Fortunately, software written for a small array can run without modification on larger arrays.

Once a satisfactory set of algorithms for a particular job is complete, an assembler converts the mnemonic code created by the simulator into binary instructions for the target machine. The assembler produces a binary file that can be loaded into a high-speed, 20-bit-wide memory, dubbed the instruction queue. The queue holds the algorithm for execution at the frame rate selected for the system. In a real-time system, say, data comes in and processed data goes out simultaneously. As the algorithms run, a complete loop through the instruction queue is repeated for every new frame passing through the grid.

The kinds of algorithms that must be developed for image processing are, of course, directly tied to both the specific demands of such processing and to the way the array works. Image-processing computations are more distinctly parallel than those of scientific and business calculations, in which memory use and the operations performed are far more random.

The speed with which the systolic array handles such parallel chores can be clearly seen by again comparing the array to a traditional processor. A von Neumann machine requires on the order of $N \times N$ cycles to process an $N \times N$ pixel image. That interval is expressed as $O(N^2)$, which is short for "order N squared". The systolic array needs only O(N), or even O(k) cycles, where k equals either the number of bits per pixel or the number of digits used in the calculation, to process the same image.

When the array processes an image, each element is active simultaneously, so the time needed to subtract one image from another is independent of the size of the image. Algorithms for the primitive operations of image processing—adding and translating an image along an axis and manipulating the gray scale—can be performed in O(k) time. Furthermore, operations that normally occur within the individual registers of a von Neumann processor (bit inversion, bit setting or resetting, and bit shifting) are easily handled in O(k) cycles by the systolic array.

### Nothing to it

Other algorithms handled just as readily by the device are those requiring information about the four or eight neighboring pixels. A 4-neighborhood algorithm can be defined as one using the north, south, east, and west processing elements of a particular portion of an image. The eight-pixel neighborhood consists of those four plus the northeast, northwest, southeast, and southwest cells. Such algorithms include 3-by-3-pixel convolution, a 3-by-3-block pattern matching, and various types of erosion and dilation. All of these are classified as local algorithms, since they do not require information from any elements other than their immediate neighbors.

Global algorithms, on the other hand, like histograms and correlations, need information from more distant elements. They take O(N) time, much faster than the time demanded by a traditional computer.

Certain fundamental operations are common

## Welcoming aboard the systolic processor

Since the Geometric Arithmetric Parallel Processor differs so radically from traditional processors, a number of aspects of design must be considered when a pc board is laid out. Foremost among these are the communications lines that join a block of systolic processors.

No support circuitry is called for between the chips, which themselves are easily linked to their neighbors to the north, south, east, and west. In that, they resemble an individual processing element within a single array, which is joined to its four nearest neighbors. Further, the 84-contact packages are readily connected since the North output of one IC is physically adjacent to the South output of an adjoining chip. The East and West ports are similarly compatible.

Terminating the outer edges of a block of arrays demands a variety of techniques, depending upon which algorithm is being executed. That presents no problem, though, since a programmable multiplexer can switch from one termination technique to another, under software control.

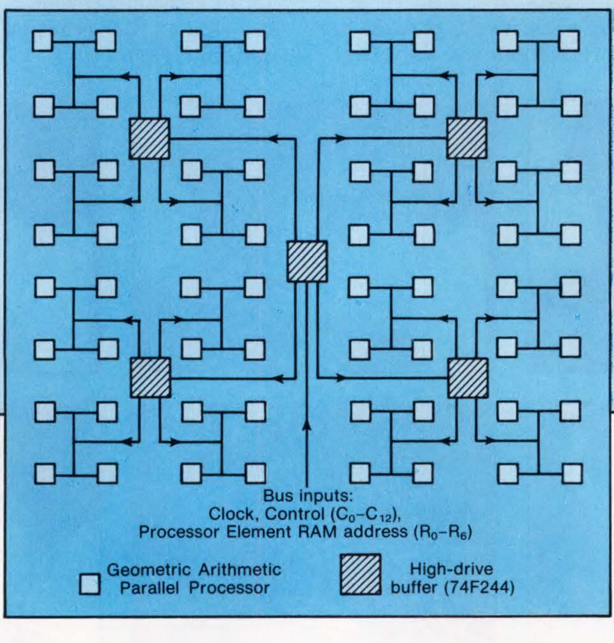
On the one hand, the edge connections can be grounded during input cycles so that all shifts bring in zeros from the outer edge of the block. Alternatively, the edges may be tied to a data bus for I/O. A third approach brings the connections from the east and north around to those of the west and south, respectively, so that data is recycled.

These connections can be made without concern for loading and fan-out, since they involve only the processor elements at the edge of the group of chips. Control, address, and clock signals, however, must be bused to each device in a grid of chips. In wraparound layouts, synchronization is critical between the clock and control lines at the edges of the block.

When large blocks of the chips are grouped together, it is generally best to drive them in groups of less than 40 chips. Driving more chips can skew timing and may exceed the power capabilities of driver chips. The routing for this type of bus is best laid out using an H-shaped topology (see the figure).

When a number of chips are being clocked synchronously and driven in parallel by command drivers, power distribution must be uniform. Therefore, boards using wire-wrapped interconnections should have full surface power and ground planes. Inattention to the capacitive details of coupling and ground planes can cause undershoot and overshoot of signals. To supply a new control word every 100 ns, keeping pace with the device's 10-MHz clock, a 20-bit-wide instruction queue for both the control and address lines is needed. Most designs, however, should include 24 or more extra bits to ensure space for control functions and looping. Static RAMs are the simplest to use for this; however, for high speed 2k-by-8-bit RAMs are preferred.

The instruction queue in a system based on a systolic array is driven by high-speed address sequences. The four extra bits in a 24-bit-wide instruction queue can be used to control jumps and loops of an address sequencer. The Global Output signal from the array can serve as a flag for conditional jumps.



to both local and global algorithms. One such operation, or building block, is overflow detection, which is used for many tasks.

One approach to it conjoins a 1-bit field with each field to be operated upon. Adding a field of 3 bits and a field of 5 bits will probably cause an overflow if it is delivered to a 3-bit field, so a 1 will be placed into the overflow field. The resultant image provides useful information about the data being processed. For instance, the overflow bit may be used to generate a visual, cue, like light or dark spots on the screen, to indicate which elements have overflowed. It can be used to interactively adjust the algorithm.

Among the other operations necessary for image processing are common arithmetic functions like addition, subtraction, and multiplication. Generally, images consist only of positive numbers representing the gray-scale value of the pixel. Image multiplication is needed for windowing or masking. A two-dimensional template representing a window may be shifted into the array and multiplied by the resident image. Any of these arithmetic operations may cause an overflow, which will be indicated if an overflow bit plane is used in the result field.

Register shifting is taken care of in the same

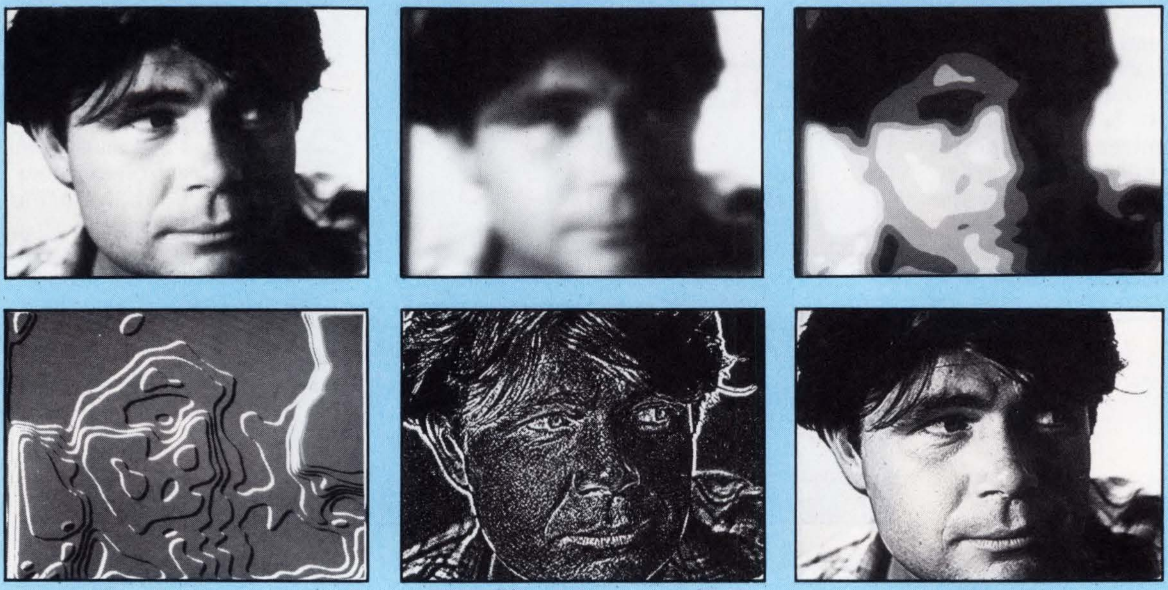
## Systolically altered states

When used with a standard camera (operating at 30 frames/s), the Geometric Arithmetic Parallel Processor can handle images in real time, as this image enhancement indicates.

The series of photos begins with a digitized 512-by-480-pixel image with 8 bits of gray scale resolution (top left). The image is first convolved, which diminishes the effects of camera noise (top center). Then it is trimmed from 8 bits to 4 (top right), reducing the number of gray-scale levels from 256 to 16. This is done to reduce the amount of data that must be processed.

As a second frame is brought into a block of chips, it also undergoes a noise-reducing convolution. The resultant image is then subtracted from the preceding one (bottom left). This subtraction determines if there has been any movement.

Another convolution is then carried out on the image so that the system can pick up hidden information (bottom center). That image is then added to the original, thus creating an enhanced photograph (bottom right).



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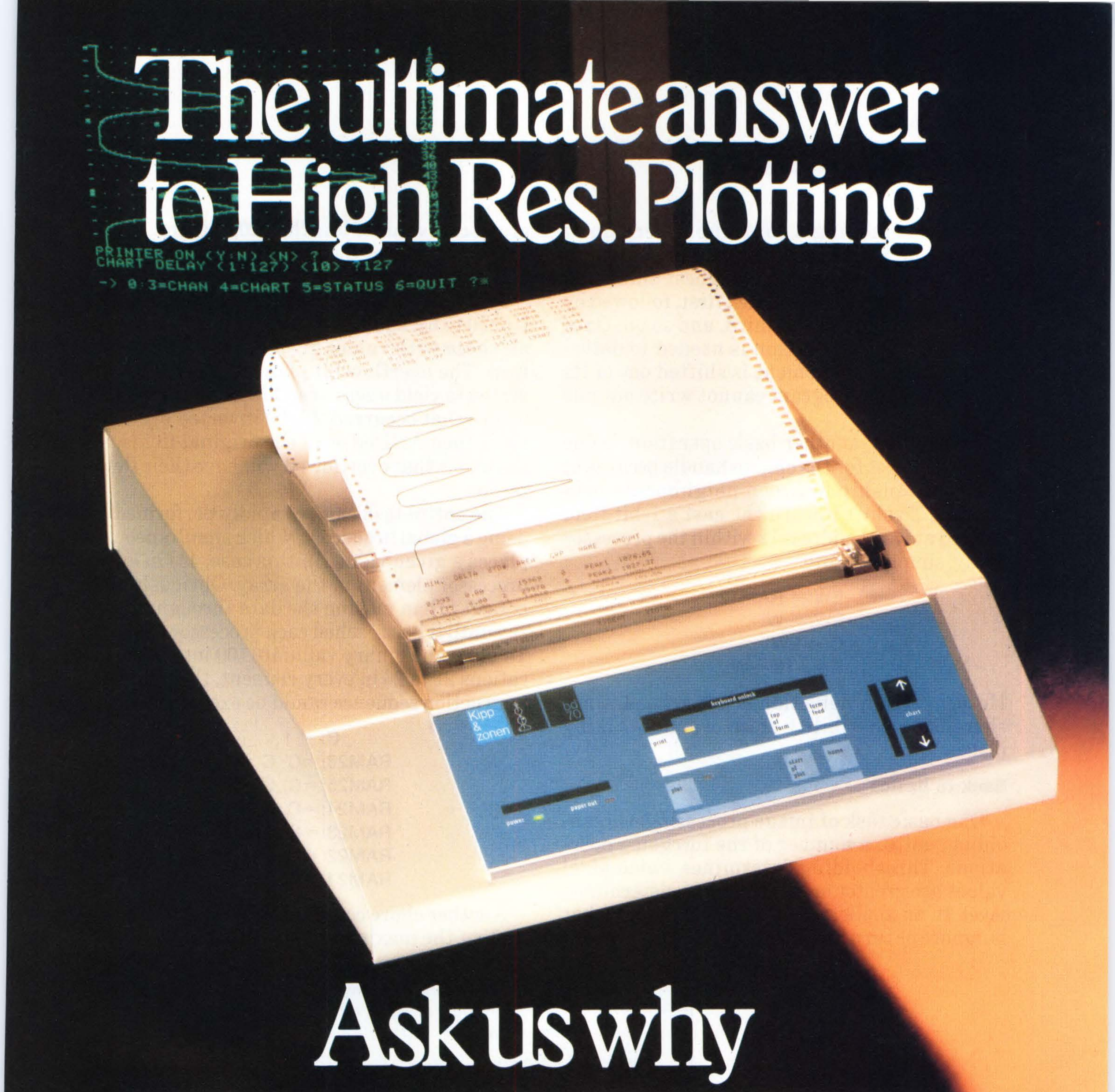


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manner as moving a contiguous section of memory on a standard machine. To shift upward in memory index, the highest numbered element in the block is shifted first, followed by the second highest, the third, and so on. Once again, overflow detection is needed to determine whether an element is shifted out of its field, since the program cannot write outside the field.

Translation, another basic operation, is one of the simplest for the chip to handle because of the relationship between neighboring processors. To shift toward the east a 1-bit field located at RAM address 12 within the processor array, simply execute:

```
EW:= RAM12
EW:= W
C:= EW
RAM 12:=W
```

Here, overflow detection is not needed, since there is no possibility of an overflow taking place.

### Back to basics

One basic task of image processing, thresholding, unites a number of the foregoing operations. Thresholding determines which pixel values are greater or less than a predetermined level. In an application that needs to zero (that is, ignore or turn into zeros) all the pixels with a gray-scale value of less than 20, the first step is to make a copy of the image's data base, which is destroyed as the task is carried out.

Since a 6-bit field can represent numbers from 0 to 63, adding 44 to every pixel will cause all those with values greater than 19 to overflow. The overflow bit plane must then be inverted to yield a zero overflow bit in every pixel where that occurred. If the inverted overflow bit is then ANDed with the original fields, all the pixels that overflowed will have their fields zeroed.

The entire task can be rapidly performed by using a global braodcast, which simultaneously places a given value (in this case, 44) in every processor element in the array. Obviously that is faster than moving the data through the array until it has reached each processor element. To place the binary value 101100 into RAM locations 21 to 26 in every element, the following instruction sequence would be executed:

```
C:= 1
RAM26:=C, C = 0
RAM25:=C, C = 1
RAM24:=C, C = 1
RAM23:=C, C = 0
RAM22:=C, C = 0
RAM21:=C
```

Another chore common to image processing, finding the maximum pixel value in an image,

**Program 1. Establishing the highest-intensity pixels**

```
COMMENT: Initialize EW = 1
NS:=0, EW:=0, C:=1
NS:=0, EW:=C, C:=0

COMMENT:  Loop from MSB to LSB and deliver MAXVAL as bit serial output on GO
for n = 8 to 1 do
{
    NS:=RAMn, EW:=EW,C:=0          (Read next bit from RAM into NS)
    NS:=NS, EW:=EW,C=CY            (Form NS "and" EW)
    NS:=C, EW:=EW, C:=0            (Send result to GO from NS)
    if GO=1                        (Bit n of MAXVAL = 0 from NS)
    {
         EW:=EW                    (EW retains present value)
    }
    if GO=0                        (Bit n of MAXVAL = 1)
    {
         EW:=NS                    (EW set to 0)
    }
}
```

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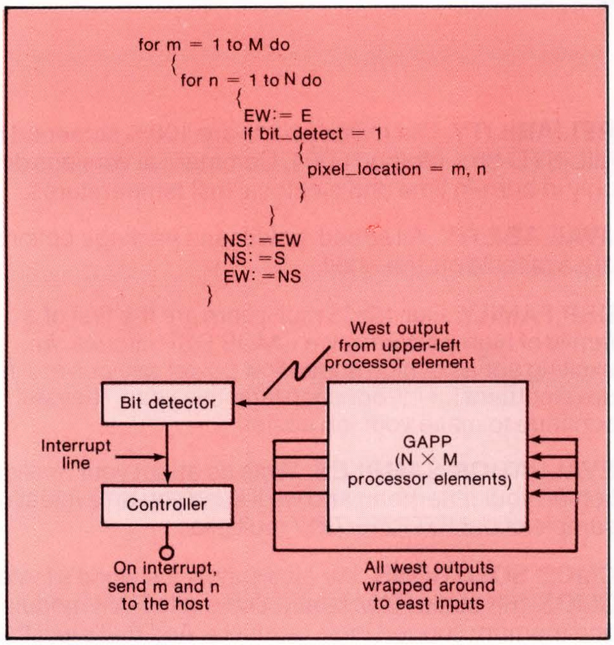
CIRCLE 146

lends itself to the architecture of the systolic array. A number of algorithms could be used, depending on the desired objective. One takes advantage of the chip's Global Output (GO) line to furnish the value of the highest-intensity pixel (MAXVAL) within a O(k) interval (Program 1).

Once the algorithm is completed, the processor elements wth the maximum intensity value will have a logic 1 stored in their EW registers. The same algorithm can also determine the value of the lowest-intensity pixel (MINVAL) by first making a negative from the image, which is accomplished by simply inverting each bit of the pixel.

In some instances, it is desirable to determine the location of the highest-intensity pixels. The only additions needed are a bit detector (a simple comparator) and another algorithm (Fig. 3).




**3. By running a specific algorithm, a comparator serving as a bit detector can determine the location of pixels with the greatest gray-scale values. When a logic 1, which denotes such pixels, is observed, the controller is interrupted and sends the location of the bit to the host.**

The comparator simply accepts inputs from the array until a logic 1 is picked up. It then sends an interrupt to the controller, which locates the highest-intensity pixels by counting the number of zeros that preceded them.

### Stand and be counted

Counting the number of pixels that are displayed at maximum intensity is also done relatively simply and quickly with the array. Traditional processors would take O(N × N) operations, but an array-based binary tree approach performs a number of additions in parallel, hence requiring only O(log N) operations. Several pairs of numbers are added within all columns of an array, then pairs of these results are added in parallel. The resulting data flows upward through the block of arrays until the sum reaches the top processor element of each column.

At that point, a second algorithm sums the values in the rows until the total for the entire block is contained in the upper-left-hand processor element. Since translation operations cause data to shift into the edge of the array, these inputs must be set to zero so that the external data contributes zero to the sum. A binary-tree summation of a column of 64 numbers first assumes that the numbers are 8-bit pixel values. They are also assumed to reside in RAM locations 1 for the LSB to 8 for the MSB (Program 2). The partial sums are stored in RAM locations 1 through 14.

### Straightforward convolutions

Convolution is one of the most important jobs performed in image processing. It uses the previously described neighborhood algorithm to determine new values for pixels, thereby enhancing an image. Convolutions are put to work along the entire range of image processing, from upgrading old photographs to improving the definition of edges in a robotic vision system.

Convolution is characterized by a high level of parallelism, so it is well suited to the systolic array. Typically, a template of new values is placed over the values of the camera image. Global broadcasting distributes the template. The objective is to move the sum outward in a spiral from the center of the template, which is

## Systolic image processor

the location of the new pixel value, to each of the matrix elements that reside under the template. At each matrix a location multiplication is performed, and the result is added to a traveling sum. The image resulting from this convolution is enhanced. Since all of the summations occur simultaneously, the parallel array processor handles the job at a good clip.

Histograms, which count the number of pixels containing particular gray-scale values, can make adjustments for changes in lighting, as well as let systems adjust to very light or very dark images. In that way they improve visual information at either end of the intensity spectrum.

The process is handled as quickly as the array's global-sum operation counts the processor elements. The elements to be counted are first identified by broadcasting a gray-scale value to every processor element and comparing it with the pixel value stored in each. Matches to the image stored in RAM locations 1 to 6 are determined by using a specific algorithm (Program 3). Various values are broadcast to create series of "bins," with different pixel levels sorted into the appropriate bins.

After this task is finished, every processor element that holds a pixel matching the broadcast pixel will have a logic 1 in RAM location 0. Before counting the number of pixels, a quick check for GO=1 will indicate if there were any pixels at all which matched the broadcast value. By determining the number of pixels in the various bins, the system can figure out whether the image is dark or light or contains a variety of shades, making adjustments as necessary.□

**Acknowledgment**

The authors wish to thank Martin Marietta Aerospace (Orlando, Fla.) for their contribution to the development of the GAPP architecture.

| **How useful?** | **Circle** |
|---|---|
| Immediate design application | 559 |
| Within the next year | 560 |
| Not applicable | 561 |

**Program 2. Binary-tree summing**

```
for m = 0 to 5 do
{
   c:=0
   for n=n1 to (8+m) do
   {
      NS:=RAMn, EW:=EW, C:=C
      NS:=NS, EW:=RAMn, C:=C
      for p=1 to 2** m
      {
         NS:=S, EW:=EW, C:=C
      }
      RAMn:=SM, C:=CY
   }
   RAM (M+9):=CY
}
```

**Program 3. Sorting pixels into bins**

```
NS:=0, EW:=0, C:=1
NS:=0, EW:=0, C:=1, RAM:0=C                     (Initialize RAM 0 = 1)
for n=1 to 6 do
{                                               (Broadcast bin bit n)
    NS:=0, EW:=0, C:=X                          (Where X is the value of
                                                 bin bit n)
    NS:=RAMn, EW:=C, C:=1                       (Read bit n of image
                                                 pixel)
    NS:=RAM127, EW:=EW, C:=1, RAM127:=SM        (SM = 1 if NS matches EW)
    NS:=NS, EW:=RAM0, C:=0                      (Read RAM 0 and compare
                                                 with RAM127)
    NS:=NS, EW:=EW, C:=CY                       (CY=1 if RAM 0 and
                                                 RAM 217 were both 1)
    NS=NS, EW=EW, C=1                           (If all six bits match,
                                                 then RAM 0 will continue
}                                                to contain 1)
```

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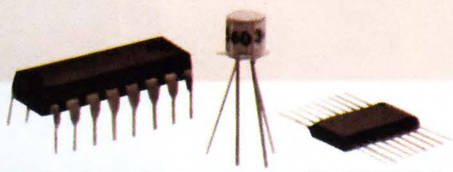

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**CIRCLE 148**

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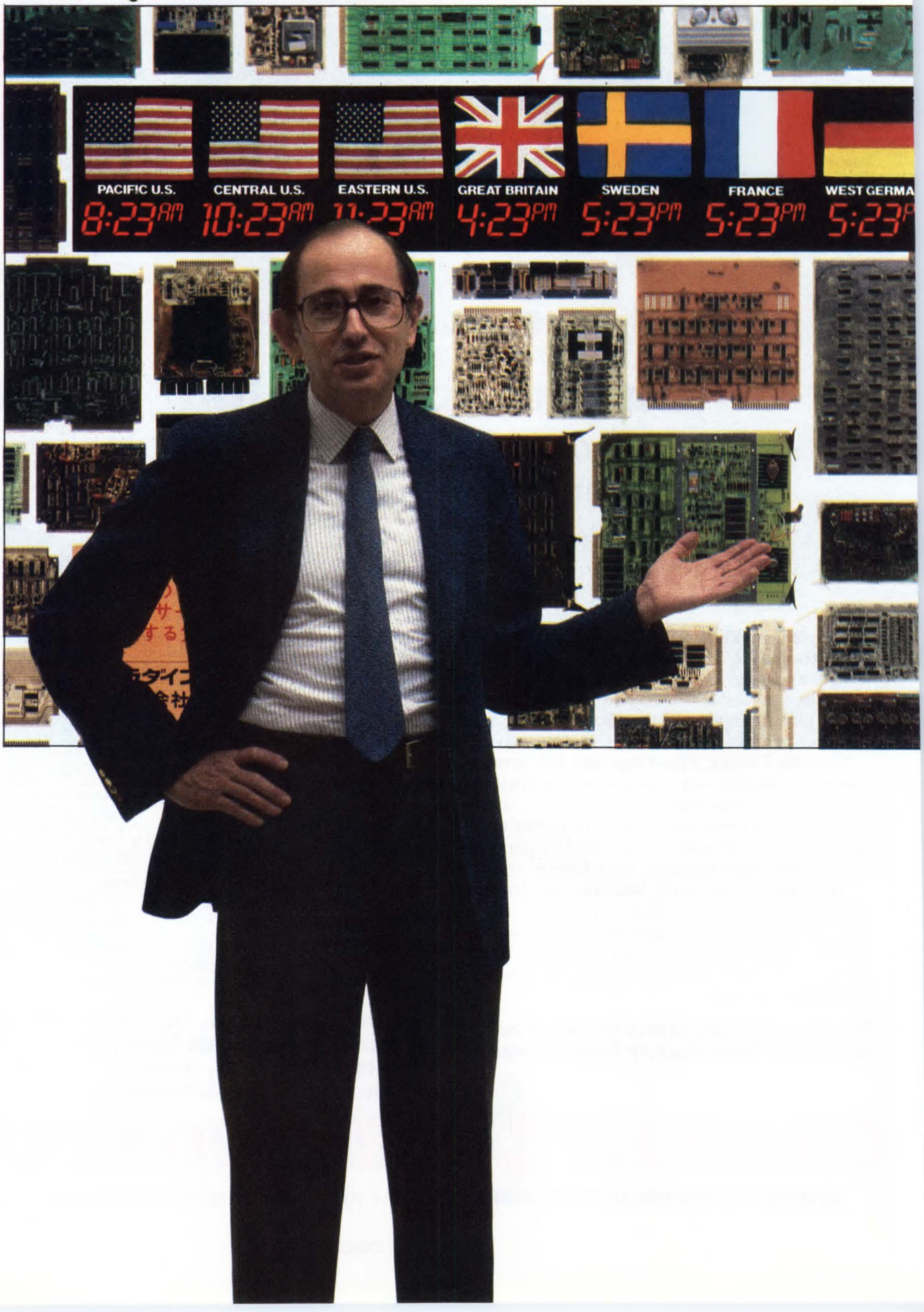

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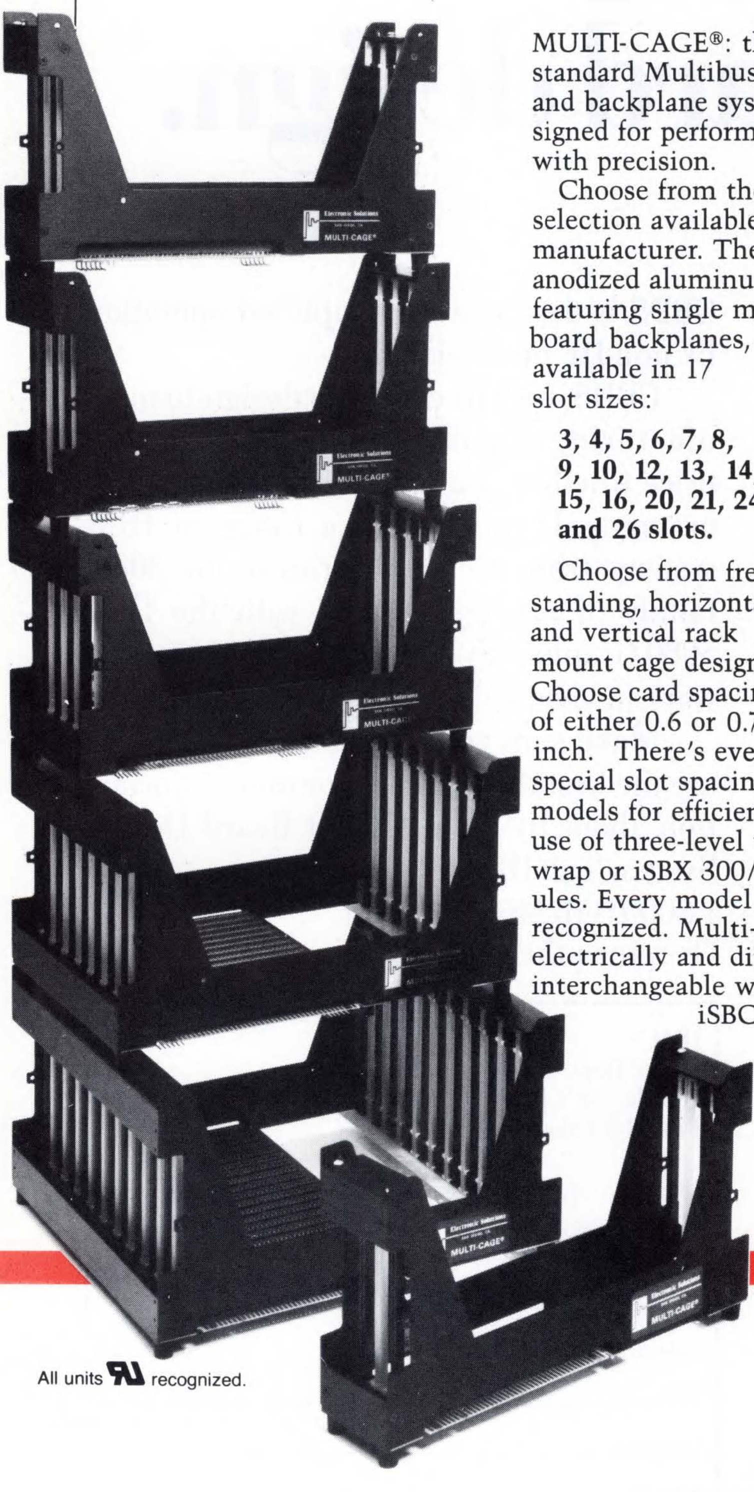

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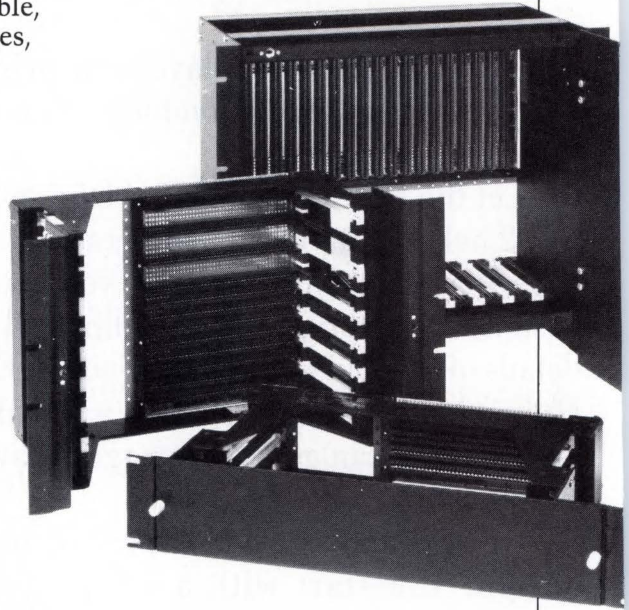

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**CIRCLE 181**

# Testing in-circuit ECL is just routine for digital oscilloscope

*Not only does a 1-GHz scope break the barriers to production testing of timing margins in ECL chips, it predicts out-of-specification performance as well.*

*This is the third in a series of articles highlighting the testing possibilities afforded by the HP 54100 1-GHz digital oscilloscope. The first detailed the scope itself (Oct. 18) and the second focused on the scope's advanced triggering mechanism (Nov. 1). The present piece addresses the problems of characterizing the performance of an ECL chip once it is installed in a circuit. A later article will discuss specific applications of the scope's logic-pattern triggering.*

The difficulty of testing high-speed ECL chips in a circuit often thwarts the engineer's need to know that their performance is within specification. Only when enough failures crop up to halt production does it seem worth the effort involved in verifying the logic's 1-ns transition times and propagation delays, as well as its stringent signal path requirements.

A 1-GHz digital oscilloscope, the HP 54100A/D, makes a host of measurements almost automatically, simplifying such jobs as characterizing ECL chips in situ. Measuring transition times, propagation delays, and loading effects takes just a small fraction of the effort that it used to. Furthermore, tasks till now impossible become practical. For example, the instrument helps predict an IC's performance even when it is operated outside of the manufacturer's specifications—in the so-called metastable state—to assist in bringing new certainty to asynchronous designs.

**Danny J. Oldfield**, Hewlett-Packard Co.

*Danny J. Oldfield joined Hewlett-Packard's Colorado Springs Division in 1978, after receiving a BSEE from the University of Tennessee. He spent a year as a customer service engineer and then moved to the division's research and development lab, where he put the finishing touches on the design of the HP 1727A high-speed storage oscilloscope. More recently, as a hardware development engineer, Oldfield contributed several analog designs to aid in developing the 54100 digitizing scope.*

To more fully appreciate the added capability of the new scope, consider the job of obtaining accurate, repeatable rise-time measurements with a conventional oscilloscope. A design engineer starts by adjusting the scope's vertical sensitivity and position controls in order to center a full-screen image of the signal. Here, the first problem arises: Adjusting the vertical sensitivity for a full screen typically means using a vernier, therefore losing the scope's calibrated voltage scale and complicating voltage measurements.

Next, the trigger level must be properly adjusted—trial and error is the only way to obtain a stable image because the control is analog. Then the horizontal sweep is adjusted for the fastest rate that still keeps the transition on screen. At the last, the engineer makes a mental note of the relative time at which the transition crosses the points at 10% and 90% of peak amplitude. The difference between the two is resolved to determine the rise time.

To further complicate matters, infrequent signals leave an image on the screen that is too dim to be measured. And slow slew rates, if they occur, invite large errors in estimating the 10% and 90% threshold-crossing points.

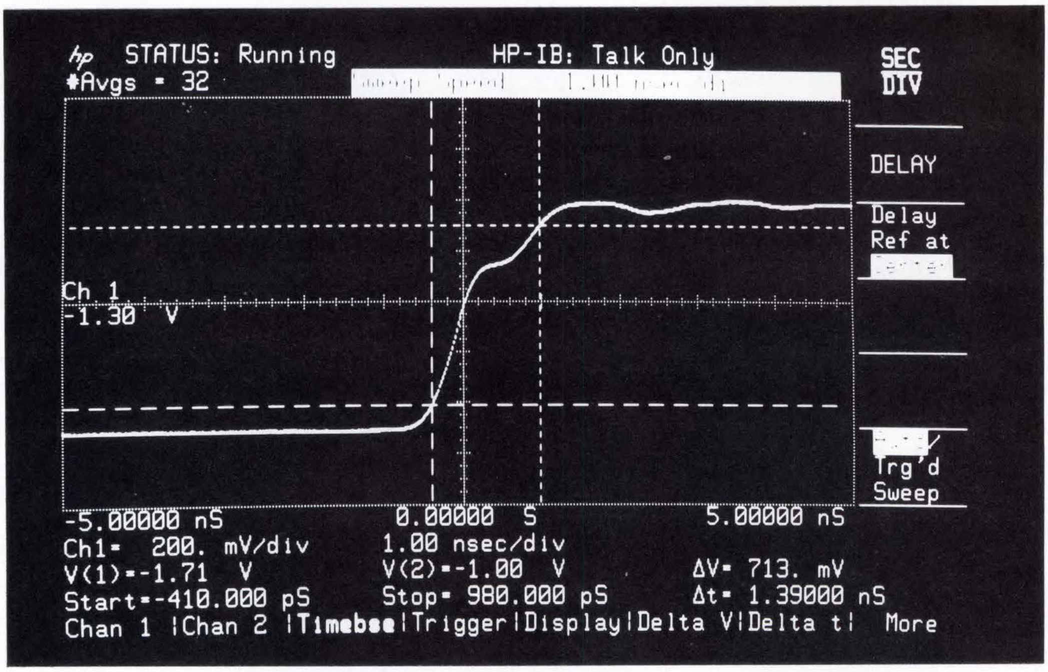
### Consider the alternative

Measuring rise time with the digitizing scope calls for the designer to simply press the ECL/TTL Preset button on the front panel. That automatically scales the display to 200 mV/division and sets the trigger level and vertical offset to −1.3 V dc. The second two settings ensure a stable trigger and center the waveform precisely on the screen. To make the actual measurement, the designer merely chooses the scope's parameter mode and presses the Rise-Time Measurement button. In an instant, the transition is automatically calculated (Fig. 1).

The swiftness of automated measurement belies the complexity of the steps taken to perform it. For example, the instrument must automatically place the horizontal markers that correspond to the 10% and 90% levels. To do so, it runs a histogram routine that calculates the signal's high and low levels and then positions the vertical markers where the signal intersects the 10% and 90% thresholds. Only when that is accomplished does the scope compute the rise (or fall) time as the difference between the two markers.

Although frequently not verified, parameters like rise time and propagation delay in ECL circuits cannot be taken for granted. In-circuit loading of chip outputs can significantly slow down edge speeds and cut critical time margins to zero. One way to ensure optimum performance is to first characterize a circuit's behavior and, if necessary, adjust the transition time to achieve the desired result. Increasing the drive current by lowering the pull-down resistor's value could be used to do so.

The correct compensation, however, can only be made when the chip is actually mounted on its printed circuit board, not by examining isolated components or calculating the adjust-




**1. ECL rise-time measurements can be made automatically with one of the algorithms stored in the HP 54100 high-speed digital oscilloscope. The ECL/TTL Preset button sets a −1.30-V dc offset and trigger point and scales the vertical deflection to 200 mV/division. The rise-time computation finds the maximum and minimum voltages and calculates the time between the 10% and 90% points.**

ment from formulas in a design manual. Actual circuit measurements are vital because the values of, say, the shunt capacitance that will determine an output's transition speed depends on the board and on component layout. But that capacitance is difficult to predict. Moreover, even when capacitance and other loading factors can be precisely determined, a designer should verify their effects. The digitizing scope does just that, and does it with ease.

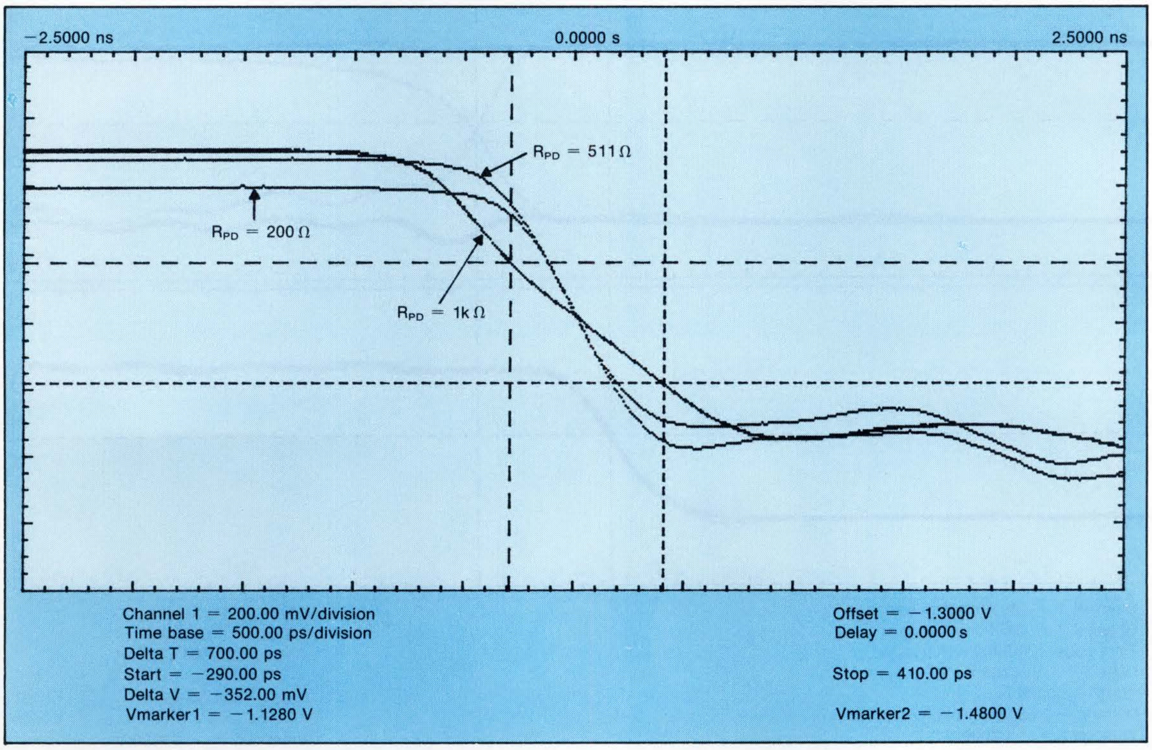
Additionally, the scope can store the output effects caused by different values of compensation. The output fall time of a 10H131 D-type flip-flop with several pull-down resistance values, when stored in the scope's memory, generates a family of curves for direct comparison and documentation (Fig. 2).

Another important high-speed parameter to check in circuit is propagation delay. That guarantees that fan-out and loading effects have not chipped away too heavily at timing margins. For the D-type flip-flop, for instance, propagation delay is the time between the clock input and an output change. To determine this measurement, the scope's display-persistence feature builds a composite waveform from the high and low levels of data being clocked in. The actual propagation time is then determined by setting a voltage marker to −1.3 V dc and putting time markers at the clock and data crossings (Fig. 3).

Propagation delay, which changes with loading, can be predicted to some extent with equations. Nevertheless, like transition time, in-circuit testing is the most reliable method of setting adequate margins.

**A matter of consequence**

A third measurement crucial to digital designers is setup time, the interval that valid data must precede a clock pulse. As with other ECL timing parameters, the designer must meet the manufacturer's specifications, which for reliable results, means knowing what temperature variations to expect and what impact they will have on timing tolerances. It is even



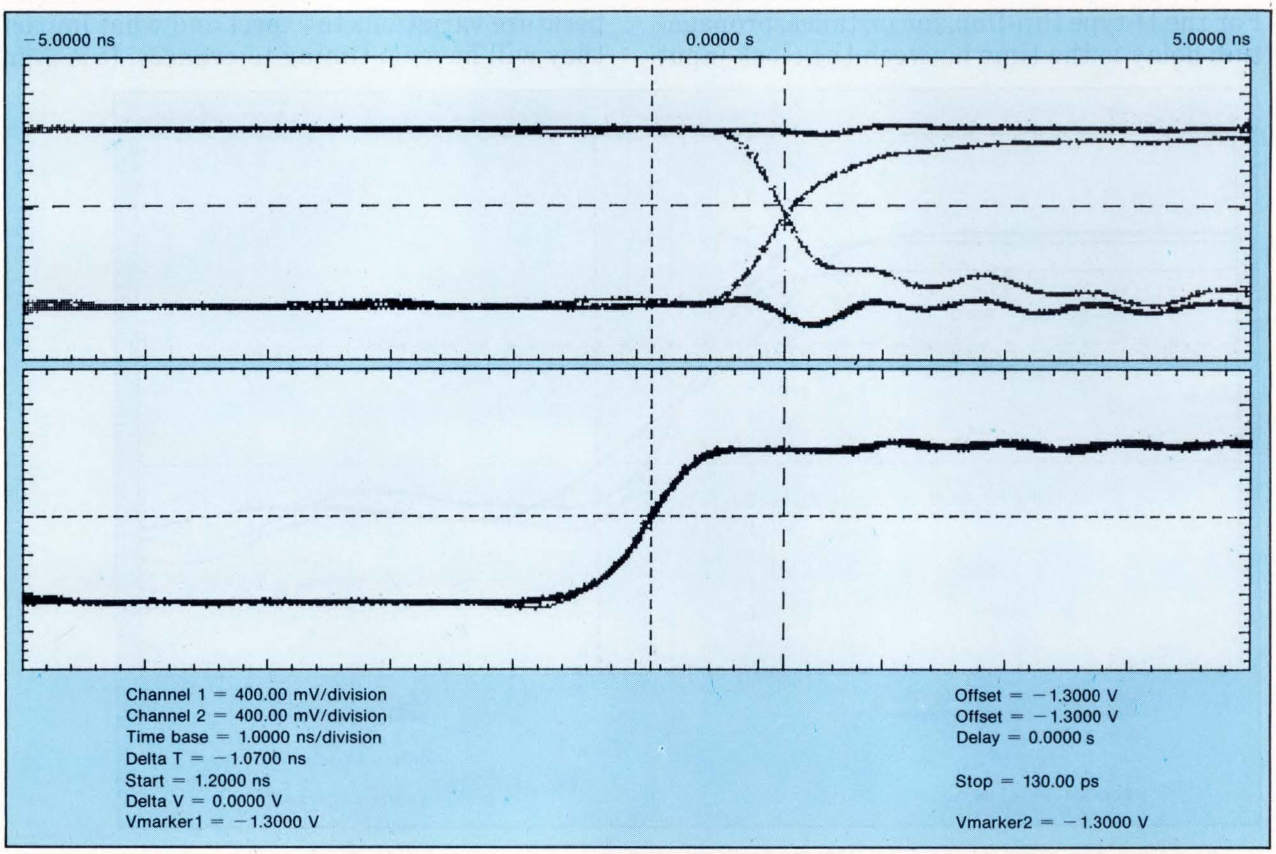

**2. The scope can store several waveforms for comparison and documentation, such as the output fall times for three different pull-down resistance values. The three are from a 10H131 D-type ECL flip-flop. Comparing waveforms lets designers pick the best pull-down resistor for a particular printed circuit board.**

important in some cases to anticipate the overall consequence of deviation from those specifications.

Consider measuring the setup time of the D-type flip-flop. According to a 1982 data book, its setup time must be at least 1.5 ns over a temperature range of 0° to 75°C. Signals are measured by the scope through its 1-GHz active miniprobes, which are connected as closely as possible to the device under test. Specifically, the upper channel (1) is connected to the chip's D input and the lower channel (2) to its clock input. Additionally, the scope's averaging mode is invoked to eliminate any uncorrelated noise from the measurement.

In the printed trace of the output, which is made by hooking up the scope to a plotter, voltage and time markers conveniently show where the measurements are made (Fig. 4). The difference in time ($\Delta_T$) between the two signals is 2.73 ns and is therefore well above the manufacturer's minimum specification. Furthermore, since the instrument automatically makes the measurement, a designer can easily place the test circuit in a computer-controlled temperature chamber. By doing so, the engineer could make the same measurement over the entire anticipated temperature range to identify, among other problems, any temperature-sensitive gates upstream of the flip-flop.

A somewhat different and far more difficult problem for a designer is characterzing a flip-flop (or other device) when its setup condition is violated. Why a designer would deliberately violate that condition may seem to be the obvious question, but it is actually unavoidable in logic synchronizers and in circuits that asynchronously refresh memories. Both circuits, because of their environments, cannot control the relative timing between certain events. In turn,




**3. The propagation delay measurement of a 10H131 flip-flop reveals that the difference in time between the clock input (lower trace) and the Q output (upper trace) is 1.07 ns. The scope's variable-persistence display simplifies measuring multiple-value waveforms by allowing the time that each data point is on the screen to be precisely adjusted.**

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those violations cause a device to operate anomalously, in what is called a metastable area. The data books are frustratingly uninformative about these states.

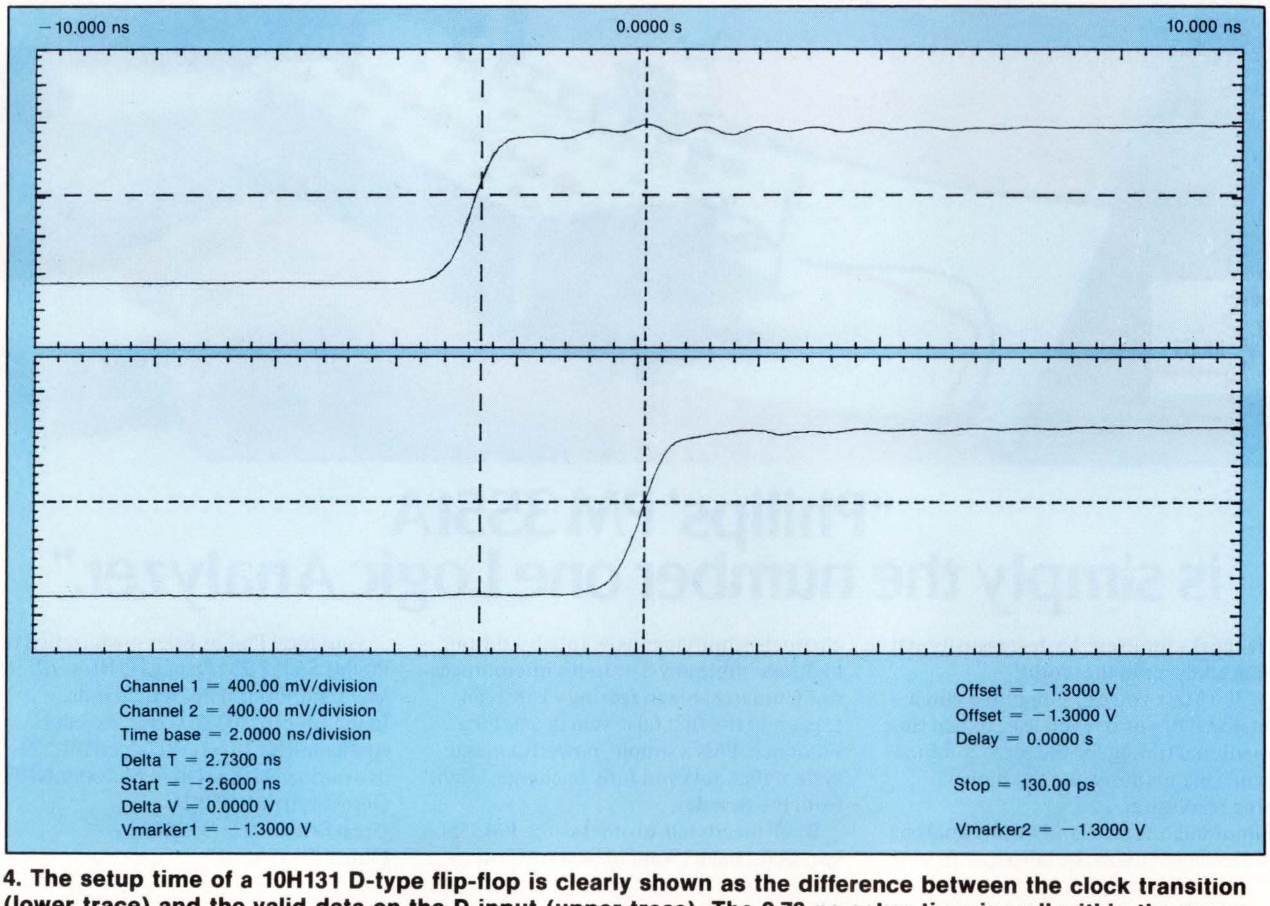
In a D-type flip-flop, which is often used in logic synchronizers and other asynchronous circuits, metastable operation is reflected in a distinct change in the output response: The output does not reach a valid logic state without a certain amount of hesitation or delay. Moreover, the amount of delay is not constant. As the output moves into the threshold region the response at first appears normal, but once there it may assume one of several different patterns.

In particular, sometimes the response appears near normal, swinging from one state to its opposite in a smooth line with little interruption. At other times, though, the transition reverses itself and returns to the original state, as if the data were never clocked. Finally, there is sometimes a significant delay following the transition into the threshold region before the output assumes a valid state. It is the last case that is of the greatest concern to system designers. They must build their circuits to tolerate the output's delay.

To accommodate this delay, designers must determine the maximum amount of time necessary for the output to settle to a valid logic state. Indeed, the need to pick a suitable delay margin is a major reason for characterizing a D-type flip-flop that operates metastably. To explore this phenomenon in greater detail, measurements were made on three functionally identical D-type flip-flops implemented in progressively faster ECL families: a 10131, 10H131, and 100131.

### In the margin

Attempting to characterize metastable outputs with a conventional scope would be futile: The small metastable error or the high concen-




**4. The setup time of a 10H131 D-type flip-flop is clearly shown as the difference between the clock transition (lower trace) and the valid data on the D input (upper trace). The 2.73-ns setup time is well within the manufacturer's recommended minimum of 1.5 ns.**

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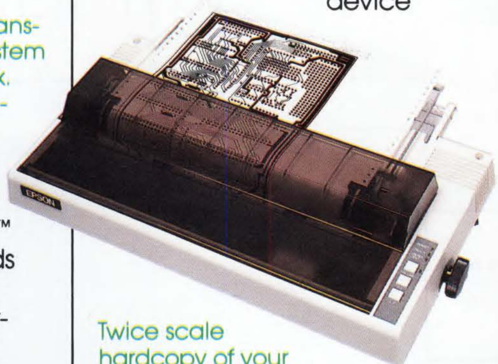

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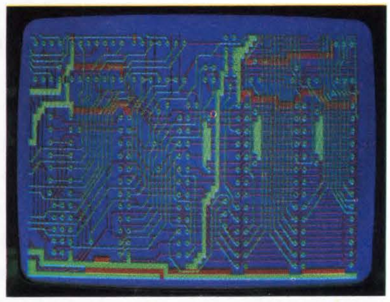

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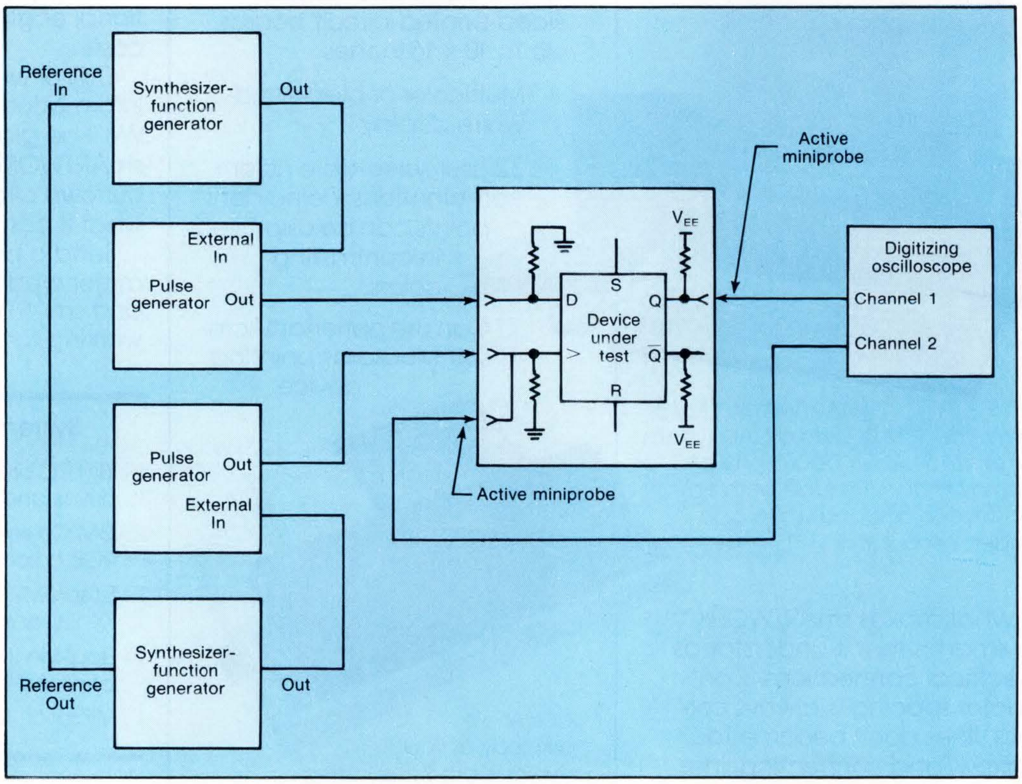
tration of data points in a short interval (and therefore small screen area) would cause the scope's display to bloom, obscuring details. On the other hand, the digitizing scope, with its infinite persistence mode, never blooms. It measures a data point, stores it in memory, and illuminates a corresponding pixel on its raster scan display. As more data points are acquired and added to memory, additional pixels are illuminated—with no chance of blooming.

To test the three chips, two high-stability (to within a few picoseconds) combination synthesizer-function generators (HP 3325As) are locked in phase. They trigger a pair of pulse generators (HP 8082As) having an output with a 1-ns rise time. This configuration of instruments applies highly synchronized, fast rise-time clock and data pulses to the device under test to achieve a high percentage of transitions in the metastable region (Fig. 5).

Initially, both synthesizers are set to 10 MHz and the outputs of the pulse generators adjusted to standard ECL voltage levels. In exploring the effects of skewing clock and data pulses, the resulting metastable window, (the time between clock and data that produces metastable operation) is found to be 75 ps. Undoubtedly, some of that time is caused by generator jitter, since experience suggests that this window is theoretically much narrower.

The clock and data transitions were first set for simultaneous transitions, to within the test instrument's 25 ps of resolution. Curiously, the metastable state is centered when the clock transitions occur 120 ps before the data transition. Although this seems contrary to the flip-flop's operation, three factors could cause the clock signal to precede the data: different on-chip delays that skewed the signals before they reached the logic-decision comparator; different thresholds between the clock and data comparators; or different probe lengths to the




**5. The test instruments for characterizing the metastable operation of an ECL device under test comprise two very stable synthesizer-frequency generators that trigger two 1-ns rise-time pulse generators. Clock and data pulse transitions drive the device at almost the same time, in violation of the chip's setup requirements, causing its output to respond anomalously.**

scope. (The third possibility seems unlikely because extra care was taken to calibrate probe-length errors to zero.)

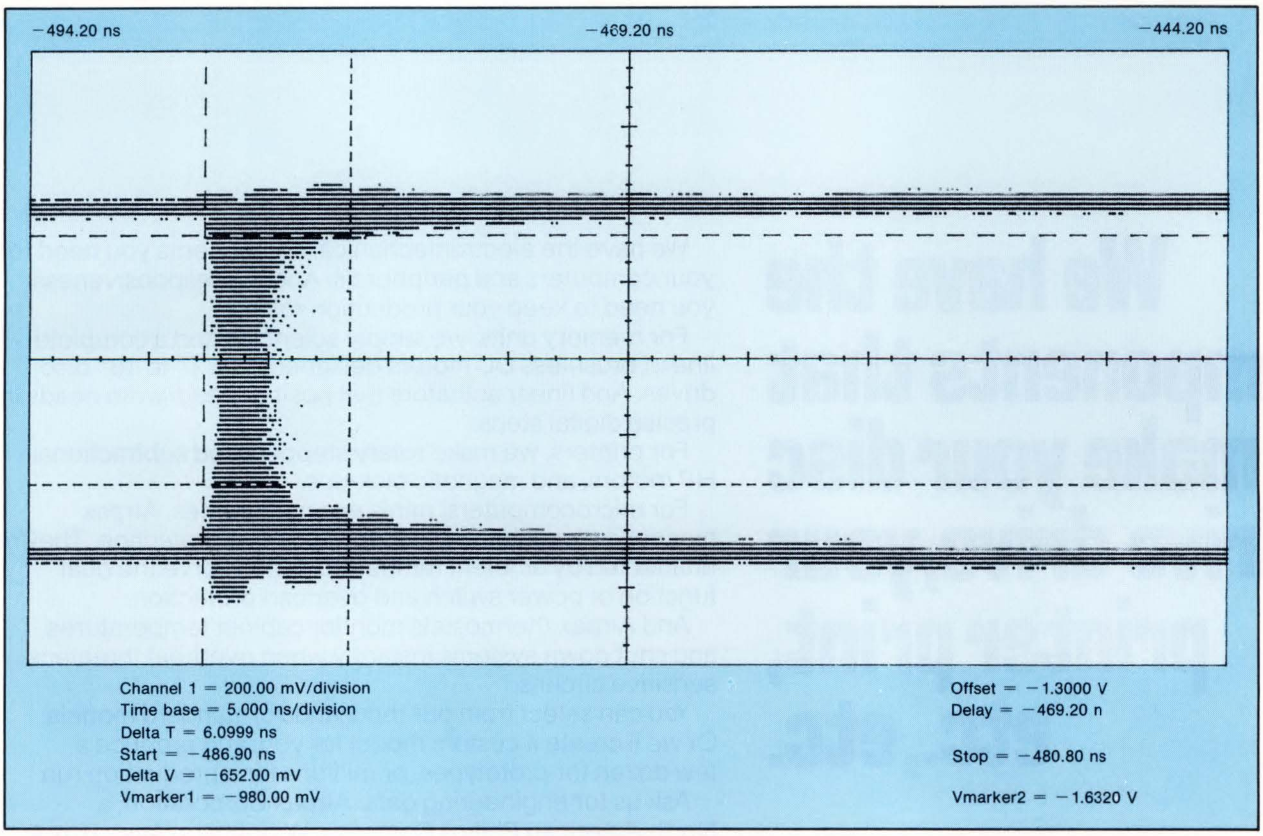
### A million tests a minute

Each chip was tested for 30 minutes, resulting in 30 million measurements apiece. The outcome shows that the 100131, although normally much faster than the 10H131, does not have a significant advantage in settling time when operating metastably. The latter chip, however, did exhibit greater ringing and overshoot. The settling times for the 10131, 10H131, and 100131 were 24.4, 6.09, and 5.8 ns, respectively.

The settling time was measured by first setting voltage markers to the maximum logic low and minimum logic high ECL levels. Then, time markers were placed at the points where a chip's output entered and left the metastable state. In other words, the markers measured the length of time that the outputs were in valid logic states (Fig. 6).

A statistical analysis reveals that metastable delay time decays in a log-normal fashion, a characteristic common to many natural events. The implication is that the probability of an output remaining metastable decreases exponentially with time. The same conclusion also follows intuitively from the fact that random noise within a chip's comparators would always tend to swing the output to one or the other valid logic state.□

| **How useful?** | **Circle** |
|---|---|
| Immediate design application | 562 |
| Within the next year | 563 |
| Not applicable | 564 |




**6. The metastable output response of a 10H131 D-type flip-flop has a settling time of about 6.1 ns. That represents the minimum delay that a designer should allow before reading the chip's outputs. The delay is the main consequence of violating the flip-flop's data-setup requirement.**

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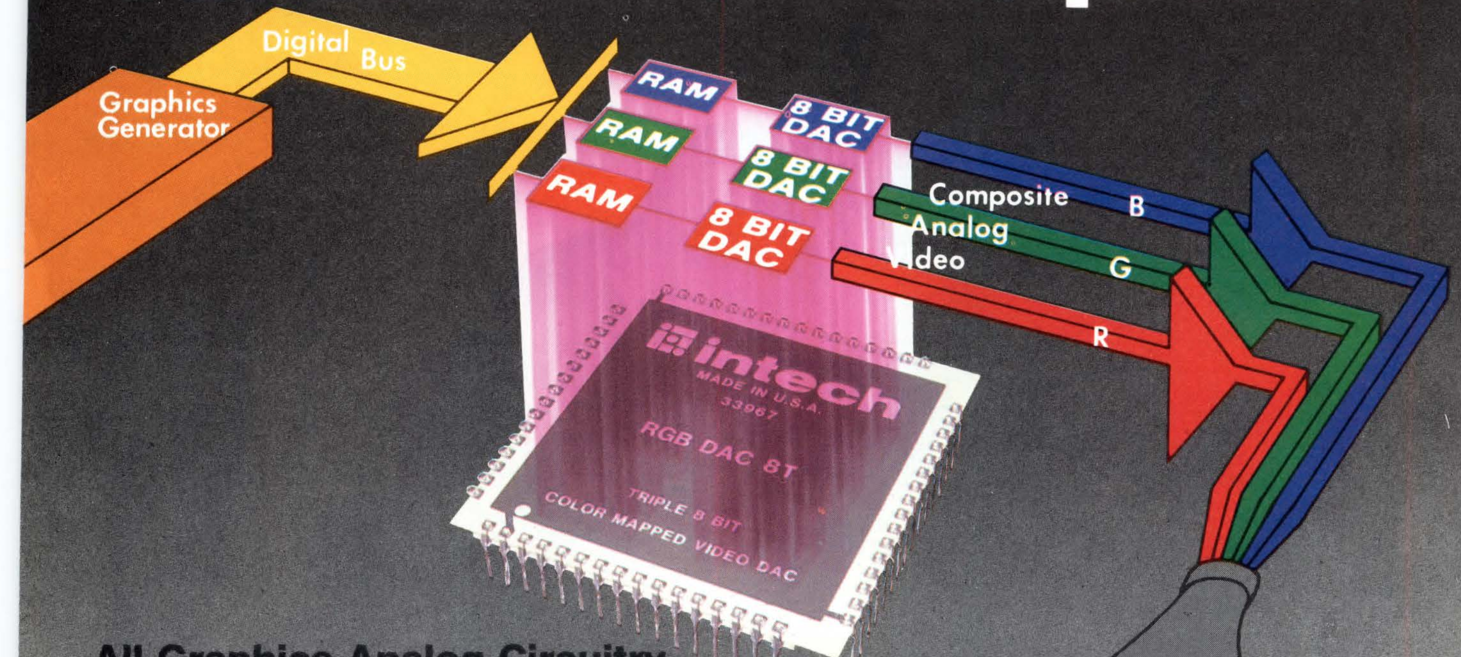


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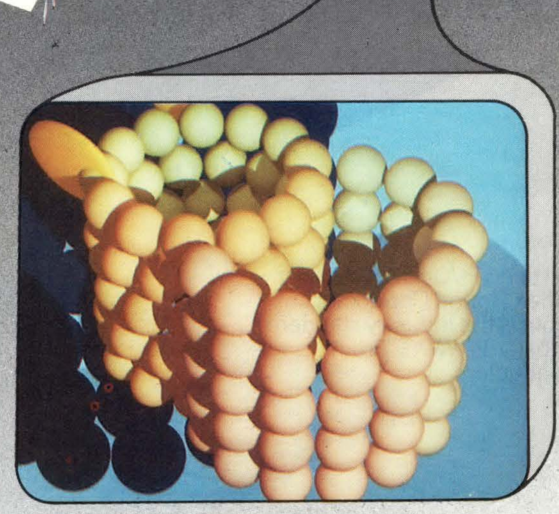

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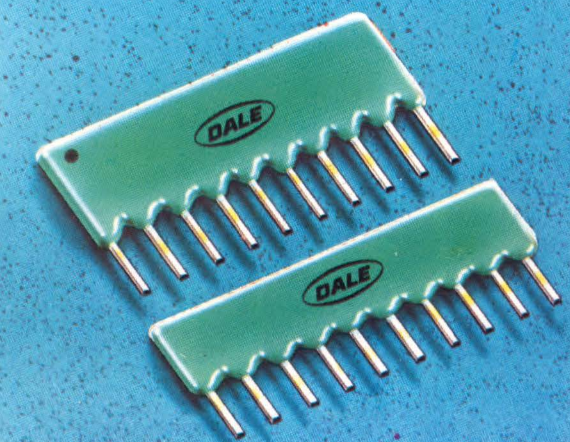

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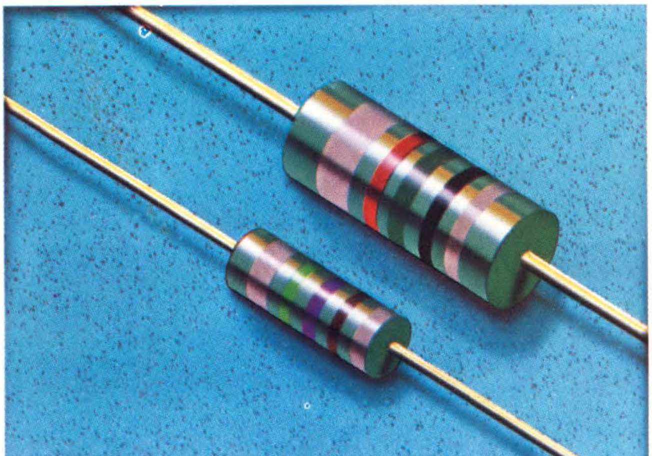

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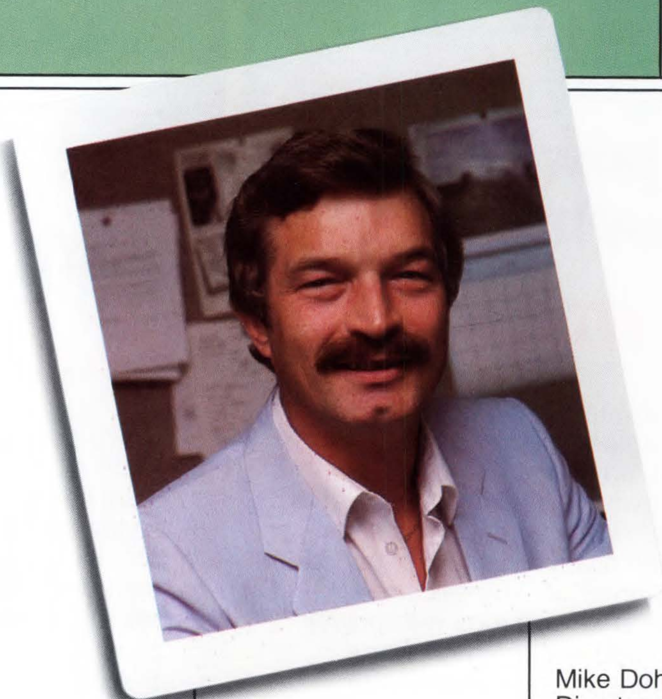

Mike Dohler,
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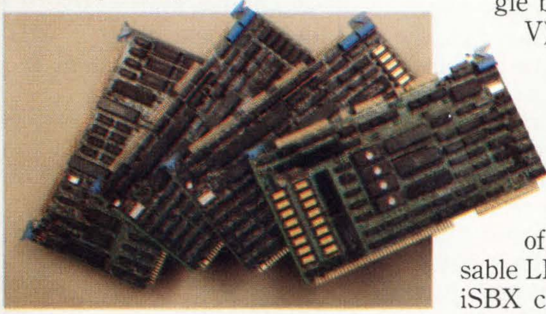

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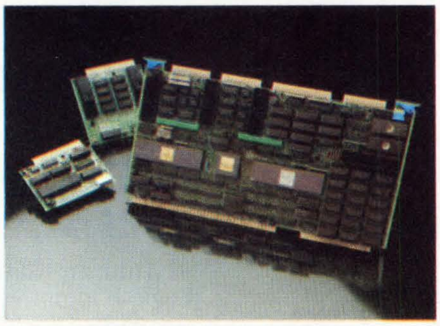

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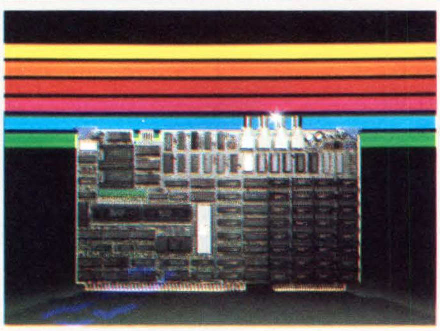

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# DESIGN SOLUTIONS

## Software routine converts shaft encoder output from Gray code into binary

**John T. Hannon**
Research and Design Engineer
Celanese Fiber Operations
PO Box 32414, Charlotte, N.C. 28232

If an 8080 or 8085 microprocessor is handy within a system, a small portion of its time can be spent converting the Gray code output of a shaft encoder into more conventional binary code. Gray code is preferred for most encoders, since only one bit changes at a time, avoiding any ambiguity.

For this application, a software routine (see the program) borrows from the technique used for hardware conversion, namely, a series of exclusive-OR gates. In hardware logic, the conversion of each bit (with the exception of the most significant bit) depends on the previously converted bit. To do the same thing with software, each bit must be converted separately, starting with the most significant bit. A bit-location word sets that step into a software loop, and every time the software completes the loop, the location bit moves through the word, one bit at a time.

The program first sets the location bit to bit 7 by inserting a logic 1 into that bit position and logic 0s into all the other positions (see the figure). Next the loop counter is set to 7 and the Gray code word is ANDed with the bit-location word, a step that makes bit 7 of the binary word

**Program for a Gray code–to-binary converter**

| LOC | OBJ | SOURCE STATEMENT | | | |
|---|---|---|---|---|---|
| 0000 | 1680 | GRYBIN: | MVI | D,80H | ; Set up location bit |
| 0002 | 1E07 | | MVI | E,07H | ; Set up loop counter |
| 0004 | 79 | | MOV | A,C | ; Get Gray word |
| 0005 | A2 | | ANA | D | ; AND with location bit |
| 0006 | 47 | | MOV | B,A | ; Store partial binary word in register B |
| 0007 | 7A | GRAY: | MOV | A,D | ; Get location bit |
| 0008 | 0F | | RRC | | ; Shift right by one bit |
| 0009 | 57 | | MOV | D,A | ; Return location bit to register D |
| 000A | 78 | | MOV | A,B | ; Get binary word |
| 000B | 0F | | RRC | | ; Shift right by one bit |
| 000C | A9 | | XRA | C | ; Exclusive-OR with Gray word |
| 000D | A2 | | ANA | D | ; AND with location bit |
| 000E | B0 | | ORA | B | ; OR with partial binary word |
| 000F | 47 | | MOV | B,A | ; Store back in register B |
| 0010 | 1D | | DCR | E | ; Decrement counter |
| 0011 | C20700 | | JNZ | GARY | ; Jump back if not zero |
| 0014 | 78 | | MOV | A,B | ; Send final result to accumulator |
| 0015 | C9 | | RET | | |
| | | | END | | |

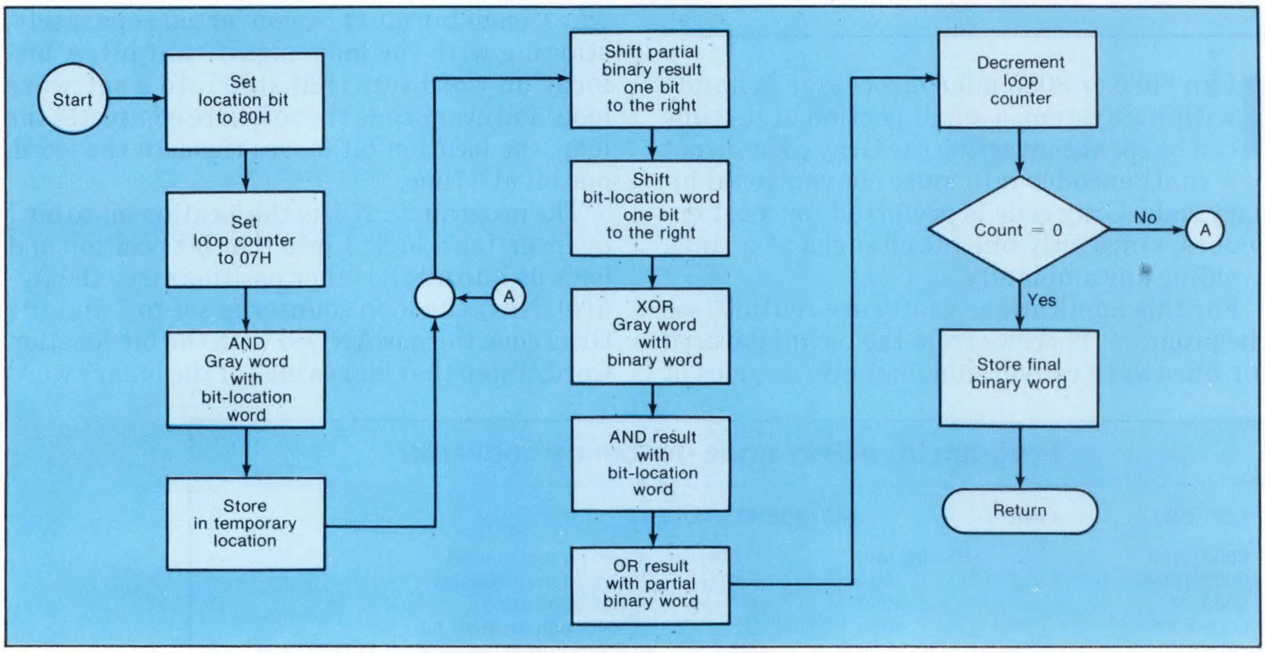
the same as bit 7 of the Gray code word. The partial binary word is then temporarily stored.

The routine then enters the loop, starting with bit 6 and repeating seven times, each time shifting the previous partial binary result one bit to the right. That shifting resembles the situation when each exclusive-OR gate in the hardware version supplies one of the inputs for the next gate in line. The stored result of the partially complete binary number is not shifted.

The loop shifts the location bit one position to the right and exclusive-ORs the shifted word and the Gray code word. The location bit and the exclusive-ORed result are ANDed, making all bits logic 0s except the bit that is selected at that time.

At this point, the result is ORed with the partial binary word and the partial result is then stored. When the loop counter decrements, it jumps back and repeats the same procedure for the next bit position, unless the counter is set at zero.

When the counter reaches zero, all bits have been operated on. The routine exits the loop and stores the final binary result. (If the software serves as a subroutine, the program returns to the main routine.) Although the program is designed for an 8-bit conversion, it can easily be expanded if a larger shift encoder is used.




**The software routine for converting the Gray code output of shaft encoders into binary words sets up a loop that converts each bit separately. Intermediate results are temporarily stored until all bits have been converted.**

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CIRCLE 193

# V-f converter doubles as clock and input of stable sine-wave source

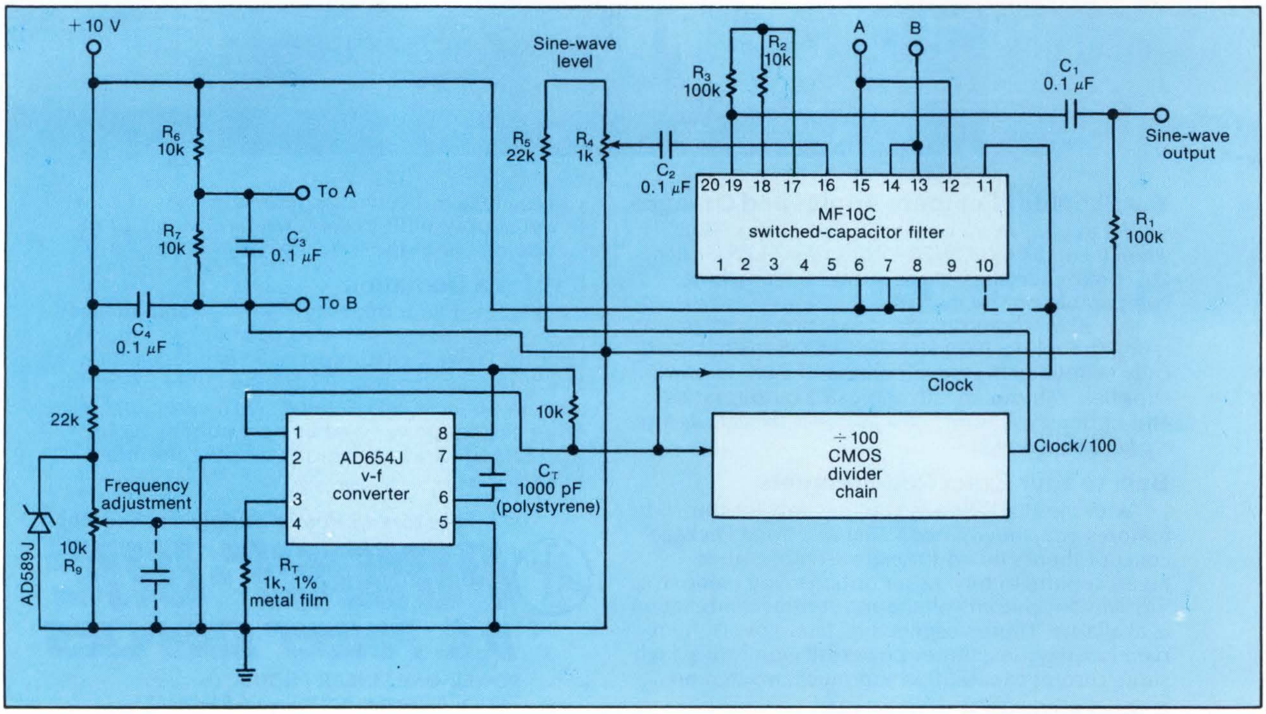
**Walt Jung**
Consultant
Analog Devices Semiconductor Inc.
804 Woburn St., Wilmington, Mass 01887

A voltage-to-frequency converter makes a versatile clock source for a switched-capacitor filter, such as the MF10C, but it can be even more valuable if its output serves as both the signal source and the clock. Such a combination of converter and filter makes a frequency-agile sine-wave source that has a very precise and predictable output.

In the circuit (see the figure), the AD654J v-f converter operates from a single supply and has a square-wave output of up to 500 kHz. That output directly becomes the filter's clock input and is also divided down by a factor of 100 to form the filter's signal input.

The frequency of the v-f converter, here 100 kHz, is determined by resistor $R_T$, capacitor $C_T$, and the applied 1-V control voltage. The voltage is set by $R_9$, a 10-kΩ potentiometer, and is stabilized against changes in the supply voltage via a 1.235 band-gap reference diode, an AD589J.

With a 10-V supply, the v-f converter produces a 10-V pk-pk square-wave output, which drives the filter. Here that filter is set to a



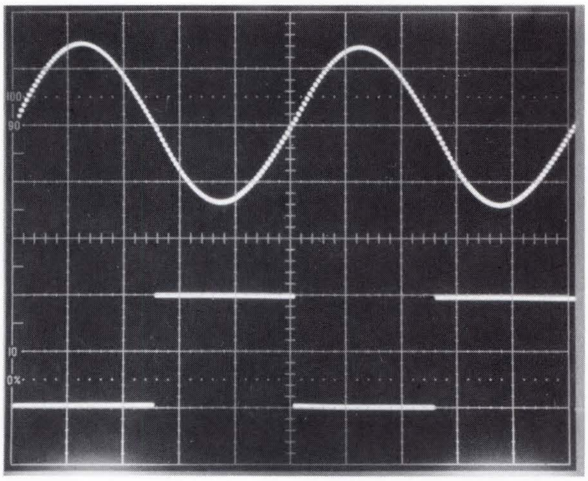

**1. A v-f converter, the AD654J, acts as both the signal input and the clock for a switched-capacitor bandpass filter. The resultant circuit is a frequency-agile and easily programmed sine-wave source that features precise and automatic tracking.**

clock-to-center-frequency ratio of 100:1, accomplished by tying its pin 12 to a middle supply voltage level. (A 50:1 ratio is available by tying the pin high.)

The output also drives a 100:1 CMOS divider that produces a symmetrical 1-kHz square wave. That signal is fed to the filter through resistors $R_4$ and $R_5$.

The filter is in its bandpass, or 1a, mode and delivers its output from pin 19. Two resistors, $R_2$ and $R_3$, control the gain and Q. An analog path to ground is furnished by a resistive divider, formed by $R_6$ and $R_7$, which is bypassed by capacitor $C_3$.

The circuit's strength is not in its overall dynamic range or signal purity but rather in its easy tunability and freedom from bouncing and uncertain settling time. Programming can be both fast and precise, the latter due in part to the v-f converter's good linearity. At an output level of 1 to 2 V rms, total harmonic distortion is on the order of 2%, limited by the clock noise.



**2. The sine-wave output, shown at 1 V/division (top), exhibits just 2% total harmonic distortion (THD) for a square-wave input of one-hundredth the clock frequency, shown at 5 V/division (bottom). The horizontal scale is 200 μs/division.**

# Pseudo-sine-wave circuit generates FSK tones without discontinuities

**Mike Huddleston**
Senior Project Engineer
Scientific-Atlanta Inc.
MS ATL 5-A
PO Box 105038, Atlanta, GA. 30348

A circuit that combines a crystal oscillator, a digital divider, and a shift register generates audio frequency-shift-keying (FSK) signals with the unusual combination of crystal-controlled accuracy and continuous-phase switching.

The common methods for generating audio-frequency signals fall short of fully achieving that objective. For instance, in the quest for high precision, when a variable modulus counter is hooked to a crystal-controlled oscillator to switch among various audio tones, the price of precision is phase discontinuities whenever the frequency is changed. One result is that the FSK signal takes excessive bandwidth.

The usual alternative, which ensures smooth keying, is to switch an audio generator's timing components—resistors and capacitors. The problem here is frequency inaccuracy, aggravated by aging and temperature drift. In addition, the high-frequency aspects of glitches caused by the switching can increase the required transmission bandwidth and play havoc with phase-locked-loop FSK demodulators.

The combined circuit (see the figure) uses two

74C193 4-bit counters, $IC_2$ and $IC_3$, to divide the output of the crystal oscillator by any integer between 1 and 255. The output of the counters is applied to $IC_4$, a 4015B dual 4-bit shift register connected as a twisted ring counter. The various outputs of the shift register are combined, through a precision resistor network, to produce a pseudosinusoid whose frequency is 1/16 of the input frequency, and which is a stair-step approximation of a sinusoid with 16 discontinuities per period.

With 1% precision resistors, the circuit's even-order harmonic output is too low to be measured. Odd-order harmonics—from 3 to 13—are suppressed by at least 30 dB. The 15th and 17th harmonics, generated by the stair-step discontinuities, are about 15 dB below the fundamental. If they become a problem, they can be handled easily by a low-pass filter.

Although a crystal oscillator is shown, any square-wave source is suitable. However, for reliable performance, the frequency of either should be between 1 and 2 MHz. The crystal frequency is based on the desired output. The latter is equal to the crystal frequency divided by 16(N+1), where N is the binary input to the dividers. For example, a 1.2-MHz crystal will generate FSK frequencies of 1070 and 1270 Hz, since it gives near-integer values for the divisor N. From the formula, the values are 69 and 58 (010000101 and 00111010) respectively. The insert shows the appropriate wiring for the dividers' inputs.

Because it is a CMOS device, the shift register's output will drive the resistive combining network with a rail-to-rail swing. The pseudosinusoid will swing from ground to +5 V and the output will exhibit an impedance of approximately 4200 Ω. Although 1% resistors are shown, the nearest 5% values can be substituted if more even-order harmonic content can be tolerated.

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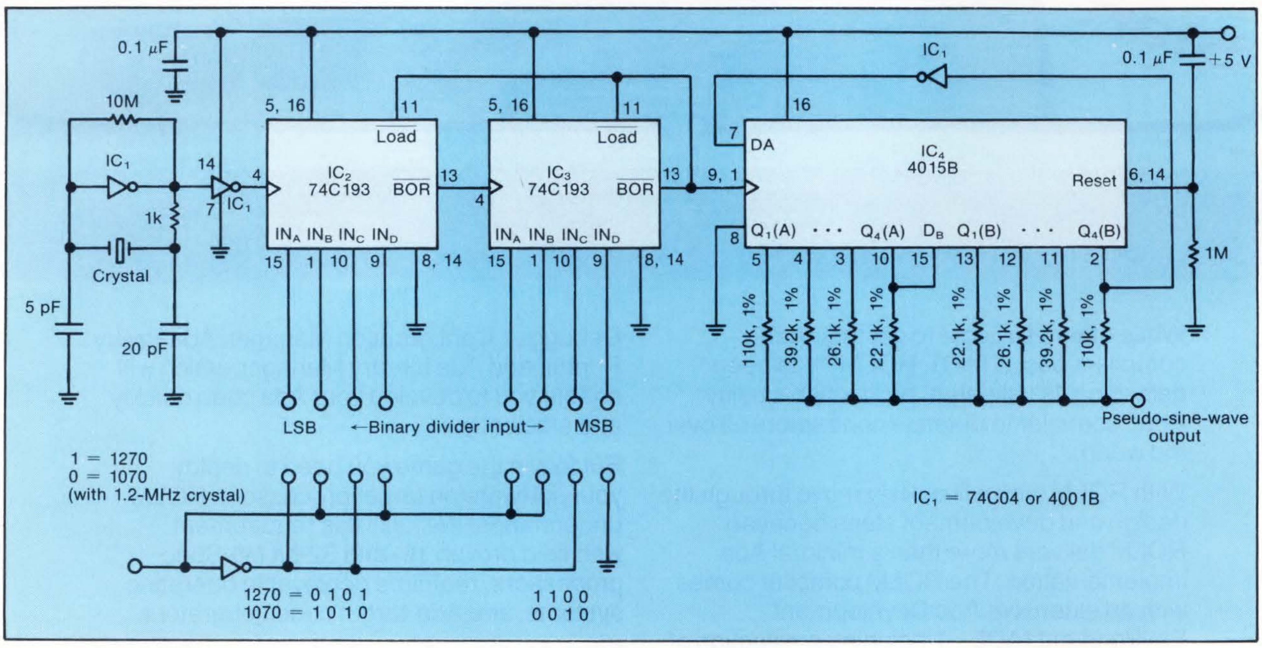
*PROM and octal latch make a simple, versatile 7-bit counter*

**Vittal Rao,** Digital Systems Section, ISRO Satellite Centre, Airport Road, Vimanapura P.O., Bangalore 560 017, India.




**A useful adaptation of two rather common circuits switches between two or more sinusoidal frequencies without any abrupt phase variations.**

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CIRCLE 197

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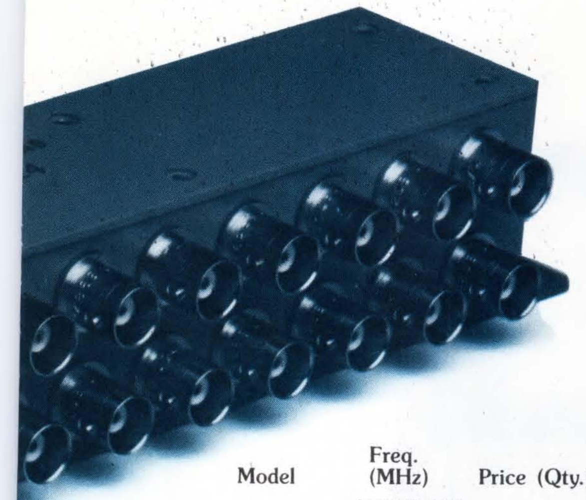

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| | **2 WAY-90°** | | |
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| PSCQ-2-3.4 | 3.0-3.8 | 16.95 | (5-49) |
| PSCQ-2-6.4 | 5.8-7.0 | 12.95 | (5-49) |
| PSCQ-2-7.5 | 7.0-8.0 | 12.95 | (5-49) |
| PSCQ-2-10.5 | 9.0-11.0 | 12.95 | (5-49) |
| PSCQ-2-13 | 12-14 | 12.95 | (5-49) |
| PSCQ-2-14 | 12-16 | 16.95 | (5-49) |
| PSCQ-2-21.4 | 20-23 | 12.95 | (5-49) |
| PSCQ-2-50 | 25-50 | 19.95 | (5-49) |
| PSCQ-2-70 | 40-70 | 19.95 | (5-49) |
| PSCQ-2-90 | 55-90 | 19.95 | (5-49) |
| PSCQ-2-120 | 80-120 | 19.95 | (5-49) |
| PSCQ-2-180 | 120-180 | 19.95 | (5-49) |
| PSCQ-2-250 | 150-250 | 19.95 | (5-49) |
| PSCQ-2-400 | 250-400 | 19.95 | (5-49) |
| PSCQ-2-450 | 350-450 | 19.95 | (5-49) |
| ZAPDQ-2 | 1000-2000 | 59.95 | (1-9) |
| ZAPDQ-4 | 2000-4200 | 59.95 | (1-9) |
| ZMSCQ-2-50 | 25-50 | 49.95 | (4-24) |
| ZMSCQ-2-90 | 55-90 | 49.95 | (4-24) |
| ZMSCQ-2-180 | 120-180 | 49.95 | (4-24) |
| ZSCQ-2-50 | 25-50 | 39.95 | (4-24) |
| ZSCQ-2-90 | 55-90 | 39.95 | (4-24) |
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| PSCJ-2-1 | 1-200 | 19.95 | (5-49) |
| PSCJ-2-2 | 0.01-20 | 29.95 | (5-49) |
| ZFSCJ-2-1 | 1-500 | 49.95 | (4-24) |
| ZFSCJ-2-3 | 5-300 | 39.95 | (4-24) |
| ZMSCJ-2-1 | 1-200 | 47.95 | (4-24) |
| ZMSCJ-2-2 | 0.01-20 | 57.95 | (4-24) |
| ZSCJ-2-1 | 1-200 | 37.95 | (4-24) |
| ZSCJ-2-2 | 0.01-20 | 47.95 | (4-24) |

| Model | Freq. (MHz) | Price | (Qty.) |
|---|---|---|---|
| | **2 WAY-0°** | | |
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| PSC-2-1 | 0.1-400 | 9.95 | (6-49) |
| PSC-2-1W | 1-650 | 14.95 | (6-49) |
| PSC-2-2 | 0.002-60 | 19.95 | (6-49) |
| PSC-2-4 | 10-1000 | 19.95 | (6-49) |
| ■ PSC-2375 | 55-85 | 19.95 | (6-24) |
| ■ PSC-2-1-75 | 0.25-300 | 11.95 | (6-49) |
| MSC-2-1 | 0.1-450 | 16.95 | (5-24) |
| MSC-2-1W | 2-650 | 17.95 | (5-24) |
| TSC-2-1 | 1-400 | 13.95 | (5-24) |
| ZFSC-2-1 | 5-500 | 31.95 | (4-24) |
| ■ ZFSC-2-1-75 | 0.25-300 | 32.95 | (4-24) |
| ZFSC-2-1W | 1-750 | 35.95 | (4-24) |
| ZFSC-2-2 | 10-1000 | 39.95 | (4-24) |
| ZFSC-2-4 | 0.2-1000 | 44.95 | (4-24) |
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| ZFSC-2-6 | 0.002-60 | 36.95 | (4-24) |
| ■ ZFSC-2-6-75 | 0.004-60 | 38.95 | (4-24) |
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| ZMSC-2-2 | 0.002-60 | 47.95 | (4-24) |
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| ZSC-2-1W | 1-650 | 32.95 | (4-24) |
| ZSC-2-2 | 0.002-60 | 37.95 | (4-24) |
| ZSC-2-4 | 10-1000 | 37.95 | (4-24) |
| ■ ZSC-2375 | 55-85 | 37.95 | (4-24) |
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| | **GHz** | | |
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| ZAPD-2 | 1.0-2.0 | 39.95 | (1-9) |
| ZAPD-4 | 2.0-4.2 | 39.95 | (1-9) |
| ZAPD-21 | 0.5-2.0 | 49.95 | (1-9) |
| | **3 WAY-0°** | | |
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| PSC-3-1W | 5-500 | 29.95 | (5-49) |
| PSC-3-2 | 0.01-30 | 29.95 | (5-49) |
| ■ PSC-3-1-75 | 1-200 | 20.95 | (5-49) |
| ■ PSC-3-1-75-2 | 10-300 | 22.95 | (5-49) |
| PSC-3-13 | 1-200 | 24.95 | (5-49) |
| ZFSC-3-1 | 1-500 | 39.95 | (4-24) |
| ZFSC-3-1W | 2-750 | 41.95 | (4-24) |
| ZFSC-3-13 | 1-200 | 39.95 | (4-24) |
| ZMSC-3-1 | 1-200 | 47.95 | (4-24) |
| ZMSC-3-2 | 0.01-30 | 57.95 | (4-24) |
| ZSC-3-1 | 1-200 | 37.95 | (4-24) |
| ZSC-3-2 | 0.01-30 | 47.95 | (4-24) |
| ■ ZSC-3-1-75 | 1-200 | 38.95 | (4-24) |
| ■ ZSC-3-2-75 | 0.02-20 | 48.95 | (4-24) |
| | **GHz** | | |
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| ZA3PD-4 | 2-4.2 | 79.95 | (1-9) |

**■ Denotes 75 ohm models**

| Model | Freq. (MHz) | Price | (Qty.) |
|---|---|---|---|
| | **4 WAY-0°** | | |
| PSC-4-1 | 0.1-200 | 28.95 | (6-49) |
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| PSC-4-3 | 0.25-250 | 23.95 | (6-49) |
| PSC-4-6 | 0.01-40 | 29.95 | (6-49) |
| PSC-4A-4 | 10-1000 | 49.95 | (6-49) |
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| ZFSC-4-1W | 10-500 | 74.95 | (1-4) |
| ZFSC-4-3 | 10-300 | 69.95 | (1-4) |
| ■ ZFSC-4375 | 50-90 | 89.95 | (1-4) |
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| ZMSC-4-2 | 0.002-20 | 69.95 | (4-24) |
| ZMSC-4-3 | 0.25-250 | 53.95 | (4-24) |
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| ■ ZSC-4-1-75 | 1-200 | 46.95 | (4-24) |
| ZSC-4-2 | 0.002-20 | 69.95 | (4-24) |
| ZSC-4-3 | 0.25-250 | 43.95 | (4-24) |
| | **GHz** | | |
| ZA4PD-2 | 1-2 | 79.95 | (1-9) |
| ZA4PD-4 | 2-4.2 | 79.95 | (1-9) |
| ZB4PD-42 | 1.7-4.2 | 99.95 | (1-9) |
| ZB4PD-4 | 3.7-4.2 | 89.95 | (1-9) |
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| ■ PSC-5-1-75 | 1-300 | 59.95 | (1-5) |
| | **6 WAY-0°** | | |
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| ■ PSC-6-1-75 | 1-300 | 78.95 | (1-5) |
| ZFSC-6-1 | 1-175 | 89.95 | (1-4) |
| ■ ZFSC-6-1-75 | 1-200 | 89.95 | (1-4) |
| | **8 WAY-0°** | | |
| PSC-8-1 | 0.5-175 | 68.95 | (1-5) |
| ■ PSC-8-1-75 | 0.5-175 | 69.95 | (1-5) |
| PSC-8-6 | 0.01-10 | 79.95 | (1-5) |
| PSC-8A-4 | 5-500 | 89.95 | (1-4) |
| ■ PSC-8A4-75 | 1-300 | 79.95 | (1-4) |
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| ZFSC-8-6 | 0.01-10 | 109.95 | (1-4) |
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| | **12 WAY-0°** | | |
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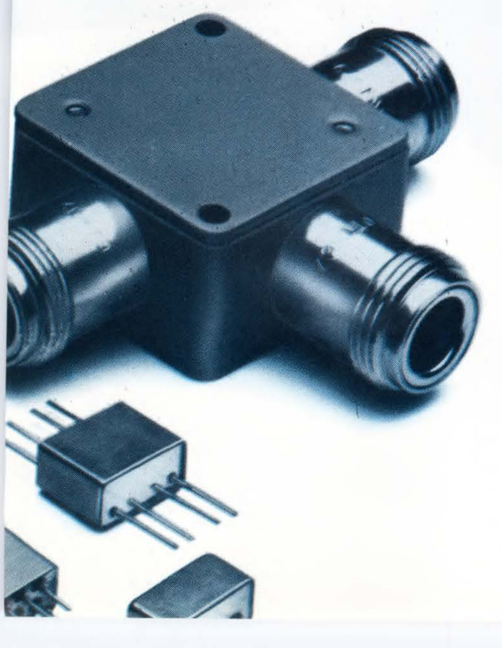
| ZFSC-24-6 | 0.025-50 | 274.95 | (1-4) |
| | **48 WAY-0°** | | |
| ZFSC-48-1 | 10-300 | 595.00 | (1-4) |
| ■ ZFSC-48-1-75 | 10-300 | 595.00 | (1-4) |



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**CIRCLE 199**

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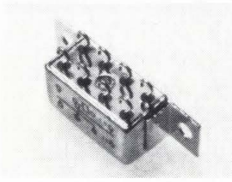
CALAY

CIRCLE 200

# Genicom Relay Technology Helps Make The Space Shuttle Fly.



The Space Shuttle is an outstanding example of some of the most advanced technology on Earth, and in space. And inside this marvel of science, Genicom relays play their vital role in making shuttle missions successful.

Genicom, formerly part of GE, is now an independently owned corporation. So the reliability of Genicom relays is insured, because Genicom combines decades of experience with the most advanced manufacturing techniques to create state of the art, precision relays.

We're experts in the specialized processing technologies that help make Genicom relays the first choice for operations in hostile environments or anywhere consistent reliability is vital.

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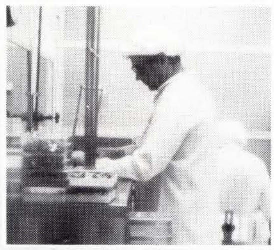

Just like the Space Shuttle, Genicom relays typify some of man's finest technology... on Earth and in space. Write or call for complete details.

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**LAMBDA ELECTRONICS**

DIVISION of Veeco INSTRUMENTS INC.

# NEW LR SERIES

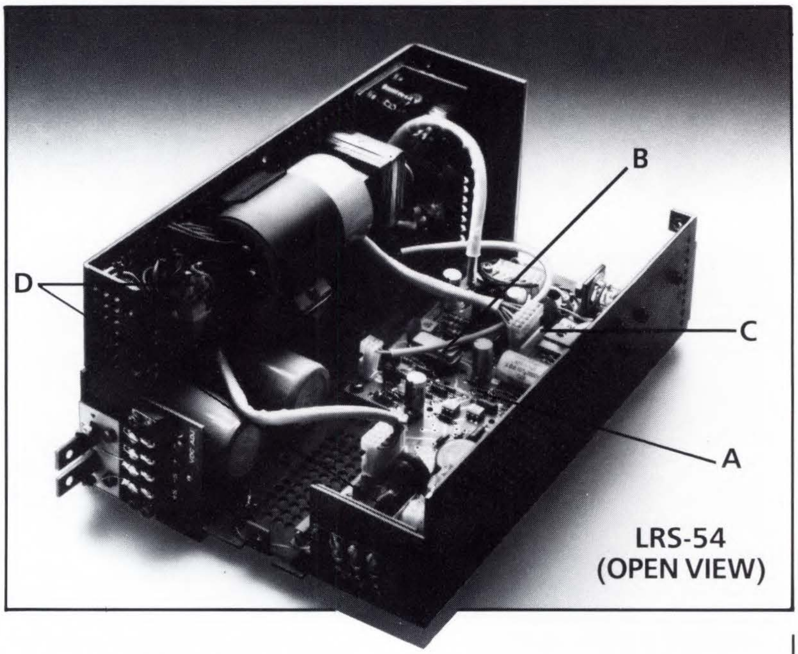
## LAMBDA'S STATE-OF-THE-ART TECHNOLOGY PROVIDES HIGHER DENSITY, EFFICIENCY AND RELIABILITY

**CIRCUIT TOPOLOGY–(A)**
Lambda's new patented circuit layout provides for simple and reliable operation and high thermal and electrical efficiency. A higher MTBF is made possible by the low parts count.

**IC CONTROL CIRCUIT–(B)**
Lambda's new custom integrated control circuit provides for reliable control and operation of the switching transistor and other housekeeping functions. This exclusive IC control circuit replaces 40 discrete components allowing the LR Series to provide better volumetric efficiency than equivalent units.

**MOS SWITCHING DEVICES–(C)**
Power MOSFET provides fast and efficient switching with minimal control and drive circuitry thereby increasing reliability.

**EMI FILTER–(D)**
Integral EMI filter is standard in all units. This filter provides protection to meet the stringent requirements of MIL-STD-461A and FCC Docket 20780 Class A.




**VOLTAGE AND CURRENT RATINGS**

| MODEL | REGULATION (line, load) | RIPPLE (mV RMS) | MAX AMPS AT AMBIENT OF 40°C | 50°C | 60°C | 71°C | PKG. SIZE | DIMENSIONS (inches) | PRICE |
|---|---|---|---|---|---|---|---|---|---|
| **5V±5% ADJ.** | | | | | | | | | |
| LRS-53-5 | 0.1%, 0.1% | 10 | 25.0 | 21.5 | 17.5 | 10.0 | 53 | 2⅜ × 4⅞ × 8 | $375 |
| LRS-54-5 | 0.1%, 0.1% | 10 | 40.0 | 34.0 | 27.5 | 19.5 | 54 | 3 × 4⅞ × 11 | 460 |
| **6V±5% ADJ.** | | | | | | | | | |
| LRS-53-6 | 0.1%, 0.1% | 10 | 21.0 | 18.5 | 16.0 | 8.3 | 53 | 2⅜ × 4⅞ × 8 | 375 |
| LRS-54-6 | 0.1%, 0.1% | 10 | 35.0 | 31.0 | 24.0 | 17.0 | 54 | 3 × 4⅞ × 11 | 460 |
| **12V±5% ADJ.** | | | | | | | | | |
| LRS-53-12 | 0.1%, 0.1% | 15 | 12.5 | 11.2 | 9.6 | 7.2 | 53 | 2⅜ × 4⅞ × 8 | 375 |
| LRS-54-12 | 0.1%, 0.1% | 15 | 22.0 | 18.5 | 15.0 | 10.0 | 54 | 3 × 4⅞ × 11 | 460 |
| **15V±5% ADJ.** | | | | | | | | | |
| LRS-53-15 | 0.1%, 0.1% | 15 | 10.0 | 9.0 | 7.7 | 5.8 | 53 | 2⅜ × 4⅞ × 8 | 375 |
| LRS-54-15 | 0.1%, 0.1% | 15 | 18.0 | 15.0 | 12.0 | 8.0 | 54 | 3 × 4⅞ × 11 | 460 |
| **20V±5% ADJ.** | | | | | | | | | |
| LRS-53-20 | 0.1%, 0.1% | 15 | 7.7 | 6.9 | 5.9 | 4.5 | 53 | 2⅜ × 4⅞ × 8 | 375 |
| LRS-54-20 | 0.1%, 0.1% | 15 | 13.5 | 11.5 | 8.5 | 5.5 | 54 | 3 × 4⅞ × 11 | 460 |
| **24V±5% ADJ.** | | | | | | | | | |
| LRS-53-24 | 0.1%, 0.1% | 15 | 6.5 | 5.8 | 5.0 | 3.8 | 53 | 2⅜ × 4⅞ × 8 | 375 |
| LRS-54-24 | 0.1%, 0.1% | 15 | 11.5 | 9.5 | 7.5 | 4.5 | 54 | 3 × 4⅞ × 11 | 460 |
| **28V±5% ADJ.** | | | | | | | | | |
| LRS-53-28 | 0.1%, 0.1% | 15 | 5.7 | 5.1 | 4.4 | 3.3 | 53 | 2⅜ × 4⅞ × 8 | 375 |
| LRS-54-28 | 0.1%, 0.1% | 15 | 9.5 | 8.5 | 6.5 | 4.0 | 54 | 3 × 4⅞ × 11 | 460 |
| **48V±5% ADJ.** | | | | | | | | | |
| LRS-53-48 | 0.1%, 0.1% | 35 | 3.3 | 2.8 | 2.4 | 1.8 | 53 | 2⅜ × 4⅞ × 8 | 375 |
| LRS-54-48 | 0.1%, 0.1% | 35 | 5.8 | 5.1 | 3.6 | 2.3 | 54 | 3 × 4⅞ × 11 | 460 |

# LR SERIES Specifications

**DC OUTPUT**
Voltage range shown in tables.

**REGULATED VOLTAGE**
regulation, line .......0.1% from 95 to 132VAC.
regulation, load ......0.1% from no load to full load.
ripple and noise......10mV RMS, 35mV pk-pk for 5V and 6V models.
15mV RMS, 100mV pk-pk for 12V through 28V models.
35mV RMS, 150mV pk-pk for 48V models.
temperature coefficient ...................0.03%/°C
remote programming resistance......1000 Ω/volt
remote programming voltage .........volt per volt

**AC INPUT**
line...............95 to 132VAC, 47-440Hz.
power..........225 watts maximum for LRS-53
380 watts maximum for LRS-54

**DC INPUT**
145VDC±10%

**EFFICIENCY**
70% min (5V through 15V models)
75% min (20V through 48V models)

**OVERSHOOT**
No overshoot at turn-on, turn-off or power failure.

**AMBIENT OPERATING TEMPERATURE**
Continuous duty −10°C to 71°C with suitable derating above 40°C.

**STORAGE TEMPERATURE RANGE**
−55°C to +85°C

**OVERLOAD PROTECTION**
Electrical
External overload protection, automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

**THERMAL**
Self-resetting thermostat

**FUSING**
Line fuse removes the power supply from the line if a short occurs in the input circuitry.

**OVERVOLTAGE PROTECTION**
Overvoltage protection is standard on all models. If output voltage increases above a preset level, inverter drive is removed.

**COOLING**
All units are convection cooled. No fans or blowers are needed.

**SOFT-START CIRCUIT**
The turn-on in-rush current will not exceed four times the steady state input current.

**DC OUTPUT CONTROLS**
Simple screwdriver adjustment over the entire voltage range.

**INPUT AND OUTPUT CONNECTIONS**
AC Input... Barrier strip mounted on chassis.
DC Output... Through heavy duty threaded buss bars.
DC Sensing... Through barrier strip adjacent to output buss bars.
Remote On/Off....Barrier strip mounted on chassis.

**MOUNTING**
Two mounting surfaces and two mounting positions.

**POWER FAILURE**
5V and 6V models will remain within regulation limits for at least 16.7 msec. after loss of AC power when operating at full load, $V_O$ max, and 105VAC input at 60Hz.

**REMOTE SENSING**
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation.

**REMOTE TURN-ON/TURN-OFF**
Provision is made for digitally controlled remote turn-on, turn-off.

**FUNGUS PROOFING**
All units are rendered fungi inert.

**MILITARY SPECIFICATIONS**
The LR series is designed to pass the following tests in accordance with MIL-STD-810C.
1) Low Pressure—Method 500.1, Procedure I.
2) High Temperature—Method 501.1, Procedures I and II.
3) Low Temperature—Method 502.1, Procedure I.
4) Temperature Shock—Method 503.1, Procedure I.
5) Temperature-Altitude—Method 504.1, Procedure I. Class 2 (0°C Operating).
6) Humidity—Method 507.1, Procedure I.
7) Fungus—Method 508.1, Procedure I.
8) Vibration—Method 514.2, Procedures X and XI.
9) Shock—Method 516.2, Procedures I and III.

**EMI**
Conducted EMI conforms to FCC Docket 20780 Class A, and MIL-STD-461A Notice 4 CEO4 for power leads.

**PHYSICAL DATA**

| Package Model | Lbs. Net | Lbs. Ship | Size Inches |
|---|---|---|---|
| LRS-53 | 3¼ | 4¼ | 2⅜ × 4⅞ × 8 |
| LRS-54 | 6½ | 7½ | 3 × 4⅞ × 11 |

**ACCESSORIES**
Rack Adapters (LRA-14, LRA-15, LRA-17) and cable system available.

**FINISH**
Grey, Fed. Std. 595, No. 26081

**Guaranteed for 5 Years**
Five year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

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Under Evaluation

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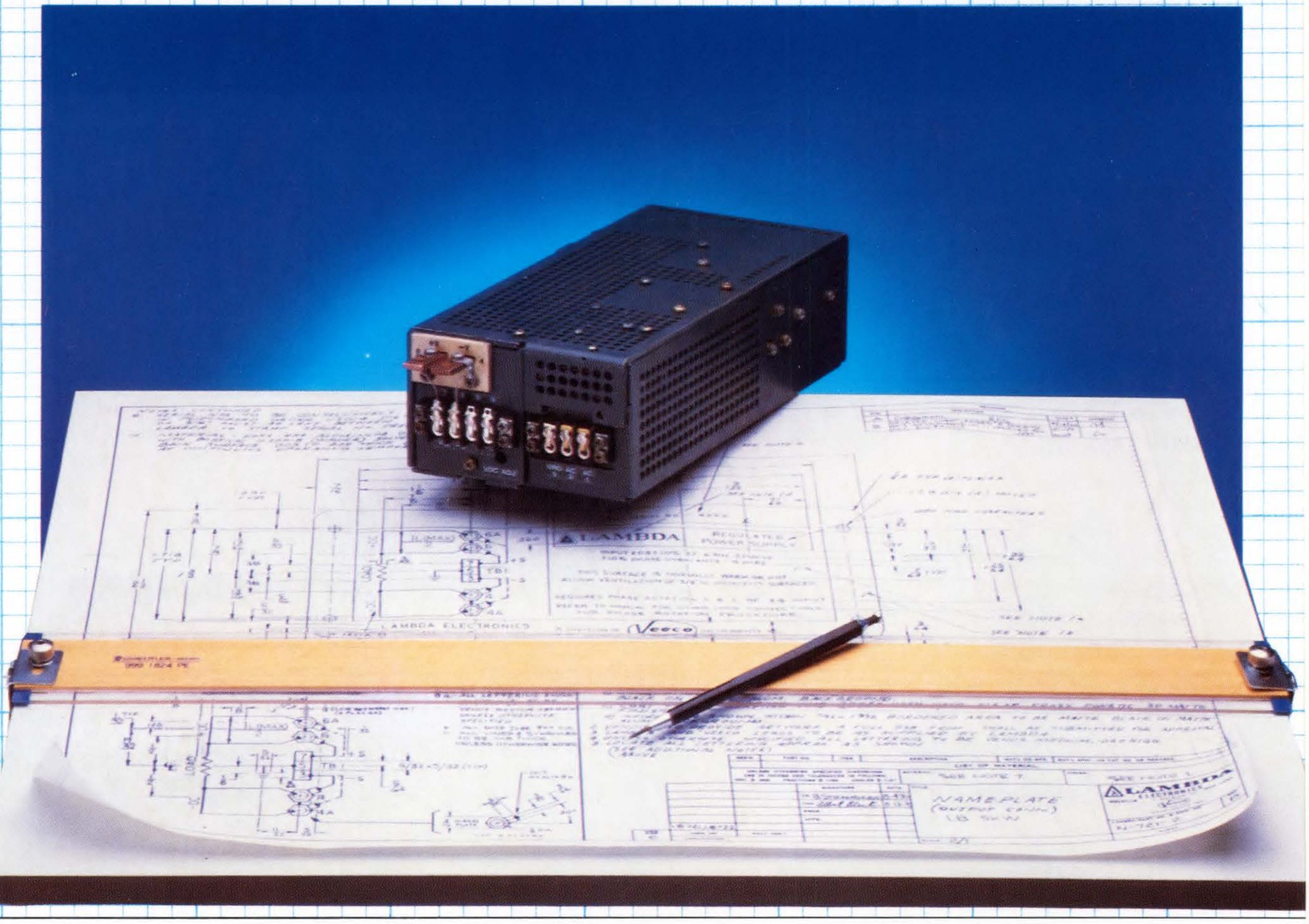

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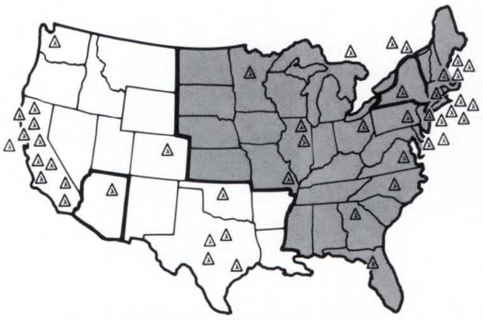

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(Required by 39 U.S.C. 3685)

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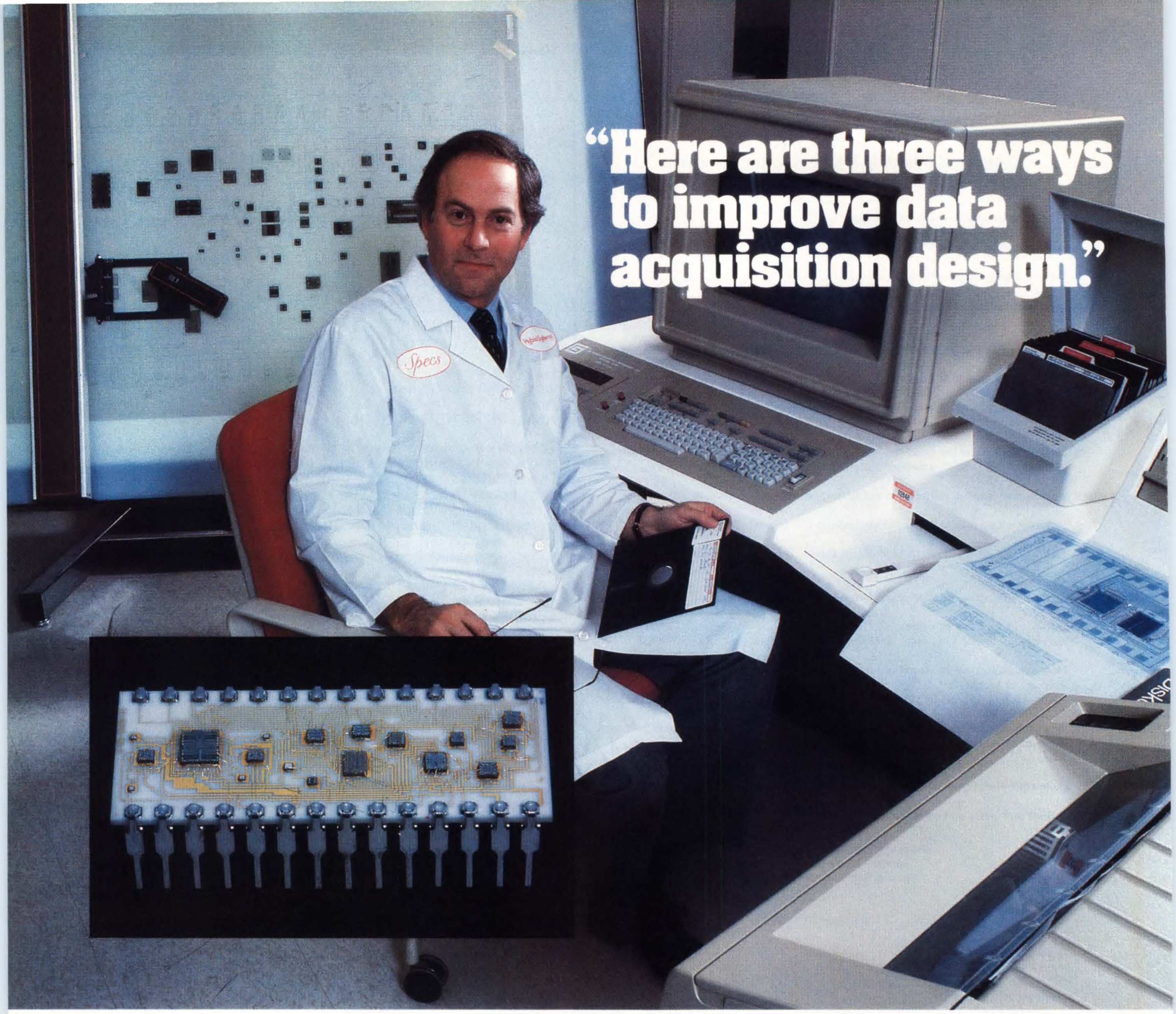


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**CIRCLE 203**

**Hybrid Systems**
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# Systolic array chip achieves unparalleled processing speeds

The first systolic array processor chip incorporates 72 single-bit microprocessors, providing a parallel architecture and hence speed—5 million 8-bit instructions each second—well-suited to image processing, pattern recognition, and signal processing.

The Geometric Arithmetic Parallel Processor (GAPP) from NCR Microelectronics is only the second chip to shun the standard von Neumann architecture, instead processing multiple streams of data simultaneously (ELECTRONIC DESIGN, Oct. 31, p. 207). It can thus perform a 21-by-21-pixel binary correlation in 1.3 ms.

The processors, which are arranged in a 6-by-12 grid, each have 128 bits of RAM, letting system designers eschew frame buffers and other costly memory devices. Incorporating memory internally also cuts down on time-consuming data fetches.

The systolic architecture lets system designers group a number of chips together, increasing throughput by increasing the number of processors performing a task. Arrays of the chips can be extended to any size, so that an image-processing system could assign one processor element to each pixel in an image. For example, 32 chips forming a 48-by-48-element array can perform 922 million 8-bit or 470 million 16-bit additions in 1 second.

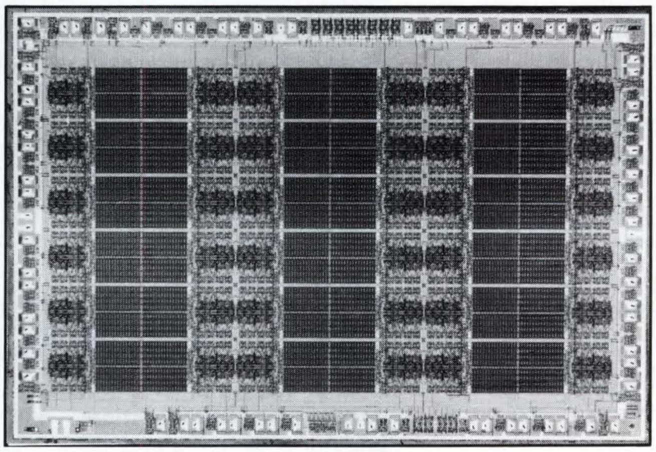
The processor elements of the CMOS chip normally communicate with their nearest neighbors on each side, although a global broadcast operation permits loading of the same data into all the processors.

Input and output occur simultaneously with processing, since one of the four latches within each processor element handles I/O, letting the arithmetic and logic unit continue processing.

The systolic array processor, operates at a 10-MHz clock rate and has a maximum power consumption of 500 mW. It requires a supply voltage of 5 V.

The chip, 100,000 mil$^2$, is housed in either an 84-pin ceramic or plastic pin-grid array. In ceramic, it will be priced at $350 for a single unit; the price for the plastic version has not yet been set. Samples will be available by year's end.

*NCR Corp., Microelectronics Division, 2001 Danfield Court, Fort Colins, Colo. 52998; Ronald Davis, (303) 226-9500.* **CIRCLE 317**



**Terry Costlow**

# Dense bipolar gate arrays are fast, testable, and radiation-hardened

With a combination of features that makes a designer's mouth water, a family of gate arrays will initially offer chips containing some 3500 and 5000 gates. These chips, developed by Raytheon, match the best densities of other bipolar (but not ECL) arrays, but offer higher performance in the form of short internal delays, built-in test features, and a radiation hardness of $10^6$ rads, total dose.

Fabricated with an oxide-isolated integrated Schottky logic process, the arrays offer typical internal delays of 1.2 ns and a power dissipation of about 120 $\mu$W per gate (ELECTRONIC DESIGN, Oct. 31, p. 46). During circuit design, however, critical paths can be sped up to cut delays to 0.9 ns—lower than for any other non-ECL array—at the expense of gate power consumption, which doubles. The CGA50L15 contains 4992 gates surrounded by 150 I/O pads; the CGA35L12, 3500 gates and 120 I/O pads.

To make the arrays more testable, two features were incorporated—one is a circuit that performs some dc parametric testing to check each output for high, low, or three-state operation, and the other are test circuits built into each appropriate macrocell in the circuit library.

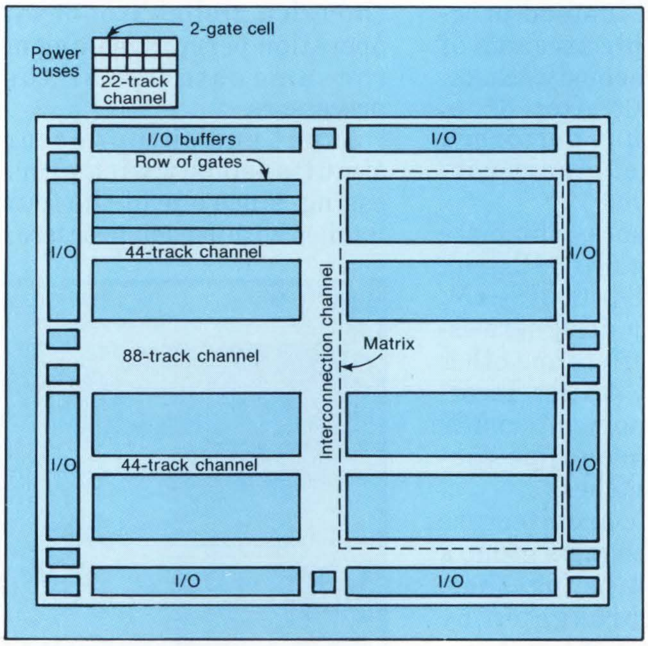
The arrays are designed to operate over the full military temperature range. They come in a wide choice of packages with high pin count.

Nonrecurring engineering charges range from $80,000 to $100,000, and the final cost of a circuit depends on quantity and package type. The arrays are supported by an integrated CAD software package and a library of macrocells that can be overlaid on a Mentor workstation to permit low-cost schematic capture.

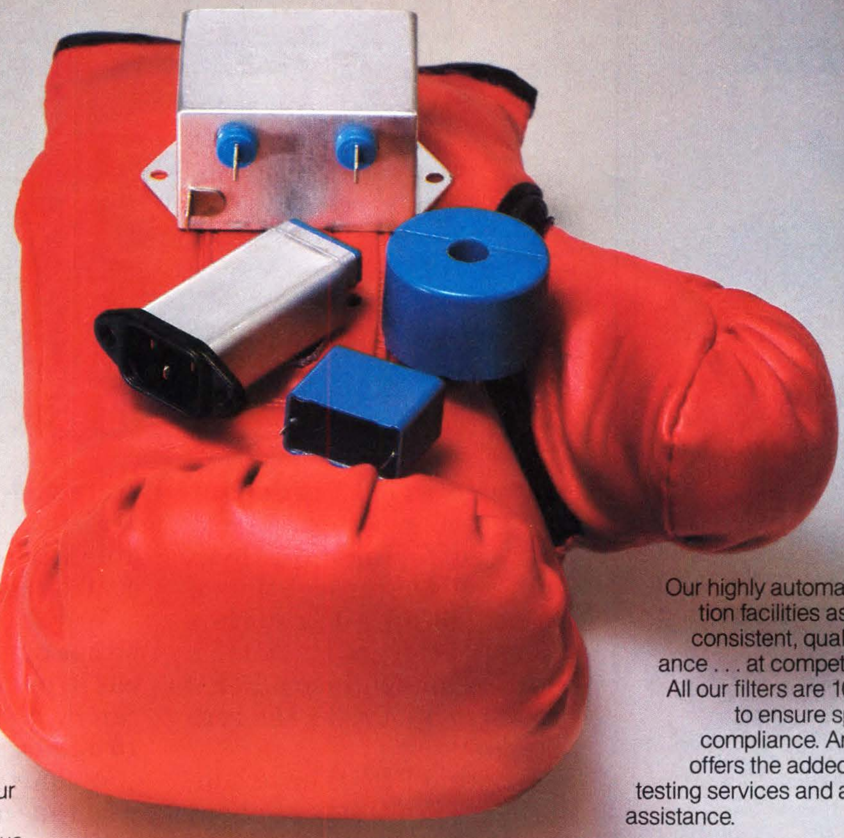
*Raytheon Co., Semiconductor Division, 350 Ellis St., Mountain View, Calif. 94043; Dick McCoy, (415) 966-7628.*

**CIRCLE 302**

**Dave Bursky**

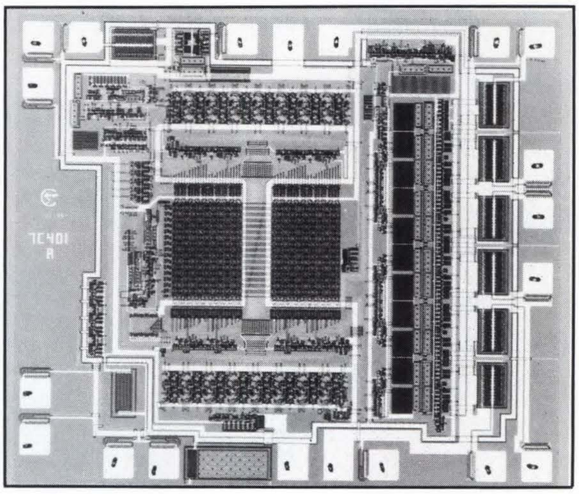



**Holding delays to as little as 0.9 ns, bipolar gate arrays come in two configurations—4992 gates and 150 I/O pads or 3500 gates and 120 I/O pads.**



**DIGITAL ICs**

# FIFOs boost system performance



Two FIFOs increase system performance by buffering data flows with a bubble-through time of 65 ns. (Bubble-through is measured from the time a word is loaded into a FIFO until it appears at the register's output.)

Existing FIFOs have bubble-through times of about 2 μs, which means that the overall system throughput is degraded. Normally, the degradation occurs because the device reading the FIFO must wait 2 μs for the word to move through. Similarly, when a device is waiting to load a full FIFO, it will be delayed 2 μs after a word is read. In both cases, the new FIFOs, developed by Cypress Semiconductor, impose only a 65-ns delay.

One device, the CY7C401, holds 64 four-bit words; its sister chip, the CY7C402, stores 64 five-bit words. A version of both chips is available with an output-enable control signal.

Words can be written into either part in 15 ns and read out in under 10 ns. The FIFO can receive a data stream of 15 million words a second.

A control signal indicates when one or more of the 64 locations in the FIFO are available. Other control lines allow the FIFOs to be stacked serially, so that two devices could give a 128-by-4-bit (or -by-5-bit) stack. The same lines can be used to expand the devices in parallel, using two parts to create an 8- or a 10-bit code stack.

In 100-unit quantities, the CY7C401 is available from stock for $35.25 and the CY7C402 for $41.25.

*Cypress Semiconductor Corp., 3901 N. First St., San Jose, Calif. 95134; (408) 943-2600.* **CIRCLE 309**

**Curtis Panasuk**

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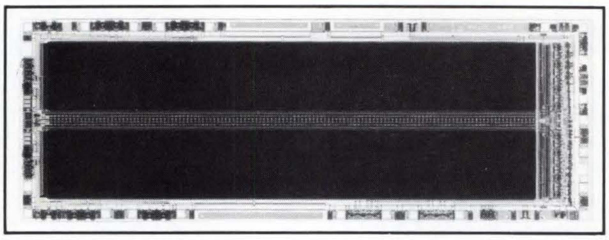
CIRCLE 205

"SEE US AT COMDEX AT THE CANADIAN GOVERNMENT BOOTH"

**DIGITAL ICs**

# Fast 64k CMOS static RAMs deliver 4 bits at a time



The first 4-bit-wide 64k static RAM to be released commercially, Integrated Device Technology's IDT7188 boasts a maximum access time as low as 55 ns and, because it is CMOS, a typical power consumption of just 225 mW (494 mW maximum) when active.

The RAM actually comes in two versions: one, the 7188L, with a battery-backup data retention capability when run off a 2-V battery (the power consumed is just 7.5 μW); the other version, the 7188S, without that capability. Both versions have a low-power standby mode in which the power consumption drops to 100 μW or 30 μW, respectively.

The chips' internal circuits are fully static, so that access and cycle times are identical. Commercial units offer access times of 55, 70, 85, or 100 ns; the military models, 70, 85, or 100 ns. Additionally, the CEMOS II technology used to fabricate the chips virtually eliminates soft errors induced by alpha particles.

The RAMs are housed in 22-pin 300-mil DIPs, have TTL-compatible input and output lines, and operate from a 5-V ±10% supply. The output lines also have a three-state capability to permit multiple banks of RAMs to share the same bus.

Military units are processed in compliance with MIL-STD-883, method 5004, ensuring reliability. Also, the chips meet MIL-STD-883, class C, requirements.

Small production quantities of both versions will be available late in the first quarter of 1985. Engineering samples will be ready early in the first quarter at a cost of $450 and $510 each for the 85-ns L and S military versions, respectively, in 100-unit quantities.

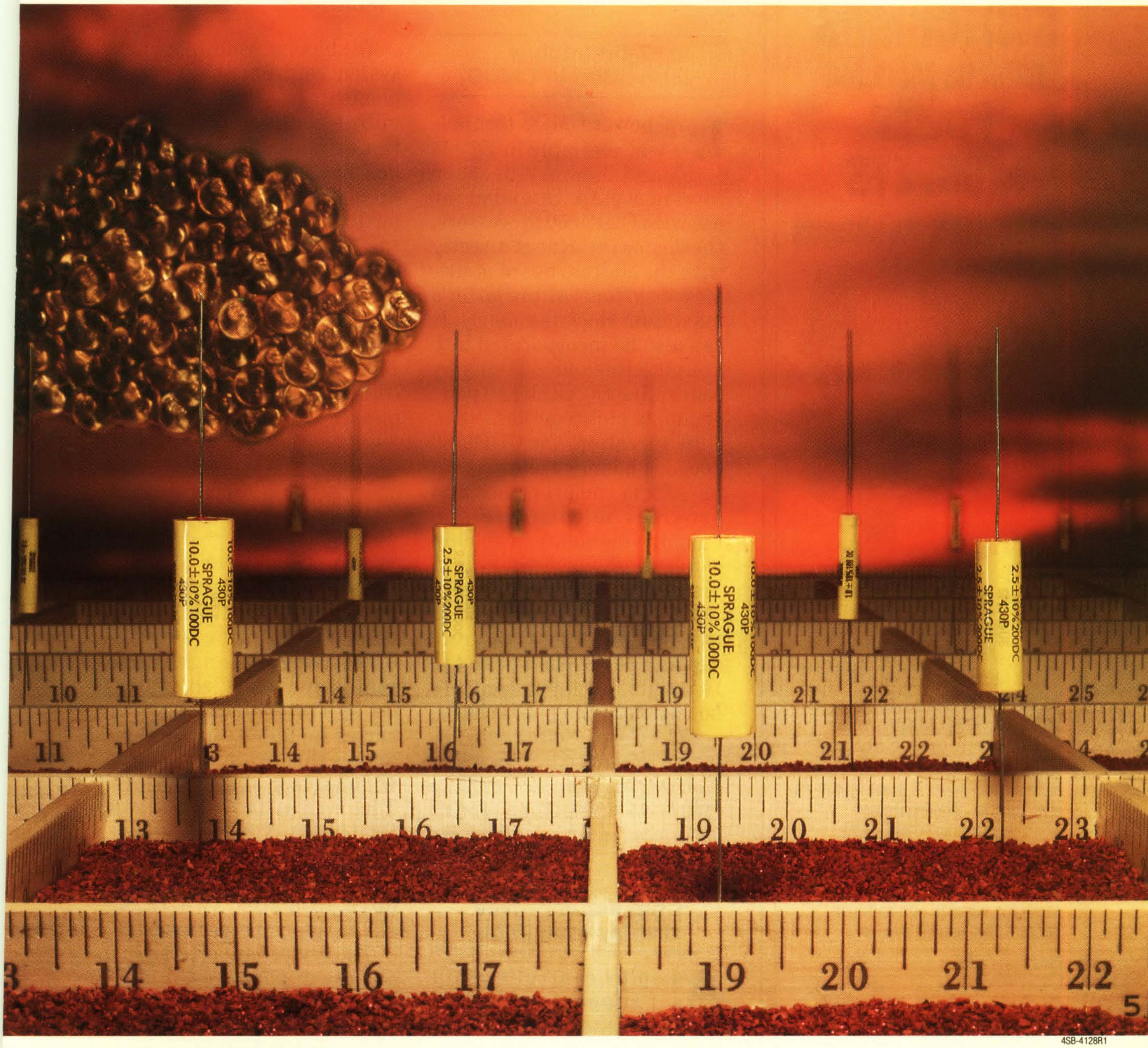
Also on the way is the IDT-7198, which is functionally the same as the 7188 but adds two Chip Select lines. It will be housed in either a 24-pin 300-mil DIP or a 28-contact leadless carrier. Samples are expected late in the first quarter.

*Integrated Device Technology Inc., 3236 Scott Blvd., Santa Clara, Calif. 95051; Sam McCarthy, (408) 727-6116.*

**Dave Bursky**

**CIRCLE 315**

# SUITABILITY.




4SB-4128R1

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Write for Engineering Bulletin 2445C to Technical Literature Service, Sprague Electric Company, a Penn Central unit, 347 Marshall Street, North Adams, Mass. 01247.

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CIRCLE 207

## DIGITAL ICs

### 7-bit latch is fabricated in CMOS

Low-power CMOS technology is available in a 7-bit latch and memory-decoder interface chip. Intended for use with CDP1800 processors, the device interfaces directly with the address bus of multiplexed systems at the latter's maximum clock frequency. It can also be incorporated into nonmultiplexed systems by connecting the clock and power supply pins together.

In operation, the CDP1883 decodes memory address inputs from the processor and provides select signals to memory elements. The chip can be used for memory systems of 16 kbytes or greater.

The CDP1883 is available in two versions, operating from supplies of 4 to 6.5 V dc or 4 to 10.5 V dc. Both versions are housed in 20-pin plastic DIPs.

*RCA Corp., Solid State Division, Route 202, Somerville, N.J. 08876; (800) 526-2177 or (201) 685-6000. $2.55 (250 to 999 units); stock.* **CIRCLE 321**

### Chip set improves display resolution

A display controller chip set supports 100-MHz video dot rates and contains three on-chip line buffers for flicker-free, smooth scrolling. One chip, the Am8052 alphanumeric CRT controller, is a fully programmable, register-oriented MOS device. Packaged in a 68-pin leadless chip carrier, it is currently offered in 5- and 6-MHz versions.

The bipolar Am8152A video system controller (VSC) complements the Am8052 by providing complete video path timing and control. The VSC has TTL outputs and runs at up to 60 MHz. An ECL-compatible version, designated the Am8153A, offers rates of up to 100 MHz.

*Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, Calif. 94088; (408) 732-2400. $77.50 (5-MHz 8052) and $32 (8152A or 53A) in quantities of 100.* **CIRCLE 322**

### CMOS gate arrays have 2.5-ns delays

The GA series of gate arrays is fabricated with a 3-μm Si-gate CMOS process, which features 1.8-μm effective gate lengths and yields devices with typical delay times of 2.5 ns. The series includes four generic arrays that are suitable for a wide variety of applications. These include the MK GA1000D,-2000D, -3000D, and -4000D gate arrays with the equivalent of 1152, 2016, 3016, and 4080 two-input NAND gates, respectively.

The devices are offered in a variety of packages, including 40-pin plastic or ceramic DIPs, ceramic leadless chip carriers, and plastic or ceramic pin-grid arrays of up to 120 pins. In quantities of 1000, the price for the MK GA 1000D in the 40-pin plastic DIP is $9.30.

*Mostek Corp., 1215 W. Crosby Road, Carrollton, Texas 75006; (214) 466-6000.*

**CIRCLE 323**

# LOCK UP GHz SIGNALS QUIETLY.

| NAME | PART NUMBER | SPEED |
|---|---|---|
| Quad NOR Gate | 10G000 | 75 ps |
| Fanout Buffer | 10G011 | 3 GHz |
| Comparator/ Driver | 10G012 | 3 GHz |
| Precision D Flip Flop | 10G021 | 3 GHz |
| 2 Stage Divider | 10G060 | 3 GHz |
| 7 Stage Counter | 10G065 | 3 GHz |

| NAME | PART NUMBER | SPEED |
|---|---|---|
| Variable Modulus Divider | 10G070 | 2 GHz |
| 7 Stage Divider | 11G566 | 4 GHz |
| Diode Array | 16G010 | 500 GHz |
| Diode Array | 16G011 | 675 GHz |
| FET Array | 16G020 | 15 GHz |
| Dual Gate FET Array | 16G021 | 15 GHz |

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GigaBit Logic, 1908 Oak Terrace Lane, Newbury Park, CA 91320. Telephone (800) GAAS-ICS (422-7427). In CA, (805) 498-9664. Telex 194449.

*Patent Pending

**GBL** GigaBit Logic

# ...THE NEXT GENERATION

CIRCLE 209

## COMPUTER PERIPHERALS

# Continuous-speech unit recognizes 200 words, costs just $4000

A continuous-speech input terminal costing only $4000 recognizes 200 words. What's more, the VET-232 SD voice entry terminal, from Scott Instruments, offers a limited speaker-independent option for only about $1000 more. Most other speech recognizers, in contrast, do not accept continuous speech, cost more (usually a good deal more), and work with smaller vocabularies.

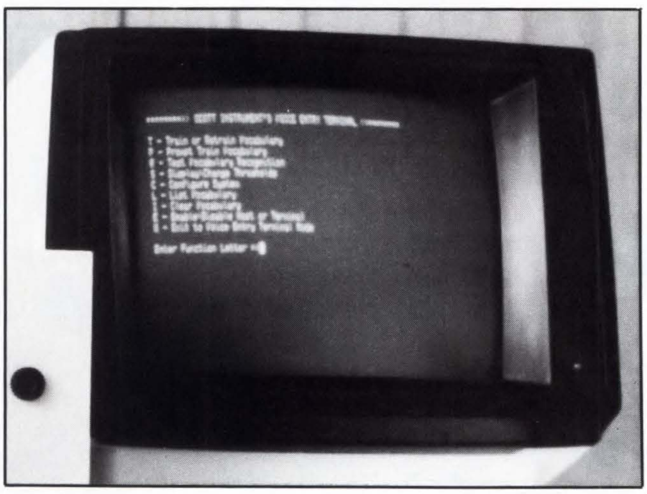
The terminal comes with 128 kbytes of RAM, expandable to 256 kbytes; a microphone for the voice input; and a speaker for spoken responses. It connects to its host computer via an RS-232 link, and a second RS-232 port provides a connection to a CRT screen.

**Heather Bryce**

Speaker-dependent recognition requires that a user "train" the system by saying each vocabulary word two times. The terminal will then recognize those words, even when they are part of a stream of "untrained" words —a novel feature for speech-input devices.

The speaker-independent option accepts the numbers zero through nine, plus "yes" and "no." Additionally, Scott Instruments will prepare custom vocabularies.

A built-in feature allows speech to replace keystrokes with words. The user can define up to 64 different words, each taking the place of as many as 30 keystrokes.



Voice response, however, is optional (users must submit either a list or a tape). The responses can serve as operator prompts, operator feedback, or final outputs. The charge is $1500 per word, with a minimum fee of $25,000.

Although the unit offers voice storage and forwarding as standard, a telephone management facility that furnishes a telephone interface is optional. Once hooked up to the phone lines, the terminal automatically answers incoming calls by taking the line off hook and can automatically dial outgoing numbers. It encodes and decodes DTMF signals, monitors calls in progress, issues a busy signal, and detects ringing and spoken responses on outgoing calls.

Prototype systems will be available in December for evaluation, and volume shipments will begin in the first quarter of 1985.

*Scott Instruments Corp., 1111 Willion Springs Drive, Denton, Texas 76205; (817) 387-9514.* **CIRCLE 410**

# Eliminate ATE component clutter with HP designed-for-systems power supplies.

Now you can choose from the widest range of ATE power supplies available to help get your automatic test systems up and running in a fraction of the time required by traditional methods. The HP system power supply family lets you choose the right power supply for your application. Replace up to five separate instruments and a web of complex interconnections with a single high-performance, extremely easy-to-use programmable power supply.

### A complete family of solutions.

HP designed-for-system power supplies let you build a system to test PC boards, for example, by giving you programmable voltage with automatic over-current down-programming to protect board traces. You can design an automatic incoming inspection system to test a wide variety of components, while investing in only a single power supply. You can program voltage and current and read both back, including instrument status, over the HP-IB.

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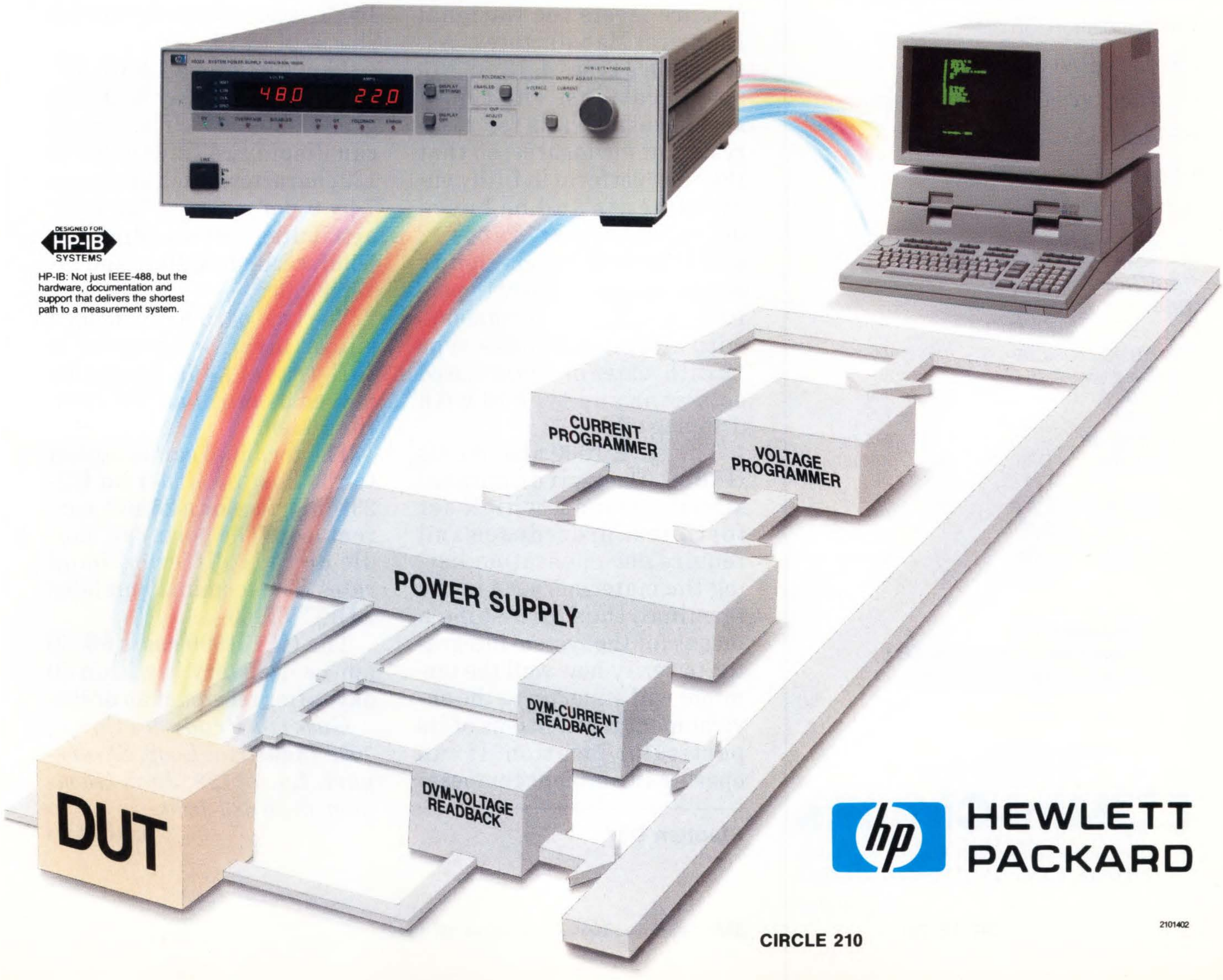
### Hewlett-Packard: A world leader in ATE power supplies.

The next time you need a versatile, reliable power supply, think Hewlett-Packard. For more information, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

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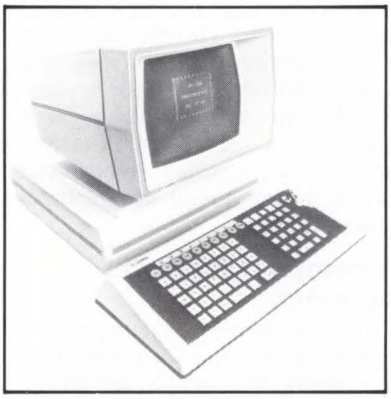
CIRCLE 210

2101402

# Video terminals withstand harsh environments



A series of video display terminals can operate in factories, oil fields, nuclear power plants, and various other harsh industrial environments. The GPC 1000 series terminals from Gamma Products are totally sealed monitors and keyboards designed to withstand blown dust, rain, snow, ice, and even seeping oil.

The GPC 1000's nonventilated cast-aluminum enclosure meets the National Electrical Manufacturers Association's types 4, 12, and 13 specifications. The type 4 specification calls for rust-resistant enclosures, so that they can perform in filthy environments and be hosed down with water. Types 12 and 13 specifications signify an enclosure's ability to perform in indoor environments with dripping liquids—type 12 with water or water-based solutions and type 13 with dripping oil.

The GPC 1000 also meets G3036.01 environmental specifications, which set forth test procedures and require documentation listing the materials used in the terminal, thus furnishing a means for the system integrator to verify how well the terminal will stand up to the environmental conditions of its particular location. It can operate in ambient temperatures of 0° to 60°C (32° to 140°F) and withstand regular shocks of 13.5 g.

The unit has a 14-in.-diagonal CRT display with P31 green phosphor. The screen can display 24 lines of 80 or 132 characters, each in its own 7-by-9-dot matrix. Character attributes include blinking, boldface, underlining, and inverse video.

The keyboard has a molded silicon layer covering its 76 full-travel keys. It can be moved as much as 8 ft from the screen.

The terminal can be linked to the host by either an RS-232 interface or a 20-mA current loop. The ports can handle up to 16 different baud rates. The terminal emulates a DEC VT100.

The GPC 1000 costs $5550 apiece. Delivery is within 30 days after receipt of an order.

*Gamma Products Corp., 7092 Industrial Loop, Shreveport, La. 71129; Jack Gammon, (318) 686-1600.*

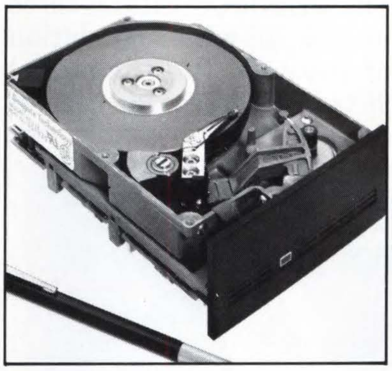
**Stephan Ohr**

**CIRCLE 311**

## COMPUTER PERIPHERALS

# Hard-disk drives have high storage

A trio of Winchester disk drives offers high storage capacity in a variety of package sizes. Leading the lineup from Seagate Technology is a 3½-in. hard-disk drive that holds 10.03 Mbytes of formatted data. The ST112 features two platters with a recording density of 10,864 bpi and an average access time of 65 ms. Its transfer rate is 5.0 Mbytes/s.



The ST225 is a half-height 5¼-in. drive with 20.05 Mbytes of formatted storage. A two-platter unit, it has an average access time of 85 ms, records at 9784 bpi, and transfers 5.0 Mbytes/s. It features an advanced stepper motor and a buffered seek mode for improved operation.

The ST4051, a full-sized 5¼-in. drive, stores 50 Mbytes on three platters. Its average access time is 40 ms, and it transfers data at 5 Mbits/s.

All three drives employ the ST412 interface. In quantities of 1000 units, the ST112 is priced at $495, the ST225 at $525, and the ST4051 at $1295. The ST112 and ST225 will be available for volume shipment this month. Evaluation units of the ST4051 will be ready in December, with quantity shipments to start in February.

*Seagate Technologies, 920 Disc Drive, PO Box 66360, Scotts Valley, Calif. 95066; (408) 438-6550.*

**CIRCLE 320**

## COMPUTER PERIPHERALS

# Plotters set speed, resolution marks

Two electrostatic plotter families from Benson establish new records for speed and resolution.

The series 9600 features three models, all with a resolution of 400 dots/in.: the model 9624, with a record speed of 1.5 in./s; the 9636, with a speed of 1 in./s; and the 9644, with a speed of 0.8 in./s. All work with the firm's Graphware 2400 element processor and GPR IV software.

The processor accepts VDM (Virtual Device Metafile) outputs used by GKS (Graphical Kernal System) systems. The software implements level 0.a of the ISO and ANSI GKS standard for two-dimensional device-independent graphics.

The 9600 plotters use a precision dynamic toning system that applies toner to the electrographic media 50 times for each media charge. A capillary drying system helps dry out the media's toner quickly and without smearing.

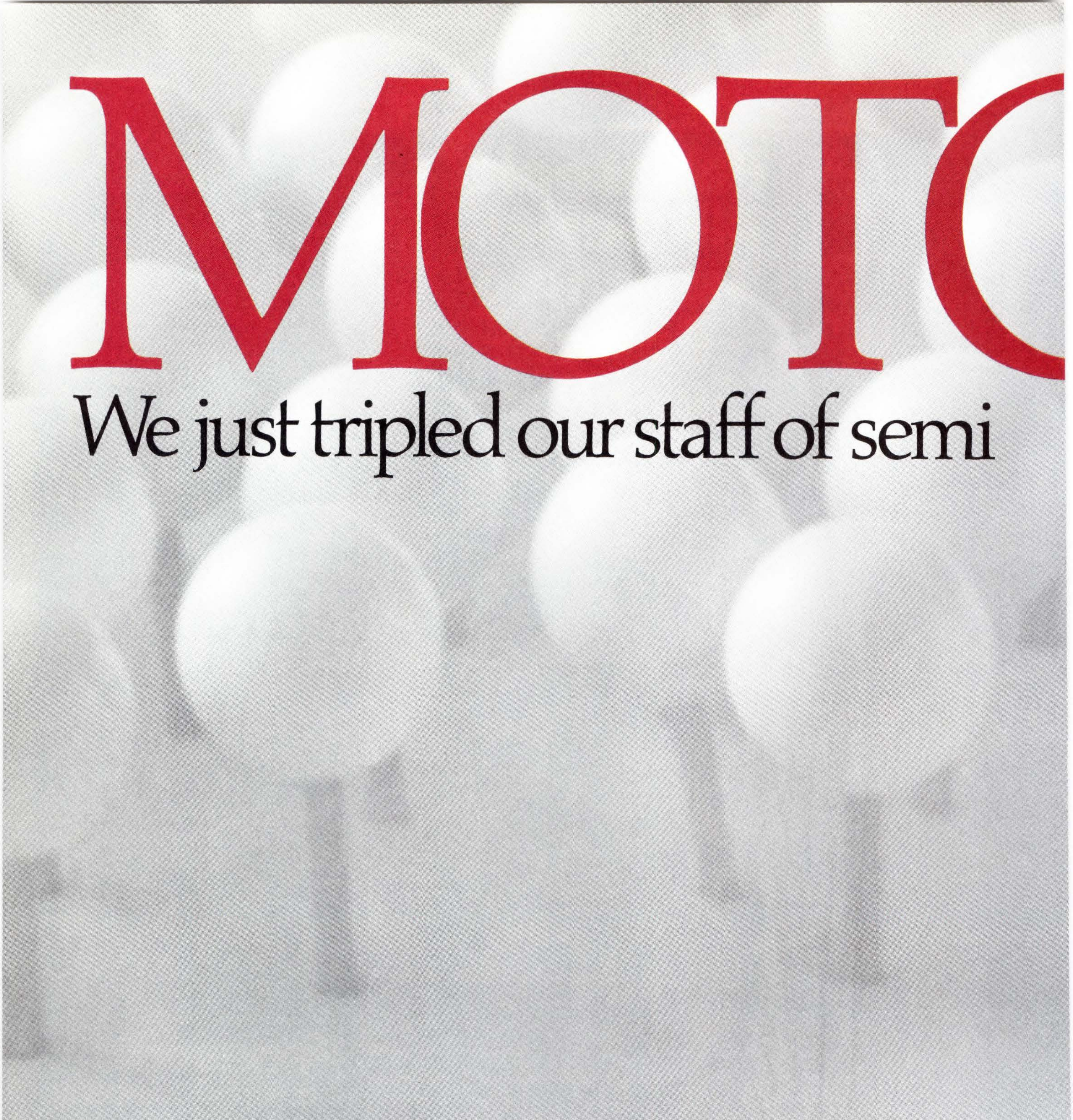
Also including three models, the series 9800 plotters all have a record-setting resolution of 508 dots/in.: the model 9824 for 24-in.-wide plots, with a speed of 0.25 in./s; the model 9844 for 44-in.-wide plots, with a speed of 0.1 in./s; and the model 9836 for 36-in.-wide plots, with a speed of 0.15 in./s.

Like the series 9600, the 9800 plotters work with the firm's Graphware 2400 processor.

The 9636 is priced at $56,010 in single quantities, the 9824 at $44,485, and the Graphware 2400 processor at $24,950. Delivery is within 60 days.

*Benson Inc., 2690 Orchard Way, San Jose, Calif. 95152. Bob Hines, (408) 945-1000.*

**CIRCLE 312**

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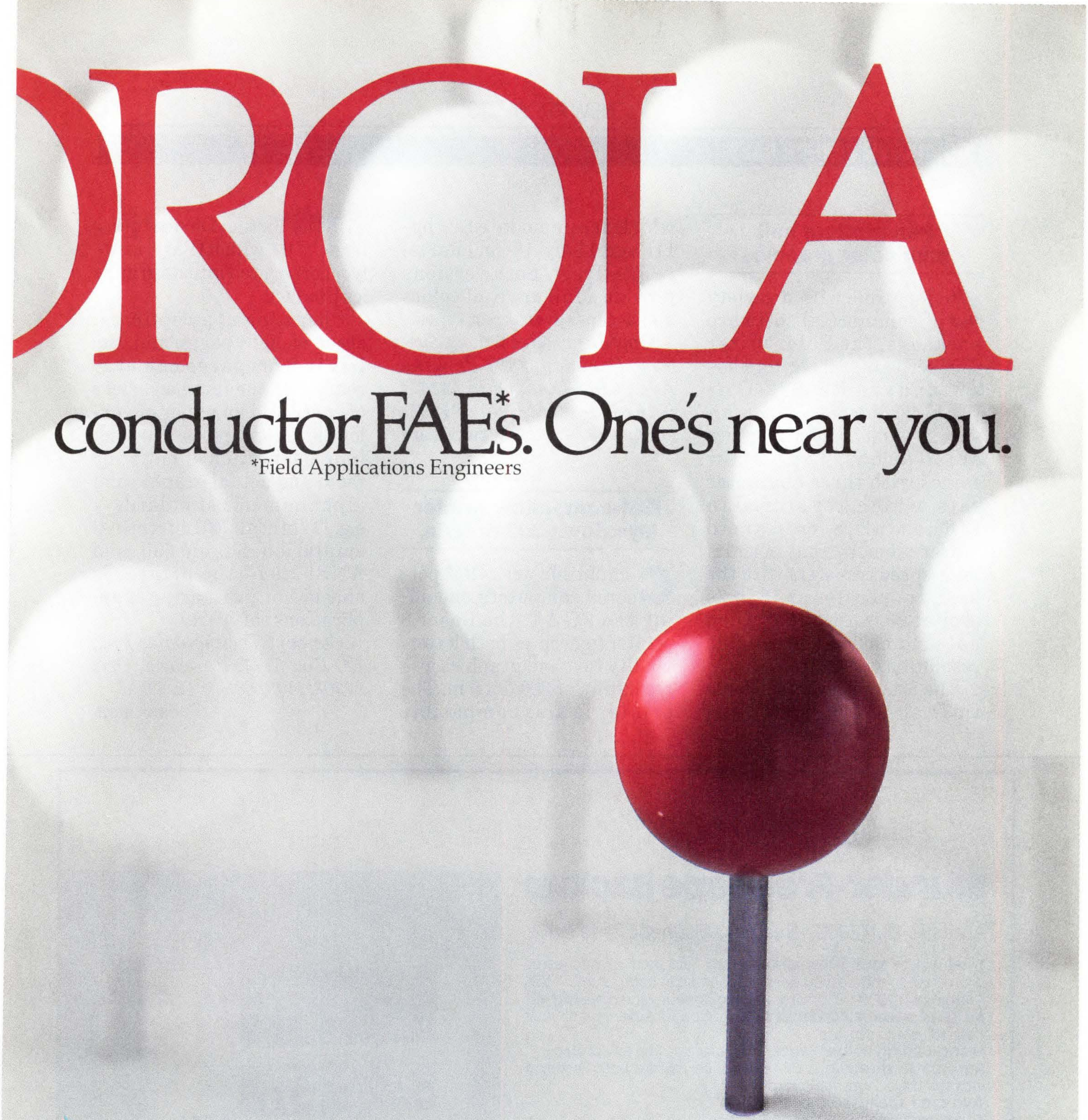


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## COMPUTER PERIPHERALS

### Pen plotters suit multicolor graphics

Compatible with a variety of commercial software packages, the Colorwriter 6300 series of pen plotters has a standard RS-232-C or IEEE-488 interface to serve a variety of multicolor graphics applications. The plotter comes with three character sets, which are stored in ROM, and a 2-, 8-, or 16-kword buffer memory that permits high-speed transfers with the host. It operates at 16 in./s—or at 20 in./s with the pen up—and has an addressable resolution of 0.001 in.

The 6300 series is available in 7- and 10-pen models, which accommodate 8½-by-11- and 11-by-17-in. charts, respectively. Both versions provide a full array of colors and accept several pen types.

*Gould Inc., Recording Systems Division, 3631 Perkins Ave., Cleveland, Ohio 44114; (216) 361-3315. From $1995; six weeks.* **CIRCLE 324**

### IBM-compatible printer lays down 300 dots/in.

Compatible with IBM personal computers, including the PC AT, the Laser 8 printer generates both letter-quality text and graphics at a resolution of 300 dots/in. The printer is also compatible with the Virtual Device Interface (VDI), which IBM recently incorporated into its graphics products.

Operating at an optimum speed of eight pages/min, the Laser 8 prepares camera-ready documents in a variety of fonts and on paper of various sizes and types. Through implementation of major de facto and actual graphic and alphanumeric standards—e.g., Tektronix 4014 terminal emulation, Diablo 630, and ANSI 3.64—the printer is able to run a vast array of applications software.

*Concept Technologies Inc., PO Box 5277, Portland, Ore. 97208; (503) 684-3314. $7995.* **CIRCLE 325**

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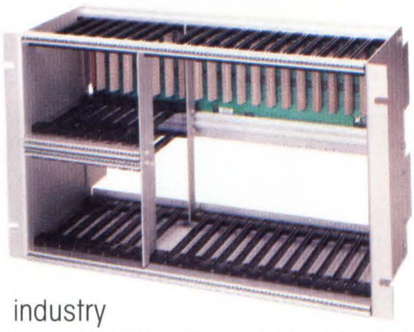

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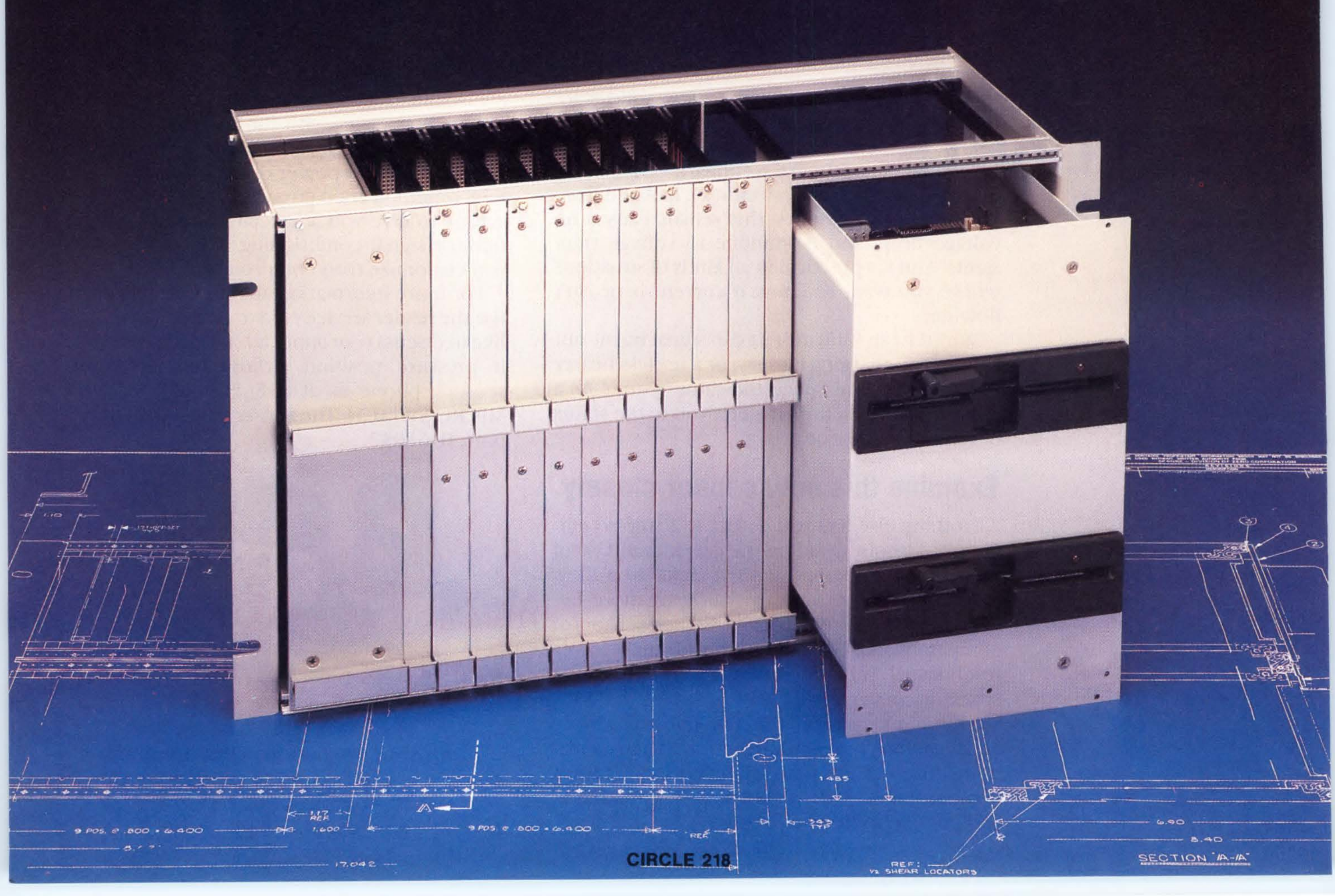

CIRCLE 218


# Sight for Sore Eyes

Hitachi helps you reduce user eye fatigue by producing monochrome and color display tubes that excel in resolution, contrast, brightness and clarity. Tubes that your customers will love at first sight, because they are the result of these human-oriented breakthroughs in CRT technology:

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**Less flicker, higher contrast**
Hitachi offers long-persistence phosphors for both monochrome and color screens to cut down irritating flicker. Numerous phosphor tones allow users to specify their own monochrome display colors; color tubes can be supplied with the traditional R-G-B combination or a new R-G-Light Blue. And lower-transmission glass, ranging from clear to grey to dark tint, can help improve contrast according to your requirements.

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**HITACHI**

CIRCLE 219

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**Hitachi, Ltd.** Electronic Devices Group, New Marunouchi Bldg., 5-1, Marunouchi 1 chome, Chiyoda-ku, Tokyo 100, Japan, Tel: Tokyo (03) 212-1111, Telex: J22395, J22432, J24491, J26375 (HITACHY), Cable: HITACHY TOKYO **Hitachi America, Ltd.** Chicago Office, 500 Park Boulevard, Suite 805, Itasca, Ill. 60143, Tel: (312) 773-0700, Telex: TWX910 651 3105 (HITACHI ITAS), Fax: (312) 773-1366 San Jose Office, 2099 Gateway Place, Gateway Office Park, Suite 550, Tel: (408) 277-0134 **Hitachi Electronic Components Europe GmbH,** Hans-Pinsel-Str. 10A, 8013 Haar, München, Tel: 089-46140, Telex: 05-22593 (HITEC D) **Hitachi Electronic Components (U.K.) Ltd.,** HITEC House, 221-225 Station Road, Harrow, Middlesex, HA1 2XL, Tel: 01-861-1414, Telex: 926293 (HITEC G)

## COMPUTER PERIPHERALS

### Graphics processor boasts low cost

High-performance business and scientific color graphics can be economically produced with the 6848 graphics system, which carries a price tag of $499.95. Based on a Z80A processor, the 6848 displays up to eight colors (chosen from a palette of 16) in a user-programmable 640-by-480, 640-by-400, or 640-by-240 format.

System hardware includes a power supply, a 192-kbyte video RAM (which can be used as a print buffer), and a 12-kbyte EPROM. It also has an RGB monitor interface, plus an RS-232-C serial port and a parallel printer port. The 6848 provides RS-170 composite video with a 16-level gray scale.

*Ultratek Co., 409 S. Raymond Ave., Alhambra, Calif. 91803; (818) 282-9056.*

**CIRCLE 326**



### Display terminal offers DEC/Tek-compatibility

Offered as a stand-alone terminal or as a retrofit board for the Zenith Z29 terminal, the GP-29 features Tektronix-compatible graphics and DEC-compatible text-mode operation. The terminal features 128 kbytes of off-screen memory for storing up to 75 pages of text and advanced graphics features, such as a dual memory plane. With the memory plane, the user can create graphics with shades of gray or overlay two separate images on the screen.

In the graphics mode, the GP-29 provides both 512-by-250-pixel resolution and a higher 1024-by-500-pixel resolution. It also has four standard text display formats: 80 by 24, 80 by 49, 132 by 24, and 132 by 49.

*Northwest Digital Systems, PO Box 15288, Seattle, Wash. 98115; (206) 524-0014. $1695 (terminal) and $995 (retrofit board).* **CIRCLE 327**

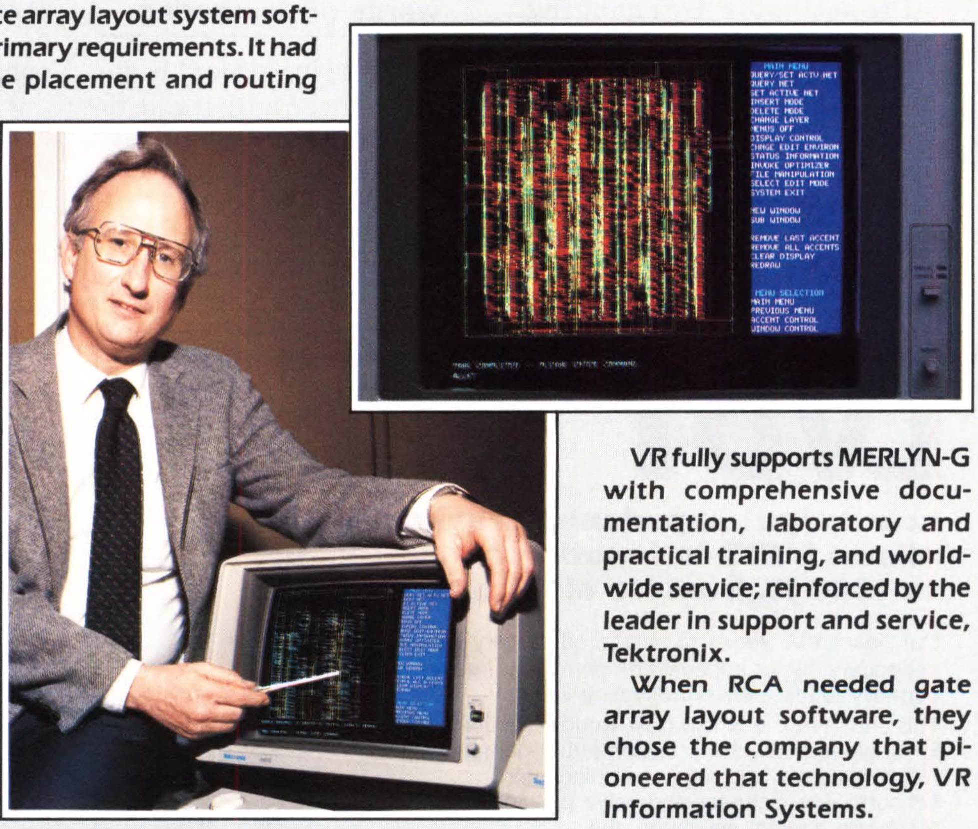
# MERLYN-G®

## Automated Layout System

# JOINS THE RCA MEGAFORCE℠

"When we were choosing gate array layout system software, we needed to meet four primary requirements. It had to offer full automation of the placement and routing functions, for rapid error-free design turnaround. It had to be expandable up to 6000 gates or more. It had to be style and technology independent, and it had to be fully supported. RCA's logical choice was MERLYN-G, from VR information Systems."

Hank Miller, Manager
Semicustom Design
Systems Engineering



RCA offers a sophisticated, but easy-to-use, semicustom design automation service for CMOS IC's, using a mix of silicon gate and CMOS/SOS technology, coupled with both gate array and PaCMOS® standard cell alternative. For a competitive edge, they use the MERLYN-G layout system in second sourcing LSI Logic's 5000 HCMOS arrays, with up to 6000 gates. They needed a system that could handle this demand. MERLYN-G's architecture allows expansion up to 10,000 gates.

VR fully supports MERLYN-G with comprehensive documentation, laboratory and practical training, and worldwide service; reinforced by the leader in support and service, Tektronix.

When RCA needed gate array layout software, they chose the company that pioneered that technology, VR Information Systems.

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CIRCLE 221

## PACKAGING & MATERIALS

### Epoxy adhesive suits diverse tasks

The Metre-Grip 303 series of multipurpose epoxy adhesives is available in four viscosities, ranging from a creamy paste to a free-flowing liquid, to suit a wide variety of bonding applications. The asbestos-free adhesive is easily mixed using equal amounts of both the base and the activator. By changing the ratio of proportions, Metre-Grip 303 can be made more flexible or more rigid. It can be used on all common materials, as well as on difficult to bond substrates such as Teflon, Tedlar, nylon, polyethylene, and vinyl.

Typical values include a flexural strength and a tensile strength of $5.0 \times 10^4$ and $2.3 \times 10^4$ psi, respectively. Shear strength at 77°F for, say, aluminum to aluminum bonding, is typically 3200 psi.

*Metachem Corp., 1505 Main St., West Warwick, R.I. 02893; (401) 822-9300.* **CIRCLE 328**

### Component sealant wards off tampering

A fast-drying sealant is applied over adjustable or removable components to prevent tampering. The Scotch-Seal 1252 sealant protects settings and calibrations of electronic equipment; seals components between assembly stages; and aids in the visual inspection of subassembly components, compartments, equipment, and parts that have been restricted to adjustment, alteration, or access by authorized personnel only.

The fire-retardant sealant resists temperatures up to 200°F without loss of adhesion. Scotch-Seal 1252 has an average bond shear strength of 170 psi on metal components.

*3M, Adhesives, Coatings, and Sealers Division, 223-1N, 3M Center, St. Paul, Minn. 55144; (612) 733-1110.*

**CIRCLE 329**

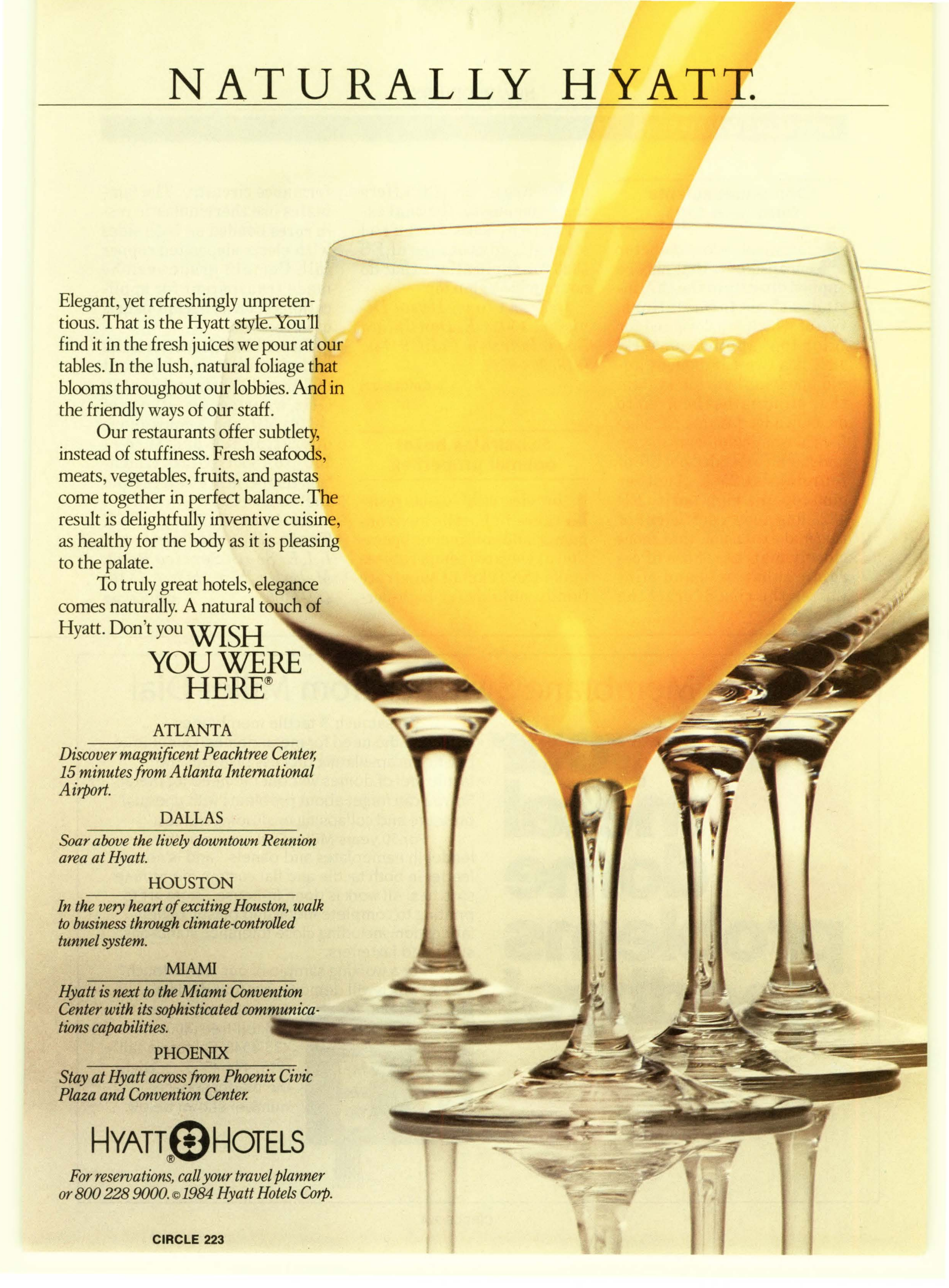




### Hardeners customize potting compound

An epoxy-based casting resin for potting and encapsulating electrical or electronic components is available with a choice of four hardeners to tailor the final casting properties and to accommodate a wide variety of processing conditions. Called Isochem resin 1251, the material has a volume resistivity of greater than $10^{14}$ Ω-cm at 25°C and a dielectric strength of greater than 450 V/mm. Its low coefficient of thermal expansion and low shrinkage characteristics reduce or eliminate stress that can damage sensitive components, as well as eliminate cracking of the casting during thermal cycling or shock.

*Isochem Products Co., 99 Cook St., Lincoln, R.I. 02865; (401) 723-2100.* **CIRCLE 330**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CIRCLE 223

## Chip encapsulants form glob tops

A family of semiconductor encapsulants that may be applied directly to the chip includes three formulations, two of which are designed for "glob top" applications. ES 4321 is a two-component liquid epoxy anhydride system that eliminates the need to develop a lead frame package for the semiconductor device and has an extended pot life of four days at 25°C. Another glob top, the high-purity ED 4323 has a low coefficient of thermal expansion that more closely matches those of ceramic substrates and minimizes the risk of cracking under stress. ES 4322 offers the same purity, thermal expansion, and flexural strength advantages of ES 4323 for applications that do not require a glob top.

*Dexter Corp., Hysol Division, 15051 E. Don Julian Road, Industry, Calif. 91749; (818) 968-6511.*

**CIRCLE 331**

## Substrates boast optimal properties

Low electrical losses, resistance to hostile environments, and continuous operation at elevated temperatures make the Tekclad substrate family suitable for high-performance circuitry. The laminates use thermoplastic resin cores bonded on both sides with electrodeposited copper foil. Certain grades can be made transparent for applications such as backlit panels or keyboards.

Functional characteristics include a dielectric constant of 3.13 at 100 kHz or 3.04 at 10 GHz, a surface resistivity of $>10^{11}$ MΩ, and a continuous operating temperature of 140° to 180°C. Glass transition temperature ranges from 190° to 225°C.

*Kollmorgen Corp., PCK Technology Division, 322 L.I.E. South Service Road, Melville, N.Y. 11747; (516) 454-4400.*

**CIRCLE 332**



**CIRCLE 224**

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CIRCLE 225

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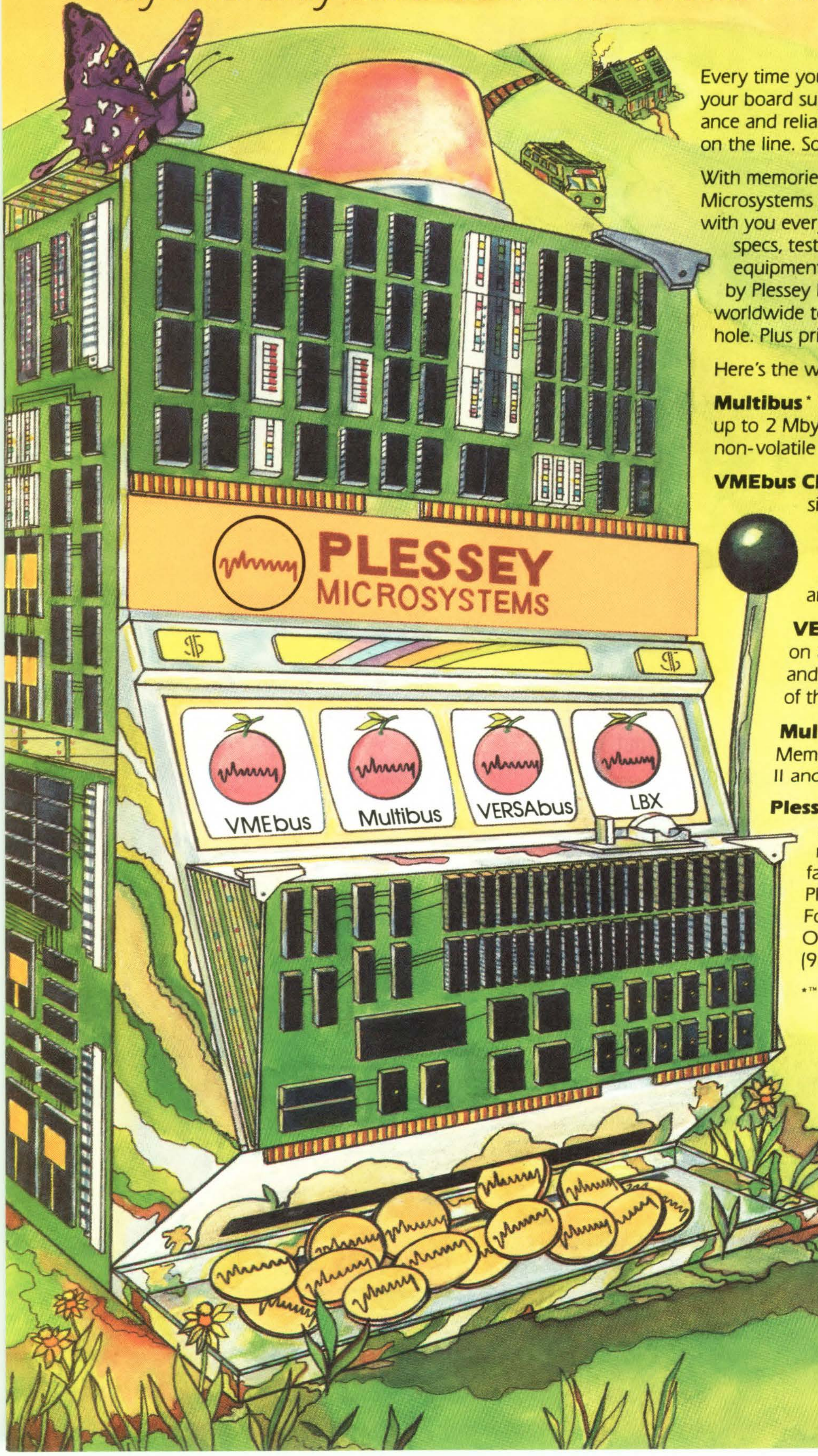


Every time you fill a slot in your system, you're betting on your board supplier. And the stakes are high. The performance and reliability of your system and your reputation are on the line. So why gamble?

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*™ Intel. †™ Motorola.

**CIRCLE 226**

**PLESSEY**
**MICROSYSTEMS**

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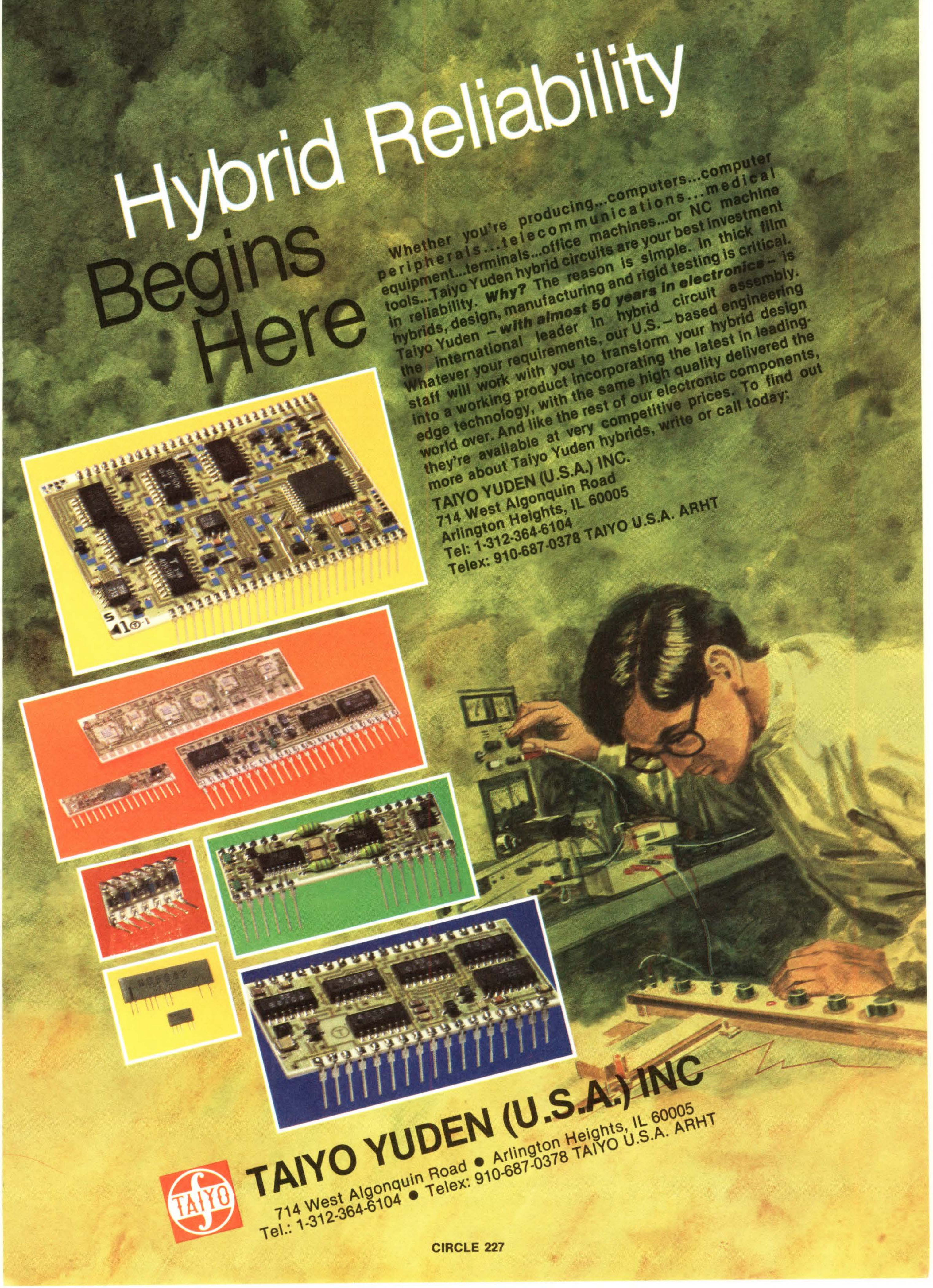
A price deal so good you have to call for details.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CIRCLE 227

# DC POWER SYSTEMS

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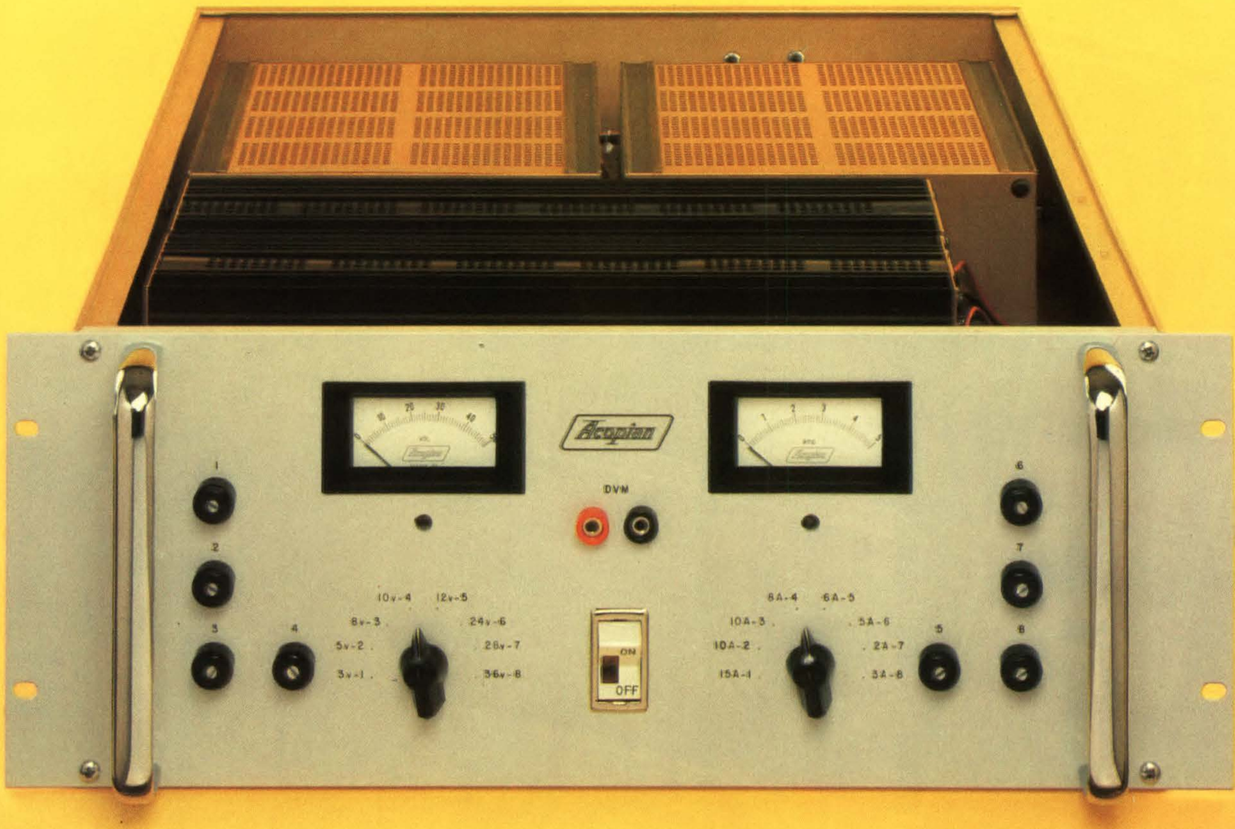
Additional information about Acopian power systems is contained in our 56-page catalog. It also describes our standard rack mounting supplies with outputs to 60 volts and to 60 amps, as well as redundant output power systems and a comprehensive line of modular power supplies. Write or call for your copy.

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**CIRCLE 228**

# Nichicon Performance

## Keeps us the high temperature capacitor choice

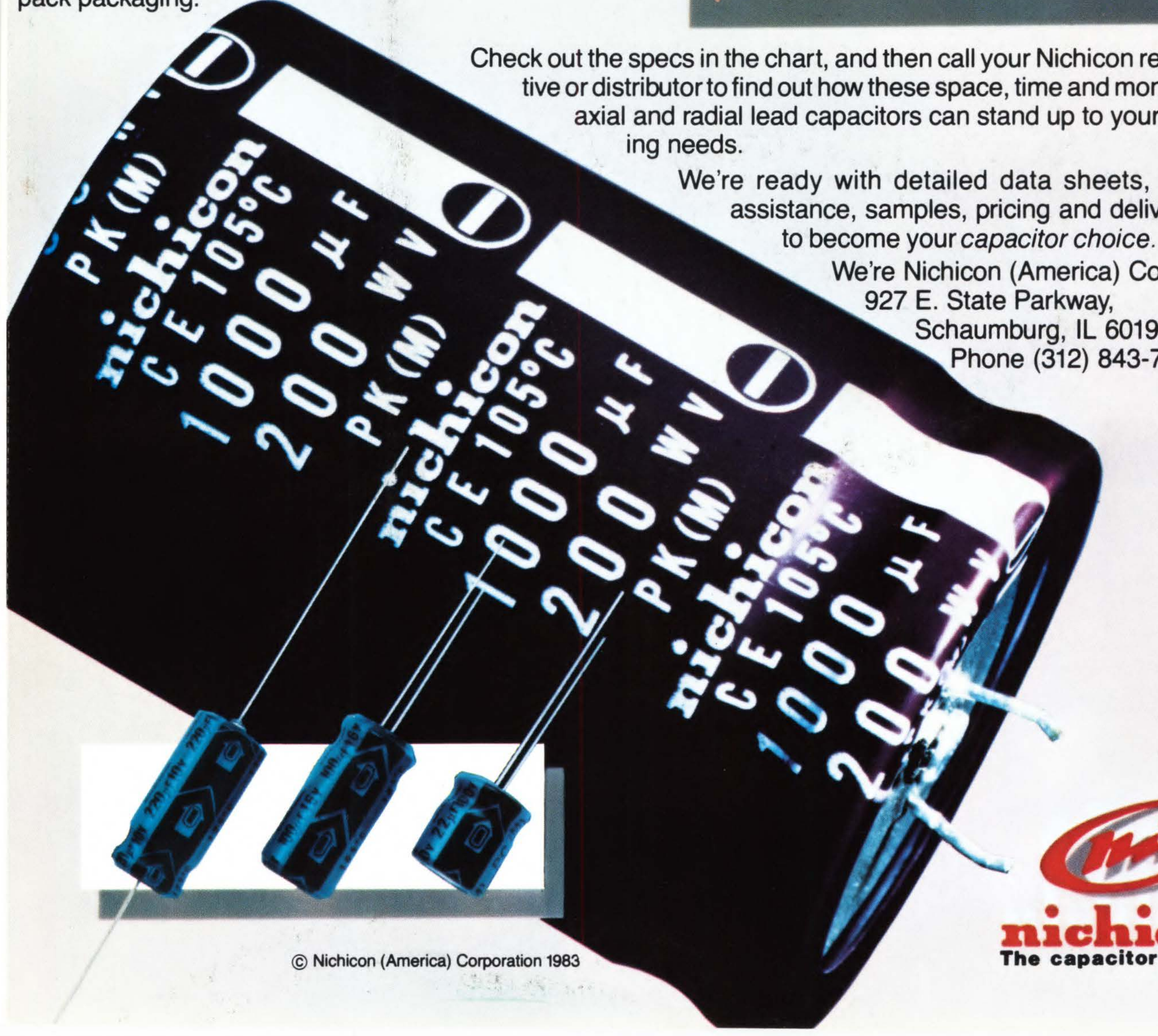
At Nichicon our capacitors are taking a lot of heat and our customers are loving every minute of it. Right up to 125°C.

Because they've discovered that Nichicon has combined high reliability performance with a price that's sure to help any cost reduction program work.

Nichicon PC, BB, BE and PK Series capacitors are available now, ready for delivery and come in your choice of standard bulk, taped and reeled or ammo-pack packaging.

**NICHICON HIGH RELIABILITY ALUMINUM ELECTROLYTIC CAPACITORS**

| Series Type | Lead Style | Series Feature | Op. Temp. Range (°C) | Rated Voltage Range (V.DC) | Capacitance Range ($\mu$F) |
|---|---|---|---|---|---|
| PC | Radial (U)<br>Axial (T) | Extended Temp. Range<br>Miniature Size | −55∽+105<br>−40∽+105 | 6.3∽100 | 0.1∽10,000 |
| BB | Radial (U)<br>Axial (T) | High Temp. Range<br>High Reliability<br>(+105°C, 3,000 hrs.) | −40∽+105 | 10∽100 | 0.47∽1,000 |
| BE | Radial (U)<br>Axial (T) | High Temp. Range<br>High Reliability<br>(+125°C, 2,000 hrs.) | −40∽+125 | 10∽50 | 0.47∽470 |
| PK | Snap-in (HS) | High Temp. Range<br>(+105°C) High Ripple Capability | −40∽+105 | 200,250 | 150∽1,000 |




Check out the specs in the chart, and then call your Nichicon representative or distributor to find out how these space, time and money saving axial and radial lead capacitors can stand up to your demanding needs.

We're ready with detailed data sheets, technical assistance, samples, pricing and delivery dates to become your *capacitor choice.*

We're Nichicon (America) Corporation,
927 E. State Parkway,
Schaumburg, IL 60195.
Phone (312) 843-7500.

**nichicon®**
**The capacitor choice.**

# Nichicon gives you your capacitor choice

## Miniature Aluminum Electrolytic Capacitors

| Series Type | Features | Operating Temp (°C) | D.C. Leakage Current (µA) | Construction | Rated Voltage Range (V. DC) | Capacitance Range (µF) | Standard Capacitance Tol. (%) |
|---|---|---|---|---|---|---|---|
| LB | • Smaller Standard Size<br>• Greater CV Density<br>• General Purpose | −40~+85 | 0.03CV (A*)<br>(4µA Min.−U)<br>(3µA Min.−T) | Radial (U) | 6.3~100 | 0.1~10,000 | ±20 (M) |
| | | | | Axial (T) | 6.3~100 | 0.47~33,000 | ±20 (M) |
| HU | • High Voltage | −25~+85 | 0.06CV +10 (C*) | Radial (U) | 160~450 | 1~100 | −10~+50 (T) |
| | | | | Axial (T) | 160~450 | 1~470 | −10~+50 (T) |
| BU | • Compact Size<br>• 3-Lead or 2-Lead Type | −40~+85 | 0.03CV (A*) | Radial (U) | 6.3~100 | 680~33,000 | ±20 (M) |
| VS•VH | • Low Profile Design<br>• Small Diameter Design | −40~+85 | 0.01CV (A*)<br>(3µA Min.) | Radial (U) | 6.3~50 | 0.1~3,300 | ±20 (M) |
| KB | • Low Leakage<br>• Tantalum Replacement | −40~+85 | 0.002CV (B*)<br>(0.4µA Min.−U)<br>(1µA Min.−T) | Radial (U) | 6.3~100 | 0.1~100 | ±20 (M)<br>±10 (K) |
| | | | | Axial (T) | 6.3~100 | 0.47~100 | ±20 (M)<br>±10 (K) |
| SA | • Super Miniature (4x7 mm Min.)<br>• Tantalum Replacement | −40~+85 | 0.01CV (B*)<br>(3µA Min.) | Radial (U) | 6.3~63 | 0.1~100 | ±20 (M) |
| SL | • Super Miniature (4x7 mm Min.)<br>• Low Leakage<br>• Tantalum Replacement | −40~+85 | 0.002CV (B*)<br>(0.4µA Min.) | Radial (U) | 6.3~63 | 0.1~100 | ±20 (M) |
| MA | • Ultra-Miniature Size<br>• Smallest Size 4x5 mm<br>• Tantalum Replacement | −40~+85 | 0.01CV (B*)<br>(3µA Min.) | Radial (U) | 4~50 | 0.1~100 | ±20 (M) |
| EB | • Non-Polarized | −40~+85 | 0.03CV (C*)<br>(3µA Min.) | Radial (U) | 6.3~100 | 0.47~1,000 | ±20 (M) |
| | | | | Axial (T) | 6.3~100 | 0.47~3,300 | ±20 (M) |

## Miniature High Temperature Capacitors

| Series Type | Features | Operating Temp (°C) | D.C. Leakage Current (µA) | Construction | Rated Voltage Range (V. DC) | Capacitance Range (µF) | Standard Capacitance Tol. (%) |
|---|---|---|---|---|---|---|---|
| IB | • High Temp. (+105°C)<br>• General Purpose | −40~+105 | 0.03CV (C*)<br>(3µA Min.) | Radial (U) | 6.3~100 | 0.1~10,000 | ±20 (M) |
| | | | | Axial (T) | 10~100 | 0.47~6,800 | ±20 (M) |
| BB | • High Temperature<br>• Low Leakage | −40~+105 | 0.002CV (C*)<br>(2µA Min.) | Radial (U) | 10~100 | 0.47~1,000 | ±20 (M) |
| | | | | Axial (T) | 10~100 | 0.47~1,000 | ±20 (M) |
| BE | • High Temp. (+125°C)<br>• Low Leakage | −40~+125 | 0.002CV (C*)<br>(2µA Min.) | Radial (U) | 10~50 | 0.47~470 | ±20 (M) |
| | | | | Axial (T) | 10~50 | 0.47~470 | ±20 (M) |
| PC | • Low ESR<br>• Wide Temp. Range | −55~+105 | 0.03CV (A*)<br>(4µA Min.) | Radial (U) | 6.3~100 | 0.47~10,000 | ±20 (M) |

## Miniature Special Application Capacitors

| Series Type | Features | Operating Temp (°C) | D.C. Leakage Current (µA) | Construction | Rated Voltage Range (V. DC) | Capacitance Range (µF) | Standard Capacitance Tol. (%) |
|---|---|---|---|---|---|---|---|
| DB<br>FB<br>GB | • Bi-Polar For Audio Crossover | −40~+85 | 0.03CV (C*)<br>(3µA Min.) | Radial (U) | 50 | 1~100 | ±20 (M) |
| | | | | Axial (T) | 50 | 1~68 | ±20 (M) |
| TM | • For Timing Circuits<br>• Very Stable at High Temp. | −40~+85 | 0.001CV +1µA<br>(B*) | Radial (U) | 10~50 | 1~470 | ±20 (M)<br>±10 (K) |
| PA | • Low ESR, Switching Regulators<br>• High Ripple, High Frequency | −55~+105 | 0.002CV (C*)<br>(2µA Min.) | Radial (U) | 6.3~200 | 1~1,000 | ±20 (M) |
| HU | • High Voltage<br>• For Switching Regulators | −25~+85 | 0.06CV +10 (C*) | Radial (U) | 200~250 | 10~680 | −10~+50 (T) |
| | | | | Axial (T) | 200~250 | 10~680 | −10~+50 (T) |
| PX | • Low ESR<br>• Smaller Package<br>• High Ripple | −55~+105 | 0.03CV (A*) | Radial (U) | 6.3~63 | 22~2,200 | ±20 (M) |

## Can Type Lytics

| Series Type | Features | Operating Temp (°C) | D.C. Leakage Current (µA) | Construction | Rated Voltage Range (V. DC) | Capacitance Range (µF) | Standard Capacitance Tol. (%) |
|---|---|---|---|---|---|---|---|
| KD | • Lug Terminal | −40~+85<br>(16~100V)<br>−25~+85<br>(160~500V) | $3\sqrt{CV}$ (C*) | Can (L) | 16~500 | 22~68,000 | −10~+50 (T) |
| HL•LL | • Snap-in Terminal for P.C.B. Mount | −40~+85<br>(16~100V)<br>−25~+85<br>(160~200V) | $3\sqrt{CV}$ (C*) | Can (L) | 16~200 | 220~15,000 | −10~+30 (Q) |
| NW<br>NK<br>NS<br>NH | • Computer Grade | −25~+85 | $3\sqrt{CV}$ (C*) | Can (L) | 6.3~450 | 120~1,000,000<br>(1F) | −10~+100 (T)<br>−10~+50 (T)<br>−10~+100 (W)<br>−10~+75 (U) |
| PS | • Snap-in Term., P.C.B. Mount<br>• For Switching Regulators | −40~+85 | $3\sqrt{CV}$ (C*) | Can (L) | 160~450 | 47~1,000 | −20~+20 (M) |
| PK | • High Ripple, Switching Reg.<br>• Extended Temp. Range<br>• Snap-in Terminal | −40~+105 | $3\sqrt{CV}$ (C*) | Can (L) | 200~250 | 150~1,000 | −20~+20 (M) |
| GM | • High Ripple, Switching Reg.<br>• Extended Temp. Range<br>• Snap-in Terminal | −25~+105<br>(400V)<br>−40~+105<br>(160~250V) | $3\sqrt{CV}$ (C*) | Can (L) | 160~450 | 47~1,000 | −20~+20 (M) |
| FL | • Low Profile<br>• Snap-in Terminal<br>• For Switching Regulators | −40~+85 | $3\sqrt{CV}$ (C*) | Can (L) | 160~250 | 82~270 | −20~+20 (M) |

## Class III Semiconductive Ceramics

| Series Type | Rated Voltage (V. DC) | T.C. | Capacitance (µF) | Standard Capacitance Tolerance | Insulation Resistance (MΩ) |
|---|---|---|---|---|---|
| H | 12 | Y5S | 0.022~0.47 | ±20% (M), +80−20% (Z) | 0.022−0.1µF−1 Min. at 12V<br>0.22µF−0.5 Min. at 12V<br>0.33µF−0.33 Min. at 12V<br>0.47µF−0.25 Min. at 12V |
| | 25 | Y5T | 0.01~0.1 | ±20% (M), +80−20% (Z) | 1,000 Min. at 25V |
| | 50 | Y5V<br>Y5T | 0.01~0.1 | Y5V: +80−20% (Z)<br>Y5T: +20% (M), +80−20% (Z) | 1,000 Min. at 50V |

## Polyester Capacitors

| Series Type | Rated Voltage (V. DC) | Capacitance (µF) | Standard Capacitance Tolerance | Insulation Resistance | D.F. |
|---|---|---|---|---|---|
| QYA | 100 | 0.001~0.47 | ±5% (J), ±10% (K), ±2% (M) | 9,000MΩMin. | 1.0% Max. at 1kHz |
| QXM (Radial) | 250, 400, 630 | 0.01~2.2 | ±5% (J), ±10% (K), ±20% (M) | ≤0.33µF-9,000 MΩMin. | 1.0% Max. at 1kHz |
| QAM (Axial) | 250, 400, 630 | 0.15~10 | ±5% (J), ±10% (K), ±20% (M) | ≥0.33µF-3,000 MΩMin. | |
| QAL | 125V. AC | 0.0047~0.22 | ±10% (K), ±20% (M) | 9,000MΩMin.<br>at 100V. DC 1 Min. | 1.0% Max. at 1kHz |

(A*)=Leakage Current after 1 minute (B*)=Leakage Current after 2 minutes (C*)=Leakage Current after 5 minutes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# ALUMINUM ELECTROLYTIC CAPACITORS

**FOR SWITCHING REGULATORS—SNAP-IN TERMINAL**
**GM • PK SERIES**
**HIGH TEMPERATURE**

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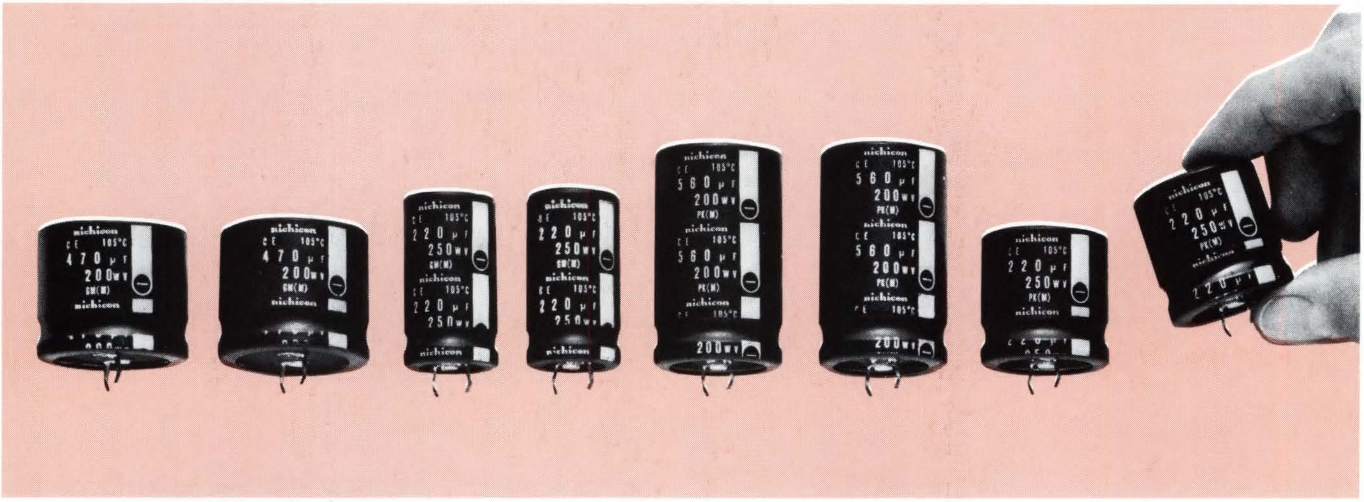
CAT.NAC-PK083

Replaces CAT.NAC-PK102

## CAN TYPE-TYPE L—GM • PK SERIES




**The Nichicon GM and PK Series** of can type aluminum electrolytic capacitors have been designed specifically to meet the high reliability and performance requirements of switching regulators. Both Series feature high temperature reliability and snap-in, positive contact leads which eliminate mounting hardware.

**The GM Series** offers +105°C reliability in case sizes comparable to +85°C units. The Series has a capacitance range of 47µF through 1,000µF and a voltage range of 160V. DC through 400V. DC. Case sizes range from 22 x 25mm to 35 x 50mm. The 400V. units are ideal for switching regulators which will be used for European export.

**The PK Series** offers twice the ripple capability of Nichicon's popular PS Series. Yet, the PK Series offers real estate saving advantages with unit case sizes of just 25 x 25mm through 35 x 50mm. The PK Series features: Operating temperature, −40°C through +105°C; Capacitance range, 150µF through 1,000µF; Voltage range, 200V. and 250V.

**PART NUMBERING SYSTEM** L GM 2D 471 M HS A

- L — Type construction (Large Can Type Aluminum Electrolytic Capacitor)
- GM — Series type (GM Series)
- 2D — Rated voltage code (200V)

| Rated Voltage | 160V | 200V | 250V | 400V |
|---|---|---|---|---|
| Code | 2C | 2D | 2E | 2G |

- 471 — Nominal capacitance
  The nominal capacitance value in microfarad (µF) is expressed by a three-digit number. The first two-digits represent significant figures and the last digit indicates the number of zeroes to follow.
  **EXAMPLE:** 470µF=471 and 1,000µF=102
- M — Capacitance tolerance (M= −20 ~ +20%)
- HS — Terminal shape (Snap-in terminal)
- A — Case diameter code

| Code | Z | A | B | C |
|---|---|---|---|---|
| Dimensions mm | 22 | 25 | 30 | 35 |
| Dimensions inch | .866 | .984 | 1.181 | 1.378 |

**STANDARD:** JIS C 5141: Characteristic W

**OPERATING TEMPERATURE RANGE:**

GM Series (160  250V) −40 ~ +105°C
GM Series (400V) −25 ~ +105°C
PK Series (200V, 250V) −40 ~ +105°C

**CAPACITANCE AND TOLERANCE:** Capacitance measurements shall be made by the bridge method at a frequency of $120Hz^{+10}_{-5}Hz$. A maximum of 1 volt RMS shall be applied during measurement.

The capacitance shall be within the specified tolerance of ±20% of the standard GM or PK Series.

**LEAKAGE CURRENT:** Measurement shall be made at rated DC voltage with an application of a steady source of power, such as a regulated power supply. A current-limiting resistor of 1,000 ohms shall be connected in series with each capacitor under test. Rated DC working voltage shall be applied to the capacitor for 5 minutes before making the leakage current measurements.

The maximum leakage current for any capacitor shall not exceed the value determined from the following equation:

$$I \leq 3\sqrt{CV}$$

where: I = Leakage current (µA)
C = Nominal capacitance (µF)
V = Rated DC voltage (V.DC)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# ALUMINUM ELECTROLYTIC CAPACITORS

## FOR SWITCHING REGULATORS—SNAP-IN TERMINAL
## GM • PK SERIES
## HIGH TEMPERATURE

nichicon

## PK SERIES

| Rated V. | 200 | | | | 250 | | | |
|---|---|---|---|---|---|---|---|---|
| Surge V. | 250 | | | | 300 | | | |
| Cap. (μF.) | Case Dia. | Dimensions | Ripple Current | ESR | Case Dia. | Dimensions | Ripple Current | ESR |
| 150 | A | 25 x 25<br>.984 x .984 | 1.25 | 1.11 | A | 25 x 30<br>.984 x 1.181 | 1.30 | 1.11 |
| 220 | A | 25 x 30<br>.984 x 1.181 | 1.65 | 0.75 | A | 25 x 40<br>.984 x 1.575 | 1.80 | 0.75 |
| | B | 30 x 25<br>1.181 x .984 | 1.65 | 0.75 | B | 30 x 30<br>1.181 x 1.181 | 1.80 | 0.75 |
| 270 | A | 25 x 40<br>.984 x 1.575 | 1.95 | 0.61 | B | 30 x 30<br>1.181 x 1.181 | 2.00 | 0.61 |
| | B | 30 x 30<br>1.181 x 1.181 | 1.95 | 0.61 | | | | |
| 330 | B | 30 x 30<br>1.181 x 1.181 | 2.20 | 0.50 | A | 25 x 50<br>.984 x 1.969 | 2.30 | 0.50 |
| | | | | | B | 30 x 40<br>1.181 x 1.575 | 2.30 | 0.50 |
| | | | | | C | 35 x 30<br>1.378 x 1.181 | 2.30 | 0.50 |
| 390 | B | 30 x 40<br>1.181 x 1.575 | 2.50 | 0.42 | C | 35 x 35<br>1.378 x 1.378 | 2.60 | 0.42 |
| | C | 35 x 30<br>1.378 x 1.181 | 2.50 | 0.42 | | | | |
| 470 | B | 30 x 40<br>1.181 x 1.575 | 2.80 | 0.35 | B | 30 x 50<br>1.181 x 1.969 | 3.00 | 0.35 |
| | C | 35 x 30<br>1.378 x 1.181 | 2.80 | 0.35 | C | 35 x 40<br>1.378 x 1.575 | 3.00 | 0.35 |
| 560 | B | 30 x 50<br>1.181 x 1.969 | 3.30 | 0.29 | | | | |
| | C | 35 x 35<br>1.378 x 1.378 | 3.10 | 0.29 | | | | |
| 680 | C | 35 x 40<br>1.378 x 1.575 | 3.60 | 0.24 | C | 35 x 50<br>1.378 x 1.969 | 3.80 | 0.24 |
| 820 | C | 35 x 50<br>1.378 x 1.969 | 4.15 | 0.20 | | | | |
| 1,000 | C | 35 x 50<br>1.378 x 1.969 | 4.50 | 0.17 | | | | |

**DIMENSIONS: Diameter ($D^{\phi}$) x Length (L) = $\frac{\text{mm}}{\text{inch}}$**

NOTE:

**Case Diameter Code** =

| Code | Nominal Case Diameter |
|---|---|
| Z | 22mm/.866" |
| A | 25mm/.984" |
| B | 30mm/1.181" |
| C | 35mm/1.378" |

**Ripple Current** = Maximum Ripple Current in Amp-RMS (At 120Hz, +85°C)

**E.S.R.** = Maximum Equivalent Series Resistance in Ohms (At 120Hz, +20°C)

**RIPPLE CURRENT CALCULATIONS:** Nichicon GM and PK Series electrolytic capacitors will withstand RMS ripple currents at the frequency of 120Hz and a temperature of +85°C as listed in the standard products table.

1. Where Nichicon GM and PK Series capacitors are operated at a temperature other than +85°C, the allowable RMS ripple current listed must be multiplied by the factor shown below:

Maximum RMS Ripple Current Multiplying Factor vs. Temperature

| 20°C | 45°C | 60°C | 70°C | 85°C | 105°C |
|---|---|---|---|---|---|
| 1.50 | 1.48 | 1.42 | 1.30 | 1.00 | 0.50 |

2. If Nichicon GM and PK Series capacitors are used at a frequency other than 120Hz, the rated 120Hz RMS ripple current listed must be multiplied by the appropriate factor shown below:

Maximum RMS Ripple Current Multiplying Factor vs. Frequency

| Series | 60Hz | 120Hz | 1kHz | 10kHz | 50kHz |
|---|---|---|---|---|---|
| GM•PK (160 ~ 250V.) | 0.8 | 1.00 | 1.50 | 1.60 | 1.63 |
| GM (400V.) | 0.9 | 1.00 | 1.15 | 1.15 | 1.15 |

# ALUMINUM ELECTROLYTIC CAPACITORS

**FOR SWITCHING REGULATORS–SNAP-IN TERMINAL**
**GM • PK SERIES**
**HIGH TEMPERATURE**

nichicon

## STANDARD PRODUCTS TABLE–GM SERIES

| Rated V. | 160 | | | | 200 | | | | 250 | | | | 400 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Surge V. | 200 | | | | 250 | | | | 300 | | | | 450 | | | |
| Capacitance (μF) | Case Dia. | Dimensions | Ripple Current | ESR | Case Dia. | Dimensions | Ripple Current | ESR | Case Dia. | Dimensions | Ripple Current | ESR | Case Dia. | Dimensions | Ripple Current | ESR |
| 47 | | | | | | | | | | | | | Z | 22 x 30<br>.866 x 1.181 | 0.36 | 10.6 |
| | | | | | | | | | | | | | A | 25 x 25<br>.984 x .984 | 0.36 | 10.6 |
| 68 | | | | | | | | | | | | | Z | 22 x 40<br>.866 x 1.575 | 0.46 | 7.30 |
| | | | | | | | | | | | | | A | 25 x 30<br>.984 x 1.181 | 0.46 | 7.30 |
| | | | | | | | | | | | | | B | 30 x 25<br>1.181 x .984 | 0.46 | 7.30 |
| 100 | | | | | | | | | Z | 22 x 25<br>.866 x .984 | 0.66 | 2,50 | Z | 22 x 50<br>.866 x 1.969 | 0.62 | 5.00 |
| | | | | | | | | | | | | | A | 25 x 40<br>.984 x 1.575 | 0.62 | 5.00 |
| | | | | | | | | | | | | | B | 30 x 30<br>1.181 x 1.181 | 0.62 | 5.00 |
| 150 | | | | | Z | 22 x 25<br>.866 x .984 | 0.82 | 1.66 | Z | 22 x 30<br>.866 x 1.181 | 0.88 | 1.66 | B | 30 x 40<br>1.181 x 1.575 | 0.84 | 3.30 |
| | | | | | | | | | A | 25 x 25<br>.984 x .984 | 0.88 | 1.66 | C | 35 x 35<br>1.378 x 1.378 | 0.84 | 3.30 |
| 220 | Z | 22 x 30<br>.866 x 1.181 | 0.98 | 1.13 | Z | 22 x 35<br>.866 x 1.378 | 1.14 | 1.13 | Z | 22 x 40<br>.866 x 1.575 | 1.24 | 1.13 | C | 35 x 50<br>1.378 x 1.969 | 1.12 | 2.30 |
| | A | 25 x 25<br>.984 x .984 | 0.98 | 1.13 | A | 25 x 25<br>.984 x .984 | 1.14 | 1.13 | A | 25 x 35<br>.984 x 1.378 | 1.24 | 1.13 | | | | |
| | | | | | | | | | B | 30 x 25<br>1.181 x .984 | 1.24 | 1.13 | | | | |
| 330 | Z | 22 x 40<br>.866 x 1.575 | 1.42 | 0.75 | Z | 22 x 40<br>.866 x 1.575 | 1.50 | 0.75 | A | 25 x 45<br>.984 x 1.772 | 1.68 | 0.75 | | | | |
| | A | 25 x 30<br>.984 x 1.181 | 1.42 | 0.75 | A | 25 x 35<br>.984 x 1.378 | 1.50 | 0.75 | B | 30 x 35<br>1.181 x 1.378 | 1.68 | 0.75 | | | | |
| | B | 30 x 25<br>1.181 x .984 | 1.42 | 0.75 | B | 30 x 25<br>1.181 x .984 | 1.50 | 0.75 | C | 35 x 30<br>1.378 x 1.181 | 1.68 | 0.75 | | | | |
| 470 | Z | 22 x 50<br>.866 x 1.969 | 1.90 | 0.53 | A | 25 x 45<br>.984 x 1.772 | 2.08 | 0.53 | B | 30 x 50<br>1.181 x 1.969 | 2.22 | 0.53 | | | | |
| | A | 25 x 40<br>.984 x 1.575 | 1.90 | 0.53 | B | 30 x 35<br>1.181 x 1.378 | 2.08 | 0.53 | C | 35 x 35<br>1.378 x 1.378 | 2.22 | 0.53 | | | | |
| | B | 30 x 30<br>1.181 x 1.181 | 1.90 | 0.53 | C | 35 x 30<br>1.378 x 1.181 | 2.08 | 0.53 | | | | | | | | |
| 560 | A | 25 x 45<br>.984 x 1.772 | 2.20 | 0.44 | A | 25 x 50<br>.984 x 1.969 | 2.28 | 0.44 | B | 30 x 50<br>1.181 x 1.969 | 2.54 | 0.44 | | | | |
| | B | 30 x 35<br>1.181 x 1.378 | 2.20 | 0.44 | B | 30 x 40<br>1.181 x 1.575 | 2.28 | 0.44 | | | | | | | | |
| | C | 35 x 30<br>1.378 x 1.181 | 2.20 | 0.44 | C | 35 x 35<br>1.378 x 1.378 | 2.28 | 0.44 | | | | | | | | |
| 680 | A | 25 x 50<br>.984 x 1.969 | 2.50 | 0.37 | B | 30 x 50<br>1.181 x 1.969 | 2.76 | 0.37 | C | 35 x 50<br>1.378 x 1.969 | 3.08 | 0.37 | | | | |
| | B | 30 x 40<br>1.181 x 1.575 | 2.50 | 0.37 | C | 35 x 35<br>1.378 x 1.378 | 2.76 | 0.37 | | | | | | | | |
| | C | 35 x 35<br>1.378 x 1.378 | 2.50 | 0.37 | | | | | | | | | | | | |
| 820 | B | 30 x 50<br>1.181 x 1.969 | 2.92 | 0.31 | B | 30 x 50<br>1.181 x 1.969 | 3.08 | 0.31 | | | | | | | | |
| | C | 35 x 35<br>1.378 x 1.378 | 2.92 | 0.31 | | | | | | | | | | | | |
| 1,000 | B | 30 x 50<br>1.181 x 1.969 | 3.40 | 0.25 | C | 35 x 50<br>1.378 x 1.969 | 3.74 | 0.25 | | | | | | | | |

**DIMENSIONS: DIAMETER (Dϕ) X LENGTH = $\frac{mm}{inch}$**

# ALUMINUM ELECTROLYTIC CAPACITORS

## FOR SWITCHING REGULATORS—SNAP-IN TERMINAL
## GM • PK SERIES
## HIGH TEMPERATURE

nichicon

**DISSIPATION FACTOR:** Measured at a frequency of 120Hz $^{+10}_{-5}$Hz, the dissipation factor shall be less than the values in *Table 1.*

*Table 1.*

| Series | Dissipation Factor (%) |
|---|---|
| GM (160 ~ 250V) | 15 |
| GM (400V) | 30 |
| PK (200V, 250V) | 10 |

**LOW TEMPERATURE CHARACTERISTICS:** When capacitors are stored at the temperatures of −40°C $^{+0}_{-3}$°C (except 400V. GM Series), −25°C $^{+0}_{-3}$°C and +20°C ±2°C respectively, the ratio of impedance measured at each test temperature with the frequency of 120 Hz$^{+10}_{-5}$Hz shall be less than the values in *Table 2.*

The capacitance change for the GM (except 400V) and PK Series at −40°C shall be no more than 25% of the initial value measured at +20°C.

The capacitance change for the 400V. Class GM Series at −25°C shall be no more than 30% of the initial value measured at +20°C.

*Table 2.*

| Series | Ratio of Impedance | |
|---|---|---|
| | Z @ −40°C / Z @ +20°C | Z @ −25°C / Z @ +20°C |
| GM (160 ~ 250V) | 15 | 4 |
| GM (400V) | — | 8 |
| PK (200V, 250V) | 12 | 3 |

**HIGH TEMPERATURE CHARACTERISTICS:** The capacitors shall be placed in an air-circulating thermostatic test chamber and be exposed to DC voltage with applied ripple current for a period of 1,000 hours for the GM Series and 2,000 hours for the PK Series at a temperature of 105°C ±2°C (shielded from direct heat radiation).

The capacitors shall then be removed from the test chamber and allowed to be stabilized at room temperature after which they shall meet each of the requirements listed in *Table 3.*

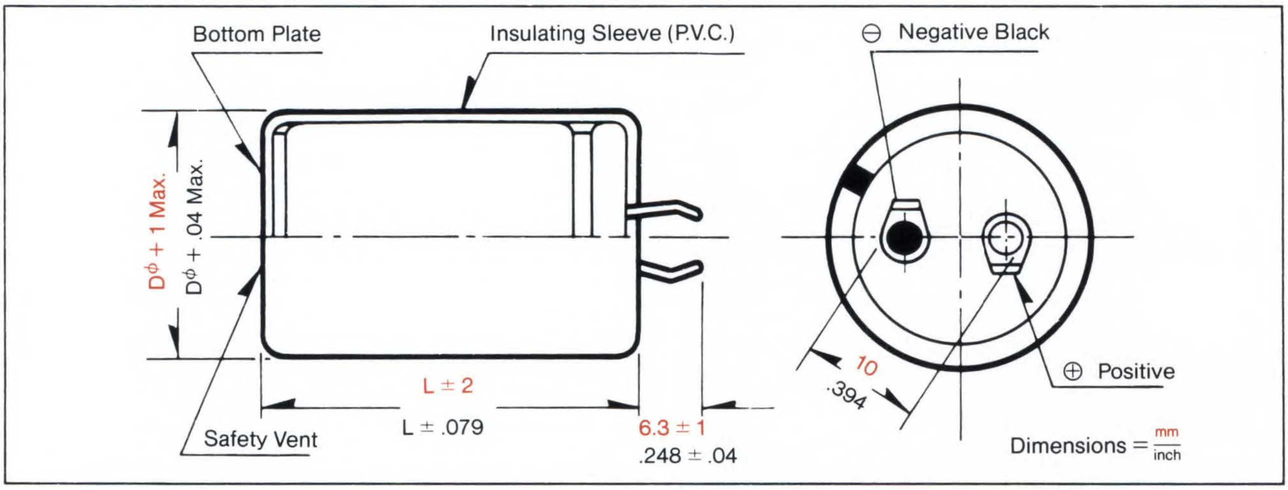
*Table 3.*

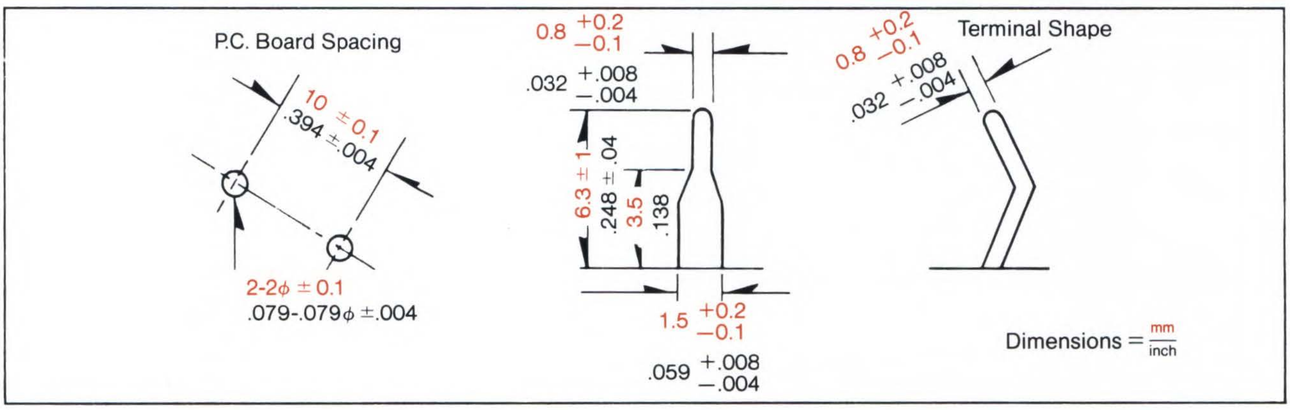
| | |
|---|---|
| Leakage current | Same as specified under Leakage Current |
| Capacitance | Within ±20% of initial measurements |
| Dissipation factor | 200% or less of values in *Table 1.* |
| Appearance | Free from leakage of electrolyte and/or other noticeable deformation |

**SHELF LIFE TEST:** Prior to testing, each capacitor in the test group is measured for capacitance, dissipation factor and DC leakage current.

Capacitors are then stored with no voltage applied at a temperature of 105°C ±2°C for 500 hours ±12 hours. Following this period the capacitors shall be removed from the test chamber and be allowed to stabilize at room temperature. Next they shall be connected to a series limiting resistor with DC rated voltage applied for 30 minutes after which the capacitors shall be discharged. After completion of these procedures, the capacitors shall meet each of the requirements as listed in *Table 3.*

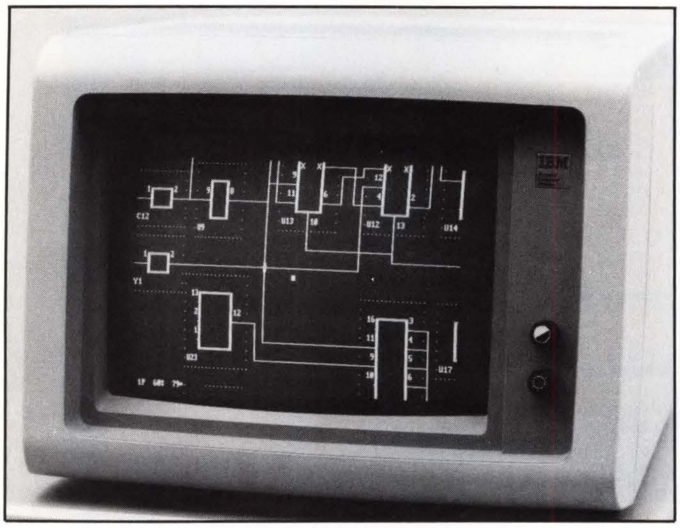
**NICHICON STANDARD TEST CONDITIONS: TESTING PERFORMED AT +20°C**



## SOFTWARE

# CAE software designs boards on IBM PCs



A software package for the IBM PC makes it easy to design and lay out printed circuit boards. The Dasoft-16 design automation system includes a component library, a design entry and schematic generation routine, an automatic router, and utilities for generating board artwork. The package, from Dasoft Design Systems, can be used to design double-sided boards up to 12.5 in. square, with wiring on a 50-mil grid.

The component library includes over 200 part types, both analog and digital.

The design entry routine allows the designer to make selections from the component library, place them on the PC's screen, and connect the devices by moving the screen cursor. All device pin numbers on network are displayed automatically; likewise, a net list is produced automatically. The plot sizes can be set for four different magnifications.

Once the schematic has been entered, with all appropriate interconnections (including power and ground lines), the automatic router takes over.

The system requires an IBM PC (or clone) with two disk drives, 256 kbytes of local memory, and an X-Y plotter for output. The complete package costs $3750 and will be available by the end of the year. The schematic entry portion, the Dasoft-168, is available separately now, for $2000.

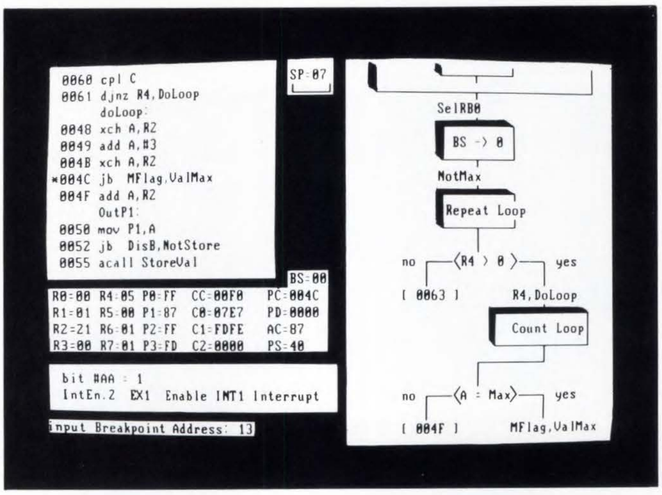
*Dasoft Design Systems Inc., 2550 Ninth St., Suite 113, Berkeley, Calif. 94710; Leslie Wieman, (415) 486-0822.*

**CIRCLE 301**

**Stephan Ohr**

**SOFTWARE**

# 8051 simulator-debugger runs on the IBM PC




The Sim-8051 gives an IBM personal computer the ability to simulate and debug programs for the 8051 single-chip microcontroller. The software, developed by Cybernetic Micro Systems, provides a powerful six-window display that shows display op codes and assembly codes, special-function registers, resister and stack pointer contents, program flow graphs, and a command line.

Similar to a previous package, the Sim-8048, introduced recently for the 8048 (ELECTRONIC DESIGN, Sept. 6, p. 299); the program has been enhanced in several ways. One major enhancement is greater feedback when a local operation is requested: When a command is selected, the requested operation is displayed in the command window.

Additionally, the software has been made very easy to use: When a programmer accesses any of the 128 fixed and 128 variable bits of the 8051's Boolean processing section, the program provides an explanation of that bit, thus saving the time that would have been spent flipping through manuals for the explanation.

A special cycle counter also has been added to help keep track of the number of times the 8051's counter completes its cycle. That, in turn, permits very long-count cycles to be examined.

The simulator-debugger costs $395, and a demonstration disk and manual $39.50. Delivery is from stock.

*Cybernetic Micro Systems Inc., PO Box 3000, San Gregorio, Calif. 94074; Ed Klingman, (415) 726-3000.*

**Dave Bursky**

**CIRCLE 308**

**SOFTWARE**

## Software lets PCs use CP/M diskettes

A software program gives IBM PC users access to data recorded on 8-bit machines using the CP/M operating system without specialized hardware or rerecording of the floppy disk. The program, which costs only $69.95, also lets users write data from the PC onto CP/M diskettes.

Micro Solutions' Uniform-PC is transparent to users, who simply insert a CP/M data diskette into the second drive of an IBM PC, PC AT, or PC XT (or compatible hardware) and run the desired application program. The system must use PC-DOS version 2.0 or higher and have one drive, either floppy- or hard-disk, for the application software and a second drive for the data diskettes.

The program works only with data diskettes, since many application packages use ROM calls or special-function keys not found on PCs or compatible machines.

The program is menu-driven, with users indicating the system used when the diskette was recorded and the type of disk drive.

All accesses and writes are made using PC-DOS commands, and the recommended system capacity is 128 kbytes, although the translation program requires less than that amount of system memory.

When an error is detected, the system displays a message on the screen and sounds a two-tone alarm. In addition, when the diskette is formatted, the program notes bad tracks and displays their location on the screen.

The software is available from stock.

*Micro Solutions Inc., 125 S. Fourth St., DeKalb, Ill. 60115; (815) 756-3411.* **CIRCLE 319**

## SOFTWARE

### Unix kit compiles C and Pascal programs

The Amsterdam Compiler Kit is a package of C and Pascal compilers (and assemblers) for a wide variety of Unix-based host and target machines, including VAX and PDP-11 computers. The kit is designed to simplify the task of producing portable compilers and interpreters needed for micro and minicomputers. Cross assemblers are provided for 8080, Z80, Z8000, 8086, 6800, 6809, 68000, and 6502 processors. The full system in source code is priced at $9950; selected binaries are priced at $4500.

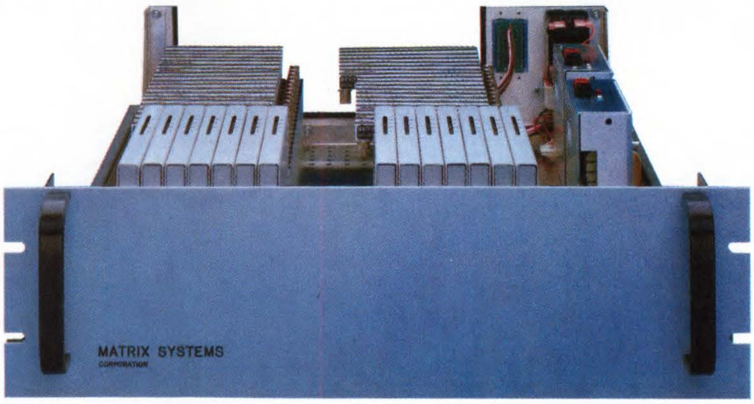
*UniPress Software Inc., 2025 Lincoln Hwy., Suite 312, Edison, N.J. 08817; (201) 985-8000.* **CIRCLE 333**

### Fortran 77 runs on IBM PC and compatibles

Providing mainframe features on an IBM PC or PC-compatible computer, F77L is a complete implementation of the ANSI Fortran 77 standard. F77L offers all of the features of Fortran 77 plus extensions that improve compatibility with IBM level H, such as being able to use a $ in a name and initialization in type statements. F77L's source file is free format; comments begin with an asterisk and continuation lines begin with an ampersand.

*Lahey Computer Systems Inc., 904 Silver Spur Road, Suite 417, Rolling Hill Estates, Calif. 90274; (213) 541-1200. $477.* **CIRCLE 334**

# Matrix Makes Switching as Easy as "OFF" or "ON"

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Whether you're switching VHF, HF, IF, video, audio or DC, Matrix Systems makes it a snap. That's because we can tailor a system to your exact needs using Reed, CMOS, or Pin Diode relays. The chart tells the story.

It pays to deal with a company like Matrix who really understands the switching business. We've been designing and delivering state-of-the-art systems for over 15 years to defense contractors, government agencies, the TV industry, ATE manufacturers - and more. Built to the toughest electrical and packaging specs imaginable.

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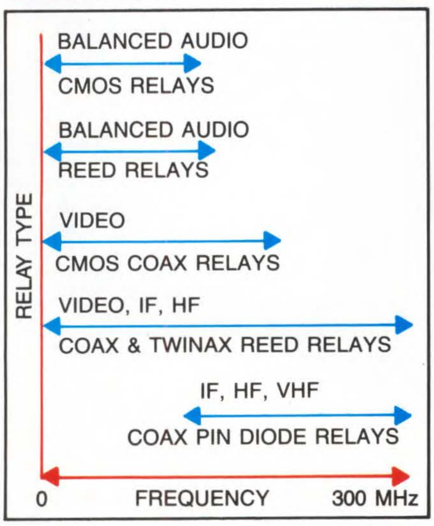
## MATRIX COVERS THE WHOLE FREQUENCY SPECTRUM




## COMPUTER COMPATIBILITY

Just apply a control input from your computer and the system will instantly route your signal to as many points as needed. 16 bit parallel interface is standard, and we also offer IEEE-488 and RS232, all with status feedback.

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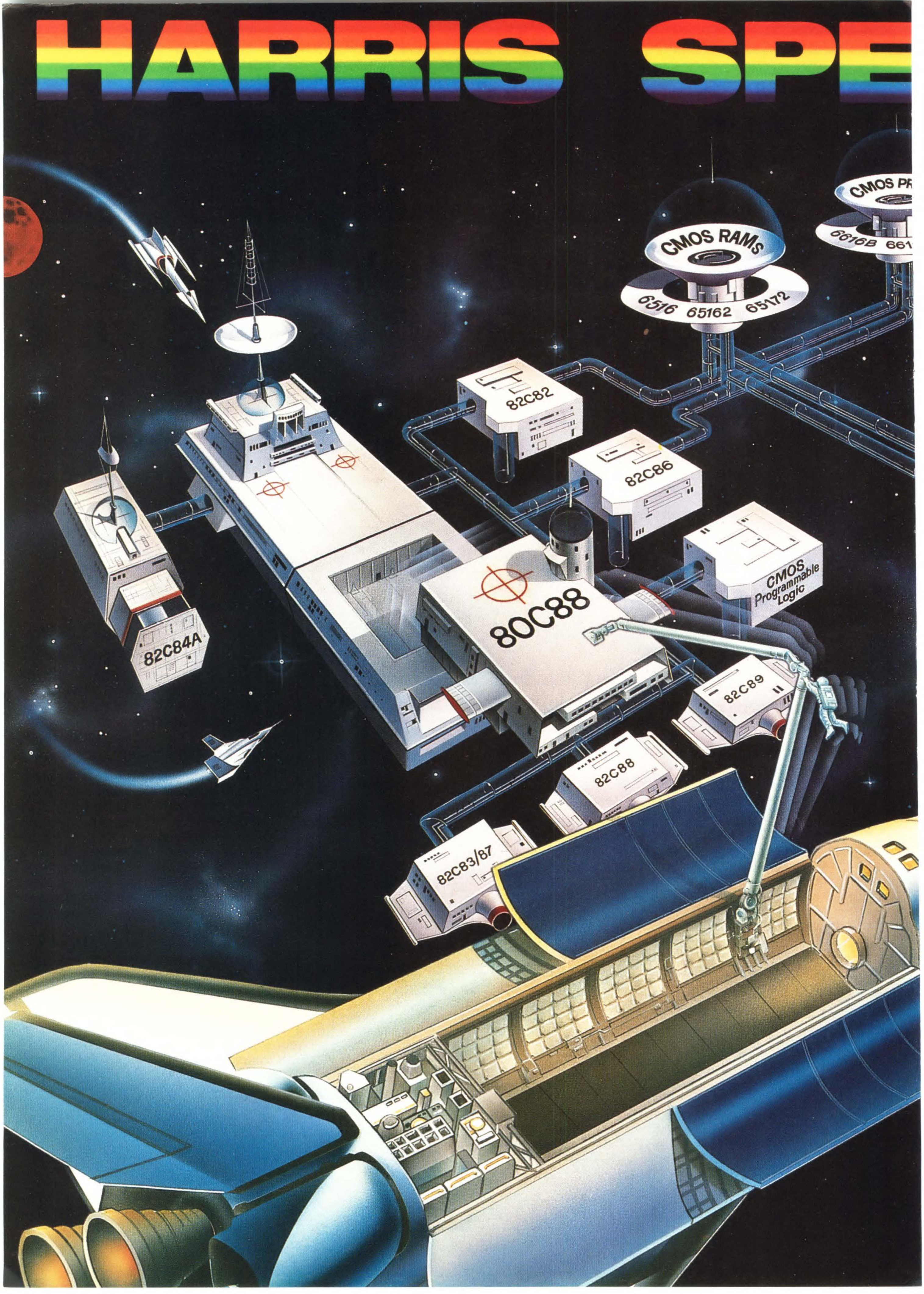
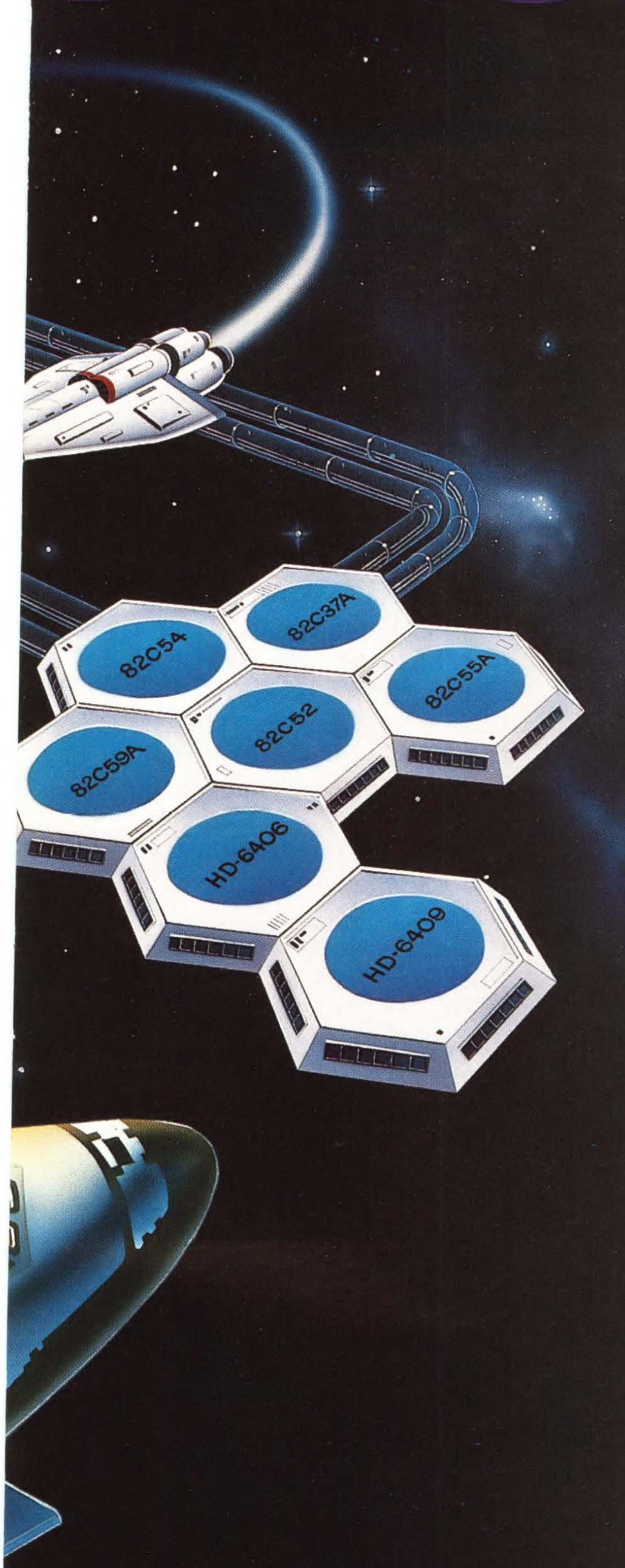
CIRCLE 236


HARRIS SPE
CMOS RAMs
6516 65162 65172
CMOS PR
6616B 661
82C82
82C86
CMOS Programmable Logic
80C88
82C84A
82C89
82C88
82C83/87

CTRUM




# Introducing the Harris 80C88.

## New CMOS Microprocessor gives 100% output with 10% power input.

Get the new Harris 80C88 8/16-bit CMOS CPU into your system. It's fully compatible with your present NMOS 8088 designs, yet consumes only 10% of the power. And the 80C88 16-bit architecture interfaces with memory and I/O via an 8-bit bus, making system design simple and efficient.

The 80C88 is a cool customer. It needs no heat sinks or cooling fans. And its completely static design gives you the freedom to run at a full 5 MHz or at reduced speed to conserve power.

You can even stop the clock to the 80C88 and put the system into a minimum-power standby mode.

There's no need to rework hardware or software. The new Harris 80C88 can execute programs designed for 8088, 8086 and 80C86 systems without any changes. Its industry-standard operation allows simple system upgrades, using your existing NMOS 8088 design and new Harris 80C86 peripherals.

Minimum and maximum operation modes let you configure your system to achieve the highest possible performance level. Over commercial, industrial and military temperature ranges. Guaranteed.

For out-of-this-world performance, get the new Harris 80C88 CMOS $\mu$P into your system—data processing, robotics, industrial controls, portable computers, telecommunications, harsh environment or military applications. It's the high-powered, low-energy successor to NMOS 8088 design. From Harris, of course.

**For more information, contact: Harris Semiconductor Digital Products Division, P.O. Box 883, MS 53-035, Melbourne, Florida 32902-0883.**

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**For your information, our name is Harris.**

**HARRIS**

CIRCLE 237

# System slashes the cost of computer-based calibration to $11,495

A computer-based calibration system is the first to cut the cost of high-resolution calibration by relying on automatic software control coupled with digitally controlled instrumentation. Developed by Shepherd Scientific, the Model 7000 precision calibration system delivers the performance of systems costing $30,000 to $40,000 for only $11,495, using the bus to calibrate instrumentation for dc and ac voltage and current and for resistance values.

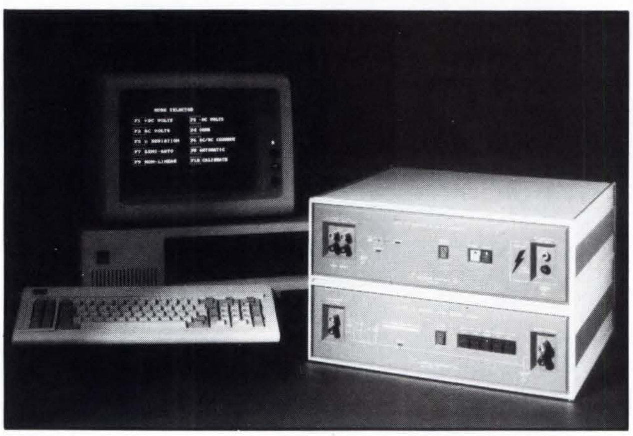
An easily used interactive software package, the Automatic Application Program, sets up the system calibration procedure during a dialogue with the user. It then executes the calibration sequences, prompting the technician when necessary. Semiautomatic or manual modes are also provided.

**Ray Weiss**

The 7000 contains an HP 85 computer. The HP 85 drives the ac-dc voltage and resistance calibrator (the Model 770), which drives a precision ac-dc current source (the Model 120).

The measurement components and software may be purchased separately and used with other popular microcomputers, including the IBM PC, the Compaq, the Apple IIe, and the HP 200.

The voltage and resistance calibrator has a general resolution of 1 ppm of the specified range. In the dc voltage range of 1.2 to 12 V, the voltage and resistance calibrator's accuracy will be held to 6 ppm (+40 μV) for 30 days; to 8 ppm (+40 μV) for 90 days, and to 10 ppm (+50 μV) for a year. The ac voltage in the same range will hold to 0.005% (+1 mV) at 0.001 Hz, to 0.02% (+20 mV) at 10 kHz, and to 0.15% (+20 mV) at 100 kHz.



The frequency resolution is 0.1% with an accuracy to within 0.01%. Resistance range settings run from 120 Ω to 1200 MΩ with currents of 100 mA to 10 nA, respectively, and accuracy to within 30 ppm to 0.5%.

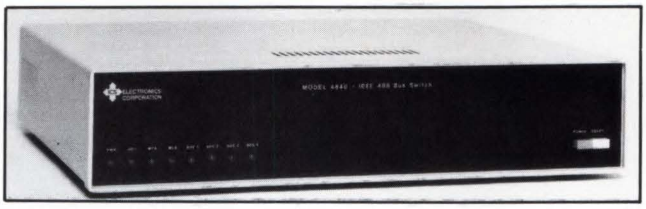
The current source has full-scale ranges in decade increments of 2 mA to 20 A with accuracies to within 0.005% (+100 nA) to 0.02% (+1 mA) at dc and to within 0.08% (+200 nA) to 0.15% (+2 mA) at 10 kHz. The input voltage is specified from 0 to 20 V, with an input impedance of 1 MΩ.

Component prices are $5998 for the 770, $1495 for the 120, and $385 for the Automatic Application Program (IBM PC version). Delivery is in 30 days.

*Shepherd Scientific Inc., 7100 Convoy Court, San Diego, Calif. 92111; (619) 268-9696.*

**CIRCLE 304**

# Multiplexer expands IEEE-488 systems



Allowing system designers to go beyond the 15-instrument limit specified for the IEEE-488 bus, the 4840 bus multiplexer from ICS Electronics connects 56 devices. The multiplexer also enables a single device to be shared among several bus controllers.

In the switching mode, the 4840 permits a single bus controller to operate as many as four IEEE-488 buses, for a total of 56 instruments (the unit occupies one position on each bus). If more than 56 instruments is required, the multiplexer switches can be ganged together with an ICS 4830B bus isolator, but with a significant degradation in system speed.

In the multiplexing mode, the unit connects up to four bus controllers to one common resource, like an IC test system. Each controller can poll the multiplexer until it is not busy and then request connection to the common resource. In an emergency, the highest-priority controller can use an override command to demand connection to the common resource bus. Should the primary controller fail, the multiplexer has a watchdog timer that will automatically switch the common bus to a backup controller.

In either mode, the unit permits any device on its buses to request service on an as-needed basis, using a Service Request interrupt. Normally, a controller will have to query every device on the bus to determine which device generated the service request. The 4840, however, automatically identifies on which of the four buses the request occurred, which means that the controller needs to poll a maximum of only 14 devices.

To prevent the occurrence of ground loops between the multiplexer's four individual ports, each is optically isolated from the others and from the common port. The bus interface at each port meets IEEE-488-1978, and the 4840 is transparent to all IEEE-488 bus commands with the exception of Pass Control.

The 4840 is available now off the shelf for $1895 in single quantities.

*ICS Electronics Corp., 2185 Old Oakland Road, San Jose, Calif. 95131; (408) 263-4844.*

**Curtis Panasuk**

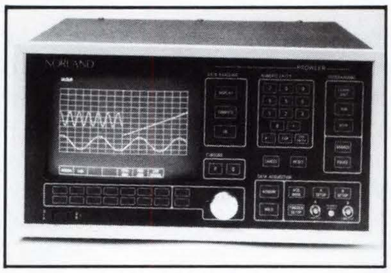
**CIRCLE 306**

**INSTRUMENTS**

# Digitizer samples at 50 MHz

Typically, digital oscilloscopes with extensive signal-processing capability cover a relatively low frequency range. Thanks to the N4009 digitizer module, the user who needs the signal-processing power of Norland's Prowler digital oscilloscope can now acquire and analyze data at sample rates of up to 50 MHz.

All of the scope's five main processing functions—mathematical, trigonometric, utility (such as rise-time and smoothing), statistical, and transfer (data memory manipulation)—work with the digitizer.



**When the N4009 digitizer module is installed in the Prowler digital oscilloscope, data can be acquired at rates to 50 MHz.**

Featuring a bandwidth of dc to 20 MHz, the module resolves 8 bits and is accurate to within ±1% up to 10 MHz. Up to 4096 data points/channel may be stored (or, optionally, 16,384), with the scope accommodating either one or two input channels.

A pretrigger delay lets the user designate the exact portion of a waveform to be captured prior to a trigger event. When combined with the unit's high sample rate, this feature allows fast transients to be analyzed easily.

The module is priced at $2500. Delivery is in 60 to 90 days after receipt of an order.

*Norland Corp., Norland Drive, Fort Atkinson, Wisc., 53538; (800) 558-0158.*

CIRCLE 303

## INSTRUMENTS

### Instrument tests AS-TTL components

The computer-controlled S-3225 logic tester offers a full range of capabilities for thorough Advanced Schottky TTL component testing. The system's hardware package comprises an integral equipment rack and a vertical test station that incorporates special pin-driver electronics optimized for high-speed TTL devices. The logic tester also meets the high-throughput requirements of production testing with interfaces for wafer probers and automatic device handlers.

Like other S-3200 series test systems, the S-3225 uses a PDP-11 computer as the system controller. Tektest III, a foreground/background-oriented test language, is used to facilitate testing, data reduction, and editing.

*Tektronix Inc., PO Box 1700, Beaverton, Ore. 97075; (503) 644-0161.*

**CIRCLE 335**

### Unit checks hard-disk read/write functions

For testing hard-disk drives used with personal computers, an emulator provides almost total repeatability of the read/write functions of both standard and sub-5¼-in. Winchester drives. The nondegradable calibration tool, which stores one track of data, accepts and returns up to 10,416 bytes of data during a read/write operation. After a seek test, track zero's data is returned until a write operation is performed.

The emulator includes programmable PROMs to reconfigure track and head capacities, index timing, data recording capacities, seek-complete timing, and power-on-to-ready timing.

*Applied Circuit Technology Inc., 2931 La Jolla St., Anaheim, Calif. 92806; (714) 632-9230. $1895; 60 days.*

**CIRCLE 336**

## INSTRUMENTS

### Benchtop computer serves incoming test

Designed to meet the specific needs of incoming test, the 2295 central station is a compact benchtop computer that operates with the SCAN (Semiconductor Component Analysis Network) software program. SCAN links the 173X series of IC test systems with the host 2295. Up to three VT-101 terminals and a total of four component testers can be connected to the 2295.

The computer is based on a PDP-11/23 processor with 250 kbytes of RAM. It is also configured with a 65-Mbyte Winchester disk drive, an 8-in. floppy disk, a serial printer, a VT-101 terminal, and cables to connect two component testers.

*GenRad Inc., 300 Baker Ave., Concord, Mass. 01742; (617) 890-4900. $24,900 (includes SCAN software); November.* **CIRCLE 337**

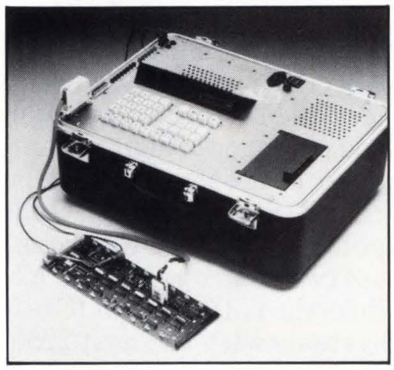
### Instrument tests microcomputer boards

For production testing of microcomputer boards, the M8 combines a ROM simulator, a logic waveform generator, and a digital IC tester into one modular package. The M8 master production tester checks 8-bit microprocessor-based boards, while S8 slave testers can be cascaded to test 16- and 32-bit products. It is designed to operate with a host computer or terminal via an RS-232-C interface.

Test procedures exercise the subject hardware (i.e., RAM, disk controllers, displays, and printers) and automatically display the test results. Up to 16 simulation logic waveforms can be generated, each independently menu-programmable. The M8 also performs pass/fail tests on digital components.

*Retrieval Service Base, 10315 SW Clydesdale Terrace, Beaverton, Ore. 97005; (503) 641-2564. $1595.* **CIRCLE 338**

## Tester diagnoses component-level faults



Capable of performing fault diagnosis at the component level, the AFD-48 portable in-circuit tester is aimed at reducing the time and cost involved in troubleshooting pc boards. Since the commands are in English, no programming knowledge is required. The tester compiles programs from the manufacturer's truth tables, which may be modified for special conditions.

The AFD-48 supplies all dc power and logic levels to the board under test, while components are checked via a cable-connected clip that is programmable for up to 40 pins. The pass or fail condition of each component is indicated both visually and audibly. An 80-character alphanumeric display isolates the faulty pins of a failed component or directs the user to the next IC. Each testing step takes only 12 μs; 2.04 ms for a 170-step pattern. Test programs are stored on standard cassette tapes.

*Roan Instruments Corp., 5655 Lindero Canyon Road, Suite 421, Westlake Village, Calif. 91362; (818) 889-8080. $22,500.* **CIRCLE 339**

# Digital interface chip works at 160 kbits/s for ISDN stystems

A network interface chip provides a full-duplex data communications link over a twisted-wire pair at rates of up to 160 kbits/s. Dubbed the MT8972 digital network interface circuit, the device is compatible with the recommended specifications of the CCITT's proposed Integrated Services Digital Network (ISDN) standard and achieves its high data rate by the first on-chip application of adaptive echo cancellation.

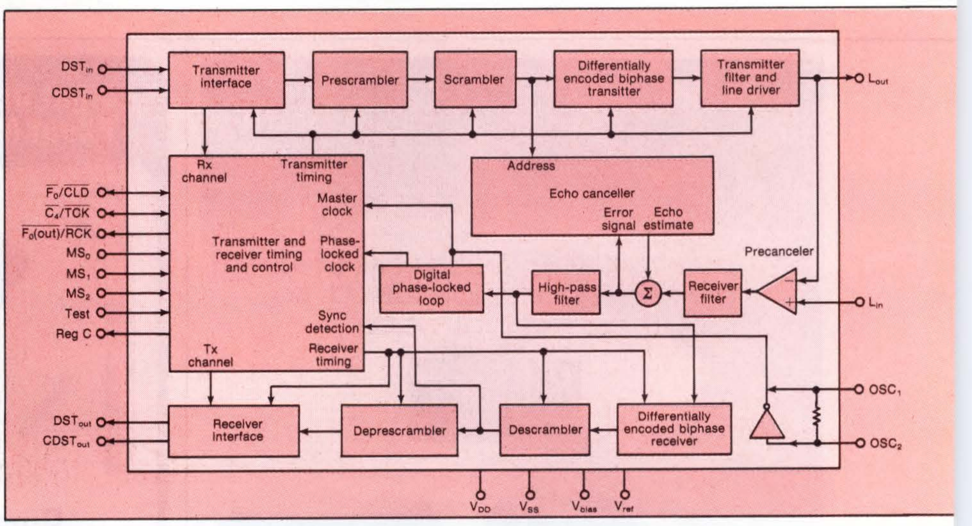
Developed jointly by Mitel and EB Communications (Oslo, Norway), the circuit employs differential biphase encoding and can transmit data up to 4 km at the 160-kbit/s speed and up to 5 km if the data rate is cut in half.

Fabricated in CMOS to keep the power consumption low—typically just 10 mA with a 5-V supply—the chip can be used for mixed data and voice transmission, digital PBXs, and even as a low-cost 80- or 160-kbit/s modem.

Also, the chip includes Mitel's proprietary Serial-Telecom bus (ST-bus), a two-wire interface that the company uses to tie various chips together in a chip-to-chip network without consuming a large number of package pins (ELECTRONIC DESIGN, Oct. 4, p. 46). It thus provides a bidirectional interface between the ST-bus and a full-duplex line that operates at either 80 or 160 kbits/s.

There are three serial ports on the chip—one for the ST-bus interface; another that accepts control signals and data; and a third to handle the full-duplex line, which contains the two B and single D channels as defined by the ISDN specifications. Data on the line consists of the combination of signals from both of the other ports.

The ports' actual data rate is 72 or 144 kbits/s, as recommended by the CCITT defini-




**Serving as the digital interface for systems conforming to the proposed Integrated Services Digital Network standard, the MT8972 chip includes adaptive echo cancellation to insure error-free communications.**

Dave Bursky

tion of the ISDN U-bus. The remainder of the bandwidth is occupied by various overhead signals required by the system.

Three Mode Select pins are used to determine one of eight modes, which include master or slave operation, parallel or serial busing, and modem operation. For timing, the chip relies on an external 10.24-MHz crystal for the internal oscillator. The oscillator frequency is then divided down to obtain the 2.048-MHz timing needed for the ST-bus and other serial ports.

The devices come in a 22-pin package. Initially, however, it will be available only in the form of an evaluation kit consisting of two printed circuit boards and documentation. The kit will be shipped starting in January, at a cost of $750 (U.S.).

*Mitel Corp., Kanata, Ont. Canada K2K 1X5; (613) 592-2122.*

**CIRCLE 318**

## X.25 multiport PAD supports SNA clusters

The PDN 5220, a multiport packet assembler/disassembler (PAD), acts as a gateway between SNA users and packet-switching networks that have interfaces complying with the CCITT X.25 standard. The PDN 5220 provides transparent communication between the network's remote SNA clusters and SNA host processors.

In addition to automatic call-setup facilities, the 5220 supports standard error-recovery procedures for each communications protocol (SDLC, BSC, and Async). The unit is available with two, four, six, or eight ports. The basic two-port version supports one SNA cluster and a single virtual circuit. A four-port configuration is quantity priced at $6500.

*Paradyne Corp., 8550 Ulmerton Road, Largo, Fla. 33540; (813) 530-2000.*

**CIRCLE 341**

## COMMUNICATIONS

### Millimeter detectors work down to −68 dBm

Four series of millimeter-wave detectors—available in nine bands ranging from 18 to 220 GHz—offer good tangential sensitivity for use in many applications. For example, fixed tuned units have a −55-dBm sensitivity at 35 GHz. Biased-type detectors have a sensitivity of −68 dBm at the same frequency.

The 971 and 925D series of self-biased detectors operate over the full waveguide band without tuning. The 973 series provides a flat, self-biased response with a VSWR ranging from 1.6:1 to 2:1 over full waveguide bands up to 60 GHz. Its output is typically 200 mV/mW at 35 GHz. The 965D series offers the highest tangential sensitivity—from −48 to −68 dBm—and is supplied with a battery bias supply.

*Alpha Industries Inc., 20 Sylvan Road, Woburn, Mass. 01801; (617) 935-5150.*

**CIRCLE 342**

### Security device needs no programming

Unlike conventional computer security devices, a random data-encryption system relies on hardware circuitry design rather than software programming to scramble data transmissions. The self-contained device, called Arbiter, requires no programs, key locks, passwords, magnetic cards, or other accessories.

With one Arbiter unit connected to the host computer and another connected to a remote terminal, real-time data is automatically transmitted in an unpredictable pattern of ASCII symbols. No two transmissions are ever alike.

*Computer Security Systems Inc., 1 Huntington Quad, Suite 1C07, Melville, N.Y. 11747; (516) 752-7790.*

**CIRCLE 343**

## COMMUNICATIONS

### Ethernet available for Unix supermicro

Intended for use with the Unix-based Samson supermicrocomputer, a local area network by the same name features front-end processing and comes with the Transmission Control Protocol/Internet Protocol (TCP/IP) package. Samson's front-end Ethernet processing offloads the system CPU of transport, network, and data-link protocols. It allows a variety of protocol architectures to be used and combined and, by reducing the workload of the CPU, maintains performance even during periods of heavy network activity. The Samson LAN meets the 10-Mbit/s transfer rate of version 1.0 of the Ethernet specification with 128 kbytes of buffer RAM.

*SGS Semiconductor Corp., Systems Division, 1000 E. Bell Road, Phoenix, Ariz. 85022; (602) 867-6241. Less than $200/user.* **CIRCLE 344**

### 1200-baud modem optimizes data transfers

To improve the efficiency of a data transfer session, a 1200-baud modem features automatic voice and data switching and is fully compatible with Bell 103, 113, and 212A dial-up modems. The InfoPhone modem is available in a plug-in card version (the Model IPI-1200) that fits inside the IBM PC or in an external stand-alone style (the Model IPX-1200), designed for any computer using a serial RS-232-C interface.

Both versions of the modem offer full-duplex 300/1200-baud communications, with automatic dialing and answering functions. The units are compatible with the Hayes Smartmodem commands and screen responses.

*Transend Corp., 2190 Paragon Drive, San Jose, Calif. 95131; (408) 946-7400. $370 (IPI-1200) and $445 (IPX-1200).* **CIRCLE 345**

**ANALOG**

# Clocked v-f converter chip delivers 0.5% accuracy, 0.1% nonlinearity at 1 MHz

A one-chip voltage-to-frequency converter derives its timing, and therefore its timing accuracy, from an external clock, rather than a one-shot multivibrator and its attendant external capacitor. This basic change from existing designs reduces initial gain errors of Burr-Brown's VFC100BG an order of magnitude to less than 0.5% of full scale. Changes in gain, in the past caused by changes in the now missing capacitor, is less than 50 ppm/°C (ELECTRONIC DESIGN, Sept. 6, p. 235).

Furthermore, nonlinearity is under 0.1% of full scale at 1 MHz and less than 0.02% at 100 kHz, as good as anything available.

The less precise AG and SG models give up very little to the BG. Gain error is under 1% and nonlinearity at 1 MHz is typically 0.025%. At 100 kHz, nonlinearity is guaranteed to be less than 0.025%. Offset voltage for the BG version is under 2 mV and rises to only 3 mV for the other models.

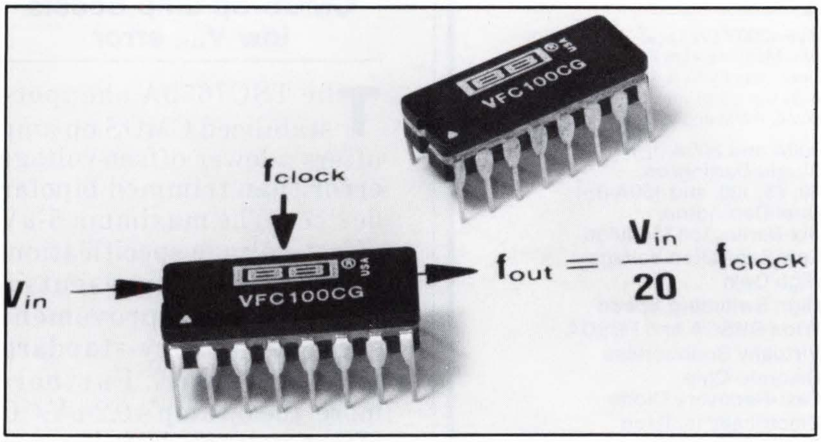
Both gain and offset errors can be reduced to zero with external potentiometers. Offset drift is 25 and 100 $\mu$V/°C for the premium and lower-grade units, respectively. Moreover, a simple autozero loop can keep the offset voltage at zero.

Like most v-f converter chips, the VFC100 can be connected to operate as a frequency-to-voltage converter. Accuracy and linearity are similar when operated in either configuration. Additionally, if the same clock is used for two units in a data link, gain errors virtually disappear. A laser-trimmed input resistor and a precision 5-V reference also contribute to gain accuracy.

The open-collector output handles 10 mA at 30 V and the unit draws a maximum of 15 mA from ±7.5- to ±18-V supplies. The AG and BG versions operate between −25° and +85°C and the SG between −55° and +125°C. All come in a 16-pin ceramic DIP. The VFC100 costs $8.85, $15.95, and $13.65 each in quantities of 100 units, for the AG, BG, and SG versions, respectively. Small quantities are available from stock.

*Burr-Brown Corp., PO Box 11400, Tucson, Ariz. 85734; Naresh Shah, (602) 746-1111.*

**CIRCLE 316**




**Frank Goodenough**

## Fast 12-bit DAC has internal reference

A 12-bit digital-to-analog converter has a buried zener voltage reference (10 V ±1% maximum) that has long-term stability and temperature-drift characteristics comparable to the best discrete or separate IC references. Designated the DAC1265A, the converter's reference temperature coefficient is ±8 ppm/°C. The device offers a 10% to 90% full-scale transition time of less than 35 ns and settles to within 1/2 LSB in 200 ns.

Applications for the converter include CRT displays, precision instruments, and data acquisition systems requiring throughput rates as high as 5 MHz for full range transitions.

*National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; (408) 721-5000. $12.95 (100 units).* **CIRCLE 346**

## CMOS op amp boasts low $V_{OS}$ error

The TSC7650A chopper-stabilized CMOS op amp offers a lower offset-voltage error than trimmed bipolar devices. The maximum 5-μV offset-voltage specification, for example, represents a fifteen-fold improvement over the industry-standard bipolar OPO7E. Furthermore, the op amp's 0.2-μV/°C offset-voltage drift is more than six times lower than the OPO7E.

The TSC7650A is pin-compatible with the ICL7650 device, but with a maximum supply current rating of 2.5 mA—a 30% reduction in maximum power dissipation when compared with the latter's 3.5-mA rating. A typical slew rate of 4.0 V/μs extends the TSC7650A's full power bandwidth by 60%.

*Teledyne Semiconductor, 1300 Terra Bella Ave., Mountain View, Calif. 94043; (415) 968-9241. $2.75 and $4.75 (100 units); six to eight weeks.*

**CIRCLE 347**

## Latchable multiplexers are μP-compatible

Two latchable multiplexers, the DG526 and DG527, include on-chip interface circuits that eliminate the need for external pull-up resistors, providing true compatibility with both TTL and CMOS devices. In addition, the ability to accept 300-ns write signals makes the devices fully compatible with microprocessors. Analog switching and data latching minimize the hardware needed to link the μP bus and analog system being controlled.

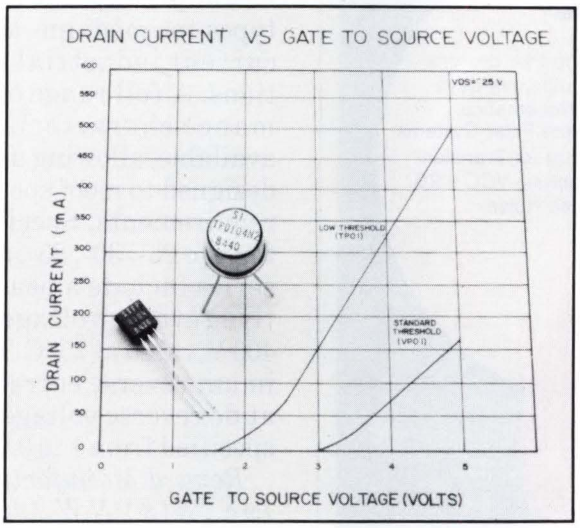
The DG526 performs 16-channel single-ended multiplexing and demultiplexing of ±15-V analog signals. The DG527 performs 8-channel differential multiplexing and demultiplexing of ±15-V common-mode and differential-mode signals.

*Siliconix Inc. 2201 Laurelwood Road, Santa Clara, Calif. 95054; (408) 988-8000. From $11.37 (100 units.)*

**CIRCLE 348**

**POWER**

# P-channel MOSFET drops threshold voltage to 2.4 V




A p-channel MOSFET boasts the lowest threshold voltage in the industry. From Supertex, the TP02L has a maximum threshold voltage of 2.4 V and an on-resistance of 2 Ω (measured at 10 V).

The DMOS device can drive continuous loads of 1.7 A when packaged in a metal TO-39 can and 0.7-A loads in a plastic TO-92 package; peak loads of 4.6 A can be driven in either package. The transistor switches voltages of up to 40 V with a switching speed of 20 ns.

Because of its low threshold voltage, it can be turned on with a low voltage. This capability is particularly important in systems where 5 V is the highest voltage available, since 5 V has not been enough to completely turn on existing p-channel MOSFETs.

To get around this problem, engineers have had to either use larger, more-expensive p-channel devices or build complex voltage boosters to increase the drive voltage. The TP02L can replace these larger MOSFETs and the booster circuits.

A sister part, the TP01L, is made from a smaller die, giving a higher switching speed of 10 ns but also yielding a slightly higher on-resistance of 4 Ω (measured at 10 V). Both devices are available from stock.

In quantities of 1000 units, the TP02L costs $1.72 each in a TO-39 can and $0.83 in the TO-92 package. In the same quantities, the TP01L costs $1.34 and $0.46, respectively.

*Supertex Inc., 1225 Bordeaux Drive, Sunnyvale, Calif. 94089; (408) 744-0100.*

**Curtis Panasuk**

**CIRCLE 310**

NEW PRODUCTS

**POWER**

## Rectifiers handle medium, high currents

An extensive line of silicon rectifier diodes comprise ½-in. press-fit and button types for medium- and high-current industrial applications. A full range of performance characteristics are available, allowing units to be designed to meet specific user requirements. Specifications for the 25-, 30-, 35-, and 50-A series include a peak repetitive reverse voltage of 50 to 400 V, rated at 25°C. The maximum reverse current, rated at dc reverse voltage, may be specified from 1 to 0.010 mA.

*Renard Manufacturing Co. Inc., 3131 NW 79th Ave., Miami, Fla. 33122; (800) 327-7244 or (305) 592-1500.*

**CIRCLE 349**

## Regulator IC sinks 10 A

Packaged in a standard 3-lead TO-3 package, the LT1038 adjustable voltage regulator supplies 10 A of output current over a 1.2- to 32-V output range. A current-limiting circuit allows the device to supply up to 23 A for 500 μs before current limiting, which makes it well suited for systems with large transient loads (such as solenoids).

The reference of the LT1038 is trimmed to ±0.8%; line and load regulation are 0.01% and 0.04%, respectively.

*Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, Calif. 95035; (408) 942-0810. $9.95 (100 units).*

**CIRCLE 350**

**POWER**

## SIP diode arrays take up little space

Replacing many standard DIP configurations in order to conserve pc board real estate, the DM3 series consists of a variety of diode arrays in single-in-line packages. The SIP arrays can be configured with silicon or germanium diodes to meet specific application requirements. The user may specify the number of diodes and the number of pins to be used in the array. One of the features of the DM3 series is that it can provide two arrays in one, with the common anode terminal of one and the common cathode terminal of the other at the same pin.

The product line is useful in a number of applications, including computer memories, telecommunications, industrial controllers, and clamping circuits.

*RPM Enterprises, 1583 E. Saint Gertrude Place, Santa Ana, Calif. 92705; (714) 556-8940. Stock to four weeks.*

**CIRCLE 351**

## Soft-recovery diode works at 6 kV

A soft-recovery rectifier diode has a crest working voltage of 6 kV and a repetitive peak reverse voltage of 7.5 kV. The average forward current of the BXY90G—the latest entry in an extensive range of glass-encapsulated high-voltage diodes—is 550 mA. With a reverse recovery time of 350 ns, the avalanche diode is suitable for application in high-frequency (20 kHz) converters for X-ray equipment and in other high-voltage equipment. The device is rated for operating temperatures of up to 165°C.

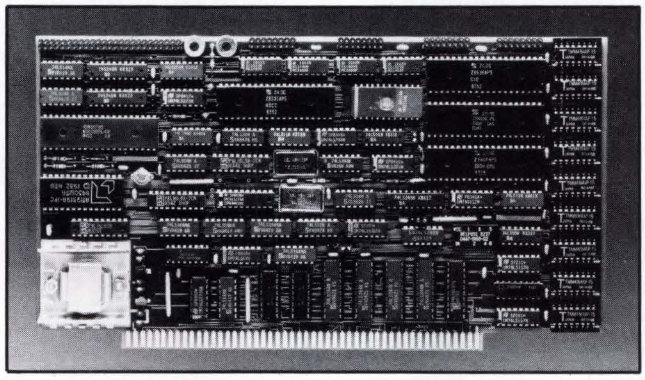
*Philips Elcoma, PO Box 523, 5600 AM Eindhoven, the Netherlands; (040) 757005; Telex: 51573.*

*Amperex Electronics Corp., 230 Duffy Ave., Hicksville, N.Y. 11802; (516) 931-6200.*

**CIRCLE 352**

**COMPUTER BOARDS**

# S-100 computer board doubles as file server



A complete S-100 computing system on one board gives the designer the flexibility of using it as a file server. Designed by Teletek, the Systemaster II is based on a Z80B (6-MHz) processor with no wait states and can also accept a Z80H (8 MHz) with one wait state.

The board runs under CP/M 3.0 as well as TurboDOS 1.4, developed by Software 2000 (Arroyo Grande, Calif.). The latter permits CP/M or PC-DOS application programs to run, with up to 16 people using the processor. It also is capable of multitasking.

A system master board running under TurboDOS, however, can directly support only two users, since it has only two serial ports. For each additional user, a sister board, the SBC 86/87, must be added onto the S-100 bus.

The Systemaster II can address up to 128 kbytes of RAM by using bank switching, and and a Western Digital WE-2797 controller allows the board to use 5¼- or 8-in. floppy-disk drives.

The board has two RS-232 ports and a 16-bit parallel port that can be used for general I/O or as a Centronics printer interface. A DMA circuit handles automatic transfers across the S-100 bus, and in January a daughter board will be available to interface the board with the SASI or the IEEE-488 bus.

Another board, the SBC 86/87, for use with the Systemaster II in multiprocessor applications, has an 8086 (5 or 8 MHz), an S-100 bus interface, up to 512 kbytes of RAM, a Centronics parallel port, and an optional 8087. Both boards contain a 2-kbyte FIFO register to allow faster transfers across the S-100 bus.

The Systemaster II is available now for $679.50 each and the SBC 86/87 for $837 in 100-unit lots. Delivery is from stock.

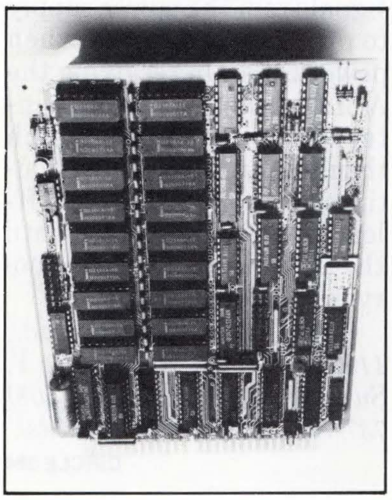
*Teletek Enterprise Inc., 4600 Pell Drive, Sacramento, Calif. 95838; (916) 920-4600.*

**Curtis Panasuk**

**CIRCLE 307**

## COMPUTER BOARDS

### Dynamic RAM board eliminates wait states

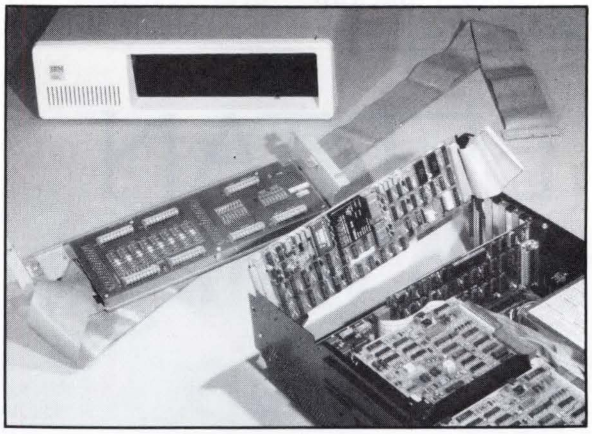


Designers of 8088- and 8085-based systems can eliminate software overhead caused by wait states during RAM refresh with the Model 7712 dynamic RAM card. Onboard circuitry enables completely transparent refresh of dynamic RAMs during push-button resets, extended wait periods, DMA transfers, and normal MPU operations. The card eliminates wait states during any read or write access and automatically initiates refresh during DMA operations.

The memory board is available in four densities: 64 or 128 kbytes (using 64k-by-1 chips) and 256 or 512 kbytes (using 256k-by-1 chips). A dual 4-bit decoder allows the 7712 to use the full 20-bit address from an 8088 CPU, or it can be latched to steer data to the appropriate 64k memory block during a 16-bit DMA address transfer.

*Pro-Log Corp., 2411 Garden Road, Monterey, Calif. 93940; (408) 372-4593. From $490 to $1750.* **CIRCLE 353**

# I/O boards serve PCs for only $1195



A family of boards offers the least expensive way to add test and measurement capabilities to personal computers—as little as $1195. The two boards introducing Burr-Brown's PCI-4000 family plug directly into IBM PC and PC XT and the Compaq personal computer expansion slots.

The PCI-4301-1 and the PCI-4301-2 analog-input boards contain 8 differential or 16 single-ended channels; a 12-bit a-d converter; and five jumper-selectable voltage ranges of 0 to 10, −2.5 to +2.5, −5 to +5, −10 to +10, and 0 to 5 V. A digital I/O system, organized as two bytes that are jumper-selectable as inputs or outputs, is also included on both boards.

The PCI-4301-2, though, has an additional two-channel analog output section with two independent 12-bit d-a converters and offers the same choice of output voltage ranges. It contains four event counters. Based on Intel's 8254 timer chip, the 16-bit counters have a maximum input frequency of 8 MHz and a minimum pulse width of 60 ns.

The PCI-4901-1 software diskette helps the user write application programs. For the simplest data acquisition operations, the diskette provides complete menu-driven commands.

Two termination panels of screw-terminal arrays, the PCI-4701-1 and PCI-4701-2, are available for the PCI-4301-1 and the PCI-4301-2, respectively.

The PCI-4301-1 costs $1195, the PCI-4301-2 $1495, and the PCI-4901-1 software diskette $425. The price of the PCI-4701-1 is $185, and the PCI-4701-2 costs $249. All products are available from stock.

*Burr-Brown Corp., PO Box 11400, Tucson, Ariz. 85734; (702) 746-1111.* **CIRCLE 313**

**Heather Bryce**

## COMPUTER BOARDS

### CMOS memory board works with iSBX bus

Enhancing the reliability of Intel single-board computers is a battery-backup memory module that is capable of storing up to 4096 bytes of data for five years. Designated the LS3032, the iSBX-compatible board utilizes CMOS memory devices that draw as little as 0.1 μA, allowing a single lithium cell to act as the standby power source.

The LS3032 uses the ACLO signal from the power supply to protect the memory when power fails. On receiving the ACLO signal, it sends an interrupt to the host, which then initiates power-fail routines. These routines can offload data for up to 4 ms until the LS3032 asserts the memory protection function.

*Computer Modules Inc., 1190 Miraloma Way, Suite Y, Sunnyvale, Calif. 94086; (408) 737-7727. $290 (10 to 24 units).*

**CIRCLE 354**

### Controllers display 1024 by 1024 pixels

Two new members of the Ultra-Res family of graphics controllers offer high-resolution graphics for IBM PC and PC-compatible computers. Designated the 4-79 and the 4-111, the boards have a programmable resolution of up to 1024 by 1024 interlaced pixels, chosen from a memory of 1 or 4 million pixels, respectively.

Based on the NEC7220 controller chip, the boards occupy a single slot in the host computer. Vectors, circles, and arcs are drawn at rates of up to 1 million pixels/s. Standard features include light-pen input, windowing, scrolling, zooming, and panning. The controllers have 9-pin D connectors for TTL direct drive, or they can generate an analog video signal.

*CSD Inc., PO Box 253, Sudbury, Mass. 01776; (617) 443-2750. $995 (4-79) and $2000 (4-111).*

**CIRCLE 355**

## COMPUTER BOARDS

### Disk controller mixes EDSI/SCSI

The Champion disk controller links 5¼-in. Winchester disk drives incorporating the Extended Small Disk Interface (ESDI) with the versatile SCSI bus. Up to two ESDI disk drives can be integrated with any computer through the use of an SCSI-based host adapter at the CPU. The Champion is a single 5.75-by-8-in. pc board, which can be mounted on the disk drive or packaged within the subsystem chassis. The board employs a MOS microprocessor and CMOS custom VLSI buffer controller and disk formatter chips. A 14-kbyte data buffer, automatic error correction, and remapping are among the Champion's standard features.

*Emulex Corp., 3545 Harbor Blvd., PO Box 6725, Costa Mesa, Calif. 92626; (714) 662-5600. $395; 30 days.*

**CIRCLE 356**

### Disk controller has expandable cache

Of particular interest to those running multi-user operating systems, the PM-3010 disk controller offers a 128-kbyte cache RAM that can be expanded to up to 16 Mbytes. Unlike other controllers, it uses a true sector caching algorithm as opposed to a track cache. Up to 128,000 sectors can be individually stored in the cache memory, with access times not exceeding 400 μs.

Up to four ST506-, SA1000-, or SMD-compatible Winchester-disk drives, plus four floppy-disk drives, can be controlled by a single 5¼-in. form factor board. The PM-3010 uses an SCSI link for communicating with the host computer at an average data rate of 1 Mbyte/s.

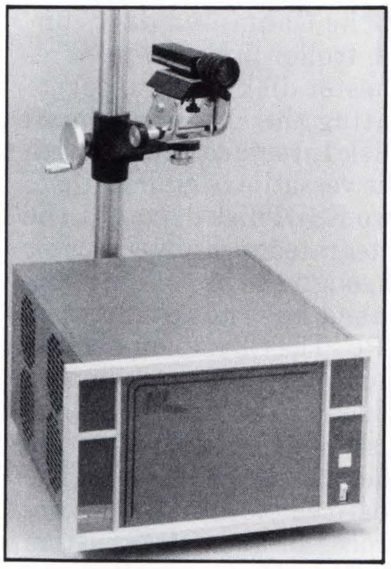
*Distributed Processing Technology, 132 Candace Drive, Maitland, Fla. 32751; (305) 830-5522. $740 in OEM quantities; first quarter of 1985.*

**CIRCLE 357**

## FACTORY AUTOMATION

# Vision system eliminates programming

Treating vision sensing as a measurement function much like those of temperature and voltage, Pattern Processing Technologies' APP 90 vision system includes all necessary programming. All the user need do is manually train the instrument by means of a "show and label" procedure that sets parameter levels.



The system then performs the measurement and analysis automatically. The result is a much simpler setup procedure and no cumbersome programming.

The APP 90 makes visual measurements over 64 levels of gray. It can inspect a part in as little as 20 ms.

The vision system accommodates up to four cameras with a resolution of 320 by 484 pixels, up to 128 independent images, and up to 256 kbytes of memory. It can handle up to 256 user-defined randomly spaced windows.

The system is priced at approximately $29,000 and is available within 60 to 90 days.

*Pattern Processing Technologies Inc., 511 11th Ave. S., Minneapolis, Minn. 55415; Paul Kraska, (612) 339-8488.*

**CIRCLE 314**

## Menus ease job of data acquisition

Operating in an IBM PC or Apple IIe computer, a plug-in data acquisition and control module accepts up to 16 inputs from temperature, pressure, strain, voltage, and current sensors without programming. Through simple menus the system logs or displays data (including minimum, maximum, average, and difference) and triggers alarms at desired set points. Ranges from 50 mV to 10 V are automatically selected, as are linearization and cold-junction compensation.

Dubbed the Analog Connection, the board offers 8 or 16 digital I/O lines. A resolution of 0.4% to 0.006% (8 to 14 bits) is selected in software.

*Strawberry Tree Computers, 949 Cascade Drive, Sunnyvale, Calif. 94087; (408) 736-3083. $889 (IBM PC)and $695 (Apple IIe); stock.*

**CIRCLE 358**

## Low-cost robot handles small parts

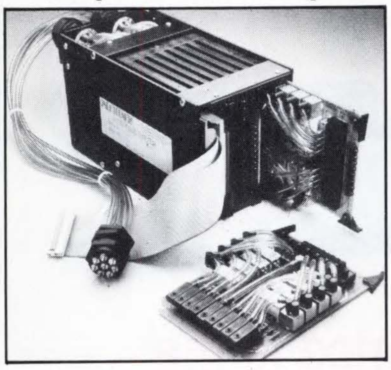
Priced under $10,000, the NND 88-5 articulating robot offers small parts handling capability usually found in equipment costing up to four times as much. Five dc servomotors with digital optical encoders ensure repeatability to within ±0.004 in. Movements with speeds of up to 20 in./s can be made along the robot's five axes.

The assembly robot has a six-program storage capacity, each with 78 set points. An RS-232-C interface connects the unit with a host computer for unlimited program capacity, as well as for loading, editing, and saving. The rugged cast-aluminum robot is just 7½ in. high by 7 in. wide by 11 in. long and weighs only 11 lb.

*Advanced Technical Products Inc., 955 W. River Pkwy., Grand Island, N.Y. 14072; (716) 773-0972.*

**CIRCLE 359**

## Electronic interface has pneumatic output



The SBX interface system accepts a digital signal from a microprocessor and converts it into a pneumatic output for a wide variety of industrial and process control equipment. The unit consists of a group of printed circuit boards that are plugged into a rack assembly. A typical 19-in. rack contains up to 10 modules, each having eight pneumatic I/O functions, for a total of 80 functions per rack assembly. The completely packaged, ready-to-install system typically requires one-tenth the space of conventional interfacing methods.

SBX interface systems are plug-compatible with most programmable controllers and accept TTL and 12 or 24-V dc inputs. Board modules in the series are completely interchangeable for maximum flexibility.

*Parker Hannifin Corp., 2 Lomar Park, East Pepperell, Mass. 01437; (800) 225-5008 or (617) 433-2721.*

**CIRCLE 360**

## Placement system handles surface devices

The MCT 6000 is a sequential-type placement system that populates printed circuit boards with surface-mounted components. The system combines a fully distributed microprocessor-based controller and a closed-loop servo drive system with automatic board and component handling functions.

Capable of operating within a placement area of up to 12 by 18 in., the MCT 6000 has a production rate of 6000 placements/hour. The system accommodates a wide variety and any mix of feeder and component types. A single placement head handles components ranging in size from 0.040 by 0.040 in. up to 1.2 by 1.2 in. Presentation media available for the MCT 6000 include carrier tapes (8, 12, 16, 24, and 32 mm), linear vibratory magazines, and several IC feeders.

*Micro Component Technology Inc., 3850 N. Victoria St., St. Paul, Minn. 55164; (612) 482-5100.*

**CIRCLE 361**

## FACTORY AUTOMATION

### Controller expands to 120 I/O channels

Both low cost and a modular design make the Mini-V-12 programmable controller suitable for small applications. With the Mini-V-12, the user may configure a simple 16-I/O system and expand it to a full 120 I/O channels as needed.

The basic system consists of a control module, a power module, and a programmer, with I/O modules added to suit the application. The programmer has an LED display and a touch-pad keyboard, as well as built-in self-diagnostics.

The miniature controller, which mounts on a standard DIN rail, features a 944-word programming capacity. In addition, 352 internal relays and 32 counters and timers permit flexible program design using seven simple instruction types.

*Veeder-Root Co., 70 Sargeant St., Hartford, Conn. 06102; (203) 527-7201.*

**CIRCLE 362**



### Temperature controller cuts start-up time

A temperature controller reduces start-up time by automatically calculating proportional band, rate, and reset values prior to the completion of warm-up. Since the unit sets all parameters before the process reaches set-point, temperature cycling and over-/undershoot are eliminated.

The Series 6050's parameter ranges include proportional band values from 0.5% to 100%, rate values from 5 to 240 seconds, and reset values from 0.5 to 24 minutes to control a broad variety of processes. It also provides drift-free temperature control (0° to 1400°F) that is accurate to within ±0.2% of span.

*Athena Controls Inc., 5145 Campus Drive, Plymouth Meeting, Pa. 19462; (215) 828-2490.* **CIRCLE 363**

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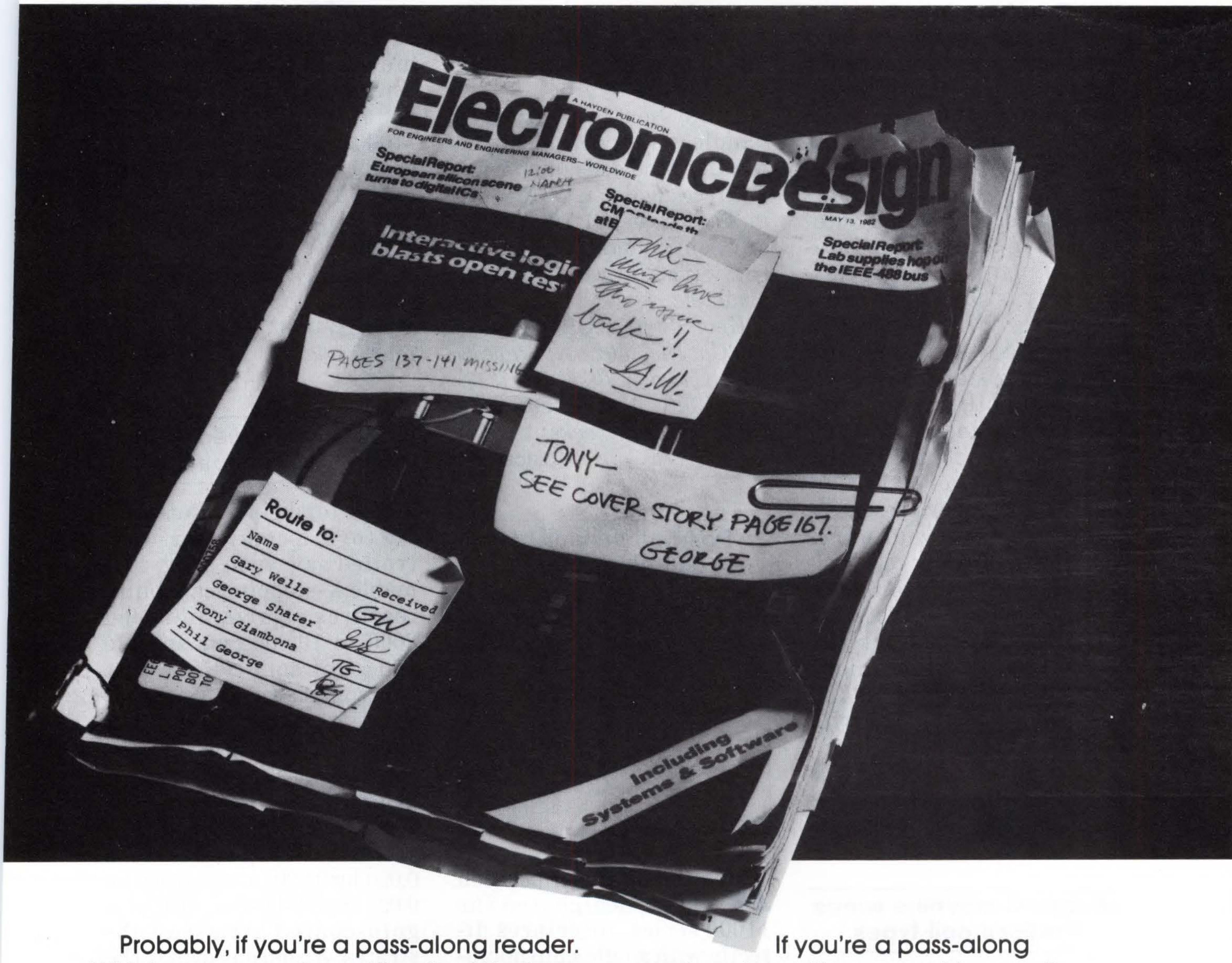


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## FACTORY AUTOMATION

### Graphics interface links work cells

Sealed in a NEMA-12 enclosure and air-conditioned to protect it from the factory floor, the CIM Factory Manager is the graphic link between islands of automation in a computer-integrated manufacturing network. It is supplied with a 30-Mbyte Winchester disk drive and a 5¼-in. floppy-disk drive. The system also has full Unix capabilities and supports all Cadlinc software.

As part of a flexible manufacturing network, the CIM Factory Manager presents a graphic preview of parts running in the work cell. It allows the operator to review and update the status of work at his station; check the status of the next job, along with all of its tooling and fixtures; and communicate with other work cells on the floor.

*Cadlinc Inc., 700 Nicholas Blvd., Elk Grove, Ill. 60007; (312) 228-7300.* **CIRCLE 364**

### μP-based machine winds limitless coil types

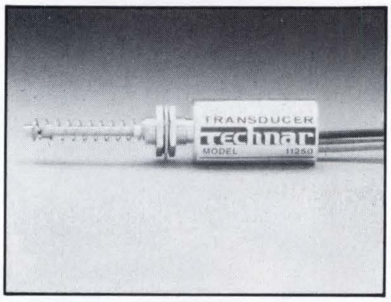
A microprocessor-controlled coil winder, the Model 7000-MPC winds virtually all coil types, including special types such as tapered or pyramid bobbin coils, variable pitch windings, and dual lateral windings. It can also handle applications where a preset number of layers and turns/layer decrease, giving a valley opposite the bobbin flange to secure finish leads. The counter-control system can automate and program many complex coil winding functions in any combination or sequence.

The system is designed to handle wire sizes of 24 to 50 AWG, round coils up to 9 in., and rectangular coils up to 4½ in. The maximum traverse for any continuous winding is 6 in., with 20 in. optionally available.

*Geo. Stevens Manufacturing Co. Inc., 6022 N. Stevens Ave., Chicago, Ill. 60646; (312) 588-1300. Approximately $32,000; 8 to 10 weeks.*

**CIRCLE 365**

### Position sensor has digital interface




An absolute linear position sensor, designated the 11000 series, interfaces directly with single-chip microcomputers without the need for an a-d converter. The transducer can be interrogated by event counters, and both the transducer and the microcomputer operate from the same supply voltage. Position measurement within a variety of media is possible since the sensing elements are inductively coupled through the sealed wall of the transducer body.

The device offers a sensing range of 3 to 25 mm (0.12 to 1 in.), depending upon the model. It also has a nonlinearity of ±0.5%. Supply voltage requirements for the 11000 series are not critical; supply current drain at 5 V dc is 5 mA. The device operates in temperatures ranging from −40° to +125°C.

*Technar Inc., 205 N. 2nd Ave., Arcadia, Calif. 91006; (818) 447-1187. $65 (100 units); four weeks.* **CIRCLE 366**

### Variable-speed saw dices chip capacitors

Used for dicing chip capacitors, a computer-controlled saw with programmable X-stepping capability features a variable-speed 3000-to-10,000-rpm spindle and a hydraulic cylinder that controls material feeding at rates from 0 to 8 in./s. The fully automatic Accu-Cut Model 5255 is capable of stepping over a 6-in. range in 0.0005-in. increments. The saw dices chip capacitors 0.020 by 0.020 in. and 0.025 by 0.025 from 2-by-2-by-0.025-in. gold-coated alumina substrates. Aremco provides the necessary materials for performing the dicing procedure, including temporary adhesives, ceramic blocks for mounting the substrates, and dicing wheels. Both resin-bonded and metal-bonded diamond blades are available.

*Aremco Products Inc., PO Box 429, Ossining, N.Y. 10562; (914) 762-0685. Approximately $16,000 (depending on accessories); 10 weeks.*

**CIRCLE 367**

## COMPONENTS

### EL membrane switches illuminate keyboards

Using a unique process to maximize the contrast enhancement of the graphic overlay, a family of screen-printed electroluminescent backlit membrane switches is a cost-effective alternative to keyboard illumination. In contrast to the pinpoint light of LEDs and incandescent bulbs, the panels offer full even illumination—from 5 to 60 fL. Moreover, they can be designed for selective lighting of individual switches, groups of switches, or for border illumination.

While the electroluminescent panels perform best with a dc-to-ac driver, they can also run on line current. Use of the panels permits flexibility in keyboard design, including tactile and nontactile configurations; environmental sealing; and ESD, EMI, and RFI shielding.

*Dorman Bogdonoff Corp., Willow Pond, Andover, Mass. 01810; (617) 470-0001.*

**CIRCLE 368**

### Card-edge connector is IBM PC-compatible

The latest addition to the 7000 series of card-edge connectors, the VL7000-62 is designed to meet the requirements of the IBM bus system. The connector—which has 31 contact pairs on a grid spacing of 0.100 by 0.200 in.—comes with full or semibellows-type contacts and is available in a wide range of termination styles and plating options. Between-contact polarization prevents pc board mismating, and insulator standoffs permit easy flux removal in solder applications. The connector is rated for 3 A, with a maximum contact resistance of 60 mV at rated current.

*Midland-Ross Corp., 205 Gateway Place, Suite 300, San Jose, Calif. 95110; (408) 993-8000. $1.77 (1000 units); stock to four weeks.*

**CIRCLE 369**

### Surface-mount LEDs come in SOT-23 housing

One of the first surface-mounted LED lamps to come in a SOT-23 clear plastic package can be used in touch keyboards as an optical failure indicator on a printed circuit board. The rectangular dimensions of the 1-mm-thick SOT-23 housing are a mere 1.3 by 3 mm. In addition to conserving pc board real estate, the tiny lamps afford a wide viewing angle of 140°.

The subminiature series, designated the LDX23XO, offers a choice of three single LED parts—high-efficiency red (LDH2310), yellow (LDY2320), and green (LDG2330)—and a double-diode red/green (LDR2340). In quantities up to 5000, the latter unit costs $0.47, while the former devices are priced at $0.45. Delivery is within eight weeks.

*Siemens Components Inc., Optoelectronics Division, 19000 Homestead Road, Cupertino, Calif. 95014; (408) 257-7910.*

**CIRCLE 370**

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# PRODUCT NEWS

## Single and dual op amps need single supply

In addition to the MC34074 single-supply op amp, **Motorola Semiconductor Products Inc. (Phoenix, Ariz.)** is offering similar devices in single and dual versions—the MC34071 and the MC34072, respectively. The op amps, which operate from a supply of 3 to 44 V, have a full power bandwidth that is typically 200 kHz for a 20-V swing. At that speed, they have a total harmonic distortion of 5%. The 13-V/µs slew rate, as well as the bandwidth, is an improvement over other single-supply op amps. The average temperature coefficient of offset is 10 µV/°C, and the common-mode rejection ratio is typically 97 dB. The prices for the devices in plastic, specified for the commercial temperature range, are $0.45 for the single op amp and $0.65 for the dual op amp (in quantities of 100).

**CIRCLE 371**

## Mini relays switch 5 and 10 kV

Especially suited for application in digital antenna couplers, laser systems, and numerous industrial high-voltage switching systems is a family of ceramic vacuum relays recently announced by **Kilovac Corp. (Santa Barbara, Calif.)**. Available in SPST, SPDT, fail-safe, and latching configurations, the K40 series of relays includes both 5-kV and 10-kV rated models with current-carrying capabilities of 15 A at dc and 3.8 at 32 MHz. The devices also offer switching times as fast as 4 ms. Weighing only 1 oz, the miniature relays are offered in a low-cost commercial version and a military version that conforms to MIL-R-83725B specifications.

**CIRCLE 372**

## 8052 employs on-chip Basic interpreter

**Intel Corp. (Santa Clara, Calif.)** has released a software-on-silicon version of its 8052 microcontroller, which features a complete Basic interpreter stored on-chip in 8 kbytes of ROM. Furthermore, the interpreter is 2.5 to 10 times faster than Tiny Basic, available in chips currently on the market. Designated the MCS Basic-52, the package offers full 8-digit floating-point arithmetic, a built-in capability to program an EPROM and EEPROM, and a user-accessible function library, as well as the 8052AH. Especially useful in time-critical industrial control applications, the MCS Basic-52 enables nonsoftware-oriented users to program the chip without knowing its architecture.

**CIRCLE 373**

## MLC capacitors offer negative TC

SFE Technologies' Electric Division (San Fernando, Calif.) is producing highly stable multilayer ceramic capacitors with negative temperature coefficients. All of the specifications for the N080 and N150—including environmental, electrical, and packaging—are identical to those of the standard NPO series with the exception of the negative temperature coefficients, $-80 \pm 30$ and $-150 \pm 30$ ppm/°C, respectively. Typical specifications for the two capacitor lines include an operating temperature range of $-55°$ to $+125°$C; voltage ratings of 25, 50, 100, 200, and 500 V; and tolerances of 1%, 2%, 5%, 10%, and 20%. Chips and radial- or axial-leaded devices are available in bulk or industry-standard tape-and-reel packages. **CIRCLE 374**

## 256k DRAMs come in three configurations

Tailored to meet the specific application needs of designers in various fields, **NEC Electronics Inc. (Mountain View, Calif.)** is bringing to market 256k dynamic RAMs in three different configurations. The products include: the uPD41256, a 256k-by-1 page-mode device now in production; the uPD41257, a 256k-by-1 nibble-mode part that is available for sampling in a ceramic package; and the uPD41254, a 64k-by-4 chip that is also being sampled in a ceramic package. The 64k-by-4 part is especially suited for terminals, personal computers, and video applications, while the 256k-by-1 devices are designed for mainframe computers and telecommunications. All three dynamic RAMs offer access times of 150 and 200 ns and are implemented in NMOS with double poly interconnects. In quantities of 100, the 41256, 41257, and 41254 are priced at $27.50, $30, and $33, respectively. **CIRCLE 375**

## SO package increases board density

Nearly doubling the number of chips that can be placed on a printed circuit board is a small-outline (SO) dual-in-line packaging option from **Gould AMI Semiconductors (Santa Clara, Calif.)**, which is available for its standard products, as well as its custom and semicustom designs. A 28-pin SO IC is a maximum 0.419 in. wide (including the gull-wing leads), compared with the 0.610-in. maximum width of the DIP. What's more, the 1.470-in.-long DIP is more than twice the length of the SO package, which is a mere 0.712 in. long. The leads of the SO IC are 50 mils apart, as opposed to the usual 100 mils. Devices can be surface-mounted using automatic pick-and-place equipment. **CIRCLE 376**



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**PRODUCT NEWS**

## Shaft cutter is easier to use

Redesigned from the ground up by **Turnex International (Newport Beach, Calif.)**, the Model 85 shaft cutter is not only 18% faster to use, but it requires a lower cutting force as well. Moreover, the tool can cut shorter device shafts—to a minimum of $1/4$ in. The guillotine-type cutting tool has seven holes for accommodating shaft dimensions of $1/4$, $1/8$, and $1/16$ in., as well as 6, 5, 4, 3, and 2 mm. The Model 85 is priced at $140 and is delivered from stock. **CIRCLE 377**

## Memory testers get additional tape drive

A second tape drive for the J386A and J386A-8 memory test systems—from the **Semiconductor Test Division of Teradyne Inc. (Woodland Hills, Calif.)**—allows program generation and compiling to be done on the test system itself rather than on an off-line controller. The second drive also enables the user to employ tape editing, compiling, and file-management functions. The unit is available as an option or as a field-upgrade package. Delivery of the latter will begin late this year; delivery of the drive as an option on a new system will begin in the first quarter of 1985. **CIRCLE 378**

## Switcher configurations suit Winchesters

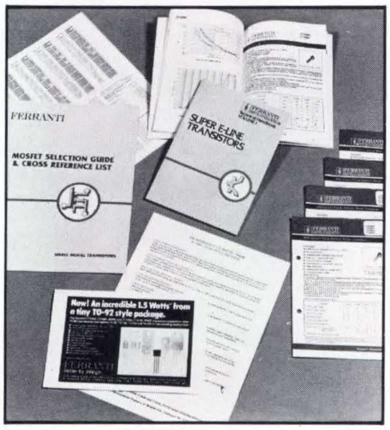
The MASS 210, **Elpac Power Systems' (Santa Ana, Calif.)** most popular magnetic amplifier switcher, is being offered in five configurations to give systems designers greater flexibility. Power combinations of $\pm 5$, $\pm 12$, $+24$, and $+28$ V are compatible with the requirements of Winchester disk drives, and the isolated outputs provide instantaneous peak loading capabilities without degradation of regulation characteristics. The main +5-V output delivers up to 20 A of continuous power. The semiregulated fourth output is floating from ground. **CIRCLE 379**

## HP analyzer and sweepers cost less

Wide market acceptance of the HP 8756A scalar network analyzer has prompted **Hewlett-Packard Co. (Palo Alto, Calif.)** to reduce the price of the instrument to $8500. The company has also lowered the costs of the two broadband sweep-oscillator rf plug-ins that are most often used with the analyzer. The HP 83592A, which has a frequency range of 10 MHz to 20 GHz, now sells for $20,500—a reduction of $3070. Spanning the frequency range of 2 to 20 GHz, the HP 83590A carries a price tag of $17,700, down from $20,310. **CIRCLE 380**

# NEW LITERATURE

## Transistors and MOSFETs




A power supply design package comprises data sheets, a selection guide, and a cross-reference list for Super E-Line and high-voltage Super E-Line transistors, plus more than 150 MOSFET types. Product descriptions, quality assurances, technical data, key parameters, and application notes are contained within.

*Ferranti Electric Inc., Semiconductor Products, 87 Modular Ave., Commack, N.Y. 11725; (516) 543-0200.*

**CIRCLE 381**

## CIM industrial computer board family

Presenting the CIM (CMOS industrial microcomputer) computer board family is a 16-page pamphlet that provides an overview of the microCMOS process—a process that offers both the speed of NMOS and the power and noise immunity of CMOS. In addition to overview information, the brochure discusses why the CIMBUS is the most functional bus structure for CMOS applications. It also contains a buy-vs-build cost comparison on board development.

*National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; (408) 721-5000.*

**CIRCLE 382**

## Male and female headers

Line drawings and specifications are given for male and female headers in a 12-page selection guide. The three-holed 8½-by-11-in. publication contains two spreadsheets on each of the header series, detailing straight and right-angle configurations, as well as single and dual-row options.

*Aptronics Corp., 9450 Pineneedle Drive, PO Box 270, Mentor, Ohio 44060; (216) 354-9239.*

**CIRCLE 383**

## Reference card saves design time

Useful for the design or repair of electronic circuits, a handy reference card presents the operating basics for a variety of components—from op amps to programmable unijunction transistors. Nondigital functions readily available in a single monolithic package are covered, including 13 diode types, 6 types of transistors, 5 families of thyristors, 4 types of light emitters, 9 types of light receivers, plus a-d and d-a converters, amplifiers, comparators, multipliers, tone decoders, VCOs, and more. Names of parts, signal names, detailed operation, and examples of key specification parameters are given on the two-sided plastic card.

*Micro Logic Corp., PO Box 174, 100 2nd St., Hackensack, N.J. 07602; (201) 342-6518. $5.95, plus $1 for postage.*

**CIRCLE 384**

## Connectors for coaxial cable

TNC and BNC connectors for more than 70 RG/U cable types are listed in a 36-page catalog. More than 330 TNC and almost 500 BNC plugs and jacks are described in single-crimp, dual-crimp, and commercial dual-crimp versions. The catalog also lists TNC and BNC connectors for semirigid coaxial cable.

*Amp Inc., Harrisburg, Pa. 17105; (717) 564-0100.*

**CIRCLE 385**

### Digital multimeters and accessories

Comprehensive information is given in an 18-page color brochure for handheld and benchtop/portable digital multimeters. Featured in the literature is the 70 Series, which combines both a digital readout and an analog bar graph in one handheld package. A full line of accessories complementing the DMM line is also described.

*John Fluke Manufacturing Co. Inc., PO Box C9090, Everett, Wash. 98206; (206) 342-6300 or (800) 246-0361.*

**CIRCLE 386**

### Ultra-thin keyboards

A product bulletin (No. 364) describes 1/10-in.-thick keyboards that utilize snap-dome contact systems. Complete electrical ratings and characteristics of the standard graphic overlays are included, along with their respective prices. Special graphic designs and color combinations are depicted.

*Grayhill Inc., 561 Hillgrove Ave., La Grange, Ill. 60525; (312) 354-1040.* **CIRCLE 387**

### FCC emissions specifications

Entitled *Eight Short Questions and Answers,* this brochure provides information on the FCC's emissions specifications for interference reduction. To further assist the engineering community, TKC has established an EMI answer line at (813) 544-2595 to answer questions related to FCC, VDE, MIL-STD, and Tempest specifications.

*TKC Publications, 8609 66th St. N, Pinellas Park, Fla. 33565; (813) 544-2594.*

**CIRCLE 388**

### Joysticks, mice, and trackballs

Positioning and tracking controls for the man-machine interface are illustrated in a 24-page catalog. Hundreds of input controls and options are described—including joysticks, force-sticks, control grips, trackballs, and mice—with a wide selection of interface circuits.

*Measurement Systems Inc., 121 Water St., Norwalk, Conn. 06854; (203) 838-5561.*

**CIRCLE 389**

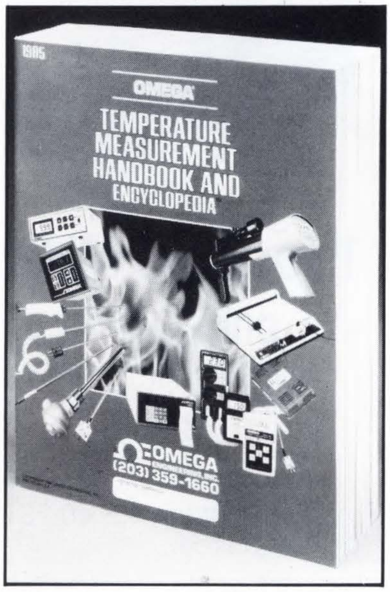
### Load cells and strain transducers

More than 50 models of load cells and strain transducers, plus a line of digital displays, are presented in a 16-page brochure. The document includes photographs, specifications, dimensional drawings, technical support data, and application notes.

*Alphatron Inc., 334 Clark St., PO Box 367, North Andover, Mass. 01845; (617) 687-2371.* **CIRCLE 390**

## NEW LITERATURE

### Temperature measurement




The *Temperature Measurement Handbook and Encyclopedia* lists and specifies a multitude of products in such categories as computer interface equipment, infrared radiation pyrometry, portable handheld instruments, laboratory monitors, controllers, and data loggers. The 718-page manual also contains an expanded technical data section on temperature measurement and control.

*Omega Engineering Inc., 1 Omega Drive, PO Box 4047, Stamford, Conn. 06907; (203) 359-7613.* **CIRCLE 391**

### Data converters and MIL-1553 products

An eight-page bulletin presents various data conversion products and MIL-STD-1553 components. Specifications and technical data are given for analog-to-digital, digital-to-analog, synchro-to-digital, and digital-to-synchro converters. Other products include sample-and-hold and track-and-hold amplifiers, plus units that perform special functions (i.e., control transformers).

*ILC Data Device Corp., 105 Wilbur Place, Bohemia, N.Y. 11716; (516) 228-7324.* **CIRCLE 392**

### Sockets for microcircuit packages

Complete dimensions and specifications are provided in an eight-page brochure for a line of proprietary sockets for JEDEC chip carriers and other multilead microcircuits, plus standard 64-pin DIP packages. Socket types include through-board and surface-mounted chip-carrier sockets, lever-action eject sockets for pin-grid array devices, LIF sockets, and special socket covers.

*Methode Electronics Inc., Interconnect Products Division, 1700 Hicks Road, Rolling Meadows, Ill. 60008; (312) 392-3500.* **CIRCLE 393**

### Broadband communications

Broadband communications products are the subject of a 308-page catalog that includes: distribution equipment, broadband data products, coaxial cable, satellite receiving equipment, off-air antennas, head-end equipment, subscriber products, and minicable/SMATV systems. The catalog also describes product support services.

*Scientific-Atlanta Inc., PO Box 105027, Department A/R, Atlanta, Ga. 30348; (404) 449-2000.* **CIRCLE 394**

### Rf testing accessories

Accessories for rf testing are presented in a 12-page brochure that provides device features, advantages, illustrations, performance specifications, and dimensions. The literature covers broadband antennas, TEM cells, field-sensor telemetry systems, directional couplers, power combiners/dividers, matching transformers, computer interface modules, and system assembly kits.

*Amplifier Research, 160 School House Road, Souderton, Pa. 18964; (215) 723-8181.* **CIRCLE 395**

### Computer supplies and accessories

Perkin-Elmer has entered the mail-order computer supply and accessory business with the introduction of a 40-page color catalog. The *P-E/Prompt* catalog features a broad range of brand name and selected products including "specials," competitively priced and ready for shipment.

*Perkin-Elmer, Data Systems Group, 2 Crescent Place, Oceanport, N.J. 07757; (201) 870-4156 or (800) 732-1632.* **CIRCLE 396**

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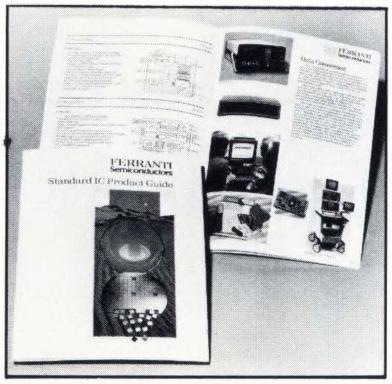
## NEW LITERATURE

### Integrated circuits




The 36-page *Standard IC Product Guide* highlights a full range of integrated circuits for telecommunications, data conversion, referencing, instrumentation, and consumer applications. It contains an overview of the technological developments of each group, along with circuit diagrams of individual devices.

*Ferranti Electric Inc., Semiconductor Products, 87 Modular Ave., Commack, N.Y. 11725; (516) 543-0200.*

**CIRCLE 397**

### TMOS power MOSFET data manual

Featuring data sheets for more than 300 standard devices, a TMOS power MOSFET data manual (DL 135) includes theory, applications, selector guides, and a cross reference. The manual covers all of the device types (comprising eleven different package configurations) currently available from Motorola. Additionally, the book contains a section on small-signal TMOS devices and a glossary of terms, symbols, and definitions common to power MOSFETs.

*Motorola Literature Distribution Center, PO Box 20924, Phoenix, Ariz. 85036. $4 (one to nine copies).*

**CIRCLE 398**

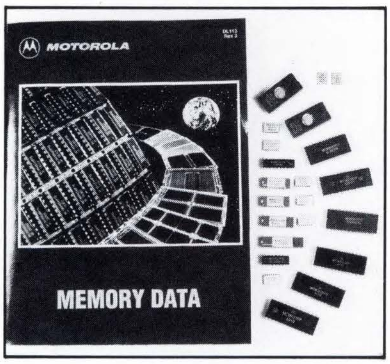
### Power supplies for CRTs

Ten families of regulated high-voltage power supplies for color and monochrome high-resolution CRTs are described and specified in a 20-page catalog. Monochrome supplies offer anode voltages of 1 to 20 kV; a color shadow-mask supply has a 30-W rating at 25 kV.

*Keltron Corp., High Voltage Division, 225 Crescent St., Waltham, Mass. 02154; (617) 894-8700.*

**CIRCLE 399**

### MOS memory devices and bubble memories




Consisting of 13 detailed chapters, a memory data book provides complete specifications for MOS dynamic RAMs, static RAMs, EPROMs, EEPROMs, and ROMs, as well as various bubble memories. The data sheets cover a broad range of topics, such as pin connections, electrical characteristics, testing, and applications information. A master index lists the 96 devices in the memory product line.

*Motorola Literature Distribution Center, 616 W. 24th St., Broadway Bldg. #1, Tempe, Ariz. 85282; (602) 994-6561.*

**CIRCLE 400**

### Series 10000 terminal blocks

A 16-page booklet details the Series 10000 terminal blocks—modular units that combine a circuit function to eliminate installation and wiring of separate electronic assemblies. Complete specifications and diagrams facilitate device selection.

*Cogenel Inc., Entrelec Division, 2 Ram Ridge Road, Spring Valley, N.Y. 10977; (914) 425-7460 or (800) 431-2308.*

**CIRCLE 401**

### General-purpose touch switches

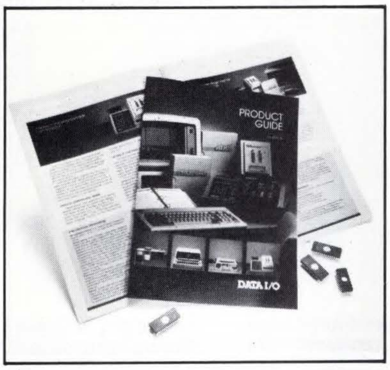
Wild Rover touch switches and switch capsules are the subject of a six-page bulletin (WRTS-8-84). Complete with illustrations and dimensional diagrams, the document provides data on switch ratings, contact resistance, life expectancy, actuation force, and other pertinent specifications.

*Refac Electronics Corp., PO Box 809, Winsted, Conn. 06098; (203) 379-2731.*

**CIRCLE 402**

# NEW LITERATURE

## PROM and logic device programmers




PROM and logic device programmers are presented in a product guide, which includes a system that programs over 1200 devices in either a stand-alone configuration or under the control of a personal computer. Specifications for all products are included.

*Data I/O Corp., 10525 Willows Road NE, PO Box 97046, Redmond, Wash. 98073; (206) 881-6444 or (800) 426-1045.*

**CIRCLE 403**

## Microelectronic artwork patterns

Adhesive-backed patterns used to create artwork for high-density printed circuits are illustrated in a 37-page catalog (No. 601). Included are patterns for hybrids, surface-mounted devices, chip carriers, small-outline transistors, small-outline packages, and custom microelectronic patterns. Also featured in the literature are grid patterns and other design and drafting accessories.

*Bishop Graphics Inc., 5388 Sterling Center Drive, Westlake Village, Calif. 91359; (818) 991-2600.* **CIRCLE 404**

## Overcurrent protection devices

Containing basic background information on fuses and circuit breakers, a 116-page handbook assists in the device selection process. The largest section of the book offers Reliance fuse product information, along with curves and ratings. The handbook also provides sizing information, a glossary of terms, and formulas.

*Reliance Electric Co., 25001 Tungsten Road, Cleveland, Ohio 44117; (216) 266-6013.*

**CIRCLE 405**

## LCD and LED display products

A 320-page display products catalog contains information on a full family of liquid-crystal displays, LCD dot-matrix modules, LED lamps, and LED displays. Application notes, a glossary of terms, industry cross-reference information, and other useful data are included in the helpful reference manual.

*A.N.D., 770 Airport Blvd., Burlingame, Calif. 94010; (415) 347-9916.* **CIRCLE 406**

## Card lists products and manufacturers

A handy reference card lists products from 226 different manufacturers of equipment used by the electronic processing industry. Tools, systems, and equipment for electronic assembly include those for surface mounting, production, IC insertion, and pc board assembly. Alphabetical listings are organized both by manufacturer and by product category.

*Henry Mann Inc., Mann Road, Huntingdon Valley, Pa. 19006; (215) 355-7200.*

**CIRCLE 407**

## Multibus boards and subsystems

Over 75 products for the Multibus—from single-board computers to multitasking systems—are described in a 16-page booklet. Products include 8085-, 8086-, and 80186-based CPU boards; disk drive controllers; serial and parallel I/O boards; and enclosures.

*Zendex Corp., 6700 Sierra Lane, Dublin, Calif. 94578; (415) 828-3000.* **CIRCLE 408**

## MIL-specified storage peripherals

Specifications and applications for rugged MIL-specified computer storage peripherals are detailed in an updated catalog. Products include a dual Winchester disk drive, a removable hard-disk system, a bubble-memory recorder, digital and analog cartridge tape recorders, plus controllers for interfacing with the MIL-STD-1553B bus.

*Genisco Memory Products Corp., 10874 Hope St., Cypress, Calif. 90630; (213) 537-4750 or (800) 821-3693.*

**CIRCLE 409**

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| St. Louis | February 11-12 |
| Dallas/Fort Worth | February 25-26 |
| Los Angeles | March 4-5 |
| Minneapolis | March 11-12 |
| Phoenix | March 18-19 |
| Washington, D.C./Baltimore | March 25-26 |
| Orlando | April 1-2 |
| Long Island | April 15-16 |
| Boston | April 22-23 |
| San Jose | April 29-30 |
| Chicago | May 6-7 |
| Denver | May 13-14 |
| Seattle | May 20-21 |
| *Washington, D.C./ Baltimore — AFCEA | June 5-6 |
| Los Angeles/Irvine | June 10-11 |
| Raleigh/Durham | July 15-16 |
| Boston | July 29-30 |
| Dallas/Fort Worth | August 5-6 |
| Long Island | August 12-13 |
| Phoenix | August 19-20 |
| San Jose | August 26-27 |
| Denver | September 9-10 |
| Orlando | September 23-24 |
| Minneapolis | Sept. 30-Oct. 1 |
| Chicago | October 7-8 |
| Los Angeles | October 21-22 |
| Washington, D.C./Baltimore | October 28-29 |
| San Jose | November 11-12 |
| Boston | November 18-19 |

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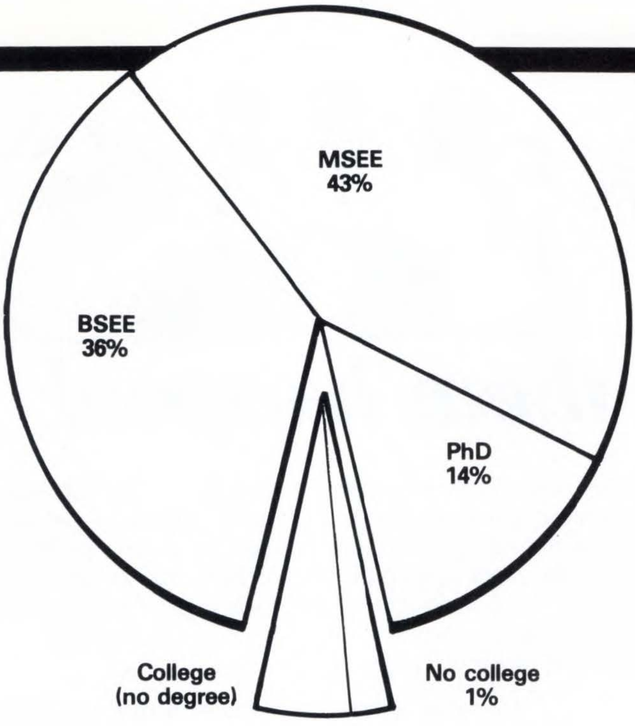


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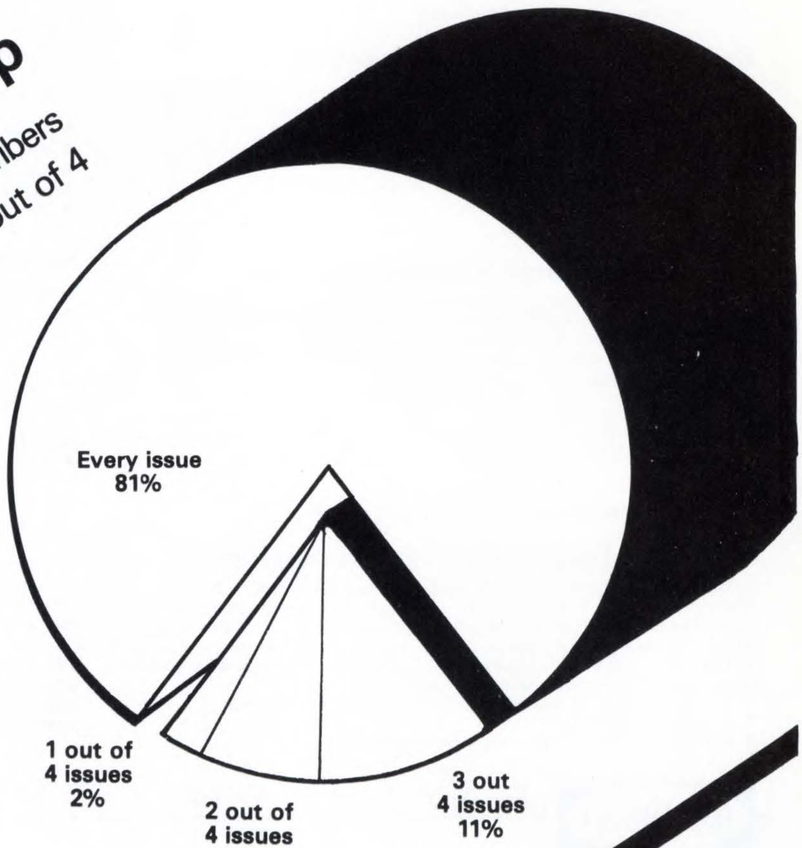





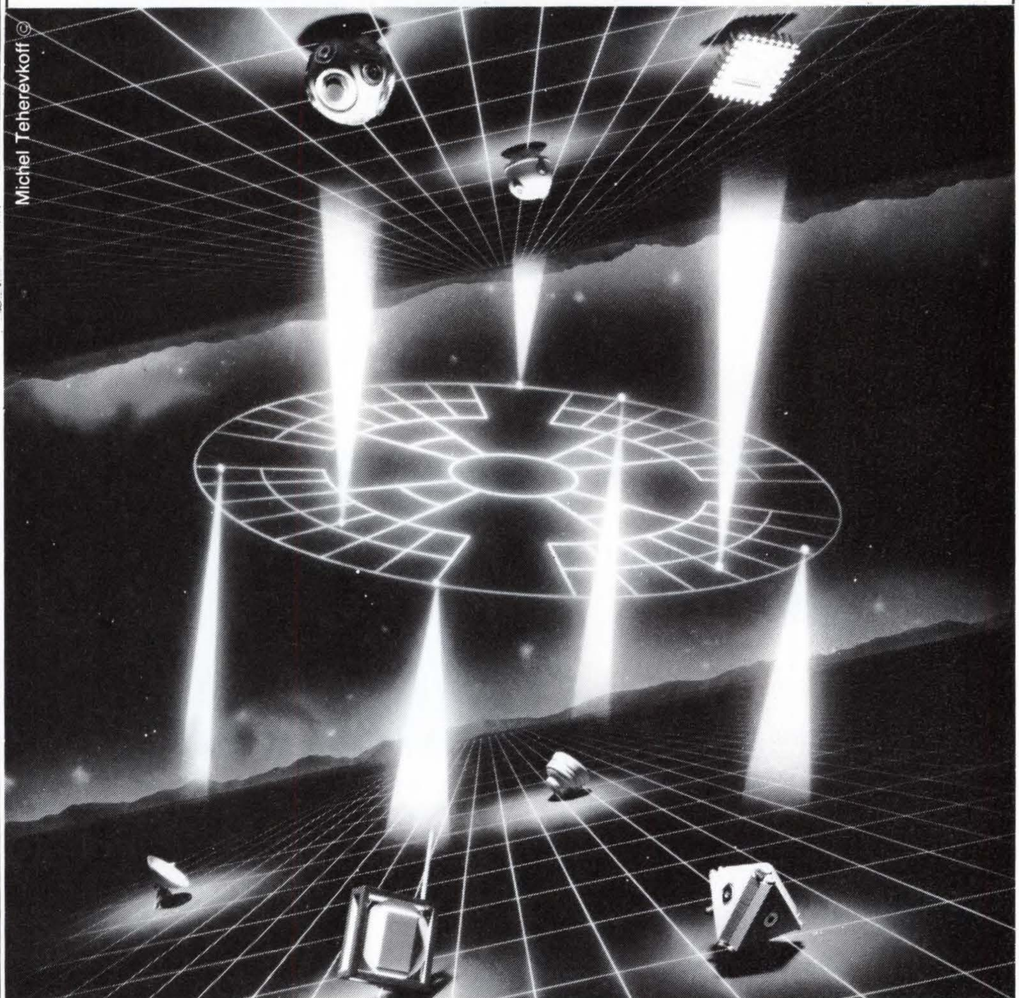

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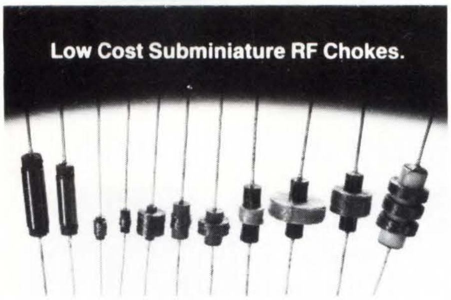


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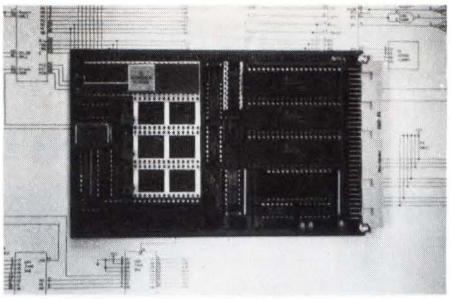

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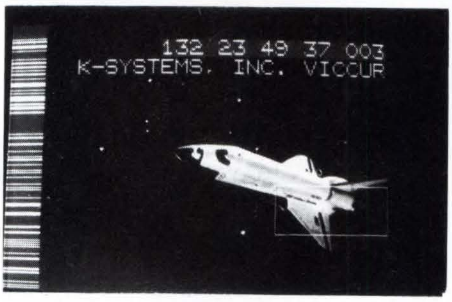
SINGLE CHIP MICROCOMPUTER **275**

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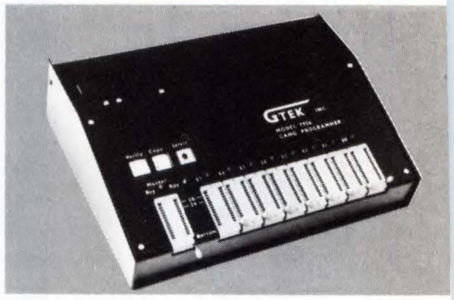


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GANG PROGRAMMER **277**


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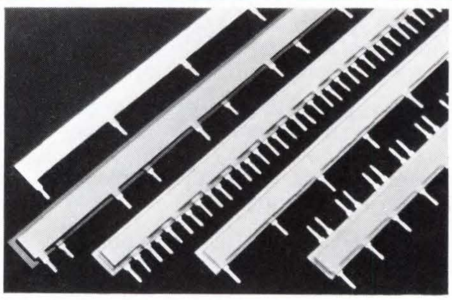
ENGINEERING SOFTWARE **278**



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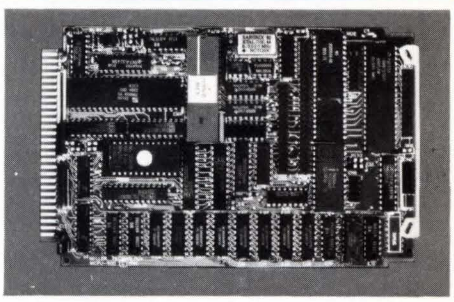
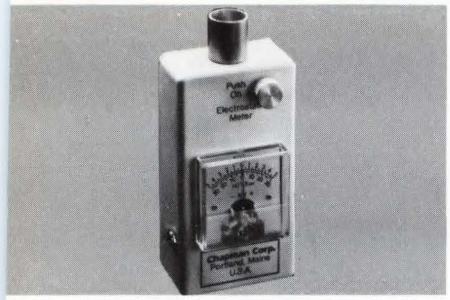
BUS BARS **279**



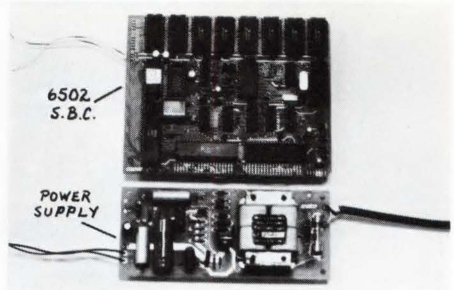
**Solve virtually all your STD system problems w/a single card.** The MCPU-900 provides 4 MHz Z80A, 64K RAM, & up to 16K ROM. 1797 disk controller handles four floppy drives w/all—digital data separator. Also on board are a serial port & 24 bit parallel port that may be used for SASI/SCSI control w/the SASI-100 board. Three 10 MHz counter/timers & Centronics printer port round out the interfacing capabilities. The $795 price includes 100 hour burn-in & 200 pg. manual. Miller Technology, Inc., 647 N Santa Cruz Ave., Los Gatos, CA 95030, (408) 395-2032.

STD MICROSYSTEM **280**



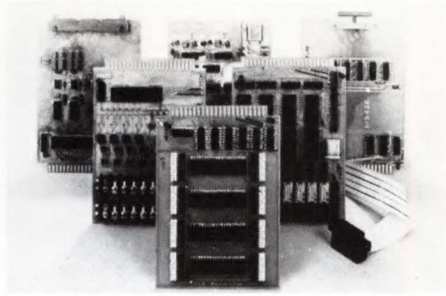

**ELECTROSTATIC METER:** For locating and measuring electrostatic voltage. An accurate, compact instrument that detects presence, magnitude and polarity of static electricity. Use to locate static problems or to position static eliminators for effectiveness. A detachable ground wire assures a reading accurate to ±5%. Chapman Corp., 125 Presumpscot St., P.O. Box 10700, Portland, Maine 04104 (207) 773-4726.

ELECTROSTATIC METER **281**




**6502 SINGLE BOARD COMPUTER** with 16K CMOS RAM, sockets for two 2532 EPROM 8K. Real time calendar clock using MM58167, one RS232 serial port using a 6551ACIA and four parallel ports using two 6522VIA. Uses a single 5 volt power source at 600MA, 5.5 × 7 inches. Assembled and tested. $389.00. 5 volt, 1 amp **SWITCHING POWER SUPPLY** with floating battery backup circuit. Input 115VAC or 10 to 15VDC, 3 × 7 inches PCB. Assembled and tested. $79.00. **Custom Programming Group, Inc.,** 47-2A Marchwood Road, Exton, PA 19341. (215) 363-8840.

CUSTOM PROGRAMMING GRP., INC., **282**

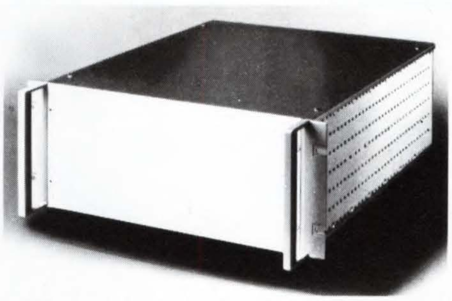


**6800/6809 Micro Modules.** OEM 6800/6809 MICROCOMPUTER MODULES for dedicated control and monitoring. Interfaces for sensors, transducers, analog signals, solenoids, relays, lamps, pumps, motors, keyboards, displays, IEEE-488, serial I/O, floppy disks. Wintek Corporation, 1801 South Street, Lafayette, IN 47904-2993. (317) 742-8428.

MICROCOMPUTER MODULES **283**


**EMI PROBLEMS?** Let Eagle Magnetic FIND your magnetic shielding problems! For more information write or call: **Eagle Magnetic Co., Inc.,** P.O. Box 24283•Indianapolis, Ind. 46224. Phone (317) 297-1030.

MAGNETIC SHIELDING **284**



**HEAVY-DUTY RACK-MOUNT ENCLOSURES TRACEWELL'S CH SERIES FEATURES:** Precision die-cast handles • Universal mounting rails standard • Captive fasteners top/bottom • Four EIA heights: 3½", 5¼", 7", 8¾" • Two depths 19" and 12" standard • Complete enclosures from $145 (1-4 pcs) • Tracewell Enclosures, 7032 Worthington-Galena Rd, Columbus, OH 43085 (800) 848-4525, in Ohio (614) 846-6175.

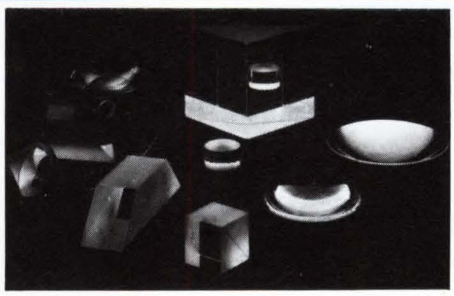
RACK MOUNT ENCLOSURES **285**


**RELIABLE 0.1 AQL SOLID STATE RELAY.** Conditioning screen at 80°C prior to shipping yields ultra-reliable 0.1 AQL SSR. UL recognized (File #55197); CSA approved. 615V meets VDE & IEC standards. The 615 series features AC load ratings to 40 amps @250VRMS, optical isolation to 3750 VRMS, logic compatible input, & zero voltage turn-on. Constant current input from 3 to 32VDC. Incorporates custom IC's to reduce component count. From $10.75 ea. in production quantities. Teledyne Solid State Products, 12525 Daphne Ave., Hawthorne, Ca. 90250 (213) 777-0077.

RELAYS **286**


**THE MICROWRITER—**Six keys do the work of sixty standard keys. You operate it with one hand and it takes only an hour to master. It weighs 2 lbs, is handheld, and redefines the word 'portable.' It is a sophisticated and powerful word-processor. Upload and download from RS232C computers or printers. $499. **MICROWRITER INC., 251 East 61 St., New York, NY 10021—Phone: (800) 654-4001 or (212) 319-8602.**

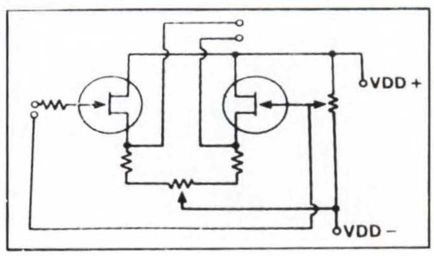
FREE USER'S MANUAL **287**



**ROLYN OPTICS CO.** supplies all types of "Off the Shelf" optical components. Lenses, prisms, mirrors, irises, microscope objectives and eyepieces and many others. All from stock. We also supply custom products and coatings in prototype or production quantities. 75 page catalog describes products and prices. ROLYN OPTICS CO., 738 Arrowgrand Circle, Covina, CA 91725 (818) 915-5707 & (818) 915-5717. TELEX: 67 0380.

OPTICS **288**

Dual, ultra Low Noise FET CD860




This dual FET is designed for low level amplifiers with input noise voltage typically 1.4nV √Hz at 1 kHz. Device has min. Gm of 25,000 μMho per side, assuring voltage gain of 25 min. with 1K drain load. The 10mA operating point is easily held due to low pinch-off voltage, as source follower, CD860 has typical output impedance of 24 ohms. Gm is matched to ±5% and VPO to ±25mV. Teledyne Crystalonics, 147 Sherman St., Cambridge, MA 02140. Tel. (617) 491-1670 • TWX: 710-320-1196.

DUAL FET **289**

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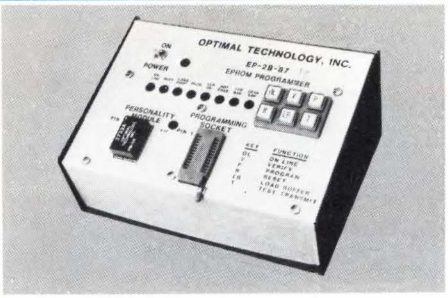


**EPROM PROGRAMMER.** Model EP-2B-87 comes with RS-232 and 20 Ma. current loop. Programs 2708, 2716, 27C16, TMS2716, 2732, 27C32, 2732A, 2532, 2764, 2764A, 27C64, 27128, 27128A, 27256, 2564, MCM68764 EPROMS; 2816A 2864 EEPROM; 8751, 38E70 MPU. Intel, Motorola, and Tektronix formats. Stand alone copy, edit, 17 RS-232 commands. Price, $575 for 8K buffer. Personality modules $18 to $36. Optimal Technology, Earlysville, Va. 22936. 804-973-5482.

EPROM PROGRAMMER **290**

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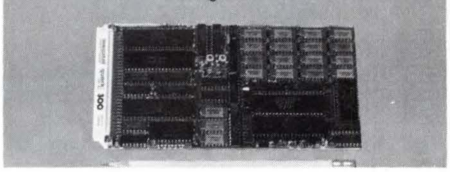

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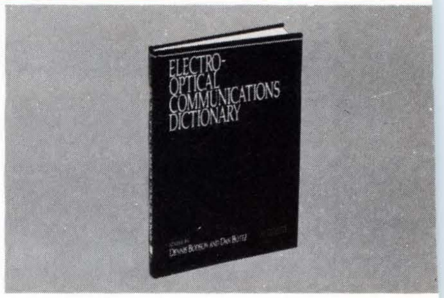
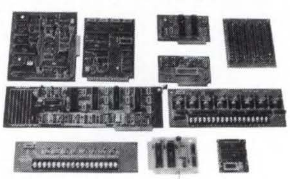
MEGATEL QUARK BOARD **291**




**ELECTRO—OPTICAL COMMUNICATION DICTIONARY:** Dennis Bodson & Dan Botez Eds., Never be at a loss for words with thi complete reference to the most commonl used terms in electro-optical communications Send $22.95 plus $2.00 to cover postage & handling to Hayden Book Company, 1( Mulholland Dr., Hasbrouck Hts., NJ 07604 Reference number 0961 must be included or your check or money order. If not satisfied return the book undamaged, within 10 days fo refund.

COMMUNICATIONS DICTIONARY **29**

## MICROCOMPUTERS AND INTERFACES



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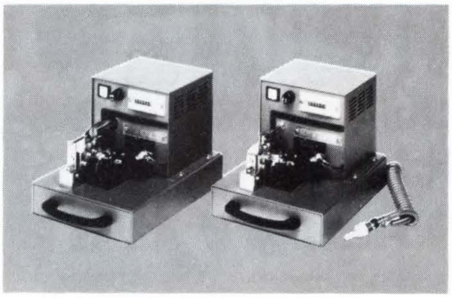
MICROCOMPUTER/INTERFACE CATALOG **293**



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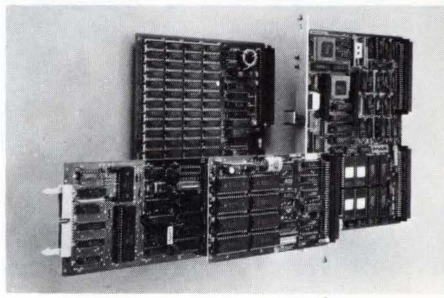
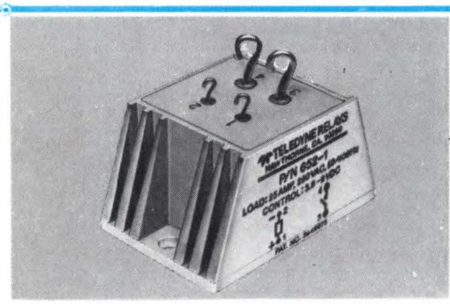
TUBE CUTTING MACHINES **294**



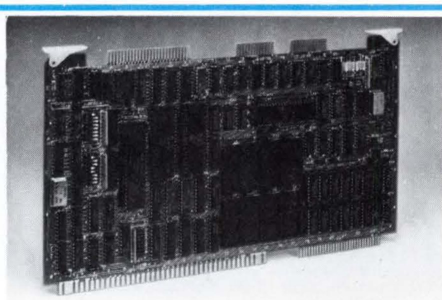
**VME 68000 FAMILY MODULES** Full MOTOROLA compatible but reinforced 8MHz/10MHz CPU modules with battery backed-up RTC & on-board CMOS RAM, 512KB and 2MB DRAM memory modules. Static 64KB RAM, ROM, Floppy I/F, Hard Disk I/F, Serial I/F modules. **AMPERE, INC.** Asahi Bldg., 5-chome, Nishi-Shinjuku, Shinjuku-ku, Tokyo Japan Telex J33101 AMPERE PHONE 03-365-0825.

CPU MODULES **295**



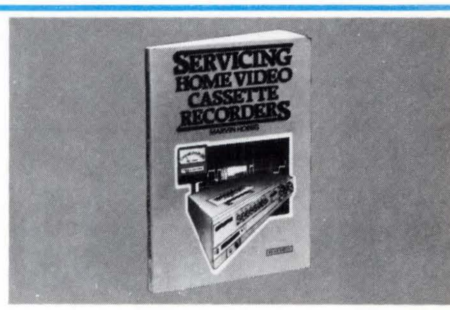

**25AMP MIL SOLID STATE AC RELAY.** Teledyne's 652 AC relay features load rating of 25A at 250VRMS over 45-440Hz frequencies. Synchronous "zero voltage" turn-on & zero current turn-off result in lower EMI levels compared w/mechanical relays. Highly immune to transients. Optical isolation 1500VRMS. Control range 3.8 to 32VDC @ 10mA. Logic compatible. Case is 1.57" × 2.41" × 1.30" QPL to MIL-R-28750/10. Meets MIL-STD-704B. Model 653 is DC version. Teledyne Solid State Products, 12525 Daphne Ave., Hawthorne, CA. 90250. 213 777-0077.

RELAYS **296**



**Z8000™ MULTIBUS™ SBC.** Z8001 or Z8002 16-bit CPU (6 MHz); 32K or 128K DRAM (upgradable to 512K); up to 48K static RAM or EEPROM; up to 128K EPROM; 2 RS-232 ports (Z8030 SCC); 40 parallel I/O lines, six 16-bit counter-timers (Z8036 CIOs); vectored interrupts. EPROM Debug Monitor, MICRO CONCURRENT PASCAL, C, FORTH, VRTX. Dev. Z8000 software on IBM PC, PDP-11, Intel MDS, Olivetti M20 or 8080/Z80 CP/M system. Z8000™ Zilog, Multibus™ Intel Corp. SINGLE BOARD SOLUTIONS, 7669 Rainbow Dr., Cupertino, CA 95014. 408-253-0181.

SINGLE BOARD SOLUTIONS **297**

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RECORDERS **298**

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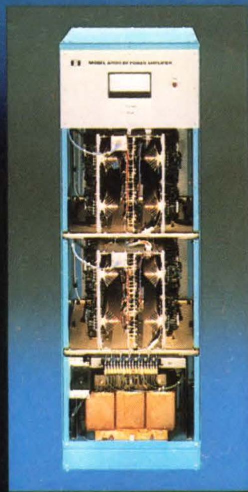

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