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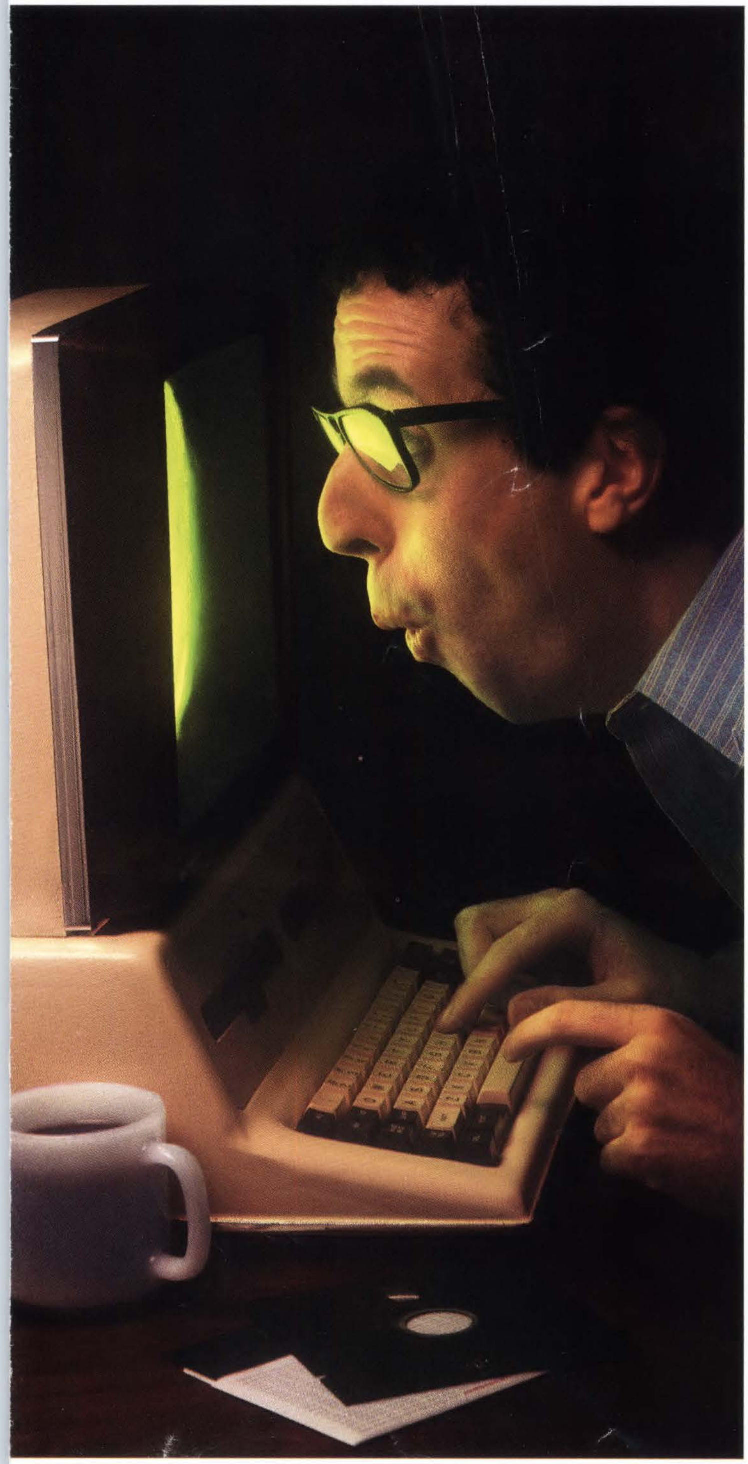
ElectronicDesign

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE
JANUARY 10, 1985

1985 TECHNOLOGY FORECAST

AMD YOUR CRT.



AMD's CRT controller family wrings every last drop of performance out of your video screen.

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The Am8052. You'll wonder where the flicker went.

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You get cleaner, crispier characters with the 100MHz video system controller. And proportional spacing down to two pixels.

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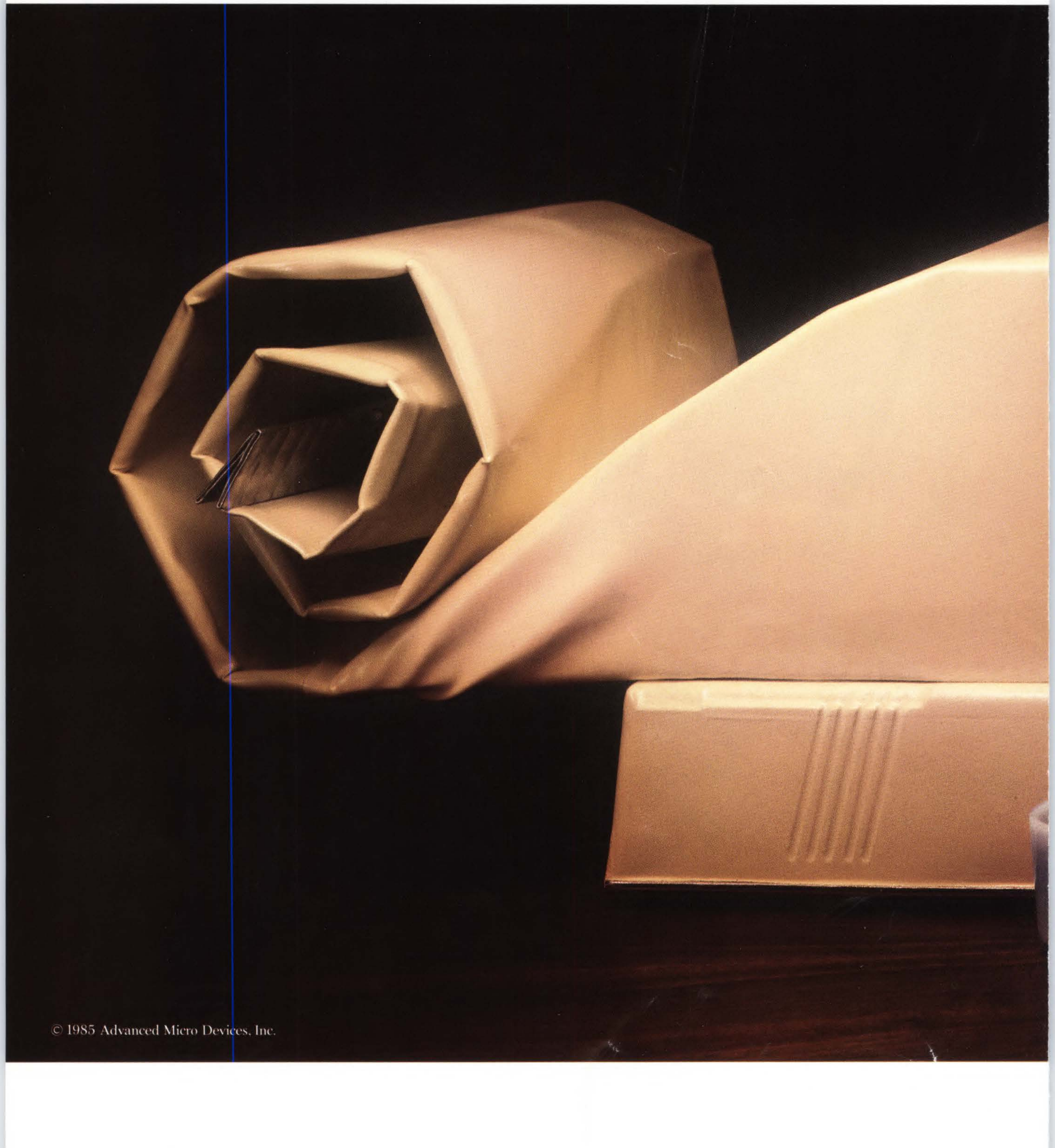
CIRCLE 131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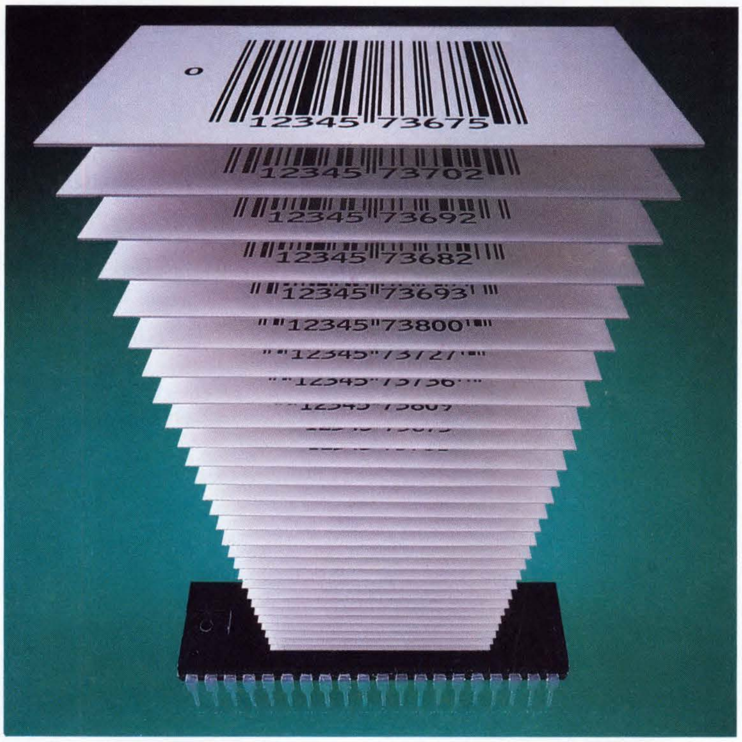
SURPRISE!

Now, designing in bar code capability is fast and easy with HP's new decoder IC and wands.

HP offers a variety of bar code solutions.

OEM's who want to help meet the needs of end-user customers are adding bar code reading capabilities to their products. And HP offers you a one-supplier solution to make these new design-ins fast and easy. Our new decoder IC and digital wands, as a product set, offer a complete component solution for bar code reading. Or, the wands are available separately. And HP can fill your orders now.



HP's new decoder IC simplifies designs.

HP's new decoder IC can save you considerable time and money in bar code software development. Both parallel and serial ASCII interfaces are available, so the IC is easy to use with most common microprocessors. It fits easily onto your PC board. There's no need

to develop your own decoding software, or use up time on your host microprocessor. And since the IC performs the functions of the typical decoding box, you eliminate that piece of equipment altogether.

Moreover, the new decoder IC gives you decoding capability for standard industrial and commercial bar codes—the 3-of-9, Interleaved 2-of-5, UPC, EAN and JAN codes—all on a single chip. And it's been optimized to use with either our new HBCS-2000 or HBCS-4000 series wands. The decoder IC and a wand are available together in the HBCR-1000 series Component Bar Code Readers.

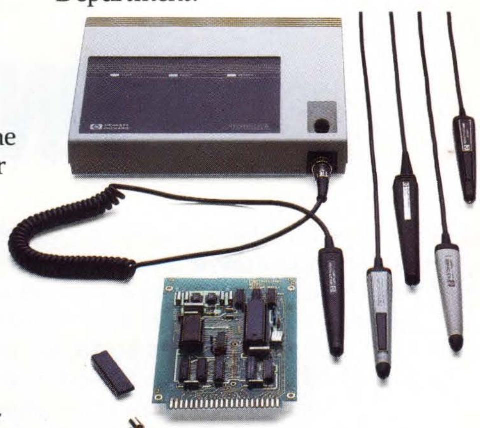
HP's new sapphire tip wands feature rugged construction.

HP's two new digital wands are designed for high performance bar code scanning in both industrial and commercial applications. They feature tough, replaceable sapphire ball tips, rugged construction, a variety of resolutions and a standard digital TTL interface. Each wand can be used at scanning angles up to 45 degrees for improved reading performance.

For your heavy industrial and LOGMARS applications, select from the new HBCS-4000 series sealed metal wands.

And for commercial or light industrial uses, choose from the HBCS-2000 series polycarbonate-cased wands.

For pricing and delivery, contact your local Hewlett-Packard authorized components distributor. In the U.S., call Hall-Mark, Hamilton/Avnet or Schweber. In Canada, call Hamilton/Avnet or Zentronics, Ltd. For more information, call your local HP sales office listed in the telephone directory white pages and ask for the Components Department.



HP: The right choices for bar code solutions.

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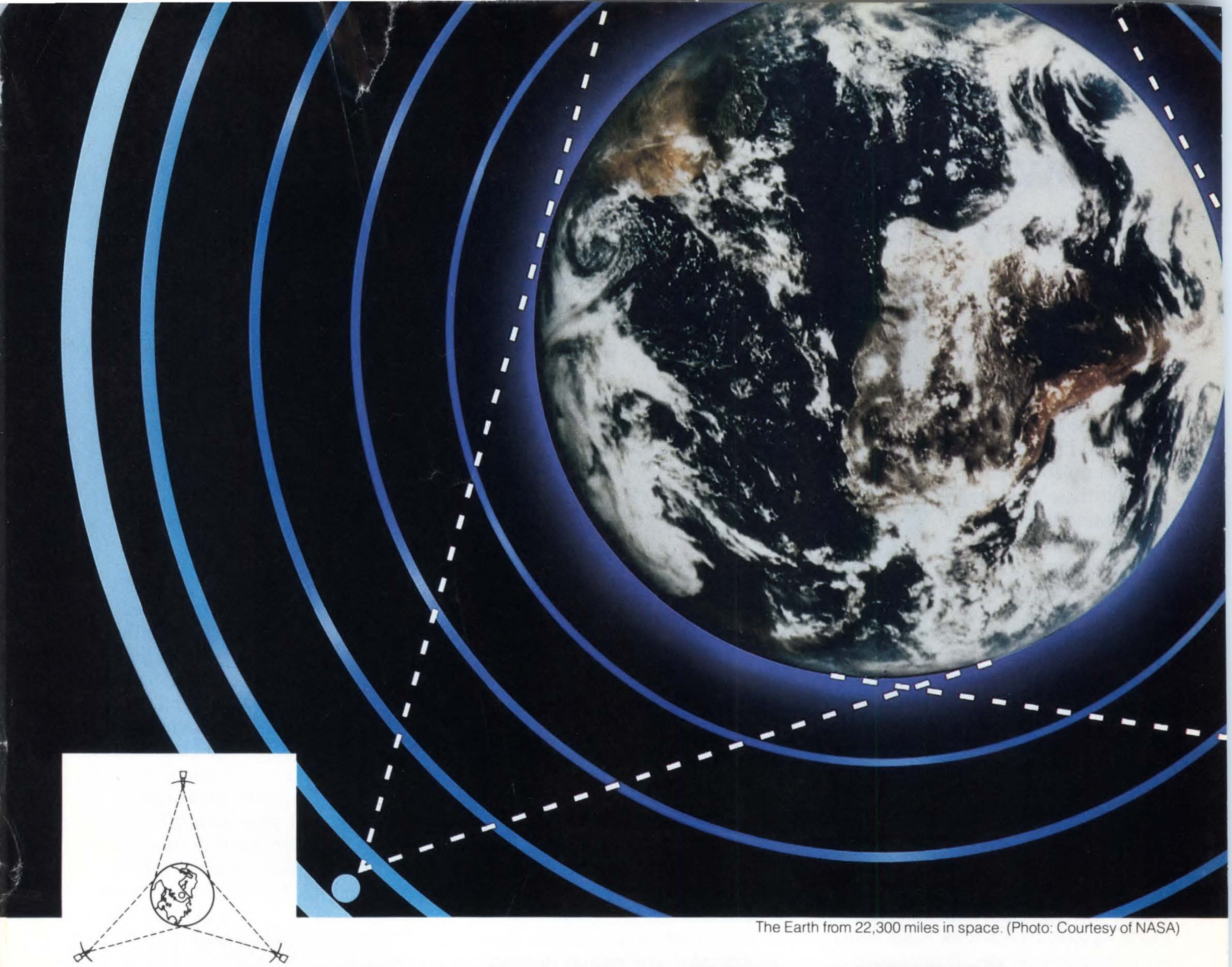
CIRCLE 2



The Earth from 22,300 miles in space. (Photo: Courtesy of NASA)

Clarke's proposed 3-satellite system.

FINDING NEW WAYS...

In 1945, Arthur C. Clarke—a British mathematician, wireless operator and creative science fiction writer found a better way to beam communications signals around the world. He theorized that an artificial satellite, carried by a rocket to an orbit 22,300 miles above the earth's equator, traveling at 6879 mph (7× the speed at which the earth rotates on its axis), would appear motionless to an observer on earth. From that height, Clarke reasoned, a radio relay station could cover one-third of the earth's surface; three such satellites, placed in geosynchronous orbit around the equator could provide worldwide communications. In 20 years, advances in electronics, miniaturization and rocketry made Clarke's dream a reality and gave the world improved communications capability.

Likewise in 1969, Mini-Circuits made its total commitment to serve the emerging communications market...by replacing expensive, custom RF signal-processing components with low-cost, catalog units with unparalleled reliability.

Our dream, like Clarke's, has come true. Over 1,000 catalog items available with such Mini-Circuits innovations as our exclusive HTRB burn-in testing, the world's only 3-year guaranteed mixers, computer-automated performance data (CAPD) to eliminate design guesswork...just to name a few.

Mini-Circuits' products have become the industry standard. We are actively dedicated to the pursuit of further improvements in product cost/performance, quality and reliability for more effective worldwide communications.

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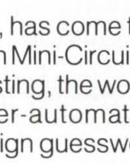


CIRCLE 3

F79 Rev. A

BEHIND THE COVER

Predicting events in the electronics industry is somewhat akin to tracking the motion of subatomic particles. Quantum mechanics states that the behavior of individual particles cannot be pinpointed, but statistical group behavior can. The greater the number of particles included, the more accurate and dependable the prediction.

Similarly, opening an arbitrarily small window to the world of technology can leave utterly the wrong impression. Try to anticipate the behavior of a single segment—the computer sector, for instance. Which computer architecture, which storage peripheral, which semiconductor processing technology—even which competing nation—will emerge on top is anybody's guess.

Even worse, watch nontechnical industry events one by one, and a bleak image may develop. At any given moment, a billion-dollar computer house may go bankrupt; the Federal government may indict a semiconductor test cheater; an established company may sue a start-up to recover stolen secrets; a trusted employee may pilfer hard-to-get ICs or help smuggle sensitive products into the forbidden Eastern Bloc.

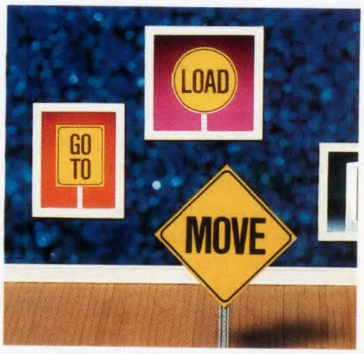
But open the viewing port to panoramic proportions, lump together all industry events—technical and otherwise—and the composite picture gives a far truer glimpse of the future. The outcome is 99% certain, and the sometimes dismaying events do not seem to count individually.

By the end of the decade, the electronics industry clearly will be among the top two or three in the U.S. It will be propelled by continuously evolving products calculated to overcome the stubborn problems of low productivity, obsolete factories, and short supplies of skilled labor. Its overall nature will undergo some striking changes: startlingly different computers, highly intellectual software, continually shrinking parts and packages.

For the enterprising participants and those who enjoy the fruits of their efforts, the electronics industry of 1990 will open some remarkable new vistas.

ElectronicDesign
January 10, 1985 Vol. 33 No. 1

Departments



Technology News

1985 Technology Forecast

Design Entries

In The Next Issue

- Technology Report: Electrolytic capacitors
- Network debugger sorts through Ethernet software and hardware
- A chip set for bus control
- The 68020's dynamic bus

Cover photography and opening spreads by Ken Schroers

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New Products

CONTENTS SPOTLIGHT

1985 Technology Forecast 110

Engineers have long been accustomed to making demands on technology. But 1985, as our Technology Forecast predicts, will force them to do an about-face: Never before has technology demanded so much of engineers. Take our report on software, expert systems to be specific (p. 112). As they move out of the lab and into the commercial realm, system designers will have to become at least proficient in software if not experts in it. Testing, too, will undergo wide-reaching changes (p. 142). Test engineers will be drawn into design matters; designers will shoulder more of the burden for instilling testability into their chips, boards, and systems. As for computers themselves, reduced-instruction-set machines (p. 174) will challenge the traditional view of system architectures, proving that bigger may not always be better.

Even something as mundane as the telephone system, as our fourth Technology Forecast discusses (p. 198), will keep enterprising designers busy preparing telecommunication chips and systems for a monumental goal—all-digital transmission and switching. Our last Technology Forecast explores a relatively new area but one that is here to stay: surface-mounted packaging (p. 232). Chip designers, process experts, test engineers, and makers of automatic test equipment all will have to learn new tricks.

Backing up those predictions, and making a few of their own, ten leading scientists foresee a new look in electronics, computers, communications, and instruments (p. 261). All agree that software—once the domain of a few—will be the driving force behind any advances.

The 68020 microprocessor 335

Few microprocessor developments have inspired system designers as much as full 32-bit chips. But reality, in the form of peripherals with interfaces 8 and 16 bits wide, sometimes barges in. The 68020 shrugs that off, thanks obviously to its speed and power and less obviously to a unique mechanism that adapts the chip's 32-bit data bus to the width of a peripheral's bus.

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Because your application calls for it. Even though we make solenoids in just about any size and shape... pull or push. AC or DC. Tubular in traditional or long life. Box frame, laminated and U-frame. Even though our standard models meet just about every electromechanical application, <u>you</u> could be designing the <u>exception.</u> In that case, we'll customize a solenoid to fit your need. Whether we modify an existing model or develop a new one, it will fit your specification. Precisely.

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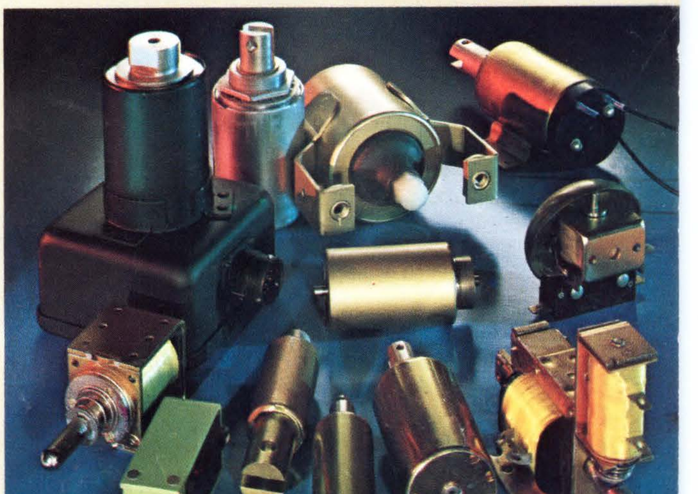

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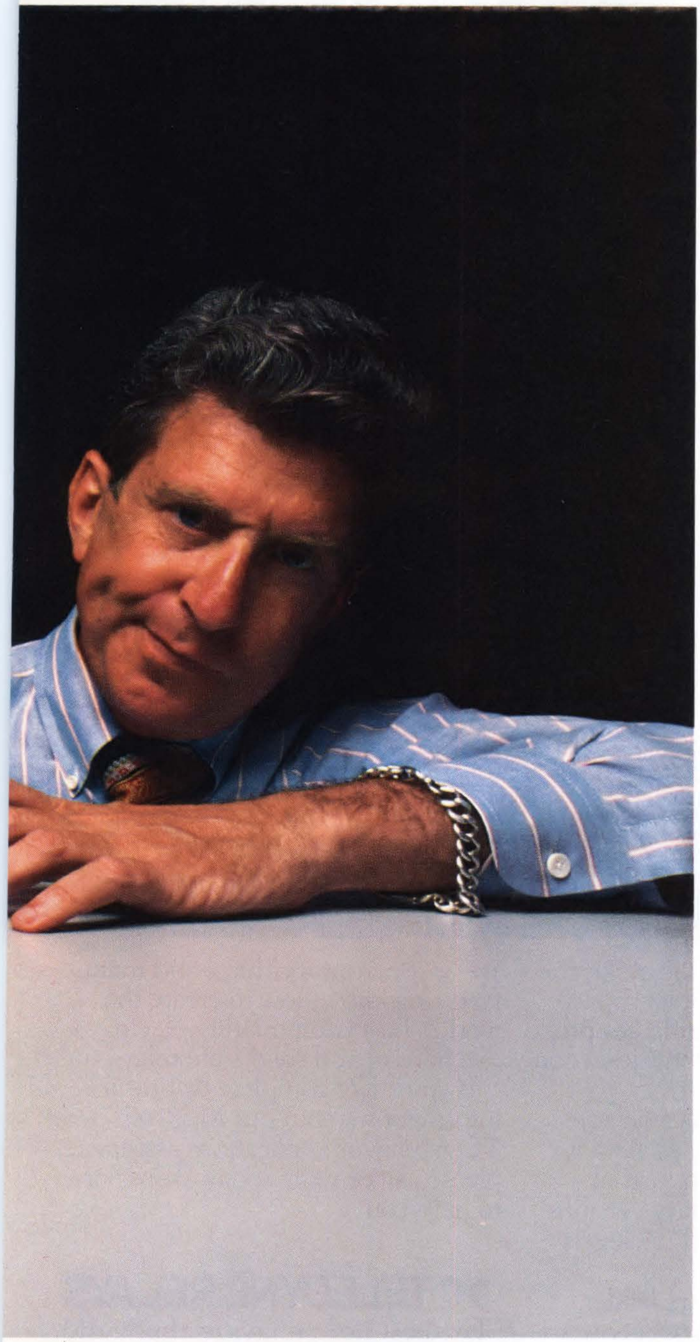

Maglatch TO-5. The world's smallest relay with indestructible memory.

Our little magnetic latching TO-5 relay simply never forgets. Once it's set with a short pulse of coil voltage, Teledyne's Maglatch TO-5 will retain its state until reset. Even if system power fails or is shut off.

Because holding power is not required, the Maglatch TO-5 uses less energy than any other relay you can buy. This makes it ideal for any situation where power drain is critical. And its tiny footprint makes it ideal for high density printed circuit boards.

For RF switching applications, the Maglatch's low intercontact capacitance and contact circuit losses provide high isolation and low insertion loss up through UHF.

The Maglatch TO-5 is available in SPDT and DPDT styles. And it comes in commercial/industrial versions as well as military versions qualified to "L," "M," and "P" levels of MIL-R-39016.

Teledyne is an industry leader. We have been for over twenty years. We've used our technical and manufacturing know-how to create the world's best subminiature electromechanical and solid state relays.

If you'd like complete technical information about our Maglatch TO-5 relay, or applications assistance, please call or write today. We're here to help you.

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CIRCLE 6

ON REFLECTION

On-the-job obsolescence: Engineering schools must assume some blame

A number of recent surveys not only have confirmed and discredited some widely held beliefs but have revealed some startling information about engineers and their careers. For instance, the Massachusetts High Technology Council found that American engineering schools leave students ill-prepared for a long and healthy career. In fact, it found that engineering managers consider their charges beyond their prime at the age of 33, and engineers themselves put the apex of their careers at age 37.

One eminent MIT professor suggests the reason: An engineer's specialties quickly become obsolete nowadays. Overspecialization—to the extent that CMOS designers can bump NMOS designers—is considered ludicrous nearly everywhere except the United States. In most European companies, for example, an engineer must be a generalist, able to switch readily from logic design to quality control and then to production.

As ELECTRONIC DESIGN's Career Survey revealed (Oct. 31, p. 137), most readers concur that knowledge of computers and software is a prerequisite for today's engineers and engineering managers. On the other hand, they shatter the contention that engineering schools overemphasize computer science at the expense of, say, analog design or mathematics. In fact, the one category in which respondents confessed to being inadequately prepared is software: A whopping 78% felt that software had gotten short shrift at their alma mater.

What should our engineering schools do to give their alumni a fairer break? Primarily, they must raise their standards. In Europe, only 25% of high-school graduates—all stringently prepared—get into college; the ratio in America is 60%. Our universities then must spend a year filling in the gaps in the students' knowledge.

In addition, all engineering schools must learn to resist industry pressures to simply crank out computer fodder—graduates who can sit down at a terminal and design an 8-bit shift register the first day on the job. In some cases, the American EE averages 1500 to 2500 hours of classroom time before graduation, compared with twice that or more elsewhere. Obviously, that is not enough time for learning both basic and immediately salable skills.

I remember a teacher in the bombed-out ruins of postwar Europe, who put it succinctly: "It won't be easy to teach you about the world without books or laboratories. But we can teach you one thing that is more important than even physics. We can and will teach you how to learn." Perhaps one problem of our engineering schools is too much equipment. In other countries, engineers must make do without gadgetry and learn timeless skills instead.

In that regard, many American schools do a dismal job. Engineers who know their physics and master the art of learning never become obsolete. Of course, it does not hurt if they also are taught how to write software—in other words, how to express their thinking clearly—because that raises their chances of being hired and being kept.

Max Schindler

Max Schindler

Every which way. Wasting time and money running around sharing data the old, inefficient, unreliable way. By hand. And foot.

With Intel's multi-user development tools, you'll never run that risk. Whether you work on a VAX,* network your Intel

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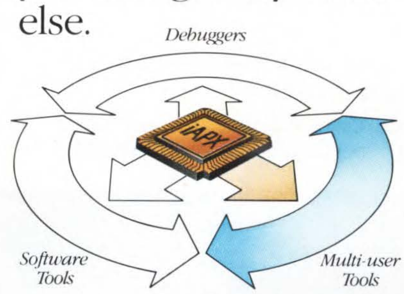

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In your system or on the bench...

the latest HP counter delivers all the right numbers. At the right price.

A new standard for your system.

The HP 5334A is quickly becoming the new system standard. And for good reason: Full HP-IB programmability is included in our low price of $2,800*. That means it's a natural for fully automatic systems. Add to that automatic peak amplitude measurements and our exclusive auto attenuation for a real counter breakthrough in this price range. Plus easy interfacing to computers, such as the HP Series 200. And the HP 5334A can even help boost your overall system performance. That's because its internal processor performs math functions and automatic measurements, which lower your system overhead.

Fast and easy measurements on your bench.

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The quickest way to get our number.

For more information on the HP 5334A Universal Counter or the full range of solutions to your time interval or frequency measurement problems, request our data sheet and our complete counter brochure. Call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

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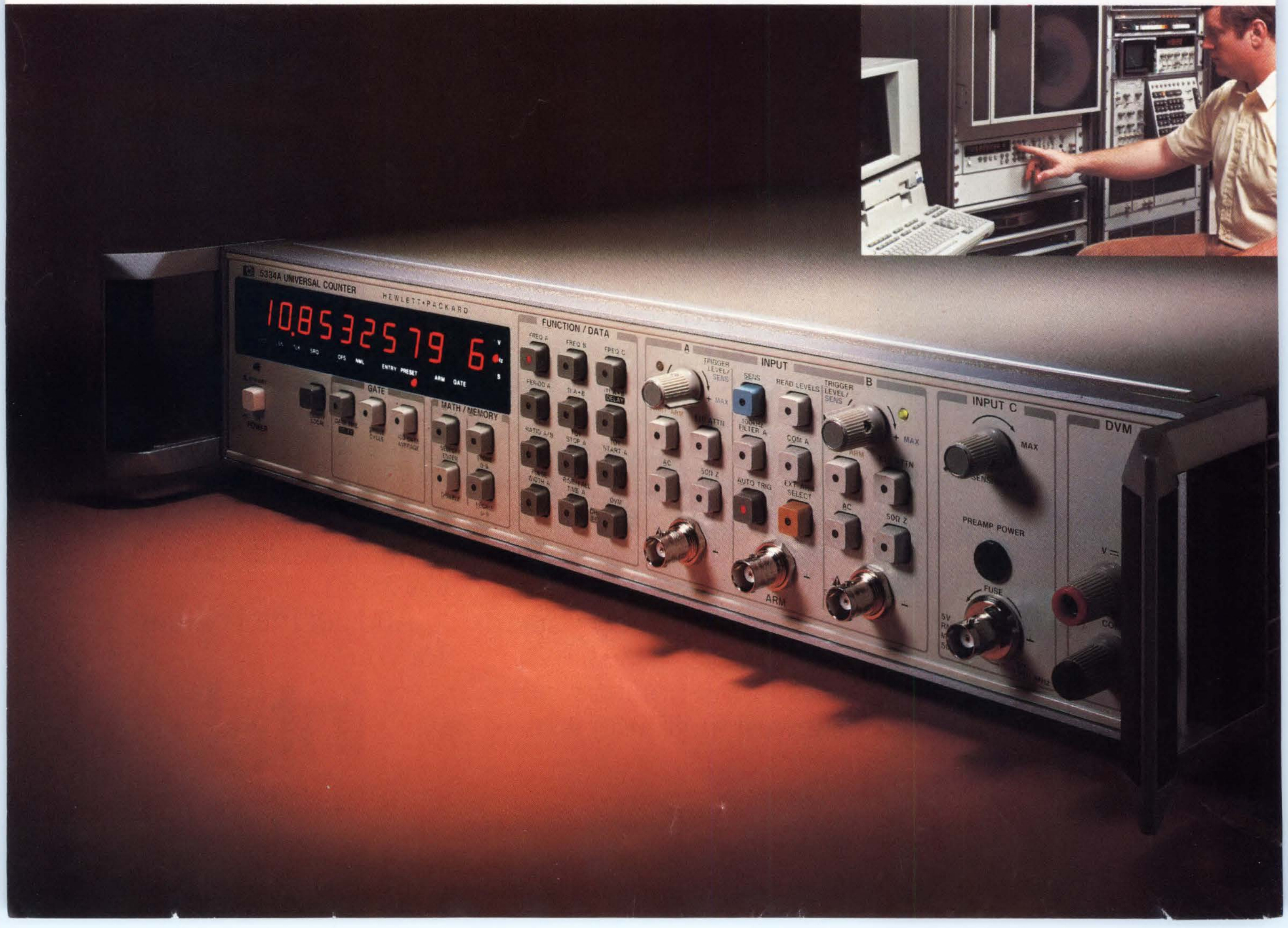


READER FEEDBACK

A notable omission

The Product Report "Focus on Board-Level Modems" in the Dec. 13 issue [p. 25], although illuminating, fails to mention one of the technical leaders in the modem industry: Cermetek Microelectronics Inc.

Our company makes a great many board-level modems. Indeed, we serve the OEM market with a comprehensive range of vertical standard-modem products, from IC components to fully packaged modems, and have over the years been responsible for a number of significant technical innovations, including the first component technology to allow an OEM to design a modem into a product.

Our board-level modems support the full range of IBM products using the latest microprocessor and LSI technology. We also make customized 300- and 1200-bit/s modem boards for a variety of OEMs.

Howard A. Raphael
President
Cermetek Microelectronics Inc.
Sunnyvale, Calif.

Setting a comparison straight

I would like to take issue with the data cited in the Nov. 29 On Reflection by Mark Brownstein, "Optical-Disk Drives May Soon Rival Winchesters, Floppies" [p. 11]. Mr. Brownstein says that 8-in. Winchesters hold up to 100 Mbytes and their access time is roughly 30 ms. He also states that although improvements are expected, they will be storing under 300 Mbytes for many years to come.

I would like to point out that we have been marketing a 212-Mbyte 8-in. Winchester for the past two years, with an access time of about 25 ms. I would also like to refresh Mr. Brownstein's memory that your Nov. 15 issue carried an article (under my byline) describing both 330- and 660-Mbyte 8-in. Winchesters ["Highest-Capacity 8-in. Drive Presents Chioce of Interfaces," p. 271], which we currently have in preproduction. The access times for these drives are an average of 18 ms or less.

Now, I realize that Mr. Brownstein is trying to make a case for optical-disk drives; however, I feel that his premise of their being rivals for the Winchesters and floppies is a bit far-reaching, particularly in view of the fact that his information on Winchesters is obviously sadly outdated.

Clyde Czernek
President
MegaVault Memories
Woodland Hills, Calif.

Preventing undesirable frequencies

It is true that the Design Solution circuit on p. 330 of the Nov. 15 issue ["Pseudo-Sine-Wave Circuit Generates

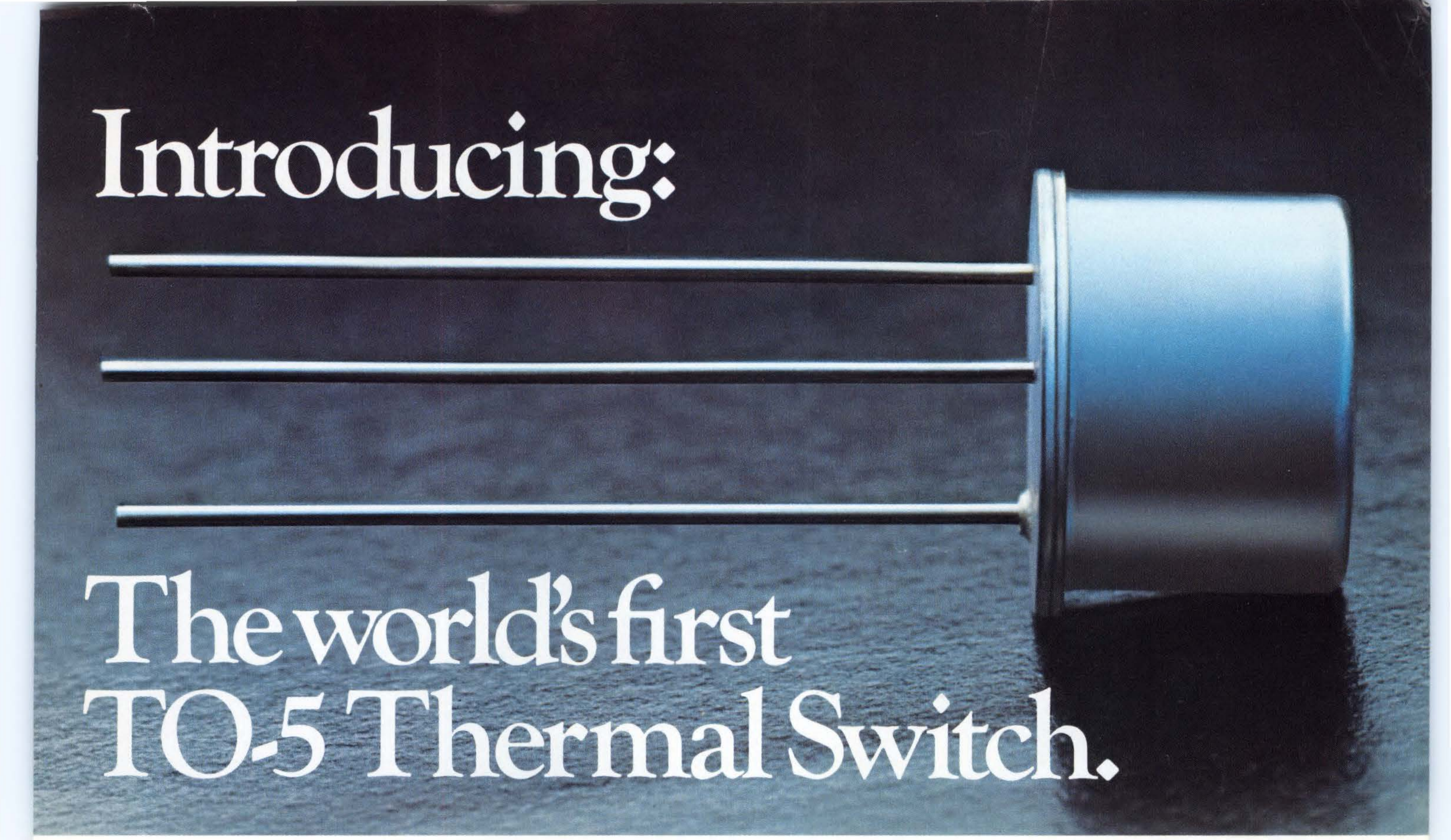
READER FEEDBACK

FSK Tones without Discontinuities"] will allow phase-continuous frequency-shift-keyed zones to be generated, but undesirable frequencies can still be produced during the transition from one frequency to the other. This can happen when the binary input is making a transition simultaneously with the load pin of the counter, a point at which an invalid binary number could be loaded. May I suggest that either the data should be synchronized with the load of the counters or the data input should be sampled and latched on the falling edge of the 74C193 clock.

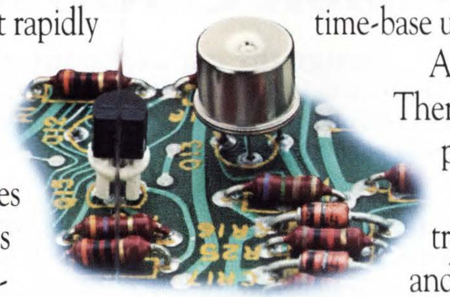
Richard Arndt
Stromberg-Carlson
Business Communications Systems
Maitland, Fla.

The author replies: *Mr. Arndt is absolutely correct in his recognition of a potential problem in my circuit, and his suggestion is an improvement.*

Although the probability of the data inputs' containing a false state coincident with the short load pulse (less than 1 μs) is low, his synchronizing scheme will eliminate it under most circumstances. The consequences of an incorrect load, should it occur, would last for only 1/16 of the period of the output pseudosinusoid but would have the effect of shortening or elongating that 1/16 period. In those cases where this is a potential problem, I would certainly recommend Mr. Arndt's solution.



The Elmwood 3600 Series TO-5 Thermal Switch provides a cost-efficient solution to solid state technology's most rapidly growing challenge – thermal density.



3600 Series Thermal Switches are SPST (Single-Pole, Single-Throw), bi-metallic, snap-action, thermal devices specifically developed for printed circuit board mounting.

Designed for logic level circuits, each quality-engineered thermal switch provides reliable temperature control insurance against damage caused by hazardous temperatures that can result from thermal density of components on PCB's, backplanes, flexible circuitry and sophisticated time-base units.

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As with all Elmwood quality-manufactured temperature controls, 3600 Series TO-5 Thermal Switches are manufactured of the finest materials and undergo rigid quality control procedures to live up to your highest performance expectations.

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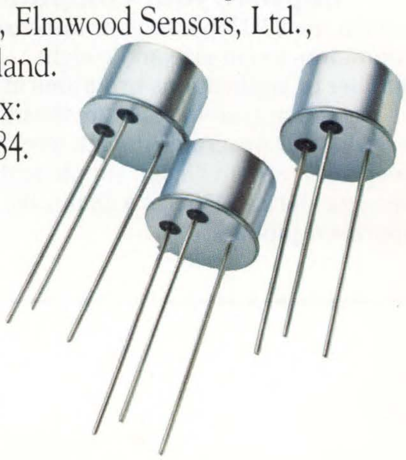

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CIRCLE 12

U.S. MEETINGS

Automated Test Equipment West Conference (ATE), Jan. 14–17. Anaheim Convention Center, Anaheim, Calif. Morgan-Grampian Expositions Group, 2 Park Ave., New York, N.Y. 10016; (212) 340-9780.

Caldon West '85, Jan. 14–17. Anaheim Convention Center, Anaheim, Calif. Morgan-Grampian Expositions Group, 2 Park Ave., New York, N.Y. 10016; (800) 782-0009.

1985 Measurement Science Conference, Jan. 17–18. Marriott Hotel, Santa Clara, Calif. Darlene Diven, Lockheed Missiles and Space Co., PO Box 3504, Sunnyvale, Calif. 94088; (408) 756-0270.

Uniform, Jan. 21–25. Infomart, Dallas, Texas. Pemco, Inc., 2400 E. Devon Ave., Suite 205, Des Plaines, Ill. 60018; (800) 323-5155.

Rf Technology Expo '85, Jan. 23–25. Disneyland Hotel, Anaheim, Calif. K. Kriner, Cardiff Publishing, 6530 S. Yosemite St., Englewood, Colo. 80111; (303) 694-1552.

1985 Society for Computer Simulation (SCS) Multiconference, Jan. 24–26. Bahia Hotel, San Diego, Calif. SCS, PO Box 2228, La Jolla, Calif. 94038; (619) 459-3888.

Communication Networks Conference and Exposition, Jan. 28–31. Washington Convention Center, Washington, D.C. Louise Myerow, CW/Conference Management Group, 375 Cochituate Road, PO Box 880, Farmingham, Mass. 01701; (617) 879-0700 or (800) 225-4698.

Mini/Micro West, Feb. 5–7. Anaheim Hilton Exposition Center, Anaheim, Calif. Electronics Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

Conference on Optical Fiber Communication(OFC '85), Feb. 11–13. Town and Country Hotel, San Diego, Calif. Optical Society of America, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.

IEEE International Solid-State Circuits Conference, Feb. 13–15. New York Hilton Hotel, New York, N.Y. Lewis Winner, ISSCC, 301 Almeria, Coral Gables, Fla. 33134; (305) 446-8393.

Integrated Machine Loading/Material Handling Systems Seminar, Feb. 19–21. Holiday Inn Livonia-West, Detroit, Mich. John R. McEachran, SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, Ext. 382.

Compcon Spring '85, Feb. 25-28. San Francisco, Calif. Linda Patterson, Compcon Spring '85, Lawrence Livermore National Laboratory, PO Box 808, MS L-72, Livermore, Calif. 94550; (415) 422-4260.

Automated Design and Engineering for Electronics Conference and Exhibition (ADEE), Feb 26–28. Anaheim Hilton and Towers, Anaheim, Calif. Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Ave., PO Box 5060, Des Plaines, Ill. 60018; (312) 299-9311.

Nepcon West '85, Feb. 26–28. Convention Center, Anaheim, Calif. Nepcon West '85, 1350 E Touhy Ave., Des Plaines, Ill. 60018; (312) 299-9311.

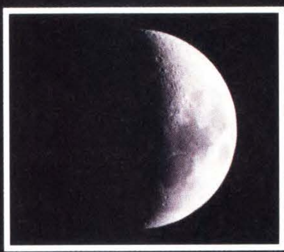
American Institute for Design and Drafting (AIDD) Exposition, March 3–8. Albert Thomas Convention Center, Houston, Texas. Philip Nowers, AIDD National Headquarters, 901 N. Washington St., Suite 509, Alexandria, Va. 22314; (703) 548-1263.

Interface '85, March 4–7. Georgia World Congress Center, Atlanta, Ga. The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

Southcon '85 and Mini/Micro Southeast, March 5–7. Georgia World Congress Center, Atlanta, Ga. Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

(continued on p. 21)

It works the night shift.



When you're working with ANVIS night vision goggles, you also want to be working with the new Vivisun 20/20 switches. A unique optics system eliminates the veiling glare and halo effect of conventional displays. When voltages are trimmed to night vision goggle flying levels, Vivisun 20/20 switches can still be read with the unaided eye.

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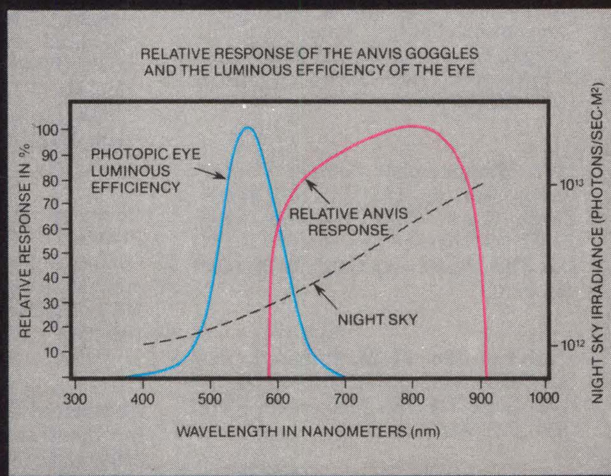

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CIRCLE 15

U.S. MEETINGS

(continued from p. 19)

Integrated Services Digital Networks Exposition (ISDN '85), March 6–8. Bally's Park Place Casino Hotel, Atlantic City, N.J. Joan Barry, Information Gatekeepers Inc., 214 Harvard Ave., Boston, Mass. 02134; (617) 232-3111.

National Design Engineering Show & ASME Conference, March 11–14. McCormick Place, Chicago, Ill. National Design Engineering Show, 999 Summer St., Stamford, Conn. 06905; (203) 964-8287.

1985 ACM 13th Annual Computer Science Conference (CSC), March 12–14. New Orleans Marriott Hotel, New Orleans, La. Della T. Bonnette, Computing & Information Services, University of Southwestern Louisiana, Lafayette, La. 70504; (318) 231-6306.

Picosecond Electronics and Optoelectronics Meeting, March 13–15. Hyatt Lake Tahoe, Incline Village, Nev. Optical Society of America, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.

International Computer and Telecommunications Conference (Comtel '85), March 18–20. Infomart, Dallas, Texas. Comtel '85, 5080 Spectrum Drive, Suite 707E, Box 17, Dallas, Texas 75248; (214) 631-6482.

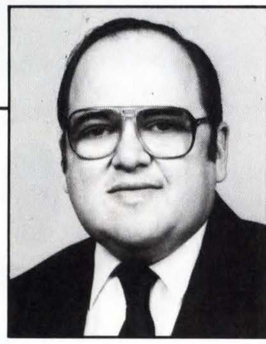
Robotic End Effectors: Design and Applications Seminar, March 19–20. Holiday Inn Livonia-West, Livonia (Detroit), Mich. John McEachram, SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, ext. 382.

Topical Meeting on Machine Vision, March 20-22. Lake Tahoe, Nev. Optical Society of America, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.

1985 Eastern Similation Conference (ESC), March 24–29. Williamsburg Hospitality House, Williamsburg, Va. Charles A. Pratt, SCS, PO Box 2228, La Jolla, Calif. 92038; (619) 459-3888.

Robotics and Automation, March 25–28. St. Louis, Mo. IEEE Computer Society, PO Box 639, Silver Spring, Md. 20901; (301) 589-8142.

PERSONALLY SPEAKING



What 1985 holds in store lays the groundwork for the next five years

In an industry characterized by a forever changing profile, making yearly predictions could be considered a chancy venture. Yet events occurring within the electronics industry this year will not only set the stage for the remainder of the decade but also reveal some clues to the next one. Since tradition prevails at this time of year, some soothsaying is in order.

- Bubble memories will be reborn, with 4-Mbit devices going into volume production and 16-Mbit ones on the horizon. Manufacturers have solved many problems that hindered the proliferation of bubble memories, and this year will see some new peripherals circuits such as increased compatibility with popular microcomputer buses.
- The introduction of a VLSI chip that can handle both floppy and Winchester disks will dramatically simplify the control electronics within disk drives. As a result, it will eliminate separate controller boards—each with 70 or so IC packages—for each drive type. Moreover, the new controller chip will be compatible with industry-standard interfaces.
- The VMEbus will seriously challenge Multibus II, as well as popular bus structures for 16- and 32-bit microcomputers. Part of the bus's strength will come from diverse support hardware, including new power supplies and data converter subsystems.
- Robotic systems will get a shot in the arm when a standard interface is agreed on for linking robots to their vision systems, programmable controllers, and other peripheral equipment. The interface—cosponsored by the Electronic Industries Association, the National Bureau of Standards, and the Robot Institute of America—will specify how various pieces of robotic equipment pass files and what form the data will take.
- The family of IBM PC personal computers, already setting de facto standards in hardware and software, will become a major force in integrated test and measurement systems. Tightly coupled to the computer, popular instruments will become essentially system-level peripherals. The arrangement will eliminate much redundancy in displays, user interfaces, and internal processing power. The integrated system will be able to test products, log and simulate data from multiple channels, and act as inexpensive controllers.
- Though system designers are eager to put their hands on 32-bit microprocessors, very few chips will be released in anything but sample form this year. The stumbling blocks include advanced CMOS processes, which have not yet been used widely in volume production, and the shortage of peripherals circuits such as memory management units.

With these predictions acting as stepping stones, the imagination can easily leap to the 1990s. Changes in memories, microprocessors, and peripherals will shape the next decade, filling it with sophisticated robots, artificially intelligent systems, and multiple-processor computers executing more than 100 million instructions a second.

Martin Gold

Martin Gold

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CIRCLE 19

NEWSPULSE

CMOS logic array cuts propagation delay to 25 ns

A CMOS programmable logic array with a minimum propagation delay of 25 ns—10 ns less than its bipolar equivalents—will soon be making its debut. The array, from Cypress Semiconductor Corp. (San Jose, Calif.), is based on a two-transistor UV EPROM cell in which one transistor is optimized for reading, the other for writing. Traditionally, EPROMs have used one transistor to tackle both tasks.

The cell's read transistor is roughly 1.5 times the size of its write transitor. Thus a larger signal is sent to a sense amplifier, enabling it to quickly determine the cell's state. Further, the smaller dimensions of the write transistor mean that a lower programming voltage is needed. The logic array is built with an n-well structure, one layer of metal, two layers of polysilicon, and 1.2–μm feature sizes. The array will be pin-compatible with Monolithic Memories' PAL-20 series and should be ready for sampling within a few months.

Special coating boosts coercivity on new-generation floppies

For the first time, coercivity on new-generation floppy disks has been virtually doubled—600 Oe, compared with the conventional 300 to 350 Oe on 5¼-in. disks—by using a proprietary cobalt-doped gamma-ferric oxide coating. Developed by Xidex Magnetics Inc. (Mountain View, Calif.), the coating makes it possible for 5¼-in.floppies to reach track densities of 96 tpi and a capacity of 1.2 Mbytes, and 3½-in. disks to hold 135 tpi and up to 1 Mbyte. Normally, lower coercivities precluded such capabilities.

Add-on board teams up IBM PC and Unix

One of the few boards to take advantage of National Semiconductor's 32000 chip family has added to the limited number of coprocessor cards that turn the IBM PC personal computer into a Unix workstation. The plug-in board, from Opus Systems (Los Altos, Calif.), carries the 32016 CPU, 32082 memory management unit, and 32081 floating-point processor. It runs the company's version of Unix System V and will be unveiled at Uniforum '85, which will be held in Dallas (Jan. 21–25).

Bonding display drivers to glass halves connections

One of the first techniques for directly mounting driver chips to the glass substrate of a dc plasma display cuts in half the number of connections typically associated with these units. Fewer links, of course, translate into greater reliability. In practice, the circuit traces are silk-screened onto the back of a glass panel, and the anode and cathode driver chips are directly bonded to it. Thus a circuit board is eliminated, along with the often touchy task of stringing leads from the board to the glass. The scheme has been put to work in a 224-by-480-line display from Dale Electronics Inc. (Columbus, Neb.). The unit, which stands 7.66 by 3.54 in., will be available in the spring. Prototypes will be released in February.

NEWSPULSE

Thick films stand in for copper in multilayer boards

Replacing most of the copper in multilayer pc boards with polymer thick films eliminates plated through-holes and lets passive components be printed as the layers are created. The scheme, devised by Dynacircuits Inc. (Franklin Park, Ill.), works with a single coating of copper as the board's base. Ten layers of circuit traces are then laid down with the thick films, or inks. These can be customized to exhibit a range of electrical and mechanical characteristics. They also create resistors, potentiometers, and edge connectors. Finally, sans much of the metal, the boards are lighter than their traditional kin.

IPI group looks to vary lengths of disk blocks and gaps

The American National Standards Committee's X3T9.3 working group is investigating recording formats that will allow its recently introduced—and widely acclaimed—Intelligent Peripherals Interface to handle variable-sized blocks and gaps. The approach lets controllers skip over defects in a disk's surface, a problem that will be encountered more frequently as bit densities increase and track widths narrow. The current IPI level 2 review document (BSR X3.130-198x) already specifies a format 0 for proprietary recording and a format 1 for fixed blocks and gaps. If adopted, the new recording scheme will become format 2. It will not affect the previously approved IPI physical interface. The subcommittee counts IBM, Control Data, Sperry, Century Data, and Xylogics among its members.

Continuous speech capabilities packed into 16 kbytes

A continuous speech board aimed at OEMs squeezes a speech-recognition vocabulary of 250 speaker-dependent words (or 20 speaker-independent words) plus voice response and store-and-forward capabilities into a mere 16 kbytes of memory. The board's speech buffer requires 2.3 to 3 kbytes of RAM for every 1.5 to 2 seconds of input. A proprietary speech algorithm is stored in ROM. The SSB 1000, from Audec Corp. (Saddle Brook, N.J.), uses a phonetic approach to recognize either isolated words or short phrases. Voice response is user-programmable.

OVER ACHIEVER.

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Outside, we gave our new 29B universal programmer a fresh coat of paint.

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The 29B's twenty-seven I/O formats enable you to interface with virtually every development system available. You can enjoy the ease of menu driven operation because the 29B's optional software driver allows you to interface with IBM®PCs. Yet, it's important to know the 29B is a completely self-sufficient system. So, if your needs don't require interfacing with a PC, the 29B can operate on its own.

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The 29B is just one example of Data I/O's commitment to giving you state of the art programming technology. And you can get it with the performance of 64k x 8 RAM for less than ever before. Like all our products, the 29B is backed by a worldwide network of field sales and service offices.

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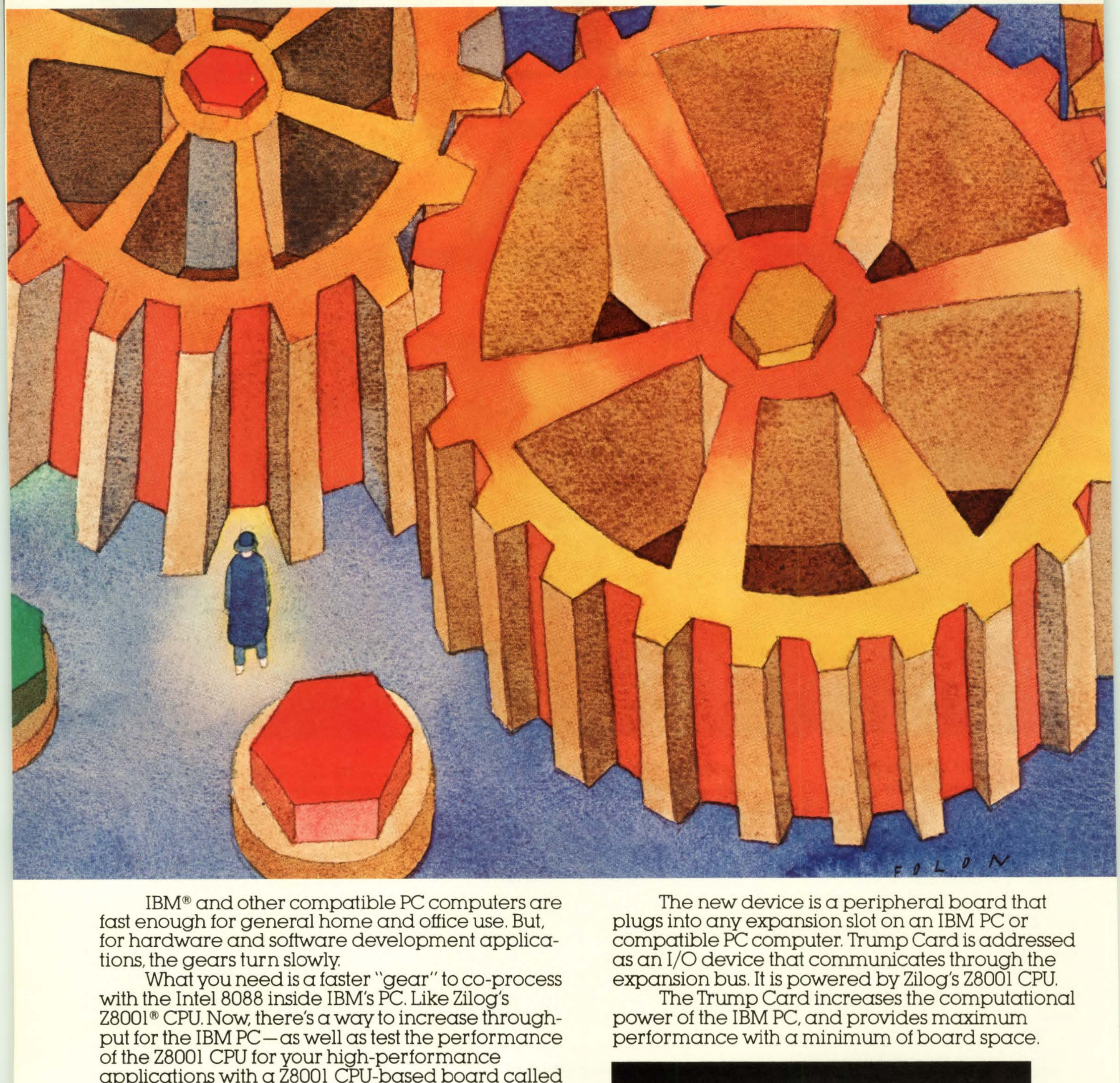
DATA I/O

CIRCLE 21

TURNING YOUR PC INTO A FASTER TOOL FOR MODERN TIMES.

This is the 3rd in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.

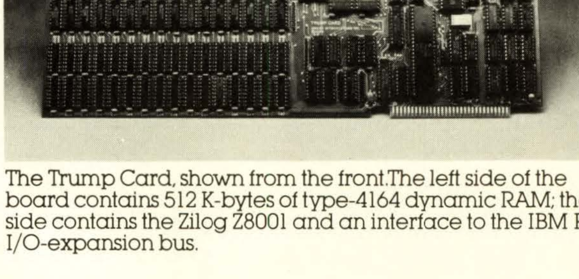


IBM® and other compatible PC computers are fast enough for general home and office use. But, for hardware and software development applications, the gears turn slowly.

What you need is a faster "gear" to co-process with the Intel 8088 inside IBM's PC. Like Zilog's Z8001® CPU. Now, there's a way to increase throughput for the IBM PC—as well as test the performance of the Z8001 CPU for your high-performance applications with a Z8001 CPU-based board called the "Trump Card" from Sweet Microsystems. And it proves dramatically how powerful Zilog's 16-bit CPU really is.

The new device is a peripheral board that plugs into any expansion slot on an IBM PC or compatible PC computer. Trump Card is addressed as an I/O device that communicates through the expansion bus. It is powered by Zilog's Z8001 CPU.

The Trump Card increases the computational power of the IBM PC, and provides maximum performance with a minimum of board space.



The Trump Card, shown from the front.The left side of the board contains 512 K-bytes of type-4164 dynamic RAM; the right side contains the Zilog Z8001 and an interface to the IBM PC I/O-expansion bus.

Z8001 COMPILER BASIC IS 80 TIMES FASTER THAN IBM INTERPRETIVE BASIC.

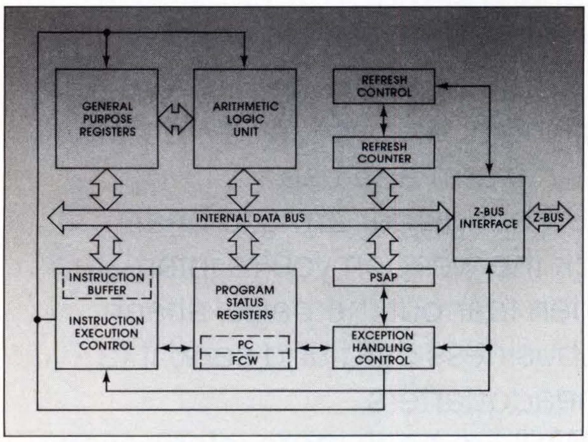
Essentially a monolithic minicomputer central processing unit, the Z8001 CPU is characterized by an instruction set more powerful than many minicomputers. As the programmer sees it, the Z8001 contains sixteen 16-bit general-purpose registers (for addresses or data) that may also be used in groups to form as many as eight 32-bit registers or four 64-bit registers. The low-order halves of the registers may be used for byte operations, thus the Z8001 CPU is able to manipulate data in 8-, 16-, 32-, and 64-bit pieces.

The Z8001 CPU, running at 10 MHz, can execute the same programs 4 to 10 times faster than the Intel 8088. What's more, the Z8001 CPU, with its large 8-megabyte memory range, makes the Trump Card's 512K bytes of memory easy to design with. (To use this memory in the card, you simply load a BASIC, CP/M-80, or C program from PC-DOS and type "RUN.")

Apple II	Apple III	TRS-80 Model II	IBM PC	IBM PC (with Trump Card)
224	222	189	190	2.4

A comparison of execution times (in seconds). Running on IBM's interpretive BASIC, a Sieve program takes 190 seconds to execute. Running the same program under TBASIC on the Trump Card Compiler takes only 2.4 seconds.

The eight addressing modes are register, indirect-register, direct-address, indexed, immediate, base-address, base-indexed, and relative-address. The instruction set utilizes data types ranging from single bits to a 32-bit long word. What's more, the processor executes 110 distinct instruction types that, when permuted by all the addressing modes and data types, create a set of more than 400 instructions.



A Z8000 CPU functional block diagram of the internal structure of the Zilog Z8000 family of high-performance microprocessors.

ALL THE PROPER SUPPORT FOR 512K BYTES OF MEMORY.

The wide range of software written for the Z8001 CPU is proven by all the programs you can run on the Trump Card. With the Z8001-based Trump Card, you can run the following software on your IBM or other compatible PC:

BASIC Compiler—TBASIC is PC BASICA-compatible. Most instructions are implemented without modification.

CP/M-80 Emulator—Allows you to run CP/M-80 Z80 assembly language programs directly. Just download your Z80 programs and run them.

C-Compiler—The industry standard version of C is available.

Debugger—Intended to aid in program development, you can examine and change memory and register contents and more.

Screen-editor—Has many word processing features, including ASCII text file development.

Multilevel Language Compiler—Allows Pascal-like control and data types, arithmetic expressions with automatic or specified allocations of registers, and more.

RAM Disk—Can allocate 128K to 387K bytes of on board memory to function as an intelligent RAM disk.

COPROCESSING IS JUST PART OF THE STORY.

The Z8001-based Trump Card is just one example of a successful application design for the Z8001 CPU. But there's far more to the Z8000 family than this.

Today, Z8000 CPU's are used in a wide range of applications, from industrial and medical products to computers and graphics imaging machines. And Zilog stands behind every application with service and software support that makes your Z8000-based products get to market on time.

Find out for yourself how much power Zilog packs into every Z8000 CPU by turning your IBM PC into a faster tool for modern times.

To get your own Trump Card and complete instructions, call Sweet Microsystems at (401) 461-0530.

For information about the Z8000 CPU, send for our complete overview or call our Literature Hot Line at 800-272-6560. For seminar dates and locations, or information on Zilog training, call 408-370-8091. Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.

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CIRCLE 22

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NEWSFRONT

One-chip μCs adopt off-the-shelf OS for real-time tasks

In just 368 bytes of program memory, a standard operating system handles task, time, and interrupt management functions.

Unlike nonprogrammable random logic, today's single-chip microcomputers need software, and OEMs generally spend a significant part of the design cycle creating it. Now, OEM designers can get a head start in product development with an operating system that manages tasks, priorities, and interrupts in real time. Even more important, it squeezes all those functions into a mere 368 bytes of program memory—well within the limited RAM found on single-chip microcomputers.

Single-chip microcomputers must handle both internal and external signals arriving at unpredictable intervals and respond to them as close to real time as possible. Thus, interrupts with microsecond reflexes are needed. At the same time, dedicated control functions are occurring in parallel, so multitasking—the concurrent operation of tasks—is a necessity.

Micro/OS-A, developed by Micro Computer Control Corp. (Hopewell, N.J.), sets up a priority-based, preemptive scheduling scheme for up to 16 concurrent tasks. It automatically allocates hardware resources to the highest-priority "ready" task, preempting any tasks with lower priorities. Ready tasks depend on the completion of time delays, interrupts from external or internal sources, or commands from other tasks. A preempted task is resumed whenever it again becomes the highest-priority ready task in the system.

A series of built-in service procedures gives the designer control over all tasks. With them, he can relocate task data structures in RAM, establish a basic system time unit, and create new tasks. Task synchronization and time delays are implemented with resume-and-wait procedures. Handlers activate interrupt flags, thus alleviating the need for user-developed interrupt source code.

The service procedures act as the intermediary between application-specific software and the control functions. They are accessed by call instructions.

For example, Set Address (SETADR) sets the RAM base address for task control blocks, allowing the system to adapt to available on-chip RAM. Another call, Create, is used to define a task with an assigned priority, starting address, and initial start-up time. Similarly, other calls set the system time units, suspend a calling task for a specified number of those units, and also reschedule waiting tasks.

The operating system, which is commercially available on disk or in EPROM, is fully tested and documented for the Intel 8048 and 8051 and the Zilog Z8 and is now being adapted to other popular microcomputer chips. Versions compatible with Isis and CP/M are now available in hexadecimal or binary object code under an OEM software license agreement.

Carole Patton

Configurable RAM cell boosts gate-array flexibility

A programmable array of RAM cell permits a gate array to be designed that incorporates various memory options, includes I/O cells, and leaves uncommitted a reasonably

NEWSFRONT

large number of logic gates. Though the resultant ECL array is not the first to blend logic and memory, it lets engineers set up dual-port interfaces, access RAM internally or externally, and vary the width of the data word.

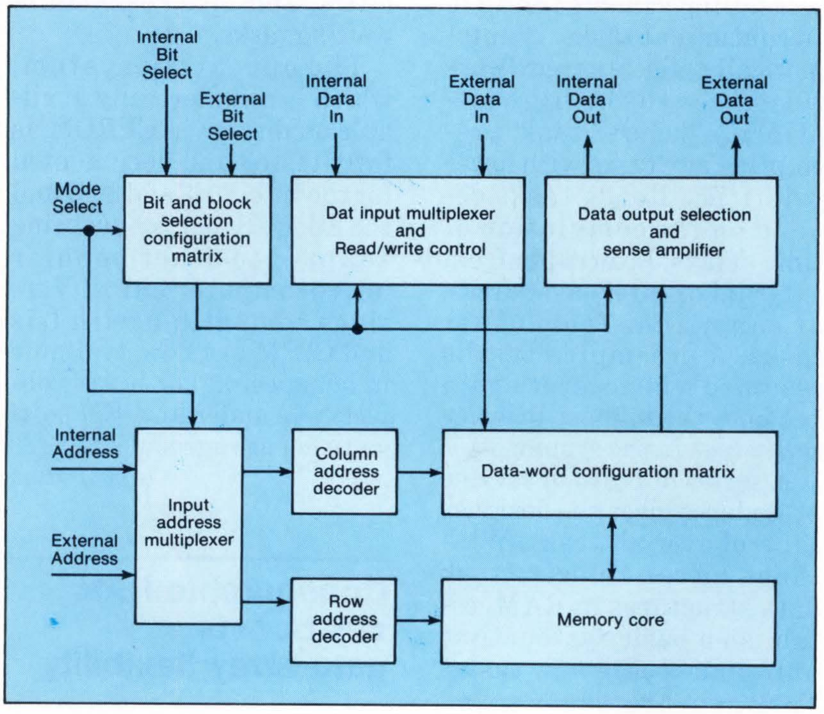
The array, under development at Applied Micro Circuits Corp. (San Diego, Calif.), consists of 1600 gates and 1280 bits of RAM. In addition, memory access times and gate propagation delays are adjustable—within limits and with tradeoffs in power dissipation.

The RAM contains a standard memory core divided into two 640-bit blocks. Normal row-address coding is used, but the column decoding and the number of I/O data ports are both variable. A data-word configuration matrix, which sets the number of bits in the word, allows the RAM to be tailored to any application (see the figure). Words of 4, 8, 16, 32, and 40 bits already exist as library macrocells, and others can be created.

The matrix makes it

The secret of the RAM's programmability is a configuration matrix that lets the output of each data column be ANDed with a column select line. Which select line is tied to each column is left to the designer and is established when the final metal mask is customized. At the same time, the outputs of the column AND gates are wire-ORed to the appropriate sense amplifier. Similarly, the data inputs are customized using the same procedure.

The control lines for selecting I/O bits can be blocked off in a variety of ways, allowing data words to be read or written in their entirety or in sections. Also, the matrix can be programmed to permit the RAM to be accessed through an external port—and that port does not have to be the same width as the word. Thus a host can, say, load or unload the RAM through a narrow port, while the internal array logic can be set up to process wide words.



To make the memory as flexible as possible, decoding logic is programmed during metalization. The logic determines the word width and the widths of the memory core's on- and off-chip interfaces.

Juggling the figures

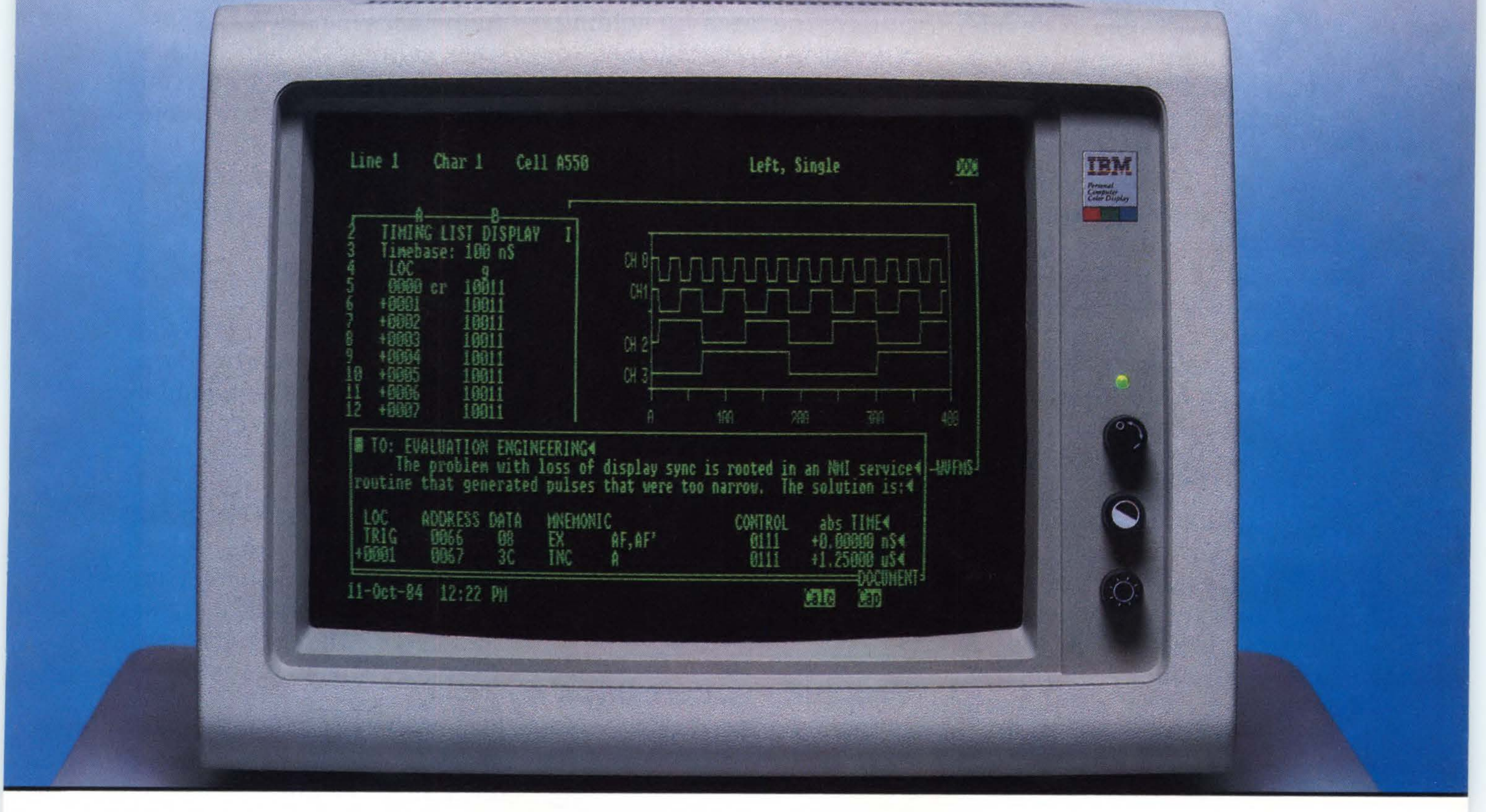
Further, designers can program the RAM cells and logic gates for various speed-power products to optimize critical paths and minimize overall power dissipation. The latter tops out at 4 W.

Finally, the RAM's access time can be adjusted from 6 to 8 ns (worst case over the commercial temperature range). The gate delays can be set from 0.28 to 0.7 ns.

The array will operate over the full military temperature range and has 104 universal I/O cells in addition to the gates and RAM. Those can be configured to link directly to TTL, ECL 10K and 100K, and mixed I/O systems.

Dave Bursky

Only our Logic Analysis Workstation can pass this screen test.



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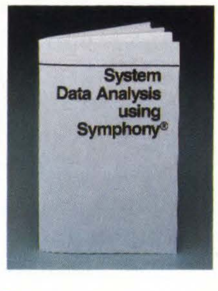

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CIRCLE 26

NEWSFRONT

CMOS process mingles high-quality analog, digital parts

A CMOS technique in the final stages of development lays down a wealth of high-speed, low-power analog and digital circuits on the same chip. Until now, most CMOS approaches delivered the goods for one or two high-performance elements but failed to meet the mark where others were concerned.

The technique, devised by Sierra Semiconductor Inc. (Sunnyvale, Calif.), creates 10-V analog circuits, EEPROM cells, switched-capacitor building blocks, and other circuitry on one piece of silicon. It goes with a modular approach of independent but compatible steps that speeds production and uses 3-μm features fabricated in an n-well bulk process.

Contributing factors

A single layer of metal and two of polysilicon form the interconnections. Late in the year, the company expects to drop chip geometry to 2 μm and add a second layer of metal.

To obtain the 10-V breakdown voltage for the analog elements and a 20-V on-chip generator for the EEPROM cells, a variant of a transistor with a lightly doped drain is employed. And a proprietary implementation sequence allows the structure to be created without extra mask steps.

To prevent latch-up—the nemesis of all CMOS circuits—guard rings are used around the transistors, components are carefully placed, and routing is handled judiciously. As an additional precaution, the latch-up holding current is characterized to make certain that the holding voltage is higher than the supply voltage.

The precision analog process should readily yield 12-bit analog-to-digital converters and high-quality switched-capacitor filters that meet the needs of 1200-baud modems and dual-tone multifrequency decoders. On the digital side, gate delays of just 2 to 4 ns are possible, and the EEPROM cells should make reconfigurable logic a snap.

Dave Bursky

Graphics accelerator cruises along at 400,000 operations/s

A dedicated bit-slice processor, multiple bus structure, and heavily pipelined system architecture give an add-on graphics accelerator the power to plow through 400,000 clipping operations and transformations a second. That is about 2 to 4 times faster than most graphics display systems—speedy enough to manipulate images almost instantaneously.

Developed by Cadnetix Corp. (Boulder, Colo.) for its family of workstations (ELECTRONIC DESIGN, Nov. 15, p. 169), the accelerator employs a microcoded graphics processor with an 88-bit-wide writable control store and pipelined register. Its pipelined architecture tackles as many tasks in parallel as possible, coming through with a cycle time of just 120 ns. And sometime in 1985, the cycle time will be cut by 20 ns, delivering an accelerator that processes 500,000 transformations a second.

Half and half

About half of the bits in the microcoded word control data manipulation; the rest handle such housekeeping functions as generating addresses controlling jumps, and the like.

The graphics processor actually comprises two subprocessors (see the figure). One subprocessor is made up of a 16-bit ALU, 16-bit multiplier, a register file, and auxiliary memory used for stack space and constant look-up. The second consists of what the company calls a system memory access machine—a block that oversees fetching primitives from the main system memory.

Dual-ported memory

To generate the 1024-by-800-pixel, 64-color bit-mapped display, the graphics display generator also contains a controller that is similar to the system memory access machine. It pulls information from the system and shifts data words into a local memory built from dual-port TMS 4161 dynamic RAMs. Each of the six planes

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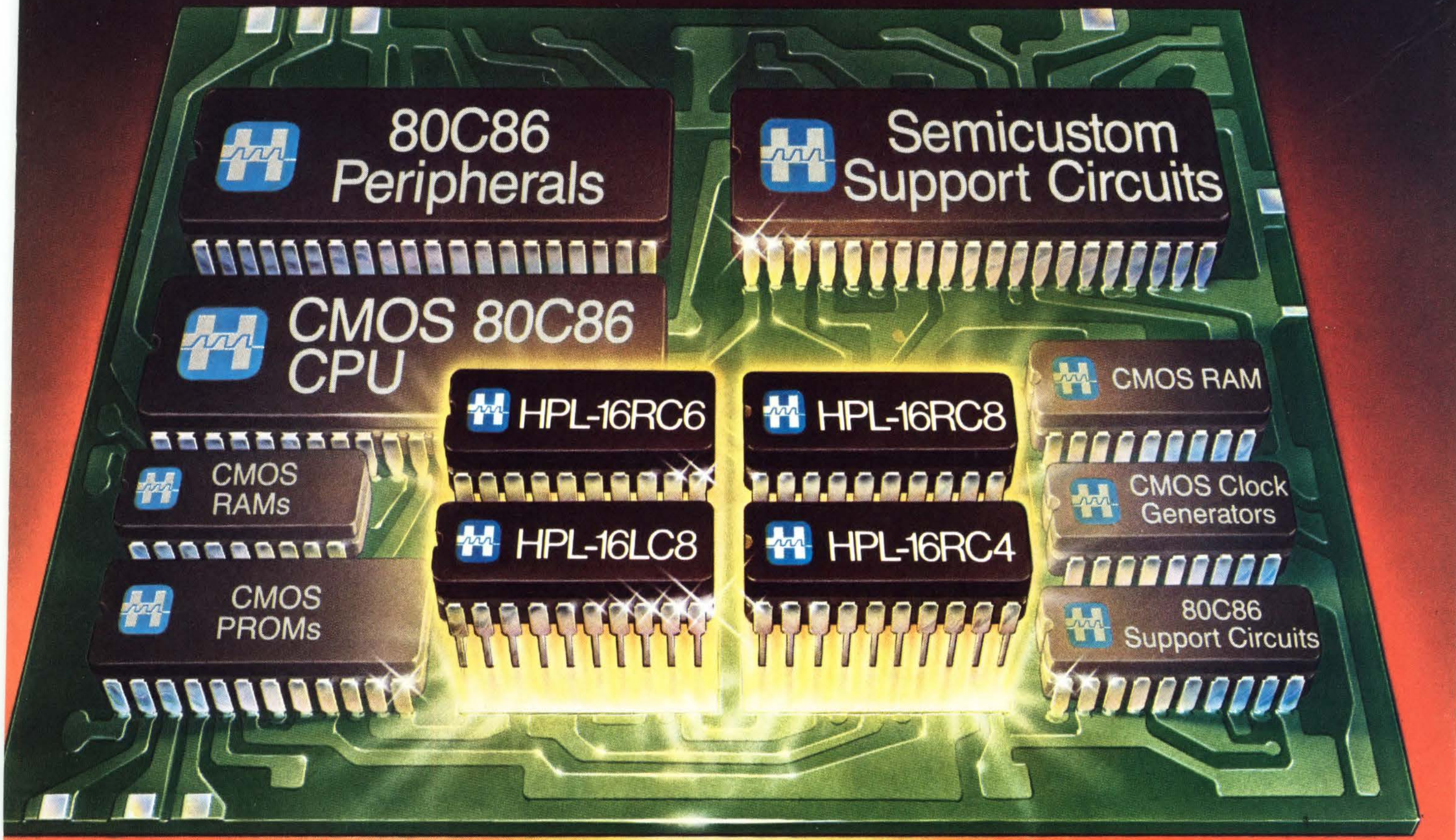

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HPL-16RC4*	Replaces 16R4, 16RP4	5 mA/MHz	
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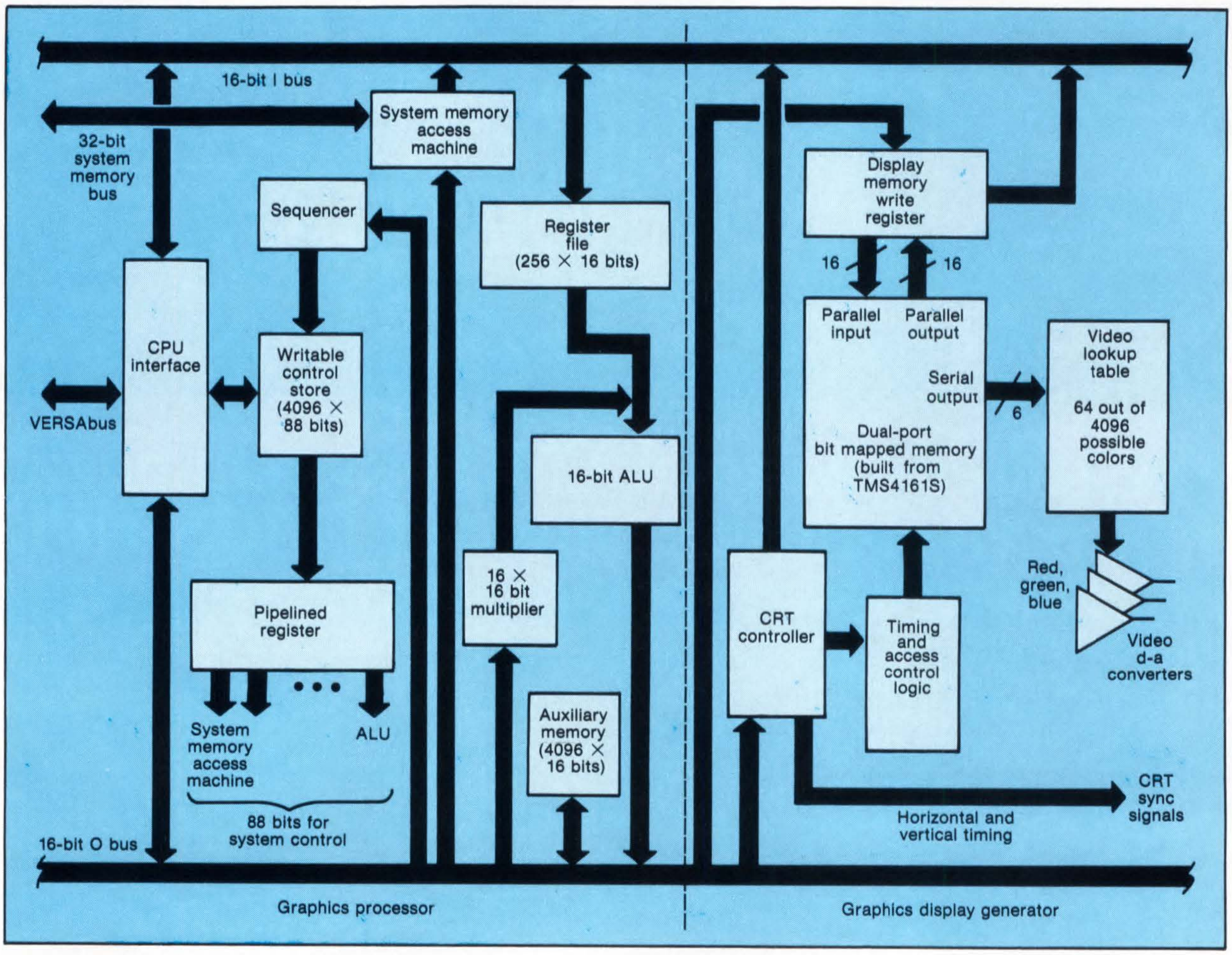
of the bit-mapped memory is organized as 64 kwords of 16 bits each.

The dual-port dynamic RAM makes the memory subsystem available to the overall system 95% of the time, in turn making for very rapid screen updating. And as mentioned, a number of operations are handled in parallel. For example, all features of a vector can be loaded, and writing to the screen can take place independently of the CPU—just supply the starting location, angle, color and begin. *Dave Bursky*

Software front end links Lisp machines to industrial world

System designers generally consider Lisp machines most appropriate for developing software,



An internally pipelined multiprocessor and multiple-bus architecture helps the graphics and display subsystem of a graphics accelerator handle 400,000 clipping operations and transformations each second. At that speed, images can be manipulated almost instantaneously.

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Slew Rate	4V/μs	4V/μs	20V/μs	20V/μs
Bandwidth	8 MHz	8 MHz	60 MHz*	60 MHz*
Voltage Noise	4.3 nV/$\sqrt{\text{Hz}}$	4.3 nV/$\sqrt{\text{Hz}}$	4.3 nV/$\sqrt{\text{Hz}}$	4.3 nV/$\sqrt{\text{Hz}}$

*Uncompensated (Minimum closed loop gain of 10)

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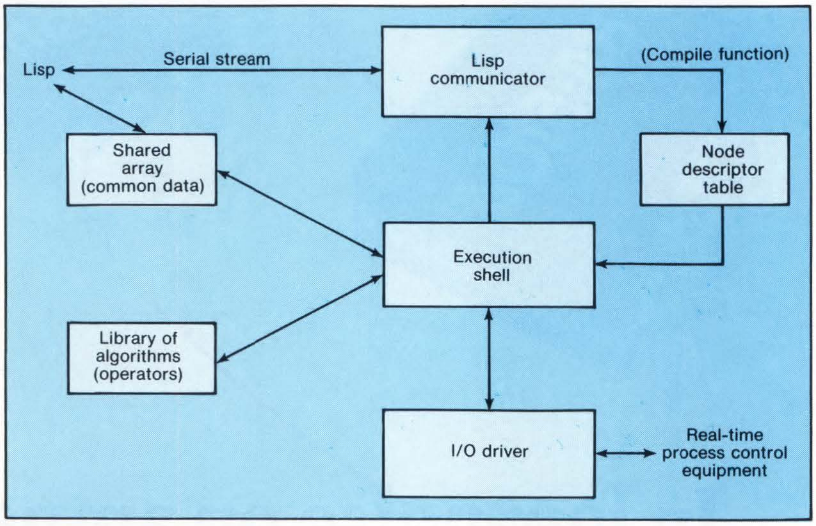
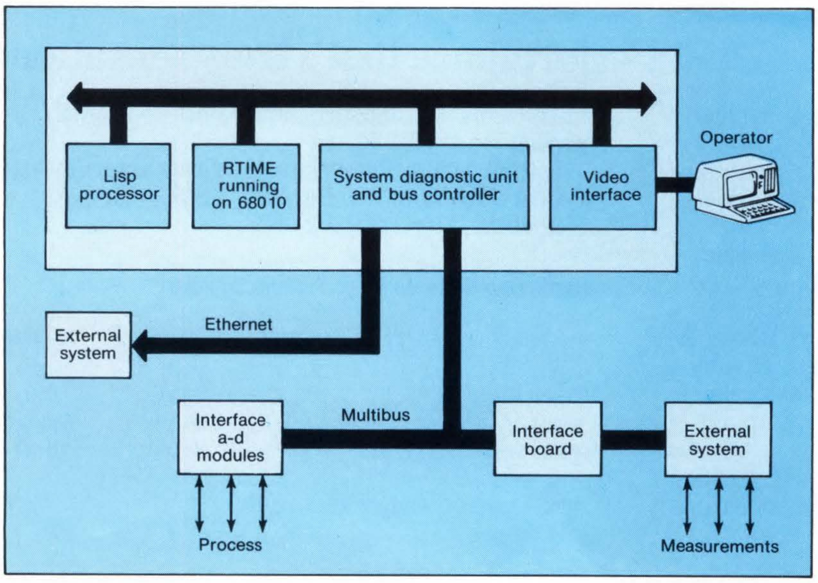
conducting research, and creating expert systems. Rarely, however, do they think of them for real-time process control. Those views will undoubtedly change when a front-end software package puts the control of real-time industrial systems in the hands of the user.

RTIME, as the package is called, acquires external data and, at timed intervals, processes it for transmission to a host processor. The user programs the front-end package, developed by Lisp Machines Inc. (Culver City, Calif.) for its Lambda system, through a Lisp processor by defining the nodes—that is, the points of processing—and the programs for them.



1. A front-end package adds real-time capabilities to a Lisp-based system through a communicator, an execution shell, and an I/O driver. Each processing point, or node, is listed within a descriptor table, and a library of algorithms contains the C code for the system's basic operators.



2. RTIME is designed to run on a 68010 coprocessor, which is part of the Lambda machine. It allows users to program real-world events in Lisp. The package interfaces with sensors and process controllers through the Multibus, with a host system through Ethernet.

A peek inside

The internal structure of the front end is key to its operation (Fig. 1). One portion, the Lisp communicator, is actually the receiving and transmitting point for data flowing between the host and the front end. It also prepares the node for the execution shell, another section of the front end.

The shell scans RTIME's node descriptor table and schedules nodes for immediate processing or, if they are awaiting incoming data, for a read-wait state. The final part of the front end, the I/O driver, handles the real-time communication with external equipment. A standard driver is supplied for Ethernet, as are tools for creating Multibus-compatible drivers.

Each program in RTIME is compiled into a set of code pointers, which refer to defined blocks of operator code within a library. Reminiscent of the earlier Fortran compilers and Forth systems, that "threaded" code minimizes system overhead.

Familiar concepts

Each node consists of an index, a name, timing data, and a function. The last of those is a program made up of predefined operators, including as-

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signments (+, −, *, log, and so on), special processing operators (lag, delay, rate), and program constructs like "If... then" and "If... alert." The latter construct notifies the host of real time conditions through software interrupts.

The front-end software runs on a 68010, which acts as a coprocessor within the Lambda system (Fig. 2). Lisp Machines plans to adopt the software for Picon, an expert system that will be able to advise operators of process control equipment in real time. Currently RTIME runs under Unix 4.2 BSD, but soon it will be running under its own operating system, thereby cutting processing overhead.

Ray Weiss

Channelless cells optimize silicon use in semicustom chips

Semicustom circuits have obvious advantages, but rarely can they match the economical silicon use of hand-crafted designs. A compact layout is a touch goal to reach with gate arrays and even with standard cells. Now, however, a standard-cell technique draws on an unusual channelless structure, developed last year for gate arrays, to eliminate dedicated wiring channels.

Each standard cell is designed with a fixed height and width, but its internal metal connections can be varied, depending on the desired circuit layout. That feature is the strongest contributor to the cell's high wiring density: As with the channelless gate array, wires can be routed through the standard cells instead of filling dedicated channels surrounding them, as is common with most standard cells.

Developed by California Devices Inc. (San Jose, Calif.), the standard cells are fabricated with a 3-μm CMOS process that employs two layers of metal. The basic cell consists of transistor pairs whose geometries are the same for every cell—a factor that simplifies circuit simulation.

Building a chip

With support software, the designers can create a chip containing about 10,000 gates, piecing together blocks of 2000 to 3000 gates. Automatic placement and routing software can handle standard-cell blocks of various sizes and shapes, and a congestion analysis routine helps maximize the circuit density (see the figure).

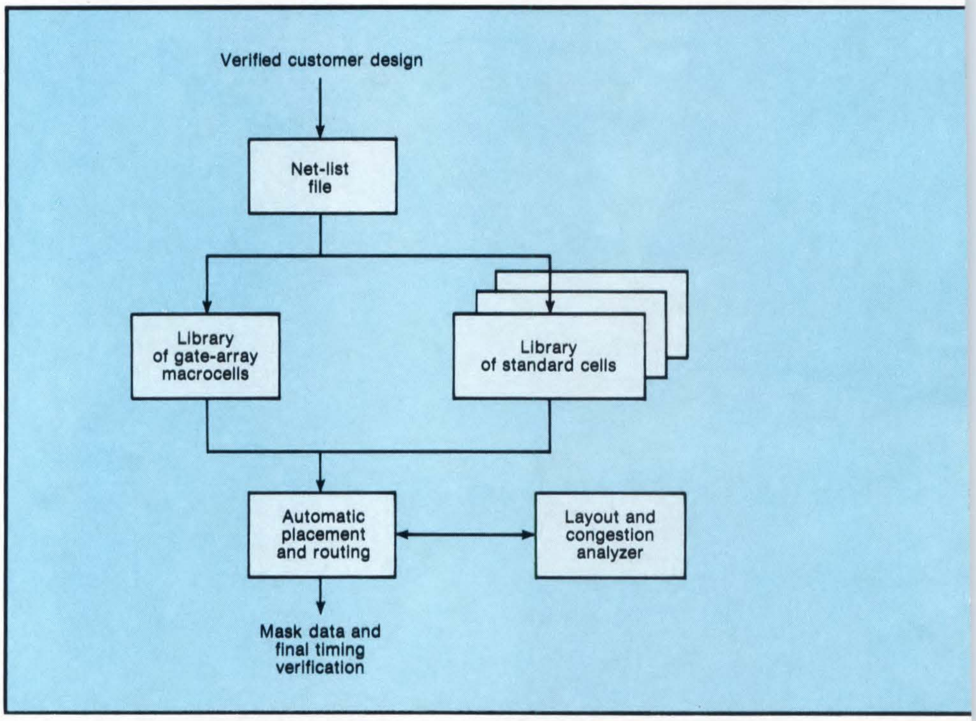
Once the user has captured a design and filed a net list, software chooses either the channelless gate array for quick turnaround or a standard cell for more customized circuitry.

Novel traits

Supercells—ROMs, RAMs, and programmable logic arrays—will be the first members of the family. The PLA supercell, for instance, has an unusual set of characteristics: It can be configured by

the user and programmed, through metal interconnections, as either a PLA or a ROM. A special option permits the user to set up a double-ended structure so that the array can be entered from either end. That alone translates into significant reductions in signal routing and thus a trimmer chip.

Supplementing the supercells, which will be introduced this spring, are the earlier members of California Devices' gate array library. Custom I/O cells will be added later this year. *Dave Bursky*



Software makes the best choice between standard cells and gate arrays once a circuit's net list has been created. In either case, the designer gets the benefits of a channelless structure, which yields dense wiring and thus extremely compact chips.

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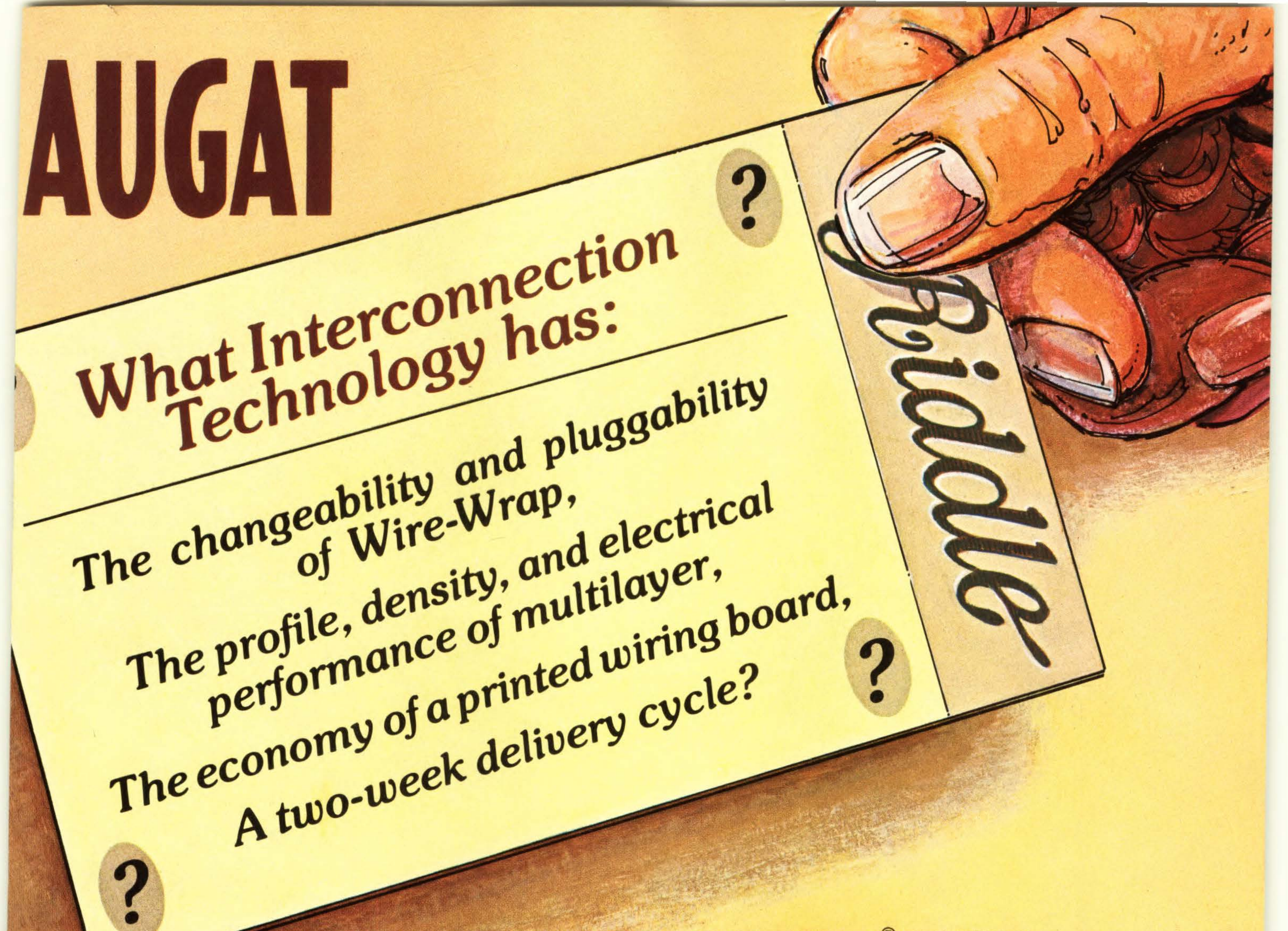

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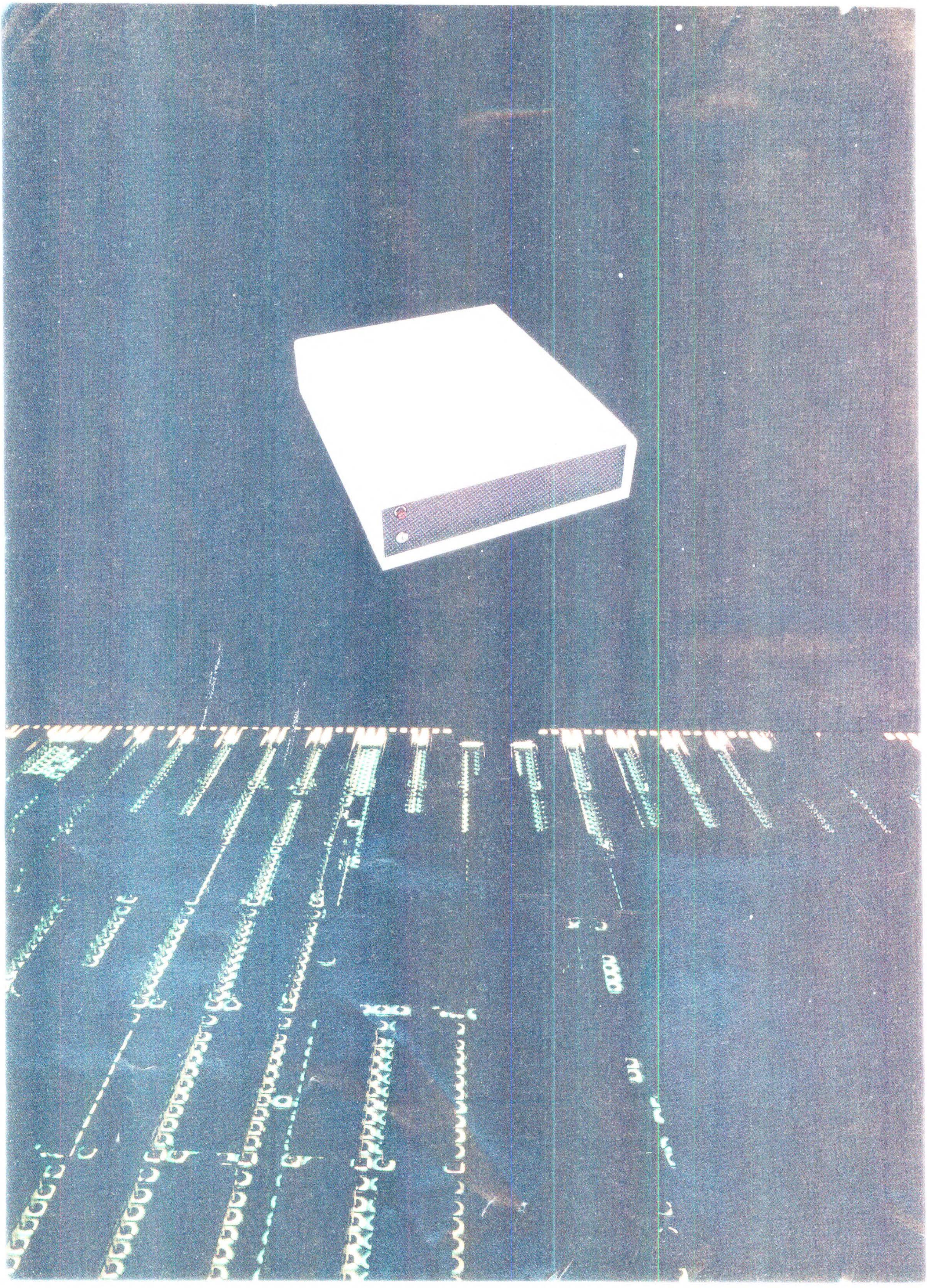

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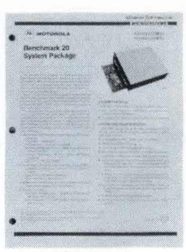

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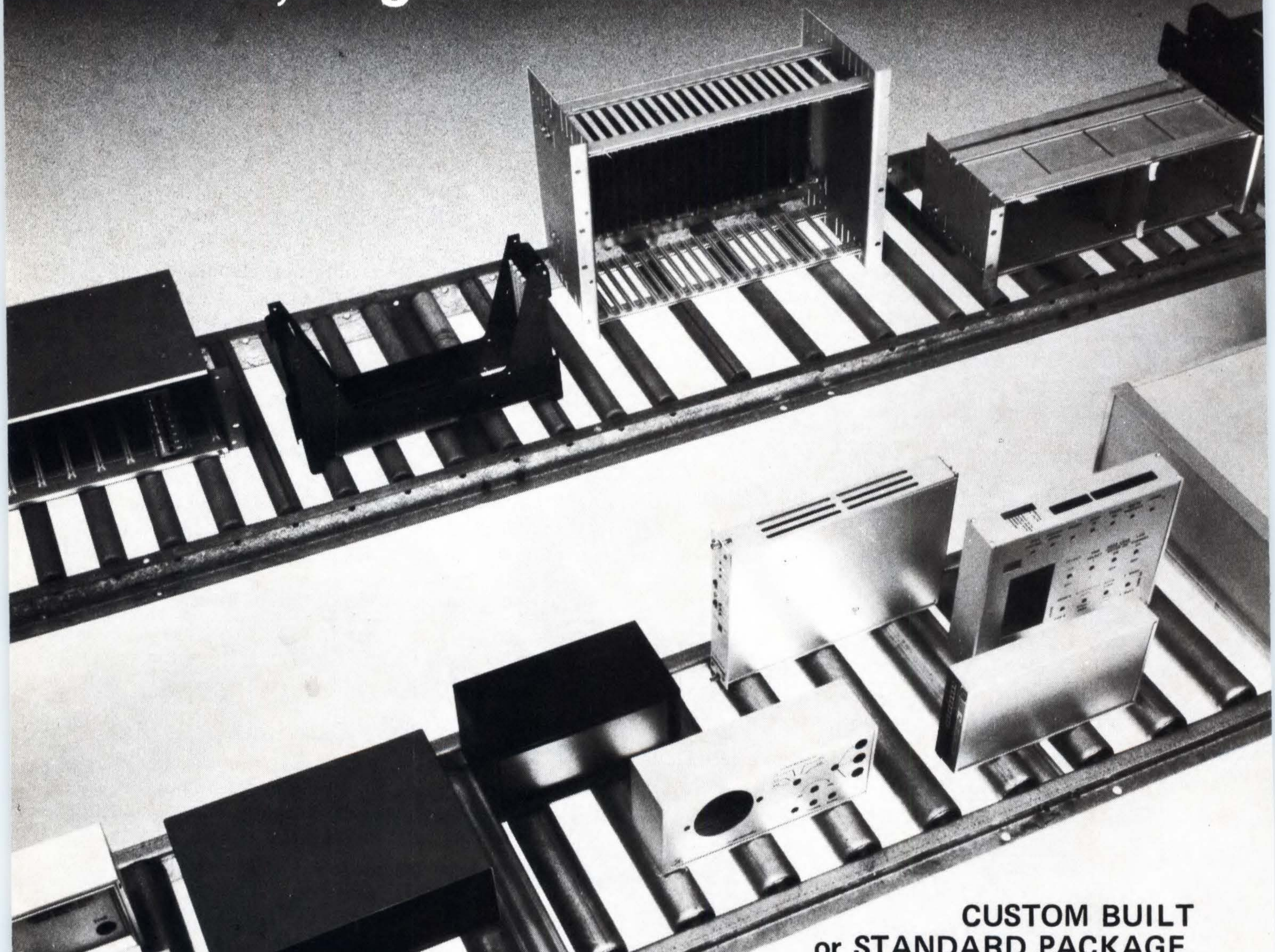


CONFERENCE PREVIEW

New languages and techniques drive advances in simulation

When a conference on computer simulation gets into gear, concurrent Prolog, time warping, and graphics will take the lead.

Software and systems with the potential to extend the power of simulation will be the prime focus at 1985's Society for Computer Simulation Conference (San Diego, Calif., Jan. 24-26). Developments for simulation in Prolog, graphics, and distributed systems will come under scrutiny as well.

Prolog, the centerpiece artificial intelligence language of the Japanese fifth-generation system, holds a great deal of promise for discrete event simulation. A high-level, machine-independent language, it treats data and program material the same; has logical, declarative semantics; and offers flexibility in the binding of variables to procedures.

Beyond rules

Prolog has much power beyond factual statements and "if... then" rules. Recursion, backtracking, and a database search mechanism are among its other capabilities. For simulation, time can be added as a variable in the statements and updated in discrete increments. However, for large simulations the speed of Prolog becomes a problem.

At the present time, work in the Prolog field is concentrated in two major areas: concurrency—that is, a nonsequential, parallel version (ELECTRONIC DESIGN, Dec. 13, 1984, p. 73) that increases execution speed—and the addition of features such as interprocess communication and time handled for process simulation.

One approach was tried at the Hungarian Institute for Coordination of Computer Technologies (Budapest), where M-Prolog was developed. A concurrent version based on M-Prolog called TS-Prolog breaks down a simulation into component processes. Predicates were built in to define components and set up communication channels between them. Only one process or component is active at a time. In the case of failure or deadlock, backtracking is invoked and another solution is found.

Additional built-in predicates were added to create processes, handle communication mechanisms, and introduce time as a factor in the simulation.

Another type of concurrent Prolog simulation is being developed in Japan under MITI's watchful eye. It achieves parallelism by refusing to allow backtracking. T-CP, a variation of concurrent Prolog, has been developed by researchers at the University of Calgary (Alberta, Canada). It uses delay or time expressions and takes the form:

```
A  :- G1 . . . Gn   <:delay:>
          B1 . . . Bk
```

Clause A is true if the guard clauses G1 . . . Gn and clauses B1 . . . Bk are true and the delay time has passed. The guard clauses precheck B1 . . . Bk and are checked concurrently against possible solutions. Each sentence is a process with a delay time for its simulated action.

One very interesting software technique for simulation is the time warp mechanism. Developed by Rand Corp. (Santa Monica, Calif.) under Air Force funding, it ingeniously simulates distributed discrete events by utilizing the concepts of messages, antimessages, annihilation, and roll-back.

To use the mechanism, a simulation is decomposed into a collection of interacting processes or objects. Each ob-

CONFERENCE PREVIEW

ject keeps its own time, referred to as local virtual time (LVT). The objects interact with one another by sending event messages that are time-stamped with the sending object's LVT and the receiving object's execution LVT.

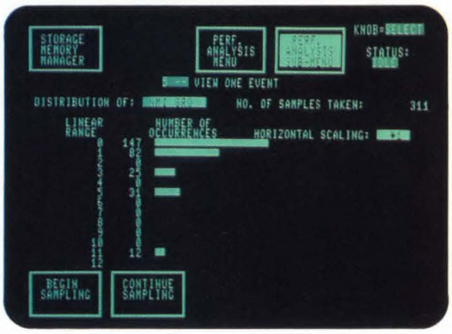
Each object will charge ahead and execute its portion of the simulation. Event messages are interchanged between objects for coordination. The received event messages are placed in a queue and executed in time-stamp order, with each object periodically checkpointing its processing and saving the state information.

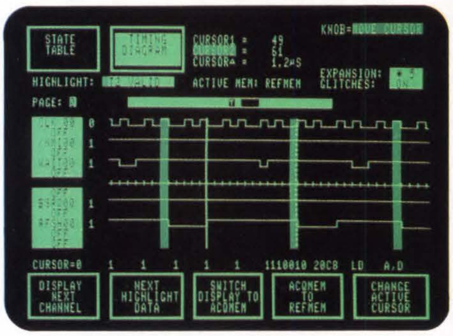
The time warp mechanism can set a large number of processes in motion that are coordinated by interchanged messages. If the messages are delayed or a later message cancels an earlier message, the object out of sync can simply roll back to an earlier event and resume processing. Furthermore, a message placed in queue or executed earlier can be canceled by sending its antimessage to the object. In effect, the mechanism embodies a kind of optimistic risk taking, judging that it is better to execute now than halt and wait for a cooperating process to catch up. One interesting side effect of this approach is that it never reaches a deadlock —it will always roll back for another try under different conditions.

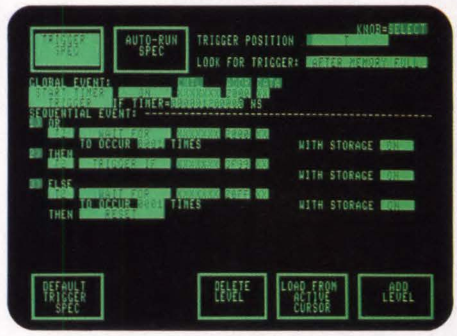
Graphics animation has proved to be effective for the simulation of distributed processes. The University of Calgary's Mona was developed on the Jade distribution prototyping system as a tool for the animation of message interactions between concurrent processes. Each system is assigned its own icon, and processes within that system use that shape. Interaction among communicating processes in dissimilar systems can be displayed simultaneously on a single CRT, providing a tool for distributed processing debugging.

Ray Weiss

THE DIFFERENCE BETWEEN NIGHT AND DAY.







1 No other logic analyzer lets you clearly see what your hardware and software are doing at the same time.

Only a correlated dual timebase allows true interaction analysis. Only Tek has it.

As your digital designs become more complex and you subdivide your design, only the 1240 lets you obtain an accurate picture of real-time interactions between independently-clocked modules.

By defining triggers based on the data from both time bases, you can easily monitor the interaction between hardware and software or the relationship of two dual processors—with information displayed in a time-aligned manner.

Stark contrast to the jumble of data or jerry-built clocking by any other system of acquisition.

2 No other logic analyzer offers such complete performance analysis. For software. And for the entire system.

By combining its dual timebase with the high-resolution, 10ns timing you need to look at hardware events, the 1240 adds a new, more powerful dimension to performance analysis: complete systems analysis.

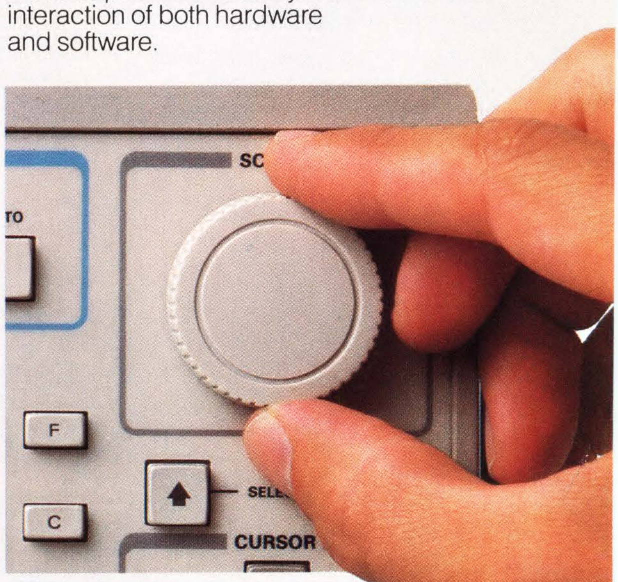
In software analysis alone, the 1240's multilevel trigger takes you well beyond the limited, continuous event analysis of other logic analyzers. Want to look at time spent in multiple interrupts during execution of a software module? Only the 1240 can measure, compare and graph the event distributions.

3 Only the Tek 1240 offers so much triggering capability for both hardware and software analysis.

For software analysis, the 1240 combines 14 levels of conditional triggering with data flow and program flow qualification. You can pinpoint where your software went wrong right away. Without wading through mountains of data.

For hardware analysis, counters, timers and duration filters allow you to quickly locate problems that result from the time characteristics—as well as the state—of the hardware.

Moreover, only the 1240's dual timebase lets you combine all these capabilities to analyze the interaction of both hardware and software.



4 Every logic analyzer claims to be easy. Only the 1240 is as easy as you want it to be.

Easy is no bargain if it comes at the expense of performance. So the 1240 lets you select from four distinct levels of operation, adding more advanced features only as your design challenges require.

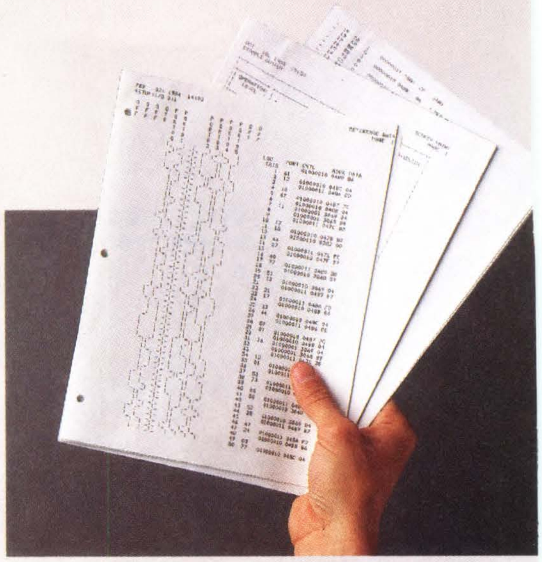
Other user conveniences are obvious at first glance: the unique touch display lets you select menu items without ever taking your eyes off the screen. Keystrokes are minimal and logical. And, proving that buttons aren't always the best answer, the smooth, flicker-free scrolling of the big front panel knob proves to be one of the 1240's most pleasing user features.

(Continued next page)

5 No other logic analyzer is as modular, expandable or versatile, to keep your costs low and compromises few.

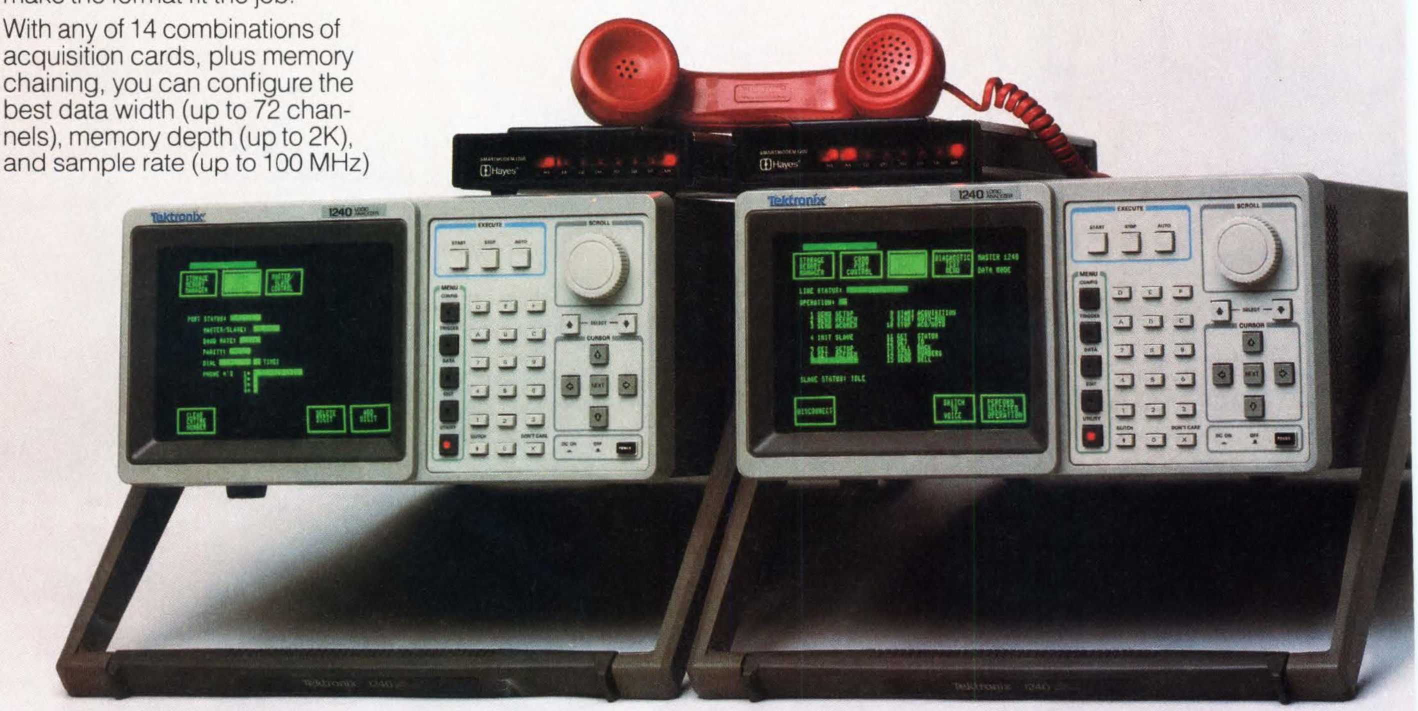
No competition here. The 1240 supports all major microprocessors. It includes three types of disassembly, so you can make the format fit the job.

With any of 14 combinations of acquisition cards, plus memory chaining, you can configure the best data width (up to 72 channels), memory depth (up to 2K), and sample rate (up to 100 MHz) for each application. You can add ROM Packs for data analysis; RAM Packs for data storage; COMM Packs for various RS-232 and GPIB communications environments, including a wide range of printer support; and a master/slave capability that makes teleservicing eminently practical by allowing two 1240's to communicate via phone lines.



In black-and-white, the 1240 is your best guarantee that problems will never evolve beyond what your logic analyzer can handle.

For more reasons, on-paper or in a personal demonstration, why the 1240 is the best of the best-selling logic analyzers, call 1-800-547-1512. In Oregon, call 1-800-452-1877. Or contact your local Tektronix Sales Engineer.



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NEWS ANALYSIS

Makers of semicustom ICs greet bit-slice devices and μPs with open arms

Builders of standard cells and gate arrays turn to microprocessors and bit-slice cores to cram computer systems on a chip.

Semicustom technology has advanced to the point that chip manufacturers can now supply functional blocks that emulate processors. These blocks—incorporated with existing semicustom memories and proprietary circuits—squeeze what is essentially an entire computer system onto a single chip, slashing size while keeping a lid on cost.

Generally, standard-cell libraries are seizing on microprocessors as their mainstays, and their gate-array counterparts are looking mostly to bit-slice processors. In both technologies, though, viewing processors as core elements is becoming increasingly common.

Interest running high

The interest in incorporating these complex blocks into standard-cell libraries is running so high that at least one company, National Semiconductor Corp. (Santa Clara, Calif.), not only intends to add a processor to its library, but also is planning semicustom spin-offs for all processors now entering the design cycle. Indeed, it has the same intention for all of its new components.

One of the most common reasons for semicustom IC manufacturers' preoccupation with processors is the reduced size that comes with combining control circuitry and custom memory configurations, I/O, and other proprietary circuits. Equally important, but less obvious, is the boost in speed that comes with the drop in external accesses inherent to the approach. Finally, the finished chip is more difficult to reverse-engineer, since there are fewer I/O pins.

One microprocessor core intended for standard-cell designs is a CMOS version of the 6502. Compatible with existing NMOS parts, the device adds 14 instructions to the standard set. (These instructions control standby and sleep modes, as well as other functions specific to CMOS.)

The cell, from NCR Corp.'s Microelectronics Division (Fort Collins, Colo.), is built with 3-μm design rules and is roughly 13,000 mils^2. It is small enough that a variety of other circuits can be built alongside it without making a chip so large that its cost would be prohibitive. For example, one chip, about 50,000 mils^2, weds the cells to 3 kbytes of ROM, 64 bytes of RAM, a timer, and other proprietary logic circuits (Fig. 1).

The 8085 is the cornerstone of another standard-cell library. Fabricated in CMOS and using 3-μm design rules, the processor is expected to come in at about 37,000 mils^2 when it becomes available later this year. Like NCR's 6502, the circuit, from Calmos Systems Inc. (Kanata, Ont., Canada) maintains compatibility with existing components but adds to the regular instruction set.

With RAM on board

Another standard-cell manufacturer takes a slightly different tack, featuring an 8049 processor cell that carries 128 bytes of RAM and 2 kbytes of ROM. Designed by Zymos Corp. (Sunnyvale, Calif.) and built with 2.8-μm rules, the entire cell takes up about 40,000 mils^2. To simplify testing (which can be difficult since the processor does not have the customary I/O pins), the company has built in a test port through which pregenerated programs can be run.

Though most standard-cell libraries are built around microprocessors, one was just

NEWS ANALYSIS

unveiled that centers on a bit-slice processor. It is also one of the first to incorporate EPROM.

A well-stacked library

The CMOS library, from Wafer Scale Integration Inc. (Fremont, Calif.), uses 2-μm technology, allowing multiple processors to be shoehorned on a chip to increase speed or bus width. A single bit-slice processor matches the performance of a bipolar bit-slice chip; four processors combined on a chip with carry and look-ahead circuitry will run 5% to 8% faster than the same circuit built using discrete bipolar chips—with an attendant reduction in power.

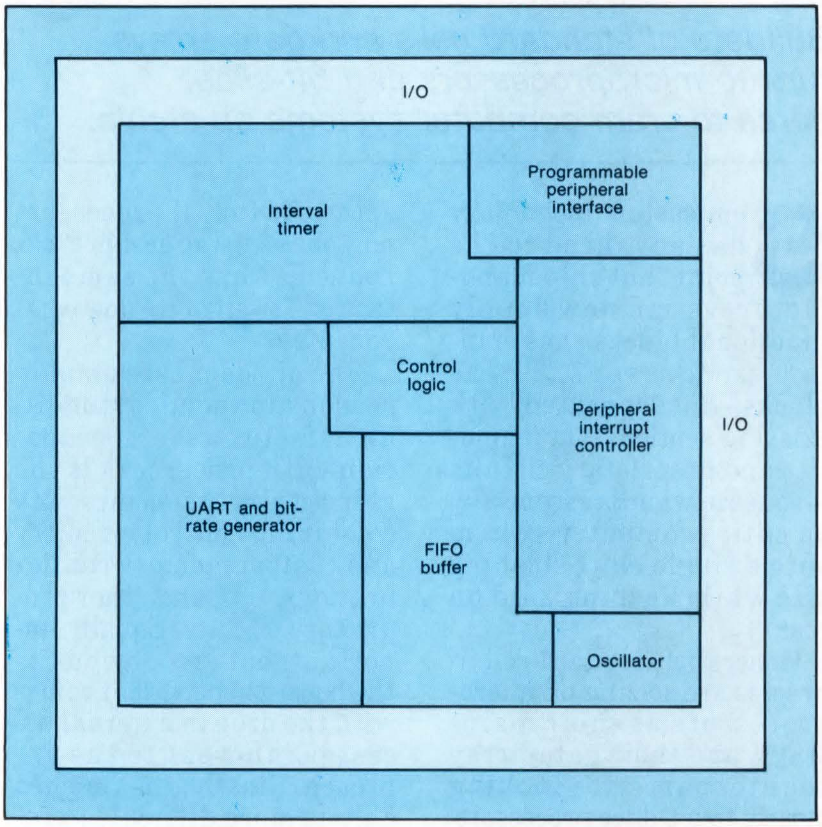
Although performance is the library's strong suit, it is also relatively flexible and compact. A 4-bit-slice processor can be placed on a single die (57,600 mils^2) with a sequencer, carry and look-ahead logic, status and shift registers, and 20 kbits of EPROM.

For controllers too

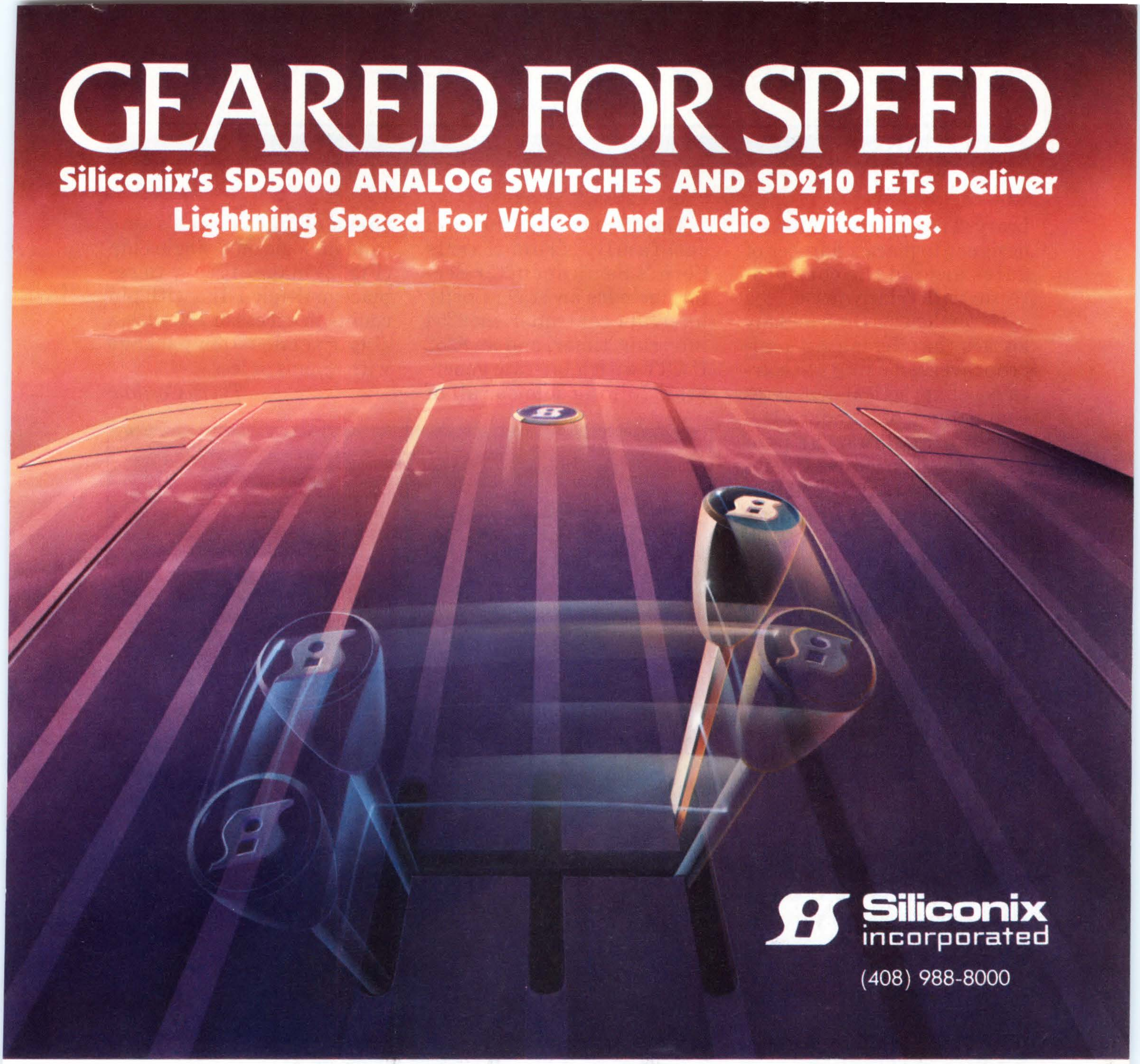
The flexibility of bit-slice processor cells has also proven beneficial in developing disk and CRT controllers and modems. Because it is easier to modify the timing and instruction set of a bit-slice core, Silicon Systems Inc. (Tustin, Calif.) has taken that approach. In addition, by combining processors on a single chip, duplication is eliminated.

The bit slice macro function of LSI Logic Inc. (Milpitas, Calif.) takes 744 equivalent gates, making it small enough to fit four functional 2901s on a single chip. A chip with 3,000 gates, enough for 4 bit slice processors and I/O, measures 240 mils per side using LSI's 2 micron technology, or 300 mils/side using 3 micron processes.

Standard-cell designers offer a mixed bag of bit-slice devices and microprocessors, but gate-array manufacturers are nearly unanimous in their choice of bit-slice technology. The notable exception is Calmos, which will use its 8085 standard cell as the core of a gate-array li-



1. Using NCR's standard-cell library, including its recently introduced CMOS 6502 microprocessor core, a semicustom chip—complete with analog functions, I/O, and all the components necessary for running the microprocessor—fits onto a single 50,000-mil^2 chip.



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brary. The approach allows a designer to place a number of gates around the core processor with relative ease.

Nevertheless, the company agrees that designing a microprocessor using gate arrays is impractical, but notes that a union of standard-cell (for laying down the processor) and gate-array technology delivers the flexibility and advantages of a gate array.

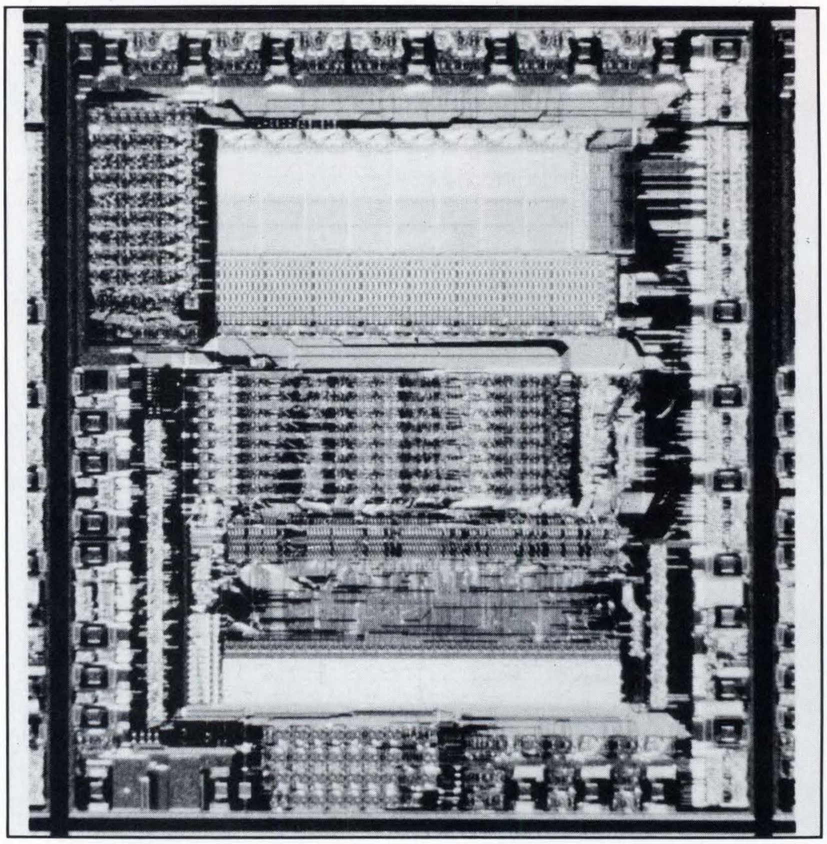
Most semicustom houses turn to CMOS for their gate arrays, but there is still a need for the blazing speed of bipolar ECL. Applied Micro Circuits Corp. (San Diego, Calif.) opted for this approach. Although the arrays can easily be used with other high-speed ECL circuits, they are also compatible with parts operating at TTL levels.

When one of the company's Q3500 family of bit-slice arrays is coupled with a single 2901, about 2000 gates are left uncommitted. That is enough to include a sequencer, carry and look-ahead logic, and the necessary registers. When a pair of processors is used, some of the control and support circuitry can be shared, still leaving room for additional circuitry.

The increasing emphasis on standard-cell microprocessors is also evident in the support circuitry beginning to appear in cell libraries. Just introduced this week is a library that does not include a processor but nonetheless underscores both the emphasis on complex standard cells and the increasing use of this technique.

The 2.5-μm CMOS standard cell family, from Harris Corp.'s Semiconductor Sector, includes an 8259 priority interrupt controller, an 8254 interrupt timer, and an 8252 UART with a bit-rate generator. Joining some or all of these circuits with some random logic on a single chip (Fig. 2) makes it easy to replace multiple DIPs with pin counts in excess of 100 with a single semicustom package with 68 pins or less.

Terry Costlow



2. The support circuits for the 8086 or 8088 can be constructed on a single chip using both new and existing standard cells. This configuration cuts the pin count to 68, from the over 100 pins associated with discrete components.

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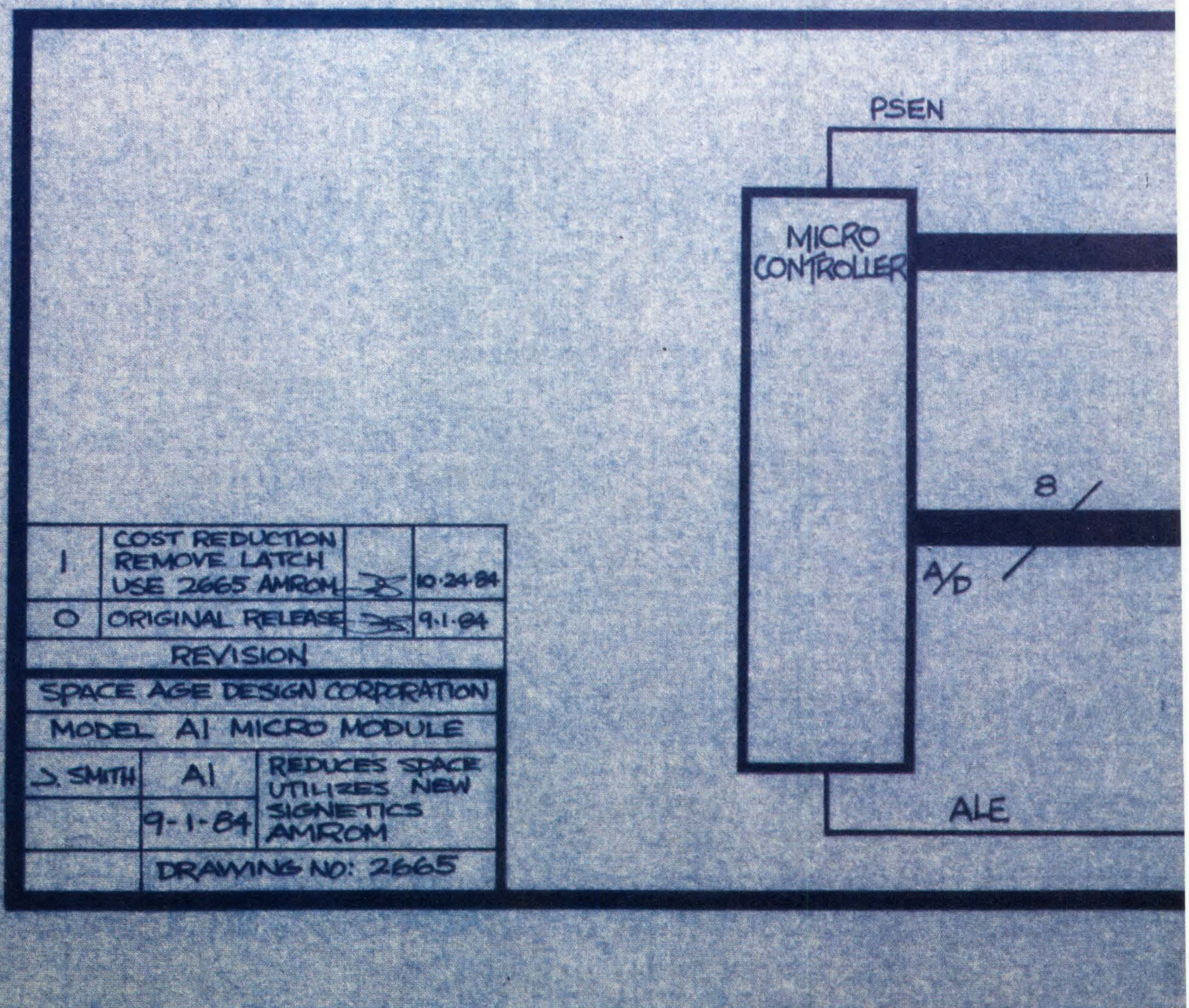

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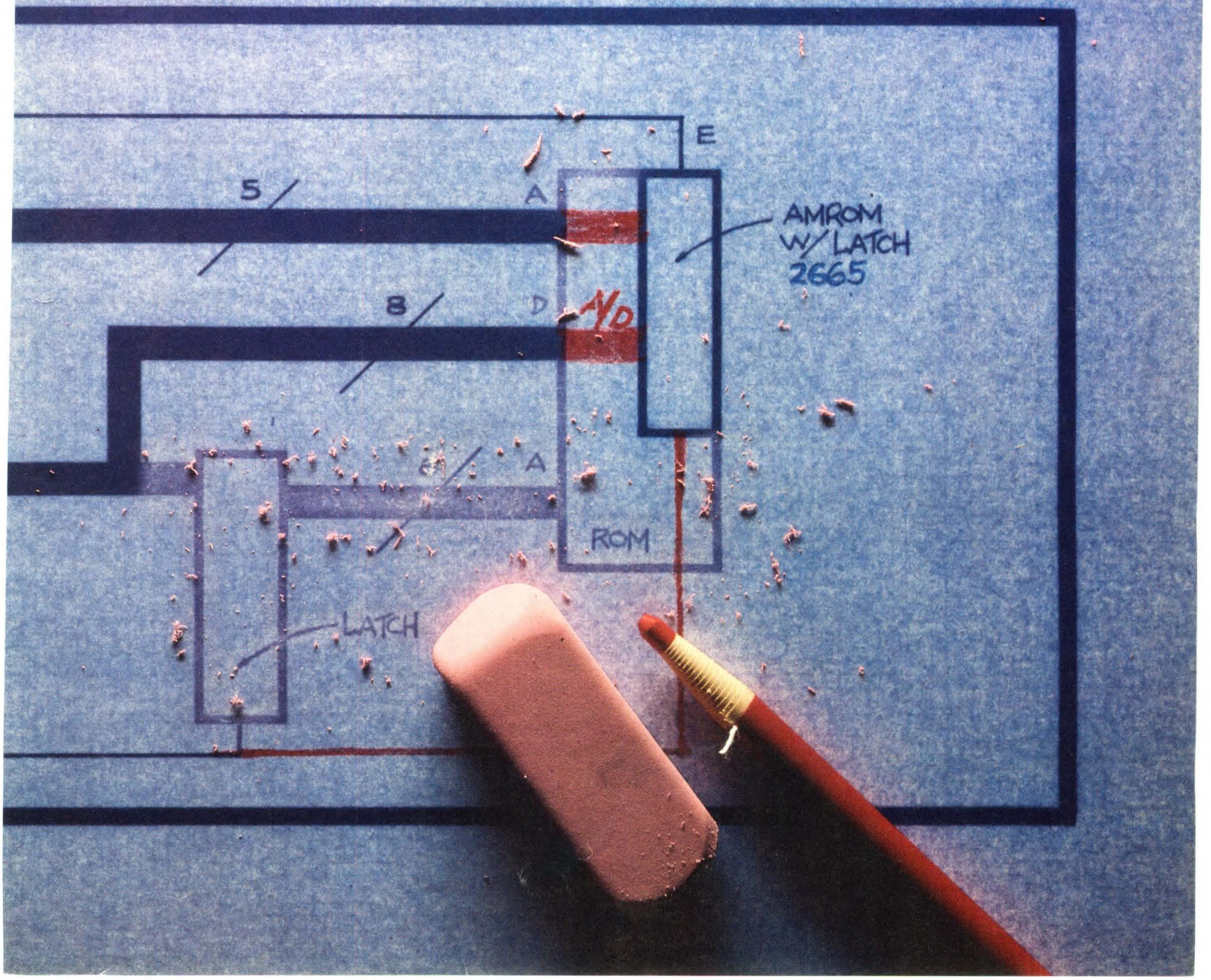

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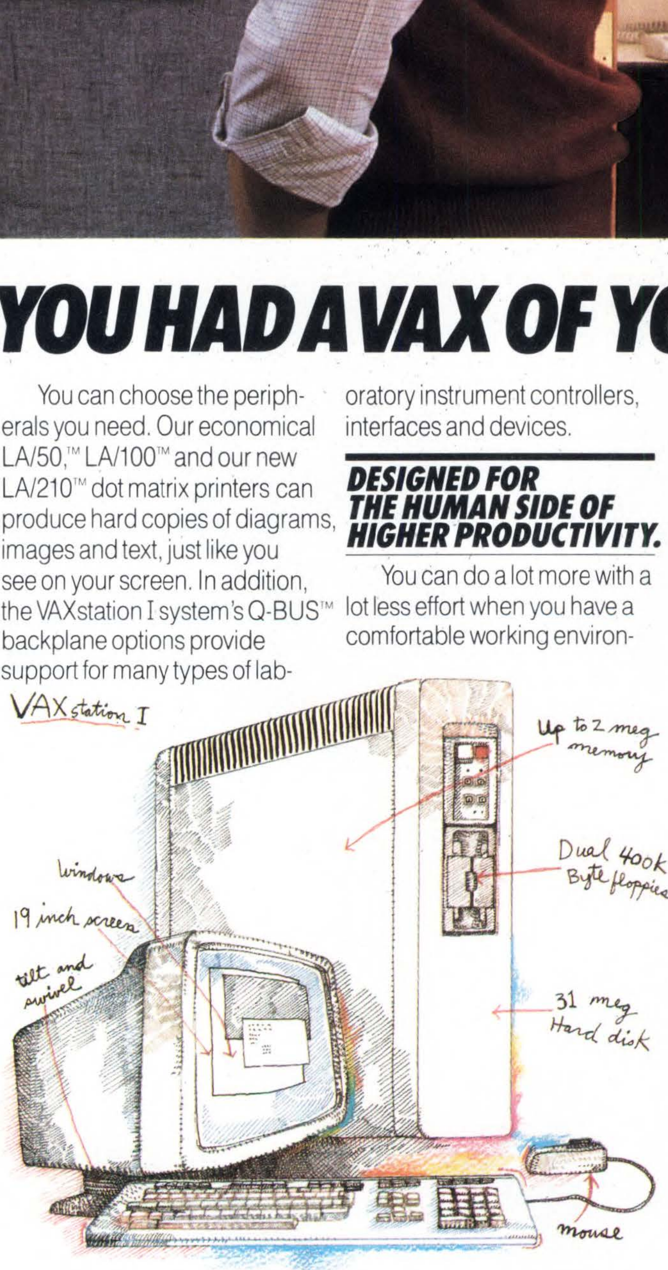

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The monitor, for instance, not only tilts, swivels and minimizes glare – it gives you a large working area with its 19-inch bit-mapped black and white display. What's more, it provides exceptional image clarity with its 960 by 864 pixel resolution. The refresh rate is 60 hertz and the display is non-interlaced, so it's virtually flicker free.

Windowing software lets you view and control multiple processes at the same time. You can overlay windows and move between them easily. You can even create highly integrated applications that dedicate multiple windows to a single process, and scale windows up or down in size.

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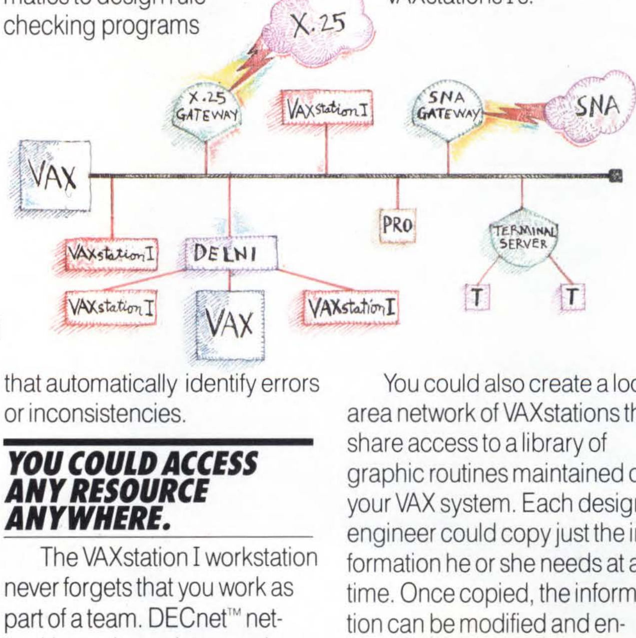
The VAXstation I workstation gives you a complete environment for many Computer Aided Engineering applications because it supports the GKS (Graphics Kernel System) industry-standard graphics application interface language and Tektronix 4014™ terminal emulation.

But VAXstation I lets you do a lot more than merely create engineering diagrams of your products. It lets you validate your designs through software because you can maintain a design rule database on your system. Then you can submit completed schematics to design rule checking programs



that automatically identify errors or inconsistencies.

YOU COULD ACCESS ANY RESOURCE ANYWHERE.

The VAXstation I workstation never forgets that you work as part of a team. DECnet™ networking software lets you share information with others in your organization over many types of communications devices.

For example, you can use an Ethernet local area network to link all your VAXstation I workstations together with your VAX system. Then you can download VAX applications to individual VAXstations I's.

You could also create a local area network of VAXstations that share access to a library of graphic routines maintained on your VAX system. Each design engineer could copy just the information he or she needs at any time. Once copied, the information can be modified and enhanced at the workstation.

You'll have an open line to the rest of the world, too, because DECnet software provides gateways to external communications environments such as packet-switched X.25 and SNA™ networks. You'll also have a wide variety of industry-standard protocols to choose from.

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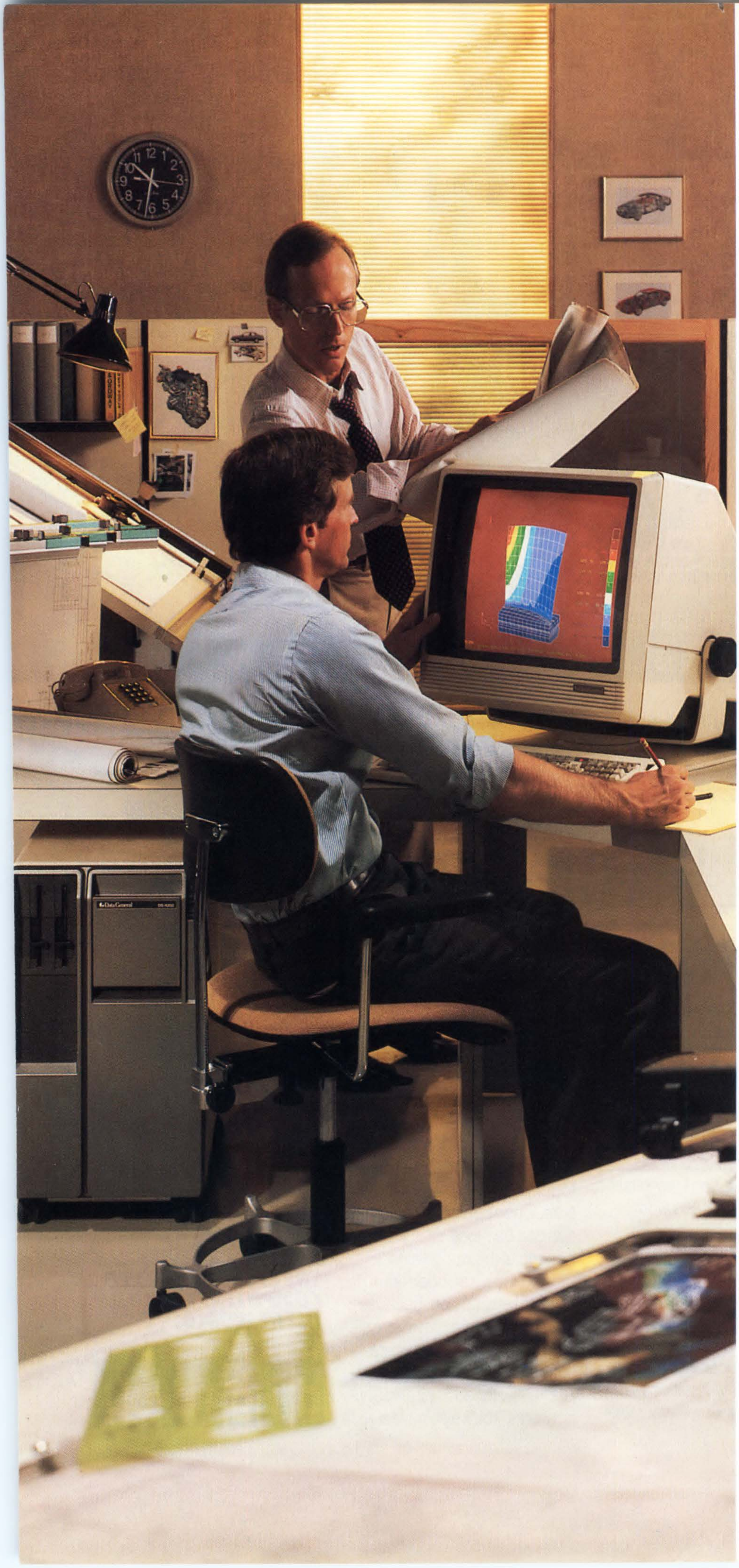

Eliminate problems

The new TMS4161 Multiport Video RAM from Texas Instruments is the first high-density dynamic RAM with two separate and independent ports. You can quickly move data out of or into the memory through the serial port at the same time the CPU is accessing the memory through the random-access port. Thus, the TMS4161 can supply video data to a bit-map display at the same time the graphics processor updates the video memory. This breaks the "bottleneck" of conventional DRAMs.

A 256-bit shift register is built in on the chip. As a result of this unique architecture, display refresh overhead consumes as little as 4% of available memory accesses rather than the typical 70% required by systems with standard DRAMs. This effectively eliminates memory contention problems inherent in computer graphics systems.

You also quadruple memory update bandwidth through the random access port. And the separate serial port can supply video data to support pixel rates to beyond 150 MHz—with a resolution exceeding 1,280 pixels per line.

These performance advantages are responsible for the Data General DS/4200 advanced engineering work station shown here, which has more functionality packed into an extremely compact system.

Proven technology for greater reliability

The TMS4161 Multiport Video RAM is built using the same proven high-volume technology as TI's industry-leading TMS4164 64K DRAM. Timing for the TMS4161 is compatible with the TMS4164—meaning that both of these top-quality memories can be mixed in the same memory system. Address pin locations are also the same on both devices, making PC board layout easy.

◀ **Improved memory efficiency** is produced by the unique multiport architecture of TI's new TMS4161 Video RAM. It increases memory system functionality while reducing system size and cost for applications such as this advanced Data General engineering work station.

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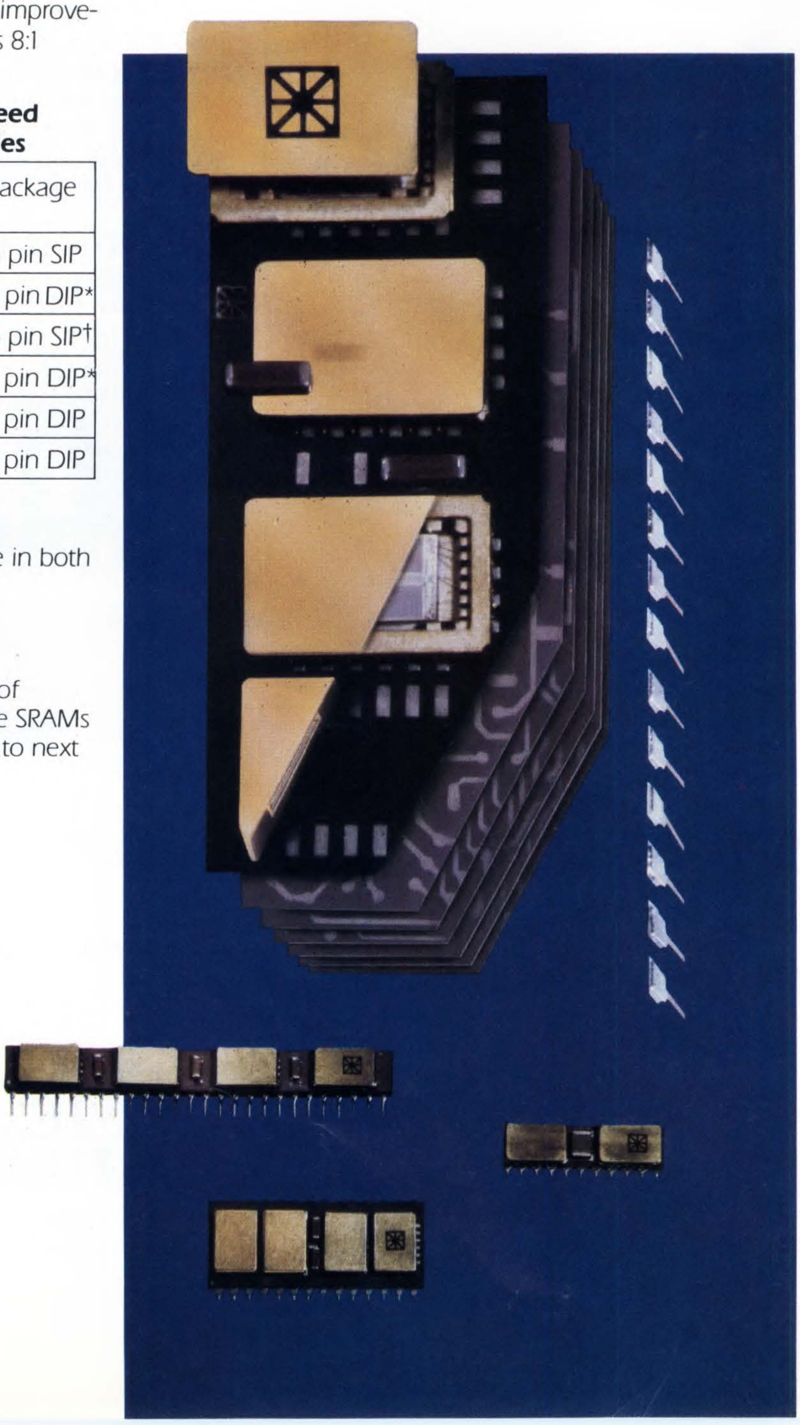

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VIEWPOINT

High resolution, full color will characterize future nonimpact printers

Keishi Kubo
Ricoh Co. Ltd.
Numazo, Japan

The past few years witnessed only the beginning of some remarkable advances in nonimpact color printing technology, declares Keishi Kubo. "We have gone from nonimpact color printers with seven colors and relatively low resolution to systems that can print between 8 and 64 colors with relatively high resolution." Augmenting that, Kubo is sure that "we are on the verge of a new generation of printers that will produce picture-quality copies with 64 colors or more at the speed expected of today's office copiers."

High-quality printing is essential since top-quality, full-color copies will be needed to supplement CRT displays. Already CRTs are widely used in remote sensing, image processing, and computer graphics, and the prospects for even wider applications exist in many other areas.

Along with more sophisticated computer-oriented applications, the demand for color printers is shifting from the simple, multicolor type, in which colors remain separate, to the full-color type, which have continuous color. Kubo goes on to explain that thermal print heads are one of the leaders in this evolution. In fact, they are advancing so quickly that they will soon be able to print two complete letter-sized sheets a minute, with a resolution of 16 dots/mm or more.

The real technical challenge, he stresses, lies in producing an image that looks smooth and uniform to the human eye. To do that, a printer would have to lay down at least 64 pixels/mm, with each pixel about 250 μm in size and made up of four dots apiece. Pixels smaller than 300 μm are generally indiscernible to the naked eye, although visual resolution obviously can vary from person to person.

Keishi Kubo has been a development leader in electrophotography, thermography, and imaging processes for Ricoh's R&D division. He graduated from Japan's Nihon University.

"To produce a good color image," Kubo believes, "there must be at least 64 density modulations [darkness levels available for each color]." Right now, most people use area gradation, a method that produces multiple density modulations by changing the number of recorded dots within a specified area. This tends to produce coarse-looking images.

But there are differing approaches to area gradation. For instance, jet-ink printers usually use a dispersion-type method, in which the recorded dots in each matrix are dispersed or decentralized. Thermal transfer printers, on the other hand, centralize the recorded dots in a matrix.

"Right now, multiple density gradation is very attractive because it creates full-color images," Kubo contends. "I believe that it can be used for a full-color printer capable of 64 density modulations—

VIEWPOINT

without increasing the resolution of the recording head. We already have a novel thermal-transfer, color-reaction paper that can yield images through density gradation. But right now it is capable of producing only 10 density modulations."

In order to get 64 density modulations with 4 pixels/mm, says Kubo, "we will need 64 density modulations for a thermal head with a 4-dot/mm resolution and 16 density modulations for one with a resolution of 8 dots/mm. Also, the head must be able to form a matrix of 4 dots for each pixel (one for each primary color and one for black). Kubo believes that when more companies realize this, research in nonimpact printing technology will focus more sharply on density modulation. *Carole Patton*

Even with semicustom CMOS chips closing in, TTL bus drivers are still ahead of the game

Ray Becker
Product Planning Manager
Digital Products Unit
Fairchild Camera and Instrument Corp.
South Portland, Me.

"Despite their strong presence now, discrete logic circuits are being used less and less frequently," states Ray Becker, "and they may soon be just a fond memory."

Swallowing up those random logic functions will be the growing families of customized circuits—gate arrays, standard cells, and hand-crafted designs.

"A few holdouts will remain," he adds. "There are a handful of standard logic circuits will be around long after bulk TTL-type chips have disappeared from designer's shelves." TTL-based bus driving circuits in particular, explains Becker, will not only remain, but will experience explosive growth over the next five years. "Since they actually interconnect subsystems, bus driving ICs like transceivers, multiplexers, and buffers form the backbone of almost every computer system built today. They'll continue as such tomorrow."

Ray Becker, currently product planning manager for Fairchild's Digital Products Unit, has held positions in engineering, sales, and marketing at both Fairchild and Texas Instruments. He holds a BSEE from Carshalton in London.

Driver ICs, Becker believes, cannot be translated economically into custom chips, largely because their output power and speed demand more silicon area than semicustom approaches can accommodate. Nevertheless, Becker urges, manufacturers "should think carefully about the design of driver ICs and how they will affect the design of future circuits. Otherwise they could lose semicustom's gains in size, speed, and power dissipation."

Converting large portions of random TTL circuitry to CMOS, for instance, would bring few benefits if the requisite driver circuits consume

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VIEWPOINT

a lot of power. Says Becker, "Designers would have to make do with large computer packages to dissipate heat, even though semicustom chips might have been able to reduce the overall system size severalfold."

Recently the industry has seen a new breed of high-speed driver circuits that are compatible with CMOS semicustom technology. Unfortunately, claims Becker, they still have a way to go before they can beat trusty low-power Schottky circuits. "The new circuits have a propagation delay of 12 ns and can drive only 8 mA; the older logic circuits have delays of 10 ns and can drive 24 to 48 mA. Moreover, the newer ones end up costing twice as much as their traditional counterparts." Considering those specifications, Becker is sure that "if you look into any high-volume personal computer, you'll find low-power Schottky drivers, not the latest generation of CMOS-compatible devices."

Yet the future of bus drivers is bright. "The failure of that new series is due largely to its 4-μm fabrication technology. A 2-μm process, now being explored by many semiconductor manufacturers, may solve some of the problems, combining the necessary speed, high driving capability, and low power consumption with a modest price."

Though Becker is sure that TTL driver functions will remain strong for five to ten years, he speculates that CMOS logic may well usurp their territory by the beginning of the century. "By then," he claims, "drivers will be built in CMOS, thanks mostly to improvements in packaging and design." Spurring that conversion will be VLSI technology, which will continue to lower the number of subsystems sharing a bus. With less-demanding drive requirements, concludes Becker, "CMOS bus drivers will fit right in."

Curtis Panasuk

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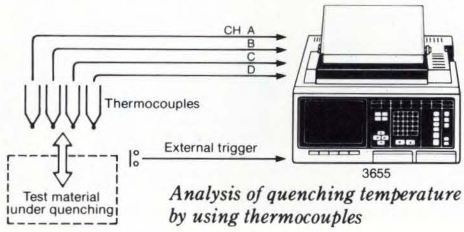
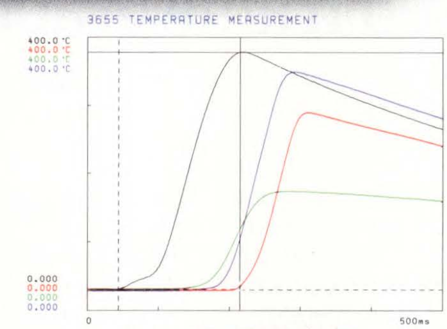


Analysis of quenching temperature by using thermocouples



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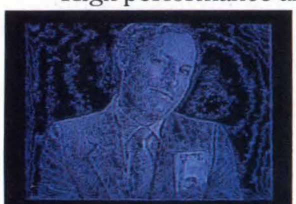

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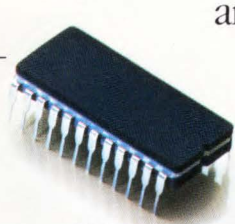

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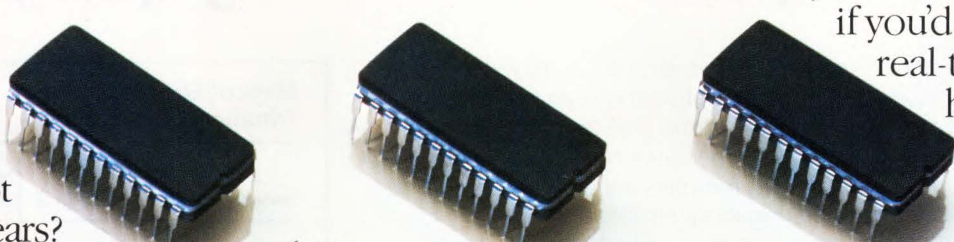

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CIRCLE 51

Purely optical switch positions itself for fiber-optic telecomm

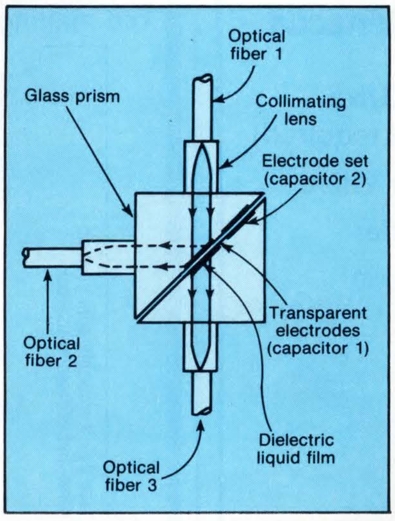
Based on prisms and liquid dielectric film, the optical switch suits tomorrow's fiber-optic telephone trunks and video systems.

Although broadband optical fibers are extremely efficient for transferring data quickly from point to point, switching data over fiber-optic trunk lines proves to be a sticky matter. The most common solutions—mechanical or electro-optical switches—may soon be displaced by a purely optical switch based on prisms and liquid dielectric.

The new component, dubbed Lidos for liquid dielectric optical switch, can switch between laser beams with diameters of 500 μm to 2 mm in less than 40 ms, far faster than mechanical parts. But like those parts, it can easily work with a broad variety of fiber sizes. As such, it is perfectly suited to fiber-optic telephone trunks and video links.

The conventional fiber-optic switch relies on mirrors or prisms which are mechanically moved or rotated, a relatively slow technique that is subject to mechanical errors and special setup considerations. Other switches, electro-optical in nature, generally convert the data on light beams into electrical signals, switch them, and then return them to optical form. That method requires many costly active components, yielding an expensive system that is prone to failure.

Mitch Beedie



The laser beam being switched is guided by an optical fiber, terminating with a collimating lens, to one side of the first prism. When the liquid dielectric is placed in the path of the incoming light beam, the beam passes ultimately to the optical fiber.

A more modern electro-optical switch is based on the change in a liquid crystal's refractive index when voltage is applied. However, the change is so small that the technique becomes inefficient. Moreover, the switch demands polarization of the light, possibly losing up to 50% of the light's intensity.

Switching to the new

Inside the new, purely optical switch—developed at Thomson-CSF's Central Research Laboratories (Orsay, France)—are two prisms, separated by 10 to 30 μm. When the switch is deactivated, the monomode or multimode laser beam coming from the optical fiber is focused by a collimating lens onto one face of the first prism and is then reflected at right angles (see the figure). The narrow gap between the two prisms is partially filled with a liquid dielectric film.

Moving liquid

When the optical beam is reflected at right angles, the fluid is outside the beam area. When the liquid is shifted directly into the beam's path, it switches the beam straight through to the second output. Since the film has the same refractive index as the prisms, the two prisms together act like a single window, enabling light to pass straight through. Moreover the identical refractive index keeps the switch's total insertion loss down to 0.5 dB.

Two parallel faces of the prisms are coated with transparent electrodes that form two capacitors, one of which lies in the path of the incoming beam. When a voltage pulse is applied to the other capacitor, the liquid flows between the capacitors, setting up an electric field that polarizes the liquid dielectric and causes electrostriction in the liquid closest to the field. That electrostriction increases local pressure, subjecting the meniscus on one side of the droplet to higher pressure than on the other side.

Since the liquid cannot be compressed, the droplet is pulled toward the source of the electric field. Once it reaches the activated capacitor—and thus switches the light beam to the relevant output—the voltage can be removed. As a result, the switch can be controlled with a voltage pulse only 500 ms long.

Determining factors

The response time of the switch depends on several factors, including the size of the capacitors and the droplet, physical parameters such as viscosity and surface tension of the dielectric liquid, and the operating voltage. The 40-ms switching time (measured from 10% to 90% intensity) was achieved on a laboratory model with 30-V pulses for light beams with diameters of 500 μm. The switch is a cube measuring 10 mm per side, with the electrodes having a surface area of 0.25 to 30 mm; a smaller version is planned for production next year.

The same principle has been used by Thomson to produce multipole switches. In that case, the light beam is directed onto the face of the first prism at an angle and is then reflected at 8 or 16 capacitors on the internal faces of the prism. The position of the liquid dielectric determines the point from which the light beam emerges. Several of these devices can be cascaded to switch more than 64 light beams.□

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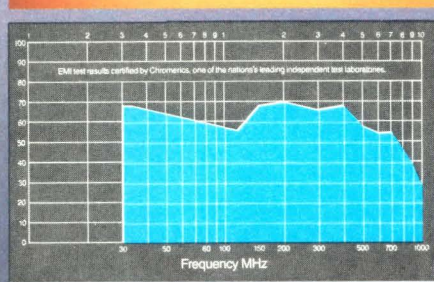

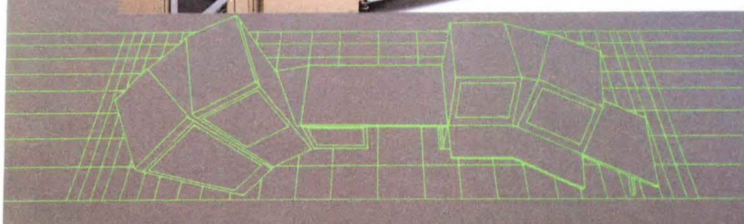

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CIRCLE 53

INTERNATIONAL MEETINGS

Micro-Computer '85, Jan. 29–Feb. 3. Frankfurt, West Germany. Philippe Hans, German American Chamber of Commerce, 666 5th Ave., New York, N.Y. 10103; (212) 974-8856.

Middle East Electricity and Electronics Exhibition, Feb. 2–6. Jeddah Expo Center, Kingdom of Saudi Arabia. Len Bennett, Logistics, 237 Park Ave., 21st floor, New York, N.Y. 10017; (212) 551-3530.

American Federation of Information Processing Societies Inc. (AFIPS-Asia '85), Feb. 14-March 2. m.v. World Wide Expo, Tokyo, Osaka, Kitakyushu, Taipai, Hong Kong and Singapore. AFIPS, 1899 Preston White Drive, Reston, Va. 22091; (703) 620-8926.

Autotech Hong Kong '85, March 7–8. Hong Kong. Autotech Hong Kong '85, Hong Kong Productivity Center, 12th floor, World Commerce Center, 11 Canton Road, Tsimshatsui, Hong Kong; 3-7235656.

Componentes Electronicos '85, March 12–15. Mexico City, Mexico, March 19–22, Guadalajara, Jal., Mexico. Raquel Polo, United States Trade Center, Liverpool 31 Col., Juarez 06600, Mexico, D.F.; or PO Box 3087, Laredo, Texas 73044.

The Scottish Computer Show and Conference, March 12–14. Anderston Exhibition Centre, Albany Hotel and Holiday Inn Hotel, Glasgow, Scotland. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TWI 3SZ, England; (01) 891-5051.

International Exhibition on Electronic Testing, Measuring Instruments and Production Technology (ChinaTronic '85), March 14-19. Tianjin Exhibition Centre, Tianjin, Peoples' Republic of China. Asdale Exhibition Services, 109-111 Gloucester Road, 21st floor, Wanchai, Hong Kong; 5-8920511.

Comtel '85, March 18–20. Infomart, Dallas, Texas. Comtel '85, International Computer & Telecommunications Conference, 5080 Spectrum Drive, Suite 707E, Box 17, Dallas, Texas 75248; (214) 631-6482.

Automatic Testing and Test Measurement '85, March 19–21. Rhein-Main-Halle, Wiesbaden, West Germany. Network Events Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, England; (0280) 815226.

Networking '85, March 23–31. Tokyo, Japan. Brad Ketchum, INC. Publishing Corp., 38 Commercial Wharf, Boston, Mass. 02110; (617) 227-4700 or Aki Tsurukame, Pacific Catalyst Group, 650 Grand Ave., Suite 1004, Los Angeles, Calif. 90017; (213) 614-0049.

IEEE Infocom '85, March 25–28. Washington, D.C. Celia L. Desmond, IEEE Infocom '85, Room 1855, 160 Elgin St., Ottowa, Ont., Canada K1G 3J4; (613) 239-4510.

Bit '85 Computer Show and Conference, March 26–29. National Exhibition Centre, Birmingham, England. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TW1 3SZ, England; (01) 891-5051.

Comdex In Japan, March 26–28. Tokyo International Trade Center, Tokyo, Japan. Milton Berns, The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

32nd International Electronics, Energy and Aerospace Exhibition (Riena), March 26–31. Rome, Italy. Riena, Via Crescenzio 9, 00193 Rome, Italy; (06) 6569343/4/5.

Internepcon/Semiconductor International, March 27–30. Korea Exhibition Center (Koex), Seoul, Korea. Cahners Exposition Group, 7315 Wisconsin Ave., PO Box 7007, Washington, D.C. 20088; (301) 657-3090.

Unix Systems Expositions '85, April 2–4. Palais des Congres, Paris, France. Networks Events Limited, Printer Mews, Market Hill, Buckingham, MD18 1JK, England; (0280) 815226.

Electronics and Electrical Engineering Exhibition, April 17–24. Hanover, West Germany. Hanover Fairs, PO Box 338, Whitehouse, N.J. 08888; (800) 526-5978 or (201) 534-9044.

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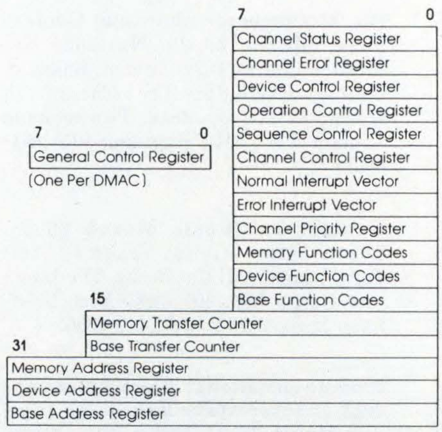

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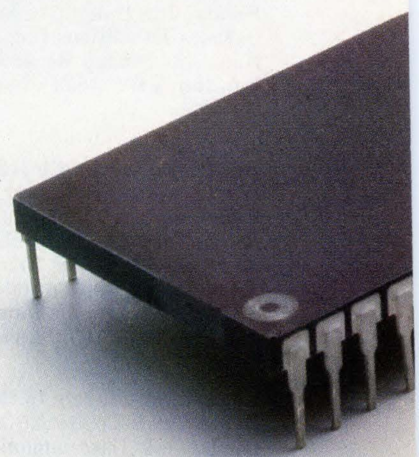

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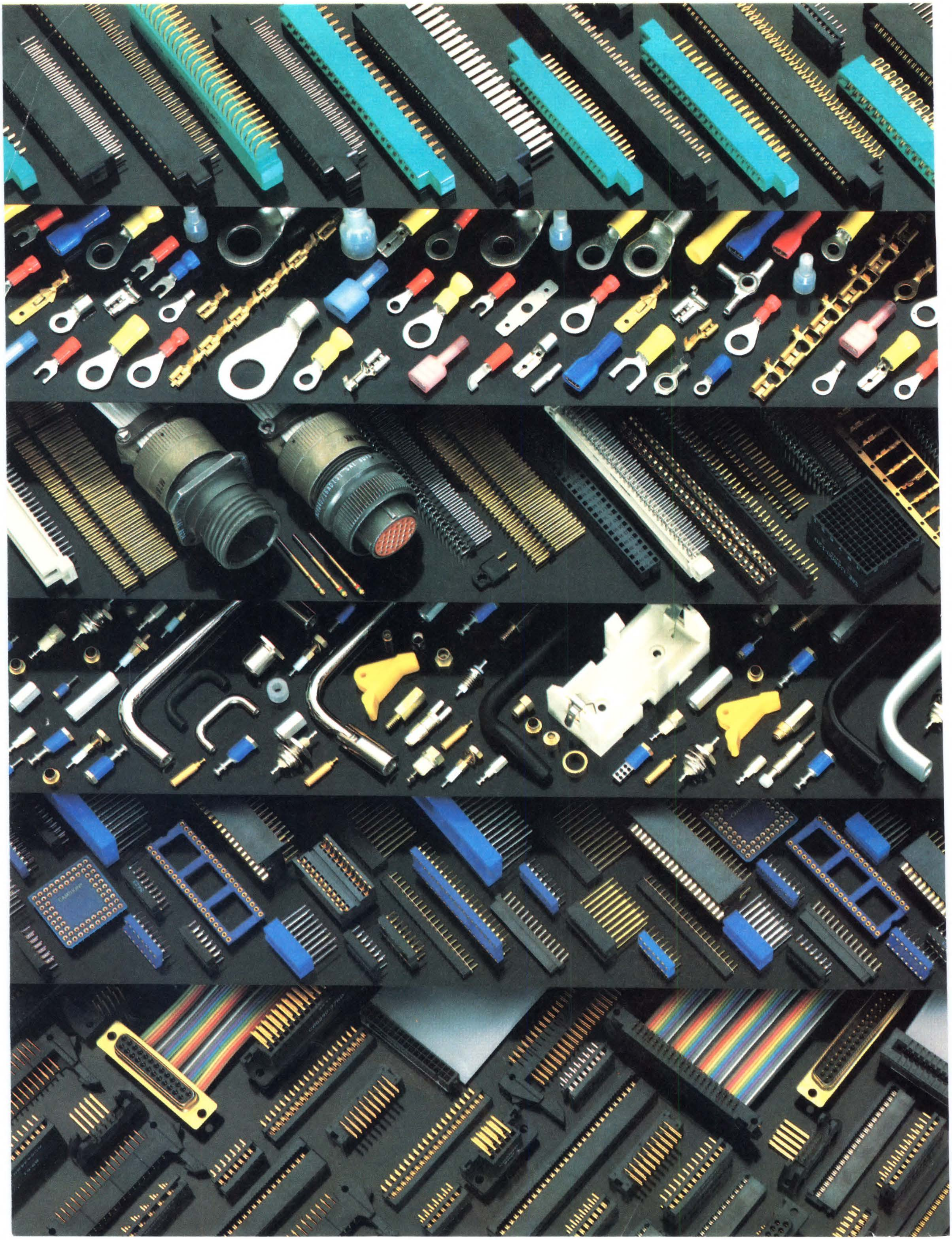

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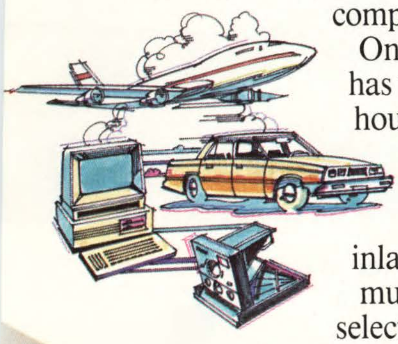

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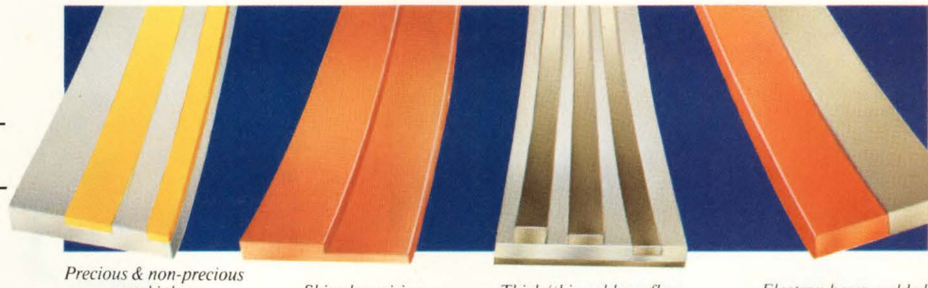

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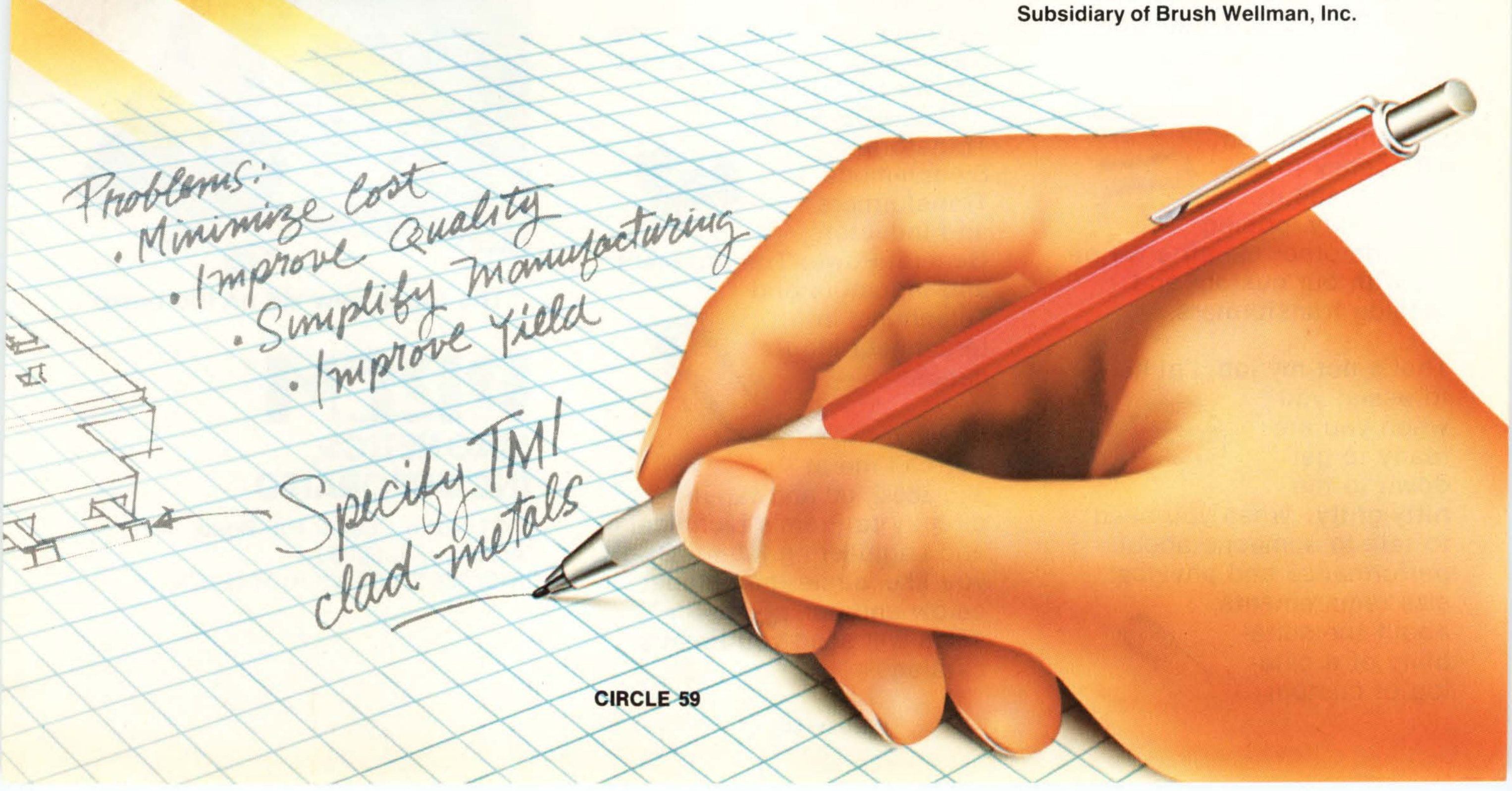
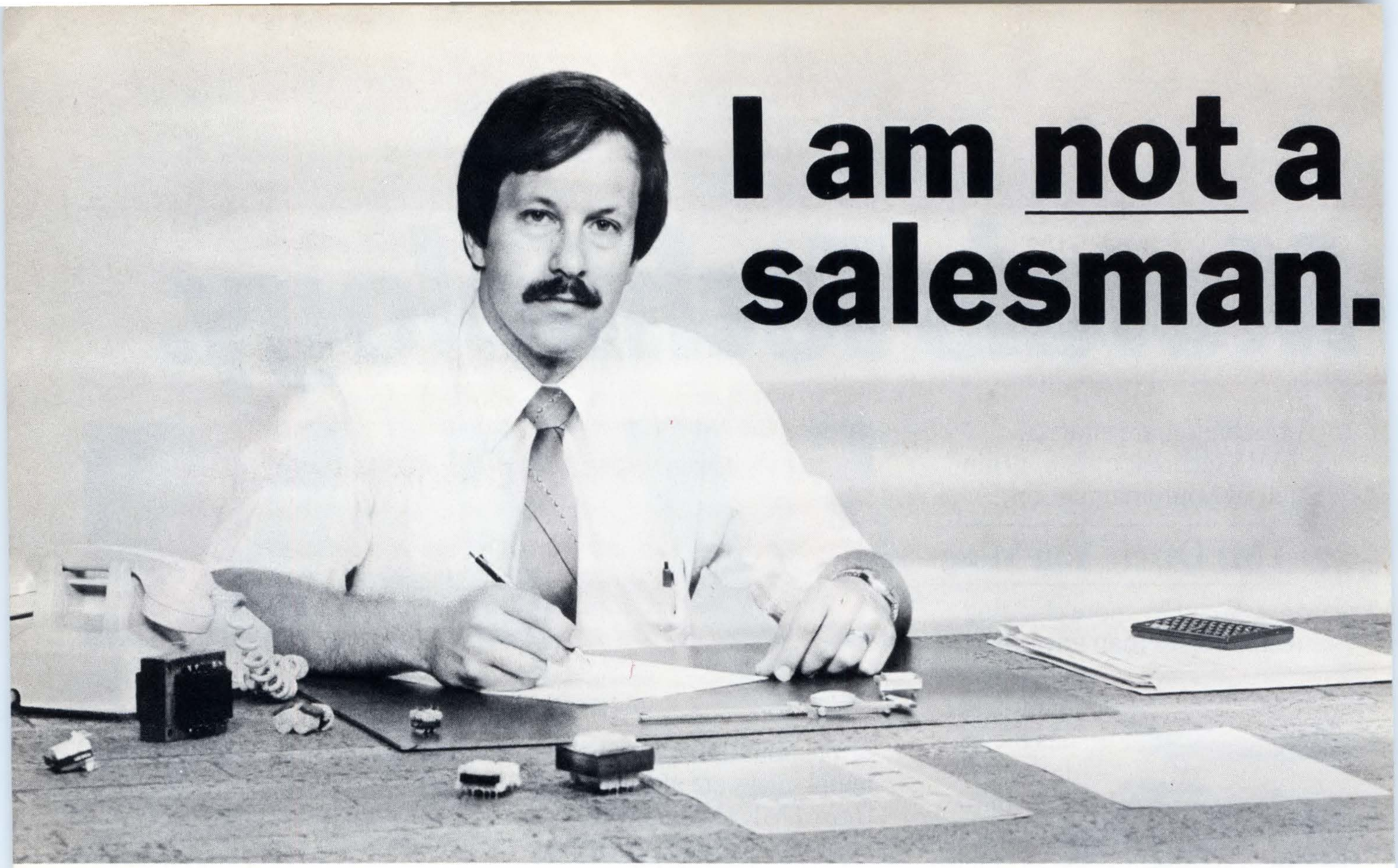


CIRCLE 59



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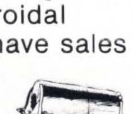

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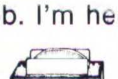

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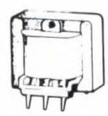

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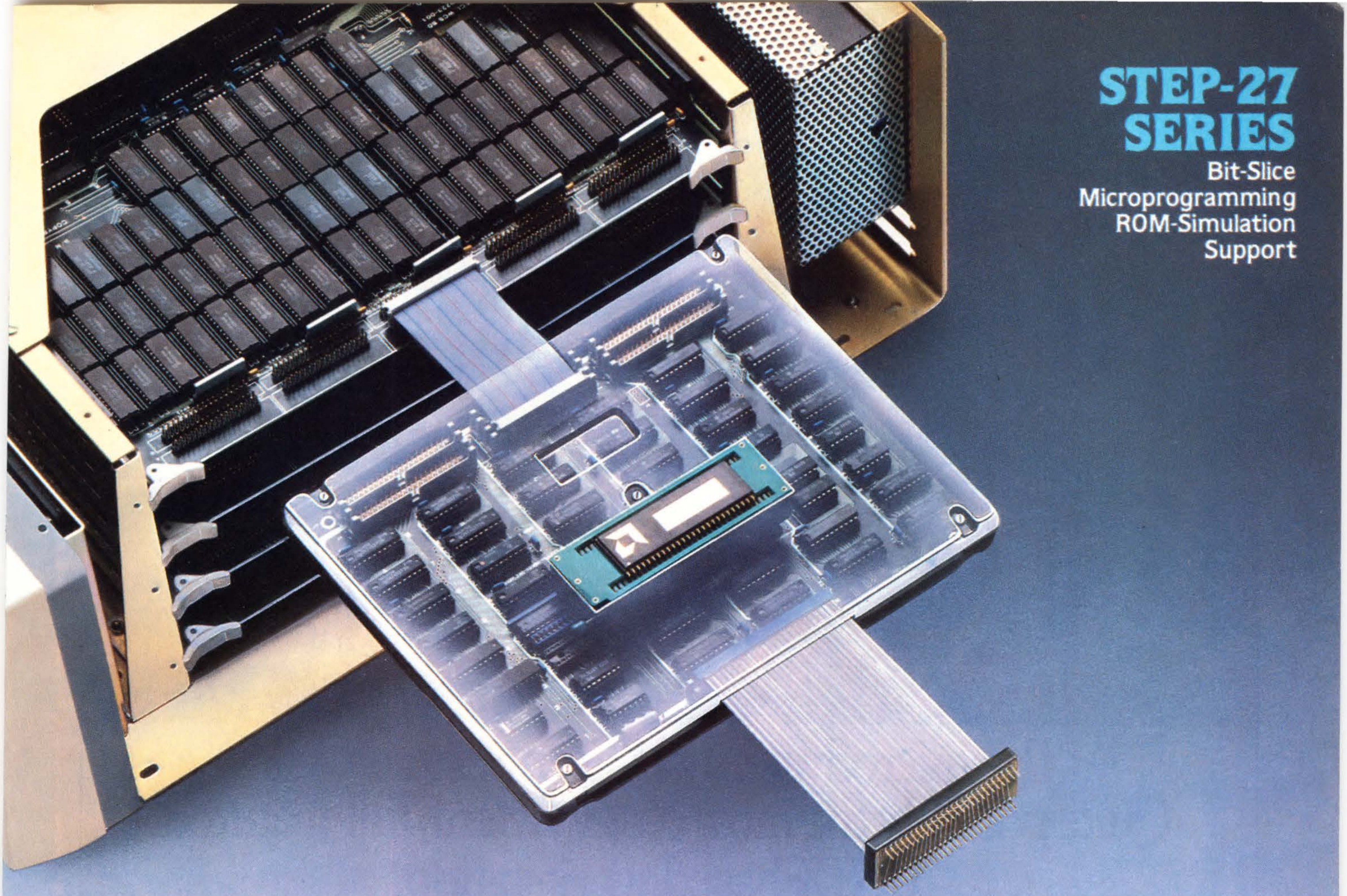

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1985 TECHNOLOGY FORECAST

For many years our Technology Forecasts have predicted enormous and rapid progress in various areas, especially in semiconductors and computers. But this year's reports foresee something more: fundamental changes in the role of the designer. New responsibilities will branch off into production and testing, and the design engineer will increasingly interact with the end users of his system.

Given the evidence presented in our lead-off report on expert systems, one can understand how the system designer must gain at least some familiarity with the subject before he can assemble a knowledge base properly. Eventually, languages now in development promise a wealth of tools that will enable users themselves to write their own knowledge bases. For now, though, a fair amount of involvement is required between the designer and the user.

Our second Technology Forecast probes an area that virtually invites the design engineer's participation — circuit testability. Here, the complexity of today's technology has finally caught up with the designer. Already testing expenses make up as much as 25% of a product's total cost, and that percentage will grow much larger if something is not done to change the trend. That "something" is for the design engineer to consider testing, or at least testability, as part of his responsibility. For that to happen, management will have to get into the act, mandating that testability and function be considered equally important design goals.

How reduced-instruction-set computers will affect engineers is difficult to predict because the machines are just in their infancy. One thing is certain, as our third Technology Forecast asserts, RISC machines will be the dominant computer form by 1990. So far only two companies are producing commercial machines, but the heavyweights are expected to make their moves any day now. Once they do, RISCs — with their incredibly high processing speed — will embark on their course toward world domination.

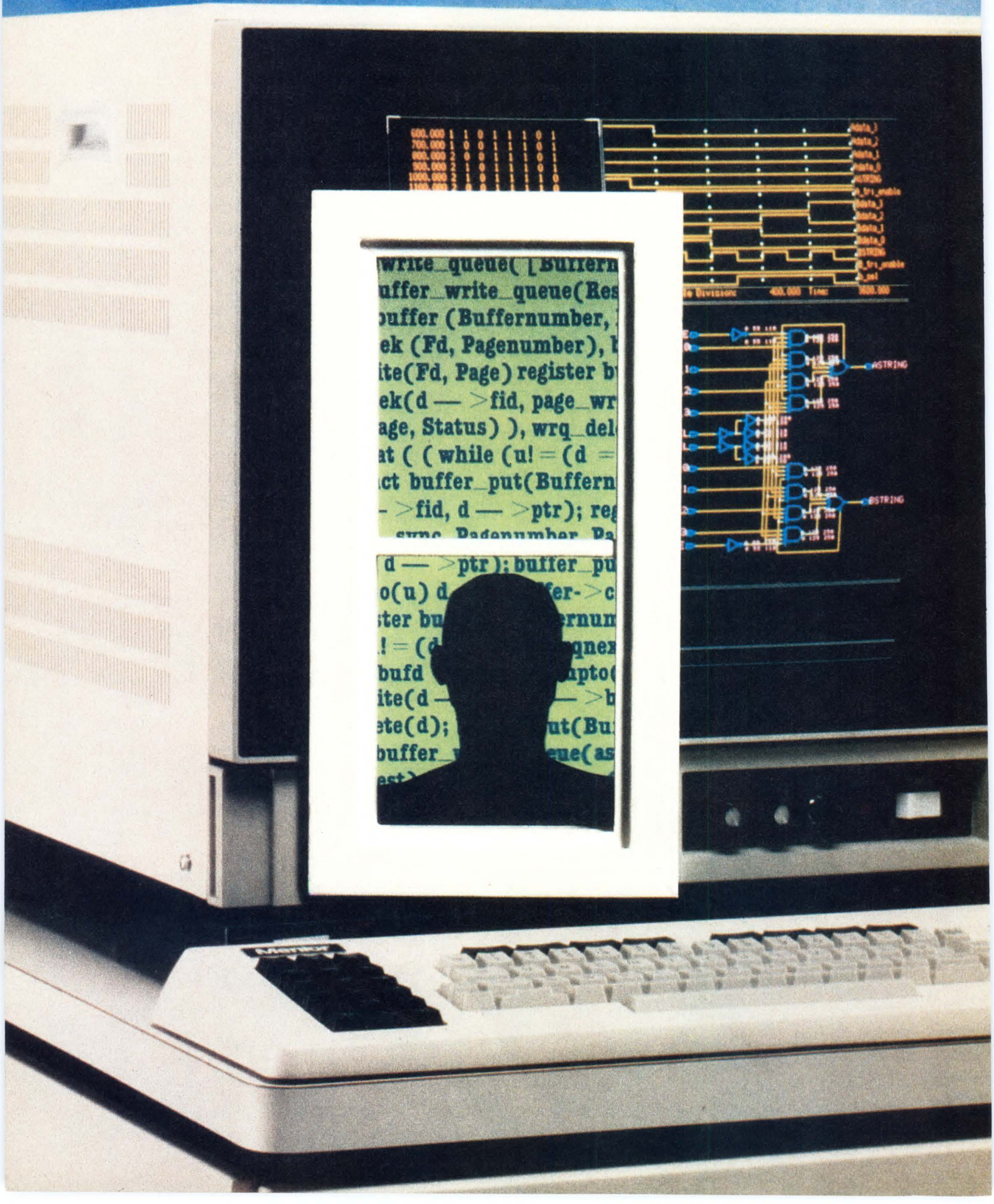
Our fourth Technology Forecast, on telecommunication ICs, examines the telephone system and its steps toward becoming an all-digital network. Key here is the Integrated Services Digital Network, or ISDN. Once it is in place, establishing a high-speed digital communication link will be as easy — and as inexpensive — as making a phone call. Modems will no longer be necessary. As a result, engineers will be able to design systems that assume the availability of reliable digital communications.

Surface-mounted devices, the topic of our final report, also dictate an expanded role for design engineers. With surface mounting, a designer's commitment will lie not in testability but rather in production. Within five to ten years, half of all components sold will be surface-mounted; the remainder will go at a premium price. All designers, in other words, will be under great pressure to learn about and use equipment, boards, and components suitable for surface mounting.

The Technology Forecast reports are not alone in predicting a changing role for the designer. Our interview section, in which ten electronics pioneers talk about the future, emphasizes how tomorrow's engineers will have to become much more proficient in software than they are today. The interviewees, each the "father" of an important technology, have no doubts that the hardware problems facing the industry will be solved without any extraordinary effort or expense. About software, they are not so sure.

The future should be interesting.

1985 TECHNOLOGY FORECAST



EXPERT SYSTEMS

On its way from research to industrial applications, artifical intelligence finds itself in the throes of rapid change. Suddenly, efficiency in the design and execution of artificially intelligent systems is assuming a dominant role. As a result, artificial intelligence work will, in years to come, divide more clearly into academic research and industrial development. In fact, some insiders predict that the fledgling field of artificial intelligence will be absorbed by those industry sectors that actually use its unusual software and concepts for their own applications.

Because qualified personnel are in extremely short supply, many researchers in artificial intelligence laboratories are already trying to come up with tools and methodologies to simplify the development of future AI products. Languages, knowledge-base schemas, user interfaces, and in-

MAX SCHINDLER

ference paradigms all are undergoing re-evaluation with an eye on efficiency.

Another obstacle must be overcome before a reliable AI industry can develop: The hardware on which its programs run must become cheaper. That is why artificial intelligence companies are addressing some mundane problems—execution speed, code size, and transportability—things that AI workers have always loved to ignore.

Finally, as commercial products, artificially intelligent systems demand ease of use, as well as robustness. Malfunctions regarded by a graduate student in an AI laboratory as merely a trivial nuisance can render the system useless to a layman, even one familiar with computer tech-

What makes an expert system tick?

Expert, or knowledge, systems differ from conventional computers in two ways: Instead of breaking down into an application program and an operating system, expert software consists of a knowledge base and an inference engine. The former contains facts and rules specific to the problem at hand, while the latter evaluates the rules. Advanced (generic) expert systems often keep metarules separate from the problem-related rules. Because the metarules determine the strategy by which the inference engine invokes the problem rules, keeping them separate adds flexibility to the system.

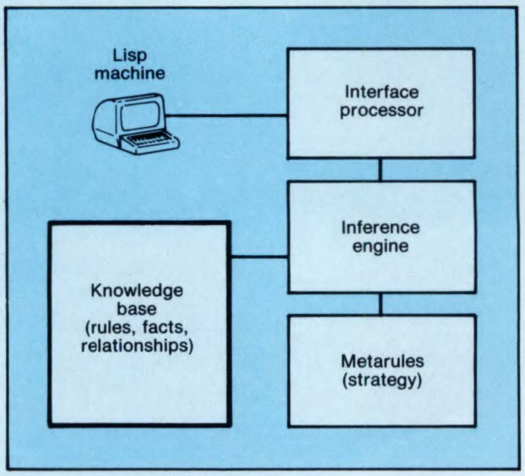
Present expert systems rely largely on two paradigms for searching the solution space (which has as many dimensions as there are variables). The first technique, called forward chaining, starts with a known state and applies the knowledge rules to find a way toward the goal. If the problem were, say, to find a route from Chicago's Lake Shore Drive to New York, the rules would specify what to do at intersections. The metarules would specify to start at the origin and perhaps to evaluate alternatives at intersections in a clockwise direction.

In contrast, the second technique, called backward chaining, would start in New York and feel its way back toward Chicago. The metarule would then tell the system to start at the goal. In this example, it is obvious that a combination of forward and backward chaining would narrow the search space substantially.

To find a route between two cities, rule-based (or "shallow") reasoning is quite adequate, but most engineering applications require that a system take into account "first principles," the laws of physics, for instance. Unfortunately, few expert system "shells" (which let the user add the expertise) support such reasoning.

On the other hand, if a system can execute only algorithmic procedures, it does not qualify as an expert system. Unlike conventional computer-aided design, inference-based reasoning can handle uncertainly—in other words, it is heuristic in nature. Whenever one single, well-defined solution exists for a problem, the algorithmic approach should be used, because it always requires smaller computer resources.

Most expert systems today are written in Lisp and hence reside on Lisp machines (see the figure). In "shell" systems the knowledge base is empty, but the interface handler often entails features to simplify knowledge acquisition.



nology. Software automation is one way to attack the problem—producing better software and lowering design costs.

Currently, artificial intelligence programs are being applied in robotics, natural-language interfaces, and expert systems. The first still remains at a level so primitive that few electronics designers need be concerned about its impact. The

Engineering systems must handle the laws of physics, not just rules of thumb

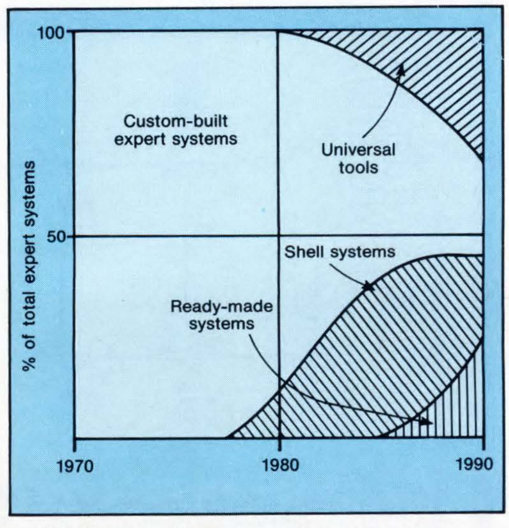
second, too, will have little effect because natural languages are inherently so ambiguous that few experts—even within the AI industry—can foresee their usefulness in any serious design work.

That leaves expert systems as an important area to be dealt with (see "What Makes an Expert System Tick," opposite). However, although the industry is concentrating its efforts here, the current shallow reasoning of expert systems lends itself primarily to such easy and lucrative applications as banking, insurance, and investment planning—not to engineering. But systems have begun to emerge that can sustain reasoning based on first principles (what artificial intelligence researchers call deep knowledge of the world) expressed by, say, the laws of physics.

From their inception in the mid-1960s through the mid-1970s, expert systems were strictly custom-made, and they cost millions. Only in recent years have methods evolved that will reduce design costs, primarily in the form of system shells and knowledge acquisition tools. Their success or failure will determine the future of the whole species (Fig. 1).

By separating the reasoning software (called the inference engine) from an expert system's domain-specific knowledge, artificial intelligence workers have learned to derive "generic" expert systems, or shells, which can be put to work with a new knowledge base. In fact, these shells, based on successful custom systems, gave birth to the AI industry. Even so, shells tend to carry the flavor of their original application goals. For example, Emycin—now available for the Texas Instruments Professional personal computer—was derived from a medical diagnostics system called Mycin. Although it lends itself readily as a diagnostic tool for auto mechanics, it is not suited for, say, process control.

All of the shell systems now available suffer from this limitation. Some industry experts therefore predict a limited future for shells. Instead, they concentrate their own efforts on more general tools. One example is the Automated Reasoning Tool—ART, as it is called—developed by Los Angeles-based Inference Corp. (ELECTRONIC DESIGN, Aug. 9, 1984, p. 153). It combines several inference paradigms



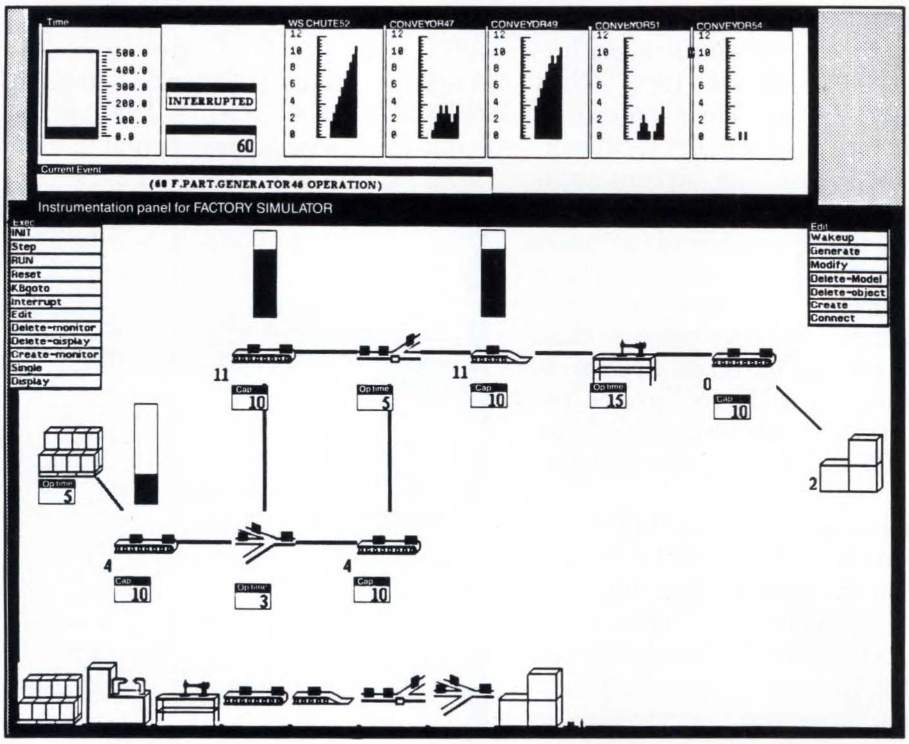
1. Originally, all expert systems were custom-built. In recent years, shell systems have begun to blossom but will eventually yield to ready-made systems and universal knowledge-processing tools.

with tools that simplify the acquisition of new domain knowledge. Another tool, KEE, from IntelliCorp (Palo Alto, Calif.), has been used for genetic research and spectroscopy but continues to introduce new features. The "active images" interface, for example, will permit the user to model, say, an automated production line (Fig. 2).

Some AI companies bet on expert system shells, others emphasize tools

Another tool for expert system generation that could prove especially helpful to engineers is KES from Software Architecture and Engineering (Arlington, Va.). Thanks to its ability to derive rules from statistical patterns, the tool can, in some applications, get an expert system running in a few days. Although field experience is still meager, KES deserves close attention in years to come.

Like so much in artificial intelligence, however, the distinction between a shell and a tool is still relatively unclear. To make matters worse, some manufacturers are beginning to shy away from the "expert system" label in cases when the user needs to supply his own expertise. "Knowledge system," "competence system," and "metasystem" are some recent buzz words applied to both shells and knowledge acquisition tools. Furthermore, no definite



2. Existing knowledge tools like KEE continue to sprout interface features like the "active images" screen. Here it is used to model an automated production line.

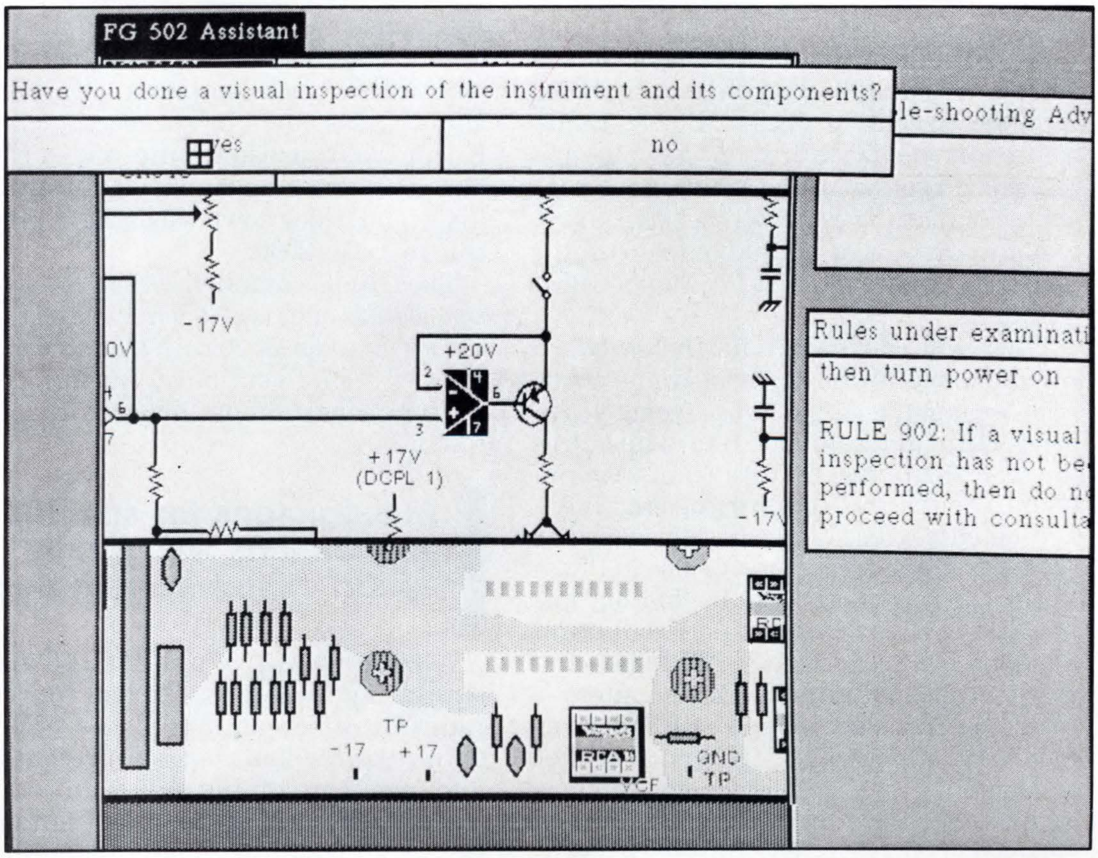
line is drawn between an expert system's inference engine and the language it uses. For the present discussion, the inference engine will be regarded as part of a shell, and languages as tools.

Semicustom systems for standard chores like testing will prove feasible

A third alternative in custom-made expert systems will emerge toward the end of the decade: ready-made systems, aimed at specific knowledge domains. For example, most electronics companies face the problem of having to repair their products. An expert system, aware of some basic natural laws and equipped to deduce problems from given test results, should be useful for enough customers to support its development costs.

Tektronix Inc. (Beaverton, Ore.), for example, needs such a system for its own repair shops, especially when it comes to fixing instruments no longer in production. So, development of an expert system is under way, and it may eventually become available to the public (Fig. 3).

In fact, once most competing firms in any given field have developed their own expert systems, turning them into commercial products will become commonplace—probably within the next ten years. These systems will be generic only in the sense that product-specific information



3. Intelligent assistants will soon simplify troubleshooting of electronic equipment. By tying schematic and physical layout together and interpreting test data, such an expert system can multiply a technician's effectiveness.

will be removed.

IC design poses another lucrative opportunity for third-party domain-specific expert systems. The CAE setup from Cericor (Salt Lake City, Utah) relies on an expandable knowledge base and applies such artificial intelligence concepts as the inheritance of properties within component classes. However, most efforts along this line will be incorporated into existing workstation packages, as exemplified by inclusion of a testability analyzer in the Logician workstations from Daisy Systems Corp. (Sunnyvale, Calif.).

Future AI hardware will need software support as badly as today's PCs

Makers of artificial intelligence hardware, too, are designing adaptable, industry-specific packages. But it stands to reason that within five years AI machines will follow in the footsteps of personal computers: They will be sold only if enough software is available to do useful work (ELECTRONIC DESIGN, Aug. 9, 1984, p. 106).

Users who cannot wait for this software can now benefit from such tools as special-purpose languages, like those from two recent artificial intelligence start-ups. Production Systems Inc. and the Carnegie Group (both in Pittsburgh, Pa.) have agreements to use languages developed at Carnegie-Mellon University (also in Pittsburgh) and prepare them for factory applications. The OPS83 from Production Systems is based on OPS3 of R1 fame—the system that configures VAX computers—while the Carnegie Group's SRL+ derives from SRL, a language with a good deal of production experience. By using such language tools, the expert system builder is relieved of concerns over inference mechanisms, just as if he were using a shell. Yet he can optimize the system for his needs.

A closer look at the Carnegie-Mellon languages proves the point. OPS83, for example, is a descendant of OPS3 and OPS5, which ran atop a Lisp environment. OPS83, however, needs no such crutches because it includes Pascal-like constructs that simplify the intermingling of rules and algorithms (Fig. 4). Statements can be executed that modify stored values (e.g., &L=&L+1), while rules can execute control statements—for example:

```
rule kill_links
  {
    &G (goal type=kill—links);
    -->
      remove &L;
  };
```

(The prefix & identifies variables.)

Because of OPS83's functionality and speed, systems with 10,000 rules will be practical for such complex applications as threat assessment or spacecraft control. In contrast, present rule-based ("production") systems, running largely atop Lisp, tend to bog down when the number of rules exceeds 2000.

The OPS83 compiler, which consists of 20,000 lines of C, is efficient enough to execute an average of 50 rules per second on a VAX-11/780. Eventually, multiprocessor hardware will boost processing speed further.

AI languages for specific applications will greatly speed expert system design

Although SRL+ and OPS83 aim at similar applications, the two represent radically different approaches. SRL+ is an integrated knowledge representation and problem-solving environment that runs atop Common Lisp, the Pentagon's favorite Lisp dialect. As a frame-based language, whose primitive is a schema, SRL+ tackles combinations of object-oriented, rule-based, and logic programming. Embedded within it are a database system, a window package, and color graphics.

A sensor-based diagnostic application has served as the proving ground for SRL. To distinguish between different external conditions, "contexts" guide the execution of rules, for example:

```
{{context
  VALUE: < true | fast | 0 | 1 >
  DESCRIPTION: "English explanation"
```

This schema contains two attributes (called slots), of which only VALUE is significant because it specifies all acceptable values for context. Most schemas are substantially larger and can become the equivalent of records in such applications as planning or decision support.

While the preceding discussion gives insight into the means by which future expert systems will be constructed, it says little about their applications. To understand those applications, a closer look at the evolution of AI software is necessary.

Three sources, or roots, feed present and future AI-based developments. Most essential are the concepts of artificial reasoning: inference methods, predicate logic, and the formalization of knowledge. Tools developed in the pursuit of these goals—the second element of current progress—have turned out to be perhaps even more important than the basic concepts. These tools include languages like Lisp and Prolog, object-oriented programming, and a wide spectrum of software development aids, richer even than the popular Unix environment.

Hardware represents the third root. Early work proceeded on mainframes, often with inadequate compilers and architectures. Not until the efficient Lisp machines surfaced did expert systems evolve into viable products. Naturally, hardware speed and cost will greatly affect future

```
rule volume_T07F03
-- compute the volume of material in T07F03 from the fluid level
   {
          (goal                          --If there is a goal
             type = volume) ;            --with volume in
                                         --its type field,

   &M     (measurement                   --And there is a measurement
             attr = level;               --with "level" in
                                         --its attribute field
             object = T07F03) ;          --and with T07F03 in
                                         --its object field
   -->
          local &VOL:real, &LEV:real;    --then the following
                                         --calculation is
                                         --to be performed

          &LEV = &M.value;
          if (&LEV <= 6.5)
             &VOL = 5.0*&LEV + 5.5
          else if (&LEV > 11.0)
             &VOL = 9.287*&LEV - 30.660
          else
             &VOL = 0.416*&LEV*&LEV + 0.135*&LEV + 19.546;
          make (computation    attr = volume;     object = T07F03;
                value = &VOL);
   };
```

4. In the Pascal-like OPS83 language, rule-based reasoning can easily be combined with algorithmic problem-solving, which is usually more efficient.

developments.

Artificial intelligence, progressing from expert system shells to process-control systems, knowledge-aided design, and special-purpose knowledge systems (Fig. 5), branches out into some important areas—knowledge acquisition, for example. However, the most ambitious, and possibly the most important, outcome of expert systems will be the steps toward software automation.

Probably the first step toward specialized, semicustom expert systems will be seen in the field of process control. Failure of a pump in a refinery or a nuclear power plant can lead to an overwhelming chain reaction of alarms. Military command and control systems attempt to solve similar problems—perhaps a massive influx of data from sonar buoys—that must be predigested to facilitate a human decision. Process control can now benefit from such research, heavily funded by the Pentagon's DARPA group.

Not surprisingly, the first major control system (to be released in the spring) comes from a hardware manufacturer—Lisp Machines Inc. (Los Angeles, Calif.). As a real-time system, the Picon requires special hardware. A 68010-based auxiliary processor handles the incoming data stream and readies it for evaluation by an expert system that runs on the main Lisp processor. The latter finally displays reasonable alternatives for the operator to choose from.

Expert systems will soon become standard in many production lines

Several electronics companies are developing process-monitoring systems for internal use. Hewlett-Packard Co. (Palo Alto, Calif.) uses a prototype system to monitor chip production. As it accumulates data from the many processes it follows, the machine actually learns from past experience by correlating test results with chip performance during the test.

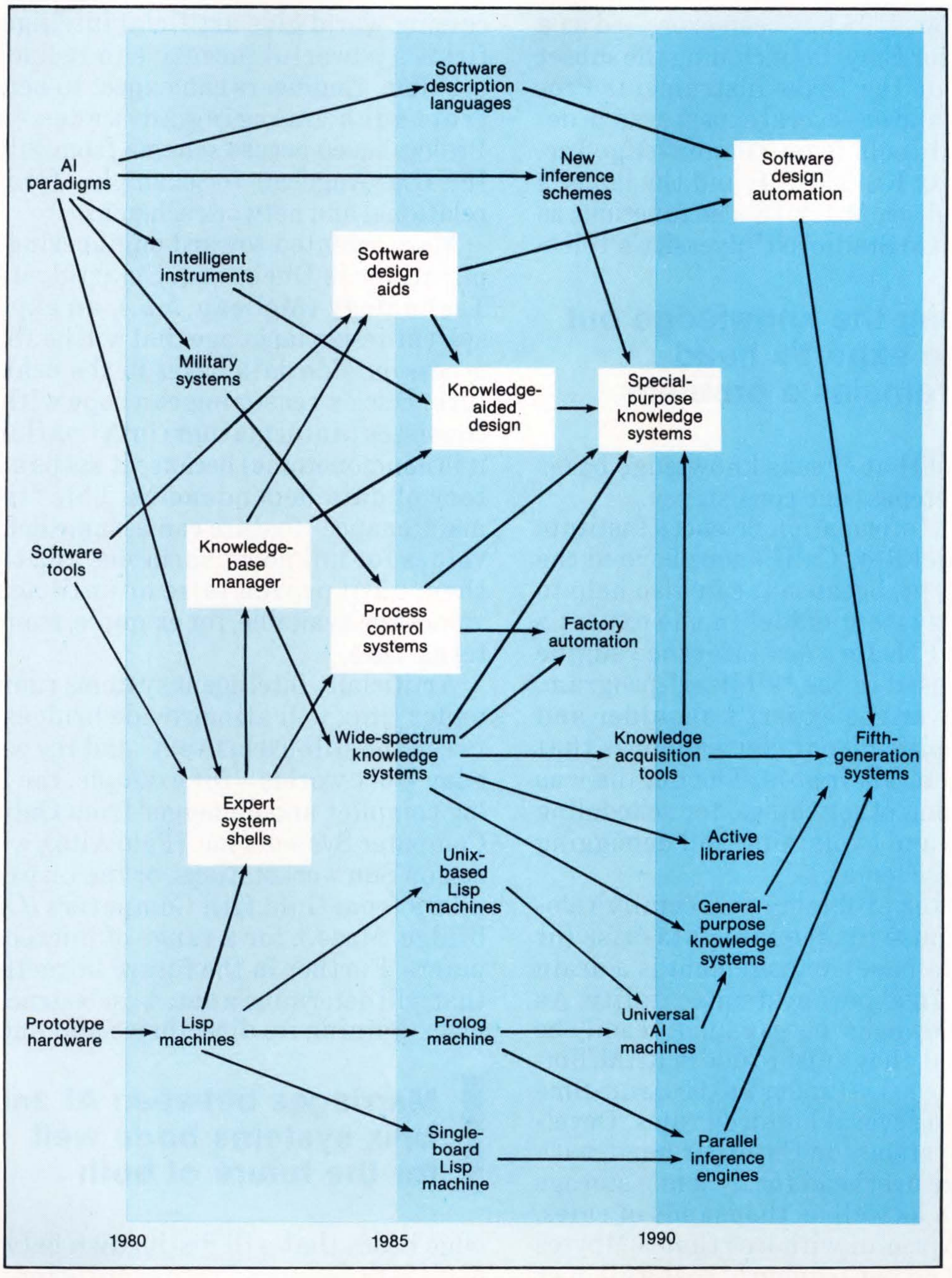
Because the interpretation of both test and process-control data requires years of experience, such applications exemplify the advantages of expert systems. As one of the production engineers sums up: "Now I don't get emergency calls at 2:00 a.m. anymore." It is a safe bet that process control systems in IC manufacturing also will catch on.

Only if standards for knowledge bases emerge, can AI systems blossom

As IC design techniques get ever more complex, even computer-aided tools can become more demanding and slower. Artificial intelligence techniques will come to the rescue. They not only can render the user interface a lot more amicable but often can speed up execution by pruning the range of possible solutions. Furthermore, knowledge bases complement the user's own experience with that culled from notable experts. Such knowledge extraction is, unfortunately, so tedious still that the transition from computer-aided design to knowledge-assisted design remains a somewhat distant promise.

However, there may be a breakthrough in the next few years, propelled by new tools for knowledge extraction and knowledge management. Late this summer, Boeing Computer Services Co. (Seattle, Wash.) is expected to introduce the Expertise Transfer System, or ETS, which permits anyone with some computer experience to construct a knowledge base without the help of a knowledge engineer.

Unlike shell systems—which often purport to facilitate the same task—the system will concentrate on the transfer of knowledge, without prejudging the manner in which that knowledge will be ap-



5. Expert systems represent but one branch in the evolution of AI-based tools. But most future knowledge systems of special interest to engineers (highlighted) are likely to spring from that branch.

plied. So far, ETS has been exercised as a front end for Emycin (including the subset available on the Texas Instruments Professional) and on several expert system development tools from Teknowledge Inc. (Palo Alto): KS-300, S.1, and the latter's IBM PC subset, M.1. ETS also functions as a front end to Stanford University's Teiresias, a tool that checks knowledge bases for completeness and consistency.

Getting the knowledge out of the expert's head still remains a problem

Work at Information Sciences Institute (Marina del Rey, Calif.) goes beyond the ETS concept, because it can also help to clarify a system model in the expert's mind. Its FIE forward inference engine has been used in the "kibitzer" program, looking over the expert's shoulder and quickly pointing out consequences that follow from his inputs. The engine was tried, among other things, for scheduling problems and explaining and debugging data-base schemas.

The latter problem is especially relevant, because inadequate data-base (or knowledge-base) management is a drain on many an expert system's vitality. As long as knowledge bases cannot readily be partitioned, they must reside in RAM, limiting inexpensive (under $10,000) run-time systems to several hundred rules. Development systems, on the other hand, with their large overhead for dynamic storage allocation as well as thousands of rules, are rarely useful with less than 4 Mbytes of RAM and consequently cost well over $50,000. Mass storage would ease those burdens.

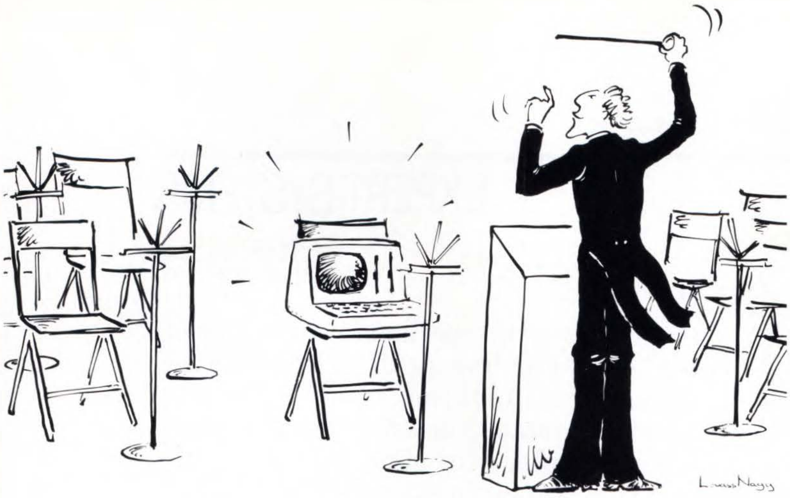
It appears that the storage problem is about to yield on several fronts. Perhaps most important is the ability of expert systems to access conventional data bases. The financial resources of the data processing world give artificial intelligence firms a powerful incentive to tackle the problem. Engineers can expect to benefit from such emerging advances—the Prolog-based access scheme from Silogic Inc. (Los Angeles), for example—for both relational and network schemas.

More oriented toward engineering applications is Duck from Smart Systems Technology (McLean, Va.), an expert-system design language that will be able to access outside data bases in the near future. Duck's reasoning can cope with inconsistent information (in AI parlance, it is nonmonotonic) because it keeps a history of data dependencies. This "truth maintenance" feature can assume default values for unknown variables and trace them until proven false or until actual values are available, for example, from external files.

Artificially intelligent systems running under Unix will also provide bridges between the still-exclusive AI and the workaday Unix worlds—for example, the Prolog compiler and debugger from Quintus Computer Systems Inc. (Palo Alto), which run on Sun workstations, or the Lisp compilers from Gold Hill Computers (Cambridge, Mass.), for a range of microcomputers. Further in the future lie methods that will determine a data base's structure by examining its directories and knowledge bases that will distinguish between different forms of representation: assertions (facts), constraints (conditions), and rules, together with their certainty factors.

Marriages between AI and Unix systems bode well for the future of both

As AI-based systems tackle an ever-growing spectrum of chores, even transitory data kept in main memory can get out of hand. For real-time analysis of speech,



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EPROM Programmers let you program, verify, compare, read, display EPROMS but cost less because they communicate through your personal computer or terminal. No personality modules! On-board intelligence provides menu-based setup for 34 different EPROMS, EEPROMS and MPUs (40-pin devices require socket adaptors). Self-contained unit with internal power supply, RS-232 interface, Textool ZIF socket. Driver software (sold separately) gives you access to all programmer features through your computer, lets you download cross-assembler output files, copy EPROM to disk.

Model 7228 Advanced Programmer —Supports all PROM types listed. Super-fast "adaptive" programming algorithm programs 2764 in 1.1 minutes.

Model 7128 Standard Programmer — Lower-cost version of 7228. Supports all PROM types except "A" versions of 2764 and 27128. Standard programming algorithm programs 2764 in 6.8 minutes.

Avocet Cross-assembler	Target Microprocessor	CP/M-80	CP/M-86 IBM PC, MSDOS**
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XASM05	6805	200.00	250.00
XASM09	6809	200.00	250.00
XASM18	1802/1805	200.00	250.00
XASM48	8048/8041	200.00	250.00
XASM51	8051	200.00	250.00
XASM65	6502/65C02	200.00	250.00
XASM68	6800/01, 6301	200.00	250.00
XASM75	NEC 7500	500.00	500.00
XASM85	8085	250.00	250.00
XASM400	COP400	300.00	300.00
XASMF8	F8/3870	300.00	300.00
XASMZ8	Z8	200.00	250.00
XASMZ80	Z80	250.00	250.00
XMAC682 *NEW*	68200	595.00	595.00
XMAC68K *NEW*	68000/68010	595.00	595.00

Model 7956 and 7956-SA Gang Programmers — Similar features to 7228, but program as many as 8 EPROMS at once. 7956-SA stand-alone version copies from a master EPROM. 7956 lab version has all features of stand-alone plus RS-232 interface.

EPROM: 2758, 2716, 2732, 2732A, 2764, 2764A, 27128, 27128A, 27256, 2508, 2516, 2532, 2564, 68764, 68766, 5133, 5143. **CMOS:** 27C16, 27C32, 27C64, MC6716. **EEPROM:** 5213, X2816A, 48016, I2816A, 5213H. **MPU (w/adaptor):** 8748, 8748H, 8749, 8749H, 8741, 8742, 8751, 8755.

7228	**Advanced Programmer**	**$ 549**
7128	**Standard Programmer**	**429**
7956	**Laboratory Gang Programmer**	**1099**
7956-SA	**Stand-Alone Gang Programmer**	**879**
GDX	**Driver Software**	**95**
481	**8748 Family Socket Adaptor**	**98**
511	**8751 Socket Adaptor**	**174**
755	**8755 Socket Adaptor**	**135**
CABLE	**RS-232 Cable (specify gender)**	**30**

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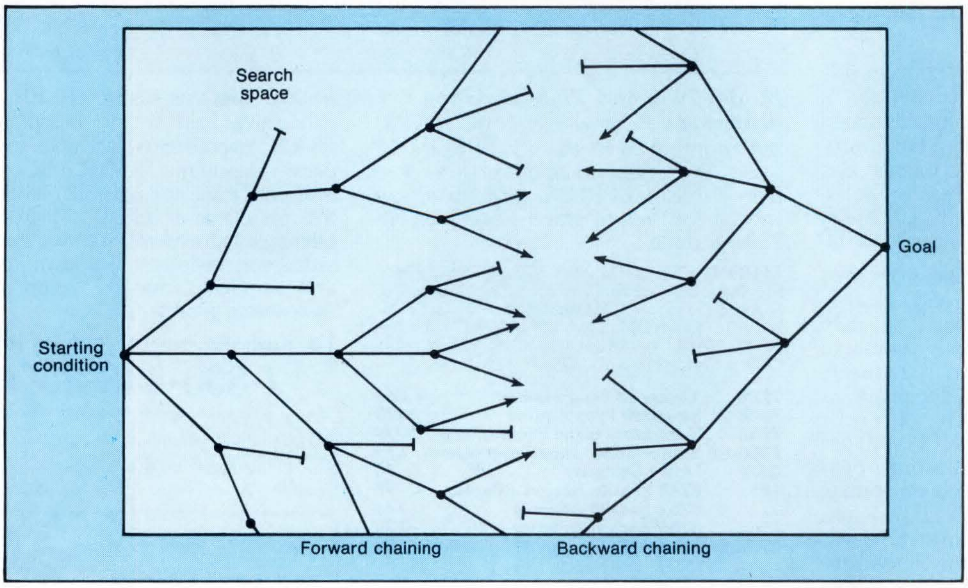
sonar signals, or images, rapid access to the fleeting data stream is just as essential as it is difficult. The most promising solution is probably the "blackboard," which functions somewhat like a relational data base. But in addition to the two normal axes—in speech processing, abstraction level (from phoneme to sentence), and degree of certainty—a third dimension represents time. While popular with researchers, no commercial blackboard system is available yet, but this is bound to change.

Once they have sorted out the knowledge base mess, artificial intelligence workers will be ready to tackle the ultimate knowledge base application: active libraries. Once this goal is reached, those in search of knowledge will no longer have to tunnel their way through racks of books or binders. The artificial librarian will query the patron—perhaps even in spoken English—and serve up all he ever wanted to know about a subject.

Optical storage, currently the only practical technology for such a library, will first find a place in expert systems—initially in the military and eventually in the home. While it is unlikely that troubleshooting in the engineering laboratory will quickly benefit from such huge knowledge bases, new insights into knowledge representation and diagnostic techniques could well pay dividends.

As knowledge bases grow, optical mass storage must offload RAM

If artificial intelligence evolves as expected, expert-system shells will lead to



6. The primary purpose of an inference engine is to reduce the "search space" in which all possible solutions lie. By combining paradigms (here, forward and back ward chaining), future systems can be made more effective.

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2005 vs. Competition

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Frequency Range	1 MHz-4.5 GHz	10 MHz-4.3 GHz	10 MHz-4.3 GHz
Step Attenuator	Standard	Not available	Optional $850
Output flatness	+/-.75 dB	Not specified	Not specified
Harmonic Markers	1, 10, 50, 100 & 500 MHz Standard	1, 10, 50, & 100 MHz Optional @ $525	1, 10, & 50 MHz
Marker Range	1 MHz-4.5 GHz	Limited	Limited
Marker Accuracy	.005% (+45 kHz >2.5 GHz)	.01%	.0005%
GPIB: Frequency **GPIB: Amplitude**	$1,500 $1,100	$1,100 Not available	$955 Not available

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CIRCLE 68 FOR DEMONSTRATION
CIRCLE 69 FOR LITERATURE

fifth-generation computers. Several intermediate steps along this path will affect design engineers. For example, wide-spectrum knowledge systems—those that can reason in several different modes—are already in evidence and are bound to influence the evolution of special-purpose expert systems. The latter represent a step beyond knowledge-assisted design tools,

Expert systems have begun to embellish today's CAE with another dimension

because they will require much less human interference. By the end of this decade, the growing complexity of engineering designs will simply mandate the utilization of such special-purpose systems.

General-purpose knowledge systems, on the other hand, represent an early form of the fifth-generation machine: a moderately intelligent assistant for everyday chores. But in this area, prediction turns more into speculation and is best left to other media.

As even smarter artificial assistants invade the design labs, fewer engineers will be busy designing products, and more will be designing the AI tools that help design the products. For hardware tools, the trends are clear: AI design systems will become more powerful, while delivery vehicles will remain simple—in most cases, personal computers will suffice. Teknowledge's M.1, for instance, is written in Prolog while its big brother, S.1, requires a Lisp machine.

In fact, Prolog is playing a growing role in artificial intelligence research, even though no Prolog machines are yet available. Most likely, microprogrammable workstations will serve the purpose at first, but architectures optimized for Prolog are already on the drawing board. At the same time, Lisp machines will continue to become both more compact and more powerful.

The popular low-end Lisp machine from Xerox Corp. (Stamford, Conn.), nicknamed Dandelion, is about to be upgraded with a new processor and 2.5 to 3 Mbytes of RAM. Little more is known about the new workstation, which has been dubbed the Dandetiger. Competitive pressures in the Lisp machine field will accelerate plans for single-board systems, thereby leveling the road for multiprocessor machines. A forthcoming 2-μm Lisp chip from Texas Instruments Inc. (Dallas) already stakes out this direction.

Although the Japanese fifth-generation project relies heavily on massive parallelism, American AI researchers are not convinced that this approach is viable. Present reasoning paradigms, at least, are largely sequential, because they descend through a search tree (Fig. 6). Usually, the number of branches that can be tested simultaneously is rather modest, and often it becomes necessary to backtrack for several levels. All work invested in searching a blind alley is wasted, regardless of the size of the search crew.

A dissenting voice from Carnegie-Mellon University, however, reopens the possibility of massive parallelism. Instead

Japan's fifth generation stresses massive parallel CPUs, but many disagree

of trying to limit the search space cleverly, researchers suggest simply proceeding with an exhaustive search, using very simple processing elements of a few gates each. From a network of such marker-passing nodes, called NETL, the present Boltzman machine has evolved. While still immature, this approach—which tries to emulate the human brain—could influence developments in the next five years.

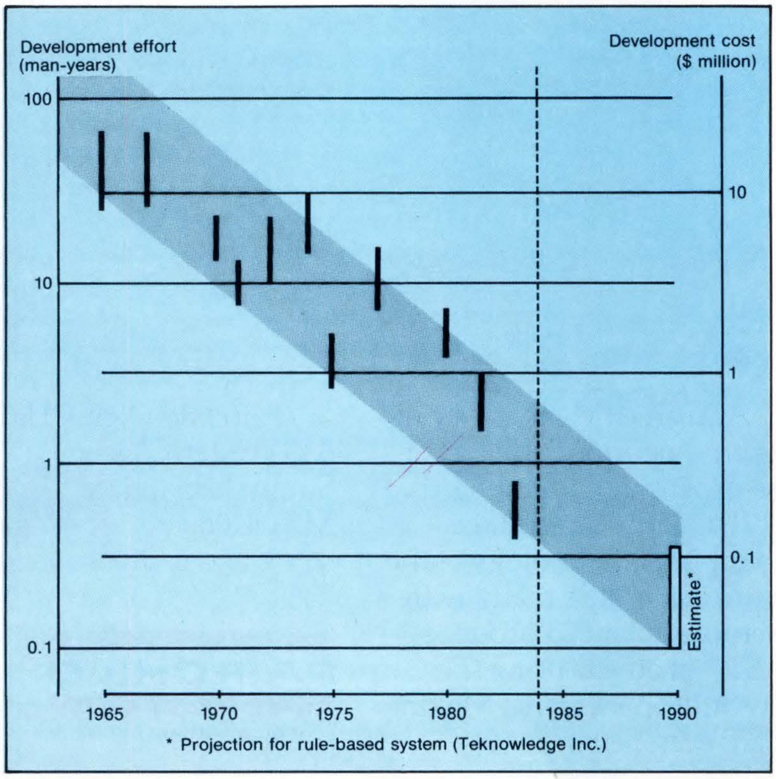
Meanwhile, conventional von Neumann machines, which have been unpopular

with the artificial intelligence community, are staging a comeback. New Lisp and Prolog compilers have proven them quite capable of fast execution, even though they still are less flexible during the development phase of AI software. If OPS83, with its Pascal-like properties, catches on, any number of engineering workstations could become suitable vehicles for expert systems.

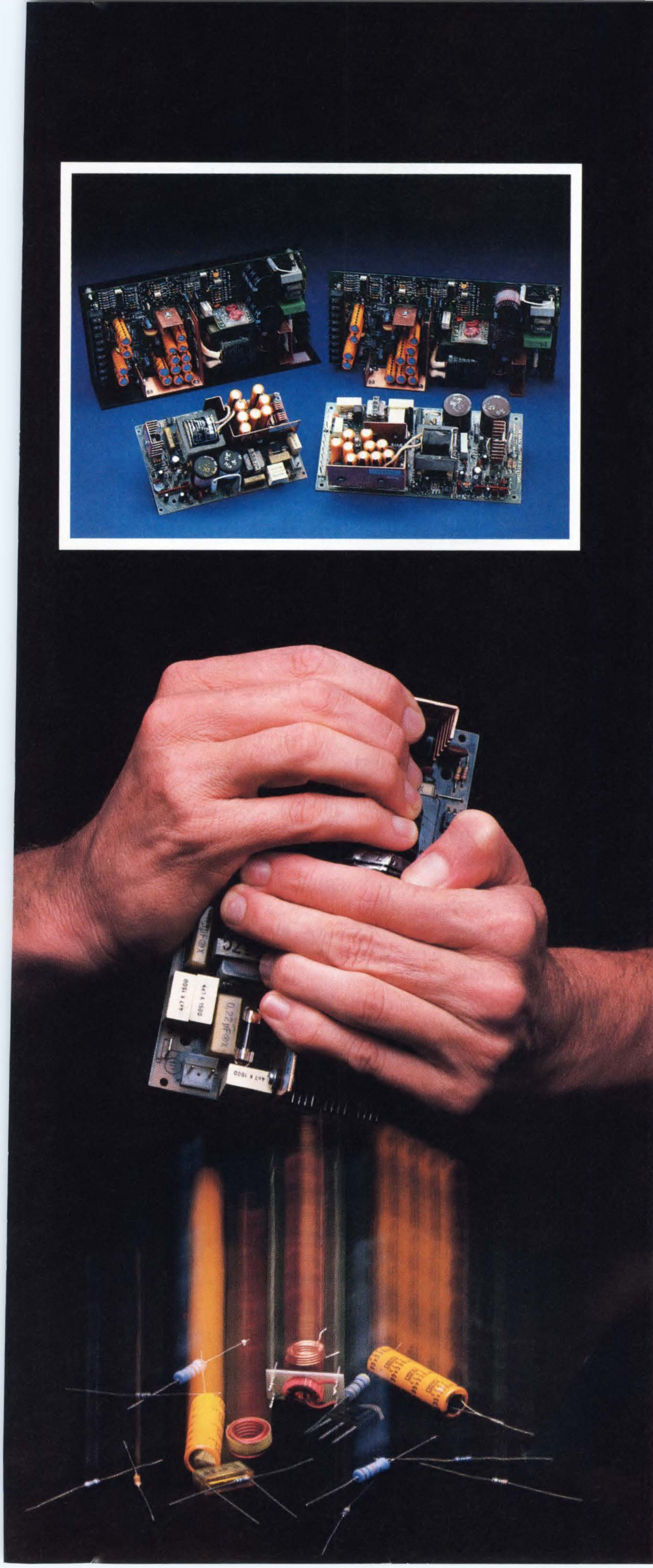
To gain insights into parallelism in forward-chaining systems of the OPS family, Carnegie-Mellon has embarked on the Production System Machine (PSM) project. Simulations with several expert systems (including VLSI design and configuration management) show that OPS83 programs begin to saturate the system at 8 to 16 parallel processors, yielding a fivefold to tenfold speedup. By combining ECL technology, a RISC architecture, and parallel processing, production-type expert systems can be expected to run 100 to 200 times faster by 1990.

While the evolution of efficient hardware was responsible for the emergence of an artificial intelligence industry, better hardware alone cannot guarantee its future. After all, expert (or knowledge) systems are mostly software packages, and software represents the bulk of development costs.

Since their beginnings in the mid-1960s, expert systems have, fortunately, become cheaper to build—in fact, by two orders of magnitude (Fig. 7). To keep up the momentum through the rest of the decade, when a 500-rule system should cost only $50,000 to develop, better design tools will be needed. Some—like new languages and knowledge



7. Since their first appearance, expert systems have become much cheaper to develop. The trend is expected to continue, dropping development costs to $100-200 per rule by 1990.



transfer tools—have already been mentioned, but they are not enough.

As expert systems get bigger, they begin to exhibit the same symptoms as traditional software: bugs, inconsistencies, and maintenance problems. But unlike, for example, the situation with aerospace software, artificial intelligence programs have been largely one-man shows, and the whole AI atmosphere has never been conducive to team efforts.

Fortunately, the fierce individualism of artificial intelligence workers has generated a wide spectrum of productivity tools, which are largely responsible for the dramatic cost reductions already attained. The time has now come to combine the best of them into consistent software design environments and discard the rest. Economic pressures on the young AI industry have defused some of the once-religious fervor attached to given tools, and a further melding of concepts and techniques can be expected in the future.

However, when it comes to the software, two distinct, though unequal, camps remain. The majority pursues an evolutionary path, while a minority stakes its future on a revolutionary breakthrough. Both camps can produce impressive evidence to support their approaches.

Of all expert systems, those for software design pose the toughest problems

Evolutionists need only point to their tremendous advances, from windows and mice to object- and class-oriented software design. Many of these tools are migrating into the software community at large—probably the surest measure of success. But to forge a comprehensive software engineering environment from individual tools will take years.

Several companies have, nevertheless, taken up this challenge. Boeing Computer Services, for one, is planning to integrate its artificial intelligence tools with more conventional tools like Argus (ELECTRONIC DESIGN, Feb. 9, 1984, p. 42). Advanced Information and Decisions Systems (Mountain View, Calif.) intends to provide means for program synthesis by 1990—based on graphics and data-flow concepts. Computer*Thought Inc. (Plano, Texas) is currently offering intelligent debugging tools for Ada, but as the knowledge base grows, a complete environment will emerge.

For better software tools some bet on evolution, others want to start over

In addition, a growing number of firms are building software tools for in-house consumption, and many follow the knowledge-engineering tack. Communications companies in particular, where often over 500 software designers work on a single system, need both a disciplined and a productive approach to software development. In the U.S., AT&T, GTE, and ITT and in Sweden, Ericsson, are embarked on such projects, but find progress exceedingly slow.

On the other hand, Tartan Laboratories (Pittsburgh, Pa.) leans toward the revolutionary paradigm. The company develops the compilers it sells in a semi-automated fashion, using its own expert systems. The compiler designer specifies the software's function in a very high-level language, and a computer has the job of producing the actual code.

However, even though compiler design is by itself a rather narrow domain of expertise, Tartan uses several different description languages to define syntax and semantics of the languages to be compiled and of the hardware on which a compiler will run (Fig. 8). Because compilation—especially parsing and flow analysis—

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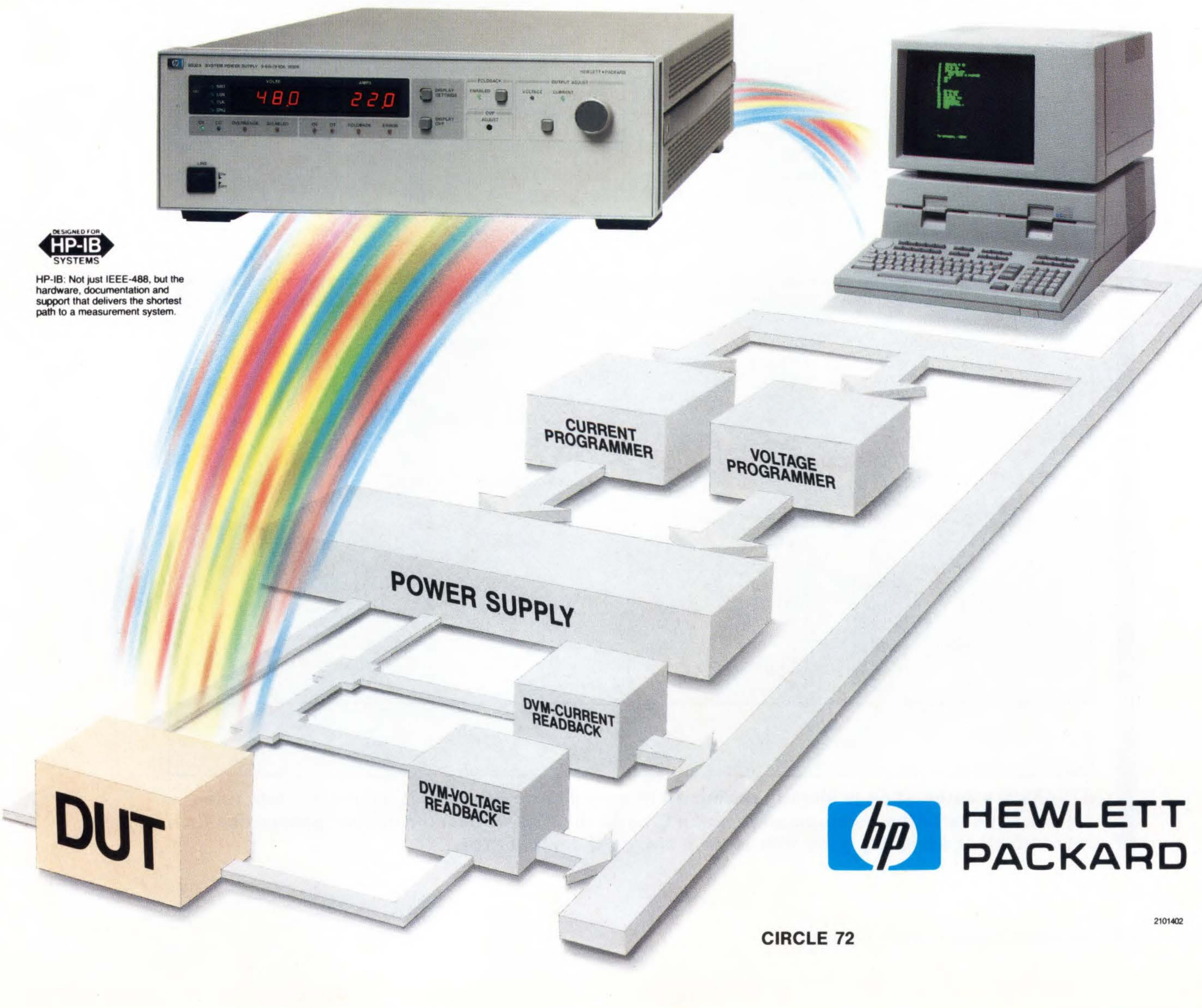

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CIRCLE 72

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obeys mathematical rules, Tartan's expert system must handle reasoning from first principles as well as rules.

Partial automation at Tartan has raised the compiler designer's productivity by an order of magnitude. But although it will take several more years to implement full automation, it is expected to add only another factor of two to productivity. For the time being at least, some natural intelligence greatly enhances proficiency of the artificial kind.

Even such pioneers of revolutionary software automation as the Kestrel Insti-

EXAMPLE PRODUCTIONS

```
$1:(mult $2:(plus $4:ANY $5:CONST) $3:CONST) =>
    SetOp[$1, plus] ;
    Alter[$2, mult, [$4,NewConst[Val[$5]*Val[$3]]];
%%
$1:(geq  $2:ANY  $3:ONE) =>
    Alter[$1, gtr, [$2,NewConst[0]]];
%%
$1:(if  $2:ANY  $3:ONE  $4:ZERO) =>
    CopyNode[$1, $2];
%%
```

(a)

EXAMPLE C PROGRAM

```
int a[10];
int x;
example ( ) {
    register i;
    for (i=1; i<=10; i++) x += a[i+1] >= 1 ? 1 : 0 ;
}
```

(b)

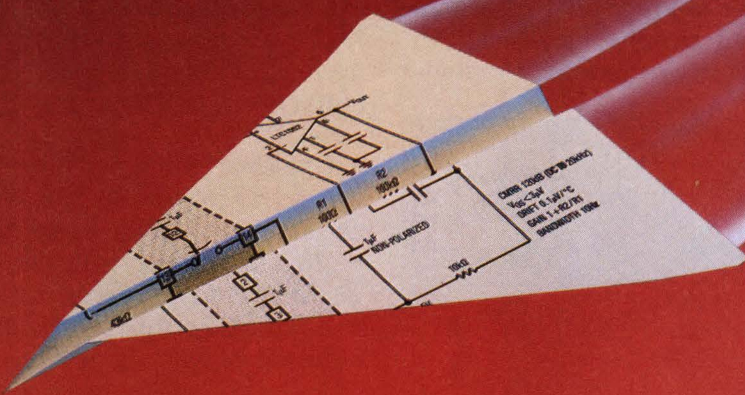
OUPUT FROM STANDARD COMPILER	OUPUT FROM TARLAN COMPILER

<pre>_example:
        .word   L14
        jbr   L16
L17:   movl $1,r11
L20:   cmpl   r11,$10
        jgtr   L19
        add13 $1,r11,r0
        cmpl   _a[r0],$1
        jlss   L9999
        movl $1,r0
        jbr   L9998
L9999: clrl   r0
L9998: add12   r0,_x
L18:   incl   r11
        jbr   L20
L19:   ret
        .set   L14,0x800
L16:   jbr   L17</pre>
	<pre>_example:
	        .word 0
	        movl $1,r4
	L1: clrl r0
	        tstl _a+4[r4]
	        bleq L2
	        incb r0
	L2: addl2 r0,_x
	        aobleq $10,r4,L1
	        ret</pre>

(c)

8. Software automation is already paying off in compiler design. In this example, three rules (a) are applied to the compilation of some C code (b). The AI-based compiler generates much more efficient assembly code than does a standard compiler (c).

A NEW APPROACH TO INSTRUMENTATION AMPLIFIERS.



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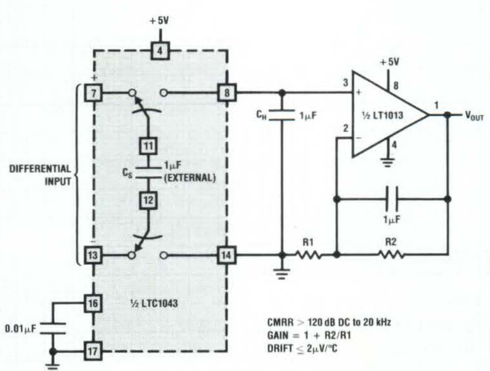

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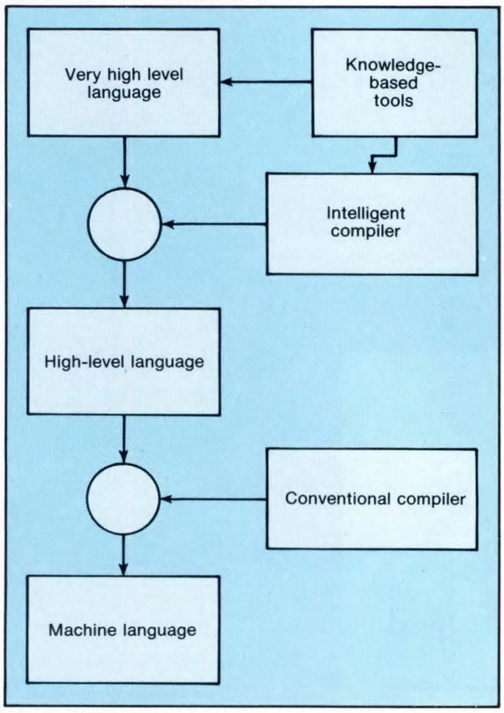
CIRCLE 73

tute (Palo Alto) and the Information Sciences Institute are not quite ready to eliminate human interaction during software design. In fact, they prefer to regard their approach as rapid prototyping, followed by stepwise refinement.

A new company, Reasoning Systems Inc. (Palo Alto) is planning to put the Kestrel research to the test, perhaps as early as this summer. Currently under beta testing, the start-up's automated program synthesis environment spans the whole software life cycle, from specification to maintenance. Domain-specific "knowledge packs" are planned for VLSI design, system programming, equipment testing and project management, among others.



9. Knowledge-based tools can greatly speed the design of software. By expressing an algorithm in a very high level language, the actual coding in Lisp or Pascal can be left to an intelligent compiler.

Knowledge-based software synthesis proceeds in several steps (Fig. 9). First, the user defines the program logic in a very high level definition language that provides for transformations and high-level data types. The language can be extended, permitting the user to define procedures. An intelligent compiler then produces an efficient, error-free implementation in a high-level language such as Lisp. Both the definition language and the compiler are controlled by the system's knowledge base.

One interesting feature of the system is its ability to synthesize hardware as well as software. During algorithm synthesis, eight additional rules that look at connectivity and data-passing "discover" the architecture most suitable for implementing a given algorithm.

Related to software automation is the science of proving a program's correctness. Proponents claim that correctness proofs will be applied to any physical device that can be fully described with software. Good examples are logic circuits, especially the often exceedingly complex VLSI, and soon ULSI (ultralarge-scale-integration) chips. In theory, designs in any field—mechanical, aeronautical, or chemical—can be proven right or wrong. The catch is that only the software model can be analyzed, and if the model fails, so does the proof.

This rather theoretical branch of AI is one that flourishes in Europe, perhaps more than in the States. In fact, it may well turn out to be the one artificial intelligence specialty where the Europeans will introduce practical applications first. At the University of Kaisers-lautern in West Germany, for example, correctness proofs will be harnessed for teaching mathematics and electronic circuitry, in addition to program verification.□

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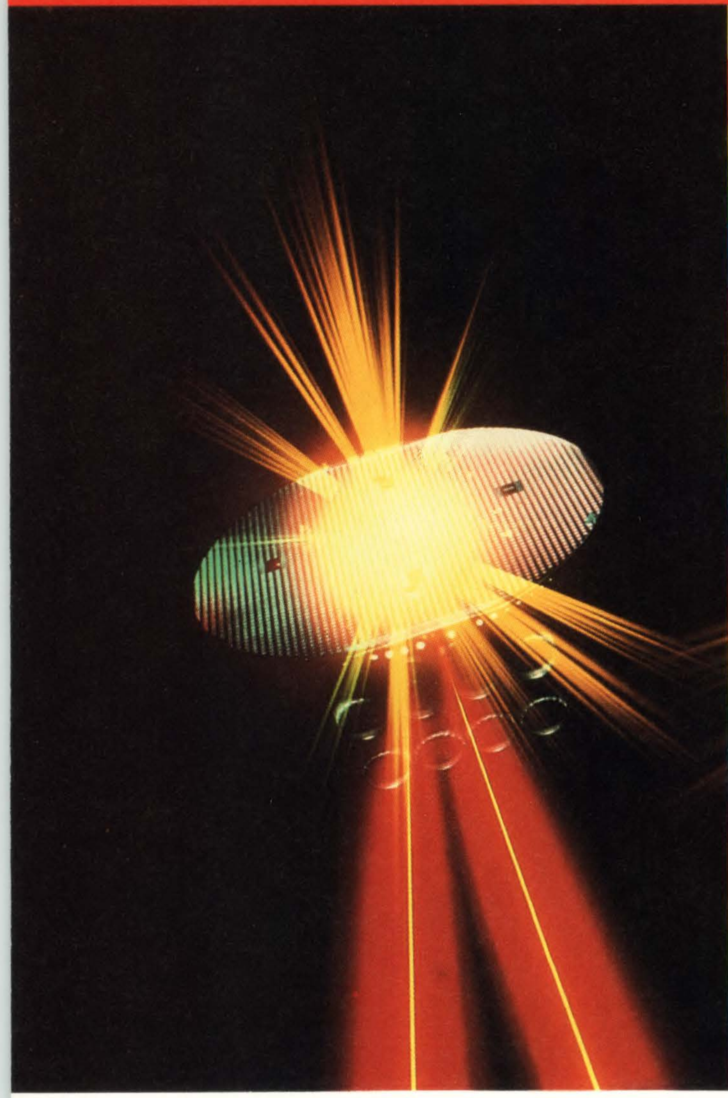

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HCT20	Dual 4-Input NAND Gate
AND GATES	
HC/HCT08	Quad 2-Input AND Gate
HC/HCT11	Triple 3-Input AND Gate
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HC/HCT365*	Hex Buffer/Line Driver; 3-State
HC/HCT366*	Hex Buffer/Line Driver; 3-State; Inverting
HC/HCT367*	Hex Buffer/Line Driver; 3-State
HC/HCT368*	Hex Buffer/Line Driver; 3-State; Inverting
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HC4050	Hex HIGH-to-LOW Level Shifter
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HC/HCT175	Quad D-Type Flip-Flop with Reset
HC/HCT273	Octal D-Type Flip-Flop with Reset
HC/HCT374*	Octal D-Type Flip-Flop; 3-State
HC/HCT534*	Octal D-Type Flip-Flop; 3-State; Inverting
HCT564*	Octal D-Type Flip-Flop; 3-State; Inverting
LATCHES	
HC/HCT373*	Octal Transparent Latch; 3-State
HCT533*	Octal Transparent Latch; 3-State; Inverting
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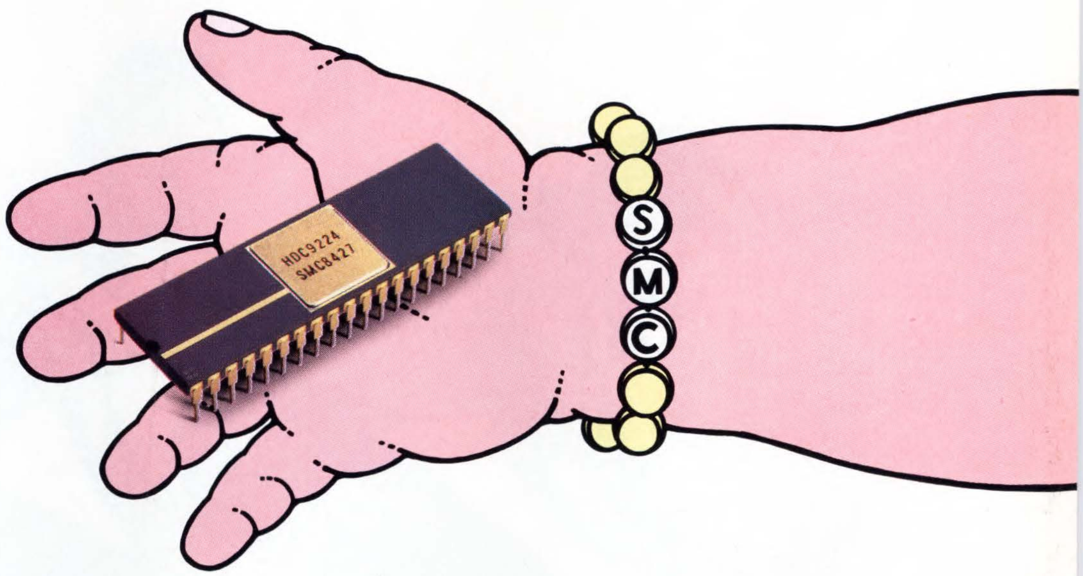

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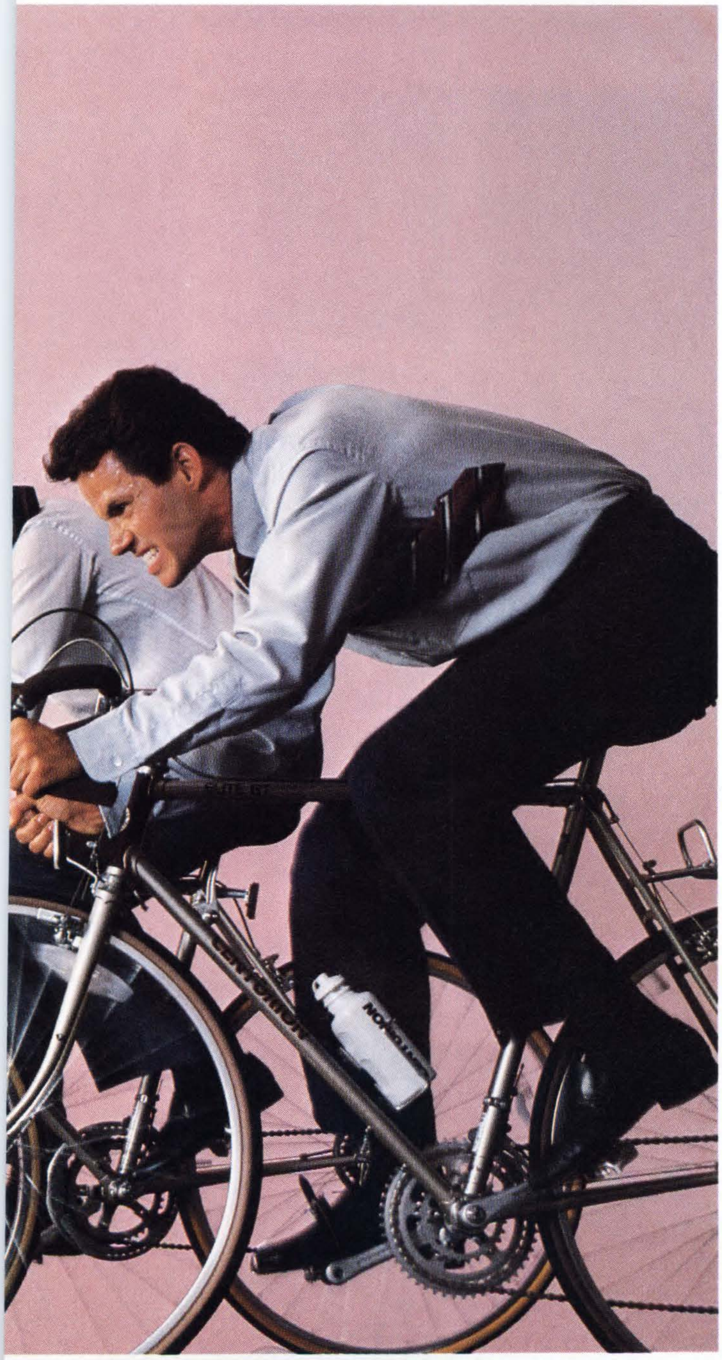

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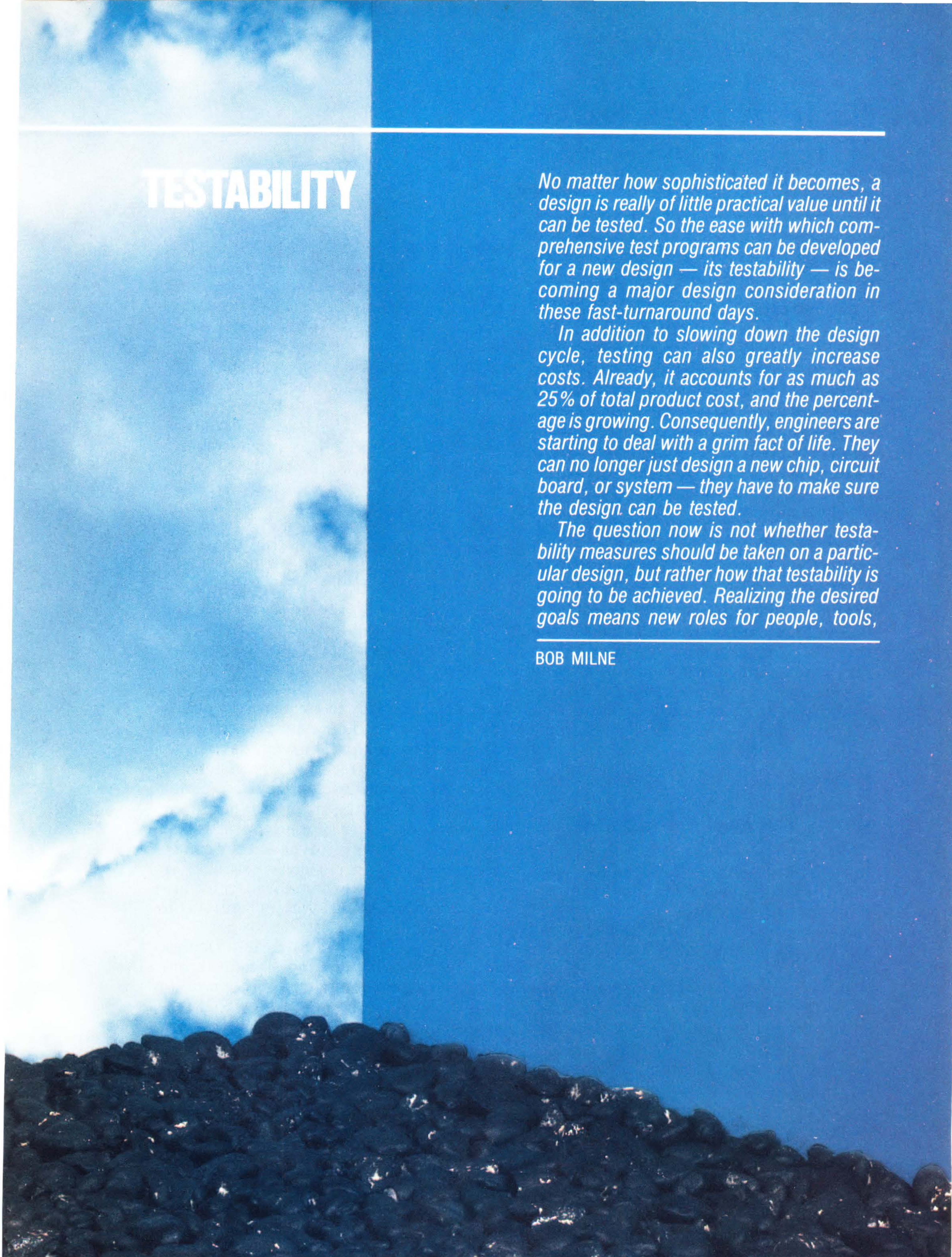

TESTABILITY

No matter how sophisticated it becomes, a design is really of little practical value until it can be tested. So the ease with which comprehensive test programs can be developed for a new design — its testability — is becoming a major design consideration in these fast-turnaround days.

In addition to slowing down the design cycle, testing can also greatly increase costs. Already, it accounts for as much as 25% of total product cost, and the percentage is growing. Consequently, engineers are starting to deal with a grim fact of life. They can no longer just design a new chip, circuit board, or system — they have to make sure the design can be tested.

The question now is not whether testability measures should be taken on a particular design, but rather how that testability is going to be achieved. Realizing the desired goals means new roles for people, tools,

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techniques, and equipment. Moreover, as the workstations design data base gets linked to prototype evaluation and manufacturing tests the loop is getting closed on the whole design and test cycle.

Right now, CAE tools give engineers the power to create complex designs that far exceed the capabilities of the tools used to generate and analyze test programs. ATPGs (automatic test program generators), for instance, do just fine with combinatorial logic but fall apart when applied to the sequential logic that forms the basis for most modern designs. Similarly, fault simulators, which grade the effectiveness of test vectors, have yet to model the unique failure modes of CMOS logic.

Forced to work with these handicaps, engineers will employ special design techniques to overcome the limitations of the test tools. Structured design approaches, for example, transform sequential circuits into combinatorial ones for test purposes, simplifying test program generation.

What's more, as VLSI designs continue to push the gate-to-pin ratio, built-in testing will become ever more important. Finally, at the board level, many engineers will be making more use of the various ad hoc techniques that make a design easier to test.

Workstations prepare to play a key role in making designs testable

In considering the whole testability picture, the engineering workstation will play a key role. In the few years that workstations have been available, engineers have taken to them like ducks to water. In fact, the introduction of the IBM PC AT has everyone saying that powerful computers are now cheap enough to really legitimize the idea of a workstation on every engineer's desk.

From a testability standpoint, however, workstations used just for design—without considering testability—can be looked upon as a way to let a designer create more testing problems faster. Fortunately, workstations are taking another path, that of linking design and test (Fig. 1).

Thanks to the workstation, people, techniques, tools, and equipment will team up to do the testability job right. Importantly, the workstation's design data base will increasingly be linked to automatic test equipment and prototype evaluation hardware. Until recently, for example, an engineer who sat down at a workstation and designed a custom device really had no good way to evaluate his prototype, unless, of course, he had access to a million-dollar chip tester. Regardless of how good a design is, the prototype can be considered untestable unless the engineer has access to hardware to verify the physical part.

Specialized test equipment for prototype evaluation is starting to appear—a trend that is likely to escalate very quickly. This new breed of tester is specifically designed to tie into the CAE data base. Basically, the tester's pattern generator takes test vectors developed by a simulator and applies them to the prototype device. Meanwhile, the tester also captures test results from the prototype so they can be compared with the responses predicted by the simulator. In other words, the engineer has a mini-ATE system right at his workstation.

One such unit, the IMS 1000 Design Master from Integrated Measurement Systems (Beaverton, Ore.), is complete right down to the test fixture. Up to 192 inputs or outputs can be handled by the unit, which supplies test patterns at rates up to 20 MHz (40 MHz optional). Importantly, the outputs from the device under test can be compared in real time with those predicted by the simulator.

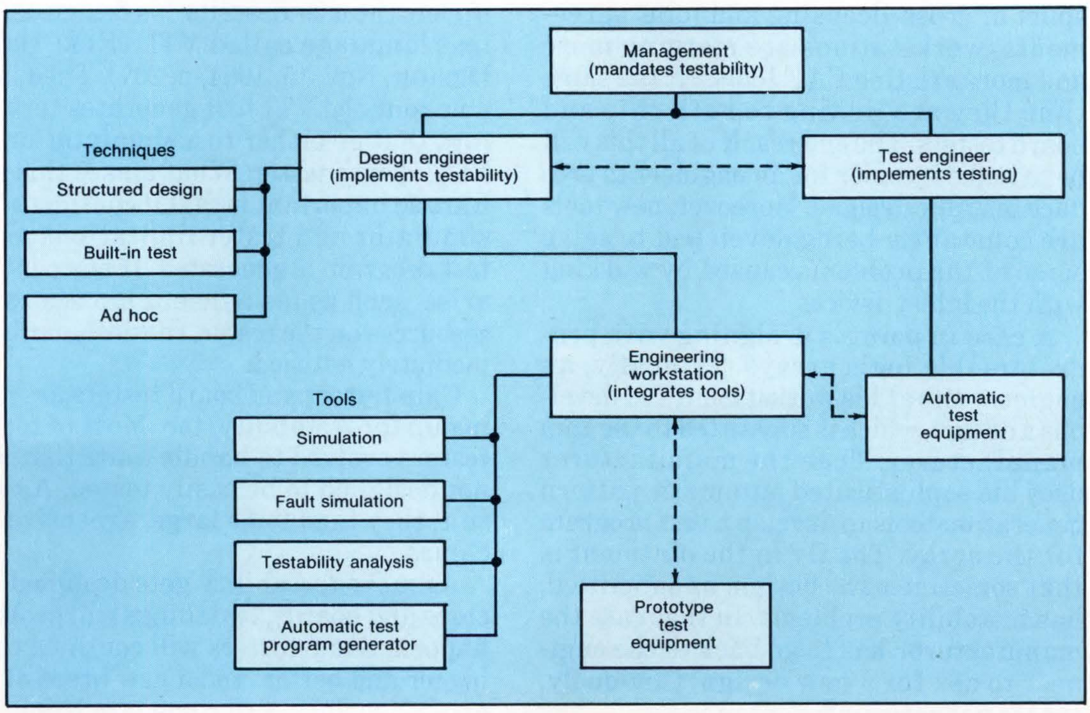
Another prototype tester actually becomes an integral part of a simulator. Dubbed the Chipchecker, the unit from

HHB-Softron Inc. (Mahwah, N.J.) ties into the company's Cadat logic and fault simulators and is driven through commands from the simulator. This allows the engineer to decide whether to apply the simulator's test vectors to a software model or download them to the Chipchecker to stimulate the physical part.

Workstations are also starting to offer their own optional prototype evaluation hardware. Users of the Idea series of engineering workstations from Mentor Graphics Inc. (Beaverton, Ore.), for example, can now equip themselves for logic analysis and pattern generation by adding the company's recently introduced HVS (hardware verification system) option.

Given the importance of prototype evaluation and the increasing use of custom and semicustom parts, there is likely to be a continuing flurry of activity in this area. The instrument houses in particular are steeped in the appropriate hardware technology. A recently introduced system, the Caesar 400 from Dolch Logic Instruments Inc. (San Jose, Calif.), packages existing instrument plug-ins such as word generators, logic analyzers, and in-circuit emulators from the company's Atlas and Colt products in a manner that is clearly intended to link to workstations. In fact, the company recently announced an agreement to supply an instrument package for CAE System's 2000 workstation.

In some cases all it takes is a software package to adapt existing instruments for prototype evaluation. This year, for instance, Tektronix Inc. (Beaverton, Ore.) released software that links the pattern generation and logic analysis functions of



1. The engineering workstation is destined to aid testability by uniting all the elements in the design-test cycle. Important links involving designers and test personnel which are just starting to appear are indicated by the dotted lines.

its DAS 9100 system directly to logic simulators.

What's more, both Hewlett-Packard and Tektronix will likely introduce engineering workstations in the near future, although they seem to be in a race to see who introduces last. One thing is certain, there is a lot of speculation about what traditional test and measurement tools, if any, will be included in these systems.

Of course, the real power of workstations lies in the software tools they incorporate, a concern so paramount that the "not invented here syndrome" is fast disappearing. Through an unprecedented spurt of cross-licensing and joint agreements, workstations are merging more and more existing CAE tools. At the same time they are linking to both chip and board testers. The end result of all this will be to make it easier for an engineer to produce testable designs. Moreover, new tools are constantly being developed to solve some of the problems caused by working with the latest devices.

Cross-licensing brings more powerful software into CAE workstations

A case in point is designing with programmable logic arrays. Typically, an engineer sits at his workstation and develops a design, which is submitted to the chip manufacturer. Then the manufacturer uses his sophisticated automatic pattern generation tools to develop a test program for the array. The fly in the ointment is that sometimes the design, as submitted, has testability problems. In that case the manufacturer has to go back to the engineer to ask for a new design. Obviously, that is not a very efficient process.

The answer is to let the designer determine whether the circuit is testable right at his workstation. Toward this end, Data I/O Corp. (Redmond, Wash.) is readying a low-cost ATPG for PAL devices from Monolithic Memories and its alternative sources. The generator will run on the IBM PC or Digital Equipment's VAX computers. Besides creating test vectors directly from the array fuse map, the program generator also tells the designer the degree of fault coverage the test vectors produce, thereby alerting him to any testability problems.

The array manufacturers are not standing still either. New chip designs are incorporating techniques such as the ability to jam load registers to make testability more certain. Testability breakthroughs are being made in the VLSI chip design area too. The idea is to alert designers to possible testing problems as early in the design cycle as possible.

Relatively new chip design software from VLSI Technology Inc. (San Jose, Calif.) lets the user describe his design using a test language called VTL (ELECTRONIC DESIGN, Nov. 15, 1984, p. 207). Then, software dubbed VTI test generates test vectors that go either to a simulator or to a VLSI device tester. What makes this software so important is that it considers both simulator and tester limitations as the test program is generated. If any conflicts arise, such as insufficient pin allocation resources on the tester, the designer is immediately notified.

Chip testers and board testers are gearing up for testability, too. Most of today's testers evolved to handle units that were not designed to be easily tested. As a result, they tend to be large, expensive machines.

As more testability gets designed into chips and boards, two things will probably happen. Some testers will continue to get bigger and better, and a new breed of less expensive units will come into being. The big testers will continue to grow in speed and pin count. Moreover, some really huge amounts of memory will go into these testers to handle the long serial test patterns required by some of the scan designs. Prices, on the other hand, will probably not rise as much as performance. Like computer products, testers will benefit from the low-cost computing power available with the latest technology.

As for the less expensive new breed, built-in testing may turn tomorrow's tester into more of a monitoring unit, with less emphasis on its stimulus capability. Moreover, built-in testing carried to the extreme may very well result in chips that can completely test themselves.

As far as people are concerned, design engineers are changing, at least philosophically. With circumstances forcing them to consider testability, they are starting to get a feel for what the test engineer has been going through all these years. In addition to workstations being linked to testers, communications paths are being opened between design engineers and test engineers. In some cases test engineers may actually supply inputs during the design phase, something that was unheard of not too long ago.

The fundamental change taking place, however, is that test engineers are no longer expected to reverse-engineer a product to develop a test program. That method is just plain impractical with today's designs and even worse with tomorrow's. For this reason all the emphasis on testability is shifting to the design process—where it belongs. The test engineer will still be responsible for automatic test equipment and test programs. But he or she will miss out on some test program generation nightmares, a condition they can probably live with. Of course, these changes will not take place overnight, but they are inevitable, a fact that management is just now starting to realize.

Testability is becoming the responsibility of the design engineer

Testability always has been, and will continue to be, a management responsibility. All too often, however, it has taken a back seat to cost considerations and schedules. The old school of thought was to get the design out of engineering and into production as soon as possible. Riding along with this philosophy was a mystical faith that somehow, along the way, the testing problems would get solved.

Today's more astute managers recognize that the old ways are no longer good enough. What is needed, they realize, is for management to mandate that testability be designed into new products. Once that is done, implementing that policy will be the responsibility of the design engineer.

Each and every design possesses some degree of testability. But when testability is not designed in, the engineer (and everybody else down the line) is stuck with what results. On the other hand, designing for testability reduces the likelihood of unpleasant surprises at test time. Moreover, testable designs are a lot easier to debug initially, an important benefit.

A highly testable digital circuit possesses several key attributes. First, it is easily initialized. Second, it is easily controlled by a small number of test vectors applied to its primary inputs. Together these two attributes determine what is called the controllability of the design.

In addition, the internal states of a highly testable circuit are uniquely and easily identifiable either through its primary outputs or through special test points. This characteristic has come to be known as the design's observability.

Because it has no internal states, and its outputs are a direct result of its present inputs, combinatorial logic shapes up pretty well from a testability standpoint. High fault coverage is readily obtained using ATPGs. The trouble is that everyone is now designing with sequential circuits.

What makes testing them tough is that

the outputs of a sequential logic circuit are determined not only by the present inputs but also by the current internal state, which in turn is a function of both the present and the previous inputs. Couple this fact with the enormous ratio of logic to I/O pins on a VLSI device and it is easy to see why controllability and observability go to pieces. What's more, ATPGs have nervous breakdowns when they work on sequential circuits. The test patterns they come up with do not produce high fault coverage.

So what alternatives exist to automatic test program generators? One method—pseudorandom pattern generation—has been around awhile and is now getting a lot of renewed interest. Well suited to testing combinatorial logic, the technique applies a series of algorithmically generated pseudorandom test patterns to the circuit under test. Then, data compaction techniques such as signature analysis are used on the circuit outputs to verify the response. Because the data compression technique allows a large number of test vectors to be easily generated at high clock rates, random pattern generation is an attractive candidate for on-chip testing schemes.

Manual generation of test patterns is not dead yet either. Often manually generated patterns will be used to supplement those generated automatically or psuedorandomly.

Fault simulation grades how well test vectors spot circuit problems

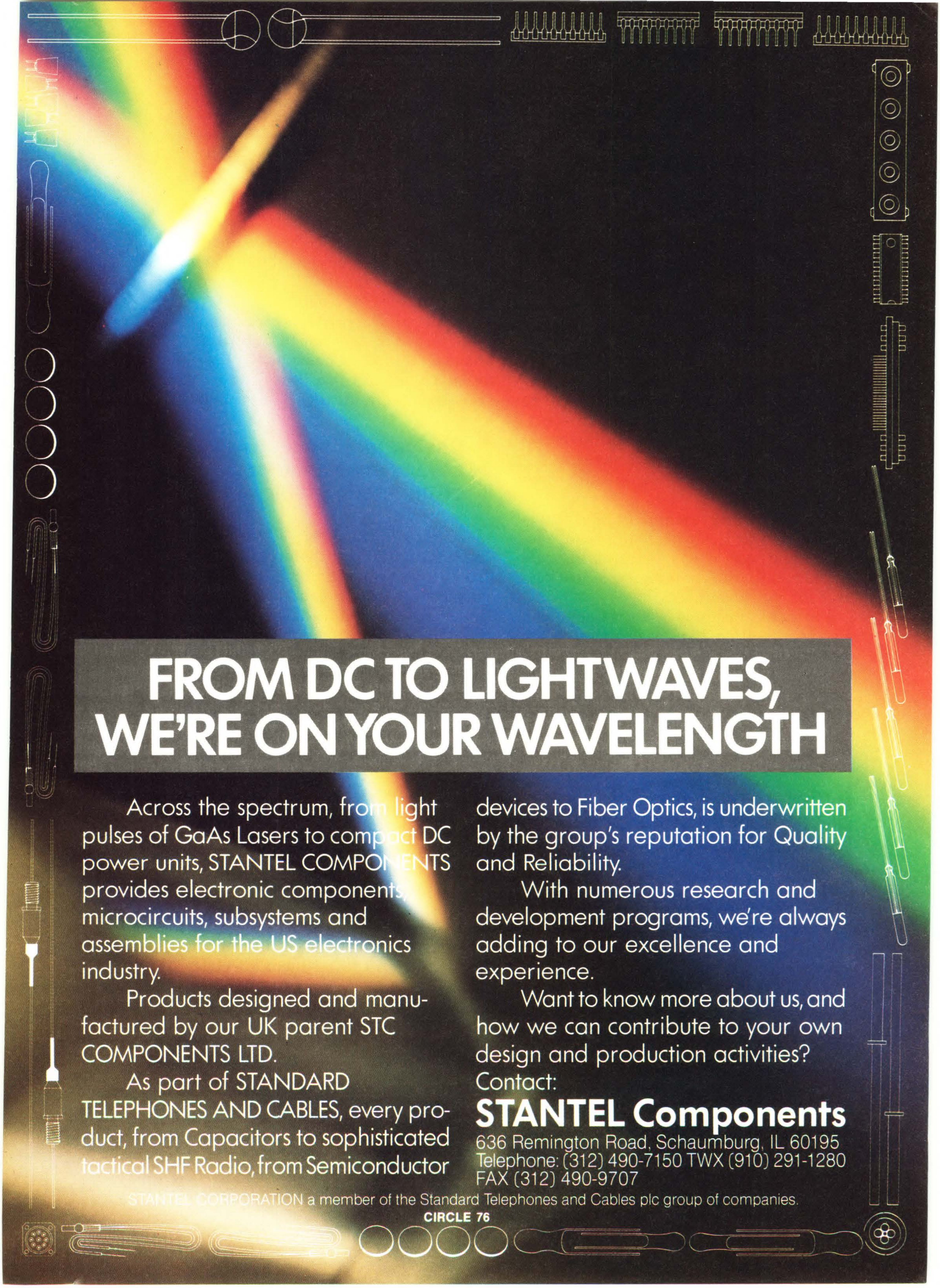
Generating test patterns is only half the battle, though. The patterns have to be evaluated as to their effectiveness at uncovering faults. That evaluation requires fault simulation, which can be done by manually inserting faults, applying the test vectors, and determining whether the fault is detected. Often, this approach is used at the system level.

At the device or board level, however, software fault simulation is very popular. As with ATPGs, however, the simulator can quickly exhaust the available computing resources. Depending on the approach, CPU time can rise according to the square or cube of the number of gates in the circuit. One way around this problem is to take a statistical approach in which only a certain percentage of all the possible faults are simulated.

Fault simulation can be done in four main ways: serially, with one fault inserted at a time; with a small number of faults in parallel; deductively, where only the good machine is simulated and fault effects are deduced from the good machine's state and the fault sources; and concurrently, where a large number of faults are simulated at the same time. Concurrent simulation, which is the fastest method, has become quite popular. Renewed interest in serial fault simulation is appearing, however, since the introduction of simulation engines. These are special-purpose hardware machines capable of simulating as many as 1 million events a second.

Elite simulation engines perform evaluations up to 1,000,000 events/s

In a recent evaluation by the Digital Equipment Corp. (Hudson, Mass.), a Zycad Corp. (Arden Hills, Minn.) LE 1002 simulation engine, which can do serial fault simulation, was compared with a software-based concurrent simulator, DECSIM. The study showed that the simulation engine's raw speed was not as important as the overall run time. Included within that run time is the setup time (the time it took to load the network description and apply the stimulus), which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was much greater than the actual simulation time. Nevertheless, on a network of 62,000 gates, the simulation engine proved to be 400 times faster.

Fault simulation is also getting a challenge from testability analysis programs that seek to rate the degree of controllability and observability early in the design cycle. Right now there are three schools of thought on the matter—testability analysis will replace fault simulation, fault simulation will never be replaced, or they both should be used together.

Actually what testability analysis is pointing towards, although it is really pie-in-the-sky right now, is a testability rule checker similar to the design rule checkers used for chip layout.

Fault simulation is under attack from another direction, too. Because they model faults as either stuck-at-zero or stuck-at-one conditions, fault simulators cannot represent some of the failure modes of CMOS circuitry. For instance, such circuits can have stuck-at-open failures, causing a gate output to retain its previous

Failures in CMOS circuits cause combinatorial logic to become sequential

value and the circuit to become sequential. Thus it would require two test vectors to detect a fault—one vector would sensitize the circuit to the fault, the other would cause it to show up. Some users, though, say that in actual practice, applying conventional fault simulators to CMOS circuits has not been as disastrous as one might think.

Lastly, the latest trend in fault simulation is to try and move it up in the design hierarchy. Recent efforts have been directed toward applying fault simulation at an architectural level, for instance. Using this approach, researchers at the AT&T Co. (Princeton, N.J.) achieved good correlation of fault coverage between an architectural model of a circuit and one realized at the gate level.

Add up all the problems with the test tools and it is easy not to be optimistic about testability. Consequently, various design techniques have been invented that take some of the strain off of the existing

Design techniques work around the limitations of the testing tools

tools. A major trend here is to use a structured design that transforms sequential circuits into combinatorial ones for test purposes. With the structured approach, the actual architecture of the design is dictated by the requirement for testability. Little is left to chance. If the rules are followed, an easily tested product will almost certainly result.

There are penalties to pay, however. Extra circuitry is needed, meaning that chips get bigger. As a result, yield and reliability may be degraded, and performance may suffer. Moreover, the rigid design rules may stifle a designer's creativity. Even so, some large vertical system houses have gone this route with a lot of success.

Depending on who is doing the looking, a given approach is either in the past, present, or future. One of the structured approaches, scan-path design, illustrates the ambiguous nature of testability quite well. For instance, in 1978 Nippon Electric Co., Ltd. (Tokyo) suggested a configuration in which modified memory elements constitute a special shift path to scan test vectors in, and test results out (Fig. 2). The memory consists of master-slave D-type flip-flops with auxiliary data and clock inputs, D_2 and C_2, respectively. D_1 and C_1 are the normal data and clock inputs.

During the scan-in operation, a test vector is applied to the primary inputs, and

another test vector at the scan input is serially shifted into the memory elements by clock 2. Then clock 1 is operated for one cycle. Next, clock 2 is used to serially shift out the test results appearing on the memory elements to the scan output. The big advantage of the technique is that a sequential circuit is reduced to a combinatorial one for test purposes.

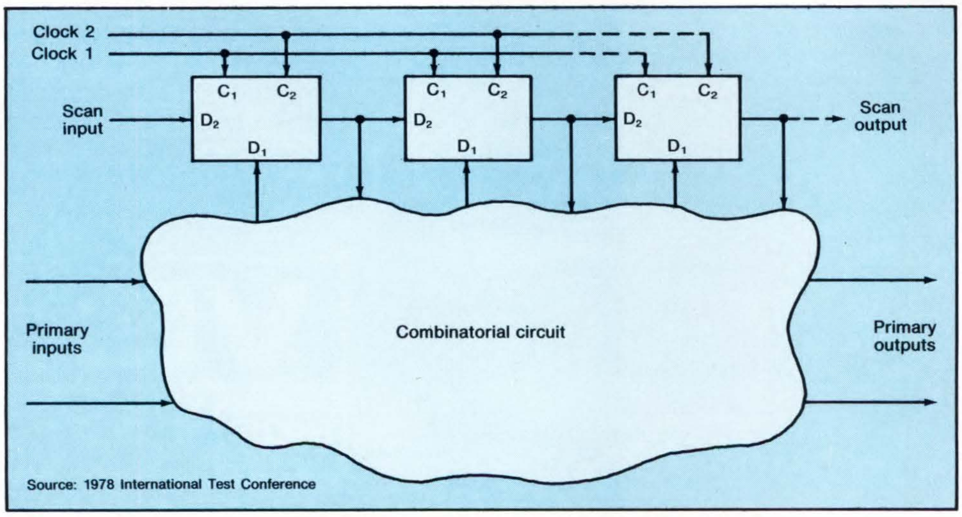
As far as the present is concerned, Honeywell Inc. (Phoenix, Ariz.) is obtaining very high fault coverage with what it calls native fault testing, its first venture into scan-path design. In this implementation, a single synchronous clock is used both for the circuit's function and to scan data in and out. A control input on the memory elements switches the circuit into the test mode.

The scan-path technique was chosen to meet the design requirement that the test program detect 99% of the stuck-at faults that might arise. Once again, because the circuit appeared as a combinatorial one for test purposes, an in-house automatic test program generator was able to generate the necessary test vectors.

Another reason the technique was chosen is that it is applicable at the chip, board, and system levels. For example, all the scan paths of the devices on a board can be serially linked to form a single path. Moreover, making the design testable increased the amount of required logic by a small amount only 5% to 7%.

Investigating scan-path design approaches for CMOS semicustom LSI chips

A look toward the future spurred a recent study to determine the applicability of scan-path techniques to CMOS semicustom LSI chips. In the study, Siemens AG (Munich, West Germany) focused on the impact of scan-path design on chip area and test generation. Their evaluation circuit contains the equivalent of 2400 gates in 534 standard cells, 157 of which are flip-flops. Moreover, the circuit has 19 input, 15 output, and32 bidirectional pins. With the circuit designed conventionally, an ATPG took 3500 seconds of CPU time to



2. In the scan-path technique implemented by NEC, the storage elements have auxiliary data (D_2) and clock inputs (C_2). During test, the element form a shift register for scanning test vectors in, and test results out using clock 2. Thus, a sequential circuit is transformed into a combinatorial one for test purposes.

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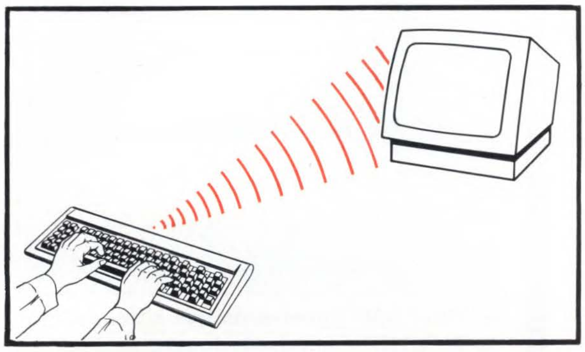

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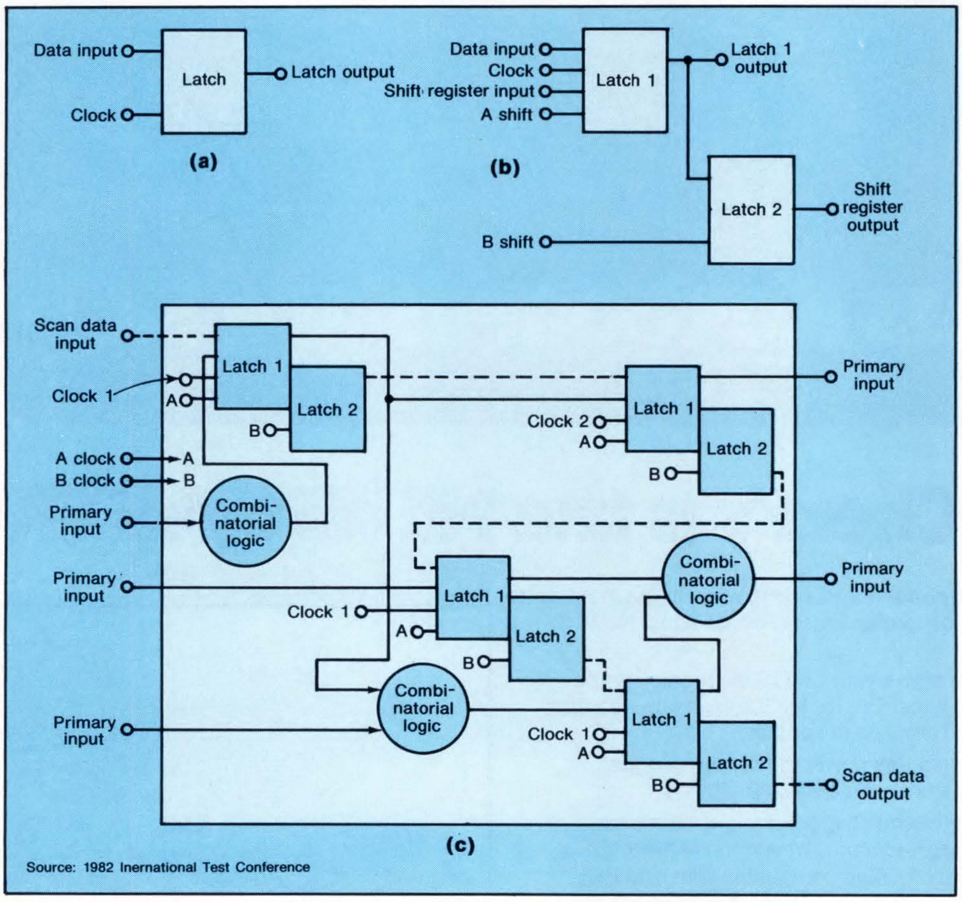
generate 8000 test vectors that detected only 38% of all stuck-at faults.

Next, a mixed strategy was tried. For openers, 7000 manually generated test vectors achieved 64% fault coverage. Added to those vectors were 13,000 randomly generated ones, which increased the fault coverage by 7%. Then, the ATPG created an additional 7800 test vectors, adding another 14% to the fault coverage. The grand total came to 30,000 seconds of CPU time for 27,800 test vectors that achieved 85% fault coverage.

When the circuit was implemented, using the scan-path technique, the chip area increased by about 14% as expected. The big news, however, came when the same ATPG was applied to the resulting pseudo-combinatorial circuit. Here, less than 400 seconds of CPU time generated 190 vectors and 95% fault coverage.

Of course, the test vectors have to be



3. The LSSD (level-sensitive scan design) technique developed by IBM uses a polarity latch to eliminate timing problems and race conditions. As long as the clock=0, the output cannot change state. After the input is stable, the clock is set to 1 and the output takes on the value of the input (a). Two latches are used to form a shift register latch (b). As implemented on a typical LSSD LSI chip, the shift register latches are clocked to form the scan path for test signals indicated by the dotted lines (c).

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Comparator/ Driver	10G012	3 GHz
Precision D Flip Flop	10G021	3 GHz
2 Stage Divider	10G060	3 GHz
7 Stage Counter	10G065	3 GHz

NAME	PART NUMBER	SPEED
Variable Modulus Divider	10G070	2 GHz
7 Stage Divider	11G566	4 GHz
Diode Array	16G010	500 GHz
Diode Array	16G011	675 GHz
FET Array	16G020	15 GHz
Dual Gate FET Array	16G021	15 GHz

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shifted in and out of the 157-element scan register. This means that about 30,000 vectors are needed by the automatic test equipment, roughly similar to that required by the conventional design. The study concludes that deciding to use the scan-path approach is not a technical question, but an economic one weighing the disadvantages of increased chip area against the improved testability for limited-production semicustom devices.

A different form of structured design called LSSD (level-sensitive scan design) was developed by IBM Corp.'s System Communications Division (Hopewell Junction, N.Y.) and its System Products Division (Boulder, Colo.). One of the driving forces behind this approach was to design sequential logic structures so that correct operation does not depend on signal rise and fall times or on circuit and wire delays. In other words, circuit operation becomes level-sensitive as opposed to edge-sensitive. The other concern was to design the storage elements so they could be operated as shift registers for test purposes, much like the scan-path approach.

The level-sensitive part of the design is accomplished with a polarity hold latch

A polarity hold latch forms the foundation for level-sensitive designs

(Fig. 3a). As long as the clock is at logic 0, the output of the latch cannot change. After the input stabilizes, the clock is set to logic 1, causing the output to take on the value of the input. The scan part of the design is realized by using two of the latches in a master-slave relationship to form a shift register latch (Fig. 3b).

To operate the latch as a shift register, data from the preceeding stage is gated into latch 1 via the shift register input when the A shift signal goes to logic 1. After the A signal returns to logic 0, the B shift signal gates the latch 1 data into latch 2.

In a typical LSSD LSI chip, the shift register latches form a scan path for testing (Fig. 3c). Appropriate clocking shifts test vectors or test results along the path indicated by the dotted line. As with scan-path testing, the LSSD technique allows sequential circuits to be tested as though they were combinatorial.

Since its inception, LSSD has undergone several refinements. One refinement adds a third latch that allows LSSD circuits to be interfaced to non-LSSD circuits. Another improvement helps overcome one of LSSD's drawbacks—it can require 20% or more extra silicon to implement it. In many parts of the circuit the L2 slave latch is used only for testing and becomes overhead when the circuit is functioning. To reduce the overhead, a second data port is added to the slave latch. This data port is clocked by a system clock, permitting it to be used to store system data when the circuit is functional.

As powerful as a technique like LSSD is, when it is combined with circuit partitioning for test purposes, a dramatic reduction in the CPU time required to generate test vectors occurs. In a study by the IBM's System Products Division, the CPU time required by an IBM 370 computer for logic structure description entry and test vector generation was studied for three situations—an unconstrained sequential network design, an unpartitioned LSSD implementation, and an LSSD implementation partitioned into sub-networks. Both the unconstrained design and the unpartitioned LSSD design reached a network size where CPU time, hence costs, rose sharply (Fig. 4). By constrast, CPU time for the partitioned design rose linearly with network size.

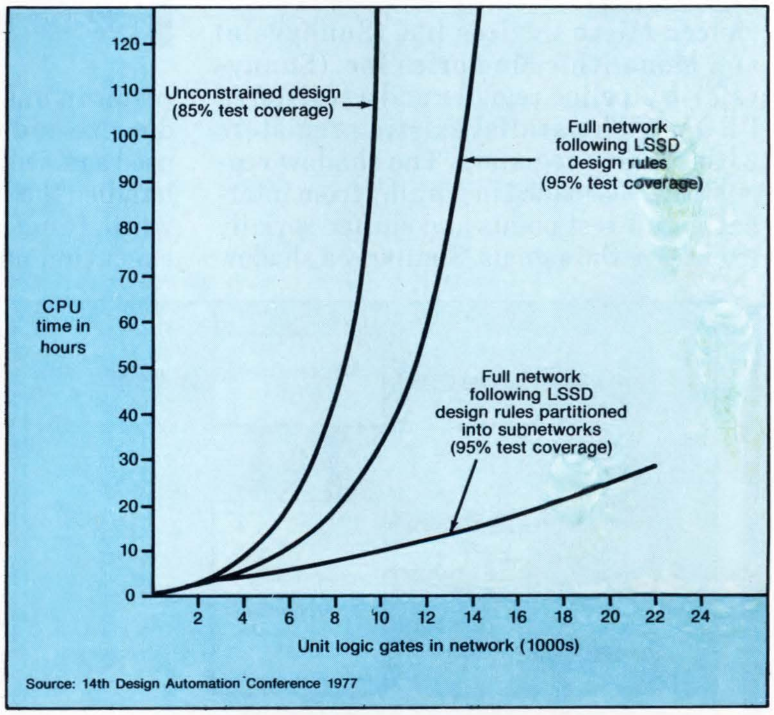
One benefit of all the scan techniques is that they greatly aid in fault isolation. By applying signature analysis to the serial stream of test data that is scanned out, it is possible to trace a fault back to the device level during board or system test.

While the foregoing approaches have all been variations on the serial scan theme, a random scan method has also been proposed for testing sequential circuits. Developed by Fujitsu Ltd. (Tokyo, Japan), the technique uses addressable latches as storage elements (Fig. 5). The array of latches also serve as test input and test output holding latches.

As each latch in the array is sequentially addressed, data applied to the scan data input is strobed into the addressed latch by the scan clock. Then, the system is clocked once and the latches are serially addressed and clocked again. As each latch is clocked, its output is fed to an AND tree where it appears at the scan data output.

An advantage of this technique is that each latch can be independently selected. Moreover, a latch can be accessed without disturbing the internal state of the circuit. Because the latch array is essentially structured like RAM, on-board memory can also be tested by steering the test signals to it using multiplexers.

There is a pretty heavy penalty to pay for random scanning, however. Two address gates are needed for each storage element, along with the address decoders



4. Partitioning a complex circuit for test purposes, even when it has been designed for testability, greatly reduces the CPU time needed to generate test programs. In this study concluded by IBM, CPU time rises linearly with gate count when an LSSD design is also partitioned. By contrast, both the unconstrained and full network LSSD designs rapidly reach points where CPU time becomes pronibitive.

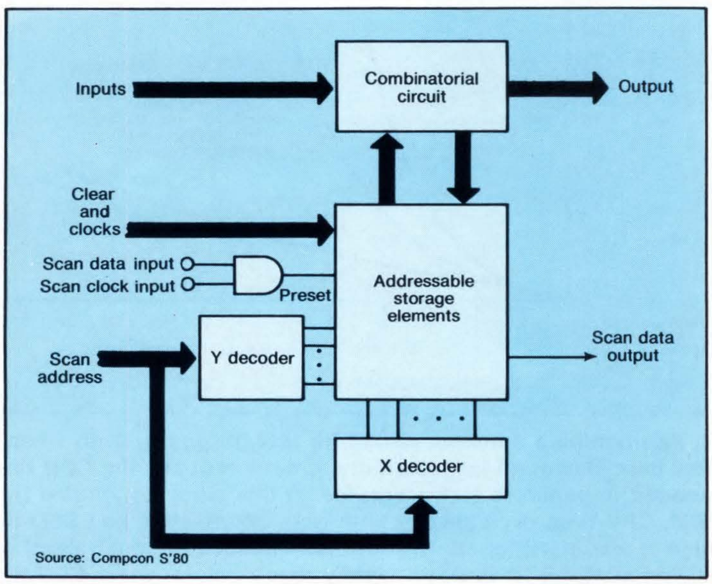
and output AND tree. This results in an overhead of three to four gates for each storage element. What's more, 10 to 20 pins are required for the scan control, data, and address pins. The pin count could be reduced to six, but then the latch elements would have to be selected by a serially loadable address counter.

Despite the benefits of scan designs, their use is not widespread. One reason is that the special memory elements needed are not available. At least two chips, however, are designed around a Serial Shadow Register (SSR) technique which is a form of scan design (ELECTRONIC DESIGN, April 14, 1983, p. 119). Jointly developed by Advanced Micro Devices Inc. (Sunnyvale) and Monolithic Memories Inc. (Sunnyvale), a pipeline register and a registered PROM each parallel existing registers with shadow registers. The shadow registers can be loaded in parallel from internal circuit test points and shifted serially to observe the signals. Similarly a shadow register may be initialized to any state for control purposes by serially shifting that state into the register.

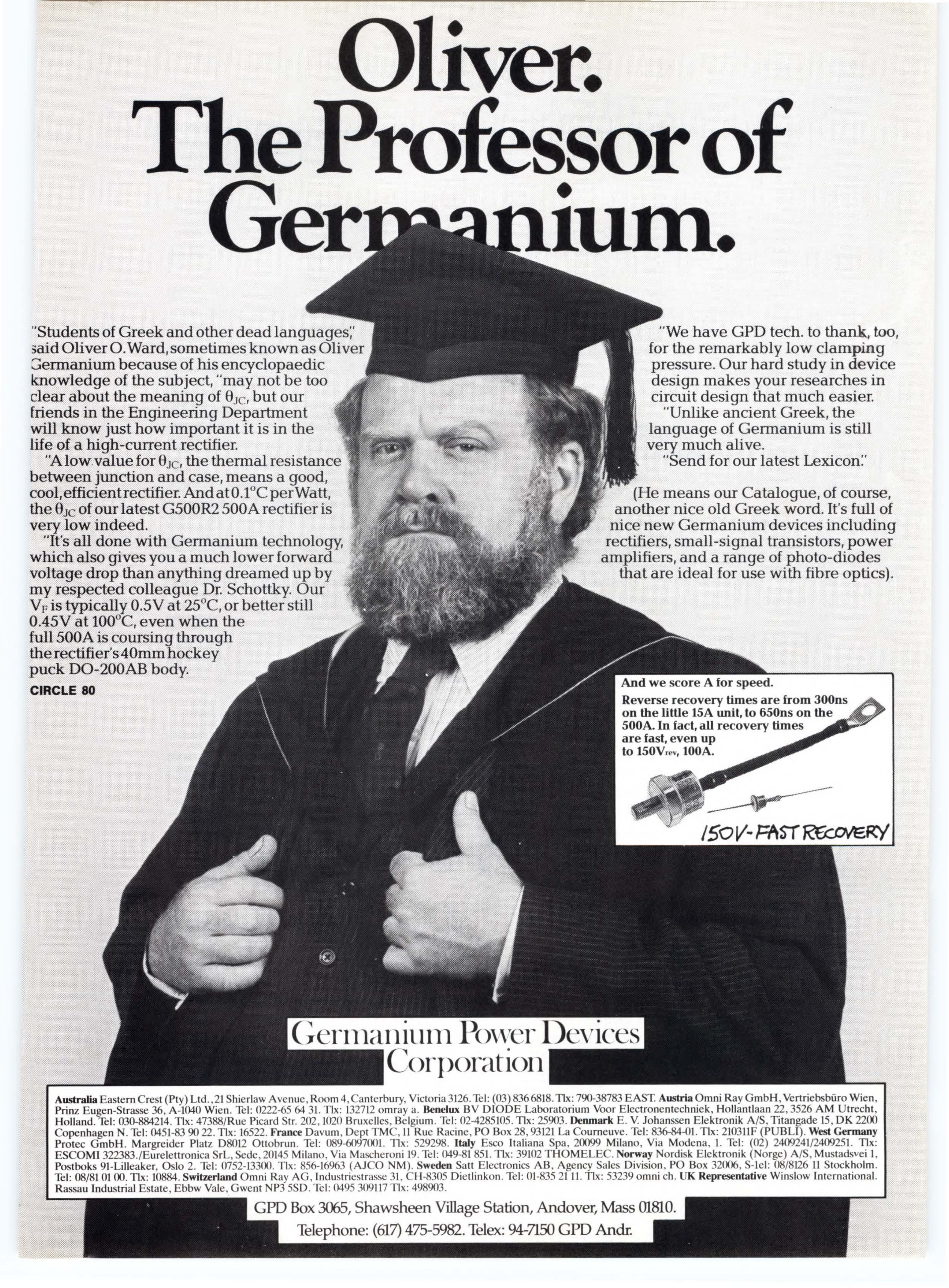
An interesting comparison is to look at scan design from the point of view of commercial VLSI chip designers. A case in point is the MC68020 32-bit microprocessor. The engineers at Motorola Inc. (Austin, Texas) knew it would be impossible to functionally test such a complex chip. At the same time,they realized that using a fully structured testing approach would

Putting testability into the design of a commercial 32-bit microprocessor

result in unacceptable increases in both die size and test time. As a result, they used a mixed approach. Structured testing handles the difficult to test control logic, while functional tests check the chip's execution unit which has good control-



5. A random scan method developed by Fujitsu places all storage elements of a sequential circuit into an addressable array. As each element is serially addressed, test data is scanned in. An important advantage of this technique is that when data is scanned out, the internal states of the circuit are not changed.



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lability and observability.

Partitioning played a big role in simplifying testing. Thanks to the bus orientation of the chip, PLAs, ROMs and the cache memory were separated from the rest of the circuitry using microcode and multiplexers. Because some of the PLAs could not be separated using the existing buses, additional partitioning was accomplished with a signature register. An on-

Testing is simplified when the design is partitioned into sections

chip register, which represents the only built-in self test used, tests those PLAs. Overall, the design team feels its test logic realized the same goals as scan design without imposing the penalty of increased die size.

Because techniques such as LSSD are not for everyone, one forward looking approach seeks to solve test problems by interfacing the controllability and observability points of a circuit to a proposed standard testability bus. Dubbed the Turino (Totally universal reset, initialization and nodal observation) circuit, the concept developed by Logical Solutions Inc. (Campbell, Calif.) can be implemented as a standard cell in a VLSI device, a gate array, or with conventional MSI components (Fig. 6).

Basically, the circuit can be divided into two major areas—the control point section, and the visibility section. When connected as shown, the circuit can be produced as a single device. Alternatively, the sections can be implemented as separate devices, combining the appropriate signals at the board or system level.

Except for the control point outputs and visibility point inputs, the connections to the circuit make up the testability bus. A minimum standard bus would require about 20 pins. Because the control point and visibility point sections are equipped with serial data inputs and outputs, expansion is easily accomplished by connecting the serial output of one circuit to the serial input of another.

Using a logic simulator, 32 visibility and control points were added to a board containing 150 ICs, several of which were LSI/VLSI devices. Compared to the standard board, test programming time was reduced 20% minimum, 50% typical; the number of test patterns was reduced by 15% minimum, 50% typical; test and troubleshooting times by 10% minimum, 25% typical; fault coverage increased by 5% minimum, 10% typical. Moreover, where LSSD type approaches typically impose a 2% to 20% overhead in additional circuitry, the proposed circuit typically imposes less than 1% overhead. The circuit has a patent pending and is available for licensing on a non-exclusive basis.

Another way around the VLSI testing problem involves taking some of the functions normally performed by a tester and building them right on the chip. Such built-in test approaches will see some pretty heavy activity in the years to come. The nice thing about built-in test is that it doesn't necessarily require the kind of total design commitment the scan tech-

Coupling built-in test with scan-design yields chips that check themselves

niques do.

One approach known as Bilbo (built-in logic block observation) couples built-in test with the shift register concept of LSSD. When placed in the test mode, each Bilbo subsystem can be operated as a shift register, pseudorandom pattern generator, or parallel signature analyzer. With one subsystem supplying test patterns, and another generating signatures, a combinatorial network between them can be tested (Fig. 7a). By reversing the roles of the two Bilbo subsystems, a second com-

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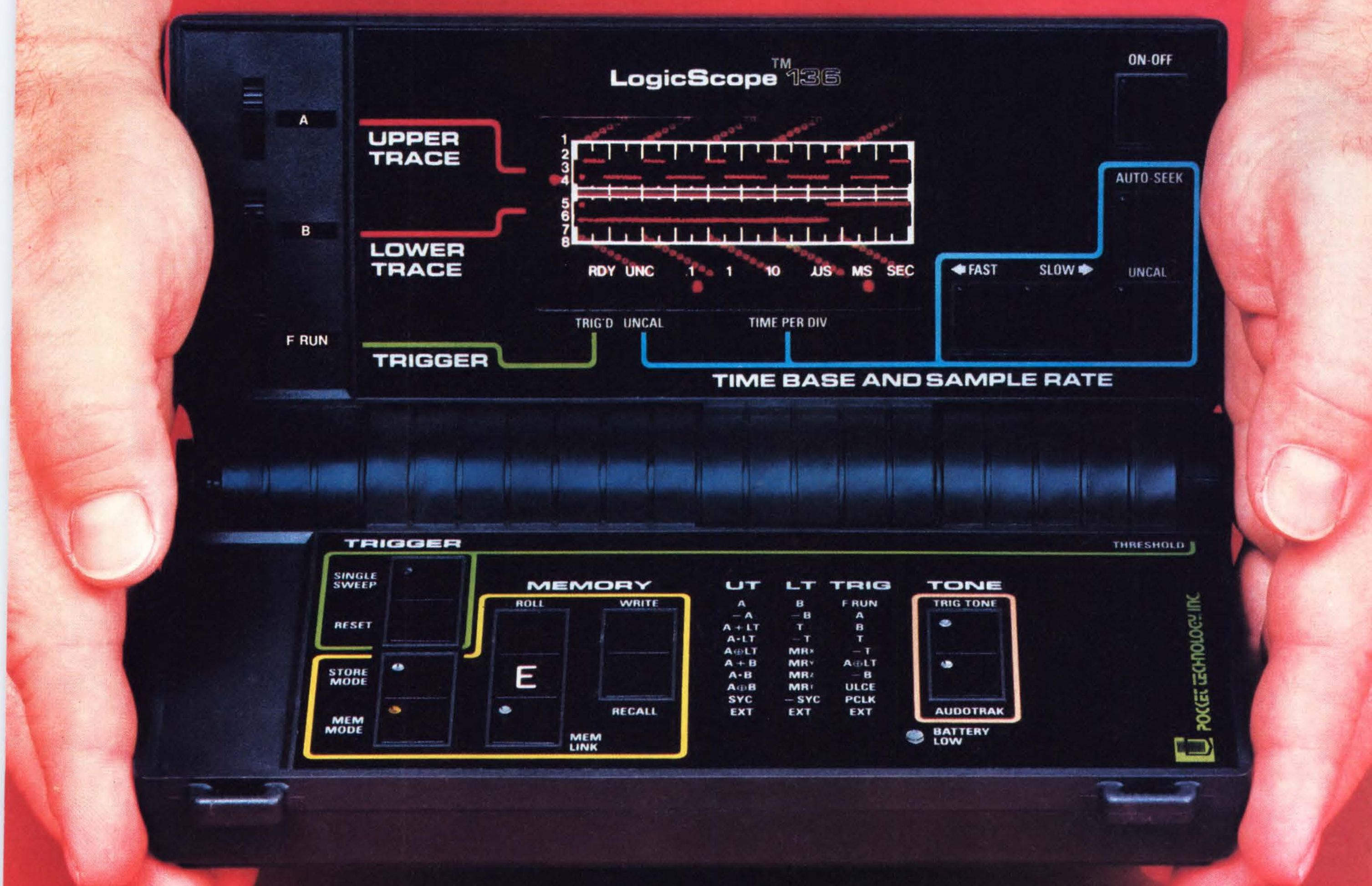

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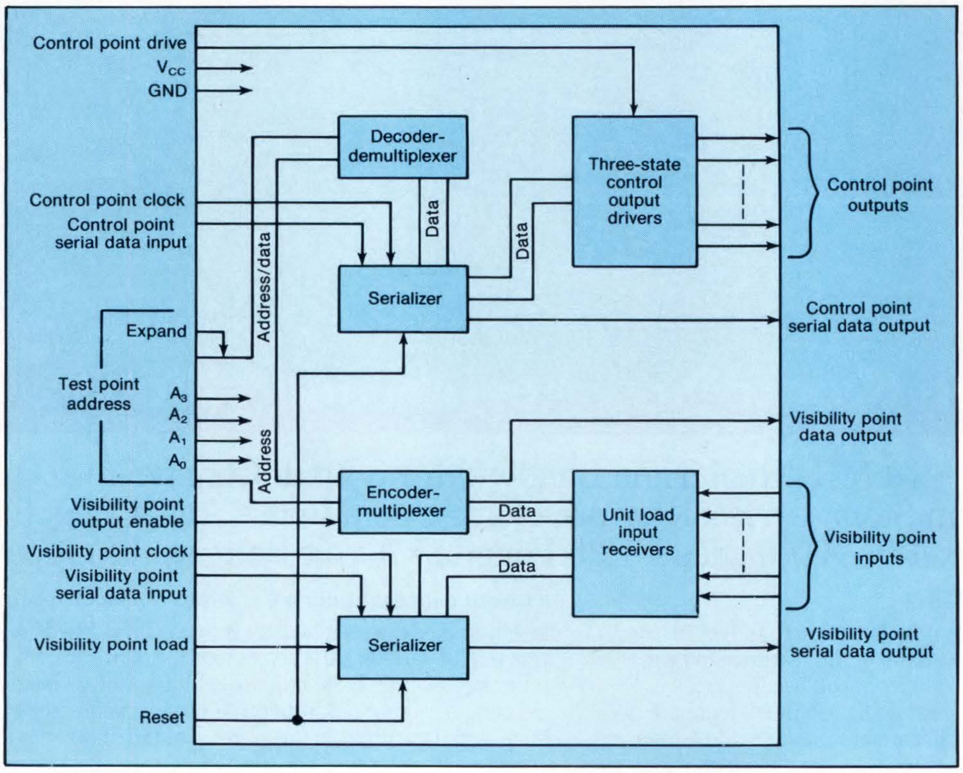
binatorial network may also be tested (Fig. 7b).

Built-in testing is almost becoming a necessity as more and more VLSI devices incorporate embedded RAMs. These are memory arrays whose address, data, and control lines are not accessable from the chip's I/O pins. One proposal for the testing of embedded RAMs uses a combination of self-test and scan techniques. By modifying the address, input data, output data, and read/write control registers, researchers at Stanford University (Stanford, Calif.) ended up with a memory that could operate either normally, or in any of three test modes: scan, single-step, and self-test.

When the scan mode is selected, all registers and flip-flops form a scan path to shift test signals in, and test results out. By shifting in the appropriate patterns, bridging faults between any two data lines and can be detected, along with faults in all the registers and their associated combinatorial circuits. Moreover, this mode also detects any single stuck-at faults in the embedded memory.

Using the single-step mode, self-testing



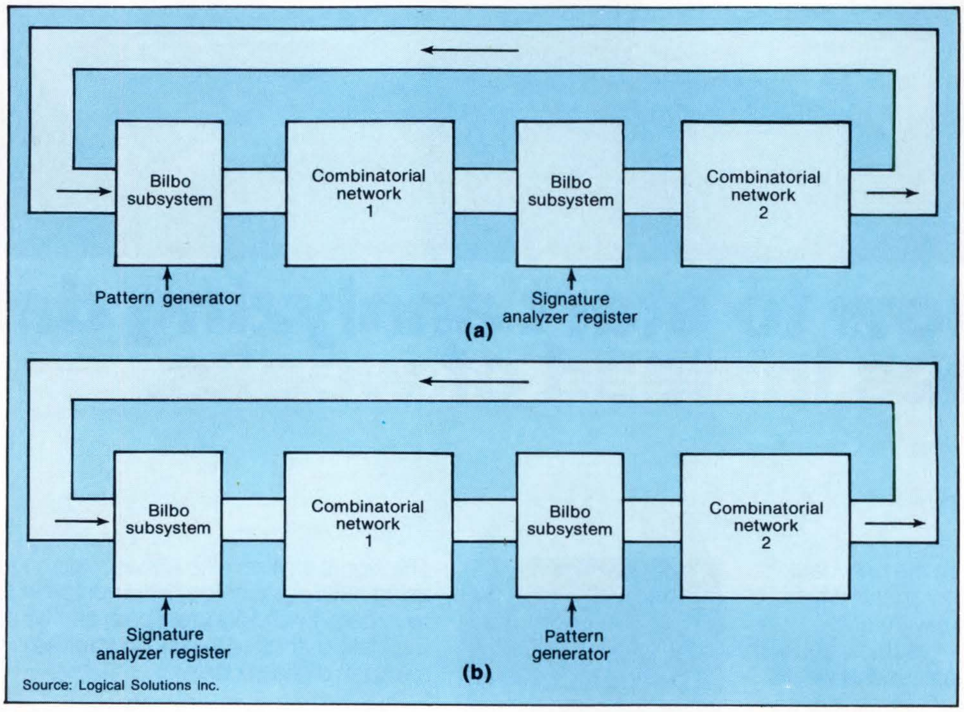
6. The Turino (Totally Universal Reset, Initialization and Nodal Observation) circuit has been proposed by Logical Solutions to interface the control and visibility points of a circuit to a standard testability bus. All connections to the circuit other than the control point outputs and visibility point inputs, are for the testability bus.

can be interrupted to look at any intermediate result. This is accomplished by scanning the data out.The self-testing itself is accomplished by applying a simple march test pattern to the memory. In this mode, the address, input data, and read/write registers operate as a march test pattern generator.

Despite elegant methods, engineers continue to design ad hoc

As elegant as the many design-for-testability schemes are, many engineers will still be designing circuit boards using ad hoc design techniques for a long time to come. The underlying philosophy behind these techniques essentially consists of watching out for potential testability pitfalls as the design evolves. In essence, the ad hoc approach is really one of applying common sense and forethought to the design. Engineers have been designing circuit boards this way for a long time, but with all the heightened awareness of testability around, they are going to be doing a better job at it.

Simply put, the designer must take



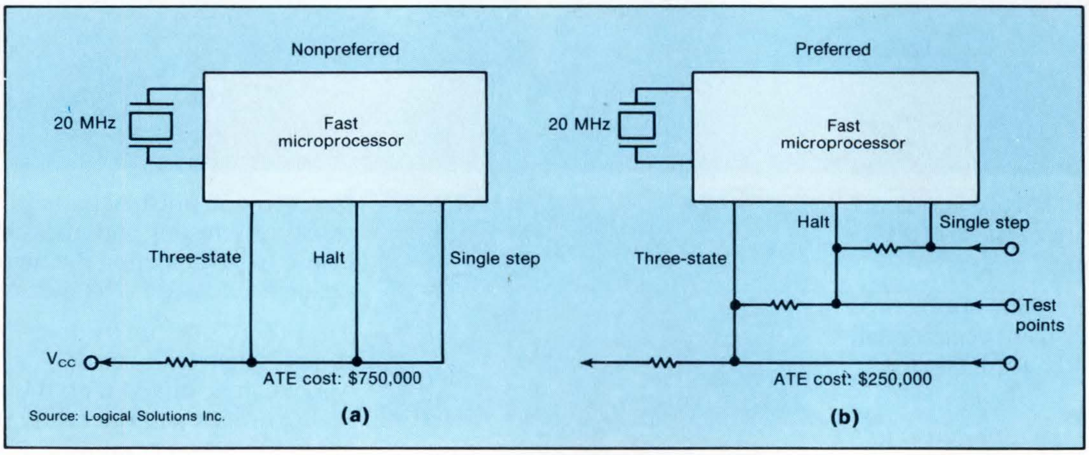
7. Using Bilbo (built-in logic block observation) subsystems, tester functions can be incorporated as part of a chip. In this example, one subsystem supplies pseudo-random test signals to network 1, while the other subsystem acts as a multiple input signature analyzer to gather test results (a). By reversing the functions of the subsystems with control signals, network 2 can be tested also (b).

whatever steps are needed to ensure that controllability and observability, the two keys that unlock the testability door, are not lost. In general, he or she uses methods such as partitioning the circuit to make it easier to test, adding provisions for breaking feedback loops, and providing a means for initializing critical parts of the circuit. Even the way the designer makes electrical connections can dramatically impair testability. For instance, something as simple as tying a microprocessor's control lines to V_{CC} or ground imposes stringent requirements on the tester itself. For instance, in one circuit (Fig. 8a), the high clock rate coupled with the inability of the tester to control the microprocessor's single-step, halt, and three-state lines mean that the circuit must be tested using expensive high-speed automatic test equipment.

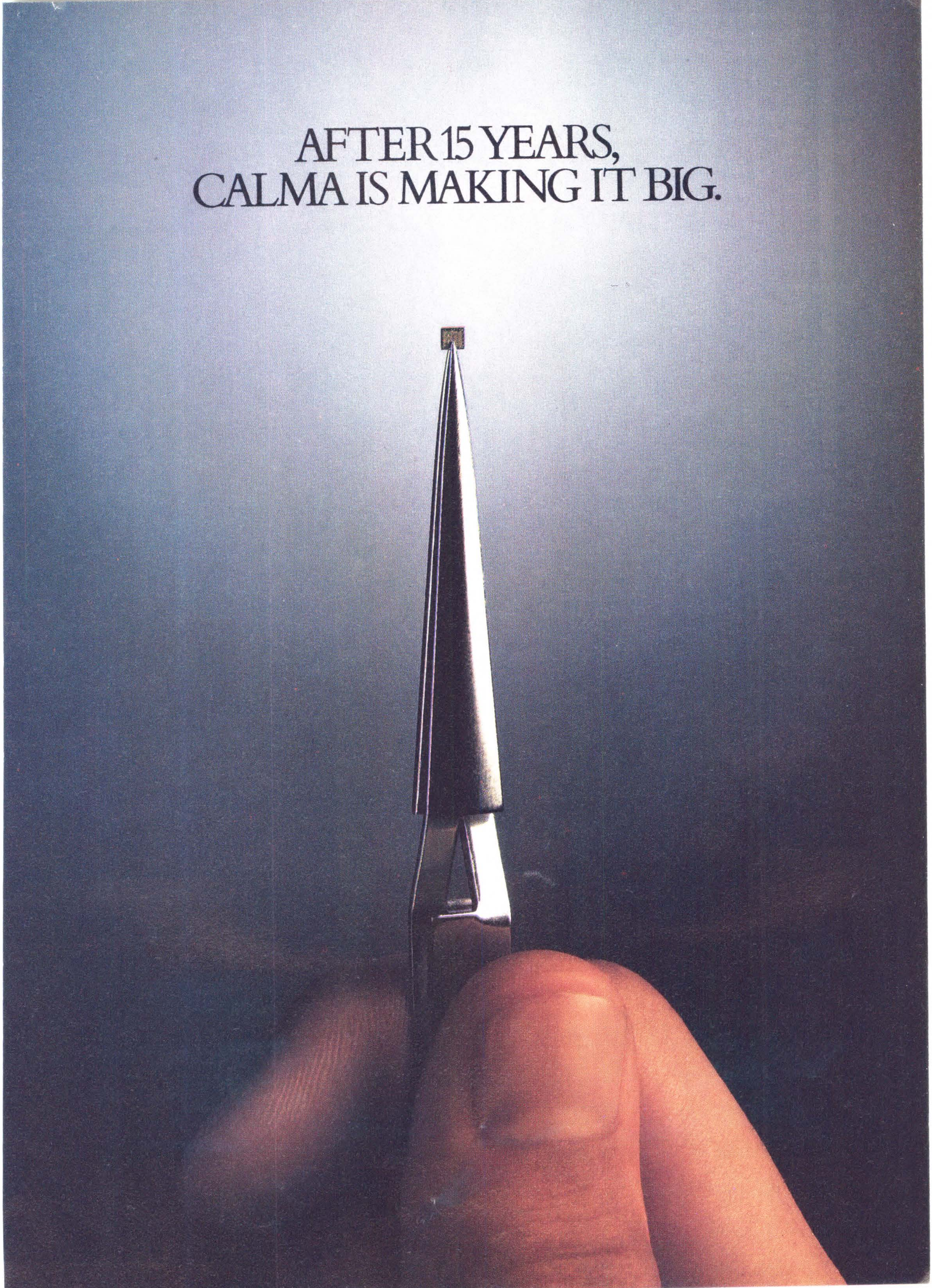
Common sense helps make printed circuit boards that are easy to test

By adding a couple of resistors and bringing out three test points forms another circuit (Fig. 8b). Now, because the microprocessor can be easily controlled, a less expensive static functional tester can be used.

Problems such as the foregoing ones happen frequently. Sometimes they are the result of something as simple as using a circuit recommended on a data sheet. It is a pretty sure bet that the majority of these circuits do not incorporate any testability considerations. The bottom line is that exotic techniques aside, there is a lot of room to achieve testability early in the design cycle. A little time spent here can save a lot of time later. In fact, the test engineer may even grow to like the designer. □



8. Something as simple as tying a microprocessor's control lines to V_{CC} or ground can cause testability problems. A high-speed functional tester must be used when the microprocessor cannot be controlled (a). Bringing out test points for control purposes allows a lower-cost static functional tester to be used (b).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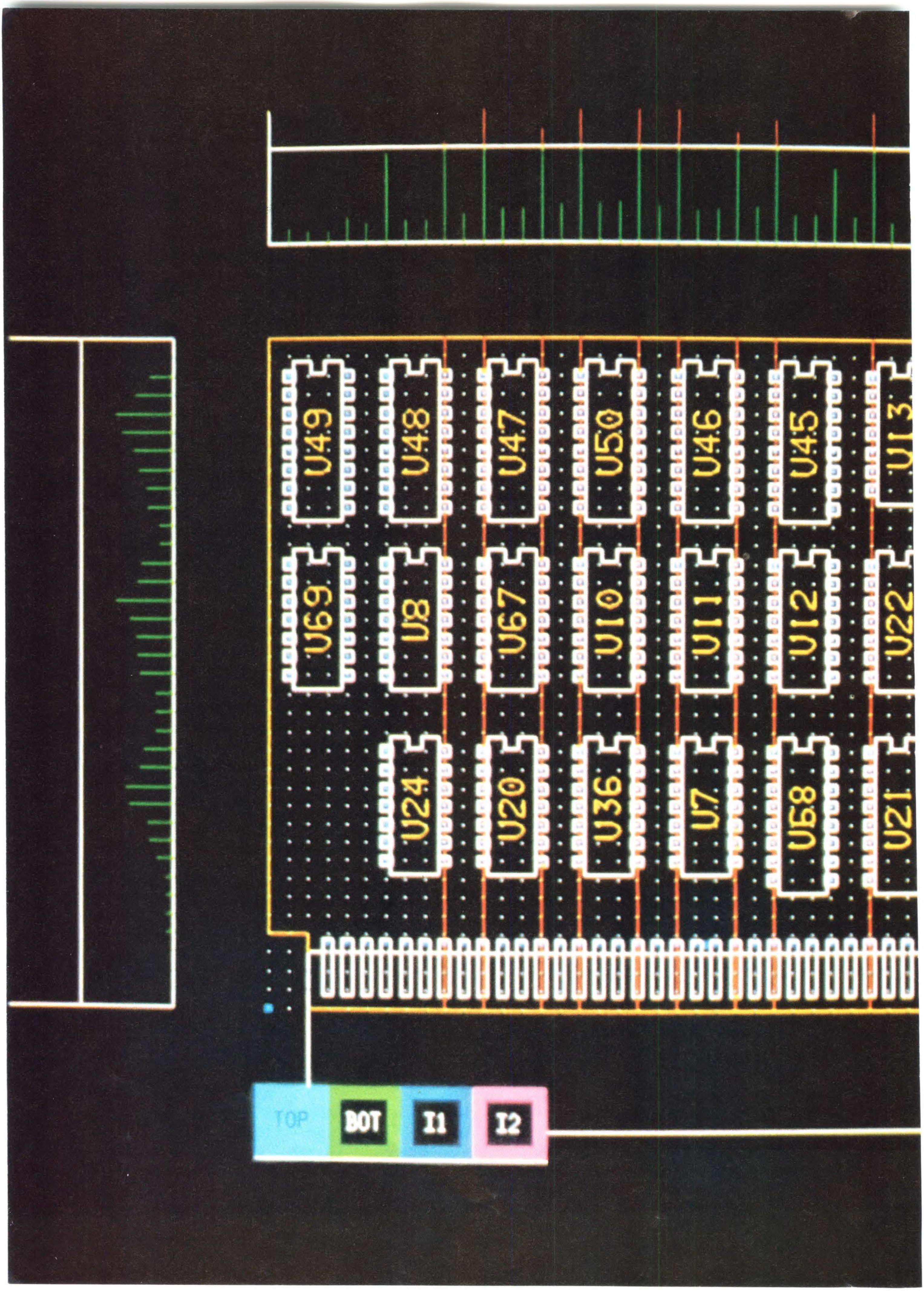
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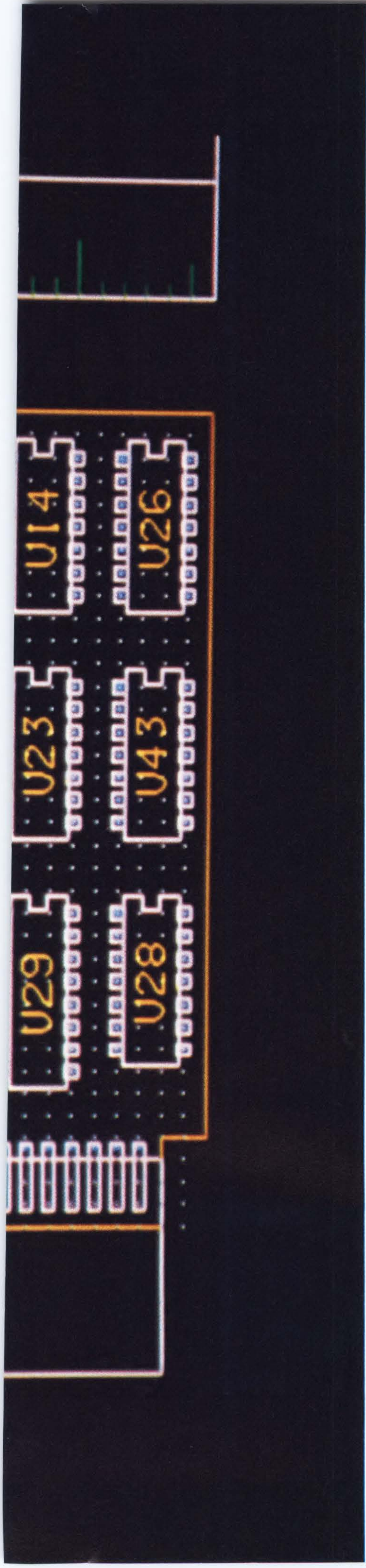

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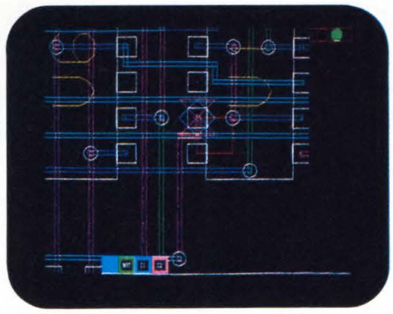

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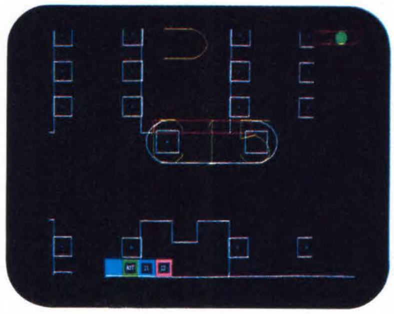

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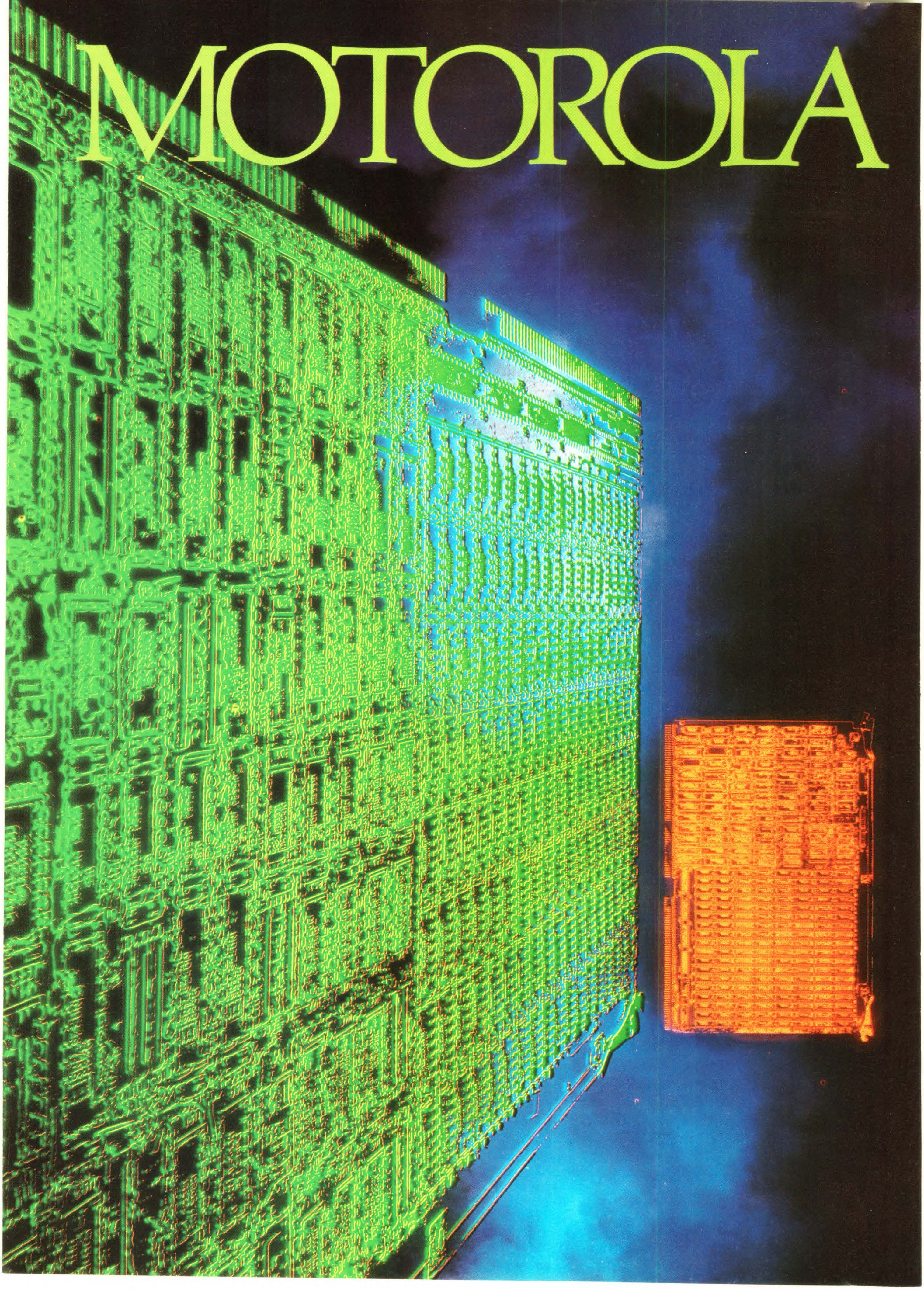
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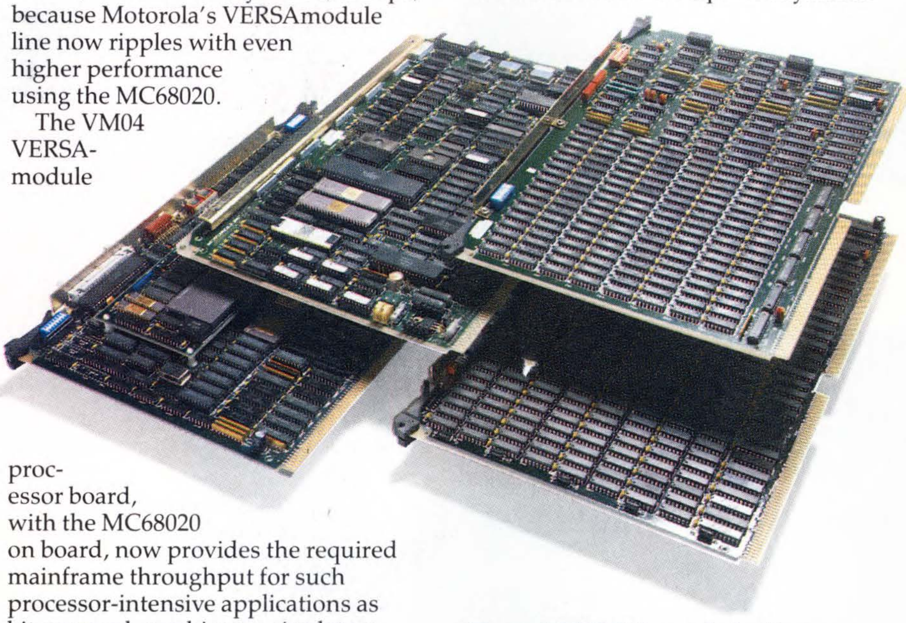

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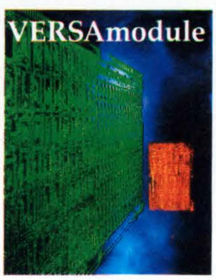

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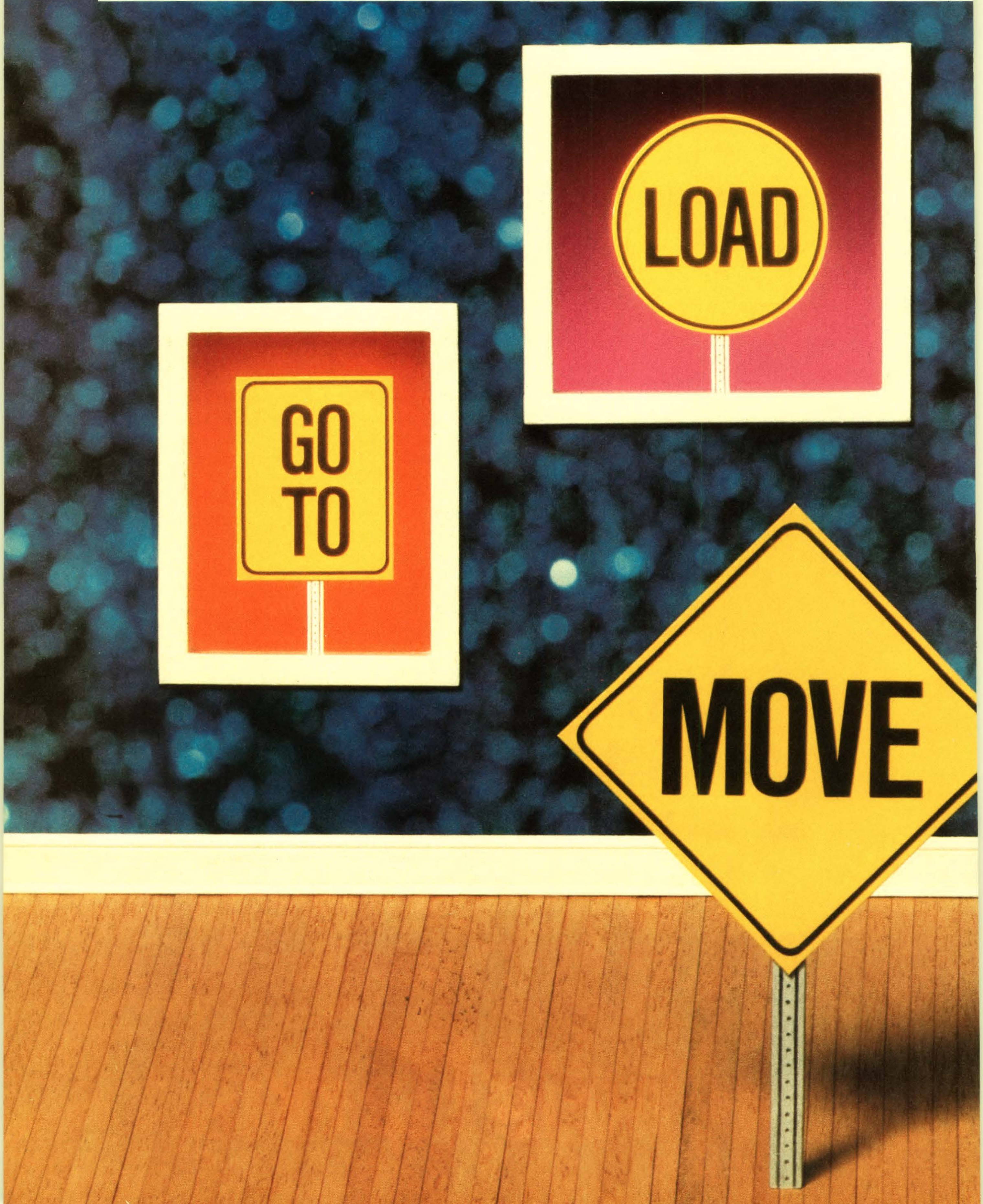


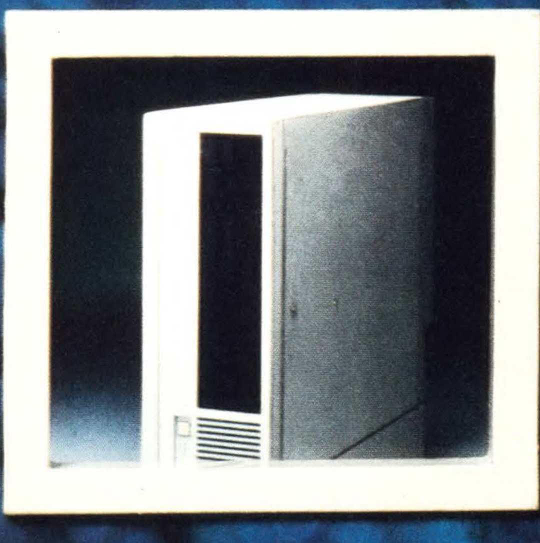
RISC MACHINES

Sometimes it seems as if the entire computer industry is bent on building more complex machines and writing more involved software. Or almost all of it: A small band of renegades is flying in the face of this tendency, championing the reduced-instruction-set computer (RISC). For them, simplicity rather than intricacy is the key not only to faster machines but to cheaper and smaller ones as well.

Adherents of the RISC approach should not be taken lightly. By the end of the decade, virtually all machines for engineering — from the smallest desktop workstations to the largest superminicomputers — will embody some aspect of the RISC concept. In fact, RISC principles will be showing up to some degree in every computer built late in the 1980s.

The current commercial implementations of RISC architectures clearly mark the two

STEPHAN OHR



primary paths that the reduced-instruction-set approach will take. Typifying one tack will be large general-purpose machines—using low-cost TTL logic—that will deliver far more power than the current generation of minicomputers. The other route leads to engineering, graphics, and other special-purpose workstations that employ proprietary VLSI chips relying on RISC technology. These machines will squeeze more power into a desktop microcomputer than is now found in the VAX-11/780.

Indeed, the lure of RISC architectures is so inviting that two computer giants—IBM Corp. (Yorktown Heights, N.Y.) and Digital Equipment Corp. (Maynard, Mass.)—have multifaceted RISC projects under way. Another, Hewlett-Packard Co. (Palo Alto, Calif.) has announced categorically that RISC architectures will be employed in all of its next generation of machines. And significant newcomers, like AT&T Bell Laboratories (Murray Hill, N.J.) are turning to RISC designers for ongoing research (see "Bucking Trends Means Taking Risks," opposite).

RISC architectures are alluring but are not suitable for all tasks

But despite this rosy outlook it would be an oversimplification to view the reduced-instruction-set machine as an across-the-board approach to every chore. For certain jobs—office computing, on-line transactions, data-base file-servers, and other I/O intensive areas—there is little evidence to suggest that the RISC method is inherently superior to other architectures.

RISC computers generally run faster not only because they execute a smaller set of instructions, but also because the instructions they do carry out are typically optimized to be completed within one machine cycle. (More conventional computers generally require a number of cycles.) Since they normally operate from register to register within a CPU (accessing main memory only with simple Load and Store instructions), reduced-instruction set machines handle simple operations faster than anything else around. Also, complex tasks can be reformulated as a series of simple instructions, and machines running a stream of these simplified instructions work measurably faster than powerful minicomputers executing more complex general instruction sets.

Further, the RISC's CPU is relieved of much of the usual arsenal of logic gates required to decode and execute complex instructions, meaning that the processors themselves can be smaller and cheaper than those available in the past. And that includes even microprocessor-based CPUs.

For instance, IBM's 801 project was based on the premise that it is possible to construct a CPU whose instructions are simplified to the point that they could be executed within one cycle. A second goal was to minimize the time the CPU is idle during memory accesses by fetching instructions and data from an on-board cache. What's more, instruction execution was overlapped with data-loading operations. A third target was to create a compiler that would allow the machine to run a subset of VM (IBM's interactive operating system).

This last objective allowed the performance of a MECL-based 801 CPU to be compared with that of a System/370-168 mainframe. IBM researchers found that the 801 took an average of 1.1 machine cycles to execute each instruction, compared to the typical 1.7 cycles needed by the 370. Observers speculate that the 801 CPU can cut through between 1.5 and 2 million instructions/s. They go on to say that if it is embodied in a commercial product (late this year or early next year) it will probably find a home in IBM's first high-

Bucking trends means taking risks

The RISC philosophy runs counter to the trend that looks to boost performance by increasing hardware and software complexity.

The proliferation of complex instruction sets has not grown out of an impulse to promote complexity for its own sake. Rather, it is a way of accommodating high-level languages. Instruction sets represent software shorthand for the lines of microcode required to program a central processing unit.

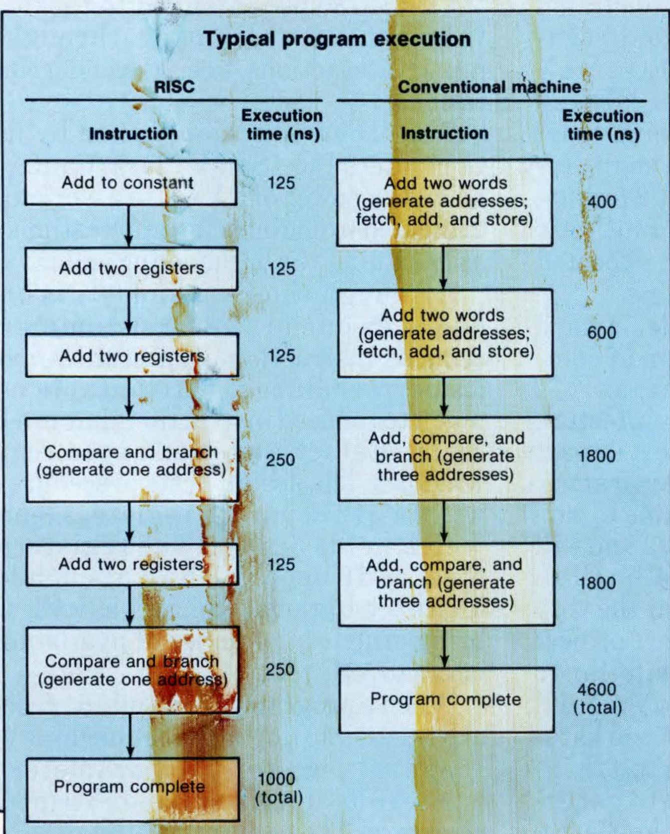
However, research carried out in the mid-1970s at Berkeley, Stanford, and IBM tracked the actual instruction flow through a variety of machines and found that the most frequently executed instructions consisted of only four or five out of the hundreds available. And these several instructions could be reduced to microcode. Alternatively, they could be built into hardwired CPUs. Instead of using microcode to reprogram gates and registers within the CPU, it is also possible to permanently configure those gates to execute a limited number of instructions. Though the hardwired CPU appears to be less versatile than its microcode-driven counterpart, it spends no time reconfiguring its gates and registers and runs significantly faster.

Additionally, researchers discovered that it is possible to rephrase some of the more complex instructions as a series of simpler ones. Also, these simplified subroutines could be driven directly by most high-level language instructions. (C is a noteworthy exception in that it needs to be compiled before execution.) High-level calls to simplified op codes, in fact, seem to execute faster than many high-level calls to the more complex set.

A third finding centered on memory hierarchies in CPU design. In short, a register stack runs faster than a cache, which, in turn, runs more quickly than main memory—although the gain in speed is traded off against expense and design complexity.

The basic argument advanced by RISC advocates is this: Simple instructions can be executed in fewer machine cycles (and with less hardware) than complex instructions, thus application programs that cascade blocks of simple instructions will run faster than equivalent programs consisting of more complex instructions. This contrasts sharply with the approach taken with conventional computers, which sometimes need hundreds of microcoded control words that, in turn, require four, five, or six machine cycles to run.

The whole purpose of RISC is to streamline the instruction-fetch, instruction-execute process of conventional computers, while retaining the programmer's links to high-level language calls. It is important to note that this tack differs from that taken in a machine built around a CPU with a significantly smaller number of machine instructions. By itself, a reduced instruction set buys very little. Rather, RISC architectures generally refer not just to the number of executable instructions, but also to reformulating the address-generation process required to fetch instructions and operands from memory and to restructuring complex instructions into simpler ones.



performance CAE workstation.

At the same time, IBM has funded an extensive research and product development project at Carnegie-Mellon University (Pittsburgh, Pa.). Although no one will say for sure, the project could yield a personal computer or a desktop micro with several times the power of the IBM-PC/AT.

Big-league players about to unveil developments in RISC-machine work

As much (or as little) is known about what IBM's largest competitor has up its sleeve as far as a RISC architecture is concerned. Digital Equipment is thought to have two RISC projects under way: One, known as the Nautilus, probably is an ECL machine that can burn through 10 million instructions/s. The machine could conceivably be a bridge between DEC's VAX family and the DEC 10 and the DEC 20 series of workstations. The second, code-named Titan, is believed to be an engineering workstation that comes in at 2 million instructions/s. It should run some VAX application software, but is not expected to be compatible with the VAX line.

Hewlett-Packard, meanwhile, is hard work on its own next generation of computers. The Spectrum project, as it is known, goes with a RISC-like architecture and probably will have the greatest impact on the company's 3000 line of mainframes. The Spectrum is believed to be able to carry out 5 or 6 million instructions/s and will most likely be fitted out with a 64-bit CPU. It will eventually take its place at the very top of HP's computer line. Another project attributed to HP is a chip set similar to Digital Equipment's MicroVAX II. Though the set is intended for workstations, the fact that it responds to 128 instructions makes it closer kin to generalized microprocessors (like the 68020) than to VLSI RISC devices.

Apart from what the major computer manufacturers may show within the next two years, at this point only three other companies are dedicated to RISC architectures. And of them, only two have announced products. Although that number may not sound very impressive, both companies are very significant. For one thing, they were the first to take the RISC architecture out of the research environment and bring it to the commercial arena. In their different approaches to reduced-instruction set computers, each is defining the likeliest directions that development will take in the future.

One path, exemplified by Pyramid Technology Corp. (Mountain View, Calif.), is to build large general-purpose machines designed to be cost and performance competitive with minicomputers like the VAX-11/780 but intended to tackle jobs from general accounting, through terminal interactions, to engineering computations.

The other direction, taken by Ridge Computers Inc. (Santa Clara, Calif.), is to bring the power of a VAX to a workstation dedicated to engineering applications such as designing ICs or modeling solids.

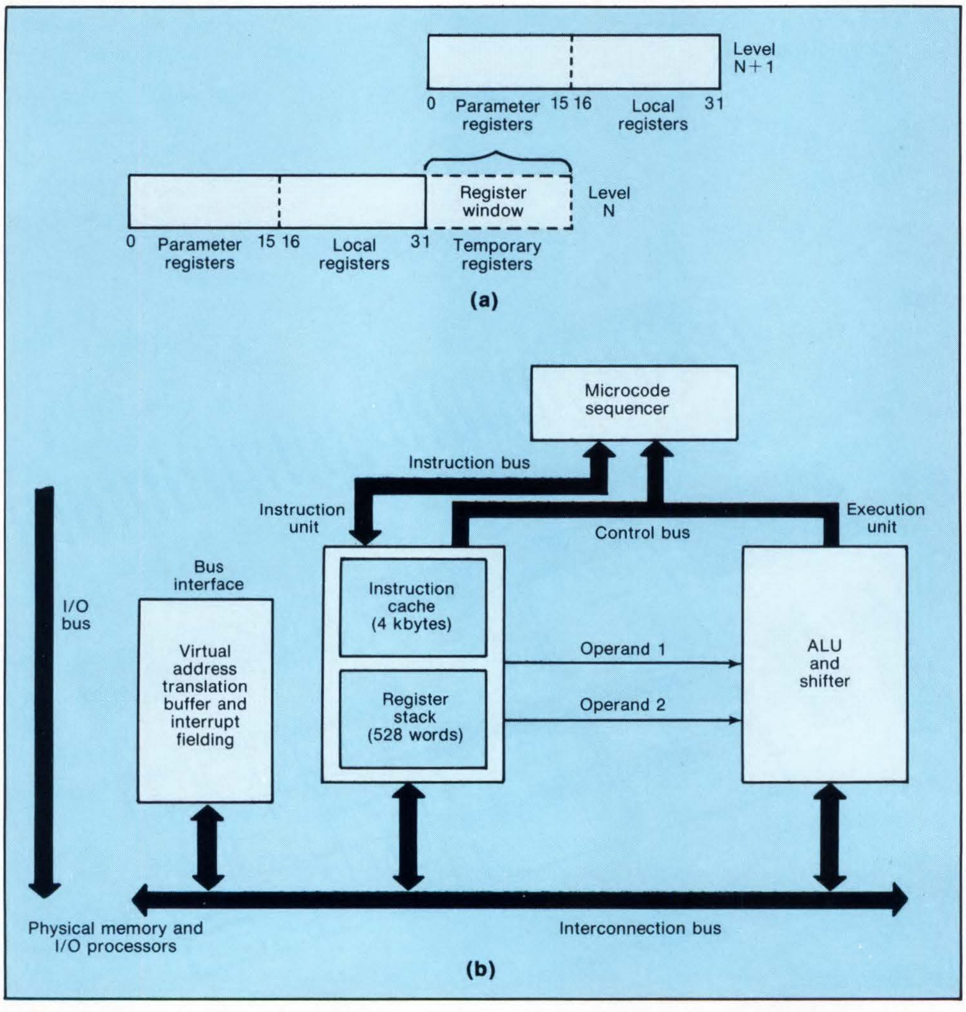
Although the Pyramid 90x is on the books as one of the first commercial reduced-instruction-set machines, most of its performance is attributable not so much to reduced instructions but to a large register stack and overlapped register windows. The design nests procedure calls within 512 separate registers, each of which holds 32 bits. The registers are stacked 16 deep, with 32 at each level. There are 16 global registers as well, which brings the total number of available registers to 528.

When a program is run, only 64 registers are accessible during each machine cycle: 16 global registers, 16 parameter registers, 16 local registers, and 16 temporary registers. The contents of the parameter registers are loaded through a window

from another level, where they occupied a temporary register. The contents of all of the registers are held in a control stack, and the stack pointer is part of the microcode executed by the CPU. This register stack, with its overlapping windows, eliminates many of the memory fetches needed to call up operands, since each operand will pop out of the stack as a machine cycle is completed (Fig. 1a).

A separate instruction bus and microcode sequencer ensure that fetch and execute instructions remained segregated and that instruction fetches will not slow down the machine (Fig. 1b). Pyramid feels that even with low-cost TTL logic devices and a 125-ns cycle time, the 90x will perform 8 to 10 times faster than a conventional machine.

Like the Pyramid computer, the Ridge 32 works with an overlapping register structure consisting of sixteen 32-bit registers. The latter, however, comes closer to being a true RISC architecture in that it



1. Overlapping the register windows on the Pyramid 90x allows data to pass from a temporary register to the top of a stack without a memory-access cycle (a). The machine's instruction bus ensures that fetches and executions proceed rapidly and independently of each other (b).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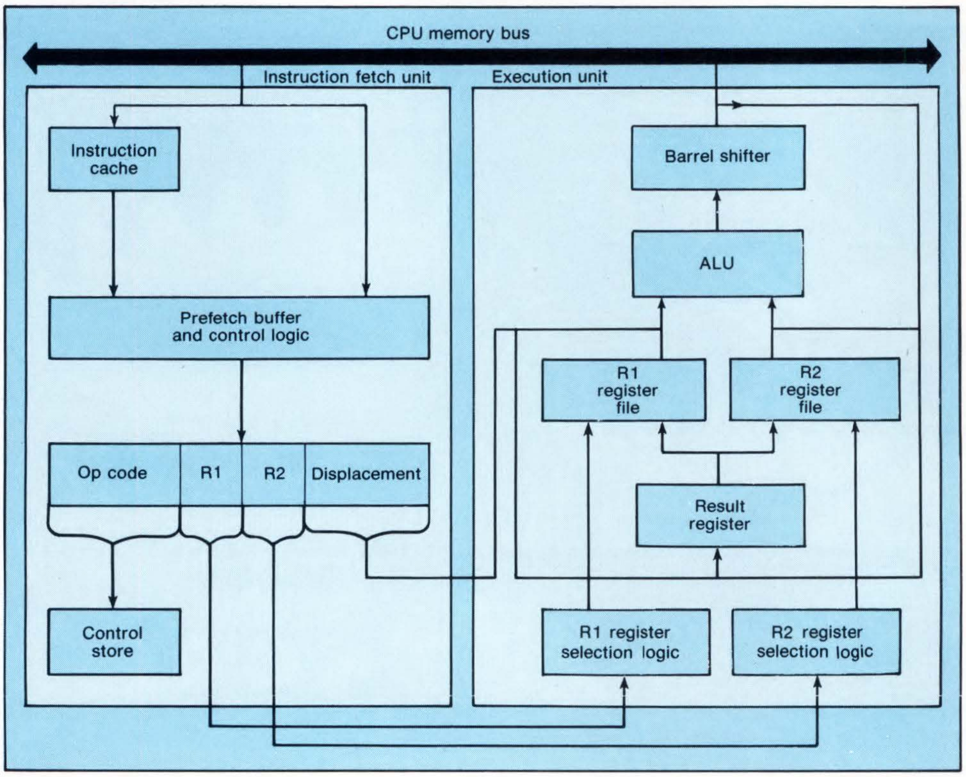
combines a reduced instruction set with an overlapped register structure. Unlike the other machine, which is geared toward general-purpose computing, Ridge's computer is slanted toward engineering applications. As a consequence, the use of the registers will depend on which of the three instruction sets—arithmetic and logic, memory reference, or branch—is being invoked. The arithmetic and logic operations—add, subtract, AND, OR—make the most intensive use of registers, which are, in turn, tightly coupled to the ALU (Fig. 2). The overlapping registers ensure that the computer wastes no time searching for instructions and handles math very fast.

Consequently, the relatively small-sized computer performs I/O operations better than a VAX-11/780 running under a Unix and works out linear equations faster than a VAX-11/750 with a floating-point accelerator (see ELECTRONIC DESIGN, June 28, 1984, p. 61).

Ridge's approach probably calls for large investments in VLSI to replace the present generation of board-level TTL-based RISC CPU's with smaller, faster, and less power-hungry chips and chip sets. It is in this area that the third contender, a new company called MIPS's Computer Systems Inc. (Mountain View, Calif.), hopes to make its mark. MIPS intent is to avoid what it calls the "just another workstation" dilemma, based on 68020, 32032 or 286 chips, by supplying chip sets



2. The CPU of Ridge Computer's System 32 is organized so that an instruction is loaded and memory is accessed at the same time that another instruction is executed. Mathematical functions take the least time, since the carry from previous operations are fed by the prefetch buffer right back to the ALU. Movement through the CPU is typically register to register.

with 5 to 10 times the performance.

In MIPS's view, a successful implementation of the RISC architecture is contingent on three factors: a VLSI chip set that can execute a reduced instruction set; a high-bandwidth memory hierarchy (capable of streaming instructions and operands through the CPU at very high speeds); and optimized compilers that can reformulate high-level languages in terms of more simple requirements.

The limits of RISC are explored at the university level

The only other work in RISC architectures is being conducted at the University of California at Berkeley and at the Computer Systems Laboratory at Stanford University (Palo Alto, Calif). This research is significant, not just because of the running start it gives commercial computer manufacturers, but because it defines most of what is known about RISC architectures. It defines what can be legitimately expected from a RISC machine and at what point its inherent advantages will inevitably trail off.

In pioneering work at Berkeley, advocates of reduced-instruction-set computers are formulating an algorithm that evaluates instructions on the frequency with which they are called, with an eye toward eliminating the extraneous ones (see Table 1, below). Those instructions most often invoked should be executed as quickly as possible, regardless of whether or not they strictly comply with what is thought of as a RISC architecture (see ELECTRONIC DESIGN, Oct. 27, 1983, p. 39). By eliminating many of the complex, seldomly used instructions, it is possible to cut down on the amount of uncommitted logic within a CPU. With fewer gates to open or close, the processor can theoretically be clocked at a much higher rate.

Benchmark tests run at Berkeley on one of the first single-chip CPUs designed to execute a reduced instruction set (the RISC I) appear to validate the overall RISC approach. C-compiler benchmark tests (which include the popular Unix quicksort and puzzle programs) conducted on Berkeley's second iteration of the RISC

Table 1. Call/Return overhead for most time-consuming operation

Statements	Frequency of use (%)	Machine instruction (%)	Memory references (%)
Call/Return: including set up, save, and restore	12	33	45
Loops	3	32	26
Assignment	38	13	15
If	43	21	13
Other	4	1	1
Total	100	100	100

Source: *IEEE Computer*

Table 2. How C stacks up on traditional computers

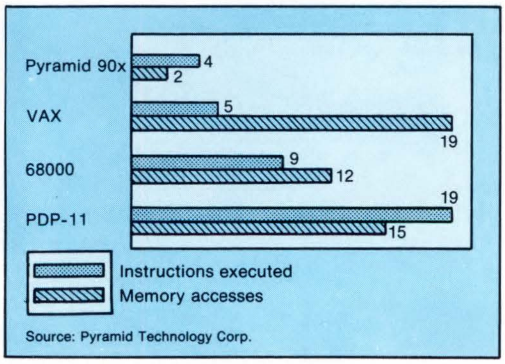
	Time (ms)	Number of instructions	Number of memory accesses
VAX-11/780	26	5	19
PDP-11	22	19	15
68000	19	9	12
RISC I	2	6	0.2

Source: *IEEE Computer*

processor (the RISC II) verify that the processor will compile C programs faster than a VAX-11/780 (see Table 2, p. 184). In case there was any doubt, the results were checked by running the VAX's own compiler program on the RISC machine; and the RISC II's compiler on the VAX. Even simulating the performance of a RISC II processor with a 500-ns machine cycle (most CPU's operate at 400 ns-machine cycle and many are clocked at 125 ns), researchers found that the RISC machine performed integer adds faster than an 8-MHz 286, a 10-MHz 16032, a 12-MHz 68000 and an 18-MHz 9000.

Critics were quick to point out that the puzzle and quicksort, as well as the compilation, were not necessarily good indicators of the RISC architecture's actual abilities. Further, they noted that an integer addition from register to register on a reduced-instruction-set machine cannot legitimately be compared with a memory-to-memory operation done with a microprocessor. Although the jury is still out, the data seems to indicate that when processors are compared for register-to-register additions, the RISC I runs no faster than a 68000 or a VAX CPU.

The only firm conclusion is that the



3. The ratio of instructions executed to memory accesses is higher for a reduced-instruction-set computer (in this case the Pyramid 90x) than for a VAX, a 68000, and a PDP-11. The smaller number of memory accesses means fewer procedure calls and parameter returns.

reduced instruction set is actually only part of the process of streamlining data flow. An equally essential aspect is pipelining instructions and data into the CPU's execution unit.

Nevertheless, the importance of the reduced instruction set should not be downplayed, since it is what is actually addressed by high-level language compilers. Looking at the instruction set for the MIPS computer, a VLSI RISC processor constructed at Stanford, and at a comparable instruction set for the Motorola 68020 is quite revealing. The MIPS processor can be addressed with less than 31 instructions, compared with the 92 needed by the 68020. To illustrate further, the MIPS machine uses one Add instruction while the 68020 requires six.

All RISC machines are not alike, as two instruction sets show

This difference affects not just the ease with which the processor can be programmed, but also the relative simplicity of designing a VLSI RISC processor. The Stanford MIPS processor, for example, is a full 32-bit 8-MHz device constructed with only 25,000 transistors. An 8-MHz 68000, in comparison, demands 68,000 transistors and delivers a data path only 16 bits wide. The Berkeley RISC I, to further heighten the contrast, called for 44,000 transistors and was implemented in silicon in less than 19 man-months—one of the fastest design implementations on record.

Equally important to the RISC philosophy is streamlining fetches. The execution of each simplified instruction depends on having the operand immediately available within the appropriate CPU register at exactly the right moment. All benefits of a RISC architecture are lost if the CPU has to hunt for the numbers it is supposed to add or compare. Research done at Berke-

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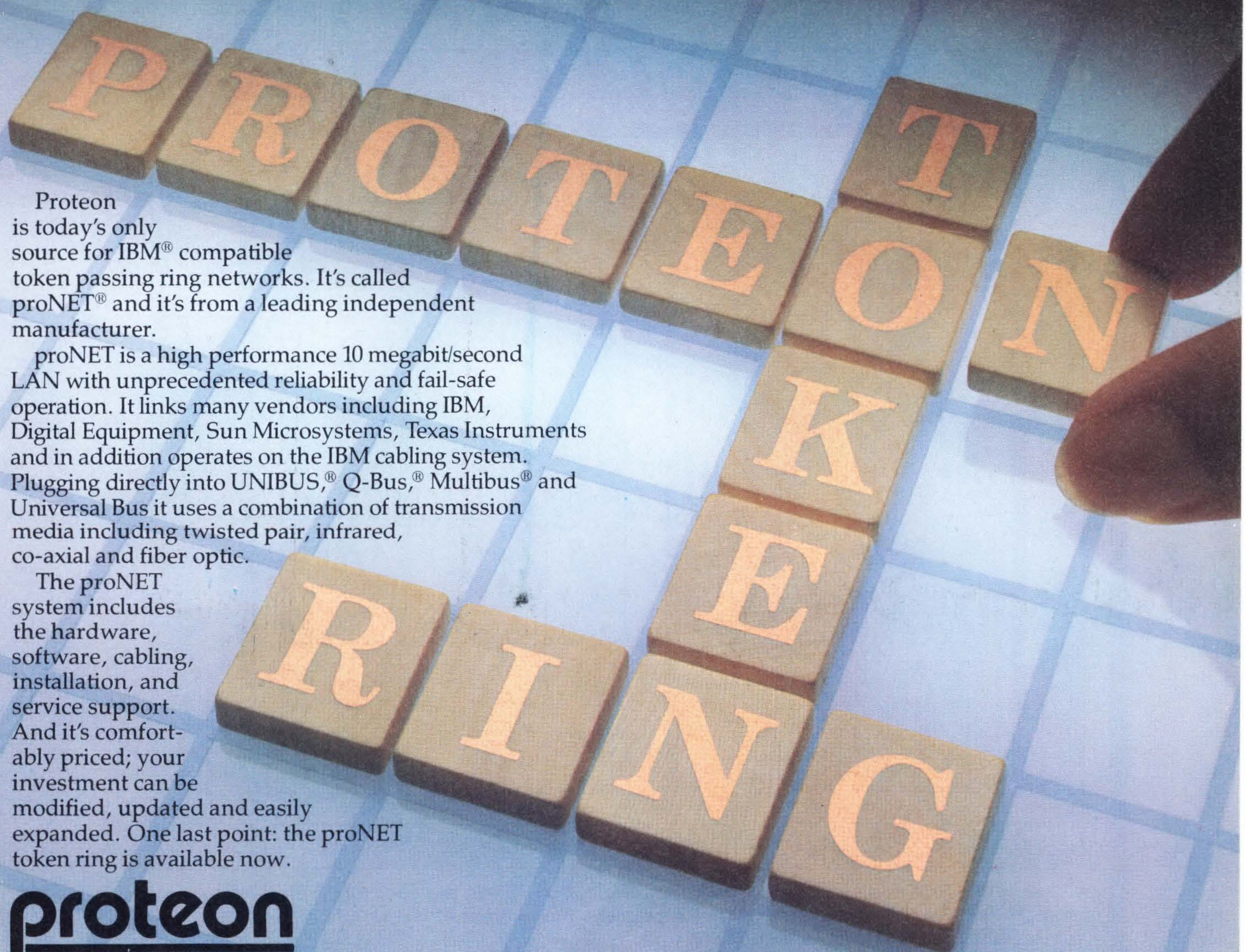

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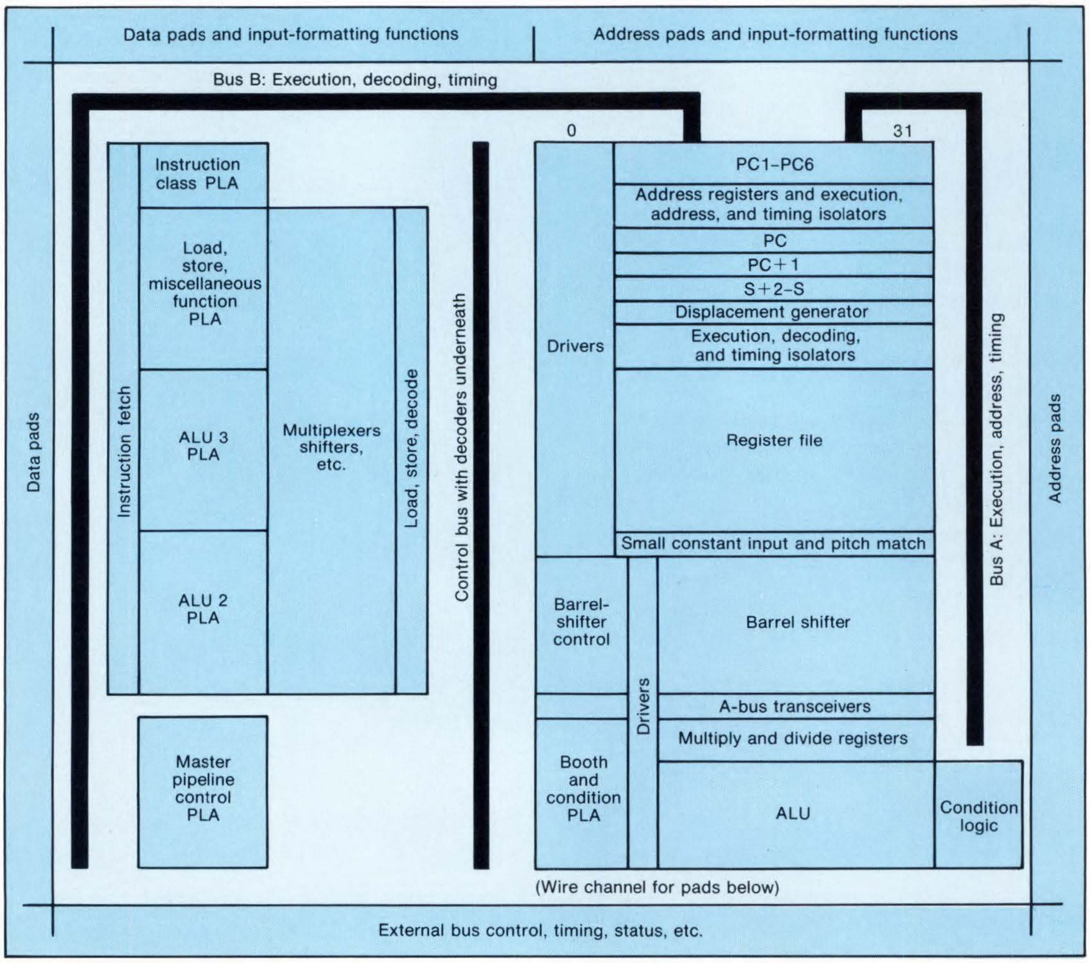
ley verifies that fetches (e.g., Call/Returns, Saves, and Restores) take up the largest segment of any processor's time (Fig. 3). Compared with the VAX and the PDP-11, the RISC I and the Pyramid 90x make far fewer accesses to main memory to accomplish the same tasks.

Thus, a high-bandwidth memory hierarchy must properly place the operands on each execution cycle. A local register-to-register operation obviously proceeds faster than generating an address and a fetch to main memory.

One way of ensuring that operands are located correctly is to put a large multiport register file on the CPU chip. The Stanford MIPS processor does just that, devoting much of its real estate to on-chip registers (Fig. 4).

It is also important to pipeline data and instructions into the CPU at the same speed. For that reason, even a TTL board-level CPU, like the one found in Pyramid's 90x, still keeps a 32-deep register stack on the CPU board to pass along instructions and operands.

The instruction pipeline can be built with simple interlocks to guarantee that



4. One of the first dedicated RISC processor chips, from MIPS, replaces much of the usual memory-fetch logic with registers. The chip halves the number of transistors on a 68000 yet delivers the same processing power.

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there is no contention for resources. This is especially important when register operations are overlapped. The processor can be completing one instruction as the next operand appears.

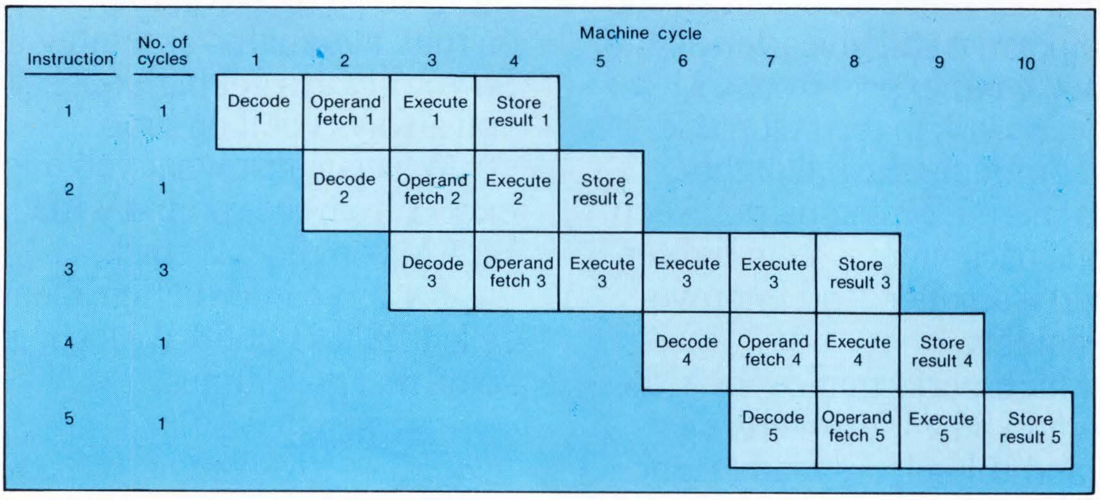
As noted, the processor cannot afford to wait for an operand. Nor can the pipeline push data prematurely into the stream, since binary-coded instructions might be mistaken for operands. The simple solution to this problem is to sequence the flow of numbers into the register stack from three separate feed registers: one for the ALU, one for the on-chip instruction memory registers, and one from local data registers (Fig. 5).

Another important consideration is that the caches must be accessible at every cycle. When addresses must be generated for a memory fetch, parallel translation lookahead buffers take care of the job quickly. In the Ridge 32, for instance, a pipelined execution unit is employed in conjunction with an instruction cache and a prefetch register to ensure that memory accesses and instruction loads are accomplished at the same time that another instruction is executed.

A math or floating-point coprocessor can be tightly coupled to the main CPU to make certain that floating-point operations eat up little overhead (ELECTRONIC DESIGN, Sept. 6, 1984, p. 38). An optimizing compiler, meanwhile, can rearrange instructions to overlap storage, branch, or coprocessor delays, or all three, with useful computations.

Such optimizing compilers are based on new algorithms devised at Stanford (the U-Code compiler) and at IBM. They make very efficient use of a uniform and fast register set and work best with simple instruction sets. The first generation of these compilers, in develoment at MIPS, will reformulate C, Pascal, and Fortran instructions to meet the more simple RISC requirements. Later RISC compilers will accommodate Cobol and Basic, and all will run under Unix System V with Berkeley 4.2 extensions.

Since the RISC compilers are compatible with a variety of high-level languages, the differences in instruction sets between a complex computer and a RISC machine are actually invisible to the user. Application programs written in high-level languages can thus be easily transported to reduced-instruction-set machines.□



5. A key requirement of the RISC architecture is overlapping register windows. This arrangement makes it possible to fetch an instruction at the same time that one operand is called up and another is decoded.

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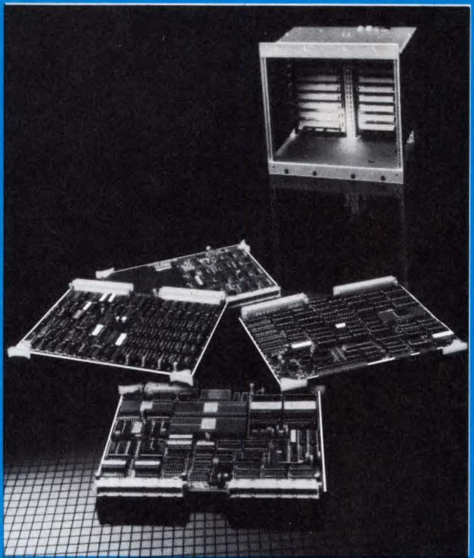

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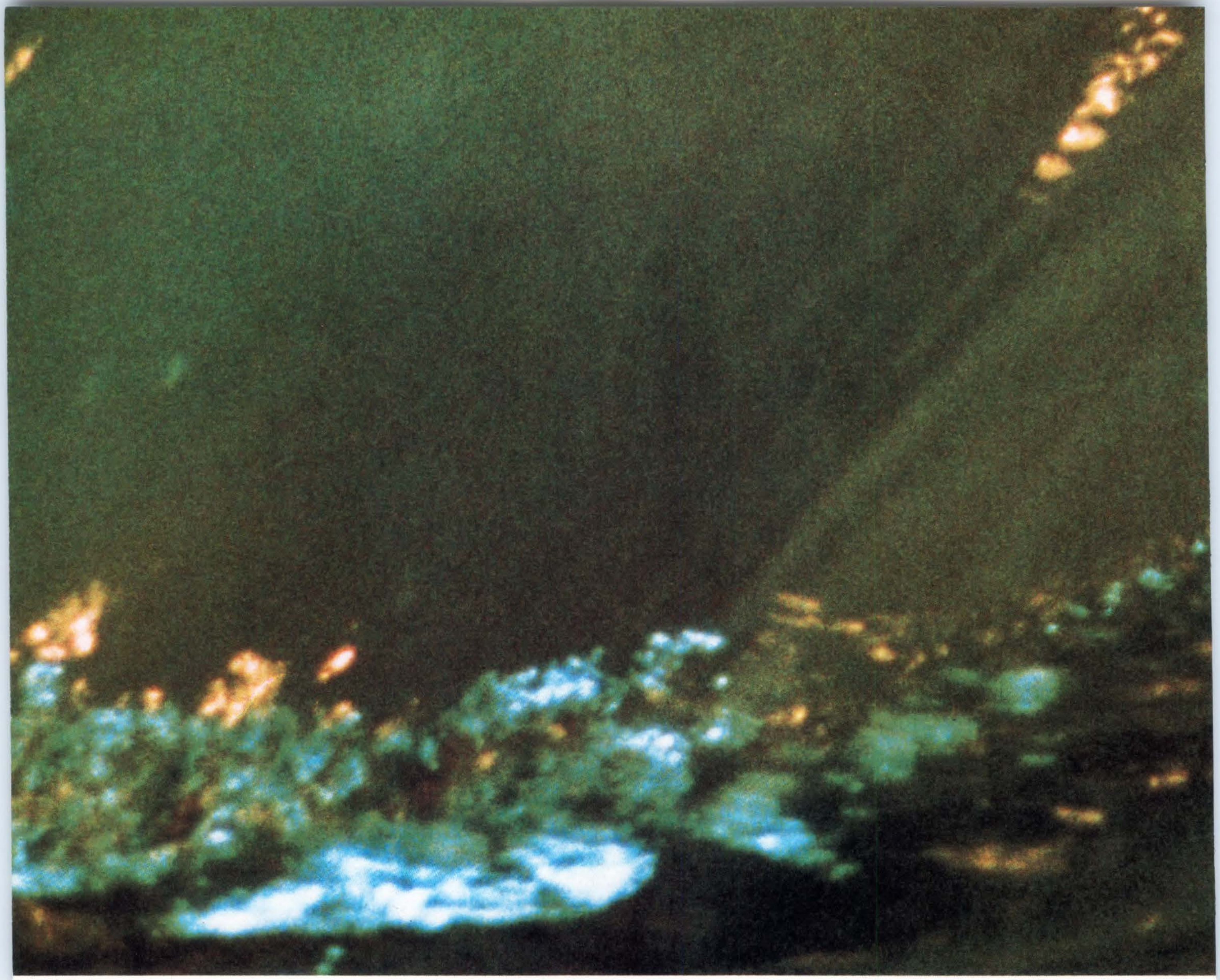

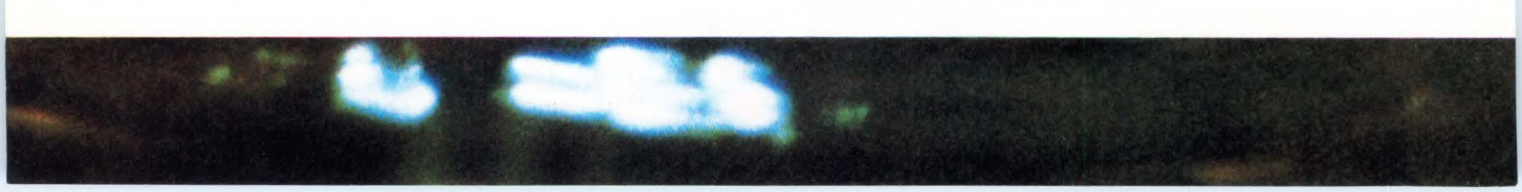

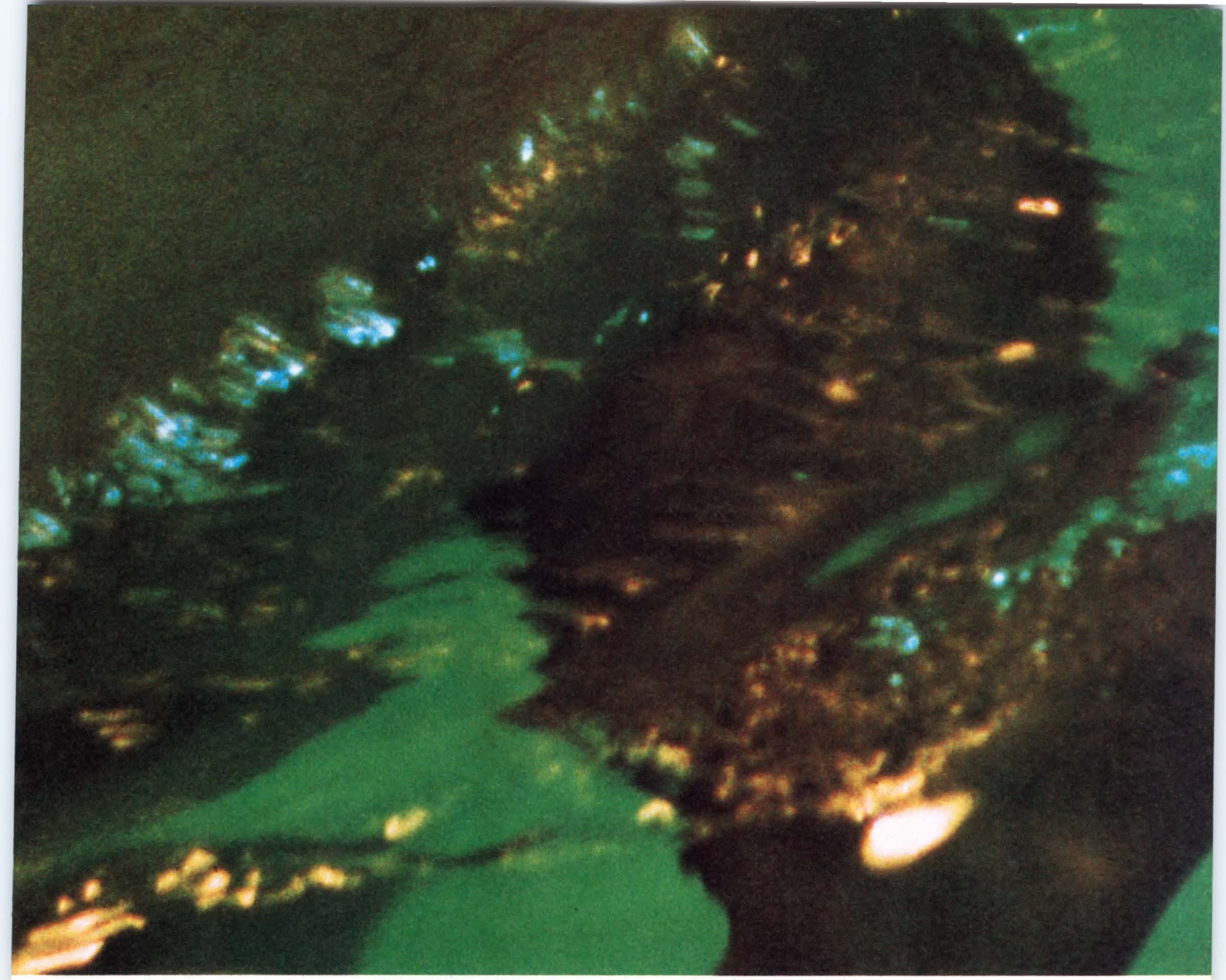


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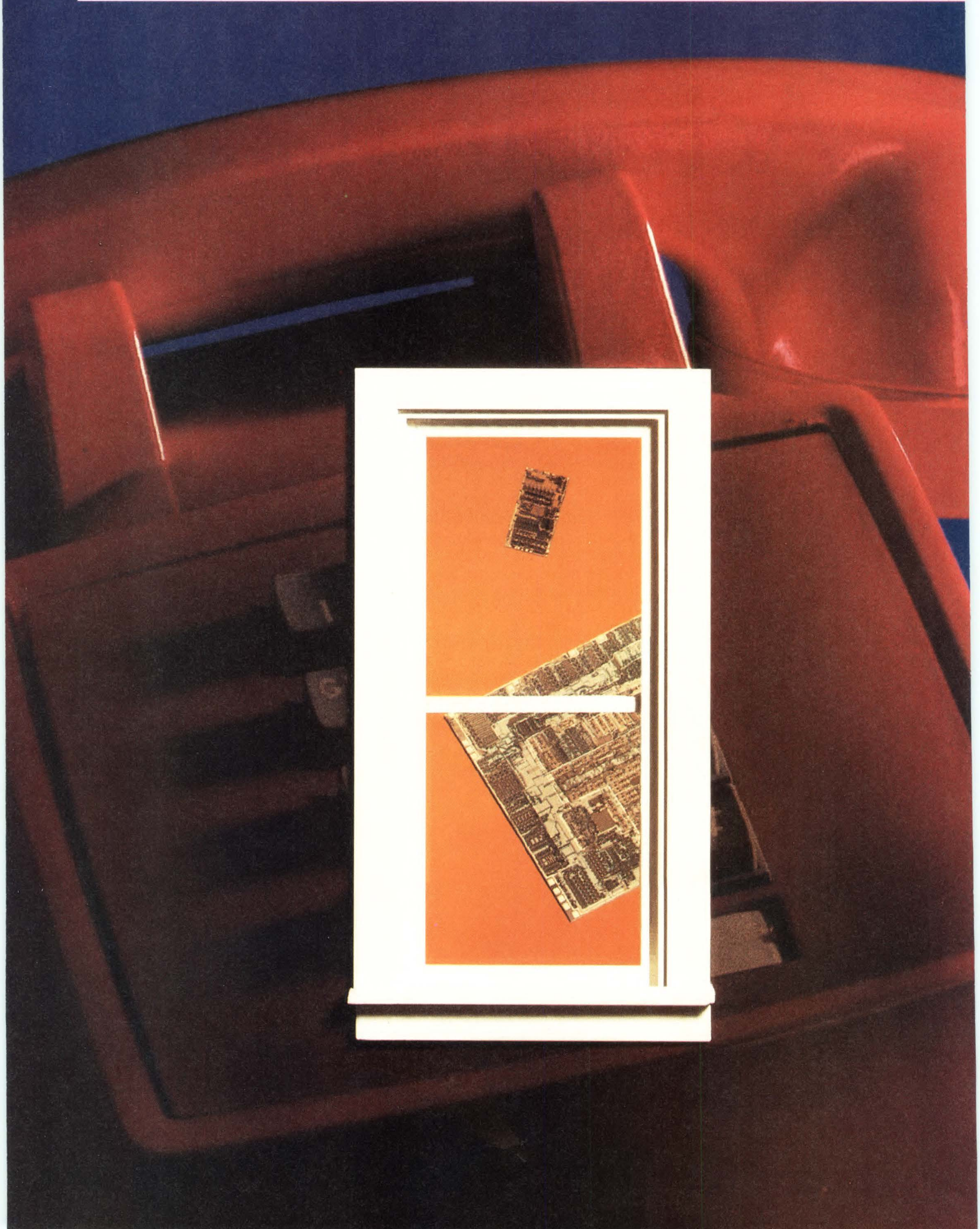


TELECOMMUNICATION INTEGRATED CIRCUITS

"Plain old telephone service" is no longer plain. In fact, by converting from analog to digital transmission techniques, the nationwide switched telephone network is undergoing a facelift that should change the profile of telecommunications worldwide. Consider the benefits: vast numbers of voice channels crammed into one line, extremely efficient switching of signals, the intermingling of voice and data signals, and the possibility of exchanging information at rates exceeding more than just a few kilobits a second.

The move to a totally digital system started in the central telephone offices and is now reaching factories and offices. One day soon it will penetrate the home as well (Fig. 1). The revolutionary changes are due largely to advances in solid-state devices now being placed on line cards, which terminate each subscriber line at a central of-

FRANK GOODENOUGH

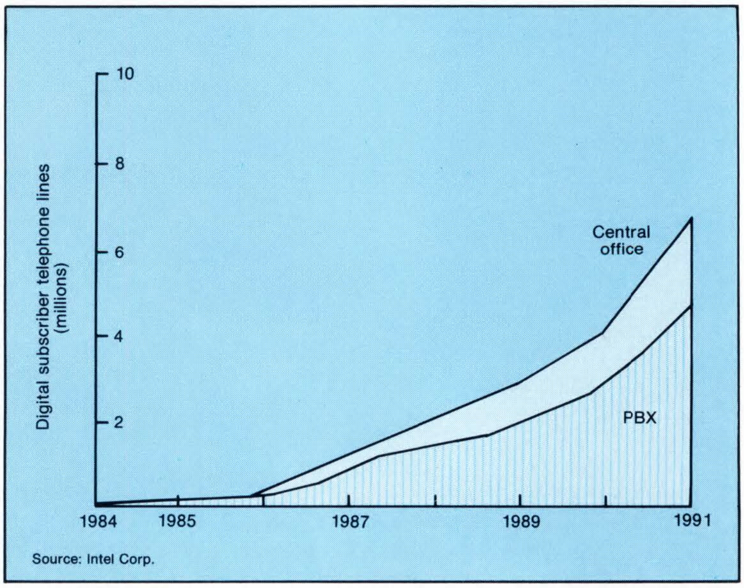
which terminate each subscriber line at a central office or a private branch exchange (PBX). Line card circuits, long built with discrete and hybrid parts, have matured into integrated circuits. Second-generation ICs are now appearing, as are the first ICs for functions that previously defied integration.

Digital signal processing will determine the shape of future telecomm ICs

New phone services are inviting a raft of other chips, ranging from digital line card controllers, time-slot assigners, and pulse-code-modulated switching networks to codec-filters, SLICs, and even special-purpose power supplies. More than any other contributing factor, these chips exploit new techniques in fabrication, advances that have produced fast, dense, and low-power digital ICs; combined high- and low-voltage analog and digital circuits; and dielectrically isolated chips that withstand 1500 V.

Digital signal-processing techniques will be perhaps the most impressive influence in telecommunication ICs, allowing them to replace analog filters in codecs, to cancel echoes, and to adjust a telephone line's impedance and longitudinal balance (common-mode rejection). Ultimately, denser CMOS processes will get the credit for allowing chips to put voice and data signals on ordinary phone lines, most likely over the relatively new Integrated Services Digital Network (ISDN).

Though still being defined, the ISDN

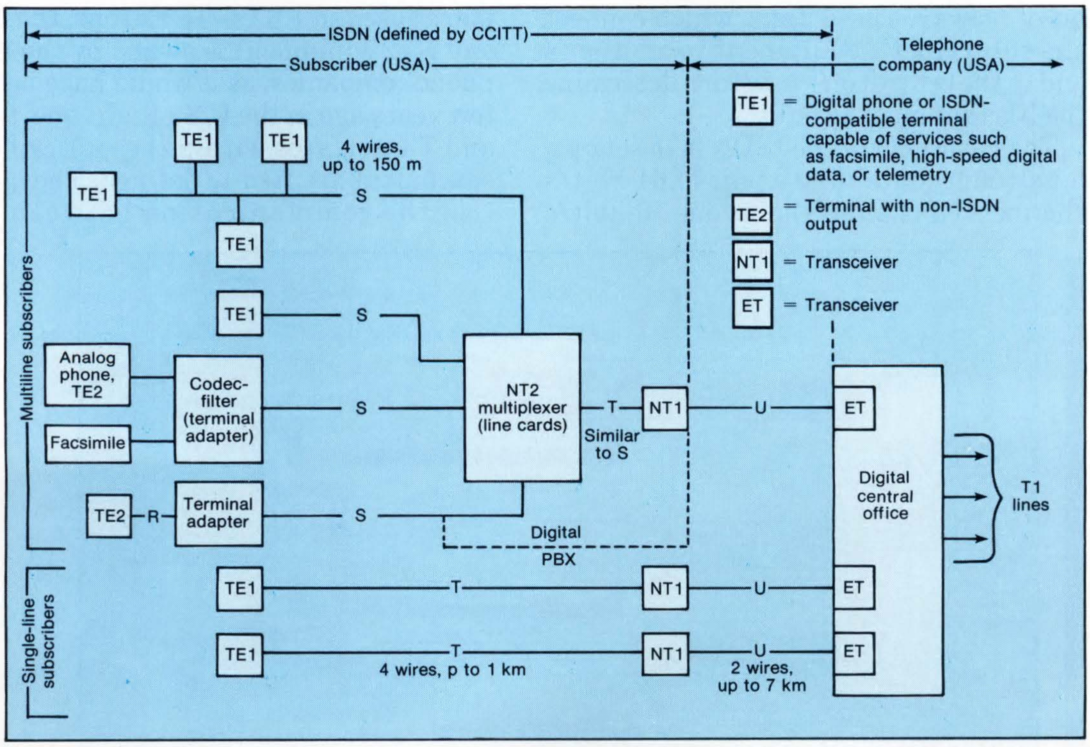


1. With the advent of the Integrated Services Digital Network, the number of telephone lines capable of carrying digitized signals—both voice and data—will increase dramatically over the next few years.

spells out simultaneous full-duplex computer-to-computer and voice-to-voice communications over an ordinary phone line at a rate of 64 kbits/s. It will be put to work first either on the lines in offices and factories that pass through PBXs or on the lines between subscribers and central offices, where the latter perform the PBX function. Later, the network will appear on the subscriber lines between homes and central offices.

The original switched telephone network was designed to do just one job: provide efficient, reliable voice communications. It did, and does, that job superlatively. However, with the exception of a few recently added services, it cannot handle raw digital data at all—hence the need for a modem to put digital data over analog lines. The popularity of modems will only rise over the next two to ten years, pushed on primarily by PBXs and personal computers. In fact, industry estimates claim that every personal computer built after 1986 will sport a modem.

Besides modems, the phone system will enjoy much broader use of both dual-tone multifrequency signaling chips and speaker phones, the latter geared for home systems. The industry is now working on special DTMF chips for building alarm systems, gathering data at low rates from remote sites (rainfall and temperature readings), verifying credit cards, and controlling processes and appliances. For their part, speaker phones will be incorporated into terminals and modem-equipped personal computers, thus permitting hands-free operation. Nevertheless, DTMF chips and speaker phones are really



2. A complete ISDN line transmits signals on two voice or data channels at 64 kbits/s full duplex. An additional 16-kbit/s packet-switching data channel carries control and signaling information.

waiting for ISDN before they can take off.

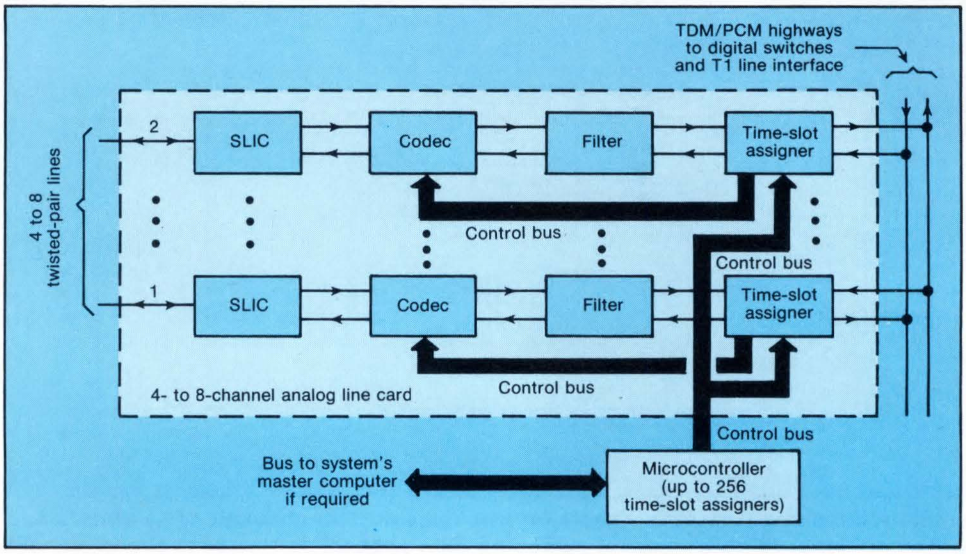
The ISDN is an international concept for digital telecommunications. Its basic characteristics are recommended by the International Consultative Committee on Telephony and Telegraphy (CCITT), and in the United States its standards are being nurtured by the T1-D1 committee, which was formed by major phone companies after the breakup of AT&T.

ISDN—an international concept—will handle voice and data, simultaneously

In simplest terms, the CCITT's recommended standards consist of a set of interfaces or communication links, with their physical, electrical, and procedural characteristics defined either firmly or with a bit of leeway. These links, which connect one subscriber's equipment to another's and to the central office, in turn determine the ICs that must be built.

The basic goal of the ISDN is to set up a bit stream containing a pair of 64-kbit/s channels (B channels) plus one 16-kbit/s channel (D channel). Each B channel carries voice signals or high-speed data, whereas the packet-switching D channel is responsible for B channel signaling or for low-rate data flow or telemetry. Besides those three channels, the ISDN specifies a rate of up to 48 kbits/s for framing and maintenance. All told, the resulting data rate can climb as high as 192 kbits/s.

The specifications apply to all the equipment on the user's premises that handles part or all of that bit stream (Fig. 2). It includes the TE1 terminals, which can be digital phones, high-speed data sources, or video or facsimile machines; terminal adapters, which convert non-ISDN data (RS-232, for example) into ISDN format (R interface); codec-filters, which handle the signal from an ordinary telephone; the NT1 transceiver connected between the S and the U interfaces; and the NT2 multiplexer used in PBXs. (In Europe, the NT1 and NT2 equipment is owned by the telephone companies, as it would have been a few years ago in the U.S.) Right now the S and T interfaces within the subscriber's equipment are firmly defined. They control the communication between the



3. Analog line cards convert telephone signals into time-division-multiplexed, pulse-code-modulated (TDM/PCM) signals at central offices and in PBXs.

client, a company's on-site equipment, and the two-wire phone line to the central office.

The S interface carries the 192 kits/s on four wires for distances of up to a kilometer over point-to-point links. For multidrop links, the maximum distance ranges from 150 meters to 1 km. In addition, a bit in the D channel resolves contention problems.

TCM's biggest problem may be that it interferes with AM radio

The U interface, which is necessary for regulatory purposes, is still being defined by the T1-D1 committee and may, in fact, turn out differently in Europe and America. The final definition will represent a trade-off between technology and cost. The interface is expected to be a two-wire, full-duplex line capable of operating over 7 km. The signaling and control rates can be limited to 18 kbits/s, resulting in a total bit rate of 162 kbits/s.

Two different techniques have been proposed for transmitting ISDN-formatted data over these lines; ping-pong and echo canceling. In the ping-pong scheme, which is based on time-compression multiplexing (TCM), the 162-kbit/s data stream is transmitted at twice that speed or faster, first in one direction and then in the other, over a two-wire line. Actually a half-duplex setup, it appears to the user like a full-duplex system transmitting data at 162 kits/s. Time-compression multiplexing makes the transceiver at one end of the line a master, the one at the other end a slave. If the technique is used over the longest line possible, adaptive line equalization must be employed to reduce the effects of line imperfections on the high-speed transmission. Extra circuitry, in that case, senses the amplitude and phase errors and compensates for them.

With echo canceling, on the other hand, the signals may actually be transmitted in both directions at the same time, as on present voice lines. However, at each end of the line, a replicated echo of the transmitted signal must be subtracted from the received signal—a difficult job to do precisely. In fact, the operation demands that each receiver keep track of the signal it transmitted a few milliseconds earlier, a task traditionally done with analog techniques but now leaning toward digital signal processing.

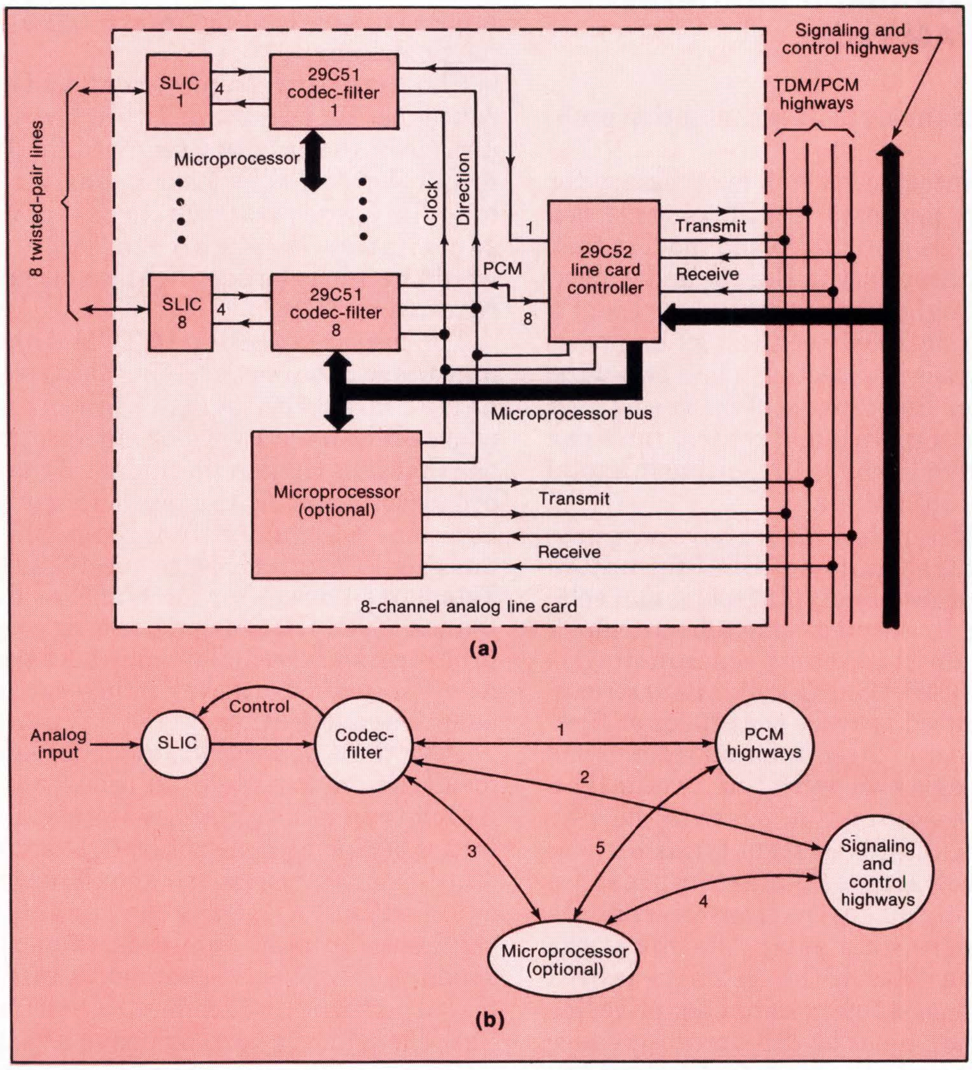
Choosing between ping-pong and echo canceling can be quite difficult. For short distances, the circuitry required for TCM is simpler and thus less expensive. For long lines, the total system cost of echo cancellation is roughly the same as it would be with the equalization circuitry required by TCM.

The major objection to TCM, though may prove to be one involving electromagnetic compatibility. Its high bit rate causes it to have a very broad spectrum, one that falls right in the middle of the AM broadcasting band. As a result, it may turn out to be economically impossible for meeting FCC interference specifications. Telephone lines, after all, make good antennas. Even if TCM can overcome those problems, there remains some doubt as to whether it can work over 7 km, even with adaptive equalization.

Despite its drawbacks, the technique is ideally suited to remote multiplexer units, which transfer signals over only a few inches of a printed circuit board, virtually eliminating any concern about adaptive equalization. RMUs, as they are called, originally brought hundreds, even thousands of lines over 24-channel T1 carriers to locations within 10 miles of a central office. Thought of as extensions to a central office, the multiplexer units physically sit in a box mounted on a telephone pole, buried underground, or lost in the bowels of an office building. For the past few years they have been used to cram ever higher numbers of phone lines into the already crowded ducts under city streets.

Right now, their internal analog line cards connect them to the T1 interface and what the ISDN specification might call the V interface. That interface governs the signals between a line card within a PBX or central office and the remote multiplexer or other signal-generating circuit for the T1 lines.

As the ISDN concept moves from debate to reality, the remote multiplexer unit—along with many other circuits—will begin the transition from analog to digital line cards. But how far away is ISDN, where is the requisite equipment, and where are the chips? Under the auspices of Bell Communications Research Corp. (Livingston, N.J.), initial system tests are



4. Third-generation line cards combine codec-filter functions on one chip and put eight time-slot assigners on a line card controller (a). A microprocessor on the card adds local control. The overall architecture equips the card with five separate signal and control paths (b).

scheduled for late 1986, even though the specifications are not scheduled for release until late this year. The trials will be carried out by several telephone operating companies in both PBX and Centrex systems (in the latter, the central office handles PBX functions).

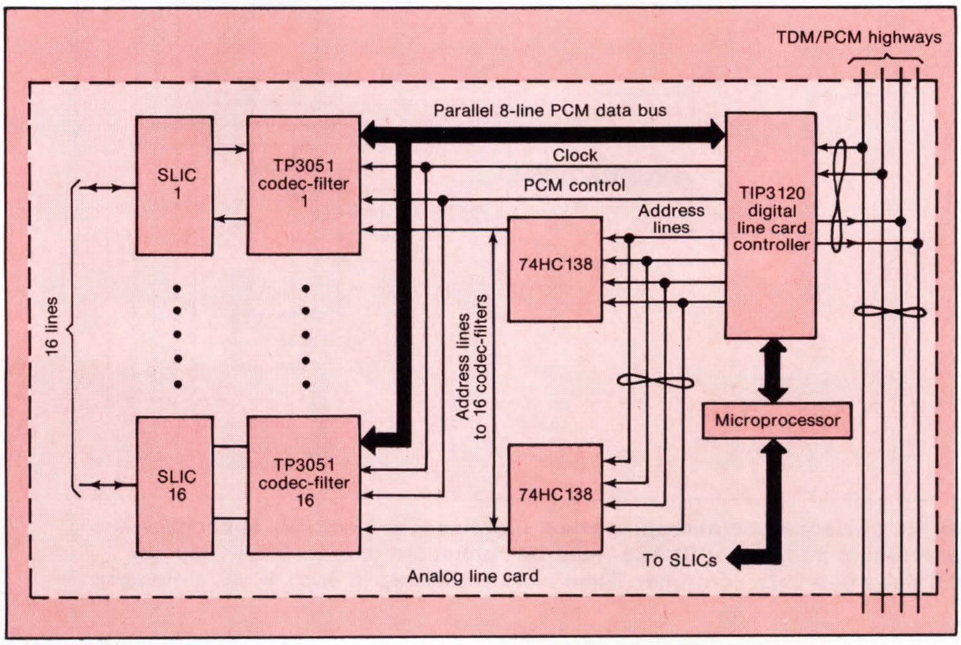
"For years to come, analog and digital line cards will be working side by side."

Many of the ICs required for ISDN exist now, riding on line cards in digital PBXs and central offices. Others are still evolving. One thing is certain: For years to come, analog and digital line cards will be working side by side.

The typical analog line card handles four to eight channels or input lines (Fig. 3). In addition to active and passive discrete parts and several relays per channel, future boards will need several ICs per channel: a subscriber line interface circuit (SLIC), a codec, its attendant filter, and a time-slot assigner. The last of those chips, under the control of an external microprocessor or computer, connects each channel at exactly the right time to the four-wire PCM highway running around the PBX. That is, it supervises the time-division multiplexing of the codec's PCM outputs.

The SLIC is best characterized not as an IC but as a multichip hybrid. When translated into IC form, it most likely will be bipolar and rely extensively on external devices to do its job, even in a benign environment like a PBX.

In comparison, codec-filter chips have been talked about and some introduced over the past 18 months, including entries from Motorola Semiconductor Products Inc. (Phoenix, Ariz.) and Gould Inc.'s AMI Semiconductors (Santa Clara, Calif.). To their own versions of the codec-filter, National Semiconductor Corp. (Santa Clara)

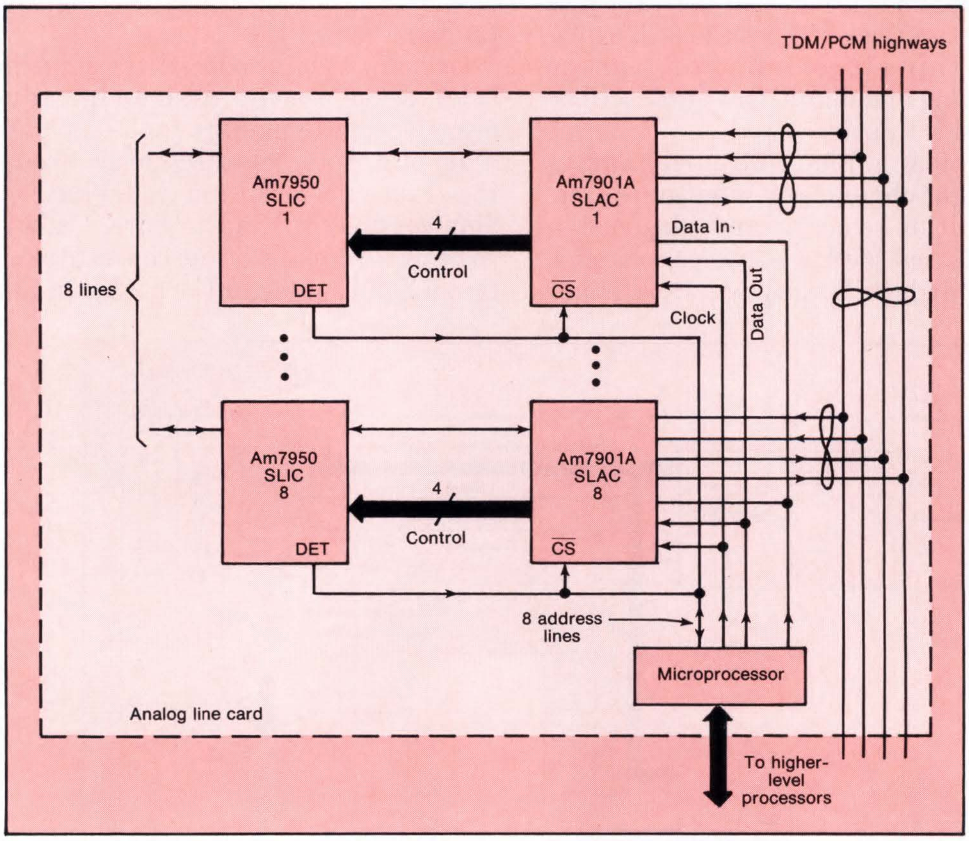


5. An eight-line parallel data bus running between codecs, the line card controller, and TDM/PCM (time-division multiplexing/pulse-code modulation) highways permits the controller chip to handle 16 lines at high speed.

and Mostek Corp. (Carrollton, Texas) each have added a power amplifier that can drive low-impedance transformers on the line side of the chip.

Though the integration level of those second-generation chips may be admirable, the third generation will actually make ISDN happen, since those chips will create an analog line card compatible with digital ones. Outwardly, the analog cards will change little, but their internal architecture and the chips or chip sets they incorporate will differ dramatically. For instance, codec-filters will perform their expected functions, assume many SLIC duties, and possibly even control that circuit. And a new chip, called a line card controller, will take on the task of assigning time slots for 8 or 16 channels.

In addition, boards or chip sets will sport parallel rather than serial interfaces between the codec-filter and the line card controller. Finally, one third-generation set draws on digital signal-processing techniques and in so doing could replace equivalent circuits based on pure analog and switched-capacitor designs. Overall, these new architectures will raise to un-



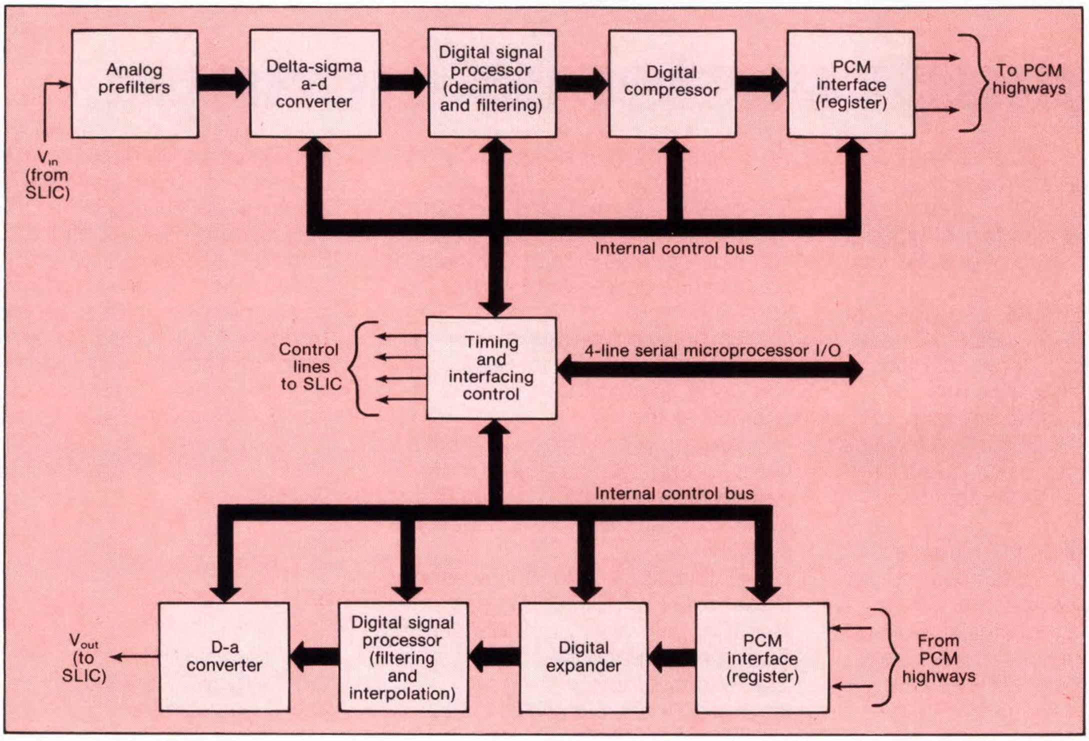
6. Under the guidance of a microprocessor, eight codecs—actually subscriber line audio processing circuits, or SLACs—can be connected to the TDM/PCM highways without a line card controller. Time slots are stored in each SLAC's memory.

precedented heights the programmability and flexibility of system designs.

Consider one architectural example that combines the line card controller chip with a codec-filter and also retains serial communication between those components. The circuitry, developed by Intel Corp. (Santa Clara), enables only one analog line card to handle eight subscriber lines, using eight SLICs, eight codec-filters, and one controller. In fact, the setup's 8-bit address would allow 32 controller chips to work with 256 subscriber lines. The line card operates with the ping-pong approach.

New circuitry allows one analog line card to handle eight lines

The controller chip, which performs the first stage of space-time switching of the PCM outputs, concentrates and multiplexes all digital information that passes between the card and the next higher level of control and switching (Fig. 4). It controls five separate paths on the card, one each for connecting the codecs to the PCM highways in the PBX, to the signal and control highways, and to a microprocessor. The chip also sets up the protocol and control functions for all information flowing between the card and the next switching level. It transmits message packets over the signal and control highways or disassembles them and puts them into a time slot on the TDM/PCM highways. The line card's codec acts as a slave to the controller chip. In fact, the PCM highway from the codecs is called the Slave Data line, which along with the



7. A SLAC tackles virtually all normally analog functions in an on-chip digital signal processor. Its functions include filtering and companding the signal after it has passed through the analog-to-digital converter.

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Slave Clock and Slave Direction lines, controls the codecs.

The codec-filter, like its second-generation NMOS predecessor, boasts external gain adjustment, μ- and A-law companding (U.S. and Europe, respectively), and a programmable power-down mode. To these features, Intel has added three internal and two external hybrid networks (two- into four-wire conversion), gain control for transmitting and receiving, three loopback modes for testing the card and its

Inside the phone system

Over the past twenty or thirty years, the nationwide telephone system has evolved into a vehicle that can efficiently handle millions of analog transmissions each day over about 90 million lines across the U.S. Essentially the system's job breaks down into a few apparently simple functions, including converting sound into an analog voltage, transmitting the analog signal to the central office, and switching signals. With the exception of dialing, ringing, and other things going on in the handset, the user—or subscriber—is virtually oblivious of the other functions.

The simple handset provides inverted-polarity and transient protection, the first through diode bridges and the second through zeners, varistors, and other discrete components. In so-called "speech" circuits, the handset also converts the two-wire lines into the four-wire signals required for connection to the earphone and microphone—actually, the BORSCHT hybrid function.

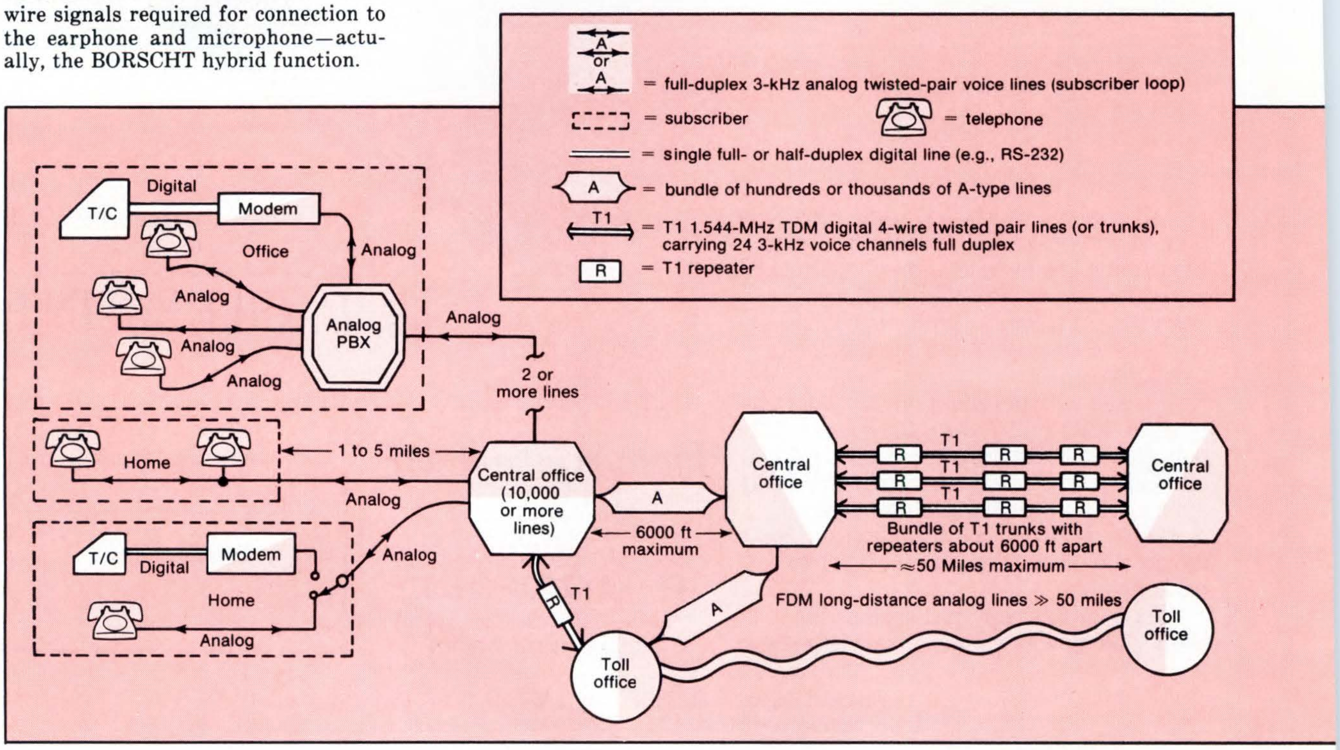
In addition, telephone circuits match transducer impedance to that of the line, compensate for line length, perform automatic gain control, and ensure that the correct amount of transmitted signal is heard by the user. Dialing circuits encode the tones and also transmit a muting signal during dialing.

The telephone circuitry must work with three signal levels: the received voice signal, which could be as low as a few millivolts rms; a transmitted signal of 1 to 2 V rms: and finally an incoming ring signal of 90 V rms. However, they must also accept dc power—48 V at 15 to 80 mA.

In telephone system talk, the pair of wires leading to the subscriber are called Tip and Ring. The former is at ground potential, the second is the hot line at −48 V. Until the phone is removed from the hook, only the ring circuits are connected to the line.

The subscriber's telephone line is #22 twisted-pair wire that usually handles signals between 300 Hz and 4 kHz but in reality can work at several megahertz. (The bandwidth of ISDN is more than 4 kHz.) The twisted-pair line, or trunk, runs a few hundred to a few thousand feet to a PBX system in an office or factory or to a telephone operating company's central office. The trunk line can stretch about a mile in densely populated areas, five or six miles in suburban or rural settings.

The primary function of the PBX and central office is the same: switching one telephone line to another. In addition, most central offices multiplex many conversations onto one channel or line. The multiplexing may be based either on time or frequency division, and the transmitted signals may be analog or



chips, and extra analog channels for controlling SLICs and setting up three-way conference calls.

The chip's three loopback modes illustrate its sophisticated design. With digital loopback, the chip retransmits the PCM signal to the controller chip, verifying and testing the path from the PCM highway to the slave codec. Analog loopback, in contrast, connects the analog output to the analog input on the SLIC side of the chip, an arrangement that permits functional

digital.

Before switching at the PBX or central office, circuitry residing on the analog line cards (digital cards, in the future) tackles the so-called BORSCHT functions for their line:

- Battery feeding—supplying the −48 V at 15 to 80 mA power required by the telephone service.
- Overvoltage protection—Guarding against induced lightning strike transients.
- Ringing—Producing the 90-V rms signal shared by all lines; a relay connects the ring generator to the line.
- Supervision—Alerting the central office to on- and off-hook conditions (dial tone, ringing, operator requests, busy signals); also the office's way of auditing the line for billing.
- Coding—if the central office uses digital switching or is connected to TDM/PCM digital lines, there are codecs and their associated filters on the line card.
- Hybrid—Separating the two-wire subscriber loop into two two-wire pairs for transmitting and receiving.
- Testing—Enabling the central office to test the subscriber's line.

Right now half of all central-office switching, and virtually all of that handled by PBXs is analog.

The switches themselves range from stepping switches and banks of relays to crossbar switches and crosspoint arrays of solid-state switches. They are slow, have limited bandwidth, eat up space, consume lots of power, and are difficult to control with microprocessors or even CPUs.

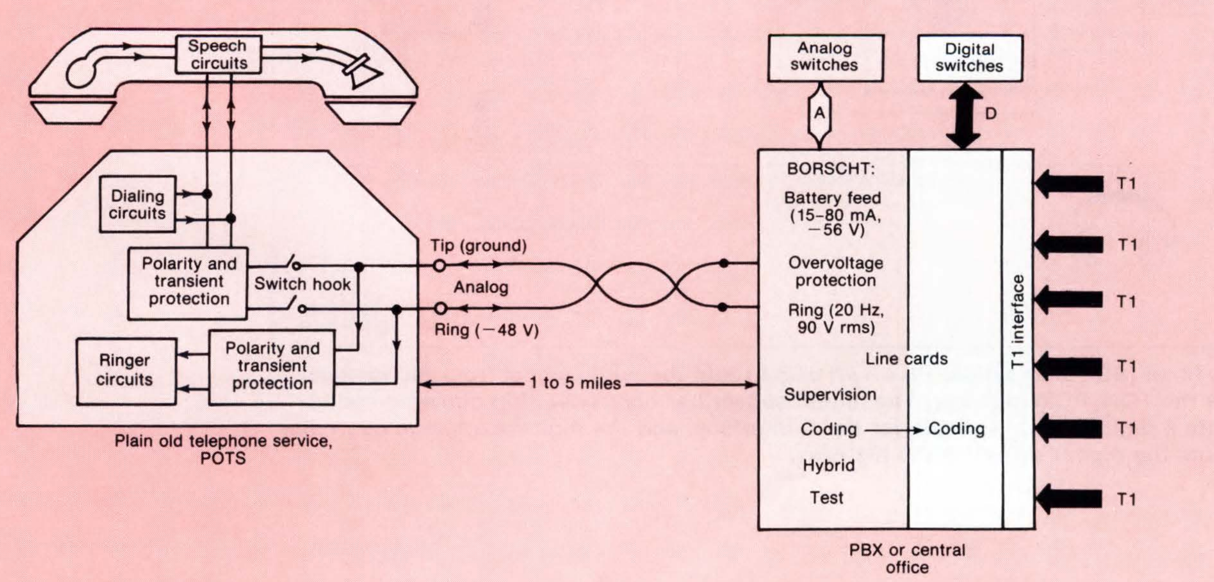
To overcome the limitations inherent in analog switching and to enable central offices to use TDM/PCM links in urban areas, telephone companies started converting to digital transmission using 8-bit words. The conversion will be virtually complete by 1990.

Bundles of twisted-pair wires running between line cards and switches have been replaced with a few serial time-division-multiplexed PCM highways. Since each 4000-Hz signal (limited in bandwidth to 300 to 3000 Hz) must be sampled at a Nyquist rate of 8 kHz, 8-bit words produce a 64-kbit/s bit stream, which flows onto the PCM highway to the switches. Those switches are now complex logic circuits controlled by CPUs and microprocessors. A given voice channel occupies just one time slot in the TDM PCM signal.

Digitally switched digital signals may flow between two analog lines coming into the central office. In that case, they are returned to a line card, reconverted into analog form, and sent over an analog line either directly to a subscriber or in a bundle of lines to a central office.

On the other hand, if the digital words are multiplexed onto a T1 carrier en route to another office, the serial bit stream is converted into the equivalent of 24 voice channels plus supervisory, signaling, and framing bits. Frames are transmitted every 125 μs, representing an effective bandwidth of 1.544 MHz.

Bundles of T1 lines carry most voice channels between central offices in densely populated areas. If the lines stretch more than 6000 feet or so, a repeater amplifies the signal and regenerates its timing.



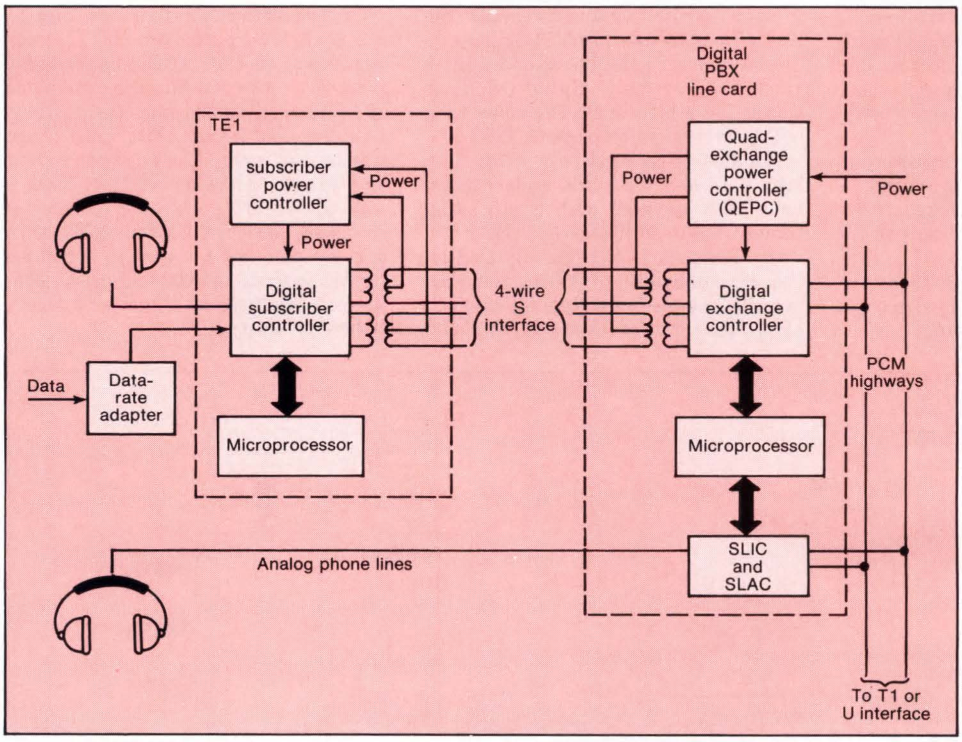
testing and gain adjustment. The last mode, subscriber loopback, connects the output of an analog-to-digital converter to the input of a digital-to-analog converter. The signal is thus compared with itself.

The high bandwidth of ISDN demands innovative approaches

The codec enters any one of these loopback modes in response to an 8-bit word inserted on the Slave Data line.

The higher bandwidth of ISDN systems demands innovative approaches to analog line cards. For instance, a built-in parallel PCM highway characterizes the latest subsystem from National Semiconductor Corp. Here the codec-filters interface with a line card controller chip (called a digital line interface circuit, or DLIC, by National) over a bidirectional parallel bus, which empties onto TDM/PCM highways (Fig. 5). Unlike the Intel circuit, this controller chip works with 16 rather than 8 codec-filters.

The mandatory microprocessor in this analog line card interfaces with the controller and the SLICs but not with the codecs. National's codec-filters, dubbed combos, employ switched capacitors, can power-down to less than 2 mW, and feature a power amplifier that drives low-impedance loads on the analog line. One version, the TP3051, handle only μ-law



8. In an ISDN-compatible PBX, two chips route the audio signal from the handset to the TDM/PCM highway. The digital subscriber controller chip converts sound into a digital signal suitable for the S interface, and the digital exchange controller puts the digital signal on the highway.

companding; the TP3056, A-law companding.

Bucking the trend, a third-generation chip set gets rid of the line card controller completely; instead it connects the codecs' PCM output directly to the TCM/PCM highways. Each subscriber line channel consists of a SLIC and a variation of the codec-filter called a subscriber line audio processing circuit, or SLAC. Like the National arrangement, this setup requires a microprocessor for each of the eight subscriber lines (Fig. 6).

Digital signal processing boosts both stability and programmability

The setup, devised by Advanced Micro Devices Inc. (Sunnyvale, Calif.), relies on the microprocessor to control and program the chips over a four-line serial I/O bus. However, much of the initial control measures, including time-slot assignments, are handled by the audio processing chip, which also sends control messages to its associated SLIC over a four-line parallel bus. Two additional lines connect the latter circuit directly to the processor.

The internal architecture of the SLAC chip is extremely unusual (Fig. 7). With the exception of the anti-aliasing filter on its input and an integral a-d converter, the chip is digital all the way. Moreover, its use of digital signal-processing techniques ultimately yields a codec that is far more programmable and stable than earlier versions. In this and other circuits, the use of digital signal processing for what have until now been analog functions gives rise to a breed of circuits that are almost completely independent of the real world. For instance, they can remain completely unaffected by temperature and time.

The a-d converter is particularly interesting. Rather than working in an 8-bit compression mode at 64 kbits/s, it actually works as a 16-bit linear circuit running at a sampling rate of 512 kHz. Not a conventional successive-approximation part, it is a modified delta-sigma converter that adds its input to the output of a d-a converter driven by the encoded digital word. The oversampled word is then fed to the digital signal processor, which decimates it (that is, reduces it to 64 kHz) and then digitally filters it.

The program for the filters resides in RAM, thus their bandwidths can be programmed by the user, as can their gain (up to 12 dB in 0.1-dB steps). Their output is digitally compressed for compliance to μ law; if that option is not chosen, the a-d converter operates as a 16-bit linear component. The output of the digital signal processor is then routed into a register for assignment of time slots and ports.

The manner in which the AMD analog line card processes the signal it receives from the PCM highway is as unconventional as its digital signal-processing approach and its delta-sigma converter. If companded, the serial word is digitally expanded and filtered. Then the programmed gain is applied, and the word is fed to an interpolator, which restores the 512-kHz sampling rate, thus obviating the necessity for a low-pass output (reconstruction) filter.

The BORSCHT functions are the toughest to integrate

Of all the functions handled on an analog line card, the BORSCHT functions, as the industry calls them, are the most difficult to integrate. Though "BORSCHT" might seem somewhat frivolous, the meanings are not: B, battery feed; 0, overvoltage protection; R, ringing; S, supervision; C, coding; H, hybrid; T, testing (see "Inside the Phone Service," p. 210). Com-

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monly, SLIC circuits are charged with handling those functions, and some are doing so on two chips or even one chip.

Although SLICs, which connect the codecs to the real world (that is, the subscriber's lines), will change radically when data conversion moves into the handset, they are not about to give up their analog capabilities.

Consider the expectations of a SLIC that is responsible for BORSCHT functions: It must be able to handle analog voltages ranging from several millivolts to over a hundred volts and dc power of 50 V at 100 mA or higher. Moreover, they must work at those voltages with 12-bit precision at 3000 Hz, even when zapped by lightning-induced transients, connected to power lines, or faced with changing impedance in the lines. As a result, SLICs now appearing differ widely in their internal structure and in the way they connect to the codec, to the ring, and to the control lines on the board.

The great SLIC debate: To use transformers or not to use transformers

Some of the upcoming SLICs will connect directly to the line, whereas others will use transformers for isolation. Some use two chips, one built with a high-voltage process and the other with a standard one. Most are characterized as CMOS, bipolar, or dielectrically isolated. Others demand many external active and passive parts, a few need virtually none, and several get assistance from codecs. In one instance, a two-chip SLIC resides in one package, in another they occupy separate DIPs.

The primary dichotomy in SLIC architecture involves whether a transformer will separate the line from the silicon chip or whether the chip will tie directly into the line. Some say that a transformer is mandatory for the environment of a phone company's central office. Moreover, it can tackle almost perfectly the BORSCHT hybrid function—that is, the separation of the two-wire subscriber loop line into two pairs of wires, one each for receiving and transmitting.

Others contend that with a good high-voltage process (bipolar or MOS) and the requisite off-chip overvoltage protection, silicon can ride on the line. Certainly, if dielectric isolation is used, a chip becomes viable, though perhaps not yet economically feasible. Already Harris Corp.'s Semiconductor Analog Products Division (Melbourne, Fla.) has developed a dielectrically isolated SLIC for central office applications. Of the two chips within the low-cost hybrid package, the one on the high-voltage line side is fabricated with a dielectrically isolated bipolar process, the low-voltage mate with junction isolation. The low-voltage chip tackles the hybrid and other BORSCHT functions.

Because Harris's hybrid can handle high voltage, it can perform functions that other SLICs cannot—for instance, creating the 70-V rms ringing voltage at 20 Hz on chip and generating off- and on-hook test signals of 2 V rms at 12 to 16 kHz. The space saved by eliminating the ringing and testing relays and the isolation transformers enables Harris to double the number of lines handled by a line card.

Dielectric isolation gives the SLIC high-voltage protection specifications of ±1000 V peak, longitudinally, when used with external shunt-protection breakdown devices. In addition, the line inputs can take 11 cycles of 60 Hz at 700 V rms.

Another two-chip SLIC does the central office job without dielectric isolation. Instead, its high-voltage chip benefits from an ion-implantation bipolar process that builds transistors with a BV_{CEO} of 140 V and a BV_{EBO} of 250 V. Moreover, the technique, developed by SGS Semiconductor Corp. (Phoenix, Ariz.), can create vertical pnp transistors, which are far superior in

current handling and bandwidth to lateral devices. The low-voltage partner chip in the package, also bipolar, uses I^2L and can handle serial I/O control signals from a line card controller at 2 Mbits/s. The entire SLIC, housed in a multipin power package, works with power peaks of up to 7 W. It can withstand the power generated during ringing, a function that, like the Harris device, it handles on chip.

Though special processes and two chips seem to be the trend for forthcoming SLICs, Texas Instruments Inc. (Dallas) is instead opting for transformers. The components prevent saturation of the core by the dc line current that passes through it, but their size does not save much space on the line card.

An alternative approach, being tried by Fairchild Linear Products (Mountain View, Calif.), uses small, flat, audio transformers with an extra winding. A SLIC-controlled current flows through that winding, which bucks the magnetic field set up by the line current. The winding may have several more turns than the output versions, meaning that the controlled current need be only a few milliamperes.

Though the industry is definitely gearing up for the ISDN—witness the dedicated line card controllers, codecs, SLICs—full implementations await transceivers and multiplexers that handle the S and U interfaces; terminal adapters that convert standard digital signals into ISDN-compatible bit streams; and the true digital handset chip. Fortunately, all of those complementary chips are now in development in the U.S., Canada, and Europe, most being prepared for introduction over the next three years.

An upcoming two-chip set, for instance, is designed for the S interface. Designed by Advanced Micro Devices, the digital subscriber controller chip connects to a handset or data-rate adapter, the digital exchange controller chip ties into a dual PCM highway (Fig. 8). The latter takes on SLIC and codec functions and also converts data flow into the format for ISDN's two B channels and one D channel (ELECTRONIC DESIGN, Dec. 13, 1984, p. 157).

Two power controller chips transmit power from the PBX line card to the terminal over a four-wire line. All of the chips fit well in a mixed analog-digital system, since the output of the exchange controller is compatible with that of the proprietary SLAC.

Intel takes another approach, pairing up a versatile new chip with existing ones to create an S interface. Here, too, the new chip is called a digital exchange controller. It has three interfaces: a four-wire S link, the three-wire TCM slave data line, and a microprocessor hookup. In a typical system, it connects the codec at one end of the S line to a line card controller at the other end. When the chip works in the slave data mode, the slave bus carries the information that normally flows over the B channels and the microprocessor interface deals with the D-channel information.

Implementing ISDN awaits development of S and U interfaces

Chips for either end of the U bus are arriving more slowly, considering the pace at which its difficult tasks are being specified. However, one or more U interface transceivers may emerge by the end of the year, all working with the B and D channels, plus the overhead bits, at 162 kbits/s over a two-wire line. Their methods for echo cancellation ensure that data will be received without accidental cancellation, even if the transmitted and received signals are identical.

In all likelihood, the forthcoming transceivers all will operate as masters and slaves and will interface directly or indirectly with the four-wire S line, dual PCM highways, and microprocessors. □

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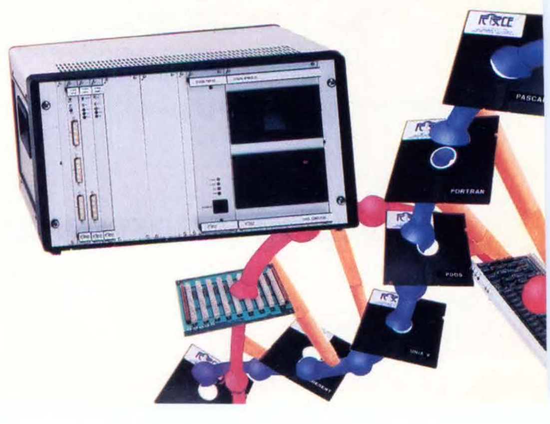

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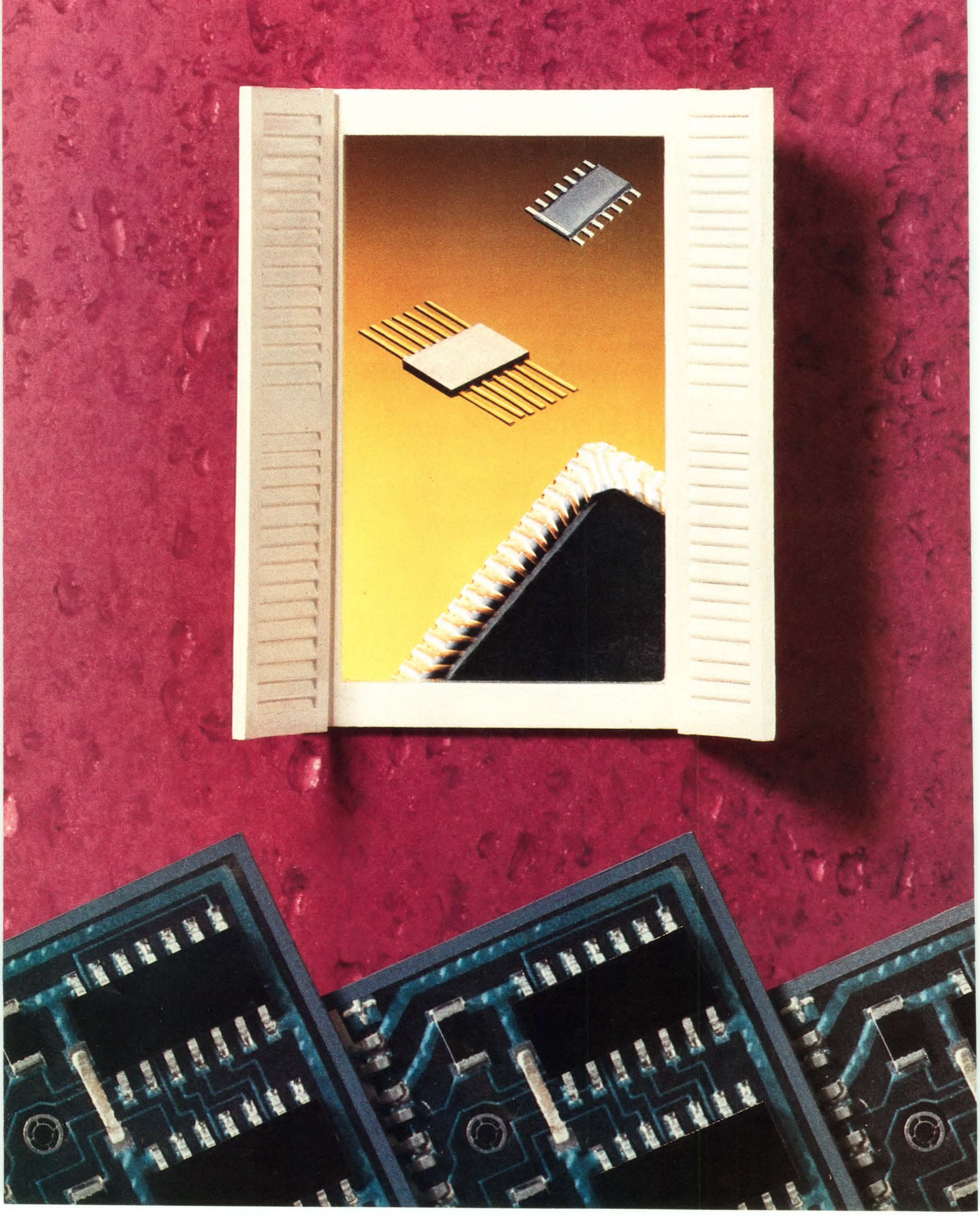


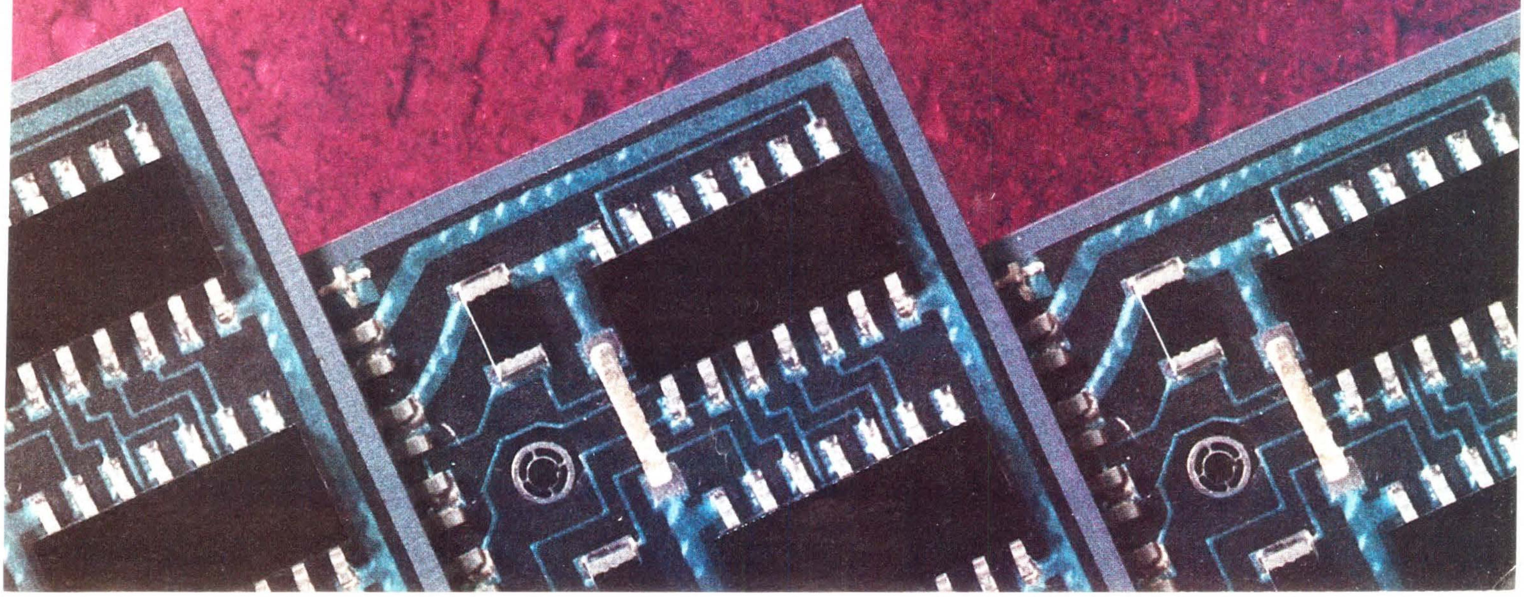
SURFACE-MOUNTED PACKAGING

By 1990 about half of all components sold will be designed for surface mounting. Behind that prediction stands feverish activity in components, packaging, and new manufacturing techniques, all guaranteeing a bright future for surface mounting.

In passive components, the main troublespots — the soldering and mounting of variable components and connectors — are finally yielding to new techniques, even though much remains to be done here. In semiconductors, new packages and materials are rising to meet the challenges posed by sharp increases in pins and concentrated heat. But the new packaging contenders seem to advance in step with new, denser ICs, and standardization is not yet in reach.

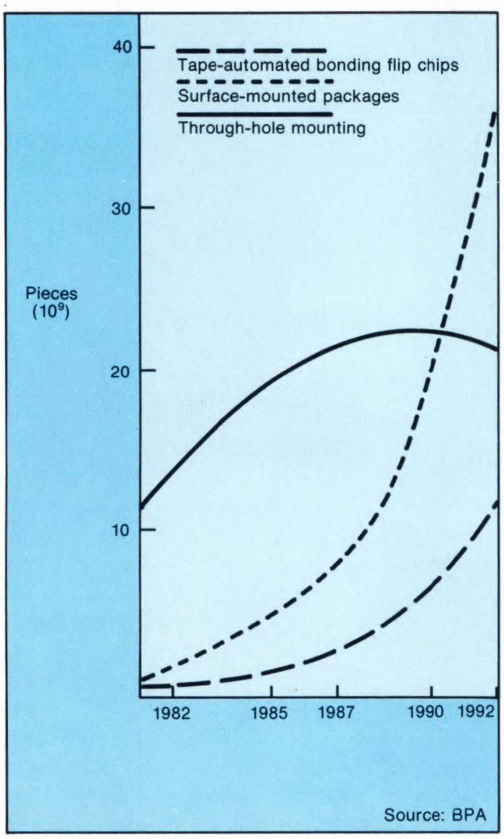
In printed circuit boards, new materials and improved clad designs plan to attack the mechanical and thermal problems associated with surface-mounted packaging. No

MITCH BEEDIE



consensus has been reached, however, and there is room for greater improvement. On top of all that, a variety of novel manufacturing and testing techniques must still be perfected. But developments suggest that surface mounting will fulfill its promise.

The benefits of surface mounting need no laboring: faster assembly; lower equipment cost, volume, and weight; improvements in reliability, vibration performance, frequency response; and immunity to electromagnetic interference. But there is another reason for manufacturers to gain experience in surface mounting: In a few years, they may have no choice.



1. Surface-mounting technology is indeed on the rise, but that does not tell the whole story. The circuits inside the packages will also use the latest semiconductor technologies. DIPs, however, will tend to stay with the older technologies.

Much of the high-volume growth will be in areas like personal computers and consumer and communication equipment, where the cost savings and performance advantages of surface mounting will be crucial. As the large manufacturers change to surface mounting, these components—which now generally cost slightly more than others—will fall below today's price for conventional components. Or, to put it another way, conventional components will be available—but at a premium.

There is, in fact, a good chance that DIP ICs will begin to fade from the industry over the next ten years (Fig. 1). By then the latest semiconductor technologies will be made only for surface mounting. Indeed, some special-purpose, high-performance ICs are already available only in chip carrier form. A manufacturer who resists the change to surface mounting too long will eventually find his equipment riding on yesterday's technologies.

Surface mounting requires a new way of thinking

Despite all that, many manufacturers are not anxious to swing over to surface mounting. For them it means a high capital outlay for production machinery, an unfamiliar design and manufacturing philosophy for the entire factor ·, and a host of mistakes during the learning phase. A major aim must therefore be to make the transition period as painless as possible.

By installing a flexible preproduction line now, a manufacturer can gain experience with the various surface-mounting techniques. After a year or two, he can start to convert production lines one by one; by then, high-volume production equipment should drop in price.

Perhaps the only point of agreement

among the different experts in surface mounting is that the changeover cannot be approached as an extension or straight replacement for conventional assembly. The design and manufacturing processes are fundamentally different. The soldered joint of a surface-mounted device, for example, serves as both the mechanical and the electrical connection. Also, placement is relative, whereas insertion is absolute—the leads either fit or they do not fit.

One basic shift that surface mounting demands is that the designer work much more closely with the production and test engineers. Testing is at best notoriously hard with surface mounting. The position of test pads must be selected carefully; otherwise in-circuit testing is impossible (see "Testing: The Achilles' Heel of Surface Mounting?," below). The real challenge for design engineers is to accept the variety of surface-mounting disciplines. To help them, forward-looking suppliers, like Philips and Texas Instruments, have been conducting workshops in surface mounting for some time.

With nearly a full range of small resistors, capacitors, diodes, transistors, and ICs now available in surface-mounted form, interest lies primarily in the passive components—such as connectors and variable parts that so far have lagged behind. Normally the major problem in converting a component to surface mounting has little to do with the method of mounting; rather it is in designing the component to withstand immersion in molten solder (see "Soldering Heats Up," p. 236). This has led to some ingenious solutions, such as capacitor trimmers from Panasonic

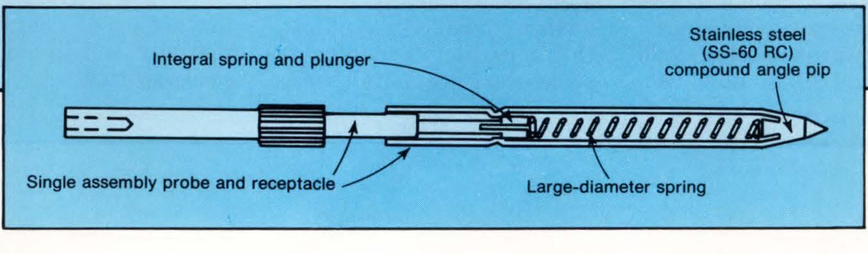
Testing: The Achilles' heel of surface mounting

When it comes to testing surface-mounted boards, there is no substitute for providing test pads at the critical nodes during system design. If that is not done, then it may well be impossible to test and diagnose faults in a circuit. Surface-mounted boards are inherently hard to test: Their internal nodes are often impossible to reach, first because they are covered by components, second because the nodes on one side of the board do not necessarily feed through to the other side.

Although some test probes are thin enough to probe surface mounted assemblies without buckling (see the figure), probing is still difficult. Probing the component directly could damage it, and a probe pushing down on the component's joint may make an open-circuit component appear good. Chip carriers are especially hard to probe, since they present a very small area from the top. Despite all of these problems, fixtures are being introduced for surface-mounted boards.

An example is the new MicroMate in-circuit test fixture from GenRad Inc. (Concord, Mass.). It attaches to any of the company's test systems. A CAD program giving pc board details and desired test points is fed into the test system, which then calculates the best positions for the probes to minimize test paths and reduce stresses in the board being tested. The output of the program is then fed to a drilling and wiring machine to produce a fixture, which can access both sides of the board simultaneously for in-circuit and functional testing.

Even with fixtures like this, however, designers must still allocate some of the space gained from surface mounting to make the circuit more testable. They can do this by including test pads for the critical circuit nodes, as well as through such techniques as self-testing.



Soldering heats up

Virtually all high-volume users of surface mounting still rely on inserted components and thus on some form of soldering: reflow, wave, or both. Most research today focuses on reflow, basically because it is inherently more suitable for surface mounting. For example, it does not suffer from such wave-soldering problems as shadowing, which occurs behind chip carriers and other large components or when one component is placed too close to another.

The benefits of vapor phase, just one reflow soldering technique, are spurring the makers of reflow equipment to develop machines capable of soldering both surface-mounted and through-hole components. That approach would eliminate not only the bridging problems associated with wave soldering but also the need for gluing the surface-mounted parts to the pc board (a must for wave soldering).

Though vapor phase is now the most popular form of reflow soldering, it is under threat from other reflow methods. For one, laser soldering is particularly suitable for high-density boards or when heat-sensitive components must be soldered, since the heat is concentrated onto the soldered joint. The technique is, however, generally favored for specialized applications, and the most serious threats to vapor phase come from infrared and microwave techniques.

Microwave soldering equipment has until now been largely unsuccessful, because the intense heat tends to damage components. However, in recent microwave-enhanced system from Teledyne Semiconductor Inc. (Woburn, Mass.), the microwaves heat an intermediate microwave-absorbent susceptor, thus providing 85% of the heat conductively; only 15% is supplied in the joints by direct microwave action. With most heat supplied in that manner, the process is insensitive to the nature of the substrate and does not overheat the components being soldered.

Infrared soldering also was largely out of favor, as the substrate's surface reflectivity tended to determine how much heat was absorbed; black plastic often reached a higher temperature than the solder itself. This has now been solved by systems that shun lamp-type emitters and focusing reflectors. Instead they favor panels using the secondary-emission principle to diffuse infrared energy across the process area. The energy is not color-selective, and most components are actually 20° to 40°C cooler than the board at reflow.

In most applications, however, microwave and infrared soldering will be hard pressed to oust vapor phase, which nevertheless has its own drawbacks: It needs expensive chemicals (although running costs are generally low), and its equipment is physically larger, with a lower throughput, than microwave and infrared solderers. Once more experience is gained with microwave and infrared soldering (the methods do not at the moment allow double-sided soldering in one pass, although ways to do this are under study), they will be serious rivals to vapor-phase systems.

Inspecting solder joints can be a real problem for surface-mounted assemblies; they are more densely packed than conventional components, and in addition the most critical part of the joint is obscured by the component. Much current testing is done visually—for example, with a microscope, video camera, and screen. Although these methods are being automated through some form of pattern recognition, they cannot spot defects obscured by components or hidden in the solder joint itself. Those defects call for the newer X-ray and laser systems.

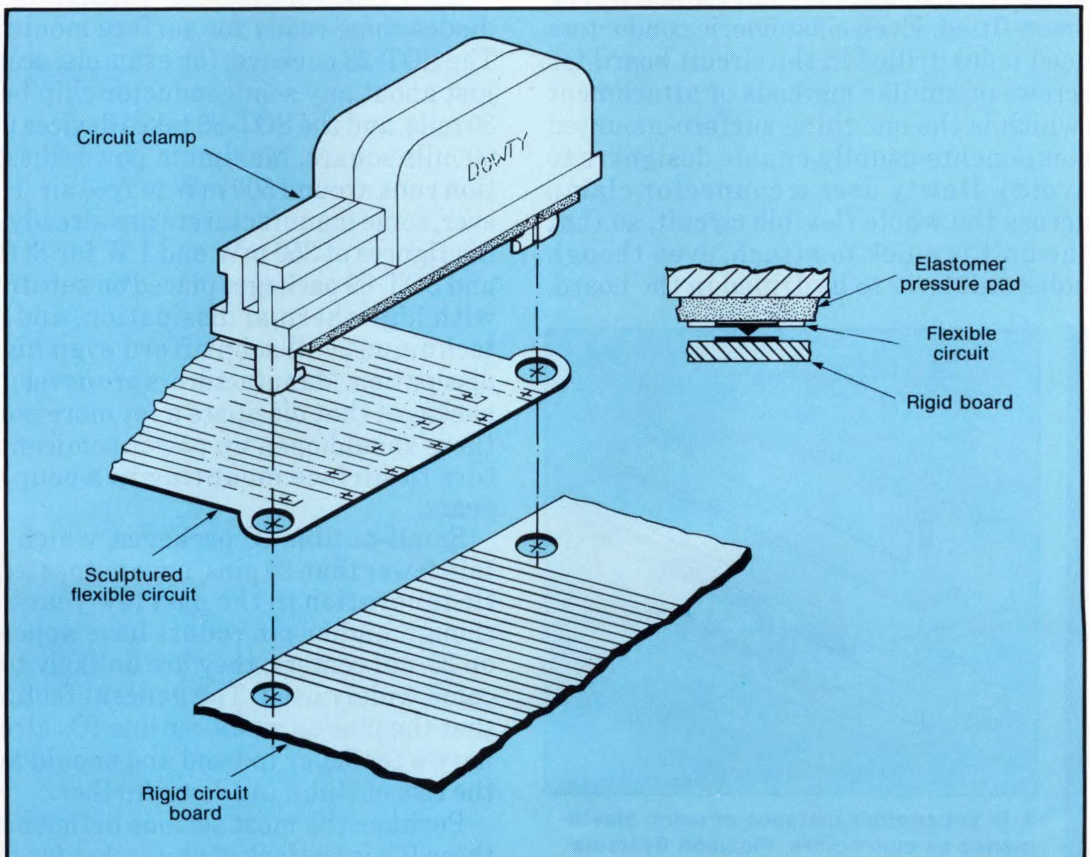
Defects in a component joint, for example, can be found by a setup from Vanzetti Systems (Stoughton, Mass.). The system combines a pulsed laser, an infrared detector, and a computer. Solder joints are heated individually. The infrared detector senses the thermal radiation from the joint, while the computer compares the joint's heat pattern with the stored patterns from good solder joints, which are grouped in a well-defined area. The radiation characteristics of joints having pinholes, cracks, or voids are different from those of a good joint; thus potentially bad joints can be easily spotted.

(Osaka, Japan) that are covered by a membrane or foil. The barrier protects the components from the solder. During the trimming operation, the user breaks the membrane to make the adjustments.

Surface-mounted edge connectors have also trailed, mostly because of slow demand, but two types have been introduced in the past few months. One is virtually identical to standard DIN connectors. For instance, 64- and 96-contact edge-connector models offered as samples by ITT Cannon (Weinstadt, West Germany) fully meet the DIN41612 specification for two-part pc board connectors—apart, of course, from the contacts themselves, which are bent for surface mounting.

The other edge-connector type is more exotic, using elastomers. One example, a ribbon connector from Dowty Electronic Interconnect (High Wycombe, Bucks., England), has a flexible connecting strip in which the conductors are raised at the interconnection points to form pressure peaks upon contacts (Fig. 2).

The flexible circuit on these connectors has two conductors for every millimeter, and the circuit aligns with a set of tracks on the printed circuit board. The contacts are made from a tin-lead alloy (another example of the shift away from precious metal terminations); it works here because of the 150-gram pressure applied on each connecting point. Plastic flow in

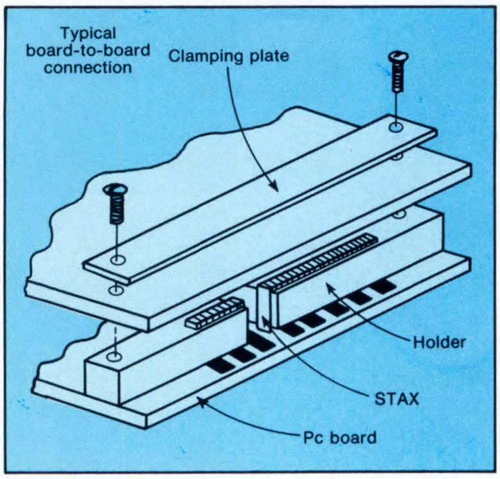


2. One of the first surface-mounted edge connectors, developed by Dowty Electronic Interconnect, shuns current approaches and instead uses elastomeric pressure pads to make contact between the board and the flexible circuit.

the tin-lead alloy produces a virtually gas-tight, vibration-resistant joint.

Elastomers can also simplify board-to-board connections. One component, developed by Flexicon Systems Ltd. (Biggleswade, England), is simply clamped between the two boards (Fig. 3). A very attractive feature, the alternate conductive and nonconductive stripes in the elastomer can give up to 250 connections per inch; these strips run parallel to the contacts on the pc boards, and the high redundancy makes the elastomer self-aligning.

With any type of surface-mounted connector how to attach it to the pc board becomes a major concern. The present DIN connector from ITT Bauelemente is attached with rivets; the final version will be press-fitted. Even elastomeric conductors need holes drilled in the circuit board for screws or similar methods of attachment (which is the one thing surface-mounted components usually enable designers to avoid). Dowty uses a connector clamp across the whole flexible circuit, so that the unit is quick to attach, even though holes still have to be drilled in the board.



3. In yet another instance of using elastomerics as connectors, Flexicon Systems' alternate conductive and nonconductive strips squeeze up to 250 connections into an inch. Once the bolts are inserted, the connectors are self-aligning.

However, manufacturers are looking at methods that will attach the connector without the need to drill holes, such as ultrasonic welding or adhesives. Much of the problem seems to rest with marked resistance to eliminating nuts and bolts, rather than any severe technical difficulty. One problem, however, is in developing a single adhesive that will hold the several different kinds of plastics used in ICs and connectors.

Semiconductors solve the problem of attaching to printed-circuit boards

Most types of discrete transistors and diodes come ready for surface mounting. The SOT-23 package, for example, accepts just about any semiconductor chip below 30 mils, and the SOT-89 takes devices up to 60 mils square. Maximum power dissipation runs around 500 mW in free air. However, some manufacturers are already giving figures of 350 mW and 1 W for SOT-23 and SOT-89 packages placed on substrates with high thermal dissipation, and new techniques will soon afford even higher dissipation. Manufacturers are developing packages that dissipate a lot more power; these should open up power semiconductors to surface mounting in a couple of years.

Small-outline IC packages, which contain fewer than 28 pins, have witnessed little innovation in the past few years. Although higher pin counts have appeared on 25-mil centers, they are unlikely to become widely used. The general feeling is that the pins on small-outline ICs already have a tendency to bend and should avoid the risk of slimming down further.

Perhaps the most serious deficiency in these ICs is the lack of any socket for these packages: The ICs must be soldered into place to conduct reliability testing. More seriously, it makes impossible for manufacturers to supply burned-in small-outline ICs.

With J leads less prone to damage than gull-wing because of their smaller footprint, it was only a matter of time before someone came up with a J-lead IC. A 20-lead package has been proposed by Texas Instruments Inc. (Dallas) for its 1-Mbit dynamic RAM. It will be interesting to see if more J-lead versions are introduced, and if they are, how they stack up against the established gull-wing small-outline packages.

As in VLSI design, heat removal is limiting the density of surface mounting. The solution leans toward lead frames with high copper content, integral heat sinks, and improved thermal conductivity for the package—all steps to improve heat dissipation. Most work on plastic-encapsulated ICs is concentrating on plastic leaded chip carriers (PLCCs) and quad flat packs.

Keeping cool is one of the major problems in surface mounting

Plastic carriers generally have a heat dissipation about 80% that of a comparable DIP, with half the heat passing through the leads and the rest radiating from the case. The thermal resistance between junction and ambient (T_{J-A}) ranges from above 100°C/W for a 20-lead carrier to about 40°C/W for a 68-lead package. One interesting innovation is an 84-pin package from Texas Instruments, a development model that has a built-in heat sink. Fins on the sink increase the heat-dissipating surface by 25% and cause turbulence in the passing air—improving the package's thermal performance by 50%. The T_{J-A} for this PLCC is a very low 5 to 15°C/W, depending on the air-flow rate.

Although much research is going on in heat dissipation, many designers feel the problem is better avoided than solved. This is illustrated by TI's experience with its finned package: The bipolar IC for which the package was designed was ultimately converted to CMOS, thus allowing a standard package to be used.

The other major concern at the moment is how to increase lead counts. In the long run, the counts will come down as integration on the ICs themselves rises. But until then, pin counts are expected to climb. Packages with high counts will likely use staggered leads or reduce the pin spacings to 40 or 25 mils. Several package proposals with pin spacings of 40 or 25 mils have, in fact, appeared in the past year, but before they can be used widely, significant improvements will be needed in pc board technology.

The pad-grid array (a surface-mounted pin-grid array) is also a contender in raising lead counts, but it suffers from a defect: Its solder joints cannot be inspected by conventional means. After an initial burst of activity on pad-grid arrays, interest appears to have fallen recently.

The lead count is inherently limited in plastic chip carriers, since larger packages can suffer reliability problems caused by thermal mismatches between the lead frame and plastic; PLCCs thus generally go up to only 84 leads, though a few go higher. One solution, a PLCC proposed by Texas Instruments, has two rows of staggered leads, allowing it to go up to 164 leads with lead spacing of 50 mils.

Other materials are also being used to encapsulate ICs. The Epic chip carrier, for example, developed by British Telecom (Ipswich, England) and Tectonic (Wokingham, England), uses neither ceramic nor premolded plastic for the casing (Fig. 4). Instead the package is made from conventional, low-cost pc board laminates, initially epoxy glass. It consists of a base containing a cavity for the chip, which is wire-bonded to the contacts. The junction coating is applied directly to the chip surface to improve reliability, and the chip is covered by a lid for mechanical protection.

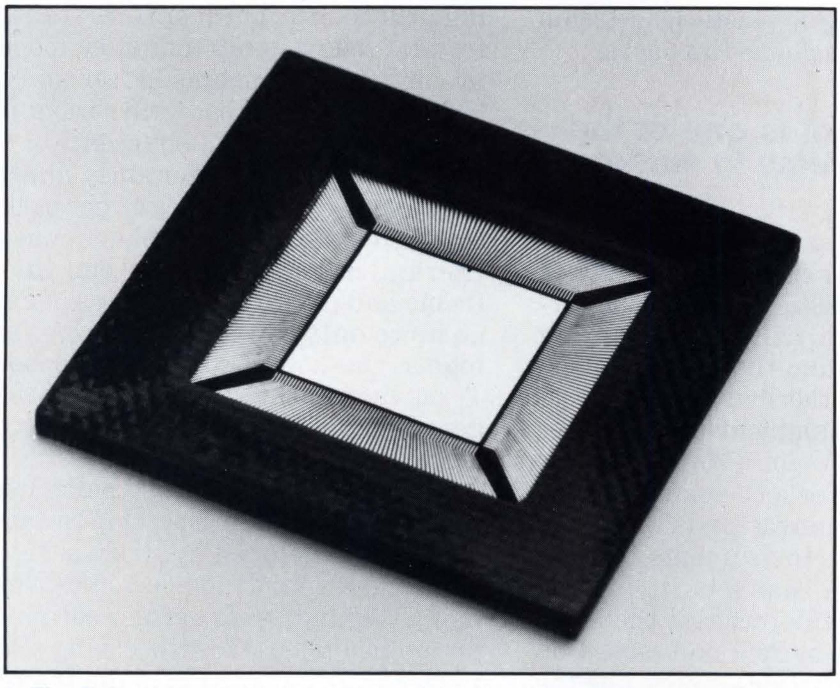
The Epic package is highly resistant to alpha radiation: Organic encapsulation has been found to reduce soft errors in static RAMs by at least two orders of magnitude below comparable ceramic packages. This package also solves the problem of mismatched thermal expansion between the ceramic chip carrier and the pc board. Since the chip carrier is made of the same material as the pc board, it produces no thermal stresses on the solder joints during temperature cycling.

With recent improvements in transfer-molding polymers and better IC passivation, the humidity problems of plastic-encapsulated ICs are declining. This will allow these and packages like Epic to fulfill the 20-year lifetime requirements for telecommunications components.

When an IC must dissipate a large amount of heat, the poor thermal conductivity of plastic—about 0.35 W/mK (watts per meter-Kelvin)—offers little alternative but to turn to ceramic packages. Work on leadless ceramic carriers (LCCCs) currently focuses, as it does for plastic carriers, on increasing the I/O count and improving heat dissipation.

Lots of heat means going with ceramic chip carriers

As one example, Texas Instruments has proposed a 132- and a 164-pad ceramic package that match the footprint of the



4. The Epic chip carrier from Tectonic and British Telecom breaks away from the traditional use of plastic and ceramic for IC packages. It comes in a range of sizes: 84 pads on 50-mil centers, 132 pads on 25-mil centers, and here a 20-mil package with 256 pads.

company's staggered-lead PLCC package. The inner row of pads has fine holes reaching up to the top of the package for inspection of the solder joint; the solder is absorbed up the hole, and the joint can therefore be inspected from the top.

For LCCC, the thermal resistance between junction and case (T_{J-C}) is of interest, because the surface on which the package is mounted profoundly affects the resistance. LCCs have an average T_{J-C} of about 10 to 25°C/W, depending on the number of pads and the die size.

At present alumina (Al_2O_3) is generally favored for leadless ceramic packages. Although its thermal conductivity is much higher than that of plastic, it is still relatively low (between 10 and 35 W/mK), and its temperature coefficient of expansion (T_{CE}) is more than twice that of silicon. Because of the unequal expansion, the crystal is generally glued to the chip carrier to take up the stress, thus reducing the thermal conductivity even further. Beryllia (BeO) has about 10 times the thermal conductivity of alumina and is beginning to find use in high-dissipation packages. But its coefficient of expansion is even higher than that of alumina; in addition, the matching process for beryllia must incorporate elaborate precautions to remove the extremely toxic BeO dust that is produced.

Alternative ceramics have been developed. Aluminum nitride, made by W.C. Heraeus (Hanover, West Germany), and silicon carbide, produced by Hitachi Ltd. (Tokyo), both have a thermal conductivity

The ins and outs of thermal mismatch

Mention problems with surface mounting, and specialists in the field will generate almost as much heat in debating solutions as do some of the critical components. This is particularly true for the topic of mismatch in thermal coefficients of expansion, T_{CE}.

The problem is well known: Ceramic chip carriers have a T_{CE} of between 6 and 7 ppm/°C. The result is stress and failures in soldered joints after as few as 100 cycles between −55° and +125°C, the temperatures specified in MIL-STD-883B.

However, questions have recently been raised about the general use of MIL-STD-883B for testing. It may be fine for evaluating the reliability of boards stored under extreme temperatures, but it bears little relevance to operating temperature gradients, where the heat is localized around the devices.

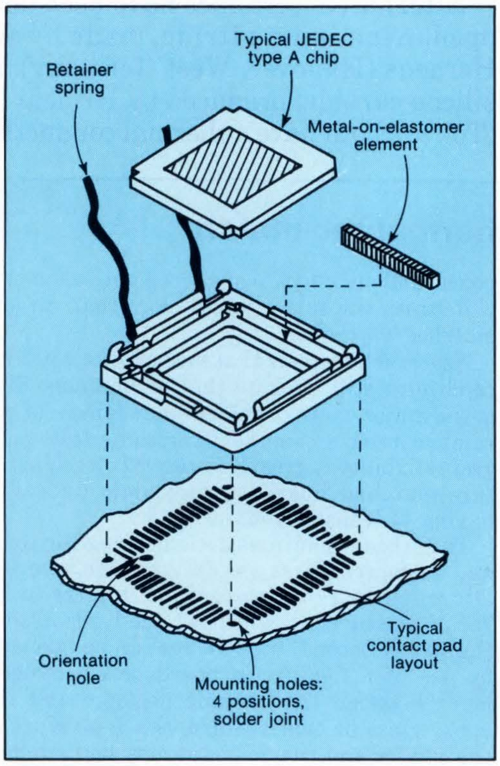
On top of this, although the temperature coefficient of the pc board is more than twice that of the ceramic carrier, the device temperature will generally be several degrees above that of the board —which, again, produces less stress than seems apparent at first. Indeed, at start-up, the carrier is much hotter than the pc board, and matched T_{CE} between both elements will strain the solder joints more than an unmatched T_{CE} would.

Nevertheless, tests that incorporate start-up conditions still indicate that mismatched T_{CE} is the major cause of solder-joint failure of ceramic carrier assemblies. The same tests suggest reliability is greatly improved on temperature-matched boards for ceramic packages having 44 leads and more.

Three basic solutions are emerging for thermal mismatch. First, the designer can ignore it altogether by rejecting ceramic carriers in favor of plastic ones, which let the leads absorb the stress. Second, the stresses can be taken up by use of a flexible pc board or elastomeric layer between the ceramic package and the epoxy-glass pc board. Third, the T_{CE} values of the carrier and the pc board may be matched.

The designer who opts for the third solution can use epoxy-glass carriers mounted on standard epoxy-glass boards (as is done with the Epic chip carrier developed by Tectonic and British Telecom), or he can match the T_{CE} of the pc board to that of the carrier by using, say, a ceramic or copper-clad invar board.

comparable to that of beryllia (BeO) and about eight times higher than that of alumina. Both also have a coefficient of thermal expansion that is almost identical to that of silicon. Of course, the perfect thermal match bewtween silicon and chip carrier only exacerbates the thermal mismatch between the chip carrier and the epoxy-glass pc board (see "The Ins and Outs of Thermal Mismatch," p. 241), since silicon carbide and aluminum nitride have a temperature coefficient about five times greater than that of epoxy boards. However, with silicon having a T_{CE} of about



5. Elastomers have made possible one of the first sockets for surface-mounted leadless chip carriers. Flexicon Systems uses four elastomeric elements to connect the leads of the carrier to the board.

2.7 and epoxy pc boards a T_{CE} of approximately 14, a thermal mismatch will exist somewhere, no matter what material is to be used. Material like silicon carbide and aluminum nitride give a thermal match at the crystal, which is where the heat is generated; a chip carrier made of either of the new ceramics, with elastomeric materials taking up the strain between the chip carrier and pc board, looks very promising.

Despite competition, plastic continues to play a major role

Nevertheless, plastic leaded chip carriers continue to compete. The two last obstacles to plastic dominance are lower thermal resistance and a more reliable hermetic seal. Techniques employing heat vias in the package could solve the thermal resistance problem. In fact, the thermal resistance of the Epic carrier went from 100°C/W to a very respectable 4° C/W. As for high-density connections, leadless ceramic carriers cannot match tape-automated bonding (TAB) technique. The LCCC is therefore becoming much more limited in scope although it is likely to remain in use for several years.

As for surface mounting plastic and ceramic carriers, two types of sockets have emerged, with one, of course, using the ubiquitous elastomer. The chip carrier socket recently produced by Flexicon Systems contains four metal-on-elastomer elements that connect the leads of the carrier to the footprint on the pc board (Fig. 5). The assembly is soldered to the pc board with four posts, and a retaining spring maintains the contact between carrier, elastomer, and pc board.

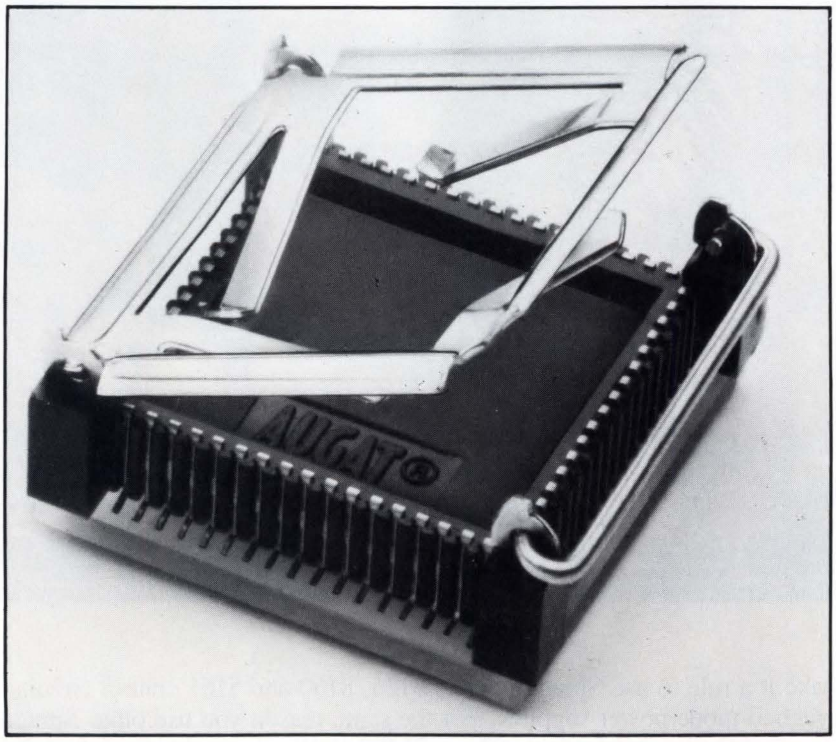
A more conventional surface-mounted leadless chip-carrier socket from Augat Components (Attleboro, Mass.) can socket JEDEC A- and B- type LCCCs. Its open-sided insulator affords good heat dissipa-

tion (Fig. 6) and allows solder joints to be examined. The chip carrier is locked into the socket by a hinged cover with latching bar, which also allows a heat sink to be mounted on the top surface. The socket is soldered to the pc board on pads having 50-mil centers.

These newer sockets, combined with new connectors and other components, are reducing the need for putting surface-mounted and conventional devices on the same board, a mix that dilutes the benefits of pure surface mounting. That leaves the pc board itself as a stumbling block in the path toward universal acceptance of surface mounting.

The past decade has seen relatively few improvements in boards. Among the improvements, line widths and spaces have gradually been shrunk to their present typical values of 0.25 mm with 0.5-mm vias. Even the jump to surface mounting has reduced widths and spaces to only 0.15 mm and via holes to 0.3 mm, sufficient for the 50-mil (1.27-mm) lead pitches of current packages. However, with packages now proposed with pitches of 25 and 12.5 mils, lines and spaces of about 0.075 mm will be needed, along with 1-mm vias. Although these dimensions are possible—Exacta (Selkirk, Scotland) has done it during preproduction of its elastomeric Chipstrate board—boards are fast approaching the stage where manufacturing methods must either be refined or changed altogether.

One solution is to turn to methods like direct laser imaging of the circuit onto the board. Although the makers of epoxy (and polyimide) glass boards will no doubt



6. A more conventional socket for leadless chip carriers, this one from Augat Components, has an open-side insulator for good heat dissipation and for inspection of the solder joints.

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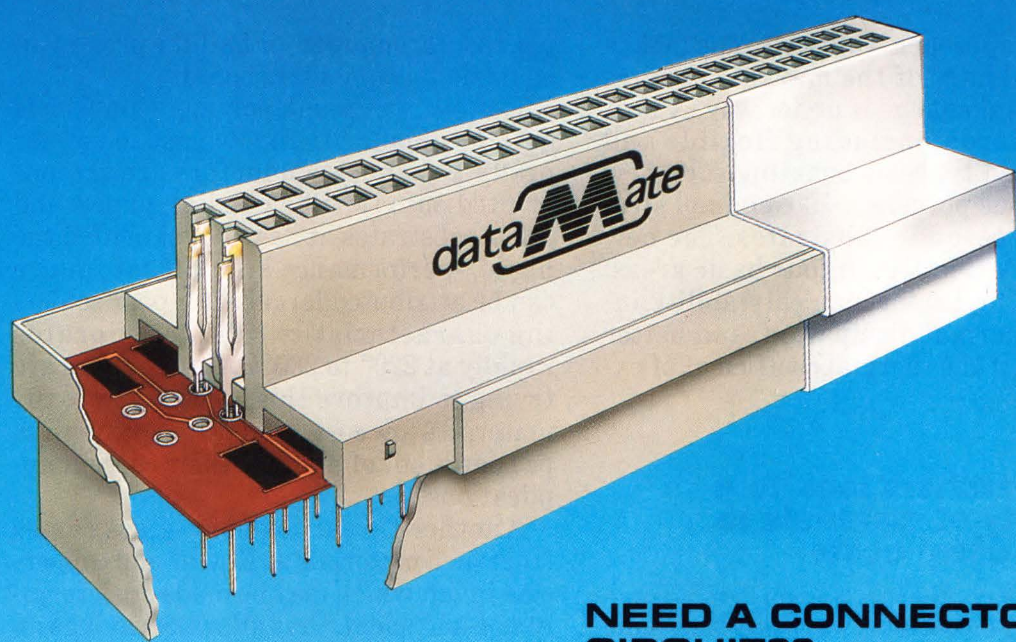

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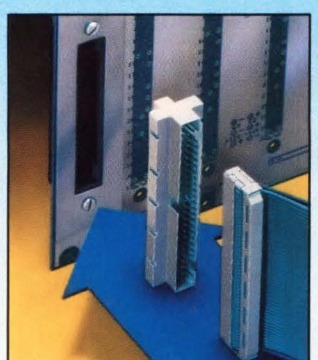

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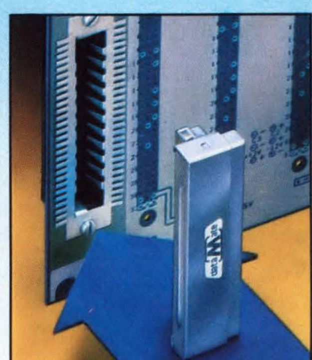

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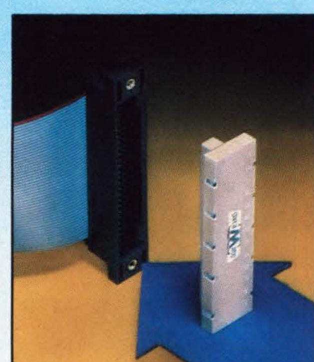

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adopt this approach—and continue to take the lion's share of the market—a more fundamental change is under way. A host of new boards, including flexible and metal-cored types, is boasting such new materials as porcelain-like enamel steel and large ceramic substrates. The new contenders compete in four basic areas: lower cost, higher mechanical stability, increased thermal dissipation, and better matching of the thermal coefficient of expansion (T_{CE}).

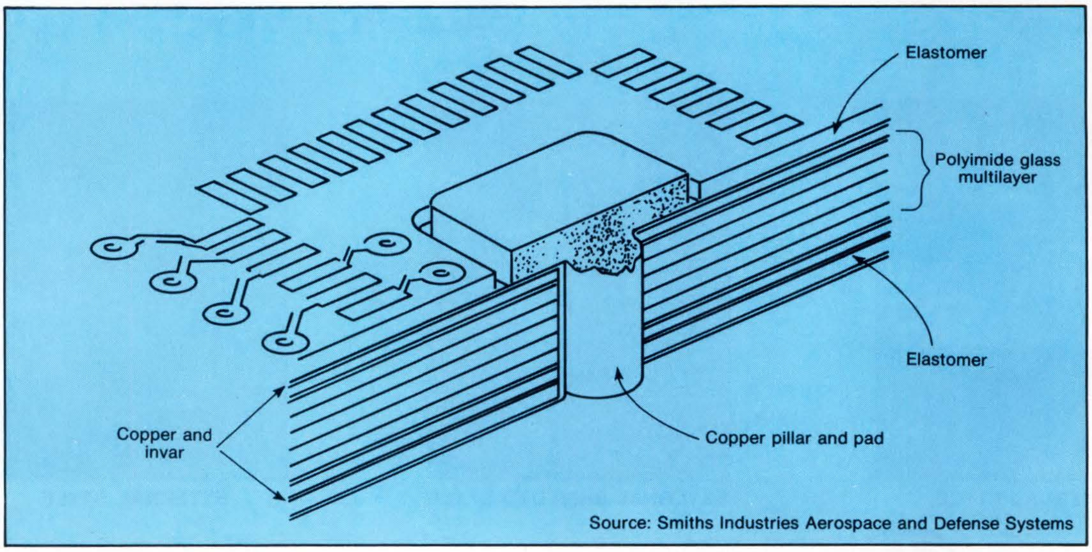
Researchers look to a variety of materials to hold down costs

On the low-cost side, work has been done by British Telecom Research Laboratories (Martlesham, Heath, England) on polymer thick film (PTF). The findings indicate that once the current technical problems—mostly involving soldering—are solved, the simpler processing of the material could slash the costs of multilayer boards; a four-layer PTF board, for example, costs around $20, or half the price of an equivalent epoxy-glass board.

However, although polymer thin film is gaining popularity in low-cost consumer products, where conductors are screen-printed onto flexible plastics, paper, and other substrates, it has not yet dented the higher-performance arena. That failure can be attributed largely to a poor soldering characteristic: PTF deteriorates rapidly at 220° to 230°C. Researchers are trying to improve this; once they do, the material's low cost could force epoxy-glass pc boards out of many of their current applications.

Another threat to epoxy-glass comes from such materials as Kevlar and copper-clad invar, which may be made structurally self-sufficient, thus allowing savings on mounting brackets and other structural members. Copper-clad invar, for example, can be drilled, punched, bent, sheared, and drawn. It may not be too soon before one side of a circuit board holds the components, while the other forms the outer casing.

Although mechanical considerations



7. With power dissipation increasing, substrates reinforced with copper-clad invar supply an effective way of matching temperature expansion coefficients while still drawing away large amounts of heat from the circuit.

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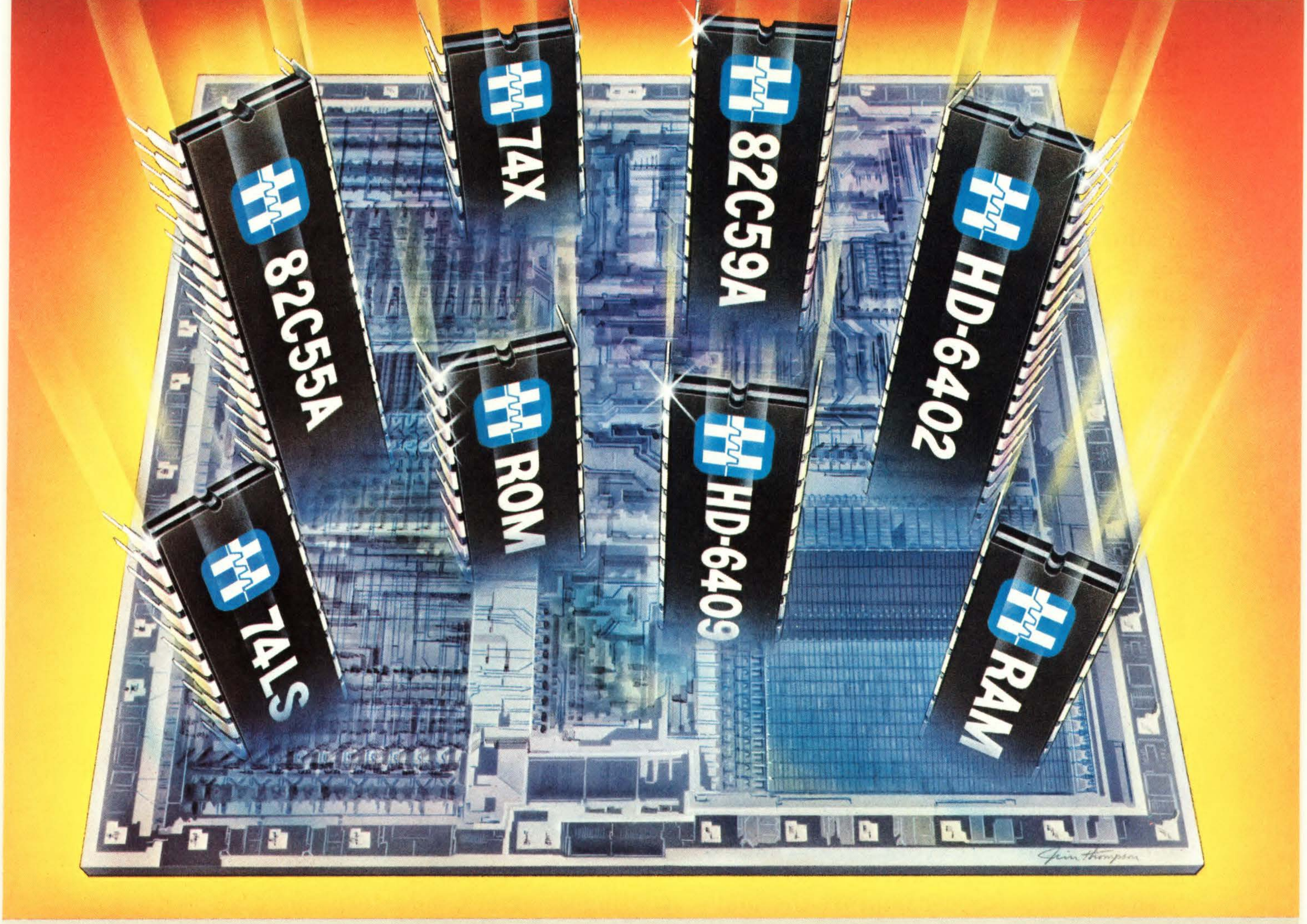

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are important, thermal dissipation is the key to success in surface mounting. With surface area dropping and circuit density rising, heat dissipation for an average board could soon be on the order of 3 to 5 W/in.^{2}. Using a material with good heat conduction properties can increase the reliability of equipment and hold down both the number of components that need heat sinks and the size of fans.

Solutions are sought for the thermal mismatch problems

Thin copper-clad invar cores, which cost no more than equivalent polyimide copper-clad pc boards, can dissipate up to 14 times more heat than identical layouts on conventional pc boards. In addition, copper pillars and vias can lead heat from components to cores (Fig. 7), and edge-mounted heat exchangers can be attached to the board to further improve thermal characteristics.

Thermal mismatch has received considerable attention of late, and perhaps the most researched solution is copper-clad invar, which bonds an invar sheet (65% iron, 35% nickel alloy) between two layers of copper. This core is sandwiched between conventional epoxy-glass or polyimide-glass laminates. Recent work by Ferranti Ltd. (Bracknell, England) and others has shown that the core can be as thin as 0.15 mm, thus making the weight of the whole board only 30% heavier than polyimide glass boards.

The manufacturer of the core can adjust the T_{CE} of the sandwiched board by varying the ratios of copper and invar in the core, which respectively have high and low thermal coefficients of expansion, to match the coefficient of the leadless ceramic carrier. Since the copper-clad core has good conductivity, it can also be used as the ground or power rail. One or two cores can be incorporated, depending on the number of laminates, with the cores close to the surface of the board for short thermal paths.

Alternative ways of getting around the T_{CE} mismatch are to increase the height of the solder joint, use flexible pc boards, or bond a 50-μm-thick compliant elastomeric layer to a conventional epoxy glass laminate. To make contacts, carbon or metallic powders are introduced to form conductive stripes in the nonconductive elastomer material. No one solution is likely to meet all needs, however, and it looks as if each will find its own applications, depending on such factors as circuit density, cost, and heat dissipation.

All of that activity would be useless if high-volume mounting machinery did not keep pace with component advances. Most manufacturers starting with surface mounting will no doubt turn to one of the many software-controlled machines that can mount just about any component, including trimmers, inductors, and high-lead-count leadless chip carriers. Quad packs and PLCCs are also beginning to be placed by the high-volume machines, and another machine for Panasonic, planned for entry this year, will mount quad packs with high lead counts and PLCCs packed in palettes.

Surface mounting calls for new kinds of production machinery

At first, speed is not important: The main object is to gain experience with surface mounting of several different product types. Machines such as the MPS100 from Dyna/Pert Precima (Beverly, Mass.) are extremely flexible and can place almost any type of component housing onto a pc board. With that variety, machine manufacturers are increasingly offering a range of feeders. The MPS100, for one, works

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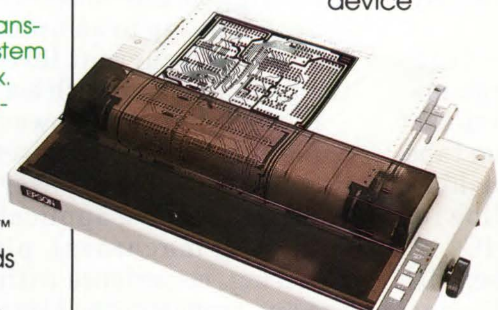

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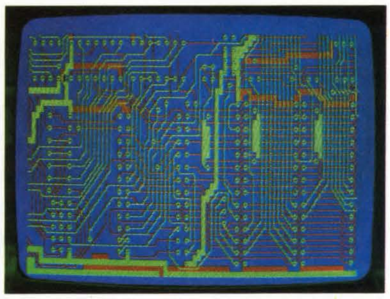

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with 12 feeder types—tape, flat vibrators, stick feeders, waffle trays, and more exotic alternatives.

Another facet of flexibility is the speed with which a machine can be reset to handle a new product line. This is most important in the early stages of surface mounting, when different techniques are being evaluated. The program for each board is held on a microcassette, and a complete set of component feeders can be kept on the machine that whole time. With the relavant feeders in place, resetting the MPS-100 for a new board takes about a minute—the amount of time involved in loading a previously written microcassette.

Various techniques ensure that components are placed correctly

After gaining some preproduction experience in surface mounting, users generally move up to faster machines. But improvements are needed so that these machines can handle different types of components. Manufacturers of high-volume machines are generally reluctant to design customized feeders, a major reason being the need for reliability and standard packaging.

Tape is generally favored for high-volume placement, and many large machines will mount just about anything that can be packed on 8-, 12- and 16-mm tape. In addition, Panasonic has two machines that accept 32-mm tape, thus allowing them to place 28-pin small-outline ICs.

Placement accuracy is on the rise, with imagers increasingly being used for pattern recognition. A solid-state imager on the MCM II, a software-controlled machine from Philips International BV (Eindhoven, the Netherlands), takes the place of the central "pipette" (placement head), scans the substrate and uses pattern recognition to guide the component into its footprint. This eliminates the errors caused by simple placement of the component according to reference points on the substrate.

Another layer of checking is tackled by a measuring device on the placement head of a software-controlled pick-and-place machine from Siemens. The detector catches out-of-specification or incorrectly sorted components. This feature is especially important for components being fed by vibration feeders, since it is relatively easy for an odd component to be dropped into the feeder bowl.

In the long run, one of the most important aspects of a production-scale automatic placement system is going to be the number of defects in assembled boards. Soldering and placement reliability of 99.95% per connection sounds high at first. But consider a complex board with 100 components and perhaps 2000 connections; the machine could be a very fast way of turning out rejects.

In the first stages of a company's experience with surface mounting, the target is generally to keep the same reject rate now obtained with automatic insertion (this often means reworking almost every board). After a year's experience, a common target is 200- to 300-ppm failures per connection—up to an order of magnitude higher than current levels for conventional components with leads.

In the long term, however, major machine manufacturers are setting targets as low as 50 ppm for the overall system, including adhesive application (on wave-soldering machines), placement, and soldering. Experience with machines like the one from Philips already indicates a placement reliability of 10 to 20 ppm, and it will be the job of designers over the next four or five years to bring each stage of the placement process down to that level. This will give a cumulative reliability of 50 to 100 ppm, the point at which zero-defect policies can begin to be implemented. □

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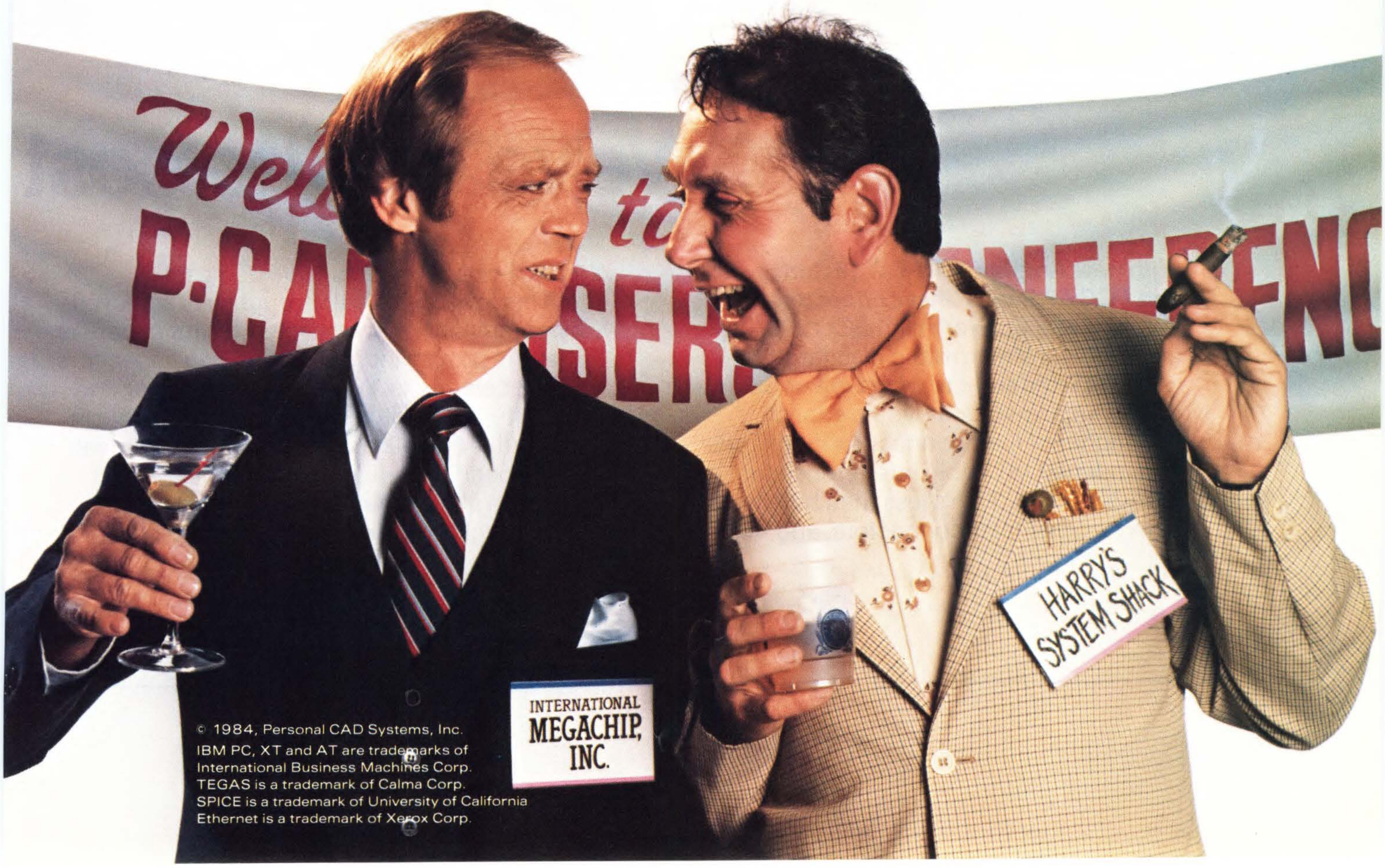

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With new Amphenol® FCC 17 Series and FCC 57 Series filter connectors.
If you have a problem with FCC 20780 compliance, electrostatic discharge or EMI/RFI interference, we have a solution at a price much lower than you'd expect.

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# of EMI/RFI control.

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CIRCLE 108

Win A Princess Caribbean Cruise For Two Plus $1000 Cash

Enter *Electronic Design's* 21st Annual Top 10 Contest

Entry blank and rules appear in this issue.
Win a luxurious Princess Caribbean Cruise for two. This ideal getaway on an elegant liner is the vacation of a lifetime! You'll be treated to extravagant meals, splendid entertainment, exciting nightlife, and plenty of fun in the sun. You'll cruise to the exotic Caribbean islands, experience their rich cultures, lounge on their beautiful beaches. Sample the perfect blend of comfort, elegance, and adventure on this dream cruise.

First prize also includes $1000 in cash to cover incidentals.
It's easy to enter, and fun to win! All you have to do is pick the ten top-scoring ads in the January 10th issue of *Electronic Design.*

Here's How You Enter
1. Official entry forms are in this issue.
2. Read the rules contained in the issue.
3. Pick the ten advertisements you think your fellow readers will best remember having seen.
4. List the ads by Company Name, Reader Service Number and Page Number on the entry card.

MAIL BEFORE MARCH 1, 1985.

Your list of selections will be checked against Reader Recall, *Electronic Design's* method of measuring readership.

PLUS more than 100 other exciting prizes for 2nd through 100th place winners!

Welcome Aboard All You Advertisers, Too.
A parallel contest with the same top prizes for advertisers, advertising agencies, and advertising personnel in companies. You too can win a luxurious Princess Caribbean Cruise or other prizes. And there'll be free reruns and readership awards for the winning ads. The Top 10 Contest issue is one of the year's biggest advertising opportunities, with extra readership for every ad.

ElectronicDesign

1985 Top 10 Contest Rules

Pick the *Top 10* advertisements in this issue and win a Princess Cruise for two plus $1,000 in cash...or more than 100 other exciting 2nd through 100th place prizes.

Reader Contest

Examine this issue of **Electronic Design** with extra care. Pick the ten advertisements that you think your fellow engineer-subscribers will best remember having seen. List these ten advertisements on the special entry form bound in this issue. *(Be sure to check the box marked "Reader Contest.")*

This year your selection will be measured against the ten ads ranking highest in the "Recall Seen" category of Reader Recall, **Electronic Design's** method of measuring readership—see item 6.

In making your choices do not include "house" advertisements placed by **Electronic Design** or Hayden Publishing Company, Inc. (such as this ad describing the contest). Don't miss your chance to be a Top 10 Winner! *All entries must be postmarked no later than midnight, March 1, 1985. Winners will be notified in May, 1985.*

READER CONTEST RULES

1. Enter your *Top 10* selections on the entry blank bound in this issue or on any reasonable facsimile. Be sure to indicate 1) the name of the advertiser; 2) the Reader Service Number for each of your choices; and 3) the page number for each of your choices. (House ads placed by Hayden Publishing Company in **Electronic Design** *should not* be considered in this contest.)
2. No more than one entry may be submitted by any one individual. Entry blank must be filled in completely, or it will not be considered. The box on the entry blank marked "Reader Contest" must be checked. **Electronic Design** *will pay postage for official entry blanks only.*
3. To enter, readers must be engaged in electronic design engineering work, either by carrying-out or supervising design engineering or by setting standards for design components and materials.
4. No cash payments, or other substitutes, will be made in lieu of any prize (except the $1000 prize).
5. Contest void where prohibited or taxed by law. Liability for any taxes on prizes is the sole responsibility of the winners.
6. Entries will be compared with the "Recall Seen" category of Reader Recall (**Electronic Design's** method of measuring readership). That entry which in the opinion of the judges most closely matches the "Recall Seen" rank will be declared the winner.
7. In case of a tie, the earliest postmark will determine the winner. Decisions of *Top 10* contest judges will be final.
8. First prize is a Princess Cruise for two and $1000 in cash.

Advertiser Contest

There's a separate contest open to all marketing and advertising personnel in companies, and to advertising agencies.

Examine this issue of **Electronic Design** with extra care. Pick the ten advertisements that you think will be best "Recall Seen" by **Electronic Design's** readers. List these ten advertisements on the special entry blank bound in this issue. (Be sure to check the box marked "Advertiser Contest.")

ADVERTISER CONTEST RULES

1. All rules for the Reader Contest will similarly apply for this contest, with two exceptions: readers engaged in electronic design engineering work, as defined in the reader contest rules, are *not* eligible to participate in this special contest. The box on the entry blank marked "Advertiser Contest" must be checked.
2. Entrants in this contest may use the official reader contest entry blanks or any reasonable facsimile.
3. This special contest is open to marketing and advertising personnel only at all manufacturing companies and advertising agencies, whether or not their companies or agencies have an advertisement in the contest issue.

FREE RERUNS FOR THE TOP 10 ADS

All ads that place in the *Top 10* will have the opportunity to be rerun at no charge in a future issue of **Electronic Design**, in a special section recognizing advertising excellence. Winning ads will be rerun in this special section only if matched in the issue by a paid advertisement of the same size and color. These free reruns will be made only from existing plates or negatives. If the advertisement qualifying for a free rerun is an insert, the winner may run up to a two-page spread from existing plates or negatives in up to 4-colors. Hayden Publishing Company, Inc. reserves the right to schedule reruns at its discretion.

Use special entry blank bound in this issue

(Blanks are also bound in the front of this issue)

Microprocessor programming made simple.

"Keep it simple" was the principle of the 14th Century English philosopher William of Occam and it has even more validity today. Faced with the problems of sophisticated computer systems, designers have found that ever more complex programming languages are further complicating their tasks. Until now.

Occam. Created for system design and implementation.

When we started designing our new VLSI family of 10-MIP transputers, we built on William's simple philosophy. To take advantage of the possibilities opened up by the transputer, we needed to create a language capable of properly addressing parallelism and multiprocessor systems.

With the ability to describe concurrency (whether timeshared or real) and to handle message-passing at the lowest level of the language, all aspects of a system can be described, designed and implemented in occam. From interrupt handling through signal processing to screen editors to artificial intelligence. And on.

But occam is not limited to our transputer family. It provides an efficient, responsive implementation language for systems built on today's microprocessors. It also opens up future possibilities with its performance-enhancing multiprocessor capabilities. And INMOS now offers a product to let you exploit occam's total capability in your system.

Simplify your job with the Occam Programming System.

The Occam Programming System (OPS) gives you the tools for complete VAX / VMS software development. This package includes an integrated editor / checker, an optimizing VAX compiler and full documentation. This gives you a supportive environment for the development of occam programs for execution on the VAX. Cross-compilers for 68000 and 8086-based systems will also be available.

What's more, the occam programs developed and proven on the OPS will give you a head start for work with the INMOS transputer. Extensions to the OPS will be available which will allow occam programs to run on the transputer.

And if you have a requirement to program the transputer in other popular high-level languages, other extensions will include compilers for C, Fortran, and Pascal.

Get started today.

Contact us for our information pack on occam, the Occam Programming System and the transputer. You'll be surprised how simple your life can be.

For quick response, call us at (303) 630-4000 or write: Occam, P.O. Box 16000, Colorado Springs, CO 80935.

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CIRCLE 110

10 VIEWS FROM THE TOP

Ten of the most eminent technologists, each a pioneer in his field, forecast the future of electronics for the rest of this decade and even through the end of the century. These distinguished scientists and industry leaders have chalked up an impressive list of contributions to modern electronics technology, laying a strong foundation for tomorrow's advances.

For example, Charles Kao is the acknowledged father of optical-fiber communications. Niklaus Wirth developed Pascal and Modula-2 software languages. Ted Hoff is the inventor of the ubiquitous microprocessor, and Charles House gave us the logic analyzer. Amos Joel developed the first electronic telephone switching system, as well as cellular radio. Similarly, Gene Amdahl is a world-renowned innovator in computer architectures, having been in on the initial development of many IBM mainframes. Sir Clive Sinclair revolutionized the field of consumer electronics, and Marvin Minsky has made an undeniable impact on the world's understanding of artificial intelligence. Robert Keyes brought life to solid-state device physics, and Brian Sear has influenced the discipline of automatic testing.

These men see an electronics world ripe with hardware advances, including fiber-optic developments that will bring electronics into wider use across all segments of society. Not surprisingly, they are certain that chips will climb to new levels of integration and performance—spawning the next generation of supercomputers. Though the future looks bright, the men collectively suggest that the going may be rough, with software becoming more critical, more complex, and more difficult to manage. In fact, software will ultimately tilt the scales between success or failure.

Charles Kao ITT Executive Scientist
ITT Corp.

Gene Amdahl Chairman and Founder
Trilogy Systems Corp.

Niklaus Wirth Professor of Computer Science
Federal Institute of Technology, Zurich

Ted Hoff Consultant

Charles House Corporate Engineering Director
Hewlett-Packard Co.

Amos Joel Consultant

Clive Sinclair Chairman and Founder
Sinclair Research Ltd.

Marvin Minsky Donner Professor of Science
Massachusetts Institute of Technology

Robert Keyes Member of the Technical Staff
IBM Thomas J. Watson Research Center

Brian Sear President
GenRad Semiconductor Test Inc.

CHARLES KAO

By the end of the decade, the single-mode fiber will have largely replaced its multimode equivalent in optical communications. Because of its smaller core diameter, designers thought that a single-mode cable is hard to work with. This prejudice has been largely overcome, thanks to a rapidly growing record of success.

Single-mode fiber will likely replace multimode even in specialized settings, like interoffice communications. And links using single-mode fibers have already transmitted data at over a thousand megabauds. By the end of the century, thousand-gigabaud links over distances exceeding one hundred kilometers will be attainable.

For very long-range communications, a promising recent development has been fiber-optic cable capable of sending data over great distances with remarkably low losses. These special cables operate in the long-wavelength infrared spectrum of 2 to 5 μm, and it is reasonable to expect repeaterless transmissions over a thousand kilometers.

To date, the most important breakthrough in fiber optics has been the development of single-frequency semiconductor lasers. These have been put to work transmitting information over optical cables in the laboratory. One problem has yet to be completely overcome: the laser's stability. Its carrier frequency still wanders under modulation. But even that shortcoming will be licked in the very near future.

Single-frequency lasers are truly the optical equivalent of rf oscillators. They allow frequency division multiplexing, in which two independent signals coexist on the same data path without interference.

The use of two or more carriers allows an optical cable to deliver at least twice as much data as it could with only one. This is analogous to sending two TV channels over the same antenna.

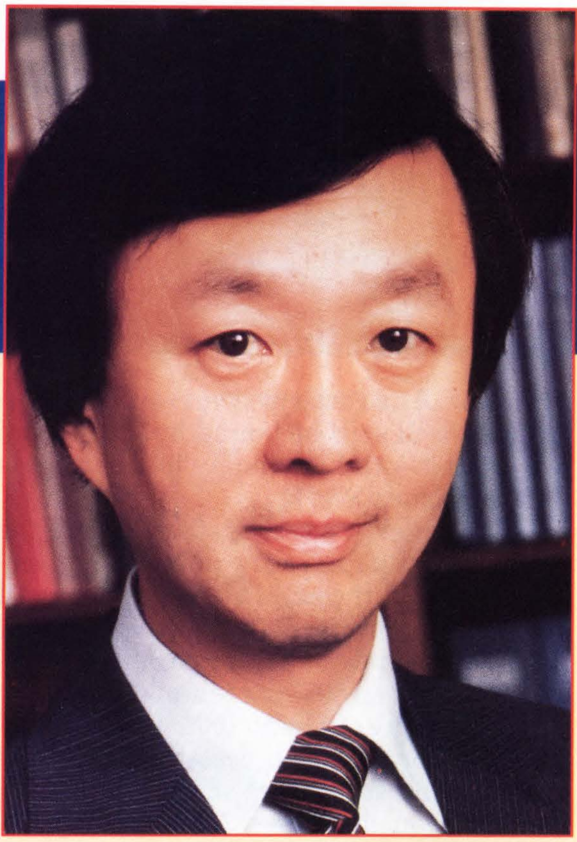
Once frequency stability is ensured, it will be possible to multiplex hundreds of totally independent carriers on the same optical cable. Each will be generated by a separate laser, just far enough removed in frequency to forestall interference. In this way the truly astounding data-carrying capacity of fiber optics will be realized.

On the detection side, improved avalanche photodiodes will soon outperform p-i-n FETs. Previous avalanche photodiodes capable of working at wavelengths greater than 1.1 μm were germanium-based devices. They suffered from relatively high noise.

Future avalanche photodiodes will be built with indium gallium arsenide, a compound with material properties that will attenuate the noise and greatly increase the gain-bandwidth products. Devices made with this compound respond at wavelengths as wide as 1.6 μm.

Using single-frequency lasers as transmitters will have the added benefit of allowing coherent detection techniques on the receiving end. It will be possible to

To date, the most important breakthrough in fiber-optic communications has been the development of single-frequency semiconductor lasers.



ITT Executive Scientist, ITT Corp.

process the incoming pulse by heterodyning the signal and using conventional detection methods, much like ordinary radio signals. The result will be not only a lower error rate, but also an even greater number of carriers on the same cable.

A new class of products combining optical and electronic functions on the same chip will also be appearing soon. One example combines an optical laser diode and its drive amplifier on one gallium arsenide substrate. To increase receiver sensitivity, a p-i-n diode detector can be combined with a FET preamplifier. The FET preamplifier has already been tested in the laboratory and should be available soon.

It might also be possible to combine the receiving diode, preamplifier, drive amplifier, and laser diode on the same semiconductor substrate. Such a component would represent an integrated transmission and reception system—in essence a repeater—on a monolithic chip. The device would likely be made of a III-V compound, like gallium arsenide, with inherent high-speed and optical-to-electronic energy conversion charactersistics.

But the future of integrated optical repeaters is uncertain. On the one hand, the technology faces fabrication difficulties. On the other, creating long-distance repeaterless optical cable may eliminate the need for repeaters entirely.

The problem of tapping into a fiber-optic cable has yet to receive wide attention. And a great deal of work is needed before fiber optics can be best utilized in different communication networking configurations. Integrated repeaters may find their most important use in that area.

Planar integrated optics is another example of the blending of optics and electronics. Here an optical pathway must be modified by means of an applied electrical field. In this way light can be modulated or switched by being focused, deflected, or directed along different pathways.

Optical switches like these are exciting but have problems of their own. Speed-power products are not as good as might be expected, and commercial development is some way off. But the technology's promise is alluring. Unprecedented speed is not the only potential benefit: Because it involves the transformation of light beams, the technique may prove to be particularly useful in fast Fourier transforms.

Charles K. Kao is the inventor of fiber-optic transmission. In 1957 he joined ITT in England and later came to the company's Electro-Optical Products Division in the U.S. He is now working at ITT's laboratories in Shelton, Conn. and West Germany. Among the many prizes he has been awarded are Sweden's L.M. Ericsson International Prize, the IEEE's Morris H. Liebman Award, and the Franklin Institute's Stewart Balantine Medal.

GENE AMDAHL

The greatest challenge facing computer designers will be liberating CPU performance from its dependence on memory access times. But this will be almost impossible to achieve as long as computer architectures are optimized for sequential processing.

Typically, a CPU executes a series of instructions. For each one, it generates a memory address, opens switches to that address, and fetches the data residing there. In such a configuration, the computer's performance is forever contingent upon how quickly it obtains the contents stored at an address. As long as computers are organized to process individual instruction streams in sequence, their speed will be determined by the memory technology used.

This dependency must be eliminated. Architecturally, it is important to eliminate sequential processing operations and to replace them with parallel processing algorithms. Technologically, we must improve device-dependent propagation speeds.

In computer architectures, a designer can segregate an instruction stream from particular memory references by building a CPU in which separate instruction and address information flows in parallel. Addresses can also be registered well in advance of the time that a particular instruction will need them. That would eliminate some of the dependence on memory addressing time.

Unfortunately, computer architects are not intent on separating instruction streams and addresses. As a consequence, evolving architectures will still be bound by sequential processing—and obviously by the access time to memory.

The parallel processing structures of the new supercomputers show promise. For vector operations, the parallelism has produced dramatic improvements in performance. But the machines rely on vector parallel processors for less than 80% of their operations.

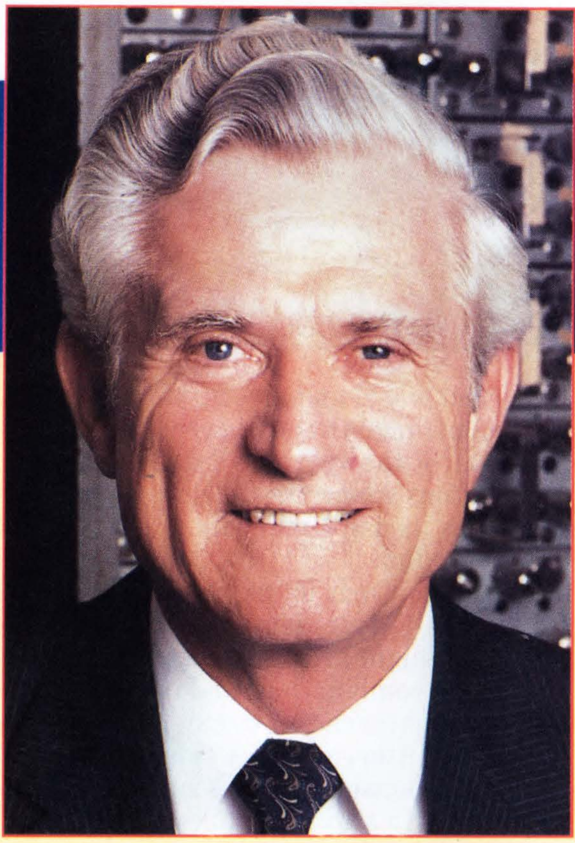
Though there can be no 100% implementation of vector parallel processing (inevitably parallel processors must share their activities with sequential ones), 90% implementation would still yield a tenfold improvement in performance over strictly sequential machines. An 80% implementation would deliver a fivefold improvement.

Even with expert systems, we will still see a great deal of sequential processing and very little parallelism. Multiple questions put to expert systems may appear to generate parallel search branches, but each of these branches is executed in sequence and depends on a sequential operation for its final resolution.

For example, no matter how many complex search branches an artificial-intelligence machine conducts, the results of each branch must still be registered, in sequence, at some central location for a comparison instruction. In fact, expert systems are a classic case of machines that are sequentially dependent.

Consequently, the results of some fifth-generation projects

Because of the dependence on sequential processing, the best hope for increasing computer performance during this decade lies with device technology.



Chairman and Founder, Trilogy Systems Corp.

are likely to be disappointing. We will see useful bits and pieces emerging—good array processors and hardware for expert systems—but not the single dramatic symbolic processor that AI people are seeking.

To be sure, there will be some movement toward parallelism. Mainframes will adopt more intelligent channels (such as peripheral controllers with built-in intelligence), and distributed-processing networks will have their own communications controllers. But these architectures will not be substantially different from the single-stream processors we see today.

Even specialized architectures are good only for a given level of performance. Though these machines pipeline instructions, each instruction still requires the CPU to compute an address.

Because of the dependence on sequential processing, the best hope for increasing computer performance during this decade lies with device technology.

Here, ECL will continue to be the fastest standard logic. CMOS will offer high performance, but it will not match the speed of ECL. It is much more economical than the latter and will be the principal workhorse in general-purpose applications, including expert systems.

The speed of CMOS devices, however, is dependent on creating small switches and positioning them close to one another. But once you step off the package with a signal, you encounter low impedances and high capacitances. Without great investments of power, these are difficult obstacles for CMOS drivers to overcome.

ECL drivers are best in this situation. It may be possible one day to construct such drivers on a CMOS IC, but the superiority of ECL technology for speed has been clearly established. For example, a 1-kbit ECL memory from Nippon Telegraph and Telephone Public Corp. features an access time of 0.8 ns. This is far better than anything projected for CMOS ICs—far better, in fact, than anything projected for gallium arsenide devices.

GaAs devices might be the fastest for simplified vector processors, especially where the gate counts are below 10,000. But if GaAs ICs are to drive signals off the chip, their performances can be worse than those of CMOS devices. A GaAs IC has very high carrier mobility, but this speed is contingent on very high impedance levels.

Gene Myron Amdahl is a recognized innovator in the field of computer technology. He started his career at IBM during the 1950s, later becoming chief designer of the 704 computer, the initial planner of the 709 and 7030; the architecture manager of the System/360. He left IBM to form his own company, Amdahl Corp., and went from there to start Trilogy Systems. He holds a BS in engineering physics and a PhD in theoretical physics.

NIKLAUS WIRTH

To understand the future of computer languages, it is best to first forget the word "language." The problem began with Algol 60, when computer scientists tried to borrow mathematical structures. So the term "programming language" became commonplace.

The idea that computer algorithms could be expressed by an ambiguous natural language has led many researchers astray. Algorithms must be described with utmost rigor and precision. Using inherently imprecise structures is utterly absurd. And in the years to come, algorithm design will be more heavily based on mathematics than it is today.

But that will not happen overnight. People tend to hang on to their software investments—be they in the form of experience and skills or programs and subroutine libraries. So new ideas spread slowly. It took Pascal 10 years to catch on, and had it not been for the fact that the microprocessor greatly expanded the software community, it might have taken even longer.

Still, Pascal did not replace Fortran—the older language was too deeply entrenched. Instead, successive revisions of Fortran grafted updated concepts onto the old roots. That's a valid technique in vineyards, where the roots are sound, but not for upgrading programming languages. Now the same approach is being tried on C. Such efforts serve only to cure the symptoms, not the disease.

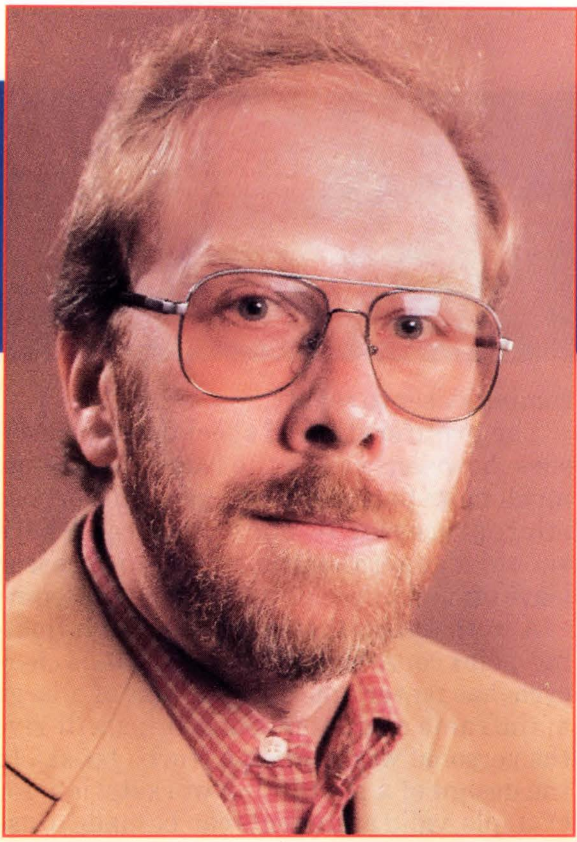
I'm afraid engineers will have to live with this imperfect world and give up the dream of a single language that will serve their needs. And that, by the way, includes Ada. Except in applications where the defense department mandates its use, I judge its prospects to be extremely dim.

Ada's big lure is its promise of solving all problems. It offers features for nearly any need that might arise—no matter how rarely. But the combinations and interactions of all these features can wreak havoc. I have heard that Ada compilers comprise several hundred thousand lines of source code. Compare this with a good compiler, say, for Modula-2, which is typically 5000 lines long. The staggering difference in length could only be justified if the benefits were of a similar magnitude.

Yet Modula-2 offers all of Ada's important features—modularity, information hiding, multitasking, hardware access, and real-time capability. So the few seldomly used features of Ada simply cannot justify its huge price tag. The Pentagon insists that a few extra million dollars will create the needed compilers, and some software houses rejoice because they are guaranteed work for years to come.

The true problem with Ada's future, the one that cannot be shrugged off, is that its complexities will have to be mastered by so many programmers, which translates into immense cost. In the private sector, memories of the PL/1 and Algol 68 languages serve to confirm the growing suspicion that

Most hardware designers believe in the same false gods as software designers—that only designs rich in features and complex in concept will impress people.



Professor of Computer Science, Federal Institute of Technology, Zurich

Ada may succumb to the same fate.

C.A.R. Hoare, of course, has predicted a bleak future for Ada in his Turing Award lecture. His answer is Occam, which concentrates on parallel processing. In fact, the concept of parallelism stands in Occam's foreground, while it is just one of Ada's many features. Occam makes it easy and natural to express concurrently executable statements and simplifies communications between parallel processes. This approach may well turn out to be just right for systems that are likely to consist of many processors. Under Occam, such systems will be interconnected over communications channels, rather than by shared memory, as today's multiprocessor systems are. And if existing systems are tightly coupled, the system bus must be used for communications, which not only requires arbitration but also tends to limit system throughput.

If such a multiprocessor system has to work in real time, congestion could be disastrous. None of the private process control languages implemented by companies or consortia seem viable to me. For instance, Pearl (used primarily in West Germany) and Chill (mandated by the CCITT) are both baroque monstrosities that are ill equipped to handle tomorrow's real-time systems.

Unfortunately, tomorrow's multiprocessor hardware may be much slower in arriving than many of us would wish. Hardware designers are, by and large, a conservative lot, since their aim is to create chips that sell well to their faithful customers. Although some of their architectures may be advertised as tuned to specific languages, in reality most are aimed at the efficient execution of assembly code and are simply downright poor in accomplishing their advertised goal.

The trouble is that most hardware designers believe in the same false gods as software designers, namely that only designs rich in features and complex in concept will impress people. In reality, a good design can be recognized by its convincing systematic structure and its suitability for the task of processing compiled code. My advice is don't introduce a new architecture until it has been evaluated with its intended compiler.

I may be prejudiced, but the whole Modula environment, which represents 25 years of healthy evolution, is more suitable for sound engineering than a complex system like Ada or Cedar (which tries to combine the best of Pascal, Lisp and Smalltalk).

Professor Niklaus Wirth last headed the computer science department at the Federal Institute of Technology (ETH) in Zurich. At Stanford University, he took part in creating the Algol W. language. He later developed Pascal, which forms the basis of most modern computer languages. Modula-2 resulted from his efforts to tailor hardware and software to work in harmony. He holds a BSEE from the ETH and a PhD from the University of California at Berkeley.

TED HOFF

Greater integration of system functions will characterize microprocessor developments over the next few years. We have already seen the integration of such functions as timers, direct-memory access channels, and memory management on microprocessor chips. Next we can expect more on-chip cache memory for program acceleration, instruction queues, and even some small instruction caches.

While new capabilities—such as on-chip instructions to handle floating-point calculations—are starting to appear, there's a lot more that can and should be done. Floating-point coprocessor chips have made tremendous progress in what could be achieved with algorithms. These chips, though, are relatively slow compared with mainframe computers, and require 1 to 10 μs for most floating-point calculations. Some new chip sets operate at millions of calculations per second. They will be the key to high-performance systems of the future.

The impact of microprocessors has already been felt in many areas. Energy control and management, medicine, consumer electronics, telecommunications, educational aids, and intelligent military weapons are just a few examples. Exciting future applications are anxiously awaited. In genetic engineering, for instance, we can look forward to processors that will accurately compute complex genetic sequences. Though that capability may still be at the science-fiction level, it is coming closer to reality.

The proliferation of specialized chips raises the question of just how much performance a general-purpose microprocessor ought to give.

The proliferation of specialized processors, however, raises the issue of just how much more performance a general-purpose microprocessor IC ought to give. Where should a general-purpose microprocessor leave off and a special-purpose device begin?

A workstation that includes a 32-bit floating-point coprocessor IC with a 100-ns clock cycle has power approaching that of a large mainframe computer. Such chips will give the personal workstation a "turbo boost." In the design of a simulation workstation, for example, valid arguments can be made to use either general-purpose or specialized CPUs or perhaps a data-flow machine containing many floating-point processors that are operating in parallel.

Though the general-purpose processor with its von Neumann architecture for serial processing still has considerable life, more dedicated architectures—that is, ones dedicated to logic or circuit simulation, data-base applications, and so forth—will serve as adjuncts to improve system performance for specific tasks.

In fact, different processor architectures are beginning to emerge, though we may not recognize them as such. We do not usually call a device that performs a peripheral function a microprocessor, whether it's a disk controller, floating-point unit, or a communications interface IC. But if you look at what goes on inside the device, you'll see much of the same types of computations

Consultant

general-purpose processors perform. Most peripheral devices have a microengine of some sort that is fine-tuned for the application at hand.

More of these dedicated architectures will evolve as new applications are defined. The gate arrays and CAD workstations needed to build them are already here. While only a few years ago the design of such chips was left pretty much to a few semiconductor manufacturers, the semicustom techniques available now have opened up the design activities to a much broader range of engineers.

With microprocessors becoming more complex, the problem of testability will arise and become quite time-consuming. Testability of a chip involves two aspects: making the chip design testable and verifying that the design does what it is supposed to do. While the first problem can be, and has been, tackled with such devices as check gates, level-sensitive scan designs, and so forth, verification may prove to be intractable. It is very difficult, if not impossible, to verify that a complex new processor architecture for which there is no proven model will work.

Complicating the testability problem is the search for design quirks, both in hardware and software. In fact, software testing will present an even bigger challenge over the next decade than hardware testing. Although we tend to be more tolerant of software bugs than of hardware faults (look at all the bugs we encounter in software programs), that attitude must change. Software costs are rising and designers are bound to find future software fixes very expensive.

Testability problems will not, of course, stop the penetration of microprocessors into all sorts of circuits. CMOS microprocessors, with their inherently low power dissipation, will accelerate the concept of portability in every aspect of electronics, including personal computers.

The computer will become an even more integral part of the data collection and management process. Consider, for example, the process of writing a check. At the present time, a person wishing to use a personal computer for home financing must perform two operations, first writing out the check, then recording that transaction in the computer file. Eventually, the purchaser will be able to orally enter order information at the merchant's terminal, and the computer will then automatically credit the merchant's records and debit the purchaser's account.

Marcian Hoff Jr., better known as Ted, is the father of the microprocessor. He worked at Stanford University and later joined Intel as manager of applied research. There he developed the first microprocessor, the 4-bit 4004, followed by the 8-bit 8008. He later became vice president of technology at Atari, leaving last year to become a consultant. He holds a BSEE from Renssalaer Polytechnic Institute and an MS and PhD in electrical engineering from Stanford University.

CHARLES HOUSE

The benches of tomorrow's engineering laboratories will not be cluttered with logic analyzers and oscilloscopes. Instead, multiple instruments will be unified into a single, compact workstation. And that move is simply indicative of the radical changes that will sweep through the test-instrument industry over the next ten years. Measurements themselves will be made on a much higher level and will be gauged in terms of overall system performance and function rather than state flow and rise times. In fact, measurement will no longer be just an engineering concern, but will be at the disposal of other professionals like doctors and chemists.

Today's design process is highly repetitive—and that too will change. An engineer builds an IC or a system and then tests it, repeating the process until the target operates exactly as it is supposed to. But computer-aided design has already advanced to the point where some simulators run a chip or system on a workstation and verify its operation without having to hook in logic analyzers or oscilloscopes. CAD will continue to strongly influence the shape of test instruments to come.

Indeed, as such simulators improve, testing as we know it will disappear: Chips will work the first time. Tomorrow's test instruments will be monitors built right into a workstation to analyze system function and performance. Their probes will be hooked directly into the interfaces between the chips that make up a system, furnishing histograms and graphs of system activity. For instance, a histogram of bus traffic in a multiple-bus system might reveal that one bus is congested while the other is relatively free. An engineer could then go back to the original to ensure a more even flow.

As CAD simulators improve, testing as we know it will disappear: Chips will work the first time, and test instruments will be monitors built right into a workstation.

The idea of a histogram of bus activity will not be limited to electrical engineering. Poets, for example, may also benefit from histograms of music-signal activity. An instrument could tell them that their rhyming words are too far apart, or that certain words are being used too often. The instrument could also tell a novelist that there are too many occurrences of a particular word, and suggest a synonym, instead.

But before bus monitors are a reality, to continue with the example, technological hurdles must be overcome. One such difficulty is originating equations that describe the flow of data and tasks in multiple-processor systems. These equations are essential, since they will allow monitors to assess the performance of each microprocessor in a multi-processor system.

Another problem to be addressed is standardizing the human interface. The industry will have to agree on how histograms and other indicators of efficiency will be displayed. A consensus will also have to be reached on how commands will be entered into a workstation. No doubt, given the level of sophistication expected of these

Corporate Engineering Director, Hewlett-Packard Co.

monitors, a command language is likely to evolve.

As CAD tools raise the level of design, engineers will ultimately be able to enter desired functions and wait for a complete set of system specifications. Thus they will no longer need to know the intricate details of circuit design or worry about the signals flowing between chips. In fact, engineers will not need to know how to pretrigger an oscilloscope or set its voltage range. Instead, tests will be carried out by connecting a probe for a local network or bus interface (such as the IEEE-802.3 or Multibus II) and watching the workstation check out the chip.

Freed from the more mundane details of their craft, designers will have more time to understand the problems they are trying to solve and familiarize themselves with the discipline to which the problem relates. Actually, this is already beginning to happen. A perfect example is a speech recognition and synthesis system. Here the designer must be as much a linguist and physiologist as an electrical engineer.

With design tools and test instruments working at a functional level, we may even reach the point when someone with a sound understanding of a problem and only a very basic knowledge of engineering could design and test systems. A doctor, for instance, may be able to create his own special heart monitor; a chemist, a process monitor.

But even if that comes to pass, engineers will always be needed. They will be working on state-of-the-art circuits that demand the detailed measurements of extremely high-speed signals. Their equipment will necessarily exhibit bandwidths on the order of tens of gigahertz.

As chip speeds take off, we'll need equally fast analog-to-digital converters for the front ends of such equipment. And they'll need to be inexpensive. As a result, the relatively high-priced today's 6-bit 1-GHz a-d converter ICs will evolve into tomorrow's low-cost 10-GHz devices, probably by 1994.

Finally, we'll need to face the issue of testability. Certainly, self-testing circuits built right on the chip, will be a great help in determining functional behavior. But for detailed amplitude or timing measurements, or both, self testing circuits are only questionably useful. They'll need to accurately measure the parameters of circuits that are already pushing technology to its outer limit, a doubtful possibility.

Charles House is regarded as the father of the logic analyzer. He has been with Hewlett-Packard since 1962, and previously was general manager for the Logic Systems Division. A guest lecturer at Stanford University and at the University of California, he was a key contributor to the GE engineering program which received the IEEE Award for Innovative Education. He holds a BS from the California Institute of Technology and an MSEE from Stanford University.

AMOS JOEL

Within five years, most of the world's telephone facilities will be digital. And this move will be paced by the growth of digital private branch exchanges and central offices that will use time-division multiplexing to switch digitized voice and data signals around the globe. In time, TDM will phase out the space-division multiplexing in switching that we've used for so long.

End-to-end digital service means that voice signals may not have to be handled at today's relatively high 64 kbits/s. For now, we're chained to that rate because of the number of digital-to-analog and analog-to-digital conversions a signal is forced to undergo during a single transmission. But with an all-digital network, we could drop to a lower digitization rate and still ensure high quality.

A lower rate also means that the popular T1 digital link will double its maximum number of channels—from 24 to 48. In turn, T1 will be used more and more for integrated voice and data communications.

Digital networks will also buy us something else—vast data bases that will be instantly accessible by subscribers—anywhere and anytime. From there, the services that will evolve are anybody's guess. We could see, for instance, toll-free facilities for locating all sorts of businesses, getting instant help with a problem, and finding the nearest office of a national organization.

The explosion in telecommunications that will follow these developments will be matched by the ability of local switches to handle more calls. Microprocessor-based switches that can shunt a million calls an hour are already waiting in the wings. That's a far cry from the 350,000 calls an hour we saw with the world's first digital switch, AT&T's #4 ESS, which was cut in 1976. That switch's capacity has almost doubled to 640,000 calls an hour. And it's not too hard to imagine that by 1990 local switches will be dealing with more than a million calls each hour.

This ability will be made possible, in part, by advances in hardware like microprocessors, memories, logic, and crosspoint-switch ICs. On the other hand, software is essential to telecommunications switching progress, and it is taking a big jump in complexity.

For one thing, the size and development costs of software programs are skyrocketing. This is a natural result of the increased emphasis on programs that must operate in real time and are efficient, reliable, and sufficiently flexible to handle new services and features as they evolve.

For another, the breakup of AT&T will push the issue of software reliability to the fore. Who will gurantee end-to-end dependability in a system that may involve several carriers? Will the software from different suppliers work well together? Can the system be trusted not to crash under any circumstance?

Digital networks will also buy us something else, vast data bases that will be instantly accessible by subscribers — anywhere and any time.

Consultant

Unfortunately, most of the failures in modern digital switches can be traced to software, not hardware, a situation I'm afraid might get much worse. Although many of today's telephone switches have suffered no more than two hours of downtime in 40 years of operation—which breaks down into 20 minutes a year—I'm not so sure we'll see that level of reliability maintained.

Telephone switching will also get a big boost from optical fibers, not only in the form of wider transmission bandwidths but also in design flexibility for central offices. The use of optical-fiber links between switch frames will allow these frames to be placed much farther apart than is possible with conventional copper wire. In time, tiny communities now served by small central offices that are themselves linked to larger offices by wire, will simply be directly linked by optical cable. The wideband services that only the larger offices offer (like video teleconferencing or integrated voice and data) will filter down to the smallest of communities, no matter how far they happen to be from the central office.

Work is also well under way that'll bring us economical fiber-optic crosspoint switches for sending real-time video signals over phone lines. One challenge to be met by these space-division-multiplexing switches is to lower the relatively high voltages needed to switch light signals over different paths. There's also work underway on using gated-diode high-energy devices as crosspoint switches. Other work further off involves the use of holographic fields to deflect light beams. At this point, TDM switches can only take care of slow-scan video and facsimile transmissions. For real-time video, we may very well have to go back to space-division multiplexing.

Keep in mind, the technology to transmit real-time video has been with us since AT&T introduced Picturephone service well over a decade ago. The sticking point is to come up with an approach that is cost effective, a goal that has eluded us except for specialized business applications.

Still, telecommunications services will expand dramatically, particularly at the local level. Helping that will be cellular radio, which will make telecommunications truly portable. The price of cellular radio has really come into line, and by the end of the decade, we may well see cellular radio standard in many cars.

For 43 years at Bell Laboratories, Amos E. Joel Jr. did ground-breaking work in telephone switching. A holder of more than 69 patents, including one for cellular radio, he received the IEEE's Alexander Graham Bell Medal, the Franklin Institute's Stuart Ballantine Medal, and the International Telecommunication Union's Centenary Prize. A member of the National Academy of Engineering and a Life Fellow of the IEEE, he holds a BSEE and an MSEE from MIT.

CLIVE SINCLAIR

With so many areas of industry and society at the beginning of their electronic evolutions, there's a tremendous push on for computing power. That need, which encompasses both conventional machines and artificial-intelligence systems, will be met only by massively parallel computers.

Hand in hand with parallel processing goes "parallel memory," locating a processor and memory on the same piece of silicon to drive speed to the limit. This trend will obviously blur today's neat distinction between processors and memories. We're likely to see more and more semiconductor companies making computers and more computer manufacturers fabricating semiconductors.

Over the next five years we should also see the power of supercomputers jump by an order of magnitude. For one thing, their number-crunching abilities will step up from the current 600 million floating-point operations a second to around 6 billion. At the same time, their memories will go from 100 to 150 Mbytes to tens of gigabytes. And minicomputer memory will hit the 100-Mbyte mark, which means we'll find the computational power of today's supercomputer in tomorrow's desktop machine. Personal computers will be right in step with the move to more power and greater memory. Five years from now even the very modest systems will pack as much as 10 Mbytes of RAM.

Since artificial intelligence eats up such staggering amounts of memory, at least for truly serious work, it may be that the availability of more memory will determine when AI really takes off. By the end of the century, if not sooner, we can expect artificial-intelligence machines with gigabytes rather than megabytes of memory. And I'll be very surprised if wafer-scale integration is not essential to making this happen.

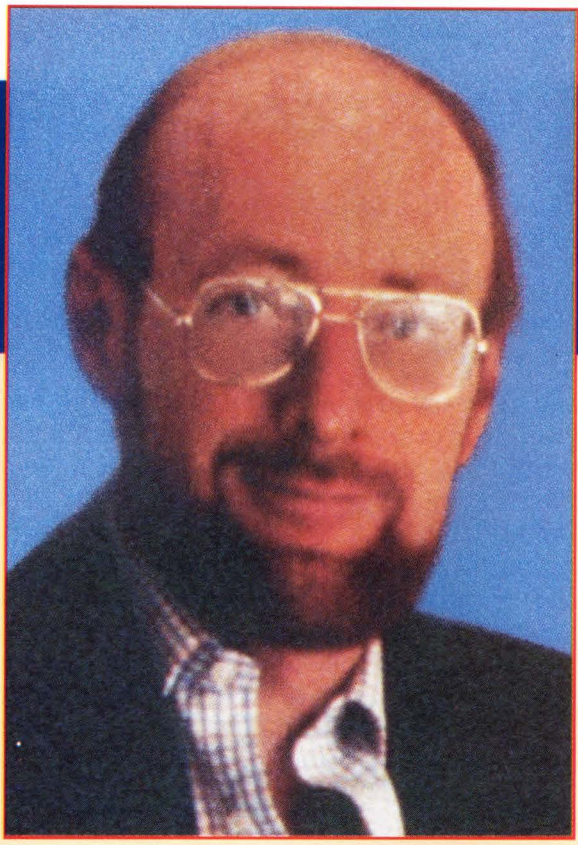
I know that a number of manufacturers have taken a stab at wafer-scale integration and failed, but it's a technology whose time has come. The techniques that have been adopted to achieve redundancy on 256-kbit and 1-Mbit RAMs can also deliver acceptable yields for ICs made with this process.

The approach has some powerful benefits in store for computing. As the number of gates to a chip rises, the approximation that the number of pins increases as the square root of the number of gates has some validity. But after a certain point, the relationship is reversed and the amount of pins actually starts to decline. Imagine a single piece of silicon that contains an entire computer, including processor and memory. Such a chip would clearly need relatively few pins.

If memory and processing are to be merged, it will be done at the highest scale possible, where the ratio of pin count to silicon area is low. Here's where wafer-scale integration, with its hundreds of thousands or millions of gates per wafer, is the key.

What it all boils down to is that before the decade is out we could very well see individual wafers carrying megabytes rather than

Clock rates — or supercomputer cycle times for that matter — are not likely to improve much unless bipolar technology undergoes a revival.



Chairman and Founder, Sinclair Research Ltd.

megabits of memory.

With wafer-scale integration and tighter geometries, the semiconductor industry should keep traveling along its accustomed route, with tenfold jumps in component count every five years. At that rate, by the end of the century we'll have a billion components on a single piece of silicon.

Speed, however, is a very different matter. Increases in operating speeds have generally lagged behind improvements in integration. Even the latest 32-bit microprocessors run at relatively slow clock rates, say, 12 MHz. Clock rates—or a supercomputer's 10-ns cycle time for that matter—are not likely to improve very much unless bipolar technology undergoes something of a revival. At the moment, since most people are pursuing the CMOS technology, this doesn't look very likely. But for boosting speed, we shouldn't be concentrating on CMOS or even on gallium arsenide—bipolar is the answer.

CMOS's low power consumption is a real advantage only in circuits where most of the silicon is idle much of the time. This is true today, where the processor occupies a relatively small amount of silicon compared with memory. But as parallel processing takes hold, and as processors are embedded in memory, more of the chip will be given over to the processor. That means a greater portion of silicon will be active at any time.

So, for a circuit made with wafer-scale integration, heat dissipation becomes the limiting factor. A wafer 4 in. in diameter dissipates about a hundred watts in free air, and if the silicon is being used to the fullest, it will have a capacitance to ground of 3 μF. Under these conditions, CMOS's clock rate is under 4 MHz, and a NMOS wafer tops out at 17 MHz. Bipolar's high transconductance and correspondingly high speed-power product deliver a 340-MHz clock. That figure is not only impressive in its own right, it beats gallium arsenide. The gallium arsenide chips that have recently shown up operate near the speed of the bipolar ICs that were available about ten years ago. And gallium arsenide is not only more expensive than bipolar, it can't be packed as densely either.

With transit times for bipolar transistors in the low picosecond range, nanosecond cycle times shouldn't be difficult to achieve. If the industry insists on staying with CMOS technology, today's 12-MHz microcomputer and 10-ns supercomputer will be with us for some time yet.

Sir Clive Sinclair, the founder of Sinclair Radionics, is a pioneer in miniature and low-cost consumer electronics. In 1972, he devised the pocket calculator. Then came an advanced digital watch in 1975 and, in 1977, the first pocket-sized TV. He later started Sinclair Research, where, in 1980, he developed the original low-cost personal computer and, in 1983, a flat-panel pocket TV. He completed his secondary education—at the age of 17—at St. George's College.

MARVIN MINSKY

If we can make a computer think, we can make it do anything. And it can be replicated just by making a copy of its program. That's why building a thinking machine is the ultimate goal of artificial intelligence researchers today.

We already have intelligent machines—machines that "know" a lot in some rigidly defined areas of expertise—but a machine actually capable of thought is not yet within our grasp.

The first step toward this goal will be creating a computer that can learn. Learning means making changes in the mind and how it approaches problem-solving. When people learn something new, they reprogram themselves. Ideally, a computers will be able to do the same: Look at their own programs, make judgments as to how they can be improved, and modify them accordingly. As it stands now, though, computer programs take just as long to solve the same problem the second time—and every subsequent time. They don't get better at problem-solving.

The most exciting breakthrough in reaching a thinking machine will be getting computers to do what people call common-sense reasoning, so that they can understand ordinary, everyday problems and situations. Right now, computers—even the ones with artificial intelligence programs—can do very specialized operations and nothing more. A computer doesn't know, for instance, that to leave a room you should go out the door. It requires very precise, unambiguous instructions for everything it does. But once a machine has common sense, we won't have to write huge programs just to tell it how to do simple things.

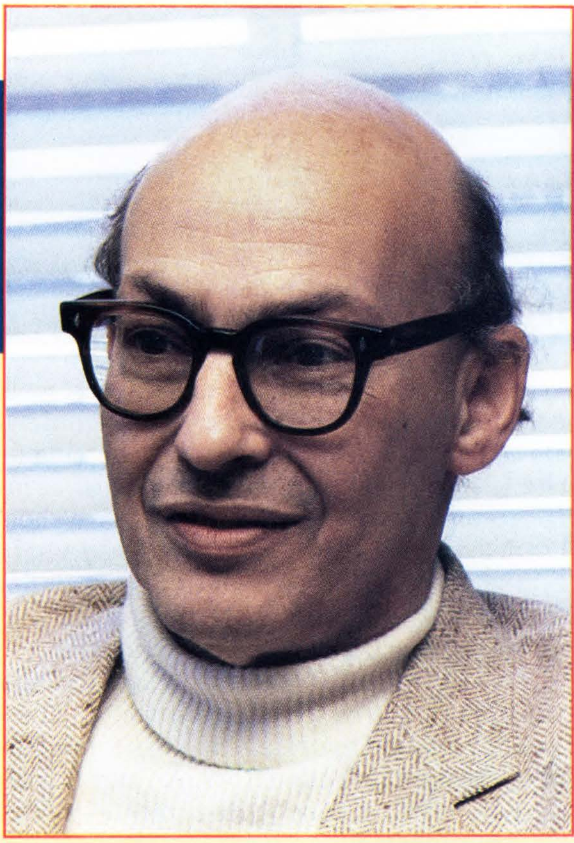
Building common sense into a computer will require some knowledge of how the human mind develops and learns. But we don't know yet how people learn, and our understanding of the thinking process—what the brain is actually doing—must be clearer if we are going to build machines with the same process.

On the other hand, it will be easier to understand how brains work once we can make machines that think. In my view, these two research areas are inseparable today.

What we need is more research in areas like epistomology, the study of knowledge. Right now, there's no theory of how the human memory—essential for any kind of learning—actually works. We don't know how bits are stored or represented in the nerve cells. Yet, people don't ever seem to run out of memory, and that's odd; you'd think they would. And animals can learn some things, but most of them can't learn much. If you try to teach a bird to speak languages, it can mimic sounds, but it can't master the grammar.

I'm working on theories of learning, and how to represent knowledge in computers. Right now, there are five or six different ways to do it, and none of them is really good enough. We are in the state of having a

Our understanding of the human thinking process — what the brain is actually doing — must be clearer if we are going to build machines with the same process.



Donner Professor of Science, Massachusetts Institute of Technology

half-dozen theories that "almost" work.

Logic is one, although I am opposed to using logic in artificial intelligence programs. Most experts in artificial intelligence use logic because the procedures are well-defined. Fifth-generation programming languages like Prolog use logic clauses—chains of reasoning—to form deductions. Consciously, people may do some of this chaining, but unconsciously believe we "reason by analogy"—that is, we go through a long process of checking memory against thousands of other experiences to see which is most similar and then matching them to the current problem. Even more important, we remember our mistakes—and try to avoid the worst ones. Most projects do not realize the importance of avoiding past mistakes, and logical reasoning does not seem good at that.

Parallel architectures are going to be important in artificial intelligence because of the speed they offer. Right now, for instance, vision systems don't work very well, but when we get parallel machines it might turn out that they are capable of more vision than we thought—just by being a hundred times faster. The same is true of semantic networks. I suspect that some of the old ideas may turn out to be practical after all.

Speed and brute force processing have made a difference in other situations as well. For example, the old chess-playing machines really didn't play chess very well, but the new ones are much better because of their speed. A hundredfold increase in speed made a real difference without adding any new ideas.

There is much talk in fifth-generation circles about the need for parallelism, but though it is essential for speed, parallelism in languages may be a matter of level. In the human mind, for instance, the speech process appears to be serial. When we think in words, we are using a single serial process to control hundreds of thousands of other parallel processes. It might be that, to solve a hard problem, we need a serial process in charge, with many parallel processes underneath.

Nobody knows how long it will take to develop computers that think, but they will come—unless somebody makes it illegal.

We'll probably start to see machines with some common-sense reasoning abilities in the next few years—most likely in the form of housekeeping robots. Obviously, they will have to reason somewhat to do a good job, but they won't have to be perfect. All they need to do is leave the house a little neater.

One of the most influential leaders in the artificial intelligence field, Marvin Minsky co-founded the Artificial Intelligence Project of the Massachusetts Institute of Technology and subsequently headed MIT's AI Laboratory. He developed new approaches in symbolic description, knowledge representation, and machine perception and new theories of imagery, memory, learning, and neural networks. He received a PhD in mathematics from Princeton University.

ROBERT KEYES

The move to scale down chip geometries will continue unabated, giving us denser general-purpose ICs like memories and microprocessors. By the end of the decade, we'll see mass-produced FETs with gate lengths of 1 μm, down from today's 2 to 3 μm. And gate widths will shrink from 10 to 20 μm to 2 to 3 μm. How will we get there?—largely with optical lithography.

Despite the predictions that optical lithography would run out of steam below 1 μm, the reports of its death have been greatly exaggerated. And its usefulness will not be limited by the resolution of light, as foretold, but rather by the resolution of the silicon processes. There's a lot more life left in optical lithography: It's already defining submicrometer dimensions in the laboratory, where 0.1-μm lines have been delineated with the aid of special techniques. And despite the popularity of electron-beam lithography, it is nowhere near taking over.

Shrinking geometries is not the only way of getting denser circuits, of course. Compaction, making better use of a given chip area, is also part of progress. Its better isolation steps also help cram things closer together—even on top of one another. The ultimate in chip compaction is three-dimensional integration, a concept that's been garnering a great deal of interest.

Compaction will push silicon processor performance to new limits, performance that will be needed by tomorrow's supercomputers.

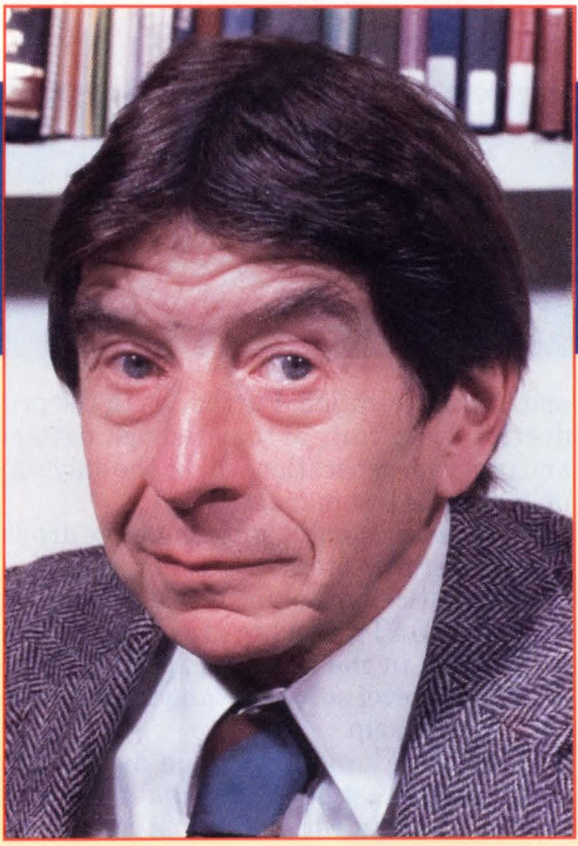
As more devices are shoehorned onto a chip...our ability to draw the heat away will become the limiting factor as far as speed is concerned.

But to build high-speed processors, we'll need to make some breakthroughs in materials science and heat removal. I'm betting on the latter to deliver new levels of computational power. As more devices are shoehorned onto a chip, its operating speed will be limited by its power dissipation. Our ability to draw the heat away will become the limiting factor as far as speed is concerned.

If we were suddenly able to draw ten times more heat away from a chip, we wouldn't necessarily be able to drive ten times more current through its conductors. At higher current densities, a conductor exhibits greater electromigration, a phenomenon that only gets worse as the conductor's temperature increases.

We've been able to retard electromigration somewhat, for example, by adding a bit of copper to the aluminum conductor. Tungsten is even better than aluminum—in terms of cutting electromigration—but tungsten has a higher resistivity than aluminum. At this point, what we need is an advance in materials science, but it is hard to see where it will come from.

Let's look instead at what we've been able to do with heat removal, say the water-cooled thermal-conduction module that houses the 3081 CPU. The 7-by-7-mm chip dissipates 5 W/cm^2; that's the kind of heat you find on a stove when you're cooking. Even better cooling will be realized by straightforward applications of engineering principles. And liquid cooling will show up more and



Member of the Technical Staff, IBM Thomas J. Watson Research Center

more as higher-performance supercomputers arrive.

I wouldn't be at all surprised to see such supercomputers using cryostats, or supercooled chambers. Although they're now bulky, these chambers are bound to be made smaller. Cryogenic cooling is the best approach of all, since a conductor's resistivity drops dramatically, and its current-carrying abilities increase by a large factor.

Even without cryogenic cooling, though, the 5-W/cm^2 dissipation levels that we consider state of the art today will more than double within a decade, through advances in water- and air-cooling techniques.

This progress will allow us to keep chip temperature to within 20° to 30°C above ambient, quite a step down from the 40° to 80°C we're used to seeing. That, in turn, will allow us better control of electromigration and increase our ability to pump more current through a chip. The result will be higher chip operating speeds.

To be fair, there are those who champion lowering operating voltages as a way of reducing power dissipation. Certainly we're running chips at much lower levels than in the past, but I don't believe we can go below 1 V. This appears to be the limit, although we're not there yet.

Pushing voltages below 1 V is limited by the very nature of digital logic. The nonlinear response of digital systems demands a certain minimum saturation level for switching from one state to another. Furthermore, a minimum potential is needed to compensate for operating voltage tolerances caused by variations in the process, operating ambients, and so on.

Getting better chip cooling will not free us from problems entirely. There's also the question of connecting the chip to the outside world, which brings up a whole new set of challenges, including those posed by wire bonding and soldering, as well as chip packaging.

Although it's been said that we'll eventually be able to put so much on a chip that it will be virtually self-contained, the truth is that designers have always managed to find reasons for more outside-world connections. Take a look at the human brain. It's divided into two halves, each with a tremendous amount of processing power, yet there are some hundred million connections between them. I'm not so sure tomorrow's chips will be any different.

Robert W. Keyes has been studying solid-state physics and the limits of device integration since the early 1950s, when he began looking into the properties of semiconductors at Westinghouse's Research Laboratory. He came to IBM in 1960. Keyes is a fellow of the American Physical Society and a member of the National Academy of Engineering. He holds a PhD in physics from the University of Chicago and was awarded the IEEE's W.R.G. Baker Prize.

BRIAN SEAR

True, the sophistication of today's chips may complicate the job of the future automatic test equipment, but I'm confident that ATE will rise to meet the new testing challenges. After all, over the past ten to fifteen years we've stayed ahead of problems generated by higher device frequency, accuracy, and pin count. I see no reason that ATE's strengths should not grow to match changing technology requirements.

The difficulties of automatic testing are easy to see: Chip complexities double every two or three years, as do the number of test vectors that deliver the stimuli to the device under test. Furthermore, the number of pins per semiconductor chip is rising incredibly quickly, with some modern monolithic ICs sporting 160 to 200 pins.

Though ATE hardware will undoubtedly evolve to satisfy that growth, software will make all the difference. Just look at its recent effect on ATE: Software has already slashed test program development time from six months or a year to just a few months. Within several years, that time will fall to a few weeks. Even more important, software tools will be able to automatically generate test patterns and vectors in a far more sophisticated fashion than manual generation can reach. Nevertheless, an overall test strategy will most likely be improved by test sequences of macrotests on sections of silicon circuitry through manual interventions. This will optimize the initial stages of chip production and characterization. Further on in the production cycle, fully automated test pattern and program generation will be the only way of life for the test manager.

As the cost of solid state memory drops, the number of vectors in a test program will rise dramatically, making it that much more difficult for ATE users to grasp just what is happening in the testing process. That's when high-level software languages will be called on for help.

High-level languages like Pascal bring structure to test programs and a growing base of Pascal talent. In the long run the test community will supplement this structured level with languages designed specifically for ATE—languages that can describe waveforms, analyze and interpret test results, and graphically represent the results on a CRT screen. Their most valuable assistance will come from software that promotes a better user interface through such handy features as windows, interactive menus, and on-line test aids.

The improved interaction between man and machine will aid designers in meeting three basic challenges: quick turnaround, higher productivity, and improved yield. Test systems will feed back information to both designers and test engineers, so that both departments can cooperatively produce tests that match a chip's needs.

Whereas simulation is the domain chiefly of design engineers, it will gradually become a valuable adjunct of the test gen-

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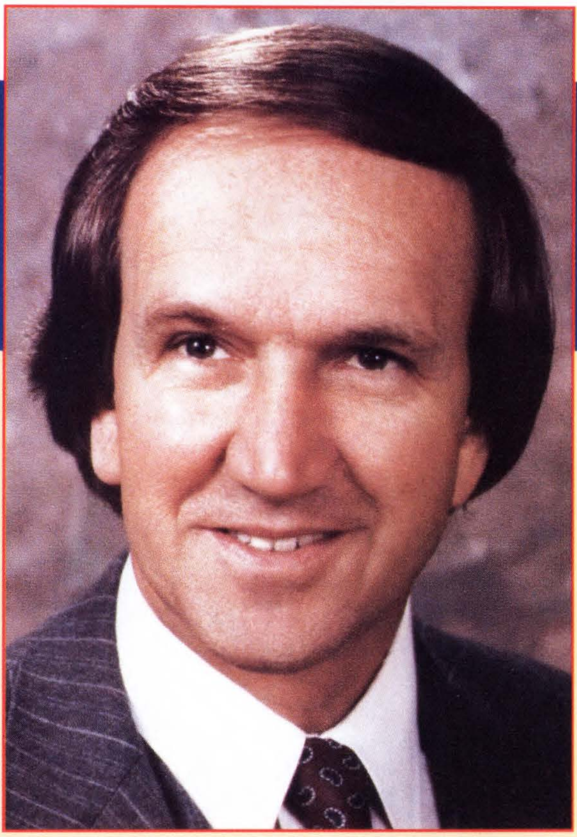


President,
GenRad Semiconductor Test Inc.

eration and validation processes. Already simulators can generate basic tests drawn from the chip structure and software-induced errors. With the right combination of simulators and other software tools, the number of duplicate test vectors should drop dramatically, so that test programs would be able to exercise a chip in much less time than they can today.

As ATE and development systems become more software-intensive, they'll start to share data with—and actually become a part of—a new CAD/CAM community. Chip designers will then have an advantage, since their familiarity with testing tools will lead to a more testable chip.

Moreover, translator programs will enable test programs written in different languages to be transported from system to system and ultimately to cross development system boundaries as well.

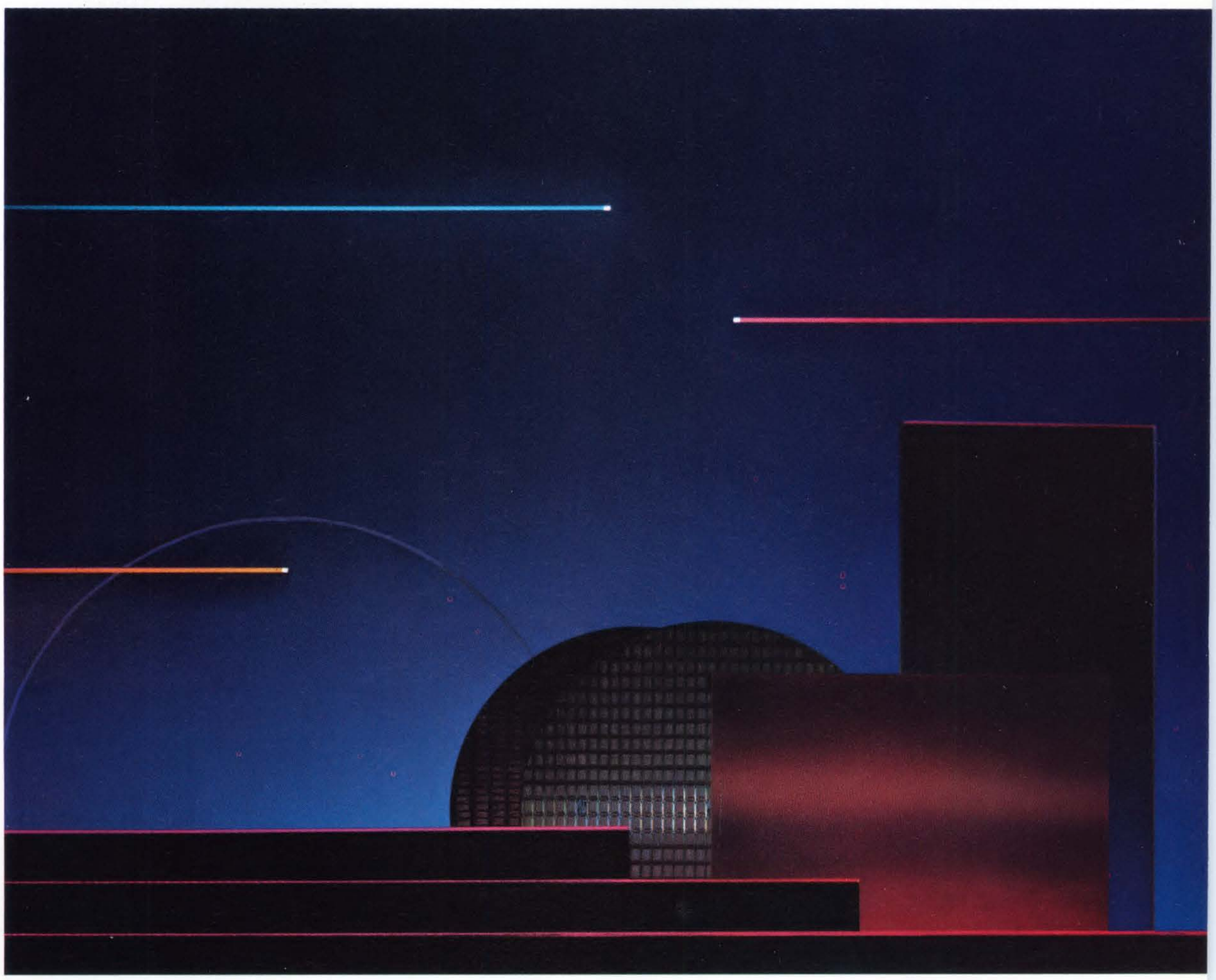
Software will also push the design of the recent pin-slice ATE architecture to a more flexible organization with reliable error fields. In the former case, each pin in a test program is assigned a specific slice of each function. In the latter case, groups of pins can be arbitrarily assigned to separate sets of functions. The shift will foster greater use of microprocessors as test pin controllers, going from the present average of one microprocessor for every four pins for parametric testing to several microprocessors for every pin.

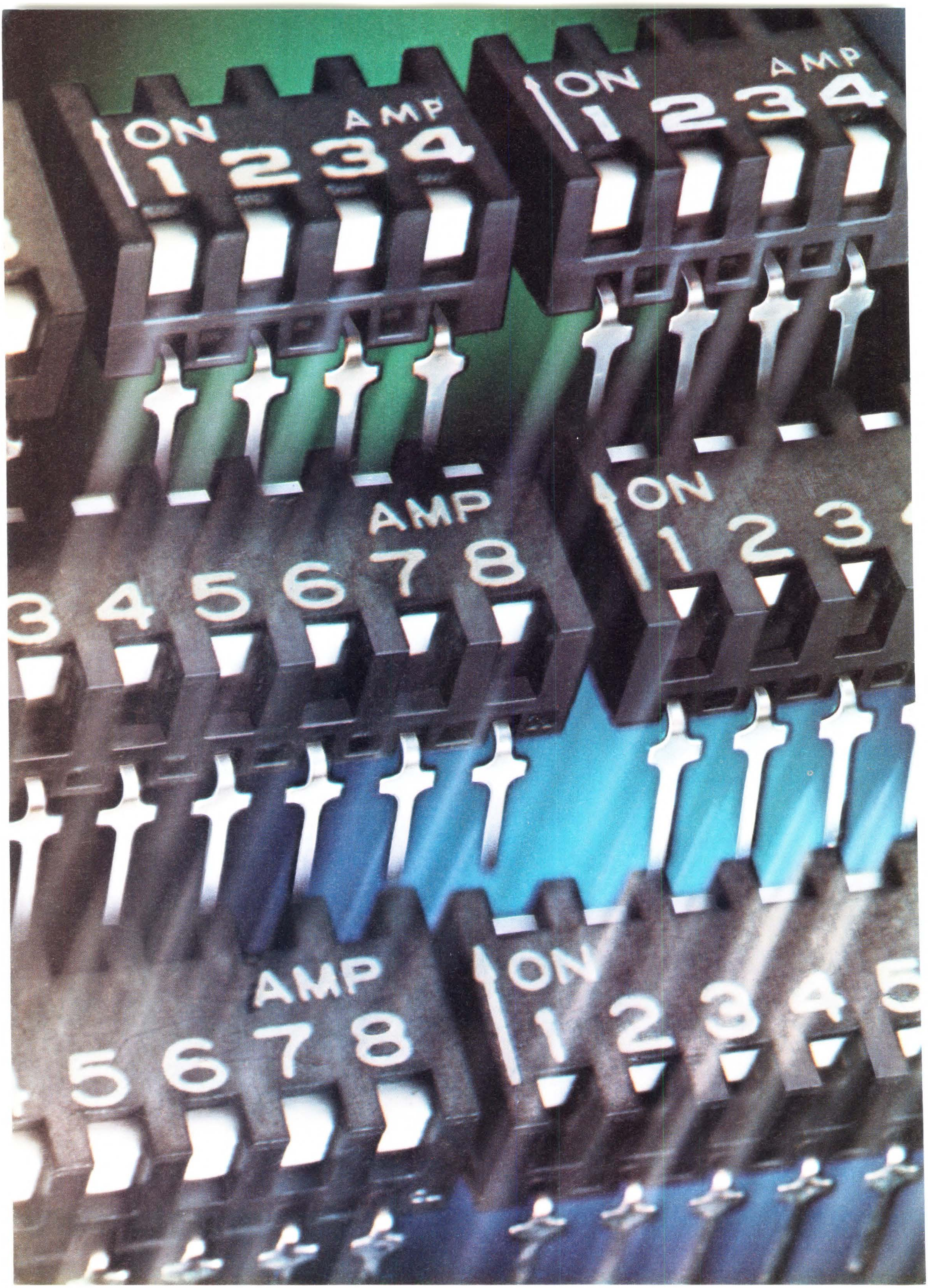
The changes in ATE hardware will probably not match the magnitude of developments in software. The general ATE setup remains one in which a chip test fixture feeds a test head, which in turn interfaces with rack-mounted equipment. Gradually processor power will migrate from the familiar racks to the test head and perhaps finally to the test fixture. As that happens, the software will mesh more closely with the semiconductor chip under test, giving ATE systems the characteristics of a distributed processing network.

One question I keep getting asked is, When are the big testers going to be replaced by self-testing circuits on the chip? People asking that question miss the point—that the test process itself evolves with the development of the chip and is not independent of it. Even the most sophisticated self-testing monolithic circuits will require the use of a large tester to check them out early in the chip's life cycle.

For the past six years Brian Sear has been a champion of VLSI testing at GenRad Semiconductor Test, which he founded, developing systems for VLSI logic, complex ceramic substrates, and production testers. Earlier, he specialized in testing at Fairchild Test Systems, where he supervised Sentry and Xincom systems. Also founder of Xincom and Interlink, Sear has a BSEE equivalent from Wimbledon Technical College and an MSEE from Drexel University.

CIRCLE 113




ON
AMP
1 2 3 4
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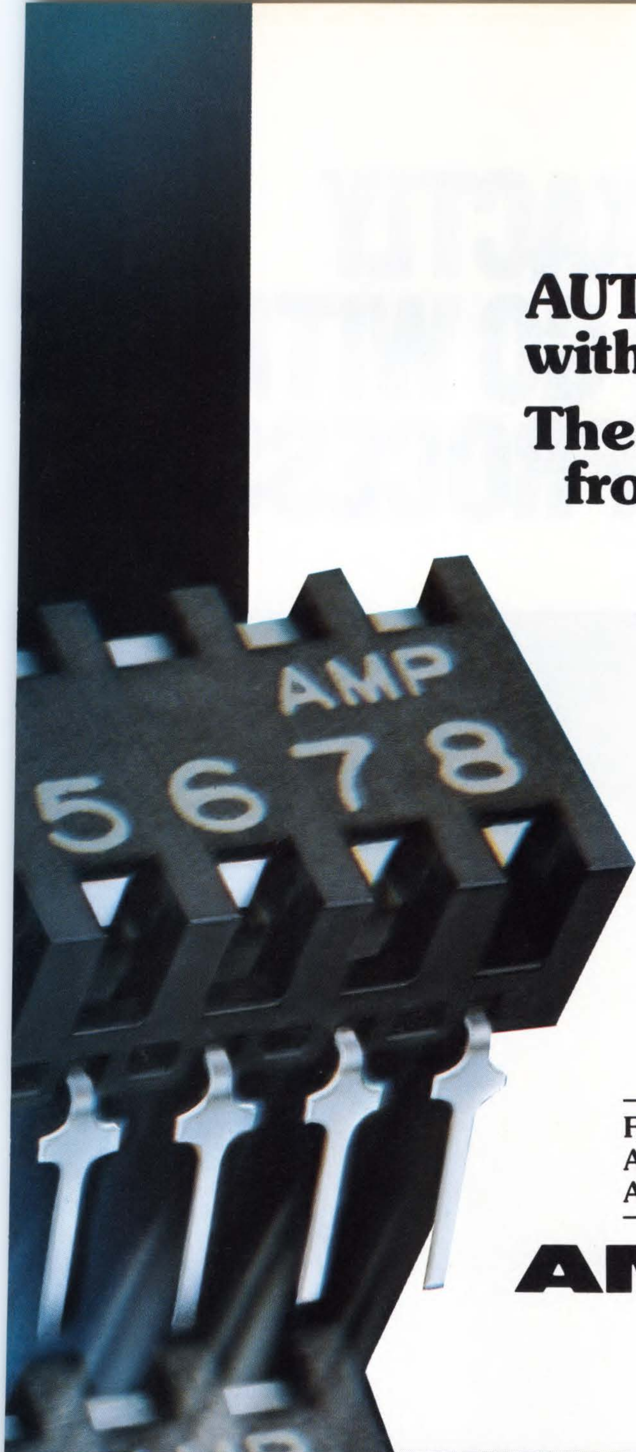

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AMP Interconnecting ideas

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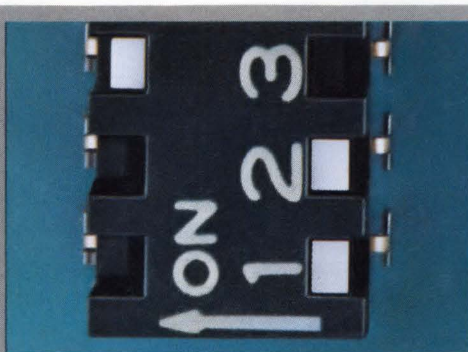

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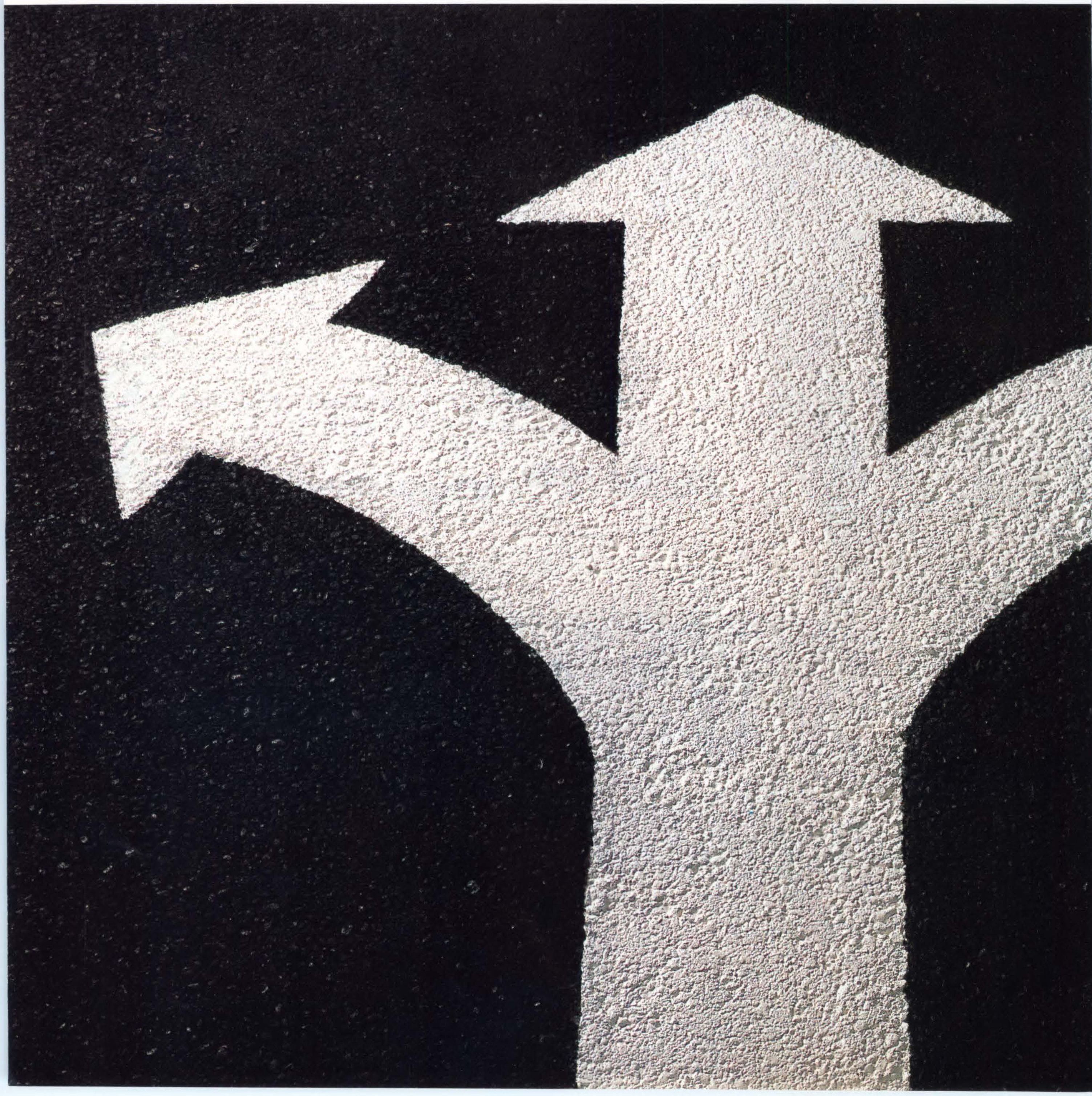

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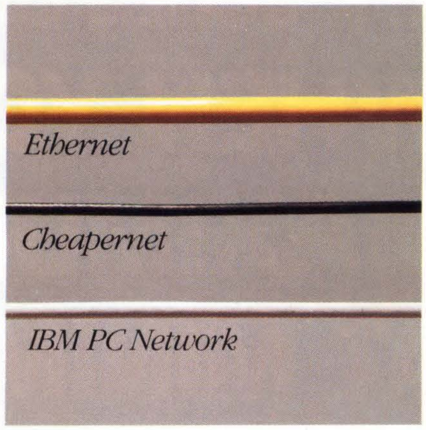

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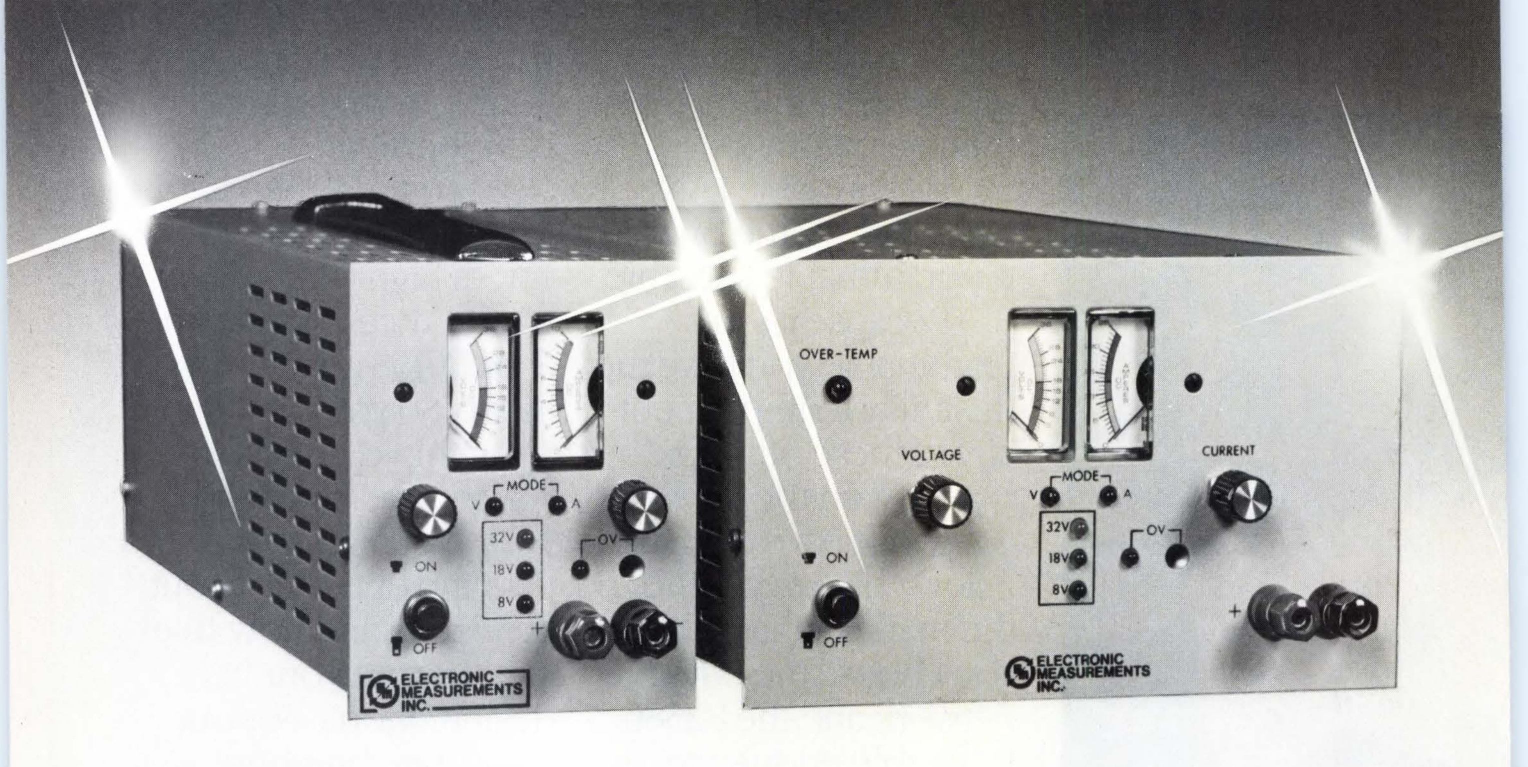

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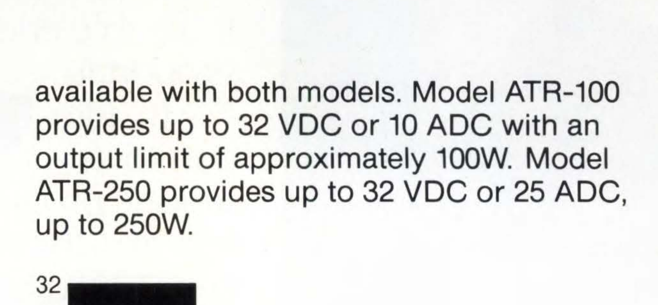

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Primed by a processor, an analog comparator chip can run its own show

With on-chip logic adjusting the comparator's threshold, the main microprocessor in a data retrieval system is free to raise throughput.

When employed in a modern data acquisition system, analog-to-digital and digital-to-analog converters often leave most of the processing and control tasks to a microprocessor. Typically, though, the user trades off system speed for the convenience and simplicity of a central controller. As a result, such systems spend significant computing resources on performing such repetitive functions as servo and process control, limit detection, and go/no-go operations.

Techniques for improving the throughput, cost, and flexibility of such systems have generally been restricted to tweaking the basic device technology of conventional a-d and d-a converters. However, two multiplexed comparators, especially valuable for control applications, expand the abilities of data acquisition hardware beyond the simple a-d converter and toward a more complex subsystem. With the ADC0852 or ADC0854 components, a microprocessor need no longer keep in constant contact with a converter or its control circuitry.

Each unit combines its own timing and control block of logic with a comparator, an analog-input multiplexer, and a unique charge-balanced 8-bit d-a converter (see "Converter Takes Charge to Balance Offsets," p. 290). The converter works at sampling rates of up to 400 kHz. All that on-chip capability allows the unit to select one of two or four analog input channels (Fig. 1); repeatedly adjust the comparator's reference (or setpoint) threshold in midstream via the d-a converter; and then compare each particular threshold (or set of thresholds) with whichever external analog input it applies to.

This process is carried on largely without intervention by the system's central microprocessor. In fact, after the processor initially programs the multiplexer and d-a converter through the Data In line, it normally communicates with them only when operating parameters change, as when an oven is set to a new temperature.

Leonard Sherman, National Semiconductor Corp.

Leonard Sherman graduated from MIT in 1975 with a BSEE and subsequently worked there at the instrumentation laboratory of the Nutrition and Food science Department. He is now an MOS analog applications engineer at National Semiconductor in Santa Clara, Calif.

A multitude of modes

Accepting analog signals ranging from ground to the supply voltage value, the versatile multiplexer in the 14-pin ADC0854 has four input channels that can be configured as either four single-ended or two differential inputs. Each channel has a high input impedance, so that source resistances of up to 1 kΩ can be driven without adding noticeable error in measuring threshold points.

A pseudodifferential input mode—geared for reference potentials other than ground—

accepts multiple inputs that have a common return path. This range of options greatly simplifies the design of analog interfaces for a variety of transducers, signal sources, and circuit configurations. One chip can process analog signals from single-ended sources, as well as signals referred to some other arbitrary level, and can do so on successive readings.

The ADC0852 is similar in function to the ADC0854 but has fewer options; thus it can be housed in an eight-pin miniature DIP. It contains a two-channel input multiplexer that operates as two single-ended or one differential input channel. The pseudodifferential capability, the external reference input, and the $+V_{in}$ line all are omitted. (The $+V_{in}$ line enables the ADC0854 to operate from an unregulated supply and can be used instead of the V_{CC} line if the input current is limited to less than 15 mA.) The remaining functions of both parts are identical.

Low power consumption (35 mW at 5 V) and a serial programming format make both ICs ideal for remote applications in which they are located near the transducer. The end-point limits, as well as the range of the threshold or set-point d-a converter, are adjusted through the chip's V_{ref} and analog ground inputs. Using a known reference voltage is especially helpful when the controller's set point must be finely adjusted. It also helps minimize or even eliminate the need for analog signal conditioning at the comparator's input.

The actual programming of the comparators is straightforward. First, the Chip Select line is

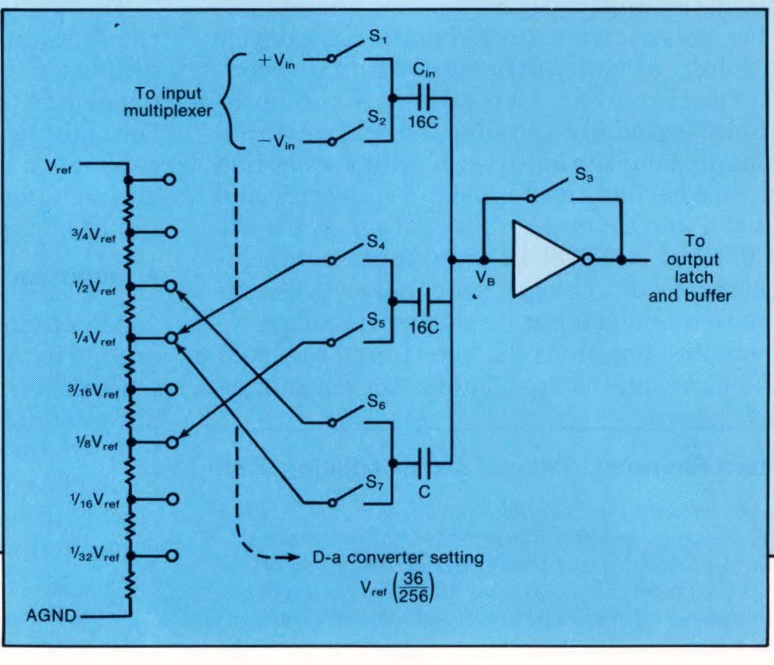
Converter takes charge to balance offsets

Charge balancing is often used to eliminate offset errors in CMOS comparators. But the ADC0852 and the ADC0854 are the first components to use the technique for a digital-to-analog converter as well. In essence, the converter serves as the differential switching device at the comparator's input (see figure).

A complete analog signal-sampling operation comprises two steps. First, the difference between the input voltage, $-V_{in}$ and the comparator or inverter's bias voltage, V_B, is stored in the input capacitor, C_{in} by closing switches S_2 and S_3. Assuming the threshold voltage is constant for one operation, the inverter thus amplifies the difference between $+V_{in}$ and $-V_{in}$ through its open-loop gain. The comparator chips use three such differential pairs, one for input signals and two for setting a reference; thus the comparator's output is actually a function of six analog inputs.

The resistive ladder connected to V_{ref} has eight taps, which can be converted into 256 (2^8) analog threshold levels with four decoding switch trees, S_3 through S_7. These trees are set and switched in and out of the circuit periodically by the control and timing logic.

One input pair uses a capacitor with a value 16 times that of the other pair to provide a suitable weighting. Therefore, at any given time the 8-bit representation of one level of the possible 256 can be selected. In this case, the switches are set for a threshold of 0010 0100 or, in analog terms, V_{ref} (36/256). Note that in this sampled system no actual dc level representing the d-a converter output exists. For that reason, the converter signal can be used only by the device's internal comparator; it cannot be supplied as a device output.



activated. Then, three bits are sent over the Data In line, selecting the appropriate analog input channel at the multiplexer. Another eight bits, traveling over the same input, direct the converter to set the comparator threshold (Fig. 2). Sampled signals that appear at the chip's channel input and exceed the set threshold bring the comparator's Data Out line high. The output signal, which is continuously updated at the clock rate, is then typically used to key a high-priority interrupt that warns of changes in important system parameters.

Heat alarm

Applications abound for the multiplexed comparators. First consider a multichannel thermocouple temperature alarm that monitors large ovens or refrigeration chambers at several locations (Fig. 3). In this case, four separate J-type thermocouples (operating over 0° to 300°C) are monitored for being under or over a certain temperature relative to a user-selected trip value.

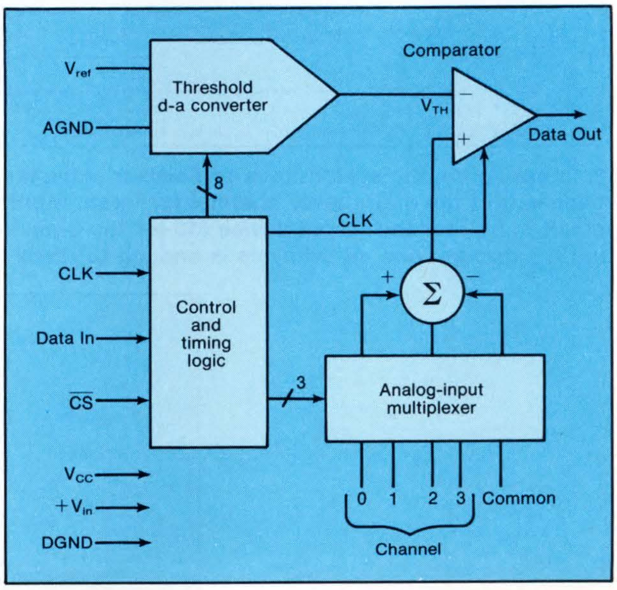
The desired temperature limit and the address of the channel to be monitored are entered through the chip's Data In line. The set limit can of course be a minimum or a maximum, depending on how the processor handles the comparator's output level. If a window comparison is required (i.e., the input normally lies between two preset limits), the processor can define separate thresholds for the upper and lower window limits, so that comparisons can subsequently be performed at any point in the process.

The comparator chip thus has monitoring capabilities well beyond those of a conventional a-d converter when used in a control application. Yet it does not place too much of an extra load on the system's central processor.

In operation, a cold-junction compensation circuit, consisting of an LM335 temperature sensor and an LF444 quad op amp, supplies the required correction for all four thermocouple inputs. The temperature sensor monitors the thermocouples' connection-block temperature (T_{ref}) and supplies a proportional compensating voltage to the chip's Common input. Compensation proceeds without further multiplexing. The circuit can be calibrated with relative ease because only one circuit must be adjusted.

The measurement and control of liquid flow represents one of the most difficult problems in industrial processing. In many cases, the best solution is a thermal flow transducer, which detects temperature changes in a fluid stream. The amount of heat picked up by the fluid—and thus its temperature rise—is a function of the flow rate past a regulated heater. This measurement technique has one major advantage: The sensor's reliability can be extremely high, because no moving parts need be placed in the stream.

The transducer itself consists of a standard heating element and two LM34 monolithic thermal sensors, which are placed in the fluid stream (Fig. 4). The heater delivers constant power to the stream at a point situated midway

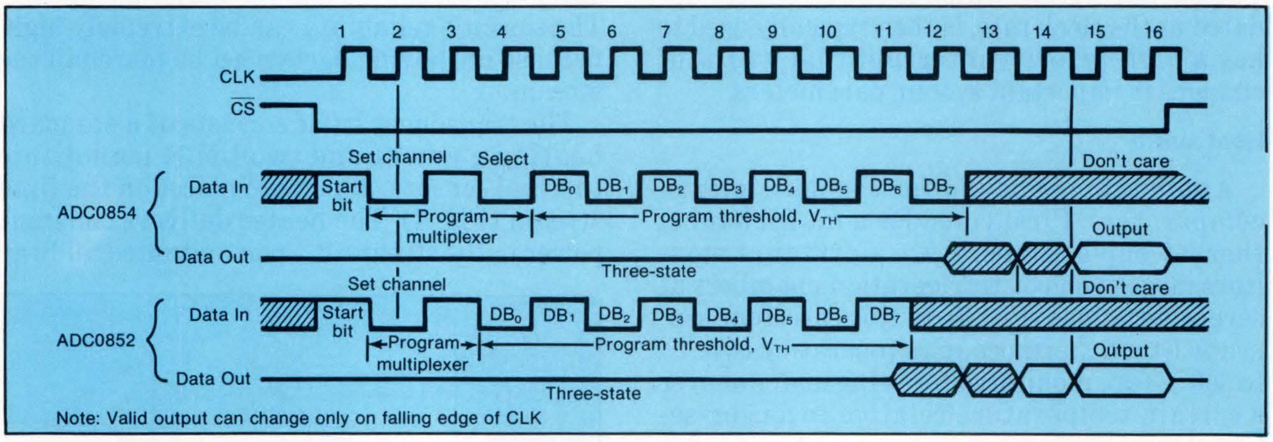


1. Timing and control logic in the 14-pin ADC0854 and the 8-pin ADC0852 comparator ICs offloads a system microprocessor of most of its analog control functions. Nevertheless, the processor is still responsible for initially setting both the comparator threshold (via the digital-to-analog converter) and the channel multiplexer. The 8-pin device unites COM and the two ground lines, omits channels 2, 3, and V^+, and combines V_{ref} with the V_{CC} line.

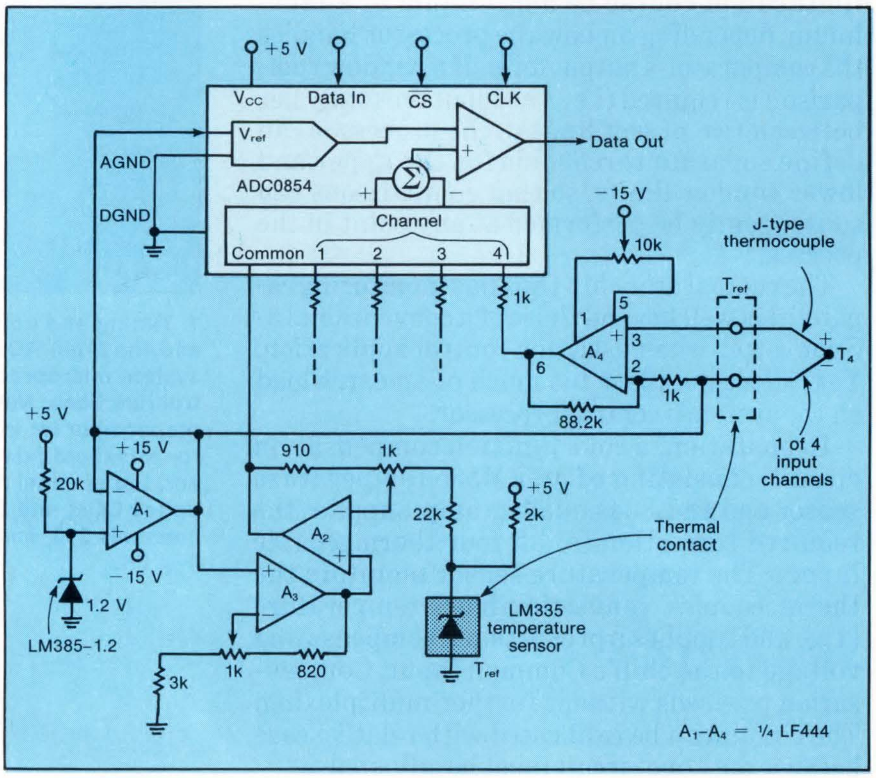
between the two sensors.

The interface required for the sensing setup is relatively simple. In this configuration, the differential-input capability of an ADC0854 compares flow direction and speed with a preset value. The chip is programmed to read the difference between the sensors, so that the direction and rate of flow can be determined.

When fluid is flowing in the direction from sensor S_1 to sensor S_2, S_1 reads the ambient liquid temperature. Meanwhile S_2 is warmed by an amount dependent on the heater's known power dissipation and the flow rate. The flow rate, F, is KW/T, where K is a constant, W is the power dissipated by the heater, and T is the differential temperature. K is a function of tube



2. In operation, the system microprocessor activates Chip Select (logic 0) and then uses the Data In line to choose first the multiplexer channel (program multiplexer) and then the comparator's threshold value. After 14 clock pulses for the 14-pin device (13 for the 8-pin version), the on-chip logic activates the comparator. Toggling CS through one on-off cycle is enough to ready the comparator for reprogramming.



3. One comparator IC can monitor up to four compensated thermocouples in a system that detects whether an oven or refrigerator is operating below or above a certain temperature. Each sensor can be assigned its own trip point within the range of 0° to 300°C.

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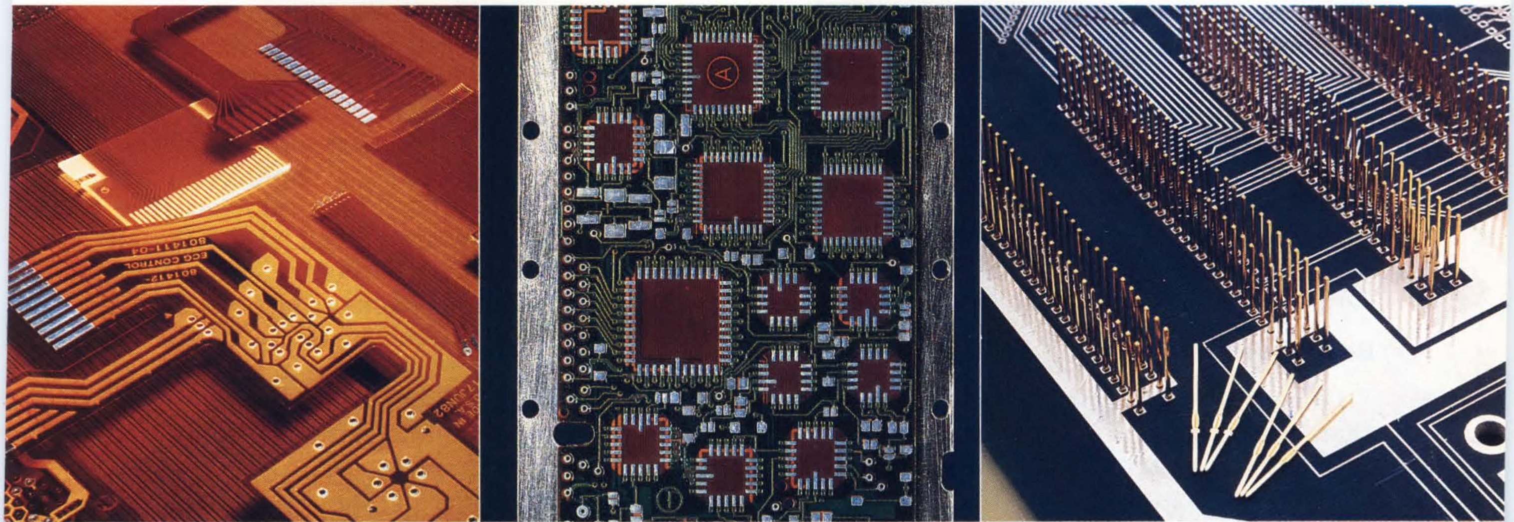

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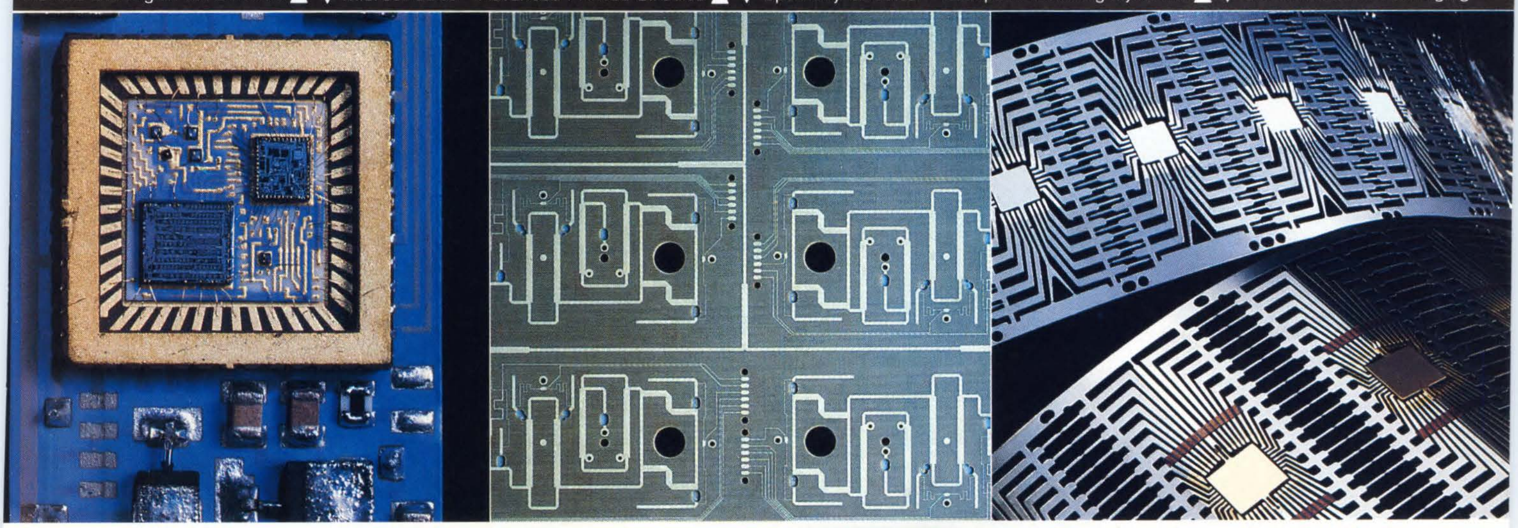

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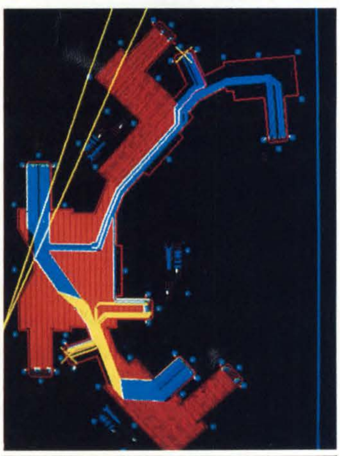

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CIRCLE 115

diameter, thermal losses, and the specific heat of the fluid that is being measured; in most cases it must be determined empirically.

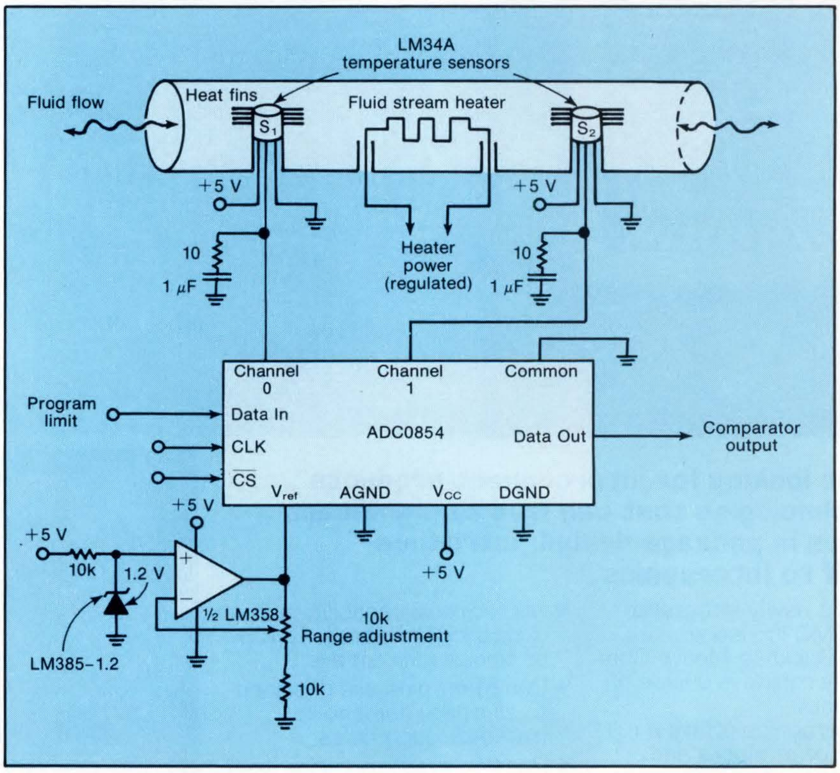
The actual value of the flow rate can be measured as well. The ADC0854 can do an a-d conversion without using extra circuitry. The conversion is achieved by stepping the comparator through a binary-weighted sequence of thresholds. This successive approximation search zeros in on the exact value with 8-bit accuracy.

Best for control

Of course, this approach takes more time than using a conventional a-d converter. But in terms of the system, it may be extremely efficient if the circuit's primary function is control and if measuring is done only occasionally. In this case, the ADC0854 constantly monitors drops (or increases) in flow rate below (or above) a minimum level. With the same hardware connections, it can also measure the actual flow rate and water temperature at less frequent intervals.

Motor control for robotics and industrial machinery finds wide use in computer-run assembly equipment, in graphics plotters, and numerous consumer areas. The ADC0852, for instance, makes an ideal dc motor controller for motion-control applications (Fig. 5). A serial data stream generated by the central microprocessor is applied to the Data In line, setting the desired speed. The chip then maintains the motor at the programmed speed without further instructions. A new speed can be selected simply by reprogramming a new threshold.

Self-regulation of the motor speed is achieved by a circuit containing a pnp power Darlington transistor, Q_1. The feedback circuit



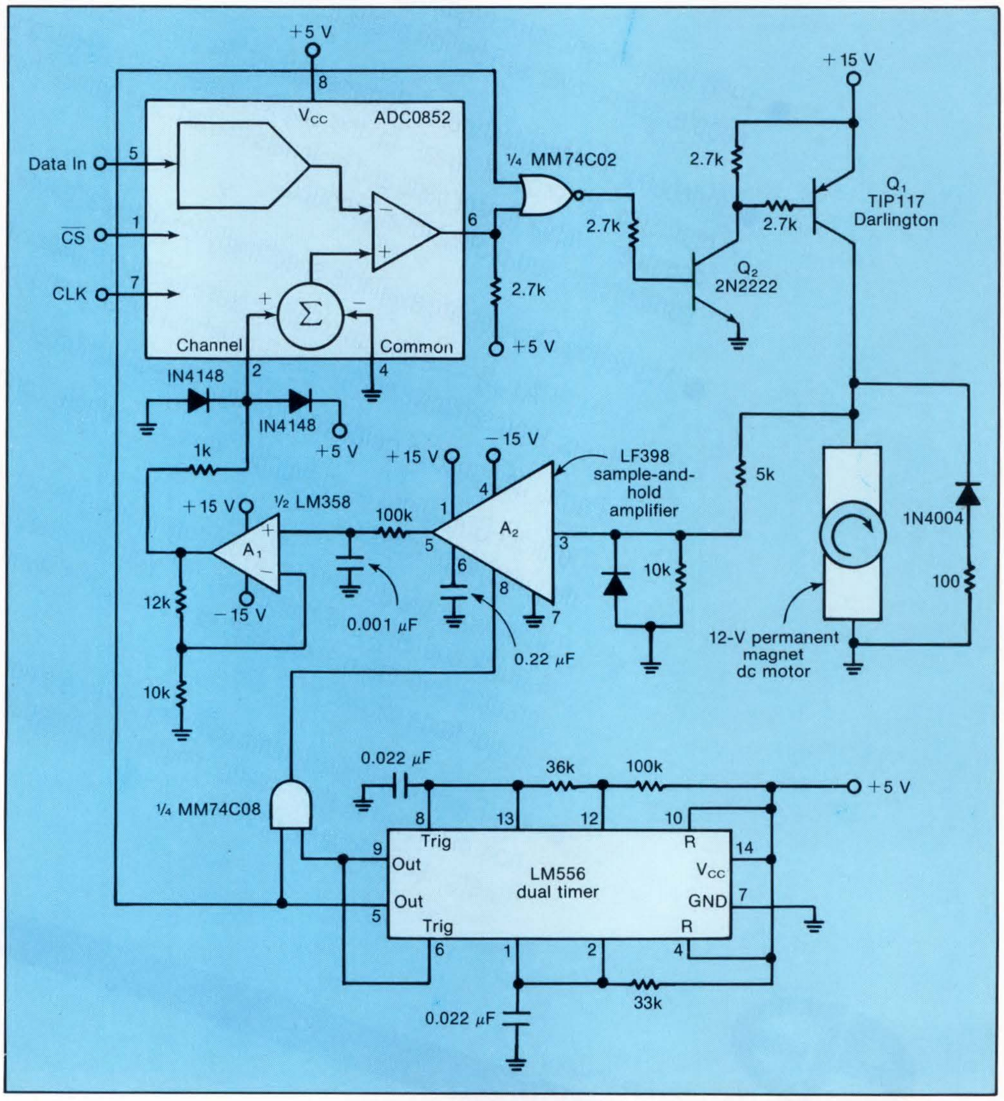
4. The ADC0854 teams up with two thermal sensors to measure the flow rate of a liquid. A differential temperature-measuring circuit enables preset limits to be detected in either direction.

Comparator chip

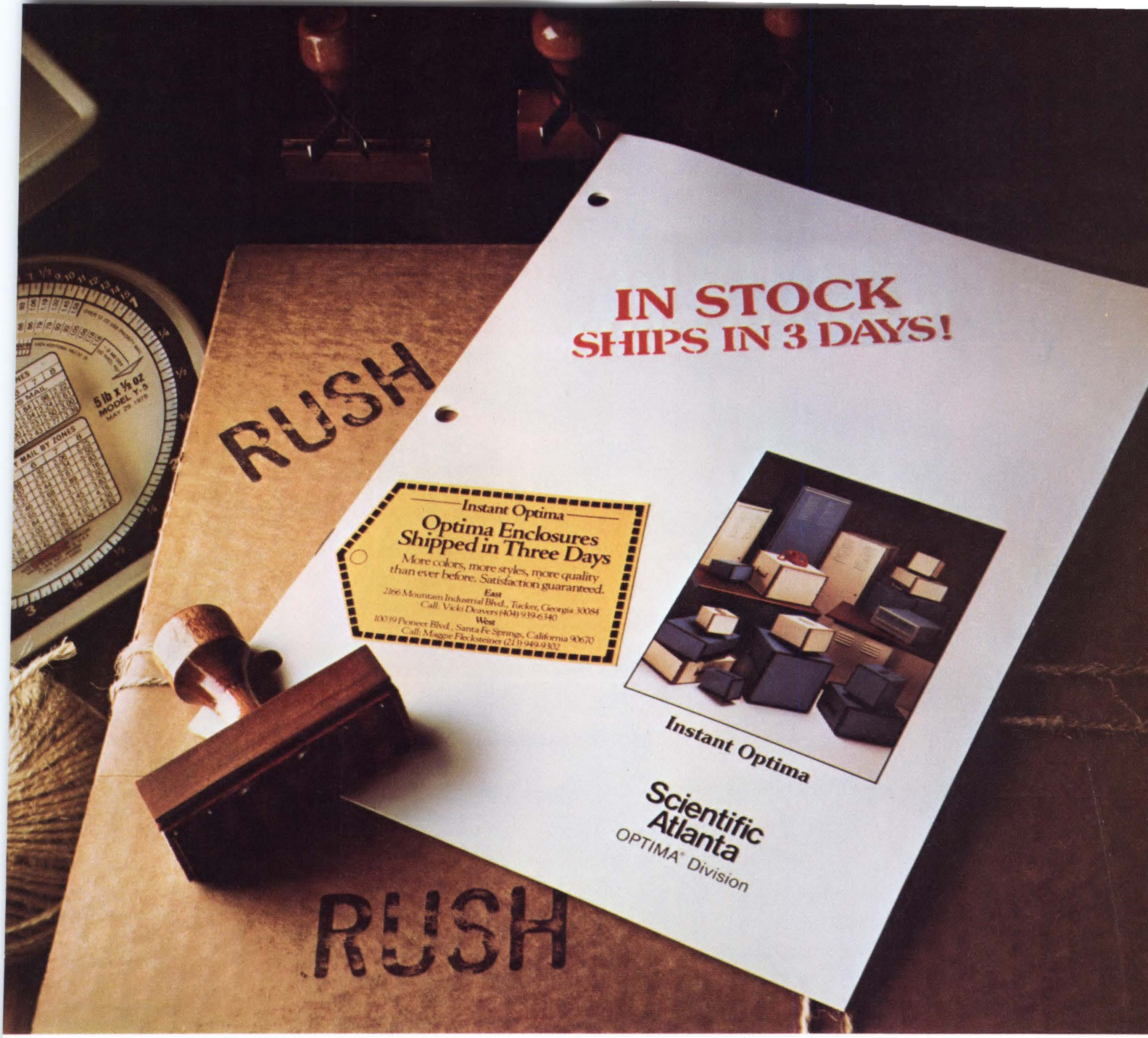
also ensures that the motor's speed is largely independent of variations in line voltage and load. A feedback signal proportional to speed is generated from the motor's back EMF while the motor is pulsed off. The signal is then sampled by sample-and-hold amplifier A_2 and smoothed by a low-pass filter before being applied to the comparator's input.

A separate oscillator and one-shot (LM556) ensure that the timing for the motor's drive never operates at a 100% duty cycle. Thus there is always some "off" time during which the speed-sensing feedback circuit can operate; otherwise, the control servo would hang up.□

How useful?	Circle
Immediate design application	541
Within the next year	542
Not applicable	543



5. In an application for which it is particularly suited, the ADC0852 controls the speed of a dc motor. A sensing loop in the controller detects back EMF, ensuring that the circuit remains insensitive to changes in line voltage and loading.



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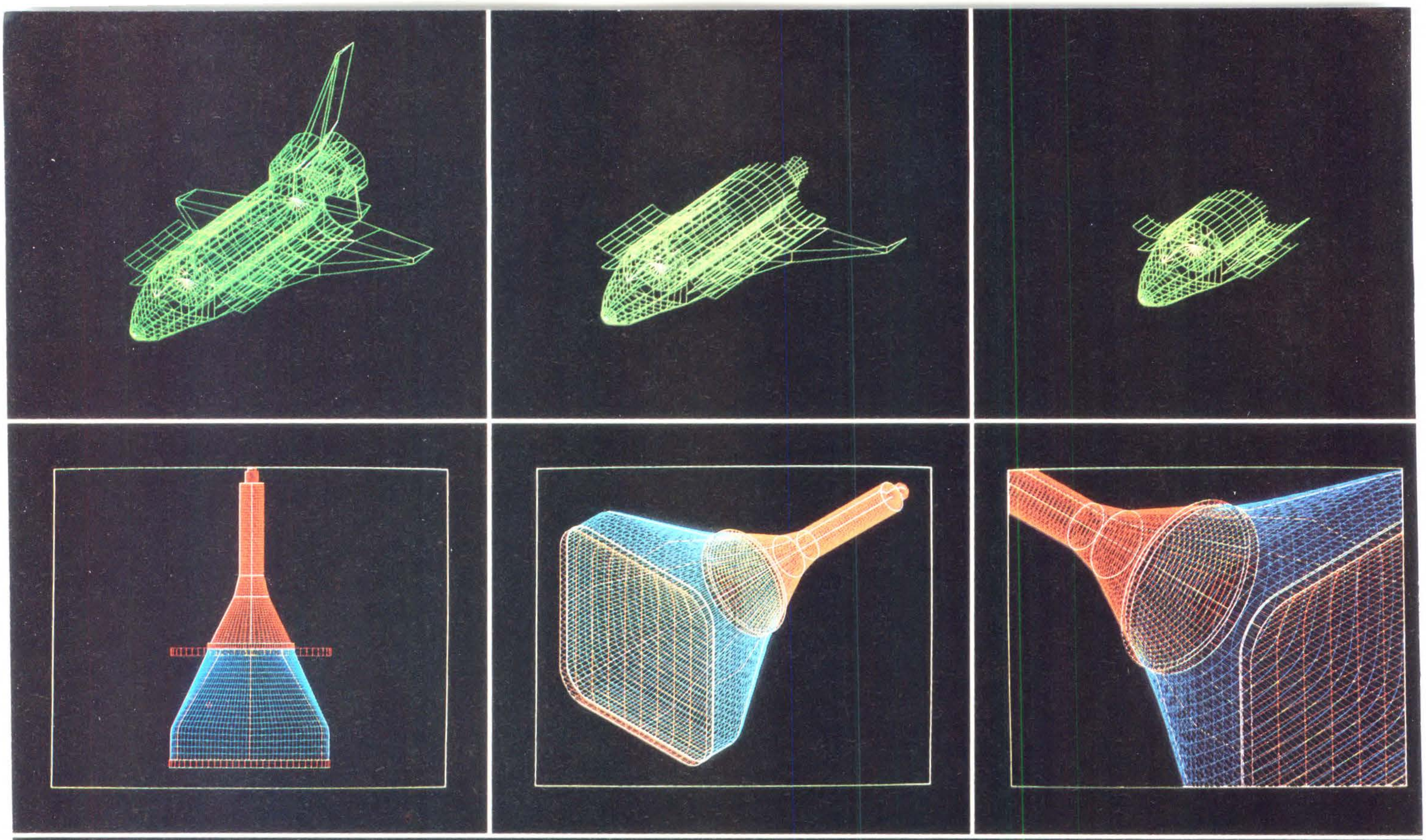

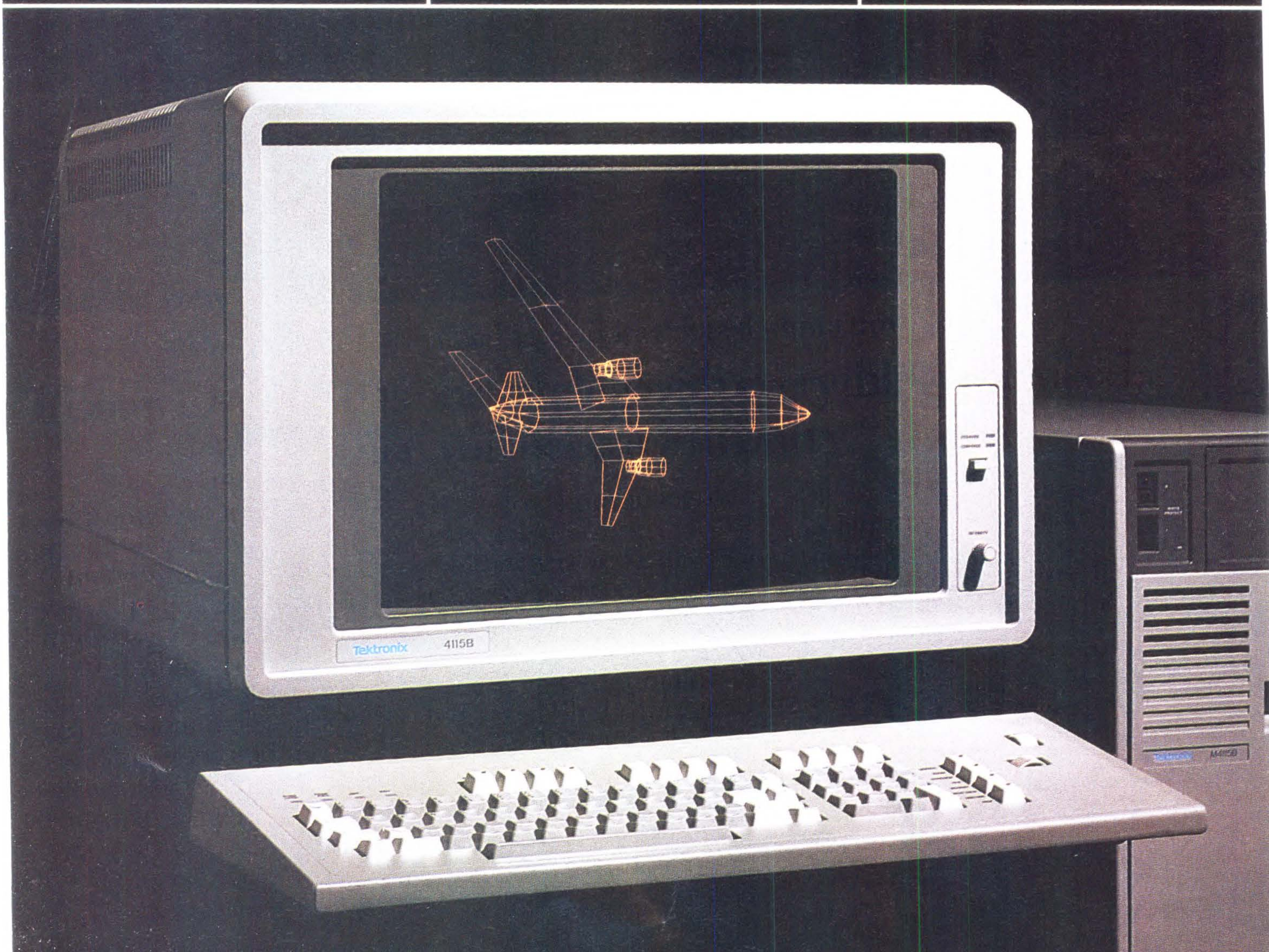
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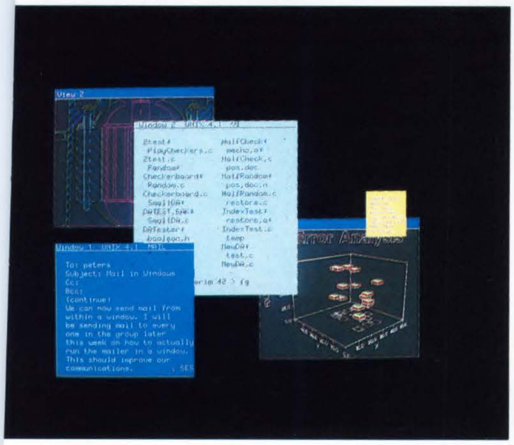

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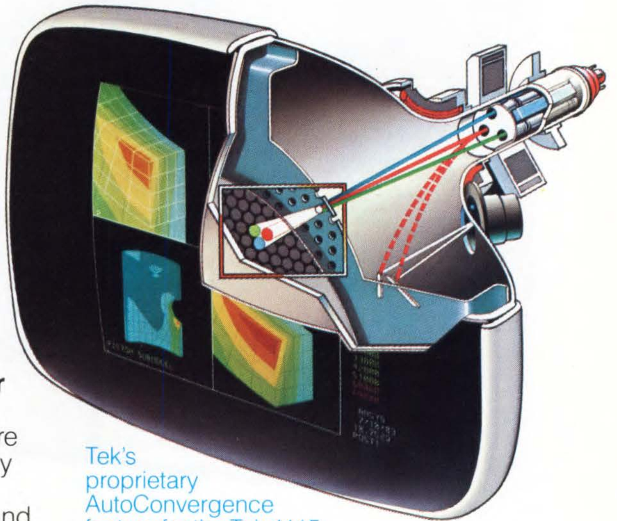

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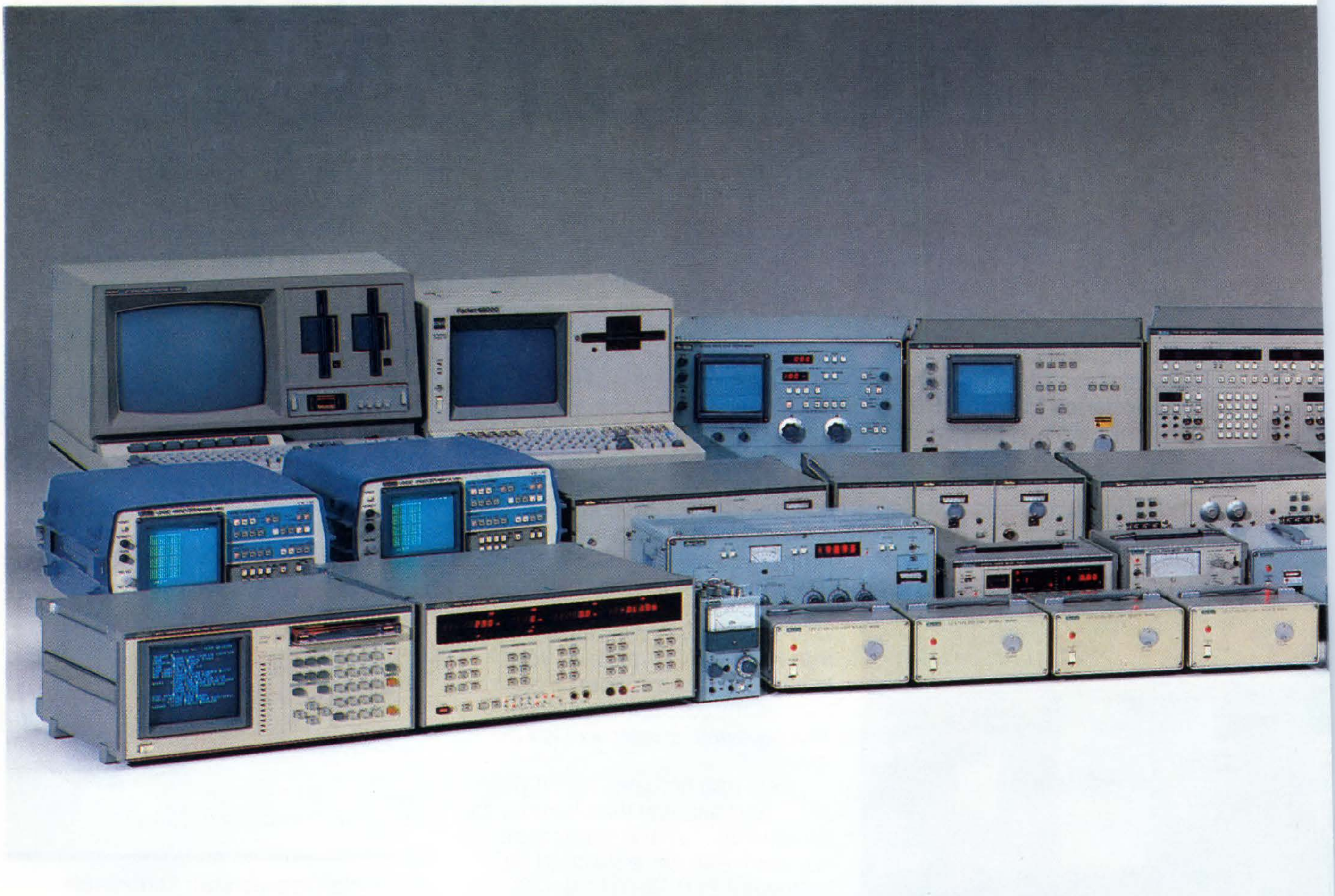

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Memory management and I/O prove 8-bit processors cannot be counted out

What seems like another 8-bit CMOS microprocessor actually includes a memory management unit plus a DMA controller and a range of I/O functions.

Far from surrendering to their 16- and 32-bit successors, 8-bit microprocessors are thriving in their own right. And although the wider CPUs are the chips of choice for high-end designs, 8-bit processors still command the lion's share of applications. Looking ahead, there is no doubt that these devices, given their low-cost, ready availability, ease of use, and growing wealth of software, will remain popular for years to come.

Bolstering this outlook is a high-speed 8-bit CMOS processor that is compatible on the machine-language level with the 8080, 8085, and Z80 families. And the HD62801 is more versatile than any of these other CPUs. For example, the chip features a central processing core that is enhanced with a memory management unit that gives the machine a 512-kbyte address space. Hence, the memory unit overcomes one of the chief drawbacks of 8-bit processors: their 64-kbyte address limitation. The core also sports a fast microcoded instruction execution unit that adds 12 instructions to the Z80's full complement and traps op-code errors. Further, its bus-state controller accommodates Z80, 6800, and 6500 peripheral chips, and a controller for managing vectored interrupts rounds out the core's features.

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Internal synergy

What's more, the microprocessor boasts powerful I/O functions like dual-channel DMA, as well as one high-speed and two standard-speed serial ports. It also carries a two-channel programmable counter and timer (Fig. 1). By squeezing so much I/O capability on chip, including a 6-MHz clock and a wait-state generator, the TTL-compatible processor reduces not only a project's part count and design time but also the risk of timing problems. Simultaneously, because all the features are on chip, there is a synergistic interplay between them. Programmable wait states and dynamic refreshing, for instance, are available during a DMA operation, and a nonmaskable interrupt will conveniently suspend or abort a DMA transfer.

Finally, as a CMOS part, the microprocessor lends itself to small, portable, and battery- or solar-powered applications. Yet the chip in no way lacks the processing power or speed needed for a desk-top or rack-mount assignment.

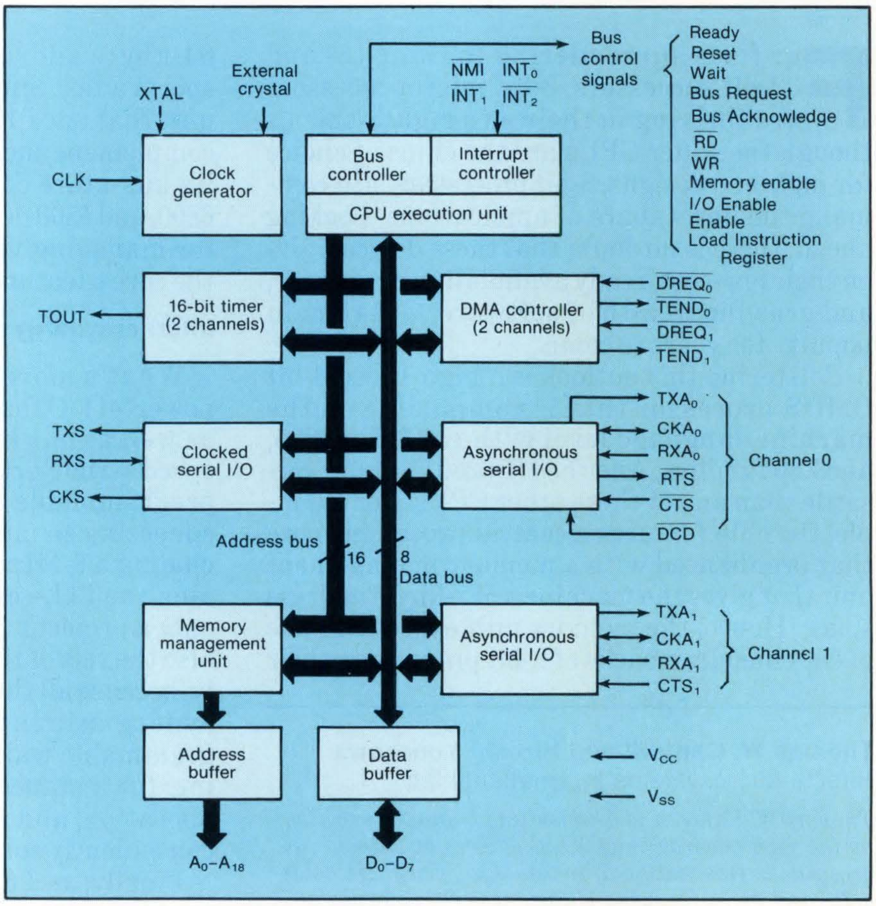
The most dramatic improvement over other

8-bit CPUs can be seen in the chip's memory management unit, which helps the processor meet the needs of memory-intensive chores without giving up compatibility with software written with 64-kbyte memories in mind. It gives programmers the choice of writing large RAM-based data structures or using RAM buffers to hold data that is written from disks. The second scheme is especially useful because it guarantees fast access to 512 kbytes of memory without sacrificing the ability to run existing application software or work with the CP/M-80 and CP/M-Plus operating systems.

The unit maps 64 kbytes of logical address space into 512 kbytes of actual memory, using a bank-switching technique similar to that found in board-level designs. The logical space is divided in three; into common areas 0 and 1, plus the bank area (Fig. 2). By programming two base registers, a designer can fit common area 1 and the bank, within 4-kbyte boundaries, anywhere into the 512-kbyte physical address space. To ensure that software written for a 64-kbyte address space can be readily employed, the processor initializes all three base registers to zero when reset.

Go forth and multiply

Besides adding memory space, the processor also adds 12 instructions to the Z80's standard set. These are useful for personal computers, office automation, and industrial and instrumentation tasks (see the table, p. 306). Among them is an unsigned 8-bit multiplication (MLT) com-



1. The HD62801 combines an enhanced central processing core (compatible with the Z80) and four major I/O subsections. The core's memory management unit expands a logical address space of 64 kbytes into one of 512 kbytes. The I/O features include a DMA controller, high-and low-speed serial ports, and dual counter-timers.

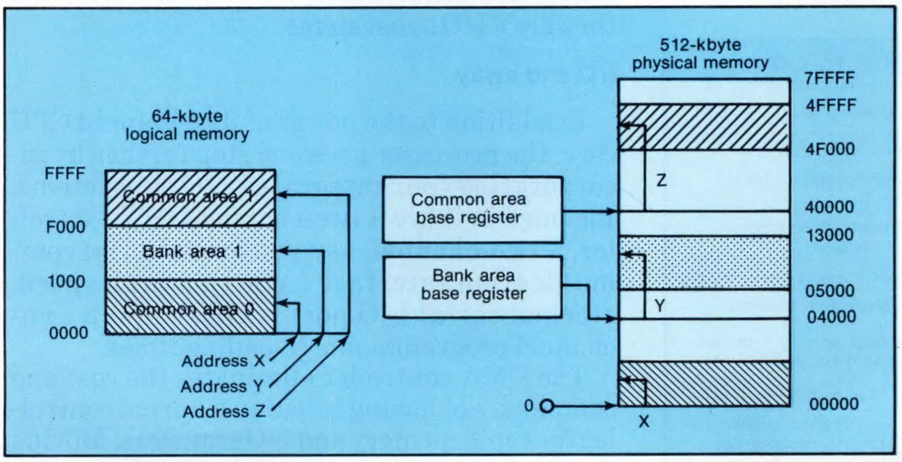
mand that yields a 16-bit result in 17 clock cycles (2.83 μs with a 6-MHz clock). This powerful instruction streamlines existing math routines and improves system performance.

Four nondestructive test instructions help to quickly check out a byte without altering its value. These instructions set the status flags as if an AND operation was executed, but without destroying the contents of the accumulator. Depending upon the instruction, a byte in the accumulator is ANDed with one in a register (TST r), in a memory location (TST m), or in an indirectly addressed memory location (TST [HL]). The fourth instruction ANDs an immediate value with an I/O port (TSTIO). Another quartet of powerful instructions, for moving data in blocks, efficiently passes information through the chip's I/O ports. And two other I/O port instructions transfer data from an immediate memory address.

The last instruction, sleep (SLP), cuts the processor's power drain from 15 to 9 mA (at 5 V dc and 6 MHz). It comes into play, along with two operating modes IOStop and System Stop, in battery-powered configurations. Invoking SLP stops all CPU activity but lets all I/O functions operate normally. Conversely, IOStop, which cuts current drain to 10 mA, shuts down all I/O functions but keeps the CPU active. System Stop, which conserves the most power, cuts the current to 3.75 mA and halts all I/O and CPU activity. Reducing the operating frequency is another way to lower power drain. For example, at a 2-MHz clock and 5-V dc supply, the current—for a fully active chip—falls to 5 mA (Fig. 3).

Speed all around

The chip's execution unit, like its expanded instruction set, is designed to speed most operations. To hasten execution, the unit is microcoded and so avoids the interconnection delays found in random logic schemes. For example, one frequently used operation, the indexed-register load, runs in 14 clock cycles rather than the Z80's 19. Using a Gibson mix of instructions



2. The on-chip memory management unit eliminates the 64-kbyte address limit associated with 8-bit microprocessors. Using it, a designer defines three areas within the 64 kbytes of addresses and maps two of them—the bank area and common area 1—into a 512-kbyte address space. The starting address of each mapped area is set by a base register, and boundaries are established at 4-kbyte intervals.

as a benchmark, the overall execution rates for instructions are 16% faster when compared with the Z80.

Another of the execution unit's features is its trap for erroneous op codes, which produces an interrupt whenever the CPU executes an undefined op code. Besides improving software reliability, it allows a designer to extend the chip's instruction set by using the undefined op code to generate a software interrupt.

Dynamic management

A bus controller that aids the processor in managing an extensive bus interface as well as refreshing a dynamic RAM array is also part of the CPU's core. Since 11 signals make up the interface, the CPU can work with wide range of peripherals. Specifically, the interface contains the control lines, like $\overline{RD}$ and $\overline{WR}$, needed to handle the peripheral chips for the 8080 and Z80, as well as the Enable line required for 6800 and 6500 peripherals.

Like other 8-bit CPUs, the processor automatically refreshes dynamic RAMs. But to reduce the power consumed by unnecessarily frequent refresh cycles—one every instruction cycle—a designer can program the RAM-refresh interval. Particularly, asynchronous RAM-refresh cycles can be separated by 10, 20, 40, or 80 clock cycles and can last either two or three clock cycles. Of course, for static RAMs, the automatic refresh function can be disabled.

A dozen instructions to go

Mnemonic	Action	Description
SLP	Sleep	Begin low-power operation
MLT	Multiply	Multiply 8-bit unsigned numbers for a 16-bit result
OUTO	Output	Send register contents to an immediate I/O address
INO	Input	Send immediate I/O address to register
OTIM	Block output	Increment or decrement memory address
OTIMR		Repeat above until counter is at zero
OTDM		Increment I/O address, decrement counter
OTDMR		Repeat above until counter is at zero
TSTIO	Logical AND test	Test I/O and immediate address
TST r		Test accumulator and register
TST m		Test accumulator and immediate address
TST (HL)		Test accumulator and memory

Another built-in feature, this one for handling slow I/O devices, is the automatic wait-state generator. It refines the chip's external Wait input (for extending bus cycles) by letting the user program a different number of wait-state cycles for I/O and memory operations.

The last subsystem of the CPU core is the interrupt controller, which manages interrupt requests from 12 different sources. Four of these are external inputs, including a nonmaskable interrupt ($\overline{NMI}$) and three prioritized interrupts $\overline{INT_0}$, $\overline{INT_1}$, and $\overline{INT_2}$. For these four, all programmable vectoring modes are hardware- and software-compatible with the Z80. The eight remaining interrupt requests are generated by the op-code trap and the chip's I/O subsystems.

I/O and away

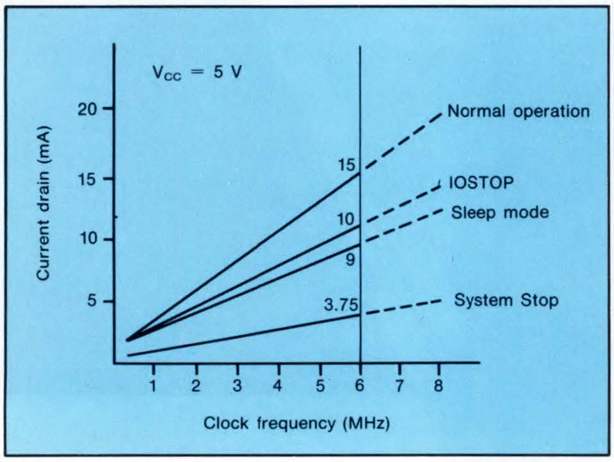
In addition to the power of its enhanced CPU core, the processor goes one step further by incorporating four integrated I/O subsystems. Included in it are a two-channel DMA controller, a two-channel, asynchronous serial communication interface (ASCI); a high speed, clocked serial I/O port (CSIO); and a two-channel programmable reloading timer.

The DMA controller eliminates the cost and complexity of having to use an external controller for rapid memory and I/O transfers. Moving data at up to 1 Mbyte/s (with a 6-MHz clock), the controller manages memory-to-memory, memory-to-I/O, and memory-to-memory-mapped I/O transfers across the full 512 kbytes of storage, as well as the 64-kbyte I/O address space. During block transfers, source and destination addresses can be incremented, decremented, or kept unchanged.

Requests for memory-to-memory transfers are handled automatically (without handshaking) using either the burst mode or cycle stealing. The first shifts data the fastest by suspending CPU activity; cycle stealing, on the other

hand, alternates data transfers and CPU cycles. For I/O DMA transfers, the processor supplies two handshaking signals: DMA Request (DREQ) and Transfer End (TEND). The second is sent to a peripheral to signal that the last byte of a DMA transfer is occurring. Finally, DREQ can be programmed for level or edge sensing.

For serial data transfers to RS-232-C peripherals, the processor turns to its two-channel, full-duplex serial interface, which includes two UARTs, a baud-rate generator, and modem control signals. Among each channel's independently programmable parameters are data length (7, 8, or 9 bits), number of stop bits (1 or 2), and parity bit (odd, even, or none). In addition, the interface detects errors in parity, data bits, and framing. The baud-rate generator makes possible rates of up to 38.4 kbits/s and uses an internal clock or an external source as its time base.



3. At a 6-MHz clock rate and 5-V dc supply, the processor draws 15 mA dc. However, the Sleep mode reduces the current drain to 9 mA, helping to conserve power for battery- and solar-powered applications. IOSTOP, by suspending all I/O functions, cuts current drain to 10 mA. System Stop suspends CPU functions as well, dropping current to 3.75 mA.

Of the two serial channels, channel 0 provides three modem control signals: Data Carrier Detect (DCD), Clear to Send (CTS), and Request to Send (RTS). Channel 1 furnishes only a Clear to Send handshake. One last feature of the serial interface makes it possible for it to address one CPU among several. This feature is a ninth data bit that can identify a serial word as an address to be checked by other CPUs on the bus.

Speedy serial

When the typical asynchronous serial interface is too slow, the processor delivers an alternative—a high-speed clocked serial I/O port. The port is ideal for multiprocessor systems because it supplies a fast communication channel between CPUs that does not tie up a system's bus. The serial port delivers half-duplex communication at up to 300 kbits/s (with a 6-MHz CPU clock) and employs three signal lines: Transmit Data (TXS), Receive Data (RXS), and Serial Clock (CKS).

The last member of the processor's I/O subsystem is a two-channel programmable reloading timer that handles the essential tasks of counting and timing. It can also be used to generate both simple and complex waveforms.

Each channel consists of a timer-data register and a reload-data register, both 16-bits wide. Whenever one of the internally clocked timer-data registers counts down to 0, it is reloaded with the contents of a reload-data register and, optionally, generates an interrupt request. Where a time-out interrupt is not appropriate, a designer can use a separate output signal that is available from one of the channels and is multiplexed with the MSB of the processor's address bus. The time-out (TOUT) signal can be set high, low, or toggled when the channel 1 timer overflows.

Overall, the microprocessor's low operating current and high level of integration suit it to industrial control. Designing the CPU into a system that uses all CMOS parts decreases the power dissipation, an approach that increases reliability and lends itself to hermetic sealing. Further, an all-CMOS strategy helps to reduce the system's size, weight, and cost.

Consider an industrial control system that takes advantage of the microprocessor's high

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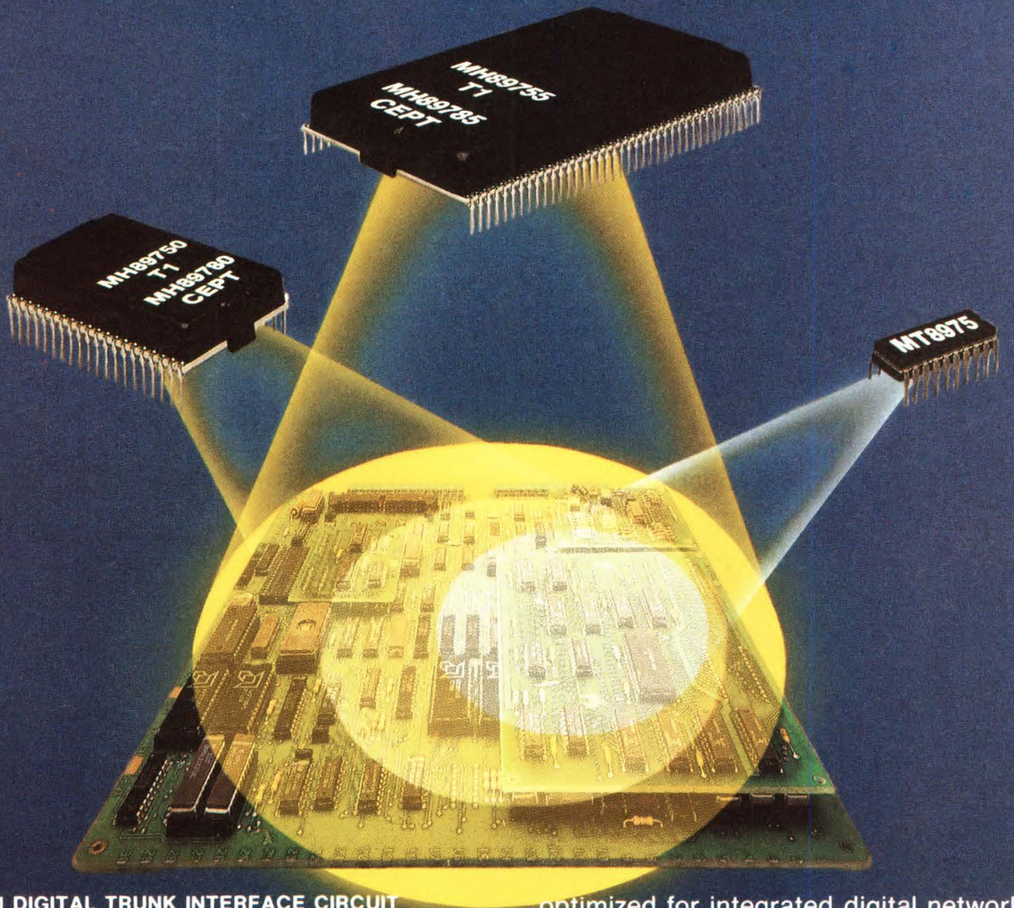

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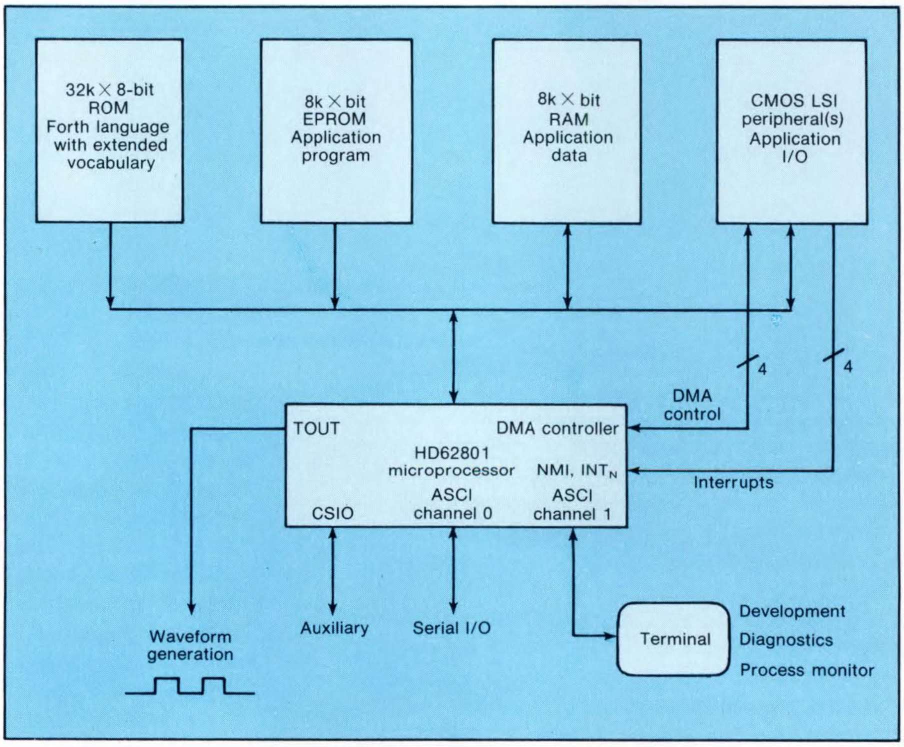
BUILDING BETTER COMMUNICATIONS WORLDWIDE speed, advanced architecture, and added instructions by incorporating its own Forth language translator (Fig. 4). Having Forth reside on the controller board simplifies program development, and the run-time package, application program, and data can each be stored in chips that fit standard JEDEC byte-wide memory sockets.

Using the byte-wide sockets makes it easy to change application programs and memory size. Further, the latest high-speed CMOS memories can hold a full version of Forth along with application-specific extensions for floating-point math, sorting, and peripheral control. As for the application program, an 8k-by-8-bit CMOS EPROM will hold one of substantial size: typically 400 to 500 lines of compiled code. Finally, 2k-, 8k- and 32k-by-8-bit CMOS RAMs can serve as needed for storing data.

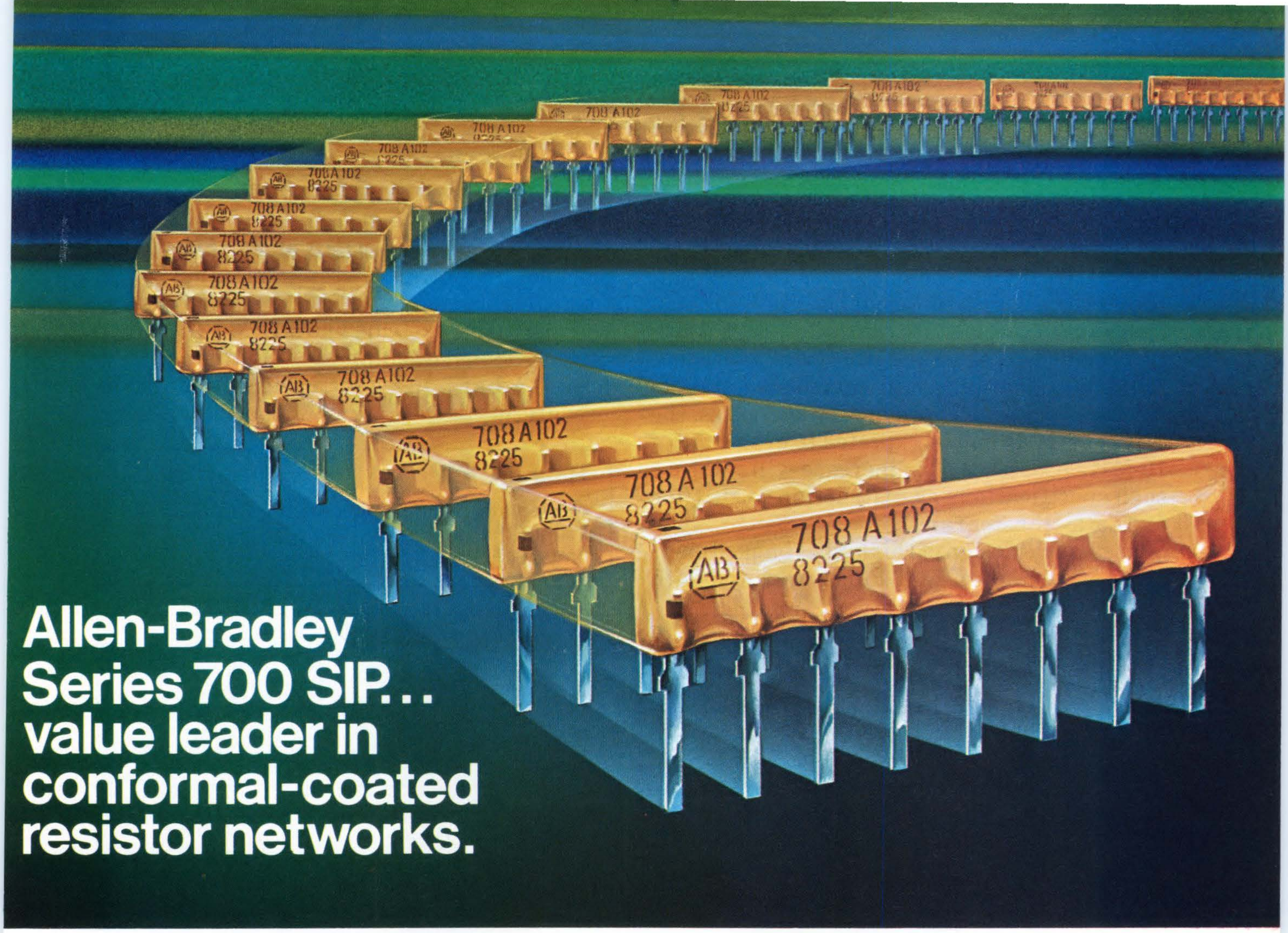
Easy to tailor

A wide variety of standard CMOS LSI devices are available to tailor the system to a specific need. Among these are parallel I/O interfaces, disk controllers, data converters, timers and counters, and telecommunications and graphics chips.

In desk-top or rack-mounted settings, where power consumption is not a consideration, the chip can run at full speed (Fig. 5). In such cases, standard NMOS 256k-by-1-bit dynamic RAMs that are automatically refreshed by the micro-



4. A Forth-language computer fabricated entirely in CMOS serves as an industrial controller with built-in development capability. A 32k-by-8-bit ROM holds the language itself; an 8k-by-8-bit EPROM stores the application program; and an 8k-by-8-bit RAM holds data. Using byte-wide memories ensures rapid matching of application requirements.



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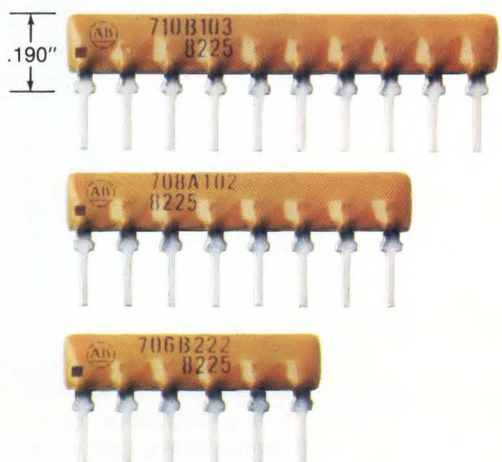

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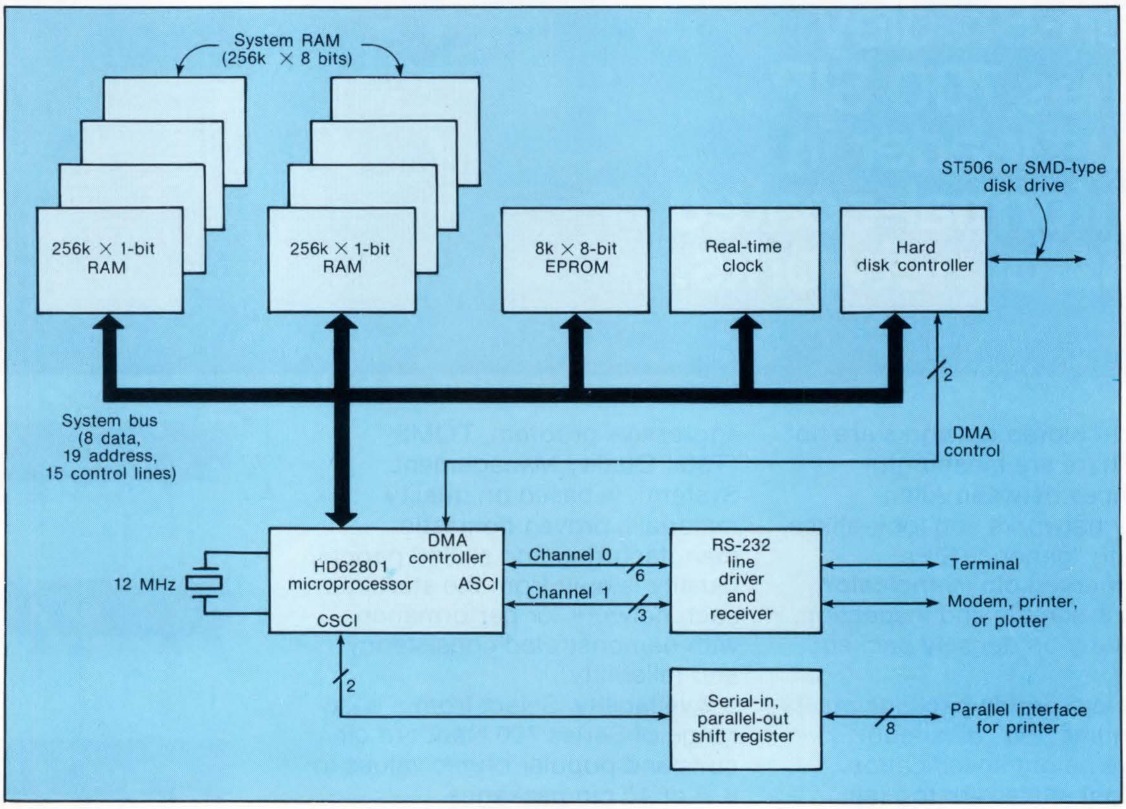
8-bit microprocessor

processor guarantee that the chip turns in its best performance. To maximize throughput, the memory access time could be fine-tuned using the chip's wait-state controller. Such a system could also use a 12-MHz crystal to produce a 6-MHz system and a minimum instruction cycle of 500 ns. And as production increases, the current 6-MHz chip is expected to evolve into a 10-MHz processor. The increase will improve such specifications as instruction-cycle time and data-transfer rate.

In a typical design of this kind, a banked operating system like CP/M-Plus works well with the chip's schemes for DMA and memory management. In fact, a low-cost system that serves four to eight users could be devised using multiuser operating systems like MP/M II, Oasis, or TurboDOS and by adding a UART for each terminal. A hard disk controller would also be needed.□

How useful?	**Circle**
Immediate design application	544
Within the next year	545
Not applicable	546



5. In a desktop or rack-mounted setting, the microprocessor, standard NMOS 256k-by-1-bit dynamic RAMs, and a banked operating system form the foundation of a small high-performance computer. The 6-MHz clock yields a minimum instruction cycle of 500 ns. To serve multiple users a UART can be added for each extra terminal.

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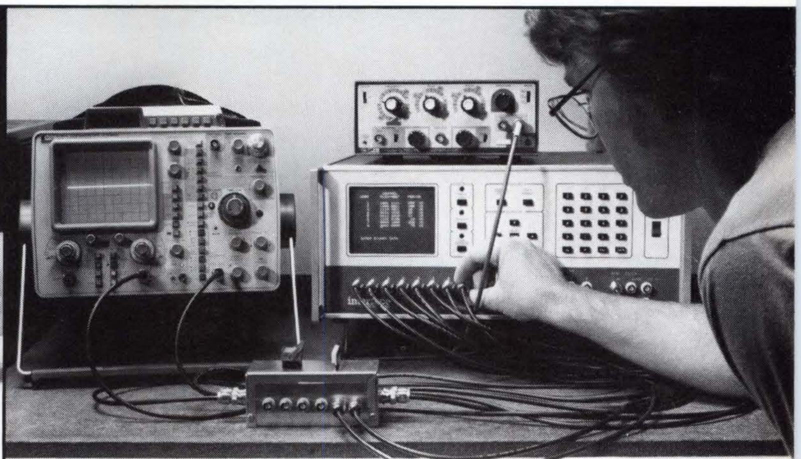

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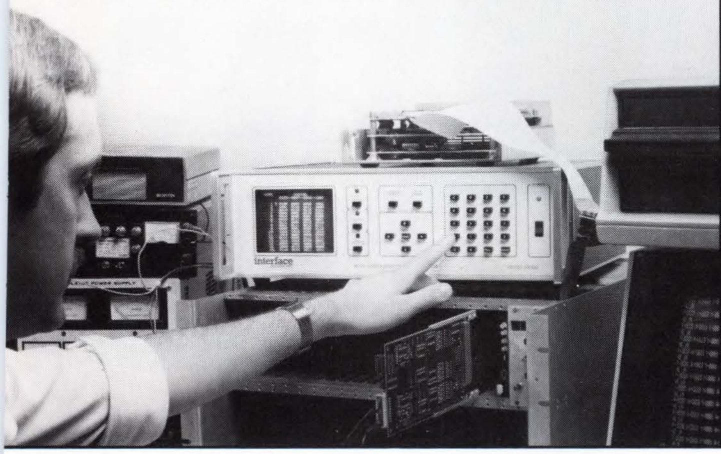
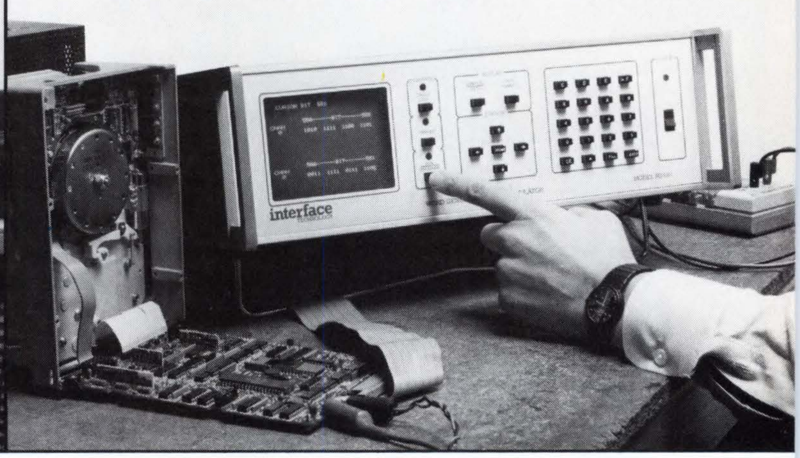


DWGs eliminate building dedicated circuitry.



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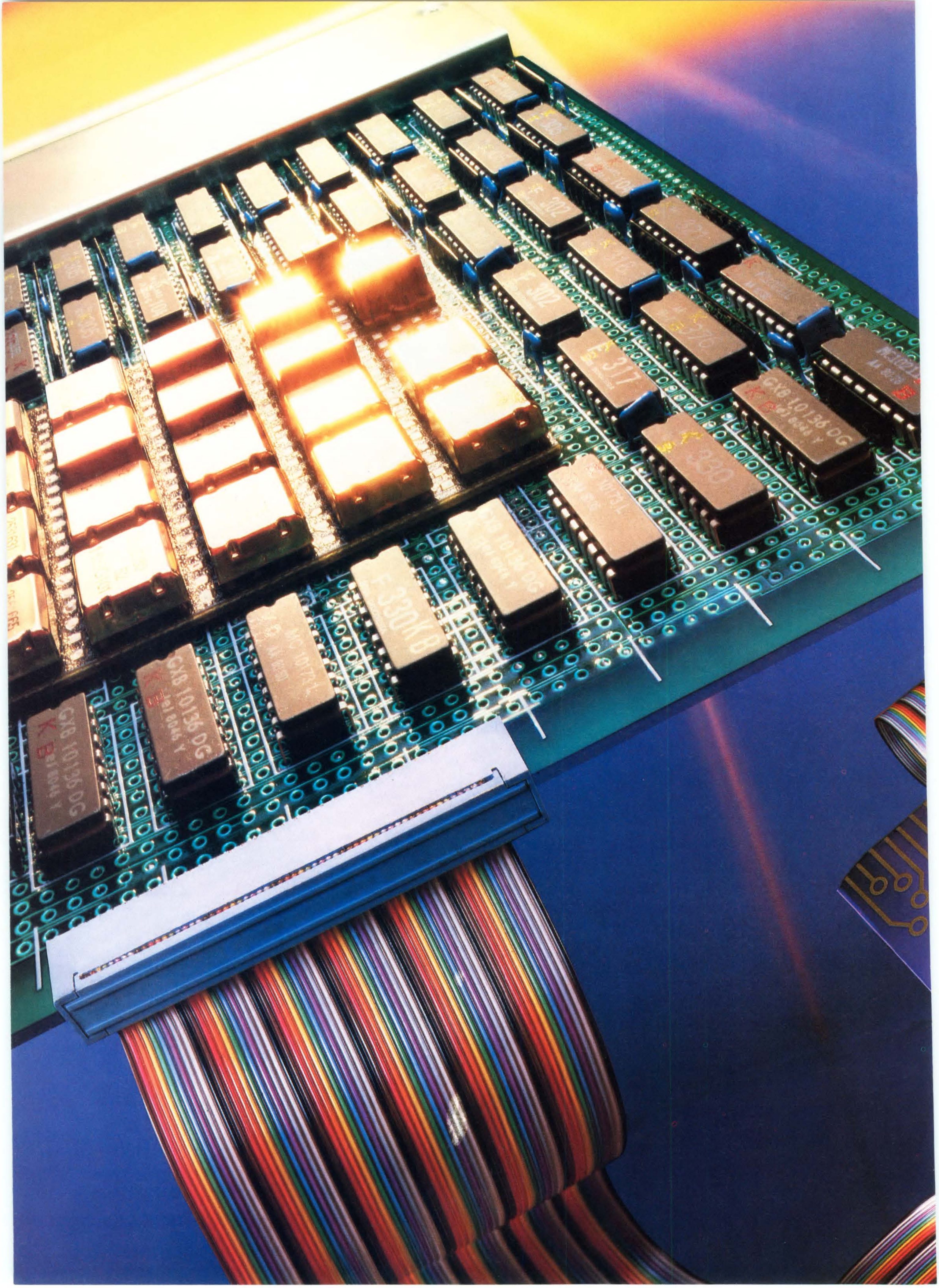
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CIRCLE 130

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Microprogram sequencer handles a system's interrupts in real time

Having a 100-ns cycle time and a range of functions, a control IC itself makes use of microcode to sequence microprograms for microprogrammable systems.

By offloading the host processor, an intelligent controller boosts the performance of many microcomputer-based systems. A microprogram sequencer, in turn, helps controllers of microprogrammable systems, especially when it also handles interrupts.

The Am29112 interruptible microprogram sequencer goes one step further by dealing with interrupts in real time. It can do this because it accepts them at the boundary of any microinstruction, instead of only at the boundaries of a select few. Further, built-in hardware handles these interrupts and thus contributes to the chip's real-time response to them.

The sequencer is an 8-bit-slice building block capable of controlling up to 64 kbytes of microprogram memory and thereby tailoring a microprogrammable system to specific applications. Indeed, the device's own instruction set and architecture reflect the same trend toward microprogrammability. The microcoded instruction set has direct counterparts for virtually every sequence-controlling statement found in high-level languages, thereby easing the compiling of such a language into microcode (see "Microcode Supports Statements in High-Level Computer Language," p. 320.) Built-in hardware makes possible parallel processing at the microprogram level. As a result, microprograms can be economically developed as small, relocatable subprograms (modules) each of which can be written and debugged independently.

To keep pace with arithmetic and logic units and other high-speed components, the microprogram sequencer has a cycle time of 100 ns. A controller designed with this sequencer frees the host for other tasks by performing complex arithmetic and logic operations on data and supporting algorithms. Moreover, since systems spend much of their time transferring information between the main memory, secondary memories, and display devices, maintaining data integrity can be a problem. The sequencer not only monitors for data consistency but also diagnoses faults in its own circuitry.

The sequencer's program counter—actually a register—and its incrementer, address multiplexer, counter, and stack are all borrowed from earlier designs (Fig. 1). The stack, however, has a full 33 levels to handle deep nesting

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Microprogram sequencer

of subroutines and interrupts. The new components are an adder for relative addressing, a register for controlling offset width, interrupt control logic, and an interrupt address register for unmaskable interrupts.

The 8-bit-slice sequencer has an address path that is 8 bits wide. Further, two devices can be cascaded to form a 16-bit-wide address path. A single-slice sequencer addresses up to 256 words of microprogram memory, but a double-slice sequencer having a 16-bit-wide address path addresses up to 65,536 words. This is enough to handle most applications. For example, a microprogram that interprets machine-level instructions typically has on the order of 1,024 words, while a microprogram that is the controller's only program usually is larger.

Some bit-slice devices can be cascaded to any word length. However, the Am29112 cannot be expanded beyond two slices. In a two-slice implementation, one is designated by an input as the least significant slice (LSS) and the other as the most significant slice (MSS). Thus a signal that propagates from the LSS to the MSS needs just one pin on each slice—an output on the LSS and an input on the MSS. Four signals on the sequencer pass between the slices. These are the carries for the program counter (PCIO), the counter (CIO), the adder (ACIO), and the zero detect (CZIO).

The Am29112 is one of the few sequencers that support interrupts at the microprogram

Microcode supports statements in high-level computer languages

Structured programming is an important tool at the microprogram level, where poor programming techniques lead to unreadable and error-filled code. The Am29112 sequencer supports structured microprogramming by providing commands that, taken together, correspond to the sequence control statements of high-level languages.

Branches and procedure calls in high-level languages have their equivalents in the sequencer's jump and jump-to subroutine instructions. More interesting are the various types of loops. The Pascal REPEAT loop, for example, is supported by two sequencer instructions:

```
REPEAT              Push PC
  .                   .
  .                   .
  .                 ., Test End Loop(condition)
UNTIL (condition)
```

The address of the loop body is pushed onto the stack at the beginning of the loop. Thus there is no loop body-label to deal with, and the branch-address field can be shared. This also applies to other instructions. The WHILE loop, for example, can be implemented with three instructions:

```
                        Push PC
WHILE condition DO      Conditional Jump
                        D and Pop (condition)
  .                       .
  .                       .
  .                     ., Test End Loop (fail)
END WHILE               D:
```

This approach, one of several, is an infinite loop with a conditional exit just before the loop body. The last instruction jumps unconditionally to the instruction that tests the condition.

A FOR loop can be implemented with two instructions using the sequencer's built-in counter:

```
FOR I: = 1 to N DO  Push PC and load L/U
                    Counter, N−1
  .                   .
  .                   .
  .                 ., Repeat Loop, L/U
                    counter
END FOR
```

A conditional branch must be provided for this microcode if N can be less than 1—a microcoded loop cannot iterate zero times.

The CASE statement relies on the multiway jump to perform the selection. Normally a jump to the end of the CASE statement is inserted after each case selection except the last. Alternatively the address of the end of the CASE statement can be pushed onto the stack just before the multiway jump and a return instruction inserted after each case selection. In this way the branch-address field is used just once, making possible more field sharing. The implementation is:

```
                    Push D
CASE N OF           Jump Multiway A
0:  .               A:     ., Return
1:  .               A+1:   ., Return
2:  .               A+2:   ., Return
3:  .               A+3:   ., Return
END CASE            D:
```

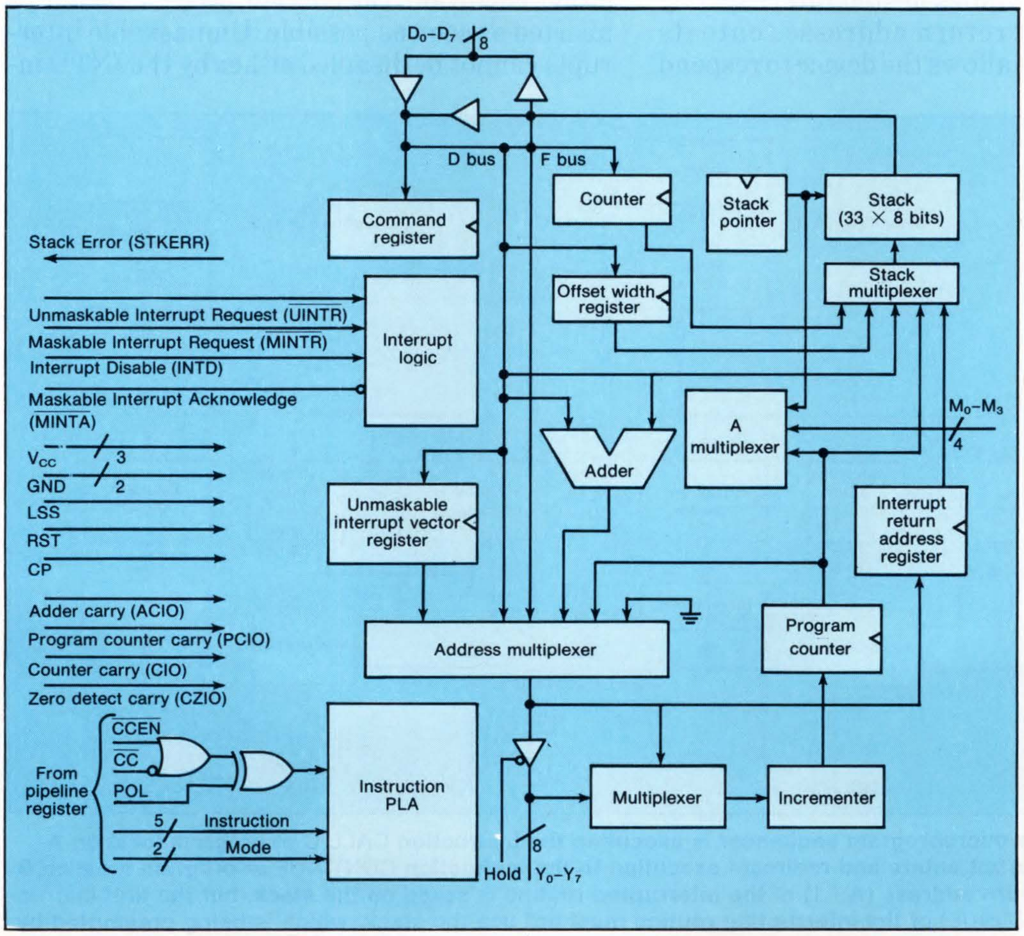
level. In comparison to polling, interrupt capability improves throughput, reduces response time significantly, and ensures more effective coding. With polling, on the other hand, the microprogram must test explicitly for interrupts at certain points. This not only produces a slower microprogram with longer response times, but it also requires more effort on the part of the programmer.

Handling interrupts expeditiously

In a microprogrammed system using the Am29112, it takes two or three cycles from the time the interrupt request is received to the execution of the first instruction in the interrupt routine. The instruction appears at the output of the sequencer's associated pipeline register. Because the chip's cycle time is just 100 ns, interrupt response times are on the order of 200 to 300 ns.

An interrupt is transparent to the interrupted microprogram, which temporarily stops running. The device handles both maskable and unmaskable interrupts (an unmaskable interrupt being used when no action can be taken to reverse the situation). An incoming interrupt turns off the Y-bus driver and loads an external interrupt address onto the Y bus (Fig. 2). The interrupt also causes the interrupt return address to be saved on the stack.

A delay of one cycle occurs between the Interrupt Request and Interrupt Acknowledge



1. The Am29112 interruptible microprogram sequencer chip is a mixture of conventional and new logic functions. To improve its ability to handle interrupts, the chip carries enhanced interrupt logic and a very deep stack—33 levels—that allows nesting of interrupts and subroutines.

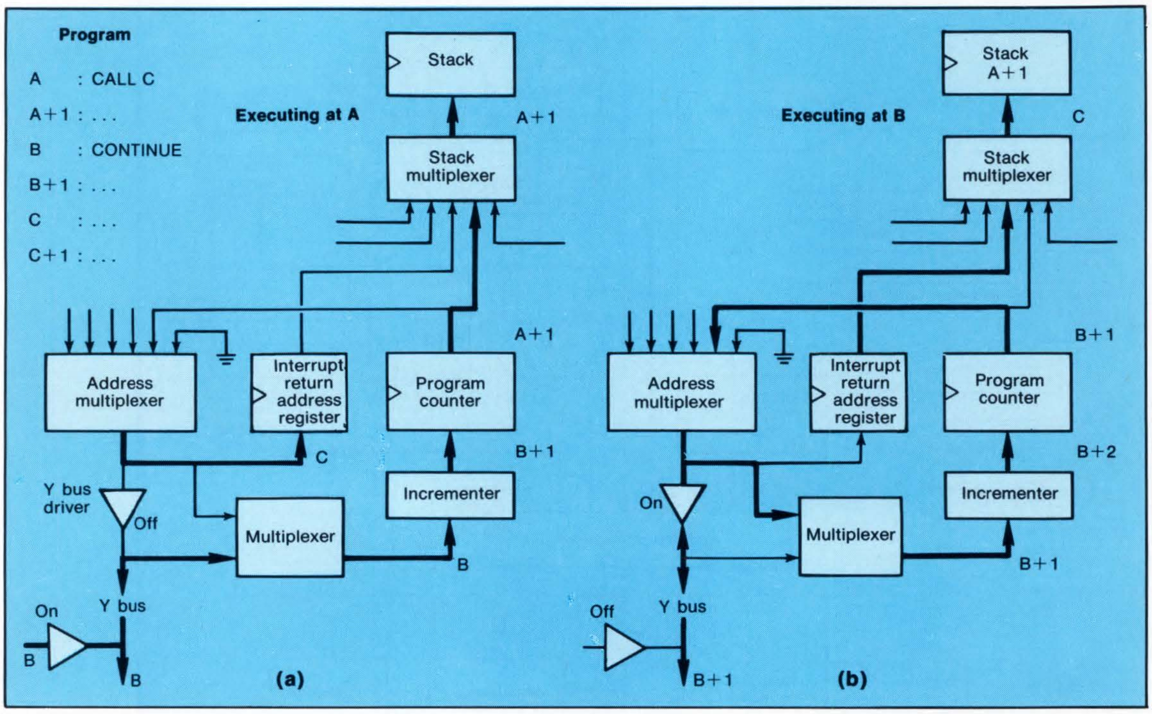
signals. An optional delay of one cycle can be inserted between the Interrupt Acknowledge signal and the actual interrupt. The delay is controlled by a so-called post-delay mode bit in the command register, and it is useful if the external device needs more time to load the interrupt address onto the sequencer's Y bus.

The interrupts can be controlled either by an interrupt disable (INTD) pin or by the sequencer's instructions. When the INTD pin is high, interrupts are disabled immediately and remain disabled for as long as the pin remains high. When the sequencer's instructions are used, interrupts are also disabled immediately and stay disabled until the enable instruction is executed.

The sequencer handles nested interrupts by pushing interrupt return addresses onto its internal stack. This allows the device to respond to a more urgent interrupt while it is servicing another one.

To service an interrupt, enough stack levels must be available when the interrupt occurs. A bit in the command register permits the delaying of interrupts if five or fewer stack levels remain unused. In addition, an instruction may be inserted at the beginning of an interrupt routine to test whether enough stack levels are available to service the interrupt when it occurs.

Unmaskable interrupts are quite different from the conventional type. They can be triggered by a system power failure or a loss of system integrity, such as a stack overflow in the sequencer. Since it is impossible to recover from either condition, the current process should be aborted as soon as possible. Unmaskable interrupts cannot be disabled either by the INTD in-



2. While the microprogram sequencer is executing the instruction CALL C **at program location A (a), an interrupt enters and redirects execution to the instruction** CONTINUE **at program location B (b). The return address (A+1) of the interrupted routine is saved on the stack, but the first instruction** (B:CONTINUE) **of the interrupting routine must not use the stack, which is being preempted by the return address already pushed onto it.**

put or by the interrupt-disable flip-flop. The routine for an unmaskable interrupt does not save the interrupt return address but instead may try to restart the system. A register in the sequencer can be loaded with the unmaskable interrupt address.

Parallelism for multiple tasks

Parallel processing is a useful option in programming, and the microprogram sequencer extends it to the microprogram level. In one approach to parallelism, a single processor is time-multiplexed among a number of tasks. In the diametrically opposite approach, there must be at least as many processors as there are tasks running in parallel.

The first approach costs the least. Each time a task is suspended, however, its state must be saved to allow it to be restored when its execution resumes. With the second approach, there is no save-and-restore overhead; it offers the fastest response time and the best performance.

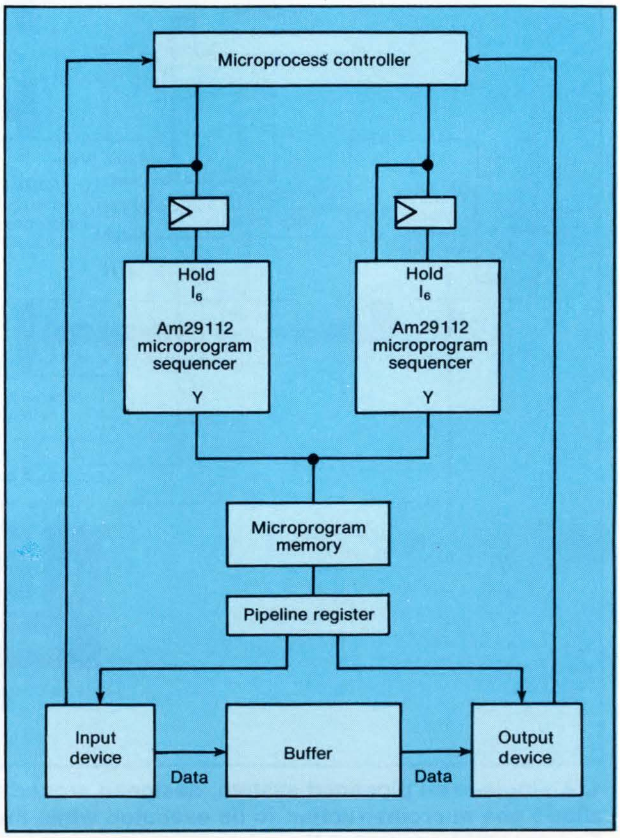
The sequencer supports the first method by saving and restoring virtually its entire state through the bidirectional data bus, or D bus. (Only the contents of the command register and unmaskable interrupt address register cannot be saved, but this is not usually a problem, since the contents are likely to be the same for all processes.) Moreover, the Am29112 is one of the few sequencers to be able to push data onto and pop it from the stack by means of its D bus.

All registers can be loaded through the bus, and the contents of most can be pushed onto the stack. Thus almost the entire stack and most of the registers are accessible from outside the chip. This is helpful not only in testing the sequencer, but also in debugging, where the contents of the counter and stack can be observed and altered. It is convenient to include the debugger in microcode in the prototype stage; this helps the sequencer debug both itself and the rest of the system.

The second parallel processing approach—a separate processor for each task—is supported by the Am29112's multiple single- or double-slice sequencer arrangement, with its unique Hold and Force Continue features. In this arrangement, two or more sequencers' Y buses are tied together and drive a single microprogram memory. One sequencer is active, and the others are put on hold. A sequencer is active when the Hold input and (one cycle later) the Force Continue input are activated.

The Hold turns off the Y bus and disables the incrementer, thus saving in the program counter the address that does not make it into the microprogram memory. The Force Continue mode prevents the sequencer from responding to an instruction intended for another sequencer. Interrupts must not occur when Hold is asserted.

In typical microprograms, most microinstructions perform an operation and continue to the microinstruction at the next sequential address. Thus the microcode field of the sequencer instruction often contains a continue instruction. This field can be better used if it is shared between the sequencer instruction and



3. Two AM29112s can process in parallel through a buffer. In such a system, one sequencer is active, while the second is on hold. Time multiplexing enables one sequencer to handle input operations; the other is responsible for outputs.

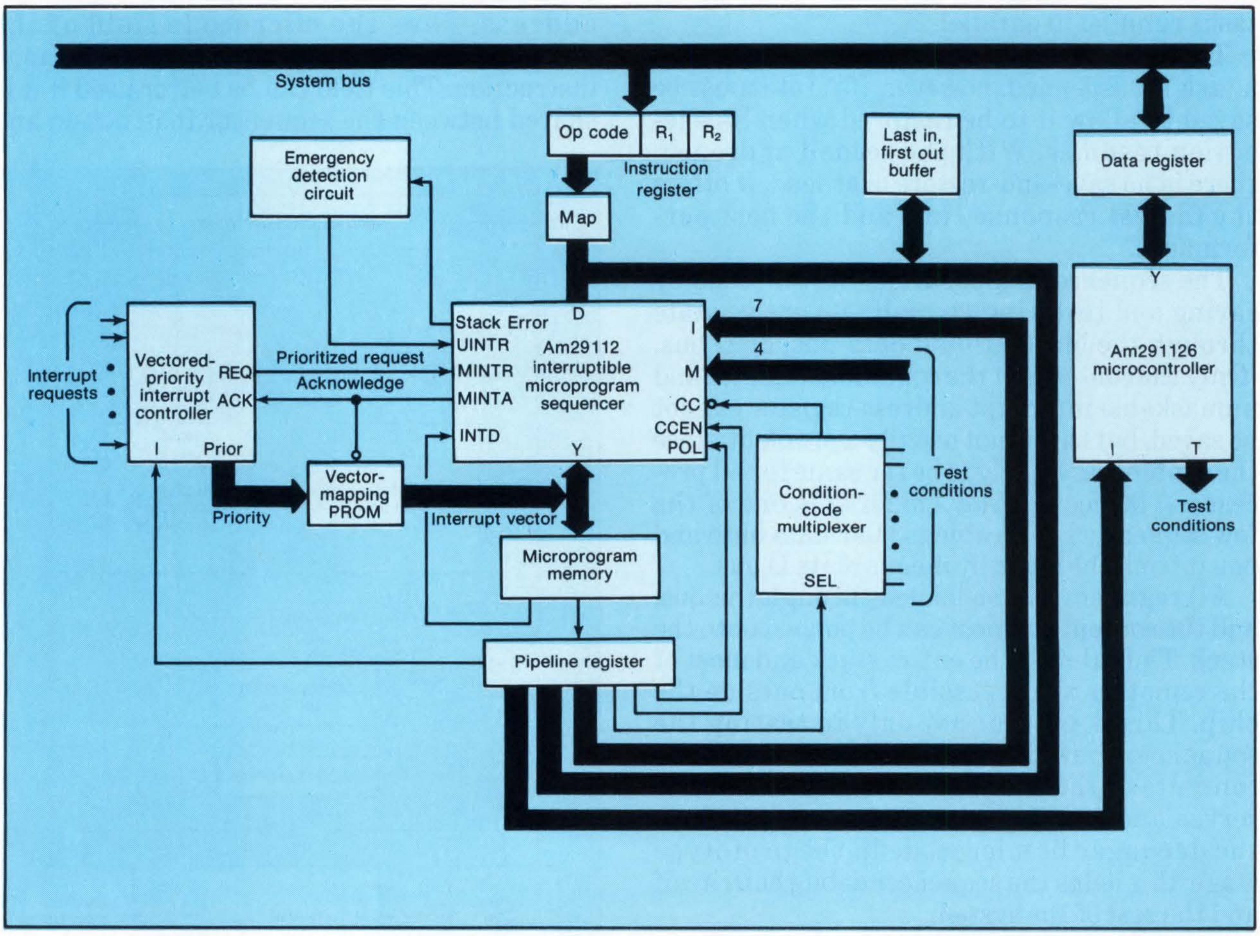
Microprogram sequencer

another device that need not be controlled on every cycle.

An extra bit in each microinstruction is needed to indicate whether the shared field controls the sequencer or the other device, and each must be able to disregard the data intended for the other. The Am29112 is the first sequencer with the ability to override the instruction lines with a Force Continue instruction (on pin I_6).

Multiple sequencers must execute different microprograms, but they execute the same program after reset and until they branch in different directions. This branching is done with a so-called multiway jump, if the multiway inputs of each sequencer are wired to different 4-bit combinations. Each sequencer jumps to a unique and predetermined location, but the sequencers can still share subroutines.

Communication between two asynchronous devices requires a buffer in their data path to smooth out differences in data rates. In a typical arrangement (Fig. 3), the two sequencers would run an input process between an input device and a buffer and an output process between the buffer and output device. Time-multiplexing the processes ensures that the buffer need handle only a single access at a time. The microprocess controller puts one



4. A single-level pipelined system, designed around the Am29112 and the Am29116 16-bit microcontroller, allows one microinstruction to be executed while the next instruction's address is generated and accessed. The Am20112 generates the microprogram memory addresses for the next microprogram to be executed.

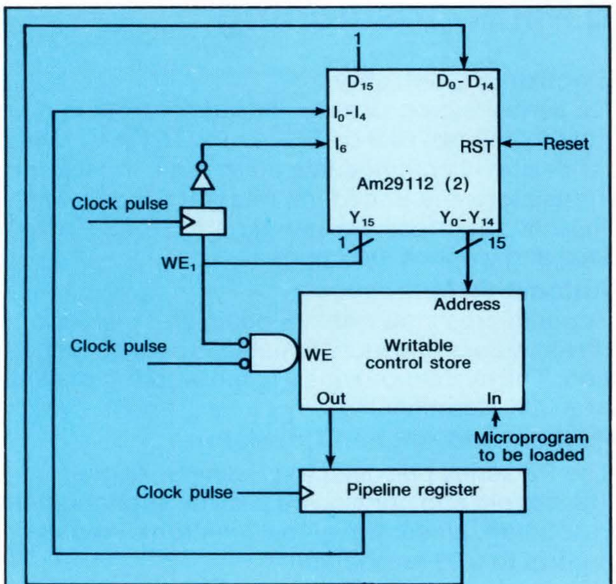
Microprogram sequencer

sequencer on hold, while the other is active. Status information flows to the controller from both sequencers.

The sequencer selects addresses for the microprogram memory on the basis of instructions, conditions, addresses, multiway inputs, and interrupt requests. The six types of sequence control are called continuation, absolute branching, program counter relative branching, multiway branching by substitution, multiway branching relative to an absolute address, and branching to the address on top of the stack.

The outcome of a conditional instruction is determined by a final condition. This is a function of the Condition Code (CC), the Condition Code Enable (CCEN), and the Polarity Control (POL) signals. Selecting proper values for CCEN and POL sets the final condition equal to the incoming Condition Code, its complement, always true (pass) or always false (fail).

A high-performance microprogrammed system can be designed with the sequencer at the heart of the control section. The system (Fig. 4) has a single-level, pipelined architecture. This permits simultaneous execution of a microinstruction, determination of the next microinstruction's address, and accessing of the address from the microprogram memory. Such an architecture inflicts no penalty for branching, an important requirement in high-performance controllers. A jump to a branch address can occur immediately in the next cycle, after the condition and new branch address are presented to the sequencer.



5. Using its Force Continue mode on pin I_6, the sequencer generates sequential addresses for a writable control store. That permits data to be written into the store faster.

A typical system in operation

The host processor initiates a task by loading a high-level customized instruction into the external instruction register. As soon as the instruction is loaded, a starting address is extracted for a specific microprogram. This microprogram performs a specific task, and after the task is completed, another instruction is loaded into the instruction register.

The starting address of the microprogram is passed through the sequencer to the microprogram memory. The first microinstruction to be executed is accessed from memory, and on the next rising edge of the clock pulse, it is loaded into the microinstruction register in the controller. When so loaded, a microinstruction performs two basic tasks: It decodes the address of the next microinstruction to be executed, and it carries out the operation on the data specified by the high-level instruction.

As the heart of the microprogram control logic, the sequencer generates addresses for the next microprogram to be executed. The decision to generate the next address depends on the instruction that the sequencer receives from two sources: the microinstruction being executed and the Condition Code input.

Branch addresses, constants for various registers, and stack pointer values are applied to the sequencer through its D port. This is a bidirectional port, to allow the stack to be unloaded into an external LIFO (last-in, first-out) structure to support task switching at the microprogram level.

To handle real-time interrupts, the Maskable Interrupt Request (MINTR) and Acknowledge (MINTA) signals are sent to the vectored priority interrupt controller. The sequencer checks

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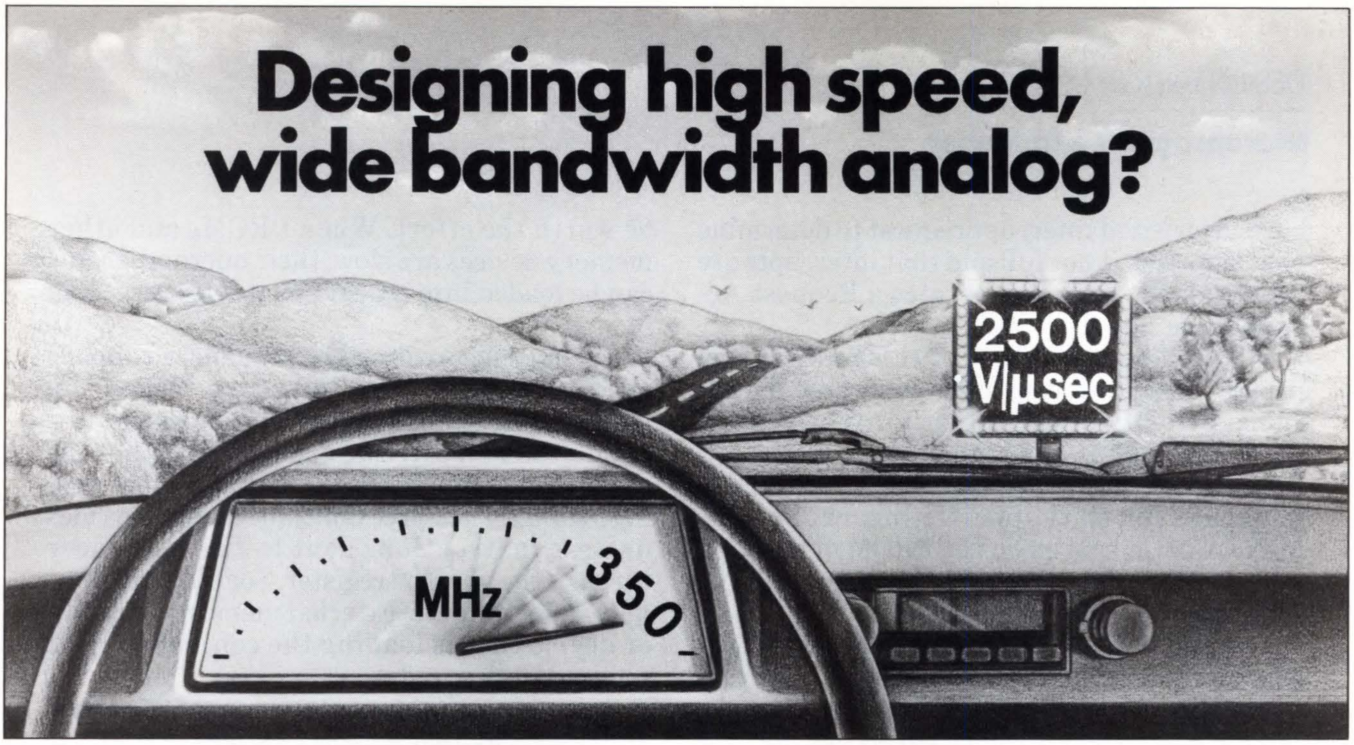

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each prioritized interrupt request to determine that the stack is not full and that interrupts are not disabled. Then it generates a Request Acknowledge signal.

With acknowledgment of this request, the priority-interrupt controller generates the encoded priority of the interrupt. The vector-mapping PROM then translates this encoded vector into the starting address of the microprogram for that specific interrupt. The MINTA output turns on the PROM output and simultaneously turns off the output of the sequencer's bidirectional Y port.

The starting address for the interrupt routine now goes onto the microprogram address bus. From there it is given simultaneously to the microprogram memory (to access the first microinstruction in the interrupt routine) and to the sequencer through its Y port (for incrementing to form the address of the next microinstruction to be executed in sequence).

At this point, the system's condition-code multiplexer selects one of the conditions present at its inputs. It then provides the result of the arithmetic or logic operation—greater than or equal to, and so forth—to the sequencer to help make a branching decision.

(Incidentally, the multiway inputs provide a powerful primitive to implement table lookups. Such inputs can be either concatenated or added to the branch address provided through the D port. The second approach allows lookup tables to be relocated without address calculations.)

The system's circuit for detecting emergencies generates an unmaskable interrupt request on a power failure or stack error. Upon receiving such a request, the sequencer branches to the unmaskable interrupt routine. The starting address of the routine is stored in the interrupt vector (INTVECT) register at system initialization.

Compensating for slow PROMs

In some cases a microprogram is not fixed, but must be written into a writable control store before execution. This permits a system to run different programs, including comprehensive diagnostic routines.

A writable control store is built with RAM chips. Even for just a single program, this can be worth the effort. When PROMs and other memory devices are slow, their microprograms can be loaded into a faster writable store (Fig. 5).

During such loading the sequencer supplies addresses to the control store. When the Am29112 runs in the Force Continue mode, it—rather than an external counter—supplies the sequential addresses to the writable store during loading. The Force Continue mode overrides useless instructions sent to the sequencer through the pipeline register. Such instructions may come from the external memory or another device that is loading the control store at reduced clock speed.

Assume a writable control store of 2^{15} words, addressed by two Am29112 slices. First, the sequencer is reset to address 0, and writing starts. The Force Continue mode starts one cycle later, and writing continues until the word at address $2^{15}-1$ has been written.

Force Continue is disabled one cycle later, at the time that the first valid instruction appears at the output of the pipeline register. The sequence is as follows:

Y_0-Y_{14}	RST	I_6	WE_1	Y_{15}
0	1	X	1	0
1	0	1	1	0
.	.	.	.	.
.	.	.	.	.
$2^{15}-1$	0	1	1	0
0	0	1	0	1
X	0	0	0	1

The address after $2^{15}-1$ is 0 because of wraparound. Signal Y_{15}, which is available because the full address space is not used, indicates completion. If Y_{15} can be guaranteed to be a 1 after completion, it can control WE directly and I_6 through a flip-flop. But this requires that D_{15} also be a 1. The write pulse to the writable control store must have a stable address and WE signal. The write pulse can be the low period of the clock. □

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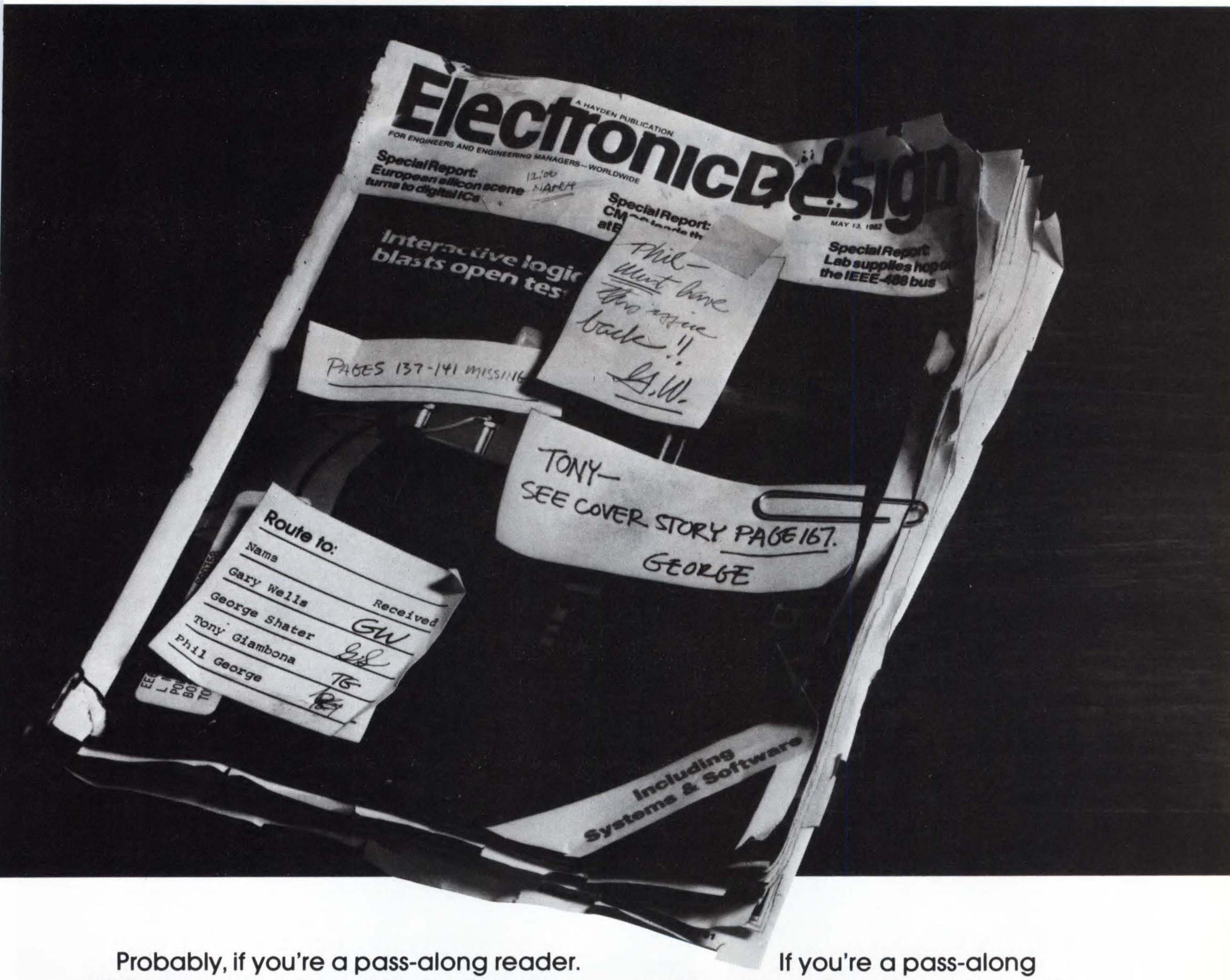

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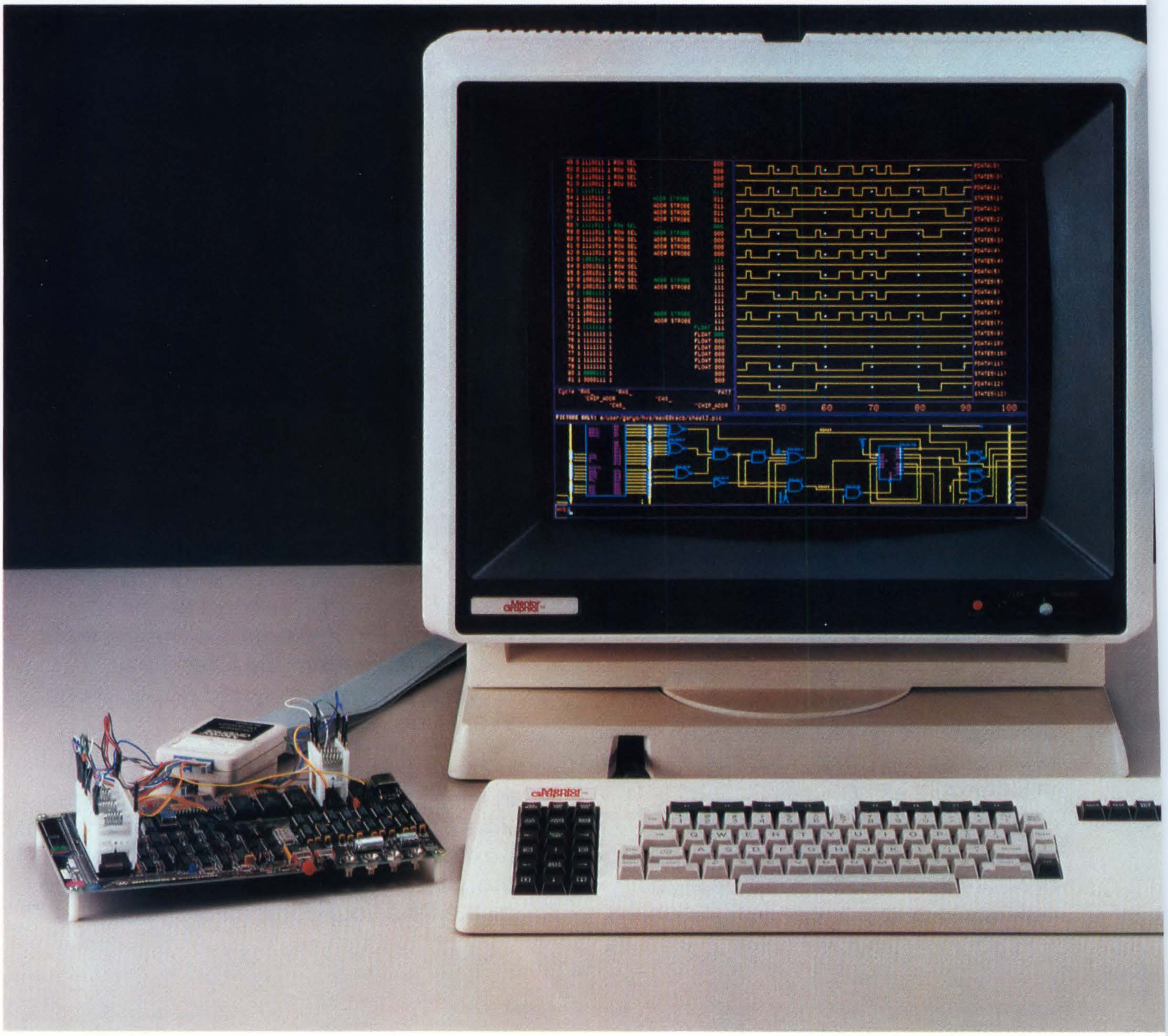

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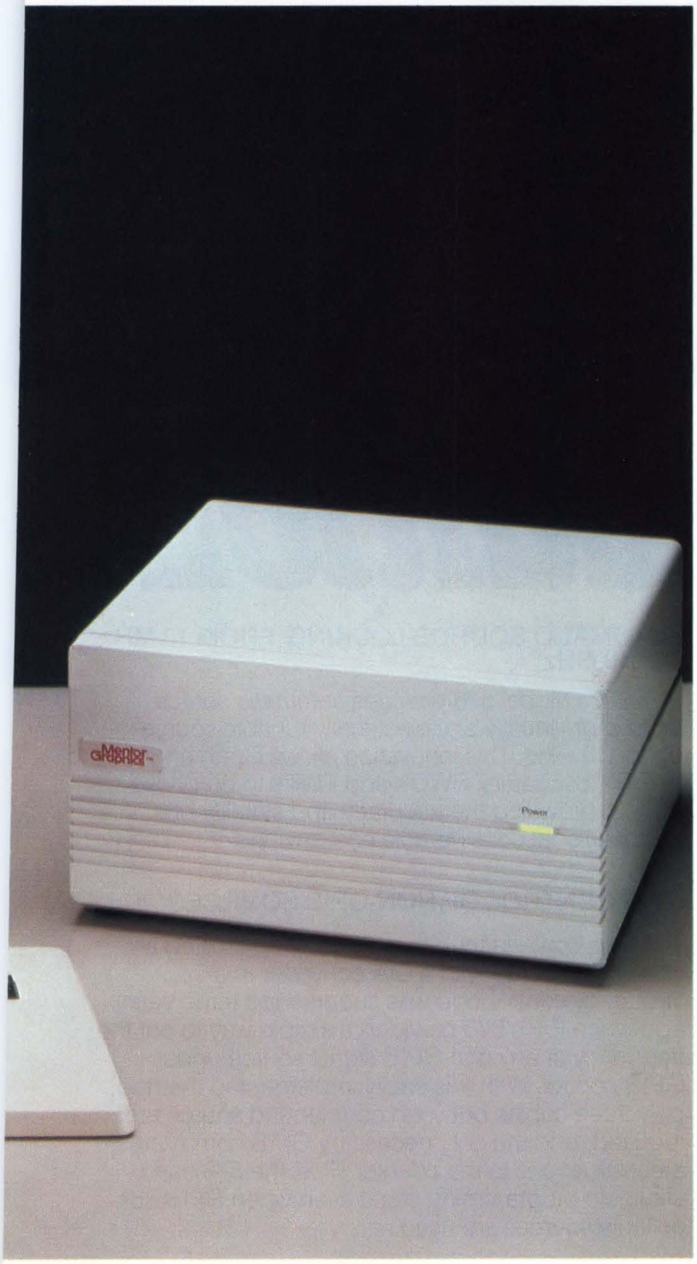

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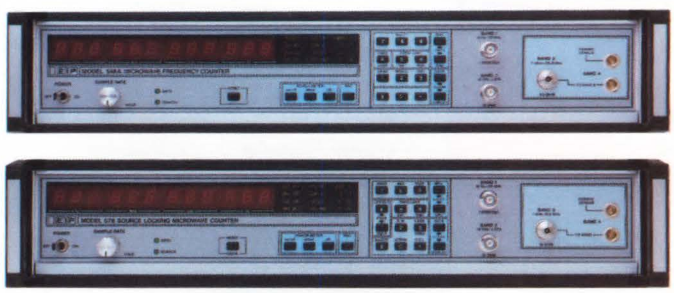

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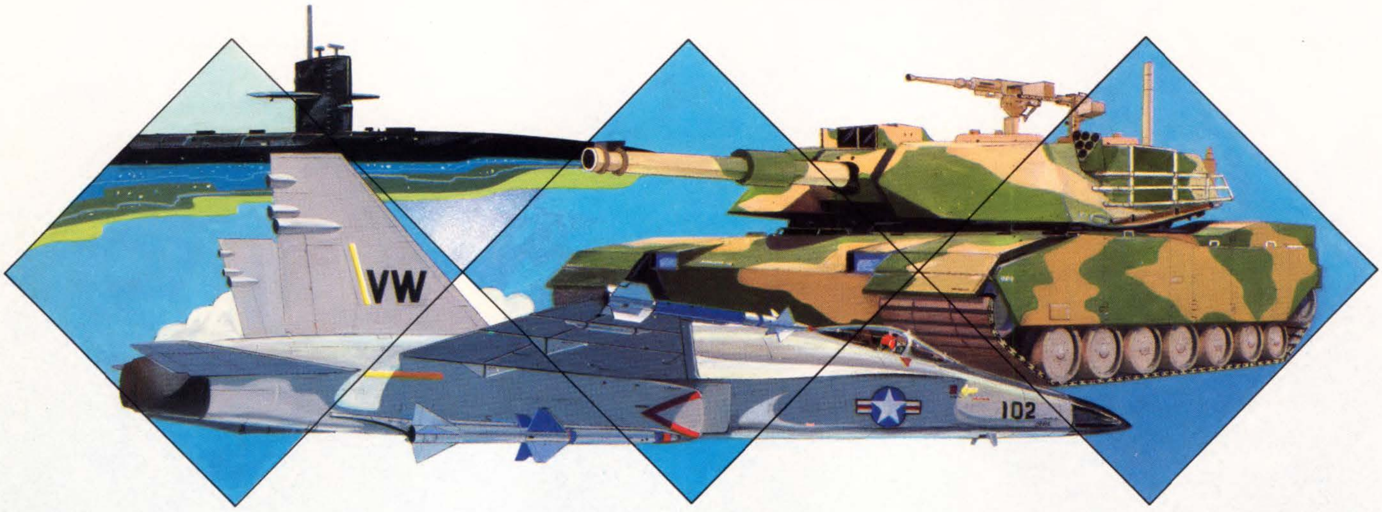

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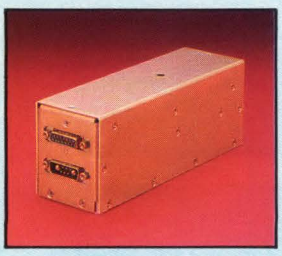

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5/12/15/24/28 VDC @
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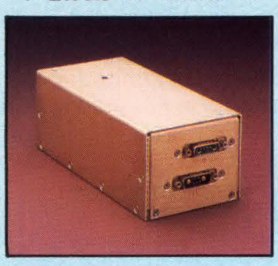
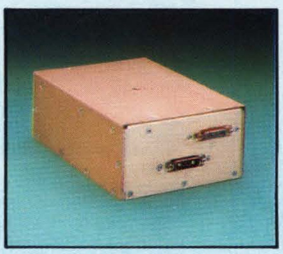
7"L x 3.5"W x 2.625"H





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180W Dual
±12/15/24/28 VDC @
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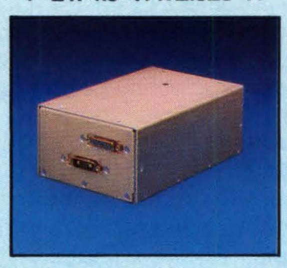

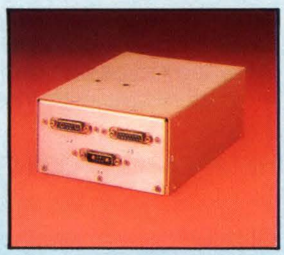

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DESIGN ENTRY

The 32-bit 68020's power flows fully through a versatile interface

A system interface may hold back a processor's power, but the 68020 goes to extra lengths to optimize its link to other chips.

This article, the first in a series on the MC68020 32-bit microprocessor, explores the chip's versatile system interface. Future topics will cover the processor's dynamic bus sizing feature, its overall performance characteristics, its support chips, and one approach to system prototyping.

Practically speaking, any microprocessor, no matter how powerful, is only as good as the bridge to the system it serves. The designer's job is to build that bridge, making the most of the processor's address, data, and control buses—essentially, the memory and I/O interface. Knowing the details of a microprocessor's interface allows designers to anticipate how factors like memory access time will ultimately affect performance.

Familiarity with the buses is no less important for heavyweight contenders like the 32-bit MC68020 than it is for popular 8- and 16-bit devices. Besides its impressive advantage in processing muscle, the 68020 chip simplifies the task of designing a system bridge: Its 32-bit-wide address and data buses afford the fastest operation for memories and other peripherals that can manage 32 bits (a "long word") at one time (Fig. 1). And if properly done, even when hooking up 8- and 16-bit peripheral interfaces, the microprocessor sacrifices nothing in performance. A unique mechanism called dynamic bus sizing automates and simplifies data transfers. Through a system of handshakes, it determines different bus widths and adjusts the number of bus cycles accordingly. A further refinement of dynamic bus sizing automatically compensates for operand misalignment—a condition that occurs when 16- or 32-bit-wide operands do not fall on standard word and wide-word boundaries in memory. Because the processor adapts instantly to bus width, a designer can plan memory and peripheral buses for the best trade-off between speed and simplicity.

Finally, real-time I/O transfers can benefit from the microprocessor's interrupt mechanism. The chip accepts seven priorities of vectored interrupt requests, taking fom the data bus an 8-bit vector number that points to a table of 32-bit addresses, one for each of 256 interrupt service routines. Alternatively, in the autovector mode, the microprocessor assigns the vector number on the basis of the interrupt's

David McCartney and **Paul Groepler**
Motorola Inc.

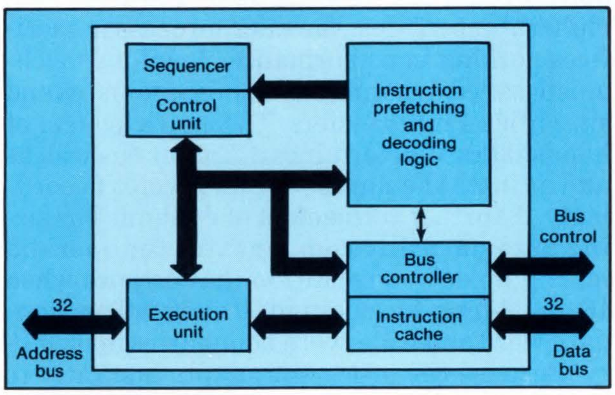
Since 1980 David McCartney has been an application engineer for the MC68000 family, currently serving as section manager for Motorola's European Product Marketing Organization in East Kilbride, Scotland. He holds a PhD in electrical and electronic engineering from Glasgow's University of Strathclyde.

Previously with Motorola's high-end applications group in Austin, Texas, Paul Groepler is now a designer of the company's graphics systems. He is a member of the Association for Computing Machinery and its special-interest group, Siggraph. Groepler has a BS in computer science from Texas A&M University.

priority. With two sources available for each interrupt, a little extra logic boosts to 14 the number of total possible interrupt sources.

Certainly, executing 32-bit instructions and operands at high speed is at the heart of the 68020's advantage over earlier members of the series, giving it four or five times the power of a 68000. For instance, bus read and write operations that take four clock cycles in the 68000 occur in just three clock cycles in the new processor.

To maximize the 32-bit chip's superiority, system designers should use components that allow the bus cycles to flow without imposing wait states on the processor. Assuming, for instance, that the processor is running at its current maximum clock rate of 16.67 MHz, it could issue a valid memory address and be ready to accept data in 90 ns. Thus, for example, the system designer could shoot for a memory chip that accesses data in 70 ns or faster, with the 20-ns difference being eaten up by delays in the address decoder. On the other hand, the designer could opt for slower memory chips but substitute speedier decoders to compensate, a situation that would also produce read and write cycles without wait states.



1. The MC68020's interface dramatically simplifies the designer's job. The 32-bit-wide data and address buses prove invaluable, and they get assistance from logic that dynamically controls the width of the bus. Also, an instruction cache helps reduce the number of external bus cycles overall.

The 68020 does, however, offer the designer yet another unusual alternative to avoiding wait states while using slow memories: By exploiting the processor's External Cycle Start signal ($\overline{ECS}$) the decoding circuitry would start before the memory address strobe actually arrives. The $\overline{ECS}$ signal appears during state 0 of every bus cycle.

Wasteful waiting

As memory access time increases and wait states occur, the processor's overall performance drops in distinct steps. In fact, if the 68020 incurs one wait state during each cycle, it loses a significant amount of processing power, downgrading by the equivalent of about one 68000 operating at 8 MHz. On the other hand, the processor can take advantage of its built-in instruction cache, which stores recently executed instructions for reuse and thus sharply reduces the need for external cycles (ELECTRONIC DESIGN, July 26, 1984, p. 235).

An optimal system built around the processor should not only incorporate fast memories but also access instructions and operands 32 bits at time from memory. Like the built-in cache, such long-word accesses reduce the number of external bus cycles and raise the number of faster internal ones. In fact, the processor begins an operand transfer assuming that the transfer will be 32 bits wide. If the interface is indeed 32 bits, it moves on to the next operand. If the bus interface is 16 bits wide, the processor generates two bus cycles, and if an 8-bit bus is used, it passes four bus cycles before moving on to the next operand.

Depending on the actual bit-width of the transfer, as determined by the particular memory or peripheral being accessed, the processor will either complete the transfer and move on to the next operand or generate extra bus cycles. Two signals, SIZ_0 and SIZ_1, indicate the width of the transfer.

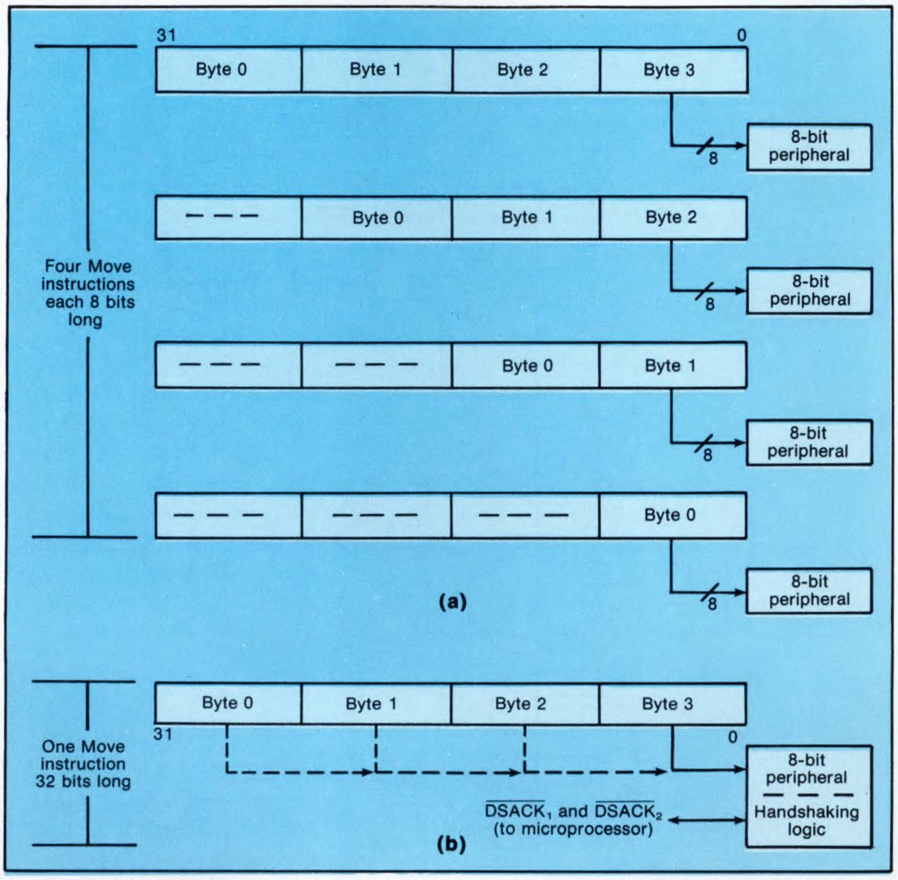
Any size fits all

The processor can adjust dynamically to different bus widths on a cycle-by-cycle basis. Thus designers can pick the bus width that is most practical for a particular device. During a transfer, a peripheral device or memory lets the processor know what its bus size is by sending two handshake signals, $\overline{DSACK_0}$ and $\overline{DSACK_1}$. Except for the fact that they are coded to reflect the bus size, the signals work exactly like the Data Acknowledge ($\overline{DTACK}$) handshake signal of other members of the family: A peripheral or memory asserts them when the data it is writing is valid or the data it is reading has been accepted.

With dynamic bus sizing, a designer can plan a high-performance system with 32-bit-wide RAM—where most system activity occurs—yet leave the ROM-based monitoring and bootstrapping section 8 bits wide. The reason is that the ROM area, though critical in the early stage of a design's development, is accessed only rarely once the system is running. Here an 8-bit bus would hardly decrease performance. It would, however, speed development because ROMs and EPROMs are typically organized as 8-bit devices.

Splitting program code among these devices for a 32-bit bus could impose a burden during the difficult embryonic stages of a system. Nevertheless, for very complex systems or for even higher performance, ROM-based code can be split among separate devices: into odd and even bytes for a 16-bit bus or four sections for a 32-bit bus.

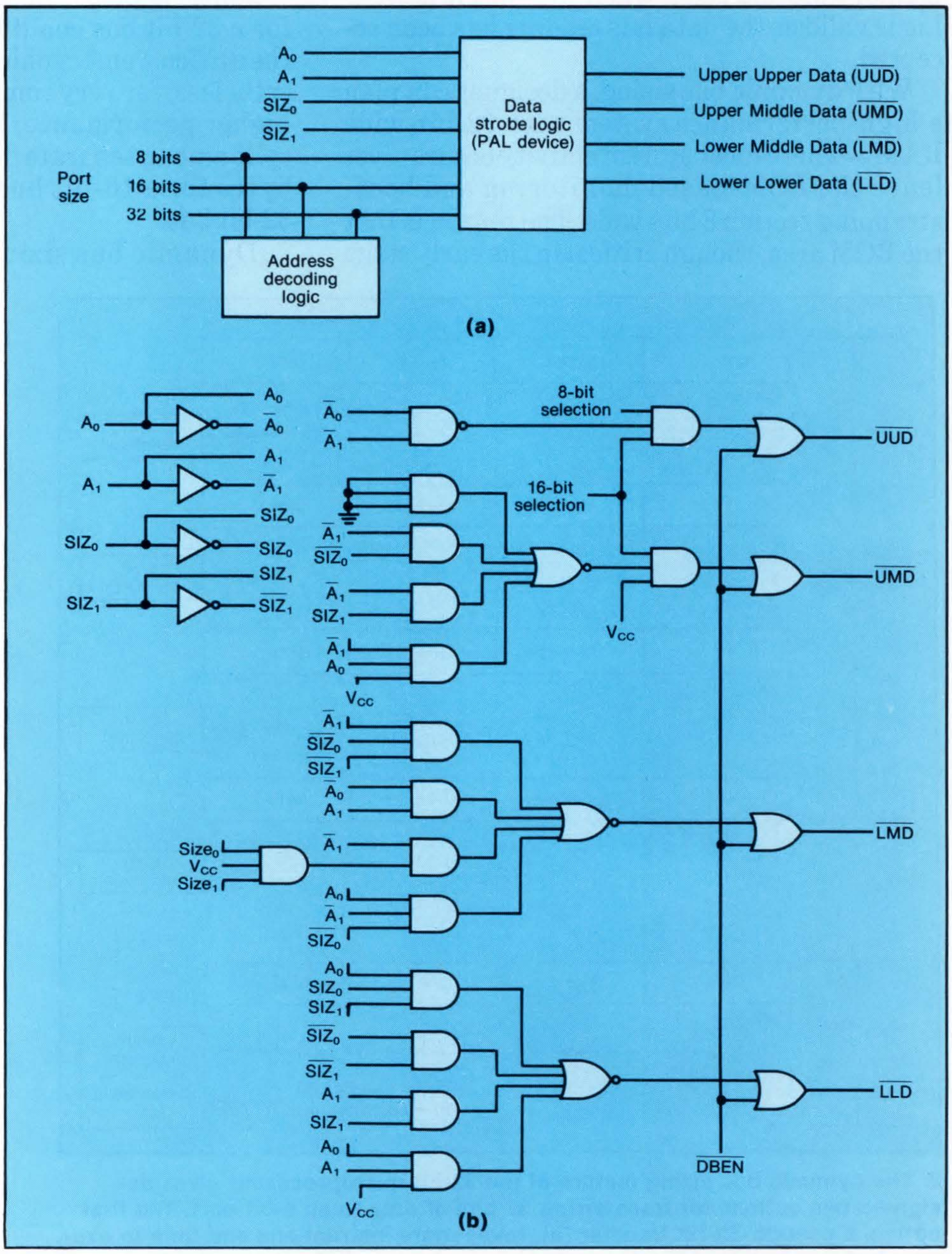
Dynamic bus sizing also gives designers



2. The dynamic bus sizing feature of the 32-bit microprocessor gives designers two options for transferring 32 bits of data to an 8-bit port. The first option, a pseudo-32-bit transfer (a), takes more instructions and time to execute but requires less hardware. The second is a true 8-bit transfer (b), meaning that 32 bits are transferred with a single instruction. Additional handshaking logic is needed to generate $DSACK_1$ and $DSACK_2$.

some leeway in transferring data to peripheral devices. They can choose between the simpler hardware scheme of addressing a pseudo-32-bit port or the greater program economy that comes from addressing a true 8- or 16-bit port (Fig. 2).

In addressing a pseudo-32-bit port, the processor transfers all of its 32 bits as if they were individual 8-bit or 16-bit transfers. Actually, interfacing with a pseudo-32-bit port disables dynamic bus sizing and forces a programmer to address an 8- or 16-bit peripheral through rep-



3. The processor must generate up to four separate data strobe signals when fewer than 32 bits are sent out at a time. The strobe signals tell a peripheral or memory device when a byte or word of data is ready. Normally, a single AND-OR-INVERT logic array could generate the four strobes (a), but when high speed requirements prevail, six TTL gates can do the job faster (b).

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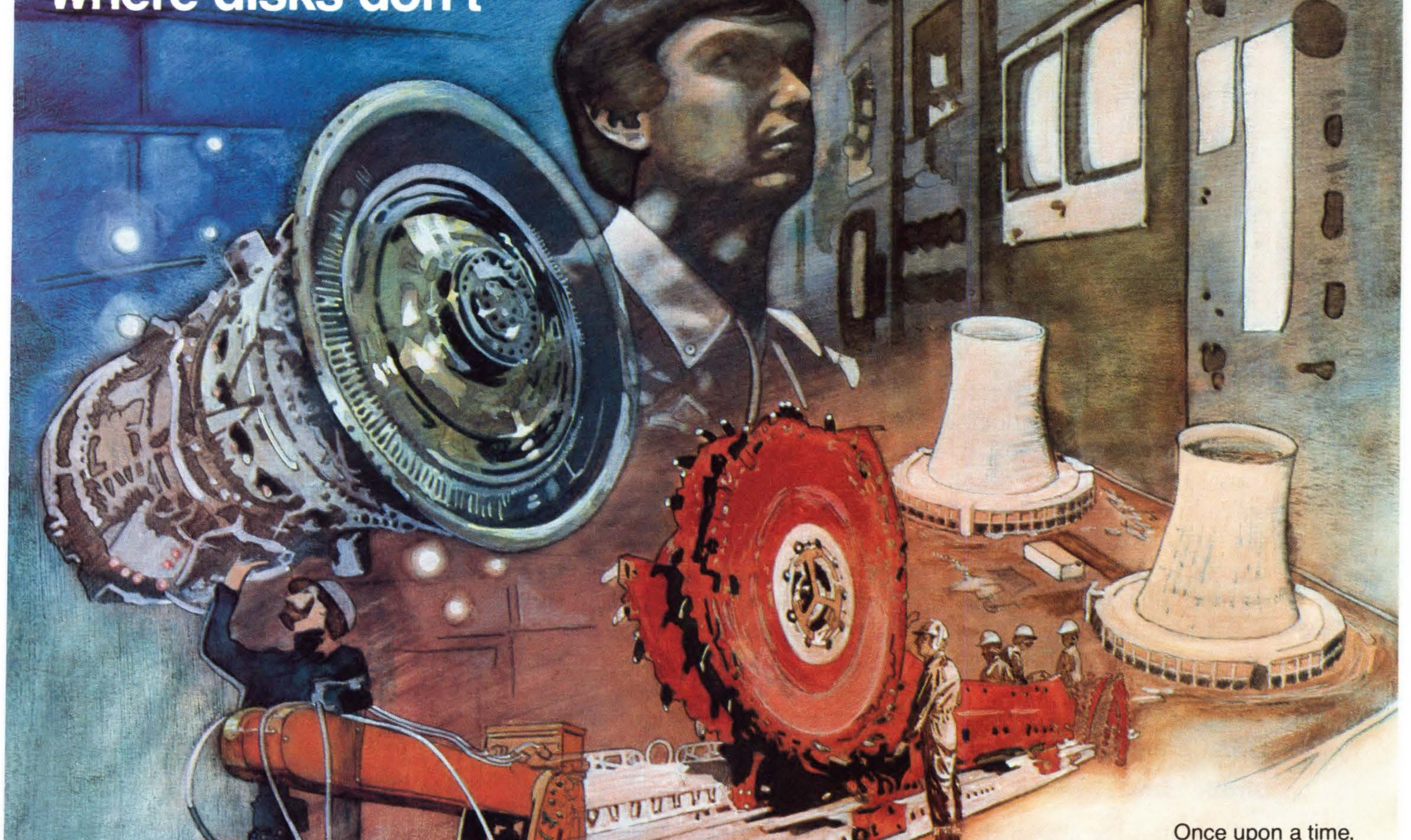

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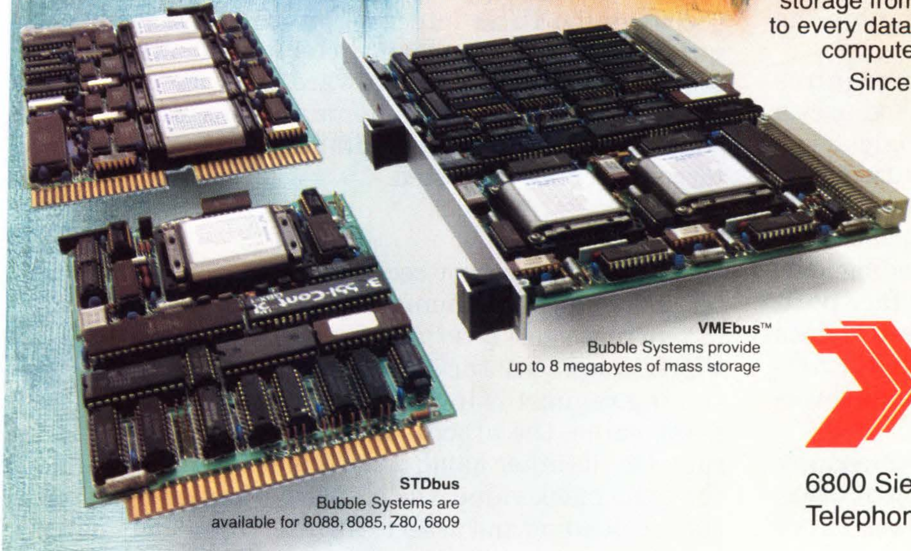

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However, the programmer must still ensure that all data transfers occur on the section of the 32-bit data bus that connects to the peripheral.

In contrast, the interface with a true byte-wide or 16-bit-wide port allows the programmer to use faster, 32-bit-wide transfer instructions. Here, the processor and external hardware automatically and dynamically change the bus size to transfer 32 bits of data across the narrower port. The processor does generate additional bus cycles to transfer the data, but they are invisible to the programmer, who can thus use 32-bit rather than byte-wide instructions. However, that method requires external hardware to generate the necessary encoded DSACK signals.

Strobe circuit needed

To adjust the size of the bus, external circuits must issue the correct strobe signals for gating data bus buffers. On a write transfer, the processor drives all sections of its 32-bit bus at once. Here again, it assumes a 32-bit transfer will occur. If fewer than 32 bits are transferred, the data strobes ensure that the data is pulled from the proper section of the bus. Under data strobe control, either peripheral-chip logic or external three-state buffers can enable the proper section of the data bus.

Actually, generating the strobes requires little additional circuitry. One method uses a single 24-pin AND-OR-INVERT logic array (Fig. 3a). Inputs to the array are the two least significant address lines, A_0 and A_1; bus size information from the processor, SIZ_0 and SIZ_1; and three lines from the address decoding logic that indicate the width of the interface port. The logic array puts out four active-low data strobes, which are needed to generate the necessary chip-selection signals or to enable three-state buffers on the data bus.

For higher speeds or unusual system setups, discrete components can replace the logic array (Fig. 3b). One implementation uses three 74LS54 AND-OR-INVERT gates, a 74LS32 quad two-input OR gate, a 74LS11 three-input AND gate, and a 74LS04 hex inverter. An even faster TTL family can be used if faster data strobe signals are needed.

Important interruptions

As with any microprocessor, the 68020's ability to handle interrupt requests is extremely important. In addition to its seven priority levels of vector interrupts, the processor offers two options for specifying the vectors that direct it to an interrupt-handling routine. Consequently it accepts interrupts from as many as 14 sources with little or no added hardware.

The interrupt option that a device ultimately picks depends on the state of the Autovector Control signal, AVEC. If AVEC is inactive, the processor takes an 8-bit value, called the vector number, from the data bus's least significant byte. On the other hand, if AVEC is enabled the chip generates the vector number internally, based on the interrupt's priority level. Moreover, the processor handles autovector interrupts as quickly as it handles normal ones because of its asynchronous interface signals.

To get 14 interrupt sources, a hardware designer simply assigns two sources to each priority level. One must generate a vector number during the processor's interrupt acknowledgment cycle, the other must force the processor into its autovector mode.

The 32-bit chip handles interrupt requests in much the same way as the other members of the 68000 family. Three interrupt priority level inputs, IPL_0 to IPL_2, accept priority-encoded requests from external hardware. Priority 7 is the highest, indicating a nonmaskable interrupt request; level 0 simply implies that no interrupt is being requested.

Setting priorities

When the processor receives an encoded interrupt request, it compares the request with the current value of a three-bit interrupt mask, which is stored in the status register. If the incoming request is lower than or equal to the mask value, the processor ignores the interrupt. On the other hand, if the request is higher than the mask value, the chip flags the interrupt as pending and asserts its Interrupt Pend-

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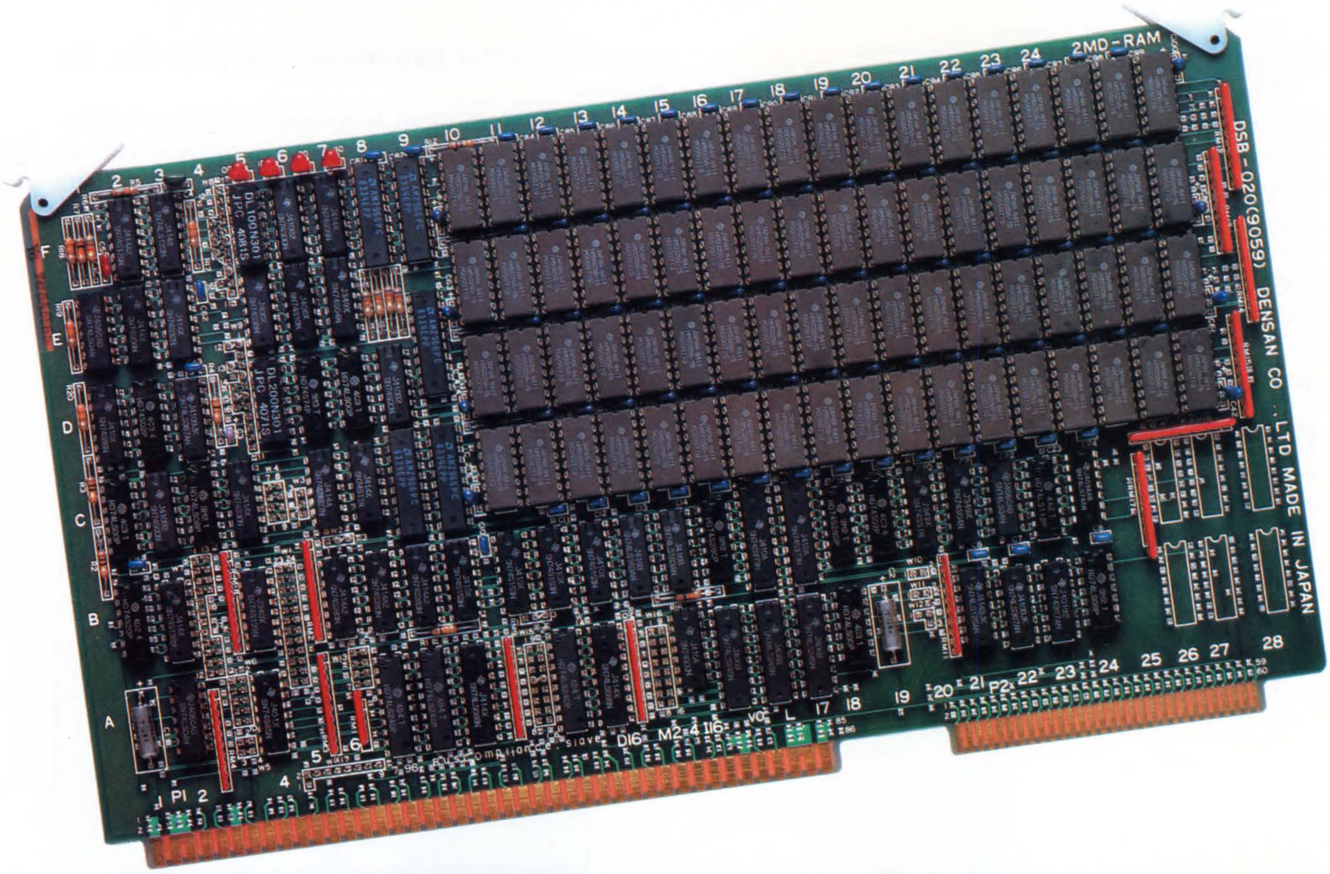

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ing output signal, IPEND.

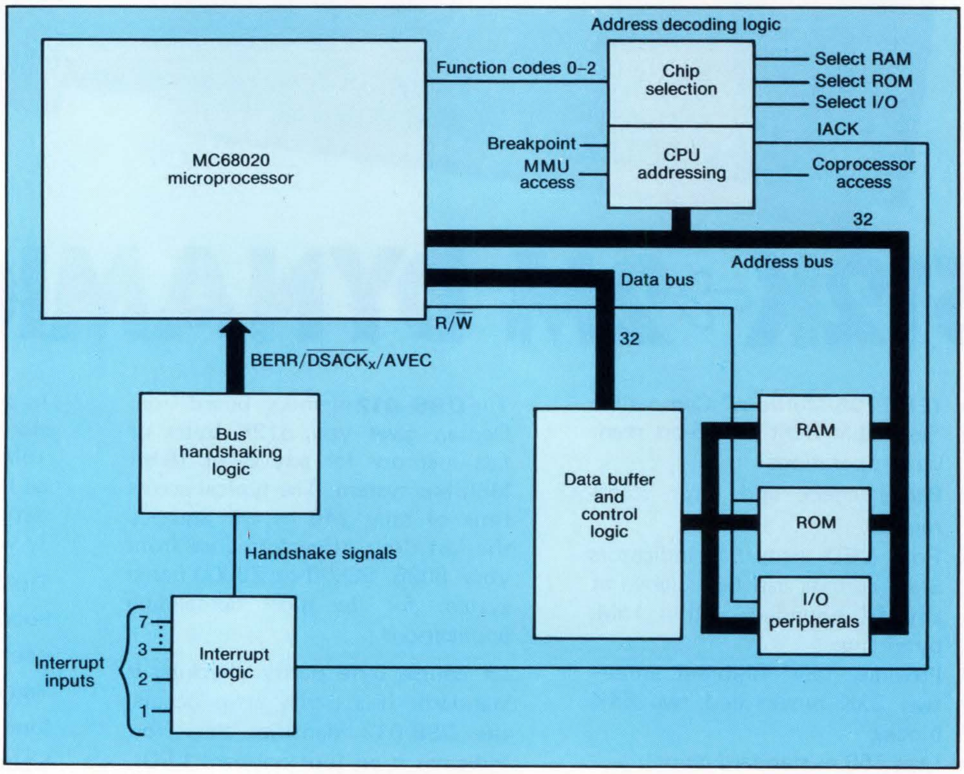
Whenever the processor reaches an instruction execution boundary—meaning it is ready to decode and execute its next instruction—it checks for a pending interrupt. On finding one, it begins an exception-processing cycle and executes an interrupt acknowledgment cycle. Before that cycle can be completed, the processor must see one of three inputs—DSACK, AVEC, or Bus Error (BERR)—or it will execute wait states until it finds one.

If the device requesting the interrupt sends a $DSACK_X$ signal, the processor takes the data from the interface port as the vector number. If AVEC is forthcoming, the processor generates the vector automatically. Finally, if BERR is asserted, the interrupt is considered to be a spurious one, and the processor assigns an appropriate vector number for handling that instance.

In any case, as soon as a vector number is generated, the processor saves its exception vector offset value, the contents of the program counter, and the contents of the status register in the supervisor stack, which is now active because the processor is in its exception-processing mode. In response to the vector number, the processor goes to the vector table, from which it fetches the 32-bit starting address of the vector-handling routine.

Send in the system

The sophisticated interface of the 68020 suits it ideally to the center of a simple yet powerful system (Fig. 4). Here both RAM and ROM are implemented as 32-bit-wide memories, taking



4. A simple yet powerful microcomputer system centers on the 68020. Both RAM and ROM sections are implemented as 32-bit-wide memories, with data transfers under the control of the data buffer and control logic. The peripherals, however, use a simple 8-bit bus, because they are accessed relatively infrequently compared with the memory devices.

full advantage of the processor's data bus. In contrast, the I/O devices, which access the processor infrequently, use an 8-bit-wide bus.

When the processor has initiated a transfer, the data buffer control logic activates only the relevant portions of the data bus, so that the chip can transfer data to either the memory or a peripheral device. The logic uses address lines A_0 and A_1, signals SIZ_0 and SIZ_1, and information about which port the processor is accessing.

In response, the bus handshaking logic encodes the DSACK signals for each bus cycle, telling the processor how wide the data transfer is. Because it gets its input from the interrupt priority logic, the bus logic must generate all handshake signals to complete an interrupt acknowledgment cycle. For that reason, it also contains a bus-error time-out circuit.

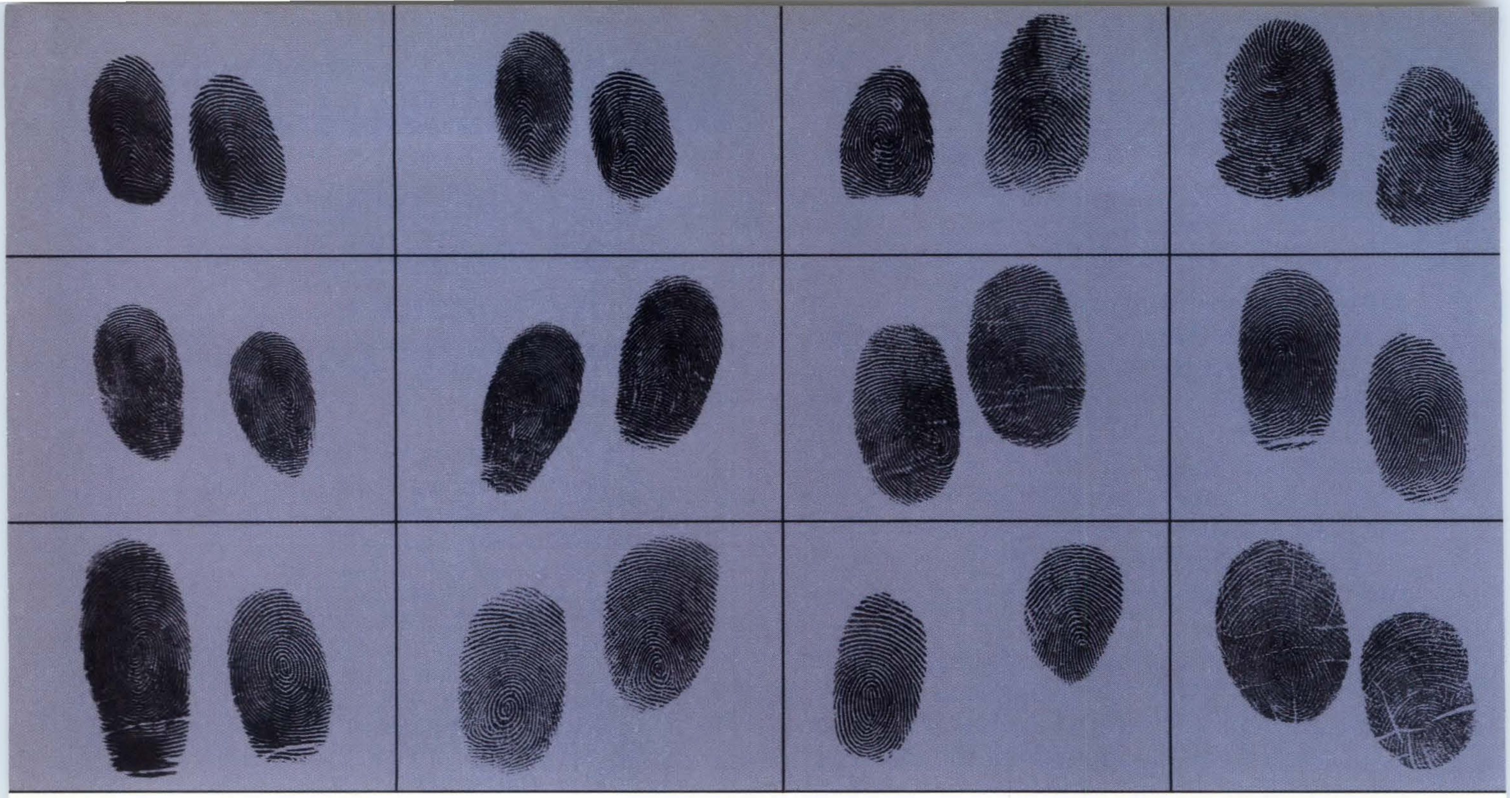
The interrupt logic itself accepts inputs from all seven interrupt sources and generates the encoded three-bit signal for the processor's interrupt priority logic inputs. During an interrupt cycle, that logic section also prompts the bus-handshake logic to generate the $\overline{\text{DSACK}}$ AVEC, or BERR signals.

Addresses for all

Finally the address decoding logic is split into two sections. One section generates the chip-selection inputs for all memory and I/O devices; the other section not only decodes accesses to the CPU address space but also develops selection signals for breakpoint instructions, for memory-management and coprocessor accesses, and for interrupt acknowledgment cycles. In an alternative configuration, the bus and buffer logic might use the address decoding signals to generate the $\overline{\text{DSACK}}$ signals and so control the data bus buffers.

Although this system uses fast static RAM, it could also incorporate dynamic RAM if the results drop in performance were acceptable. In that case, additional circuitry would handle dynamic RAM refreshing.□

How useful?	Circle
Immediate design application	550
Within the next year	551
Not applicable	552



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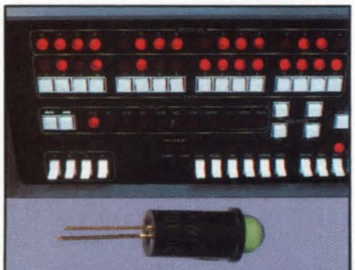

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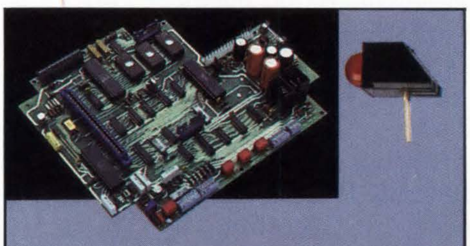

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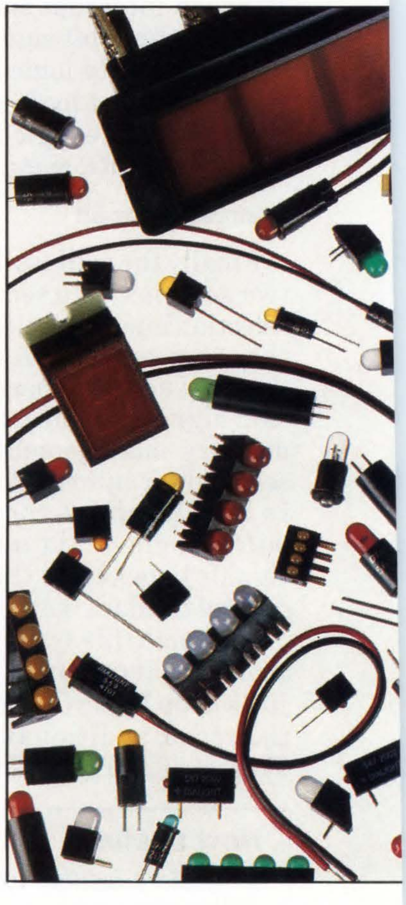

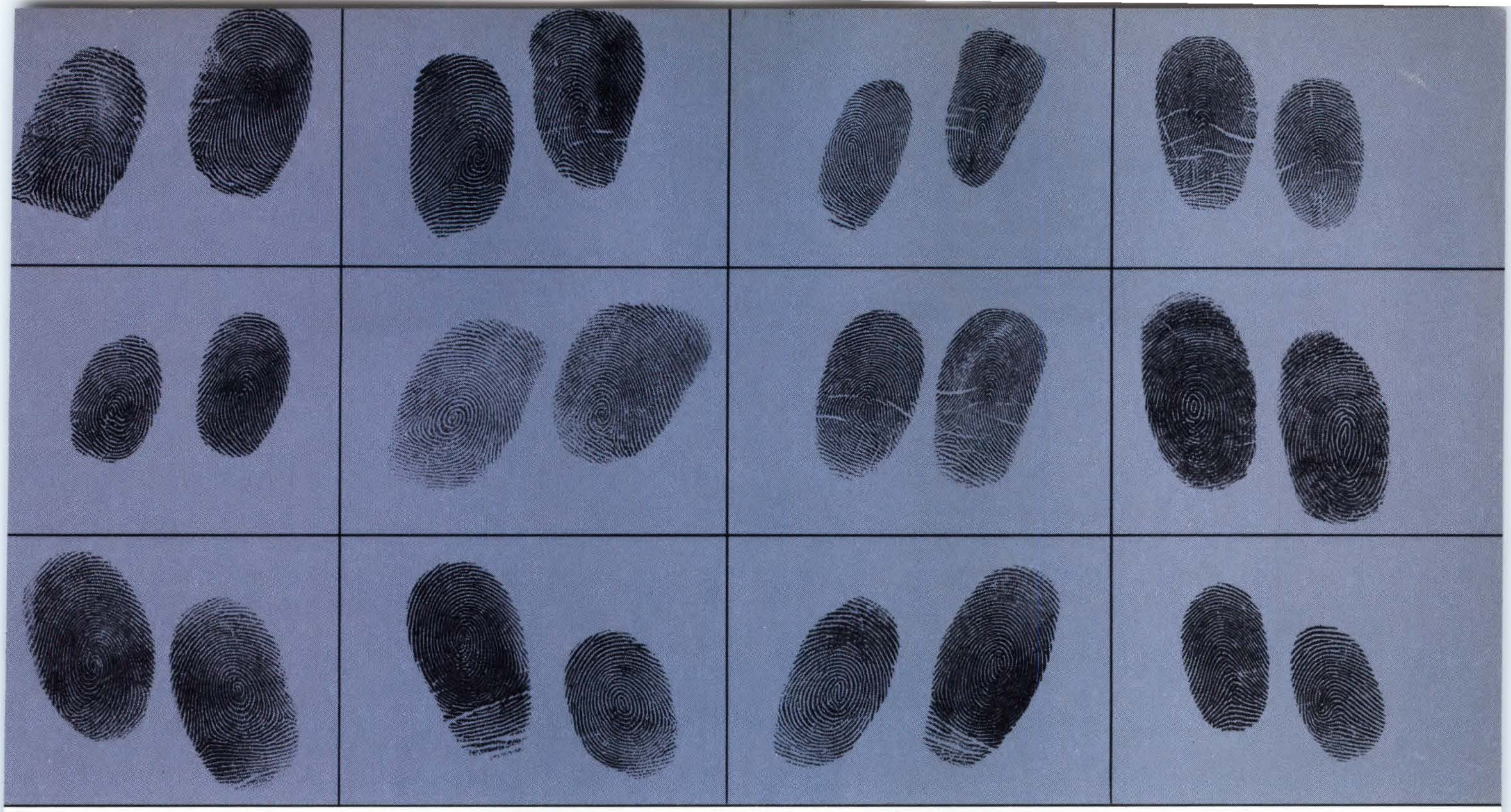

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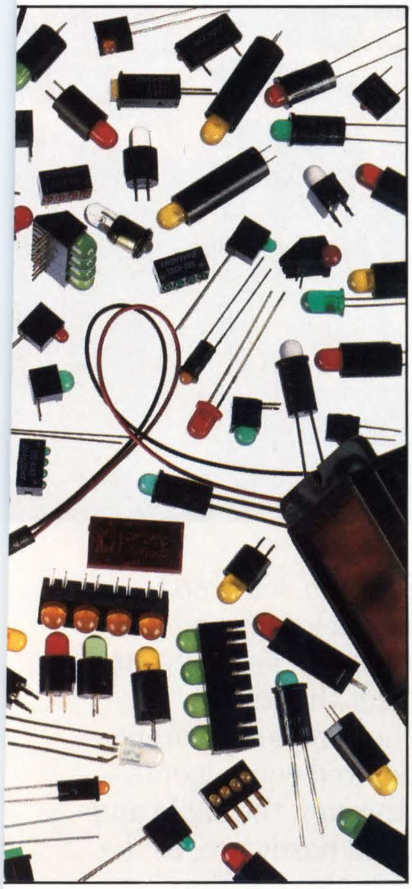

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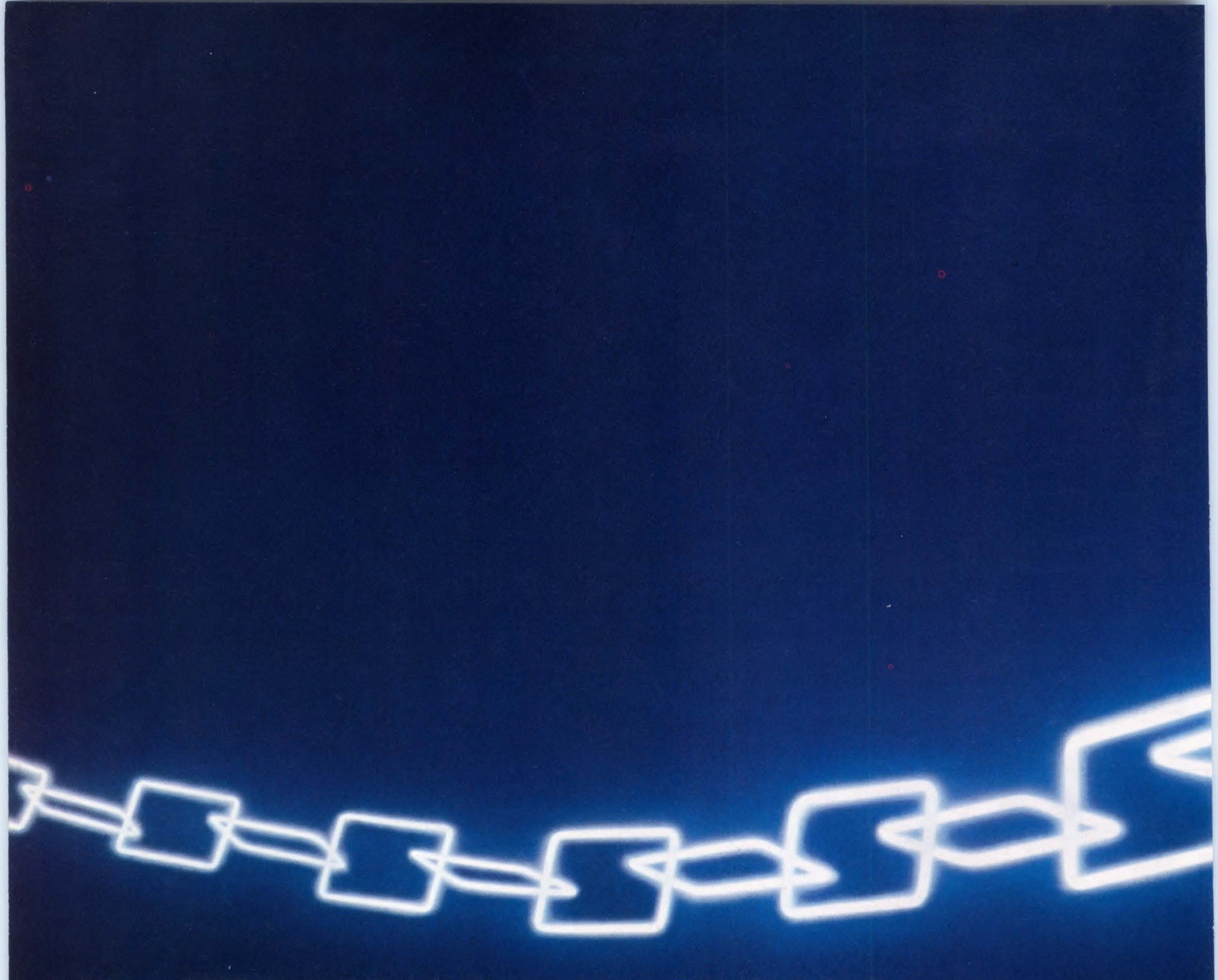

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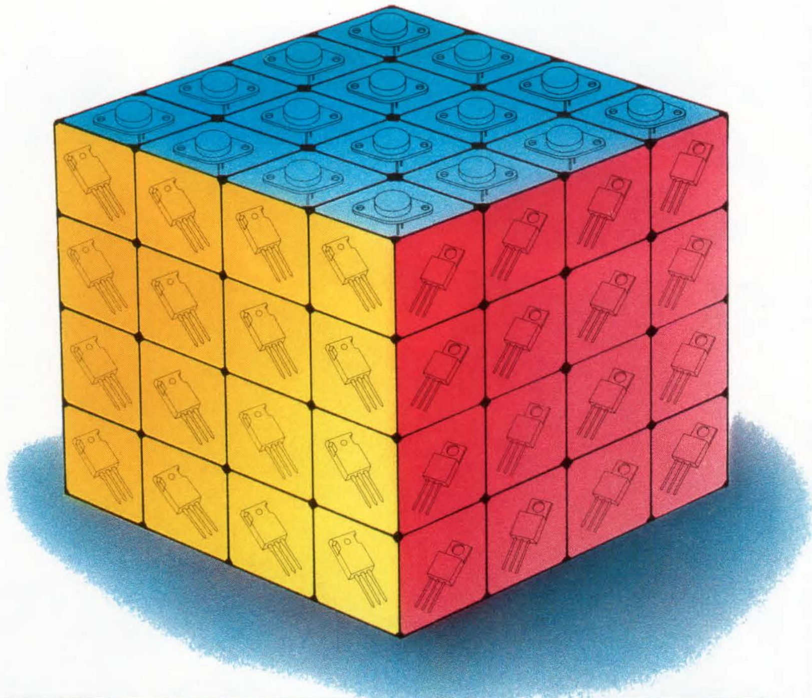

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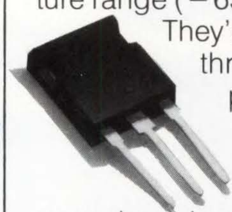

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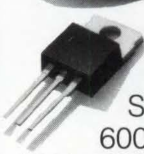

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Systolic arrays fill the bill as data-base management heads for gigabyte range

Parallel-processing building blocks with distributed memories offer speed and ease of use in systems where von Neumann architectures would falter.

This is the last in a five-part series on the first commercial systolic array processor chip. The initial article was the cover story of the Oct. 31 issue, and with the exception of Dec. 27, an installment has appeared in every succeeding issue.

Data-base management has become increasingly important in recent years, especially for relational data bases. However, as the size of these data bases moves toward the gigabyte range, conventional von Neumann architectures are too slow to meet demands. In large part, this is because the basics of data-base management—storing, retrieving, searching, updating, deleting, merging and ordering data—are not numerical operations. System designers must spend considerable time translating the basic data-base commands into host instruction sets for use on conventional processors.

Compounding this problem is a conflict between the requirements of operating systems and data-base managers. Ideally, a data-base system should store indexes in locations that contain only the information the indexes reference. However, operating systems distribute data to make the best use of available storage. Moreover, there is a tendency in von Neumann virtual memory systems to swap out pages of data frequently used by the data base. The biggest bottleneck of the von Neumann architecture is that all data processing is sequential. The net result of all these factors is a great increase in the data that a system must get from memory—sometimes 10 times more than is actually needed.

A practical solution is to develop parallel processing data-base management systems, and designers can do this with the Geometric Arithmetic Parallel Processor (GAPP), a systolic array containing 72 single-bit processors. Each processor has 128 bits of RAM. The chip, the first commercially available two-dimensional systolic array, processes data words in parallel, working on words of varying lengths by sequen-

Alexis Koster and **Norman Sondak**
San Diego State University
Paul Sullivan, NCR Microelectronics

An associate professor in the Information Systems Department of San Diego State University, Alexis Koster concentrates his research on such parallel programming languages as Prolog. Previously, he developed language processors for NCR. Koster has a PhD in computer science from the University of North Carolina at Chapel Hill.

Norman Sondak is chairman of San Diego State's Information Systems Department, where he is involved with designing computer and information systems. He has led the computer science department at Worcester Polytechnic Institute and earned a PhD from Yale.

Paul Sullivan is the business unit director for digital signal-processing devices at NCR's Microelectronics Division in Fort Collins, Colo. Before joining the company, he worked with Hughes Research Laboratories. He holds a PhD and an MSEE from the University of Southern California.

tially processing each bit, that is, it is a word-parallel, bit-serial processor.

A basic relational data-base scheme can be implemented with the systolic array, but since its architecture is not similar to that of von Neumann processors, the architecture of the relational data-base system will also differ. The systolic array processor can be used in a subsystem or as part of another system.

An accent on speed

The chip's single-instruction, multiple data-path (SIMD) architecture increases throughput in common tasks within the relational data base. The chip, arranged in rows and columns of processing elements, handles rows and columns of data.

For instance, in a relational **Join** operation (Fig. 1), two tables (a) are linked to create a third table (b). The array forms each row in the result by joining two rows, one from each of the tables. The selected rows each have a common element. A **Semi-Join** operation produces an output from only one of the tables, but the items selected for output depend upon the second table (c).

In a typical processing system, each of these steps must be handled sequentially. However, the systolic array can work with all the rows and tables at the same time, producing the Join tables much faster. Each processor element in the array works on an individual datum (item of data). The array can be used with various data base formats: a number of chips can be tied together to make a large grid of processor elements, thereby increasing throughput.

Since a parallel processor handles data faster than its traditional counterpart, its I/O rates must correspondingly be faster. Mainframe parallel processors have used three major approaches, and all can be used with systems built with the systolic array. The earliest technique dedicated a head for each track of the fixed disk that the data-base management system used

File 1

Student	Major
John	Math
Peter	English
Michelle	French

(a)

File 2

Class	Student
Management 301	Michelle
Management 301	Peter
Math 201	John
Math 201	Michelle

File 3

Student	Major	Class
John	Math	Math 201
Peter	English	Management 301
Michelle	French	Management 301
Michelle	French	Math 201

(b)

Student	Major
John	Math
Michelle	French

(c)

1. The systolic array chip can easily handle such relational data-base operations as Join and Semi-Join. A Join operation, for instance, links files 1 and 2 (a) to form file 3 (b). The Semi-Join operation then searches the newly formed table, pulling out which students are enrolled in a mathematics class (c).

for storage. The technique also proposed a processor for each multiple head to furnish the utmost in throughput.

But the high cost of multiple head disks, coupled with the expense of individual processors for each track, forced compromises. Now, high speed, moving-head technology has been developed so that there is only one head for each disk surface, greatly trimming the requisite number of heads and processors.

As memory prices have dropped, data-base architectures have moved toward cache memories. Large disk caches increase speed, minimizing the number of disk accesses while delivering faster transfer rates than are possible with off-the-disk approaches.

Regardless of the approach taken, the systolic array will generally be used only to perform dedicated data-base processing: its architecture does not lend itself to the diversity of tasks that must be performed by a host computer.

Block by block

As with other set-ups discussed in this series, the systolic array data-base management system can be built building-block style. Groups of GAPP devices can be put together, to form an SIMD array of the required size. In addition, several different blocks can each perform specific tasks so that the complete data base machine operates as a multiple-instruction, multiple-data-path (MIMD) system.

One block, for example, can address the basic task of any data-base manager: searching the memory to locate some required information or to determine that it is not in the system. The systolic array easily makes such comparisons in parallel. Consider a search for a 12-character comparand (the comparand is the required data that is compared with the data in memory). If each character is made up of 6 bits, the 12-character search can be handled neatly by the 72 processor elements of one chip (Fig. 2).

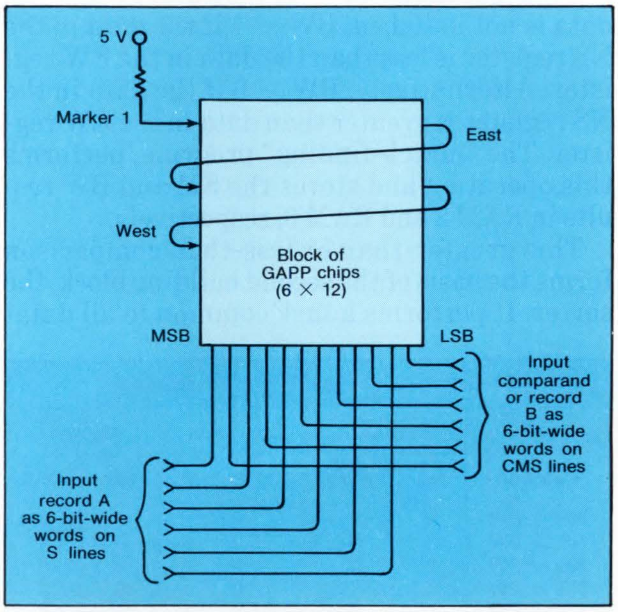
The code for loading the comparand into the chip is simple: CM:=CMS (repeated 12 times) followed by the instruction EW: = RAM0, RAM0=CM. The EW register, one of four registers in each processor element, is loaded via the CMS line. Since several systolic arrays can be linked to form grids, it is easy to increase the size of a grid to match the typical word size and processing rates of the system.

As the data is being fed into the grid, it streams through the chips, entering on the south and exiting at the north. After each character is clocked into the array, an exclusive OR comparison is performed and the result placed in the NS register. If all characters in the array match, then the global output (GO) flag is high.

I don't care

The comparand can be masked so unimportant characters or bits represent a "don't-care" condition. Locations being masked with the "don't-care" condition will place a 0 in RAM 2, while all other locations will have a 1 in RAM 2. The result of the exclusive OR comparison is then ANDed with the mask in RAM2 before the result is placed in the NS register.

This type of exact match is useful for searching text files for specific information. In a common variation of this operation, like "find and replace," the replacement word can be stored in



2. The chip can accept and process input record A, which comes from memory, and the comparand or input record B. If it cannot complete the processing in one pass, the signal can be wrapped around and run through again.

Systolic array chip

one of the RAM addresses. When the desired word is found, its replacement can easily be substituted while data streams through the array at rates up to a million characters per second.

Shuffling the cards

Another major task of any data-base management system is sorting. This involves a bit-comparison operation that is somewhat similar to the compare operation. But in comparing bits for sorting, the system must determine not only whether the data in the NS register matches that in the EW register, but also whether it is greater or less than that contained in the EW register.

The system does this three-way comparison by examining both the Sum (SM) and Borrow (BW) outputs from the ALU (see the table, below). If condition C = 0 and the data in the NS register matches the data in the EW register, then SM = 0. If the data in the NS register does not match, then SM = 1. However, when the data is not matched, BW = 1 if the data in the NS register is less than the data in the EW register. Alternatively, BW = 0 if the data in the NS register is greater than data in the EW register. The "match-finding" program, performs this operation and stores the SM and BW results in RAM 2 and RAM 3, respectively.

This greater-than or less-than comparison forms the basis of the second building block, the sorter. It performs a task common to all data-

A three-way sorting comparison

Relation	Input		Condition	Output	
	NS	EW	C	BW	SM
NS < EW	0	1	0	1	1
NS > EW	1	0	0	0	1
NS = EW	0	0	0	0	0
NS = EW	1	1	0	0	0
NS < EW	0	1	1	1	0
NS > EW	1	0	1	0	0
NS = EW	0	0	1	1	1
NS = EW	1	1	1	1	1

base systems: reordering data, based on the user's request. With minor alterations, the traditional ordering and sorting algorithms used with conventional serial processors can be easily switched to take advantage of the parallel processing of the systolic array. The result is an increase in performance.

The sorting algorithm used in a systolic array system is basically just a parallel version of the classical exchange sort, in which pairs of numbers or other data are exchanged to reflect their relative position in the sorting order. For instance, pairs of data are first compared in the order in which they are found in memory (1 and 2, 3 and 4). Then they are paired again for the next comparison (2 and 3, 4 and 5). At each comparison, the pairs of items not in order are exchanged (Fig. 3).

Getting a perfect match

To implement such a sorting algorithm with the systolic array chip, two strings comprising records A and B must be loaded into the array, much as was done in the comparator block. Each record is again assumed to consist of 12 characters of 6 bits each. Once they are loaded in, the SM and BW output bits are computed to find matches (see the program, p. 354).

If the records do not match, the system must determine whether record A is less than or greater than record B. The systolic array does this by searching the bit string until the first unmatched character is found, then identifying the MSB that does not match, again using bit comparison.

The array does this by shifting a marker, or "1" bit, in serpentine fashion through all the processor elements as shown in Figure 2. The maker propagates until it finds the "FIRST" responder, where RAM2=1. Then RAM3 is examined in that processor element to determine whether the records should be swapped.

During this operation the device must make an exchange or no-exchange decision before the records are loaded into the next row of sorter blocks. This may require the marker to propagate through all 72 processor elements within some chips. Meanwhile, other chips in the grid are idle until all devices have completed their swaps.

Each sorting cycle for comparing pairs takes less than 24 μs. Thus eight records can be sorted through the eight stages in 192 μs, and eight more records can be entered into the pipeline every 24 μs.

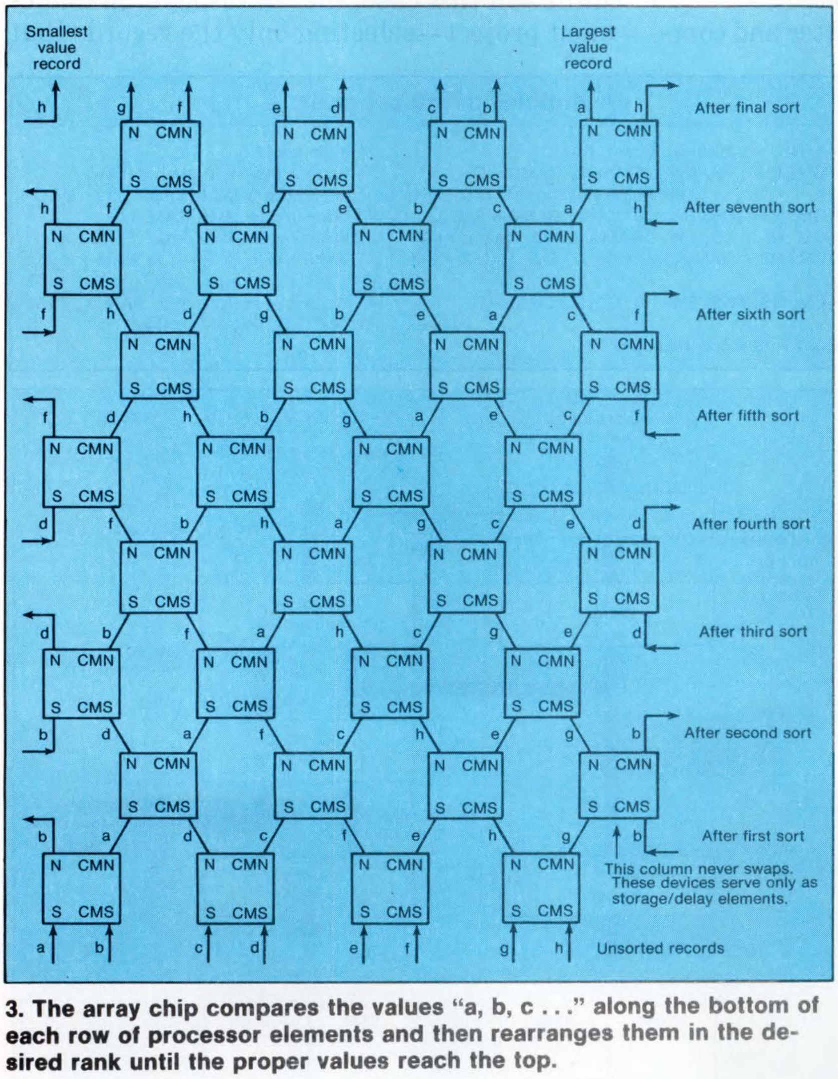
A sort using the systolic array chips will take N steps to process N elements, compared with N^2 steps for a typical von Neumann processor.

Forging links

Systolic array building blocks can easily be linked into systems that perform the data-base functions. The comparator block alone can perform queries involving only one file, such as "Find all employees hired before 1980."

The data-base records are read in parallel and loaded into the grid of systolic array chips. Both the query field, "date of employment," and the constant, "1980" are loaded into the comparator. As the compare function is performed, the records that are less than "1980" are sent to the host, while the others are ignored.

The use of two comparator blocks allows designers to perform more complex tasks, like finding "employees hired after 1980 whose salary is greater than $25,000." Two blocks of systolic arrays can search in parallel to find



3. The array chip compares the values "a, b, c . . ." along the bottom of each row of processor elements and then rearranges them in the desired rank until the proper values reach the top.

Systolic array chip

matches for both the time and salary constants. The results are then passed to a third block, which performs the AND function that determines acceptance or rejection for the two-part query.

Table settings

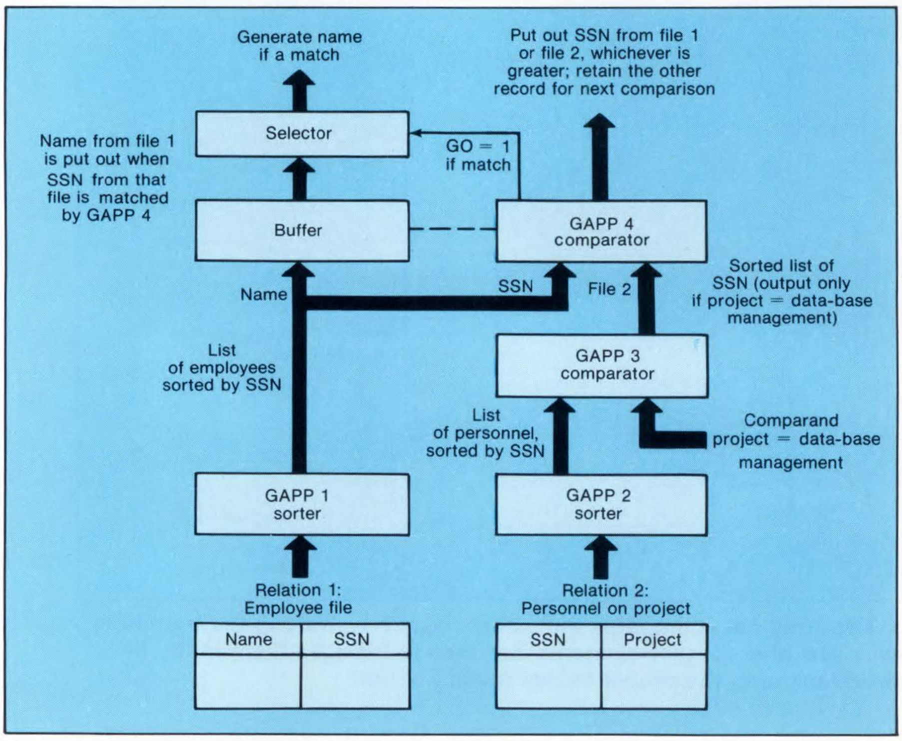
A related function that can be performed much more quickly with parallel processors is a multiple file operation like **Join** or **Semi-Join**. A **Semi-Join** operation, the most common in most data-base processing systems, produces a subset of one table; this subset is determined by a relationship from a second table.

This operation requires both sorter and compare blocks (Fig. 4). The search for "employees working on the data-base project" is a typical **Semi-Join** operation; it uses two files. The two in this example have a matching component, the Social Security number, that lets the system list the personnel on the project, even though their names are not in the project file. The task can be performed by several blocks of GAPP devices. The two files are passed through two sorter blocks. There the lists are put in order employing the Social Security numbers.

A third block, a comparator, compares the data in the project record in memory to the constant—in this case, the "data-base" management project—selecting only the records that

A match-finding program

```
CM:=0, NS:=0, EW:=0, C:=0, RAM0:=C              /* Initialize */
CM:=CMS, NS:=S, EW:=0, C:=0, RAM0:=C            /* Repeat this instruction until all
        characters of the two records to be compared are loaded into the array */
CM:=CM, NS:=NS, EW:=0, C:=0, RAM0:=SM           /* Write record A to RAM 0 */
CM:=CM, NS:=NS, EW:=RAM1, C:=0, RAM1:=CM        /* Write record B to RAM 1 and EW */
CM:=CM, NS:=RAM2, EW:=0, C:=BW, RAM2:=SM        /* Write SM = A ⊕ B to RAM 2 and
                                                   NS*/
CM:=CM, NS:=NS, EW:=0, C:=0, RAM3:=C            /* Write BW = Ā • B to RAM 3 */
                                                /* Test GO: If GO = 1 then
   record A matches record B */
```



4. A configuration of parallel processor building blocks can tackle data-base tasks. Here four chips search through two files to find the names of workers involved in a data-base management project.

match. The results are then passed to another comparator block, with only the Social Security number going to this group of systolic arrays. This sorter block then looks for matches with the file that has both names and Social Security numbers. When a Social Security number from the employee file is not in the list on the comparator block, that record is removed from the buffer by the selector. When the two records match, the employee's name is passed through the selector to the host computer. This type of parallel processing architecture provides several orders of magnitude higher throughput than a von Neumann machine.

By using building blocks in this fashion, a designer can easily create a full system divided into five units: the host, the systolic array controller, the systolic array blocks, a switching matrix, and a storage device (Fig. 5).

The host performs typical tasks, including processing and compiling queries, issuing commands to the systolic array, and receiving responses, as well as handling user communications and interfacing. The GAPP controller need be no more than a dedicated microcomputer. It receives commands from the host and analyzes them, then dispatches programs and I/O commands for the array. It also receives the output from the arrays when the tasks are completed. The controller then selects data from this response and sends the appropriate data to the host. Each block of chips in the system has an address, so the controller can distribute programs over the appropriate control lines.

The switching matrix serves as the link between the storage device and the systolic array building blocks. Storage can be handled by disks or cache memory. □

How useful?	Circle
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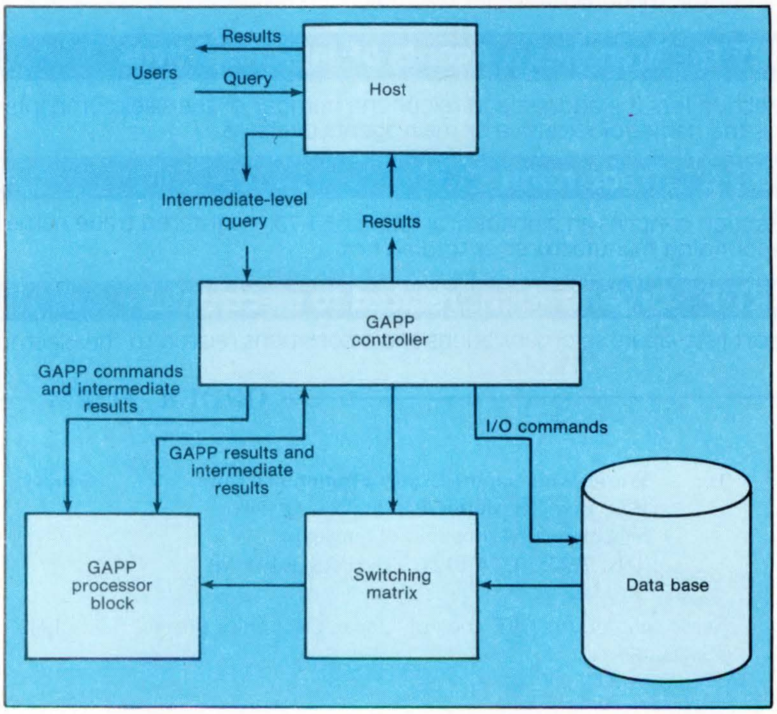

5. Systolic array chips can be called into duty in a data-base management system, forming a processor block, a controller, and a switching matrix. The matrix prepares data for array processing.

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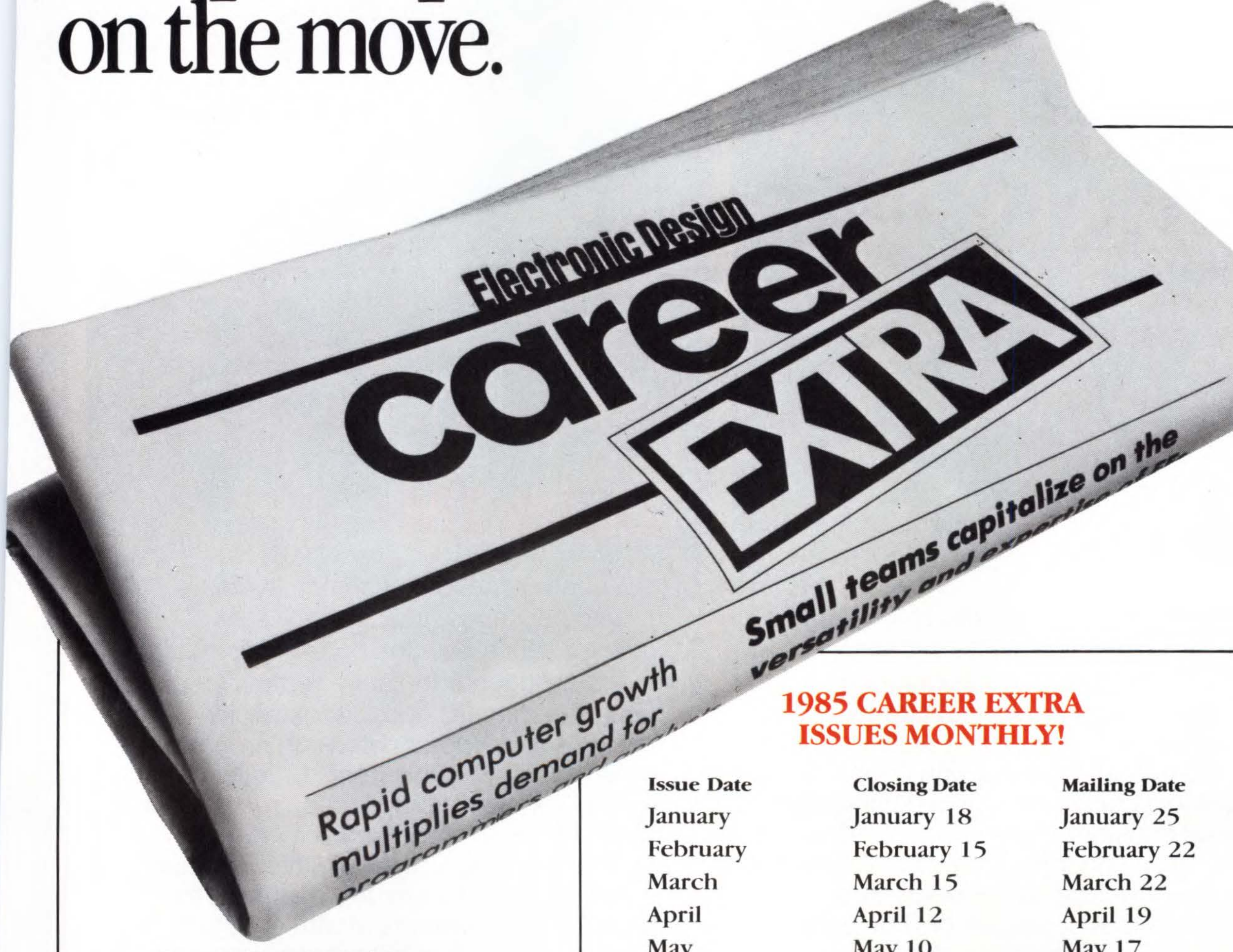

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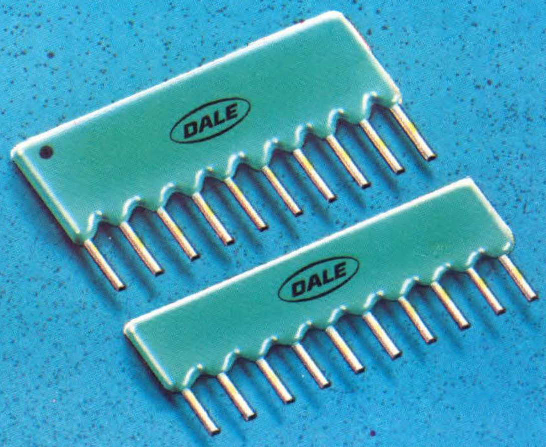

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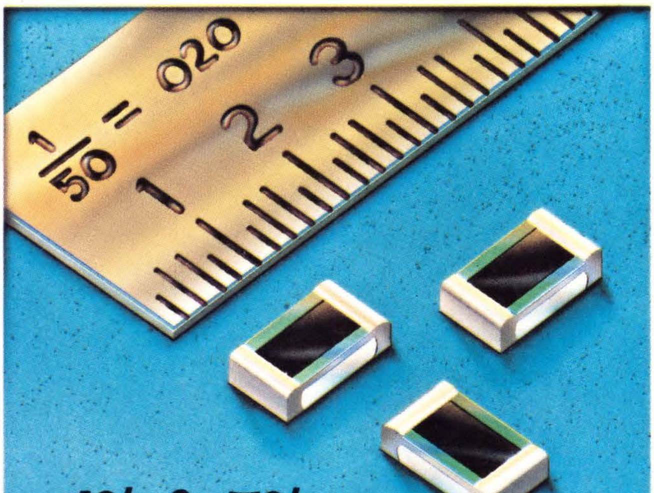

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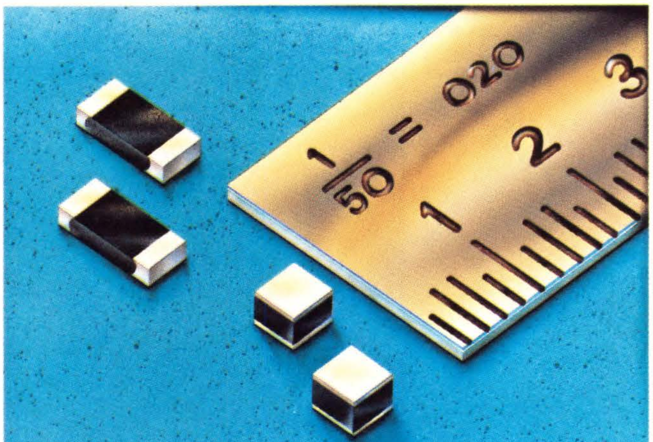

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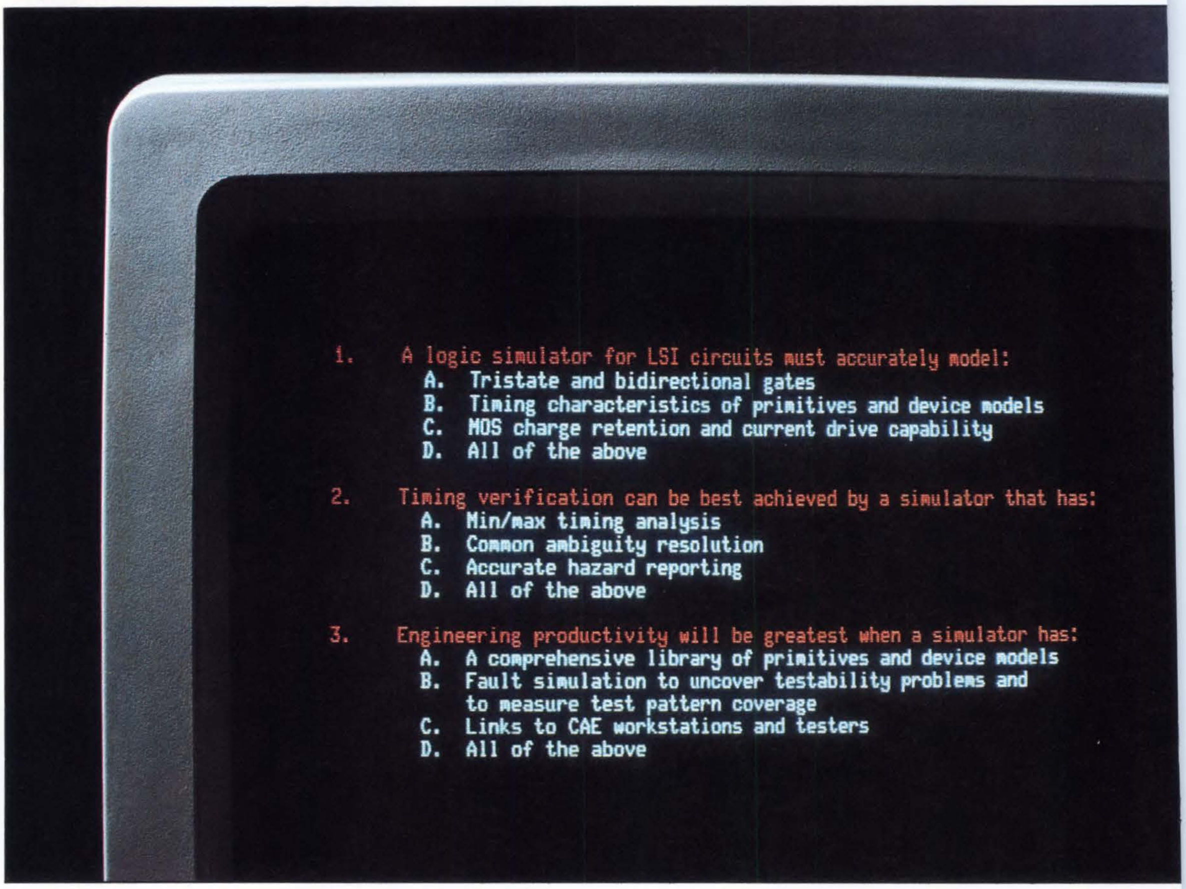

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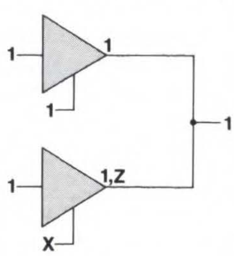

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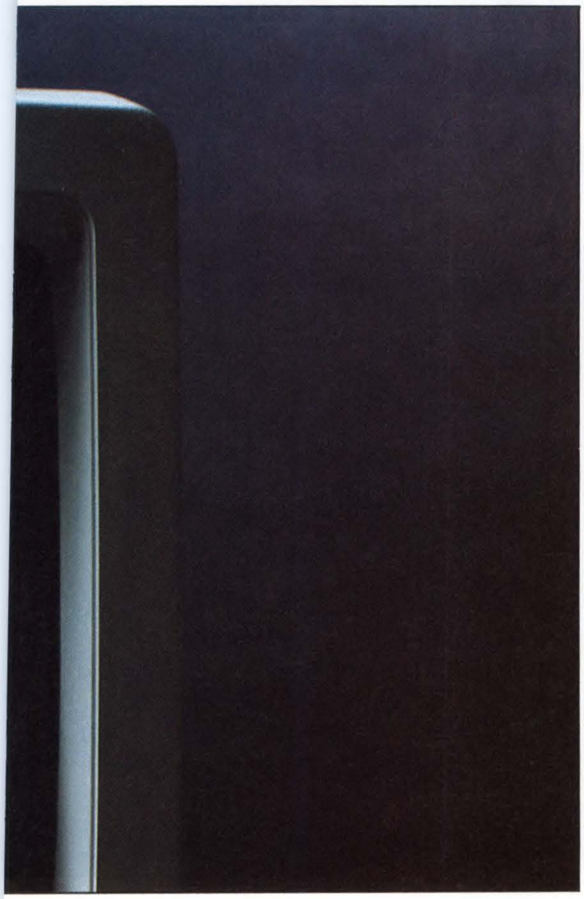

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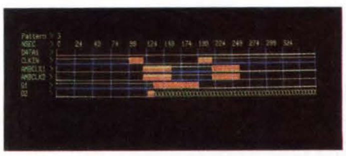

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CIRCLE 181

DESIGN SOLUTION

Logic-triggered amplifier upgrades oscilloscope for digital troubleshooting

A vertical amplifier module plugs right into an oscilloscope, giving it the triggering skills to track and analyze digital system faults.

Because digital logic operates within an analog environment, a synergism of the testing techniques used for both should ideally produce a powerful yet general-purpose tool for pre- and post-production troubleshooting. But simply pairing a logic analyzer and an oscilloscope is insufficient to root out faults in digital systems, since the analyzer's triggering style must be adapted specifically to the oscilloscope's needs.

The 7A42 logic-triggered vertical amplifier does just that for the high-speed oscilloscopes in the 7000 series, turning them into effective tools for high-resolution measurement, display, and analysis of the signals generated by TTL, ECL, or CMOS logic. The plug-in subsystem helps create analog representations of such common digital signal problems as ringing, overshoot, and undershoot, and it even deals handily with high-speed logic applications, where precise timing is critical for proper circuit operation.

David White and **Craig Wasson,** Tektronix Inc.

As product manager for Tektronix's Laboratory Instruments Division in Portland, Ore., David White directs the digital storage oscilloscope line, as well as defining and introducing additions to it. When he joined the company in 1978, he built and installed semiconductor test systems.

Craig Wasson, a graduate of the Oregon Institute of Technology, has been with Tektronix for 10 years, serving the past three as a logic analyzer support specialist and applications engineer in the company's Design Automation Group.

Being designed for periodic waveforms and single-shot events, an oscilloscope customarily employs level and slope triggering schemes, which are ineffective for digital pulses. Moreover, it lacks an internal means of distinguishing one digital pulse from another. Logic analyzers, on the other hand, see data as a succession of high and low levels and depend on discrete sampling, so that the behavior of a signal between sampling clock pulses remains unknown.

Old fixes don't work

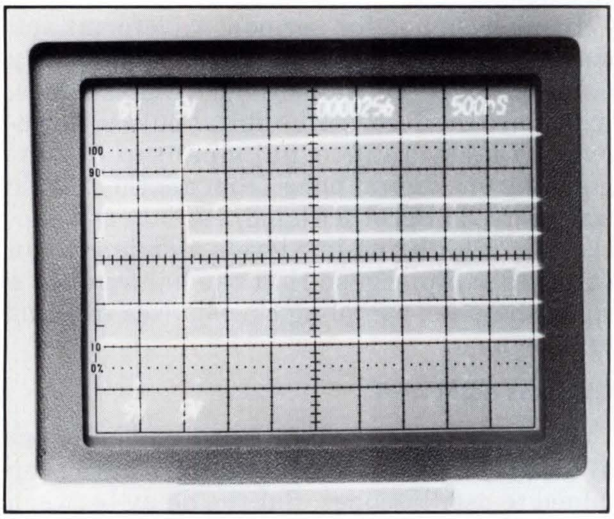
To obtain real-time information on individual digital signals, word recognizers have been added to oscilloscopes. But the delay between the recognition of an event and the start of a sweep can be so long that the event passes before it can be displayed. Similarly, when a scope is triggered by a logic analyzer, a trigger signal can reach the scope two or three machine cycles too late, as often happens these days when the system under test has a very high clock speed. The user can try to anticipate the occurrence of any event and set a triggering scheme accordingly, but because scopes provide very little pretrigger information, that is a difficult and often impossible task.

The 7A42 dashes that problem. Its advanced, programmable triggering mechanism makes it

Logic-triggered amplifier

resemble a logic analyzer, helping pinpoint glitches based on a complex set of digital events—a common requirement for efficient troubleshooting of microprocessor-based systems. The 7A42, which occupies the two slots for plug-ins in the 7000 series mainframe, has four independently programmable channels that simultaneously trigger a display of up to four traces. A clocking pulse can qualify the triggering function in much the same way as a logic analyzer does when operating in a synchronous mode.

In addition to nested Boolean-function triggering, the vertical amplifier can start the scope's time-base sweep on the rising or falling edge of a pulse that has been qualified by other signal levels. As an added advantage, a separate trigger-view function permits the trigger output or an external clock input to be displayed. Logic switching thresholds are independently variable to allow triggering by the output signals of mixed-logic devices.



1. The oscilloscope, when connected to three control lines and to the strobe output of a microprocessor system, reveals normal logic levels. No crosstalk or ringing is evident.

Because of the amplifier's analog approach to digital data acquisition, its timing resolution is better by nearly an order of magnitude than that of the fastest logic analyzer. A 350-MHz bandwidth and a maximum differential delay of 200 ps between channels optimizes high-resolution timing measurements, including such subtle and time-critical factors as pulse width, signal rise and fall times, and propagation delay. In contrast, for the same display resolution a logic analyzer would need a 5-GHz sampling rate.

Error-reporting functions guide the operator through instrument setup and manipulation. Functionally grouped pushbuttons, a color-coded front panel, and multicolored LED indicators communicate the instrument's status. An internal battery preserves both parameter settings and status information when external ac power is removed.

The system under test

Consider a typical application in which the logic-ready scope debugs a prototype microprocessor system. The representative system uses a common I/O bus to service a CPU, two disk drives, a keyboard, and a CRT display. The test setup includes a 1-GHz scope equipped with the logic-triggered vertical amplifier and a plug-in time base. A logic analyzer with a dual time base is desired and should have 72 data acquisition channels. It should also work at 50 MHz synchronously and 100 MHz asynchronously and have 14 triggering levels and an external trigger input.

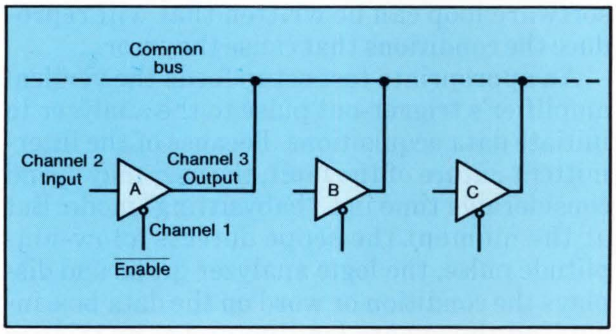
During development of the prototype system, bad data appears intermittently on the CRT screen with the good data. But the bad-data episodes occur in no discernible pattern. As with other systems, troubleshooting here entails finding one intermittent fault amid an almost limitless number of possibilities. The process begins with the broadest overview of the system's problem and gradually narrows the field of focus until the problem has been isolated to a specific area.

After first giving the system a thorough visual examination, the user employs the oscilloscope to search for obvious problems on the

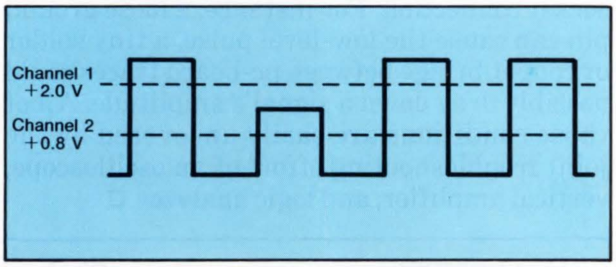
CPU control lines—the link common to all system peripherals. Because those lines are highly susceptible to overloading and interference, they are likely suspects. Properly used, the scope's speedy display can verify timing, observe signal quality, and check for noise. By connecting one probe to each of three control lines and to one strobe line, the user can confirm timing specifications. Verification, which also plays a part in initial testing, makes sure the setup and hold times on the control lines are long enough for data to latch.

Continuing the search

Signal quality should show adequate levels, without excessive ringing. If the levels of signal reflections, aberrations, or cross-talk are not unusual (Fig.1), the problem does not originate from the control lines, and testing must move to other areas, such as bus contention.



2. Bus contention occurs when two or more devices try simultaneously to drive a common bus. The vertical amplifier generates a trigger whenever the device's output does not match its input after it has been enabled. A special filter in the amplifier prevents inadvertent triggering caused by propagation delay through the buffer.



3. To find low-amplitude pulses, the vertical amplifier's NOT CH1 AND CH2 **function triggers on any pulse that remains within the TTL transition area (0.8 to 2 V) longer than the period defined by the trigger filter.**

A common cause of intermittent problems in bus-oriented systems, contention arises when more than one device attempts to drive a common bus at the same time, usually because of a part fault or poor circuit design. The condition is difficult to detect with either an oscilloscope or a logic analyzer. Besides causing an invalid logic level that results in the transfer of bad data, bus contention can also create a substantial power-supply glitch, another fault that is extremely difficult to detect with an ordinary oscilloscope because of the aperiodic nature of bus activity. Further, the level and slope triggering mechanisms of a conventional scope cannot recognize that condition.

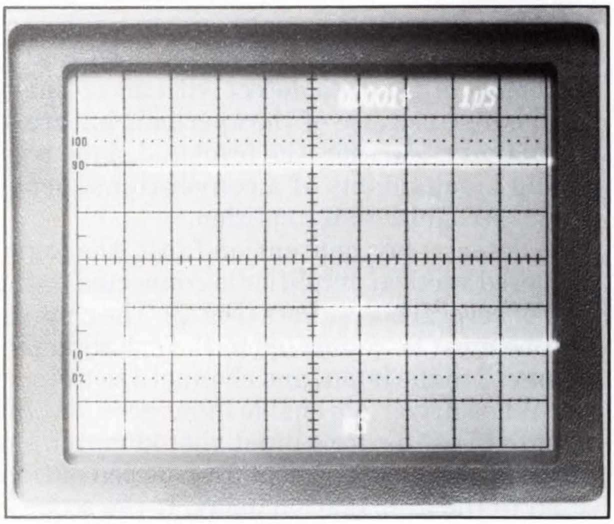
To detect a bus contention fault, the logic-triggered vertical amplifier is connected to the first of several bus drivers (Fig. 2). The channel 1 probe must be connected to the enabling pin, channel 2 to the input, and channel 3 to the output. When driver A's enable input goes low, the signal at that device's input should match the signal at the output, except for a period of time equal to the propagation delay. If the scope is set to trigger when those conditions are not met—that is, when the input and output do not match—it is easy to determine if some other driver on the bus is overpowering the first's output.

If all measurements appear to be within acceptable limits but bad data is still coming over one of the system's 16 data lines, the investigation continues with a search for low-amplitude pulses or those that only reach half-logic levels.

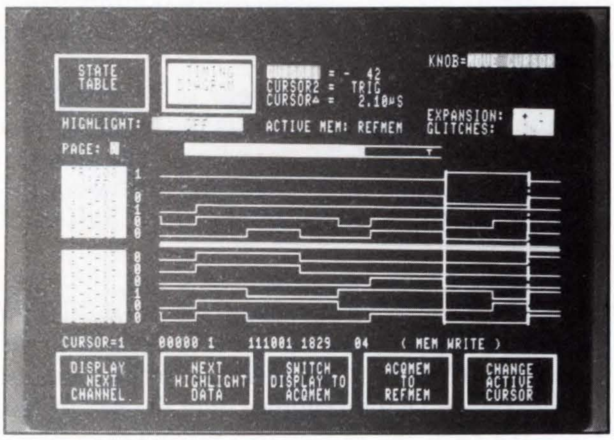
Elusive errors in a logic system, low-amplitude pulses are not recognized as valid logic levels and as a result do not trip conventional analyzer triggers. Contributing to the problem are ordinary scope triggers, which cannot distinguish between pulses in a pulse train. To be discerned, a pulse must have a higher-than-normal amplitude.

A split personality

Because all four amplifier channels can be assigned a distinct threshold recognition level, the dual-threshold triggering scheme of the vertical amplifier helps find low-amplitude pulses or half-logic levels. To locate and trigger on a low-amplitude TTL pulse, the channel 1 and channel 2 probes are connected to the same suspect point. Channel 1's switching threshold is set for 2 V and channel 2 to 0.8 V. Setting the trigger switch to **NOT CH1 AND CH2** causes the scope to monitor the data line, looking for a pulse that is less than 2 V—that is, NOT CH1—and greater than 0.8 V—NOT Ch2 (Fig. 3).



4. The vertical amplifier snares a low-amplitude pulse out of a busy data stream.



5. The logic analyzer's ability to display pretriggering data comes to the fore in pinpointing an intermittent fault. When a low-amplitude pulse is detected by the scope, it sends a trigger pulse to the logic analyzer to initiate data acquisition. The events leading up to the scope trigger are displayed on the analyzer's screen.

The oscilloscope's time base must be set to normal-trigger annd positive-slope (+Slope) positions so that it will trigger on the output of the vertical amplifier. Because the same signal is present on channels 1 and 2, only one channel need be displayed to indicate the trigger function.

That function monitors, in turn, each of the 16 data lines, checking for a low-amplitude pulse. In the example, the scope displays that pulse (Fig. 4), indicating the line carrying the bad data but not yet the reason for the bad data's occurrence. The logic analyzer aids in the final task.

Scope serves the analyzer

Because a logic analyzer can share pretriggering information with an oscilloscope, it can easily determine which peripheral device was controlling the bus before, during, or after the error occurred. With that information, a short software loop can be written that will reproduce the conditions that cause the error.

An appropriate test setup feeds the vertical amplifier's trigger-out pulse to the analyzer to initiate data acquisitions. Because of the intermittent nature of the fault, the user may spend considerable time in a "babysitting" mode. But at the moment the scope detects a low-amplitude pulse, the logic analyzer grabs and displays the condition or word on the data bus, including the events leading up to the trigger (Fig. 5).

Narrowing the problem area often pinpoints a particular integrated circuit that is active on the data line at the exact moment bad data appears. The IC itself might have to be replaced or a close inspection might show a defective pin-socket connection. For instance, a loose ground pin can cause the low-level pulse, a tiny solder or copper bridge between pc-board traces could possibly drag down a signal's amplitude. All of those conditions are easily uncovered by the joint troubleshooting effort of an oscilloscope, vertical amplifier, and logic analyzer. □

How useful?	**Circle**
Immediate design application	556
Within the next year	557
Not applicable	558

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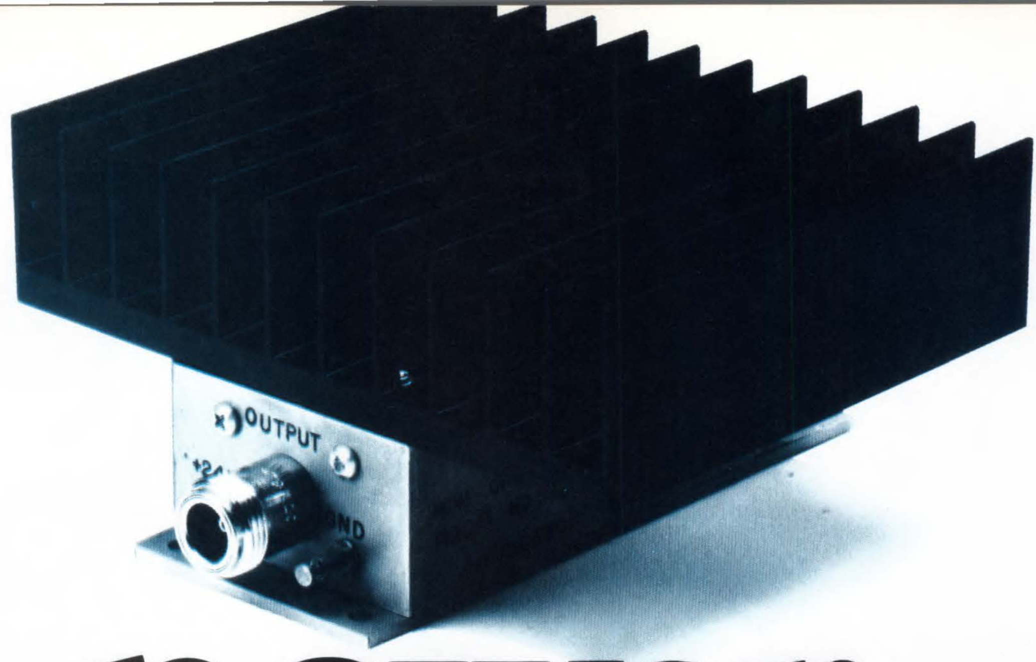
CIRCLE 182



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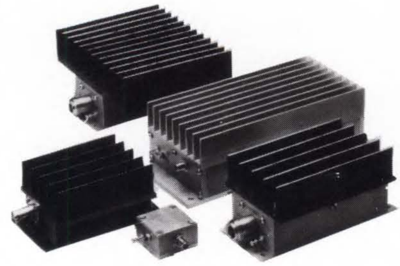

Model No.	Freq. MHz	Gain dB	Gain Flatness dB	Max. Power Output 1dBm Compression	Noise Figure dB	Intercept Point, Typ. 3rd Order	DC Power Voltage	DC Power Current	Price $ Ea.	Qty.
ZHL-32A	0.05-130	25 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-3A	0.4-150	24 Min.	±1.0 Max.	+29.5 dBm Min.	11 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-1A	2-500	16 Min.	±1.0 Max.	+28 dBm Min.	11 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-2	10-1000	15 Min.	±1.0 Max.	+29 dBm Min.	18 Typ.	+38 dBm	+24V	0.6A	349.00	(1-9)
ZHL-2-8	10-1000	27 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.65A	474.00	(1-9)
ZHL-2-12	10-1200	24 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.75A	599.00	(1-9)
ZHL-1-2W	5-500	29 Min.	±1.0 Max.	+33 dBm Min.	12 Typ.	+44 dBm	+24V	0.9A	495.00	(1-9)
ZHL-42	700-4200	30 Min.	±1.0 Max.	+29 dBm Min.	7.5 Typ.	+38 dBm	+15V	0.69A	895.00	(1-9)
ZHL-7-2W	600-800	28 Min.	±1.0 Max.	+33 dBm Min.	12 Typ.	+43 dBm	+24V	0.9A	525.00	(1-9)
ZFL-2000	10-2000	20 Min.	±1.5 Max.	+17 dBm Min.	7 Typ.	+30dBm	+15V	0.1A	179.00	(1-9)

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CIRCLE 183

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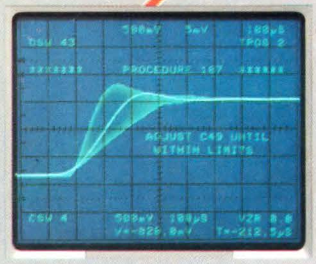
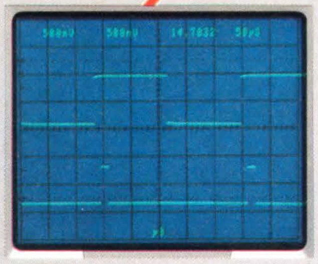
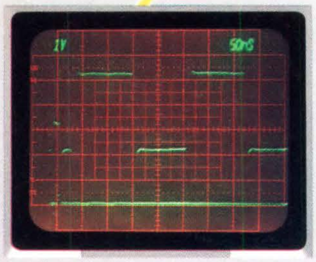


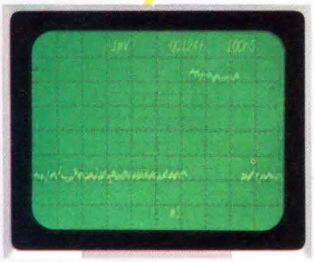
Envelope Mode. Displays upper and lower tolerance limits to simplify production testing and calibration. **System:** R7603 with 7D20 Programmable Digitizer.



Counter/Timer. Oscilloscope-controlled counter/timer permits measurements to counter accuracy on displayed waveforms. **System:** R7603 with 7D15 Universal Counter/Timer.

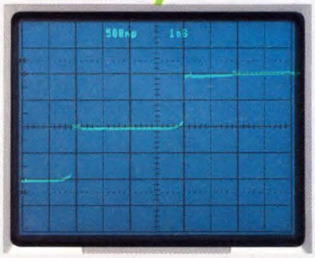


Glitch Capture Application. Unique logic triggering solves problems caused by abnormal pulses. **System:** 7834 with 7A42 Logic-Triggered Vertical Amplifier, 7D11 Digital Delay Unit.



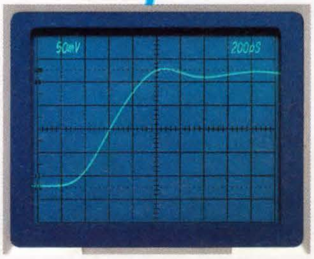
Differential Measurements. High gain differential amplifier captures 5mV signals. **System:** 7834 with 7A13 Differential Comparator Amplifier.

THE ANSWER
BY ANY MEASURE

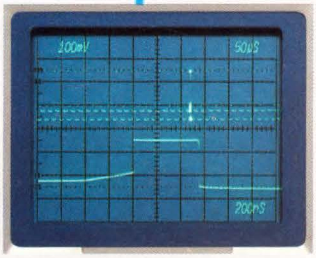


Time Domain Reflectometry. Open transmission line reflects pulse; time of reflection represents the electrical length of line. **System:** 7854 with 7S11 Sampling Unit, 7S12 TDR/Sampler.

Waveform Processing. Keystroke programming enables user to design measurement routines tailored to individual tests or experiments. **System:** 7854 with Waveform Calculator Keyboard.



Single Shot Measurements. Unmatched writing rate of 20 cm/ns provides bright display even at 200 ps/div. **System:** R7103 with 7A29 1 GHz Amplifier, 7B10 Time Base.



Microchannel Plate CRT. Normalizes intensity so both low and high rep rates can be viewed simultaneously. **System:** R7103 with 7A29 1 GHz Amplifier, 7B92A Dual Time Base.

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CIRCLE 185

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UNITED TECHNOLOGIES MOSTEK

CIRCLE 186

A-d converter makes speed/accuracy tradeoffs under software control

An analog-to-digital converter lets engineers select, in real time, through software, the combination of accuracy and resolution that is needed. Designed to work in tandem with a microprocessor, the TSC5000, from Teledyne Semiconductor, is a dual-slope integrating converter that can operate anywhere from 14 bits of resolution at 5 conversions/s down to 8 bits at 400 conversions/s. The actual maximum resolution of the device is 4½ digits, or 1 part in 20,000, in which case the nonlinearity is 0.0025%.

Fabricated in CMOS, the part has all the necessary components to perform dual-slope conversion, including an input buffer, an integrator whose parameters are controlled by externally attached components, switches, and two comparators.

To perform a conversion, a microprocessor switches the input signal into the integrator to charge it for a span of time, then switches in an opposite-polarity voltage. That slowly discharges the integrator down to zero, at which point an interrupt signal is sent to the microprocessor.

The microprocessor measures the time to charge up and discharge the integrator and calculates the digital value from the duration. Increasing the time the signal to be measured is applied to the integrator increases the number of bits of resolution, but also the conversion time.

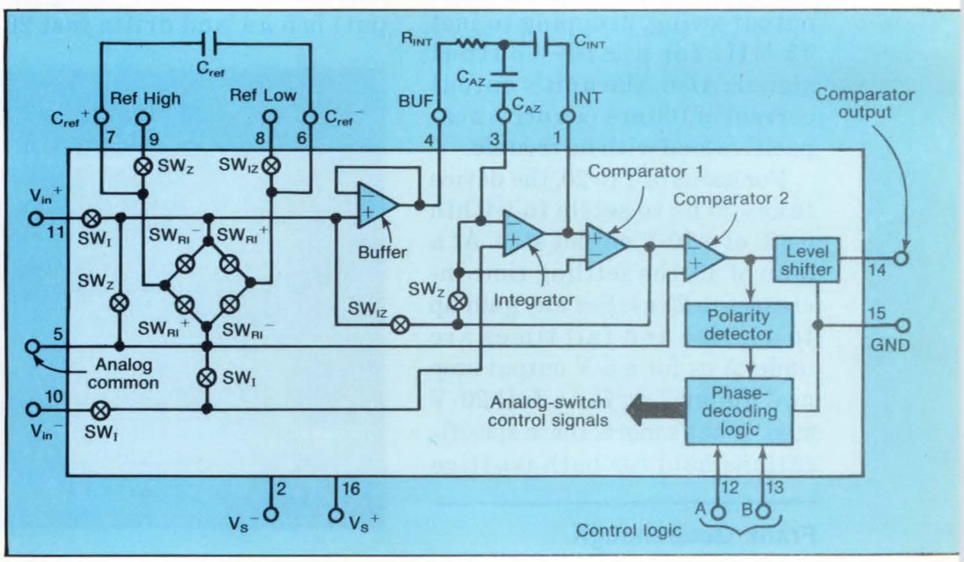
The device accepts four commands from the microprocessor. A Zero command resets the integrator. An Autozero command calibrates the device so that it will give a zero digital reading for a zero input. Lastly there is a command that switches the signal to be measured into the integrator and one that switches the voltage reference into the integrator.

The converter has a differential input so that measurements can be made in the presence of heavy common-mode noise. It handles inputs in the range of +4 to −4 V, converting them with a sensitivity of 100 μV. Supply voltages of ±5 V are required, each drawing 1.5 mA.

Available in plastic or ceramic 16-pin packages for the commercial and industrial temperature ranges, respectively, the chip sells for $5.20 and $6.80 in 100-unit quantities.

Teledyne Semiconductor, 1300 Terra Bella Ave., Mountain View, Calif. 94043; (415) 968-9241.

CIRCLE 319



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ANALOG

Low-cost hybrid op amp slews at 3000 V/μs, reaches beyond 100 MHz

By combining small-outline-packaged devices with thick-film hybrid technology, an ultrafast wideband operational amplifier sells for only $49 each in single-unit quantities and yet outperforms devices costing up to five times as much. Made by Comlinear, the CLC300 slews at 3000 V/μs and extends its small-signal bandwidth to beyond 100 MHz at a closed-loop gain of one. Moreover, that bandwidth drops to only 85 MHz at a gain of 10. Additionally, the unit's small-signal response remains flat to within ±0.5 dB for any gain of up to 45 MHz.

Reflecting its ultrafast slew rate, the op amp's power 3-dB bandwidth is 65 MHz for a ±5-V output swing, dropping to just 45 MHz for a ±10-V output signal. Also, the unit's output current of 100 mA can drive a capacitive load with no trouble.

For gains of 1 to 20, the device takes 20 ns to settle to within 0.8% of a 10-V output step. At a gain of 40, the settling time increases to 25 ns. For any gain up to 40, rise and fall times are under 5 ns for a 5-V output step and under 7 ns for a full 20-V step. What's more, these specifications hold for both positive and negative output steps and for both inverting and noninverting amplifier configurations.

In addition, the device's phase and noise performance are very respectable. The op amp shifts the phase of linear signals by less than 2°/MHz. For gains of up to 40, the deviation from linear phase is only 5° from dc all the way out to 45 MHz. Broadband noise is held to 4 μV between 10 Hz and 1 MHz, increasing to 30 μV at 85 MHz.

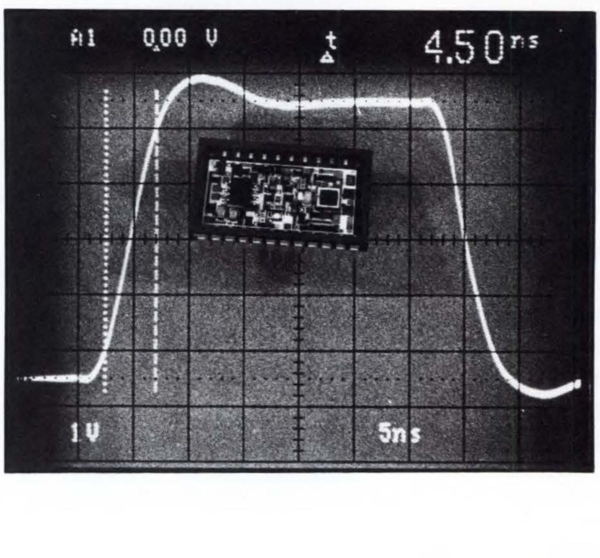
Like most ultrafast amplifiers, the hybrid sacrifices a little performance in the case of dc specifications. Its offset voltage is 10 mV, which drifts but 25 μV/°C. Similarly, its bias current (at the noninverting input) is 5 μA and drifts just 20 nA/°C. At the inverting input, offset voltage drift rises to 50 nV/°C and offset bias drift to 25 μA/°C. The thermal resistance of the case in still air (θ;) is 25°C/W.

Other specifications include a respectable common-mode rejection ratio of 60 dB. For such a fast op amp, current drain is a low 25 mA from a dual ±15-V supply.

The op amp is housed in a 24-pin double-width ceramic DIP and priced at $49 apiece in small quantities and $39 each in lots of 100. Small quantities are available from stock.

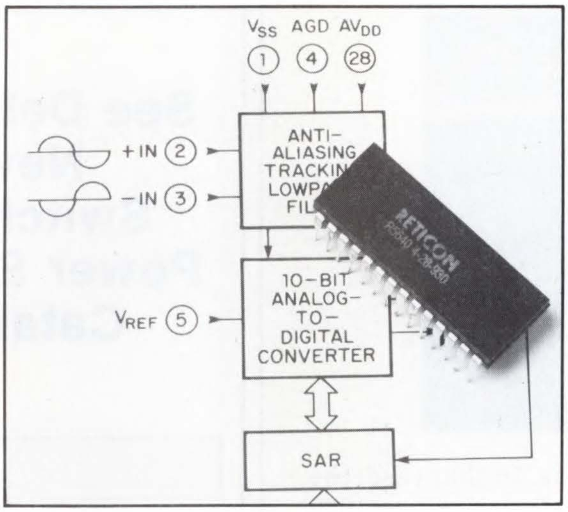
Comlinear Corp., 2468 E. 9th St., Loveland, Colo. 80537; Wayne Lonowski, (303) 669-9433.

CIRCLE 307



Frank Goodenough

A-d converter chip carries its own filter



For the first time a monolithic a-d converter does not require a supporting anti-aliasing filter chip. The RT5640, a 10-bit device from EG&G Reticon, incorporates a high-performance switched-capacitor filter that is tunable over the range of 20 Hz to 15 kHz (ELECTRONIC DESIGN, Sept. 6, p. 205). Thus it serves handily the needs of 8- and 16-bit microprocessors undertaking the complex signal processing necessary for such applications as speech recognition and sonar.

It also integrates a sample-and-hold circuit and has both serial and parallel outputs—one of only a few a-d chips to do either. Its sampling rate can vary from 20 Hz to 40 kHz, and its conversion time from 25 μs to 50 ms, by varying the frequency of an input clock.

The filter, a seventh-order elliptical low-pass circuit, has 0.2 dB of passband ripple and a stopband rejection ratio of more than 60 dB. In addition, mask changes can be made for different filter characteristics.

The converter's 10-bit output comprises a sign bit and 9 magnitude bits. The chip also generates an interrupt signal after a conversion is complete, and a microprocessor can keep reading the converted value until the next conversion is complete.

The input signal must be between +3.5 to −3.5 V. Supply requirements are ±6 V, and the current drain is 20 mA for each voltage.

The part is available immediately in a 28-pin plastic package for the commercial temperature range. It sells for $22 in 100-piece quantities.

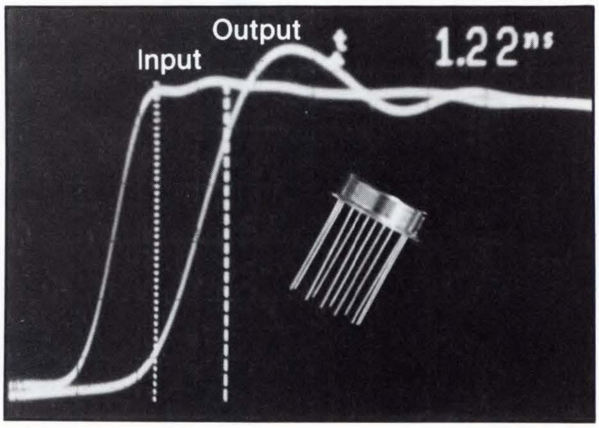
EG&G Reticon, 345 Potrero Ave., Sunnyvale, Calif. 94086; (408) 738-4266.

CIRCLE 320

Curtis Panasuk

ANALOG

Unity-gain buffer slews at 2500 V/μs



Designed for unity-gain applications, the EL2004 voltage buffer and line driver can slew at 2500 V/μs and offers a bandwidth of 350 MHz. The hybrid circuit, developed by Elantec, thus offers a higher-performance solution to problems previously solved by discrete-component circuits or hybrids such as the LH0033, for which it can serve as a drop-in upgrade or replacement. Typical applications include coaxial-cable and video-line drivers, high-speed sample-and-hold circuits, and flash-converter buffers.

Additionally, when operated from $\pm$15-V supplies, the buffer has a signal rise time of just 1 ns typical and 2.5 ns worst case, with a 100-Ω load. The typical settling time to within 1% is 6 ns.

The circuit, however, can also operate from $\pm$5-V power supplies and has a second set of guaranteed specifications at those levels. In that case, the slew rate slows down to 1000 V/μs typical, the rise time increases to 1.7 ns typical, and the settling time grows to 8 ns.

With either $\pm$15- or $\pm$5-V supplies, the buffer can deliver up to 100 mA into a load.

When operated at the higher supply levels, the buffer draws 24 mA maximum, and its actual voltage gain with a $\pm$10-V input swing is 0.96 minimum with a 1-kΩ load and 0.90 with a 100-Ω load. The military version has minimum gain values of 0.97 and 0.92, respectively.

Available in a commercial version as well, the circuit comes in an eight-lead TO-8 package, and a leadless chip carrier can be ordered. Samples are available from stock; in 100-unit quantities, the buffer costs \$20.85 or \$45.04 for the industrial and military (883B) versions, respectively.

Elantec Inc., 1996 Tarob Court, Milpitas, Calif. 95035; Dave Long, (408) 945-1323.

CIRCLE 309

Dave Bursky

ANALOG

Chip detects pulses in Winchester drives

For use in Winchester disk drive systems, the DP8464 disk pulse detector combines analog and digital circuitry to detect the amplitude peaks of signals received from the read/write amplifier. When changes in the magnetic flux occur, it translates the analog signals into digital pulses. The DP8464 is designed to reside in the disk drive with its output connected to the industry-standard DP8460 data separator.

Programmable features of the chip include automatic gain-control response, gate-channel filter response, time-channel filter response, comparator hysteresis, and data output pulse width. The DP8464 is currently available in a 300-mil-wide 24-pin DIP; a 28-pin plastic chip carrier is planned for 1985.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; (408) 721-5000. $27.50 (100 units).
CIRCLE 323

Tiny 16-bit converter fits inside resolver

Occupying a mere 1 inch square, a 16-bit digital-to-resolver converter fits inside a size 15 (or larger) resolver. Its small size, combined with an angular accuracy of up to 1 arc-minute, makes the HDR2406 suitable for many industrial applications. Matched thin-film resistors ensure angular accuracy of the sine and cosine outputs over any of the converter's entire operating temperature ranges (commercial, industrial, or military).

Although the HDR2406 is designed to interface with 8- and 16-bit microprocessors, it can be used in conventional applications without any external components or additional connections. It has a pin-programmable reference input of 115 or 26 V rms and requires a ±15-V dc power supply.

Natel Engineering Co., 4550 Runway St., Simi Valley, Calif. 93063; (805) 581-3950. From $230; stock to six weeks.
CIRCLE 324

V-I converter aims at industrial applications

Powered by any supply from 12 to 32 V, the Model 930/MK298 voltage-to-current converter has a quiescent current drain of less than 50 mA and an input impedance of 1 MΩ. The scale factor with a 10-V input is 5 mA/V, which is accurate to within 1%. A potentiometer adjusts the minimum output level of 0.5 mA to 4 mA, providing a "live" zero. Input ranges of less than 10 V are accommodated by substituting one resistor. The converter has a full output current range of 0.5 to 50 mA; the output compliance voltage is 0 to 27 V.

The 930/MK298 is packaged on a plug-in card including a connector and built-in card guides. It is compatible with standard Calex system components, such as instrumentation amplifiers and strain gauge modules.

Calex Manufacturing Co. Inc., 3355 Vincent Road, Pleasant Hill, Calif. 94523; (415) 932-3911. $124; stock.
CIRCLE 325

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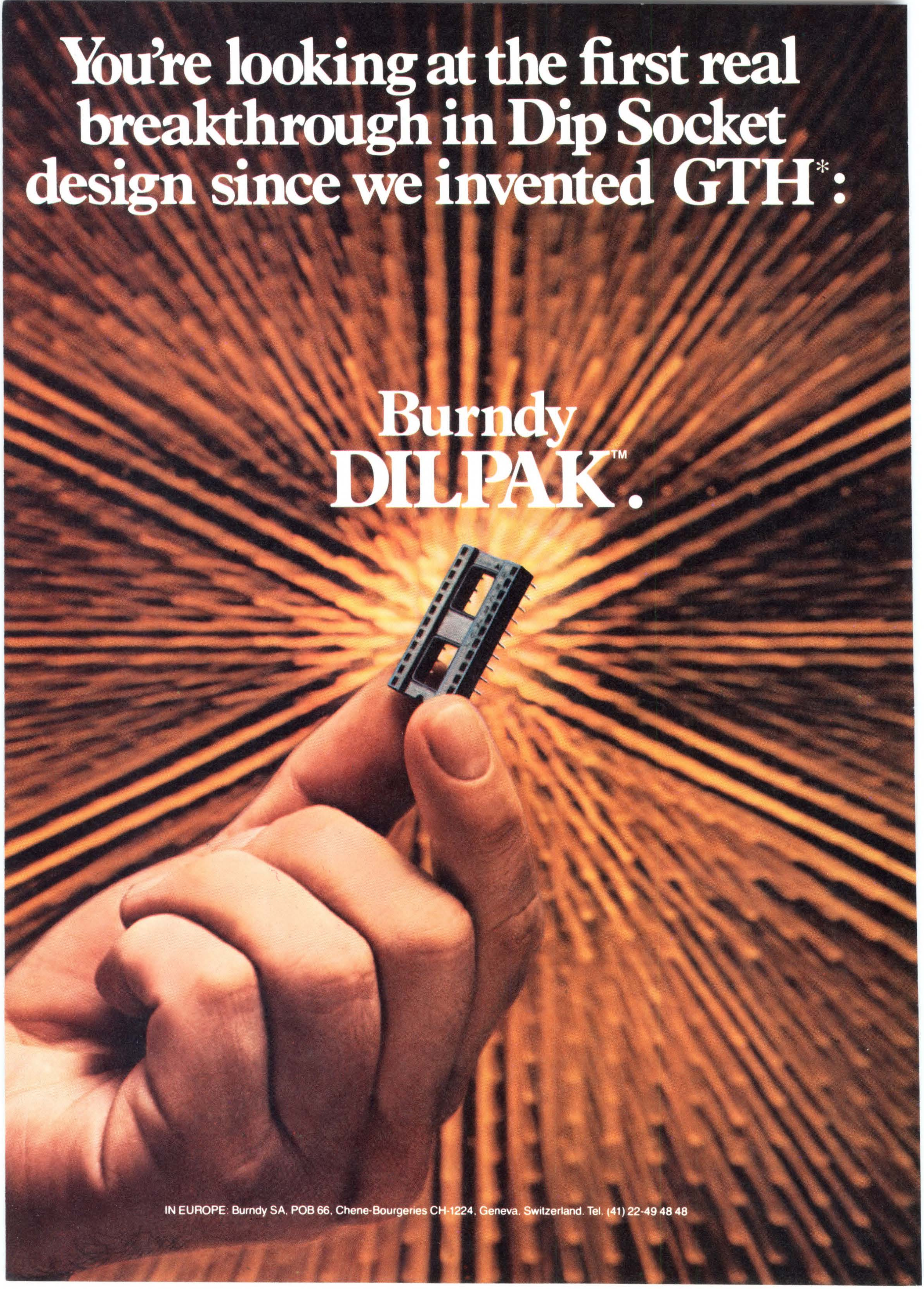
CIRCLE 116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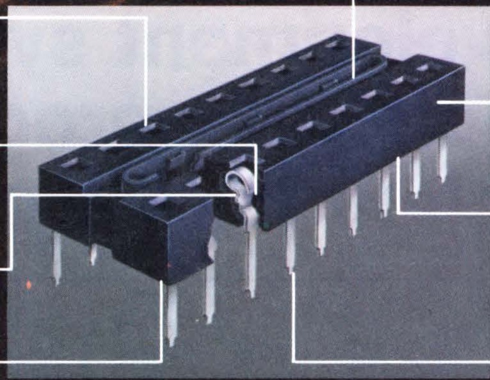

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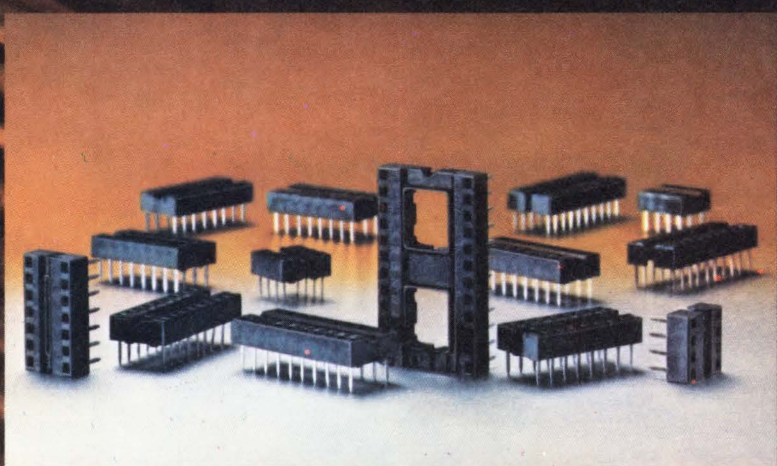
CIRCLE 193



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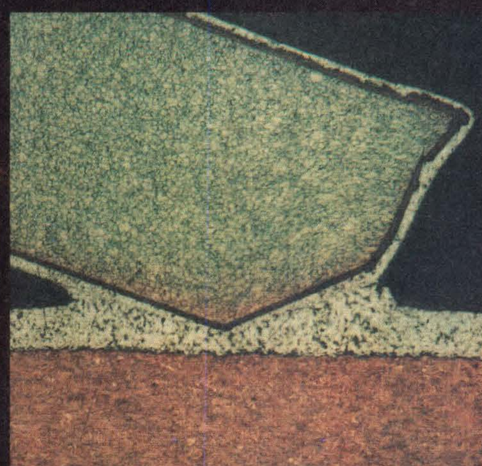

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INTERNATIONAL NEW PRODUCTS

68000 development system runs multiple Unix programs in real time for 4 users

The Eurosys 16 development system for designs based on the 68000 microp ocessor family enables as many as four persons to each run several programs simultaneously in real time. The modular unit, from Euroka OY, runs under the new OS-9/68000, a Unix-compatible real-time, multi-user, multitasking operating system. It accepts high-level languages, like C, Basic, Pascal, and Cobol, as well as assembler.

The system lets each user run several programs simultaneously in the background mode while he or she is editing and developing a program in the foreground mode.

In addition, once the program or programs have been developed, the unit, being based on single-Eurocard modules, can form the heart of the target system itself, for such equipment as graphics workstations, measurement computers, and robot controllers. It has 13 free slots for expansion cards.

The system uses an 8- or 10-MHz 8/32-bit 68008 processor and 256 kbytes of dynamic RAM. It has four RS-232-C interfaces having speeds of 150 to 19,200 bauds and a SASI (Shugart Associates Systems Interface) link that connects to a 20-Mbyte Winchester and a 500-kbyte floppy-disk drive. A QIC-02 interface allows four streaming-tape drives to be connected as well.

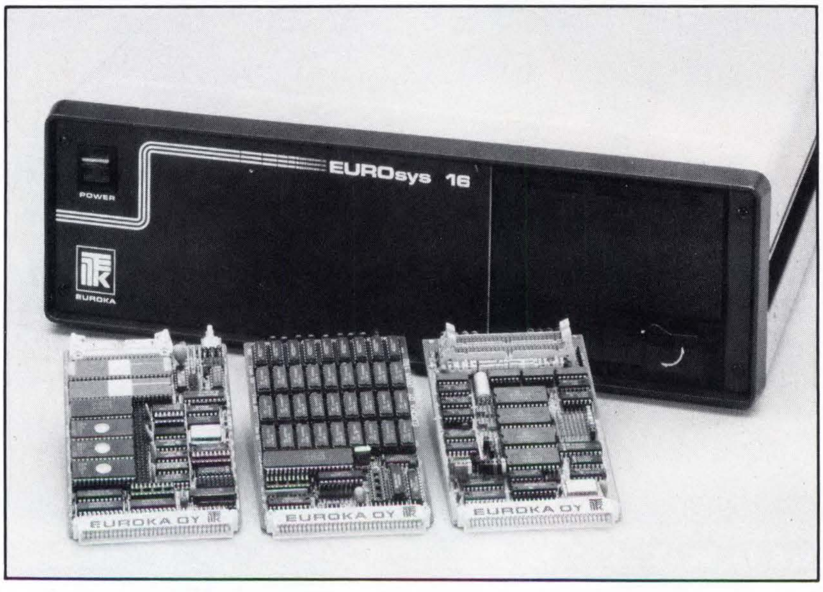
The operating system may be easily customized, as it consists of a collection of self-linking, independent modules (e.g., kernel, disk file manager, and command interpreter). Its hierarchical structure simplifies the organization of the application software, and the tree structure of its file system makes file manipulation very straight forward. It has multilevel prioritized interrupt handling and accepts user-defined interrupts.

Multiple tasks can share common program or data modules, and semaphores are used for process coordination. Because all time-critical sections of the operating system are coded in assembly language, the system response time is only milliseconds.

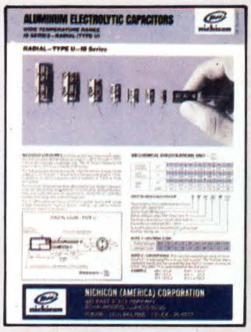
The unit is 140 by 450 by 450 mm, consumes a maximum of 0.7 A from a 240-V supply, and costs £5600.

Euroka OY Elektroniikka, Hameentie 155 C 52 a, 00560 Helsinki 56, Finland; +358 0 799522; Telex: 125490 euro sf.

CIRCLE 505



Mitch Beedie



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Miniature Aluminum Electrolytic Capacitors

Series Type	Feature	Operating Temp. (°C)	D.C. Leakage Current (μA)	Construction	Rated Voltage Range (V.DC)	Capacitance Range (μF)	Standard Capacitance Tol. (%)
LB	• Standard Size • General Purpose	−40~+85	0.03CV (A*) (4μA Min.)	Radial (U) Axial (T)	6.3~100 6.3~100	0.1~10,000 0.47~33,000	±20 (M) ±20 (M)
VX	• Smaller Standard Size • High CV Density • General Purpose	−40~+85	0.01CV (B*) (3μA Min.)	Radial (U)	6.3~100	0.47~10,000	±20 (M)
HU	• High Voltage	−25~+85	0.06CV+10 (C*)	Radial (U) Axial (T)	160~450 160~450	1~100 1~470	−10~+50 (T) −10~+50 (T)
BU	• High CV Products	−40~+85	0.02CV (C*) (3000μA Max.)	Radial (U)	6.3~100	1,000~3,300	±20 (M)
VS	• Low Profile Design	−40~+85	0.01CV (B*) (3μA Min.)	Radial (U)	6.3~50	0.1~4,700	±20 (M)
KB	• Low Leakage • Tantalum Replacement	−40~+85	0.002CV (B*) (0.4μA Min. – U) (1μA Min. – T)	Radial (U) Axial (T)	6.3~100 6.3~100	0.1~100 0.47~100	±20 (M)/±10 (K) ±20 (M)/±10 (K)
SA	• Super Miniature (7mm Height) • Tantalum Replacement	−40~+85	0.01CV (B*) (3μA Min.)	Radial (U)	6.3~50	0.1~100	±20 (M)
SL	• Super Miniature (7mm Height) • Tantalum Replacement • Low Leakage	−40~+85	0.002CV (B*) (0.4μA Min.)	Radial (U)	6.3~50	0.1~100	±20 (M)
SP	• Super Miniature (7mm Height) • Non-Polarized	−40~+85	0.05CV (B*) (10μA Min.)	Radial (U)	6.3~50	0.1~47	±20 (M)
MA	• Ultra-Miniature (5mm Height) • Tantalum Replacement	−40~+85	0.01CV (B*) (3μA Min.)	Radial (U)	4~50	0.1~220	±20 (M)
EB	• Non-Polarized	−40~+85	0.01CV (C*) (5μA Min.)	Radial (U) Axial (T)	6.3~100 6.3~100	0.47~1,000 0.47~3,300	±20 (M) ±20 (M)

Miniature High Temperature Capacitors

Series Type	Feature	Operating Temp. (°C)	D.C. Leakage Current (μA)	Construction	Rated Voltage Range (V.DC)	Capacitance Range (μF)	Standard Capacitance Tol. (%)
PC	• Standard Size • Wide Temp. Range • General Purpose	−55~+105	0.03CV (A*) (4μA Min.)	Radial (U)	6.3~100	0.47~10,000	±20 (M)
		−40~+105	0.03CV (A*) (4μA Min.)	Axial (T)	6.3~100	0.47~10,000	±20 (M)
BB	• High Temperature • High Reliability	−40~+105	0.002CV (C*) (2μA Min.)	Radial (U) Axial (T)	10~100	0.47~1,000	±20 (M)
BE	• High Temp. (+125°C) • High Reliability	−40~+125	0.002CV (C*) (2μA Min.)	Radial (U) Axial (T)	10~50	0.47~470	±20 (M)
ST	• High Temp. (+105°C) • Super Miniature (7mm Height)	−40~+105	0.01CV (B*) (3μA Min.)	Radial (U)	6.3~50	0.1~100	±20 (M)

Miniature Special Application Capacitors

Series Type	Feature	Operating Temp. (°C)	D.C. Leakage Current (μA)	Construction	Rated Voltage Range (V.DC)	Capacitance Range (μF)	Standard Capacitance Tol. (%)
PX	• Low ESR • Smaller Package • High Ripple	−55~+105	0.03CV (A*)	Radial (U)	6.3~63	22~2,200	±20 (M)
TM	• For Timing Circuits • Very Stable at High Temp.	−40~+85	0.001CV+1 (B*)	Radial (U)	10~50	1~470	±20 (M) ±10 (K)
HA	• High Frequency, High Ripple	−25~+85	100 (C*)	Radial (U)	25	2.2~10	±10 (K)

Can Type Lytics

Series Type	Feature	Operating Temp. (°C)	D.C. Leakage Current (μA)	Construction	Rated Voltage Range (V.DC)	Capacitance Range (μF)	Standard Capacitance Tol. (%)
HL/LL	• Snap-in Terminal for P.C.B. Mount	−40~+85	$3\sqrt{CV}$ (C*)	Can (L)	16~100	470~22,000	−10~+30 (Q)
UB	• Snap-in Term., P.C.B. Mount • Smaller Size	−40~+85	$3\sqrt{CV}$ (C*)	Can (L)	16~100	1,000~15,000	±20 (M)
NW/NK/NS	• Computer Grade	−25~+85	$3\sqrt{CV}$ (C*) (10mA Max.)	Can (L)	6.3~450	120~1,000,000 (1F)	−10~+50 (T)
PS [LR]	• Snap-in Term, P.C.B. Mount • For Switching Regulators • [Smaller Size]	−40~+85 (160~250) −25~+85 (350~450)	$3\sqrt{CV}$ (C*)	Can (L)	160~450 [400]	47~1,000 [47~330]	±20 (M)
PK	• High Ripple, Switching Reg. • Extended Temp. Range • Snap-in Term., P.C.B. Mount	−40~+105	$3\sqrt{CV}$ (C*)	Can (L)	200~250	150~1,000	±20 (M)
GM [GF]	• High Ripple, Switching Reg. • Extended Temp. Range • Snap-in Term., P.C.B. Mount • [Smaller Size]	−40~+105 (160~250) −20~+105 (400)	$3\sqrt{CV}$ (C*)	Can (L)	160~400 [400]	47~1,000 [47~330]	±20 (M)
FL	• Low Profile (20mm Height) • Snap-in Term., P.C.B. Mount • For Switching Regulators	−40~+85	$3\sqrt{CV}$ (C*)	Can (L)	160~250	82~270	±20 (M)

Class III Semiconductive Ceramics

Series Type	Temperature Characteristics	Rated Voltage (V. DC.)	Capacitance (μF)	Standard Capacitance Tolerance	Insulation Resistance (MΩ)	Dissipation Factor (at 1kHz)
HET	Y5T	12	0.022~0.47	±20% (M) +80~−20% (Z)	12V: 0.022~0.1μF −1 Min. 0.22μF −0.5 Min. 0.33μF −0.33 Min. 0.47μF −0.25 Min. 25V: 0.01~0.22μF −1,000 Min. 0.47μF −500 Min. 50V: −1,000 Min.	12V: 7.0% Max. 25V: 5.0% Max. 50V: 5.0% Max.
		25	0.01~0.1			
		50	0.01~0.1			
HEV	Y5V	12	0.047~0.47			
		25	0.022~0.47			
		50	0.01~0.1			

Polyester Capacitors

Series Type	Rated Voltage (V. DC)	Capacitance (μF)	Standard Capacitance Tolerance	Insulation Resistance	D.F.
QYA	100	0.001~0.47	±5% (J), ±10% (K), ±20% (M)	9.00MΩMin.	1.0% Max. at 1kHz
QXM (Radial)	250, 400, 630	0.01~2.2	±5% (J), ±10% (K), ±20%(M)	≤0.33μF-9.00 MΩMin.	1.0% Max. at 1kHz
QAM (Axial)	250, 400, 630	0.15~10	±5% (J), ±10% (K), ±20% (M)	>.033μF-3,000 MΩMin	
QAL	125V. AC	0.0047~.022	±10% (K), ±20% (M)	9,000MΩMin. at 100 V. DC 1 Min.	1.0% Max. at 1kHz

(A*) = Leakage Current after 1 minute (B*) = Leakage Current after 2 minutes (C*) = Leakage Current after 5 minutes

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CIRCLE 194

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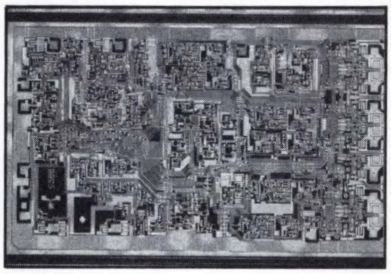
8086/8088 peripherals draw 40% less current

A series of second-generation peripherals for the 8086 and 8088 microprocessor families consume 40% less current than the types that they replace: The circuits take just 90 to 140 mA, instead of the 160 to 230 mA needed by their equivalents. Designed using standard cells [ELECTRONIC DESIGN, Dec. 27, p. 69 or 69E] and made with a two-layer-metal buried-collector process, the range consists of a clock generator-driver, a bus controller, and octal latches, and bus transceivers.

The SAB 8288A bus controller consumes a maximum of 140 mA. It decodes the three outputs from the system microprocessor



and generates command and control timing for the bus. A strapping option on the chip configures it for use with a multimaster system bus and separate I/O bus.

The SAB 8284B/SAB 8284B-1 clock generator and driver consumes a maximum of 110 mA and uses a crystal or TTL frequency source to generate an 8- or 10-MHz system clock, respectively, for the 8086 family devices.

The range is completed by the SAB 8282A noninverting and SAB 8283A inverting octal latches and the SAB 8286A noninverting and SAB 8287A inverting octal bus transceivers. These devices each have a maximum power consumption of 90 mA.

All of the ICs require a single 5-V supply, and all are housed in 20-pin plastic DIPs, except for the clock generator-driver, which comes in an 18-pin DIP.

Siemens AG, Zentralstelle für Information, Postfach 103, D-8000 Munich 1, West Germany; (089) 2340; Telex: 52 100-25.

CIRCLE 502

V.23 modem fits on a single chip

Besides modulation and demodulation circuits, a single chip includes all the control and timing functions needed to implement a CCITT V.23 modem having a baud rate of 75, 600, or 1200 bauds.

The XV9001 from Plessey Semiconductors incorporates all necessary switched-capacitor filtering for frequency-shift-keyed data, including anti-aliasing and bandpass filters for the input data stream and smoothing filters for the output data stream. It generates six FSK frequencies between 390 and 2100 Hz for the different baud rates, and all frequencies are accurate to within ±2 Hz. The maximum response time to a change of input data is 5 μs.

The chip provides delays for the Clear to Send (CTS) and Carrier Detect (CD) signals. These lines can be overridden by externally generated signals, allowing the IC to be interfaced with members of the PIC1650 series of microprocessors.

The device can be used with either two- or four-wire systems. All data and control inputs and outputs are compatible with TTL and CMOS logic.

The chip, which is encapsulated in a 24-pin DIP, uses a standard, low-cost 3.58-MHz crystal for a frequency reference. Current consumption is typically 20 mA from +5- and −5-V supplies, and the operating temperature range is 0° to 70°C.

Plessey Semiconductors Ltd., Cheney Manor, Swindon, Wilts. SN2 2QW, England; (0793) 36251; Telex: 449637.

CIRCLE 501

Low-cost IC recognizes 16 words

A speech recognition chip costing only about Sw. fr. 15 handles a vocabulary of 16 words. With the HCMOS H6005, from Microelectronic-Marin, trained for a particular speaker, the recognition accuracy is 95%; for speaker-independent use, the accuracy depends on pronunciation.

Besides a couple of resistors and capacitors, a complete system consists of the IC, a low-cost electret microphone, an audio preamplifier, 8 kbytes of PROM, 2 kbytes of RAM, a 32-kHz watch crystal, and an 8-bit microprocessor. Software is available for the Z80 and is being developed for the 6502.

The microprocessor's operating system is held in the PROM. The speaker-independent vocabulary is stored in ROM; speaker-dependent systems require a person to "train" the system before each use, with the words placed in RAM. For larger vocabularies, two ICs can be connected in parallel to a 16-bit microprocessor.

The IC has a seven-channel spectrum analyzer with a frequency range of 150 to 4800 Hz. A switched-capacitor filter on each channel has a variable threshold, and the circuit automatically adjusts to different voice volumes.

The signal from each channel is sampled at 128 Hz; this frequency is generated by an internal oscilllator controlled by an external 32.768-kHz crystal.

The digitized output is placed on a seven-line data bus and passed to the microcomputer at a rate of 896 bits/s. Software held in PROM compares the received signal with that of the words in RAM and selects the nearest word.

The circuit works from a 5-V supply and consumes typically 150 μA. It comes in a 16-pin plastic DIP.

Microelectronic-Marin, CH-2074 Marin, Switzerland; (038) 352121; Telex: 952790 eem ch.

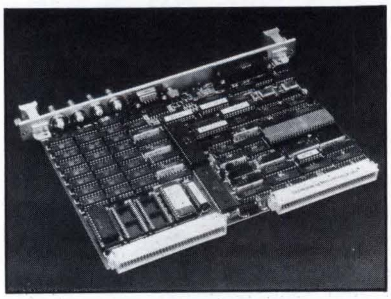
CIRCLE 504

VME graphics board resolves 262,000 pixels

The EFD-GRC1 double Eurocard produces medium-resolution graphics for VMEbus systems. From Thomson-CSF, it uses a 12-MHz EF9367 graphics display processor to produce a 3-bit-deep, 512-by-512- or 512-by-256-pixel noninterlaced scan.

The card has 192 kbytes of video RAM with a typical cycle time of 200 ns—enough to store two complete display pages. It also has 8 kbytes of RAM and 32 kbytes of ROM, both with cycle times of 350 ns.

The board features two display modes, ASCII and vector plotting, plus a fast-writing mode (in which the video output



is turned off while the display is being built up) with an average writing speed of 900,000 dots/s. It holds in ROM 95 eight-by-seven-dot ASCII characters, the sizes of which are programmable from 1 to 16 dots in each direction.

The board has composite video, 525- or 625-line CCIR, and TTL-compatible RGB video outputs, plus a TTL-compatible composite sync line. There is also a serial RS-232 communications interface.

An EF68121 intelligent peripheral controller allows a keyboard and printer to be connected. In addition, a light pen may be optionally connected.

The board accepts supplies of +5, +12, as well as −12 V, with a 1.5-A drain on the 5-V line.

Thomson Semiconductors, Communication Department, Grenoble, 45 Ave. de l'Europe, 78140 Velizy, France; (3) 946-9719; Telex: 204780F.

CIRCLE 503

TREASURES OF THE DEAP.™

Discover the riches of Fujitsu Bipolar PROMs.

Many rewards come to those who explore the mysteries of the DEAP.

Fujitsu's Diffused Eutectic Aluminum Process. Our exclusive programming technology that produces bipolar PROMs of outstanding reliability, access times and programming yields.

The secret of the DEAP lies beneath the surface. The die surface. There below is where we program a Fujitsu PROM cell.

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And because DEAP lets us produce PROMs of greater density, you enjoy the fastest access times around. For example, our 64K PROM at 55 nanoseconds is the fastest in the industry.

But one of the nicest discoveries about our bipolar PROMs is that they're available in quantity. In densities from 2K to 64K. And in a variety of packages.

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FMI Sales Offices. Atlanta 404/449-8539. Austin 512/343-0320. Boston 617/964-7080. Chicago 312/885-1500. Dallas 214/669-1616. Houston 713/784-7111. Minneapolis 612/454-0323. New York 516/361-6565. No. Calif. 408/866-5600. S. Calif. 714/720-9688.

CIRCLE 196

Desktop computers are compatible with PDP-11

Two series of desktop or 5¼-in.-rack-mounted computer systems are both hardware- and software compatible with DEC's PDP-11 minicomputers and suit applications ranging from dedicated single-user workstations to multiterminal systems with 16 users. The 6300 series uses an 11/23 processor, and the 8300 series uses an 11/73 processor. Both series employ DEC's Q-bus and have 256 kbytes of RAM, upgradable to 4 Mbytes, and a 10-, 20-, or 40-Mbyte Winchester disk drive or a 40-Mbyte fixed-removable drive. A 15-Mbyte Plessey CSV streaming-tape system or 48-Mbyte TK25-compatible tape cartridges may be used as backup.

Plessey Peripheral Systems, Burcote Road, Towcester, Northants. NN12 7PF, England; (0327) 51919.

CIRCLE 506

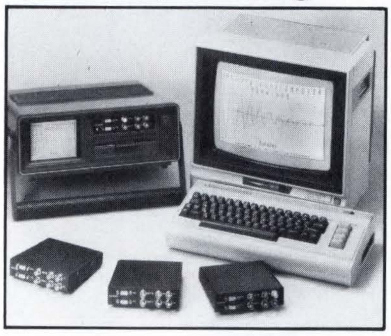
Package links IBM PC to mainframes, minis

The WASP (Workstation Automatic Script Processor) software package enables an IBM PC or compatible personal computer to communicate with IBM mainframes and DEC minicomputers. The package runs on the small machine under the PC-DOS or MS-DOS operating system and has a simple menu-driven user interface. The PC needs a minimum of 128 kbytes of RAM, one floppy-disk drive, and interface hardware for IBM 3270 emulation. With the package, it functions as an ordinary terminal and links to any system including IBM's 4300, 33xx, 30xx, and System 34/36/38, as well as the DEC PDP-11 and VAX computers, that can attach to an IBM 3270 or VT100 terminal. No extra software is needed in the host.

Philips, Data Systems Division, PO Box 523, 5600 AM Eindhoven, the Netherlands; (040) 756943; Telex: 51573.

CIRCLE 507

Interface module gives portable μC analog I/O



An interface module fits into the storage slot of Commodore's portable SX64 computer, allowing the computer to be used for control, data acquisition, and measurement analysis. The ADS (analog-digital system) module may also be used with a Commodore 64 and a separate monitor. It has four analog inputs and two analog outputs, each having a ±10-V range and 12-bit accuracy. There also are four digital, TTL-level inputs and four 100-V, 0.5-A relay contacts. The module samples each input and updates all the outputs—analog, digital, and relay—every 7 ms.

The interface may be programmed using Commodore Basic. It is priced at £500, and a complete SX64 system is available for £1450.

CIL Microsystems Ltd., Decoy Road, Worthing, Sussex BN14 8ND, England; (0903) 210474; Telex: 87515 WISCO G ATT MIC.

CIRCLE 508

4-to-20-mA converter fits inside connection head

A remote conversion unit for potentiometers and sensors fits into standard industrial connection heads and takes its power from the signal voltage. The LP01 standard model is designed for potentiometers with a total resistance of 2 to 5 kΩ, with units for other resistances available on request. It converts the potentiometer setting into a standard 4-to-20-mA signal. A fault in the potentiometer will cause the output signal to fall below 4 mA or to rise above 20 mA.

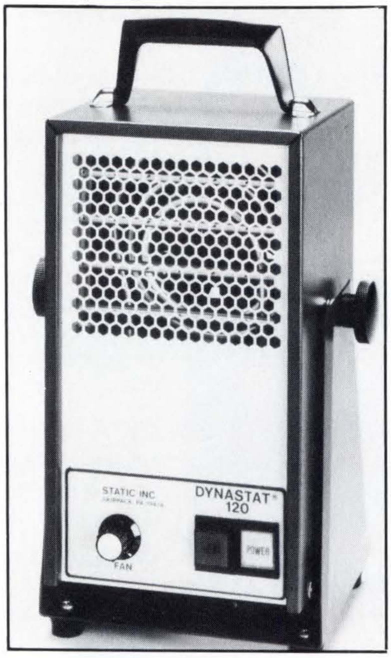
Degussa AG, Postfach 110533, D-6000 Frankfurt 11, West Germany; (069) 218-2860 or 218-2230; Telex: 41222-0 dg d.
fitted in the meter.

CIRCLE 509

NEW PRODUCTS

PACKAGING & MATERIALS

Ionizing air blower employs 100-cfm fan



Smaller and lighter than most units, the Dynastat 120 series of ionizing air blowers incorporates a fixed or adjustable 100-cfm fan that provides a smooth flow of ionized air to control static electricity. Adjustable fan speeds range from 50 to 100 cfm.

An integral heater is available to warm the ionized air for operator comfort. With the heater on, the unit draws 1.3 A—approximately 50% less than comparable blowers. With the heater off, the unit draws only 0.3 A.

The blowers have a primary effective range of approximately three feet and a maximum effective range of up to six feet. The 11-lb units re 6½ in. wide by 5¼ in. deep and stand 11 in. high.

Static Inc., PO Box 80, Skippack, Pa. 19474; (215) 584-9604. From $340 to $440.

CIRCLE 326

PACKAGING & MATERIALS

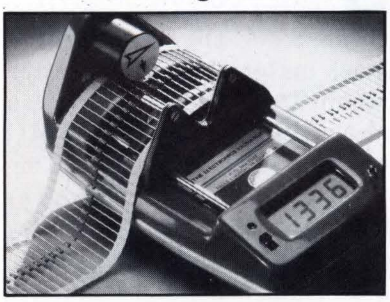
System adds, repairs gold finger contacts

The CRC 1000 gold contact laminating system adds or replaces gold finger contacts on printed circuit boards. Production yields are increased by repairing rejects, and full restoration of traces marred by scratches, corrosion, pits, or voids is accomplished by the lamination of new, precisely etched, polyimide adhesive-backed replacement contacts.

Circuit Repair Corp., 31 Corporate Place-128, Audubon Road, Wakefield, Mass. 01880; (617) 245-1030.

CIRCLE 327

Component counter eliminates guesswork



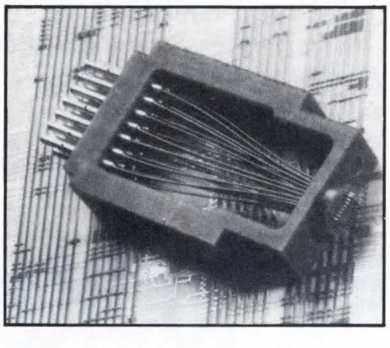
An electronic counter with a four-digit liquid-crystal display counts resistors, diodes, and capacitors that are taped and reeled. The unit, called the Count 2, uses an infrared detection and counting circuit to determine the number of components passed through it. It also allows for forwards or backwards counting. The tape guide is adjustable for any width between 1.8 and 4.6 in. Rechargeable nickel-cadmium batteries allow the Count 2 to operate for 10 hours. A plug-in power supply is also included.

Electronics Exchange, PO Box 2537, Falls Church, Va. 22042; (703) 280-5358. $750.

CIRCLE 328

PACKAGING & MATERIALS

Module allows close-center probing

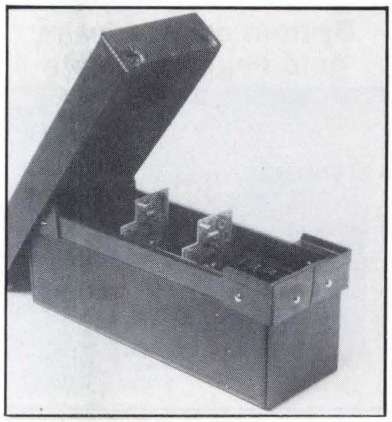


Designed for testing bare substrates on test centers down to 0.010 in., a probe module contains flexible wire contacts in a dedicated housing that matches test points. The wire contacts provide a full travel range of 0.030 in. and have a minimum contact force of 0.5 oz (1.25 oz maximum). The module utilizes an Euler-column probing technique, which can also be used to design and manufacture custom modules to fit a variety of test applications. The maximum contact density is 400 contacts/in.^{2}.

Everett/Charles Contact Products Inc., 700 E. Harrison Ave., Pomona, Calif. 91767; (714) 625-5551.

CIRCLE 329

Conductive totes protect components



Conductote is a corrugated plastic tote that protects sensitive components from electrostatic discharge. Constructed of a carbon-impregnated copolymer, the handling system has a volume resistivity of 10^3 to 10^5 Ω-cm, which is unaffected by long-term use. It complies with DOD 263 specifications for conductive packaging material and MIL-P-82646. All Conductotes are custom-designed to meet users' requirements. Sizes can be as small as 1 square in. or as large as necessary, and there is no minimum order size.

Set Point Paper Co. Inc., 69 Elm St., Foxboro, Mass. 02035; (617) 543-3800.

CIRCLE 330

Chrome substrate optimizes device masks

Suitable for most semiconductor printing applications, a see-through chrome mask material produces better resolution and edge sharpness than iron oxide. The SMC chrome blank is also an improved version of standard see-through types. The transmission, or optical density, of the SMC blank is 2% at 400 nm. Reflectivity is approximately 20% in both the exposure and alignment wavelength ranges.

Balzers Optical Group, 170 Locke Drive, Marlborough, Mass. 01752; (617) 481-9860.

CIRCLE 331

SOFTWARE

Fortran engineering arrives for the IBM PC in full battle dress

Software engineering techniques and tools have been applied to the large computers but are only slowly appearing for personal computers. Designed for the IBM personal computer and compatibles, a full set of integrated software engineering tools for the design, creation, testing, and optimization of Fortran programs, known as the PC Fortran Programming Environment (PC FPE), changes all that.

This tool set, from Softool, is compatible with the company's existing FPEs for larger systems such as the DEC VAX. It may be used as the software basis of a stand-alone Fortran development station or with a larger system (initially the VAX) for development tasks that do not require the host processor's full power. Tasks such as editing, debugging, documentation, and static testing can be offloaded.

Among the tools are a documenter for setting up standards and providing templates; an interface documenter for cross-references and interfaces; a software instrumenter for tracing, debugging, testing, and optimization; a library of existing routines and code for inclusion into new programs; and a preprocessor to supply structured programming constructs for Fortran. Additionally, a communications program can either pass files between the VAX and the PC or let the PC act as dumb terminal for host processing. Also, an easily used interface is featured that includes 12 volumes of on-line tutorials.

The PC FPE supports either the IBM Professional Level or the Microsoft Fortran compiler. Fortran developed on the PC can be uploaded to the host processor and any compiler inconsistencies will be flagged by the host system FPE. Additionally, an automatic conversion translator program for Fortan (FACT) is available; residing in the VAX, it translates Fortran from the VAX into the PC Fortran subset for execution on the smaller system.

An IBM or equivalent PC with a minimum of 256 kbytes and two floppy disks is required for the package, but the use of 640 kbytes and a 10-Mbyte hard-disk drive will increase performance substantially. An Intel 8087 math coprocessor will also improve performance.

Priced at $1495 for a single copy, the PC FPE will be available in February.

Softool Corp., 940 S. Kellogg Ave., Goleta, Calif. 93117; (805) 964-0560.

CIRCLE 312

Ray Weiss

SOFTWARE

Schematic entry software also programs logic

A software package that runs on all models of the IBM PC and their look-alikes enables an engineer to enter schematics, then translate (compile) those schematics into programming patterns for all existing PAL and IFL (integrated fuse logic) devices, bipolar PROMs, and CMOS EPROMs and EEPROMs. The patterns are in the standard JEDEC file format and can be downloaded into any logic programmer over an RS-232 link.

Previously, engineers were limited to describing their programmable logic functions in Boolean equations and function tables, a tedious process at best and one more suited to mathematicians or logicians. The schematic method permits engineers to work with the system in the same way that they think about their design. The software also permits a user to enter his functions with equations and tables.

Assisted Technology's package, known as CUPL-GTS, comes with a mouse and a graphics board that works with the IBM monochrome video controller board, increasing the display resolution of the IBM monitor from 720 by 352 pixels to 1056 by 360. This increased resolution makes possible a menu interface with full command names and a more readable representation of logic functions.

Available functions include AND, NAND, OR, and NOR gates; three-state buffers; and four types of flip-flops. Users can pick one of these, specify parameters, then connect the inputs and outputs.

The package sells for $4995. Delivery is from stock.

Assisted Technology Inc., Suite 150, 2381 Zanker Road, San Jose, Calif. 95131; (408) 942-8787.

CIRCLE 315

Curtis Panasuk

SOFTWARE

Design tool compiles logic-device schematics

Written in C for easy portability, A+Plus allows users of erasable programmable logic devices (EPLDs) to enter designs using logic schematics. Other input formats include interactive net lists, state diagrams, and traditional Boolean equations. A+Plus runs on the IBM PC and PC-compatible computers, and it is compatible with third-party programmers such as Data I/O and Stag machines.

The initial release of A+Plus is supplied on 5¼-in. diskettes and includes IBM-compatible device programming hardware for Altera's family of EPLDs.

Altera Corp., 3525 Monroe St., Santa Clara, Calif. 95051; (408) 984-2800. $2500.

CIRCLE 332

Simulation program optimizes design cycle

The latest member of the TEGAS family of CAE software, TEXSIM/B (TEGAS Extended Simulator/Behavioral) is a comprehensive simulation package for printed circuit board design and semicustom and full-custom IC design. TEXSIM/B supports a hierarchical design approach with mixed-level simulation (simulation of a circuit description with a combination of behavioral, gate, and transistor elements).

The software is currently available on Calma systems for approximately $70,000 and will be offered on the Apollo-based TEGAStation in early 1985.

Calma Co., 2901 Tasman Drive, Santa Clara, Calif. 95050; (408) 970-1679.

CIRCLE 333

SOFTWARE

Equation processor runs on IBM PC

A professional math tool for the IBM PC, Equate allows up to 799 equations to be entered anywhere on the screen using standard algebraic notation. The interactive constants window contains over 400 physical constants and measurement conversions, which can be inserted into the equation. The user can also add equations or other constants to the window. When a function key is pressed, Equate evaluates the equations, prompts for undefined variables, and produces double precision (16 digit) results.

The program's forms feature helps create application worksheets by prompting the user for data and arranging all results into tables. Supplied with Equate is a disk that contains worksheets for solving simultaneous equations, calculating standard deviation and variance, and calculating area and moments of inertia for the principal shapes.

Banyan Systems Corp., 5632 E. Third St., Tucson, Ariz. 85711; (602) 745-8086. $195.

CIRCLE 334

Program backs up μC hard disk

Competing with streaming tape backup systems costing up to 15 times as much is a software program that backs up and restores any or all files on a microcomputer's hard disk. Unlike streamers, which copy the entire disk, Bakup software copies only those files that have been altered or changed. In addition, it automatically creates a data base of backup information from which files can be chosen for restoration. The Bakup program also prints a variety of reports and features context-sensitive help screens. The program runs on an IBM PC XT or compatible computer and requires 256 kbytes of memory.

InfoTools Inc., 1138 Pomeroy Ave., Santa Clara, Calif. 95051; (800) 538-8157 or (408) 246-3462. $149.95.

CIRCLE 335

DIGITAL ICs

Preprogrammed μC directs speech chip for simple, compact voice I/O

To make the task of building a speech recognition and synthesis system simpler, the VRS1000, a single-chip microcontroller has been preprogrammed to complement the SP1000 speech-processing chip that General Instrument introduced about a year ago. The controller (a PIC-7040 microcomputer) thus becomes the first chip to contain all the control software so that very simple and compact systems can be built to add speech recognition or synthesis to personal computers and other digital systems.

The algorithms in the controller's ROM let the device control the SP1000 and feed it stored speech from an external ROM for synthesis or perform speaker-dependent discrete-word recognition with an accuracy of up to 98%.

In a typical application, the pair of chips could be set to recognize between 10 and 20 user-defined words from a given list and switch between lists by means of a menu. Consequently, although the instantaneous size of the vocabulary is only about 20 words, the actual number of words can be extended almost indefinitely (limited only by the system's memory capacity).

The speech chip can readily be connected to most 8-bit microprocessor buses and is programmed via four user-accessible registers. The heart of the chip is a filter block that operates as an eight-stage all-zero lattice filter in the analysis mode and as a 10-stage all-pole lattice filter in the synthesis mode.

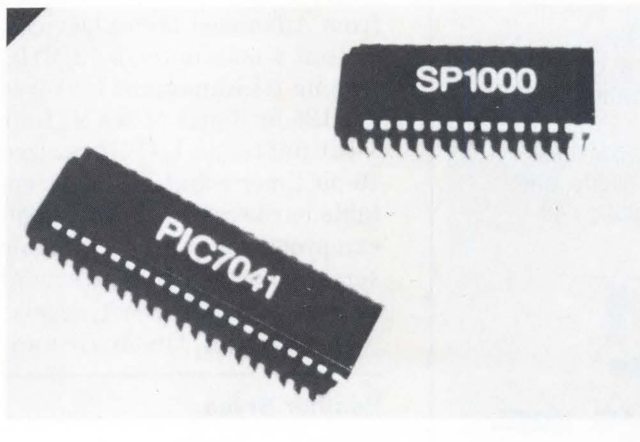
Like the speech processor, the controller is fabricated in NMOS, operates from a 5-V supply, and consumes about 500 mW. Unlike the speech chip, though, which is housed in a 28-pin package, the controller comes in a 40-pin DIP.

To evaluate the chip set, the company offers a board that can plug into a long card slot in most IBM-compatible personal computers. On the VRSM1000 board, which comes with disk-based demonstration and interface software, are the two chips as well as a ROM with several words of prepared speech, plus support circuits for both synthesis and recognition. What's more, a board developed by Telinnovation can be used in conjunction with the VRMS1000 to develop speech utterances (see p. 422).

The chip set, but not the evaluation board, is aimed at OEM systems. It will cost just $12.77 apiece in 10,000-unit quantities. The board is priced at $500 in single-unit quantities and comes complete with manual, software, and microphone. All items are available from stock.

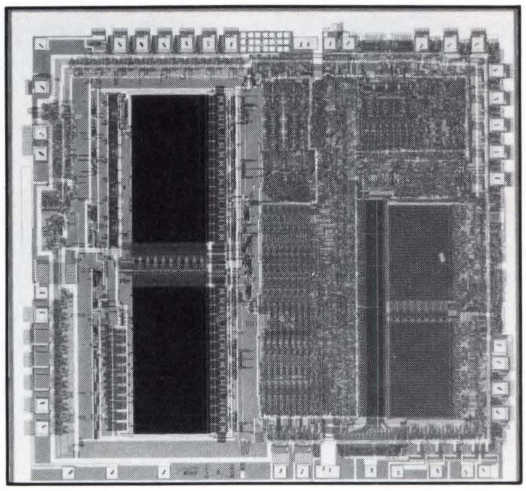
General Instrument Corp., 600 W. John St., Hicksville, N.Y. 11802; Janet May, (516) 933-3280.

CIRCLE 310



Dave Bursky

8-bit microcomputer contains 64-kbit EPROM



Based on the popular 8-bit 8051, the Am9761H contains 64 kbits of EPROM, the largest amount of EPROM storage available on a single-chip microcomputer and twice the amount on the EPROM version of the 8051, the 8751. Consequently, it can take on new and larger control applications while saving the designer 12 to 16 weeks' lead time over a standard ROM-based implementation.

Completely pin-compatible with the 8051, the NMOS device, from Advanced Micro Devices, runs at a maximum of 12 MHz. Among its important features are 128 by 8 bits of RAM, four 8-bit ports, 32 I/O lines, two 16-bit timer-counters. Other notable hardware includes a Boolean processor, a programmable serial port, and five interrupt sources with two priority levels.

In addition, the device addresses 64 kbytes each of program memory and data memory and performs a multiplication or division in four cycles. Four I/O ports add to the microcomputer's flexibility.

Programming is a simple matter, involving writing into the EPROM while applying a 21-V programming voltage. The 21-V source must be well-regulated and glitch-free to prevent spikes that cause permanent damage to the device. A security bit guarantees against unauthorized access to the EPROM's contents.

The chip is available now, with production quantities requiring four to eight weeks for delivery after the receipt of an order; it costs $105 apiece in 100-unit lots. The "H" suffix indicates operation over the commercial temperature range.

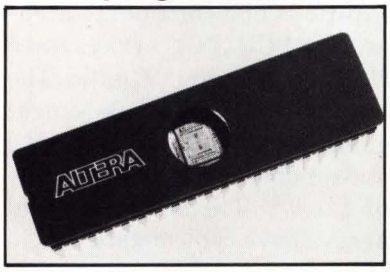
Advanced Micro Devices Inc., 4115 Freidrich Lane, Austin, Texas 78744; (512) 441-6900.

Heather Bryce

CIRCLE 308

DIGITAL ICs

Logic array is reprogrammable



Designed with CMOS EPROM technology, a reprogrammable logic device has 1200 gates and more than 14,000 reprogrammable bits. Designated the EP1200, the array features dedicated latchable inputs, local and global communications, product-term sharing, buried registers, and programmable I/O structures. The device—which comes in a windowed 40-pin ceramic DIP—is capable of operating at speeds above 16 MHz, while dissipating only 400 mW in the active mode. Standby power dissipation is only 15 mW.

Altera Corp., 3525 Monroe St., Santa Clara, Calif. 95051; (408) 984-2800. $129.50 (100 units).

CIRCLE 336

Image processor chip handles 5 MIPS

Due to the use of a non-von Neumann architecture, a single-chip image processor is capable of processing 5 million instructions/s. Furthermore, up to 14 of the uPD7281D chips can be cascaded to achieve even greater processing speeds. When installed in a personal computer, the image processor can rotate graphics or pictures of 640 by 400 pixels to any angle in no more than 1.4 seconds.

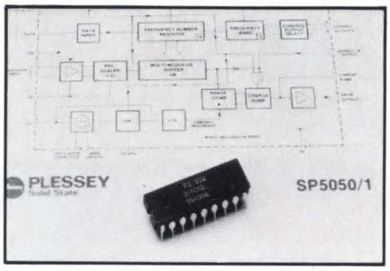
In addition to image processing, the uPD7281D can be used for high-speed signal processing and numerical calculations. It features an on-chip 16-by-16-bit multiplier, which has multiplication times of up to 200 ns. Available instructions include barrel shift, bit operation, and bit check.

NEC Electronics Inc., 401 Ellis St., Mountain View, Calif. 94043; (415) 960-6000.

CIRCLE 337

DIGITAL ICs

2-GHz synthesizer chip reduces system costs



Designed for use in satellite, TV, or cable TV receiver devices, a 2-GHz single-chip frequency synthesizer reduces development costs by eliminating the need to match a divider with the synthesizer. When used with a voltage-controlled oscillator, the IC creates a complete phase-locked-loop system capable of synthesizing a range of frequencies from 64 to 2048 MHz.

Housed in an 18-pin DIP, the SP5050 consists of a divide-by-32 prescaler with its own preamplifier and a 14-bit programmable divider controlled by a serially-loaded data register. The device is also available without the preamp, designated the SP5051.

Plessey Solid State, 3 Whatney, Irvine, Calif. 92714; (714) 951-5212. $20.

CIRCLE 338

60-cell library backs CMOS gate arrays

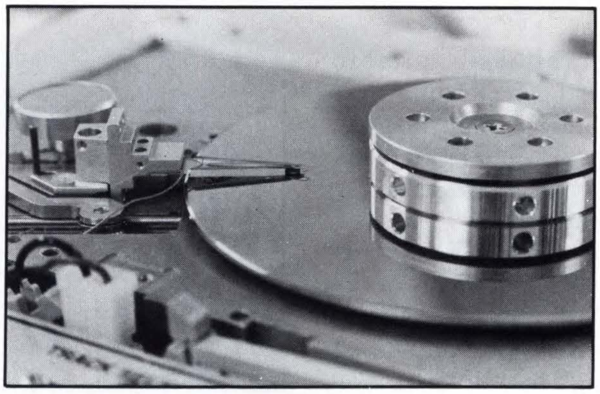
Two families of CMOS gate arrays are supported by a library of 60 predefined macrocells, including master-slave flip-flops and compound latches. The PCC/PCF arrays have 330, 450, 700, and 1100 gates. The high-speed family has typical gate delays of 2.6 ns at 5V (25°C) and an operating voltage range of 2 to 6 V. The medium-speed arrays have typical gate delays of 8 ns at 5 V (25°C) and an operating voltage range of 3 to 15 V. A variety of DIP and SO packages is available.

Signetics Corp., 811 E. Arques Ave., Sunnyvale, Calif. 94086; (408) 739-7700.

Philips Elcoma, PO Box 523, 5600 AM Eindhoven, the Netherlands; (040) 757005; Telex: 51573

CIRCLE 339

Thin-film heads serve 1200-tpi drives



A series of thin-film read/write heads is one of the first to meet the needs of advanced hard-disk drives having densities in excess of 1200 tpi. The 1200 series, an addition to Read-Rite's RR-1212 line, will handle a data track width as thin as 250 μin.

The heads are intended for new-generation, high-capacity hard-disk drives employing advanced servo-tracking techniques to increase track densities and higher data transfer rates to handle greater bit densities.

The heads are built by sputter-depositing magnetic poles on and plating copper coil windings onto the ultrasmoooth surface of an alumina and titanium carbide substrate. The heads have two rails (one for writing, the other for reading), each 0.030 in. wide. The metal poles are deposited on these rails.

The write head is specified for a 1600-μin.-wide top pole and a 1750-μin.-wide bottom pole; the read head, for 700 μin. for the top pole and 850 μin. for the bottom pole. Together, they produce head gaps of 38 and 30 μin., respectively.

The coil structure of the head consists of 24 center-tapped turns. With a flying height of 13.5 μin. (+1.5 μin.), a 45-mA write current, and a 3600-rpm disk speed, the heads will provide a minimum amplitude of 400 μV into an industry-standard SSI-104 read channel. Under these conditions, the signal-to-noise ratio is better than 30 dB.

The recommended suspension consists of Whitney flexures with about 15 grams of pressure.

Evaluation samples of the heads are available now at a price of $100 each, with a minimum order being 10 pieces. In very large OEM quantities, however, the price will approach that of ferrite heads (approximately $15 each).

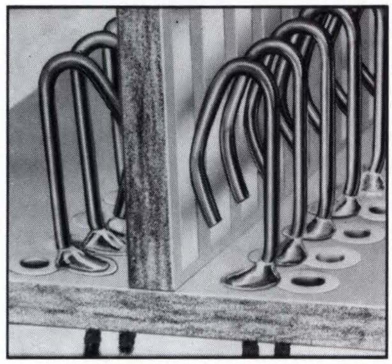
Read-Rite Corp., 345 Los Coches St., Milpitas, Calif. 95035; Fred Barez, (408) 262-6700.

CIRCLE 318

Stephan Ohr

COMPONENTS

Packaged wire-form connectors have contacts



An established, reliable mating technique that promises to outlast the printed circuit board itself is now implemented for the first time in dual-contact form. The DRP series of Digi-Klip card-edge connectors, from Components Corp., consists of free-standing wire connector, formed from a tough beryllium-copper alloy wire that holds tight and keeps on gripping.

Available earlier as single-contact units (the SRP series), the connectors are packaged in plastic carrier strips that make mounting and positioning easy. Previously, wire-form card-edge connectors, which give the tightest contact, have only been available unpackaged, so that they needed to be individually soldered on to the motherboard. In addition, they were limited only to single-contact versions.

The connectors mate so tightly that they form a gas-tight contact. Thus they eliminate the need for precious metal plating on the connector and the circuit board tab.

The combination of the wire form, the beryllium-copper alloy, and a proprietary heat-treating process that optimizes the temper after the alloy has been formed into the desired shape produces contacts that maintain their tight spring—in tests at the company, the connectors required the same extraction force even after 5000 mating cycles.

After soldering, the plastic carriers can be removed by the motherboard maker after the normal washing cycle or left in place as a protective device until the product is used. They are removed with a special tool, much like an IC extractor, and can be either disposed of or recycled back through Components Corp. for credit.

Carrier-strip contact spacing is available in popular increments of 0.100, 0.125, 0.150, or 0.156 in., and row spacing is the standard 0.200 in. Any number of contact points can be specified so that no terminal positions go unused, and the price depends on the number of contacts specified per strip.

Standard configurations are available from stock; custom configurations take four to six weeks. A subminiature version is scheduled for availability in June.

Components Corp., 6 Kinsey Place, Denville, N.J. 07834. (201) 627-0290.

CIRCLE 322

Carole Patton

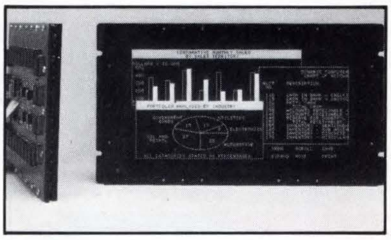
COMPONENTS

EL flat panel slims down to 3/4 in.

Only the second electroluminescent flat-panel display subsystem to appear commercially with a CRT-sized screen for computer systems, the EL6648 MX from Planar Systems is only 3/4 in. thick and takes up a mere 5% of the volume of a comparable CRT.

The panel has a matrix of 256 rows by 512 columns (131,072 pixels), for a display of 25 lines by 80 characters of text or graphics. It is housed in a package 5.7 in. high by 10.3 in. wide and weighs only 16 oz.

Extensive use of custom ICs and surface-mounted packaging



are responsible for trimming the package size from 1.8 in., the thickness of the one previous computer-sized EL display (also made by Planar Systems).

Although the unit draws more power than thin-panel liquid-crystal displays, its 6 to 8 W typical, 15 W maximum, is still much lower than a CRT's power consumption. Also, it operates in virtually all lighting conditions, whereas the readability of LCDs depends on the ambient light.

Compatible with many existing CRT controllers, the panel uses two driver chips for the rows and two for the columns. It is designed to operate from 0° to 55°C and to be stored at −40° to +75°C.

Shipments begin this month at $775 each in orders of 1000 units. The price is $1750 for up to 4 units and $875 for 25 to 49 units.

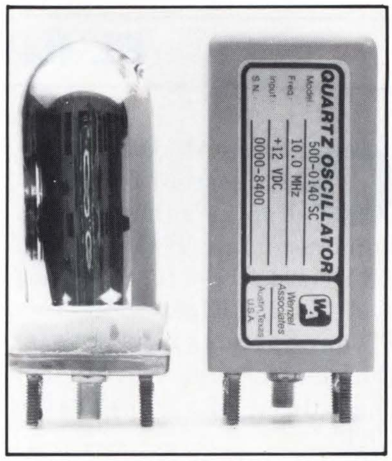
Planar Systems Inc., 1400 NW Compton Drive, Beaverton, Ore. 97006; (503) 629-2006.

CIRCLE 304

COMPONENTS

Quartz oscillator has low phase noise

A miniature ovenized quartz oscillator uses SC-cut crystals to achieve low phase noise, low power consumption, and good thermal stability for frequencies between 3 and 11 MHz. SSB phase noise for the Small Fry series 5-MHz oscillator can be specified to −140 dBc at 10 Hz from the carrier and better than −165 dBc at 1 kHz from the carrier. For 10-MHz models, the respective figures are −135 dBc and −165 dBc. The device consumes less than 1 W at 25°C, while maintaining a typical temperature stability of $\pm 2 \times 10^{-9}$ from −25° to +65°C. The Small Fry comes in a package size of 1.5 by 1.5 by 3 in.



Wenzel Associates Inc., 11124-B Jollyville Road, Austin, Texas 78759; (512) 345-2703. From $510 to $780.

CIRCLE 340

UV fluorescent lamp is just 2³/₈ in. long

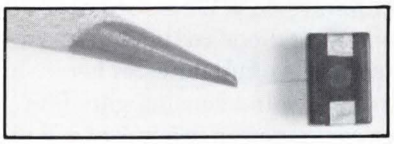
One of the smallest ultraviolet fluorescent lamps on the market is 2³/₈ in. long and only ³/₈ in. in diameter. Despite its small size, the 1-W Model BF959 delivers 300 $\mu W/cm^2$ of intensity and is rated for 20,000 hours. The UV fluorescent lamp is also available in a 1.6-W configuration. This version offers an intensity of 600 $\mu W/cm^2$, however, the rated life drops to 10,000 hours.

JKL Components Corp., 13343 Paxton St., Pacoima, Calif. 91331; (818) 896-0019. From $4.20 (100 units); stock.

CIRCLE 341

COMPONENTS

Film chip capacitor comes in mini cases



In keeping with the trend toward miniaturization, the MKT 1824 metallized-film chip capacitor comes in three sizes with maximum lengths of 4.2, 5.7, and 7.5 mm. All three sizes are rated for 63 V dc. Capacitance values range from 0.01 to 0.15 μF for the 4.2- and 5.7-mm-long devices and from 0.01 to 0.22 μF for the 7.5-mm-long chip. The MKT 1824 capacitor is suitable for wave soldering up to 260°C (for 5 seconds) and reflow soldering up to 260°C (for 10 seconds).

Roederstein Electronics Inc., PO Box 5588, 2100 W. Front St., Statesville, N.C. 28677; (704) 872-8101.

CIRCLE 342

Tactile-feel keypanel weathers >5M cycles

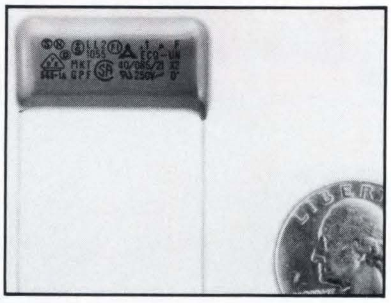
The Microkey Elastomer MKE keypanel features a proprietary silicon rubber dome-switch mat that provides true breakover tactile feel and reliability in excess of five million cycles. The switch mat also offers spillproof ESD protection to the keypanel's circuitry. Contact resistance is 200 Ω maximum with a 5-ms bounce. Prices as low as $0.15 per key station (for large quantities) make the MKE cost competitive.

Advanced Input Devices, W. 250 A.I.D. Drive, Coeur d'Alene, Idaho 83814; (208) 765-8000.

CIRCLE 343

COMPONENTS

Film capacitors meet international standards



Designated the ECQ-UN series, a family of metallized-film capacitors is approved by most international standards agencies, including UL, CSA, VDE, SEMKO, and SEV. The universal capacitors are suitable for across-the-line applications meeting UL/CSA standards and class X applications meeting European standards as interference suppressors. Values ranging from 0.001 to 0.22 μF are available with tolerances of $\pm 20\%$. Rated voltage is 250 V ac at 50/60 Hz.

Panasonic Industrial Co., Electronic Components Division, 1 Panasonic Way, Secaucus, N.J. 07094; (201) 348-5246. $0.20 (typical); 12 to 14 weeks.

CIRCLE 344

Optical interrupter uses Schmitt trigger

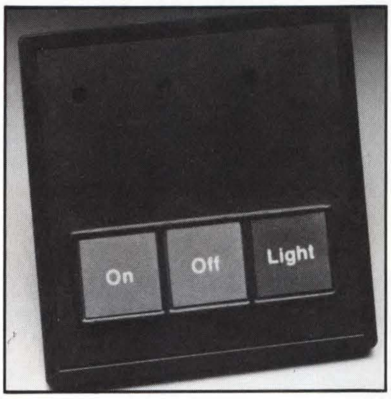
A low-power optical interrupter module employs a Schmitt trigger to produce switching speeds with rise and fall times of 0.1 μs. Designated the H21L (with mounting tabs) or the H22L (without tabs), it consists of a GaAs infrared-emitting diode coupled to an integrated circuit detector across a 3-mm (1/8-in.) sensing gap. Power consumption is 5 mA at 5 V in the detector and 15 mA at 1.6 V in the emitter. The H21/22L operates from supplies of 4 to 15 V, and its open-collector output sinks 20 mA to under 0.4 V. Typical applications include robot position sensing or shaft encoder and positioning in disk drives.

General Electric Co., Power Electronics Semiconductor Department, W. Genesee St., Auburn, N.Y. 13021; (518) 454-2533. $1.95 (1000 units).

CIRCLE 345

COMPONENTS

Keyboard module is customizable



Permanently molded into a bezel for front-panel mounting, a control-display module contains a user-specified number of dome switches, LED indicators, electronic components, and a pin connector. The dome switches are actuated through auxiliary external circuitry to deliver up to 10 mA at 24 V dc to the terminals of the built-in connector. Actuation of the switches also illuminates the respective LED indicator. The normally open SPDT switch contacts have a resistance of less than 100 Ω.

Tricon Industries Inc., Electromechanical Division, 2325 Wisconsin Ave., Downers Grove, Ill. 60515; (312) 964-2330.

CIRCLE 346

18-wire print head performs wire shifting

An 18-wire dot-matrix print head performs print-wire shifting, which increases the vertical dot density to produce letter-quality print and high-density graphics. The shifting motion is completed in 3 to 5 ms and requires less than 2 W continuous. What's more, the head is capable of operating at speeds of up to 2000 impressions/s per print wire.

The Series 4500 comprises three models, which offer vertical resolutions ranging from 72 to 240 dots/in. in single-pass and double-pass modes.

DH Technology Inc., 575 Maude Court, Sunnyvale, Calif. 94086; (408) 738-2082. From $110 (OEM quantities); four to eight weeks.

CIRCLE 347

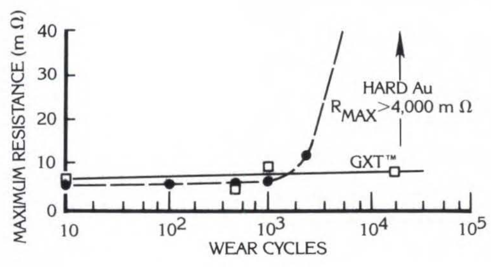
New Du Pont GXT™ plating These magnified

Cutaways of pins (shown in these microphotographs) prove GXT plating resists wear better than gold. After 25,000 mating cycles, note the minimal deterioration of the Du Pont coating. With GXT, a cycle life greater than 25,000 cycles is possible.

Tests also show the GXT plating system is better than gold in solderability, porosity, bend ductility, and corrosion resistance. Yet GXT can reduce costs as much as 20%.

Independent testing laboratories have proved that the Du Pont GXT plating system is *superior to gold* in wear resistance, solderability, porosity, environmental corrosion resistance and bend ductility. And is as *good as gold* in contact resistance and wire-wrapping performance.

Moreover, connectors protected by this remarkable new coating system frequently cost considerably less than comparable parts plated with gold. For example, savings of up to 20% are possible on pins plated with GXT. (Savings depend on the price of gold and upon the amount of gold being replaced.)



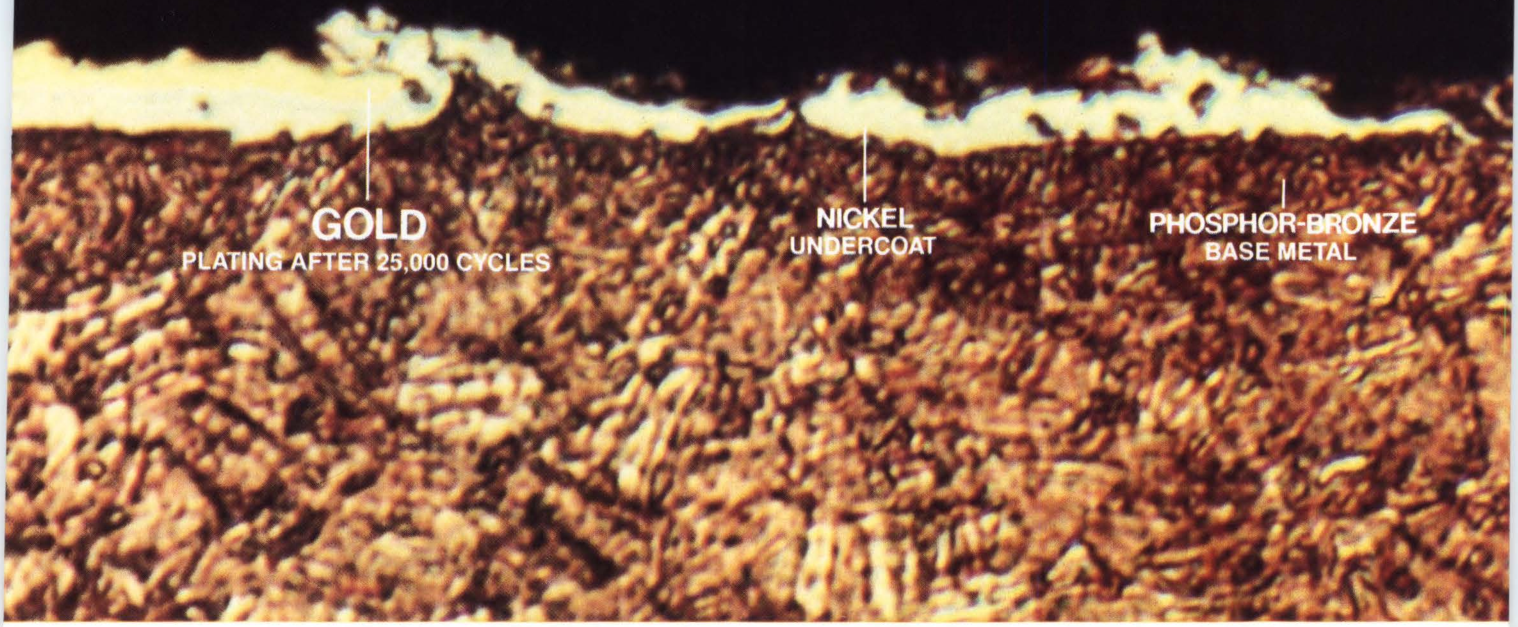
GXT assures minimum contact resistance after wear and exposure to H_2S

By 25,000 cycles, gold shows contact resistance increases to 4,000 milliohms or higher. In contrast, GXT shows excellent electrical performance even after 25,000 cycles.

GXT is a trademark of the Du Pont Company.

Berg Electronics is now

outwears, outperforms gold. connector pins prove it.



In these tests, other gold substitutes didn't measure up to GXT, either. In porosity, solderability, intermetallic growth, bend ductility, internal stress, and manufacturing process stability, the GXT plating system clearly outperformed all other gold alternatives including other palladium-nickel and pure palladium coatings.

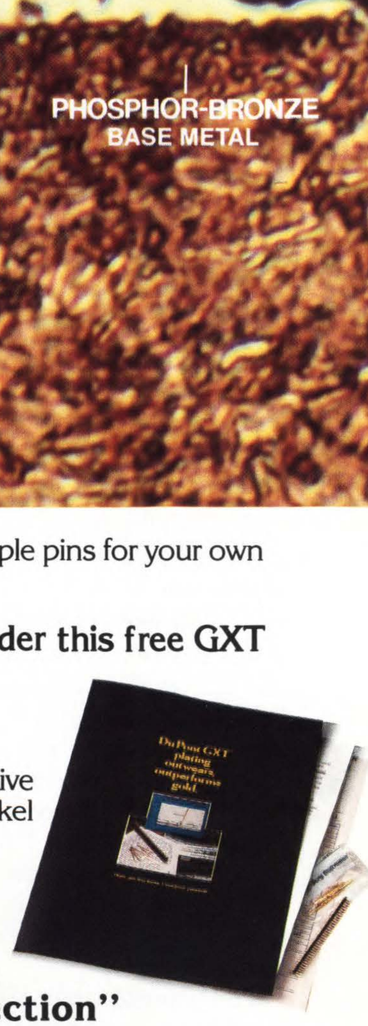
In fact, in no test did any gold substitute—or gold itself—outperform GXT.

GXT plating, an exclusive Du Pont development, is now available on Du Pont's 0.025″ square pins, including BergStik™ headers, BergPost™ and BergPin™ terminals, and compliant press-fit pins. Some industry leaders already have switched from gold to GXT to help improve the reliability of their products.

If you require high reliability connectors, you're sure to want complete test results. They're yours for the asking...along with sample pins for your own tests/inspection.

Get all the facts! Order this free GXT Convincer Kit.

Review results from independent test laboratories. Proof positive that GXT palladium-nickel plating outwears, outperforms gold. To request kit. . .



Make the "Du Pont Connection"
Call (800) 237-2374 EXTENSION 201

Or write The Du Pont Company,
Du Pont Connector Systems,
30 Hunter Lane, Camp Hill, PA 17011.

DU PONT CONNECTOR SYSTEMS

DU PONT
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CIRCLE 150

INSTRUMENTS

Programmer handles 99% of device types

A universal programmer allows an engineer to program over 99% of all existing programmable logic devices, including PROMs and PAL and IFL (integrated fuse logic) devices. The Model 60A, made by Data I/O, is available with a handler interface for programming parts in production quantities.

PROMs are verified by reading the loaded value and comparing it with the desired value. PAL and IFL devices can be tested by applying a group of 128,000 pseudorandom test patterns to a known good part, generating a signature. This signature can then be produced from parts under test and compared with the good signature to verify functionality.

The programmer provides a second way to test PAL and IFL devices by accepting test vectors generated by languages, which allow a selected stimulus to be applied to a part and the output examined. Both the fuse and bit programming patterns, as well as the test vectors, can be loaded into the machine over an RS-232 interface using the JEDEC file format standards.

A menu-driven screen lets a user easily control the programmer. All entered variables are stored in EEPROM. Chip parameters are stored in ROMs, and parameters for new chips can be added by plugging in a new ROM set.

The programmer comes with 20, 24, and 28 pin sockets. An extra adapter is available that allows the sockets to be extended several feet out to a chip handler. With that type of setup, which includes a special capacitor boost that strengthens the signals going out to the head, to hold down programming errors, a user could program 20 parts in 30 seconds.

The Model 60A is available two weeks after receipt of an order for $3425 for a single unit. The handler interface costs an additional $1000.

Data I/O, 10525 Willows Road NW, C-46, Redmond, Wash. 98052; (206) 881-6444.

CIRCLE 316

Curtis Panasuk

Monitor debugs 8-bit microprocessors

Packaged in the form of a breakout box, a microprocessor bus-monitoring instrument is a useful debugging aid for real-time control software, since it does not affect the operation of the system under test. The Model 08 is available for use with a variety of 8-bit microprocessors. With some additional parts, the system can be easily reconfigured to accommodate 6502, 6809, 8085, and Z80 devices.

The user selects a set of trigger conditions and a delay value. Each time a bus cycle matches the trigger conditions, the monitor delays the specified number of cycles. It then captures the states of the address bus, along with two successive data bus cycles. The results are displayed on the instrument's dot-matrix display.

Mecklenburg Engineering, PO Box 744, Chagrin Falls, Ohio 44022; (216) 338-4237. $490.

CIRCLE 348

INSTRUMENTS

PC-based workstation performs logic analysis

Costing less than most standalone logic analyzers, the MicroAnalyst workstation integrates the power of an IBM PC AT with the Series 2000 logic analyzer and a Lotus-based general-purpose software package. Five software functions—spreadsheet, data base, word processing, graphics, and communications—allow the user to perform complex data analysis.

The complete workstation, including the PC AT and the Lotus software, is priced at $17,900.

Northwest Instrument Systems Inc., 15201 NW Greenbriar Pkwy., Suite 140, Beaverton, Ore. 97006; (503) 645-5151.

CIRCLE 349

Synthesizer switches in less than 100 ns

A board-level frequency synthesizer operates from dc to 15 MHz and switches in less than 100 ns—one of the fastest switching speeds in the industry. What's more, the VDS-2000 maintains perfect phase continuity at the switching point. The synthesizer has a standard resolution of 1 Hz. Phase noise is extremely low, even very close to the carrier, and spurious levels as low as −60 dBc are available. Accuracies to within a fraction of a part per million are optional.

The board, which requires less than 42 in.^{2}, can provide simultaneous pulse (TTL) and sinusoidal outputs, control of phase, and digital output of phase information. The VDS-2000 is also available in a chassis with a power supply and interface.

Sciteq Electronics Inc., 7380 Clairemont Mesa Blvd., San Diego, Calif. 92111; (619) 292-0500.

CIRCLE 350

INSTRUMENTS

Board tester speeds analog checks

Combining up to 3,072 hybrid pins with high speed and accuracy for analog measurements, the Series 700, System 770, in-circuit tester from Factron meets the test requirements of complex printed circuit boards.

Using a new architecture, dubbed AMS (automatic measurement system), the tester holds analog errors to less than 1%. Moreover, at its highest test speed the unit is 3 to 10 times faster than conventional units.

The analog accuracy is achieved with a high-frequency switch matrix that greatly reduces the effects of residual capacitance and resistance. Also, predictive algorithms based on waveform sampling and analysis techniques accurately and rapidly determine the end-state responses to ac and dc input stimuli. In addition, five levels of sensitivity let the user maximize speed and accuracy for a particular set of test conditions.

Like its sister product, the System 730, the tester checks digital devices according to their timing specifications. Guard-pin contention is eliminated using the company's Flexpin architecture.

The base price of the tester is $185,000. Deliveries will begin in the second quarter of the year.

Factron, Latham, 299 Old Niskayuna Road, Latham, N.Y. 12110; (518) 783-3600.

CIRCLE 302

INSTRUMENTS

Portable servo writer cuts costs fivefold

Well suited for R&D, production, and depot service applications, the PR1000 writes Winchester servo tracks without the use of a mechanical positioner, granite blocks, lasers, or other accessories. The portable unit cuts the cost of a full-blown servo writer from over $250,000 to under $50,000. Furthermore, the PR1000 servo writer is fully programmable and does not require costly reconfiguration to handle different sets of drive characteristics.

Pioneer Research, 1745 Berkeley St., Santa Monica, Calif. 90404; (800) 848-1745 or, in California, (800) 233-1745.

CIRCLE 351

Z80 emulator is versatile, easy to use

Providing both hardware and software for interactive emulation of the Z80 microprocessor, the Z-Scan 80 emulator can be used as a stand-alone unit or with a host development system. Simplistic operation through the use of a menu-driven interface, a command file executive, and a full debugger command set further enhances the emulator's versatility.

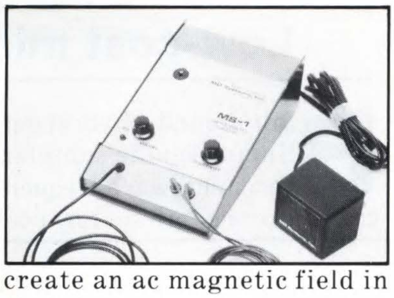
The Z-Scan operates at 4, 6, or 8 MHz and provides real-time emulation from 32 1-kbyte blocks of mappable memory. Using its 4k-by-32-bit block of RAM, the emulator handles up to 4096 trace cycles.

Zilog Inc., 1315 Dell Ave., Campbell, Calif. 95008; (408) 370-8126. $6695.

CIRCLE 352

Instrument locates short-circuit sources

Unlike instruments that detect only the presence of a shorted circuit in printed circuit board assemblies, the MS-1 traces the shorted path to locate the source of the fault. It contains a 300-kHz low-voltage signal source, which is used to create an ac magnetic field in the vicinity of the shorted current path. The MS-1's Omni-Probe responds to any orientation of the resulting three-dimensional flux patterns and emits an audible tone whenever it is held near a 300-kHz current-carrying conductor. Faults are typically located in less than one minute.



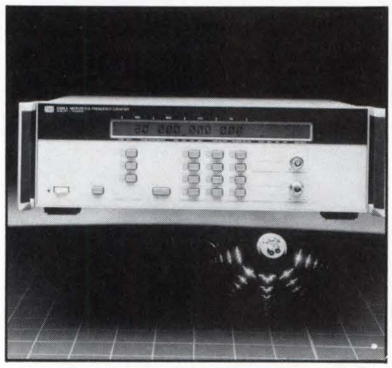
MD Systems Inc., 3178 Doolittle Drive, Northbrook, Ill. 60062; (312) 564-3110. $299.

CIRCLE 353

INSTRUMENTS

Low-cost microwave counters transfer data fast

Built around a hybrid gallium arsenide sampler, two microwave frequency counters combine low cost with fast data transfer and a resolution of better than 1 Hz, plus optional low-aging-rate oscillators. The 20-GHz HP



5350A and the 26.5-GHz HP 5351A from Hewlett-Packard are priced at $5000 and $6000, respectively.

Because of the single-synthesizer design and new measurement algorithm, the counters can send 80 measurements/s over the HP-IB while tolerating up to a 20-MHz FM variation on the input signal.

Their sensitivity is rated at −25 dBm from 500 Hz to 12.4 GHz, −20 dBm from 12.4 to 20 GHz, and −15 dBm from 20 to 26.5 GHz. A separate low-frequency input with 0.001-Hz resolution measures signals from 10 Hz to 525 MHz.

A smoothing function, invoked from the keyboard, uses a running weighted-average technique to maintain full resolution when measuring unstable sources. Moreover, an offset feature adds or substracts successive measurements from a chosen or measured value, displaying only deviations.

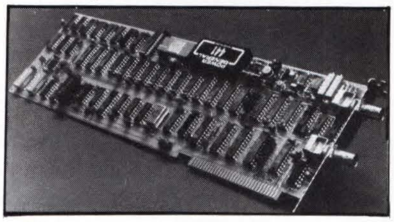
Both units are delivered in six weeks from receipt of an order.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Road, Palo Alto, Calif. 94303.

CIRCLE 301

COMPUTER BOARDS

A-d converter board captures transients



One of the first commercially available 8-bit a-d converter boards for the IBM PC, the PCTR-160 digitizes and stores analog signals at a base sampling rate of up to 20 MHz. Finer resolution can be achieved by equivalent-time sampling at 40, 80, or 160 MHz. Pre- and post-trigger modes of operation are available under software control.

General Research Corp., Adaptronics Products, 7655 Old Springhouse Road, McLean, Va. 22102; (703) 893-5900. $2300; stock to 30 days.

CIRCLE 354

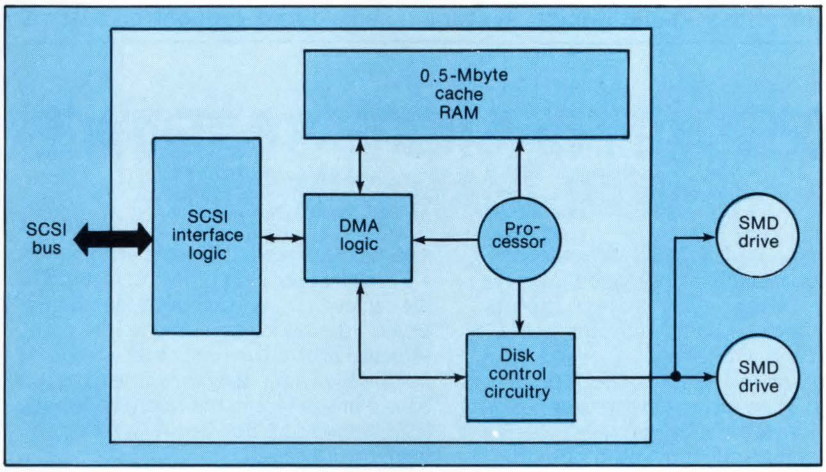
CMOS computer board totes 5-A relays

Suitable for industrial control, a CMOS board-level computer features eight onboard 5-A relays (Form C). Designated the C-Con, the board is programmed in simple 6805 assembly language and includes 128 bytes of static RAM. It also includes 6 kybtes of EPROM and forty-eight parallel I/O lines. A multiplexed serial interface via the Data-Link three- or four-wire bus permits communications with peripheral boards up to 4000 ft away.

Valinor Electronics Inc., 1268 Pembroke St., Uniondale, N.Y. 11553; (516) 538-3247.

CIRCLE 355

SMD drive controller slashes access times



The first SMD drive controller board containing a cache memory of 0.5 Mbyte speeds up data accesses by an order of magnitude or more over other controllers. The ASC-800, from Advanced Storage Concepts, uses 64-kbit dynamic RAMs for the cache; future versions will use 256-kbit chips to provide 4 MBytes of cache memory.

Normally, the head moves to find a track, a process that involves a seek time—20 or 30 ms for a high-performance drive. Additionally, there is a rotational latency for locating the sector, which averages 8.3 ms for most drives. These delays add up to 28 to 38 ms.

With the ASC-800 and a hit in the cache, however, these delays are not a part of the transfer, and the access time is under 1 ms. Thus with a 50% hit rate, the performance of the system can be approximately doubled (to 14 ms), although the company predicts hit rates of 70% to 80%, depending on the application.

Implementing the standard SCSI interface, the controller transfers data at 3 Mbytes/s and supports the disconnect/reconnect feature, which allows a device to disconnect itself at any time if its access time is exceptionally long.

Another performance-enhancing feature is an early write command that pipelines the operation for simultaneous accesses. The controller will prewrite to the cache so that the host may begin to write to another disk while the previous one is still completing its write.

The drive costs $1990 in OEM quantities and will be available beginning in the second quarter.

Advanced Storage Concepts Inc., 9660 Hillcroft, Suite 325, Houston, Texas 77096; (713) 729-6388.

CIRCLE 313

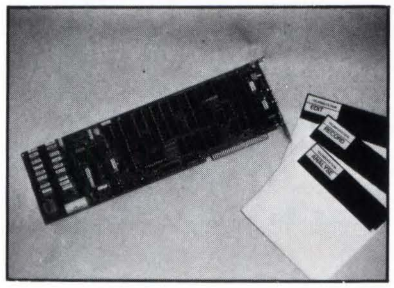
Heather Bryce

COMPUTER BOARDS

Speech development board plugs into IBM PC

A single board turns an IBM PC personal computer into a vocabulary or phrase development system for General Instrument's SP1000 speech-processing chip. Designed by Telinnovation, the board and supporting software package costs just $2000.

In conjunction with the software and a tape recorder, the board gives designers the means to record speech, digitize it, analyze it, as well as to extract the parameters to be stored and edit them, review the data, and set up the code for direct loading into a PROM programmer. It plugs into a full-sized slot in the PC and contains a 12-bit analog-to-digital converter to digitize the recorded speech. To test the final code, the development board also contains an SP1000 speech chip.



To use the software and hardware, the PC should be equipped with a hard-disk drive, at least 256 kbytes of RAM, an 8087 coprocessor, and either a color monitor adapter or a video card like the one from Hercules. Thanks to the coprocessor, the computer takes about 10 minutes to process 1 second of speech and extract the parameters. For large amounts of speech, the program permits tasks to be stacked so that the processing can be done overnight.

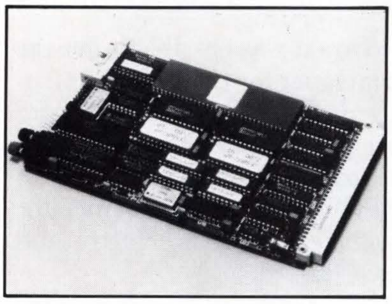
Delivery is from stock.

Telinnovation Inc., 4100 Moorpark Ave., San Jose, Calif. 95117; Charles Davis, (408) 249-1190.

CIRCLE 305

COMPUTER BOARDS

68000-based Eurocard works with G-64 bus



Utilizing a 16-bit 68000 microprocessor, the GESMPU-4A microcomputer board is built on a single-height Eurobcard (100 by 160 mm) that is compatible with the G-64 bus (the de facto standard in most European countries). The single-board computer's 68000 microprocessor operates at a clock rate of 8 MHz, with clock frequency generated by an on-board crystal oscillator. The GESMPU-4A has four JEDEC-standard sockets to accommodate up to 128 kbytes of EPROM and up to 16 kbytes of RAM. It also incorporates a triple 16-bit timer and an RS-232-C serial interface with a fully programmable baud rate. The GESMPU-4A can interface with a growing number of 8- and 16-bit memories and peripherals that are compatible with the G-64 bus (more than 300 products are available from approximately 50 manufacturers worldwide).

Gespac Inc., 550 E. Grandview, Mesa, Ariz. 85203; (602) 962-5559. $475.

CIRCLE 357

Filter board is STD bus-compatible

A microprocessor software-controlled switched capacitor filter is available on a board that is compatible with the STD bus. Programmed frequencies span from 1 Hz to 5 kHz—or to 30 kHz slightly stepped, but smoothed by a simple resistance-capacitance circuit.

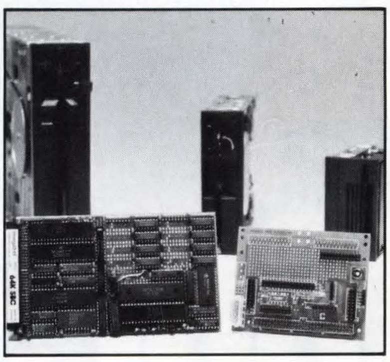
The board sustains a pair of individually programmed clocks, each capable of setting the center frequency of a pair of second-order filters. Each second-order filter has designated high-pass, low-pass, and bandpass outputs. The Q and gain of the high-, low-, and bandpass sections may be modeled to fulfill specific requirements of varied applications.

With software modifications, the pair of second-order filters can be cascaded to yield a fourth-order filter. Higher-order filters may be obtained by using a second board.

Spectra Design Time, PO Box 146, San Luis Obispo, Calif. 93406; (805) 544-6093. $350.

CIRCLE 358

SBC has on-board video controller



A single-board computer with an on-board video controller interfaces directly with a TTL or composite video monitor, eliminating the need for a terminal. The module also includes a 6-MHz Z80B CPU, 64 kbytes of RAM, a floppy-disk controller, and serial and parallel I/O—all on a board that is only 4 by 6 in. The package is supplied with a copy of CP/M 2.2, complete with a customizable BIOS, CP/M utilities, and source code.

The board is capable of operating in an alphanumeric mode and in a bit-mapped graphics mode. The latter supports a resolution of 640 by 240 pixels. The former provides a display consisting of 80 columns by up to 35 lines.

Megatel Computer Technologies, 1051 Clinton St., Buffalo, N.Y. 14206; (416) 745-7214. $375 (including a transition board and connector).

CIRCLE 359

Analog I/O board works with STD bus

Compatible with the STD bus, a multifunction analog I/O board has four differential and eight single-ended analog inputs, plus eight analog outputs. The gain of the RSD-7518's differential and single-ended inputs is resistor-programmable from 1 to 1000 and 1 to 10, respectively. Resolution on all channels is 12 bits, accurate to within ±0.05% FSR, ±1/2 LSB. Six programmable input modes permit sampling on single or multiple channels, sample averaging, and determination of sample minimums and maximums. The RSD-7518's output channels may be used as voltage outputs, current loop outputs, or a combination of both.

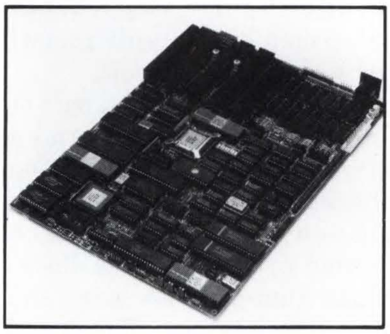
Robotrol Corp., 16100 Caputo Drive, Morgan Hill, Calif. 95037; (408) 778-0400. $595; two weeks.

CIRCLE 360

COMPUTER BOARDS

IBM PC–compatible computer board offers more

An IBM PC-compatible computer gives engineers a one-board building block to create a variety of designs and at the same time, thanks to MS-DOS compatibility, runs thousands of pieces of software. The SBM-88, from Mostron, has the capability of an IBM PC, plus monochrome video and floppy-disk controllers, and still provides five IBM PC-compatible slots that can be used to plug in any of the 300 boards available for special applications.



The board can run as well under the CP/M operating system and iRMX-86, a real-time operating system that is suited to automation applications. It also has a BIOS in ROM, developed by the company, to provide compatibility for application programs that make calls that bypass MS-DOS.

By using custom CMOS gate arrays it was possible to get the controller for the CRT and floppy disks onto the one board, along with 256 kbits of RAM (expandable up to 640 kbits), an 8087 coprocessor, IBM printer and keyboard interfaces, and two RS-232 ports.

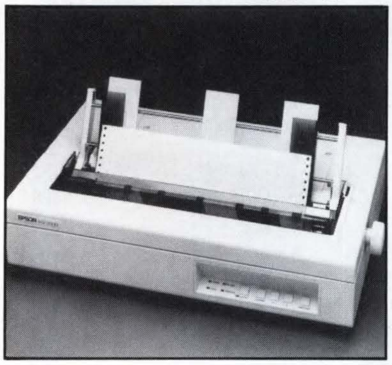
The board, 12 by 8½ in., consumes 2.5 A at 5 V and requires 50 mA at ±12 V. It is available now for evaluation, with volume production slated for February. The price in 100-unit quantities is $560 each.

Mostron Inc., 560 Valley Way, Milpitas, Calif. 95035; (408) 946-1727.

CIRCLE 314

COMPUTER PERIPHERALS

Ink-jet printer eliminates clogging



Epson's first ink-jet printer, the SQ-2000 features a cleaning system to ensure reliable operation. The system automatically cleans the printhead every few pages in a 1-second cycle. Additionally, the user may initiate a 10-second cycle that cleans both the ink line and the printhead. The printer also initiates the 10-second cleaning process whenever it is shut off and turned on.

When the unit is powered down, ink is extracted from the line and replaced with a solvent. Air, which can dry the ink and clog the printhead, is prevented from entering the line by means of a suction cup that covers and extracts ink from the printhead. When the printer is powered on, the solvent is flushed out and replaced with ink.

The SQ-2000 prints draft copy at 176 char/s and letter-quality copy at 88 char/s—at noise levels lower than 50 dB. It uses a sealed ink cartridge to prevent air bubbles from entering the line.

Epson America Inc., OEM Products Division, 23600 Telo Ave., Torrance, Calif. 90505; (213) 534-4500. Less than $2500 (OEM discounts available).

CIRCLE 356

Hard-disk subsystem stores 1.4 Gbytes

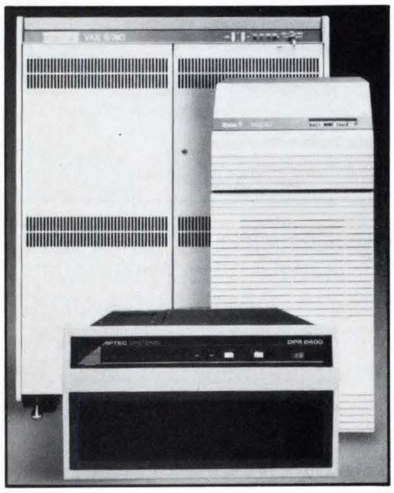
A disk storage subsystem handles 1.4 Gbytes of unformatted data (1.2 Gbytes formatted), with very fast transfers between the host and the peripheral controller. Created by Aptec Computer Systems for DEC's VAX computers, the DPS-1412 combines a 1.4-Gbyte 14-in. hard-disk drive (Ibis Systems' Model 1400) with Aptec's DPS-2400 controller.

The controller provides a data transfer rate of12 kbytes/s between host and peripheral in the burst mode and 10 Mbytes/s in the normal mode—a substantial improvement over the 1.5 kbytes/s typically associated with DEC's Unibus architecture. This high-speed transfer is especially useful in scientific, image-processing, and graphics applications, which require extensive number crunching and therefore often use hard-disk space as an extension of main memory.

The speed of the controller is due to its internal Data Interchange Bus, a 32-bit bus capable of carrying 24 Mbytes/s, and to a series of parallel 16-bit microprocessor cards that handle the buffered transfers to and from the host. The processor cards, in addition, provide intelligence (to manage disk formatting operations) and expandable buffering of 1 to 200 Mbytes.

Integrating the storage subsystem with its VAX host is relatively easy, thanks to I/O

Stephan Ohr



drivers (supplied by Aptec) which are added on the VAX. The drivers include operating software (monitor and executive) for the controller and a communications program.

In addition, application- or peripheral-specific software for the controller can be created using Fortran programs (which must be compiled before use) or a C-like language called Staple. An alternative is to select I/O driver routines from an available library using short call routines written in Fortran or Staple. The Fortran compiler, Staple interpreter, and I/O library are optional.

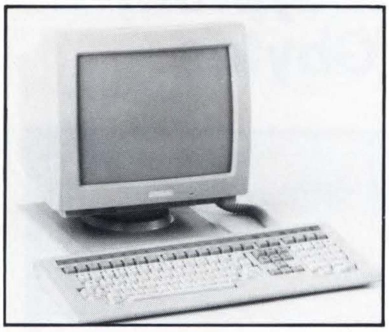
A complete subsystem, including software, is priced at $123,000. Additional disk drives with adapters for the controller are available for $81,000 apiece.

Aptec Computer Systems Inc., 10180 SW Nimbus Ave., Portland, Ore. 97223; Woodrow Wittmayer, (503) 620-9840.

CIRCLE 321

COMPUTER PERIPHERALS

Low-cost terminal emulates VT220



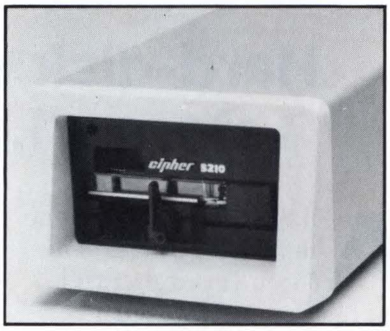
Priced nearly 40% lower than the DEC VT220, the TVT-7220 video terminal offers 100% emulation of the DEC unit. Quantity shipments of the TVT-7220, which carries a suggested retail price of $850, are available immediately. The terminal has a 14-in. display, a tilt-and-swivel enclosure, and a 105-key DIN-standard keyboard. The display screen can be formatted for 80 or 132 columns. In addition to full emulation of the VT220, the TVT-7220 emulates the VT100 and VT52 terminals.

Tatung Co. of America Inc., 2850 El Presidio St., Long Beach, Calif. 90810; (800) 421-2929 or (213) 637-2105.

CIRCLE 361

FloppyTape unit works with IBM PC XT

Users of the IBM PC XT can take advantage of 1/4-in. cartridge tape backup with the Model 5210 FloppyTape system. The Model 5210, which provides 25 Mbytes of storage, is designed to use the industry-standard floppy-disk interface and to respond to floppy-disk commands. Since it plugs directly into the computer's external floppy-disk interface connector, the need for



a controller interface card is eliminated.

The Model 5210 is capable of backing up two IBM 10-Mbyte hard disks or one 20-Mbyte hard disk at approximately 1 Mbyte/min onto a single DC600A 1/4-in. tape cartridge. The system also adds three new commands to PC-DOS for backup, restoring, and formatting functions.

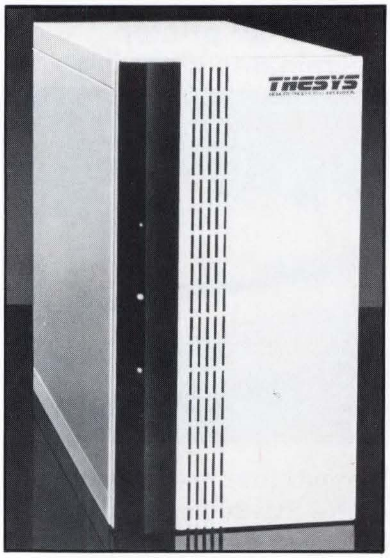
Cipher Data Products Inc., 10101 Old Grove Road, San Diego, Calif. 92138; (800) 982-8808 or (619) 578-9100. $1095; January, 1985.

CIRCLE 362

Fast memory system is cost-effective

Not only does the Fastfile semiconductor memory system reduce the cost of high-speed storage, but it improves microcomputer response times as well. Prices for the storage system range from $1795 for the 1.5-Mbyte capacity to $3495 for the 5-Mbyte version. Access times are less than 0.25 ms, with data transfer rates of up to 1 Mbyte/s.

The Fastfile system, which utilizes 256k memory chips, works with the IBM PC and PC-compatible computers. It comprises the memory unit, along with an uninterruptible power supply, PC-DOS-compatible



software, an integral memory controller, and positive fan cooling.

Thesys Memory Products Corp., 7345 E. Acoma Drive, Scottsdale, Ariz. 85260; (602) 991-7356.

CIRCLE 363

Monochrome displays work with IBM PC

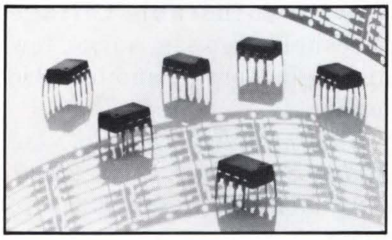
Two 12-in. monochrome display terminals are fully compatible with the IBM monochrome adapter used for the PC. Each unit has a video bandwidth of 25 MHz and produces a display of 80 characters by 25 lines. The Model TR-122MYP features a long-persistence yellow phosphor display; the TR-122M9P has a long-persistence P39 green phosphor display. The direct etched faceplates of each model are designed to minimize glare.

Panasonic Industrial Co., Computer Products Division, 1 Panasonic Way, Secaucus, N.J. 07094; (201) 348-7183. $259 (MYP) and $249 (M9P).

CIRCLE 364

POWER

FET driver provides 1500 V of isolation



An optically coupled FET driver provides 1500 V of isolation for operation in telecommunications, process control, data acquisition, and ATE. The FDA-200 comprises a GaAlAs LED coupled with two proprietary photovoltaic-output ICs encapsulated in a wave-solderable 8-pin DIP. As little as 1 mA of LED current can drive the FDA-200 to speeds of under 1 ms.

Theta-J Corp., 107 Audubon Road, Wakefield, Mass. 01880; (617) 246-4000. Less than $2 (1000 units).

CIRCLE 365

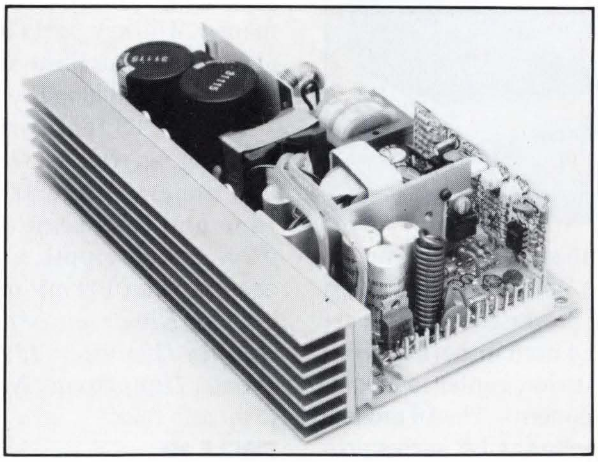
Protection device monitors generators

The FBB frequency-band monitor-relay is designed to monitor single-phase standby or portable generator sets. When the frequency goes above or below the preset limits, an internal relay de-energizes. A differential between energize and de-energize pevents oscillations at the set point. The FBB device operates from 24, 120, or 240 V ac at 50, 60, or 400 Hz.

Diversified Electronics Inc., PO Box 207, Leesburg, Fla. 32748; (800) 874-0619 or (904) 787-7259.

CIRCLE 366

100-W supplies occupy only 53.4 in.^{3}



The XL100 series of 100-W switching power supplies sport an exceptionally small package of 7.5 by 3.75 by 1.9 in., for a volume of 53.4 in.^{3}. Available from CEI, the series features single, triple and quad output models offering combinations of ±5-, ±12-, ±15-, and ±24-V outputs.

All members of the series use a power FET design and operate at a switching frequency of 100 kHz. Typical efficiencies range from 70% to 85%.

For those applications requiring operation in low-air-flow environments, vertical or horizontal heat-sink fins are available at no extra cost. In those cases, the total package size increases only slightly, to 7.5 in. by 4.6 in. by 1.9 in.

The supplies offer current foldback on all high-current outputs, with limits adjusted to individual specifications; dynamic in-rush protection; and a selectable connector for operation at either 110 or 220 V ac. An FCC Class A line filter is included as standard.

Noise and ripple are each 25 mV rms maximum. Line regulation on all outputs is ±0.5% for input variations ranging from 85 to 13 V ac or from 170 to 270 V ac. For the 5-V output, load regulation is within ±0.5%. For the 12-, 15-, or 25-V outputs, it is within ±1% when set by the factory and within −4% to +1% when adjusted by the user. All supplies meet VDE hi-pot specifications, in addition to UL 1012 and CSA safety requirements for data-processing equipment.

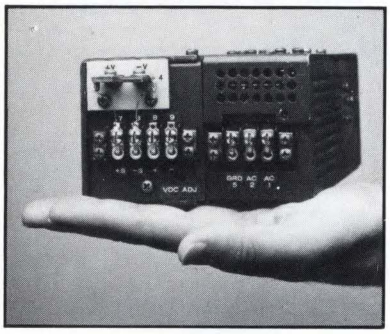
The pricing for lots of 100 is $103 each for the single-output units and $108 each for the quad-output supplies. Delivery is in two to four weeks.

CEI Corp., PO Box 501, Londonderry, N.H. 03053; Matt Pierson, (603) 623-8888 or (800) DC POWER.

CIRCLE 303

POWER

Switching supply has reduced parts count



To enhance reliability, the LR series of fifth-generation switching power supplies incorporates a custom integrated control circuit that replaces 40 discrete components. The 16 models that comprise the LR series provide adjustable fixed voltages of 5 to 48 V. Current ratings include up to 40 A for the lowest-voltage supply and up to 5.8 A for the highest-voltage supply. Ripple is from 10 to 35 mV, depending on the output voltage. Line and load regulation are 0.1%.

The supplies are available in two package sizes: the LRS-53, which is rated for up to 225 W, is 2³/₈ by 4⁷/₈ by 8 in.; the LRS-54, rated for up to 380 W, is 3 by 4⁷/₈ by 11 in. Respective prices for LRS-53 and LRS-54 models are $375 and $460.

Lambda Electronics, 515 Broad Hollow Road, Melville, N.Y. 11747; (516) 694-4200. Stock.

CIRCLE 367

Four-output switcher supplies up to 1050 W

Operating from a 115-V ac single-phase 47- to 440-Hz input, a switching power supply delivers 1050 W of power. The modular unit's four dc outputs provide 5 V at 200 A, −5 V at 1 A, and ±15 V at 1.5 A. The Model M7963 meets MIL-E-16400 and MIL-E-5400 specifications, enabling it to be used in government defense programs and demanding industrial environments. Military parts and packaging also contribute to its high reliability and long life.

The M7963 features current limiting, as well as overvoltage and undervoltage protection. Line and load regulation are 0.2%. Noise, ripple, and spikes are less than 100 mV pk-pk.

Ceag Electric Corp., Power Supply Division, 1324 Motor Pkwy., Hauppauge, N.Y. 11788; (516) 582-4422.

CIRCLE 368

Voltage detector sends ASCII data

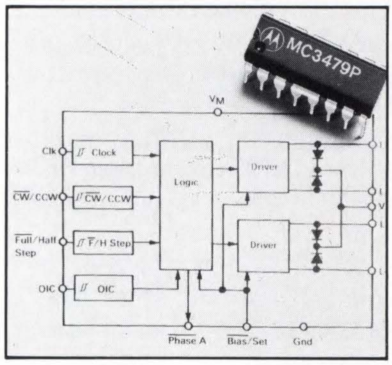
To protect computers and other sensitive electronic equipment, the Remotector VMD400/410 detects, identifies, and quantifies incoming power-line voltage aberrations. The obtained data can be displayed on any ASCII terminal or personal computer equipped with an RS-232-C port. The unit's remote monitoring capability allows data from several locations to be sent over the standard telephone network.

The detector monitors single- and three-phase lines up to 680 V, with adjustable voltage thresholds for sag, surge, low and high average, and impulse levels.

Superior Electric Co., 383 Middle St., Bristol, Conn. 06010; (203) 582-9561. From $3200 to $3500.

CIRCLE 369

Monolithic IC drives two-phase steppers



Housed in a high-thermal-dissipation version of the industry-standard 16-pin DIP, the MC3479P is designed to drive two-phase stepping motors used for disk drives and robotics. Clockwise and counter-clockwise motor operation, including rotation reversal, is selectable. The monolithic IC also permits full or half-step rotation, depending on the logic input, and can handle sustained motor currents of up to ¼ A per phase. A single power-supply pin for both the logic circuit and the motor-coil current covers a range of 7.2 to 16.5 V.

Motorola Semiconductor Products Inc., PO Box 20912, Phoenix, Ariz. 85036; (602) 897-3823. $3.10 (100 units); six to eight weeks.

CIRCLE 370

COMPUTER SYSTEMS

Unix-based computer goes portable

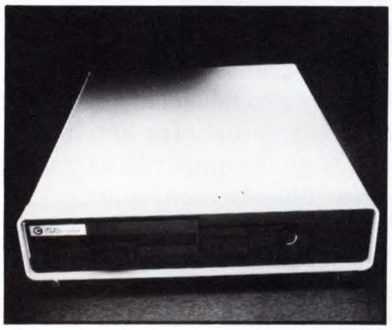
The first computer in a portable package to run under Unix will serve as an aid to software developers and other computer users who must do their work away from the host. The Integral Personal Computer, from Hewlett-Packard, takes its directions from a ROM-based version of Unix III, called HP-UX. (In addition to the convenience of its being stored in ROM, HP-UX is one of the fastest versions of Unix running on any machine.)

The computer uses a 68000 and has 800 kbytes of local memory and a 3½-in. disk drive for up to 710 kbytes of file or program storage. A 25-lb unit 13 in. wide, 16 in. high, and 7 in. deep, it includes a 9-in. electroluminescent display driven by a proprietary graphics processor, a built-in ink-jet printer, five slots for I/O cards, and an HP-IB (IEEE-488) expansion interface.

The $4995 price includes the operating system and the HP Windows and HP Personal Applications Manager software. Available software includes CAD, mathematics and statistics, data-base management, communications, spreadsheets, and word-processing packages, as well as Basic and C interpreters. Delivery is from stock.

Hewlett-Packard Co., 1020 NE Circle Blvd., Corvallis, Ore. 97330; Attn: Inquiries Manager.
CIRCLE 317

Multi-user computer runs 8-/16-bit programs



Enabling users of stand-alone CP/M-based computers to enter a multi-user, multitasking environment while protecting their hardware and software investments is the MC-186, a dual-processor computer capable of handling both 8- and 16-bit programs. When networked to the MC-186, IBM PC-compatible computers can run both CP/M and PC-DOS programs.

The MC-186 operates under MC-DOS, an enhanced version of Concurrent DOS. It allows up to four programs to run concurrently on up to eight different workstations. What's more, up to 255 MC-DOS-compatible computers—such as the IBM PC or leading S-100 bus-based machines—can be linked in a high-speed network.

Gifford Computer Systems, 2446 Verna Court, San Leandro, Calif. 94577; (415) 895-0798.
CIRCLE 371

Memory management enhances multi-user μC

Using a memory-management scheme to enhance multi-user operation, a Multibus-compatible line of 16/32-bit computer systems operates as fast as nonmemory-management types. Using a 68000 or 68010-μP and with the Regulus operating system, the SBE 300 executes at 10 MHz without wait states. The memory-management circuitry contains 32 independent maps, each capable of supporting a real-time task that is 4 kbytes to 8 Mbytes in size.

The CPU interfaces with a high-speed disk controller through the SBEX-SASI multimodule interface. Mass storage is provided by a 10-Mbyte 5¼-in. hard disk and a 320-kbyte 5¼-in. floppy. The rack-mounted SBE 300 has 10 Multibus slots, eight of which are available for expansion. The more compact SBE 350 offers four expansion slots from its total of six.

SBE Inc., 4700 San Pablo Ave., Emeryville, Calif. 94608; (800) 221-6458 or (415) 652-1805. $5795 including software (100 units); 30 days.
CIRCLE 372

Micros link PCs with Unix environment

Two Unix-compatible multi-user business systems—part of the CIES 680 family—offer IBM PC users a cost-effective gateway into the Unix environment. The CIES 680/100 supports 4 to 12 users and is priced between $14,995 and $30,000. The 40-user CIES 680/200 starts at $29,995.

With PCworks, a networking application package, IBM PCs and PC-compatible computers can be linked with the CIES 680 machines. The 680/100 and 680/200 serve as network managers, allowing PCs to communicate with one another and to utilize the 680s' powerful hardware and software. The CIES family supports the Regulus, Pick, and RM/COS operating systems.

CIE Systems Inc., 2515 McCabe Way, Irvine, Calif. 92713; (714) 660-1800.

CIRCLE 373

Lisp machine is attractively priced

With prices starting at $52,500, the Lambda/E is designed to be a cost-effective delivery vehicle for artificial-intelligence application packages. The most compact of all LMI's Lisp machines, it features the same high-speed NuBus architecture common to all the LMI products.

The Lambda/E employs a 32-bit Lisp processor with a 128-Mbyte virtual address space. In addition to 2 Mbytes of physical memory, the system can be configured with multiple disk drives to provide up to 1120 Mbytes of storage.

Lisp Machine Inc., 6033 W. Century Blvd., Los Angeles, Calif. 90045; (213) 642-1116. Second quarter.

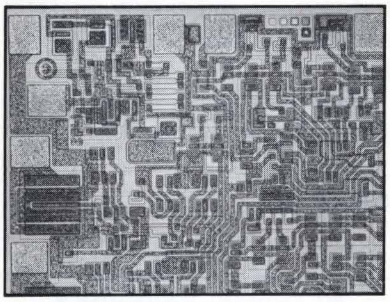
CIRCLE 374

COMMUNICATIONS

Versatile repeater shuts out noise, crosstalk

Although intended for restoring and retransmitting time-division-multiplexed PCM telephone signals riding on a T1 carrier, a monolithic repeater can even handle 2-Mbit/s digital data over up to 6000 ft of twisted-pair lines and includes clock-shutdown circuitry. Since the latter ends transmission if the level of the input signal does not allow accurate reconstruction, the RPT-83 transmits neither noise nor crosstalk.

The chip, from Precision Monolithics, contains a broadbrand preamplifier, an agc circuit, a phase-locked clock oscilla-



tor, and output line drivers. With its gain-bandwidth product of better than 1500 MHz, the preamp compensates for system losses of 45 dB or more at frequencies of up to 10 MHz. Together with the agc circuit, the preamp compensates for signal level changes of 30 dB.

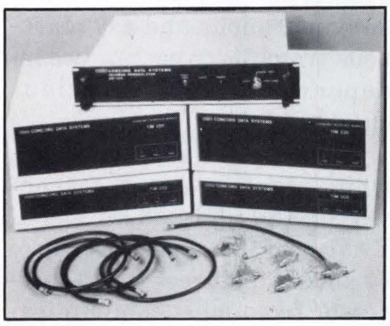
Because it can handle digital signals having frequencies of 100 kHz to 3 MHz, the RPT-83 suits a wide variety of applications, including signal recovery from fiber-optic lines, transmission of geophysical signals from remote sensors over long distances, and of course communication between computers.

The device comes in a 16-pin ceramic DIP and sells for $6.15 each in lots of 100. Small quantities are available from stock.

Precision Monolithics Inc., 1500 Space Park Drive, Santa Clara, Calif. 95050; John Christensen, (408) 727-9222.

CIRCLE 306

Broadband LAN kit permits evaluation



Comprising four Token/Net interface modules, a translator head-end, and broadband cabling, a local area network starter system allows the evaluation of an IEEE-802.4 broadband token-bus network. The Token/Net interface module (TIM) contains a 5-Mbit/s rf modem, a media-access unit that implements the token-passing access method, and a control unit, which provides TIM management functions and the user interface ports.

Concord Data Systems, 303 Bear Hill Road, Waltham, Mass. 02154; (617) 890-1394. $12,000 to $20,000; stock.

CIRCLE 375

Security system uses nonrepetitive passwords

To prevent unauthorized access to any network or multi-user system, the PFX identity authentication system requires a new password for each user every time the system is accessed. The PFX system consists of a personalized hand-held unit, called a PassPort, and the A1000 authentication server, which is a special-purpose computer that attaches to the host computer.

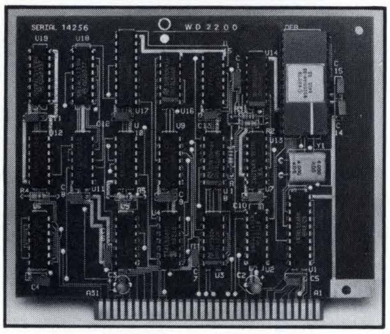
For each identity authentication process, the A1000 supplies the host computer with a nonrepetitive numerical challenge and the corresponding response. The user enters the challenge number into the PassPort unit, which computes the same response as the A1000. Access is gained after the correct response from the PassPort is typed into the terminal.

Sytek Inc., 1225 Charleston Road, Mountain View, Calif. 94039; (415) 966-7330.

CIRCLE 376

COMMUNICATIONS

Encryption board works at 1.3 Mbits/s



One of the fastest encryption devices currently available, the WD2200 data security board allows personal computer users to control or prohibit access to data files. The board, which is based on the NBS-approved WD2001 data encryption chip, operates at a data transfer rate of 1.3 Mbits/s.

Designed for use with IBM PC and PC-compatible computers, the WD2200 automatically encrypts and decrypts data while remaining transparent to the applications software. It protects data on floppies, hard disks, and tapes.

Western Digital Corp., 2445 McCabe Way, Irvine, Calif. 92714; (714) 863-0102. $95 (OEM quantities).

CIRCLE 377

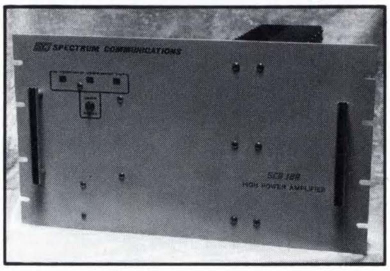
Infrared device links ProNET LANs

As an alternative to physical cable connections, an infrared communications link provides the same high-speed and reliability for ProNET token-passing networks. The infrared device can link the networks together or act as a connecting medium in a single star-shaped ring. Information is transmitted at a speed of 10 Mbits/s over unobstructed distances of up to 250 meters. The device is lightweight and easy to install, requiring only a stable platform.

Proteon Inc., 4 Tech Circle, Natick, Mass. 01760; (617) 655-3340.

CIRCLE 378

Rf power amplifiers cover VHF/UHF ranges



Two rf power amplifiers, the SCA100 and the SCA100V provide output power levels of up to 150 W at 136 to 174 MHz and up to 100 W at 406 to 512 MHz, respectively. The rf drive capability for the SCA100 is 10 W; for the SCA100V, rf drive is 30 to 40 W. A massive heat sink permits cool operation in hot environments, even under 100% continuous-duty conditions. The units come in standard 19-in. rack-mounted enclosures.

Spectrum Communications Corp., 1055 W. Germantown Pike, Norristown, Pa. 19401; (215) 631-1710. $793.

CIRCLE 379

Operating system enhances popular LANs

Advanced NetWare 1.0, a LAN operating system, allows the use of multiple file servers on any NetWare-supported local area network. Each user has simultaneous access to eight servers, with storage capacities reaching 500 Mbytes per server. Advanced NetWare also allows multiple networks to be interconnected through NetWare Bridges, a hardware and software package that connects file servers of different networks. The operating system software can be installed on virtually all popular LANs.

Novell Inc., 1170 N. Industrial Park Drive, Orem, Utah; 84057; (801) 226-8202. $1595.

CIRCLE 380

PC board supports multiple protocols

Linkup, a family of hardware and software products, allows high-speed network communications between IBM PC and PC-compatible computers and mainframes. The plug-in adapter boards support a variety of synchronous and asynchronous protocols on each of two independent communications channels.

The Linkup 1 adapter board, which employs a protocol converter and up to 36 kbytes of RAM, operates at speeds of up to 64 kbits/s and frees the PC processor from most communications tasks. The Linkup XT and XT+ boards offer line speeds of up to 19.2 kbits/s. Together with Linkup protocol and emulation software—including VT52/100, 3270 SNA, 3270 BSC, 3770 SNA, and 3780 BSC—they provide multiple network access.

Information Technologies Inc., 7850 E. Evans Road, Scottsdale, Ariz. 85260; (602) 998-1033.

CIRCLE 381

FACTORY AUTOMATION

Data acquisition and control system is modular

A stand-alone data acquisition and control system is quickly modified or expanded with self-configuring plug-in I/O modules. The ease with which the modules are changed also lowers installed costs. For remote monitoring and control, the SCADAR (supervisory control and data acquisition remote) Series 10 from Burr-Brown is equipped with an RS-232-C interface that permits communications with a host computer, such as an IBM PC or a VAX.

The base unit—a self-contained 8088-based single-board computer—has eight digital inputs, four digital outputs, and four analog inputs, plus four connectors to accommodate additional I/O modules. Up to 255 Series 10 units may be separately addressed in a single system.

Two plug-type terminal blocks at the edge of the modules (cards) enables them to be removed without disturbing the sensor and signal wiring. Available modules offer a choice of analog, digital, and pulsed inputs and digital or analog voltage and current outputs.

The system comes in a rugged wall-mounted or an attractive desktop enclosure. A NEMA-4 housing is also available for harsh environments.

The basic system is priced at \$2500; I/O modules start at \$475. Production shipments are scheduled to begin in March.

Burr-Brown Corp., Data Acquisition and Control Systems Division, 3631 E. 44th St., Tucson, Ariz. 85713; Del Ellis, (602) 746-0711.

CIRCLE 311

FACTORY AUTOMATION

LAN card links STD bus and IBM PC

Based on the WD2840 LAN controller chip, a LAN interface card connects the IBM PC with the STD bus for industrial control applications. The card, designated the NETPC/STD, implements a token bus protocol that is similar to Arcnet, but with higher throughput rates (1 Mbit/s) and greater noise immunity. Lengths of up to 1000 ft between daisy-chained nodes are permitted, with a maximum total distance of 10,000 ft.

Beal Communications, 11020 Audelia Road, Suite C101, Dallas, Texas 75243; (214) 340-2044. $495.

CIRCLE 382

Front end replaces controllers, data loggers

Operating as a stand alone process computer or as a remote front end for distributed control and/or data acquisition, the Safe 8000 replaces programmable controllers and data loggers. It is programmed in Safe Basic, which provides 64 PID control algorithms, 128 timers, and 26 priority interrupts.

The SAFE 8000 comprises a CPU module and up to eight card cages. Each I/O rack supports up to 128 analog channels or 256 digital channels. Communications are handled via two RS-232-C and two RS-422 ports.

Dynage/Controls Inc., 2 Willowbrook Road, Cromwell, Conn. 06416; (203) 635-6257. From $3767.

CIRCLE 383

Tiny camera performs robot vision tasks

Unusually small, lightweight, and rugged, a solid-state video camera lends itself to robotics, industrial, aerospace, and security applications. The Micro-Cam has an optical sense head that is only 3 in.^{3} and weighs just 2.3 oz. The device is encapsulated in a shock-absorbing material for durability in harsh environments. A flexible 6-ft cable links the sense head with the power supply and electronics module, which has an output that is capable of driving a 50-ft video coaxial cable to a remote TV monitor or recorder. The camera operates from an ac line or from a 12-V battery.

Applied Science Laboratories, 335 Bear Hill Road, Waltham, Mass. 02154; (617) 890-5100.

CIRCLE 405

Vision system finds pcb assembly errors

The Checkpoint automatic visual tester simultaneously detects assembly errors on the top and bottom of a loaded printed circuit board. The system's WideEye scanners search the test area to locate any board positioned to within ±0.5 in. of the expected location. It then reads the identification code and calls up the appropriate test routine. Images of both sides of the board are captured and analyzed to detect such faults as missing or damaged components. The 5500 vision system also verifies component identification numbers and shapes, as well as date and lot codes.

Cognex Corp., 72 River Park St., Needham, Mass. 02194; (617) 449-6030. Second quarter of 1985.

CIRCLE 384

Graphics printer is factory-hardened

Complementing the IBM 5531 industrial computer is a graphics printer designed to operate on the factory floor. The printer, like the computer, can withstand temperature extremes, humidity, vibration, dust, and voltage variations. Designated the IBM 5533, the bidirectional printer produces 120 char/s and responds to a variety of commands that control page spacing, select desired character sets, and tab to specified columns.

IBM Manufacturing Systems Products, Mail Drop 4006, PO Box 3025, Boca Raton, Fla. 33432; (305) 998-7066.

CIRCLE 385

PRODUCT NEWS

Rectifiers come in TO-218 plastic cases

Previously available in TO-3 metal cans, three series of silicon rectifiers from **Semicon Inc. (Burlington, Mass.)** are now being offered in TO-218 plastic packages, reducing component costs and simplifying pc board mounting. The SSB Schottky rectifier series replaces the SSH series; the SUR ultra-fast-switching (35-50 ns) rectifier series replaces the SUES series; and the SR switching rectifier series has been renumbered. Prices for the repackaged devices, in quantites of 100, are approximately $4 for the SSB and SUR series and $2.60 for the SR series—vs approximately $5 for the SSH and SUES series and $3 for the previously used SR numbers. All of the devices have a maximum forward current of 30 A at 25°C. The PIV rating for the SSB series is 20 to 80 V, while the SUR and SR series cover 50 to 1000 V.

CIRCLE 386

Program links CAD data, in-circuit test

A software package from **Marconi Instruments' ATE Division (Sunnyvale, Calif.)** automatically generates in-circuit test programs, fixture designs, and computer-aided repair (CAR) graphics using the data derived from a CAD system. Called CADlink, the program uses the CAD data base to develop a color graphic board-description file that enables Marconi's CAR system to display traces and components on pc board assemblies. CADlink employs the same data to generate test programs, assign test nodes, and design the pin layout and wiring for bed-of-nails fixures to be used with the System 80 in-circuit tester.

CIRCLE 387

Program simplifies analog filter design

Filter synthesis software comes from **Analog Design Tools Inc. (Menlo Park, Calif.)** as an option for its Analog Workbench, an engineering workstation for designing analog circuits. The S/Filsyn program allows the user to design a wide range of filter types, including passive, active, microwave, switched capacitor, and digital (FIR and IIR). The user need only specify the performance requirements and parameters for the desired filter, and S/Filsyn indicates which circuits will be needed to meet those criteria. The program accommodates low-pass, high-pass, linear-phase low-pass, bandpass, band-reject, delay-equalizer, and bandpass impedance-matching designs. Priced at $17,500, the S/Filsyn option will be available during the third quarter.

CIRCLE 388

ElectronicDesign

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■ To provide a central source of timely electronics information.
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Want to contact us? Address your correspondence to:

Editor
ELECTRONIC DESIGN
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PRODUCT NEWS

Interface options extend graphics system

To provide a greater number of system environments access to the VectorScan 512 color graphics system, **Applied Data Systems Inc. (Laurel, Md.)** is offering optional serial, parallel, and IEEE-488 interfaces. Also available is a version of the VectorScan system that will plug into the IBM PC and PC-compatible computers. Additionally, the company has announced a memory expansion option to expand the internal memory map from 128 to 512 kbytes, providing the user with four independently stored images.

CIRCLE 389

Bernoulli storage available for Macintosh

Previously available for use with such computers as the IBM PC and those from Compaq, Zenith, and Texas Instruments, the Bernoulli Box is now compatible with Apple's Macintosh computer. The mass storage system, from **Iomega Corp. (Ogden, Utah)**, uses 5¼-in. flexible disk cartridges that hold 5 Mbytes of formatted data and are completely interchangeable from one drive to another. The Macintosh Bernoulli Box, which is 5.1 by 10.7 by 12.5 in., has an average access time of 50 ms. Start and stop times are 5 and 10 seconds, respectively. The unit's suggested retail price is $1895; the 5-Mbyte Iomega cartridges sell for $59.

CIRCLE 390

10-MHz version of 80186 μP is unveiled

In addition to 6- and 8-MHz versions, **Advanced Micro Devices Inc. (Sunnyvale, Calif.)** is now offering a 10-MHz version of the 80186 microprocessor. One of the first such devices available at this speed, AMD's 10-MHz 80186 increases system throughput by 25%. It is packaged in a 68-pin leadless chip carrier and is priced at $98 each in quantities of 100. The processor will also be available in a pin-grid array package during the first half of the year.

CIRCLE 391

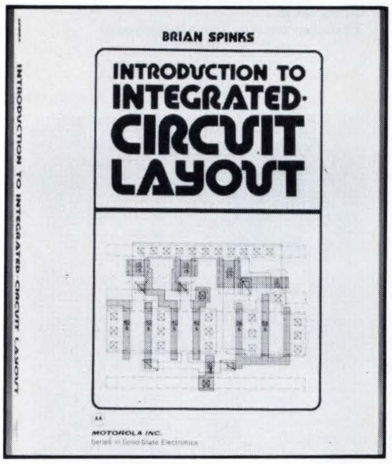
Voice-synthesis chip costs less

Votrax Inc. (Troy, Mich.) has reduced the price of the SC01 voice synthesizer—a solid-state device that enables computers to speak with an unlimited vocabulary—to the lowest level in the product's three-year history. The new price of $32 in unit quantities can be further reduced for larger orders. Encapsulated in a 22-pin CMOS package, the SC01 producers continuous speech at an average data rate of 70 bits/s.

CIRCLE 392

APPLICATION NOTES

Integrated circuit layout and design



Entitled *Introduction to Integrated Circuit Layout*, this textbook provides the basic theory for the layout of MOS ICs and a method for translating a logic diagram into a schematic diagram used for designing an integrated circuit. Also shown are techniques for designing a composite drawing of masks for use in the fabrication of ICs. A glossary of trade vocabulary is included, along with drawings, diagrams, and examples. The material is compiled solely from sources provided by members of Motorola's design staff.

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721; (512) 928-6804. $19.95 (soft cover), $24.95 (hard cover).

CIRCLE 393

Applying conductive coatings

A four-page brochure discusses the use of metallic-filled conductive coatings for RFI/EMI shielding. The bulletin covers surface preparation, mixing and handling, masking of parts, application, quality control and testing, safety precautions, and drying times.

Advanced Coatings & Chemicals, 4343 Temple City Blvd., Temple City, Calif. 91780; (818) 579-6270.

CIRCLE 394

Selecting relays, timers, and controls

A 36-page booklet serves as a valuable reference manual for the selection of electronic and electromagnetic components and controls. It contains definitions, descriptions, illustrations, and applications information for various components, including most types of relays, timers, counters, switches, and proximity sensors.

Relay Specialists Inc., 13-00 Plaza Road, Fair Lawn, N.J. 07410; (201) 797-3313.

CIRCLE 395

Using packaged capacitor assemblies

Employing multiple-capacitor assemblies is the subject of a four-page treatise, which discusses the reasons for doing so and the effects—both obvious and subtle—of series and parallel connections on operating parameters. Reliability data is also included.

Tansitor Electronics Inc., PO Box 230, West Road, Bennington, Vt. 05201; (802) 442-5473.

CIRCLE 396

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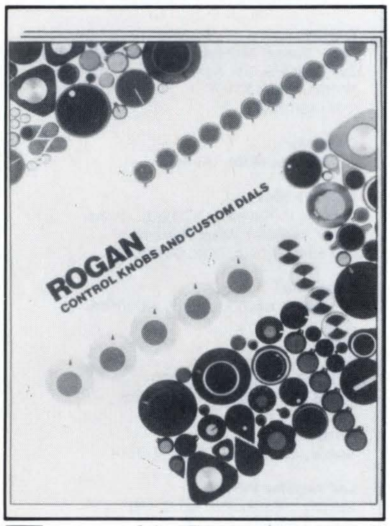
NEW LITERATURE

Control knobs and custom dials



Featured in Rogan's control knobs and custom dials catalog is the company's copyrighted material specification and mechanical tolerance standards—the first published standards in the knob industry. The data helps determine exactly how a given knob will perform, both functionally and aesthetically, in a given application. The products in the 44-page catalog are fully illustrated and displayed with skirts, inlays, indicators, and dials.

Rogan Corp., 3455 Woodhead Drive, Northbrook, Ill. 60062; (312) 498-2300.

CIRCLE 397

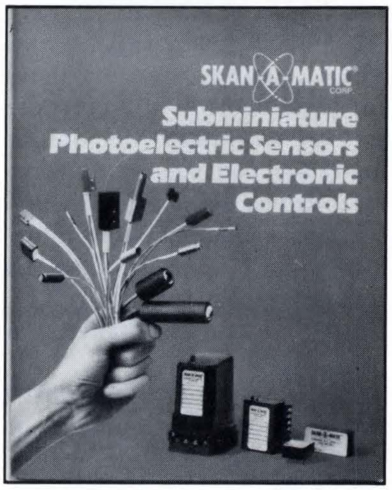
Filters and traps for cable TV

Patterned as a tutorial guide, a comprehensive catalog (C/84) specifies filters and traps for cable television, as well as filters for MATV, SMATV, and TVRO systems. The catalog offers complete descriptions and applications for all products. It also explains the pole trap leakage standard, the factory test method to ensure that trap leakage conforms to FCC requirements.

Microwave Filter Co. Inc., 6743 Kinne St., East Syracuse, N.Y. 13057; (315) 437-3953.

CIRCLE 398

Photoelectric sensors, controls

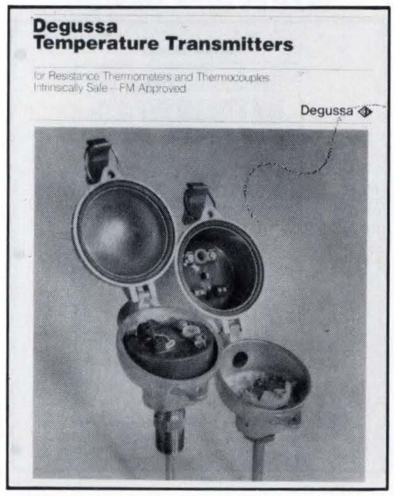


More than 30 product series are featured in a 114-page catalog of subminiature photoelectric sensors and electronic controls. Products include through-beams, reflective scanners, and special-purpose scanners. An informative technical section describes the individual components of a photoelectric system and discusses response time, sensing modes, output devices, and selection criteria.

Skan-A-Matic Corp., Route 5 W., PO Box S, Elbridge, N.Y. 13060; (315) 689-3961.

CIRCLE 399

Temperature transmitters



Temperature transmitters for resistance thermometers and thermocouples are the subject of an eight-page booklet. The document contains detailed drawings, design specifications, and application diagrams.

Degussa Corp., Metal & Catalyst Division, 104 New Era Drive, South Plainfield, N.J. 07080; (201) 757-6500.

CIRCLE 400

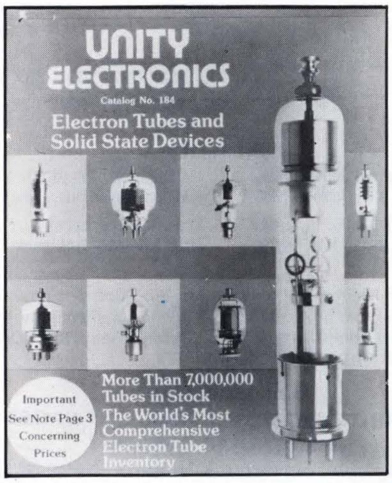
Solid-state choppers and analog switches

Solid-state choppers and analog switches are specified in a 32-page brochure, which contains numerous circuit diagrams, illustrations, mechanical data, and applications information. The miniature devices are suitable for military and industrial applications.

Solid State Electronics Corp., 18646 Parthenia St., Northridge, Calif. 91324; (213) 993-8257.

CIRCLE 401

Electron tubes and solid-state devices



Electron tubes—such as special-purpose industrial tubes, magnetrons, klystrons, traveling wave tubes, and ballasts—are listed in a catalog, along with prices and conversion charts. Four pages of ICs and solid-state devices are also included, covering Schottky devices, transistors, varactors, rectifiers, microprocessor components, and voltage regulators.

Unity Electronics, 107 Trumbull St., Elizabeth, N.J. 07207; (201) 351-4200.

CIRCLE 402

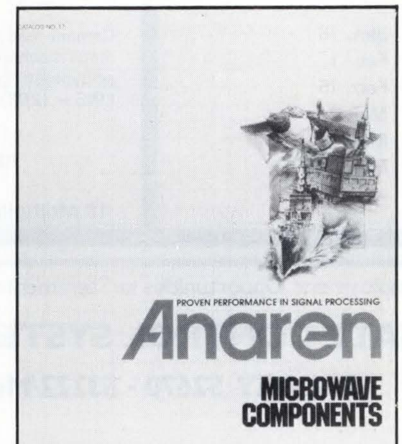
Resistance temperature detectors

More than 200 resistance temperature detectors (RTDs) and accessories are described in a 60-page catalog (TS-101), including models for improved sensing in both OEM and end-user systems. An introductory section helps the reader compare sensor types, choose an RTD element, and identify possible sources of system error.

Minco Products Inc., 7300 Commerce Lane, Minneapolis, Minn. 55432; (612) 571-3121.

CIRCLE 403

Microwave components and systems



Over 400 microwave components are presented in a 224-page catalog (No. 17) written in a simple-to-use, cross-referenced format. Among the products covered are 90° and 180° hybrids, directed couplers and power dividers, mixers, modulators, p-i-n attenuators, and phase discriminators. Complete application and technical data is given for each component. The catalog also highlights Anaren's digital EW receiver line, quality-assurance program, and hi-rel capabilities.

Anaren Microwave Inc., 6635 Kirkville Road, Syracuse, N.Y. 13057; (315) 432-8909.

CIRCLE 404

Recruitment Advertising

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Conduction engineering/economic analysis of equipment malfunctions and recommending appropriate corrective action. Designing/developing modifications to analylog/digital circuitry, data transmission links, communications equipment, electro-mechanical equipment, or process control computer programs.

Reviewing/approving field modification requests, making corrective design changes to hardware or software, and updating documentation.

MINIMUM QUALIFICATIONS:

Two years of experience in the California state service performing the duties of an Assistant Control System Engineer. **or** Three years of professional control system or electronic experience, including at least two years in the design, development and appplication of control systems utilizing complex electronic circuitry, combinations of electronic, electro-mechanical and hydraulic equipment, digital logic techniques, data transmission and interface equipment; and equalivalent to graduation from college with major work in engineering, or related physical sciences.

An oral examination will be given in California during March/April 1985 and will cover a candidate's:

Knowledge of: Practices and techniques involved in the design, development and maintence of complex automatic process control systems.

Ability to: Perform research work on new equipment for process control system applications and analyze technical information pertaining to the operation of existing control systems with a minimum of guidance or training; work cooperatively with others; give technical direction to subordinate personnel.

Submit resumes by January 31, 1985 to: Department of Water Resources
1416 Ninth Street, Room 304-2
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Attention: Exam Unit

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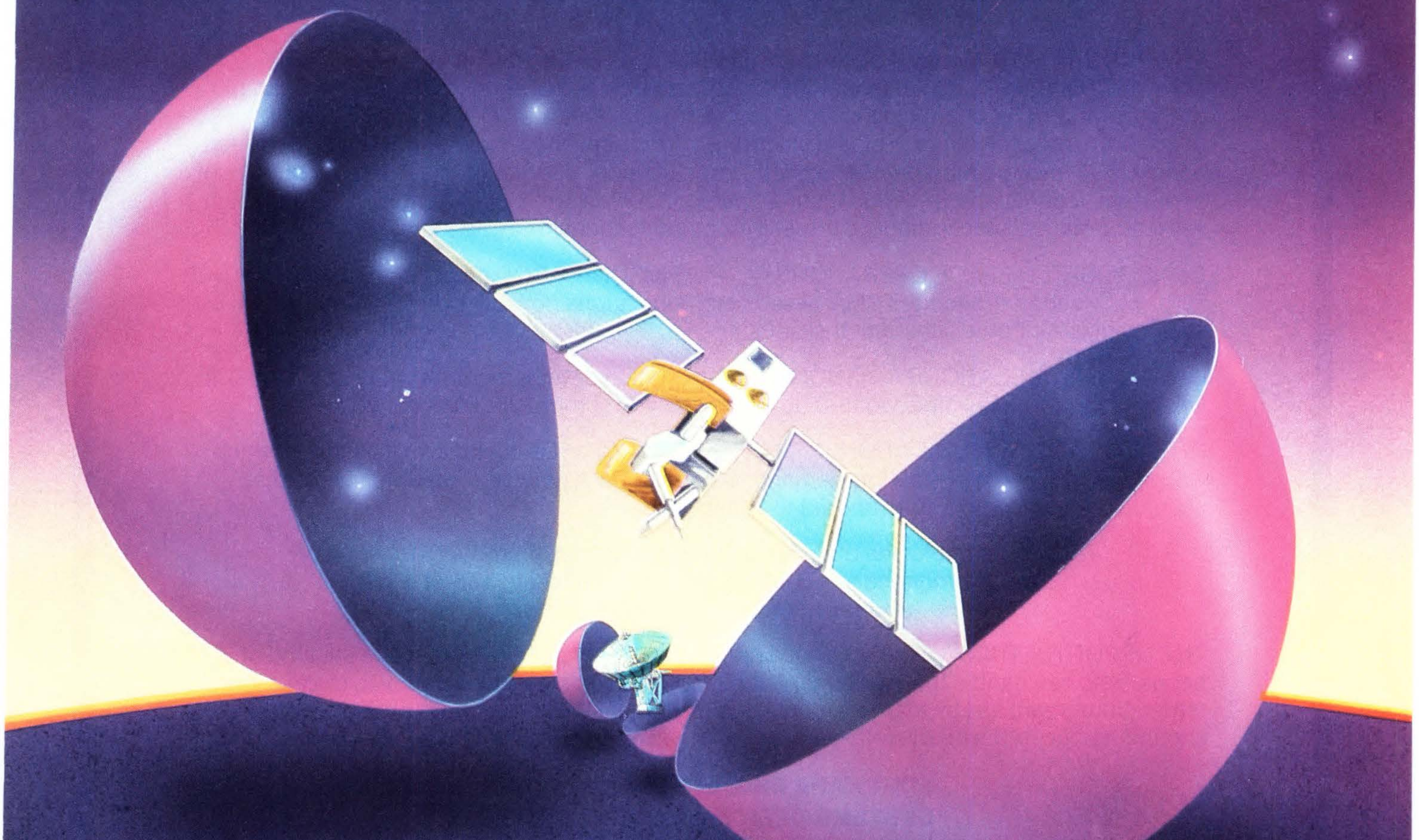

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WE'VE GOT IT!

THE PROGRAMS. . . Today, Fairchild Communications & Electronics Company is an evolving division of Fairchild Industries which draws on established traditions of leadership and innovation. Our charter is to meet new market challenges in telecommunications by building on our experience in digital electronics. This challenge is met through an integrated approach. . . design, manufacturing, testing and support. . . executed by a dedicated team of engineers, technicians, and management personnel. Now we're staffing for programs which will lead America's technological thrust in communications well into the next century.

CONSOLIDATED SPACE OPERATIONS CENTER (CSOC). . . DOD program to develop the most sophisticated, secure, TDMA-based communications network ever installed. This system links Air Force sites with the CSOC.

NASA COMMUNICATIONS (NASCOM). . . Earth station development for systems which will link NASA operational sites world-wide with a satellite communications network.

INTEGRATED COMMUNICATIONS CONTROLLER (ICC). . . Development of systems which will provide the latest in real-time demand assigned TDMA networks capable of providing secure, integrated voice, data and video-conferencing.

The key technologies underlying the development of products for each of these programs are TDMA, encryption, switching and network management under software control.

THE OPPORTUNITIES. . . The advanced projects on board at Fairchild require the kind of people who can handle the challenge. Bright, motivated professionals ready to make a long-term commitment as key team members and leaders for these important projects. We're expanding our staff with the following positions; all require relevant degrees and experience.

- ☐ **SOFTWARE ENGINEERS**
- ☐ **SYSTEMS DESIGN AND TEST ENGINEERS**
- ☐ **COMMUNICATIONS SALES MANAGER**
- ☐ **HARDWARE DESIGN ENGINEERS**
- ☐ **PROGRAM DIRECTOR**

THE LOCATION. . . Fairchild Communications & Electronics Company is located in Germantown, Maryland on a 200-acre complex only 30 minutes from the heart of the Nation's Capital. Our campus-like facility offers an exceptional working environment. You'll see recreational facilities which include a golf course, tennis courts, softball field, and workout facilities. It's the ideal place to expand professionally in a relaxed atmosphere. For more information on our current and planned staffing requirements, write: Professional Employment, Fairchild Communications & Electronics Company, 20301 Century Blvd., Mailstop S-5, Germantown, MD 20874-1182 or call (301) 428-6493.

FAIRCHILD

COMMUNICATIONS & ELECTRONICS COMPANY

An Equal Opportunity Employer M/F

NEW CHALLENGES IN COMMUNICATIONS

The Sperry Challenge in Salt Lake City
Delivering innovative systems in an exciting and competitive marketplace is a formidable challenge—one that we accept.
At work within the Micro Products Division and Sperry Network Systems groups, we'll surprise you with uncommon opportunities for career growth in state-of-the-art microprocessor and network communications technology.
We are seeking individuals with expertise in the following areas: UNIX Software programming, Systems design engineering, systems programming, SNA, DCA, OSI communications architectures, LAN technology communication software engineering, and many others.
At Sperry, you'll work in a business environment which encourages your participation as you share responsibility with other team members, for developing new generations of micro-based products and data communications systems.
This is the Sperry challenge and we invite your participation.
And, nowhere in America will you find better skiing than in Utah—powder snow, blue skies and sunshine less than 40 minutes away from work.
If you are interested in the Sperry challenge, please send your resume to:
SPERRY, Employment Dept., Attn: Dept. 1D
322 N. Sperry Way, Salt Lake City, Utah 84116
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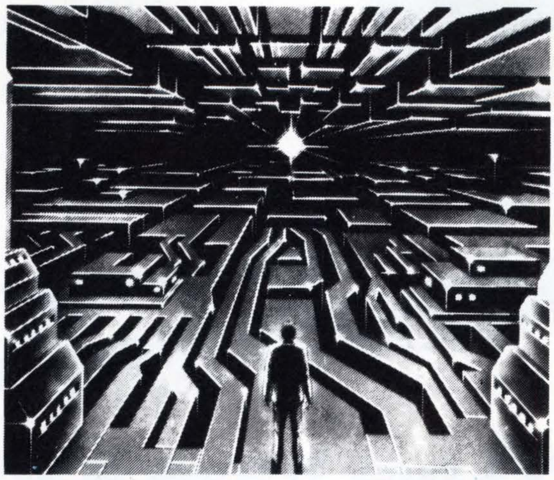
INTEL...HAVING A VISION.



MAKING IT HAPPEN.

Our leadership is a result of our technology...that's how the VLSI revolution came about, here at Intel. Our standard setting microelectronics developments include the first RAM, EPROM, microprocessor, single-board computer, microcomputer development system, and million-bit bubble memory. We also originated CMOS and HMOS technologies, and we will continue to set the standard in the next generation of advanced microprocessors, memory devices and microcontrollers. Intel professionals have vision, desire, convictions and discipline to lead...do you?

PROCESS DEVELOPMENT SCIENTISTS

Carry out independent advanced development in the areas of thin films, plasma etch and diffusion for next generation IC products. Areas of emphasis are:

- LPCVD enhancement, and
- Defect reduction and yield improvement.

All positions require a PhD in Chemistry, Chemical or Electrical Engineering or related fields, with at least 5 years experience in research and development.

ADVANCED MEMORY DESIGN ENGINEERS

Responsible for the design and characterization of advanced memory products, including DRAM, E/E^{2}PROM, Static RAM and Magnetic Bubble Memories. Responsibilities include all phases of logic design, circuit design, characterization and transfer. BS/MS/PhD in Engineering Sciences plus related experience.

FUNCTIONAL/PHYSICAL DESIGN CAD

We are seeking CAD professionals with logic and fault simulation, behavioral modeling and mixed level simulation for our Functional Design area. Our Physical Design area requires expertise with layout synthesis including sticks, place and route, cell compilers as well as post design tools including pattern generation and frame generation. CAD and workstation experience desired.

SYSTEMS CAD (Oregon)

This area encompasses functional and physical aspects of board and system-level products. This includes functional through gate-level simulation, testing and test generation, and automatic placement and routing for boards.

PRODUCT ENGINEERS-DEVELOPMENT

Will develop test programs, yield/cost analysis on Sentry, Teradyne, LTX or Megatest systems. Responsible for product characterization and new product introduction for memory component, microprocessor or peripheral products groups. BS/MSEE and related MOS/CMOS experience.

VLSI DESIGN ENGINEERS

Design new high-integration, high-performance CMOS/CHMOS microprocessors or peripherals. Responsible for architecture/microarchitecture simulation, chip and circuit design, chip planning, and layout supervision on CMOS/CHMOS products within our peripheral or microprocessor groups. BS/MS/PhD in Engineering Sciences plus related experience.

Dedicated professionals are now extending our technology into a growing family of components for the future. If you have vision, we'll help you make it happen. For consideration, send your resume to the locations that interest you c/o Intel Employment, Dept. 155830, **Phoenix, AZ,** 5000 W. Williams Field Road, Chandler, AZ 85224; **Santa Clara, CA,** P.O. Box 2546, Santa Clara, CA 95051; **Folsom, CA,** 151 Blue Ravine Road, Folsom, CA 95630; **Albuquerque, NM,** 4100 Sara Road, Rio Rancho, NM 87124; **Portland, OR,** 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124-6497. An Equal Opportunity Employer M/F/H.

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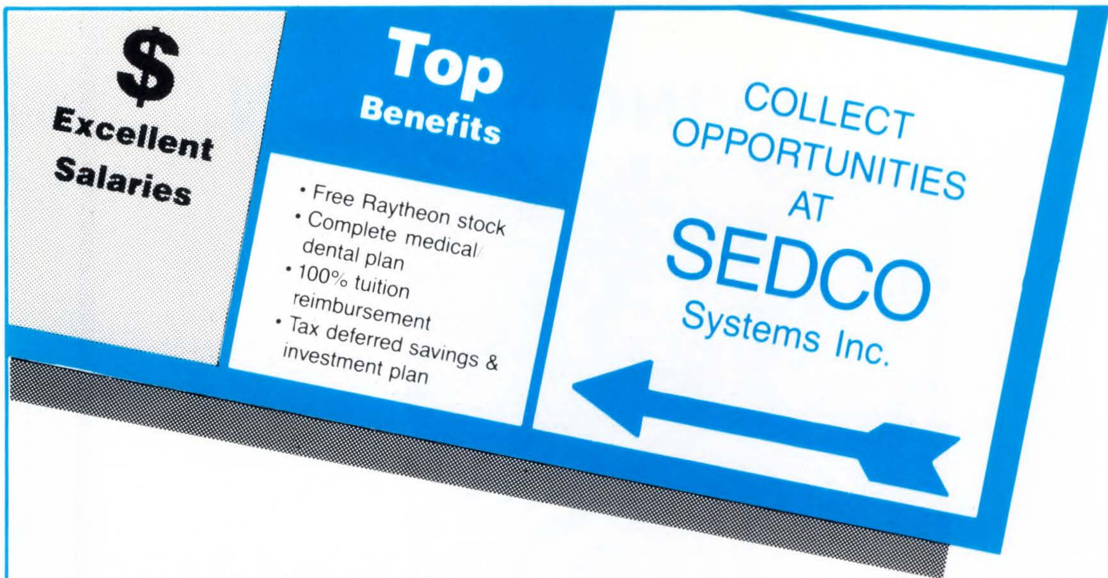


At SEDCO we have a monopoly on the best engineering careers.

We've cornered the market on blue-chip careers in engineering as well as manufacturing and engineering support. We achieved this enviable position by capitalizing on the technological strength and financial resources of Raytheon, our parent company. We've also invested heavily in diversification, expanding from independent research in advanced electronics to full performance capability—from initial conceptual design to systems production and support services.

At SEDCO, the pay-off for your expertise is both immediate and long-term. **Immediately,** you'll be involved in pushing the limits of microwave component and phased array technology with emphasis on its application to our national defense. For example, you could be part of a team responsible for ECM Phased Array Antenna Systems which is an integral part of the B-1 Program. In the **long-term,** you can look forward to a unique kind of career satisfaction. The kind you get from a professional environment where you're given meaningful responsibility and rewards, where your individuality is encouraged and where you have the opportunity to effect change.

We have a full range of engineering, manufacturing and engineering support positions immediately available. All require degrees (typically a BS/BSEE for engineers) and directly applicable and current experience combined with previous work in advanced electronics for the military.

ENGINEERING

MICROWAVE

Section Managers

7–10 years' experience required, including project or program management (manpower and budget allocation). Will have responsibility for design and development of antennas and passive microwave components. Other duties include proposal writing and subsystem analysis.

Sr. Engineers

Requires 5–10 years' experience. Will design/develop antennas and passive microwave components (2–40 GHz) and maintain budget and schedule control over approximately 5 people.

Engineers

Requires 2–5 years' experience. Will design/develop passive microwave components (2–40 GHz) and antennas.

ADVANCED SYSTEMS

Sr. Engineers

- Will be responsible for the support of all IR & D programs. Requires BSEE and 6+ years' experience in receiver and digital signal processing techniques with knowledge of microprocessor software—2900 family—essential.
- Primary responsibilities will focus on advanced ECM applications toward new business. BSEE and 6+ years' experience in radar ECM and threat intercept systems engineering required.

Engineers

- Will assist on proposal preparations and interface with support groups. Will also be involved with theoretical analysis. Requires BSEE/Physics and 2+ years' experience in RF technology including stripline, antenna and transition lines.
- Will design driver circuits, be involved in test measurement and assist on proposal preparations. Requires BSEE/Physics with 2+ years' experience in Computer Program in Basic or HFL required. Working knowledge of transistors. LSI and IC's mandatory.

Proposal Managers

Will edit, organize and write proposals for new business and be involved in cost management. Requires BSEE and 8+ years' experience with related knowledge of ECM systems, phased array antenna and control processor engineering necessary.

ELECTRICAL

Principal Engineers/Section Managers-Analog Design

MBA and 15 years' experience required. Will direct feasibility studies and proposal generation for high speed analog signal processing (AD/DA converters), including analog systems architecture. Will also supervise designers of power supply voltage regulators. Strong management background essential.

Sr. Engineers

- Requires minimum 8 years' experience. Will design analog circuits and power supply, including switching and linear voltage regulators, power switching circuits and shunt regulators. Will also be involved in electrical power system and analysis.
- Requires 8 or more years' experience in RF IF MIC receiver design in the frequency range of 100 MHz to 10 GHz and active passive microwave integrated circuit design (2–18 GHz). Must have working familiarity with filters, attenuators, limiters, switches and solid state amplifiers.
- Requires minimum 7 years' experience in hardware/software design for computer-based process control, ATE, precision measurement and positioning equipment. Will conduct hardware software integrations and system text. Must be experienced with the INTEL 8080, Z80 microprocessors as well as HP 9836 microcomputers.

Please send a detailed resumé, indicating position applied for and including salary history, to: **Director of Personnel, Dept. ED10, SEDCO Systems, Inc., 65 Marcus Drive, Melville, N.Y. 11747**

SEDCO SYSTEMS, INC.

A Raytheon Company

US Citizenship Required

An equal opportunity employer, M/F

MOTOROLA'S GOVERNMENT ELECTRONICS GROUP

Motorola's Government Electronics Group is a leader in the research, development and production of electronic hardware for our country's defense, national security and space programs. Our success is founded on the strengths of people like Ralph Love. People with the minds to imagine and the skills to do.

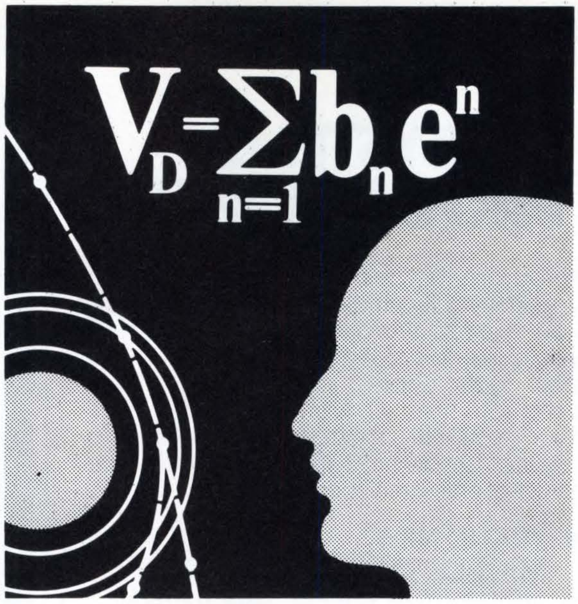
If you are such an individual and have a background in one of the following areas, we'd like to talk to you.

Principal System Engineers/Designers
Knowledge should include communications signal processing theory, awareness of current communications technology and strengths and weaknessess of hardware/software for implementation trade-off purposes. Abilities must include system concept development, testing and refinement. Prefer BSEE and 5 years related experience. Contact Paulette Dorris.

Senior Mechanical Engineers — Responsible for conducting thermal, structural and vibration analysis in support of project requirements during product design, fabrication, assembly and testing. Experience in electronic packaging for military applications, design of mechanical elements of mechanisms and exposure to DOD-STD-100 and DOD-D-1000 highly desirable. Prefer BSME and 4 years experience. Contact Jerry Chadwick.

Software Manager — Engineer to manage a large software development project. Must have technical ability to understand unique hardware interfaces, design and evaluate multi-tasking operating systems and project cost and schedule for future developmental tasks. Prefer BSEE or BSCS with 10 years related experience. Contact Jerry Chadwick.

Systems Engineers — Senior level engineers to direct the technology inception effort for radar programs. Considerable customer interface in conceptualizing system technologies to enhance and expand current projects into fully functional C^3I systems. Prefer BSEE with 10 years experience. Project leader experience a plus. Contact Jerry Chadwick.



Test Equipment Development Manager — Manager of development projects for manual and automatic test equipment for missile radar fuze development and production programs. Experience in test equipment system architecture, system level spec generation, radar signal processing and design of computer driven IEEE bus controlled systems. Contact Jerry Rule.

Join the people of Motorola's Government Electronics Group. The benefits are many, including sunny Arizona — a land as beautiful as it is booming with recreational and cultural outlets. For more information, send your resume in confidence, or call the appropriate technical recruiter collect at (602) 949-3759. Motorola Government Electronics Group, 8201 E. McDowell Rd., Dept. B241, Scottsdale, AZ 85252.

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Government Electronics Group

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"If you want a broad spectrum of experience, you'll find the right technical outlet at Motorola."

Ralph Love
ENGINEERING MANAGER, Radar Systems Office

The Mind to Imagine
THE SKILL TO DO

programming

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If you are the best Systems Programmer you know... If a tricky problem can keep you excited from sunset to sunrise... If you'd like to work hard using the world's best tools to produce the world's best products, then we want you at Microsoft. You'll work with a few others like yourself to create breakthroughs in the software state-of-the-art. Working with...

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Microsoft provides the best systems programming work environment...

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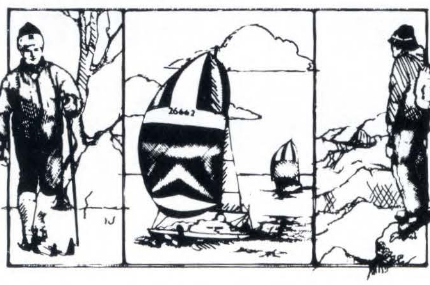
...a small company with lots of interaction and sharing of ideas.

And to make a good thing better, Microsoft is located in the great Pacific Northwest with mountains, skiing, beaches, forests, rivers and lakes all within easy reach. We're just 15 minutes away from Seattle - a livable city with mild winters and affordable housing. Send your name, address, phone, and summary of languages and systems you've worked with (and sample of your source code, if you have it) to: **MICROSOFT CORPORATION, Department SC, 10700 Northup Way, Box 97200, Bellevue Washington 98009.** We are an equal opportunity employer.



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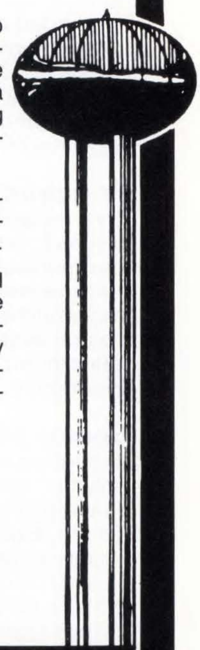
General Motors' Advanced Product and Manufacturing Engineering Staff has immediate challenging opportunities in Controls Engineering.



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Seeking CNC control hardware specialists to help develop state-of-the-art high performance equipment and cells for the manufacture of automotive components. Those applying should possess a BSEE or MSEE and should have working knowledge of interfacing equipment to automatically guided vehicles and robots.

Candidates must have U.S. Citizenship or Visa status which permits them legally to accept permanent employment under U.S. Immigration laws.

Exploring new automotive frontiers with GM means virtually unlimited opportunity to realize your full career potential, plus the outstanding salaries and benefits only the leader in its industry can offer. To receive prompt, confidential consideration, please submit your resume with salary history/requirements to:

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Software Engineers

Space Applications Corporation, a leader in systems and software engineering, is involved in projects of international impact — projects that offer the challenge and diversity you deserve.

Opportunities exist for individuals with a BS/MS/PhD in Math, Physics, Engineering or Computer Science and experience in spacecraft command and control, computer communications security, satellite communications, military C^3I and/or SIGINT systems analysis. Prior aerospace experience desirable.

We have openings in Santa Ana, CA; Sunnyvale, CA; Seattle, WA; and Washington, D.C.

We offer an attractive salary and benefits package. For prompt, personal consideration, send your resume with geographic preference to: **Carmen Barbee, Dept. ED, Space Applications Corporation, 300 E. Sandpointe Ave., Suite 300, Santa Ana, CA 92707.** An Equal Opportunity Employer/U.S. Citizenship Required.

SPACE APPLICATIONS CORPORATION

HARDWARE/FIRMWARE/SOFTWARE ENGINEERS

Bendix Test Systems' significant growth in ATE means significant career opportunities for you.

Dramatic ongoing projects and R&D programs are stretching our ATE capabilities. . . and engineers. . . to the utmost.

We are a pace-setting division of the Fortune 30 Allied Corporation; our operations in Teterboro, New Jersey are expanding. There's an exciting range of new openings. Filling them has our highest priority.

If you have a minimum of a BSEE (or degree in math, physics or CS) and have the experience specified, here are "invitations" to initiate career discussions, and broaden your professional horizons:

Manager, Software Engineering

Must have at least 10 years in development of SW to support avionic systems, preferably automatic test equipment software. MSEE and 5 years of leadership experience preferred. Knowledge of modern software languages and techniques essential. Background in ATE highly desired. Will take charge of the development of ATE compilers and test executive programs for multiple projects. Will also manage the development of next generation ATE software.

Supervisory RF Engineer

At least 5 years of specialized experience in ATE/RF applications essential. Will assume RF design project responsibilities. Supervisory experience beneficial.

Microprocessor-based Designer/Engineer

Openings for engineers with at least 1 year's experience in digital microprocessors and software, as well as for senior engineers with 3 or more years related experience and knowledge of Intel 8086 family, development tools, and IEEE-488 bus protocols.

Senior Firmware Engineer

Staff and senior staff openings for engineers with a minimum of 5 years experience in firmware engineering, and thorough knowledge of Assembly language, modern microprocessor architectures and interfaces, and/or Intel 8086 programming and broad digital hardware/analog circuitry design/debug experience.

Waveform Analysis Engineer

Openings for senior and staff engineers with 5-15 years of experience in the field, and knowledge of Fourier Analysis technique, sampling and other HW/SW techniques used for digitizing and analysis of waveforms. Knowledge of Digital Signal Processing techniques and D/A and A/D conversion techniques highly desirable.

Software Designer/Engineer

Openings at staff, senior engineer and engineer levels. Designers must have 5-10 years of software design experience; ATE experience preferred—as is knowledge of ATLAS, operating systems, compilers and test executives, as well as modern computer architectures. Other openings require 1, 2 or more years of applicable experience.

Artificial Intelligence Engineer

Senior and staff level openings. Must have 5-15 years of background, and working knowledge/experience of knowledge-based or expert SW systems. Knowledge of heuristic techniques and application to systems is an asset—as is ATE experience.

Graphics Engineer

5-10 years of experience in field essential—as is thorough knowledge of high order languages and data structures. BSEE or CS degree vital; advanced degree preferred.

Analog System Designer

Must have at least 4 years experience in the design and development of analog control systems. Ability to control a project also necessary. Digital experience is an asset.

Microwave/Millimeter Wave Engineer

Openings for engineers with a minimum of 5 years of experience in microwave technology. Specific electronic warfare and millimeter wave experience required.

For prompt, confidential consideration, and full briefing by senior managers if qualified, please send your resume with salary history to: Mr. Blaise A. Russo, Manager, Employee Relations, Bendix Test Systems Division, Route 46, Teterboro, New Jersey 07608. An equal opportunity employer.

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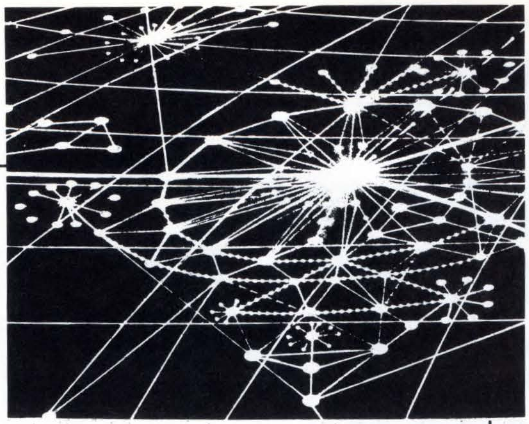

Engineers

We Are Improving Communications Through Your Imagination

At CASE RIXON, you will find a system of internal communications designed for the professional. It allows you to concentrate on improving global communications instead of fighting red tape. The spirit of our company is one of dedication, enthusiasm and adventure. CASE RIXON believes in its product and believes in its people. We recognize and reward innovative thinking and we appreciate the impact your ideas can have on the data communications industry.

For those individuals who are interested in accepting responsibility and who grow with each challenge, CASE RIXON offers the ideal climate for making real contributions. We currently have opportunities in the following areas:

- Network Management Architecture
- LANS Research Engineering [Broadband]
- Hardware Design Engineering
- Software Design Engineering
- LSI Design Engineering
- Applications Engineering [pre and post sales support]

For complete information about these outstanding positions, call John Jaeger at [301] 622-2121, or send your resume in confidence to: CASE RIXON COMMUNICATIONS, Inc., 2120 Industrial Parkway, Silver Spring, MD 20904. An equal opportunity employer.

CASE
COMMUNICATIONS

Become Part Of The Success Of MSB System's New Medical Products Division

MSB SYSTEMS is a recognized leader in advanced acoustical signal processing technology. The following key technical positions involve start-to-finish project responsibilities and offer exceptional professional growth.

System Design Engineer

BSEE with at least 5 years experience in the design and development of digital image processing systems. MSEE preferred. Responsible for the architectural and functional design of high performance image processors and of picture archiving and communication systems.

Digital Signal Processing Engineer

MSEE, Ph.D. preferred, with at least 3 years experience in the computer modelling, analysis and design of adaptive signal processing or image processing systems. Must have a strong background in modern estimation theory and spectral analysis techniques. Knowledge of hardware and software implementation of digital signal processors is highly desirable.

Digital Design Engineer

BSEE, MSEE preferred, with minimum 3 years experience in the design and development of digital signal processing and microprocessor based systems.

Analog Design Engineer

BSEE, MSEE preferred, with at least 5 years experience in the design and development of H.F. circuits, including pulsers, power amplifiers, low noise receivers, adaptive controls, A/D and D/A converters, with a strong background in interfacing analog and digital circuitry.

We provide excellent salaries, a comprehensive benefits program and a superb life-style in Southern Connecticut, only one hour from N.Y.C. Please send your resume, in confidence, to: Operations Manager, MSB SYSTEMS, INC., P.O. Box 2029, Westport, CT 06880. An Equal Opportunity Employer.

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RF Design	$49,000
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Digital Logic	$44,000
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Microprocessors	$44,000
CAD/CAM Systems	$45,000
Fiber Optics R/D	$45,000
Microwave Systems	$50,000
Medical Diagnostics	$49,000

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ENGINEERING OPPORTUNITIES

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Superior technology has pushed FMC to the forefront of our field, and it's kept us growing. Our current objective, which continues ten years of sustained growth, will increase the size of our electronics-engineering staff by 35% by the end of 1985. We're prepared to offer challenging engineering opportunities in project leadership to qualified professionals with 5 or more years experience.

SEQUENCE AND CONTROL LOGIC ENGINEER

You'll direct the development of advanced control systems incorporating interactive displays, 16-bit microprocessors, and self-diagnostics. We require a BSEE or MSEE, 5 years' experience or more in logic design, microprocessors, and software development, as well as some supervisory background and a record of effective interaction with mechanical designers and non-engineering professionals. Defense industry experience would be an asset.

SENIOR LOGIC & MICROPROCESSOR DESIGN ENGINEER

You'll provide support to all phases of design and development of high-performance electronics equipment utilizing the most recent advances in digital logic and microprocessors. We require a BSEE or MSEE, and at least 5 years' related experience. A working knowledge of the 8086 would be a plus.

DATA BUS ENGINEER

You'll be involved in design and development of state-of-the-art fiber optic data bus systems employing 16-bit microprocessors, semi-custom ICs and high speed logic. A good knowledge of data bus architecture, protocol, reconfiguration, and error handling are required. BS/MSE and 5 years of experience are required.

MATERIALS ENGINEER

Excellent opportunity for candidate seeking an application-oriented research environment. Solid understanding of composite materials, high temperature coatings, materials fabrication process and corrosion resistance is essential. An MS in Materials Science is required.

ARTIFICIAL INTELLIGENCE SCIENTIST

Qualified professional is needed to develop Expert Systems in Symbolic or equivalent machines for DoD application. Solid experience with Rule Based Expert Systems and one of the AI languages (LISP, C, PROLOG, etc.) is preferred. Candidates holding PhD in Computer Science; PhD in Psychology with computer exposure and 4 years experience; or MS in Computer Science with 4 years experience will be considered.

The satisfaction of an engineering career with FMC does not stop with powerful technology and flexible career paths. We also offer compensation that will reward your experience and skills with attractive salaries and generous benefits. **For consideration, please call Sherry Peterson at (612) 572-6540 or Dennis Mixdorf at (612) 572-6539, or forward your resume and salary history in confidence to: Professional Staffing, FMC Corporation, Northern Ordnance Division, Dept. ED, 4800 East River Road, Minneapolis, MN 55421.**

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Career Extra, the industry's leading recruitment newspaper is now reaching over 200,000 engineering and computer professionals on the move.

1985 CAREER EXTRA ISSUES MONTHLY!

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March	March 15	March 22
April	April 12	April 19
May	May 10	May 17
June	June 7	June 14
July	July 8	July 12
August	August 16	August 23
September	September 13	September 20
October	October 11	October 18
November	November 8	November 15
December	December 6	December 13

Career Extra combines with Electronic Design and Systems & Software to give you maximum savings at frequency discounts. *Plus* bonus distribution at the hottest trade shows and job fairs in the industry!

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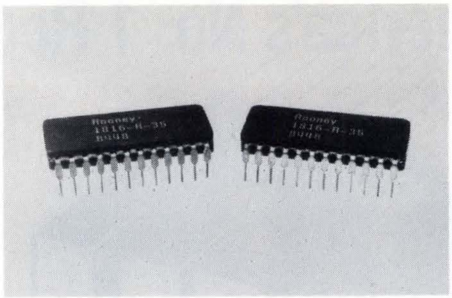
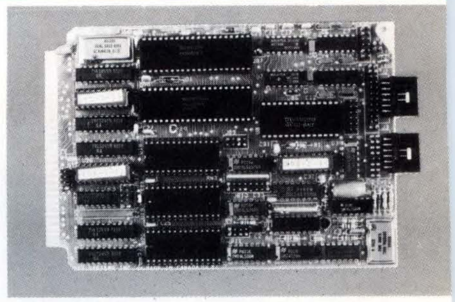
VERNITECH **251**



The 1816-R is a 5 volt 2048x8 bit electrically erasable programmable read only memory (E^2prom). Intended for use in applications that require or would benefit from non-volatile memory capable of in-system modification, WHERE EXTENSIVE WRITE CYCLES ARE NOT REQUIRED. Guaranteed for at least 100 write cycles with full 10 year data retention. Devices are tested, burned-in and guaranteed. Price is $5.95 ea. (1k quan.) Offered exclusively by **ROONEY & ASSOCIATES**, Alamo Corp. Ctr. 102 S. Tejon, Ste. 1100 Colorado Springs, Co. 80903 (303) 578 -3326.

NEW (SHORT CYCLE) E^2PROM **252**



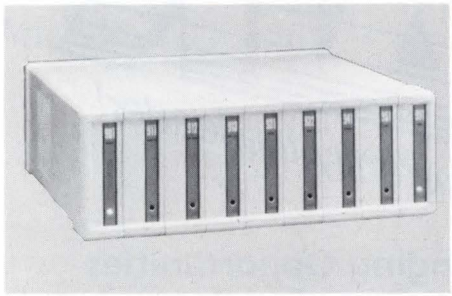
DSTD-102 is a complete STD Z80 BUS compatible single board microcomputer. This board contains byte-wide memory sockets for up to 24K Bytes of EPROM and RAM, two serial RS232C channels and fair counter/timer channels, 2.5 or 4.0 MHz operation, programmable waitstate generator and an on-board memory disable capability. dy-4 SYSTEMS, 888 Lady Ellen Pl., Ottawa, Ontario, Canada K1Z 5M1. 613-728-3711.

DSTD 102 **253**

Guaranteed FCC/VDE Compliance!

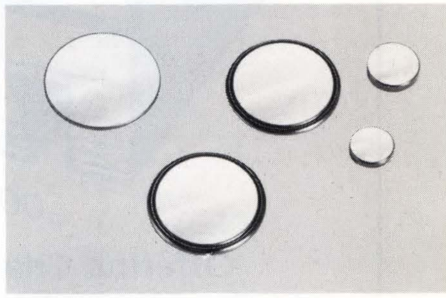
In case of failure, you need to know exactly how to bring your device into compliance. Our test sites are tested to be identical to the FCC's. We show you inexpensive, effective board level fixes to satisfy the regulation. We are also your complete one-stop U.S. test facility for VDE regulations. Total assistance on overseas submissions, too. Fixed price, agreed upon in advance. **Dash, Straus & Goodhue, Inc., 593 Massachusetts Avenue, Boxborough, MA 01719 (617) 263-2662.**

FCC/UDE COMPLIANCE **254**



PC-BASED DATA ACQUISITION PERFECTED The ACRO-900 Modular Data Acquisition and Control System works with any PC; requires no programming knowledge, but can also be programmed; provides true, on-board intelligence; offers speed, ease-of-use and modular design at an attractive price. From ACROSYSTEMS, 66 Cherry Hill Drive, Beverly, MA 01915. (617) 927-8885—Dave Bennett.

DATA ACQUISITION **255**

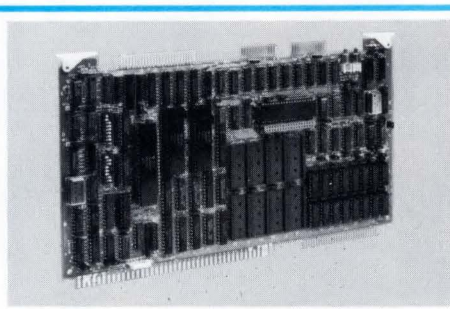


Seiko Instruments now offers three models of Lithium Batteries, CR2016, CR2025, and CR2032. Primarily designed for memory backup applications, these button type batteries feature: wider operating temperature range, higher energy density, superior leak resistance, stable operating voltage, and high reliability. For complete details and pricing information, contact Seiko Instruments U.S.A., Inc., 2990 W. Lomita Blvd., Torrance, CA 90505 (213) 530-8777.

LITHIUM BATTERIES **256**

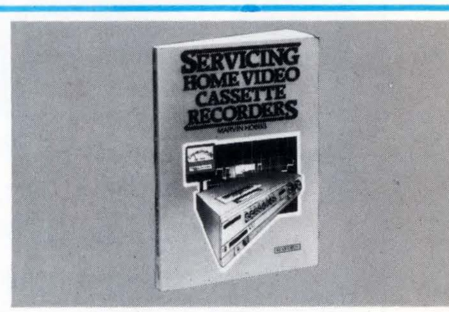
PSPM Seies, 25W Modular Switcher. *5V-5A, *12V-2A, *24V-1A meets int'l safety & EMI/RFI specs, including UL/CSA/VDE-0871/875. I/O isolation is 3750 VAC & creepage distance between I/O circuitry is 9 mm. Leakage current is less than 5 ua which meets medical standards. The units are short circuit protected, have soft start circuitry, & list at $156.00 each in 1-9. Ask for our complete modular AC/DC & DC/DC catalog. **Total Power International, Inc.** 418 Bridge St., Lowell, MA 01850: (617) 453-7272.

SWITCHING POWER SUPPLIES **257**



10 MHz Z8000™ PERFORMANCE In addition to 10 MHz, the NEW MBx8000 SBC features a single width SBX connector for adding standard expansion modules, such as the SBSxFDC Floppy Controller. MBx8000 maintains all the capabilities of its predecessor, the MB8000: Z8001/Z8002 CPU 4/6/10 MHz; 32K/128K/512K DRAM; up to 48K static RAM or EEPROM; up to 128K EPROM; 2 RS-232 ports; 40 parallel I/O lines; six 16-bit counter-timers; etc. Z8000™ Zilog. SINGLE BOARD SOLUTIONS, 7669 Rainbow Drive, Cupertino, CA 95014. (408) 253-0181.

SINGLE BOARD SOLUTIONS **258**



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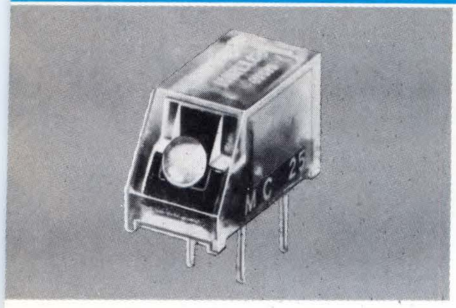
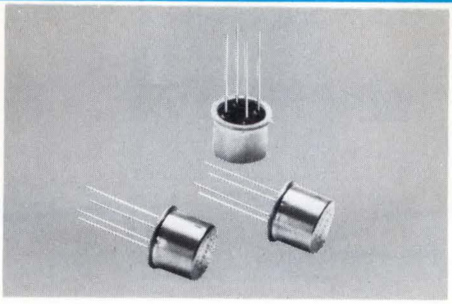
RECORDERS **259**



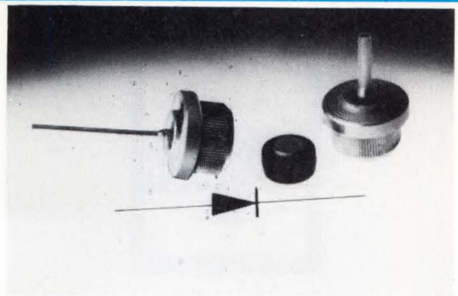
PC CIRCUIT LATCHING FAULT INDICATOR. Smallest new magnetic-latching MC 25 indicator mounts on pc boards to indicate circuit status. When pulsed, internal drum rotates to display color, retains position until reset. Ultra-small, lightweight, enclosed in clear dustproof Lexan case, with 4 solder pins for individual or gang pc mounting. Op. temp range 0°C to 71°C. Bulletin, Prototypes. Minelco, Inc., Division of Talley Industries, 135 South Main St., Thomaston, CT 06787-0459. Phone 203-283-8261. TWX 710-475-1091.

FAULT INDICATOR **260**



MIL SOLID STATE AC/DC RELAY Teledyne's M640-1W features AC/DC switching up to 40V, & low on resistance (2 ohms typ), Transformer coupling provides 1000VAC isolation & low off-state leakage. Hybrid microcircuit assembly to MIL-883B in TO-5 case. MIL P/N M28750/5-001 on QPL. The M640-1W is used as data coupler, isolated line driver, current loop switch, analog & transducer signal switching. $38 ea for 500 pcs. Teledyne Solid State Products, 12525 Daphne Ave., Hawthorne, Ca, 90250 (213) 777-0077.

RELAYS **261**



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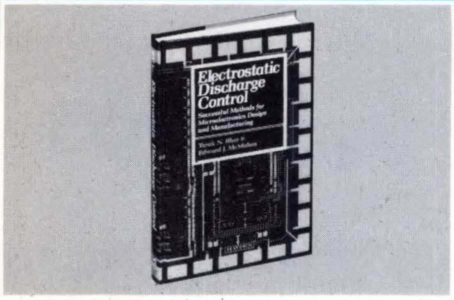
RENARD'S SILICON DIODES **262**



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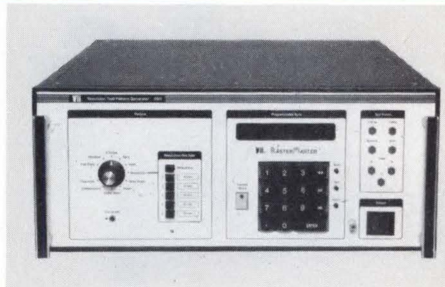
SINGLE BOARD COMPUTER **264**



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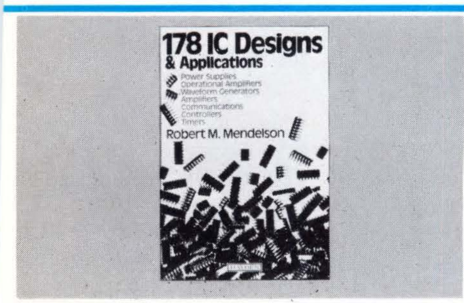
PROGRAMMABLE VIDEO GENERATOR **265**



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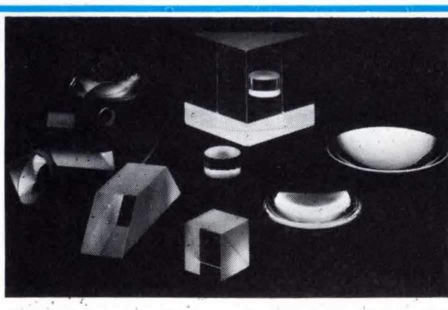

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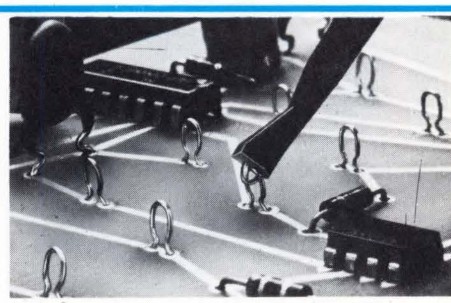
OPTICS **267**



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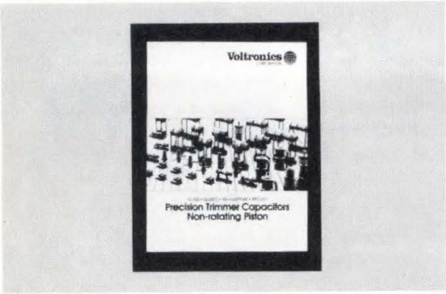
COMPONENTS CORPORATION **268**



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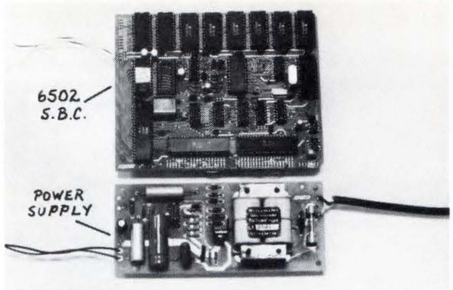
CATALOG **269**



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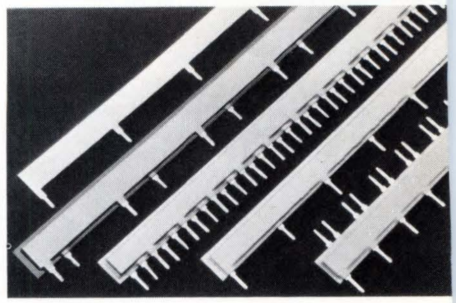
CUSTOM PROGRAMMING GRP., INC. **270**



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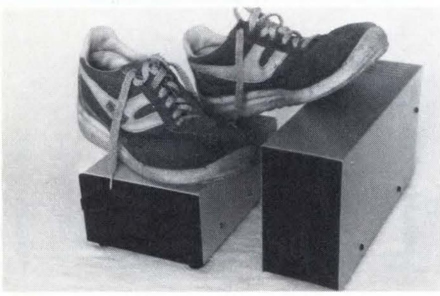

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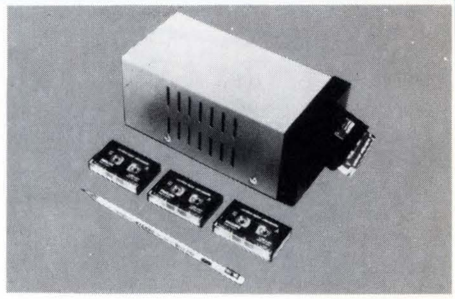
SWITCH BOXES **273**



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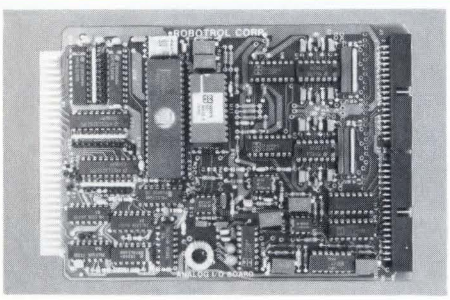
MINI CASSETTE SYSTEM **274**



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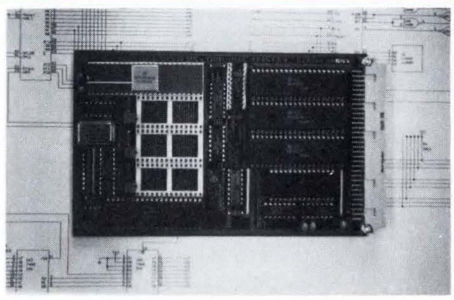

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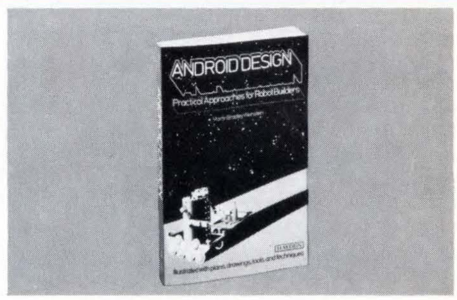

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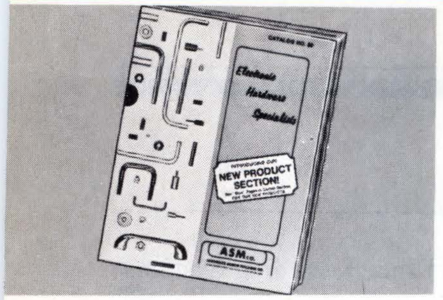

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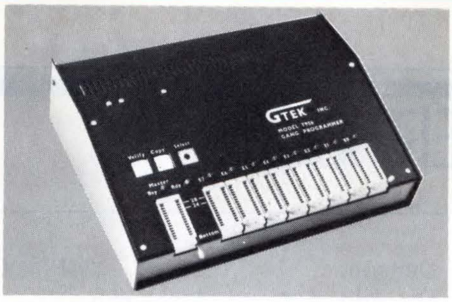

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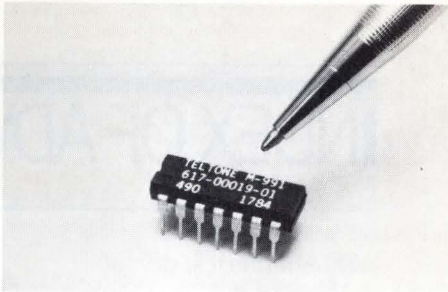

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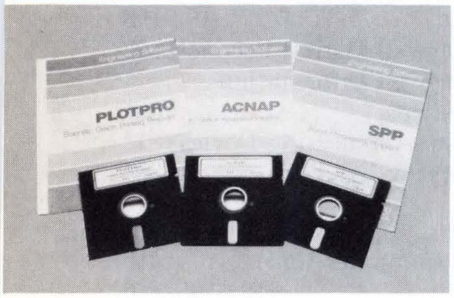
M-991 **280**



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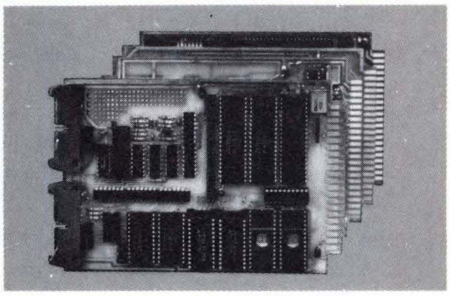

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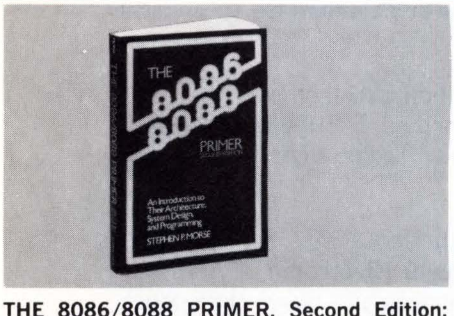
SINGLE BOARD COMPUTER **283**



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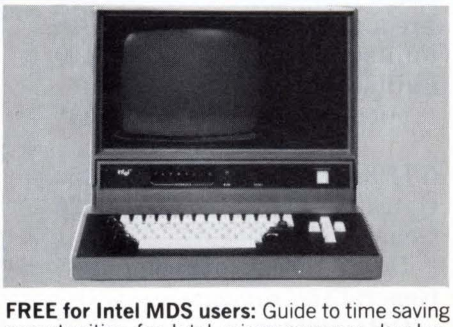

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2	●			
3	●	●■	●	●
4	●			
5	●			
6	●	●■	●	●
7	●			
8	●			
9	●			
10	●	●■	●	●
12	●			
15	●			
20	●	●■	●	●
30	●	●	●	●
40	●	●	●	●

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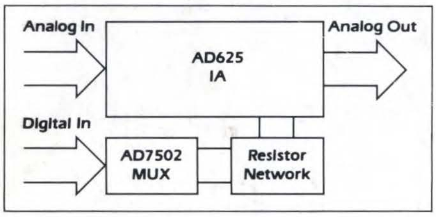

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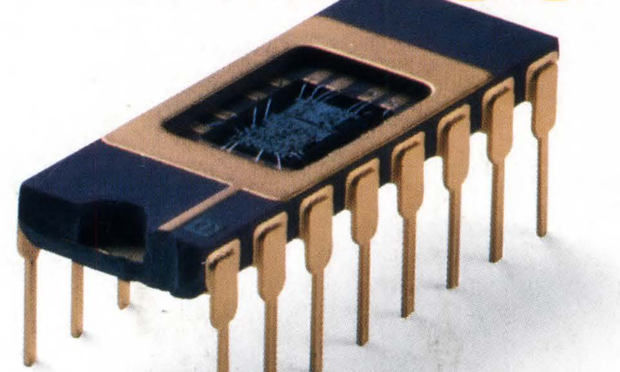

The new AD625 In-Amp: Come up with a problem it can't solve.

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