

**WHY MIXED-SIGNAL DESIGNERS PREFER ASICs
STANDARD-CELL X86 FAMILY EASES DESIGNS**

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

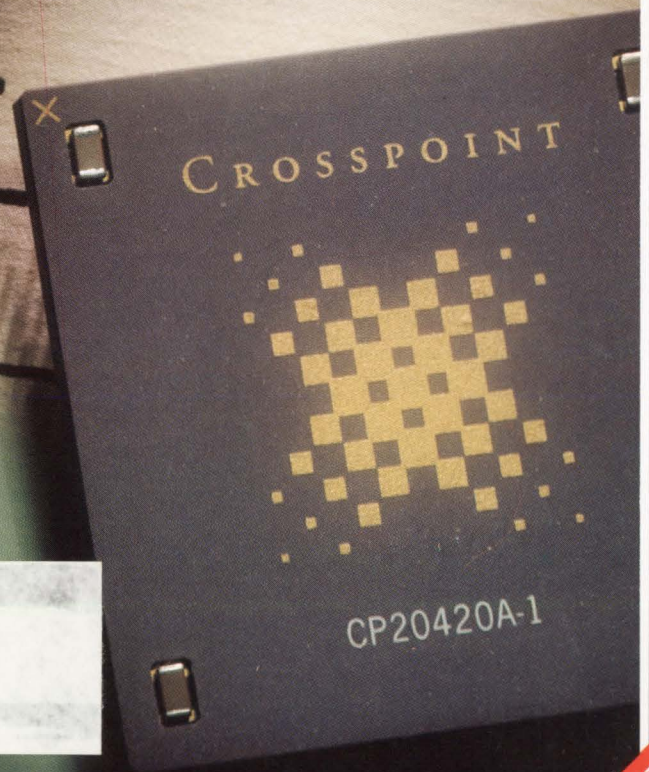
ELECTRONIC DESIGN

A PENTON PUBLICATION

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NOVEMBER 21, 1991

**REDEFINING
THE GATE
IN FPGAs**



• A PREVIEW OF WESCON

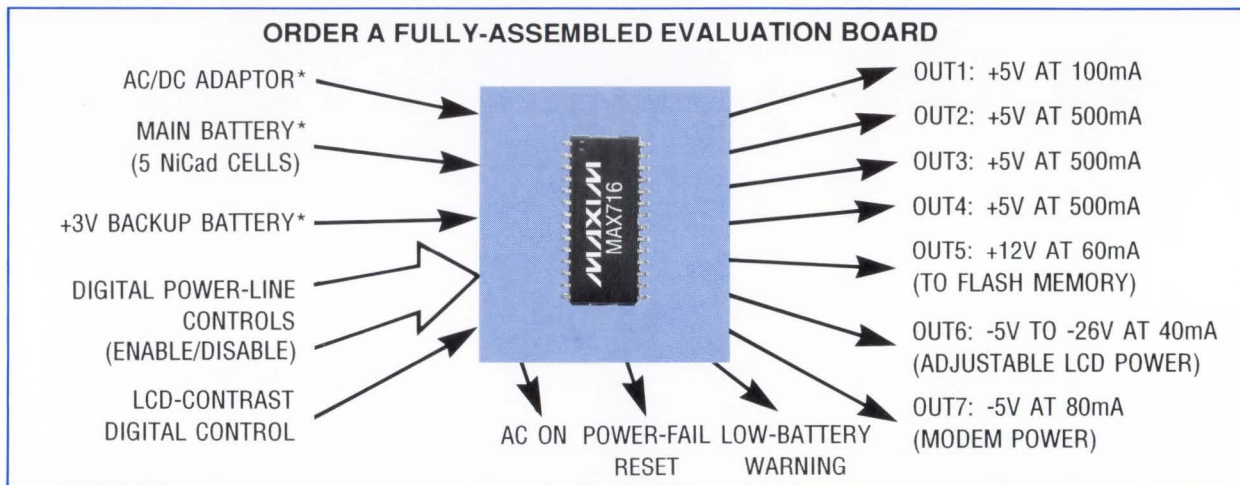
• PIPS: POWER, INTERCONNECTS, PASSIVES, SWITCHES/RELAYS

QUICKLOOK

WORLD'S SMALLEST POWER SUPPLY FOR PORTABLES

Load & Power Management System Has 7 Supplies In One IC!

Maxim's new MAX714-MAX716 combine up to four +5V low dropout linear regulators, three DC-DC switching regulators and power-supervisory functions—all in one IC! Save power and extend battery life by shutting down inactive subsystems in your portable equipment. Each of the 7 voltage outputs from MAX716 can be independently turned on and off digitally. Efficiency remains at a high 83% with both light and heavy loads. And, they interface with portable computer chip sets from Intel (386SL), VLSI (Scamp Power Management Unit), and Chips & Technologies (82C63).



A complete MAX716 Evaluation Board contains an entire supply for portable load and power management.

- ◆ **83% Typical Efficiency**
- ◆ **35 μ A Standby Current**
- ◆ **Backup Battery Switchover**
- ◆ **Low Voltage Warning**
- ◆ **Digital LCD Contrast**
- ◆ **Space-Saving DIP and SO Packages**

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	MAX714	MAX715	MAX716
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+12V Flash Memory Output	—	✓	✓
Inverting Switching Reg. -5V	—	✓	✓
-5V to -26V Adjustable LCD Output	✓	✓	✓
Pin Count	14	24	28

POWER SUPPLIES ANALOG

+5V To \pm 15V DC-DC Converter Delivers 30W

The MAX716 MAX714 DC-DC converter provides the highest power available for generating +5V and \pm 15V outputs. The MAX716 MAX714 DC-DC converter provides the highest power available for generating +5V and \pm 15V outputs. The MAX716 MAX714 DC-DC converter provides the highest power available for generating +5V and \pm 15V outputs.

Evaluation Kit Simplifies Prototyping

Maxim's new MAX716 MAX714 DC-DC converter provides the highest power available for generating +5V and \pm 15V outputs. The MAX716 MAX714 DC-DC converter provides the highest power available for generating +5V and \pm 15V outputs.

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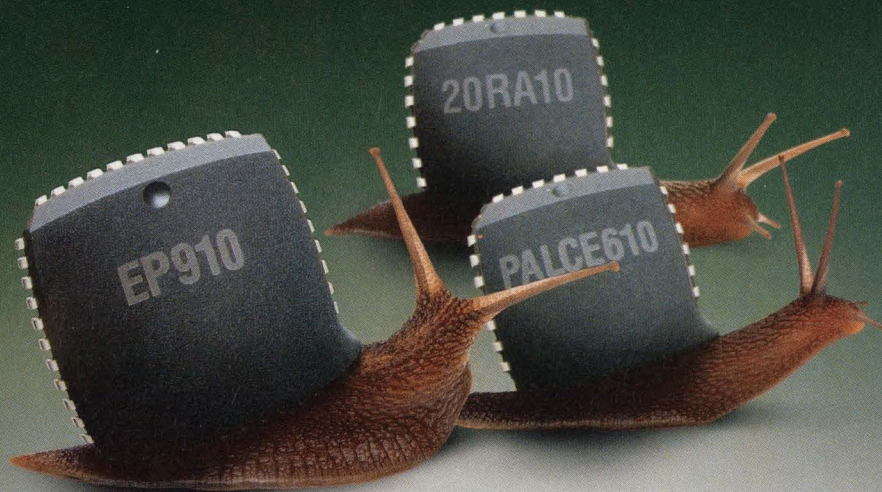
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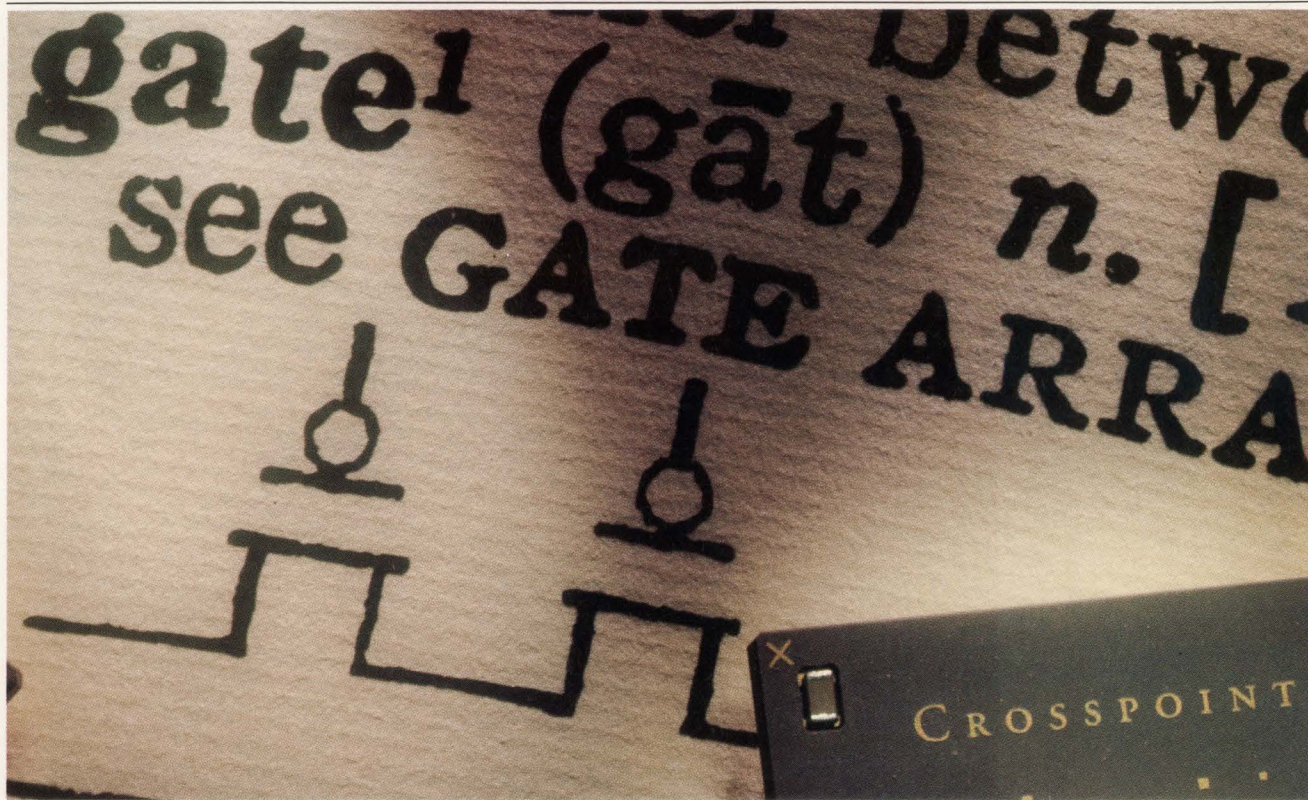


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1967 First Place Award
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- A new super-intelligent digital multimeter
- New design tools for FPGAs
- Getting F-V converters to settle fast—without ripple
- Developing tests that meet new communications standards
- The emerging applications for piezoelectric-film sensors
- PLUS:
Ideas for Design
Pease Porridge
Technology Advances
QuickLook

Oops, a typo. In our October 24 issue, on p. 24, we called out the part number for the single-chip AT controller from ACC Microelectronics as the ACC2146. It should have been the ACC2046, as indicated correctly further down in the story.

Also, on our cover in the same issue, the SPT7912 was inadvertently transposed to read as SPT9712. The story inside correctly called it out as SPT7912. *ED*

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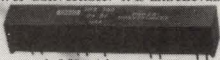
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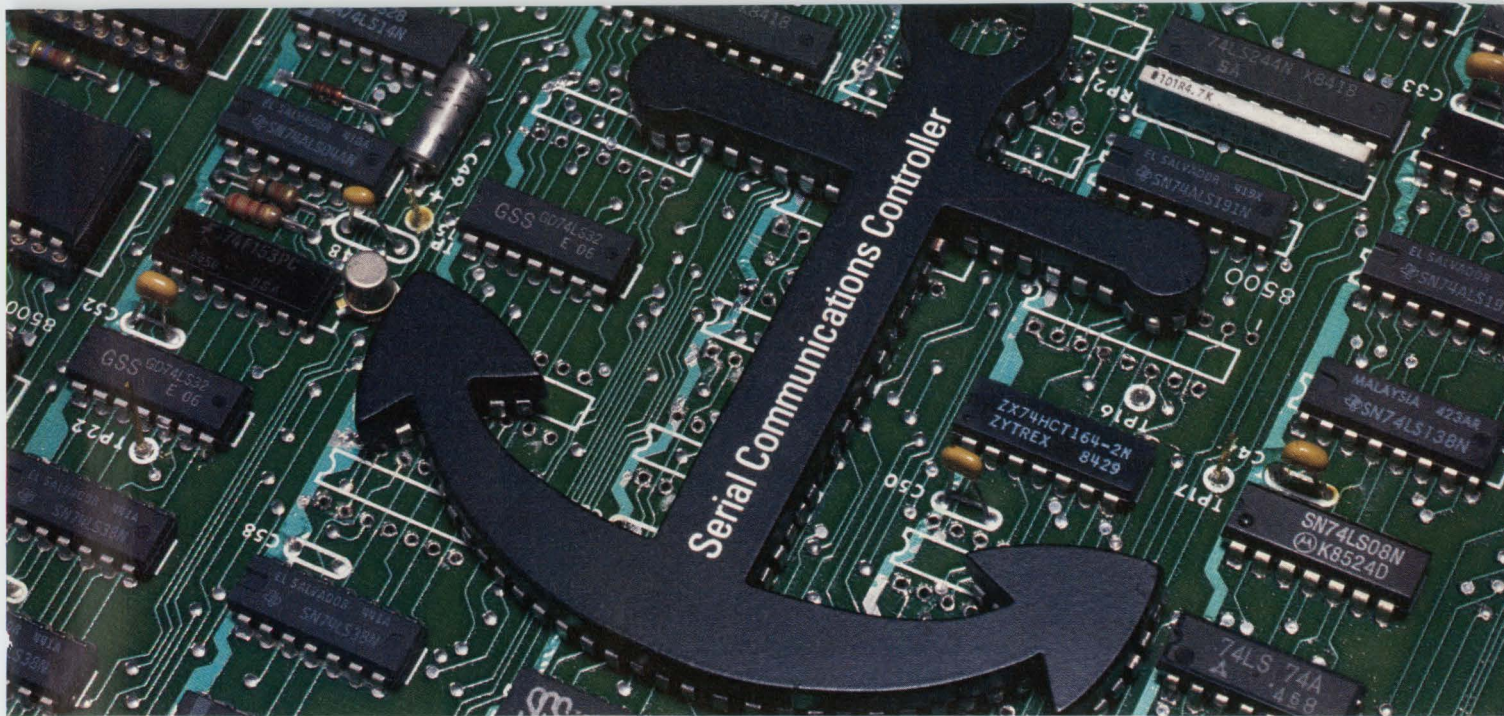
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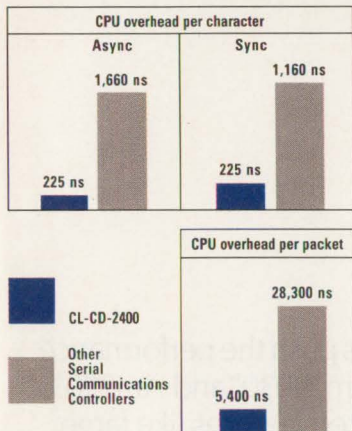
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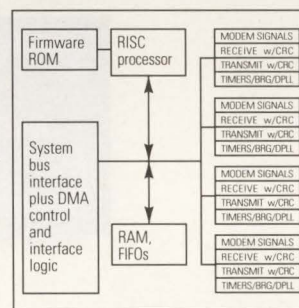
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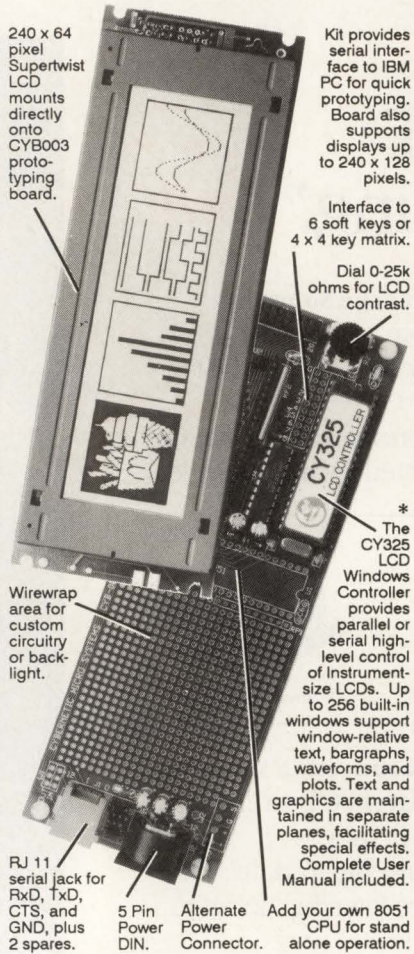
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EDITORIAL

WHAT'S ALL THIS PEASE STUFF, ANYHOW? FIND OUT AT WESCON THIS WEEK

For more than a year now, we've been publishing "Pease Porridge," a column probably best described as commentary on the art of being an engineer, both in terms of design philosophy and career, written by Bob Pease, Staff Scientist, National Semiconductor. In our editorial announcing the column (*Sept. 13, 1990, p. 14*), we said that Bob would have lots of freedom to express his opinions, and noted that "sometimes they'll be outlandish and even humorous, but they'll always be insightful and thought-provoking." Since then, our research has shown that it is consistently one of the best read sections in *Electronic Design*. It's also the source of a great deal of reader interactivity with the magazine. We and Bob thank all of you who have taken the time to write letters in response to his column. In the future, we'll publish more of these letters, which frequently shed further light on Bob's main points.

Within Bob's busy schedule that involves the job of designing linear ICs at National Semi, he turns out a column every two weeks. That's not an easy task. I recall reading about one newspaper columnist, who, when asked how he managed to turn out a column every day, explained: "It's not so difficult. You just sit in front of the typewriter every day and sweat blood." But Bob says many columns are still left in him, just waiting to be entered into the computer.

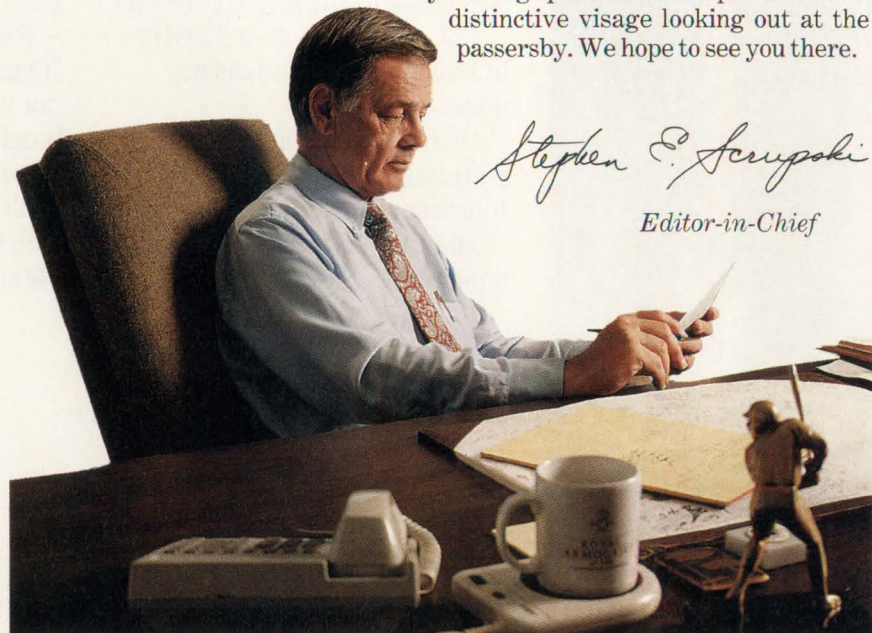
In this issue's "Pease Porridge," Bob strikes a responsive chord in all of us with any amount of experience in this industry. He discusses the feelings surrounding the subject of losing touch with former classmates and co-workers, pondering their whereabouts and how they're doing. In fact, Bob describes an innovative way to contact with out-of-touch former comrades.

We're happy to announce that those of you attending Wescon in San Francisco this week will have a chance to meet and talk with Bob, at *Electronic Design's* booth, number 3510. Bob has graciously consented to interrupt his busy work agenda, and will spend 10 hours of booth time over the three-day period to meet all comers.

Here's the schedule for Bob's meetings at our Wescon booth: Tuesday, Nov. 19: 11:00 A.M. to 1:00 P.M. and 2:00 to 4:00 P.M.; Wednesday, Nov. 20: 10:00 A.M. to 12:00 P.M. and 2:00 to 4:00 P.M.; Thursday, Nov. 21: 10:00 A.M. to 12:00 P.M. If you're at Wescon, and have the time, please stop by. You'll recognize the spot by the large poster with the photo of Bob's distinctive visage looking out at the passersby. We hope to see you there.

Stephen E. Scrupski

Editor-in-Chief



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LRMS-2D	5-1000	DC-1000	+7	6.8	40	7.25
LRMS-2U	10-1000	10-1000	+7	6.5	46	11.45
LRMS-5	5-1500	DC-1000	+7	6.0	41	13.95
LRMS-11A	1400-1900	40-500	+7	7.0	25	16.95
LRMS-1LH	2.0-500	DC-500	+10	5.8	47	7.95
LRMS-2LH	5-1000	DC-1000	+10	6.6	40	8.95
LRMS-5LH	10-1500	DC-900	+10	5.4	38	14.95
LRMS-1MH	2.0-500	DC-500	+13	5.7	44	8.95
LRMS-2MH	5-1000	DC-1000	+13	6.6	44	9.95
LRMS-5MH	10-1500	DC-900	+13	5.8	46	15.95
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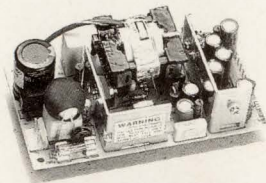
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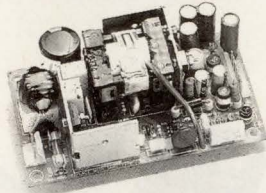
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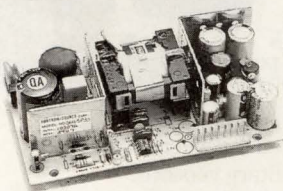
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TECHNOLOGY BRIEFING

MEMORY DRIVES ANALOG IC TECHNOLOGY

It may be difficult for die-hard analog designers to accept, but analog and mixed-signal ICs owe a lot to memory technology, both IC memory and mass storage. Digital memory is becoming a major technology driver for future high-performance analog ICs, while smaller, higher capacity disk drives are placing more stringent demands on their analog signal processing and control circuits for better performance.

For years, DRAMs have been acknowledged as the process-technology driver for digital ICs. But there has been significant fallout from DRAM technology for analog, mixed-signal, and even power ICs. Certainly, the fine-line lithography developed for DRAMs now make possible bipolar-transistor f_t s undreamed of a few years ago. Moreover, without the anisotropic-etch trenching technology borrowed from DRAMs, future high-volume production of the next generation of fast wide-band *precision-linear* analog ICs would be severely limited. To maximize the f_t s and the "precision" of the vertical npn and pnp transistors needed for these ICs (they are built on a complementary bipolar processes), an advanced silicon-on-insulator (SOI) technology like SIMOX, ZMR, and wafer bonding is needed.

Conventional dielectric isolation (DI), as now used by Harris, AT&T, Elantec, and Sipex, won't cut it. Not only is it limited to four-inch wafers, but packing density is low and wafers are IC specific. On an SOI wafer, a layer of oxide (or other insulating material) separates a thin layer of working silicon from a standard-thickness wafer, providing structural support. Reactive-ion-etching (RIE), the technology adapted from DRAMs, then creates narrow trenches between the wafer's working-silicon surface and the insulating material on which it lies. The trenches divide the wafer into isolated islands of silicon. Oxide is grown on the side walls of the trench, and the remaining space between the oxide walls are filled with polysilicon to produce a planar surface.

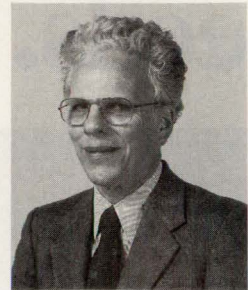
One of the major types of products to come off these processes will be read/write channel ICs for high-end disk drives. These ICs will range from the preamplifiers at the head to the complete read channel, including the main amplifier, programmable filters, AGC, and clock-recovery circuits.

The "power" ICs in disk drives can also take advantage of SOI processes. While not needing gigahertz bandwidths, the head-positioning servo needs low-noise, high-gain circuits on the input, plus low crossover distortion in the output drive circuitry. The processes create very small transistors with good dc specifications at low collector current, and thus lend themselves to the input circuits. Larger matched complementary transistors handle the drive circuits.

Though complementary devices aren't mandatory for controlling and driving the spindle motor, their availability almost always simplifies a design. And the fast, small npns should minimize both size and losses in this PWM circuitry. In addition, the isolation provided by the dielectric isolation between devices and circuit blocks on the IC should help control the noise in this potentially noisy circuit.

What kinds of broad-based generic analog ICs will these upcoming technologies pick up in their path? For starters, there's the next generation of fast op amps, comparators, and buffers, which will sport useful bandwidths to hundreds of megahertz. Add to that video amplifiers for HDTV and a wide range of "low-frequency" (up to 1 GHz) RF applications, such as analog and digital cordless telephones and wireless LANs.

Still, SOI-based processes will face continual challenges from device developers trying to tune up potentially lower-cost processes. There still is room for improvements in junction-isolated complementary-bipolar processes, junction-isolated all-npn processes, analog biCMOS processes, and even pure CMOS processes. Whatever the case, developers of such processes will keep one eye on what's happening over on the DRAM side of the house.



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	San Fernando	Feb 27	IL	Arlington Hts.	Nov 7	NY	Buffalo	Nov 18	VA	Falls Church	Jan 17
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	San Gabriel	Sep 18	IN	Fort Wayne	Feb 4		Rochester	Nov 19		Seattle	Mar 5
	San Jose	Sep 12	MA	Andover	Oct 24		Syracuse	Nov 20	WI	Madison	Nov 6
	San Jose	Mar 3		Boxborough	Oct 23	OH	Cleveland	Feb 6		Milwaukee	Nov 5
	Santa Barbara	Sep 13		Newton	Oct 23		Columbus	Feb 5			
	Orange County	Sep 20	MD	Baltimore	Jan 16	ONT	Ottawa	Sep 27			Sept, Oct, Nov dates are 1991
	Orange County	Feb 25					Toronto	Sep 26			Jan, Feb, Mar dates are 1992

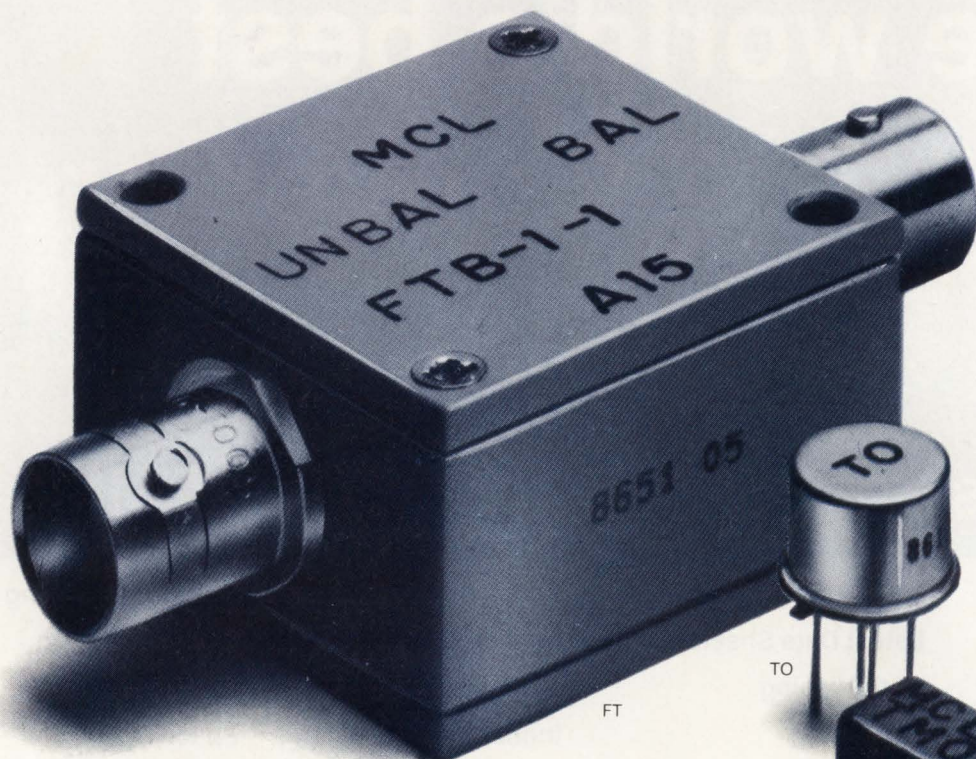
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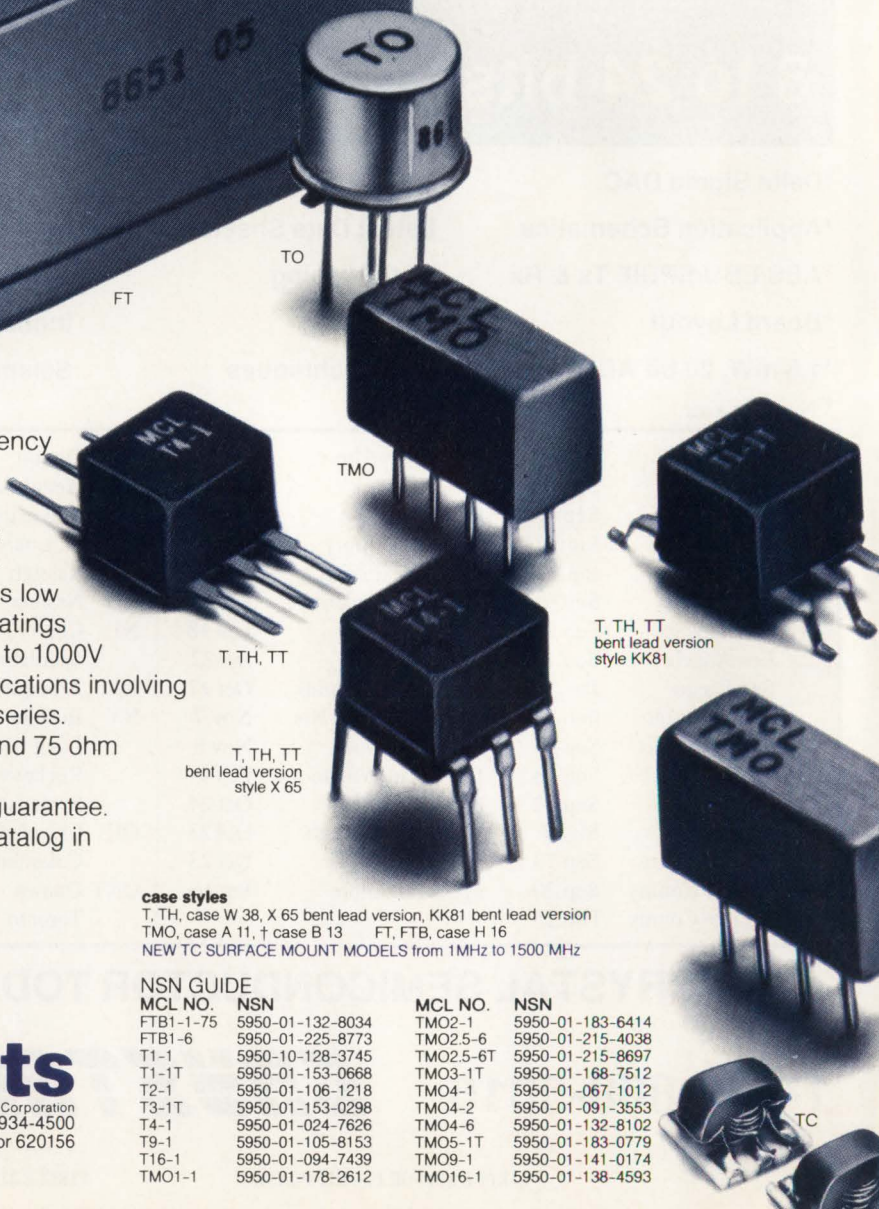


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T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

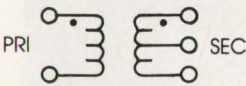
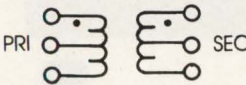
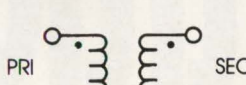
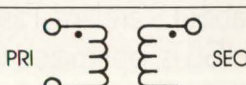
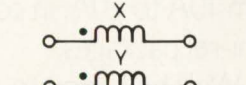
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		T2-1T	2	.07-200	.07-200	.1-100	5-50	4.95		
		T2.5-6T	2.5	.01-100	.01-100	.02-50	50-20	4.95		
		T3-1T	3	.05-250	.05-200	.1-200	5-70	4.95		
		T4-1	4	2-350	2-350	.35-300	2-100	3.25		
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45		
		T5-1T	5	3-300	3-300	6-200	5-100	4.95		
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95		
		T13-1T	13	3-120	3-120	7-80	5-20	4.95		
		T16-6T	16	.03-75	.03-75	.06-30	1-20	5.65		
		T4-1H	4	10-350	10-350	15-300	25-200	5.95		
		TMO1-1T	1	.05-200	.05-200	.08-150	2-80	7.95		
		TMO2-1T	2	.07-200	.07-200	1-100	5-50	8.45		
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45		
		†TMO3-1T	3	.05-250	.05-250	1-200	5-70	7.95		
TMO4-1	4	2-350	2-350	.35-300	2-100	6.25				
TMO5-1T	5	3-300	3-300	6-200	5-100	8.45				
TMO13-1T	13	3-120	3-120	7-80	5-20	8.45				
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	1-50	6.95		
		TT1.5-1	1.5	.075-500	.075-500	2-100	1-50	5.95		
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		TT4-1	3	.05-200	2-50	2-50	1-30	5.95		
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95		
		TT25-1	25	.02-30	.02-30	.05-20	1-10	9.95		
		TTMO25-1	25	.02-30	.02-30	.05-20	1-10	11.95		
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45		
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95		
		C	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
T1.18-3	1.18			0.01-250	0.01-250	0.02-200	0.03-50	5.65		
T1-6	1			.01-150	.01-150	.02-100	.05-50	5.65		
T1.5-1	1.5			.1-300	.1-300	.2-150	5-80	4.45		
T1.5-6	1.5			.02-100	.02-100	.05-50	0.1-25	5.65		
T2.5-6	2.5			.01-100	.01-100	.02-50	.05-20	4.45		
T4-6	4			.02-200	.02-200	.05-150	1-100	4.45		
T9-1	9			.15-200	.15-200	.3-150	2-40	3.95		
T16-1	16			3-120	3-120	7-80	5-20	4.45		
T36-1	36			.03-20	.03-20	.05-10	1-5	6.95		
C	TO	TO-75	1	10-500	—	10-500	40-250	6.95		
		T1-1H	1	8-300	8-300	10-200	25-100	5.95		
		T9-1H	9	2-90	2-90	3-75	6-50	6.45		
		T16-H	16	7-85	7-85	10-65	15-40	6.45		
		C	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
				TMO1-1	1	15-400	15-400	35-200	2-50	6.25
				TMO1.5-1	1.5	.1-300	.1-300	2-150	5-8	8.45
				†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
				†TMO4-6	4	.02-200	.02-200	.05-150	1-100	7.95
				TMO6-1	6	3-200	3-200	5-150	5-50	7.95
TMO9-1	9			.15-200	.15-200	.3-150	2-40	7.95		
TMO16-1	16			3-120	3-120	7-80	5-20	7.95		
D 	T			T2-1	2	.050-600	.050-600	.1-400	5-200	3.95
				T3-1	3	5-800	5-800	2-400	2-200	4.45
		T4-2	4	2-600	2-600	5-500	2-250	3.95		
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95		
		T14-1	14	2-150	2-150	5-100	2-50	4.95		
		D	TMO	TMO2-1	2	.050-600	.050-600	.1-400	5-200	7.95
				TMO3-1	3	5-800	5-800	2-400	—	8.45
				TMO4-2	4	2-600	2-600	5-500	2-250	7.95
				TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
				TMO14-1	14	2-150	2-150	5-100	2-50	8.45
D	FT			FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
				FT1.5-1	1.5	1-400	1-400	5-200	1-100	35.95
E 	FTB			FTB-1	1	2-500	2-500	5-300	1-100	36.95
				FTB1-6	1	.01-125	.01-125	.05-50	1-25	36.95
				■FTB1-75	1	5-500	5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25		
		T626	1	0.01-10	0.01-10	0.2-5	0.4-2	3.95		

■ Denotes 75 ohm models

* FOR A AND B CONFIGURATIONS

Maximum Amplitude Unbalance

0.1 dB over 1 dB frequency range

0.5 dB over entire frequency range

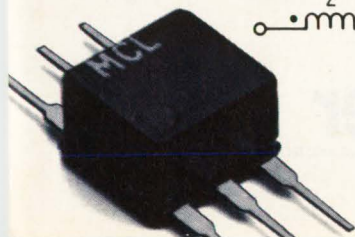
Maximum Phase Unbalance

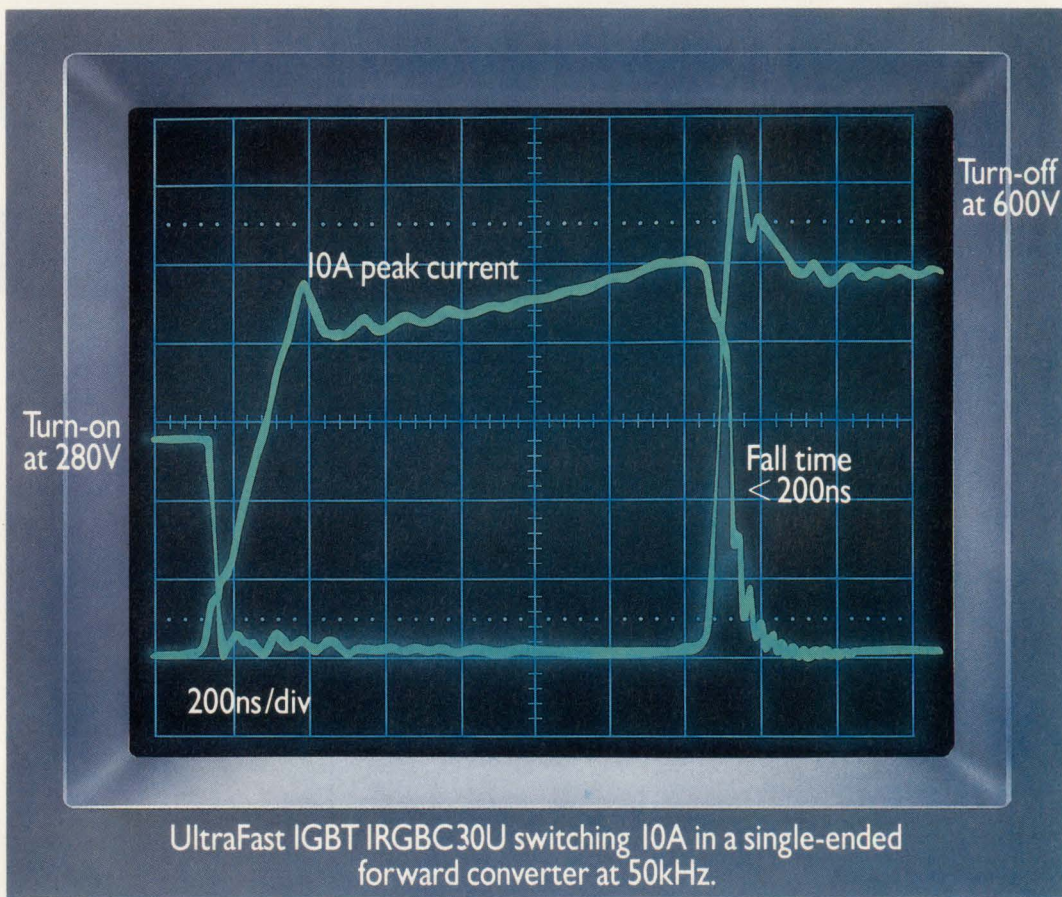
1.0° over 1 dB frequency range

5.0° over entire frequency range

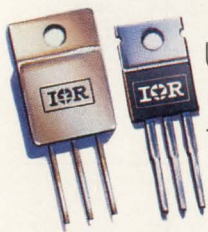
CIRCLE 200 FOR U.S. RESPONSE

CIRCLE 201 FOR RESPONSE OUTSIDE THE U.S.





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CIRCLE 178 FOR U.S. RESPONSE

CIRCLE 179 FOR RESPONSE OUTSIDE THE U.S.

OPTICAL INTERCONNECTS TARGET PARALLEL CPUS

A fiber-optic mesh extender (FOME), supporting multigigabit data-transfer rates, will allow the interconnection of multiple supercomputer systems to form a single large mesh. FOME will be jointly developed by Honeywell Corp., Minneapolis, Minn., and the Supercomputer Systems Div. of Intel Corp., Beaverton, Ore., under a recently awarded government contract that's part of the Photonic Interconnect Insertions into Strategic Computing project (referred to as Prism). The goal of the project is to enhance scalability and demonstrate a practical concept for implementing a software-compatible, tera-operation-per-second computer. The FOME architecture will minimize latency and provide usable bandwidth across multiple Gbit/s fibers to achieve high aggregate bandwidths. Photonic interconnects provide a larger bandwidth and longer interconnection length than copper or coaxial cables and are immune to electromagnetic radiation. They also have no ground loop or crosstalk problems and implicitly have a higher reliability, since they can typically reduce the connection complexity by about 16:1. *DB*

EUROPEAN ASIC VENDORS INK SECOND-SOURCE PACT

Five leading European ASIC vendors and three of their major customers will adopt a common ASIC library implemented in the vendors' 0.7- μ m CMOS processes. Under the terms of the agreement, GEC Plessey Semiconductors of the United Kingdom, France's European Silicon Structures, Germany's Siemens Semiconductor Group, Philips Semiconductors of the Netherlands, and the Italian-French SGS-Thomson Microelectronics will all include the library as part of their overall ASIC library offering. As a result, users can design ASICs and have them produced in any of the five vendors' silicon foundries. Developed in collaboration with ASIC users Robert Bosch GmbH of Germany, France's computer maker Bull, and International Computers Ltd. of the U.K., the new "Integrated Design and Production System" (IDPS), includes the ASIC library and its associated design methodology, and promises to become an industry standard for ASIC design. The participants believe that IDPS will put the European ASIC industry in a better competitive position by allowing multiple European sourcing of ASICs in up-to-date processes, quick turnaround, and prototypes that work right the first time, as well as fast ramp-up to volume production. The library currently contains a wide range of digital standard cells and I/O cells, a macro library, and a family of module generators, and will be complemented by an analog cell library for use on the same 0.7- μ m CMOS processes. The agreement allows for continued cooperation in library development, including migration to 0.5- μ m CMOS processes. *JG*

BRIGHT LEDs LIGHT UP T-BIRD TRADEMARK

A joint development by Hewlett-Packard Co. and Ford Motor Co. has resulted in a special lighting package that provides full-width LED lighting across the back of the 1992 Ford Thunderbird automobile. Because the new design required lighting across the top of the trunk, the shock and vibration environment ruled out the use of incandescent bulbs. High resistance to shock and vibration also qualifies the LEDs for automotive lighting systems with complex shapes, such as wraparound tail lamps. The LEDs are made by H-P's TS-AlGaAs (transparent-substrate aluminum-gallium-arsenide) process, which produces LEDs that are 100 times brighter than conventional devices. In addition to automotive applications, high-intensity LEDs can also be used for highway signs, exterior moving-message signs, airport runway illumination, and emergency signaling devices. *ML*

MORE R4000 PARTNERS UNVEIL CPU PLANS

Toshiba America Electronic Components Inc., Irvine, Calif., has added its name to the list of companies licensed to manufacture or create custom versions of the R3000 and R4000 RISC processors from MIPS Computer Systems, Sunnyvale, Calif. Toshiba plans not only to offer the CPUs, but also to create its own offshoots, as well as chipsets to reduce the number of peripheral components needed for CPU support. Not known for its CPU activity, Toshiba has been a licensee of Motorola's 68020 CISC processor, which it sells in Japan either to its own divisions or to other customers. The addition of the R3000 and R4000 will give Toshiba some high-end CPUs that it can employ in either embedded or general-purpose applications.

As part of the R4000 unveiling by MIPS in late September, Integrated Device Technology Inc. and Siemens Corp., both in Santa Clara, Calif., released details of their CPU support plans—both will manufacture all three pinout options of the R4000. The IDT 79R4000PC and the Siemens SAB-R4000PC are the 179-pin version that contains the primary cache, but cannot be expanded to handle a secondary cache. Both of the other versions, the 4000SC and 4000MC, come in 447-pin, pin-grid array packages and include secondary-cache support. IDT also plans to offer these two chips in 500-contact, dual leadless chip-carrier packages. Both an R4000

Schematic Design Tools

Programmable Logic Design Tools

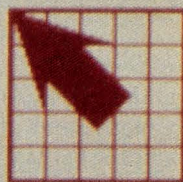
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PC Board Layout Tools

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Schematic

Editors

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Configure Schematic Design Tools

Category: Electrical Rules Matrix

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o t s z r

Input Pin

Input/Output Pin

Output Pin

Open Collector Pin

Passive Pin



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News



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demo



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Create Netlist

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evaluation board and a secondary-cache module are also available from IDT. The MC version also has control signals that support either snooping or directory-based cache coherence schemes, simplifying its use in multiprocessor applications. Initial sample prices in lots of 1000 for the Siemens chips are \$1050 and \$1250 for the PC and SC versions, respectively. Contact Toshiba at (714) 455-2000, Bob Rowe at IDT at (408) 492-8631, and Siemens at (408) 980-4546. *DB*

BENCHMARK GAGES FILE-SERVER PERFORMANCE

The LADDIS Group, an organization of leading network file system (NFS) vendors, has introduced the first vendor-neutral NFS benchmark program for measuring file-server performance and capacity in heterogeneous networks. The benchmark has been submitted to the Systems Performance Evaluation Cooperative (SPEC), Fairfax, Va., a nonprofit organization that develops, maintains, and endorses benchmarking tools for all aspects of computer-systems performance. SPEC is expected to include the program in its benchmark suite next year. An improved version of the nfsstone benchmark introduced by Legato Systems two years ago, the LADDIS benchmark will provide NFS customers with a standard measure they can use for load planning, system configuration, and equipment comparison. Written in C, the software runs on platforms from Data General, Digital Equipment, and Sun Microsystems. The program generates precise traffic directed at target NFS servers; the results are presented in a graph that depicts NFS operation, throughput, and response time. The LADDIS Group consists of representatives from Legato Systems, Auspex Systems, Data General, DEC, Interphase, and Sun. *ML*

POSITIONING SYSTEM CUTS SERVOWRITER COST

A closed-loop servo positioning system that delivers 0.4-microradian resolution promises to simplify and reduce the cost of writing disk-drive servo tracks. Based on a distance-measuring interferometer that can position the tracks for densities of up to 10,000 tracks/in., the CMX 3030 accepts digital position move commands from a host and converts the commands into an angular displacement of a mechanical output shaft. Unlike previous servowriter subsystems, the self-contained positioning system from CMX Systems Inc., Meriden, Conn., reduces the complexity of the rest of the system, requiring only a track writer and clock electronics. Since cost is lowered by a factor of five or more to just \$15,000 for the positioning system, and hardware design of the servowriter is simplified, more units can be installed by drive manufacturers. Internal software in the CMS 3030 relates the input commands and interferometer count (with less than 1- μ m resolution) to the required track-to-track movement. Contact Richard Moore at (203) 238-2622. *DB*

COMDEX SHOWS OFF GRAPHIC ACCELERATORS

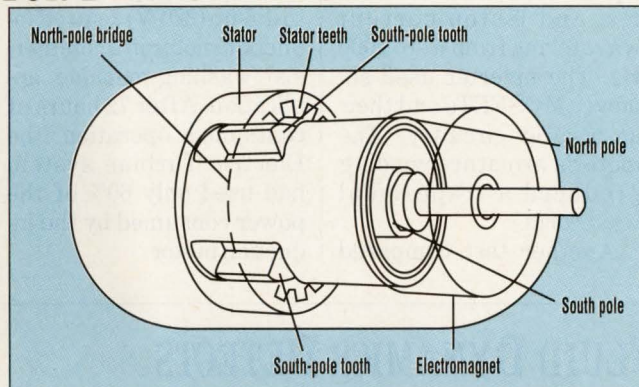
Techniques that accelerate windows software by factors of two to ten appeared in many forms at last month's Comdex in Las Vegas. Choices ranged from window accelerator cards based on chips such as those released earlier this year by S3 Corp., Santa Clara, Calif., and Weitek Corp., Sunnyvale, Calif., to the TMS 34010 and 020 programmable graphics processors from Texas Instruments Inc., Dallas. Other solutions included the use of a local-bus interface (instead of the typical AT-bus add-in card). These techniques are aimed at speeding up the process of repainting a complex image on a screen or moving an image from one place to another.

Cards unveiled at Comdex included the Flickerfree Windows/VGA 8800 card from Genoa Systems Corp., San Jose, Calif. The card employs the S3 chip (the 86C911) and provides a 70-Hz refresh and an average 5-times improvement in Windows software speed. Also using the S3 chip, Glad Systems Inc., Milpitas, Calif., and Advanced Integration Research Inc., San Jose, Calif., released their Flashview SuperVGA card, and AVIEW2E 32-bit EISA-bus card, respectively. Both cards claim a 4-to-5-times speed advantage over the ET4000 VGA controller from Tseng Laboratories, Newtown, Pa., the acknowledged top-performing VGA controller. Both also claim a 40% speed improvement over the IBM Corp. extended graphics adapter (XGA). Many others, including Cardinal Technologies Inc., Lancaster, Pa.; Diamond Computer Systems Inc., Sunnyvale, Calif.; Mylex Corp., Fremont, Calif.; Portacom Technologies Inc., San Jose; and STB Systems Inc, Richardson, Texas, also released S3-based cards.

In another approach to Windows, Mylex employs a TMS 34020 graphics processor for an EISA-bus graphics card that delivers screen resolutions of 1600 by 1200 pixels. The card runs Windows 3 as well as the SCO Open Desktop interface. Employing its own accelerator chip (the W5086), Weitek released its Power-for-Windows card, which improves application speed by a factor of two for 640-by-480-pixel resolution, and by a factor of four when the resolution increases to 768 by 1024. *DB*

3D FLUX PATH HEIGHTENS BRUSHLESS DC TRACTION-MOTOR PERFORMANCE

Dc traction motors have the necessary speed-torque characteristics to move a large inertial load and then maintain operation under reduced-load conditions when the driven device reaches terminal velocity. Typical of such applications are trains, cranes, elevators, and fork lifts. The weak spot in this device, causing recurring downtime and maintenance expense, has been the motor's soft carbon brushes, used for field excitation. A patented motor design, developed by American Motion Systems, Inc., Camarillo, Calif., provides the same speed-torque characteristics of a conventional dc traction motor, without the disadvantages of carbon brushes. The use of electromagnetic-field excitation, instead of permanent magnets, allows the field flux to be adjusted electronically to produce any required combination



of speed, power factor, torque, and efficiency.

Called the Electric Turbine, the brushless traction motor is a 3-phase variable-reluctance machine driven by an ac inverter or brushless dc drive. Brushless operation is made possible by the unique rotor design. The two-piece rotor consists of mild-steel inner and outer components, which channel magnetic flux across an air gap to and from stationary field coils. Axial projections on the outer rotor component constitute one magnet

pole, and two radial projections on the inner rotor component constitute the opposite polarity (*see the drawing*). Upon rotor assembly, the cavity between the two rotor components is filled with aluminum, so that the two parts are mechanically fixed together but magnetically isolated.

A bobbin-shaped coil of magnet wire, wound on a core attached to one of the motor's end bells, generates the field flux and is separated from the rotor by air gaps. The stator (armature) functions the same way as those in conventional 3-phase synchronous or induction motors. Both the armature and field windings do not rotate. Cases and bearings are the same standard components and materials used in other motors. The inner and outer rotor components are inexpensive mild-steel castings, separated by an inexpensive, die-cast nonferrous support that is cast in place.

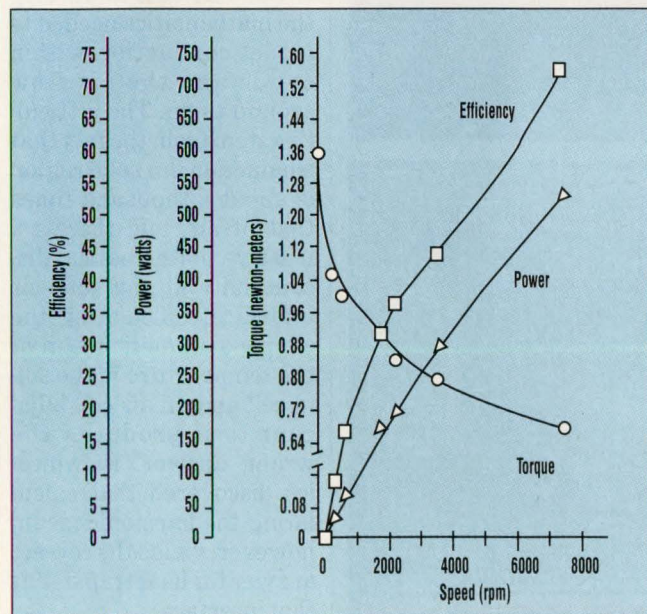
In operation, the electromagnetic flux path passes from the center of the field coil, through the field-coil back iron, and to the outer rotor component's axial projections. Continuing ra-

dially from these projections, the flux then enters the stator winding in a fashion similar to a synchronous motor. Flux returns radially from the stator into the radial extensions of the inner component of the rotor and continues axially along the shaft to the field core.

Dan McGee, coinventor of the motor, says the name Electric Turbine comes from the 3D flux path produced by this axial-to-radial flux distribution. With salient north and south poles formed at the inner and outer rotor components, the Electric Turbine can operate as a synchronous motor when energized by a 3-phase open-loop power source, or as a brushless dc motor when equipped with a rotor-position sensor and connected to a brushless dc drive.

Traction-motor torque is inversely proportional to the square of the speed. This is accomplished by connecting the armature and field winding in series and electrically commutating the armature phases. The brushless dc drive must provide both power and commutation to the brushless traction motor. The power source can be electronically commutated pulsed dc, or more typically trapezoidal or sinusoidal ac, fed to the motor's three or more armature phases.

Several fractional-horsepower Electric Turbine motors have been tested in a variety of National Electrical Manufacturers Association (NEMA) frame sizes. In one test for a NEMA 42-frame, 8-pole Electric Turbine design, continuous motor torque for speeds from 0 to 7500 rpm dropped from 1.34 to



0.66 newton-meters, while drive efficiency increased from 0 to 71.9% (see the performance curves on the previous page). The motor was connected to a rocking-mount dynamometer with a 2.5-lb load connected to a 12-in. lever. The ac-inverter power source rectified a single-phase sinusoidal input (between 212 and 218 V at 1.3 to 3.4 A

with a 100% power factor), and generated 3-phase, pulse-width-modulated square waves from 0 to 67 Hz, and 6-step current waveforms from 67 to 1000 Hz. The inverter used six power MOSFETs and their associated circuitry. The motor's armature winding produced a trapezoidal waveform.

Another test compared

the power consumption of a 1-hp (120-V) variable-speed Electric Turbine drive system against a 0.5-to-1.5-hp (220-V) 2-speed induction motor in a commercial washing-machine application. After 72 hours of continuous operation, the Electric Turbine system had used only 60% of the power consumed by the induction motor.

American Motion Systems can size an Electric Turbine to any horsepower, speed, torque, or efficiency requirement. Or, the company can supply the specialty rotor, dc-field excitation, and electronics for final assembly by the user. Interested parties may call Bill LaRosa, president, at (805) 482-0407.

MILT LEONARD

COMPUTATIONAL FLUID DYNAMICS DETECTS THERMAL PROBLEMS IN ELECTRONIC SYSTEMS

A new approach to an old technology combines the power of computational fluid dynamics (CFD) with electronic-design automation, eliminating the steep CFD learning curve while providing engineers with accurate thermal estimates of electronic systems. Although CFD, a technology that's been around for about twenty years, is perfectly suited for predicting air distribution in electronic systems, its tools are cumbersome and complex, restricting its use thus far to products with longer design cycles, like jet airplanes. Now a British company called Flowmerics Inc., Westborough, Mass., has come up with a software package, Flotherm, whose menu-driven interface brings fluid dynamics within reach of electrical engineers.

All electronic systems dissipate thermal energy into the environment by a combination of conduction, convection, and radiation. In most cases, air is the primary cooling medium and air movement is the primary heat-transfer mechanism. Predicting how the

air will move through a system before it's built is one of the most difficult and important problems engineers face. It's not enough to calculate a basic heat-balance equation, because engineers need to know ex-

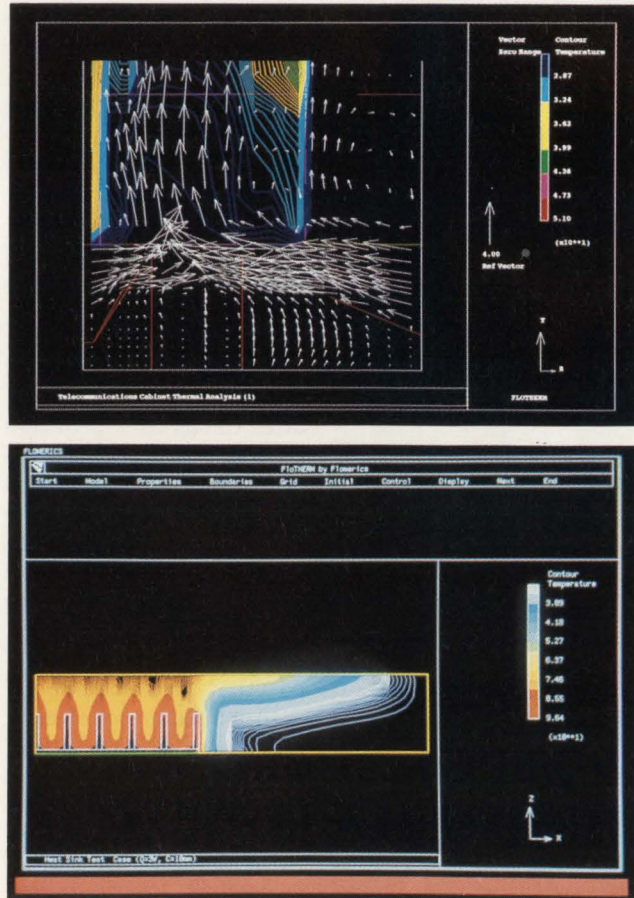
actly where the air will and will not go.

One of Flotherm's special menus provide a quick, simple method of representing a pc board in an enclosure—an enormously complicated task for users

of traditional CFD programs. The menu accepts parameters such as the heat dissipation across each region of a board, and defines entities like fans with such factors as flow rate and air temperature.

CFD solves the fundamental differential equations that govern the conservation of mass, momentum, and energy in fluid flow. The differential equations are transformed into vast arrays of algebraic equations that define the interactions between tiny fluid "cells" and their neighbors.

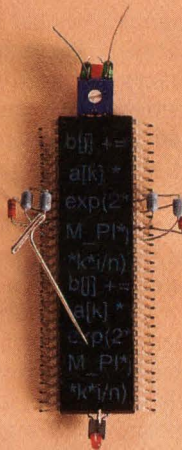
According to Mike Reynell, Flowmerics president, it was difficult to develop the mathematics needed to model conduction within solids and the air flow around them. The difficulties stem from the fact that conduction in a solid region is about a thousand times that of air, and there's a massive mathematical discontinuity at any solid-air interface. Calculating the simple arithmetic mean of the temperature in the solid cell and an air cell adjacent to it produces the wrong answer. Flowmerics discovered that calculating the harmonic mean, however, yields the correct answer for heat transfer at that interface.



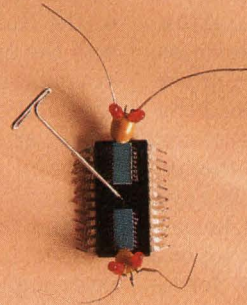
Now catch the bugs that defy logic.



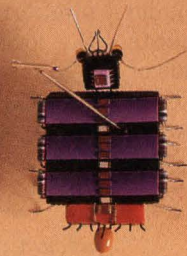
LOCK UP



INCORRECT REGISTER VALUE



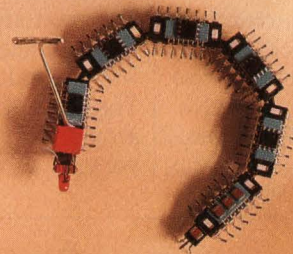
RANDOM OUTPUT



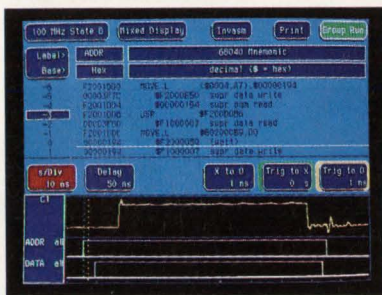
PARITY ERROR



UNEXPECTED EXCEPTION



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Another problem area Flowmerics encountered in going from general CFD to electronic-design CFD is buoyancy calculation. Buoyancy is sometimes, but not always, an important factor in forced-convection electronic systems, in which fans and other devices move the air. In a system that has no fan, however, like a television set or a monitor, the only forces that drive the air through the system are natural buoyancy forces. The buoyancy term, while critical to the design, is difficult to include in the CFD equations without making the equations unstable.

Flotherm is currently a stand-alone package, although the company has been developing several interfaces. Users must manually enter the Flotherm

information with a menu-driven, Motif-like interface. The first thing users specify are the properties of the fluid that's used to cool the system. Next, users must define the size of the solution box (the area, larger or smaller than the finished product, under study).

After the solution box is defined, it must be divided into computational cells, or elements. The program does this automatically with a mesh generator. Users then define any features inside the solution box, such as solid objects or heat sources, that affect air flow or temperature. The next step is to define flow boundary, i.e., the entry and exit points of air. These could include, for example, a fan, an opening, a vent, or a grill. Lastly, us-

ers list incidental sources. These include resistances caused by a perforated surface such as a filter or drilled plate.

The program uses the inputs to calculate the air flow and display it graphically (see the photograph, top). In the example given, Flotherm shows air-velocity vectors and temperature contours at the air-inlet region of a cabinet containing telecommunications equipment.

Flotherm also calculates heat flow at the device level, a process that requires completely different calculations from those required by system-level problems. Designers build up complex components out of solid blocks made of silicon and ceramic. Then they layer these blocks together, each with its own

thermal conductivity. A heat source can be placed inside the solid.

Results for device-level problems are also shown graphically (see the photograph, bottom). In this example, temperature contours in both the solid and air are shown for a heat sink attached to a 4-W device in a natural-convection environment. For this type of device-level calculation, users need to input only the geometrical information, heat dissipations, and conductivities of solid regions. When designing for a forced-convection environment, users need to perform a cabinet-level simulation to determine the local air velocity and temperature before performing this detailed, device-level calculation.

LISA MALINIAC

COLOR-RECOGNITION SYSTEM DISTINGUISHES MORE COLORS, MORE ACCURATELY AND FASTER

The latest version of a color-recognition system developed by AEG of Frankfurt, Germany, distinguishes colors much faster and more accurately than the human eye. For use in automated industrial processes to spot and help sort objects according to their color, the system can differentiate between more than 20,000 different mixtures of the red, green, and blue primary colors. Recognition time is from 1 to 5 ms, depending on contrast.

The computer-based Logipal 4 system is the latest version of color-recognition equipment that AEG has been marketing for a number of years. Version 4 adds software control of

many functions and parameters, and is now menu-driven.

Color recognition is basically accomplished by splitting the light from an object into the primary colors' spectral ranges, according to each color's wavelength, and by comparing the intensity of the three color components with stored reference data. Colors with wavelengths in the range of 400 to 700 nm can be recognized.

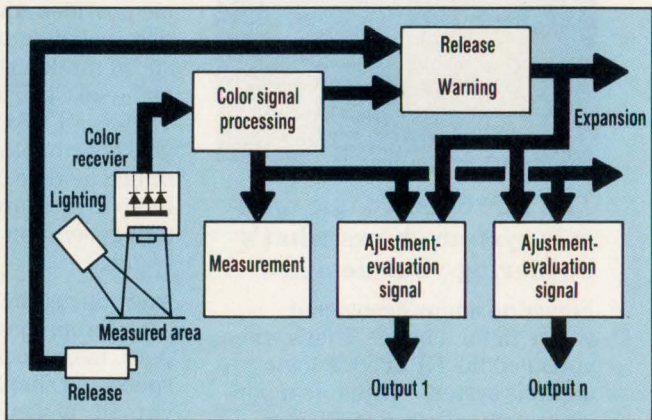
The recognition process is accomplished by means of a defined-wavelength halogen lamp, an optical cable with a scanning head, a color receiver, and a compact computer with an 8-bit processor for evaluating the received color informa-

tion (see the figure). It begins when the light from the lamp, which goes through an optical cable and bounces off a lens in the scanning head, is trained on the object whose color is to be recognized.

The reflected light, hitting the lens and passing

back through the optical cable, enters the color receiver. The receiver, in turn, divides the light into the spectral fractions of red, green, and blue, and converts the intensity of each part into a dc voltage.

The three dc voltages are transformed into four relative voltages, representing the percentages of the three colors as well as the brightness level. The



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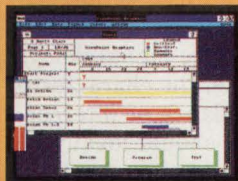
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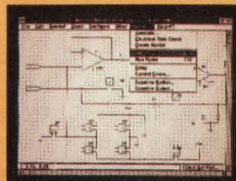
CAM

**PROJECT
MANAGEMENT**



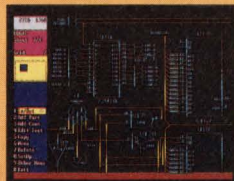
**PROJECT
MANAGEMENT**
Software

**CIRCUIT
SIMULATION**



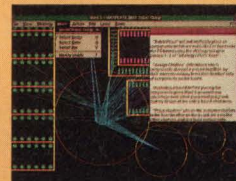
PSPICE
Windows Schematic
Capture

**PCB
LAYOUT**



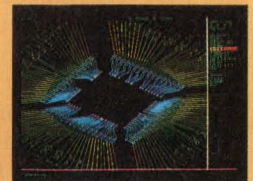
PADS-LOGIC
Schematic
Capture

**AUTOPLACE
AUTOROUTER**



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Autoplacement
New!

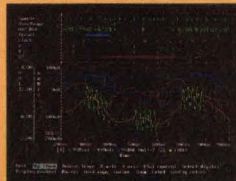
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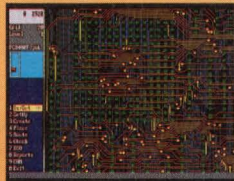
AUTO CAE/PCB
Layout
Software



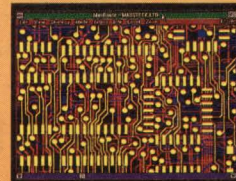
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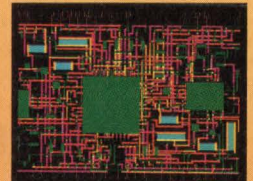
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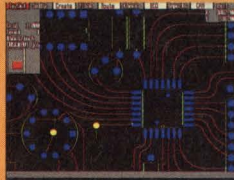
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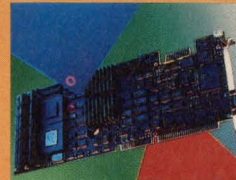
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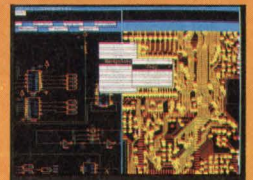
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three color voltages remain constant, even when the distance to the object changes. When colors to be sorted differ mainly in brightness, the brightness, or grey level, can be the determining value.

The computing system compares the measured voltages with stored color reference data, generating a signal when the color is correctly recognized and identified. Reference colors are stored as voltage levels or as memory locations in the processor-controlled computer modules.

The halogen lamp has a service life of about 5,000 hours, and intensity variations due to aging are automatically compensated for. The distance from the scanning head to the object

can span 5 mm to 1 m. The area whose color is to be determined can be from 0.5 to 150-mm in diameter.

Logipal 4 is available in a compact rack version or a desktop version with monitor and keyboard. It can have up to four color receivers. The software controls different functions such as color-data comparison, correction calculations, white balance, and the feeding in of a color as a reference.

Automated industrial processes are a natural application area for Logipal 4; among them, selecting and distributing bottles and boxes according to color, screening colored package surfaces with stick-on labels, and controlling the selection of components in

car-body assembly.

Other jobs include recognizing cables, inspecting solder joints on rotors of small generators, check-

ing the insulation of copper-wire coils, and monitoring the color of varnishes, glazes, and enamels.

JOHN GOSCH

STRIPLINE CONNECTOR SYSTEM HOLDS DOWN RINGING

As computers get smaller and faster at the same time, the issues of signal delays and noise become more and more critical. Of paramount importance is the matching of impedances in connectors, cables, and lines. At this week's Wescon/91 show, Fujitsu Microelectronics Inc., San Jose, Calif., will introduce a matched-impedance (50- Ω) stripline connector system on a 0.050-in. pitch (*see*

the figure). The FCN-260 connectors promise maximum crosstalk of as low as 1.2% on a 1-ns rise-time signal.

To reduce signal delays and noise, the characteristic impedance of interconnections should ideally be matched to their load impedances. In this way, the ringing noise and crosstalk on signals are minimized. In conventional connectors, all contacts have the same form and the ground

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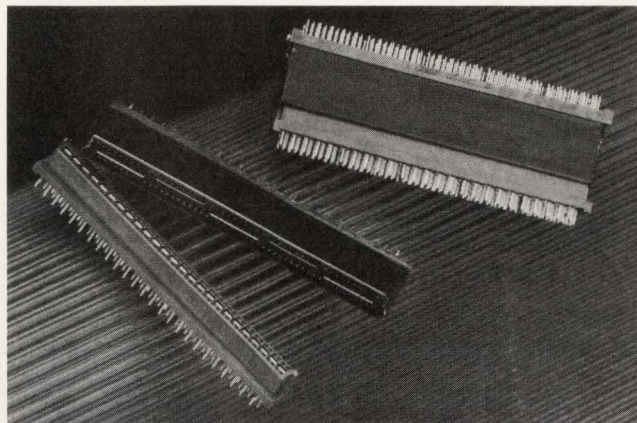
The advertisement features a central computer monitor displaying a 3D visualization of a memory array. Two men are shown in profile, one on the left gesturing towards the monitor and one on the right looking at it. Overlaid on the monitor is a schematic diagram of a memory system. The diagram shows a 'PROCESSOR' on the left connected to 'SRAM' blocks. The top SRAM block contains 'TAG MEMORY' and is connected to 'ADDRESS BUS' and 'DATA BUS'. The bottom SRAM block contains 'DATA MEMORY' and is also connected to 'ADDRESS BUS' and 'DATA BUS'. A 'CACHE CONTROL LOGIC' block is connected to the top SRAM and a 'MAIN MEMORY' block. Arrows indicate data flow between the processor, SRAMs, cache control logic, and main memory. Labels include 'ADDRESS BUS', 'DATA BUS', 'SELECT', 'HIT', and 'TAG MEMORY'.

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contacts are selected from them. Typically, the number of ground contacts is equal to or less than the number of signal contacts, in which case the ground contact does not provide a good reference. This results in poorly controlled impedance matching and ensuing losses of fidelity.

Fujitsu tackled the crosstalk problem by using large blade-shaped ground contacts on the centerline and a ground shell around the plug. As a result, all signal contacts have ground planes on both sides, which accounts for the connectors' classification as a stripline structure. The characteristic impedance of the connector is designed to be 50 Ω , $\pm 10\%$, and is achieved by control



of the dimensions, construction, and the insulator's permittivity. The broad contacts work as the reference plane, whether they are ground or power contacts.

Because a printed-wiring board (PWB) has wide ground planes and fine sig-

nal lines close to the ground, the ground works as a reference and the signals transmit in an unbalanced load. When an unbalanced transmission line such as a PWB and a balanced line such as a twisted pair or conventional connector are linked, balance-

unbalance mismatch will occur. At the connected point, reflection sets in even if the characteristic impedance is equal. Then, as the electromagnetic radiation to the outside world grows, the crosstalk increases.

But the ground in the FCN-260 connector is far larger than a signal contact, so that the signals can maintain the same unbalanced transmission mode in the connector as on a PWB. This enables the connector to be used for a high-speed bus. The design also eliminates the need for dedicated ground contacts so that more signal contacts can be used to transmit high-frequency signals of 40 MHz or higher.

DAVID MALINIAK

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Product family highlights

Part #	Orgn.	Speeds (ns)	Features
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ATT7C116	2Kx8	10,12,15, 20,25ns	Common I/O Output Enable
ATT7C166	16Kx4	10,12,15, 20,25ns	Common I/O Output Enable
ATT7C185	8Kx8	10,12,15, 20,25ns	Common I/O Output Enable Two Chip Enables
ATT7C174	8Kx8	12,15,20,25ns	Tag RAM, Flash Clear & Comparator
ATT7C183	2x4Kx16 or 8Kx16	25,35,45ns	Cache RAM for 386 Systems
ATT7C194	64Kx4	15,20,25ns	Common I/O
ATT7C199	32Kx8	12,15,20,25ns	Common I/O
ATT7C157	16Kx16	15,20,24,33ns	Synchronous



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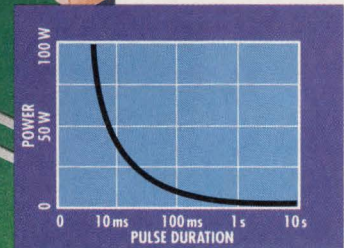
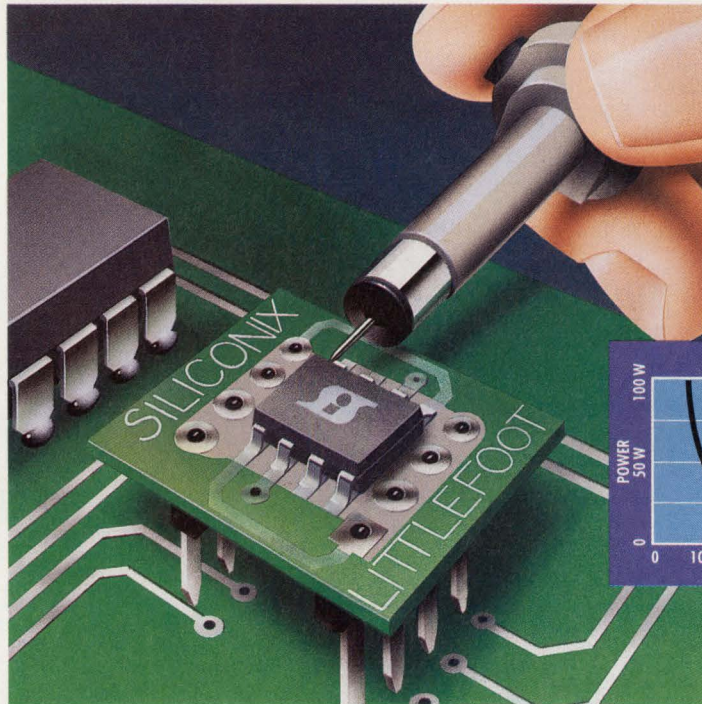
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Current Rating:	4.5 A
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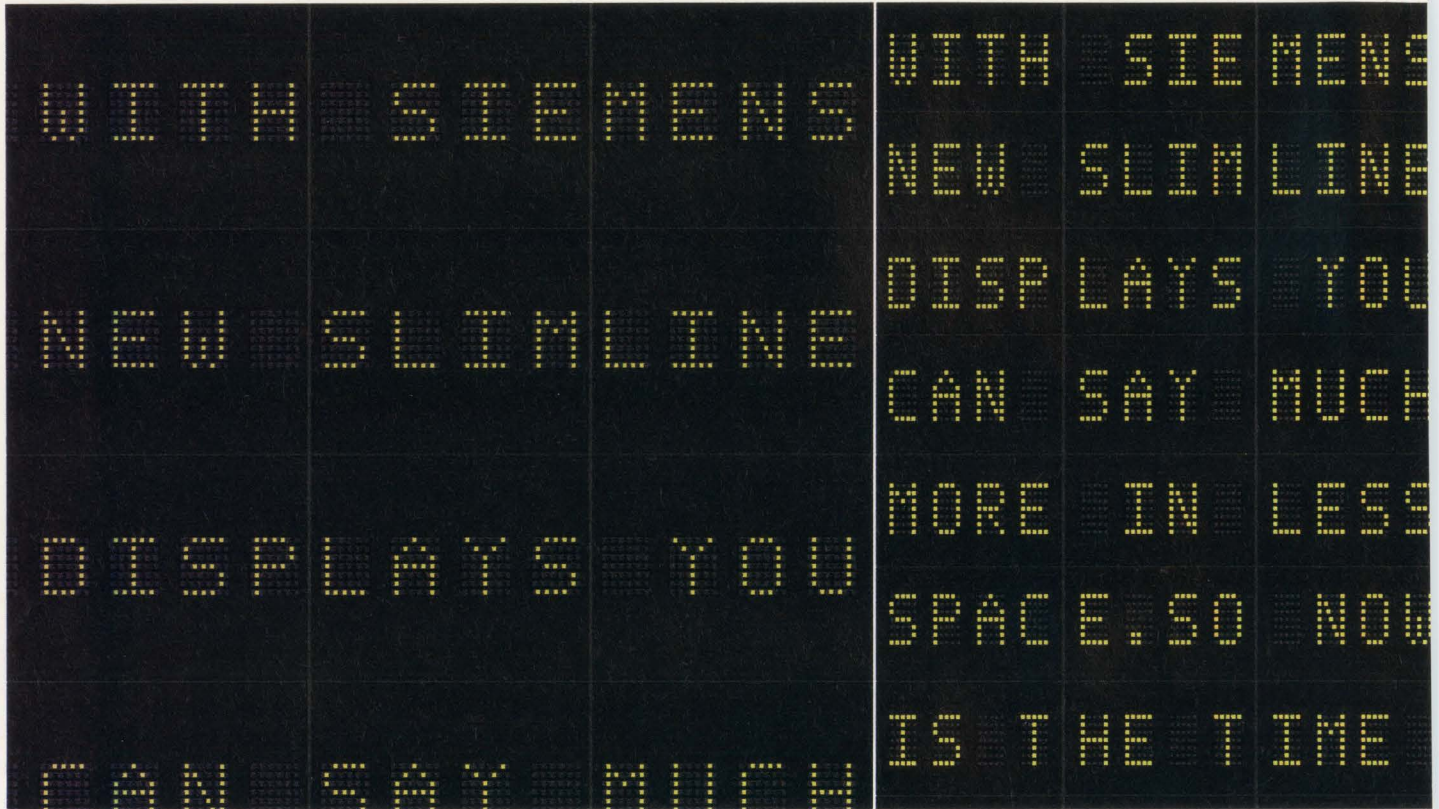
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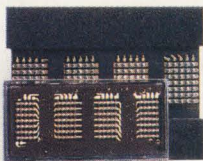
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FRANK GOODENOUGH

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These conclusions are drawn after a week spent talking informally with over 30 designers of analog and mixed-signal circuits and systems. None are in the semiconductor business. Some are still working on their first design, while others have been practicing their profession for five or more years. At least one cut his teeth on vacuum tubes, while others are recent college graduates. Several are the company's only designer; others are the lone analog hands in 20-person IC design groups. All still consider analog design their expertise.

The survey cuts a clear swath across practitioners of virtually all available analog and mixed-signal ASIC technologies. It includes metal-mask-configured analog and mixed-signal arrays, as well as standard-cell-library, full-custom technologies (which need a complete set of masks) for pure analog and mixed-signal circuits. It turns up designers who use Harris Semiconductors' Fast Track, which can turn an analog circuit designer into a custom IC designer virtually overnight. And it also includes designers using direct write-on-wafer electron-beam lithography from United Silicon Structures (US2).

ASIC processes covered range from general-purpose bipolar arrays, whose npn transistors provide f_s of 300 MHz, to Tektronix's bipolar arrays, whose npn transistors reach 10 GHz. It includes 1-to-2- μm CMOS standard-cell/custom technologies, and Plessey's CMOS mixed-signal arrays. Also included are Exar's latest complementary biCMOS standard-cell process, offering 1.1-V 4-GHz npn and 1.5-GHz pnp transistors, along with similarly powered 2- μm CMOS and EEPROM processes. Also represented: 1.5- μm CMOS-on-sapphire; radiation-hardened, standard cells from ABB HAFO; and US2's 1- μm electron-beam CMOS process.

LIKE A MARRIAGE

Several major points become clear from the interviews (see "What ASIC users are saying," p. 38). To start, first-pass success can be accepted as routine. However, the system/circuit designer must approach each new ASIC with an open mind. All those interviewed agree that the single most important factor for success lies in a close working relationship between user and vendor designers. For this marriage to work, the vendor must understand the user's system; the user must understand the vendor's technology and its limits. This is true whether the user (70% of those surveyed) or the vendor (30%) is responsible for the IC's design. Vendor-designed ASICs are included because in virtually every case, the user provides the vendor with a block diagram, and/or a schematic, and/or a bread-

ANALOG AND MIXED-SIGNAL ASICS

board, and detailed specifications based on a thorough knowledge of the vendor's technology. In many cases, even if the vendor designed the chip, the user duplicated the simulation and built and tested additional breadboards.

Second, whether using arrays or cell libraries, most designs are done at the transistor level. While most vendors provide macros for arrays and offer large contingents of analog cells in their cell libraries, only one or two macros or analog cells can be used for any particular ASIC. This is borne out by the experience of several analog and mixed-signal ASIC vendors, who have concentrated their ASIC technologies over the past several years in large measure on standard products. They too have found that the demands of analog systems on circuit design are just too unique to be filled by even several hundred analog cells. How else to explain the thousands of successful standard-product analog ICs available, many over twenty years old?

Not all chips, however, must be designed completely at the transistor

level. In many cases, macros and cells can be modified. Many users have created their own library of macros or cells over a period of time, which they use repeatedly. In effect, the circuit/system designer must learn to think like an IC designer.

DISKS TO DIPSTICKS

Designers interviewed reveal a mind-boggling array of applications for ASICs. Except for those working on chips for PCs, tape drives, or disk drives, no duplication of end-use products appears. (Disk drive manufacturers have long been major users of analog and mixed-signal ASICs, both array and cell-based). The case histories shown here show typical migration paths to analog and mixed-signal ASICs, taken for typical reasons.

The "Elektronik Dipstik," developed by a Houston company, is an oil-level indicator for automotive and marine internal-combustion engines. The circuitry for this device all fits on one of Raytheon's bipolar analog arrays. The ASIC monitors temperature sensors mounted on a special

dipstick and reports oil levels when interrogated with a pushbutton. The company's first ASIC, it was begun with a discrete breadboard. The company then took it to Raytheon to see if its size and cost could be trimmed. Raytheon built a second breadboard from its own kit parts and hooked it to a dipstick. After testing that design, Raytheon put the circuit on one of its arrays. The Dipstik's developer says the next time they'll need an IC, they'll do more of their own design.

Using an array from the same Raytheon family, a designer at an avionics company built circuits that will go into Boeing's next-generation 777 airplane, Boeing's first wide-body fly-by-wire aircraft. The firm's first ASIC, it will form the servo amplifiers that link the digital data from the cockpit to the valves controlling the flight-control surfaces. Boeing instructed the designer to halve the board area of existing designs, and cut power from 10 to 2 W. The circuit designer built a breadboard with Raytheon kit parts; Raytheon did the simulation. The board-level circuit, however, had been simulated origi-

WHAT ASIC USERS ARE SAYING

• *On engineers' perceptions of analog and digital designs:*

"Analog designers learn digital design more easily than digital designers learn analog design."

"Most digital designers *still* consider analog design a black art."

• *On the usefulness of going the ASIC route:*

"Just do it."

"Be wary of jumping in feet first."

"The lower power almost always provided by an ASIC, even if not high on the priority list, can become a real advantage."

• *On lessons learned while going the ASIC route:*

"Basic system problems are most apt to prevent first-pass success."

"...your second one is easier."

"If you're laying out an array by

hand, get a big eraser."

"...learn to be an IC designer."

"When working at very high frequencies, often an IC, and thus an ASIC, is the only way to achieve the required performance."

"Accept the idea that you must do things differently."

"Move to mixed-signal designs slowly. Do an analog chip and a digital chip the first time, then a mixed-signal chip."

"The first time, don't try and put all circuitry on one chip. For example, use two small arrays instead of one big one."

"Don't simulate to death if time-to-market is important...It's not always necessary for first silicon and thus the end product to work exactly right when put into a beta site."

• *On the vendor/user relationship:*

"Know your silicon vendor's de-

signers as well as you know your own."

"If the vendor is doing the design, do *everything* in parallel."

"Know the constraints of the process."

"Have it designed before you choose the vendor."

"Vendors need better control of their processes over time. Next year's chips may not work in your end product if transistor f_s or betas change up or down."

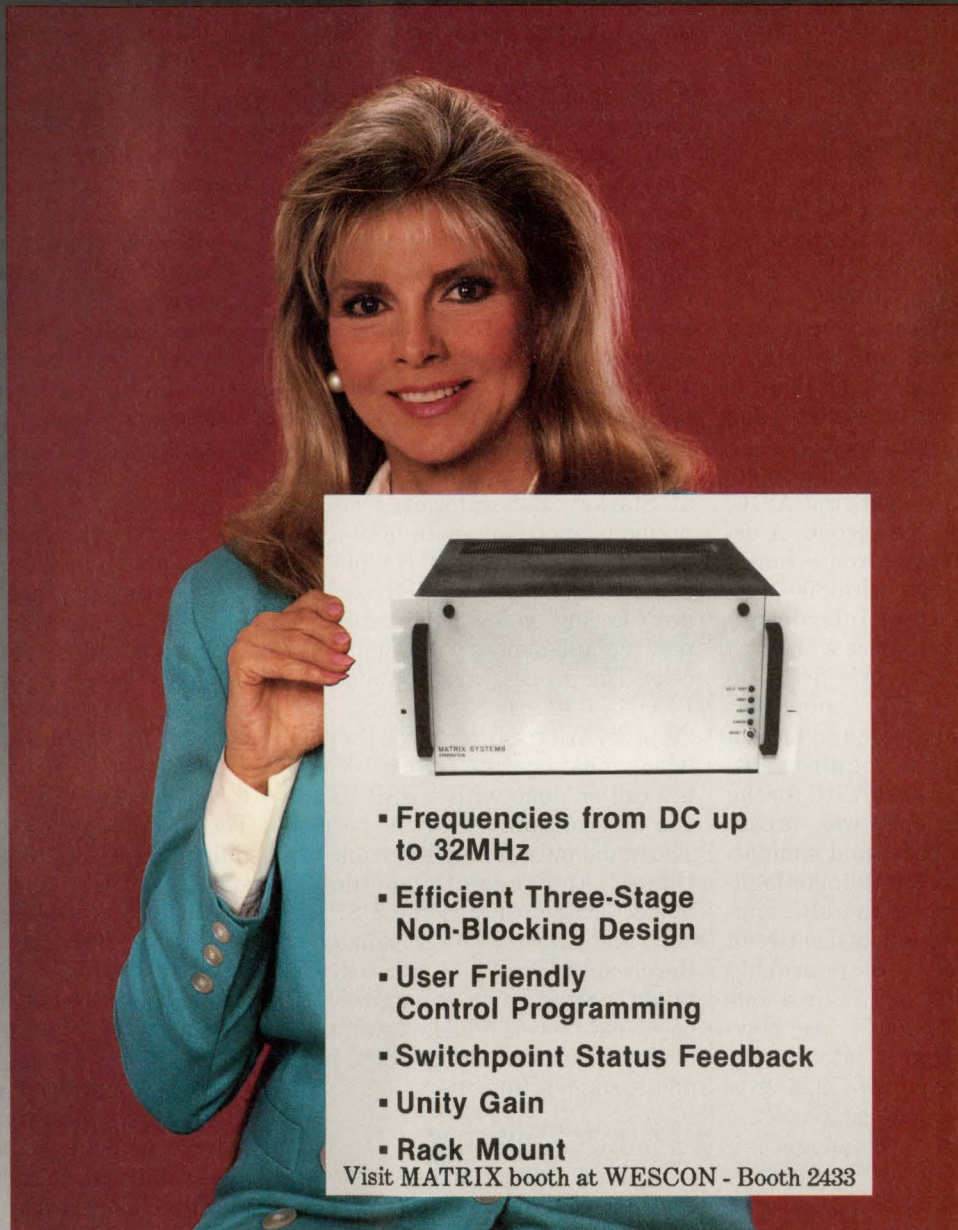
• *On breadboarding:*

"Breadboard....breadboard....breadboard...."

"If you breadboard the whole system as well as the ASIC, you'll insure that the ASIC functions in the system. Breadboards tell you what you forgot."

"When you schedule the program, *plan* on two passes. The first is a silicon breadboard."

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ANALOG AND MIXED-SIGNAL ASICS

nally with Daisy software.

In most ASIC designs, but especially with cell-based technologies, layout is left to the vendor. However, a designer who had designed the circuits for a hand-held, auto-ranging multimeter worked closely with Holt when drawing the floorplan. He had used standard cells from Holt's CMOS library. Joint work on the layout insured minimum noise and thermal effects. CMOS was used to minimize input current. Single transistors equal in area to all the digital circuits minimized CMOS-op-amp input noise, and auto-zero circuits minimized drift. The ASIC essentially made the final product possible. It minimized size, power, and cost, and kept the design proprietary.

Some brave designers will breadboard and simulate their first ASIC, but only simulate the second. A designer at a military electronics house used a bipolar array with 800-MHz npn transistors from Interdesign Custom Arrays to replace a discrete radar-warning-receiver's dc-to-10-MHz logarithmic video amplifier. Again, the IC was needed to meet a new project's space requirement. And again, it was a first ASIC for the firm. While this chip was breadboarded with kit parts and simulated, a second ASIC, for a similar logarithmic amplifier, was merely simulated. Although it contained between 90 and 100 transistors, the entire chip was simulated on a 386 PC in about 20 minutes. This speed is rare, however; most designers interviewed can't simulate a complete chip on a PC. They do it in functional blocks.

While most ASIC technologies allow you to design at the transistor or macro/cell level, Harris' Track software and process let you go one step further: designing your own fast, vertical npn and pnp transistors. You call out the specifications (β , f_t , etc.) you need and the tool comes up with a device of the proper size, shape, and performance. First you simulate your transistor, then your circuit, as you build it transistor-by-transistor. When you finish, you not only have a schematic, but also a schematic-based layout.

A designer at Oak Ridge National

Laboratories used Fast Track to design a family of charge amplifiers, essentially quad, current-feedback op amps, which may be used by the millions in the calorimeter for the super collider. The technology made possible tradeoffs between current and voltage noise and device-level design, helping to make the circuit radiation-hardened. While the ASIC approach was used primarily to reduce size and cost, it also cut power and upped reliability by permitting the amplifiers to be closer to the tens-of-thousands of detectors they monitor, thus reducing the lead inductance from cabling.

Expert analog IC designers will tell you not to put a radical new circuit design on a radical new process. One who didn't listen was a designer at Starkey Laboratories, who had previous successes with both array and cell-based ASICs. He put the first hearing aid with DSP-based digital filtering on a chip, using Exar's new complementary biCMOS process. The process also contains EEPROMs (ELECTRONIC DESIGN, Aug. 22, p. 29). All the filtering on the chip, which must operate from a 1-V supply rail, is done with a DSP IC and can be programmed by the patient. The audio-output amplifier runs in a Class-D (pulse-width-modulated) mode. Exar designed the DSP circuit, and Starkey the remainder of the circuits. The ASIC approach was taken primarily to minimize size, cost, and power, while allowing the designer to get a proprietary jump on the competition.

HEALTH MONITORS

In many cases, analog designers first use analog simulation in the design of an ASIC. A company building hazardous-gas detectors put all the circuitry for a new model on a mixed-signal Plessey CMOS array. One of the few not using Microsim's P-Spice on a 386-based PC, the company used Intusoft's version of Spice to do the job on models supplied by Plessey. The detectors represent a three-way cross between beepers, the film-type detectors worn by individuals working near ionizing radiation, and the old-fashioned gas-detecting device

of the coal mine—the canary. Each electro-chemical-sensing detector is clipped to a miner's clothing, beeps when sensing a hazardous gas, and must run for a year on a battery. The sensor is only good for about a year, so an internal clock keeps time and it beeps when the year is up.

The ASIC approach was taken primarily to cut size, power, and cost, and to get a proprietary jump on competitors. The resulting detector is both smaller and cheaper than possible with other design approaches, and uses just 400 μ W of power. According to its designer, design refinements can trim power dissipation even further, to just 150 μ W.

Of course, system problems often stand in the way of first-pass success. A case in point is a designer at a pharmaceutical company, who put the circuitry for a blood glucose analyzer on a full-custom, mixed-signal Texas Instruments CMOS ASIC. The IC takes the signal from a photo sensor, conditions it, digitizes it, and drives a liquid-crystal display. It must operate for more than five years off a lithium battery. It must also be very low in cost, as it is made for home use by diabetic patients. The designer gave TI a complete, detailed block diagram and a set of specifications.

The first-pass design did not do the job, however, because the designer did not understand the battery's performance and didn't do enough simulation. More complete simulation, before handing TI the specifications, would've produced a working design. Again, the ASIC approach was taken primarily to minimize cost and power, but also to shrink size and increase reliability. The result was the first such device for under \$50.

When space is at a constraint and when working at frequencies above, say, 100 MHz, only an IC can provide the performance required. This was the reasoning behind a family of gigahertz RF circuits that were put on Tektronix analog arrays. The designer of military global-positioning satellite (GPS) system components chose the arrays, built on Tektronix's "super-hi-pi" process. They not only have 7-GHz npn transistors, but

ANALOG AND MIXED-SIGNAL ASICS

thin-film resistors as well. Having used the arrays for several years, the designer was able to develop a set of reusable macros that include RF mixers, amplifiers, and analog switches—the last no mean trick on a bipolar process. Both size and performance demands were met, and cost was also minimized. Seizing on the cost advantage, a designer at another company devised a custom IC on the same Tektronix process for a consumer product: a complete GPS navigator for small boats.

So far, little has been said about the relative merits of using electronic-beam lithography as a process approach, or the use of arrays vs. cells vs. full-custom ICs, as design approaches. Experience with digital ASICs is one of the few areas that may help a little in dealing with these issues. In most cases, three factors determine the choice of process and design method: volume, turn-around time, and cost. There are, however, some exceptions to these rules.

Normally, you choose the full-custom approach for the highest-volume designs, and arrays and/or electron-beam lithography for the lowest-volume jobs. Turn-around time is fastest for the electron-beam technique; full-custom, of course, takes

the most time. Arrays tend to have the lowest non-recurring-engineering (NRE) costs, and full-custom the highest. However, give Orbit Semiconductor a GED tape (a processing tape containing design parameters) and they'll give you a dozen prototypes of an analog or mixed-signal cell-based or custom IC in a couple of weeks for under \$2000. Canadian manufacturers have access to a government-sponsored program that provides similar services.

If you can afford the NRE costs, electron-beam lithography seems to be the way to go for quick chip turn-around. To minimize size and power, for example, a designer of military electronics put the equivalent of a 32-channel, 5-MHz, 25-ns, logic analyzer on a single CMOS chip built using US2's electron-beam technology. The complex chip had six-phase clocks running at 60 MHz. Total turn-around time from start of design to prototypes ran less than three months and NRE costs ran about \$50,000. Chip volume ran about 1000 pieces, at about \$200 per chip.

TOTE THAT WAND

"Learn IC design" is a common refrain among designers interviewed, although on-the-job training seems

to work. More than one of the designers admitted they were a little scared at the start of their first chip, but in virtually every case the design went smoother than expected. One designer made a few mistakes on his first ASIC, for wand-type bar-code readers, winding up with ground loops. Still, although not quite to specifications, the chip worked the first time.

Bar-code readers may seem simple, but just think about the clock-recovery problem inherent in a scan velocity set by the human hand operating the wand. Additionally, the code may have been printed by a dot-matrix printer, so a scan may go between the dots and miss one bar or more. The designer chose to put all the reading and analysis circuitry—all pure analog signal-processing—on a single Plessey bipolar array.

The most important reasons for choosing a particular process technology for your ASIC are similar to those for choosing a standard-product IC. If the process offers dielectric isolation—as with the bipolar arrays offered by Sipex and Harris, the Fast Track from Harris, and AAB HAFO's silicon-on-sapphire CMOS cells—then it's easier to think like an IC designer. That's because there are fewer parasitics to worry about,

A SAMPLING OF ANALOG AND MIXED-SIGNAL ASIC SUPPLIERS

AAB HAFO Inc. San Diego, Calif. CIRCLE 711	Electronic Technology Inc. Ames, Iowa CIRCLE 719	IMP (Integrated Microelectronic Products Inc.) San Jose, Calif. CIRCLE 726	NCR Fort Collins, Colo. CIRCLE 732	Sipex Corp. Billerica, Mass. CIRCLE 739
AEG Telefunken Somerville, N.J. CIRCLE 712	GEC Plessey Scotts Valley, Calif. CIRCLE 720	Interdesign Custom Arrays Corp. Sunnyvale, Calif. CIRCLE 727	National Semiconductor Corp. Santa Clara, Calif. CIRCLE 733	TLSI Farmingdale, N.Y. CIRCLE 740
AT&T Microelectronics Reading, Penn. CIRCLE 713	Genum Corp. Burlington, Ontario, Canada CIRCLE 721	Micrel Inc. Sunnyvale, Calif. CIRCLE 728	Orbit Semiconductor Sunnyvale, Calif. CIRCLE 734	Tektronix Inc. Beaverton, Ore. CIRCLE 741
Advanced Linear Devices Inc. Sunnyvale, Calif. CIRCLE 714	Gould AMI Pocatello, Idaho CIRCLE 722	Micronix Integrated Systems Inc. Aliso Viejo, Calif. CIRCLE 729	Raytheon Co. Mountain View, Calif. CIRCLE 735	Texas Instruments Inc. Dallas, Tex. CIRCLE 742
Analog Devices Semiconductor Wilmington, Mass. CIRCLE 715	Harris Corp. Melbourne, Fla. CIRCLE 723	Micro Linear Corp. San Jose, Calif. CIRCLE 730	SGS-Thomson Dallas Tex./Phoenix Ariz. CIRCLE 736	US2 (United Silicon Structures) San Jose, Calif. CIRCLE 743
Arizona Microtek Mesa, Ariz. CIRCLE 716	Hewlett Packard Co. Corvallis, Ore. CIRCLE 724	Motorola Inc. Phoenix, Ariz. CIRCLE 731	Sierra Semiconductor San Jose, Calif. CIRCLE 737	VLSI Technology San Jose, Calif. CIRCLE 744
Cherry Semiconductor East Greenwich, R.I. CIRCLE 717	Holt Integrated Circuits Inc. Irvine, Calif. CIRCLE 725	Motorola Inc. Phoenix, Ariz. CIRCLE 731	Silicon Systems Inc. Tustin, Calif. CIRCLE 738	
Exar Corp. San Jose, Calif. CIRCLE 718				

ANALOG AND MIXED-SIGNAL ASICS

and good vertical pnp transistors are inherent in a complementary bipolar process. In addition, if you need a radiation-hardened device, dielectric isolation is a good place to start. In a military system, for example, a mixed-signal controller for a microwave/millimeter-wave IC (MMIC) fit neatly on the AAB HAFO process. It had 13,000 transistors (3000 gates) and numerous comparators. In addition to achieving a radiation-hardened design, the ASIC was used to meet space, power, and cost needs.

Where once, most ASIC vendors operated like old Henry Ford—you could have any process you wanted as long as it was black—that philosophy has now changed. Many vendors of both arrays and cell-based technologies offer several processes. Many like those from Exar and Gould AMI represent “modular” processes, in which you get only the kinds of devices you need for your

design. An exception is National Semiconductor's Classic group, which started out (at Fairchild) with both a CMOS and a bipolar process and now has just added biCMOS.

A designer at a company building power supplies used both the CMOS and bipolar processes for linear and switching regulator circuits. While cutting board space was the major incentive for using an ASIC, some of the supplies used a particular circuit block as many as four times. However, it was only put on the chip once. Board layout was much simpler with the block in separate packages. In addition, various supplies used the circuit block as many as four times. Multiple chips with the same circuit added flexibility and upped volume, thereby lowering cost.

If you've used accelerometers for test applications, for instance, subjecting your designs to a vibration regimen, you know that the mass of

the transducer can affect the accuracy of the measurements. For similar reasons, however, you would also like to have the signal conditioning located right at the sensor. Thus signal conditioning becomes a natural for ASICs. A circuit designer at a transducer house found Interdesign's small bipolar arrays particularly well suited for signal conditioning in a capacitance-based accelerometer. The accelerometer had to handle 100-kHz signals, yet only a few thousand units were to be produced a year and a low price was imperative. An ASIC fit the bill.

As a final example, take TI's cell-based CMOS technology. Using it, a designer at a candy company put the circuitry for something as mundane as a vending-machine coin changer on a chip, while a designer at a video-system company used it to build a video decoder containing 100-MHz logic and voltage-controlled oscilla-

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ANALOG AND MIXED-SIGNAL ASICS

tors. The chip also contained analog-to-digital and digital-to-analog converters, as well as a ROM look-up table. You could call it a mixed-signal glue chip.

ASIC INCENTIVES

Of all the reasons for taking the ASIC route, size constraints come in first in this informal survey. Keeping costs down comes in second, and keeping power dissipation low comes third. Increasing performance was not the primary consideration, sharing last place with increasing reliability and making the product more proprietary.

As to the type of design implemented, 38% of those queried designed mixed-signal chips using cells from mixed-signal libraries (includes several custom and three electron-beam designs). This was closely followed by 35% purely analog designs. Some 15% of the designs were analog

ICs from mixed-signal cell or custom libraries. Mixed-signal ICs on arrays made up 12% of the total.

Of the of users queried who designed their own ASICs, 90% performed these designs at the transistor level. However, some were able to use a few macros (on arrays) or analog cells. In the 30% of designs in which the vendor was responsible, the user often duplicated some or all of the vendor's work.

About one half of all designs were breadboarded by users, but none of the electron-beam designs were breadboarded. In addition, vendors occasionally breadboarded the design themselves. About 75% of breadboarded designs were also simulated, and of those, about 65% were simulated by users. About 38% of all designs were both simulated and breadboarded.

The type of tools employed were about equally divided between Mi-

crosoft's P-Spice and others' tools. Often, cell-library vendors provided their own, since most major IC vendors, and many of the smaller ones, have their own Spice version.

About two thirds of the designs were crafted on PCs, the remaining third done on (mostly Sparc-based) workstations. PCs ranged from a lone PC/XT to a lone PS-2, but over half were 386-based. □

If you're using analog or mixed-signal ASICs and would like to share your experiences with your fellow readers, drop us a note or fax us your comments to (201) 393-0204. If we receive enough responses, we may publish them in a future issue.

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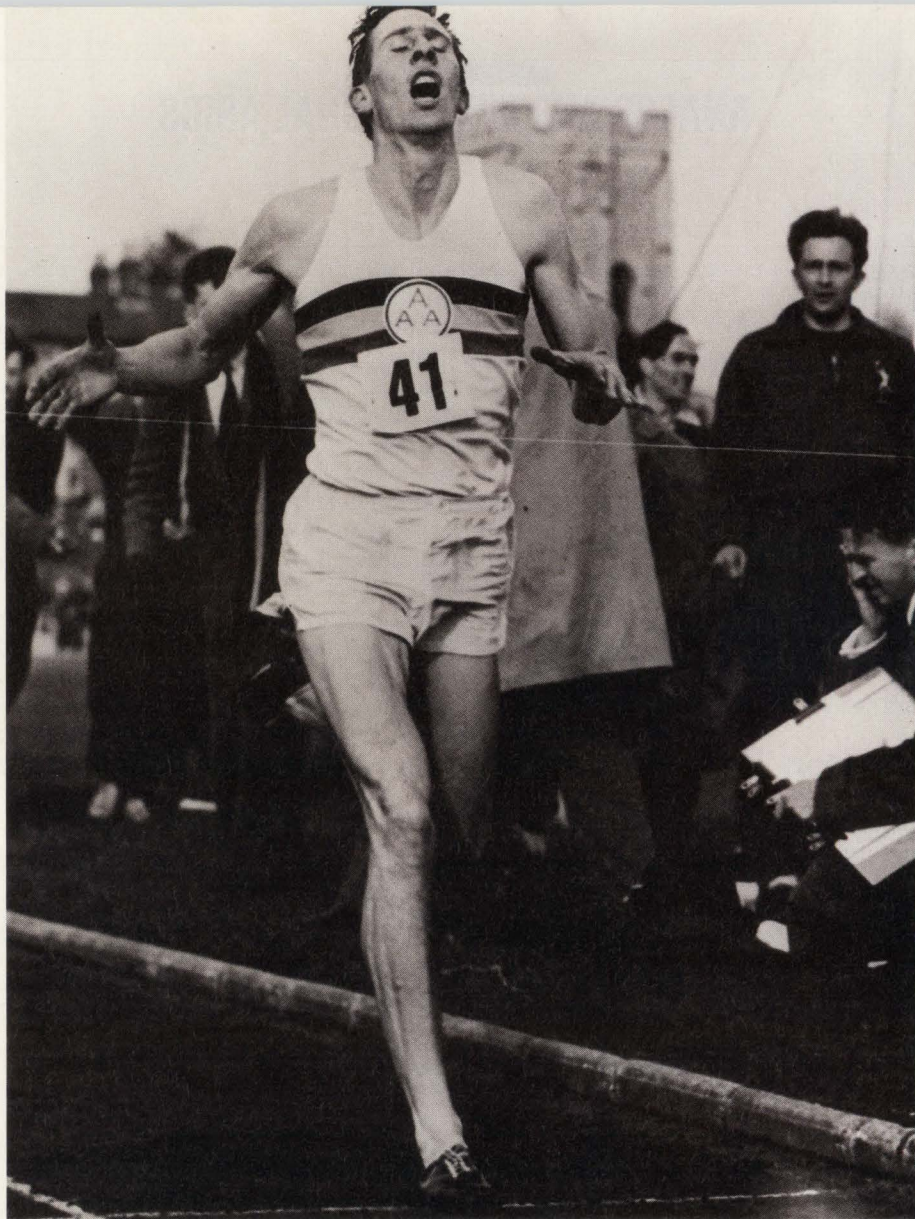
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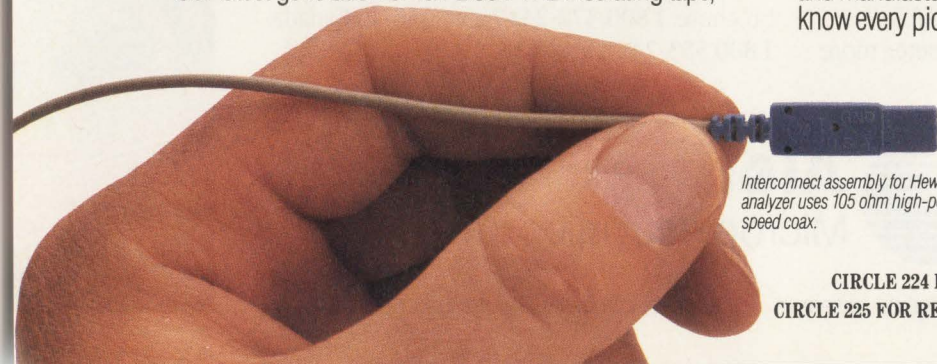
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APPLIED TECHNOLOGY DOMINATES CONFERENCE PAPERS AT WESCON

MILT LEONARD

Technical sessions at this year's Wescon assist engineering decision makers who must cope with fast-moving technological changes. Twenty-nine sessions cover topics including field-programmable gate arrays (FPGAs), high-speed logic design, design for manufacturability and testability, communication networks, programmable-logic devices (PLDs), PC architectures and applications, and more. As a bonus, a special two-hour session features hardware demonstrations and panel discussions on the emerging technologies of virtual reality. Various known as artificial reality, cyberspace, or telepresence, virtual reality goes beyond two-dimensional computer simulations. Through the use of sophisticated software and wearable peripherals such as gloves and goggles, it creates the illusion of an actual full-motion, three-dimensional, even tangible world. The Wescon conference takes place at San Francisco's Moscone Convention Center, Nov. 19-21.

HIGH-SPEED LOGIC

Reflecting the industry's ongoing push for ever-faster data rates in data-processing systems, the lion's share of the program goes to high-speed logic design. Four sessions with a total of 19 papers offer help in dealing with clock distribution, noise, power consumption, interconnect options, and other problems associated with designing high-speed systems.

Four presentations from key device suppliers compare various clock-distribution schemes, and describe benefits, features, and application details of new minimum-skew clock drivers. Another track compares recent standard high-speed logic devices that support high-performance CPUs. Two papers from Integrated Device Technology, Inc., Santa Clara, Calif., trace recent trends in

high-speed device designs and present options for high-speed glue logic using CMOS and biCMOS chips.

A new way to design high-speed data paths is the subject of a paper from Quality Semiconductor, Inc., Santa Clara, Calif. The authors describe the operation and application of the QuickSwitch family of TTL-level CMOS bus-connect devices. These switches reportedly replace traditional TTL buffers and transceivers to reduce propagation delay, noise, control complexity, and power dissipation. They are used in switching applications such as signal multiplexing, resource sharing in multiprocessor systems, and crossbars.

Yet another high-speed logic family is described by National Semiconductor Corp., Santa Clara, Calif. The presentation compares the bipolar family of FASTr TTL logic chips against competing CMOS and biCMOS logic families. Also included are descriptions of National's enhanced process technology and design techniques, which produce buffer delays below 3.9 ns.

Next-generation logic devices must not only keep pace with increasing bus widths and faster clock rates, but must minimize their impact on circuit-board area as well. Texas Instruments, Inc., Sherman, Tex., explores how various fine-pitch surface-mount packages simplify high-speed logic design. The author discusses how the small-outline IC (SOIC) package has evolved along two distinct paths: the 2.0-mm high shrink small-outline package (SSOP) with a 0.635-mm lead pitch, and the 1.1-mm high thin SOP (TSOP) with a 0.65-mm lead pitch. Application examples are given for both packages.

Several presentations address chip- and board-level interconnect design, which becomes a critical issue as clock frequencies exceed 50 MHz. Intel Corp., Hillsboro, Ore., describes its approach to designing a CMOS 100-MHz microprocessor. Researchers at National Semiconductor Corp. analyze the physical operational limits of tradition-

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The SM-S and SM-L series quartz crystals are mounted in high-temperature-resistant, low-profile (0.1-in.-high) packages capable of withstanding 275°C soldering temperatures for at least 30 s without damage. Unlike conventional surface-mount packages, which are sealed by epoxy or solder preform, the new packages are resistance-welded metal enclosures mounted on a gold-plated ceramic base. The SM-S

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**Mercury United Electronics Inc.,
Rancho Cucamonga, CA; (714)
466-0427. CIRCLE 145**
■ Booth 4240

al high-speed interconnect technology for VLSI devices running at frequencies up to 500 MHz. After describing alternative techniques for minimizing crosstalk, the discussion introduces the Multilevel Microcoaxial Interconnect technology and its potential for overcoming high-frequency barriers.

The topic continues with a paper from MicroUnity Systems Engineering, Inc., Sunnyvale, Calif., which reviews the electrical characteristics of circuit interconnects for pc boards, multichip modules (MCMs), and monolithic ICs. Interconnect design for Phase II of the Department of Defense's Very High Speed Integrated Circuit (VHSIC) program and for gallium-arsenide military systems is the topic of a presentation from Raytheon Co., Marlborough, Mass. Techniques are examined for optimizing high-speed signal paths, such as the use of low-dielectric-constant materials, pressure-contact connectors, and buried resistors.

A related session examines the role of specialty memory devices in the design of high-performance systems. Presentations from Integrated Device Technology, Quality Semiconductor, and Sharp Microelectronics Technology, Camus, Wash., focus on trends in bidirectional, synchronous, and programmable-flag FIFO buffers; high-density and synchronous dual-port memories; and cache modules. The papers include detailed product features, de-

sign methodologies, application examples, and design trade-offs.

While solutions abound for achieving high speed in chip- and board-level products, an equally vital specification is electromagnetic-compatibility (EMC) requirements of domestic and international regulatory agencies. Following an overview presentation on combatting electromagnetic interference (EMI) by Dr. Michael L. Gilbert of National Semiconductor's facility in South Portland, Maine, five presentations discuss the specifics of dealing with EMI. Harris

Semiconductor, Somerville, N.J., addresses techniques for minimizing conducted EMI. These include choosing the proper digital IC process family, using effective decoupling, and selecting the proper line termination. Michael Violette of Washington Laboratories, Ltd., Gaithersburg, Md., then discusses common EMI errors and how to avoid them.

National Semiconductor also evaluates EMI noise sources in a typical laptop computer design, and presents several design recommendations. William Erickson, president of Syvax, Inc., San Jose, Calif., describes successful design techniques the company has used to comply with FCC regulations. The session closes with a paper from Chomerics, Inc., Woburn, Mass., which offers electrical and mechanical solutions for suppressing EMI.

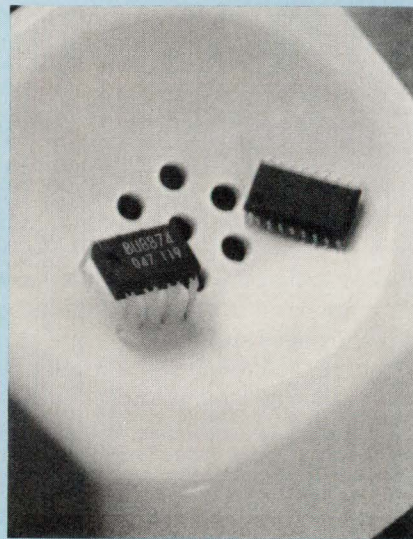
PROGRAMMABLE LOGIC

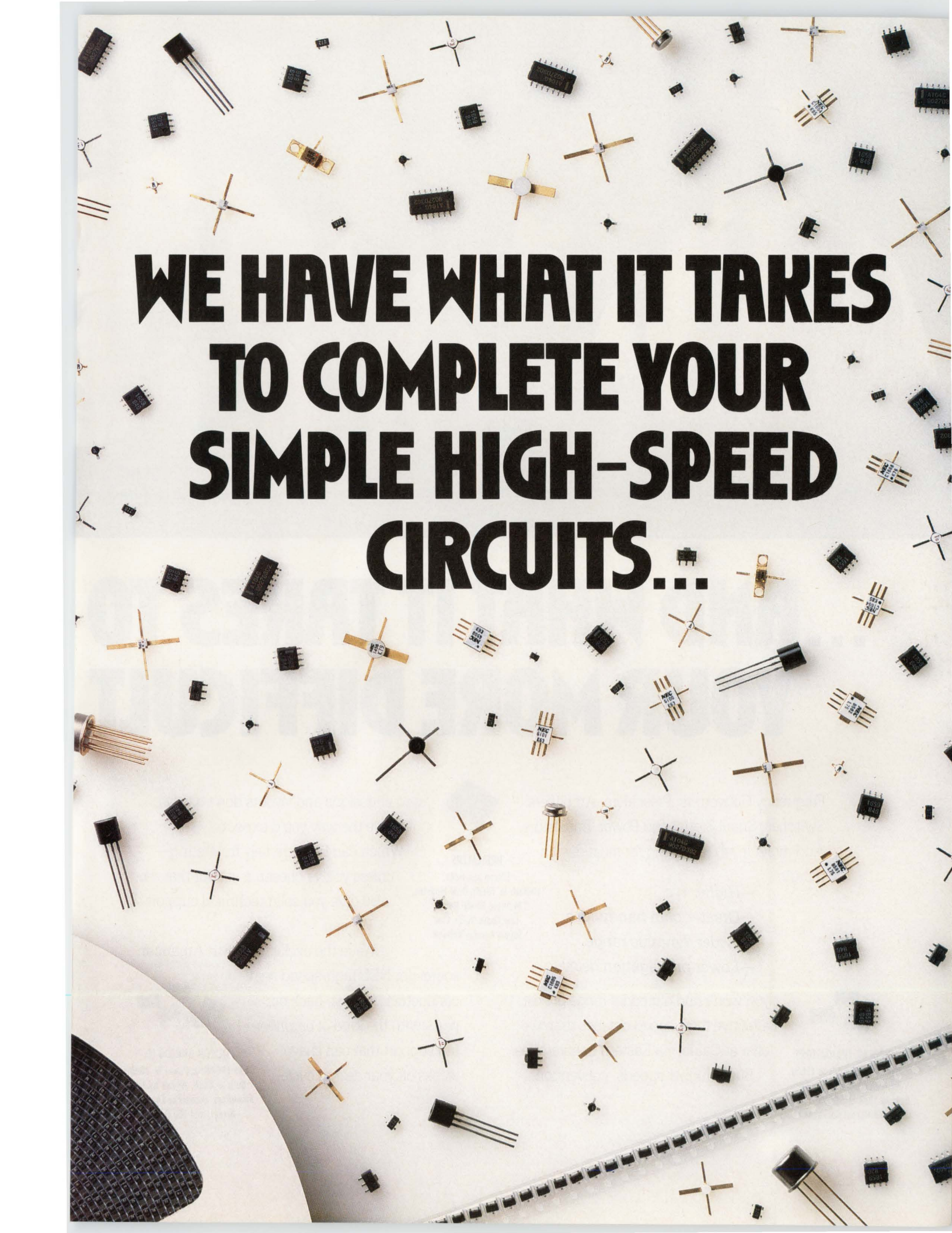
PLDs not only contribute to design efficiency and performance, but also shorten design cycles and hence, time to market. Unfortunately, the continuous introduction of new architectures and device types is outpacing the designer's ability to keep up. Attendees at four sessions on PLDs gain insight into the architec-

DTMF RECEIVER CHIP DECODES TONE SEQUENCES

Designed for telephones and answering machines, the model BU8874/8874F dual-tone multi-frequency (DTMF) receiver translates unique telephone tone sequences into a serial output for telecommunications systems. Available in 8-pin DIP and 18-pin SOIC versions, the chip operates from 5 V at 2.2 mA, and draws 0.1 mA in the standby mode. Maximum power dissipation is 500 mW in the DIP, and 550 mW in the SOIC package. The device features a 45-dB dynamic input range, a power-down mode, a serial 4-bit binary data output, and hysteresis on the ACK (Acknowledge) input pin.

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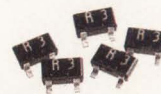
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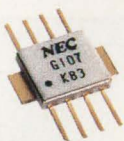
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tures, performances, and applications of the two types of PLDs—channel-based devices (FPGAs) and segmented-block-based devices (PALs, GALs, and FPLAs)—plus supporting development tools.

The first of two sessions on FPGAs open with a paper by VLSI Technology, Inc., San Jose, Calif., which reviews how next-generation devices have overcome prior limitations in performance, density, flexibility, and development-tools support. QuickLogic Corp., Santa Clara, Calif., then presents an FPGA benchmark for designers of high-speed CMOS/TTL systems. This presentation also demonstrates a surface-mount pc-board working prototype that measures clock skew, propagation delay, and maximum clock frequencies of single-chip and chip-to-chip state machines.

Using multiple circuit diagrams and performance curves, Actel Corp., Sunnyvale, demonstrates how to implement counters, adders, and state machines in FPGAs to get higher performance, shorter design time, and lower cost than PLD, gate-array, or SSI/MSI implementations. Xilinx, Inc., San Jose, Calif., ends this session by showing how its XC4000 FPGA family integrates system-level functions previously requiring external components.

A second Xilinx presentation kicks off the companion session on advanced CAE tools for FPGA design. It covers currently available tools and methodologies, and focuses on emerging trends. Another Xilinx paper in this session describes the BLOX module-generator system for aiding designers using the XC4000 FPGA family. Data I/O Corp. follows by introducing a new intelligent fitter technology for FPGAs. The Redmond, Wash., company explains FPGA fitter technology, how it differs from a PLD fitter, and how the its own ABEL-FPGA design process provides automated fitting, device-independent design, intelligent device selection, and architecture benchmarking. Following a discussion by ViewLogic Systems, Marlborough, Mass., which examines the merits of various hardware-descrip-

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Dialight Corp., Manasquan, N.J.;
(908) 223-9400. **CIRCLE 747**
■ Booth 448-450

tion languages for synthesizing and simulating FPGA designs, Mentor Graphics Corp., Wilsonville, Ore., traces the evolution of the FPGA design process.

The session on segmented-block-based PLDs opens with an overview on architectural innovations in high-density PLDs by Advanced Micro Devices, Inc., Sunnyvale, followed by National Semiconductor explaining the need to benchmark PLDs to determine performance levels, capacity, and applicability. Next, a paper from Intel advocates the use of global-architecture PLDs with complex macrocells instead of segmented-architecture PAL-type devices

for improved connectivity and deterministic timing. This paper is followed by a presentation from Altera Corp., San Jose, Calif., which introduces the MAX 7000 family of EPLDs. Included are descriptions of the architecture, macrocells, logic-array blocks, programmable-interconnect arrays, programmable speed and power control, and design support tools. This session concludes with an AMD presentation on its MACH family of high-density PLDs, which offer predictable fast delays.

The emergence of higher-density PLD architectures is accompanied by new computer-aided design tools that combine the device-independent

IC-MEMORY CARDS BOAST LITHIUM-BATTERY BACKUP

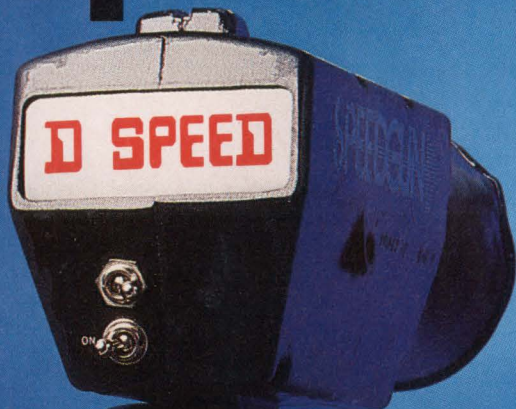
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PCMCIA standard 68-pin package configurations. Pricing for the cards is available upon request.

Panasonic Industrial Co., Secaucus, N.J.; (201) 392-6406. **CIRCLE 748**
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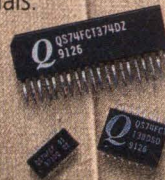
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138D (Decoder)	4.0	821D (Register)	5.3
139D (Decoder)	4.0	823D (Register)	5.3
521D (Comparator)	4.1		

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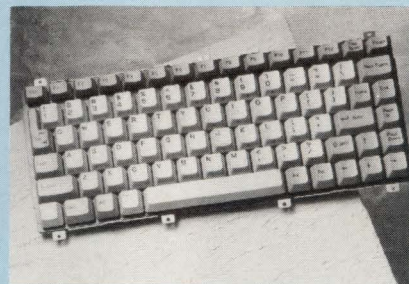
front-end design function and the back-end fitter. Four papers in a separate session cover new PLD design tools for system-level design. National Semiconductor opens this session with an overview of PLA architectures, software, device fitters, place-and-route requirements, and standardization. A presentation by Minc Inc., Colorado Springs, Colo., argues for a well-integrated design environment that includes both PLD and FPGA devices.

PLD performance is limited without the support of design tools that can fit the user's logic equations into the device. Intel software engineers continue this session with a description of two algorithms that solve this problem of product-term allocation. Their paper compares the algorithms with respect to speed and fit. Lattice Semiconductor Corp., San Jose, Calif., closes this session by comparing the architectural trade-offs between FPGAs and high-density PLDs.

Despite the present limitations of process geometry, die size, packaging, and design tools, ASIC technology continues to offer the potential of integrating a complete system on a chip. Several conference papers cover ASIC technology advances and application trends that point the way toward this goal. Mitsubishi Electronic Corp., Itami, Japan, reviews current submicron technologies for

PC KEYBOARD HAS MEMBRANE SWITCHES

The FKB7200 series keyboard has optimized size, keystroke, key layout, tactile feedback, and weight for laptop and notebook PCs. The keyboard measures 11.56 in. long, 5.05 in. wide, and 0.59 in. high, and weighs 9.0 oz. The 3.0-mm keystroke has quiet tactile feedback, a 13-to-83-mm C-row height, and a minimum operational life of 10 million keystrokes. The FKB7200 is available now for \$21 each in quantities of 5000 to 9999. Semicustom and full-custom units are also available.



Fujitsu Component of America, Inc., San Jose, CA; (408) 922-9000.

CIRCLE 750
■ Booth 0917

CMOS logic, and compares the reliability of new device structures against conventional technologies. Mitsubishi's author also describes a multilevel interconnect design for next-generation 0.5- μ m ASICs.

Hitachi America, Ltd., Brisbane, Calif., projects ASIC packaging trends for the coming decade, predicting silicon feature sizes down to 0.3 μ m, die sizes up to 25 mm per side, pinouts up to 1000 pads, and complexities approaching 1 million gates. Digital Equipment Corp., Franklin, Mass., follows by reviewing trends in ASIC design methodologies, including in-system verifica-

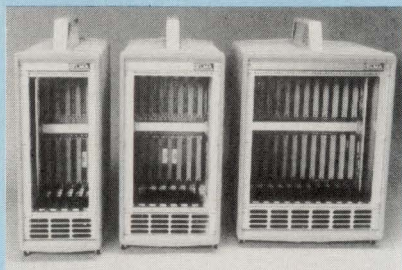
tion, logic synthesis, and design for testability. Closing the session, Compass Design Automation, San Jose, Calif., and VLSI Technology jointly discuss ASIC design-tool trends in the 90s, and projects design-tool needs for the year 2000.

Until the system-on-a-chip concept becomes a reality, MCM technology is a viable packaging option for 40-MHz-plus subsystems demanding the densest form factor. In the session on MCMs, Ross Technology, Inc., Austin, Tex., gives an excellent example of how MCM technology permits higher clock frequencies, consumes less power, has less capacitive loading, and uses less board space than a Sparc CPU chip set implemented in discrete packages. MCM design-tool requirements are outlined in a paper from the University of California at Berkeley. And nCHIP, Inc., San Jose, Calif., examines the driving forces behind MCM technology and discusses implementation specifics. The session concludes with a system manufacturer's perspective on MCMs by Sun Microsystems, Mountain View, Calif.

Systems implementation is the focus of two sessions on embedded-control technology. The first examines key issues and trends in the development and deployment of real-time and embedded systems. The opening presentation by Wind River Systems, Inc., Alameda, Calif., dis-

VME ENCLOSURES COVER MANY APPLICATIONS

System 32 enclosures are available in tower, desktop, and portable configurations for VME systems interfacing with VMEbus, VXIbus, SUNbus, Multibus II, and PC systems. The enclosures offer heights from 2U to 6U form factors and depths from 10 to 20 in. Also available are a variety of colors, backplane flexibilities (J1, J2, and J3), power supplies from 85 to 1500 W, fan modules, disk-drive holders, and cable, switching, and wiring. The tower configuration comes in 3-, 5-, 7-, and 12-slot versions. All systems are avail-



able from stock or up to two weeks starting at \$1200 each in lots of 20.

Elma Electronic Inc., Fremont, CA; (415) 656-3400. CIRCLE 749
■ Booth 347, 349

SMallTalk.

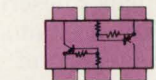
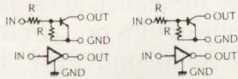


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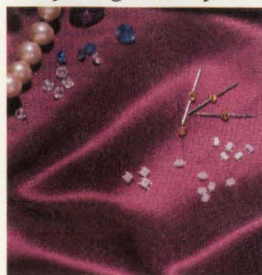
up to two transistors and four resistors. One component provides several functions, and that means lower placement cost, higher reliability, lower component count, less real estate, and reduced inventory. Standard V_{CE} ratings of 11V to 120V, and current ranges from 30mA to 100mA, are available.



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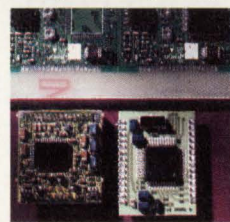
orange, yellow and green; and dual-chip types that give you combinations of colors. You can even get a three-color effect with red and green chips combined to make amber.

We offer standard brightness and high luminance, lensed LEDs packaged in SOT-23s, and lensed mini-molded styles. Brightness ranges from 555 to 660 nanometers.

They can turn product designs into gems.

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You need density? How about 50 components per square centimeter?



That's what we've achieved in our newest hybrid circuits, thanks to TAB packaging, fine pitch lead spacing, and screening resistors

and capacitors back-to-back—directly onto the substrate to improve shielding.

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Resistance range is 5.6Ω to 1.5MΩ, and power dissipation is 0.063W with a maximum 12.5V working voltage.

We're now also offering a strong line of ceramic chip capacitors with package sizes as small as 0603. (1.6mm x 0.8mm). They're offered in NPO, X7R, Z5U, and Y5V dielectrics.



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And we continue to offer innovations like multiple-function transistors, unique diode packages, surface mountable networks, and industry-leading component densities.

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The Model 9210 GPIB pulse generator accepts up to two plug-in output modules to meet a range of waveform requirements. The Model 9211 output module has a maximum repetition rate of 250 MHz, variable edge times from 1 ns to 1 ms, and a 5-V pk-pk output into 50 Ω . The Model 9212 module has a 300-MHz maximum repetition rate with edge times from 300 ps to 1 ns, and the same pk-pk output. The Model 9213 module has a 100-MHz maximum repetition rate with edges variable from 6.5 ns to 95 ms, and delivers 16 V pk-pk into 50 Ω .

The 9210 mainframe is priced at \$5900 each; the 9211, 9212, and 9213 mainframes are priced at \$1600, \$2200, and \$1000 each, respectively.

*LeCroy Corp., Chestnut Ridge
NY; (914) 425-2000. **CIRCLE 751**
■ Booth 2641-2643*



discusses the concept of integrating real-time operating systems with standard networking protocols to create a new real-time client-server topology. Real-Time Systems, Los Gatos, Calif., addresses the emergence of standards for real-time Unix kernels and Posix. And Dataquest, San Jose, Calif., discusses trends in the real-time and embedded-systems market. Issues associated with embedded-systems tools and development are examined in a presentation by Microtec Research, Inc., Santa Clara, Calif.

Microtec Research is also mentioned in a paper by Fujitsu Microelectronics, San Jose, Calif., which cites the role of Microtec's dedicated development tools in the design of Fujitsu's MB96930 32-bit Sparc-compatible RISC processor. Scheduled in the session on embedded-control devices, this presentation stresses how the customization of the Sparclite architecture for embedded controls—plus its reference development environment—ensures the availability of Sparc-compatible products for a spectrum of applications.

Embedded MIPS RISC solutions are the subject of a paper by Integrated Device Technology, which covers features and performance of IDT's RISController family, including price/performance trade-offs and application areas. An inside look

at the design methodologies used for a 100-MIPS superscalar microprocessor is offered in a presentation by National Semiconductor's facility in Israel. The Swordfish is the company's newest member of the Series NS32000/EP family of embedded system processors. The authors describe device architecture and the design environment—including details on module definition, logic, timing, and layout design.

This session also includes a paper from VLSI Technology, Tempe, Ariz., which describes the ARM RISC machine for low-cost embedded control. The session also includes a demonstration by Adaptec, Inc., Milpitas, Calif., on minimizing the workload of host microcomputers by using single-chip embedded SCSI controllers.

A separate but related session deals with trends in embedded-control memory. Xicor, Inc., Milpitas, Calif., leads the program by describing memory families suited to specific embedded-control environments, and then focuses on its recently released controller-specific EEPROM. National Semiconductor follows by describing the operation, performance, and application of nonvolatile ferroelectric memories. These devices are based on a combination of CMOS technology and a polycrystalline ceramic film of lead-zirconate-titanate (PZT).

A PROM with a cache-like architecture for embedded applications is the subject of a presentation by Cypress Semiconductor, San Jose, Calif. This paper describes how the device offers no-wait-state performance in support of high-performance microprocessors from AMD,

ROTARY SWITCH USES OPTICAL CONTACTS

The series 61 rotary encoder switch interrupts light falling on a pair of phototransistors to provide a 2-bit quadrature-coded output. The lack of metal-to-metal contacts increases switch life to a million switching cycles, compared to the 25,000 cycles of operation typical for an electromechanical rotary switch with metal-to-metal contacts. An integral pushbutton switch is provided for inputting the desired setting. Prototype quantities are available from stock to two weeks; production quantities are available two to four weeks from receipt of order for \$10.50 each in quantities of 100.

*Grayhill, Inc., LaGrange, IL; (708)
354-1040. **CIRCLE 752**
■ Booth 1241-1243*



WESCON PREVIEW

Intel, and Motorola, which feature burst-mode interfaces to memory. The session closes with a description of a monolithic device for storing analog signals by Information Storage Devices, Inc., San Jose, Calif.

Portable-computer applications and architectures also figure prominently in this year's technical program. A special session featuring panelists from PC and workstation manufacturers probes the controversy over platforms for electronic design. Representing the viewpoints of Visionics, OrCAD, Intergraph, Sun, and the EDAC Standards Committee, the panelists also discuss the role of standards in reaching maxi-

mum application performance independent of the system used.

The session on portable applications for PC-compatible chip sets examines the technical challenges inherent in memory management, power consumption, system power

management, power cycling, and interrupt handling. VLSI Technology starts off by examining the issues of high levels of integration for PCs. A second paper by VLSI Technology describes its chip set solution for power management in desktop and

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The microprocessor-based model PL 5010 tester has a resident device library covering over 90% of existing 14- to 28-pin ICs, including over 600 commonly used TTL and CMOS digital devices. Optional custom programming allows users to generate tests



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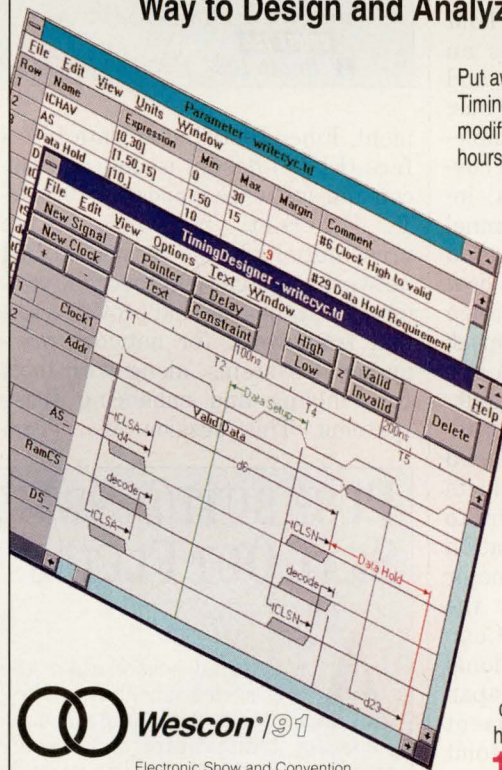
B+K, Maxtec International Corp., Chicago, IL; (312) 889-1448.

CIRCLE 753

Booth 2335, 2337

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laptop computers. Intel then describes how an architectural extension to its i386 microprocessor family eliminates the need for designers of notebook computers to trade off compatibility with power management and portable utilities.

The session continues with papers from AMD and Chips & Technology, Inc., San Jose, Calif., which discuss power-consumption considerations and system solutions for laptop and notebook designs. Battery options for portable computers are the subject a presentation by Duracell, Inc., Bethel, Conn. This paper identifies all the factors to be considered in selecting a primary or secondary battery for specific-usage profiles.

Three papers in the session on PC-bus architectures focus on developments beyond the AT bus. IBM Corp., Boca Raton, Fla., gives an overview on the architecture and features of the Micro Channel bus, discusses key Micro Channel implementations in the industry, and covers current industry activities, including those of the Micro Channel Developers Association. CompuAdd Corp., Austin, Tex., then shows how to boost AT-bus performance through AT "hot slots," and Chips & Technologies describes an ISA-bus superset that optimizes throughput.

Five papers in a related session address high-density, silicon-based memory cards for use in products ranging from palmtop computers to digital cameras and communication devices. This session covers major technical issues addressed by the standards set by the Personal Computer Memory Card International Association (PCMCIA), the Japan Electronic Industry Development Association (JEIDA), and the Joint Electron Device Engineering Council (JEDEC). These papers review the PCMCIA standard, discuss design criteria for PCMCIA cards, the features and benefits for system designers, and present and future applications.

Another technology with heightened visibility at Wescon is communication networks. This year three sessions cover Open Systems Interconnection (OSI) network manage-

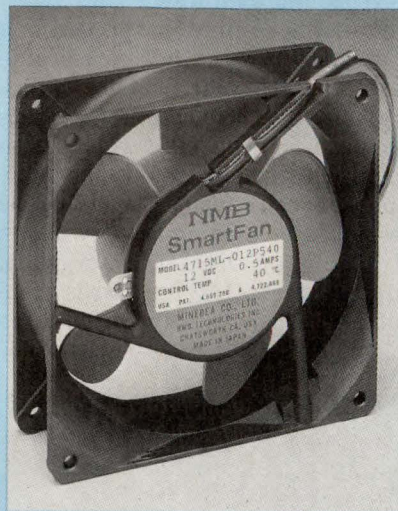
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NMB Technologies Inc., Chatsworth, CA; (818) 341-3355.

CIRCLE 754

■ Booth 1027, 1029



ment, Fiber Distributed Data Interface (FDDI) design issues, and silicon and software trends for 10Base-T Ethernet networks. Five presentations in the session on OSI network management cover the various OSI standards that provide a formal framework for network management systems, along with tools for building and enhancing these systems. This session also intro-

duces a fully OSI-compliant network management system, along with an overview of recent developments.

FDDI technology is the subject of four papers in a second networking session. Addressing FDDI networks from the perspective of both system designers and system integrators, this session includes a detailed study of FDDI architectures and capabilities, and focuses on the functionali-

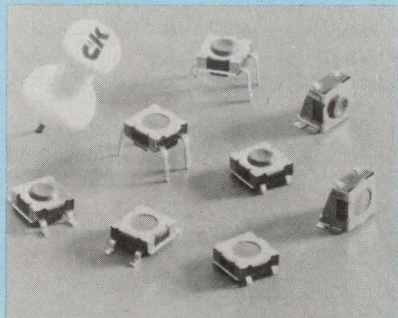
PUSHBUTTON SWITCHES SEAL OUT FLUIDS

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ery is 4 to 6 weeks from receipt of order.

*C&K Components, Inc., Newton, MA; (617) 964-6400. **CIRCLE 755***

■ Booth 1950, 1952



WESCON PREVIEW

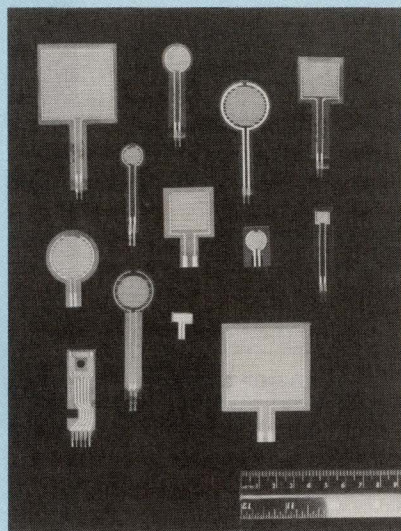
RESISTIVE SENSORS WIDEN APPLICATION RANGE

Force-sensing resistors (FSRs) convert changes in pressure into changes in resistance for such diverse products as computer-input devices, keypads, and machine-control devices. The sensors are less than 0.5-mm thick, require zero travel distance, and have a rated life exceeding 10 million switch cycles. Available in four basic configurations, the FSRs can be used individually as pressure sensors or switches, or in matrices configured as keypads with X-Y-Z functionality to translate X-Y position information, and the force (Z) applied at the indicated position.

Interlink Electronics, Carpinteria, CA; (805) 684-2100.

CIRCLE 156

■ Booth 2012



ty, architecture, and design issues related to developing concentrators, bridges, and workstations for the network. An overview of FDDI-local-area-network systems management is also included.

Five papers in the third networking session cover the evolution and development of Ethernet. Described are the latest architectures for super-hubs, bridges and management

modules, distributed and remote network management for workstation and bridges/servers, and the impact of silicon integration on desktop connectivity. □

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CIRCLE 157

■ Booth 1447



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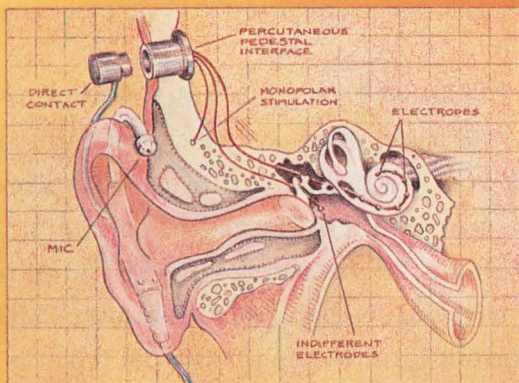
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CIRCLE 264 FOR U.S. RESPONSE
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We call it a FET Array.



She'd call it a Miracle.



Hammer. Anvil. Stirrup. Drum.
Simple names for the complex natural "hardware" that allows us to hear. If it's injured—or congenitally defective—the deafness that occurs can't always be helped by conventional hearing aid.

A cochlear implant bypasses the damage, delivering filtered and processed analog signals directly to electrodes implanted deep in the inner ear. These signals stimulate the audio nerves in a natural way, allowing—in most cases—the deaf to hear.

The variety of applications for our new *RFA120* never ceases to amaze us. But then, a linear array that combines *both* bipolar *and* JFET gain blocks can provide some pretty versatile characteristics:

RFA120 FET Array
Operating Range: $\pm 5V$ to $\pm 15V$
Input Offset Voltage: 5 mV typ.
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The RFA120 is a low power device that's ideal for signal conditioning applications. One of our favorites also takes advantage of its small size.

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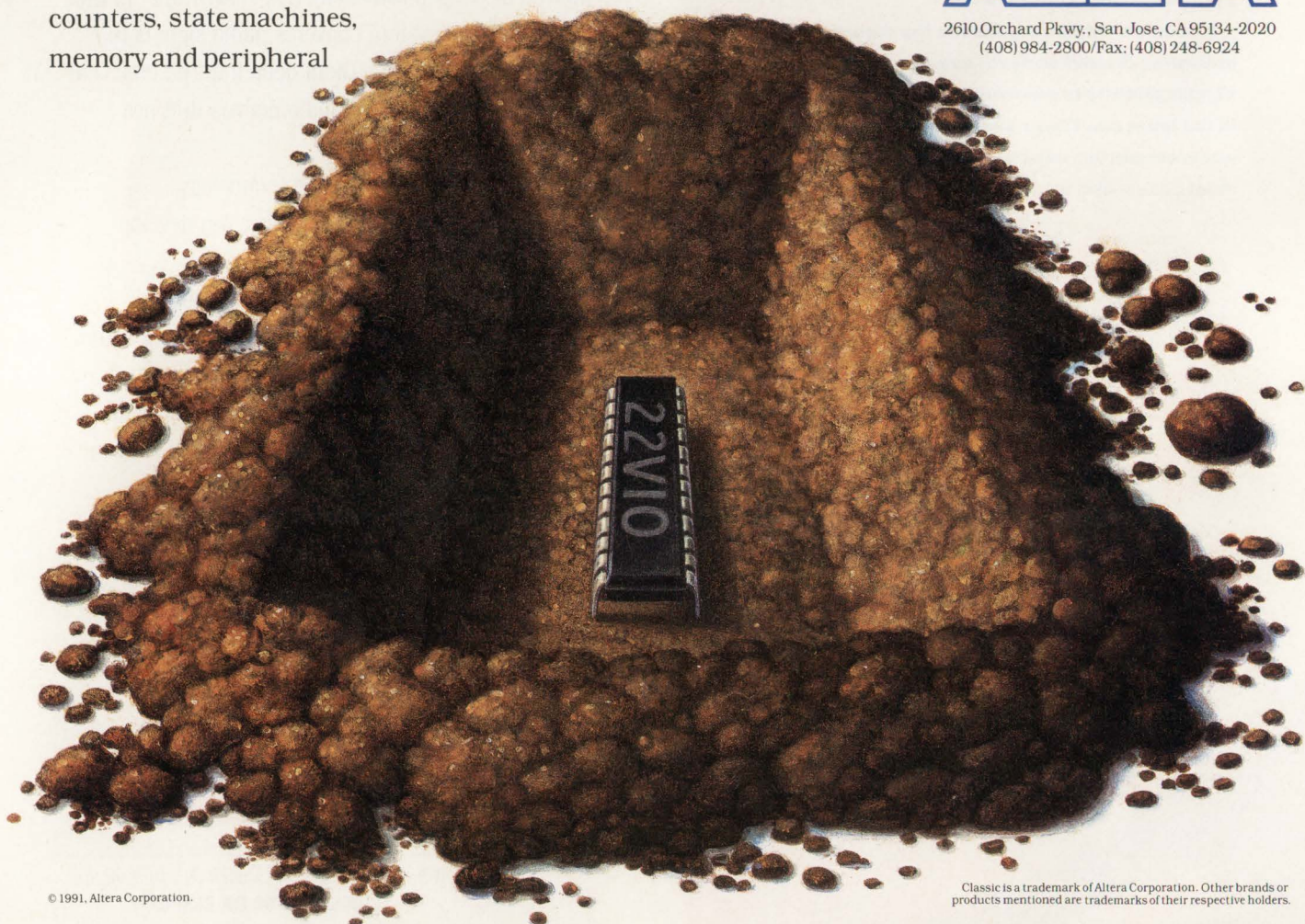
The EP610 also gives you a wide selection of low-cost Altera and third-party development tools to choose from. And a great future to look forward to—the rest of the Altera Classic™ EPLD family. Like our 68-pin, 48-macrocell, 20ns EP1810 with more density and I/O than other mid-range CMOS PLDs. And our 12ns, 20-pin EP330 that replaces over 20 kinds of PAL's and GAL's.

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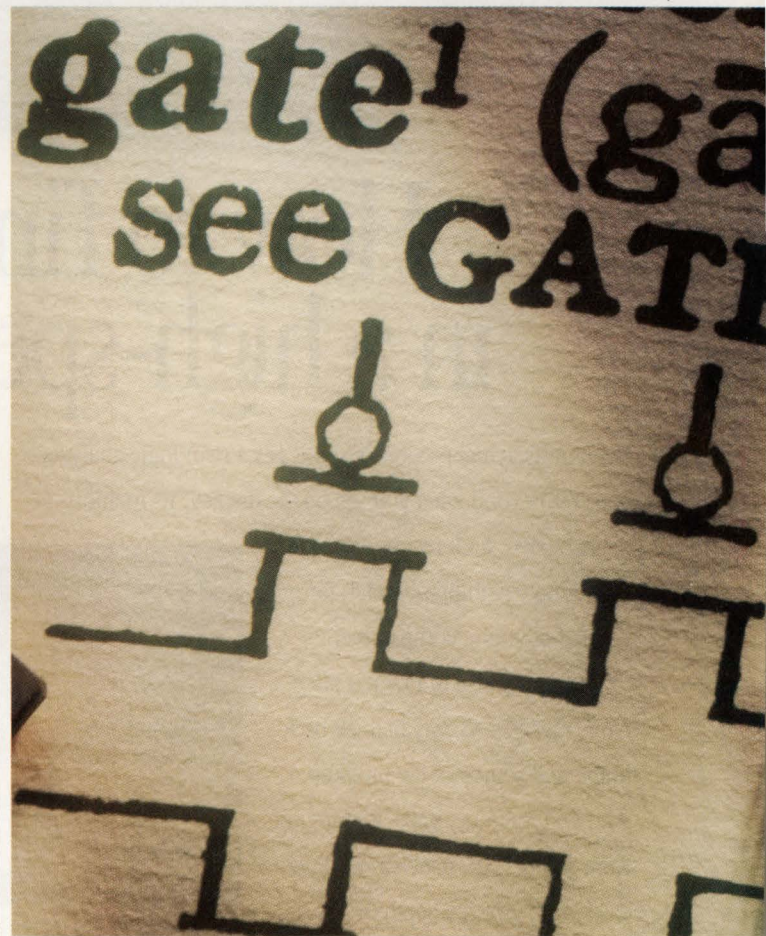
FPGAS MIRROR MASKED GATE-ARRAY ARCHITECTURE

G DAVE BURSKY

ate arrays have long been accepted as the shortest turnaround time and relatively flexible option that mask-configured semi-custom design approaches offer. At low levels of circuit complexity—several thousand gates, for example—field-programmable logic arrays have tried to dominate that market by offering turnaround times of hours rather than weeks. However, the basic logic-cell architectures of most field-programmable structures have not given designers the full range of flexibility of gate arrays, or the tens of thousands of available gates.

By combining low-impedance antifuse technology, a novel interconnection scheme, and very-small transistor-pair building blocks, Crosspoint Solutions came up with a field-programmable alternative to gate arrays. Based on a gate-array-like architecture that yields a family of six chips with densities from 2200 to 20,000 available gates, the CP20K series of field-programmable gate arrays promises designers gate-array configurability. And that flexibility comes with performance comparable to metal-configured gate arrays fabricated with 1.2-to-1.5- μm CMOS process technology.

Like some gate arrays, the CP20K series chips include many I/O pins and can efficiently implement small blocks of memory. They also permit automatic or interactive place-and-route of the logic circuitry, allowing users the ability to fine-tune performance and maximize gate utilization. The series comes with a full range of design tools that can be integrated with most design-tool suites. To aid in system testability, the chips include an IEEE 1149.1-compatible JTAG (Joint Test



Automation Group) interface. Through that interface, boundary-scan testing, as well as other tests on the chips, can be performed.

As with most medium-complexity gate arrays, each CP20K chip is organized as rows of logic cells separated by channels that contain the wiring paths (*Fig. 1*). Long rows, each composed of hundreds of cells, are diffused into the silicon with a 0.75- μm CMOS process. Above the silicon, two levels of metal inter-



How to find a needle in a high-speed haystack.

Even in its actual proportions, the Tek Prism logic analyzer goes far beyond what you see on the display. Its memory depth, speed, fault recognition and triggering capabilities stretch far beyond anything comparable.

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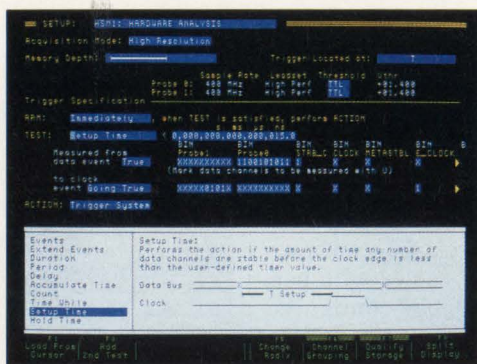
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FPGAS MIMIC GATE-ARRAY FEATURES

connection are deposited. The first level is deposited between each of the rows, into wide horizontal channels that hold many signal-routing paths and antifuse points that tie the signals to the transistors in the silicon. Above that first layer of metal is an insulating layer and more anti-

fuses, and above that is the second level of metalization, patterned in lines that are mostly at right angles to the first level of metal.

A key aspect of Crosspoint's approach are proprietary antifuses the company developed. The antifuses are very-small-area programmable

switches that have a very high impedance (1 G Ω) in their unprogrammed state, and a very low resistance (100 Ω) after programming. The fuse elements are one-time programmable, though. Consequently, some extra caution should be taken to verify a design as thoroughly as possible prior to programming a chip. Because the fuse area is very small—typically just one μm on a side, the fuses add very little capacitance—just 0.65 fF. Thus, the RC delay introduced by fuses in the signal-propagation path is very small, and the FPGAs can therefore operate at fairly high frequencies.

In some performance tests (versus other metal-gate-array and FPGA approaches), Crosspoint's approach delivered results nearly 50% faster than those estimated for such vendors as Actel and Xilinx for their respective A1280 and XC4005 FPGAs, and just slightly slower than a metal gate array from LSI Logic—the LCA 10k series (*Table 1*). (To derive the numbers for Actel, Xilinx, and LSI Logic, Crosspoint imple-

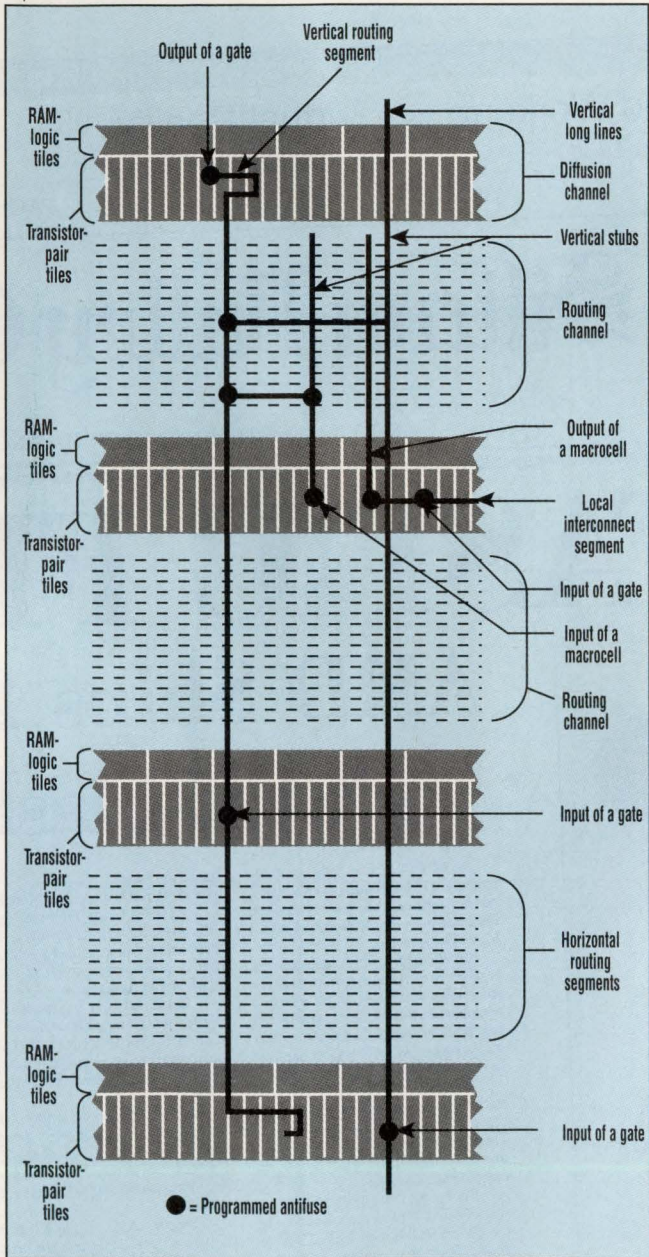
mented the designs on the respective companies' design systems to come up with the best-case numbers listed in the table.) Note that in one test where hard-wired cell structures such as latches in the I/O cell are involved, Crosspoint's results are similar to the others'.

Furthermore, in some examples in which field-programmable logic chips employ on-chip hard-wired structures, they will benchmark at speeds that are competitive with or even faster than macros created in Crosspoint's array. In general, however, Crosspoint expects its chips to operate 20 to 40% faster than most other FPGAs and within 20% of the delays possible in metal-configured sea-of-gates arrays (1.2 to 1.5 μm).

The logic-cell structures in the Crosspoint approach are actually divided into two types. In contrast, gate arrays typically have only a single cell type throughout the core area. The first cell type is a simple transistor-pair structure that's commonly used in many gate arrays. In the scheme, pairs of n- and p-channel transistors are defined as transistor-pair tiles (TPTs), and the tiles are adjacent to each other in the rows (*Fig. 2*). To isolate adjacent logic functions, the gates of one pair of transistors are reverse-biased in a manner similar to that used in some mask-programmed arrays; this approach is called gate isolation.

Located across the top of each row are the second-type cells—the RAM-logic tiles (RLTs). These cells contain enough resources to implement memory cells, latches, or multiplexers and Exclusive ORs or NORs. Each RLT has eight ports, six for input signals, one for an output, and one that's bidirectional. Four of the lines are permanently connected to the long interconnection lines to serve as the column and row controls and as the data bit. The other four lines are programmable.

A tight coupling exists within the diffusion regions between TPTs and RLTs. Local metal interconnections form the macrocells. At each two-wire intersection. When programmed, it forms a low-impedance connection between the wires, thus



1. THE HEART OF Crosspoint's field-programmable gate arrays combines an antifuse technology and a channeled array architecture. The architecture contains diffusion regions of transistor-pair tiles and RAM-logic tiles. The tiles are separated by routing channels that contain wire segments of various lengths. When programmed, the antifuses interconnect the channel wires to the tile-block transistors.

News Flash

SPORTS

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Training Equipment

PAGE 2B

SCIENCE AND TECHNOLOGY

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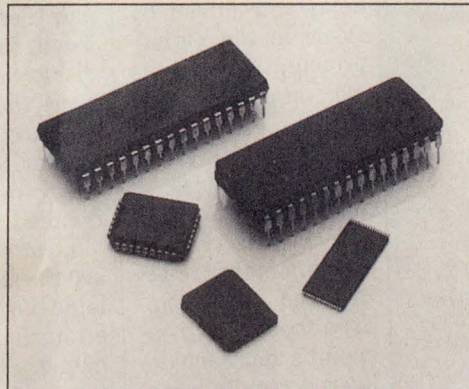
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FANTASTIC FLASH



How Fast Is A Flash? A Direct Comparison

Density	AMD	Fastest Competitor
256K	90ns	120ns
512K	90ns	120ns
1 Mbit	90ns	120ns
2 Mbit	90ns	150ns

AMD Ships 2 PLCC Flash

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications.

Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash —

hence the name.

Standard, But With A Little More Flash
AMD's Flash memory family effectively etches in silicon the de-facto standard for this burgeoning technology that is compatible with Intel's initial Flash architecture.

Because AMD Flash memories are pin-for-pin compatible with the now standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents alike.

"Alternate source may be an inadequate term," said Jerry Sanders, chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior resource."

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

Engineer Spontaneously
Combusts At Meeting

Vice Pro
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From AMD.

FOOD

Chips And Salsa

A Business Person's Guide To Silicon Valley Restaurants

PAGE 7F

ette

MORNING EDITION

ASHES!

Megabit, 90ns, Memories

The AMD Flash family offers designers and purchasers many packaging options. Particularly popular is AMD's advanced 2 Megabit, PLCC part. Other packaging options include PDIP, CDIP and LCC in 256K, 512K, 1 Mbit and 2 Mbit capacities. TSOP packages will be available in the second half of this year. (LCC not currently available in 2 Mbit.)

AMD's 2 Mbit Flash memories come complete with embedded program and erase algorithms on board. These automatic algorithms speed up the design process and considerably shorten time to market. Previously, engineers were required to develop tedious and time-consuming algorithms to implement in-system reprogrammability. AMD's automatic algorithms also allow several Flash memories to be written or erased at once, without tying-up the CPU. The system is now free to perform other tasks while these operations are in

progress. AMD plans to include embedded algorithms in a future release of its 1 Mbit part.

The Ultra-Violet Blues

Flash technology is particularly suited to applications requiring reprogramming in place, because these devices can be reprogrammed in seconds, and within the system.

To update the code on a UV EPROM, the part must first be removed from the system. Once removed, erasure can take up to a full 20 minutes. After reprogramming, the part is then plugged back into the system. The process can result in damage to other components, costly service calls, and headaches.

Flash memories, on the other hand, can be bulk erased in about one to two seconds, without system disassembly. Reprogramming can then be accomplished via floppy disk, over phone lines, or even ISDN
(continued)

Stop the presses!

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ident To Speak
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FPGAS MIMIC GATE-ARRAY FEATURES

configuring the macrocells.

The TPTs give the CP20K series the equivalent granularity of gate arrays. They also yield an identical macrocell library, permitting a simple transition for designers already familiar with gate-array cell libraries. Circuits implemented with metal-configured gate arrays can easily be mapped into the Crosspoint cell library, or vice-versa, making the FPGAs ideal candidates for prototyping standard gate-array designs.

To make the implementation of memory cells more efficient, the RLT blocks contain the right amount of logic resource so that small memory structures such as static RAMs, register stacks, and FIFO registers, can be created. To create a block of memory, the RLTs are interconnected using a network of row, column, and read/write control signal lines. The lengths of the row and column lines were preselected such that two separate RAMs can be implemented on each array. When RLTs are used as memory bits, the adjacent TPTs are still available for logic; they're not used by the memory function.

Although the arrays in the family pack from 2200 to over 20,000 gates, on average the gate utilization will hit between 60 and 80% when the

TABLE 1: CP20K FAMILY MEMBERS

Model	Available gates	Usable gates	I/O pads	Power pads
CP20220	2245	1300-1800	91	42
CP20420	4245	2500-3400	130	60
CP20840	8421	5100-6700	180	90
CP21200	12,125	7200-9700	219	100
CP21600	16,171	9600-13,000	250	110
CP22000	20,260	12,000-16,200	270	125

company's automatic placement and routing tools are employed. Additional interactive placement-and-routing tools permit designers to tweak various aspects to fine-tune critical speed paths and optimize gate utilization. In addition to the logic gates, the chips pack from 91 to 270 I/O pads, plus an additional 42 to 125 power pads. The exact combination of gates and I/O pads for each chip is summed up in *Table 2*.

Each I/O pad can be configured as either an input, output, or bidirectional signal line. The I/O circuitry can implement CMOS or TTL thresholds with or without pullups, and eight of the inputs also include Schmitt-trigger capability. The output drive for each line is also programmable—4, 8, or 12 mA can be selected, as well as the slew rate and whether the line has a normal output or open-drain or open-source connections.

In the higher gate-count chips,

clock distribution becomes a significant issue. To deal with it, designers at Crosspoint included four independent clock trees that will ease the distribution problem and keep signal skew to less than 1 ns. Four pin locations on each chip are designated at clock inputs. The

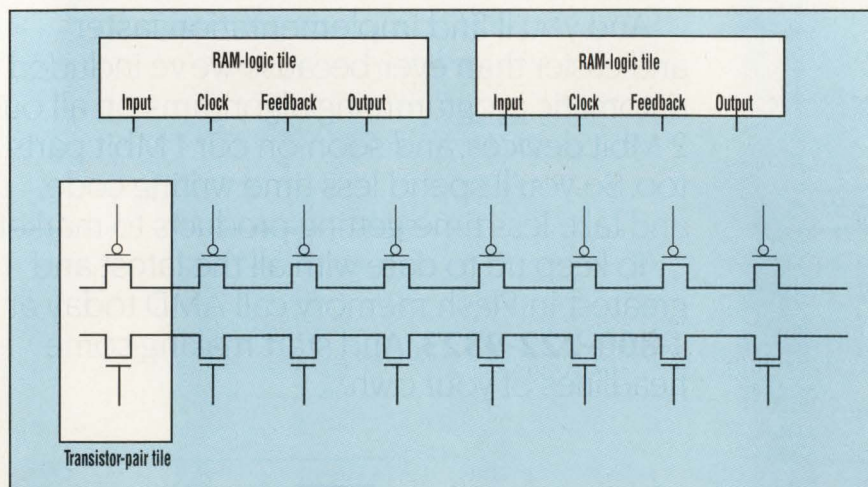
trees can get their inputs from internal or external sources, and unused clock pins can be used as standard input lines (with Schmitt inputs) if not needed for clock inputs.

Although some connections between cells are done inside the diffusion channels, the majority are made using the wiring in the routing channels. These channels hold wire segments of various lengths that appear to be floating (programming elements are actually placed at each end of the segment). A channel-segment length ranges from eight TPTs minimum, to the entire length of the row of tiles. The number of segments per length is determined by a statistical analysis of gate-array connectivity.

On the level above the routing channels, the second level of metal interconnection resources run perpendicular to the channel wires. The vertical wires are divided into three wire types:

1. Vertical-routing segments: wires that originate from a TPT and span five TPTs horizontally, and then go vertically up or down four rows and span five more TPTs horizontally before they end.
2. Vertical stubs: lines that originate at a p-channel gate in a transistor-pair cell or at one of the four RLT programmable ports. They span the length of the routing channel.
3. Long lines: wires that extend the entire distance, or 1/2, 1/3, or 2/3 the distance of the array height. These are typically used to make long vertical connections.

At each intersection of a vertical line and a horizontal line in the routing channel is an antifuse. Although that creates a large number of antifuse sites in an array—the 4200-gate chip contains 470,000 antifuses—only about 4% of the fuses are actual-



2. TRANSISTOR PAIRS arranged in long rows form the basic building blocks for all logic inside the CP20K family of FPGAs. A transistor-pair tile is formed from one n- and one p-channel transistor. Above the row of transistor pairs are the RAM-logic tiles, which contain sufficient resources to implement memory cells, multiplexers, Exclusive-ORs or NORs, or other functions.

FPGAS MIMIC GATE-ARRAY FEATURES

ly programmed for any configuration and thus detract only slightly from the chip's performance.

Testing the antifuses or, for that matter the logic implemented on the chip, could be a difficult job, especially as the gate counts climb over several thousand on a chip. To make this task easier, a JTAG-compliant test port and controller were embedded on each of the arrays. The test port, in addition to being used to test the part, is also used by the programmer as the entry method loading in the configuration pattern.

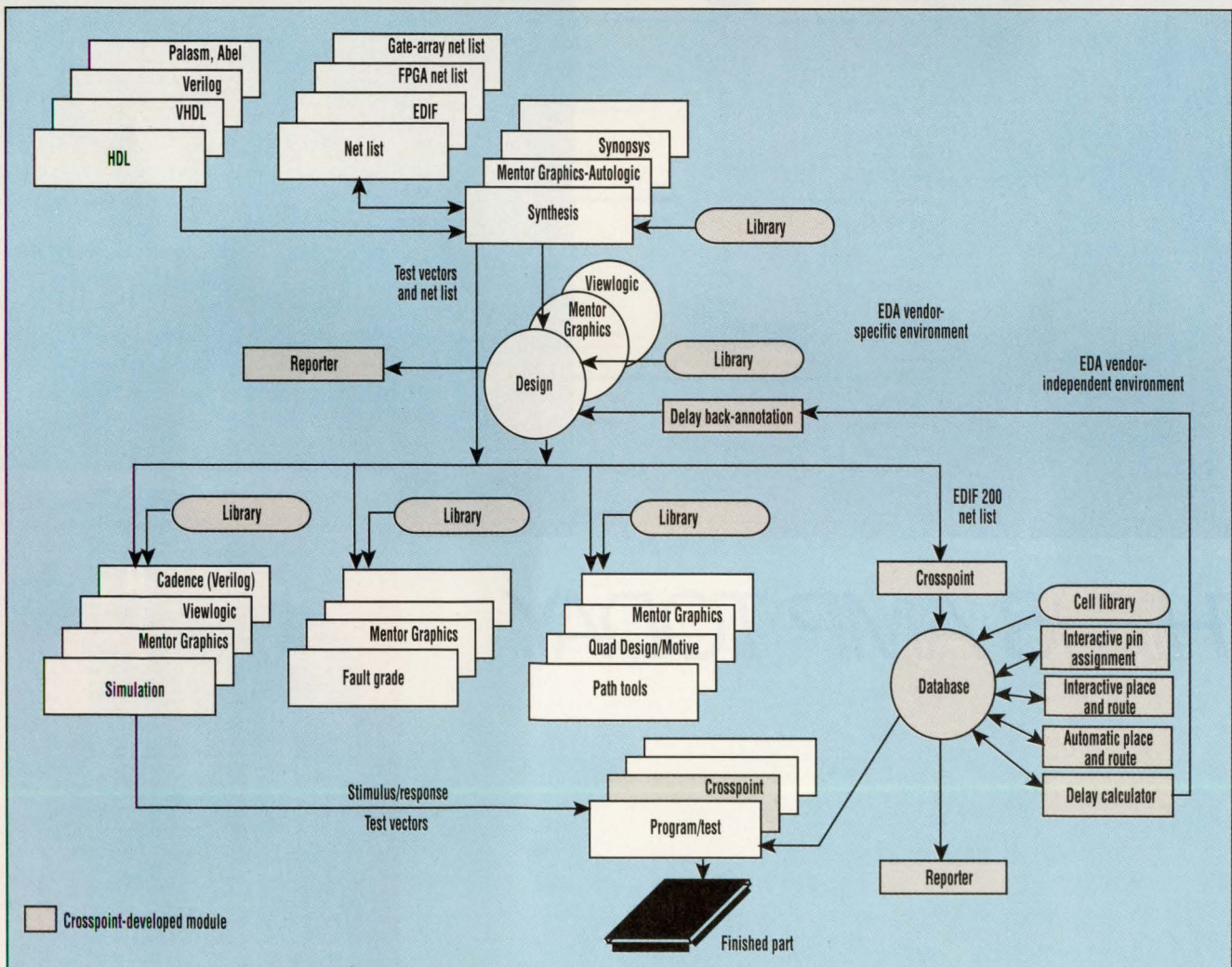
In addition to the basic functionality defined in the standard for a JTAG port, Crosspoint added some optional features, including a device-identi-

fication register, a 32-bit configurable user register, and three-stage scan capabilities. An additional test register was also included to enable users to enter in a proprietary scan chain for built-in self-test functions, or perform data-scan operations for further testing of the chip.

To configure the chips, circuit development mimics that of a gate array until the final patterning stage. And to do the development with a minimum of effort, Crosspoint created a suite of development tools that run under an X-windows Motif interface and can readily tie into many established tools and frameworks, such as those from Mentor, Viewlogic, Synopsys, and Cadence. These

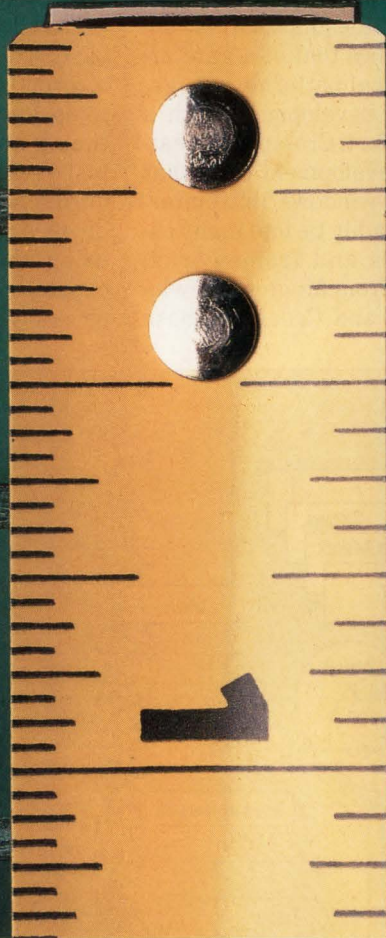
tools include a library of several hundred macrocells, automatic and interactive place-and-route routines, a delay calculator with back annotation, an EDIF file reader, a pin and package editor, a fuse-map translator and device programmer, and several design kits.

Each tool ties into the central database, which can also be used to feed information to additional third-party tools for simulation, fault analysis, timing analysis, logic synthesis and test-vector creation (Fig. 3). A standard schematic-capture program can be used to enter the design. Then by using the EDIF netlist-translation capability, the circuit representation enters the database.

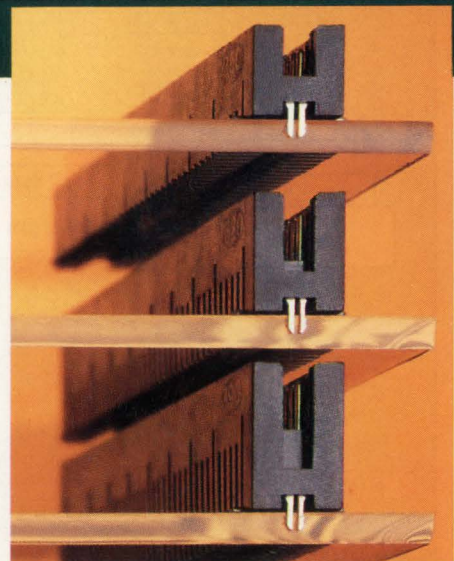


3. CIRCUIT DESIGN with the Crosspoint arrays includes a suite of design tools that might commonly be seen in most mask-programmed gate-array design examples. The shaded regions represent the library and tools developed by the company. These can be merged into synthesis, schematic-capture, simulation, fault-analysis software, or even framework tools from third-party companies.

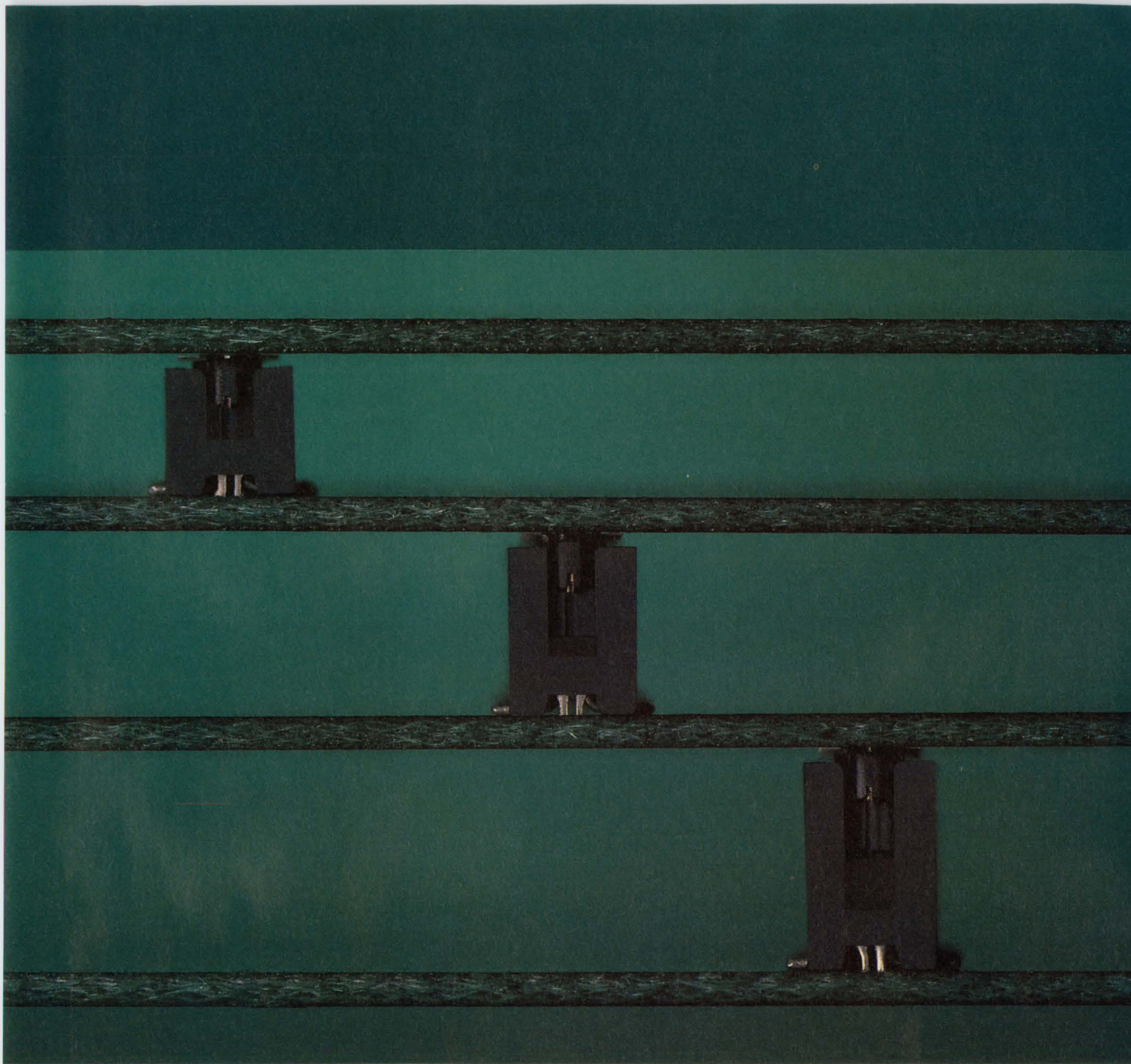
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TABLE 2: TYPICAL BENCHMARK COMPARISONS

Logic test (1)	Actel	Crosspoint	LSI Logic	Xilinx
NAND2	25.4 ns	12.0 ns	9.8 ns	22.7 ns
D flip-flop (clock to Q)(2)	19.9 ns	16.0 ns	10.0 ns	14.5 ns
5-level combinatorial (2 multiplexers and 3 gates)	70.0 ns	33.0 ns	21.4 ns	58.0 ns (3)
5-level clocked logic (2 registers and 3 gates in between)	32.1 MHz	52.0 MHz	93.2 MHz	42.4 MHz

Notes:

1. Measurements include input and output buffer delays, use logic in the core of the array, and assume a 50-pF load on the output.
2. For Actel and Crosspoint, the D-latch used was in the I/O logic; with Xilinx, the D flip-flop was in the I/O buffer.
3. Xilinx claims they can achieve 29 n² for this logic configuration.

The system-user interface permits multiple windows within the X-window environment and accepts data via popup menus and dialog boxes. Software even permits multilevel undo operations to backtrack during the design. A key area that company designers focussed on is automatic placement and routing. The program they developed includes several placement and routing algorithms to

maximize efficiency and minimize manual effort at the final stages.

For instance, the placement portion starts with a fast-placement algorithm that performs successive quadratic programming to do a first-level placement. Next, (or alternatively), a placement algorithm based on simulated annealing, is applied. Finally, a placement mapper using a maximal independent set algorithm

does the final placements. Once the placements are done, the routing portion first employs a fast global router that does trunk routing. Next a better router performs course-maze routing. Finally, a detailed router does the legal, fuse-level maze-routing. □

PRICE AND AVAILABILITY

Samples of the 4.2-kgate chip in the CP20K family are available in January, 1992, and samples of the other chips are slated for release throughout 1992. Price for the 4.2-kgate chip is \$277.70 in 100-unit quantities. It will come in a 155-lead ceramic pin-grid array or a 160-lead ceramic quad-sided flat package.

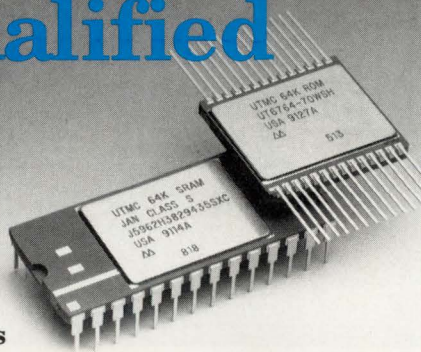
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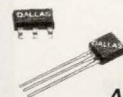
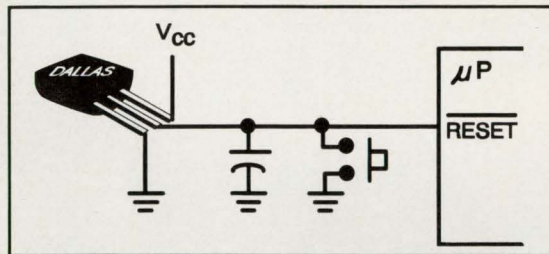
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Watchdog Timer		<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Nonvolatize RAM				<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Write Protect Memory				<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
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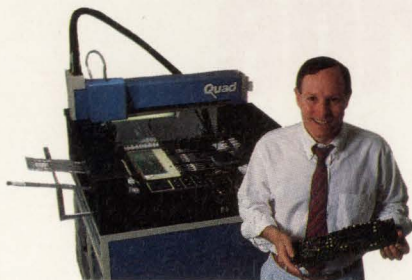
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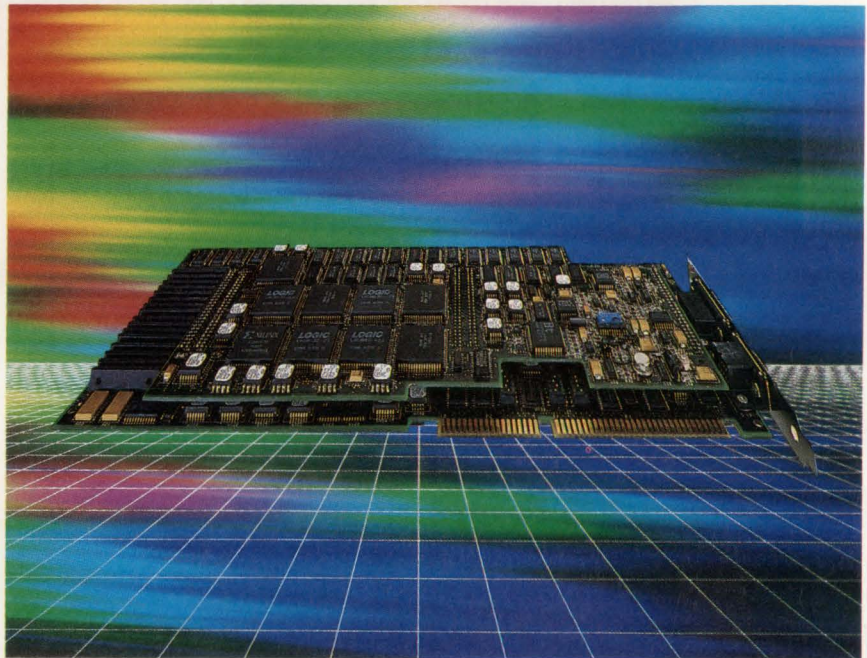
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CIRCLE 146 FOR U.S. RESPONSE

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WHEN THE MAIN-MEMORY CACHE IN
UNIX SERVERS IS SUPPLEMENTED
WITH AN I/O CACHE, SYSTEM THROUGHPUT
AND EFFICIENCY GO UP.

CUT I/O TRANSFER DELAYS BY ADDING AN I/O CACHE

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Workgroup servers—typically perceived as network computer resources—are systems that must be readily available to handle tasks upon the requests of clients. Designing such servers requires a thorough knowledge of the needs of network clients; however, all servers should be able to support multiple large processes with fast context switching. Typical server tasks include computation-intensive jobs, file storage and backup, communication protocol processing, and network link management.

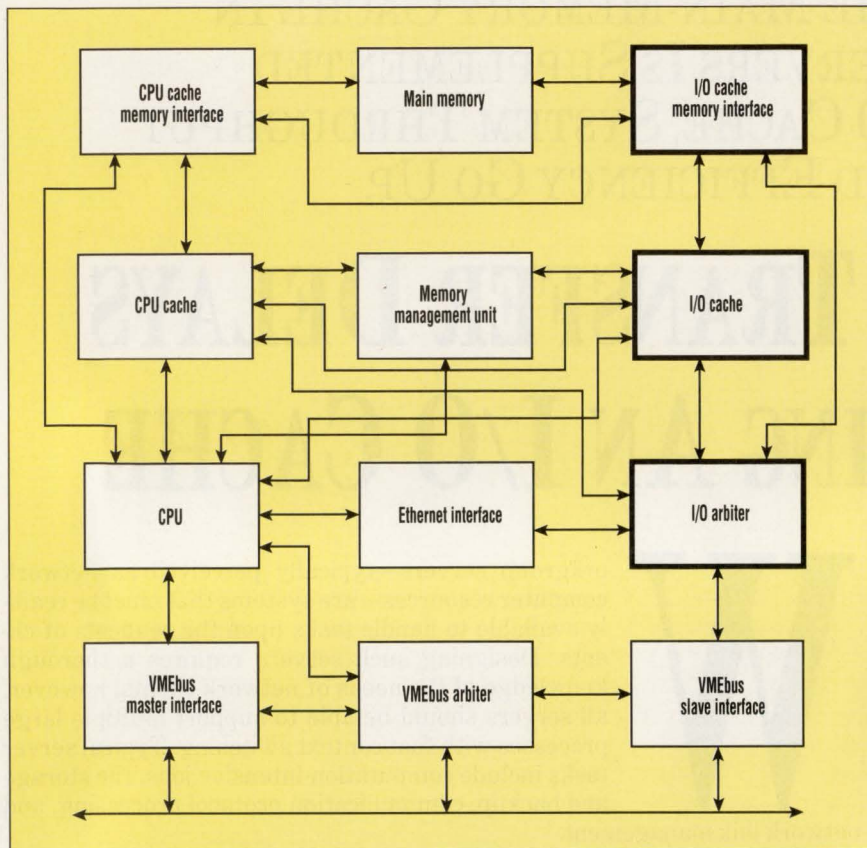
A general-purpose workstation often possesses some, though not all, of the attributes needed for a server—a high-performance RISC CPU, fast floating-point hardware, high throughput networking capabilities, and high bandwidth for system I/O. Although a server can be “derived” by souping up a workstation with larger disk drives, a more powerful system can be created by designing a server from the ground up.

One of the goals of server design is improving CPU performance while achieving a balanced I/O bandwidth. One way to accomplish this is to add a virtual-address I/O cache to the CPU board—an approach employed by Sun Microsystems in its 33-MHz SPARCserver 490. The use of a cache-based I/O subsystem reduces CPU cache interference and offloads the burden on the CPU caused by random system-I/O operations. I/O caching also increases system memory-access efficiency and minimizes memory latencies for I/O transactions.

The use of cache memory, of course, isn't new. However, it has traditionally been applied only to the main CPU processing requirements. Devoting a virtual-address I/O cache to I/O activities creates a separate speed-matching buffer for the I/O devices. It also reduces the frequency of address translation and main-memory access due to the nature of the write-back algorithm. Furthermore, a dedicated I/O cache minimizes CPU cache interference, because the CPU cache is only accessed when a data consistency check must be done. The I/O cache thus offloads the burden from the CPU, since the I/O data movement experiencing an I/O cache hit will not disturb the CPU's operation.

The System Performance Evaluation Cooperative (SPEC) has developed a number of benchmark suites that effectively measure a computing system's performance. SPEC's test suites, however, do not have benchmarks for evaluating I/O bandwidth and combined performance between CPU and I/O. To fill that gap, Sun has developed a set of benchmark programs it uses internally (See *Benchmarking I/O Performance*, p. 82). A combination of SPEC

I/O CACHING FOR HIGH THROUGHPUT



1. THE ADDITION OF AN I/O CACHE that shares the main memory and CPU of a RISC-based server improves system response to I/O devices. Thus a server can respond faster to devices tied into its system bus, i.e., the VMEbus, or to local resources such as its Ethernet interface and the CPU. The I/O cache serves as a data buffer between the main memory and I/O devices, with a dedicated data path between the I/O devices the I/O cache.

benchmarks and Sun's I/O benchmarks were then run across three generations of RISC-based hardware to show how performance changes as the system architecture evolves (*Tables 1A and 1B*).

The SPECmarks, both integer and floating point, demonstrate the linear scalability of the system architecture. However, the I/O bandwidth figures for three generations do not follow the same linear curve—just the CPU computational power of the three server generations scales linearly with the system clock speed. It is the cache-based I/O subsystem that scales the I/O bandwidth of system C by two-fold, compared to that of the earlier implementations.

The addition of an I/O cache to a server's CPU board is relatively simple. The board's main memory and

the memory-management unit are shared between the I/O devices—such as the VMEbus interface control logic for peripherals and an Ethernet interface—and the CPU (*Fig. 1*). The CPU is buffered by its own cache, which provides a dedicated data path. An I/O cache serves as a data buffer between the main memory and I/O devices, providing a dedicated data path between the I/O devices and the main memory.

Both the CPU cache and the I/O cache are accessed and tagged with virtual addresses. The main difference is that the CPU cache executes a write-back-with-write-allocation algorithm, while the I/O cache implements a write-back-with-no-write-allocation algorithm.

Handshake protocols between the CPU cache and the I/O cache maintain data consistency between the

CPU cache, the I/O cache, and main memory. Arbitration schemes are also implemented for address translation services by the MMU as well as main memory accesses.

Separating the system I/O operations from the system memory interface allows CPU designers extra degrees of freedom. As a result, they can optimize the memory interface and thus improve memory-access efficiency, resulting in better overall system performance.

In low-cost systems, system memory often resides on the same bus with system I/O devices and the CPU. In such a configuration, CPU memory accesses are often stalled when system I/O transfers to and from main memory are in progress. This I/O interference is usually a result of the speed mismatches between the I/O devices and the host CPU—most I/O device transfer rates cannot match the speed of the CPU when accessing memory.

For example, a recently released VMEbus-based IPI-2 disk controller can only transfer data at 6 Mbytes/s over the VMEbus, while a RISC CPU chip running at 33 MHz can access an off-chip cache at a rate equivalent to a 120 Mbyte/s peak bus bandwidth. Furthermore, most asynchronous I/O bus protocols, such as used on the VMEbus, are less than optimum for operations between the CPU and memory. By separating the data path for I/O devices from that of the CPU, it is possible to define and construct a more efficient memory interface protocol.

The protocol gets its efficiency by reducing the overhead involved in the handshake, which can be accomplished in three steps. First, both the CPU cache and I/O cache should execute a write-back policy. The memory interface can thus optimize burst data transfers. Second, the memory interface is defined as synchronous, so that it can run at the same speed as the rest of the system. And third, the interface is widened to reduce the number of cycles needed to transfer a data burst, without incurring an unreasonable cost on the system.

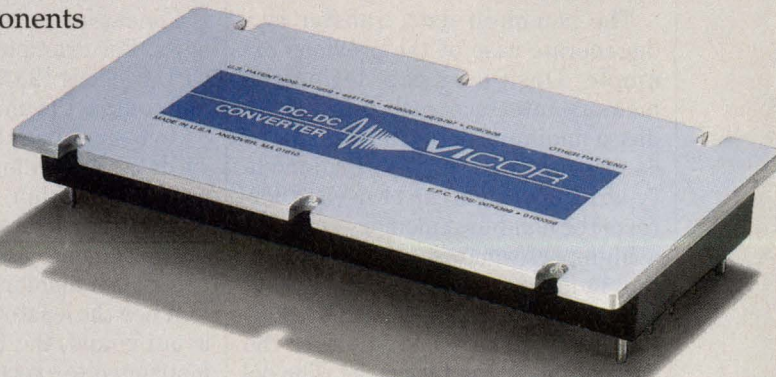
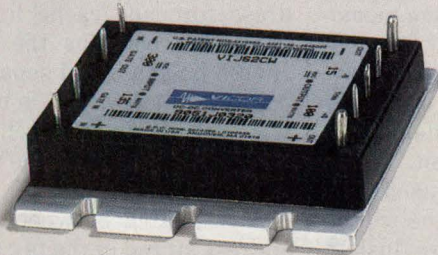
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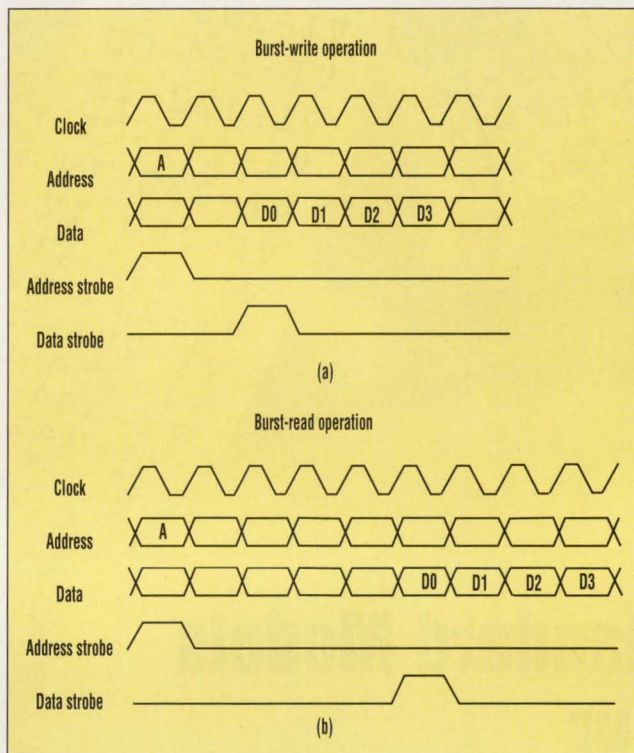
CIRCLE 287 FOR RESPONSE OUTSIDE THE U.S.

I/O CACHING FOR HIGH THROUGHPUT

bits, one possible synchronous protocol that imposes minimal overheads works well if the size of the burst data transfer matches the size of the data line in the CPU cache (Fig. 2). Just six cycles on the bus are needed for a 32-byte burst write—about equivalent to a 177-Mbyte/s peak bus bandwidth (with a 33-MHz clock). In addition, the memory interface can be designed to buffer the burst-write data transfer to free up the interface for other activity. It can then execute the actual memory write in the background.

The burst-read protocol can be similar to that for the burst write. The memory read, however, is a process synchronous to the host-system operation itself. It cannot be pushed into the background, as with the burst-write operation. Besides, the error-correction or parity-check process should take place before the data from memory can be shipped back to the accessing destination. The interface protocol cannot reduce the effect of these sequential events. However, the system design could include cache-read-miss prefetch and wrapped-around reads, to boost the overall memory-read efficiency.

The non-burst data transfer is a degenerate case of the previous example. Designers can define the memory interface such that it handles a minimum data transfer size of 64 bits per transfer. The read-modify-write operation can be used to perform the non-burst memory write. In a high-performance server system, the non-burst memory read/write operations should be limited to those that cannot be cached in either the CPU cache or the I/O cache. The occurrence of non-burst memory operations is very rare and is controlled by the system software. In fact, the overall system performance degradation due to the non-burst memory



2. FOR A SYNCHRONOUS protocol in which the memory-interface width is 64 bits, the size of the burst data transfer should match the size of the data line in the CPU cache. Also, the memory interface can be designed to buffer the burst-write data transfer to free up the interface for other activity (a). The burst-read protocol can be similar to that for the burst write (b).

access is invisible in practice.

The architecture of a virtual address I/O cache is slightly different from that of the CPU cache. The CPU cache is a high-speed linear storage device intended to match the CPU's access speed, and its content is a linear image of the system memory's. For example, if the size of the CPU cache is 128 kbytes, it can literally contain the image of 16 pages (at 8 kbytes per page) of system-memory data. According to the demand-paging algorithm, the least-recently-used page will be swapped out of the system memory when a demanded page is not memory-resident.

When the least-recently-used page is out-bound, the CPU cache will be instructed to execute a page flush to maintain data consistency between the CPU cache and main memory. During a page flush, the CPU cache must write-back and invalidate every cache line in the out-bound page.

If the entire out-bound page is CPU cache-resident, the page flush could induce a page's worth of address translation and main-memory access operations.

In contrast, an I/O cache is a page cache. Since I/O data movement tends to be sequential memory access, the most-recently-used hardware resource can be reused for subsequent data transfers, as long as no two I/O devices can be mapped onto the same virtual address page. In other words, data movement to and from each individual I/O device—data transfers with the address in the same virtual page—can use the same data-line entry in the I/O cache. (For more on cache trade-offs, see "Cache Design Trade-offs," p. 88).

This optimization of hardware resources has several advantages for designers:

- It simplifies cache-entry replacement management and reduces the cost of the hardware implementation.

- It ensures automatic I/O

cache write-back on cache-entry replacement, and eliminates the difficulty in handling scattered, partially-modified cache entries.

- It minimizes the complexity of the page flush, since there will only be one data line entry per page in the I/O cache.

For an I/O cache that executes the write-back-without-write-allocation policy, the status of the virtual address for each cache line and the page that contains the cache line should be examined separately (Tables 2A and 2B). This is because the I/O cache is a page cache that contains only one data line's worth of data buffer per page.

A mismatch between the virtual address stored in the tag and that of the indexing address does not constitute a cache-miss condition if the I/O cache encounters a cache-write operation. In this case, if the page was previously accessed, then the trans-



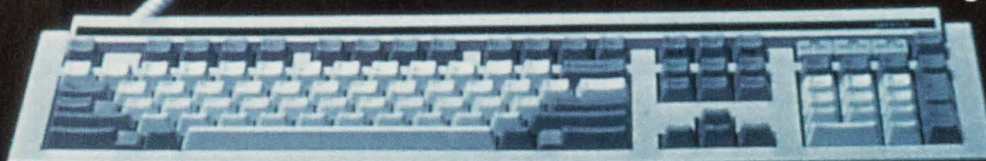
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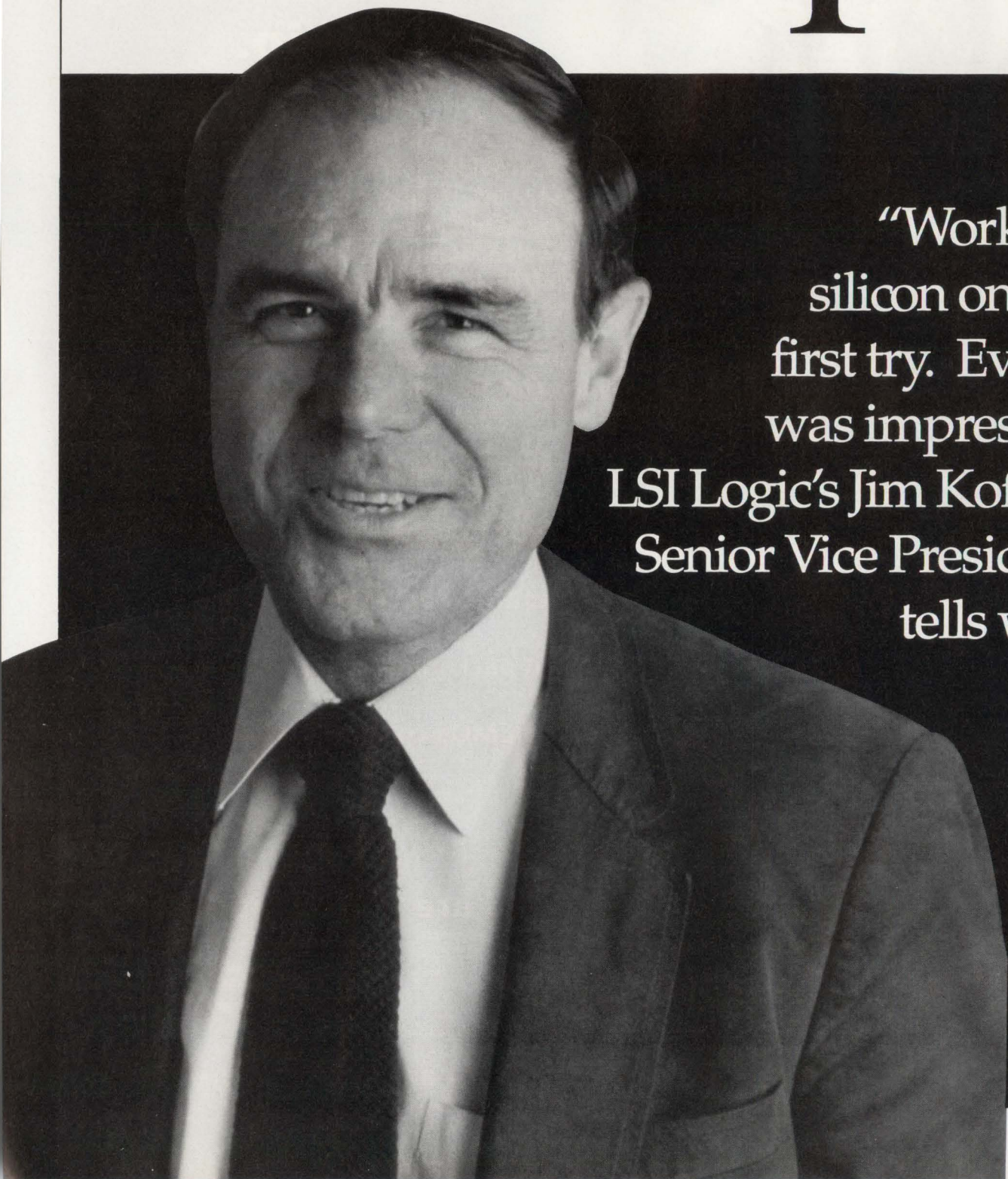
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I/O CACHING FOR HIGH THROUGHPUT

lation of the virtual page number to the physical page number can be skipped. Otherwise, the translation must occur to ensure that the page mapping is valid. In the case of an I/O cache read, this virtual page number reference does not apply, because a memory-read operation requires a reference to the physical page number.

The cache line status can be marked with the valid and modified bits. The valid bit represents the validity of the page mapping in both the I/O cache read and write operations. The modified bit should only be used in the I/O cache write operation, and should be ignored in the read operation. The attribute of the virtual page number is marked with the "cachable" bit, which indicates if the virtual page has been mapped as cachable in the I/O cache.

A walk through a

TABLE 1A: SYSTEM HARDWARE COMPARISON

Hardware	System A	System B	System C
Clock speed	16.7 MHz	25 MHz	33 MHz
Cycle time	60 ns	40 ns	30 ns
CPU cache	128 kbytes	128 kbytes	128 kbytes
	Direct-mapped	Direct-mapped	Direct-mapped
	16 bytes/line	16 bytes/line	32 bytes/line
	Virtual	Virtual	Virtual
	Write-back	Write-through	Write-back
System bus	VME	VME	VME
I/O cache	N/A	N/A	4 kbytes
			Direct-mapped
			32 bytes/line
			Virtual
			Write-back
System I/O	Via CPU cache	Not via CPU cache	Via I/O cache
	Consistent	Consistent	Consistent
HW contexts	8	16	64

TABLE 1B: COMPARISON OF BENCHMARK RESULTS

Benchmark	System A	System B	System C	Remarks
Integer SPEC	8.7	12.2	19.4	Geometric mean
FP SPEC	7.8	10.6	15.8	Geometric mean
VME bandwidth (MBytes/s)	4.48	4.51	10.62	Disk read
VME bandwidth (MBytes/s)	4.52	3.94	6.55	Disk write
TP1 throughput	26	34	51	@ 40 processes
Multuser rating	71	74	114	# users
RTE response (sec)	1300	800	200	@ 64 users

BENCHMARKING I/O PERFORMANCE

Although the SPEC consortium has many benchmarking suites for compute-oriented workstations, the suites don't measure the efficiency of the I/O portion of the system. To make such measurements special benchmarks can be developed. One such benchmark routine measures the system I/O bandwidth by setting up one file (10 million bytes) on each system disk drive. Each disk is then hooked up to a different disk controller. The program then initiates simultaneous sequential raw disk reads or writes using 63 kbytes as the data transfer size. In the case of Sun products, the system bus in the servers under

test is the VMEbus and the measured system I/O bandwidth reflects the sustaining bandwidth realized through the VMEbus.

Another benchmark, known as the TP1 benchmark, is a multi-user on-line transaction processing test that uses the Sybase SQLserver Release 4.0 EBF to simulate retail banking transactions. The outcome of the test measures a relational data-base management system's ability to support large numbers of update-intensive and commit-intensive transactions.

Multi-user performance is benchmarked using a program called AIM III, which simulates multiple users in a time-sharing

environment by generating realistic levels of CPU, I/O, and context-switching activity. It measures system performance under a load of multiple processes and indicates the number of users that can be supported by the system while maintaining a standard level of system throughput.

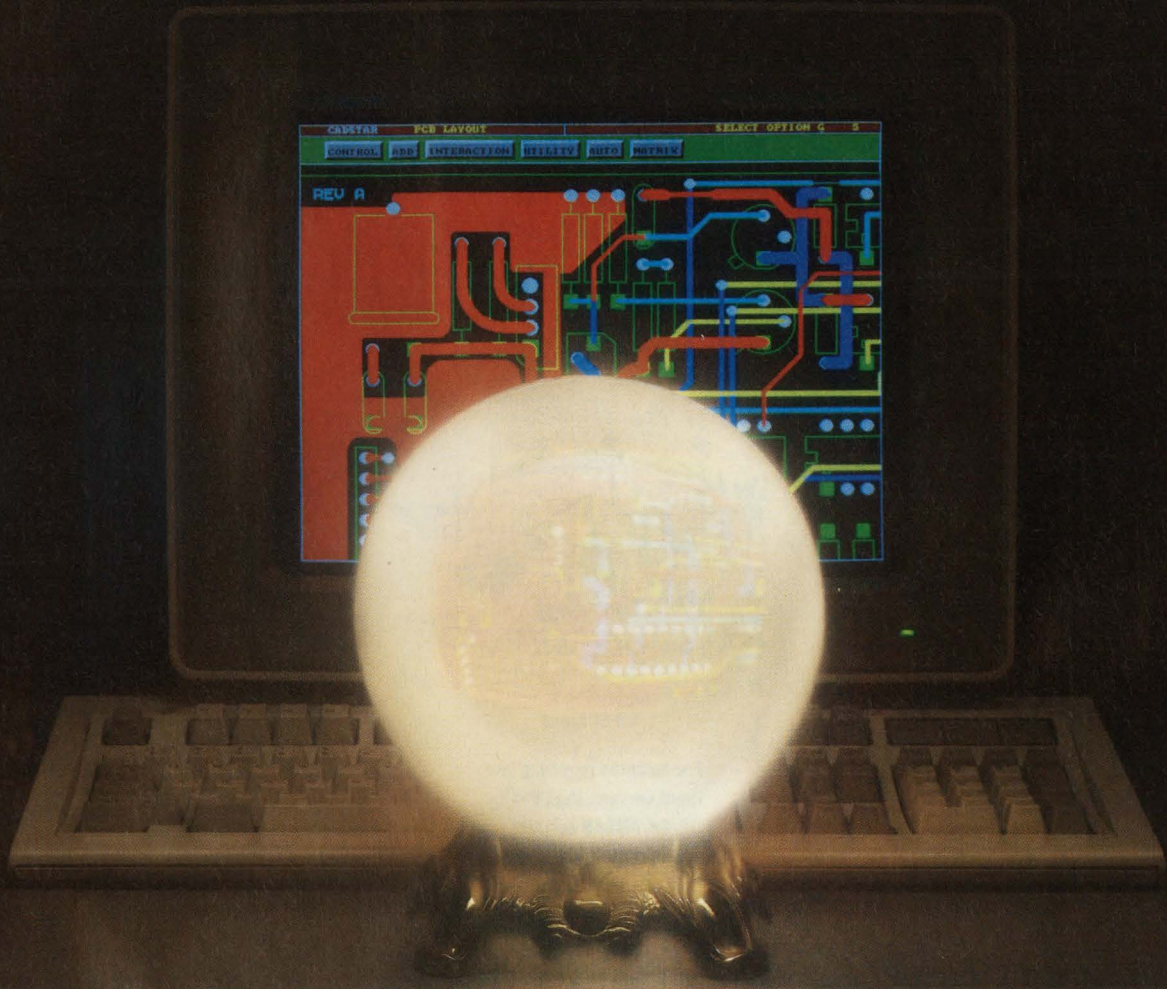
Yet another benchmark, the Remote Terminal Emulation (RTE) MUSBUS program, emulates multi-user activity by issuing multiple processes from many different sources, which generates realistic network traffic. The outcome indicates the system's ability to meet I/O, CPU and context switching demands in a multi-user environment.

write access to the I/O cache better illustrates the operation. First, the incoming virtual address should match the address stored in the I/O cache tag; second, the line in the I/O cache should be marked as valid and modified; and third, the virtual page number should be marked as cachable in the I/O cache. If all conditions are met, then the incoming data will be written into the line in the I/O cache for temporary buffering.

However, if there is no match, the page number is marked as hit, the line is also marked as valid but not modified, and the virtual page number is marked as non-cachable in the I/O cache. In this case, the incoming data will be written directly to the system memory instead of first being buffered by the I/O cache.

The I/O cache read cases can be treated in a

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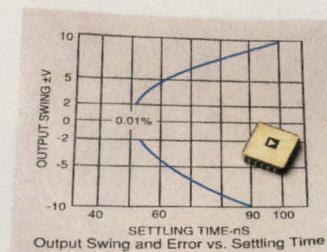
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CIRCLE 231 FOR RESPONSE OUTSIDE THE U.S.

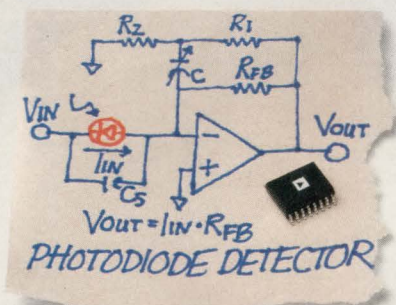
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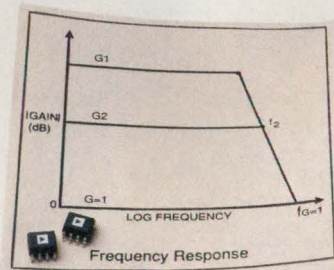
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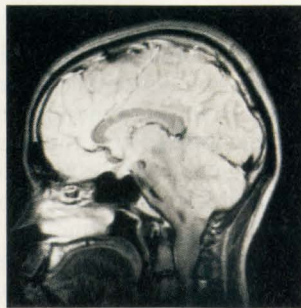
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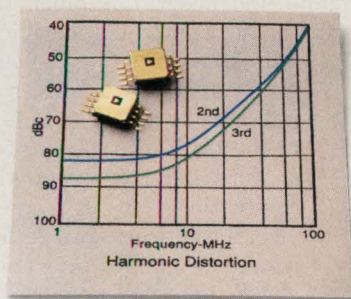
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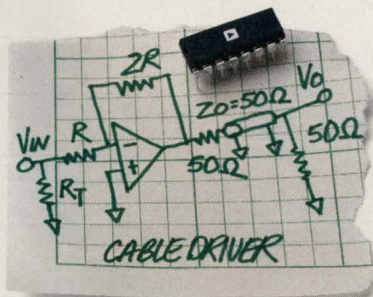
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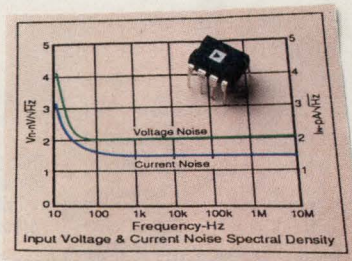
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I/O CACHING FOR HIGH THROUGHPUT

similar fashion. If the indexing virtual address encounters a match with the address stored in the I/O cache, and the line has been marked as valid, then the data will be supplied by the I/O cache to the accessing destination. If there is no match—that is, if the line is marked as valid and modified but the virtual page number is marked as non-cachable in the I/O cache, the data will be fetched from the main memory before it's transferred to the accessing destination.

Additional engineering trade-offs can be made in order to simplify the integration of the CPU cache and the I/O cache onto the same CPU board. For starters, the size of the I/O cache data line can be made to match that of the CPU cache. And, the system software can be designed so that all data moved to and from the I/O devices will have virtual addresses that align to the cache data line boundary. Transfers with unaligned addresses will be made non-I/O-cachable.

Furthermore, all I/O transfers with cache-line-aligned addresses can be made to be cache-line-based transactions, so that the partially modified line would only occur at the last data transfer of the entire transaction. The system software then instructs the I/O cache to execute a page flush in order to return the last data line left behind in the I/O cache back to main memory.

By taking some of these trade-offs into account, a server system can be implemented with 1 Mbyte allocated for the virtual addresses of VME-based I/O devices (8 kbytes/page), as was done in the SPARC-server 490. With each active I/O device mapped onto a different virtual page, multiple I/O transactions can be queued up at the same time.

The cache line size is 32 bytes per line, the same as the CPU cache. The I/O cache contains 4 kbytes of static RAM, which holds the 128 allocated virtual pages.

Another engineering trade-off in system design can be made by pulling the command and descriptor blocks for the Ethernet interface out of the main memory and putting them in the I/O cache. These data are used by the system software to set up the Ethernet interface.

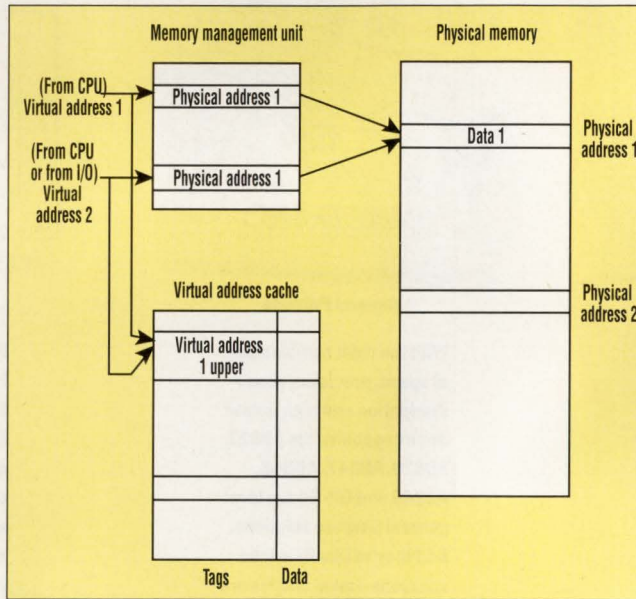
To perform its tasks, the Ethernet interface must execute read-modify-write operations on the command and descriptor blocks. However, the I/O cache that is supposed to buffer normal I/O data does not support the read-modify-write operation with I/O-cachable data, because the command and descriptor blocks for VME devices are non-I/O-cachable.

The Ethernet interface, though, always initiates a prefetch of the command and descriptor block for

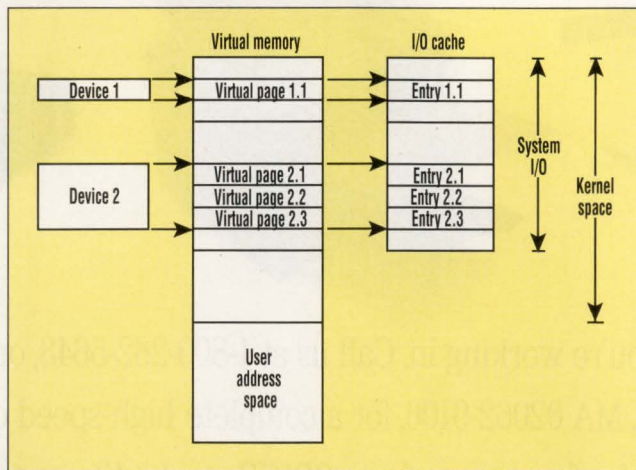
the next data buffer while a data transfer using the currently used data buffer is still in progress. The non-I/O-cachable data transfer suffers a delay during the arbitration for MMU service, the address translation time, the cache-coherency check, and the memory latency. Not caching the prefetched command and descriptor blocks defeats the original intent of using the I/O cache to minimize the penalties mentioned above.

To solve this problem, linear storage can be designated in the I/O cache to hold the Ethernet interface's command and descriptor blocks. The linear storage portion of the I/O cache and the CPU cache can be organized in the same way: The I/O cache's linear storage can literally cache all the Ethernet command and descriptor blocks. The system software can then treat this linear storage as an extension of the main memory.

All data blocks in this linear storage will stay in the I/O cache while the machine is up, because they are part of the system memory dedicated to networking. To the Ethernet interface, the command and descriptor blocks are portions of the I/O cache that are separated from the normal I/O data path. When the command and descriptor blocks are prefetched by the Ethernet



3. WHEN TWO SEPARATE virtual-page numbers are mapped to the same physical-page number, the two virtual addresses are called synonyms. Synonym detection is done by the system hardware with software support.



4. DIRECTLY MAPPING I/O DEVICES into a kernel's address space with a unique set of virtual pages assigned to each device lets the I/O devices communicate with the system memory very efficiently.

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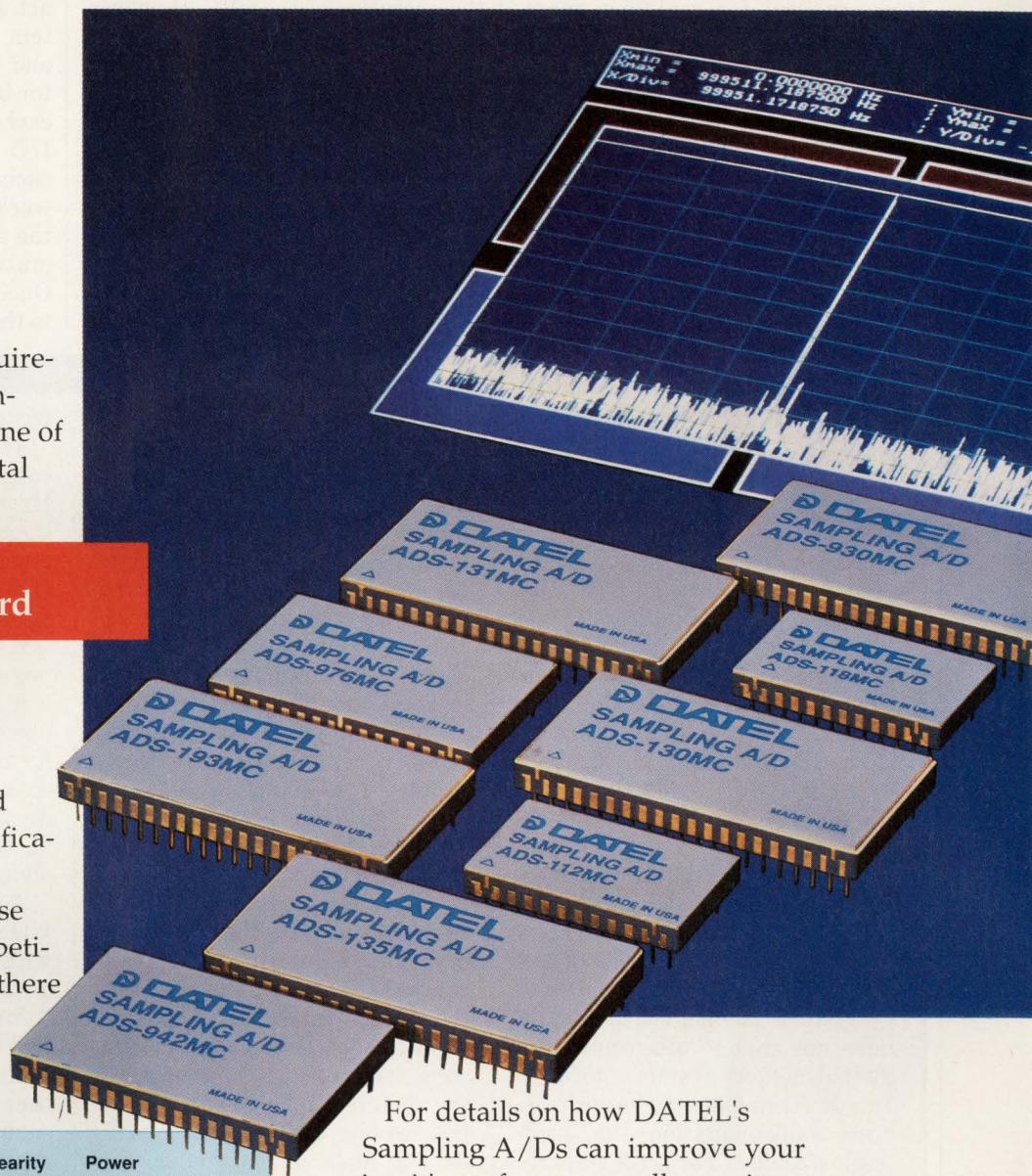
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ADS-117	12	2.0	±3/4	1.4	24-PIN
ADS-132	12	2.0	±1/2	2.9	32-PIN
ADS-118	12	5.0	±1/2	2.3	24-PIN
ADS-131	12	5.0	±3/4	3.6	40-PIN
ADS-130	12	10.0	±3/4	3.8	40-PIN
ADS-924	14	0.300	±1	1.3	24-PIN
ADS-928	14	0.500	±1/2	2.9	32-PIN
ADS-941	14	1.0	±3/4	3.1	32-PIN
ADS-942	14	2.0	±3/4	3.2	32-PIN
ADS-944	14	5.0	±1	3.4	32-PIN
ADS-976	16	0.200	±2	1.8	32-PIN
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I/O CACHING FOR HIGH THROUGHPUT

interface during normal data transfer, the cache speed makes this feature practical for real-time operation.

I/O operations on the system bus (for example, VMEbus) are under the control of the system software. That software, in turn, controls the system's I/O arbiter, which manages I/O-cache accesses. For optimal I/O data throughput, the I/O arbiter should allow I/O operations to have default access to the I/O cache via the system bus.

Network interface access to the I/O cache can be asynchronous to the operation of the CPU. However, the network interface is only equipped with a limited internal data buffer, which must be either filled or emptied in time to meet network speeds. Additionally, the network interface also needs access to the I/O cache in order to fetch the command and descriptor blocks. It can do this while the network I/O transfers are occurring through the I/O cache.

The I/O arbiter can use a "round-

robin" algorithm for arbitrating the I/O cache access by its three major activities: I/O operations via the system bus, network I/O operations, and network command-and-descriptor-block prefetching. When the I/O cache is idle, the default state allows I/O operations to access the I/O cache via the system bus. When network I/O transfers require access, the arbiter will preempt the I/O operations via the system bus as well. Once the network I/O gains access to the I/O cache, it will be allowed to

CACHE DESIGN TRADEOFFS

With a virtual cache, virtual-to-physical address translation is only needed when the CPU encounters a cache miss. For a reasonably-sized virtual cache running with less than a 1% miss rate, skipping the address translation process speeds up cache access considerably. The MMU performs address translation while the CPU accesses the virtual cache. The resulting physical address is only needed when the physical memory must be referred to.

Another advantage of the virtual cache over its physical counterpart is that the physical cache is usually limited by the size of the page defined by the virtual memory system. The page size usually does not change often once the virtual memory system is defined. In a direct-mapped cache with discrete implementation, the fixed-page size does not scale linearly with the advances of component technology. This is not true for the virtual cache.

On the other hand, the physical cache uses a simpler mechanism for maintaining cache data coherency than its virtual counterpart. The mapping of a direct-mapped cache for each data line is done using the data address modulo of the cache size to index into the line position. With a physical cache, the cache tag of each data line contains the unique physical page number. When a data line is in-

dexed, the cache tag identifies whether the cache access has encountered a hit or miss. A hit means that the physical page number of the indexing address matches the physical page number of the indexed data line stored in the tag. The hit/miss criterion also contains the user context identification number as part of its checking algorithm.

The cache write policy also categorizes caches into different groups. Two commonly invoked write policies include write-through and write-back. The write-through policy means that a cache write access will bring the result of a write to the main memory. The write-back policy will cause the cache to be updated and the main memory to be updated when a cache write-back occurs at some later point. Unfortunately, the difference between the two policies sometimes results in stale data in main memory when the write-back policy is chosen. Care must be taken in order to maintain the coherence of data between the cache and main memory.

There are also two options for cache writes: write-with-allocation and write-without-allocation. With the former, the data in main memory is brought to the cache before the cache update. This is a read-modify process done at the cache. For write-without-allocation, the data is written directly to the cache. The write-back policy is usually implemented with the

write-with-allocation option.

The linear storage model of a cache works well for CPU data. However, this model can be further simplified to match the characteristics of I/O data because I/O devices tend to invoke linearly consecutive addresses during DMA operation. In a demand-page system, where each I/O device is mapped as an independent object with its addressing capability measured in units of pages, the data flow tends to stay in the mapped page with sequential and linearly increasing or decreasing addresses.

A cache memory for buffering I/O data can thus be organized with a single line per page, as all of the addresses of the data going through the buffer are sequential and consecutive. Cache data line replacement will occur naturally, because the data line of the next sequential transfer automatically replaces the data line of the previous transfer. This kind of cache memory can thus be viewed as a page cache.

The advantages of a page cache over a linear cache are less data buffer capacity (hence smaller cache size) and simpler management algorithms (hence less complexity) for achieving cache functionality. However, the page cache is a degenerate case of a general-purpose linear cache and can only be used to buffer the data streams that have sequential and linearly consecutive addresses.

I/O CACHING FOR HIGH THROUGHPUT

fill or empty the internal data buffer in the network interface. The operation for prefetching the network command and descriptor blocks can be interleaved with the network I/O and the system bus I/O operations, with a guaranteed slot based on the round-robin algorithm.

The existence of two autonomous, virtual-address-accessed, write-back caches introduces design complexity usually observed only in multiple-processor systems. The CPU cache and I/O cache form a parallel cache system. Data coherence between the CPU cache, the I/O cache and the main system memory can be maintained by the hardware with software support.

The first complication in this parallel cache system comes from synonyms that are inherent to all caches accessed and tagged with virtual addresses. These synonyms (also known as aliases) are different virtual addresses that map to the same physical address.

With a virtual cache, both the indexing address and the cache tag contain a virtual page number. When the two virtual page numbers disagree, the system must refer to the MMU to determine whether the two separate virtual page numbers are mapped to the same physical page number. If they are, the two virtual addresses are called synonyms (Fig. 3). A synonym check

TABLE 2A: I/O DATA WRITTEN TO CPU MEMORY VIA THE I/O CACHE

VA status		Line status		Page	Activity
Line VA	Page VA	Line Val	Line Mod	I/O cache cacheable	Action by I/O cache controller
Hit	X	Yes	Yes	Yes	Data buffered in I/O cache
Hit	X	Yes	No	No	Data written through
Hit	X	Yes	No	X	Data buffered in I/O cache and line marked Val and Mod
Hit	X	No	X	No	Data written through
Hit	X	No	X	Yes	Data buffered in I/O cache and line marked Val and Mod
Miss	Hit	Yes	Yes	Known	Stored data written back, new data buffered in I/O cache and line marked Val and Mod
Miss	Hit	Yes	No	No	Data written through
Miss	Hit	Yes	No	Yes	Data buffered in I/O cache and line marked Val and Mod
Miss	Hit	No	X	No	Data written through
Miss	Hit	No	X	Yes	Data buffered in I/O cache and line marked Val and Mod
Miss	Miss	Yes	Yes	No	Data written through
Miss	Miss	Yes	Yes	Yes	Stored data written back, new data buffered in I/O cache and line marked Val and Mod
Miss	Miss	Yes	No	No	Data written through
Miss	Miss	Yes	No	Yes	Data buffered in I/O cache and line marked Val and Mod
Miss	Miss	No	X	No	Data written through
Miss	Miss	No	X	Yes	Data buffered in I/O cache and line marked Val and Mod

TABLE 2B: I/O DATA READ FROM MAIN MEMORY VIA THE I/O CACHE

VA	Line status		Page	Activity
Line VA	Line Val	Line Mod	I/O cache cacheable	Action by I/O cache controller
Hit	Yes	X	X	Data read from I/O cache
Hit	No	X	No	Data fetched from main memory
Hit	No	X	Yes	I/O cache line fill from main memory, line marked Val only and data read from I/O cache
Miss	Yes	Yes	No	Data fetched from main memory
Miss	Yes	Yes	Yes	Stored data written back, I/O cache line fill from main memory and line marked Val only, data read from I/O cache
Miss	Yes	No	No	Data fetched from main memory
Miss	Yes	No	Yes	I/O cache line fill from main memory, line marked Val only and data read from I/O cache
Miss	No	X	No	Data fetched from main memory
Miss	No	X	Yes	I/O cache line fill from main memory, line marked Val only and data read from I/O cache

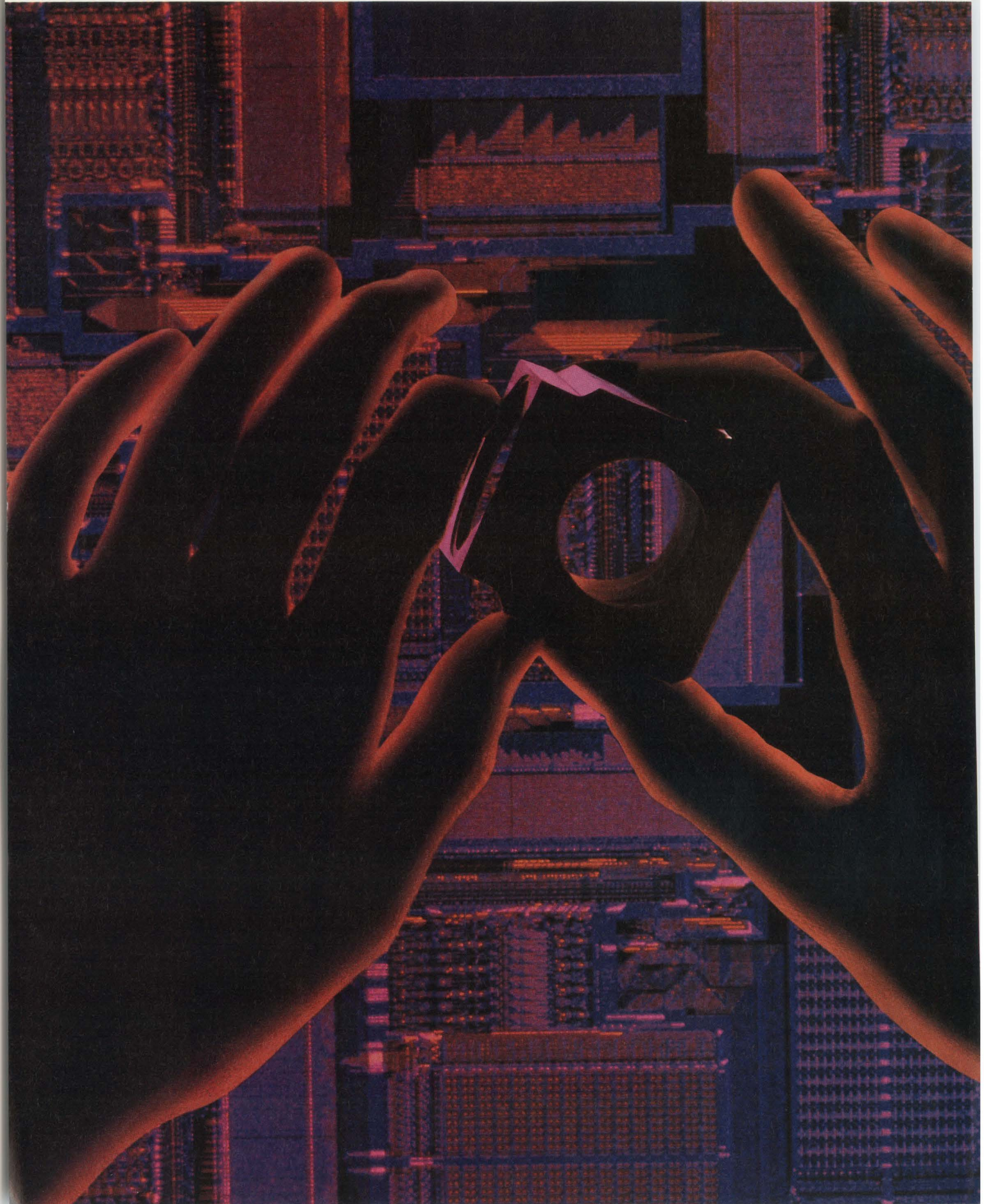
must be done in every virtual cache miss, in order to determine whether or not the data line in the virtual cache should be replaced.

In a direct-mapped virtual cache, a synonym check can be done in three steps. The first is to translate the indexing virtual address while accessing the virtual cache. If the cache access encounters a miss, the resulting physical page number is temporarily saved. The virtual page number in the cache tag is then used to cycle through the MMU for its translation. The resulting physical page number is compared with the saved copy of the physical page number from the previous translation. If the two physical page numbers agree, a synonym exists.

Synonym detection is done by hardware with software support. The system software makes the aliasing addresses modulo the CPU cache size in order to force the aliasing addresses to hit the same cache entry. Addresses that do not follow the synonym rule will not be made CPU-cacheable. Synonym detection will be performed by the hardware for every CPU cache miss, whether it is due to I/O data transfer or to a true CPU access.

Another problem is maintaining the updated copy of data in main memory when the I/O devices are trying to update the memory image or requesting data from memory. The I/O cache uses the Valid and Mod-

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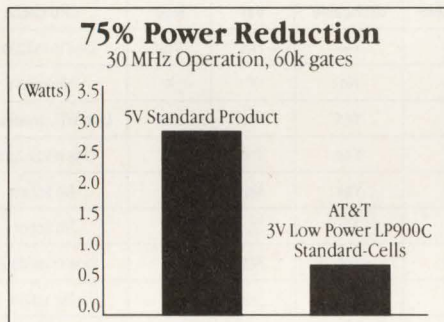
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ified bits in its tags to keep track of the status of the data line. When the I/O cache needs to access the main memory, a data consistency check must be performed by the CPU cache (Tables 3A and 3B). It is important to maintain data coherency between the CPU cache and main memory, between the CPU cache and the I/O cache, and between the I/O cache and main memory. The page status of each virtual page number is specified with two cachable bits, one of which defines whether the page is cachable in the CPU cache, while the other defines the cachability of the page in the I/O cache. The CPU cache line status is marked by the Valid and Modified bits. The action column reports the operations performed by the CPU cache controller and the I/O cache controller.

A write access to the I/O cache can cause it to request a memory transfer, in order to transport the entire data line back to main memory. If the indexing virtual address encounters a match in the CPU cache, the data-line status in the CPU cache must be examined along with the attributes of the virtual page number in the MMU. If the data line in the CPU cache is marked as valid and modified and the virtual page number has been marked to be cachable in both the CPU cache and the I/O cache, then the data line in the CPU cache must be invalidated and the data line in the I/O cache must be written back to main memory. In doing so, the memory will thus contain the most up-to-date copy of the data modified by the I/O device. If the CPU operation requires the data just modified by the I/O device, a CPU cache line-fill operation will be performed to bring the

updated copy back to the CPU cache from main memory.

Similarly, where the attributes of the virtual page number in the MMU have been marked as cachable in the I/O cache but not in the CPU cache, then the line status in the CPU cache becomes "don't care" and the data line in the I/O cache will be written back to main memory while the CPU cache control logic does nothing. Again, the main memory will contain the most up-to-date copy of the data modified by the I/O device.

If an I/O device tries to read data from the I/O cache, and that read requires the I/O cache to fetch data from main memory, then the attributes of the virtual page number as well as the data-line status in the CPU cache must be checked to ensure that the data is the most up-to-date copy. For a line of data in the CPU cache to be transferred to the I/

O cache for a requesting I/O device, several conditions must be met (Fig. 4). First, the indexing virtual address must encounter a match in the CPU cache; second, the data-line status in the CPU cache must be marked as valid and modified; and third, the virtual page number must also be specified as cachable in both the CPU cache and the I/O cache. Then the CPU cache must first write back the data line to main memory before that line of data can be transferred.

If the virtual page number is marked as cachable in the I/O cache and not in the CPU cache, then the main memory contains the most up-to-date copy of the data requested by the I/O device. The I/O cache controller performs a line-fill operation to transport a line's worth of data from main memory to the I/O cache before supplying the requested data to the I/O device.

The interlocking hardware interface between the CPU cache, the I/O cache, and the main memory interface can ease the implementation of data coherency protocols (Fig. 5). When the I/O cache initiates a DMA transaction, it notifies the CPU cache of the need for translating the virtual address into the physical address. The CPU cache controller prepares the MMU for executing the address translation and signals the I/O cache at the end of the address translation operation.

When I/O data must be written to the main memory, the I/O cache could supply the data to the I/O cache memory interface at the same time as the address is being translated. When the address translation is finished, the I/O cache could resume its next operation, as the main memory interface would automatically

TABLE 3A: I/O DEVICE WRITES TO CPU MEMORY VIA THE I/O CACHE

Page status		CPU cache status		Action	
I/O cache cachable	Cache cachable	Line Val	Line Mod	CPU cache	I/O cache
Yes	Yes	Yes	Yes	Line invalidated	Line WB, invalidated
Yes	No	X	X	No action	Line WB, invalidated
No	Yes	Yes	Yes	Line WB, invalidated	Data WT
No	Yes	Yes	No	Line invalidated	Data WT
No	Yes	No	X	No action	Data WT
No	No	X	X	No action	Data WT
Yes	Yes	Yes	No	Line invalidated	Line WB, invalidated
Yes	Yes	No	X	No action	Line WB, invalidated

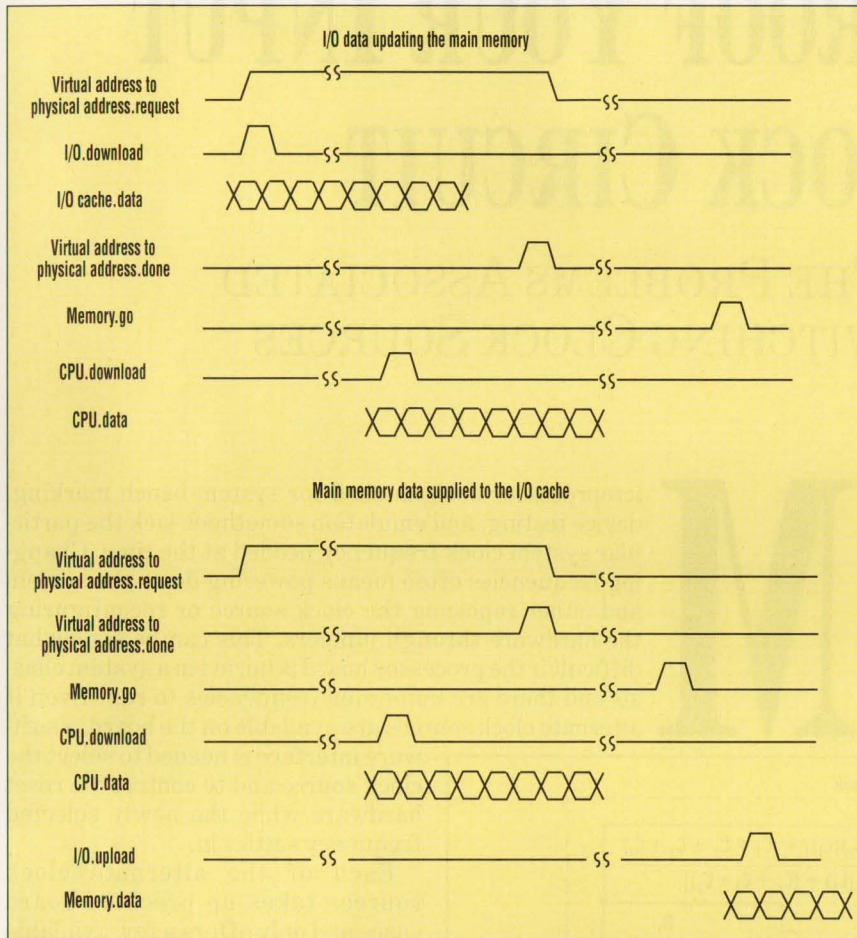
WB = Written back WT = Written through

TABLE 3B: I/O DEVICE READS FROM CPU MEMORY VIA THE I/O CACHE

Page status		CPU cache status		Action	
I/O cache cachable	Cache cachable	Line Val	Line Mod	CPU cache	I/O cache
Yes	Yes	Yes	Yes	Line WB, stay valid	Line fill
Yes	Yes	Yes	No	No action	Line fill
Yes	Yes	No	X	No action	Line fill
Yes	No	X	X	No action	Line fill
No	Yes	Yes	Yes	Line WB, stay valid	Data fetch
No	Yes	Yes	No	No action	Data fetch
No	Yes	No	X	No action	Data fetch
No	No	X	X	No action	Data fetch

WB = Written back

I/O CACHING FOR HIGH THROUGHPUT



5. THE INTERLOCKING hardware interface between the CPU cache, I/O cache and the main-memory interface facilitates the implementation of data coherency protocols. In cases where I/O data is supplied by the main memory, then the I/O cache can wait for the main-memory interface to provide the data before it finishes its current operation. If this happens, the main memory interface can use the IO.Upload signal to notify the I/O cache when the memory data burst is available for the I/O cache to absorb (bottom).

send the I/O data back to the main memory.

If, however, the I/O data is supplied by the main memory, then the I/O cache will wait for the main memory interface to provide the data before it finishes its current operation. The main memory interface can use the "IO.UPLOAD" signal to notify the I/O cache when the memory data burst is available for the I/O cache to absorb.

After the virtual-address-translation operation, the CPU cache can proceed with checking the alias and the write-back operation, which may require downloading an entire cache line from the CPU cache to the CPU cache memory interface. The CPU

cache must signal the CPU cache memory interface that the cache data download operation has ended, so that the main memory can be updated with the data from the CPU cache before the I/O data is merged with it. □

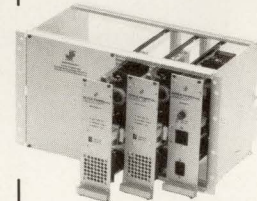
Michael M. Hsieh is a CPU hardware design engineer at Sun Microsystems Inc., Mountain View, Calif.

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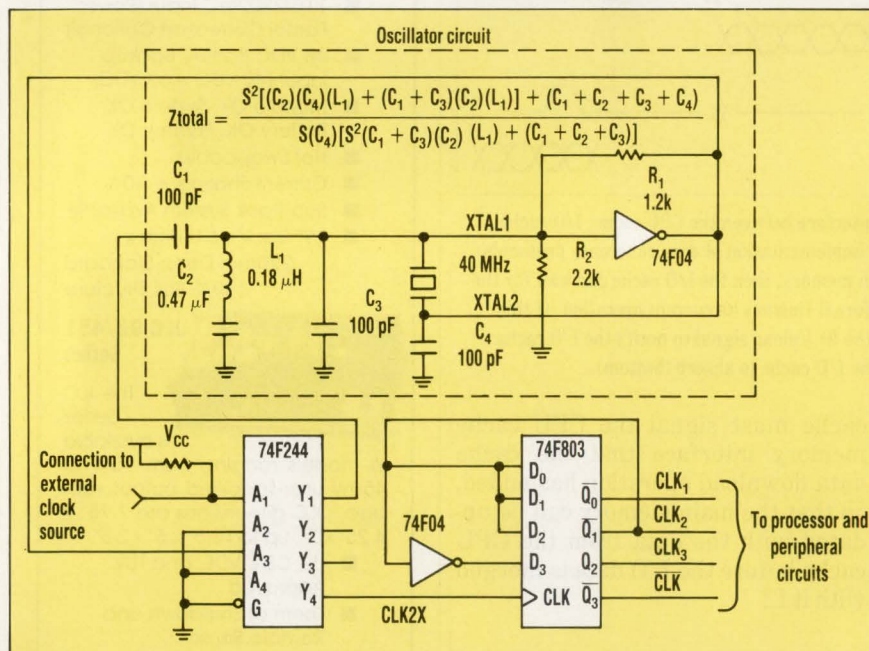
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REMOVE THE PROBLEMS ASSOCIATED WITH SWITCHING CLOCK SOURCES

Microprocessor designs used for system bench marking, device testing, and emulation sometimes lack the particular system clock frequency needed at the time. Changing frequencies often means powering down the system and either replacing the clock source or reconfiguring the hardware through jumpers. This can be somewhat difficult if the processor board is buried in a system chassis and there are numerous frequencies to run. Even if alternate clock sources are available on the board, a software interface is needed to select the clock source and to control the reset hardware while the newly selected frequency settles in.

Each of the alternate clock sources takes up precious board space and only offers a few available frequencies. Connecting to an external frequency generator might seem to solve the problem. However, a software-select interface is still required to enable the external clocking path. Also, selecting the external clock might hang the system if the external frequency source is either powered down or disconnected. This may seem like a minor inconvenience unless the hardware and software environments require an extensive setup procedure to perform a complex system analysis.

The problems associated with switching clock sources and having the system hang when alternate clock sources are turned off can be avoided by building clock circuits that dynamically switch between an



1. BY COMBINING an on-board crystal-controlled oscillator with a connection to an external frequency source, the problems associated with switching clock sources can be averted. If the external clock stops operating, the 40-MHz crystal oscillates, supplying a frequency source for the rest of the circuit.

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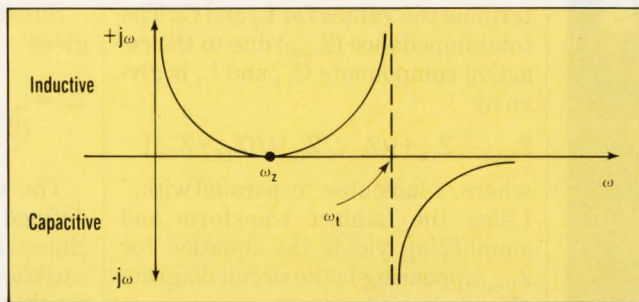
REMOVE SWITCHING CLOCK-SOURCE PROBLEMS

external clock and a built-in source. One possible circuit combines an on-board crystal-controlled oscillator with a connection to an external frequency source (Fig. 1). Because both options are available at the same time, a software-select mechanism isn't required. If the external clock source is either unconnected or in a high-impedance state, the 40-MHz crystal is allowed to oscillate, supplying a frequency source to the rest of the circuit. When a frequency change is required, the processor is held in a reset mode while the new frequency is dialed in on the frequency generator. The system needn't be powered down, reconfigured, and put back together. Also, the software doesn't have to interface with the system's reset hardware because the reset button can be held manually while changing frequencies.

If an external clock source connects to the input of the 74F244 buffer, then the buffer's output is coupled to the oscillator section (signal XTAL1) through capacitor C_1 , overdriving the crystal. This prevents the crystal from oscillating. The 74F04 inverts the XTAL1 signal which is then buffered through the 74F244, which produces the CLK2X signal. The 74F803 divides the CLK2X signal by two to generate the system clock signals (CLK1, CLK2, CLK3, and CLK). Motorola's 74F803 quad D-type flip-flop contains matched propagation delays on its outputs.

Both the high-to-low and low-to-high transitions are guaranteed to skew together with a maximum variation of 1 ns on the Q1 output and 1.5 ns for the other outputs. Also, the skew between any two outputs is guaranteed to be within 1.5 ns. This allows generation of extremely tight duty cycles for the system clock, which is a requirement for processors operating at high frequencies. Designing a divide-by-two circuit with a 74F74 flip-flop results in a possible skew of 5 to 6 ns because the minimum and maximum propagation delays must be accounted for.

External clock and a built-in source. One possible circuit combines an on-board crystal-controlled oscillator with a connection to an external frequency source (Fig. 1). Because both options are available at the same time, a software-select mechanism isn't required. If the external clock source is either unconnected or in a high-impedance state, the 40-MHz crystal is allowed to oscillate, supplying a frequency source to the rest of the circuit. When a frequency change is required, the processor is held in a reset mode while the new frequency is dialed in on the frequency generator. The system needn't be powered down, reconfigured, and put back together. Also, the software doesn't have to interface with the system's reset hardware because the reset button can be held manually while changing frequencies.



2. THE REACTANCE CURVE is based on the equation for the circuit's total impedance— W_z is found to be neither inductive nor capacitive. The function switches from the inductive to the capacitive region at pole ω_1 .

The 74F803 eliminates the analysis of these delays by guaranteeing a maximum delay skew. The MC88913 and MC88914 divide-by-two flip-flops match propagation delays for operation at high frequencies. Both flip-flops generate CMOS-level outputs and are TTL compatible.

The circuit's oscillator section uses a 3rd-overtone, 40-MHz parallel-resonant crystal to control the operating frequency. The oscillator's amplifier stage uses a 74F04 inverter to amplify the XTAL1 signal. XTAL2 has a 180° phase shift from XTAL1 and is used as feedback to the crystal. Also, the XTAL2 signal is buffered through the 74F244 buffer and used as a clock source for the rest of the system.

The 74F04's input is biased between 1.4 and 1.5 V, which is the inverter's switching region. The R_1 - R_2 resistor network creates a voltage divider from the inverter's output to its input. This divider uses the inverter's output as the voltage source to allow self compensation for any variation in resistor values. This makes the circuit self-biasing around the switch point and, thus, eliminates the need for any high-precision resistors. Because the inverter's input is biased at the switch point, the output can be expected to spend half its time driving a high voltage and the other half of its time driving a low voltage. Therefore, the average dc voltage at the inverter's output (V_{out}) is given by:

$$V_{out} = V_{OH}/2$$

where V_{OH} is the inverter's output

high voltage (around 4.4 V). The inverter's input voltage (V_{in}) is given by the voltage divider equation

$$V_{in} = \left(\frac{R_2}{R_1 + R_2} \right) V_{out}$$

Substituting for V_{out} gives

$$V_{in} = \left(\frac{R_2}{R_1 + R_2} \right) \left(\frac{V_{OH}}{2} \right)$$

and solving for R_1 gives

$$R_1 = \left(\frac{R_2}{V_{in}} \right) \left(\frac{V_{OH}}{2} \right) - R_2$$

Picking a value of 2.2 k Ω for R_2 and solving for R_1 yields

$$R_1 = \left(\frac{2.2k}{1.45} \right) \left(\frac{4.4}{2} \right) - 2.2k = 1.14k$$

Rounding to the next-common value resistor gives 1.2 k Ω for R_1 .

Capacitors C_3 and C_4 adjust the slew rate of the inverter to contain a component of the crystal frequency for startup conditions. The values for C_3 and C_4 were determined experimentally.

The inverter and R_1 - R_2 voltage-divider network can be eliminated when connecting to either a microprocessor or a commercially available oscillator package that directly supports crystal devices. The XTAL1 and XTAL2 signals connect to the oscillator package or microprocessor pins, which are typically labelled with the same signal names.

Inductor L_1 and capacitor C_2 form a tank circuit that filters out the crystal's fundamental frequency to ensure oscillation at the 3rd harmonic. Because the crystal appears inductive at parallel resonance, the tank circuit must also be inductive at the fundamental frequency, thus preventing oscillation. The tank circuit appears capacitive at the 3rd harmonic, canceling the inductance of the crystal, and therefore supporting oscillation.

The reactive components seen by the crystal must be analyzed to de-

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termine the values for L_1 and C_2 . The total impedance (Z_{total}) due to the reactive components C_{1-4} and L_1 is given by

$$Z_{total} = Z_{C4} + [(Z_{C1} // Z_{C3}) // (Z_{L1} + Z_{C2})]$$

where // indicates "in parallel with." Using the Laplace transform and simplifying yields the equation for Z_{total} appearing in the circuit diagram (Fig. 1, again).

In the reactance curve of this equation, ω_z is neither inductive nor capacitive and is found by setting the numerator of the above equation to zero (Fig. 2). The pole of interest, ω_t , where the function switches from the inductive to the capacitive region, is found by setting the denominator to zero. Once the equation for ω_t is simplified, the inductor value can be chosen to place ω_t between the crystal's 2nd and 3rd harmonics. Because the tank circuit's reactance is inductive at the fundamental frequency, the crystal oscillates at the 3rd harmonic. The poles of the equation are calculated using the equation:

$$S(C_4)[S^2(C_1 + C_3)(C_2)(L_1) + (C_1 + C_2 + C_3)] = 0$$

This function has a pole at zero. However, the pole of interest, ω_t , is given by

$$[S_2(C_1 + C_3)(C_2)(L_1) + (C_1 + C_2 + C_3)] = 0$$

Solving for S yields

$$S^2 = \frac{-(C_1 + C_2 + C_3)}{(C_1 + C_3)(C_2)(L_1)}$$

If the value for C_2 is chosen to be much greater than C_1 and C_3 , the equation simplifies to

$$S^2 = \frac{-1}{(C_1 + C_3)(L_1)}$$

Substituting $j\omega$ for S yields

$$\omega_t = \frac{1}{\sqrt{(C_1 + C_3)(L_1)}}$$

where ω_t is in radians/s. It relates to the frequency (f_t) by:

$$\omega_t = 2\pi f_t$$

Substituting and solving for L_1 gives

$$L_1 = \frac{1}{(2\pi f_t)^2 (C_1 + C_3)}$$

The value for C_1 was previously defined as 100 pF. C_2 was arbitrarily chosen to be 0.47 μ F, which partially satisfies the assumption that C_2 is much greater than C_1 and C_3 . Arbitrarily making C_3 equal to C_1 completely satisfies the C_2 assumption. The 3rd overtone parallel-resonant crystal has a frequency rating of 40 MHz. The fundamental frequency (f_0) is therefore 40 MHz/3 or 13.33 MHz. The tank circuit's pole (f_t) should be placed between $2f_0$ and $3f_0$ or between 26.67 and 40 MHz. Using 27 MHz for f_t and evaluating the equation for L_1 yields

$$L_1 = \frac{1}{(2\pi 27 \text{ MHz})^2 (100 \text{ pF} + 100 \text{ pF})} = 0.17 \mu\text{H}$$

Rounding to the nearest commercial available inductor gives 0.18 μ H for L_1 .

For printed circuit boards, all capacitors and resistors should be soldered directly in place. L_1 should be left socketed so the tank circuit can be removed. If a fundamental crystal is used, L_1 should be removed. Also, if an alternate crystal frequency is desired, then L_1 should be recalculated and replaced.

Problems associated with changing clock frequencies can be avoided by letting the clock circuit dynamically switch between an on-board frequency source and an external frequency source. A big advantage of using this method is that it keeps the system from losing clock information even if the external frequency source is turned off. Thus, it prevents system failures. □

Don Atkins is a system design engineer at Motorola. He holds a BSEE from the University of Illinois.

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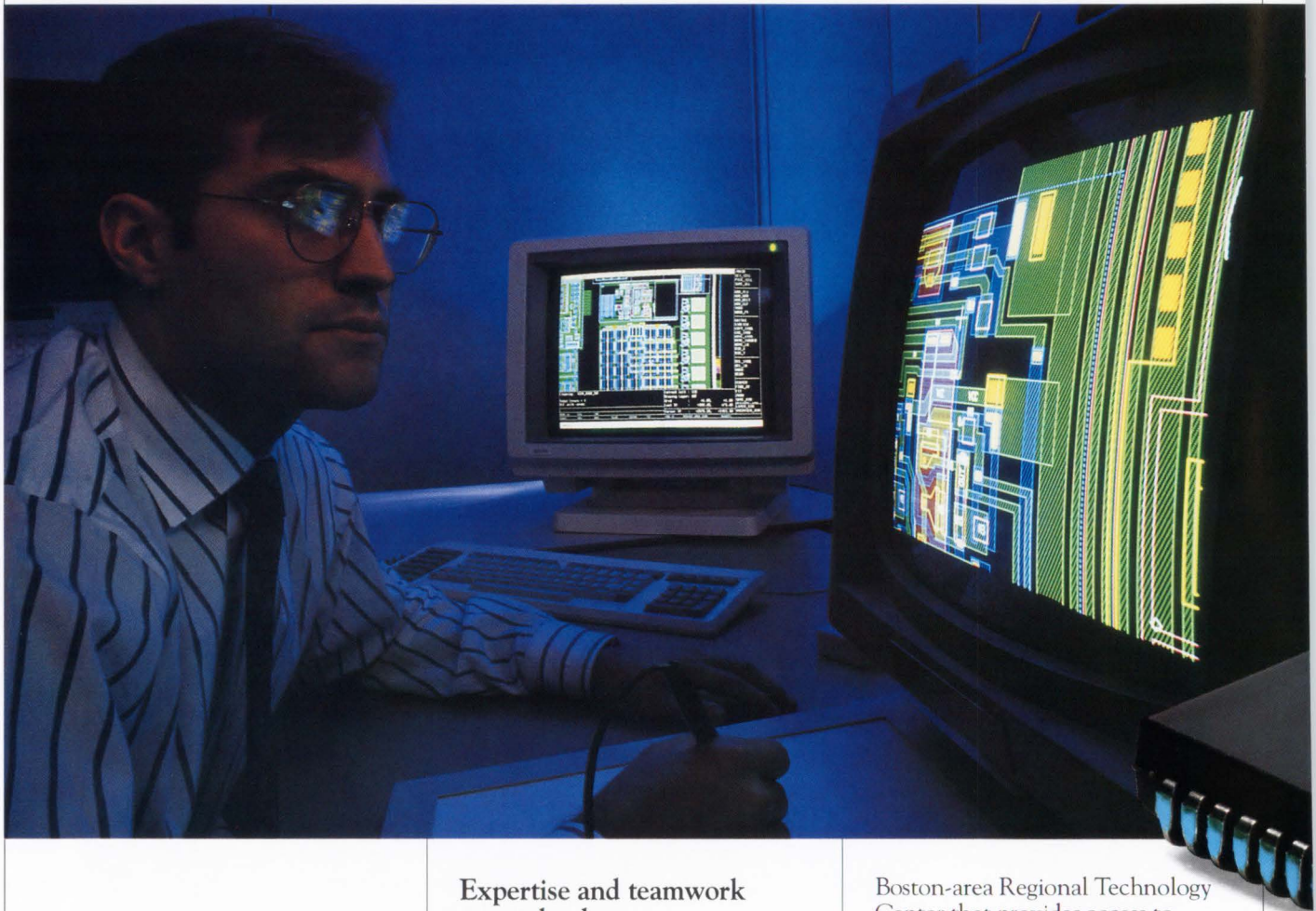
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TECHNOLOGIES



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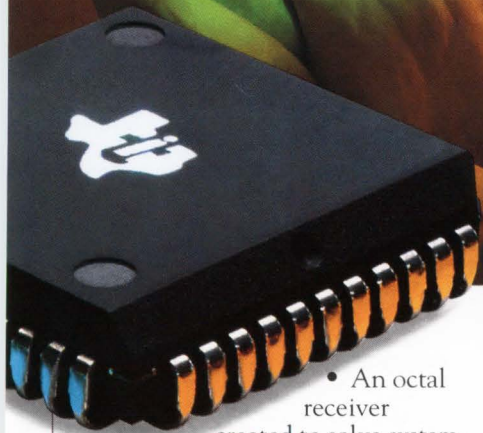
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— Nick Ilyadis, Product Engineer
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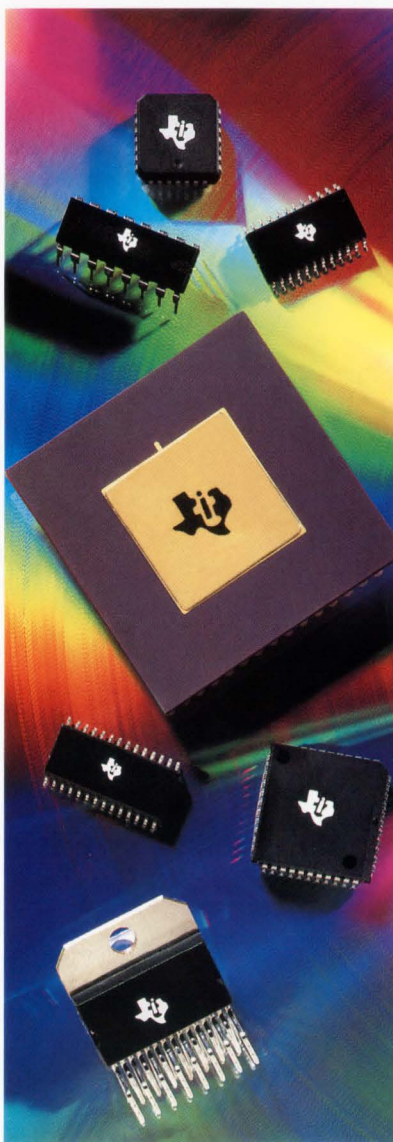
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ELECTRONIC DESIGN

High-Performance Packaging Increases System Speed And Density

Bare chips on silicon substrates can free VLSI designs from the constraints of single-chip packages.

BY ERIC BOGATIN

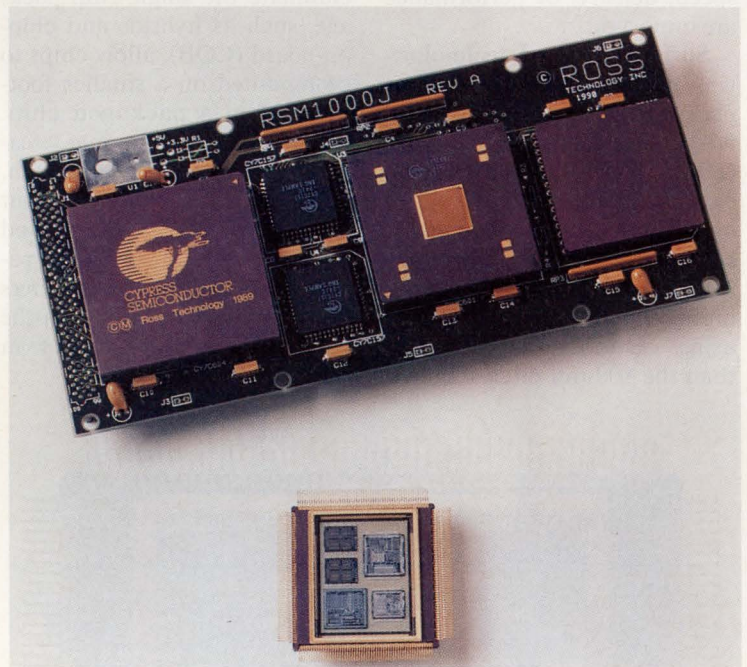
nChip, 1971 North Capitol Ave., San Jose, CA 95132; (408) 945-9992, ext. 228.

Advances in IC technology have delivered rapid increases in the performance of individual ICs. But without advanced packaging techniques, much of these IC-performance gains can be lost at the system level. The limiting factor in the performance of high-speed electronics systems is increasingly apparent: the 30-year-old packaging strategy of single-chip packages on printed-wiring boards (PWBs).

The single-chip approach has not been without technological advances, and we are well into the latest evolutionary step, which is the transition from through-hole-mounted to surface-mounted packages. But VLSI devices are getting larger, which means more inputs and outputs and finer-pitch pads on the chip. In addition, system-clock frequencies are higher and so is power dissipation. As a result, the conventional packaging technology, even with surface mounting, is no longer transparent to the system performance. The use of single-chip packages on pc boards often limits the intrinsic performance of which today's VLSI devices are capable.

The two critical packaging-related problems caused when state-of-the-art VLSI chips are

1. Drastic size reductions can be seen in this comparison of a typical RISC-microprocessor chip set using conventional single-chip packaging to the equivalent functionality in a bare-die MCM rendering.



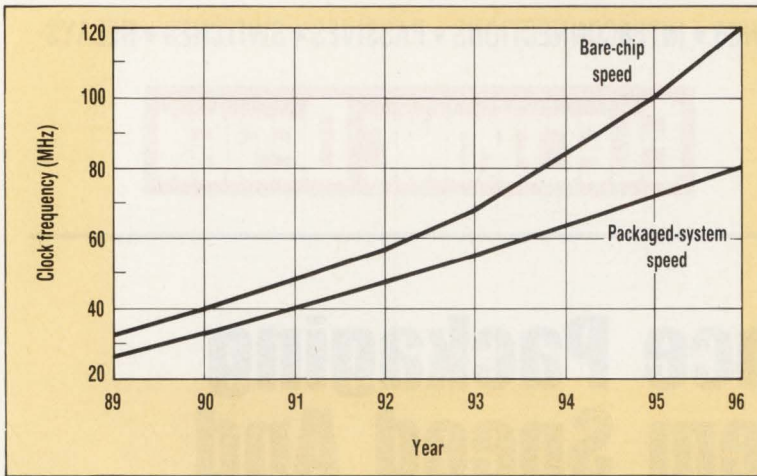
packaged conventionally are limited clock frequency and excessive noise. Wringing the best performance out of new, advanced VLSI chip technologies calls for advanced packaging technologies.

The introduction of multi-chip-module (MCM) technology, in which the single-chip package is eliminated and multiple bare die are mounted very close together on a high-density-interconnection (HDI) substrate, is one such enabling strat-

egy. One approach to MCMs uses silicon as the base and is called a silicon circuit board (SiCB). An example of a five-chip set implemented as an MCM, compared with its equivalent circuit implemented in the conventional approach, is shown (Fig. 1).

MCM technology incorporates short interconnection lengths between chips, small electrical parasitics associated with the chip bonding, and enhanced features which allow the

■ HIGH-PERFORMANCE PACKAGING ■



2. Using a CMOS microprocessor as an example, this graph shows that as raw processor speeds increase, the limitations imposed by single-chip packaging become more severe.

system-clock frequency to approach the chips' ultimate limit. As this technology moves up the learning curve, it's becoming a very cost-effective solution for packaging problems where speed, density, or performance are important.

Surface-mounted technology was motivated by these same performance factors. Compared with dual-in-line packages (DIPs), surface-mounted chip carriers offer a smaller footprint on the board and allow chips to be mounted closer together. Surface-mounted PWBs can have higher interconnection density using via grids that are finer than the 100-mil pitch required

for through-hole mounting. But the use of single-chip packages still fundamentally limits the proximity of chips and contributes to lower clock frequencies.

Other technologies which eliminate the single-chip package, such as hybrids and chip-on-board (COB), allow chips to be mounted on a smaller footprint than a packaged chip. These methods share many features with the MCM approach, especially in assembly. Without the expense of a package, and with the use of low-cost pc-board substrates, COB offers not only more density than the conventional strategy, but in some cases lower costs.

The line-width and via-pitch manufacturing limitations of pc-board technology constrains the interconnection density available to COB substrates. COB will be a cost-effective solution for low-performance systems composed of a few chips or chips of low pin count such as memory. For large chips with high I/O counts, fine pitches, and high clock frequencies, MCM substrates offer a better balance of cost and performance.

The impact of packaging and interconnections on a system's clock frequency can be roughly estimated by determining how much they contribute to the propagation delay of a critical net. Considering first-order effects, especially in CMOS circuits, the RC rise time associated with charging the capacitance of interconnection nets increases propagation delay.

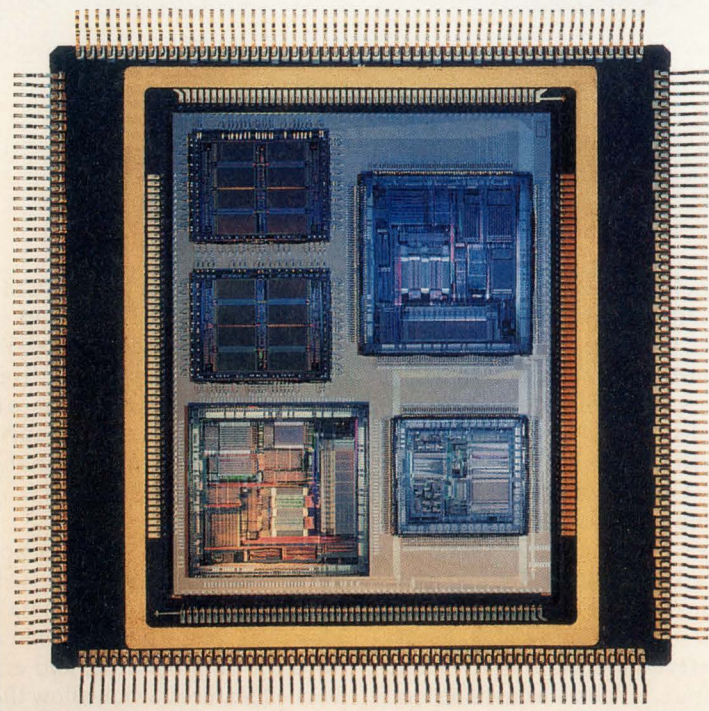
The RC is formed by the resistance of the drivers, which typically is 40 to 80 Ω (as in, for example, the LSI Logic LCA100k gate-array series). It's also formed by the capacitance of the package and interconnection traces. A ceramic-PGA-package trace, for example, has a typical capacitance of about 7 pF.

The capacitance per unit length of a controlled-impedance interconnection can be estimated from the characteristic impedance, Z_0 , and the relative dielectric constant of the insulating material, ϵ_r , using:

$$C_L = \frac{85}{Z_0} \sqrt{\epsilon_r} \text{ (pF/in.)}$$

Therefore, a 50- Ω trace in an FR4 PWB, with a dielectric constant of 5.0, has a capacitance per length of about 3.8 pF/inch.

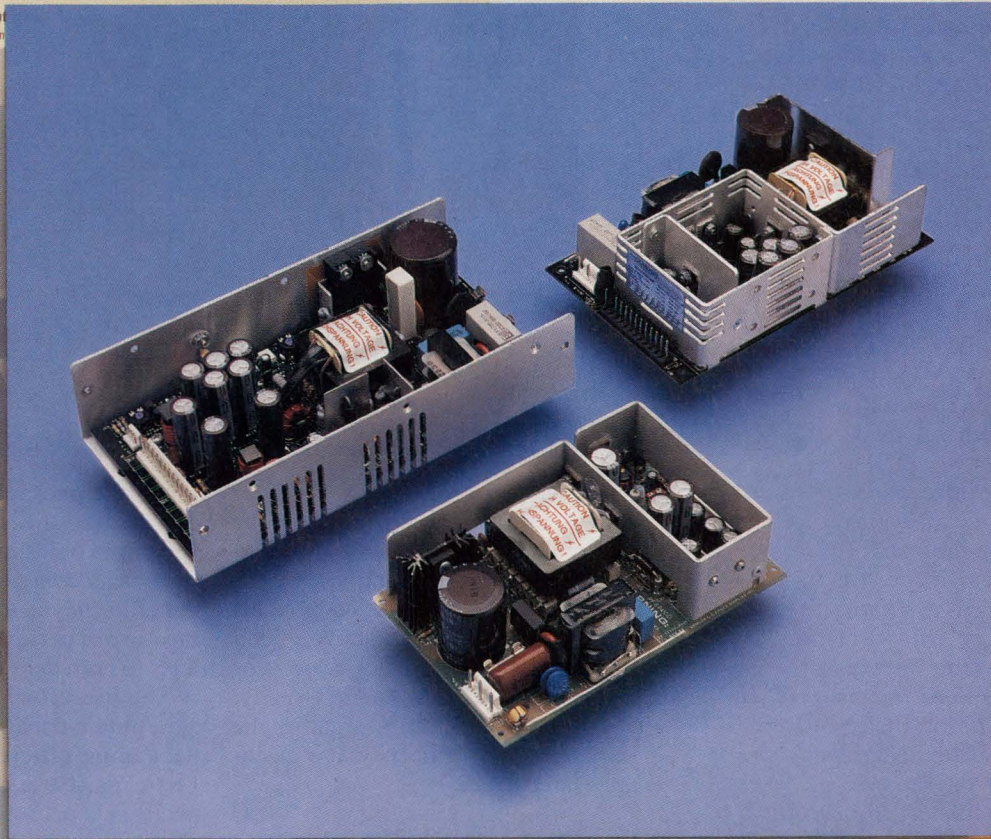
In a typical set of five RISC chips, as shown in Fig. 1, the logic depth for a critical net is about 20. Such a critical net could contain five package traces, and a total interconnection length of about 15 in. In this example, the



3. Shown is a close-up view of a five-chip RISC multichip module. Note the high packaging efficiency that's achieved.

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total load capacitance seen by the off-chip drivers would be $5 \times 7 \text{ pF} + 3.8 \text{ pF/inch} \times 15 \text{ in.} = 92 \text{ pF}$, which means an RC delay of between 3.7 ns and 7.4 ns. This additional "wiring" delay is a result of the packaging and interconnection.

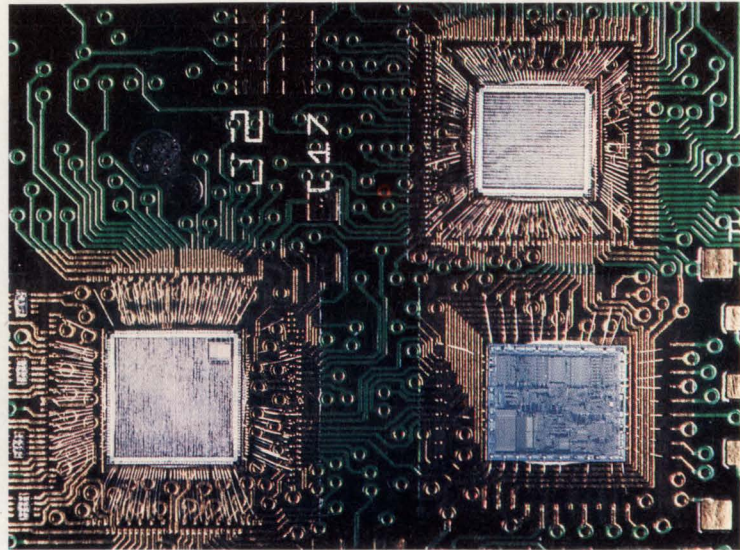
In the 1980s, when clock frequencies were about 10 MHz, the wiring delay might have been only 4 ns out of a total period of 100 ns. In the 1990s, with clock frequencies pushing 50 MHz, the packaging-related wiring delay can make the difference between a 40-MHz system with a period of 25 ns and a 50-MHz system with a clock period of 20 ns.

In an MCM, the interconnection lengths are cut by a typical factor of 5 to 10. In the example shown, the typical interchip lengths are 0.3 in. (Fig. 1, again). With a dielectric constant of 3.75, interconnection capacitance on SiCB substrates is about 3.3 pF/in. The low dielectric constant and short lengths drop the typical interconnection-loading capacitance from almost 100 pF for single-chip packages and boards to $5 \times 0.3 \text{ in.} \times 3.3 \text{ pF/inch} = 5 \text{ pF}$ for the MCM version. The added wiring delay is only 0.2 to 0.4 ns.

Another illustration shows how much the conventional packaging strategy keeps systems from reaching their potential clock frequency compared to the MCM version (Fig. 2). This assumes a conservative wiring delay of 4 ns for the single-chip packaging approach and 0.4 ns for the MCM approach. As VLSI technologies evolve, the limitations posed by single-chip packages and pc boards worsen.

In addition to the RC delays, there are time-of-flight delays, clock skew, and reflection noise, which also reduce the operating system-clock frequency. These problems increase with interconnection length, and are minimized in MCM designs using

4. This illustration shows an example of a chip-on-board (COB) application for a notebook computer (courtesy of Promex).



SiCB substrates.

A useful rule of thumb for the potential performance degradation of a packaging strategy is the "packaging efficiency." This is the ratio of the active silicon area to the total package or board area in a system. Usually, the Greek letter, η , signifies the packaging efficiency. It is calculated from:

$$\eta = \frac{\text{Silicon area}}{\text{Package area}}$$

The packaging efficiency relates not only the density of active silicon area that does the work of information processing, but also the lengths of the interconnections between them, which contributes to wiring delays and slows the system. The

lower the packaging efficiency, the greater the separation between the chips and the greater the wiring delay. Thus, packaging efficiency is a very sensitive measure of performance that relates to both density and speed.

The use of single-chip packages puts intrinsic limits on the packaging efficiency possible. First, consider a peripheral-I/O package. For every pad on the chip, there is a lead on the package, and, typically, every possible peripheral location on the chip is used by a pad. The area of the chip will increase linearly with the square of the chip-pad pitch, P^2_{chip} . The area of the package, which is its footprint, will increase linearly with the square of the package-lead pitch, P^2_{package} . The packaging

COMPARING SUBSTRATES TO ICs

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Line width	125 μm	10 μm	2 μm
Line pitch	825 μm (three track)	25 μm	5 μm
Interconnection density	90 in./in. ² (three track, six signal layers, 50% capacity)	1000 in./in. ² (two signal layers, 50% capacity)	5000 in./in. ² (2 signal layers, 50% capacity)
Via diameter	625 μm	5 μm	1 μm
Via pitch	1250 μm	35 μm	5 μm
Via density	400 in./in. ²	500,000 in./in. ²	2,500,000 in./in. ²
Surface feature	125 μm	10 μm	2 μm

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efficiency for a peripheral package is given by:

$$\eta = \frac{P_{\text{chip}}^2}{P_{\text{package}}^2}$$

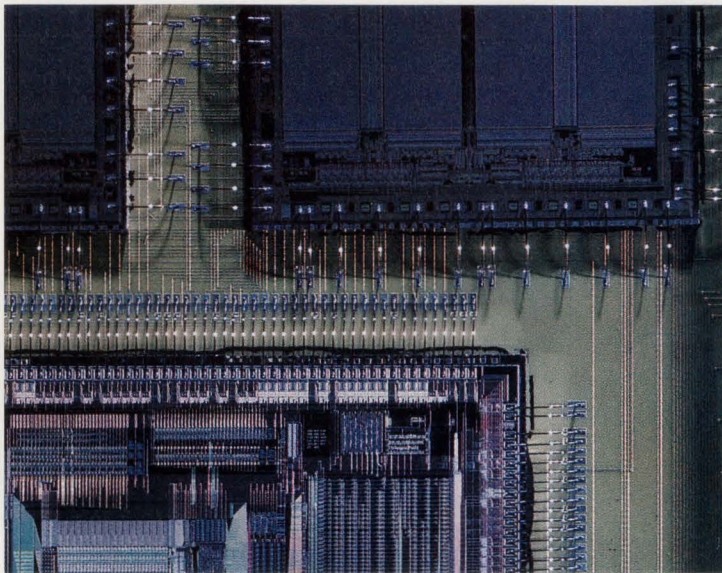
For example, off-the-shelf gate arrays, which are produced in high volume, have a peripheral pitch of 6 mils. They are typically packaged in surface-mounted quad flat packs (QFP) with a peripheral pitch of 25 mils. The packaging efficiency of this combination is less than 6%. If an array of these very-high-density packages were mounted "cheek-to-jowl" on a circuit board, as tightly as possible, the absolute best packaging efficiency for the system would be 6%. The situation is getting worse with next-generation VLSI devices.

Leading-edge ASIC gate arrays use 5-mil pitch, and some (Motorola's MCA3, for example) are at a 4-mil pitch on the chip. At a 4-mil peripheral pitch on the chip, the absolute best packaging efficiency for the leading-edge surface-mounted packages would be only 2.5%. This means that with the conventional packaging strategy, about 97.5% of the board area is devoted to raising the wiring delay, cutting the clock frequency, limiting the performance density, and boosting the overall installed cost. This extremely low packaging efficiency is an intrinsic feature of single-chip packages, which act as a space transformer linking the chip's fine features to the board's coarse features.

In comparison, the packaging efficiency of an MCM can be as high as 50% (Fig. 3). The two chief factors which contribute to the extremely high packaging efficiency are a small footprint for chip attachment and the high interconnection density available to route all the traces required, within the footprint of the chips.

Though COB might improve packaging efficiency compared

5. The fine features in the interconnections on a silicon-circuit-board MCM resemble those on the chips it packages. This close-up view is a 50X magnification.



with single-chip packages, the geometric features and fabrication technology of PWBs constrain both the minimum footprint of the chip on the substrate and the extra area of substrate needed to make the interconnection. This typically limits the packaging efficiency of COB applications to less than 10%.

COB modules are fabricated with conventional PWBs and bare die which are attached with epoxy. Electrical connections are made using tape-automated bonding (TAB) in high-volume applications such as calculators and watches, and by wire bonds in low-volume applications. An illustration shows a close up of three chips wire-bonded to a PWB substrate. The assembly is used in the Poqet notebook-computer application (Fig. 4).

The basic element of a PWB is a layer of glass weave embedded in an epoxy resin. These layers typically are 10 to 50 mils thick. On both sides is laminated copper foil, typically one ounce per square foot in weight, which is about 1.2-mils thick. Dry-film photoresist is laminated on each side and the required conductor traces are left covered by the photoresist after developing.

The exposed copper is etched off in a wet subtractive process.

In general, the finest feature that can be reliably etched by a subtractive process is about five times larger than the thickness of the metal layer. For 1-oz copper, at 1.2 mils thick, the finest feature that can be fabricated is about 6 mils. For 0.5-oz copper, the finest feature is about 3 mils. Most commercial board suppliers can do 6-mil lines and spaces, and more advanced suppliers will do 5-mil lines and spaces for a premium. Only a few merchant vendors worldwide can supply 4-mil lines and spaces.

Electrical connections between layers is accomplished by mechanically drilling holes, which are plated. In a multilayer board, these double-sided layers compose the inner layers. Stacks of multiple inner layers can be laminated together, with B-stage epoxy between them to act both as insulation and the glue to hold the composite structure together. Connections between these layers is by through holes, which are drilled and plated. In this way, multilayer boards with up to 25 conductor signal layers are fabricated.

Conductor traces are routed between the array of through holes, which are on either a 100-

or 50-mil grid. When only one trace can fit between grid points, the board is termed "one track." When two traces per layer can fit between grid points, the board is termed "two track."

Typical multilayer boards used in small computers are two track and are composed of four to eight layers. Large mainframe computers use boards that may contain 20 to 40 layers of two- or three-track types. Of course, the more tracks and layers in a board, the higher the cost. Most COB applications are cost driven and so typically are one or two track, with only two or four layers at most.

The interconnection density available in a substrate is measured in terms of how many inches of trace can be routed per square inch of substrate. In a two-track board with a 100-mil grid of through holes, each signal layer can hold, at most, 20 in./in.². In a board with six signal layers, typical of most workstation products, there would be a maximum possible interconnection density of 120 in./in.².

At best, in most cases, only 50% of this interconnection density is rendered usable by routing constraints. As the number of layers increase, the percentage of usable traces drops because of routing channels being blocked by through holes. In the previous example of a two-track board with six sig-

nal layers, the maximum interconnection density would be 120 in./in.². The practical interconnection density would be closer to 60 in./in.².

In high-density boards, via density further limits interconnection density. On a 100-mil grid, the density is only 100 vias/in.². On a 50-mil grid, only 400 vias/in.² are possible. Pitches finer than 50 mils are difficult to manufacture.

The use of PWBs as substrates for COB was made possible by the introduction of electronic-grade, ionically cleaned epoxy encapsulants. These materials are applied to the chip after it's attached, bonded, and tested to protect it from handling and the environment. With the right selection of material and processing, a "glob-top" coating is as reliable as a hermetic package.

The fabrication of silicon-circuit-board HDI substrates is more like IC manufacturing than COB-substrate manufacturing. This means that performance upgrades and cost reductions for SiCBs will mirror the path of IC manufacturing. In a top-view close-up of a SiCB module, the substrate resembles the ICs it holds (*Fig. 5*).

A cross-section of a typical multilayer SiCB is shown (*Fig. 6*). A standard IC-grade, 5-in. silicon wafer serves as the substrate. The first metal layer is the

ground plane. Deposited on top is a thin layer of a dielectric insulator which, when overcoated by the power plane, acts as a high-capacitance, low-inductance decoupling capacitor. For CMOS devices, simultaneous switching noise is a critical problem. An integrated decoupling capacitor teams with short wire bonds to minimize this noise source.

Two signal layers are constructed with 2- μ m-thick aluminum metal, which can be patterned to as fine as a 10- μ m line width. Signal lines on each layer can be as close as 25 μ m, allowing a maximum of 1000 inches of trace per square inch of substrate (for two signal layers at 50% capacity). This means that virtually all designs can be routed on just two signal layers.

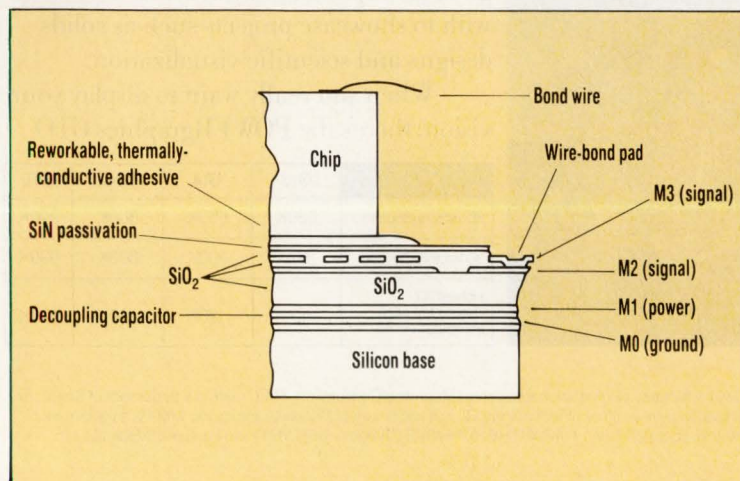
A layer of SiO₂ dielectric separates the metal layers with vias of 5- μ m diameter on a 35- μ m pitch. This via density allows over 500,000 vias per square inch. This is over 1000 times denser than COB substrates.

The top surface is a protective overcoat of SiO₂. Windows are opened to expose bonding pads, which can be on the same pitch as the interconnection traces.

It's possible to compare the features and the interconnection densities possible with advanced COB substrates and early-generation SiCB substrates, with typical IC features (*see the table*). In their infancy, SiCBs offer an interconnection density that's almost an order of magnitude greater than that of COB substrates. If SiCBs continue to reflect the migration path of IC technology, then they have another order-of-magnitude of capability headroom.

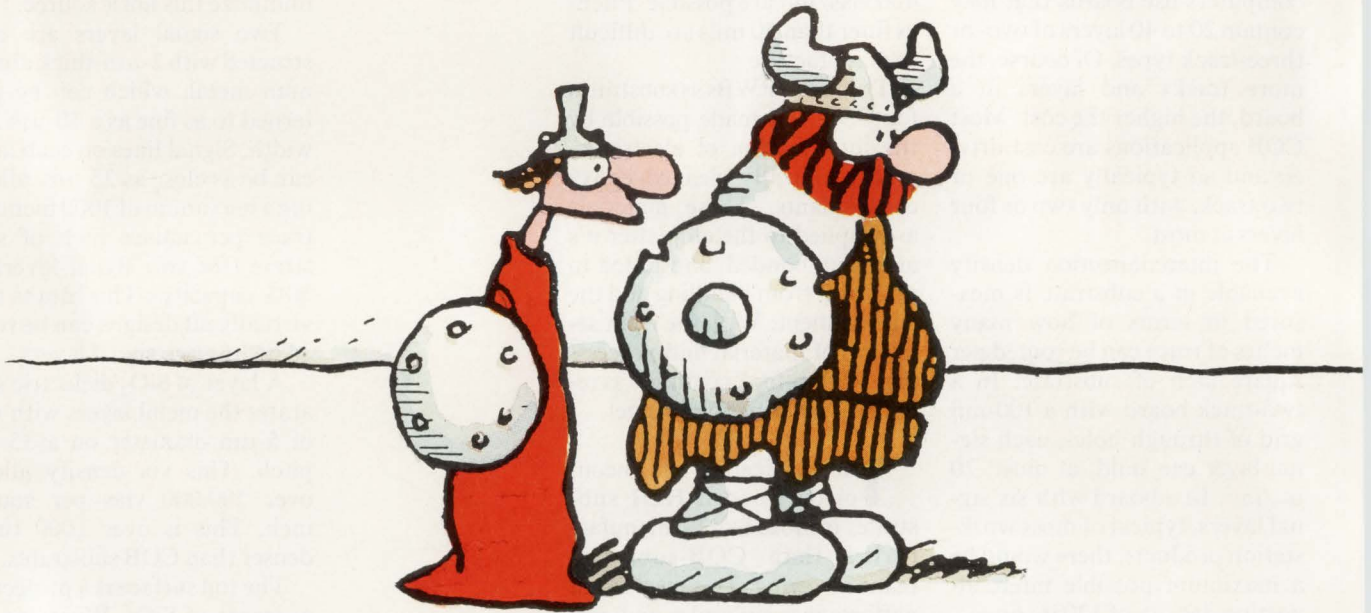
These fine features mean that SiCB modules have the potential for packaging efficiencies typically greater than 50%. What's more, all the nets can be routed on only two signal layers in an area not much greater than that of the die themselves.

The term with the most influ-



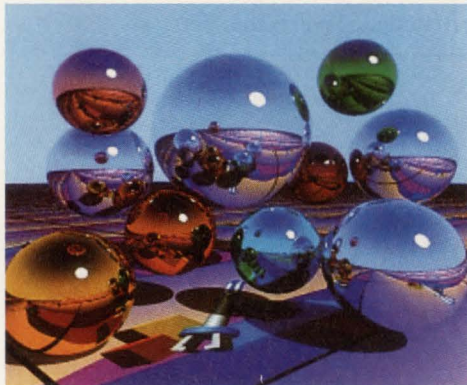
6. Shown in cross section is the make-up of a silicon circuit board.

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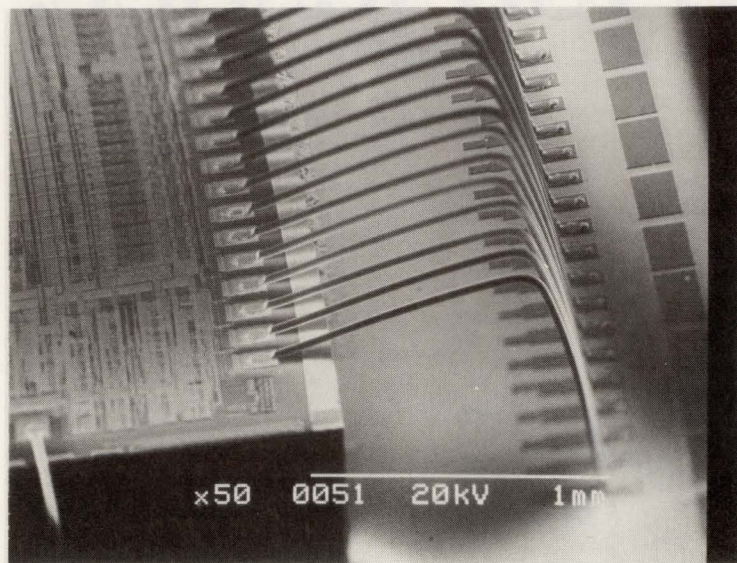
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7. A scanning electron micrograph shows a close-up of the wire bonds between chip and silicon circuit board. The wire bonds are on a 4.5-mil pitch.

ence on clock frequency is interconnection length, which is measured roughly by packaging efficiency. In addition, SiCB substrates have unique features which solve the other three important performance-related problems: minimizing electrical noise, providing adequate thermal management, and ensuring high reliability.

Electronic noise is dominated by simultaneous switching noise, also called ground bounce or delta-I noise, and by loss of signal integrity to impedance discontinuities. Switching noise results from voltage drops across inductance in the ground path, which is caused by output gates discharging the interconnection lines. When this transient voltage appears on the ground line, it's seen by all the gates sharing the ground line and can cause a false output on otherwise quiet drivers.

The magnitude of the ground-bounce voltage, V_{noise} , varies as:

$$V_{noise} \approx L_{bonding} \times \frac{C_{load} \times N_{gates}}{(rise\ time)^2}$$

The bad news is that as the number of simultaneously switching drivers goes up, as happens with wider buses, and edge rates increase, ground-

bounce noise will rise. This is becoming a problem in leading-edge CMOS VLSI devices.

SiCB MCM circuits help solve ground bounce in three ways. The same factors which help shorten wiring delays, low dielectric constant and short lengths, also minimize the interconnection capacitance. This is the primary source of capacitance seen by output drivers. Lower interconnection capacitance will mean lower switching currents and lower ground-bounce voltage.

Second, ground-line inductance is kept to a minimum by allowing very short bonds and low-inductance ground planes. As a general rule of thumb, the self-inductance of a wire bond is about 26 nH/in. The effective inductance of a ground wire will be slightly less because of the mutual inductance of adjacent signal lines. When the substrate's pad pitch is coarser than the chip pad pitch, the resultant fanout can make for long wire bonds. Typical IC pitches are at 6 mils and leading-edge chips are at 5-mil pitch. The pad pitch on COB substrates is typically 10 to 12 mils. For example, some of the wire bonds in the COB example in Fig. 4 are almost 100 mils long.

In comparison, wire bonds on SiCB substrates can be as short as 50 mils. An illustration shows parallel wire bonds between an ASIC chip and a SiCB substrate on a 4.5-mil pitch with no fan out (Fig. 7). The pads on the substrate match the pads on the chip. The worst-case inductance for a ground line would be 1.3 nH for the SiCB wire bonds and 2.6 nH for a COB wire bond.

Finally, solid planes are used to distribute power and ground to the via right at the wire-bond pad. Thus, the only inductance in the ground path is the wire bond's 1.3 nH. As flip-chip assembly is introduced in future merchant SiCB modules, even this 1.3-nH inductance will be decreased significantly.

The internal ground planes in the SiCB also maintain the interconnection signal lines as controlled impedances. Short lines means signal integrity is not compromised. A 1-in. length of interconnection will behave like a lumped capacitance load for rise times greater than 0.4 ns, which might be found in a circuit having a clock frequency of 150 MHz or less. Complex termination schemes are not needed even into the 100-MHz clock-frequency range.

In addition to the manufacturing technology being borrowed from the IC industry, the materials in SiCBs are exactly the same as those in chips. The substrate is silicon, the metalization is aluminum, and the dielectric is SiO_2 . The mix of these materials is well understood, and existing IC processes yield ultra-reliable fabricated structures.

The use of silicon as a substrate allows an exact TCE match to the chips. This is more critical as chip size increases, and as flip chip enters mainstream merchant modules. With no polymers in the structures except the die-attach material, there is little opportunity for water to be absorbed. As a result,

■ HIGH-PERFORMANCE PACKAGING ■

corrosion effects are minimized.

The thermal pathway from the back of the die through the interconnection layers and the silicon base is through high thermal-conductivity materials. The typical thermal resistance of all these layers is $0.17^{\circ}\text{C}/\text{W}\cdot\text{cm}^2$. In addition, the silver-filled epoxy die-attach material contributes a thermal resistance of about $0.2^{\circ}\text{C}/\text{W}\cdot\text{cm}^2$. A 10-W chip of 1 cm on a side, for example, would have a junction-to-case temperature drop of only 3.7°C , which is extremely low.

Thin-film multilayer technology is just now being incorporated in leading-edge systems. Small MCMs based on SiCB technology developed at Lawrence Livermore Labs are still flying in satellites five years later. Ross Technologies has

Conventional packaging of state-of-the-art VLSI chips limits clock frequencies and causes excessive noise, making advanced packaging a necessity.

committed its Sparc chip set to SiCB technologies. IBM recently announced that its new RS/6000 100-MHz RISC chip set would be packaged on a thin-film silicon circuit board.

As the limits of single-chip packages on circuit boards becomes more of a stumbling block and bare-die modules are required, the substrate of choice for fast, high-density circuits will be silicon circuit boards. They'll win out over traditional older technologies because of higher performance density at lower cost per function.

For further reading:

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2. Tummala, R. R., and Rymas-

zewski, E. J., Microelectronics Packaging Handbook, van Nostrand Reinhold, New York, 1989.

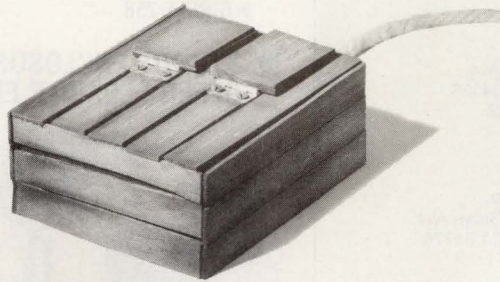
3. Electronic Materials Handbook, Volume 1, Packaging, ASM International, Materials Park, Ohio, 1989.

Eric Bogatin is nChip's director of application engineering and product planning. He holds a BS in physics from the Massachusetts Institute of Technology, Cambridge, and an MS and Ph.D in physics from the University of Arizona, Tucson.

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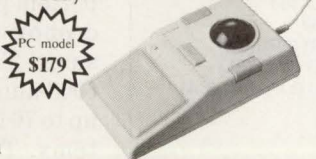


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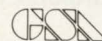
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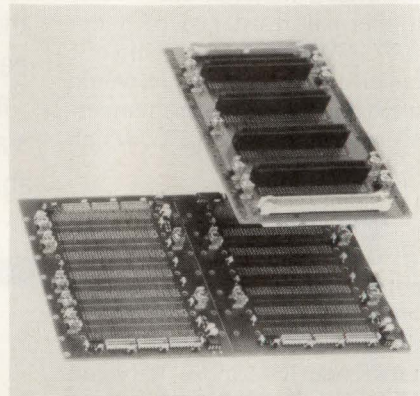
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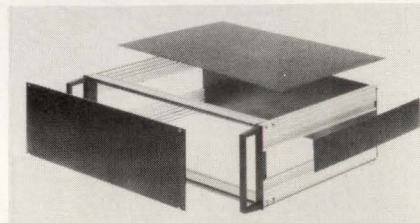
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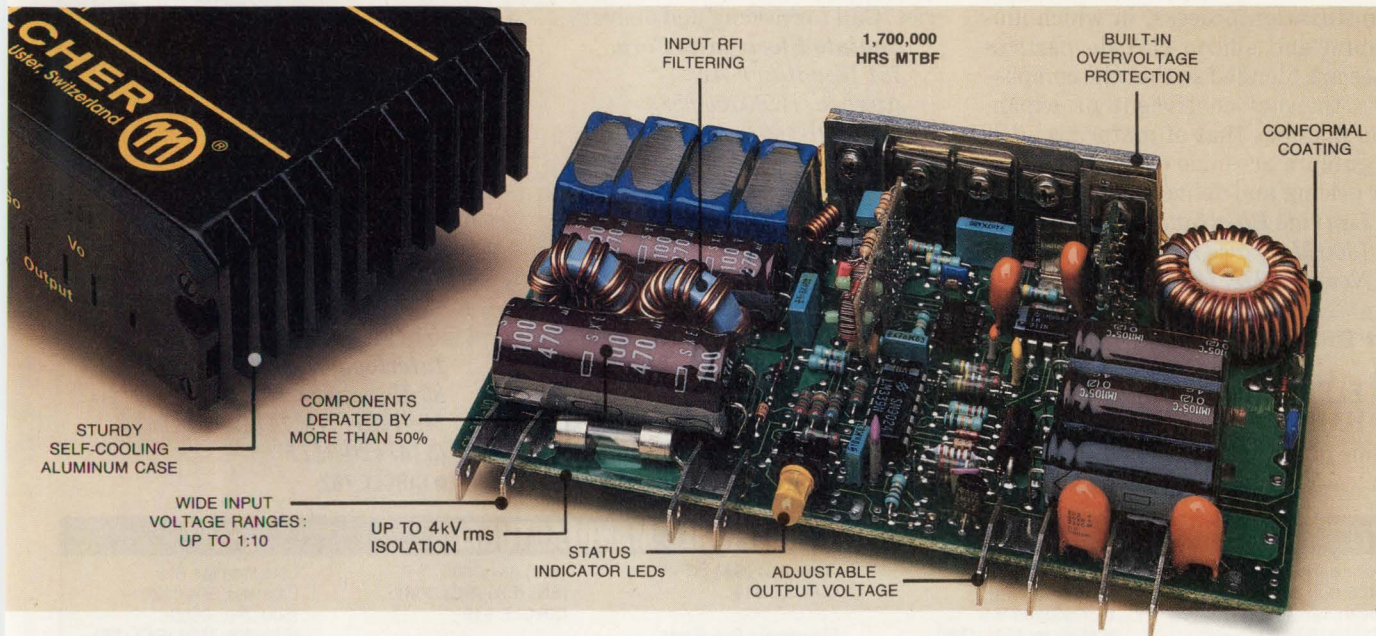


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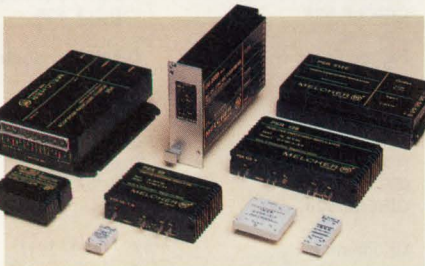
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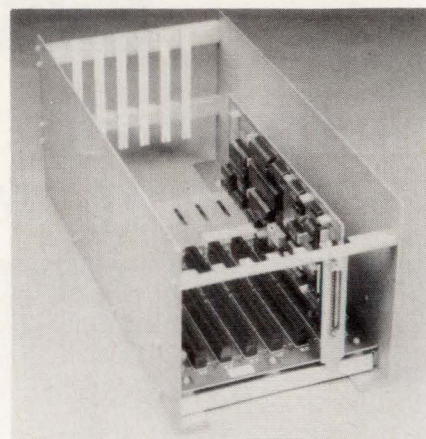
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(503) 476-8871
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(ER)
CIRCLE 607

EG&G Wakefield Engineering
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Wakefield, MA 01880
(617) 245-5900
(EN) (EA)
CIRCLE 608

EMCA-Remex Products
Ablestik Laboratories
160 Commerce Dr.
Montgomeryville, PA 18936
(215) 855-1000
(IK) (PC) (TF)
CIRCLE 609

ERNI Components
520 Southlake Blvd.
Richmond, VA 23236
(804) 794-6367
(GP)
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Electrical Insulation Suppliers
300 N. Mannheim Rd.
Hillside, IL 60162
(708) 547-5400
(ES) (ER) (FR) (GK) (SE) (TB)
(VE) (WN) (CC) (EL) (EN)
(EP) (EA) (FP) (FE) (FL) (IK)
(LA) (MM) (PM) (RE) (SO)
CIRCLE 611

Electro Insulation
3921 Ventura Dr.
Arlington Heights, IL 60004
(708) 632-1020
(ER) (TB) (CC) (EN) (EA) (LA)
(PM) (RE)
CIRCLE 612

Electro-Science Labs Inc.
416 E. Church Rd.
King of Prussia, PA 19406
(215) 272-8000

(EN) (PC) (SA) (TF)
CIRCLE 613

Electronic Solutions
Scanbe
6790 Flanders Dr.
San Diego, CA 92121
(619) 452-9333
(BM) (CM) (EM) (GP) (MP)
(MI) (RA) (ER) (GK)
CIRCLE 614

Elma Electronic Inc.
41440 Christy St.
Fremont, CA 94538
(415) 656-3400
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(RA) (VR) (ER)
CIRCLE 615

Emcor Products/Crenlo Inc.
1600 Fourth Ave. N.W.
Rochester, MN 55901
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(RA) (VR)
CIRCLE 616

Emerson & Cuming Inc.
Div. of W.R. Grace & Co.
77 Dragon Ct.
Woburn, MA 01888
(800) 832-4929
(CC) (EN) (EA) (IK) (PM)
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Enclosure Technologies Inc.
256 Airport Industrial Dr.
Ypsilanti, MI 48198
(313) 481-2200
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(IN) (RA) (VR)
CIRCLE 618

Epoxy Technology Inc.
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Billerica, MA 01821

(508) 667-3805
(EN) (EA) (PC) (PM)
CIRCLE 619

Equipto Electronics Corp.
351 Woodlawn Ave.
Aurora, IL 60506-9988
(708) 897-4691
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Anaheim, CA 92806
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Frenchtown Ceramics Co.
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Frenchtown, NJ 08825
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Fujipoly Inc.
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(908) 272-3850
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Fujitsu Component of America
Component Div.
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San Jose, CA 95054
(408) 922-9000
(ER)
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GE Plastics
Inquiry Handling Service (see p. 117 for key)
(continued on p. 112)

One Plastics Ave.
Pittsfield, MA 01201
(800) 845-0600
(EL) (EP) (FP) (RE) (TF)
CIRCLE 625

GE Silicones
260 Hudson River Rd.
Waterford, NY 12188
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(RE) (SA)
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GEM Inc.
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Escondido, CA 92025
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(GP) (BM) (CN) (PT) (EM)
(MI) (CM)
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Gardiner Solder Co.
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Chicago, IL 60632
(312) 847-0100
(FL) (SO)
CIRCLE 628

General Devices Co. Inc.
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Indianapolis, IN 46239
(317) 897-7000
(GP) (VR) (EM) (MI) (CM)
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► CIRCLE 763

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A range of ATR chassis enables full MIL-spec microcomputer boards to be built into complete systems that

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19428
(215) 825-6050
(EA) (FL) (SO) (TF)
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Hirose Electric USA Inc.
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Simi Valley, CA 93065
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CIRCLE 632

Hoffman Engineering Co.
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Indium Corp. of America
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(315) 768-6400
(SO)
CIRCLE 636

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18327-0136
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(TB) (VE)
CIRCLE 637

Interlogic Industries
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Melville, NY 11747
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North American Industrial Group
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Markel Corp.
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(TB)
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Master Bond Inc.
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Hackensack, NJ 07601
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(SA)
CIRCLE 645

Mereco Technologies
Mereco Products
1505 Main St.
West Warwick, RI 02893
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(RE) (SA)
CIRCLE 646

Meritec
div. of Associated Enterprises
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Painesville, OH 44077
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(CC)
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Olin Hunt Conductive Materials
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Ontario, CA 91761
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Omega Shielding Products Inc.
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Optima EPS
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Tucker, GA 30202
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CIRCLE 654

PacTec
Div. of LaFrance Corp.
Enterprise & Executive Aves.
Philadelphia, PA 19153
(215) 365-8400
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CIRCLE 655

Panduit Corp.
17301 S. Ridgeland Ave.
Tinley Park, IL 60477-0981
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(TB)
CIRCLE 656

Parker Seal
J-B-L Div.
P.O. Box 15009
Spartanburg, SC 29302
(803) 573-7332
(ER) (EL)
CIRCLE 657

Penstock Inc.
520 Mercury Dr.
Sunnyvale, CA 94086-4018
(408) 730-0300
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CIRCLE 658

Permagile Industries Inc.
Insulcast Div.
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Plainview, NY 11803
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CIRCLE 659

Philips Components
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Boulder, CO 80302
(303) 444-1461
(IN)
CIRCLE 671

Premier Metal Products Co.
381 Canal Pl.
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(VR) (ER)
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(MP)
CIRCLE 673

Qualitek International Inc.
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Addison, IL 60101
(708) 628-8083
(FL) (SA) (SO) (TF)
CIRCLE 674

RTP Co.
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Winona, MN 55987
(507) 454-6900
(EL) (EP) (RE)
CIRCLE 675

Radstone Technology Corp.
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(CM) (EM) (MI) (RA) (WT)
CIRCLE 676

Ray Products Co. Inc.
11565 Federal Dr.
El Monte, CA 91731
(818) 579-4250
(CM) (IN) (PT) (ER)
CIRCLE 677

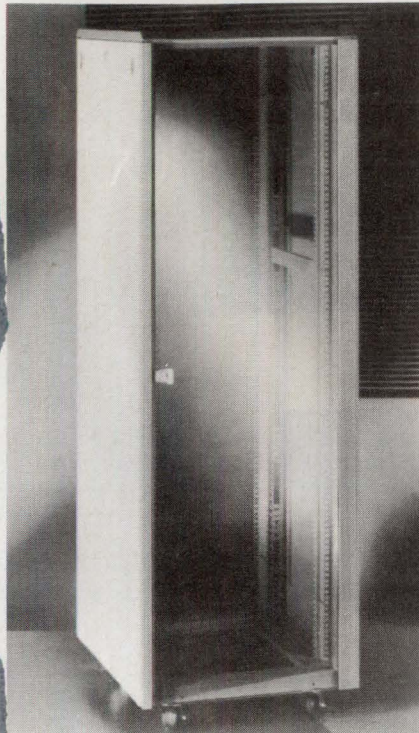
Revere Aerospace Inc.
845 North Colony Rd.
Wallingford, CT 06492
(203) 269-7701
(ER)
CIRCLE 678

Ribbon Cable Co.
8753 Lion St.
Rancho Cucamonga, CA
91730
(714) 987-0007
(ER)
CIRCLE 679

Rittal Corp.
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Springfield, OH 45501
(513) 399-0500
(IN) (PT)
CIRCLE 680

(see p. 117 for key)
(continued on p. 113)

▼ **19-IN. RACK SYSTEM BOOSTS FLEXIBILITY**

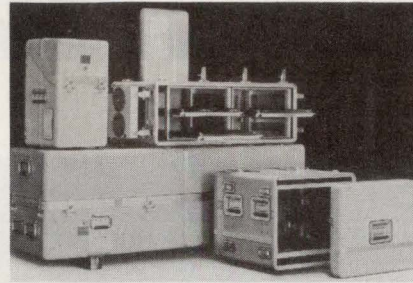


A lightweight, yet very strong frame is offered by the IMRAK 1400 19-in. rack system. The basic structure can take loads up to 500 kg (1100 lbs) while complying fully with IEC 297-2 standards. Three standard depths are offered: 800, 600, and 400 mm.

Heights range from 12U to 57U. Pricing begins at \$750. Delivery is from stock to four weeks.

BICC-VERO Electronics
1000 Sherman Ave.
Hamden, CT 06514
(203) 288-8001
▶ **CIRCLE 765**

▼ **TRANSIT CASES SHRUG OFF HAZARDS**

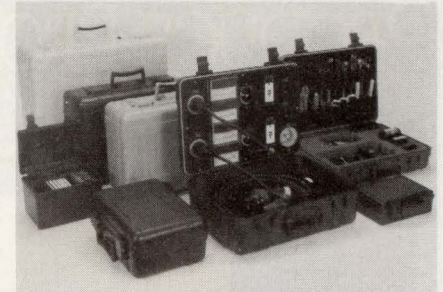


Handling, transportation, and environmental hazards are no problem for a diverse line of transit cases. The compression-molded cases provide high strength-to-weight ratios, resistance to rough handling and projectile impacts, and environmental toughness. Custom applications are available.

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Grants Pass, OR 97526
(503) 476-8871
▶ **CIRCLE 766**

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Underwater Kinetics
1020 Linda Vista Dr.
San Marcos, CA 92069
(619) 744-7560
▶ **CIRCLE 767**

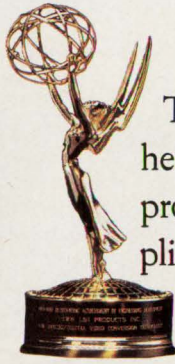
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Robison Electronics Inc. 3580 Sacramento Dr. San Luis Obispo, CA 93403-8121 (805) 544-8000 (PM) CIRCLE 681	Shogyo International Corp. 87 Northern Blvd. Great Neck, NY 11021 (516) 466-0911 (PT) CIRCLE 685	Strongbox P.O. Box 2726 Culver City, CA 90231-2726 (213) 305-8288 (GP) (MI) (CM) CIRCLE 689	(508) 839-5987 (ER) CIRCLE 693	(619) 744-7560 (CM) (EM) (GP) (IN) (MI) (PT) (WT) (ES) (ER) (GK) (VE) (EL) (EP) (RE) CIRCLE 697
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Schroff Inc. 170 Commerce Dr. Warwick, RI 02886 (800) 451-8755 (BM) (CN) (EM) (GP) (IN) (MP) (MI) (PT) (RA) (VR) (ER) CIRCLE 683	Stantron Unit of Zero Corp. 6900 Beck Ave. North Hollywood, CA 91605 (818) 841-1825 (BM) (CN) (IN) (VR) (EM) (MI) (CM) CIRCLE 687	Techmar Corp. 5420 McConnell Ave. Los Angeles, CA 90066 (800) 832-4627 (GP) (IN) CIRCLE 691	Tra-Con Inc. 55 North St. Medford, MA 02155 (617) 391-5550 (CC) (EN) (EP) (EA) (PM) (RE) CIRCLE 695	Vector Electronic Co. 12460 Gladstone Ave. Sylmar, CA 91342 (818) 365-9661 (BM) (CM) (EM) (GP) (IN) (MI) (PT) (ES) (ER) CIRCLE 699
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		Temp-Flex Cable Inc. 11 Depot St. South Grafton, MA 01560	Underwater Kinetics 1020 Linda Vista Dr. San Marcos, CA 92069	

(see p. 117 for key)
(continued on p. 117)

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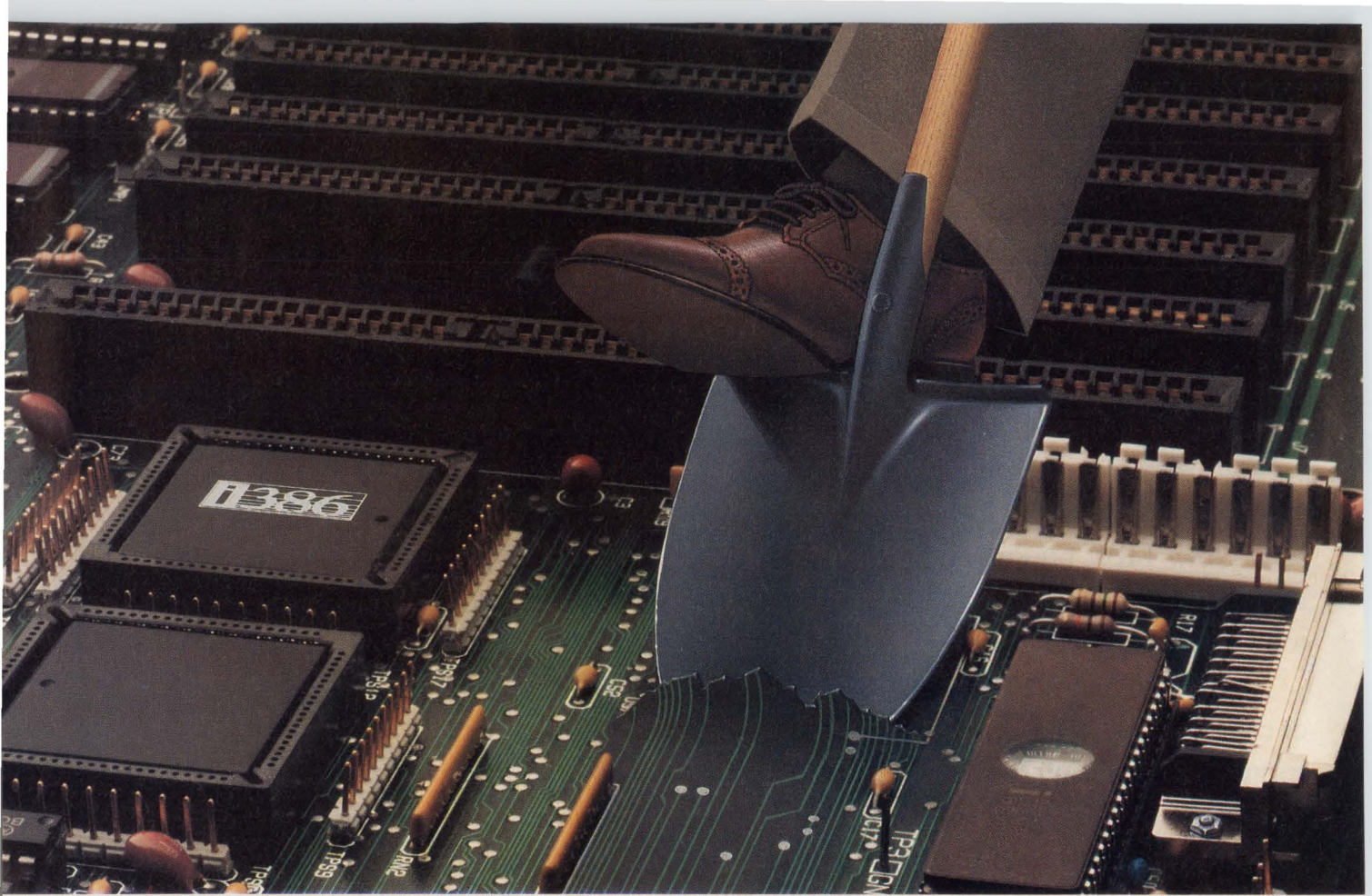
For data sheets, applications and other information on TRW's TMC22090 Video Encoder, as well as to be first in line for coming attractions, call or write today:

TRW LSI Products Inc.,
P.O. Box 2472, La Jolla, CA 92038
(619) 457-1000, FAX (619) 455-6314
(800) TRW-LSIP (800) 879-5747



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So step on it. And call us at **1-800-227-1817, ext. 52** today. We think you're going to really dig it.

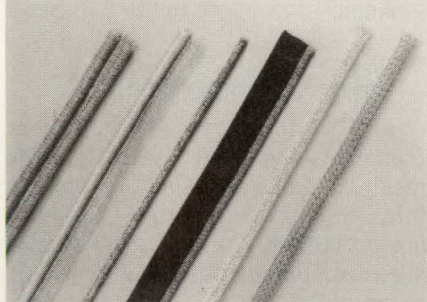


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A line of knitted wire-mesh shielding called ElectroNit offers attenuation as much as 20 dB higher than conventional materials. The shielding fea-



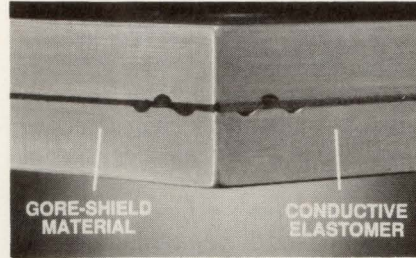
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Delaware Water Gap, PA 18327
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► **CIRCLE 768**

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W.L. Gore & Associates Inc.
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Newark, DE 19714
(302) 738-4880

► **CIRCLE 769**

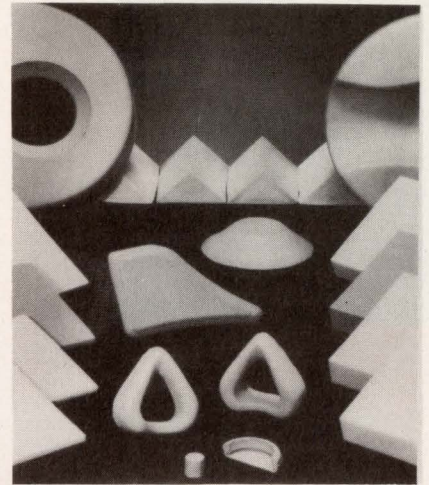
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A packaged assortment of irradiated-polyolefin, heat-shrinkable tubing comes in ten standard military colors. The Rainbow-Pak tubing is shrinkable to 50% and meets Type ST 221 to MIL-I-23053B/5 specifications. Designed for quick identification of cables, bundles, and terminations, the tubing comes in six-in. lengths.

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West Babylon, NY 11704
(516) 249-6150

► **CIRCLE 770**

▼ **ENERGY-EATING FOAMS PROTECT AGAINST SHOCK**



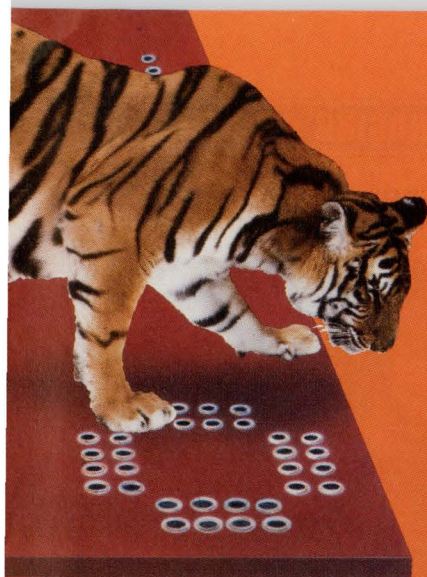
Custom-moldable formulations are now available for the Confor line of ergonomic urethane foams, as well as standard compounds in sheets, buns, or die-cut parts. The conformable foams feature high impact absorption and slow rate of return from deflection for many applications in shock protection, cushioning, and gasketing. Recovery time from shock is adjustable. Call for pricing and delivery.

E-A-R Specialty Composites
7911 Zionsville Rd.
Indianapolis, IN 46268
(317) 872-1111

► **CIRCLE 771**

PACKAGING AND MATERIALS MANUFACTURERS

		KEY		Materials	
Videojet Systems Int'l Inc. 2200 Arthur Ave. Elk Grove Village, IL 60007 (800) 654-4663 (ES) (ER) CIRCLE 701	Wamco Inc. Mingo Loop, P.O. Box 337 Oquossoc, ME 04964-0337 (207) 864-3344 (BM) (CM) (IN) (PT) (RA) (WT) CIRCLE 705	Zero Stantron Zero Enclosures 777 Front St. Burbank, CA 91502 (818) 841-1825 (BM) (CN) (CM) (EM) (GP) (IN) (MI) (RA) (VR) (WT) (ER) (GK) (SE) (EA) CIRCLE 709	(BM) Bench mounted (CN) Consoles (CM) Custom design (EM) EMI/RFI design (GP) General purpose (IN) Instrument cases (MP) Microcircuit packages (MI) Military design (PT) Portable (RA) Racks (VR) Vertical racks (WT) Water tight	(CE) Ceramics (CC) Conformal coatings (EL) Elastomers (EN) Encapsulants (EP) Engineering plastics (EA) Epoxies and adhesives (FP) Films, polyester (FE) Films, polyimide (FL) Fluxes (IK) Inks (LA) Laminates (MM) Magnetic materials (PC) Passivation coatings (PM) Potting materials (RE) Resins (SA) Seals (SO) Solders (SU) Substrates (TF) Thick films	
Vista Performance Polymers 900 Threadneedle Houston, TX 77079 (713) 588-3515 (EP) CIRCLE 702	Wieland Inc. 466 Main St. New Rochelle, NY 10801 (914) 633-0222 (GP) (CM) (GK) (TB) CIRCLE 706	Zippertubing Co. 13000 S. Broadway Los Angeles, CA 90061 (213) 321-3901 (ES) (ER) (MG) (SE) (TB) (EN) (MM) (PM) CIRCLE 710	Shielding (ES) Electrostatic (ER) EMI/RFI (FR) Ferrites (GK) Gaskets (MG) Magnetic (RC) Rooms, chambers (SE) Sheets, strips (TB) Tubing (VE) Vents (WN) Windows		
W. L. Gore Electronics Products Div. 555 Paper Mill Rd. Newark, DE 19711 (302) 738-4880 (GK) (LA) CIRCLE 703	Wilson Case Inc. P.O. Box 1106 Hastings, NB 68901 (402) 463-5040 (IN) CIRCLE 707	Zoltech Corp. 7023 Valjean Ave. Van Nuys, CA 91406 (818) 780-1800 (BM) (CM) (EM) (GP) (IN) (RA) (VR) (ER) CIRCLE 825			
W. L. Gore & Associates Inc. Electronic Products Div. 4755 E. Beautiful Ln. Phoenix, AZ 85044 (602) 438-2017 (ER) (LA) CIRCLE 704	Z Systems Inc. 3080 Olcott St., #110 C Santa Clara, CA 95054 (408) 980-1563 (MP) (SU) CIRCLE 708				

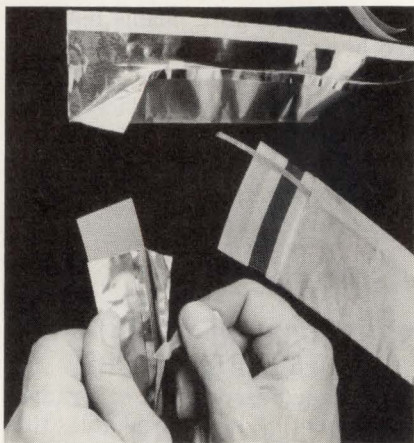


Ready to
make the
jump to
surface
mount?

PACKAGING & MATERIALS

▼ FLAT-CABLE SHIELDING OFFERS 100% COVERAGE

A dual-fold design enables a flat-cable EMI shield to provide 100% coverage for excellent shielding effectiveness. The pre-fold design consistently aligns flat-ribbon cable in the shield for labor savings. The shield can be applied during cable assembly

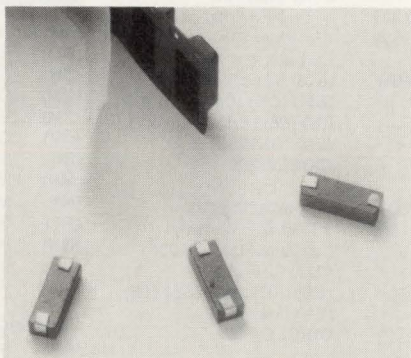


or as a field upgrade to existing units. Composition is a 0.002-in. layer of aluminum and a 0.001-in. layer of polyester film, which is equivalent to 0.001-in. copper foil and performs better at higher frequencies. Call for pricing and delivery.

Temp-Flex Cable Inc.
11 Depot St.
South Grafton, MA 01560
(508) 839-5987

► CIRCLE 772

▼ SMT FERRITE BEADS COME IN TWO SIZES



Two surface-mounted ferrite beads for EMI/RFI suppression come in sizes of 0.335 in. (8.9 mm) and 0.160 in. (4.6 mm). The beads are made of 4S2 ferrite material and offer impedances matching those of the most frequently used tape-and-reeled beads on wire. Construction consists of a piece of flat tinned copper wire

passed through and crimped on the rectangular ferrite bead. Samples are available now. Call for pricing.

Philips Components
5083 Kings Highway
Saugerties, NY 12477
(914) 246-2811

► CIRCLE 773

▼ WOVEN-COPPER SHIELD CONTAINS EMI NOISE

A shielding material that's woven from fine copper wire forms a tight mesh that's highly flexible, yet retains complete continuity of shielding protection. Copper Cloth shielding is combined with an outer jacket to zip onto any cable, round or flat. Types CC-80 and CC-100 have wire counts of 80-by-80 and 100-by-100 per inch, respectively. Call for pricing and delivery.

The Zippertubing Co.
P.O. Box 61129
Los Angeles, CA 90061
(213) 321-3901

► CIRCLE 774

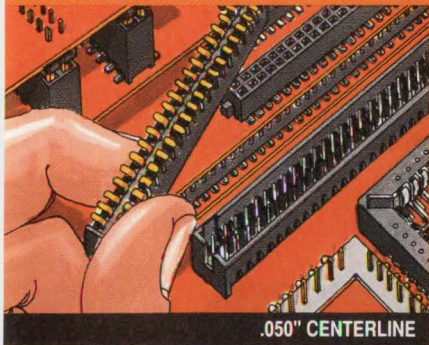
▼ LOW-FORCE EMI GASKETS TERMINATE THEMSELVES



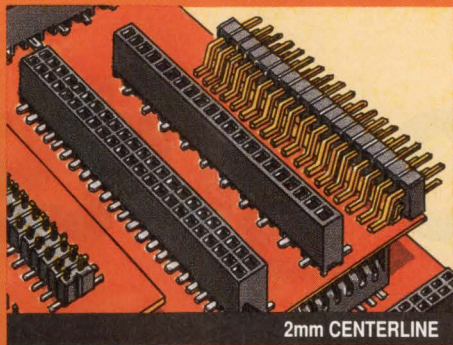
Designed specifically for commercial electronic enclosures, the Soft-Shield II EMI gaskets are self-terminating, low-closure-force devices. The gaskets provide up to 60-dB attenuation from 30 MHz to 1 GHz. A foam core requires a closing force of less than 1 lb/in., which permits more flexibility in enclosure design. Call for pricing and delivery.

Chomerics Inc.
77 Dragon Ct.
Woburn, MA 01888
(617) 935-4850

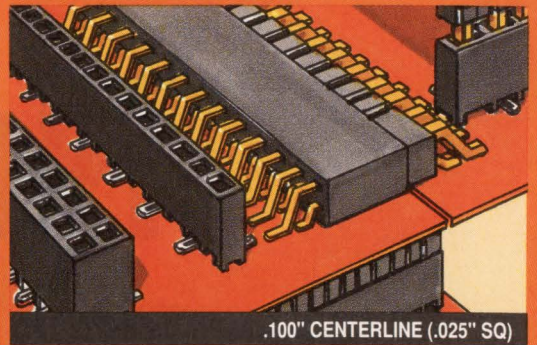
► CIRCLE 775



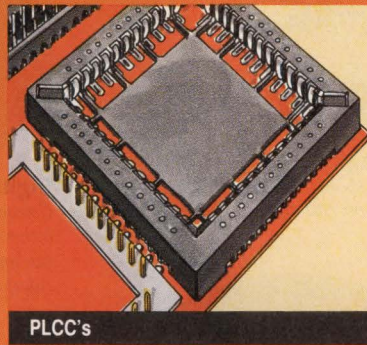
.050" CENTERLINE



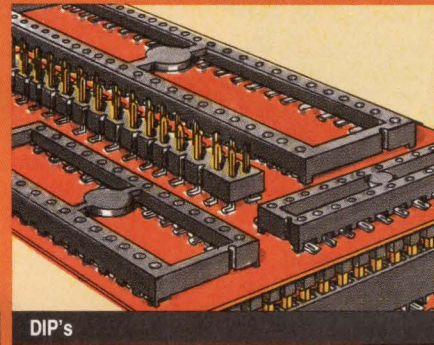
2mm CENTERLINE



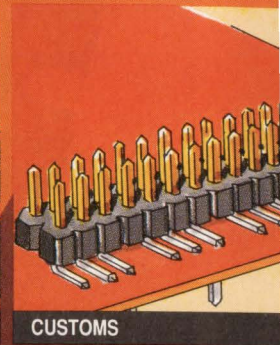
.100" CENTERLINE (.025" SQ)



PLCC's



DIP's



CUSTOMS

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solutions
assure a
safe landing!

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surface mount interconnects
than Samtec.

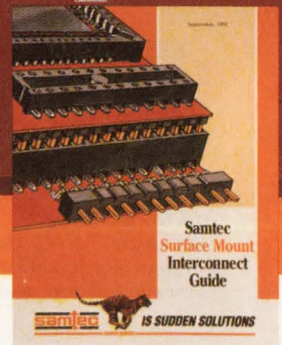
Samtec surface mount Strips, DIP's and PLCC's are designed for automated assembly, VP or IR soldering and to optimize electrical and mechanical properties.

Our new Surface Mount Guide shows thousands of Interconnect solutions. And, if you don't see the solution you need, we'll design one to satisfy your most demanding application. Call today.

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CIRCLE 246 FOR U.S. RESPONSE

CIRCLE 247 FOR RESPONSE OUTSIDE THE U.S.



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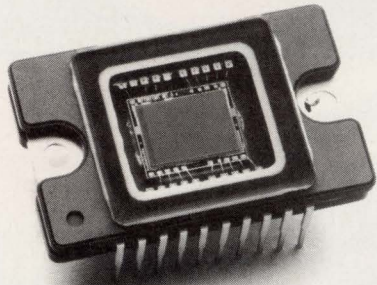
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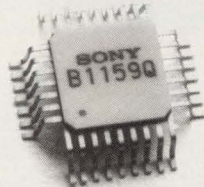
SAMTEC, INC. P.O. Box 1147 • New Albany, IN 47151-1147 USA • Phone 812-944-6733 • Fax 812-948-5047 • TWX 810-540-4095 • Telex 333-918

No guts.



CCD Image Sensors

The CCD technology that led to Sony's leadership in color video cameras is now available to you.



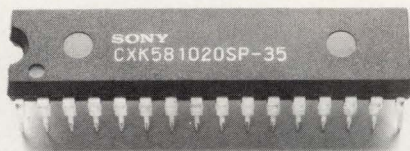
ECL Standard Logic

Wide range of high-speed, high-performance ECL logic devices. Low cost and design simplicity.



Digital Audio

Consumer-based leading-edge technology. Compact design. Small package. Capable of CD-ROM interface.



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Broad family covers all your fast-processor, cache-memory requirements.



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Super high-speed operation combined with low power consumption and extensive I/O interfaces.



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Sony's A/V IC leadership applies directly to new multimedia systems. Superior bipolar linear technology in encoder/decoder.



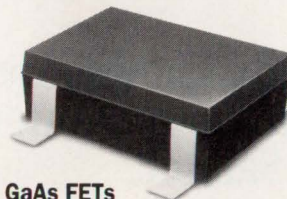
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Largest, most diverse family in the industry. The first products scheduled to come from our new San Antonio fab.



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High speed performance, self-timed RAM with register synchronous SRAM.



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State-of-the-art performance, reliability and uniformity. Ideal when low noise is critical.



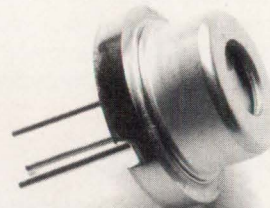
D/A Converters

High speeds to 500 MHz, low glitch energy, and low power consumption in very small packages.



A/D Converters

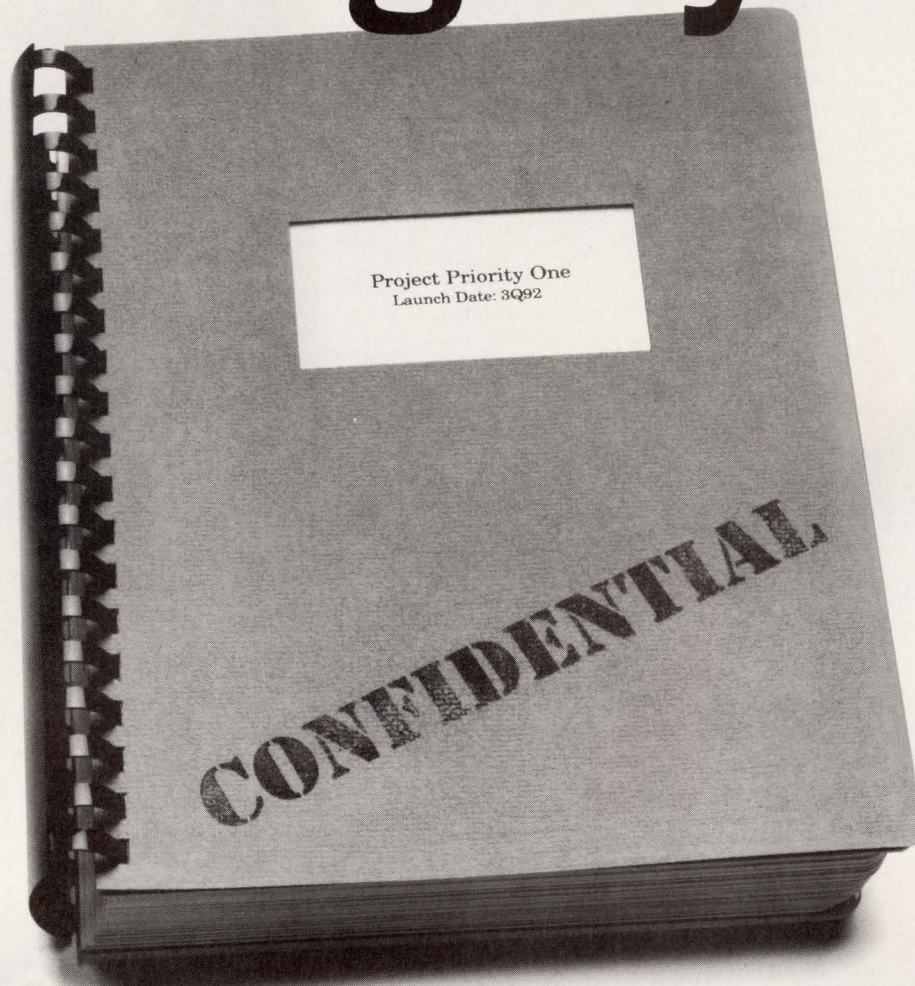
18 models including the world's fastest. Fewer pins, smaller packages, low power consumption, and guaranteed low error rates.



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Wide power range, high reliability, huge selection. Ideal for optical disk, laser printer and microsurgery designs.

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If you can't get the parts you need, you can't get your best designs out the door.

And that's where we can help. With cutting edge SRAMs—high and low speed. With high speed A/D and D/A converters. With high speed ECL logic chips. And with a long list of other components—the same components that have made Sony's consumer electronics so successful.

Perhaps more important, we're always here to help. With a design center to support your design engineers, in developing applications all the way through

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To learn more about our custom design support, our competitive prices, and our full line of components, just call us today at (714) 229-4331 or (416) 499-1414 in Canada. You can even FAX us your current requirements at (714) 229-4285 or (416) 499-8290 in Canada.

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Sony Canada, 411 Gordon Baker Road, Willowdale, Ontario M2H 2S6.

CIRCLE 258 FOR U.S. RESPONSE

CIRCLE 259 FOR RESPONSE OUTSIDE THE U.S.

CONDITIONED "FRONT END" POWER

RUGGED AC-DC OFF LINE SOURCES



AC INPUTS
1 ϕ and 3 ϕ available

- True N+1 current sharing for loads to kilowatts.
- .99 power factor correction – provides 25% more usable power with low harmonic distortion.
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24 to 300V available
(including 28V, 48V, 155V, 270V)

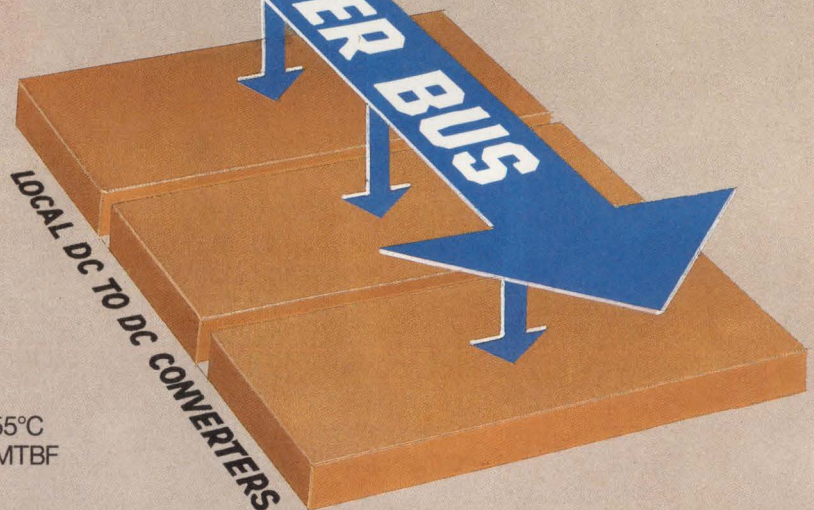


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**IDEAL FOR USE
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DC-DC CONVERTERS AND SYSTEMS**

Features include 600 watt low profile 2" high package; lightweight, unpotted designs; environmental performance to Mil-Std-810D; -55°C to +85°C operation without derating; extended MTBF greater than 350,000 hours...

Call **toll free** for additional technical information and application assistance **1-800-421-8181** (in California 805/484-4221)



ARNOLD MAGNETICS CORPORATION

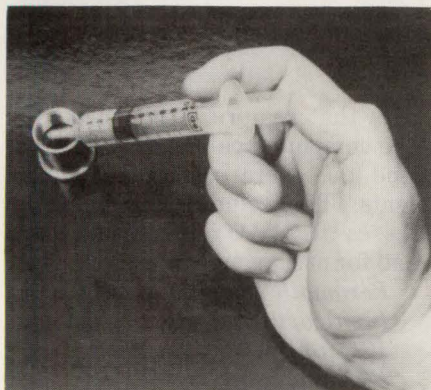
4000 Via Pescador, Camarillo, California 93012 • Phone: (805) 484-4221 • Fax: (805) 484-4113

CIRCLE 100 FOR U.S. RESPONSE

CIRCLE 101 FOR RESPONSE OUTSIDE THE U.S.

▼ **POTTING COMPOUND OFFERS LOW VISCOSITY**

A thermally conductive, electrically insulating epoxy system performs well in casting, potting, and encapsulation applications. The EP30AO system, which cures at room temperature or faster at elevated temperatures, has an exceptionally low viscosity. The material is available in



quantities from pints to five-gallon pails. Call for pricing and delivery.

Master Bond Inc.
154 Hobart St.
Hackensack, NJ 07601
(201) 343-8983
► CIRCLE 776

▼ **HYBRID ENCAPSULANTS KEEP LEAKAGE LOW**

Low, stable leakage currents are maintained in severe environments by the Rely-Imide 600 series of hybrid encapsulants. The materials, which are designed for coating thick- and thin-film hybrid circuits, feature moisture resistance, stress relief, and protection against high-voltage breakdown. Call for pricing and delivery.

Ablestik Laboratories
20021 Susana Rd.
Rancho Dominguez, CA 90221
(213) 764-4600
► CIRCLE 777

▼ **SILICON SUBSTRATES USE THIN-FILM PROCESS**

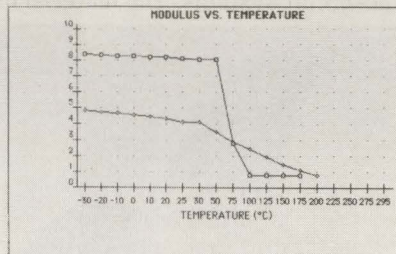
Advanced thin-film processing techniques are used to produce silicon microsystem substrates for hybrids and multichip modules. The substrates combine high-density interconnections with precision passive components. Unencapsulated IC die can be mounted directly on the substrates and wire-bonded to it. Features include up to five layers of in-

terconnections, standard pitches of less than 2 mils, and total routing density of over 1000 lines/in. Call for pricing and delivery.

Z Systems Inc.
3080 Olcott St., #110C
Santa Clara, CA 95054
(408) 980-1563
► CIRCLE 778

▼ **DIE-ATTACH ADHESIVE HAS LOW MODULUS**

A silver-filled, electrically conductive adhesive is designed for bonding large chips to substrates in a manner that reduces stress. The K/5022-81 adhesive features a low modulus and a very high glass-transition temperature of over 225°C. This combination



of properties is a necessity for wire bonding at high temperatures. Call for pricing and delivery.

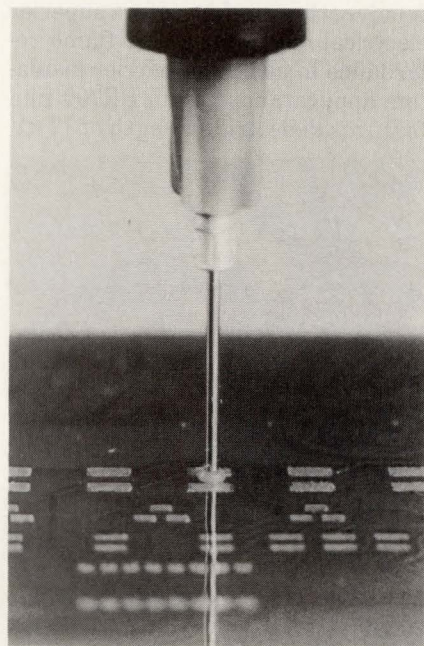
Epoxy Technology Inc.
14 Fortune Dr.
Billerica, MA 01821
(800) 227-2201
► CIRCLE 779

▼ **AQUEOUS SOLDER MASK IS SCREEN PRINTABLE**

A photodefinable, fully aqueous solder mask is available that can be applied with conventional screen printing. The PC 801 solder mask achieves high definition and complete encapsulation of dense circuits while taking advantage of the speed and economy of screen printing. The single-part, epoxy-based photopolymer is for use over bare copper and tin-lead. Excellent adhesion is featured to all areas of the circuit board as is uniform, skip-free encapsulation of the circuitry. Call for pricing and delivery.

AMP-AKZO Electronic Materials
710 Dawson Dr.
Newark, DE 19713
(302) 292-6242
► CIRCLE 780

▼ **ACRYLIC ADHESIVE MEETS SMT NEEDS**



A single-part acrylic adhesive is formulated specifically for the requirements of surface-mounted assembly. SMD Adhesive 881 offers excellent green strength, high dot profile, 24-hour open time, a low minimum curing temperature, and long shelf life. The adhesive can be dispensed by hand, machine, or screen printed. Components are held securely during placement and transport. The non-migrating adhesive has excellent resistivity. Call for pricing and delivery.

Multicore Solders
Cantiague Rock Rd.
Westbury, NY 11590
(516) 334-7997
► CIRCLE 781

▼ **UV-CURABLE INKS COME IN MANY COLORS**

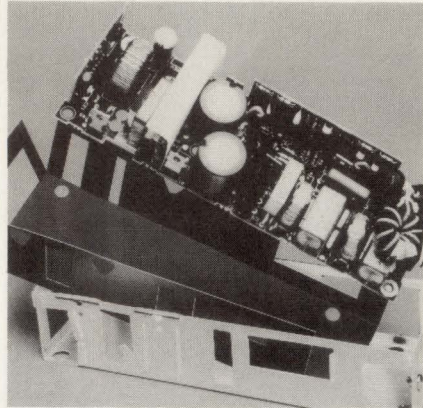
A broad selection of colors is available in the 100 Series of UV-curable, one-component marking inks for products or components. The inks can be applied with standard marking equipment and feature high bond strength and rapid curing (typically 2 seconds or less). Formulations conform to EIA Standard RS359. Call for pricing and delivery.

UVEXS Inc.
580 N. Pastoria Ave.
Sunnyvale, CA 94086
(408) 737-7100
► CIRCLE 782

MATERIALS

▼ POLYCARBONATE FILM WON'T BURN EASILY

A polycarbonate film offers superior electrical capabilities and flame retardance in electrical-barrier insulation applications. Lexan FR700 film features dielectric strength of 17 kV



at 10-mil thickness and low water absorption of 0.28%. Glass-transition temperature is 156°C. The film is easily fabricated in applications calling for sharp folds or die-cut shapes. Call for pricing and delivery.

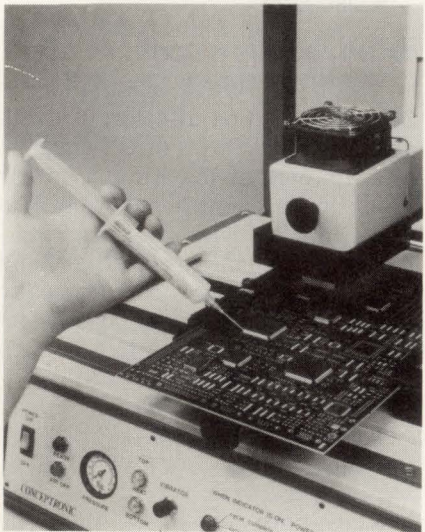
GE Plastics

*Inquiry Handling Service
PR #43-91
One Plastics Ave.
Pittsfield, MA 01201
(800) 451-3147*

► CIRCLE 783

▼ REWORK FLUX RESOLDERS OPENS, SHORTS

A rework flux is designed to reduce the time and effort involved in resoldering opens or shorts on pc boards with SMT components. Series SF33 flux is designed to last until the re-



work is finished. It won't pull back, shrink, evaporate, discolor, char, or burn. Only a hard, clear residue is left behind that requires no solvent cleaning. Pricing is \$20 and \$37 for 5-cc and 10-cc syringes, respectively. Delivery is from stock.

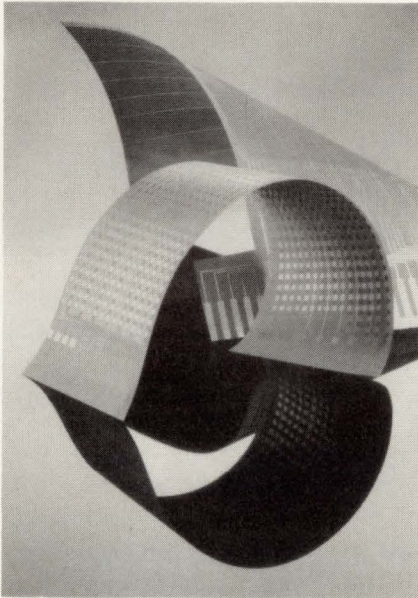
Heraeus Inc.

*Cermalloy Division
24 Union Hill Rd.
West Conshohocken, PA 19428
(215) 825-6050*

► CIRCLE 784

▼ FLEX-CIRCUIT LAMINATE OVERCOMES SHIFTING

A proprietary adhesive helps Gore-Clad flexible-circuit laminate to overcome material shifts and temperature limitations of other flexible-circuit systems. The material of-



fers tight control of X-Y thermal-expansion coefficients, which reduces the movement of material to less than half that of other laminates. Gore-Clad laminates cost from \$20 to \$50 per square foot depending on construction and volumes. Call for samples.

W.L. Gore & Associates

*555 Paper Mill Rd.
Newark, DE 19714
(302) 738-4880*

► CIRCLE 785

▼ POTTING COMPOUND DISPERSES HEAT WELL

Specifically engineered to a thermal conductivity of 7 BTUs, the RTVS 27 HTC silicone compound is well suited to potting dense component pack-



ages that require heat dissipation. The compound can significantly extend the operating life of components. The color-coded compound passes UL 94V-O flammability tests. Call for pricing and delivery.

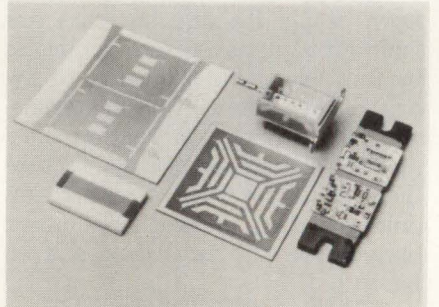
Permagile Industries Inc.

*Insulcast Division
101 Commercial St.
Plainview, NY 11803
(800) 645-7546*

► CIRCLE 786

▼ HYBRID SUBSTRATES ARE TAILORED TO NEEDS

Three improved grades of beryllia ceramic substrates are available, each tailored to a specific performance level of thin-film hybrid circuits. Thermalox 995 now comes in



larger standard sizes up to 3 in.² with flatness of 0.003 in./in. Thermalox 995T is a significant upgrade that offers an ultra-smooth surface of 2 to 4 μin. CLA with minimal surface inconsistencies. Maximum flatness is 0.005 in./in. Thermalstrates BW2000 is a tape-cast ceramic product with a smoother, more predictable surface finish than previous cast grades of the material. Call for pricing and delivery.

Brush Wellman Inc.

*6100 Tucson Blvd.
Tucson, AZ 85706
(602) 746-0251*

► CIRCLE 787

BEST OF THE '90s

NKK backs you with over 1,001,250 different toggle, rocker, pushbutton, slide, lighted, keypad, keylock, rotary and DIP rotary switches — including the best new ideas of the '90s. See them all in the pages of our new 456-page switch catalog. For your free copy, call (602) 991-0942 or FAX (602) 998-1435.

NKK Switches
7850 E. Gelding Dr.
Scottsdale, AZ 85260

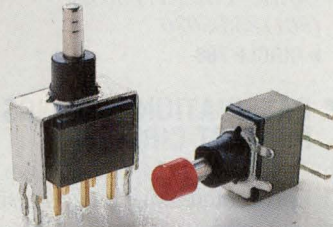
NKK switches

WORLD'S SMALLEST



NKK introduces the surface mount G3T with patented STC contacts, gull-wing terminals. VPS or infrared reflow solderable.

EASY DOES IT



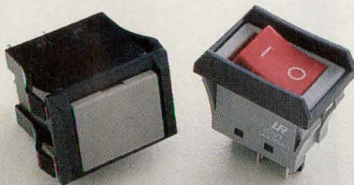
Washable M2B subminiature pushbuttons feature very-light-touch, snap-acting contacts. Straight, right angle, vertical PC terminals.

ULTRA-MINI



New ND switch is half the size of ordinary binary coded DIP rotaries. Washable and universal footprint pattern.

TV STAR



JW rockers & JP pushbuttons. High inrush current resistance protects against contact welding. TV-8 (16 Amp) + TV-5 (10 Amp) Rated.

40TH YEAR of Innovation

WORTH A MILLION



Million operations from unique LED illuminated JB keypad switch. Red, green or yellow LED options.

DOUBLE DUTY



Logic-level for PCB or power rating for snap-in panel mounting, from very low-profile UB pushbuttons with full-face LED illumination.

TURNING POINT



Washable Binary Coded DIP rotary DR-A switch can be PC or panel mounted. Crisp operation. Right angle or straight terminals.

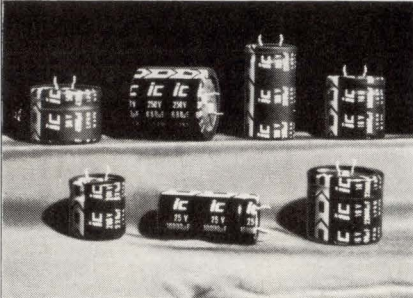
100,000 CHOICES



YB pushbutton yields literally 100,000+ part numbers with variations in mounting, illumination, circuitry and color.

ic[®] LBA/LMU

Snap-Mount Aluminum Electrolytic Capacitors



Proven Reliability ...100% Burn-In Tested

- LBA 300 Mfd. to 1,800 Mfd.
LMU 300 Mfd. to 1,500 Mfd.
- 200 WVDC to 400 WVDC
- LBA -40°C to +85°C
LMU -40°C to +105°C
- ±20% Std. (±10% (K) Opt.
or -10%, +30% (Q) Opt.)
- Low ESR, Low Impedance
- Solvent Tolerant Seal Std.

ic[®] TECH TIPS

Type LBA and Type LMU Snap Mount electrolytic capacitors offer extremely high CV density and have very long operating life. The Low ESR design allows for operation at maximum rated ripple current levels, enabling the designer to streamline circuitry with fewer devices. The modern rugged Snap Mount design allows quick and efficient attachment to a printed circuit board. These rugged capacitors are perfect for the latest design filters in both conventional and switch mode power supplies. Designed with welded terminations, low ESR and low inherent inductance. Types LBA and LMU provide the range of configuration for present and future designs.

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Performance and Delivery.

ic[®] ILLINOIS CAPACITOR, INC.

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Lincolnwood, Illinois 60645
(708) 675-1760
Fax (708) 673-2850

CIRCLE 176 FOR U.S. RESPONSE

CIRCLE 177 FOR RESPONSE OUTSIDE THE U.S.

MATERIALS

▼ COPPER-CLAD LAMINATES USE LOW PRESSURE

A line of polyester-epoxy, copper-clad laminates uses a low-pressure laminating process. The result is a laminate with superior electrical characteristics compared with FR4, CEM-1, or FR2. The MC2 material replaces CEM-1, and MC# replaces FR4. Call for pricing and delivery.

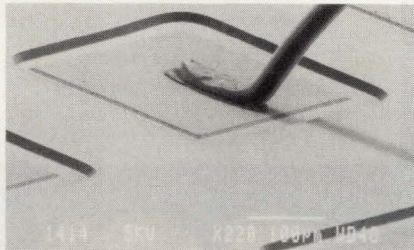
Glasteel Industrial Laminates

P.O. Box 910
Collierville, TN 38017
(901) 853-5070

► CIRCLE 788

▼ PASSIVATION COATINGS PROTECT CIRCUITRY

The Ultradel 1414 passivation coatings protect sensitive microcircuitry against moisture, particulates, and



mechanical damage during wafer handling and assembly operations. The coatings feature low modulus, low moisture absorption, and excellent adhesion to a variety of substrates. Call for pricing and delivery.

Amoco Chemical Co.

200 E. Randolph Dr.
Chicago, IL 60601-7125
(312) 856-3200

► CIRCLE 789

▼ THERMOPLASTIC POLYMERS BOAST HIGH PERFORMANCE

A range of high-performance characteristics at more attractive cost than competing materials is offered by the Suprel SVA family of thermoplastic polymers. The polymers are designed for injection molding in consumer electronics, telecommunications, electrical enclosures, instrument housings, computer enclosures, and more. The inherently flame-retardant materials offer high impact strength and good looks. Call for pricing and delivery.

Vista Chemical Co.

900 Threadneedle
Houston, TX 77079-2990
(713) 588-3000

► CIRCLE 790

▼ SMT SOLDER PASTES ELIMINATE CFC SOLVENTS



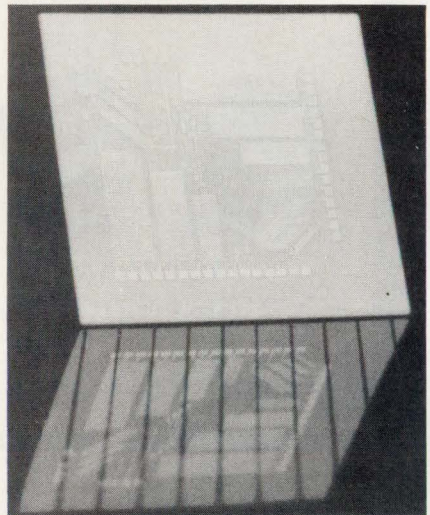
Two solder pastes, one water-soluble and the other a no-clean type, are designed to eliminate CFC solvents from pc-board processing. The WMA-SMQ (R)60 water-soluble solder paste contains no organic acids, which are corrosive and conductive. The NC-SMQ70 series of no-clean pastes has no halides for long-term reliability. Both can be used in fine-pitch stencil printing.

Indium Corp. of America

P.O. Box 269
Utica, NY 13503
(315) 797-1630

► CIRCLE 791

▼ GOLD CONDUCTOR FILLS CERMET PASTE



The Multisyst 3261 cermet paste is a high-density, thin-printing gold conductor that's compatible with the company's other conductors, resistors, and dielectric materials. All are designed to fire in an 850°C profile. The 3261 conductor incorporates a gold powder that guarantees lot-to-lot reproducibility.

EMCA-REMEX Products

160 Commerce Dr.
Montgomeryville, PA 18936
(215) 855-1000

► CIRCLE 792

OUR SALES ARE UP!

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REASON NO.1:

The *largest* line of enclosures in the industry . . . meeting *any* need.

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Local inventory and support means *fast* service and delivery from our nationwide network of the *finest* distributors.



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Bud East, Inc.
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Willoughby, Ohio 44094
(216) 946-3200
FAX: 216-951-4015

BUD
Bud Industries, Inc.

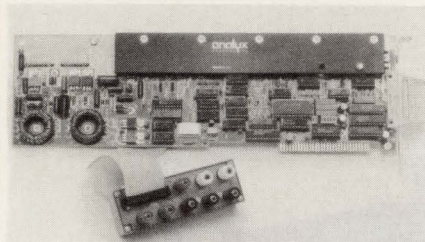
Bud West, Inc.
7733 West Olive Avenue
P.O. Box 1029
Peoria, Arizona 85345-0350
(602) 979-0300
FAX: 602-878-5371

CIRCLE 120 FOR U.S. RESPONSE

CIRCLE 121 FOR RESPONSE OUTSIDE THE U.S.

▼ **ATE POWER SUPPLY DRIVES PC-BASED TEST**

A programmable power supply for ATE applications can be installed in PC AT- or EISA-based test systems. Unlike typical IEEE-488-style DUT supplies, the ATEPS-1606 supply is a triple-output unit that's totally con-



tained within the PC. The supply can simultaneously deliver zero to +6 V at from zero to 2 A and two independently programmable bipolar outputs of -15.75 to +15.75 V at zero to 200 mA each. Single quantities cost \$995 including software. Delivery is from stock.

Analyx Systems Inc.
P.O. Box 14644
Fremont, CA 94539
(415) 656-8017

► **CIRCLE 793**

▼ **WIDE-INPUT CONVERTERS REGULATE THEIR OUTPUT**



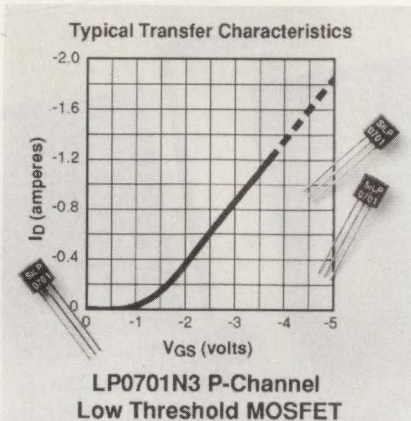
Not only do the CA Series dc-dc converters accept inputs from 9 to 36 V dc and 20 to 72 V dc, but they also regulate up to 12 W of power per cubic inch from a standard 3-by-3-by-0.375-in. case. The units perform over a 4:1 voltage range while delivering 5-, 12-, and 15-V dc outputs in single, dual, and triple combinations. An LC input filter keeps reflected ripple low. Pricing is about \$85 in lots of 100. Small quantities are available from stock.

Wall Industries Inc.
5 Watson Brook Ct.
Exeter, NH 03833
(800) 321-WALL

► **CIRCLE 794**

▼ **P-CHANNEL MOSFET HAS 1-V GATE THRESHOLD**

The industry's first p-channel, enhancement-mode MOSFET with a maximum gate threshold of 1 V is the LP0701. The unit comes in the TO-92 package (LP0701N3) and in die form (LP0701ND) and has a drain-to-source breakdown voltage of 16.5 V.



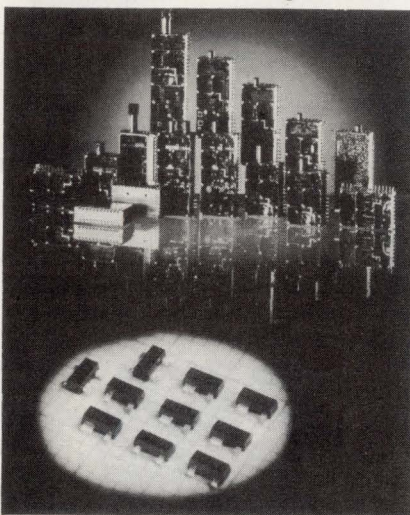
Drain-to-source on resistance is guaranteed at 1.5 Ω maximum at a V_{GS} of 5 V and I_D of 300 mA. Applications include circuits using high-side switches, push-pull logic, or 5-V logic levels interfacing with high voltages. The TO-92 version costs \$0.70 in lots of 1000. Samples are available from stock.

Supertex Inc.
1350 Bordeaux Dr.
Sunnyvale, CA 94089
(408) 744-0100

► **CIRCLE 826**

▼ **DUAL-GATE MOSFET DROPS INTO TUNERS**

Working in both UHF and VHF tuners, the BF998 low-noise, dual-gate MOSFET combines a high transfer



admittance of 24 ms with a low 2.1-pF input capacitance. The device reduces loading on the band filter that feeds it, making it simple to design into pre-stages of TV tuners, radio receivers, and other communication equipment. The depletion-type tetra-rod serves as a gain-controlled amplifier up to 1 GHz and accepts a 12-V supply. Call for pricing and delivery.

Philips Components
Discrete Products Division
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404
(407) 881-3308

► **CIRCLE 795**

▼ **POWER MOSFETS COME IN SO PACKAGES**

Two additions have joined the Little Foot family of power MOSFETs in small-outline (SO) packages. The Si9942DY and Si9959DY will be used in low-voltage motor-control applications in disk, tape, and optical drives. The Si9959DY contains two 50-V n-channel MOSFETs rated at 0.3 Ω and 2 A. The Si9942DY contains an n- and a p-channel MOSFET, each rated at 20 V. The n-channel device is rated at 0.125 Ω and 3 A, and the p-channel device is rated at 0.2 Ω and 2.5 A. In lots of 100,000, the Si9942DY and Si9959DY go for \$0.87 and \$0.74, respectively. Samples are available now and production lots are delivered from stock to four weeks.

Siliconix Inc.
2201 Laurelwood Rd.
Santa Clara, CA 95054
(408) 988-8000

► **CIRCLE 796**

▼ **9-V LITHIUM BATTERY LASTS UP TO 10 YEARS**

A life expectancy of up to 10 years is featured in the model CR 9-V LiMnO₂ battery. The 950-mAh hard-cased battery is built from cells with 25% more energy density than conventionally built LiMnO₂ batteries. Self-discharge is less than 0.5% per year. Performance is improved for low-drain applications such as memory backup. Pricing is \$9.99 at quantities up to 1000. Delivery is in three to five weeks.

Varta Batteries Inc.
300 Executive Blvd.
Elmsford, NY 10523
(914) 592-2500

► **CIRCLE 797**



100 Years Ago
We Lit-Up A
Single Market.
Today Philips
Innovations
Spark Markets
Worldwide.



Philips Components



PHILIPS

A Look Back At A Company Built On Looking Ahead.

From A Single, Small Factory... To A Global Presence In A Variety Of Established And Emerging Markets.



Philips innovations in sound have spanned decades — up to today's high-precision audio technology.

Pure, unwavering determination frequently works miracles. It did for Gerard Philips a century ago, when he bought a small factory, hired 10 workers, and proceeded to build what would become a global business enterprise.

With carbon filament lamps as the firm's first product, and Gerard's brother Anton Philips as its first sales manager, the start-up company grew quickly to

prominence in the lighting market of Europe.

Through the years, the company's continuous, wide-ranging research yielded knowledge and capabilities to broaden the product range. The original carbon-filament lamps gave way to incandescent lamps, and later, to gas-discharge lamps. X-ray tubes were followed by X-ray equipment; and the early radio valves, followed by complete radio receivers.

By the midpoint of the company's first century, Philips' technical expertise had grown to encompass phonographs, telecommunications equipment, and electric shavers.

Today, worldwide, Philips Components serves major end markets which include computers and electronic data processing, the multi-faceted automotive and industrial markets, the military/government sector, and highly specialized professional systems.

In automotive electronics, Philips Components products fulfill traditional applications such as car radios and sound systems, engine and transmission controllers, instrument displays, driver information centers, and other electronic systems. Other applications include anti-lock braking systems, airbags, and cellular telephones.

Philips Components Discrete Products Division has become a strong component supplier to the electronic data processing industry. Primary application areas for our components are telecommunication and networking products, monitors and terminals, peripheral board-level components, power supplies, and tape storage products.

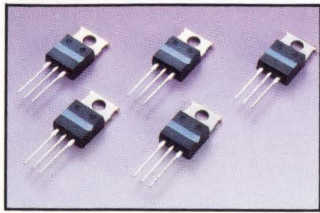
The hundred-year story of Philips is one of marketing growth, based on ever-increasing technical expertise — a direct result of the intense dedication to research which has characterized the company since year one. As the world's technological capability continues to expand, so too will the commercial opportunities for Philips, in existing markets and in new ones yet unknown.

Our century-long spirit of innovation continues. Use the attached reply card to learn more about our products.



On front: A.J. Philips and company staff members marked key developmental moments in broadcasting and other fields.

Philips Innovation: TOPFET®
It's The First Monolithic
Full Protected MOSFET.



TOPFET® provides over-temperature protection for T_j above 150°C...short-circuit load protection...rugged overvoltage clamping for inductive load repetitive switching...input ESD protection...and reverse battery protection.

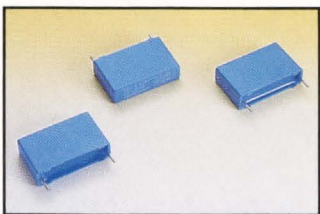
This integrated device embodies N-channel enhancement mode DMOS technology, and requires minimal external components for high-reliability protection.

Characteristics include good immunity to high dV/dt , and a low operating input current at an input level of 5 V. Maximum on-state resistance ranges from 28 mΩ to 100 mΩ and maximum continuous drain source voltage is 50 V.

The first TOPFET at 50 mΩ resistance is available now. The rest of the series will become available by 2nd quarter 1992.

® Registration pending. TOPFET is the Philips designation for Temperature & Overload Protected Field Effect Transistor.

NEW: 719J4 Series Capacitors For Interference Suppression Designed To Meet Worldwide Requirements.



Philips' new radial-box capacitor series carries these approvals: ULI1414, CSA, VDE 565-1, SEMKO, NEMKO, DEMKO, OVE, IMQ, FI, and SEV 1055.1978.

Devices are constructed of flame retardant materials and have a dual dielectric system which prevents active flammability under fault conditions.

Capacitance range 0.010 to .68 μF; tolerance is ±10%; voltage rating is 250 VAC @ 50/60 Hz @ 85°C.

The capacitors are available in bulk or on tape and reel, and designers' sample kits or bulk samples are also available.

Circulators And Isolators For RF, In Easy-Reference Full-Line Brochure.

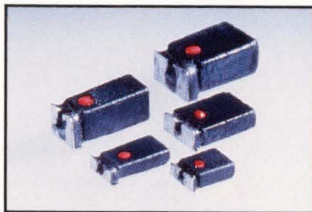


Philips' extensive product line provides over 160 high-quality coaxial and waveguide circulators and isolators. Applications include radio and TV transmitters, navigation aids and radio links, air traffic control systems, radar, mobile telephone systems, magnetic resonance tomography, industrial microwave heating systems, and wideband measurement.

Both product types range in frequencies from 68 MHz to 18 GHz, providing up to 50 dB isolation, with insertion loss as low as 0.2 dB, and CW power ratings from 1W to 6.5 KW.

The full-color brochure lists the complete selection of available circulators and isolators. Devices with alternate connectors and operating frequencies may also be available on request.

Maximum Capacitance In Minimum Size: Series 49XC Tantalum SMD® Chips.



Here's top performance in surface mount tantalum chip capacitors: the highest capacitance rating at a given rated voltage. And the advanced 49XC XTRA CHIP Series devices require as little as one-seventh the volume needed for typical molded tantalum chip capacitors.

49XC Series capacitance range is 1.0 μF through 220 μF, in the voltage range from 4 to 50 VDC. These capacitors operate from -55°C through +85°C with full rating; through +125°C with voltage derating.

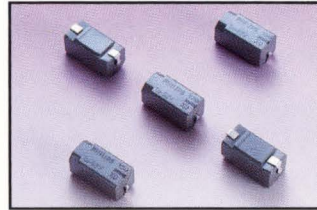
In five standard case sizes (D, E, F, G, and H), 49XC Series chips possess a unique, patented construction which yields devices exhibiting AC characteristics ideally suited for

high-frequency applications.

Packaging is 12 mm embossed tape, reeled, for efficiency in handling and storage. This packaging conforms to EIA Standard RS-481 and is compatible with all tape-fed high speed placement equipment.

Availability of 49XC Series tantalum chips: stock to eight weeks ARO.

Aluminum Electrolytic Chip Capacitors: Now Broader Range, In Smaller Sizes.



Philips 2222-139 Series Long Life SMD® Capacitors now offer longer working life as well as enhanced specifications.

Useful life of the devices is 200,000 hours @ 40°C. Load life rating is 2,000 hours, at 105°C.

The series provides capacitances from .22 μF to 220 μF, in the operating temperature range of -55°C to +105°C. Voltage ratings between 6.3 V and 63 V are standard; 100 V and 160 V are available on special order.

Cases sizes for the series are 10.8 x 4.1 x 4.4 mm, 13.8 x 4.1 x 4.4 mm, 14.3 x 6.2 x 6.9 mm, and 14.3 x 7.6 x 8.2 mm. The 4.4 mm mounting height is ideal for use on low-profile printed circuit boards.

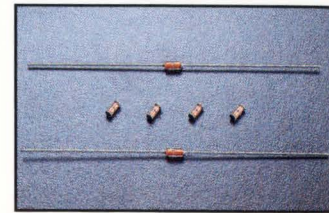
Fully flame-retardant, molded construction helps to insulate and protect against harsh environments, and make these capacitors suitable for flexible terminals, reflow and wave soldering.

Due to their self-healing, dielectric, electrolytic technology, the devices are insensitive to voltage spikes. Thus they do not require current-limiting resistors.

Application areas include automotive, telecommunications, electronic data processing, and control equipment. Smoothing, coupling, decoupling, buffering, and timing are among the frequently specified functions.

Availability: stock to 12 weeks ARO.

NEW: Fast-Acting, Highly Durable NTC Thermistors For Harsh Environments.



Excellent temperature-sensing performance comes in a choice of glass-encapsulated packages!

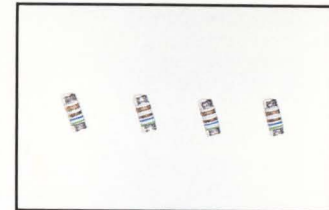
Series 2322 633 8.... thermistors are axial-leaded, in the SOD-27 package developed in Europe. Series 2322 633 5.... devices are electrically equivalent, in the SOD-80 surface mount MELF package.

Both series offer resistance ratings of 10, 20, or 30 KΩ, tolerances of ±5% or ±10%, β(25/85) of 3977, and β tolerance of 1.3%.

Series 2322 633 8.... performance is guaranteed from -40°C to +155°C. These devices are ideal for automotive and telecommunications applications.

Both series are available from stock.

Thin Film Technology, SMD® Combined In MELF Resistor.

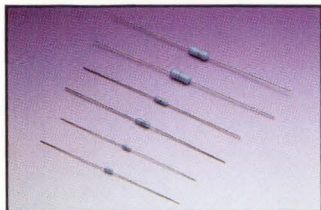


Philips 9B1406 MELF precision resistor benefits from technology used in manufacturing leaded metal film resistors—even though it comes in a surface mount package.

This thin film SMD® resistor is formed by depositing metal film on a high alumina core which is then capped and spiralled to value. The 9B1406's end caps are coated with nickel-copper-nickel and pure tin. The result: excellent soldering characteristics are maintained after long storage.

The MELF resistor offers TCs down to ±15 ppm/°C and tolerances to .1%. Availability is .22 ohm to 10 megohm in the 5% 50 PPM version. In bulk or tape and reel.

Ultra Precision Metal Film Resistors Available Now.



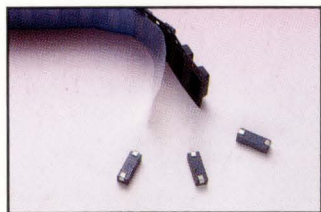
Philips is taking aim at test and instrumentation and measurement equipment with its UPR 5000Z series of ultra precision metal film resistors.

Initially developed to replace high precision wirewounds, the series is ideal for replacing bulky metal foil designs. Use them for A to D conversions and other circuitry requiring precise, stable resistors.

Available in three body sizes ranging from 1/20W to 1/3W, the resistors feature tolerances as low as $\pm .01\%$ and temperature coefficients starting as low as $\pm 2\text{ppm}/\text{C}$. Other series characteristics: excellent temperature and time stability, low voltage, low noise, and high initial accuracy and tracking.

Ask UPR 5000Z resistors in bulk or on tape and reel. Delivery from stock or within 8 weeks ARO.

NEW: Ferrite Beads For Surface Mount Production.



New beads are in .335" (8.9mm) and .160" (4.6mm) size categories, and are manufactured of 4S2 ferrite material.

Impedances match those of the most frequently used tape and reeled beads-on-wire.

Construction: a piece of flat tinned copper wire passed through and crimped on the rectangular ferrite bead.

Packaging: on tape with 8mm between centers, wrapped on 13-inch reels (2,800 pieces per reel) in accordance with EIA Standard 481A.

Applications: EMI/RFI suppression.

Samples now available.

New Metal Film Technology Yields Miniature-Size Power Resistors Up To 3 W.



Philips' new PR series is a miniature power resistor line of 1, 2, and 3 watt devices. The 1 watt unit is the same size as an RN55.

The new resistors have a 5% tolerance level and a temperature coefficient of 250 ppm. The devices combine high wattage capability with low hot spot parameters.

Size is .295 inches CL-CL. Packaging is RS296D Class 1 tape and reel for automatic insertion.

Availability: stock to 12 weeks ARO.

Newest Data Disk Set On Discrete Semiconductors Covers 3,600 Type Numbers.



Two-disk set includes quick-search feature and menu format, product descriptions, and comparative data on competitors' devices.

Disks run on all IBM PC/XT/AT computers and compatibles.

Specifying and ordering discrete semiconductors is easier than ever!

Sales Offices and Manufacturer Representatives

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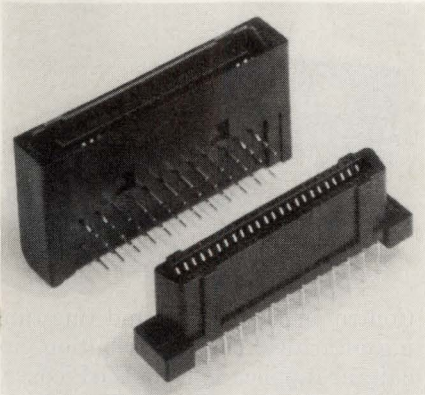
1-800-447-3762

Philips Components



PHILIPS

▼ **HALF-PITCH CONNECTOR LINKS BOARDS TOGETHER**

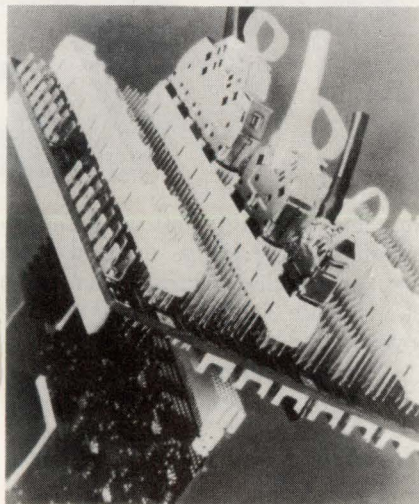


A half-pitch (0.050-in.) board-to-board ribbon connector lets designers choose a pin-and-socket or belows-type connector for their application. The FCN240 series connectors offer mating pins in two rows with 0.050-in. spacing between contacts and 0.100 in. between rows. The board side has a four-row, zig-zag configuration on a 0.050-by-0.075-in. grid. Current rating is 2 A dc and voltage rating is 240 V ac. Up to 96 pins are offered. Pricing for a 68-pin model is \$6.66 in lots of 1000.

Fujitsu Microelectronics Inc.
3545 North First St.
San Jose, CA 95134
(800) 642-7616
▶ **CIRCLE 798**

▼ **HIGH-DENSITY CONNECTOR OFFERS METRIC SIZES**

A 2.5-mm high-density connector system fits backplane and daughter-board applications in modern rack systems. The har-pak system's five-row design offers solderless pcb termination, 3D modularity, high con-

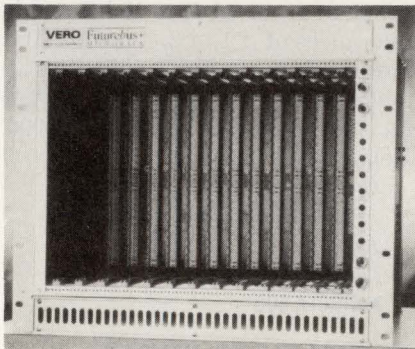


tact density, EMI protection, and the ability to surface-mount components on two sides of daughter cards without loss of a 15-mm card pitch. The quasi-coax contact configuration allows standard signal leads to be used for high data rates of up to 1.5 GHz.

Harting Elektronik Inc.
P.O. Box 95710
Hoffman Estates, IL 60195
(708) 519-7700
▶ **CIRCLE 799**

▼ **DEVELOPMENT SYSTEM AIDS FUTUREBUS+ USERS**

A Microrack development system is available based on Profile F of the Futurebus+ specification for high-performance computing applications. The Microrack includes a backplane supporting a 128-bit-wide data

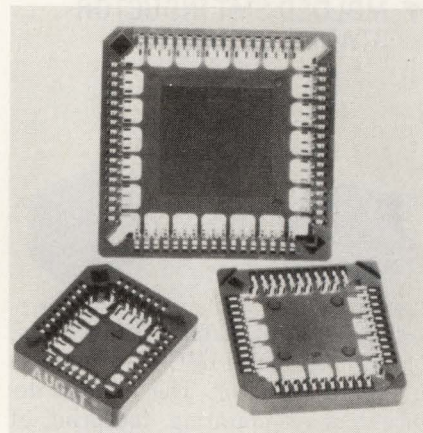


bus with central arbitration. RC termination networks minimize skew; and multiple decoupling capacitors, guard tracks, and power and ground planes hold down ground bounce and crosstalk. The complete system with power supply goes for about \$5000. Delivery is in four to six weeks.

BICC-VERO Electronics Inc.
1000 Sherman Ave.
Hamden, CT 06514
(203) 288-8001
▶ **CIRCLE 800**

▼ **SMT PLCC SOCKETS LAY LOW FOR NOTEBOOKS**

An ultra-low-profile socket for PLCCs stands just 4.45 mm off pc boards. The SMU Series surface-mounted sockets accept Jedec-dimensioned chip carriers on 1.27-mm centers from 20 through 84 positions. The low profile meets height packaging restrictions in high-density disk drives, laptops, and notebook computers. Typical pricing for a 68-position socket is \$2.34 in lots of 1000.



Augat Inc.
452 John Dietsch Blvd.
Attleboro Falls, MA 02763
(508) 699-9821
▶ **CIRCLE 801**

▼ **SMT ZIF CONNECTOR SUIT HIGH-DENSITY NEEDS**

A 0.5-mm pitch and 2-mm height above the board makes the Series FLZ connector well suited for high-density applications. The surface-mounted ZIF connector's contacts are zero-insertion-force type with from six to 30 contacts. Contact material is phosphor bronze, tin/lead plated with a rating of 0.5 A ac or dc. Pricing ranges from \$0.30 to \$0.40 in OEM quantities.

J.S.T. Corp.
1200 Business Center Drive
Suite 400
Mt. Prospect, IL 60056
(800) 292-4243
▶ **CIRCLE 802**

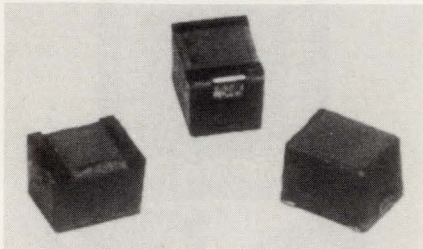
▼ **SEMCONN CONNECTOR LAUNCHES ACCESS.BUS**

An enhanced Semconn connector for the new ACCESS.bus link from DEC is available from Molex. ACCESS.bus is the first open serial bus that can link up to 14 I/O devices to workstations and PCs, allowing devices to be swapped without rebooting. The link combines DEC protocols, device drivers, and some DEC electrical standards with the Philips/Signetics I²C bus. The special Semconn series consists of the 71565 receptacle and 71564 plug. Pricing depends on style and quantity.

Molex Inc.
2222 Wellington Ct.
Lisle, IL 60532
(708) 969-4550
▶ **CIRCLE 803**

PASSIVES

▼ MOLDED SMT INDUCTOR STANDS 2.2-MM TALL



A height of only 0.087 in. (± 0.008 in.) is featured in the IMC-1210 surface-mounted inductor. The molded device has a mounting footprint of 0.125 in. long by 0.098 in. wide. Inductance values range from 0.01 to 100 μH in tolerances of $\pm 10\%$ and $\pm 20\%$. The devices are compatible with vapor-phase and infrared soldering. An inductor with a value of 10 μH and a $\pm 10\%$ tolerance costs \$0.35 in quantities of 2000. Delivery is from stock to 10 weeks.

Dale Electronics Inc.

P.O. Box 180

East Highway 50

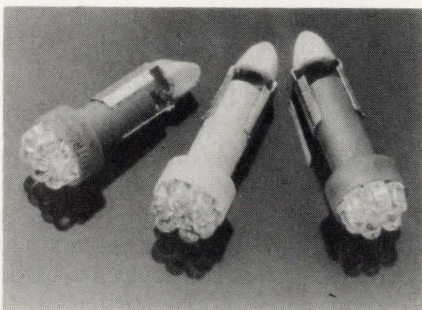
Yankton, SD 57078

(605) 665-9301

► CIRCLE 804

▼ SLIDE-BASED LEDs REPLACE FILAMENTS

The 5SB clustered LED lamp directly replaces the failure-prone T-2 #5 telephone slide-base lamp. The LED replacement has an operating life of 100,000 hours, which is about 15



times longer than the incandescent. Operating at voltages from 6 V to 120 V ac or dc, the slide-based LED clusters are characterized by high ambient light to LED light ratios. Prices are about \$11 in lots of 100. Small quantities are delivered from stock.

Ledtronics Inc.

4009 Pacific Coast Hwy.

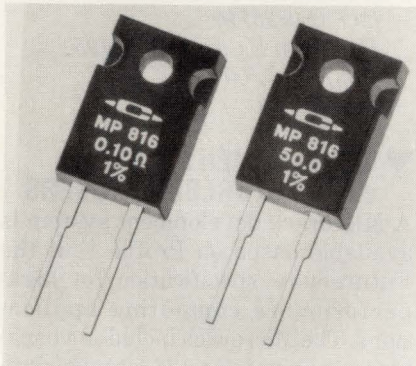
Torrance, CA 90505

(213) 549-9995

► CIRCLE 805

▼ HIGH-POWER RESISTOR DISSIPATES 16 W AT 25°C

Thanks to its all-molded TO-220 power package and proven Micronox resistance-film system, the Type MP816 Kool-Pak power film resistor is able to dissipate 16 W at a case temperature of 25°C. The non-induc-



tive device comes in a resistance range of from 0.1 Ω to 10 k Ω and in tolerances of ± 1 , ± 2 , ± 5 , or $\pm 10\%$. Single-screw mounting simplifies attachment to a heat sink. A 10- Ω , $\pm 5\%$ resistor costs \$1.04 in lots of 5000. Delivery is in six weeks.

Caddock Electronics Inc.

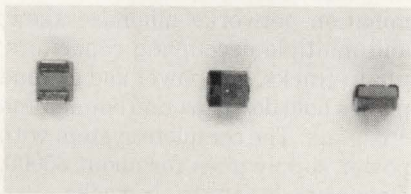
1717 Chicago Ave.

Riverside, CA 92507

(714) 788-1700

► CIRCLE 806

▼ TINY TANTALUM CAP SUITS SPECIALTY TASKS



The world's smallest molded tantalum capacitor for specialty, hybrid, and high-reliability applications is the TAZ R chip capacitor. The device measures 0.087 in. long by 0.055 in. wide by 0.047 in. high. Designed as a drop-in replacement for conformally coated capacitors, the TAZ R is initially available in ratings of 1.0 $\mu\text{F}/10$ V, 2.2 $\mu\text{F}/4$ V, and 0.47 $\mu\text{F}/20$ V. Pricing ranges from \$0.40 to \$0.67 depending on quantity and tolerance. Delivery is in eight to ten weeks.

AVX Corp.

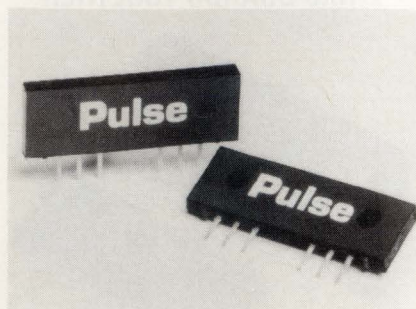
69 Landry St.

Biddeford, ME

(207) 282-5111

► CIRCLE 807

▼ PICOSECOND DELAY LINE CONTROLS CLOCK SKEW



Control of clock skew and fine tuning of critical clock-distribution circuits are applications for the Picosecond delay-line series. Delay values offered are 100 ps to 1000 ps in 100-ps increments. Excellent delay-to-rise-time ratios and delay tolerances permit greater control of system-timing performance. In lots of 1000, pricing is \$2.44. Small quantities are delivered from stock.

Pulse Engineering

7250 Convoy Ct.

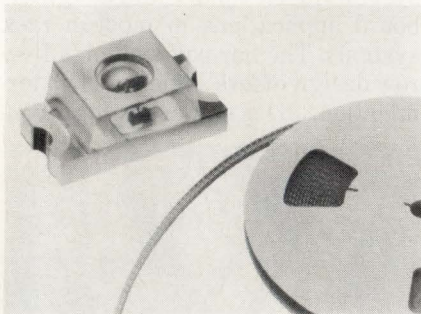
San Diego, CA 92111

(619) 268-2400

► CIRCLE 808

▼ CHIP-TYPE LEDs ARE SMT-READY

Leadless, chip-type LEDs have been developed for surface mounting in ultra-compact, optoelectronic applications. The chips are suited for high-density mounting using automatic insertion equipment or other automatic machinery such as robots. Either dip or reflow soldering can be



applied. Virtually any combination of single or dual chips, emitted color, lens shape, and polarity orientation is available. Call for pricing and delivery.

Stanley Co. Inc.

2661 Gates Ave.

Irvine, CA 92714

(800) LED-LCD1

► CIRCLE 809

POWER-ONE Offers 2 Million Voltage/Current Combinations Within 2 Weeks.



Modular High Power Up To 2000 Watts

You're in the initial stages of design. You need a prototype and you're facing a deadline. You also need a power supply with specific voltage/current outputs. And you need it fast!

That's where POWER-ONE's fully modular SPM High Power Series comes in. Single, dual, or triple output modules enable you to specify up to 15 DC outputs...from stock. With delivery time as little as two weeks.

And there's more. The incredibly versatile SPM represents the industry's highest power density—up to 2000 watts of multiple output power in the most compact package available today. There's even an optional on-board UPS capability. And no matter what configuration you require, be assured this internationally recognized power supply will meet the toughest safety regulations, worldwide.

So remember...whatever your requirements, we're keeping our shelves stocked for those urgent, limited-quantity deliveries. You'll get the exact voltage/current combination you need, on time. Every time.



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CIRCLE 222 FOR U.S. RESPONSE

CIRCLE 223 FOR RESPONSE OUTSIDE THE U.S.

SWITCHES & RELAYS

▼ LOAD MONITOR CHECKS RELAY STATUS

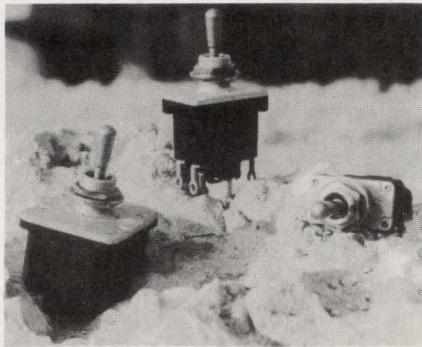
A system is available that monitors the status of dc-input electromechanical or solid-state relays which control ac loads. The ELM-101 electronic load monitor consists of a solid-state sensing module that's electrically matched to an external relay trip circuit breaker. The system monitors the load-controlling relay through comparison of its input and output status. Pricing is \$28.50 in lots of 100. Delivery is from stock.

Potter & Brumfield Inc.
200 S. Richland Creek Dr.
Princeton, IN 47671
(812) 386-2162

► CIRCLE 810

▼ SEALED TOGGLE SWITCH TAKES AMBIENT ABUSE

Designed to meet severe environmental applications, the NT Series sealed toggle switch has several construction features such as molded-in elastomer seals that enable it to withstand splashing and wash-



downs. In addition, the terminal inserts are molded into the thermoplastic case. Options include one-, two-, or four-pole circuitry and several terminations. List prices range from \$11.59 to \$26.44 depending on style and quantity.

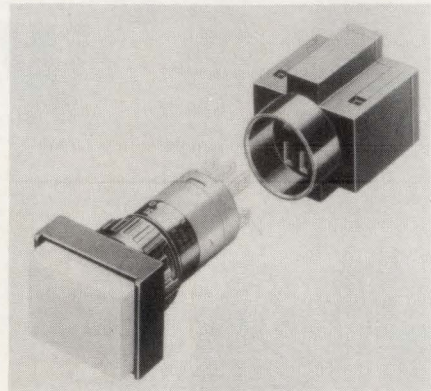
Micro Switch
11 W. Spring St.
Freeport, IL 61032
(815) 235-6600

► CIRCLE 811

▼ PLUG-IN ADAPTER JOINS SWITCH LINE

A plug-in adapter with screw connections for switches with quick-con-

nect terminals has been added to a line of switch products. The adapter, part #31-943.0, is designed for compatibility with EAO switches featuring a 5/8-in. and 7/8-in. mounting



hole and snap-action switching elements. Screw connections take two 1-mm round wires. List price is \$4.95. Delivery is in three to four weeks.

EAO Switch Corp.
198 Pepe's Farm Rd.
Milford, CT 06460
(203) 877-4577

► CIRCLE 812

YOUR FULL HOUSE TRANSFORMER COMPANY



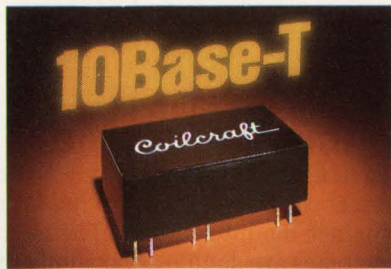
BASLER ELECTRIC HOLDS THE CARDS

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MAGNETIC PRODUCT GROUP

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Phone 618/654-2341 • FAX 618/654-2351

CIRCLE 116 FOR U.S. RESPONSE
CIRCLE 117 FOR RESPONSE OUTSIDE THE U.S.



Module integrates all 10Base-T magnetics

This module provides all the low-pass filters, transformers and common mode filters needed to implement a 10Base-T (IEEE 802.3i) interface.

The M2021-A is an encapsulated, package measuring 1.375" x .725" x .500" high. In addition to a pair of isolation transformers and low-pass filters, the module includes single-ended filters to provide balance and reduce common mode noise. (A module without common mode filtering is also available.) The unit's 2000 Vrms isolation meets IEEE 802.3 and IEC safety standards and the common mode filter chokes reduce emissions for FCC and VDE compatibility.

For more information, contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

CIRCLE 128 FOR U.S. RESPONSE
CIRCLE 131 FOR RESPONSE OUTSIDE THE U.S.



Low cost current sensors for 60 Hz applications

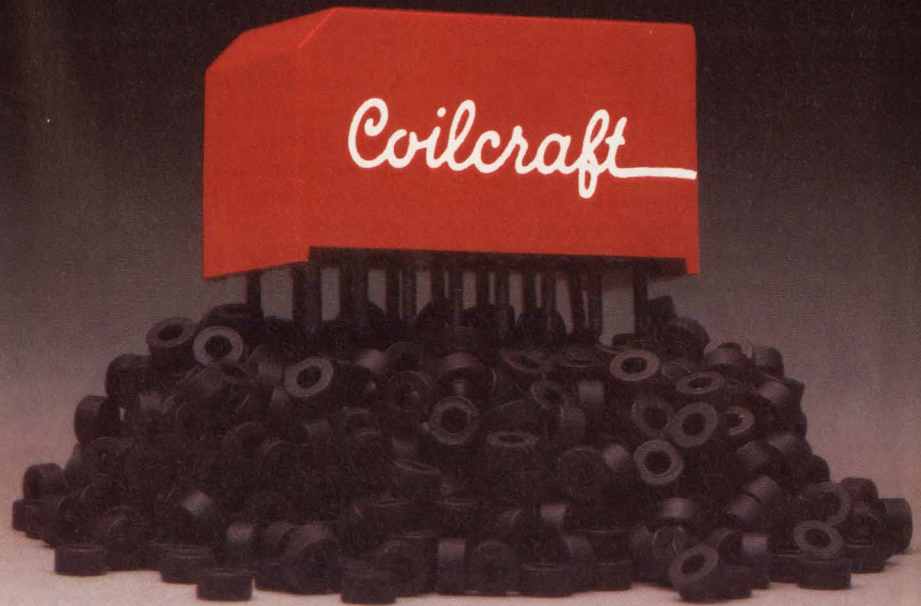
Coilcraft's low-cost current sensor is intended for 60 Hz applications. This compact part (roughly 3/4" square by 1/2" thick) is encapsulated in a protective epoxy coating with a 1/8" diameter through-hole. The sensor functions as the secondary of a current transformer while the conductor carrying the current to be measured serves as the "one turn primary."

Min. wall thickness of the hole is 0.5 mm which meets IEC 380, VDE 0730, and other requirements when used with an insulated conductor. Typical output voltages range from 12 mV at 1 Amp to 90 mV at 10 Amps.

For more information, contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

CIRCLE 129 FOR U.S. RESPONSE
CIRCLE 132 FOR RESPONSE OUTSIDE THE U.S.

Higher performance EMI filtering for high speed data lines

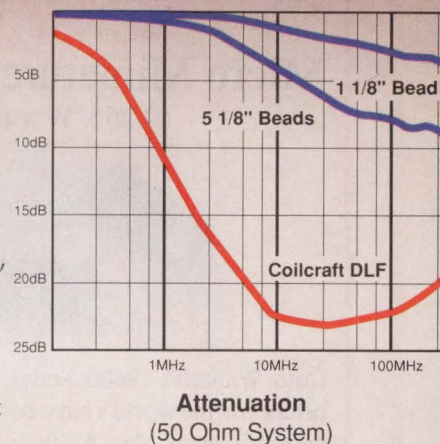


All these ferrite beads can't equal the EMI suppression of a single Coilcraft Data Line Filter.

Our new DLFs are the most effective, low-cost way to eliminate common mode EMI from digital signals, logic level power lines, and inter-equipment cables.

Available in 8, 4, 3 and 2-line versions, Coilcraft DLFs provide >15 dB attenuation from 30 to 300 MHz. Up to 40 dB simply by adding capacitors!

Because they use a single magnetic structure to filter multiple lines, you get differential *and* common mode noise suppression, something other filters can't do.



Coilcraft Data Line Filters are easier to install and usually take less board space than beads or baluns. And they're far less expensive than filtered connectors—around 2¢ per dB per line.

For details on our complete line of Data Line Filters, circle the reader service number. Or call 800/322-2645 (in IL 708/639-6400).

Designer's Kit D101 contains 2,3,4 and 8-line filters. \$65.



CIRCLE 130 FOR U.S. RESPONSE

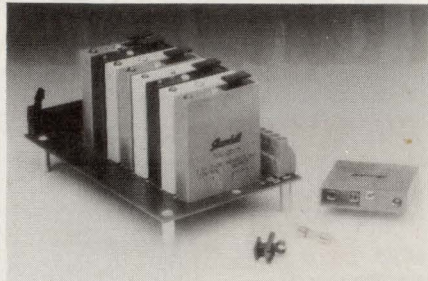
CIRCLE 133 FOR RESPONSE OUTSIDE THE U.S.

1102 Silver Lake Road, Cary IL 60013

SWITCHES & RELAYS

▼ FUSED I/O MODULES INCORPORATE PULLER

Fuse replacement is no longer a problem with the G5 I/O module. Rather than having to remove the module to check or replace its fuse,



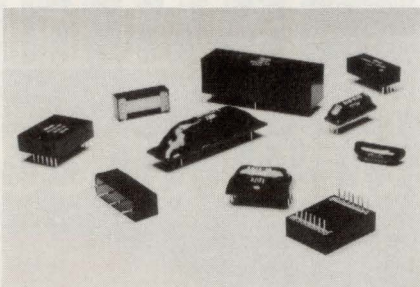
the module incorporates a fuse puller at its top to easily remove a 5-by-20-mm glass fuse from its clips. The G5 design is available in 5-, 15-, and 24-V ac and dc modules. Compatible rack and controller boards are also offered. An ac-output module goes for \$6.50 in lots of 250.

Grayhill Inc.

561 Hillgrove Ave.
LaGrange, IL 60525
(708) 354-1040

► CIRCLE 813

▼ REED-RELAY LINE EXPANDS ITS HORIZONS



An expanded line of Omnipin reed relays gives users great flexibility in their circuit design. Users can choose from many standard packages or match other electrical characteristics and footprints without major tooling costs. Coil voltages range from 3 to 24 V in Form A, B, or C relays with up to six switches per relay. Pricing is as low as \$1.47 in lots of 1000. Delivery is in from two to six weeks.

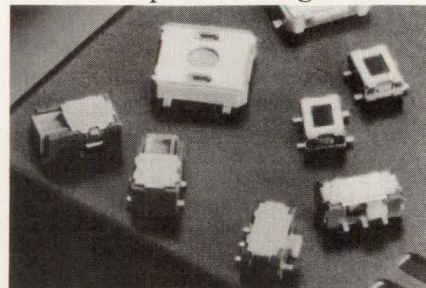
INRESCO Inc.

2411 Atlantic Ave.
Manasquan, NJ 08736
(908) 223-6330

► CIRCLE 814

▼ MINI SMT SWITCHES COME IN THREE STYLES

Tactile, push, and slide-style switches are available in a line of miniature surface-mounted units. The tactile switches are double-action units that feature a sharp detent click at one or two contact points. Ratings are 12 V



dc at 50 mA. Push switches are appropriate for low-current applications. All three types are compatible with reflow soldering and come in tape-and-reel packaging.

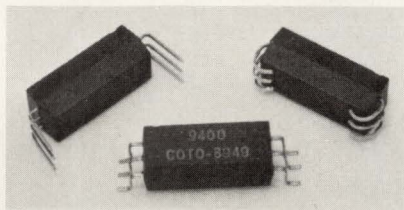
Noble U.S.A. Inc.

5450 Meadowbrook
Industrial Ct.
Rolling Meadows, IL 60008
(708) 364-6038

► CIRCLE 815

2 GHz

Micro Miniature Reed Relays (0.255"W x 0.550"L)



Coto Wabash's 9400 Series surface mount package offers you the world's most compact reed relay package currently available. A 50Ω coaxial shield makes this relay suitable for switching applications up to 2 GHz. The 9400 Series offers very low capacitance, excellent RF Characteristics, and is available with "J", Gull, Axial, or Radial Leads. The thermoset epoxy package withstands 430°F reflow soldering which makes this relay compatible with surface mounting manufacturing techniques. Call or write to us today for a free full line "Partners is Design" catalog.

COTO WABASH

A Kearney-National Company
55 Dupont Drive, Providence, R.I. 02907
Tel: (401) 943-2686 Fax: (401) 942-0920

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CIRCLE 276 FOR U.S. RESPONSE
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▼ POWER-PRODUCTS CATALOG PACKS 42 NEW MODELS

A full line of HP-IB dc power supplies and electronic loads, which includes 42 new models, is explained in a 28-page catalog. The power-supply line includes single- and multiple-



output units as well as a mainframe with easily interchangeable modules. Supplies range from 25 to 2000 W, to 225 A, and to 500 V. Electronic loads are specified at up to 600 W, 150 V, and 120 A.

Hewlett-Packard Co.
19310 Pruneridge Ave.
Cupertino, CA 95014
(800) 752-0900

► CIRCLE 816

▼ LOW-PROFILE CONNECTORS DETAILED IN CATALOG

The PAK-50 low-profile interconnection system is featured in a new catalog. The units permit board stacking as tight as 7 mm between boards. Other options for spacing include 8, 9, 10, and 12 mm. The 0.050-in.-pitch connectors are available in from 20 to 120 positions. The easy-to-use catalog includes specifications, technical drawings, and photos.

Robinson Nugent Inc.
800 E. Eighth St.
New Albany, IN 47150
(800) 338-8152

► CIRCLE 817

▼ ELECTRONIC ENCLOSURES FILL 316-PAGE CATALOG

Information on modular racks, sloped-front consoles, electronic desks, computer furniture, and instrument cabinets is contained in a 316-page modular-cabinet catalog. Technical sections include schematic

NEW LITERATURE



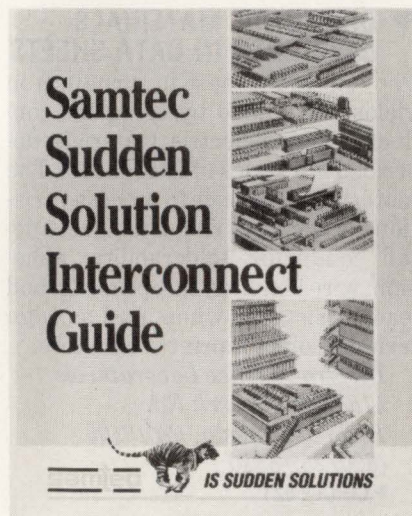
drawings and complete dimensions. A new section covers the company's EMI/RFI-shielded enclosures.

Equipto Electronics Corp.
351 Woodlawn Ave.
Aurora, IL 60506-9988
(708) 897-4691

► CIRCLE 818

▼ INTERCONNECTION GUIDE HAS APPLICATION ANSWERS

Sixty-four pages of ideas for interconnection applications fill Samtec's latest Interconnect Solutions Guide.

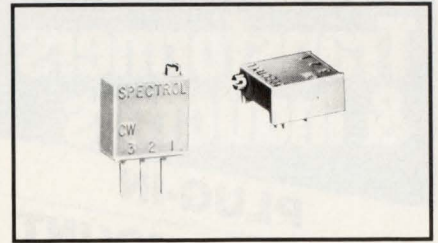


The book features surface-mount connectors, micro and low-profile types, board-stacking systems, square header and socket systems, specialty sockets, and more. Extensive drawings and complete specifications are included.

Samtec Inc.
P.O. Box 1147
New Albany, IN 47151
(800) SAMTEC9

► CIRCLE 819

Multi-Turn Cermet Trimmer Measures Only 3/8" Square



Spectrol's 3/8" square multi-turn cermet trimmer, the Model 64, offers five package/terminal styles to choose from. The unit is available in three side-adjust and two top-adjust versions, with pin configurations to suit any standard PCB application. This low cost space saver is available in resistance ranges from 10 ohms to 2 megohms with a $\pm 10\%$ resistance tolerance. It also features solder plated terminals, an integral multi-finger wiper contact, superior setability and stability, a TEMPCO of ± 100 PPM/ $^{\circ}$ C, a CRV of 3%, and is sealed for solvent and aqueous cleaning. Power rating 0.5 W at 85 $^{\circ}$ C.

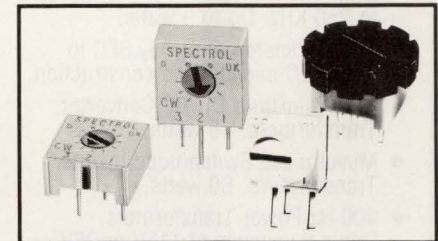
Spectrol®

Spectrol Electronics Corporation
4051 Greystone Drive, Ontario, CA 91761
Phone: (714) 923-3313 Fax: (714) 923-6765

CIRCLE 260 FOR U.S. RESPONSE
CIRCLE 262 FOR RESPONSE OUTSIDE THE U.S.

Spectrol's Model 63

Available in 12 Different Models



Spectrol's 3/8-inch square single-turn cermet trimmer, the Model 63 is offered in four terminal styles with pin configurations to suit any standard PCB application as well as two top-adjust and two side-adjust versions, and two different knob types. Quick adjustment is achieved with a multi-fingered wiper. Resistance range is from 10 ohms to 2 megohms with a $\pm 10\%$ resistance tolerance. Features include improved solder-plated terminals, and an "O" ring seal for solvent and aqueous washing. Tempco is 100 ppm/ $^{\circ}$ C, and a CRV of 2% or 2 ohm. The Model 63 continues to provide excellent performance as the industry standard across a broad spectrum of applications.

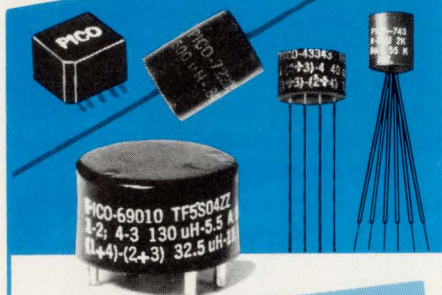
Spectrol®

Spectrol Electronics Corporation
4051 Greystone Drive, Ontario, CA 91761
Phone: (714) 923-3313 Fax: (714) 923-6765

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CIRCLE 263 FOR RESPONSE OUTSIDE THE U.S.

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TRANSFORMERS

QPL standards available
MIL-T-27/103-1 thru 16, MIL-T-27/172-1 thru 50,
MIL-T-27/357-1 thru 114, MIL-T-27/358-1 thru 123,
MIL-T-27/359-1 thru 147

- Audio Transformers ranging in size from $\frac{1}{4}'' \times \frac{1}{4}''$ to $\frac{3}{4}'' \times \frac{1}{16}''$, 20 Hz to 250 KHz. Up to 3 watts.
- Pulse Transformers .05 μ SEC to 100 μ SEC miniaturized construction.
- Ultra-miniature DC-DC Converter Transformers. 40 watts.
- Miniaturized Switchmode Inverter Transformers. 60 watts.
- 400 Hz Power Transformers. Primary voltages of 115V or 26V. Plug-in construction. Ultra-miniature
- Microphone/Transducer Audio Input.
- MIL-STD-1553 Interface Multiplex Data BUS Pulse Transformers.

POWER INDUCTORS

QPL standards available MIL-T-27/356-1 thru 63

- Inductance values to 20mH with DC currents to 23 amps

COMMON MODE INDUCTORS

HIGH "Q" INDUCTORS

**PICO
Electronics, Inc.**

453 N. MacQuesten Pkwy. Mt. Vernon, N.Y. 10552

Call Toll Free **800-431-1064**

IN NEW YORK CALL **914-699-5514**

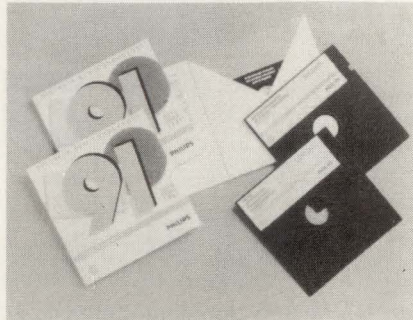
FAX **914-699-5565**

See EEM
or send direct for
FREE PICO Catalog

NEW LITERATURE

▼ FLOPPY DISKS DOLE DISCRETE-SEMI DATA

A set of floppy disks for IBM PCs and compatibles contains key data on a comprehensive range of discrete semiconductors. The disks are offered in sets of two, each equipped



with a quick-search feature that enables users to locate specific type numbers, obtain competitors' data, and order products. Full data is included for more than 3600 type numbers.

*Philips Components
Technical Literature Dept.
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404
(800) 447-3762*

► CIRCLE 820

▼ DIELECTRIC MATERIALS DESCRIBED IN DATA SHEETS

Proven increases in production yields are gained by using the conductor and dielectric materials described in a series of data sheets. The materials' tolerance to process variations is the key. The data sheets detail conductor solderability, adhesion, wire bonding, thin printing, and leach resistance when used as edge terminations for printed resistors.

*Electro-Science Laboratories
416 East Church Rd.
King of Prussia, PA 19406
(800) 257-8340*

► CIRCLE 821

▼ RARE-EARTH MAGNETS BOAST HIGH PRECISION

A 16-page, full-color brochure describes a full line of high-performance rare-earth magnets for diverse applications. Advances in raw-material development as well as processing are described, as are the company's capabilities in developing magnets for new applications. A technical section details the magnets' properties.

*Shin-Etsu Polymer America Inc.
34135 7th St.
Union City, CA 94587
(415) 475-9000*

► CIRCLE 822

▼ EQUIPMENT HANDLES COME IN WIDE ASSORTMENT

Handles for electronic equipment, furniture, and other applications are the subject of an 84-page catalog. An extensive selection of round, half-round, oval, rectangular, offset, slanted, folding, contemporary, and



bar handles is described. Made of aluminum, brass, and stainless steel, the handles are offered in dozens of finishes.

*Vemaline Products
333 Strawberry Field Rd.
Warwick, RI 02887-6979
(800) 227-0254*

► CIRCLE 823

▼ HYBRID AND IC BOOK INCLUDES CONVERTERS

A product-line excursion into dc-dc converters and monolithic amplifiers is reflected by the fifth printing of Apex's 264-page hybrid and IC handbook. The handbook features the new DB2800 series of dc-dc converters as well as the recently introduced PA41, the world's first 350-V monolithic op amp. Complete data sheets detail a wide selection of high-voltage, high-current, and high-speed power amplifiers.

*Apex Microtechnology Corp.
5980 N. Shannon Rd.
Tucson, AZ 85741
(800) 448-1025*

► CIRCLE 824

CIRCLE 216 FOR U.S. RESPONSE

CIRCLE 217 FOR RESPONSE OUTSIDE THE U.S.

Oh no. Please, not now. Not with manufacturing release next week.

THE PROTOTYPE DOESN'T WORK.

Six ASICs, fifteen PLDs and the whole thing's gone south. Maybe I should go south too. Yeah, hop a bus. Head for Mexico.

THE PROTOTYPE DOESN'T WORK.

Software? Could be. Hardware? Might be. So where do I start? At the beginning, of course. And just where is that, smart guy?

THE PROTOTYPE DOESN'T WORK.

And my performance review comes up next month. Maybe they'll just forget about all this, right? Yeah. Sure.

THE PROTOTYPE DOESN'T WORK.

Wait. What about that glitch in the handshake on the first pass? Couldn't reproduce it. Maybe it just reproduced itself.

THE PROTOTYPE DOESN'T WORK.



These are just a few of the reasons Tek makes a complete line of scopes, logic analyzers and signal sources. Instrumentation that can quickly get to the core of your prototype's problems. Whether they're digital, analog or software. Because even when your prototype doesn't work, Tek does. **TALK TO TEK/1-800-426-2200**

Tektronix

Test and Measurement

CIRCLE 274 FOR U.S. RESPONSE
CIRCLE 275 FOR RESPONSE OUTSIDE THE U.S.

rugged plug-in amplifiers



0.5 to 2000 MHz from \$13⁹⁵ (10 to 24 qty)

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MODEL	FREQ. RANGE (MHz)	GAIN dB		MAX PWR [†] dBm	NF dB (typ)	ISOL. dB (typ)	DC PWR V/ma	PRICE \$ ea.
	f_L to f_U	min	flat ^{††}				(10-24)	
MAN-1	0.5-500	28	1.0	+8	4.5	40	12/60	13.95
MAN-2	0.5-1000	18	1.5	+7	6.0	34	12/85	15.95
MAN-1LN	0.5-500	28	1.0	+8	2.8	39	12/60	15.95
◇MAN-1HLN	10-500	10	0.8	+15	3.7	14	12/70	15.95
MAN-1AD	5-500	16	.05	+6	7.2	41	12/85	24.95
MAN-2AD	2-1000	9	0.4	-2	6.5	28	15/22	22.50
MAN-11AD	2-2000	8	0.5	-3.5	6.5	22	15/22	29.95

^{††}Midband $10f_L$ to $f_{U/2}$, $\pm 0.5\text{dB}$ [†]1dB Gain Compression ◇Case Height 0.3 in.
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CIRCLE 202 FOR U.S. RESPONSE

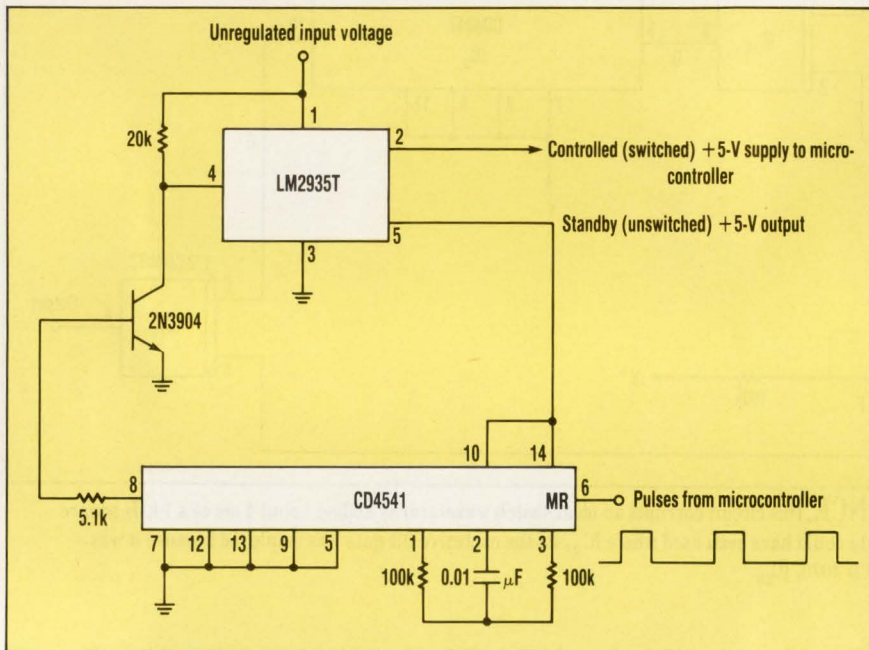
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JULES SCHLESINGER

Greenwald Industries, 1340 Metropolitan Avenue,
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BY CYCLING THE POWER to the microcontroller off and on, this supervisory circuit can bring a latched-up microcontroller to a normal operating state.

Most supervisory circuits for microcontrollers work by activating the controller's reset line when the output pulses generated by properly running software unexpectedly cease. Those supervisory

circuits typically contain a retriggerable one-shot, which stays triggered so long as the microcontroller keeps generating pulses. If the pulses stop, the one-shot times out, and the supervisory circuit puts out its reset signal.

Although such supervisory circuitry is effective most of the time, there are occasions when the μ C fails to respond to its reset input. In such cases of (nondestructive) latch-up, the only way to get the controller going again is to cycle its power off and then back on. That is exactly what this improved supervisory circuit does (see the figure).

The circuit makes use of a low drop-out voltage regulator, the LM2935T. That device has a shut-off pin and a +5-V standby output, which is not controlled by the shut-off pin. The circuit's other key components are a CD4541 oscillator/counter wired as a divide-by-8192 counter, and a transistor, which drives the LM2935T's shut-off line.

In normal operation, pulses from the microcontroller continually reset the counter before the critical count of 4096 is reached. If the pulses disappear for any reason, be it a software glitch or anything else that makes the controller latch up, the counter will count past 4095. At 4096 its output (pin 8) goes high and turns off the power to the μ C.

The power is kept off for about 9.4 seconds (4096 times the period of the oscillator, which is 2.3 milliseconds) and then turns back on. If the μ C output pulses do not then begin, it will cycle on and off at 9.4-second intervals until the fault is cleared.

The circuit is simple, very inexpensive, and completely adjustable to different timing requirements. □

CIRCLE
523 SPARE LAMP TURNS ON
AUTOMATICALLY

M.S. NAGARAJ

Digital Systems Div., Insat-II Building, I.S.R.O. Satellite Centre,
 Airport Road, Vimanapura P.O., Bangalore - 560 017, India.

When even a brief outage by an incandescent lamp is unacceptable—in a traffic light or an operating theater, for example—this simple circuit may be just what the doctor ordered. It monitors the current

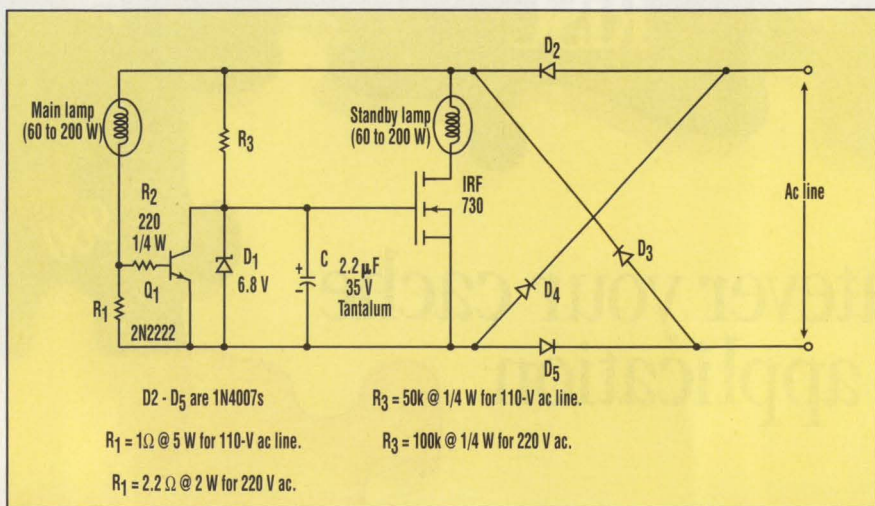
through the lamp, and should that current fall to zero, immediately activates a standby device—a separate lamp or a second filament in the same bulb as the first. Note that an alarm may be connected across the standby device to call attention to

the fact that a failure has occurred and that the main lamp needs to be replaced.

The circuit works by monitoring the lamp current with a small current-sampling resistor, R_1 (see the figure). The drop across that resistor is between 0.5 and 1.7 V rms for bulbs between 60 and 200 W. That's sufficient to keep transistor Q_1 turned on, which in turn keeps the capacitor, C, discharged and the MOSFET and standby lamp turned off.

When the main lamp blows, Q_1 is switched off, allowing R_3 , Zener di-

IDEAS FOR DESIGN



THE STANDBY LAMP turns on automatically when the main lamp burns out, thanks to the action of this watchdog circuit. The component values can easily be changed to handle lamps outside the 60-200-W range.

ode D_1 , and C to develop a voltage V_z across the gate and source terminals of the MOSFET. That turns on the MOSFET, which, in turn, directs

power to the standby lamp.

Care was taken in the design to ensure that the main lamp's turn-on surge current does not cause Q_1 's

bias current to exceed its maximum allowable rating. The design also ensures that the Q_1 base current is high enough to keep the MOSFET solidly turned off even under brownout conditions, when the supply voltage drops as low as 80% of nominal.

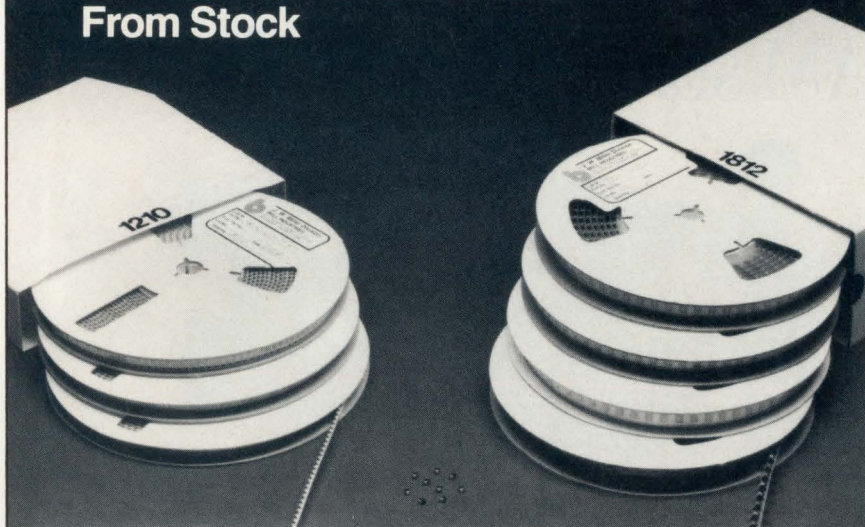
Although the circuit was designed and tested for lamps in the range of 60 to 200 W, the component values may be altered to accommodate lamps (and other loads) of just about any power rating. \square

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IFD Winner for
June 27, 1991

Carl Spearow, Sundstrand Corp.,
4747 Harrison Ave., Rockford, IL
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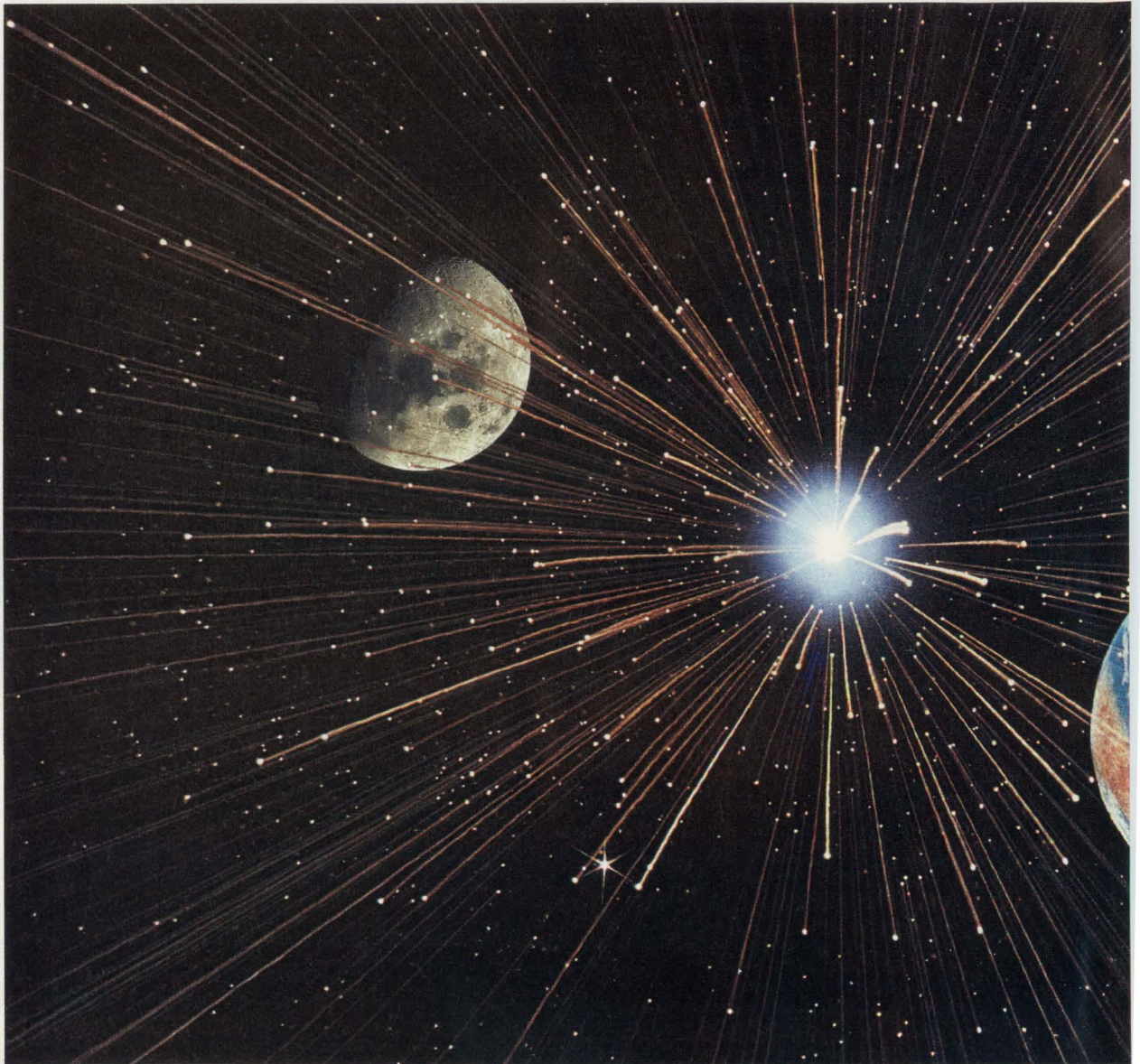
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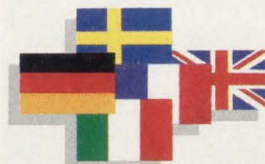
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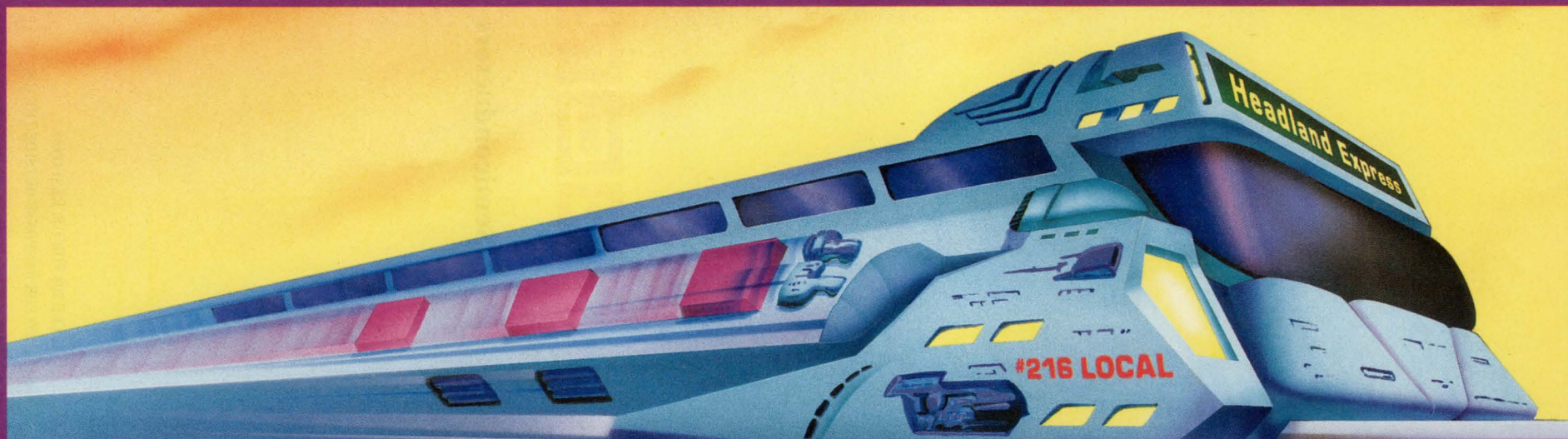
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QUICKLOOK

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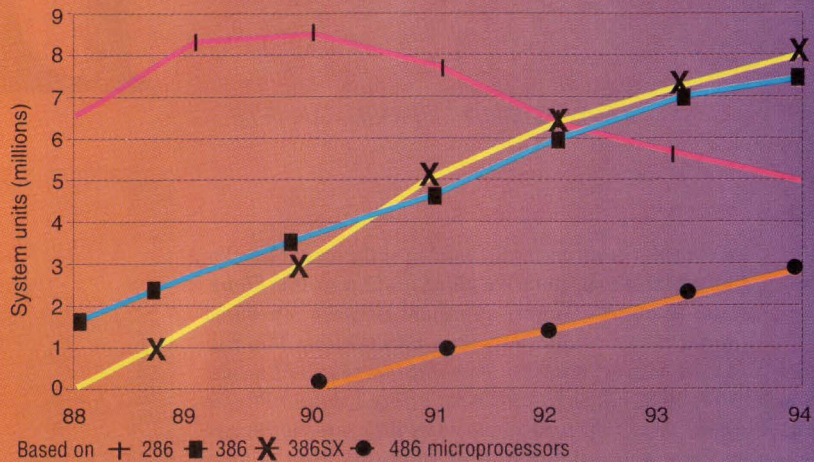
Electronic enclosures can be specified on an IBM compatible PC with a free disk from Equipto Electronics Corp. Selections include modular cabinets in vertical and slope front consoles and enclosures engineered to meet EMI/RFI, FCC, military, and Tempest requirements. Contact Equipto Electronics Corp., 351 Woodlawn Ave., Aurora, IL 60506-9988; (708) 897-4691; fax (708) 897-5314. CIRCLE 453

Share all your executables; pay for your shareware; don't hit the computer; back up files after you have found them." These tongue-in-cheek directives come from "All I Really Need to Know I Learned from my Computer" in the *Effector* newsletter published by the Electronic Frontier Foundation.

On a more serious note, the foundation aims to ensure the rights and responsibilities of computer users. Most visible is its defense of hackers charged with electronic trespassing. The foundation examines issues of privacy and civil liberties arising from advances in computer-based communications.

Student memberships are \$20; regular membership is \$40. Contact the foundation at 155 Second St., Cambridge, MA 02141; (617) 864-1550; fax (617) 864-0886. CIRCLE 454

POWERFUL PCs PICK UP STEAM



KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ

President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085



Using the recording and charting technique described in the Nov. 7 Kmet's Korner, problems are grouped into similar categories. The methods used to correct design-related errors have been discussed. In this column, I'll pay attention to problems discovered when a product is tested. The probability that testing will expose a number of problems with the product during the execution phase is near unity. Allowances for this effect should have been made within the plan by adding test activities into the structure of the network and by establishing task durations that anticipate test problems. In cases where this foresight is not a part of the plan, the project manager can expect to do a fair amount of real-time management when the problems are revealed.

Once noted by a team member, the problem is recorded and as assignment made to an individual, or team, to develop a solution. Where the solution is quick and easy, little needs to be done except to acknowledge that the work has been performed and to make certain that no major milestone has been affected. When solutions are not readily obtained, affected individuals get involved to establish a plan of attack. This plan can then be added to the product execution network and tracked through to completion.

It is then reasonable to expect the project/program network to undergo modification each time a major problem is uncovered. In exercising this discipline, problems are prevented from "falling through the cracks" and a log is automatically maintained to produce data that can be used in future projects to estimate the amount of time to allocate for resolving problems on a per-unit basis.

In projects/programs where problem resolution is factored into the base plan, the project manager should follow up on each test problem as it is reported to make certain it is within the range structured into the plan. As input is received that goes beyond the anticipated range, the task of solving the problem is assigned to the appropriate individual and added to the structure of the project/program network. With this action, the problem is automatically recorded and its solution is now an integral part of the tracking system. A special code can be assigned to problems that have been uncovered by testing to assist the team in isolating particular problem areas.

QUICKLOOK

TIPS ON INVESTING

People whose job is to spot trends in the way the rest of us live, work, play, and invest our time and money see a pattern emerging as the 20th century comes to a close. More engineers are voting with their dollars: products, issues, and even candidates for public office are being supported or rejected based on how they measure up to social concerns.

If you can control the types of products you bring into your home or the support you give to issues that concern you, why can't your investments reflect some of your social values? The fact is, they can.

The economic and market forces that are beginning to shape the 90s are presenting unique challenges and opportunities to engineering investors. You can take advantage of these opportunities and support your own social agenda by seeking out some companies whose policies most closely reflect your priorities.

This is known as socially responsible investing; two types are avoidance investing—excluding investments that are in conflict with your social values—and supportive investing—seeking out investments in companies whose corporate policies closely parallel your social concerns. You can use either of these approaches or a combination of both, but to be successful, these methods require the thoughtful articulation of both investment objectives and social criteria before an investment program is implemented. If you would like your investments to reflect your social consciousness, you have essentially three options for achieving this goal:

- **Managing your own investment portfolio.** This approach offers the advantage of being able to customize your investment criteria according to your values. The disadvantage is the time commitment required in taking on this task. Managing a portfolio of investments is a time-consuming process by itself. Adding to it the time required to screen potential investments for their compatibility with your social concerns expands the workload and makes this approach impractical for many engineering investors.

- **Mutual funds.** A number of mutual funds invest according to a defined set of criteria and provide for professional management of your assets. Most mutual funds accept investments as small as \$1,000. If you are investing within a retirement plan, the investment sometimes can be even less. By reading the mutual fund's prospectus, you can decide if the fund's socially responsible criteria are a reasonably good match with your own objectives.

- **Individual portfolio management.** Individual portfolio management by a professional investment manager allows you to customize your portfolio by communicating your objectives in detail to the professional you select to manage your assets. Another benefit is that your assets are managed by full-time investment professionals.

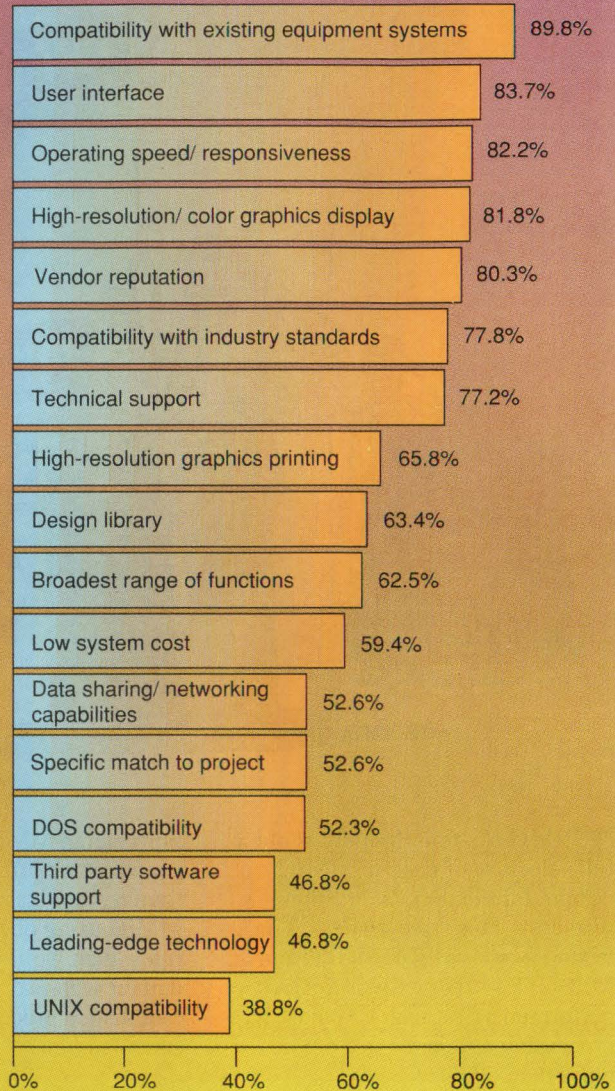
However you decide to let your investment goals work with your social concerns, it is important to research your options carefully and choose the method that is right for you. The key is to get the best advice possible: don't be afraid to comparison shop and weigh all the pros and cons.

If you choose to delegate the socially responsible investment function to a mutual funds manager or individual portfolio manager, explore the manager's experience in this particular area, and research the manager's performance history in socially responsible investing before making an investment decision. Call or write to me for a free brochure and more information at the address below:

Henry Wiesel is a financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221 or (908) 389-8653. Wiesel is also a qualified pension coordinator with the Private Client Group. He invites questions.

CAD/CAE SURVEY

WHEN YOU PICK A SUPPLIER FOR A CAE OR CAD SYSTEM, WHAT IS MOST IMPORTANT?



Source: a survey of Electronic Design readers by The Adams Co., Palo Alto, Calif. (415) 325-9822

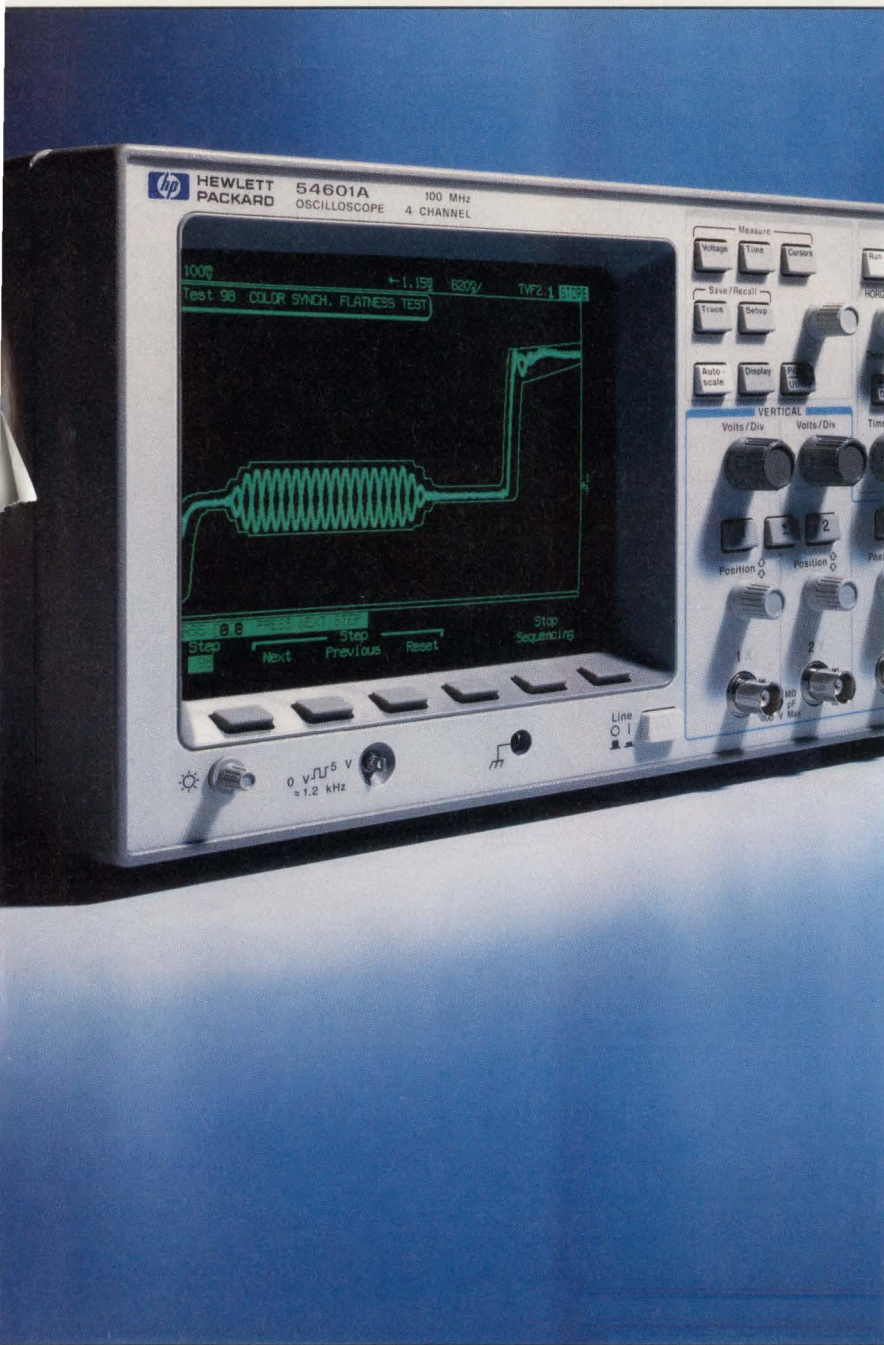
Readers gave multiple answers to question

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... that up to 90% of the 234,000 defense engineers in the U. S. could lose their jobs in the wake of the biggest defense demobilization since the end of World War II. And the number of engineers in the workforce now should meet present demand, given economic growth in the U. S. that averages, but doesn't exceed, 3.2% a year during the nineties. Market forces work reasonably well to correct imbalances in engineering supply and demand.

Robert Rivers, econometrics forecaster appearing at the IEEE U. S. Activities Careers Conference

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CIRCLE 293

PEASE PORRIDGE

whole 'nother story.

Anyhow, people drove in from 50 miles south and 100 miles west and 90 miles north, and some people merely had to walk across the street. Others sent in their best regards by fax, from 5000 miles away. We had about 40 people there. There were people who had never attended one of our reunions before, and our Cruise Director, Al Riskey of Datel, agreed that we were finally getting more efficient at inviting people. We invited some by phone, and others by mail, and our redundant techniques caused some people to get 3 or 4 invitations.

I ran into one young woman who just happened to be promoting a system for laser identification and labeling of wafers and masks — which I just happened to have a serious active need for. I mean, every once in a while, we have a project coming along great, and the wafers come out not working because somebody put on the wrong mask. It's been my pet peeve for a few years, that if every can of beans at the Safeway gets a bar code, and every other letter delivered to your door, then why can't a mask get a bar-code, too, to ensure that a computer can lock out an improper mask? So Pat Green had a real piece of good news for me, and I hope we do a million dollars of business with her company*. If we do, then *we'll* save \$2 million. Of course, it will take some additional hardware and software, so that when a special engineering run needs a screwy sequence of masks, we can override the computer.

Fortunately, with these bar codes, we won't run out of legal codes very quickly. Have you ever noticed the bar codes on the front of a letter? Have you counted the *number* of bars on that? I bet you didn't notice that they cleverly inserted as many as 52 bars. The coding, of course, isn't true binary. It's a 7,4,2,1 decimal code, with a parity bit and parity word. But if it were in binary — well, 2^{52} is a VERY large number — about 5×10^{30} . With such a big number, you could have a separate mail code for your front door and another one for your back door, because there are only about 6×10^{30} square feet on the surface of the whole earth. So I don't think we will run out of codes very soon, even if we put a code on each wafer. Now, a code

on each die, I'm not so sure about...

So, as with the other reunions, I ran into some nice people who had ideas that were really stimulating. Not just the enforced jollity of a group of random people forced into proximity, but the matching up of random pairs or triplets of bright people with interesting ideas. Just as, at the MIT reunion, I ran into a guy who wanted to buy a dozen copies of my new book** to pass around to his engineers and technicians. Just as I ran into artistic and talented people at other reunions. Just as I ran into a person at another reunion who was having problems with her word processor as it interfaced to her printer, and I figured out how to trick it into giving her the correct margins.

So, in addition to the good news of the bar-code business, I found this reunion business a good success. For instance, there may be a person that you associated with, years ago, and that person may have been (so you thought) a boring or useless or unpleasant person. But (after a number of years) that person suddenly becomes interesting, skilled in a field that just happens to be fascinating to us, as we listen and learn.

I mean, once upon a time, we were all kids. But as we grow up, we become better rounded individuals; and other people do, too. So, if you're deciding whether to attend a reunion, I would recommend that you really should. You may run into some fascinating ideas, some pleasant memories, even some good business — but you won't be bored, not for very long.

And the best part is, if you want to call a reunion, you can figure out how to do it yourself. I have attended Amelco Semiconductor Alumni Reunions, and reunions of National Semiconductor's ALIC group, and I have also heard about some good Fairchild reunions. All it takes is a park where you can gather and picnic, or a local bar where anybody who will buy even a ginger ale is always welcome. No matter where you worked, you can run your own reunions. I won't say that the art of getting everybody found and invited and actually in attendance is trivial, but you can figure it out.

Here's one technique I've used to find a person who seems to have dropped off the earth, and I used it to locate the for-

mer owner of my house. An insurance company kept sending her statements about the value of her policy, but I had no idea where to forward these letters. But I did have her social security number. So I sent a polite note to the IRS, asking them to forward the note to the person with this social security number, as there was this valuable information that I wanted to forward. Shortly she wrote to me from Baltimore, thanking me for getting this material sent to her.

So if you know somebody's social security number, I'm sure you will admit there are some people who can always find their man! And they're willing to help you forward a little note; whether the person wants to write back is another matter.

Ah, that reminds me — even at the Philbrick reunion, there were people we could not invite because we had no address for them. Where is Louis Watson? Where is Bob Boyd, Dave LeVine, Brian O'Brien? Suzanne McGovern, Adele Fata, Ann Havey, Sue Taipale, Jeanne Finnert? Brad Vachon, Everett A. Day, Ralph Daigle, Dan McKenna, Dick Hewson, Bob Squarebriggs, Maurice Goldwater, James Royer, Dick Davis — where are these guys? Unfortunately, we don't know the social security numbers for these people. So I'd appreciate it if my readers will just remind these guys, all of these missing persons, and anybody else that ever worked for Teledyne Philbrick or George Philbrick Researches, that we really do want their addresses, so we can invite them to the next reunion. If we can get most of them to show up, we can make a really *great* reunion.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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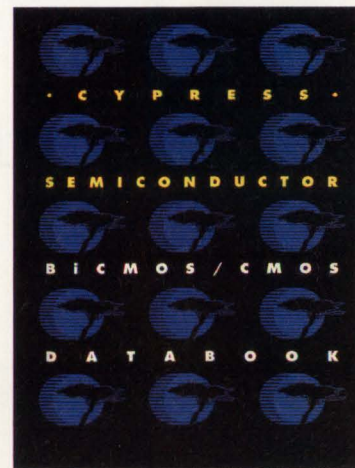
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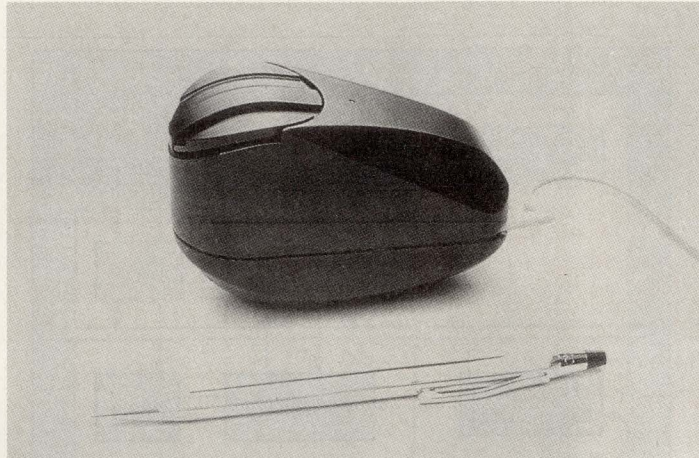


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CIRCLE 164 FOR U.S. RESPONSE
CIRCLE 165 FOR RESPONSE OUTSIDE THE U.S.



1. TWO MICROGYROSCOPES inside the GyroPoint sense an operator's hand movements to control the orientation of images on a computer screen. The pointer can operate as a conventional mouse with unrestricted desktop area, or as a free-space pointer to control 3D images. Five buttons let the user activate the device, select on-screen objects or menu options, and control lateral or rotational image movement.

SCREEN DISPLAYS FOLLOW
HAND MOVEMENTS SENSED BY TINY
INTERNAL GYROSCOPES.

COMPUTER POINTER CONTROLS 3D IMAGES IN FREE SPACE

MILT LEONARD

Devices that control objects displayed on a computer screen range from a simple mouse to full 3D-input peripherals. No single device, however, provides a full range of capability. Although relatively inexpensive and immune to electrical noise, a computer peripheral like a mouse or trackball has just fair resolution, no 3D capability or absolute positioning, and a restricted operating space. On the other hand, digitizing tablets have better resolution and are also immune to electromagnetic interference, but they have even worse mobility than a mouse or a trackball, have no absolute positioning, and provide no 3D capability. In applications requiring 3D capability, limits on absolute-position capability, mobility, and resolution prevail, in systems priced upwards of \$3000 and based on magnetic, ultrasonic, or strain-gage technology.

Using a revolutionary gyroscope design, Gyration, Inc. has developed a computer pointer that operates in free space to manipulate 3D screen im-

3D COMPUTER POINTER

ages. Unlike systems that calculate a pointer's position within a confined free-space volume using triangulation techniques and ultrasonic or magnetic sensors, Gyration's GyroPoint operates in a space limited only by the length of the cable connecting it to the host computer. And where positioning error in other 3D pointers increases as the pointer approaches the limits of the defined free-space volume, the GyroPoint's accuracy doesn't vary with distance.

The GyroPoint controls the orientation of a computer-generated image in three directions and in real time. The device can be used like a mouse on a desktop, but without the need for a mouse pad. It can also be held in mid-air. Weighing just 5 oz., the device comes in a plastic housing 3.65-in. long, 1.68-in. wide, and 2.30-in. high (Fig. 1).

TWO TINY GYROS

The heart of the pointer consists of two miniature gyroscopes—called GyroEngines—mounted inside, one vertically and the other horizontally. The combined gyroscopes sense the operator's rotational hand motion about the horizontal (pitch and roll) and vertical (yaw) axes. Electrical signals describing these three degrees of freedom are sent out to the host computer simultaneously.

The pointer's housing is shaped symmetrically to accommodate both left- and right-handed users. For the same reason, the GyroPoint's two-piece cable can exit from the left or right side of the housing. The segment of cable exiting the pointer connects to an adapter cable, which is available in several versions for connection to most popular PCs and workstations.

Three programmable pushbutton switches on top of the housing, like mouse keys, allow the user to pick objects or menu selections on the computer screen. A fourth mode-select button on the front of the unit signals whether a lateral (up-down, left-right, forward-back) or corre-

spondingly angular motion (pitch, yaw, roll) is being reported to the screen for applications requiring all six degrees of freedom.

In the default mode, the GyroPoint's motion data is translational to emulate the host-computer-system's native mouse. Pressing and holding the front button issues rotational motion data. The convention for interpreting this data is defined



2. A TYPICAL GYROSCOPE used in military aircraft (right) weighs about 5 lb. and is 5 in. wide by 8 in. high. In contrast, the GyroEngine (left) is about the size of a roll of film. Five electrical contacts on the top of the GyroEngine provide power to the unit: two for power to the gyro motor, and three for torque voltage, which corrects for gyro precession.

by the user and application developer. Thus, the unit avoids the crosstalk (image jitter) problems associated with pointers that report all six degrees of freedom simultaneously. Located on the bottom of the unit is the pointer's on/off switch.

An LED indicator on top of the pointer reports the mouse's operating status and fault conditions, such as gimbal lock. Gimbal lock occurs when the pointer (outer gimbal of a gyroscope) is tilted more than 82 degrees from the spin axis of its inertia wheel, which would render motion sensing and reporting impossible. Gimbal lock is remedied by de-energizing the inertia-wheel motor, placing the GyroPoint in a horizontal position, and then re-energizing the motor. This recovery sequence is handled by the unit's internal control

electronics. The angular range for yaw is 360 degrees continuous.

The power requirement for GyroPoint is under 0.1 W. In its simplest mode, the unit is plug-and-play-compatible with any application that can use a Microsoft mouse or an Apple Macintosh mouse. Supporting RS-232C, RS-423, and Apple Desktop Bus interfaces, the GyroPoint has nominal data rates that range from 1200 to 4800 baud. Operating voltage for the GyroPoint is +3 V dc (+6 V dc for an RS-232 interface).

When used with IBM PCs or compatibles that don't need 3D support, the GyroPoint can work with Microsoft Windows drivers (MOUSE.DRV for Windows 3.0, or MOUSE.COM, or MOUSE.SYS for DOS applications). For the Apple Macintosh computer, the system comes with the standard Macintosh driver, and plugged into workstations from Silicon Graphics or Sun Microsystems, the pointers require a driver from the workstation vendor. Support of 3D-input requires custom drivers from a system or application vendor.

ENABLING TECHNOLOGY

Gyration's breakthrough in computer-pointer design is made possible by the company's development of a gyroscope about the size of a roll of film (Fig. 2). Where conventional gyroscope designs are large and heavy units with price tags ranging from \$1000 to \$200,000, the GyroEngine weighs just 1.2 oz., measures 1.25 in. in diameter and 1.75 in. high, and can be operated from a battery. Unlike prior gyroscope designs, which require external circuits to convert analog motion signals to digital form, the GyroPoint's gyroscopes generate digital motion signals with a 0.1-degree resolution, or 10 counts per degree.

The basic gyroscope mechanism follows conventional designs, which consist of an inner gimbal assembly containing the inertia wheel and motor, and an outer gimbal frame. To minimize weight and cost factors,

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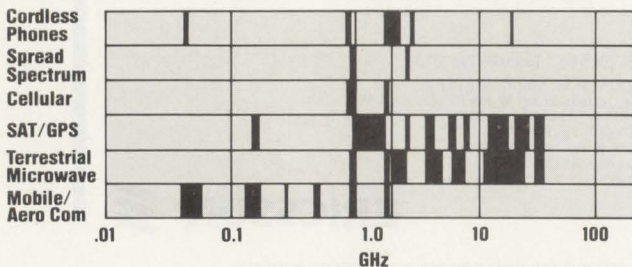
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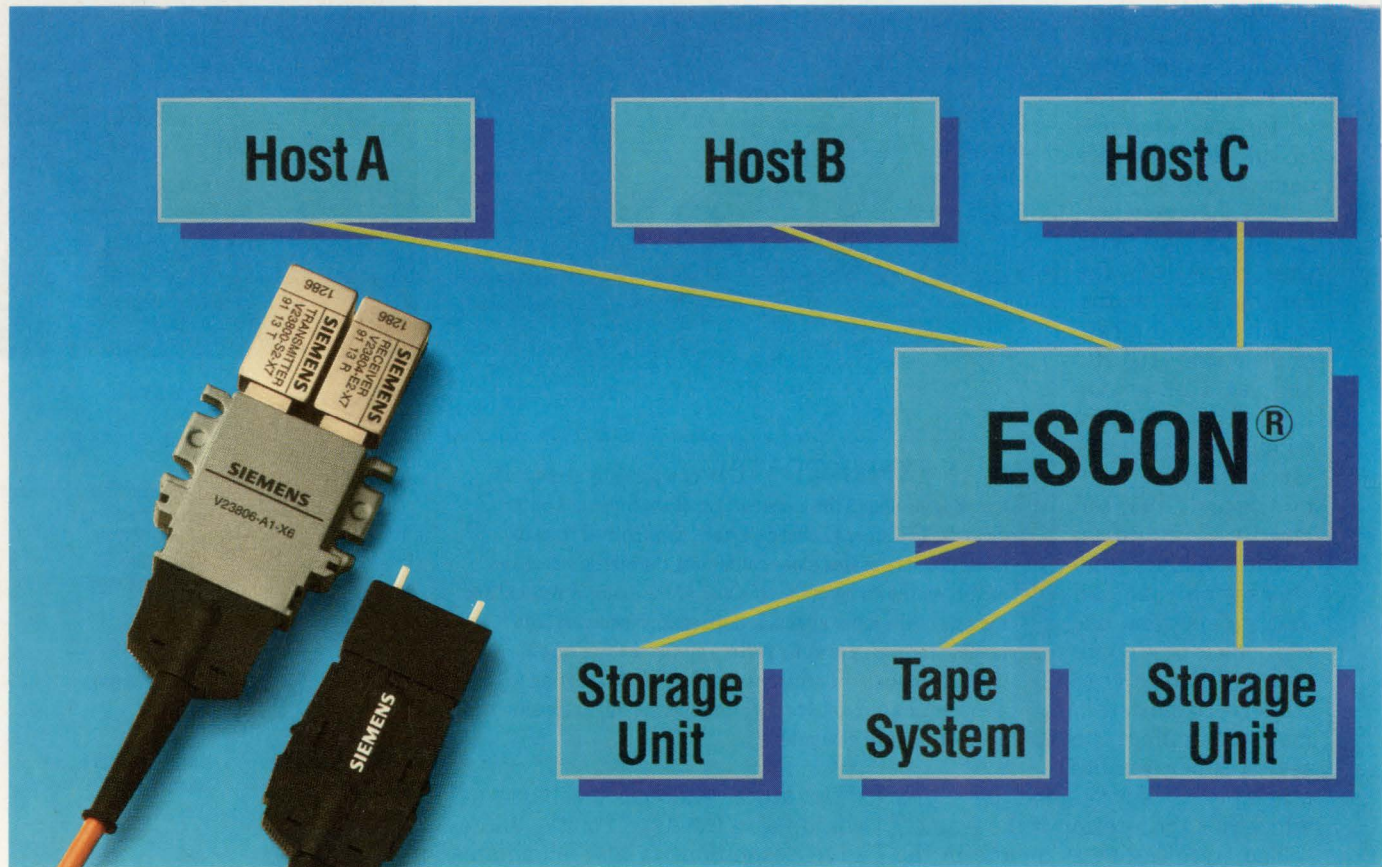
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CIRCLE 254 FOR U.S. RESPONSE

CIRCLE 255 FOR RESPONSE OUTSIDE THE U.S.

ASIC DESIGN SYSTEM

ic with bubble diagrams, arithmetic functions with datapath diagrams, and algorithmic functions with VHDL. The final description can be a combination of both text and graphics, and is then the basis for analysis and implementation.

Logic Assistant then converts the specification into behavioral VHDL code. The VHDL can be exported to a third-party VHDL simulator. Consequently, ASIC Navigator lets design teams perform analysis of their entire system, including the ASIC subsystems, to ensure that it works before proceeding to implementation. Simulation of the specification at the behavioral level allows design changes and debugging to occur early in the design process, resulting in a faster overall time-to-market and greater system reliability.

After the specification is approved, it can be converted into ASIC devices. However, users must first decide how to best implement this high-level design. The description may be partitioned into one or more gate arrays or standard cells, each of which can be created in a variety of different silicon implementations. Options include various architectures and packages.

Design Assistant helps users evaluate this variety of options to produce an optimal implementation. It evaluates users' partitioning and, for each ASIC and process technology, provides an estimated die size, various packaging options, power consumption, and estimated gate count (see the figure). Users can then interact with the tool on what-if analyses, exploring alternatives using different partitionings of the design or swapping standard cells for gate arrays or new process technologies. In this manner, users can find an optimum scheme that meets specification requirements.

Once a design solution is decided on, the behavioral description must be converted into gates. The job of converting behavior into a useful structure is generally still a labor-intensive operation, even with the availability of synthesis tools. Although commercially available logic synthesizers convert random logic

and state machines into net lists, large parts of a complex ASIC are still left for the designer to implement in other ways. For example, complex data paths and memory must still be done manually.

One option for designers is to choose existing cells in an ASIC library. The problem with this is that designers can't change these cells because they're off-the-shelf optimized functions that must be used as is. Another alternative is to use compiled cells. Unfortunately, designers must manually configure each compiled cell and import it into the larger design description along with the synthesized logic and any hardwired cells in the design.

CREATING LOGIC

Engineers need a tool that will take the ASIC system specification and automatically implement it according to the desired partitioning. With ASIC Navigator, this need is filled by the ASIC Synthesizer. ASIC Synthesizer creates random logic and state machines, compiles all the data paths in the design, and synthesizes the exact-size memory that users specify. In other words, it compiles the complete design directly from the ASIC system specification. In addition, floor planning determines optimal placement and provides accurate delay characteristics for timing analysis.

ASIC Synthesizer will produce portable net lists or a complete layout when used with the company's physical design system. The tool offloads engineers from having to manually convert behavior into gates. It produces a VHDL structural model of the just-completed ASIC with complete annotation of timing characteristics from floor planning. The VHDL model can then be used in a board- or system-level simulation.

Once the actual logic is generated, users must determine and implement the correct level of test coverage for the device. They must ascertain where to add built-in testability circuits to allow for greater fault coverage. Navigator's Test Assistant does this automatically.

Test Assistant helps users select

the right test architecture for their test strategy, and synthesizes the necessary structures and connects them within the design. It also generates all test vectors needed to control and test the test structures. Supported test schemes include internal scan, boundary scan, built-in self-test (BIST), and multiplexed isolation architectures.

Internal scan is supported by means of automatic synthesis of the scan chain during functional synthesis, or by automatic insertion into an existing structural design. Both multiplexed-flip-flop and level-sensitive scan-design (LSSD) schemes are provided. The Compass Scan ATVG (automatic test-vector generation) tool generates test vectors for the scannable design. The boundary-scan support is a full IEEE 1149.1 implementation. Test Assistant automatically builds the boundary-scan ring, inserts the chosen controller, and makes the appropriate connections to the chip circuitry.

ProFault is a probabilistic fault simulator within Navigator that performs fast and accurate determination of the fault coverage for the design. QTV is the system's timing verifier that informs users of the impact of the testability circuits on the design's timing.

After the design is completed, ASIC Navigator automatically generates the VHDL representation of the ASIC system at the behavioral and structural level, including full timing annotation at the structural level. Such good, detailed documentation is required by the Department of Defense. □

PRICE AND AVAILABILITY

The ASIC Navigator Design System will be available to beta sites in the first quarter of 1992. Full release is scheduled for the second quarter. The system runs on DEC, Hewlett-Packard, and Sun workstations, at prices starting at \$100,000.

Compass Design Automation Inc., 1865 Lundy Ave., San Jose, CA 95131; Terry Strickland, (408) 434-7943. CIRCLE 512

How VALUABLE?	CIRCLE
HIGHLY	568
MODERATELY	569
SLIGHTLY	570

ETHERNET CHIP SET COVERS ALL 802.3 APPLICATIONS

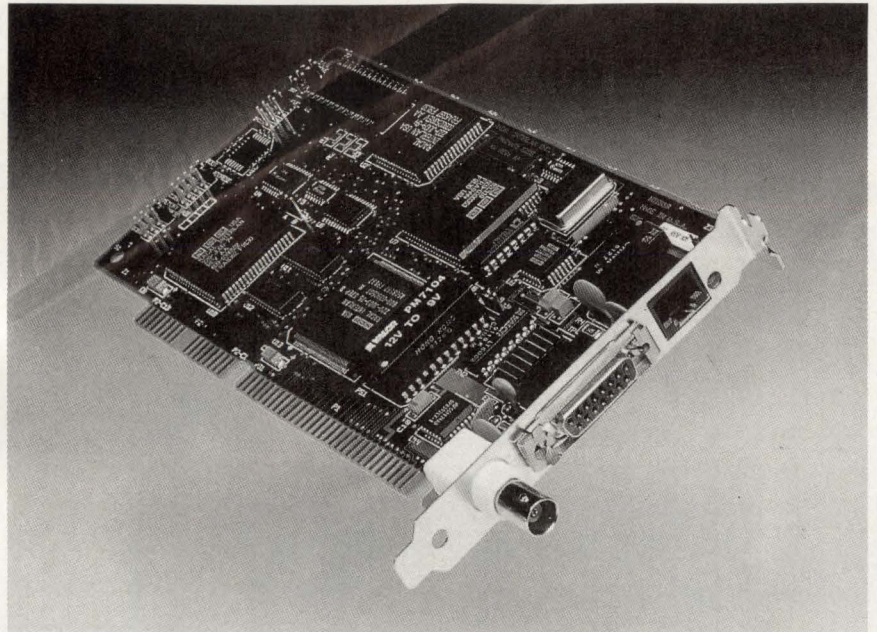
MILT LEONARD

A joint development by NCR Microelectronic Products Div. and Racal-Datacom has produced the 92C1XX family of Ethernet chips which provides all the functions necessary for implementing any 802.3 application. NCR will offer the chip set to the merchant market, and Racal-Datacom will market the first board product using the chip set. Based on NCR's EtherCore technology, the four-chip set contains the NCR92C110 media-access controller (MAC) with an embedded Manchester encoder/decoder (MENDEC) and attachment-unit interface (AUI), the NCR92C105 network-management module (NMM), the NCR92C143 ISA slave/host-interface module (ISASHIM), and the NCR92C140 bus-interface module (BIM). Target applications include 802.3 LAN adaptor cards, PC and workstation motherboards, pocket and laptop LANs, and X-terminals.

Containing all the MAC-layer control functions for IEEE 802.3 LANs, the 92C110 includes separate control and data buses for concurrent control and data transfers. With the use of appropriate bus-interface logic, the chip is also capable of accommodating 8-, 16-, or 32-bit systems.

Reloading FIFO-buffer data after a collision is not required for automatic retransmission of a data packet. The chip also accepts both broadcast and multicast address packets, supports ten network addresses internally, and provides for external address checking in bridge applications. Three loopback-diagnostic modes are available for checking the controller only, for checking the controller and MENDEC, and for checking the controller, MENDEC, and transceiver. The MAC comes in an 84-pin PLCC or an 80-pin QFP, and is priced at \$12.95 each in quantities of 5000.

The 92C105 NMM tracks and controls all 37 network events specified by the 802.3 standard. Chip capabili-



ties include collecting information on several packet-transmission and reception events, packet-transmission retry history, and total packet size in bytes. The NMM can be used as an option to configure a LAN product which fully supports layer management. Packaged in a 68-pin PLCC, the 92C105 is priced at \$10.95 each in quantities of 5000.

Supported by any required glue logic, the 92C143 ISASHIM can be substituted for other standard bus interfaces such as Extended Industry Standard Architecture (EISA) or IBM's Micro Channel Architecture (MCA). The host interface can also be configured for proprietary architectures by integrating the user's bus logic.

This device is targeted for ISA-compatible applications such as 8- and 16-bit Ethernet adaptor cards or PC motherboards. It supports four levels of system interface: I/O, interrupt control, memory slave, and interface to the MAC chip. The 92C143 is available in a 120-pin PQFP for \$13.90 each in quantities of 5000.

The fourth member of the chip set, the 92C140 BIM, interfaces the host-

system bus with the EtherCore-based LAN for proprietary systems or for standard bus architectures. Sixteen-bit systems require one 92C140 per system, and 32-bit systems can use two BIMs without any additional glue logic. The BIM also provides a transparent data path between the Ethernet controller and on-board memory. The chip is packaged in an 84-pin PLCC and is priced at \$9.95 each in quantities of 5000.

NCR's EtherCore chip set will first be applied in Racal-Datacom's NI6610-3M PC Ethernet card, a triple-media, 8/16-bit plug-in for IBM PC XT/AT, PS/2 Models 25/30, and IBM compatibles (*see the photo*). The card has connectors for thick Ethernet, thin Ethernet, and 10Base-T media. Priced at \$369 each in production quantities, the card will be available in December 1991.

NCR Microelectronic Products Div., 2001 Danfield Ct., Fort Collins, CO 80525; (303) 226-9550.

CIRCLE 484

Racal-Datacom LAN Inter-networking Div., 155 Swanson Rd., Boxborough, MA 01719; (508) 263-9929.

CIRCLE 485

DATA-ACCESS ARRANGEMENT COMES IN A DIP

Thanks to advanced micromodule technology, the circuitry that connects a modem to the public switched telephone network is now available in a DIP-size module

that's less than 0.4-in. high, and occupies an area of about 1 in.². The 73M9001 from Silicon Systems can be used in modems in notebook, laptop, and palmtop PCs which are required to meet the performance requirements of

CCITT V.32 and V.32bis.

A proprietary VLSI chip with die-on-board mounting contains transmit and receive amplifiers, a programmable audio monitor, and relay drivers. Also contributing to the small size is a proprietary miniature transformer with a high-permeability ferrite core. The module also contains the circuitry needed to meet FCC part 68 and UL 1459 second-edition standards, which include a 1500-V isolation-barrier test.

Other features are an off-hook relay, ring detection, 2-to-4-wire conversion, signal processing for correct transmit and receive levels for applications up to 14.4 kbits/s, and a power-down mode. Power consumption is 55 mW in the active and 10 mW in the power-down mode. The 73M9001 is priced at \$17 each in quantities of 10,000.

Silicon Systems, Inc., 14351 Myford Rd., Tustin, CA 92680; (714) 731-7110.

CIRCLE 456

■ MILT LEONARD

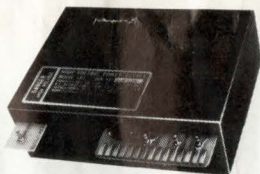
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CIRCLE 318 FOR U.S. RESPONSE

CIRCLE 319 FOR RESPONSE OUTSIDE THE U.S.

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Philips Components, Discrete Product Div., 2001 W. Blue Heron Blvd., Riviera Beach, FL 33404-5099; Miriam Coleman, (407) 881-3257. **CIRCLE 457**

NEW PRODUCTS

DIGITAL ICS

LASER-PRINTER CONTROLLER PROCESSES 2000 CHARACTER/S

Character generation in laser printing and display usually causes a bottleneck within the system. The Adobe Type 1 coprocessor eliminates that bottleneck. The chip

can render text at up to 2000 characters/s, said by the company to be 25 times quicker than the fastest RISC-based printer controllers available today.

The Type 1 coprocessor performs all

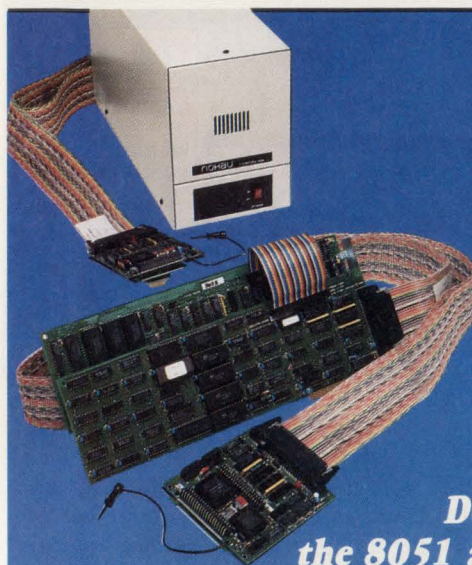
the steps of rendering characters from any of the more than 10,000 available Type 1 outline fonts. These steps, now done in hardware, were traditionally performed in software. The steps include program interpretation, hint processing, transformation of font-outline coordinates, and intelligent character filling.

The coprocessor can be incorporated into PostScript printers and display controllers, regardless of the CPU chip that's employed. Printers with the chip will run at their rated engine speed, regardless of the number of fonts and point sizes in a document. This also holds true for Kanji characters, which typically put a heavier burden on the font-processing devices.

Although the part was developed by Adobe, the company won't sell the chips; instead, it hopes to license the technology to companies building laser printers. Samples of the Type 1 coprocessor are now available.

Adobe Systems Inc., 1585 Charleston Rd., P. O. Box 7900, Mountain View, CA; (415) 961-4400. **CIRCLE 460**

■ RICHARD NASS



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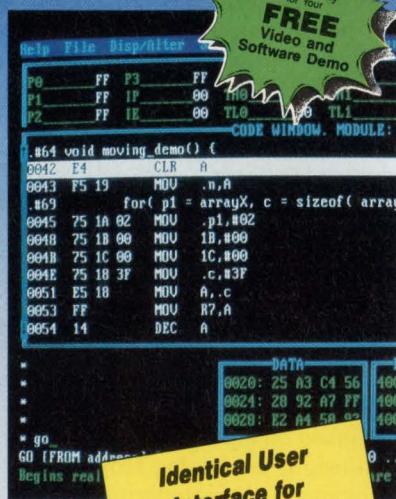
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CIRCLE 210 FOR U.S. RESPONSE

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A trio of ECL-to-CMOS transceivers, the SC3001, 3002 and 3010 are all 40-bit fully registered biCMOS chips that can work at system speeds of up to 100 MHz. The bidirectional SC3001 has separate ECL inputs and outputs for maximum data transfer rates and minimum skew. The CMOS side has bidirectional three-state 50-mA symmetrical outputs that include internal "soft" termination to improve signal fidelity when driving highly capacitive loads. The SC3002 is similar to the 3001, except that it has common ECL input and output lines. The 35-Ω output drivers can handle 70-Ω ECL double-end terminated buses and backplanes. Rounding out the trio is the SC3010, a unidirectional ECL-to-CMOS synchronous translator designed to propagate ECL addresses and control signals into a CMOS environment. When used to control a DRAM array, the chip can be set up to provide time-multiplexed "double" copies of the RAS and CAS. All three chips have built-in scan testability. All are immediately available, and in 100-unit lots, they sell for \$107 apiece.

Silicon Connections Corp., 16868 Via Del Campo Court, San Diego, CA 92127; Dave Zimpfer, (619) 674-1050. **CIRCLE 461**

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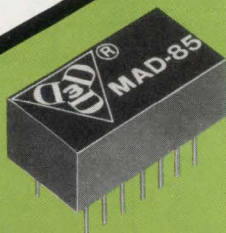
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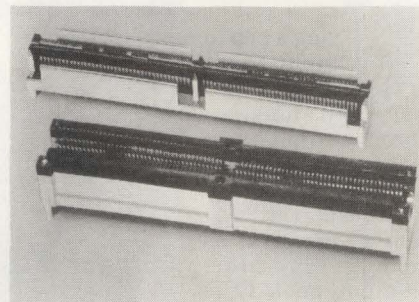
CIRCLE 144 FOR U.S. RESPONSE

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NEW PRODUCTS

PACKAGING

HIGH-DENSITY CONNECTOR LINKS DIGITAL BOARDS

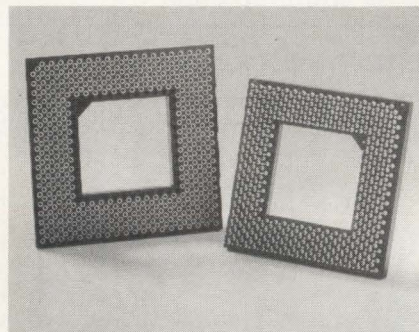


For low-crosstalk interconnections in high-speed, digital-system applications, the Micropax board-to-board connector comes in 0.050- and 0.025-in. centerlines. The stackable connector is also being used as a docking connector in notebook PCs. Die-cast metal housings deliver good electrical and mechanical performance. The receptacle and header come in straddle-mount and vertical through-mount configurations. Call for pricing and delivery information.

DuPont Connector Systems, Barley Mill Plaza, Wilmington, DE 19898; (800) 237-4357. CIRCLE 464

INTERSTITIAL SOCKET BOOSTS PGA PIN DENSITY

A family of interstitial pin-grid-array (PGA) sockets delivers a 55% increase in pin density compared with conventional PGA sockets. The sockets pro-



vide a means of mounting the MIPS R4000 RISC processor as well as other devices offered in interstitial arrays. A screw-machine receptacle with an ultra-low insertion force greatly reduces the forces encountered with the high pin counts of interstitial packages. Pricing is \$35.18 in lots of 1000 for the PZA 447H509B5-39C-R (for the R4000 CPU). Small quantities are delivered from stock.

McKenzie Technology, 44370 Old Warm Springs Blvd., Fremont, CA 94538; (510) 651-2700. CIRCLE 465

NEW PRODUCTS

INSTRUMENTS

IEEE-488



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16-MHz 386sx EMULATOR ADDS NO WAIT-STATES

The CodeStalker 386sx, an emulator for the 386sx microprocessor, runs at 16 MHz with no wait states. Its 4-ksample trace memory captures machine cycles at full speed, and its four independent hardware breakpoints can be set anywhere in the processor's address space, in either RAM or ROM locations. A programmable trace trigger can delay trace acquisition until a particular address or range of addresses is encountered, or it can stop collection on the same condition. External hardware events can also trigger trace collection. Users can also set an unlimited number software breakpoints. The emulator includes 512 kbytes of overlay RAM that can be split into two separate banks. By sacrificing complex breakpoints and performance-analysis features, the CodeStalker 386sx fills a niche between low-end runtime-only units and large development systems costing \$20,000 or more. The CodeStalker 386sx, including a source-level debugger that works with most C compilers, costs \$9995 and is available from stock.

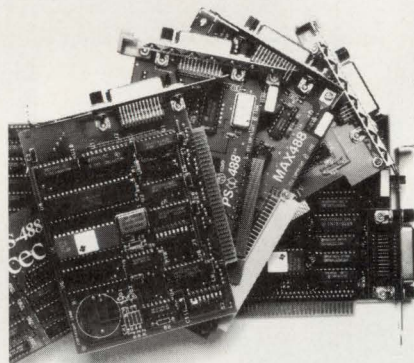
Softaid Inc., 8300 Guilford Rd., Columbia, MD 21046; (800) 433-8812 or (301) 290-7760. CIRCLE 466

TRUE 4-CHANNEL SCOPE HAS 200-MHz BANDWIDTH

The PM 3094 analog oscilloscope delivers true 4-channel, 200-MHz capability in an economically priced instrument. Unlike 4-channel scopes with a 2+2 configuration, the PM 3094 has four individual amplitude settings and offers a full range of 2 mV to 5 V on each channel. In addition, users can make dual-trace differential measurements using two traces. The scope features automatic setup on all channels, as well as

on-screen cursor measurements. In place of the traditional potentiometers and trim capacitors, the PM 3094 uses digital-to-analog converters and vari-caps. Signal switching is done under microprocessor control. This arrangement allows automatic, closed-case calibration to within 1% accuracy for cursor measurements. The PM 3094 costs \$3390 and is available within 4 weeks of ordering. A 2+2 version, the PM 3092, costs \$2990.

John Fluke Mfg. Co. Inc., P.O. Box 9090, Everett, WA 98206-9090; (206) 347-6100. CIRCLE 467



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A Macintosh-compatible hardware and software package performs real-time data acquisition, analysis, and display at up to 100 MHz. The ADC488/16 digitizer offers 16 single-ended or eight differential analog inputs. The ADC488/8S has eight differential analog inputs. The digitizers' 100-kHz sample rates permit capture of repetitive signals with bandwidths to 50 kHz and transients as fast as 20 μ s. The companion software, SuperScope, features an on-screen, virtual front panel that allows access to the package's features through the Mac's point-and-click interface. The software supplies 45 analysis functions and displays up to eight waveforms at once. Bundled as the SS-Pack/16, an ADC488/16, SuperScope, and an IEEE-488 interface, software, and cable cost \$2995. Separately, Su-

perScope costs \$995; the ADC488/16, \$1795; and the ADC488/8S, \$2295.

Iotech Inc., 25971 Cannon Rd., Cleveland, OH 44146; (216) 439-4091.

CIRCLE 468

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Two software packages are designed to simplify capacitance-vs.-voltage (C-V) testing of semiconductors while improving accuracy and productivity. The Model 5957 Simultaneous C-V Software package helps users obtain both high-frequency (100 kHz and 1 MHz) and quasi-static capacitance measurements. The Model 5958 C-V Utilities Software offers high-frequency device characterization and production-monitoring tools. The Model 5957 supplies instrument-control, measurement, and analysis capability for all the hardware in a simultaneous C-V system. The Model 5958 performs a variety of process control tests. The package supports all the capabilities of the Model 590 C-V analyzer, including ranges from 2 pF to 2 nF, pulsing, and sweep rates up to 1000 points per second. In addition to many of the same analysis capabilities of the Model 5957, the Model 5958 has features for users working in production control. The Model 5957 costs \$1990 and the Model 5958 costs \$2490. Delivery is within 2 weeks.

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1150 or (216) 248-0400. CIRCLE 469



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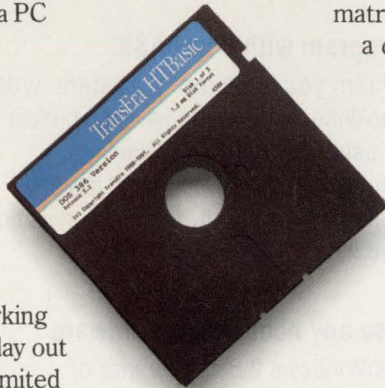


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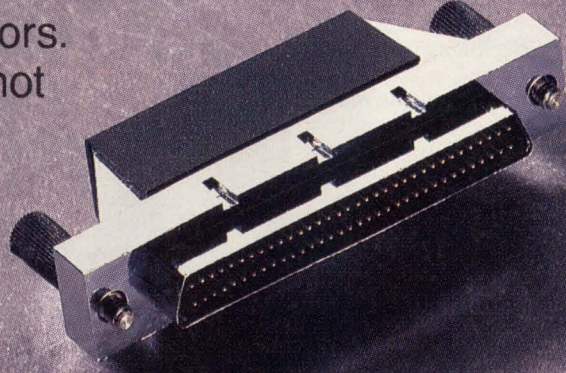
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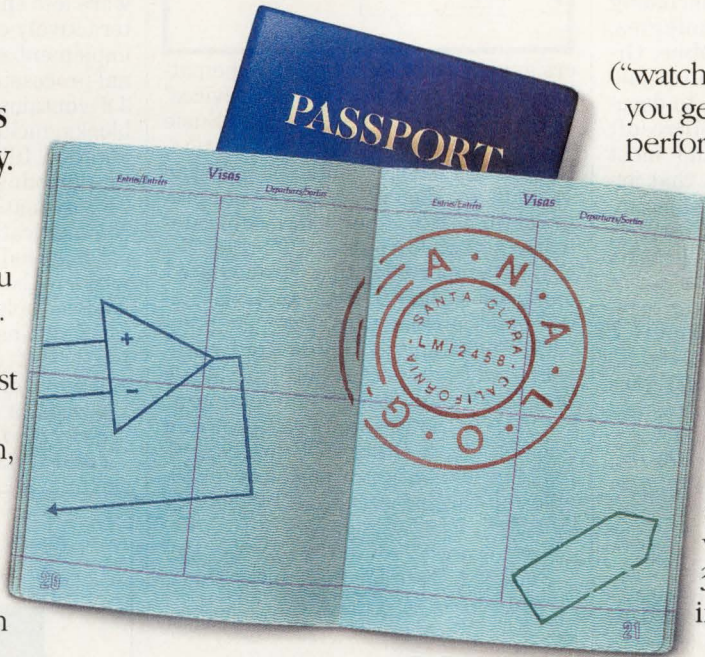


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("watchdog" comparison mode) you get optimized system performance at a throughput rate of 87kS/s min. A four-channel version will be available in 1992.

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These commands allow

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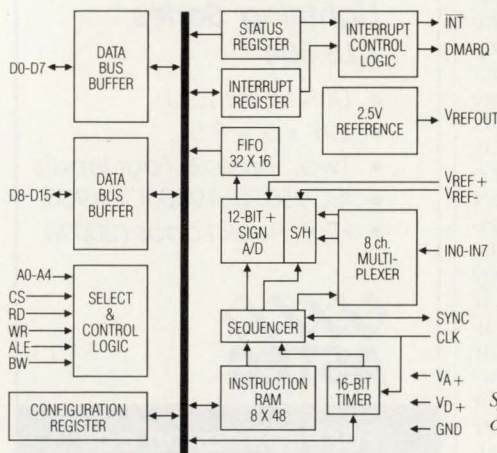
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Besides doubling the power of the company's 15-W MTO Series' industry-standard pinouts, the converter increases the operating temperature and input voltages to full military ranges.

High-frequency (575-kHz) conversion permits reduction of the package height by about 20%. The units are also built using a modular manufacturing system that lowers the cost per watt by at least 40%.

As a triple-output device, the converter offers an advantage to designers. Often, systems require a combina-

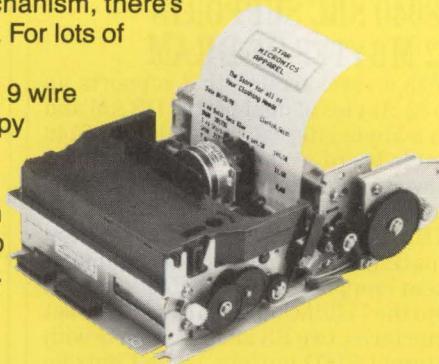
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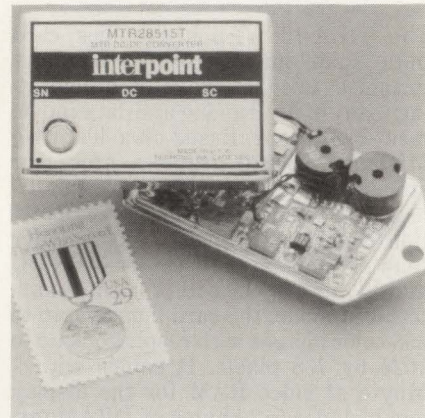


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CIRCLE 268 FOR U.S. RESPONSE

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tion of 5 V to power digital logic and either +12 or +15 V dc to drive linear components. The best way to handle this requirement is with one multiple-output supply that converts the power bus to the three voltages. For 15 W and less, the MTO Series does the job. But for higher power levels, designers have had to squeeze in two 15-W parts. That's where the cost and space savings of the MTR Series comes in.

A wide input range of 16 to 40 V dc is offered, as is an efficiency rating of over 77%. The units are fully isolated and carry typical line and load regulation as low as 15 mV. Also, highly flexible loading permits up to 67% of the total rated output power to be drawn from the main output and up to 30% from either auxiliary output. At 1.345 by 1.950 by 0.41 in., power density is up to 28 W/in.³.

A fixed-frequency, pulse-width-modulated design is used for low noise. Internal filters provide typical output ripple voltage of 30 mV pk-pk and input ripple current of 20 mA pk-pk. Audio rejection is up to 50 dB. MTBF is about 100,000 hours per MIL-HDBK-217.

Prices for the MTR Series dc-dc converters start at \$449 in lots of 100. Small quantities are available from stock.

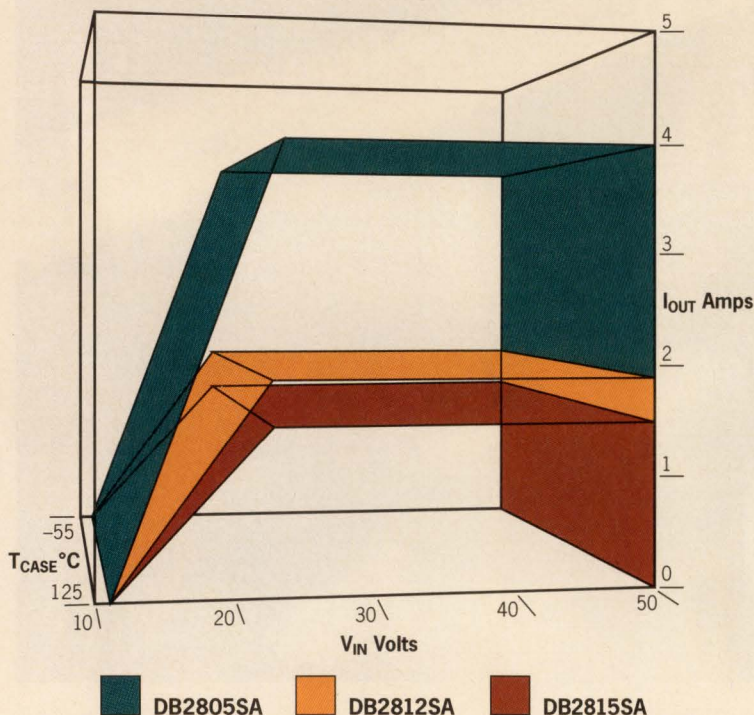
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CIRCLE 483

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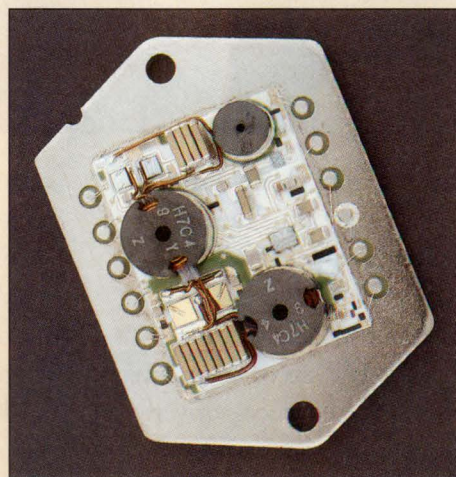


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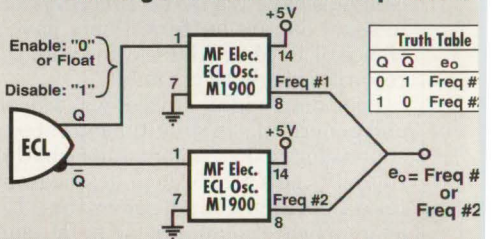
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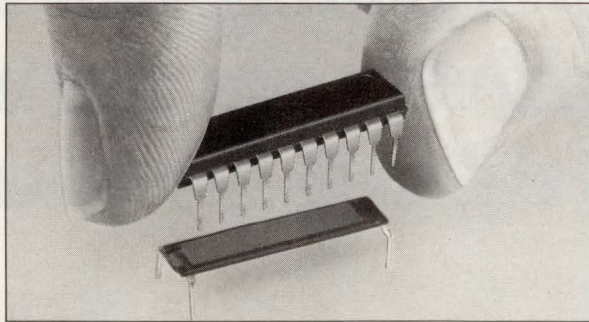
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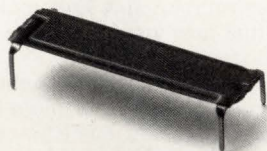
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CIRCLE 234

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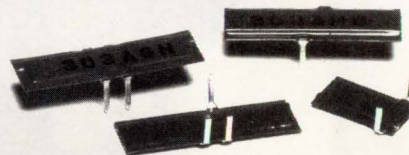
Improve board performance without redesign. Noise problems are solved by retrofitting on existing boards.



CIRCLE 235

MICRO/Q 1000 CUSTOM CAPACITORS

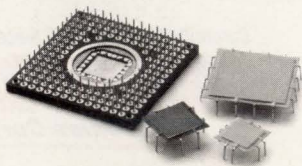
Special pinouts are available to address the wide variety of specialty DIPs such as analog devices, op-amps, and the center pinout advanced CMOS devices. Applications include: decoupling, EMI/RFI filtering, and compensation.



CIRCLE 236

MICRO/Q 3000 CAPACITORS

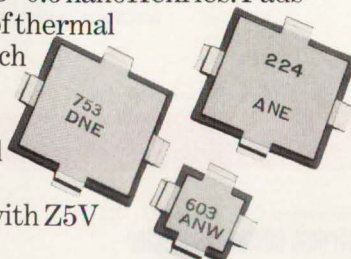
Reduces noise associated with the use of PGA and PLCC devices. Several part sizes are available to address a variety of package sizes, Micro/Q 3000 is designed to be used with all 16/32-bit MPUs, DSPs, GSPs, FPPs, gate arrays, standard cells, and fully custom ASICs.



CIRCLE 237

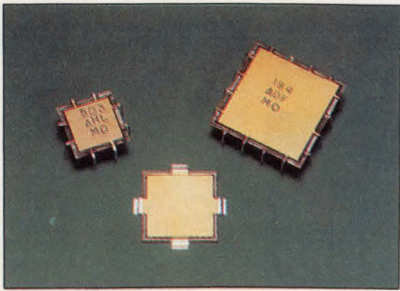
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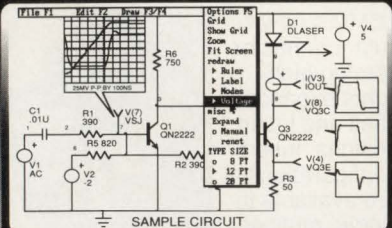
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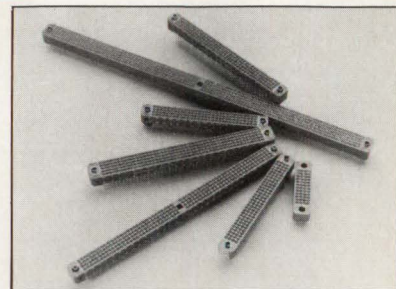
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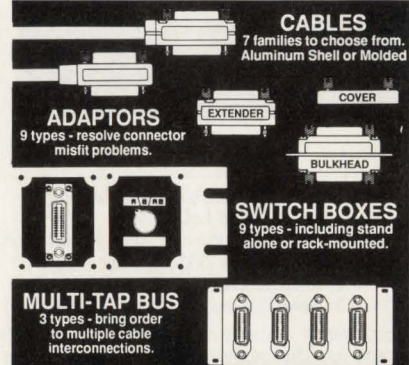


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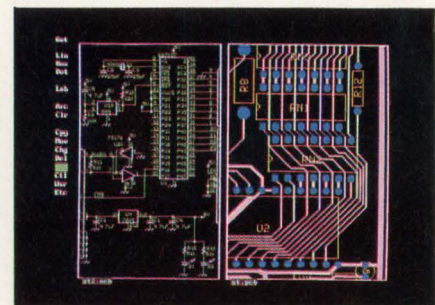


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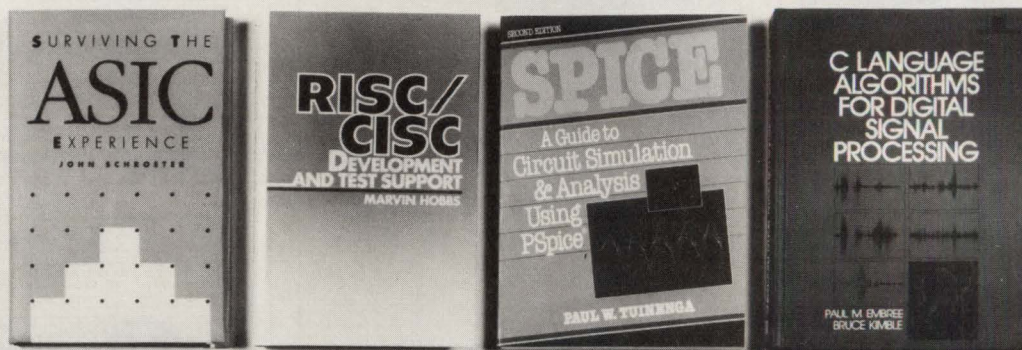
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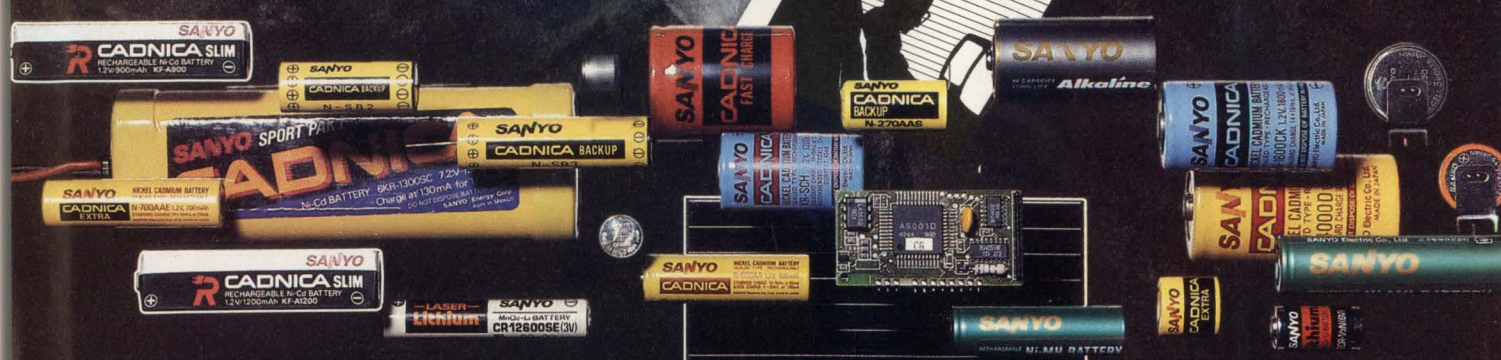
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t_s Settling Time (to 0.1%) (Typ)	90	90	100	75	340*	nsec
A_{VOL} Open Loop Gain (Typ)	50	7	45	28	450	V/mV
V_{OS} Offset Voltage (Max)	1	2	6	3	0.9	mV
I_{OS} Offset Current (Max)	0.3	0.4	1	—	.00005	μA
I_B Bias Current (Max)	0.3	8	1.7	3	.0001	μA
e_n Voltage Noise (f = 10KHz)	17	22	25	3.3	15	nV/ \sqrt{Hz}
i_n Current Noise (f = 10KHz)	3	1.5	4	2.1	.002	pA/ \sqrt{Hz}
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