ELECTRONIC DESIGN

JANUARY 9, 1992

FOR ENGINEERS AND ENGINEERING MANAGERS--WORLDWIDE

TECHNOLOGY FORECAST: BUILDING ON TODAY'S FOUNDATIONS

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- AN EARLY LOOK AT THE ISSCC
- TWELVE INVITED EXPERTS PREVIEW THE FUTURE

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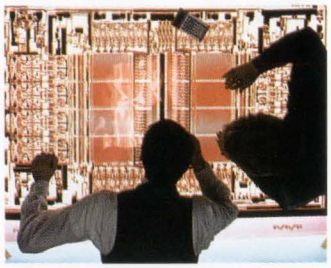

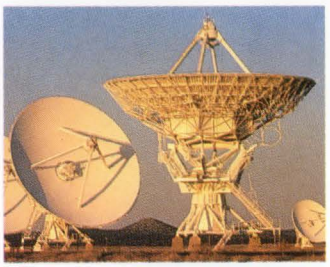

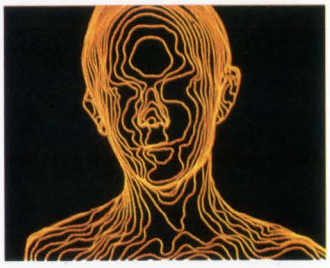

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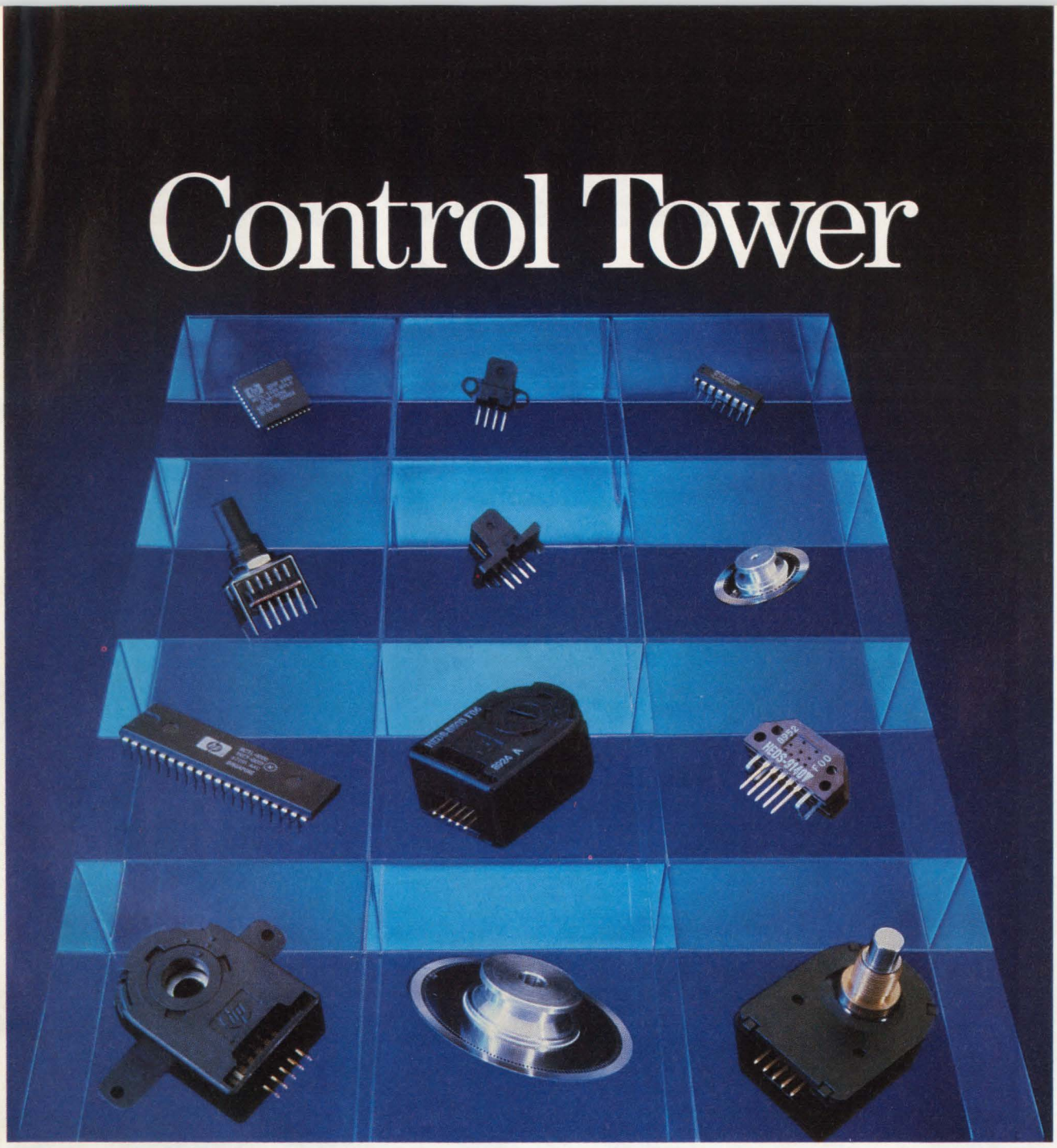
Control Tower



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JANUARY 9, 1992 VOL. 40, NO. 1

ELECTRONIC DESIGN

40 YEARS OF EDITORIAL EXCELLENCE

COMING NEXT ISSUE
- Special Report: Memory-card technology opens up new schemes for I/O connections
- PIPS Special Section: Power, Interconnections, Passive components, Switches and Relays
- Designing for electrical-transient immunity
- First details on new special-purpose DRAMs
- Using single-slope a-d conversion for low-cost solutions
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1978 Certificate of Merit
1980 Certificate of Merit
1986 First Place Award
1989 Certificate of Merit

Correction: On page 26 in our November 21, 1991 issue, the telephone number for CMX Systems was listed as (203) 238-2622. It should be (203) 238-3622. Also, the positioning system was correctly cited as the CMX 3030 in the initial part of the story, later it was incorrectly called the CMS 3030. *ED*

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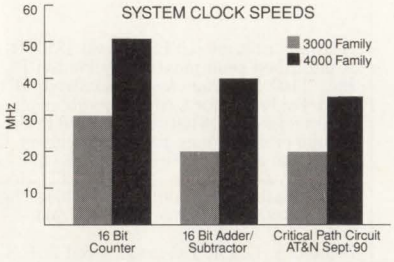

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Device speed alone doesn't determine the fastest, highest-performance logic device.

When you're designing, the clock on the wall is every bit as important as the clock speed of the chip.

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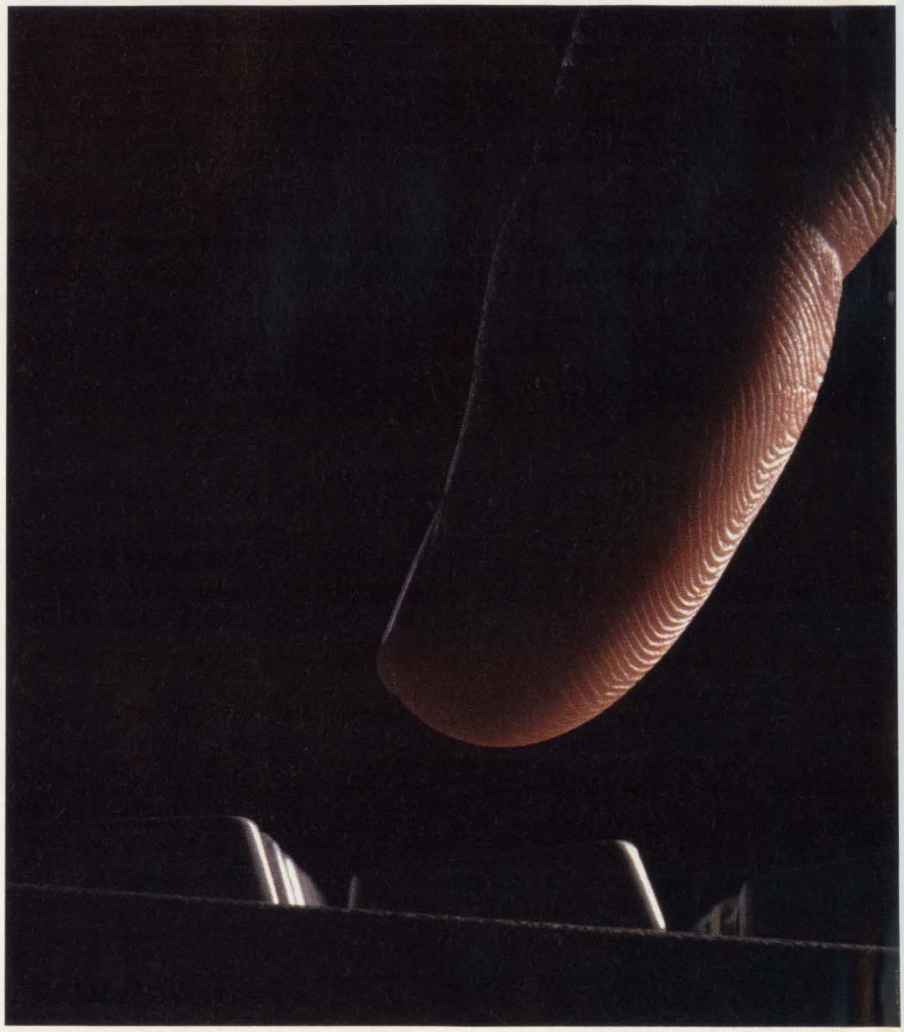

Our new push-button software makes programming other logic devices seem positively tedious.

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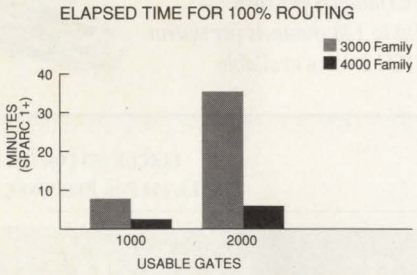
And not only do our FPGAs save you an enormous amount of time early on, they also save you time later when you need to make those "last minute" enhancements.

It's one more way we make it easier for you to get your product to market as fast as possible. First time. Every time.



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CIRCLE 244 FOR U.S. RESPONSE

CIRCLE 245 FOR RESPONSE OUTSIDE THE U.S.

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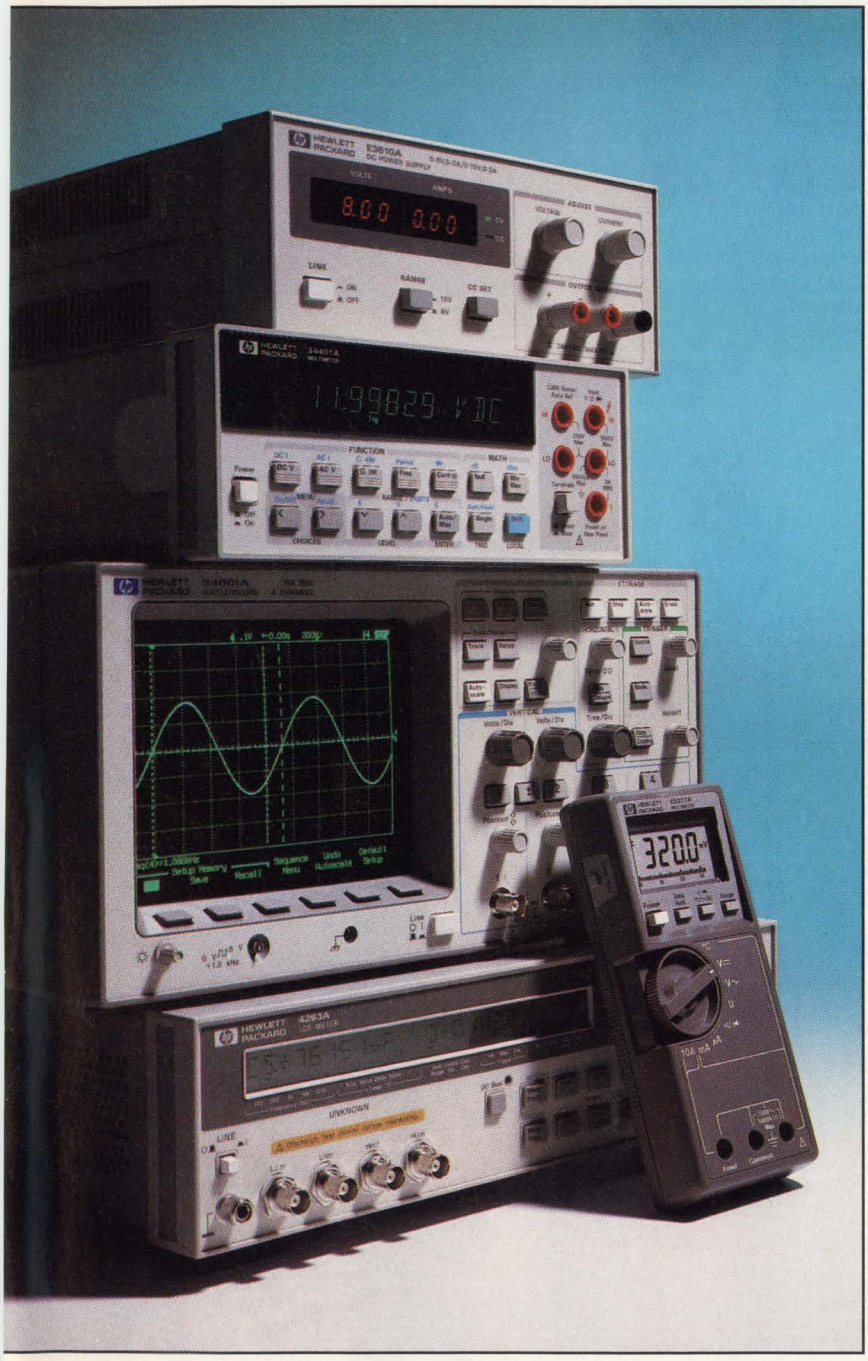

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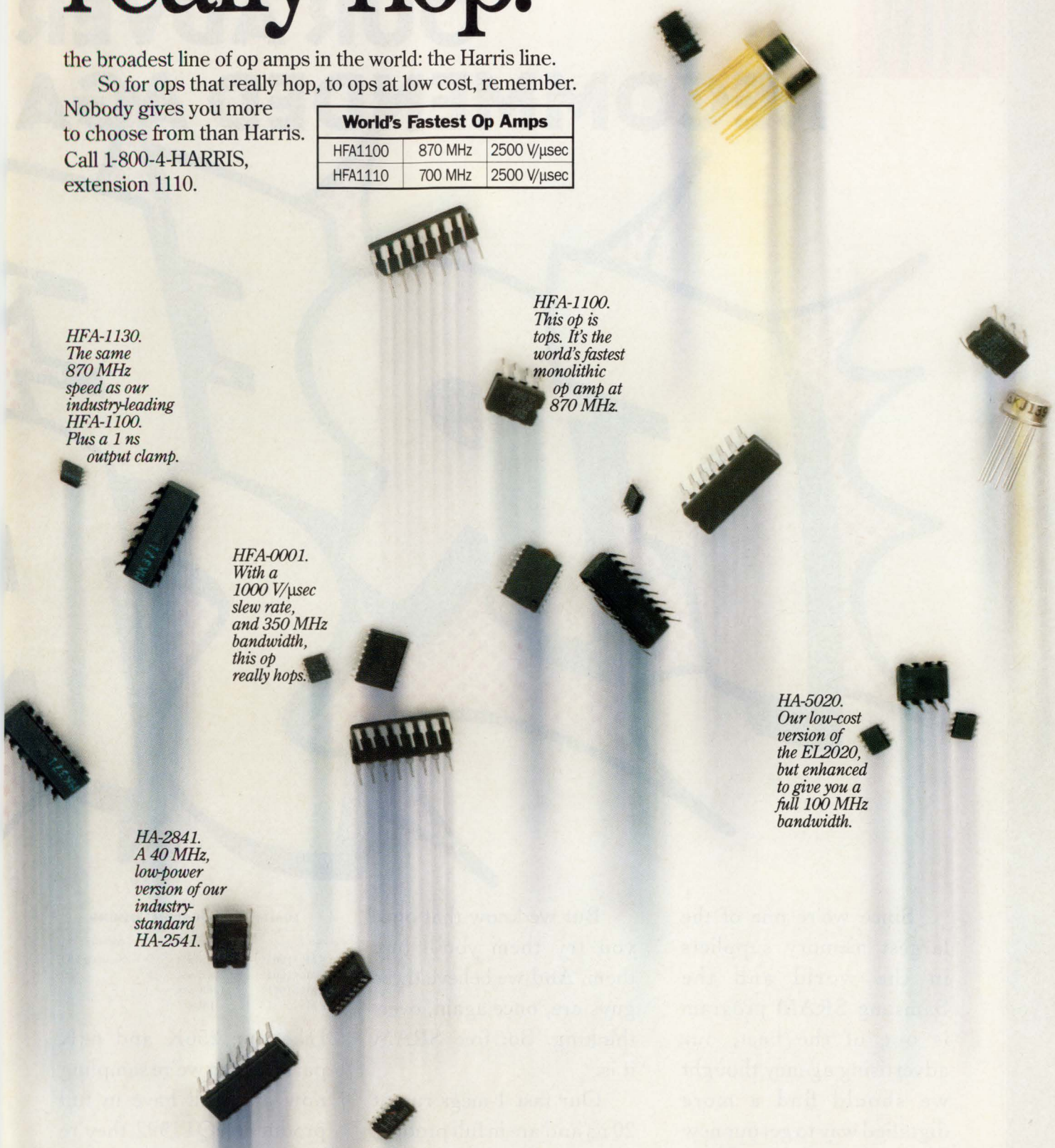

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KM64257A*	64K x 4	
KM6466B*	16K x 4	Output Enable
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CIRCLE 198 FOR U.S. RESPONSE

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MORE THAN JUST ANOTHER YEAR

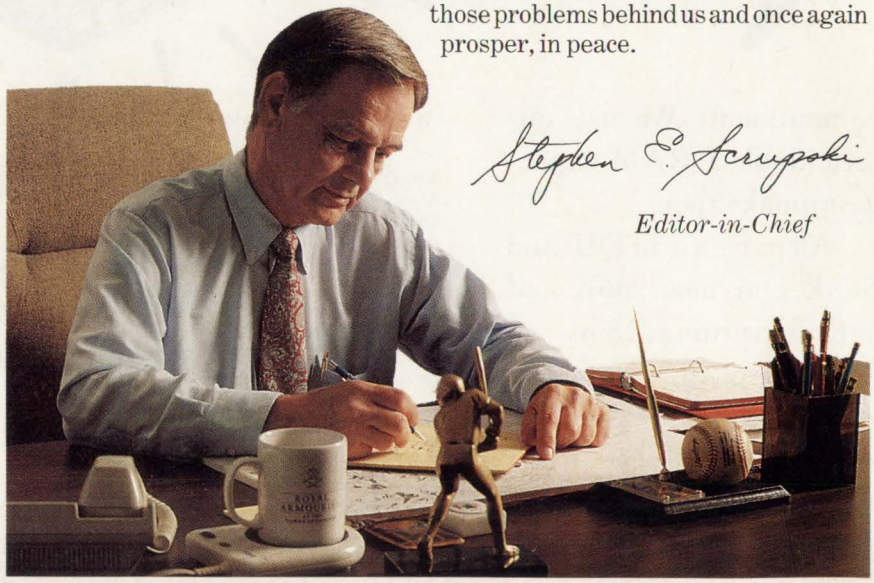
Happy new year! 1992 is a landmark year for us at Electronic Design because it marks our 40th anniversary, and, to highlight this event, we've planned a Special Issue in November. Throughout the coming months, we'll give you more details on the Anniversary Issue. We'll also offer you an opportunity to participate by asking for your inputs on the contents of certain special sections that we're considering.

Despite the urge to wax nostalgic at such times, the basic thrust of the issue will be the future. Electronic Design is built on the foundation of giving its readers a look ahead at the technologies and products that will help them attain a competitive edge in their next product. Thus, we plan to devote most of that blockbuster issue to articles that focus on the future, rather than on the past: a look ahead at possible technology breakthroughs and their impact on system performance.

As for this issue, those of you who are longtime readers of Electronic Design know that the first issue of each year features our Technology Forecast Special Report. This year, we return to fundamentals with a report on the enabling technologies that will lead to future advances in product performance. The Technology Forecast, which begins on p. 37, features four staff-written pieces that focus on digital semiconductors, linear and mixed-signal semiconductors, optoelectronics, and packaging. Two further articles look at networking for the global design environment and techniques for designing with multichip modules. The report closes with ten one-page articles that assess the trends in ten specific technologies: microprocessors, displays, EMI, micromachining, instrument accuracy, test probes, capacitors, power supplies, magneto-optical memories, and computer boards.

We have, in fact, a full slate of technology special reports and design applications on tap for our 26 issues this year. Also returning are such popular sections as Pease Porridge, QuickLook, Ideas for Design, our technical conference previews, and our Salary and Career Surveys. In addition to the regular features, you can look forward to the PC Design and PIPS (power, interconnections, passive components, and switches and relays) special sections six times during the year, and our Test & Measurement Update four times.

We know that the coming year will unleash a host of interesting technology advances that will be covered in Electronic Design. Beyond that, here's hoping that 1992 not only advances technologically, but also politically and economically worldwide, where we can finally put those problems behind us and once again prosper, in peace.



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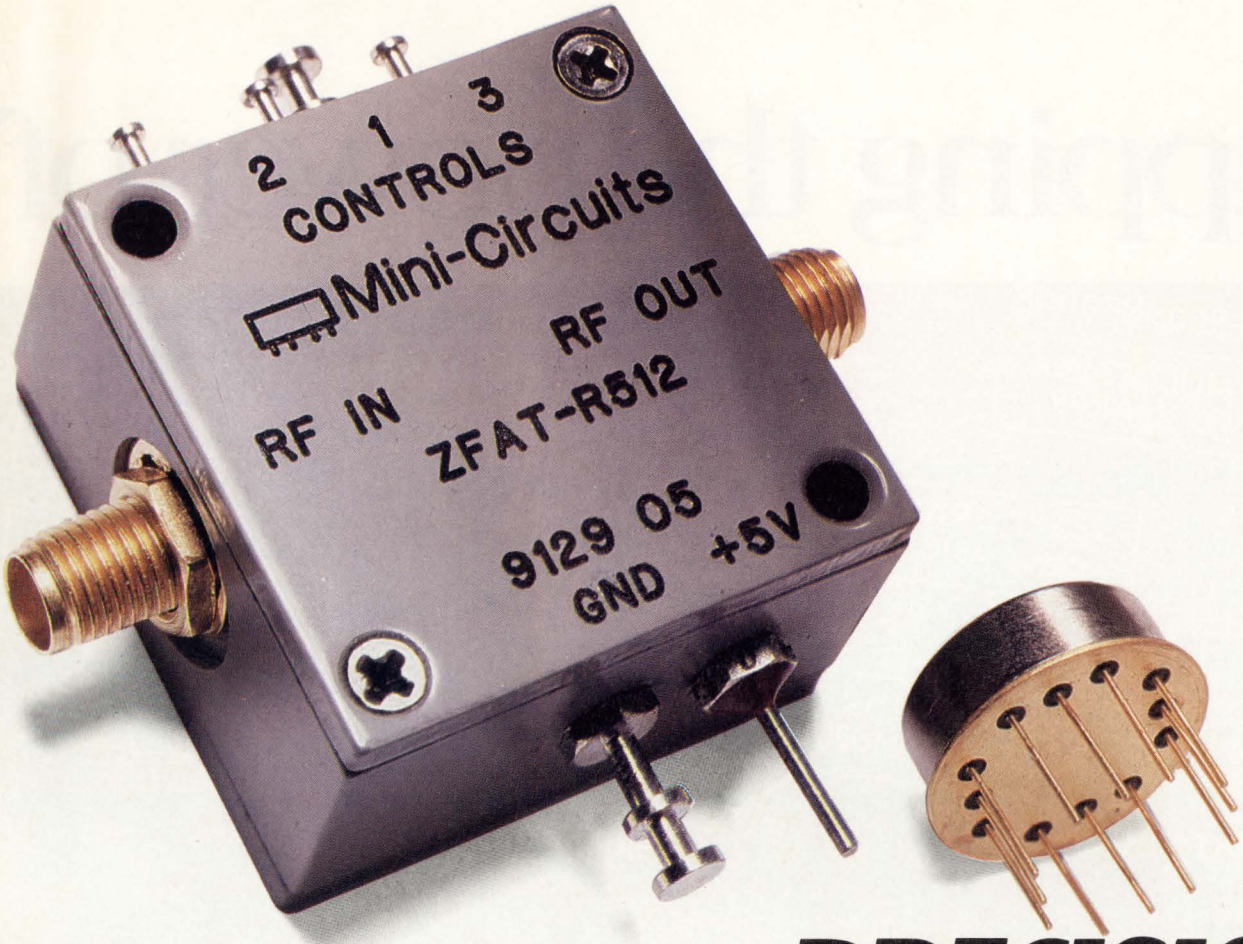
Editor-in-Chief



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1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

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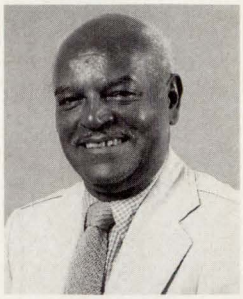

MILT LEONARD
SENIOR EDITOR

Attempts to replace the cathode-ray-tube (CRT) monitor with more manageable flat-panel display devices have met with little success. Even though they're bulky and generate lots of heat, the venerable CRT still sets the price and performance standards against which competing display technologies are compared. However, the surging demand for "thinness" in desktop and portable computers is accelerating the development of flat-panel displays with dramatically improved viewing quality, power consumption, and cost.

Of the three existing forms of flat-panel displays – liquid crystal (LCD), plasma, and electroluminescent (EL) – industry observers think active-matrix LCDs (AMLCDs) have the most potential to dominate the flat-panel market. AMLCDs use amorphous or silicon thin-film transistors (TFTs) to control individual pixels on the display panel. Overall AMLCD performance already exceeds or compares favorably with other flat-panel technologies in terms of viewing criteria. On the negative side are limited viewing angle, operating temperature range, and panel size; vulnerability to shock, vibration, and high humidity; and high power dissipation. The biggest drawback is cost. Today's color AMLCDs can cost up to 12 times as much as a color CRT, and from 5 to 10 times as much as other flat-panel technologies.

AMLCDs can now be fabricated with feature sizes under 5.0 μm. But unlike IC processing, where the probability of a defect landing on a die decreases as the number of chips on a wafer increases, AMLCDs are made with one "chip" per wafer. Therefore, further feature-size shrinks to get smaller "die" dimensions doesn't necessarily mean higher yields, which presently range from 10 to 40%. And to decrease cost, most industry efforts focus on minimizing process-related defects.

The industry's concern over AMLCD yield was apparent in new equipment rollouts at SEMICON/Japan last month. Various American, European, and Japanese firms introduced integrated processing systems that control contamination by using robotics and automated substrate transport between processing chambers under vacuum. But according to Francois J. Henley, president of Photon Dynamics Inc., San Jose, Calif., a yield loss of up to 40% can occur during electrical testing of a panel alone. This is because the testing technologies are adaptations of systems designed for IC testing.

What's also needed are non-intrusive in-process inspection and repair strategies that depart significantly from methods developed for the semiconductor industry. It's now understood that inspection and repair equipment for active-matrix LCDs should be designed around the requirements of AMLCD technology – namely automation, high throughput, in-process operation, noncontact and nondestructive inspection, and networked inspection and repair systems. This way, yield is boosted by detecting and repairing defective pixels prior to final panel assembly.

To obtain maximum AMLCD yield, the ultimate approach may be integrating such a system with automated processing schemes. Last year, Photon Dynamics introduced an inspection and repair system based on a patented noncontact pixel-sensing technique. The system uses several advanced technologies, including laser optics; laser-controlled physical optics; electro-optics; image processing; and electronics test, measurement, and inspection. A report from Stanford Resources Inc., San Jose, Calif., says this type of in-process testing can reduce manufacturing costs by about 50%, even with testing-equipment costs factored in. Integrated inspection and repair could further reduce manufacturing cost by another factor of three, the report states.

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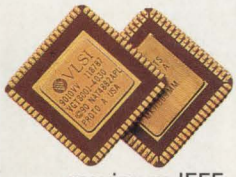

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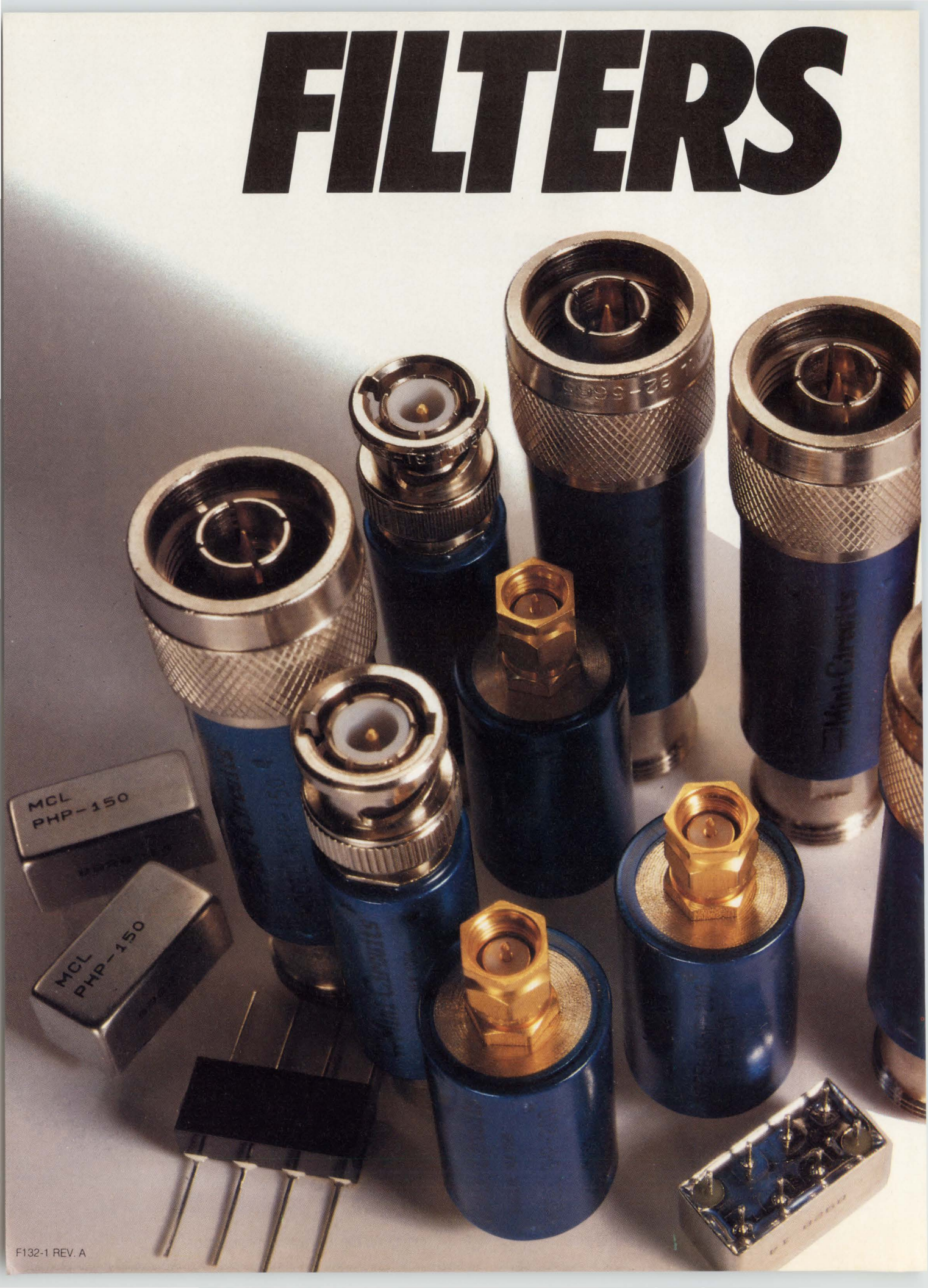
FILTERS



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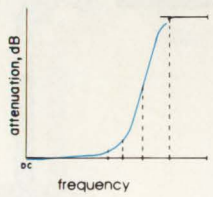
LOW PASS



low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
PLP-5	DC-5	8-10	10-200	PLP-250	DC-225	320-400	400-1200
PLP-10.7	DC-11	19-24	24-200	PLP-300	DC-270	410-550	550-1200
PLP-21.4	DC-22	32-41	41-200	PLP-450	DC-400	580-750	750-1800
PLP-30	DC-32	47-61	61-200	PLP-550	DC-520	750-920	920-2000
PLP-50	DC-48	70-90	90-200	PLP-600	DC-680	840-1120	1120-2000
PLP-70	DC-60	90-117	117-300	PLP-750	DC-700	1000-1300	1300-2000
PLP-90	DC-81	121-137	167-400	PLP-800	DC-720	1080-1400	1400-2000
PLP-100	DC-98	146-189	189-400	PLP-850	DC-760	1100-1400	1400-2000
PLP-150	DC-140	210-300	300-600	PLP-1000	DC-900	1340-1750	1750-2000
PLP-200	DC-190	290-390	390-800	PLP-1200	DC-1000	1620-2100	2100-2500

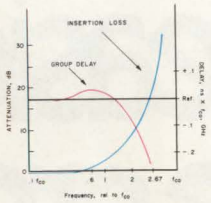
Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95. Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCLF-135	DC-135	210-300	300-600				

Price, (1-9 qty), all models: $11.45

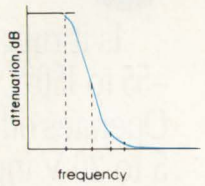
Flat Time Delay, dc to 1870MHz



Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X	VSWR Freq. Range, DC thru 0.6fco X	Group Delay Variations, ns Freq. Range, DC thru fco X	Group Delay Variations, ns Freq. Range, DC thru 2fco X	Group Delay Variations, ns Freq. Range, DC thru 2.67fco X
PBLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
PBLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
PBLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
PBLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
PBLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
PBLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

HIGH PASS

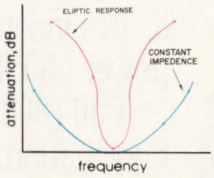


high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.	Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1	PHP-400	DC-210	210-290	395-1600	1.7:1
PHP-50	DC-20	20-26	41-200	1.5:1	PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-100	DC-40	40-55	90-400	1.8:1	PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-150	DC-70	70-95	133-600	1.8:1	PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-175	DC-70	70-105	160-800	1.5:1	PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-200	DC-90	90-116	185-800	1.6:1	PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-250	DC-100	100-150	225-1200	1.3:1	PHP-1000	DC-550	550-720	1000-2200	1.9:1
PHP-300	DC-145	145-170	290-1200	1.7:1					

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

BANDPASS



bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
PBP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
PBP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
PBP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

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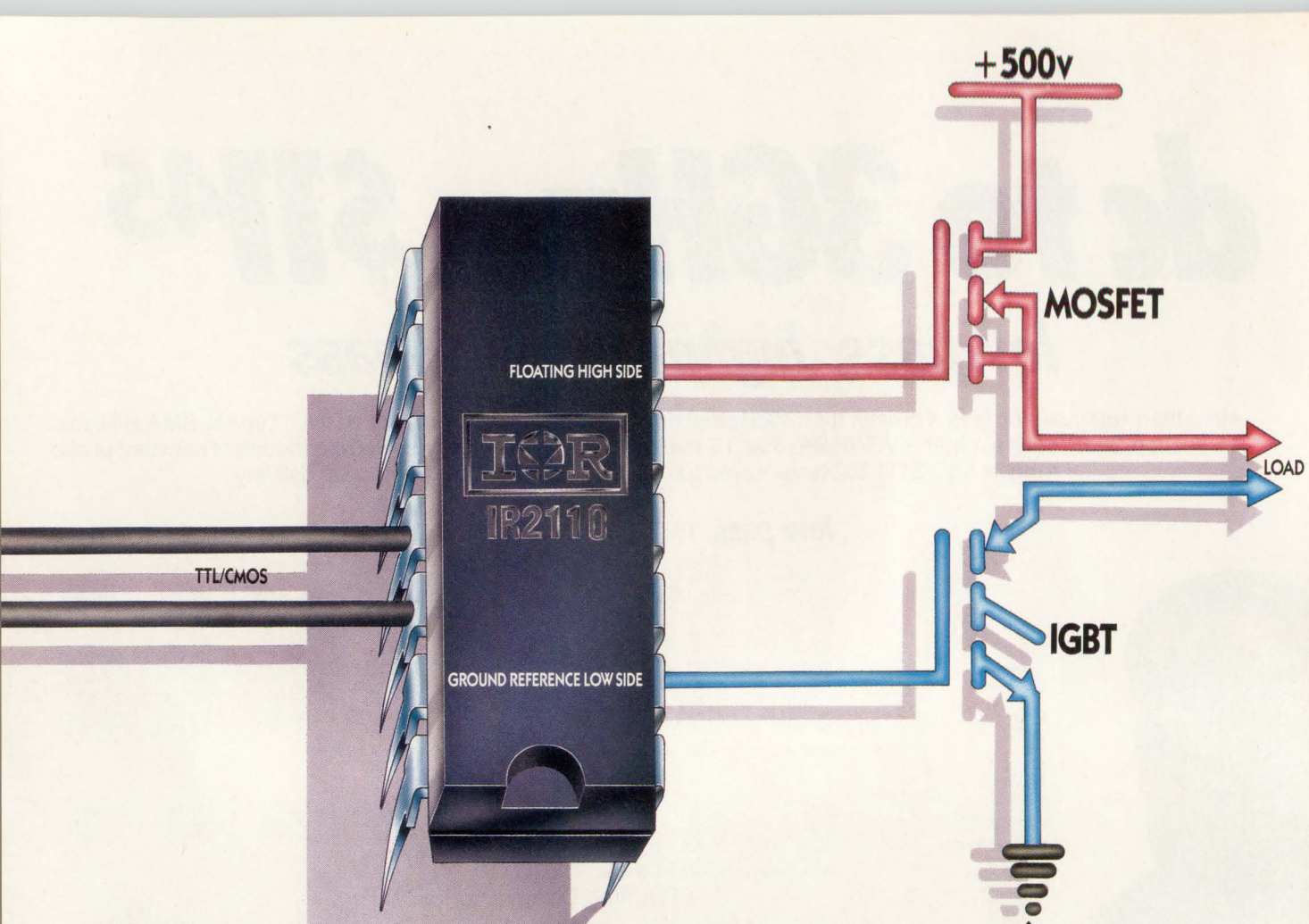

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CIRCLE 192 FOR U.S. RESPONSE CIRCLE 193 FOR RESPONSE OUTSIDE THE U.S.

SUPERCONDUCTORS IMPLEMENT LOGIC GATES

The world's first digital-logic gates using high-temperature superconductors have reportedly been built. Researchers at the Applied Technology Div. of TRW Inc., Redondo Beach, Calif., have simulated 4-ps rise times for the devices, which translates to 250 billion switching operations per second. TRW says the architecture can be used for all Boolean functions. Functions already demonstrated include AND, EXOR, EXNOR, inversion, and buffer. Each logic gate is formed by a string of dc superconducting quantum-interference devices (SQUIDs), which are thin films made from the ceramic compound yttrium-barium-copper oxide. The gates were originally operated at temperatures from 4.2 to 36K. But recently developed grain-boundary-junction technology will enable the logic gates to work at 65K. Power dissipation of each gate is about 2 nW. High-speed circuitry will dissipate a projected 100 nW, and 10-GHz operation will dissipate 1 W of power. TRW's high-temperature circuits resemble CMOS designs and are amenable to gate-array and ASIC approaches. For more information, call Susan Brough, (310) 812-5227. *ML*

POLYMERS IMPROVE ELECTRO-OPTIC DEVICES

Chemists at the Naval Weapons Center (NWC), China Lake, Calif., have developed several nonlinear optical polymers (NLOPs) that overcome the limitations of conventional nonlinear optical crystals for use in fiber optics, avionics, and photonics applications. Currently used nonlinear optical crystals (such as lithium niobate) are brittle, not easily integrated with silicon or gallium-arsenide structures, and are costly to produce. In contrast, the new NLOPs have a lower dielectric constant, as well as higher electro-optic coefficients, mechanical toughness, stability, and design and manufacturing flexibility. In addition, the new materials are compatible with silicon processing. Waveguides produced with NLOPs can be spin-coated, patterned, etched, and cladded with existing IC manufacturing processes. Other applications include high-speed fiber-optic switches and modulators, diode-laser frequency doublers, and integrated electro-optic devices, such as optical interconnects in high-speed optical computers. NWC is developing NLOPs for Langmuir-Blodgett processing, which has excellent film-thickness control. The Center is offering six classes of NLOP compositions for licensing. For more information, call Martha Harrington, (619) 939-1698/1215. *ML*

CFI SET TO RELEASE STANDARDS COMMERCIALLY

The CAD Framework Initiative Inc. (CFI), Austin, Texas, changed its organizational structure and standards-release process to closely model the product-release practices of commercial companies. Organizational changes include the addition of a Product Marketing Council to provide strategic direction to the technical committees within CFI. The Council will attempt to close the gap between CFI standards, the products being developed by EDA tool suppliers, and the needs of the EDA users and tool integrators. Also, CFI's standards-release process now has a Pilot Implementation Program step to bring EDA-tool suppliers, tool integrators, and tool users deeper into the standards-definition and delivery procedures. All participants in the Pilot Program will receive a pilot-release version of the standards, and will then help determine how well the final standards address complex tool-integration tasks. All sponsor and corporate CFI members are eligible to participate in pilot projects, which will begin this month. Details on the program are available from CFI at (512) 338-3739. *LM*

MULTIPLE-GATE FET AIMED AT NEURAL NETS

With the addition of multiple, independent gate electrodes to a single MOS transistor, the transistor can calculate the weighted sum of every input and control its "on" or "off" state based on the result of the weighted-sum calculation. Consequently, the neuron MOSFET (neuMOS) exhibits a function similar to that of a biological neuron cell, such as found in the brain. Developed by Dr. Tadahiro Ohmi and Tadashi Shibata at the department of electrical engineering of Tohoku University, Sendai, Japan, the neuMOS element could form a variable-threshold transistor, a neuron in a neural network, a single-gate digital-to-analog converter, and even "soft" logic (logic that can be configured to any of 16 logic functions just by changing the control signals). Unveiled at last month's International Electron Devices Meeting in Washington, D.C., the experimental device was fabricated with a standard double-polysilicon n-channel MOS process. The structure consists of a floating gate and multiple input gates that are capacitively coupled with the floating gate. And because the summing operation occurs in a voltage mode via the capacitive coupling effect, the device essentially consumes no power. That makes it an ideal candidate for use in high-integration ICs. *DB*

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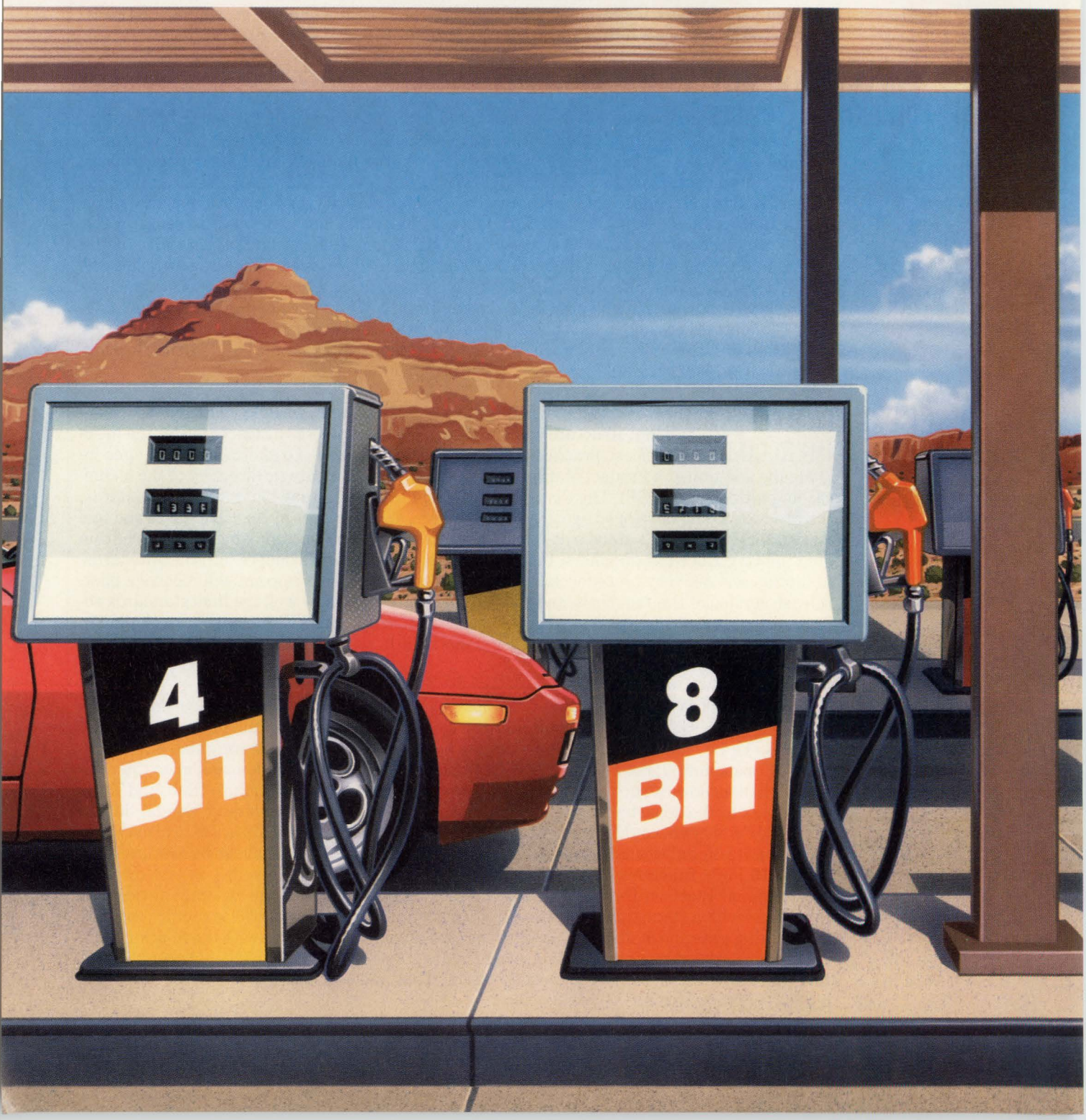

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CIRCLE 131 FOR U.S. RESPONSE

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SENSORS USE THIN FILM WITH SHAPE MEMORY

A proprietary sputtering technique developed by the TiNi Alloy Co., Oakland, Calif., deposits films of nickel-titanium alloy with shape memory onto various substrates. Films have been produced on both glass and silicon, in thicknesses ranging from 2000 Å to 50 μm. The alloy has the unique property of assuming its original shape upon application of electrical power after it's deformed by an external force. The principle behind the shape-memory effect is the temperature-dependent change in the material's crystal structure. In a pneumatic-valve application, for example, the shape-memory film is deformed by a constant air pressure to seat against a valve orifice. When electrical current is passed through the film, the generated heat transforms the membrane to its high-temperature phase, thereby lifting the film off the inlet orifice. Valve opening and closure occurs in 15 ms. Other applications under development are Schottky-junction sensors and two-state microscopic elements for optical storage. For more information, call John Busch, (415) 658-3172. *ML*

IMPROVED STATE AVERAGING AIDS POWER-SUPPLY DESIGN

Simulating switched-mode power supplies with a mathematical-behavioral approach called state averaging can increase simulation speed by as much as 1000 times over standard Spice techniques. State averaging isn't a new idea; many EDA vendors sell state-averaged models of a power supply's pulse-width-modulator chip. However, Dazix, Huntsville, Ala., is working with U.K.-based ERA Technology Ltd. to develop a unique switched-mode power-supply design aid based on the state-average technique. ERA has an implementation that differs from the existing models for three reasons: the complete circuit, not just the pulse-width-modulation controller, can be modeled with state averaging; the circuit's frequency response (Bode plot), and consequently its stability, can be analyzed; and current-mode controllers can be modeled. The ERA technology will be incorporated into the Dazix Analog Design Engineer product. Call (205) 730-2000. *LM*

DESIGN PROCESS SHRINKS SBC DEVELOPMENT TIME

System designers can create semicustom single-board computers (SBCs) in just twelve weeks using the Application Specific Automation Processor (ASAP) from Ziatech Corp., San Luis Obispo, Calif. With the help of ASAP, designers can achieve the right mix of processor, I/O, and peripheral functionality by using predesigned and tested I/O circuit modules that have a proven core-processor module. Because the boards are constructed with pretested parts, the bugs should be minimal. The ASAP approach bridges the gap between off-the-shelf products and proprietary solutions. Typical ASAP boards are designed to the STDbus standard form factor (4.5 by 6.5 in.) using the STDbus edge connector. An STD 32 backplane connector or an SBX expansion interface for daughterboard modules offers added flexibility. For more information, contact Ziatech at (805) 541-0488. *RN*

PORT EASES BUILDING REAL-TIME CONTROL JOBS

Developers working with embedded real-time applications may have an easier time of it in the wake of an agreement between Talerian Corp. and Wind River Systems. Under the pact, Talerian, Mountain View, Calif., will port its RTworks real-time development tools to the VxWorks real-time operating system and development environment from Wind River Systems, Alameda, Calif. As a result, developers will have the means to build workstation-based or embedded real-time applications that require intelligent control. They'll also be able to distribute real-time applications across multiple hosts in a client-server architecture. By including sophisticated graphics, knowledge-based systems, and interprocess communications, RTworks enables developers to build intelligent real-time monitoring and control systems for Unix and VMS workstations. VxWorks expands the RTworks realm to applications requiring a real-time operating system. *SVT*

FPGA ALLIANCE PROGRAM UPS MEMBERSHIP TO 19

Three more companies have joined Actel Corp.'s Industry Alliance Program, a program that enables companies to have technical and cooperative marketing relationships with the Sunnyvale, Calif.-based FPGA supplier. The addition of GenRad Design Automation, Isdata, and Logic Automation brings the total membership number to 19 EDA and gate-array companies. GenRad and Isdata represent the first companies from the U.K. and Germany, respectively, to join the program. The program's goal is to provide Actel customers with links to third-party tools and ASIC-migration paths. Actel supplies Alliance members with its software and technical assistance for Actel-product-support development. For more information, call Actel at (408) 739-1010. *LM*

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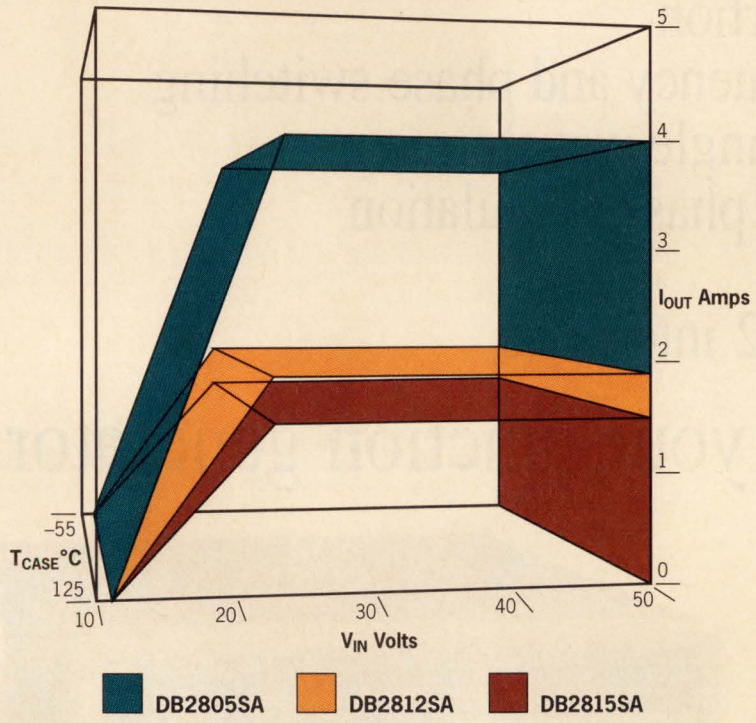

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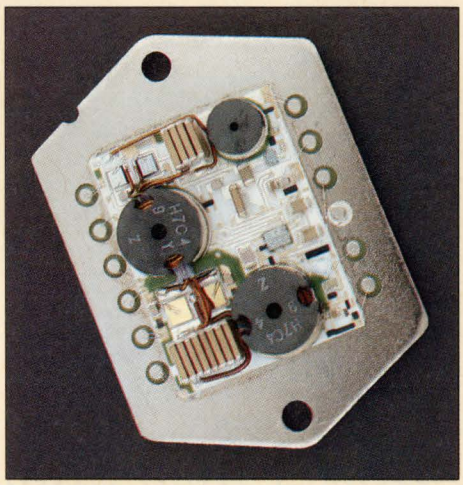

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RISC Processors, Multimegabit RAMs, And Mixed-Signal Developments Highlight ISSCC

High-performance microprocessors, dense memories, and precision analog and mixed-signal circuits will be showcased at next month's International Solid-State Circuits Conference. The conference's 80 technical papers will detail such innovations as a 1000-MIPS processor implemented with 0.3-μm features, sub-15-ns 16-Mbit SRAMs, 8-bit 650-MHz analog-to-digital converters, and a 10-Gbit/s silicon-bipolar chip set for optical communications. Other developments covered include active-matrix thin-film transistor technology, and image sensing and processing.

To achieve a throughput of 1000 MIPS, researchers at the Central Research Laboratory of Hitachi Ltd., Tokyo, Japan, integrated two superscalar processors, each with a two-level cache memory, onto a biCMOS chip by employing 0.3-μm design features—a technological first. The chip can operate at 250 MHz, with each processor executing two instructions per clock, for a total throughput of 1000 MIPS. About 1.02 million transistors are employed by the processors, each of which has a 1.2-ns 32-bit adder, a 1.3-ns eight-port register file, and a 2.8-ns translation-lookaside buffer and cache memory.

A pair of biCMOS chips—a 3-million-transistor Sparc-compatible superscalar RISC processor and a companion 2.2-million-transistor cache-controller chip—both capable of operating at 50 MHz, will be described by Sun Microsystems Inc., Mountain View, Calif., and Texas Instruments Inc., Dallas. The SuperSparc CPU chip packs 36 kbytes of first-level cache, a complete memory-management unit, and a full double-precision floating-point unit. It can execute up to three instructions per clock, yielding a throughput of up to 150 MIPS. The cache-control chip provides 264 kbits of tag RAM that supports up to 2 Mbytes of external cache memory. Two different multiprocessor-system bus interfaces and two different I/O electrical interfaces are supported by the controller.

Both a CISC and a RISC processor will be detailed in a pair of papers from Digital Equipment Corp., Hudson, Mass. The RISC device has a 64-bit architecture and runs at 200 MHz to deliver a peak throughput of 400 MIPS. The CMOS circuit includes 8-kbyte instruction and data caches, and can execute two instructions per clock to achieve its 400-MIPS peak performance. Fabricated with 0.75-μm design rules in a 3.3-V process, the CPU is a power-hungry device due to its high clock rate—power dissipation goes up to 30 W.

The CISC processor is also implemented with the same 3.3-V submicron technology. It employs a macropipelined architecture and dissipates about 18 W when running at 100 MHz. The chip's clocks-per-instruction ratio is 2.4 times better than for the company's micropipelined implementation of the same instruction set. Consequently, a performance benchmark of 50 Specmarks is attained when running at a frequency of 100 MHz.

Another high-performance CPU to be disclosed in the same session is a 289-MFLOPS supercomputer on a chip developed by Fujitsu Ltd., Atsugi, Japan. Also fabricated in CMOS, the processor operates at 70 MHz and achieves a 289-MFLOPS throughput for single-precision computations and 149 MFLOPS for double-precision operations. To move data on and off the chip quickly, designers implemented a bus that can transfer 560 Mbytes/s. To perform the computations, the processor contains six vector pipelines, four of which operate simultaneously with four-way bank-structured vector registers containing 8 kbytes each.

To support such high-performance processors, dense and fast static RAMs as well as new-architecture dynamic RAMs are being developed to fill the system designer's wish list. A pair of 16-Mbit SRAMs, one from NEC Corp., Sagamihara, Japan, and the other from Fujitsu's Kawasaki research center, achieve access times of 12 and 15 ns, respectively. Both are based on 0.4-μm design rules and CMOS processes. The NEC device is made from a quadruple-polysilicon, double-metal process with thin-film-transistor (TFT) active loads. It operates from a 3.3-V supply and dissipates just under 300 mW when running at 30 MHz. Fujitsu's chip operates from a 3-V supply, and dissipates only 60% of the power of NEC's chip—165 mW at 30 MHz.

Experimenting with 1-V process technology, Hitachi's researchers will detail the fabrication of a small 4-kbit test chip. The memory cells employ TFT loads and are fabricated with 0.4-μm design rules. When scaled to a 4-Mbit RAM, the larger chip would occupy about 75 mm^2 and draw just 0.7 μA of standby current.

Pushing biCMOS for high-speed memory, Toshiba Corp., Kawasaki, and NEC have crafted 3.3-V, 4-Mbit SRAMs that access in just 9 and 6 ns, respectively. The Toshiba memory is organized as 256 kwords by 16 bits and consumes just 430 mW when operating at 50 MHz with TTL I/O levels. NEC's part employs ECL I/O or 3.3-V TTL I/O (with TTL I/O, access time slows

ISSCC – WANT TO GO?

The International Solid State Circuits Conference will be held at the San Francisco Hilton Hotel, Feb. 19-21. For registration details and the full advance program, contact Diane Suiters at Courtesy Associates, 665 15th St. NW, Suite 300, Washington D.C. 20005; (202) 639-4255, or by fax at (202) 347-6109.

to 8 ns) and is organized as either 4 Mwords by 1 bit or 1 M by 4. It dissipates 750 mW with the ECL I/O and just 230 mW with the TTL option.

Suprisingly, there are only two DRAM papers at this year's conference venue—in past years it seemed that high-density DRAM papers dominated the spotlight. The first describes a novel combination DRAM and SRAM circuit developed by Mitsubishi Electric Corp., Itami, Japan. The IC combines 16 kbits of SRAM cache memory along with 4 Mbits of DRAM. The cache-DRAM can transfer data at 100 MHz over its cache port, and includes a copy-back scheme that keeps the copy-back time equal to the DRAM access time, and a flexible DRAM-to-cache mapping scheme.

The other DRAM paper is from NEC and details a 64-Mbit device that can be accessed in just 30 ns. The chip includes a built-in test-and-repair capability to reduce test cost and increase reliability. Additional memory papers include a 16-Mbit flash device from NEC and a 4-Mbit flash EEPROM developed by Toshiba. Both can be read or programmed from a lone 5-V supply. NEC's chip also has a selective sector-erase capability that allows any 512-word sector to be erased and reprogrammed, minimizing the memory update time.

Data conversion is also a hot topic at the upcoming conference, with over a half-dozen papers focused on ADCs. The fastest of the lot is an 8-bit, 650-MHz folded-architecture ADC developed at the Philips Research Labs, Eindhoven, the Netherlands. Implemented in a silicon bipolar process, the chip takes advantage of folding interpolation and comparator error averaging in the analog domain to achieve 7.8 effective bits at a 150-MHz input and a 650-MHz conversion rate. The chip dissipates a mere 850 mW from a –4.5-V supply.

Slowing the conversion rate to 50 MHz, a second bipolar device from Philips ups the resolution to 10 bits by employing a fully-differential pipelined architecture. An on-chip sample-and-hold amplifier and digital error correction give the chip 66 dB of signal-to-(noise + distortion) ratio at the 50-MHz conversion rate. The chip consumes about 750 mW from a –5-V supply.

A trio of 12-bit devices from Hewlett-Packard Co., Palo Alto, Calif.; Stanford University, Stanford, Calif.; and a joint development by Analog Devices Inc., Wilmington, Del., and the University of Illinois at Urbana will also be described. The H-P chip runs at 20 MHz and employs a 10-stage ripple-through architecture with on-chip track-and-hold and digital error correction. Able to maintain the signal-to-noise ratio over the full Nyquist bandwidth, the converter can limit the harmonic distortion to –72 dB with some external adjustment. This chip, though, is rather power-hungry, consuming 3.5 W when powered by +5- and -5.2-V power supplies.

The converter from Stanford runs at only 5 MHz but employs a fully-differential two-step architecture with analog and digital error correction. The third 12-bit converter, a CMOS device developed by Analog Devices, employs an all-digital linearity improvement scheme to reduce feedthrough, offset, and digital-to-analog-converter errors, and to simultaneously improve the total harmonic distortion from –64 to –77 dB. Another paper by Analog Devices will describe a 17-bit algorithmic high-resolution converter implemented in biCMOS. The chip exhibits 15 bits of resolution with a 500-μs conversion time. On-chip auto-gain-ranging with offset cancellation lets the chip achieve the 17-bit dynamic range with only 20 μV of dc offset voltage.

Circuits for communications applications are scattered throughout various sessions at the upcoming conference. For instance, a frequency divider that can operate at up to 18.26 GHz will be described by researchers at Varian Corp.'s Research Center, Palo Alto, Calif. Implemented in gallium-arsenide two-dimensional electron-gas structures, the divide-by-N prescaler can be extended to eventually allow input frequencies up to 80 GHz. The 18.26-GHz input speed, though, is beaten by a 28-GHz silicon-bipolar dynamic frequency divider that NEC will describe in another session. The 1.5-mm^2 NEC circuit includes spiral inductive loads, polysilicon resistors, and aluminum-silicon-dioxide-aluminum capacitors and can divide the input signal by a 1:16 ratio.

In the same session as its divider paper, NEC will deliver details of a 10-GHz chip set for coherent optical communication systems. The amplifier chip provides 20 dB of gain when running at 10 GHz, while the mixer chip keeps the conversion loss to just 10 dB.

Researchers from the University of California at Los Angeles will detail simple NMOS circuits that can operate at 1.8 Gbits/s with jitter of just 13 ps rms. Part of the circuit includes a phase-locked loop (PLL) that extracts the clock from a 2^{23}-bit pseudorandom sequence that comes in at 1.8 Gbits/s. A 6-GHz PLL was also developed by the University of California with support from TRW Inc., Redondo Beach, Calif. The PLL employs AlGaAs/GaAs heterojunction bipolar devices and includes a frequency quadrupling voltage-controlled oscillator, a full balanced mixer, a lag-lead loop filter, and an output buffer.

In other sessions, image sensing and processing will be spotlighted with several papers detailing 2-Mpixel imaging chips targeted at the high-definition TV market. Sony Corp., Atsugi, Japan, Toshiba, and NEC will describe image sensors in 1- and 2/3-in. formats. The Toshiba and NEC CCD sensors are set up on the 1-in. format. Overlaid with an amorphous silicon photo-conversion layer, the Toshiba chip achieves a dynamic range of 108 dB. The NEC device is a little more limited, with a 75-dB dynamic range. Sony squeezes the same number of pixels into a 2/3-in. format chip, employing a lenticular microlens array and a scaled output structure to achieve a 70-dB dynamic range.

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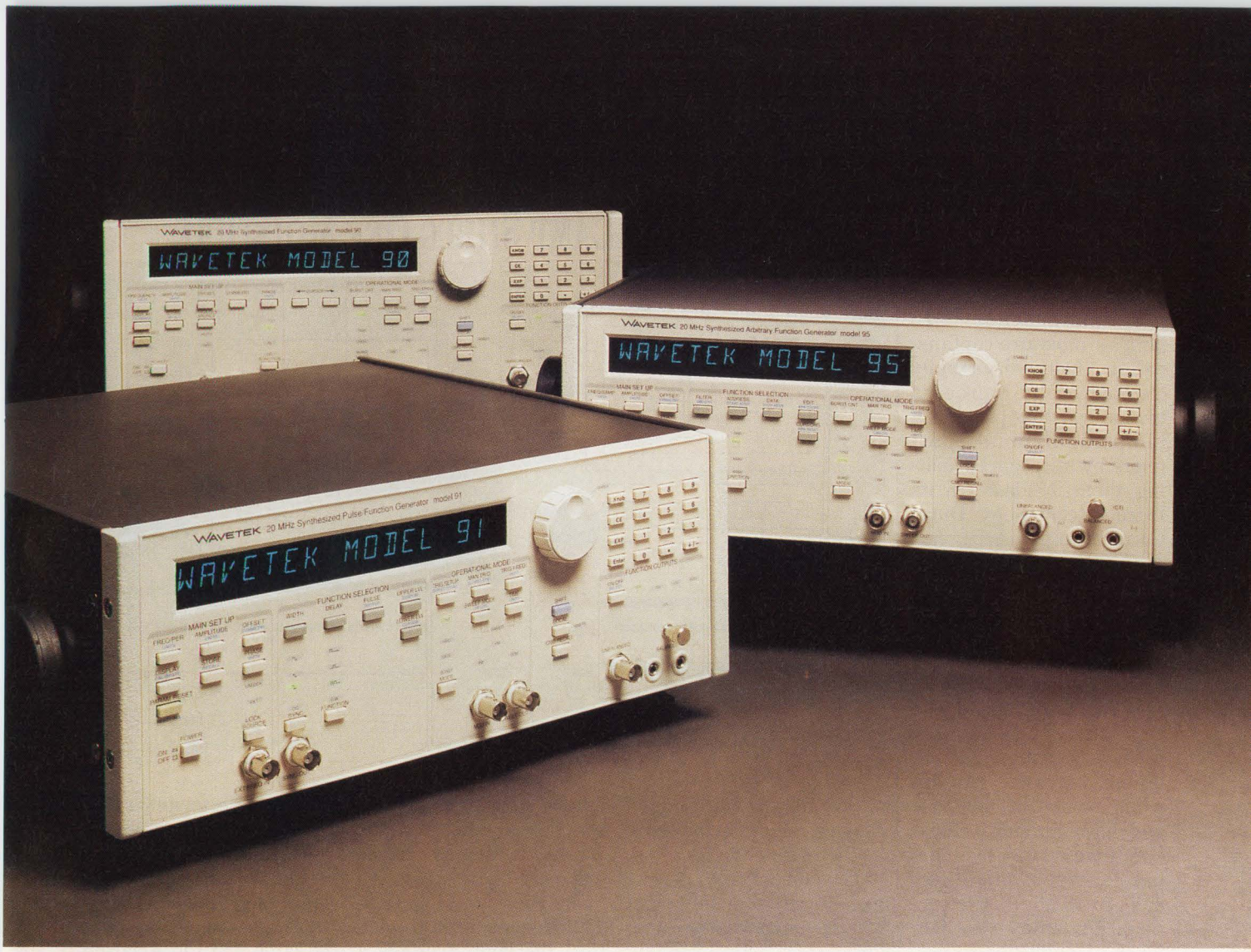

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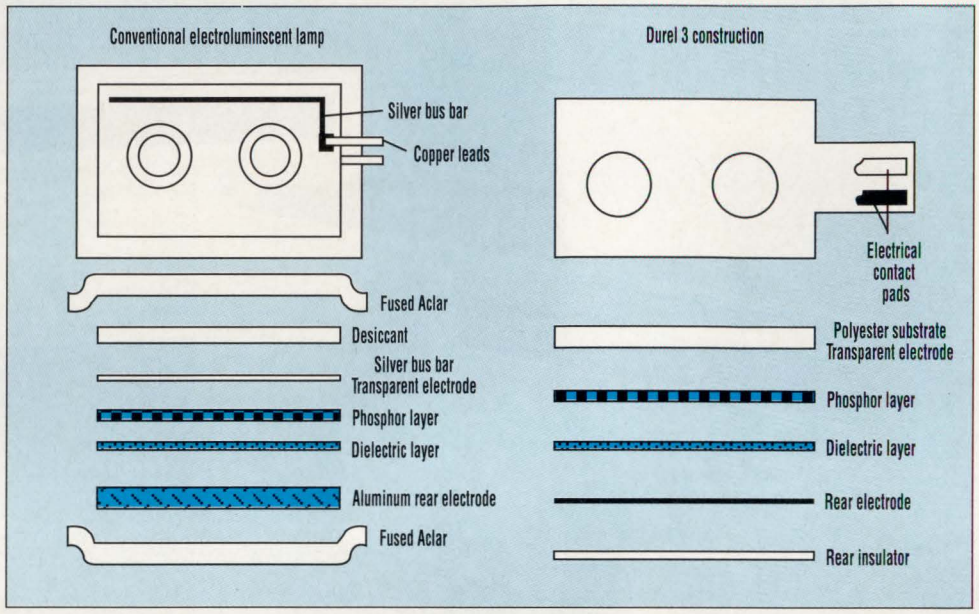
SEALED PHOSPHORS LET THIN EL LAMP SHRUG OFF MOISTURE

The most common failure mode of electroluminescent (EL) lamps—moisture contamination—has been virtually eliminated by a process technology that protects a lamp's individual phosphors by microencapsulating them in glass. In its Durel 3 technology, Durel Corp., Tempe, Ariz., has produced extremely thin, flexible EL lamps that last 300% longer in intensely accelerated environmental testing than conventional EL lamps.

If left unprotected, the zinc sulfide phosphor used in most conventional EL lamps degrades rapidly when exposed to moisture and high humidity. Most lamps would dim to an unusable level of brightness in 24 to 48 hours. Conventional EL lamps use a thin layer of polyester to provide a moisture barrier for the phosphor layer. In addition, a somewhat better encapsulation material, polychlorotrifluoroethlyene (PCTFE), or Aclar, is used to keep moisture away from the phosphor layer. In most cases, a desiccant layer is also added.

Although using polyester and PCTFE encapsulation provides some moisture protection, it's only a partial solution. PCTFE has the lowest moisture-vapor permeability of any polymer, but it still lets some moisture through and will be doomed to eventual failure in a high-humidity application. In addition, the plastic-packaged EL lamps can range up to 50 mils in thickness, which can limit their flexibility and hence their range of applicability. Moreover, all such lamps require edge-sealing, which further limits their scope of use.



The Durel 3 technology, in contrast, eliminates the plastic encapsulation and desiccant layer by microencapsulating each individual particle of zinc sulfide in glass *(see the figure)*. The resulting 8-to-10-mil-thick lamp is 50 to 75% thinner than conventional EL lamps. The simpler, less costly construction also results in an unlit border of just 25 to 50 mils. Conventional lamps have an unlit border of 100 mils or more.

In addition, the Durel 3 lamp has been shown in accelerated environmental testing to hold up an average of four times as long. The company hopes that its lamps' durability in extreme humidity will break open new application areas, such as marine applications. There, EL lamps could backlight keypads and displays on communication and navigation equipment. One automotive application, an ambulance control panel, shows the lamps' ability to be formed in unique shapes and die cut with holes. The ambulance-panel lamp has 130 holes cut into it. In addition, the lamp overlays a membrane switch and backlights the elastomer keypad that sits on top of it. As the keypad is pressed to actuate the switches, the lamp is flexible enough to withstand the actuation.

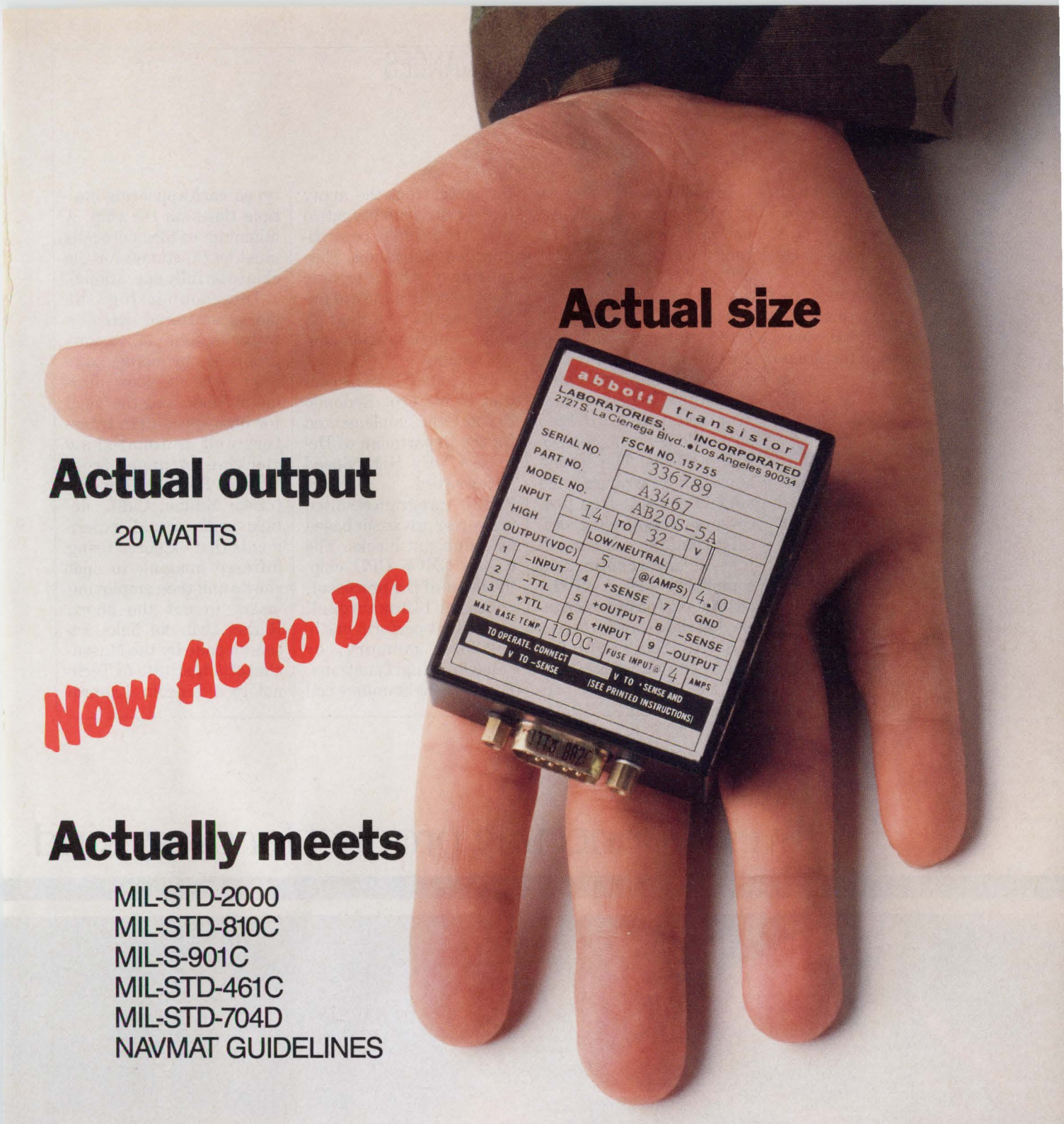
The cost of the Durel 3 lamp falls between that of the polyester-encapsulated lamp and the Aclar-encapsulated type. Call Doug Olson at (602) 731-6204 for information.

DAVID MALINIAK

WAFERSCALE INTEGRATION CONFERENCE ADDRESSES A WIDE RANGE OF TOPICS

As system performance requirements outstrip the ability to create single-chip solutions, designers look to waferscale integration and complex multichip modules to solve demanding signal- and data-processing needs. As a result, reconfigurability, site-to-site interconnections (including clock distribution), and testing are key issues that must be dealt with to ensure that reliable, high-performance systems can actually be built. Such topics, along with applications of waferscale integration to neural networks (NNs), image and video processing, phased-array radar, and signal processing, will be focal points at the upcoming IEEE International Conference on Wafer Scale Integration.

Because of yield issues and the random defects that appear on wafers during the manufacturing



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stage, obtaining enough good blocks and interconnecting them to form a functional system is essential. Over a half-dozen papers at the conference specifically address this topic. Evaluating optimal spare allocation for defect-tolerant VLSI, a presentation by the University of Illinois at Urbana-Champaign analyzes the best ratio of spare blocks by taking into account process complexity and other factors based on block size. Focusing on memory redundancy, an analysis employing a center-satellite model is discussed by the University of Massachusetts at Amherst to examine yield optimization for redundant multimegabit RAMs.

In addition, the University of Michigan at Ann Arbor will examine self-reconfiguration of processor arrays by applying two NN learning approaches. The first employs an NN that's interconnected and programmed to readily execute a maximum matching algorithm. That algorithm helps assign fault-free spare elements to replace faulty blocks. The second approach rearranges the surviving fault-free processors to restore the logical structure, and can adjust its interconnection complexity based on the desired performance criteria that the user sets up.

Simulated examples show that the NN approaches offer better performance from the array (higher survivability rates) than traditional reconfiguration algorithms. Furthermore, the intrinsic fault-tolerant nature of the NNs results in a degradable reconfiguration-control scheme.

The SuperChip project that TRW Corp., Redondo Beach, Calif., implemented for the Department of Defense's Very High Speed Integrated Circuit (VHSIC) program resulted in a vector processor based on redundant blocks. The 0.5-μm CMOS CPU chip, the heart of the processor, contains 142 macrocell blocks that perform mathematical, memory, or housekeeping functions. There are eight unique cell types, each appearing multiple times on the chip. A minimum of 61 macrocells must be functional for the chip to be fully operational.

Interconnecting the blocks scattered across a wafer results in various problems, including power-line shorts, poor intermetal links, and the need for high-speed data transfers and minimal-skew clocking. A paper from Hughes Research Laboratories, Malibu, Calif., details some actual experiments that explored using infrared imaging to spot shorts and then employing lasers to cut the short. Rather than cut links, research done by the Massachusetts Institute of Technology's Lincoln Labora-

WANT TO GO?

The IEEE International Conference on Wafer Scale Integration will be held at the Fairmont Hotel in San Francisco, Calif., Jan. 22-24. For copies of the advance program and registration, contact Michael W. Yung at Hughes Research Laboratories, RL69, 3011 Malibu Canyon Rd., Malibu, CA 90265; (213) 317-5657, or by fax at (213) 317-5484.

tory, under the sponsorship of the United States Department of the Air Force, describes using a laser to weld the cross-point of two links to form connections while maintaining insulation integrity between links.

The long connection paths on a wafer are sources of large amounts of clock and signal skew. To that end, researchers from the University of South Florida, Tampa, will present an analysis of skew and clocking issues across wafers. Sample clock distribution networks, fabricated on 4-in. wafers, were evaluated for skew and other ac-performance changes versus power dissipation, layout area, and harvesting yield. Employing optical interconnects even across a wafer can also minimize skew. However, it's a much more complex solution due to the task of integrating the optical transmitters and receivers on the wafer. One interesting optical-bus interconnection scheme will be described by researchers at the University of Texas at Austin.

When implementing wafer-level integration, power consumption levels can add up very quickly, to the point where single wafers can dissipate 100 W or more. Consequently, careful attention to circuit details can have large payoffs. For instance, another paper by the University of Texas looks at ways to reduce the dynamic power consumption by examining the optimization of adders. Six different types of CMOS adders are examined for area, power, and other factors.

In the case of CMOS adders, the adder that requires the fewest logic transitions to perform its operation would be the most desirable. If speed were the key consideration, then a carry-lookahead adder would be the best choice for 16-bit operations, while either a carry-select or the carry-lookahead adder would be best for 32- or 64-bit applications. If gate count and the speed were equally important, then a carry-skip adder would be the best choice.

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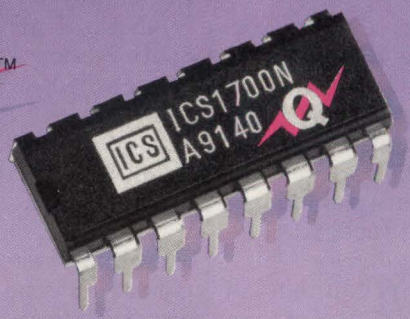

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PROCESS ADVANCEMENTS FUEL IC DEVELOPMENTS

IMPROVEMENTS IN LITHOGRAPHY, ETCHING, AND DEPOSITION HOLD THE KEY.

BY DAVE BURSKY

Each new year, designers have come to expect more circuitry to be crammed onto IC chips than the year before. Thus far, the doubling of chip integration every two years or so has led to commercial multimillion-transistor microprocessors, 16-Mbit memories, and logic chips with several-hundred-thousand gates. Key dimensions on production chips are already scaled below 1 μm, with volume production of chips boasting 0.7-μm minimum features available from multiple suppliers.

To stay competitive and bring even-smaller features into the production environment, IC manufacturers around the world pour billions of dollars into all aspects of chip production. Research into lithography, etching, and deposition is providing answers to drawing finer lines; cutting smaller holes for contacts or gaps between lines; or depositing metal or dielectric materials for interconnections, isolation, or capacitors.

Additional research into device and circuit structures will simultaneously yield new transistor structures and circuits that allow denser and faster chips to be fabricated. Transistors in the 0.5-μm range will allow gates to offer sub-100-ps delays, 16-kbit RAMs to access in 6 ns, and 16-bit multipliers to deliver product terms in just 7.5 ns.

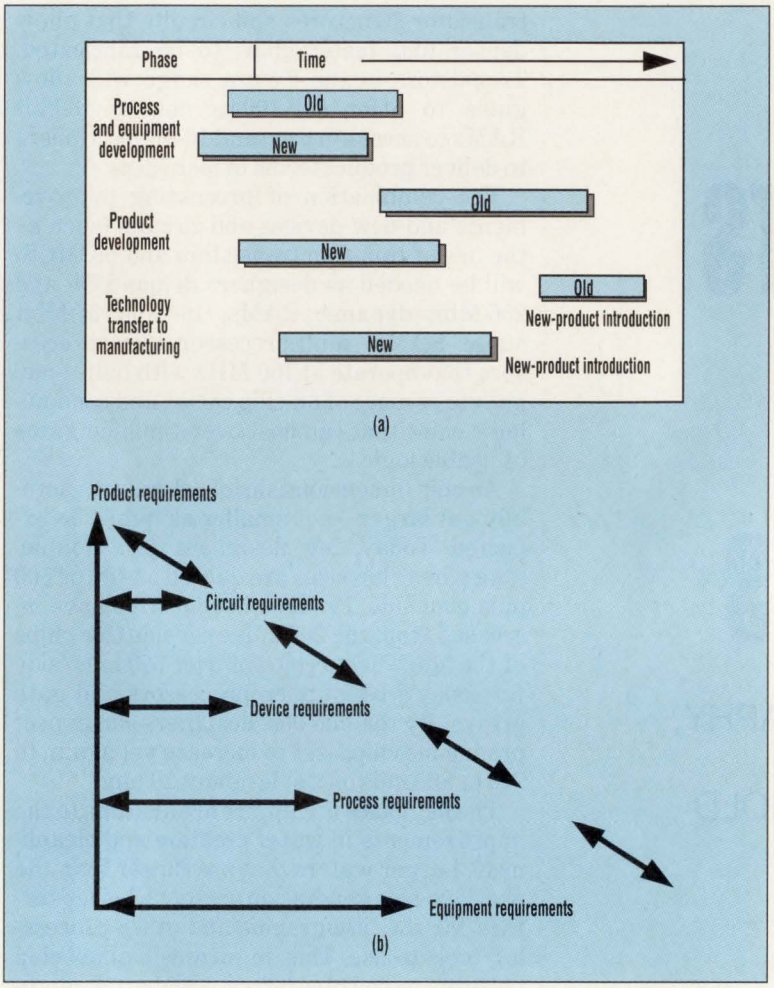
The combination of processing improvements and new devices and circuits (such as the use of thin-film transistors and biCMOS) will be needed as designers demand 64- and 256-Mbit dynamic RAMs, 16- and 64-Mbit static RAMs, multiprocessor microprocessors that operate at 100 MHz with half-a-megabyte or more of on-chip cache, and random-logic chips that can host over 1 million gates of usable logic.

As chip dimensions shrink, chip areas actually get larger—not smaller as might be expected. Today, few designers do a double-take when chip sizes are quoted as 400 or 500 mils on a side. Producible chip sizes have increased from the 200 mils on a side (for chips of the late '70s) to chips of over 600 mils/side for today's latest microprocessors and gate arrays. By the mid-90s, designers can expect producible chip sizes to increase yet again, to 700 or 800 mils on a side (about 20 mm).

The increases in chip size are also due to the improvements in wafer creation and cleanliness. Larger wafers that are flatter than the previous-size generation present a better surface for the lithographic and other processing tools to use. This, in turn, will allow chip patterns to be transferred with better reproduction quality. Wafer sizes have increased from about 3 in. (75 mm) in diameter in the late '70s to today's 8-in.-diameter (200-mm) disks. Several companies have already adopted the 8-in. wafers, and many others are slowly preparing to convert their production lines to the larger wafers. These large wafers can be manufactured with flatness variations of less than 0.6 μm—about the same resolution of the lithographic tool (the stepper) itself.

Better filtering of the air and of lithographic resists to remove particulates also goes a long way in reducing defects that could impact yield. Most fabrication areas today are of class 10 or better quality—no more than 10 1-μm-diameter (or larger) particles per cubic foot of air. On the other hand, the latest fabs—and the ones on future drawing boards—are designed for class-1 operation (only one 1-μm or larger particle per cubic foot of air) or better. In contrast, fabs in the '70s were typically class 1000. In the early '80s, class 100 sufficed for most processing.

To achieve those low levels of particulates, facility engineers have paid a lot of attention to details—from the human factors to the



1. To meet the needs of system designers, large semiconductor manufacturers like Motorola typically have three stages of process development occurring simultaneously—one to develop the processes and manufacturing equipment needed, one for ongoing product development, and the third involving the transfer from research to manufacturing (a). The multiple facets required to define a chip and all aspects of design and production must interact with each other to ensure that all pieces of the puzzle couple tightly together (b).

particulates generated by the fabrication equipment. This meticulousness makes the class-1 clean room possible today and will perhaps lead to sub-class-1 rooms in the mid '90s. Self-cleaning tools, precision robotic controls for wafer movement and handling, and air showers for personnel, are just a few of the many improvements to reduce particulates.

Device and circuit structures are also evolving. Over the past decade, CMOS technology usurped more than 70% of the market that bipolar logic once enjoyed. Advanced CMOS, merged bipolar and CMOS circuits, high-performance bipolar ECL chips, and even some gallium-arsenide circuits all offer designers better densities, faster operating speeds, and lower power/function than ever before. All four circuit approaches vie for the designer's attention.

The most advanced chips unveiled at major industry conferences, such as the International Electron Devices Meeting and the International Solid-State Circuits Conference, often foretell production technology by about two to five years. DRAMs have often been used as proving grounds for almost all aspects of manufacturing technology because their predictable growth allows designers to readily extrapolate most aspects required to implement the next generation or two of devices *(Table 1)*. The increase in DRAM capacity—and thus the various lithographic features to make the chips practical—can readily be extrapolated due to the consistent quadrupling of chip density.

Muddy Definitions

However, aside from the memory-only chips, the clear categorization between memory and logic chips has become muddied. Today's microprocessors contain as much memory on them as did the previous generation of stand-alone SRAM chip, while "smarter" memories now include considerable logic on the chip to provide features such as cache control, error checking and correction, counters for self refresh, or specialty circuits for video applications. The wide array of nonvolatile memory capabilities—UV EPROM, flash EPROM, EEPROM, and flash EEPROM—can also be mixed with the logic or other storage technologies giving designers a wealth of resources.

To make such a cornucopia of circuits available, most large semiconductor suppliers typically have three or four "generations" of processes in development at one time *(Fig. 1a)*. For example, at Motorola Inc., Austin, Tex., there are many overlapped processes and pieces of the development cycle transpiring concurrently. In fact, there are many interlinking phases of development, from the product-definition stage through the specification of the production equipment and processes *(Fig. 1b)*. No product is really a stand-alone development; each depends heavily on many interrelated research activities.

In addition to a process that runs on their most advanced production line, companies

TABLE 1: DRAM LITHOGRAPHIC REQUIREMENTS

Storage capacity (bits)	First year in production	Minimum feature (μm)	Overlay accuracy (μm)	Chip area (μm^2)
256 k	1984	1.7	0.7	35
1 M	1987	1.0	0.5	50
4 M	1990	0.7	0.35	70
16 M	1992/3	0.5	0.25	100
64 M	1996	0.35	0.18	140
256 M	2000	0.25	0.13	200
1 G	?	0.18	0.09	280

might typically have a prototype line running the next process to be qualified for full production, and behind that a process they expect to be the next pilot process, and so forth. This is typical of today's processes. Mass production this year centers on chips with minimum features of 0.7 to 0.8 μm. Chips with 0.5-μm features are already being fabricated on some pilot production lines. Devices with 0.35-μm features are readily producible in laboratory prototyping facilities. And research is underway to produce 0.25-μm and smaller features.

To minimize the number of new processes put in place at a facility and the number of pieces of new equipment needed to facilitate a fabrication line, most companies try to modularize the process flow. By doing so, new processes can take advantage of existing process modules and just add the necessary new modules that complete the new process. At Texas Instruments Inc., Dallas, the procedure to merge new steps into existing flows is referred to as "harmonization," explains Dr. Pallub Chatterjee, a vice president at TI. By exploiting existing hardware, some up-front engineering costs can be reduced and the ramp-up time can be minimized.

Though many aspects of chip manufacturing are interrelated, the three key areas are lithography, etching, and deposition, which are all closely linked. The step-and-repeat lithography systems most popular with today's advanced mass-production facilities are referred to a g- and i-line steppers after the light wavelength that shines through the lens to expose the resists. Systems using i-line steppers were expected to run out of performance below 0.5 μm, due to the long 365-nm wavelength of the mercury-arc light source.

With optical steppers, the field of exposure ranges from about 12-14 mm on a side for 10:1 reduction lenses, 17.5 to 20 mm per side for 5:1 systems, and still larger for 1:1 systems. However, as the size of chips increases beyond those limits, the steppers must be able to "stitch" multiple fields together to form the larger patterns as chip dimensions exceed 600 or 700 mils on a side. Once field stitching is mastered, the field-size limit will no longer restrain chip size.

TABLE 2: MOSFET SCALING TRENDS

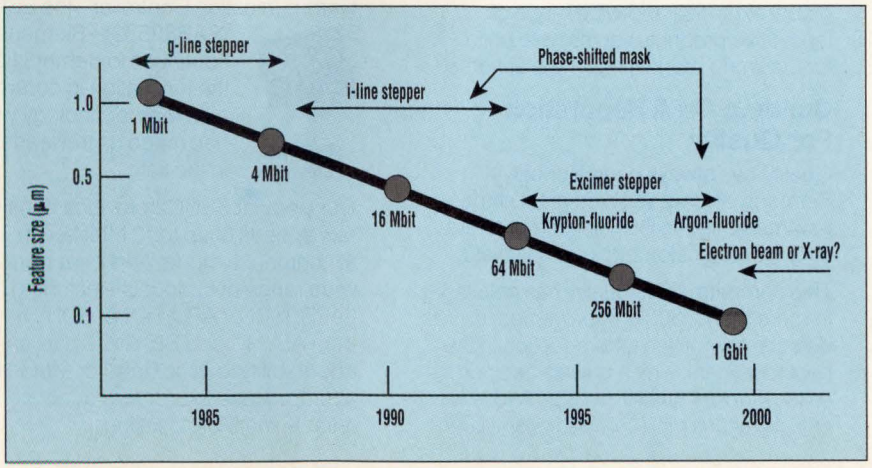
	1993-1994	1996-1997	1999-2000
Line widths	0.5 μm	0.35 μm	0.25 μm
Power supply	3.3 V	3.3 V	2.0-2.5 V
Gate oxide thickenss	11 nm	9 nm	6-7 nm
Gate length (n-channel/p-channel)	0.5/0.6 μm	0.35/0.35 μm	0.25/0.25 μm
Switching speed (fan-out = 1)	95 ps	68 ps	45 ps
Drain structure			
NMOS	FOLD*	Graded diffused drain	Conventional
PMOS	Conventional	Lightly doped drain	Conventional
Gate structure	n^+ polysilicon	n^+ polysilicon NMOS p^+ polysilicon PMOS	n^+ polysiicon NMOS p^+ polysilicon PMOS

*FOLD: fully overlapped lightly doped drain
Source: Toshiba

Improvements in lenses, overlay registration between mask layers, and the development of phase-shift mask techniques, are giving the optical stepper a new lease on life down to feature sizes of 0.4 μm and perhaps smaller *(Fig. 2)*. The phase-shift mask changes the phase of the light passing through adjacent features on the mask by 180°. That phase change causes edge diffraction to be canceled, rather than reinforced, by the diffraction pattern of the neighboring feature. With no cancellation, edge diffraction would limit resolution. The result of the phase shift is an intensity profile that has a pronounced dip between features, which suggests that each feature will be clearly resolved.

To do the phase shifting, the special masks must change the length of the optical path of the beam to be shifted. To do that, the thickness of the mask must be altered in the regions where the phase-shift must be done. The thickness of the phase-shifting region is different for different wavelengths of the light that hits the mask and that thickness must be precisely controlled during mask manufacturing.

Due to the complexity of manufac-



2. The i-line stepper is currently the workhorse of the semiconductor industry. Through the application of phase-shift masking, i-line systems can be extended into the sub-0.5-μm range. Such small features were once thought to be the domain of excimer-laser, electron-beam, and X-ray lithography systems. Phase shifting gives the i-line steppers an extension of several years to their usable life, pushing out the day when manufacturers will have to radically change their lithography systems. (Source: Cymer Laser Technologies).

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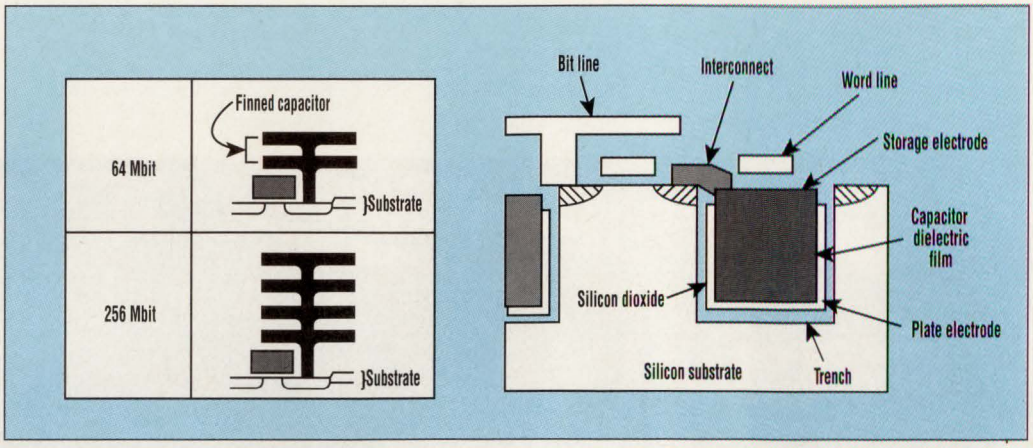
turing the phase-shift masks, and thus their high cost—more than twice that of a standard mask, the use of such masks is now limited to just one or two key layers on highly regular mask patterns. As the masks become easier to create, costs will come down and phase-shift masks will probably become a standard part of I-line lithography for minimum feature dimensions in the 0.35-to-0.5-μm range.



3. Two memory cell types will be used in forthcoming 16-, 64-, and 256-Mbit dynamic RAMs. One consists of the trench-capacitor storage cell that etches a high-aspect-ratio trench into the substrate to form the capacitor (left). Another involves building the storage cell above the substrate to form finned structures. These structures can use three or four layers of polysilicon to create a capacitor (right).

The use of deep-ultraviolet-light wavelengths will soon be possible, too, thanks to the development of excimer-laser light sources, explains Dr. Uday Sengupta, a vice president at Cymer Laser Technologies Inc., San Diego, Calif. Such sources, based on krypton-fluoride or argon-fluoride gases, provide light with wavelengths of 248 or 193 nm, respectively. Those shorter wavelengths, he continues, improve the optical resolution, allowing optical systems to create features approaching 0.2 μm.

Such small features were once only thought possible with electron-beam direct-write lithography or projection X-ray systems. The one mitigating factor for deep UV is the small depth-of-focus—about 0.5 μm. That short distance will force the chip fabricators to add extra processing steps to planarize the surface of the wafer, so that the mask images can be properly transferred.

Resist technology will also play a role in extending the usable life of optical lithography. For instance, research at Siemens AG in its Germany offices, has led to a two-layer resist scheme that can achieve dimensions as small as 0.3 to 0.25 μm. By employing two layers, only a thin, uniform film need be exposed, reducing the stepper's depth-of-focus problem.

The much thicker underlying film ensures identical exposure. To enhance the top layer's resistance to anisotropic dry etching, the film is subjected to a simple chemical after-treatment. It produces a chemical expansion of the resist lines (CARL), which allows vias as small as 0.15 μm and similar-width isolated multi-micron-deep etch troughs to be created. To produce such small dimensions, the lithography system must have an optical resolution of 0.4 μm (krypton fluoride excimer lasers). The CARL-resist scheme can also be restructured for even finer line features when argon fluoride excimer-laser steppers are available.

By extending the useful life of the optical stepper with phase-shift masks or excimer lasers, other technologies now in the wings—projection X-ray, and direct-write E-beam or laser lithography—will stay in the wings. Because these newer technologies represent a significant departure from existing tools, most firms are reluctant to use relatively unproven tools on production lines.

Direct-write E-beam and laser systems are in use for mask making, with E-beam systems popular for the creation of 1:1 reticles (masks) used in optical and X-ray step-and-repeat systems. In a few cases, companies that manufacture small-lot custom chips also use E-beam systems for direct pattern writing on wafer surfaces, thus eliminating the need to create masks altogether.

TABLE 3: BIPOLAR-PROCESS TRENDS

Process	P101	P111	P201	P231
Minimum feature size, μm (critical dimension)	1.4	1.2	1.2	0.8
Metal pitch, μm (layers 1/2/3)	4/4	4/4/8	2.8/2.8/2.8	2/2/2
Average logic density, equivalent gates/mm^2	350	500	1000	2000
Average memory density, bits/mm^2	350	500	1000	2000
Maximum number of utilized gates, equivalent gates	35,000	95,000	200,000	400,000
Worst-case equivalent gate delay, ps	330	280	160	120
Gate power consumption, μW	380	380	380	380
Production status	Now	Now	1st quarter 1992	2nd quarter 1993

Source: Bipolar Integrated Technology

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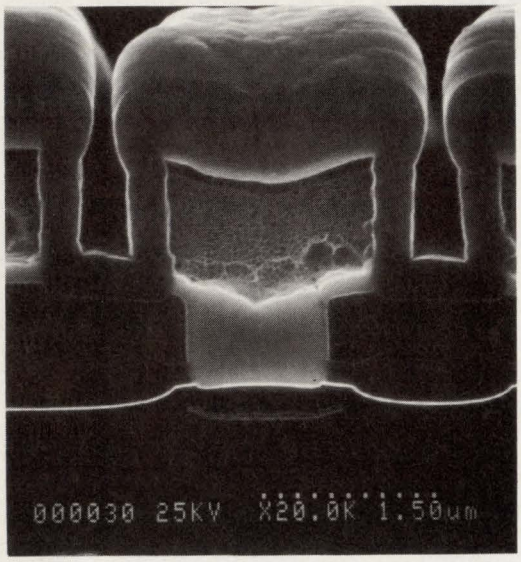

4. Tungsten plugs, such as these deposited by Integrated Device Technology, are used to fill the via holes, planarizing the dielectric surface between the first and second levels of metal, as well as between the second and third levels of metal. Planarization eliminates the step-coverage problem that plagued previous circuits employing sputtered aluminum interconnection layers.

operations along with pattern lithography for subsequent layers. Dry-etch systems employing plasma ion sources and enhanced with magnetic or electron-cyclotron resonance are the industry workhorses. These systems create the vertical etch profiles needed for the fine features and trenches demanded by the circuit designers. As for deposition, ion implantation, epitaxial silicon and gallium-arsenide growth, and various forms of chemical-vapor deposition (CVD) for oxides and metal layers, are all being put to work to build the highest-density chips.

As with lithography, the time needed to complete any process step is also a critical issue. In lithography, for example, the sensitivity of the resist (the more sensitive the resist, the shorter the exposure time), the exposure time per site, and the time needed to move from site to site, are key aspects affecting wafer throughput. Brighter light sources, more sensitive resists, and faster step-and-repeat algorithms and mechanisms are all being developed to make the expensive steppers more productive. Similarly, with etching and deposition systems, throughput is a key aspect that's always under the microscope.

Of all ICs manufactured, DRAMs present the greatest challenge to pushing the limits of process technologies, due to their ever-increasing need for higher storage capacities. Here, memory designers have three types of cells to choose from. One choice is to use lateral cells. These are the simplest to manufacture, but they also occupy the largest chip area. Another choice is to employ smaller-area trench cells that go down into the silicon. These, however, require tight etching control and high etch selectivity. A third choice is to go with similarly-sized "finned" or cylindrical storage cells by depositing three or four layers of polysilicon and oxide dielectrics above the wafer surface. The latter two exploit the third dimension by digging into or building on top of the substrate to implement the storage cells *(Fig. 3)*.

For some memory manufacturers, deep trenches (typically 4 to 8 μm) are essential to form the capacitor storage cells used in the DRAMs. In other applications, shallower trenches are used instead of oxide-isolation schemes to isolate adjacent active devices. The creation of the vertical trenches in the silicon saves lateral chip area and allows designers to minimize chip area because memory cells can be made smaller and adjacent transistors located closer together.

To etch the trenches, plasma systems are constantly upgraded to create extremely steep etch profiles, so that trenches with depth-to-width ratios of 5:1, 10:1, and even 20:1 can be repeatedly formed in the wafer. High selectivity, accurate end-point detection, and etch speed are the keys to etching the trench without etching the rest of the wafer surface (thus achieving the close-to-vertical sidewalls of the trench).

Trench cleaning is also critical because filaments from the silicon or residual contaminants can cause structural discontinuities that degrade the storage capability of trench capacitors. A secondary light-etch step can be added to the process flow to clean up some of these potential problems.

In a typical scenario, openings in the exposed mask layer would typically form the pattern of where the trenches must be etched. When etching begins, the exposed silicon is removed by the plasma. However, the resist or silicon-dioxide layers in the protected regions are also etched away, but at a much slower rate because the plasma's effects (its selectivity) are optimized in this step to remove silicon, not silicon dioxide.

The power levels required to perform operations such as etching or ion implantation in reasonable time periods cause some other problems that processing groups have to deal with—surface damage to the uppermost layers of the silicon that contain the very thin junctions formed by ion implants and diffusions. Subsequent processing steps that thermally anneal the surface can repair damage to the atomic lattice structure of the silicon. However, much care must be taken in the annealing process because the shallow junctions are especially sensitive to high temperatures—heat could cause the ions to shift around and destroy or deform the junctions.

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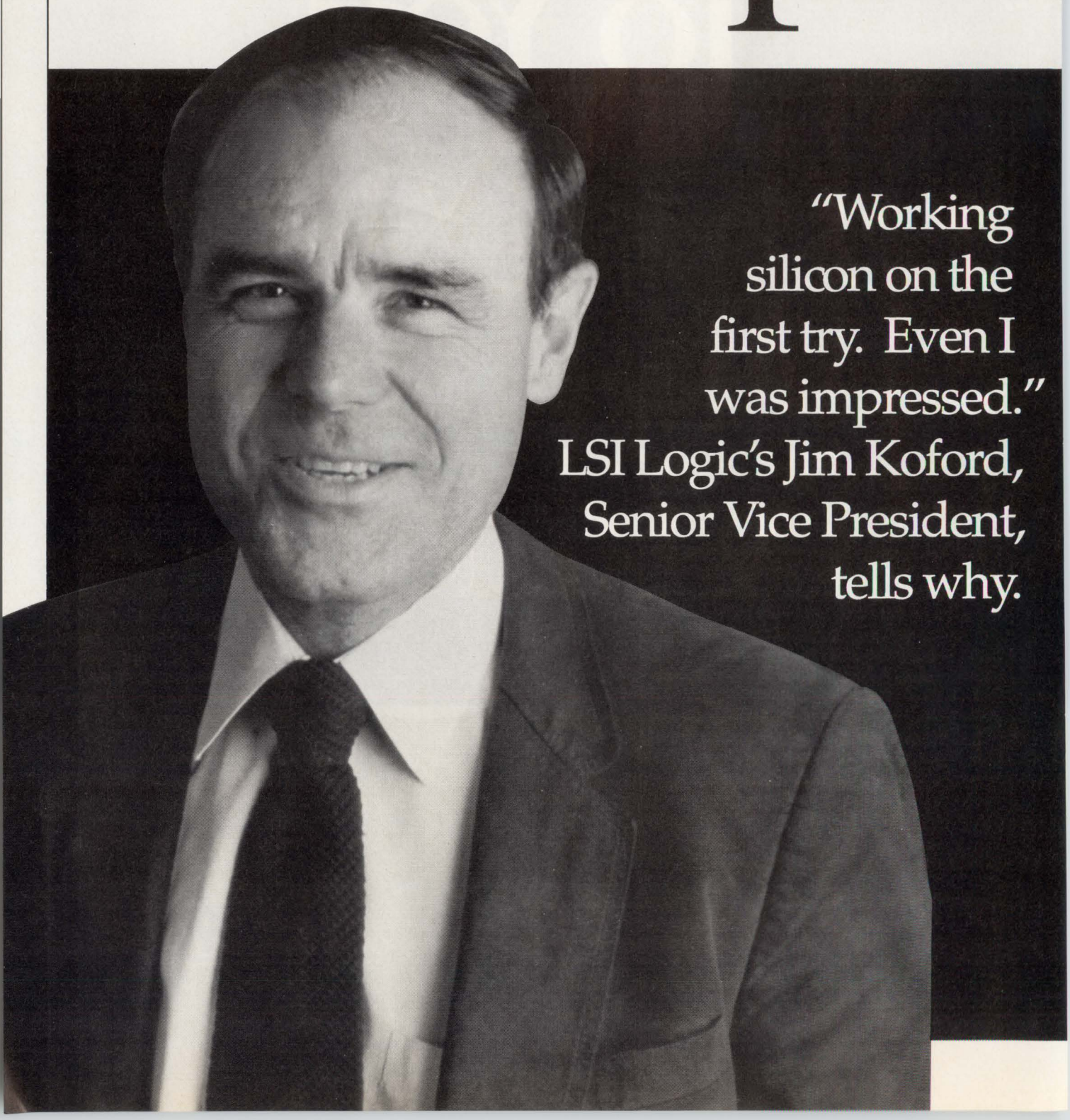

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depths will decrease to just a tenth of a micrometer or so, making the structures even more sensitive to damage from plasmas, implants, and high temperatures. Future etch processes will need to be gentler and still provide good etch rates, uniformity, selectivity, and profile control. Most of the recently released etching systems can deliver results with uniformities to within about 5%. However, over the next few years, the tolerance will have to tighten as the feature sizes shrink.

Although plasma etching has virtually taken over almost all key etch steps, some recent developments with chemical etching or the use of focused ion-beam systems show promise for future processing. In fact, chemical etching seems to be coming back when used with light mechanical grinding of the wafers. This combination is being experimented with to planarize the intermediate dielectric layers as a wafer is manufactured.

Flattening The Surface

A critical aspect of manufacturing for new-generation chips is planarization, which is necessary because in many cases three or more levels of metal interconnection layers, or three or four levels of polysilicon, can be used. Random logic circuits implemented in gate arrays, and structured logic such as microprocessors, gain significant density improvements as they switch from two to three levels of metal interconnections. However, as more levels are added, the surface planarity that each successive metal layer must be deposited upon gets worse, requiring additional corrective action.

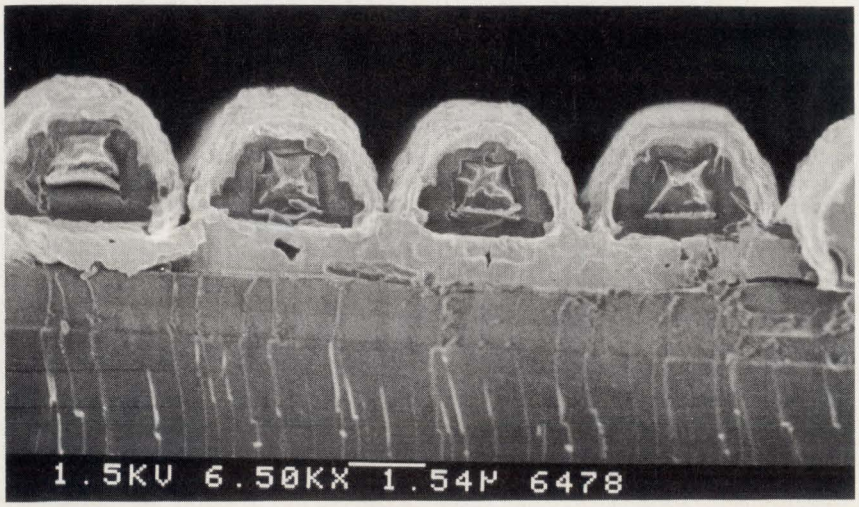
According to Tony Alvarez, director of technology at Cypress Semiconductor, San Jose, Calif., planarity must be managed, layer-by-layer, as dimensions decrease. A key reason, he explains, is the small depth of focus for the optical-lithography systems. To build static RAMs (Cypress's key products), designers will have to move to three or four layers of polysilicon, but not for resistor elements.

As the layers increase, surface planarity will suffer unless layers are planarized. Polysilicon resistor loads will give way from those used in the 1-Mbit generation of SRAMs to thin-film transistors in the 4- and 16-Mbit generation of SRAMs. The thin-film transistors would be implemented in the polysilicon above the surface of the wafer. The thin-film devices reduce the memory cell's leakage current by a considerable amount over the leakage in polysilicon-resistor-based cells. A difference of just 1 nA per cell, for instance, translates to 4 mA at the chip level—a significant amount of current if battery backup is a key requirement.

The most attractive planarization schemes now gaining acceptance include the use of tungsten plugs, which are formed by CVD, and aluminum plugs, which can now be deposited by a sputtering scheme. Experiments with copper CVD also show promise, but such systems will probably stay in the lab until the mid- to late '90s. The tungsten and aluminum CVD schemes are starting to replace approaches that deposit overly thick layers of dielectric, and then etch back the surface to planarize the top edge prior to depositing the metal layer.

In its efforts to add a third layer of metal in its next-generation CMOS process, the CEMOS 7, researchers at Integrated Device Technology Inc., Santa Clara, Calif., kept aluminum for the level-1 metal layer to minimize RC delays, but added tungsten plugs to planarize the surface upon which level-2 metal is deposited *(Fig. 4)*. The triple-metal process, slated for production release by mid-1993, will employ drawn feature sizes of about 0.6 μm and have a metal-to-metal pitch of 1.2 μm.

Careful attention must be paid to the contact- and via-hole openings to make sure they don't get over-etched and become too wide, or under-etched and prevent contact with the underlying layer. Often, a short surface-reflow operation is done with thermal annealing systems to reduce the vertical sidewall slopes and even out any etchback differences. The reflow thus minimizes any step-coverage problems that metallization layers often encounter. (Step coverage problems refer to the thinning or even non-deposition of metal along



5. Selective deposition of dielectric material around an air-bridge conductor and a subsequent layer of metallization allows National Semiconductor's researchers to create on-chip coaxial conductors—the equivalent of shielded cables. Although still experimental, such etching and deposition capabilities will make possible many novel configurations during the next few years.

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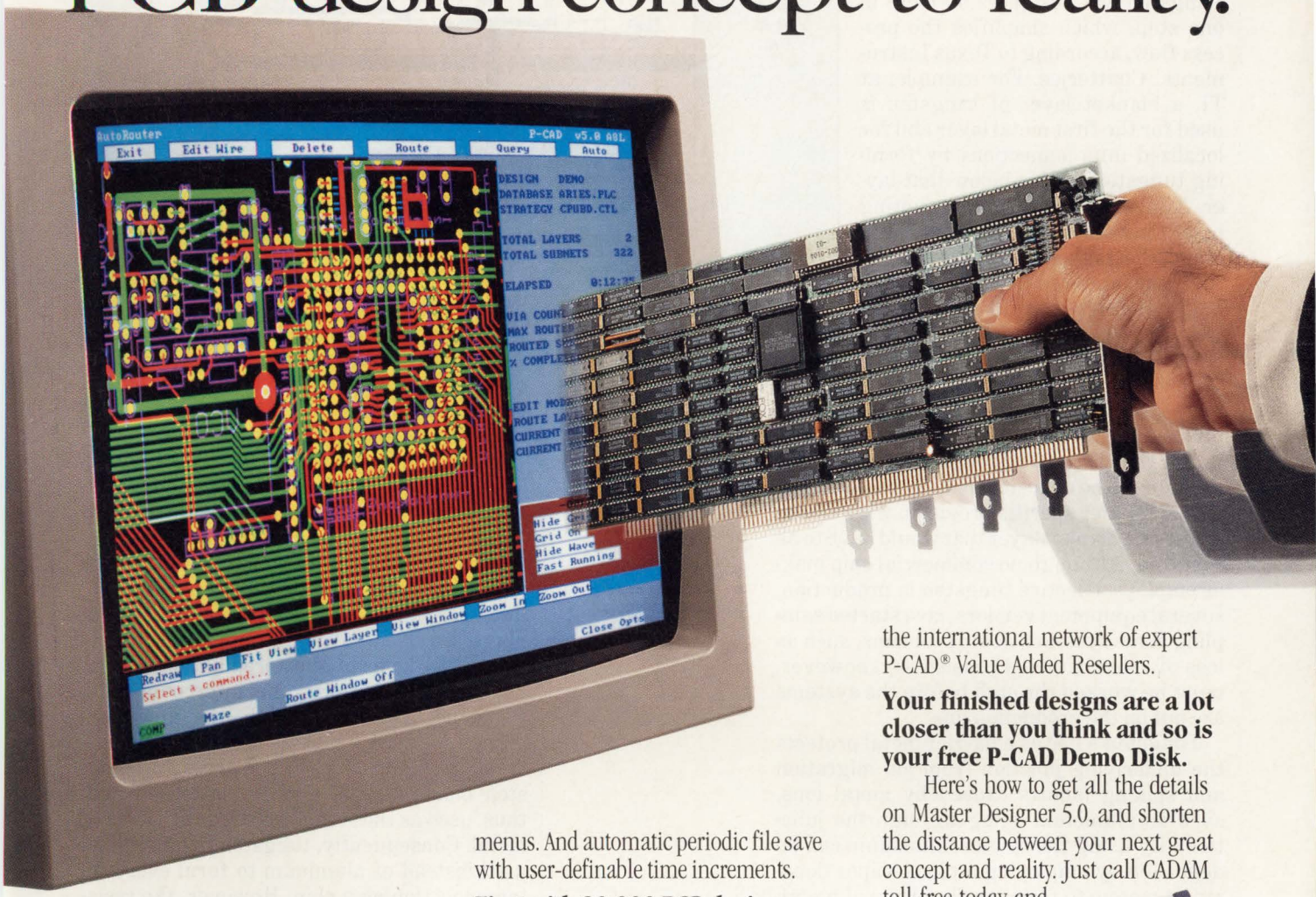

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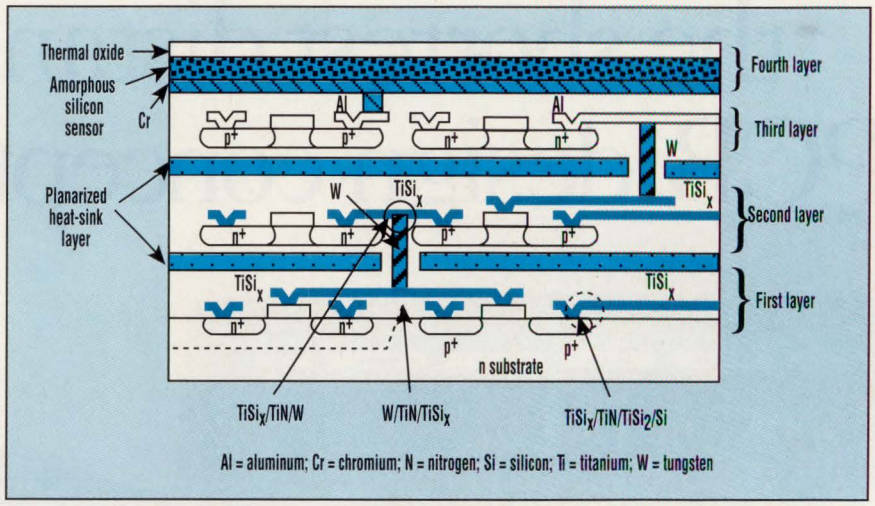
the inside vertical edge and corner of a via or contact opening.)

Tungsten deposition schemes—both blanket and selective—are beginning to replace the insulation-deposition and etch-back approach. Tungsten lets designers do more in one step, which simplifies the process flow, according to Texas Instruments' Chatterjee. For example, at TI, a blanket layer of tungsten is used for the first metal layer and for localized interconnections by forming tungsten-silicide below that layer. Tungsten has a higher melting point than aluminum, so it can withstand the higher process temperatures encountered during the latter half of the chip-manufacturing process.



6. Four layers of single-crystal silicon were stacked one above the other by researchers at Matsushita to form an image processor. The chip both detects the image as well as processes the digital information, eliminating the complex interdevice wiring that must typically be implemented to interconnect imaging arrays to all of the amplifiers and signal-processing logic.

Depositing Selectively

Selective deposition is a potential solution to the complexity of blanket tungsten approaches because it requires one process step rather than three. The selectivity permits the tungsten to be deposited only in the contacts, vias and other specified regions, without the waste of a blanket layer that would have to be removed. Although no commercial chip maker employs selective tungsten in production, several equipment vendors have started sampling some systems. Some problems, such as loss of selectivity and consistency, however, must be worked through before the systems are put on the production line.

Tungsten's use as a barrier metal protects the underlying junction from ion migration and spiking (shorts caused by metal ions, such as aluminum going through the junction). By using the barrier, aluminum can be deposited by employing a phase-vapor deposition system to form the first level of metal, and etching to form a bimetal line when the second layer of metal is deposited. That approach also reduces metal electromigration and improves chip reliability.

Recent research advances, however, show that there's still plenty of life left with aluminum for use as a plug-fill material. A new deposition scheme combines standard magnetron sputtering with heating to increase aluminum mobility. Fill aspect ratios of 3:1 were demonstrated in 1990 by SGS-Thomson Microelectronics, Carrollton, Tex,, and more recently by others. ASM America Inc., Phoenix, Ariz., a supplier of deposition systems, has shown aluminum can give tungsten a run for its money as a planarizing plug.

Experiments show that aluminum provides step coverage over 95% and has a resistivity of less than 3 $\mu\Omega$-cm. A small amount of copper doping helps reduce electromigration. Aluminum also offers one major advantage over tungsten: Aluminum sputtering can be done on basically the same equipment already in use, and in one step.

In the blanket schemes, the CVD systems deposit tungsten into the via and then continue depositing tungsten on top of the insulating layer. Because tungsten adheres loosely to silicon dioxides—but well to metals and to silicon—the tungsten that overlays the insulator can easily be etched back if only the plugs are used. After the etch-back operation, a flat layer of sputtered aluminum can be deposited to form the interconnection. With the blanket approach, the unwanted tungsten can readily be removed by etching.

Rather than just be etched away, the tungsten blanket could also be patterned and, thus, used as the second, third, or nth level of metal. Consequently, tungsten layers can be used instead of aluminum to form every interconnection on a chip. However, the resistance of tungsten is several times that of aluminum, so it's unlikely that all-tungsten interconnect systems will be the dominant metal scheme for on-chip interconnections.

To date, interconnections on chips are single-conductor planar lines. However, as on-chip frequencies increase, coaxial conductors that provide shielding or controlled impedances will be needed. Experimenting with coaxial conductors, researchers at National Semiconductor Corp., Santa Clara, Calif., created coaxial structures made from tungsten that mimic shielded coaxial cables *(Fig. 5)*.

To make the conductors, Court Skinner, the company's Director of Technology, explains that metal wire that becomes the core conductor must first be deposited and then the material around the conductor must be

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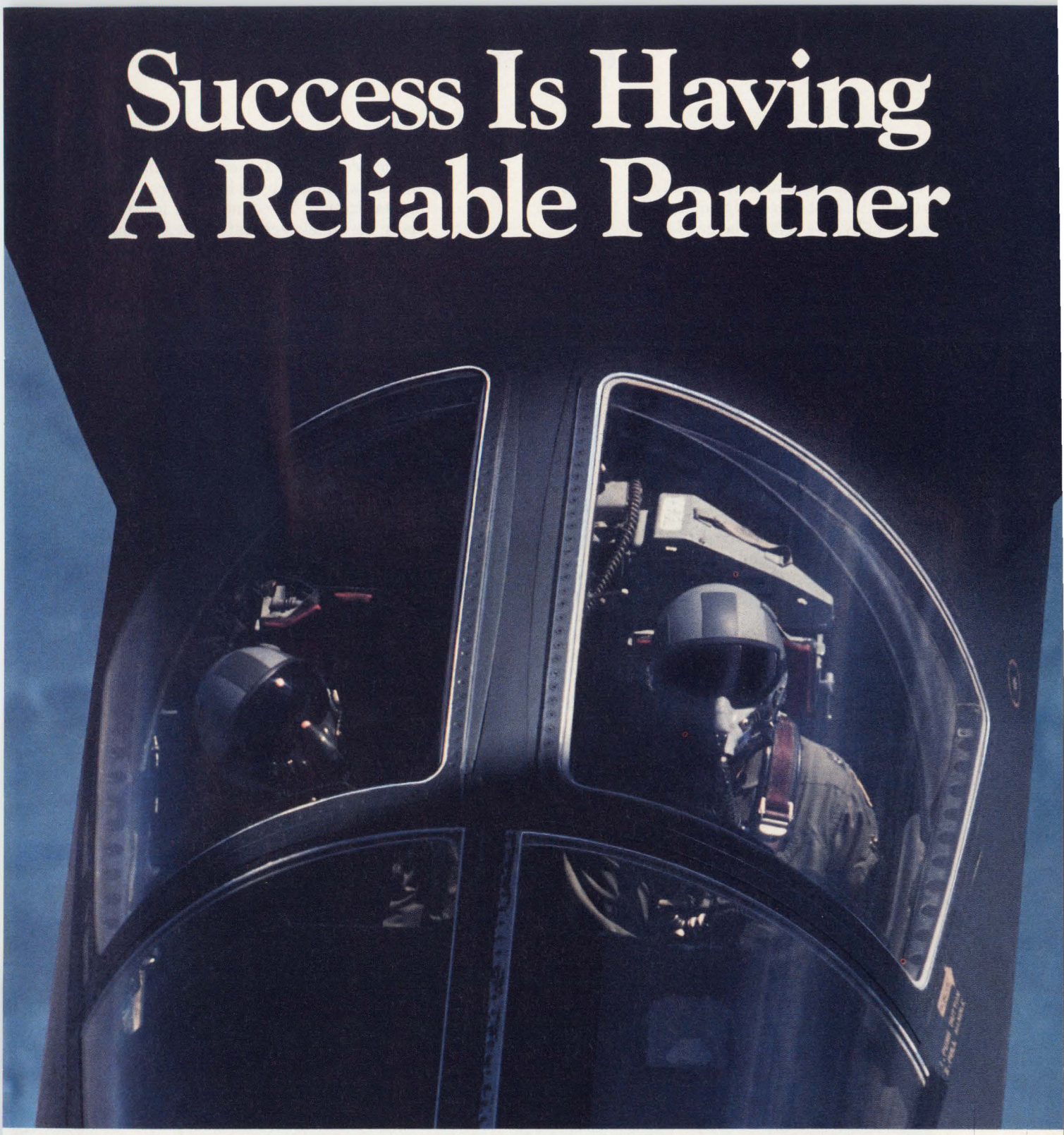

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removed so that the conductor becomes an air bridge. Then insulating material that only adheres to the metal of the air-bridge material is deposited. Finally, the second layer of metal is deposited on top of the insulating material to form the coaxial shield. Multiple conductor paths can thus be simultaneously created for shielded, low-noise signal transfers.

Developments in lithography, etching and deposition promise not only great strides in chip integration levels, but also in circuit performance. One novel area is the creation of three-dimensional circuits in which multiple layers of active elements are stacked one above the other to form complex subsystems on a single chip. At last September's European Solid-State Devices Research Conference in Montreux, Switzerland, numerous papers presented results of Japan's 3D IC project, sponsored by the Research and Development Association for Future Electron Devices in Tokyo. Efforts in large-area silicon-on-insulator (SOI), gallium-arsenide on silicon, and wafer bonding were detailed.

One effort describes the creation of five stacked layers of 9.5-by-9.5-mm SOI crystal fabricated by researchers at Toshiba Corp., Kawasaki, Japan, by using electron-beam recrystallization. To connect the layers, especially the widely separated ones, Toshiba developed a 6-μm via-hole-filling scheme that can deal with vias with aspect ratios of 7:1. Devices made in the recrystallized layers are 0.25-μm-gate MOS transistors formed by optical lithography and reactive-ion etching.

Additional activities described by the Association include a multilayer IC for range sensing. The chip, from Mitsubishi Electric Co. Ltd., Itami, Japan, has four layers that respectively contain a 64-by-64 array of image sensors, one row of 64 sensor circuits, an 8-by-8 array of 2-bit CMOS a-d converters, and a CMOS ring pointer plus an 8-by-8 subtraction circuit on the fourth layer. From Matsushita Electric Industrial Co. Ltd., Osaka, Japan, another 4-layer chip packs a complete parallel image processor containing a 64-by-64 array of sensors on one layer, level detectors on the second, the frame memory on the third level, and the arithmetic circuits on the lowest layer *(Fig. 6)*.

However, along with the shrinking fea-

tures come what might be some design challenges at the device and circuit level. For instance, as key dimensions shrink below about 0.6 μm, supply voltages must be reduced or the transistors will overload. The industry is already starting to jump onto the 3.3-V reduced power-supply standard defined by JEDEC. Reducing the operating voltage either internal or external to the chip reduces voltage stresses and thins out oxide levels without damaging the devices.

The lower voltages, though, may impact performance unless designers can compensate for the bias differences. Changes in transistor design and ion-implant levels will be made to adjust device thresholds and keep circuit performance as high as practical. At 3.3 V, biCMOS logic should work fine when implemented with devices in the 0.5-μm range. However, in the latter part of the decade, dimensions should drop to about 0.25 μm, and that might require the supply level to drop still further to less then 2.4 V *(Table 2)*. With such a low supply level, many designers question the performance or flexibility of biCMOS logic. Many believe that biCMOS is a short-term solution for the first half of this decade and full CMOS will be the long-term answer.

One way to counter the lower performance of the biCMOS circuits is to use dual power supplies—an approach suggested by both Dr. Susumu Kohyama, general manager of the LSI division of Toshiba Corp., Tokyo, and Tony Alverez, director of technology development at Cypress Semiconductor. Rather than power the circuits from a 3.3-V supply, use dual supplies, such as one that provides the standard 5 V and another that supplies the lower 3.3-V level. At lower supply voltage levels, performance degrades quickly and the dual-supply approach could extend the usable life of ICs into the next century.

BiCMOS circuits currently deliver performance gains of 50 to 100% over standard CMOS circuits, but at the cost of adding three to five masks steps to overall chip processing. With 0.8-μm features, a biCMOS chip can outperform a similar circuit implemented with pure CMOS logic with 0.5-μm features. However, biCMOS' manufacturing complexity and its higher prices have held back its widespread popularity for logic and memories.

Pure bipolar circuits are also advancing as feature sizes decrease. One of the few companies specializing in bipolar-only technology, Bipolar Integrated Technology Inc., Beaverton, Ore., has several generations of processes scheduled through mid-1993 *(Table 3)*. The most advanced process relies on relatively relaxed design rules—0.8-μm minimum feature sizes. With the ability to pack up to about 400,000 equivalent gates onto a chip area of 225 mm^2, the process relies on tight metal-metal spacing—just 2 μm—for all three levels of metal interconnections.

Combinations of doping and specialized lithography allow designers at Hitachi Ltd., Tokyo, to build a 64-GHz bipolar transistor, as described last month at the International Electron Device Meeting (IEDM) in Washington D.C. The addition of germanium to the base of bipolar devices was also discussed at both the 1990 and 91 IEDMs by IBM, Yorktown Heights, N.Y., and Princeton University, N.J. Such transistors have exceptionally high cutoff frequencies and would make ideal building blocks for logic circuits. Germanium logic circuits, though, will have to wait. Germanium-base structures are still experimental and probably won't be used commercially until the latter part of this decade in anything other than discrete form.

The promised merger between GaAs and silicon is also coming closer as more reproducible results are achieved with GaAs layers deposited on silicon wafers. Such an approach can potentially solve three design issues. First, it can eventually drastically lower the substrate cost of GaAs circuits because only a thin epitaxial film would be needed rather than an entire GaAs wafer. Second, the silicon substrate provides a better thermal path for heat removal and a sturdier working base material. And third, it would allow the close coupling of high-speed or optical GaAs components or circuits to ULSI silicon logic, eliminating the need to propagate high-speed signals across a circuit board.□

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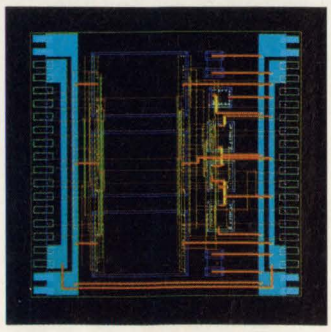

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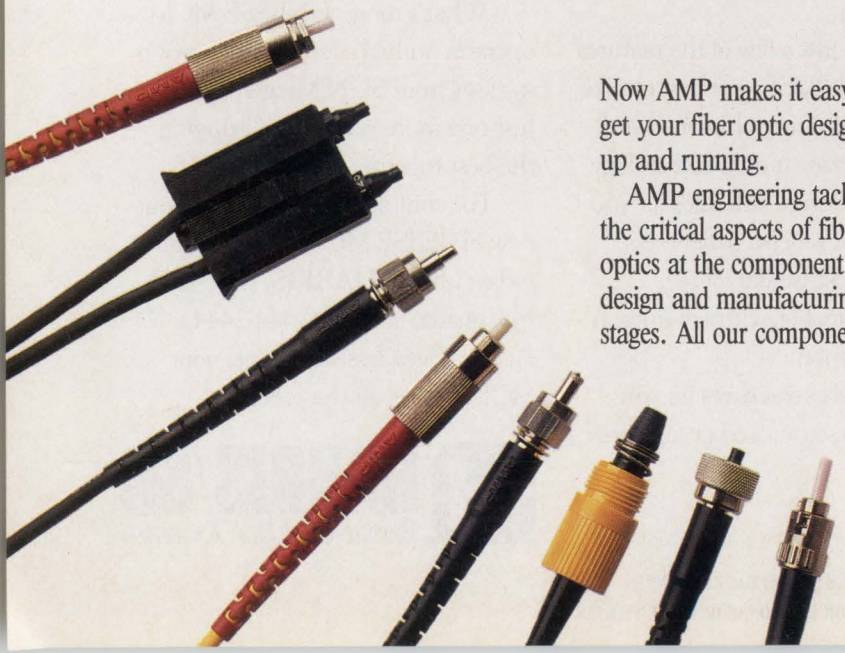

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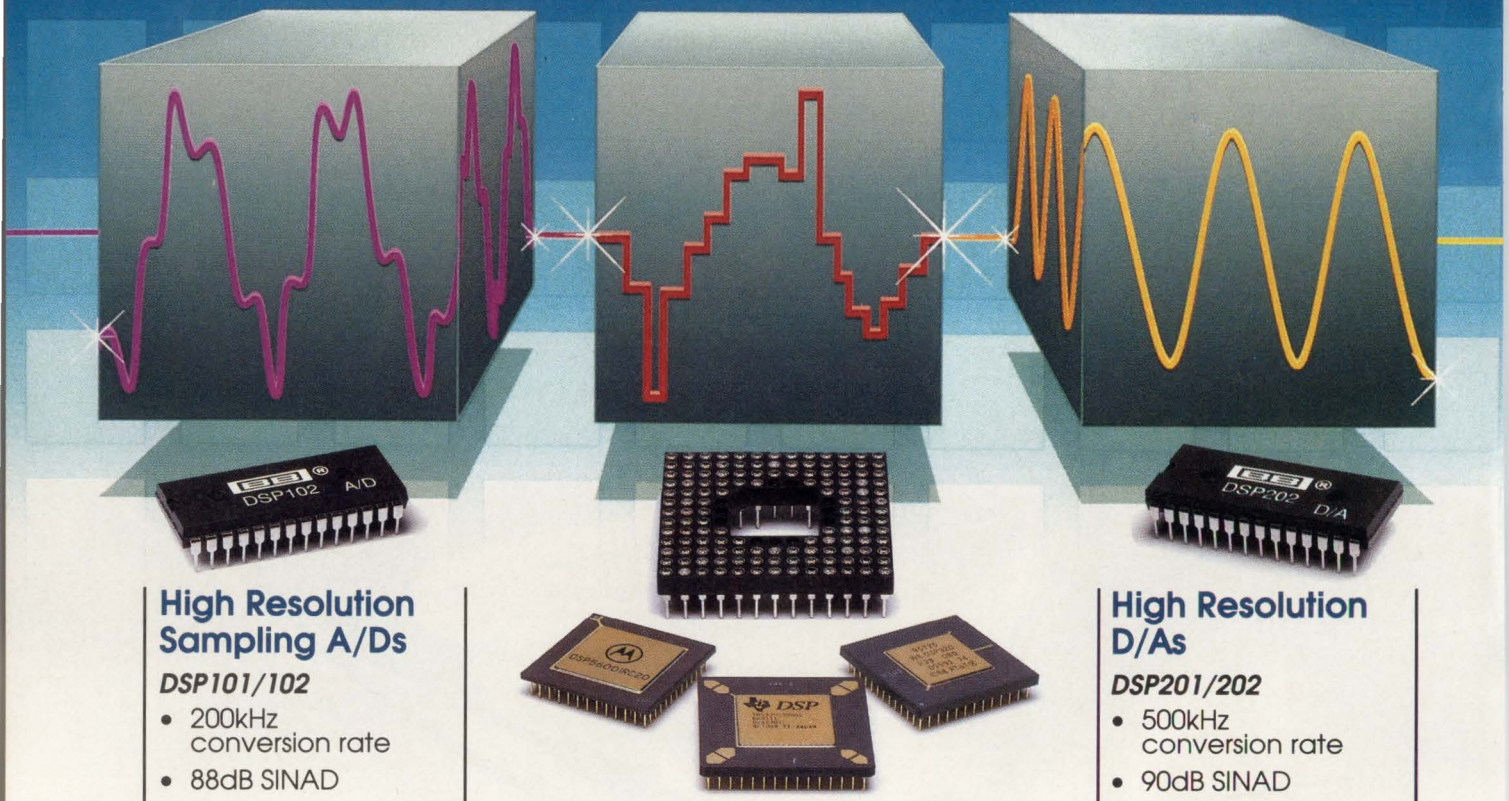

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NEW PROCESSES TO SPAWN NEXT-GENERATION ANALOG, MIXED-SIGNAL, POWER ICs

FUTURE SUBMICRON PROCESSES ON SOI WAFERS TO BOAST f_ts BEYOND 25 GHz.

BY FRANK GOODENOUGH

The next generation of analog, mixed-signal, and power/high-voltage ICs will be built on processes that didn't even exist five years ago. Though these future processes are currently in different stages of development, they represent an ongoing revolution in semiconductor processing. The devices to be built on them will create products ranging from disk drives, cordless telephones, and wireless local-area networks, to global-positioning-system (GPS) receivers, PC and workstation graphics, imaging systems, motor controls, and classic data-acquisition systems. Most of these ICs will be true mixed-signal systems on a chip. Some will be largely digital. But analog, including RF, and/or power-control functions will tie them to the real *analog* world.

The real sleeper technology for the next generation of ICs may be the wafers these ICs will be built on. Direct wafer bonding is turning dielectric isolation (DI) into a broad-based technology available to anyone. Bonded wafers, and IC processes designed for them, will become the technology of choice for the highest-performance analog, mixed-signal and power/high-voltage ICs. Of the half-dozen or so companies either serious or thinking about the technology, all are considering it for high-speed analog/mixed-signal applications.

Over half of these companies are also considering the technology for power/high-voltage ICs. Wafer bonding, or some other form of silicon-on-insulator (SOI) technology, such as SIMOX (separation by implantation of oxygen), may also take over mainstream digital CMOS as gate lengths drop well below 0.5 μm (ELECTRONIC DESIGN, *"A brief review of SOI technologies and their advantages," Dec. 19, 1991, p. 40).*

One new major application area on the rise for analog and mixed-signal silicon IC technology is RF circuits, made possible by IC-transistor unity gain cutoff frequencies (f_ts) reaching above 10 GHz. Such f_ts are expected to challenge those of future transistors made from gallium arsenide and other III/V materials.

Long the domain of discrete and hybrid devices, RF circuits are now going the monolithic-IC route. The demand for "personal" wireless (both voice and data) communications links has moved once exotic applications into consumer products found in discount stores. It's known that one IC supplier's goal is to own all of the silicon between the antenna and the microphone or speaker of a cellular telephone. RF chips will go into upcoming digital cordless telephones, advanced modems, GPS receivers and re-broadcast transmitters, and direct-broadcast satellite (DBS) TV receivers. Transistors with similar bandwidths will be required for the ICs to bring glass-fiber cables into every home either via cable-TV or the telephone system.

With a few exceptions (particularly the domination of the high-speed op-amp field by Harris Semiconductor), most analog and mixed-signal ICs, until recently, have been built on versions of processes little changed over the last 15 to 25 years. Robert Widlar's μA709 op amp on the "standard bipolar process" came out in 1967, and National Semi-

conductor added JFET op amps to the process in 1974. The metal-gate CMOS process used for most chopper-stabilized op amps, integrating analog-to-digital converters, and analog switches (which originated at Intersil, now Harris Semiconductor) isn't much younger. In fact, whereas most digital ICs today are built in fabrication facilities that required their chief executive officers to "bet the company," the vast volume of analog ICs shipped today still can be built in already-paid-for "obsolete" fabrication facilities (it should be noted that many are built-in advanced fabrication facilities where significantly higher yields are usually achieved). Moreover, with the exception of the CMOS devices, ICs that could operate with 30 V between their rails were the order of the day.

The revolution in semiconductor processing didn't explode on the scene. Various innovative product developments that took place during the 1980s (and even earlier) truly represented what was to come. Like virtually all advanced analog ICs, most were the work of skilled circuit designers taking advantage of available semiconductor processes.

Crystal Balls Needed

Today, the time-to-market factor dominates process development. Since looking even five years ahead is impossible, new-process development must be quick. To ensure having processes available when IC designers need them, one major semiconductor company is looking to develop a new process in under two years.

One way to cut process development time is to draw more heavily from mainstream digital technology, rather than just use the techniques and equipment developed for it (fine-line lithography, reactive ion etching, trenching, polysilicon emitters, double-metal interconnects, recessed oxide). A second, and quite different path, is to employ a long-range plan for process development with evolutionary, but significant, performance upgrades as time passes. With this approach and a little insight, processes are available when they're needed. A third approach, the so-called modular process, exploits the other two approaches.

In a modular process, each module builds a particular type of active or passive device (npn transistor, CMOS inverter, oxide capacitor). The designer, as if in a cafeteria, and with an eye on the budget, picks and chooses the modules needed for a particular IC. If a new kind of device is needed, or better specifications are needed for an existing device, only a process specific to that device or specification need be developed.

One way to cut process development time is to draw more heavily on mainstream digital technology, rather than just use the techniques and equipment developed for it

A number of process types compete fiercely with each other for the next generations of analog, mixed-signal, and power ICs, just as the ICs to be built with them compete for the system designer's tasks. And although the distinct line between process types may tend to blur as time passes, most process types will be used throughout the 1990s. IC designers can now choose among at least five different process types:

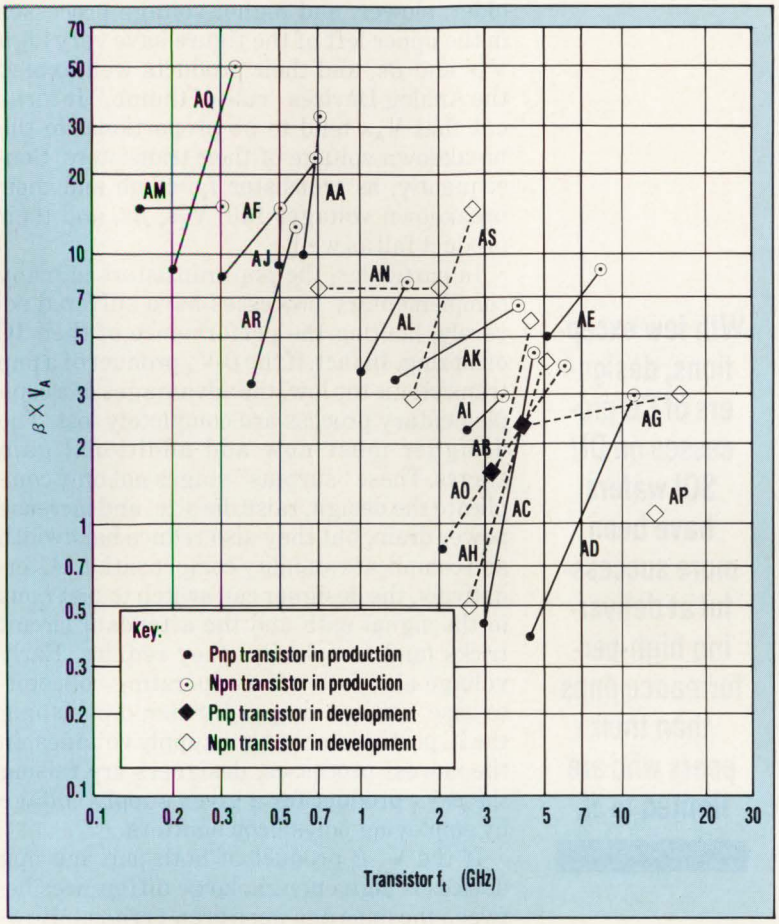
- *Bipolar technologies* limited to very high-speed vertical npn transistors. These are either upgraded versions of the 25-year-old workhorse "standard bipolar" process, or are derived from digital ECL processes.
- *High-speed complementary bipolar (CB) processes* using either junction isolation (JI) or dielectric isolation (DI).
- *Fine-geometry CMOS processes*, either upgraded versions of so-called linear CMOS processes, or modified or even non-modified versions of digital CMOS processes.
- *Power and high-voltage IC processes* containing a mix of two or more of the following transistor types: high-voltage npn, pnp, DMOS, or CMOS transistors; or small-signal npn, pnp, and CMOS transistors.
- *High-speed biCMOS processes*, which may be upgraded versions of today's analog biMOS technologies or some mix of the previous four processes.

Three Development Paths

Each of these five process types fits nicely into one of the three process-development paths, which aim to ensure that future processes will be available when needed. The two pure-bipolar process types demand that the long-range planning approach be used. Fine-line CMOS processes must rely on access to mainstream digital IC technology. And successful biCMOS processes must be modular in structure.

Until recently, power and high-voltage IC processes have represented a slow, evolutionary-type technology. But that may change, with those processes evolving into modular methods that eventually merge with biCMOS technology.

However, the ultimate process type for the late 1990s will be modular—on bonded wafers. The 5-V technology will offer CB transistors with f_ts beyond 10 GHz, submicron CMOS, and EEPROMs. In addition, it will offer DMOS transistors that can switch 50 V at currents of hundreds of milliamperes.



HIGH-SPEED ANALOG BIPOLAR AND COMPLEMENTARY BIPOLAR CMOS PROCESSES

Code	Company	Process type	Voltage	Product status
AA	Analog Devices	CBJI	30 V	Now
AB	Analog Devices	CBBW	12 V	Soon
AC	AT&T	CBJI	13 V	Now
AD	AT&T	CBJI	5 V	Soon
AE	Harris Semiconductor	CBBW	30 V	Soon
AF	Harris Semiconductor	CBDI	30 V	Now
AG	Motorola Semiconductor	CBBW	5 V	Experimental
AH	Raytheon Semiconductor	CBJI	12 V	1992
AI	Elantec	CBDI	15 V	In development
AJ	Linear Technology	CBJI	30 V	Now
AK	Exar	CBJI-CMOS	5 V	Now
AL	Exar	CBJI-CMOS	18 V	Now
AM	Texas Instruments	CBJI	30 V	Now
AN	Texas Instruments	CBJI	30 V	1992
AO	Maxim (VLSI Technology)	CBJI	5 V	Now
AP	Tektronix	npn-only JI	5 V	In development
AQ	National Semiconductor	CBJI	30 V	Now
AR	National Semiconductor	CBJI	30 V	Now
AS	National Semiconductor	CBJI	30 V	In development

CB = complementary bipolar
JI = junction isolation
DI = conventional dielectric isolation
BW = bonded wafer dielectric isolation

1. Cutoff frequency, f_t, and the product of current gain, β, and Early voltage, V_A, represent the primary figures of merit for high-frequency transistors aimed at analog ICs. Here they're plotted against each other for the npn and pnp transistors from a number of present and future bipolar processes. As f_t climbs, the voltage rating (noted by each data point) and β-V_A product fall, particularly that of the pnp in complementary processes.

Starting with CB processes, this article will explore these merging technologies individually to see where they are today, where they're going, what's important, what kind of chips are going to be built on them, and who is going to use them.

WAND WAVING

For IC designers stuck for years with JI, npn-only processes, access to a DI-CB process must give them the feeling that they're Mandrake the Magician waving a wand over the silicon. Not only can fast vertical pnp transistors "complement" the npn transistors, but every transistor can be isolated from every other transistor with a layer of silicon dioxide (glass) rated to take over 2000 V. And at least theoretically, any kind of active or passive silicon device yet conceived can be put on the chip, as well as devices like laser-trimmable thin-film resistors. Reduced parasitic capacitances raise speeds and bandwidths while the dc parasitics that cause latch-up effects disappear.

The latest process of this genre comes from Harris, the inventors of DI. Called UHF-1, it provides a true glimpse of the future (ELECTRONIC DESIGN, *Dec. 19, 1991, p. 35)*. UHF-1 not only represents the first example of using bonded-wafer (SOI) technology with available products in the merchant-market analog-IC field, but its vertical npn and pnp transistors offer the analog-IC designer unprecedented performance characteristics. The process possesses f_ts of 8 and 4 GHz for the npn and pnp transistors, respectively, and also equips these npns and pnps with Early voltages (V_As) of 60 and 40 V, respectively. Until UHF-1, transistors this fast (particularly pnps) haven't offered designers the luxury of Early voltages this high.

V_A, along with the more familiar current gain, β, and the product of V_A and β, can be considered *the* prime figures of merit for bipolar transistors aimed at analog ICs. Process-dependent, these figures of merit, until now, have been overlooked except among analog-IC designers or their process-designing compatriots. In fact, at the recent International Electron Devices Meeting (IEDM) in Washington D.C. last December—the primary venue for describing the latest achievements in semiconductor process/device technologies—just one paper mentioned V_A and the product β-V_A.

Essentially, V_A defines the collector (output) resistance of a bipolar transistor. The higher its value, the higher the resistance, and the more closely the device approaches the ideal npn or pnp transistor with an infinite

output resistance (that is, a perfect current source). Forcing current into that high-resistance node creates voltage gain in a common-base circuit. The higher the V_A, the higher the gain. Current sources and current mirrors dominate analog-IC design, when both are biasing circuits and acting as dynamic loads. Once again, transistor V_A determines current-source performance.

Precocious Product

The product of β and V_A is similarly important (the units for β multiplied by V_A are obviously volts, but because the product is a figure of merit with no "practical" meaning, it's usually left dimensionless). In a cascode configuration (a common-emitter-connected transistor in series with a common-base-connected device), the core of most of today's op-amp designs, voltage gain is directly proportional to that β-V_A product. Consequently, a high β-V_A product helps eliminate unnecessary gain stages, which in turn helps create faster and wider-bandwidth ICs while maintaining precision. This product is ideal as a figure of merit, because it tends to be a constant over a range of operating currents for a given device. That is, as β typical rises and falls in value with increasing collector current, V_A changes proportionally in the opposite direction.

Designers at Analog Devices follow a rule of thumb: The β-V_A product should be in the same ballpark as the accuracy of the circuit in significant bits of resolution. That is, if an op amp offers accuracy to within 0.1% (about 10 bits), its β-V_A product should be about 2^{10} or about 1000. Similarly, the transistors in 12-bit-accurate (0.01%) circuits need a β-V_A product of about 4000. Thus, to evaluate the relative merits of the transistors from different processes for wideband and high-speed analog circuits, taking into account f_t as well as the β-V_A product, they should be plotted against each other *(Fig. 1)*.

In the figure, straight lines connect npn and pnp transistors from the same CB process. Data points for npns without a pnp cohort indicate an npn-only process. Circles represent processes on which products are being built today. Diamonds represent processes in some stage of development. The two uppercase letters by each line connecting npn-pnp pairs are keyed to additional process information in the table. The voltage displayed with each data point is the "practical operating" voltage for ICs built on the process.

By glancing at the figure, it can be seen why V_A, and its product with β, may have been neglected in the past. Transistors from older, slower, and higher-voltage processes in the upper-left of the figure have very high V_As and βs, and their products well exceed the Analog Devices "rule of thumb." It turns out that V_As tend to be proportional to the breakdown voltage of their transistors. Consequently, as transistor f_ts climb and their breakdown voltages fall, V_As, βs, and their product fall as well.

With few exceptions, designers of CB processes on DI/SOI wafers have been more successful at delivering high-performance pnps than their peers who are limited to JI.

In particular, the pnp transistors in many complementary processes have suffered severely, limiting the performance of their IC offspring. In fact, if the β-V_A product of a pnp transistor is too low, the advantages of a complementary process are completely lost. The designer must now add additional gain stages. These "surplus" stages not only complicate the design, raise die size, and increase power drain, but they also reduce bandwidth and complicate stability compensation. Alternatively, the designer can switch to just npns in the signal path and the attendant circuit tricks (and complexity) they require. Early voltage also falls off as operating collector-to-base voltage drops, further diminishing the IC performance at low supply voltages. In the newest processes, designers are raising the β-V_A product for a given supply voltage by employing polysilicon emitters.

If the V_A-β product of both pnp and npn devices is high enough, large differences between the pnps and npns aren't critical. However, large differences between the f_ts of the npn and the pnp transistors will limit the final IC's speed and bandwidth to that permitted by the slower device, and the condition will cause second-harmonic distortion in complementary circuits. As a result, solely using the npns becomes an alternative solution. Obviously, a complementary process suffering from pnps that are both significantly slower and have a limited V_A-β product offers the IC designer a real challenge.

Benchmarks

With few exceptions, designers of CB processes on DI/SOI wafers have been more successful at delivering high-performance pnps than their peers who are limited to JI. This is somewhat expected due to JI's greater dc and ac parasitics, as well as processing complexity. However, two JI processes stand out as CB benchmarks regardless of wafer type—those from Analog Devices and Linear Technology *(data points AA and AJ, respectively, Fig. 1)*. Though V_A isn't a problem in 30-V processes, the two JI processes have given virtually identical f_ts to both npns and pnps. And both did it by optimizing the pnp transistor. In an approach opposite that of others,

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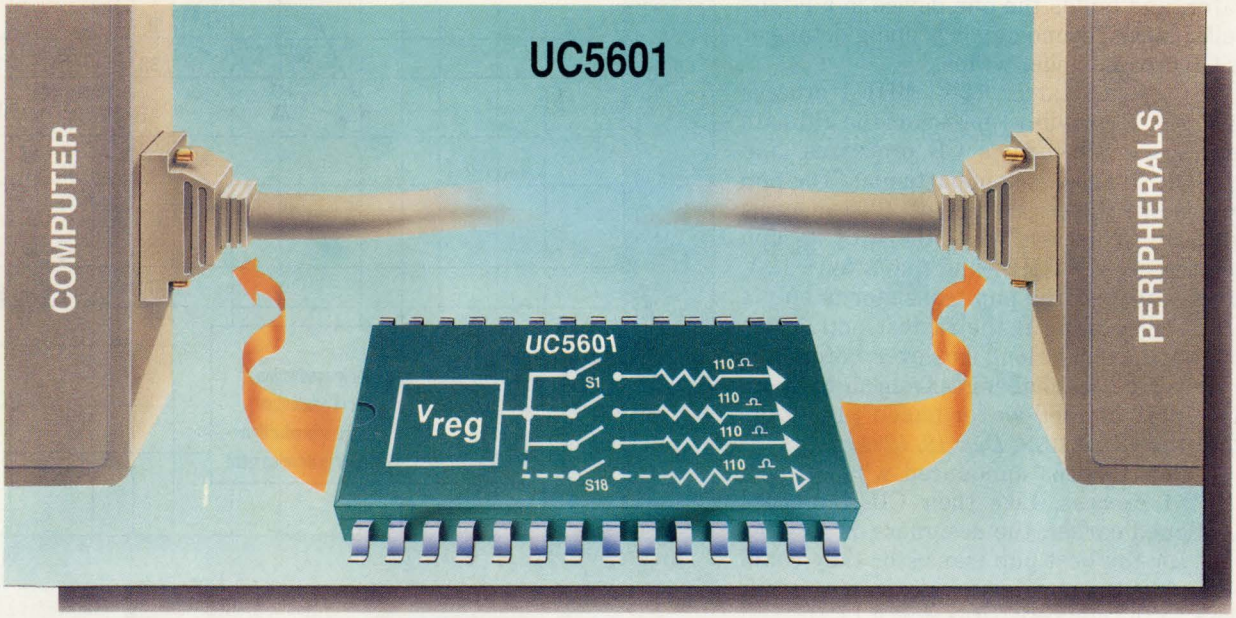

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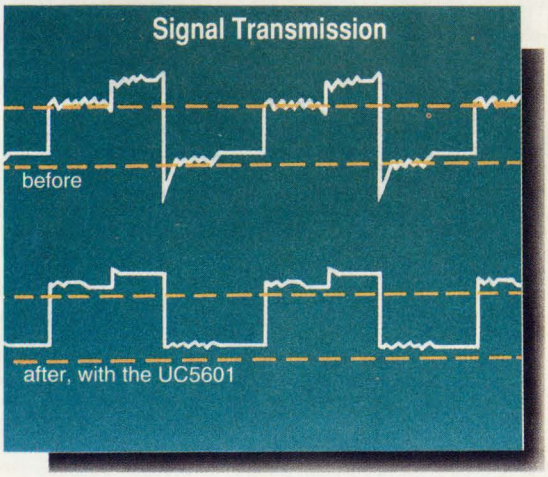

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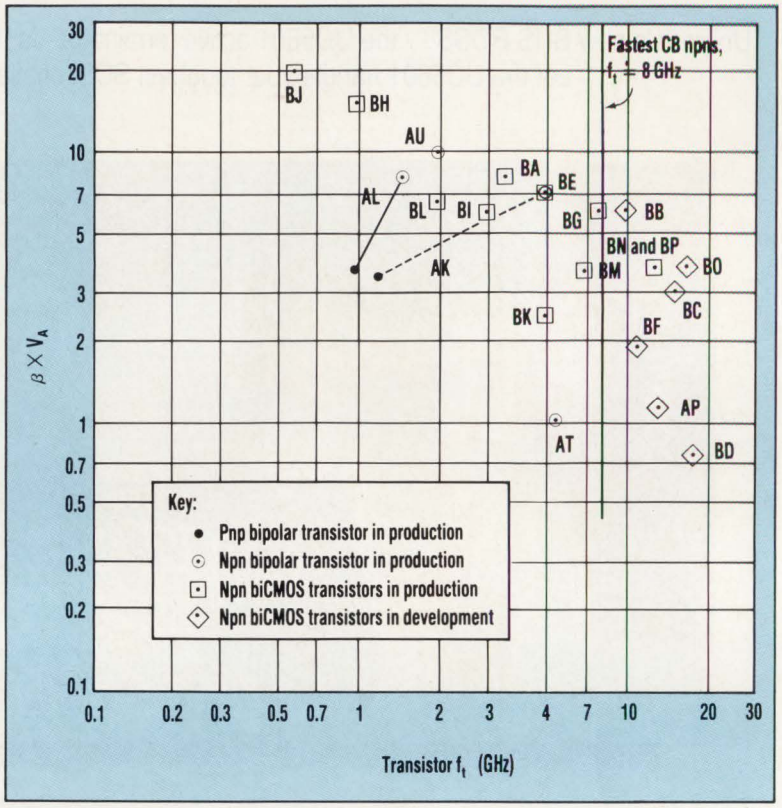
both companies designed the best possible pnp transistor and took the resulting npn transistor. Analog Devices did the job with a patented design that builds the pnp device in p-type epitaxial silicon grown on an n-type wafer, and builds the npn device in a p-type well. Linear Technology is keeping details of its CB process under wraps.

At present, Harris' 12-V, UHF-1 process *(AE, Fig. 1)* certainly represents the ultimate benchmark for today's CB processes, and DI/SOI-CB processes in particular. The pnp transistor's V_A-β product of 4000 ensures precision. However, while the f_t of its npn counterpart is 8 GHz—and that's for a 12-V device—that of the pnp transistor is only 4 GHz, still making it the fastest pnp device around. It won't be long, however, before this process receives challenges from an additional pair of bonded-wafer-based processes (ELECTRONIC DESIGN, *Dec. 19, 1991, p. 35)*.

Analog Devices announced what it calls XFCB-1 process. Like their CB-JI process mentioned earlier, the designers of XFCB-1 went for the best pnp transistor they could get and let the npn device take care of itself. The f_t of the pnp transistor runs 3.1 GHz, and its β-V_A product is 1500. The f_t of the npn transistor is 4.5 GHz and the β-V_A product is 5800 *(AB, Fig. 1)*. Products are expected from the process later this year. From a process point of view, it will be interesting to compare the op amps, comparators, and other devices coming from these two quite similar processes. Unlike digital ICs, as in the past, it will be the analog-IC-circuit designers with their bags of tricks who will determine which ICs become "top guns."

Make Or Buy

Although the first with products, Harris and Analog Devices aren't the only aficionados of bonded wafers. Motorola Semiconductor, in a joint venture with Unitrode, is eying bonded wafers in the laboratory, and Unitrode expects to have products by mid-year. Another company is in the "thinking-about-it" stage. Like Harris, Motorola is building its own wafers while Analog Devices buys them from Shinetsu Electric of Japan. This can be considered "natural" for both Harris and Motorola. Harris makes its own DI wafers now, and Motorola, one of the few major U.S. semiconductor companies, isn't totally at the mercy of off-shore wafer suppliers. By pulling the basic silicon boules, then slicing, grinding, and polishing the wafers, Motorola manufactures about 25% of its total wafer needs. In addition, Motorola and Unitrode, like Harris, are interested in the technology for power



HIGH-SPEED ANALOG NPN-ONLY BIPOLAR AND BICMOS AND CB-CMOS PROCESSES

Code	Company	Process type	Voltage	Geometry	Product Status
BA	Analog Devices	JIbiCMOS	10 V	1.6 μm	Now
BB	Analog Devices	JIbiCMOS	10 V	1 μm	In development
BC	Analog Devices	JIbiCMOS	5 V	0.5 μm	In development
BD	AT&T	JIbiCMOS	5 V	0.8 μm	Now
BE	Harris Semiconductor	JIbiCMOS	10 V	1 μm	Now
BF	Raytheon Semiconductor	JIbiCMOS	5 V	0.8 μm	1992
BG	National Semiconductor	JIbiCMOS	12 V	2 μm	1992
BH	Texas Instruments	JIbiCMOS	20 V	2 μm	Now
BI	Texas Instruments	JIbiCMOS	12 V	2 μm	Now
BJ	Texas Instruments	JIbiCMOS	30 V	2 μm	Now
BK	Micro Linear	JIbiCMOS	5 V	1.5 μm	1992
BL	Optimum	JIbiCMOS	15 V	1.5 μm	Now
BM	Optimum	JIbiCMOS	5 V	0.7 μm	1992
BN	Signetics	JIbiCMOS	5 V	0.8 μm	Now
BO	Signetics	JIbiCMOS	5 V	0.7 μm	In development
BP	Silicon Systems	JIbiCMOS	5 V	1 μm	Now
AK	Exar	CBJI-CMOS	5 V	----	Now
AL	Exar	CBJI-CMOS	18 V	----	Now
AP	Tektronix	npn-only JI	5 V	----	In development
AT	GEC Plessey	npn-only JI	5 V	----	Now
AU	Silicon Systems	npn-only JI	12 V	----	Now

CB = complementary bipolar
JI = junction isolation
DI = conventional dielectric isolation

2. Bipolar and biCMOS semiconductor processes compete with each other for the fabrication of high-volume analog and mixed-signal ICs. Their primary figures of merit, f_t and the product of current gain β and Early voltage, V_A, are plotted against each other to permit comparison. Each data point displays the transistor's voltage rating, and the gate length of the MOS transistor (if biCMOS).

and high-voltage ICs, as well as analog chips.

Though Motorola hasn't made the firm decision to go to bonded wafers, they've achieved the highest f_t in the technology. A test chip for a 5-V process sports a blazing 16-GHz npn transistor with a β-V_A product of 3000 *(AG, Fig. 1)*. However, the f_t of the pnp transistor is just 4 GHz, albeit offering a β-V_A product of 2400. Motorola feels that it can raise these f_ts to 22 and 6 GHz, respectively, while remaining at 5 V.

Wafer bonding may be the wave of the future, but conventional DI will have staying power. Elantec has a new 15-V process being developed on DI that's expected to provide an npn transistor with an f_t of 3.5 GHz, while that of its pnp cohort will be 2.5 GHz *(AI, Fig. 1)*. The β-V_A products are expected to be 3000 for the npn transistors, and 2250 for the pnp transistors.

That's no reason to give up on JI, though. AT&T is announcing products on its CBIC-V process, a 5-V process providing npn and pnp transistors with f_ts of 10.2 and 4.3 GHz, respectively *(AD, Fig. 1)*. But with a β-V_A product of only 440 for both npns and pnps, like its 13-V CBIC-U predecessor process *(AC, Fig. 1)*, it will offer IC designers a challenge. However, many of the low-voltage, ultra-fast op amps available today, like those from Comlinear, are built on the CBIC-U process. This only proves that there are at least a handful of IC designers around who know how to design wideband, fast op amps with limited β-V_A products.

The CBIC-U process itself is being challenged by ICs from Maxim, whose designers are designing products on the VLSI Technology process *(AO, Fig. 1)*. Moreover, it will soon see additional competition from an upcoming Raytheon process *(AH, Fig. 1)*.

National Semiconductor's VIP-III process, currently in development, is another interesting JI process to watch *(AS, Fig. 1)*. The company is convinced from its success with the earlier VIP-I and VIP-II processes *(AQ and AR, Fig. 1)* that analog system designers want to keep their sacred $\pm$15-V supply rails, at least for a while. But those designers want speed and bandwidth, too. Therefore, the VIP-III process will wind up as the fastest 30-V (JI or DI) process available or proposed. Moreover, the ratio of npn and pnp f_ts runs less than 2:1—2.7 and 1.5 GHz, respectively. And with the high supply voltages come β-V_A products of 15,000 and 3000 for the npn and pnp transistors, respectively.

In applications that don't demand the blinding speed of newer processes, virtually all of these processes offer IC designers a pair of additional and more subtle advantages over existing high-speed processes—a superior speed-power product and greater packing density. That is, these processes can build replacements for today's fast op amps, comparators, and other linear functions that draw an order-of-magnitude less current and operate on lower supply voltages. These advantages, always critical in the digital IC world, are becoming significant for analog and mixed-signal ICs for several common reasons. Many of the new applications run off batteries, and many are mixed-signal ICs with significant amounts of logic. While finer-line lithography has never cut op-amp or comparator size by much because low-noise-input and current-handling output transistors are physically large, it can reduce the size of the digital devices. National's VIP-III process is aimed at these applications.

Wafer bonding may be the wave of the future, but conventional DI will have staying power.

The goal of TI's Excalibur-II process *(AM, Fig. 1)* is to lower the power required by existing general-purpose low-frequency applications. Typical examples include low-power voice-band telecommunications ICs and precision references. While its fgfints are limited, the β-V_A product of both npn and pnp transistors exceeds 15,000. Moreover, while its ICs are rated for 40-V operation, high yields can be obtained to over 60 V. Their faster, upcoming Excalibur-III process *(AN, Fig. 1)*, which will build ICs that can operate comfortably at 36 V, typically handle 60 V.

But TI won't guarantee operation at the higher voltages. Why not? Driven by the computer, consumer, and automotive industry's demand for "quality," TI like the other major broad-based IC suppliers, holds all products to 6-sigma quality. That is, only one IC in about a million will not meet all of its guaranteed data-sheet specification. Obviously, that's mandatory for digital ICs, and high-side switches for cars and other high-volume consumer applications. However, many low-volume users may be willing to take the chance of getting one out-of-specification device in every 10,000 (or even every 1000), and they will also pay more for a tighter-specified device. Smaller-niche suppliers don't hold their designers and product managers to a 6-sigma quality level. For example, monolithic op amps with different grades offering offset voltage spreads of ten to one are readily available.

A large percentage of these CB processes also offer a JFET transistor, a true indication that these are *analog* technologies. In earlier, non-complementary processes, the JFET played a dual role. It supplied low-bias-current inputs and usually a p-channel FET that

upped the slew rate by taking the place of a fast pnp transistor in the signal path. While the FETs in these complementary processes need not play a role beyond the input circuits, their speeds won't be limited. The FET in the Harris Semiconductor UHF-1 process sports an f_t of 4 GHz.

For the most part, amplifiers built with these FETs won't require ultra-low bias currents, because source impedances will be low due to the high frequencies involved. Nevertheless, they are targeted at such major tasks as: high-speed integrators, current-to-voltage converters at the output of high-speed digital-to-analog converters, sensing the current from fast photodiodes, buffering the storage capacitor in high-speed sampling amplifiers, and fast analog switches when MOSFETs aren't available.

Of all the advanced CB processes, Exar's XRBICMOS modular technology *(AK and AL, Fig. 1)* in many ways presents the clearest window to the future (ELECTRONIC DESIGN, *Aug. 22, 1991 p. 29)*. It offers speed and precision (npn f_ts reach 4 GHz and β-V_A products reach 8000). In addition, this truly modular, mixed-signal process furnishes 2-μm CMOS for dense logic, CMOS transistors rated at more than 75 V, and polysilicon-oxide-polysilicon capacitors for switched-capacitor circuits. The modularity also permits designing for operation from either 18- or 5-V rails, with the latter providing both higher speed and the ability to work down to 1 V. The key to the process, though, may be its EEPROM module that permits trimming the analog circuits and programming their digital equivalents. One of the beta sites for the process builds hearing aids. The complete hearing aid is put on one chip, marking the first time digital filtering was used in this venue. The filter, a digital-signal processor, is user- and/or doctor-programmable in real time. And it runs off a supply of just 1 V.

Exar's foresight in adding CMOS to a CB process is amplified by the fact that virtually every designer working on a CB process indicated to this writer that CMOS will be added within two to five years. Similarly, nearly all of the advanced biCMOS process designers interviewed indicated that a vertical pnp transistor was on the list of additions to their processes, within similar time frames.

What else can you expect out of these complex technologies in the next few years? One interesting development involves data-converter applications. To date, high-speed data converters, whether DACs or ADCs, haven't required fast vertical pnp transistors. Until recently, all-npn-type bipolar processes have done the job, and now biCMOS processes are joining that fray. On the other hand, CB processes have been limited to purely linear circuits, such as amplifiers.

CB processes will branch out in other directions offering higher rather than lower voltage ratings.

As the demands for ever more functions on one chip continue, an IC designer using a CB process, and driven by a customer, will eventually put the signal conditioning on the same chip as a flash or multistep ADC. At that time, it will be interesting to see if that innovative designer will find a use for the high-speed pnp transistor to increase circuit performance, simplify the design, or cut the power needed by the converter. Initially, ICs like the npn-only converters will use current-mode logic (CML) on chip, and interface to the digital world with ECL. It will be intriguing if the fast pnp transistors can also aid the logic-circuit designer.

Furthermore, CB processes will branch out in another direction. Versions will be developed with higher, rather than lower, voltage ratings. Driving the RGB inputs of a CRT with video represents at least one place where these ICs are needed. While raising the voltage rating to 60 V or more will sacrifice some f_t (say, dropping it from 3 or 4 GHz down to 1 GHz), the output device can be a little slower if all of the other transistors in the circuit are fast enough. Essentially, these higher-voltage transistors will be on the same chip as the faster, low-voltage devices.

Analog-IC designers have long survived and triumphed without fast vertical pnp transistors. As a result, several companies have leveraged their analog-IC-circuit design expertise by developing high-speed, npn-only, analog-IC processes from slower similar technologies. These include National Semiconductor, Silicon Systems, Tektronix, and TRW, among others. AT&T, on the other hand, has adapted an ECL process for the same purpose *(Fig. 1, again)*.

Plots of f_t versus β-V_A for npn-only bipolar processes are also compared against those for npn-only analog biCMOS processes *(Fig. 2)*. Moreover, the figure contains the Exar CB-biCMOS process and a vertical line indicating the f_t of the fastest CB npn transistors. In addition to the operating voltage, each data point lists the effective gate length of the CMOS devices.

Along with the latest biCMOS technologies from Signetics and Silicon Systems, the advanced npn-only technologies represent the fastest merchant-market, analog-IC processes available today. Moreover, with the exception of the 16-GHz npns on the experimental Motorola process, it appears that future npn-only bipolar and biCMOS technologies will

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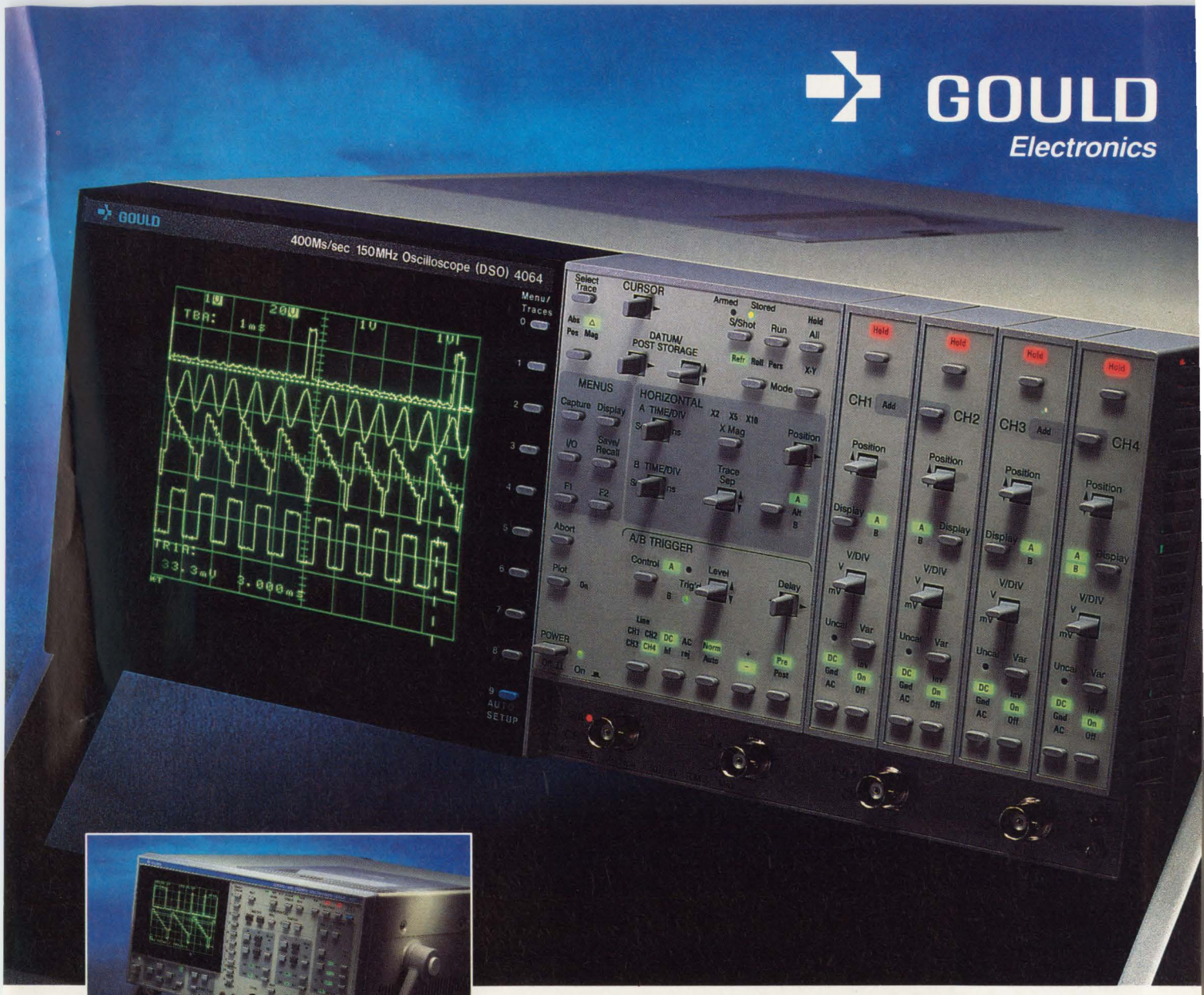

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continue to lead CB processes in speed.

These advanced, and future, *analog* biCMOS processes represent several development paths. But most add digital CMOS to either an ECL process or to an analog bipolar process. It's these npn-only (including biCMOS) processes from GEC Plessey, Tektronix, Silicon Systems, Raytheon, Optimum, and AT&T, with f_ts above 4 GHz, that aim at the RF applications mentioned earlier. Adding high-speed, dense, CMOS logic lends these technologies to ICs that were just recently considered members of the RF genre. These include 12-bit, 100-MHz DACs for direct-digital frequency synthesis, and 12-bit 20-MHz ADCs for IF down-conversion in lieu of heterodyning. As mentioned earlier, today's data converters don't need fast pnps. Consequently, they're not required at all. In addition, even in pure linear circuits, most RF applications are handling small ac signals (typically less than 1 V rms), which are usually ac-coupled. Therefore, dc response is unnecessary and fast pnps aren't needed for level shifting in the signal path. Present use of converters in these applications represents the tip of a pure-technology-driven iceberg.

Power Modules

While most of the biCMOS processes are modular, not all of them offer dazzling speed. Many jobs still exist for general-purpose analog and mixed-signal ICs. TI's modular, 2-μm LinBiCMOS process *(BH, BI, and BJ, Fig. 2)* is a good example. The three npns shown, featuring different operating voltages and f_ts, can all be built on the same chip. The process also offers metal-oxide-metal capacitors for switched-capacitor circuits. Future modules will include higher voltages for the MOS devices (up to 50 V), and even power DMOSFETs that can handle 45 to 60 V and 2 to 10 A. The process might also include EEPROMs to be used for trimming, and eventually a vertical pnp transistor.

Until recently, power and high-voltage processes have basically stood alone on the outside of the mainstream analog, mixed-signal, or digital process. However, as indicated by TI's future outlook, that may be changing. Further indication can be seen by last year's 68HC05 microcontroller from Motorola Semiconductor that sported eight DMOSFETs, each rated at 6 V and 300 mA. Motorola's goal is to get the voltage rating of the FETs to a level of at least 30 V.

Other suppliers of these power-control ICs see operating voltages moving from 400 to 800 V, and ultimately to 1200 V. Thus, high-side drivers would control 1200-V MOSFETs and insulated-gate bipolar transistors (IGBTs) running off the rectified 440-V, three-phase ac-power line in the U.S. Access to bonded wafers becomes almost mandatory for such devices. Similar, and even higher, isolation voltages are needed for automotive ignition jobs. Bonded wafers will also experience activity in high-voltage telecommunications applications, such as subscriber-line interface circuits (SLICs) where 200 V of isolation is required.

Bonded wafers bring superior voltage isolation to high-voltage IC processes and they permit the use of IGBTs in an IC.

Bonded wafers bring superior voltage isolation to high-voltage IC processes, and they permit the use of IGBTs in an IC. This has been virtually impossible on today's JI processes, regardless of voltage rating, because when the IGBT turns on, it floods the rest of the die with minority carriers. This turns on all of the other devices, which isn't exactly a happy thought. Putting the IGBTs in oxide-isolated islands eliminates this disease.

Though it's here to stay for low-voltage ICs, bonded-wafer technology still has some problems to solve when it comes to incorporating high-voltage transistors (as distinct from high-voltage isolation of low-voltage transistors). Trench etching must be accelerated. After bonding, the wafers for building ICs are thinned by lapping. The lower the voltage rating and the higher the operating frequency of the transistors, the thinner the wafer. For example, Harris thins the UHF-1 wafers to under 10-μm thick, more than enough to stand off 12 V. However, silicon on the order of 30-μm thick is needed to stand off 200 V, and even thicker silicon will be required at 500 and 1000 V. The anisotropic etching techniques used to dig the trenches were borrowed from dynamic-RAM technology, and are more than fast enough for the "shallow" trenches. But they must also be accelerated as voltages climb.

Not all power ICs need to work at hundreds of volts, or even at tens of volts. In fact, high-volume, portable, consumer products, such as camcorders, cameras, and CD players, all require motor-control ICs working efficiently between 4.5 and 9 V. The need for "power management" in laptop, notebook, palmtop, and smaller computers means a need for efficient power ICs in this voltage range and even lower. Siliconix and others are attempting to increase the efficiency of the low-voltage DMOS switches in these ICs, and are even considering a move to CMOS.

As noted earlier, using low-voltage, fine-line, mainstream digital CMOS processes for analog ICs started in the 1980s. It works well for high-resolution (12 bits and up) ADCs us-

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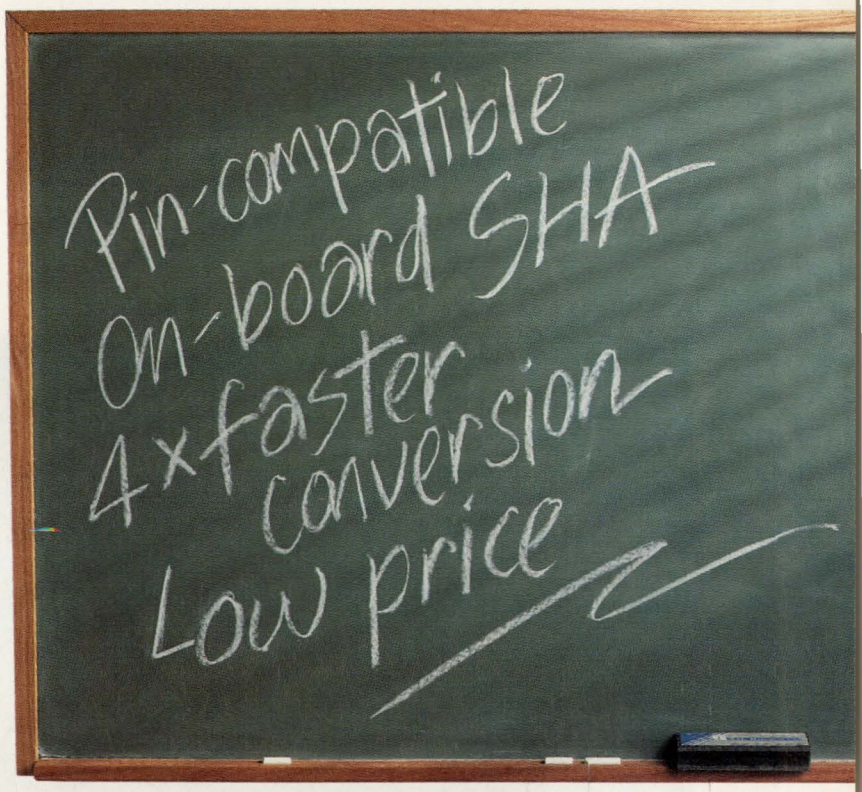

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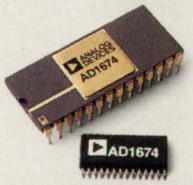

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ing switched-capacitor techniques, and is a natural for 16-bit-and-up delta-sigma ADCs which have 99%-digital circuitry. In both applications, the high packing density significantly cuts die size. Some companies use raw digital processes (particularly if fab-less), while others like TI and NCR add a high-quality capacitor module. However, the major application for digital CMOS will be for 8- and 10-bit RAMDACs and flash and multistep ADCs with large amounts of additional digital circuitry surrounding them. The DACs will go into high-definition TVs (HDTVs), while the ADCs will go into imaging systems.

With many analog ICs wending their way into mainstream digital CMOS processes, major efforts will be made to follow digital ICs toward finer and finer line-width lithography. There were skeptics who said that analog CMOS circuits wouldn't work below 2 μm. The same message got louder for 1 μm, and it still rages on today, yet available CMOS transistors have proven this message wrong. NCR has comparators working on 0.7-μm CMOS and expects to follow their digital-circuits migration to 0.5 μm. So far, the finer-geometry analog circuits have both sped up and improved. For example, offset voltages drop because even though transistor size remains constant for analog circuits, finer-line lithography processes improve device matching.

Coming full circle, many experts now say that as digital CMOS drops below 0.5 μm, SOI will improve performance by eliminating parasitic bipolar transistors and by reducing ac parasitics, and that at some gate length (0.1 to 0.3 μm), SOI will be mandatory. A full session at last month's IEDM was devoted to this technology, testifying to its importance, which should facilitate analog circuits migrating to ultra-fine-line lithography.

For some applications, metal-gate CMOS is the best way to go, particularly if you already have a fully-paid-for fab. And Teledyne Components thinks it can be improved. The company, a leader in applying the process to analog ICs, such as chopper-stabilized amplifiers, integrating ADCs, and power MOSFET drivers, expects to reduce gate lengths, which in turn will raise speeds and cut die size. All other things being equal, metal-gate CMOS offers about 1/5 the noise of silicon-gate CMOS and an order-o-magnitude lower propagation delay due to lower sheet resistance.□

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CIRCLE 159 FOR U.S. RESPONSE
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THE WORLD OF COMMUNICATIONS IS MOVING TO FIBER OPTICS

ELECTRONS TEAMED WITH PHOTONS PRODUCE STUNNING THROUGHPUTS.

BY MILT LEONARD

Although copper-wire networks have made impressive strides in communications technology, the genre's technology of the future is clearly fiber-optic networks. In addition to its inherent advantages of wider bandwidth, lower losses, and immunity to electromagnetic interference, optical-fiber media has the potential to offer unlimited network capacity. With the promise of optical-fiber media well in sight, R&D facilities around the world are intensifying efforts to develop advanced optoelectronic components devices to meet fiber's potential *(Fig. 1)*.

At Telecom 91, Dr. Robert W. Lucky, executive director of AT&T Bell Laboratories, Holmdel, N.J., identified the characteristics of optical fiber that have propelled the technology into dominance in today's long-distant plant. Optical fibers are remarkably error-free, with typical error rates of about one in 100 billion. They also offer tremendous economy of scale in long-distance transmission, whose cost continues to drop as capacity increases, resulting in an exponential increase in bandwidth per unit cost.

Data-transmission rate over a single fiber has grown annually at nearly 100% over the last two decades, Lucky says. The SONET standard transmission rate is about 2.5 Gbits/s, and will likely be 10 Gbits/s in the near future. Experimental systems have exhibited 32-Gbit/s rates—the equivalent of a half-million digitized voice channels on one fiber.

Experts generally attribute escalating data rates primarily to advances in laser technology. State-of-the-art lasers that convert electronic signals into light pulses for communication over fiber can now produce well-defined light pulses that have durations of less than a nanosecond. Improved lasers that emit light of "rock-steady" wavelengths will usher in the age of coherent optical transmission, which sends different data simultaneously on different wavelengths through the same single fiber. While current communications systems transmit only unitary information, coherent optical transmission opens the way to multiplexed transmissions.

Monochromatic laser light is generated by stimulated emission. When certain atoms or molecules are excited by photons of a particular frequency, they emit photons identical in frequency and phase to the incident photons. Monochromatic light is produced when the process is repeated by trapping these photons between two mirrors.

Most networks presently drive lightwave signals along the fiber with semiconductor lasers that are directly modulated with signal current. Although continuing research aims at enhancing the frequency response of direct-modulation lasers, further increases in switching frequency are expected to be minimal. That's because the technology is approaching its theoretical speed limits.

Another problem with this type of laser is spectral purity, which determines lightwave-signal transmission distance on an optical fiber. The chromatic dispersion of an optical fiber and the relatively large frequency chirp of a directly modulated semiconductor laser limits transmission distance. This condition calls for closely spaced signal regenerators along the transmission line.

One possible solution under investigation at AT&T Bell Laboratories, Murray Hill, N.J., is the monolithic, colliding-pulse mode-locked (CPM) semiconductor laser. Unlike direct-modulation lasers, this device operates continuously and has generated a pulse train at over 350 billion pulses per second under laboratory conditions.

High switching speed results from circulating two pulses in the laser cavity at the same time. Pulse duration is shortened when

the pulses collide and interact in the center of the cavity. Using quantum wells enables the optical phases of the various oscillating frequencies to lock together, which generates clean, transform-limited pulses with durations of under 10^{-12} seconds. With a high spectral purity, the laser can support more data channels for any network bandwidth.

The laser also makes it possible to use soliton pulse transmission in optical fiber, which requires pulses of high spectral purity that have specific shape and amplitude *(see "What's a soliton?," p. 76)*. The CPM laser has yet to advance beyond the stage of a laboratory research tool. For practical application, modulators, photodetectors, and receiver circuits must be developed that can support its switching speed.

1. Error-free transmission of lightwave signals has been demonstrated at AT&T Bell Laboratories at 10 Gbits/s over a 2000-km optical fiber. The system regenerates the signal with amplifiers consisting of spliced-in segments of erbium-doped fiber, instead of electronic regenerators used in existing long-haul lightwave transmission systems. Using this technology, AT&T and Kokusai Denshin Denwa of Japan will construct the world's first optically amplified trans-Pacific undersea system in 1995.

Impurity-induced disordering of multiquantum-well (MQW) processing is an attractive technique for fabricating lasers and other planar optoelectronic ICs. Although lasers made with MQW processing of gallium-arsenide/aluminum-gallium-arsenide (GaAs/AlGaAs) or indium-gallium-phosphide/aluminum-gallium-indium-phosphide (InGaP/AlGaInP) devices have been developed, lattice mismatching in the various device layers has restricted the output to short wavelengths. To obtain longer wavelengths for fiber applications, scientists at the Optoelectronic and Microwave Devices Laboratory of Mitsubishi Electric Corp., Hyogo, Japan, are investigating InGaAsP/InP as an alternative material for an MQW laser design. The structure's active region has zinc-diffusion-induced disordered regions on both sides for carrier confinement, and effectively performs as an embedded optical wave guide *(Fig. 2)*. The laser works at room temperature and produces wavelengths from 1.3 to 1.6 μm.

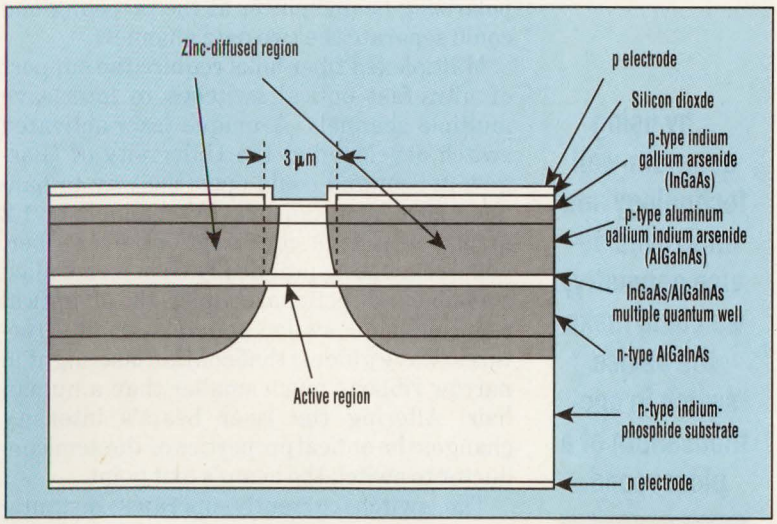
Characterizing the performance of fiber-optic devices or systems for data-communications applications requires the use of a tunable continuous-wave (CW) laser that produces wavelengths in the near-infrared region of the electromagnetic spectrum around 1.3 μm. This is the wavelength at which many optical fibers used in data communications operate with the least distortion. According to a published report by researchers at Cornell University's College of Engineering, Ithaca, N.Y., no such 1.3-μm source is currently available. However, work at Cornell may soon lead to a source of this caliber.

Color-center lasers are tunable for wavelengths spanning 1.45 to 3.9 μm. For wavelengths shorter than 1.1 μm, a number of systems are available, including the dye laser and a more-recently developed solid-state laser based on titanium-doped sapphire, which provides useful power over the tunable range of 0.7 to 1.1 μm. But no powerful source has been tunable between 1.1 and 1.4 μm.

Cornell's experimental setup includes a solid-state lasing material called the gain medium, a pump beam to supply energy to the medium, two lenses to focus the laser radiation, two mirrors to reflect the light back and forth through the medium, and a prism to disperse the emitted light and allow the laser to be tuned to a specific wavelength *(Fig. 3)*.

This work is based on the use of forsterite as the gain medium. Forsterite is a naturally occurring mineral composed of magnesium, silicon, and oxygen atoms, with trace amounts of metallic impurities, such as chromium and iron. The mineral is part of the olivine family of minerals, which form a major part of the earth's mantle. Experiments show that forsterite enables a laser to be tuned from 1.2 to 1.32 μm—very close to the desired range—with almost 2 W of CW output power.

"We think that we can make this laser even better," says Clifford Pollock, an associate professor at Cornell's School of Electrical Engineering. The presently used forsterite crystal exhibits unwanted absorption at the longer wavelengths, which increases overall loss of laser light between the two mirrors. This results in reduced power, efficiency, and tuning range. "We suspect that the tuning range



2. An experimental MQW laser from Mitsubishi, fabricated by a Zn-diffusion-induced disordering process, operates at room temperature and can produce wavelengths from 1.3 to 1.6 μm. The MQW layer sandwiched between the AlGaInAs layers acts like a waveguide in the active region.

for an optimized crystal could extend up to 1.4 μm and the overall power output could nearly double," Pollock adds. Although few applications require this much power, improved efficiency would mean less required pump power for current performance levels. Related work at Cornell involves synthesizing and growing single crystals of forsterite, which opens up a wide range of other application possibilities. For example, thin films of single-crystal forsterite grown on a substrate would enable the construction of integrated optical circuits based on tunable light sources for use in sensors, optical amplifiers, and instrumentation. With further processing refinements, researchers feel it may be possible to process large areas of substrate material to create laser arrays and signal-processing optics.

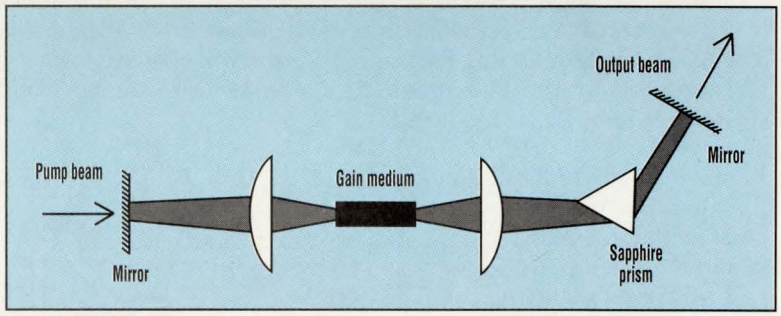
In another industry first, scientists at AT&T Bell Laboratories, Murray Hill, N.J., have made what is reportedly the world's smallest semiconductor laser. The device resembles a microscopic thumbtack with a 5-μm-diameter head that's 400-atoms thick, and is attached to the semiconductor substrate by a thin post. At least 10,000 of the lasers can fit on the head of a pin. Photons travel around the edge of the laser, which can be used either as a surface-emitting or side-emitting device.

The microdisc laser consists of layers of InGaAs sandwiched between layers of InGaAsP, using metal-organic chemical-vapor-deposition (MOCVD) and microlithographic processing. Richard Slusher, head of Bell Laboratories Optical Physics Research department, says the development is part of a research program directed toward future switching and computing technology.

Scientists at the IBM Thomas J. Watson Research Center, Yorktown Heights, N.Y., have developed a lateral p-i-n photodetector that has an 18.0-GHz bandwidth for the 1.3-μm wavelength used for fiber-optic transmission. With 3- to 5-V bias voltage (compatible with the supply voltages of digital circuits), the extracted bandwidth exceeds 5 GHz. The GaInAs structure is compatible with heterostructure-based FET technologies.

Another technology that promises to significantly impact optical transmission systems are the recently invented rare-earth amplifiers. Unlike conventional regenerators used to receive, amplify, and retransmit lightwave signals, erbium amplifiers don't need to be changed to accommodate new wavelengths added to the system. They can amplify an optical signal across a broad band of wavelengths, regardless of signal modulation. Typically consisting of sections of fiber doped with erbium-in-lanthanide, they're spliced into the main cable at intervals exceeding 300 km *(Fig. 4)*. Operating with a laser pump source, they can amplify an optical signal by a factor of up to 1000 without converting it to an electrical signal, which must be done with conventional repeaters.

Intense research activity in laser technology continues to find ways to produce faster devices with clean output spectra. If the technology does run out of gas, future increases in transmission speed are expected to come from wavelength-division multiplexing (WDM), which transmits multiple wavelengths simultaneously on the same fiber, with each wavelength constituting a different data channel. Conceivably, a fiber could support a thousand 1-Gbit/s signals. To date,



3. A tunable laser being developed by Cornell University scientists uses a forsterite gain medium to produce wavelengths from 1.2 to 1.32 μm. This capability is useful to characterize the performance of fiber-optic components and systems for data-communications applications. Further improvements in the medium could extend the tuning range up to 1.4 μm.

only one-tenth of one percent of the available fiber bandwidth is being used.

Because solitons of different channels with different velocities can pass through each other without permanent effect, the WDM technique has the potential to increase the capacity of a soliton-transmission system significantly. The only result of soliton collision is a mutual and negligible displacement in time. In a practical system, collision length—the distance two solitons travel down a fiber while passing through each other—must be

at least twice as long as the amplifier spacing to avoid large shifts in pulse arrival time. Theoretically, WDM could allow one fiber to carry up to five 5-Gbit/s channels spaced 0.25-nm apart for a total span of just 1 nm. But until the problem of precisely equalizing the amplifier gains of that many channels is solved, the first practical system will more likely have just two channels spaced about 0.2 nm apart.

An alternative multiplexing technique for lightwave signals is phase-division multiplexing (PDM). Using PDM with soliton signals can double the single-channel bit rate with only a modest cost increase over the WDM method for end-station hardware. In PDM, the output of a mode-locked laser would be split into two equal parts, with each part electro-optically modulated with a stream. The beams would then be recombined so that the pulses of one stream are orthogonal to those of the other and interleaved in time. Electronically controlled wave plates at the receiving end would compensate for any effects of changing fiber birefringence on the polarization. (Birefringence is the difference in longitudinal and lateral indices of refraction that's created by the fabrication process for optical fiber. The result is the separation of a light beam into two diverging beams.) Finally, a polarizing beam splitter at the receiving end could separate the two data channels.

...by using quantum-well technology and imprroved device geometry, we could make the device switch in one-thousandth of a picosecond.

Multiplexed fiber links require the support of ultra-fast optical switches to interleave multiple channels. A unique laser-activated switch developed at the University of Glasgow in Scotland could open the way to handling 2000 simultaneous TV channels or 1.2 million telephone conversations over fiber, while consuming practically no power. Called a nonlinear directional coupler, the all-optical semiconductor switch contains small structures (wave guides) that confine laser light in narrow ribbons much smaller than a human hair. Altering the laser beam's intensity changes the optical properties of the semiconductor to switch the beam's exit point.

The switch currently operates instantaneously with 10-ps light pulses. "But by using quantum-well technology and improved device geometry, we could make the device switch in one-thousandth of a picosecond," says Dr. Stuart Aitchison, researcher at the University of Glasgow. Such performance would have profound implications on time-division multiplexing techniques.

Researchers are also investigating other forms of lightwave transmission. One possible alternative to solitons is to transmit ordi-

WHAT'S A SOLITON?

Standing alongside a local barge canal in 1834, John Scott Russell, a Scottish shipbuilder and engineer, observed a solitary wave moving across the water's surface. The wave seemed to travel as far as he could see without losing its shape. Intrigued by the phenomenon, Russell jumped on his horse, as the story goes, and followed the wave for several miles along the canal. By the end of the century, an equation had been developed for Russell's solitary wave. In 1965, two Bell Laboratories scientists observed that solitary light waves survive collisions with one another, and thus renamed them *solitons*.

A soliton is an energy wave, or pulse, designed to retain its shape, duration, and strength as it moves through a specific medium. In a single-mode optical fiber, a soliton is immune to effects of pulse-broadening chromatic dispersion, and to the frequency-broadening effects of light intensity. Any minimum-bandwidth pulse of reasonable shape and a peak intensity greater than a 2:1 ratio will evolve into an exact soliton as it propagates along the fiber. Experiments have shown that the soliton is robust against all known fiber and other system defects of reasonable magnitude.

The soliton can be viewed a self-trapped pulse, as depicted in the drawing showing runners on a mattress. Each runner represents a finite wavelength within a pulse of high-intensity light. This creates a moving "valley" of higher dielectric-constant fiber material. The moving valley pulls along slower runners while retarding the faster ones to maintain the original pulse shape as valley propagates along the fiber.

In 1973, Akira Hasegawa of AT&T's Bell Laboratories Electromagnetic Phenomena Research Dept. suggested that a pulse of photons could exist in optical fibers, just as Russell's soliton existed in water. He also proposed the idea of a soliton-based transmission system. However, no transmission medium is perfect, and a soliton in optical fiber needs an energy boost to retain its original shape and energy level while traveling long distances. For soliton transmission through an optical fiber, this boost is provided by a separate "pump" laser.

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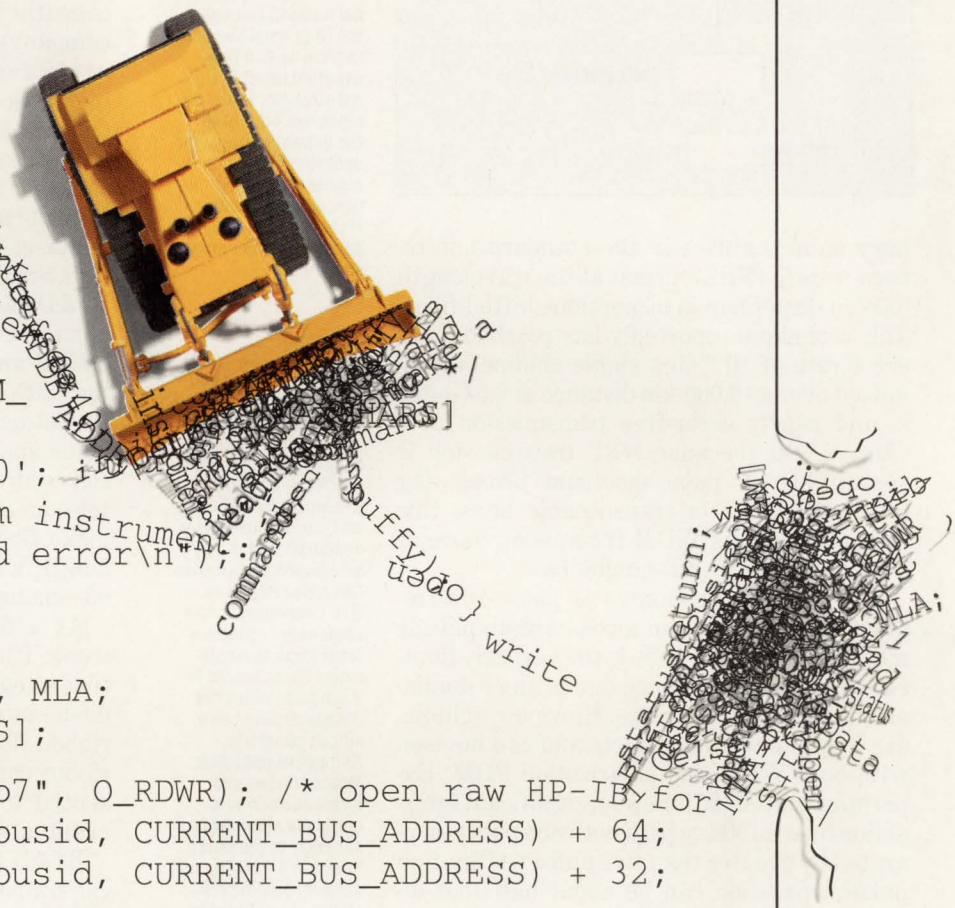
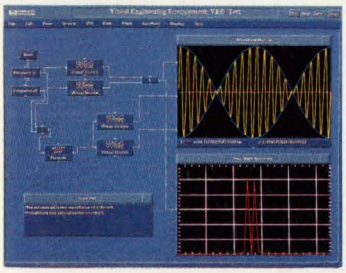


```
void service(eid)
int eid;
{ int stat, byte;
/*serial poll instrument*/
byte=hpib_spoll(eid);
if ( (byte<0)||! (b
    printf("SRQ Prob
   return; }
stat=my_read(eid, DVM_
if (stat>0) {
    buffy[stat] = '\0'; i
    printf("Data from instrument:
else printf("I/O read error\n");
return; }

main() {
int busid, stat, MTA, MLA;
char command[MAXCHARS];

busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB for
MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
stat = BUTTON_BIT ;
sprintf(command, "KM%02o", stat); /* 2 octal digits */
```



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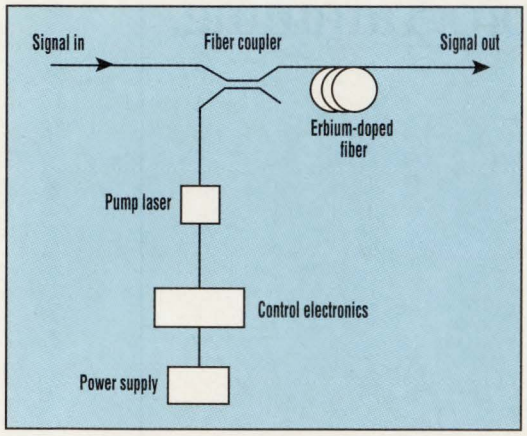


4. Rare-earth-doped amplifiers can boost lightwave signal strength in fiber cables across a broad range of wavelengths. The atoms of a rare-earth dopant in a spliced-in length of fiber are excited by a pump laser. Thus, a lightwave signal passing through the fiber amplifier can receive up to a thousandfold boost in signal strength. Initial designs use erbium as the dopant material for optimum fiber-communication wavelengths. Other dopants under investigation include neodymium and praesodymium.

nary square pulses in the standard non-return-to-zero (NRZ) format at the wavelength of zero dispersion in dispersion-shifted fiber. This technique reportedly has reached a bit-error rate of 10^{-10} in a single channel transmitted over a 10,000-km distance at 2.5 Gbits/s, and nearly error-free transmission at 5 Gbits/s. But because NRZ transmission is susceptible to pulse-spectrum broadening (over 100 GHz) in transoceanic lines, this method prohibits WDM from using more of the fiber's bandwidth capability.

Yet another alternative is phase- or frequency-shift keying in a constant-amplitude mode. The problem here is the severely limited transmission distance due to fiber nonlinearity and amplifier noise. However, solitons are immune to such effects and can be used with both WDM and polarization PDM. Experiments at AT&T show no significant interaction over a 100-km path between pulses separated by greater than five pulse widths, and pulse separation can be about half that allowed without multiplexing.

AT&T Bell Laboratories scientists have demonstrated an ultra-fast optical-fiber-ring LAN that uses solitons and all-optical logic gates. They say a network based on this design might handle data at 100 Gbits/s peak, making it over 1000 times faster than existing electronic systems. The gate uses soliton trapping and dragging to produce on-off signals for digital communication.

The proposed design uses four logic-gate modules at a node (information-switching point) to read the address of a data packet to verify its destination. The design is in an early stage of research on ultra-high-speed networks using all-optical devices. Researchers are now interconnecting the various parts of the nodes to form a larger switching fabric.

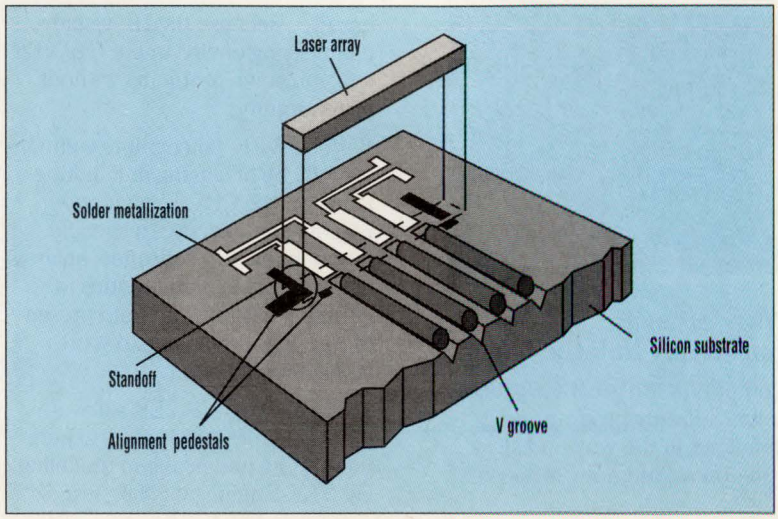
Increased use of fiber links in local-area networks (LANs) is spurring research in connectivity technology. "From the standpoint of volume in the datacom sector, we see the greatest market potential in fiber-based FDDI (fiber distributed data interface) LANs, channel-to-I/O links, and systems-interconnect application," explains Art Strube, executive vice president of BT&D, Wilmington, Del. BT&D, a venture between the Du Pont Co., Wilmington, Del., and British Telecom (the world's fourth largest telephone company), specializes in lightwave components for telecommunications networks, high-speed fiber channels, LANs and metropolitan-area networks (MANs), military communications and control systems, and digital cable-TV applications.

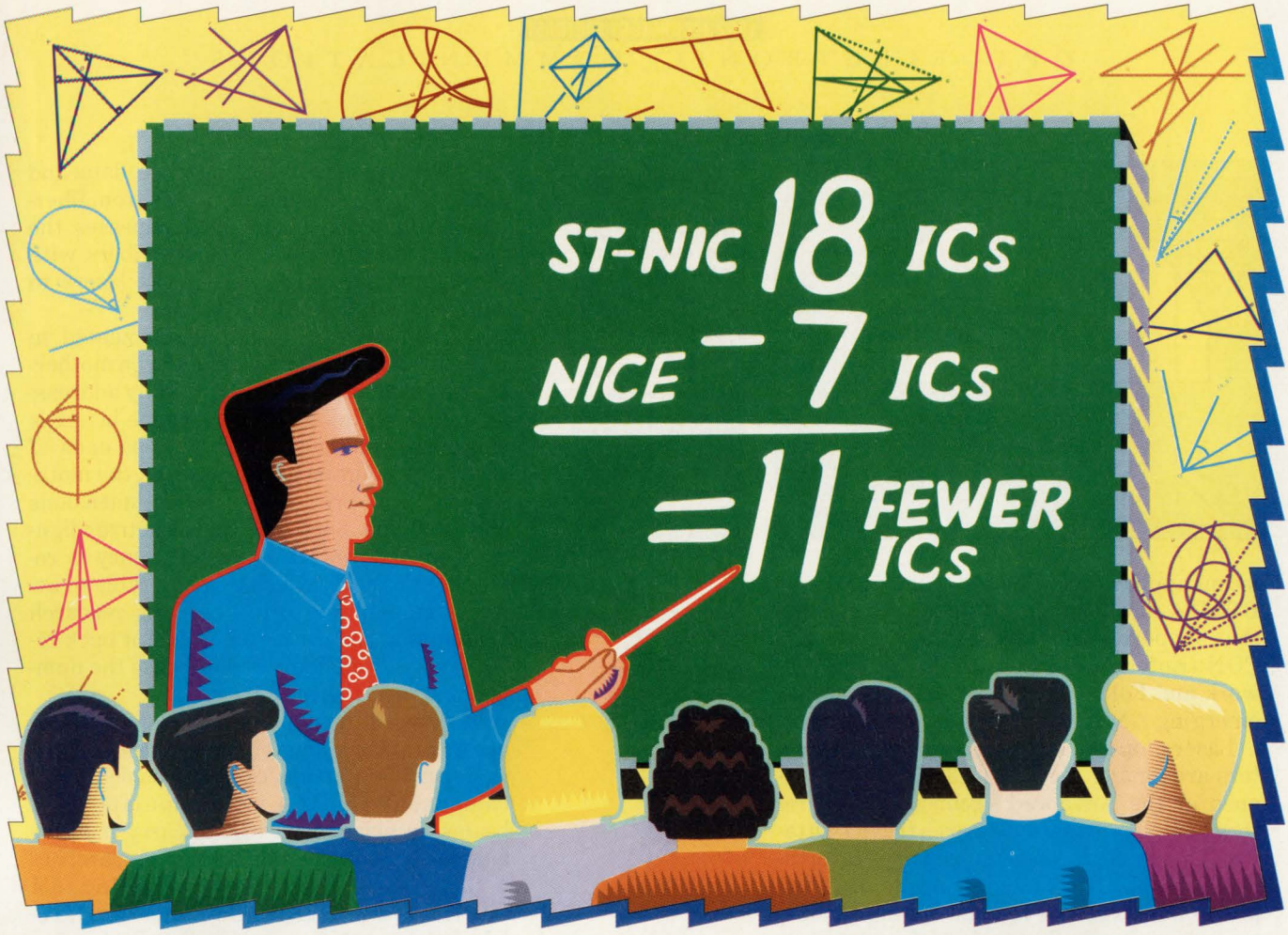
"Optical amplifiers are future key components in at least three application areas," says Strube, "datacom, telecom, and CATV." BT&D has launched a two-prong R&D development effort in this arena. Semiconductor optical amplifiers can be designed for both the 1300- and 1550-nm wavelengths, with potential use in the datacom and fiber-to-the-home applications. The erbium-doped amplifier is already used in 1500-nm long-distance telecom and CATV networks. Strube says to make fiber amplifiers at the 1300-nm wavelength, a different rare-earth dopant is needed—namely, praesodymium.

As a first step into the OEIC (optoelectronic IC) arena, BT&D is developing chips that integrate arrays of lasers with monitor diodes as well as p-i-n arrays for connection to ribbon-fiber interconnects (multiple fibers in ribbon configuration). These elements are essential to lower-cost system interconnects, eventually leading to optical backplanes.

BT&D is also developing a variety of optical transmitters and receivers for SONET and Europe's Synchronous Digital Hierarchy (SDH). The company feels SONET and SDH will dictate the standards for most future te-

5. Short-distance optical-fiber distribution to homes and businesses will require low-cost components to become practical. One way to minimize assembly and packaging costs is demonstrated in a hybrid distribution device being developed by GTE Laboratories. The component couples a laser array to single-mode fibers seated in V grooves, which are micromachined on a silicon substrate. Alignment pedestals located on the substrate surface automatically align the laser array to the fibers to within 1 μm. The resultant coupling efficiency is comparable to that obtained with costly active-alignment methods.





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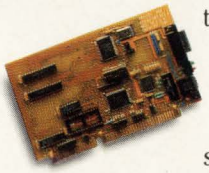

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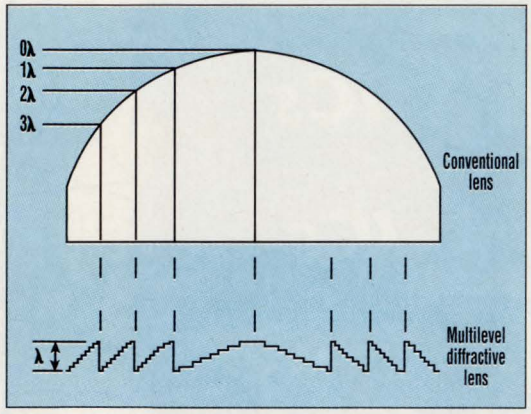

6. Binary-optics technology has the potential to become an indispensable tool for fabricating optoelectronic ICs that combine optical elements with electronic circuits on chips. By using CAD design methods and VLSI processing, the technology can produce on-chip microscopic optical elements like lenses and laser-beam multiplexers, and can even create layered structures of optics and electronic devices in parallel form. This cross section shows the binary-optic equivalent of a conventional lens, which can be arrayed in densities up to 20,000 lenses per square centimeter.

lecom applications. One other major area of BT&D's development focus is on products that support IBM's recently announced ESCON (Enterprise System Interconnect) network and Follow-on Fiber Channel (another emerging ANSI standard).

Lasers, optical amplifiers, and optodetectors are among the new OEICs being developed at the Advanced Technology Laboratory of Bell-Northern Research (BNR), Ottawa, Canada. As the R&D subsidiary of Northern Telecom, BNR is applying its MOCVD processing expertise to build up semiconductor layers on optoelectronic devices in layers as thin as a few atoms. BNR has already developed the ridge-wave-guide laser that has a median lifespan of 600 years. Current activity focuses on developing GaAs chips that operate in the 10-Gbit/s range for use in Northern Telecom's optical transmission systems.

The world's longest land-based fiber-optic cable is Northern Telecom's TubeStar system, which stretches 7000 km (4300 miles) across Canada. The $430-million system can carry 24,192 voice-equivalent channels. A backup system with different routing uses a 2.488-Gbit/s transport developed by BNR.

On a more local scale, telephone companies are expected to begin installing FITL to add 3 million access lines on fiber in 1996. By 2001, over 40 million U.S. homes will be connected to a nationwide fiber-optic subscriber-loop network. These predictions come from a market study by KMI Corp., a fiber-optics and communications consulting firm in Newport, R.I. High-capacity fiber links will allow telephone companies to offer a new range of broadband services, including video-on-demand, HDTV, and expanded cable-TV and video-phone services, the study says.

One device under development at GTE Laboratories, Waltham, Mass., looks promising for such applications. The device distributes multiple communication signals by coupling a laser array into four separate optical fibers *(Fig. 5)*. Intended for sending voice, data, and video signals over short distances from fiber-based networks to homes and businesses, the design automatically aligns the fibers with the light-emitting cavities of the lasers to within a tolerance of 1 μm.

The single-mode fibers are cemented in grooves micromachined in the silicon motherboard. An array of four individually addressable, GaAsP/InP ridge-wave-guide lasers is mounted epitaxial-side down at the ends of the fibers. Alignment pedestals on the motherboard and precise V-groove dimensions eliminate the need for costly active-alignment procedures. Coupling efficiency is reported at 6 to 7%, which is comparable to active-alignment performance. But research continues to reduce the potential for back-reflection laser damage, and increase the number of arrayed lasers.

Rockwell International Corp., AT&T, and others are examining binary-optics technology for placing arrays of microscopic optical components on ICs to manipulate light beams, in place of wiring, to carry massive amounts of information. Other researchers in this area are Texas Instruments Inc., 3M Co., Honeywell Inc., Perkin-Elmer Corp., Polaroid Corp., and General Electric Co.

"Binary optics is a diffractive optics technology that uses computer-aided design and VLSI processing techniques to fabricate optical elements," explains Dr. Edward Montamedi, Rockwell's program manager for the Microoptics Technology Dept., Thousand Oaks, Calif. Where conventional optics uses mechanical polishing to produce a curved optical surface of a specific profile, binary optics transfers a binary surface-relief pattern to a dielectric or metallic substrate by using high-resolution lithography and ion-beam etching *(Fig. 6)*.

A recent collaboration between scientists at Rockwell International's Science Center, Thousand Oaks, Calif., and the Massachusetts Institute of Technology's Lincoln Laboratory, Lexington, Mass., has produced a microlens array that will enhance the light coupling to a solid-state photomultiplier (SSPM) photon detector. The SSPM can detect individual photons. "The technology can also produce telescope optics, contact lenses, arrays of coupled laser microcavities, and laser-beam multiplexers," says Montamedi.□

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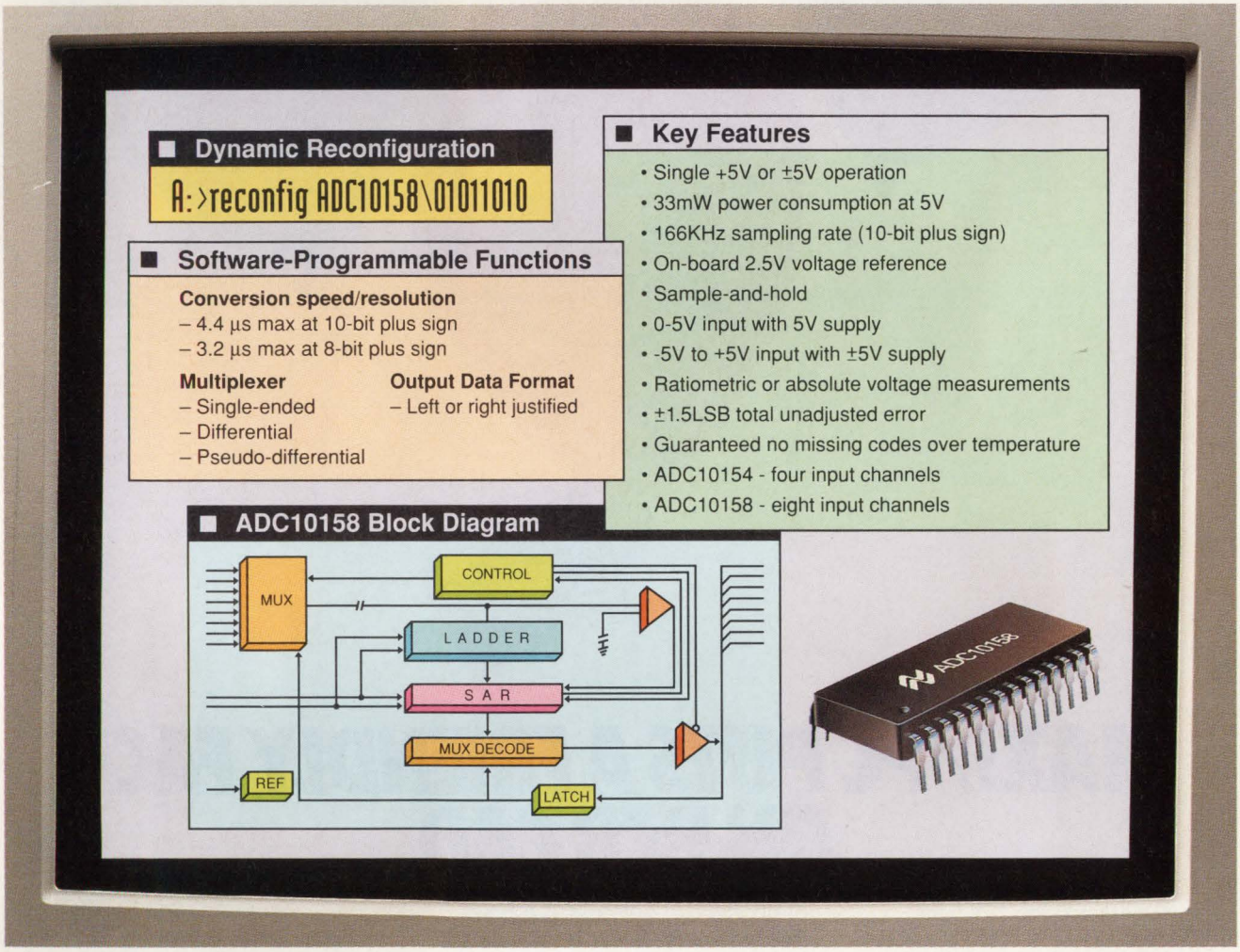

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CIRCLE 180 FOR U.S. RESPONSE

CIRCLE 181 FOR RESPONSE OUTSIDE THE U.S.

FUTURE PACKAGING DEPENDS HEAVILY ON MATERIALS

PACKAGING DESIGN MUST RISE TO A SYSTEM LEVEL FOR TOMORROW'S MULTICHIP MODULES TO UNLEASH THE POWER OF THE SILICON THEY'LL HOUSE.

BY DAVID MALINIAK

The road promises to become narrower and steeper for designers in the 1990s. Even now, notions of desktop systems with gigahertz clock rates are taking shape for some designers, and the hardware for achieving such goals is just a tweak or two of IC lithography away. But questions loom: How will designers eliminate the parasitic and path-length effects of packaging, which worsen as speed increases? What about the thousands of I/O lines to be connected? The answers to these and other technical questions lie with package designers and, to a large extent, with the basic materials and processes they'll be using to craft their designs.

At virtually every level of packaging, from the housings for single chips to that of entire systems, the materials and processes used will have greater effect than ever before as system speed increases. In some cases, the package, which in days past was thought of as an element of the system, is now the entire system, or a large chunk of it. As a result, designers will no longer be able to take basic configuration decisions for granted. Those decisions must be made earlier than before in the design cycle. Thus, their implications will reach to the very heart of the system's performance—the movement of signals from each element of the system to others.

For the foreseeable future, the multichip module (MCM) will be the basic packaging vehicle for upcoming generations of high-end systems. Paralleling the developments in the MCM area will be those of single-chip packages, which will maintain their dominance in low- to mid-range systems. For both, a host of material- and process-oriented issues must be resolved before the processing power of tomorrow's silicon can be unleashed.

Many technical challenges are presented by MCMs, and quite a few fall into the materials arena. First, one must justify their expense for a given application. Then the problems of substrate selection, dielectrics and their performance, die attachment and interconnection, and others are all for the materials engineers to solve. There are also infrastructure issues to be worked out. The overall assembly philosophy—chips first or chips last—is another issue that has an impact on the reworkability of MCMs. Moreover, the assembly technique must be considered with respect to the layout of chip I/O.

A Faster Future

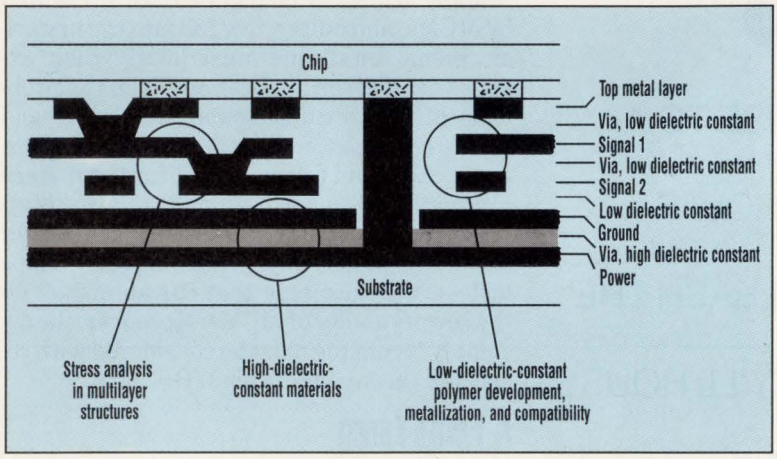
Anticipated future demands for packaging vary with expectations of system performance. At the Microelectronics and Computer Technology Corp. (MCC), the Austin, Texas-based industry consortium, the goal for the next few years has already been mapped out. By the mid-90s, MCC's plan is to assemble a 300-MHz superworkstation with a 3-ns cycle time. Such a system might have 10 million gates in its CPU. The total system will dissipate around 1500 W and will require 200 to 300 A of input current. Not only that, MCC hopes that optimization of packaging and assembly technology would drive the cost of such a machine under $5000.

MCC's superworkstation is envisioned as a single chassis carrying four stacked MCMs. Each MCM would hold about 100 chips, with each chip having about 500 I/Os. The interconnection density would be on the order of 1000 in./in.^{2} (in other words, 1000 in. of wiring in an area measuring 1 in.^{2}). MCC hopes that future advances in IC integration would reduce the number of chips so that only one MCM would be needed. By the year 2000, it's hoped that the cost might fall to $1000.

It's apparent that MCMs will be needed in such a high-end machine. In these applications, performance demands override cost concerns. But because of their relatively high cost, chances are that MCM technology will

begin to be used on a wide scale only when they're needed to break the performance bottleneck imposed by single-chip packages. Finding the right applications for MCMs is a key consideration. MCMs are unlikely to be used in such applications as automotive electronics, where there's intense pressure to keep costs low. But for high-performance applications with relatively low volume, an MCM's cost may well be tolerable.

The reliance on singly packaged chips will have to be rethought at system clock rates of 50 to 100 MHz by various estimates. Somewhere in that range is where single chips, surface mounted on pc boards, will be too far apart to handle those clock frequencies. After that, the MCM will be the way, at least for now, to get chips close enough together to exploit their raw speed.



1. For dielectric materials, research thrusts are ongoing into materials with both lower and higher dielectric constants. In the future, concern will mount with respect to the compatibility of materials and their ability to withstand stress.

The shift to MCMs will begin as clock rates in high-end workstations approach those of high-end bipolar computers, which means the 50-to-100-MHz range. "The switch to MCMs will most likely begin with RISC processors designed for scientific computing, where a large cache memory is needed," says Jerry Kopcsay, a research staff member at IBM's T.J. Watson Research Center, Yorktown Heights, N.Y. The on-chip cache found on today's 80486 processors is relatively small compared to what will be needed in future RISC-based, vector-processing applications. In spite of the continuing advances in on-chip integration of memory, Kopcsay says, additional cache memory will be needed on one or more other chips. Where MCMs come in, says Kopcsay, is in bringing the CPU and cache memory into close proximity.

Many issues remain to be sorted out, however, before the technology to achieve such lofty goals becomes practical. One issue is MCM substrate selection. At the low end are laminated substrates using typical pc-board materials like FR-4. These substrates, referred to as MCM-L, are attractive because of their low cost, but their wiring density is limited to 50 to 150 cm/cm^2. Their speed capability is also limited to 100 to 200 MHz.

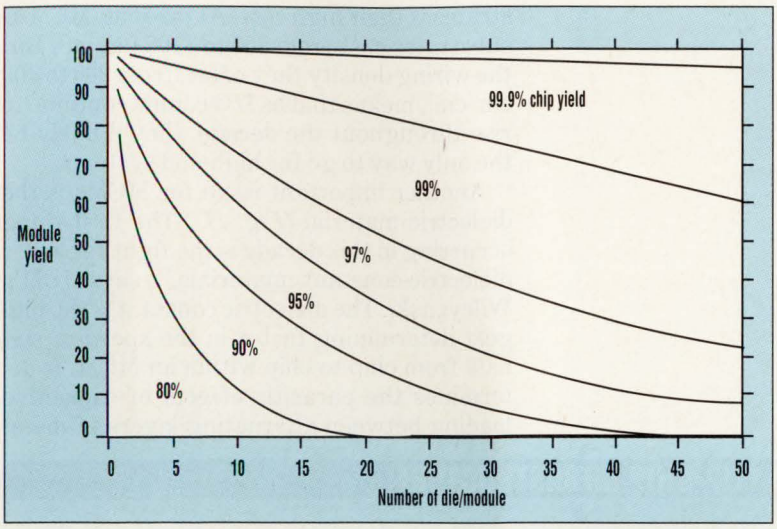
MCM-L substrates will be the first type to become widely used because of their relatively low entry costs. Therefore, the need arises for materials development in fine-pitch pc boards with higher-temperature materials, moving away from FR-4 and more into polyimide and other resins. Only then will volume use of MCMs begin to take shape.

MCM-L material technology has some potential for being extended to compete with the next levels, which are cofired ceramics (MCM-C) and deposited thin-film approaches (MCM-D). For that to happen, designers will need low-dielectric-constant laminates. These materials, however, will need to be thinner than usual for fabrication of high-density vias. With such developments, Brad Nelson, MCC's manager of microfabrication technology, believes that laminates can continue to compete favorably with MCM-C technology at the higher end of their speed range.

Extending Laminar Substrates

As an example of the extendability of MCM-L technology, researchers at IBM Corp.'s Yasu Technology Applications Laboratory, Yasu, Japan, have developed a packaging technology called surface laminar circuit (SLC) that permits mixing of flip-chip components, SMT devices, and through-hole components (ELECTRONIC DESIGN, *Dec. 5, 1991, p. 31)*. By using photosensitive epoxy to create insulating layers, the wiring density becomes double that of conventional pc-board technology. That's because the 130-μm-diameter photoetched vias are much smaller than drilled holes. Plated through-holes can also be on the boards, though. The technology aims to reduce the cost of boards for portable consumer products, primarily laptop and notebook PCs.

Although IBM doesn't consider SLC technology as an MCM substrate technology first and foremost, it's a big step toward cost reductions in direct-chip attachment. In fabricating the double-sided glass-epoxy boards, a copper-clad layer is etched with the wiring footprint. Next, a photosensitive epoxy resin is applied to the top side of the first signal layer to produce the first insulation layer in which via holes are photoetched. The epoxy is then treated with permanganate to anchor the plating of a second copper signal layer. Finally, the signal lines are etched, a second insulating layer is applied, and a pad layer is



2. Good, working chips are absolutely essential in achieving high production yields at the module level. As the number of chips on modules increases, module yields fall rapidly with only slight decreases in chip yields.

plated and patterned on the mounting surface.

To achieve its cost reductions for portable electronics, the SLC technology uses standard, commercially available materials. It's also a process innovation in that C-4 flip-chip attachment is done using ordinary eutectic solder, which melts at 183°C instead of the 310°C for normal C-4 processing. This enables IBM to perform flip-chip attachment in a board-assembly environment rather than a costlier, more tightly regulated MCM-assembly environment.

Some experts, however, believe that the density of wiring in MCMs for high-end tasks will be too dense for FR-4 or similar materials. Having to encapsulate the devices and cool the board "makes me uneasy because the material is not so stable," says Janusz Wilcyznski, director of packaging technology at IBM's T.J. Watson Research Center. In addition, Wilcyznski believes that the future clock rates requiring MCMs will be too high for FR-4 to support.

That leaves designers of MCMs for high-end applications with MCM-C and MCM-D materials. The MCM-C technology is a mature one and has been demonstrated in a number of high-end military and commercial applications. It too, however, has its limitations. MCC has found that interconnection densities in ceramic substrates are limited by screen printing. It takes many layers to achieve high densities, which makes the technology costly. Densities in ceramic run from 100 to 250 cm/cm^2. Recent advancements were made to reduce dielectric constants and improve the material's coefficient of temperature expansion, says MCC's Nelson.

Some extension of ceramic-substrate technology is possible, MCC's Nelson states. That would call for reduced custom tooling requirements and better dimensional tolerances for processing of larger formats. Improved tolerances would also permit interfacing with thin-film and high-density interconnections.

One improvement that can be made is the glass-ceramic material used by IBM in a 5-in.^{2} package for its System/390 computers. The 63-layer substrate has a dielectric constant lower than any other ceramic material in commercial production, the company claims. Signal propagation, which is about 25% faster than the alumina-ceramic material it replaces, is partly due to the use of copper wiring at a density of 140 ft./in.^{2}. That presented a tough challenge, because the substrate must be sintered with the wiring in place. Therefore, the substrate had to harden before the wiring melted. The company's engineers induced the ceramic to crystallize at 1742°C, which is just 203°C under the copper's melting point.

But with the wiring density in ceramic substrates growing by about 20% per year, there's a limit to the technology's usefulness at the high end. "One can project how much more mileage is left in the standard cofired-ceramic technology," says C. Kumar N. Patel, executive director of the Research, Materials Science, Engineering, and Academic Affairs Division of AT&T Bell Laboratories, Murray Hill, N.J. In light of the estimated boom in ceramic-wiring density, ceramic-substrate technology will hit its density limit in two to five years, he says. The primary reason is that ceramic substrates can't be fabricated flat enough. "When you get down to line widths approaching a few micrometers, the yields go down significantly," says Patel. In terms of speed, however, Patel believes that silicon-on-ceramic technology will support circuitry into the gigahertz range.

Silicon Takes Over

Within five years' time, though, MCM-D technology will take over for ceramics in the high-end systems, Patel contends. The base materials for these deposited thin-film approaches are primarily silicon, although ceramics are used in many cases, as are metals and composites. Silicon, however, will always have the advantage of a perfect thermal-expansion-coefficient match to the bare die that are mounted on it. For that reason and others, Mike McShane, manager of advanced package development at Motorola's Advanced Package Development Prototype Lab, Austin, Texas, considers silicon to be close to an ideal substrate material. "You can put in a

silicon-substrate line with 10-, 20-, or 25-μm design rules—you don't want the traces at real fine pitches because of the losses and crosstalk," says McShane. "And you don't need real tight planarity for substrates."

Aluminum, gold, or copper conductors can be deposited on silicon through evaporation, sputtering, or electroplating. This enables the conductors to be patterned by means of photolithography. Then thin-film dielectrics of polyimide or other polymers can be spun, sprayed, or extruded onto the surface. That process is repeated for multiple interconnection layers linked by staggered vias.

The primary problem with silicon substrates is their high cost. At present, MCM-D substrates cost from $50 to $100 per in.^{2}. But the wiring density they offer, from 200 to 400 cm/cm^2, means that as I/O counts continue to rise throughout the decade, they'll likely be the only way to go for high-end systems.

Another important issue for MCMs is the dielectric material *(Fig. 1)*. "The first thing occurring in this decade is the fight for lower dielectric-constant materials," says IBM's Wilcyznski. The dielectric constant is the biggest determining factor in the speed of signals from chip to chip within an MCM. It determines the parasitic effects of capacitive loading between alternating layers of metal

BUILDING A FLIP-CHIP INFRASTRUCTURE

All indications are that in tomorrow's advanced multichip modules, flip-chip die attach will be a predominant technology. The advantages of flip chip are well documented. But for flip-chip technology to become a widespread practice, the IC manufacturers may have to begin selling bare, unpackaged die, which, historically, has been an unpopular idea.

The problems of moving bare, bumped chips from supplier to assembler occur in a couple of areas. Handling the chips is a difficult problem because of their fragility and sensitivity to static. Testing of the die, with no leads attached, is another sticky problem.

One of the difficulties with flip chip as opposed to TAB technology is that with TAB, the attachment problem is broken up into manageable chunks. The chip maker has much more control of the process. Once the chip is inner-lead-bonded to the tape frame, it becomes, in effect, a packaged device that can be tested and guaranteed before shipping to a customer, who can verify that test. The customer makes the outer-lead bonds, which makes it easier to distinguish a problem in the inner leads from a problem in the outer leads. That way, you know which way to point if a problem arises. "When there's a problem with flip-chip attachment, you don't know whether to point up to the chip manufacturer or point down to the substrate," says Dennis Herrell, director of the Packaging/Interconnect Program at MCC. Herrell assumes that the chip manufacturer would be applying solder bumps to the die before delivering them to users.

Only the most vertically integrated companies, such as IBM, have the ability to even work effectively with bare die in-house. When it comes to IC manufacturers selling them to customers, the key will be building strong relationships. "Our history says that we don't do it," says Mike McShane, Motorola's manager of advanced packaging development. "But if a customer wants it, it'll be considered as a business decision. That means strong partnerships and alliances and doing business with honor and trust, not finger pointing when things go wrong."

"Bare die would be sold, although reluctantly," says Jack Belani, National Semiconductor's manager of packaging. Handling bare chips means more cost to the chip makers, and that cost would be passed along. On top of that, IC makers would not like to lose the value-added revenue gained from packaging their chips conventionally. But, echoing McShane's view, Belani adds that it'll be customers who will ultimately determine what decisions would be made.

In the future, system designers will want more subsystems and systems delivered. They will be specifying functionality, and won't care if it comes on one piece of silicon or a multichip module. Thus, in terms of packaging development, the chip designer, the package designer, and the system designer must work together early on to ensure that the product will meet the customer's expectations. It's likely, however, that it would be large customers, such as a Sun Microsystems, a Hewlett-Packard, or an Apple Computer that would have the clout to force the issue.

As part of its efforts to develop the infrastructure for widespread adoption of MCM technology, one of the goals of MCC's on-going flip-chip project is to develop methods of bumping bare die so that they can be used for either flip-chip or TAB attachment. "That may only be a solution for relatively small volumes, but it might fill a prototyping gap," says MCC's Herrell.

Rather than selling die to those who would integrate them into modules, the IC manufacturers may in the future choose to begin building modules themselves. Companies like Motorola and Intel, which have older-generation fab lines, could conceivably use that equipment to fabricate their own silicon substrates for use in multichip modules.

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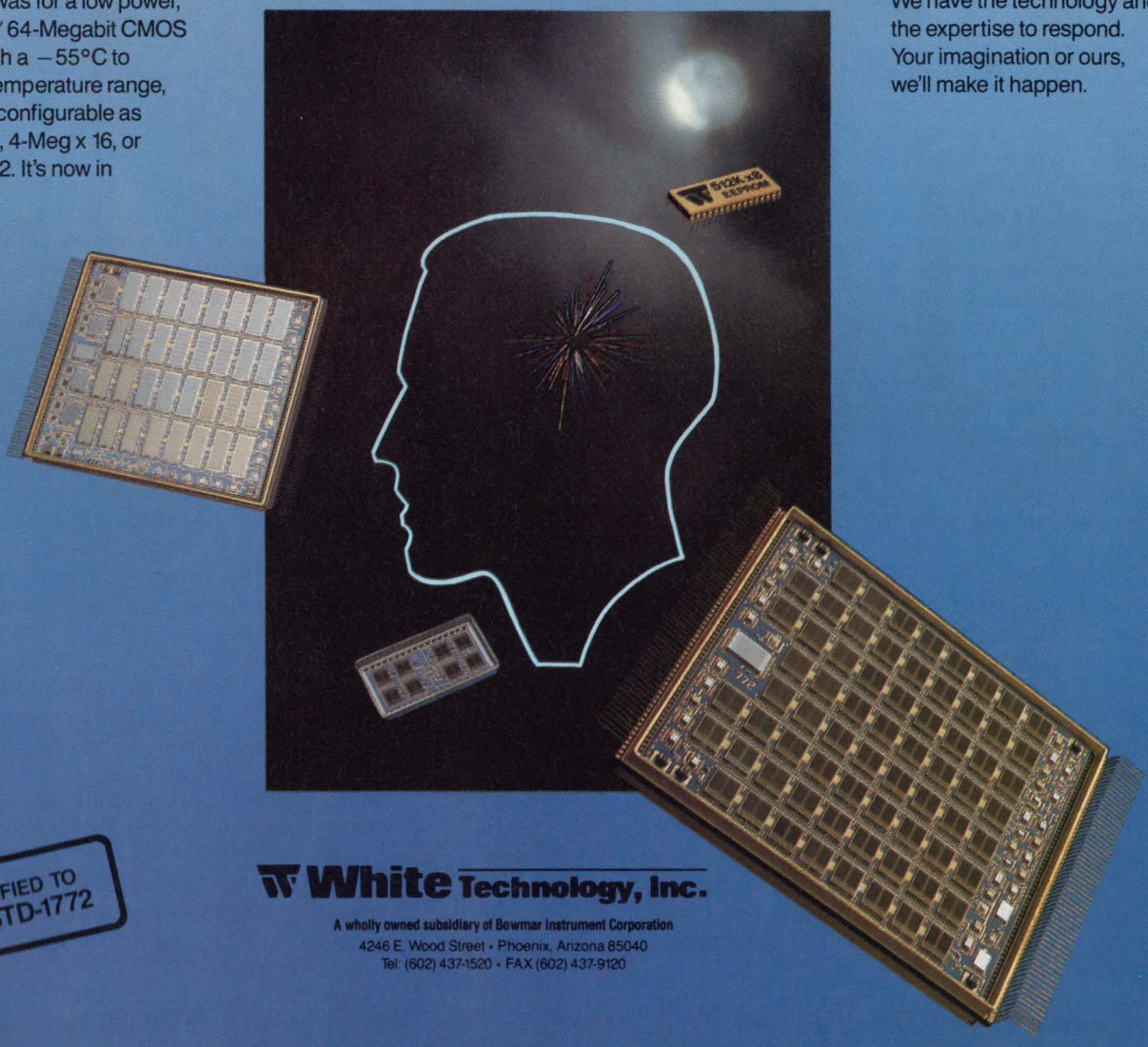

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and dielectric.

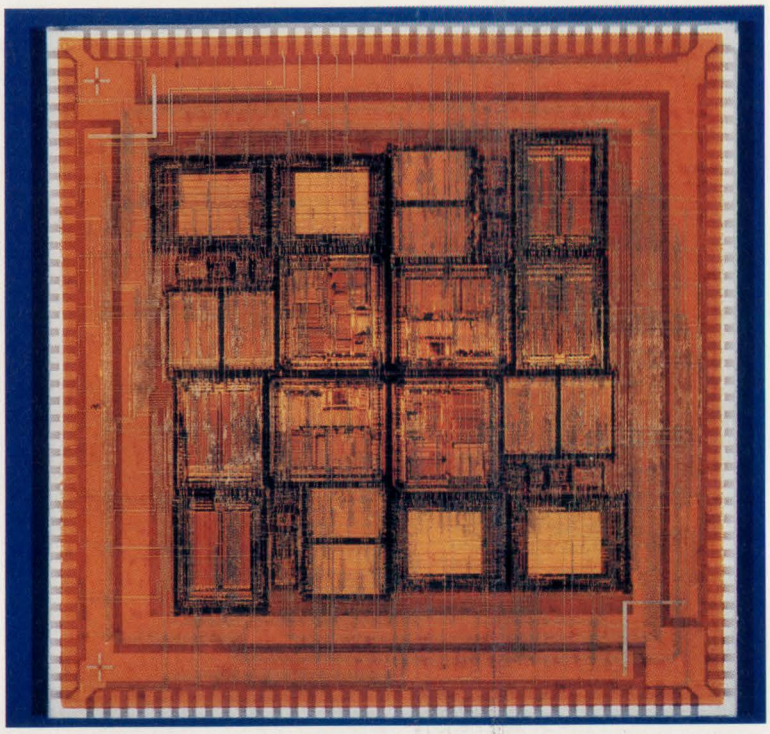
For MCM-D technology, most research in dielectrics centers around polyimides and alternatives to it. Theoretically, the best dielectric constant is a vacuum, with a value of 1. At present, polyimide-based dielectrics run from a high of about 3.5 to a low of about 2.9. The main question, according to David Knorr, assistant professor of materials engineering at Rensselaer Polytechnic Institute (RPI), Troy, N.Y., is how low does the dielectric constant have to go before the polyimides must be replaced? Because the signal-propagation delay is a function of the square root of the dielectric constant, small increments in the constant won't have much impact on performance. Knorr's guess is that the constant will have to go to about 2.3 in alternate materials before switching over can be justified.

Toward The Perfect Polymer

The perfect dielectric polymer would have a temperature coefficient of expansion that fell somewhere between silicon and the metallization layers in the MCM. It would have a dielectric constant of around 2, be highly processable, have a very smooth surface finish, adhere well to various metals including copper and gold, and be relatively low cost. Unfortunately, in the real world, research into dielectrics is rife with trade-offs. For instance, some work at RPI on alternative dielectric materials involves fluorinated versions of polyimides, which have somewhat lower dielectric constants. A potential difficulty with such materials, however, is their low adhesion to other materials, which diminishes their usefulness as a dielectric.

Although MCM designers would prefer a large step down in dielectric constant, incremental improvements are available that can somewhat improve MCM performance. For example, Dow Plastics, Midland, Mich., offers a thermoset dielectric material called benzocyclobutane (BCB), which takes the dielectric constant down to about 2.7. In addition, the material offers the advantage of lower water absorption than polyimide, which can eliminate the need to bake the material during processing to remove water. Water absorption in the dielectric can adversely affect its constant and cause changes in its characteristic impedance.

An emerging trend in dielectric materials that may improve future module manufacturability is photoimageability. Photoimageable polymers, already widely used in Japan and experimented with at IBM, could remove several steps from the process of creating interconnection layers. But at present, the dielectric constants of photoimageable polymers aren't quite as low as traditional dry-etch types. And they're not likely to be popular with users without prior photolithography experience. Nevertheless, Dow Plastics is readying a photoimageable version of BCB that it claims will maintain the electrical properties of the dry-etch version.



3. This example of high-density-interconnect technology is how MCMs may look in the future. The module, which is made by Texas Instruments, Dallas, houses 36 chips on a silicon substrate measuring 2 in. on each side. Peak computing speed is 180 MIPS.

Although the trend toward lower dielectric constants addresses the signal-distribution function of the dielectric layers, it doesn't address the anticipated increase in power-distribution requirements. MCC's 300-MHz machine planned for 1995 will rely on chips that consume power in the 50-W neighborhood. Isolating the power-distribution network from the signal-distribution system is now done primarily with decoupling capacitors. At some point, such schemes could begin to slow systems down. Also, the simultaneous switching of the large number of logic circuits on future MCMs could inject large amounts of noise into the system, which would induce false switching. And as voltage levels for logic switching fall in the future from 5 V to 3.3 V to under 3 V, as is anticipated, the noise tolerance in MCMs will fall drastically.

Though careful layout and a well-thought-out set of design rules could alleviate these problems to some degree, the answer may lie in thin-film materials with a high dielectric constant. Under a contract with the U.S. Department of Defense's Defense Advanced Research Projects Agency (DARPA), re-

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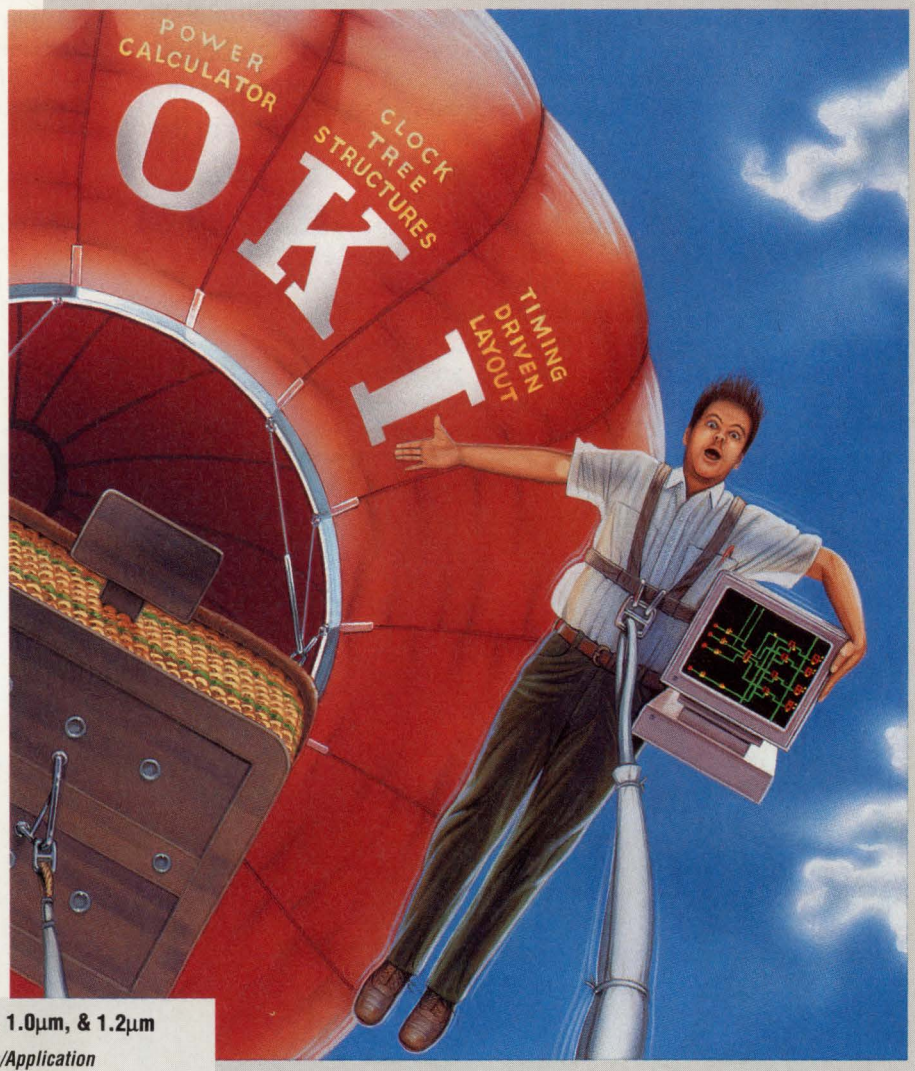

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searchers at RPI are developing materials that can be used as integral decoupling capacitors in MCMs. Such capacitors could be buried in the dielectric layers or placed in proximity to the chips. Or, placed between the power and ground planes, these capacitors could provide a reservoir of power that can be drawn from to dampen the voltage swings resulting from simultaneous switching.

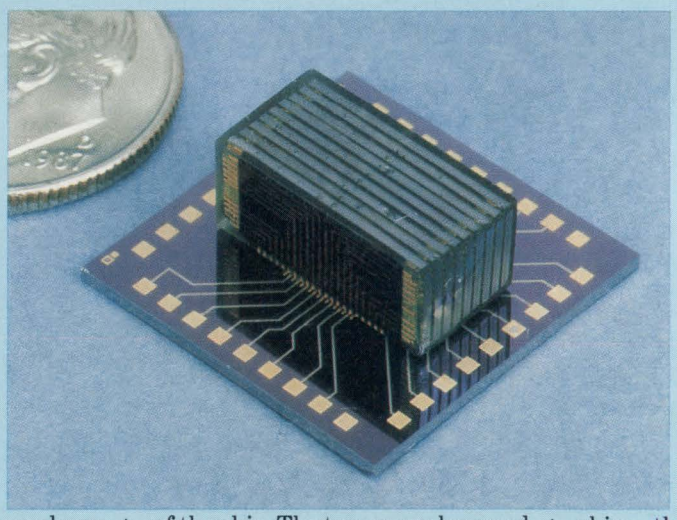
In the end, it'll be a case-by-case cost-performance analysis that will determine which substrate and dielectric option is right for a given application. But regardless of the substrate used, the next issue for designers to consider when looking at MCMs will be how to attach and interconnect chips to the module. Basically, four options for MCM chip attachment are available: wire bonding, tape-automated bonding (TAB), flip-TAB, and flip chip. A variation on the latter two is area-array methods, which encompasses such schemes as IBM's controlled-collapse chip-connection (C-4) technology and area-array TAB.

Flip chip is likely to be the leading method of chip interconnection to multichip-module substrates in the 1990s.

Each of the four interconnection methods has advantages and disadvantages. A key measure of merit is the distance each method permits chips to be mounted from each other. Obviously, the object in MCMs is to cover as much of a substrate with silicon as possible. According to Mike Nevares, department manager of microelectronic packaging systems in the Defense Systems and Electronics Group, Texas Instruments, Dallas, today's wire-bonding technology lets him mount chips roughly 100 mils apart. Next best is TAB, which permits mounting of chips from 50 to 80 mils apart. Then, flip-TAB gets the distance down to a maximum of 50 mils with just 10 mils between the ends of the lead pads. But the champ of substrate utilization, however, is flip chip, with which chips can be

THE 3D PATH TO HIGHER DENSITY

For now, MCMs represent a clear path to extremely dense, highly integrated blocks of circuitry that will far outstrip the packaging density of past technologies, such as surface-mounted pc boards. But some are already looking beyond MCMs as they exist today toward a means of still higher integration. "I don't know what MCMs will look like in 10 years, but they won't look like they do today," says Dr. John Prince, director of packaging research at the Semiconductor Research Corp., Research Triangle Park, N.C., and a faculty member at the University of Arizona at Tucson. For Prince, MCMs with planar chips mounted side-by-side on a substrate is merely an extension of business as usual. Higher integration requires ways to pack more function per unit volume than that.



One approach that has met with some success is 3D packaging. A number of manufacturers have pursued various methods of stacking memory chips. Texas Instruments has demonstrated its ability to stack from eight to ten 1-Mbit DRAMs or 256-kbit SRAMs in packages about the size of a sugar cube *(see the figure)*. To do so, each chip's I/O is rerouted with one layer of metallization at the wafer level down to one edge of the chip. The traces are bumped and attached to a TAB leadframe, which facilitates testing of the chips. The chips can then be glued together into the cube, which is flip-chip-attached to a substrate. For 1-Mbit SRAMs, the cube yields a memory density of 83 Mbits/in.^{3}, compared with 2 Mbits/in.^{3} for conventional surface-mounted packages.

Another company, Irvine Sensors Corp., Costa Mesa, Calif., has been able to stack as many as 100 layers of 4-Mbit DRAMs for a total of 50 Mbytes of memory in the same sugar-cube-sized package. This density is achieved by thinning the die at the wafer level to as small as 7 mils.

Under funding from a Strategic Defense Initiative contract, Irvine Sensors' 3D-packaging technology will be used to demonstrate an artificial neural network. In the baseline architecture, which already exists, a very dense grid of detector material converts an optical image into electrical signals. The grid is attached to a stack of processing chips that performs operations analogous to that performed by the human eye. Over 16,000 pixels of a scene can be sensed and initially processed by a cube. In the neural-network application, this architecture is taken a step further by attaching a second cube that will perform higher-level processing functions.

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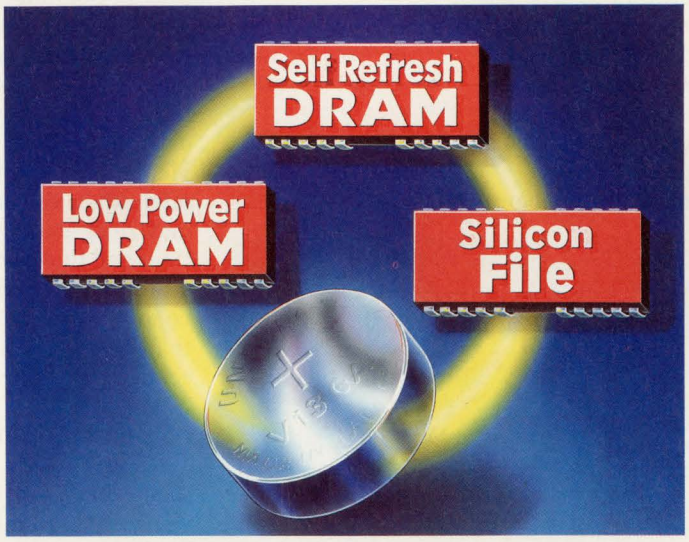
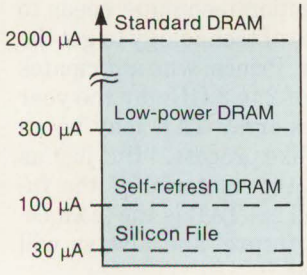
Low-power DRAMs

The Low-down on Memory Power



Memory devices are as varied as the applications they are designed for, but in this age of miniaturization and mobility they have one thing in common: power consumption must be rockbottom. Capacity, speed, price or package choice may be your highest priority, but you'll be glad to know that DRAM memories from NEC operate on an absolute minimum power supply.



Based on a 0.7 µm, stacked capacitor process, NEC's 4 Megabit DRAMs offer high access speeds and convenient configurations for a wide range of desktop and portable applications. Competitively priced standard DRAMs have the high capacity required by stationary systems, while low-power DRAMs with a 300 µA data retention current are ideal for laptops and other equipment frequently on the move. NEC's Silicon File, only needs a 30 µA refresh current, and is designed to do duty as a solid-state disk in mainframes, workstations and PCs. Data retention by way of a 3 V battery gives this memory static RAM quality. Another device with extremely low power consumption is the self-refresh DRAM with a byte and word structure and optional parity. Intended for new low-power designs, such as notebook and palm PCs, it requires a mere 100 µA standby current. Compatible as to function, speed and pin assignment, all these DRAMs can also be configured as SIMM modules or memory cards.

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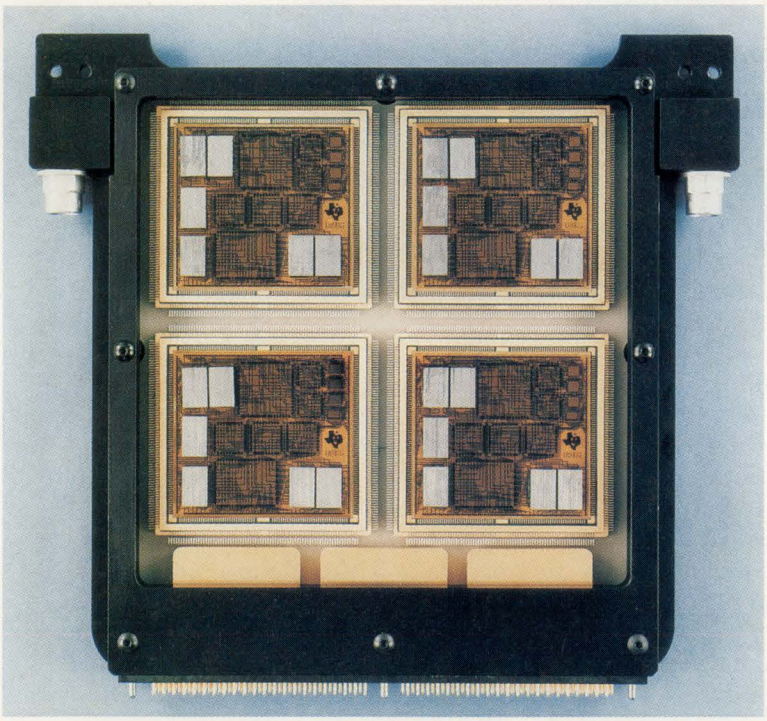
mounted just 10 mils apart. Nevares says, however, that chips are typically mounted about 20 mils apart to permit substrate repairs if necessary.

For that reason, flip chip is likely to be the leading method of chip interconnection to MCM substrates in the 1990s. But there are some infrastructure issues to be decided before flip chip takes flight *(see "Building a Flip-Chip Infrastructure," p. 86).*

In addition to infrastructure problems, flip-chip's tight spacing also means more thermal problems. According to Andy Paul, president of the MCM operation at Cypress Semiconductor, San Jose, Calif., going tighter than the 4-mil outer-lead bond that TAB now offers may mean more thermal problems than the density increase is worth. This leaves flip-chip adherents with the question of how to address heat removal.

Again, material science may be able to provide an answer. Scientists in MCC's Enabling Technologies (ET) Program are working on thermal-interface pastes that will address the issue in two ways. When working with individual die, the natural solution to thermal problems is to glue a heat sink to the back of the chip. But at the MCM level, and especially with flip-chip die, this becomes impractical. The next level, then, would be to attach a common heat sink for the whole module. But planarity variations from chip to chip make this impractical as well.



4. An extension of high-density-interconnect (HDI) technology is seen in this module, which features a two-sided HDI layer. Harbingers of greater functional density to come is evidenced by the module's use of Texas Instruments' 3D memory cubes, which can be seen sitting atop the HDI layer.

Here where the thermal-interface paste being developed at MCC comes in. The material as it stands now has a very thick consistency and is very stiff, yet still compliant. According to Ollie Woodard, manager of the ET Program, MCC has had some success by applying this paste to the backs of the chips and then applying a common heat sink. In addition to its very high thermal conductivity, the paste also makes up for the differences in planarity between the individual chips. It's basically a conductive powder and a liquid mixed in the proportions required to create the right consistency.

Wire-bonding technology keeps improving and is down to 40-μm pitch capability, which means that the venerable technology is probably here to stay in many high-end applications. "Wire bonding keeps pushing TAB over the edge of the table," says Motorola's McShane. "When you can wire bond at a 4-mil pitch, then you don't need TAB." This trend may relegate TAB to niche applications with finer and finer pitches, McShane added. In addition to its pushing TAB technology, wire bonding is bound to remain less expensive than TAB because of the wafer-bumping costs that TAB incurs.

Area Array Arrives

Some industry experts, however, maintain that area-array techniques, which can provide very high interconnection densities, will be the way to go. One believer in area-array attachment is Dr. John Prince, director of packaging research at the Semiconductor Research Corp., Research Triangle Park, N.C., and a faculty member at the University of Arizona at Tucson. Prince states that "in the future, the chip-connection technique needs to be an area-array type of technology to get the contact density." Dr. Prince, who anticipates system-clock rates of 2 to 3 GHz by the year 2001, feels that area-array TAB may be an alternative to a C-4-like process. "But just as gallium arsenide is the 'material of the future' and always will be, TAB is the 'connection method of the future' and always will be," Prince maintains.

A critical factor in building future MCMs will be to ensure that the chips are in working order before committing them to a substrate. The more chips a module is to carry, the greater the impact of chip yield on overall module yield after assembly *(Fig. 2)*. To get a 95% yield at the module level, module builders need a chip yield of no less than 4000 ppm. Despite flip chip's advantages in substrate utilization, the bare bumped die required by the methodology are difficult to test at the wafer level or after they've been sawed into

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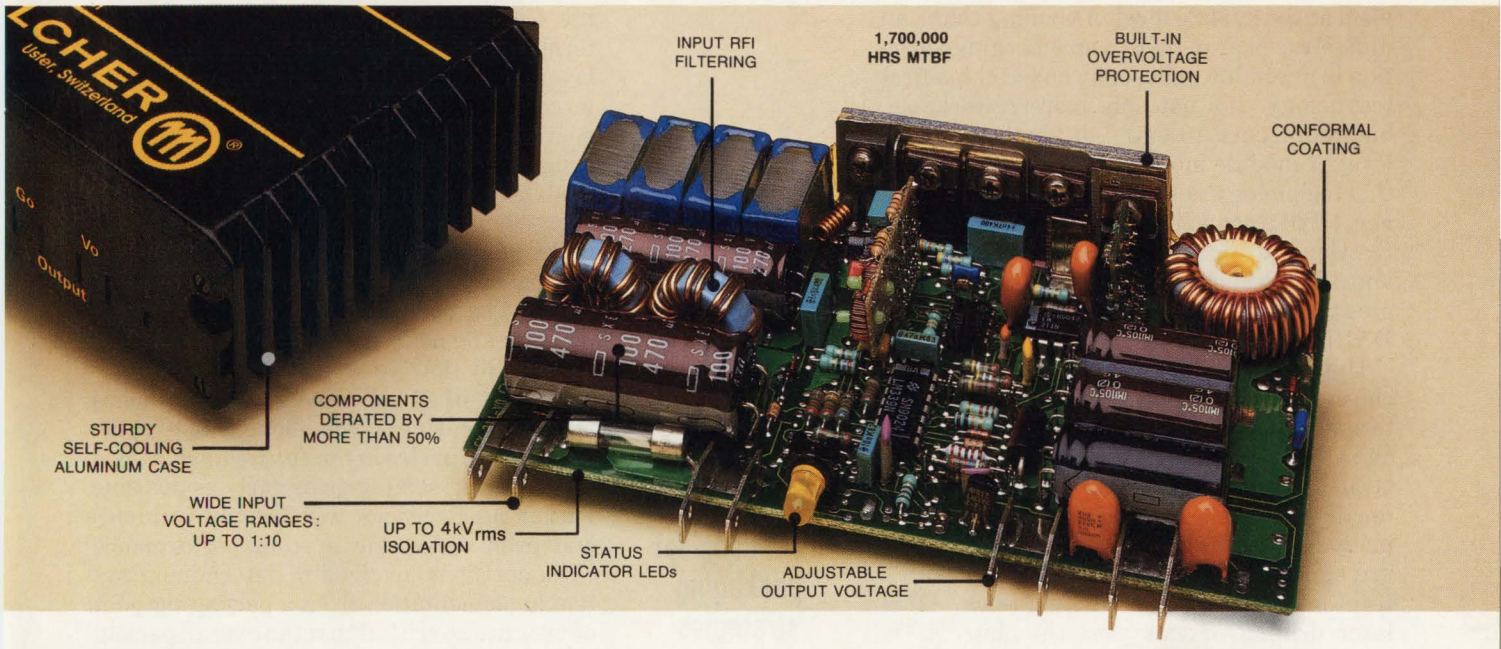

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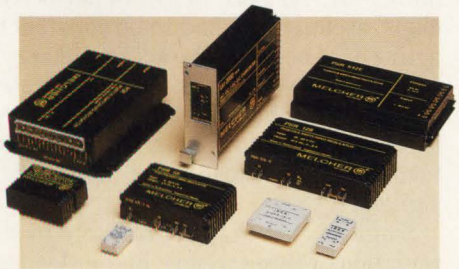

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chips. In this regard, TAB has the edge with its leadframe and the convenience it offers for building in test points.

Ideally, a builder of MCMs would like to be given nothing but good, working chips, which would go a long way toward ensuring 100% yield at the module level. Assuming that's an unlikely scenario, there's an emerging variation in assembly philosophy called chips-first technology. It's not only more reworkable, but represents an entry to another, higher level of module integration. One example of this technology is the high-density interconnect (HDI) technology that was developed by the General Electric Co., Schenectady, N.Y., and is being commercialized by Texas Instruments under the terms of a three-year DARPA contract *(Fig. 3)*.

Unlike chips-last technology, in which chips are soldered to the interconnect-patterned substrate in one manner or another, chips-first technology merely uses the substrate as a fixture and a cooling medium. After the chips are affixed face-up with a thermally conductive adhesive to cavities milled in a substrate, they're laminated over with a Kapton layer that's about 1-mil thick. After laser drilling of vias over the chips' I/Os (which can be anywhere on the chips), the Kapton layer is metallized down to the pads on the chips and coated with photoresist, which is scanned with a laser for the interconnect patterning. Etching the copper and washing off the remaining photoresist leaves the first layer of metal. Subsequent layers can be added by spinning on layers of polyimide and repeating the process.

The technology offers several attractive features for future MCM builders. If changes or rework are required, the interconnect layer is easily removed. The laser patterning is done directly from the CAD database for the module, so no masks need to be changed to pattern a new interconnect layer. The chips can be mounted as close as 10 mils apart, which can yield substrate utilization of up to 90%. Substrate materials can be alumina, alumina nitride, silicon, silicon carbide, graphite, or whatever material serves the thermal requirements of the application. Thermal conductivity is also improved by the fact that the chips are mounted directly on the substrate, with no dielectric layers in between. Also, the chips won't need bumping, saving time and expense.

Once its DARPA-sponsored MCM foundry is in full operation, Texas Instruments will demonstrate the HDI technology. One concept, which would take advantage of the company's previously developed 3D packaging technology *(see "The 3D Path To Higher Density," p. 90)*, shows what the HDI technology can lead to in terms of packaging density *(Fig. 4)*.

Because of packaging's influence on system performance, future design cycles must consider packaging strategies as early as possible.

Each MCM substrate has cavities in which chips are placed virtually edge to edge. With the CAD-database-driven drilling and patterning laser, multiple thin-film metallized layers are sequentially added to form the interconnect structure. On top of the interconnect structure are six of the 3D memory cubes. The chassis is a SEM-E form-factor module that measures about 5.5 by 6 by 0.6 in. Processing power for the unit as a whole is 1.6 GFLOPS and 400 MIPS. Each module would dissipate about 75 W for a total dissipation of 300 W. The hollow substrate that the MCM modules and next-level interconnect rests on is cooled by flowing liquid.

In light of MCM packaging approaches, which increasingly will include 3D topologies, design cycles in the future must consider packaging strategies as early as possible. Packaging decisions will heavily influence and even determine system performance. "The decisions involved in determining system implementation from a packaging point of view are so critical that the overall packaging issue has been elevated to a system level," says Milt Buschbom, Texas Instrument's product manager for high-performance ASICs. "You'd better be thinking about it at the definition stage for a given system. Any time after that, you're too late."

The layout of chips and the placement of their I/O must be tuned to the packaging strategy being considered. "We've seen cases where we've looked at ASICs with customers and how the devices would be efficiently implemented as a module. To do that implementation, we had to totally rethink what we were doing at the chip level," says Buschbom.

In the case of TI's 3D memory architecture, bonds are made in the active areas of chips. The same is true of the lead-on-chip with center-bond technology that TI developed jointly with Hitachi America, Brisbane, Calif., for 16-Mbit DRAM packages (ELECTRONIC DESIGN, *Mar. 14, 1991, p. 29)*. In both cases, the chips' architecture had to be constructed for active-area bonds. "The active memory array of the chips is about as sensitive to stress as can be," Buschbom relates. From step one, their design had to be created with the lead attachment uppermost in the minds of the designers.

Single-chip packages are likely to see continuation of three trends: higher lead counts, tighter lead pitches, and thinner packages.

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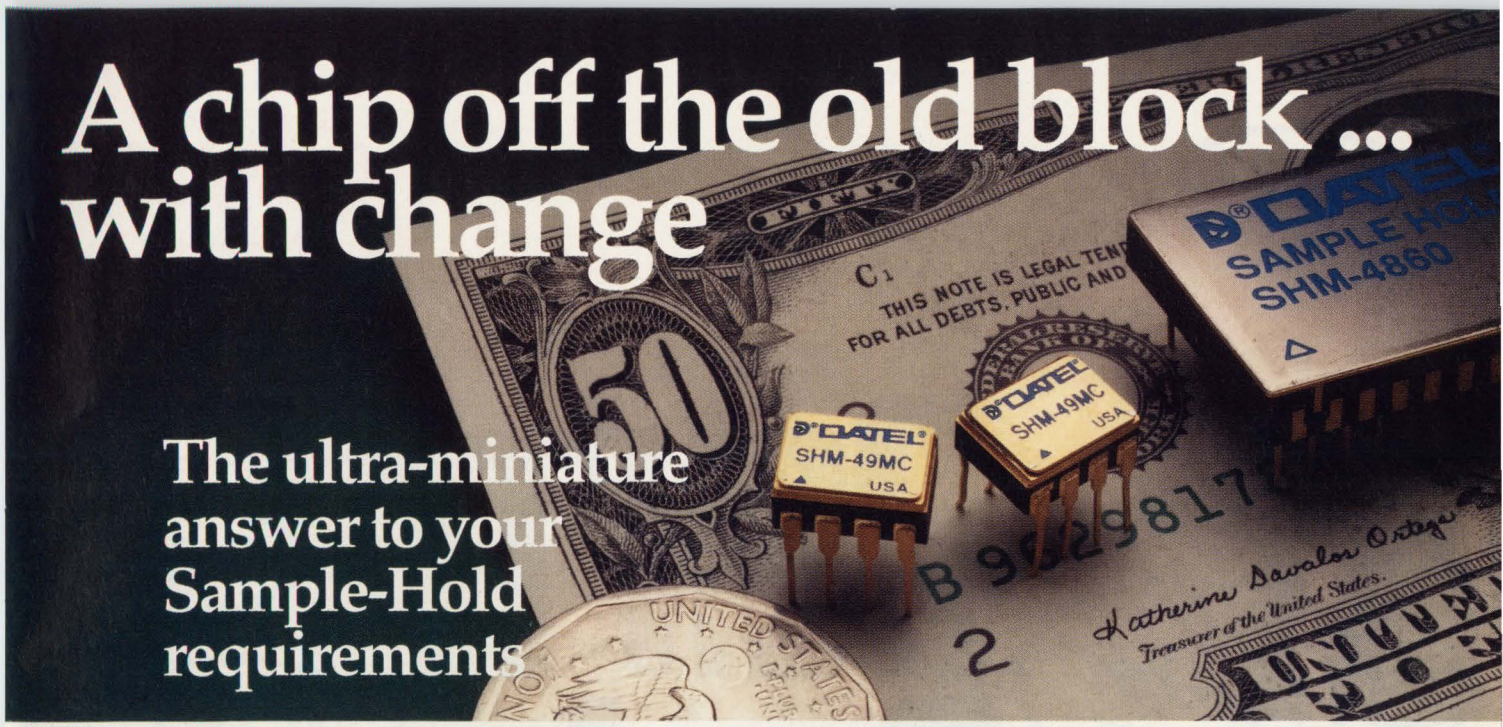

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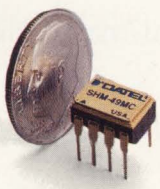

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The combination of these trends leads to more materials and process issues. "Harmonizing the packages with the chips is a very important requirement," says Dr. Walter H. Schroen, TI Fellow in the Process Automation Center of Texas Instruments. "It will be more and more difficult to take the power out of the chips. And it will be more and more challenging to make them reliable."

Single-chip packages are taking on more functionality, which is driving the trend to more I/O. With IC-lithography roadmaps stretching to 0.25-μm design rules, single-chip functional density will continue to increase. As we move from the era of very-large-scale integration (VLSI) to the reign of ultra-large-scale integration (ULSI), single-chip lead counts will explode into the 500+ range and higher.

With higher lead counts comes tighter pitches, which helps keep chips from getting too large. At least one manufacturer, S-MOS Systems, San Jose, Calif., plans to introduce a quad flat pack (QFP) with a 0.3-mm pitch. That would give them 504 leads in a 40-mm/side package. At present, the company offers a 304-lead package in the same size. Packages with 1000 leads on a 0.3-mm pitch have been prototyped by Motorola, as have packages on 0.15-mm pitches.

Single-Chip Challenges

Just as with MCM technology, efficient usage of board space is a driver of packaging and interconnection technology for single chips. Technical challenges include such items as the molding compounds, the formation of the wire loops from chip to leadframe, and the leadframes themselves.

As packages become thinner, it'll become harder to ensure their reliability. The integrity of the plastic that surrounds the silicon and leadframe will be more difficult to achieve. The thin, small-outline J-leaded package (TSOP), which is commonly 1-mm thick, is about to give way to 0.5-mm (20-mil) packages, sometimes called paper-thin packages (PTPs). In such a package, the silicon will have to be back-grinded down to a thickness of about 8 mils, which is very difficult without cracking the die. After leaving another 6 mils for the leadframe and tape, only about 6 mils remains for the molding compound. Such an application requires a low-viscosity molding material that can squeeze itself into a very fine aperture.

From a process perspective, the importance of stress equalization will increase as packages become thinner. With silicon being made thinner, its intolerance to being flexed by the plastic as it expands and contracts with thermal dynamics increases. But as the plastic thins, this will be less and less of a problem, says Schroen. Still, the importance of equalizing the stresses exists, which will require close attention to, and intimate knowledge of, process variables.

Close attention to and intimate knowledge of process variables will become more important as packages become thinner.

Another requirement for these extremely thin packages is a low loop in the wire bond from die to leadframe, which involves still more difficulties. As the gold wire is heated at its tip to form a ball for bonding, heat conducts up the wire and changes its crystalline size and orientation. The enlarged crystals lose some mechanical strength and result in a wire bond with somewhat lower pull strength than is desirable. This imposes a limitation on how low the loops can be made. Typically, pure gold can be looped to a height of from 5 to 7 mils, says Schroen.

In efforts to make lower looping possible, Texas Instruments, for one, is investigating additives to the gold wire to increase its strength. Researchers have found that adding boron or copper in amounts less than 1% make the metal considerably stiffer by inhibiting the gold crystals' tendency to enlarge when heated. This makes the wire more bendable.

Yet another possible solution to the wire-looping problems in thin packages may be found in a technique called ribbon bonding. Ribbon bonding still involves a metallic lead consisting of a wire or a ribbon (a ribbon is a wire that's somewhat stiffer, because it has less flexibility in the direction of the width). But because the ribbon is bonded using ultrasonic wedge bonding instead of thermocompression as with ball bonding, the bonds are made at room temperature. With no temperature changes in the wire from melting the ball, there's no corresponding weakening of the wire. The wedges can be so small that the loop height is essentially zero.

As for the leadframes themselves, there's some work to be done on copper alloying. As pitches get finer and finer, the copper for etched leadframes tends to be too brittle. "There's got to be some basic metals work to improve the alloys and make them more malleable," says Steve Saller, director of contract manufacturing at S-MOS Systems. According to Saller, yields are too low for lead bending with today's copper alloys.□

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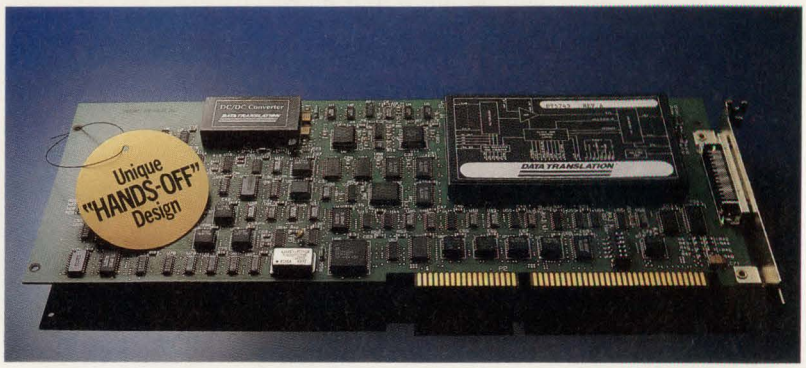

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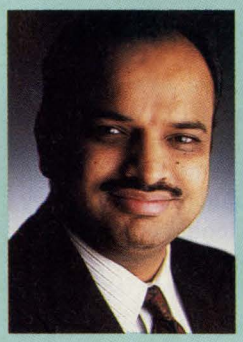
MULTICHIP-MODULE TECHNOLOGY WILL DRIVE EDA EVOLUTION

SYSTEMS LED BY MCM TECHNOLOGY WILL NEED MULTIDIMENSIONAL CONSTRAINT-DRIVEN DESIGN



SANDEEP KHANNA
Sandeep Khanna is Valid's product marketing engineer for pc-board, MCM, and hybrid analysis tools. He has an MBA and an MSEE from the University of Bridgeport, Conn.

Technological advances are the sculpturing tools that constantly reshape people's lives. As tomorrow becomes reality, video conferencing will allow people in different continents to conduct meetings as if they were in the same room. It will also improve health care by remotely providing the expertise of the big-city medical centers to rural areas. In addition, personal-computer, telecommunications, and audio-video technologies will merge, and the resulting multimedia technology will allow people in remote locations to work together on the same computer files with high-quality audio and visual information, such as voice and full-motion video. One important technology that's needed to reach these eventualities is multichip modules (MCMs).

IBM first used MCM technology in its mainframes over a decade ago. Multichip packaging is a very simple concept and it offers some fundamental advantages over packaged devices interconnected on a pc board. In boards, the maximum number of pins per chip, the maximum logic density, and the maximum operating frequency are limited by the wiring density and the electrical and thermal characteristics of the chip and board interconnect methods.

In MCM packaging, the unpackaged die are mounted on a substrate with high die-to-substrate-area ratios, high achievable I/O counts, and high interconnect densities. Interconnect delay, which is a major factor in the overall system performance, is substantially reduced. Three factors make this reduction possible: high component densities that allow for reduction in the interconnect length, eliminating parasitics associated with one level of packaging, and the lower dielectric constant of frequently used materials that increase the propagation velocities of signals *(see the table)*.

Currently, however, multichip-module technology is only afforded by high-cost, low-volume mainframe computer systems. The long development cycles and higher development and manufacturing costs can only be afforded at the high end. As cost and time-to-market improves, however, multichip-module technology will become a viable technology for lower-end systems.

For this to happen, however, a new breed of design tools is needed to reduce the cost and time associated with the development cycle. The traditional serial design approach with pockets of automation won't be acceptable if maximum performance and density are squeezed out of the design *(Fig. 1)*. Consequently, the next generation electronic-design-automation tools must provide:

- High-level design verification, synthesis, and partitioning tools that allow engineers to work at the conceptual level, thinking in terms of functions they want to implement rather than the actual physical mapping of their functions.

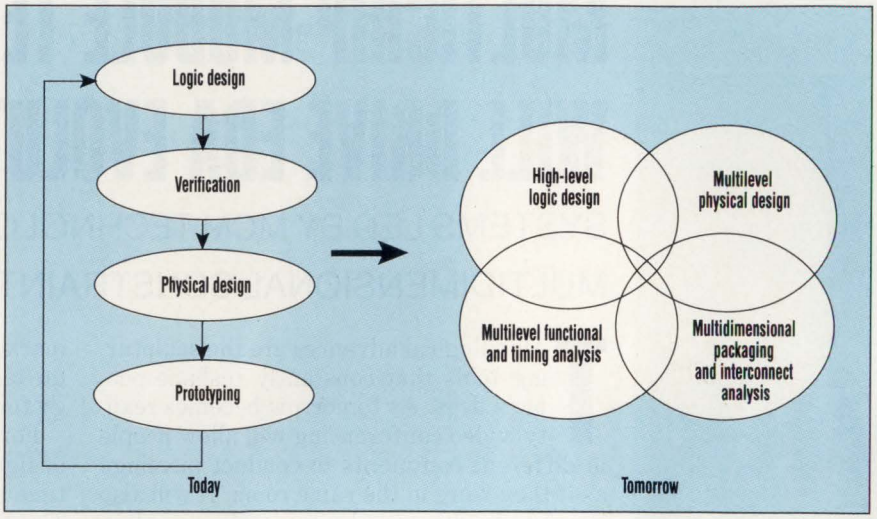
- Multilevel physical design tools that are equally applicable at the IC, MCM-substrate, and board levels in a homogeneous environment. These design tools need to encourage multidimensional, constraint-driven design optimizations and trade-offs at various levels of a design's physical hierarchy.

An MCM designer must be able to simultaneously control and optimize the various performance and quality constraints, such as thermal distribution, delays, crosstalk, ringing, simultaneous switching, and electromagnetic-interference noise. In addition, they will have to control them at each step of the design process: placement, pinout assignment, and routing. All of these criteria will have to be met, not as a part of design verification or a post-processing cycle as it exists today, but rather as a constraint-definition design cycle. All of these capabilities should become an inseparable part of the automatic tools, just as manufacturability-design-rule checkers are today *(Fig. 2)*.

A dichotomy will exist with designers of the future: some will move enthusiastically to a higher level and others will have to be driven to work at a higher, more abstract level. In the past, when engineers moved from designing with discrete devices to ASICs, they were

forced to simulate their designs. When the move was to larger ASICs, they were forced to design at the RTL level and employ synthesis tools to generate gate-level descriptions. Now, the move to multi-ASIC MCMs will require the introduction of sophisticated design reuse and partitioning tools while expanding the scope of the synthesis technology *(Fig. 3)*.

Future users will be able to provide a stochastic description of a system. Then intelligent fuzzy-logic techniques will use these abstract, partial descriptions of the system to search out the appropriate modules from previous designs that best meet the partial description. These modules may exist in the form of off-the-shelf cards, MCMs, individual ASICs, or megacells. Then, based on other criteria, such as development time, design and material costs, power dissipation, and size, a loosely assembled view of the design would be presented to the designer. The user would then synthesize the missing functions and glue these predesigned modules together to customize the system to his current needs. Making this possible requires technological advances in hierarchical library management and intelligent library-search techniques.



1. Today's design process will evolve from a serial process with islands of automation into a true concurrent design process.

Up-Front Trade-Offs

Synthesis technology will encourage design at a higher conceptual level. It will also allow engineers to conduct up-front design trade-offs and optimizations. The actual implementation and technology-mapping details will be handled by the automatic synthesis tools. The scope of the tools will expand to synthesize a design defined at the behavioral level. In addition, there will be a suite of synthesis tools focused on specific design applications, such as data path, memory, random logic, and digital-signal processing. However, higher-level languages with graphical design and intelligent design-reuse/library-search constructs will be required to make this multifunction synthesis possible.

In the future, engineers will want to package entire subsystems on one wafer to avoid the performance degradation caused by the secondary interconnect. However, wafer-scale integration is still considered a technology of the future due to high costs and low yields. The future will also bring the need to copackage various technologies, such as CMOS, biCMOS, ECL, GaAs, optoelectronic, and optical components, in small highly-reliable enclosures of reasonably low cost. Physical design alternatives (for example, ICs, MCMs, circuit boards, and backplanes) and quality issues (such as thermal and noise management) are important considerations in assessing the feasibility of high-performance systems. They must be selected to ensure that the high-speed characteristics of individual components can be optimally used when they're integrated to form a complex system. Physical design choices are often key elements in determining the power, space, cost, and reliability performance of electronic systems.

To minimize the performance lost due to secondary interconnect, design architecture, and physical partitioning are extremely critical to system performance. For example, in microprocessor-based systems, it's necessary for the CPU and cache memory to be in close proximity to minimize access time. To achieve this, a designer could place a primary cache on the CPU chip and a secondary cache in close proximity on a common MCM. However, the main memory may be packaged on another MCM.

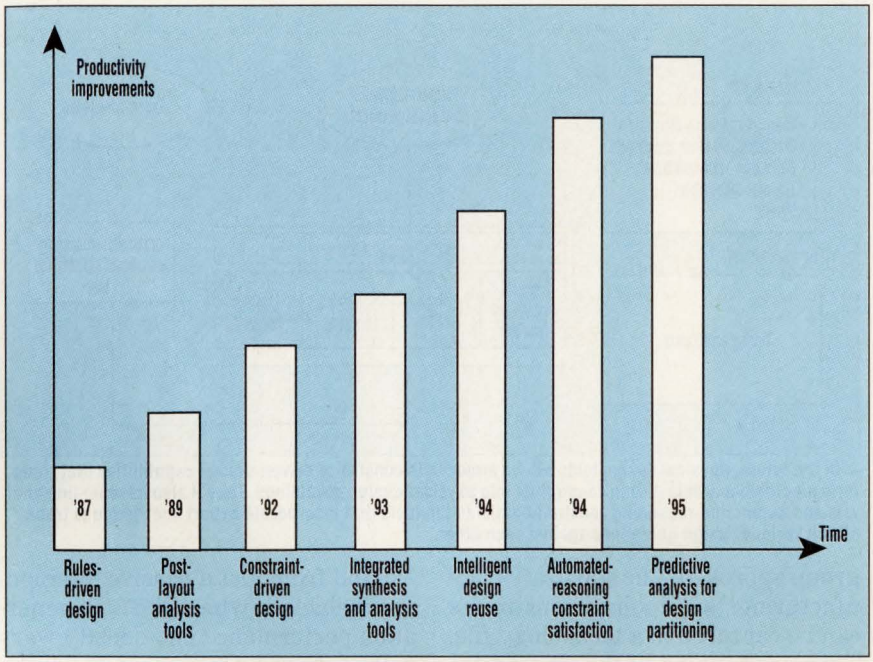
Partitioning Techniques

There are other partitioning techniques, such as pipelining, that mask the effects of the secondary interconnect. Because of these techniques, the computer architects' experience will continue to be paramount. However, predictive-analysis techniques will be developed to model entire packaging hierarchies to study these trade-offs. A combination of physical and architectural models will be used to describe the packaging hierarchy, ranging from a chip to the full system. The resulting set of coupled equations will then be solved to compute system characteristics and figures of merit. These include partitioning, signal delays on critical paths, coupled noise, switching noise, power dissipation, and heat transfer. This kind of approach will allow architects to optimize critical aspects of a packaging architecture.

Most designs consist of

A COMPARISON OF MCM AND PC BOARD PERFORMANCE

	Multichip module	Pc-board system
Chip delay	4.5 ns	4.5 ns
Package	0 ns	1.0 ns
Interconnect	0.5 ns	1.7 ns
Clock speed	200 MHz	135 MHz



2. Upcoming advances in EDA technology will reduce development time in spite of expected increases in design complexity.

physical hierarchy made from hundreds of components. Physical design tools must handle both intra- and inter-levels of each hierarchy. Unlike today's single-level physical design tools, tomorrow's tools will be multilevel in nature. Decisions made at one level of physical hierarchy will dictate optimizations at another level. For example, pin assignment will place pins in the current level of the physical hierarchy by optimizing the upper level of the design in a top-down manner. Pin assignment plays the role of a bridge that transfers some information from the upper hierarchy to the lower. It should consider the wiring of both ICs and the MCM while meeting electrical constraints such as simultaneous switching output (SSO) and tolerant load-to-load distance. To effectively reduce the simultaneous-switching-output noise, the number of gates that can switch at the same time in a given area is restricted. Current physical design tools leave the burden of conducting these multilevel trade-offs in the designer's hands.

In a similar scenario, once the material characteristics and the cross-sectional definitions of the secondary interconnect (an MCM) are defined, a user knows about the loads that a given I/O buffer will be driving. This information can be used to optimize the driver on the IC. Today's design environment supports only a bottom-up methodology. Here, the IC drivers, which are designed first, handle the most severe of loading conditions. This results in high power dissipation and high propagation delay through the driver. What's needed is a multilevel environment that supports information flow in both directions, facilitating top-down design and bottom-up verification and implementation.

Uncovered Concerns

It used to be that the secondary interconnect, such as a pc board, could be treated as a passive interconnect medium. The worst thing that could go wrong would be that the layout wouldn't reflect the schematic. But the move towards MCM technology is being driven by the need for higher speed and density. Higher clock speed and density will bring many previously uncovered manufacturing, electrical, and mechanical concerns that often conflict with each other. It's unrealistic to train an entire workforce of packaging engineers who may not have the engineering background to be cognizant of every issue while designing MCMs. It's also unrealistic to expect that electrical engineers can be trained to adhere to all manufacturing criteria.

How, then, will future design teams resolve the problem of increasing complexity in layout coupled to non-engineers doing design? An average design has approximately 100 integrated circuits, 2000 nets, and 5000 driver-receiver pairs. Imagine having to specify multinet path delay, clock skew, crosstalk, simultaneous switching noise, component temperature, and other constraints on the schematic one driver-receiver at a time. It would become discouragingly tedious and inefficient to do this task manually. In fact, a typical designer would probably rather design the printed-circuit board by hand than to manually enter all of the constraints.

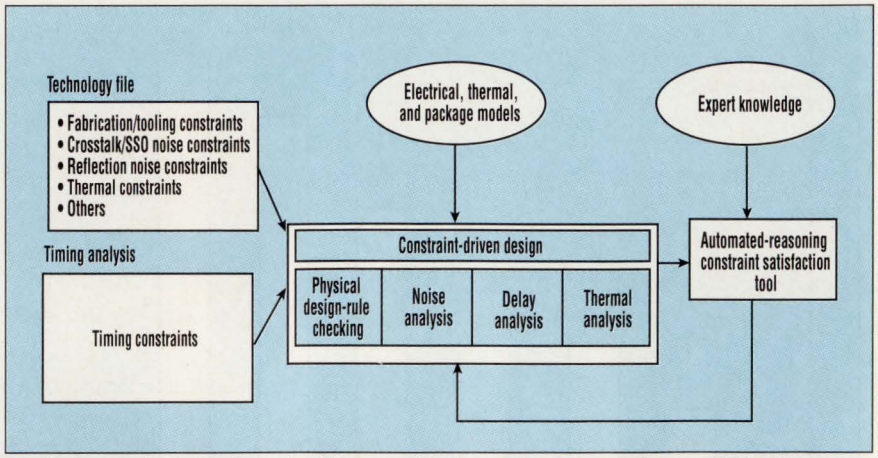
Moreover, the constraints placed manually on the schematic are conservative rule-of-thumb type of constraints that may lead to costly overdesigns and missed performance targets. Having an engineer address each of these concerns would lead to placing constraints on only the most critical of nets. Often, though, the known critical nets don't cause problems, it's the ones ignored as being non-critical. Hence, the constraint definition must be comprehensive and multidimensional, and must reflect the specific design.

Depending on the type, constraints will have different sources. For example, the amount of noise that's tolerable is a function of the noise immunity of the technology being driven. On the other hand, the maximum allowable delay on a given driver-receiver pair is a function of a specific design's timing. To encourage multidimensional constraint definition will require the advent of technology files and close coupling of timing-analysis tools with constraint-driven-layout tools. Technology files will be the repository for technology-dependent constraints. Other design-dependent constraints will be driven by the timing-simulation tools. Hence, the physical design-automation tools will satisfy innumerable timing requirements

for path delays, clock skew, and several electrical characteristics. This should minimize the time and effort expended by the designer identifying and correcting potential layout-related signal-integrity problems.

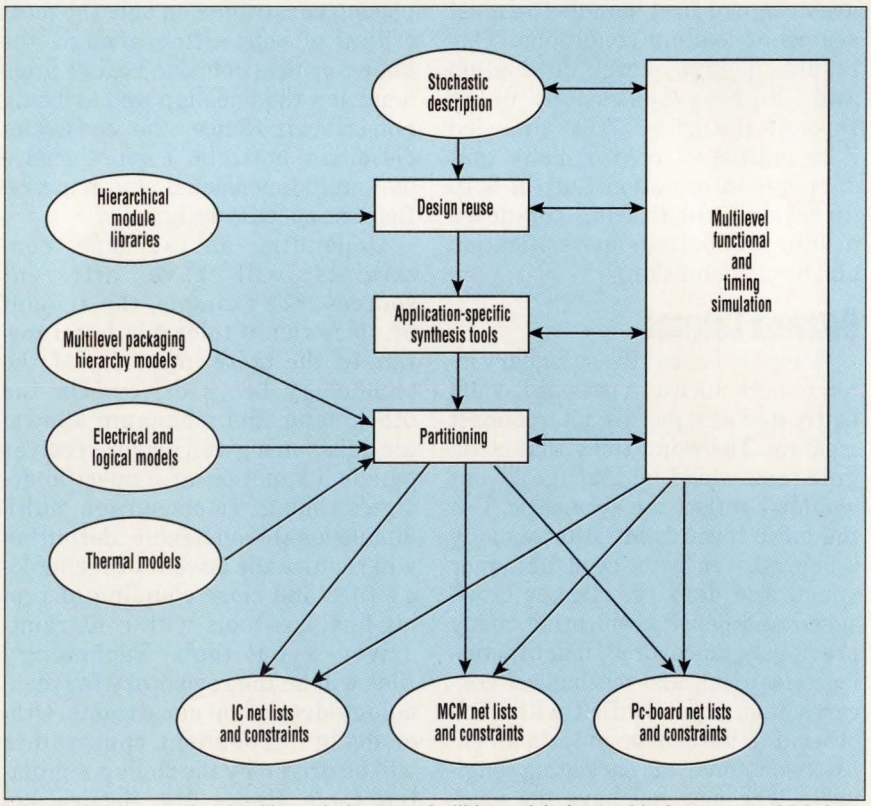
Prototype Debugging

Prototype debugging has been traditionally considered an acceptable point for detecting any design errors in card designs. The errors can usually be corrected quickly and a new board prototyped in a reasonable amount of time and cost. In contrast, multichip fabrication is much slower and retooling is more expensive. Therefore, an error-free, manufacturing-oriented physical design process is required. The steps in the design process and substrate fabrication should be integrated into one process, controlled by one group. What's needed is a means to capture manufacturing concerns in the CAD tool so that the physical-layout designers couldn't deviate from those concerns unless the controlling group approved. The substrate manufacturing and tooling constraints can be captured in a technology file. This concept of technology files would allow the physical designers to leverage the engineer's knowledge, include the manufacturing details, and still perform the layout function as quickly as possible.



4. In the future, physical design tools will be armed with constraint-driven-design capabilities that transform electrical and fabrication constraints into physical-design guidelines. They'll also have on-line analysis and automated-reasoning constraint-satisfaction tools that incorporate expert knowledge to trade off the various design guidelines against each other.

The scope of physical design will expand from just a passive interconnect vehicle to where the next generation performance and density wars will be waged. On the one hand, the physical design tools will be driven by constraints provided by technology files, timing simulation tools, and interconnect model bases that translate electrical and thermal constraints into physical entities so that intelligent design decisions can be made. On the other hand, these physical design tools will be armed with analysis software that provides quick on-line feedback on whether the initial decisions are adequate or need modification. Relieving the engineer from the mundane and arduous constraint-definition process and from the feedback loop will greatly improve the quality of designs and accelerate turnaround times *(Fig. 4)*.



3. New technology, such as intelligent design reuse facilities and design partitioning across multiple levels of packaging hierarchies, will be introduced into the logic-design process. This will allow engineers to make informed trade-off decisions about various aspects of their designs.

Tool Migration

Further improvement of design time requires migration from general-purpose analysis tools to optimized tools that are designed to plug into the place-and-route tools. If a microsecond is needed to lay down a piece of interconnect and a minute is needed to analyze its effect, coupling these tools together won't yield much gain in design quality or turnaround. The collection of interconnect-analysis tools currently available provides an adequate solution for today's human-driven design and verification cycle. However, they will quickly become obsolete by the

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automated, multidimensional, constraint-driven design needs of MCM designers.

Another deficiency in these general-purpose tools is the lack of resemblance to a specific design situation. For example, every crosstalk-analysis tool available today assumes that all adjacent signals switch simultaneously, which results in pessimistic crosstalk predictions. In this scenario, an informed user must use his intelligence about the given circuit to separate real problems from false alarms. To make this analysis reflect a given design will require tight coupling between timing-analysis tools and the layout-analysis tools.

Once the physical design tools and the analysis tools are coupled together, the next logical step will be to trade off each of these constraints against each other. For example, two components may be placed next to each other to meet the timing constraint, but that placement decision may lead to local thermal distribution, routability, and simultaneous-switching noise problems. The analysis tools may provide feedback on each of these potential problems. But what's ultimately needed is a decision-making tool employing artificial-intelligence automated-reasoning techniques that will trade off the feedback from the various analysis tools into the next design decision.

While engineers strive to produce optimal designs, the reality of production deadlines and cost constraints often causes the ideal solution to be sacrificed. The outcome is a product that, although functional, isn't always the best. This inefficiency often occurs when physical design is artificially separated from system design and analysis. This artificial barrier must be dropped because squeezing every bit of performance out of a design will require the merging of packaging and interconnect modeling technology, logic and timing analysis tools, and physical design tools.□

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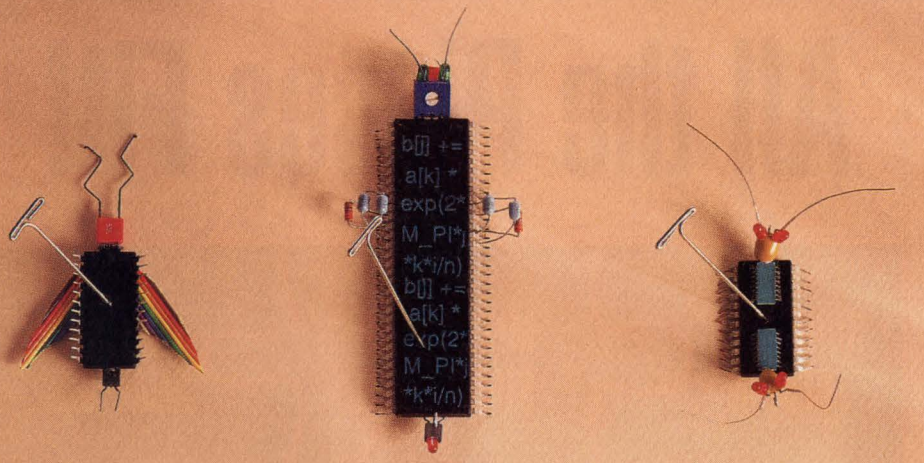

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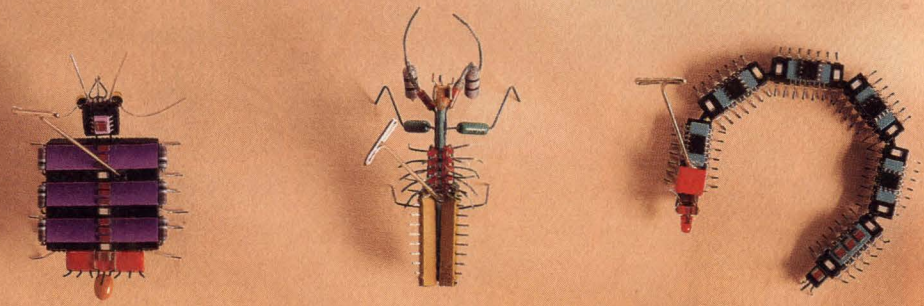

PARITY ERROR

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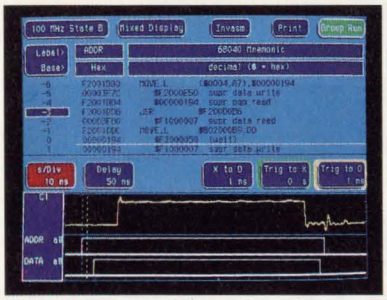

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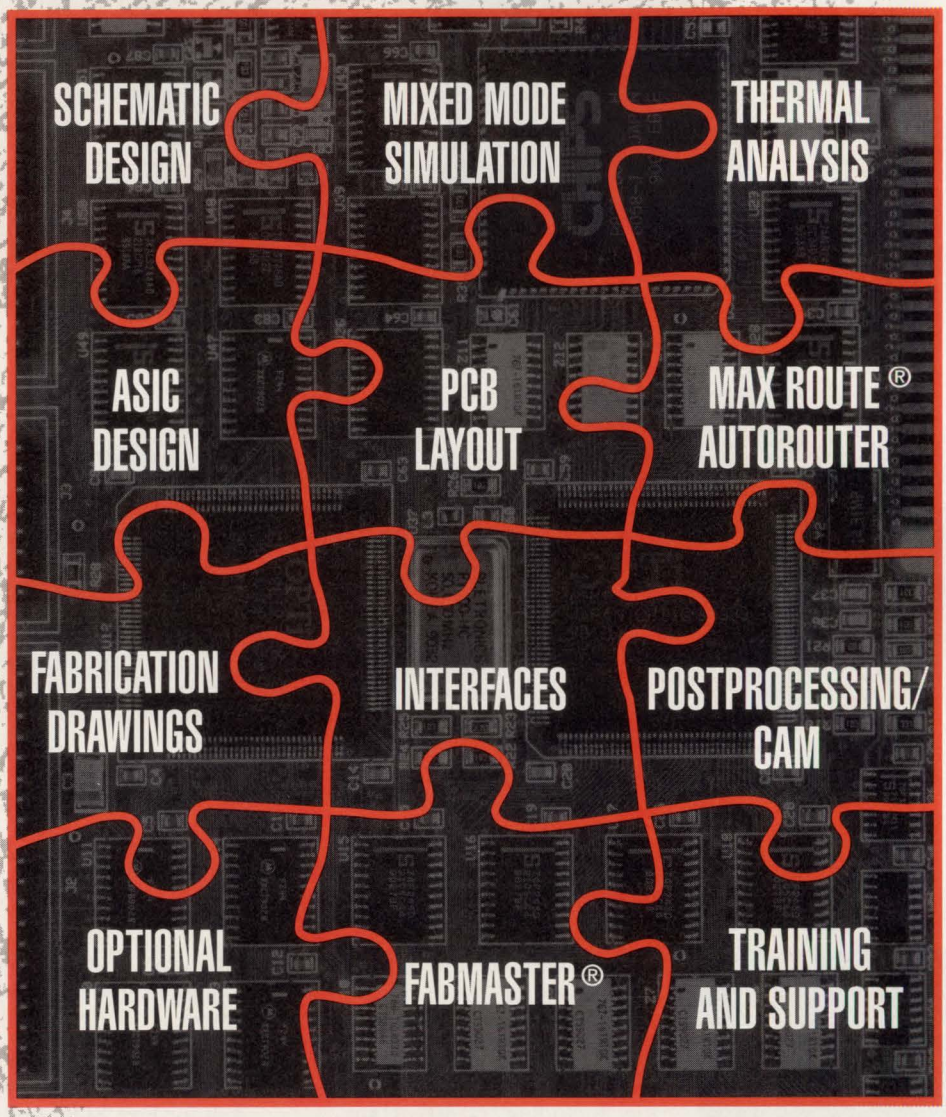

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NETWORKING ADVANCES WILL ANCHOR CONCURRENT ENGINEERING

TO KEEP PACE IN THE 1990s, NETWORKS WILL NEED TO BE FASTER AND MORE ECONOMICAL.

KEN WILLETT
A founder of Mentor Graphics, Ken Willett is the framework architect with the company's Framework Products Division. He holds a Masters degree in Computer Science from Washington State University.

As more electronics companies adopt Concurrent Engineering (CE) to improve their responsiveness to customer requirements, networking will play an ever-more-crucial role. New interconnection techniques will expand their geographic reach to every site worldwide.

Faster hardware components and new media will increase data bandwidth by orders of magnitude. And lower-cost connections will bring all of the platforms in touch with the product development environment. These advances will improve the breadth of CE's impact and help companies achieve more advanced CE practices.

In its most elemental form, a network provides electronic-mail services. Team members have a standard, readily available, reliable method of sharing their thoughts. However, with design cycles shrinking, design team members can't make trade-offs fast enough through such serial means. Just as the telephone has replaced the written letter in everyday communication, so will more interactive technologies, like video teleconferencing, replace electronic mail for design-team collaboration.

Today, many engineering organizations have progressed beyond electronic mail to distributed file sharing. Team members can use remote file servers to store design data. This relieves local data storage requirements and makes it possible to share databases among team members. Distributed file sharing goes beyond just messaging—it allows the interaction of ideas through the design itself. But just like electronic mail, the collaboration of design team members will force a movement to share entire databases, not just files, over the network.

Future network advances will also have considerable impact in what's being called the organization dimension *(see "The Dimensions of Concurrent Engineering" p. 109).* By making communication more accessible and reliable, networks move team members from communication to collaboration. That makes it easier to solicit advice and opinions, and to build consensus. By connecting users to central server resources, networks ensure that each team member has all of the computer power he or she needs. And by putting all databases in the same environment, the network plays a role in controlling the quality of the end product. However, as more engineers, parts vendors, and customers become involved in the CE process, tomorrow's networks will have to stretch to provide cost-effective communication with all of these sources.

Another point to consider is that CAD frameworks build on top of the local-area network (LAN) connections to implement the interfaces among specific engineering tools and the engineers themselves. The efficiency with which a framework can link these people and programs depends heavily on the power of the network technology. Because CAD tools demand more and more services from the framework, such as access to multiple disparate databases, LAN services will have to become faster and broader to support new generations of CAD design environments.

Commercially available frameworks and networks provide a concurrent-engineering capability at what is defined in *Concurrent Engineering: The Product Development Environment of the 1990s,* authored by Don Carter, as the first CE phase: interoperable tools and tasks. Advances in network technology will work with framework technology to implement more advanced concurrent engineering phases.

FUTURE TRENDS

Given the demands on network services, concurrent engineering will be most affected by three trends: increasing network speed, more platforms connecting to networks, and the development of global networks.

The first area of network evolution concerns the speed with which networks can transmit data. Engineering network bandwidth is jumping from today's hundreds of kbits/s to Mbits/s.

As rates climbed to 10 and 100 kbits/s, engineers moved from electronic mail to sharing entire pages of text and line drawings *(Fig.*

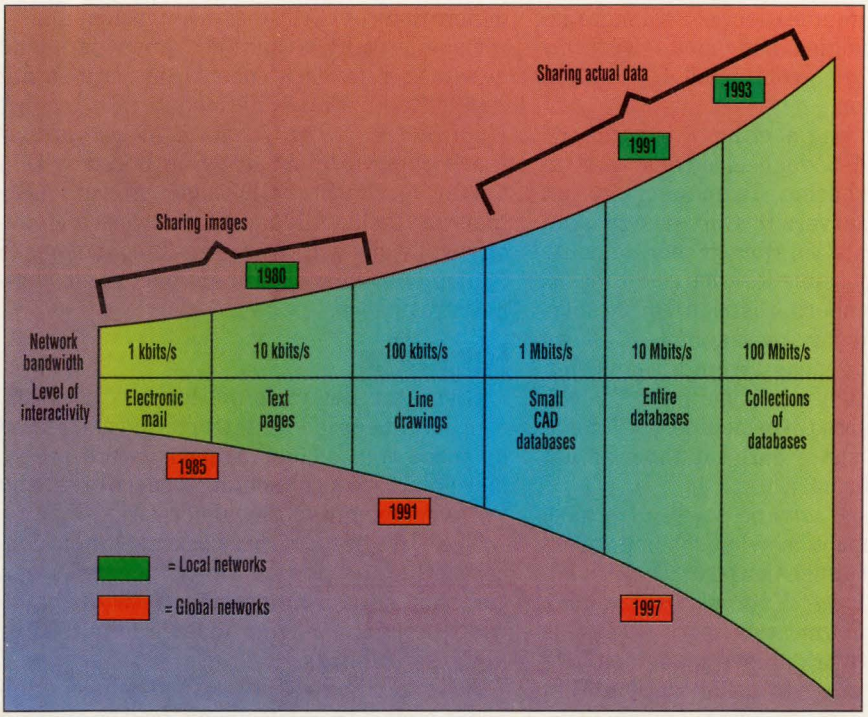
1). But given the millions of bytes needed to represent physical and electrical entities, it becomes clear that today's network users can only share abstractions, simplifications, or specific views of those entities, not the entities themselves.

Even today, networks are using new hardware and communication protocols to increase available bandwidth on existing and new media. For example, Ethernet networks using the 10-baseT format can supply increased bandwidth through inexpensive thin coax or twisted-pair telephone lines, rather than heavy cable, for local workgroups.

Due to the cost effectiveness of 10-baseT Ethernet, most of today's engineering environments are now switching to network data rates in the range of 10 Mbits/s. As a result, their design environments can begin to sustain real interaction between network nodes. For example, a million-pixel graphical image of a system could be shared over the network with an acceptable response time. This lets programs utilize remote graphics more easily, enabling compute-intensive programs to remain on compute servers and user workstations to serve primarily as graphics front-ends. For example, Mentor Graphics' network has a bandwidth of 10 Mbits/s, allowing the company to run remote graphics applications over the network.

Workstation technology is also pushing the need for a 10 Mbit/s bandwidth. Performance has skyrocketed from 1 MIPS just six years ago to as high as 50 MIPS. Now designers can perform large analyses on their desktops, but they need to get 100 Mbytes of design data to the workstation.

As workstation performance improvements continue unabated, the typical workstations of 1995 will execute at least 50 MIPS, and the leading platforms will provide around 250 MIPS. Feeding data to these workstations will necessitate 100-Mbit/s transaction speeds. Fiber-optic media running the fiber distributed data interface (FDDI) delivers bandwidth as high as 100 Mbits/s, so most companies will switch their engineering environments to fiber-optic cabling by 1995. Team members will progress from sharing images of such things as a CAD drawing representing a CAD database to real-time sharing of entire databases. At these higher information rates, network-based platforms can send a complete computer-readable description of a design, fast enough that engineers can effectively share the description. Engineers can thus take advantage of the enormous power on their desks, and can move from communication to collaboration.



1. As network bandwidths increase from thousands to millions, engineers can move from communicating to collaborating by effectively sharing design databases.

Connecting More Platforms

The second networking advancement will be connecting all engineering platforms to the network. This change will result from a drop in connection price points and improvements in networking software and hardware products.

In the 1980s, a typical network connection cost about a thousand dollars for the hardware alone. As a result, it was too expensive for most personal computers and terminals. But an Ethernet connection is no longer a significant price premium. Network connection cards have dropped an order of magnitude in price, so any desktop computer can become part of the network.

Consequently, personal computers can now support the efforts of a concurrent-engineering design team. Many engineering tools on PCs currently perform isolated tasks for a single user, like programming a programmable logic device, which can support the team CE effort. Also, X-Windows packages running on PCs give access to a range of tools and data residing on Unix platforms, albeit at lower levels of interactive, graphics performance than the workstations. For such activities as schematic capture and project management, where access is more important than real-time data sharing, X-Windows will become another tie into the engineering environment. X-Windows doesn't take advantage of the PC's processor, so it will introduce more demands on the network compute server. In effect, the X-Windows PCs will become the new time-share terminals. Future CE environments will combine PCs running applications, PCs running X-Windows, and workstations.

Productivity and competitiveness will be further improved by intercon-

necting entire organizations, from the IBM mainframe in the finance department to the Apple Macintosh computers in marketing *(Fig. 2)*. Network vendors are already introducing "integration platforms" that can link all functions within a company. Through products like multiprotocol routers, companies will be connecting what used to be islands of functionality into distributed networks. Moreover, as the boundaries of networks change, the notion of a static network will no longer be applicable. As they evolve in the next five years, data-management and tool-management services will be able to work across constantly evolving groups and departments.

Finally, as all computing platforms come onto the network, network technology will evolve to harness all available computing power for every user. This move to distributed processing will depend on the development of software that can manage the access to computers transparently to the users—the network appears as one big computing resource. Organizations like the Object Management Group (OMG) are setting the standards to assist this software development process.

For example, the OMG's Object Request Broker (ORB) defines the mechanisms whereby a networked environment can transparently manage and arbitrate all of the requests for resources on the network. By allowing the network to assign tasks to available computer platforms, companies can exploit all available CPU cycles. And by dynamically matching tasks to resources, the ORB also deals with the changing network topology and resources.

Global Networks

The third advance in network technology will be the growth of reliable global network connections. Until recently, trying to send tens or hundreds of megabytes overseas across telephone lines resulted in error rates too high to complete the transaction. And the cost of interconnecting more than one site within a particular geographic region to sites in other regions was too high for linking worldwide organizations.

Fortunately, intercontinental rates have already improved. For example, Mentor Graphics' software engineers at Wilsonville, Ore., can release new versions of software via a network connection to Tokyo, Japan for local customization. As recently as a year ago, the software would have been written to tape, and then the tape would be mailed—a three-day turnaround. A direct satellite link has since reduced the turnaround to overnight, a dramatic improvement that can simplify work across two continents.

However, this link is still not fast enough for real data sharing. Today's leased-line interconnections can reliably transmit only 1 Mbits/s. Just like LAN bandwidths, this rate is far too slow for effective data sharing. By 1995, these interconnections will improve to about 10 Mbits/s, making data sharing across an ocean much more feasible.

Special connections (such as T1 links) will remain too expensive for connection to all potential intracontinental sites. Fortunately, the coming digitization of the phone lines

THE DIMENSIONS OF CONCURRENT ENGINEERING

Concurrent Engineering is more a complete corporate philosophy than just a design methodology. It requires organizing the team members, tools, and data to facilitate a constant exchange of ideas and design choices. To quantify its extent in today's companies, Don Carter defined four dimensions of concurrent engineering in his book, *Concurrent Engineering: The Product Development Environment of the 1990s* (Addison-Wesley Publishing Co., New York, N.Y., 1991). The four dimensions are:

- *Organization* This dimension outlines the relationship of the group members within the multidisciplinary teams. Engineering managers create, empower, and support a team whose composition is created for the specific product. The team members themselves assume the authority and responsibility for their design decisions, and they toil toward shared, explicit goals.
- *Communication infrastructure* This dimension links people, ideas, specifications, processes, and feedback paths. It includes formal and informal contacts among members, and the mechanisms that assist the interaction. The communication infrastructure facilitates the flow of decisions within the other three dimensions.
- *Requirements* This dimension spans the total set of industry, company, and particularly customer requirements for a product. Elements defined in this dimension determine what a customer wants, ensure that the customer is getting it, and apply internal and external standards to the product's design.
- *Product development* This dimension defines the total product development process—from design conception to manufacturing and support. It includes specific aspects like component libraries, downstream impact of design decisions, and continuous improvement of the development process.

In a balanced concurrent-engineering environment, these dimensions are in relative harmony. Most often, this harmony occurs in design teams of one person, in which communication of specifications, trade-offs, and processes is inherent. As an increasing number of individuals become involved in the product development, every dimension becomes more and more complicated. For teams of experts collaborating on a design, technology like computer-aided design (CAD) frameworks and computer networks are necessary underpinnings to formal concurrent-engineering practices.

will provide lower-cost, high-bandwidth connections to all sites within a particular country or continent. Within the next ten years, every telephone will have the potential to access the network using digital telephone lines, making it more cost effective for companies with worldwide facilities to link all of their personnel by networks.

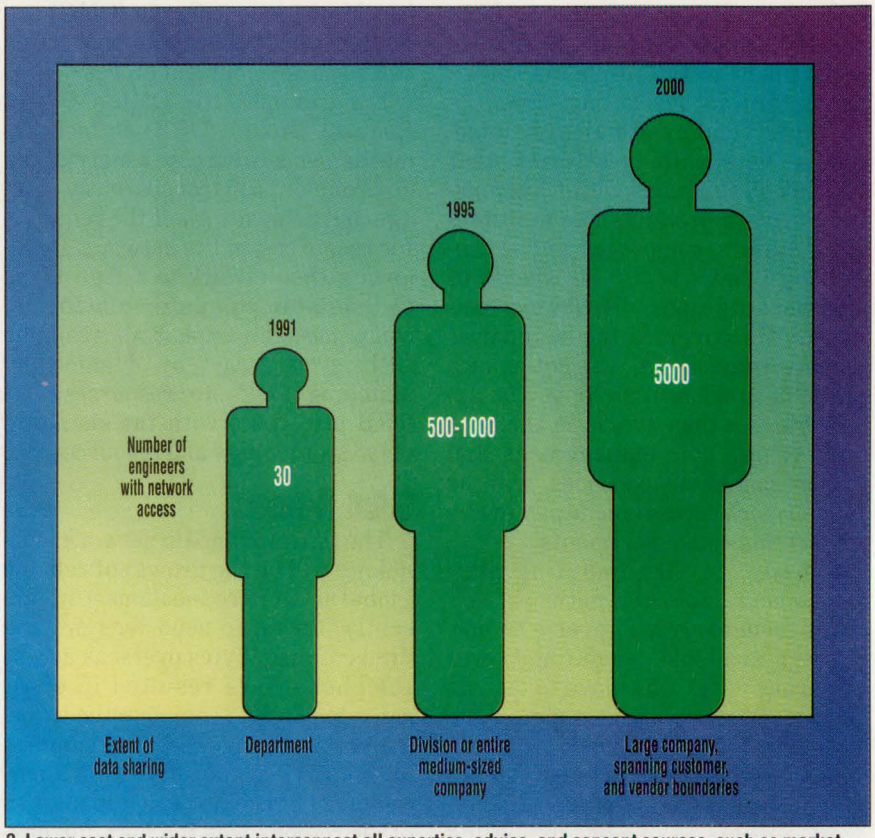
The Global Connection

These network advances will help companies automate concurrent engineering more completely. Therefore, all company resources that can assist in product development will interact more efficiently. Even overseas talent will become part of the design team. At the same time, companies will have to develop more powerful data and team-management tools to coordinate these expanded opportunities.

The most obvious impact will be in the Communication Infrastructure dimension. Every platform, at home or in the office, here or abroad, will be touched and enhanced by the design-automation environment.

Lower cost and wider extent will improve links to all sources of expertise, advice, and consent. Low-cost connections will bring marketing, purchasing, and other functions in closer contact with the design team. Collaboration will extend to all possible customer needs, enhancing the Requirements dimension.

With more sites connected more inexpensively, customers and vendors will become information brokers for the development process. By the year 2000, entire corporations as well as their customers and vendors will be able to share ideas and resources over networks *(Fig. 3)*. Customers can relay requirements and orders more quickly and regularly. Design teams can collaborate with suppliers for more exact estimates of cost and delivery. As the whole product life cycle becomes linked by networks—from vendor to customer—the Organizational dimension of concurrent engineering grows. This means that design project managers will have to plan for the input and feedback from customers and vendors as well as all disciplines in the design team.



2. Lower cost and wider extent interconnect all expertise, advice, and consent sources, such as marketing, purchasing, manufacturing, other development groups, and even customers and suppliers.

The dynamic nature of the networks will grow with their wider range. It will become more difficult to pin down the exact collection of network resources at any one time. As a result, companies will need to plan for replication of services. This replication will include hardware resources like printers and compute servers, and software resources like applications and network management tools, all of which will need to be replaced and updated regularly.

Global Design Teams

The second major impact of the network advances will be the proliferation of international design teams. With high-speed network links between continents and cost-effective digital telephone links, geographic proximity will become of less importance to group dynamics. This change will directly expand the Organizational dimension of concurrent engineering—literally.

While some companies already field experts in multiple countries, today's technology (i.e., facsimile machines and high-cost, centralized network connections) severely limits the rate of interaction among team members. When networks can pass millions of bits per second reliably from Minneapolis to Manila, team members will share large portions of the design database as easily as if they were located right down the hall from each other.

Furthermore, two-way video technology will make desktop meetings an effective way to collaborate overseas. The distinction between meeting locally or remotely will become less important. At Mentor Graphics, two-way video facilities between company sites has already proven more efficient in day-to-day business than travel. Unfortunately, limited access to the video facilities prevents its use for ad hoc communication. With computer monitors on every desk, video communication will be available to everyone, just like a telephone.

As companies master the management and dynamics of international

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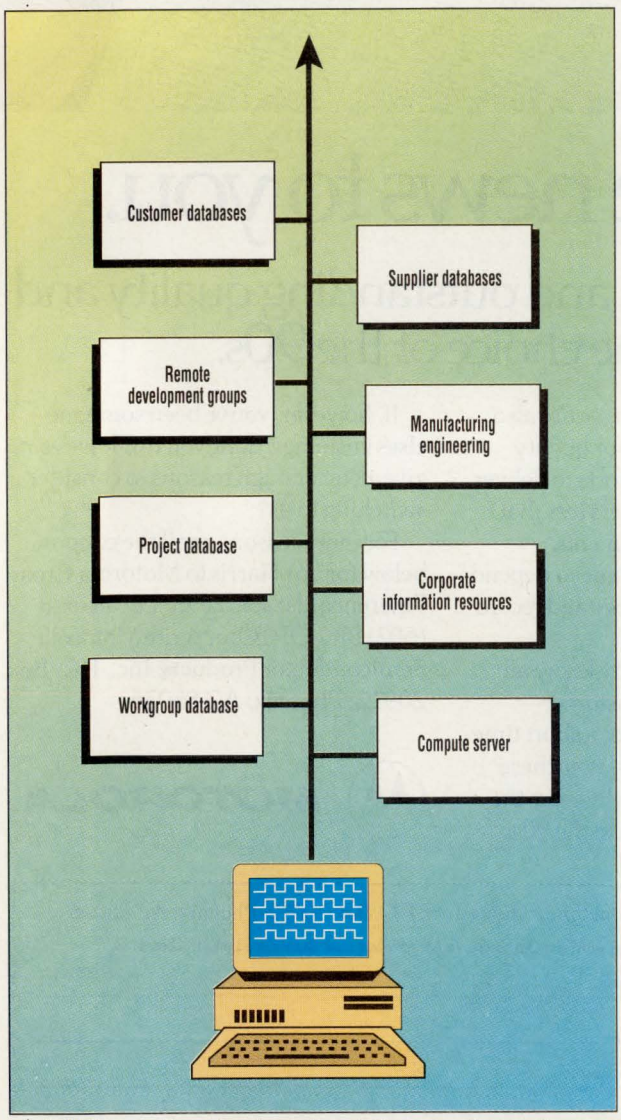
design teams, the option will open up to compress the design schedule by using more hours in each day. When a design team completes a work day in San Jose, for example, its current data could be accessed by a team in Tokyo to continue the effort.

Then the design database could move on to Paris for more continuous effort, and back to San Jose the next day. The logistical challenge of such an arrangement will be a necessary trade-off given contracting market windows.

Finally, international design efforts will simplify the customization of products for local markets, as well as simplify the use of local parts suppliers and local engineering talent.

A third impact of the network advances will involve the rapidly growing number of users, databases, and resources available across the network. Node counts will grow from hundreds to thousands or tens of thousands. Companies will begin measuring on-line data storage in terabytes. And applications will have the option of interacting with any of hundreds of other applications, peripheral hardware like printers, and a variety of databases.

These trends will create problems in just finding data and resources. Enormous amounts of computing platforms exist on the network—if the exact name and location of what's needed isn't known, then it won't be found. To deal with this issue, extensions to the network operating systems are under development to assist in tracking and accessing global resources.



3. With expanding network speeds and interconnections, entire corporations as well as their customers and vendors will be able to share ideas and resources over networks.

The object-oriented paradigm embodied in the Object Request Broker shows one solution to this problem. It provides a basis for software developers to create programs that communicate with objects, not specific programs or databases. The networks can then manage the communication between objects, locally or distantly. The ORB, for example, will contain a mechanism to manage naming conventions across multiple domains, providing translation services if necessary.

Locating available sources of compute power will also require a standard management mechanism. Some applications, like Mentor Graphics' QuickFault fault simulator, CheckMate IC verification system, and Parade place-and-route tool, can already distribute computing tasks among multiple nodes on a LAN. Each of these examples, however, does so on its own. In the future, the ORB will offer a more standard approach that will be able to replicate this feat on a much grander scale.

For engineering environments in particular, the CAD framework will provide further levels of access and management. It will define specific mechanisms for design team members and tools to access data and resources within the concurrent-engineering process. The CAD framework will be able to track the creation of data, control its versioning and archiving, and notify relevant users and applications of the existence of this data. Particularly, in the CAD Framework Initiative (CFI) model for inter-tool communications, tools will register with other tools when specific kinds of data are available. The difficulty lies in defining how and when specific tools and types of data should interact.

The Decision Support System (DSS) within Mentor Graphics' Falcon Framework is a first step in this direction. It provides a graphical method to put together a monitoring function without much programming. And it helps design engineers to query information from a multidisciplinary database and process it according to proprietary procedures.

These three impacts of networking technology will help push companies to the second phase of CE transition. With all computing platforms linked across the network, companies can start standardizing database access, user interfaces, and sharing the processing power of computers. They can achieve consistency and interactivity in their methods of communicating and manipulating information. And interoperability standards like the Object Request Broker will help create applications that start to take advantage of the huge number of resources available across the network. The end result is an interoperable computing environment. This new phase of automated concurrent

engineering will improve the efficiency and productivity even more than the first stage.

Companies will optimize use of personnel, data, and capital. Economies around the world have distinct specialties: engineering in some quarters, for example, and manufacturing in others. Global companies will have more flexibility in applying computers and experts to concurrent-engineering projects. For example, many EDA companies are already contracting more software programming to the well-educated pool of computer professionals in Asia.

Productivity and efficiency will also grow with the close collaboration between vendors and suppliers. For example, electronics companies will be able to easily transfer entire databases for evaluation by customers. Vendors could provide on-line, up-to-date catalogs of parts, and provide more accurate quotes.

For an analogy, the automobile industry has been establishing such links in the 1980s. Instead of designing all parts and putting out a request for bids, automotive designers can release design specifications and drawings for parts to potential suppliers and quickly get feedback on manufacturability and cost. This allows several iterations between the design group and the supplier before the parts are committed to production. In the electronics industry, such cooperation may involve the development of ASICs, subsystems, and system software.

Moving to higher levels of concurrent engineering will magnify its ultimate benefits: Cooperation of all experts to create a higher quality, more valuable product; defining and streamlining procedures for faster design cycles; and reducing design iterations and fixes to build a more cost-effective product. Networking and automated concurrent engineering will work together to bring about these benefits.□

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MICROPROCESSOR ARCHITECTURES WILL EVOLVE IN THE 90s

SOFTWARE COMPATIBILITY WILL DRIVE FUTURE ARCHITECTURES.

MICHAEL SLATER
Michael Slater is the editor and publisher of Microprocessor Report (Sebastopol, Calif.), an independent newsletter on microprocessor technology, and acts as a consultant on microprocessor-related strategic issues. He also organizes the annual Microprocessor Forum conference.

The 1990s have made way for a rich assortment of microprocessors and architectures, ranging from low-cost 4- and 8-bit designs to powerful 32-bit chips, along with a spectrum of architectural styles from classic RISC chips to the complex 80386 and its successors. While the temptation to invent entirely new architectures persists, the general-purpose computing market will be dominated for most—if not all—of the decade by evolutionary descendants of existing designs.

From the earliest microprocessors dating back to 1971 to the 32-bit CPUs that emerged in the mid-80s, microprocessor architectures underwent radical changes. Because the early architectures were highly constrained by the limits of silicon technology, major revisions were needed to continue the quest toward high performance.

Today's 32-bit architectures don't beg for change as their predecessors did. Some aspects of current designs—such as delayed branches—are less than optimal for next-generation, superscalar implementations, but microprocessor designers will accept these blemishes in return for access to a large software base. Availability of application software is key in the battle among general-purpose microprocessors, and the benefits of compatibility with existing software will likely outweigh the gains promised by radical architecture changes. This driving force has allowed Intel's 386/486 series to dominate desktop computers in the face of countless competitors armed with more modern architectures.

Although entirely new architectures will likely be limited to small niches, all architectures will evolve, adding new features in ways that maintain compatibility with existing software. By the mid-90s, most high-end architectures will be enhanced with 64-bit addressing and 64-bit integer arithmetic capabilities. The MIPS R4000 was the first processor to offer these features. Other recent architectural enhancements include the Version 1.1 extensions to HP's "Snakes" PA-RISC implementation; the SPARC version 8 extensions seen in TI's SuperSPARC and other future SPARC chips; and the PowerPC revisions to IBM's RS/6000. The PowerPC's alterations simplified the architecture for lower-cost, higher-integration implementations. In the other cases, the extensions fill gaps in the original architectures, such as SPARC's lack of multiply and divide instructions or the R4000's lack of interlocked loads and synchronization primitives.

The most exciting microprocessor prospects for the next decade aren't in instruction-set architecture, but in implementation. Superscalar designs will decode, dispatch, and execute several instructions per clock cycle—possibly as many as three to five instructions per clock. These gains will come slowly and painfully, though, because the limited amount of parallelism in typical programs makes it difficult for a superscalar machine to reach its potential. The biggest gains will be realized by combining superscalar processors with compilers designed for such implementations. Out-of-order and speculative execution techniques will also help extract maximum performance.

Increasing integration levels will reduce system chip count as well as bolster performance. By mid-decade, the single-chip PC or "PC-on-a-chip," which require only external memory and some I/O buffers, will dominate mainstream systems. Merging microprocessors with core logic will all but eliminate the chip-set business as it's known today. A proliferation of different processor and system-logic chips will appear using standard CPU cores, but with different combinations of on-chip memory and peripherals optimized for particular applications.

Eventually, an entirely new class of architectures should emerge, just as RISC did in the 1980s, but probably not until well past the middle of the decade. The new architectures will supply sufficiently powerful benefits to overcome the software inertia. The focus of the 1990s, however, will be on faster and more integrated implementations of today's architectures, and evolutions of those architectures.□

PASSIVE- AND ACTIVE-MATRIX LCDs TO DOMINATE FLAT-PANEL DISPLAYS

PLASMA AND ELECTROLUMINESCENT PANELS, AS WELL AS CRTs, WILL ALSO FIND APPLICATION NICHES.

LAWRENCE E. TANNAS, JR.
Lawrence E. Tannas, Jr., president of Tannas Electronics, Orange, Calif., is an internationally recognized consultant and lecturer on electronic information displays. Prior to his becoming a consultant in 1983, he worked for over 20 years in the displays and controls industry. He holds BSEE and MSEE degrees from UCLA.

Advances in flat-panel displays (FPDs) are progressing at a breakneck pace, with most coming from Japan, where the focus is on liquid-crystal displays (LCDs). Several Japanese companies have invested over two billion dollars in FPD technology, building large factories to manufacture LCD FPDs. These include compensated supertwisted nematic (STN) LCDs with passive matrices aimed at moderately priced computer-graphics applications. Also included are amorphous-silicon (a-Si) thin-film-transistor (TFT) active-matrix displays, designed for higher-priced color TVs and high-quality imaging applications. By the year 2000, these two types will dominate FPDs—two-thirds of all FPDs sold at that time will be LCDs.

STN LCDs will be fabricated on production lines similar to those presently being used to make TN LCDs. But a-Si TFT LCDs will require a brand new class of production methods and machines. Creating the TFTs and circuit-board-size glass substrates will require micron-photolithography precision. And to produce the a-Si material, expensive 350°C thin-film plasma-etching chemical-vapor-deposition equipment will be needed.

Japan is also producing polysilicon TFT LCDs for camcorder viewfinders and projectors, as well as metal-insulated-metal (MIM) LCDs. Electrically controlled birefringent LCDs, as well as ferroelectric LCDs, have been developed and demonstrated and will soon be committed to manufacture. And polymer-dispersed liquid-crystal material is being studied for overhead-projector LCDs.

Plasma display panels (PDPs) and electroluminescent (EL) displays, which compete with LCDs, are two other areas being exploited. But developments in high-information-content (HIC) LCD panels will change this picture during the 1990s. The number of production-quantity HIC LCD panels now exceeds PDPs by approximately an order-of-magnitude, and EL panels by two orders-of-magnitude. Furthermore, there's been no increase in the production capacity of PDPs or EL displays. That's because PDPs and EL displays cost more than LCD FPDs, and they still don't have color in production. Until they do, these displays will be relegated to the custom medical and industrial markets.

But PDPs and ELs continue to be applied in custom industrial and workstation applications, where ruggedness and high performance are required. Each type has inherently long life and a wide operating temperature range. In addition, each has wider viewing angles, is faster and brighter, and has more contrast than any LCD configuration.

CRTs will coexist with, rather than replace, FPDs. FPDs can't compete in price with CRTs at the low end, nor in performance at the high end. For comparable performance, FPDs cost five to ten times the cost of CRTs. As a result, LCD FPDs will be limited to displays having 3- to 18-in. diagonals during the 1990s. Compensated STN LCDs will tackle 3- to 18-in. panels with some graphics performance and limited color, and a-Si TFT LCDs are intended to address 3- to 16-in. panels with video performance in color. CRTs will be very cost-effective for display sizes of 36 to 40 in.

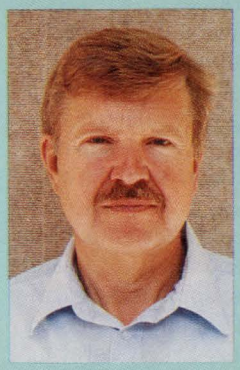
Consumer-priced TVs-on-the-wall aren't feasible before the year 2000, due to technical barriers and manufacturing costs. And only somewhere around the year 2000 will large direct-view color HDTV FPDs be slated for production. CRT and LCD projectors will compete for the large-size HDTV market.

With few exceptions, Japan's domination of the LCD FPD market can be traced to its research and development into high-volume production. The few exceptions are Philips in the Netherlands, which recently announced that it's constructing an active-matrix LCD factory in Eindhoven, and Seiko Instruments of Japan, which just built a factory in Italy to manufacture passive-matrix LCDs. Companies in the U.S. and other countries have delayed and avoided making the necessary investment in FPD technology. Still, it's not too late for them to become more aggressive.□

These observations are based on two study trips to Japan by this author, in May and November, 1991, as part of two U.S. National Science Foundation panels on HDTV and HIC displays.

DESIGNERS WILL BE PAYING MORE ATTENTION TO EMC TESTING

ELECTRONIC EQUIPMENT WILL HAVE TO MEET TOUGHER ELECTROMAGNETIC COMPATABILITY RULES.



SIEGFRIED LINKWITZ
Siegfried Linkwitz is a senior engineer working on products for diagnostic and compliance testing for electromagnetic interference at Hewlett-Packard Co.'s Signal Analysis Div. He graduated from the Technical University in Darmstadt, Germany with a diplom ingenieur degree in electrical engineering. Linkwitz is a member of the U.S. Standards Committee on Electromagnetic Compatibility.

Worldwide, the electronics industry must pay increasing attention to electromagnetic compatibility (EMC) to comply with new European Community (EC) regulations. Any manufacturer that wants to sell to EC countries must comply with the EC rules, which are expected to be implemented between 1992 and 1994. The regulations not only cover product classes that were regulated in the past, but also include generic standards for products not previously included.

Furthermore, the EC rules include new standards for immunity from electromagnetic emissions, as well as limits on emissions. Many manufacturers will have to set up new test facilities, acquire new test equipment, and develop new test processes to characterize a product for immunity.

The need for more compliance tests will increase the desire to automate EMC testing. Every EMC test department already uses personal computers or workstations to archive test data, generate test reports, and often to control test equipment. But much of today's software requires a fair amount of operator intervention and decision making because of the unknown character and complexity of the signals being investigated. Future software will become more powerful, leading to increased automation capabilities.

The trend towards automation is supported by new test facilities that simplify EMC characterization. Traditional radiated-emission testing on an open-area test site (OATS) is plagued by ambient signals that make it difficult to identify emissions from the device under test (DUT). Therefore, designers will increasingly turn to small, shielded rooms free of ambient-signal interference to evaluate a product to a first order, and to determine the emission frequencies before proceeding with an OATS test.

In addition, shielded rooms will be needed to contain the strong electromagnetic fields required for radiated immunity tests. When fully lined with absorbing material—including the metal floor, which acts as a groundplane—these anechoic rooms will offer the field uniformity needed for immunity tests. Eliminating the ground plane will also simplify radiated-emissions testing.

Not only will test facilities see further development, so will the measurement processes and the test equipment. In general, instruments will become easier to use when they're able to execute complex measurement sequences automatically. Test equipment will also become more specialized or configurable for tasks like testing the immunity to electrostatic discharge or power-line transients and surges.

The widely used OATS measurement will also be simplified. OATS testing will benefit from smarter measurement-automation software and from processes that can distinguish between ambient and DUT signals and can quickly find the maxima of emissions from moving turntables and towers.

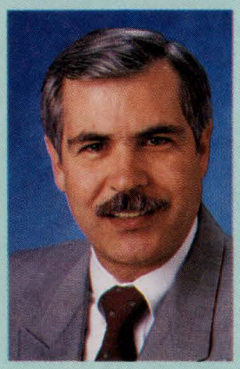
Finally, the effect of EMC education and training on the task of EMC testing should not be underestimated. Some universities are beginning to offer specialized courses in EMC, adding to the great number of seminars already offered by EMC consultants. These courses create a better understanding of how to solve EMC problems once they've been detected during testing. More important, though, the courses teach the value of good EMC design at an early stage in the product-development process.

As a result, more emphasis will be placed on precompliance testing. Such testing requires readily accessible test facilities, such as a GTEM (gigahertz transversal electromagnetic field) cell or anechoic room. It also requires test equipment that's easy to use not only for the EMC specialist, but also for the product designer who only uses it occasionally during the product development cycle.

In summary, the trend in EMC testing leans toward automation to achieve greater product throughput and reduced product development time and cost. These goals will be achieved by more suitable test facilities, smarter and simpler instrumentation, and ultimately by greater knowledge about effective, economical EMC design.□

SILICON MICROSTRUCTURES: NEW TECHNOLOGIES, NEW MARKETS

MICROMACHINED SENSORS ARE NOW HERE IN VOLUME; COMPLEX SILICON ACTUATORS ARE CLOSE BEHIND.



KURT PETERSEN
Kurt Petersen is a founder and vice president for technology at Lucas NovaSensor, Fremont, Calif. He began his career in micromachining at IBM Research Laboratories, San Jose, Calif. Petersen received a BS in electrical engineering from the University of California at Berkeley and an MS and ScD in electrical engineering from the Massachusetts Institute of Technology, Cambridge.

Silicon micromachining has launched a whole new industry that's revolutionizing sensor and actuator fabrication. The technology of sculpturing tiny, intricate 3D structures from silicon is rapidly taking over the sensor market. Today, a vast array of silicon micromachined sensors is available. Though pressure sensors are dominant now, many other sensor types are emerging. And micromachined actuators loom on the horizon. Some day, we'll see sensors, actuators, and their processing circuitry—a closed-loop control system—all on the same chip.

Many technical problems that held back high-volume manufacturing viability of silicon micromachining are now behind us, as was proven in the automotive and medical industries where micromachined silicon sensors abound. Over 25 million silicon micromachined pressure-sensor chips are annually fabricated worldwide. Their diverse applications include automotive manifold pressure sensing, intensive-care disposable blood-pressure sensing, depth measurements for scuba divers, altimeter sensing, gas- and fluid-pressure sensing for industrial-process control, and sensing for aerospace engine control. Other new applications continue to progress, such as medical angioplasty, home blood-pressure cuffs, automotive oil- and tire-pressure measurement, and so on.

Expansive growth is also projected for solid-state micromachined acceleration sensors, particularly for automotive applications. The two primary applications are low-G sensors for suspension control and high-G sensors for crash detection in air-bag systems.

A significant outgrowth of micromachining is silicon fusion bonding (SFB), a technique that bonds two silicon wafers together into one substrate with no intermediate bonding materials. In SFB, the final assembly behaves as one uniform, single-crystal silicon structure. Because both silicon substrates can be micromachined before and after bonding, complex and versatile microstructures can be created. And since the mechanical structure is silicon, all of the sensing technologies and capabilities developed over the past 20 years are directly applicable. This has allowed the quick introduction of high-performance pressure and acceleration sensing chips based on SFB technology. Applications range from the space shuttle to cardiac pressure sensing (the world's smallest) to automotive acceleration sensors.

A recent silicon micromechanical-processing technology that deserves close scrutiny is surface micromachining. Here, an alternating series of thin insulating polysilicon layers are sequentially deposited and patterned. The insulating material is then etched away, leaving miniature, 3D mechanical features suspended less than a micrometer above the silicon wafer's surface. Deposited polysilicon films have created the most sophisticated micromechanical devices yet, including an electrostatic silicon micromotor. Freely rotating polysilicon rotors, about 2 μm thick, less than 100 μm in diameter (about the diameter of a human hair), are now routinely built and operated in university labs.

A number of key indicators have substantiated the worldwide significance of silicon sensor and micromachining technologies. A soon-to-be-released study by Battelle Europe determines that about 300 companies, research organizations, and universities are engaged in these technologies. And while a recent study by the U.S. Congress' Office of Technology Assessment strongly recommends federal funding of critical commercial industries, including micromachining, the German government has already scheduled investments of about $60 million a year through 1993. Japan's Ministry of International Trade and Industry (MITI) has provided $200 million in total funding for sensor and micromachining R&D.

With the maturing of the silicon sensor industry, sensor-manufacturing quality standards are finally being improved. Customers aren't satisfied with "percent" defect levels, the previous norm of the industry. No sensor manufacturer will survive the 90s without a commitment to company-wide Total Quality Control programs.□

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CIRCLE 216 FOR U.S. RESPONSE

CIRCLE 217 FOR RESPONSE OUTSIDE THE U.S.

CHOOSING INSTRUMENT ACCURACY BECOMES MORE COMPLICATED

SEVERAL FACTORS WILL CHANGE THE WAY DESIGNERS LOOK AT TEST-EQUIPMENT ACCURACY

KRIS JONES
Kris Jones, senior product planner in John Fluke Mfg. Company's Service Equipment Group, received her BSME from the University of Colorado. Before joining Fluke, Jones served in various engineering and marketing capacities at Hewlett-Packard Co.

The rapidly increasing electronic content of so many everyday items—such as automobiles, appliances, motor controllers, alarm systems, and industrial process controllers—creates many complex challenges for designers. Not the least of these is determining the accuracy of the test tools used to design, manufacture, and troubleshoot these systems. Cost constraints force most users to trade off accuracy against other desired features.

An ideal measurement could be made by comparing it against an accepted reference standard, such as those maintained by the National Institute of Standards and Technology. But obtaining and maintaining such a standard isn't practical for most users, so they must rely on an instrument's accuracy specifications to tell them how close their measurements are to the ideal value.

However, many variables other than an instrument's specified accuracy can introduce errors into real-world measurements. Some obvious factors are the general maintenance of test equipment and environmental conditions during a measurement, such as temperature, humidity, and pressure. The specific method used to take the measurement can also introduce errors. Factors like the type, size, and location of sensors or transducers can greatly affect measurement accuracy.

In addition, characteristics of the property being measured may affect measurement accuracies. For instance, a growing number of nonlinear loads—PCs, electronic office machines, ac and dc adjustable-speed motor drives, and so forth—are used in homes, offices, and manufacturing facilities. Because these nonlinear loads can result in complex waveforms in power-distribution systems, understanding the characteristics of the signals being measured is growing increasingly important for accurate measurements.

For example, an accurate average-responding multimeter, calibrated to the RMS value of a sine wave, may give inaccurate readings for power-distribution systems containing harmonics caused by nonlinear loads. In this case, more accurate readings might be taken using a true RMS multimeter, which can measure signals with nonsinusoidal waveforms. The signal must, of course, be within the meter's bandwidth and crest-factor specifications. This growing signal complexity is leading some users toward test instruments that can display waveforms, as well as accurately read out true RMS voltage or current values.

In addition to changes in power-distribution systems, the increasing complexity of electronic equipment is affecting the accuracy required of test equipment. For example, the growing use of surface-mount technology and ASICs makes for more complicated and costly troubleshooting during design, manufacturing, and field service. Some companies are responding by developing built-in self-test circuitry for ICs, circuit boards, and even complete systems.

This trend is a factor in the accuracy required of test equipment because in some industries, built-in self-test has led to several levels of troubleshooting, with different accuracy requirements. In the mainframe industry, for example, first-level troubleshooting may involve a technician going to a customer site to exchange a circuit board that has failed the computer's self-test. This "field service" technician may require only very basic test tools. A second-level "depot repair" technician may next troubleshoot this board to the component level, using more accurate and sophisticated test tools to find the cause of the failure.

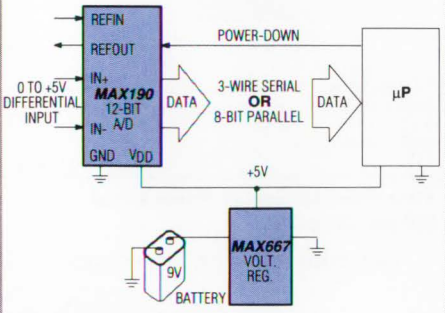
This two-tier scheme suggests that designers of test equipment should be prepared to serve two divergent markets. One requires simpler, less accurate, and less costly meters for use by first-level technicians. The other demands more sophisticated instruments for use by high-level persons facing increasingly complex troubleshooting problems.

Selecting the best test tools for a given application involves trade-offs between budget and performance, consideration of tools being used successfully by others in similar applications, and a look at emerging technologies that may affect future requirements.□

MAXIM DESIGN NEWS
Analog Design Insights from Maxim Integrated Products No. 23

Analog Solutions For Tough Design Problems

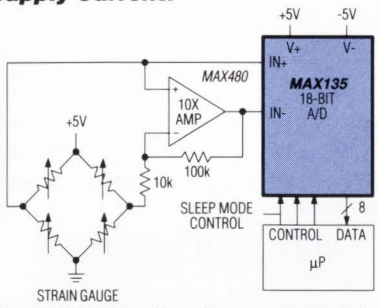
Fastest, +5V-Supply 12-Bit ADC



The **MAX190** converts rail-to-rail signals to either serial or parallel data in 7.5µs on battery power. Precision laser-trimmed reference, clock and track/hold included on-chip. The MAX190's already-low 15mW power consumption is reduced to 150µW during shutdown.

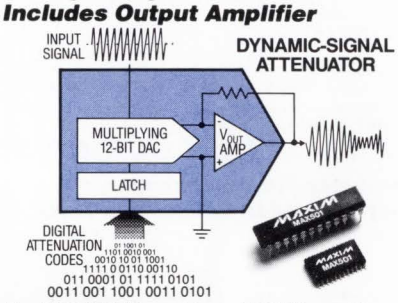
(CIRCLE 246)

15-Bit ADC Uses Only 125µA Supply Current!



The **MAX135** low-noise, 5V-powered, multi-slope integrating ADC provides ±0.005% accuracy at 16 conversions per second, while requiring only 125µA of supply current over temperature (10µA in sleep mode). Resolution is extended to 18 bits with 3 sub-LSB bits and data averaging. 8-bit data bus and 3 logic control lines simplify µP interfacing. **(CIRCLE 247)**

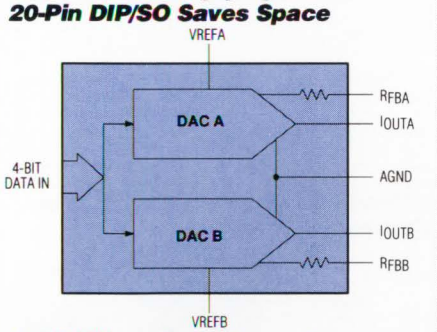
4-Quadrant Multiplying Voltage-Output 12-Bit DAC Includes Output Amplifier



The **MAX501/502** combine a BiCMOS amplifier with ±10V drive capability and a laser-trimmed, thin-film-resistor DAC on a single chip. These DACs accept a DC or AC reference and have buffered input latches that are easily interfaced to both 8-bit (MAX501) and 16-bit-wide (MAX502) data buses.

(CIRCLE 248)

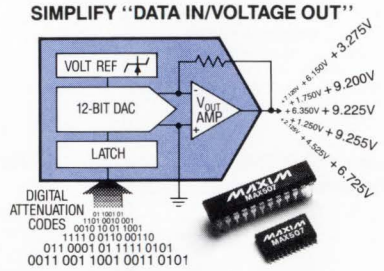
Dual 12-Bit Multiplying DAC in 20-Pin DIP/SO Saves Space



The **MX7549** current-output, four-quadrant multiplying DAC features 1% resistance match between DACs, making many dual applications possible. The new DAC has ±½LSB max integral nonlinearity, ±5ppm/°C max gain temperature coefficient, and operates from a single +5V to +15V supply. Pin compatible to AD7549.

(CIRCLE 249)

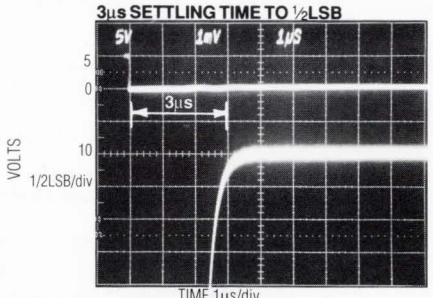
Complete 12-Bit Voltage-Output DAC Includes +5V Reference



The **MAX507/508** combine a laser-trimmed DAC, a high-performance BiCMOS output amp, and a buried-zener voltage reference on a single IC, greatly improving reliability compared to multi-chip solutions. Data is transferred into the input register in 8+4-bit (MAX508) or 12-bit (MAX507) wide data formats.

(CIRCLE 250)

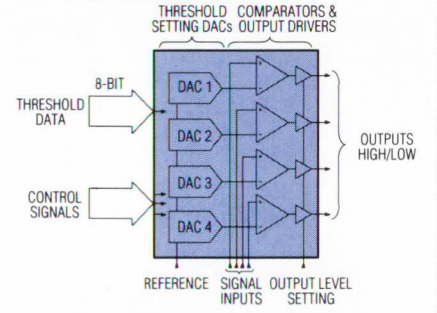
Quad 12-Bit Voltage-Output DACs Replace 8 Components!



The monolithic **MAX526** replaces 4 DACs and 4 op amps. Monotonic 12-bit performance guaranteed with ½LSB relative accuracy over temperature for all 4 outputs and 1LSB total unadjusted error with no zero- or full-scale adjustments at +25°C. Outputs settle to ½LSB in 3µs.

(CIRCLE 251)

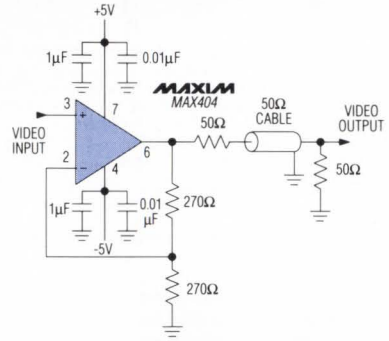
Four Comparators With On-Chip DAC Adjustable Thresholds



New **MAX516** automates calibration, minimizes part count with 4 BiCMOS comparators with DAC-programmed input thresholds in a single device. Features include 0.4% resolution, 1.5µs propagation delay and 50mW max power consumption.

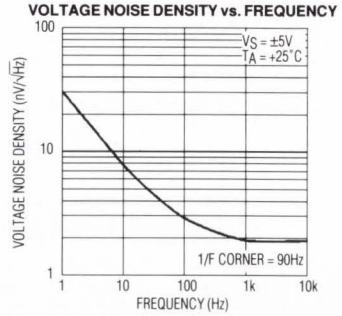
(CIRCLE 252)

Broadcast Quality Video Op Amp



The **MAX404** video op amp has 0.01° differential phase and 0.05% differential gain while operating from ±5V supplies. Featuring 80MHz gain-bandwidth and 500V/µs slew rate, this amplifier is ideal for video and other high-speed applications. 50mA continuous output current is guaranteed. **(CIRCLE 253)**

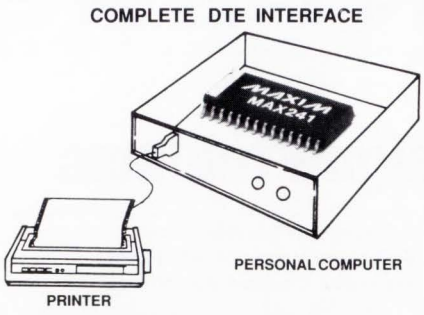
Lowest Noise Dual Op Amp For 5V Systems



The **MAX412** provides the **best noise performance** — even at very low supply voltages. <2.4nV/√Hz @ 1kHz noise guaranteed! With a guaranteed output voltage swing of 7.3VPP and greater than 97dB SINAD (Signal/THD+N) while operating from ±5V supplies, the MAX412 is ideal for 5V systems. 8-pin DIP/SO.

(CIRCLE 254)

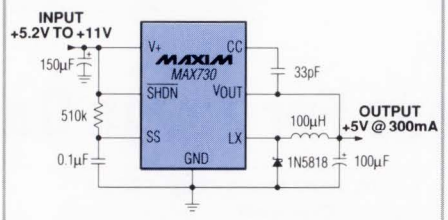
Complete +5V Serial Port IC With 1µF External Caps!



The **MAX241** is a complete serial port on a single chip. It features 4 drivers and 5 receivers in a 28-pin SO package. A separate shutdown mode reduces supply current to a mere 1µA.

(CIRCLE 255)

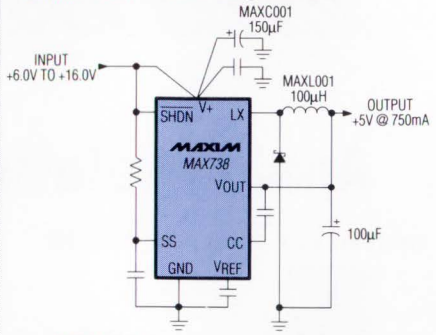
Small +5V PWM Regulator Has 94% Efficiency!



The **MAX730** is the smallest complete PWM step-down available. Its 8-pin SOIC package and all surface-mount external components fit into 0.55 square inches. It delivers up to 300mA from 5.2V to 11.0V inputs with 94% efficiency.

(CIRCLE 256)

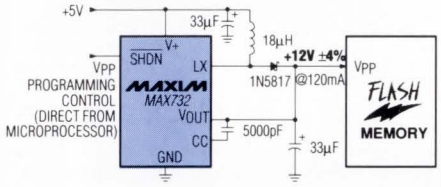
Guaranteed 750mA Output From Small +5V PWM Regulator



The **MAX738** PWM step-down switching regulator is ideal for high-efficiency step-down applications. It has a 6V to 16V input voltage, up to 750mA output current, and 88% efficiency.

(CIRCLE 257)

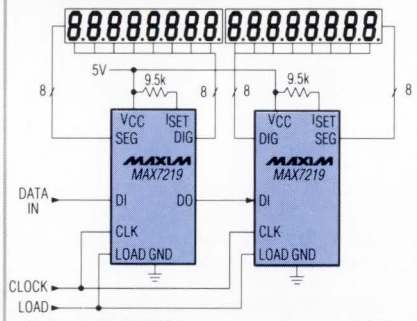
Complete Flash Memory Programmer In 1/2 Square Inch!



The **MAX732** 200mA step-up regulator is a simple, compact flash memory programming supply that has direct µP-controlled shutdown. It will step up from +5V to +12V±4% at 200mA with 88% efficiency. Pre-assembled evaluation kit available.

(CIRCLE 258)

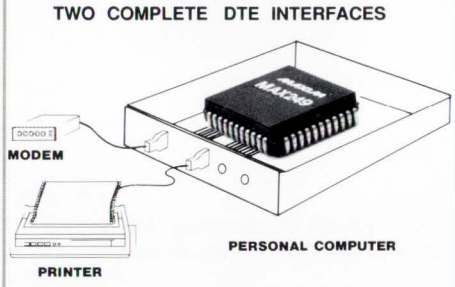
8-Digit 10MHz LED Display Driver Works With Any µP!



The new **MAX7219** has an easy-to-use serial 3-wire interface and digital/analog brightness control. Only one external resistor is required to set the segment current for all LEDs. The MAX7219 has 1kHz per digit scan rate and is available in a compact 24-pin SO package.

(CIRCLE 259)

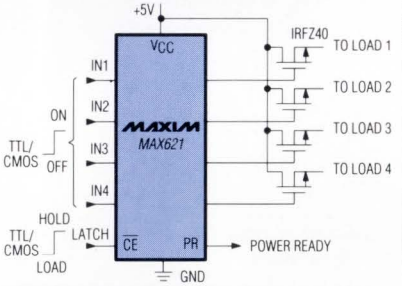
Two RS-232 Serial Ports On A Single Chip!



The **MAX249** has 6 drivers and 10 receivers — two complete Data Terminal Equipment (DTE) serial ports on one chip, making it ideal for space-critical applications. Plus, the MAX249 uses space saving 1µF capacitors and is guaranteed to operate at data rates up to 64kb/s.

(CIRCLE 260)

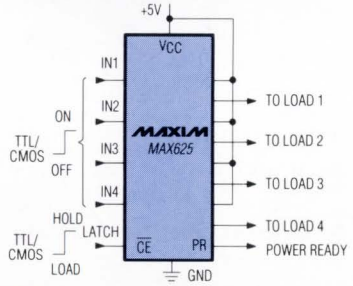
Simplify Battery Load Management, Drive 4 Low-Cost N-MOSFETs from +5V



The **MAX621/620** drive 4 low-cost 35A/0.028Ω N-MOSFETs from 4.5V to 16.0V inputs. It combines a power supply, four latched MOSFET drivers, protection circuitry — all in a single 18-pin IC. The MAX621 has internal charge-pump capacitors; MAX620 costs less and requires 3 inexpensive external components.

(CIRCLE 261)

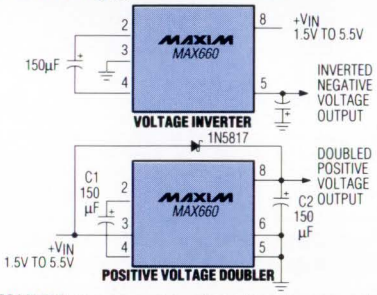
Four 0.2Ω Switches In 0.3in² — No External Components!



The **MAX625** allows logic signals to switch four 1A loads (4A peak), simplifying load switching in low-voltage systems and extending battery life. It has a 4.5V to 16.5V input supply range and 70µA typical quiescent current. Ideal for battery-powered and distributed power applications requiring high efficiency and small size. Available in 24-pin narrow plastic DIPs.

(CIRCLE 262)

100mA-Output, Monolithic Voltage Converter Upgrades ICL7660



The **MAX660** charge-pump voltage inverter converts a +1.5V to +5.5V input to a -1.5V to -5.5V output. It is a pin-compatible high-current upgrade of the ICL7660. 100mA is supplied with only a 0.65V voltage drop, compared to only 15mA with the ICL7660. Efficiency exceeds 90% for most applications.

(CIRCLE 263)

★ DATA SHEETS ★

MAX190	(CIRCLE 246)	MAX404	(CIRCLE 253)	MAX249	(CIRCLE 260)
MAX135	(CIRCLE 247)	MAX412	(CIRCLE 254)	MAX621/620	(CIRCLE 261)
MAX501/502	(CIRCLE 248)	MAX241	(CIRCLE 255)	MAX625	(CIRCLE 262)
MX7549	(CIRCLE 249)	MAX730	(CIRCLE 256)	MAX660	(CIRCLE 263)
MAX507/508	(CIRCLE 250)	MAX738	(CIRCLE 257)		
MAX526	(CIRCLE 251)	MAX732	(CIRCLE 258)		
MAX516	(CIRCLE 252)	MAX7219	(CIRCLE 259)		

★ FREE SAMPLES ★

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ACTIVE PROBES WILL HELP DESIGNERS TEST FASTER CIRCUITS

INCREASING DENSITY WILL REQUIRE MORE PROBE ADAPTERS AND POSITIONING TOOLS

PHIL APPLEBEE
Phil Applebee, a product marketing manager in Tektronix's Test and Measurement Group, received his BSEE from Portland State University, Portland, Ore. He has seven years experience in marketing probes for Tektronix.

As IC speed and density increase over the next few years, circuit designers and test engineers will face new challenges. Devices will be more difficult to probe by hand, forcing a greater reliance on probe adapters and probe positioning tools. The increased use of surface-mount technology will exacerbate the problem. And as edge speeds enter the subnanosecond range, transition zones will be even more difficult to capture. Probe capacitance, resistance, and inductance will become critical. To solve these problems, engineers will, in all likelihood, decrease their reliance on passive and Z_0 probes, and turn to higher-bandwidth active probes.

The typical general-purpose 10X passive probe has an input impedance of 10 MΩ/10 pF, measured at the probe tip. The resistive load this puts on today's low-impedance circuits is negligible. However, the input capacitance is relatively high. This capacitive loading slows the rise time of logic pulses and decreases the amplitude (that is, loads the output) of high-frequency sources. The higher the frequency, the worse the problem.

Previous alternatives to the problem of capacitive loading have included lower-impedance passive probes. Z_0 probes offer a very low tip capacitance, but at the expense of relatively high resistive loading (typically 500 Ω and 1 pF). The resulting voltage divider action between the source and the probe reduces the actual and displayed amplitude by the ratio $R_{probe}/(R_{probe} + R_{source})$.

Active probes, however, approach the ideal performance for signal-acquisition devices because such probes provide low input capacitance and high input resistance, even at high frequencies. Energy to drive the active elements in these probes is obtained either from an external power supply, or from the oscilloscope itself, not from the signal source (the circuit under test), as is the case with passive probes. This configuration effectively minimizes cable, termination, and oscilloscope input capacitance.

The trend toward active probes is already well under way. Over the past several years the use of active probes has virtually doubled. Confronted with data transfer rates of hundreds of megabits per second and beyond, testing departments are looking at active probes as a way to decrease the effects of circuit loading.

The problems of decreasing chip size and lead accessibility will strengthen the case for active probes. Handheld probing will become increasingly difficult, if not impossible. Surface-mount technology will not only reduce access to chip leads, but will also obsolete probing from the opposite side of the board. Probe adapters and probe-positioning tools will become the norm.

New attachment schemes will be introduced to access chip leads. One example might be personality modules designed for specific chips. Such tools, however, often add their own loading to the circuits under test. Active probes will be needed to counteract or minimize these loading effects.

Of course the perfect solution to any loading problem is completely noninvasive probing, where the probe makes no contact with the device under test. Technologies such as electron-beam, infrared, and laser probing have attracted lots of attention, but solutions to the difficulties associated with bringing such schemes to general-purpose applications continue to remain just out of reach.

As is often the case, cost will be a concern. Active probes generally cost three to six times the price of general-purpose passive probes. But the technical difficulties of building higher-bandwidth passive probes are likely to increase their cost, bringing them more in line with active probes. In addition, the price/performance ratio of active probes is already improving.

Finally, reduced chip size and accessibility will compel chip and probe manufacturers to work together closely. As smaller geometries are introduced, efforts to implement standards for lead spacings and package dimensions will have to be speeded up. And chip and probe vendors will have to work hand-in-hand throughout the development process to insure that probing solutions hit the market in sync with chip introductions.□

MATERIALS WILL DRIVE PROGRESS IN SMD TANTALUM CAPACITORS

HIGH-CV TANTALUM POWDERS AND NEW CATHODE LAYERS ARE REQUIRED TO JUMP TO HIGHER CAPACITANCES.

MITSUHIRO TATEBE
Mitsuhiro Tatebe is general manager of NEC Corp.'s Electronic Component Application Engineering Division, Tokyo, Japan. Tatebe joined NEC in 1965, when he received a bachelor's degree in engineering from Nihon University, Japan.

It's interesting to note that while the present slump in the electronics industry has resulted in a plateau for most capacitors, the surface-mounted (SMD) tantalum-capacitor market continues to grow. As with any product, significant enhancements in capacitor characteristics must be made so that existing and new markets can expand and prosper.

Although SMD tantalum capacitors have found their way into a growing variety of electronic products, the devices still have many potential applications. These include medical applications, power supplies, aviation, and traffic-management systems. For SMD tantalums to be successful in any of these areas, they will have to be improved dramatically. For example, powder manufacturers must increase the amount of capacitance-voltage (CV) per gram and molding compounds must be improved, among other tasks.

Through improvements in powder and reductions in the temperature coefficients of molding compounds, tantalum capacitors will be able to withstand higher thermal stress. Because tantalum capacitors are polarized (which requires their insertion in the proper direction), fused chip technology has been in greater demand. Currently, general fuse blow-out specifications call for a 5-second delay at 5 A. Although such events are rare, product-liability considerations prompted tantalum-capacitor manufacturers to work toward a solution. While many users are satisfied with the 5-second, 5-A specification, some companies are changing the fuse material so that blow-out will occur more quickly, at lower currents, and with higher reliability.

Downsizing in all capacitor products, which is driven by the use of higher-purity powder and new processing techniques, will take devices from today's C-case size to the A-case size in a few years. State-of-the-art SMD tantalum capacitors would fall just under 1400 CV (220 μF/6 V) in a package measuring 7.3-mm long by 4.3-mm wide by 4.1-mm tall. It's estimated that tantalum powder will peak at 100,000 CV per gram, but no tantalum-powder manufacturer can produce such potent powder today. Present technology can produce about 30,000 CV per gram. To reach higher levels, powder makers will have to remove more oxygen, sodium, and other impurities than is currently present in the material, which will require process-technology advances on their part.

To develop higher CV values, improvements such as alternatives to the capacitors' manganese-dioxide (MnO_2) cathode layer must be developed. This layer affects characteristics of tantalum capacitors, including dc leakage, dissipation factor, impedance, and equivalent series resistance (ESR). Capacitor manufacturers will have to improve or even change the materials presently used in the cathode layer, because the MnO_2 would not be efficient with the improved high-CV powder.

By continually using MnO_2 along with improved, higher-purity powder, the capacitance, dissipation factor, and dc leakage might be adversely affected. Therefore, new cathode-layer materials, including complex salt (TCNQ), polypyrole (both highly conductive polymer films), or other materials may have to be developed by the tantalum-capacitor manufacturers. However, MnO_2 could still be used with improved high-CV powder if other processes, such as decomposition processing for the MnO_2, are changed. Changes in sintering temperatures would have to be lowered and a higher vacuum would also be necessary.

Improved high-purity powder and new or improved cathode-layer materials would mean improvements in ESR, dissipation factor, and dc-leakage characteristics compared with current levels. This will also increase the tantalum capacitors' resistance to high humidity and soldering heat, which are major factors in automotive and other high-reliability applications.

Surface-mounted tantalum capacitors are expected to keep pace with technology demands and production pressures, and will continue to be a vital part of our expanding electronic technology.□

SWITCHING POWER SUPPLIES WILL BECOME SYSTEM-LEVEL COMPONENTS

DISTRIBUTED-POWER ARCHITECTURES ARE DRIVING THE CHANGE IN ATTITUDE TOWARD SWITCHERS.

PAUL TODD
Paul Todd, the founder and president of Todd Products Corp., Brentwood, N.Y., has more than 40 years of experience in the power-supply industry. Todd holds a degree in electrical engineering from City College of New York.

Switching power supplies have come a long way from their initial emphasis on small size and high efficiency. This decade will see simultaneous advances on many fronts, including electrical circuit design, mechanical packaging, heat-transfer mechanisms, and design for manufacturability. The most important trend will be the dc-dc converter's evolution as a "power component" designed as part of a system, rather than a subassembly to be bought and designed in as an afterthought.

This trend is consistent with emerging distributed-power architectures. Today, more companies are embracing the concept of distributed power, which will determine the future course of switching-power-supply product development and applications. With power densities reaching up to 60 W/in.^{3} in a 150-W converter, the power supply has a well-deserved place on the printed-circuit board next to its electronic load. But to avoid the necessity of large heat sinks to cool these converters, rational thermal management and high-efficiency design will become an inherent requirement. Such trends are already evident with the use of insulated metal substrates, which use the printed-circuit board itself as a heat sink.

This issue is expected to become critical as on-board voltages move from the 5-V standard to 3.3 V, and further to 2.2 V and 1.5 V. As the output voltage declines, the power supply's efficiency also declines. Major component breakthroughs will be required for power supplies to function with a 90% efficiency at such low voltages. Some possibility exists, though—the U. S. Navy is developing a 100-W/in.^{3} converter with an efficiency of more than 90% at 1.5 V. Hopefully, this technology will be made available in the future for commercial applications.

The primary determinant of this evolution will be technology that can optimize the various electrical, mechanical, and thermal parameters required for a specific application. For example, it won't be enough to have high power density without high efficiency. Otherwise, a large heat sink will kill all of the power-density gains. Low efficiency and hot spots will also be a cause of product failure.

The issue of reliability, which remains the most important for users, will be the major factor in integrating component and circuit design along with modern manufacturing techniques. It's the need for high reliability and low cost that will drive power supplies in specific segments towards standardization and customization.

In addition, such products could be manufactured with more automation, which eliminates the inconsistencies of human assembly. At this time, the obstacles to automation are posed by diverse and large components, including electrolytic capacitors, inductors, and heat sinks. The movement toward distributed power will help eliminate the components that require hand assembly.

Development and commercial availability of components remains the key to advances in power supplies. Many interesting topologies have already been analyzed and documented. The component industry has responded with the introduction of megahertz rectifiers and multiresonant controller chips for various topologies. But the power-supply industry is still waiting for low-drop diodes and high-power surface-mounted devices.

Advances in manufacturing, like statistical process control, will also be required to eliminate error-causing procedures. Such advances in methodology will ultimately lead to "six-sigma" manufacturing processes. Beyond the fundamentals of technology, such features as power-factor correction and universal inputs in ac-dc switching power supplies will become standard as the products will be developed for the global markets.

These advances in power supplies will be achieved by a synergistic approach to component, circuit-design, and manufacturing techniques. This interlink of design provides an interesting insight in a switching power supply. That's because in many cases, the individual developments that make up a power supply aren't done concurrently. However, technology remains the glue that can bind all of the disparate developments.□

FUTURE LASER-RECORDING TECHNIQUES WILL BOOST MO DRIVES

AS CAPACITY INCREASES, LIGHTER-WEIGHT, LOWER-POWER HEADS MUST BE DEVELOPED.

MICHAEL HELSEL
Michael Helsel is responsible for product marketing for Teac America Inc.'s Data Storage Products Division, which oversees product introductions and marketing efforts for the company's data-storage products.

Last year, 3.5-in. magneto-optical (MO) disk drives were introduced by nearly a dozen companies including IBM, Sony, and Teac. These first-generation products accept a combination of standard 128-Mbyte-capacity media, for both rewritable and read-only (O-ROM) applications. For 3.5-in. MO technology to fully realize its potential, next generation products must offer increased capacities, shorter access times, and reduced power requirements while dramatically reducing cost. R&D efforts are already underway in the critical areas of laser recording, head assembly, and media composition.

To reach the 7-Gbyte capacities projected for optical drives by such manufacturers as Sony and Teac for the year 2000, the development of short-wave lasers and advanced recording methods will be necessary. A 20% reduction in laser wavelength (from 780 to about 630 nm) makes it possible to record multiple wavelengths on one track, a process similar to magnetic data recording on different levels of the media (surface and sub-surface levels). The more powerful and responsive laser-diode heads and photo-diode detectors currently under development will be able to distinguish between the various wave lengths. Moreover, allowing the optical media's magnetic fields to change more rapidly will eliminate three disk revolutions for erase, write, and verify functions.

Combining modified constant angular velocity (MCAV) laser technology with non-return to zero, change on ones (NRZI) edge-triggered recording can increase recording efficiency and pack more bits into tighter spaces. NRZI is an efficient method for using high densities at low frequencies, while MCAV is similar to zone-bit recording that's done in hard drives. It permits higher densities in the outer tracks of the optical disk, thus keeping linear densities constant.

Smaller and lighter weight heads are essential for faster seek and access times. In the recent product releases, the optical head was redesigned so that the fewest possible parts remained in the moving head. The remaining components were placed elsewhere within the head-disk assembly. More powerful laser diodes will be required for the heads to react faster. Hence, power requirements will be reduced through the lighter weight construction. Lower power consumption will also be attained with more condensed single-chip LSI circuitry that will allow 1-in. high form-factor drives to be built. Reducing the mechanical and electrical part count paves the way for low-cost volume production while contributing to product reliability.

When overwriting data, magnetic flux reversals between two magnetic states must occur rapidly. More advanced optical heads must be developed to accomplish this. In addition, a higher-quality media formulation must be developed to permit lighter weight heads. More sensitive media requires less power to cause a transition between states. As a result, lighter heads are possible. A material more sensitive to low laser power and magnetic fields than the polycarbonate materials currently used must be developed. As disks spin at higher speeds with increased densities, there's less time for a transition to take place. A purer material is needed so that a refraction occurs when a beam of light enters it. Glass-based materials offer these properties but are too heavy. A lightweight solution will likely be developed based on some type of plastic.

Today's optical data-storage products will function as external memory systems for the PC audio and graphics markets and to some extent, as a replacement for Winchester disk drives. Eventually, multimedia applications will come into play, but not until optical capacity is increased and access times and transfer rates are improved. Within the next decade, 3.5-in. MO drives will begin replacing today's floppy-disk drives.

Although development of the key technological areas of these products is underway, perhaps the most critical factor in the future of 3.5-in. MO technology is adherence to the standards established by the ANSI/ISO committees. Deviation from these standards could hinder further technical development.□

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ONE-TOUCH BOARD DESIGNS: FANTASY OR REALITY?

BOARD DESIGNERS FOLLOW IN THE FOOTSTEPS OF ASIC DESIGNERS BY USING PREDEFINED MODULES.

JERRY GIPPER
Jerry Gipper is the product marketing manager for VME board products at the Motorola Technical Systems Div., Tempe, Ariz. He received a BS in computer engineering from Iowa State University, Ames, Iowa, and an MS in computer engineering from San Jose State University, Calif.

Imagine this scenario: You, as a board designer, sit down at your design workstation and begin work on your next project. The resident CAE package steps you through a series of questions concerning the design's architecture, I/O, peripherals, memory requirements, system bus, and other key parameters. After entering some information pertaining to performance and cost goals, you issue the command to design. Within minutes, the board layout is completed, simulated, and a file is ready to send to the pc-board manufacturer. If the current trend toward automation in board-design technology continues in the coming years, this vision may become a reality.

With such automated design tools, designers will be able to concentrate on higher-level system issues, such as bus architecture, performance, functionality, and quality. The impact of "what-if" trade-offs can be quickly evaluated. For example, designers could question the price/performance trade-offs of whether to use a single-memory bank rather than a two- or four-way interleaved array, or if peripherals with built-in DMA should be used instead of intelligent I/O processors.

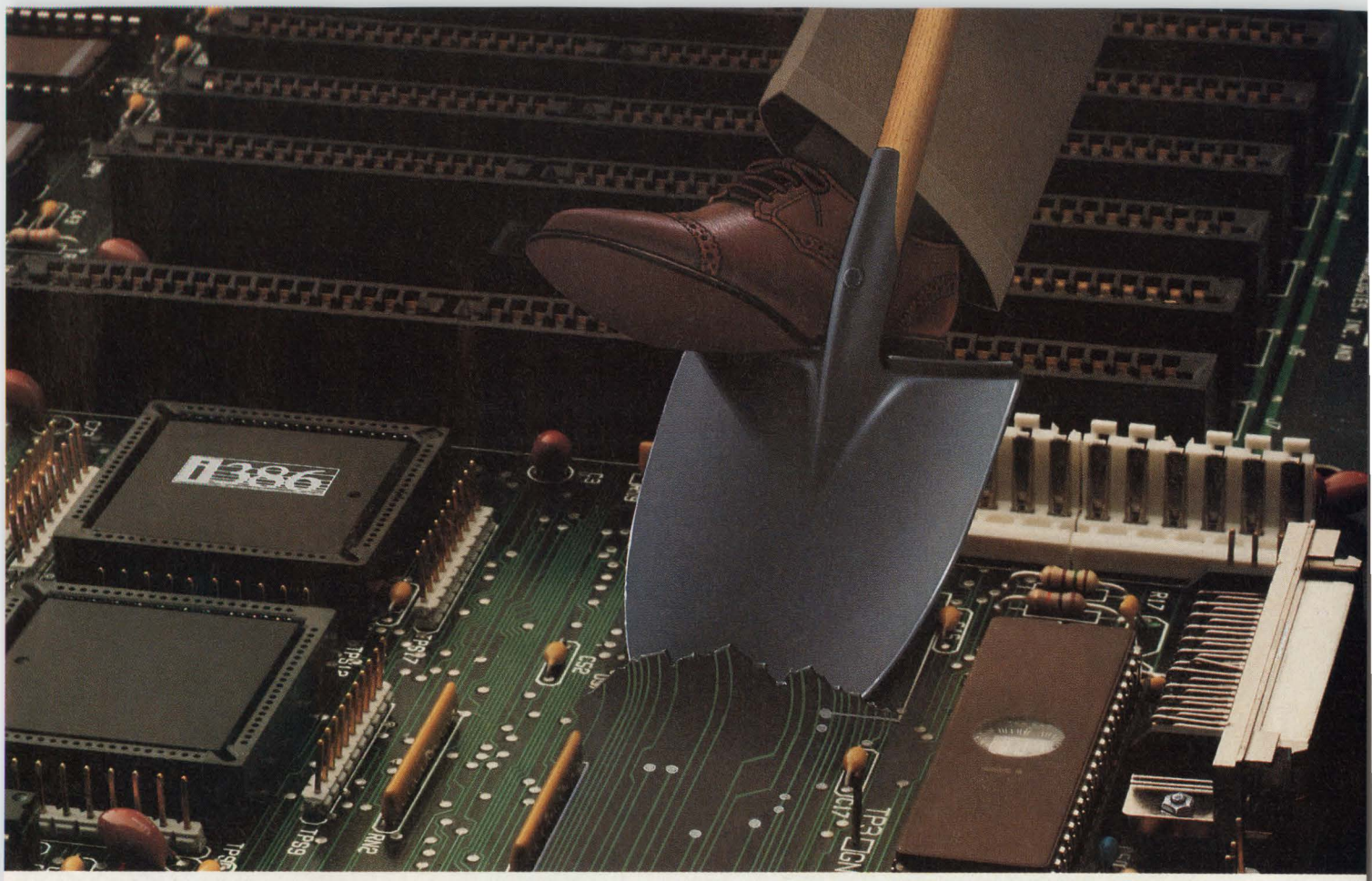
The focus of board designs is changing from isolated modules to system solutions. The board designer must design for system performance by weighing all aspects of performance, from disk and network I/O to processor MIPS. Using the fastest processor doesn't always ensure the fastest final product. Board designers are, in fact, following the trail blazed by ASIC designers, where the products are produced from a set of predefined functional modules.

The increased use of ASICs and highly integrated VLSI components lets engineers add far greater functionality to designs than ever was possible within the same board space. The ASIC and VLSI components will appear as functional modules that designers can keep in their "bags of tricks" for use on multiple designs. With intelligent CAE tools, the designers can manipulate the modules to quickly and easily complete the board design. The functional modules also allow designers to construct multipurpose boards. For example, processor functionality can be combined with application-specific memory or I/O. Board products should emerge with several times the functionality in the same space required by previous generations. Because multifunction and increased-function boards will become more complex, having advanced and simplified design tools will become increasingly important.

By using board-level functional models, designers will simply specify what functionality is desired on the board. Such items as memory, processor, networking, I/O, and bus configurations will be retained in a database library on a file server, and will be available to all designers within the company. The appropriate library functions can then be selected by the designers, laid out, and simulated, all within the same CAE environment. Finally, the completed design is released to the manufacturer. This method could cut the design cycle from the present twelve or more months to just six to eight weeks.

Designers will be able to see immediately how design modifications will affect the performance of each functional module, as well their impact on other factors, such as timing, manufacturability, etc. In addition, they can see how the functional modules interact with each other. Computerized design tools can swiftly weigh the effects of performance trade-offs by quickly simulating various solutions. In addition, the tools can alert designers immediately to quality flaws and offer alternatives. Gone will be the days of developing prototypes and doing redesigns.

Mid-decade designers will need to put a greater effort into design quality while maintaining high levels of performance and functionality. The expected competitive market will require designers to minimize costs. Highly automated design tools that unshackle engineers from the burdens of today's designs will help them to accomplish these goals. In the "best scenario" future, board-design tools will become expert systems that will design the best solution under the guidance of the system architect.□



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Frequency (MHz)	dc-500	500-2000	2000-5000	dc-500	500-2000	2000-5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	———	20	———	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) 19.95 ZYSW-2-50DR (SMA) 59.95		

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CIRCLE 521 UNIT LETS SCOPES LOOK AT 4 TRACES

M.J. SALVATI
Flushing Communications, 150-46 35th Avenue, Flushing, NY 11354; (718) 358-0932.

Several "quick-and-dirty" schemes for displaying multiple traces through a single oscilloscope channel have been published over the years. However, they all lack adequate positioning and/or amplitude control. In addition, most of them display only time-sequence information rather than actual waveforms.

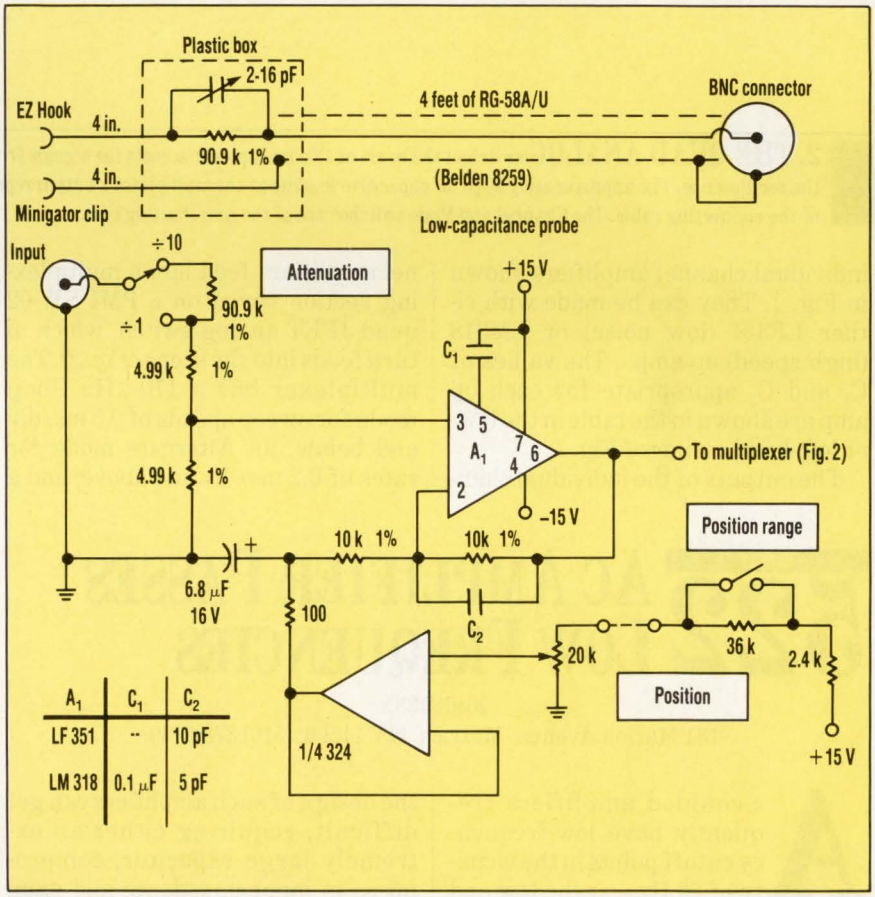
This adapter delivers a high-fidelity display of the actual analog or digital waveform. It offers individual trace positioning and sufficient amplitude control to set up non-overlapping displays for any logic family or a wide range of analog signals. Moreover, it uses readily available, inexpensive parts.

To use the adapter, either set the scope for external trigger or take the trigger from the other input channel, if it's used. Using the oscilloscope's position control, place the initial baseline near the top of the screen. From that position, each of the adapter's four Position pots *(Fig. 1)* will be able to move its trace anywhere on screen, regardless of the scope's attenuator setting. At the scope's most sensitive settings, the adjustment will be easiest if the Position Range switch is open.

For best results, use the optional low-capacitance probes and set the Attenuation switch to its ÷1 position. Alternatively, make a direct connection and set the switch to ÷10. In either case, the input resistance will be 100 kΩ and the available overall deflection factors will range from 0.5 to 10.0 V/div. For 50 mV/div sensitivity, a direct connection can be combined with the ÷1 switch setting, though the input resistance is reduced to 10 kΩ.

The low-capacitance probes are easily fabricated from BNC-equipped RG-58A/U coax and 3/4-in. plastic boxes.

The adapter requires four of the



1. FOUR OF THESE individual channel amplifiers and low-capacitance probes are required by the four-trace adapter. The Position Range switch and its two associated resistors are shared by all four amplifiers.

IFD WINNER

IFD Winner for August 8, 1991

Jim Williams, Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 954-8400. His idea: *"Chopper FETs Improve Amp."*

IFD Winner for August 22, 1991

Michael Wyatt, SSO Honeywell Inc., 13550 Hwy. 19 S., MS931-4, Clearwater, FL 34624; (813) 539-5653. His idea: *"Active Filter Gets Higher Frequencies."*

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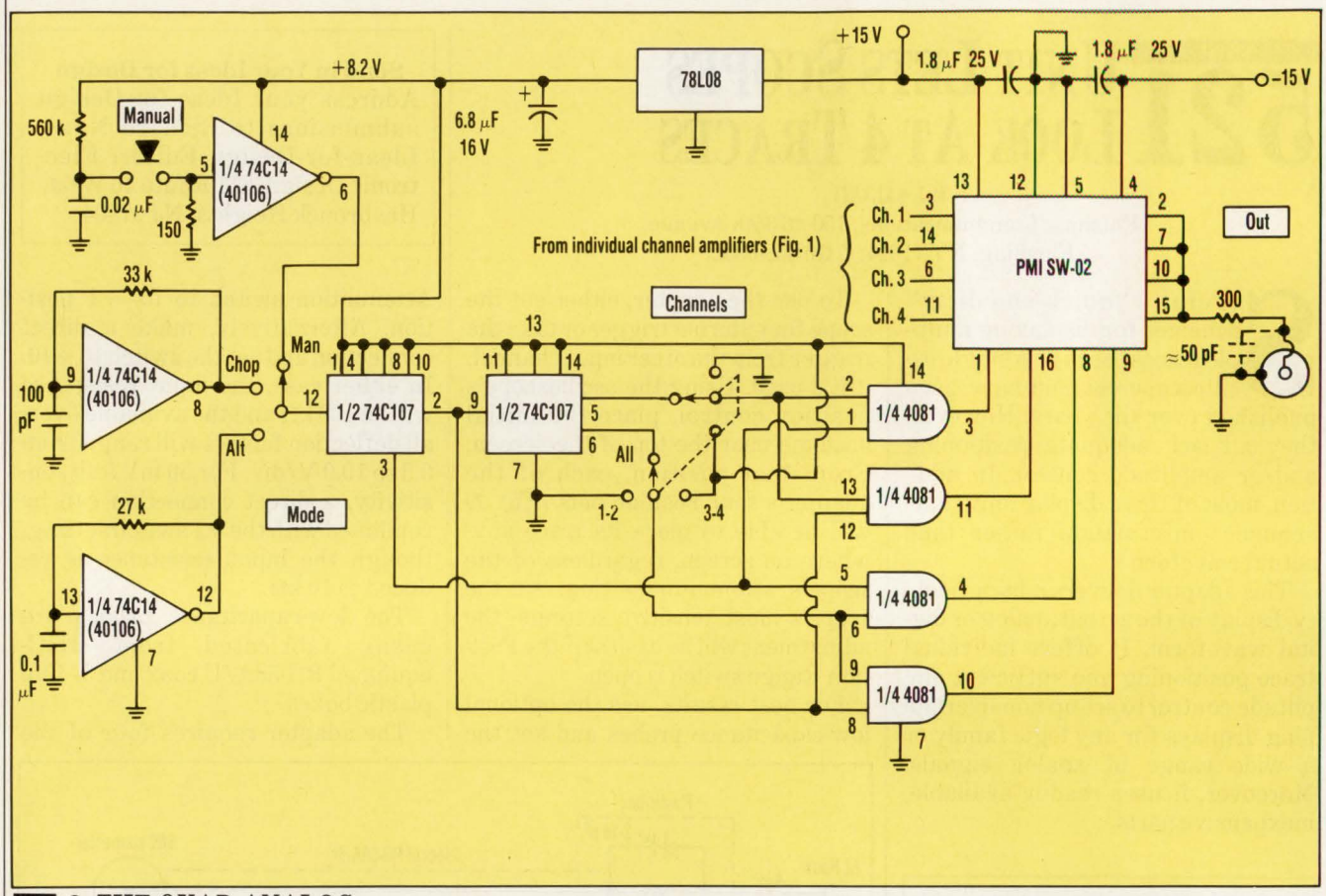

2. THE QUAD ANALOG switch at the heart of this multiplexer accepts the signals from the four amplifiers of Fig. 1 and sends them to the oscilloscope. The approximately 50 pF of capacitive loading at the multiplexer's output represents the scope's input capacitance plus that of the connecting cable. The Channel and Mode switches are of the non-shorting type.

individual channel amplifiers shown in Fig. 1. They can be made with either LF351 (low noise) or LM318 (high speed) op amps. The values of C_1 and C_2 appropriate for each op amp are shown in the table in the lower left-hand corner of Fig. 1.

The outputs of the individual channel amplifiers feed into a multiplexing section based on a PMI SW-02 quad JFET analog switch, which in turn feeds into the scope *(Fig. 2)*. The multiplexer has a 170-kHz Chop mode for sweep speeds of 0.5 ms/div and below; an Alternate mode for rates of 0.2 ms/div and above; and a Manual stepper mode. The stepper mode cycles through the channels, displaying a different single trace each time the Man button is pushed. The Channels switch allows the display of all four channels simultaneously, channels 1 and 2 only, or channels 3 and 4 only.□

CIRCLE 522

AC AMPLIFIER PASSES LOW FREQUENCIES

JOHN DUNN
181 Marion Avenue, Merrick, NY 11566; (516) 378-2149

Ac-coupled amplifiers frequently have low-frequency cutoff points in the vicinity of 20 Hz—at the low end of the audio spectrum. For applications that require passing much lower frequencies while still blocking dc, the design of such amplifiers can get difficult, requiring either an extremely large capacitor, compromises in input impedance and gain, or quite possibly, both.

By basing the amplifier on a negative-resistance converter instead of on the more common technique of input bootstrapping, it is possible to build a device with an extremely low cutoff frequency, a modest-sized capacitor, and independently adjustable gain and input resistance *(see the figure)*.

The first stage of the two-stage amplifier is a negative-resistance converter, which sets the amplifier's input resistance. Together with capacitor C_1, that resistance establishes the low-frequency cutoff point. The independent second stage sets the amplifier's gain.

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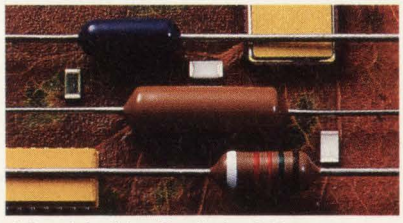

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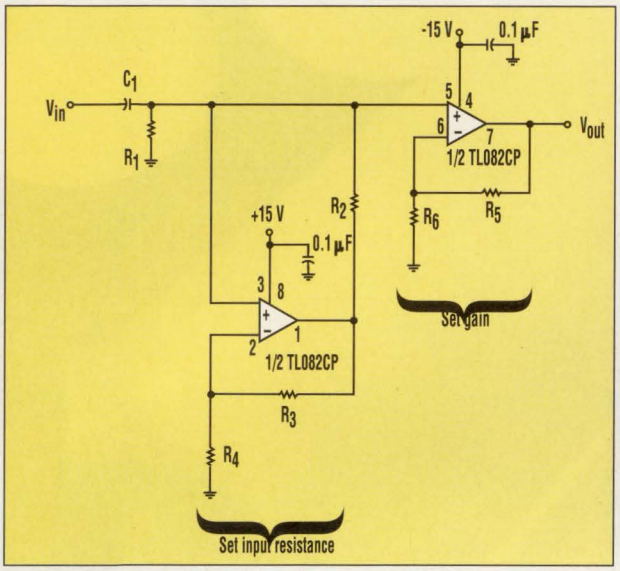


INDEpendently adjustable gain and input resistance are two features of this very low cutoff ac-coupled amplifier. Because the negative resistance converter input stage makes possible extremely high input resistances, the input capacitor can be of modest size and still pass frequencies below one hertz.

The formulas for input resistance, cutoff frequency, and gain are as follows:

$$R_{in} = R_1R_2R_4 / (R_2R_4 - R_1R_3)$$

$$f_{co} = 1/(2\pi R_{in}C_1)$$

and

$$G = (R_5 + R_6) / R_6.$$

Referring to the diagram, if $R_1 = R_2 = R_4 = 100\ k\Omega$ and $R_3 = 97.6\ k\Omega$, then the input resistance is raised from the 100-kΩ value of R_1 to approximately 4 MΩ. With that resistance, a moderate sized input capacitor, C_1, of 0.1 µF will give a cutoff frequency of approximately 0.4 Hz. The upper cutoff frequency of the amplifier is determined mostly by the op amp characteristics, in this case a dual TL082CP.□

CIRCLE 523

GET +5V/100 MA FROM FOUR CELLS

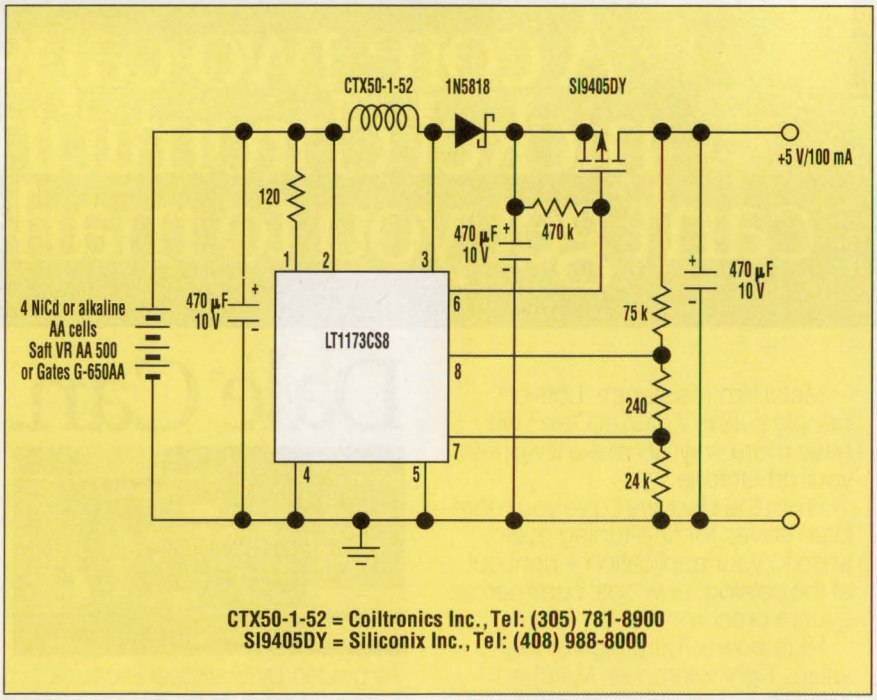
MITCHELL LEE
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900.

In many instances, a four-cell battery is the popular choice for portable instruments. But this poses a special problem for instruments with 5-V circuits—the battery's terminal voltage isn't well behaved. For example, a battery of four, fresh alkaline cells develops about 6.5 V, but at end-of-life the voltage falls to 3.6 V under load.

NiCd cells have only a slightly narrower range—about 4 V to 6 V. A flyback topology dc-dc converter can handle the job, but requires a tricky transformer design.

A unique solution to the problem is based on a dual-mode conversion circuit *(see the figure)*. Producing a 5-V, 100-mA output from a four-cell input, the converter only requires a simple two-terminal inductor. At input voltages below 5.5 V, the circuit operates as a burp-mode boost converter, with the MOSFET held in the On state. At higher input voltages, the boost converter shuts down and the MOSFET acts as a series pass element in a very-low-dropout regulator. The error amplifier is contained in the LT1173CS8 micropower dc-dc converter.

Because it operates with inputs ranging from 3.6 to 7 V, the converter allows direct interchanging of alkaline and NiCd cells. It also permits in situ charging of NiCd cells.□



CTX50-1-52 = Coiltronics Inc., Tel: (305) 781-8900
SI9405DY = Siliconix Inc., Tel: (408) 988-8000

USING A SIMPLE two-terminal inductor, this dual-mode, dc-dc converter operates with battery terminal voltages ranging from 3.6 to 7 V. When the battery voltage falls below 5.5 V, the circuit operates as a burp-mode boost converter. At higher voltages, it functions as a very-low-dropout regulator.

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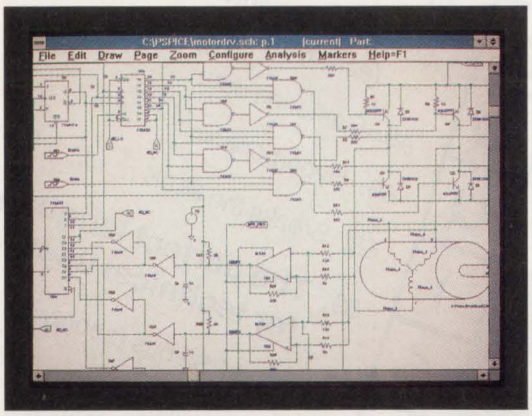

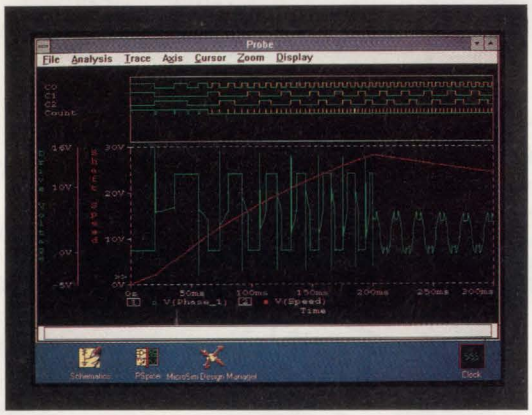

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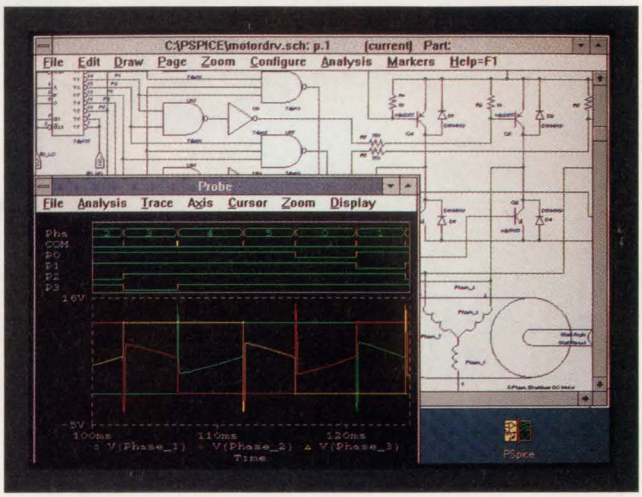

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ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

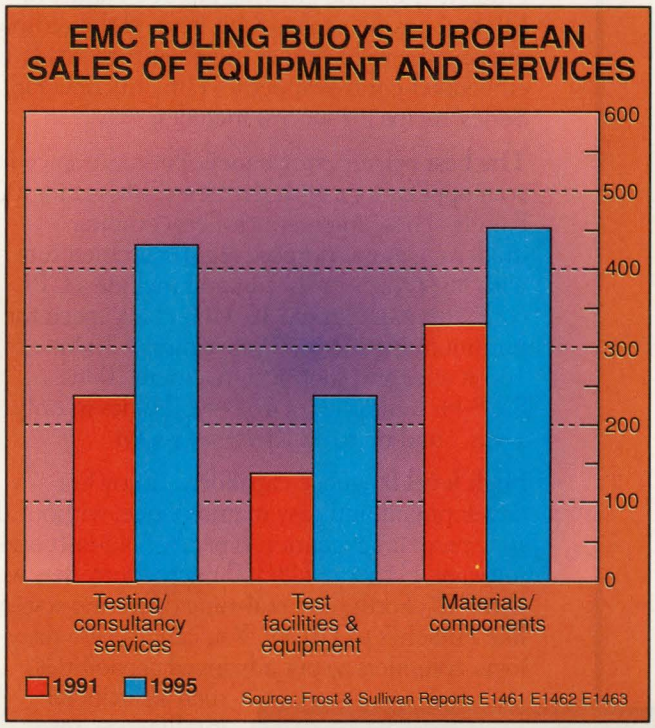
MARKET FACTS

The market for electromagnetic equipment and services is getting a shot in the arm. A European Community directive makes it mandatory that electronics and communications equipment meet electromagnetic compatibility (EMC) standards by 1995. Manufacturers in defense and electronic data processing (EDP) sectors already incorporate EMC in designs, but overall the EMC market has plenty of room for growth, predicts market researcher Frost & Sullivan Inc.

One sector with lucrative potential is the one for testing and consultancy services. That should increase from about $240 million this year to about $430 million in 1996, according to the New York-based company. EMC testing will account for three-quarters of the market. The consulting that's now done by test houses is likely to become independent, Frost & Sullivan says.

Highest growth rates are expected to be seen in EDP. Revenues in that sector will rise from $67 million this year to $147 million in 1995. Meanwhile, the defense sector, owing to tighter budgets, will grow more slowly, rising from $72 million this year to $81 million in 1995.

The market for EMC test facilities and equipment will increase from $136 million this year to $239 million by 1996. The biggest national markets in Europe for EMC equipment and services are Germany, the U. K., and France, followed by Switzerland and Italy.



TALES FROM THE SKUNK WORKS

Despite the legends, skunk works are elusive. Though they are more topical than ever today because of the distress and decline of U. S. high-tech commerce, they remain rare in business practice and literature. It is worth considering why. Most business writings and most consulting practices deal with process. Since the 1930s and Frederick Taylor, legions of management experts have fed at the trough of improved process. Probably 90% of the work in the field starts with something measurable—cost, time, zero defects, capacity utilization—then quantifies it and puts in place processes to improve it.

Managers love process, and most consultants work there for the same reason that Willie Sutton robbed banks, "Because that is where the money is." Few if any have ever been fired for improving a client's processes. It is helpful and safe. Wall Street loves predictable things, and process is predictable.

But improvement does not help if you have the wrong products. Incremental process does not yield a jet aircraft, a PC, a CD player, or a walkman. If Edison had been an MBA, he might have invented a large candle. Instead he ran a skunk works to create "inventions to order."

The use of skunk works has been considered—and rejected—by most learned U. S. business experts and managers. Creativity disrupts process and tends to be unpredictable; a skunk works is particularly so. It's worthwile to consider why skunk works are rejected.

First, the very act of isolating a group of development and support people is seen as an admission that the remaining organization is a) flawed and b) not up to the task of innovation. These are fighting words for powerful corporate animals, who often stomp out the skunks. Why not admit *all* organizations are flawed? The Japanese do and spend every second of every day adapting. Just as there are many types of tools and numerous flavors of ice cream, there are various forms of innovation. Second, skunk works are noted for episodic innovation, not continuous improvement. Excellent results are being obtained by "closed loop" or "core" teams. These combine the skunk works organizational form with process to achieve rapid, continuous, incremental improvement. The last objection is that we lack leaders, but more on that in the next column.

John D. Trudel: The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax 543-6361.

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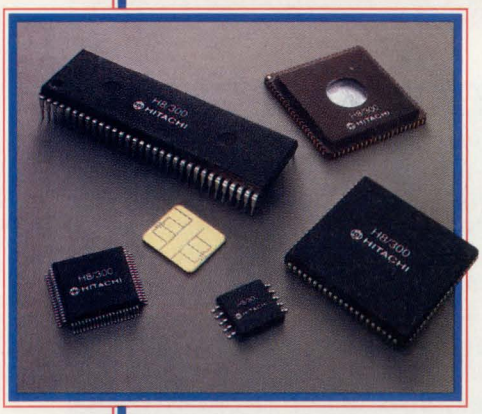

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Timers		3				5	10
Serial Channel		2				1	2
A/D Converter						8-Bit, 8 Channel	8-Bit, 16 Channel
Interrupts		4 External 16 Internal				9 External 19 Internal	9 External 47 Internal
I/O Ports	1-Bit I/O Common	47 I/O 4 Input Only				58 I/O 8 Input Only	50 I/O 16 Input Only
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The kit consists of the Sony Vbox video/computer interface for computer control of Sony consumer video products with a LANC (local applications controller) port and Media Maker CV, a special version of MacroMind's MediaMaker desktop video publishing software. MediaMaker CV enables Mac users to create videotapes from graphics, animation, and sounds stored on the Mac. The interface consists of the controller box, power supply, and cables to connect the Mac and compatible Sony video peripherals—Sony's 8-mm and VHS VCRs and 8-mm camcorders. The kit has a list price of $399. Further information is available by calling (800) 222-0878.

An application environment across all hardware and operating systems heads the wish list of many users and managers. To that end, the Object Management Group is developing the Object Management Architecture. It will enable objects to transparently make and receive requests and responses within an object-oriented environment. At the heart of the standard, the Object Request Broker (ORB) supplies the communications highway, enabling objects to interact over a network of different systems. Written ORB specifications are available for $50. The six companies involved are Digital Equipment Corp., Hewlett-Packard, HyperDesk Corp., NCR Corp., Object Design Inc., and SunSoft Inc. Contact Elizabeth Jewett, member relations, OMG Headquarters, 492 Old Connecticut Path, Framingham, MA 01701; (508) 820-4300; 820-4304.
CIRCLE 451

CodeCheck/2 software determines if C and C++ products developed on OS/2 2.0 are portable to DOS 5.0. Windows 3.0, OS/2 1.0, and other 16-bit platforms. A 32-bit expert system, CodeCheck/2 reads all variants of C and C++ source code. It sells for $495 for DOS systems, OS/2 at $695; AIX licenses are $995 a seat. Source code can be licensed for minicomputers and mainframes. Contact Abraxas Software Inc., 7033 S. W. Macadam Ave., Portland, OR 97219; (503) 244-5253; fax 244-8375.
CIRCLE 452

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CIRCLE 453

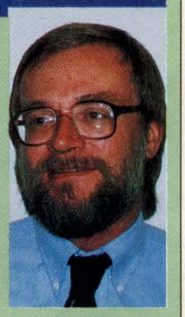
DID YOU KNOW?

. . . that 42% of the world consumer electronics market is in Japan.
Texas Instruments Inc.

. . . that overall, 1991 will show 7.8% industry growth, with double-digit growth in 1992–3.
Semiconductor Industry Association

KMET'S KORNER

...Perspectives on Time-to-Market



BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

A product concept that successfully exits the promotion phase gets staffed and funded as it begins the definition phase. Recall that this phase is initiated by transferring a new product definition sheet (NPDS) to the team. Team members will work within resource and time constraints to figure out exactly what will be produced during the fully staffed execution phase. Of course, a model of the execution phase is developed during the brief, but intense, planning phase to allow an orchestrated cross-functional, concurrent development of the new product.

When execution is complete, the product is delivered to market to initiate the flow of revenue to the developing organization. The point where revenue begins to flow marks the end of the time-to-market measurement interval. Like the starting point of measuring the time to market interval, this moment in time is relatively easy to identify.

With the entire measurement interval understood and in view, a time to market decomposition is easily produced:

	Typical	Achievable
Concept promotion	2 years	1 year
Definition	1.5	0.9
Planning	0	0.1
Execution	2.5	1
Total TTM	6 years	3 years

Figures in the typical column are not statistically rigid, but they are based on projects I have in my database. While my numbers might be interesting, I encourage you to determine actuals within your product development environment. Then, you'll be able to set goals that you think are achievable within your organization. Generally speaking, by doing a few things right, it's possible to shave years off your total TTM.

QUICKLOOK

TIPS ON INVESTING

Income tax planning should play an important role in an engineers' investment decisions at every stage of adult life. Each stage has its own tax-planning issues. When an engineer is still working and hasn't experienced a change in tax rates, tax-planning strategies do not change much. The main concern is to maximize after-tax investment returns and to begin to reposition a portfolio to reduce risk and generate additional income, if necessary, to meet retirement income needs. Some engineers, who have a large amount of company stock in their portfolios, may want to reduce their exposure to this issue by reallocating assets to create a more diversified portfolio.

Upon retiring, the most important decision concerns how and when to take distributions from employer-sponsored retirement plans. For those receiving lump sum distributions, a decision must be made either to roll over the distribution into an IRA or to have the distribution taxed immediately using favorable tax treatment. If an engineer turned age 50 by Jan. 1, 1986, he or she can use five-or ten-year forward averaging for a lump sum distribution (with any pre-1974 amounts eligible to be taxed at a flat 20% capital gain rate, if chosen). Others can use five-year averaging only once and only after they have reached age 59 1/2. The typical lump sum distribution often represents the most money an engineer receives in his or her lifetime. A poor decision could cost thousands of dollars, and assistance from a professional is recommended.

After retirement, tax planning involves different areas. For example, many engineers sell their homes to move to smaller residences or retirement communities and face a large tax liability on the resultant capital gain. Taxpayers are permitted a one-time exclusion of up to $125,000 of the profit on their primary residence. To qualify, the home must have been the primary residence for three of the last five years and either spouse must be at least age 55.

Retirees need to be aware that some Social Security benefits may be taxable. If a retiree's adjusted gross income plus tax-free interest plus one-half of the Social Security benefit exceeds a limit ($25,000 for singles and $32,000 for couples), up to one-half of Social Security benefits will be added to taxable income. Engineers also face a loss of benefits if they continue to work during retirement. In 1991, if a retiree is 65 or older and collecting Social Security benefits, he or she loses $1 of benefits for every $3 of earned income over $9,720. If an engineer is under 65, he or she loses $1 of benefits for every $2 earned income over $7,080. However, no benefits are lost for those engineers who are 70 and above.

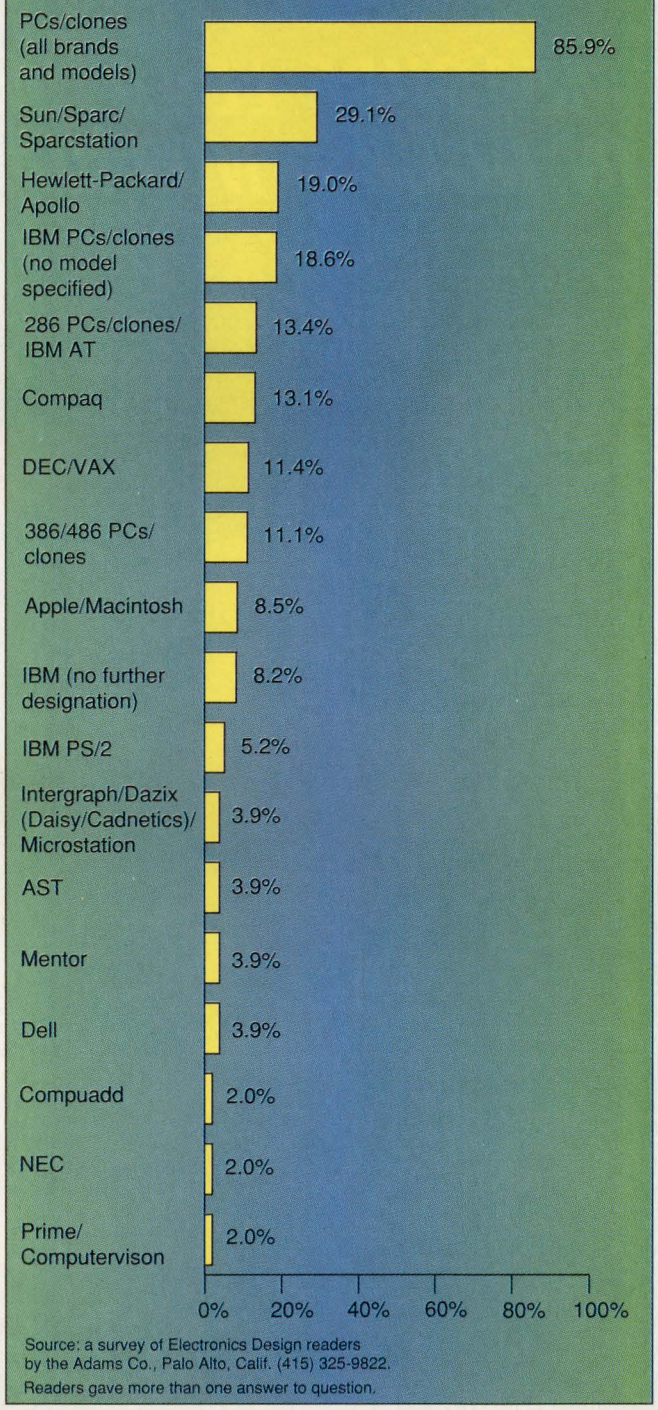
Just before retirement, earned income is usually at its highest, resulting in a high tax bracket. As a result, many investors have invested in municipal bonds. After retirement, these engineers may need to reconsider whether they are still beneficial in their retirement tax bracket. Generally, municipal bonds are appropriate only for those investors in a federal tax bracket above 15%.

Before taking steps to implement any tax strategy, it's important to speak with your tax and/or legal adviser. For a free copy of "Making the Most of your Lump Sum Distribution," a Shearson Lehman Publication, contact me at the address or phone number below.

Henry Wiesel is a financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221. He is also a qualified pension coordinator.

CAD/CAE SURVEY

WHICH COMPUTER OR SYSTEM DO YOU USE FOR CAD/CAE APPLICATIONS?



Source: a survey of Electronics Design readers by the Adams Co., Palo Alto, Calif. (415) 325-9822. Readers gave more than one answer to question.

An incorrect price was given in the Sept. 26 issue for the EMC Information Package, a guide to electromagnetic compatibility, published by the UK's Institution of Electrical Engineers (IEE). U. S. price is $74.75. Contact Publication Sales, IEE, P. O. Box 96, Stevenage, Hertfordshire, SG1, 2SD, UK; phone 44 438 313311; fax 44 438 742792.

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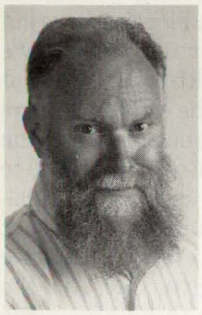
WHAT'S ALL THIS NEGATIVE FEEDBACK STUFF, ANYHOW?

Once upon a time, I worked as Director of Development at Philbrick Researches in Boston. I was reporting directly to George Philbrick himself. (I'll have more stories to tell about him another day.) One day George asked me, could I name the earliest example of a system with feedback? I thought for a few seconds and then conceded, "No, I couldn't."

George proceeded to tell me about some master clock builders who had designed many beautiful high-precision clocks back in the 14th or 15th century (I'm trying to give you this story from memory after a full 20 years). They had a tedious procedure for trimming and adjusting the rate of the pendulum for each new clock, to bring it up to the correct speed so that it agreed with a master clock.



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

But one of the master workman decided to get smart and lazy. He added a little mechanical detector so if a new clock's pendulum were to fall behind the reference, it would trip a cog which would then rotate the screw on the new pendulum and shorten it up, making it run it faster. Conversely, if it ran ahead, the screw would be turned so as to lengthen the pendulum. Of course, this was operated as a sampled-data system – it did not exactly work in real time. So if the pendulum's speed was too far out of synch, the servo would not work. But the lazy fellow was able to do some first-order tweaking and then go home. When he came to work in the morning, the new clock's pendulum would be perfectly matched with the reference.

WOW! Let's give a cheer for 1550s technology. This is not only a feedback loop – it's also one of the world's first PLLs (phase-locked loops). That would, of course, be the first if there's any truth to this story. I've searched a little and have not been able to confirm its validity, though. But maybe there's an element of truth in there. Maybe I don't have the century quite right. But, it's an impressive story, and George did tell it to me.

The next week, when it was time for our meeting, I told George that I had an example of feedback that was older than his, by a large margin. He looked at me quizzically and I explained. When the ox or bullock was first tamed and domesticated thousands of years ago, it was found that if you put a ring through the nose of the ox, you could easily lead it with a gentle tug, and the beast would follow you closely. At first, the ox would follow closely to avoid pain in his sensitive nose, but eventually he would learn to follow because it was his job and habit.

Even a small child could learn to lead an ox pulling a heavy cart or sledge, by tugging lightly on a thin cord. So here is the original Unity-Gain Follower, with a *high* input impedance, and a *low* output impedance. Even if the ox didn't pull the load quite far enough, he was still under control "inside the loop," because even a child could tug a few more inches on the cord to get the load pulled up to exactly where he wanted it. I can't tell if that feedback goes back 5000 or 6000 years or more, but it surely is a good old example, and George had to concede that.

In the early 1800s, steam engines were developed to a rather high degree of sophistication. To maintain speed, the governor was invented. The centrifugal force on a couple of rotating fly-balls was coupled into a linear motion that could open or close the throttle. The basic governor had finite gain, so if a load was applied, the engine would slow down and then work its way back up a little – but not all the way back, due to the finite gain. To obtain substantially perfect speed regulation, governors were devised with tricky mechanical linkages so that they had infinite gain. But some of these were unstable. Finally, improved designs had infinite dc gain, but a well-controlled dynamic response, to help keep the loop stable. To think all this stuff went on back in the 1880s! I can look up a whole bunch of these old designs in my old Encyclopedia Britannica, the 1891 edition. YES, *1891*, not 1981!

Now, come to think of it, George Philbrick told me of a saw mill he designed when he was young. He said he designed it to idle at a moderately slow speed, to save on fuel and energy. But when a load was applied, it would speed up smoothly, so as to apply maximum power when the load was heaviest. Of course, any *simple* governor could not do this, because if it sensed the inertial load of the saw blade, it would speed up as it sensed the torque being sent to speed up the inertial load. It could not easily distinguish this from a lossy load, such as a log being cut by the saw teeth. This loop would normally oscillate with a vengeance, back and forth from the highest speed to a stall speed.

But, of course, George claimed he had designed a detector that could distinguish the difference between a dynamic load and a lossy load, and he could servo the loop with adequate stability. In theory, one could indeed do this. But when George was young (in the 1930s and 1940s), I doubt if the tools were easily at hand. Still, I would not want to bet him that he did not or could not do it. After all, in 1970 I designed an analog-to-digital converter that could easily have been built in the

PEASE PORRIDGE

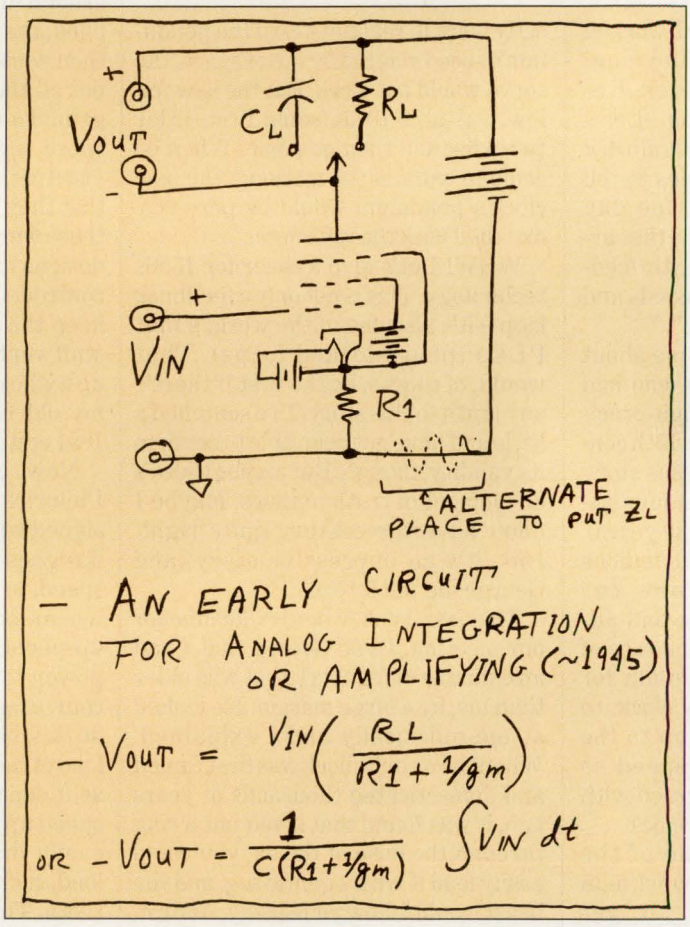
1940s or earlier. But I still think George was pulling my leg.

In the 1930s, Mr. Harold S. Black devised his famous theories about negative feedback at Bell Labs. The best amplifiers of the time still had excessive distortion. When you cascaded 40 or 60 stages of amplifier, as you might do in a long-distance telephone line, the distortion kept building up. With the aid of feedback, the amplifiers' distortion could be cut to negligible levels, even after many cascaded stages. The story of how Black became aware of the advantages of negative feedback, while crossing New York harbor on a ferry-boat, was recounted a few years ago in the *IEEE Spectrum*, and makes fascinating reading....

It was only a matter of time before this led to the analog computer and the operational amplifier. Now, we all know that a basic operational amplifier can integrate a signal. But in the early days of analog computation, even a single pentode could perform integration *(refer to the sketch)*. George Philbrick worked with many things of this type – crude, imperfect, but inspiring. Who invented the operational amplifier? Nobody argues that there was only one inventor, but there were groups of engineers who helped convert those crude, unidirectional current pumps into the familiar op-amp functions we know. And George was one of those pioneers.

During World War II, George worked with analog computing systems, training gunners to do a better job of aiming their guns at fast-moving planes. He found that if you inserted a controller circuit between the man and the gun, it could be tailored to improve the response and accuracy. He could also tailor this response to make the job more difficult, more awkward. He added lags to make it really very difficult to aim the gun. Then after some more practice he removed the lags, and the gunner was now quicker and more accurate than ever. So this was used as part of the training.

George also devised controller networks that, under favorable conditions, could aim a gun at the correct angle ahead of the plane's image – the "lead" – better than a human could. He designed controllers that were very good at adapting to any changes in the dynamics of the gun-aiming circuits.



However, there was one situation George said he could not handle with his controllers: If the gain reversed – if the knob that was supposed to make the gun go to the left made it go right – he could not accommodate that. These days, of course, you could design a computer that would detect this reversed response and then make it work right. But back in the 40s, it wasn't so easy.

Now *that* reminds me of one of my pet experiments. Somebody told me that if you're riding a bicycle, and you cross your hands on the handlebars, your servo will goof up and you will crash. I tried it. I crashed. I will concede that if you think *really hard* and lock up your shoulder with your arms, you may be able to steer the bike to servo things and not crash. But if you just let your arms push and pull, as if they were not crossed, well, I warn you now, it's easy to crash a bike. Please do not hurt yourself. You do not really have to try it; just think about it. But if go ahead with this endeavor, try it on a soft lawn where you won't get ruined when you crash.

These days, there are so many examples of negative feedback, that it's almost preposterous to try to count them. If you have a VCR, the motors are driven at a precise speed by a loop controller. Radios have AFC and AVC loops. A refrigerator's thermostat is a crude, bang-bang controller. Kids' toys act as robots with feedback.

A single op amp may have 2 or 3 feedback loops. When we are driving our cars or riding our bicycles, if we get off center in our lane, we servo back to where we want to be. If the car's speed errs from the bogey value, the speed control pulls it back to the right speed. There's almost no limit to the amount of negative feedback that we use in a given day. And the more we think about the Good Old Days, the better we can appreciate how things work, and how things got to be this way.

Now, I'm only writing about Negative Feedback. I was not intending to write about George Philbrick. Imagine what I'd have said if I had intended to write about George.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

Address:
Mail Stop C2500A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

SRAM-Based Reconfigurable Logic Cells Yield Flexible, Fast Logic Arrays That Surpass Other FPGAs.

Reprogrammable FPGAs Offer Gate-Array Speed

Dave Bursky

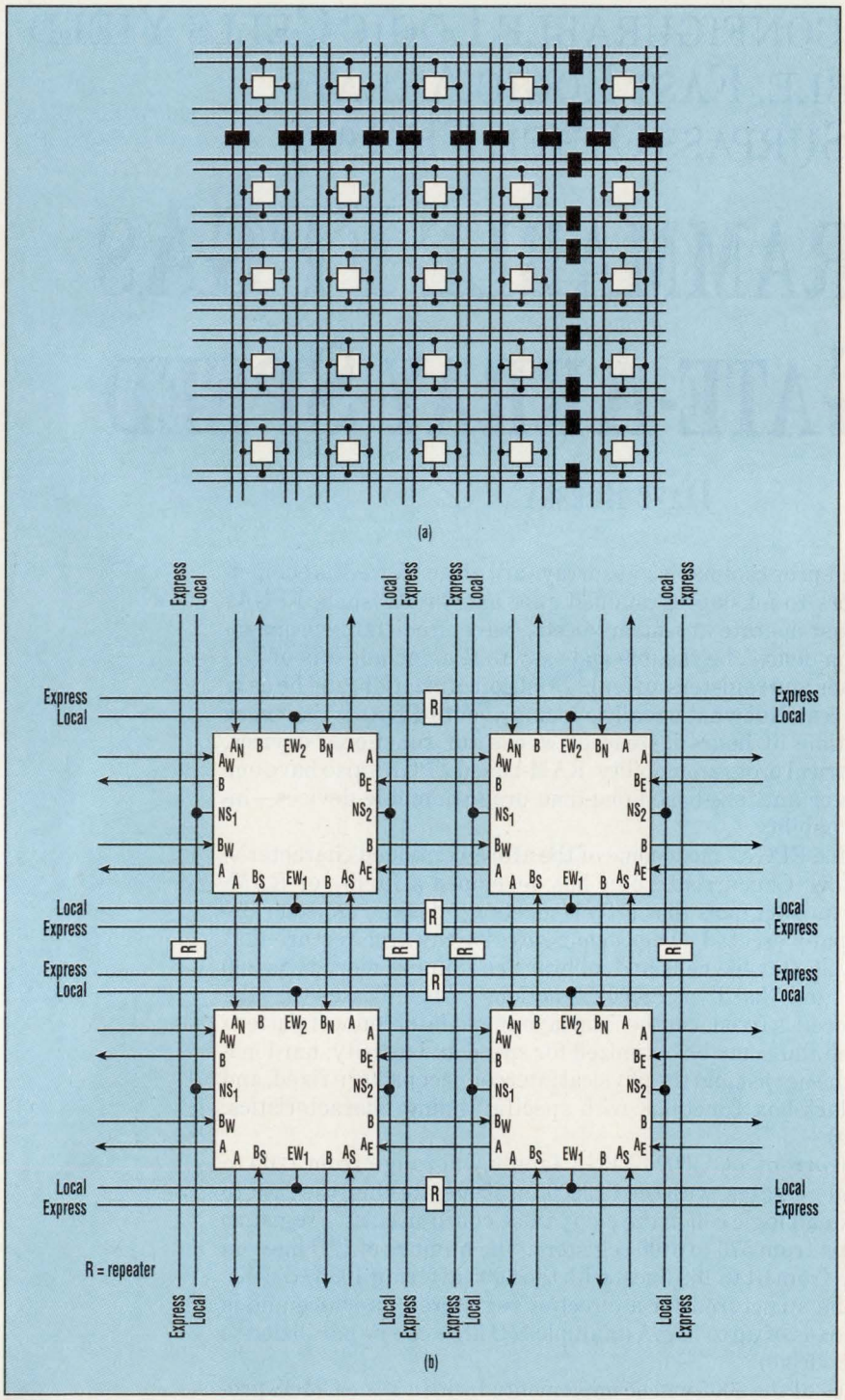
Field-programmable gate arrays are often viewed as competitors to mask-programmed gate arrays. As such, FPGAs must operate at similar speeds, have predictable propagation delays, be flexible and easy to use, include lots of I/O lines and registers, offer high silicon utilization, and be easy to test. But what's really enticing about FPGAs is their very short turnaround time of hours instead of weeks for functional devices, thanks to their electrical programmability. RAM-based FPGAs also have one other advantage over antifuse-based one-time programmable devices—in-system reprogrammability.

Currently available FPGAs meet some of the aforementioned characteristics, but not all. Now, Concurrent Logic has developed a family of RAM-based FPGAs and support tools that it feels meets *all* desired aspects. Designers at the company created a very symmetrical array architecture that includes lots of small, flexible cells and a library containing more than 200 predesigned "soft" and "hard" macrocell functions (soft indicates that the net list of the macrocell is fixed, yet the final layout and interconnect pattern of the cell is not, and thus may be optimized for speed and density; hard macrocells have both the net list and the physical interconnect pattern fixed, and are treated like black-box functions with specific timing characteristics, heights, and widths).

Densities of Concurrent's CLi6000 FPGA family will range from 1200 to about 10,000 equivalent gates, with the CLi6005, a 5000-gate chip, the first to be released. Each small logic cell in the chip can be configured as a register, thus giving the chips from 576 to 6400 registers. The number of I/O lines on the chips will range from 64 to 160 lines, with the 6005 offering 108 I/O cells. Each I/O cell can be structured for a direct or registered interface and is capable of driving loads of up to 12 mA (multiple I/O lines can be paralleled to increase the current drive).

The initial samples of the 6005 will be implemented with a 1-μm CMOS process, but production lots will be ramped up on a 0.8-μm process for improved speed. However, even at 1 μm, the chip is no laggard. At 0.8 μm, though, on-chip flip-flops can toggle at 150 MHz, according to the company, and functions like simple counters can run at clock rates of 90 MHz. With the finer geometries, a 16:1 multiplexer incurs a delay of just 14 ns, a 24-bit decoder has a 13-ns delay, and a 16-bit loadable up/down counter can run at 70 MHz. Such speeds represent a significant performance improvement in the state of the art of field-programmable gate arrays.

Like the other RAM-based FPGAs, the CLi6000 chips can be set up to self-



1. THE TOP VIEW of the CLi6000 array architecture created by Concurrent Logic could almost be thought of as an array of checkerboards within a checkerboard. In this small fraction of one square of the larger checkerboard, the small black rectangles (repeaters) demarcate the border of each large square of the checkerboard (a). Within each square is an 8-by-8 array of reconfigurable logic cells (one quarter of which is shown here) interconnected by local and express signal buses, as well as neighbor-to-neighbor connections in all four directions (b). Repeater blocks in the horizontal and vertical buses are embedded every eighth logic cell to allow local bus signals to switch onto the express bus, or vice versa.

boot from an external nonvolatile memory (such as an EPROM, EEPROM, or flash memory) or under control from a host system. There are seven configuration modes possible with the chip, modes 0 to 6, with mode 0 being a configuration reset.

Multiple 6000-series members can be interconnected on a board and then loaded sequentially. Furthermore, even after a system is configured, it can be partially or completely reconfigured. Partial reconfiguration can be done on a selected basis to areas of the chip that are not currently in use.

Factors like board area, configuration time, and component cost will determine which mode should be set up. A typical boot sequence requires about 8 ms to initialize all core cells, internal logic and the I/O logic, and then allows the configuration data to be loaded.

Depending on the mode—bit-sequential or byte-sequential—the load time will change by a factor of 8:1. The CLi6005, for instance, requires just over 8000 bytes of configuration data—in the byte-sequential mode, 8000 transfers can be done in about 8 ms. In the bit-sequential mode, however, over 64,000 transfers must be performed, which would increase the time required to more than 64 ms.

CHECKERBOARD SQUARE

The basic array architecture is reminiscent of a checkerboard within a checkerboard *(Fig. 1a)*. Each square of the checkerboard consists of an 8-by-8 array of identical programmable logic cells. A quarter of such an array is shown in Fig. 1a. Vertical and horizontal signal buses, each incorporating repeaters, make up the grids that separate each 8-by-8-cell block.

Each repeater drives both a local and an express signal bus, with each cell in the array connected to the local bus lines. The repeaters are inserted to buffer the propagating signals and regenerate them every eight cells. These operations minimize loading effects and thus improve device performance.

Signals can be routed from the lo-

cal bus to the express bus (or vice versa) through a repeater. Although that limits access to the express bus, it also reduces express-bus loading and thus allows signals to be routed across longer distances.

The repeaters can be programmed by the user to provide any of 29 different connection options. Some of those available options include isolating bus segments from each other, connecting two local-bus segments, connecting two express-bus segments, or, as mentioned earlier, providing a transfer path from a local bus to the express bus, or vice versa.

As a result, each logic cell ties into four local signal buses that are appropriately labeled East-West 1 and 2, and North-South 1 and 2 (EW_1, EW_2, NS_1, and NS_2, respectively). Signals from the buses can then enter or exit on any side of the cell *(Fig. 1b)*. In addition to connecting to the local buses, each cell also attaches directly to its four nearest neighbors through four ports.

Each port has two input lines (A_x and B_x), and two output lines (A and B), respectively (the x subscript refers to one of the compass points—N, E, W, and S). Signal paths that make a turn of 90° (switching from an E-W local bus to a N-S local bus or vice versa) are routed through cells, but they don't affect the normal operation of the cell.

Flexible Interconnections

The logic cell's flexibility basically comes from a simple arrangement of a D-register with an Ex-OR input buried with some gates and multiplexers *(Fig. 2)*. The input multiplexers enable the user to select any two of a total of ten possible inputs (eight from adjacent logic cells plus a fixed "1" input).

Output multiplexers route any of four signals to the A outputs and any of four signals to all four B outputs. The A multiplexer output also feeds signals to the local routing bus through four bidirectional pass gates, and can feed the signal back to the input of some of the cell's internal gates. Inputs from the local bus also go through the pass gates and through some selection logic. In all, a total of 20 combinatorial states, 11 register states, 4 constant states, and 4 three-state functions are possible with the cell.

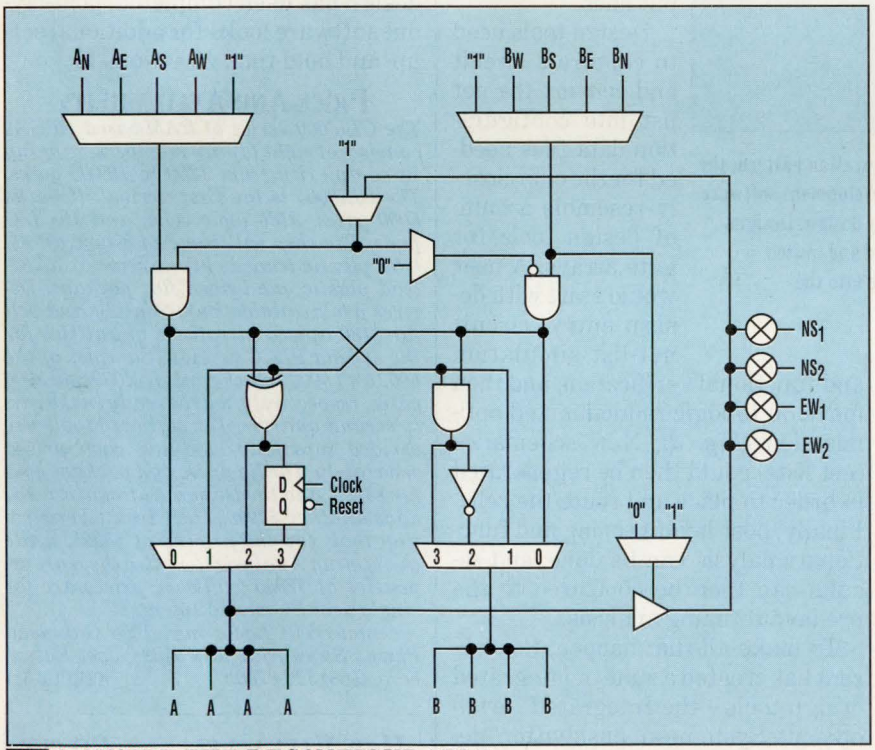
Thanks to the over 30 cell states, a rich and flexible set of logic functions can readily be implemented. Some of the functions are the expected NOR, NAND, AND, OR, and simple multiplexers, as well as many register options. These options range from a simple D-type register to versions preceded by a two-input multiplexer.

In addition to the local and express buses that criss-cross the chip, clock-distribution logic is embedded on the north end of the chip. It sends clock signals to the D flip-flops in every logic cell. The network is set up on a column-by-column basis, and allows each column of cells to be independently clocked. At the top of each column is a configurable multiplexer that passes one of four inputs: a global clock signal supplied by an off-chip source, a signal from the express bus closest to the distribution logic, the cell's output at the top of a column, or a constant "1" (no clock). Clock skew across a column is less than 100 ps, and less than 200 ps between adjacent columns. Across the entire chip, the clock-distribution scheme maintains the clock skew to less than 1 ns.

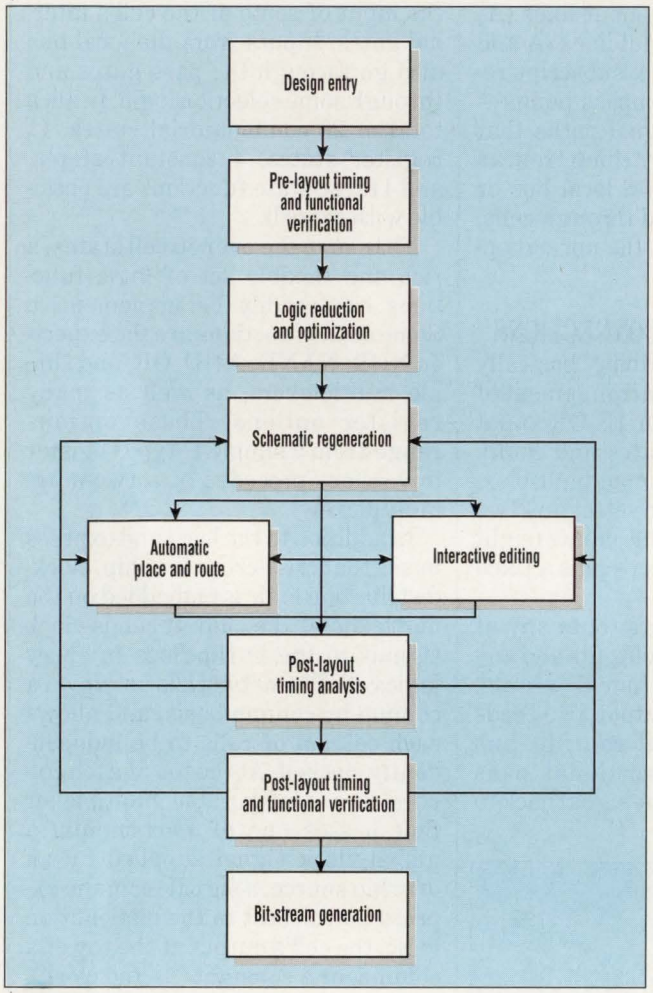
On the south end of the array is additional circuitry that implements asynchronous reset logic for the D flip-flops in the cells. As with the clock circuitry, the reset logic is configured on a column-by-column basis, allowing each column to be independently reset.

Surrounding the entire array are the configurable I/O cells, which contain an active pull-up and slew-rate control. Signals are received and sent via logic cells adjacent to the I/O cells—special entrance and exit cells.

Entrance cells accept the signal from the signal pin and route it to both the express and local buses. Exit cells accept inputs from express



2. INSIDE THE RECONFIGURABLE logic cell are a number of multiplexers that control the signal selection and routing. The cell can select any three of 14 input signals and deliver three signals to several output lines simultaneously. The cell can perform 20 combinatorial functions, 11 registered operations, and four constant operations.



3. TO DEVELOP THE RAM configuration pattern, the design flow using Concurrent's integrated development software looks very similar to the flow for a gate-array design. Designs are first entered, simulated, optimized, placed and routed, resimulated, and, when acceptable, converted into the configuration bit pattern.

and local buses and deliver a signal through a three-state buffer to the I/O pin. Entrance and exit cells can also be configured to provide registered inputs or outputs.

The CLi6005 comes in either 84- or 132-lead packages, giving the user a choice of I/O pin counts and a lower-cost option in the case of the 84-lead package. In addition to the multiple power and ground pins and up to 108 I/O lines, the chip has eight dedicated timing and control pins. Some of those pins include a Configuration Control line, which when brought low switches the chip into its configuration mode, and three mode-selection pins whose states determine the configuration mode that has been selected for the chip.

There are two clock pins (one configuration and one global) and a chip-selection pin that must be held low in addition to the Configuration Control line. The control lines also contain the Reset pin, which when pulled low, causes one or more columns of cells to be reset to their unconfigured state. Some of the I/O pins serve dual functions—during configuration they become address outputs, memory control, and data-input lines.

Design tools used to capture a circuit and convert the net list into configuration data files needed for the chip closely resemble a suite of design tools for gate arrays. A user would start with design entry, circuit net-list simulation and functional verification, and then move on to logic reduction and optimization *(Fig. 3)*. New schematics (net lists) could then be regenerated in order to place and route the cells. Finally, post-layout timing and functional analysis can be done, and results can then be compared to the pre-layout timing analysis.

To make all that happen, Concurrent has created a suite of integrated design tools—the Integrated Development System—a pushbutton design manager and a macrocell library that start by tying into the Viewlogic design-capture software. All of the software is set to run on 80386- or 80486-based PCs or compatibles. Versions that will run on popular workstation families will follow later in 1992. The software that Concurrent sells is divided into four main modules—the Basic Design Package, a Design Automation Kit, Circuit Verification tools, and Timing Analysis tools.

Schematics are captured by employing the macrocell library and Viewlogic's Viewdraw software. Viewsim, another package from Viewlogic, allows users to simulate the completed circuit, with results displayed in waveform format. Advanced timing analysis tools highlight critical timing paths and setup-and-hold violations on the layout, and back-annotate them to the schematic. Logic reduction and optimization helps eliminate logic redundancies and double inversions, and also helps the designer to find more efficient logic implementations.

Automatic placement and routing, along with an interactive interface, give the user total control over chip layout and signal routing. Once the design has been completed, post-layout software looks for additional setup- and hold-time variations.□

PRICE AND AVAILABILITY

The CLi6000 series of RAM-based FPGAs consists of eight family members, ranging in complexity from 1200 to 10,000 gates. The CLi6005 is the first arrival. It packs 5000 gates, 3136 logic cells, and 108 I/O pads. The chip will come in either an 84-lead plastic leaded chip carrier or a 132-lead plastic quad-sided flat package. Devices are available immediately and sell for $180 apiece in volume quantities for the 84-lead PLCC version. Samples of the 6002 and 6003, which contain 2000 and 3000 gates, respectively, will be ready in the early second quarter. The software tools are divided into four modules, each priced separately. The Basic Design package goes for $3995, and the Design Automation Kit adds another $3995. The Circuit Verification tools top the pricing at $4995, while the Timing Analysis tools are the least expensive at $2995 (software prices are for single-user PC environments).

Concurrent Logic Inc., 1290 Oakmead Pkwy., Sunnyvale, CA 94086; Joel Rosenberg, (408) 522-8700. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	560
MODERATELY	561
SLIGHTLY	562

486-Based Embedded VXI Controller Runs To 50 MHz

A 486-based embedded controller brings workstation-level performance to VXI systems without the throughput bottlenecks of an external controller. The EPC-7 is a two-slot, C-size module that comes in 33- or 50-MHz versions. All software developed for the industry-standard 386-based EPC-2 controller, including application programs, will run unmodified on the EPC-7.

The controller comes with a hard drive with up to 240-Mbyte capacity. A 3.5-in. floppy drive is optional. The unit includes a serial port and a printer port. Three SMB connectors permit external routing of VXIbus trigger and clock signals. A SCSI connector can be used for tape-backup devices or other storage media, such as optical disks.

The EPC-7 also incorporates the RadiSys Expansion Module (EXM) bus architecture. The EXM bus allows users to add up to four I/O expansion modules (three if the floppy drive is installed). An adapter module, which requires an additional VXI slot, holds two more EXM cards.

EXM cards currently available provide ports for IEEE-488, Ethernet, two additional RS-232 channels, RS-422, and RS-485. Also available are a modem, VGA controller (800 by 600 pixels), high-resolution VGA controller (1024 by 768 pixels), PC video controller, solid-state disk modules (up to 6 Mbytes), and an interval timer module. For specialized interfaces not available on EXM cards, the EPC7-AM adapter module holds a full-length PC AT card.

The controller runs EPConnect, a software development and runtime package that includes all the software defined by the VXIbus specification, such as resource-management software and VXI word serial communication drivers. The module also runs development tools and code generators from Giordano Associates, Hewlett-Packard, NCR, Tektronix, and Wavetek without modification.

EPC-7 prices start at $6995 for a base configuration that includes a 33-MHz 80486 CPU, 2 Mbytes of DRAM, a 52-Mbyte hard drive, a 3.5-in. floppy drive, and the EPConnect runtime package for DOS. A VGA graphics controller is available separately as an EXM module for $450.

RadiSys Corp. *19545 N. W. Von Neumann Dr., Beaverton, OR 97006; (503) 690-1229.* **CIRCLE 460**

■ *JOHN NOVELLINO*

GPIB Interface Offers 1.5-Mbyte/s Speed

The KPC-488.2AT is an IEEE-488.2 interface that supplies the fastest data transfer rate available. The board reaches data rates of 1.5 Mbytes/s on both read and write operations. In addition, a built-in software bus analyzer eliminates the need for a separate IEEE-488 bus analyzer. The KPC-488.2AT was developed by Capital Equipment Corp. and is marketed by Capital Equipment and Keithley MetraByte.

The KPC-488.2AT supports more operating systems and languages than other IEEE interfaces. Programmers can choose from DOS, Windows 3.0, OS/2, or SCO Unix operating systems. Instruments are controlled by either fast callable subroutines or by file I/O commands, which are language independent. The subroutines support most popular programming languages, including Basic, Visual Basic, C, Turbo C++, Pascal, and Fortran.

The interface works with Co-Operator, a toolkit for programmers that produces pop-up screens representing instrument front panels. Users push "buttons" on these front panels and Co-Operator automatically generates test program code in Basic, C, Pascal, or Fortran. In addition, the KPC-488.2AT is compatible with Keithley Asyst data-acquisition software, such as Asyst 3.1, Asystant GPIB, and Viewdac 2.0. The board works with all IEEE-488 devices and satisfies all requirements of the new IEEE-488.2 specification.

The KPC-488.2AT costs $495 and delivery is in two weeks.

Keithley Instruments Inc. *Data Acquisition Div., 440 Myles Standish Blvd., Taunton, MA 02780; (508) 880-3000.* **CIRCLE 461**

■ *JOHN NOVELLINO*

Board Tester Specifies Edge Placement To The UUT

The HP 3074 is a high-performance functional board tester that features HP Extended Edge Placement Accuracy (HP e_2PA), which specifies signal quality of $\pm$5.5 ns all the way to the unit under test (UUT). HP e_2PA automatically takes into account all path variables, including fixture wiring, variations in temperature and slew, and voltage offsets.

The tester has an application rate of 20 million patterns per second, with a 50-MHz drive clock capability and 80-MHz sync-to-clock capability. The HP 3074 incorporates the new Simplate XG-50 fixture, which can deliver a high-quality signal to the UUT at speeds to 50 million patterns per second. Instead of using twisted-pair wiring to ground high-frequency signals, the fixture's three-dimensional extended ground matrix consists solely of ground interface pins, UUT probes, and a custom ground plane. The Simplate XG-50 fixture is easy to build and debug and is compatible with other board testers in the HP 3070 family.

The system uses a new technology for fault dictionaries that cuts the diagnostic time needed to isolate intermittent failures by reducing the amount of manual probing required. To cut development time, designers can integrate test simulation tools from Mentor Graphics into the system. Other simulators, both design and test, can be linked to the HP 3074 through a variety of third-party tools.

The HP 3074 prices start at $350,000. Availability is 10 weeks after receipt of an order.

Hewlett-Packard Co. *19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.* **CIRCLE 462**

■ *JOHN NOVELLINO*

PC-BASED EMULATOR HANDLES 68HC16, 68300

Developers working with Motorola's 68HC16 and 68300 16-bit microcontrollers can use the EMUL16/300-PC in-circuit emulator to debug their systems. The PC-based emulator offers real-time emulation to the chips' full speed, which is currently 16.78 MHz, and can be used for higher-speed devices when they become available. Included in the package are a plug-in emulator board, a 5-ft. long twisted-pair cable, a pod board, and an optional trace board. The pod board has 1 Mbyte of breakpoint RAM, and the emulator board has 1 Mbyte of shadow RAM, which records all writes to both external and internal memory at full speed. The emulator software runs under Windows 3.0. Thus users can monitor several activities at once. For example, the shadow RAM can be displayed while the emulator runs at full speed. The EMUL16/300-PC is available immediately at a price of $1995.

Nohau Corp., 51 E. Campbell Ave., Campbell, CA 95008; (408) 866-1820. CIRCLE 463

HANDHELD DIGITAL SCOPE HAS 60-MHZ BANDWIDTH

The Model 224 handheld digitizing oscilloscope features a 60-MHz bandwidth and a 10-Msample/s sampling rate. The scope, which weighs only 4.4 lbs., is powered by two rechargeable batteries that run the unit for 3 hrs. The isolated-channel architecture isolates each of the scope's two channels from the other and from earth ground. As a result, true floating measurements can be made safely up to 400 V per channel or 800 V pk-pk. Users can store four front-panel setups in memory and four waveforms, for use as templates or for analysis. The unit is programmable through a standard RS-232C port. When linked to a PC with a modem, the Model 224 can be controlled with Tek's Virtual Instrument Software, CAT200. The scope's control can be manipulated through the keyboard or mouse, just as they would be handled manually on the instrument panel. Features include autoset, autolevel trigger, and TV field triggering. The Model 224 costs $2750 and is available 4 weeks after ordering.

Tektronix Inc., Test and Measurement Group, P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200. CIRCLE 464

MICROWAVE SWEEPERS FIT 2-SLOT VXI MODULES

A series of VXI-based microwave sweepers offers users a choice of four frequency ranges. The 2-slot, C-size modules are mounted in low-vibration, RFI-shielded housings with filtered and stabilized VXIbus control and power lines. This packaging arrangement offers performance that is superior to that of many bench or rack-mounted instruments. Level accuracy is ±0.5 dB for all models, and leveled output power is +10 dB. Options for pulse modulation and step attenuation allow the sweepers to act as signal generators. Users can select pulse widths to 100 ns and attenuations to 120 dB. Both options fit within the 2-slot package. A phase-lock option supplies 20-MHz resolution. Models and ranges include the Model 3251LS, 1 to 3 GHz; Model 3251SC, 2 to 8 GHz; Model 3251X, 8 to 12.4 GHz; and Model 3251Ku, 12 to 18 GHz. Prices start at $14,950, with delivery within 6 weeks.

Racal-Dana Instruments Inc., 4 Goodyear St., Irvine, CA 92718; (800) 722-3262. CIRCLE 465

FAST ANALOG I/O BOARD OFFERS 16 CHANNELS

The DAS-1600 is a fast analog I/O board that includes a 16-channel, 12-bit analog input section with a 100-kHz maximum conversion rate. The board works with IBM PC, XT, AT, 386, and 486 computers. The analog inputs can be configured as 16 single-ended or eight differential channels. Included are two analog outputs with 12-bit resolution and four switch-selectable output ranges. The DAS-1600 also has 32 bits of digital I/O—four input bits, 4 output bits, and 24 user-selectable bits. An on-board pacer clock makes it easy to time samples without the need for timing software or external signals. The board comes with a software driver that can be called from a number of Basic programming languages. The driver performs all necessary I/O and register functions. An optional Advanced Software Option helps users create custom applications. The DAS-1600 costs $899, and the ASO-1600 Advanced Software Option costs $200. Delivery is in four weeks.

Keithley MetraByte, 440 Myles Standish Blvd., Taunton, MA 02780; (508) 880-3000. CIRCLE 466

6U VME COPROCESSOR PERFORMS 1.1 BOPS

With the V-C40 Hydra VME-bus coprocessor board, 1.1 billion operations/s (BOPS) and a bandwidth of 240 Mbytes/s are possible. Ariel Corp. says that the board offers twice the processing performance and four times the I/O bandwidth of competitive 6U coprocessor boards.

Built with four TI TMS320C40 DSP processors, the Hydra features 64 Mbytes of DRAM and up to 5 Mbytes of zero-wait-state static RAM, organized in eight banks. Four of the eight banks serve as local memory, while the remaining banks operate as global memory. Each DSP processor has direct access to one local bank and one global bank through two independent 32-bit memory buses running at 100 Mbytes/s.

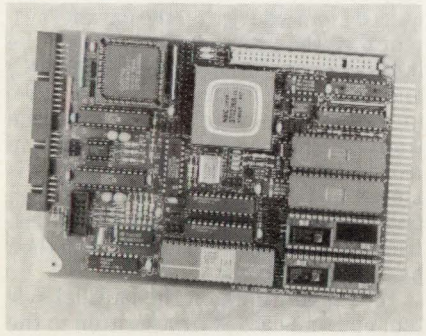
Each processor includes six byte-wide, bidirectional, parallel I/O ports, as well as a high-speed DMA controller. With six independently programmable DMA channels, the controller can be programmed to transfer data simultaneously through all six ports without interrupting program execution.

The Hydra can serve as either a bus master or slave. It supports block transfers of up to 35 Mbytes/s. An optional VSB interface allows users to customize the board for particular applications. Available now, Hydra starts at $9995.

***Ariel Corp.**, 433 River Rd., Highland Park, NJ 08904; (908) 249-2900.* CIRCLE 467

■ *RICHARD NASS*

PC/AT SBC REPLACES COSTLY STDBUS SYSTEMS

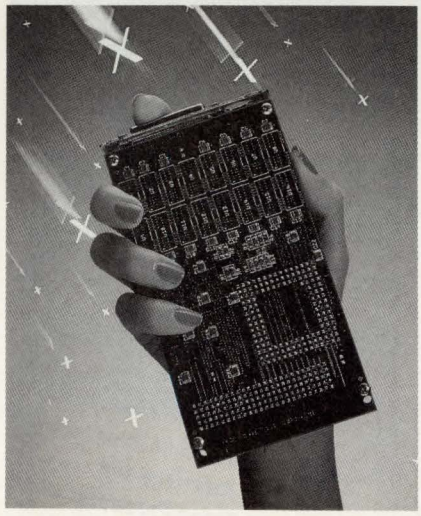


The cost of PC/AT compatibility on the STDbus slips under $400 with the MCM-SBC53 single-board computer (SBC). The 4.5-by-6.5-in. board replaces high-performance, high-cost, industrial PCs. The board's 2 Mbytes of storage and three I/O channels eliminate the need for multiple boards. The SBC is based on NEC's 10- or 16-MHz V53 CPU that's compatible with Intel's 80286 processor. An 80287 is supported, as well as EPROMs, EEPROMs, flash EEPROMs, and static, battery-backed, and pseudo-static RAMs. An optional 170-mAh battery can supply standby power for two of the memory sockets. Two software development tools, C-Thru-ROM and ROM-DOS, ease generation of application software for embedded applications. Available now, prices start at $399 in quantities of 500.

WinSystems Inc., 715 Stadium Dr., Suite 100, Arlington, TX 76001: (817) 274-7553. CIRCLE 468

SPARC-COMPATIBLE BOARD ACCELERATES X-WINDOWS

Text and graphics in an X windows system can be accelerated using the X-Cellerator MX. The single-slot board, designed for Sparc-compatible systems, supports a video resolution of 1280 by 1024 at 60 MHz and features off-screen memory to store fonts and pixel bit



maps. With the product, users receive X software, drivers, a dedicated graphics coprocessor, 4 Mbytes of local memory, a 64-by-64-pixel bit-mapped hardware cursor, a keyboard port, and an 8-bit color frame buffer.

Megatek Corp., 9645 Scranton Rd., San Diego, CA 92121; (619) 455-5590. CIRCLE 469

PROTOTYPING BOARD SPEEDS STD 32 DESIGNS

STD 32 board designers can speed up their development cycles using the STD 32 Developer and Prototyping kits. Both products come with the STD 32 bus specification, fabrication drawings and finger-pattern film, a license for STD 32 manufacturers and users, and data sheets for existing STD 32 products. Software is also included with both kits, supplying mechanical figures in AutoCAD format and OrCAD schematics. These files can be used as templates for new board designs or for mechanical dimensioning.

The prototyping kit adds a prototyping board for design proofs. The double-length board comes with or without the Extended Architecture extensions that permit high-performance memory transfers. CPU and I/O versions of the board are available. Both configurations supply seven +5-V locations for bulk capacitors, and one location each for positive or negative 12-V capacitors. Bypass-capacitor locations for ±12 V are included, as well as provisions for high-frequency +5-V bypass-capacitors. The developer's kit is priced at $90, while the prototyping kit costs $950 in either configuration.

***Ziatech Corp.**, 3433 Roberto Ct., San Luis Obispo, CA 94301; (805) 541-0488.* CIRCLE 470

■ *RICHARD NASS*

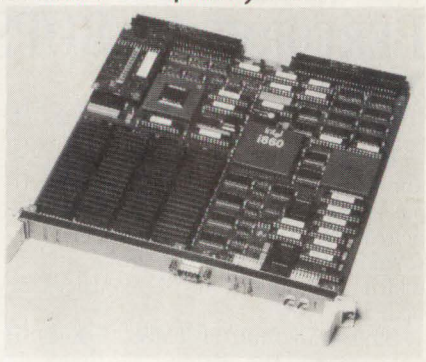
STDBUS BOARD COMBINES 486, 8 MBYTES DRAM

The MCM-SBC486 combines a 486SX or 486DX microprocessor and up to 8 Mbytes of on-board memory on an STDbus single-board computer. The PC/AT-compatible board supports both 8- and 16-bit data transfers. It automatically senses and switches to the proper mode. To insure compatibility with slower memory or I/O cards on the bus, the board switches speed while accessing the STDbus. The MCM-SBC486 comes with DMA controllers, three counter-timers, sixteen interrupt channels, a keyboard controller, and a battery-backed real-time clock. It also includes a power-fail reset and a watchdog timer for remote and unattended use. Prices start at $2895.

WinSystems Inc., 715 Stadium Dr., Suite 100, Arlington, TX 76011; (817) 274-7553. CIRCLE 471

2K-BY-2K DISPLAY CONTROLLER COMES IN BELOW $10,000

Designed for such embedded applications as manufacturing control, data processing, and graphics-based modeling, the M860 6U single-board computer (SBC) delivers 40 MIPS at 40 MHz. The board, from Mentec Computer Systems, Dublin, Ireland, is based on Intel's i860 RISC microprocessor operating at either 33 or 40 MHz and fits into a Multibus II backplane.



The board's memory (8 to 32 Mbytes) has been optimized to minimize the number of clock cycles that the processor has to wait to access memory. The first access to memory requires five cycles, but all subsequent accesses to the same page of DRAM will have zero wait states.

The I/O buffer area of the M860 contains 256 kbytes of 25-ns static RAM. The i860 uses this memory to buffer transfers to and from the parallel system bus. For example, if data is required from a device on the parallel system bus, the processor configures the message-passing coprocessor (MPC) and the DMA controller with the required parameters and allows the transfer to be completed under the control of these two devices. The data is placed in the static RAM buffer area and the processor is notified that the transfer is complete. The data can then be copied to the DRAMs.

To transfer data on the parallel system bus, the data is first written to the static-RAM buffer area and the MPC and DMA controller are programmed with the required parameters for the transfer. Then, the i860 can operate from main memory while the MPC and DMA controller transfer data from the static-RAM buffer area to the device.

The M860 contains eight programmable DMA channels, two of which are used in conjunction with the MPC to control data transfer over the parallel system bus. Three 16-bit programmable interval timers are included, as well as an RS-232-compatible programmable asynchronous serial interface.

With 8 Mbytes of DRAM and a 33-MHz processor, the M860 sells for $10,995. A 40-MHz board with 32 Mbytes of memory is priced at $19,995.

Mentec Computer Systems Ltd., *Dun Laoghaire Industrial Estate, Pottery Rd., Co Dublin, Ireland; (353) 1 2858444.* **CIRCLE 472**

■ *RICHARD NASS*

12-BIT VMEBUS CARD SAMPLES TO 10 MHZ

The MPV957 high-speed analog-input card for VMEbus systems provides sampling rates up to 10 MHz with 12-bit-resolution analog-to-digital conversion. Enabling fast block data transfers to main memory for laser scanners, high-speed industrial data-acquisition, and transient-analysis tasks, it comes in a 6U VME form factor.

The MPV957's accuracy is within ±0.2% of full-scale range at the 10-MHz maximum sampling frequency. It's supported with the MPV958 series of 4- and 8-Mbyte memory boards (64-Mbyte boards will be available early 1992). Use of the memory boards lets the MPV957 perform block transfers of converted data to main memory, allowing the MPV957 to operate at full conversion rate, while also giving the system access to recently acquired data.

Software-programmable features include the ability to switch between 8- or 12-bit resolution. The board has an internal 64-MHz clock and can also be clocked externally. Acquisition can be continuous, and initiated by an external trigger or through software.

On-board buffer memory will accommodate 256 12-bit samples or 512 8-bit samples. The MPV957's input-voltage range is ±1 V, with a programmable ±1-V offset to match individual system requirements. Input impedance is greater than 10 MΩ. The board, specified for operation over the 0 to 60°C temperature range, sells for $9,995.

Pentland Systems Ltd., 1 Cochrane Square, Brucefield Industrial Park, Livingston, West Lothian, EH54 9DR, Scotland; 44 0 506 464666. CIRCLE 495

DISPLAY LIVE VIDEO ON A VGA MONITOR

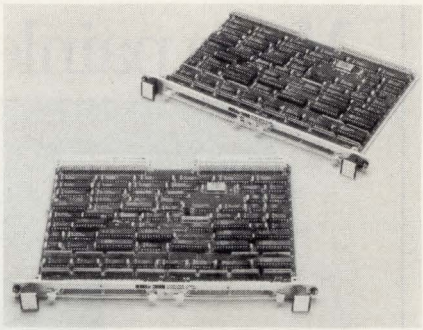
Live video can be displayed and manipulated on a VGA screen using the EXM-14 PC video acquisition board. In addition, images can be frozen, stored, and recalled. The input video signal can come in either RGB or composite form from such devices as television cameras, camcorders, and VCRs. The signal is combined with the graphics output from the attached VGA controller, then to a VGA monitor that's plugged into the board. Applications include integrated manufacturing systems, automated test equipment, and medical electronics. The board is available now for $1250.

RadiSys Corp., 19545 NW Von Neumann Dr., Beaverton, OR 97006; (503) 690-1229. CIRCLE 473

SEND SIGNALS FROM ONE VME CHASSIS TO ANOTHER

Using the Model 417 Repeater, a VMEbus backplane can be extended from one chassis to another, transparent to the system. The two-board set repeats the VME-32 or VME-64 bus architecture outside a primary VME chassis to a secondary chassis so that they operate as one integrated system. Users simply plug the two boards in and they're ready to go. There's no software overhead and no hardware configuring to do. One of the two boards goes into slot one of the secondary chassis and the other board goes into any slot except slot one in the primary chassis.

The repeater supports A16, A24, A32, and A64 addressing; D8, D16, D32, and D64 data sizes, and all transfer, release, and arbiter selections. Maximum signal delay is 100 ns. Signals driven from one chassis to the other are retimed so that timing specifications aren't compromised. Trapezoidal transceiver circuitry is used to reduce crosstalk and ensure signal integrity. In single quantities, the Model 417 repeater sells for $1445.



Bit 3 Computer Corp., 8120 Penn Ave. S, Minneapolis, MN 55431; (612) 881-6955. CIRCLE 474

■ *RICHARD NASS*

DATACOM CHIP IDENTIFIES INCOMING-CALL SOURCE

The XR2211 caller-ID circuit from Exar Corp. decodes frequency-shift-keyed (FSK) modem signals for displaying the calling number at the user's premises while the phone is on-hook. For use in telephones, facsimile machines, modems, answering machines, and PBXs, the phase-locked loop (PLL) system operates on 4.5 to 200 V dc, and over a frequency range of 0.01 Hz to 300 kHz. It can handle analog signals ranging from 2 mV to 3 V, and interface with DTL, TTL, and ECL logic families.

The circuit consists of a PLL for tracking an input signal within the passband, a quadrature-phase detector for carrier detection, and an FSK voltage comparator which provides FSK demodulation. External resistors and capacitors set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power-supply voltage provides ratiometric operation to minimize system performance variations with power-supply changes.

Available in a 14-pin plastic DIP for commercial- or military-temperature ranges, the XR2211 is priced at $0.65 each in quantities of 250,000.

***Exar Corp.**, 2222 Qume Dr., San Jose, CA 95161-9007; (408) 434-6400.* CIRCLE 475

■ *MILT LEONARD*

ISDN TRANSCEIVER CHIP SKIMPS ON POWER

The T7264, a 2B1Q transceiver IC, meets the full T1.602-1991 ANSI standard for ISDN while consuming just 275 mW typical. The transceiver encodes, transmits, receives, and decodes digital signals carried over conventional telephone lines. The lines serve on the central-office and customer sides of a 2-wire communications link. Low power consumption results from the device's mixed-signal technology, which also provides superior analog performance on a 2B1Q line. Fabricated in AT&T's 0.9-**m**m linear CMOS technology, the T7264 is available now in sample quantities. Full production of a 44-pin PLCC-package version is scheduled early next year, and is priced at $27 each for production quantities.

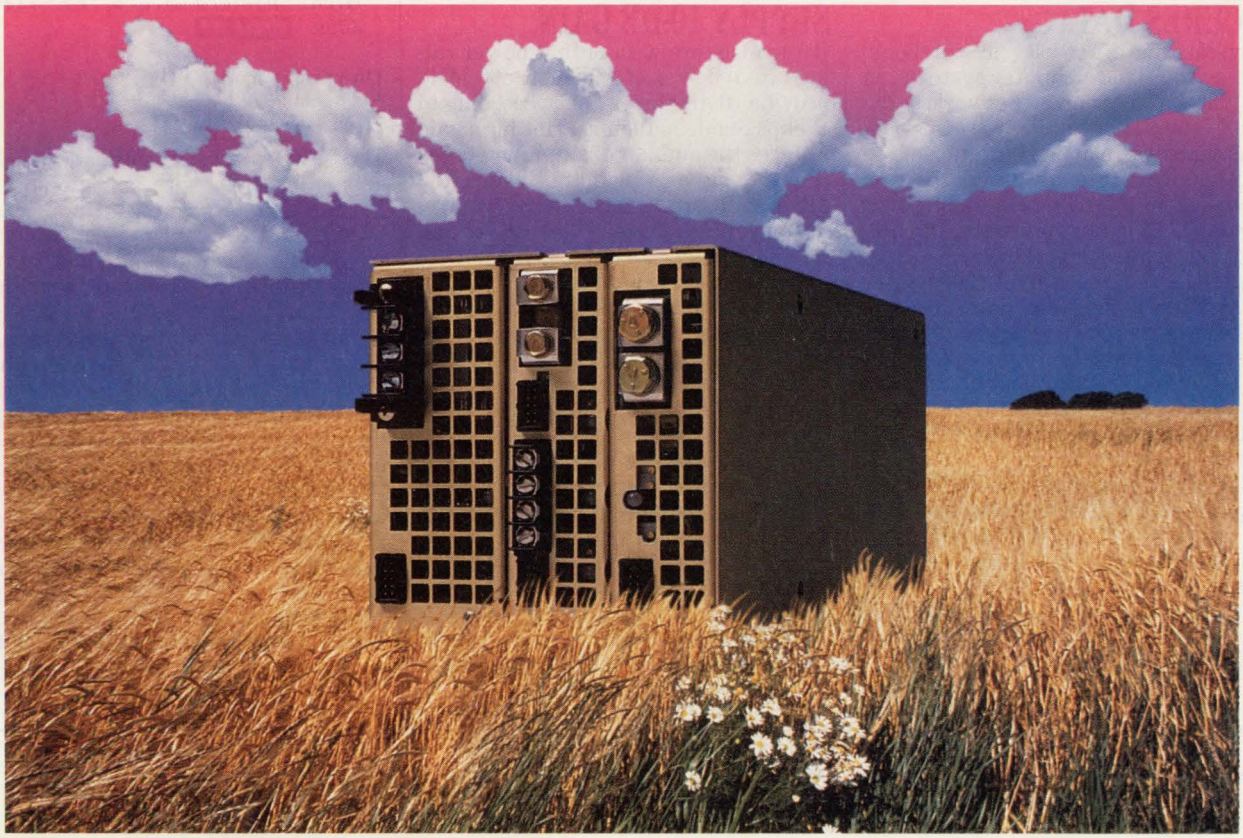
AT&T Microelectronics, Dept. 52AL040420, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447, ext. 809. CIRCLE 476

RF SWITCH SLASHES POWER CONSUMPTION

Consuming one-tenth the power of other RF switches, the NE/SA630 is a bidirectional single-pole, double-throw switch that handles wideband signals ranging from dc to 1 GHz. The part draws 140 μA from a 5-V supply and has a typical throughput loss of 1 dB at 200 MHz. Off-state isolation is 50 dB at 400 MHz and 27 dB at 1 GHz. With a typical 25-ns switching time, the switch accommodates data rates up to 400 MHz. To prevent unwanted oscillation in the off channel, unused inputs of the device are internally terminated at 50 Ω. The part is also protected from electrostatic discharge. Typical applications include video switches, FSK transmitters, filter selectors, antenna switches, and digital cellular front-end switches. Available in an 8-pin plastic DIP or surface-mount package, the switch is priced at $2.79 each in quantities of 100.

Signetics Co., 811 E. Arques Ave., Sunnyvale, CA 94088-3409; (408) 991-2000. CIRCLE 477

THIS YEAR'S HARVEST HAS YIELDED SOME COLORFUL RESULTS



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1-800-233-9973

For Literature or Information

CIRCLE 139 FOR U.S. RESPONSE CIRCLE 140 FOR RESPONSE OUTSIDE THE U.S.

ENCRYPTION CHIP SECURES DATA

Providing data security in notebook, laptop, and fixed computer systems, as well as in local-area networks, the VM007 data-encryption processor contains a hardware implementation of the National Institute of Standards and Technology (NIST) data-encryption standard. At maximum speed, the programmable device can encrypt or decrypt data at a rate of over 190 Mbits/s in any mode using 64-bit data words. A flow-through architecture supported by separate plain-text and cipher-text ports provides simultaneous data transfer into and out of the device. A built-in self-test program tests the device upon power-up.

Currently sampling, the VM007 encryption chip will be available in an 84-pin ceramic LCC in commercial- and military-temperature ranges for $750 each in quantities of 1000.

VLSI Technology Inc., 8375 South River Pkwy., Tempe, AZ 85284; (602) 752-8574. CIRCLE 478

RF TRANSISTORS SUPPLY 10-DB GAIN

RF transistors with output power ratings of 100 W and 150 W at 500 MHz provide 10-dB power gain, according to Philips Semiconductors. This high gain reduces the number of amplifier stages required in a transmitter, while the MOS structure ensures easy control using voltage drive. The BLF547 and BLF548 are VHF/UHF n-channel enhancement-mode vertical D-MOS push-pull transistors and feature gold metallization. The devices have no internal input or output matching networks, which allows them to cover broadband rf applications from VHF to UHF in communication transmitters. Nominal supply voltage is 28 V with efficiency of more than 50%. The transistors come in a four-lead balanced flange package with two ceramic caps (SOT-262A2). Pilot prices are Hfl 235 (BLF547) and Hfl 350 (BLF548) at Hfl 1.74 = $1 US; prices depend on importing country.

Philips Semiconductors, Eindoven, The Netherlands, 31 40 722091; Philips Components, 2001 West Blue Heron Blvd., Riviera Beach, FL 33404-5099. CIRCLE 479

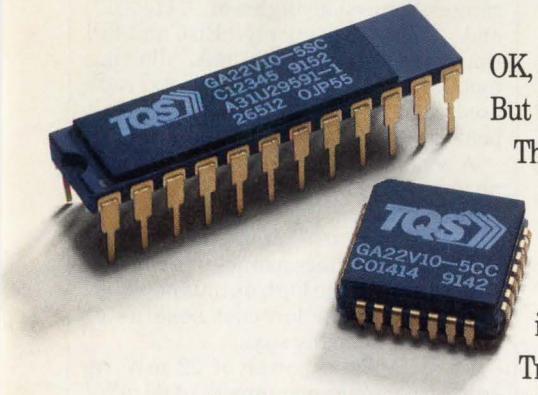
ETHERNET IC SWITCHES BETWEEN MEDIA

The 82503 is an AIU/10Base-T single-chip transceiver with an auto-port-selection feature that automatically switches a LAN controller between coaxial-cable Ethernet and common unshielded telephone twisted-pair Ethernet (TPE). Ordinarily, an Ethernet port requires an serial-interface device for connecting it to a LAN controller, and a TPE requires both a serial interface and a attachment unit. The 82503 combines both functions on one chip. It also detects and corrects polarity errors on the twisted-pair wire. Intended for use in portable, desktop, and workstation platforms, the transceiver is packaged in a PLCC and is priced at $10 each in quantities of 1000.

Intel Corp., 3065 Bowers Ave., P. O. Box 58065, Santa Clara, CA 95052; (800) 548-4725. CIRCLE 480

For years, people have been trying to run 100 meters in under 9 seconds, clear 8 feet in the high jump, and hit 5.5 ns in a 22V10 PLD.

We're still having some trouble with the first two.



OK, the Olympics may not be in our future.
But the 5.5 ns barrier is history.

The 125 MHz* TriQuint GA22V10-5 isn't just a pipe dream. It's proven. TTL-compatible. Price-competitive. And shipping right now.

We make it available in both surface-mount and DIP packages.

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*125 MHz external, 200 MHz internal

CIRCLE 129 FOR U.S. RESPONSE

CIRCLE 130 FOR RESPONSE OUTSIDE THE U.S.

TRANSISTOR PUSHES 32 W IN PCN BASE STATIONS

An output power 50% higher than any of the company's transistor types promises to turn Philips Semiconductors' 32-W LXE18300X into a new industry standard for transmitting transistors. Aimed at Personal Communications Network (PCN) base stations, the bipolar transistor will give a big boost to the power needed to service mobile phones in densely populated areas (particularly during peak hours). The common-emitter device also has a high power gain—typically 10 dB to reduce the number of the transmitter's amplification stages. The LXE18300X is a microwave silicon power transistor that works as a high-performance amplifier in class AB transmitters. The output power is 32 W for 1 dB compression, measured at 1.85 GHz at a 24-V supply and 300-mA collector current. Intermodulation distortion is below –30 dBc at an average output power of 15 W. The efficiency is a high 44%.

Besides reducing end-user equipment running costs, this allows operation with a junction temperature of only 98°C. That lengthens the device's operating life. The transistor comes in an FO-91 hermetically sealed metal ceramic envelope. The Philips LXE18300X sells for between $220 and $350 apiece depending on quantity. Samples are available now.

In Europe, Philips Semiconductors, P. O. Box 523, NL-5600 AM Eindhoven, The Netherlands. Contact Arnold Blekking, phone 0031 40 722091. In U.S., Philips Components, Discrete Products Division, 2001 West Blue Heron Blvd., Riviera Beach, FL 33404-5099; contact: Miriam Coleman, (407) 881-3257. CIRCLE 481

IR LED EMITTERS BRIDGE SPEED GAP

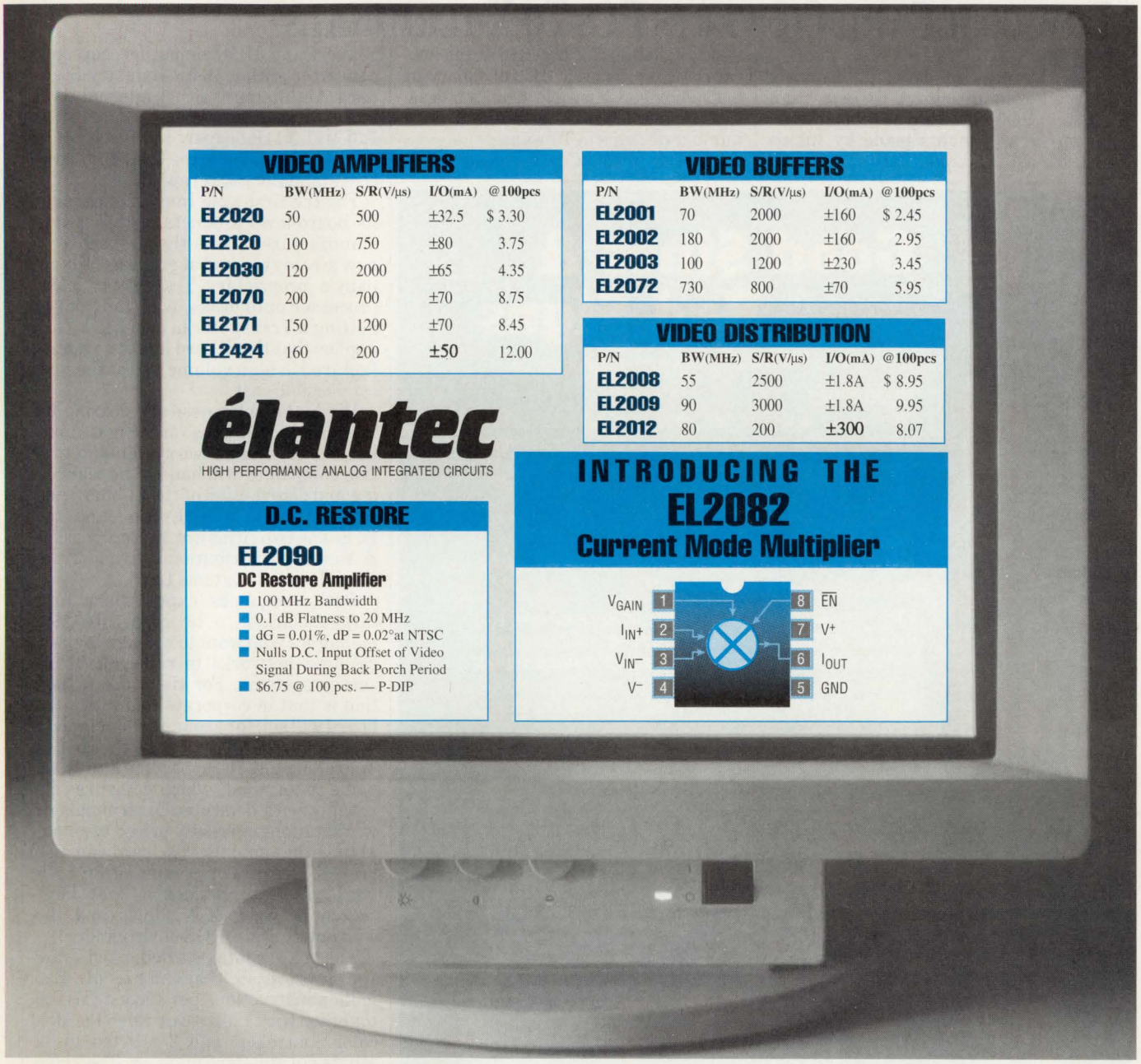
The introduction of the SFH474, SFH475, and SFH476 extends Siemens's range of infrared (IR) LED emitters. These are intended to bridge the gap between low-speed, general-purpose IR emitters and high-cost, high-speed fiber-optic emitters, the company says. The emittters cover the range of emission angles of ±11, ±17, and ±28°, respectively. Rise-and-fall times are 100 ns at 100 mA, allowing modulation at up to 5 MHz. Total radiated power is 10 mW at 100 mA with a peak wavelength of 830 nm.

A second group of devices is designated SFH414, SF415, and SF416. These offer similar emission half-angles of ±11, ±17, and ±28°, respectively. The emitters use a new technology to combine the high output power of GaAlAs with the low-cost benefits of GaAs, the company says.

Total radiated power of 22 mW results in a minimum intensity of 63 mW/steradian at 100 mA (type SFH414-V). All the emitter devices are available in the standard T1-3/4, 5-mm plastic package. Available now, the devices are $0.35 apiece in thousands.

Siemens Components Inc., Opto-Electronics Div., 1900 Homestead Rd., Cupertino, CA 95014; (408) 725-3508. CIRCLE 482

élantec opens your window — to the video world!



VIDEO AMPLIFIERS

P/N	BW(MHz)	S/R(V/µs)	I/O(mA)	@100pcs
EL2020	50	500	±32.5	$ 3.30
EL2120	100	750	±80	3.75
EL2030	120	2000	±65	4.35
EL2070	200	700	±70	8.75
EL2171	150	1200	±70	8.45
EL2424	160	200	±50	12.00

VIDEO BUFFERS

P/N	BW(MHz)	S/R(V/µs)	I/O(mA)	@100pcs
EL2001	70	2000	±160	$ 2.45
EL2002	180	2000	±160	2.95
EL2003	100	1200	±230	3.45
EL2072	730	800	±70	5.95

VIDEO DISTRIBUTION

P/N	BW(MHz)	S/R(V/µs)	I/O(mA)	@100pcs
EL2008	55	2500	±1.8A	$ 8.95
EL2009	90	3000	±1.8A	9.95
EL2012	80	200	±300	8.07

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INTRODUCING THE EL2082
Current Mode Multiplier

EL2082 200 MHz Current Mode Multiplier APPLICATIONS

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CIRCLE 178 FOR U.S. RESPONSE CIRCLE 179 FOR RESPONSE OUTSIDE THE U.S.

LOW-COST CARD CONVERTS PCs TO X-TERMINALS

The cost of Unix X-terminals could plummet to less than $1000 following novel manufacturing arrangements made by Inmos Ltd. for a PC adapter card. To ensure wide availability of the card at the lowest cost, the Bristol, UK subsidiary of SGS Thomson Microelectronics has assigned manufacturing licenses to a number of firms in Taiwan.

The IMS B020 iX card is designed to convert any IBM-compatible personal computer with a 16-bit Industry Standard Architecture (ISA) internal data bus into an X-Windows terminal with full MIT X11R4 capability. But it could also be used to form the basis for a low-cost standalone X-terminal.

For the first time Inmos is licensing its board-level products to third-party manufacturers. It is the first move in new strategy aimed at getting the company's proprietary Transputer RISC processor onto desks, with the goal of getting a Transputer in every PC. That implies that the iX card has to be manufactured in high volume and at the lowest possible cost.

While the Taiwanese are gearing up their production lines for the mass market, closer to home two system-integration companies will handle the marketing and distribution of the iX board and related products in Europe and the U. S. The two firms are Microprocessor & Memory Distribution Ltd. and Transtech Parallel Systems Ltd.

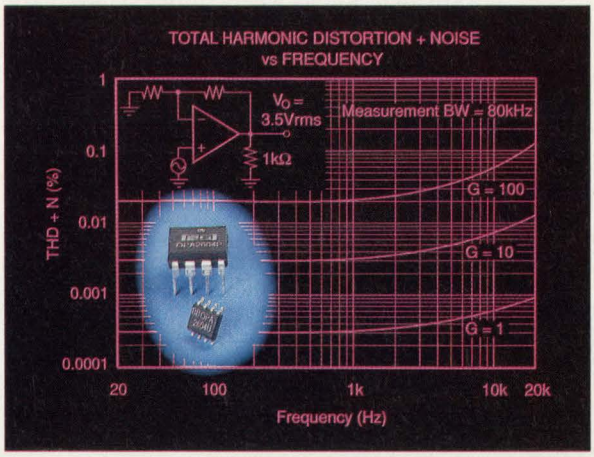
Both companies expect their first target market to be corporate MIS managers who want to convert their local area networks to run Unix-based server systems. For them the attraction is that in corporate quantities the board will sell for around $800 complete with software. That will be the cost of upgrading any PC to become a fully capable X-terminal, which compares favorably with dedicated X-terminals or workstations currently priced at several time that amount. The card can also protect investment in existing PC software since it provides a "hot key" switch between X-Windows and the conventional MS-DOS environment.

The board contains a dedicated Transputer processor that can execute 12.5 million instructions per second (MIPS) together with 1 Mbyte of video RAM; a color controller; and 2 Mbytes to 12 Mbytes of standard memory. The video display driver supports screen resolutions of up to 1,024 by 768 pixels with up to 256 colors displayed simultaneously on a standard low-cost video graphics adapter (VGA) display or an enhanced high-resolution super VGA screen. To take advantage of the card's capabilities, a separate higher resolution monitor can be used for applications such as computer-aided design. Inmos is developing a fiber distributed data interface (FDDI) terminal adapter module.

***Inmos Ltd.**, 1000 Aztec West, Almondsbury, Bristol, BS12 4SQ, UK; 44 0454 617910.* **CIRCLE 483**

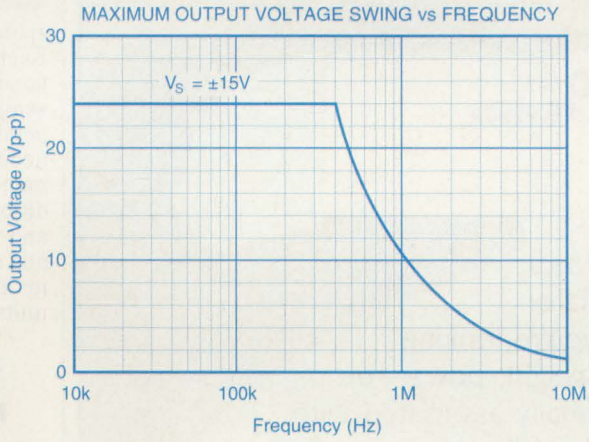
■ *PETER FLETCHER*

Dual Op Amp Delivers High Speed, 0.0003% THD+N



More For Less

With our new OPA2604 dual, FET-input op amp you'll get 20MHz gain-bandwidth, 25V/µs slew rate, and very low harmonic distortion. Just right for active filter, spectrum analyzer, and transducer amplifier applications, and more. It's also pin compatible with the "industry standards". Just drop it in and power it up. If you're working in dynamic signal processing, you should be working with the OPA2604. Better performance at a super price is hard to beat.



These Features Tell The Story

- Slew Rate 25V/µs
- Gain-Bandwidth 20MHz
- Noise ..... 10nV/√Hz
- THD + N 0.0003%
- Input Bias Current 100pA
- Supply Range ..... ±4.5V to ±24V
- Unity-Gain Stable
- 8-pin Plastic DIP and 8-lead Plastic SOIC
- From $1.35 each in 1000s. U.S. OEM prices.

Great For Audio

The sound quality of the OPA2604 is excellent. Its low noise, low distortion, and low price make it ideal for professional audio equipment, compact disc players, and digital/audio tape player/recorders. And, its wide supply range and ability to drive 600Ω loads is also a plus. For a detailed data sheet and samples contact your local Burr-Brown sales office, or call **1-800-548-6132.**

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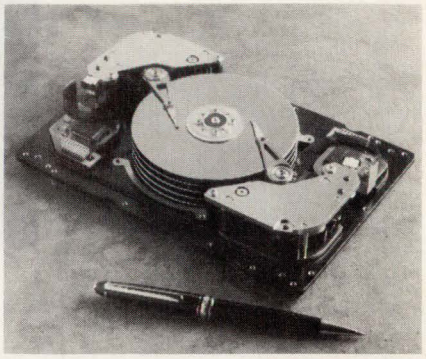
CIRCLE 176 FOR U.S. RESPONSE

CIRCLE 177 FOR RESPONSE OUTSIDE THE U.S.

DUAL-ACTUATOR DRIVE HANDLES 140 I/OS PER SECOND

Up to 140 I/Os per second can be handled by the dual actuators of Conner Peripherals' Chinook hard-disk drive. The 510-Mbyte, 5-1/4-in.-form-factor drive is targeted toward applications where throughput is critical to overall system performance, such as high-end workstations, file servers, client-server applications, and multi-user systems.

Typically, data is stored to and retrieved from the rotating disk one request at a time. A bottleneck results when too many requests are made simultaneously, a common occurrence in I/O-intensive applications. The Chinook drive solves this problem by implementing dual actuators, located 180° from each other. The two actuators respond to data requests independently. Each of the two data paths has an independent channel, buffer controller, and sequencer. This design allows two independent processes to occur simultaneously, nearly doubling the performance of single-actuator drives. In addition, because both actuators can read and write data, the effective seek time and rotational latency is cut in half, to 3 ms and 6.7 ms, respectively. Evaluation units are available now for $1595.



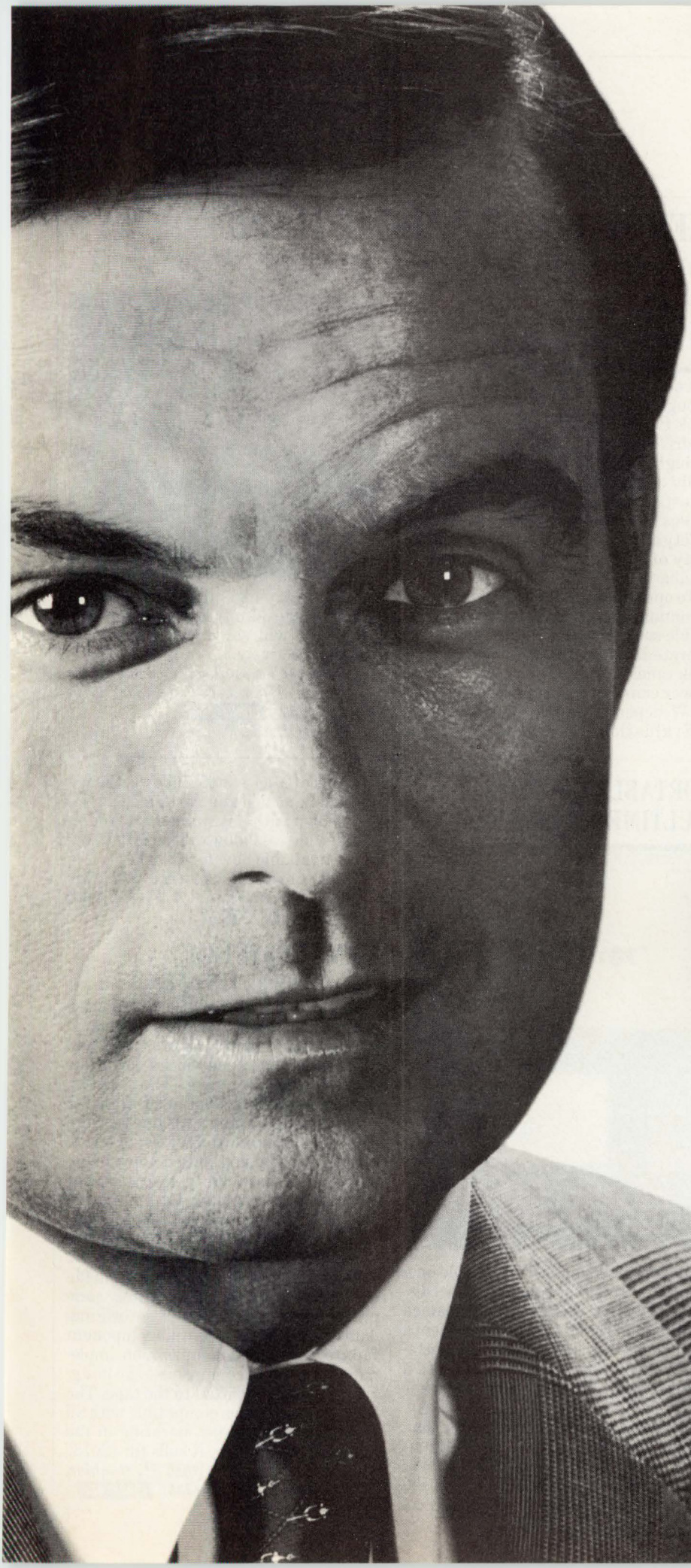
Conner Peripherals Inc., 3081 Zanker Rd., San Jose, CA; (408) 456-4500. CIRCLE 484

■ *RICHARD NASS*

AUDIO INTERFACE IMPORTS ANALOG SIGNAL

Using the ProPort Model 656, users can send recording-studio-quality analog audio to ISA, EISA, Sun, VME, Macintosh, HP, and Next computers. The self-contained digital-audio interface operates through the computer's serial port. The ProPort's programmable sample rate ranges from 5 to 96 kHz, making it suitable for any application that requires high-quality signal I/O in the audio domain, including speech processing, laboratory data acquisition and signal generation, or speech research. The 96-kHz sample rate produces a passband that's flat to ±0.1 dB from 20 Hz to 40 kHz. Built-in tracking input filters prevent aliasing. Available now, the ProPort 656 sells for $1595.

Ariel Corp., 433 River Rd., Highland Park, NJ 08904; (908) 249-2900. CIRCLE 485



"Direct mail can be informative, but I get more useful information from my trade magazines."

Your customers and prospects do get helpful information from the direct mail they receive. But, the fact is, the buying influences you need to reach depend more on their trade publications for information that helps them make buying decisions. A recent study, conducted by the Forsyth Group, confirms it.

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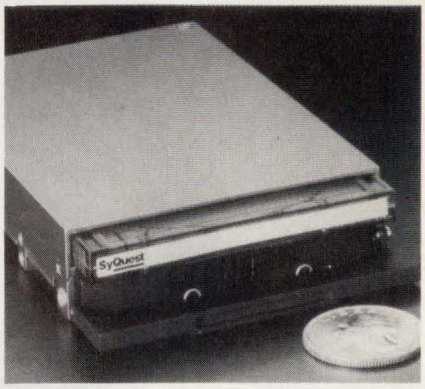
REMOVABLE 42.8-MBYTE HARD DRIVE FITS 2-1/2-IN. SPACES

Unlimited storage can be obtained by using removable cartridges in a Winchester-disk drive. And now, those drives are small enough to fit in a laptop or even notebook PC. The SyQuest SQ2542A 2-1/2-in. drive holds 42.8 Mbytes on each 1/4-in.-high cartridge. The drive is mechanically and electrically compatible with industry-standard 2-1/2-in. hard-disk drives. Removable cartridges offer safety and security, as well as the flexibility of carrying large applications or databases anywhere.

To optimize seek time and power consumption, the drive offers a programmable-seek capability. The drive can operate in three different modes, with seek times ranging from 14.5 to 22 ms. Power consumption ranges from 1.4 to 1.2 W, depending on the seek time used.

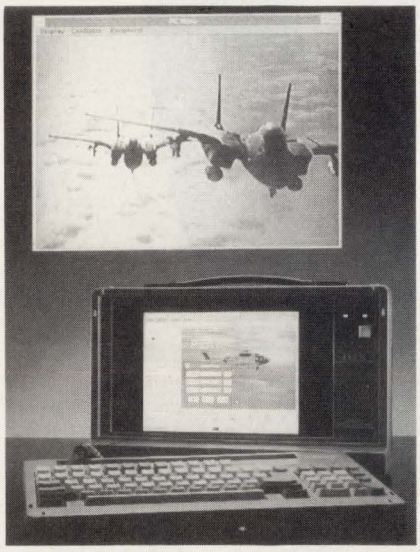
Evaluation units of the SyQuest SQ2542A hard-disk drive are available now. In large quantities, the drives and cartridges will sell for $250 and $60 each, respectively.



SyQuest Technology, *47071 Bayside Pkwy., Fremont, CA 94538; (510) 226-4150.* **CIRCLE 486**

■ *RICHARD NASS*

PORTABLE CARRIES MULTIMEDIA IMAGES



Full-motion video is now available on a thin-film-transistor color flat-panel display. The MPAC display can be teamed with any of Dolch Computer System's high-end 386- and 486-based PAC portable systems. The Dolch display uses a Sharp 640 by 480 thin-film transistor (TFT) display, which yields 24,389 colors with a response time of better than 40 ms. The video picture can be input from most industry-standard analog sources. By using the Multimedia Extensions of Microsoft Windows, the image can be scaled and positioned at will and shown with any number of freeze-frame video windows. The MPAC option is available now for $3995.

Dolch Computer Systems, 372 Turquoise St., Milpitas, CA 95035; (408) 957-6575. **CIRCLE 487**

8-MM SUBSYSTEM REACHES 25 GBYTES

Exabyte Corp.'s EXB-8500c 8-mm cartridge tape subsystem offers the largest capacity, fastest transfer rate, and quickest search speed in its form factor, the company says. The 5-1/4-in. tape drive offers sustained transfer rates of up to 25 Mbytes/s and storage capacities of up to 25 Gbytes on one 8-mm cartridge using data compression. High-speed searches achieve a rate of 187.5 Mbytes/s. In an uncompressed mode, the drive stores 5 Gbytes, transfers data at 500 kbytes/s, and searches at speeds up to 37.5 Mbytes/s. The drive's compression scheme immediately decompresses data after compression and compares it to the original data. This is to ensure that component failure within the compression implementation won't compromise the integrity of the data written to the tape. The EXB-8500c remains compatible with all Exabyte drives while operating in the uncompressed mode. It sells for $2675.

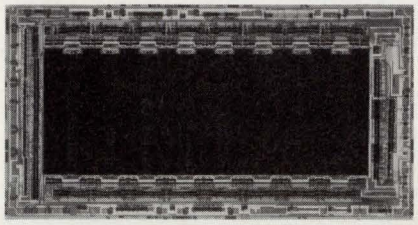
Exabyte Corp., 1685 38th St., Boulder, CO 80301; (303) 442-4333. **CIRCLE 488**

2-MBIT VRAM OPTIMIZED FOR GRAPHICS SYSTEMS

Packing double the number of bits of other video RAMs—2 Mbits—the μPD482234 and 482235 VRAMs have also been optimized to handle the higher bandwidth data and faster display refresh requirements of graphic subsystems. The dual-ported memories from NEC are organized as 256 kwords by 8 bits and include a 4-kbit data register as well as a 512-word-by-8-bit byte-serial I/O register. The host DRAM port of either chip can be accessed in 70 or 80 ns, depending on the speed grade. Data can be transferred over the byte-wide video port at 17-ns/byte for the 70-ns version and 20 ns/byte for the 80-ns option.

The 482235 differentiates itself from the 482234 by offering a new high-speed transfer mode the company calls hyperpage. The 482235 reduces transfer times over the CPU port. The standard fast-page mode version allows 45-ns/byte transfers for data in the current row. The hyperpage version achieves a transfer time of 35 ns/byte by extending the duration of the data output and thus extending the data-valid time. That allows the page-cycle time to be shortened.

Both chips improve on the company's previous 1-Mbit VRAMs—a serial write cycle, split write and masked-write transfers, serial I/O direction switching, stopping-column control capability, and a special-function output



signal. The serial-write feature improves screen-clear operations, while the others are more geared for overlays and image movement. At maximum speed, the VRAMs dissipate about 800 mW. The chips are available in 40-lead SOJs and shrink ZIPs, and 44-lead TSOPs. In sample quantities either VRAM is $30 each. Samples are available now.

NEC Electronics Inc., 401 Ellis St., P. O. Box 7241, Mountain View, CA 94039; Tom Nishimura, (415) 965-6177 **CIRCLE 489**

■ *DAVE BURSKY*

FOUR-CHANNEL DMA CHIP HANDLES MULTIPLE BUSES

Able to control direct-memory-access transfers at up to 66 Mbytes/s, the MB92411 quad-channel DMA controller can tie into most 32-bit CISC or RISC microprocessors. The Fujitsu chip can even be controlled by two microprocessors in the same system that either share one bus or operate on separate unmatched buses. The dual control capability is made possible thanks to an on-chip 16-byte message buffer and a four-byte data-hold register that handles the data alignment. Such resources suit the chip for bus-master applications in which two different buses and processors are trying to control the data flow. Dynamic bus sizing is implemented by the chip so that the controller can handle data transfers between buses with different widths. The controller provides a 32-bit address and handles 8-, 16-, or 32-bit data transfers.

The chip supports burst, cycle-steal and fly-by data transfer modes and operates at clock rates of 20, 25, and 33 MHz. Those three clock speeds yield data transfer speeds of 26.7, 33.3, and 44 Mbytes/s. If the block transfer mode is used, transfer speeds increase to 40, 50, and 66 Mbytes/s, respectfully. By using two DMA controllers in tandem, memory-to-memory fly-by operations can be implemented. The four independent channels can be prioritized in any of four ways and can also be multiplexed to provide optimium system utilization. Multiple DMA sequences can also be executed consecutively by employing the chip's sequential- or link-descriptor chain modes.

Available from stock, the MB92411 comes in a 172-lead ceramic pin-grid-array package. In lots of 1000, the chip sells for $110, $120, or $135, respectively for the 20-, 25-, and 33-MHz versions.

***Fujitsu Microelectronics Inc.**, IC Div., 3545 N. First Street, San Jose, CA 95134-1804; Charlie Shafton, (408) 922-9000.* **CIRCLE 490**

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ZERO-POWER PLDs CLAIM TOP SPEED FOR CLASS

Offering the shortest delays of any 20-pin zero-power programmable logic chips, the PLC18V8Z-25 offers a propagation delay of just 20 or 25 ns. On standby the chip consumes just 100 μA, and when active the chip current drain increases by 1.5 mA/MHz, to a maximum power at 30 MHz that is about one-fourth that of the power consumed by conventional PAL devices. The chip has two-level logic elements and 10 inputs, 74 AND gates, and 8 output macrocells. JEDEC files for the popular 16V8 and other PAL devices can be used to program the PLC18V8Z using the SIMPAL-2 software the company offers at no charge to chip customers. Additional software support comes in the form of Snap design software, which runs on a PC and can synthesize and optimize logic functions from a netlist.

To implement the zero-power logic the chip employs input transition detection circuitry to detect system bus activity and automatically adjust the current consumption. Three versions of the chip will be available—two 20-ns versions rated for the commerical and industrial temperature ranges (0 to 70 and –40 to +85 °C) and a militarized version rated at 25 ns and spanning –40 to +125 °C. The chip comes in three packaging options as well—a 20-pin ceramic windowed DIP, a 20-pin plastic DIP, and a 20-lead PLCC. The plastic DIP version sells for $3.75 apiece in lots of 1000. Samples are available now.

***Philips Semiconductors, Signetics Co.**, 811 E. Arques Ave., P. O. Box 3409, Sunnyvale, CA 94088-3409; Frank Logan, (408) 991-2355.*

CIRCLE 491

■ *DAVE BURSKY*

TAB-BASED SPARC CARD TRIMS SIZE, UPS SPEED

The CYM6122L 10-chip dual-CPU Sparc module runs at 40 MHz, condensing its already compact dual-processor module by taking advantage of tape automated bonding. The module reduces the space required for a two CPU implementation from the postcard-sized CYM6002K Sparc module to a card about half the size—just 3.3 by 2.5 in. On the card are two CY7C601 integer CPUs, two 7C602 floating-point processors, two 7C605 multiprocessor memory managers, and four 7C157 cache RAMs. Like the previously released card, the 6122L attaches to the Sun Mbus interface. The shorter delays of the TAB-based card allow the chips to communicate faster and thus deliver a slightly higher throughput even though they run at the same clock frequency. The module greatly eases system design since it comes fully tested and burned in before system assembly. In lots of 100 the 40-MHz TAB module sells for $2648.

Cypress Semiconductor Corp., 3901 N. First Street, San Jose, CA 95134-1599; Andy Paul, (408) 943-2600. **CIRCLE 492**

NEW PRODUCTS

ANALOG

TRIPLE VIDEO ADC HAS 30-MHZ SCAN RATE

A scanning rate of 30 MHz makes a video analog-to-digital converter the fastest such device, according to its developer. Intended to handle TV's three color components, the SDA 9205-2 from Siemens AG, Munich, Germany, integrates three 8-bit video A/D converters on a chip. The device permits oversampling. That is, it uses a scan rate of more than twice the signal frequency. External antialiasing filtering can be simplified, thanks to internal digital filtering. The new Siemens converter, developed at the company's facilities in Villach, Austria, features internal clamping and separately selectable scanning data formats, which conform to the CCIR/Rec. 601/656 international standard. To accommodate the three A/D converters on one chip, the SDA 9205-2 uses CMOS technology that permits high speed and a high integration density at low power consumption. With a signal-to-noise ratio of 46 dB, the device is suitable for digital image processing in PCs, TV sets, and video recorders. The chip is supplied in a plastic leaded chip carrier PLCC-68 package. The Siemens SDA 9205-2 sells for about $15 apiece in lots of 10,000. Samples are now available.

Siemens AG, Semiconductor Group, P. O. Box 80 17 09, Balanstr. 73, D-8000 Munich 80, Germany. Contact Maximilian Huber, phone 0049 89 4144 4538. CIRCLE 493

28-PIN PACKAGE HOLDS DUAL PIN DRIVERS

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Brooktree Corp., 9950 Barnes Canyon Rd., San Diego, CA 92123; (619) 452-7580. CIRCLE 494

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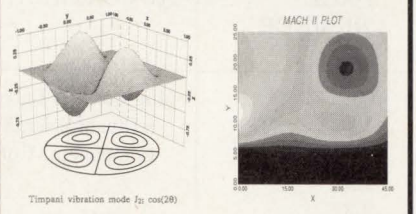

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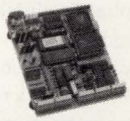

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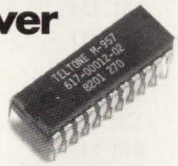

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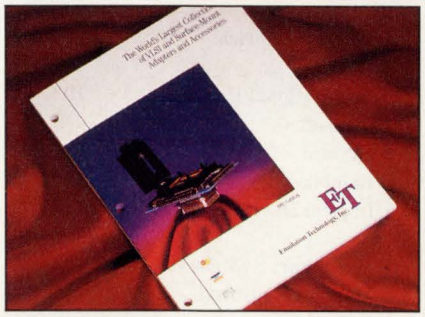

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dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8 □	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.
• 1dB Gain Compression
□ +4dBm 1 to 2 GHz

Unbelievable, until now…tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

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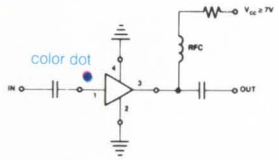

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Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 220, 470, 680, 1000 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047. .068, .1μf

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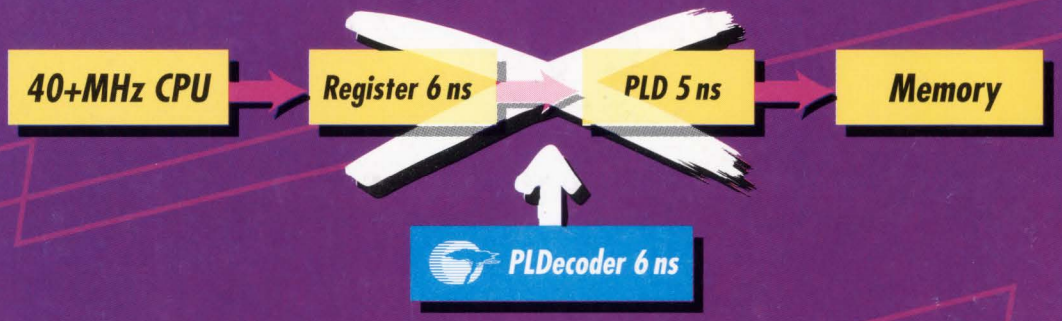

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