

# ELECTRONIC DESIGN

APRIL 2, 1992

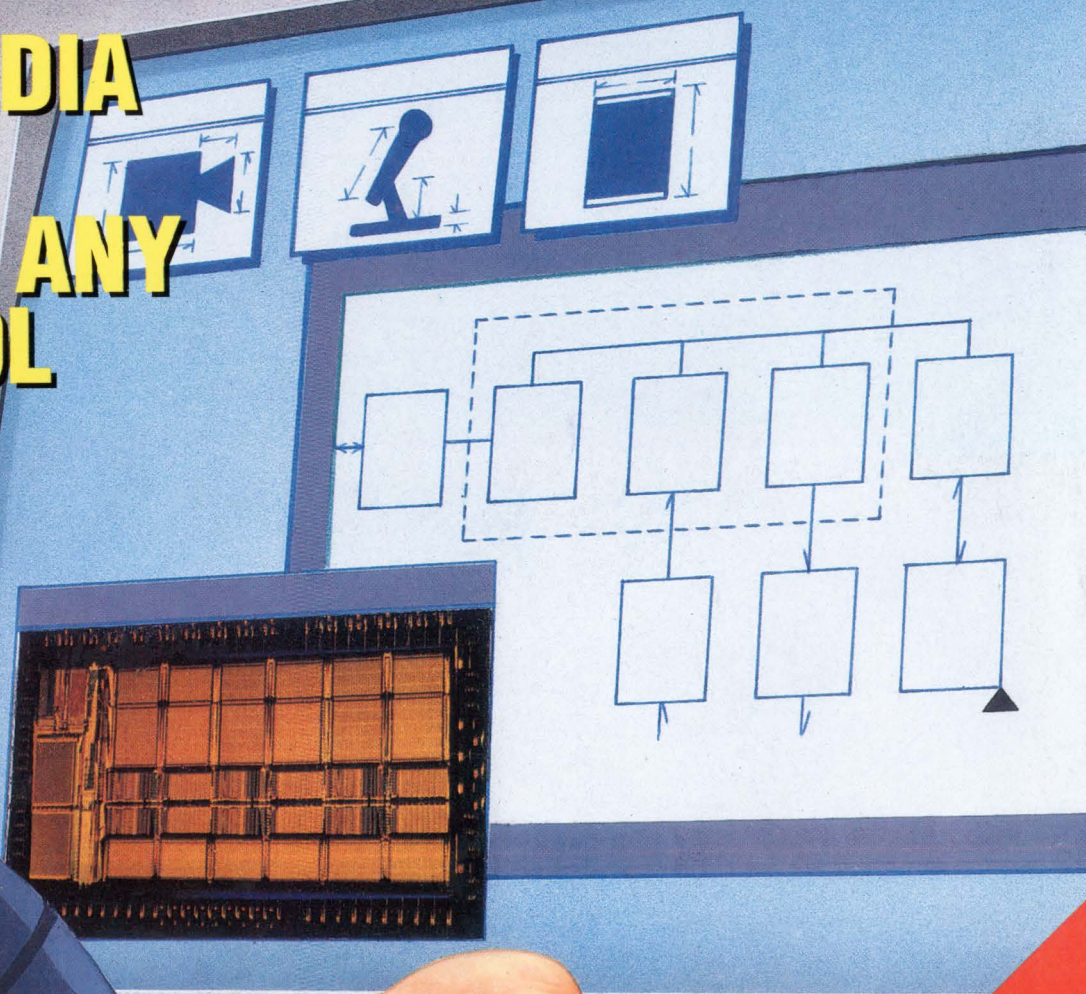
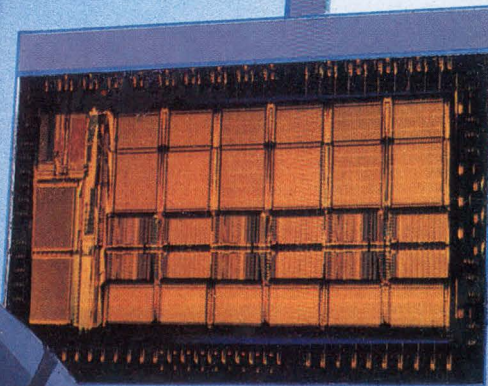
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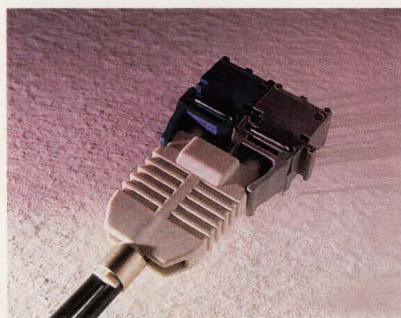
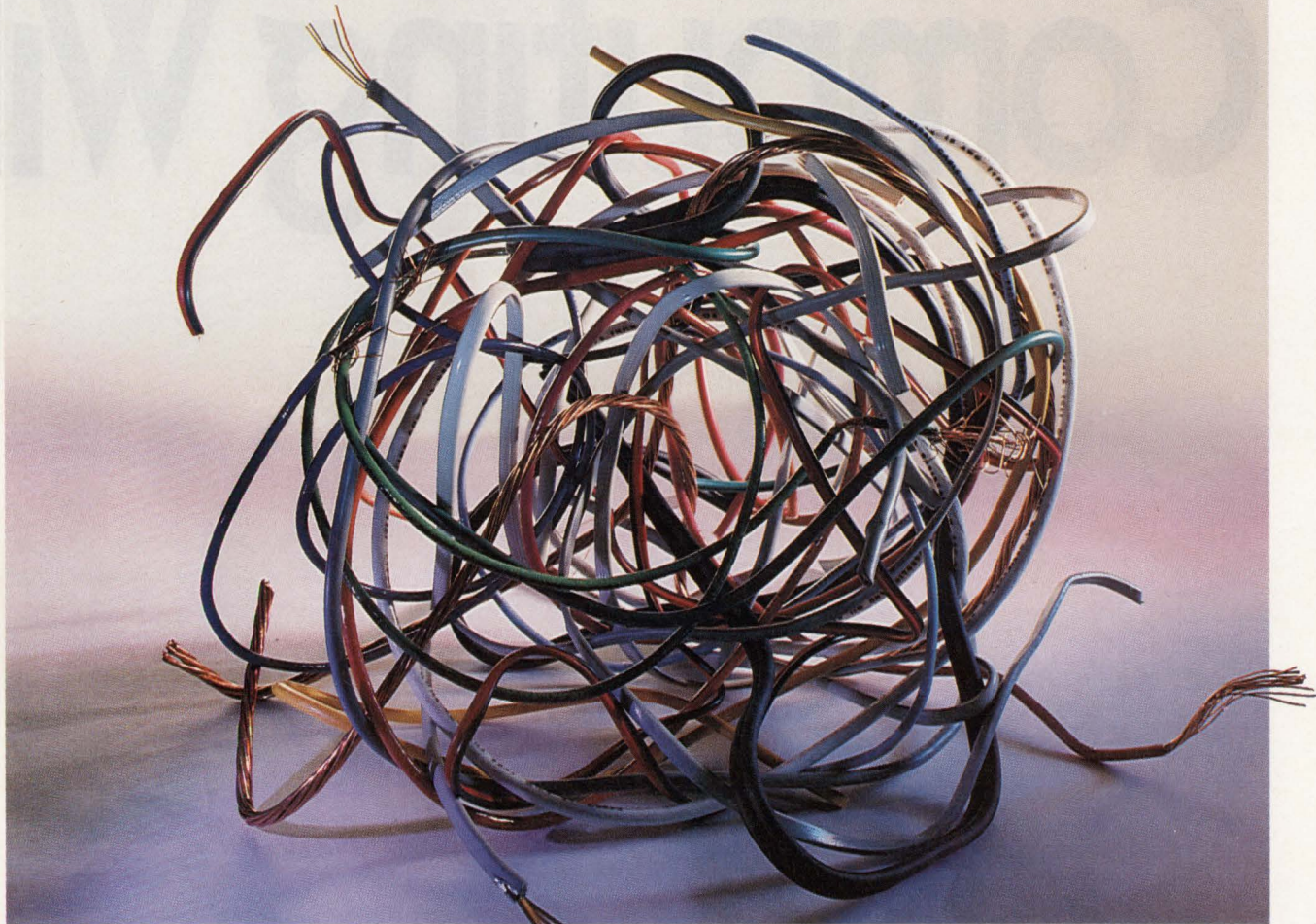


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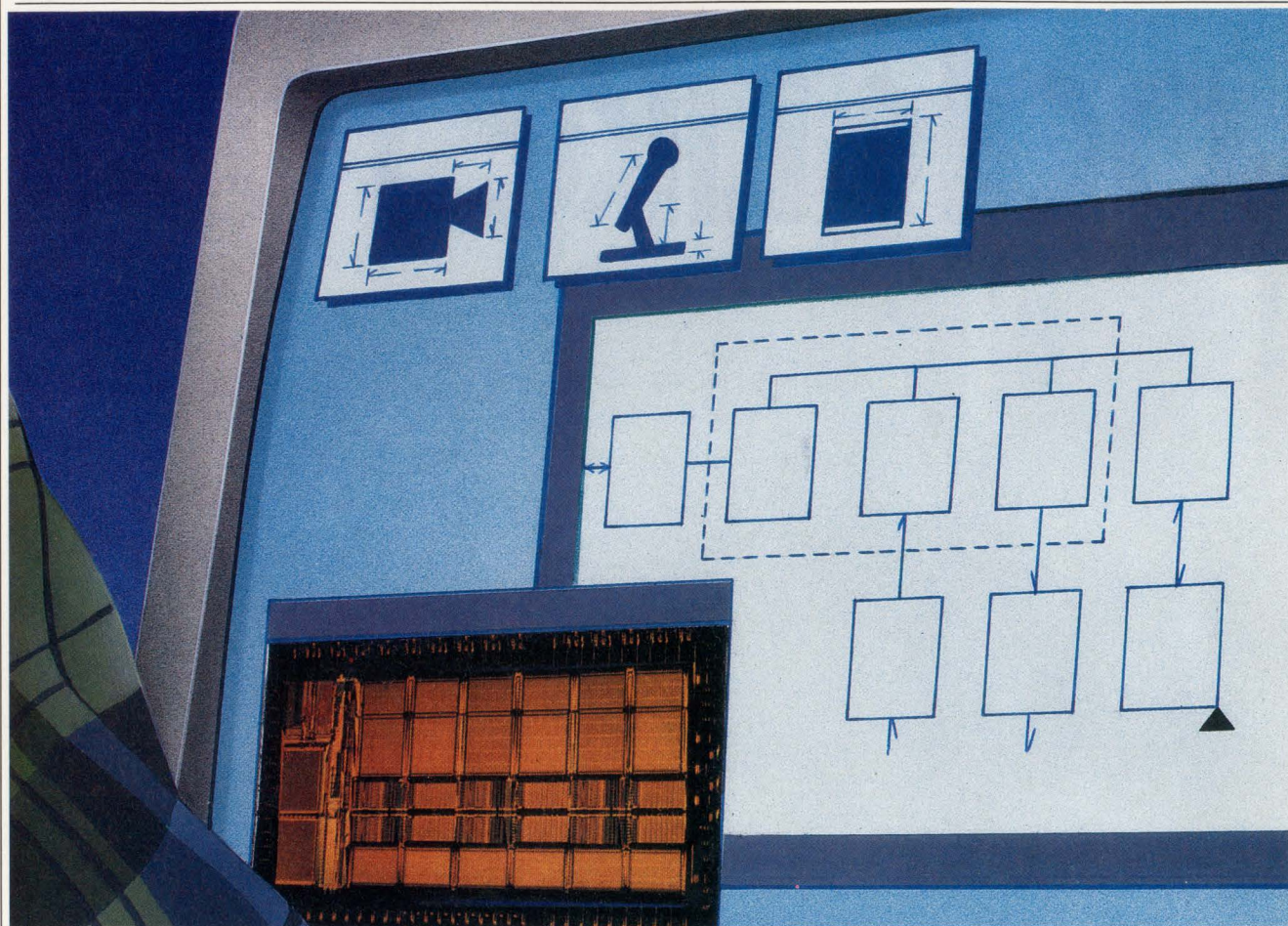


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# ELECTRONIC DESIGN



**COVER FEATURE** **45 SILICON SOLUTION MERGES VIDEO, STILLS, AND VOICE**  
Codec chip set drives standard algorithms for desktop multimedia and video conferencing.

**ELECTRONIC DESIGN REPORT** **57 ENHANCED SRAMS PROPEL SYSTEMS PERFORMANCE**  
The venerable static RAM evolves as users demand versions tuned for narrow market segments.

**DESIGN APPLICATIONS** **73 IMPROVE NOISE ANALYSIS WITH OP-AMP MACROMODEL**  
By enhancing the macromodel for op-amp Spice simulations, a more realistic analysis of noise sources can be done.

**PRODUCT INNOVATIONS** **99 ON-CHIP 8-BIT DACS SET COMPARATOR THRESHOLDS**  
On-chip 8-bit DACs set and vary threshold voltages of a quad, 1.5- $\mu$ s comparator, and 4- and 10-ns single ECL and TTL comparators.

**104 LOGIC EMULATION PROMOTES PARALLEL DESIGN METHODS**  
A specialized software algorithm maps designs to FPGAs for verification of circuits before they're built.

**106 PROCESS ANALOG AND DIGITAL SIGNALS ON A PC**  
PC/AT boards supply synchronized analog and digital stimuli while measuring analog and digital response of device under test.



**14 EDITORIAL**

**18 TECHNOLOGY BRIEFING**

TAB positions itself for growth

**23 TECHNOLOGY NEWSLETTER**

- High-speed 3.3-V logic operates down to 1.2 V
- 64-bit RISC CPU IC to spearhead workstations
- Holland hosts analog-circuit workshop
- PC buyers get lifetime warranties, discounts
- Mixed-signal arrays hold 12-GHz npns
- Gyroscope-based PC pointer goes wireless
- RAMBUS-DRAM socket looms on the horizon
- Transceiver targets wireless networks

**33 TECHNOLOGY ADVANCES**

- SAW, ACT technologies combine to produce 50 billion multiply-accumulate/second ICs
- MCM conference stresses system-level design

**83 IDEAS FOR DESIGN**

- Get three colors from a bicolor LED
- Precisely check low resistances
- Transfer data from a DMM to a PC

**89 QUICK LOOK**

- First annual concurrent engineering award at Test & Design Expo
- First-of-a-kind products: Will AT&T's picture phone hit a grand slam?
- Engineering investors and mutual funds
- Which technical books are the most popular in Silicon Valley?

**95 PEASE PORRIDGE**

What's all this calculator stuff, anyhow?

**NEW PRODUCTS**

- 114 Digital ICs**  
Highly integrated cache-tag RAMs perform matches in 12 ns
- 119 Analog**
- 121 Instruments**
- 123 Packaging & Production**
- 124 Communications**  
Development kit simplifies multimedia design effort
- 126 Power**
- 128 Computer-Aided Engineering**  
Analog behavioral modeling, VHDL support embellish broad EDA software line

**135 INDEX OF ADVERTISERS**

**137 READER SERVICE CARD**

**COMING NEXT ISSUE**

- Special Report: Digital audio's impact on high-resolution DACs
- How to extend voltage-reference options with op amps
- First details on a switching-regulator IC for laptop PCs
- Special Section: Designing PC systems
- Evaluating the communications performance of next-generation boards
- Implementing new graphics standards for local buses
- Review of new products for personal computers
- A new family of high-performance CMOS op amps
- PLUS:  
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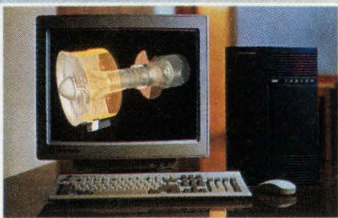
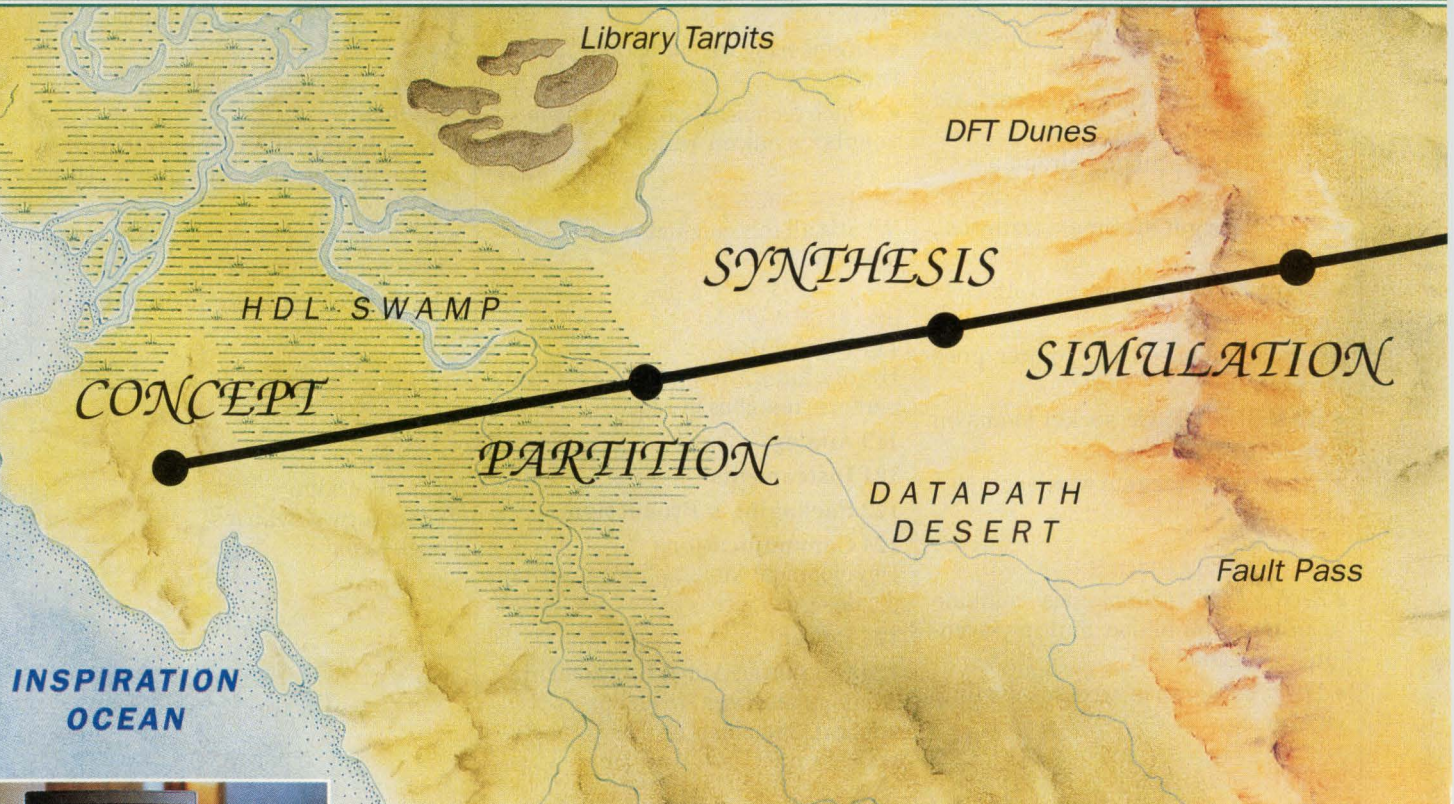
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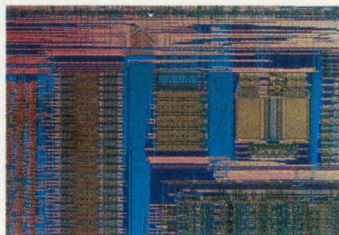
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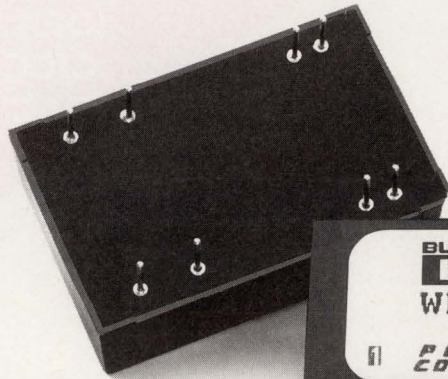
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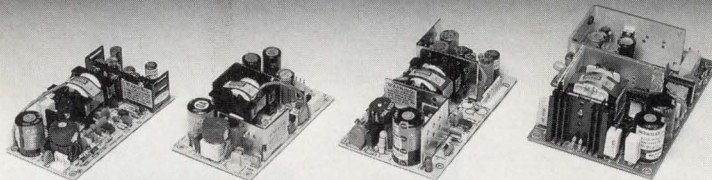
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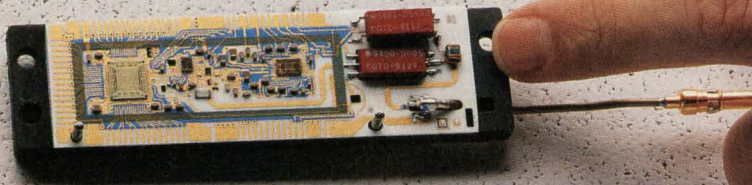
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CIRCLE 150 FOR U.S. RESPONSE

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## EDITORIAL

### BLAME IT ON...THE MOON?

**H**as anyone ever considered the possibility that holes in the ozone layer are exposing us not only to more intense ultraviolet radiation from the sun, but also to more intense illumination from the full moon? How else can anyone explain the recent rash of lunacies that we see all around us?

Case in point no. 1: The average salary of major-league baseball players now is about one million dollars per year. However, ballplayers aren't alone in that income bracket. They're in a class with many executives of in-the-red corporations, whose boards of directors seem to be much less demanding of performance excellence than baseball managers. For one group, only teammates and fans get hurt when the manager makes a bad decision, while the other has thousands of other people's jobs riding on his or her decisions.

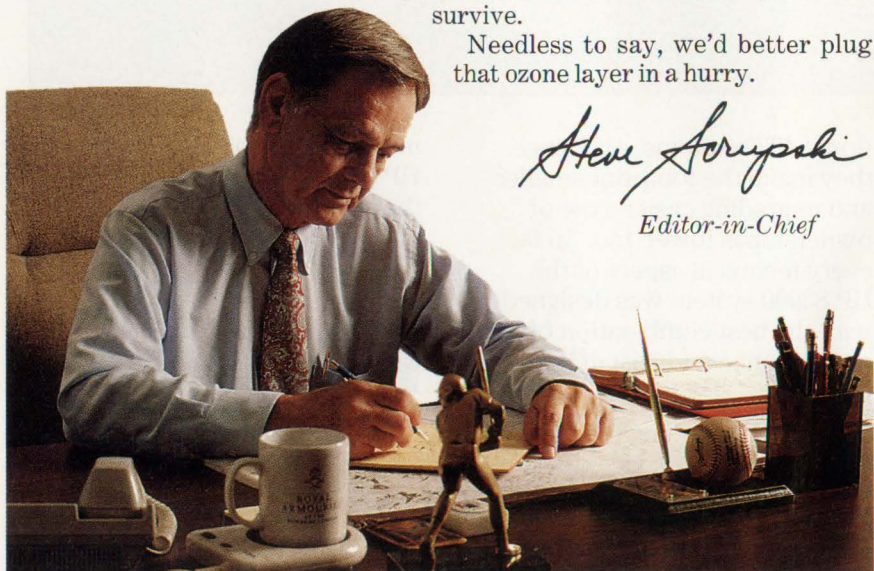
Case in point no. 2: In a New York Times article about the shrinking number of jobs for physicists in the U.S., IEEE president-elect Merrill W. Buckley draws fire for his remarks on the immigration of foreign engineers in times of high unemployment. This view is disputed by a professor of physics who says, "Without the foreign physicists who came to the United States during this century, American science would have been in a sorry state." That may have been true earlier in this century. But today, the knowledge and talent of many trained American engineers and physicists are wasted in menial technical jobs, if they have jobs at all. Companies, for whatever reason, no longer invest in research and development as they once did, surrendering the future for short-term budget gains today. And still, universities beat the drums for more students, with claims of a looming shortage of engineers and scientists.

Case in point no. 3: The House of Representatives turns out to be a club for rubber-check writers. According to our Constitution, the House is the source of any bill that raises revenue, and now it becomes clear why the federal government always operates under a deficit. And these people are the same ones who waited until the middle of the night, when bill-paying, hard-working citizens (those who still had their jobs) were sleeping, to vote themselves a raise. Once again, Walt Kelly's Pogo is proven right: "We have met the enemy and he is us."

Case in point no. 4: Politicians continue to jump aboard the trade protectionist bandwagon, instead of coming up with programs that would help U.S. manufacturers compete in today's and tomorrow's global marketplace. That's the best way to assure that voters will have jobs in the future. International competition is going to intensify in the coming years, and only the quality producers — and their workers' jobs — will survive.

Needless to say, we'd better plug that ozone layer in a hurry.

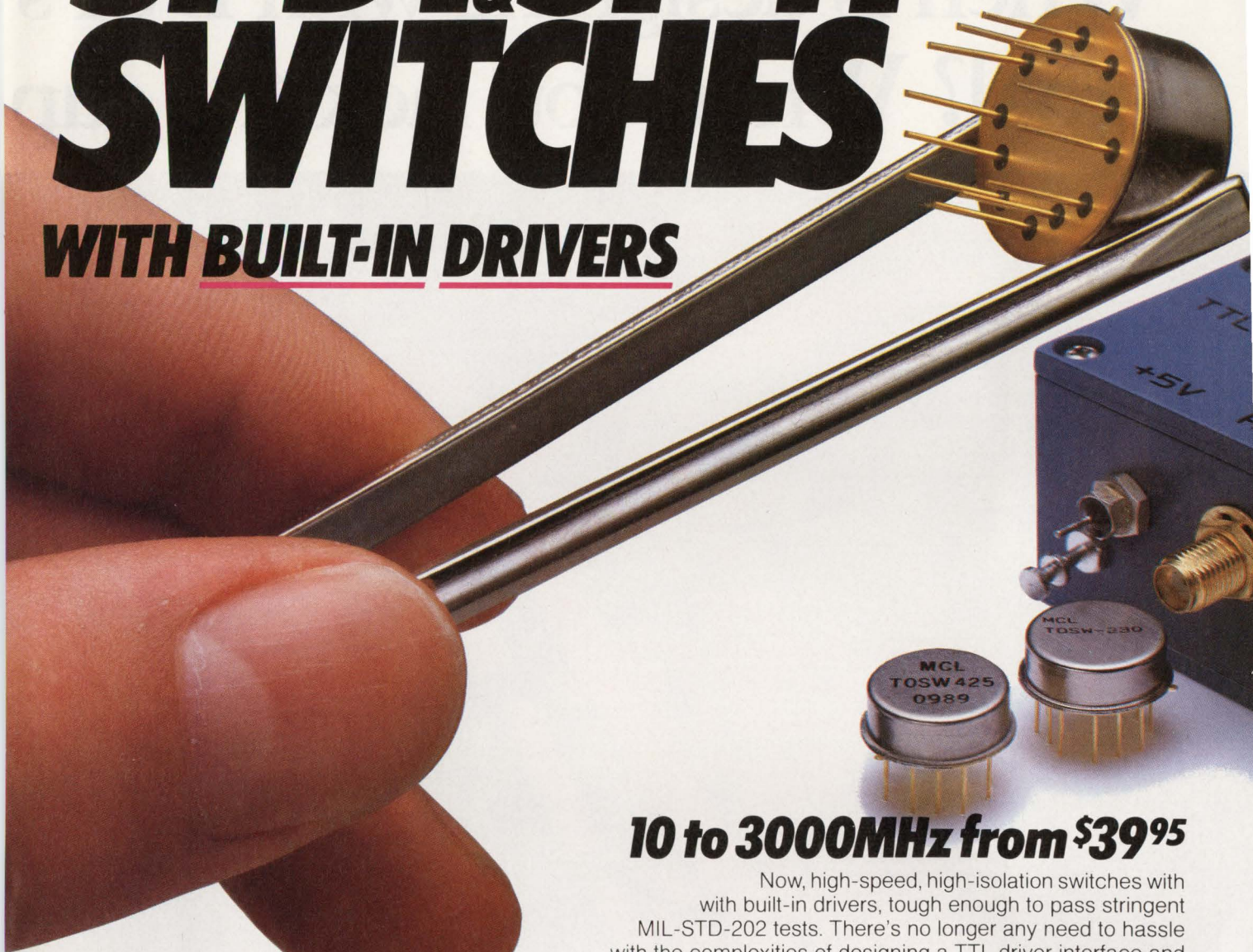
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100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ.	max.	typ.	max.
	1.3	1.6	1.3	1.6
Switching Time (μsec) (from 50% TTL to 90% RF)	typ.	max.	typ.	max.
	2.0	4.0	2.0	4.0
Oper. Temp.(°C)	-55 to +100		-55 to +100	
Stor. Temp.(°C)	-55 to +100		-55 to +100	
Price (10-24)	\$39.95		\$59.95	
(1-9)	\$89.95		\$109.95	

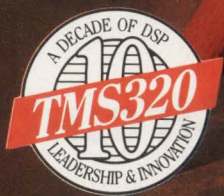
CIRCLE 122 FOR U.S. RESPONSE

CIRCLE 123 FOR RESPONSE OUTSIDE THE U.S.

F126 REV. A



When is designing with DSPs  
stool? When you lack the sup



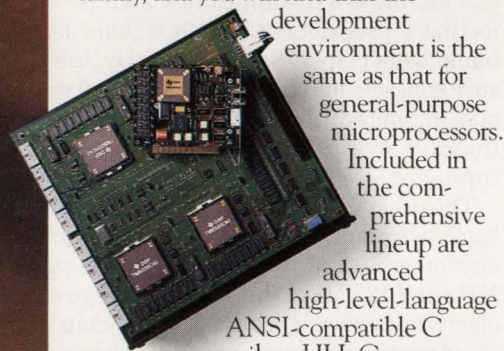


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development environment is the same as that for general-purpose microprocessors. Included in the comprehensive lineup are advanced high-level-language ANSI-compatible C compilers, HLL C-source-

## Tap into plenty of help

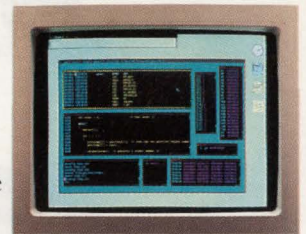
Our technical hot line connects you with TMS320 specialists who can answer your questions, provide more information or discuss a fine design point. We also maintain an on-line bulletin-board service.

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includes more than 100 university labs.

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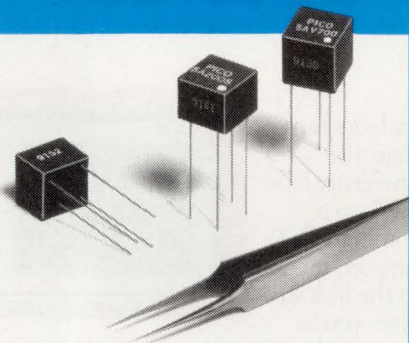
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## TECHNOLOGY BRIEFING

### TAB POSITIONS ITSELF FOR GROWTH

**T**ape-automated bonding (TAB) is making inroads as an enabling technology for future generations of multichip modules (ELECTRONIC DESIGN, Jan. 9, p. 83). But despite its wide acceptance in Japan and growth in the U.S. and Europe, the technology does have its critics. At the recent Fourth International TAB Symposium, San Jose, Calif., a new direction was described for TAB that sidesteps many of its pitfalls and may offer an avenue for substantial growth as a mainstream packaging technology.



DAVID MALINIAK  
COMPONENTS & PACKAGING

In developing a technique called demountable TAB (DTAB), researchers at Hewlett-Packard's Circuit Technology R&D Center, Palo Alto, Calif., sought to overcome the limitations that TAB's critics have decreed for years. These include the technology's high entry cost, the expense of applying gold bumps to chips, and the need for ever-finer pitches for pc-board traces. The loudest complaints concern the difficulties TAB poses for rework and repair. But by perfecting a proprietary bumpless inner-lead-bond process, HP eliminated the bumping of chips. More importantly, the package's separable outer-lead pressure contacts make for easy removal from the board after mounting. This creates unlimited rework, not to mention ease of diagnostics and field service at the chip level. The 284-lead package uses area-array connection directly to through-hole vias on the pc board, eliminating the need for fine-pitch traces.

The package plugs into precise alignment holes in the pc board. The board is backed by a spring stiffener and the package is secured by screws. Compressed elastomer is used to apply force to the outer leads. In performance tests at 65 MHz and 125 MHz, the DTAB package equalled or exceeded the thermal and electrical performance of any single-chip VLSI package. The package also withstood aggressive environmental testing. As a result, HP envisions DTAB as potentially spurring the proliferation of high-performance TAB technology.

Researchers are also investigating other ways of getting around gold bumping of die for TAB attachment. A report from IBM Corp.'s Endicott, N.Y. facility describes a process called solder-attach tape technology, in which the inner leads aren't bonded by thermocompressing gold bumps on the chip. Instead, the heat necessary to form the bond is transferred to a tin-lead solder bump on the chip and gold-plated TAB leads by convection from hot gas applied through a nozzle over the bond site. The leads are pressed into the preheated solder by the nozzle, which applies the hot gas. A cool-gas cycle then solidifies the joint.

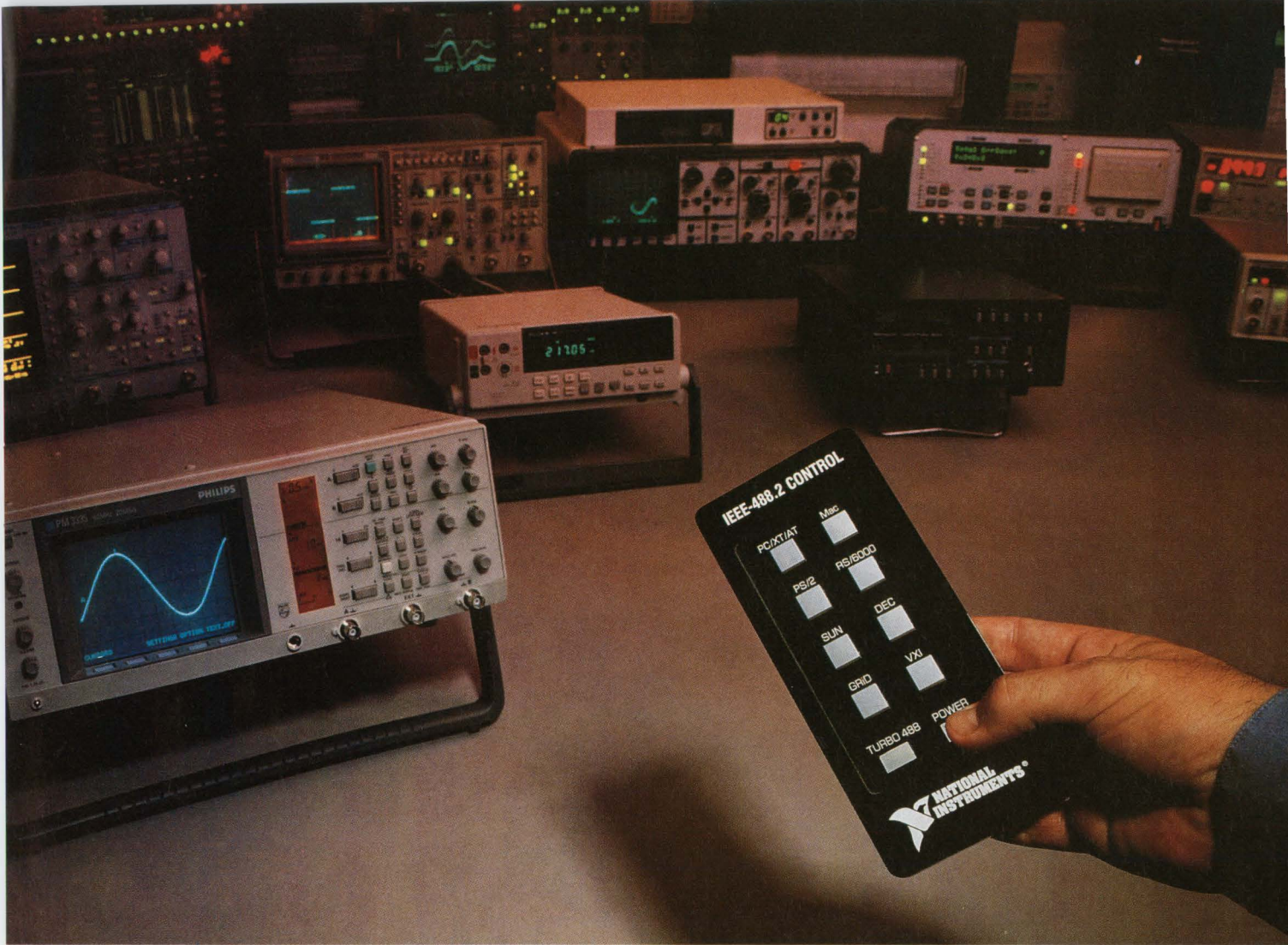
The advantages of this technique, which borrows from IBM's established flip-chip methodology, is that bonds can be formed over active circuitry. This means that array footprints can be packaged. Earlier TAB methodologies were limited to perimeter connections. The shorter line lengths will reduce capacitive loading and other parasitic effects. Hence, devices will be faster.

Some MCM developers have discovered that module testing requires a multi-phased approach to hardware test, and that TAB technology provides for easier assembly than wire bonding. In addition, it's easier to sort for good die when they're mounted in TAB carriers. The experiences reported by the Tactical Systems Division of Rockwell International Corp., Anaheim, Calif., show that MCM developers have a better handle on the complexity of module assembly and verification than ever before.

Rockwell's approach to designing its dual-1750A processor module for a high-speed missile-interceptor program may well point the way for future MCM developers. The company attributes its first-pass success to months of up-front work at the system level, which included an effort to reduce design complexity.

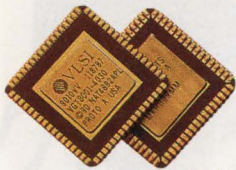
Thus, as TAB developers and end-users explore ways to expand the technology's applicability, TAB inches closer and closer to the mainstream of packaging technology.





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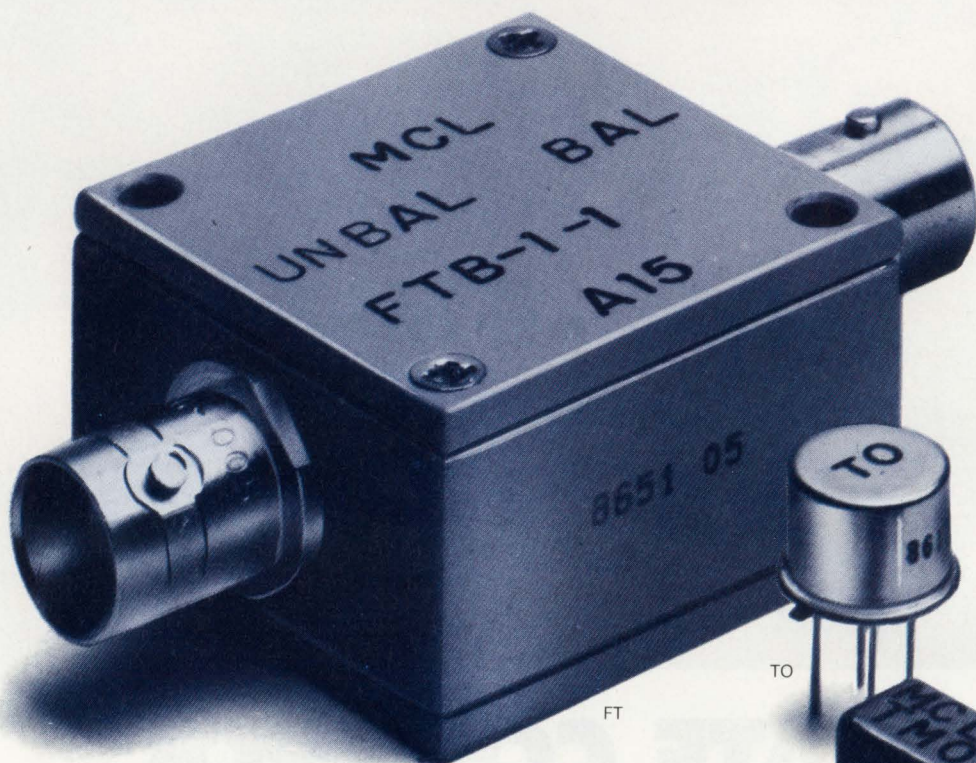
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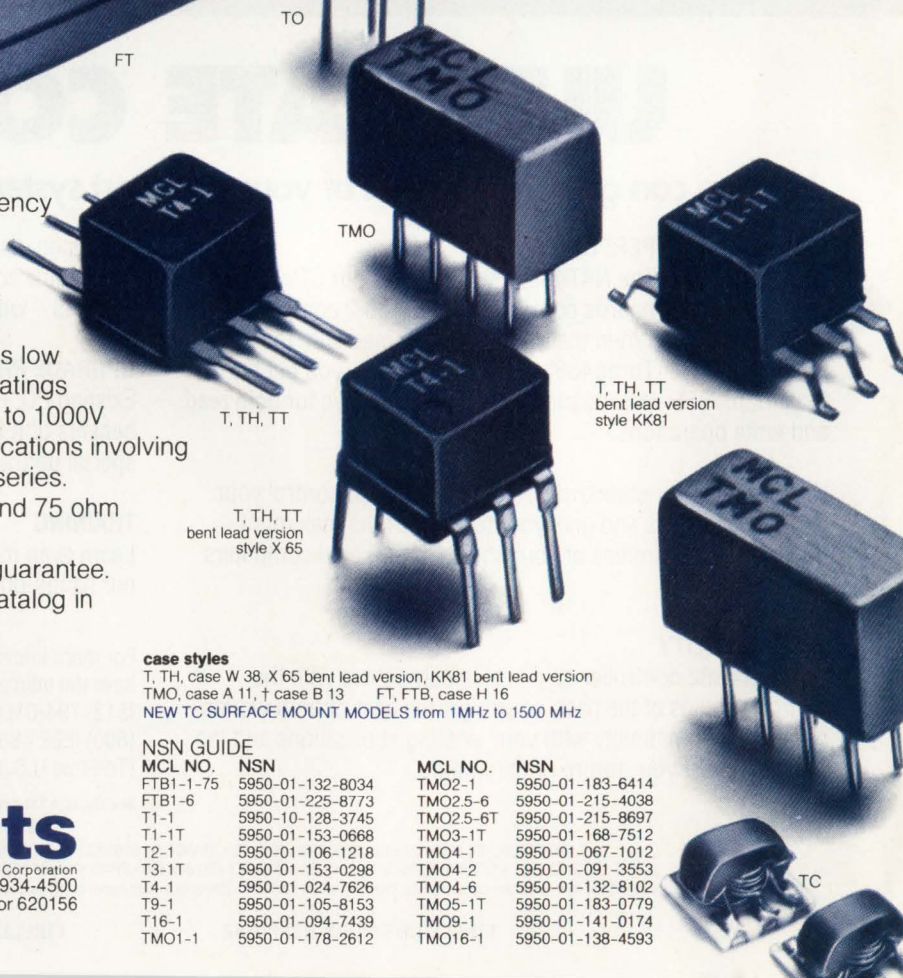


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#### case styles

T, TH, case W 38, X 65 bent lead version, KK81 bent lead version  
 TMO, case A 11, † case B 13 FT, FTB, case H 16  
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#### NSN GUIDE

MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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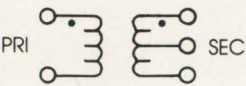
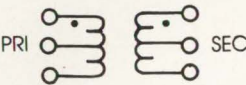
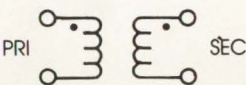
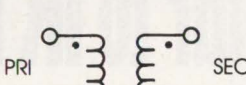
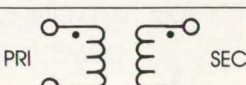
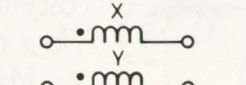
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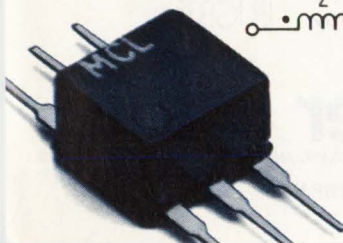
case style number see opposite page	MODEL NO.	$\Omega$ RATIO	FREQUENCY MHz	INSERTION LOSS			PRICE \$ Qty. (1-9)		
				3dB MHz	2dB MHz	1dB MHz			
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	2-80	4.45	
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95	
		T2-1T	2	.07-200	.07-200	.1-100	5-50	4.95	
		T2.5-6T	2.5	.01-100	.01-100	.02-50	50-20	4.95	
		T3-1T	3	.05-250	.05-200	.1-200	5-70	4.95	
		T4-1	4	2-350	2-350	.35-300	2-100	3.25	
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45	
		T5-1T	5	3-300	3-300	6-200	5-100	4.95	
		T8-1T	8	.03-140	.03-140	10-90	1-60	7.95	
		T13-1T	13	3-120	3-120	7-80	5-20	4.95	
		T16-6T	16	.03-75	.03-75	.06-30	1-20	5.65	
		TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
		TMO	TMO1-1T	1	.05-200	.05-200	.08-150	2-80	7.95
			TMO2-1T	2	.07-200	.07-200	.1-100	5-50	8.45
			†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
			†TMO3-1T	3	.05-250	.05-250	.1-200	5-70	7.95
		TMO4-1	4	2-350	2-350	.35-300	2-100	6.25	
		TMO5-1T	5	3-300	3-300	6-200	5-100	8.45	
		TMO13-1T	13	3-120	3-120	7-80	5-20	8.45	
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	1-50	6.95	
		TT1.5-1	1.5	.075-500	.075-500	2-100	1-50	5.95	
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45	
		TT4-1	3	.05-200	2-50	2-50	1-30	5.95	
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95	
		TT25-1	25	.02-30	.02-30	.05-20	1-10	9.95	
		TTMO25-1	25	.02-30	.02-30	.05-20	1-10	11.95	
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45	
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95	
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25	
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65	
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65	
		T1.5-1	1.5	.1-300	.1-300	2-150	5-80	4.45	
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65	
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45	
		T4-6	4	.02-200	.02-200	.05-150	1-100	4.45	
		T9-1	9	.15-200	.15-200	3-150	2-40	3.95	
		T16-1	16	3-120	3-120	7-80	5-20	4.45	
		T36-1	36	.03-20	.03-20	.05-10	1-5	6.95	
		TO	TO-75	1	10-500	—	10-500	40-250	6.95
		TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
			T9-1H	9	2-90	2-90	3-75	6-50	6.45
			T16-H	16	7-85	7-85	10-65	15-40	6.45
		TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
			TMO1-1	1	15-400	15-400	35-200	2-50	6.25
			TMO1.5-1	1.5	.1-300	.1-300	2-150	5-8	8.45
			†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	1-100	7.95	
		TMO6-1	6	3-200	3-200	5-150	5-50	7.95	
		TMO9-1	9	15-200	15-200	3-150	2-40	7.95	
		TMO16-1	16	3-120	3-120	7-80	5-20	7.95	
D 	T	T2-1	2	.050-600	.050-600	.1-400	5-200	3.95	
		T3-1	3	5-800	5-800	2-400	—	4.45	
		T4-2	4	2-600	2-600	5-500	2-250	3.95	
		T8-1	8	.15-250	.15-250	25-200	2-100	3.95	
		T14-1	14	2-150	2-150	5-100	2-50	4.95	
		TMO	TMO2-1	2	.050-600	.050-600	1-400	5-200	7.95
			TMO3-1	3	5-800	5-800	2-400	—	8.45
			TMO4-2	4	2-600	2-600	5-500	2-250	7.95
			TMO8-1	8	.15-250	.15-250	25-200	2-100	7.95
			TMO14-1	14	2-150	2-150	5-100	2-50	8.45
		FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95	
E 	FTB	FTB-1	1	2-500	2-500	5-300	1-100	36.95	
		FTB1-6	1	.01-125	.01-125	.05-50	1-25	36.95	
		■FTB-1-75	1	5-500	5-500	5-300	10-100	36.95	
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25	
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95	

■ Denotes 75 ohm models

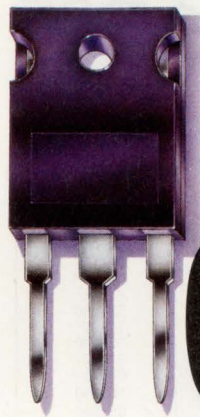
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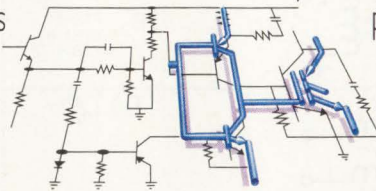
Size. Its smaller footprint and lower component count saves a lot of board space.

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## HIGH-SPEED 3.3-V LOGIC OPERATES DOWN TO 1.2 V

Useful battery life in portable electronic equipment such as notebook computers and cordless telephones can be extended with two families of low-voltage logic recently introduced by Philips Semiconductors, Eindhoven, the Netherlands. Both families are intended for use as glue logic with 3-V versions of 16- and 32-bit processors and high-capacity memories. Dubbed HLL for high-speed low power, and LV for low voltage, they operate with supply rails as low as 1.2 V. That means they can work in circuits powered by one rechargeable cell or by two alkaline or carbon-zinc primary batteries. The output of a typical NiCd cell drops to 1.2 V when it needs recharging, while primary cells have an end-of-life output of around 1.8 V. Power consumption for the two families is said to be one-half that of standard CMOS logic and input capacitance is 3.5 pF. HLL devices provide propagation delays of 2.5 ns in 3.3-V systems, while LV devices offer a delay of 8 ns. Each group has latch-up-free operation and can connect directly with most bipolar TTL devices. Both families will soon be produced commercially at a newly completed wafer-fabrication plant at Nijmegen, Holland. Philips expects to announce 20 devices in each family this year, with samples of the first circuits, the 74HLL33240 and 74LV244 3-state octal buffer-line drivers, available now. The drivers are available in plastic SO 24- and 20-pin packages, respectively. Versions in SSOP packages are planned for the end of this year. In Europe telephone Tinus V.D. Wouw at 031 80 532662. In the U.S. contact Albert Beijer at (408) 991-3626. *PF*

## 64-BIT RISC CPU IC TO SPEARHEAD WORKSTATIONS

As the gap between PCs and workstations closes, the ante for next-generation desktop systems has been upped for PC suppliers with the release of the 64-bit Alpha RISC microprocessor by Digital Equipment Corp., Maynard, Mass. DEC plans to use the 21064 in both its own VAX computer systems and the standard ACE-compatible computer systems, as well as sell the CPU chip and license its manufacturing rights to semiconductor suppliers. That last ploy is comparable to the approach Mips Computer Systems Inc. uses for its RISC CPU families (Mips Computer Systems has just agreed to merge with Silicon Graphics, creating one of the largest suppliers of RISC-based systems hardware). The Alpha CPU, which offers about the same peak performance as that of the original Cray-1 supercomputer, has a feature set similar to that of the Mips R4000 processor—a full 64-bit RISC CPU and floating-point unit, dual 8-kbyte caches (twice that of the R4000), demand-paged memory management, parity and error-checking and correction, and a four-word write buffer. Operating with 200-MHz clocks and 3.3-V supplies, the Alpha delivers a throughput of about 400 MIPS. The chip will be housed in a 431-lead pin-grid array, dissipating about 23 W when running at 150 MHz (300-MHz external differential clocks). The first commercial version runs at 150 MHz (300 MIPS) and sells for \$1650 each in lots of less than 1000 units. Quantity shipments will start in July. Contact Richard Wittick, (508) 493-5111. *DB*

## HOLLAND HOSTS ANALOG-CIRCUIT WORKSHOP

The Delft University of Technology in the Netherlands will host an International Workshop entitled Advances in Analog Circuit Design. Conceived by Prof. Johan Huijsing of Delft Univ., it will be held April 8-10 in Scheveningen. The three topics that will be covered, one for each day, are operational amplifiers, analog-to-digital converters, and analog CAE/CAD. Unlike a typical conference, there will be no concurrent sessions. A sampling of invited speakers and their subjects include: Derek Bowers (Analog Devices, Santa Clara, Calif., U.S.), *The Impact of New Architectures on the Ubiquitous Op Amp*; Michael Steyaert (Catholic Univ. of Leuven, Belgium) *Op Amp Design for Maximum Gain-Bandwidth: Bipolar vs. CMOS*; Klaas Bult (Philips Research Labs, Eindhoven, the Netherlands) *Super-Stage CMOS Op Amps*; John Corcoran (Hewlett Packard Labs, Palo Alto, Calif., U.S.) *High-Speed Sampling and A-D Conversion*; Tapani Ritoniemi (Tampere Univ. of Technology, Tampere, Finland), *High-Speed 1-Bit Sigma-Delta Modulators*; Andy Thurston (GEC-Marconi Research Centre, Chelmsford, Essex, U.K.) *Bandpass Sigma-Delta A-D Conversion*; and Marc Degrauwe (Centre Suisse d'Electronique et de Microtechnique, Neuchatel, Switzerland), *Tools for Analog Design Planning*. Telephone Prof. Johan Huijsing at 031 15 785745, or fax: 031 15 785755. *FG*

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PC manufacturers typically offer warranties ranging from 6 to 18 months. Hyundai Electronics America, San Jose, Calif., claims it has enough confidence in its products that it's taking their warranty to the farthest extreme—the company is offering a lifetime warranty on qualifying PC products. Hyundai claims that this is a first in the PC industry. The warranty covers the base system, including the motherboard and other related components such as the video card, floppy disk drives, and the keyboard. In addition, the company says that users purchasing a new system can get popular



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## MIXED-SIGNAL ARRAYS HOLD 12-GHZ NPNS

To build the highest-speed mixed-signal array, Tektronix, Beaverton, Ore., has moved to its latest trench-isolated process, GST-1 (Gigaspeed Silicon Technology). GST-1 allows Tektronix to build npn transistors with an  $f_t$  of 12 GHz at a mere 600  $\mu$ A, while offering twice the packing density of its predecessor, the SHPi (Super-High Pi) process. And that's with a beta of 40 and an Early voltage of 15. This self-aligned, double-polysilicon process uses a deep trench to isolate individual devices from each other in lieu of diffusions. The trenches are oxide-lined and back-filled with polysilicon. Trenching increases the packing density and decreases parasitics. The process uses a thin base and a highly doped emitter, which together can build high-speed transistors with good dc characteristics. At a current of 1 mA, the  $V_{BE}$  mismatch between any two npn transistors (the cause of differential-pair offset voltage) runs under 2.5 mV. The array, called Quick Chip 7, uses a tile architecture. One-third of the chip's center portion is a digital section; the other two-thirds is an analog section. The former section consists of one large tile with over 300 npn transistors for ECL circuits. Four large tiles form the analog section, which contains over 200 npn transistors. For additional information, contact Dave Bernel at (503) 627-2515. *FG*

## GYROSCOPE-BASED PC POINTER GOES WIRELESS

Last year, Gyration Inc., Saratoga, Calif., introduced a gyroscope-based handheld computer pointer with an attached cord, an apparatus very similar to a mouse. A second version, called GyroPoint Remote, now communicates with a PC through RF transmissions. Like the original design, the pointer housing encloses a position-sensing miniature gyroscope. However, instead of sending cursor-control signals to a computer through an umbilical cord, the signals are sent by a transmitter connected to a user-worn belt or clip that connects to the pointer through a 3-ft. spiral cord. The receiver is attached to the computer by a 2-ft. cord that's Apple- (ADB-) or PC/RS232-compatible. GyroPoint Remote communicates with a PC at distances up to 50 ft. The device is compatible with all software programs based on Microsoft Windows and Apple Macintosh. Platforms from Sun Microsystems and Silicon Graphics need additional software drivers to use the pointer. GyroPoint Remote will be available from OEMs and independent resellers in June at a suggested retail price of \$995. For more information, call (408) 255-3016. *ML*

## RAMBUS-DRAM SOCKET LOOMS ON THE HORIZON

A high-performance interconnection for Rambus Inc.'s DRAM architecture is in the works. Augat Inc., Attleboro, Mass., is teaming up with the Mountain View, Calif.-based company to develop a surface-mountable memory-module socket that will address users' needs for a rugged, reliable interconnect. The socket will also represent a Rambus-compatible interface for memory and logic devices from Fujitsu, NEC, and Toshiba, who have declared support for the Rambus architecture with compatible DRAMs, ASICs, and bus-interface support circuits. The socket will facilitate memory-system expansion for hundreds of Rambus DRAMs in a small footprint. The Rambus interface is implemented on ICs that forge a link to the Rambus Channel, a memory-interface bus that delivers 500-Mbyte/s data transfers (*ELECTRONIC DESIGN*, Mar. 19, p. 137). *DM*

## TRANSCIVER TARGETS WIRELESS NETWORKS

Requiring no FCC licensing, the GINA (Global Integrated Network Access) data transceiver developed by GRE America Inc., Belmont, Calif., uses spread-spectrum technology to send and receive data at selectable rates up to 128 kbaud in a half-duplex mode. Operating in the 902- to 928-MHz frequency band, the transceiver is housed in a 1.52-in.-high enclosure that's 4.17-in. wide and 5.0-in. deep. An omnidirectional, 50- $\Omega$  antenna is attached to the housing. GINA connects to any device that has an RS232 serial port, and supplies up to 12 communication channels using four different direct-sequence-modulation codes with a bit-error rate of under 1 ppm. Transmission power of 1 W provides a line-of-sight range of up to 1000 ft. Operating power is 12 V dc. For more information, call (415) 591-1400 or 800-233-5973. *ML*



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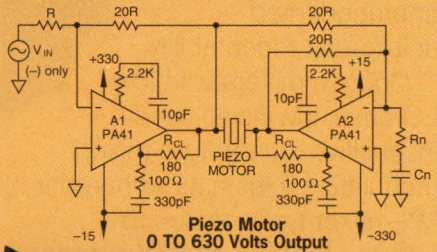
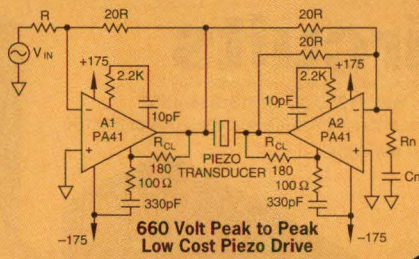
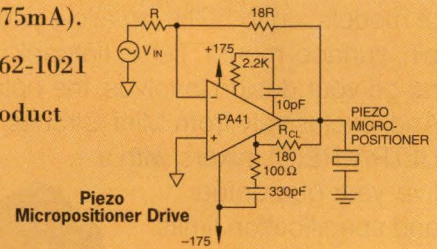
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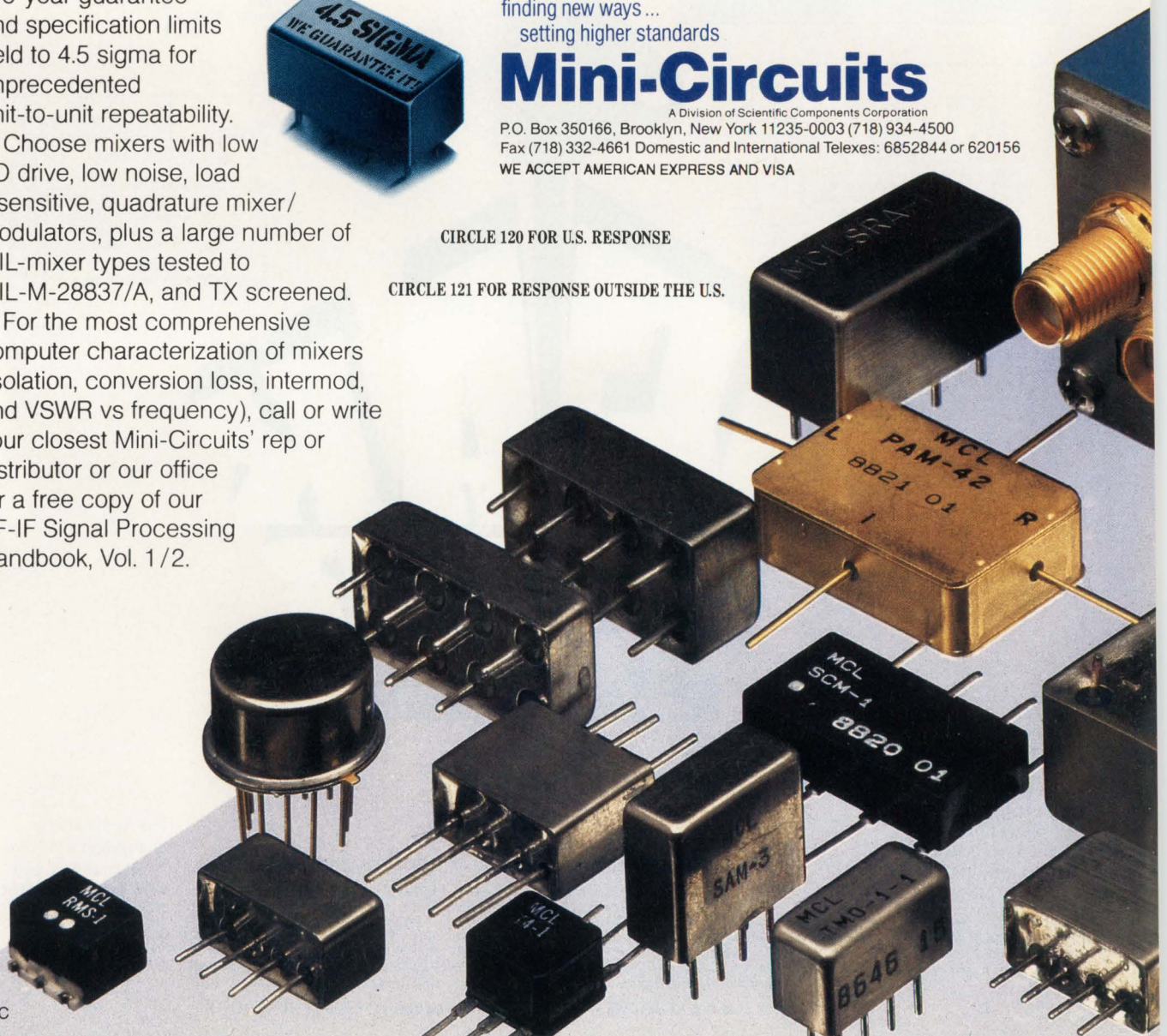
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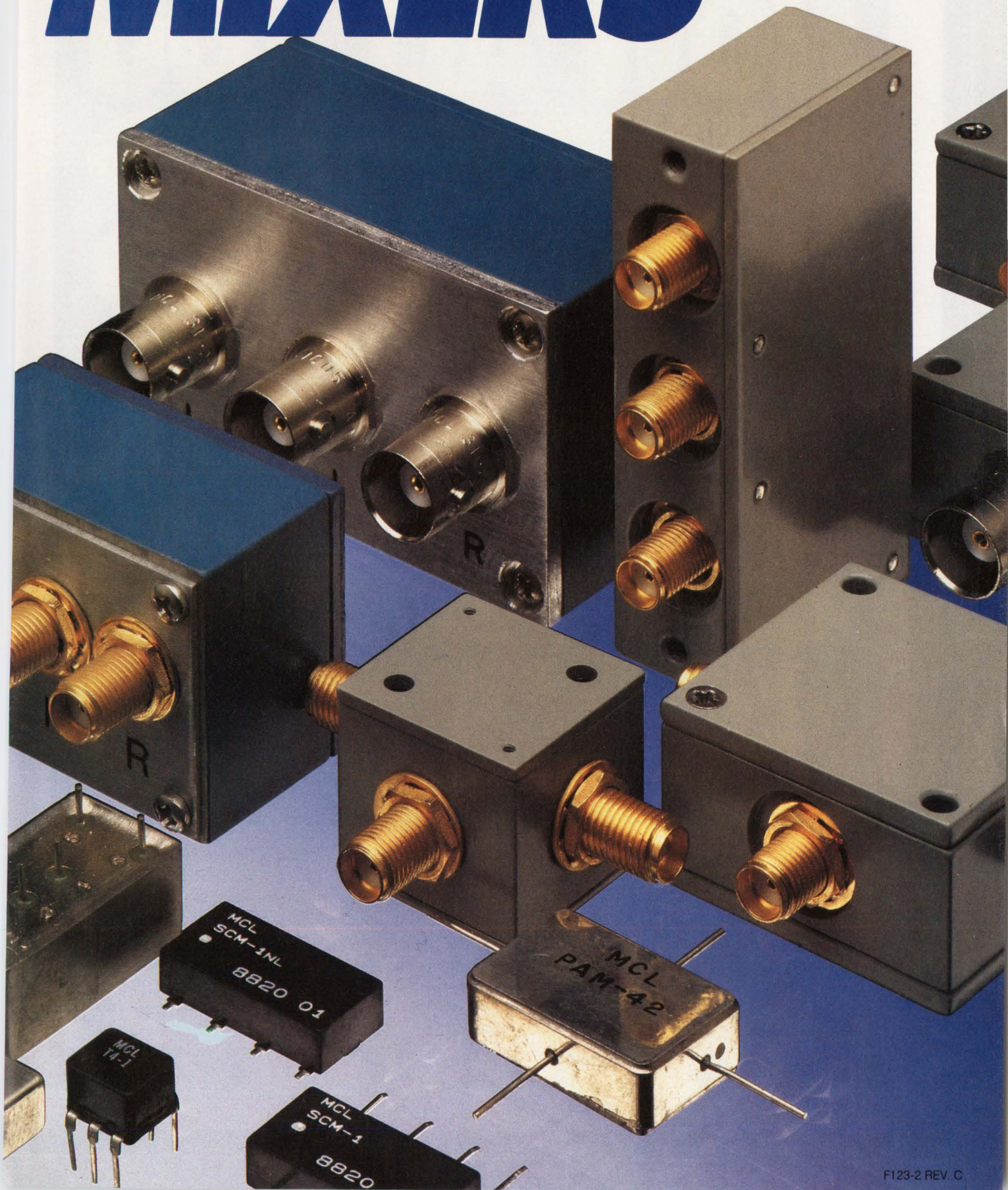
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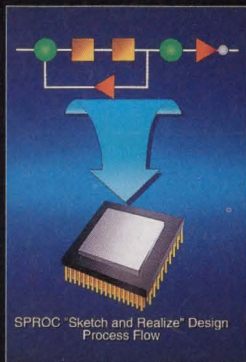
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## SAW, ACT TECHNOLOGIES COMBINE TO PRODUCE 50 BILLION MULTIPLY-ACCUMULATE/SECOND ICs

**S**urface-acoustic-wave (SAW) technology is now coming to the fore to perform analog-signal processing at unheard-of speeds. The SAW principle is being applied to a phenomenon that for years has been under development—acoustic charge transport (ACT) technology. The analog-signal-processing power resulting from this union is best put in digital parlance: SAW/ACT circuits can perform 50 billion multiply-accumulate operations per second (MACs). Such analog-processing power is often the only way to go, particularly for applications where accuracy of less than about 10 bits is sufficient and blazing real-time speed is often vital.

The joining of SAW and ACT technologies stems from a merger between Electronic Decisions Inc., Urbana, Ill., and Comlinear Corp., Fort Collins, Colo. Electronic Decisions, under Bill Hunsinger's direction, has been developing ACT technology for the last ten years, with funding help from the Defense Advanced Research Projects Agency (DARPA). Hunsinger invented the ACT concept at the University of Illinois at Urbana. The Electronic Decisions/Comlinear merger has borne fruit with a single IC that has supercomputing speeds (Fig. 1).

With ACT, designers can build tapped delay lines to create transversal or finite-impulse-response (FIR) filters with signal bandwidths in the 150-to-500-MHz range. FIR filters

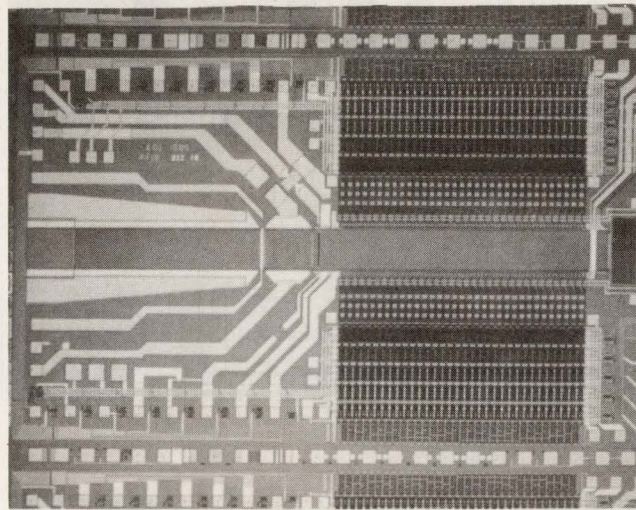


Fig. 1

have long been used to perform correlation functions, although on lower-frequency signals. In fact, digital realizations of FIR filters lie at the heart of many digital-signal-processing algorithms.

Such filters are also found on-chip in delta-sigma analog-to-digital converters. It should be noted that even these ACT-implemented FIR filters are, like switched-capacitor filters, sampled-data systems. However, unlike switched-capacitor filters, they offer virtually unlimited speed. With ACT technology, filter sampling rates are approaching 400 MHz. That puts them on a par with the fastest 6- and 8-bit bit flash ADCs available. Moreover, because ACT filters perform multiplication and accumulation operations simultaneously, no supercomputer is required to finish the job.

ACT devices are built on gallium arsenide, not for GaAs' speed, but for its piezoelectric capability to

create the SAW (Fig. 2a). In fact, rather than being fabricated on a submicron GaAs line, the ACT ICs are made on a modified CMOS process with 8- $\mu$ m lithography. ACT technology essentially represents a marriage of SAW and GaAs IC

technologies.

Consider the simple ACT delay line shown (Fig. 2a, again). An input signal  $x(t)$  is applied to an input ohmic contact (IC) on a depleted n-type epitaxial GaAs layer, which itself is grown on a semi-insulating GaAs substrate. On the same substrate, a high-Q transducer generates a SAW that propagates across the surface at 2846 m/s. Because the material is piezoelectric, the propagating surface wave induces a series of electric fields within the epitaxial layer. These fields can be thought of as traveling potential wells.

Each potential well that passes under the input contact injects a number of electrons, proportional to the input voltage at that instant, into the well. The fields associated with the surface wave then transport these packets of electrons (charge packets) along the ACT "channel" and away from the input

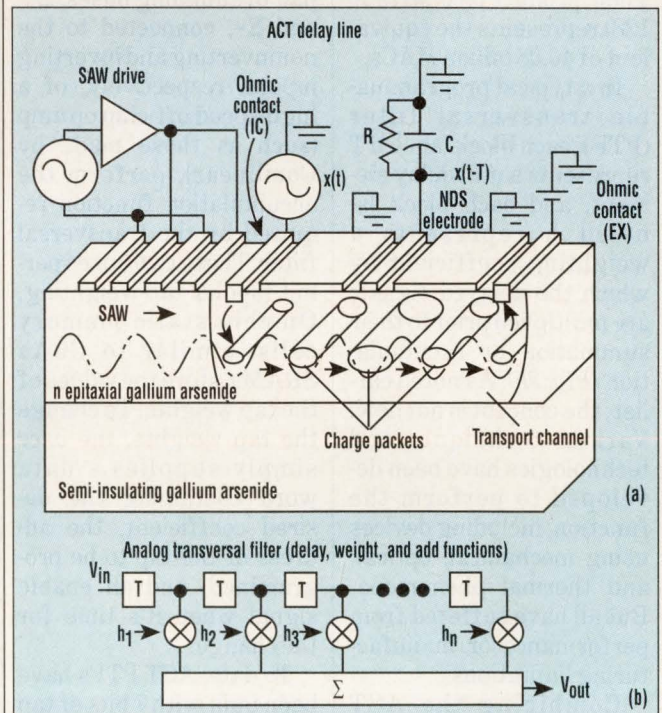


Fig. 2



contact. This process converts the analog input signal into a discrete-time signal (sampled in time, but not quantized in amplitude). During the transport process, the signal can be considered "stored" in the device, thereby achieving the analog memory required for the signal-processing operation.

As the signal is passed down the line, it can be sensed by a series of non-destructive sense (NDS) electrodes, or "taps". They measure, but do not change, the amount of charge in each well. These taps provide the delayed versions of the input signal required to realize the FIR filter. At the end of the ACT channel, another ohmic contact (EX) removes the charge from the wells, and if required, produces a sampled and delayed version of the input signal. Present devices sampling at 360 MHz have been built with 128 taps. Their product (360 MHz  $\times$  128) represents the equivalent of 46.08 billion MACs.

In a typical programmable transversal filter (PTF), each block labeled T represents a unit delay element, and each block labeled h represents a weighting coefficient by which the delayed signals are multiplied prior to their summation or accumulation (Fig. 2b). As noted earlier, the concept is not new. Various techniques and technologies have been developed to perform the function, including devices using mechanical, optical, and thermal phenomena. But all have suffered from performance or manufacturing limitations.

Combining the ACT tapped delay line with on-

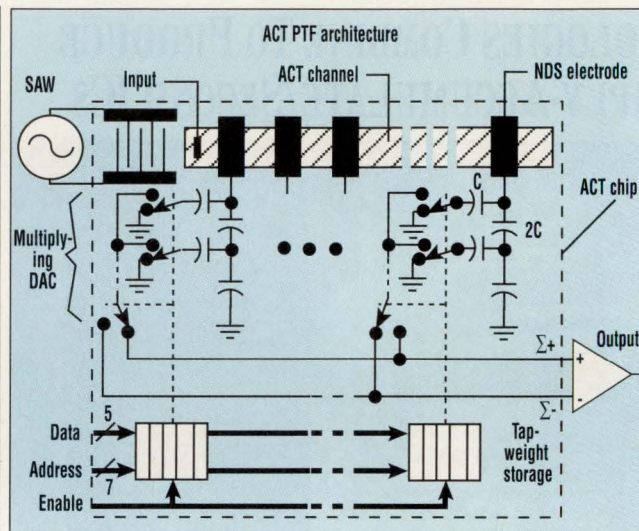


Fig. 3

chip tap-weighting and memory circuits creates a manufacturable (at reasonable cost), high-performance PTF (Fig. 3). The taps are weighted by programmable attenuators formed from capacitive multiplying digital-to-analog converters (MDACs) C and 2C that set the magnitude of each coefficient. A pair of summing buses,  $\Sigma+$  and  $\Sigma-$ , connected to the noninverting and inverting inputs, respectively, of a high-speed off-chip op amp (such as those made by Comlinear), perform the accumulation function required by the transversal filter. These two buses permit bipolar tap-weighting. On-chip static memory cells, similar to GaAs SRAMs, store the values of the tap weights. To change the tap weights, the user simply supplies a data word containing the desired coefficient, the address of the tap to be programmed, and an enable signal when it's time for the change.

To date, ACT PTFs have been built with 7 bits of tap weight and with up to 128

taps. Tap spacings range from 2.8 to 10 ns, and tap-programming rates are 1 to 5 MHz. Future goals for ACT PTFs include 10 bits of tap-weight control, up to 1024 taps, 1-ns tap spacing, sampling rates to 1 GHz, and programming rates to 20 MHz.

Transversal filters provide a correlation function. That is, they examine a received signal and perform signal recognition (detection) by comparing it with a priori examples of the signal. This is often called pattern recognition. The human eye, ear, and brain perform this function continuously and accurately at speeds that bring supercomputers to their knees.

Examples of ACT transversal applications include radar and sonar signature analysis to evaluate a threat or a target. That is, a fighter plane might examine the signature of an impinging radar signal and determine if it's friend or foe, and if the latter, what kind of source (from ground or air, gun or missile) it came from. Needless to say, these applica-

tions can't afford two hours of computer time to get the answer. Alternatively, the aircraft might examine the signature of its own returned signal and determine more accurately the nature of the target.

ACT also has real-world commercial applications. For example, the first ACT product will go into the read channel of high-end (over 1 Gbyte of storage) disk drives. Digital audio broadcasting, or DAB, is another application. Presently, the FCC, the commercial broadcasting industry, automotive companies, and several major semiconductor companies are discussing various schemes to transmit CD-quality audio over existing or new AM and FM radio channels. The most attractive solution would involve a system in which a separate digitally encoded signal is broadcast simultaneously and within the already allocated bands. However, it must not interfere with conventional signals. A receiver based on ACT has been built and its feasibility demonstrated, a feat that until now was proven virtually impossible to achieve.

The ACT technique lets the receiver instantaneously track and cancel standard analog FM or AM signals while allowing an underlying digital signal to pass through. Listeners with conventional radios will receive standard (analog) broadcast channels as those with DAB-capable receivers receive both the standard and the CD-quality signals.

For additional ACT information, call Daniel Fleisch at (217) 367-2600.

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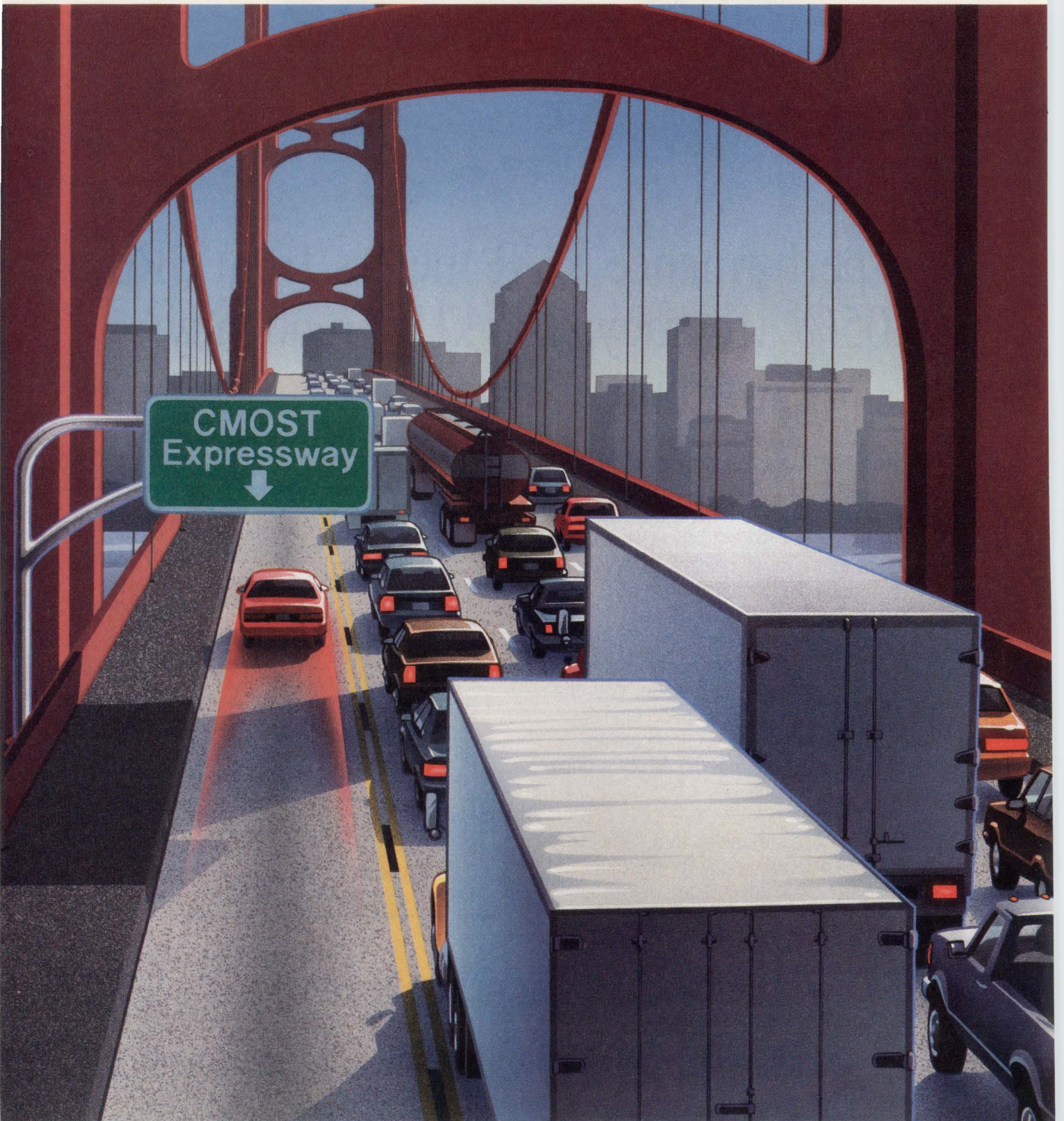
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## MCM CONFERENCE STRESSES SYSTEM-LEVEL DESIGN

**W**ith multichip modules (MCMs) now a vital cog in systems design, packaging has graduated to system-level priority status. To underscore this trend, the First International Conference on Multichip Modules will be held this week in Denver. In addition to spotlighting the newest developments in MCMs, the conference's 70 technical papers provide comprehensive coverage of applications, materials, trade-offs, performance analysis, testing, and reliability. All of the issues covered point toward the industry's heightened per-

ception of packaging as a determining factor in system performance.

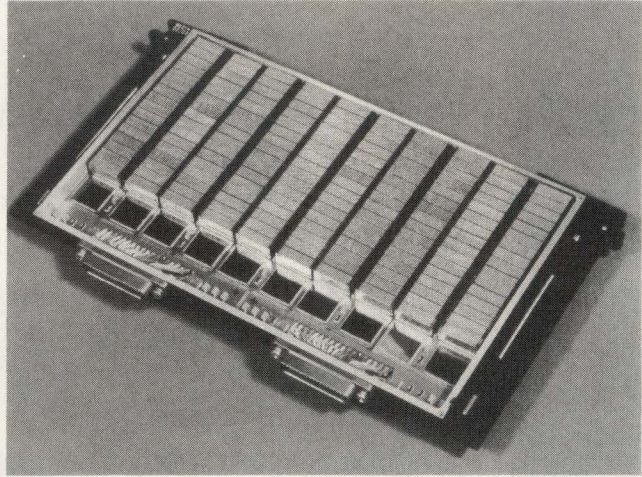
In fact, some of the newest MCM developments reflect a systems-level approach to package design. For instance, in its design of a solid-state recording (SSR) device for the Defense Advanced Research Projects Agency (DARPA), Texas Instruments, Dallas, began with the goal of packaging 4 Gbytes of memory in 100 in.<sup>3</sup> (see the figure). To do so, the company relied on its 3D memory-packaging scheme, which was also developed under a DARPA contract. The SSR is built

with multiple 3D memory cubes packaged on a single silicon substrate. It's intended an alternative to more cumbersome magnetic-tape machines.

The SSR is composed of a memory-interface unit (MIU) and one or more 1.2-

Gbit memory units (GMUs). The current SSR chassis holds up to three GMUs or 3.6 Gbits. Each GMU houses 1.2 Gbits of static RAM in slightly more than 10 in.<sup>3</sup>.

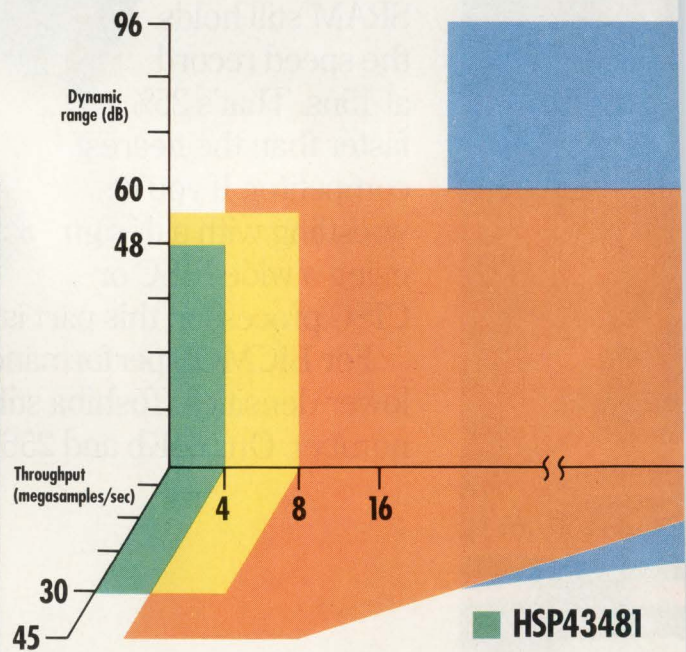
A GMU consists of 1280 1-Mbit SRAMs, 10 flip-



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TAB-bonded CMOS ASICs, four flip-TAB-bonded buffers, and a handful of discrete parts, all placed on a high-density silicon substrate. Of the seven individual substrates that comprise the GMU, five are identical memory-bank substrates. Each holds 32 3D stacks, 2 flip-TAB-bonded ASICs for memory interface and control, and 16 discrete components. The memory-bank substrate has 9568 top metal pads over a 4.066-in.<sup>2</sup> area, which TI claims as the world's densest conglomeration of I/O interconnections on silicon. There are 404 individual nets that require over 50 feet of routing on each memory-bank substrate.

The conference will also

delve into the ongoing migration of MCM technology from high-end military and aerospace applications to low-cost, high-volume commercial applications. An example of this is the joint effort by Multichip Technologies Inc., Ross Technologies Inc., and Mentor Graphics Inc., all of San Jose, Calif. The trio banded to create a dual-RISC-chip set module for use in workstations.

The processor was originally designed and built on a 3.3-by-5.7-in. pc board, using chips in ceramic quad flat packs. Although that version was capable of a 40-MHz clock rate, the packaging and board interconnect limited its speed. The less expensive MCM version, which was designed

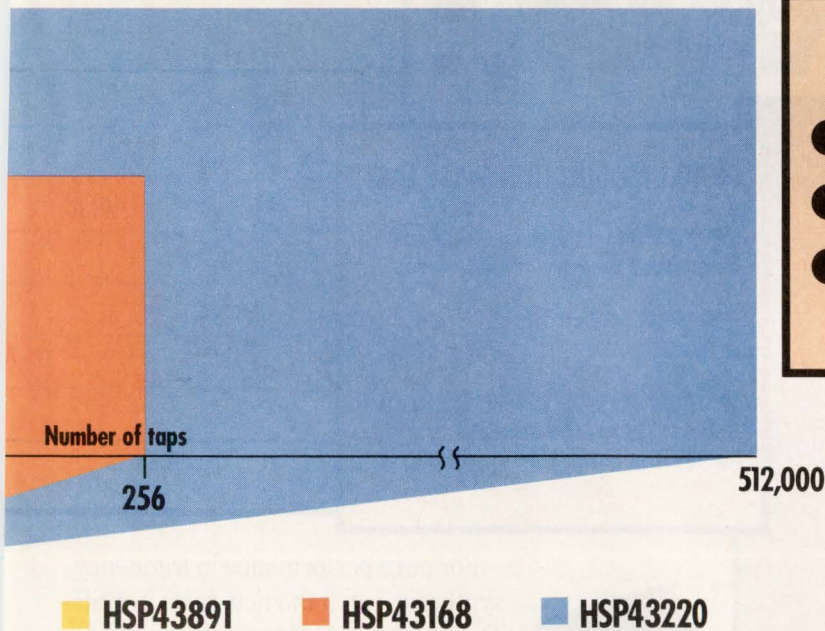
using Mentor Graphics' MCM Station software, showed a 20% speed increase and consumed 10% less power than the 28-W pc board. Analysis showed that the same chip set designed specifically for MCM use could achieve up to 60 MHz, which is a 1.75X improvement compared with the pc-board version.

Manufacturability is essential to continue the migration of MCM technology from high-end to middle- and low-end systems. A technique called planar bonding developed by CNET-France Telecom, Meylan, France, requires no special processing equipment (with the exception of an inserting machine) and uses standard chips. But the technique's

short and thick wire bonds from chip to substrate offer a 3X to 5X speed improvement compared with traditional wire bonding.

Planar bonding involves using a YAG (yttrium-aluminum-garnet) laser to cut holes in a silicon substrate, into which the chips are placed by vacuum tweezers. Once inserted in the holes, the surface of the chips is planar with that of the substrate. After alignment under visual inspection, the chips are glued in by microinjecting liquid resin into the 80-to-100- $\mu$ m gap between the chip and substrate.

A lithographic patterning technique was first used to simultaneously connect all of the chip bonding pads to the sub-



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## TECHNOLOGY ADVANCES

strate. This method, however, required precise filling of the chip-to-substrate gap and a planarization step. The alternative was the planar-bonding technique, which permits wire bonds as short as 100 to 200  $\mu\text{m}$ . By contrast, conventional wire bonds are often longer than 600  $\mu\text{m}$ . Other benefits offered by the technology are that it's easily repairable, and it can fabricate optoelectronic hybrids with deposited wave guides as chip-to-wafer interconnections.

Once the manufacturability issue is settled, other system considerations must be hashed out. As system cycle time decreases, the challenge of distributing high-frequency clock signals among the

different levels of packaging becomes more severe. A paper from IBM Corp.'s East Fishkill, N.Y. facility, states that the clock system should be viewed as an application that spans every technology comprising the computer. As the clock signal is distributed to various parts of the system, the goal is to minimize clock skew, which is defined as the arrival-time difference between any two clock edges.

Several factors contribute to clock skew, but careful design can mitigate them. For instance, nominal design variations, such as differences in via capacitances, can be controlled by careful layout of the clock-distribution network. Another contributor

to skew is the delay tolerances of the circuits and packages. Chips and packages can be sorted to reduce these variations. The clock system can also be designed to be "tunable." Other skew contributors include coupled noise, delta-I noise, and reflection noise. Reflection noise, which results from capacitive loading and packaging discontinuities, is controllable if carefully designed.

Testability and reliability are also hot topics for MCM builders and users. Many problems with die and module testing must be overcome before MCMs represent a reliable, cost-effective vehicle for systems houses. At the ASIC Division of Motorola Inc., Chandler, Ariz., the MCM

test philosophy includes not only a functional-module test, but also good electrical and thermal analysis. This again illustrates the need for a system approach to MCMs.

Motorola's test approach begins well before final-module testing by simulating design parameters to ensure that the design operates within its specified limits, and to generate test vectors for final testing. After physical design is performed with an MCM place-and-route tool, special analysis tools are applied to evaluate the electrical and thermal properties of the design.

The hardware-test methodology encompasses both die and module testing. Functional testing is per-

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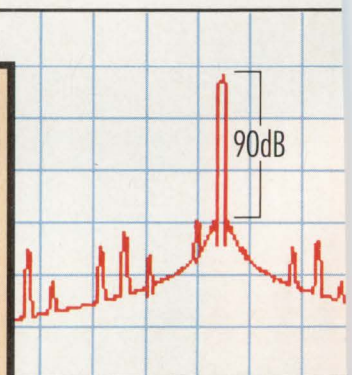
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## TECHNOLOGY ADVANCES

formed at the expected operating frequency, and includes propagation-delay measurements, setup-and-hold measurements, and parametric testing. Then, characterization testing is executed to determine the module's electrical and thermal properties.

Thermal considerations are still another area of concern for MCMs that can benefit greatly from a system-level design approach. A paper from Alcoa Electronic Packaging Inc., Alcoa Center, Pa., describes an analysis of various methods of removing heat from flip-chip-mounted die. One such method used a glass-filled solder-bump encapsulant to improve heat flow from the die to the substrate. That's be-

cause, generally, heat transfer through the solder bumps is inadequate for individual chips dissipating 10 to 30 W. The other methods involved conducting heat from the back of the die to the module's lid. The transfer media studied include metal-filled elastomers, conductive pastes, and solders.

The results showed that indium-alloy solders had the highest thermal performance for back-of-die heat removal. The metal-filled elastomers proved to be effective, but not as effective as the thermally conductive pastes. Going the other way with a solder-bump encapsulant is also effective, but it makes rework more difficult.

Materials research is a

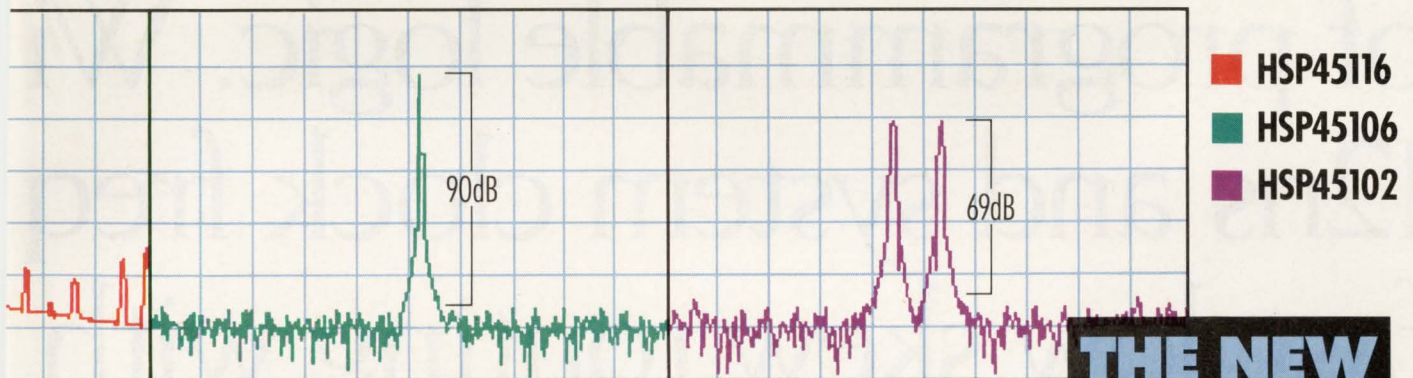
key to improving the performance of high-end MCMs. The dielectric constant of substrate materials is critical for reducing coupling between conductors, which provides lower levels of crosstalk as well as lower dielectric losses and impedances. Because dense ceramic-glass substrate materials have already been pushed to their limit in terms of dielectric constant, materials researchers have turned to controlled-porosity ceramics as an alternative.

At the University of Illinois, Urbana, a process for synthesis of hollow mullite microspheres holds promise as a way to lower the dielectric constant of ceramics (mullite is an orthorhombic silicate of alumi-

num). Research centers on a dielectric-constant range of 2.5 to 3.5. A new material in this range would nearly double the propagation speed of alumina, which is a standard material in MCM packaging. Polyimide falls in this particular range, but its relatively high moisture absorption, poor heat dissipation, inability to withstand serial processing, and other drawbacks impose design limitations not associated with inorganic materials like ceramics. The work at Urbana represents an effort to produce a low-dielectric-constant material that can be reheated to more than 800°C and stay within known metallization techniques.

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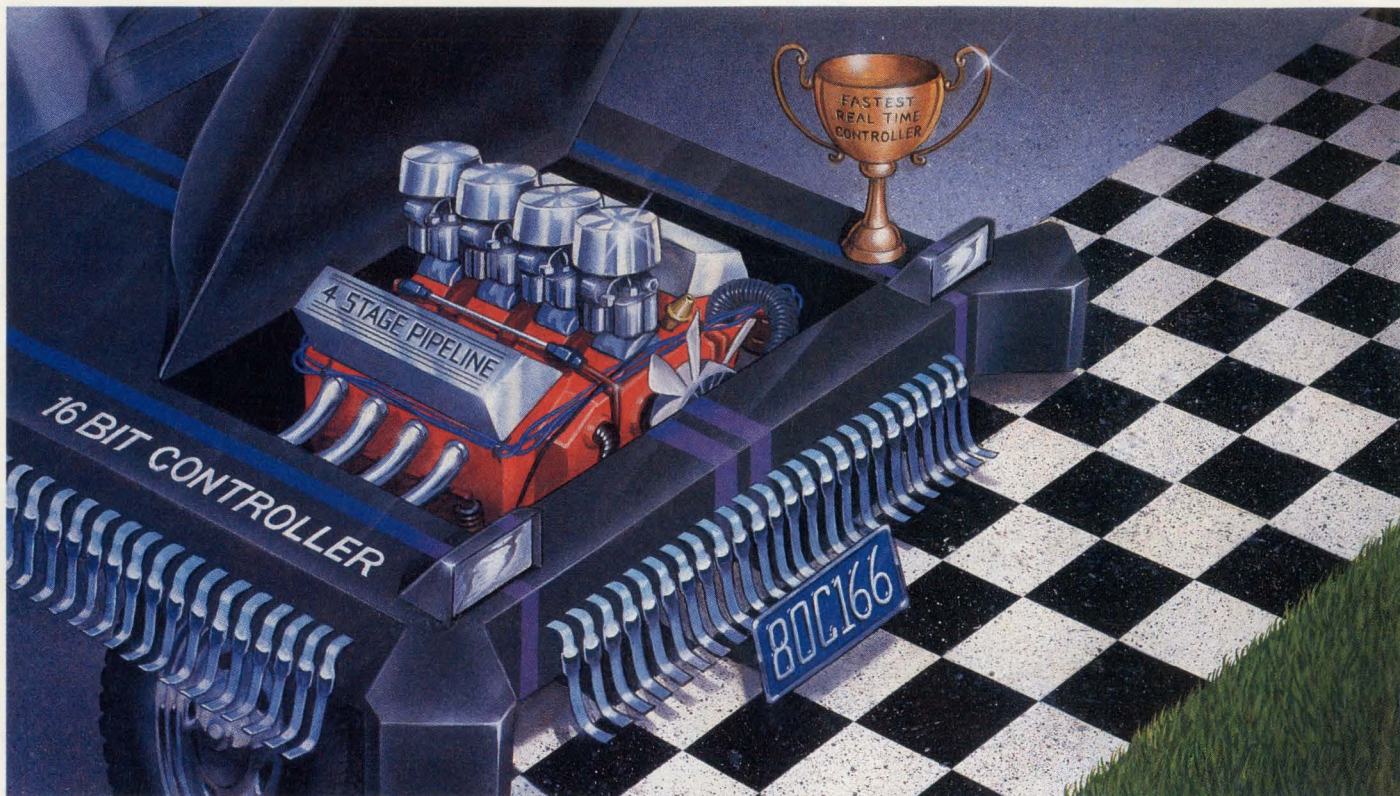


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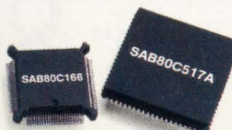
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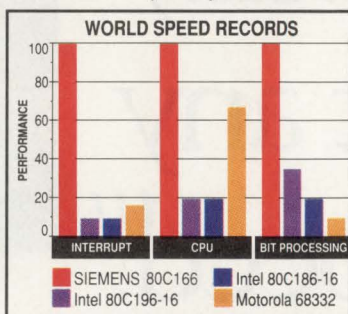
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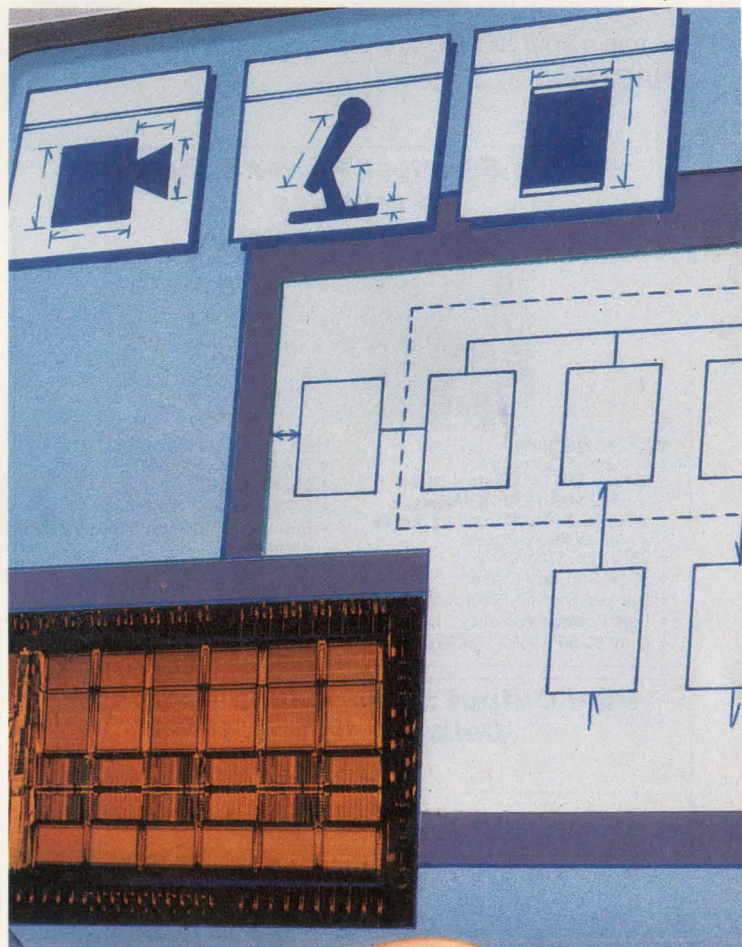
# SILICON SOLUTION MERGES VIDEO, STILLS, AND VOICE

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**O**ne of the biggest roadblocks to the spread of stored interactive video and video-telephony technologies has been the lack of low-cost compression and decompression hardware. As vital elements for transmitting and storing huge amounts of video, graphical, and audio data, compression and decompression algorithms have been available for some time. But prior silicon designs for implementing these compute-intensive algorithms left much room for improvement in terms of price, pc-board area, parts count, and power consumption.

The industry's latest silicon solution to this dilemma is a joint development by AT&T Microelectronics and AT&T Bell Laboratories. The AVP1000 video-codec chip set executes MPEG (Motion Picture Experts Group) and Px64 (called H.261 by the Consultative Committee for International Telephony and Telegraphy) compression and decompression algorithms for full-motion video. When used with the AT&T DSP3210 digital-signal processor, the chip set also performs JPEG (Joint Photography Experts Group) encoding to form the core technology for building desktop PCs with stored interactive video and video telephony capability. This technology can also be applied to a variety of other interactive point-of-sale and point-of-information machines, such as automatic tellers, cash registers, and kiosks.

The chip set consists of four devices: two encoder options (the AVP1300E and 1400E), the AVP1400D decoder, and the AVP1400C system controller. The low-cost AVP1300E is a Px64 encoder that also performs MPEG I-



frame encoding (see "About compression algorithms," p. 49). Greater compression ratios and picture quality are offered by the AVP1400E encoder, which also executes Px64 and full MPEG encoding (I-frame, P-frame, and B-frame). Both versions have ten major function blocks each (Fig. 1).

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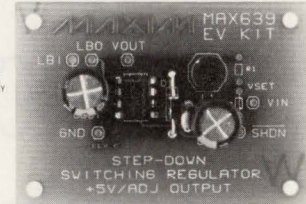
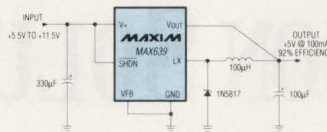
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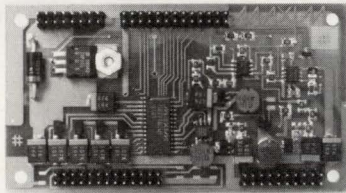
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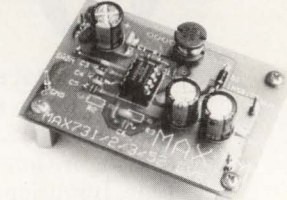
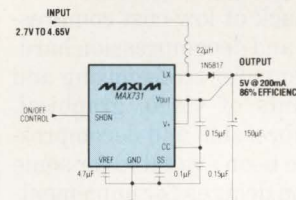
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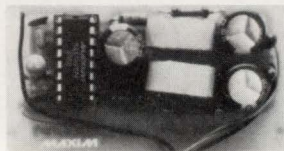
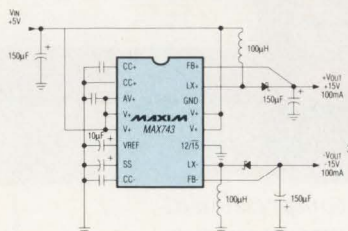
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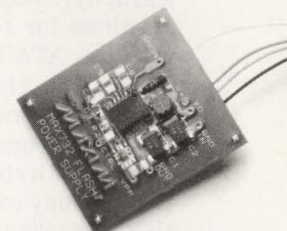
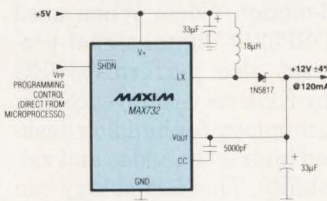
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- ◆ No Transformers
- ◆ Only \$4.49<sup>†</sup> - MAX743CPE

#### MAX743 EV Kit Includes:

- ◆ MAX743CPA Dual-Output, Switch-Mode Regulator
- ◆ PC Board
- ◆ 150 $\mu\text{F}$  Capacitors
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- ◆ 100 $\mu\text{H}$  Inductors
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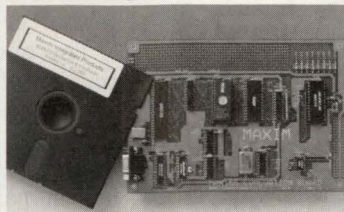
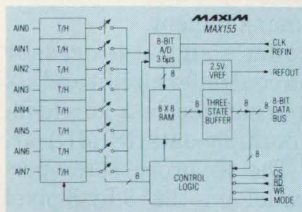
<sup>†</sup>1000-up recommended resale, excludes freight and duty.



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## First 8-Channel Simultaneous ADC — No Phase Delay!



### MAX155 Features:

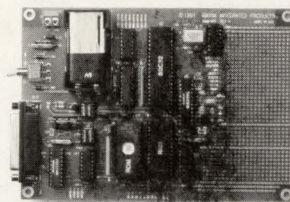
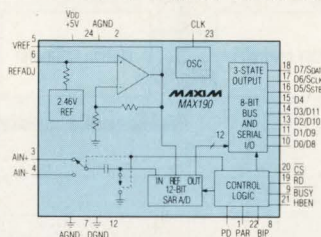
- ♦ 8-Bit, 8-Channel ADC
- ♦ 8 Track and Holds (T/H)
- ♦ 3.6 $\mu$ s Conversion Time/Channel
- ♦ +2.5V Internal Reference
- ♦ Single +5V or Dual  $\pm$ 5V Supply Operation
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- ♦ Only \$10<sup>†</sup> - MAX155BCPI

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  - ♦ MAX233: +5V, RS232
  - ♦ MAX660: CMOS Volt. Conv.

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## 5V Powered 12-Bit ADC with T/H



### MAX190 Features:

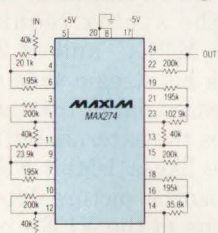
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## 8th-Order Lowpass and Bandpass Filter



### MAX274 Features:

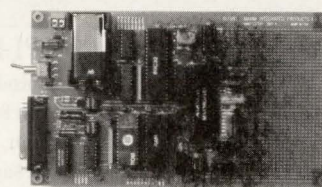
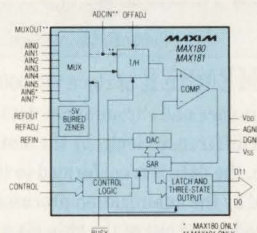
- ♦ Supports Butterworth, Bessel, and Chebyshev
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- ♦ Continuous Time Architecture
- ♦ Low Noise
- ♦ No Clocks Required
- ♦ Only \$4.95<sup>†</sup> - MAX274BCNG

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- ♦ MAX274 Filter IC
- ♦ Filter Design Software
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## Complete 8-Channel, 12-Bit DAS



### MAX180 Features:

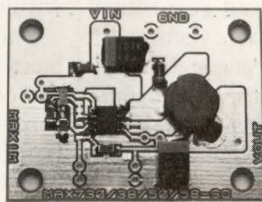
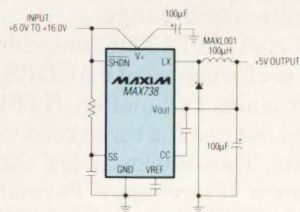
- ♦ 12-Bit 8-Channel ADC
- ♦ Built-In Track & Hold
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- ♦ Int. 25ppm/ $^{\circ}$ C Reference
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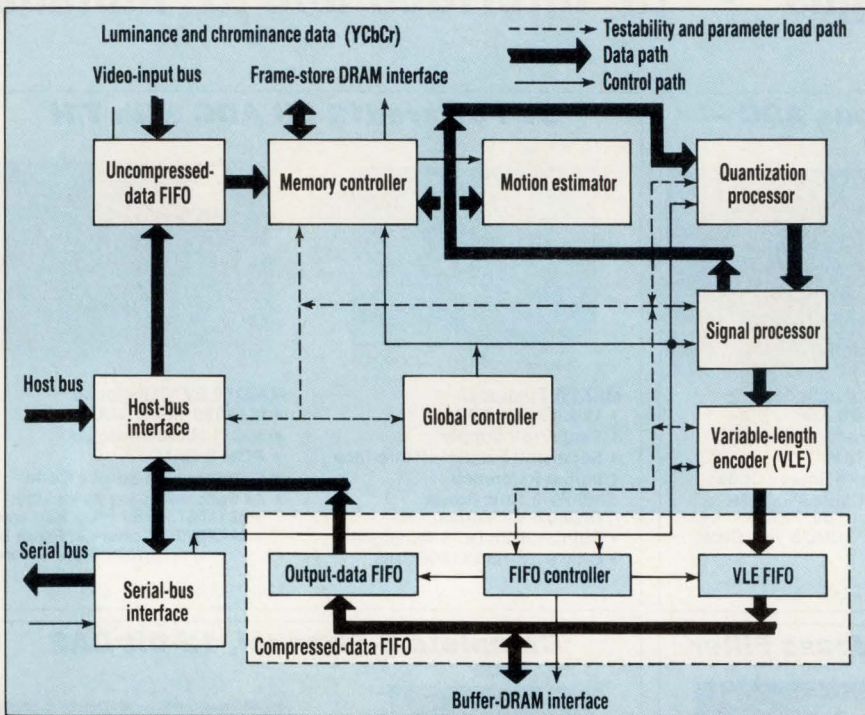
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# MULTIMEDIA CHIP SET



**1. THE MOST COMPLEX MEMBER** of the AVP1000 video-codec chip set is the encoder circuit. Incoming pixel luminance and chrominance data (YCbCr) over the video input bus is converted to 8-by-8-pixel difference blocks by the motion estimator and then passed to the signal processor. Here, the data is transformed to the frequency domain and quantized according to data supplied by the quantization processor. The quantized blocks then pass to the variable-length encoder and out of the chip via a three-part compressed-data FIFO, which absorbs picture-dependent fluctuations in the VLE's data rate, and is output into the serial bus.

to the rest of the encoder function blocks. Raster-scanned input luminance and chrominance data (YCbCr) in a 4:1:1-bit format is held in a 3-kbit uncompressed-data FIFO buffer until it's written into an external 1-Mbyte frame-store DRAM. The FIFO buffer can receive data through either the host bus or a video-input port. A programmable FIFO level register generates a host-interrupt signal at a predetermined level and provides FIFO status on the video-input port.

The encoder's motion estimator circuit compares current-frame macroblocks with previous-frame macroblocks (reference frames) within a finite search area, which is centered on the position of the current macroblock. The motion estimator circuit then finds the reference macroblock having the closest match to the current macroblock.

The encoder's memory controller

arbitrates access to the frame-store DRAM. It transfers the contents of the uncompressed FIFO into the DRAM. It then reads the appropriate search area from the previous frame and the current macroblock from the DRAM into the motion estimator. Next, it writes the motion estimator's best-matched and reference macroblocks and motion vectors to the quantization processor. This is followed by writing the coded macroblock generated by the signal processor into DRAM. The memory controller interfaces directly with industry-standard DRAMs and automatically generates refresh cycles.

Output frame rate and quantization-step size are determined by the quantization processor on the basis of best picture quality, without overflowing or underflowing the video buffer. The processor does this by using an adaptive quantizer and buffer-control algorithm that en-

ables users to adjust picture quality, encoding delay, and output frame rate. A constant-quality, variable-bit-rate mode allows the user to set the quantization-step size. The quantization processor is also responsible for buffer management.

The encoder's signal processor consists of a controller circuit and six processors organized in a single-instruction, multiple-data (SIMD) architecture. The six processors operate in parallel on the 8-by-8-pixel blocks, performing such functions as discrete cosine transformations (DCTs), quantization, zig-zag scanning, inverse discrete cosine transformations (IDCTs), as well as inverse quantization.

Information produced by the signal processor goes to the variable-length encoder (VLE), which generates a compressed bit stream in compliance with the syntax requirements of the MPEG and H.261 standards. This bit stream then enters the compressed-data FIFO buffer, which makes the external buffer DRAM operate like a 1-Mbit FIFO buffer, and absorbs picture-dependent fluctuations in the VLE's output data rate. The FIFO holds the compressed bit stream that is read by the serial interface or the host.

For higher compression ratios and picture quality, the most-powerful and compute-intensive coding technique available is motion-estimation with full-exhaustive search, which is used by both AT&T encoders. This technique performs a motion search by evaluating each individual pixel within a finite search range.

The low-cost AVP1300E encoder has a peak performance of 6.5 GOPS. The chip provides full-motion H.261 compressed images for three resolution formats. These formats are the CIF (Common Interchange Format of 352 pixels by 288 lines), the QCIF (Quarter CIF of 176 pixels by 144 lines), and the CIF240 (325 pixels by 240 lines), at a refresh rate of up to 30 frames/s. The encoded bit rate is selectable from 40 kbits/s to 4 Mbits/s.

The encoder chip performs H.261 compression with both intracoded-frame (I-frame) and predictive-frame (P-frame) techniques. I-frame



# MULTIMEDIA CHIP SET

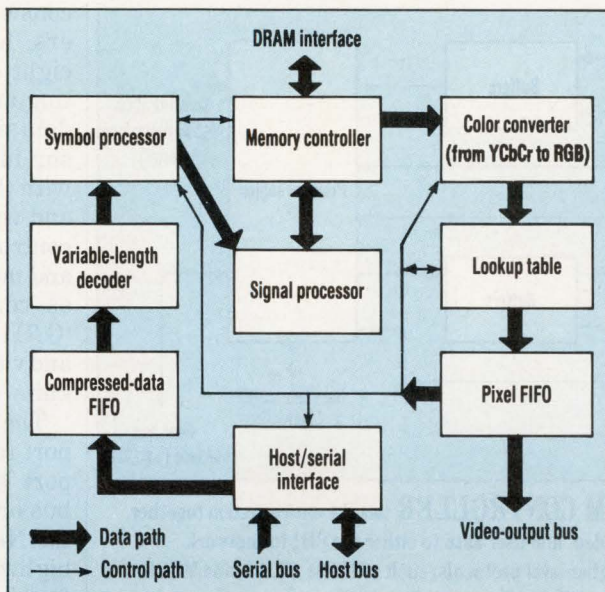
coding exploits redundant pixels within a frame; P-frame coding produces higher compression ratios by exploiting pixel redundancies between frames. To support digital editing and high-resolution still images, the chip also provides MPEG I-frame compression. Motion vectors for P-frames are derived from a full exhaustive search over a  $\pm 15$ -pixel motion-search range. Spatial resolution is user-definable in multiples of 16 bits, up to 720 pixels by 576 lines, with downloadable quantization matrices.

Like the low-cost encoder, the 25-GOPS AVP1400E encoder also performs full H.261 compression using I-frames and P-frames. In addition, the encoder combines motion estimation with full exhaustive search over a greater pixel range ( $\pm 32$  pixels) within a one-half-pixel accuracy. For even greater compression ratios and better picture quality, the chip also supports up to two successive inter-

polative frames (B-frames).

Both encoders require 1 Mbyte of external 60-ns DRAM when configured for MPEG and H.261 operation. They also accept raster-scanned

YCbCr data from an input video bus or host-bus interface, and deliver compressed output data through either their host or serial-bus interfaces. On-chip FIFO buffers absorb picture-dependent fluctuations in the compressed data rate. The encoders also use an adaptive quantizer/buffer control algorithm that enables users to adjust picture quality, encoding delay, and output frame rate. The encoders interface directly with external DRAM and the AVP1400C system controller.



**2. THE DECODER'S** primary controller is the programmable symbol processor, which receives symbols and frequency-domain data from the variable-length decoder and passes this information to the signal processor, which recreates the original luminance and chrominance video signals. The color-space converter transforms this luminance and chrominance data to RGB format.

## DECODING THE DATA

The AVP1400D decoder accepts compressed data through either its parallel host bus or its serial bus, and delivers decoded raster-scanned 24-bit RGB or 4:2:2 YCbCr pixels through either its host bus or a dedicated pixel bus. Key features include on-chip color conversion, a 4-kbit FIFO buffer for storing compressed data, and direct interfaces to the sys-

## ABOUT COMPRESSION ALGORITHMS

**D**ata compression serves as the linchpin of stored interactive video and telephony by supporting the reduced data rates necessary for efficient disk storage, bus-bandwidth usage, and network transmission. It's also by far the most compute-intensive of the tasks required for multimedia systems. MPEG (Motion Picture Experts Group) and H.261 requirements for decompression are explicitly defined, and decoder implementations from one vendor to the next must be consistent.

However, compression algorithms are not clearly defined by the standards. Consequently, encoders from various vendors claim to be MPEG- and H.261-compliant yet they can differ sub-

stantially in several performance features. These features include compression ratio, bit rate, frame rate, resolution, delay, and picture quality. I-frame MPEG encoders are optimized for still frames and digital editing. Conversely, full-function MPEG encoders maximize compression ratios and picture quality by using motion-estimation operations with full exhaustive search over expanded search ranges, together with techniques involving one or more interpolative frames.

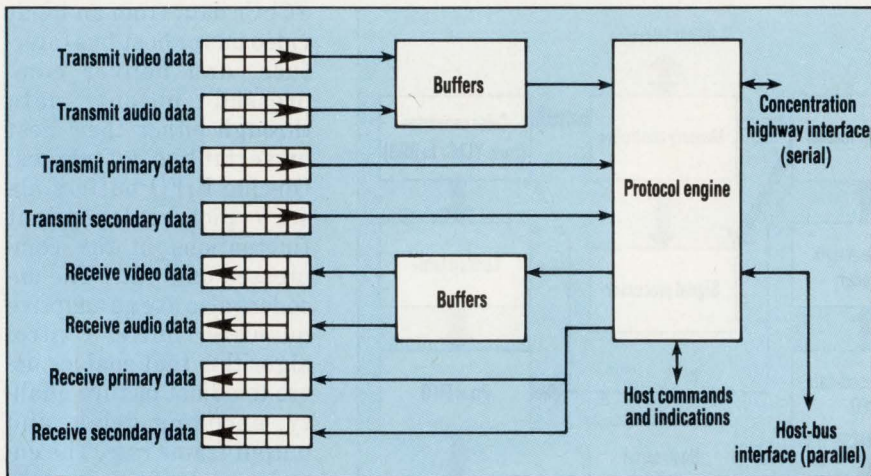
H.261 encoders are optimized to provide good picture quality with minimal delay over a broad range of bit rates. Available devices typically differ in maximum encoded bit rate, resolution, the motion-estimation algorithm, or delay. A

broad range of bit-rate capability (56 kbits/s to over 1.5 Mbits/s) is necessary to maintain good picture quality when transmitting over a range of telecommunications channels, such as Switched 56, basic-rate ISDN, T1, primary-rate ISDN, and CEPT (Conference of European Post, Telephone, and Telegraph).

MPEG encoding provides even more flexibility, which results in even greater variations in encoder quality among vendors. For example, MPEG doesn't fix picture resolution or motion-estimation search range. As a result, some encoders support low-resolution images to claim full-motion video capability. One of the most significant ways MPEG encoders differ is in compression technology.



# MULTIMEDIA CHIP SET



**3. THE AVP1400C SYSTEM CONTROLLER** ties the entire system together, formatting and connecting audio, video, and user data to either the CHI for network transport, or to the host bus. All higher-level protocols, such as H.221, H.242, and MPEG systems-layered, are executed by the AVP1400C's protocol engine.

tem controller and to 1 Mbyte of external 70-ns DRAM (Fig. 2).

The host/serial interface synchronizes host-bus and serial-bus signals to the main input clock. It also contains chip-reset logic. A variable-length decoder (VLD) converts the compressed bit stream into symbols according to the MPEG and H.261 variable-length decoding algorithms. The decoder's primary controller is the programmable-symbol processor, which receives symbols from the VLD and issues commands to the memory controller and signal processor for recreating the original video.

Under control of the symbol processor, the signal processor has an SIMD architecture for performing arithmetic functions, such as IDCT and inverse quantization. Pixel data moves between the signal processor and external frame-store RAM under the control of the decoder's memory control-

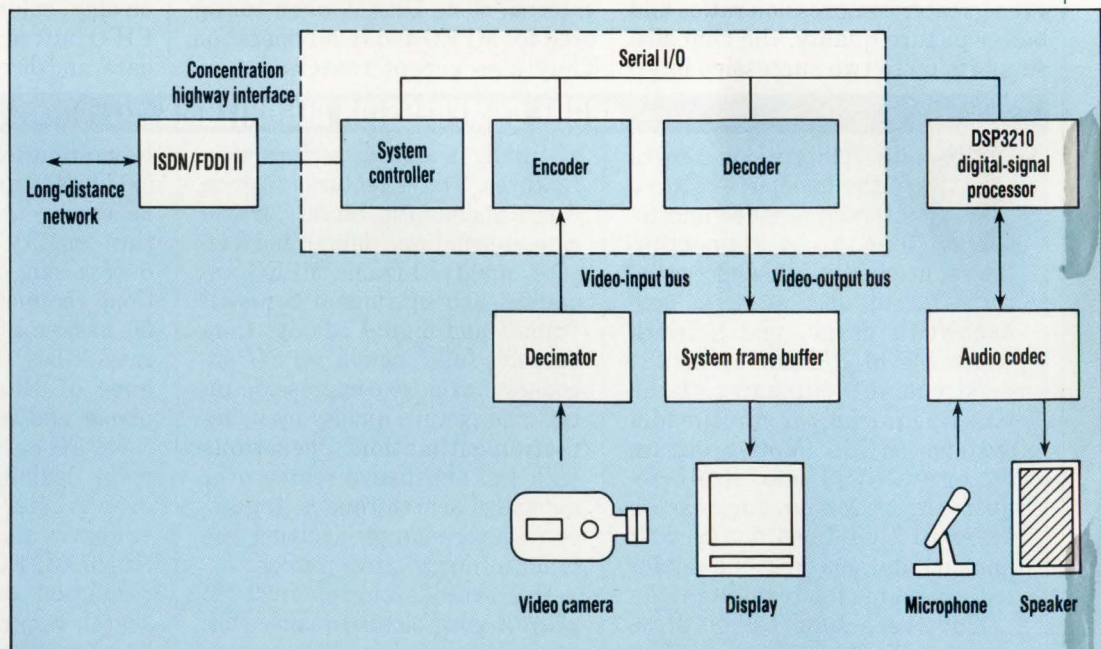
ler. This controller also converts decoded frames from a 4:1:1-bit format to a 4:2:2-bit format, and sends them to the color converter. The memory controller circuit has a glueless interface to industry-standard DRAMs and automatically generates refresh cycles.

The AVP1400C system controller

consists of a protocol engine, buffers, host-bus FIFO buffers, and eight data I/O pipes, for transmitting and receiving audio, video, and data signals (Fig. 3). The host processor initializes and communicates with the APV1400C by reading from and writing to its configuration and control registers. These registers set and monitor system attributes, such as compression mode, audio type (G.711 or G.722 are two examples), and video bandwidth (for instance, 56 kbits/s or 1.5 Mbits/s).

The host bus is the primary input port for MPEG data. The H.221 data port is selectable between the host bus or the Integrated Services Digital Network (ISDN) concentration highway interface (CHI). This interface is a configurable four-wire serial, time-division-multiplexed interface that provides full-duplex access to external communications channels at data rates up to 4096 kbits/s. External SRAM is needed to store the downloadable program for the chip's internal RISC processor.

The controller's serial-bus interface connects directly to the encoder and decoder, and to AT&T's DSP16,



**4. USED WITH THE DSP3210** digital-signal processor, the AVP1000 video-codec chip set (dashed lines) comprises the core of a multimedia and videoconferencing system. Such a system can interface to a high-speed network such as ISDN and FDDI II. The only major external functions needed are an audio codec for connecting a microphone and speaker, a system frame buffer for connecting a video monitor, and a decimator for interfacing to a video camera.







## MULTIMEDIA CHIP SET

DSP32, and DSP3210 digital-signal processors. Ten serial I/O channels are allocated among ten different functions for transporting audio, video, and data signals.

### SYSTEM DESIGN

AT&T says the AVP1000 video-codec chip set uses compression algorithms that surpass the minimum requirements of the standards. Full MPEG compliance requires not only compression and decompression, but also MPEG systems-layer multiplexing and demultiplexing for audio, video, and user data. Similarly, full H.261 compliance calls for a variety of framing, channel-management, error-correction, and other communications functions. These include the H.221 transport protocol that addresses the multiplexing, demultiplexing, and framing of audio, video, and user data; H.230 which defines call setup and tear-down procedures;

H.242 which defines the handshaking protocol for two videoconferencing terminals; and the means of determining frame-bandwidth allocation between audio, video, and user data.

Where most competitive solutions assign these functions to higher-level software, the AVP1000 chip set combined with the DSP3210 digital-signal processor provides all of the functionality required for MPEG, H.261, JPEG, and audio (Fig. 4). In addition, these devices offer a number of key system-level functions not included in the standards, such as channel management and acoustic echo cancellation.

The chip set also supplies the functions needed to support teleconferencing. Once audio, video, and user data are encapsulated as H.221 frames, they must be transported over a telecommunications network. Presently, the most commonly used

links for video telephony are T1, fractional T1, Switched 56 (56-kbits/s Accunet), and switched 384-kbits/s lines. Basic-rate and primary-rate ISDN services will be added in the future. The AVP1400C's CHI bus offers a direct interface with AT&T's family of communication ICs for all of these telecommunications links. Through the CHI, the controller can transmit and receive H.221 frames to and from the network's communications controller.

### RELIEVING OVERHEAD

Relieving the host bus of this traffic reduces the load for the host, freeing it to perform other multimedia tasks. It also enables the network clock to be recovered for synchronizing the audio codec that provides audio data to the DSP3210.

AT&T offers a solution to support network cards that provide only a host-bus interface without using the



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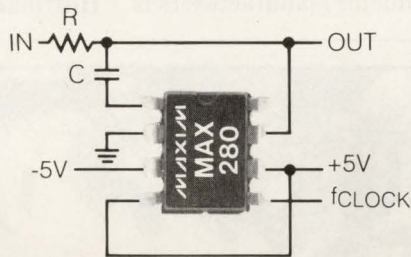
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## MULTIMEDIA CHIP SET

CHI. The solution employs a phase-lock loop (PLL) controlled by the DSP3210 audio decoder. The frequency of the PLL is controlled by a signal from the 3210 based on the FIFO-buffer level. In addition, audio samples are dropped during periods of silence. But the best solution is to wire a direct CHI connection between AT&T communication ICs and a video controller.

Another valuable feature integrated into the AVP1000 video-codec chip set is the functionality commonly provided by Channel Service Units (CSUs). These \$10,000 box-level systems combine, synchronize, and lock multiple incoming and outgoing communications channels. The AVP1400C system controller combines and synchronizes up to three switched 56-kbit/s, switched 384-kbit/s, and ISDN B-channel lines.

One of the biggest challenges facing semiconductor manufacturers is

how to partition their designs among hardware and software, to maximize performance and flexibility while minimizing cost. Some companies sacrifice performance for maximum flexibility by using a general-purpose programmable processor to support both proprietary algorithms and MPEG, H.261, and JPEG requirements. Because compute-intensive operations such as motion estimation require 20 GOPS or more of processing power, full-motion and H.261 designs typically require several general-purpose processors. Other companies use a hardwired solution to maximize performance at the expense of reduced flexibility, which is required for responding to changing standards.

AT&T chose a hybrid design that exploits the best of these two approaches. Compute-intensive functions, such as motion estimation and Huffman encoding, are fixed in the

standards and are unlikely to change. Consequently, AT&T implements these functions in hardware. Programmability is reserved for those aspects of the algorithm that can be tailored to specific applications. These include functions that determine frame rate, delay, bit rate, and resolution. Sections of the standard that are less stable, such as specified by H.221 and H.242, and less-compute-intensive functions, like those specified by H.261, are implemented in on-chip, downloadable software because their status is more likely to change.

Also better suited to a programmable approach are JPEG and MPEG/H.261 audio standards, which cover a broad range of options and special cases. JPEG, for example, supports a wide range of different resolution, color space, and compression ratios. Similarly, MPEG and H.261 each support several levels of audio quality, some of which have yet to be standardized.

AT&T exploits the general-purpose programmability of the DSP3210 digital-signal processor to handle such functions. The various audio options of the MPEG, and H.261 recommendations are implemented as a library of DSP3210 C-callable multimedia software modules. Depending on application requirements, one or more of these modules are loaded, scheduled, and executed on the DSP3210, under the control of AT&T's VCOS (Visible Caching Operating System). □

### PRICE AND AVAILABILITY

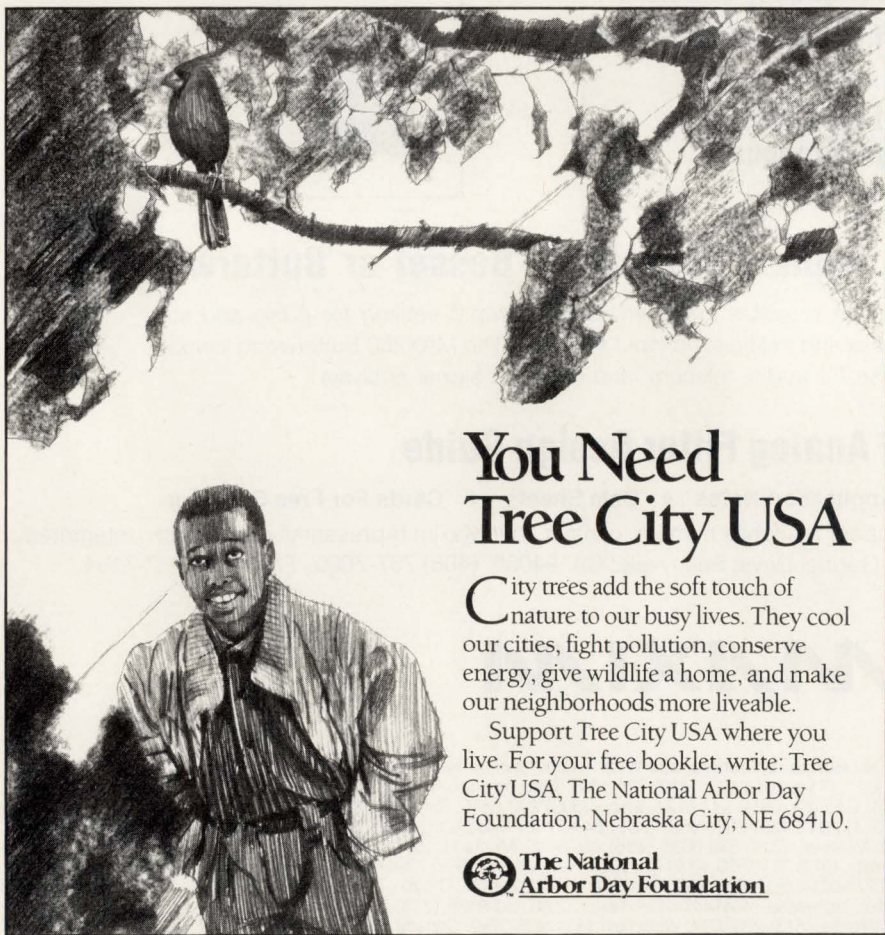
*The AVP1000 video codec chip set, comprised of the AVP1300E encoder, the AVP1400D decoder, and the AVP1400C system controller, is available now in OEM quantities for \$376 per set. The AVP1400E encoder will be available in the fourth quarter of 1992. All three chips are available in a 159-pin plastic PGA package.*

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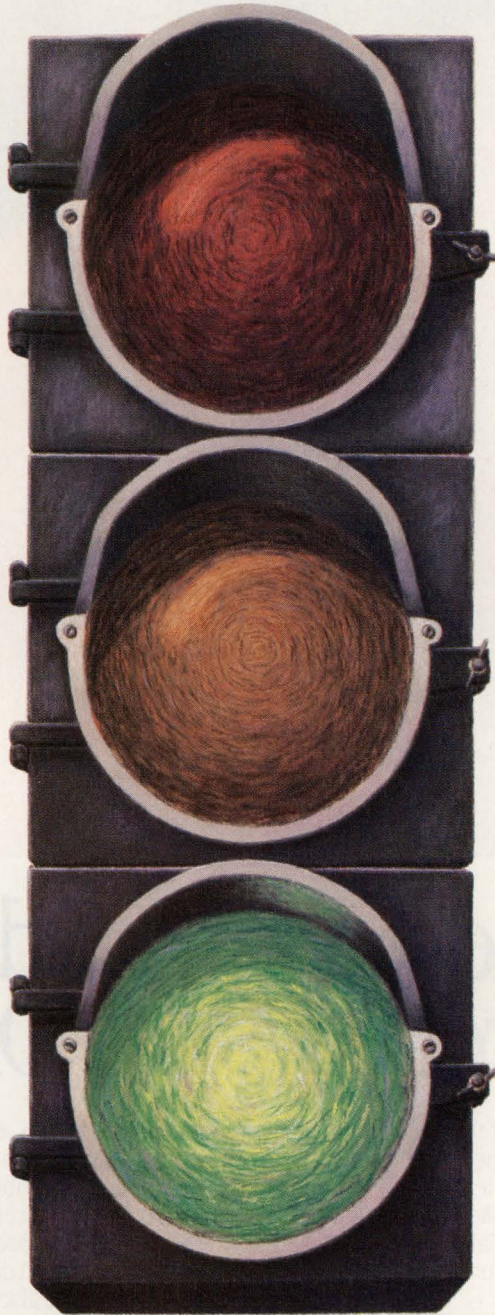
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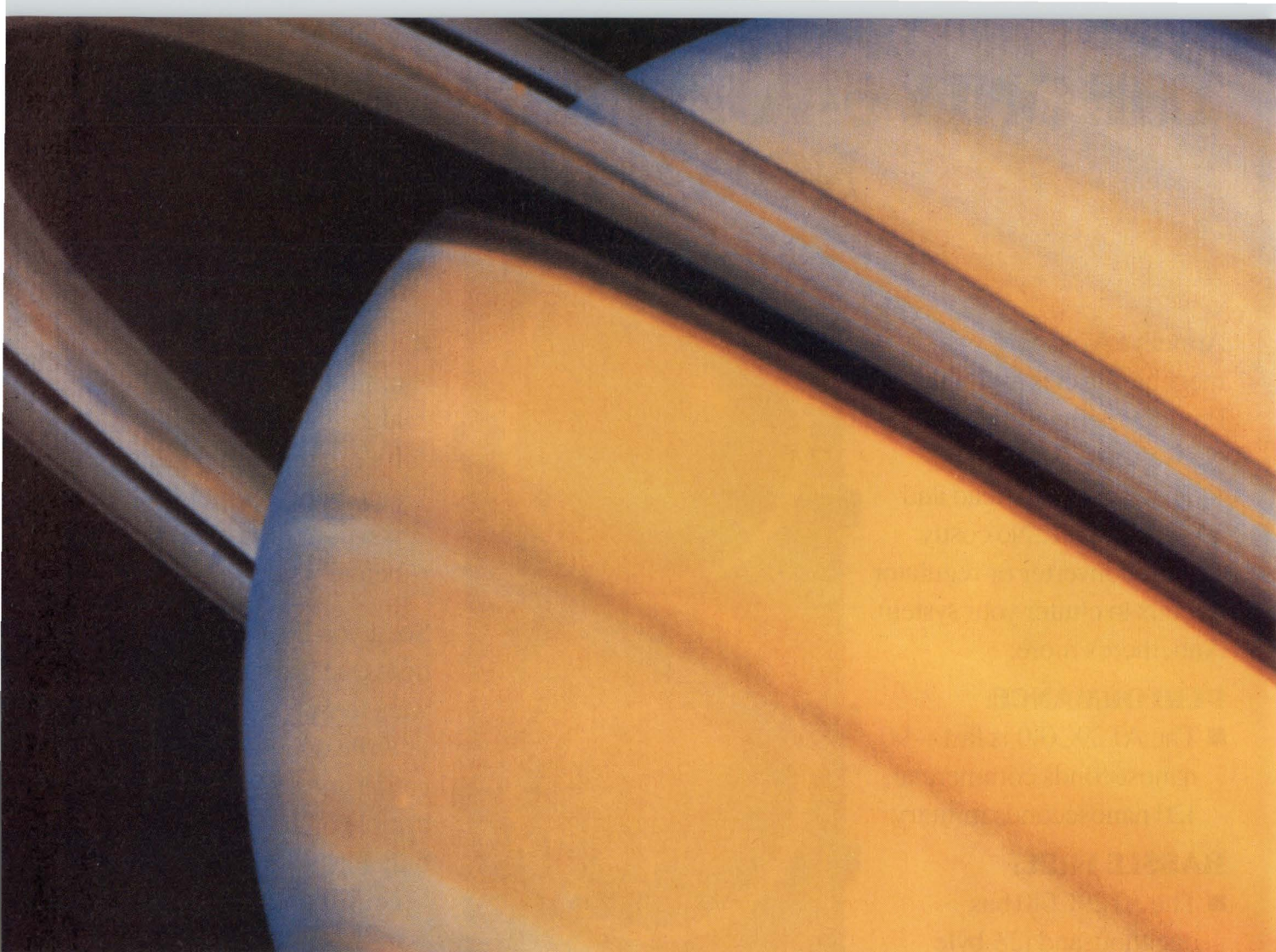
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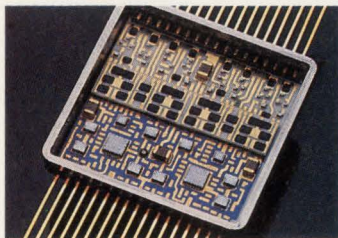




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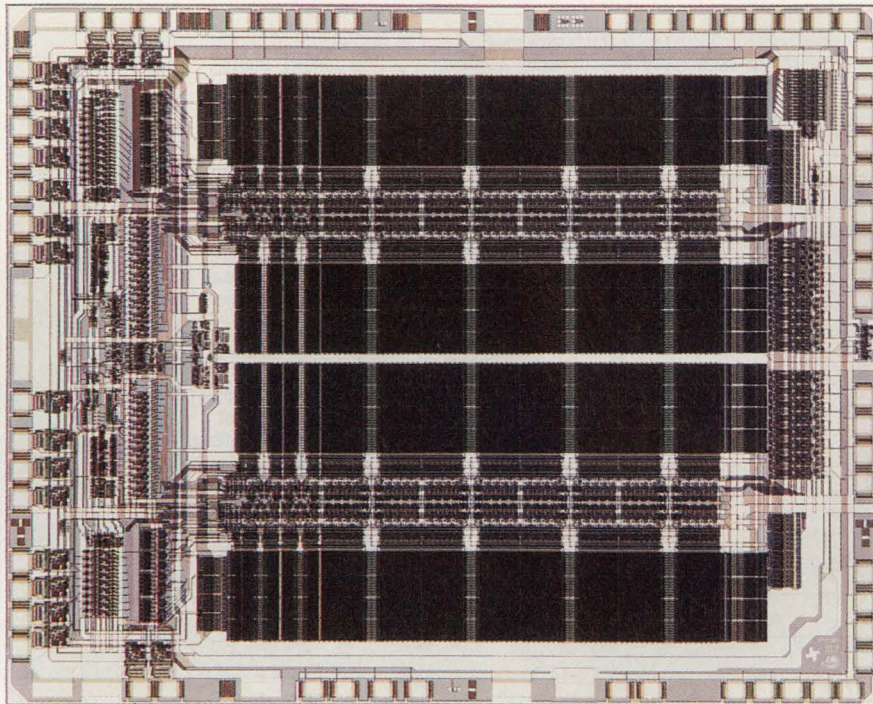
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Cypress Semiconductor Corp.

# ENHANCED SRAMS PROPEL SYSTEMS PERFORMANCE

**T**he dependency of high-performance computer systems on large primary and secondary caches has pushed high-speed static RAMs into greater prominence in these systems. Although they're not the only systems that place demands on static RAMs for shorter access times and higher storage capacities, CISC- and RISC-based microprocessor systems are rapidly becoming the number one consumers of fast static memories, due to their reliance on caches to hold key information.

As each generation static RAM is

**DAVE BURSKY**

## THE VENERABLE STATIC RAM EVOLVES AS USERS DEMAND VERSIONS TUNED FOR NARROW MARKET SEGMENTS.

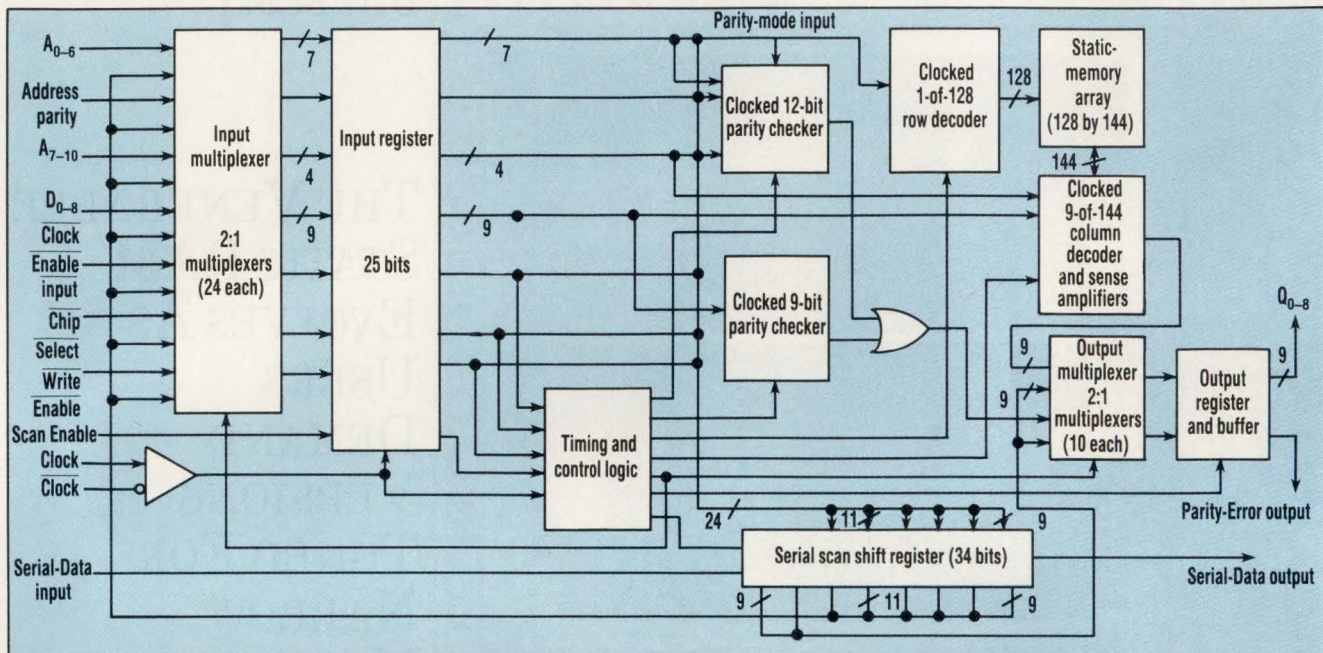
introduced, the definition of "fast" seems to evolve along with the technology. Today's definition of fast, at less than 25 ns per memory access, wasn't even achievable 10 years ago when 55 to 70 ns was considered fast. And for future-generation memory chips, that definition will fall to the 10-to-15-ns range.

To speed the chips, silicon designers are moving from CMOS to biCMOS processes. In some cases, that also includes employing either ECL interfaces or full bipolar ECL circuit designs to attain the sub-10-ns access times required by top-performing systems. Furthermore, chip-feature sizes are shrinking, and with the smaller features come improved speed, higher density, and more systems flexibility.

Not only have the memory access times shortened, but the variety of memory types and the storage capacities have grown considerably. No longer are SRAMs only available in 1-, 4-, and 8-bit-wide configurations, but also in 5-, 9-, 10-, 12-, 16-, 18-, 20-, 24-, and soon even in 32- or 36-bit-wide pinouts. And some of those are specialized versions incorporating such features as burst-transfer



## FAST AND WIDE STATIC RAMS



### 1. ALL SIGNAL-TIMING OPERATIONS

are kept internal on the SY100492 self-timed static RAM developed by Synergy Semiconductor. An on-chip timing and control-logic block manages all internal operations once the clock and write-pulse signals are received by the memory. The timing block then supplies all of the correctly sequenced signals for the parity checkers, the row and column decoders, the output multiplexer and output register, and the serial-scan diagnostic shift register. Direct control of all internal operations minimizes signal skews and maximizes chip performance—the access time is just 5 ns for the 9-bit-wide word.

modes, cache-tag control logic, input or output registers or latches, self-timed write control signals, and more. These chips continue to widen the range of choices available to the designer to best match the memory subsystem to the system architecture.

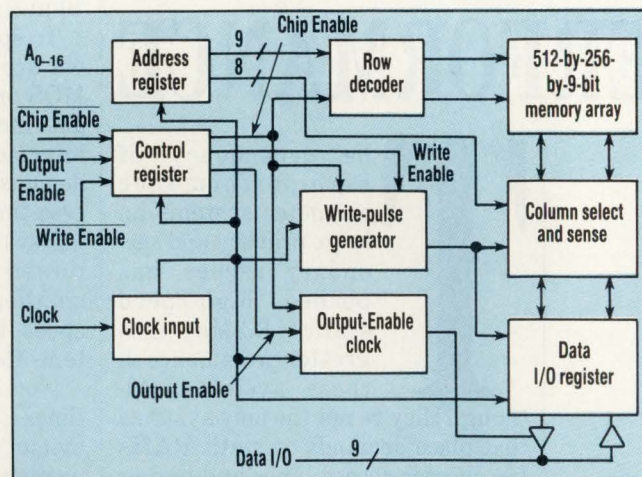
Memory densities for fast SRAMs have progressed to the point where designers can choose storage capacities ranging from below 16 kbits/chip to 1 Mbit for production devices. Such devices are typically fabricated with minimum feature sizes of between 0.7 to 0.9  $\mu\text{m}$  for the gates—the smallest features currently in volume production by most suppliers. Furthermore, early samples of 4-Mbit SRAMs, fabricated with 0.5- $\mu\text{m}$  features, are also being released to a few companies for early evaluation. Research labs, working with deep-sub-micron process-

es that typically have features around 0.35- $\mu\text{m}$  minimum, are trying to produce viable samples of 16-Mbit devices.

With memory densities quadru-

pling, memory cells are now switching back to full CMOS structures. Early SRAMs were typically fabricated with six-transistor (6-T) memory cells, employing p-channel devices as active load elements to form CMOS memory cells. However, as densities increased beyond 64 kbits, the area required for 6-T memory cells made chip sizes uneconomical. Thus, most static-memory designs switched to a four-transistor (4-T) cell that used high-value polysilicon resistors as the load elements. That 4-T cell shrinks the area by about 30% over the 6-T cell, allowing the 256-kbit and 1-Mbit memory generations to be made with reasonable chip areas.

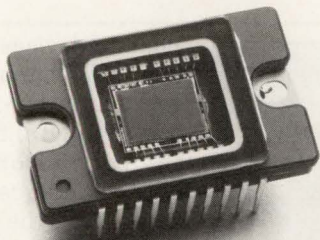
As a result, although most SRAMs sold today are referred to as CMOS devices, the arrays of memory cells at the heart of the chips are typically



**2. A SIMPLER FORM** of a self-timed 9-bit-wide SRAM is achieved in this design by AT&T Microelectronics. A control register on the ATT7C341 captures the write pulse from the external system by sampling the write line with a clock signal. Once captured, the write signal is regenerated by the write-pulse generator and distributed to the logic surrounding the memory core and the data input and output registers.

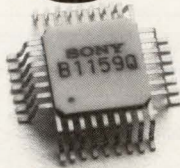


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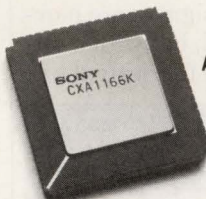
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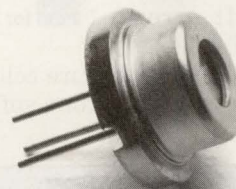
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## FAST AND WIDE STATIC RAMS

built from just n-channel devices, while the surrounding support logic contains full CMOS circuitry. However, as densities grow beyond the 1-Mbit range, several factors come together that force designers to reconsider the 6-T cell.

For starters, the individual cell leakage currents allowed by the polysilicon resistors mount up and make the overall chip leakage current too large. In addition, the area required for even higher-value polysilicon resistors would exceed the current area required by the memory cell, making the chip too large. Finally, the 4-T cells are more sensitive to alpha-particle-induced upsets (soft errors) than the 6-T cells, and with up to 4 million or more cells on the chip, it's very likely for a soft-error to occur.

Thus, memory designers are moving back to a 6-T cell, but with a difference. Rather than fabricate the p-

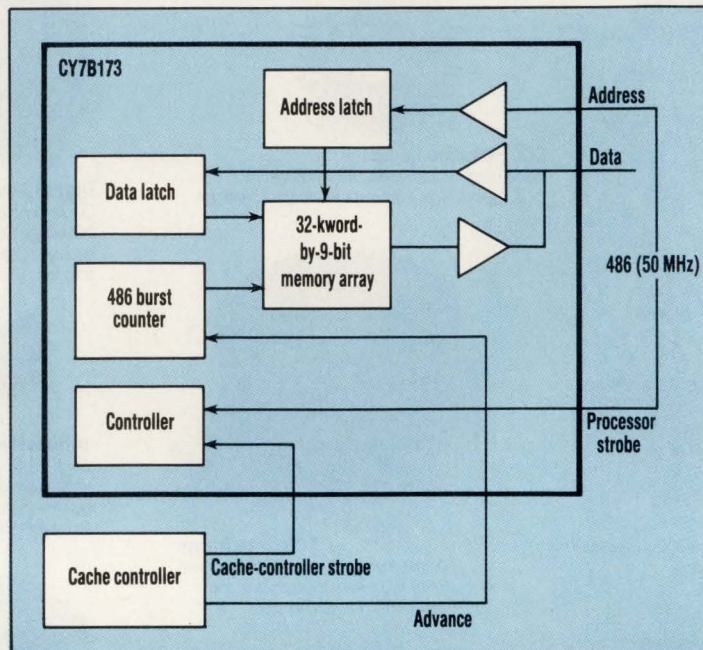
channel devices in the silicon, the manufacturers are using thin-film transistors (TFTs) fabricated in polysilicon layers above the substrate. By fabricating the p-channel devices above the substrate, they don't add to the area consumed by the cell. However, they still provide the multi-gigaohm resistances required to keep the per-cell leakage current to just a few picoamperes.

The penalty faced by the SRAM makers, though, is a much more difficult fabrication process. To form the TFTs, three to five additional processing steps are required. The steps include the use of two or three polysilicon layers plus the two layers already used in most SRAM manufacturing. Those extra processing steps will initially keep the price of the 4-

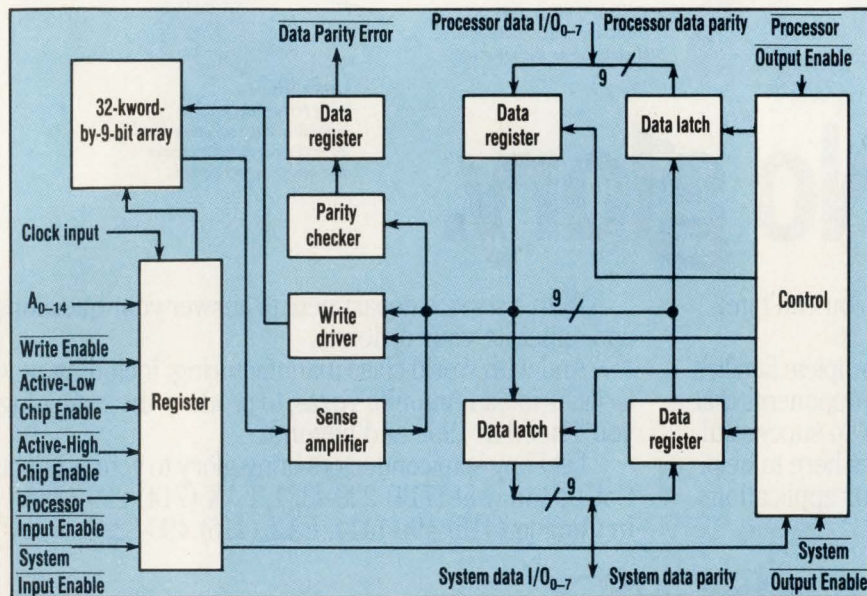
Mbit and 16-Mbit devices very high.

Today's 33-MHz, 32-bit CPUs can employ SRAMs with access times of 20 to 25 ns. However, as CPU clock speeds increase to 50 MHz, SRAM access times must shrink still further—to between 10 and 15 ns—to keep pace with the fast processors. And cache sizes are also increasing in most new systems. Early 16- and 32-kbyte caches are giving way to cache sizes of 64 to 256 kbytes on current-generation systems. In some high-end systems, 1-Mbyte caches are already in use.

As access times shorten, system designers face the problem of controlling the duration of the write signal to the SRAM. To make the SRAM more responsive to the signal and simplify the designer's system implementation task, several SRAM manufacturers created the self-timed RAM (STRAM). This special memory contains all of the timing and control logic to perform the write operation, as long as the input signal to the write-control pin has a



**3. DESIGNED SPECIFICALLY** to connect directly to the Intel 80486 microprocessor is this Cypress CY7B173 burst SRAM. A special 2-bit burst counter and a small localized bus controller embedded in the SRAM eliminate the need to incorporate control logic in the cache controller. The counter cycles the memory array to retrieve four memory words in the out-of-order sequence required by the 80486. A similar version is available for linear address bursts, as required by the Motorola 68040.



**4. TWO DATA PORTS** on the forthcoming Motorola MCM62110 cache RAM enable the chip to isolate the local processor bus from the main system memory bus. As a result, bus loading is reduced on the local bus and CPU speed is improved. On-chip parity checking logic also ensures the integrity of data moving over the chip's internal data bus.



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## FAST AND WIDE STATIC RAMS

minimum acceptable duration (to ensure that the signal isn't just a transient on the line).

The fastest self-timed chip, with an access time of just 5 ns, is an 18-kbit (including a parity bit) bipolar ECL memory developed by Synergy Semiconductor (Fig. 1). The 2-kword-by-9-bit memory includes input and output registers that make it easier for the chip to be incorporated into various pipelined architectures.

The chip's self-timed approach minimizes the impact of timing skews on the memory array's cycle time. All input signals are held in registers on the chip at the transition of the memory clock signal. By registering all inputs and keeping the setup and hold times to less than 2 ns, skew problems are minimized, making very short cycle times practical. Output registers hold the output data valid for an extended portion of the cycle, easing system read-timing requirements.

One feature available on the STRAM is the hidden write cycle. With that hidden cycle, the STRAM can operate at twice the bandwidth of the data output bus. The hidden-write cycle is a scheme that interleaves the read and write cycles in such a way that the write-cycle timing has no effect on the data output bus (read timing). To implement this capability, some subtle changes must be made on how the Chip Select and Write Enable pins are controlled, in comparison to the scheme used on standard SRAMs.

Both AT&T and Sony offer megabit-density CMOS STRAMs, organized as 128 kwords by 9 bits, with 20-ns cycle times and 10-ns clock-to-access times (Sony also has a slightly faster 16.6-ns-cycle-time version). Like the ECL

chip, they pack self-timed write-pulse generation. Register inputs on the chips for all input signals (addresses, data, Write Enable, Chip Enable, and Output Enable) are positive-edge-triggered, as is the output register (Fig. 2).

Similar self-timed operation is embedded into several cache memory chips as well. For instance, Cypress Semiconductor offers several versions of a 32-kword-by-9-bit single-port cache RAM. Motorola is close to releasing a two-ported 32-k-by-9 cache RAM that adds to its current family of 32-k-by-9 CMOS RAMs offered for Sparc, 68040, 80486, and other processors. The Cypress CYB7B173/174 are biCMOS 32-k-by-9 memories that can be accessed in just 14 ns (clock to output). The 7B173 is optimized for use with Intel i486-based systems and includes a two-bit wraparound counter that supports the 80486's nonlinear burst sequence (Fig. 3). The 7B174 sup-

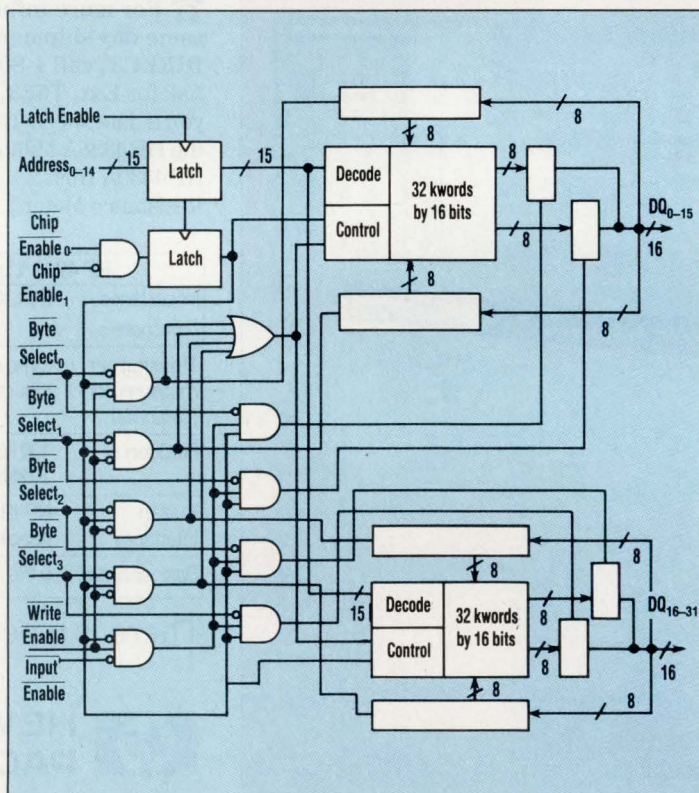
ports a linear burst sequence.

Two address strobe signals can be sent to the chips, one generated by the processor and one by the cache controller, allowing either block to control the memory. By simply sending an "advance" strobe signal to the memory chip, the host system sequences the burst-address counter through its four addresses to supply the four words needed by the CPU's internal cache.

By adding a second I/O data path to its 32-k-by-9 synchronous self-timed write SRAM, Motorola was able to squeeze the chip's access times to as little as 15 ns (17- and 20-ns versions are available as well). The dual 9-bit ports on the forthcoming MCM62110 aren't set up the same way as in a dual-port memory. Instead, they both tie into the same internal data bus and can read or write the same 9-bit words to two external buses (Fig. 4).

The dual sets of data-input registers and data-output registers allow users to isolate the processor bus from the system bus (the memory bus). That reduces the capacitive loading on the processor's local bus and thereby improves system operating speed, trims the chip count and board space, and also cuts system cost. A bypass data path enables data that's written to the input register to skirt around the memory array and be written directly into the output data latches. Consequently, the system can directly write to the processor (or vice versa) for the case of time-critical operations.

In addition to the bypass feature, the 62110 allows data to be streamed between the system and processor ports in either direction. The streaming is done by first latching data



**5. AN 18-BIT BUS** that carries a 16-bit tag and Valid and Dirty flag bits is included on the Cypress CY7B181, one of the widest cache-tag memories available. On-chip comparators and match logic can perform an address match in just 12 ns. A separate dedicated I/O data port allows the tag and data fields to be loaded separately.



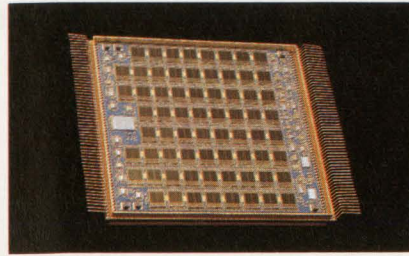


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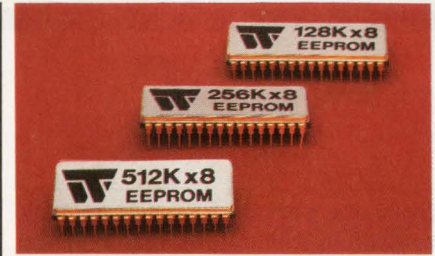


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### 1, 2, & 4-Megabit CMOS EEPROMs

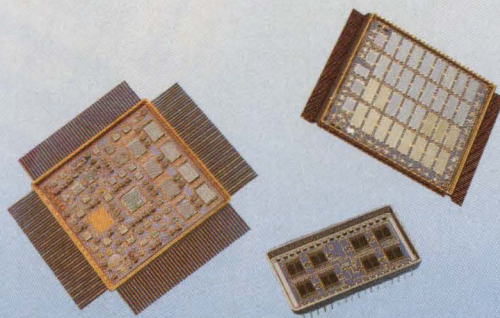
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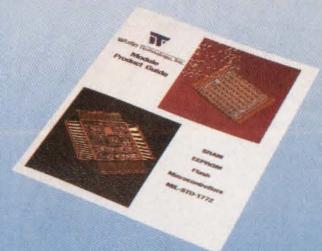
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## FAST AND WIDE STATIC RAMS

from one port and asynchronously controlling the output enable of the other port. The RAM can also be written to while data is streaming through the ports. During every read cycle, the chip performs odd-parity checking.

The dual ports also enable the chip to function as a memory chip that has separate input and output buses. That allows data to be set up during the same cycle as a read operation, avoiding the loss of a cycle solely for reading the memory contents. Although initially conceived as the secondary-cache data-memory chip to support the cache controller for the forthcoming 88110 RISC processor, the 62110 can be used with almost any other processor—the Mips Corp. R4000, the Sparc family, the Intel 80486, and, of course, Motorola's own MC68040.

Motorola, which is planning to offer both 16- and 18-bit versions of a

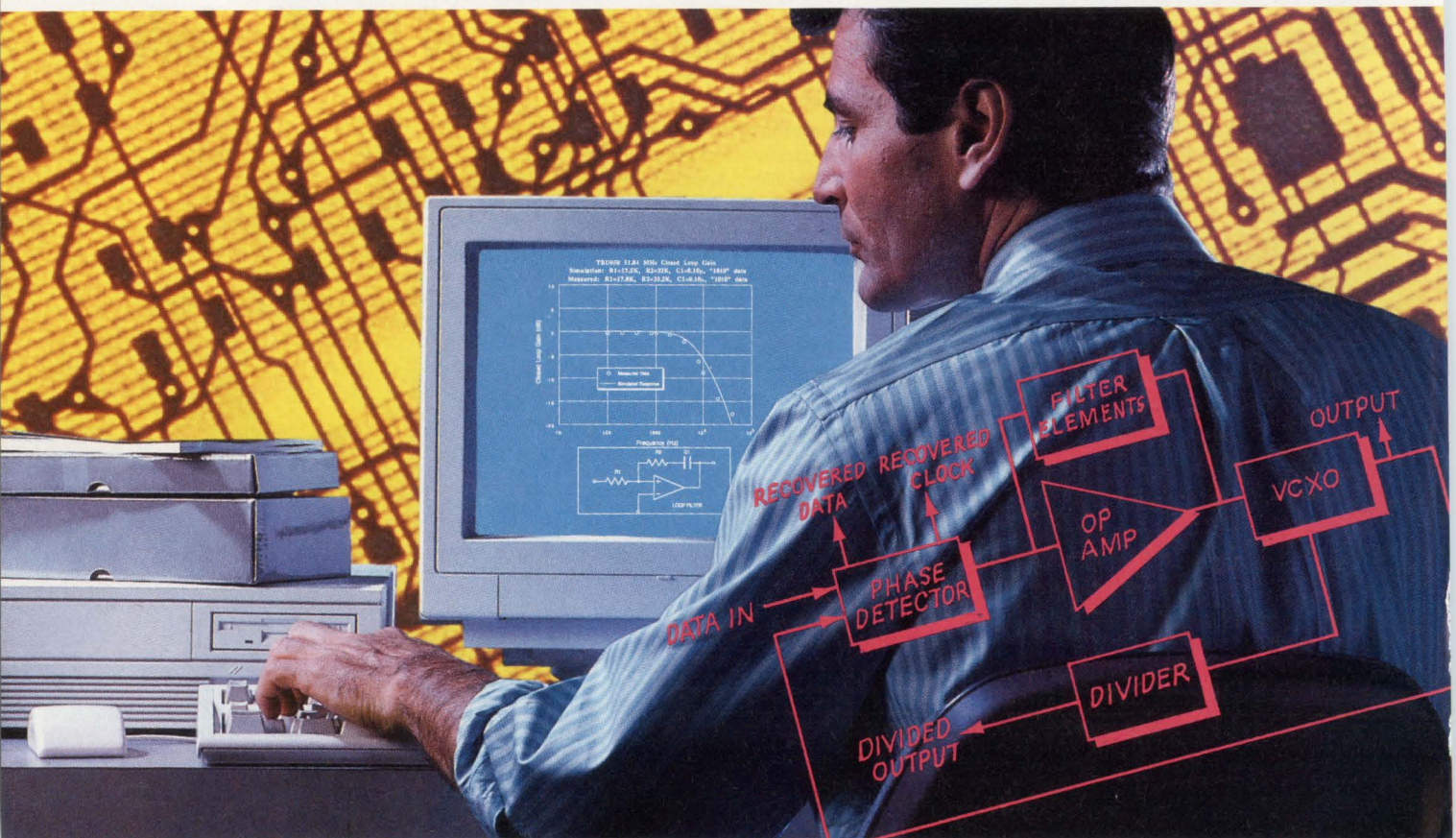
64-kword-deep cache data RAM, is putting the finishing touches on its 1-Mbit MCM6299x series. Included in the series are three biCMOS chips that can access data in just 12 ns. The synchronous 62990 (with input registers and output data latches), and the asynchronous 995 and 996 (with input latches) are all offshoots of the same chip. They contain separately-bused I/O buffers that permit the chip data buses to tie into 3.3-V system buses, while the rest of the chip runs from a 5-V power supply. With just two chips, a 256-kbyte secondary cache for the 80486 microprocessor can be implemented.

Latched cache RAMs are also readily available from such companies as Austek, Intel, Sony, and several others that sell secondary cache components into the personal-computer market to mate with chips like Intel's 82385 cache controller. Typical of such chips is the Sony

CXK7701J, which is organized as either an 8-kword-by-16-bit memory or a 4-kword-by-16-bit by 2-way set-associative memory. The shortest standard access time for the chip runs 30 ns, but a special fast-output-enable mode trims the access time to just 10 ns. Intel has also created several high-integration cache subsystems that not only incorporate the cache control logic, but the cache memory as well. By closely integrating the cache and the controller, Intel designers can get system-level performance equivalent to large caches (64 kbytes) from relatively small caches (16 kbytes).

Several other companies have a number of wide-word data SRAMs as well. Cypress Semiconductor, for example, has a CMOS 16-k-by-16 chip called the CY7C157A, which can be accessed in just 18 ns. The memory, optimized for use with RISC processors like the Sparc, includes data-in-

## Designing a "drop-in & power-up"





## FAST AND WIDE STATIC RAMS

put and data-output latches as well as the self-timed write to minimize the effect of signal skews. Internally, the RAM is organized as two banks of 16 kbytes, each with their own self-timed control block. The chip is now alternate-sourced by several companies—Integrated Device Technology is probably the most widely acknowledged alternate supplier. Both AT&T Microelectronics and Micron Technology also expect to produce similar chips sometime later this year.

Micron plans to have both 16-bit-wide (the 58C1616) and 18-bit-wide (the 1618) versions of the synchronous 16-kword memories. Initial speed grades will include 15-, 17-, 20-, and 25-ns versions. By the end of the year, the company also expects to have a 13-ns version. For portable systems, the company intends to offer 3.3-V versions of the same memories. The chips will come in 20- or 35-

ns grades and consume just 100 mA maximum, and just 3 mA on standby. In addition, latched (asynchronous) versions of the same chips will come in 16-k-by-16 and -by-18 organizations (the MT5C2516 and 2818, respectively). The chips will have the same speed grades and will also be available later this year in 3.3-V-supply options.

Latched and registered versions of 16- or 18-bit-wide megabit SRAMs are available from a number of companies—Electronic Designs, Integrated Device Technology, and several others. The shared I/O bus versions are typically housed in 52-lead PLCCs; a few suppliers are also looking at PQFP-housed versions. One typical offering is the LH21028 from Sharp, a 64-k-by-18-bit chip with access times as short as 20 ns. Transparent address latches on the address bus reduce bus loading and improve system performance. When

the latches are used, they allow the SRAM to hold the internal address constant while permitting the external address to change in preparation for the next access, thus speeding up the system. Although the chip is designed for operation at 5 V, it has a low-voltage (2-V) data-retention mode that permits battery backup for short duration power failures.

At the megabit level, Micron also expects to release both synchronous and asynchronous versions (MT58C1289 and 1189, respectively) of its 128-kword-by-9-bit SRAM in 16.6- and 20-ns speed grades. These chips were designed to initially support large caches for Sparc-based systems, and consume about 800 mW when accessed every 20 ns. On standby, the power drops to 300 mW.

A specialized cache-memory chip, the MS443 from Mosel, employs a dual-port architecture and contains special data-path registers that hold

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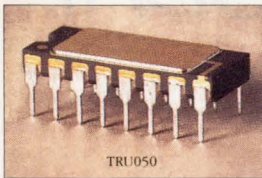
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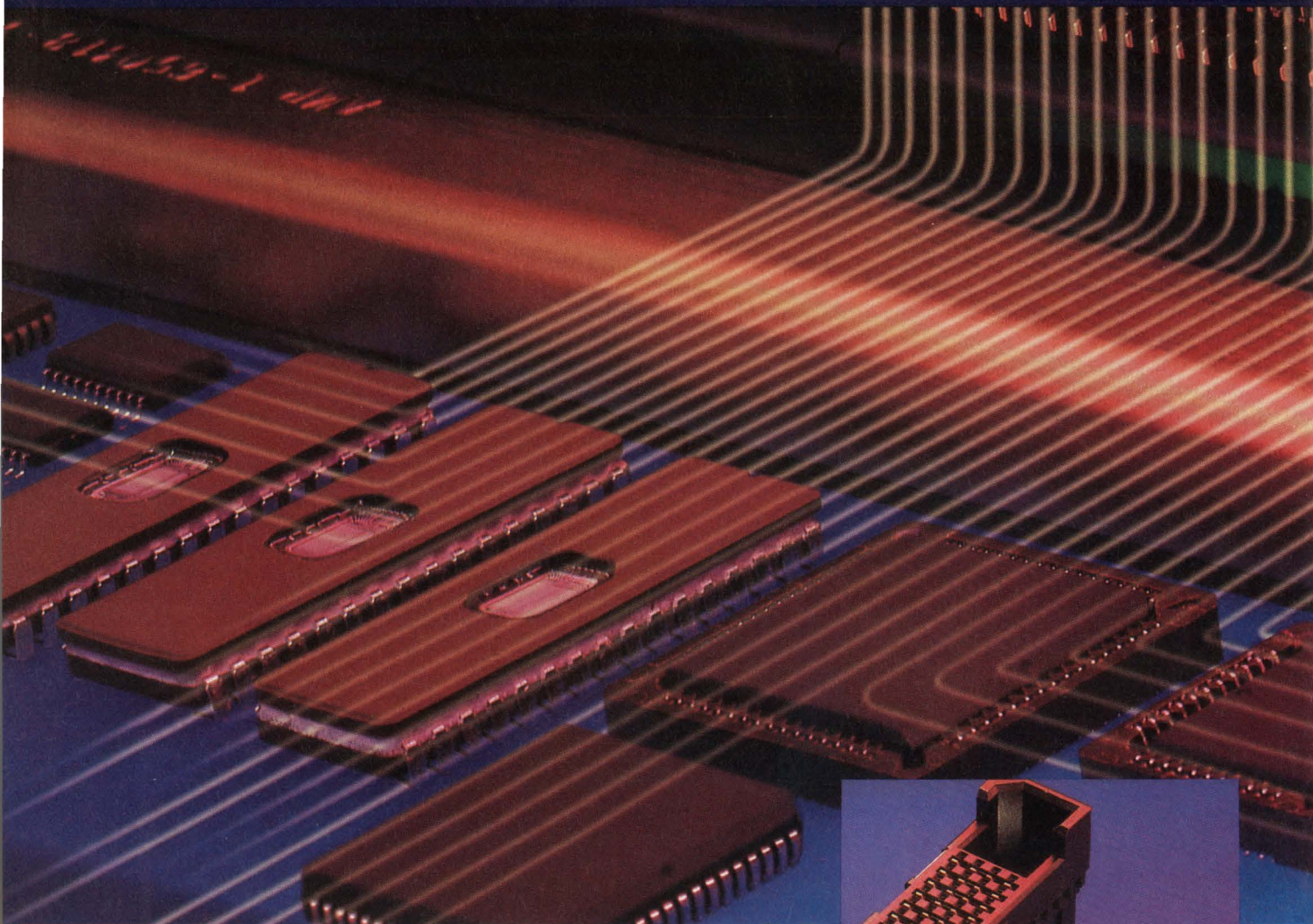
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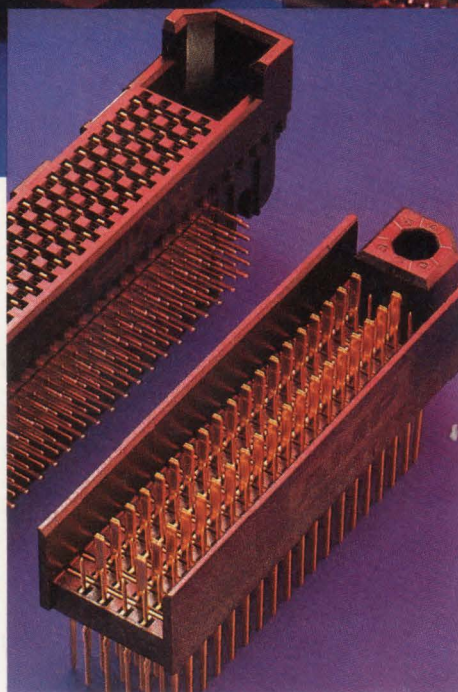
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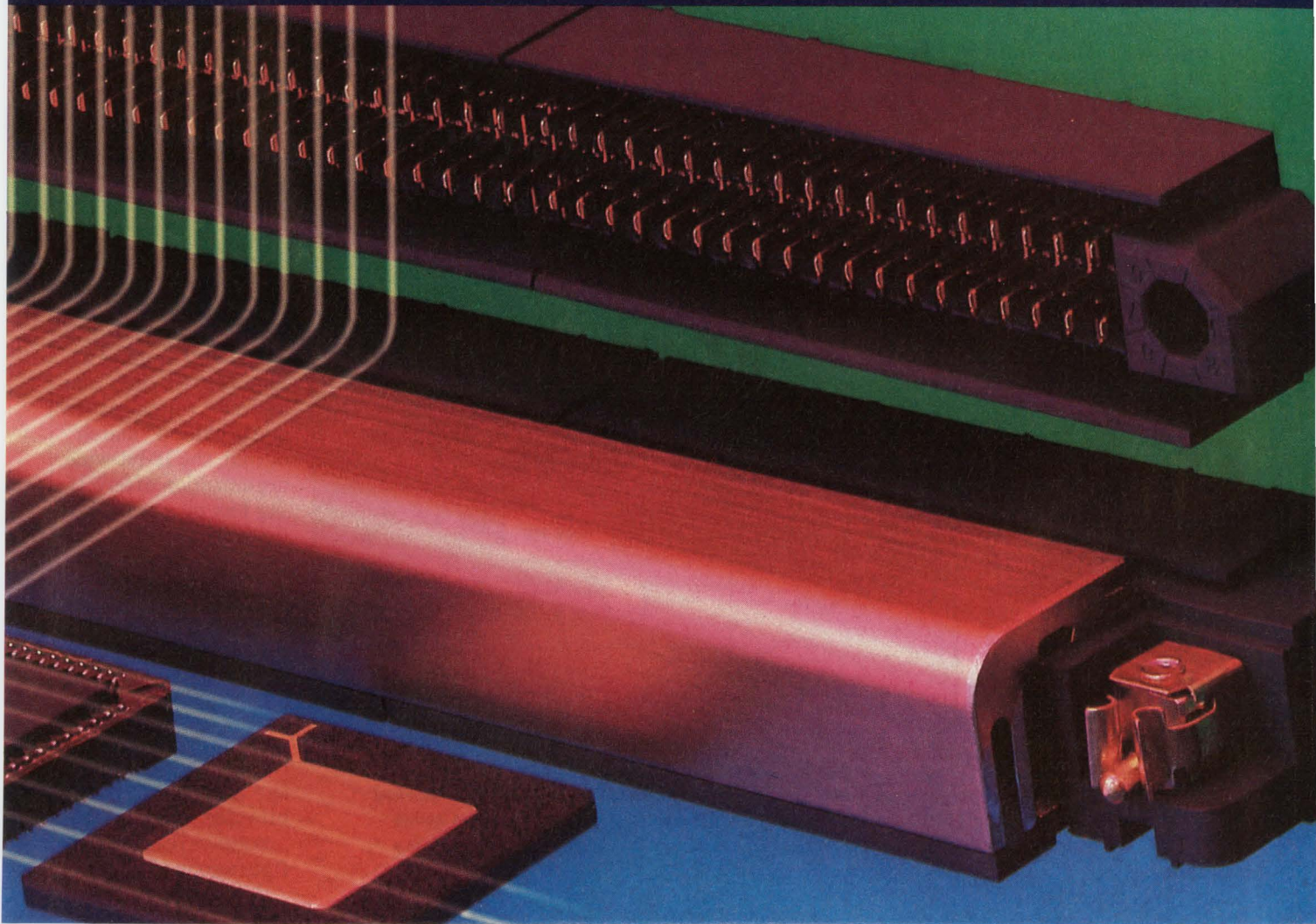


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## FAST AND WIDE STATIC RAMS

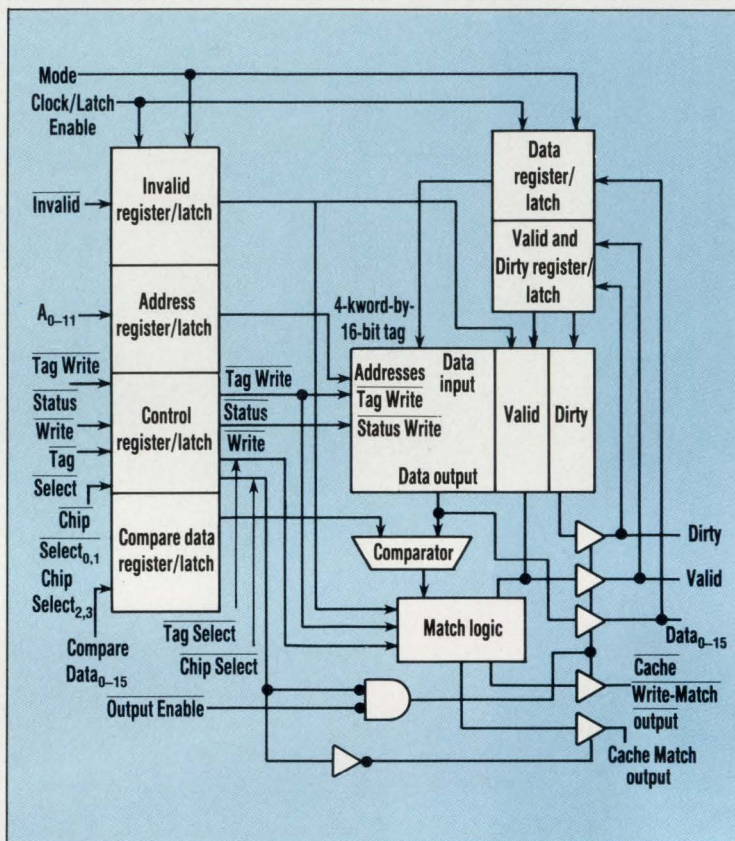
hit and miss addresses, and read and write registers that hold data (ELECTRONIC DESIGN, Apr. 25, 1991, p. 115). The RAM has two banks of memory cells, each organized as four planes, with each plane retaining 2-kwords-by-9-bits. That gives the chip a total capacity of 144 kbits, including parity bits. Data can be loaded or read with standard address-access modes. When trying to quickly transfer data during a cache update, the memories can be switched to their "turbo" mode, which allows burst data transfers at up to 256 Mbytes/s.

The SRAM contains an internal 32-bit data bus, so four RAM chips can be cascaded to form a 64-kbyte cache with a 128-bit line width. The cache SRAM can simultaneously latch up to 16 bytes in a single clock.

On-chip data-path registers channel data into, out of, and around the memory array in single-clock increments. Beyond serving as a cache, the chip has a bypass mode that enables fast data to stream directly between the system port and the CPU port of the MS443, while imposing only a 5-ns delay on the data. That mode is particularly useful when a Read-Miss occurs. Furthermore, with the memory chip's internal pipeline, self-timed write operations can be implemented to make the most of available timing overlaps.

## WIDE BUS

The static RAM with the widest data bus has just been released by a newcomer to the SRAM market, Silicon Design Technology. The chip, which was jointly designed by SDT and Electronic Designs Inc., will also



**6. THE ONLY 32-BIT-WIDE** static RAM, a 32-kword-by-32-bit chip developed by Silicon Design Technology and Electronic Designs, is structured as two 16-bit-wide memory banks controlled by byte-decoding logic that permits byte-write operations. Transparent address latches allow the chip to readily tie into most 32-bit processors and serve as a single-chip data-cache solution.

be sold by EDI. The asynchronous 1-Mbit device is organized as 32 kwords by 32 bits and will be available in access times ranging from as little as 12 ns to 20 ns for the slowest grade. It's designed for either 5- or 3-V operation, and includes input address latches as well as individual byte-select lines that function in either the read or write mode (Fig. 5). In addition, SDT plans to offer both a 36-bit-wide version for systems that require parity, and narrower-word memories—all the way down to single-bit wide architectures.

The cache-data SRAMs support the cache-tag memories. The tag RAMs must be exceptionally fast because their access time is the major component in determining the speed of an address match in the cache. The most highly integrated cache-tag memory is the just-released

CY7B180 and 181 from Cypress Semiconductor. Organized as 4 kwords by 18 bits, the biCMOS memories can perform an address match in just 12 ns, or access the tag RAM in 15 ns (see "Highly integrated cache-tag RAMs perform matches in 12 ns," p. 114).

Unlike most other cache-tag memories that contain just the address comparators and provide a "match" output, the 18-bit-wide organization offers 16 tag bits plus two additional bits. These bits can be user-defined (as in the 7B180) to handle the MESI (modified, exclusive, shared, invalid) protocol in multiprocessor configurations. Or they come preassigned (as is the case in the 7B181) as the Valid and Dirty bits for use in uniprocessor cache configurations (Fig. 6).

An even wider 20-bit cache-tag chip, the MK4202 developed by SGS-Thomson, comes in speed grades of 20, 22, and 25 ns (match access time), which would suit the chip to some of the same systems as the Cypress chips. The 20-bit-wide offering, though, is only half as deep, with a depth of just 2 kwords. The chip does, however, offer a flash-clear capability that permits the memory's entire contents to be invalidated in one cycle. The chip can be tied directly into processors like the Motorola 68030 and 040, as well as CPUs like the Intel 80386.

Another biCMOS cache-tag RAM comes from Texas Instruments. Although they're not wide-word memories (9 bits or wider), they're worthy of note because some of them employ a 5-bit-wide architecture. The company just released a series of five devices that all offer address-to-



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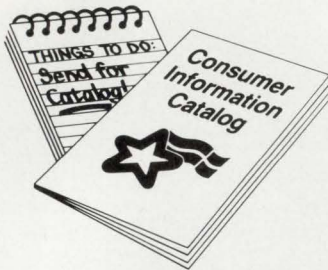
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## FAST AND WIDE STATIC RAMS

match times of 12 ns, which suits them for systems running at up to 50 MHz. Self-timed writes and word widths of 4 or 5 bits let these chips serve as building blocks for custom-configured caches. Two of the chips are 2-way, 8-kword-by-4-bit open-drain devices with or without latches (the SN74BCT2160 and 2165, respectively). The three others are 16-kword-by-5-bit devices that have to-

tem-pole or open-drain outputs. One of the previously mentioned -by-5 open-drain RAMs includes latches (the three chips are the 2163, 64, and 66, respectively). □

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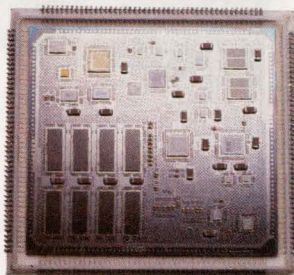
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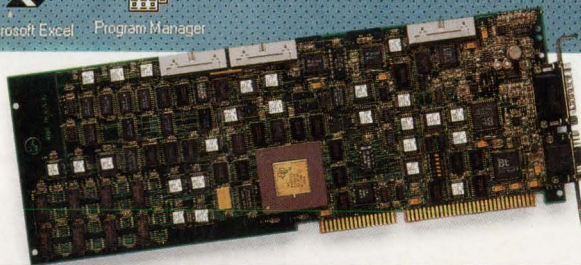
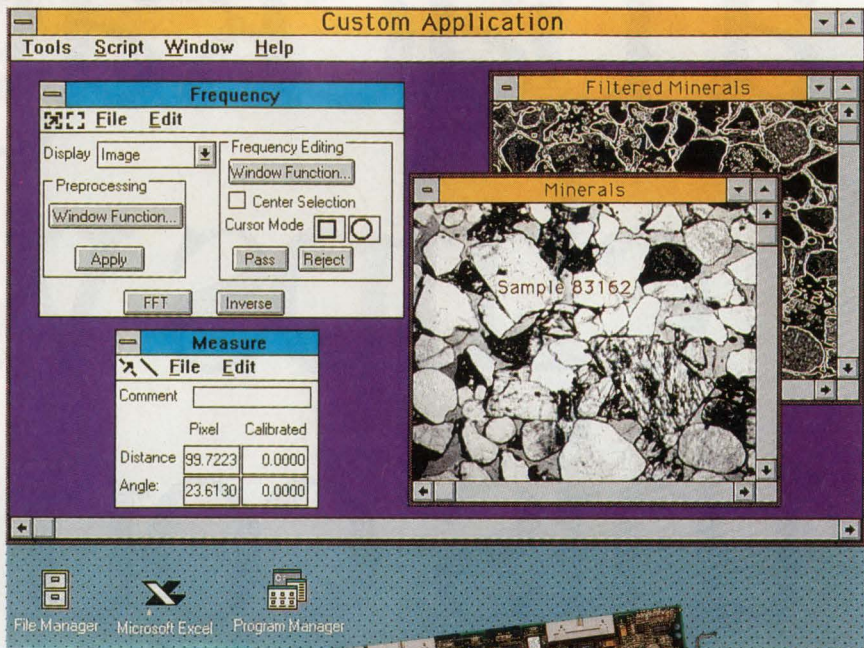
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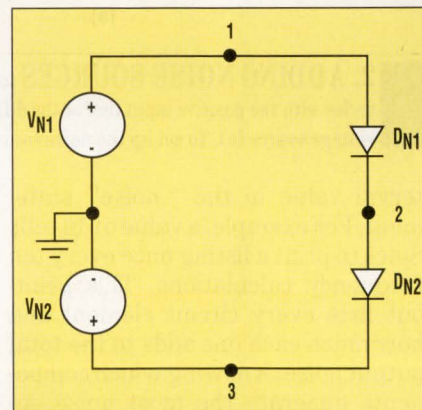
oise in operational amplifiers has never been easy to model and project, whether it's done with software packages like Spice or with pencil and paper. Determining the spectral and total noise over a given bandwidth is a daunting and tedious task, and it requires that all noise sources—resistors, amplifiers, etc.—be considered. Although Spice programs have noise analysis capabilities, previously available op-amp macromodels, including the Boyle model, lack noise parameters.

Because the internal impedances of typical macromodels don't exactly match those of the actual device, using the models for noise analysis often results in gross errors. To address this problem, a new modeling technique that incorporates accurate voltage and current noise sources, originally developed at the Precision Monolithics Div. of Analog Devices Inc. (ADI), allows designers to do full noise analysis on a system level.

The usefulness of simulating noise with a Spice program can be appreciated by any engineer who has gone through the calculations by hand. A hand analysis requires calculating the individual noise contribution of each op amp, resistor, and any other active device. Then, all of the contributions must be summed together by a root-sum-square, with that sum multiplied by the square root of the circuit's bandwidth.<sup>1</sup>

For lower-frequency circuits, the amplifier's 1/f noise becomes significant, so the 1/f noise must be integrated into the total. In more complex circuits with multiple stages and many resistors and capacitors, the task seems to grow exponentially. Luckily, Spice can do all of the work—given an accurate op-amp model.

Spice can also analyze the noise contributions of each circuit element to determine the dominant sources. A detailed listing is generated in the Spice ".out" file by specifying an in-



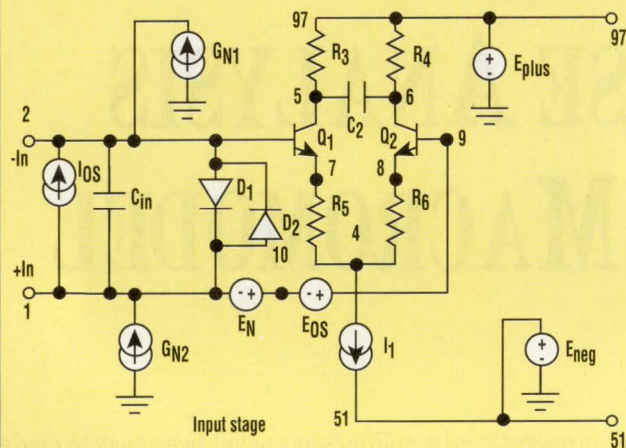
**1. A SIMPLE** noise-source model for use in Spice simulations consists of two identical series-connected voltage sources linked in parallel with a pair of series-connected diodes. The node between the voltage sources is grounded, while the noise output is taken from the node between the two diodes.

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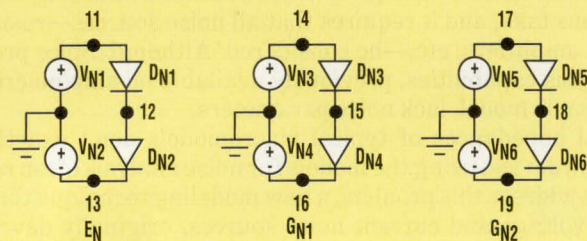
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R4	6	97	0.0619				
C1N	1	2	4E-12				
C2	5	6	16.07E-9				
I1	4	51	1				
IOS	1	2	3.5E-9				
EOS	9	10	POLY(1)	30	33	10E-6	1
Q1	5	2	7	QX			
Q2	6	9	8	QX			
R5	7	4	0.0107				
R6	8	4	0.0107				
D1	2	1	DX				
D2	1	2	DX				
EN	10	1	12	0	1		
GN1	0	2	15	0	1		
GN2	0	1	18	0	1		
EREF	98	0	33	0	1		
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ENEG	51	0	50	0	1		

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DN1	11	12	DEN
DN2	12	13	DEN
VN1	11	0	DC 2
VN2	0	13	DC 2

\* CURRENT NOISE SOURCE WITH FLICKER NOISE

DN3	14	15	DIN
DN4	15	16	DIN
VN3	14	0	DC 2
VN4	0	16	DC 2

\* SECOND CURRENT NOISE SOURCE WITH FLICKER NOISE

DN5	17	18	DIN
DN6	18	19	DIN
VN5	17	0	DC 2
VN6	0	19	DC 2

(b)

**2. ADDING NOISE SOURCES** to the input of the op-amp macromodel is straightforward. The voltage noise source is connected in series with the positive input line of the differential pair, while the two current noise sources are connected to the input pins preceding the voltage source (a). To set up the noise sources as part of the Spice net list is a simple matter of inserting the definitions into the listing (b).

interval value in the ".noise" statement. For example, a value of 10 tells Spice to print a listing once every ten frequency calculations. This print-out lists every circuit element and how much each one adds to the total output noise. Knowing which components generate the most noise enables a designer to more easily optimize his system.

In the interest of increasing simulation speed and simplifying development, Spice macromodels rely on ideal voltage- and current-controlled sources with resistors, capacitors, and a limited number of transistors and diodes. As a result, the internal

schematic representation of a macromodel has very little similarity to the actual op amp's circuitry. This modeling approach can give accurate results for dc, ac, and transient simulations. However, unless noise is specifically taken into consideration when developing the model, trying to simulate for it will give erroneous results.

For example, if the macromodel has large internal resistors that don't correspond to elements in the actual circuit, those resistors can generate excessive noise during a simulation. Unfortunately, Spice doesn't allow users to make specific

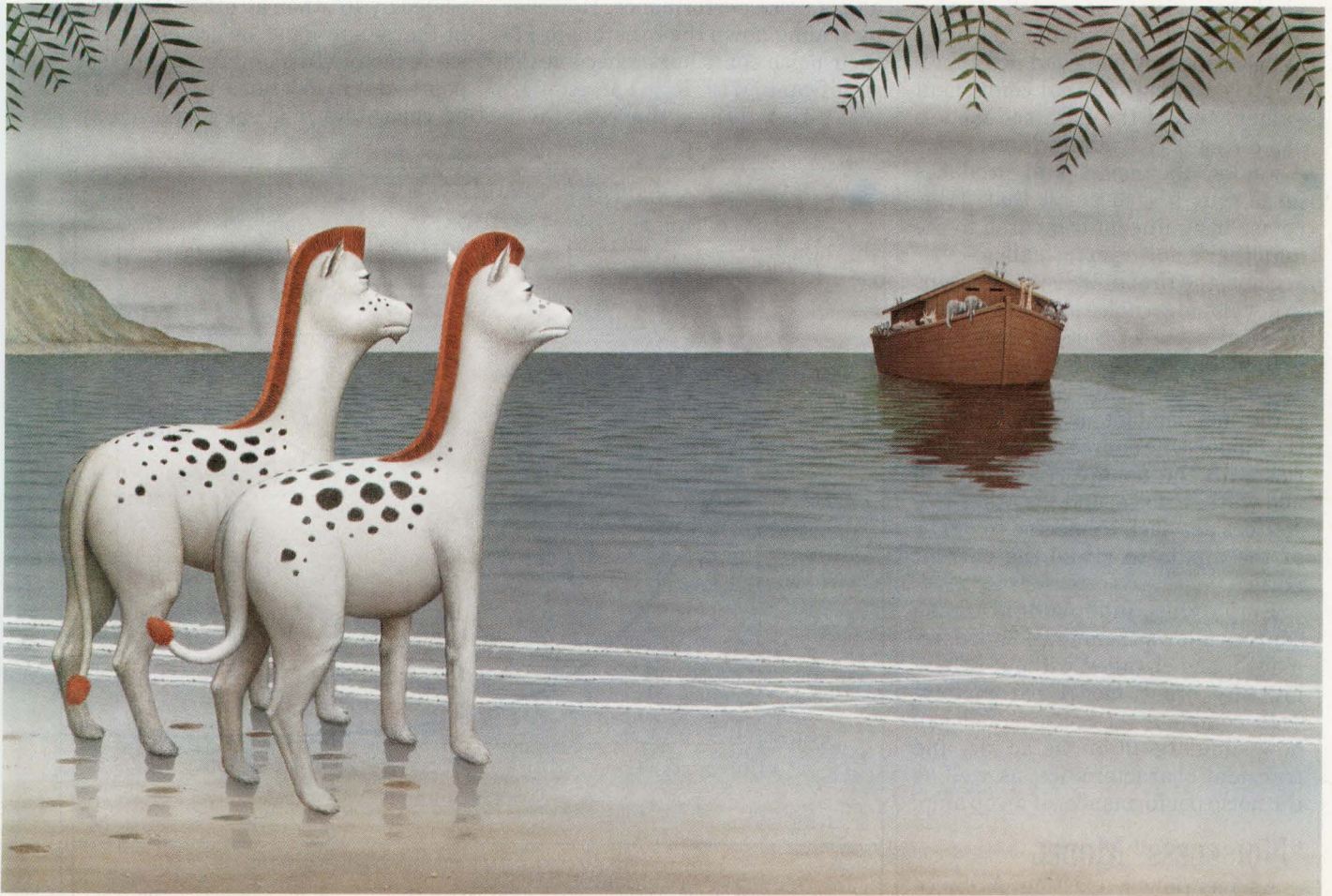
resistors or any other other devices noiseless. Rather, when Spice performs a noise analysis, it calculates the noise generated by all resistors and active semiconductor devices without exception.

An improved model (referred to as the ADSpice model) with an open architecture allows for very accurate performance simulations under ac, dc, and transient simulations.<sup>2</sup> However, when a noise analysis is performed using this model, the results can easily be over 100 times greater than that of the actual device.

Fortunately, the same feature of macromodelling that allows the de-



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# MODELLING OP-AMP NOISE

vice's behavior to be modelled using ideal elements also enables the noise to be accurately modelled. By appropriately scaling internal component values, any of the ADSPICE models can be made essentially "noiseless." Actually, the model still produces noise, but it's so small that it becomes insignificant compared to the amplifier's noise performance.

Thus, the first of three major steps in developing a noise model is to modify an existing ADSPICE op-amp model to make it noiseless. The next two steps are to create and then add three independent noise sources to the model. One source is placed in series with the noninverting input to add voltage noise, and the other two sources are each connected to either of the inputs to model the current noise.

Employing independent noise sources allows them to be added, removed, and changed without affecting any other model parameters. This complete ADSPICE model can now simulate all of the ac, dc, and transient characteristics, as well as the noise performance, of an op amp.

## "NOISELESS" MODEL

As mentioned, existing ADSPICE macromodels generate too much noise due to unrealistic values for internal resistances and transistors. Thus, to reduce the noise to insignificant levels is basically an exercise in scaling.

For example, in the existing model, the pole and zero stages use 1-M $\Omega$  resistors in combination with capacitors or inductors to set the frequency. Each resistor produces 128 nV/ $\sqrt{\text{Hz}}$  of noise, which is calculated using the standard equation for thermal noise:

$$e_n = \sqrt{4kTR} \quad (1)$$

where:

$e_n$  = voltage noise in V/ $\sqrt{\text{Hz}}$

$k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  joules/K

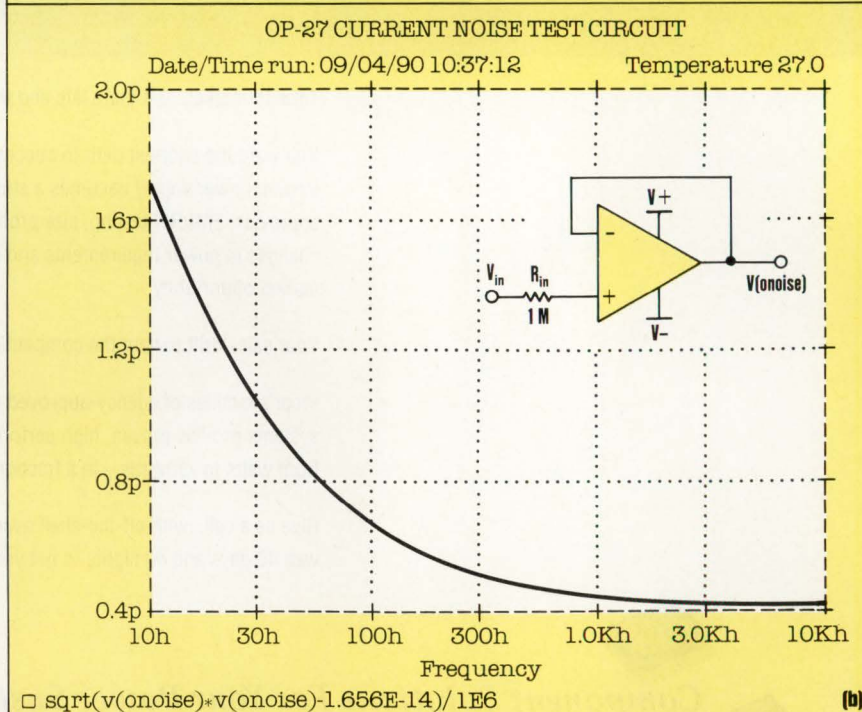
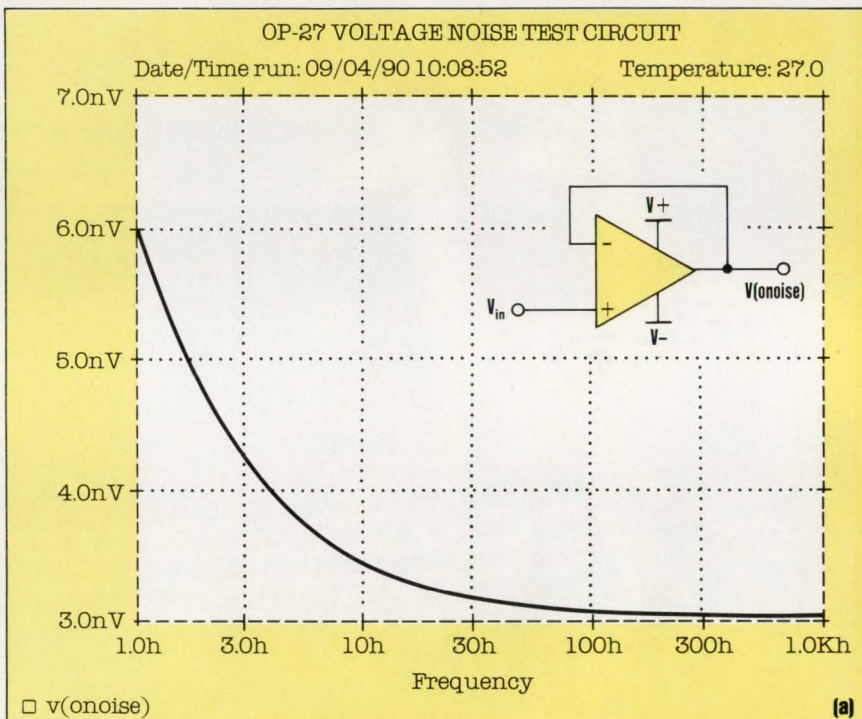
$T$  = absolute temperature in Kelvin (K)

$R$  = resistance in ohms

The 128 nV/ $\sqrt{\text{Hz}}$  is already a factor of ten larger than a typical op

amp's noise performance. However, by scaling down the resistors to 1  $\Omega$ , their noise contribution becomes insignificant (With  $R = 1 \Omega$ ,  $e_n = 128 \text{ pV}/\sqrt{\text{Hz}}$ ). When the resistor is

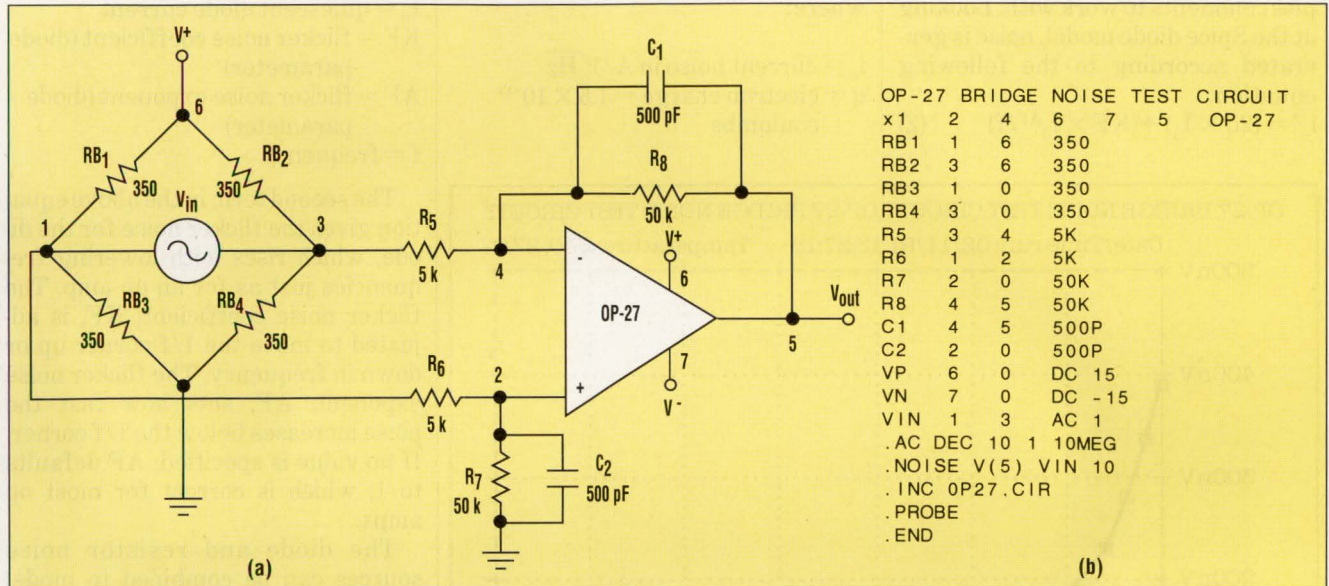
scaled by  $10^6$ , then all other elements in that stage must be scaled by the same factor. To maintain the correct pole and zero locations, any associated capacitors must be increased by



**3. SIMULATING THE MACROMODEL'S** voltage noise density vs. frequency results in a curve that closely matches an actual OP-27's response (a). A current-noise simulation also produces a curve that matches the performance of an actual device (b).



## MODELLING OP-AMP NOISE



**4. THIS BRIDGE CIRCUIT** illustrates how total system noise can be analyzed using ADSpice model of the OP-27 (a). The circuit is characterized with a simple net list that includes the op-amp macromodel (b).

the same factor, and any inductors or resistors must be decreased by the same factor. Also, the voltage-controlled current sources that set the stage's gain must be increased by the same factor.

In addition, the input stage must be altered to lower the noise. A transistor's voltage noise is inversely proportional to its collector current, so by increasing the collector current the noise becomes insignificant. A current of 1 A works in most cases. Again, other elements in the stage must be scaled by the same amount to maintain the original ac and dc characteristics.

The final change in the model requires the removal of two differential resistors connected in series across the inputs. Typically, the common-mode rejection ratio (CMRR) is multiplied by the voltage at the node between these resistors. Unfortunately, these resistors add excessive noise at higher frequencies as the CMRR decreases. Merely reducing the size of these resistors would make the input impedance unacceptably low, so they must be removed completely.

Sensing the common-mode voltage now requires sensing each input and averaging the two voltages. Spice can easily do this by using a

voltage-controlled source with two controlling variables. That results in the following equation:

$$\text{Common-mode error} = (\text{CMRR}/2)(\text{VIN}+) + (\text{CMRR}/2)(\text{VIN}-)$$

Through these adjustments, an ADSpice model can be made "noiseless." As an example, simulating the OP-27 model without the added noise sources results in a voltage noise of 140 pV/ $\sqrt{\text{Hz}}$ , which is much lower than the device's performance of 3 nV/ $\sqrt{\text{Hz}}$ .

### SIDE EFFECTS

One side effect of lowering the model's internal resistances is a dramatic increase in the amount of simulated quiescent supply current. This problem can be overcome by connecting false supplies to the high-current stages and connecting the actual supplies to the output stage only.

The false supplies are voltage-controlled voltage sources that mirror the supply voltages. Doing this maintains the correct current in the external voltage supplies.

However, the model now internally dissipates very large amounts of power, which is reflected in the total power dissipation specification printed at the end of a Spice output file.

Thus, when simulations are run using the noise model, the power dissipation of the actual power supplies should be carefully looked at by checking their individual currents.

Now that the ADSpice model is "noiseless," independent noise sources must be created and added to the model. Amplifiers contain current and voltage noise, and each type of noise is comprised of broadband or thermal noise and flicker or 1/f noise. Spice can model both types of noise.

Broadband noise is most easily modelled with a resistor; 1/f noise uses a diode. Thus, a noise source could be simply a resistor in series with a diode. A few details must still be considered, but this is basically how a noise source can be created for Spice modeling.

Setting the broadband noise requires that the proper resistor value be calculated. Spice uses Equation 1 to determine a resistor's thermal noise in all of its calculations. To set the broadband noise, the value for  $e_n$  from the data sheet should be used to solve for  $R$ . For example, to get  $e_n = 4 \text{ nV}/\sqrt{\text{Hz}}$ , the equation yields  $R = 1 \text{ k}\Omega$ .

Flicker (1/f) noise is also built into Spice in every semiconductor element, of which diodes are the sim-



# MODELLING OP-AMP NOISE

plest elements to work with. Looking at the Spice diode model, noise is generated according to the following equation:

$$i_n^2 = (2q \times I_d) + (KF \times I_d^{AF}/f) \quad (2)$$

where:

$i_n$  = current noise in  $A/\sqrt{Hz}$   
 $q$  = electron charge =  $1.6 \times 10^{-19}$  coulombs

$I_d$  = quiescent diode current  
 $KF$  = flicker noise coefficient (diode parameter)  
 $AF$  = flicker noise exponent (diode parameter)  
 $f$  = frequency

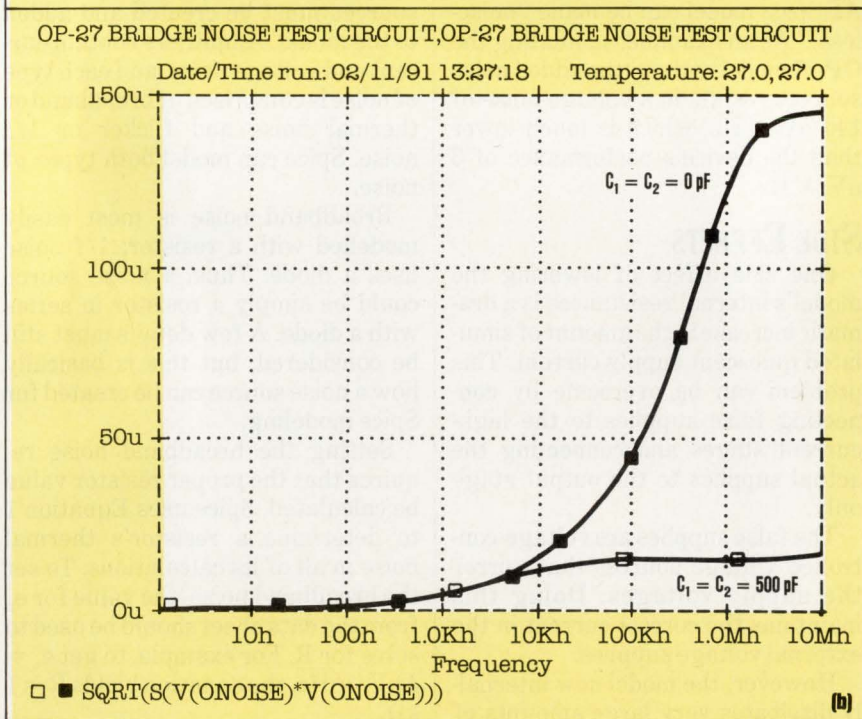
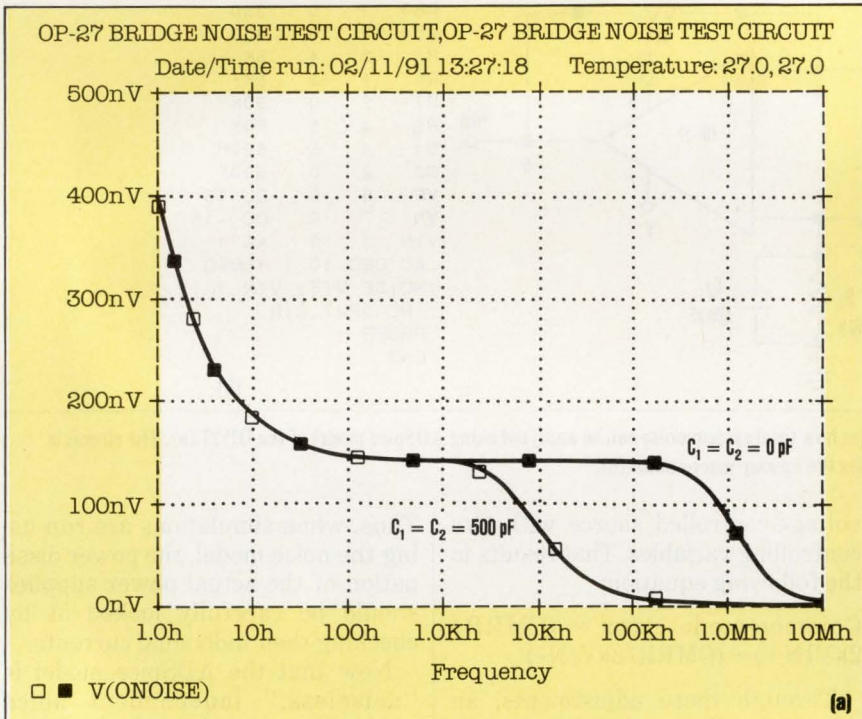
The second term in the above equation gives the flicker noise for the diode, which rises with lowering frequencies just as for an op amp. The flicker noise coefficient,  $KF$ , is adjusted to move the  $1/f$  corner up or down in frequency. The flicker noise exponent,  $AF$ , sets how fast the noise increases below the  $1/f$  corner. If no value is specified,  $AF$  defaults to 1, which is correct for most op amps.

The diode and resistor noise sources can be combined to model any op-amp noise source with broadband and  $1/f$  noise. The diode model actually includes a parasitic resistance,  $RS$ , whose value defaults to 0. To save a node and time during a Spice analysis, the resistor that generates broadband noise is included as  $RS$ .

The actual topology of a noise generator consists of two series-connected voltage sources connected in parallel with two series-connected diodes (Fig. 1). Generated noise is measured at the junction between the two diodes (node 2). By centering the source around ground, the dc bias on node 2 is eliminated, preventing the amplifier's offset from being affected. To guarantee that node 2 is exactly 0 V dc, the two voltage sources  $V_{N1}$  and  $V_{N2}$  must be identical, and the two diodes  $D_{N1}$  and  $D_{N2}$  must be also identical.

A side effect of having the two diodes in series is that any noise generated by one is actually divided in half by the resistive divider formed by the two devices in series. For example, if  $RS = 1 \text{ k}\Omega$ , it generates  $4 \text{ nV}/\sqrt{Hz}$  of noise, but its contribution to node 2 is only  $2 \text{ nV}/\sqrt{Hz}$ . However, because noise adds by root-mean-square, the two resistors' contributions must also be added using the rms formula. That results in the following equation for total broadband noise:

$$E_N^2 = (e_{nRS1}/2)^2 + (e_{nRS2}/2)^2$$



**5. PLOTTING THE BRIDGE CIRCUIT'S** noise as a function of frequency shows the effect of the two band-limiting capacitors (a). A more useful plot depicts total system noise integrated over the entire bandwidth (b).



## MODELLING OP-AMP NOISE

since  $e_{nRS1} = e_{nRS2}$  then

$$E_N = e_{nRS} / \sqrt{2}$$

$$\text{where } e_{nRS} = \sqrt{4kTRS}$$

Note:  $e$  represents the noise contribution from a single source and  $E$  represents the aggregate noise.

The flicker-noise calculation is more involved because it's based on the quiescent diode current,  $I_d$ , which is unknown. To actually solve for  $I_d$  would require numerical iteration or inaccurate graphical methods. Spice will do all of the work, though.

The noise-generator circuit should be run in Spice with the calculated value for  $RS$  in the diode model. Then, the dc bias solution in the ".out" file will show the current through the voltage sources, which is equivalent to  $I_d$ .

Once  $I_d$  is known, the current noise is calculated using Equation 2. Any current noise is converted into voltage noise by the impedance seen by the source. In this case, Spice places the current-noise source in parallel with the conductance,  $g_D$ , of the diode. This, according to the small signal equivalent circuit, is equal to:

$$g_D = I_d / V_T$$

where:  $V_T$  = thermal voltage = 25.8 mV at 27°C

Any current noise is multiplied by one over the conductance to create voltage noise. Therefore, to generate the voltage flicker noise ( $e_{fnD1}$ ) of the diode, the equation becomes:

$$e_{fnD1}^2 = (i_n^2) (1/g_D)^2$$

$$e_{fnD1}^2 = (KF \times I_d^{AF}/f) (1/g_D)^2$$

And to get the total flicker noise:

$$E_{FN}^2 = (e_{fnD1}/2)^2 + (e_{fnD2}/2)^2$$

$$E_{FN} = e_{fnD} / \sqrt{2}$$

The factor of one-half comes from the resistive divider of the two diodes, which divides the rms noise in half. The  $2qI_d$  term of the diode noise is ignored because it's insignificant compared to the thermal noise generated by the resistors. When calculating the 1/f noise, the broadband

noise must be rms-subtracted from the noise figure before calculating KF. For example, the OP-27 has broadband voltage noise equal to 3 nV/ $\sqrt{\text{Hz}}$  and 1/f noise at 1 Hz equal to 6 nV/ $\sqrt{\text{Hz}}$ . Thus, to calculate for KF in the above equation,  $E_{FN}$  should equal 5.2 nV/ $\sqrt{\text{Hz}}$ .

This noise generator topology can be used for both voltage and current noise. The determining factor is whether a voltage-controlled voltage source or a voltage-controlled current source introduces the noise into the input stage.

### ADDING THE NOISE IN

Up to this point, the noise sources have not yet been connected to the ADSpice model. To connect them is actually a simple task. First, the voltage-controlled sources must be placed in the input stage (Fig. 2a). For voltage noise, a voltage-controlled voltage source,  $E_N$ , is inserted in series with the positive input pin.  $E_N$  is controlled by the center node of the noise generator, and for convenience,  $E_N$ 's gain is set to 1. Consequently, to get a input voltage noise of 3 nV/ $\sqrt{\text{Hz}}$ , the noise generator must be set to 3 nV/ $\sqrt{\text{Hz}}$ . The Spice net list for the circuit probably illustrates most accurately how the noise elements are tied into the rest of the model (Fig. 2b).

Adding current noise sources is similar except that voltage-controlled current sources are used. The current noise sources ( $G_{N1}$  and  $G_{N2}$ ) are connected to each input and again have a gain of 1.

Now, however, instead of producing voltage noise, they produce current noise of the same magnitude as the noise generator. For example, to get 5 pA/ $\sqrt{\text{Hz}}$  of current noise, the noise generator must produce 5 pV/ $\sqrt{\text{Hz}}$ .

Three separate noise generators are needed rather than just using two—one for the voltage noise and one for each current noise sources. Using the same generator for both current-noise sources reduces the effective noise by as much as 30% due to the op amp's high common-mode rejection.

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## MODELLING OP-AMP NOISE

ration of the OP-27 model, the accuracy of the model's noise voltage can be checked easily (*Fig. 3a*). Because the model provides a gain of +1, the output noise is equal to the input noise.

Furthermore, since there is no source impedance, the current noise is effectively zero. The results of the simulation, when compared with the response of an actual OP-27, show the accurate modelling of the noise over the entire frequency range from 1 Hz to 1 kHz.

By adding a large source impedance on the  $V_{in}$  line, the unity-gain amplifier can be used to test current noise (*Fig. 3b*). Any input current noise will be multiplied by the source resistor, resulting in voltage noise. Spice gives the total output voltage noise from all sources.

So, when this circuit is used, the noise of the 1-M $\Omega$  source-impedance resistor should be rms-subtracted

from the results. Finally, the result must be divided by the value of the source resistor to get the current noise. The equation at the bottom of the graph charts only the current noise, which is very close to the OP-27's actual measured response.

A simple bridge circuit works well as an example of using the ADSpice model to find the total noise of a system (*Fig. 4a*). A net list can characterize the bridge amplifier (*Fig. 4b*). Capacitors  $C_1$  and  $C_2$  are used as low-pass filters to remove high-frequency noise.

This particular simulation was executed twice, the first time with the capacitors in place and then without them. The resulting plots show that the noise falls off much sooner with the capacitors in place, as is expected (*Fig. 5a*).

However, the total noise is a more meaningful result that can help gauge the system's performance.

Knowing this value and comparing it to the input level gives the signal-to-noise ratio (SNR) for the circuit. Finding the total noise requires integrating the noise over the circuit's entire frequency range. Doing so is straightforward in many Spice simulators that allow calculations to be performed on the output.

For example, MicroSim Corp.'s PSpice simulator integrates the noise using the following equation:

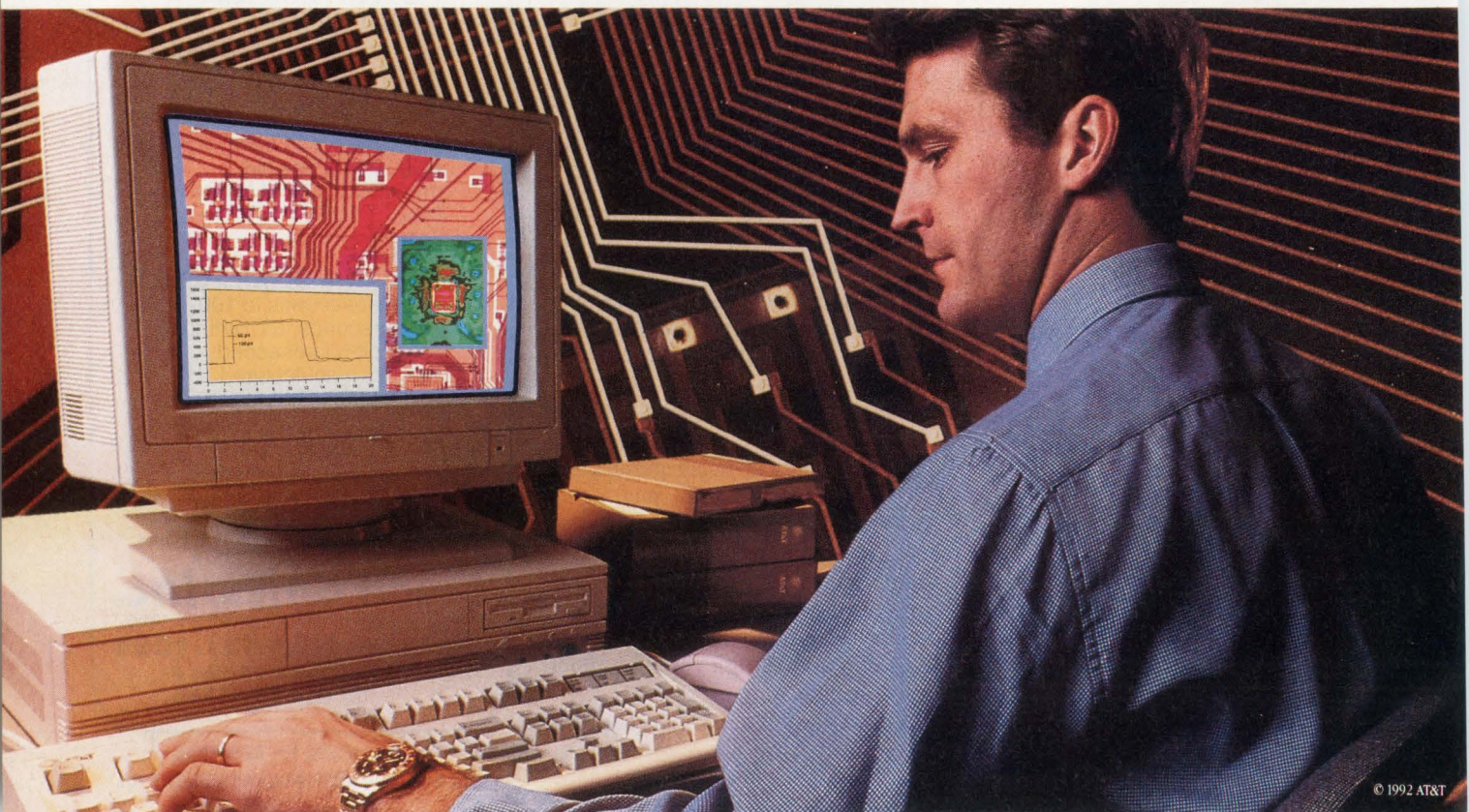
$$E_T = \text{sqrt}(s(v(\text{onoise}) * v(\text{onoise})))$$

The "s" operator integrates the square of the output noise, and then the "sqrt" operator takes the square root of the total.

This is essentially an rms sum of the noise at each frequency (*Fig. 5b*). As the graph shows, the total noise is much less when the capacitors are in place—just 15  $\mu\text{V}$  rms compared to 140  $\mu\text{V}$  rms.

The SNR can easily be calculated

## Breakthrough multichip modules





## MODELLING OP-AMP NOISE

from this graph by taking the expected signal level and dividing by the total noise from the graph. The SNR is then just  $20 \times \log$  of the result. For example, a signal level of 15 mV rms gives a SNR of 60 dB and 41 dB, respectively. The peak-to-peak noise can also be calculated by multiplying the total noise by 6.<sup>3</sup>

### BIG CONTRIBUTORS

If a listing of the computed noise at 10 iteration intervals is examined for the bridge circuit, it would reveal that the two 5-k $\Omega$  resistors contribute the most noise. Adding just their contributions together shows that they create 129 nV/ $\sqrt{\text{Hz}}$  of the total 140 nV/ $\sqrt{\text{Hz}}$  of noise.

Speed is always a concern when simulating a circuit with Spice. A model's usefulness is reduced if the simulation chews up too much time. To keep simulation time down, the ADSpice model uses ideal elements

and limits the number of nonlinear components.

Running Spice on the bridge amplifier took 15 seconds on a 33-MHz 386 PC clone and 65 seconds on a 12-MHz 286 PC. In comparison, the same simulation was done without simulating the noise, and that simulation run took 9.8 seconds on a 33-MHz PC. While the noise analysis increases the simulation time by 50%, the total time is still somewhat short.  $\square$

### References:

1. "Minimization of Noise in Operational Amplifier Applications"; AN-15, Linear and Conversion Handbook, 1986, Analog Devices-Precision Monolithics Division.
2. Complete net lists of some of the existing Spice models are given in the following ADI Application Notes: AN-110, AN-117, AN-120, AN-126, and AN-132. A complete ex-

planation of the original model is given in: AN-138, SPICE-Compatible Op Amp Macro-Models.

3. AN-15, Linear and Conversion Handbook.

*The entire ADSpice library is available on diskette and can be obtained free of charge from Analog Devices by calling the Literature Department at (617) 329-4700. Copies of the application notes referenced may also be obtained from the same source.*

*Joe Buxton, senior applications engineer for the Precision Monolithics Division of Analog Devices, received a BSEE from the University of California at Berkeley.*

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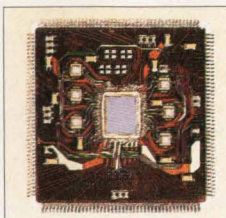
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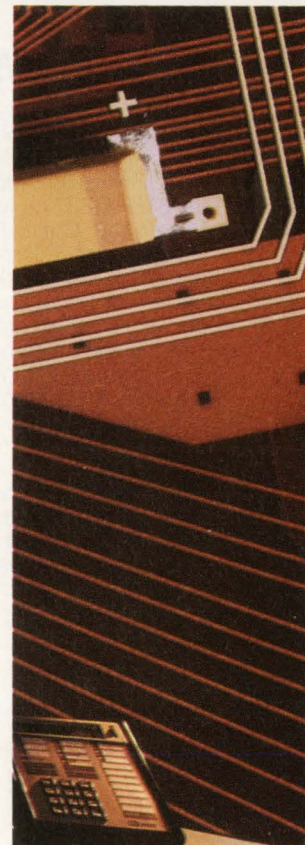
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For detailed specs and computer-automated performance data (CAPD), refer to Thomas Register Vol. 23, MicroWaves Product Directory, EEM, or Mini-Circuits' 718-pg Handbook.

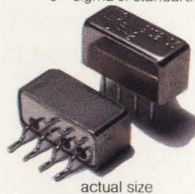
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TUF-2 TUF-2SM	50-1000	5.73	0.30	47	4.95
TUF-5 TUF-5SM	20-1500	6.58	0.40	42	8.95
TUF-860 TUF-860SM	860-1050	6.2	0.37	35	8.95
TUF-11A TUF-11ASM	1400-1900	6.83	0.30	33	14.95

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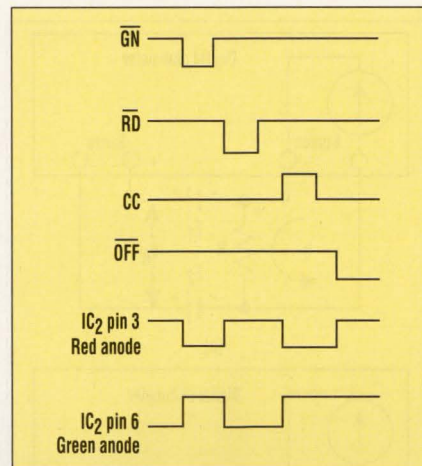
Action Manufacturing Co., 100 East Erie Ave., Philadelphia, PA 19134-1089; tel.: (215) 739-6400; fax: (215) 423-7749.

Many makers of bicolor light-emitting diodes claim a total of four states for their devices—red, green, orange, and off. Those devices actually contain just two LEDs, one red and one green, in an anti-parallel arrangement. Therefore, to make them produce an orange output requires alternating between red and green above the eye's flicker fusion frequency. How best to do that is perhaps less than self-

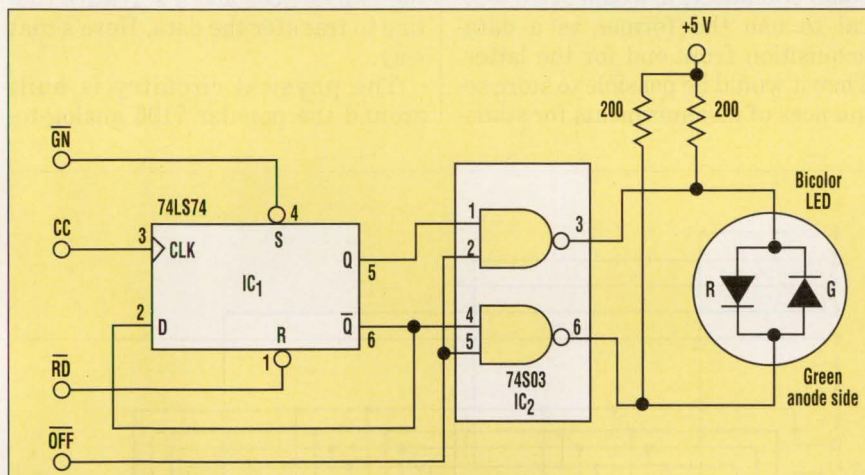
evident, and a bit more involved than driving a garden variety LED.

The simple circuit shown permits the exploitation of all four states of the bicolor LED (Fig. 1). When GN goes low, so does pin 3 on IC<sub>2</sub> (Fig. 2). That allows current to flow from the 5-V supply, through one of the 200-Ω resistors, and through the green LED, making the light green. Similarly, having RD go low makes the light red.

The positive edge of the CC



**2. THIS TIMING diagram** illustrates how the various inputs affect the two LEDs. The green LED is on when the red anode (green cathode) is low. Similarly, the RD input turns on the red LED by forcing the red cathode (pin 6 of IC<sub>2</sub>) to be low.



**1. JUST FOUR PARTS** comprise this controller for bicolor LEDs. The NAND gates work with the OFF signal to inhibit the LEDs.

(change color) signal changes the color of the emitted light. Therefore, to produce orange, a clock with a rate above, say, 100 Hz needs to be applied to pin 3 on IC<sub>1</sub>. It's possible to vary the shade of orange by controlling the cycle time of a complementary pair of signals applied to GN and RD.

The remaining state is off. Driving OFF low inhibits both LEDs by forcing both NAND gate outputs high. OFF may also be used with CC to create a red-off-green-off type of blinking. That's achieved by applying complementary or identical signals to CC and OFF at the desired rate. □

# CIRCLE 522 PRECISELY CHECK LOW RESISTANCES

O.R. BUHLER

Storage Technology Corp., MS: 0231, 2270 South 88th St., Louisville, CO 80028; (303) 673-7109.

It's a well-known fact that when measuring very low resistances, special care must be taken to avoid errors. Four-terminal techniques are regularly employed, for example, to eliminate test lead IR errors. But even four-termi-

nal measurements don't address the problem of thermal EMFs (electromotive forces) in the test leads (see the figure, a).

That problem can be eliminated by making two four-terminal measurements—a normal one, and one with

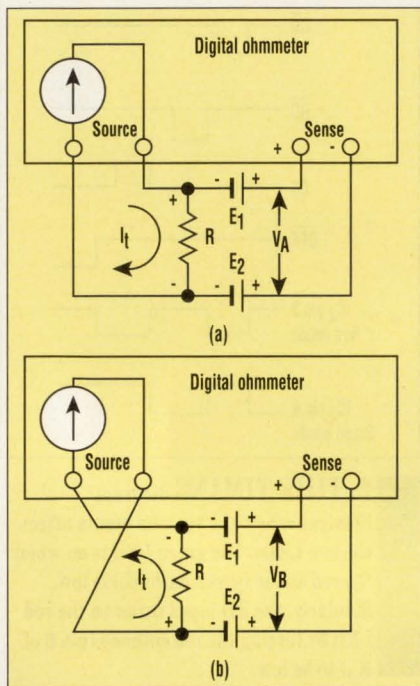
the current source leads reversed (see the figure, b). Averaging the results of the two measurements gives an enhanced result that's free of thermal EMF errors.

To understand why the technique works, consider that the value of R found by the normal measurement, R<sub>A</sub>, is actually given by:

$$R_A = (V_A - E_1 + E_2) / I_t$$

where I<sub>t</sub> is the test current, V<sub>A</sub> is the measured voltage, and E<sub>1</sub> and E<sub>2</sub> are the thermal EMFs. Similarly, the value of R determined with the current source leads reversed (R<sub>B</sub>) is given by:





**E<sub>1</sub> AND E<sub>2</sub>** represent the thermal emfs that can ruin a low-resistance measurement (a). By taking a second reading with the current direction reversed (b) and averaging the results, the errors caused by those emfs can be eliminated.

$$R_B = (-V_B + E_1 - E_2)/I_t$$

Hence, averaging the two readings, R is given by:

$$R = (R_A + R_B)/2 \\ = (V_A - V_B)/2I_t$$

This expression eliminated the thermocouple voltages E<sub>1</sub> and E<sub>2</sub>. In effect, by reversing the current source leads and taking two readings, an extremely low frequency ac test signal was applied to remove thermocouple voltages and minimize reactive effects.

Because the voltage measured with the current source leads reversed (V<sub>B</sub>) will always be negative, and its magnitude is all that's required, the most convenient expression for R uses its absolute value as follows:

$$R = (V_A + |V_B|)/2I_t$$

This method was tested using a commercial four-terminal instrument and a 0.03-Ω, 1% resistor. To ag-

gravate the thermocouple effect, the instrument manufacturer's test-lead recommendations were purposely ignored. First, the resistor was measured using only two leads. The result was a value of 0.169 Ω. Obviously, the lead resistance swamped out the unknown resistor value, mandat-

ing a four-terminal measurement. The normal four-terminal measurement resulted in a value of 0.0341 Ω, which was about 14% high. The reversed measurement yielded 0.0266 Ω, about 11.3% low. Averaging the two together resulted in a corrected value of 0.03035 Ω. □

## CIRCLE 523 TRANSFER DATA FROM A DMM TO A PC

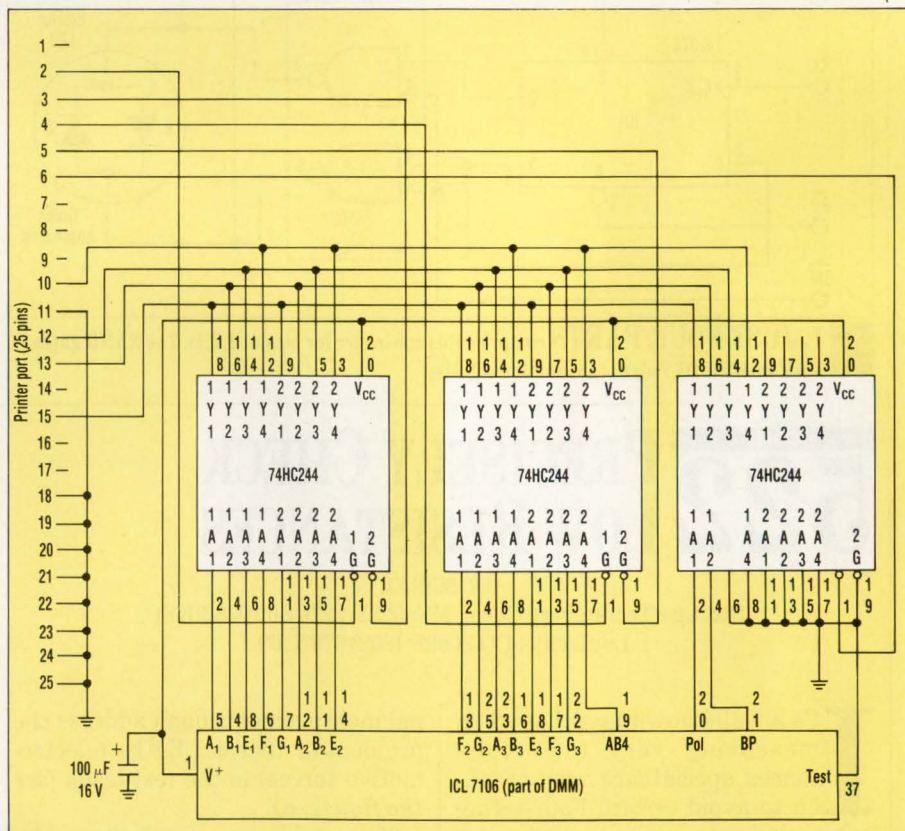
YONGPING XIA

23008 Arlington Ave., # 20, Torrance, CA 90501; (213) 784-2000.

**G**iven the measurement capabilities of a digital multimeter (DMM) and the computational power of a personal computer, it would seem logical to use the former as a data-acquisition front-end for the latter. Then it would be possible to store sequences of measurements for statis-

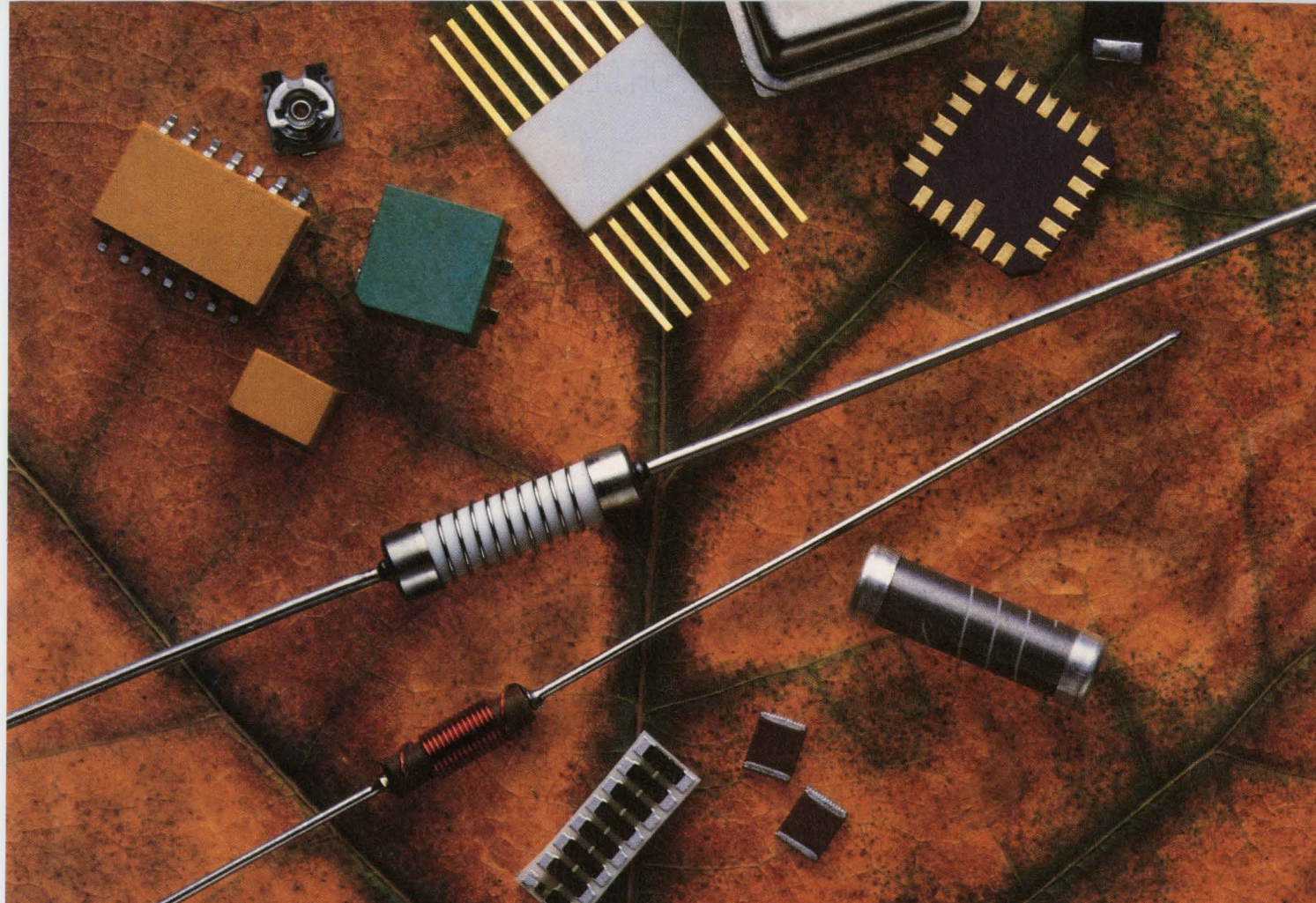
tical analysis, calculate products and ratios like gain and power, identify peak values, and so on. All that's needed is a way to physically connect the two devices and a software routine to transfer the data. Here's that way.

The physical circuitry is built around the popular 7106 analog-to-



**1. THE THREE CHIPS** that comprise the interface between the PC and DMM consume so little power that they can be driven by the DMM's supply.





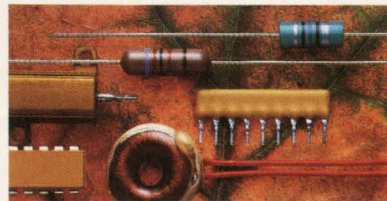
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## IDEAS FOR DESIGN

digital converter, which is at the heart of many 3-1/2-digit DMMs (Fig. 1). That chip, which is designed to drive liquid-crystal displays directly, has a common output signal called BP plus a set of seven segment

lines for each digit. The lines are all low-frequency square waves. The segments that have the same phase as BP are off, while those that are out of phase are on.

Although seven segment outputs

are available for each digit, only five are needed to specify the desired number. Therefore, only 15 lines are required to specify three digits. Three additional lines—BP, polarity, and the fourth half-digit—yield a total of 18 lines connecting the DMM to the PC.

Three 74HC244s buffer the outputs from the 7106. Because they require very little current, they can be powered by the DMM. An independent supply isn't necessary.

The PC connects to the interface circuitry through its parallel printer port. That port is broken down into an 8-bit output section (378H) and a 5-bit input section (379H). Five bits of the output section control DMM-signal-line selection, allowing the PC to read four bits of DMM data at a time. Therefore, a total of only five cycles is required to read all 18 of the signal lines.

A Quick Basic program reads the DMM and displays the data on the PC screen (Fig. 2). It can easily be modified as required by different applications. □

```

DIM d(4)
DIM dat(4)
OUTADDRESS = &H378      ' set output address
INADDRESS = &H379      ' set input address
SELECT1 = &HFE         ' set five selections
SELECT2 = &HFD
SELECT3 = &HFB
SELECT4 = &HF7
SELECT5 = &HEF
OUT OUTADDRESS, SELECT5      ' test BP=0
10  datain = (INP(INADDRESS) AND &H10) / 8
   IF datain = 0 THEN GOTO 10
   datain = (INP(INADDRESS) AND &H10) / 8
   IF datain = 2 THEN GOTO 10
   OUT OUTADDRESS, SELECT1    ' read A1,B1,E1,F1
   datain1 = (INP(INADDRESS) AND &H78) / 8
   OUT OUTADDRESS, SELECT2    ' read G1 A2,B2,E2
   datain2 = (INP(INADDRESS) AND &H78) / 8
   OUT OUTADDRESS, SELECT3    ' read F2,G2,A3,B3
   datain3 = (INP(INADDRESS) AND &H78) / 8
   OUT OUTADDRESS, SELECT4    ' read E3,F3,G3,AB4
   datain4 = (INP(INADDRESS) AND &H78) / 8
   OUT OUTADDRESS, SELECT5    ' read pole
   datain5 = (INP(INADDRESS) AND &H78) / 8
   d(1) = datain1 + (datain2 AND 1) * &H10      ' combine A1-G1
   d(2) = (datain2 AND &HE) / 2 + (datain3 AND 3) * 8      ' combine A2-G2
   d(3) = (datain3 AND &HC) / 4 + (datain4 AND 7) * 4      ' combine A3-g3
   d(4) = (datain4 AND 8) / 8      ' find AB4
   pole = datain5 AND 1      ' find pole
   FOR i = 1 TO 4      ' convert to BCD
   SELECT CASE d(i)
     CASE &HF
       dat(i) = 0
     CASE 2
       dat(i) = 1
     CASE &H17
       dat(i) = 2
     CASE &H13
       dat(i) = 3
     CASE &H1A
       dat(i) = 4
     CASE &H19
       dat(i) = 5
     CASE &H1D
       dat(i) = 6
     CASE 3
       dat(i) = 7
     CASE &H1F
       dat(i) = 8
     CASE &H1B
       dat(i) = 9
     CASE 0
       dat(i) = 10      ' overflow
   END SELECT
   NEXT i
   IF dat(1) = 10 THEN GOTO 20      ' if overflow
   outdata = d(4) * 1000 + dat(3) * 100 + dat(2) * 10 + dat(1)
   IF pole = 1 THEN outdata = -outdata      ' form output data
   PRINT outdata
   GOTO 30
20  IF pole = 1 THEN PRINT "- Overflow"
   IF pole = 0 THEN PRINT "+ Overflow"
30  END

```

**2. THIS QUICK BASIC** routine captures the output of the DMM's 7106 analog-to-digital converter for analysis and display by the PC.

### IFD WINNERS

**IFD Winner for  
November 21, 1991**

**M.S. Nagaraj**, Digital Systems Div., Instat-II Building, I.S.R.O. Satellite Centre, Airport Rd., Vimanapura P.O., Bangalore-560 017, India. His idea: "Spare Lamp Turns On Automatically."

**IFD Winner for  
December 5, 1991**

**John Dunn**, 181 Marion Ave., Merrick, NY 11566. His idea: "Vary Capacitance To Positive Or Negative."

### VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a \$150 Best-of-Issue award and becomes eligible for a \$1,500 Idea-of-the-Year award.



File: coming  
Queue: ed/1  
Route to Donna Bright  
Penton

## COMING ATTRACTIONS:

May 1 (Closes April 3)

### ASICs and CAE: CICC Preview

In this multi-part report, three of ELECTRONIC DESIGN's editors—Dave Bursky, Milt Leonard, and Lisa Maliniak—focus on the papers to be presented at the upcoming CICC conference. This report will examine the latest technology breakthroughs in ICs, test techniques, digital circuits, and mixed-signal devices. It's compelling reading for all designers and managers who are designing or using ICs, ATE, software tools, workstations, synthesis tools, IC testers, test hardware, chip-design tools, and CAE.

May 14 (Closes April 17)

### Special Report: Multi-Media

If you've been eager for design information concerning multi-media systems—systems that combine audio and video—this Special Report is just what the doctor ordered. Computer Systems Editor Richard Nass will unveil the latest technologies and how to apply them to tomorrow's multi-media designs.

### Electro Preview

Also in this issue, John Novellino, the industry's most experienced Test & Measurements Editor, goes behind the scenes at ELECTRO (Boston, May 12-14), one of the major showcases for manufacturers of electronic instruments, components, hardware and interconnections, and CAE software. This horizontal industry-wide show is important to all senior designers and test engineers. Our report evaluates the major new product introductions as well as the technical papers to be discussed at the show.

May 28 (Closes May 1)

### Digital Semiconductors: BiCMOS Technology

Two of *Electronic Design's* most senior editors—Semiconductor Editor Dave Bursky and Analog Editor Frank Goodenough—team up in this issue for this Special Report on BiCMOS Technology. Bursky will examine digital biCMOS—from new chip developments to process improvements—while Goodenough will look at leading-edge mixed-signal devices. It's one report that designers will refer back to all year long.

### Special Section: PIPS

**(Power sources, Interconnections, Passive components, and Switches and relays)**

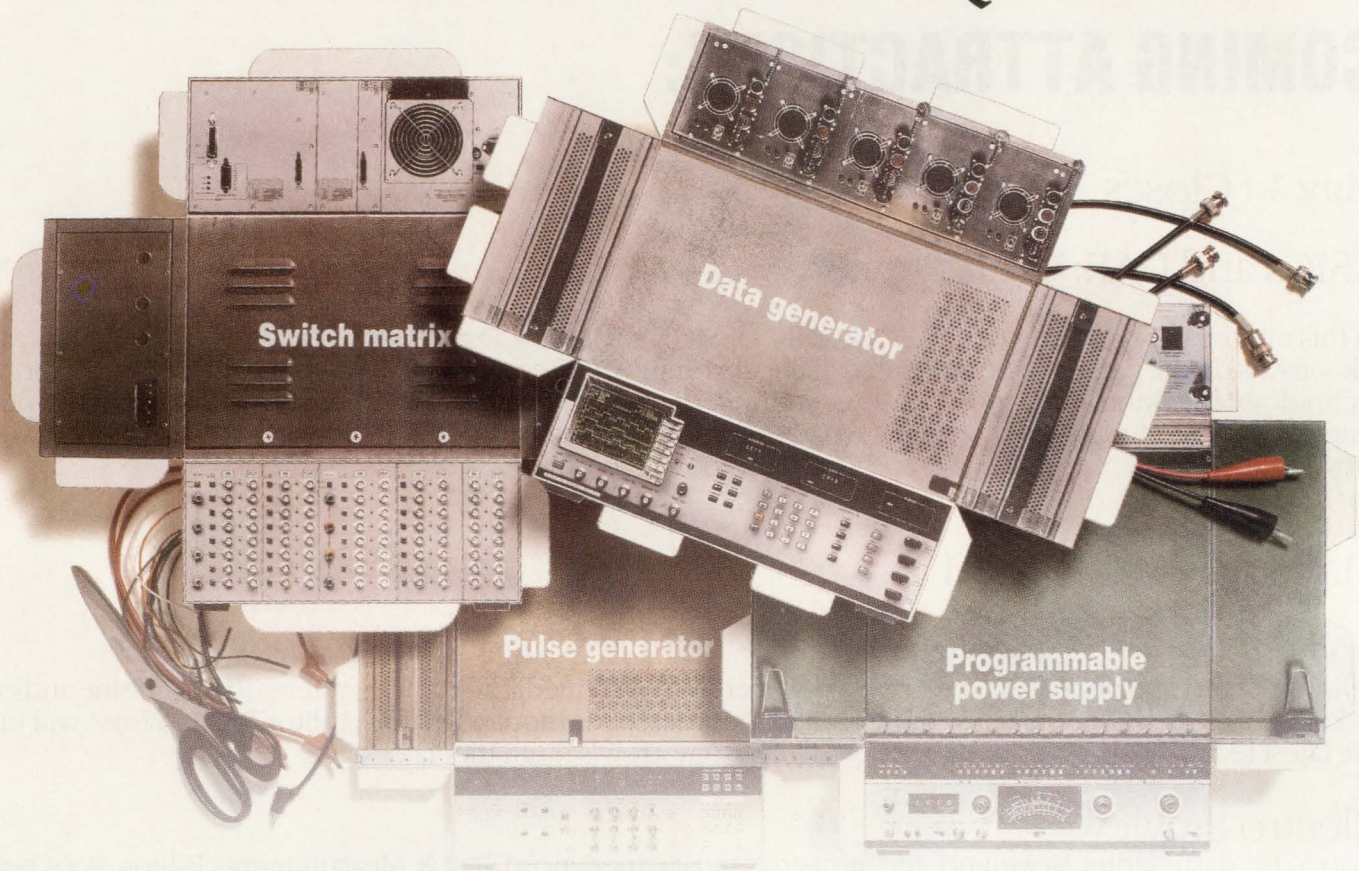
Six times in 1992, *Electronic Design* PIPS Special Sections examines the latest product offerings for engineers and managers who specify basic products. Our PIPS coverage this issue focuses on passive components and includes a who's who of passives manufacturers and their products, giving this issue *great shelf-life*. Five major categories are covered: resistors, capacitors, inductors & coils, crystals & oscillators, and optoelectronics. In addition to a technical article on passives, PIPS capsulizes power sources, interconnections, and switches and relays.

In Every Issue...

Our Ideas For Design along with our Technology Newsletter, New Products, and Quick Look sections bring Electronic Design readers the latest in test and measurement, computer-aided engineering, and components.



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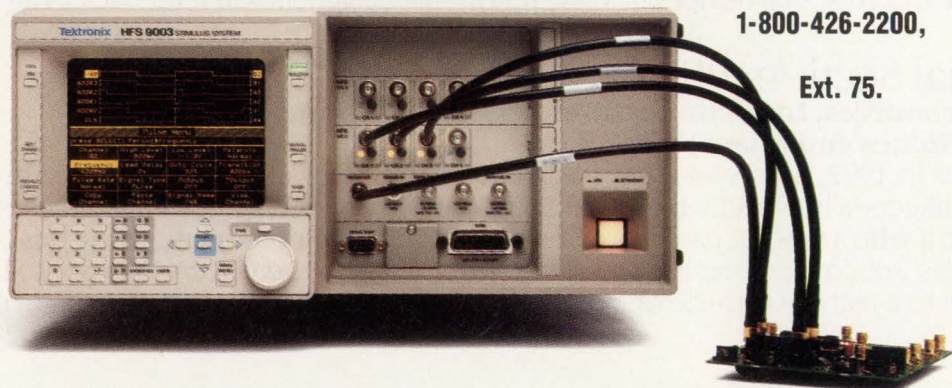
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# QUICK LOOK

EDITED BY SHERRIE VAN TYLE

## MARKET FACTS

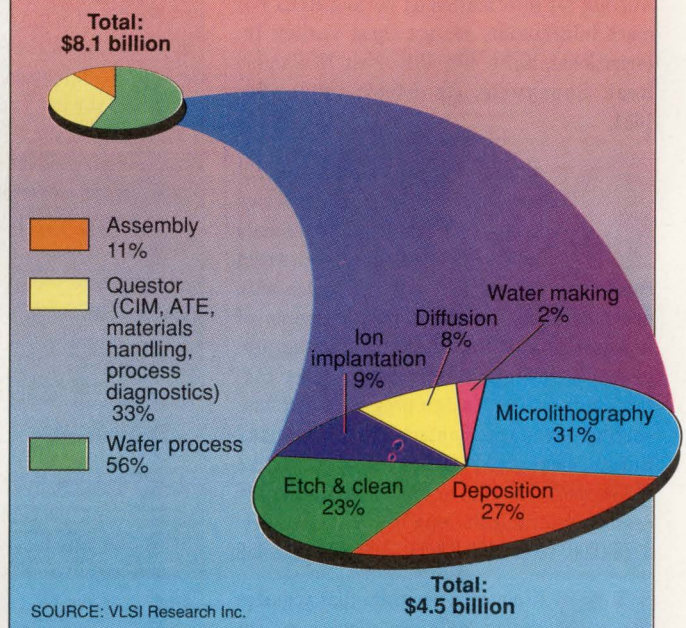
**R**evenues in semiconductor equipment fell off 4% last year compared with 1990, according to VLSI Research Inc., of San Jose, Calif. Of various sectors in the \$8.1 billion equipment market, wafer processing gear suffered the largest decline, falling 9.1% to \$4.5 billion. Still, the semiconductor equipment market performed better than expected, especially with fears of a deepening recession at the close of 1991, says the market researcher.

Some companies quit buying front-end equipment, like lithography and track equipment, which fell by 24% to \$1.4 billion. Deposition equipment also declined, dropping 7.9% to \$1.2 billion. The etch and clean market inched up 1.4% to hit \$1.05 billion.

Questor systems—how VLSI Research describes the sector for computer-integrated manufacturing, automated test equipment, materials handling, and process diagnostics—held steady at \$2.7 billion. Revenues in the automated test equipment (ATE) market increased by \$100 million to hit \$1.4 billion. Sectors closer to wafer processing, like process diagnostics, also saw declines, 2.4% to \$700 million. Materials handling fell 9% to \$580 million, down 9% from the previous year.

The assembly sector performed best, with revenues up 17% to \$849 million. Most of this revenue growth stems from ASM International Technology's contract with the former USSR, notes VLSI. Assembly was boosted by packaging, which saw a 31% increase in revenues, to \$433 million. The bonding and inspection market rose just 3.2% to \$325 million; revenues in dicing equipment grew 9.8% to \$90 million.

## HOW SEMICONDUCTOR EQUIPMENT MARKET STACKED UP LAST YEAR



## QUICK NEWS: CONFERENCES

**A**s companies race to get products out the door on time, within budget, more attention is being paid to concurrent engineering—where design and test managers and engineers work closely together throughout the entire product life cycle. The first annual Concurrent Engineering Award will be presented to recognize companies that have successfully implemented CE in product development at a new conference, Test & Design Expo, May 11-14, 1992, at the Garden State Convention Center in Somerset, N. J. As sponsor of the award, *Electronic Design* will compile all entries and vote on the award, along with the Test & Design Expo technical advisory committee. Criteria for the award include product development time, percentage of products within original budget, number of design iterations, customer/supplier involvement, and structure of the product-development team. Entry deadline is April 17, 1992. Besides exhibits of design software and hardware and test equipment, the expo will have a technical program of tutorials, sessions, and forums. For entry criteria, contact Sharon Schifano, Technical Program Manager, Test & Design Expo, 13760 Noel Rd., Suite 500, Dallas, TX 75240; (800) 223-7126; fax (214) 385-9003. CIRCLE 451

**T**he third annual Women in Engineering conference will be held May 31-June 2 at the Capital Hilton in Washington DC. The conference is sponsored by WEPAN, a national network to give women more access to engineering careers, and coordinated by the Office of Women's Programs at Stevens Institute of Technology in Hoboken, N. J. Keynote speakers include Sheila Tobias, author of *Overcoming Math Anxiety* and *They're Not Dumb, They're Different: Stalking the Second Tier*. Contact Susan Metz, director, Office of Women's Programs, Stevens Institute of Technology, Castle Point on the Hudson, Hoboken, NJ 07030; (201) 216-5245. CIRCLE 452

**A**dvanced cleanroom concepts, computer tools for reliability, behavior of equipment under mechanical shock, and CFC alternatives for precision cleaning are among the technical sessions scheduled for the annual meeting of the Institute of Environmental Sciences. The meeting, which will be held May 4-8, 1992, at the Opryland Hotel in Nashville, Tenn. This year's theme is technical excellence in a global economy. Contact the IES, 940 E. Northwest Highway, Mount Prospect, IL 60056; (708) 255-1561; fax (708) 255-1699. CIRCLE 453



## OFFERS YOU CAN'T REFUSE

**U**sers of the Verilog hardware description language now have an international bulletin board system for sharing information through USENET, a worldwide network consortium. The BBS was started by Open Verilog International, which supports and promotes use of the previously proprietary Verilog HDL. OVI's technical committee members will participate in the BBS, especially regarding standards and technical issues. To access the Verilog HDL BBS, logon to USENET and use the BBS name comp.lang.verilog for information on verilog HDL. For more information, contact Open Verilog International, Suite 408, 1016 East El Camino Real, Sunnyvale, CA 94087; (408) 776-1684. CIRCLE 454

**S**oftware for designing active filters is free from Burr-Brown Corp. Program outputs include print-outs of standard real-world component values. The package comes with documentation, including measurements of representative filters designed by the program. A DOS-compatible, 5.25-in. disk contains three filter design programs and supporting software. Contact Mary Douglass, Burr-Brown Corp., P. O. Box 11400, Tucson, AZ 85734; (602) 746-1111 or (800) 548-6132; or access an electronic bulletin board at (602) 741-3978 (300/1200/2400 8,N,1). CIRCLE 455

**P**CI-meter, a program that acquires analog data for display as on-screen digital and analog meters and bar graphs, has a free demo disk. High and low alarm setpoints can be configured to trigger digital outputs when setpoints are reached. Process values can be modified to engineering units using scaling factors and linearization for thermocouples is also supported. Meters can be saved to PCI-meter application files and reconfigured at any time. Contact Intelligent Instrumentation, 1141 W. Grant Rd., MS 131, Tucson, AZ 85705; (602) 623-9801; fax (602) 623-8965. CIRCLE 456

**A**PC-based catalog for electronic enclosures is free to engineers and buyers of electronic enclosures. Cab-net software from Equipto Electronics includes more than 10,000 line items, text descriptions, color photos, accessories, technical drawings, and prices. For a free copy, contact Equipto Electronics, 351 Woodland Ave., Aurora, IL 60506-9988; (708) 897-4691; fax (708) 897-5314. CIRCLE 457

## K M E T ' S K O R N E R

### ...Perspectives on Time-to-Market



**BY RON KMETOVICZ**

President, Time to Market Associates Inc.  
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

**W**ould you knowingly start on product development that could take 5, 10, 15, 20, or more years to get to the market? Besides taking this time, would you be willing to make frequent trips to the bank or financial markets to get the cash needed to do the job as cumulative development costs reach for the stratosphere?

Next, can you live with the fact that only a few people, possessing limited data, have the product and market vision to make the venture successful? And finally, will you be able to tolerate the frequent change in direction necessitated by using learn by doing development? If you can honestly answer "yes!" to all of these questions and want to learn how to make your prospective plan a business success, then you're ready to consider doing first-of-a-kind new product development.

Risk and uncertainty are extremely high in developing new products. Examining the product classification matrix shows that first-of-a-kind developers work with new product concepts that they intend to take into new markets. As such, these inspired individuals pick the path that contains the greatest possible number of perils. If the people with the vision prove to be right, new businesses, industries, markets, and companies will materialize. As a result, the potential for significant reward substantially offsets the ever-present possibility of failure.

Within the past 20 years, major first-of-a-kind product introductions include the microprocessor, video cassette recorder, personal computer, workstations, and critical support programs as well as application software. To this short list, add products that were first of a kind in your field of interest. Each product listed and those you have thought of were many years in the making. And, when they first arrived on the market, potential customers had to be shown why they needed and should buy the product. Yet, behind the scenes, there were people driving these efforts that had a vision of how they would create markets and generate business success.

Where are today's first-of-a-kind products? One example that comes to my mind is AT&T's recent introduction of the picture phone. This gadget is a classic first-of-a-kind production. To begin with, it has been a long time in the making. I remember seeing a prototype picture phone at the New York World's Fair in 1964—that was 28 years ago! Between then and now, how much money do you think AT&T has plowed into an effort that had to be of the on-again, off-again, variety?

I conservatively estimate the total development figure to be at least \$60 million. Somehow over this extended period of time the idea stayed alive within AT&T. Would anyone care to guess how this happened? I also speculate that technological change over this extended development period caused AT&T to scrap many of its ideas. And yet, in 1992, you can go out and buy your own picture phone for a mere \$1500. Why?

You may not know why yet or maybe you think the picture phone is a dumb idea. But if AT&T is taking this introduction seriously, the company will soon be talking to the people it thinks should buy a picture phone. If the product and the push into new markets are effective, money will begin to flow in AT&T's direction. Will 1 million units or 10 million units be sold worldwide two to three years from now? No matter, at 1 million units it's a billion dollar market; at 10 million units it's just ten times larger! AT&T has its organization focused on what the company thinks will be a new multi-billion dollar per year market. And the marketing gurus should now be doing all in their power to help make this market materialize. Let's see what happens over the next few years. The question is, will AT&T hit a grand slam?

In the meantime, look at the new product efforts in your portfolio. If you have a first-of-a-kind venture, assess whether your organization is equipped to deal with high risk product and market issues.



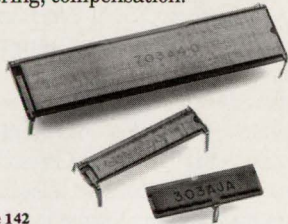
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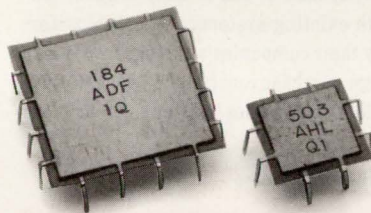
- Special pinouts to address wide variety of specialty DIPs such as analog devices, op-amps, center pinout advanced CMOS devices.
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Circle 142

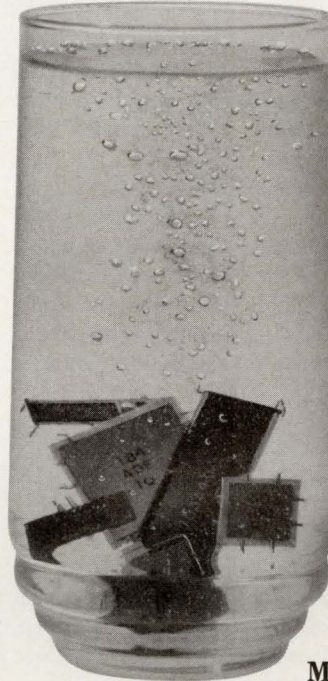
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nate discrete decoupling capacitors, and boost the reliability of the PCB assembly.

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- Board rigidizer
- Heat sinking function

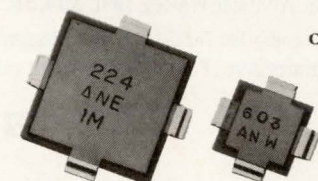


Circle 146 for Immediate Need (U.S. Response)  
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Circle 145



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*Henry Wiesel is a financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221. He invites questions and comments.*

## BESTSELLERS

*Which technical books are the most popular in Silicon Valley?*

### ELECTRONICS:

1. *SPICE: A Guide to Circuit Simulation and Analysis Using PSpice* by Paul W. Tuinenga. Prentice-Hall, 1992. **\$24.**
2. *The Art of Electronics, 2nd ed.*, by Paul Horowitz and Winfield Hill. Cambridge University Press, 1990. **\$54.50.**
3. *Spice for Circuits and Electronics Using PSpice* by Mohammed H. Rashid. Prentice-Hall, 1990. **\$25.80.**
4. *BiCMOS Technology and Applications* edited by Anthony R. Alvarez. Kluwer Academic Publishers, 1989. **\$68.50.**
5. *Noise Reduction Techniques in Electronic Systems, 2nd edition* by Henry W. Ott. John Wiley & Sons, 1988. **\$51.95.**

### COMPUTER SCIENCE:

1. *Learning GNU Emacs* by Debra Cameron and Bill Rosenblatt. O'Reilly & Associates, 1991. **\$24.95.**
2. *C++ Primer, 2nd edition* by Stanley B. Lippman. Addison-Wesley, 1991. **\$32.25.**
3. *The New Hacker's Dictionary* edited by Eric Raymond. Massachusetts Institute of Technology (MIT) Press, 1991. **\$10.95.**
4. *Programming the Display PostScript System with Nextstep* by Adobe Systems. Addison-Wesley, 1992. **\$26.95.**
5. *C++ Programming Language, 2nd edition*, by Bjarne Stroustrup. Addison-Wesley, 1991. **\$34.50.**

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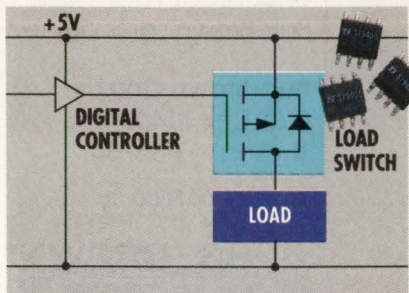
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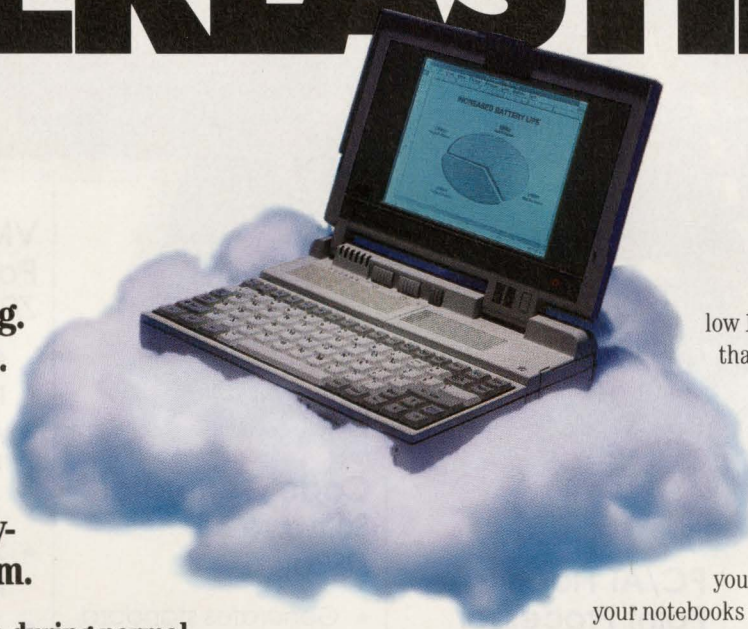
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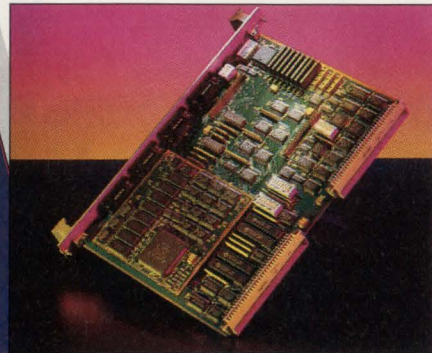
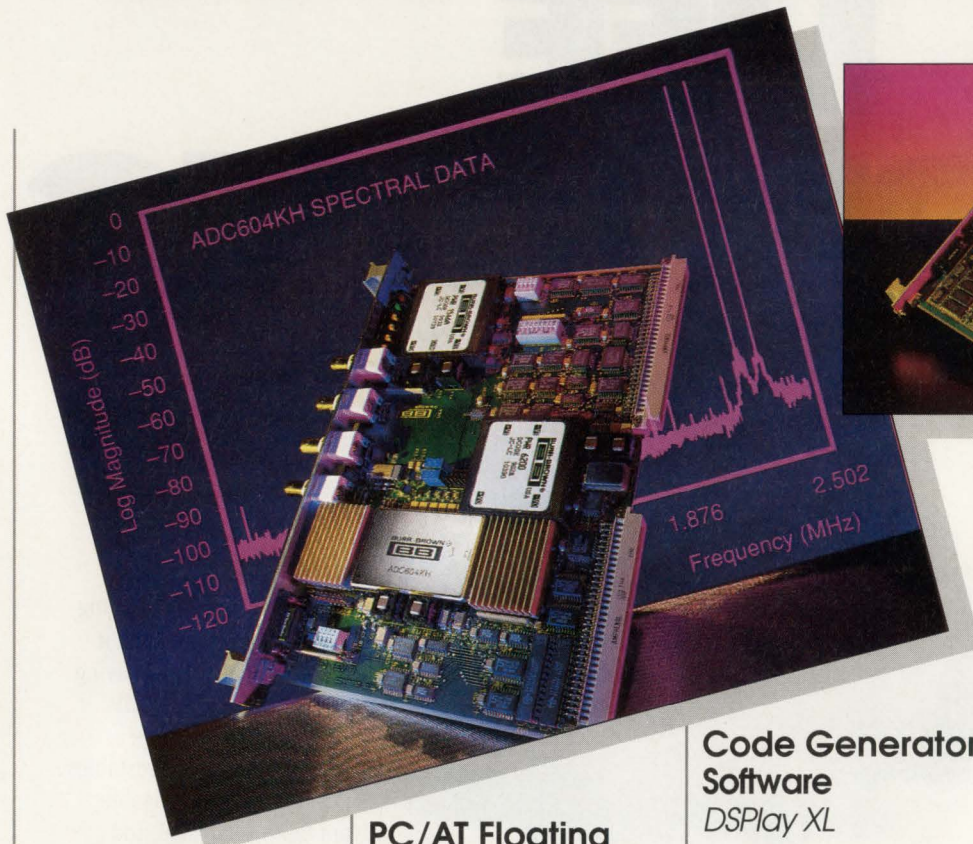
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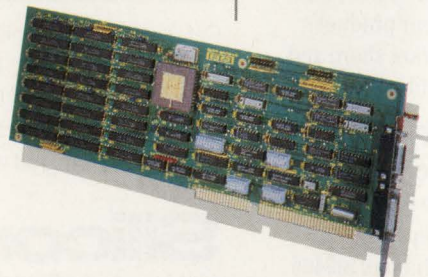
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# WHAT'S ALL THIS CALCULATOR STUFF, ANYHOW?

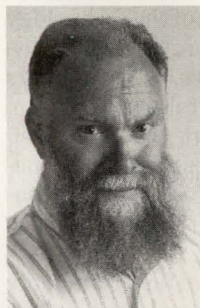
*(Thoughts on the Accuracy Limits of Scientific Calculators...)*

**H**ow willingly we trust our calculators! Yet, like everything else, these ubiquitous tools do have limits. In particular, their accuracy limits are beginning to show in our ever more complex and precise engineering calculations. To illustrate the problem, here's a simple calculation that you can work on your own calculator:

$$((1 - (\cos(3/7))^2 - (\sin(3/7))^2)^{0.25} = 0 \text{ ???})$$

Remembering the trigonometric identity for squared sines and cosines, you know the answer has to be zero. But your 10-digit calculator probably gives an answer on the order of  $4 \times 10^{-6}$ , a much larger discrepancy than you would expect from the calculator's claimed 10-digit resolution. This error, of course, comes from accumulated truncation and round-off errors in the transcendental algorithms — the computational version of NOISE.

Another source of squirrely readings is the low voltage levels used in modern calculators. The MOSFETs' inherent analog underpinnings become apparent at low supply voltages, where channel voltages may vary only 10:1 between the 1 and 0 digital states. In essence, each



**BOB PEASE**  
OBTAINED A  
BSEE FROM MIT  
IN 1961 AND IS  
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SCIENTIST AT  
NATIONAL  
SEMICONDUCTOR  
CORP.,  
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CALIF.

FET is a linear amplifier at both of its digital extremes. As a linear amplifier, it can pick up and amplify strong RF or pulsed fields. For some plastic-cased models, operation near a terminal's horizontal transformer, a radar transmitter, or a medium-frequency broadcast station can jump the display reading without any apparent cause.

The calculator IC's analog roots are, in fact, the reason why you can't buy portable scientific calculators with better than 12-digit precision. It becomes a matter of voltage regulation. The battery's voltage drops about 40% as its energy is drained. Ordinary calculator chips have Power-Supply Rejection Ratios on the order of 180 to 210 dB, allowing 8 to 10 digit calculators to operate without error ( $10^{(200/20)} \text{ dB} = 10^{10} = 10 \text{ digits}$ ). Leading-edge companies like HP and TI use voltage regulators and factory calibration to gain another 60 dB of suppression, bringing dependable performance to the 13-digit level. But that's about it for portable units.

Although careful analog design keeps PSRR errors below digital significance in scientific calculators, those techniques can't provide the high precision needed in accounting calculators. Consequently, calculating a really large number — such as the bottom line for the second overrun of a military hardware contract — will show some variable errors in the last digits on a 14-digit accounting calculator. In fact, aerospace accountants are rumored to earn their lunch money simply by changing to fresh calculator batteries before the final column addition. Fortunately for them, "calculator faith" hides these small transgressions

from the GAO (Government Accounting Office).

The accounting calculators represent a large market, and their accuracy demands will likely fuel research for improved battery and regulator technology in the next decade. Japanese researchers hope to produce accurate 14-digit machines by the turn of the century, spurred by suspicions of low-battery use when converting trade-balance dollars to yen. Despite these incremental improvements, however, some analog experts smugly hint that digital engineers will never design a calculator accurate to one part in  $10^{16}$ .

Analog engineers in the know infer that the Digital Illusion can't be supported beyond 16 digits. At that precision, the digital two-state simplicity collapses and all circuits revert to their basic analog nature. The prima donna digital engineers must then face the dirty "real world" uncertainties that we analog engineers face every day. Just as playtime for digital bus design ended at 20-MHz data rates, the Digital Illusion ends at 16 digits.

The analog engineer — always thoughtful, physically attractive, and suave — doesn't base the Digital Illusion's limit on mere speculation. Nay, this limit has roots deep in theoretical physics, a subject quite familiar to the analog engineer's restless intellect. In fact, it's the famous Heisenberg Uncertainty Principle that imposes an absolute 19-digit limit on digital-calculator accuracy. In 1927, as many experienced analog engineers will recall, Heisenberg recognized that the minimum energy kicked into a system (when making a measurement) is inversely proportional to the measurement time. That is,  $dE \times dt$  can never be less than Planck's constant,  $4.14 \times 10^{-15}$  electron volts per Hertz (eV/Hz). Consequently, the longer you take to do something, the less disruptive energy is injected, and the more exact the result.

The occurrence of an Uncertainty Error is, of course, probabilistic. It can occur in any calculation, as students of engineering quickly discover, but it is much larger and more likely in calculations where the disruptive energy is large — i.e., where the calculation time



# PEASE PORRIDGE

is short (or when you are in a big hurry). Consider some facts from your own experience... calculations done on a Cray super-computer at gigaflops rates (earthquake prediction, rainfall prediction, national debt prediction, origins of the universe) are subject to great uncertainties, whereas computations done on a slide rule at deciflops rates (resistor values, the price of 12cp

amps) are seldom wrong by more than 5%. These Uncertainty Ratios remain valid even at microflop rates. For example, computer programs that require several man-years of debugging are much more reliable than those that work the first time.

Calculating the 19-digit limit is beyond the scope of this short article, but is recommended as an exercise for the

Gentle Reader. Start with Maxwell's equations. Use a 3.6-V lithium battery, 2N3904 transistors, and 99.2 eV (12.648 nm) lithography to establish boundary conditions (savvy analog engineers will use their slide rule's div, curl, and grad scales to make quick work of the vector differential equations). Your answer may differ somewhat from 19, depending on how much you rush the calculations. If you must use a digital computer, analog engineers amicably recommend that you stick with an Apple I, Altair 680, IMSAI 8080, or PDP-8 models to minimize spurious answers.

I hope this peek into calculator theory will dispel the blind trust in calculator and computer results, and in all that complex digital stuff. Now that you've been alerted to a future of continuing digital problems, you will not be surprised when your naïve colleague's new 17-digit calculator sinks into Digital Nirvana when trying to pin down the penultimate digit. You will know that calculators, like everything else, face limits. The Digital Illusion can't shelter us indefinitely. Although the affable, warm-hearted analog engineers have used all of the technology at their disposal to stretch the Illusion over the last 40 years, their numbers dwindle, and the digital engineer's age of innocence must end. A moment of silence, please, for those generous analog folks who have worked so continuously and indiscreetly during these long, hard years.

Now just a couple of final comments from RAP: While I would love to say that I wrote this, I must give all the credit to James A. Kuzdrall, P. E., Chief Engineer at Intrel Service Co., P.O. Box 1247, Nashua, NH 03061. When I saw Mr. Kuzdrall's draft of this, I knew it was a perfect choice for this guest editorial. He's a man after my own heart.

*And, lastly, April Fool!*

All for now. / Comments invited!  
RAP / Robert A. Pease / Engineer

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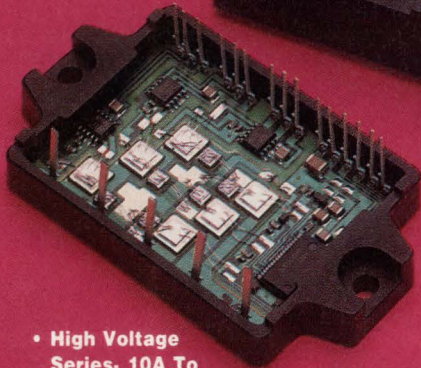
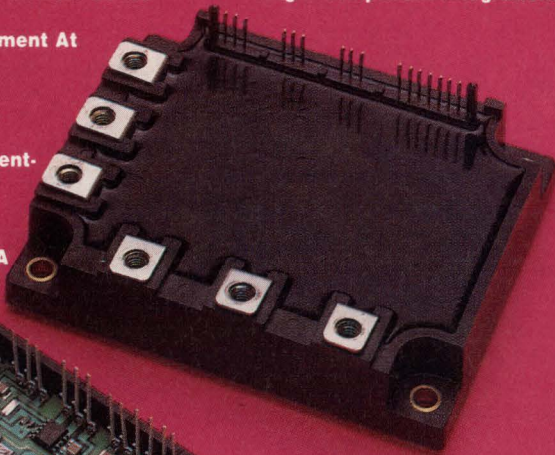
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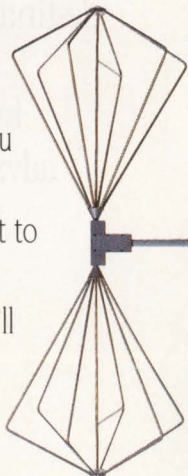




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# ON-CHIP 8-BIT DACs SET COMPARATOR THRESHOLDS

ON-CHIP 8-BIT DACs SET AND VARY THRESHOLD VOLTAGES OF QUAD, 1.5- $\mu$ S COMPARATOR, AND 4- AND 10-NS SINGLE ECL AND TTL COMPARATORS.

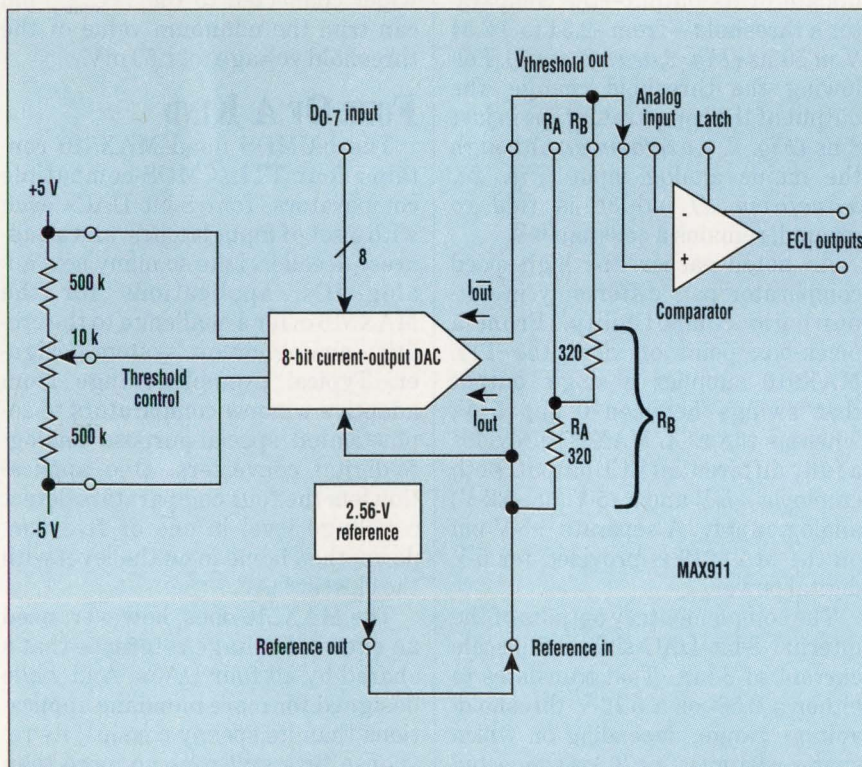
FRANK GOODENOUGH

**W**

ith the exception of zero-crossing applications, in which the reference is ground or common, every data converter's comparator needs a reference. In many applications, standard reference values such as 1.25, 2.5, 5, or 10 V aren't what you need, and some oddball voltage like 1.73 V may be required that calls for a trimpot or often a more

complex approach involving a digital-to-analog converter. Here, the reference is set by a host processor. Such an approach also lets you change the reference voltage on the fly. To simplify the job of building this type of microprocessor-controlled, or adaptive, comparator, Maxim has readied the MAX910, MAX911, and MAX516. They represent the first in a family of programmable-threshold comparators containing on-chip DACs. The MAX910 and MAX911 offer high speed; the third offers four comparator-DACs on one chip.

The MAX910 and MAX911 differ only in speed and output-logic compatibility. The former supplies one TTL/CMOS output, while the latter has a fully differential ECL output (Fig. 1). Built on a high-speed complementary-bipolar (CB) process, the MAX910's TTL response time (propagation delay) is a maximum of 10 ns, and the MAX911 ECL response time is 4 ns. Each contains one comparator, an 8-bit DAC, a voltage reference, and a pair of output-span-setting resistors. If the parallel 8-bit word to the DAC must be latched, ex-



**1. AN ON-CHIP 8-BIT** current-output DAC sets the threshold voltage of the 4-ns MAX911 comparator from Maxim, between -2.56 and +2.56 V. The fully-differential ECL-output unit is designed to allow users to set and vary the comparator's threshold-voltage levels with relative ease and at high speed.



# ON-CHIP DACS WITH SETTABLE-THRESHOLD COMPARATORS

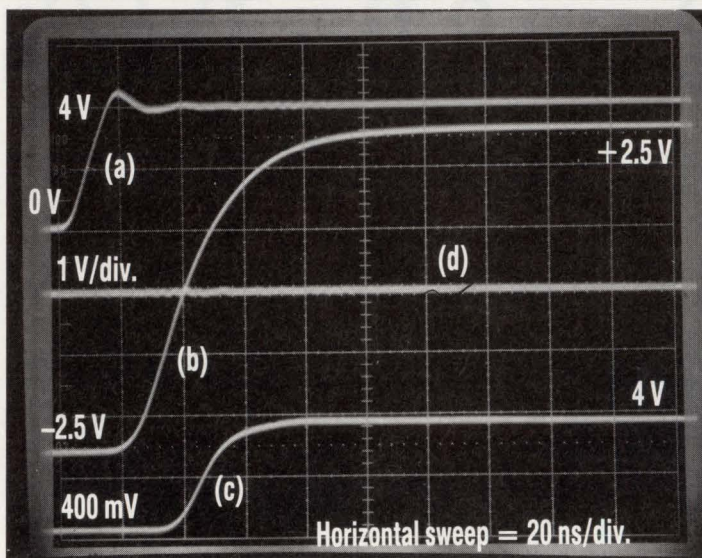
ternal ICs are required for the job. On the other hand, the comparators' output can be latched, so it's unaffected by changes in the analog or digital inputs. Bringing the Latch pin low freezes the comparators' output. With the pin high or floating, any change in analog input or code may shift the output from high to low or vice versa.

In high-speed comparator applications where the threshold voltage must be updated rapidly, the combination of a comparator and a parallel-data-bus DAC on one chip not only cuts the speed-reducing effects of stray capacitance, but also reduces board space, design time, and cost. High-speed automatic test equipment (ATE) used to test semiconductors represents a good example of such an application. Or, two or more of these ICs can be used to build an extremely versatile window comparator for waveform analysis and clock recovery in data-recording and communications systems.

## TWO TIMINGS

Two response times define the dynamic performance of these fast comparator-DACs, depending on whether the comparator's digital input is fixed and its analog input varies, or vice versa. In the normal operating mode, the conventional response time extends from when the analog input exceeds the comparator's threshold value to when the digital output changes from low to high, or high to low. In this mode, both the MAX110 and MAX111 can track 100-MHz signals.

When used with fast-changing DAC-set threshold voltages, the comparator's output response time, due to a code change that moves the threshold voltage through the existing analog input voltage, becomes important. For example, following a TTL input code change from all zeros



**2. FOLLOWING AN INPUT** code change from all zeros to all ones (a), the output of the MAX910's DAC shifts from  $-2.56$  to  $+2.56$  V in under 50 ns (b), and the output of the comparator changes state (c) a few ns later. However, the analog input (d) remains unchanged from 0 V. The MAX910 from Maxim is a comparator with a variable-threshold on-chip 8-bit DAC.

to all ones (Fig. 2, waveform a), the MAX910's DAC achieves a full-scale update of its output—the comparator's threshold—from  $-2.54$  to  $+2.54$  V in 50 ns (Fig. 2, waveform b). Following the threshold change, the output of the comparator flips in just 8 ns (Fig. 2, waveform c), although the minus analog input (Fig. 2a, waveform d), which is tied to ground, remains a constant 0 V.

As noted earlier, the high-speed comparator pair differ only in output-logic compatibility. From a black-box point of view, the TTL MAX910 supplies a single output that swings between 0 and 5 V, whereas the ECL MAX911 provides a fully differential ECL output. Both employ a  $+5$ -V and a  $-5$ -V (or  $-5.2$ -V) analog supply. A separate  $+5$ -V pin on the MAX910 is provided for 5-V digital power.

The complementary outputs of the internal 8-bit DAC sink a full-scale current of 8 mA. That translates to either a 2.56- or a 5.12-V threshold-voltage range, depending on which span-resistor ( $R_A$  or  $R_B$ ) is connected to the threshold-voltage output pin  $V_{\text{threshold out}}$ . The DAC's output current,  $I_{\text{out}}$ , flowing through the span resistors, develops the code-depen-

dent voltage available at the  $V_{\text{threshold out}}$  pin. Span-resistor choice determines the full-scale voltage range and thus the resolution of the threshold voltage applied to the comparator's input.

When the internal 2.56-V reference is used with the 320- $\Omega$  span resistor  $R_A$ , the digital input code varies  $V_{\text{threshold out}}$  from 0.01 to  $+2.56$  V with a resolution of 10 mV/least-significant bit. Using both span resistors to form a 640- $\Omega$   $R_B$ —the  $R_B$  pin is connected to  $V_{\text{threshold out}}$ —results in a  $V_{\text{threshold out}}$  between  $-2.54$  and  $+2.56$  V at a resolution of 20 mV/LSB (Fig. 1, again). Alternatively, an external reference and/or span resistors can be used. An optional voltage divider containing a potentiometer with its wiper connected to the  $\text{TH}_{\text{control}}$  pin can trim the minimum value of the threshold voltage to  $\pm 50$  mV.

## FOUR OF A KIND

The biCMOS quad MAX516 contains four TTL/CMOS-compatible comparators, four 8-bit DACs each with a set of input latches, and an address decoder. Like so many new analog ICs, applications for the MAX516 offer a challenge to the creative analog circuit/system designer. Typical examples range from adaptive window comparators to sophisticated special-purpose analog-to-digital converters. One application lets the four comparators detect a voltage level in one of five windows, then home in on the level with the closest DAC.

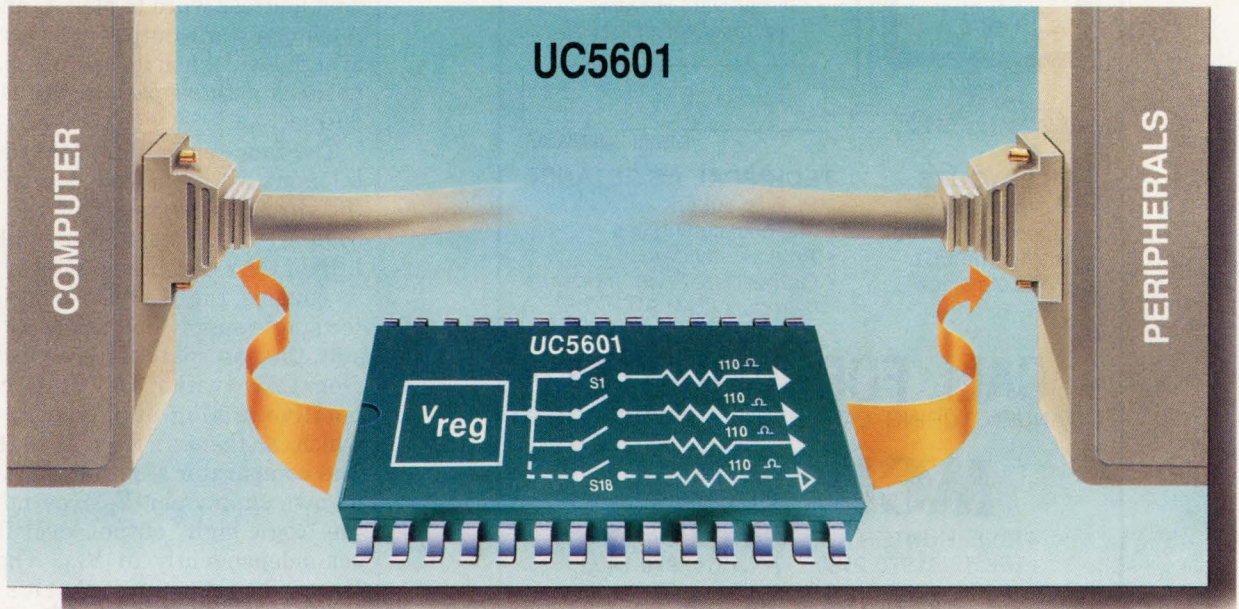
The MAX516 does, however, need an external voltage reference that's shared by all four DACs. And while designed for more mundane applications than its speedy cousins, its response time still runs no more than just 1.5  $\mu$ s.

Unlike its cousins, only the plus inputs of the comparators are brought out to pins, and the DAC outputs con-

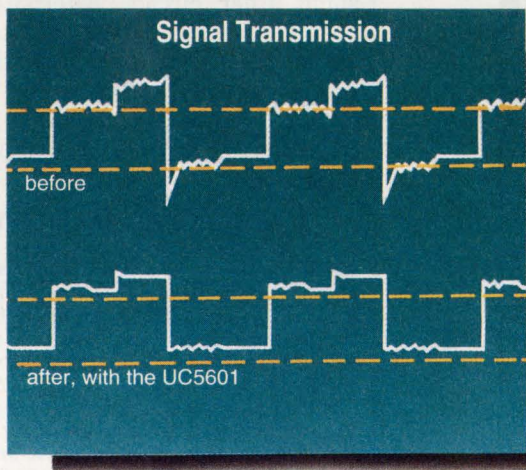


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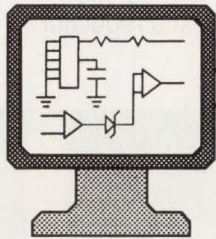
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nect directly to the comparators' minus inputs. However, each DAC's register is loaded with a different digital word under the direction of a 2-bit address word to pins A<sub>0</sub> and A<sub>1</sub>. A comparator's output goes to a logic high level when its analog input is positive with respect to the DAC's output.

The four sequentially loaded digital-input words independently vary the threshold voltages of the four comparators from 0 V to within 1 LSB of the reference voltage. Unlike its cousins, the MAX516 is designed for single-supply operation. As a result, the external reference can run from 1.25 to within 3.5 V of the chip's positive analog supply rail, V<sub>DD</sub>, which can then run from 4.5 to 16.5 V. The comparator's output stage has its own supply pin (V<sub>CC</sub>), permitting the "logic high" output levels to be set independently of V<sub>DD</sub>. That is, V<sub>CC</sub> can be set at 5 V so that it's compatible with standard TTL/CMOS logic levels. It can also be set up to 300 mV higher than V<sub>DD</sub> to achieve greater noise immunity, or to drive some other circuit. Alternatively, both analog and digital circuits can work off +5 V to 1.5 V, even if the reference, and thus the analog input signal, is limited. The MAX516 dissipates just 50 mW from a 5-V power supply. □

### PRICE AND AVAILABILITY

Both the MAX910/911 and the quad MAX516 come in 24-pin packages, in narrow-DIP and wide-body SOIC versions. All three comparator-DACs are available for the commercial- and extended-industrial-temperature ranges. In addition, the MAX 516 is available in 24-pin CERDIPs for the military-temperature range. In quantities of 1000, the MAX910 and MAX911 start at \$6.25 each. In similar quantities, the MAX516 starts at \$6.00 each (or \$1.50 per comparator-DAC).

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

For the MAX516, contact Steven Leandro.

CIRCLE 512

For the MAX910 and MAX911, call Steven Pratt.

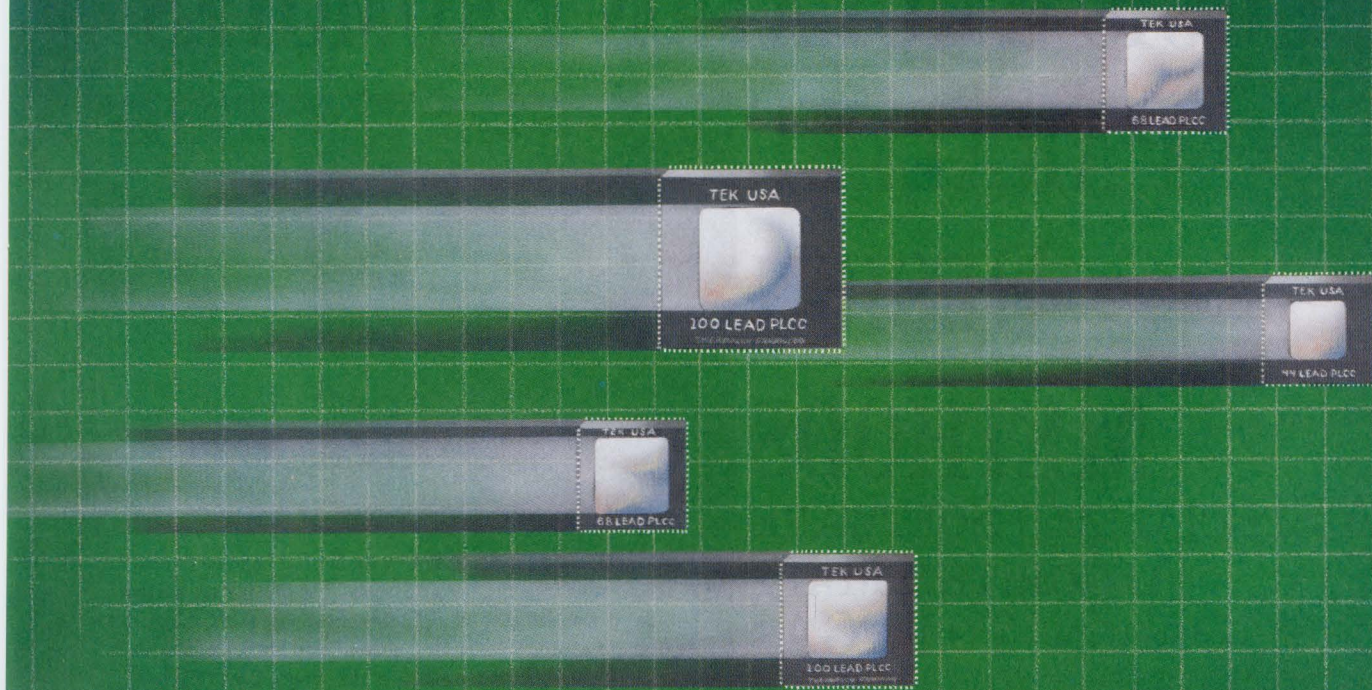
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MODERATELY	539
SLIGHTLY	540



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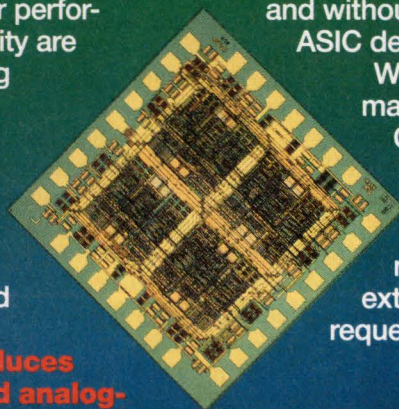
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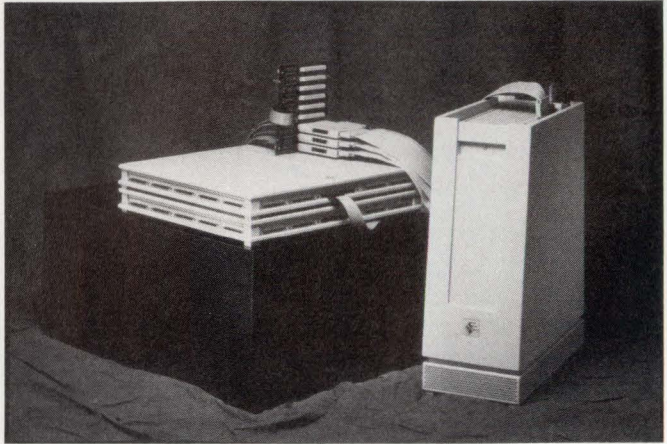
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# LOGIC EMULATION PROMOTES

## PARALLEL DESIGN METHODS

A SPECIALIZED SOFTWARE  
ALGORITHM MAPS  
DESIGNS TO FPGAs  
FOR VERIFICATION OF  
CIRCUITS BEFORE  
THEY'RE BUILT.



**MODULARITY IS KEY** to the Mars II logic-emulation configuration from PiE Design Systems. The DebugWare portion of the system (sitting at the right side of the photo) is a standalone unit that's used as a server for multiple Logic Block Modules (located on the table in the middle of the photo). Each LBM is compact enough to fit on a workbench, close to the target system. In addition, LBMs can be linked to emulate larger designs. Interface buffers called Pods (sitting on top of the LBM in the middle of photo) connect the DebugWare and LBM to the target system using lightweight, flexible cables.

LISA MALINIAK

**T**raditional serial design environments promote isolation of hardware and software development, which can lead to problems. For instance, when a design team eventually integrates a project's hardware and software modules, they may find errors due to differences in interfaces or misinterpretations of a common specification. To make matters worse, these errors are discovered late in the design cycle when corrections cost the most time and resources.

Parallel hardware and software development, however, bypasses many of these problems. Unfortunately, all of the EDA technology needed for parallel development, mainly in the area of simulation, is still not in place. Slowly but surely, however, the proper tools are becoming available.

One new tool that takes a step in the parallel-development direction is the Mars II logic-emulation product from PiE Design Systems. Engineers use logic emulation to create hardware representations of the designs they're working on, which are then used as models in the target system for system-level debugging and analysis. Logic emulation differs from traditional software simulation because engineers can exercise complex VLSI components in target-hardware systems, and discover any errors much earlier in the design cycle.

Mars II is built from field-programmable gate arrays (FPGAs), which create a general-purpose hardware product that's reusable and reprogrammable. Logic emulation maps a logic design into the FPGAs, providing a physical representation of a circuit. The hardware can then be plugged into the end product for analysis of a design that's still being developed.

What most distinguishes the Mars II product from current logic-emulation products like Quickturn's hardware modeler is the innovative timing-driven partitioning software that automates the logic-emulation process, says Lavi Malhotra, director of product marketing. The software reduces emulation time to hours and provides a high degree of FPGA transparency because a compiler insulates users from the technology-dependent limitations of the underlying hardware. A specialized algorithm, called the Constructive Timing Optimization



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*reason we produced*

*The*

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F I R S T

16 *meg*

D R A M ?



Y E S *there was.*

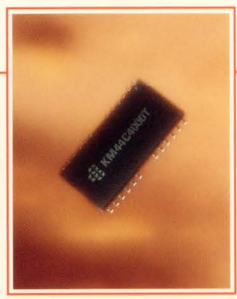
T O L E T

*you*

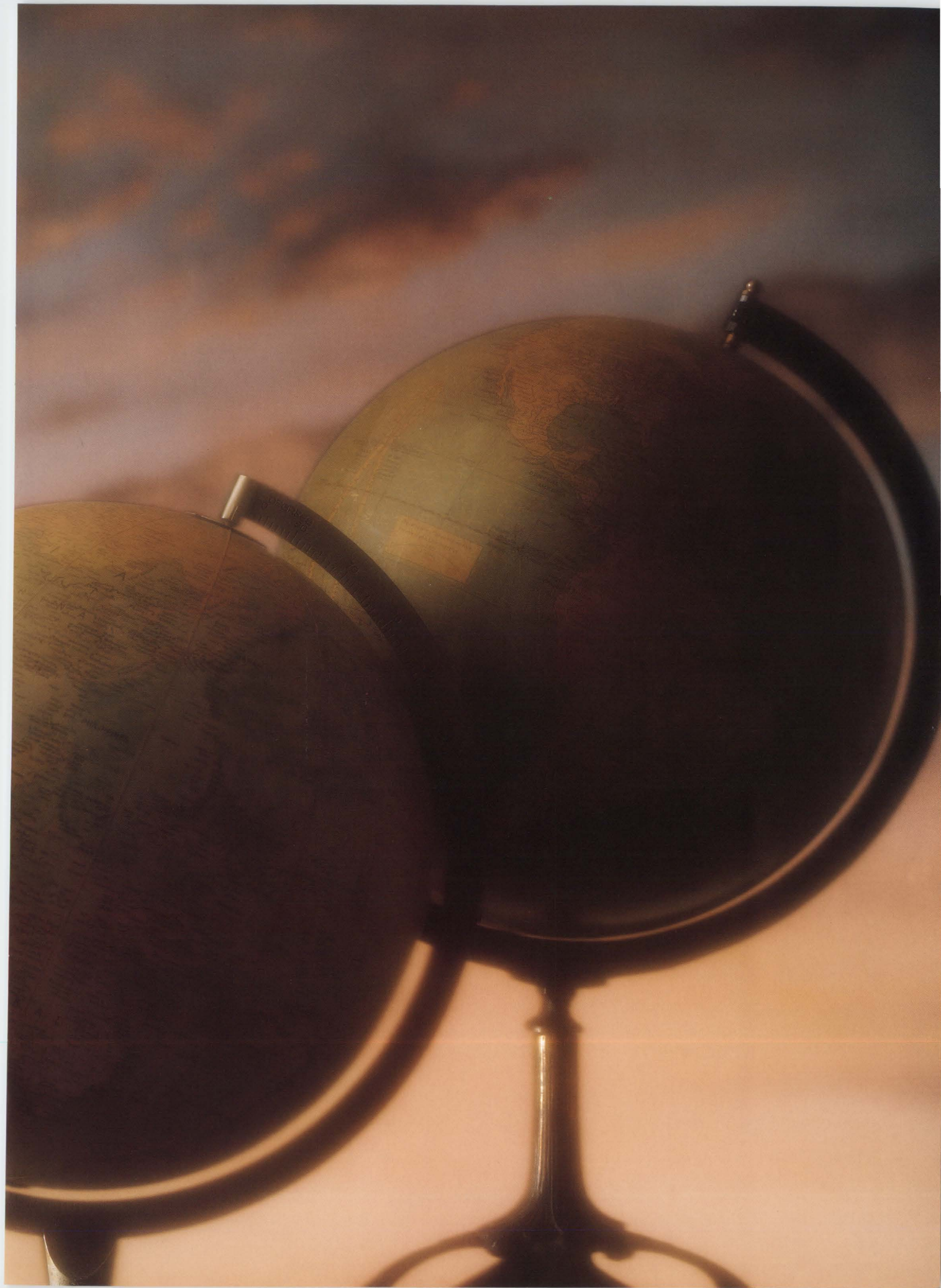
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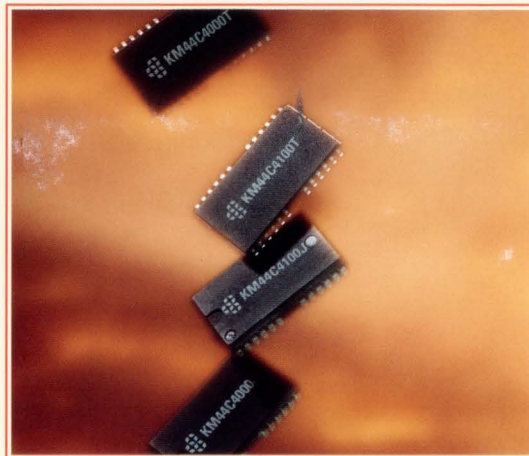
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## LOGIC-EMULATION SYSTEM

(CTO) algorithm, automatically partitions a design and maps it to the logic-emulation hardware in one pass. Earlier emulation systems required multiple passes and user intervention in the design-compilation process. In addition, PiE added timing synthesis that ensures correct hold time for design implementation in the emulator.

Another big difference between the PiE and Quickturn products, says Malhotra, is in the hardware architecture (see the figure). The Mars II architecture is modular, and separates the debugging and emulation functions. The debugging function is a shared resource supporting several emulation modules. Functions are added as they're needed. Also, Mars II can support a mixed-FPGA emulation environment, so future emulation modules based on newer FPGA technology can co-exist with older modules on the same project.

The Mars II logic-emulation family is made from a set of shared software and hardware modules. Software modules, which run on users' workstations, include the compiler, emulation kernel, analyzer, and functional test. The compiler uses the CTO algorithm, FPGA technology information contained in the kernel, and hardware-interconnect technology to partition designs and map them to hardware. The emulation kernel comprises the software core that manages both the FPGA data and hardware resources. In addition, the object-oriented kernel provides a graphical user interface based on X-Windows and Motif. Finally, the analyzer controls and displays data for logic analysis, and the functional test verifies emulation system setup, providing another step for testing designs before beginning emulation.

Three hardware modules help make up the Mars emulation system, the DebugWare unit, the Logic Block Module (LBM), and the Pods. The DebugWare unit is a standalone part that supports three major functions. First, it acts as an emulation server that connects to an Ethernet LAN through its Ethernet interface, to connect many engineers in a team-oriented design emulation or proto-

type project. Second, it acts as a logic analyzer, providing 2000 trigger states, 576 probing channels with 64 kbits of storage per channel, and general-purpose probing. Last, as a functional tester, it supports datalog speeds (collecting and logging in data) up to 8 MHz with 64 kbits of storage.

The LBM is a general-purpose, reusable emulator based on the Xilinx 4000 series of FPGAs. A typical LBM supports 25-k-gate designs in a single configuration, or 50-k-gate designs with a dual-LBM configuration, both at up to 8-MHz clock rates. Each LBM supports 720 pins and 8 external clock sources.

The Pods act as the electrical and mechanical link between the LBM and the target-hardware system. Special data and clock Pods provide the necessary buffering between the LBMs and the target system, and connect the two with lightweight, flexible cables. In addition, 12 mA of drive current meets most of today's interface needs.

Modularity is built into the Mars II hardware so users can add capabilities as needed. Although the current Mars product is built with the Xilinx 4000 series of FPGAs, its architecture makes it possible to exploit the next generation of FPGA technology as it becomes available. Users can also mix older and newer technologies to upgrade while protecting their existing investments. □

### PRICE AND AVAILABILITY

*Available now, Mars II is offered as a package consisting of an emulation base and a debug base. Pricing varies depending on configuration. For example, a Mars II system with 50k gates, 100-pin emulation configuration, and 200 probes for debugging, costs \$98,000 for the debug base and \$108,000 for the emulation base. The debug base can be expanded in 100-probe increments that cost \$20,000 each. The emulation base can be expanded in 25k-gate increments costing \$54,000 each.*

*PiE Design Systems Inc., 757 N. Mary Ave., Sunnyvale, CA 94086-2909; (408) 738-8899.*

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How VALUABLE?	CIRCLE
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MODERATELY	551
SLIGHTLY	552

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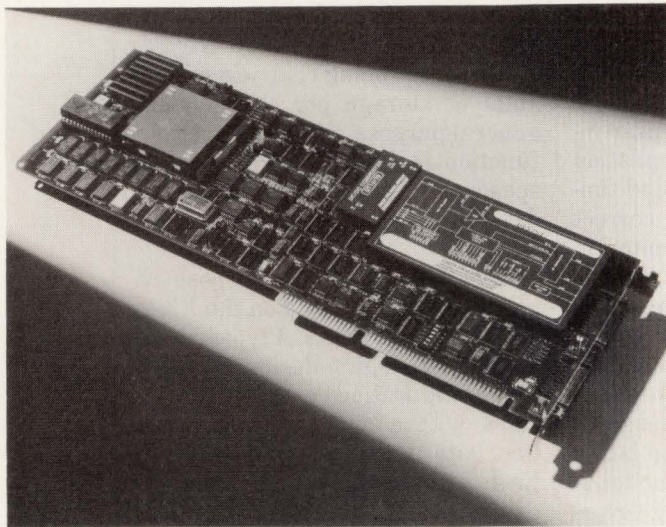
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RICHARD NASS

**E**ngineers working with personal computers typically have no trouble acquiring analog or digital data from their data-acquisition system. But they do have problems getting both analog and digital data at the same time. Data Translation has solved this dilemma with its DT3801 series boards. The mixed-signal simulation boards supply synchronized analog and digital stimuli while concurrently measuring the analog and digital response of a system under test. All subsystems can be clocked synchronously or totally independently. This is Data

Translation's first attempt at a mixed-signal board.

Mixed-signal boards similar to the DT3801 series do exist, but none operate in the PC environment, and most are aimed at the audio market. Some configurations contain digital-to-analog and analog-to-digital converter boards tied to a dedicated digital I/O board that can output digital patterns, but they can't supply synchronized analog and digital stimuli and capture a synchronized analog and digital response all on the same board.

The DT3801 family consists of three boards, the 3801-G, the 3808, and the 3809, each differing in reso-



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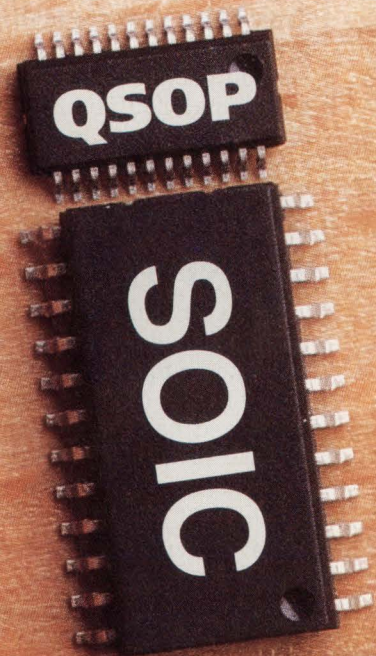


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2158	2273	2574	2834	158	273	574	834
2161	2299	2640	2841	161	299	640	841
2163	2373	2646	2843	163	373	646	843
2191	2374	2648	2845	191	374	648	845
2193	2377	2651	2854	193	377	651	854
2240	2533	2652	2861	240	533	652	861
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# MIXED-SIGNAL SIMULATION BOARDS

lution, throughput, and I/O arrangement. Each board is based on the Texas Instruments' TMS320C40 32-bit floating-point digital-signal processor. This part supplies the digital output (Fig. 1). The 320C40 contains six communication ports which Data Translation uses for multiprocessor arrangements. One of the ports can be multiplexed to communicate with additional 320C40s. Linking one 320C40 communication port to the communication port of a second 320C40 gives five extra communication ports by default.

## TIE DSP TO DMA

The DSP chip comes with a six-channel intelligent DMA controller that can be tied to each communication port. Hence, data doesn't have to be moved back and forth between 320C40 processors. This arrangement suits random data movement throughout each board. While each board employs all six communication

ports, it can also switch one port off to apply it to a second board for acceleration purposes.

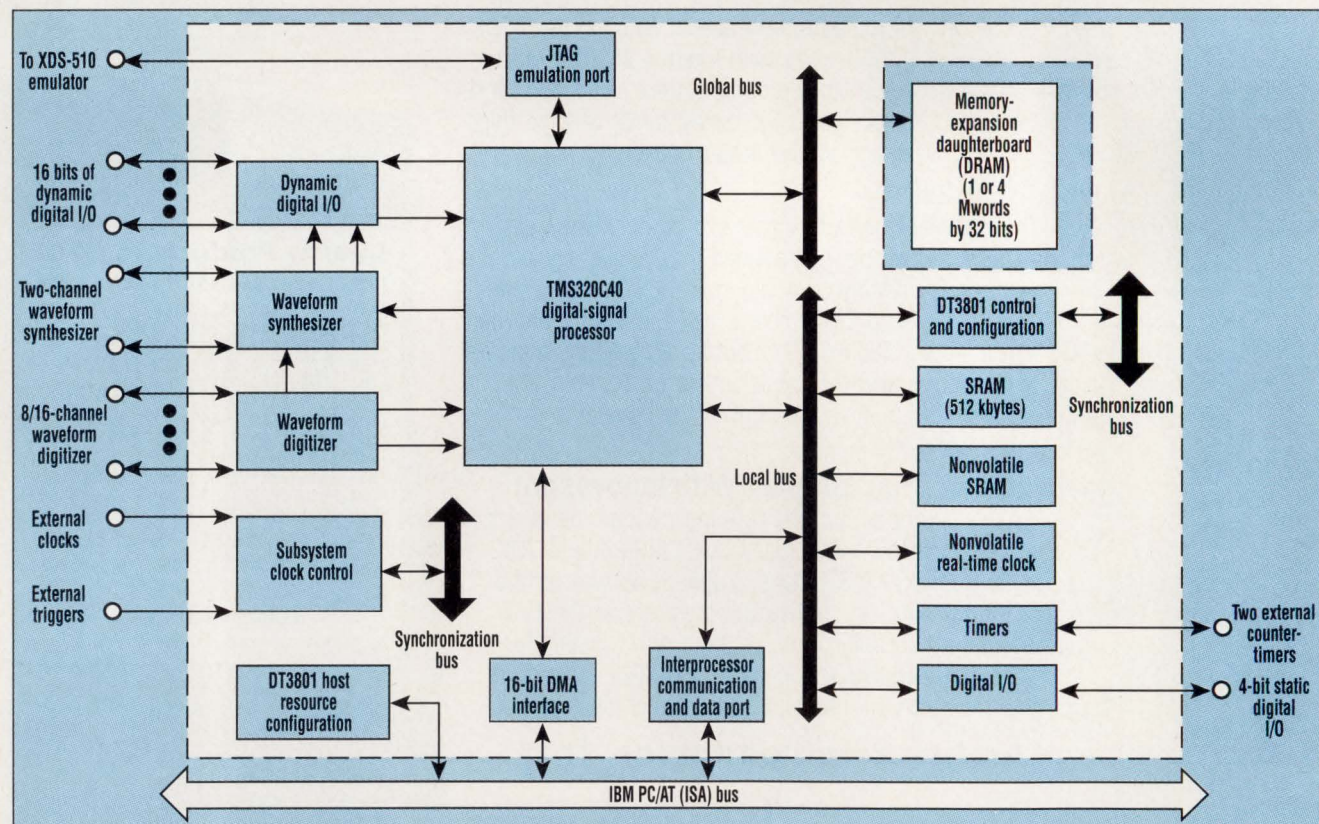
The 3801-G board offers a resolution of 12 bits, a throughput of 250 kHz, eight differential input channels, and comes with antialiasing filters. The 3808 board has a resolution of 16 bits, a throughput of 160 kHz, eight differential input channels, and simultaneous sample-and-hold capability. The 3809 board features a resolution of 12 bits, a throughput of 1 MHz, and 16 single-ended or 8 differential input channels.

Data Translation's designers paid particular attention to the design of each board's memory subsystem, especially the memory hierarchy and how communications should take place with the host. The boards' standard configuration includes 128 kbytes of zero-wait-state SRAM, which becomes the primary program execution area.

The boards will accommodate vari-

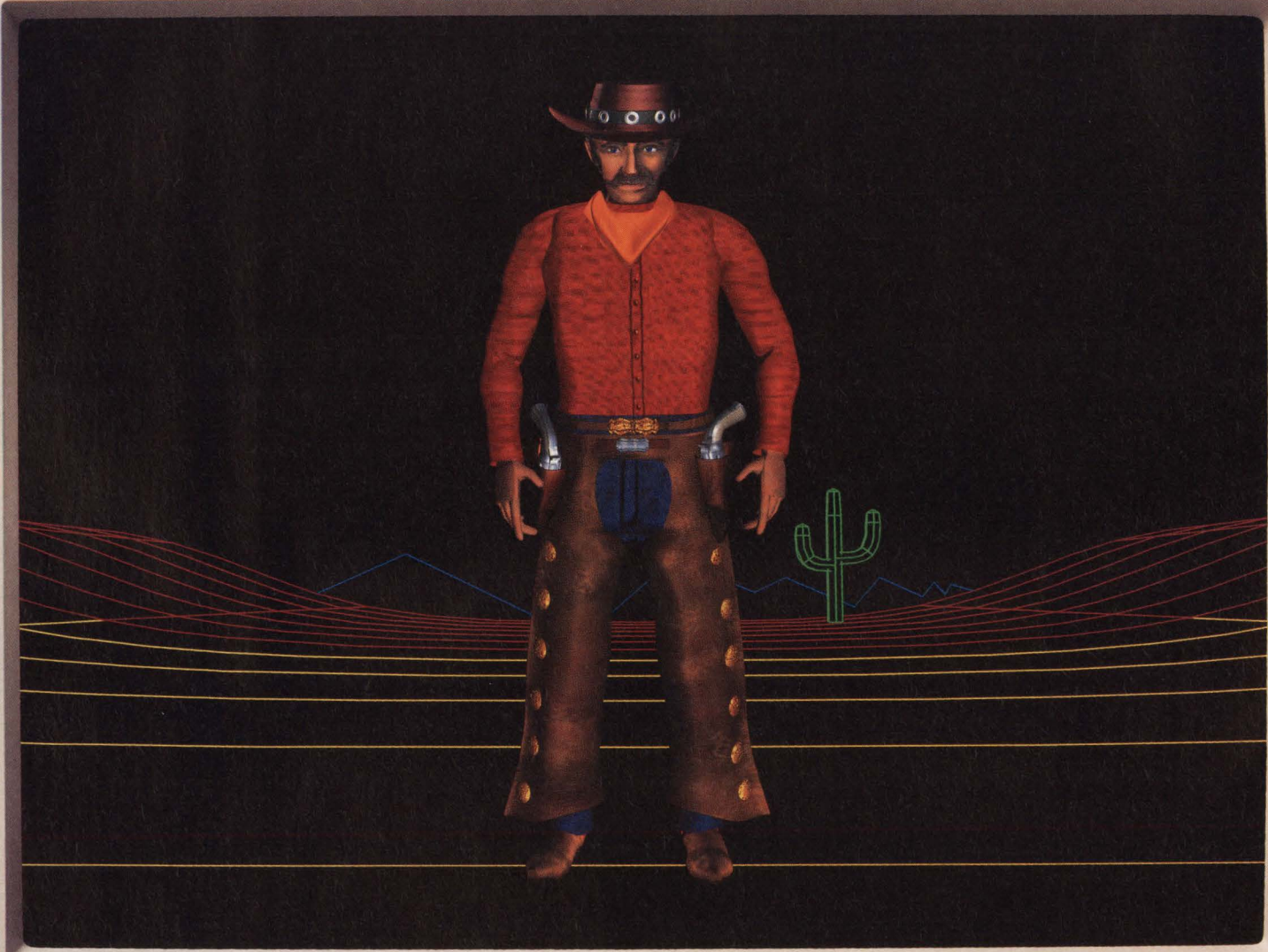
ous mezzanine cards. Initially, just memory cards will be available, serving as the primary data-storage space (Fig. 2). Here, users can download waveforms from the host and then operate directly from the 3801's on-board memory. An 8-kbyte non-volatile SRAM is also included so that once a device is configured, all configuration data is retained. Users can boot either directly from a PC or from one of the mezzanine cards. For an application in a harsh environment, such as on a factory floor, it would be more appropriate to boot from the card so rotating media could be eliminated.

The boards offload the task of data processing from the host. Once the program is downloaded to the board, it operates independently of the host. Typical data-acquisition boards acquire data into system memory, then let the PC processor handle it. But that processor typically isn't suited for intensive algorithm-



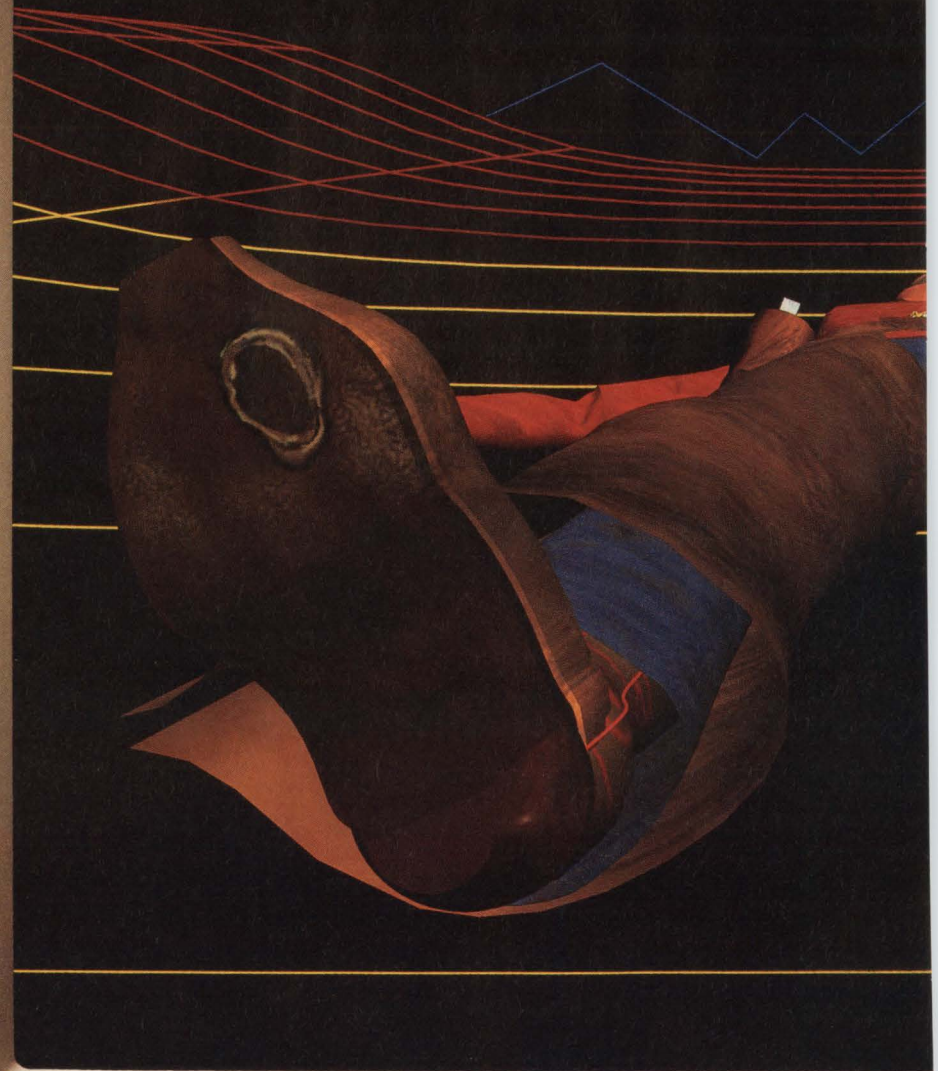
**2. MEMORY CAN BE EXPANDED** on Data Translation's DT3801 mixed-signal simulation boards by adding mezzanine boards. Data Translation will initially offer three modules: the EX1, EX2, and EX3. The EX1 supplies 4 Mbytes of DRAM while the EX2 supplies 16 Mbytes. The EX3 adds 4 Mbytes of DRAM plus EPROM for loading applications directly from the daughterboard.



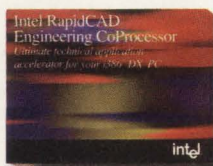


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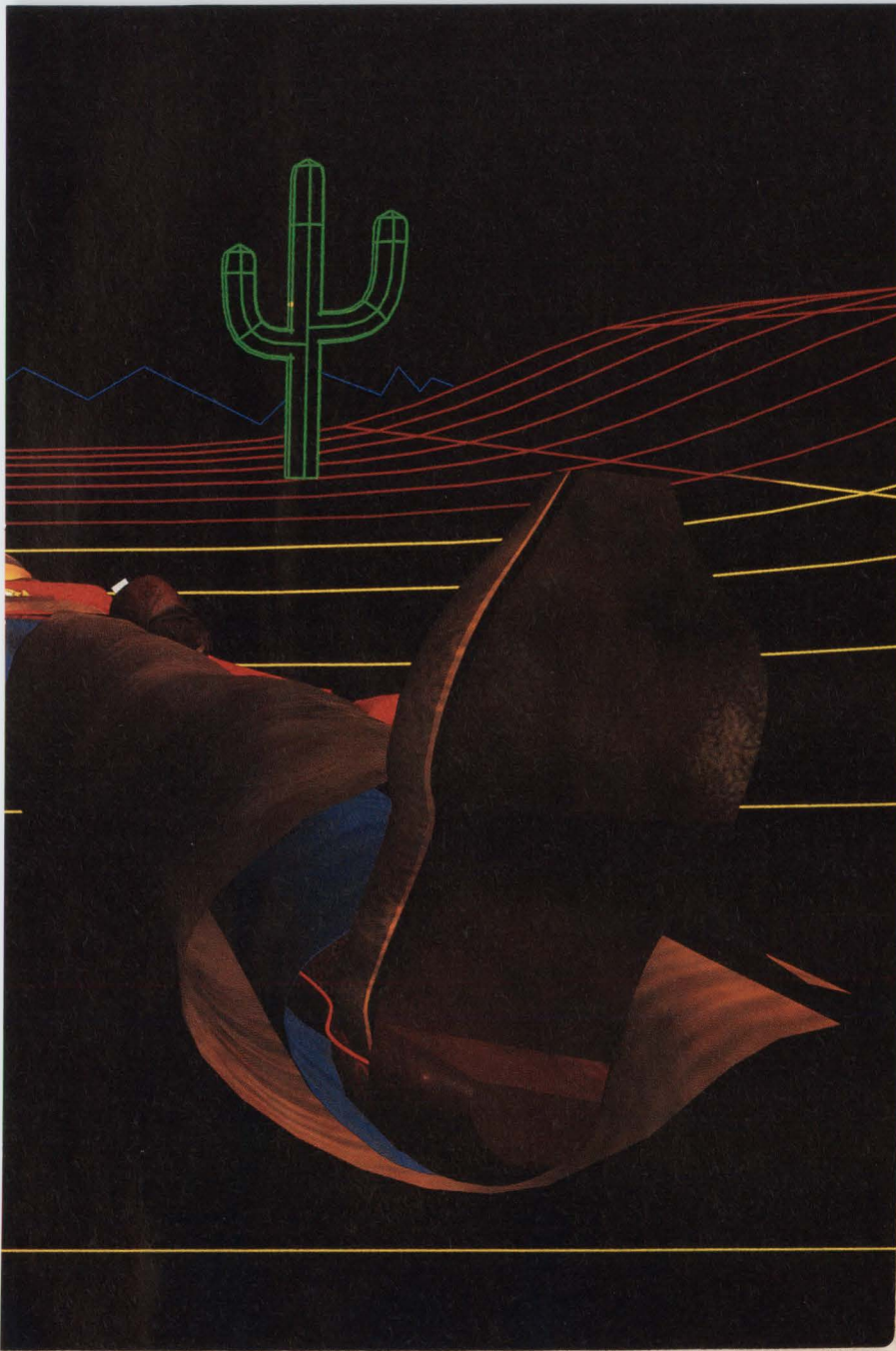
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CIRCLE 1



## MIXED-SIGNAL SIMULATION BOARDS

mic processing. Using the 3801, the data can be preprocessed by the 320C40 prior to sending it to the host. The 3801's DMA interface contains 16 bits, but 16 or 32 bits can be selectively passed from the DSP chip's memory space into the host. If it's a 32-bit quantity, the interface logic essentially makes two transfers to the host.

### DOS AND WINDOWS

Initially, the boards will operate in the native DOS environment. A Windows 3.0 version will follow shortly. The Windows version will be fully compliant with the company's recently announced DT-Open Layers specification (*ELECTRONIC DESIGN*, Feb. 6, p. 30). The design philosophy that was implemented for the software offered an easy migration path from the DOS product to a Windows product. Respinning it to work under Windows didn't require a major

overhaul.

Though Data Translation sees many engineers moving toward the Windows environment, it anticipates concerns regarding sustainable performance while operating under Windows, especially when transferring large blocks of data using direct memory access. In a Windows environment, there's a fixed DMA buffer size that degrades sustainable performance into system memory. Windows offers other inherent advantages, though, such as the ability to open multiple applications. But most users looking for pure performance should stick to the DOS version.

The board's objective is to rapidly move data so the 320C40 is free to do the intense algorithmic number crunching. Data Translation's designers worked with the SPOX operating system because it fit well with the architecture. SPOX, an industry-standard real-time DSP operating

system from Spectron Microsystems, Santa Barbara, Calif., supplies a multiprocessing kernel as well as device independence so that each subsystem looks the same from the SPOX vantage point. Hence, the direct memory access can be coordinated with just one or two calls from the application-programmer's level. In addition, SPOX supplies an extensive math library of DSP functions that can operate on the data.

Initially, three of Data Translation's existing daughterboards were ported to the 3801 family—others will follow. The EX1 contains 4 Mbytes of DRAM and the EX2 supplies 16 Mbytes of DRAM. The EX3 supplies 4 Mbytes of DRAM, but also adds EPROM that's used for booting applications from the daughterboard. The expansion memory can store output waveforms or acquired samples. It can also be used as a secondary program execution area for large applications. When the company decides to include a connection to DT-Connect II, it'll come through a module.

Other features of the boards include dual bidirectional message queues and a built-in nonvolatile real-time clock that time-stamps data sets in case a critical event occurs. A single 4-bit static digital I/O port controls external equipment when using the dynamic digital input and output subsystems in clocked mode. Two 16-bit counter-timers are included for rate generation and event counting. And a JTAG test port supplies full emulation support during application development.

### PRICE AND AVAILABILITY

All three boards in the DT3801 family are priced at \$5995. The DOS version will be available by the end of the summer and the Windows 3.0 version will come several months later. The EX1 expansion module costs \$995 each. Prices have not yet been set for the EX2 and EX3 modules.

Data Translation Inc., 100 Locke Dr., Marlboro, MA 01752; (508) 481-3700.


CIRCLE 514

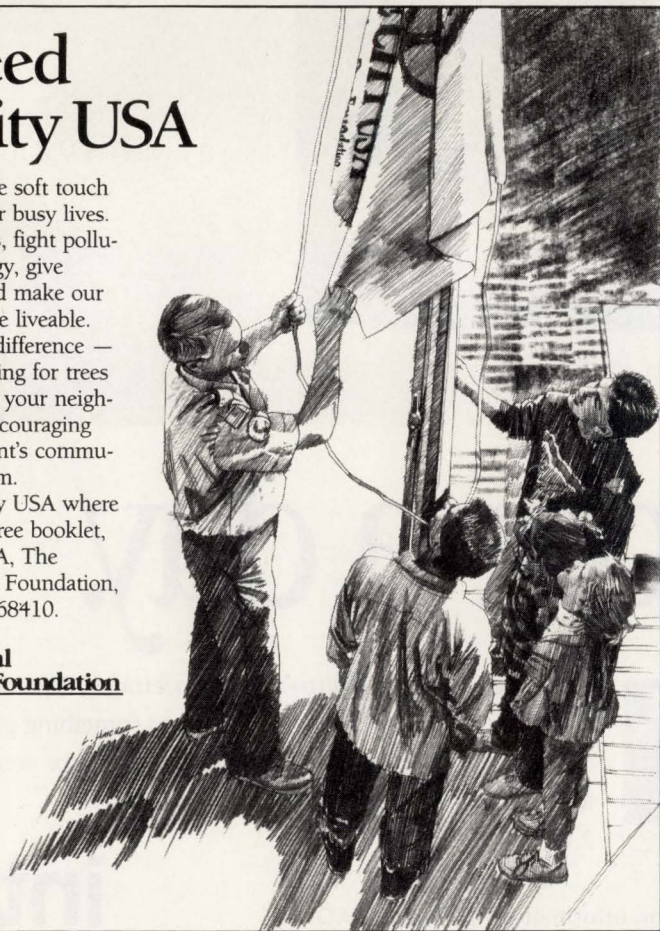
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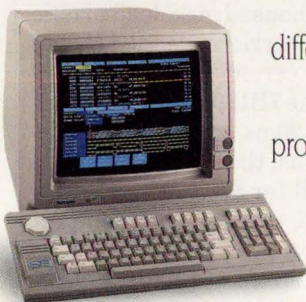


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# HIGHLY INTEGRATED CACHE-TAG RAMS

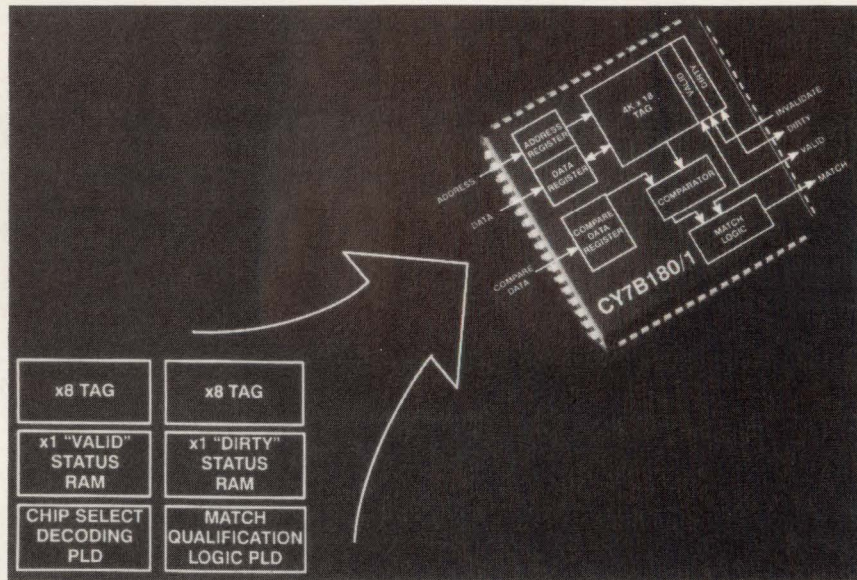
## PERFORM MATCHES IN 12 NS

DAVE BURSKY

The first cache-tag RAMs to offer 18-bit-wide outputs, the CY7B180 and 181 chips also integrate more of the required system-support logic onto the memory chip than other cache-tag memories. Organized as 4 kwords by 18 bits, the BiCMOS memories also have the fastest address-to-match times—just 12 ns—as well as 15-ns tag RAM access times. Those short times allow cache subsystems to operate at system clock speeds of 50 MHz. As a result, the chips are attractive for RISC as well as CISC system designs and for use even as cache data RAMs.

A typical cache containing 128 kbytes of storage and employing a 32-byte line size requires a 15-bit tag address. Now, with a single chip, not only can the 15-bit address (16 bits maximum) be supported, but the memory chips also have two additional bits that provide status information for each cache entry. Valid and dirty flags, for example, are implemented with the 7B181, which is optimized for uniprocessor applications. The 7B180 was optimized for multiprocessor system architectures and leaves the two bits uncommitted, allowing users to define their function. Previously two 8-k-by-8 or four 4-k-by-4 RAMs were required to provide the same capability.

To save designers board space, design effort, and improve performance, designers incorporated the cache status validation and chip-select decoding on the memory chips. That typically eliminates several additional circuits typically required in cache subsystems. For starters, the chips eliminate the need for a separate memory to store the valid and dirty status bits or the MESI (modified, exclusive, shared, invalid) status bits in multiprocessing systems. Further, by incorporating the decoding logic the 7B180 and 181 allow designers to cascade up to four chips (16 k lines of cache tag) without any performance penalty typically en-



countered with off-chip decoding.

Both ICs operate in clock or latch mode and have separate compare data and data ports, which allow the chips to perform a comparison and simultaneously read out the selected tag data in a single clock cycle. That improvement in memory architecture typically saves at least one clock cycle over previous cache-tag approaches. The older approach often requires two cycles to compare and read out tag data during a copy-back cache miss. The ICs' input address and data latches allow the memories to be easily integrated into pipelined architectures.

Both chips are also the first to offer independent access to the tag and status fields in the memory arrays. Such access capability eliminates the need to read out tag data and write it back into the tag memory when only the status bits must be changed. A separate I/O data port allows the transfers without interfering with the other operations of the chips.

To better support uniprocessor applications, the CY7B181 employs the Valid cache-status bit to qualify its Match Address signal. That eliminates the need for external logic to perform the qualification, and thus

improves overall response time. Circuits on the chip also allow all the valid bits to be cleared in only two cycles, rather than one bit per cycle. That allows the cache to be flushed faster and eliminated the need for an external resettable RAM. Write hits cause the chip's dirty bit to be set automatically, thus saving several cycles since the processor doesn't have to wait while the cache controller sets the tag's dirty bit.

The 7B180 chip, which is aimed at multiprocessor systems, has slightly different control logic. The user can define the two status bits to implement up to four states for the MESI protocol, ensuring cache coherency.

When running at top speed, the chips consume about 1.3 W. The chips can be housed in 68-lead plastic leaded chip carriers, leadless chip carriers, or ceramic pin-grid-array packages. The 7B180 and 181 come in 12-, 15- and 20-ns speed grades. In PLCC versions, the 7B180 and 181 in hundreds sell for \$72.05, \$43.20, and \$40.05 apiece, respectively. Samples are available now.

Cypress Semiconductor Corp.,  
3901 N. First St., San Jose, CA  
95134; Paul Fechtelkötter, (408) 943-2600.

CIRCLE 460



## NEW PRODUCTS

DIGITAL ICs

### NONVOLATILE RAMS STORE DATA 100 YEARS

**T**wo nonvolatile RAMs from Xicor automatically transfer static RAM data bit for bit to an on-chip EEPROM at power down and automatically reload the preserved EEPROM data into RAM when power is restored. Both CMOS, floating-gate devices complete a store operation in 5 ms or less. The EEPROM, which retains data for 100 years or more, is specified for 1 million store cycles. The RAM has unlimited write operations. The X20C16 2-kword-by-8-bit NOVRAM is available with 35-, 45-, and 55-ns access times. Data recall from EEPROM takes 10  $\mu$ s or less. The 5-V chip draws 100 mA active current and 250  $\mu$ A in standby. In thousands, the 55-ns part is available now in the commercial temperature range for \$19.69 and \$18.71 each in 28-pin Cerdip and plastic DIP packages, respectively. The Mil-Std-

883 Cerdip costs \$49.23 in the same quantity.

Xicor's X24C45 serial NOVRAM has a 16-word-by-16-bit static RAM overlaid with an EEPROM array. It has 2- $\mu$ s or less recall. Active current is 10 mA; standby current is 50  $\mu$ A. The chip's serial port is compatible with single-chip microcomputers such as the COPS from National Semiconductor Corp. and the 8051. Package options are 8-pin miniDIP and 8-lead SOIC. In the commercial temperature range, 1000-piece prices are \$1.44 and \$1.55 each for the DIP and SOIC packages, respectively. Industrial temperature range pricing is \$1.68 and \$1.85 each in the same quantities for the plastic and SOIC packages, respectively.

*Xicor Inc., 851 Buckeye Ct., Milpitas, CA 95035-7493; (408) 432-8888.*

**CIRCLE 461**

■ MILT LEONARD

### PROGRAMMABLE CLOCK IC GENERATES 275 MHZ

Implementing an on-chip phase-locked loop that generates timing signals of up to 275 MHz, the Bt440 programmable clock chip from Brooktree can supply timing signals for high-resolution graphics monitors. An enhanced version of the Bt438, the Bt440 clock chip's programmable nature lets it take advantage of a low-frequency crystal. Then the chip can multiply the basic clock frequency by a factor of 8, 16, 20, or 32 to generate the pixel clock signals that drive the RAMDACs.

As a result, the programmability allows a single crystal to generate timing for 1152-by-900, 1280-by-1024, and 1600-by-1280 pixel monitors with less than 1-ns of jitter. The chip also generated four load clocks at one-fourth the clock speed to drive the external video RAM's additional RAMDACs. That allows the use of the same frame buffer architecture across different monitors or platforms. A reset function included in the programmable clock chip allows it to fix the number of pipeline levels for the company's RAMDACs. Housed in a 28-lead PLCC, the Bt440 programmable clock chip sells for \$25 apiece in lots of 100. Samples of the clock chip are immediately available.

*Brooktree Corp., 9950 Barnes Canyon Rd., San Diego, CA 92121; Allyn Pon: (619) 452-7580.*

**CIRCLE 462**

### MCU DEVELOPMENT TOOLS TRIM START-UP COST

Aimed at reducing the cost of developing applications, a starter kit for the ST6210 and 6215 8-bit microcontrollers takes advantage of low-cost PC AT-compatible computers. The kit consists of a small development board/programmer for the EPROM versions of the microcontrollers, a cable to tie the board into the PC's printer port, software for the user-supplied PC, data books and four EPROM-based MCUs. The software consists of an assembler, linker, simulator, and the interface to drive the programmer. Several software application modules that users can copy and link into their applications are also included. The ST6210/6215 controllers include 64 bytes of data RAM, an 8-bit timer with 7-bit prescaler, a watchdog timer, and an 8-bit a-d converter with either 8 (6210) or 16 (6215) analog inputs. The ST6210 comes in a 20-pin package and has 12 programmable I/O lines; the 28-pin ST6215 has 20 programmable I/O lines. Both chips come with 2 kbytes of UV-EPROM storage and for production, the chips can be had in ROM-based or one-time programmable options. Kits for either the 6210 or 6215 sell for \$299 apiece.

*SGS-Thomson Microelectronics, 1000 E. Bell Rd., Phoenix, AZ 85022; Graham Trickey: (602) 867-6100.*

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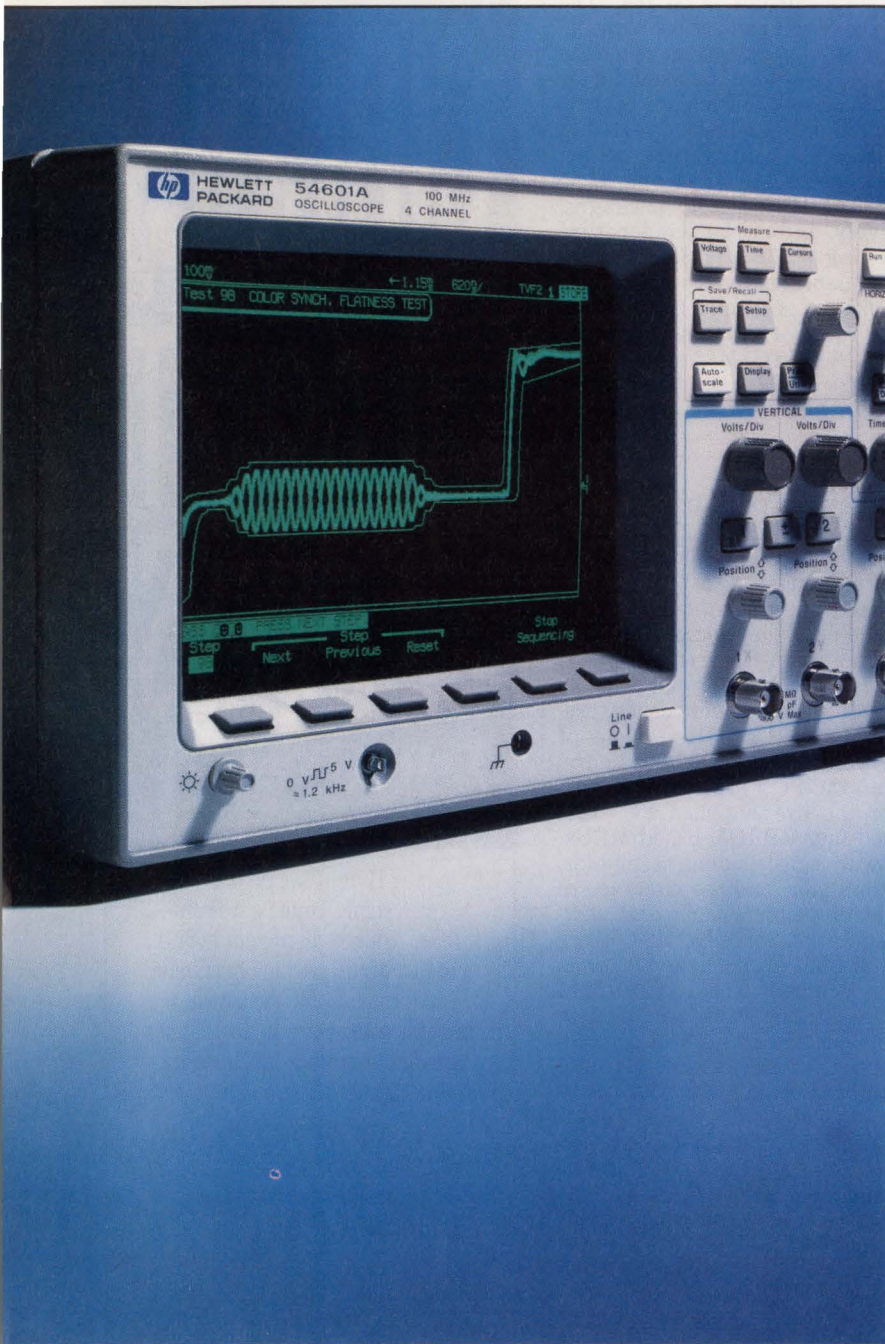
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## NEW PRODUCTS

DIGITAL ICs

### FAMILY OF GAAS LOGIC CHIPS CLOCKS AT 10 GHZ

Claiming the highest operating frequency for any family of logic chips, the NLG41xx and 42xx family of gallium-arsenide logic circuits has a maximum clock input frequency of 10 GHz. Like the previously available GaAs logic chips from NTT Electronics Technology Corp., Tokyo, and offered in the U.S. by KBK, the new family can tie directly into either ECL or source-coupled FET logic and operates from a single -3.5-V supply.

Eleven chips are planned for both the 41xx and 42xx families. Chips in the families have signal rise and fall times in the 35- to 55-ps range, depending on the chip. Initial functions to be released include the 4120 1:2 clock distribution circuit; the 4119, a two-input AND/NAND gate; the 4101, a master-slave D flip-flop; the 4103, a two-input XOR/XNOR gate; the 4115, a 2:1 input selector; and the 4122, a 1:2 demultiplexer with reset. All of the chips have maximum operating frequencies of 10 GHz except for the 4115, which has a maximum speed of 18 Gbits/s. All the 41xx-family chips come in 28-lead TB-28 ce-

ramic leaded packages that can be surface-mounted.

In the NLG42xx series are more complex functions—the 4219, a 1:4 demultiplexer with reset, and the 4218, a 4:1 multiplexer with reset. They are housed in 32-lead ceramic surface-mountable packages (type SE-32). Functions not yet available but slated for release later this year include a T flip-flop, a 2:1 multiplexer, and a two-input OR/NOR gate.

Power consumption for the 41xx family ranges from 1.3 W for the NLG4103 to about 2 W for the NLG4122. The 4219 and 4218 have respective power drains of 2.7 and 3 W. Samples of most chips are now available and range in price from \$1500 to \$3000 apiece in small quantities. The older NL45xx, 46xx, and 47xx series chips have operating frequencies that range from 2 to 8 GHz, and prices that range from \$400 to \$1600/chip.

*KBK Inc., Paramount Plaza, Ste. 1206, 3550 Wilshire Blvd., Los Angeles, CA 90010; (213) 389-9406.*

CIRCLE 464

DAVE BURSKEY

### FFT PROCESSOR FITS ON ONE CHIP DOES 1024 POINTS IN 97 $\mu$ S

A self-contained processor that performs fast Fourier transforms, the PDSP 16510 can act as a stand-alone signal processor or as a slave processor to a host system. The chip's internal memory can hold data sets for up to 1024 real or complex points and can compute a full 1024-point complex FFT in just 97  $\mu$ s. That speed is equivalent to a processor delivering 450 MIPS and a data sampling rate of 6.8 MHz. The GEC Plessey FFT processor can also perform 16, 64, and 256-point transforms. Up to six FFT chips can also be connected in parallel to achieve even higher throughputs and boost the data sampling rate to a maximum of 40 MHz.

Data and coefficients are both represented by 16-bit words. And block floating-point computations are done to extend the dynamic range of the FFT chip. The large internal RAM that holds the data points removes the memory-transfer bottleneck in building-block approaches that use off-chip memory.

When operated in its continuous mode, the FFT processor simultaneously employs three on-chip control units that concurrently allow new data to be loaded, current data to be transformed, and previous results to be output. No external buffering is needed for transforms of up to 256 points—the PDSP 16510 can be connected directly to an a-d converter and operate continuously. Data blocks can be overlapped by either 0, 50%, or 75%.

When processing complex data, the circuit delivers the real and imaginary components of the frequency bins. Those values can be fed directly into a circuit such as the PDSP 16330 Pythagorean processor to derive the magnitude and phase angle directly from the data. The PDSP 16510 comes in an 84-lead pin-grid-array package. In thousands the chip sells for \$595 apiece. Samples are available from stock.

*GEC Plessey Semiconductors, 1500 Green Hills Rd., Scotts Valley, CA 95067; (408) 438-2900. CIRCLE 465*

DAVE BURSKEY

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## NEW PRODUCTS

DIGITAL ICs

### FAST PLDS CUT DELAYS TO 7.5 AND 10 NS

Employing electrically erasable configuration cells, the PALCE16V8 and PALCE22V10 are fast, direct replacements for the popular 20-pin GAL and 24-pin 22V10 devices. The 7.5-ns propagation delay of the 16V8H-7 suits it for systems with clock speeds of 100 MHz, making it one of the fastest GAL devices available. It is also pin, function, and fuse-map compatible with the GAL devices. With its 10-ns propagation delay, the 22V10H-10 allows system speeds to hit 83 MHz, the highest speed yet for a CMOS implementation of the 22V10 architecture. The PALCE22V10H-10 comes in 28-lead PLCCs and 24-pin DIPs and sells for \$14.60 apiece in 100-unit lots; the PALCE16V8H-7 comes in 20-lead PLCCs and DIPs and sells for \$5.25 apiece in 100-unit lots. Both chip types are available from stock.

*Advanced Micro Devices Inc., 901 Thompson Place, P. O. Box 3453, Sunnyvale, CA 94088-3453; (408) 749-5703. CIRCLE 466*

### SPACE-SAVING PACKAGE DOUBLES VRAM DENSITY

By squeezing two chip cavities onto a single vertical-in-line ceramic package, the MVM8256V doubles the effective storage density of systems employing 1-Mbit video RAMs. Military and industrial versions of the 40-pin 2-Mbit memory have access times of 100, 120, or 150 ns on the DRAM port and 25 to 35 ns for the video port. The 0.1-in-wide VIL package occupies minimal board space and short of a multichip module offers the highest memory packaging density for military applications. The fastest speed grade, processed to Mil-Std-883, sells for \$310 apiece in hundreds. Production quantities will be ready 8 to 10 weeks after ordering.

*Mosaic Semiconductor Inc., 7440 Carroll Rd., San Diego, CA 92121; John Guerrero: (619) 271-4564. CIRCLE 467*

### 32-BIT-WIDE FIFO MEMORY PACKS 32 KBYTES

Organized as 1 kword by 32 bits, the PDSP 16540 first-in/first-out memory

can serve as a flexible data buffer in any wide word system. Designed to support the GEC Plessey PDSP 16510 fast-Fourier transform processor, the FIFO memory nonetheless can tie into most CPUs. The PDSP 16540 FIFO memory can sustain data-read rates of up to 40 MHz from the read port and data-write rates of up to 16 MHz on the write port.

The number of words that can be read as a sequential block can be programmed in multiples of 32 words, up to a maximum of the entire 1024-word address space. Furthermore, a user can define the number of words to be re-read before new data is added. As a result, a designer has at hand a versatile solution for data-block overlapping—a technique often used in FFT processing. The wide 32-bit input and output buses afford fast data movement. Housed in an 84-lead pin-grid-array package, the CMOS chip sells for \$211 apiece in thousands. Samples are available from stock.

*GEC Plessey Semiconductors, 1500 Green Hills Rd., Scotts Valley, CA 95067; (408) 438-2900. CIRCLE 468*

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## Small Company's New Golf Ball Flies Too Far; Could Obsolete Many Golf Courses

Pro Hits 400-Yard Tee Shots During Test Round

Want To Shoot An Eagle or Two?

By Mike Henson

MERIDEN, CT — A small golf company in Connecticut has created a new, super ball that flies like a U-2, putts with the steady roll of a cue ball and bites the green on approach shots like a dropped cat. But don't look for it on weekend TV. Long-hitting pros could make a joke out of some of golf's finest courses with it. One pro who tested the ball drove it 400 yards, reaching the green on all but the longest par-fours. Scientific tests by an independent lab using a hitting machine prove the ball out-distances major brands dramatically.

The ball's extraordinary distance comes partly from a revolutionary new dimple design that keeps the ball aloft longer. But there's also a secret change in the core that makes it rise faster off the clubhead. Another change reduces air drag. The result is a ball that gains altitude quickly, then sails like a glider. None of the changes is noticeable in the ball itself.

Despite this extraordinary performance the company has a problem. A spokesman put it this way: "In golf you need endorsements and TV publicity. This is what gets you in the pro shops and stores where 95% of all golf products are sold. Unless the pro uses your ball on TV, you're virtually locked out of these outlets.

TV advertising is too expensive to buy on your own, at least for us.

"Now, you've seen how far this ball can fly. Can you imagine a pro using it on TV and eagle-ing par-fours? It would turn the course into a par-three, and real men don't play par-three's. This new fly-power forces us to sell it without relying on pros or pro-shops. One way is to sell it direct from our plant. That way we can keep the name printed on the ball a secret that only a buyer would know. There's more to golf than tournaments, you know."

The company guarantees a golfer a prompt refund if the new ball doesn't cut five to ten strokes off his or her average score. Simply return the balls — new or used — to the address below. "No one else would dare do that," boasted the company's director.

If you would like an eagle or two, here's your best chance yet. Write your name and address and "Code Name S" (the ball's R&D name) on a piece of paper and send it along with a check (or your credit card number and expiration date) to National Golf Center (Dept S-203), 500 S. Broad St., Meriden, CT 06450. Or phone 203-238-2712, 8-8 Eastern time. No P.O. boxes, all shipments are UPS. One dozen "S" balls cost \$24.95 (plus \$3.00 shipping & handling), two to five dozen are only \$22.00 each, six dozen are only \$109.00. You save \$55.70 ordering six. Shipping is free on two or more dozen. Specify white or Hi-Vision yellow.

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## NEW PRODUCTS

ANALOG

### VIDEO-BAND IC OP AMP ADDS 60-DB OF DC GAIN CONTROL

**C**lean gain control of wideband or fast signals—no trivial task—becomes especially difficult if the wideband signal source is remote from the site of the gain-setting signal. This holds true whether it is fixed or variable, manual or system generated. And as the required bandwidths for video and fast precision pulses climb to new highs, “remote” can come to mean a few inches of printed-circuit board. Linear Technology’s LT1228 video-band op amp IC supplies that remote gain-control function.

This IC, in its 8-pin DIP, consists of a differential-input, variable transconductance (current-to-voltage or  $g_m$ ) amplifier ahead of the company’s 100-MHz current-feedback op amps, the LT1229 and LT1230. The gain of the transconductance stage is varied 60 dB by changing the current into its  $I_{SET}$  pin from 1  $\mu$ A to 1 mA. The current can be “set” by a fixed or variable resistor connected to a fixed or variable volt-

age. Or a voltage or current-output d-a converter can control the current via digital words from a host microprocessor or microcontroller.

The  $g_m$  stage provides a small-signal bandwidth from dc to 75 MHz, nicely complementing the 100-MHz current-feedback op amp that follows it. The current output of the  $g_m$  stage drives an on-chip resistor. The signal voltage developed across it is applied to the plus input of the op amp. This op amp input, as well as the minus input are brought out to pins on the IC for setting gain independently of the gain of the  $g_m$  stage. The characteristics of the op amp are virtually identical to those in the LT1229 and LT1230. The LT1228 can also be used to build video faders, AGC amplifiers, tunable filters, and oscillators. In quantities of 100, they cost \$3.95 each.

*Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 637-5545* **CIRCLE 469**  
**■ FRANK GOODENOUGH**

### 150-MHZ RGB AMPLIFIER-SYSTEM IC FEEDS HIGH-RESOLUTION CRTS

**W**ith the use of National’s LM1204 RGB (red-green-blue) three-channel video amplifier, designers can cut the dimensions of a driver board for high-resolution color CRTs from 11 in. by 11 in. to just 5 in. by 5 in. As a result, the board can fit next to the neck of the CRT. The LM1204 amplifier cuts board size by slashing the number of discrete components required on the board. Each of the 3.5-V pk-pk RGB outputs of the IC sports a 3-dB bandwidth of 150 MHz, while providing up to 20 dB of gain for each channel.

Each output is designed to feed the typical discrete-transistor video amplifier used to drive the CRT’s cathodes. That performance lends it to monitors for XGA (1024 by 768 pixels), VESA, and CAD (1280 by 1024 pixels), and even 1600 by 1280-pixel systems. The smaller board not only saves space, but also simplifies board design and cost (parts, manufacturing, and test), and makes it easier to shield the circuit from interference. A true system-on-a-chip, the LM1204 amplifier system IC further

cuts board size by processing all the other signals feeding the CRT.

Besides three matched RGB amplifiers, the amplifier IC contains a de-voltage-controlled contrast control, de-voltage-operated drive control for each amplifier, and a dual clamping system for both brightness control and video blanking.

The chip also contains a back-porch clamp-pulse generator activated by an external  $\pm H/HV$  sync or composite video signal. The IC runs off 12 V and the dc control voltages are from 0 to 4 V, easily generated with 8-bit digital-to-analog converters from a serial digital bus. The commercial grade LM1204 comes in a 44-pin PLCC and goes for \$6.85 in hundreds. A military version is expected in the fall. The LH2426 IC, a three-channel high-voltage CRT driver—for use between the LM1204 and CRT cathodes—is expected to be released shortly.

*National Semiconductor Corp., P. O. Box 58090, Santa Clara, CA 95052-8090; Peter Himes, (408) 721-7517.* **CIRCLE 470**  
**■ FRANK GOODENOUGH**

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CIRCLE 217 FOR RESPONSE OUTSIDE THE U.S.



## NEW PRODUCTS

ANALOG

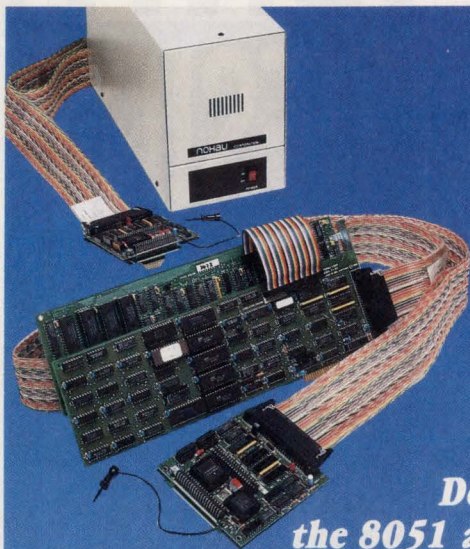
### IC PLL SYNTHESIZES FREQUENCIES TO 1.1 GHz

The CMOS MC145191 phase-locked loop synthesizes clock frequencies to 1.1 GHz. Its phase/frequency detectors are optimized for operation from a single 5-V rail, and it draws 7 mA. It

uses a byte-oriented format for operation with its 4-MHz data-rate serial interface port. Its proprietary bit-grabber registers don't require address/steering bits for random access to the three registers. Tuning is accomplished via a 3-byte serial transfer to the 24-bit "A" register, which is com-

patible with standard serial interfaces. On-chip circuits support an external crystal and a programmable reference output. Standby current in the sleep mode is 50  $\mu$ A. The MC145191 comes in a 20-pin SOG package and runs \$5.50 each in lots of 500.

**Motorola Digital-Analog Integrated Circuits Div., P. O. Box 6000, Austin, TX 78762; (800) 521-6274 CIRCLE 471**



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The full-blown simulator is an extension of the DEMO. You can load up to 64K of code and use 64K of XDATA space. You can program an "external environment" to interact with your code to simulate your target system. The emulator is the hardware extension of the simulator!

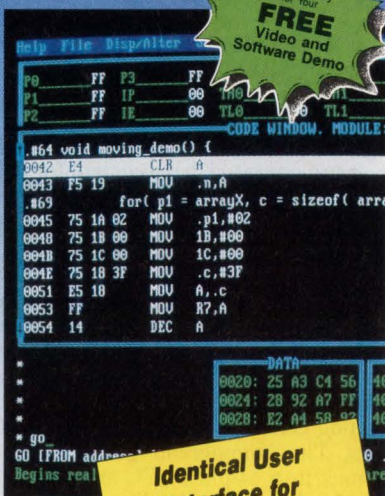
### In-Circuit Emulation

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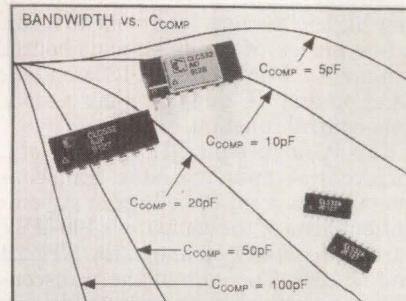
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### ANALOG MULTIPLEXER SWITCHES IN 17 NS



With active input and output stages, the CLC532 two-input analog multiplexer IC switches the output between inputs in under 20 ns. The -3-dB bandwidth for a 2-V pk-pk output is a minimum of 21 MHz, and increases to 140 MHz for a 100-mV pk-pk output. Changing the compensation capacitor alters the bandwidth and the differential gain and phase. Maximum output-settling time for a 2-V step to 0.01% of final value is 24 ns. The CLC532 comes in a 14-pin DIP. Commercial-grade units run \$13 each in thousands.

**Comlinear Corp. 4800 Wheaton Dr., Fort Collins, CO 80525; Alan Hansford, (303) 226-0500. CIRCLE 472**

### OP AMP SWITCHES INPUTS IN UNDER 10 NS

Sporting a pair of TTL-selectable, true-differential inputs, Burr-Brown's OPA676 SWOP amp (switched-input op amp) measily handles a variety of high-frequency multiplexing applications. It switches inputs in under 10 ns and typically can settle to 0.01% of final value for a 625-mV output step in under 25 ns (outputs settle to 0.1% and 1% in 15 and 9 ns, respectively) and offers minimum full power bandwidth of 25 MHz. Applications include programmable-gain amplifiers, synchronous demodulators and active filters. In a 16-pin DIP, and quantities of 100, the military grade OPA676 goes for \$78.40 each, the commercial grade for \$23.94 each.

**Burr-Brown Corp., P. O. Box 11400, Tucson, AZ 85734; John Conlon, (800) 548-6132. CIRCLE 473**

Australia (02) 654 1873, Austria (0222) 38 76 38, Benelux +31 1858-16133, Canada (514) 689-5889, Czechoslovakia 0202-2683, Denmark (42) 65 81 11, Finland 90-452 1255, France (01)-69 41 28 01, Germany 08131-25083, Great Britain 0962-73 31 40, Greece 01-862-9901, Hungary (1) 117 6576, Israel (03) 48 48 32, Italy (011) 771 00 10, Korea (02) 784 784 1, New Zealand (09) 392-464, Portugal 01-80 9518, Norway 02-649050, Singapore (065) 284-6077, Spain (93) 217 2340, Sweden 040-9224 25, Switzerland (01) 740 41 05, Taiwan (02) 7640215, Thailand (02) 281-9596, Yugoslavia 061 621066

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CIRCLE 133 FOR RESPONSE OUTSIDE THE U.S.



## NEW PRODUCTS

INSTRUMENTS

### POWER SUPPLY TESTER SIMULATES REAL CONDITIONS

**T**he FlexStar 8000 is a dual-output power supply tester that helps engineers test power supplies in realistic environments and under a variety of load conditions. The system can generate two independent loads simultaneously, simulating everything from static loads to complex current profiles.

In addition, the 8000 can measure the current profiles of actual system loads,



such as a disk drive during spin-up. Users can store these profiles in the tester's nonvolatile memory so they can be used in later tests to simulate actual conditions. The system can measure the input ac voltage and current to the supply under test and can calculate its efficiency under variable loads. Or it can control the ac power while measuring the supply's output current and voltage. Other measurements include baseline voltage, voltage regulation from minimum to maximum, transient responses, response time, ac noise and ripple, ac noise on two bandwidths, and dc ripple from 1 to 1000 Hz. Users can set ac power thresholds and employ the 8000 as a power-line monitor, so that power spikes or dropouts can be time stamped.

The tester measures 15-by-4-by-15 in. and weighs only 20 lbs. Its internal rechargeable batteries will operate the system for up to 4 hrs.

The FlexStar 8000 power supply tester is priced under \$10,000 and is available 30 days after receipt of an order.

*FlexStar, 2040 Fortune Dr., Suite 101, San Jose, CA 95131-1823; (408) 433-0770. CIRCLE 474*

■ JOHN NOVELLINO

### CARD OFFERS 500-MHZ TIMING, 100-MHZ LOGIC ANALYSIS

**T**he HP 16550A logic analysis card supplies up to 100-MHz state and 500-MHz timing capability to the HP 16500A modular logic analysis system. Each card offers 102 channels with a 4-ksample/channel memory. Two cards can be connected to deliver 204 channels or 102 channels with an 8-ksample memory.

The new card can cross-trigger other card sets in the mainframe, so users can analyze multiple microprocessors in the same design simultaneously. For maximum readability and time correlation, the card interleaves listings and/or waveforms between analysis modules. Also, the card's fast setup-and-hold specification makes possible measurements on designs that use devices with short data-valid windows. The unit has a 3.5-ns setup and 0-ns hold (3.5/0) specification, which can be adjusted to 0/3.5 ns in 500-ps steps.

All HP 16550A channels can perform

state or timing analysis, so users do not have to reprobe the system to change between analysis modes. The card can do 500-MHz conventional timing on half its channels or 250 MHz on all channels. It also does 250-MHz transitional timing on half channels or 125 MHz on all channels. Up to five cards can be installed in one mainframe to create a 510-channel logic analyzer.

Trigger features include 12-level, 125-MHz sequencing with 10 pattern terms, two 32-bit range terms, two timers, and two glitch/edge detectors that can be used for state as well as timing triggering. The card can detect 3-ns glitches.

The HP 16550A logic analysis card costs \$8800, and the HP 16500A system mainframe costs \$7700. Delivery is 4 to 6 weeks for both.

*Hewlett-Packard Co., 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. CIRCLE 475*

■ JOHN NOVELLINO

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## NEW PRODUCTS

INSTRUMENTS

### IEEE-488



Control any IEEE-488 (HP-IB, GP-IB) device with our cards, cables, and software for the PC/AT/386, EISA, MicroChannel, and NuBus.

### D-A BOARD UPDATES 16 CHANNELS WITHOUT SKEW

The PC-422 digital-to-analog boards update all 8 or 16 channels simultaneously with no time skew between channels. Each analog output channel delivers 12-bit resolution and a 3- $\mu$ s settling time, for a 330-kHz update rate. A special buffering feature allows all channels to be updated at a 1-MHz rate using block transfers or direct memory access. The boards run on IBM PC/ATs and compatibles. In single quantities the 8-channel PC-422A costs \$995, and the 16-channel PC-422B is \$1695. A software utility, PC-422SET, that exercises the board completely, including a disk file playback mode, costs \$50. Delivery is in 4 weeks.

**Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000. CIRCLE 476**

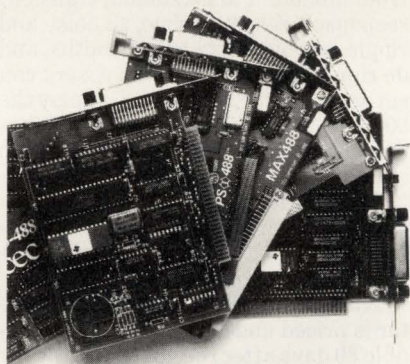
### UNIT ACQUIRES DATA ON ETHERNET WORKSTATIONS

An Ethernet-based data-acquisition device, the I/O Station 464, allows workstations to capture test data directly so that the workstation can immediately analyze the data at high speed. Other advantages of connecting the data-acquisition device directly to a workstation include multiple user access and Ethernet's ability to connect up to 500 m. of cable. The I/O Station 464 has four IEEE-P996 slots for plug-in modules. The unit accommodates up to 64 analog input, 32 analog output, 640 digital I/O, or 96 counter-timer channels. The modules can acquire data at resolutions to 16 bits and rates to 1 MHz. The I/O Station 464 costs \$3995 in single quantities and is available with 4-week delivery starting June 15. Volume discounts are available.

**Strawberry Tree Inc., 160 S. Wolfe Rd., Sunnyvale, CA 94086; (408) 736-8800. CIRCLE 477**

### LOGIC ANALYZER-PATTERN GENERATOR-RUNS ON PCS

The R3700 is a PC-based combination pattern generator and logic analyzer. The unit features 2-ksample/channel buffers, 32 data channels, 4 three-state channels, and 1 trigger channel. Clock, gate, three-state, and strobe signal inputs allow external control of the instrument. By using the included turn-key software, operators can quickly set up any stimulus pattern and output that pattern to the board under test in a



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single-shot, continuous, or burst mode. Outputs are TTL- and CMOS-compatible and can be delayed by the user. Output files are available in ASCII, hex, decimal, octal, or binary form. The unit runs on any IBM PC or PS/2 through the parallel port. The R3700 costs \$2995 and is available immediately.

**Rapid Systems Inc., 433 N. 34th St., Seattle, WA 98103; (206) 547-8311.**

**CIRCLE 478**

### QFP CLIPS PERMIT FAST TESTING OF NEWEST ICs

The Flexible Interface Network series of QFP test clips offers users fast, easy-to-access test connections with the latest surface-mounted, through-hole, or socket-mounted ICs. The clips come in three pin counts—100, 132, and 196—for Jeduc plastic or ceramic QFPs. Each size comes in three styles. One features a platform with 0.100-in. headers for industry-standard (IDC)

connector cables. The second has 0.050-in. connectors on flexible circuitry for direct attachment to an emulation board. The third style has an FIN clip with integral 0.050-in. connectors for most instrument ribbon cable assemblies. In lots of 1 to 9, prices range from \$396.67 for the 100-pin Model 5775 to \$615 for the 196-pin Model 5783. Delivery is from stock.

**ITT Pomona Electronics, 1500 E. Ninth St., Pomona, CA 91769; (714) 469-2900. CIRCLE 479**

### POD ADAPTS EMULATOR TO 8X053/54 DEVICES

The POD-C054 adapts the EMUL51-PC modular PC-based in-circuit emulator to the Philips Semiconductor 83C053/54 8-bit CMOS microcontrollers and the 87C053/54 EPROM versions. With the POD-C054, the EMUL51-PC can emulate the microcontrollers in all modes at full speed and memory size (up to 16 kbytes for the 8XC054 units). This includes all nine pulse-width-modulated commands and all three digital video outputs. The pod has a 42-pin shrink DIP plug for direct insertion into the devices' 70-mil pitch socket. The emulator supports several C compilers and debuggers from major suppliers. The POD-C054 is available immediately at a cost of \$895.

**Nohau Corp., 51 E. Campbell Ave., Campbell, CA 95008; (408) 866-1820. CIRCLE 480**



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## HIGH-LEAD-COUNT TAB PACKAGES SPEED DESIGNS

**W**ith lead counts up to 608 pins and outer-lead bond pitches of 0.25 mm, S-MOS Systems' tape-automated-bonding (TAB) packaging capabilities offer designers the extra flexibility needed to improve system reliability and shorten assembly time. The 35-, 48-, and 70-mm tapes meet Jedec Metric Format 4-001S. They're made up on a semicustom basis for applications including ASICs, LCD controllers, and drivers in memory cards for workstations, desktop and palmtop computers, personal-communication systems, and portable industrial systems.

At a 0.25-mm lead pitch and 0.5-mm test-pad pitch, 35-mm TAB is available with up to 192 pins. The same lead pitch with a 0.4-mm test-pad pitch can accommodate up to 224 pins, and at a 0.3-mm test-pad pitch, the maximum pin count is 258. Body sizes for 35-mm tape range from 14 by 14 mm to 20 by 20 mm.

At the same 0.25-mm lead pitch, TAB packaging using 48-mm tape offers pin counts of 256 (0.5-mm test-pad pitch), 320 (0.4-mm test-pad pitch), and 384 (0.3-mm test-pad pitch). For 48-mm tape, body sizes range from 16 by 16 to 28 by 28 mm. Pin counts for 70-mm tape are 436, 544, and 608 for the same respective test-pad pitches.

The advantages of TAB packaging are well known, and include higher mounting densities, easier surface mounting of high-lead-count devices, and customizable configurations. The packages also help shrink circuitry to use less printed-circuit-board real estate, and facilitate the design of systems with small form factors. TAB also permits functional testing and burn-in of devices before mounting, easy repair of defective chips, and quick, one-pass gang bonding of leads.

Nonrecurring-engineering charges for TAB packaging include a punching tool at \$4000, layout and masking at \$4400, and, if using inner-lead bonding (ILB), an ILB tool at \$4000. Prototype delivery is in 12 weeks. Initial production delivery, after customer test and qualification, is in seven to eight weeks. On-going production deliveries take three to four weeks.

**S-MOS Systems, 2480 N. First St.,  
Ste. 180, San Jose, CA 95131-1002;  
(408) 954-0120. **CIRCLE 485****

■ DAVID MALINIAK

## FUTUREBUS+ PRODUCTS CONFORM TO IEEE 896.2

**A** family of products, including system enclosures, backplanes, card cages, and wire-wrap boards, conforms with the requirements of Futurebus+ Profile F and is compatible with the optional requirements of Profiles A and B. They are designed in accordance with IEEE 896.2. The Series 222 enclosures offer system packaging for 128-bit applications. The card-cage area has hard-metric card guides with integral electrostatic discharge clips. The guides can accommodate 14 boards of variable thickness, ranging from 1.4 to 2.57 mm. The enclosures sell for \$9500.

The Series 224 14-slot backplanes support distributed and central arbitration with the central arbiter located at slot 1. To compensate for incident wave switching, the backplane has on-board surface-mount terminations. The backplanes are priced at \$3000. The Series

223 rack-mount card cage is designed in accordance with the mechanical specifications detailed in IEEE P1301.

The wire-wrap boards, Series 231 are designed for prototyping and backplane evaluation. The boards use National Semiconductor BTL transceivers in 9-bit plastic quad flatpacks. All stubs meet the specified requirements for incident wave switching. The chip-to-connector interface section is prerouted and optimized for Futurebus+ applications. The eight-layer boards incorporate Hybricon's patented ultra-high-density pin pattern for maximum density and very-high-frequency design for high-speed products. The E connector contains 80 pins for I/O, and 276 pins are available for front-panel I/O. The wire-wrap boards start at \$1900.

**Hybricon Corp., 12 Willow Rd.,  
Ayer, MA 01432; (508) 772-  
5422. **CIRCLE 486****

■ RICHARD NASS

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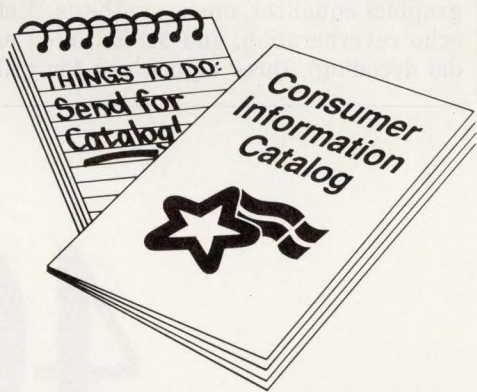
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## DEVELOPMENT KIT SIMPLIFIES MULTIMEDIA DESIGN EFFORT

MILT LEONARD

A joint effort by Texas Instruments and Atlanta Signal Processors has produced the Elf-31 Multimedia Developer's Toolkit for designing a variety of multimedia capabilities into personal computers. The kit's principal hardware component is an AT-compatible circuit board built around TI's TMS320C31 floating-point digital signal processing chip. The circuit board supports stereo 16-bit input/output, a telephone-line interface, the Musical Instrument Digital Interface (MIDI), voice I/O, and COMM 1 and 2 emulation for modem operation. The kit also includes software tools and a library of DSP functions that support voice mail, speech recognition, digital audio, modems, facsimile, and image/speech compression and analysis. Optional daughter boards have digital audio I/O and an SCSI port.

The Toolkit includes 16 multimedia-related functions, including six speech compression and decompression algorithms, six music-related algorithms (such as a 10-band stereo graphics equalizer, music synthesis, echo reverberation, and MPEG audio decoding), three algorithms for



Group 3 and Group 4 facsimile, and the JPEG image compression and decompression algorithm. These tools enable hardware designers to develop boards with a variety of multimedia capabilities for PCs, such as telephone answering machines, facsimile machines, image editors, graphic equalizers, and recorders for playing and editing stereo music.

Additional DSP multimedia tasks, such as signal processing for speech, music, imaging, and telephony, can be handled by using the Toolkit's DSP development tools, which include a loader, assembler, C compiler, and C source debugger. The kit also provides object code and, in

some cases, source code of the DSP algorithms. For PC software developers, a host application programming interface (API) gives access to the DSP functions of the TMS320 DSP. Besides the Developer's Toolkit, an Evaluation Toolkit is also available for demonstrating the operation of the 16 multimedia algorithms on the development board.

The Elf-31 Multimedia Evaluation Toolkit is available now from Texas Instruments, Atlantic Signal Processors, and authorized TI distributors for \$2000 each, which can be applied toward the price of the Developer's Toolkit. The Developer's Toolkit will be available in June for a suggested price of \$5000 each, which includes the board, C-compiler, debugger, and object-code licenses for 10 multimedia functions. The development board is also available separately at a suggested price of \$995 each in quantities of 10.

*Texas Instruments Inc., Semiconductor Group, SC-92004, P. O. Box 809066, Dallas, TX 75380-9066; 11-800-336-5236, ext. 3990. CIRCLE 495*

*Atlantic Signal Processors, Inc., 770 Spring St., Atlanta GA 30308; (404) 892-7265. CIRCLE 496*

# 40 YEARS

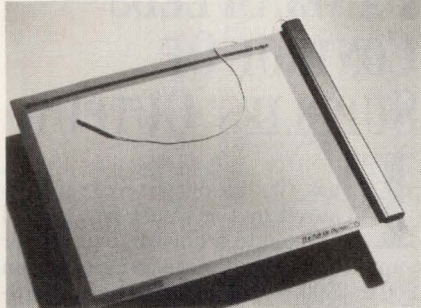
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## NEW PRODUCTS

COMPUTERS & PERIPHERALS

### DIGITIZER ROLLS UP FOR STORAGE



Save valuable office space by using the Roll-Up, a large format digitizer. The full-size tablet can be rolled out for use on a desk or drafting table, then rolled up for easy storage. The 6-lb. Roll-Up, just 1/16 in. thick, comes in two sizes, 30 by 36 in. and 36 by 48 in. The device's transducers supply a resolution of 1/1000 in. with an accuracy of  $\pm 0.01$  in. No calibration is ever required. Also, because no external power source is needed, the tablet can be used with portable systems. The Roll-Up comes with a one-button stylus with a side switch or a four-button cursor. Windows and AutoCAD drivers are included.

*GTCO Corp., 7125 Riverwood Dr., Columbia, MD 21046; (410) 381-6688. CIRCLE 497*

### KIT INTEGRATES FLOPTICAL-DRIVE

Designers can easily support the industry-standard 21-Mbyte 3-1/2-in. flopti-

cal disk drives using the Floptical Connection Kit. Floptical technology combines the properties of optical and magnetic data recording. The \$199 kit contains Adaptec's 16-bit SCSI host adapter, software utilities, an internal SCSI cable, and a user's manual. The SCSI host adapter can support six de-

vices. These include two floptical drives, two floppy disk drives, and two hard disk drives. In addition, the host adapter lets a PC boot from any of the three media types.

*Adaptec Inc., 691 South Milpitas Blvd., Milpitas, CA 95035; (408) 945-8600. CIRCLE 498*

### FAULT-TOLERANT SERVERS MULTIPROCESS TOO

**B**ased on hardware fault tolerance, the first member of the Integrated Micro Products XT family of Unix servers offers scalable performance of 27 to 54 MIPS in a desk-side cabinet. The XTM server's fault-tolerant CPUs, referred to as CpuSets, are boards based on dual- or triple-redundant 68040s running at 33 MHz that meet almost any desired level of system integrity. Each CpuSet has its own cache and primary memory. Furthermore, the XTM model hosts either one or two CpuSets. As a result, besides redundant CPUs it can pack a second CpuSet to double the system throughput from 27 to 54 MIPS. Future family members will host up to eight CpuSets to attain close to 200 MIPS.

Each component in the system is replicated so that the system has no single point of failure—even internal VME buses are duplicated. All active parts are also user-replaceable online. Furthermore, application programs do not

have to be modified to run on the system—internal software “hides” the fault-tolerant structure and lets the application think it's running on an ideal “virtual” machine. The system comes with 16 to 256 Mbytes of main memory, 330 to 2400 Mbytes of mirrored disk storage and has dual I/O channels. The disk subsystems employ a combination of mirroring and checksums to ensure data integrity. When a failed drive is replaced, the mirror drive restores data in a background mode. Battery backup is included in the power modules to provide for graceful power-downs if extended power-outages occur. Price for the base XTM system starts at \$50,000 for the 27 MIPS unit (including the Unix System V operating system license) and increases by \$10,000 for the 54 MIPS option.

*Integrated Micro Products Inc., 16795 Lark Ave., Los Gatos, CA 95030; Brian Knowles, (408) 399-5088. CIRCLE 499*

■ DAVE BURSKEY

# OF LEADERSHIP

## ELECTRONIC DESIGN

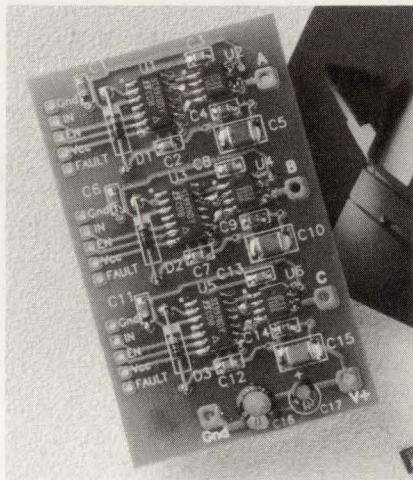


## HALF-BRIDGE DRIVER AND MOSFETS IN SOICs HANDLE 5 A AT 40 V

Now you can build a complete 40-V, 5-A per winding, motor-control subsystem with just two surface-mount components per 5-A winding. These are the small motors used—under microprocessor control—in printers, plotters, and copiers. For each MOSFET half bridge, you use the Siliconix Si9940DY "Little Foot," an 8-pin SO-8 containing a pair of 50-m $\Omega$ , 50-V FETs rated at 5 A. For a driver the Siliconix Si9976DY does the job. The Si9976DY contains both high and low-side drivers for an n-channel MOSFET half bridge. Its integrated charge pump provides the floating supply needed to drive the gate of the high-side FET positive relative to its drain. A typical three-phase drive is shown in the figure.

Other features of the Si9976DY driver include cross-conduction (shoot-through) protection, undervoltage lockout (UVLO), shorted output protection, and a digital output indicating the type of fault. Cross conduction is avoided by preventing the high-side driver from turning on until the low-side driver has been off for a fixed delay.

At power up, undervoltage lockout is implemented by keeping both drivers off until the internal, regulated supply is approximately one base-emitter volt-



age drop below the supply's nominal value of 16 V. After power up the undervoltage lockout circuit continues to monitor the internal supply and, if an undervoltage condition occurs, both drivers are turned off and the fault output goes high. In quantities of 100,000 the Si9976DY driver goes for \$0.90 each, the Si9940DY dual MOSFET sells for \$1.40 each.

**Siliconix Inc.**, 2201 Laurelwood Rd., Santa Clara, CA 95056; (800) 554-5565, ext. 1400. **CIRCLE 487**

■ FRANK GOODENOUGH

## SECOND SOURCE ARRIVES FOR IC SWITCHERS

Designers hesitant to use any of the sole-sourced complete switching regulators ICs (with on-chip power switch) need fear no more. Now Semtech Corpus Christi (formerly Lambda Semiconductor) has announced a form, fit, and function second source for the LM1575 and LM2575 simple switchers from National Semiconductor. They are available in TO-220, TO-3, 16-pin DIP, and 24-pin SOICs. In quantities of 100 they go for \$3.50 each.

**Semtech Corpus Christi**, 121 International Dr., Corpus Christi, TX 78406; (512) 289-0403. **CIRCLE 488**

## IC SWITCH KEEPS HIGH VOLTAGE OFF ICs

Looking much like a three-terminal linear regulator, the SP710 three-lead power IC from Harris protects low-

voltage ICs from supply-rail transients ranging from  $\pm 16$  V to  $\pm 90$  V. The input pin, the left-hand pin of the TO-220 package, connects to supply rails between 4.5 and 16 V.

The output pin on the right connects to the load, and the center pin (the tab) connects to ground. If the input voltage exceeds  $\pm 16$  V the chip disconnects the supply rail from the load. The input can take up to  $\pm 90$  V for up to 15 ms and up to 24 V continuously. During shutdown, load current will not exceed 20 mA. The chip also shuts down if the die temperature exceeds 150°C. With supply rails of 4, 9, and 16 V at switch currents of 175, 500, and 800 mA, respectively, the voltage drop across the switch runs a maximum of 250, 650, and 1050 mA, respectively. In quantities of 1000, the SP710 power IC goes for \$2.95 each.

**Harris Semiconductor**, P. O. Box 883, Melbourne, FL 32901; (800) 4 Harris, ext. 1041. **CIRCLE 489**

## SMART FRONT PANEL SPEEDS CONTROL OF SUPPLIES' OUTPUT

Fast, flexible output control is ensured by the smart front panel affixed to a line of 15 dc power supplies. With outputs ranging from 200 to 2000 W, the HP 6500 Series power supplies constitute a broad offering for benchtop or system applications that don't require HP-IB control of the supply.

The HP 6500 Series of supplies includes three power ranges: 200 W, 500 W, and 2000 W. Each power range offers five supplies that vary by voltage rating.

Front-panel controls provide three methods of setting the output voltage and current. A numeric-entry keypad lets the user set the voltage quickly and precisely, while up-down buttons and rotary-pulse generators enable users to increment and decrement voltage and current settings in small steps quickly and conveniently. An external voltage signal can also be applied for control of the output voltage. For repetitive benchtop testing, up to five states or sets of power-supply settings can be stored and recalled for easy sequencing. The supplies can also be connected in autoperallel with other models of the same ratings.

Excellent noise performance is provided for tests that require noise-sensitive measurements. The peak-to-peak ripple and noise spans from a low of 3 mV pk-pk on the low-power, low-voltage models to a high of just 16 mV on the 2-kW, 120-V model.

Overcurrent, overvoltage, and over-temperature protection, which are more commonly found on system power supplies than on bench units, are provided for both the supply and the device under test (DUT). These features protect the DUT by disabling the supply's output voltage when potentially dangerous conditions occur.

Pricing ranges from \$1650 to \$1750 for the 200-W units, from \$2100 to \$2300 for the 500-W supplies, and from \$3650 to \$3800 for the 2000-W units. Delivery is estimated at four weeks from receipt of order.

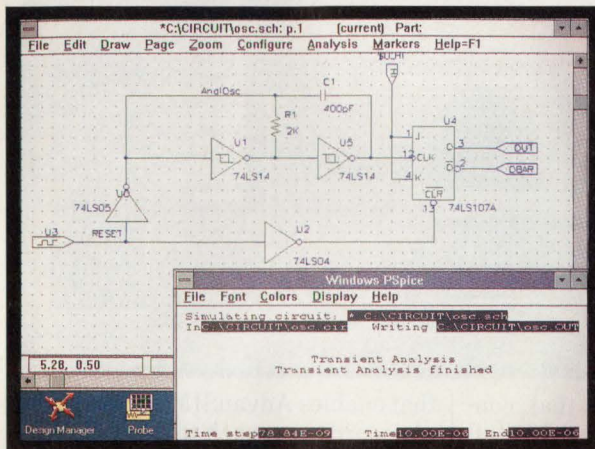
**Hewlett-Packard Co.**, 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. **CIRCLE 490**

■ DAVID MALINIAK

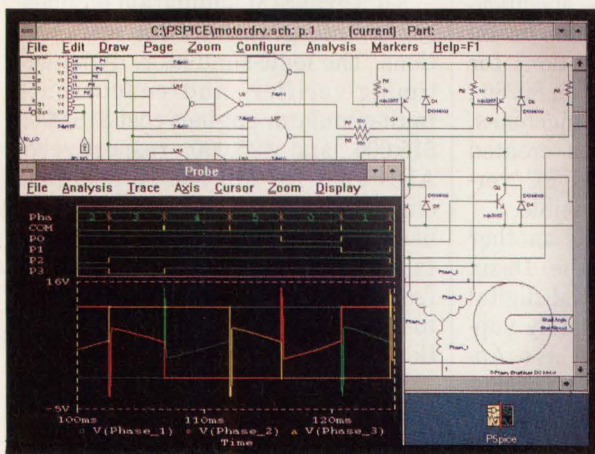


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# ANALOG BEHAVIORAL MODELING, VHDL SUPPORT EMBELLISH BROAD EDA SOFTWARE LINE

LISA MALINIAK

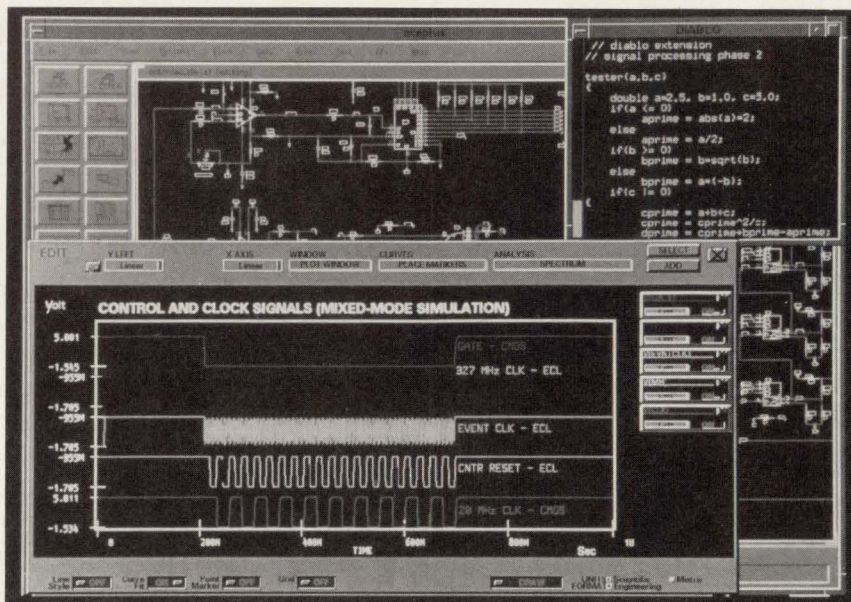
Enhancements ranging from analog behavioral modeling to VHDL support strengthen the newest software line from Dazix. The enhancements, which include new products and the porting of existing products to Sun workstations, expand the Dazix offering for a wider choice of tools and platforms.

One of the new products is the Dazix/Intergraph Analog Behavioral Language Option (Diablo). Diablo is based on industry-standard C and C++ programming languages. The language's flexibility lets users program complex analog behaviors and functions without the traditional restrictions imposed by built-in primitives to the simulator. With Diablo, the simulator can access pertinent model information through program calls during run time.

Diablo is integrated with the entire suite of Dazix analog design tools, including the Apex Plus simulator. Apex Plus is a circuit simulator for analog, mixed-mode, and mixed-discipline circuits. It merges the analog, board-level, and native mixed-mode simulation capabilities of the Intergraph Integrated Simulator (ISIM) with the IC-simulation strength of the Dazix Apex simulator. The end product is a tool that can simulate large designs in their entirety, and at many levels of complexity and model abstraction. Both Diablo and Apex Plus run on Intergraph and Sun workstations, and sell for \$4000 and \$15,000 respectively.

Another new product is the ACE-Plus Design Entry software, a unified entry environment that merges all the company's existing design capture into one tool. It serves as a common front end for all the Dazix EDA environments, supporting the range of system- to IC-level designs. When a design is entered in ACE-Plus, a master design database is created for all future tasks.

ACEPlus is tightly linked to the Dazix Master Librarian, a central-



ized relational database that contains component information for all the design tools. Graphic symbols are found and placed on the schematic from that database by using a combination of component attributes, or by querying parametric specifications of parts. ACEPlus runs on Intergraph and Sun workstations for \$7000. A PC version runs on 80286-, 80386-, and 80486-based machines, and sells for \$3500. Files created with the workstation and PC versions are completely compatible.

Full VHDL simulation is another enhancement added to the Dazix product line. The AdvanSIM digital simulation engines completely support IEEE 1076 VHDL. Three AdvanSIM engines for logic and timing simulation, dynamic timing verification, and concurrent fault simulation are fully compatible and share a common model library.

New AdvanSIM support for user-definable data types gives engineers the ability to incorporate third-party simulation data into their analyses. In addition, AdvanSIM has new capabilities for mixed-mode simulation when used in conjunction with the Dazix A/D Bridgeway (ADB). ADB is an intelligent control processor

that enables AdvanSIM to take a single-engine approach to designs with mostly digital but some analog circuitry by its ability to simulate its own analog or mixed-signal behavioral models.

All AdvanSIM simulation engines run on Intergraph and Sun workstations. The logic-simulator, dynamic-timing-verifier, and concurrent-fault-simulator engines cost \$18,000, \$15,000, and \$25,000, respectively. ADB goes for \$10,000. In addition, engineers can purchase a graphical user interface for \$9000. The interface compiles a simulation database from the schematic, allowing users to run logic, timing, or fault simulation using just the schematic.

Finally, Dazix is announcing that two of its existing products, MCM Engineer and the StarTrak pc-board router, will be available on both the Intergraph and Sun workstations. MCM Engineer is a tool for the design, verification, and manufacture of multichip modules (MCMs). Pricing for MCM Engineer starts at \$18,000. StarTrak costs \$40,000.

Dazix, an Intergraph Co., One Madison Industrial Park, Huntsville, AL 35894-0001; (205) 730-2000.

CIRCLE 481





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Your customers and prospects agree that trade shows are worth attending. But they also agree that specialized business publications are worth a great deal more to them. Because that's where they find more of the important information they need to know. A recent study, conducted by the Forsyth Group, proves it.

Almost 10,000 business and professional decision makers participated in the study. They were asked what sources they find most useful in providing information about the products and services they buy for their companies. Trade shows, salespeople and direct mail were all well regarded. But overall, specialized business publications clearly took top honors.

Trade magazines are also at the top of the list when you consider cost per contact. No other medium is more efficient. Or has more credibility.

For a free copy of the study, please write to American Business Press, 675 Third Avenue, Suite 400, New York, NY 10017.

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**SENIOR DESIGN ENGINEER**

Responsible for research and development of advanced models for temperature variation, high frequency parasitics, current-flow dependent behavior, and scaling effect of both bipolar and CMOS devices. Successful candidate will also research and develop computation efficient models to improve circuit simulation time, process and device characterization, extraction methodology for sub-micron integrated circuit fabrication processes, analyze statistical data of best/typical/worst case models, develop correlation theory of device parametric interdependency for various process technologies, develop and enhance measurement capability and HP programs, improve accuracy for dc, ac, transient, C-V profiling and S-parameter characterization of semiconductor devices from -55C to 175C with wafer probing station, HP network analyzer, HP LCRZ meter, HP semiconductor parameter analyzer, HP computer, etc.

Requirements: Ph.D. in Electrical Engineering with more than 5 years laboratory experience in design, fabrication, and electrical characterization of solid state and thin film devices, experience in micro-electronics, semiconductor device physics, solid-state physics, and integrated circuit modeling and simulation, knowledge of integrated circuit design, fabrication process, and SPICE simulation. Must also possess extensive measurement technique at low temperature and microwave frequency and have a strong background in electromagnetic wave, microwave circuit and device, statistical analysis, thermal physics, numerical analysis, and experience of HP instrumentation and programming on HP computer.

Send resume to P.O. Box 1509, Kennebunkport, ME 04046 no later than April 29, 1992. Must show proof of legal authority to work in U.S. EOE M/F/V/H.

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The Synthesis Design Environment (SDE) from Dazix captures, verifies, synthesizes, and optimizes digital circuits using VHDL. The SDE high-level environment links multiple design-capture methodologies, various specialized synthesis engines, and VHDL simulation and analysis. As a result, users have the flexibility to design independently of target technologies.

Engineers describe a circuit's behavior using VHDL, capturing its intended functionality rather than its implementation. Actually, any combination of entry methods may be used, including Boolean equations, truth tables, state machines, state diagrams, C, Abel, hardware description languages, and schematics. After concept entry, the design's functionality is analyzed and debugged with the Dazix VHDL Design System.

Once the functionality is verified,

synthesis technology creates gate-level structure and optimizes the design for area and speed. The synthesis technology that's tightly meshed within SDE includes ArchSyn for behavioral synthesis, MacroSyn for data-path synthesis, LogSyn for logic synthesis and optimization, and TestSyn for testability synthesis. These products, which are exclusively offered by Dazix, are based on many years of research and development by AT&T Bell Laboratories. Data I/O's PLD- and FPGA-synthesis software is also tightly integrated in SDE.

The Synthesis Design Environment, which is shipping now, runs on Intergraph and Sun workstations. The ArchSyn, MacroSyn, LogSyn, and TestSyn products cost \$15,000, \$10,000, \$30,000, and \$25,000, respectively.

*Dazix, an Intergraph Co., One Madison Industrial Park, Huntsville, AL 35894-0001; (205) 730-2000.*

**CIRCLE 482**

■ LISA MALINIAC

**CHIP SET SPEEDS CAD PROGRAMS BY UP TO 70%**

A two-chip engineering coprocessor improves performance of technical, engineering, and scientific applications on Intel386 DX microprocessor-based machines by as much as 70%. The Intel chip set, which is called RapidCAD Engineering CoProcessor, combines floating-point operations and CPU functions to run tasks like 3D rendering nearly 70% faster than an Intel386 DX processor and Intel387 DX Math CoProcessor combination. RapidCAD is aimed at CAD applications such as AutoCAD, but also ups performance on scientific analysis software. The larger of the two chips combines the functions of the 386 DX processor and 387 coprocessor into one device, and replaces the 386 DX CPU in existing systems. The smaller chip drops into the socket usually reserved for the math coprocessor. It contains the interface logic to manage math exceptions, like dividing by zero. The RapidCAD Engineering CoProcessor is available now for \$499.

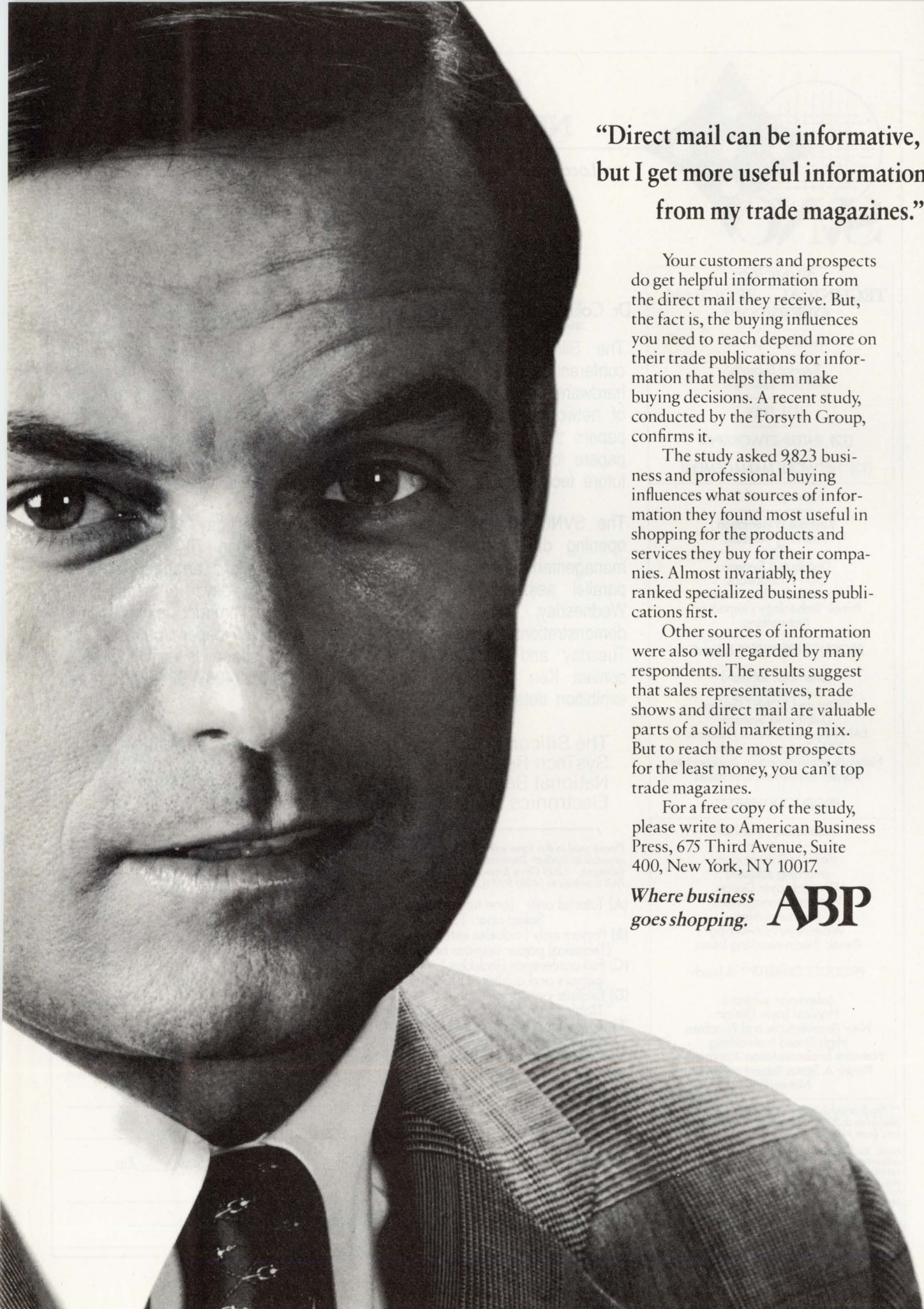
*Intel Corp., 3065 Bowers Ave., P. O. Box 58065, Santa Clara, CA 95052-8121; (800) 538-3373, ask for literature package "BO." CIRCLE 483*

**BOARDS LINK PGAS TO HARDWARE MODELER**

A 120-channel board adapter teamed with either a 180-pin or 208-pin interface board helps engineers connect pin-grid-array (PGA) devices to the Teradyne D300 Hardware Modeling System for simulation. A hardware modeler lets engineers use actual VLSI devices to supply the logical data needed for circuit and fault simulation. The board adapter is a pre-wired motherboard that accepts either interface as a daughterboard containing the device under simulation. Using a daughterboard to plug in the device under simulation makes it simple and inexpensive for engineers to swap devices. Both interface boards include power and ground connections. In addition, every channel-to-pin link is marked and identified individually to ease the cutting and jumping that engineers may be required to do. The 120-channel adapter board costs \$2200. A 160-channel version is also available. The 180-pin and 208-pin PGA interface boards go for \$690 and \$615, respectively. All products are shipping now.

*Teradyne Inc., 321 Harrison Ave., Boston, MA 02118; (617) 482-2700. CIRCLE 484*





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Your customers and prospects do get helpful information from the direct mail they receive. But, the fact is, the buying influences you need to reach depend more on their trade publications for information that helps them make buying decisions. A recent study, conducted by the Forsyth Group, confirms it.

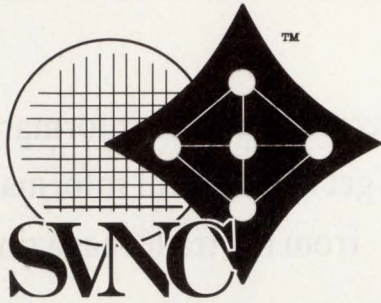
The study asked 9823 business and professional buying influences what sources of information they found most useful in shopping for the products and services they buy for their companies. Almost invariably, they ranked specialized business publications first.

Other sources of information were also well regarded by many respondents. The results suggest that sales representatives, trade shows and direct mail are valuable parts of a solid marketing mix. But to reach the most prospects for the least money, you can't top trade magazines.

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# THE SILICON VALLEY NETWORKING CONFERENCE

Location : The Santa Clara Convention Center, Santa Clara, California and the adjacent Westin Hotel

**APRIL 27 - 29, 1992**

## KEYNOTE SPEAKERS:

Eric Benhamou, Chief Executive Officer, 3Com Corp.  
 Dr. Colin Mick, Technical Director, Network Products, Comdisco Systems Inc.

### SVNC'92 TECHNICAL PROGRAM OVERVIEW\*

Monday, April 27

Tutorial Subjects  
(full day seminars)

(T1) FDDI

(T2) INTERNETWORKING

(T3) NETWORK MANAGEMENT

Tuesday, April 28

Keynote Presentation  
(morning subjects)  
FDDI

Distributed Systems  
LAN Foundations

Future Technology Issues  
Panel: Technology's Impact on  
Networking

PRODUCT EXHIBITS\*\* & Lunch

(afternoon subjects)  
Internetworking

ISDN and SONET Design  
Distributed Systems

LAN Applications and Protocols  
LAN Technology Issues

Network Implementation Approaches  
Panel: Implementation Issues

PRODUCT EXHIBITS\*\*

Wednesday, April 29

Keynote Presentation  
(morning subjects)  
Physical Layer Design

Network Management  
Internetworking

Wide-Area Networking  
Panel: Internetworking Issues

PRODUCT EXHIBITS\*\* & Lunch

(afternoon subjects)  
Physical Layer Design

New Architectures and Functions  
High-Speed Networking

Network Implementation Approaches  
Panel: A Status Report on Global  
Networking

\*tentative; subject to change

\*\* Product exhibits are open from Noon to 2 pm and from 5:30 to 7:30 pm on Tuesday, April 28, and from Noon to 2 pm on Wednesday, April 29.

Note: Registration fees for the conference include coffee-break refreshments, lunch, one set of tutorial notes and/or conference proceedings, and one exhibits admission. A \$100 handling fee will be charged for registrations cancelled before March 30, 1992; no refunds after March 30.

Make your room reservations directly with the Westin Hotel, 5101 Great America Parkway, Santa Clara, Calif. (408) 986-0700; Ask for the special SVNC room rate.

The Silicon Valley Networking Conference is the only networking conference that focuses on the DESIGN side of network-related hardware down to the chip level as well as the development and use of network management and testing software. In addition to technical papers that focus on design issues there will be panel sessions and papers for system planners and strategic MIS executives that focus on future technology trends and network implementation issues.

The SVNC program venue consists of three full-day tutorials on the opening day (Monday, April 27) and more than 70 technical and management-oriented paper and panel presentations arranged in three parallel sessions on the second and third days (Tuesday and Wednesday, April 28 and 29). Table-top product exhibits and demonstrations will supplement the technical paper program on Tuesday and Wednesday. Limited exhibit space is still available; contact Ken Majithia at SysTech Research - (408) 924-3930 - for exhibition details.

The Silicon Valley Networking Conference is a creation of SysTech Research. SVNC is co-sponsored by 3Com Corp., National Semiconductor Corp., and Electronic Design and Electronics Magazines (Penton Publications).

## SVNC'92 REGISTRATION FORM

Please mail in this form with your payment. Make checks payable to SysTech Research and mail to: SysTech Research, 1248 Olive Branch Lane, San Jose, CA 95120. FAX inquiries to (408) 997-8265.

	Payment * postmarked by 3/30/92	Payment * postmarked after 3/30/92	Payment at the door
(A) Tutorial only (one tutorial on 4/27) Select one: T1 --- T2 --- T3 . . . . .	\$250	\$295	\$350
(B) Papers only (includes exhibits entry) (Technical paper sessions on 4/28, 29). . . . .	\$350	\$395	\$450
(C) Full conference (includes 1 tutorial, all papers and exhibits); mark tutorial in (A). . .	\$450	\$495	\$550
(D) Exhibits-only admission (Table top exhibits only on 4/28 or 4/29). . .	\$ 25	\$ 25	\$ 25
(E) Extra proceedings (For pick-up at the conference); If not attending, add \$20/domestic, \$40/intnl, for shipping. . . . .	\$ 85	\$ 85	\$100

\*New extended deadline dates; after 4/16 do not mail, bring for at-door registration Tax ID #77-026-4602

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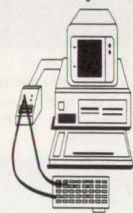
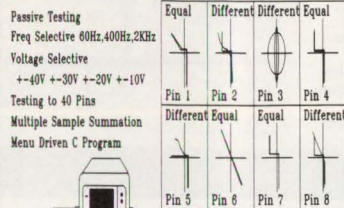
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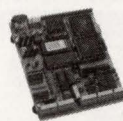
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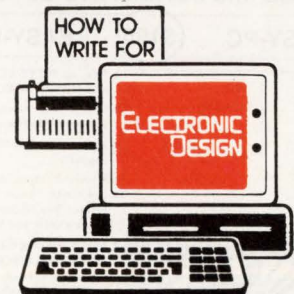
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Thinking of writing a technical article for publication in Electronic Design? This 12-page brochure contains just about everything you need to know about the process: submitting the outline, tips on writing the manuscript, preparing the artwork, and more.

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ELECTRONIC DESIGN



# ELECTRONIC DESIGN

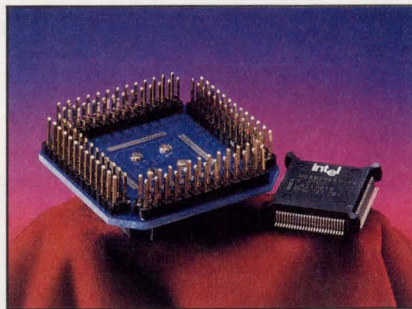
DIRECT CONNECTION ADS

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May 1	4/4/92
May 14	4/17/92
May 28	5/1/92
June 11	5/15/92
June 25	5/29/92
July 9	6/12/92
July 23	6/26/92
August 6	7/10/92
August 20	7/24/92
September 3	8/7/92
September 17	8/21/92
October 1	9/4/92
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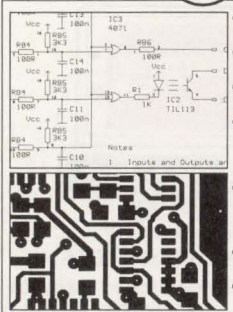
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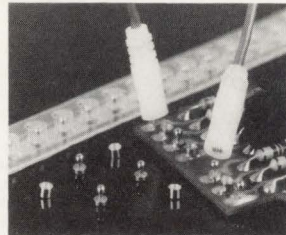


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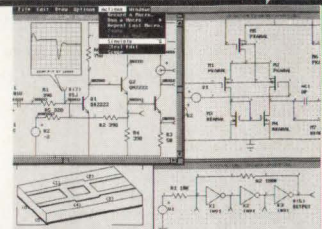


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## INDEX OF ADVERTISERS

ADVERTISER	READER SERVICE	PAGE NUMBER	ADVERTISER	READER SERVICE	PAGE NUMBER
	U.S. / OUTSIDE U.S.			U.S. / OUTSIDE U.S.	
ACCEL Technologies	402	133	Murietta Circuits	128, 129	102
Advanced Micro Devices	80, 81	2-3	National Golf Center	◇	118
	148, 149	10-11	National Instruments	130, 131	19
Altera	206, 207	42-43*	Nohau	132, 133	120
AMP	82, 83	66-67	Number One Systems	410	133
Apex Microtechnology	84, 85	27	Oxley, Inc.	411	134
AT&T	86, 87	64-65*	Pacific Hybrid	212, 213	115
	88, 89	80-81*		214, 215	117
Atmel	236, 237	55		216, 217	119
B&C Microsystems	407	134		218, 219	121
Burr-Brown	208, 209	94	Philips Semiconductor	232	35-37**
Capital Equipment	90, 91	122	Philips Test		
Comdisco	92, 93	98	& Measurement	◇	61**
Compass			Pico Electronics	136, 137	18, 79
Design Automation	94, 95	6-7	Power Convertibles	172, 173	8
Cybernetic Micro			Powerex	174, 175	96
Systems	150, 151	14	Professional Digital		
Cypress Semiconductor	◇	Cover IV	Components	403	133
Dale Electronics	96, 97	85	Quality Semiconductor	220, 221	107
Data Translation	98, 99	72	Raytheon	140, 141	56
Digital Equipment	152, 153	30-31	Rogers Corp.	142-147	91
Dow Plastics	100, 101	71		408	134
Emulation Technology	406	134	Samsung Electronics	178, 179	42-43**
Fortron Source	154, 155	8	Samsung		
Genashore	408	134	Semiconductor	176, 177	104A-104D*
Harris Semiconductor	226, 227	38-39	Siemens Components	180, 181	44*
	228, 229	40-41	Siliconix	◇	93
Hewlett-Packard Co.	106	1	Sony Semiconductor	184, 185	59*
	158, 159	12-13	Stanford Research	186, 187	35*,44**
	104, 105	61*	Star Semiconductor	188, 189	32
	102, 103	116*	Systech Research	◇	132
Hitachi Europe	1	**	Tektronix	194, 195	88
Huntsville				190, 191	97
Microsystems	210, 211	136		196, 197	103
IBM	◇	24-25		192, 193	113
Information			Texas Instruments	◇	16-17
Handling Services	110, 111	52	Toshiba ECD	234, 235	36-37*
Intel	1	109-111	Unitrode Integrated		
International			Circuits	198, 199	101
Microcircuits	400	133	UTMC	230, 231	69
International Rectifier	112, 113	22	Vicor	200, 201	75
Intusoft	412	134	White Technology	202-205,	
Lambda Electronics	114, 115	48A-48D*		222-225	63
Lattice Semiconductor	160, 161	Cover II	Z-World Engineering	404	133
Maxim Integrated					
Circuits	162, 163	46-47			
	164, 165	51			
	166, 167	53			
Mesago, Messe					
& Kongress GmbH	168, 169	124-125**			
Micon Technology	170, 171	9			
MicroSim	116, 117	127			
Mini-Circuits Laboratory,					
a Div. of Scientific					
Components Corp.	122, 123	15			
	118, 119	20-21			
	120, 121	28-29			
	126, 127	82			
	124, 125	Cover III			

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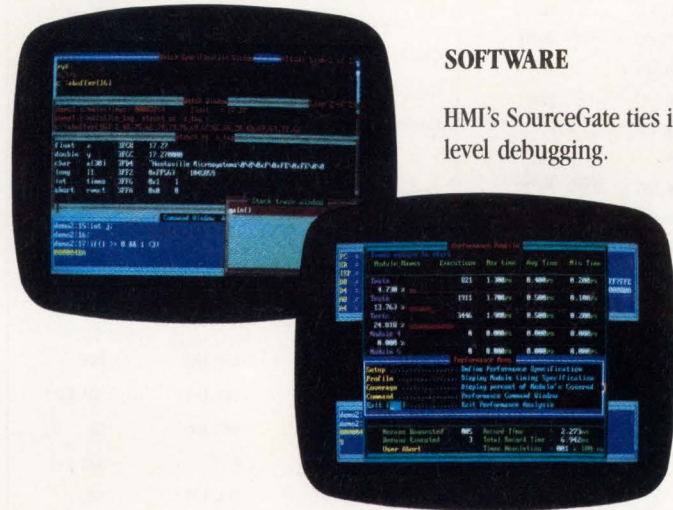
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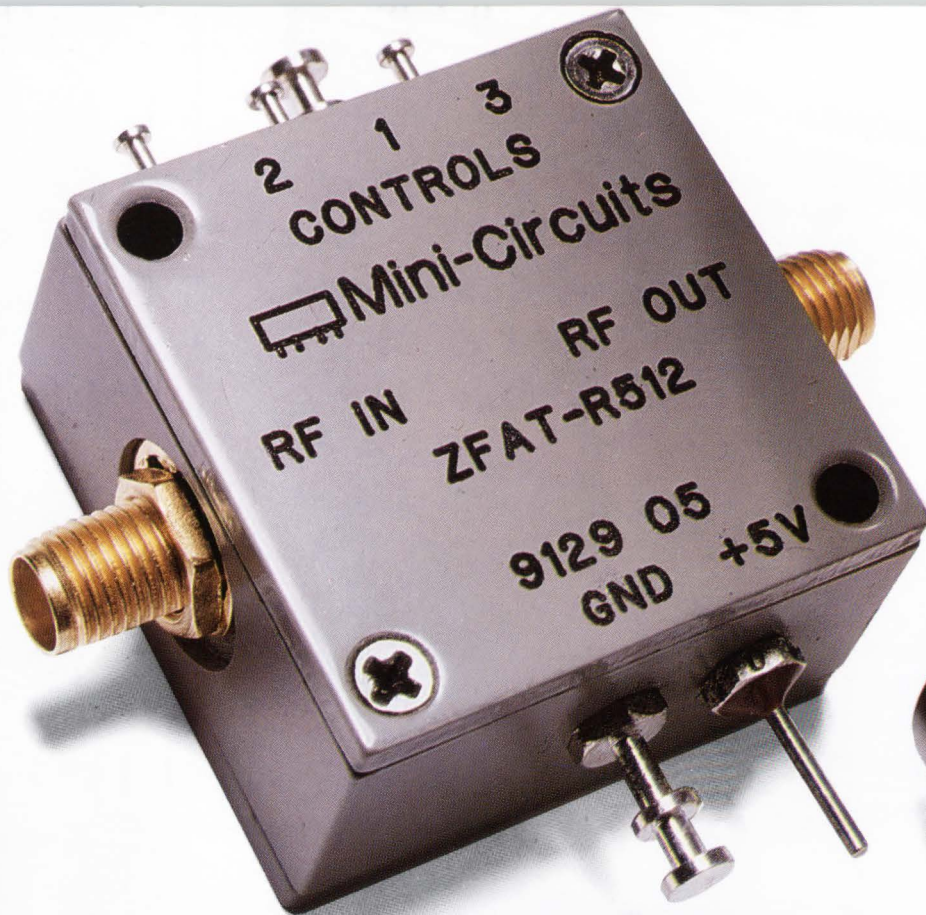
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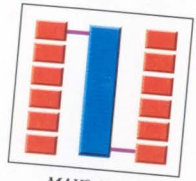
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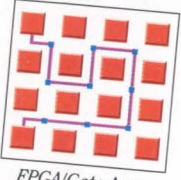
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