Q/DH Controller
User's Guide

10177X07

October 1982

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CHAPTER 1

How To Use This Manual

Congratulations on your purchase of a Q/DH from ABLE Computer. We are sure it will provide you with years of satisfactory service. We have prepared this manual to help you maximize the effectiveness of the Q/DH in your system. This manual is provided to assist you with the installation, use and care of Q/DH; it does not provide repair information. If you have problems with your Q/DH, we prefer that you let us repair it in our factory. This manual assumes that you are familiar with the LSI-11 architecture and Q Bus structure. For information about the LSI-11, refer to the following DEC documents:

* Microcomputers and Memories Handbook

* Microcomputer Interfaces Handbook

For information about the Q Bus, refer to the following DEC documents:

* Microcomputers and Memories Handbook

* PDP-11 Bus Handbook

You may also wish to refer to the following ABLE documents for Q/DH system information:

* ABLE Q/DH Subsystem User's Guide, document number 10180X07

* ABLE Dual Purpose Distribution Panel User's Guide, document number 10129X07

This manual is organized into the following chapters:

* Chapter 2 contains general description of Q/DH and lists its special features. It also includes programmable line parameter information, electrical specifications, and physical specifications. Photographs of the Q/DH are included in this chapter.

* Chapter 3 contains detailed instructions on installation. The functions of all switches on the board are described. Information on maintenance features, including microdiagnostics is also contained in this chapter.

* Chapter 4 contains information on the care of Q/DH and troubleshooting tips in the event that a problem occurs. The procedure for obtaining assistance form ABLE Computer is also described.

* Chapter 5 describes a typical application for Q/DH. Terminal/communications information, wiring information for modem connection, and Q Bus connector information is also provided.

* Chapter 6 contains descriptions of data handling registers, modem registers, timing considerations for transmitter/receiver speed programming, break control, and transmitter and receiver timing. Maintenance mode considerations are also provided.

* Chapter 7 describes on how Q/DH works. Message transmission and reception, modem control, ring signal application, baud rate selection and the diagnostic microprOgram, are described.

* The appendices provide an interrupt level strapping chart to alter the priority level of Q/DH and loopback connection information.

  The appendices contain a spare parts listing for those wishing to maintain a spare parts inventory and also a list of materials for the Q/DH.

CHAPTER 2

What Is Q/DH?

2.1 GENERAL DESCRIPTION

The Q/DH is a microprocessor-based controller which connects a Q Bus system to 8 or 16 asynchronous communications lines. It provides DMA (direct memory acess) output capabilities and modem control. It is system software compatible with the DEC DH11 and DM11-BB. An 8 line Q/DH can be installed in any standard quad Q Bus backplane. A 16 line Q/DH requires two quad slots. See Figure 2-1.

2.2 FEATURES

* DMA capability provides significant system throughput improvement over interrupt-driven devices.
* Large input silo improves input handling capacity which reduces data overrun probability for block mode terminals and computer-to-computer interconnects.
* Word DMA output transfers allow optimum Q Bus utilization.
* Operating system software compatible with DEC DH and DM.
* On-board pencil switches for address and vector selection add flexibility and eliminate jumpers.
* Comprehensive self-test diagnostic with LED display.
* Available with EIA panel or with a line adapter/panel which offers both EIA and 20ma current loop channels.

* Diagnostic loopback connectors are built into optional distribution panels.

* Provides interface and signals conforming to EIA RS-232-C standards.

* Modem events reported under interrupt control to eliminate system overhead associated with DZV11-style modem scanning.

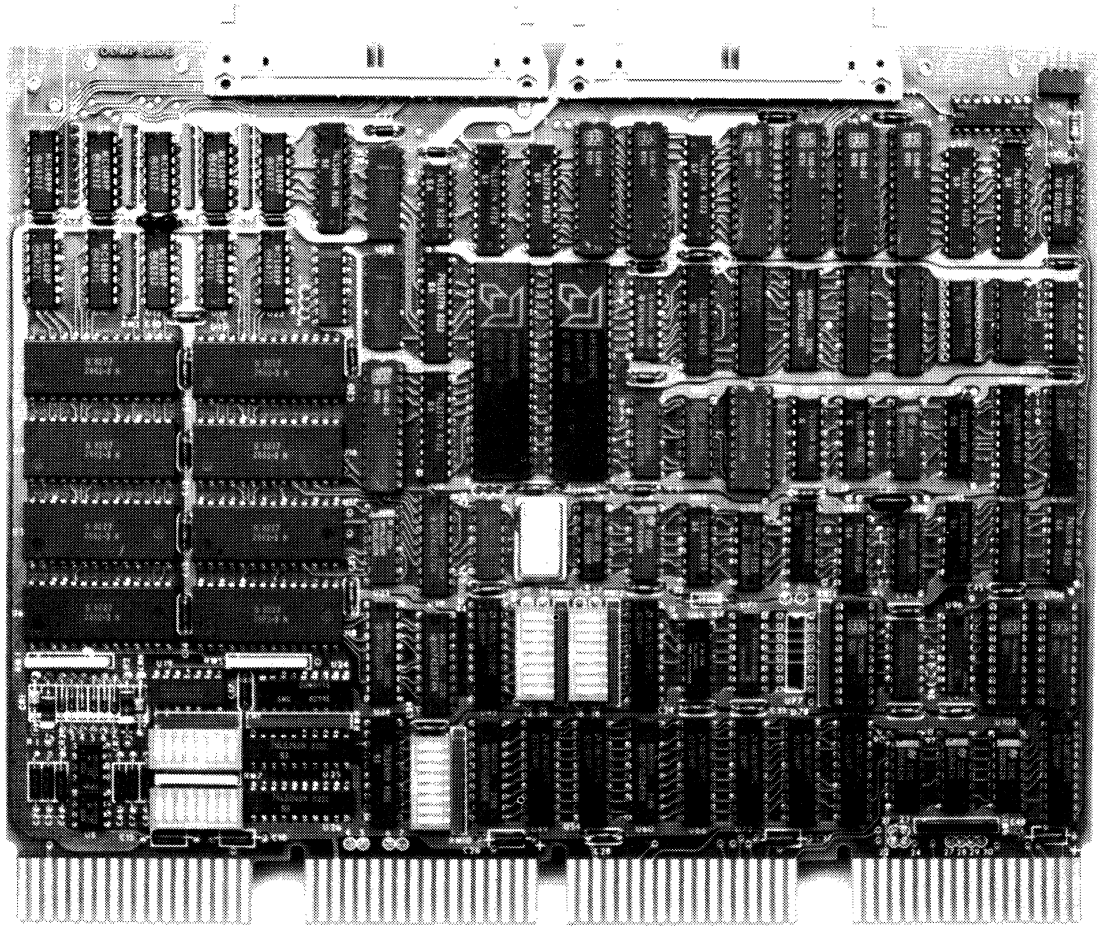


Figure 2-1: Q/DH Controller Model 10176

2.3 SPECIFICATIONS

2.3.1 Programmable Line Parameters

Character Length:	5, 6, 7, or 8 data bits
Number of Stop bits:	1 or 2 for 6-, 7-, or 8- bit characters; 1 or 1.5 for 5-bit characters
Parity Generation/Detection:	Odd, even, or none
Operating Modes:	Full duplex
Transmitter/Receiver Speeds (Baud):	0, 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, 9600, plus 19200 (replacing External A)

2.3.2 Electrical Specifications

Bus Loading:	Controller
	DC Loads: 1 AC Loads: 2
	Expander Board
	DC Loads: 0 AC Loads: 2

Power Requirements:

Controller

5.0 amps at +5V
0.35 amps at +12V

Expander Board

1.5 amps at +5V
0.35 amps at +12V

Interrupt Request Level: DH function is set at BR5. DM function is set at BR4. Priority levels may be user-modified.

2.3.3 Modem Control

For each line, the Q/DH moniters two data set output control signals, ring and carrier, and controls one data set input control signal, Data Terminal Ready.

2.3.4 Addressing

Device Address: The Q/DH requires eight consecutive word addresses in the floating address space which starts at 760010. All Q/DH units in a system should have consecutive word addresses.

The modem control requires two consecutive word addresses, the first of which must be a multiple of four. Address space has been assigned for 16 Q/DH Controllers. The first is at 770500; the second starts at 770510, and so forth.

Interrupt Vectors: The Q/DH requires three interrupt vectors, two consecutive vectors XX0 and XX4, are for the receiver and the transmitter respectively. A separate vector, XXX, is for the modem. These are in the floating vector space (300 - 776).

2.3.5 Physical Specifications

Board Size: The Q/DH Controller is a standard quad-width board. Rectangular dimensions are 10.45 inches (26.5 cm) x 8.40 inches (21.3 cm). The board is shown in Figure 2-1.

The Q/DH Expander board is also a quad-width board.

CHAPTER 3

How To Install Q/DH

3.1 INSTALLATION PROCEDURE

This chapter explains in detail how to install Q/DH. Below is a brief, step-by-step procedure.

1. Determine the address assignment of the DM portion and set switch S4 accordingly (Section 3.5 and Section 3.6.1).

2. Determine the address assignment of the DH portion and set switch S5 accordingly (Section 3.5 and Section 3.6.2).

3. Determine the vector assignment of the DM portion and set switch S2 accordingly (Section 3.5 and Section 3.6.3).

4. Determine the vector assignment of the DH portion and set switch S1 accordingly (Section 3.5 and Section 3.6.4).

5. Refer to Table 3-4 for switch S3 functions and set the switch accordingly (Section 3.7.1).

6. Set maintenance switches to achieve the desired functions (Section 3.7.1).

7. If interrupt levels other than the ones factory set are required, modify the jumper connections (Section 3.8).

8. Remove power from the system (Section 3.9).

9. Install Q/DH board in vacant slot (Section 3.10).

10. Check that there are no vacant slots between the Q/DH and the CPU.

11. Apply power to the system, checking the LEDs to verify internal operation of the board (Section 3.12).

12. Run the diagnostics (Section 3.11).

3.2 UNPACKING THE Q/DH

The Q/DH is shipped in a special container to prevent damage during shipment. It is recommended that this container be saved for use in the event that the product requires subsequent reshipment. Unpack the contents carefully and inspect for any signs of damage. If damage is found, notify the carrier immediately.

3.3 VERIFY THAT YOU RECEIVED WHAT YOU ORDERED

Be sure that you received what you ordered by checking the board numbers. Q/DH has two numbers found on the backside of the board in the upper right corner: 10176 (etched) and 10177 (stamped). See Figure 3-1. The expander board has 10176 (etched) and 10178 (stamped) on the board.

3.4 EQUIPMENT NEEDED TO USE THE Q/DH

You will need the following equipment to use the Q/DH:

* LSI-11 Q Bus computer system

* One vacant quad slot for mounting the Q/DH for an 8 line, or two vacant quad slots for a 16 line.

* Sufficient power

3.5 HOW TO DETERMINE ADDRESS AND VECTOR ASSIGNMENTS

The DH portion of the Q/DH uses eight words of floating address space. The floating address space begins at 760010 as shown in Figure 3-2. Addresses within this space are assigned according to rank. Table 3-1 shows the ranks assigned to devices addressed in this range.

The DH uses addresses located after any DJ11's in the system. Each DH requires eight consecutive addresses starting with an address that is a multiple of 20 (octal). For example, for a system with no DJ11 units, register address assignments for three Q/DH units are as follows:

Unit	Octal Register Address
1st Q/DH	760020 - 760036
2nd Q/DH	760040 - 760056
3rd Q/DH	760060 - 760076

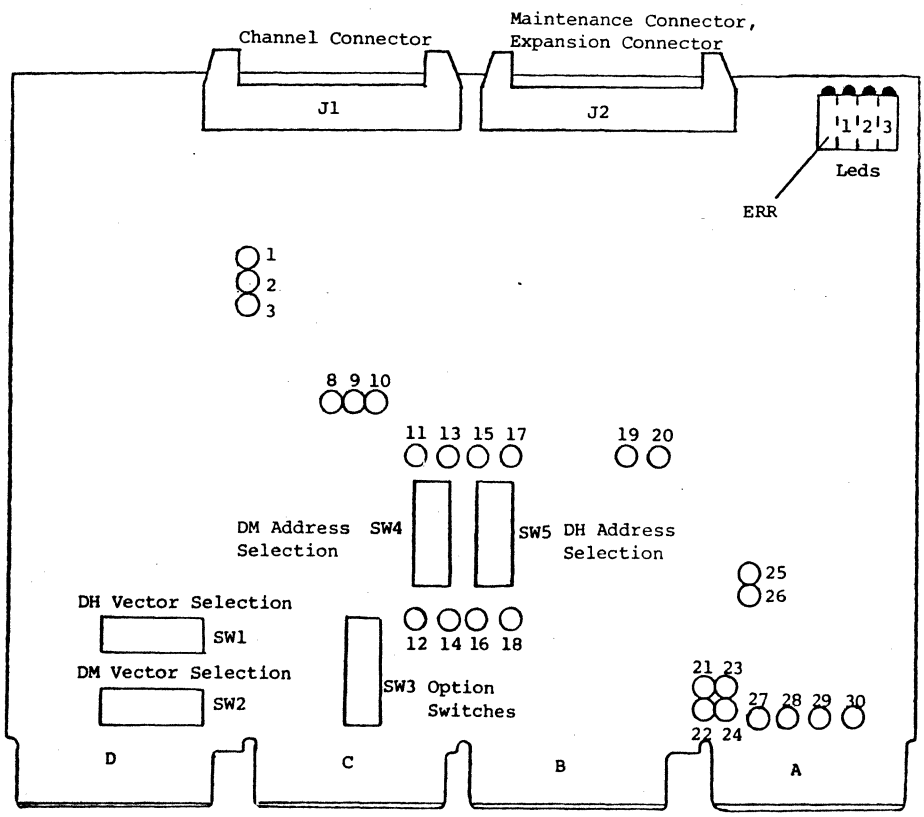


Figure 3-1: Q/DH Board Layout

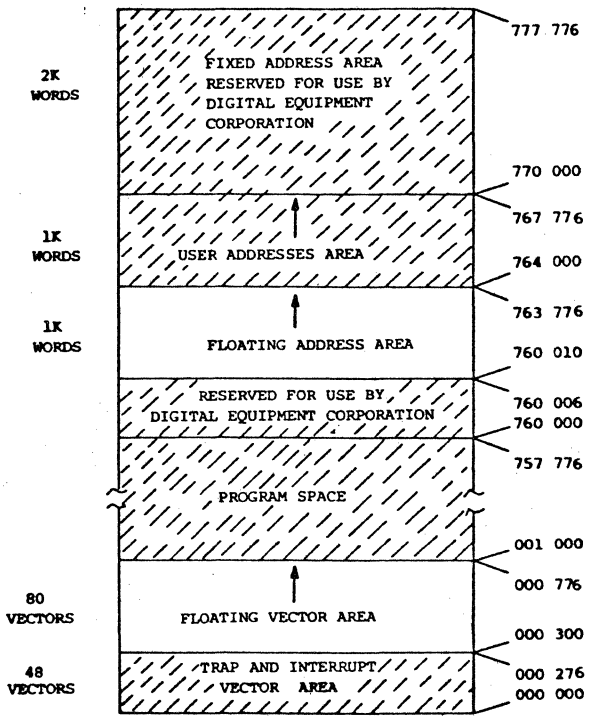


Figure 3-2: Address Map

Notice that, although the system in this example contains no DJ11 units, address 760010 cannot be assigned to the first Q/DH unit because it is not a multiple of 20 (octal).

Rank	Unibus Device	Q Bus Device
1	DJ11	
2	DH11,	Q/DH
3	DQ11	
4	DU11	DUV11
5	DPU11	
6	LK11A	
7	DMC11,DMR11	
8	DZ11, DZ/16	DZV11
9	KMC11	
10	RL11 (extra)	RLV11 (extra)

Table 3-1: Device Ranks for Floating Address Assignment

The DM portion of the Q/DH requires two additional consecutive word addresses. Available address space is from 770000 through 773770. The addresses assigned to the registers of the first DM in a system are 770500 and 770502. The addresses for additional DM registers start at consecutive addresses which are multiples of 10 (octal). Thus, the addresses for a second DM are 770510 and 770512; those for a third DM are 770520 and 770522; and so on.

The DH uses two interrupt vectors (for the receiver and transmitter interrupts). The DM uses one interrupt vector. Vector addresses for all devices are assigned in order from 300 through 774 according to the DEC rankings listed in Table 3-2. Find the device in your system with the lowest rank number and assign this 300, etc. Next find the device with the second lowest rank number and assign it the next consecutive vector address. Continue until all vector addresses are assigned. If a device is added to an existing system, its vector address must be inserted at the normal position and all other device addresses incremented accordingly. Table 3-3 shows the sample vector addresses for the Q/DH.

NUMBER	DEVICE TYPE	Q BUS DEVICE
1	DC11	
2	KL11, DL11-A,B, QUAD/B	DLV11,-F,-J
3	DP11	
4	DM11-A	
5	QUADRACALL, DN11	
6	DM11-BB,	Modem of Q/DH
7	DR11-A	DRV11-B
8	DR11-C, DUAL I/O	DRV11
9	PA611 Reader	
10	PA611 Punch	
11	DT11	
12	DX11	
13	DL11-C,D,E, QUAD/C,E	DLV11-E
14	DJ11	
15	DH11, DH/DM	Q/DH
16	GT40	
17	LPS11	
18	DQ11	
19	KW11-W	KWV11
20	DU11	DUV11

Table 3-2: Floating Interrupt Vector Device

Device	Channels		Vector
1st DM	0 - 15		300
2nd DM	0 - 15		304
1st DH	0 - 15	Receiver	310
		Transmitter	314
2nd DH	0 - 15	Receiver	320
		Transmitter	324

Table 3-3: Typical Vector Addresses

3.6 HOW TO SET THE DEVICE ADDRESS AND VECTOR SELECTION SWITCHES

3.6.1 DM Device Address Switch (S4)

Device addresses for the DM portion of the Q/DH are set using switch S4 on the board. Refer to Figure 3-1 for the location of switch S4 and Figure 3-3 for switch descriptions. Use Appendix A to determine the device address switch settings. The starting address can be determined by referring to the information in Section 3.5.

3.6.2 DH Device Address Switch (S5)

Device addresses for the DH portion of the Q/DH are set using switch S5. Refer to Figure 3-1 for the location of switch S5 and Figure 3-3 for switch descriptions. Use Appendix A to determine the device address switch settings. The starting address can be determined by referring to the information in Section 3.5.

NOTE

An open switch is accomplished by pressing the side of the switch marked "OPEN."

3.6.3 DM Vector Address Switch (S2)

Vector addresses for the DM portion of the Q/DH are set using switch S2. Refer to Figure 3-1 for the location of switch S2 on the board and Figure 3-3 for switch descriptions. Use Appendix B to determine the vector address switch settings. Section 3.5 describes how to determine the desired vector addresses.

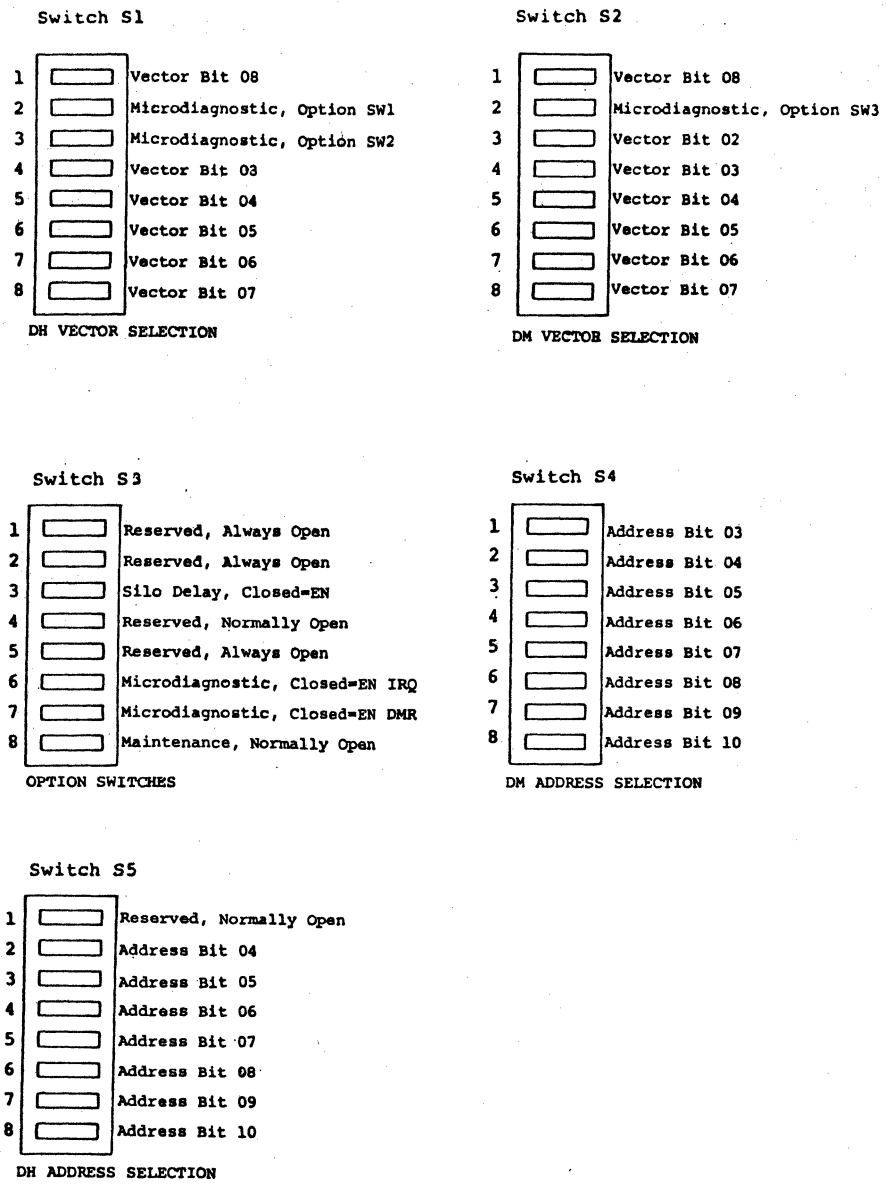


Figure 3-3: Q/DH Switch Descriptions

3.6.4 DH Vector Address Switch (S1)

Vector addresses for the DH portion of the Q/DH are set using switch S1 on the board. Refer to Figure 3-1 for the location of switch S1 and Figure 3-3 for switch descriptions. Use Appendix B to determine the vector address switch settings. To determine the desired vector addresses refer to Section 3.5.

3.6.5 Miscellaneous Functions

Switch S4 contains a variety of functions for the Q/DH. Appendix B lists these functions.

3.7 MAINTENANCE FEATURES

3.7.1 Maintenance Features

For maintenance purposes, there are six switch positions which control the resident microcoded diagnostic for the Q/DH. Refer to Table 3-4 for definitions and functions of these switches. Table 3-7 lists the execution sequence of the microdiagnostic.

For normal operation, set the switches as follows:

Switch S1, position 2 - Closed

Switch S1, position 3 - Open

Switch S2, position 2 - Open

Switch S3, position 6 - Open

Switch S3, position 7 - Open

Switch S3, position 8 - Open

Switch S3 Position	Function
1	Not Used.
2	Not Used.
3	When closed, enables the silo delay feature. The receiver interrupt is delayed by about 20ms if there are fewer than 16 characters in the input silo. This reduces the number of interrupts when a line is used as a link to another computer. When open,this switch disables the silo delay feature.
4	When open, transmission on a line is terminated in a manner identical to the DH11. When closed, a zero byte count will always terminate transmission on a line.
5	Not Used.
6	When closed, this switch runs the IRQ micro-test if in microdiagnostic maintenance mode.
7	When closed, runs the DMR micro-test if in microdiagnostic maintenance mode.
8	This switch is closed to disable the cable maintenance mode. It is normally open except when the Q/DH is used without an ABLE distribution panel.

Table 3-4: Switch S3 Functions

Switch	Setting	Function
S2-2		LOOP ON MICRODIAGNOSTIC (NO EMULATION)
	Open	Runs the microdiagnostic on power-up and exits to emulation when done.
	Closed	Remains in the microdiagnostic on power-up.
S1-2		HANG ON SECTION IN ERROR
	Open	Microdiagnostic continues when an error is encountered.
	Closed	Microdiagnostic hangs when an error is encountered.
S1-3		LOOP ON SECTION
	Open	Advances to next section at end of each section.
	Closed	Remains in current section is S6-1 is closed.
S3-6		RUN IRQ TEST
	Open	IRQ test will not be run.
	Closed	IRQ test will be run if LOOP ON MICRODIAGNOSTIC is set.
S3-7		RUN DMR TEST
	Open	DMR test will not be run.
	Closed	DMR test will be run if LOOP ON MICRODIAGNOSTIC is set.
S3-8		CABLE MAINTENANCE DISABLE
	Open	Allows microdiagnostic to detect when cables are installed in maintenance position. Will allow UART TEST to check EIA drivers and receivers.
	Closed	UART TEST will use internal loop-backs.

Table 3-5: Maintenance Switch Settings
(See notes on the following page.)

NOTE:

1. Bus and UART section are bypassed when switches are set to proceed into emulation due to the time required to perform the UART test, and because the Bus tests may disturb the system.

2. Any error detected in the first section of the microdiagnostic will cause a hang regardless of the switch settings.

3. The "ERR" indicator is reset at the beginning of each section of the microdiagnostic.

4. When running the bus tests, a "BR" instruction (777 octal) should be executed at location zero.

EXECUTION SEQUENCE	SECTION (as encoded in LEDs)
Power Up	
1	Section 7 - SEQ
2	Section 3 - DATA (2901)
3	Section 1 - DBIT
4	Section 5 - PROM
5	Section 4 - BUF
6	Section 6 - BUS (DMR, IRQ)
7	Section 2 - UART If S2-2 is open, Section 6 and 2 are bypassed and emulation is entered after Section 4.

Table 3-6: Microdiagnostic Execution Chart

3.7.2 Maintenance Display

The Q/DH contains four LEDs for maintenance display purposes. These LEDs are located at the top of the board. Figure 3-1 shows the location of the LEDs. Refer to Table 3-7 for descriptions of the LED displays. Section 3.12 provides more information on the LEDs.

DISPLAY				DESCRIPTION
ERR	1	2	3	
off	off	off	off	END PASS/ EMULATION
off	off	off	on	Testing Section 1 - DBIT
off	off	on	off	Testing Section 2 - UART
off	off	on	on	Testing Section 3 - DATA (2901)
off	on	off	off	Testing Section 4 - BUF
off	on	off	on	Testing Section 5 - PROM
off	on	on	off	Testing Section 6 - BUS (DMR, IRQ)
off	on	on	on	Testing Section 7 - SEQ
on	off	off	off	Error - Undefined problem
on	off	off	on	Error in Section 1 - DBIT Error
on	off	on	off	Error in Section 2 - UART Error
on	off	on	on	Error in Section 3 - DATA (2901) Error
on	on	off	off	Error in Section 4 - BUF Error
on	on	off	on	Error in Section 5 - PROM Error
on	on	on	off	Error in Section 6 - BUS Error
on	on	on	on	Error in Section 7 - SEQ Error

Table 3-7: Maintenance Display Chart

3.8 PRIORITY SELECTION

The standard priority interrupt levels for the Q/DH are IRQ5 for the DH and IRQ4 for the DM. These levels are factory wired and require no user adjustment.

If you wish to change interrupt levels for the DH or DM, use the strapping chart in Appendix C.

3.9 PREPARING YOUR SYSTEM FOR THE Q/DH

To prepare your system for installing the Q/DH, remove power from the system. Use either the front panel switch or the master breaker switch. We suggest that both switches be turned off.

Once power is removed from the system, locate a vacant quad slot to accomodate the Q/DH board. If a 16 line unit is being installed, locate two adjacent quad slots. Remove any previously installed bus grant continuity cards from this slot.

The Q/DH is designed to operate in a 4-level interrupt configuration. This means that it will moniter the bus for higher level interrupts. If a higher level interrupt occurs, then the Q/DH will pass the acknowledge signal to the next device on the bus. This allows use of the Q/DH in position-independent arbitration configurations.

If any single-level interrupt devices are used in a position-independent configuration, they must be placed at the end of the bus for arbitration to function properly.

3.10 HOW TO INSTALL THE Q/DH INTO YOUR SYSTEM

Prior to installing the Q/DH board, verify that the address and vector switches are set to the desired settings. Insert the board into the selected vacant slot, using the card guides to ensure that it is properly positioned. Insert the board so that it is firmly seated in the slot. If a 16 line unit is being installed, insert the expander board into the second slot and install the interconnect cable.

3.11 INSTALLATION VERIFICATION

3.11.1 ZDHM Diagnostics

The Dec ZDHM diagnostic can be used to verify operation of the Q/DH and/or your system. It should be noted, however, that the ZDHM diagnostic will not run as is. The 200 baud level must be disabled by using the patches listed in Table 3-8.

LOCATION	WAS	IS	MNEMONIC
12164	62737	4737	JSR PC, PATCH
12166	2100	40000	
12170	1220	240	NOP
12472	62737	4737	JSR PC, PATCH
12474	2100	40000	
12476	1220	240	NOP
40000	Don't Care	62737	ADD 2100,STMP7
40002	Don't Care	2100	
40004	Don't Care	1220	
40006	Don't Care	22737	CMP 200 BAUD, STMP7
40010	Don't Care	14600	
40012	Don't Care	1220	
40014	Don't Care	1771	BEQ PATCH
40016	Don't Care	207	RTS

Table 3-8: Patches to Dec Diagnostic ZDHM revision D0 for the Q/DH

3.11.2 Internal Diagnostics

Power can be applied once the Q/DH has been installed into the system. During the power-up sequence, the Q/DH performs an internal diagnostic. This diagnostic verifies a majority of internal operations of the Q/DH. With the maintenance switch set for normal operation, it does not check circuitry that is used to interface to the Q Bus.

The diagnostic mode is switch selectable. Refer to Section 3.7 for proper switch settings.

Proper internal operation of the Q/DH can be verified by monitoring four LEDs near the top of the board. Figure 3-1 shows the location of the LEDs. When power is applied, all four LEDs should light up and after a very short flash, should all turn off. Any LED which remains lit indicates a malfunction and requires investigation. Table 3-7 supplies the definitions of the four LEDs and Chapter 4 provides troubleshooting tips in case an LED remains lit.

If all four LED displays turn off after power has been applied to the system, address the Q/DH through the operator front panel or ODT. Examine the second address assigned to the Q/DH (address 76XXX2, the NRCR register). Immediately following application of power, the Q/DH microcode places the vector settings for the DH and DM devices in this register. Refer to Figure 3-4 for switch verification. If the vector settings are incorrect or the device does not respond, verify the vector and address settings as described in Section 3.5. Repeat the above operation.

If the micro-diagnostics passes, and the address and vector settings have been verified, continue to verify installation of the Q/DH by executing the software diagnostic.

CHAPTER 4

What To Do If Q/DH Does Not Work

4.1 HOW TO CARE FOR Q/DH

ABLE products are designed to provide years of service with a minimum of care. Here are a few tips to help you avoid problems.

* If a printed circuit board is frequently inserted and removed, it tends to build up a gum-like residue on the contacts. Clean this residue off using alcohol or freon. Use of a pencil eraser can remove some of the gold on the contacts, so if you choose to use one, go easy.

* Every six months remove each printed circuit board and clean off any accumulated dust. Dust can impede air flow. While the board is out, inspect it for any visual evidence of a potential problem such as damaged components, loose connections, etc.

* Schematics for your Q/DH can be ordered from the ABLE factory. Document numbers are listed below.

10176003 Q/DH PC Board

* If you wish to maintain a spare parts inventory. Refer to the recommended list in the appendix.

* If a problem arises with the operation of your Q/DH, follow the steps outlined in the following sections.

4.2 TROUBLESHOOTING TIPS

4.2.1 LEDs On

When the ERR LED remains lit, a failure in the micro-diagnostics is indicated. We suggest that you run the power-up sequence a few times to verify consistency of the ERR failure.

If either of the following conditions occur, switch S2 position 2 may be closed and should not be. Check this and all other switch settings.

* The ERR LED is off, but other LEDs are lit.

* If the ERR LED is lit, LED 2 is lit, LED 3 is off, and LED 1 is in either state.

If the above conditions persist, your Q/DH can be considered faulty. If so, contact the ABLE Product Support Center as outlined in Section 4.3.

An optional switch has been provided which allows progression into the emulation mode if an ERR has occurred in the micro-diagnostic. Section 3.7 provides information on how to set this switch.

In any case, an ERR failure should be reported to the ABLE Product Support Center so that it can be evaluated and resolved.

4.2.2 Verify Configuration And Installation

Experience has shown that the greatest number of problems with Q/DH involve configuration or installation errors. An address, vector, or interrupt level assignment may be inconsistent with system definitions. A correct assignment may be incorrectly specified in the system generation or incorrectly implemented by switch settings or jumper placements.

1. Using Sections 3.5 and 3.6 verify that address and vector assignments and switch settings are correct.

2. Using Section 3.8, check that interrupt level jumpers are correctly placed and are making contact.

3. Use a voltmeter to verify that the +5V and +12V are within +5% of their nominal value. If not, adjust the associated power supplies using the backplane listed in the Appendix E.

If a fault in a Q/DH board is indicated, call ABLE as described in sections 4.3 and 4.4.

4.3 CUSTOMER SERVICE

ABLE Computer's goal is to provide each customer with a product that works well in his system. We design and build our products to provide high reliability and to minimize problems. When a problem does arise, it is our intent to do everything in our power to quickly and efficiently solve it.

4.3.1 Who to Call for Service Within the United States

If your Q/DH does not function properly and you are within the United States, contact our Product Support Center before sending it for repair. Have serial numbers available when calling.

ABLE Computer
1732 Reynolds Avenue
Irvine, California 92714
(714) 979-7030
TWX 910-595-1729

If your product requires repair, we prefer that you return it to the factory. Use the original container or a corregated cardboard carton with at least one inch of cushioning material on all sides. Include a description of the problem and a hard copy of the failure mode or system dump when available. Be sure to include your name, address, and telephone number. Ship it to the above address.

4.3.2 Who to Call for Service Outside the United States

If your Q/DH does not function properly, contact your local distributor or telex ABLE Computer for the name and address of your local distributor:

TWX 910-595-1729

In Europe, telex our London office at:

Telex 848715 ABLE G

Or, our Haar by Munich office at:

Telex 5213883 ABLE D

CHAPTER 5

How To Use Q/DH

5.1 TYPICAL APPLICATIONS

The Q/DH connects a LSI-11 system to eight or sixteen terminals designed to interface with asynchronous communications lines. It provides direct memory access (DMA) output capabilities.

Figure 5-1 illustrates typical interfaces beween the Q/DH and local or remote terminals.

The Q/DH is used to interface with local terminal devices or, via modems and dedicated lines, with remote terminal devices. When commumicating with remote terminals via datasets that interface over switched networks, modem control is available for all lines.

5.2 TERMINAL/COMMUNICATIONS LINK INTERFACE INFORMATION

Table 5-1 lists the pin assignments on connectors J1 on the Q/DH. These connectors provide the interface with the external distribution system for a Q/DH.

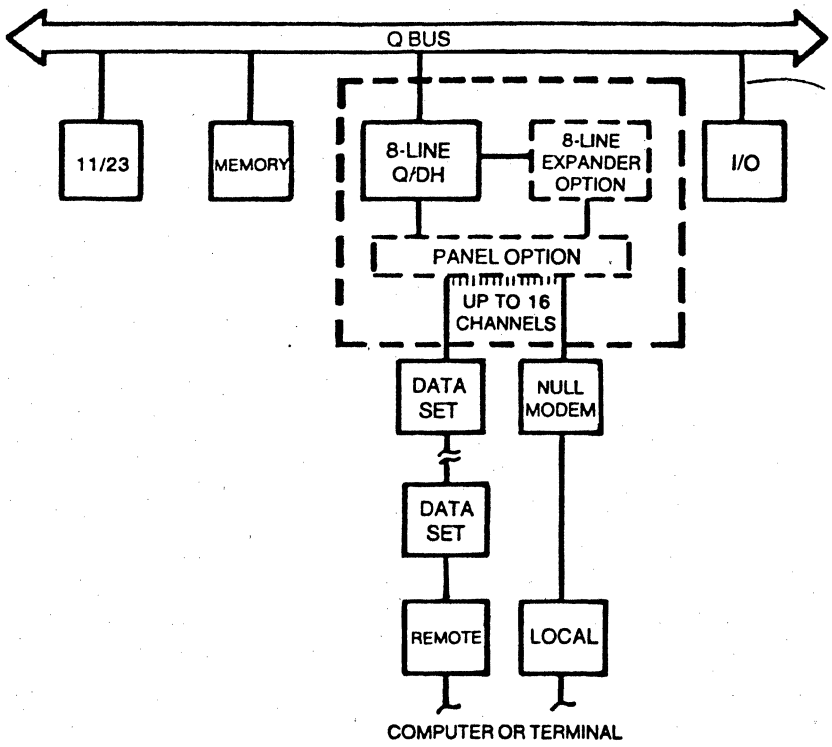


Figure 5-1: Q/DH Applications

J1			
DTR00-H	1	2	CARR00-H
DTR01-H	3	4	CARR01-H
DTR02-H	5	6	CARR02-H
DTR03-H	7	8	CARR03-H
DTR04-H	9	10	CARR04-H
DTR05-H	11	12	CARR05-H
DTR06-H	13	14	CARR06-H
DTR07-H	15	16	CARR07-H
MAINT-H	17	18	GND
TXD00-H	19	20	RING00-H
RXD00-H	21	22	GND
TXD01-H	23	24	RING01-H
RXD01-H	25	26	GND
TXD02-H	27	28	RING02-H
RXD02-H	29	30	+5V
TXD03-H	31	32	RING03-H
RXD03-H	33	34	+5V
TXD04-H	35	36	RING04-H
RXD04-H	37	38	+5
TXD05-H	39	40	RING05-H
RXD05-H	41	42	-12V
TXD06-H	43	44	RING06-H
RXD06-H	45	46	-12V
TXD07-H	47	48	RING07-H
RXD07-H	49	50	-12V

Table 5-1: Connectors on Q/DH Controller

5.3 Q BUS CONNECTOR INFORMATION

Tables 5-2 through 5-5 list Q Bus signals accepted or supplied by the Q/DH via the connectors on the board.

SIDE 1	CONNECTOR A PIN	SIDE 2
BIRQ5-L	A	+5V
BIRQ6-L	B	
BDAL16-L	C	GND
BDAL17-L	D	+12V
	E	BDOUT-L
	F	BRPLY-L
	H	BDIN-L
GND	J	BSYNC-L
	K	BWTBT-L
	L	BIRQ4-L
GND	M	BIAKI-L
BDMR-L	N	BIAKO-L
	P	BBS7-L
	R	BDMGI-L
	S	BDMGO-L
GND	T	BINIT-L
	U	BDAL00-L
	V	BDAL01-L

Table 5-2: Q/DH Controller Connector A Pin Assignments

SIDE 1	CONNECTOR B PIN	SIDE 2
BDCOK-H	A	+5V
	B	
BDAL18-L	C	GND
BDAL19-L	D	+12V
BDAL20-L	E	BDAL02-L
BDAL21-L	F	BDAL03-L
	H	BDAL04-L
GND	J	BDAL05-L
	K	BDAL06-L
	L	BDAL07-L
GND	M	BDAL08-L
BSACK-L	N	BDAL09-L
BIRQ7-L	P	BDAL10-L
	R	BDAL11-L
	S	BDAL12-L
GND	T	BDAL13-L
	U	BDAL14-L
+5	V	BDAL15-L

Table 5-3: Q/DH Controller Connector B Pin Assignments

SIDE 1	CONNECTOR C PIN	SIDE 2
	A	+ 5V
	B	
	C	GND
	D	+12V
	E	
	F	
	H	
GND	J	
	K	
	L	
	M	BIAKI-L
GND	N	BIAKO-L
	P	BUS-D05-L
	R	BDMGI-L
	S	BDMGO-L
GND	T	
	U	
	V	

Table 5-4: Q/DH Controller Connector C Pin Assignments

SIDE 1	CONNECTOR D PIN	SIDE 2
	A	+5V
	B	
	C	GND
	D	+12V
	E	
	F	
	H	
GND	J	
	K	
	L	
GND	M	
	N	
	P	
	R	
	S	
GND	T	
	U	
+5V	V	

Table 5-5: Q/DH Controller Connector D Pin Assignments

CHAPTER 6

How To Program Q/DH

6.1 DATA HANDLING REGISTERS

The data handling portion of Q/DH is software compatible with the DEC DH11. It contains eight Q Bus addressable registers. Table 6-1 contains general information about these registers. As illustrated in Figure 6-1, three of these are actually 16-register groups with one register for each line. When one of these groups is addressed, the register within the group is determined by the current line number in the four least significant bit positions of the system control register (SCR). Figure 6-2 illustrates register format. The following paragraphs describe the function of each register.

6.1.1 System Control Register

Bit	Description
15	Transmitter Interrupt. This read/write bit is set when the final character in a message buffer is loaded into a UART transmitter holding register. It causes an interrupt if bit 13 is set.
14	Storage Interrupt. This bit is set when a character transfer from a receiver holding register to the silo is inhibited because the silo is full. It causes an interrupt if bit 12 is set. This bit is read only in the normal mode and read/write in the maintenance mode. When not in the maintenance mode, the silo has a 255 character capacity.

REGISTER	ADDRESS	ACCESS	WORD/BYTE ADDRESSABLE
System Control Register	X00	Mixed See 6.1.1	Word/Byte
Next Received Character Register	X02	Read Only	Word Only
Line Parameter Register (Group)	X04	Read/Write	Word Only
Current Address Register	X06	Read/Write	Word Only
Byte Count Register (Group)	X10	Read/Write	Word Only
Buffer Active Register	X12	Read/Write	Word Only
Break Control Register	X14	Read/Write	Word Only
Silo Status Register	X16	Mixed See 6.1.8	Word/Byte

Table 6-1: Data Handling Register List

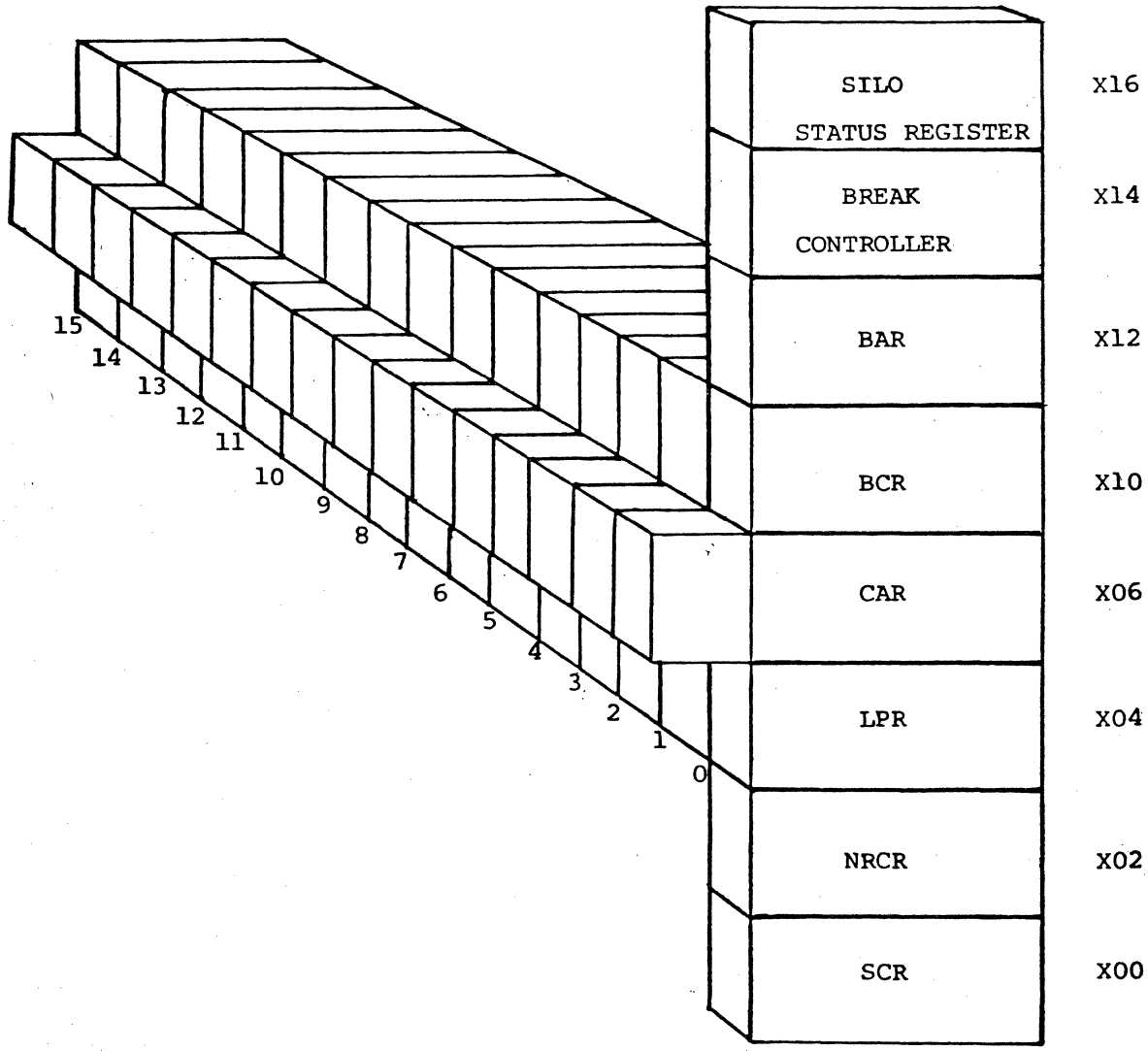
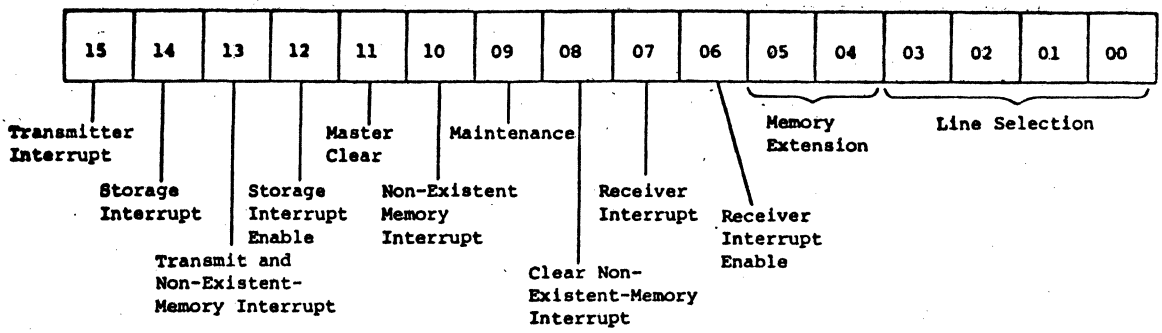
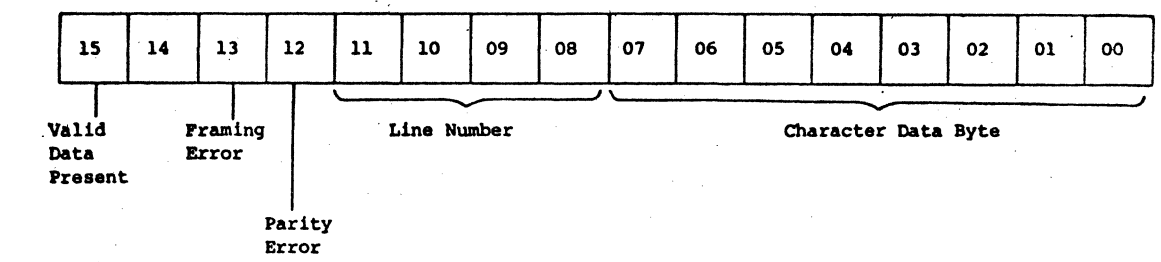


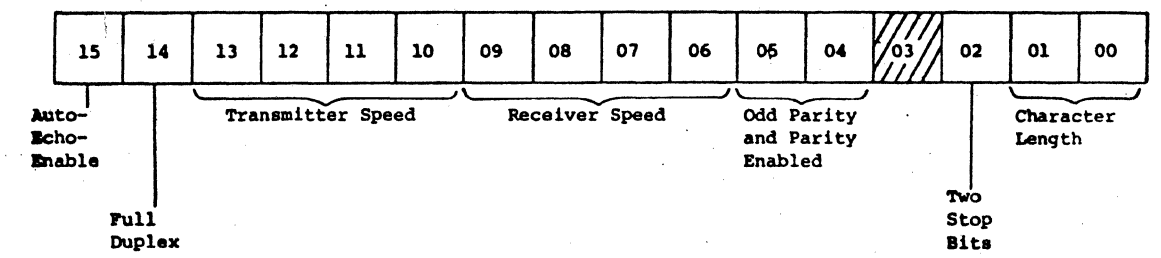
Figure 6-1: Data Handling Registers



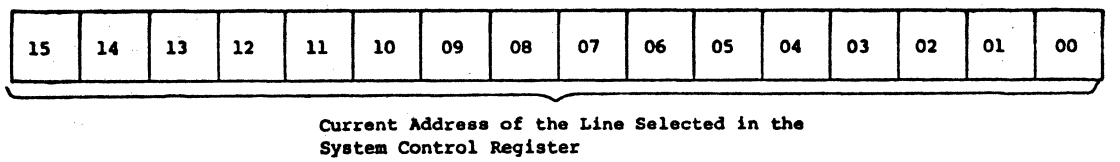
SYSTEM CONTROL REGISTER (X00) (See Section 6.1.1)



NEXT RECEIVED CHARACTER REGISTER (X02) (See Section 6.1.2)

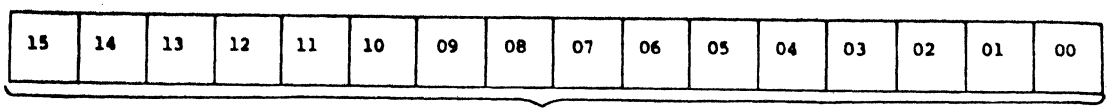


LINE PARAMETER REGISTER (X04) (See Section 6.1.3)

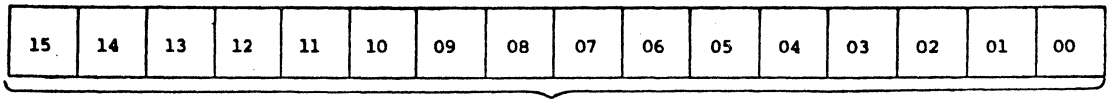


CURRENT ADDRESS REGISTER (X06) (See Section 6.1.4)

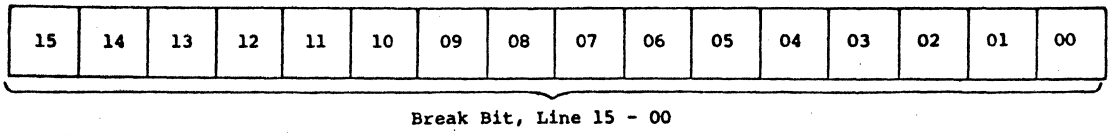
Figure 6-2: Data Handling Register Formats



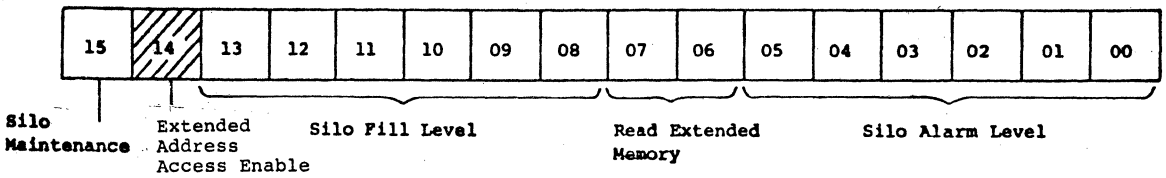
BYTE COUNT REGISTER (X10) (See Section 6.1.5)



BUFFER ACTIVE REGISTER (X12) (See Section 6.1.6)



BREAK CONTROL REGISTER (X14) (See Section 6.1.7)



SILO STATUS REGISTER (X16) (See Section 6.1.8)

Figure 6-2: Data Handling Register Formats (Con't.)

Bit	Description
13	Transmit and Non-Existent-Memory Interrupt Enable. When set, this read/write bit enables an interrupt in response to the setting of bits 10 or 15.
12	Storage Interrupt Enable. When set, this read/write bit enables an interrupt in response to the setting of bit 14.
11	Master Clear. When set, write only bit places the data handling portion of the Q/DH in the initialized status in which the silo, the UART's, and most register bits are cleared.
10	Non-Existent-Memory Interrupt. This bit is set if no RPLY response is received within 20 microseconds of the assertion of DIN by the Q/DH during a DMR transaction. The lack of response indicates that the addressed memory location does not exist. Setting this bit causes an interrupt if bit 13 is set. This bit is read only in the normal mode and read/write in the maintenance mode.
09	Maintenance. When set, this read/write bit places the Q/DH in the maintenance mode.
08	Clear Non-Existent-Memory Interrupt. When set, this bit clears bit 10 and itself.
07	Receiver Interrupt. This bit is set when the number of characters stored in the silo exceeds the alarm level specified by the low byte of the silo status register. It generates an interrupt if bit 06 is set. This bit is read only in the normal mode and is read/write in the maintenance mode. If there are fewer than sixteen characters in the silo and S3-3 is closed, there will be a delay of about 20ms before this bit is set. This reduces interrupt overhead when a line is used as a link to another computer.
06	Receiver Interrupt Enable. When set, this read/write bit enables an interrupt in response to the setting of bit 07.

Bit	Description
05,04	Memory Extension. When the program writes the current address register for the line selected by bits 03 through 00, read/write bits 05 and 04 are written into bits 17 and 16 of that current address register. When the system control register is read, the bit 05 and 04 values are those most recently written into these bit positions. Notice that these are not necessarily the current values of bits 17 and 16 of the Current Address Register for the currently selected line.
03 - 00	Line Selection. These read/write bits specify the line (horizontal) address of the register to be written or read when the line parameter, current address, or byte count register is addressed.

6.1.2 Next Received Character Register (X02)

Bit	Description
15	Valid Data Present. This bit is set when the remaining bit positions of the register contain valid information and is reset when the register is empty.
14	Data Overrun. This bit is set when at least one preceding character of the same message has been overwritten and lost in the UART holding register.
13	Framing Error. This bit is set when the current character is not framed by the programmed number of stop bits. This is usually interpreted as the reception of a break.
12	Parity Error. This bit is set when the current character exhibits incorrect parity as received from the line.
11 - 08	Line Number. These bits contain the number of the line from which the character was received.
07 - 00	Character Data Byte. This byte contains the data bits of a character from the line whose number appears in bits 11 through 08. When the character has less than eight data bits, these bits are right-justified and unused bits of the byte are zeros.

6.1.3 Line Parameter Register (X04)

Prior to transmitting or receiving messasges on a line, the program must define certain parameters for the line by writing the line parameter register. In order to write into the line parameter register for a line, that line number must first be written into the system control register. The line parameter register is a read/write operation register, but when read it reflects the value last written, and not the value for the currently selected line.

Bit	Description
15	Auto-Echo-Enable. When this bit is set, characters received on the line are automatically transmitted back (echoed) on the line by Q/DH.
14	Half/Full Duplex. In the full duplex mode (bit 14=0), transmission and reception can occur simultaneously. In half duplex mode (bit 14=1), the receiver is disabled when characters are being transmitted.
13 - 10	Transmitter Speed. These bits define the transmitter baud rate in the table following.

13	12	11	10	Speed (Baud)	13	12	11	10	Speed (Baud)
0	0	0	0	Zero	1	0	0	0	600
0	0	0	1	50	1	0	0	1	1200
0	0	1	0	75	1	0	1	0	1800
0	0	1	1	110	1	0	1	1	2400
0	1	0	0	134.5	1	1	0	0	4800
0	1	0	1	150	1	1	0	1	9600
0	1	1	0	Invalid	1	1	1	0	19200
0	1	1	1	300	1	1	1	1	Invalid

Table 6-2: Transmitter Baud Rate

NOTE

The following restrictions are associated with line speed selection:

1. Speed codes 6 (200 baud) and 15 (External B) are not valid.

2. One circuit has been provided for support of split speed operation. Differing receive and transmit speeds can be selected for a given line, however, the receive speed selected may not differ from some other split receive speed already in effect.

09 - 06 Receiver Speed. These bits define the receiver bit rate in the same manner and with the same restrictions that bits 13 - 10 define the transmitter baud rate.

Bit Description

05,04 Odd Parity and Parity Enabled. The combined states of these bits determine the parity generated by the UART transmitter and the parity required by the UART receiver for the line as follows:

05	04	Parity
0	0	None
0	1	Even
1	0	None
1	1	Odd

03 Not Used.

02 Two Stop Bits. When this bit is set, 1.5 stop bits are appended to transmitted characters having 5 data bits; and 2 stop bits are appended to transmitted characters having from 6 through 8 data bits. When this bit is reset, one stop bit is appended to all transmitted characters regardless of length. Recieved characters are always checked for one stop bit.

01,00 Character Length. These two bits specify the number of data bits in received and transmitted characters as follows:

01	00	Data Bits
0	0	5
0	1	6
1	0	7
1	1	8

6.1.4 Current Address Register (X06)

Prior to transmitting a message over a line, the program must write the starting address of the data buffer containing the message into the current address register for that line. This involves first writing the line number and the address extension bits into the system control register and then transferring the remainder of the starting address directly to the current address register. During this second transfer, Q Bus bits 00 through 15 are written into bit positions 00 through 15 of the current address register and the address extension bits from bit positions 04 and 05 of the system control register are written into bit positions 16 and 17 of the current address register.

To read the current address for a line, the program must write the line number into the system control register. It can then read bits 00 through 15 of the current address by reading the current address register and bits 16 through 17 by reading the silo status register which contains these bits in bit positions 06 and 07.

The Q/DH has an extended mode to allow 22 bit DMA operations. In this mode, the lower 16 bits are loaded as above. Then bit 14 of the silo status register is written with a one, and the upper 6 bits of the 22 bit address are written into the lower 6 bits of the current address register. At that time, bit 14 of the SSR is automatically cleared.

6.1.5 Byte Count Register (X10)

Prior to transmitting a message over a line, the program must also write the 2's complement of the number of characters (bytes) in the message into the byte count register. As in the case of the line parameter and current address register, the line number must first be written into the system control register in order to address the byte count register for the line. The byte count register can then be either written or read by the program.

6.1.6 Buffer Active Register (X12)

This register contains one bit for each line; bit n is for line n. The program sets bit n to start transmission of a message over line n after the message has been written in a data buffer in LSI-11 memory and the starting address and length of the data buffer have been transferred to the current address register and byte count register for the line. The Q/DH subsequently resets the bit for the line at the time that the last character of the message is loaded into the UART holding register. Because the Q/DH resets the bits in this register, the program must use BIS instructions to set these bits.

6.1.7 Break Control Register (X14)

This register contains one bit for each line; bit n is for line n. The program sets the bit for a line to start the transmission of a break on that line and resets the bit to terminate the transmission of the break. (Refer to paragraph 6.4 for break control timing information.)

6.1.8 Silo Status Register (X16)

Bit	Description
15	Silo Maintenance. When set, this read/write bit causes a fixed binary pattern to be sent to the silo for checking. To send more characters, this bit must be cleared and then set again.
14	Extended Address Access Enable. When this read/write bit is set, the upper 6 bits of the full 22 bit DMA address may be read from or written to the low 6 bits of the CAR. This bit is cleared when the CAR is accessed
13 - 08	Silo Fill Level. These read-only bits indicate the number of characters currently held in the silo. 000000 can indicate either an empty silo or a silo with more than 63 characters. For an empty silo, the valid data present bit (15) of the next received character register is reset while for a silo with more than 63 characters, it is set. Also, if an attempt has been made to load another character into a full silo, then the storage overflow bit (14) of the system control register is set.
07,06	Read Extended Memory. These read-only bits are A17 and A16 of the current address register for the line whose number is held in the line selection field (bits 03 through 00) of the system control register.
05 - 00	Silo Alarm Level. When the silo fill level exceeds the value written into this read/write field by the program, receiver interrupt bit 07 of the system control register is set. If receiver interrupt enable bit 06 of the system control register is set, this causes an interrupt. If there are fewer than sixteen characters in the silo and S3-3 is closed there will be a delay of 20ms before this bit is set. This reduces interrupt overhead when a line is used as a link to another computer.

6.2 MODEM REGISTERS

The DM portion implements a software compatible subset of the DEC DM11-BB. It contains two Q Bus addressable registers, the control and status register and the line status register. As illustrated in Figure 6-3, the byte-wide line status register is actually a register group

that includes one register for each line. When the line status register group is addressed, the particular register is read or written as determined by the line number held in the control and status register. The following paragraphs describe the two registers. Figure 6-4 illustrates register formats.

NOTE

The only actual signals are Ring, Carrier, and Data Terminal Ready. All others are simulated for software compatibility.

6.2.1 Control and Status Register

Bit	Description
15	Ring Flag. This read-only bit and DONE (bit 07) are set when a transition from OFF to ON is detected for the RING signal from the line specified by bits 03 through 00. Setting CLEAR SCAN (bit 01) resets the stored value of RING so that an existing ON condition appears as a transition and sets this bit and DONE.
14	Carrier Flag. This read-only bit and DONE (bit 07) are set when any transition of the CARRIER signal from the line specified by bits 03 through 00 is detected. Setting CLEAR SCAN (bit 11) resets the stored value of CARRIER so that an existing ON condition appears as a transition and sets this bit and DONE.
13	Clear to Send Flag. This read-only bit and DONE (bit 07) are set when any transition of the CLEAR TO SEND signal from the line specified by bits 03 through 00 is detected. Setting CLEAR SCAN (bit 11) resets the stored value of CLEAR TO SEND so that an existing ON conditon appears as a transition and sets this bit and DONE.

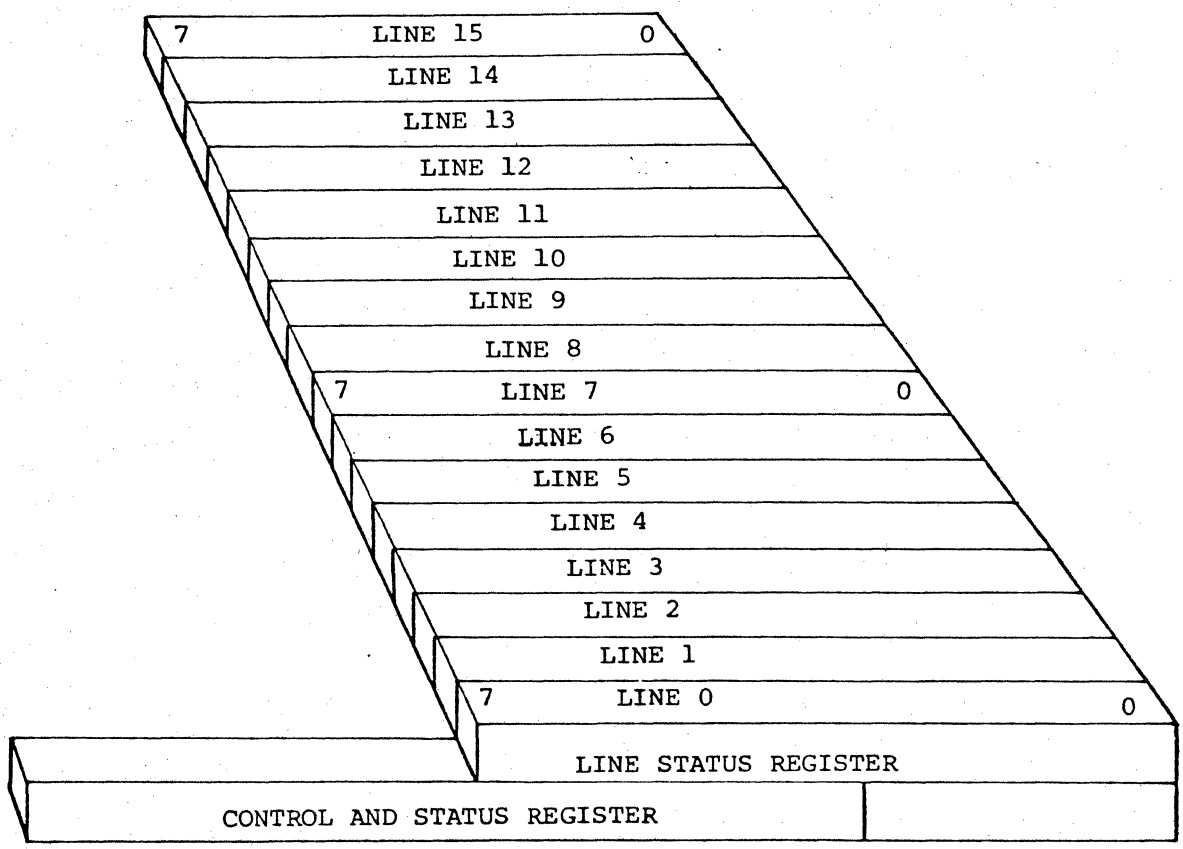
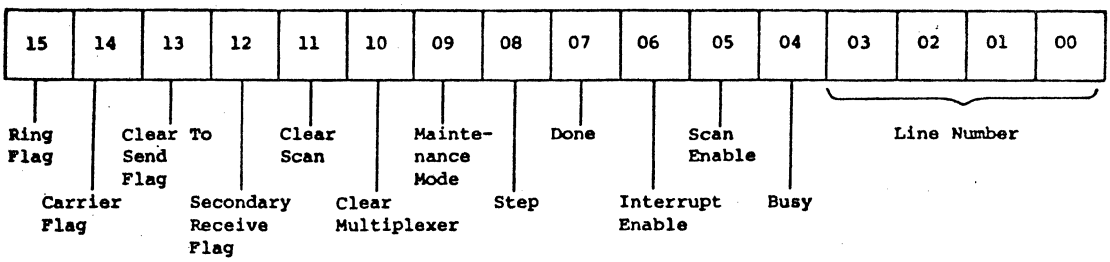
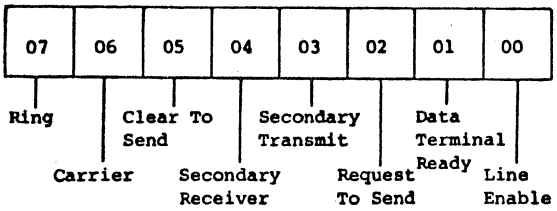


Figure 6-3: Modem Registers



CONTROL AND STATUS REGISTER (770XX0) (See Section 6.2.1)



LINE STATUS REGISTER (770XX2) (See Section 6.2.2)

Figure 6-4: Modem Register Formats

Bit	Description
12	Secondary Receive Flag. This read-only bit and DONE (bit 07) are set when any transition of the SECONDARY RECEIVE signal from the line specified by bits 03 through 00 is detected. Setting CLEAR SCAN (bit 11) resets the stored value of SECONDARY RECEIVE so that an existing ON condition appears as a transition and sets this bit and the DONE bit.
11	Clear Scan. Writing a ONE into this write-ONE-only bit clears bits 09, 07, 06, 05 and 03 through 00 and initiates a sequence which clears the scan memory. With the scan memory cleared, any ON condition of a RING, CARRIER, SEND, or SECONDARY RECEIVE signal is detected as a change of state during subsequent scanning and causes the associated change flag (bits 15 through 12) to set.
10	Clear Multiplexer. Writing a ONE into this write-ONE-only bit clears bits 03 through 00 (SECONDARY TRANSMIT, REQUEST TO SEND, DATA TERMINAL READY, LINE ENABLE) of all 16 line status registers.
09	Maintenance Mode. Setting this read/write bit forces the RING, CARRIER, CLEAR TO SEND, and SECONDARY RECEIVE inputs to the line scanner to the ON condition for test purposes. If this is preceded by the writing of a ONE into CLEAR SCAN (bit 11) then an interrupt (if enabled) should be generated for every line that is scanned.
08	Step. Each time that a ONE is written into this write-ONE-only bit, a STEP sequence is initiated. During this sequence, the line number held in bits 03 through 00 is incremented, signals from the newly addressed line are evaluated for transitions, and change flags (bit 15 through 12) and the DONE flag (bit 07) are set if any transitions are detected. This bit can be used rather than SCAN ENABLE (bit 05) to provide a scan rate controlled by the program. Note, however, that this scan rate should be high enough so that CARRIER signals will not switch ON and OFF during the interval between successive scans of a line. Note also, that DONE does not inhibit STEP.

Bit	Description
07	Done. This read/write bit is set when bit 15, 14, 13, or 12 sets. With DONE set, the line scanner is disabled so that bits 03 through 00 contain the number of the line associated with the condition which causes DONE to set. If INTERRUPT ENABLE bit 06 is also set, an interrupt routine normally resets DONE so as to release the line scanner. This bit is also reset by INITIALIZE and by CLEAR SCAN (bit 11).
06	Interrupt Enable. When this read/write bit is set, the DM interrupt function is enabled. The bit is cleared by INITIALIZE and by CLEAR SCAN (bit 11).
05	Scan Enable. When this read/write bit is set the DM is placed in the automatic scanning mode. In this mode, the scanner increments the line number held in bits 03 through 00 and checks for transitions of the signals from the newly addressed line until a transition is found. At this time the appropriate transition flag (bits 15 through 12) and DONE (bit 07) are set. Scanning is then inhibited until the program resets the DONE bit.
04	Busy. This read-only bit is set when lines are being scanned. The program should change line numbers (bits 03 through 00) only when BUSY is 0.
03 - 00	Line Number. These read/write bits, held in a counter, point to one of the 16 line-status registers and select inputs from one of the 16 lines for transition detection. The line number is incremented at the start of each scan cycle and is reset to 0000 by INITIALIZE or by CLEAR SCAN (bit 11). Notice, that since the incrementing of the count occurs at the start of each scan cycle, the first line tested after a reset is 0001 rather than 0000.

6.2.2 Line Status Register

Bit	Description
07	Ring. This read-only bit indicates the status of the modem RING signal.
06	Carrier. This read-only bit indicates the status of the modem CARRIER signal.
05	Clear to Send. This read-only bit indicates the

status of the modem CARRIER signal. This is done for software compatibility.

04 Secondary Receive. This bit is a read-only copy of the SECONDARY TRANSMIT bit (03).

03 Secondary Transmit. This bit is copied into SECONDARY RECEIVE (04) for diagnostic compatibility. This bit is reset by INITIALIZE or by CLEAR MUX (bit 10) of the control and status register.

02 Request to Send. This bit is not used. The bit is cleared by INITIALIZE and CLEAR MUX. It is read/write.

01 Data Terminal Ready. This bit allows the modem to maintain the data mode. It is cleared by INITIALIZE and CLEAR MUX. This bit is read/write.

00 Line Enable. This bit enables the state of RING, CARRIER, CLEAR TO SEND, and SEC RX to be sampled by the program and tested for transitions. It is cleared by INITIALIZE and CLEAR MUX. This bit is read/write.

6.3 TRANSMITTER/RECEIVER SPEED PROGRAMMING CONSIDERATIONS

IN THE DH11, speed code 1110 selects External Input A. In the Q/DH, this speed code selects 19.2K baud. In the DH11, speed code 0110 selects 200 baud and speed code 1111 selects External Input B. In the Q/DH these speed codes are invalid.

NOTE

The 19200 baud rate has a clock error of +3.125%. If the Q/DH is used with a device having the same error there will be no problem.

In the Q/DH, different non-zero receiver and transmitter speeds can be selected for a given line only if one of these rates is obtained from the source shared by the 200 baud and External B speed codes. If this restriction is not observed, the programmed transmitter speed determines both the transmitter and the receiver speeds for the line.

The zero baud selection provides the means by which the program can turn off any line. A useful application of this capability involves turning off unused line receivers in the presence of excessive circuit noise so as to avoid the receipt of spurious characters.

6.4 BREAK CONTROL TIMING

In order to time the transmission of a break so that no significant message characters are lost, the transmitter interrupt associated with a dummy message containing two null characters is used to time the setting of the BREAK bit for the line.

The use of the dummy message is necessary because the transmitter interrupt indicates the completion of the message transfer from the message buffer in the computer memory to the Q/DH rather than the completion of the message transmission by the Q/DH. This interrupt timing allows the program to write message (n + 1) in the message buffer and write the starting address and word count for this message while the final characters of message n are being transmitted. Specifically, at the time of the transmitter interrupt, there are two message characters still to be transmitted, one in the UART transmit holding register. Thus, by using the interrupt associated with the dummy message to time the setting of the BREAK bit, the break is started when the two null characters of this message reside in these registers. (The break begins at the instant that the BREAK bit for the line is set in the break control register.)

A second dummy message can be used to time the duration of the break. This message should be made up of null characters, since the last two characters are actually transmitted after the transmitter interrupt associated with the message has been used to time the resetting of the BREAK bit for the line. This timing method provides a break duration equal to the character period times the number of characters in the second dummy message. (The break ends before the final two characters of the second dummy message are transmitted but it includes the two character periods of the first dummy message transmission.)

6.5 TRANSMITTER AND RECEIVER TIMING CONSIDERATIONS

Because characters are transmitted asynchronously, message integrity is not affected by the speed with which characters are supplied to the UART. Continuous transmission is achieved if the UART transmit holding register receives character (n + 1) during the period when character n is being transmitted. Since the Q/DH uses word accesses to LSI-11 memory, only one DMA access is required for every two transmit characters. However, to maintain continuous transmission each access must be completed within one character period of its initiation.

The 255-word silo provides buffer storage for received characters. If the silo becomes full, then characters cannot be transferred to it from UART receiver holding registers. Thus, if this happens, characters may be overwritten in one or more UART modules. The amount of time that the program has to service a receiver interrupt depends upon the number of lines from which messages are currently being received, the receiver speeds, and the silo alarm level value that has been written in the silo status register. A low silo alarm level value increases the time available to respond to the interrupt. However, if the program responds immediately, the lower value increases program overhead because more interrupts will have to be serviced to transfer a given number of characters. The Q/DH decreases this overhead by interrupting after sixteen characters have been received or after 20ms have passed since the first character is received.

If the transfer of a character from the holding register of a UART receiver has to be inhibited because the silo is full, STORAGE INTERRUPT bit 14 of the system control register is set and if STORAGE INTERRUPT ENABLE bit 12 is set, an interrupt request is initiated to inform the program that the silo is full. The program may still have time to empty the silo before an overrun occurs.

6.6 MAINTENANCE MODE CONSIDERATIONS

When maintenance (bit 09 of the system control register) is set, the UART modules are placed in the local loopback mode. In this mode, the receiver input from the line is ignored, the transmitter output to the line is held at the marking level, and the serial output from each UART transmitter shift register is connected to the serial input of the receiver shift register so that each charater transmitted by the transmitter section is received by the receiver section. The silo is reduced to 64 words.

Also, when MAINTENANCE is set, the LSI-11 program can write the STORAGE INTERRUPT, NON-EXISTENT-MEMORY INTERRUPT, and RECEIVER-INTERRUPT (system control register bits 14, 10, and 07) which are normally read only.

When SILO MAINTENANCE (bit 15 of the silo status register) is set, a 1010101010101010 is loaded into the silo. Each successive clearing and setting of SILO MAINTENANCE loads another copy of this pattern into the silo. In order to fill the silo with this test pattern, all receiver speeds must be set to zero baud and the silo must be emptied of previously received characters.

When J1 Pin 17 is not shorted, the following occurs:

* Silo size is reduced to 64 words.
* Secondary transmit and secondary receive are internally looped together.
* Clear to Send is the same as Carrier.
* Ring and Request to Send are internally looped together.

CHAPTER 7

How the Q/DH Works

7.1 ARCHITECTURE

The Q/DH is a microprocessor-based unit organized around an 8-bit internal data bus (DB00-DB07). The use of an 8-bit microprocessor and an 8-bit internal data bus holds etch density at a reasonable level, enhancing reliability.

The 1024-byte buffer and 2901 microprocessor can be either read or written from the internal bus via bi-directional ports. Every other element that interfaces with the bus is limited to either input access or output access. Data can be transferred over the bus from any element having output access to any element having input access.

The interface between the internal data bus and the Q Bus involves two byte-wide registers.

Words received from the Q Bus are loaded into the data/address input low-byte and data/address input high-byte registers. The two bytes of the word are then transferred separately over the internal data bus.

The two bytes of a word to be transferred from the Q/DH to the Q Bus are written into the data/address output low-byte and data/address ouput high-byte registers These registers are gated simultaneously onto the Q Bus during the word transfer time.

7.2 ASYNCHRONOUS SERIAL LINE INTERFACES

A Universal Asynchronous Receiver-Transmitter (UART) module is provided for each of the 8 asynchronous serial lines. The UART modules make the conversions between the parallel bytes supplied and accepted by the host processor, and asynchronous serial characters exhibiting the appropriate format. The character format and the receive-transmit rate for each line are controlled by information written into the parameter register for the line by the program. The line parameters for each line are maintained in mode registers of the UART module assigned to the line.

Registers in the UART modules are read and written via an 8-bit UART data bus (UB00 through UB07). This bus interfaces with the internal data bus via two registers, one which buffers bytes directed from the internal data bus to a UART and the other which buffers bytes directed from a UART to the internal data bus.

The serial transmit-data outputs from the UART modules are applied to BREAK gates. The enabling of the BREAK gates is controlled by the "RTS" signal in the UARTS. Setting this bit results in the application of a spacing level to the associated transmit line, independently of the transmit-data signal being supplied by the associated UART module.

Receive-data signals from the 8 lines are accepted by data receivers whose outputs are applied to the UARTs.

In addition to the data signal interfaces with the asynchronous serial lines, the Q/DH controls one modem signal [Data Terminal Ready (DTR)] directed to each line and monitors two modem signals (CARRIER and RING) received from each line. The DTR lines are controlled by the "DTR" bits in the UARTs. The CARRIER signal is gated onto the internal data bus. The RING signal is connected to the "DSR" input of the UARTS.

The expander board implements a second set of 8 lines.

7.3 MICROPROGRAM ARCHITECTURE

The microprogram is divided into routines which service specific events. Each event is assigned a priority. When a service routine is ready to yield control, the event status is evaluated and control is passed to the routine for the highest priority event that is currently pending. (The lowest priority is assigned to a default event which, by

definition, is always pending.) One class of events involves the reading or writing of a device register by the host processor program. In this case, control passes to a routine which services the reading or writing of the particular device register that is being addressed.

7.4 Q BUS ADDRESS INTERFACE

The Q Bus address interface contains a set of switches for assigning the address of the DH and a set for the DM. The micro-program disables the DM set when the DM vector is set to zero.

7.5 Q BUS INTERRUPTS

The microprocessor initiates interrupt requests to the host processor via the Q Bus request interface section of the Q/DH. The Q Bus request interface section implements the protocol required to obtain Q Bus mastery. The obtaining of Q Bus mastery appears as an event which causes control to be passed to a servicing routine. This routine places the correct vector in the data output registers and gates it to the Q Bus data/address lines. The Q Bus request interface section is then commanded to assert the RPLY signal.

The vectors are set in switches which are read over the internal data bus.

7.6 BUFFER RAM, TABLE PROM, AND ASSOCIATED ELEMENTS

The 1024-byte buffer RAM can be read and written from the internal data bus. This memory is used to contain the input silo, some of the registers accessible from the Q Bus, and various registers used by the emulation firmware.

The 1024-byte table PROM can be read from the internal data bus. This table memory is used to perform functions which would otherwise take an excessive number of micro-instructions.

The Memory Address Register (MAR), writable from the internal data bus, is used to address these two memories in conjunction with eight micro-instruction bits in a fixed base, variable offset format.

7.7 UART ADDRESS REGISTER AND ASSOCIATED ELEMENTS

One of the elements that can be written from the internal data bus is the UART Address Register (UAR). During a transaction with a UART, this stored address is decoded to produce the chip-enable signal which determines the particular UART selected for the transaction.

Bit 3 of this register is used to select the 8-line group to be involved with the current UART operation. A zero selects the controller board, and a one selects the expander board.

7.8 DIAGNOSTIC LIGHT EMITTING DIODES

When power is applied to the Q/DH a diagnostic program is run before the emulation program is entered. Associated with this program are four light-emitting diodes (LEDs) identified by silk-screening as ERR, 1, 2, and 3. At power turn-on, all four of these indicators are turned on by the hardware. As the diagnostic runs, the states of LEDs 1 through 3 change to display binary values indicating different sections of the diagnostic program as these sections are executed. If the diagnostic runs successfully, all four of the LEDs are turned off at the time that the emulation is entered and remain off until another power turn-on. Thus, if the ERR indicator remains lit, a problem is indicated. The number displayed on LEDs 1 through 3 then provides information about the nature of the problem.

In general, any error prevents the entrance to the emulation microprogram. This causes the Q/DH to not respond to software, and, depending on the operating system, is configured out of the system. A switch setting overrides this condition and allows the emulation program to be entered even if a problem is detected. However, if the first section of the diagnostic cannot be completed, the emulaton program is not entered. In this case, all four LEDs remain lit.

Since the diagnostic program verifies most internal Q/DH functions, successful completion of the diagnostic provides a strong indication that any problem that is encountered arises from some external source such as an installation error.

APPENDIX A

Address Switch Settings

This appendix contains the switch settings for the DH and DM (modem) addresses.

DM Address	Switch 8	7	6	5	4	3	2	1	DM Address	Switch 8	7	6	5	4	3	2	1
770000	C	C	C	C	C	C	C	C	770550	C	C	-	C	-	-	C	-
770010	C	C	C	C	C	C	C	-	770560	C	C	-	C	-	-	-	C
770020	C	C	C	C	C	C	-	C	770570	C	C	-	C	-	-	-	-
770030	C	C	C	C	C	C	-	-	770600	C	C	-	-	C	C	C	C
770040	C	C	C	C	C	-	C	C	770610	C	C	-	-	C	C	C	-
770050	C	C	C	C	C	-	C	-	770620	C	C	-	-	C	C	-	C
770060	C	C	C	C	C	-	-	C	770630	C	C	-	-	C	C	-	-
770070	C	C	C	C	C	-	-	-	770640	C	C	-	-	C	-	C	C
770100	C	C	C	C	-	C	C	C	770650	C	C	-	-	C	-	C	-
770110	C	C	C	C	-	C	C	-	770660	C	C	-	-	C	-	-	C
770120	C	C	C	C	-	C	-	C	770670	C	C	-	-	C	-	-	-
770130	C	C	C	C	-	C	-	-	770700	C	C	-	-	-	C	C	C
770140	C	C	C	C	-	-	C	C	770710	C	C	-	-	-	C	C	-
770150	C	C	C	C	-	-	C	-	770720	C	C	-	-	-	C	-	C
770160	C	C	C	C	-	-	-	C	770730	C	C	-	-	-	C	-	-
770170	C	C	C	C	-	-	-	-	770740	C	C	-	-	-	-	C	C
770200	C	C	C	-	C	C	C	C	770750	C	C	-	-	-	-	C	-
770210	C	C	C	-	C	C	C	-	770760	C	C	-	-	-	-	-	C
770220	C	C	C	-	C	C	-	C	770770	C	C	-	-	-	-	-	-
770230	C	C	C	-	C	C	-	-	771000	C	-	C	C	C	C	C	C
770240	C	C	C	-	C	-	C	C	771010	C	-	C	C	C	C	C	-
770250	C	C	C	-	C	-	C	-	771020	C	-	C	C	C	C	-	C
770260	C	C	C	-	C	-	-	C	771030	C	-	C	C	C	C	-	-
770270	C	C	C	-	C	-	-	-	771040	C	-	C	C	C	-	C	C
770300	C	C	C	-	-	C	C	C	771050	C	-	C	C	C	-	C	-
770310	C	C	C	-	-	C	C	-	771060	C	-	C	C	C	-	-	C
770320	C	C	C	-	-	C	-	C	771070	C	-	C	C	C	-	-	-
770330	C	C	C	-	-	C	-	-	771100	C	-	C	C	-	C	C	C
770340	C	C	C	-	-	-	C	C	771110	C	-	C	C	-	C	C	-
770350	C	C	C	-	-	-	C	-	771120	C	-	C	C	-	C	-	C
770360	C	C	C	-	-	-	-	C	771130	C	-	C	C	-	C	-	-
770370	C	C	C	-	-	-	-	-	771140	C	-	C	C	-	-	C	C
770400	C	C	-	C	C	C	C	C	771150	C	-	C	C	-	-	C	-
770410	C	C	-	C	C	C	C	-	771160	C	-	C	C	-	-	-	C
770420	C	C	-	C	C	C	-	C	771170	C	-	C	C	-	-	-	-
770430	C	C	-	C	C	C	-	-	771200	C	-	C	-	C	C	C	C
770440	C	C	-	C	C	-	C	C	771210	C	-	C	-	C	C	C	-
770450	C	C	-	C	C	-	C	-	771220	C	-	C	-	C	C	-	C
770460	C	C	-	C	C	-	-	C	771230	C	-	C	-	C	C	-	-
770470	C	C	-	C	C	-	-	-	771240	C	-	C	-	C	-	C	C
770500	C	C	-	C	-	C	C	C	771250	C	-	C	-	C	-	C	-
770510	C	C	-	C	-	C	C	-	771260	C	-	C	-	C	-	-	C
770520	C	C	-	C	-	C	-	C	771270	C	-	C	-	C	-	-	-
770530	C	C	-	C	-	C	-	-	771300	C	-	C	-	-	C	C	C
770540	C	C	-	C	-	-	C	C	771310	C	-	C	-	-	C	C	-

Table A-1: DM Address Switch Settings (SW4)

DM Address	Switch 8	7	6	5	4	3	2	1	DM Address	Switch 8	7	6	5	4	3	2	1
771320	C	-	C	-	-	C	-	C	772070	-	C	C	C	C	-	-	-
771330	C	-	C	-	-	C	-	-	772100	-	C	C	C	-	C	C	C
771340	C	-	C	-	-	-	C	C	772110	-	C	C	C	-	C	C	-
771350	C	-	C	-	-	-	C	-	772120	-	C	C	C	-	C	-	C
771360	C	-	C	-	-	-	-	C	772130	-	C	C	C	-	C	-	-
771370	C	-	C	-	-	-	-	-	772140	-	C	C	C	-	-	C	C
771400	C	-	-	C	C	C	C	C	772150	-	C	C	C	-	-	C	-
771410	C	-	-	C	C	C	C	-	772160	-	C	C	C	-	-	-	C
771420	C	-	-	C	C	C	-	C	772170	-	C	C	C	-	-	-	-
771430	C	-	-	C	C	C	-	-	772200	-	C	C	-	C	C	C	C
771440	C	-	-	C	C	-	C	C	772210	-	C	C	-	C	C	C	-
771450	C	-	-	C	C	-	C	-	772220	-	C	C	-	C	C	-	C
771460	C	-	-	C	C	-	-	C	772230	-	C	C	-	C	C	-	-
771470	C	-	-	C	C	-	-	-	772240	-	C	C	-	C	-	C	C
771500	C	-	-	C	-	C	C	C	772250	-	C	C	-	C	-	C	-
771510	C	-	-	C	-	C	C	-	772260	-	C	C	-	C	-	-	C
771520	C	-	-	C	-	C	-	C	772270	-	C	C	-	C	-	-	-
771530	C	-	-	C	-	C	-	-	772300	-	C	C	-	-	C	C	C
771540	C	-	-	C	-	-	C	C	772310	-	C	C	-	-	C	C	-
771550	C	-	-	C	-	-	C	-	772320	-	C	C	-	-	C	-	C
771560	C	-	-	C	-	-	-	C	772330	-	C	C	-	-	C	-	-
771570	C	-	-	C	-	-	-	-	772340	-	C	C	-	-	-	C	C
771600	C	-	-	-	C	C	C	C	772350	-	C	C	-	-	-	C	-
771610	C	-	-	-	C	C	C	-	772360	-	C	C	-	-	-	-	C
771620	C	-	-	-	C	C	-	C	772370	-	C	C	-	-	-	-	-
771630	C	-	-	-	C	C	-	-	772400	-	C	-	C	C	C	C	C
771640	C	-	-	-	C	-	C	C	772410	-	C	-	C	C	C	C	-
771650	C	-	-	-	C	-	C	-	772420	-	C	-	C	C	C	-	C
771660	C	-	-	-	C	-	-	C	772430	-	C	-	C	C	C	-	-
771670	C	-	-	-	C	-	-	-	772440	-	C	-	C	C	-	C	C
771700	C	-	-	-	-	C	C	C	772450	-	C	-	C	C	-	C	-
771710	C	-	-	-	-	C	C	-	772460	-	C	-	C	C	-	-	C
771720	C	-	-	-	-	C	-	C	772470	-	C	-	C	C	-	-	-
771730	C	-	-	-	-	C	-	-	772500	-	C	-	C	-	C	C	C
771740	C	-	-	-	-	-	C	C	772510	-	C	-	C	-	C	C	-
771750	C	-	-	-	-	-	C	-	772520	-	C	-	C	-	C	-	C
771760	C	-	-	-	-	-	-	C	772530	-	C	-	C	-	C	-	-
771770	C	-	-	-	-	-	-	-	772540	-	C	-	C	-	-	C	C
772000	-	C	C	C	C	C	C	C	772550	-	C	-	C	-	-	C	-
772010	-	C	C	C	C	C	C	-	772560	-	C	-	C	-	-	-	C
772020	-	C	C	C	C	C	-	C	772570	-	C	-	C	-	-	-	-
772030	-	C	C	C	C	C	-	-	772600	-	C	-	-	C	C	C	C
772040	-	C	C	C	C	-	C	C	772610	-	C	-	-	C	C	C	-
772050	-	C	C	C	C	-	C	-	772620	-	C	-	-	C	C	-	C
772060	-	C	C	C	C	-	-	C	772630	-	C	-	-	C	C	-	-

Table A-1: DM Address Switch Settings (SW4) (Con't.)

DM Address	Switch 8	7	6	5	4	3	2	1
772640	-	C	-	-	C	-	C	C
772650	-	C	-	-	C	-	C	-
772660	-	C	-	-	C	-	-	C
772670	-	C	-	-	C	-	-	-
772700	-	C	-	-	-	C	C	C
772710	-	C	-	-	-	C	C	-
772720	-	C	-	-	-	C	-	C
772730	-	C	-	-	-	C	-	-
772740	-	C	-	-	-	-	C	C
772750	-	C	-	-	-	-	C	-
772760	-	C	-	-	-	-	-	C
772770	-	C	-	-	-	-	-	-
773000	-	-	C	C	C	C	C	C
773010	-	-	C	C	C	C	C	-
773020	-	-	C	C	C	C	-	C
773030	-	-	C	C	C	C	-	-
773040	-	-	C	C	C	-	C	C
773050	-	-	C	C	C	-	C	-
773060	-	-	C	C	C	-	-	C
773070	-	-	C	C	C	-	-	-
773100	-	-	C	C	-	C	C	C
773110	-	-	C	C	-	C	C	-
773120	-	-	C	C	-	C	-	C
773130	-	-	C	C	-	C	-	-
773140	-	-	C	C	-	-	C	C
773150	-	-	C	C	-	-	C	-
773160	-	-	C	C	-	-	-	C
773170	-	-	C	C	-	-	-	-
773200	-	-	C	-	C	C	C	C
773210	-	-	C	-	C	C	C	-
773220	-	-	C	-	C	C	-	C
773230	-	-	C	-	C	C	-	-
773240	-	-	C	-	C	-	C	C
773250	-	-	C	-	C	-	C	-
773260	-	-	C	-	C	-	-	C
773270	-	-	C	-	C	-	-	-
773300	-	-	C	-	-	C	C	C
773310	-	-	C	-	-	C	C	-
773320	-	-	C	-	-	C	-	C
773330	-	-	C	-	-	C	-	-
773340	-	-	C	-	-	-	C	C
773350	-	-	C	-	-	-	C	-
773360	-	-	C	-	-	-	-	C
773370	-	-	C	-	-	-	-	-
773400	-	-	-	C	C	C	C	C
773410	-	-	-	C	C	C	C	-
773420	-	-	-	C	C	C	-	C
773430	-	-	-	C	C	C	-	-
773440	-	-	-	C	C	-	C	C
773450	-	-	-	C	C	-	C	-
773460	-	-	-	C	C	-	-	C
773470	-	-	-	C	C	-	-	-
773500	-	-	-	C	-	C	C	C
773510	-	-	-	C	-	C	C	-
773520	-	-	-	C	-	C	-	C
773530	-	-	-	C	-	C	-	-
773540	-	-	-	C	-	-	C	C
773550	-	-	-	C	-	-	C	-
773560	-	-	-	C	-	-	-	C
773570	-	-	-	C	-	-	-	-
773600	-	-	-	-	C	C	C	C
773610	-	-	-	-	C	C	C	-
773620	-	-	-	-	C	C	-	C
773630	-	-	-	-	C	C	-	-
773640	-	-	-	-	C	-	C	C
773650	-	-	-	-	C	-	C	-
773660	-	-	-	-	C	-	-	C
773670	-	-	-	-	C	-	-	-
773700	-	-	-	-	-	C	C	C
773710	-	-	-	-	-	C	C	-
773720	-	-	-	-	-	C	-	C
773730	-	-	-	-	-	C	-	-
773740	-	-	-	-	-	-	C	C
773750	-	-	-	-	-	-	C	-
773760	-	-	-	-	-	-	-	C
773770	-	-	-	-	-	-	-	-

Table A-1: DM Address Switch Settings (SW4) (Con't.)

DH Address	Switch 8	7	6	5	4	3	2	1	DH Address	Switch 8	7	6	5	4	3	2	1
760020	C	C	C	C	C	C	-	-	761020	C	-	C	C	C	C	-	-
760040	C	C	C	C	C	-	C	-	761040	C	-	C	C	C	-	C	-
760060	C	C	C	C	C	-	-	-	761060	C	-	C	C	C	-	-	-
760100	C	C	C	C	-	C	C	-	761100	C	-	C	C	-	C	C	-
760120	C	C	C	C	-	C	-	-	761120	C	-	C	C	-	C	-	-
760140	C	C	C	C	-	-	C	-	761140	C	-	C	C	-	-	C	-
760160	C	C	C	C	-	-	-	-	761160	C	-	C	C	-	-	-	-
760200	C	C	C	-	C	C	C	-	761200	C	-	C	-	C	C	C	-
760220	C	C	C	-	C	C	-	-	761220	C	-	C	-	C	C	-	-
760240	C	C	C	-	C	-	C	-	761240	C	-	C	-	C	-	C	-
760260	C	C	C	-	C	-	-	-	761260	C	-	C	-	C	-	-	-
760300	C	C	C	-	-	C	C	-	761300	C	-	C	-	-	C	C	-
760320	C	C	C	-	-	C	-	-	761320	C	-	C	-	-	C	-	-
760340	C	C	C	-	-	-	C	-	761340	C	-	C	-	-	-	C	-
760360	C	C	C	-	-	-	-	-	761360	C	-	C	-	-	-	-	-
760400	C	C	-	C	C	C	C	-	761400	C	-	-	C	C	C	C	-
760420	C	C	-	C	C	C	-	-	761420	C	-	-	C	C	C	-	-
760440	C	C	-	C	C	-	C	-	761440	C	-	-	C	C	-	C	-
760460	C	C	-	C	C	-	-	-	761460	C	-	-	C	C	-	-	-
760500	C	C	-	C	-	C	C	-	761500	C	-	-	C	-	C	C	-
760520	C	C	-	C	-	C	-	-	761520	C	-	-	C	-	C	-	-
760540	C	C	-	C	-	-	C	-	761540	C	-	-	C	-	-	C	-
760560	C	C	-	C	-	-	-	-	761560	C	-	-	C	-	-	-	-
760600	C	C	-	-	C	C	C	-	761600	C	-	-	-	C	C	C	-
760620	C	C	-	-	C	C	-	-	761620	C	-	-	-	C	C	-	-
760640	C	C	-	-	C	-	C	-	761640	C	-	-	-	C	-	C	-
760660	C	C	-	-	C	-	-	-	761660	C	-	-	-	C	-	-	-
760700	C	C	-	-	-	C	C	-	761700	C	-	-	-	-	C	C	-
760720	C	C	-	-	-	C	-	-	761720	C	-	-	-	-	C	-	-
760740	C	C	-	-	-	-	C	-	761740	C	-	-	-	-	-	C	-
760760	C	C	-	-	-	-	-	-	761760	C	-	-	-	-	-	-	-
761000	C	-	C	C	C	C	C	-	762000	-	C	C	C	C	C	C	-

Table A-2: DH Address Switch Settings (SW5)

DH Address	Switch 8	7	6	5	4	3	2	1	DH Address	Switch 8	7	6	5	4	3	2	1
762020	-	C	C	C	C	C	-	-	763020	-	-	C	C	C	C	-	-
762040	-	C	C	C	C	-	C	-	763040	-	-	C	C	C	-	C	-
762060	-	C	C	C	C	-	-	-	763060	-	-	C	C	C	-	-	-
762100	-	C	C	C	-	C	C	-	763100	-	-	C	C	-	C	C	-
762120	-	C	C	C	-	C	-	-	763120	-	-	C	C	-	C	-	-
762140	-	C	C	C	-	-	C	-	763140	-	-	C	C	-	-	C	-
762160	-	C	C	C	-	-	-	-	763160	-	-	C	C	-	-	-	-
762200	-	C	C	-	C	C	C	-	763200	-	-	C	-	C	C	C	-
762220	-	C	C	-	C	C	-	-	763220	-	-	C	-	C	C	-	-
762240	-	C	C	-	C	-	C	-	763240	-	-	C	-	C	-	C	-
762260	-	C	C	-	C	-	-	-	763260	-	-	C	-	C	-	-	-
762300	-	C	C	-	-	C	C	-	763300	-	-	C	-	-	C	C	-
762320	-	C	C	-	-	C	-	-	763320	-	-	C	-	-	C	-	-
762340	-	C	C	-	-	-	C	-	763340	-	-	C	-	-	-	C	-
762360	-	C	C	-	-	-	-	-	763360	-	-	C	-	-	-	-	-
762400	-	C	-	C	C	C	C	-	763400	-	-	-	C	C	C	C	-
762420	-	C	-	C	C	C	-	-	763420	-	-	-	C	C	C	-	-
762440	-	C	-	C	C	-	C	-	763440	-	-	-	C	C	-	C	-
762460	-	C	-	C	C	-	-	-	763460	-	-	-	C	C	-	-	-
762500	-	C	-	C	-	C	C	-	763500	-	-	-	C	-	C	C	-
762520	-	C	-	C	-	C	-	-	763520	-	-	-	C	-	C	-	-
762540	-	C	-	C	-	-	C	-	763540	-	-	-	C	-	-	C	-
762560	-	C	-	C	-	-	-	-	763560	-	-	-	C	-	-	-	-
762600	-	C	-	-	C	C	C	-	763600	-	-	-	-	C	C	C	-
762620	-	C	-	-	C	C	-	-	763620	-	-	-	-	C	C	-	-
762640	-	C	-	-	C	-	C	-	763640	-	-	-	-	C	-	C	-
762660	-	C	-	-	C	-	-	-	763660	-	-	-	-	C	-	-	-
762700	-	C	-	-	-	C	C	-	763700	-	-	-	-	-	C	C	-
762720	-	C	-	-	-	C	-	-	763720	-	-	-	-	-	C	-	-
762740	-	C	-	-	-	-	C	-	763740	-	-	-	-	-	-	C	-
762760	-	C	-	-	-	-	-	-	763760	-	-	-	-	-	-	-	-
763000	-	-	C	C	C	C	C	-									

Table A-2: DH Address Switch Settings (SW5) (con't.)

APPENDIX B

Vector Switch Settings

This appendix contains the vector switch settings for the DH and DM (modem) vectors.

DM Vector	Switch 8	7	6	5	4	3	2	1	DM Vector	Switch 8	7	6	5	4	3	2	1
Disabled	-	-	-	-	-	-	X	-	200	C	-	-	-	-	-	X	-
004	-	-	-	-	-	C	X	-	204	C	-	-	-	-	C	X	-
010	-	-	-	-	C	-	X	-	210	C	-	-	-	C	-	X	-
014	-	-	-	-	C	C	X	-	214	C	-	-	-	C	C	X	-
020	-	-	-	C	-	-	X	-	220	C	-	-	C	-	-	X	-
024	-	-	-	C	-	C	X	-	224	C	-	-	C	-	C	X	-
030	-	-	-	C	C	-	X	-	230	C	-	-	C	C	-	X	-
034	-	-	-	C	C	C	X	-	234	C	-	-	C	C	C	X	-
040	-	-	C	-	-	-	X	-	240	C	-	C	-	-	-	X	-
044	-	-	C	-	-	C	X	-	244	C	-	C	-	-	C	X	-
050	-	-	C	-	C	-	X	-	250	C	-	C	-	C	-	X	-
054	-	-	C	-	C	C	X	-	254	C	-	C	-	C	C	X	-
060	-	-	C	C	-	-	X	-	260	C	-	C	C	-	-	X	-
064	-	-	C	C	-	C	X	-	264	C	-	C	C	-	C	X	-
070	-	-	C	C	C	-	X	-	270	C	-	C	C	C	-	X	-
074	-	-	C	C	C	C	X	-	274	C	-	C	C	C	C	X	-
100	-	C	-	-	-	-	X	-	300	C	C	-	-	-	-	X	-
104	-	C	-	-	-	C	X	-	304	C	C	-	-	-	C	X	-
110	-	C	-	-	C	-	X	-	310	C	C	-	-	C	-	X	-
114	-	C	-	-	C	C	X	-	314	C	C	-	-	C	C	X	-
120	-	C	-	C	-	-	X	-	320	C	C	-	C	-	-	X	-
124	-	C	-	C	-	C	X	-	324	C	C	-	C	-	C	X	-
130	-	C	-	C	C	-	X	-	330	C	C	-	C	C	-	X	-
134	-	C	-	C	C	C	X	-	334	C	C	-	C	C	C	X	-
140	-	C	C	-	-	-	X	-	340	C	C	C	-	-	-	X	-
144	-	C	C	-	-	C	X	-	344	C	C	C	-	-	C	X	-
150	-	C	C	-	C	-	X	-	350	C	C	C	-	C	-	X	-
154	-	C	C	-	C	C	X	-	354	C	C	C	-	C	C	X	-
160	-	C	C	C	-	-	X	-	360	C	C	C	C	-	-	X	-
164	-	C	C	C	-	C	X	-	364	C	C	C	C	-	C	X	-
170	-	C	C	C	C	-	X	-	370	C	C	C	C	C	-	X	-
174	-	C	C	C	C	C	X	-	374	C	C	C	C	C	C	X	-

Table B-1: DM Address Vector Switch Settings (SW2)

DM Vector	Switch 8	7	6	5	4	3	2	1	DM Vector	Switch 8	7	6	5	4	3	2	1
400	-	-	-	-	-	-	X	C	600	C	-	-	-	-	-	X	C
404	-	-	-	-	-	C	X	C	604	C	-	-	-	-	C	X	C
410	-	-	-	-	C	-	X	C	610	C	-	-	-	C	-	X	C
414	-	-	-	-	C	C	X	C	614	C	-	-	-	C	C	X	C
420	-	-	-	C	-	-	X	C	620	C	-	-	C	-	-	X	C
424	-	-	-	C	-	C	X	C	624	C	-	-	C	-	C	X	C
430	-	-	-	C	C	-	X	C	630	C	-	-	C	C	-	X	C
434	-	-	-	C	C	C	X	C	634	C	-	-	C	C	C	X	C
440	-	-	C	-	-	-	X	C	640	C	-	C	-	-	-	X	C
444	-	-	C	-	-	C	X	C	644	C	-	C	-	-	C	X	C
450	-	-	C	-	C	-	X	C	650	C	-	C	-	C	-	X	C
454	-	-	C	-	C	C	X	C	654	C	-	C	-	C	C	X	C
460	-	-	C	C	-	-	X	C	660	C	-	C	C	-	-	X	C
464	-	-	C	C	-	C	X	C	664	C	-	C	C	-	C	X	C
470	-	-	C	C	C	-	X	C	670	C	-	C	C	C	-	X	C
474	-	-	C	C	C	C	X	C	674	C	-	C	C	C	C	X	C
500	-	C	-	-	-	-	X	C	700	C	C	-	-	-	-	X	C
504	-	C	-	-	-	C	X	C	704	C	C	-	-	-	C	X	C
510	-	C	-	-	C	-	X	C	710	C	C	-	-	C	-	X	C
514	-	C	-	-	C	C	X	C	714	C	C	-	-	C	C	X	C
520	-	C	-	C	-	-	X	C	720	C	C	-	C	-	-	X	C
524	-	C	-	C	-	C	X	C	724	C	C	-	C	-	C	X	C
530	-	C	-	C	C	-	X	C	730	C	C	-	C	C	-	X	C
534	-	C	-	C	C	C	X	C	734	C	C	-	C	C	C	X	C
540	-	C	C	-	-	-	X	C	740	C	C	C	-	-	-	X	C
544	-	C	C	-	-	C	X	C	744	C	C	C	-	-	C	X	C
550	-	C	C	-	C	-	X	C	750	C	C	C	-	C	-	X	C
554	-	C	C	-	C	C	X	C	754	C	C	C	-	C	C	X	C
560	-	C	C	C	-	-	X	C	760	C	C	C	C	-	-	X	C
564	-	C	C	C	-	C	X	C	764	C	C	C	C	-	C	X	C
570	-	C	C	C	C	-	X	C	770	C	C	C	C	C	-	X	C
574	-	C	C	C	C	C	X	C	774	C	C	C	C	C	C	X	C

Table B-1: DM Address Vector Switch Settings (SW2) (con't.)

DH Vector	Switch 8 7 6 5 4 3 2 1	DH Vector	Switch 8 7 6 5 4 3 2 1
000	- - - - - - X X -	400	- - - - - - X X C
010	- - - - - C X X -	410	- - - - - C X X C
020	- - - - C - X X -	420	- - - - C - X X C
030	- - - - C C X X -	430	- - - - C C X X C
040	- - - C - - X X -	440	- - - C - - X X C
050	- - - C - C X X -	450	- - - C - C X X C
060	- - - C C - X X -	460	- - - C C - X X C
070	- - - C C C X X -	470	- - - C C C X X C
100	- - C - - - X X -	500	- - C - - - X X C
110	- - C - - C X X -	510	- - C - - C X X C
120	- - C - - C - X X -	520	- - C - - C - X X C
130	- - C - - C C X X -	530	- - C - - C C X X C
140	- - C C - - X X -	540	- - C C - - X X C
150	- - C C - - C X X -	550	- - C C - - C X X C
160	- - C C C - X X -	560	- - C C C - X X C
170	- - C C C C X X -	570	- - C C C C X X C
200	- C - - - - X X -	600	- C - - - - X X C
210	- C - - - C X X -	610	- C - - - C X X C
220	- C - - C - X X -	620	- C - - C - X X C
230	- C - - C C X X -	630	- C - - C C X X C
240	- C - C - - X X -	640	- C - C - - X X C
250	- C - C - C X X -	650	- C - C - C X X C
260	- C - C C - X X -	660	- C - C C - X X C
270	- C - C C C X X -	670	- C - C C C X X C
300	- C C - - - X X -	700	- C C - - - X X C
310	- C C - - C X X -	710	- C C - - C X X C
320	- C C - C - X X -	720	- C C - C - X X C
330	- C C - C C X X -	730	- C C - C C X X C
340	- C C C - - X X -	740	- C C C - - X X C
350	- C C C - C X X -	750	- C C C - C X X C
360	- C C C C - X X -	760	- C C C C - X X C
370	- C C C C C X X -	770	- C C C C C X X C

Table B-2: DH Vector Address Switch Settings (SW1)

APPENDIX C

Priority Strapping

This appendix contains priority interrupt levels on the Q/DH. The Q/DH is able to interrupt on level 4 and level 5. Selection of interrupt priority is made by strapping "E" points together (or removing straps). The "E" points associated with the DH portion of the Q/DH are E19 and E20. The modem control "E" points are E25 and E26. In each case, the "E" points are strapped together to select priority level 4, and are disconnected to select priority level 5.

DH = 4 MODEM = 4	DH = 4 MODEM = 5
E19 ----- E20	E19 ----- E20
E26 ----- E25	E26 E25

DH = 5 MODEM = 4	DH = 5 MODEM = 5
E19 E20	E19 E20
E26 ----- E25	E26 E25

Table C-1: Interrupt Level Strapping

APPENDIX D

Voltage Sources on the Backplane

This appendix provides the voltage sources on the Backplane.

VOLTAGE	BACKPLANE PINS
+5	AA2, BA2, BV1, CA2, DA2, DV1, EA2, FA2
+12	AD2, BD2, CD2, DD2
Ground	AC2, BC2, CC2, DC2, EC2, FC2, AT1, BT1, CT1, DT1, ET1, FT1

Table E-1: Voltage Sources on Backplane

APPENDIX E

Spare Parts List

This appendix provides a recommended spare parts list for Q/DH, including vendors and part numbers.

Description	Vendor Part No.	ABLE Part No.	Reference Designation	Vendor*
IC Quad 2-In NAND	SN74S00N	349-174-000	U58	TI
IC Quad 2-IN NAND	SN74LS00N	349-274-000	U65	TI
IC Hex Inverter	SN74S04N	349-174-004	U19,U43,U89	TI
IC Hex Inverter	SN 74LS04N/J	349-274-004	U95	TI
IC Quad 2-In And	SN74S08N	349-174-008	U82,U107	TI
IC Triple 3-In NAND	SN74S10N	349-174-010	U88,U101	TI
IC Triple 3-In AND	SN74S11N	349-174-011	U76	TI
IC Quad 2-In Or	SN74S32N/J	349-174-032	U35	TI
IC Dual D Flip-Flop	SN74S74N	349-174-074	U52,U70	TI
IC 3 to 8 Decoder	SN74S138N	349-174-138	U28,U99,U104	TI
IC 3 to 8 Decoder/Mux	SN74LS138N	349-274-138	U32	TI
IC Dual 2 to 4 Decoder	SN74S139N	349-174-139	U64	TI
IC 8 to 3 Priority Enc.	SN74148N	349-074-148	U105	TI
IC 8 to 1 Mux	SN74S151N	349-174-151	U94	TI
IC 8 to 1 Mux	SN74LS151N	349-274-151	U56	TI
IC Quad 2 to 1 Mux	SN74S157N	349-174-157	U87	TI
IC Quad 2 to 1 Mux	SN74LS157N	349-274-157	U57,U63	TI
IC Octal D Flip-Flop	SN74LS273	349-274-273	U106	TI
IC 8 Bit Addressable Latch	SN74LS259	349-274-259	U91,U96	TI
IC 8 Bit Latch 3-St	SN74LS373N	349-274-373	U38	TI
IC Octal D Flip-Flop	SN74LS374N	349-274-374	U33,U39,U74	TI
IC Octal D Flip-Flop w/ENABLE	SN74LS377N	349-274-377	U36,U37,U41 U46,U61,U92, U98,U100	TI
IC Microprocessor	AM2901BPC	349-229-001	U42,U51	AMD
IC Microprogram Seq.	AM2911	349-229-011	U68,U80,U86	AMD
IC Prog. Comm Inter. USART	2661-3N	349-402-661	U3,U4,U5,U6 U15,U16,U17, U18	Signetics
IC 8 Bit Equal to Comparator	AM25LS2521PC	349-252-521	U44,U59	AMD
IC Interface Quad Bus Trans. O.C.	DS8641N	345-008-641	U90,U97,U103	NSC
IC Interface Quad Bus Trans w/Logic O.C.	AM2908PC	345-029-008	U49,U54,U66, U72,U78,U84, U109	AMD
IC Interface Quad Drvr	MC1488P	345-001-488	U2,U10,U14, U23	Motorola
IC Interface Quad Rcvr	MC1489P	345-001-489	U1,U9,U11, U12,U13,U22	Motorola
IC Intrfce Oct. Invtr/	SN74LS240N		U25,U26,U27,	TI

Drvr 3-State		345-274-240	U34	
IC Intrfce Oct Buff/	SN74LS244N		U62	TI
Drvr 3-State		345-274-244		
IC Intrfce Oct. Buff/	SN74LS245N		U45,U60	TI
Drvr/Rcvr 3-State		345-274-245		
IC Intrfce MOS Clk Drvr	MH0026C	345-000-026	U7,U8	NSC
IC Dual Baud Rate Gen.	COM8116P	349-408-116	U24	SMC
IC RAM 16x4 O.C.	SN74S189N	347-174-189	U75,U81	TI
IC RAM 1Kx4 3-St 70 NS	2148	347-421-480	U29,U30	Intel
Diode Switching 1N4606	FDH600	341-200-600	CR2-CR7	Fairchil
Diode Zener 9.1V 1W	1N4739A	341-309-100	CR1,CR8	Motorola

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* Vendor: TI = Texas Instruments; AMD = Advanced Micro Devices
NSC = National Semiconductor; SMC = Standard Micro Systems Cor

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APPENDIX F

List of Materials

This appendix contains a list of materials for the Q/DH including vendors and part numbers.

Description	Vendor Part No.	ABLE Part No.	Qty.	Ref. Desig.	Vendor
IC Quad 2-In NAND	SN74S00N	349-174-000	1	U58	TI
IC Quad 2-IN NAND	SN74LS00N	349-274-000	1	U65	TI
IC Hex Inverter	SN74S04N	349-174-004	3	U19,U43,U89	TI
IC Hex Inverter	SN74LS04N/J	349-274-004	1	U95	TI
IC Quad 2-In And	SN74S08N	349-174-008	2	U82,U107	TI
IC Triple 3-In NAND	SN74S10N	349-174-010	2	U88,U101	TI
IC Triple 3-In AND	SN74S11N	349-174-011	1	U76	TI
IC Quad 2-In Or	SN74S32N/J	349-174-032	1	U35	TI
IC Dual D Flip Flop	SN74S74N	349-174-074	2	U52,U70	TI
IC 3 to 8 Decoder	SN74S138N	349-174-138	3	U28,U99,U104	TI
IC 3 to 8 Decoder/Mux	SN74LS138N	349-274-138	1	U32	TI
IC Dual 2 to 4 Decoder	SN74S139N	349-174-139	1	U64	TI
IC 8 to 3 Priority Enc.	SN74148N	349-074-148	1	U105	TI
IC 8 to 1 Mux	SN74S151N	349-174-151	1	U94	TI
IC 8 to 1 Mux	SN74LS151N	349-274-151	1	U56	TI
IC Quad 2 to 1 Mux	SN74S157N	349-174-157	1	U87	TI
IC Quad 2 to 1 Mux	SN74LS157N	349-274-157	2	U57,U63	TI
IC Octal D Flip-Flop	SN74LS273	349-274-273	1	U106	TI
IC 8 Bit Addressable Latch	SN74LS259	349-274-259	2	U91,U96	TI
IC 8 Bit Latch 3-St	SN74LS373N	349-274-373	1	U38	TI
IC Octal D Flip-Flop	SN74LS374N	349-274-374	3	U33,U39,U74	TI
IC Octal D Flip-Flop w/ENABLE	SN74LS377N	349-274-377	8	U36,U37,U41, U46,U61,U92, U98,U100	TI
IC Microprocessor	AM2901BPC	349-229-001	2	U42,U51	AMD
IC Microprogram Seq.	AM2911	349-229-011	3	U68,U80,U86	AMD
IC Prog. Comm Inter. USART	2661-3N	349-402-661	8	U3,U4,U5,U6 U15,U16,U17, U18	Signetic
IC 8 Bit Equal to Comparator	AM25LS2521PC	349-252-521	2	U44,U59	AMD
IC Interface Quad Bus Trans. O.C.	DS8641N	345-008-641	3	U90,U97,U103	NSC
IC Interface Quad Bus Trans w/Logic O.C.	AM2908PC	345-029-008	7	U49,U54,U66, U72,U78,U84, U109	AMD
IC Interface Quad Drvr	MC1488P	345-001-488	4	U2,U10,U14, U23	Motorola
IC Interface Quad Rcvr	MC1489P	345-001-489	6	U1,U9,U11, U12,U13,U22	Motorola
IC Intrfce Oct. Invtr/ Drvr 3-State	SN74LS240N	345-274-240	4	U25,U26,U27, U34	TI
IC Intrfce Oct Buff/ Drvr 3-State	SN74LS244N	345-274-244	1	U62	TI
IC Intrfce Oct. Buff/ Drvr/Rcvr 3-State	SN74LS245N	345-274-245	2	U45,U60	TI

IC Intrfce MOS Clk Drvr	MH0026C	345-000-026	2	U7,U8	NSC
IC Dual Baud Rate Gen.	COM8116P	349-408-116	1	U24	SMC
IC RAM 16x4 O.C.	SN74S189N	347-174-189	2	U75,U81	TI
IC RAM 1Kx4 3-St 70 NS	2148	347-421-480	2	U29,U30	Intel
Res. 5% 1/4W 1K Ohms	CB1025	310-012-102	3	R3,R4,R6	AB
Res. 5% 1/4W 220 Ohms	CB2215	310-012-221	1	R5	AB
Res. 2% 1/2W 47 Ohms	RL20S470G	310-022-420	2	R1,R2	IRC
Diode Switching 1N4606	FDH600	341-200-600	6	CR2-CR7	Fairch:
Diode Zener 9.1V 1W	1N4739A	341-309-100	2	CR1,CR8	Motoro:
Res. Mod 8 Pin SIP 5% 470 Ohms	MSP08A01-471J	311-471-002	2	RM6,RM13	Dale
Res. Mod 10 Pin SIP 2% 8.2K Ohms	MSP10A011822G	311-822-000	6	RM9,RM10, RM11,RM12, RM14	Dale
Res. Mod 8 Pin SIP 5% 33K Ohms	MSP08A01-333J	311-333-002	4	RM2,RM3, RM4,RM8	Dale
Res. Mod 8 Pin SIP 5% 4.7K Ohms	MSP08A01-472J	311-472-002	3	RM1,RM5,RM7	Dale
Res. Mod 8 Pin SIP 2% 330/680	MSP08A5-331/681G	312-221-003	1	RM15	Dale
Cap. Cer. SIP-8 10% 470Pf 100V	460CH471X9PD	321-637-417	1	CM1	Sprague
Cap. Mica 5% HV 200Pf	CD15FD201J03	320-029-201	1	C40	CDE
Cap. Mica 5% HV 470Pf	CD15FD471J03	320-029-471	1	C9	CDE
Cap. Cer. 10% 50V .01UF Axial (.160)	DK12BX103K	322-226-103	31	C10-C14,C17, C20-C25,C27-C36,C38,C39, C41-C47	Corning
Cap. Tantalum 20% 20V 4.7 Mfd. Submin-Axial	T322B475M020AS	322-244-475	11	C2-C4,C6-C8, C15,C18,C26, C37,C48	Kemet
Optics LED, Red, Quad	555-4003	331-204-001	1	CR9	Dialigh

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* Vendor: TI = Texas Instruments; AMD = Advanced Micro Devices
NSC = National Semiconductor; SMC = Standard Micro Systems Corp.
AB = Allen-Bradley; IRC = TRW/IRC; CDE = Cornell Dublier
