AD 10 SYSTEM ARCHITECTURE

CHAPTER 2

2. SYSTEM ARCHITECTURE

2.1 INTRODUCTION

The AD-10 is an extremely high speed peripheral processing system designed to relieve its host processor of a significant portion of its mathematical computations. This results in a corresponding reduction in computer time required to solve large complex problems, particularly those requiring multivariant function generation.

The AD-10 operates under the overall control of the host processor. The host processor is normally one of the Digital Equipment Corporation PDP-11 family of general purpose processors, as ADI has developed an extensive software system for the PDP-11/AD-10 combination. Interconnection of the PDP-11 to another digital processor is a relatively straightforward task and is more cost effective then adapting the entire software system. The PDP-11/AD-10 software is described separately, but includes the capability to prepare, load, debug, and modify the AD-10 programs and data base as well as provide the necessary interaction during run time.

The AD-10, in addition to operating from its stored data base, is able to communicate with the host processor or other devices during run time. Devices other than the host processor are connected to the Input/Output Channel Controller (IOCC) which may contain both analog and digital interfaces.

2.2 SYSTEM ORGANIZATION

The AD-10 is a highly structured, bus oriented system comprised of a large data memory and a variety of specialized processors and controllers. These system modules are interconnected by the AD-10 MULTIBUS as illustrated in the block diagram of Figure 2.1. The internal operation is entirely synchronous, although the system is designed to operate with asynchronous external devices. Each processor contains its own program memory, eliminating the need for inter-processor instruction transfer. This distributed memory and processing concept substantially reduces the number of transactions which would otherwise have to take place on the MULTIBUS.

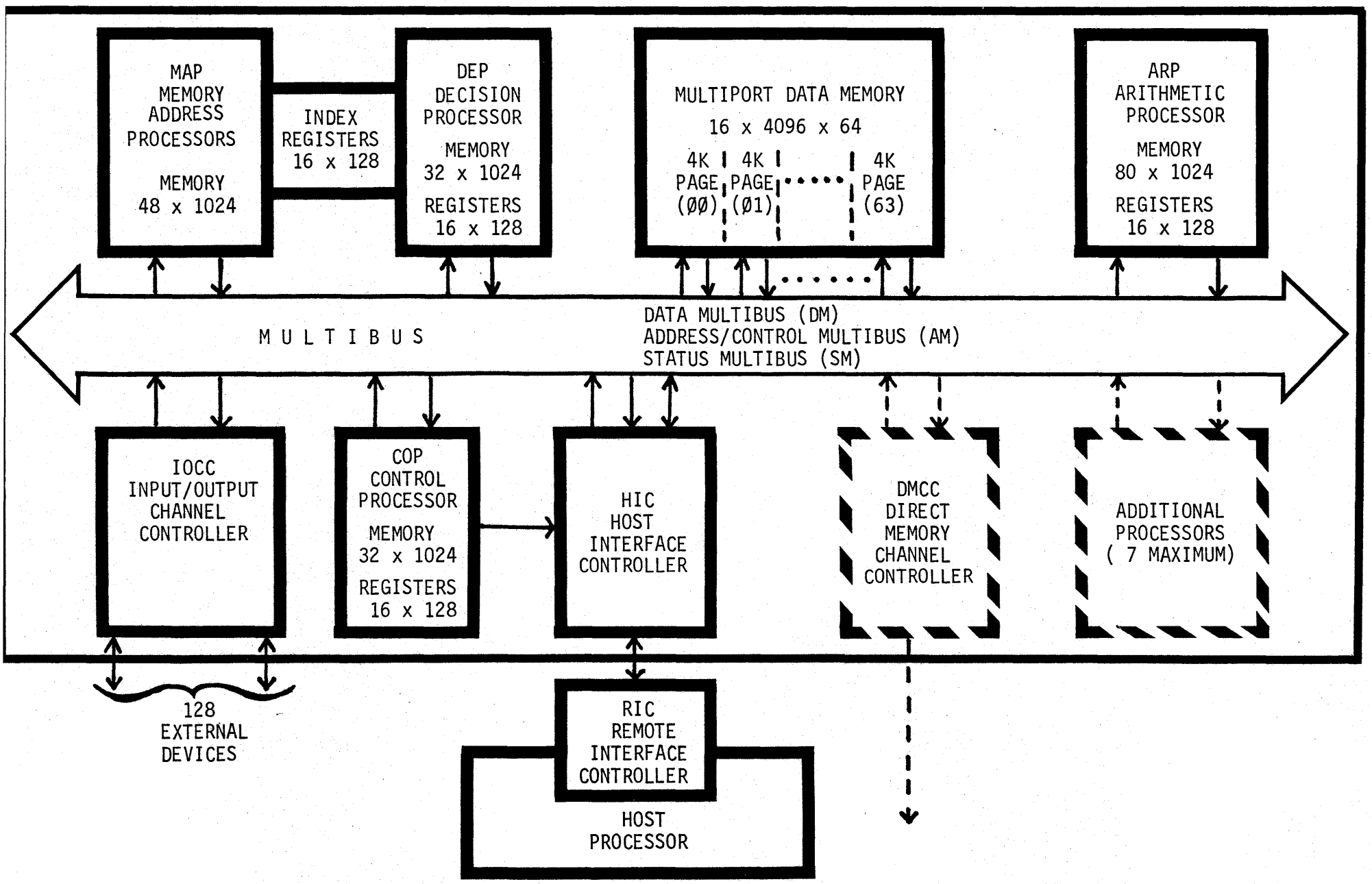


FIGURE 2.1 AD 10 BLOCK DIAGRAM

The following summary is provided to properly place each element of its AD-10 in perspective. Detailed descriptions are provided in subsequent sections of this or other chapters.

2.2.1 MULTIBUS

The AD-10 MULTIBUS is a high speed, synchronous communication bus that distributes system power and timing and interconnects all system modules. The MULTIBUS operates at a 20 MHz data rate and is provided with hardware for data parity generation and checking, bus contention detection, and memory refresh circuitry.

2.2.2 DATA MEMORY

The AD-10 Data Memory is an interleaved, multiport MOS memory that is expandable to 256K 16-bit words. Each 4K word page has a cycle time of 500 ns but is independently connected to the MULTIBUS. This structure permits the interleaving of data transfers with a resultant data transfer rate of 20 MHz.

2.2.3 HIC/RIC HOST INTERFACE CONTROLLER/REMOTE INTERFACE CONTROLLER

The HIC/RIC combination interfaces the AD-10 to the host processor. The RIC interfaces to the appropriate port of the host processor, which is directly to the Unibus® in the case of the PDP-11. The HIC contains all of the registers and features to allow the host processor to efficiently operate the AD-10 during run time as well as providing access to the innermost operations of the AD-10 for program debugging and maintenance.

2.2.4 COP - CONTROL PROCESSOR

The COP provides a programmed source of control of the total AD-10 system during run time. The COP controls the ACTIVE/WAIT state and program counter of each processor, and is equipped with 128 general registers plus decision making and branching capability. The COP also directly operates the IOCC.

2.2.5 ARP - ARITHMETIC PROCESSOR

The ARP performs the actual mathematical operations required of the AD-10. The ARP operations may involve integers, scaled fractions, or a combination of these and is capable of 30 million arithmetic operations (adds and multiplies) per second.

2.2.6 DEP - DECISION PROCESSOR

The DEP is a logical binary processor that is equipped with an internal storage file and the ability to compare a word from this file to a word from the MULTIBUS. The DEP can also modify the contents of the Index Registers used by the MAP for indirect addressing. This allows the DEP, through a logical decision process, to cause the MAP to address the desired locations in DATA MEMORY.

2.2.7 MAP - MEMORY ADDRESS PROCESSOR

The MAP generates the physical addresses required to access any location in Data Memory. The address stated in a MAP instruction may be modified by the contents of an Index Register that has been set by the DEP. An alignment network is also provided to facilitate accessing pairs of values at maximum speed.

2.2.8 IOCC - INPUT/OUTPUT CHANNEL CONTROLLER

The optional IOCC provides a 10MHz word transfer rate interface between the AD-10 and equipment other than the host processor. The IOCC provides addressing, control, and data paths for up to 128 devices. These devices may include any combination of A/D and D/A converters and logic buffers, allowing interface of the AD-10 to analog or digital devices. Devices may be logically grouped under program control for simultaneous command control.

2.2.9 DMCC - DIRECT MEMORY CHANNEL CONTROLLER

The DMCC design has not been finalized at this time. The purpose, however, is to provide a connection between the AD-10 and a direct memory access type channel of a large digital system. The design will accomodate a variety of word formats and channel characteristics.

2.2.10 ADDITIONAL PROCESSORS

The AD-10 is prewired to accept additional system modules including processors. The specific function and characteristics of these modules will be defined as they are developed.

2.3 MULTIBUS DESCRIPTION

2.3.1 INTRODUCTION

The AD-10 MULTIBUS is an extremely high speed, synchronous communication bus that interconnects the AD-10 system modules. The bus is designed to operate at 20 million transactions per second (20 MHz word rate) in a completely synchronous manner. Up to 29 system modules may be physically attached to this bus and thereby interconnected with each other. Information may be placed on the MULTIBUS by any one system module (source device), and this information is then available to all system modules (destination device(s)). Whether a particular device is a source or a destination for information is determined by the current instruction word or hardware logic in each device, and no handshake is involved. Therefore, the source and destination device(s) must be independently commanded to perform their tasks during the appropriate bus cycle.

The MULTIBUS is actually comprised of three buses; the DATA MULTIBUS (DM), the ADDRESS/CONTROL MULTIBUS (AM), and the STATUS MULTIBUS. This is illustrated in Figure 2.2. In addition, power and timing signals are distributed to all systems modules via the MULTIBUS.

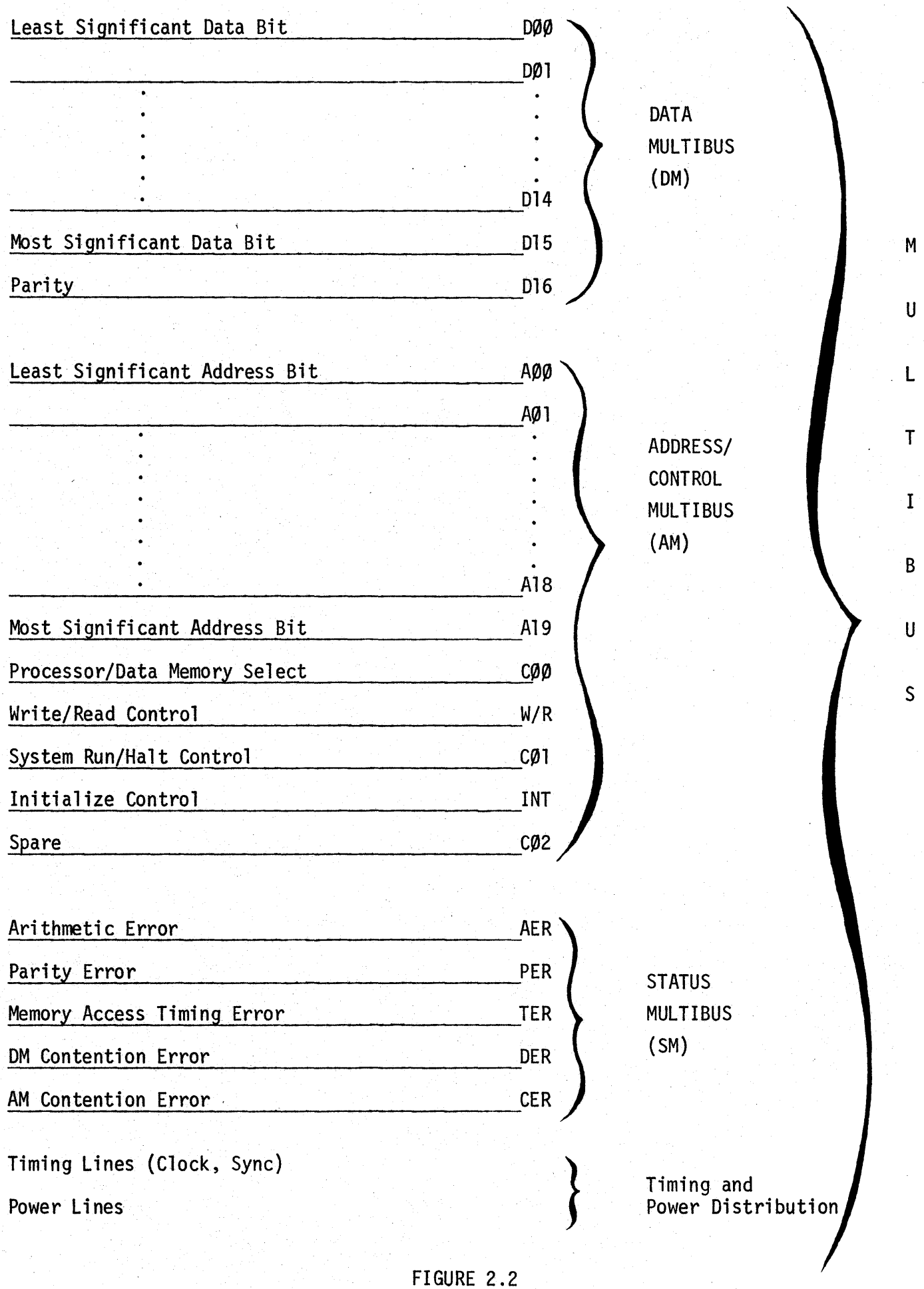

Least Significant Data Bit
D00
D01
D14
Most Significant Data Bit
D15
Parity
D16
DATA MULTIBUS (DM)
Least Significant Address Bit
A00
A01
A18
Most Significant Address Bit
A19
Processor/Data Memory Select
C00
Write/Read Control
W/R
System Run/Halt Control
C01
Initialize Control
INT
Spare
C02
ADDRESS/ CONTROL MULTIBUS (AM)
Arithmetic Error
AER
Parity Error
PER
Memory Access Timing Error
TER
DM Contention Error
DER
AM Contention Error
CER
STATUS MULTIBUS (SM)
Timing Lines (Clock, Sync)
Power Lines
Timing and Power Distribution
MULTIBUS

FIGURE 2.2

2.3.2 DATA MULTIBUS (DM)

The DATA MULTIBUS consists of sixteen data lines plus a parity line. Odd parity is generated on all DM transactions, but it is checked only during transfers out of Data Memory.

2.3.3 ADDRESS/CONTROL MULTIBUS (AM)

The AM consists of twenty-five (25) lines. Five of these are control lines and the remaining twenty (AØØ-A19) are normally address lines, but may also serve as data or control lines in special cases as explained below.

2.3.3.1 SYSTEM CONTROL LINES:
Initialize (INT)

The INT line, when set to a "1", causes the AD-10 system to be initialized. This line can be asserted only by the host processor through the HIC. Initialization operations performed include placing the AD-10 in Halt, placing all processors in the Wait state, resetting to zero all processor program counters and pause counters, and clearing specific registers in the HIC. Certain bits in the processor status words are cleared only by reading them. These bits are not cleared by asserting the INT line.

Run/Halt Control Line - CØ1:

This line controls the Run/Halt state of all processors in the AD-10. When set to a "1", all processors are in the RUN state, although they may be individually or collectively placed in either the Active or Wait state by the Control Processor. The Run state can be initiated only by the host processor through the HIC. The Halt mode occurs whenever this line is a "Ø". The Halt state can be initiated by internally generated signals through mask registers in the HIC or by the host processor.

CONTROL LINE CØ2 - SPARE
Write Control Line (W/R):

This line, when set to a "1", specifies that information is to be written into the register or memory location specified by other bits of the AM. Normally, the information is furnished by the DM, but in special cases the data is also provided on the AM. Conversely, a "Ø" on this line specifies a read operation.

Processor/Data Memory Select - CØØ:

This bit, when a "1", specifies access to the Data Memory. Otherwise, the address is interpreted as other than Data Memory.

2.3.3.2 Address Bits

Figure 2.3 provides a table that summarizes the use of bits AØØ-A19 of the AM for all bit combinations. The following comments augment the listing.

In general, Write operations require that the information to be written into the specified memory location or register must appear simultaneously on the DM. Similarly, the data requested during a Read operation will generally appear on the DM. For "fast" devices, the data will appear during the same bus cycle time. These "fast" devices include processor program memory, processor status words, and other registers that may be accessed in 15 ns. Slow devices include Data Memory and the devices in the IOCC. The 450 ns delay between the read command and the appearance of the data on the DM is explained in the section on Data Memory.

Special cases where data also appears on the AM include: loading the processor program counters, setting the processor Active/Wait Status (COP instructions only), and writing instructions to the IOCC.

	W/R	C Ø Ø	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	A 1Ø	A Ø9	A Ø8	A Ø7	A Ø6	A Ø5	A Ø4	A Ø3	A Ø2	A Ø1	A ØØ
ADDRESS NOP	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	X	X	X	X	X	X	X	X	X	X	X	X
WRITE DATA MEMORY	1	1	MEMORY PAGE ADDRESS								MEMORY WORD ADDRESS HIGH ORDER | LOW ORDER											
READ DATA MEMORY	Ø	1	MEMORY PAGE ADDRESS								MEMORY WORD ADDRESS HIGH ORDER | LOW ORDER											
WRITE PROGRAM MEMORY	1	Ø	PROCESSOR NUMBER (1-15)				Ø	FIELD ADDRESS (Ø-5)					MEMORY WORD ADDRESS HIGH ORDER | LOW ORDER									
READ PROGRAM MEMORY	Ø	Ø	PROCESSOR NUMBER (1-15)				Ø	FIELD ADDRESS (Ø-5)					MEMORY WORD ADDRESS HIGH ORDER | LOW ORDER									
LOAD PROCESSOR PROGRAM COUNTER	1	Ø	PROCESSOR NUMBER (1-15)				Ø	1	1	Ø	WORD TO PROGRAM COUNTER (Ø to 1023)											
READ PROCESSOR PROGRAM COUNTER	Ø	Ø	PROCESSOR NUMBER (1-15)				Ø	1	1	Ø	PROGRAM COUNTER CONTENTS											
LOAD PROCESSOR STATUS ENABLE	1	Ø	PROCESSOR NUMBER (1-15)				Ø	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
											(CONTROL WORD FROM DM)											
READ PROCESSOR STATUS WORD	Ø	Ø	PROCESSOR NUMBER (1-15)				Ø	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
											(STATUS WORD TO DM)											
LOAD PROCESSOR ACTIVE/WAIT	1	Ø	Ø	Ø	Ø	Ø	Ø	1	#7 A	#7 W	#6 A	#6 W	#5 A	#5 W	#4 A	#4 W	#3 A	#3 W	#2 A	#2 W	#1 A	#1 W
LOAD I/O CONTROL	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	IMMEDIATE DATA											
READ I/O CONTROL	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	IMMEDIATE DATA											
LOAD OTHER DEVICES (4K)	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø	X	X	X	X	X	X	X	X	X	X	X	X
READ OTHER DEVICES (4K)	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø	X	X	X	X	X	X	X	X	X	X	X	X
LOAD OTHER DEVICES (4K)	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	1	X	X	X	X	X	X	X	X	X	X	X	X
READ OTHER DEVICES (4K)	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	1	X	X	X	X	X	X	X	X	X	X	X	X
REFRESH	Ø	Ø	X	X	X	X	1	1	MEMORY REFRESH ADDRESS													
UNASSIGNED	1	Ø	X	X	X	X	1	Ø	X	X	X	X	X	X	X	X	X	X	X	X	X	X
UNASSIGNED	Ø	Ø	X	X	X	X	1	Ø	X	X	X	X	X	X	X	X	X	X	X	X	X	X

FIGURE 2.3 AM BIT PATTERN SUMMARY

2.3.4 STATUS MULTIBUS (SM)

The SM is comprised of five (5) lines that are available to all system modules and terminate in the Error and Halt Status (EHS) register in the HIC. By use of the Halt Mask Resister (HMR) and Interrupt Mask Register (IMR) in the HIC, selective control is provided to allow any one of these lines to cause an AD-10 Halt and/or to interrupt the host processor. Actuation of one of these lines by a system module lasts only one bus cycle time, but the EHS register latches this data until it is read by the host processor.

Arithmetic Error (AER):

The basis for activation of the AER line is described in the respective chapter for each processor. In general, however, this line can be actuated by the ARP to indicate data overflow, by the MAP to indicate page overrange or underrange and by the DEP and COP to indicate a comparison result.

Parity Error (PER):

The parity error line is activated whenever a parity error is detected on the DM. Since parity is checked only on transfers from Data Memory, this is the only time the PER signal can be generated.

Memory Access Timing Error (TER):

A memory access timing error signal will result whenever access to a page of Data Memory is attempted and that page is busy due to a previous access instruction. This is illustrated in the Data Memory description in the next section. If this happens, the previous memory access instruction continues uninterrupted, and the memory access instruction that caused the TER signal is ignored.

DM Contention Error (DER):

The DER line is activated by hardware detection of more than one system module attempting to serve as a source to the DM during a given bus cycle.

AM Contention Error (CER):

The CER line is activated by hardware detection of more than one system module attempting to serve as a source to the AM during a given bus cycle.

2.3.5 BUS CHARACTERISTICS

Timing circuitry in each system module utilizes the clock (CKØ) and Synchronization (SYNC) signals distributed by the MULTIBUS to maintain the synchronous operation through out the system. Each module is synchronized to a 50 ns bus cycle time, allowing two complete bus transactions during each AD-10 instruction cycle. A module programmed or caused by hardwired logic to serve as a source to the DM and/or AM has the output of its bus load (L) register enabled onto the MULTIBUS for the entire 50 ns bus cycle time. This information is transmitted to and received by the bus store (S) registers in ALL system modules. The S registers are enabled to store the information after three fourths of the bus cycle time has elapsed, thereby allowing for time skew and bus propagation time. This also holds the data in the S register for the first three fourths of the next bus cycle time, allowing adequate time for this data to be moved from the S register for processing as required by the individual system module. Whether or not this data is used by a particular system module depends upon its current instruction or, in the case of hardwired logic, by the information present on the bus. In any case, new data will be written into the S register 50 ns later.

The instructions provided for the processors are structured to include (or hide) the MULTIBUS transactions. Many instructions contain the words First, Second, or Double. These words allow the programmer to precisely specify the time relationship of a complete transaction. Figure 2.4 illustrates the sequence for "First" instruction pair in the source and destination devices. The First in the source instruction will cause the data to be placed in the L register of the source processor during the first half of the instruction cycle. This information will appear on the MULTIBUS during the second half of the instruction cycle.

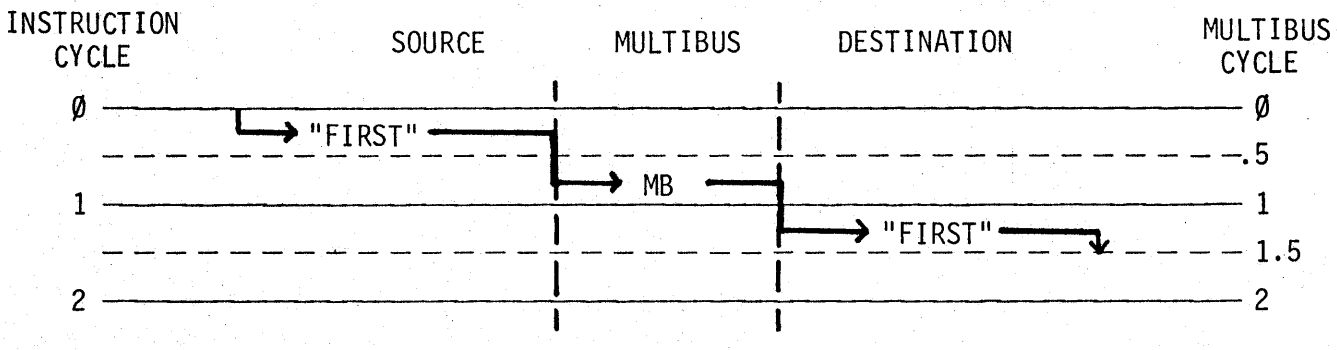


FIGURE 2.4 MULTIBUS TRANSACTION

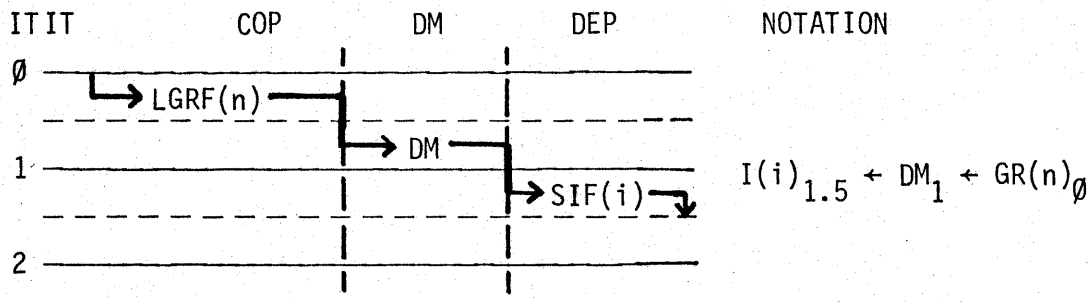


FIGURE 2.5a COP - DEP "FIRST" DATA TRANSFER

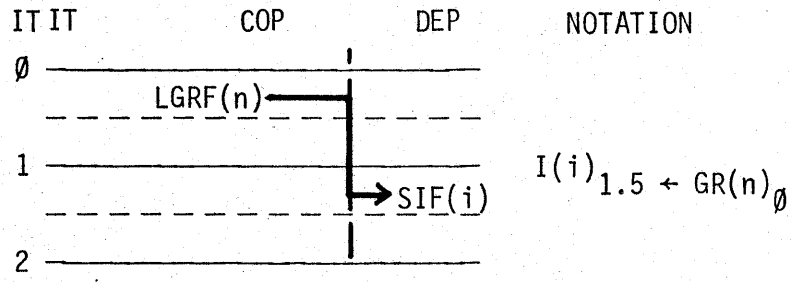


FIGURE 2.5b COP - DEP "FIRST" DATA TRANSFER

The data will then be available in the destination device's S register during the first half of the next instruction cycle. This requires a First in the destination device instruction to operate on this data before the information of the next bus cycle is written into the S register. Thus, a First in the source device's instruction requires a First (or equivalent) in the destination device(s) instruction one instruction cycle later. The same applied to a Second, and a Double is simply a microprogrammed combination of a First and Second.

A notation system has been developed to clearly express transactions. This notation utilizes subscripts that relate all transactions to instruction cycles. Where transactions to or from the MULTIBUS are expressed, the subscript used denotes the point at which the information is available in the S registers. Figure 2.5a illustrates a complete transaction where data stored in General Register n of the COP is transferred to Index Register i of the DEP. The notation, beginning at the right, states that the contents of General Register n at instruction cycle Ø are available from the DM at instruction time 1 and is stored in Index Register i by instruction time 1.5. Figure 2.5b illustrates that the same transfer can be shown with an implied MULTIBUS transaction.

2.4 DATA MEMORY

2.4.1 INTRODUCTION

The AD-10 Data Memory is an interleaved MOS memory expandable to 256K words. Each word consists of sixteen data bits plus a parity bit.

Functionally, the memory is divided into pages of 4096 words. Each page is a independent entity with its own timing and address decoding logic, bus storage (s) registers, and bus load (L) register. This architecture, illustrated in Figure 2.6, permits the interleaving of data transfers and resultant data rate of up to 20 MHz.

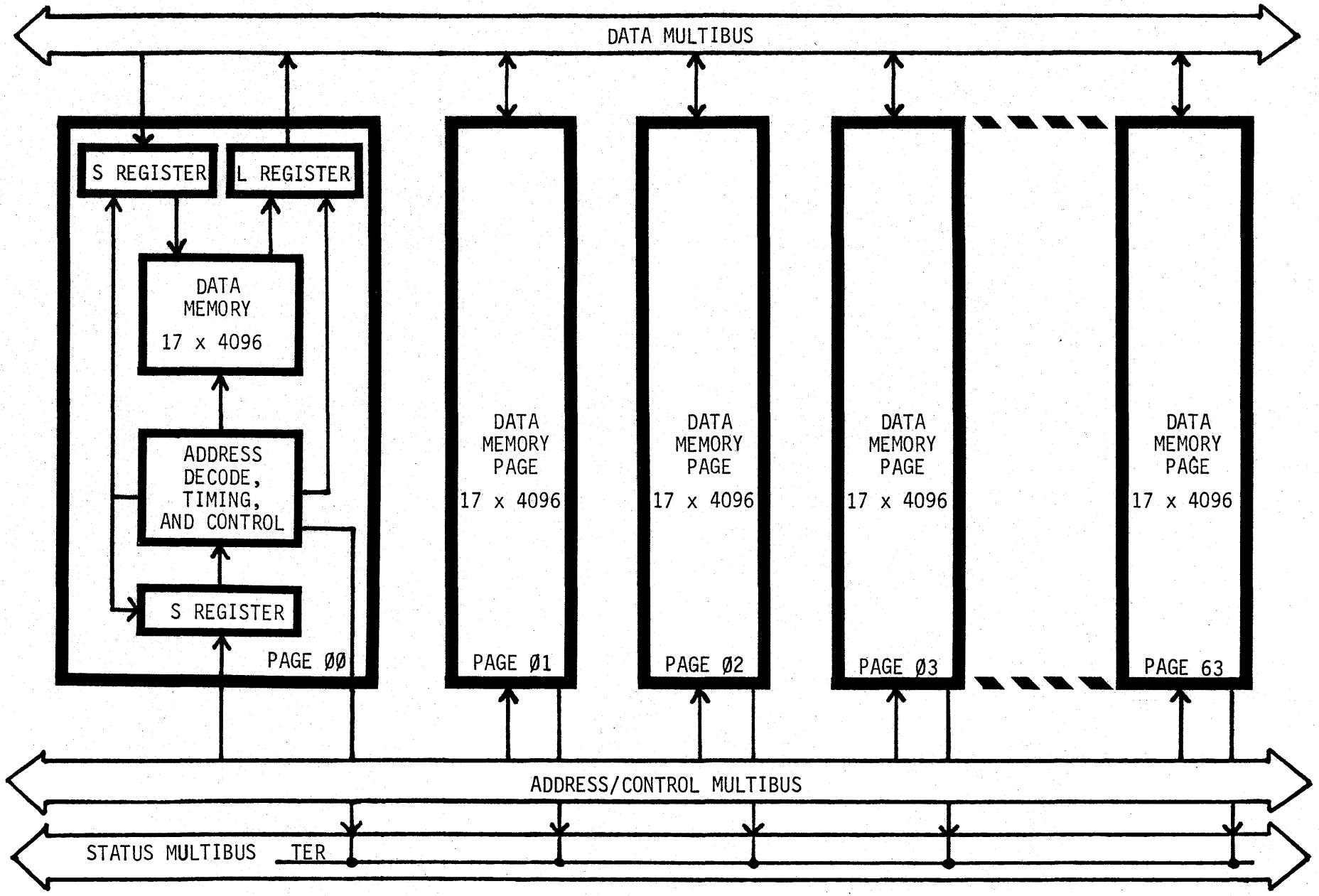


FIGURE 2.6 DATA MEMORY BLOCK DIAGRAM

When writing into data memory, the address and data must appear simultaneously on the AM and DM respectively. This information is automatically received by the S registers of each page. When the address decoding logic detects its page address, the S registers are latched, preventing further loading of these registers until the writing operation is completed. Similarly, a read instruction will cause the S registers to be latched when the appropriate page address is detected and after a delay, the contents of the specified memory location are placed in the L register and subsequently, onto the DM. Any attempt to access that same memory page while it is in the process of writing or fetching data will be ignored and memory access timing error (TER) line of the SM will be activated. The page is available again after five complete instruction cycles.

2.4.2 Memory Timing

Each page of the data memory requires 4 1/2 instruction cycles to complete a read or write operation. However, the MULTIBUS is available for other transactions during this time, as are other pages of memory. Figure 2.7 illustrates the details of the timing for both a write and a read sequence.

In the Write sequence, it is assumed that the address is issued by a WAF a [Write Aligned (address a) First] instruction in the MAP. This causes the address to be placed in the MAP's L register during the first half of the instruction cycle and enabled onto to AM during the second half of the instruction cycle. At the same time, the ARP instruction MOV1 R,L will cause the contents of the R (Result) register to be placed in the ARP's L register during the second quarter of the instruction cycle. The data from the ARP's Result register will then appear on the DM during the second half of the same instruction cycle simultaneously with the address issued by the MAP. This is received by all memory pages and other system modules, but only the addressed page latches its S registers. That page is then in a busy state until the end of instruction cycle 4, and is available again for data resulting from processor instructions during instruction cycle 5. Note, however, the MULTIBUS was occupied for only one bus cycle (50 ns).

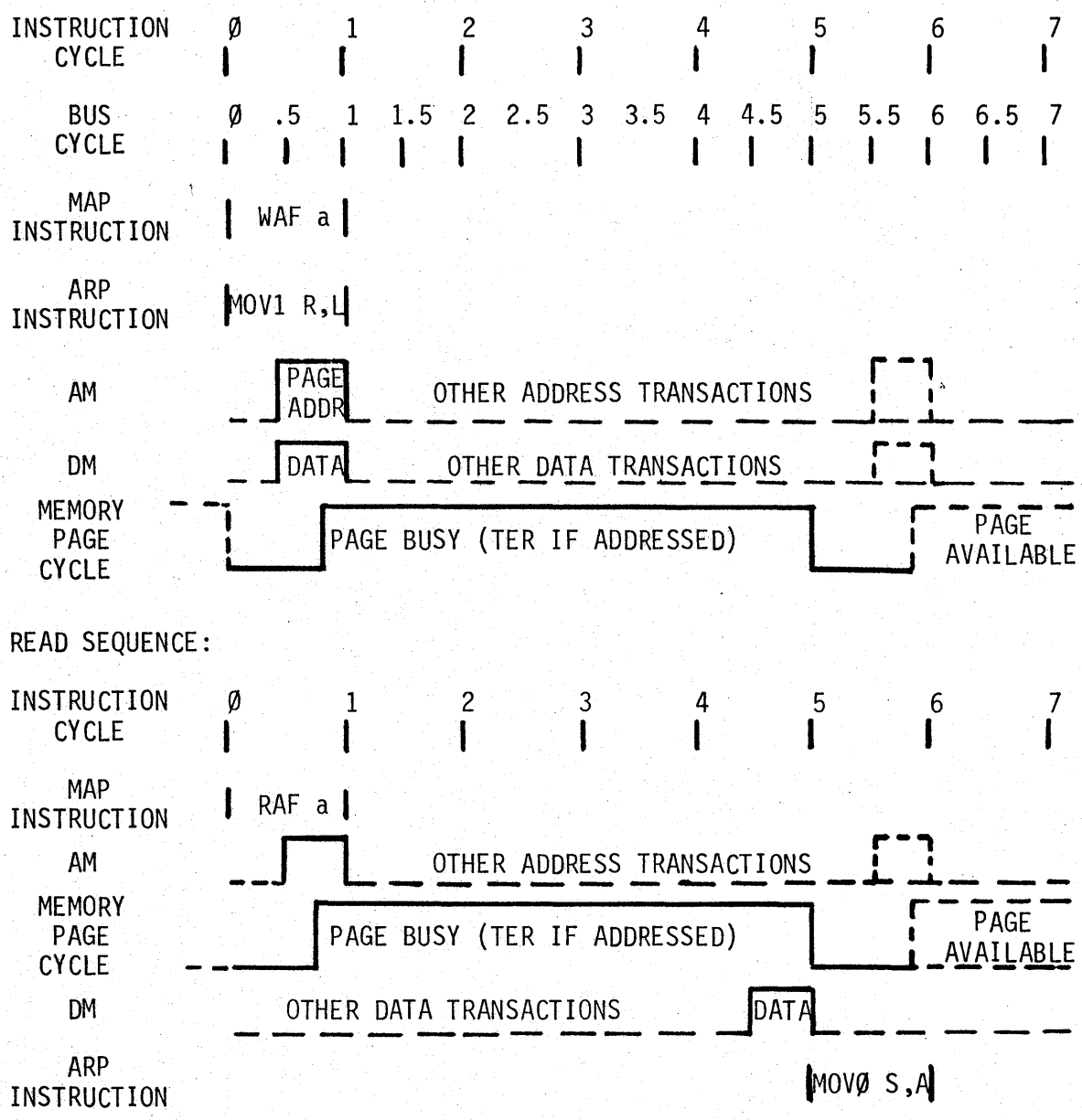


FIGURE 2.7 DATA MEMORY ACCESS TIMING

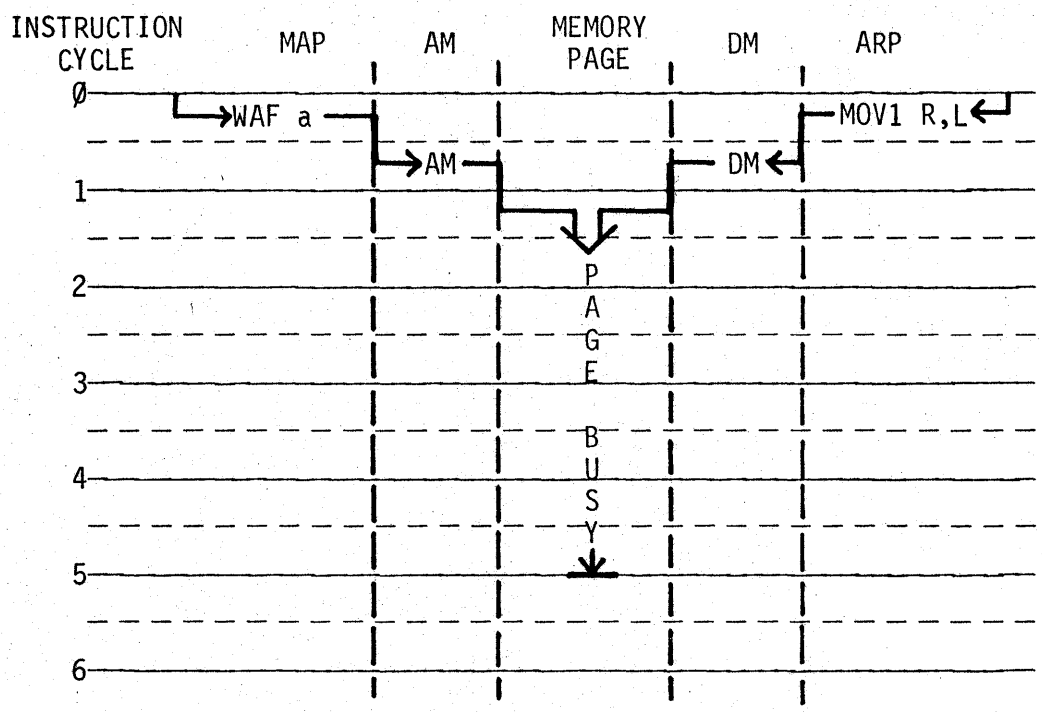


FIGURE 2.8 DATA MEMORY WRITE SEQUENCE

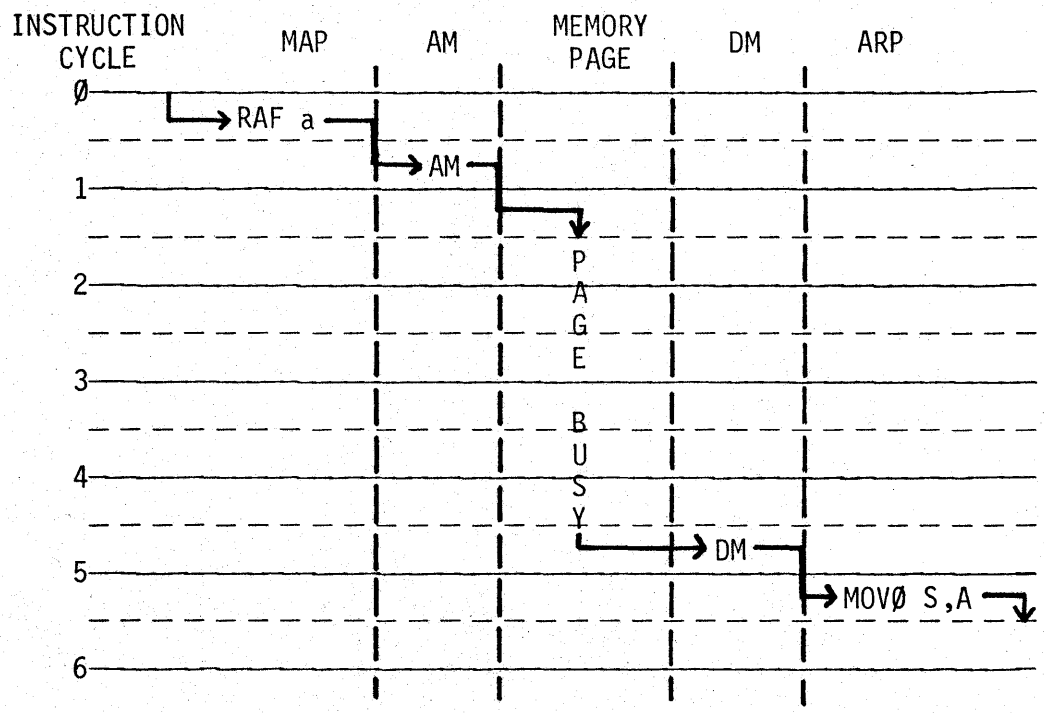


FIGURE 2.9 DATA MEMORY READ SEQUENCE

These transactions, expressed in the notation described in paragraph 2.3.5, are:

$$AM_1 \leftarrow ALIGNED(ADDRESS)$$

$$MEM_5(ADDRESS) \leftarrow DM_1 \leftarrow R_{\emptyset}$$

Figure 2.8 illustrates this operation graphically.

The Read sequence assumes a MAP instruction of RAF a [Read Aligned (Address a) First] during instruction cycle Ø. The memory page address decoding and latching of the S registers proceeds as previously described. The contents of the specified memory location are placed on the DM 4 1/2 instruction cycles later and is in the destination device's S register at the beginning of instruction time 5. The ARP instruction MOVØ S,A (or MOV1 S,A) will move this data to the ARP's A register before new data appears in the S register. Stated mathematically,

$$AM_1 \leftarrow ALIGNED(ADDRESS)$$

$$A_{5.25} \leftarrow DM_5 \leftarrow MEM_1 (ADDRESS)$$

Figure 2.9 presents the same information graphically.

2.4.3 DATA MEMORY REFRESH

The MOS memory circuits used in the AD-10 Data Memory are fully refreshed every 1.6ms to avoid loss of data. The AD-10 is provided with the necessary circuitry to accomplish the refresh activity automatically and in a manner completely transparent to the host processor. The refresh activity can also be initiated under program control to provide exact time repetition of complete programs.

The refresh activity requires the use of the MULTIBUS, and therefore the system is halted when the refresh activity is initiated. The Halt activity, including the activation of the Shutdown/Restart Buffer, plus the refresh activity for one sixteenth (1/16) of the memory, requires approximately 3 us. The refresh sequence is initiated automatically every 100 us unless a RFR instruction is issued sooner from

the COP. Thus, the refresh activity causes a 3 us dead time to occur at least every 100 us, but does not otherwise affect the system operation. The RFR instruction can sometimes be used to effectively mask the refresh time by overlapping it with other operations such as A/D conversion. The refresh activity is also initiated automatically whenever the system Run (CØ1) control line is asserted.

2.5 HOST PROCESSOR INTERFACE

2.5.1 INTRODUCTION

The Host Interface Controller (HIC), together with the Remote Interface Controller (RIC), interfaces the AD-10 to the host processor. In general, the host processor will be one of the Digital Equipment Corporation PDP-11 family of digital computers.

2.5.2 HOST INTERFACE CONTROLLER

The HIC, which is integral to the AD-10, communicates with the RIC through matched transmitter/receiver pairs over distances up to 300 meters. The RIC, in turn, is connected to the PDP-11 Unibus®, and provides all signals necessary to communicate with the asynchronous Unibus. A description of the RIC is provided in the paragraph 2.5.4

Operating through the HIC hardware with ADI furnished software, the PDP-11 (and hence the operator) is able to monitor and control the AD-10 system operation, effect data transfers, and perform detailed diagnostics of both the AD-10 program execution and hardware performance. The HIC has been designed to minimize the volume and overhead of required data transfers during program execution and yet provide access by the host processor to the innermost operations of the AD-10. The AD-10 should be regarded as an extension of the PDP-11 system, and the operator may use any of the PDP-11 hardware and software facilities as appropriate. This can range from FORTRAN call statements to use of the PDP-11 console switch panel for direct operator access.

The HIC automatically halts the AD-10 anytime it is accessed by the host processor. This allows the host processor to set or examine any accessible register in the AD-10 without disturbing the program execution relationships among the various system modules.

2.5.3 ORGANIZATION:

The Block diagram of the HIC is provided in Figure 2.10. The HIC contains or accesses up to 160 registers plus providing for a block transfer of up to 256 words to or from the Data and Processor Program Memories. These registers may be grouped as System Registers, Shutdown/ Restart Buffer Registers, History Registers, Test Registers, a Bus Address Register that operates in conjunction with the Data Bus Window, and finally access to the individual processor program counters, status enable registers, and status registers. Each of the register groups interface to all or portions of the MULTIBUS.

SYSTEM REGISTERS

These registers are essentially the termination point of the STATUS MULTIBUS and the control portion of the ADDRESS/CONTROL MULTIBUS. All system mode control (Run/Halt, Initialize, and Test) is provided in this group as well as the system status (error) registers and the halt and interrupt mask registers.

SHUTDOWN/RESTART BUFFER REGISTERS

The Shutdown/Restart Buffer Registers relieves the host processor of the burden of synchronizing MULTIBUS transactions when the system is halted and then restarted. These registers record all DATA MULTIBUS transactions plus appropriate error signals following a halt, and then place this recorded data back onto the MULTIBUS in the proper time sequence after the system is again placed in Run. This provides protection against errors resulting from a system halt or memory refresh sequence occurring between the time data is requested from Data Memory and when it is available on the DM. Sufficient pointers and capacity are available in the Buffer to allow successive Halt/Run (single step) operations.

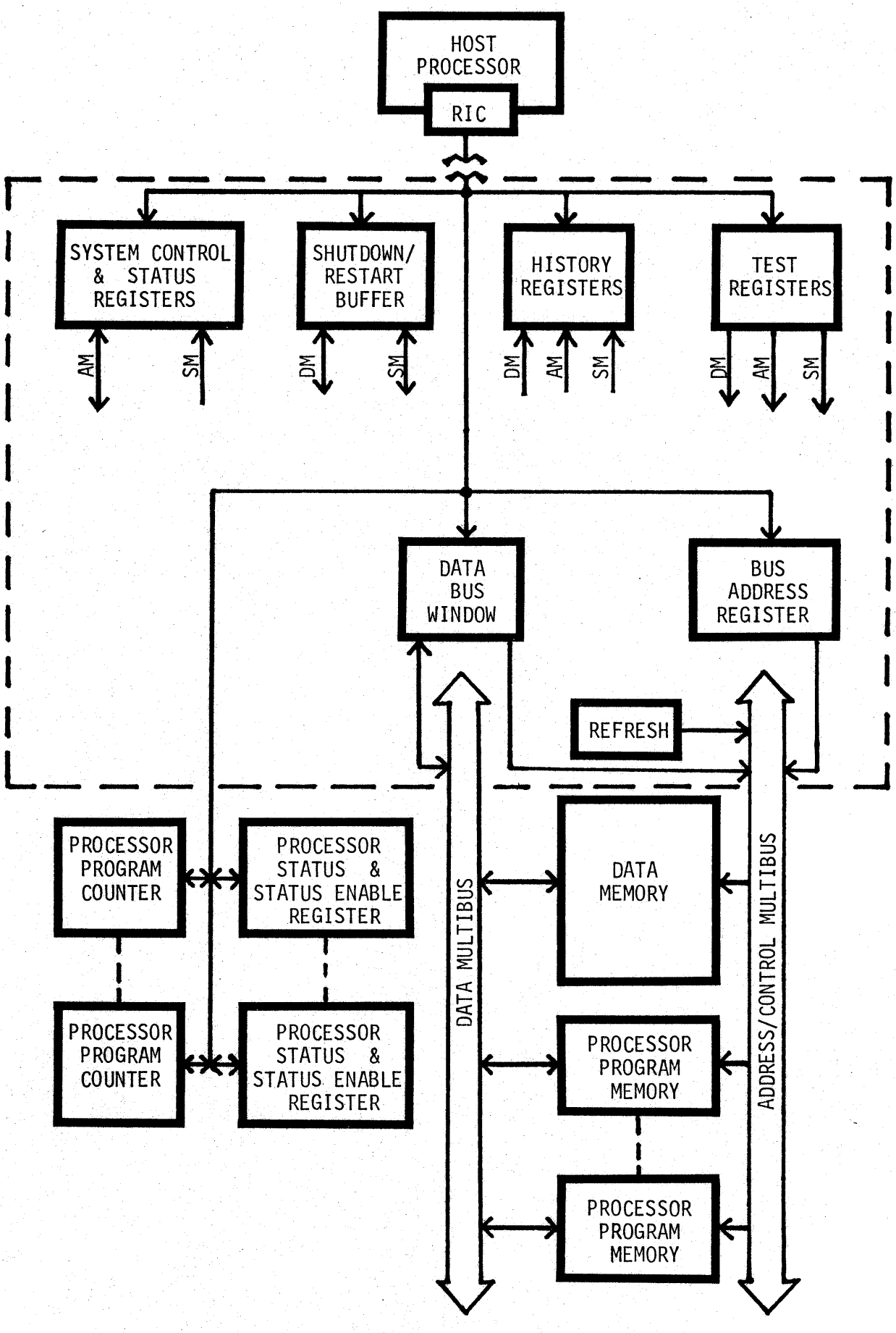


FIGURE 2.10 HOST INTERFACE CONTROLLER (HIC) BLOCK DIAGRAM

HISTORY REGISTERS

The History Registers always contain the MULTIBUS information present during the sixteen most recent MULTIBUS transactions. The recording operation is halted when the system is halted. The History Buffer Counter Register (HBC) is used by the host processor via the HIC to access the data in the History Buffer in the correct time sequence beginning with the most recent transaction.

TEST REGISTERS

The Test Registers may be used for a variety of purposes, but the primary purpose is to provide a means of exercising the AD-10 system at full speed with known data. These registers transmit sixteen bus cycles of pre-programmed (by the Host Processor) information onto the MULTIBUS. The History Registers as well as all other system modules may then be examined after a test sequence to determine proper operation and provide fault identification.

BUS ADDRESS REGISTER (BAR) AND DATA BUS WINDOW

The Data Bus Window, together with the Bus Address Register, provides the capability of transmitting blocks of data up to 256 words in length to or from the Data Memory or the Processor Program Memories. This is accomplished by first loading into the BAR the high order 12 bits of the physical address. The low order eight bits and the W/R line state are derived from the Data Bus Window address transmitted by the PDP-11. This allows up to 256 contiguous words to be transmitted between the AD-10 memories and the PDP-11 without reloading the Bus Address Register.

PROCESSOR PROGRAM COUNTERS

The program counters of the individual processors may be read and/or set by the host processor through the HIC. Both the COP and the host processor are sources of control of these counter registers.

PROCESSOR STATUS ENABLE REGISTERS

The status register of any processor may be read by the host processor. The effect of this is dependent upon the processor, but in general this includes enabling one more error condition(s) to access the STATUS MULTIBUS.

PROCESSOR STATUS REGISTERS

The status register of any processor may be read by the host processor. The information obtained is defined in the respective processor chapter. In general, however, this provides the remaining pause count, the Active/Wait status, and the current condition of the special bits relating to errors or results.

2.5.4 REMOTE INTERFACE CONTROLLER (RIC)

The Remote Interface Controller (RIC) interfaces the AD-10 to the host processor. As set forth in paragraph 2.1, the host processor is normally one of the PDP-11 series of computers. For this reason, only the RIC-11 is described.

Specifically, the RIC-11 provides:

1. Communication with the AD-10 through differential transmitter/receiver pairs.
2. AD-10 address control and selection.
3. Interface to the asynchronous PDP-11 Unibus with appropriate handshake signals.
4. RIC Status and Control registers.

TRANSMITTER/RECEIVER PAIRS

The differential transmitter/receiver pairs are matched to those in the HIC, providing reliable data transmission over distances up to 300 meters.

AD-10 ADDRESS CONTROL AND SELECTION

The AD-10 requires a maximum of 417 addresses of the 4096 addresses available on the PDP-11 Peripheral Memory Space (External Page). Selection of addresses for the AD-10 system is controlled by jumpers within the RIC hardware. One address is required for the RIC Status and Status Enable Register. Another contiguous 160 addresses are required to access the features and registers of the AD-10 via the HIC. Finally, 256 contiguous addresses are required for the DATA Bus Window feature in the HIC. The only address restriction is that the DATA BUS WINDOW must be located at a base address that is a multiple of 1000 octal bytes.

UNIBUS INTERFACE

The RIC-11 is connected directly to the PDP-11 Unibus and contains all of the hardware necessary to provide the interlocked asynchronous communication characteristic of the Unibus. The AD-10, through this channel to the Unibus, is always a slave device. It is capable of causing an interrupt if the appropriate enable registers have been set, but all transfers are under the control of the CPU or other devices connected to the Unibus.

RIC-11 STATUS REGISTER

The RIC-11 Status Register is a 16-bit register that may be read by other devices connected to the Unibus (normally the CPU). Only bit 15 (most significant bit) is used as follows:

> Bit 15 - Set to a 1 when the AD-10 is connected to the RIC-11 and is under power. A Ø indicates that either the AD-10 is not connected or not powered.

RIC-11 STATUS ENABLE REGISTER

Only Bit Ø6 of the 16 bit Status Enable Register is used. When this bit has been set (by the CPU) to a 1, then an interrupt request emanating from the IMR (Interrupt Mask Register) in the AD-10 HIC will be recognized by the PDP-11.

2.6 GENERAL PROCESSOR DESCRIPTION

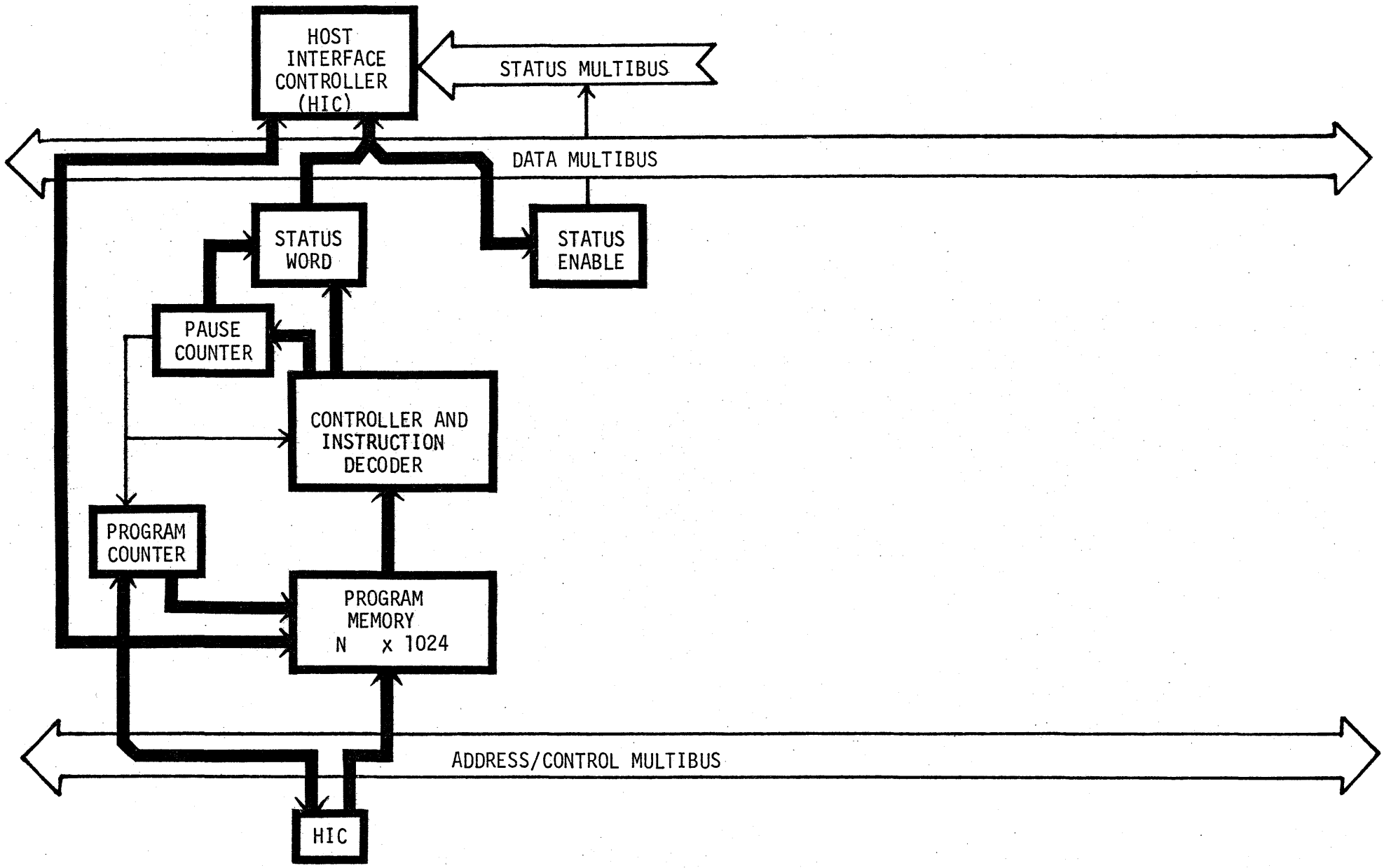
The AD-10 is equipped with a variety of processors that are optimally designed to perform a specific function. However, these processors share a common design philosophy that is described in this section. The special characteristics of each processor are discussed in the respective processor chapters.

All processors interface to the MULTIBUS and may be designed to access any portion of the MULTIBUS. In addition, each processor derives its timing from the clock and synchronization signals carried on in the bus. The interface to the DM and the AM is provided through bus storage (S) registers and bus load (L) registers. New data is written into the S registers each and every bus cycle regardless of whether or not that particular processor has need of that information. The processor must be programmed to operate on the information at the appropriate time. Similarly, output information must be placed in the L register(s) at the appropriate time, as new data in the L register(s) will cause the contents to be placed on the bus during the next bus cycle time. Except for the ARP, the processor instructions automatically handle the loading of the L register(s) and hence this is not a concern of the programmer.

The block diagram of Figure 2.11 illustrates the functional organization typical of all processors. This diagram omits the processor address decoding, timing; and S and L registers for clarity.

CONTROLLER AND INSTRUCTION DECODER

The Controller and Instruction Decoder is the heart of the processor. Here the instructions brought from memory are decoded and the specified operations implemented. These may encompass a wide variety of operations, many of which happen simultaneously. The extremely fast computational speed of the AD-10 processors is due in a large part to the configuration of the instruction word.



AD 10 PROCESSOR ORGANIZATION BLOCK DIAGRAM

FIGURE 2.11

(out of order) → next p. should precede this...

processor is Active. The program counter (and the controller/instruction decoder) stop whenever the processor is placed in the Wait state or a system Halt occurs or when the Pause Counter is active.

The contents of the Program Counter may be read and/or set by the host processor through the HIC. The COP (Control Processor) may also set the contents of the Program Counter in all processors including its own. This feature, together with the decision capacbility of the COP,, allows program looping and conditional execution to be programmed in any processor.

PAUSE COUNTER

Each processor contains a Pause Counter and is equipped with an instruction to set the pause counter. Except for the COP. the pause instruction, resulting in the execution of the instruction followed by a pause of n instruction times. The Pause Counter contains three bits in all processors except the COP. which is equipped with a 10 bit Pause Counter.

The contents (remaining count) of the Pause Counter are displayed in the processor Status Word which may be read by the host processor through the HIC. Reading this register does not affect the contents of the Pause Counter. The Pause Counter may be set only by an instruction in the respective processor, and is automatically cleared whenever the contents of the Program Counter are changed.

STATUS WORD

The processor Status Word is a register which contains the status and error information of each processor. This register may be read by the host processor through the HIC. The contents of the status word are explained in the respective processor descriptions, but in general this displays the electrical presence of the processor, the Active/Wait status, the remaining pause count, and the errors or conditions that have occurred since the last status word reading.

The word is sized to the requirements of the processor and may range up to 96 bits in length. This provides the capacity to specify many complex operations in a single word and reduces the complexity of the decoding logic. The instruction set generally takes advantage of this word length, but a significant amount of microcoding is still possible to further increase the processor speed.

The control signals to all parts of the processor emanate from the controller. However, only those that relate to instructions are illustrated in the block diagram by a narrow line. The broad lines indicate multiple lines generally carrying address or data information.

PROCESSOR PROGRAM MEMORY

Each processor contains 1024 words of high speed bipolar memory. The word length of each memory is tailored to the tasks required of that processor with a minimum of 16 bits and a maximum of 96 bits. Each group of 16 bits is referred to a Field, with Field Ø being the low order bits of the instruction word. Some bits within the instruction word are not used, and these bits are always read as a zero.

The memories may be loaded or read by the host processor through the Data Bus Window in the HIC. This is accomplished by first setting the Block Address Register in the HIC to the desired base address. This one time operation includes setting the processor address (number), the field address, and the high order bits of the desired word in memory. Blocks of up to 256 "words" may then be transmitted through the Data Bus Window where a "word" is 16 bits comprising one field of the total instruction word. The field address in the BAR remains constant, thereby accessing the same field of successive instruction words. The AD-10 Debugger automatically accesses the BAR to load or examine complete instruction words.

PROGRAM COUNTER

The Program Counter specifies the next instruction word to be transferred from the program memory to the instruction decoder. Normally, the counter is incremented by one for each AD-19 instruction time when the

STATUS ENABLE

The Status Enable register is an enabling register that allows selective control by the host processor of signals that may access the AER line of STATUS MULTIBUS. If a signal (error or condition) is enabled to the SM, it will cause the AER bit in the EHS register of the HIC to be set. The activity then initiated is controlled by the HMR and IMR registers in the HIC.