APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
1020089	8510	A	RELEASE PER 8500-13	10/28/76	
1020090	8530				

8500

NOTES :

1. For Revisions See Sheet 2

PRE-PRODUCTION

NOV 01 1976

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± .XX ± .XXX ± DECIMALS ± ANGLES ±	CONTRACT NO.	AMCOMP SUNNYVALE, CALIFORNIA	
	APPROVALS / DATE		
	DRAWN W. Roma 10/7/76	PRODUCT SPECIFICATION MODEL 8500 DISC MEMORY	
MATERIAL	CHECKED 10/19/76		
FINISH		SIZE A / CODE IDENT NO. / DRAWING NO. 1570013 / REV A	
DO NOT SCALE DRAWING		SCALE / SHEET 1 OF 21	

1570013

PAGE NUMBER

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A							

SIZE	CODE IDENT NO.	DRAWING NO.	REV
A		1570013	A
SCALE		SHEET 2	

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LIST OF TABLES AND FIGURES

1.0 INTRODUCTION

1.1 Scope

This specification describes a rotating memory designed for storage of data with an average access time of 8.3 milliseconds (3600 RPM), or 16.7 milliseconds (1800 RPM) and a maximum storage capacity of 38.4×10^6 bits.

1.2 Model Number

The Model Number is constructed as shown below:

85X0-Y

X	SPEED
1	1800 RPM
3	3600 RPM

Y	NUMBER OF TRACKS
16	Sixteen tracks
32	Thirty-two tracks
48	Fourty eight tracks
64	Sixty-four tracks
96	Ninety-six tracks
128	One hundred and twenty-eight tracks
192	One hundred and ninety two tracks
256	Two hundred and fifty six tracks

2.0 REFERENCE DOCUMENTS

2.1 Outline and Mounting Drawing - DWG. No. 1520006

2.2 Power Supply Specification - DWG. No. 1510017-01

3.0 GENERAL SPECIFICATIONS		8530 Series	8510 Series
3.1	Storage Capacity (Maximum)	40.2×10^6 bits	40.2×10^6 bits
3.2	Data Tracks (Maximum)	256 (plus 32 spares)	256 (plus 32 spares)
3.3	Bits/Track (Unformatted absolute Maximum)	157,000	157,000
3.4	Gap between TO and 1st Sector	40 microseconds/ min.	40 microseconds min.
3.5	Bits/Sector		

The maximum sector length is determined by the track capacity, from the following relationships:

Case 1: Track capacity $<$ 122,000 bits:
Max Sector Length = 1,550 bits

Case 2: Track capacity $>$ 122,000 bits:
Max Sector Length = $1550 - \frac{0.11}{7}(C - 122000)$

3.6	Preamble (written by Disc Memory)	19 bits	19 bits
3.7	Postamble-Write Guard Bits (written by Disc Memory)	1 bit	1 bit
	- Guard Space	12 bits	12 bits
3.8	Rotational Speed	3600 $\pm$ 95 RPM	1800 $\pm$ 55 RPM
3.9	Average Access Time	8.3 $\pm$ 0.2 milsec.	16.7 $\pm$ 0.4 milsec
3.10	Data Transfer Rate (at 150,000 bits/track)	9.0 $\pm$ 0.6 M Bits/sec	4.5 $\pm$ 0.3M Bits/sec
3.11	Disc Diameter	12 inch	
3.12	Recording Medium	NiCo with Rhodium protective overcoat	
3.13	Recording Density (at 150,000 bits/track	7448 Bits/Inch Maximum (innermost data track)	
3.14	MTBF	10,000 hours for 85XX-256 models	

SIZE	CODE IDENT NO.	DRAWING NO.	REV
A		1570013	A
SCALE		SHEET 5	

3.15 MTTR — One hour

3.16 Error Rate

Recoverable Errors:

The occurrence of recoverable errors shall be less than one error in 10^{11} bits read.

Non-recoverable Errors:

The occurrence of non-recoverable errors shall be less than one error in 10^{12} bits read.

NOTE: A non-recoverable error is defined as a single bit or many consecutive bits in error from which valid data cannot be recovered within three consecutive passes through the same data record.

3.17 Preventative Maintenance

The Disc pre-filter and power supply filters shall be replaced when they become dirty.

4.0 ENVIRONMENTAL SPECIFICATIONS

4.1 Temperature

Operating (assumes writing at one extreme and reading at the opposite extreme)	0 to 55°C
Non-operating (On Site)	0 to 65°C
Non-operating (Shipping and storage properly packed)	-30 to 65°C

4.2 Temperature Change

Operating max. for data reliability	10°C per hour

4.3 Relative Humidity

Operating without condensation:	10% - 90%
Non-Operating without condensation	10% - 90%

4.4 Shock and Vibration

Vibration	Operating:	.040" double amplitude displacement, 5-22 Hz; 1g acceleration max, 22 - 500 Hz
	Non-operating	.040" double amplitude displacement, 5-30Hz; 2g acceleration max, 30 - 500 Hz
Shock:	Operating:	5g 11 Msec 1/2 sine wave
	Non-operating	5g 11 Msec 1/2 sine wave

4.5 Shipping

The packaged product to meet the approval of the NATIONAL SAFE TRANSIT COMMITTEE, Project 1A. (100 lbs or less)

4.6 Altitude

Operating:	10,000 feet
Non-operating:	25,000 feet

4.7 Atmosphere — Non-corrosive

5.0 POWER REQUIREMENTS

5.1 A.C. Power

5.1.1	Voltage (single phase, rear panel selectable)	88 - 108 VAC RMS 105 - 130 192 - 240 210 - 260
5.1.2	Frequency	47 - 53 Hz 57 - 63 Hz
5.1.3	Start Current (with 120 volts)	8.3 amps maximum
5.1.4	Run Current (with 120 volts)	2.7 amps maximum

SIZE	CODE IDENT NO.	DRAWING NO.	REV
A		1570013	A
SCALE		SHEET 7	

5.1.5 Motor Start Time — 20 seconds maximum

5.1.6 A toggle power ON/OFF switch provides power control for motor and D.C. power supply.

5.1.7 A single fuse protects the transformer. The fuse is located in the line cord receptacle at the rear of the unit.

5.2 Power Loss

The system is capable of withstanding an A.C. power loss of 10 milliseconds without malfunction or data error.

5.3 UL/CSA Approval

5.3.1 UL Component Recognition per UL-478 will be obtained and maintained, except for 50 Hz only units.

5.3.2 CSA Listing per C22.2 will be obtained and maintained, except for 50 Hz only units.

6.0 MAJOR MEMORY SYSTEM COMPONENTS

The 8500 Series is composed of the following major component parts.

6.1 Disc

A 12-inch diameter, .200 inch thick plated with nickel cobalt is mounted to the spindle assembly. The disc has a thin Rhodium overcoat to allow contact start - stop.

6.2 Spindle

The disc is mounted to the spindle via a "zero - clearance" assembly which maintains the disc location throughout the machine's temperature range. The locking device is an impeller to provide filtered air for pressurizing the enclosure. The spindle is driven by means of a belt and step pulley.

6.3 Drive Motor

A capacitive start, 50/60 Hz induction motor provides the power to the disc. A step pulley compensates for a change in line frequency. Separate motors are used for 1800 and 3600 RPM applications.

6.4 Read/Write Head Assemblies

6.4.1 Standard triple transducer configuration read/write heads are used.

6.4.2 The transducers contact the disc when the disc is not rotating, and fly 12 ± 5 micro inches when the disc reaches operating speed.

6.5 Memory Assembly

6.5.1 The basic memory assembly consists of the baseplate spindle, disc, head plate, and motor.

6.5.2 The memory assembly is supported by four shock mounts.

6.5.3 The rotating assembly is in a dust sealed enclosure which is pressurized by a filter impeller system; the minimum required pressures are:

.05 inches of water:	1800 RPM
.20 inches of water:	3600 RPM

6.5.4 The maximum allowable particle count in the rotating assembly is: less than 5 particles, 0.5 microns or larger over a 10 minute period and a flow rate of 0.01 cubic feet/minute.

6.6 Interface Electronics

6.6.1 The digital interface electronics are packaged on a vertically mounted P.C. Board (Interface Board) at the back of the package.

6.6.2 The Input/Output functions of the disc unit are transmitted and received by 7400 TTL family devices.

6.7 Read/Write Electronics

With the exception of the Clock Preamplifier, the analog Read/Write and the head selection electronics are packaged on a P.C. board (Memory Board) which is mounted directly above the Disc Memory Sub Assembly.

6.8 Bit Clock, Sector and Track Origin Generation

6.8.1 One triple transducer head assembly is mounted to detect the recorded bit clock, sector clock and track origin (TO).

6.8.2 Clocks are recorded on two tracks simultaneously for the purpose of having one identical spare.

6.8.3 Changing from one track to the spare set is accomplished by changing a wire wrap jumper.

6.8.4 The third track may be used to record an AMCOMP standard format.

6.8.5 Protection is provided to prevent erasure or alteration of these recorded timing signals.

6.9 D.C. Power Supply

6.9.1 The D.C. Power Supply exhibits the following general characteristics.

+5V ± 3%, 4.5A
+24V ± 3%, 1.0A
-12V ± 3%, 1.0A

6.9.2 The specifications of the power supply are documented in DWG. No. 1510017-01

6.10 Other Assemblies

6.10.1 The tray assembly supports the Disc Memory Sub Assy and also mounts the A.C. input connector and inner slides.

6.10.2 The rear panel assembly mounts on the tray and holds the Interface Card. The rear panel assembly also mounts the I/O connectors for the active unit.

6.10.3 The RFI cover encloses the electronics and reduces both susceptibility to and emissions of stray magnetic fields. The RFI cover is easily removed for access to the major electronics.

7.0 PHYSICAL CHARACTERISTICS

7.1 Outline Dimension

7.1.1 Height 8.75 inches

7.1.2 Depth 22.00 inches

7.1.3 Mounting Width: Standard 19-inches

7.1.4 The outline dimensions and mounting details are documented in DWG No. 1520006.

7.2 Weight 95 lbs

8.0 INTERFACE SPECIFICATIONS - GENERAL

8.1 Levels

8.1.1 The I/O signal levels and pertinent figures are defined as seen on the I/O connector.

8.1.2 Signal levels on the bus of the disc memory system are nominally 0 and +3.0 volts, which are compatible with both TTL and DTL family of circuits.

8.1.2.1 Interface logic levels are defined as shown below:

LOGIC 0	0 volts nom. +0.4 volts max.
LOGIC 1	+2.4 volts min. +3.0 volts nom. +5.25 volts max.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
A		1570013	A
SCALE		SHEET 11	

8.1.3 Every line must be driven toward ground by a NPN transistor collector that is capable of sinking 48 ma and maintaining a maximum saturated output voltage of 0.4 volts.

The following integrated circuits are especially suited to these requirements:

Part Number	Manufacturer
Sn 7438, SN75451	Texas Instruments

8.1.4 All signals to and from the disc are negative true (except BUS terminated and illegal address)

8.1.5 All signal lines will also be terminated at the controller.

8.1.6 A typical Driver-Receiver configuration is shown in Figure 1.

8.2 Daisy-Chaining

8.2.1 The interface allows for (4) disc units to be daisy-chained and operated by one controller.

8.2.2 The bus system is designed for a maxi mum length of 30 feet considering a 9.0 M bit transfer rate.

8.3 Interface Connectors

8.3.1 Two 50-pin connectors are provided in the rear panel assembly to allow daisy chaining. A mating connector (Part No. 1090010-01) is available.

8.3.2 The following table identifies the interface signal pin assignments.

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	RETURN	42	READ
18	DISC READ	43	RETURN
34	N/C	10	WRITE
35	TRACK ADDRESS-7	27	RETURN
2	TRACK ADDRESS-6	11	READ DATA
19	TRACK ADDRESS-5	28	RETURN
3	TRACK ADDRESS-4	44	BUS TERMINATED
20	TRACK ADDRESS-3	45	RETURN
36	TRACK ADDRESS-2	12	WRITE DATA
37	TRACK ADDRESS-1	29	RETURN
4	TRACK ADDRESS-0	13	SPARE 1
21	UNIT SELECT 3	30	DC GROUND
5	UNIT SELECT 2	46	READ CLOCK
22	UNIT SELECT 1	47	RETURN
38	UNIT SELECT 0	14	SPARE 2
39	RETURN	31	RETURN
6	ILLEGAL ADDRESS	15	WRITE CLOCK IN
23	RETURN	32	RETURN
7	NOT USED IN 8500	48	SPARE 3
24	RETURN	49	RETURN
40	TRACK ORIGIN	16	WRITE CLOCK OUT
41	RETURN	33	RETURN
8	SECTOR CLOCK	17	SHIELD GROUND
25	RETURN	50	SHIELD GROUND
9	SECTOR WRITE		
26	RETURN		

TABLE I. J2 - INTERFACE SIGNAL PIN ASSIGNMENT

SIZE	CODE IDENT NO.	DRAWING NO.	REV
A		1570013	A
SCALE		SHEET 13	

9.0 INTERFACE SIGNAL DEFINITION - DISC INPUT SIGNALS

9.1 Unit Select

9.1.1 Four unit select lines are provided to support chaining up to four discs on a single cable assembly.

One line is assigned to a disc. Selection is made by the installation of a jumper assembly on the interface board.

All discs will be shipped with the Unit Select 1 jumper installed.

9.1.2 The proper unit select line must be set to logic zero to allow the disc to write, read, or change track address.

9.1.3 Following the end of a read operation, the unit must stay selected for at least 1 usec. See Fig. 4.

9.1.4 By adding a jumper from TP22 to TP58 the following additional functions are disabled by deselecting the unit.

Write Clock Out
Sector Clock
Disc Read
Track Origin

9.2 Write

9.2.1 When the signal is set to a logic zero, data on the WRITE DATA line will be recorded on the selected disc track.

The WRITE signal must be set to a logic zero synchronized to the SECTOR CLOCK.

The WRITE command must remain at a logic zero until the last bit of data has been transmitted and then reset to a logic one (Ref. Figure 2)

9.3 Read

9.3.1 When this signal is set to a logic zero, the READ DATA along with the READ CLOCK will be transmitted from the selected data head.

The READ signal must be set to a logic zero synchronized to the SECTOR CLOCK.

The READ command must remain at a logic zero until the last bit has been received and then reset to a logic one (Ref. Figure 4).

9.4 Write Data

9.4.1 When WRITE is a logic zero, this signal line will carry serial NRZ data to be recorded on the selected data head.

9.5 Write Clock In

9.5.1 This signal is the cable delayed version of WRITE CLOCK OUT.

WRITE DATA is received in the disc electronics with this continuous clock (Ref. Fig. 3). WRITE CLOCK IN must be present for a min. of 20 bits after sending the last WRITE DATA bit.

9.6 Track Address

9.6.1 These eight lines provide the binary address of the data head to which a write or read operation is to be performed.

These lines must be present and stable as long as a write or read operation is performed.

The full eight lines are to be used regardless of the specific number of heads installed in the disc (256 maximum, 16 minimum).

9.7 Sector Write

9.7.1 The clock format can be written with this line, when the disc unit has been properly set up for initialization by a field engineer.

10.0 INTERFACE SIGNAL DEFINITION - DISC OUTPUT SIGNALS

10.1 Track Origin

10.1.1 The TRACK ORIGIN is a single pulse, one bit wide, defining the start of a disc revolution.

This signal line, normally a logic one, is pulsed to a logic zero to indicate TRACK ORIGIN.

10.2 Sector Clock

10.2.1 The SECTOR CLOCK is a single pulse, one bit wide, defining the start of a sector. All WRITE and READ commands are timed from the SECTOR CLOCK.

This signal line, normally a logic one, is pulsed to a logic zero to indicate SECTOR CLOCK (Ref. Figure 5).

10.3 Read Data

10.3.1 When READ is a logic zero, this signal line will provide serial NRZ data from the selected data head in synchronism with the READ CLOCK. (Ref. Figure 4)

10.4 Read Clock

10.4.1 The READ CLOCK defines each bit of data to be read on the READ DATA output line.

The READ CLOCK is only present when actual data is present on the READ DATA line. The READ CLOCK is a repetition pulse with a period of one bit (Ref. Figure 5).

10.5 Write Clock Out

10.5.1 The WRITE CLOCK OUT is a continuous clock signal defining each bit cell on the track.

This signal shall be used to transmit WRITE DATA to disc unit and shall be returned to the disc unit as a WRITE CLOCK IN.

The WRITE CLOCK OUT can be used to strobe the Sector and Track Origin Clocks into the Controller.

10.6 Disc Ready

10.6.1 When this signal is a logic zero, the disc unit is ready to reliably transmit or receive data.

The DISC READY will be set to a logic one under the following conditions:

1. DC voltages below acceptable limits

2. Disc rotational speed below reliable operating range.

3. BUS TERMINATED is at logic zero.

10.7 Illegal Address

11.7.1 This signal will be set to a logic one when the received address exceeds the maximum address of the machine or, in machines equipped withthe write lock-out feature, a write operation is attempted on a"locked-out" track.

10.8 Bus Terminated

10.8.1 The BUS TERMINATED signal senses the power to the active disc interface terminations. A logic zero on this line indicates a loss of power to the signal line terminations. All other interface lines should be considered invalid.

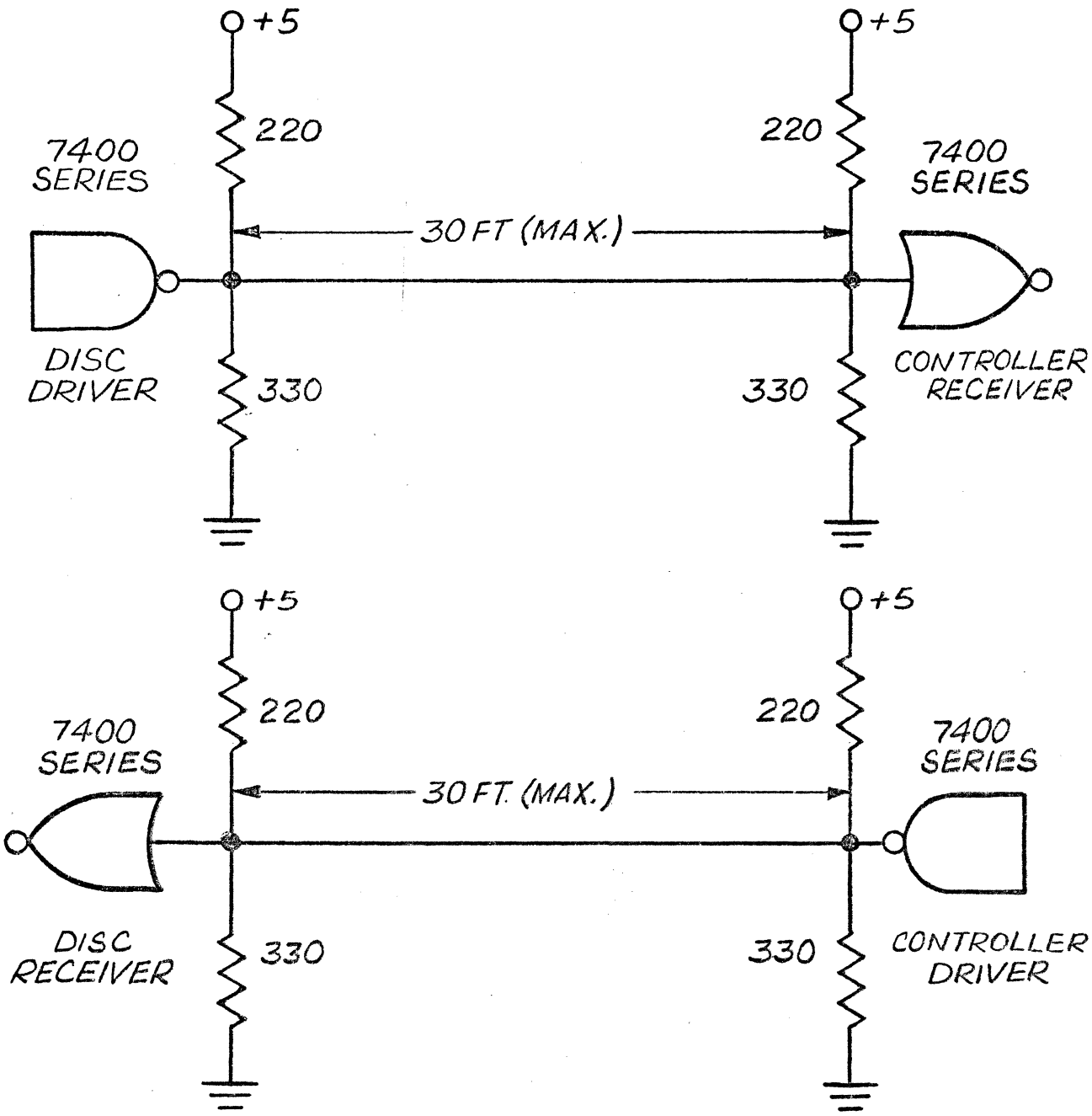
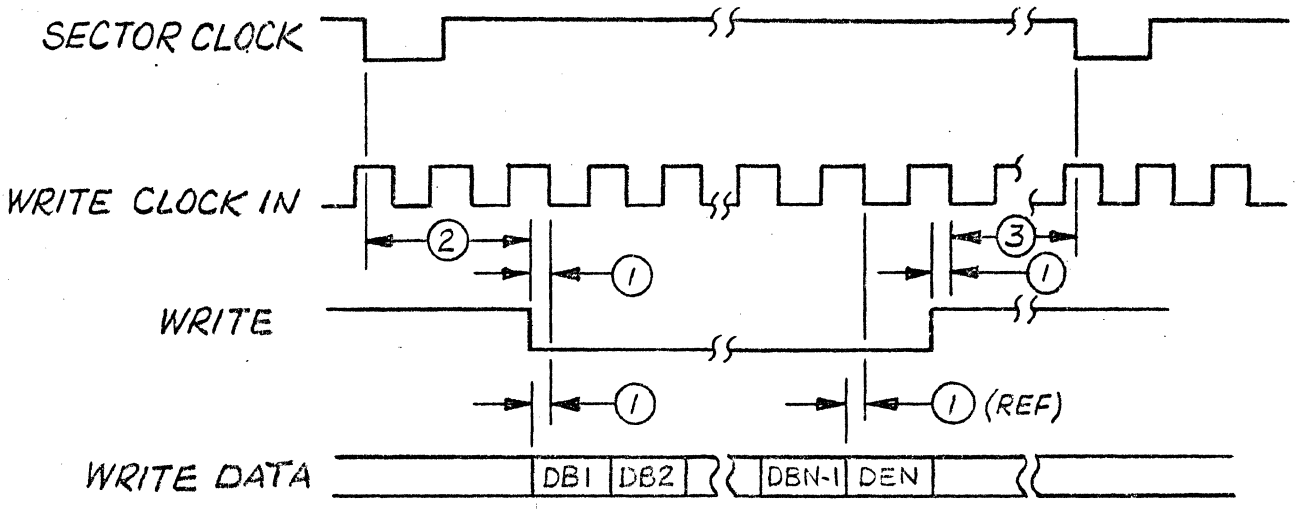


Figure 1. Typical Driver-Receiver Configuration

SIZE	CODE IDENT NO.	DRAWING NO.	REV
A		1570013	A
SCALE		SHEET 18	

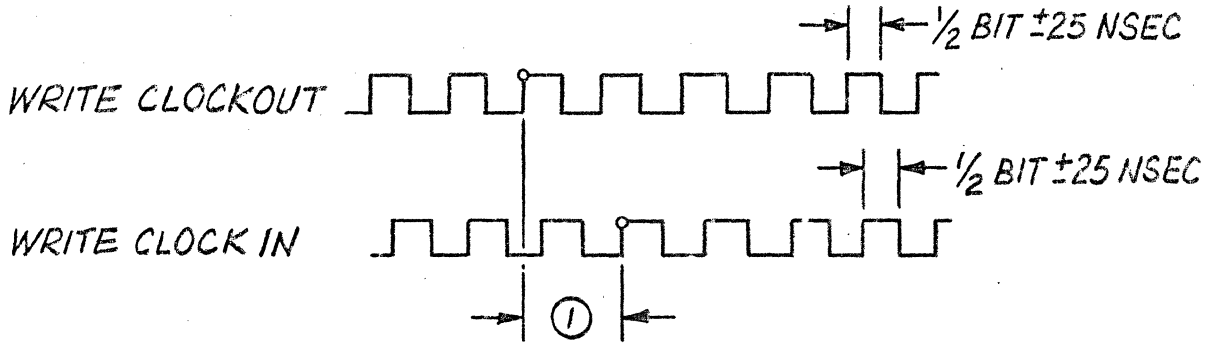


① 25 nsec. min; 1 bit - 25 nsec. max.

② turn around delay<4 bits Once established must be constant ± 25 nsec.

③ 32 bits -②

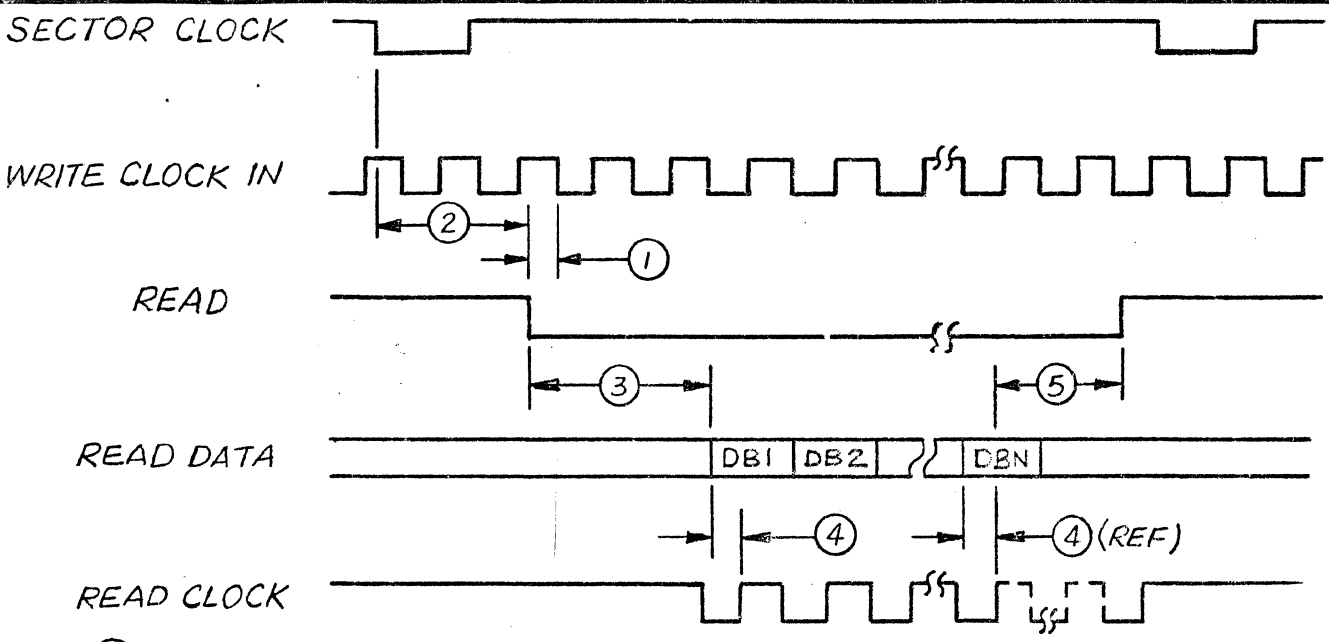
Figure 2. Timing Diagram, Write Timing



① Round trip cable, driver/receiver delay. Once established must remain constant ± 25 nsec.

Figure 3. Timing Diagram, Clock Timing

SIZE	CODE IDENT NO.	DRAWING NO.	REV
A		1570013	A
SCALE		SHEET 19	



① 25 nsec. min; 1 bit - 25 nsec. max.

② Turn around delay < 4 bits. Once established must be constant ± 25 nsec

③ 24 ± 4 bits

④ 1/2 bit -40/-20 nsec

⑤ Turn around delay <4 bits. Once established must be constant ± 25 nsec.

NOTE:

1) Following receipt of DBN and Read Clock N, additional Read Clocks may occur due to turn around delay of Read reset. These clocks should be ignored.

2) Last Sector Clock to Truck-Origin is equal in time relations like a Sector Clock to the next Sector Clock.

Figure 4. Timing Diagram, Read Timing

SIZE	CODE IDENT NO.	DRAWING NO.	REV
A		1570013	A
SCALE		SHEET 20	

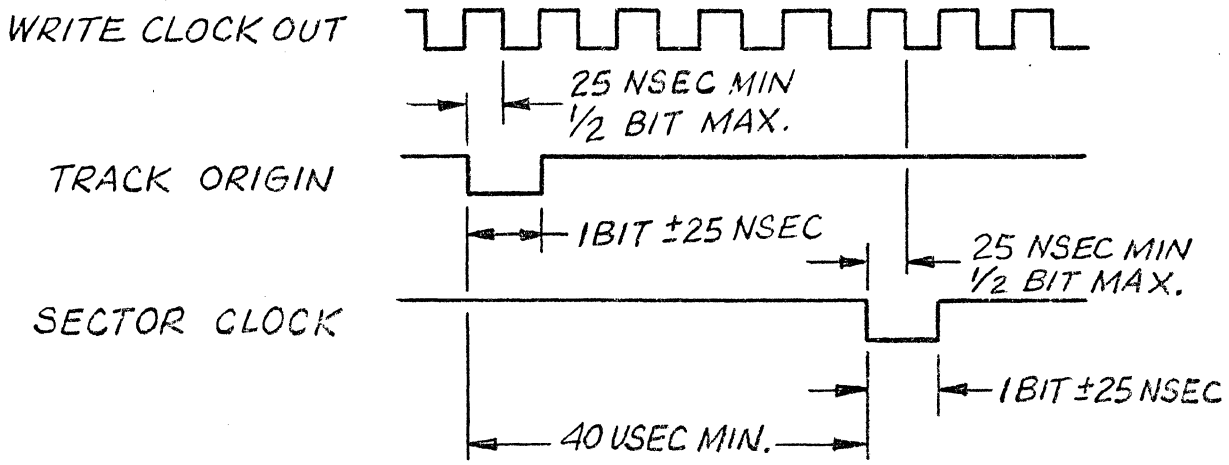


Figure 5. Timing Diagram, Basic System Timing

SIZE	CODE IDENT NO.	DRAWING NO.	REV
A		1570013	A
SCALE		SHEET 21	

RECORDING CODES IN THE 8500

1. NRZI

2 MFM (AMCODE)

WHICH ONE ?

1. NRZI

   a) Simple to encode & decode

   b) Large "window"

   c) Previously used in 8400

2. MFM

   a) NO JITTER PROBLEMS

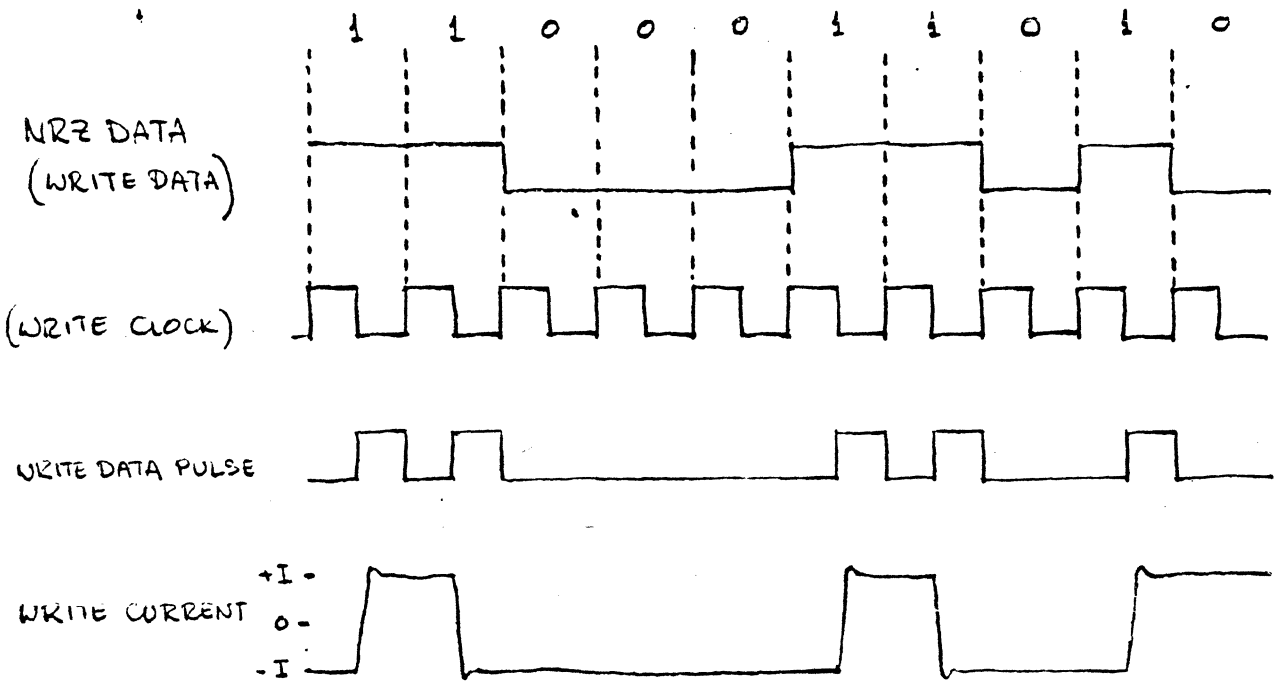
   b) No sector size limitations

   c) Same ratio of fci to Bpi as NRZI, therefore no loss in density.

ENCODING RULES

NRZI

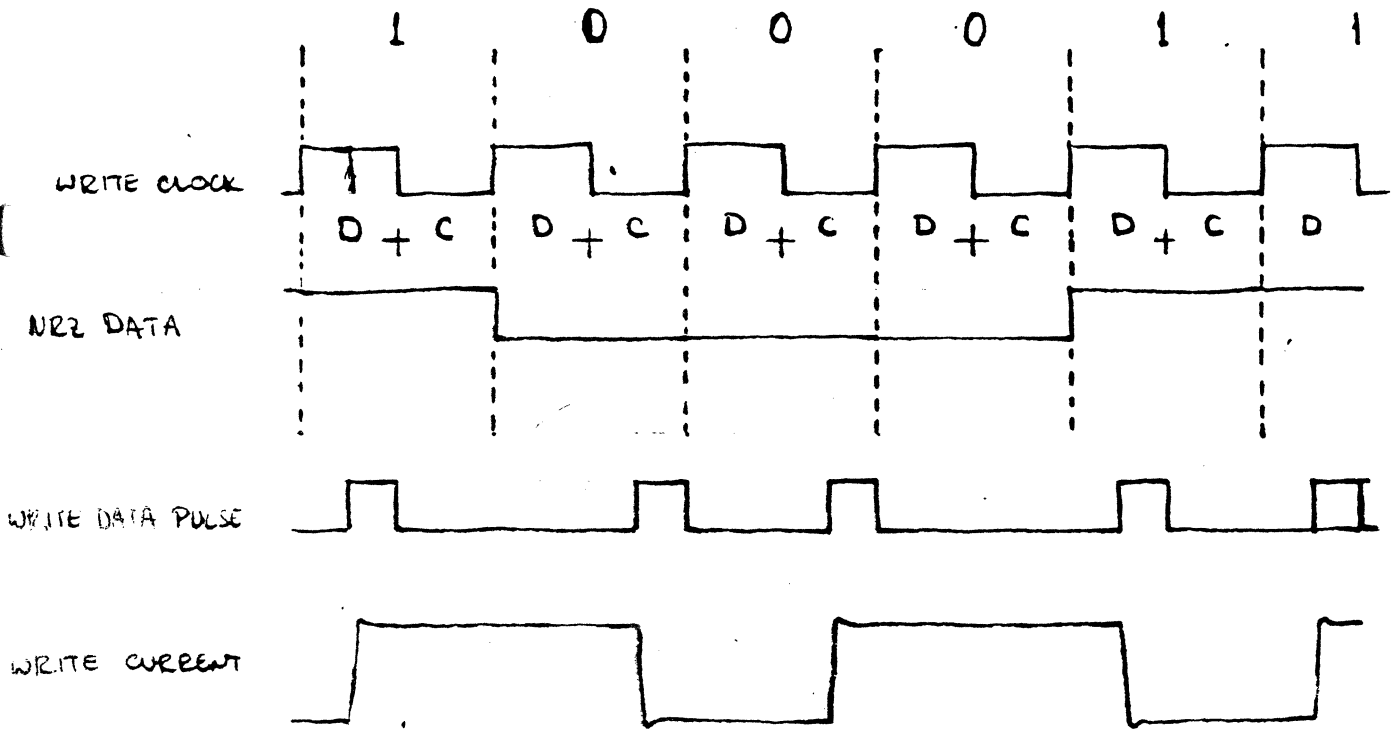
A flux Change for every 'one'.



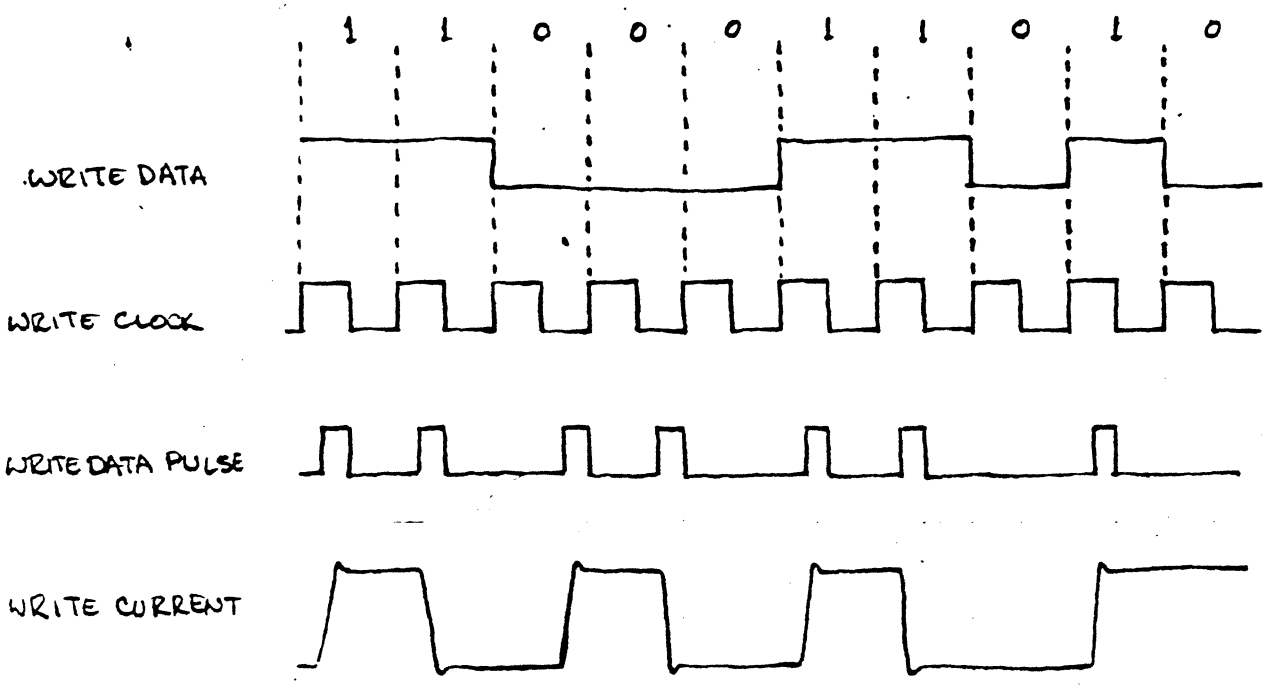
ENCODING RULES

MFM

1. A flux change in the "Data" half of the cell for every "one".
2. A flux change in the "Clock" half of the cell for every "zero" except when a "zero" is followed by a "one".

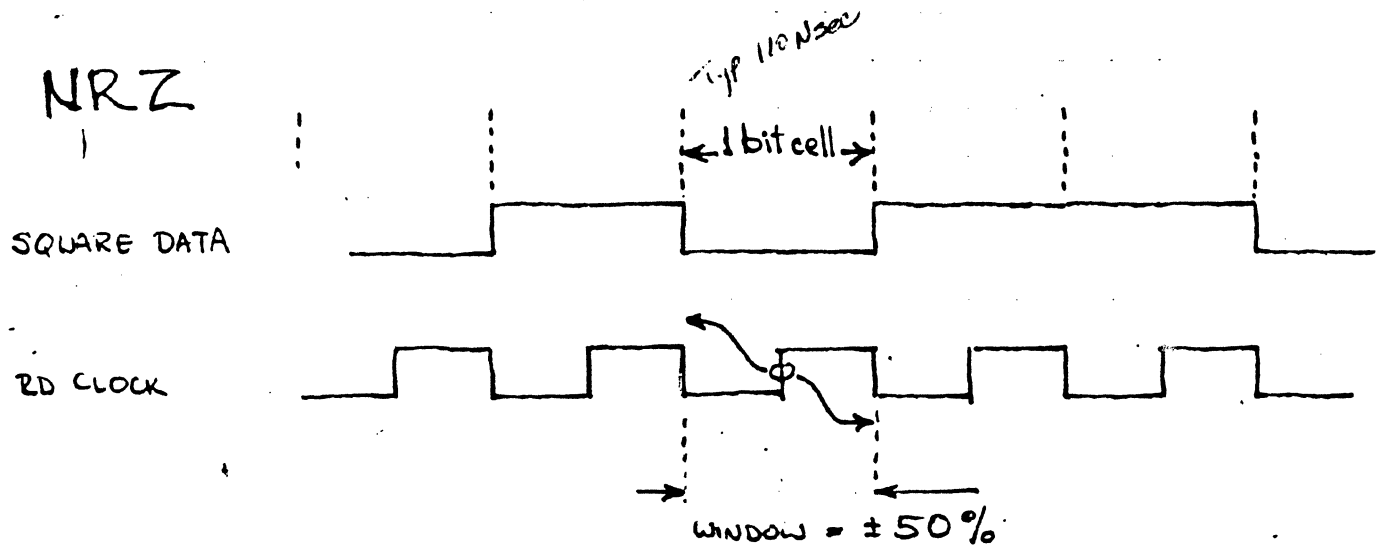


MFM PATTERN (same as NRZI pattern used previously)



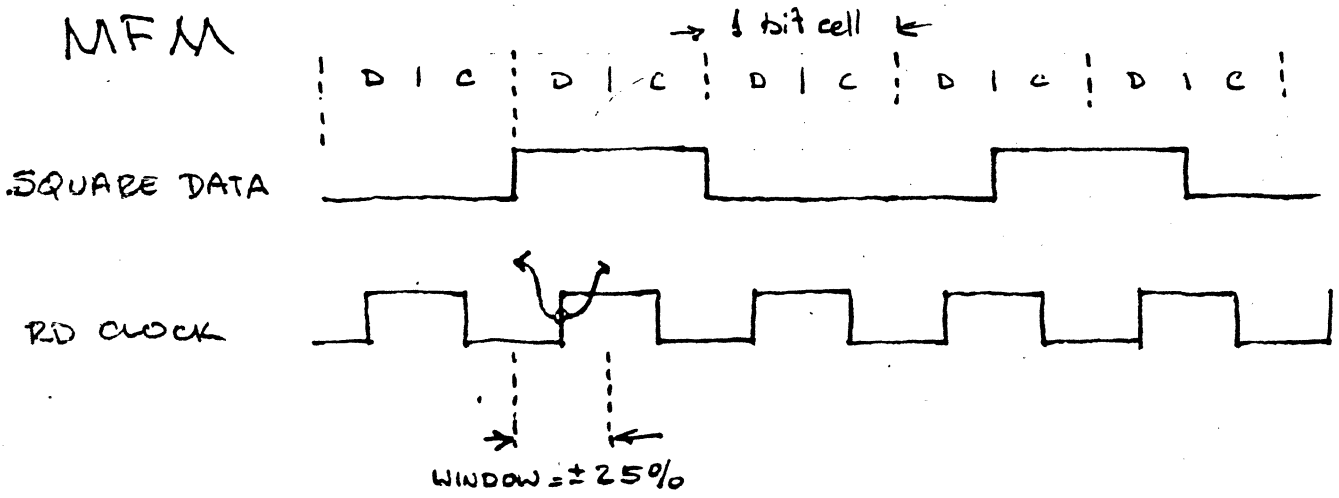
WHAT IS THE WINDOW ?

NRZ



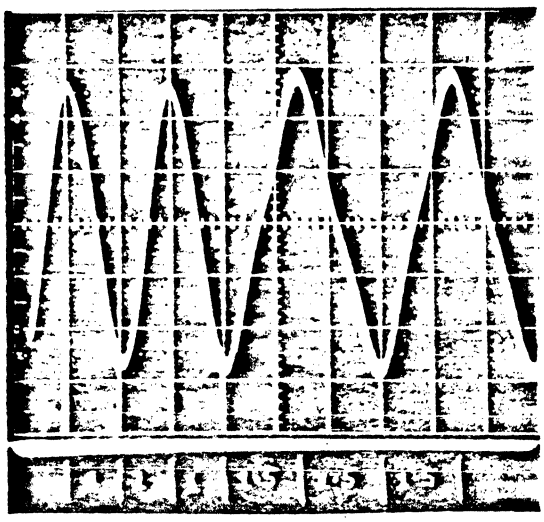
∴ The leading edge of clock can drift ±50% of the bit cell before it misses the data transition.

MFM



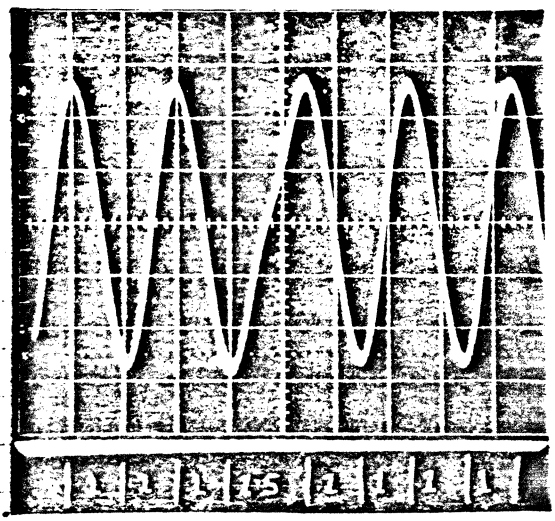
∴ The leading edge of the clock can drift ±25% of the bit cell before it misses a transition in the Data half of the cell.

TYPICAL PATTERNS

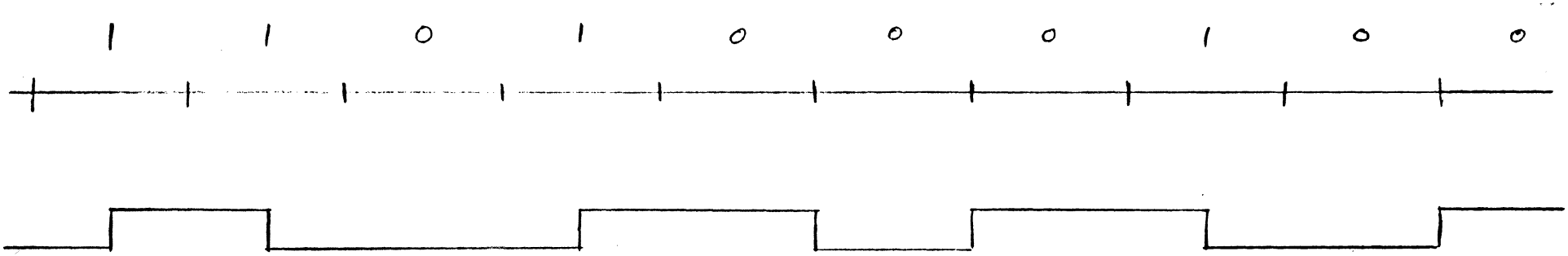


1111001001

1111010101



1111000000

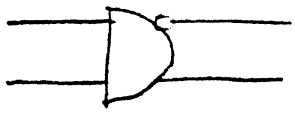


MFM PATTERN RULE

1. "ONES" BIT – WRITE FLUX CHANGE IN CENTER OF CELL
2. "ZEROS" BIT – WRITE FLUX CHANGE AT END OF CELL IF NEXT BIT IS A ZERO
3. FLUX CHANGES ARE NOT CLOSER THAN ONE BIT TIME
4. FLUX CHANGES ARE NOT FARTHER APART THAN TWO BIT TIMES.

AMCODE

10124 - QUAD TTL - ECL TRANSLATOR



4 / PACKAGE

10231 - DUAL TYPE D FLIP FLOP

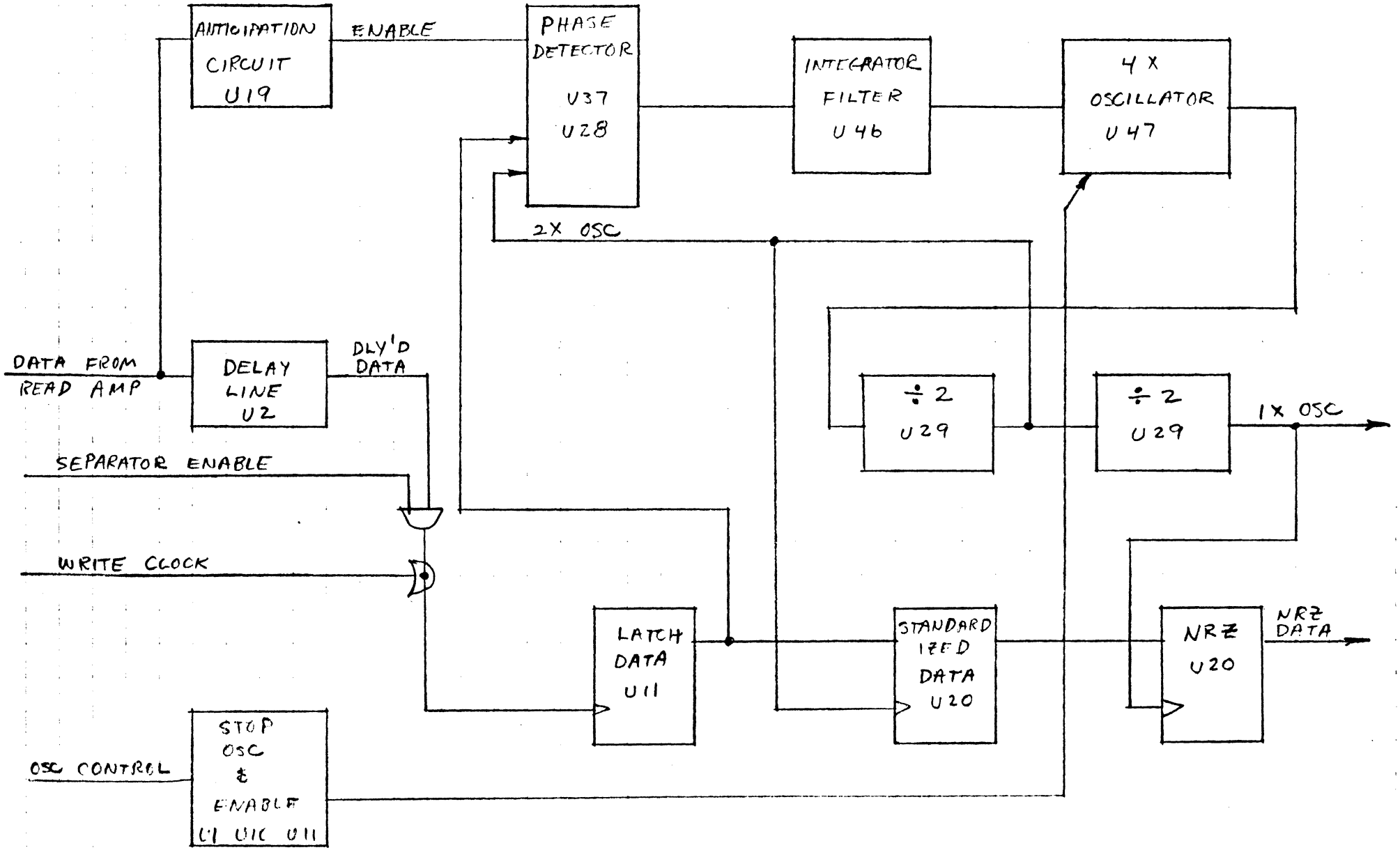
POSITIVE EDGE TRIGGER
POSITIVE LEVEL SET - RESET

10125 - QUAD DIFFERENTIAL INPUT ECL-TTL TRANSLATOR

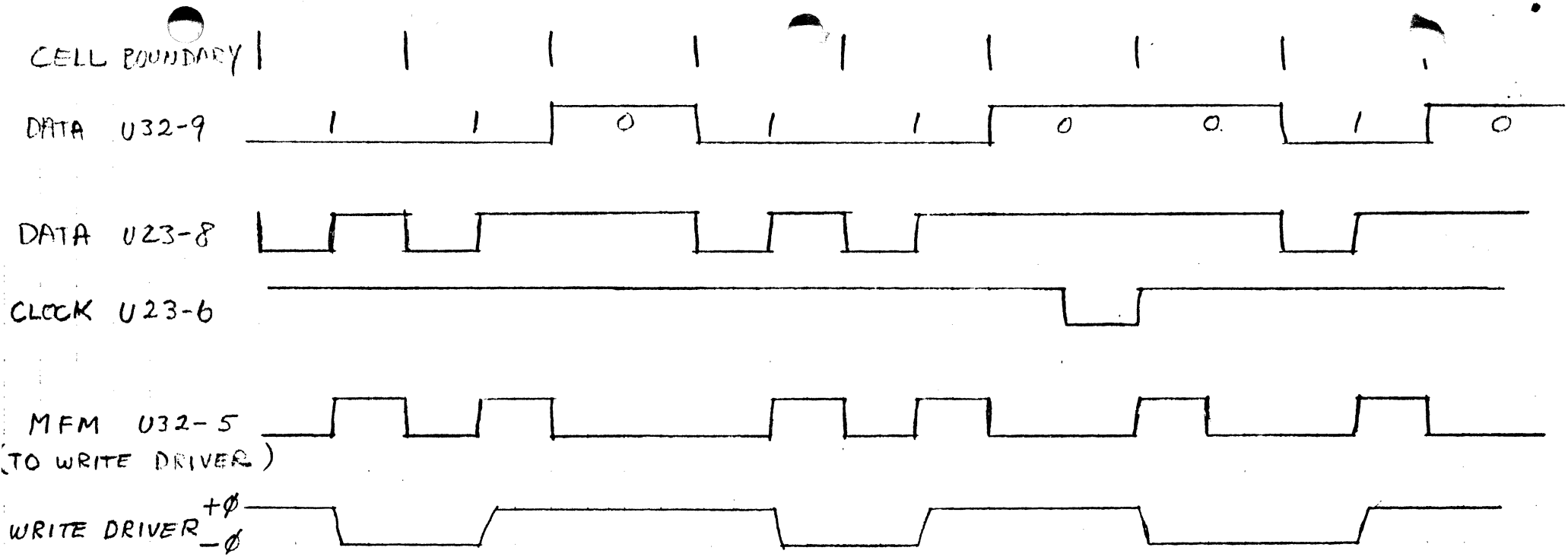
10104 - QUAD AND/NAND

10116 - DIFFERENTIAL LINE RECEIVER

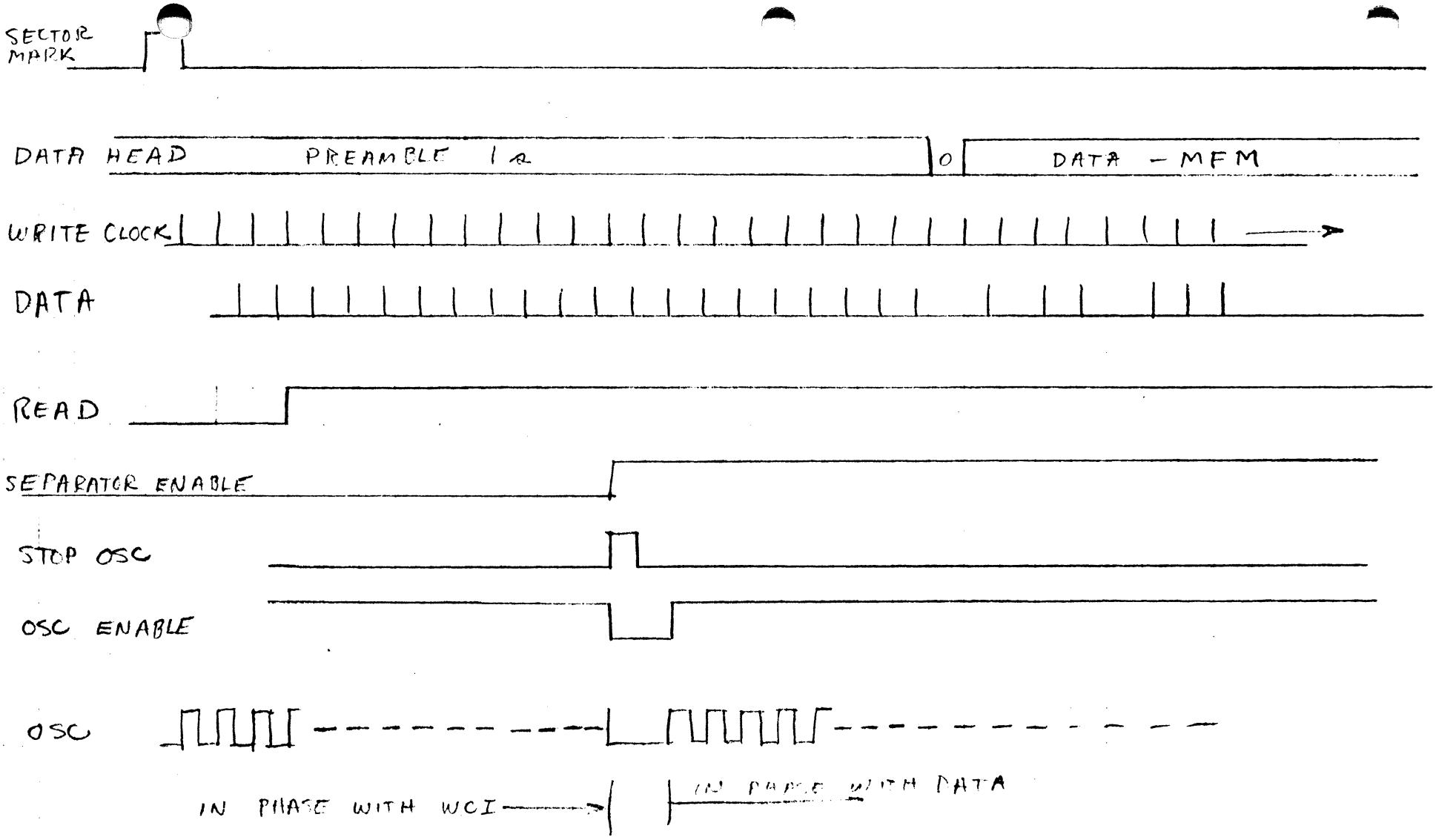
ASSUME NOMINAL LEVELS -0.9 V TRUE
-1.8 V FALSE



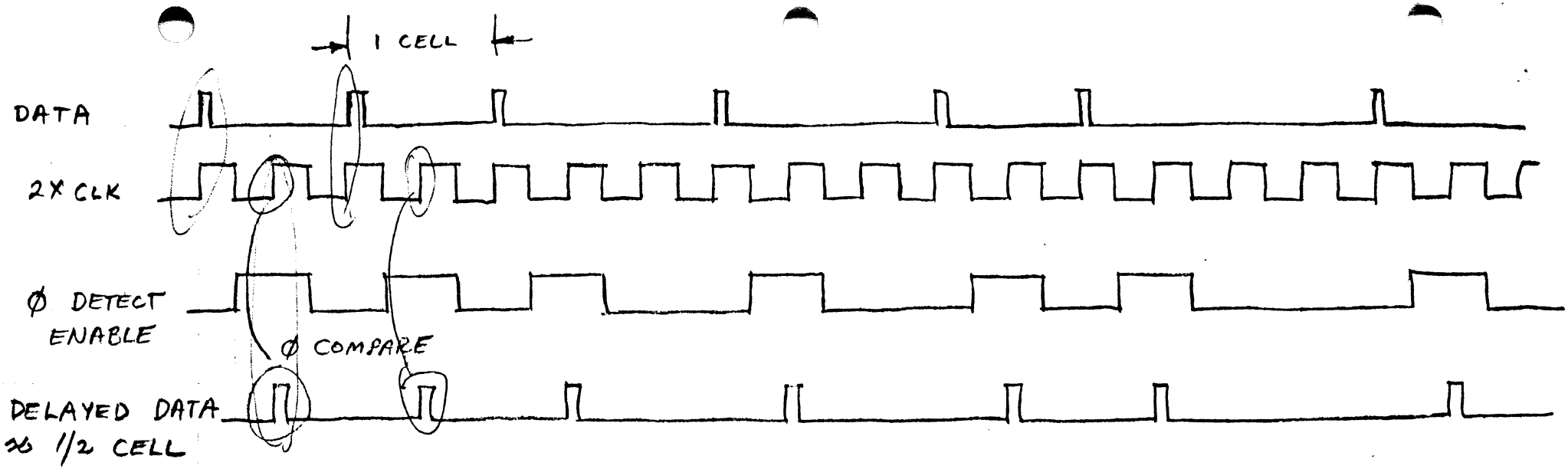
DATA SEPARATOR BLOCK

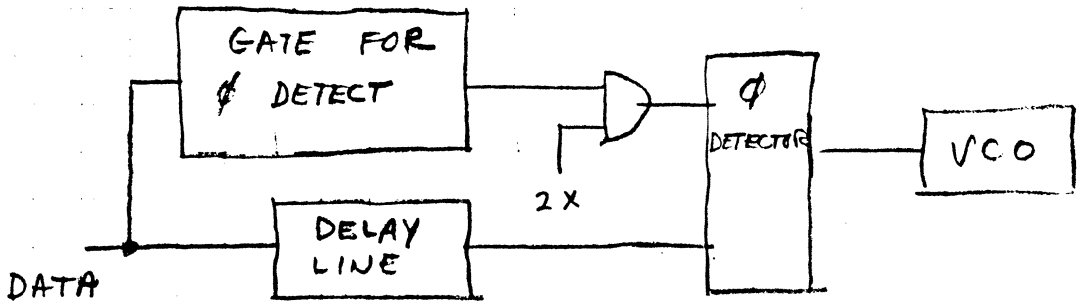


MFM WRITE ENCODE



SEPARATOR SYNC





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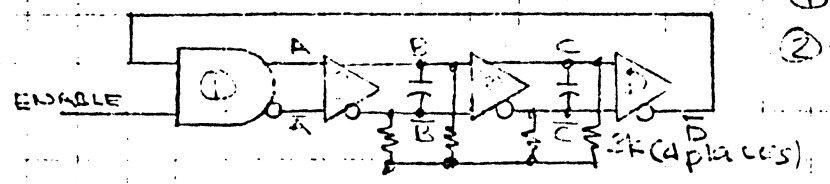
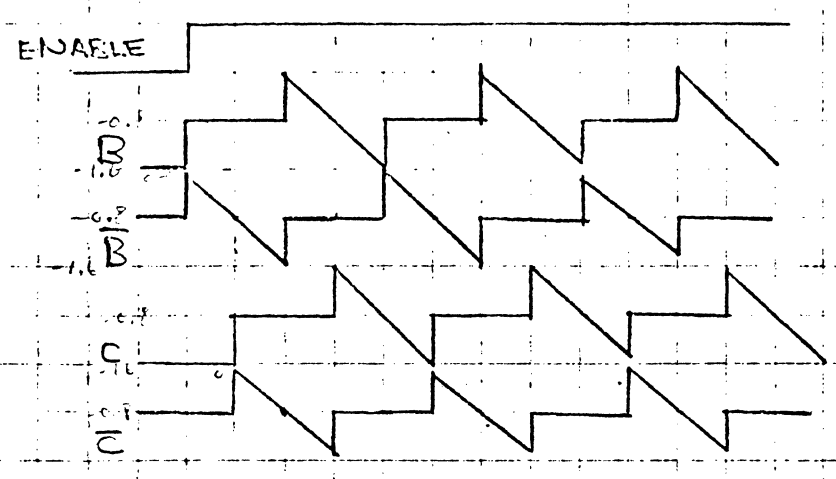
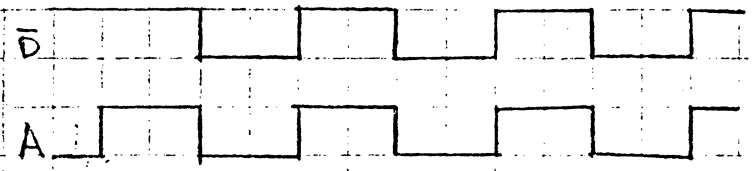
BASIC Ø DETECT



① = 10104

②-④ = 10116





$$i = C\frac{dv}{dt} = \frac{V_c}{R}$$

$$\Delta T = \frac{\Delta V}{V_c} RC$$

Timing of 1 period = Prop delay of ① + Pd of 2 + RC ② + Pd ③ + RC ③ + Pd ④

$$= 3 \times P_D \text{ 10116} + P_D \text{ of 10104} + \frac{\Delta V}{V_c} RC$$

$$20.6nS = 3 \times 2nS + 2.2nS + \frac{.8V}{4.55V} RC$$

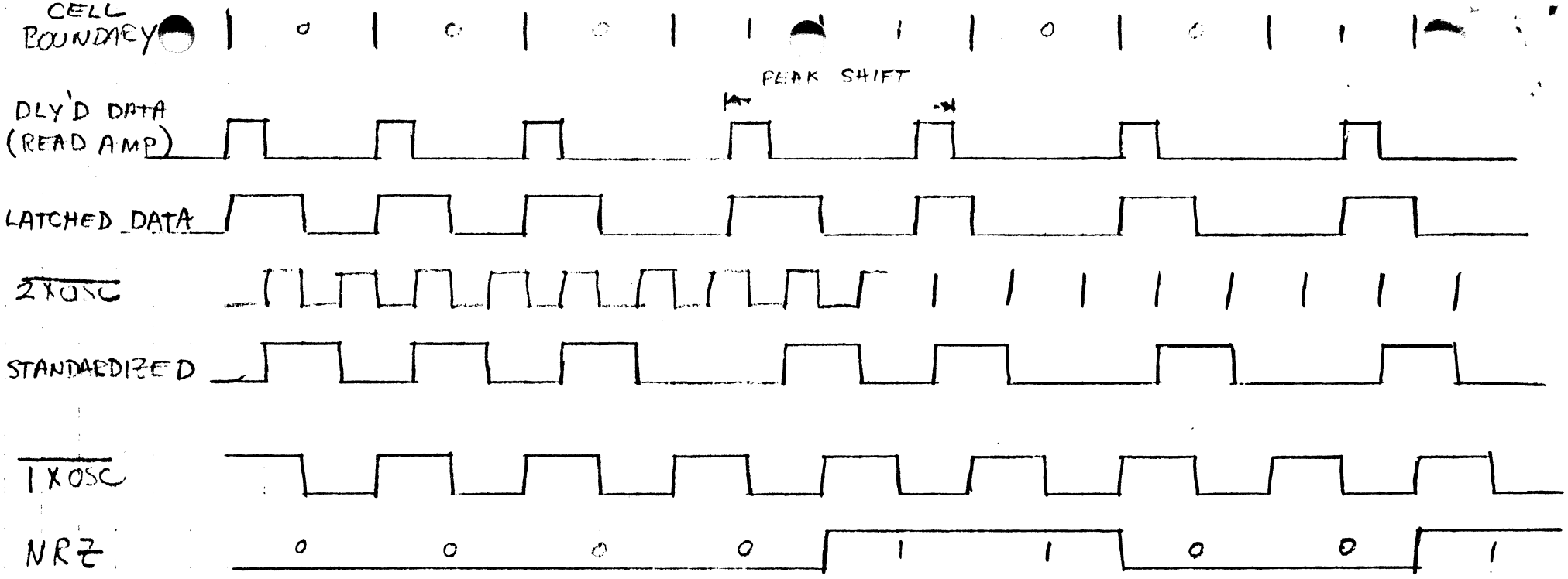
$$20.6nS = 8.2nS + \frac{.8V}{4.55V} RC$$

$$10.6nS = \frac{.8}{4.55} RC \qquad RC = \frac{4.55}{.8} \times 10.6nS = 60nS$$

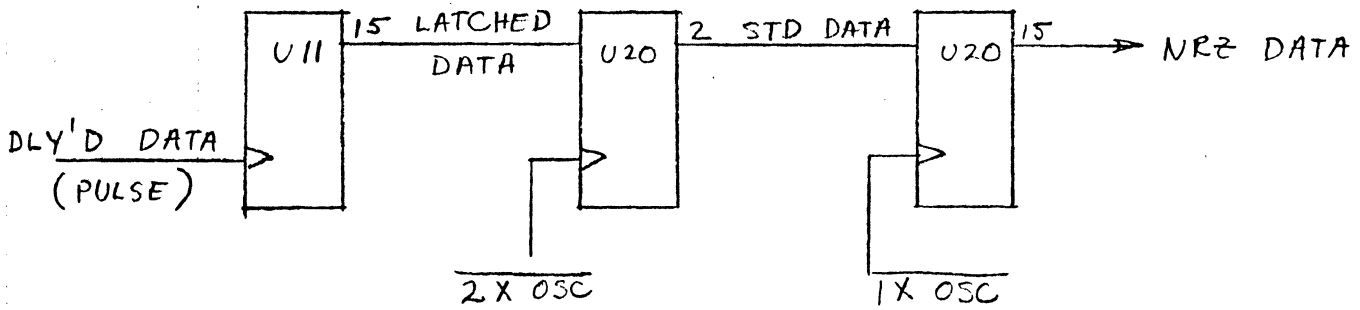
for Voltage Range of -2V to -10V ; mean = -6V

$$V_c = V_{in} - V_{switch} = -6V + 1.45 = 4.55V$$

for 48 MHz : period $= \frac{1}{48 \times 10^6} = 20.6\,nS$



AMCODE
DATA RECOVERY



GENERAL INFORMATION
SECTION I — HIGH-SPEED LOGICS

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high-speed logic is the most direct way to improve system performance and emitter-coupled logic (ECL) is today's fastest form of digital logic. Emitter-coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

MECL PRODUCTS

Motorola introduced the original monolithic emitter-coupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III (MC1600 series), MECL 10,000, MECL 10800, and PLL (MC12000 series) families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1 ns edge speeds and propagation delays along with greater than 500 MHz flip-flop toggle rates, make MECL III useful for high-speed test and communications equipment. Also, this family is used in the high-speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in large high-speed systems showed the need for an easy-to-use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10,000 is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy — MECL 10,000 gates use less than one-half the power of MECL III. Finally, low gate power and advanced circuit design techniques have permitted a new level of complexity for MECL 10,000 circuits. For example, the complexity of the MC10803 Memory Interface Function compares favorably to that of any bipolar integrated circuit on the market.

The basic MECL 10,000 Series has been expanded by a subset of devices with even greater speed. This additional series provides a selection of MECL 10,000 logic functions with flip-flop repetition rates up to 200 MHz min. The MECL 10,200 Series is meant for use in critical timing chains, and for clock distribution circuits. MECL 10,200 parts are otherwise identical to their 10,000 Series counterparts (subtract 100 from the MECL 10,200 part number to obtain the equivalent standard MECL 10,000 part number).

Continuing technical advances led more recently to the development of the M10800 LSI processor family. The M10800 family combines the performance of ECL with the system advantages of LSI density. Architectural features of the M10800 family significantly reduce the component count of a high-performance processor system. The M10800 LSI family is fully compatible with the MECL 10,000 and MECL III logic families for a complete selection of system design components.

MECL FAMILY COMPARISONS

Feature	MECL 10,000			MECL III
	10,100 Series 10,500 Series	10,200 Series 10,600 Series	10,800 LSI*	
1. Gate Propagation Delay	2 ns	1.5 ns	1 – 2.5 ns	1 ns
2. Output Edge Speed	3.5 ns	2.5 ns	3.5 ns	1 ns
3. Flip-Flop Toggle Speed	160 MHz	250 MHz	N.A.	300 – 500 MHz
4. Gate Power	25 mW	26 mW	2.3 mW	60 mW
5. Speed Power Product	50 pJ	37 pJ	4.6 pJ	60 pJ

*Average for Equivalent LSI Gate.

FIGURE 1a – GENERAL CHARACTERISTICS

Ambient Temperature Range	MECL 10,000	M10800	MECL III	PLL
0° to 75°C	MCM10100 Series	–	MC1697P	MC12000 Series
-30°C to +85°C	MC10100 Series MC10200 Series	MC10800 Series	MC1600 Series	MC12000 Series
-55°C to 125°C	MC10500 Series MC10600 Series MCM10500 Series	–	MC1648M	MC12500 Series

FIGURE 1b – OPERATING TEMPERATURE RANGE

Package Style	MECL 10,000	M10800	MECL III	PLL
16-Pin Plastic DIP	MC10100P Series MC10200P Series	–	MC1658P	MC12000P Series
16-Pin Ceramic DIP	MC10100L Series MC10200L Series MC10500L Series MC10600L Series MCM10100L Series MCM10500L Series	MC10804L MC10807L	MC1600L Series	MC12000L Series MC12500L Series
16-Pin Flat Package	MC10500F Series MC10600F Series MCM10500F Series	–	MC1600F Series	MC12513F
20-Pin Ceramic DIP	–	MC10805L	–	–
24-Pin Plastic Package	MC10181P	–	–	–
24-Pin Ceramic DIP	MC10181L, MC10581L	MC10802L	–	–
24-Pin Flat Package	MC10581F	–	–	–
48-Pin Ceramic Quil	–	MC10800L Series	–	–
14-Pin Plastic DIP	–	–	MC1648P	MC12000P MC12002P MC12020P MC12040P
14-Pin Ceramic DIP	–	–	MC1648L	MC12000L MC12002L MC12020L MC12040L
14-Pin Flat Package	–	–	MC1648F	MC12540F
8-Pin Plastic DIP	–	–	MC1697P	–

For package information see page 1-28.

FIGURE 1c – PACKAGE STYLES

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Figure 1 provides the basic parameters of the MECL 10,000, M10800, and MECL III families. But these provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

- **Complementary Outputs** cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

Low Cross-Talk due to low-current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10,000 series). A basic MECL 10,000 gate consumes less than 8 mW in on-chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No "Line Drivers" are listed in MECL families, because *every* device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted-pair transmission lines as long as 1000 feet.

Wire-Wrap Capability is possible with MECL 10,000 and the M10800 LSI family because of the slow rise and fall time characteristic of the circuits.

Open Emitter-Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistors of approximately 50 kΩ permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

Motorola's MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10,000 is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for larger systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers. However, the high bandwidths of MECL 10,000, MECL III, and MC12,000 are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL will continue to grow in the industrial market through complex medical electronic products and high performance process control systems.

MECL 10,000 and MECL III have been accepted within the Federal market for numerous signal processors and navigation systems. Full military temperature range MECL 10,000 is offered in the MC10500 and MC10600 Series, and in the PLL family as the MC12500 Series.

BASIC CONSIDERATIONS FOR HIGH-SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.

2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.

3. The possibility of "crosstalk" between adjacent signal leads is proportionately increased in high-speed systems.

4. Electrical noise generation and pick-up are more detrimental at higher speeds.

In general, these four characteristics are speed- and frequency-dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent "gate delay" is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10,000 Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 2). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low-impedance, emitter-follower outputs of MECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.*

The increased affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10,000, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.*

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.

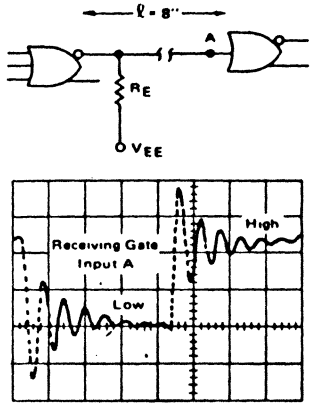


FIGURE 2a – UNTERMINATED TRANSMISSION LINE
(No Ground Plane Used)

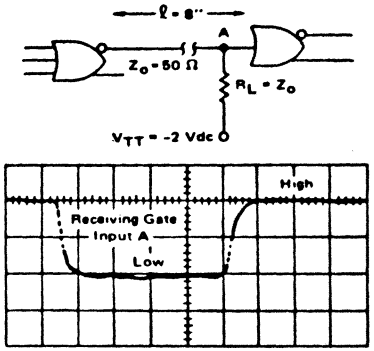


FIGURE 2b – PROPERLY TERMINATED TRANSMISSION LINE
(Ground Plane Added)

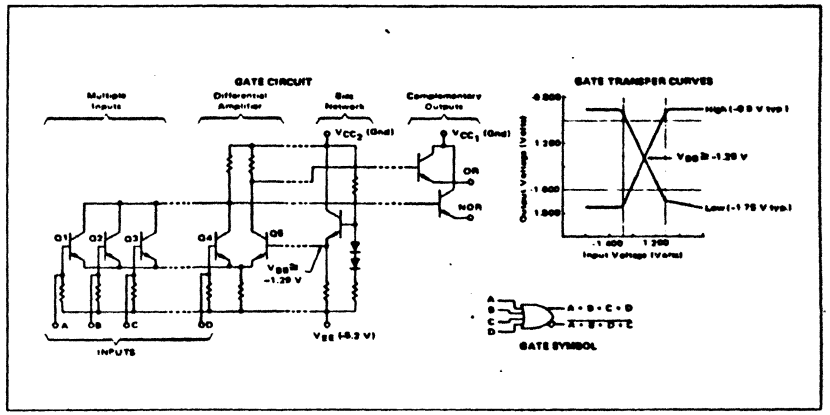


FIGURE 3 – MECL GATE STRUCTURE AND SWITCHING BEHAVIOR

CIRCUIT DESCRIPTION

The typical MECL circuit, Figure 3, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function.

Power-Supply Connections – Any of the power supply levels, V_{TT}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case, $V_{CC} = 0$, $V_{TT} = +2.0$ V, $V_{EE} = -5.2$ V.

System Logic Specifications – The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of $V_{OL} = -1.75$ V to a HIGH state of $V_{OH} = -0.9$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's." Then

"0" = −1.75 V = LOW (typical)

"1" = −0.9 V = HIGH

Circuit Operation – Beginning with all logic inputs LOW (nominal −1.75 V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting. Under these conditions, with the base of Q5 held at −1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or −2.09 V. (The 0.8 V differential is a characteristic of this P-N junction.) The base-to-emitter differential across Q1 – Q4 is then the difference between the common emitter voltage (−2.09 V) and the LOW logic level (−1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the −1.75 V LOW state to the −0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common-emitter point rises from −2.09 V to −1.7 (one diode drop below the −0.9 V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at −1.29 V, the base-emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 – Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 – Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Current:

I_{CC} Total power supply current drawn from the positive supply by a MECL unit under test.

I_{CBO} Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.

I_{CCH} Current drain from V_{CC} power supply with all inputs at logic HIGH level.

I_{CCL} Current drain from V_{CC} power supply with all inputs at logic LOW level.

I_E Total power supply current drawn from a MECL test unit by the negative power supply.

I_F Forward diode current drawn from an input of a saturated logic to MECL translator when that input is at ground potential.

I_{in} Current into the input of the test unit when a maximum logic HIGH ($V_{IH\ max}$) is applied at that input.

$^*I_{INH}$ HIGH level input current into a node with a specified HIGH level ($V_{IH\ max}$) logic voltage applied to that node. (Same as I_{in} for positive logic.)

$^*I_{INL}$ LOW level input current, into a node with a specified LOW level ($V_{IL\ min}$) logic voltage applied to that node.

I_L Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.

$^*I_{OH}$ HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.

$^*I_{OL}$ LOW level output current: the current flowing into the output, at a specified LOW level output voltage.

I_{OS} Output short circuit current.

I_{out} Output current (from a device or circuit, under such conditions mentioned in context).

Current (cont.):

I_R Reverse current drawn from a transistor input of a test unit when V_{EE} is applied at that input.

I_{SC} Short-circuit current drawn from a translator saturating output when that output is at ground potential.

Voltage:

V_{BB} Reference bias supply voltage.

V_{BE} Base-to-emitter voltage drop of a transistor at specified collector and base currents.

V_{CB} Collector-to-base voltage drop of a transistor at specified collector and base currents.

V_{CC} General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).

V_{CC1} Most positive power supply voltage (output devices). (Usually ground for MECL devices.)

V_{CC2} Most positive power supply voltage (current switches and bias driver). (Usually ground for MECL devices.)

V_{EE} Most negative power supply voltage for a circuit (usually −5.2 V for MECL devices).

V_F Input voltage for measuring I_F on TTL interface circuits.

V_{IH} Input logic HIGH voltage level (nominal value).

$^*V_{IH\ max}$ Maximum HIGH level input voltage: The most positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed.

V_{IHA} Input logic HIGH threshold voltage level.

$V_{IHA\ min}$ Minimum input logic HIGH level (threshold) voltage for which performance is specified.

$^*V_{IH\ min}$ Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Input logic LOW voltage level (nominal value).

$^*V_{IL\ max}$ Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{ILA} Input logic LOW threshold voltage level.

$V_{ILA\ max}$ Maximum input logic LOW level (threshold) voltage for which performance is specified.

$^*V_{IL\ min}$ Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{in} Input voltage (to a circuit or device).

V_{max} Maximum (most positive) supply voltage, permitted under a specified set of conditions.

$^*V_{OH}$ Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.

V_{OHA} Output logic HIGH threshold voltage level.

$V_{OHA\ min}$ Minimum output HIGH threshold voltage level for which performance is specified.

$V_{OH\ max}$ Maximum output HIGH or high-level voltage for given inputs.

$V_{OH\ min}$ Minimum output HIGH or high-level voltage for given inputs.

$^*V_{OL}$ Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.

V_{OLA} Output logic LOW threshold voltage level.

$V_{OLA\ max}$ Maximum output LOW threshold voltage level for which performance is specified.

$V_{OL\ max}$ Maximum output LOW level voltage for given inputs.

$V_{OL\ min}$ Minimum output LOW level voltage for given inputs.

V_{TT} Line load-resistor terminating voltage for outputs from a MECL device.

V_{OLS1} Output logic LOW level on MECL 10,000 line receiver devices with all inputs at V_{EE} voltage level.

V_{OLS2} Output logic LOW level on MECL 10,000 line receiver devices with all inputs open.

*JEDEC, EIA, NEMA standard definition

Time Parameters:

t_{+}	Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.
t_{-}	Waveform fall time (HIGH to LOW), 90% to 10%, or 80% to 20%, as specified.
t_r	Same as t_{+}
t_f	Same as t_{-}
t_{+-}	Propagation Delay, see Figure 9.
t_{-+}	Propagation Delay, see Figure 9.
t_{pd}	Propagation delay, input to output from the 50% point of the input waveform at pin x (falling edge noted by – or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by – or rising edge noted by +). (Cf Figure 9.)
$t_{x\pm y\pm}$	
t_{x+}	Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified.
t_{x-}	Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified.
f_{Tog}	Toggle frequency of a flip-flop or counter device.
f_{shift}	Shift rate for a shift register.

Read Mode (Memories)

t_{ACS}	Chip Select Access Time
t_{RCS}	Chip Select Recovery Time
t_{AA}	Address Access Time

Write Mode (Memories)

t_W	Write Pulse Width
t_{WSD}	Data Setup Time Prior to Write
t_{WHD}	Data Hold Time After Write
t_{WSA}	Address setup time prior to write
t_{WHA}	Address hold time after write
t_{WSCS}	Chip select setup time prior to write
t_{WHCS}	Chip select hold time after write
t_{WS}	Write disable time
t_{WR}	Write recovery time

Temperature:

T_{stg}	Maximum temperature at which device may be stored without damage or performance degradation.
T_J	Junction (or die) temperature of an integrated circuit device.
T_A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.
θ_{JA}	Thermal resistance of an IC package, junction to ambient.
θ_{JC}	Thermal resistance of an IC package, junction to case.
lfpm	Linear feet per minute.
θ_{CA}	Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e_g	Signal generator inputs to a test circuit.
TP_{in}	Test point at input of unit under test.
TP_{out}	Test point at output of unit under test.
D.U.T.	Device under test.
C_{in}	Input capacitance.
C_{out}	Output capacitance.
Z_{out}	Output impedance.
$^{*}P_D$	The total dc power applied to a device, not including any power delivered from the device to a load.
R_L	Load Resistance.
R_T	Terminating (load) resistor.
R_p	An input pull-down resistor (i.e., connected to the most negative voltage).
P.U.T.	Pin under test.

*JEDEC, EIA, NEMA standard definition

SECTION II — TECHNICAL DATA

GENERAL CHARACTERISTICS and SPECIFICATIONS

(See pages 1-6 through 1-8 for definitions of symbols and abbreviations.)

In subsequent sections of this Data Book, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOLS AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. The symbols used in this book, and their definitions, are listed on the preceding pages.

MAXIMUM RATINGS

The limit parameters beyond which the life of the devices may be impaired are given in Figure 4a. In addition, Table 4b provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. A typical transfer curve and associated data for all MECL families is shown in Figure 5.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

FIGURE 4a — LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Unit	MECL 10,000	M10800 LSI	MECL III
Characteristic	V_{EE}	Vdc	-8.0 to 0	-8.0 to 0	-8.0 to 0
Supply Voltage (V_{CC} = 0)	V_{TT}	Vdc	–	-4.0 to 0	–
Input Voltage (V_{CC} = 0)	V_{in}	Vdc	0 to V_{EE}	0 to V_{EE}	0 to V_{EE}
Input Voltage Bus (V_{CC} = 0)	V_{in}	Vdc	–	0 to -2.0①	–
Output Source Current Continuous	I_{out}	mAdc	50	50	40
Output Source Current Surge	I_{out}	mAdc	100	100	–
Storage Temperature	T_{stg}	°C	-55 to +150	-55 to +150	-55 to +150
Junction Temperature Ceramic Package②	T_J	°C	165	165	165③
Junction Temperature Plastic Package	T_J	°C	150	–	150

NOTES: ① Input voltage limit is V_{CC} to -2 volts when bus is used as an input and the output drivers are disabled.

② Maximum T_J may be exceeded (< 250°C) for short periods of time (< 240 hours) without significant reduction in device life.

③ Except MC1666 – MC1670 which have maximum junction temperatures = 145°C.

FIGURE 4b – LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristics	Symbol	Unit	MECL 10,000	M10800 LSI	MECL III
Operating Temperature Range Commercial ①	T_A	°C	MC: −30 to +85 MCM: 0 to 75	−30 to +85	−30 to +85
Operating Temperature Range MIL ①	T_A	°C	−55 to +125	–	−55 to +125 (MC1648M)
Supply Voltage (V_{CC} = 0)②	V_{EE}	Vdc	MC: −4.68 to −5.72 MCM: −4.94 to −5.46	−4.68 to −5.72	−4.68 to −5.72
Supply Voltage (V_{CC} = 0)	V_{TT}	Vdc	–	−1.9 to −2.2	–
Output Drive Commercial	–	Ω	50 Ω to −2.0 Vdc	50 Ω to −2.0 Vdc	50 Ω to −2.0 Vdc④
Output Drive MIL	–	Ω	100 Ω to −2.0 Vdc	100 Ω to −2.0 Vdc	–
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	ns	–	10	③

NOTES: ①With airflow ≥ 500 lfpm.
②Functionality only. Data sheet limits are specified for −5.2 V ± 0.010 V.
③10 ns maximum limit for MC1690, MC1697, and MC1699.
④Except MC1648 which has an internal output pulldown resistor.

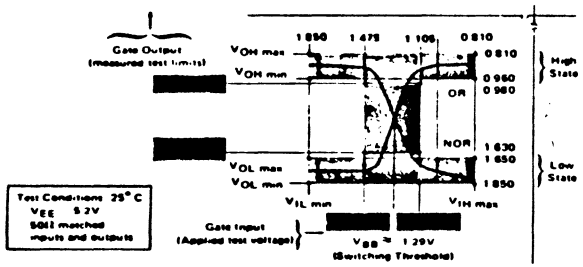


FIGURE 5 – MECL TRANSFER CURVES (MECL 10,000 EXAMPLE) and SPECIFICATION TEST POINTS

The first set is obtained by applying test voltages, $V_{IL\ min}$ and $V_{IH\ max}$ (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between $V_{OL\ max}$ and $V_{OL\ min}$, and V_{OHmax} and V_{OHmin} specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, $V_{ILA\ max}$, is applied to the gate and the NOR and OR outputs are measured to see that they are above the $V_{OHA\ min}$ and below the $V_{OLA\ max}$ levels, respectively. Similar checks are made using the test input voltage $V_{IHA\ min}$.

The result of these specifications insures that:

a) The switching threshold (≈ V_{BB}) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

b) Quiescent logic levels fall in the lightest shaded ranges;

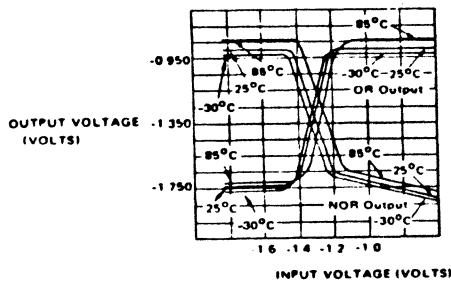
c) Guaranteed noise immunity is met.

Figure 6 shows the guaranteed MECL 10,000 and MECL III logic levels and switching thresholds over specified temperature ranges. As shown in the Figure 6a Typical Transfer Curves, MECL outputs rise with increasing ambient temperature. All circuits in each family have the same worst-case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

All of these specifications assume −5.2 V power supply operation. Operation at other power-supply voltages is possible, but will result in further transfer curve changes. Transfer characteristic data obtained for a variety of supply voltages are shown in Figure 7. The table accompanying these graphs indicates the change rates of output voltages as a function of power supply voltages.

TRANSFER DATA FOR TEMPERATURE VARIATIONS

FIGURE 6a – TYPICAL TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE
(See tables below for data)



Forcing Function	Parameter	−55°C①	−30°C②	0°C③	25°C②	25°C①	75°C③	85°C②	125°C①
		MC10500 MC10600 MCM10500	MC10100 MC10200 MC10800	MCM10100	MC10100 MC10200 MC10800	MC10500 MC10600 MCM10500	MCM10100	MC10100 MC10200 MC10800	MC10500 MC10600 MCM10500
V_{IHmax} =	V_{OHmax}	−0.880	−0.890	−0.840	−0.810	−0.780	−0.720	−0.700	−0.630
	V_{OHmin}	−1.080	−1.060	−1.000	−0.980	−0.930	−0.900	−0.890	−0.825
	V_{OHAmin}	−1.100	−1.080	−1.020	−0.980	−0.950	−0.920	−0.910	−0.845
V_{IHAmin}		−1.255	−1.205	−1.145	−1.105	−1.105	−1.045	−1.035	−1.000
V_{ILAmax}		−1.510	−1.500	−1.490	−1.475	−1.475	−1.450	−1.440	−1.400
	V_{OLAmax}	−1.635	−1.655	−1.645	−1.630	−1.600	−1.605	−1.595	−1.525
	V_{OLmax}	−1.655	−1.675	−1.665	−1.650	−1.620	−1.625	−1.615	−1.545
V_{ILmin} =	V_{OLmin}④	−1.920	−1.890	−1.870	−1.850	−1.850	−1.830	−1.825	−1.820
V_{ILmin}	I_{INLmin}	0.5	0.5	0.5	0.5	0.5	0.3	0.3	0.3

NOTES ①MC10500, MC10600, and MCM10500 series specified driving 100 Ω to −2.0 V.
②MC10100, MC10200, and MC10800 series specified driving 50 Ω to −2.0 V.
③Memories (MCM10100) specified 0–75°C for commercial temperature range, 50 Ω to −2.0 V. Military temperature range memories (MCM10500) specified per Note 1.
④Special circuits such as MC10123, MC10118, MC10119, and MC10800 family bus outputs have lower than normal V_{OLmin}. See individual data sheets for specific values.

Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. V_{EE} = −5.2 V ± 0.010 V.

FIGURE 6b – MECL 10,000 DC TEST PARAMETERS

Forcing Function	Parameter	−30°C	25°C	85°C
V_{IHmax} =	V_{OHmax}	−0.875	−0.810	−0.700
	V_{OHmin}	−1.045	−0.960	−0.890
	V_{OHAmin}	−1.065	−0.980	−0.910
V_{IHAmin}		−1.180	−1.095	−1.025
V_{ILAmax}		−1.515	−1.485	−1.440
	V_{OLAmax}	−1.630	−1.600	−1.585
	V_{OLmax}	−1.680	−1.620	−1.575
V_{ILmin} =	V_{OLmin}	−1.890	−1.850	−1.830
V_{ILmin}	I_{INLmin}	0.5	0.5	0.3

NOTE All outputs loaded 50 Ω to −2.0 Vdc except MC1648 which has an internal output pulldown resistor.

ELECTRICAL CHARACTERISTICS

Each MECL III series device has been designed to meet the dc specification shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. V_{EE} = −5.2 V ± 0.10 V.

FIGURE 6c – MECL III DC TEST PARAMETERS

TRANSFER DATA FOR POWER SUPPLY VARIATIONS

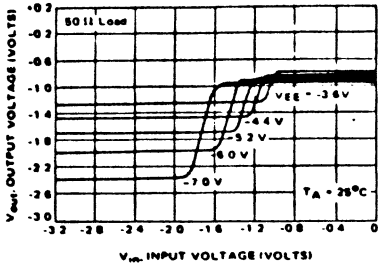


FIGURE 7a – MECL III/10,000 "OR"

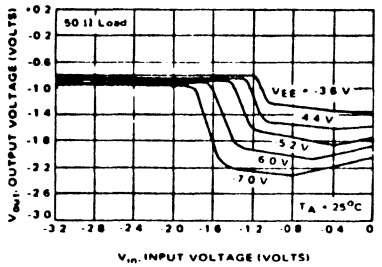
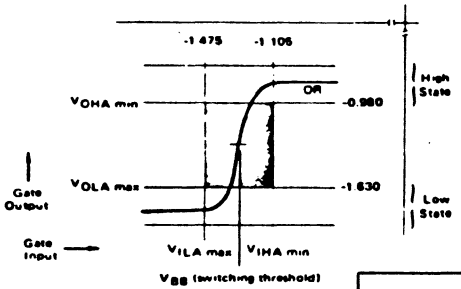


FIGURE 7b – MECL III/10,000 "NOR"

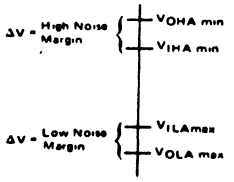
Voltage	MECL 10,000*	MECL III	M10800 LSI
$\Delta V_{OH}/\Delta V_{EE}$	0.016	0.033	0.016
$\Delta V_{OL}/\Delta V_{EE}$	0.250	0.270	0.030
$\Delta V_{BB}/\Delta V_{EE}$	0.148	0.140	0.015

*and subsets: 10,200, 10,500, 10,600.

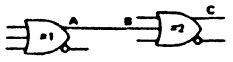
FIGURE 7C – TYPICAL LEVEL CHANGE RATES



Specification Points for Determining Noise Margin



Noise Margin Computations



Family	Guaranteed Worst-Case dc Noise Margin	Typical dc Noise Margin
All MECL 10,000	0.125	0.210
MECL III	0.115	0.200

FIGURE 8 – MECL Noise Margin Data

NOISE MARGIN

"Noise margin" is a measure of a logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript ($V_{OHA\ min}$, $V_{OLA\ max}$, $V_{IHA\ min}$, $V_{ILA\ max}$) in the transfer characteristic curves.

Guaranteed noise margin (NM) is defined as follows:

$$NM_{HIGH\ LEVEL} = V_{OHA\ min} - V_{IHA\ min}$$
$$NM_{LOW\ LEVEL} = V_{ILA\ max} - V_{OLA\ max}$$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 8.

At a gate input (point B) equal to $V_{ILA\ max}$, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst case" condition, since the $V_{OLA\ max}$ specification point guarantees that no device can enter the transition region before an input equal to $V_{ILA\ max}$ is reached. Clearly then, $V_{ILA\ max}$ is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 8 it can be observed that the $V_{OLA\ max}$ specification insures that the LOW state OR output from gate #1 can be no greater than $V_{OLA\ max}$.

Note that $V_{OLA\ max}$ is more negative than $V_{ILA\ max}$. Thus, with $V_{OLA\ max}$ at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of $V_{ILA\ max}$ on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from $V_{OLA\ max}$ to $V_{ILA\ max}$. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10,000 levels shown:

$$NM_{LOW} = V_{ILA\ max} - V_{OLA\ max}$$
$$= -1.475\ V - (-1.630\ V)$$
$$= 155\ mV.$$

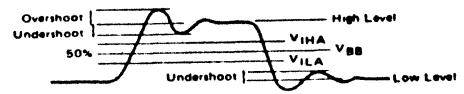
Similarly, for the HIGH state:

$$NM_{HIGH} = V_{OHA\ min} - V_{IHA\ min}$$
$$= -0.980\ V - (-1.105\ V)$$
$$= 125\ mV$$

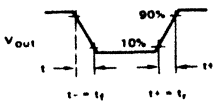
Analogous results are obtained when considering the "NOR" transfer data.

Note that these noise margins are absolute worst case conditions. The lesser of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

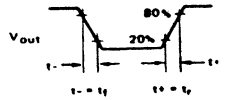
As shown in the table, typical noise margins are usually better than guaranteed – by about 75 mV.



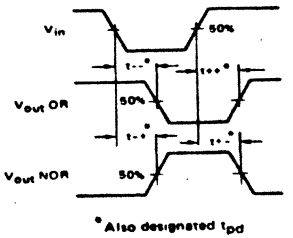
MECL WAVEFORM TERMINOLOGY



MECL III Rise and Fall Times



MECL 10,000 Rise and Fall Times



MECL Propagation Delay

FIGURE 9a – TYPICAL LOGIC WAVEFORMS

Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise-margin specifications, but also other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise-margin specifications. This subject is discussed in greater detail in Application Note AN-592.

AC OR SWITCHING PARAMETERS

Time-dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, or access time, in the case of memories. Since this terminology has varied over the years, and because the "conditions" associated with a particular parameter may differ among logic families, the common MECL waveform and propagation delay terminologies are depicted in Figure 9. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for MECL 10,000 are given in the curves of Figure 10.

SETUP AND HOLD TIMES

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For MECL logic devices, t_{setup} is the minimum time (50% – 50%) before the positive transition of the clock pulse (C) that information must be pres-

FIGURE 9b – MEMORY CHIP SELECT ACCESS TIME WAVEFORM

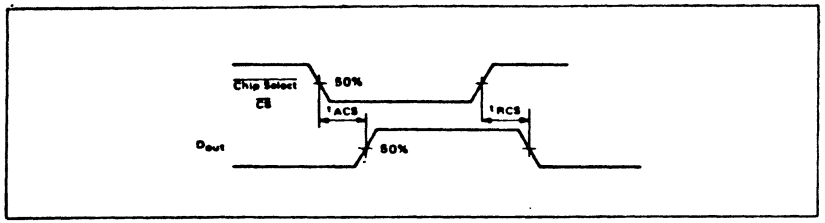
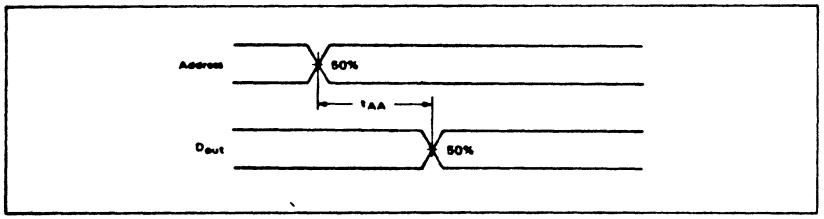


FIGURE 9c – MEMORY ADDRESS ACCESS TIME WAVEFORM



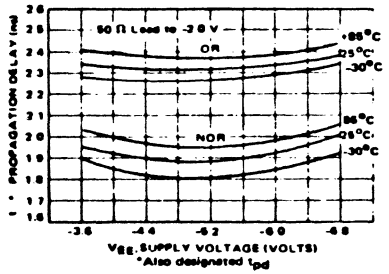


FIGURE 10a – TYPICAL PROPAGATION DELAY t-- versus V_{EE} AND TEMPERATURE (MECL 10,000)

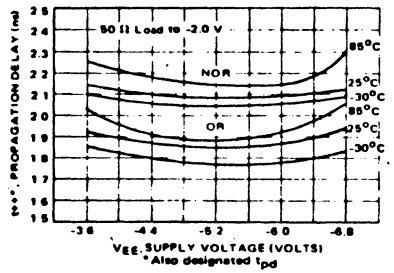


FIGURE 10b – TYPICAL PROPAGATION DELAY t++ versus V_{EE} AND TEMPERATURE (MECL 10,000)

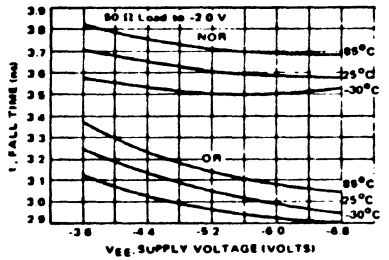


FIGURE 10c – TYPICAL FALL TIME (90% to 10%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10,100)

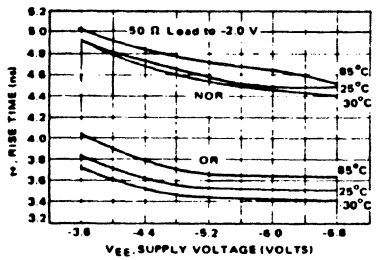


FIGURE 10d – TYPICAL RISE TIME (10% to 90%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10,100)

sent at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 11a.

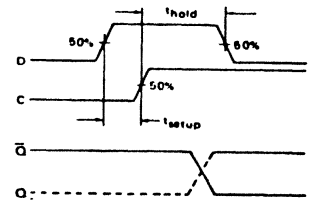


FIGURE 11a – SETUP AND HOLD WAVEFORMS FOR MECL LOGIC DEVICES

For MECL memory devices, t_{setup} is the minimum time before the negative transition of the write enable pulse ($\overline{WE}$) that information must be present at the chip select ($\overline{CS}$), Data (D), and address (A) inputs for proper writing of the selected cell. Similarly t_{hold} is the minimum time after the positive transition of the write enable pulse ($\overline{WE}$) that the information must remain unchanged at the inputs to insure proper writing. Memory setup and hold waveforms are shown in Figure 11b.

In specifying devices, Motorola establishes and guarantees values (shown as minimums on the data sheets) for t_{setup} and t_{hold}. For most MECL circuits, proper device operation typically occurs with the inputs present for somewhat less time than that specified for t_{setup} and t_{hold}.

TESTING MECL 10,000 and MECL III

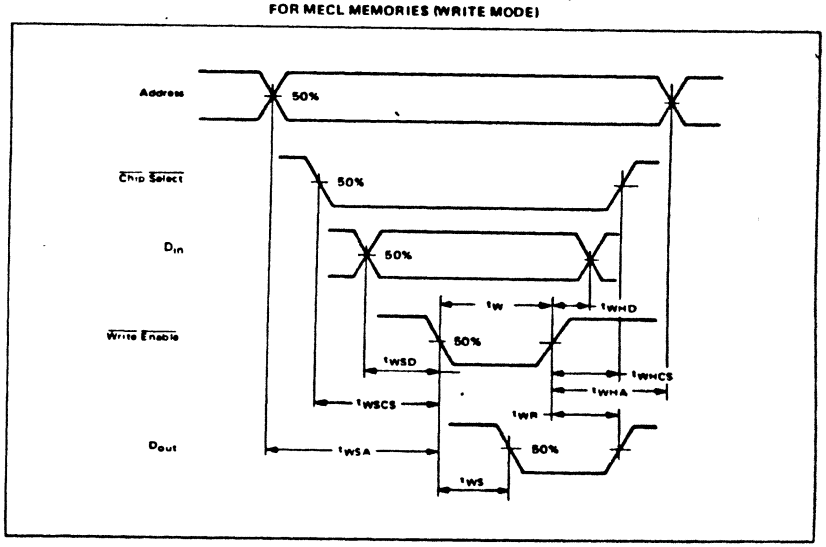
To obtain results correlating with Motorola circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 12a, and a typical memory test circuit in Figure 12b.

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1}, V_{CC2}, and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling scope interface runs directly to the 50-ohm inputs of Channel A and B via 50-ohm coaxial cable. Equal-length coaxial cables must be used between the test set and the A and B scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended.

Interconnect fittings should be 50 ohm GR, BNC, Sealectro Conhex, or equivalent. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin.

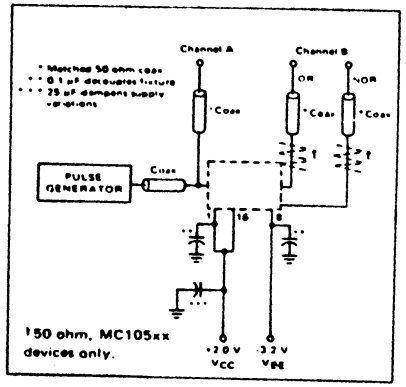
FIGURE 11b – SETUP AND HOLD WAVEFORMS FOR MECL MEMORIES (WRITE MODE)



The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10,000 and 1.5 ns for MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of ≈ ±400 mV about a threshold of ≈+0.7 V when V_{CC} = +2.0 V and V_{EE} = −3.2 V for ac testing of logic devices.

The power supplies are shifted +2.0 V, so that the device under test has only one resistor value to load into – the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Motorola and customer testing. Unused outputs are loaded with a 50-ohm resistor (100-ohm for MIL temp devices) to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25 μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1 μF, as is the V_{EE} pin.

Additional information on testing MECL 10,000 and understanding data sheets is found in Application Notes AN-579 and AN-701.



NOTE: All power supply levels are shown shifted 2 volts positive.

FIGURE 12a – MECL LOGIC SWITCHING TIME TEST SETUP

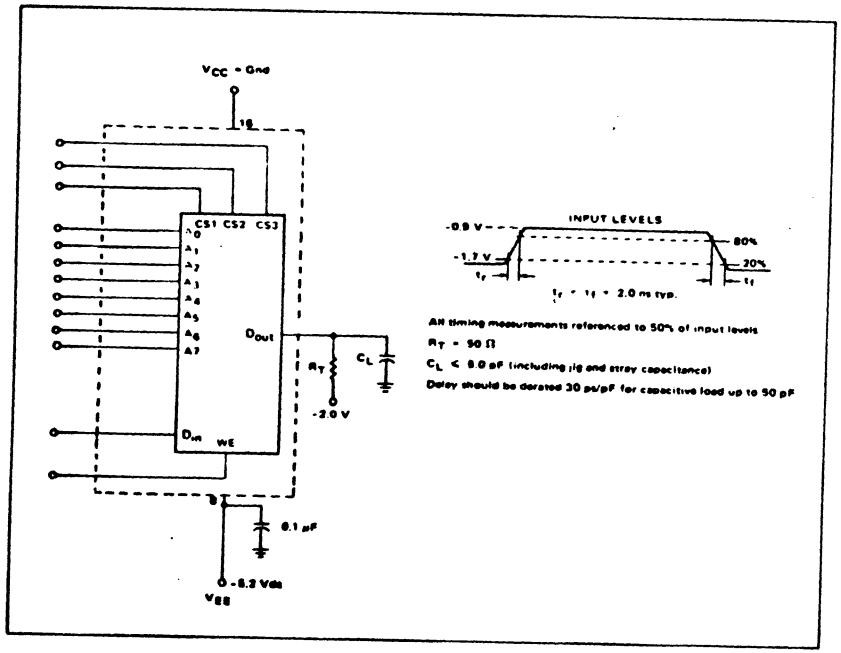


FIGURE 12b – MECL MEMORY SWITCHING TIME TEST CIRCUIT

SECTION III — OPERATIONAL DATA

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at −5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The −5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect.

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF low-inductance capacitor between ground and the −5.2 V line every four to six packages, are recommended.

Most MECL 10,000 and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pull-down resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

The table in Figure 13 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to −2.0 Vdc	5.0	4.3
100 ohms to −2.0 Vdc	7.5	6.5
75 ohms to −2.0 Vdc	10	8.7
50 ohms to −2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

FIGURE 13 – AVERAGE POWER DISSIPATION IN OUTPUT CIRCUIT WITH EXTERNAL TERMINATING RESISTORS

The power dissipation of MECL functional blocks varies with both temperature and V_{EE}. Typical variations are shown in Figure 14. The graph is normalized so that it applies to all MECL lines. The reference temperature is 25°C and the reference power is obtained by multiplying the typical I_E value (total power supply drain current specified on the data sheet) by V_{EE} (5.2 V). For those devices where only the maximum value of I_E is specified on the data sheet, typical power dissipation is approximately 80% of that calculated with the I_E (max) specification.

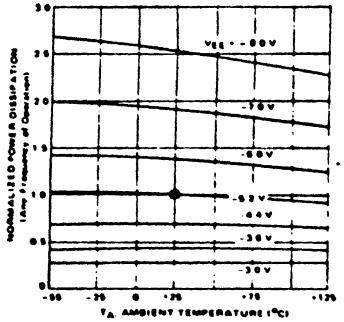


FIGURE 14 – NORMALIZED POWER DISSIPATION versus TEMPERATURE AND SUPPLY VOLTAGE

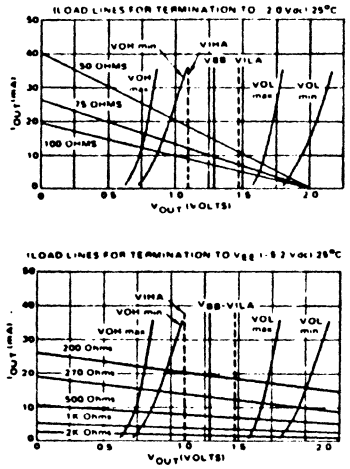


FIGURE 15 – OUTPUT VOLTAGE LEVELS versus DC LOADING

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of load current for MECL III and 10,000 are shown in Figure 15. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

MECL 10,000 and MECL III circuits typically have a 7 ohm output impedance and are relatively unaffected by capacitive loading on a positive-going output signal. However, the negative-going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to -2.0 Vdc or 270 ohms to -5.2 Vdc. A 100 ohm resistor to -2.0 Vdc or 510 ohms to -5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.

Terminated transmission line signal interconnections are used for best MECL 10,000 or MECL III system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1+C_d/C_o}$. Here C_o is the normal intrinsic line capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10,000 transmission line vary with the line impedance. For example, with Z_o = 50 ohms, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when Z_o = 100 ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10,000 gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5 to 7 pF is commonly used in loading calculations.

UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low-signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single-ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs). Input pulldown resistor values are typically 50 kΩ and are not to be used as pulldown resistors for preceding open-emitter outputs.

Several MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE}. Also, several MECL memories do not have input pulldowns on all inputs.

Several MECL circuits do not operate properly when inputs are connected to V_{CC} for a HIGH logic level. Proper design practice is to set a HIGH level as about -0.9 volts below V_{CC} with a resistor divider, a diode drop, or an unused gate output.

SECTION IV — SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit—from the junction region to the ambient environment. The basic formula (s) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\bar{\theta}_{JC} + \bar{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\bar{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).
$\bar{\theta}_{JC}$ = average thermal resistance, junction to case
$\bar{\theta}_{CA}$ = average thermal resistance, case to ambient
$\bar{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) MECL 10,000 devices.

Only two terms on the right side of equation (1) can be varied by the user—the ambient temperature, and the device case-to-ambient thermal resistance, $\bar{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\bar{\theta}_{CA}$ thermal resistance term. $\bar{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\bar{\theta}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Figure 16. In Figure 17, this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life (≥ 100,000 hours).

FIGURE 16 — THERMAL RESISTANCE VALUES FOR STANDARD MECL IC CERAMIC PACKAGES

Package Type (All Using Standard* Mounting) (All Gold Eutectic Die Bond)	THERMAL RESISTANCE IN STILL AIR $\bar{\theta}_{JA}$ (°C/Watt)		$\bar{\theta}_{JC}$ (°C/Watt)	
	Average	Maximum	Average	Maximum
14 Lead Dual In Line 1/4" X 3/4" Alumina Die Area = 4096 Sq Mils	100	130	25	40
14 Lead Flat Pack 1/4" X 1/4" Alumina Die Area 4096 Sq Mils	165	205	40	60
16 Lead Dual In Line 1/4" X 3/4" Alumina Die Area 4096 Sq Mils	100	130	25	40
16 Lead Flat Pack 1/4" X 3/8" Beryllia Die Area = 4096 Sq Mils	86	115	13	20
20 Lead Dual In Line 1/4" X 1" Alumina Die Area = 11,349 Sq Mils	73	95	16	25
24 Lead Dual In Line 1/2" X 1 1/4" Alumina Die Area = 8192 Sq Mils	46	55	10	15
24 Lead Flat Pack 3/8" X 5/8" Beryllia Die Area = 8192 Sq Mils	40	52	6	10
48 Lead Quad In Line (QUIL) 1/2" X 1 1/4" Alumina Die Area = 16,384 Sq Mils	40	52	8	12

*Standard Mounting Methods
Dual In Line: In socket or on PC Board with no contact between bottom of package and socket or PC Board
Flat Pack: Bottom of Package in direct contact with non-metallized area of PC Board.

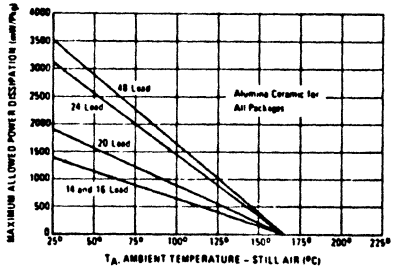


FIGURE 17a — AMBIENT TEMPERATURE DERATING CURVES (CERAMIC DUAL-IN-LINE PKG)

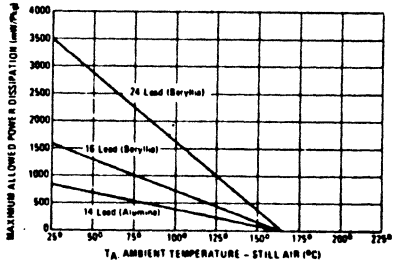


FIGURE 17b — AMBIENT TEMPERATURE DERATING CURVES (CERAMIC FLAT PKG)

AIR FLOW

The effect of air flow over the packages on $\bar{\theta}_{JA}$ (due to a decrease in $\bar{\theta}_{CA}$) is illustrated in the graphs of Figure 18. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual-in-line packaged MECL 10,000 quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 18, $\bar{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$$T_J = P_D(\bar{\theta}_{JA}) + T_A$$

$$T_J = (0.195\ W)(50°C/W + 25°C = 34.8°C$$

Under the above operating conditions, the MECL 10,000 quad gate has its junction elevated above ambient temperature by only 9.8°C.

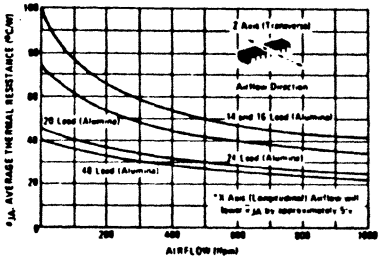


FIGURE 18a — AIRFLOW versus THERMAL RESISTANCE (CERAMIC DUAL-IN-LINE PKG)

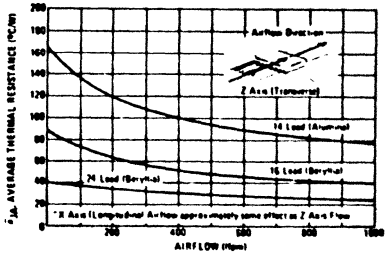


FIGURE 18b — AIRFLOW versus THERMAL RESISTANCE (CERAMIC FLAT PKG)

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

The majority of MECL 10,000, 10800, and MECL III users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last

package is a function of the air flow rate and individual package dissipations. Figure 19 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 lfpm along the Z axis.

FIGURE 19 – THERMAL GRADIENT OF JUNCTION TEMPERATURE (16-Pin MECL Dual In-Line Package)

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10,000, 10800, and MECL III devices are given for an operating temperature range from −30°C to +85°C (0° to +75°C for memories) in Figure 6b and 6c of Section II, TECHNICAL DATA. These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heat sinking (i.e., dual-in-line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non-metallized area of P/C board). Under these conditions, adequate cooling is provided to keep the maximum operating junction temperatures below 145°C for MECL III device types 1666-1670 and below 165°C for all other MECL device types.

The designer may want to use MECL devices under conditions other than those given above. The majority of the low-power device types may be used without air and with higher θ_{JA}. However, the designer must bear in mind that junction temperatures will be higher for higher θ_{JA}, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual-in-line ceramic device operated at θ_{JA} = 100°C/W (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a θ_{JA} = 50°C/W. (Level shift = $\Delta T_J \times 1.4$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heat sinking are intended to provide the designer with sufficent information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEAT SINK SUGGESTIONS

With large high-speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two-sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two-ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 20, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug-in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

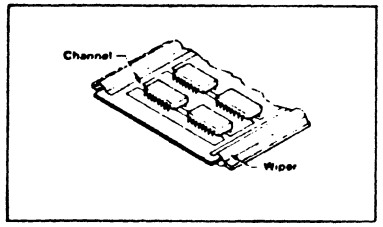


FIGURE 20 – CHANNEL/WIPER HEAT SINKING ON DOUBLE LAYER BOARD

For operating some of the higher power device types* in 16 lead dual-in-line packages in still air, requiring θ_{JA} < 100°C/W, a suitable heat sink is the IERC LIC-214A2WCB shown in Figure 21. This sink reduces the still air θ_{JA} to around 55°C/W. By mounting this heat sink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, θ_{JA} is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for memories) or in lowering TJ for improved reliability.

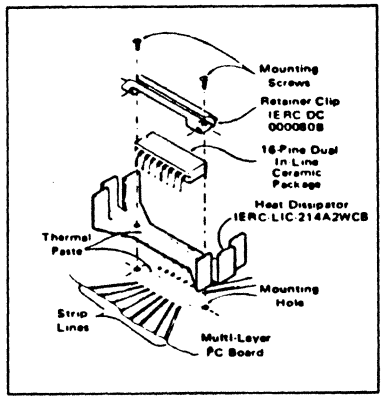


FIGURE 21 – MECL HIGH-POWER DUAL-IN-LINE PACKAGE MOUNTING METHOD

It should be noted that the use of a heat sink on the top surface of the dual-in-line package is not very effective in lowering the θ_{JA}. This is due to the location of the die near the bottom surface of the package.

Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended −5.2 volts and TTL/DTL at +5 V supply, currently available translator circuits, such as the MC10124 and MC10125, may be used.

For systems where a dual supply (−5.2 V and +5 V) is not practical, the MC12000 includes a single supply MECL to TTL and TTL to MECL translator, or a discrete component translator can be designed. For details, see MECL System Design Handbook. Such circuits can easily be made fast enough for any available TTL.

* MC1554, 1678, 1694, 10128, 10129, 10136, 10137, 10177, 10182, and 10804. Max P_D > 800 mW.

MECL also interfaces readily with MOS. With CMOS operating at +5 V, any of the MECL to TTL translators works very well. On the other hand, CMOS will drive MECL directly when using a common −5.2 V supply.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10,000 functions are presently available to interface MECL 10,000 with MOS logic, MOS memories, TTL three-state circuits, and IBM bus logic levels. See Application Note AN-720 for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high-speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10,000 at top circuit speed, when high-density packaging is a requirement, or when transmission line interconnects are used.

Point-to-point back-plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10,000 speeds, this applies to line runs up to 6 inches, and for MECL III up to 1 inch (maximum open wire lengths for less than 100 mV undershoot). But, because of the open-emitter outputs of MECL 10,000 and MECL III circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 22.

Resistor values for the connection in Figure 22a may range from 270 ohms to 2 kΩ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull-down resistors in the range of 50 ohms (100 ohm minimum for MC10,500 and MC10,600 Series parts) to 150 ohms, to −2.0 Vdc, as shown in Figure 22b. Use of a series damping resistor, Figure 22c, will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance. The open emitter-follower outputs of MECL III and MECL 10,000 give the system designer all possible line driving options.

** Limited only by line attenuation and bandwidth characteristics.

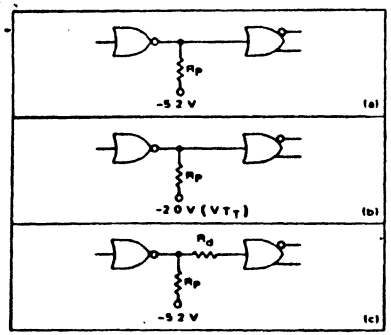


FIGURE 22 – PULL-DOWN RESISTOR TECHNIQUES

One major advantage of MECL over saturated logic is its capability for driving matched-impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The MECL III and MECL 10,000 emitter-follower output transistors will drive a 50-ohm transmission line (100 ohms or greater for MECL 10,500 and MC10,600 Series) terminated to −2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 23a, uses a single resistor whose value is equal to the impedance (Z_0) of the line. A terminating voltage (V_{TT}) of −2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R1 and R2. Figure 23b illustrates this method. The following two equations are used to calculate the values of R1 and R2:

$$R1 = 1.6\ Z_0$$

$$R2 = 2.6\ Z_0$$

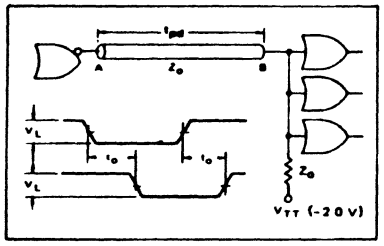


FIGURE 23a – PARALLEL TERMINATED LINE

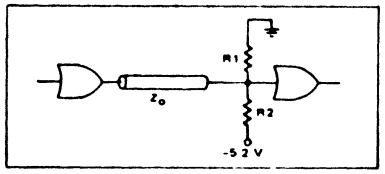


FIGURE 23b – PARALLEL TERMINATION – THEVENIN EQUIVALENT

Another popular approach is the series-terminated transmission line (see Figure 24). This differs from parallel termination in that only one-half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

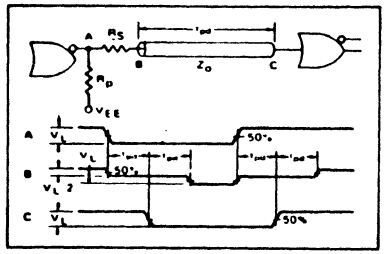


FIGURE 24 – SERIES TERMINATED LINE

To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 24), the reflections in the transmission line will be terminated.

The advantages of series termination include ease of driving multiple series-terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points.

For board-to-board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies. No significant performance degradation occurs for lengths up to 20 feet for MECL III, and up to 50 feet for MECL 10,000.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL III or MECL 10,000 function are connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 25. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common-mode noise rejection of the line receiver ignores common-mode cross talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

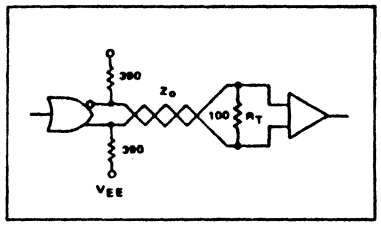


FIGURE 25 – TWISTED PAIR LINE DRIVER/RECEIVER

If timing is critical, parallel signal paths (shown in Figure 26) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wire-wrapped connections can be used with MECL 10,000. For MECL III, the fast edge speeds (1 ns) create a mismatch at the wire-wrap connections which can cause reflections, thus reducing noise immunity. The mismatch occurs also with MECL 10,000, but the distance between the wire-wrap connection and the end of the line is generally short enough so the reflections cause no problem.

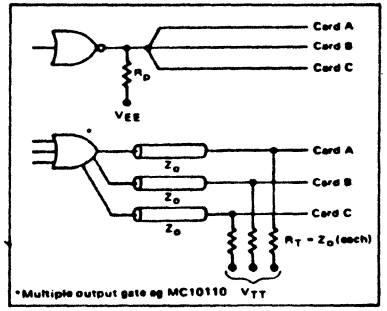


FIGURE 26 – PARALLEL FANOUT TECHNIQUES

Series damping resistors may be used with wire-wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire-wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differentially using a line receiver.

The recommended wire-wrapped circuit cards have a ground plane on one side and a voltage plane on the other, to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire-wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point-to-point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire-wrap boards designed for MECL 10,000 are available from several vendors.

Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 27). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

Stripline is used with multilayer circuit boards as shown in Figure 27. Stripline consists of a constant-width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these lines.

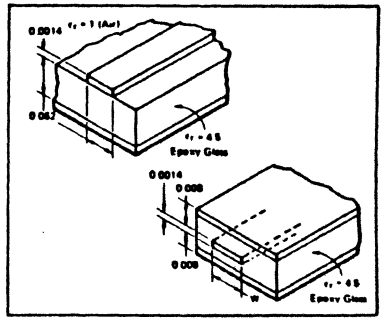


FIGURE 27 – PC INTERCONNECTION LINES FOR USE WITH MECL

CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10,000 speeds, either coaxial cable or twisted pair line (using the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of the application of this technique is shown in Figure 28.

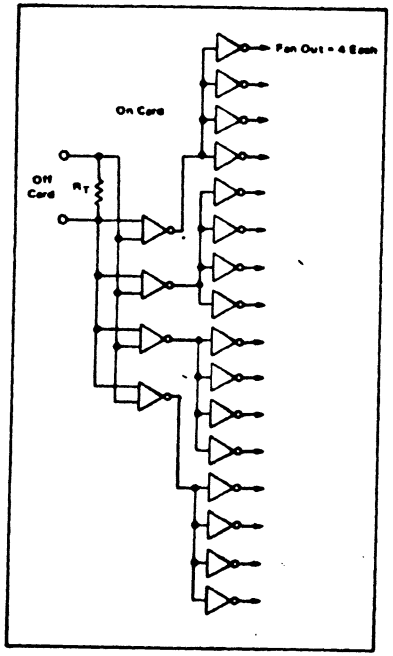


FIGURE 28 – 64 FANOUT CLOCK DISTRIBUTION

Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

A. On-card Synchronous Clock Distribution via Transmission Line

1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.
4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.
5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.
6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.
7. For wire-OR (emitter dotting), two-way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100-ohms impedance. This method should be used when wire-OR connections exceed 1 inch apart on a drive line.

B. Off-Card Clock Distribution

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed-impedance ribbon cable. At the far end of the twisted pair an MC1692 differential line receiver is used. The line should be terminated as shown in Figure 25. This method not only provides high speed, board-to-board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. Wire-OR (can be produced by wiring MECL output emitters together outside packages).
2. Complementary Logic Outputs (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 29.

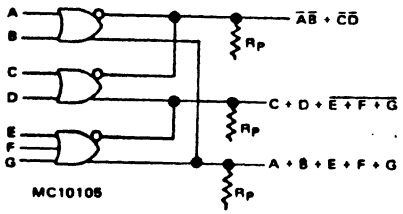


FIGURE 29 – USE OF WIRE-OR AND COMPLEMENTARY OUTPUTS

The connection shown saves several gate circuits over performing the same functions with non-ECL type logic. Also, the logic functions in Figure 29 are all accomplished with one gate propagation delay time for best system speed. Wire-ORing permits direct connections of MECL circuits to busses. (MECL System Design Handbook and Application Note AN-726).

Propagation delay is increased approximately 50 ps per wire-OR connection. In general, wire-OR should be limited to 6 MECL outputs to maintain a proper LOW logic level. The MC10123 is an exception to this rule because it has a special V_{OL} level that allows very high fanout on a bus or wire-OR line. The use of a single output pull-down resistor is recommended per wire-OR, to economize on power dissipation. However, two pull-down resistors per wired-OR can improve fall times and be used for double termination of busses.

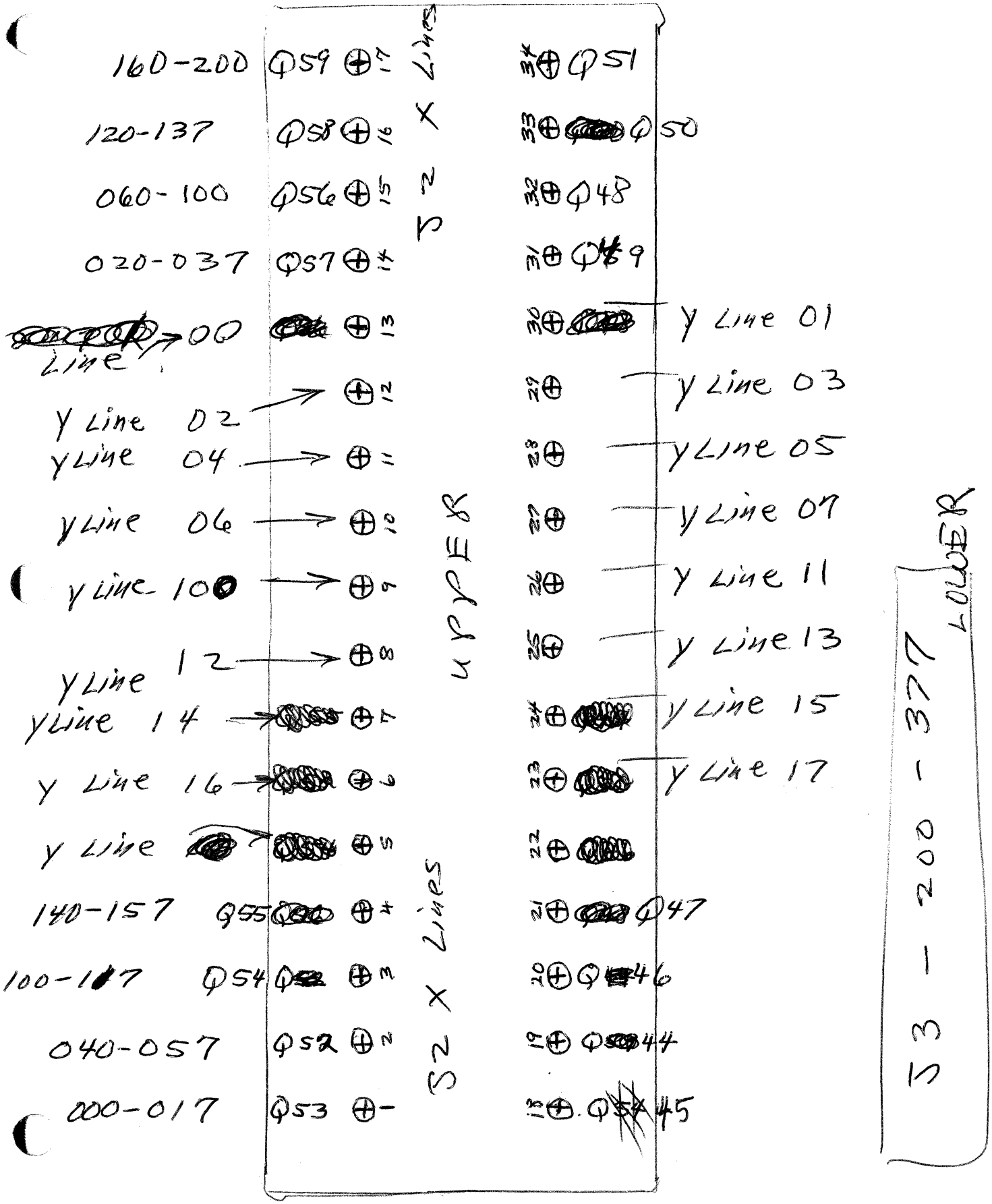
Wire-OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

SYSTEM CONSIDERATIONS – A SUMMARY OF RECOMMENDATIONS

	MECL 10,000	MECL III
Power Supply Regulation	10% or better*	10% or better*
On-Card Temperature Gradient	Less Than 25°C	Less Than 25°C
Maximum Non-Transmission Line Length (No Damping Resistor)	8"	1"
Unused Inputs	Leave Open**	Leave Open**
PC Board	Standard 2-Sided or Multilayer	Multilayer
Special Cooling Requirements	No	No
Bus Connection Capability	Yes (Wire-OR)	Yes (Wire-OR)
MSI/LSI Parts	Yes	Yes (MSI)
Maximum Twisted Pair Length (Differential Drive)	Limited by Cable Response Only, Usually > 1000'	Limited by Cable Response Only, Usually > 1000'
The Ground Plane to Occupy Percent Area of Card	> 50%	> 75%
Wire Wrap may be used	Yes	Not Recommended
Compatible with MECL 10,000	–	Yes

*At the devices.

**Except special functions without input pull-down resistors.


160-200
120-137
060-100
020-037
000-017
140-157
100-117
040-057
Q59
Q58
Q56
Q57
Q55
Q54
Q52
Q53
Q51
Q50
Q48
Q49
Q47
Q46
Q44
Q45
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4
3
2
1
-
34
33
32
31
30
29
28
27
26
25
24
23
22
21
20
19
18
52 X Lines
52 Y Lines
y Line 01
y Line 03
y Line 05
y Line 07
y Line 11
y Line 13
y Line 15
y Line 17
y Line 00
y Line 02
y Line 04
y Line 06
y Line 10
y Line 12
y Line 14
y Line 16
13 - 200 - 377
LOWER

8500 test switches

```
0 ABORTS TEST
1 HALT ON ERROR
2 PRINT CYCLE COUNT
3 LOOP ON TEST
4, 5, 6, SELECT TEST
0 0 0 => TESTS 1 THRU 4
0 0 1 => TEST 1 DISCRETE CONTROLLER TESTS
0 1 0 => TEST 2 DIAGNOSTIC MODE
0 1 1 => TEST 3 SIZE/WRITE PROTECT
1 0 0 => TEST 4 DATA TRANSFER (SECTOR)
1 0 1 => TEST 5 DATA TRANSFER (SUB SECTOR)
1 1 0 => TESTS 1, 2 AND 4
1 1 1 => TESTS 2 AND 4
7 READ ONLY
8 WRITE ONLY
9 INHIBIT DATA ERROR PRINT
10 INHIBIT STATUS ERROR PRINT
11 INHIBIT END OF TEST PRINT
12 TWO READS PER WRITE INHIBIT
13, 14, 15 SELECT DATA PATTERN
 0   0   0 => ALL PATTERNS
 0   0   1 => RANDOM
 0   1   0 => INCREMENTING
 0   1   1 => TRACK/SECTOR ID
 1   0   0 => WORST CASE
 1   0   1 => ONES
 1   1   0 => ZEROES
 1   1   1 => SELECTABLE

SET DATA SWITCHES - CONTINUE
```