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Micro
Devices, Inc.

Am95/6120
Dual-Density
Floppy Disk Controller

User's Manual

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PREFACE

This manual provides general information, an installation and interface guide, and programming information for the Advanced Micro Computer, Am95/6120 Flexible Disk Controller board. Additional information can be obtained from the following documents.

Western Digital Corporation	FD1793 X-01	Data Sheet
	FD1793 X-01	Application Note
Advanced Micro Devices	Am9517	Data Sheet
	Am9517	Application Note
	Am9085	Data Sheet
Shugart Associates	SA800/801	OEM Manual

This manual is intended for use by systems engineering and programming personnel. A minimum of tutorial information is included. Standard abbreviations and acronyms are used in the text.

Both active-high (positive true) and active-low (negative true) signals are discussed. To eliminate confusion and simplify the notation, the following signal convention is used. Whenever a signal is active-low, its mnemonic is followed by an asterisk (*). For example, MEMR* denotes an active-low signal. Active-high signals are denoted without the asterisk.

Hexadecimal numbers are noted in this manual with a starting numeral and a final letter H. For example, 0FF3H or 123H are hexadecimal numbers.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The Am95/6120 Floppy Disk Controller is a high speed board providing the OEM with a powerful and easy-to-use means to interface industry standard 5.25 inch and 8 inch single or double density flexible disk drives to Multibus compatible OEM computers such as the Am95/4000 series MonoBoard and SBC-80 series single board computers.

The 6.75 x 12 inch board includes the Am9085 processor, the FD1793 Floppy Disk Controller, 1K-byte of high speed static RAM buffer, the Am9517A DMA Controller, 3K-byte of E-PROM with firmware, and five mailbox registers.

Am95/6120 features include:

- CONTROLS FOUR DRIVES, 5.25 inch or 8 inch Flexible Disk Drives, Single or Double-sided.

8 inch, single density:	IBM 3740 (FM) Media Format Compatible
8 inch, double density:	IBM System 34 (MFM) Media Format Compatible
5.25 inch single and double density:	Shugart - Recommended Format Compatible

- DISTRIBUTED I/O PROCESSOR ARCHITECTURE. Performs all Disk I/O without host CPU intervention by means of its own dedicated processor, control firmware, and RAM buffer.

- CONTROL FIRMWARE. Provides program code for READ, WRITE, EXECUTE, and INITIALIZE plus several other commands for error checks and status words.

- HIGH THOUGHPUT by means of On-Board DMA Controller, programmable for either block or byte mode transfers. 20-bit addressing allows transfers up to 1M-byte.

- CONFIDENCE CHECK. Automatically provides a diagnostic check on start-up of RAM, ROM, FDC, and DMA. Returns status word to CPU.

- AUTOMATIC SYSTEM BOOT. Provides a selectable system boot capability with the booting routine resident on disk and automatically read into memory on start-up, initialization, and reset.

- VERSATILE INTERFACE. SBC/Multibus† compatible, single or multimaster environment. Operates as an intelligent slave.
- AUTOMATIC CRC GENERATION AND CHECK.
- HEAD UNLOADING. Head unloaded after idle disk rotations to assure long diskette life.

1-2. FUNCTIONAL DESCRIPTION

The Am95/6120 Floppy Disk Controller (FDC) is a microprocessor based disk controller that accepts commands from the host computer via the system bus. These commands are executed by the on-board CPU, allowing the host computer to perform other tasks while the disk controller is busy.

Two modes of operation are available. In polling mode, the Am95/6120 board status register can be read by the host computer at any time. In interrupt mode, up to eight jumper-selectable interrupts are available to signal the computer of the end of an operation.

1-3. DATA TRANSFER

Under control of the Am9085 processor and on-board operating firmware, the FD1793 controller chip selects a particular disk drive, accesses a specific location on that disk and writes onto or reads from that disk. Up to 64 disk sectors can be transferred with a single command. The head is automatically unloaded after 15 idle disk rotations. Automatic track-seek-verify, automatic CRC generation and check, and write protection verification are performed. The floppy disk controller frees the host CPU while it concurrently processes each disk I/O request.

Data transfers are performed in either full buffered mode, burst (buffered) mode or direct mode. In buffered mode, a block of 128 bytes (single density) or 256 bytes (double density) is transferred with a single bus request. Once it gains control of the bus for a full buffered mode data transfer, the controller holds the bus until all the bytes in the block are transferred. If more than one block is to be transferred, the controller generates multiple bus requests (one for each block). In burst mode, each block of data is transmitted in bursts of 64 bytes or 16 bytes, with a bus request for each burst. The controller releases the bus after each burst, and requests the bus for the next burst until the block is transferred. The facility to transfer multiple blocks in burst mode is provided. The firmware performs this operation.

†Multibus is a trademark of Intel Corporation.

A user can specify a data transfer of up to 64 blocks of data with a single user command. For a read operation in buffered mode, a sector of data is transferred from disk to on-board buffer RAM, and then, when the controller has control of the bus, from the buffer RAM to the host system. For a write operation the direction of data transfer is reversed and a block of data is transferred from the host system to the buffer RAM, and then to the disk.

In direct (byte) mode, the data is transferred directly between a disk drive and the host system. A bus request is necessary for each byte transfer. Transfer rates depend on the speed of the host system memory, up to a maximum rate of 30,000 bytes per second in direct mode single density or 60,000 bytes per second double density.

1-4. COMMUNICATIONS

All communications between the host CPU and the Am95/6120 takes place independently through five mailbox registers. These consist of 8-bit registers which have dual access, either from the host system or the on-board CPU, and appear as I/O ports. These are described in figure 1-1.

1-5. DISK DRIVE COMPATIBILITY

The Am95/6120 can drive up to four 5.25 inch or 8 inch flexible disk drives, with single or double sided capability. Compatible disk drives are listed in table 1-1.

CPU PORT#	N	N+1	N+2	N+3 (-IOWC)	N+3 (+IOWC)
8-Bit* Registers	R0	R1	R2	R3	R4
FDC Port#	30H	31H	32H	33H (+Read)	33H (+Write)
	When referencing the FDC, this register is used to specify disk drive disk side, DMA mode, also selects options for 'retries' interrupt signal at EOP, and sector interlacing.	Used to specify starting track when referencing disk... and high address byte (A_{15}-A_8) when referencing Global memory.	Used to specify starting sector when referencing disk... and low address byte (A_7-A_0) when referencing Global memory.	Used to specify commands to floppy disk controller plus amount of data associated with each operation.	Used to report initial confidence test error check and status words.

* Switch Selectable Base Address (N)

Figure 1-1. Mailbox Registers

TABLE 1-1. DRIVE COMPATIBILITY

Drive	1 Sided, 8 Inch Drive	2 Sided, 8 Inch Drive	1 Sided, 5.25 Inch Drive	2 Sided, 5.25 Inch Drive
SHUGART	SA800	SA850	SA400	SA450
SIEMENS	FDD100-8	FDD200-8	FDD100-5	FDD200-5
REMEX	RFD2000	RFD4000	----------	----------
MEMOREX	550	552	----------	----------
PERTEC	----------	FD650	FD200	FD250
MPI	----------	----------	51-S	52-S
TEAC	----------	----------	FD50A	----------
CDC	----------	9406-3	----------	----------
MFE	----------	700	----------	----------

1-6. BUS INTERFACE

The Am95/6120 is compatible with the SBC/Multibus bus standard. It can operate as one master in a multi-master environment. It can generate one of eight jumper-selectable interrupts at the end of each operation.

1-7. FIRMWARE

The 3K E-PROM based firmware controls all the major disk operations. Once a command is initiated by the host CPU, the Am95/6120 Floppy Disk Controller Board operates under its control. The factory-shipped firmware is present in three 2708 EPROMS.

The firmware receives host CPU commands through four I/O ports which the host CPU addresses as N through N+3 (selectable address N). These ports are associated with the four mailbox registers R0 through R3. When the operation requested by a command is completed, a status byte is returned through the fifth mailbox register R4, which appears to the host CPU as port N+3. Port N+3 serves the function as a command register during host CPU write operations and as a status register (to indicate completion of an operation and return any error flags) during a host CPU read operation.

The firmware is initiated by Reset. It initially performs a confidence test on the board ROM, RAM, DMA, and disk controller chip. An LED fault indicator is included on the board, it lights at the start of the confidence test and extinguishes only if all of the tests are passed. A jumper selectable option allows automatic booting at host system initialization without system processor intervention.

1-8. AUTOMATIC BOOT FROM DISK

When the jumper option is installed, the host system automatically boots code stored on disk each time the system is initialized (Reset). The code residing on Track 0, Sector 1 is read from the disk and written into system RAM memory at location 0000. To implement this option, the SID line on the Am9085 CPU is grounded by a jumper. The CPU must be in a Not Ready state (e.g. HOLD signal asserted). This can be accomplished by means of a power-up system-reset jumper. After the boot transfer to RAM memory, the Am95/6120 firmware releases the HOLD to allow the CPU to begin fetching instructions at location 0000.

1-9. PHYSICAL DESCRIPTION

The Am95/6120 board is Multibus compatible with connector P1 serving as the Multibus interface. Connectors P3 and P4 are used to interface up to four minifloppy or standard disk drives. Board dimensions, interface connectors, power requirements, and environmental characteristics are listed in table 1-2.

1-10. SPECIFICATIONS

Table 1-2 lists the board specifications, including physical and electrical parameters, and functional characteristics.

TABLE 1-2. Am95/6120 SPECIFICATIONS

PARAMETERS	CHARACTERISTICS
Recording Media Formatting	a) Flexible diskette, 8 inch diameter, one or two sided: Single Density: IBM 3740 soft sector 77 tracks/side 26 sectors/track 128 bytes/sector FM data format Double Density: Side 0, track 0 formatted in single density, all remaining tracks formatted in double density. IBM System 34 soft sector 77 tracks/side 26 sectors/track 256 bytes/sector MFM data format b) Flexible diskette, 5.25 inch diameter, one or two sided. Single Density: Modified IBM 3740, soft sector 35 tracks/side 18 sectors/track 128 bytes/sector FM data format Double Density: (Side 0, Track 0 is always single density) Modified System 34, soft sector 35 tracks/side 18 sectors/track 256 bytes/sector MFM data format
Backplane Compatibility	Multibus

TABLE 1-2. Am95/6120 SPECIFICATIONS (Cont.)

PARAMETERS	CHARACTERISTICS
Disk Drive Compatibility	Shugart SA800, SA850, SA400, SA450 Memorex 550, 552 Siemens FDD120 CDC 9406-3 Remex Pertec MPI TEAC
Disk Data Rate	8": 4µsec/bit single density, 2µs/bit double density 5/4": 8µsec/bit single density, 4µs/bit double density
Direct Memory Access Maximum Data Rate	200 Kilobytes/second
Physical Characteristics	Height: 17.15 cm (6.75 inches) Width: 30.48 cm (12.00 inches) Depth: 1.57 cm (0.62 inches) Crated Weight: 1.50 kg (3.00 pounds)
Electrical Characteristics	DC power requirements +5 V at 1.65 A typical, 2.80 A max +12 V at 0.11 A typical, 0.14 A max
Environmental Characteristics	Temperature: Operating: 0°C to 55°C Non-Operating: -55°C to +85°C Humidity: Operating: 0 to 90% humidity without condensation Non-Operating: up to 100% without condensation of water or frost
Drive Interface	Refer to table 2-6
Connectors	P1 - 86 pin, 0.156 inch spacing, edge connector P2 - 60 pin, 0.10 inch spacing, edge connector P3 - 34 pin, 0.10 inch spacing, edge connector P4 - 50 pin, 0.10 inch spacing, edge connector

CHAPTER 2
INSTALLATION AND INTERFACE

2-1. INTRODUCTION

This chapter provides instructions for unpacking and preparing the Am95/6120 Board for connection to a microcomputer system. System bus signal characteristics, connector pin assignments and timing information necessary to interface the FDC board to a CPU and Floppy Disk Drives are also included in this chapter.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severly damaged or water-stained, request the carrier's agent to be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection. Shipping damages should be immediately reported to the carrier.

NOTE

Do not attempt to service the board yourself as this will void the warranty.

It is suggested that salvageable shipping cartons and packing materials be saved in case the product must be shipped in the future.

2-3. PRE-INSTALLATION OPTION SELECTION

Before connecting the FDC board to the microcomputer system, switches and jumpers must be set to the desired positions to select the features that are required to customize the board for its intended use. The following paragraphs provide information on switch and jumper selection.

2-4. BOARD SELECT SWITCHES

The AM95/6120 board may be jumpered to respond to a particular 8-bit or 16-bit address. One six-position DIP switch, SW2, positions SW 2-1 through SW 2-6, is used select an 8-bit base address or the low-address byte of a 16-bit base address. One eight-position DIP switch, SW1, positions SW 1-1 through SW 1-8, (when enabled by installing Jumper 9) is used to select the

high-address byte of a 16-bit address. Referring to table 2-1, address bits 2 through 7 correspond to switches SW 2-6 through SW 2-1, respectively. Similarly, bits 8 through 15 correspond to switches SW 1-8 through SW 1-1. Address bus bits 0 and 1 are decoded directly, to select mailbox registers R0 through R4.

TABLE 2-1. BOARD SELECT SWITCH SETTINGS

SWITCH NUMBER	ADDRESS BIT	REGISTER SELECTION				
		R0	R1	R2	I/OWC R3	I/ORC R4
SW1-1*	15 *					
SW1-2*	14 *					
SW1-3*	13 *					
SW1-4*	12 *					
SW1-5*	11 *					
SW1-6*	10 *					
SW1-7*	9 *					
SW1-8*	8 *					
SW2-1	7					
SW2-2	6					
SW2-3	5					
SW2-4	4					
SW2-5	3					
SW2-6	2					
------	1	0	0	1	1	1
------	0	0	1	0	1	1

*16-bit address selection (high-byte), active only when Jumper 9 is installed.

2-5. INTERRUPT SELECTION

An interrupt request, generated on the FDC board, can be jumpered to one of eight system interrupt lines (INT0 - INT7). The selected interrupt request is brought off-board through connector P1. The jumper options are shown in table 2-2.

TABLE 2-2. INTERRUPT JUMPERS

JUMPER	SYSTEM BUS INTERRUPT	J1 CONNECTOR PIN
0	INT0*	41
1	INT1*	42
2	INT2*	39
3	INT3*	40
4	INT4*	37
5	INT5*	38
6	INT6*	35
7	INT7*	36

2-6. POWER-UP HOST RESET

The power up system reset is enabled when Jumper 13 is installed. When enabled, the Am95/6120 asserts a system reset (INIT*) when power is applied. The reset is held active until the on-board Am9085 CPU executes an OUT 49 instruction. Subsequent OUT 49 instructions toggle the system reset (INIT*).

2-7. 16-BIT BOARD SELECT

With Jumper 9 installed, board selection is defined by a 16-bit address. Otherwise, board selection is defined by an 8-bit address. For 16-bit addressing, Multibus address lines ADR0* through ADRF* are decoded. When Jumper 9 is not installed only ADR0* through ADR7* will be decoded.

2-8. AUTOBOOT ON RESET

Jumper 8 controls the state of the Am9085 serial input data (SID) line. If the jumper is installed, the data in drive 0, side 0, track 0, sector 1, is automatically loaded into system memory at address 00000H.

2-9. MEMORY DISABLE

Jumper 14 can be used in conjunction with the Limited Master Mode jumper (10) to disable on-board memory, and instead, access off-board memory when memory addresses 0000H through 0FFFH are specified. Refer to the paragraphs in chapter 3, on Limited Master Mode for a full discussion.

2-10. LIMITED MASTER MODE

When Jumper 10 is installed, the Am95/6120 internal bus controls the system bus. In this mode, the Am95/6120 becomes the exclusive bus master; it cannot co-exist with any other bus master. Refer to the paragraphs in chapter 3 for a full discussion of Limited Master Mode.

2-11. MINIFLOPPY COMPATIBILITY

Installing Jumper 15 and removing U34 from its socket selects 5.25 inch Minifloppy Compatible formatting and timing. Formatting is in accordance with Shugart Associates minifloppy track-formatting specifications. With Jumper 15 installed, write precompensation and phase-lock-loop operation are not used.

2-12. VCO TEST

Jumper 16 is used during maintenance and check-out. When it is installed, the voltage controlled oscillator circuit is allowed to free-run. This allows the free running frequency to be measured and adjusted. Refer to chapter 5 for procedures to adjust the VCO.

2-13. 9085 NOT READY

When Jumper 12 is installed, the AM9085 CPU is held in a not-ready state. This jumper is used during maintenance and check-out to control Am9085 activity.

2-14. HEAD STEPPING RATE

Jumpers 15 and 17 control the head stepping rate, to accomodate various 8 inch and 5-1/4 inch drives. When a drive capable of a different head stepping rate than 10 ms. is being used, (e.g. Shugart double sided floppy drive), the controller will support it with a jumper change as shown in the following table.

HEAD STEPPING RATES

RATE	JUMPER 15	JUMPER 17	USED ON DRIVE TYPE
3 ms		x	Fast 8
10 ms			Standard 8
12 ms	x	x	Fast 5-1/4
30 ms	x		Standard 5-1/4

2-15. SYSTEM INTERRUPT SELECTION

A single jumper, installed in one of the eight jumper locations, 0 through 7, selects the desired system-bus interrupt line.

0	INT0*
1	INT1*
2	INT2*
3	INT3*
4	INT4*
5	INT5*
6	INT6*
7	INT7*

2-16. INSTALLATION

Following the board configuration with the on-board switches and jumpers, the board can be inserted into system backplane, the floppy disk drive cables connected, and power applied. If the board fails to operate, notify Advanced Micro Computer Service Manager.

NOTE

Do not return the board to AMC under any circumstances without an approved return material authorization number (RMA), which will be provided by the Service Manager.

2-17. SYSTEM INTERFACE

The Am95/6120 connects to the system backplane through connector P1. The 8 inch disk drives are connected through P4 while 5.25 inch disk drives are connected through P3. See figure 5-1.

2-18. BUS INTERFACE

Connector P1 is an 86 pin double-sided edge connector that interfaces the FDC board to other system components through the system backplane. Multibus pin assignment for connector P1 are listed in table 2-3.

2-19. ADDRESS (ADR0* THROUGH ADR13*)

The 20-bit address from the system bus is used by the on-board DMA to access up to 1 megabyte of memory ADR0* is the least significant address bit. Address bits 2 through 7 (ADR2* - ADR7*) are compared with the board address select switches; only an address that matches the selected switch settings is recognized by the FDC board. Address bits 0 and 1 are used to access various on-board register locations for externally-generated I/O read/write operations.

TABLE 2-3. SYSTEM BUS CONNECTOR P1 PIN ASSIGNMENTS

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5 V	+5 Vdc	4	+5	+5 Vdc
	5	+5 V	+5 Vdc	6	+5	+5 Vdc
	7	+12 V	+12 Vdc	8	+12	+12 Vdc
	9	-5	-5 Vdc	10	-5	Not Used
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK*	Bus Clock	14	INT*	Initialize
	15	BPRN*	Bus Priority In	16	BPRO*	Bus Priority
	17	BUSY*	Bus Busy	18	BREQ*	Bus Request
	19	MRDC*	Mem Read Command	20	MWTC*	Mem Write Command
	21	IORC*	I/O Read Command	22	IOWC*	I/O Write Command
	23	XACK*	XFER Acknowledge	24	INH1*	Inhibit 1 (RAM)
INTERRUPTS	25		Not Used	26	INH2*	Inhibit 2 (ROM)
	27	BHEN*	Not Used	28	ADR10*	
	29	CBRQ*	Common Bus Request	30	ADR11*	Address Bus
	31	CCLK*	Not Used	32	ADR12*	
	33	INTA*	Interrupt Acknowledge	34	ADR13*	
	35	INT6*		36	INT7*	
	37	INT4*	Parallel Interrupt	38	INT5*	Parallel Interrupt
	39	INT2*	Requests	40	INT3*	Requests
	41	INT0*		42	INT1*	
ADDRESSES	43	ADRE*		44	ADRF*	
	45	ADRC*		46	ADRD*	
	47	ADRA*		48	ADRB*	
	49	ADR8*	Address Bus	50	ADR9*	Address Bus
	51	ADR6*		52	ADR7*	
	53	ADR4*		54	ADR5*	
	55	ADR2*		56	ADR3*	
	57	ADR0*		58	ADR1*	
DATA	59	DATE*		60	DATF*	
	61	DATC*		62	DATD*	
	63	DATA*	Data Bus	64	DATB*	Data Bus
	65	DAT8*		66	DAT9*	
	67	DAT6*		68	DAT7*	
	69	DAT4*		70	DAT5*	
	71	DAT2*		72	DAT3*	
	73	DAT0*		74	DAT1*	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77	-----	----------	78	--------	----------
	79	-12	-12 Vdc	80	-12 V	-12 Vdc
	81	+5	+5 Vdc	82	+5	+5 Vdc
	83	+5	+5 Vdc	84	+5 V	+5 Vdc
	85	GND	Signal GND	86	GND	Signal GND

2-20. DATA (DAT0* THROUGH DATF*)

Sixteen bidirectional data lines are used to transmit or receive information between the FDC and an external (host) system. These lines are driven by the master on write operations and by the addressed slave (memory or I/O) on read operations. The system bus can handle both 8 or 16 bit data transfers. Only bits DAT0* through DAT7* are used when executing eight-bit transfers (DAT0* is the least significant bit).

2-21. INTERRUPT REQUEST LINES (INT0* THROUGH INT7*)

These eight lines are used to connect jumper-selectable interrupts to the data bus. The on-board Am9085 generated interrupt can be connected to any of the eight interrupt request inputs. INT0* is the highest priority interrupt and INT7* is the lowest priority.

2-22. INITIALIZATION (INIT*)

This signal from the system bus resets the board to a known internal state.

2-23. INPUT/OUTPUT READ COMMAND (IORC*)

The IORC* signal is used for I/O input control. The I/O port address is on the system address bus. IORC*, along with a port address recognized by the FDC, is a request to read data from the addressed FDC register.

2-24. INPUT/OUTPUT WRITE COMMAND (IOWC*)

The IOWC* signal indicates that an I/O port address is on the system bus address lines. The address and data must be stable on the system bus 50ns prior to activation of the write command.

2-25. MEMORY READ COMMAND (MRDC*)

The MRDC* signal performs in the same manner as the IORC* signal except that a memory address is on the address bus instead of an I/O port address. MRDC* is generated by the FDC to read data from main (host) memory.

2-26. MEMORY WRITE COMMAND (MWTC*)

The MWTC* signal performs in the same manner as the IOWC* signal except that a memory address is on the address bus instead of an I/O port address. MWTC* is generated by the FDC to write data into the main (host) memory.

2-27. TRANSFER ACKNOWLEDGE (XACK*)

This signal is sent to the FDC from the system bus indicating that the specified read or write operation has been completed and that data has been placed onto, or accepted from, the system bus data lines.

2-28. FLOPPY DISK DRIVE INTERFACE

Connector P3 is a 34 pin double-sided edge connector that interfaces the FDC board to the 5.25 inch, minifloppy drives. Connector P4 is a 50 pin double-sided edge connector that interfaces the FDC board to the 8 inch floppy drives. Because of data format and precompensation requirements, only minifloppy drives or standard drives can be connected at a time.

Multiple floppy disk drives are connected together through a 50 pin flat cable to P4, or through a 34 pin flat cable to P3, in daisy chain fashion. Pin assignments for P3 are listed in table 2-4, pin assignment for P4 are listed in table 2-5. More detailed signal descriptions are found in the Shugart Associates SA800/801 OEM manual. The last drive connected to the string must have a terminator installed.

2-29. Track Greater than 43

The TG43* signal is associated with standard floppy operation. When active, it indicates to the disk drive that the read/write head of the selected drive is positioned between tracks 44 and 76. This signal can only be active during a read or write command.

2-30. Write Protect*

When a write command is issued by the FDC, the write protect signal is sampled by the FD1793 Floppy Disk Formatter/Controller. If a logic low is present, the write command is terminated immediately and the write protect status bit is set.

TABLE 2-4. P3 CONNECTOR PIN ASSIGNMENT

COMPONENT SIDE		CIRCUIT SIDE	
PIN	SIGNAL NAME	PIN	SIGNAL NAME
2	----------	1	GROUND
4	----------	3	GROUND
6	DS04*	5	GROUND
8	INDEX*	7	GROUND
10	DS01*	9	GROUND
12	DS02*	11	GROUND
14	DS03*	13	GROUND
16	MOTOR ON*	15	GROUND
18	DIRECTION*	17	GROUND
20	STEP*	19	GROUND
22	WRITE DATA*	21	GROUND
24	WRITE GATE*	23	GROUND
26	TRACK ZERO*	25	GROUND
28	WRITE PROTECT*	27	GROUND
30	READ DATA*	29	GROUND
32	SIDE SELECT*	31	GROUND
34	----------	33	GROUND

2-31. Track Zero*

When active (logic low), the TR00* signal from the disk drive indicates the read/write head is positioned at track 00.

2-32. Index Pulse*

The index pulse is a 10usec logic low pulse which indicates to the FDC that the selected disk drive read/write head has sensed the index hole on the diskette.

2-33. Ready*

The READY* signal is only used with the 8 inch floppy disk drives. This signal from the selected drive indicates its ready status and is examined prior to initiating a read or write command by the FD1793. If READY* is active, the read or write command is initiated. Otherwise the operation is not initiated and an interrupt is generated. A seek operation can be performed regardless of the ready signal condition.

TABLE 2-5. P4 CONNECTOR PIN ASSIGNMENT

COMPONENT SIDE		CIRCUIT SIDE	
PIN	SIGNAL NAME	PIN	SIGNAL NAME
2	TG 43*	1	GROUND
4	----------	3	GROUND
6	----------	5	GROUND
8	----------	7	GROUND
10	TWO SIDED*	9	GROUND
12	----------	11	GROUND
14	SIDE SELECT*	13	GROUND
16	IN USE*	15	GROUND
18	HEAD LOAD*	17	GROUND
20	INDEX*	19	GROUND
22	READY*	21	GROUND
24	----------	23	GROUND
26	DS01*	25	GROUND
28	DS02*	27	GROUND
30	DS03*	29	GROUND
32	DS04*	31	GROUND
34	DIRECTION*	33	GROUND
36	STEP*	35	GROUND
38	WRITE DATA*	37	GROUND
40	WRITE GATE*	39	GROUND
42	TRACK DATA*	41	GROUND
44	WRITE PROTECT*	43	GROUND
46	READ DATA*	45	GROUND
48	----------	47	GROUND
50	----------	49	GROUND

2-34. Write Gate*

The write gate signal, from the FDC board to the disk drive, is active when a write operation is performed.

2-35. Write Data*

The write data stream is a serial train of data and clock pulses. Pulse width is listed in table 2-6.

2-36. Direction (DIRC)

The direction signal is either a logic high or low and indicates to the disk drive the direction the heads must move when the step signal

activates. A logic-high at P4-34 (and P3-18) (DIR) causes the head to move out (toward track 00), and a logic low causes the head to move in (toward track 76).

2-37. Step* (STEP*)

The step signal is described in table 2-6, and causes the disk drive heads to move one track in or out (depending on the state of the DIRC signal). (See table 2-6 for timing.)

2-38. Two Sided*

When active, this signal indicates that a double-sided drive is in use.

2-39. Read Data*

Raw data (clock and data together) from the diskette come to the FDC board via the READ DATA* line and are processed by the on-board data separator where the clock and data pulses are separated and gated to the FD1793.

TABLE 2-6. DRIVE INTERFACE SPECIFICATION

	8 INCH S.D.	8 INCH D.D.	5.25 INCH S.D.	5.25 INCH D.D.
Head Load Time, Maximum	40ms	40ms	40ms	40ms
Time/Step, Minimum	3ms	3ms	12ms	12ms
Step Pulse Width, Minimum	2us	2us	4us	4us
Write Data Pulse Width	450-550ns	150-250ns	900ns-1100ns	300ns-500ns
Read Data Pulse Width, Minimum	150ns	150ns	150ns	150ns
Write Precompensation	+200ns ON TRACKS >43	+200ns ON TRACKS >43	NONE	NONE

2-40. Drive Select* (DS01*-DS04*).

Four drive select lines (DS01* - DS04*) go from the FDC board to the disk drives to select a specific drive. Only one of these lines is active (low) at a time. Each drive must be address programmed to a location 1 through 4.

2-41. Side One*

An active (low) logic level on the side select line selects the read/write head on the side 1 surface of the diskette. An inactive (high) logic level selects side 0.

2-42. In Use/Motor ON*

When active (low), this line is used by minifloppy (5.25 inch) disk drives to turn off the motor when not in use to extend its life, or by a standard drive to signal its use by lighting the LED indicator (requires jumpers).

When used to control the spindle motor of minifloppy drives, the motor can be turned off when no activity is required, for example, after 10 idle disk rotations. The motor must be turned on at least one second before performing a read or write operation.

When used in the signal mode, an activity indicator can be turned on to show the in-use operating status. This requires installation of special jumpers in the disk drive. Refer to the appropriate disk drive manual.

2-43. Head Load*

When active (low), this signal loads the read/write head against the diskette. This operation may require installation of special jumpers in the disk drive. Refer to the appropriate disk drive manual.

2-44. Floppy Disk Interface Characteristics

The AC timing characteristics are listed in table 2-6.

CHAPTER 3
OPERATION AND PROGRAMMING

3-1. INTRODUCTION

The Am95/6120 contains 3K bytes of on-board firmware to program all major disk operations. The firmware receives host CPU commands through four ports and registers referred to as mailbox registers R0 through R3. Once a command is initiated by the host CPU, the Am95/6120 Intelligent Floppy Disk Controller operates without further host CPU intervention until the operation is complete. Each operation is terminated by a return-of-status byte through a fifth register R4, which indicates completion of the requested command. In the case of operational errors, R4 also stores appropriate error flags. Detailed error checking is provided by two commands.

3-2. BOARD CONFIGURATION

Each Am95/6120 FDC board must be configured for use in a specific system. When shipped, the board is configured for AmSYS8/8. If the configuration is incorrect for your system, the jumpers must be changed and the board address select switches must be set. Chapter 2 discusses jumper selection and address switch settings.

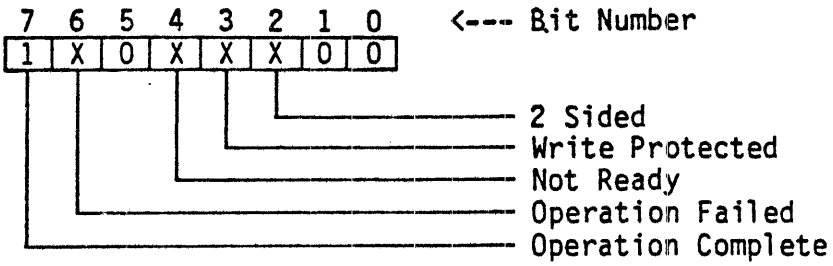
3-3. FIRMWARE DESCRIPTION

The Am95/6120 Floppy Disk Controller firmware resides in 3K bytes of E-PROM. A firmware listing is available in publication number 0680153.

The firmware consists of program routines for the on-board Am9085A CPU. These routines interrogate the mail box registers, set-up operating parameters, evaluate and implement commands, exercise the FD1793 Floppy Disk Formatter/Controller and the Am9517A Multi-Mode DMA controller, determine and report error conditions, and perform other Floppy Disk Controller board operations.

On power up or when the reset signal is asserted on the system bus, the firmware initially performs a confidence test on the board ROM, RAM, DMA, and 1793 FDC. An on-board LED fault indicator lights at the start of the confidence test and turns off after approximately one-quarter second if all four test pass.

Following successful completion of the confidence test, the firmware performs an idle-loop, waiting for the host to issue a command and the on-board command flag to set. The command flag is set when a command is transferred from the host CPU into the command register (R3).



3-24. SPECIAL EXECUTE COMMAND

This command allows access to firmware routines. It can transfer from 64 to 640 bytes of Am9085 code from an area in host memory to the on-board RAM, starting at address 0D80H, and then begin execution at this same address. Transfers are made in 64 byte blocks; 10 blocks comprise 640 bytes. User code must be assembled to execute, starting at address 0D80H.

Call Sequence:
- R0 MSB of 20-bit address
- R1 NSB of 20-bit address
- R2 LSB of 20-bit address
- R3 Command code and block count (CX)

Processing: One through 10 blocks of 64 bytes of program data are transferred from the host memory to on-board RAM and executed. The starting address of RAM in 0D80H and ends at 0FFFH, providing an area of 640 bytes.

The firmware passes control to the externally provided routine through a subroutine call. The user routine must pass control back to the firmware through a RET instruction. The program stack, on entry to the user routine, is 20 bytes in length and empty. It must be empty on return to the firmware. The user program must provide any status response (R4) required by the host system.

Upon return to firmware control, a Board Reset Command is performed. This is equivalent to a power-ON reset initially performed when power is first turned on.

Return: If desired, a return code can be provided by user code. If the RET instruction is used to return to the firmware, the returned status byte is the Power-On/Reset status byte.

3-25. PROGRAMMING APPLICATIONS

The following information consists of Am95/6120 functional descriptions related directly to user programming applications. Several user applications are described at functional step level.

3-26. POWER-ON/RESET

A power-on reset is automatically performed when power is initially applied to the Am95/6120 board following a return from executing user code initiated with the Special Execute command or with a Board Reset command.

A series of tests are performed. The status byte (R4) returns the results of the tests. The flowchart illustrated in figure 3-8, shows the power-up sequence.

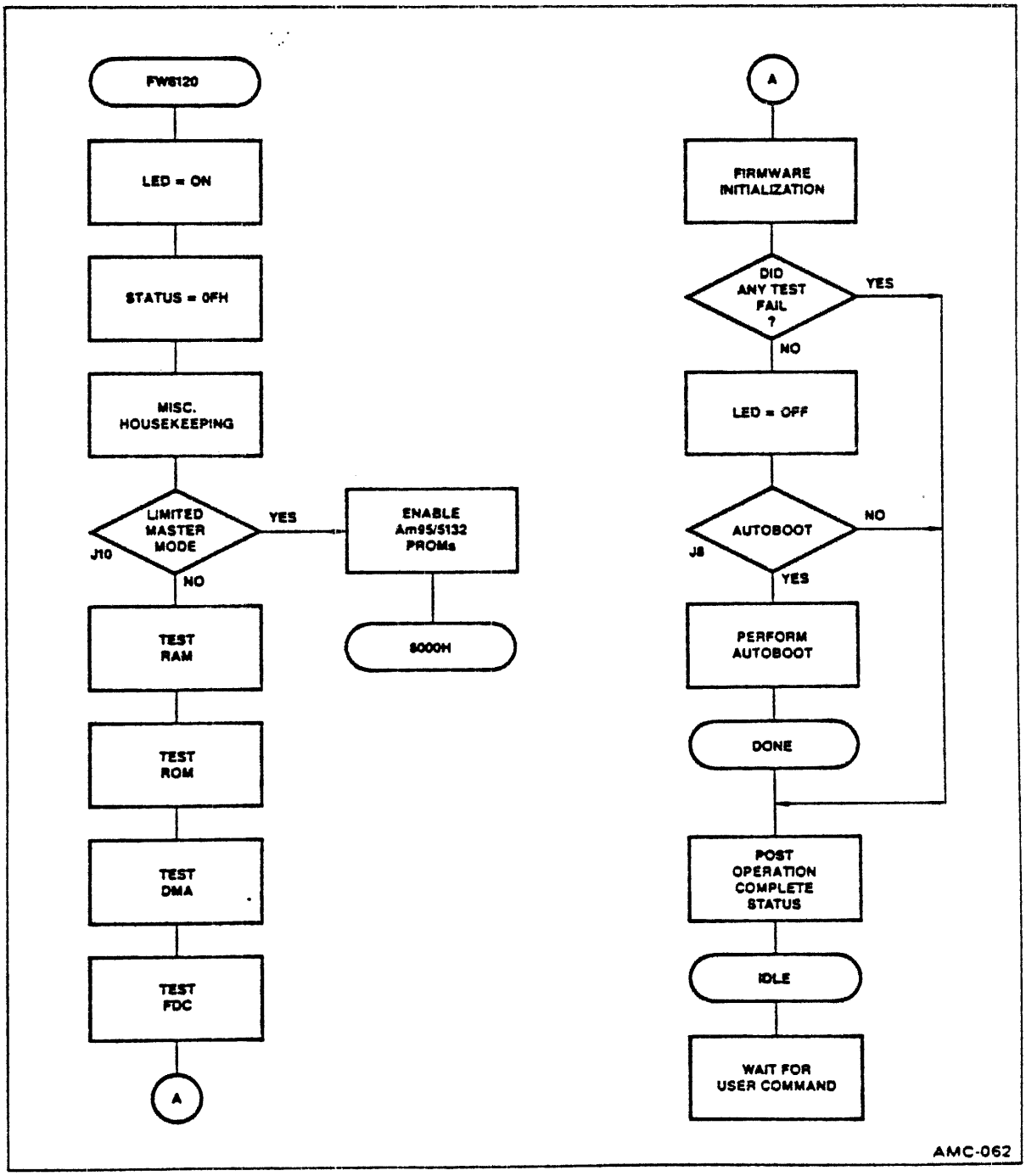


Figure 3-8. Power-On/Reset Sequence

As each test is successfully performed, the corresponding bit in the Status byte is turned off. If all tests pass, the LED will be turned off. If the IPL tests fail, bit 7 is set and the IDLE routine is executed. If IPL completes successfully, the Status byte has a value of 0 and a check is made to determine if the autoboot jumper is installed. If it is, the autoboot routine is performed and any errors will be reported as an operation-failed Status byte (bit 6 set). The value of the Status byte for each of the operations is shown in figure 3-9.

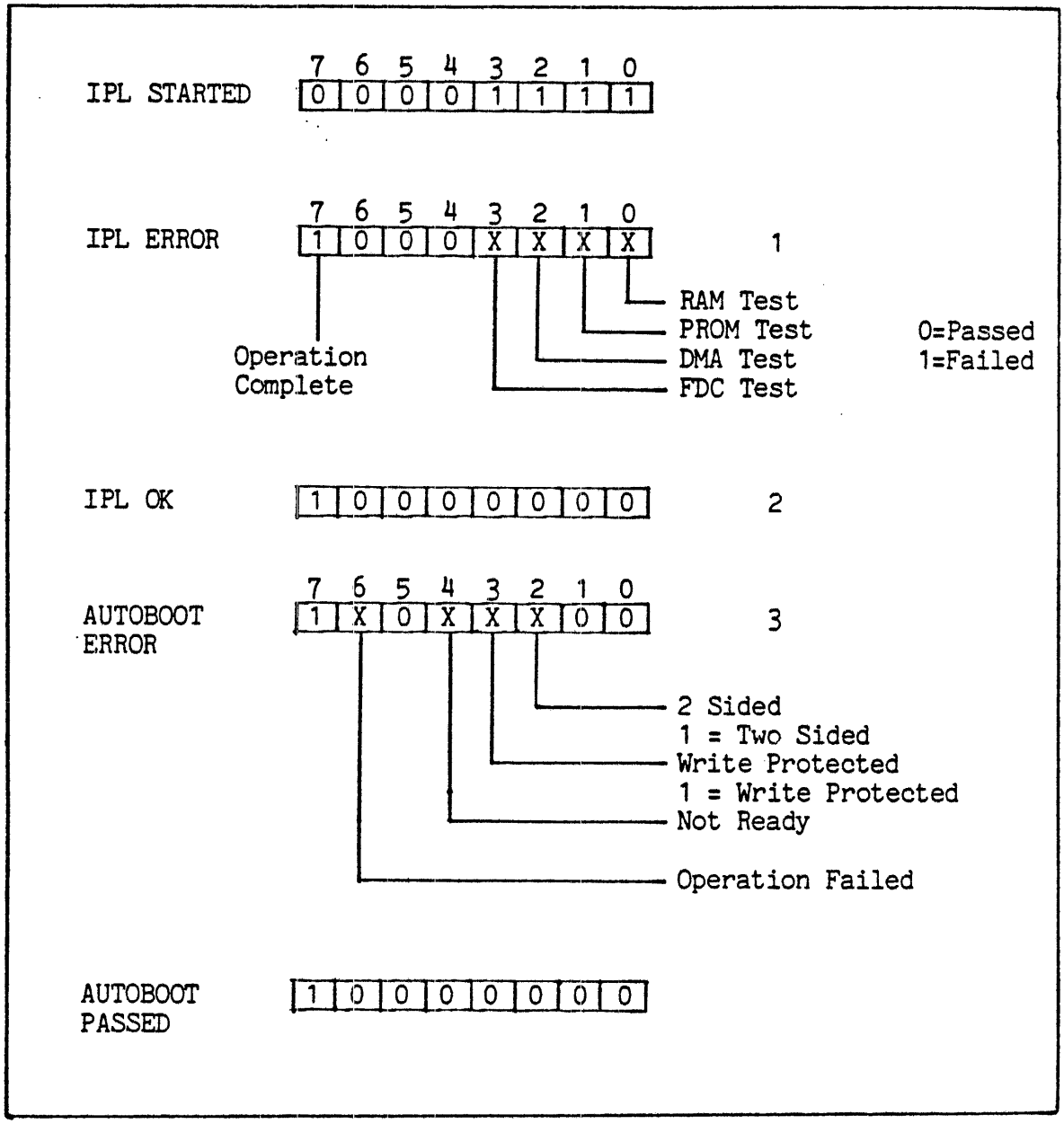


Figure 3-9. Power-On Status Byte

3-27. LIMITED MASTER MODE

When the limited master mode jumper is installed, the Am95/6120 is able to access system resources, including system RAM and ROM. The board can be operated as a general purpose CPU board, but not as a multi-master nor with standard Multibus timing. On-board RAM and ROM may be disabled by installing the memory disable jumper so that only off-board RAM and ROM are accessible. Refer to the appropriate paragraphs in chapter 2 for a description of the limited master mode and memory disable jumpers. A typical application of limited master mode is to run diagnostics programs in system memory.

Following a board reset, a check is made to determine if the limited master mode jumper is installed, and if it is, a branch to location 8000H is performed. With the memory disable jumper not installed, locations 0H through 0BFFH are on-board ROM, locations 0C00 through 0FFF are on-board RAM and all locations above 1000H are off-board. When in limited master mode and with the memory disable jumper installed, all memory locations refer to off-board memory.

When using limited master mode, the following rules must be observed:

- System memory above address 0FFFFH can only be accessed using a DMA transfer, programmed as a main memory access.
- All off-board memory-to-memory DMA transfers must occur within the same 64K-byte segment of system memory, since the contents of the page register remain unchanged throughout the complete DMA transfer.
- The page register is only active during DMA transfers programmed as main memory accesses. Otherwise both internal and system bus addressing occurs as though the page register contains 00H.
- When the memory disable jumper is installed, off-board memory is accessed instead of on-board memory at the same address. If the memory disable jumper is not installed, memory addresses between 0000H and 0FFFH are on-board addresses.
- Memory timing is Multibus compatible only during main-memory DMA accesses. Otherwise all memory and I/O accesses assume a maximum access time of 450 nanoseconds, do not use XACK* and are basically 8085-generated timings. Also the Multibus signals BCLK and CCLK are not generated on-board.
- I/O addresses 00H through 4FH are reserved for on-board resources. Off-board port addresses can use I/O addresses 50H through FFH.
- In limited master mode, no multi-master capability exists, the Am95/6120 has exclusive use of the system bus and resources.

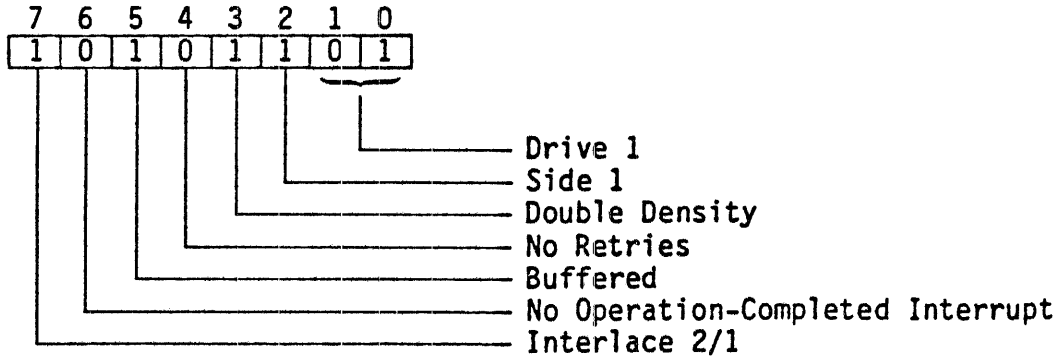
3-28. TYPICAL COMMAND SEQUENCE

A disk operation is performed, under firmware control, following the input of a command code in mail-box register R3. However, prior to the input of this code, other parameters must be entered to define the disk drive and the mode in which it is to be exercised, the track and sector if a data transfer is to be performed, the main memory address if data is to be moved to or from main memory, and other information as needed. The following example is a typical sequence of user software operations to write 10 sectors of data onto drive 1, starting at track 4, sector 1. The transfer is to be buffered, on side 1, double density, and interlaced 2/1. Table 3-2 lists the sequence of operations for a typical WRITE operation.

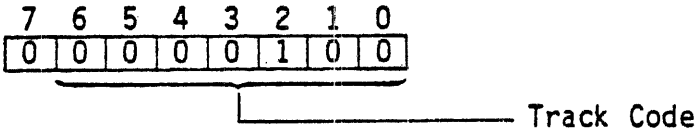
TABLE 3-2. TYPICAL COMMAND SEQUENCE

STEP	OPERATION
1.	Read Status Byte -- wait for Operation Complete bit (bit 7) to set.
2.	Write Unit Code in R0, Write Track Code in R1, Write Sector Code (including Side Compare bit) in R2. Issue Set Parameters command in R3.
3.	Write MSB of memory address in R0, NSB in R1 and LSB in R2. Issue WRITE Command (including Sector Count) in R3.
4.	Loop, checking status Byte for Operation Complete. Check Operation Failed bit. If operation failed, proceed with step 5.
5.	Perform Error Analysis. (Sense Status 2 Command)

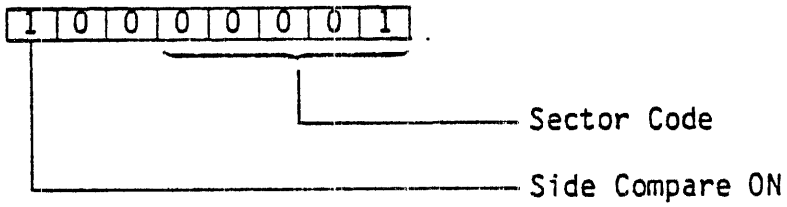
The unit code in step 2 will be as follows:



The track code in step 2 will be as follows:

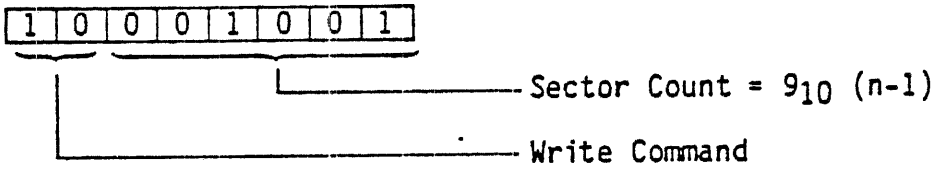


The sector code in step 2 will be as follows:



Assuming a memory address in step 3 of 040FEH, the address code in R0, R1, and R2 will be as follows:

The WRITE command in step 3 will be as follows:



3-29. COMPONENT LEVEL PROGRAMMING

The following paragraphs contain chip level programming and interface information for the Am9085A Microcomputer, the Am9517A Multimode Direct Memory Access Controller (DMA), and the FD1793A Floppy Disk Formatter/Controller.

3-30. Am9085A MICROCOMPUTER

The Am9085A is an 8-bit general purpose microcomputer capable of accessing up to 64K bytes of memory and executing code byte-by-byte. The code executed by the Am9085 resides in the FDC on board E-PROMS, memory locations 0000-0BFF. The CPU chip is controlled exclusively by the firmware and the system CPU does not have access to control this device. Because of the complexity of the Am9085 and the various ways it can be used, and because many books and descriptions are currently in publication, it would be redundant to repeat that data here. If detailed information on the Am9085A CPU chip is required, consult the Am9085 User's Manual.

3-31. MULTIMODE DIRECT MEMORY ACCESS (DMA) CONTROLLER Am9517A

The Am9517 DMA controller provides the FDC board with the capability to transfer data to/from the FDC board and main memory and to route data on the board using four separate channels. The data channels can be programmed to perform single transfer mode or block transfer mode.

3-32. Single Transfer Mode

When in the single transfer mode, the Am9517 is programmed to make a single byte transfer. The word count is decremented/incremented following each transfer. A terminal count (TC), reached when the word count is zero, causes an autoinitialize when the channel is so programmed.

3-33. Block Transfer Mode

When using the block transfer mode, the Am9517 is programmed to continue making transfers upon activation of the DREQ signal until a terminal count, caused by the word count going to zero, or an external end of process signal.

3-34. Addressing

The Am9517 DMA controller uses 16 consecutive I/O port addresses (10H through 1FH) for reading and writing of the twelve internal registers. The port addresses and their functions are listed in table 3-3.

TABLE 3-3. DMA (Am9517A) I/O PORT ADDRESSES

I/O PORT	INPUT FUNCTION (IOW)	OUTPUT FUNCTION (IOR)
10	Channel 0 Address	
11	Channel 0 Word Count	
12	Channel 1 Address	
13	Channel 1 Word Count	
14	Channel 2 Address	
15	Channel 2 Word Count	
16	Channel 3 Address	
17	Channel 3 Word Count	
18	STATUS REGISTER	COMMAND REGISTER
19	Not Used	REQUEST REGISTER
1A	Not Used	SINGLE MASK REGISTER
1B	Not Used	MODE REGISTER
1C	Not Used	CLEAR BYTE POINTER FLIP-FLOP
1D	Temporary Register	MASTER CLEAR
1E	Not Used	Not Used
1F	Not Used	ALL MASK REGISTER

3-35. Registers

The Am9517 DMA controller's twelve addressable registers are listed in table 3-4. These register addresses are listed in table 3-3 and their functions are described in the following paragraphs.

3-36. Command Register

This 8-bit register controls the operation of the Am9517. It is programmed by the Am9085 and is cleared by Reset. The port address of the command register is 18H and IOW active. The function of each command bit is illustrated in figure 3-10.

3-37. Mode Register

Each of the four channels has its own 6-bit mode register. When the Am9085 is writing into this register, bits 0 and 1 determine which channel mode register is to be written. The port address of the mode register is 1BH and IOW active. The bit assignment and definition are shown in figure 3-11.

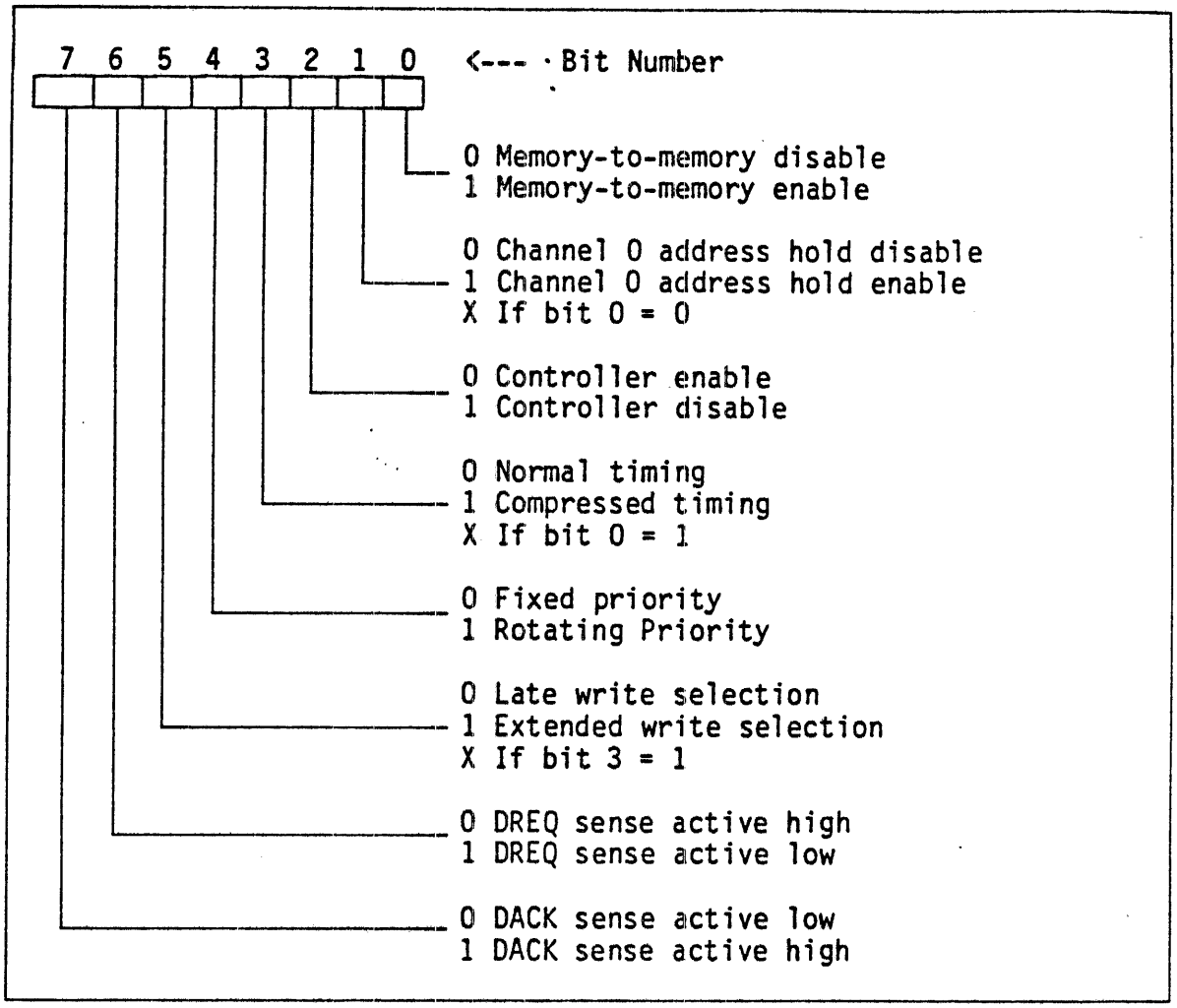


Figure 3-10. Am9517A Command Register

3-38. Request Register

The Am9517 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the four bit register. Each register bit is set or reset separately under software control or as cleared on generation of a terminal count or end of process. The port address of the request register is 19H and IOR active. To set or reset a bit, the software loads the proper form of the data word, shown in figure 3-12.

3-39. Mask Register

Each channel has associated with it a mask bit which can be set to disable the incomming DREQ. Each mask bit sets when its associated channel produces an end of process and the channel is not programmed for autoinitialization. Each bit of the four bit mask register can be set or cleared separately under software control.

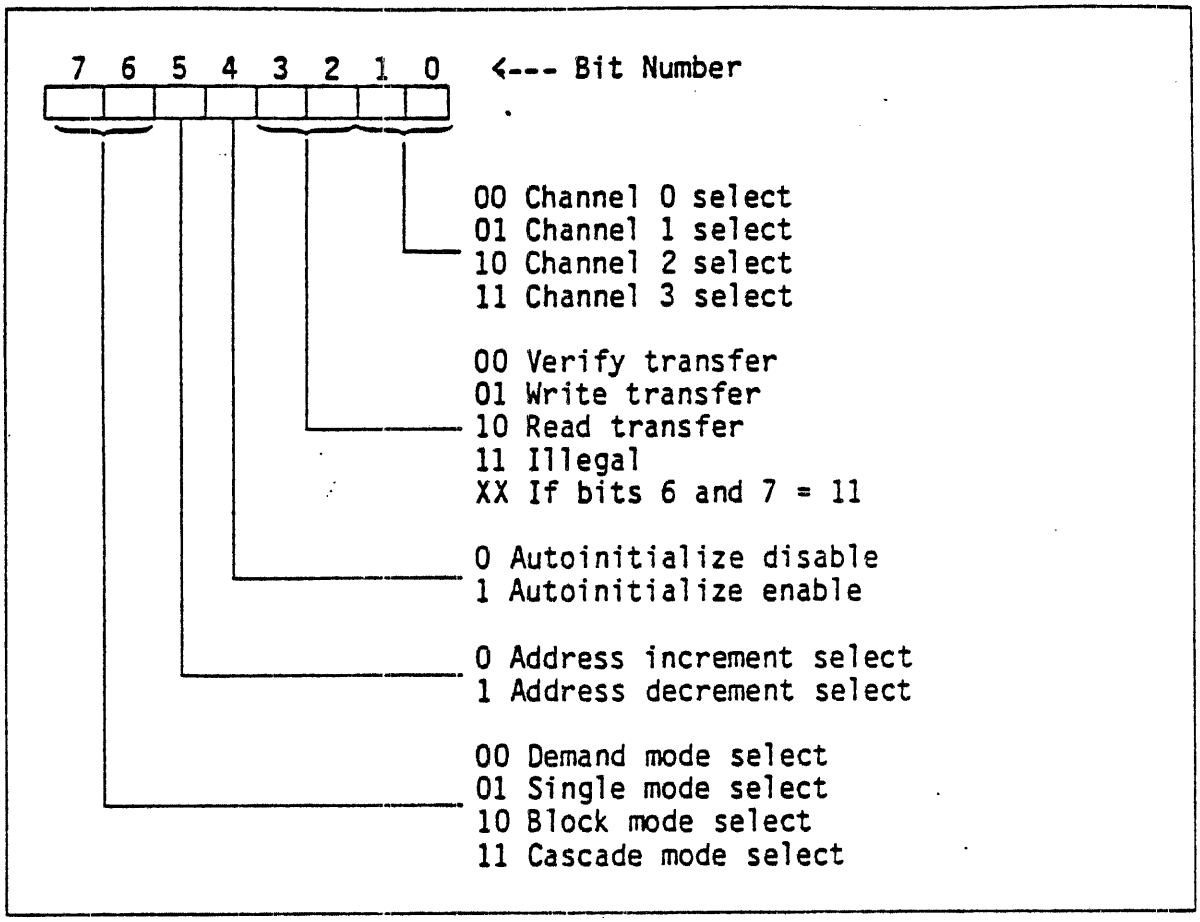


Figure 3-11. Am9517A Mode Register Bit Assignments

The entire register is set by Reset, which disables all DMA requests until a clear mask register instruction allows them to occur. The port address to set individual bits is 1AH with IOR active and when all four bits are written with a single command, address port 1FH and IOW active. The bit configuration and definitions are shown in figure 3-13.

TABLE 3-4. Am9517A INTERNAL REGISTERS

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

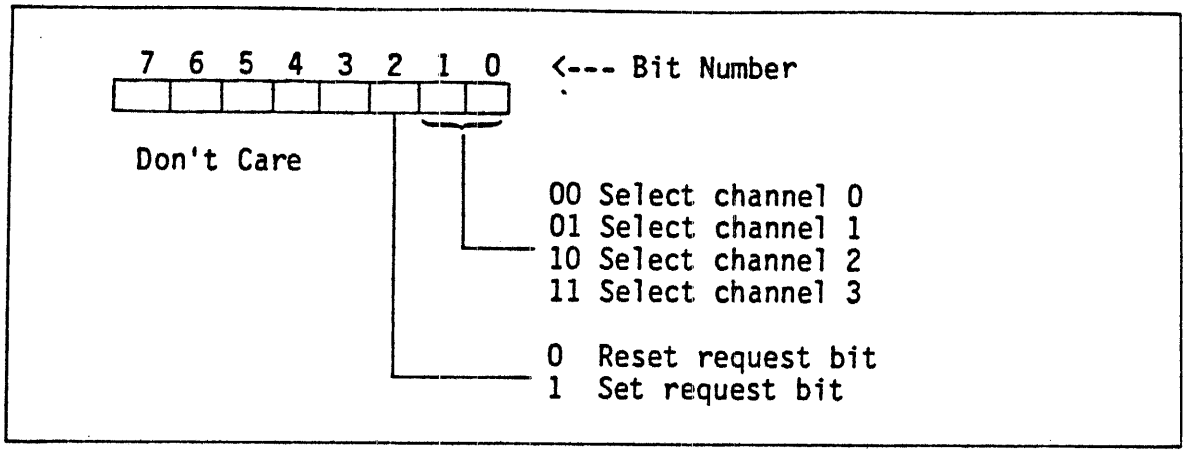


Figure 3-12. Am9517A Request Register

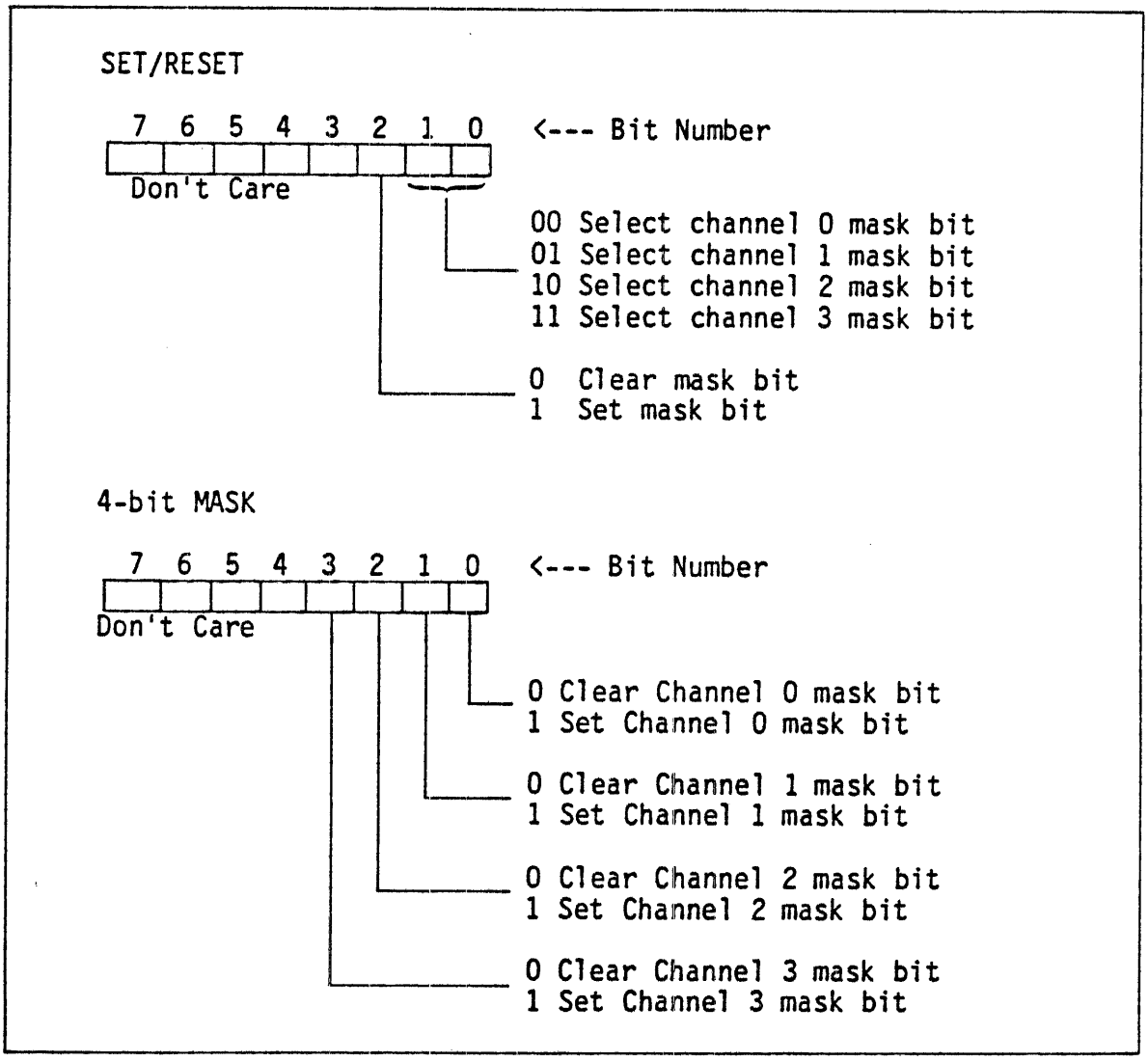


Figure 3-13. Am9517A Mask Register

3-40. Status Register

The status register contents are available to be read out by addressing port 18 and activating IOR. It contains the device status which includes the channels that have reached a tunnel count and which channels have pending DMA requests. Bits 0-3 are set each time a terminal count is reached by the appropriate channel. These bits are cleared upon Reset and on each Status Read. Bits 4-7 are set when the corresponding channel request services. Figure 3-14 shows the bit configuration of the Status Register.

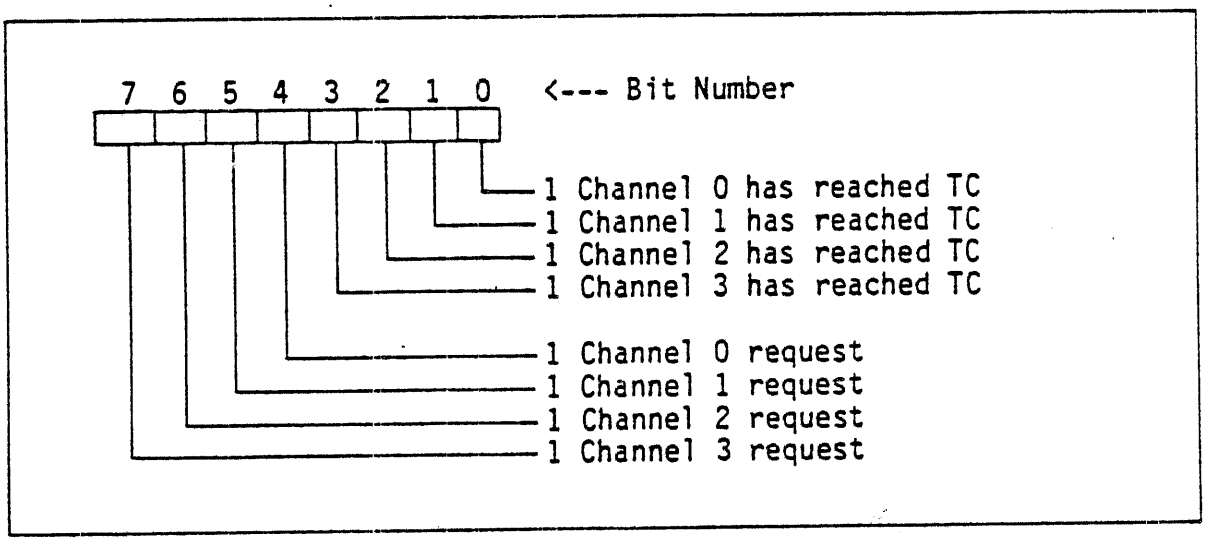


Figure 3-14. Am9517A Status Register Configuration

3-41. Temporary Register

The temporary register resides at address port 1D and holds data during memory-to-memory transfers. When the transfer is complete, the last word moved can be read by the microprocessor. This register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

3-42. Software Commands

There are two additional software commands that can be executed on the Am9517 that do not depend on any specific bit pattern on the data bus. These two commands are described in the following paragraphs and the address codes are shown in table 3-5.

TABLE 3-5. SOFTWARE COMMAND CODES

Operation	Registers Affected	Signals						
		CS	IOR	IOW	A3	A2	A1	A0
Clear FF	Internal First/Last Flip/Flop	0	1	0	1	1	0	0
Master Clear	Clear: Command Status Request Temporary Internal First/Last Flip/Flop Set: Mask	0	1	0	1	1	0	1

3-43. Clear First/Last Flip-Flop

This command is executed prior to writing or reading new address or word count information to the Am9517. This initializes the flip/flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

3-44. Master Clear

This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The Am9517 will enter the Idle cycle.

3-45. FLOPPY DISK FORMATTER/CONTROLLER FD1793

The FD1793A is a MOS LSI device that performs the functions of a Floppy Disk Formatter/Controller. The FD1793A is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The device is included in the floppy disk controller board, and contains a flexible interface organization that accomodates the firmware interface and the disk drive interface.

The firmware to processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The device operates on a multiplexed bus with other bus oriented devices.

3-46. Processor Interface

The FD1793 to Am9085 processor interface is accomplished through the eight Data Access Lines (DAL) and associated control signals. Data, status, and control words out of or into the FD1793 use the DAL. The DAL contains three state buffers, which are enabled as output drivers when Chip Select and Read Enable are active, and enabled as input receivers when Chip Select and Write Enable are active.

When data transfer through the FD1793 is required by the Am9085, the device address is decoded making the Chip Select (CS) line active. The two address ports on the FD1793 and the accessed registers are listed in table 3-6. The address bits A1 and A0 combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the registers.

TABLE 3-6. FD1793 ADDRESS PORT ASSIGNMENT

A1/A0	READ (RE)	WRITE (WE)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During DMA types of transfers between the FD1793 Data Register and the buffer or main memory, the Data Request (DRQ) output is used in Data Transfer Control. This signal also appears as status bit 1 during read and write operations.

3-47. Floppy Disk Interface

The floppy disk interface consists of head positioning controls, write gate controls, and data transfer lines. A 2.0MHz $\pm$1% squarewave clock is required at the CLK input for internal control timing in standard floppy mode (4 MHz for minifloppy). Commands read into the FD1793 from the Am9085 are implemented and the appropriate signals are sent to a selected disk drive.

3-48. Command Description

The FD1793 accepts and executes eleven commands. The command words should be loaded into the command register only when the busy status bit is off (Status Bit 0). An exception is the Force Interupt command. When a command is being executed, the busy status bit is set. When a command is completed, an interrupt is generated and the Busy Status bit is reset. The status register indicates whether a command is computed or an error occured. The commands are divided into four types and are explained in the following paragraphs.

3-49. Restore (Seek Track 0)

When this command is read into the command register and execution is implemented, the track 00 (TR00) input is sampled. If TR00 is active, indicating the Read/Write head is positioned over track 0, the track register is filled with zeroes and an interrupt is generated. If TR00 is not active, stepping pulses at a rate specified by bits 0 and 1 are sent to the drive unit until TR00 is activated. At this time the TR is filled with zeroes and an interrupt is generated. If the TR00 does not activate after 255 stepping pulses, the operation is terminated automatically, the interrupt is set, and the seek error status bit is set. A verification operation occurs if bit 2 of the command is set. The Restore command is implemented automatically when the master reset occurs. Figure 3-15 illustrates the bit configuration of the command register for a RESTORE command.

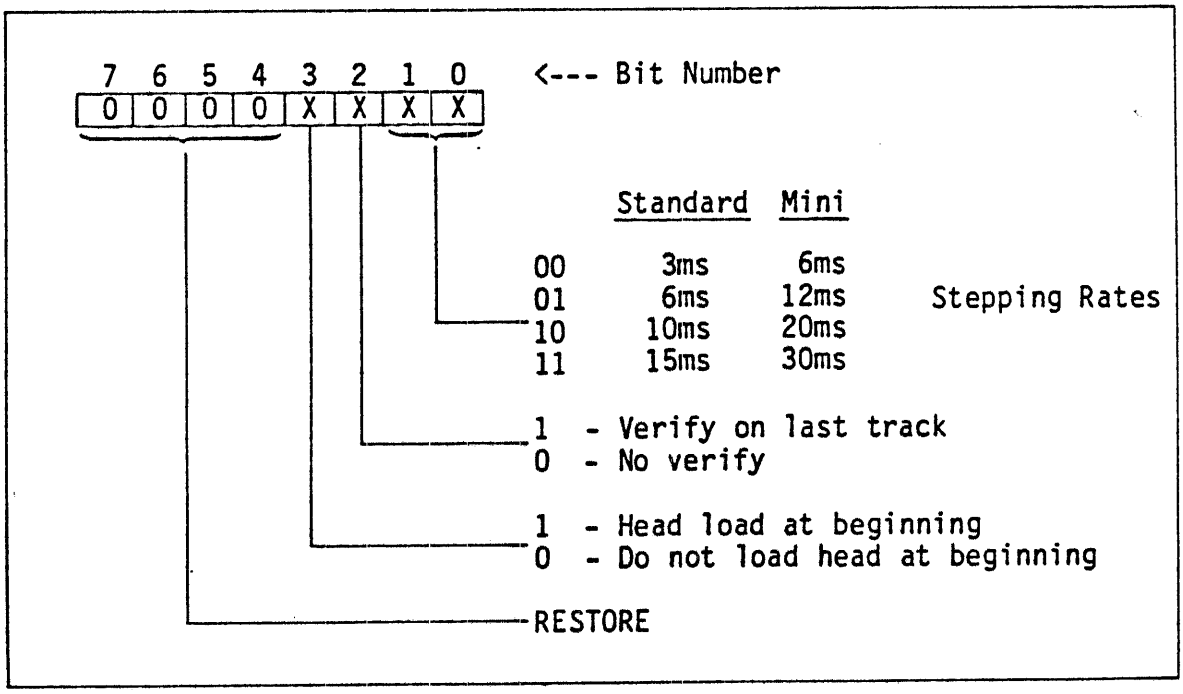


Figure 3-15. FD1793 Restore Command

3-50. Seek

This command assumes the track register contains the current Read/Write head track position and the data register contains the desired track number. The FD1793 updates the track register and issues stepping pulses in the proper direction, positioning the Read/Write head, until the contents of the track register equal the data register. At this point the Read/Write head is positioned over the desired track. An interrupt is generated at the end of this operation. Figure 3-16 illustrates the command register bit configuration for a SEEK command.

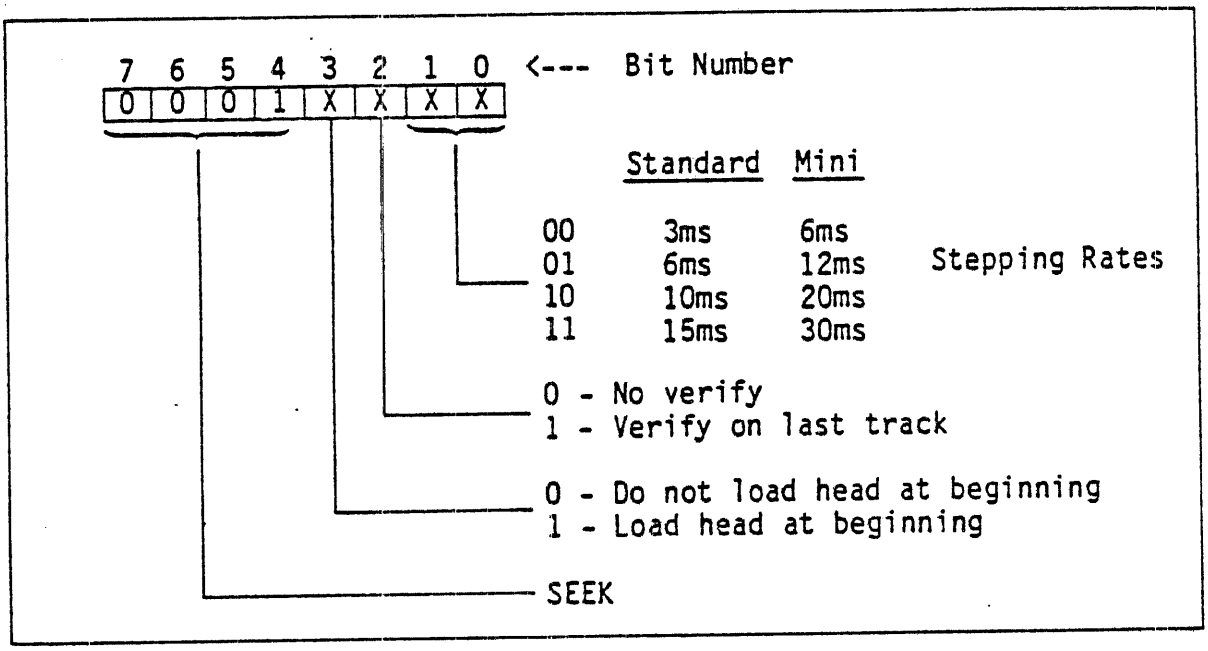


Figure 3-16. FD1793 Seek Command

3-51. Step-In

The STEP-IN command causes the FD1793 to issue one stepping pulse such that the Read/Write head moves one track toward track 76. An interrupt is generated at the completion of this command. Figure 3-19 illustrates the command register bit configuration for a STEP-IN command.

3-52. Read

When the READ command is issued to the FD1793, the following events occur. The Read/Write head is loaded, the Busy status bit is set, and when the ID field (with the correct track number, sector number, and CRC) is encountered, the data read from the disk data field is transferred to the DMA controller for routing. The Data Address Mark (AM) must be found within 30 bytes (43 bytes in double density) of the last ID field CRC byte, if not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of

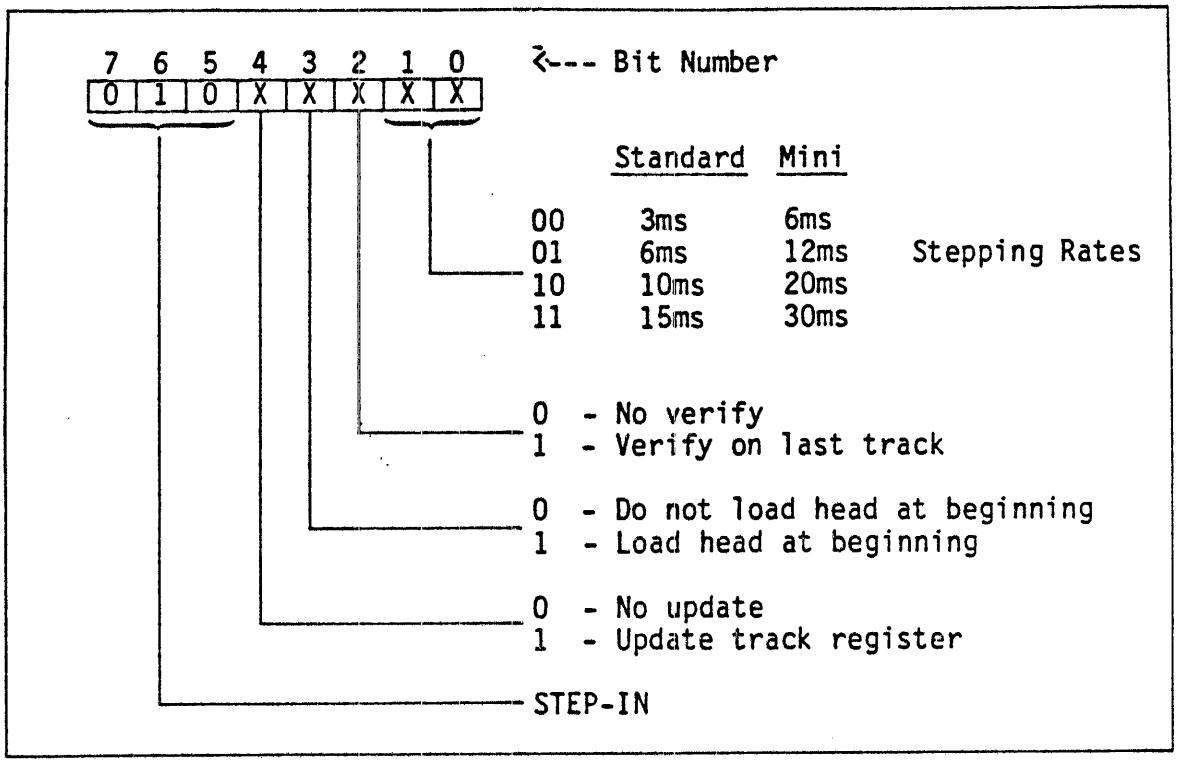


Figure 3-17. FD1793 Step-In Command

data is shifted through the Data Shift Register (DSR), it is transferred to the Data Register (DR) and DRQ is generated. When the next byte is encountered in the Data Shift Register (DSR), it is transferred to the DR and another DRQ is generated. If the DMA has not read the previous contents of the DR before a new character is transferred, that character is lost and the Lost Data status bit is set. This sequence is repeated until the entire data field is read. If a CRC error occurs at the end of the data field, the CRC error Status bit is set and the command is terminated.

When the read operation is complete, the type of Data Address Mark read in the data field is recorded in the Status Register. For a definition of the bits affected, see the Status Register description. Figure 3-20 illustrates the command register bit configuration for a READ command.

3-53. Write

Upon receipt of the WRITE command, the Read/Write head is loaded (HLD active) and the Busy status bit is set. When the correct ID field is located, a DRQ is generated. After 11 bytes (single density) or 22 bytes (double density) of the CRC field, Write Gate (WG) activates if the DRQ is serviced. If the Data Register has not been loaded, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, WG activates and six bytes of zeroes are written on the diskette.

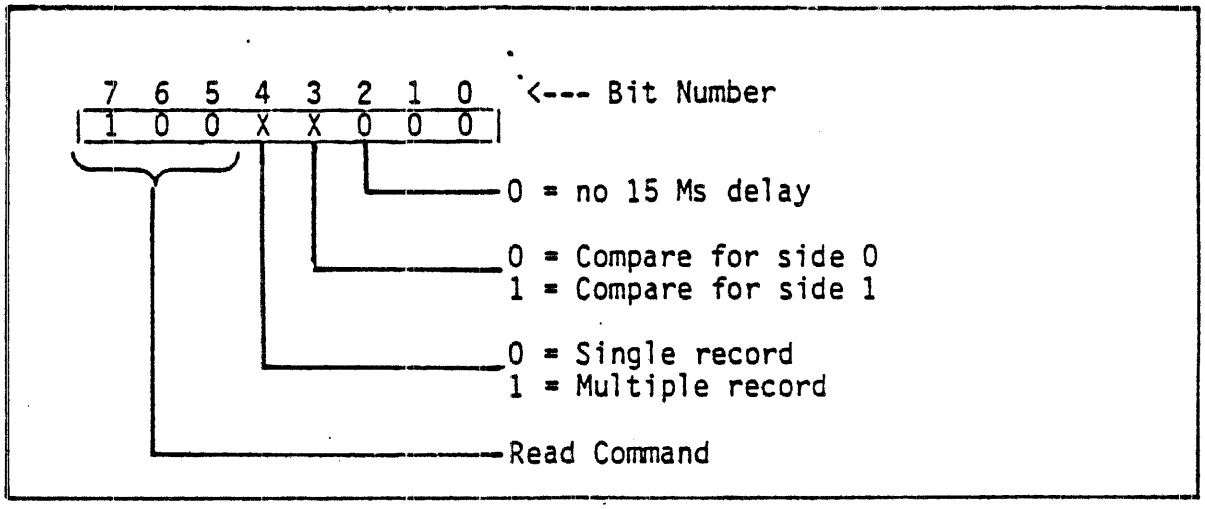


Figure 3-18. FD1793 Read Command

The FD1793 proceeds to write the data field and generate DREQ to the DMA. If a Data request is not serviced in time for continuous writing, the Lost Data Status bit is set and a byte of zeros is written on the diskette, but the command is not terminated. When the last data byte is written, the two-byte CRC is computed internally and written, followed by a one byte gap of logic ones. The command is then terminated. Figure 3-19 illustrates the command register bit configuration for a WRITE command.

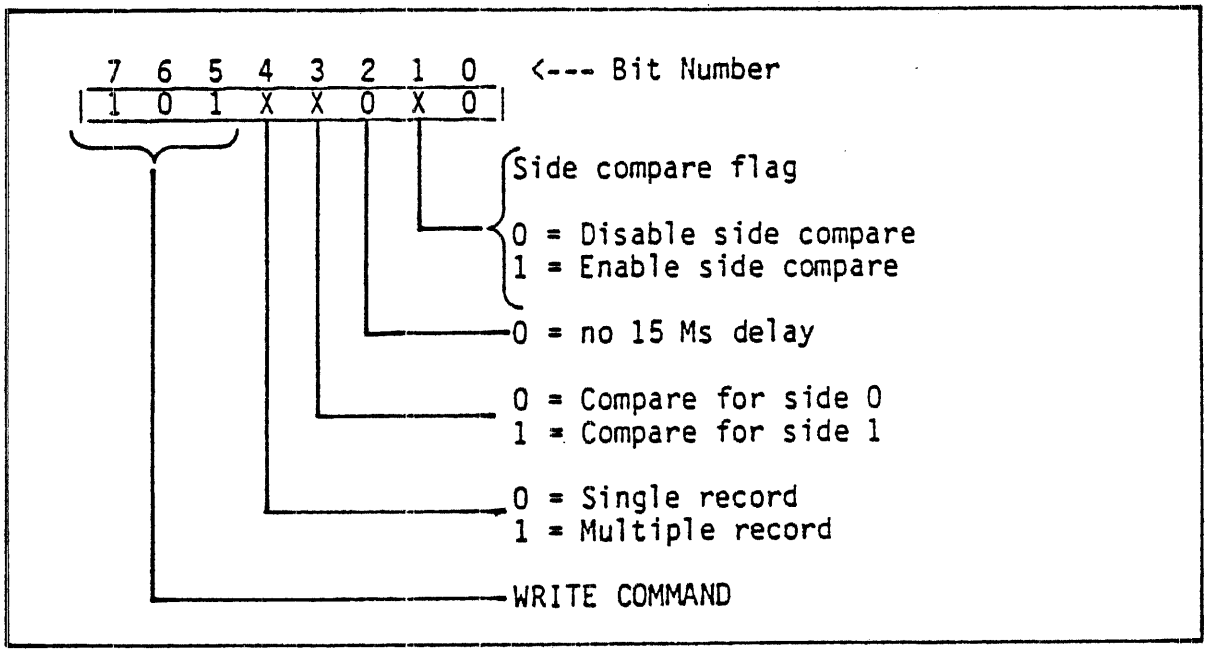


Figure 3-19. FD1793 Write Command

3-54. Write Track

The Write Track command is initiated by loading the Read/Write head and setting the Busy status bit. Writing on the disk occurs coincident with the leading edge of the index pulse and terminates at the next index pulse. Data Request is activated with the receipt of the Write Track command, but no writing occurs until the first byte is read into the Data Register. If the Data Register is not loaded by the arrival of the first index pulse, the operation is terminated and interrupt activated. If, once writing is instituted, a byte is not present in the Data Register when required, a byte of zeros is substituted. Address marks and CRC characters are written on the disk by detecting certain data patterns in the write data stream as shown in table 3-7. The CRC generator is initialilzed when any data byte from F7 to FE is about to be transferred from the Data Register to the Data Shift Register.

Table 3-7. Data Pattern Control Bytes for Initialization

Data Pattern in DR (Hex)	FD179X Interpretation in FM ($\overline{DDEN}$ = 1)	FD1791/3 Interpretation in MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 w/CLK = FF	Write 00 thru F4, in MFM
F5	Not allowed	Write A1* in MFM, preset CRC
F6	Not allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, CLK = C7, preset CRC	Write F8 thru Fb, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, preset preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

* Missing clock transition between bits 4 and 5
** Missing clock transition between bits 3 and 4

3-55. Force Interrupt

This command can be loaded into the command register at any time. If a command is being executed (Busy Status Bit set), that command is terminated and an interrupt generated upon the selected condition programmed by bits 0 through 3. Figure 3-20 illustrates the command register for a FORCE INTERRUPT command.

3-56. Status Register

The Status Register is located at address port 00 and at the receipt of any command except Force Interrupt, the Busy status bit is set. Also, the rest of the status bits are updated or cleared for the new command. When the Force Interrupt Command is received and a command is being executed, the Busy status bit is reset and the other status bits remain unchanged. If no command is being executed when a Force Interrupt is

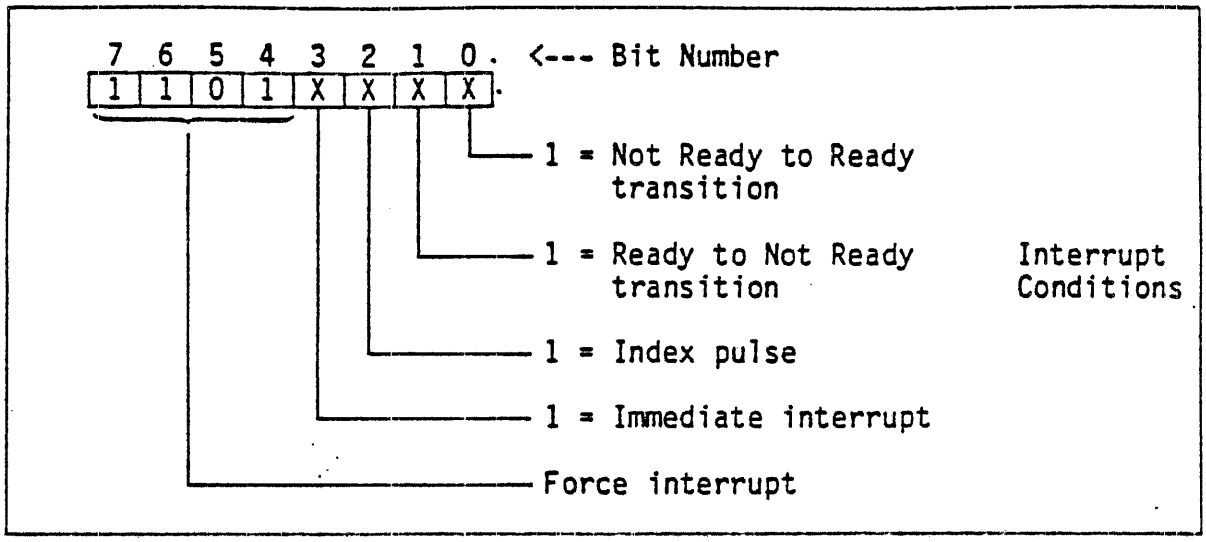


Figure 3-20. FD1793 Force Interrupt Commmand

received, the Busy status bit is reset and the other status bits are updated or cleared. Figure 3-21 illustrates the bit configuration of the Status Register.

(BITS)

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Bit	All Type I Commands	Read Address	Read	Read Track	Write	Write Track
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
A0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Figure 3-21. FD1793 Status Register

CHAPTER 4
THEORY OF OPERATION

4-1. INTRODUCTION

The FDC board operates under command of the host CPU. Communication between the host system and FDC board take place through five mailbox registers. Three of these register are used to accept variable user parameters, one is used to accept firmware commands, while the fifth register provides the host system with a final status code at the completion of each command.

The commands and variable user parameters are interpreted by the on-board Am9085 CPU to produce floppy disk drive control signals for the FD1793 Floppy Disk Formatter/Controller. Data transfer between disk and host system memory in performed by an LSI circuit consisting of an Am9517 Multimode DMA Controller.

In addition to firmware control of floppy disk operations, the FDC board accepts user code for execution. All facilities contained in the Am95/6120 FDC such as drive control register, board control register, FD1793 Disk Controller, mailbox registers, and 9517 DMA Controller are accessible via down-loaded user code.

4-2. BLOCK DIAGRAM

Figure 4-1 includes a block diagram of the Am95/6120 FDC. When operating in Limited Master Mode, the signal paths, marked with an asterisk, are active.

4-3. BOARD CONTROL REGISTER

The board control register accepts byte data from the on-board CPU to specify internal operations on the FDC board. The board control register is accessed through on-board I/O port 48H and is write-only. The bit format of the board control register is shown in figure 4-2.

4-4. BOARD STATUS REGISTER

The board status register provides temporary storage for status signals from internal board functions. These signals are switched under control of the on-board CPU to the internal data bus. The board status register is accessed by reading on-board I/O port 48H. The format of the board status register is shown in figure 4-3.

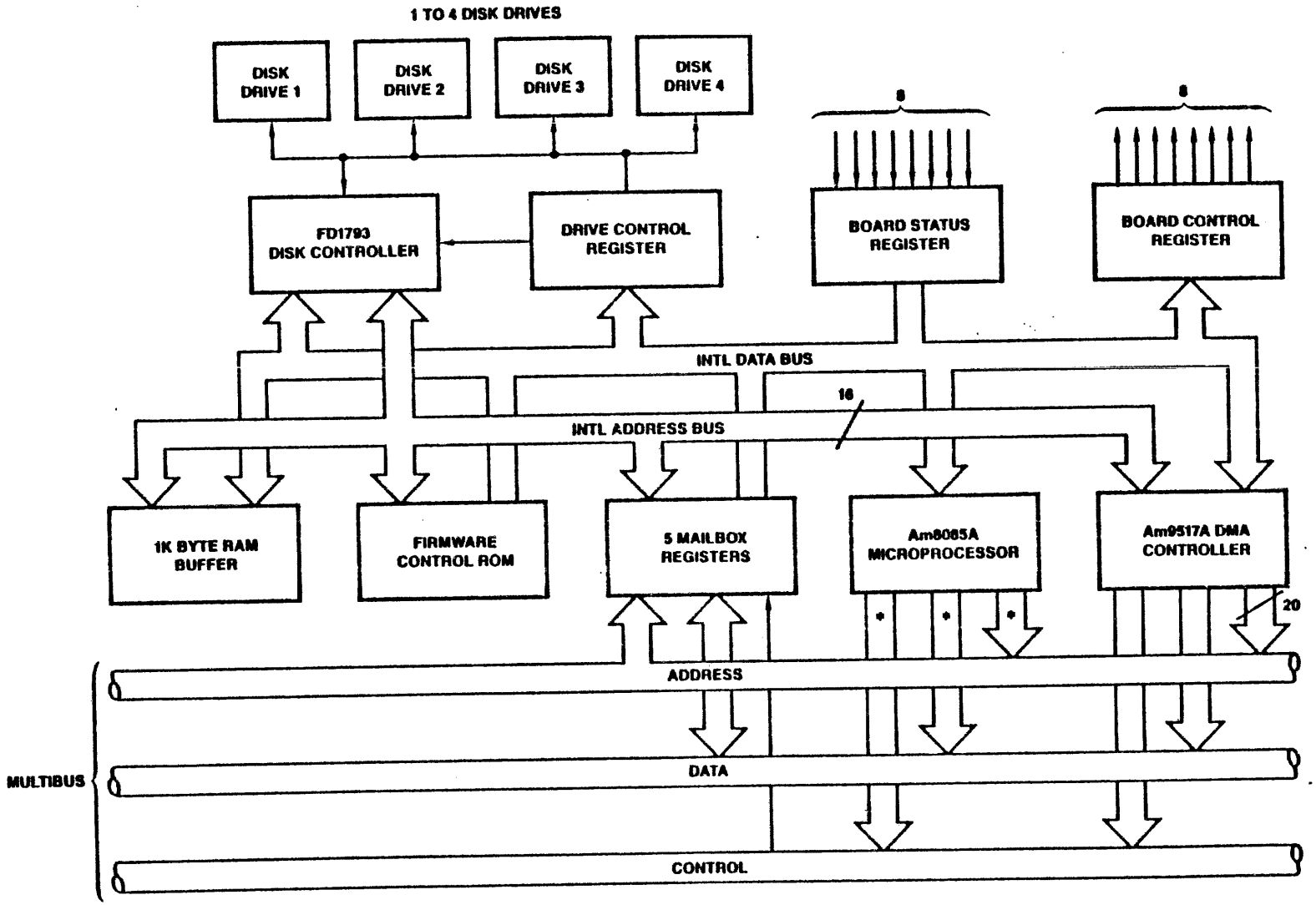


Figure 4-1. Block Diagram

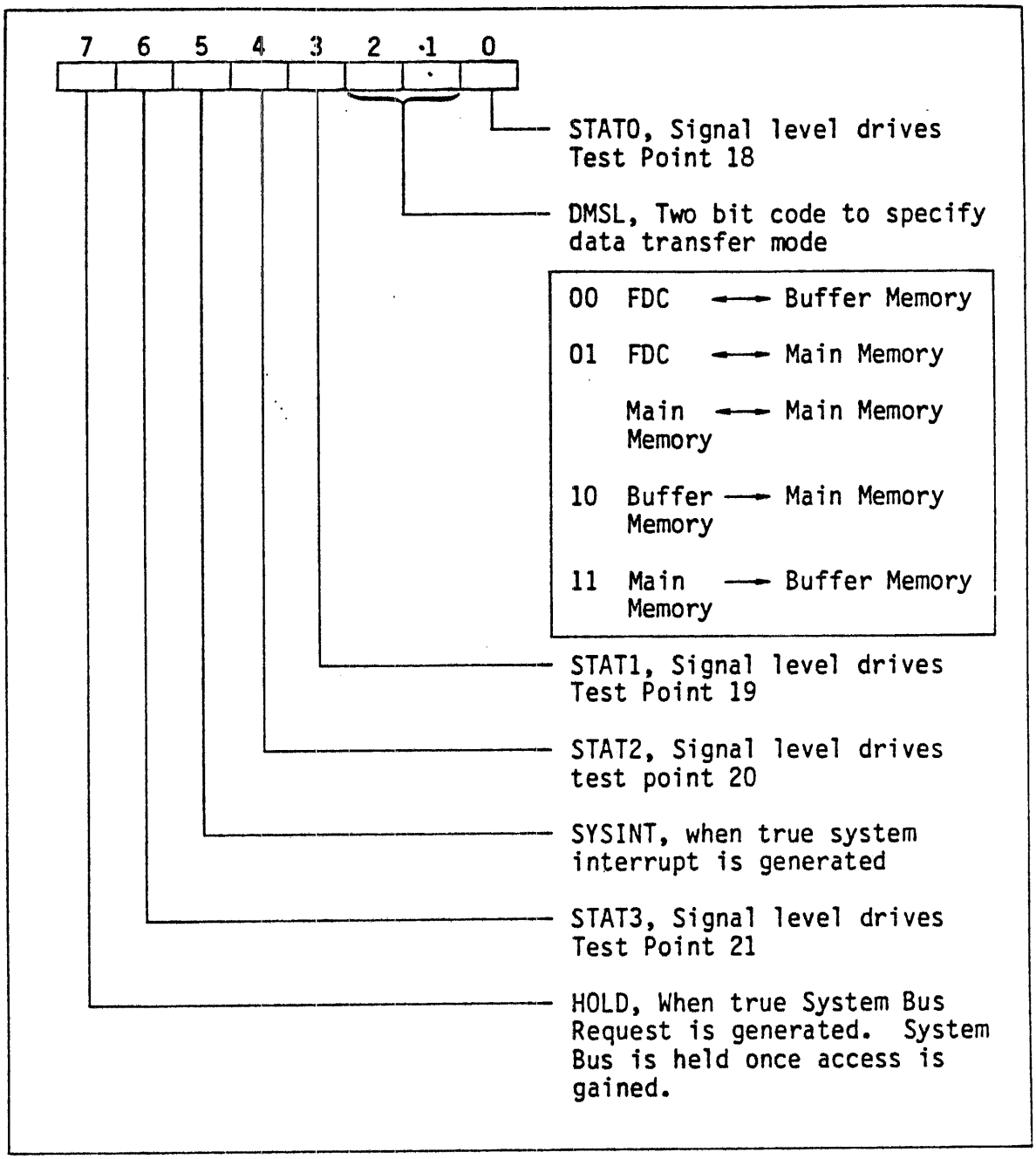


Figure 4-2. Board Control Register

4-5. DRIVE CONTROL REGISTER

The drive control register provides temporary storage for several of the disk drive control signals which are output to the disk drives through connectors P3 and P4. The drive control register is accessed by the on-board CPU, through I/O port 4DH (write only). The format of the drive control register is shown in figure 4-4.

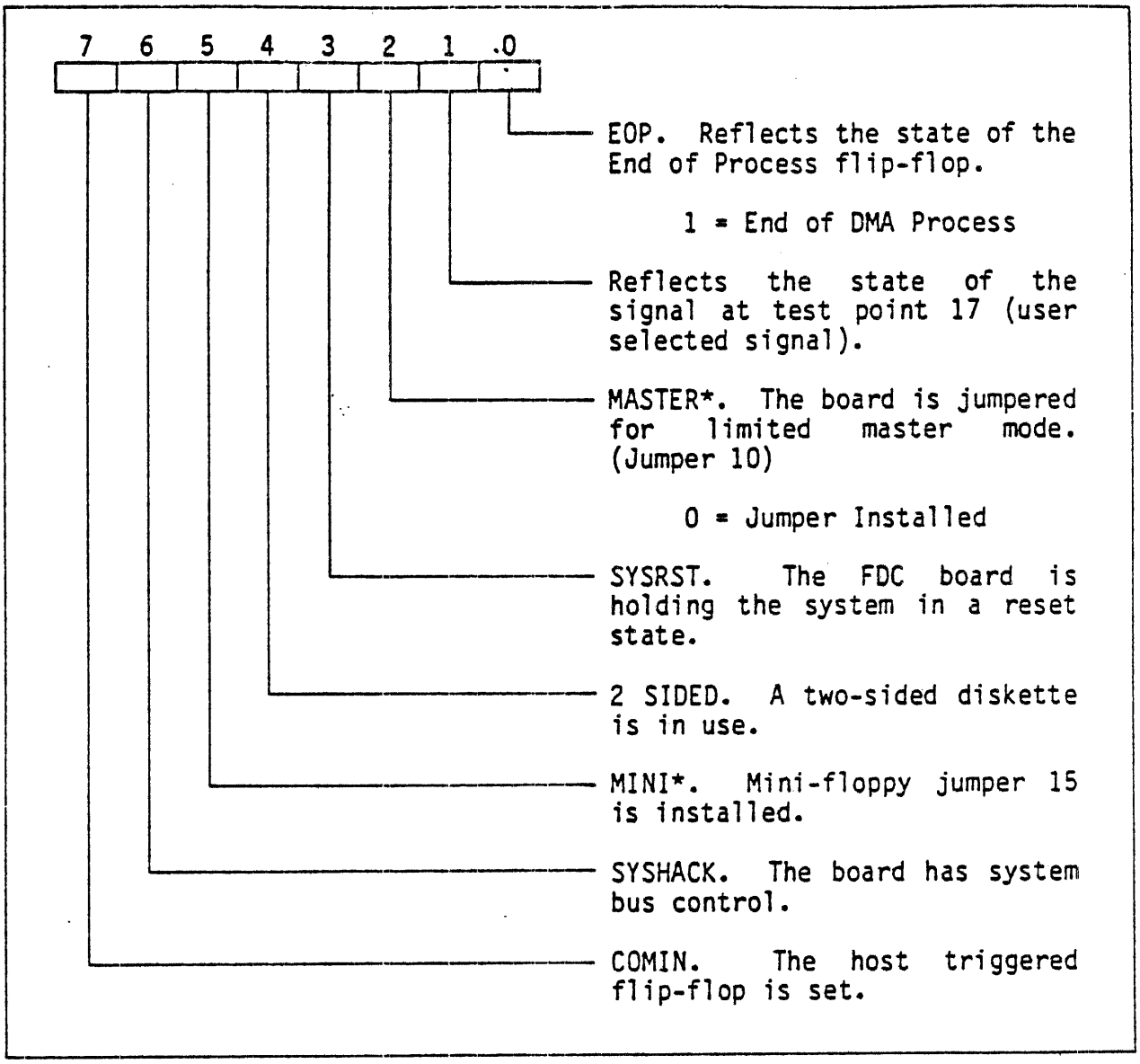


Figure 4-3. Board Status Register

4-6. ON-BOARD MEMORY

On board memory consists of 3K Firmware ROM and 1K RAM. Figure 4-5 is the memory map.

4-7. RAM

RAM consists of 1K bytes on two Am9114 devices. RAM is used by the factory supplied firmware as data storage, stack area, and disk I/O buffer. It is available as a user program area for down loaded user code (Special Execute Instruction).

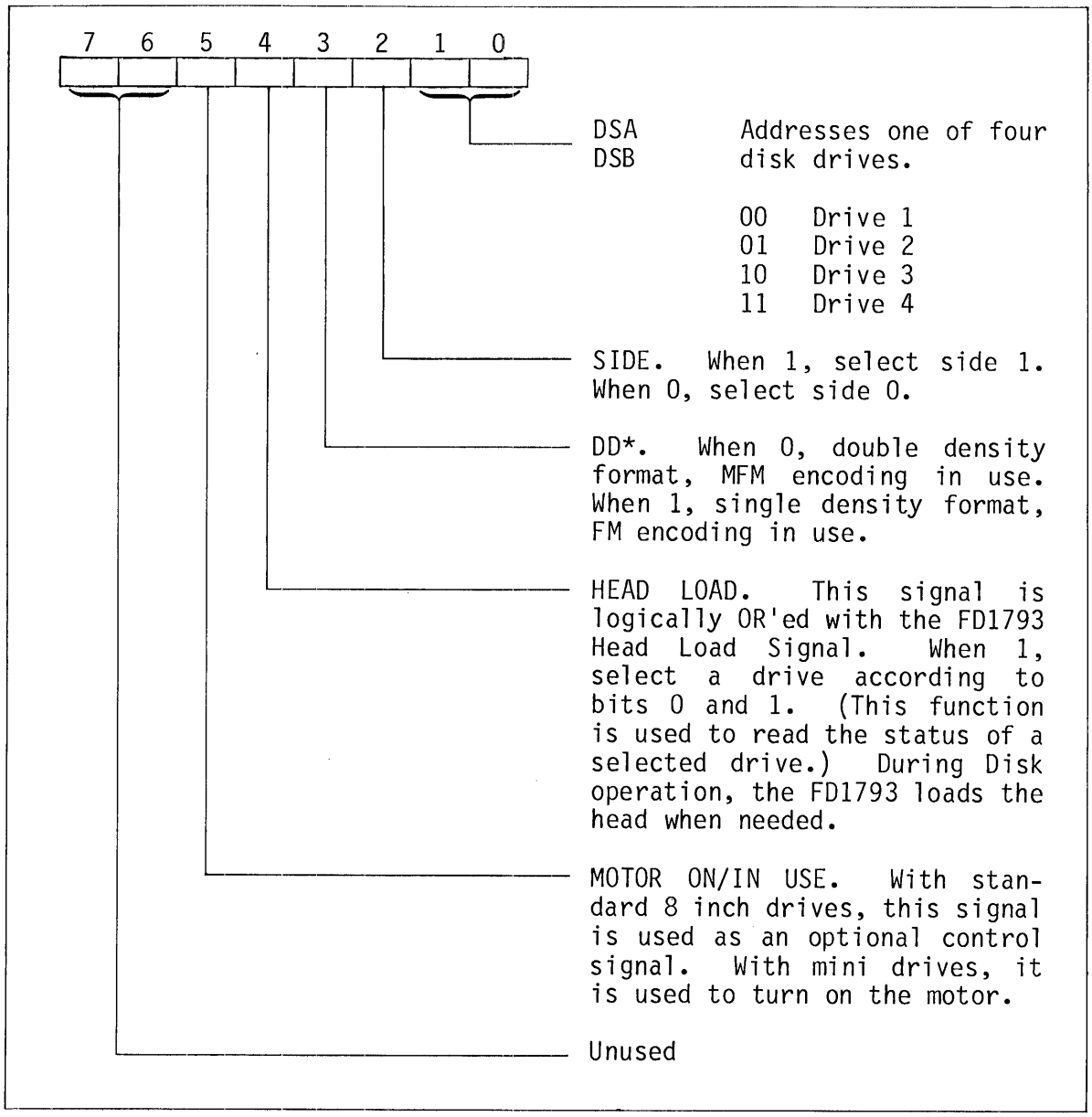


Figure 4-4. Drive Control Register

4-8. FIRMWARE ROM

The FDC operating firmware is supplied on three 2708 E-PROM devices. The FDC firmware is discussed in detail, and a listing is provided in Am95/6120 Firmware Listing Manual, publication number 00680153.

4-9. DISK CONTROLLER

The disk controller circuits consist of an LSI FD1793 device, disk drive interface circuits and a phase-lock-loop data separator.

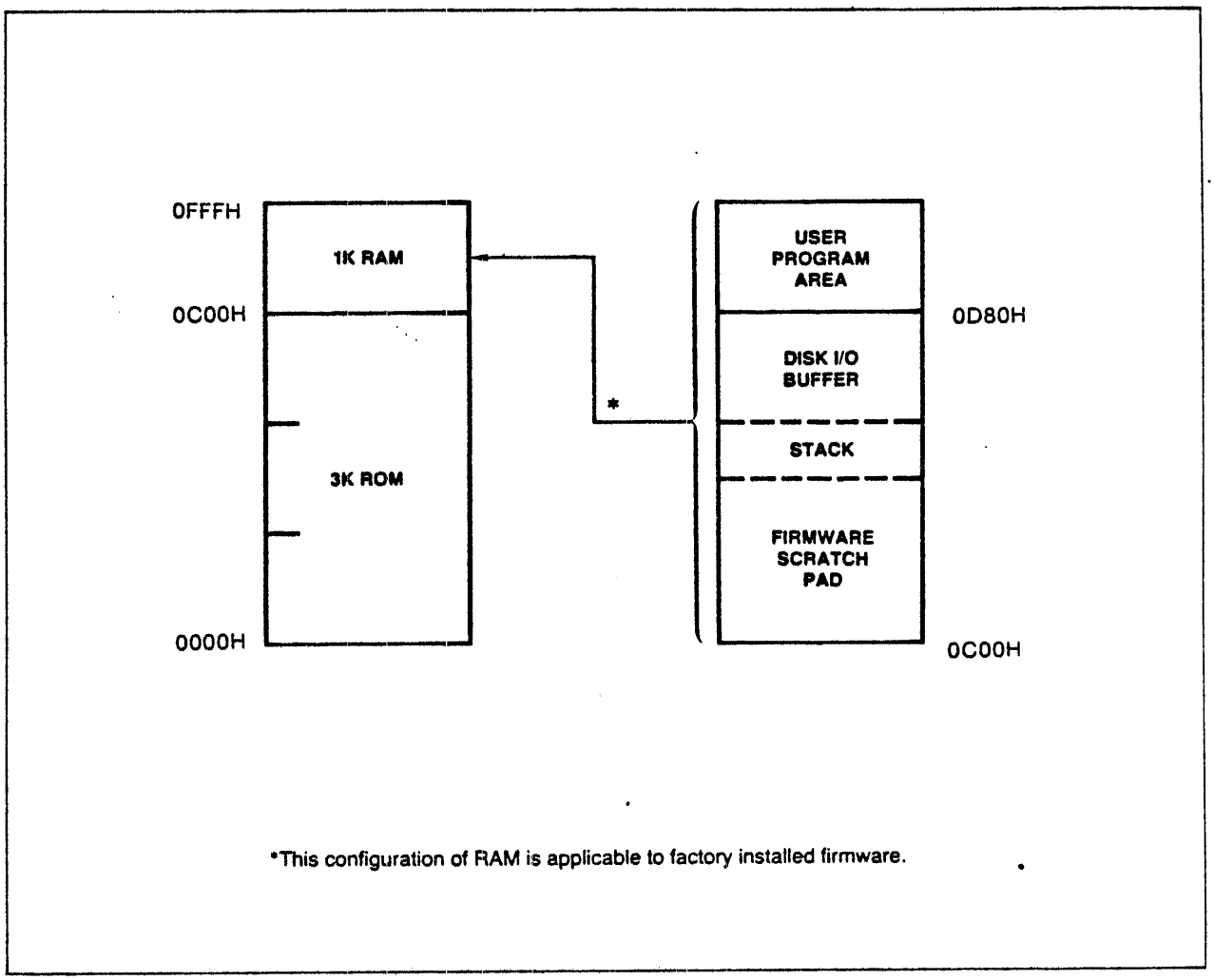


Figure 4-5. On-Board Memory Map

4-10. FD1793 FLOPPY DISK CONTROLLER

This LSI device provides data formatting and disk drive control signals. A description of this device is included in section 3.

4-11. DISK DRIVE INTERFACE CIRCUITS

These circuits are used in conjunction with the FD1793 to provide signal buffering, write precompensation for double density disk storage on tracks greater than 43, and drive control logic.

4-12. PHASE LOCK LOOP

The phase lock loop is used to control the 8 MHz Voltage Controlled Oscillator (8VCO) frequency when the FDC is configured for double density operation. The filter constants in the phase lock loop (C2, C49, and R4) are optimized for standard disk (8 inch) double density operation. When used for minifloppy operation, device U34 must be removed from the board. A block diagram of the phase lock loop is shown in figure 4-6.

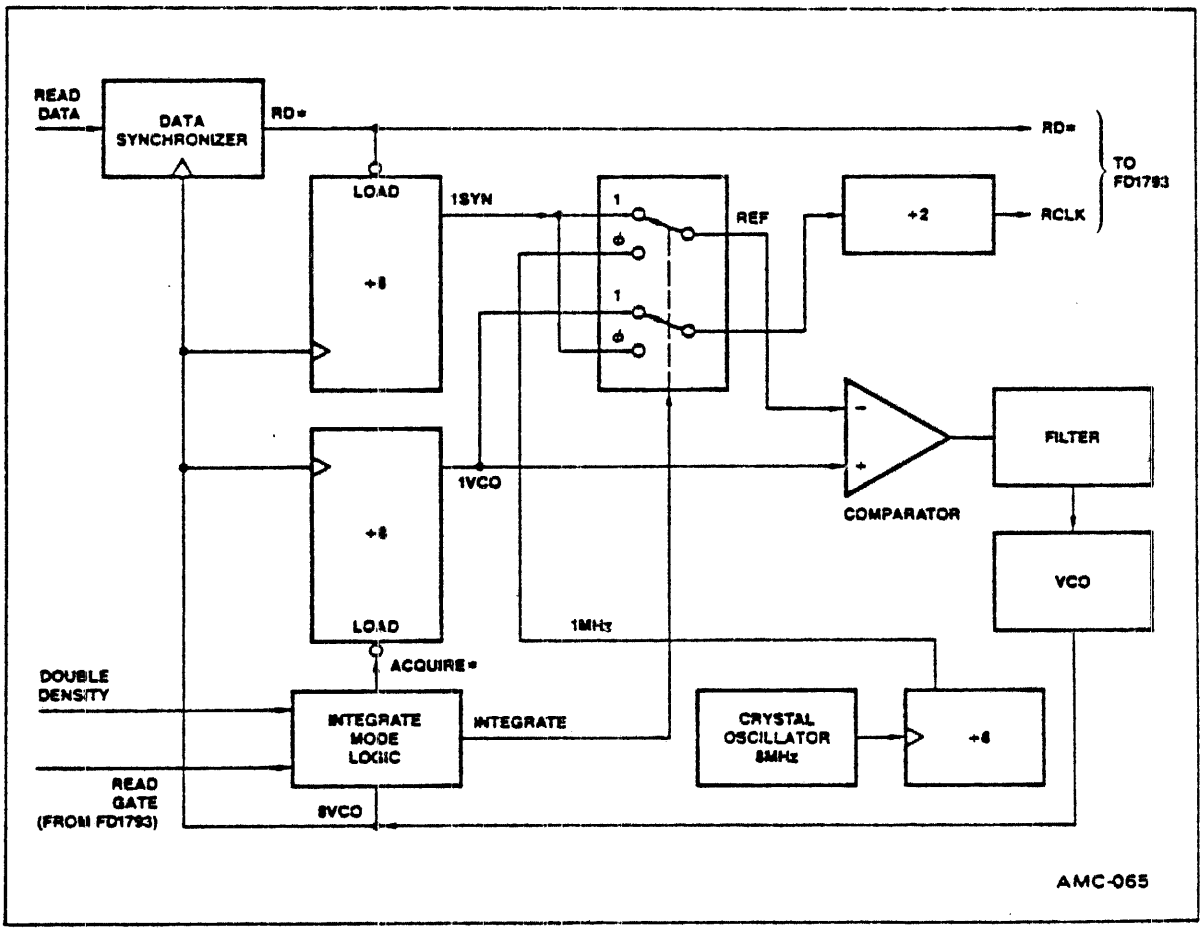


Figure 4-6. Phase Lock Loop Block Diagram (Standard Floppy Only)

The phase lock loop operates in a data-lock mode (integrating phase-locked counter) or in a crystal-lock mode (counter separator). Read operation starts with the phase lock loop in crystal-lock mode. Crystal lock mode holds the VCO frequency to within 3 percent of nominal. Following four bytes of zeros from the SYNC field, the FD1793 generates the READ GATE signal. If the Am95/6120 is in double density mode and the U34 device is installed, the Acquire (ACQ*) signal is generated. The period of one ACQ* pulse is the same as one Read Data (RD) pulse. The INTEGRATE signal is generated at the trailing edge of ACQ*, and is used to switch the phase lock loop to data-lock mode. The following 12 bytes of read data zeros are used to lock the loop phase to the read data signal. Timing is shown in figure 4-7.

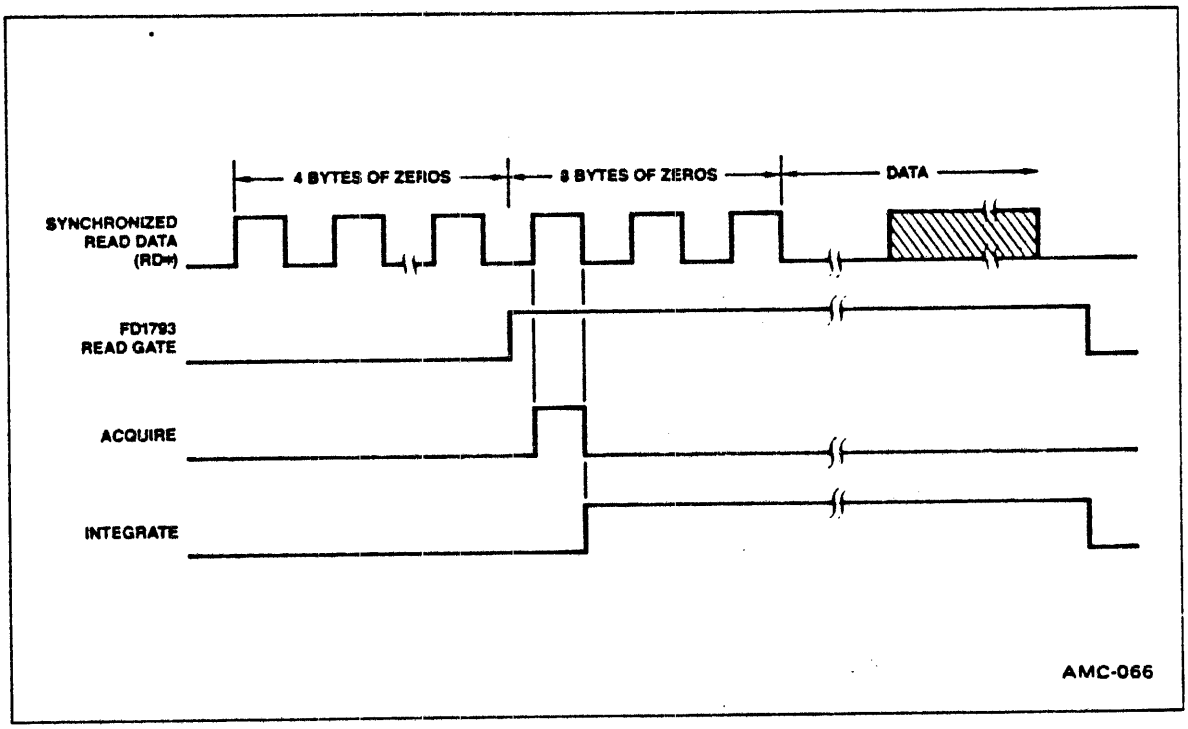


Figure 4-7. Phase Lock Loop Mode Timing

4-13. MAILBOX REGISTERS

The mail box registers store eight bits each. Each register has dual access so that R0, R1, R2, and R3 are written into from the host system and read by the on-board CPU. R4 is written into from the on-board CPU and read by the host system. R0, R1, R2, and R3 consists of two, 4-bit by four, read/write register files. R4 is an 8-bit D-register. A description of the mailbox function is included in section 3.

4-14. LSI CIRCUITS

The remainder of the circuits shown in the block diagram are LSI devices. These consist of the 8085 microprocessor, the 9517 DMA controller, and the FD1793 disk controller. Refer to the appropriate catalog for description of these devices.

4-15. Software Access to On-Board Functions

The factory supplied firmware controls on-board functions through I/O operation of the on-board CPU. These functions, including I/O addresses are listed in table 4-1.

TABLE 4-1. ON-BOARD I/O ADDRESSES

FUNCTION	ADDRESS	COMMENT
Board Functions		
Status Register	48H	Read
Command Register	48H	Write
System Reset (Toggle)	49H	Write
Start FD1793 Reset	49H	Read
DMA, PAGE REGISTER	4AH	Write
Stop FD1793 Reset	4AH	Read
Reset COMMAND-IN Flip Flop	4BH	
Reset End-of-Process Flip Flop	4CH	
Load Drive Select Register	4DH	Write
FDC Board Reset	4FH	
DMA Controller Functions		
Address Register CH0	10H	R/W
Word Count Register CH0	11H	R/W
Address Register CH1	12H	R/W
Word Count Register CH1	13H	R/W
Address Register CH2	14H	R/W
Word Count Register CH2	15H	R/W
Address Register CH3	16H	R/W
Word Count Register CH3	17H	R/W
Status Register	18H	Read
Command Register	18H	Write
Request Register	19H	Write
Single Mask Register	1AH	Write
Mode Register	1BH	Write
Clear Byte Pointer (flip-flop)	1CH	
Temporary Register	1DH	Read
Master Clear	1DH	Write
All Mask Register	1FH	Write

TABLE 4-1. ON-BOARD I/O ADDRESSES (Cont.)

FUNCTION	ADDRESS	COMMENT
Mailbox Register		
R0 Host to FDC	30H	Read
R1 Host to FDC	31H	Read
R2 Host to FDC	32H	Read
R3 Host to FDC	33H	Read
R4 FDC to Host	33H	Write
Floppy Disk Controller (FD1793)		
Status Register	00H	Read
Command Register	00H	Write
Track Register	01H	R/W
Sector Register	02H	R/W
Data Register	03H	R/W

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter contains information to maintain and adjust the Am95/6120 FDC board. The information includes service and repair assistance information. VCO adjustment procedures, and service diagrams consisting of schematics and board component layouts.

5-2. SERVICE AND REPAIR ASSISTANCE

Service and repair assistance can be obtained from Advanced Micro Computers by contacting the AMC Field Service Department in Santa Clara, California at one of the following numbers:

Telephone: (408) 988-7777

Toll Free: (800) 672-3548 California

(800) 538-9791 U.S.A. (except California)

If it is necessary to return a product to Advanced Micro Computers for service or repair, contact the Field Service Department at the previously listed telephone number. A Return Material Authorization number will be provided along with shipping instructions and other important information that will help AMC provide you with fast, efficient service. When reshipment is due to the product being damaged during shipment from AMC, or when the product is out of warranty, a purchase order is required for the AMC Field Service Department to initiate the repair.

Prepare the product for shipment by repackaging it in the original factory packaging material, if available. When the original packaging is not available, wrap the product in a cushioning material (such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, New Jersey) and enclose in a heavy-duty corrugated shipping carton. Seal the shipping carton securely, mark it FRAGILE, and ship it to the address specified by the AMC Field Service Department.

Customers outside of the United States can contact an AMC Sales Office or Authorized AMC Distributor for directions on obtaining service or repair assistance.

5-3. COMPONENT LOCATIONS

Figure 5-1 is the component location diagram.

5-4. MAINTENANCE

5-5. TEST POINTS

Test points are provided at the P3/P4 edge of the board. These points are marked 18, 19, 20, 21, 22, and 23. Each test point consists of two pins, with the pin nearest the board edge being the active pin, and the corresponding pin away from the board edge being the reference ground. Pins 18, 19, 20, and 21 provide access to the STAT0, STAT1, STAT2, and STAT3 board-control-register status signals. Pins 22 and 23 are used for the 500 KHz frequency test point and VCO control voltage test point.

5-6. EDGE CONNECTOR CONTACT MAINTENANCE

The board connectors must be kept clean. Intermittent operation can sometimes be cleared by retracting the board from the socket and then reseating it. The contacts can be cleaned with a commercial grade of isopropol alcohol or a fluorocarbon solvent. Use a clean cloth, saturated in the cleaning solution, and gently wipe the contacts.

5-7. VCO ADJUSTMENT

The VCO is factory adjusted and should not require field adjustment. Any attempt to adjust the VCO frequency in the field will void the warranty. The following procedure is included for out-of-warranty maintenance, when one or more of the phase-lock-loop components are replaced during repair and the VCO frequency is incorrect.

Allow the board to warm up for at least 10 minutes. Install jumper 16. Connect a dc voltmeter across R34. Adjust "Trimpot" R11 for a minimum voltage reading. The voltage must be less than 10 millivolts. Remove jumper 16.

5-8. SERVICE DIAGRAMS

The Floppy Disk Controller component locations are shown on the assembly drawing, figure 5-1.

Schematic diagrams of the Floppy Disk Controller are shown in figure 5-2 through 5-6. Active-low (logical 0) signals are specified by an asterisk (*) following the signal name.

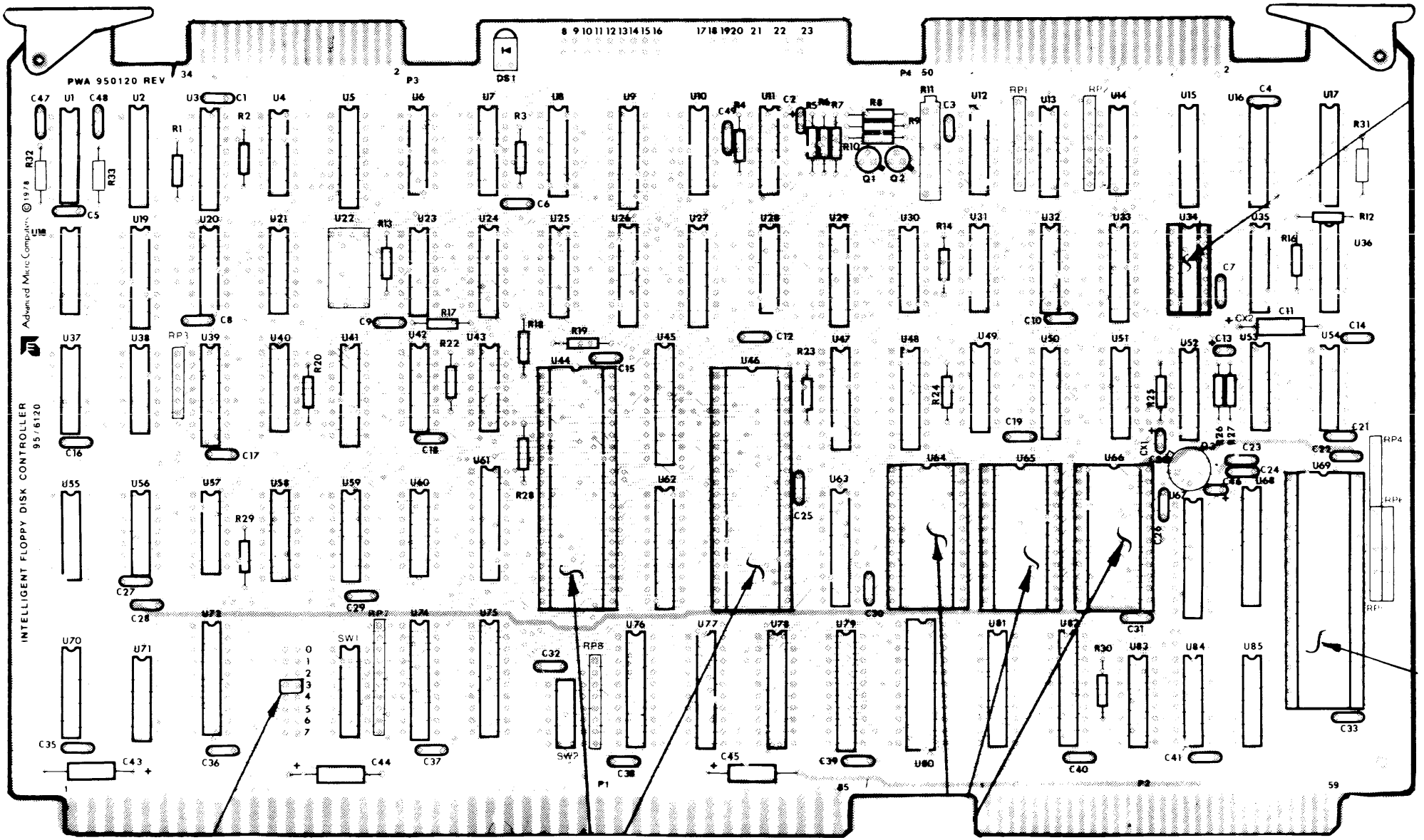


Figure 5-1. Component Locations

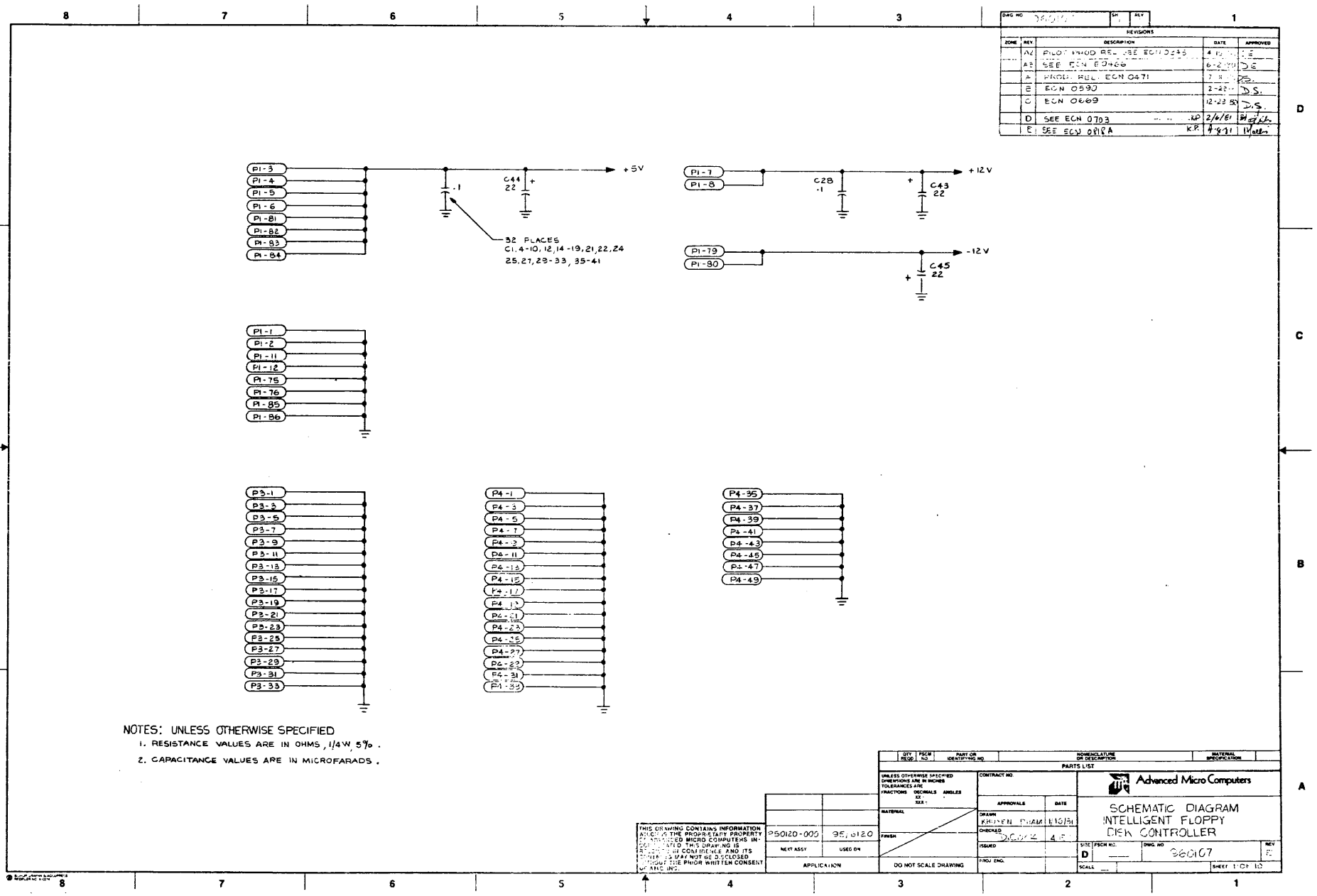


Figure 5-2. AMC 950120-000 Schematic, Sheet 1

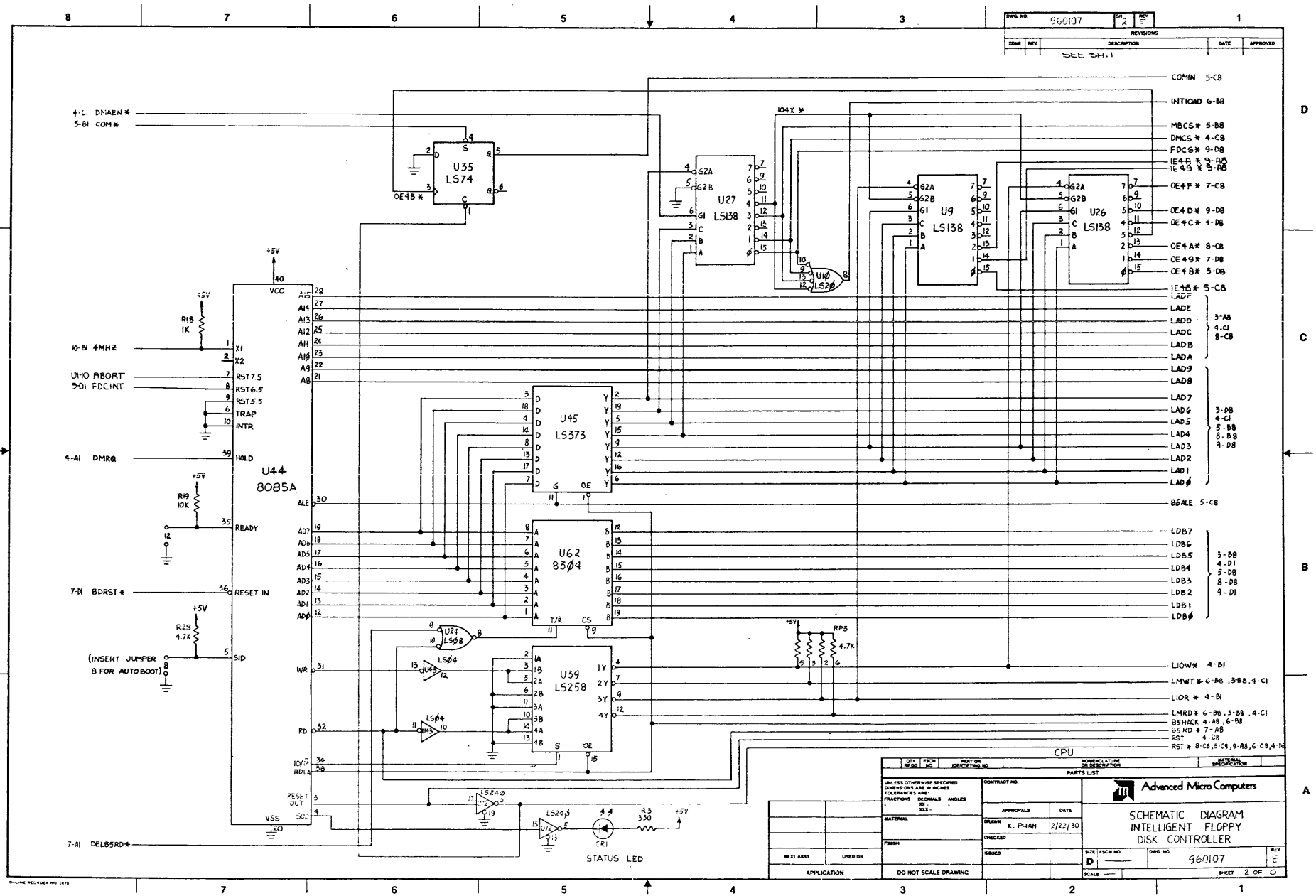


Figure 5-3. AMC 950120-000 Schematic, Sheet 2

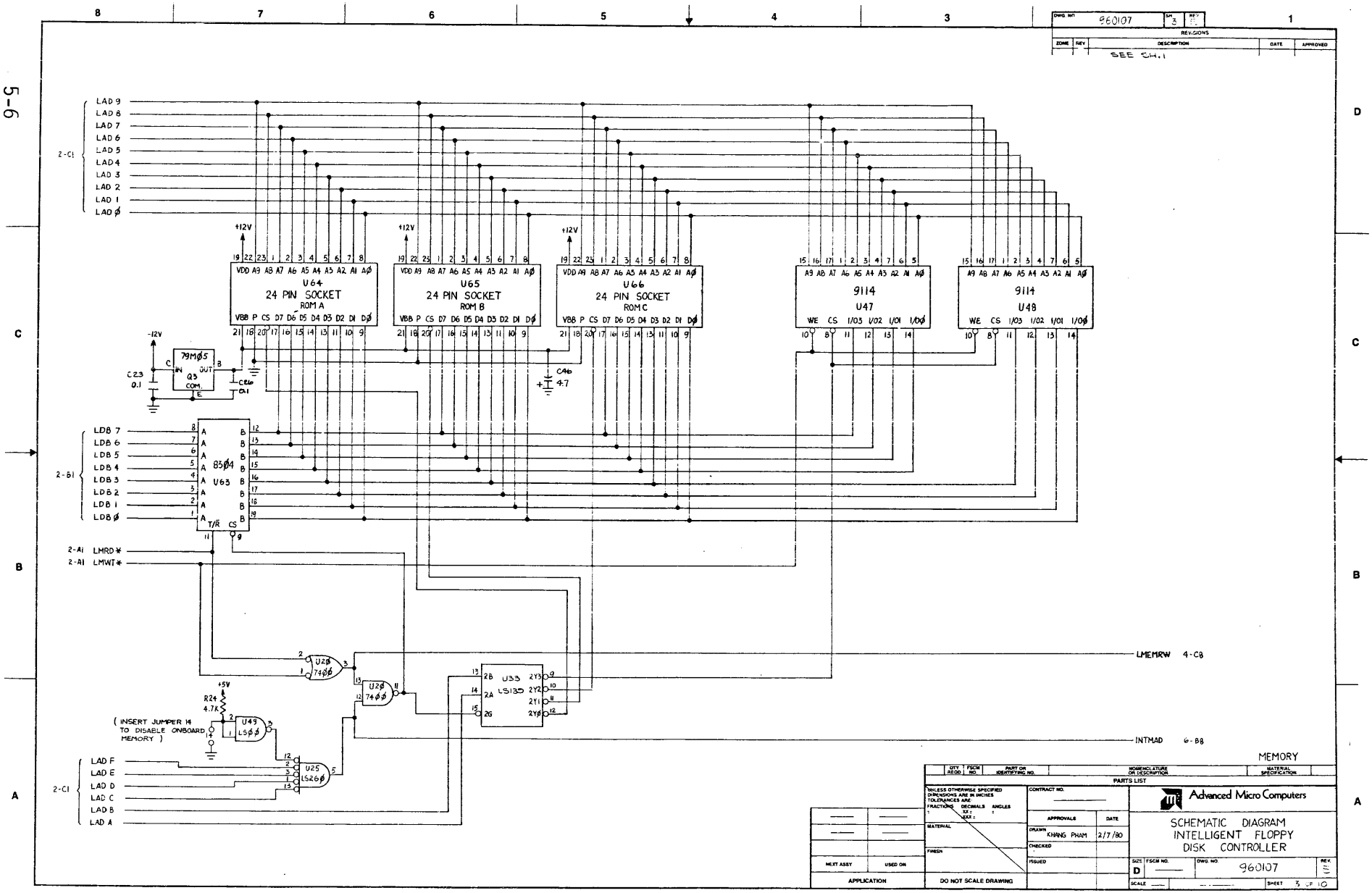


Figure 5-4. AMC 950120-000 Schematic, Sheet 3

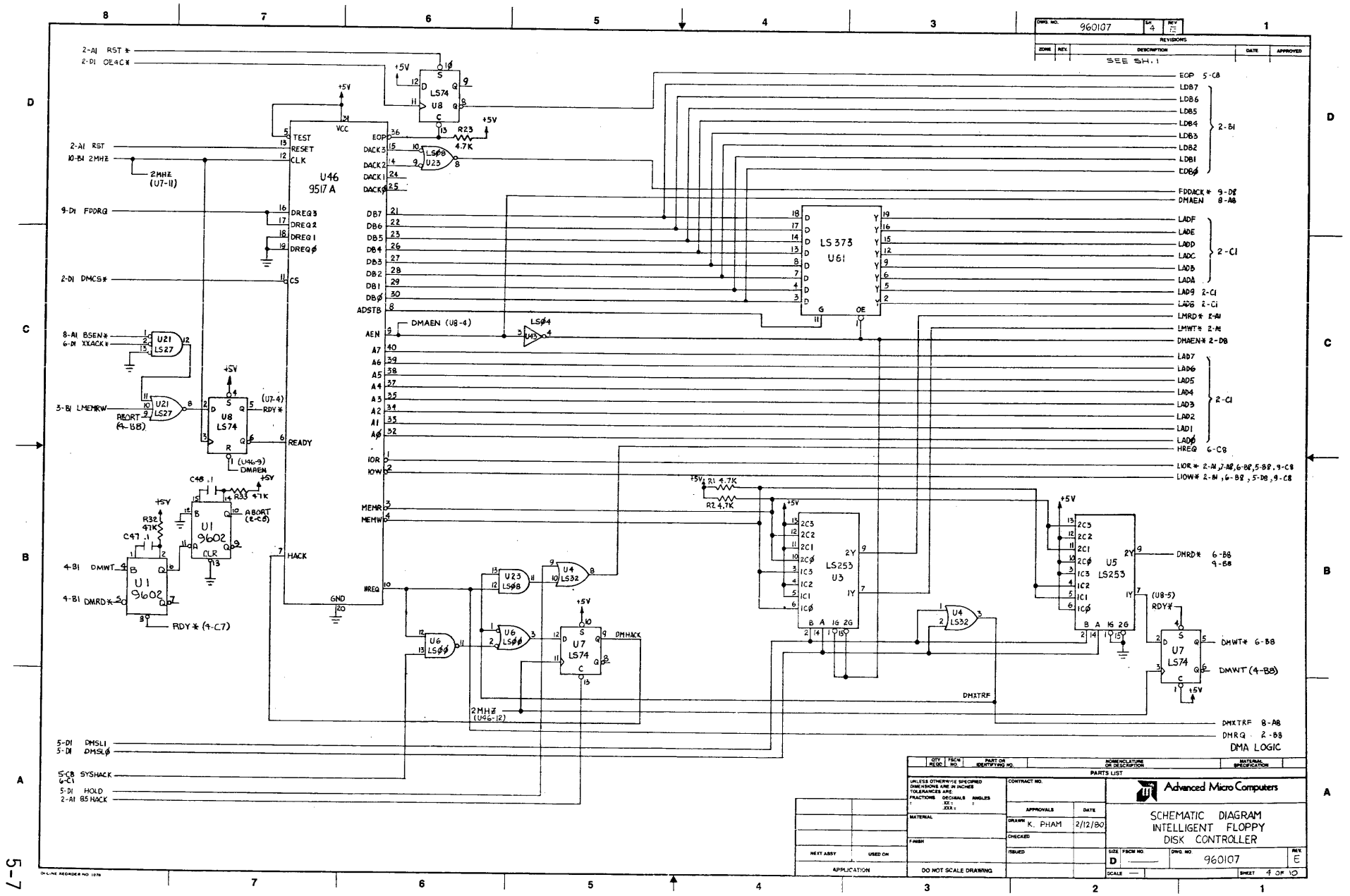


Figure 5-5. AMC 950120-000 Schematic, Sheet 4

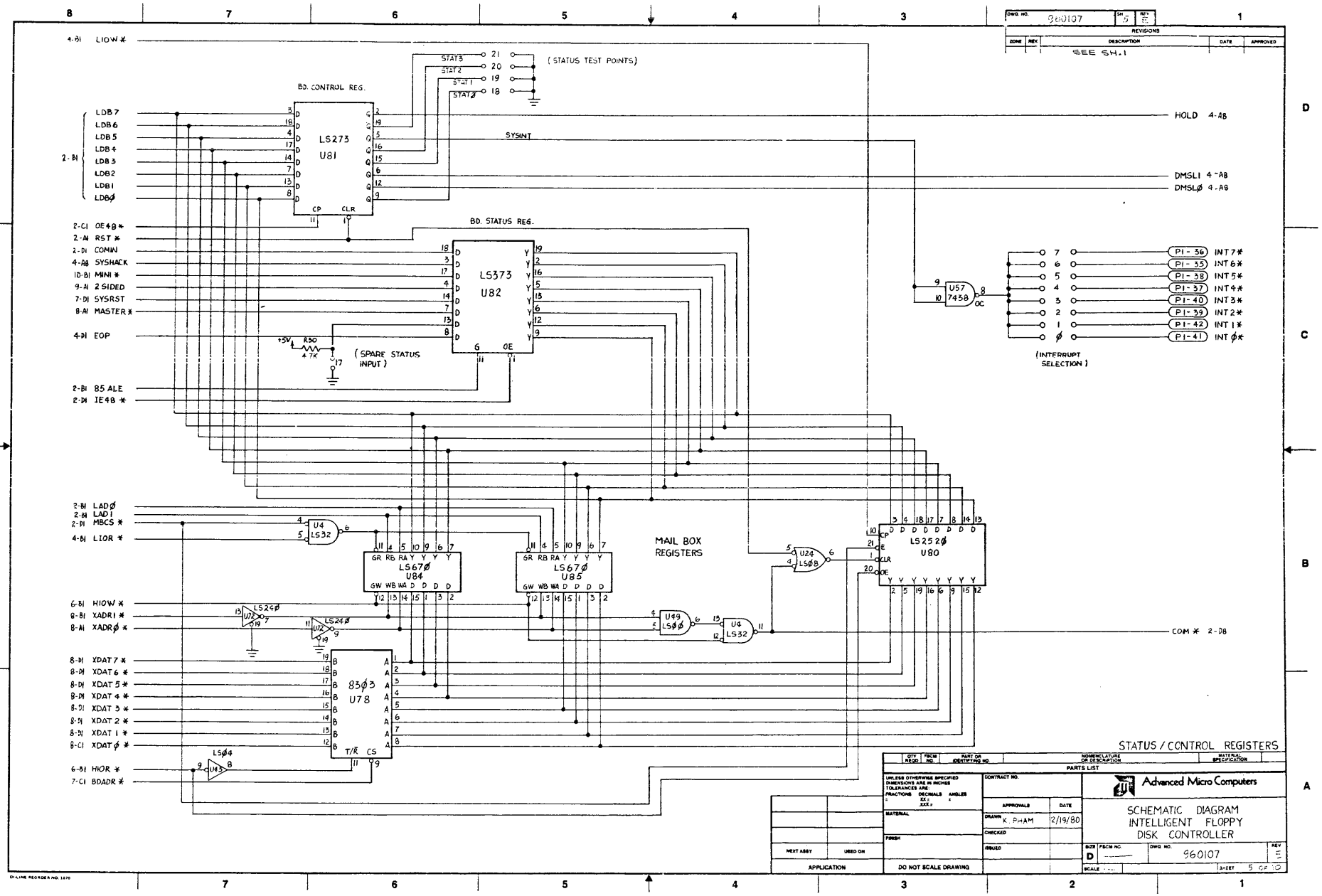


Figure 5-6. AMC 950120-000 Schematic, Sheet 5

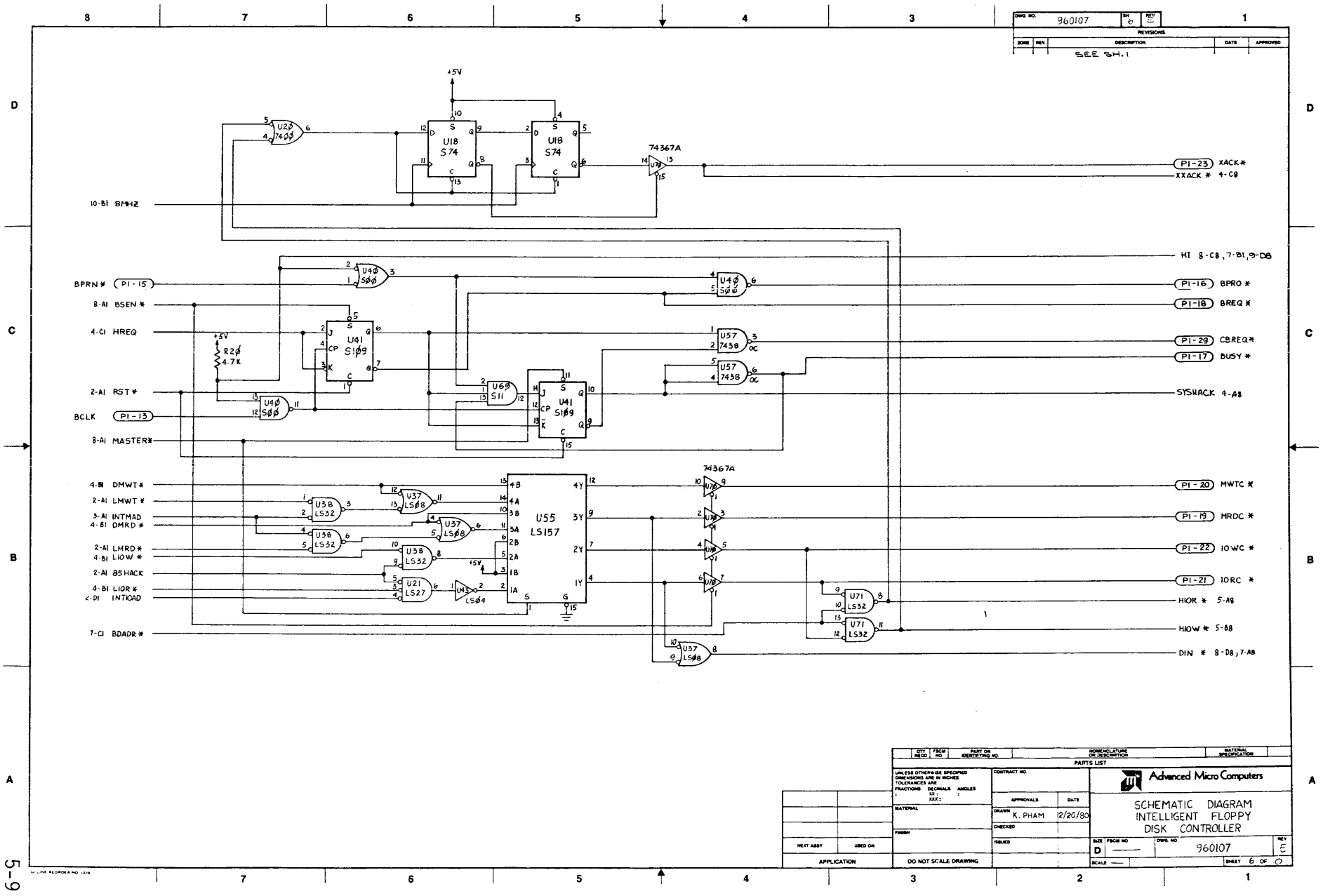


Figure 5-7. AMC 950120-000 Schematic, Sheet 6

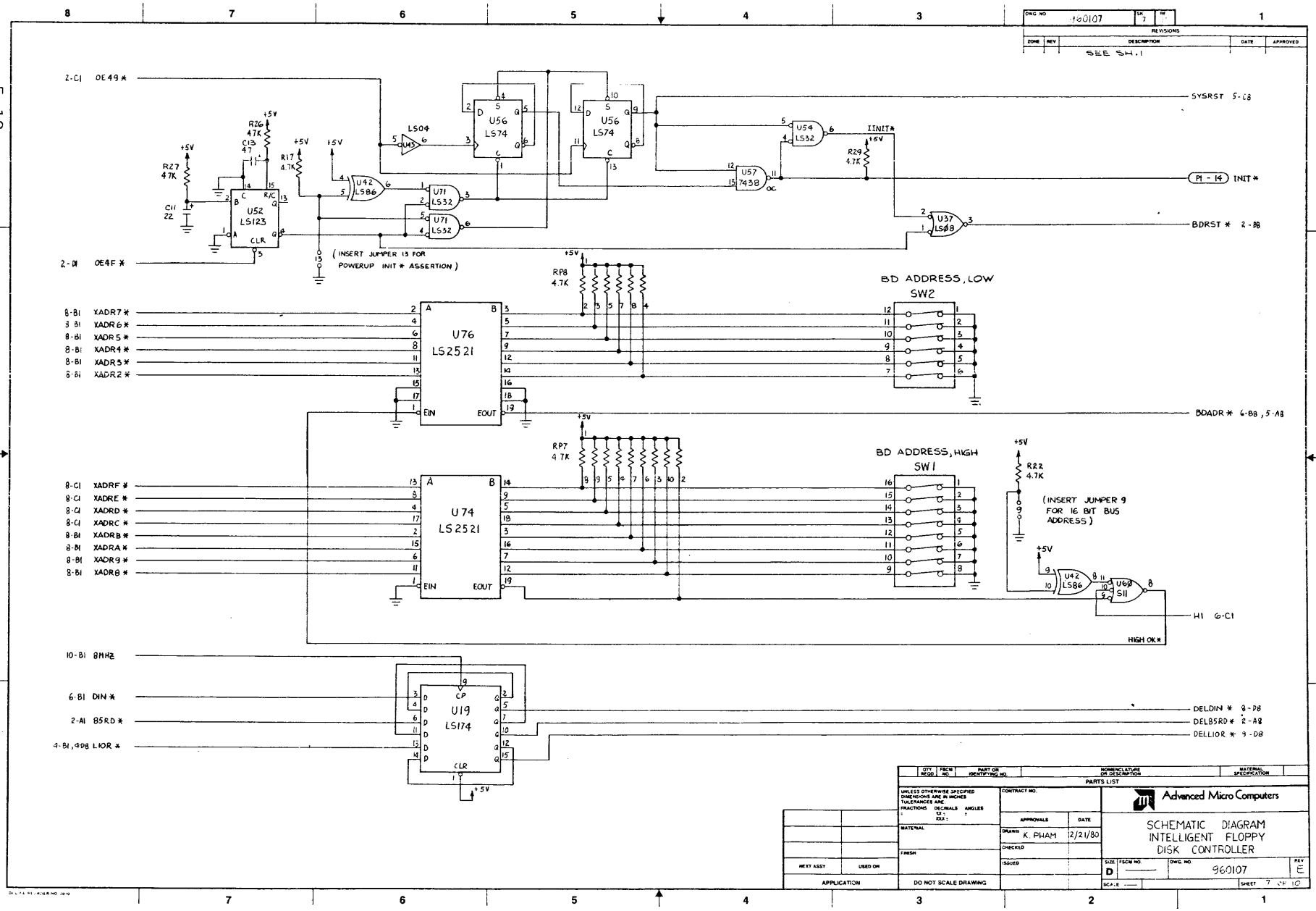


Figure 5-8. AMC 950120-000 Schematic, Sheet 7

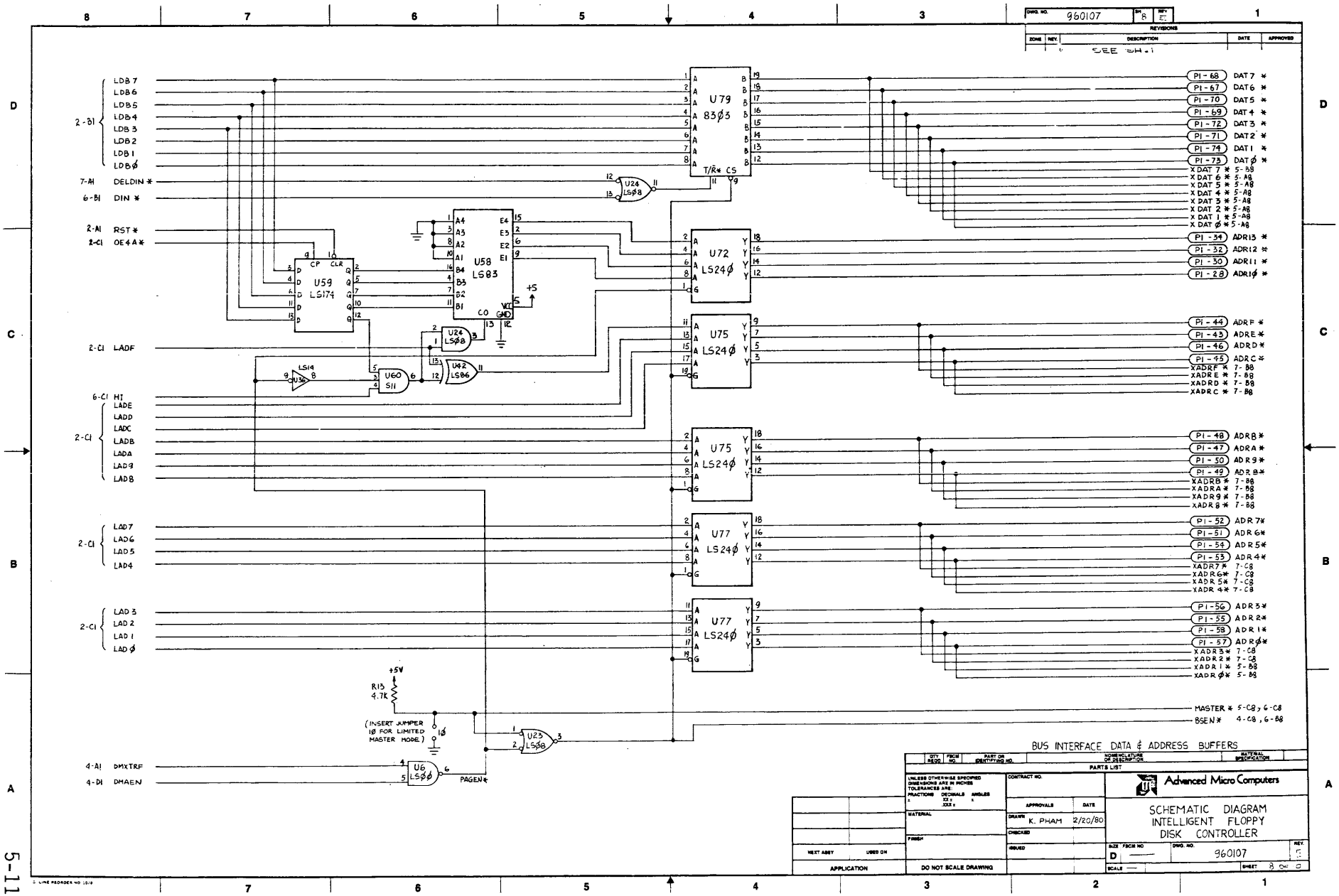


Figure 5-9. AMC 950120-000 Schematic, Sheet 8

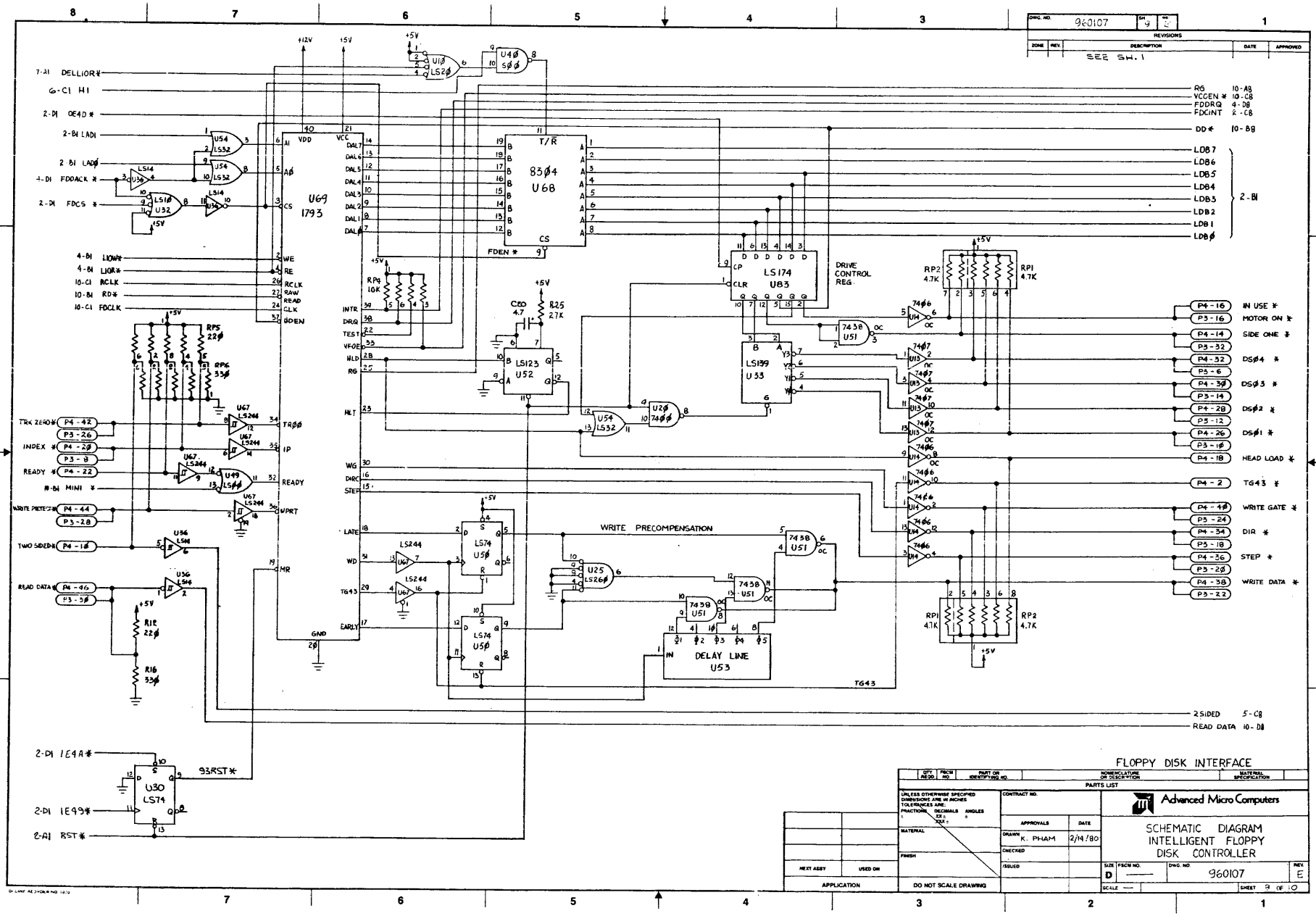


Figure 5-10. AMC 950120-000 Schematic, Sheet 9

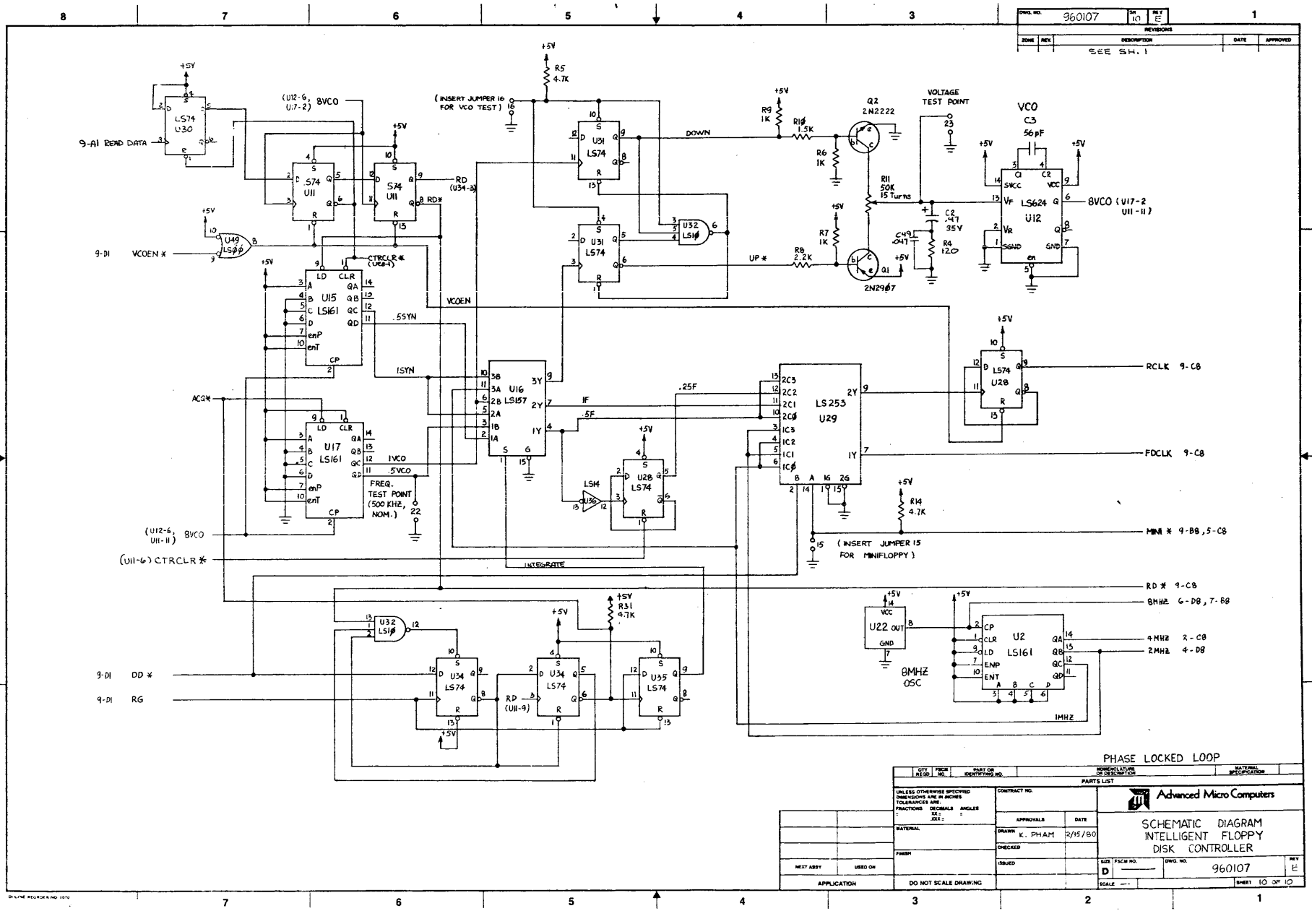


Figure 5-11. AMC 950120-000 Schematic, Sheet 10

COMMENT SHEET

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Publications Department
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Santa Clara, CA 95051

TITLE: Am95/6120 Dual-Density Floppy Disk Controller User's Manual
PUBLICATION NO: 059901341-001 Revision D

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