Cromemco

3100 & 3101 TERMINAL

SERVICE MANUAL

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SECTION IV

Theory of Operation

4.1 INTRODUCTION

This section contains the theory of operation for the BEEHIVE B150 Terminal. This discussion is presented as a functional description at a detailed block diagram level referencing appropriate functional blocks on the diagrams.

4.2 GENERAL FUNCTIONAL DESCRIPTION

The B150 consists of four basic functional components, Power Supply, Monitor, Keyboard and Main Logic Board. Figure 4-3 shows the basic functional flow diagram of the terminal. These functions are briefly described in the following paragraphs.

4.2.1 Power Supply

The Power Supply provides the required, regulated DC voltages to the terminal. This assembly will operate on 100, 115, or 230 VAC 50/60 Hz power (see Section II).

4.2.2 Monitor

The Monitor Assembly includes a 12 inch (30.5 cm), diagonally measured, CRT and its supporting solid-state circuitry. The Monitor is controlled by the vertical and horizontal synchronization signals, and the video signals generated on the logic board. A full screen of information consists of 24 lines of 80 characters and a one raster scan between lines. Brightness and contrast adjustments are provided by external potentiometers located on the rear panel, (see Figure 2-2, Section II). Other monitor adjustments are discussed in Section V and in Appendix A.

4.2.3 Keyboard

The keyboard is the input device used by the operator to communicate with the terminal. The keyboard contains the switches and supporting circuitry to generate the appropriate control signals and ASCII codes utilized in the B150 terminal. The keyboard conforms to the proposed ANSI keyboard standard for data keys, but has been expanded to facilitate the capabilities of the B150.

4.2.4 Logic Board

The Logic Board contains the major function and control circuits in the B150 termina. It also holds all of the DC voltage regulators to power the unit, with the exception of the +5 V regulator. The basic operations accomplished by the main logic board are: Generation of data and control signals for the monitor, interaction with the keyboard, control of the data sent between the B150 and any external device, and generation of the basic timing signals essential for the operation of the terminal.

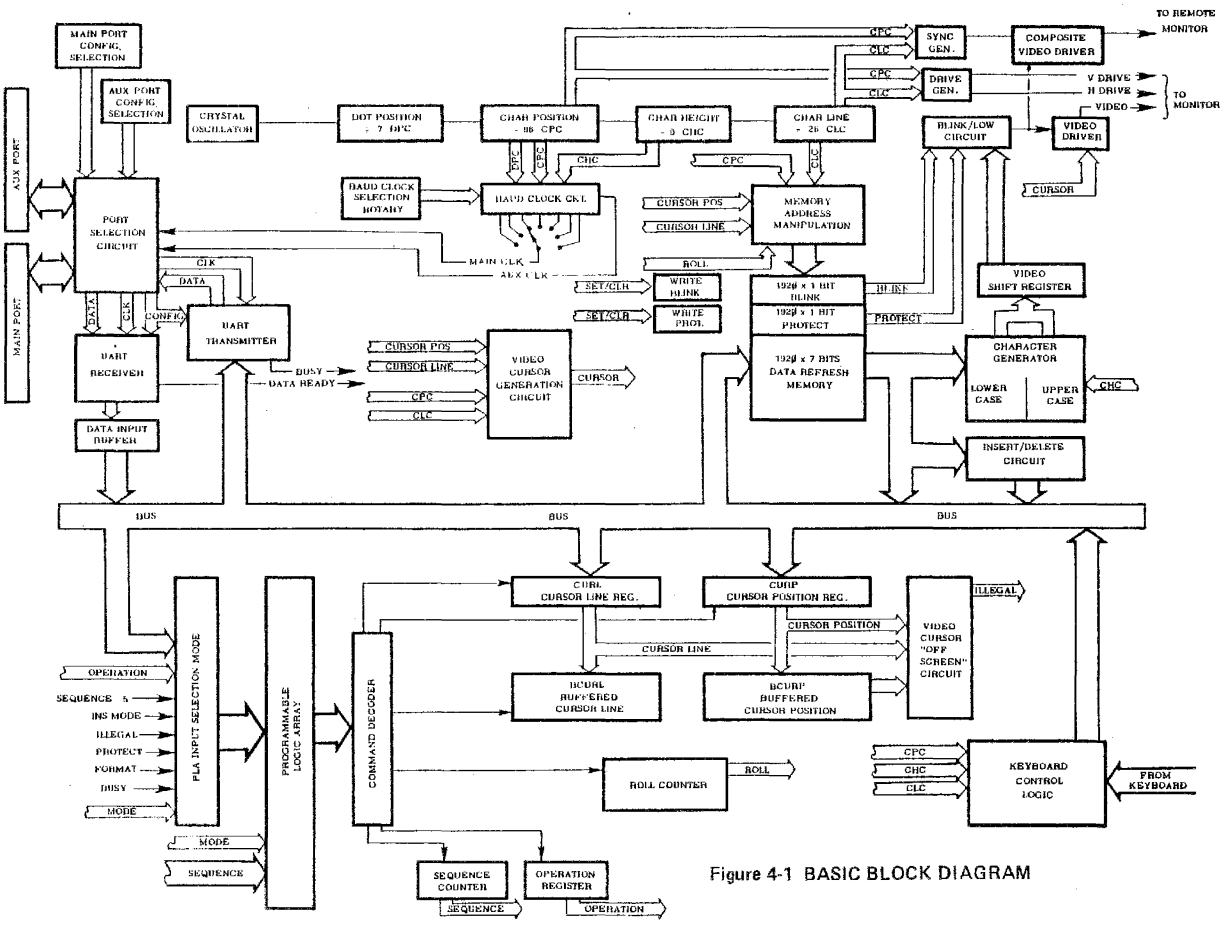


Figure 4-1 BASIC BLOCK DIAGRAM

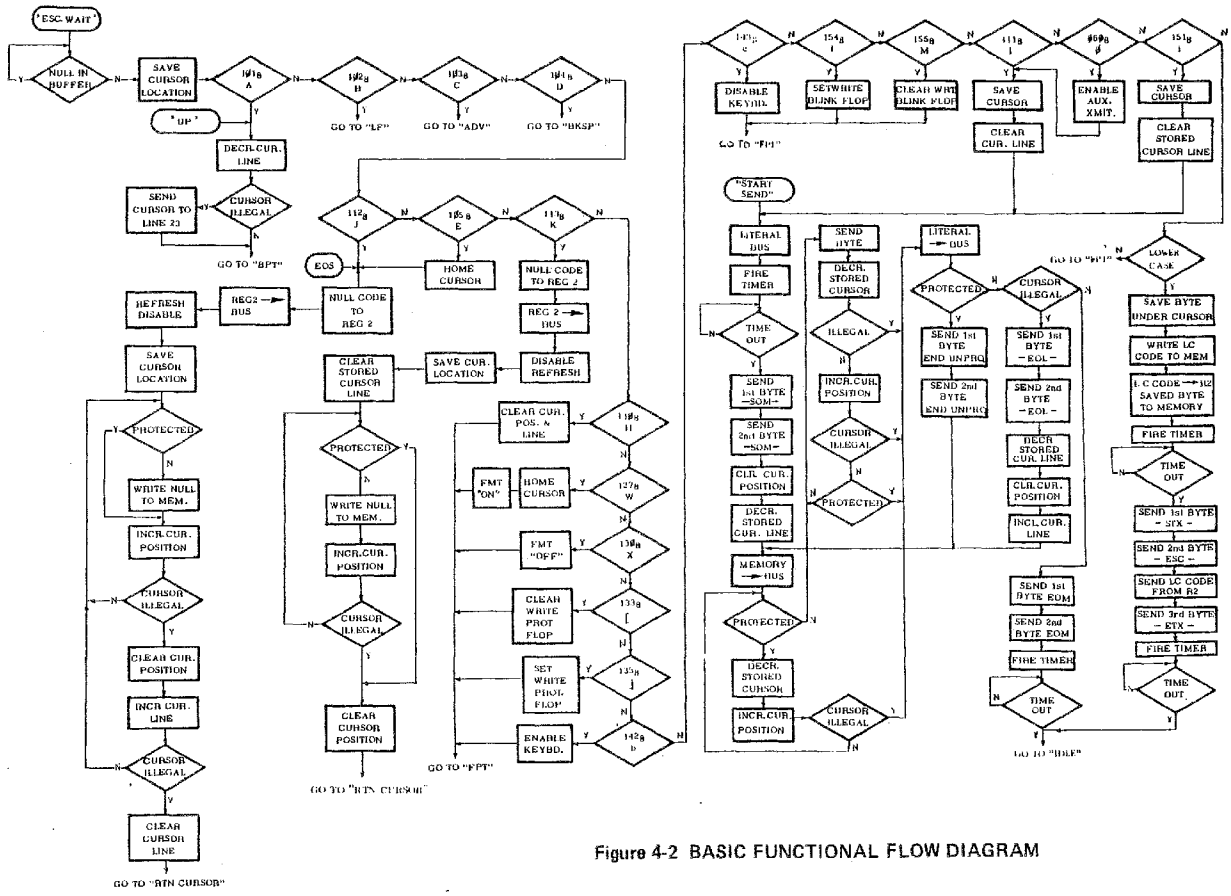


Figure 4-2 BASIC FUNCTIONAL FLOW DIAGRAM

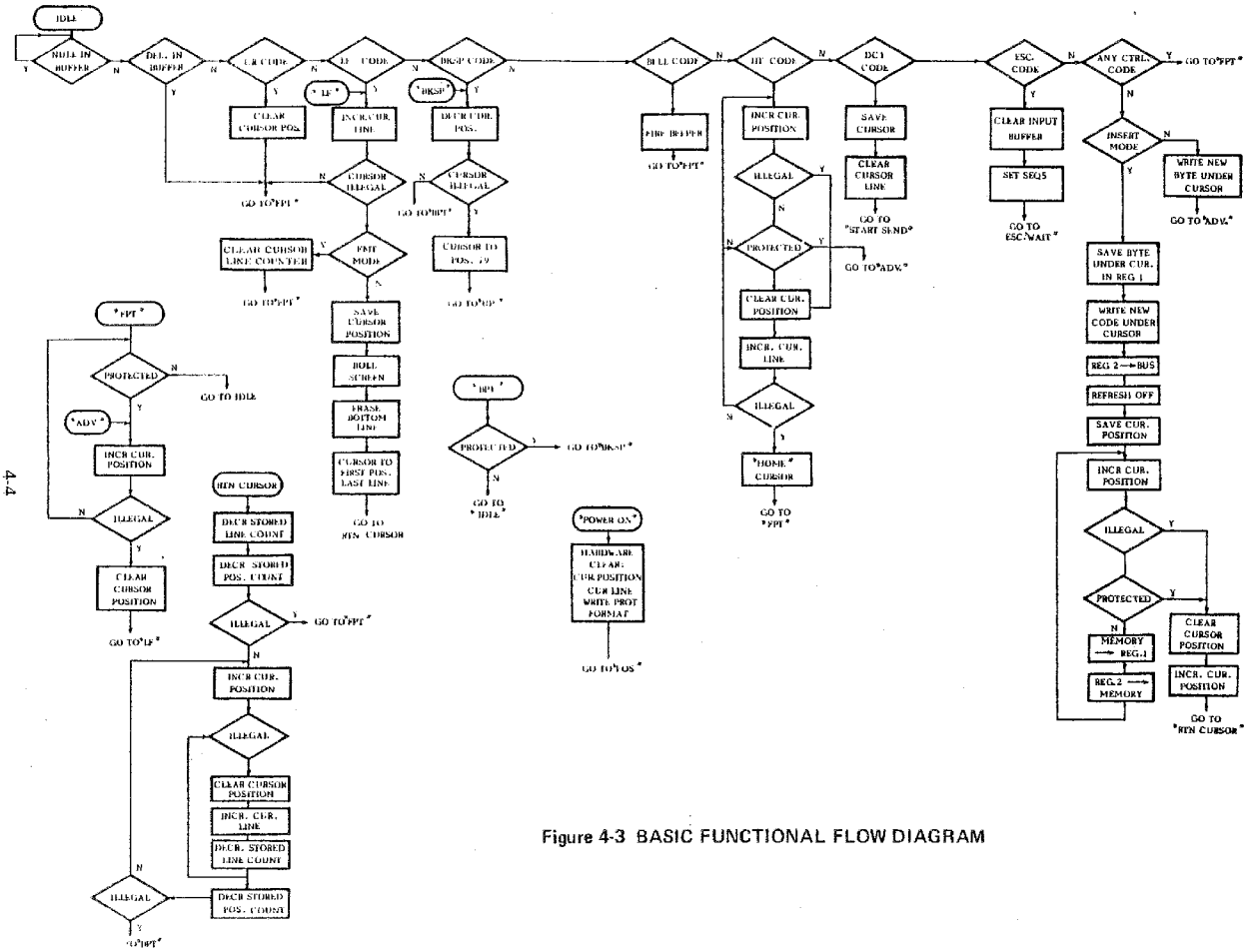


Figure 4-3 BASIC FUNCTIONAL FLOW DIAGRAM

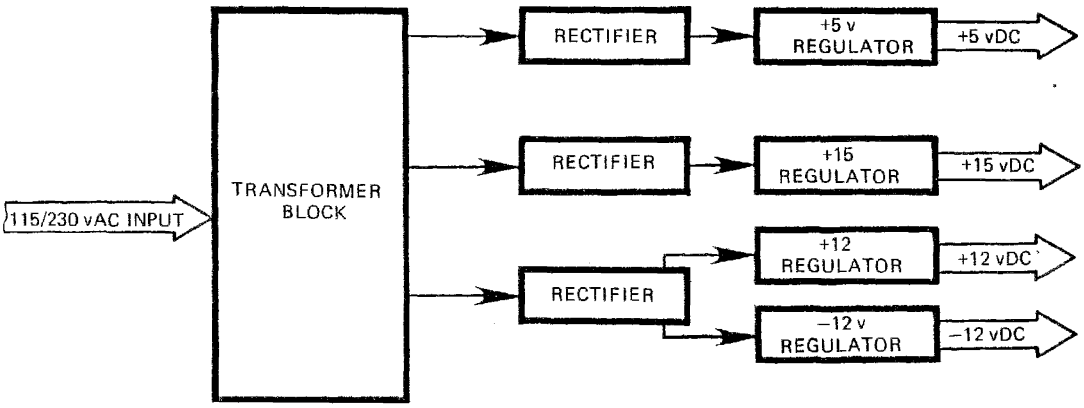


FIGURE 4-4 POWER SUPPLY BLOCK DIAGRAM

4.3 DETAILED FUNCTIONAL DESCRIPTION

A detailed discussion of the BEEHIVE B150 terminal operation is contained in the following paragraphs. The Subassembly components of the terminal are functionally interdependent, however, the isolation of various functions to the responsible subassembly is relatively simple. The function of each subassembly is also described. Schematic diagrams are provided in Section VI of this manual.

4.3.1 Power Supply

The Power Supply provides +5, +15, +12, and -12 VDC voltages to the circuitry from a 115 or 230 VAC source at 50 or 60 Hz. Figure 4-4 is a block diagram of the Power Supply subassembly. The DC regulators utilized are overcurrent and thermally protected.

The power applied to the Power Supply is stepped down in voltage. The transformer output voltages are rectified by three bridge circuits. The output from the rectifiers and filters provides power to the +5, +15, +12, and–12 VDC regulator circuits.

4.3.2 Monitor

The monitor displays data on the CRT in a pattern determined by the vertical and horizontal synchronization signals, and the video information driving signals. A +15 VDC voltage is applied by the Power supply to the Monitor. Appendix A presents general and detailed data on the Monitor Assembly.

4.3.3 Vertical Synchronization

Vertical synchronization is applied to the vertical oscillator and triggers it at the vertical refresh rate determined by the driving logic. The vertical frequency is stabilized by the vertical frequency control, which determines the point of oscillation. The output pulse of the vertical oscillator is applied to the driver amplifier which shapes the pulse and is controlled by the vertical linearity control. The output of the driver amplifier is applied to the vertical driver by way of the height control. The vertical driver output pulse is applied to the yoke of the CRT and causes vertical deflection. The refresh rate is 50 - 60 Hz. switch selectable.

4.3.4 Horizontal Synchronization

The horizontal synchronization pulses are applied to the horizontal amplifier where they are amplified and applied to the horizontal driver. The output of the horizontal drive is applied through the width coil to the yoke, where it causes the horizontal deflection. The horizontal deflection signal is also applied to the flyback transformer. The horizontal deflection signal is stepped up to approximately 12 KV where it is then rectified, filtered and applied to the anode cap of the CRT to provide the high voltage required.

4.3.5 Video Information

The Video Information is applied to the video amplifier by way of the contrast control, external to the monitor. The video information signal from the video amplifier is applied to the cathode of the CRT gun to cause an On/Off condition corresponding to light patterns of the screen. The brightness control is external to the monitor and varies the voltage on the accelerating grid of the CRT.

4.3.6 Keyboard

The keyboard is compatible with ANSI standards. Section III defines the ASCII codes available and shows the keyboard layout.

The keyboard enables the operator to manually input information to the terminal. When a key is depressed, the keyboard logic generates the corresponding 7-bit ASCII code and presents the data in parallel form to the keyboard data lines. After a short delay for debouncing, the strobe is driven to its active level and held there as long as the key is held down. For those keys which auto repeat, the strobe line is pulsed at a 15 character per second rate. The BREAK key is not encoded, but is a function line that is driven low for approximately 400 milliseconds when the key is depressed.The following keys cause special 8-bit (non-ASCII) codes: AUX SEND, ↓ , →, ←, ↑ , CLEAR/HOME, SEND, EOS, EOL, and DELETE CHAR. These codes are used internal to the CRT only and are not transmitted.

4.3.7 Display Organization

The main timing chain (oscillator, dot position counter, character position counter, character height counter, and character line counter)

defines the configuration of the display on the CRT. There are 27 lines, 3 of which are used for vertical retrace and 24 of which are used to display characters. The 27 lines are composed of ten scans each. Each scan being composed of 7 x 10 dot matrix field which contains a 5 x 7 character matrix for the displayed character.

Oscillator The oscillator is crystal controlled with a frequency of 10.8864 MHz. Two 74H04's are connected in series by a 100pf capacitor. Each 74H04 has a 1 Kohm feedback resistor around it. A 10.8864 MHz crystal is connected from the input of the first 74H04 to the output of the second. The output of the oscillator is buffered, inverted and fed to the Dot Position Counter.

Dot Position Counter This divide-by-seven counter defines each of the seven dots required to compose one character. The outputs of this four stage counter are labeled DPC1, DPC2, DPC4, and DPC8. The Counter actually presets to a count of 10, counts up through the overflow point at 15 to a count of zero, and presets then back to a count of 10. The Dot Position counter output, DPC8, drives the Character Position Counter.

Character Position Counter The Character Position Counter is composed of two binary-type counters that define 96 character times, each being seven dots wide. The output of the Character Position Counter drives the Character Height Counter.

Character Height Counter The Character Height Counter is a standard counter that defines 10 scans of 96 characters each, with each character being seven dots wide. The output of the Character Height Counter drives the Character Line Counter.

Character Line Counter The Character Line Counter is a binary counter that starts at a count of zero and counts to a maximum of 26 for a total of 27 character lines. The final output of this counter runs at the vertical refresh rate.

Horizontal and Vertical Drive The Horizontal Drive is started when the Character Position Counter leaves the video area of the scan and is active for the following 40 character times. The high active output of this flip-flop is sent to the monitor on pin 9 of connector J1.

The vertical drive is generated during the time that the Character Line Counter is decoding 24.

4.3.8 Cursor Location Counter

The Cursor Location Counter identifies the location of the cursor. This is a count made from the Cursor Line Counter, called CURL, and the Cursor Position Counter, called CURP. These two counters, in conjunction with the ROLL counter, are used to address the memory to determine the entry point of the next character. The cursor location counters are compared with the next character. The cursor location counters are compared with the Character Position Counter and the Character Line Counter to generate the signal called CNTR CURSOR. This signal is used to generate the cursor displayed on the CRT. Also associated with the cursor location counters is the appropriate circuitry to move the cursor up, down, right, left, home,etc. A LINE FEED code causes the Cursor Line Counter to increment by one. A CARRIAGE RETURN code clears the Cursor Position Counter.

With the terminal operating in FORMAT MODE, when the cursor is incremented off the bottom line, the cursor automatically wraps around to the top of the display, i.e., the Cursor Line Counter is reset to zero. However, if the terminal is not in FORMAT MODE, the display scrolls whenever the cursor increments from a count of 23.

A scroll is initiated by any of 3 functions if activated when the cursor is on the last line of the display and the terminal is not in FORMAT MODE:

a. LINE FEED or CTRL J
b. CURSOR DOWN or ESC B
c. If the cursor is on the last position of the last line.

    1. Cursor right

    2. Any displayable character

    3. Space

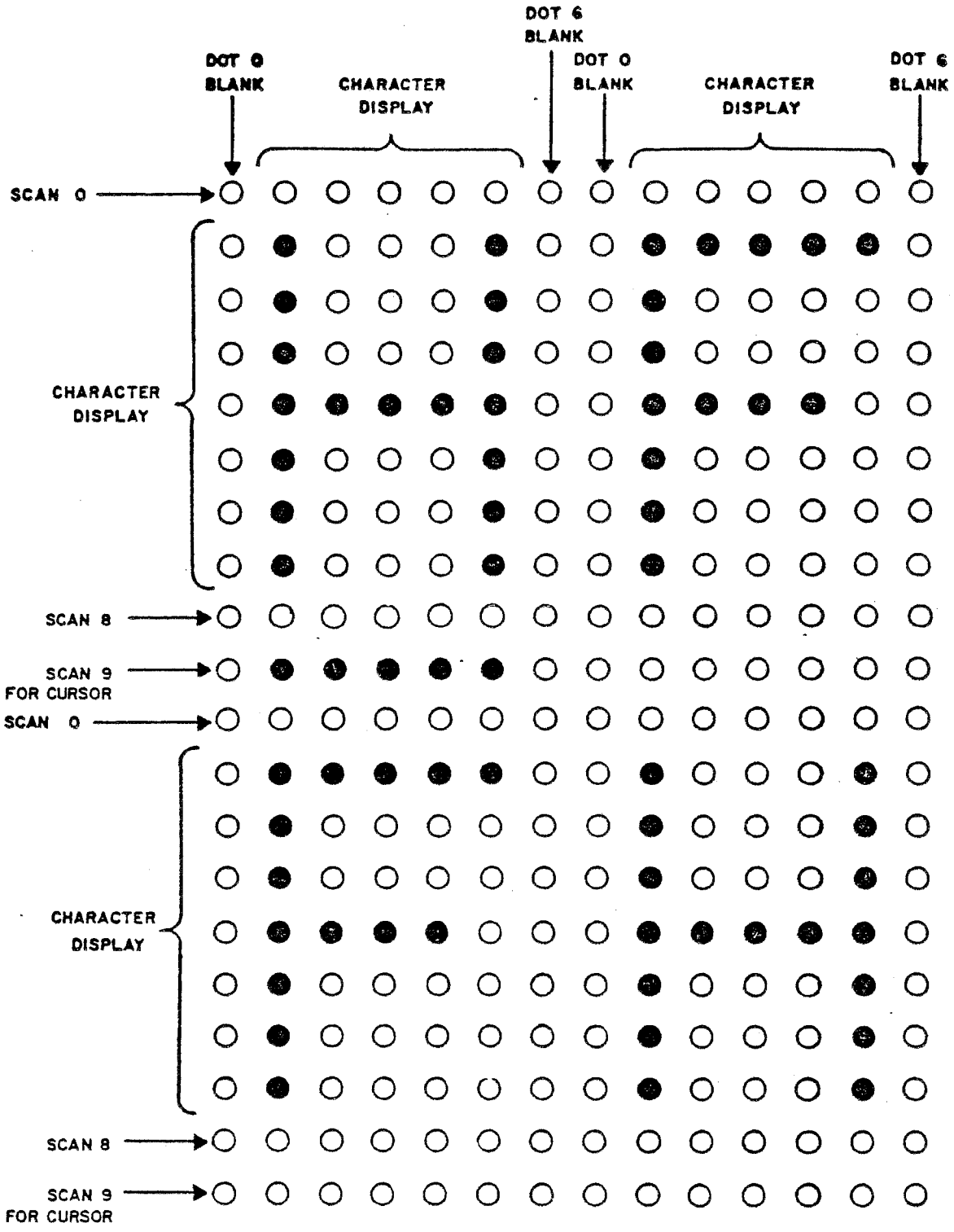


FIGURE 4-5

CHARACTER DOT MATRIX

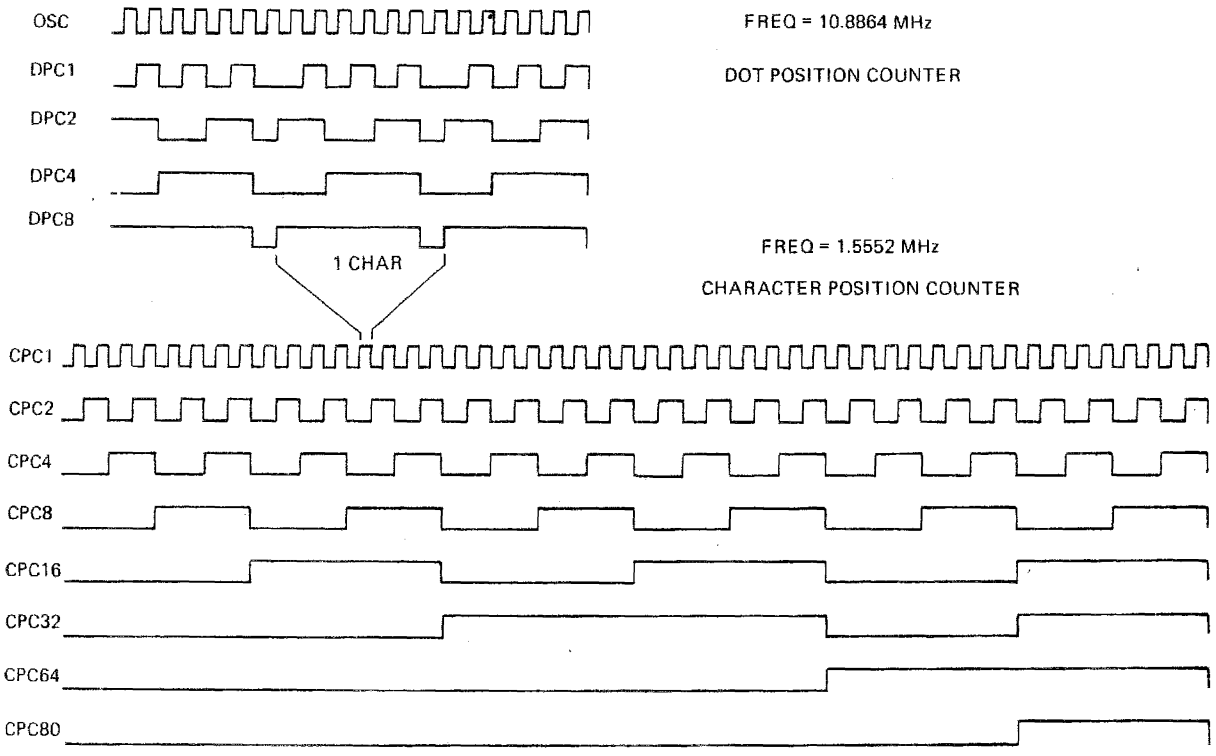


FIGURE 4-6 TIMING DIAGRAM

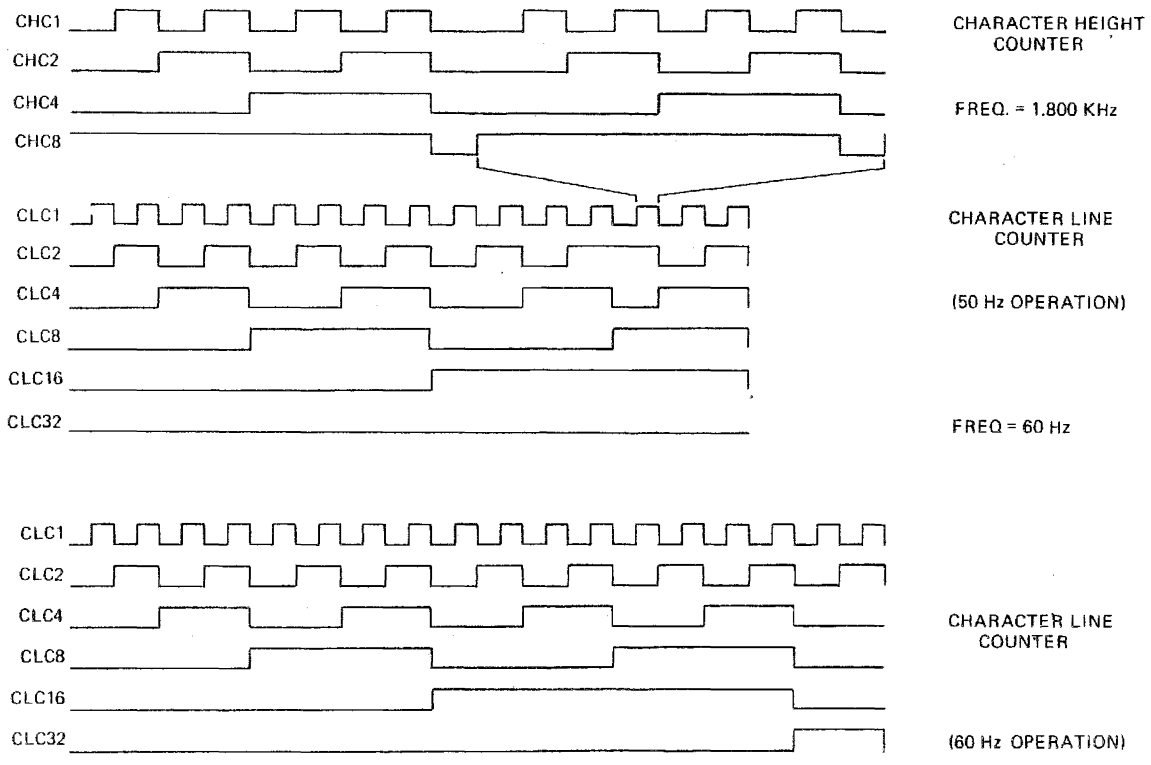


FIGURE 4-7 TIMING DIAGRAM

4.3.9 Memory

The page memory is actually a 2048 byte memory. Each byte consists of 9 bits: 7 for data, one for protect, and one for blink. Of these 2048 bytes, 1920 are displayable. The program does not have the capability of displaying or writing into the remaining 128. In order to write data into the page memory from the receiver, the memory address is muxed over to the cursor location registers and the signal WRITE is generated. The UART is then reset and is capable of receiving the next character. The page memory output is sent to the character generator input buffer at the proper time to generate the displayable characters. The program has the capability of shutting down the screen refresh for any given operation to increase the program operating time.

4.3.10 Character Generator

The Character Generator is a read-only memory (ROM) that is addressed by the character (in ASCII). The scan configuration and the character indicates the pattern desired on that scan. The nine-bit dot patterns are generated which form a portion of a character. The output of the character generator is applied to the parallel-to-serial video shift register.

4.3.11 Video Shift Register

The parallel-to-serial Video Shift Register is loaded with data by the low-active signal, DPC8, and is clocked by the main oscillator output. The dots are shifted out, mixed with cursor information, and blanking signals, and applied to the monitor through the CONTRAST control as video information.

4.3.12 Input/Output Operations UART (Receiver)

Data can be received by the B150 from one of three sources; from the two I/O interfaces into the receive side of the UART or from the keyboard through the transmit side of the UART to the receive side of the UART.

The UART is driven by a clock generated internally off the main counter chain. No separate oscillator is required. A rotary switch located on the back panel switches the clock rate for operation from 75 to 19200 baud. The times 16 clock is then applied to the transmitter and receiver of the UART.

The EIA line receiver receives data at RS 232C levels and gates them into the UART when the B150 is on-line. Through the same gating, data is brought in from the transmit side of the UART. The data is brought into the UART where it is converted to parallel (seven bits) data.

4.3.13 UART (Transmit)

The keyboard data lines for bits 1 through 7 are applied to the transmit input data lines along with the seven BUS lines. Also coming from the keyboard circuit is a load signal which triggers the UART to initiate the transmission. As the UART receives the character for transmission, it performs the appropriate parity generation, provides one or two stop bits, divides the X16 clock to get the baud rate, and transmits the character. The character is applied through an EIA RS 232C interface to the computer or modem. Also coming from the UART is output data at a TTL level which is applied to the receiver side of the UART through the previously mentioned logic. The EIA interface includes a Data Terminal Ready signal which indicates the status of the B150 to the computer and a Request to Send signal which indicates that the terminal has data to send to the computer. The Clear-to-Send line coming from the computer is monitored at the EIA RS 232C interface levels. It is received by a line receiver which converts it to TTL levels and applies it to the UART clock control circuit to control transmission. An optional times 8 clock (TTL levels) is available as part of the interface. The BREAK key is on the keyboard and enables a timer which holds the transmit data line in a spacing condition for a predetermined length of time.

4.3.14 Block Send Circuit

The Block Send feature allows the operator to compose a message on the terminal screen and then, by depressing the SEND key, cause the terminal to send the entire message to the computer at the selected baud rate.

The sequence of operations is described in Figure 4-1.

The operation is as follows:

1. Raise Request-to-Send .
2. When Clear-to-Send, send STX (ØØ2) header.
3. Send data
4. If FORMAT and END OF PROTECTED FIELD, send HT code (111_8)
5. If not FORMAT and END of LINE, send CR/LF sequence. ($015_8/012_8$)
6. When end of message, send ETX (003_8)
7. Time out and drop Request-to-Send.

4.3.15 Auxiliary Send Circuit

The Aux Send feature is identical to the Block Send except for two points:

1. The message is transmitted out the AUX Port instead of the Main I/O Port.
2. The delimiters sent at the start of message, end of unprotected field, end of line, and ETX are selected from a different portion of the Block Send ROM.

4.3.16 Special Function (F1-F16)

Sends a code sequence to the computer from the terminal. The code is instigated by pressing any one of the 16 function keys.

1. An STX is transmitted (002_8)
2. An Escape code (033_8)
3. Code character (see ASCII Code Chart Table 3-2)
4. And ends with an ETX (003_8)

SECTION V

Maintenance

5.1 INTRODUCTION

This section contains information to aid in the maintenance of the B150 Terminal. Preventive and corrective maintenance procedures are specified as well as troubleshooting aids and techniques.

5.2 PREVENTIVE MAINTENANCE

No scheduled periodic maintenance is required. However, several precautions can be taken periodically to ensure proper operation. Care should be exercised to see that there is proper air circulation for the fan. The terminal should not be placed on a shag carpet or other soft surface that could impede the air entrance to the fan. Special care must be taken to ensure that no paper or other loose articles are placed under the terminal. The degree of dust density in the air should be considered in selecting the location of the terminal.

The interior of the unit may be wiped free of dust. Accumulation of dirt causes overheating and component breakdown. Dirt acts as an insulating blanket and prevents efficient heat dissipation. A small brush is very useful for dislodging dirt; a cotton-tipped applicator is good for narrow or hard to get places.

The following is a list of the troubleshooting aids that are provided in this manual to assist in the troubleshooting of functional failures.

Circuit Schematics	See Section VI
Detailed Block Diagram	Figures 1, 2, & 3 of Section IV
Functional Flow Diagram	
Timing Diagrams	See Section IV
Glossary of Terms	Appendix B
Troubleshooting Flow Diagrams	This Section
Disassembly/Assembly procedures	This Section
Adjustment Procedures	
Configuration/Strapping	See Section II
Power Supply Adjustments	See Section II
Character Dot Matrix	See Section IV

5.2.1 Troubleshooting Equipment

The following is a list of tools and standard equipment required to repair a B150 Terminal:

V/O Multimeter
Oscilloscope
Assorted Electronic Hand Tools

5.3 CORRECTIVE MAINTENANCE

This section provides corrective maintenance information to aid in servicing the B150 Terminal. It is suggested that the configuration sheet and the turn-on procedure be consulted before performing the corrective maintenance described here (see Section III).

5.3.1 Troubleshooting Preliminary Considerations

The most common problem occuring in B150 are switch, control and operation related. A simple procedure may be followed to help determine if the problem is control and/or operation-related or internal circuitry related by checking the following:

Illegal Operation (Refer to Section II)
Improper Baud Rate Setting
Wrong Transmit or Receive Mode
Loose Interconnect Cable

5.3.2 Troubleshooting Flow Diagrams

A list of troubleshooting flow diagrams is given in Table 5-1. This index lists apparent failure and refers the user to the proper flow diagram. The Table is only intended to allow the user to verify the subassembly where trouble exists and not to indicate the specific problem. The user is advised to return the defective subassembly and have that subassembly repaired or replaced by an authorized service agent.

1. Find the apparent trouble in the Troubleshooting Flow Diagram Index.

2. Proceed to the specified Troubleshooting Flow Diagram in the diagram section and begin the troubleshooting procedure.

3. If an adjustment procedure is referenced in the Troubleshooting Flow Diagram, perform the adjustment and return to the flow diagram to complete the troubleshooting process.

4. Reference is made to Timing diagrams contained in (Section VI) this manual.

5.3.3 Full-Duplex Echoplex Test

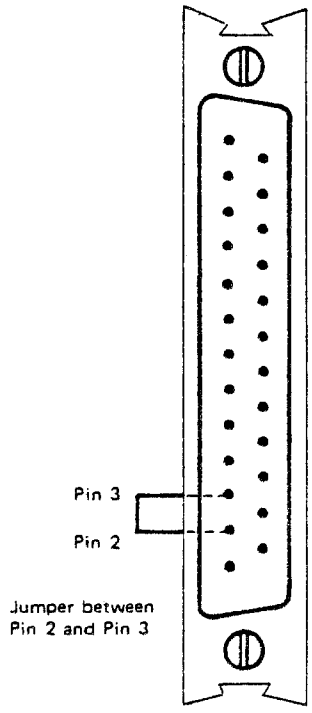
A specially wired connector may be assembled that will allow the operator to perform this test. This connector tester allows the terminal to be operated and tested independent of an external data device. The connector mates with the Main I/O Port. Set-up for the test is as follows:

FDX (Full Duplex Mode)
Baud Rate -- Any Setting
Test Connector Installed in the I/O Port

Enter data from the keyboard as you would if you were on-line to a computer. If data is displayed on the screen properly, then the B150 is transmitting and receiving data properly.

The Test Connector is wired as follows: (Refer to Figure 5.1.)

Connects Transmitted Data Line out of the terminal to received data line into the terminal. Pin 2 to Pin 3 of the I/O Port.



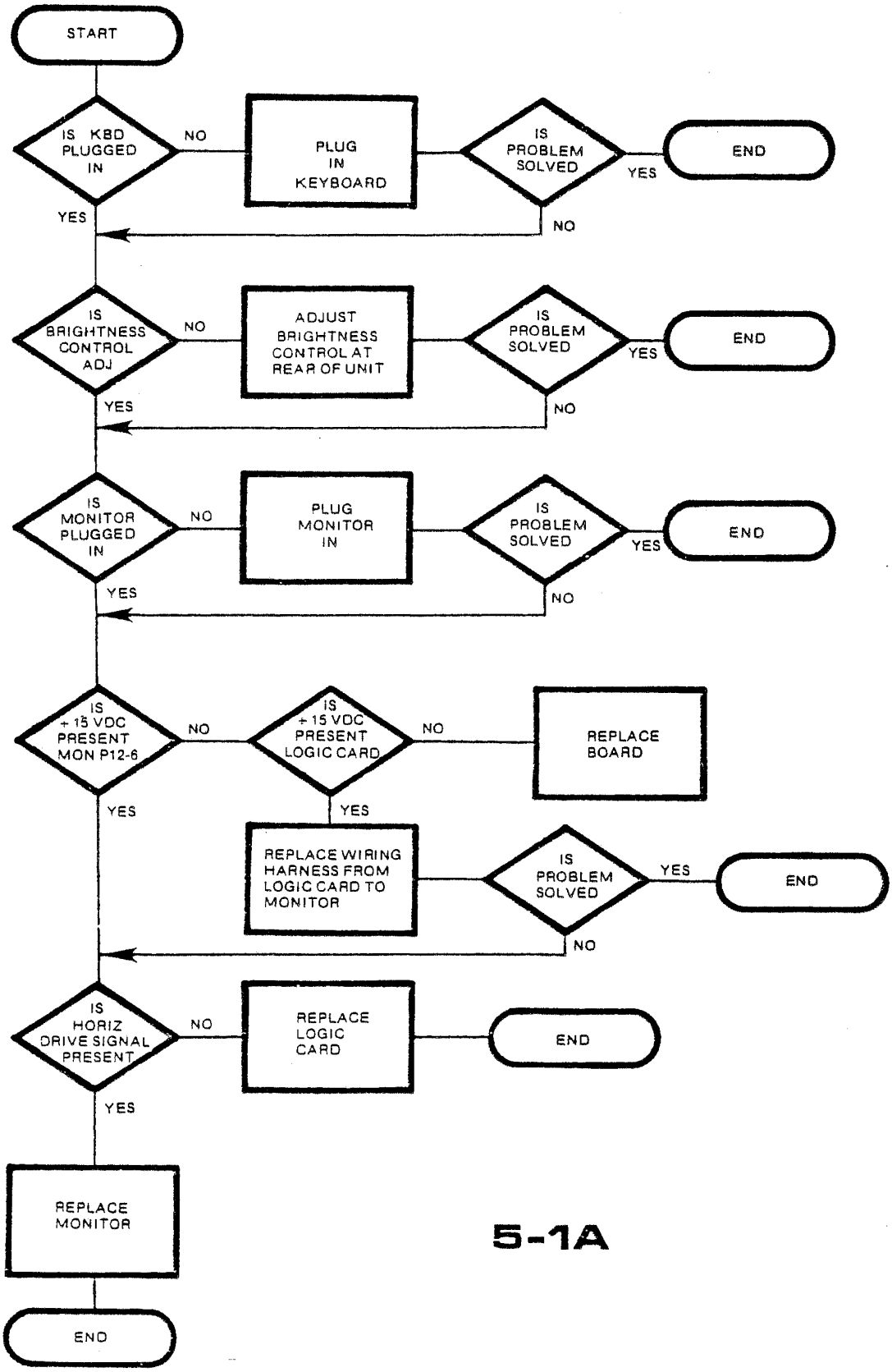
Male Type Amphenol Connector

Beehive Part No. 606-0011-25 AP

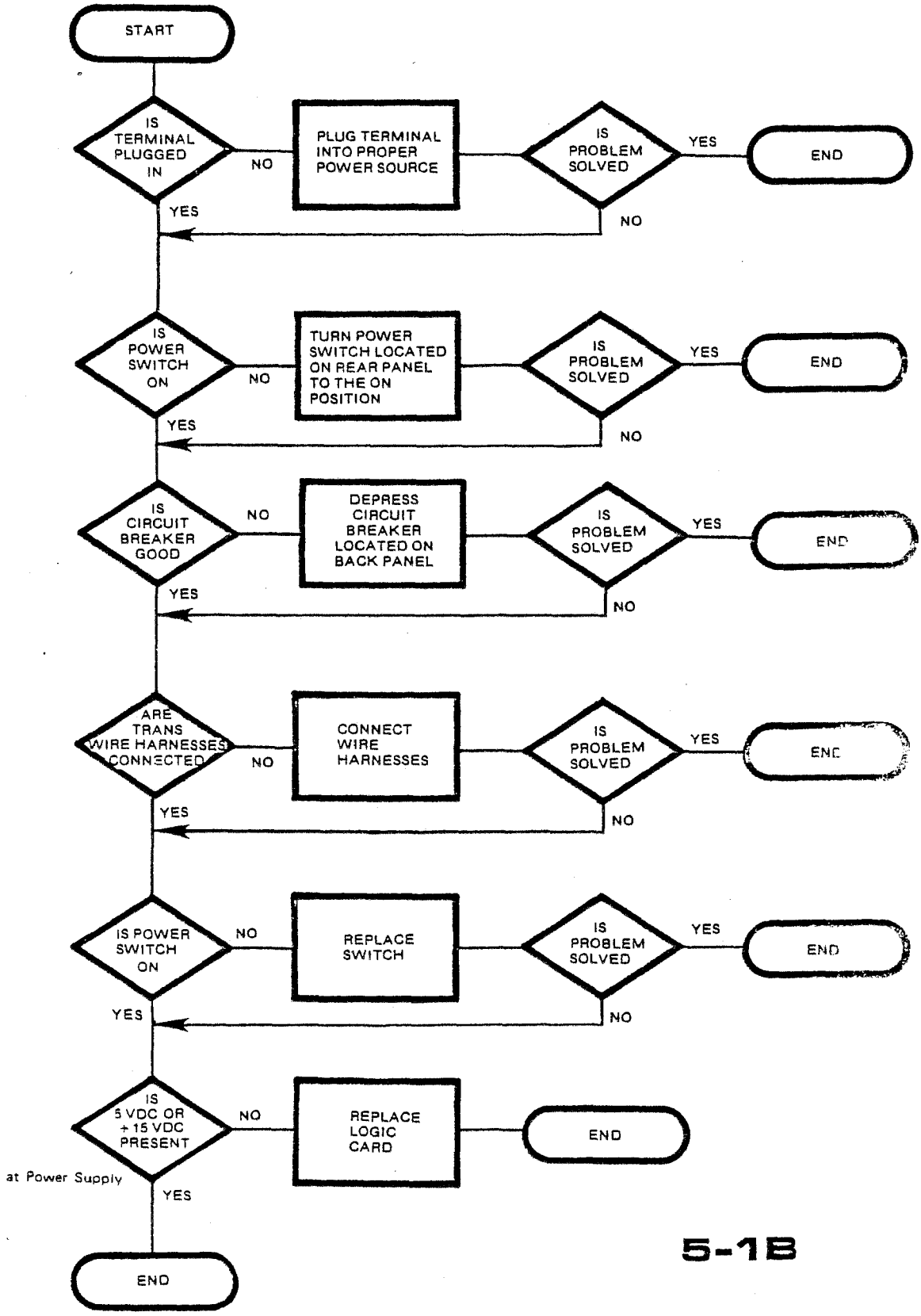
Figure 5-1
ECHOPLEX TEST CONNECTOR

Table 5-1. Troubleshooting Flow Diagram Index

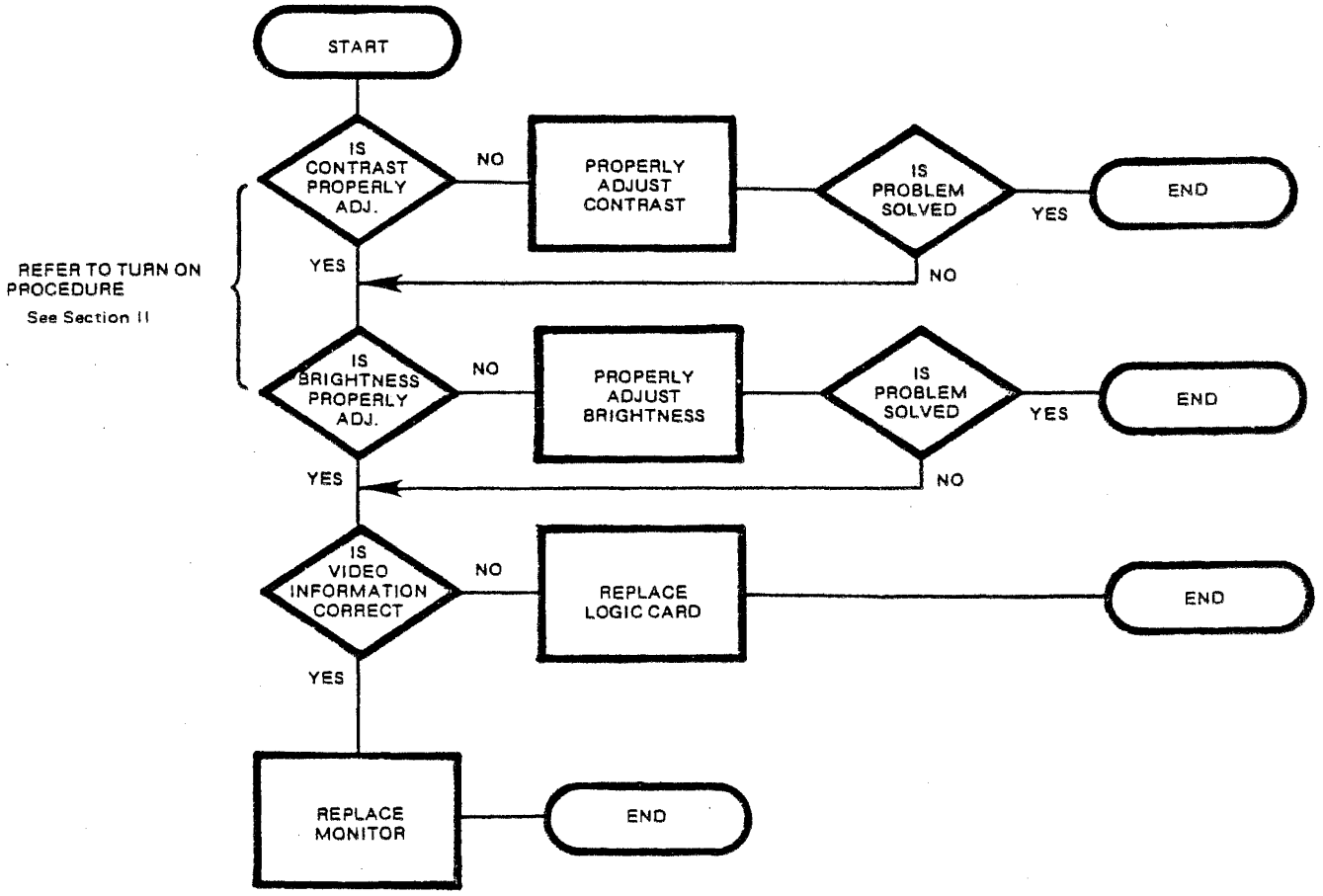
Apparent Failure	Troubleshooting Flow Diagram
GENERAL	
No raster present	5-1A
No raster present	5-1B
OFF LINE	
Cursor either absent, multiple cursors, cursor not in home position or screen filled with video blocks	5-2A
No character displayed when written, non cursor advance	5-2B
Wrong character displayed	5-2C
No escape functions	5-2D
No control functions	5-2E
ON LINE	
No data being transmitted	5-3A
Transmits invalid data	5-3B
No reception	5-3C
Receives invalid data and/or improper parity	5-3D
DISPLAY	
All displayed characters out of focus	5-4A
Rolling display	5-4B
Display too tall/short for screen size	5-4C
Height of displayed characters uneven	5-4D
Display too wide/narrow for screen size	5-4E
Display not centered	5-4F
Tilted display	5-4G
Others A. Single vertical line B. Physical damage C. Dot in center of screen D. Uneven intensity/focus E. Burned phosphor F. Uneven display dimensions G. Excessive H.V. Arcing	5-4H


START
IS KBD PLUGGED IN
NO
PLUG IN KEYBOARD
IS PROBLEM SOLVED
YES
END
YES
NO
IS BRIGHTNESS CONTROL ADJ
NO
ADJUST BRIGHTNESS CONTROL AT REAR OF UNIT
IS PROBLEM SOLVED
YES
END
YES
NO
IS MONITOR PLUGGED IN
NO
PLUG MONITOR IN
IS PROBLEM SOLVED
YES
END
YES
NO
IS +15 VDC PRESENT MON P12-6
NO
IS +15 VDC PRESENT LOGIC CARD
NO
REPLACE BOARD
YES
YES
REPLACE WIRING HARNESS FROM LOGIC CARD TO MONITOR
IS PROBLEM SOLVED
YES
END
NO
IS HORIZ DRIVE SIGNAL PRESENT
NO
REPLACE LOGIC CARD
END
YES
REPLACE MONITOR
END

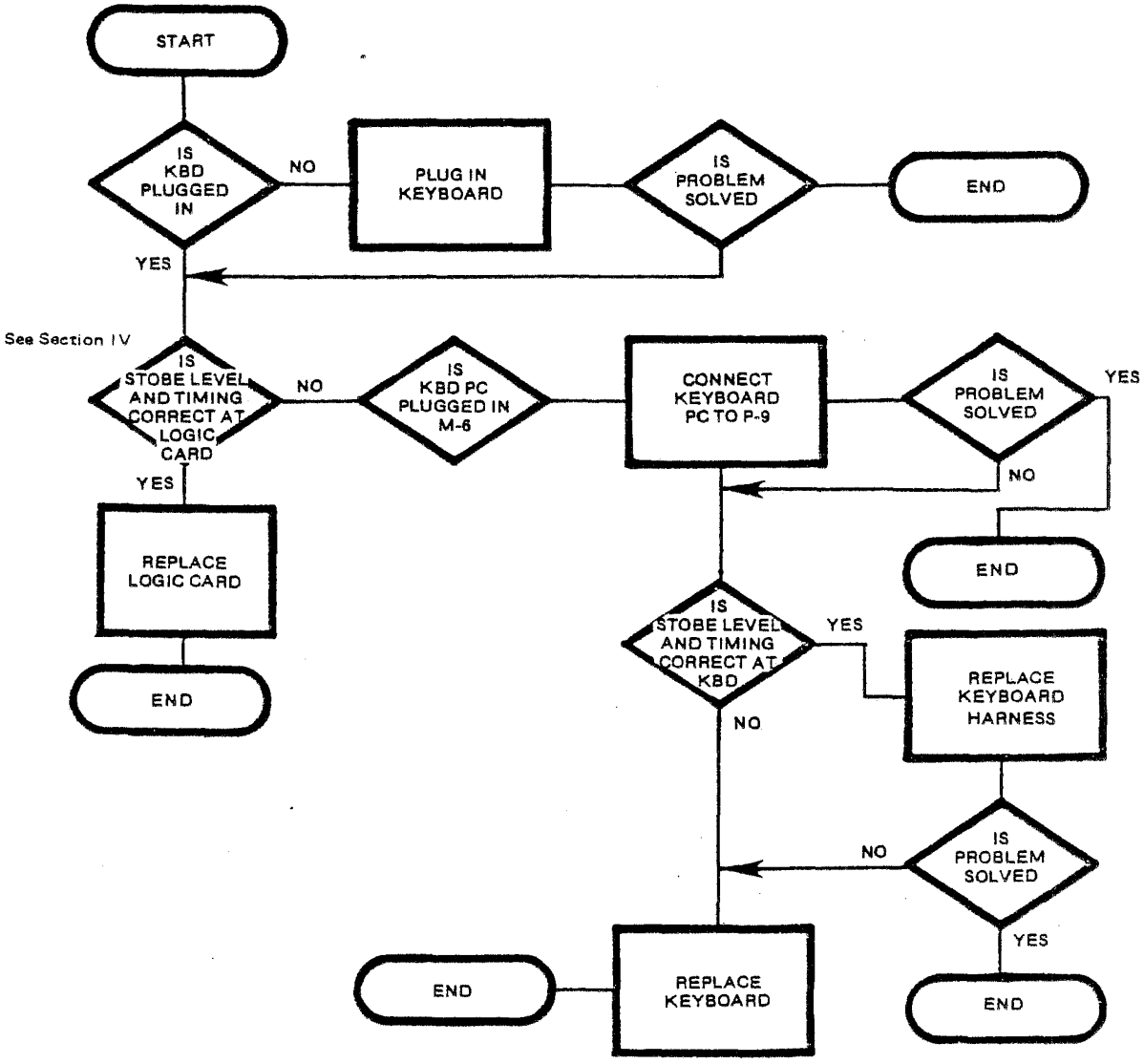
5-1A


START
IS TERMINAL PLUGGED IN
NO
PLUG TERMINAL INTO PROPER POWER SOURCE
IS PROBLEM SOLVED
YES
END
NO
YES
IS POWER SWITCH ON
NO
TURN POWER SWITCH LOCATED ON REAR PANEL TO THE ON POSITION
IS PROBLEM SOLVED
YES
END
NO
YES
IS CIRCUIT BREAKER GOOD
NO
DEPRESS CIRCUIT BREAKER LOCATED ON BACK PANEL
IS PROBLEM SOLVED
YES
END
NO
YES
ARE TRANS WIRE HARNESSES CONNECTED
NO
CONNECT WIRE HARNESSES
IS PROBLEM SOLVED
YES
END
NO
YES
IS POWER SWITCH ON
NO
REPLACE SWITCH
IS PROBLEM SOLVED
YES
END
NO
YES
IS 5 VDC OR +15 VDC PRESENT
at Power Supply
NO
REPLACE LOGIC CARD
END
YES
END

5-1B

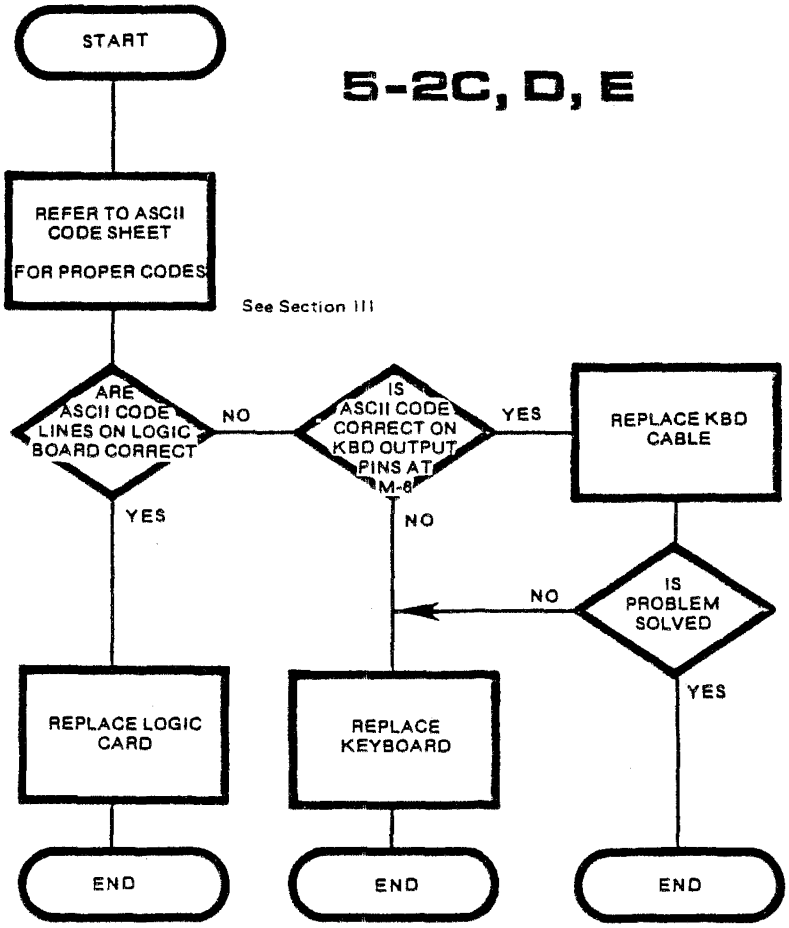

START
IS CONTRAST PROPERLY ADJ.
NO
PROPERLY ADJUST CONTRAST
IS PROBLEM SOLVED
YES
END
NO
YES
REFER TO TURN ON PROCEDURE
See Section II
IS BRIGHTNESS PROPERLY ADJ.
NO
PROPERLY ADJUST BRIGHTNESS
IS PROBLEM SOLVED
YES
END
NO
YES
IS VIDEO INFORMATION CORRECT
NO
REPLACE LOGIC CARD
END
YES
REPLACE MONITOR
END

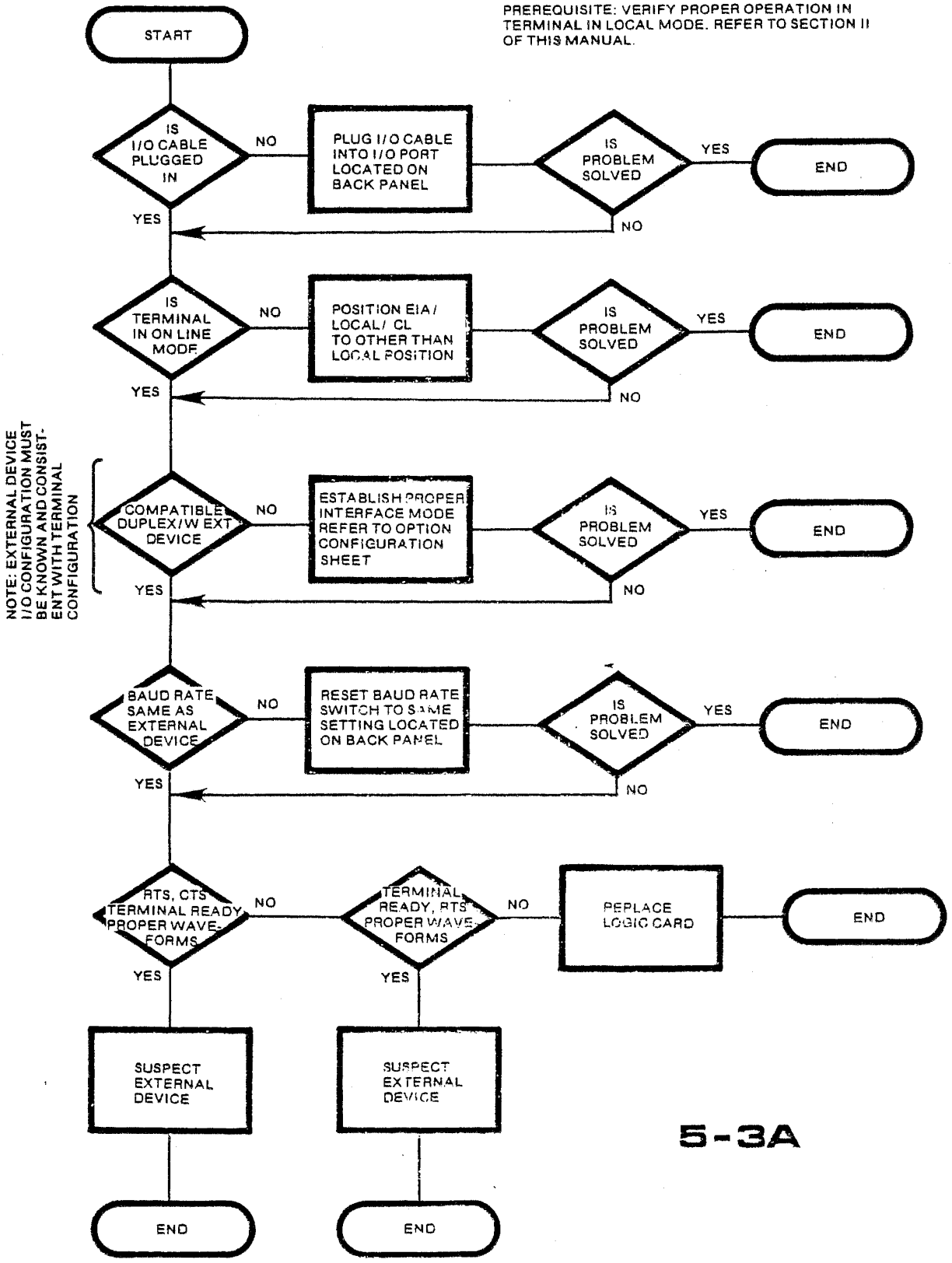
5-2A


START
IS KBD PLUGGED IN
NO
PLUG IN KEYBOARD
IS PROBLEM SOLVED
END
YES
See Section IV
IS STOBE LEVEL AND TIMING CORRECT AT LOGIC CARD
NO
IS KBD PC PLUGGED IN M-6
CONNECT KEYBOARD PC TO P-9
IS PROBLEM SOLVED
YES
NO
END
YES
REPLACE LOGIC CARD
END
IS STOBE LEVEL AND TIMING CORRECT AT KBD
YES
REPLACE KEYBOARD HARNESS
NO
NO
IS PROBLEM SOLVED
YES
END
REPLACE KEYBOARD
END

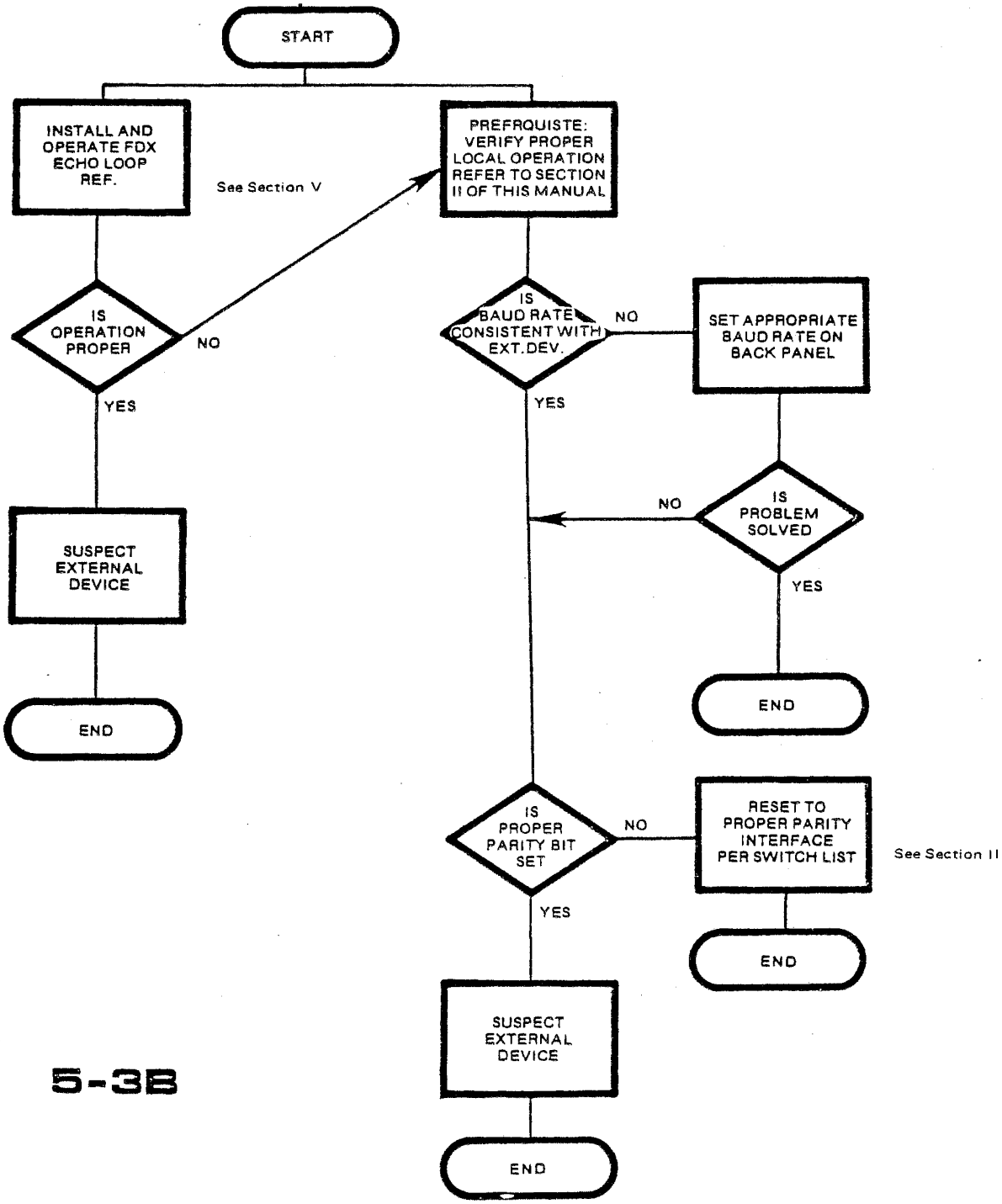
5-2B

5-2C, D, E


START
REFER TO ASCII CODE SHEET FOR PROPER CODES
See Section III
ARE ASCII CODE LINES ON LOGIC BOARD CORRECT
NO
IS ASCII CODE CORRECT ON KBD OUTPUT PINS AT M-8
YES
REPLACE KBD CABLE
YES
NO
IS PROBLEM SOLVED
NO
YES
REPLACE LOGIC CARD
REPLACE KEYBOARD
END
END
END

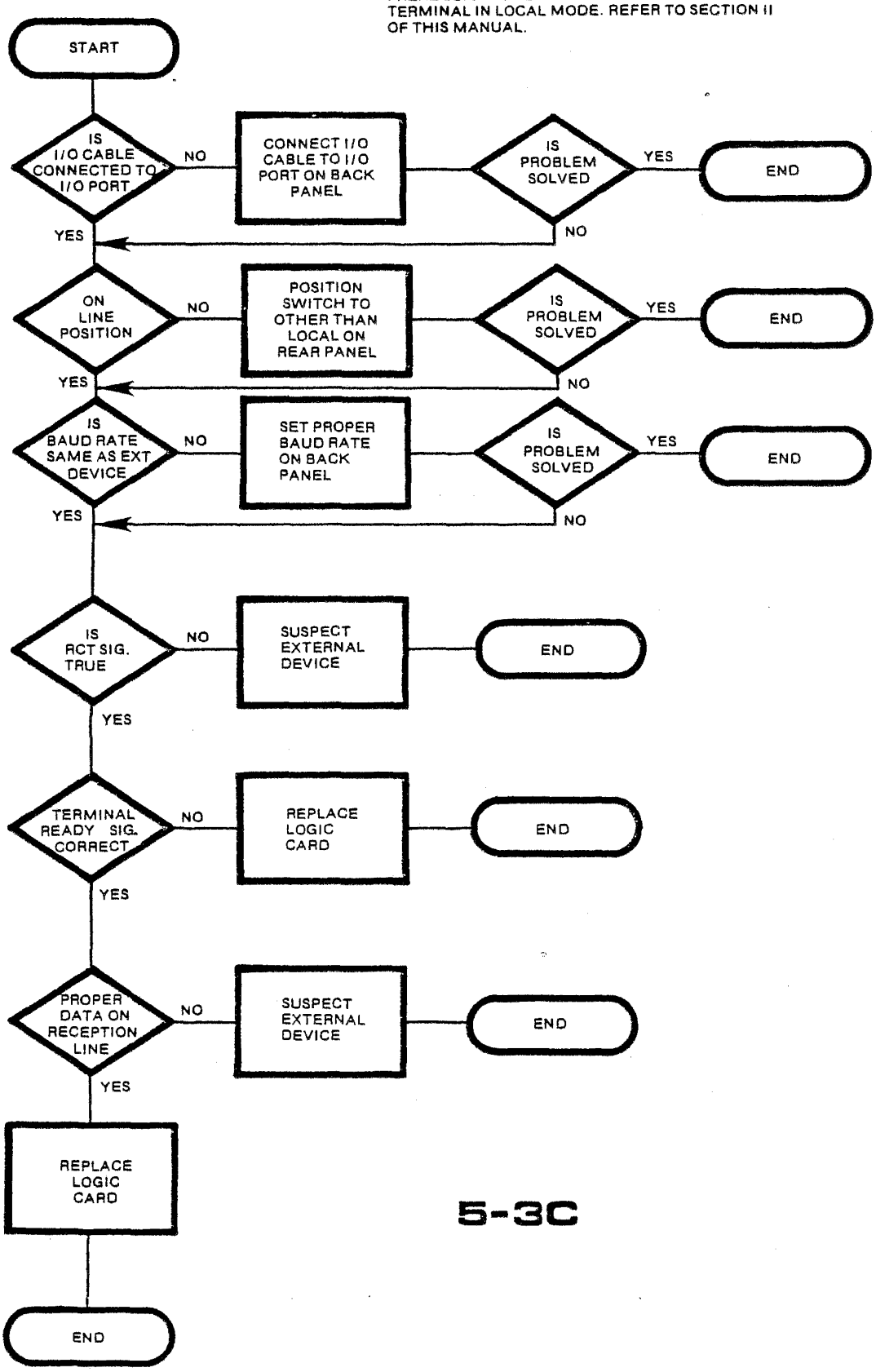

PREREQUISITE: VERIFY PROPER OPERATION IN TERMINAL IN LOCAL MODE. REFER TO SECTION II OF THIS MANUAL.
START
IS I/O CABLE PLUGGED IN
NO
PLUG I/O CABLE INTO I/O PORT LOCATED ON BACK PANEL
IS PROBLEM SOLVED
YES
END
YES
NO
IS TERMINAL IN ON LINE MODE
NO
POSITION EIA/ LOCAL/ CL TO OTHER THAN LOCAL POSITION
IS PROBLEM SOLVED
YES
END
YES
NO
NOTE: EXTERNAL DEVICE I/O CONFIGURATION MUST BE KNOWN AND CONSISTENT WITH TERMINAL CONFIGURATION
COMPATIBLE DUPLEX/W EXT DEVICE
NO
ESTABLISH PROPER INTERFACE MODE REFER TO OPTION CONFIGURATION SHEET
IS PROBLEM SOLVED
YES
END
YES
NO
BAUD RATE SAME AS EXTERNAL DEVICE
NO
RESET BAUD RATE SWITCH TO SAME SETTING LOCATED ON BACK PANEL
IS PROBLEM SOLVED
YES
END
YES
NO
RTS, CTS TERMINAL READY PROPER WAVE-FORMS
NO
TERMINAL READY, RTS PROPER WAVE-FORMS
NO
REPLACE LOGIC CARD
END
YES
YES
SUSPECT EXTERNAL DEVICE
SUSPECT EXTERNAL DEVICE
END
END

5-3A

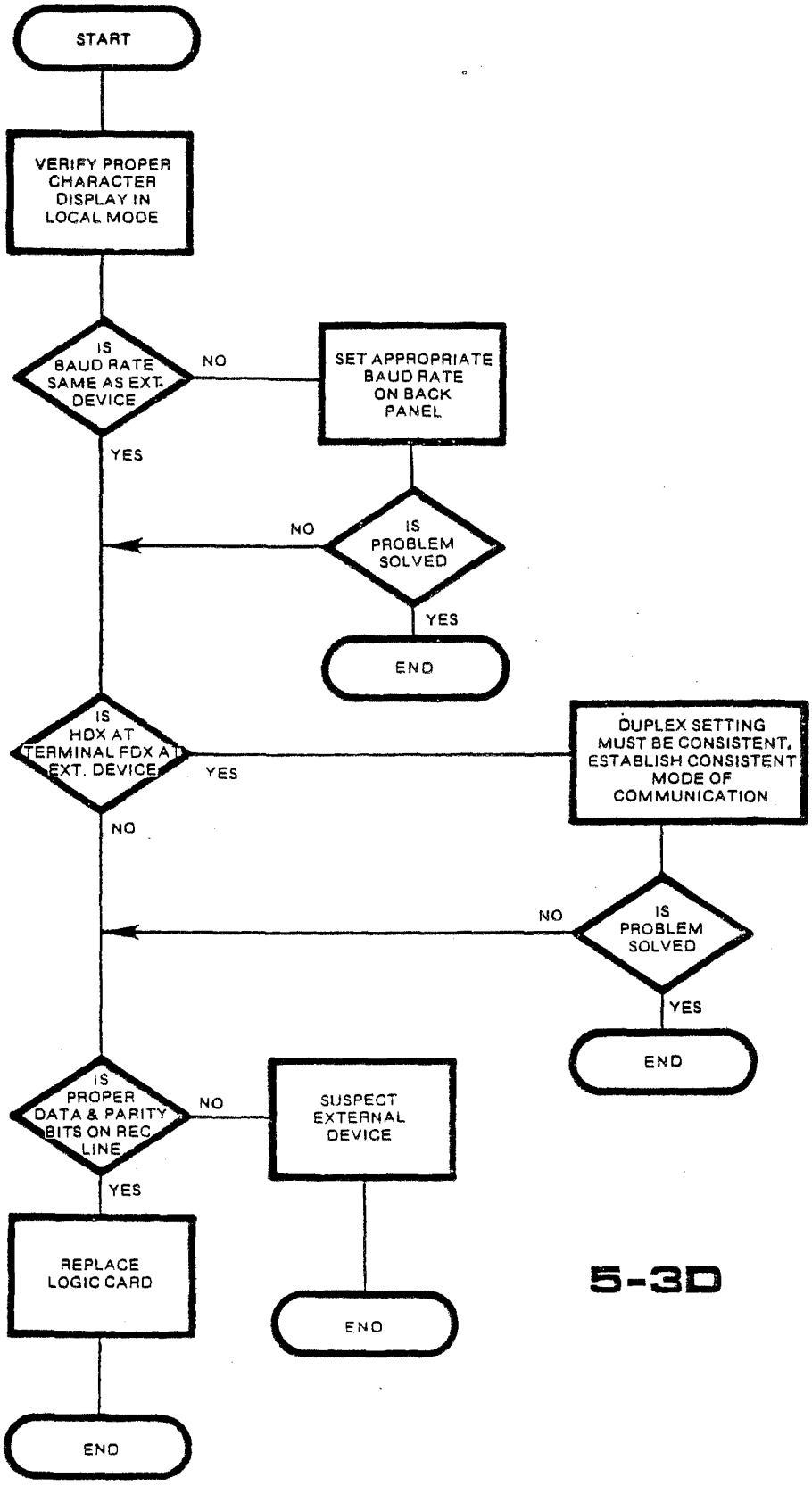

START
INSTALL AND OPERATE FDX ECHO LOOP REF.
See Section V
PREFRQUISTE: VERIFY PROPER LOCAL OPERATION REFER TO SECTION II OF THIS MANUAL
IS OPERATION PROPER
NO
YES
IS BAUD RATE CONSISTENT WITH EXT.DEV.
NO
SET APPROPRIATE BAUD RATE ON BACK PANEL
YES
NO
IS PROBLEM SOLVED
YES
SUSPECT EXTERNAL DEVICE
END
END
IS PROPER PARITY BIT SET
NO
RESET TO PROPER PARITY INTERFACE PER SWITCH LIST
See Section II
YES
END
SUSPECT EXTERNAL DEVICE
END

5-3B

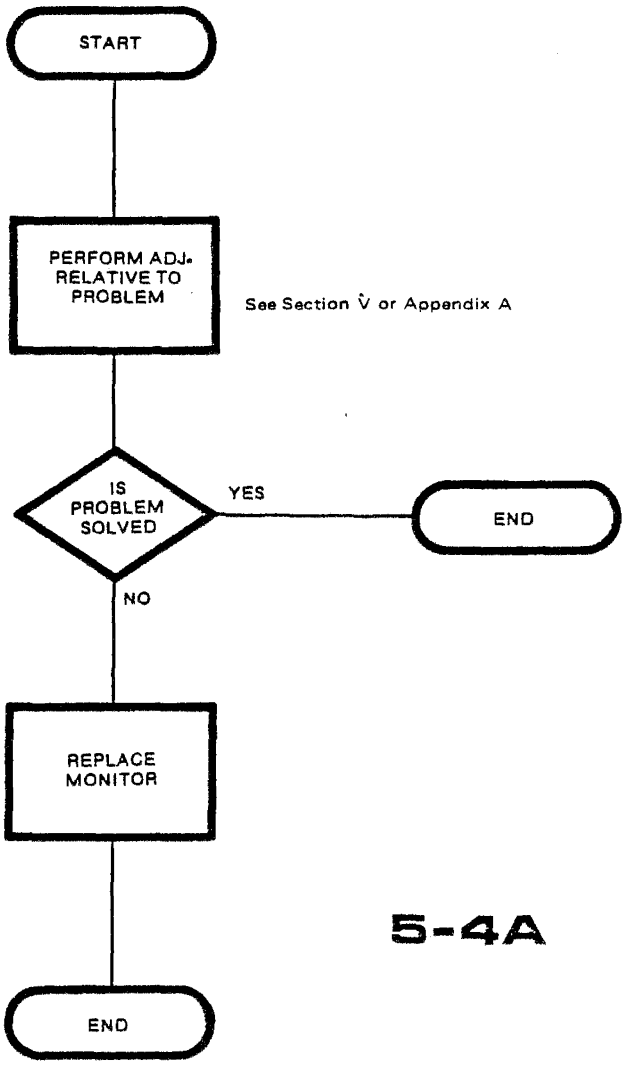
PREREQUISITE: VERIFY PROPER OPERATION OF TERMINAL IN LOCAL MODE. REFER TO SECTION II OF THIS MANUAL.



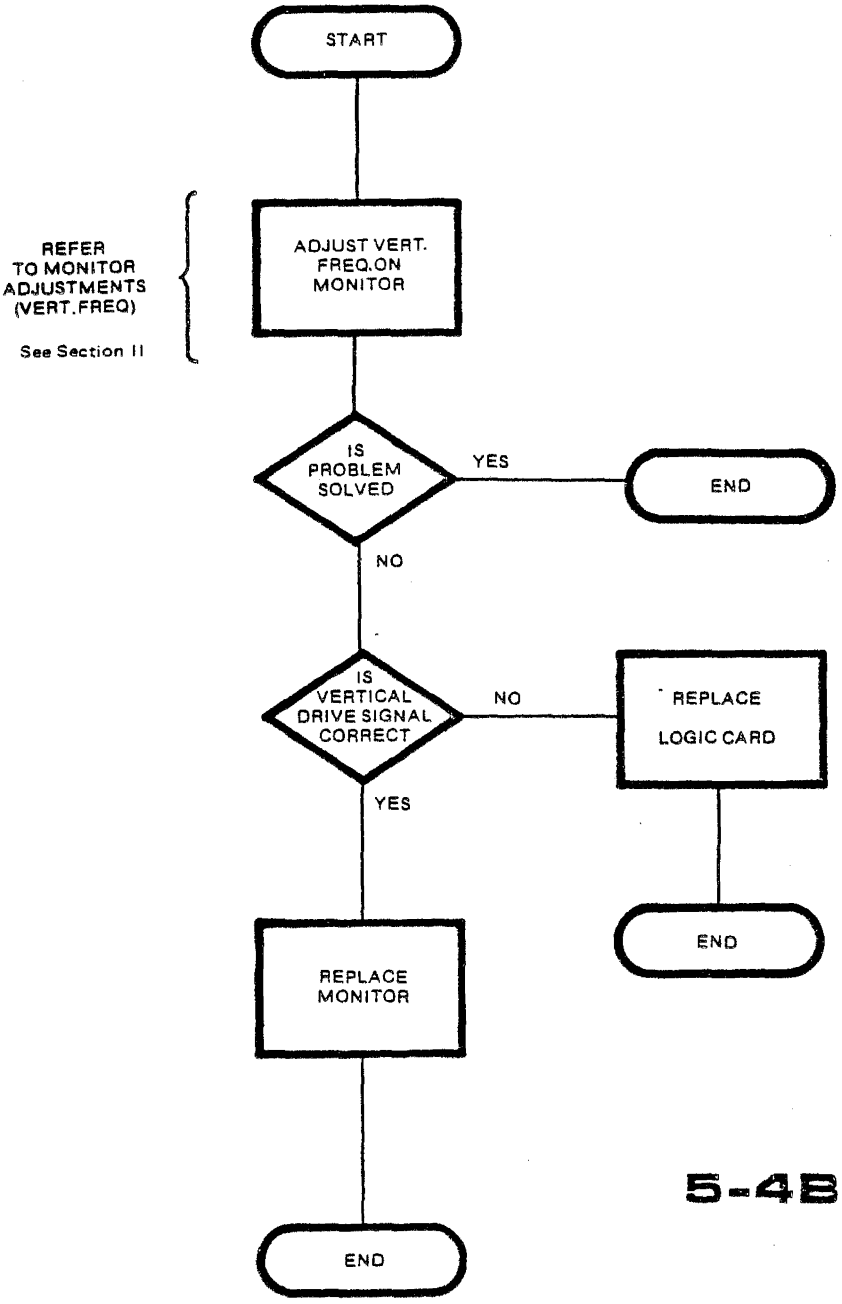
5-3C


START
VERIFY PROPER CHARACTER DISPLAY IN LOCAL MODE
IS BAUD RATE SAME AS EXT. DEVICE
NO
SET APPROPRIATE BAUD RATE ON BACK PANEL
YES
NO
IS PROBLEM SOLVED
YES
END
IS HDX AT TERMINAL FDX AT EXT. DEVICE
YES
DUPLEX SETTING MUST BE CONSISTENT. ESTABLISH CONSISTENT MODE OF COMMUNICATION
NO
NO
IS PROBLEM SOLVED
YES
END
IS PROPER DATA & PARITY BITS ON REC. LINE
NO
SUSPECT EXTERNAL DEVICE
YES
REPLACE LOGIC CARD
END
END

5-3D

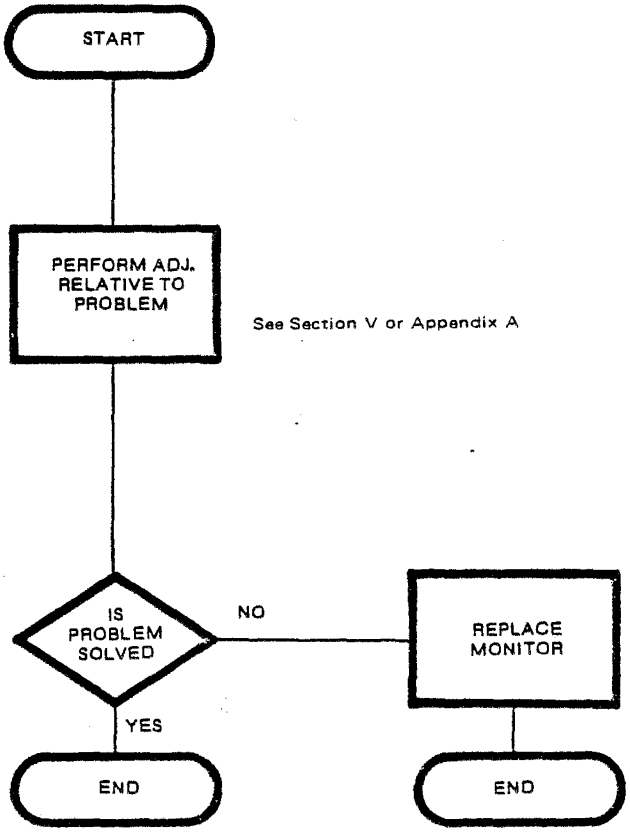

START
PERFORM ADJ. RELATIVE TO PROBLEM
See Section V or Appendix A
IS PROBLEM SOLVED
YES
END
NO
REPLACE MONITOR
END

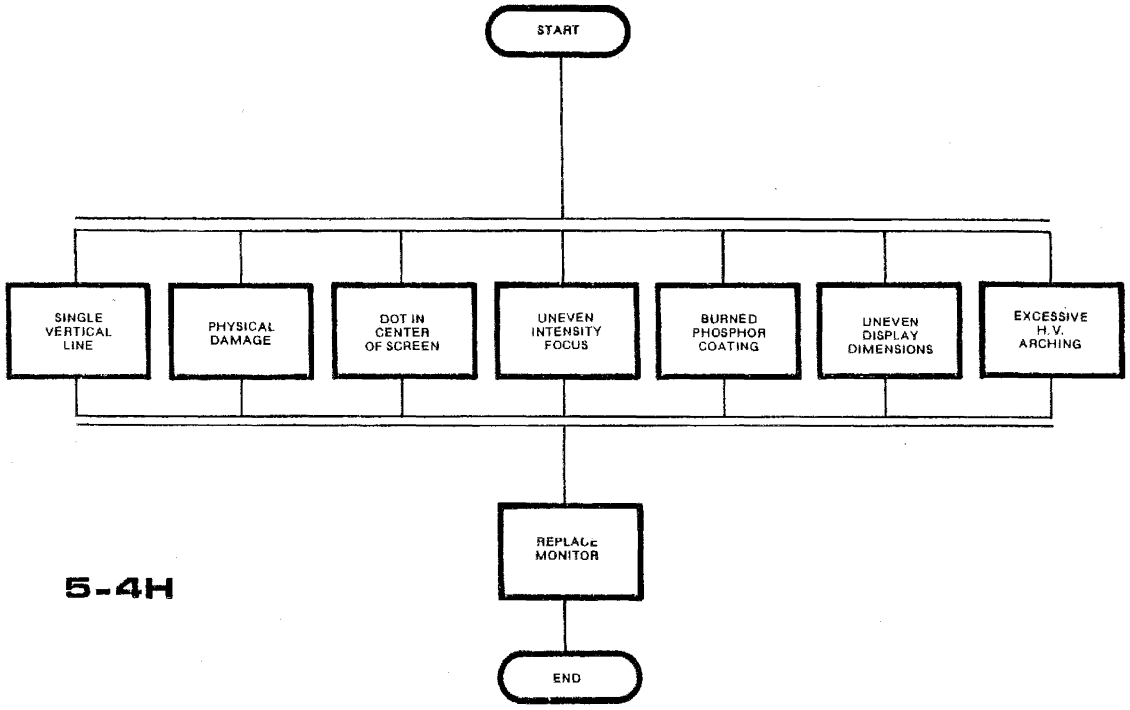
5-4A


START
REFER TO MONITOR ADJUSTMENTS (VERT.FREQ)
See Section II
ADJUST VERT. FREQ.ON MONITOR
IS PROBLEM SOLVED
YES
END
NO
IS VERTICAL DRIVE SIGNAL CORRECT
NO
REPLACE LOGIC CARD
END
YES
REPLACE MONITOR
END

5-4B

5-4C, D, E, F, G


START
PERFORM ADJ. RELATIVE TO PROBLEM
See Section V or Appendix A
IS PROBLEM SOLVED
NO
REPLACE MONITOR
YES
END
END


START
SINGLE VERTICAL LINE
PHYSICAL DAMAGE
DOT IN CENTER OF SCREEN
UNEVEN INTENSITY FOCUS
BURNED PHOSPHOR COATING
UNEVEN DISPLAY DIMENSIONS
EXCESSIVE H.V. ARCHING
REPLACE MONITOR
END

5-4H

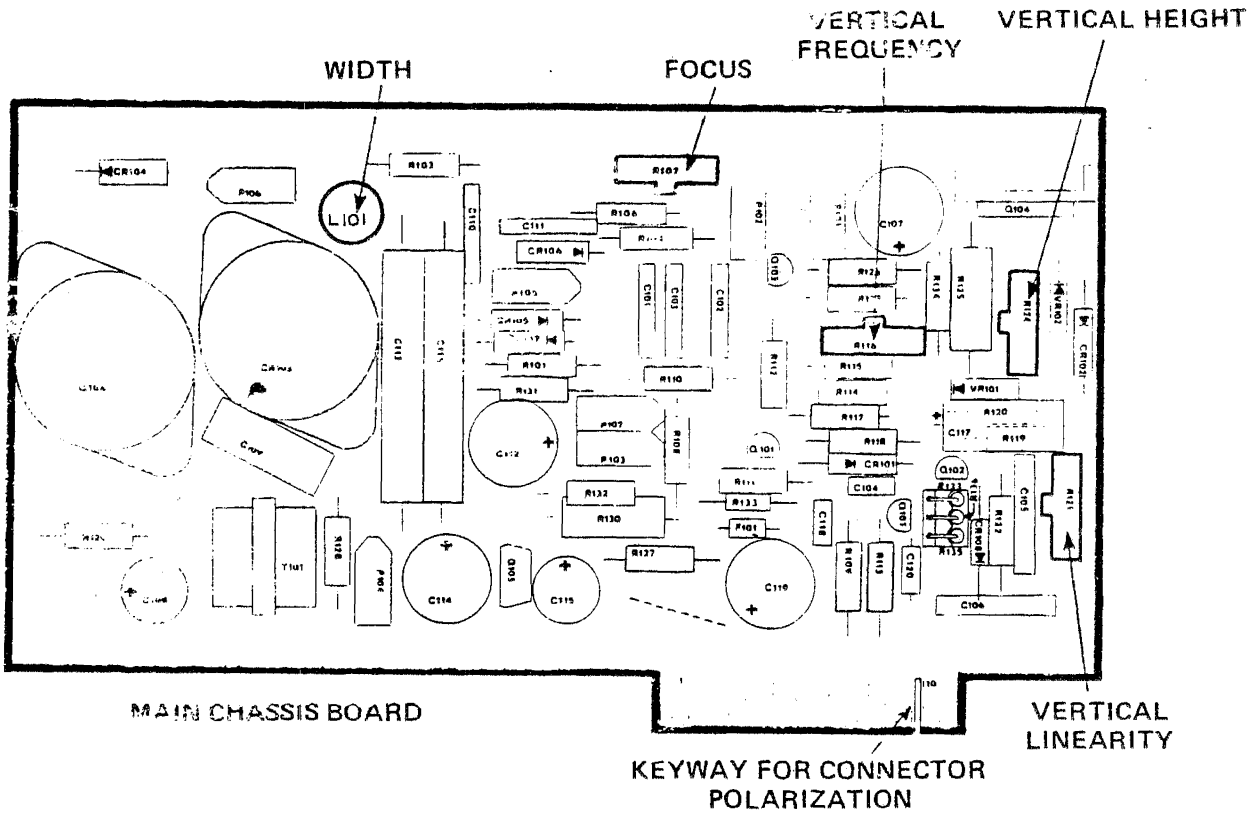


FIGURE 5-2 MONITOR ADJUSTMENTS

5.4 MONITOR ADJUSTMENTS

The following adjustments should be made while the monitor is in the 8150 terminal.

The adjustments that follow should be done with the terminal case removed. A drawing of the Monitor PC Board adjustment points is shown in Figure 5-2, while other monitor adjustments are made from the back panel of the terminal.

- Brightness
- Contrast
- Vertical Adjustments
- Focus
- Centering

WARNING: The Monitor employs high voltages. Care should be used in making any adjustments as power will be applied to the Monitor.

The brightness & contrast controls (located on the back panel) should be positioned to a point where the white raster on the CRT is extinguished. Fill the screen of the CRT with characters from the keyboard and adjust the contrast control for the sharpest display of the characters in the upper left hand side of the screen.

The vertical frequency control (R 116, Figure 5-5) is set to the approximate mechanical mid-point initially. This adjustment will correct for a rolling display and should be adjusted to correct that symptom alone. No discrete measurement is necessary, except for a visual observation as to the steadiness of the display.

Fill the screen again with characters. The vertical height control (R 124, Figure 5-2) should be adjusted 6½ inches from the top of the characters on the first row to the bottom of the characters on the last row in the center of the display.

The vertical linearity control (R 121, Figure 5-2) should be adjusted so the characters on the first row are equally as tall as the characters on the last row. Their height should be approximately 0.18 inches (46 mm).

If the screen is blank, fill it with characters and adjust the horizontal width coil (L101, Figure 5.2) for 8½ inches (21.6 cm) from the left margin to the right margin of the display characters.

The horizontal linearity is adjusted to correct for the compression of the display on the left hand side of the screen. To correct this, loosen the clamp securing the yoke and slide the cardboard sleeve in or out to give uniform width to the characters on the right and left borders of the display.

Adjust the focus control (R 107, Figure 5-2) for best overall display focus. It may be necessary to readjust the contrast control and repeat this step.

Centering of the display is accomplished by rotating the small permanent magnets glued behind the deflection yoke. Magnets should be removed and reglued with silicone adhesive. If the display as a whole is tilted, correction may be accomplished by rotating the entire yoke.

Additional descriptions and adjustments can be found in Appendix A.

5.5 DISASSEMBLY PROCEDURE B150

The B150 disassembles into replacable components: The Keyboard, Monitor Assembly, Logic Board, and Fan. All Major components can be removed and replaced quickly. An accompanying diagram Figure 5-3, shows major assembly sections and their interrelation. The following explanations relate to this diagram.

5.5.1 Case Removal

The reinforced fiber case is one piece and is fastened to the chassis with six screws and lock washers. The screws are located: Two on the front of the case below the keyboard, and four screws in the back of the case surrounding the black rear panel. Lift the case straight up for removal.

Assemble in the reverse order.

5.5.2 Logic Board Removal

Place the terminal in an upside down position on a soft surface to avoid damage. Remove the (5) screws and lock washers that secure the Bottom Plate to the chassis. The Logic Board is attached to the Bottom Plate with plastic clips (see Point A, Figure 5-3).

CAUTION: Do not remove the screws holding the keyboard.

Carefully lift the Bottom Plate/Logic Board and notice that there are four wiring harness attachment points: One for the keyboard at the front of the Logic Board (see Point B, Figure 5-3) and three for the power supply/monitor electronics and +5V regulator at the left rear (if the terminal is viewed from the bottom) of the Logic Board (see Point C, Figure 5-3). Carefully remove the keyboard strap and lift the front of the board so that the other plugs can be removed. The rear plugs have a plastic spring clip type connector that must be compressed before removal. The board should be pulled forward to clear the switches and plugs from their holes in the rear of the chassis and the board can then be removed.

Assemble in the reverse order.

5.5.3 Keyboard Assembly

Remove the case as described above. Remove the seven screws and lock washers (see point E, Figure 5-3) from the underneath side of the chassis on the keyboard end. Move the keyboard away from the monitor slightly and unplug the wire strap from the logic board to the keyboard (see Point F, Figure 5-3). Remove the keyboard.

Assemble in the reverse order.

5.5.4 Fan Removal

The Fan is removed by first removing the case (see above) and removing the four mounting screws at the back of the terminal (see Point G, Figure 5-3). Unhook the power cord and remove.

Assemble in the reverse order.

5.5.5 Monitor Assembly Removal

The bottom plate/logic board and case should be removed first (see above). Three screws and lock washers (see Point D, Figure 5.3)) hold the Monitor Assembly to the chassis. Remove the screws from the underside of the chassis. The complete Monitor Assembly can then be removed.

Assemble in the reverse order.

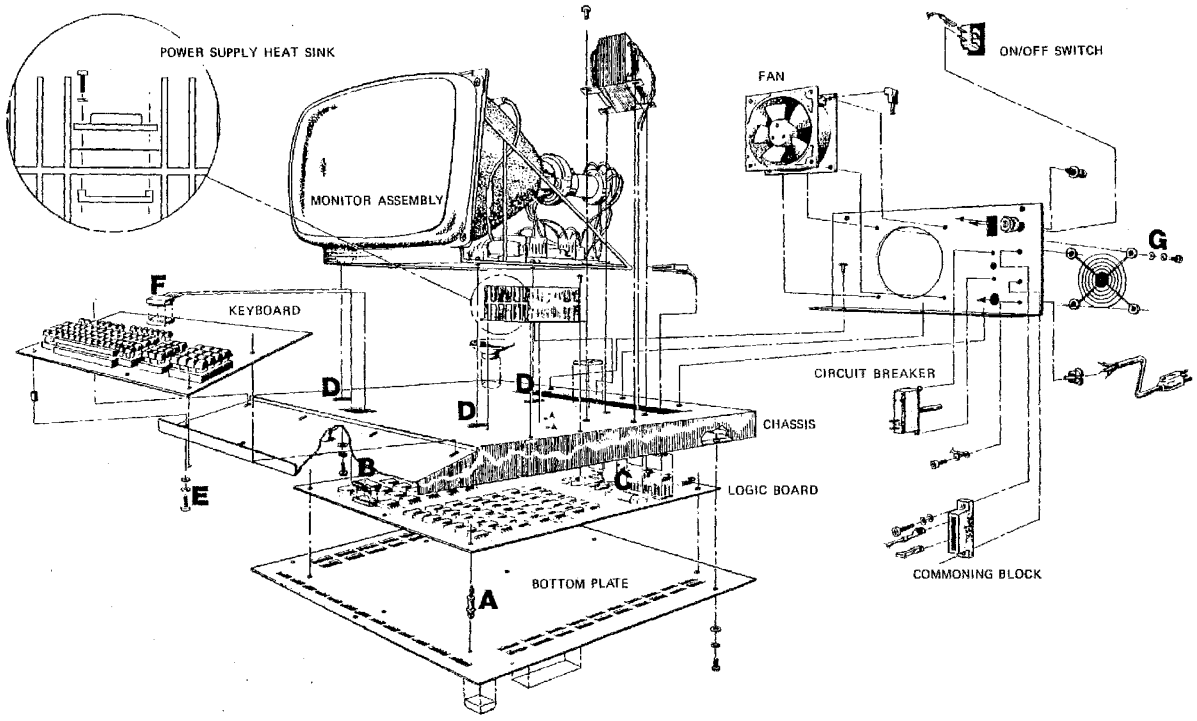
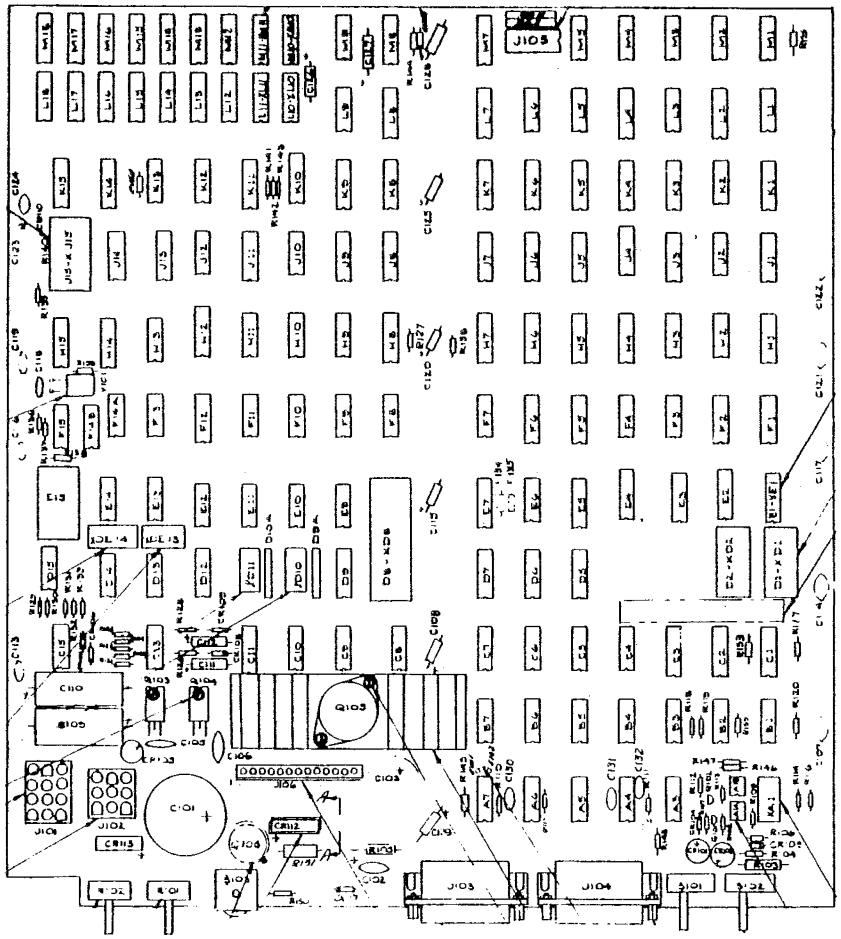


FIGURE 5-3 ASSEMBLY DRAWING (B150)

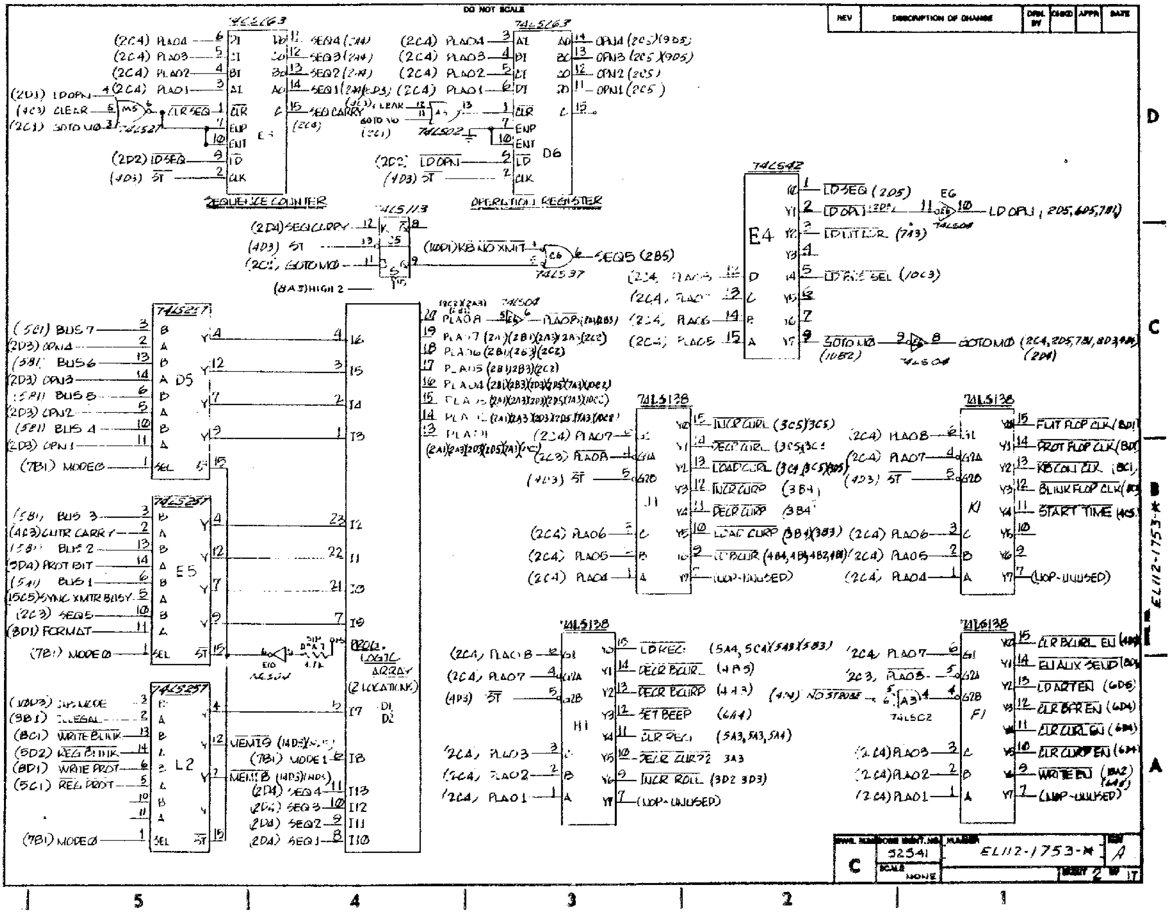
SECTION VI

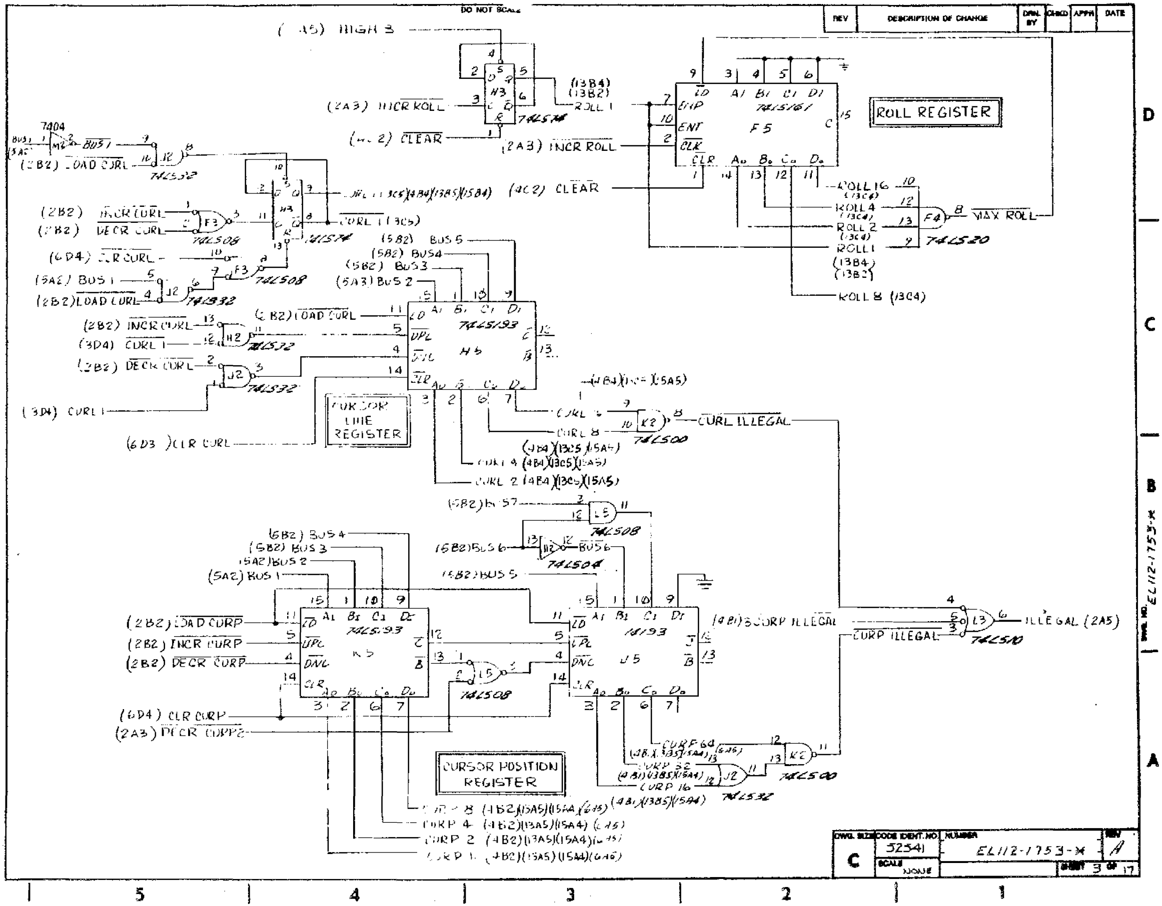
Drawings / Schematics

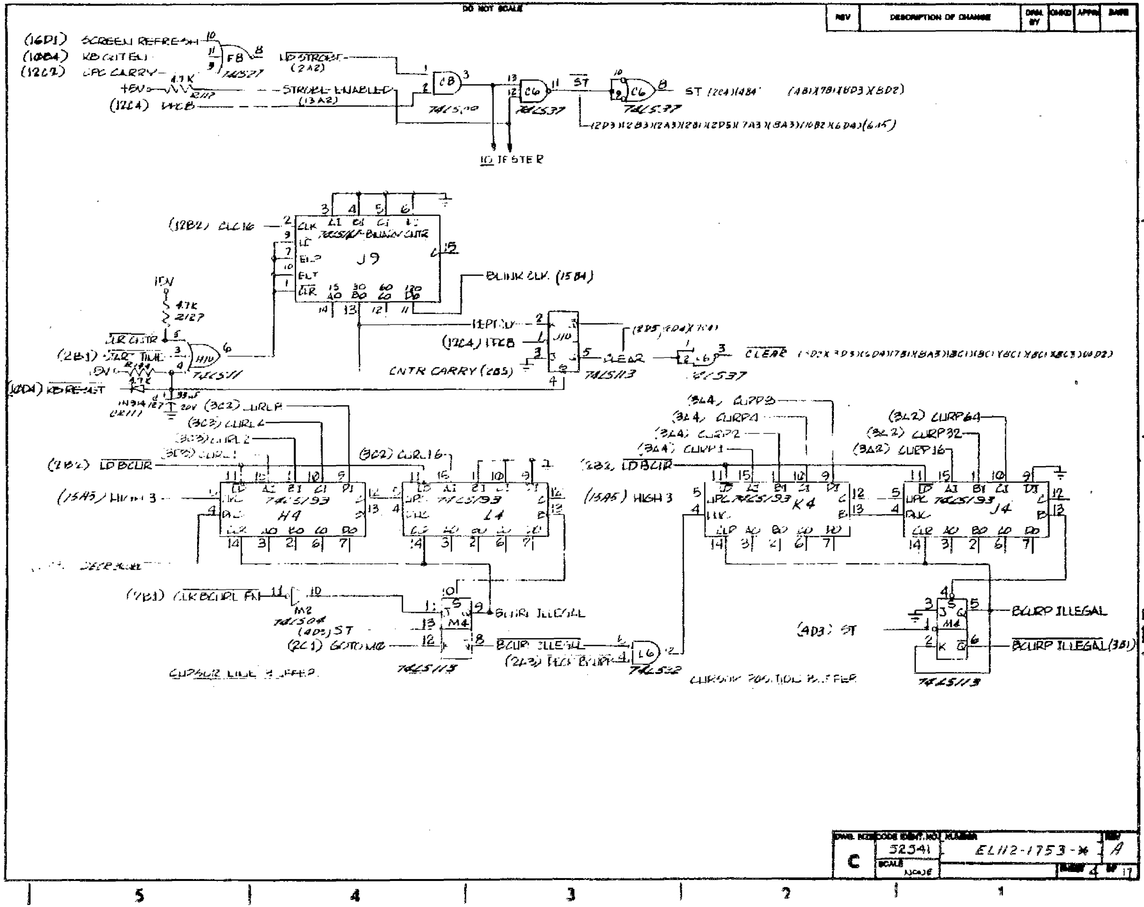


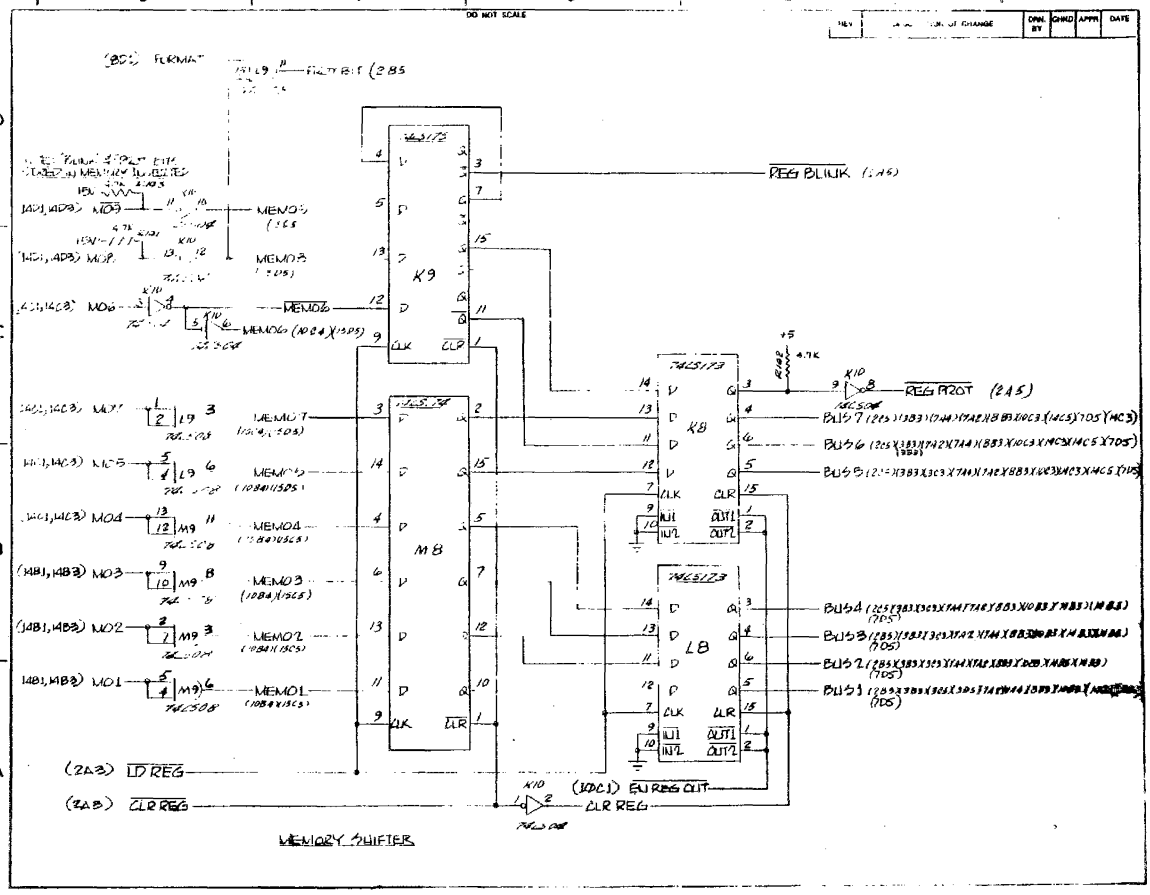
B150 Logic Board Assembly Drawing

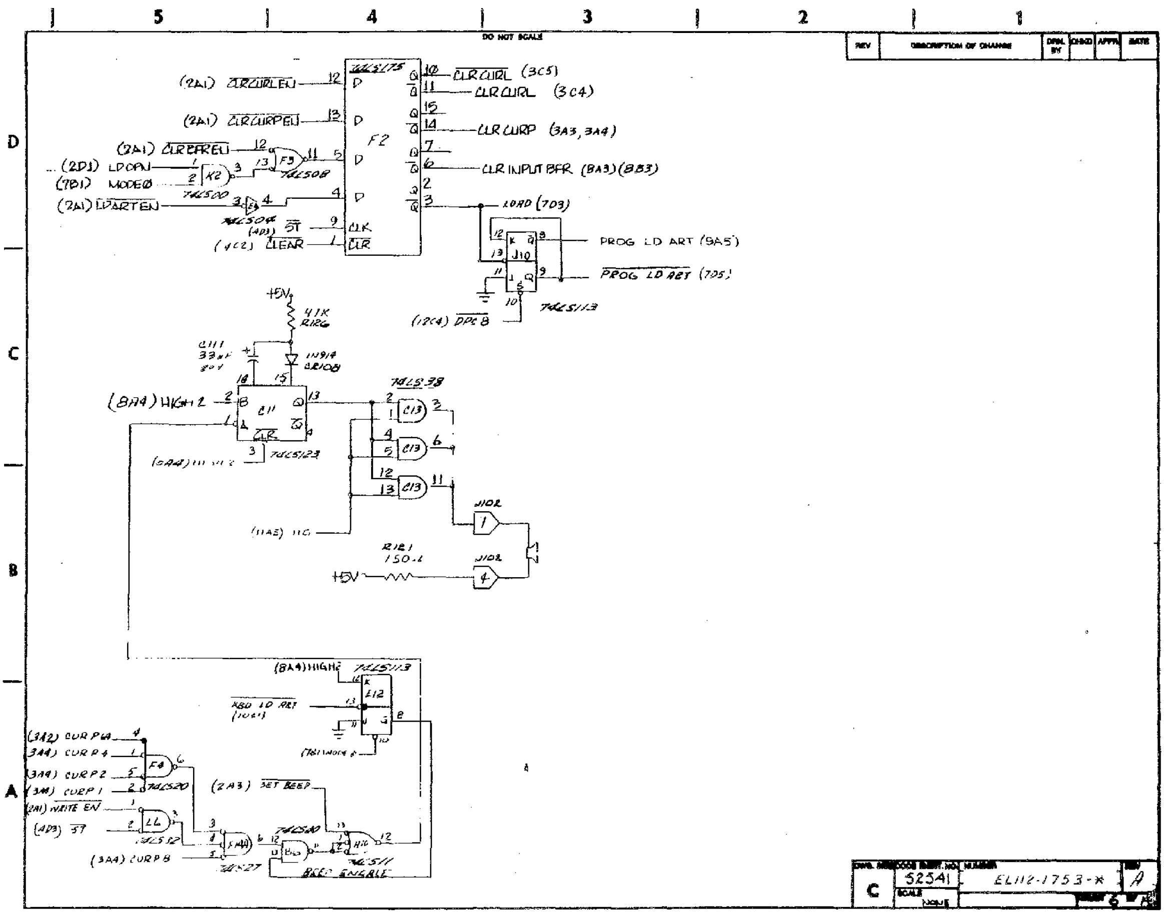
1 of 17 B150 Schematic

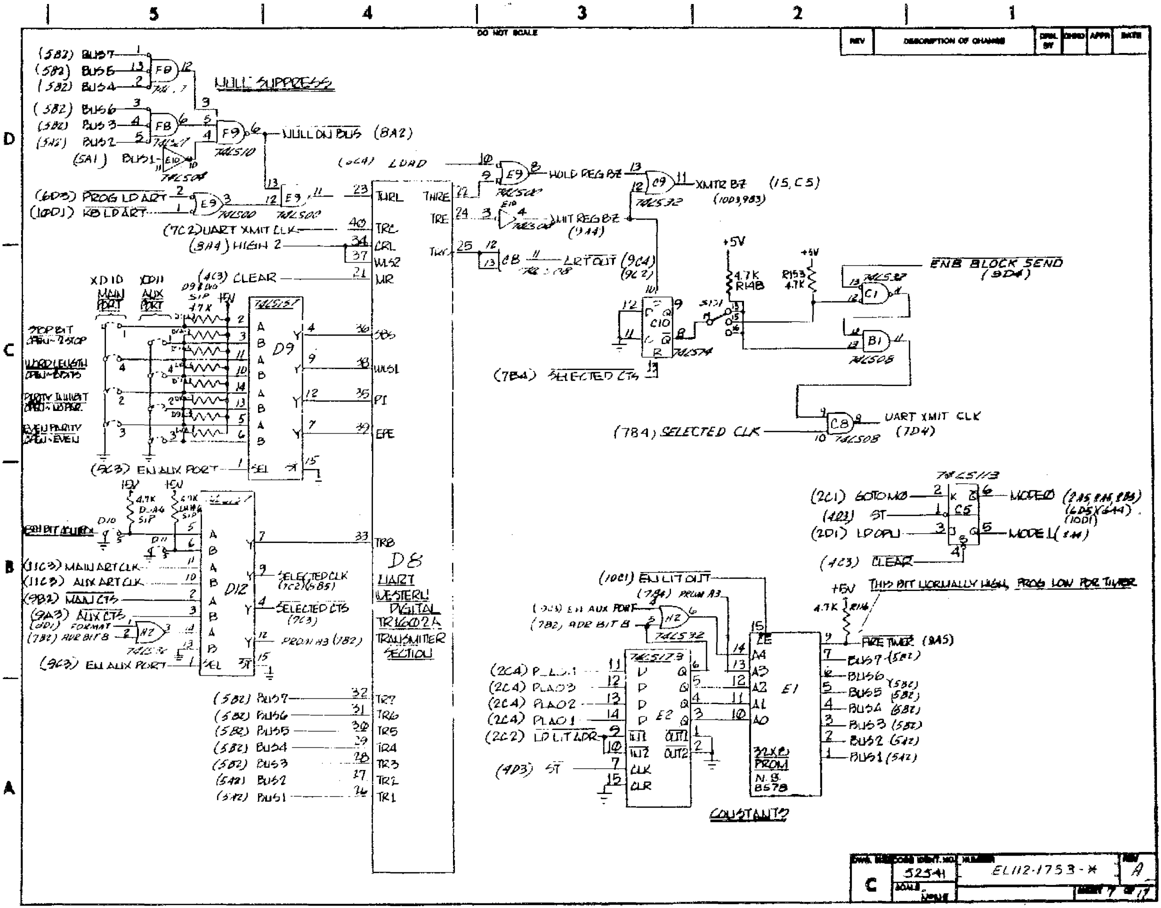

DO NOT SCALE
REV
DESCRIPTION OF CHANGE
DRN. BY
CHKD
APPR
DATE
74LS163
SEQUENCE COUNTER
OPERATION REGISTER
74LS113
74LS37
74LS04
74LS42
E4
LD OPN
SEQ5 (2B5)
GOTO MØ
74LS257
D5
E5
L2
PROG. LOGIC ARRAY
(2 LOCATIONS)
74LS138
J1
K1
H1
F1
LD REG
DECR BCUR
DECR BCURP
SET BEEP
INCR ROLL
(UOP-UNUSED)
INCR CURL
DECR CURL
LOAD CURL
INCR CURP
DECR CURP
LOAD CURP
FLIP FLOP CLK
PROT FLOP CLK
BLINK FLOP CLK
START TIME
CLR BCURL EN
EN AUX SEND
LD ARTEN
CLR BFR EN
CLR CURL EN
CLR CURP EN
WRITE EN
MODE Ø
MODE 1
C
52541
EL112-1753-M
A
NONE
5
4
3
2
1
D
C
B
A

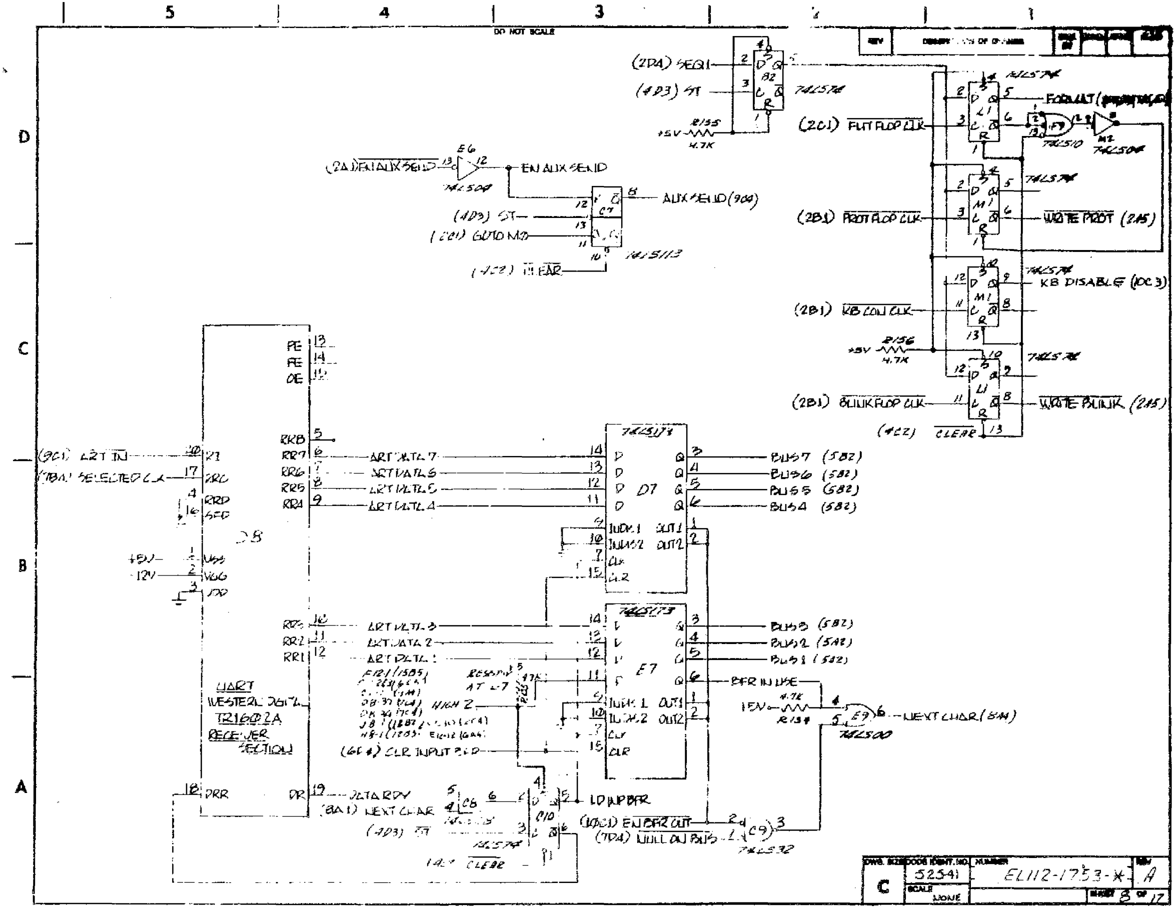

DO NOT SCALE
REV
DESCRIPTION OF CHANGE
DWN BY
CHKD
APPR
DATE
ROLL REGISTER
74LS161
F5
INCR ROLL
CLEAR
ROLL 1
ROLL 2
ROLL 4
ROLL 8 (13C4)
ROLL 16
MAX ROLL
74LS20
74LS74
7404
LOAD CURL
INCR CURL
DECR CURL
CLR CURL
74LS08
74LS32
74LS193
H5
CURSOR LINE REGISTER
CURL 1
CURL 2
CURL 4
CURL 8
CURL 16
CURL ILLEGAL
74LS00
74LS04
LOAD CURP
INCR CURP
DECR CURP
CLR CURP
K5
J5
CURSOR POSITION REGISTER
CURP 1
CURP 2
CURP 4
CURP 8
CURP 16
CURP 32
CURP 64
CURP ILLEGAL
ILLEGAL (2A5)
74LS10
DWG SIZE
CODE IDENT NO
NUMBER
C
52541
EL112-1753-X
SCALE NONE
SHEET 3 OF 17
A
B
C
D
5
4
3
2
1


DO NOT SCALE
REV
DESCRIPTION OF CHANGE
SCREEN REFRESH
CPC CARRY
STROBE ENABLED
74LS00
74LS27
74LS37
BLINK CLK. (15B4)
J9
CNTR CARRY (2B5)
CLEAR
74LS113
74LS11
74LS93
H4
L4
K4
J4
M4
M2
74LS04
HIGH 3
BCURP ILLEGAL
74LS32
D
C
B
A
52541
EL112-1753
5
4
3
2
1

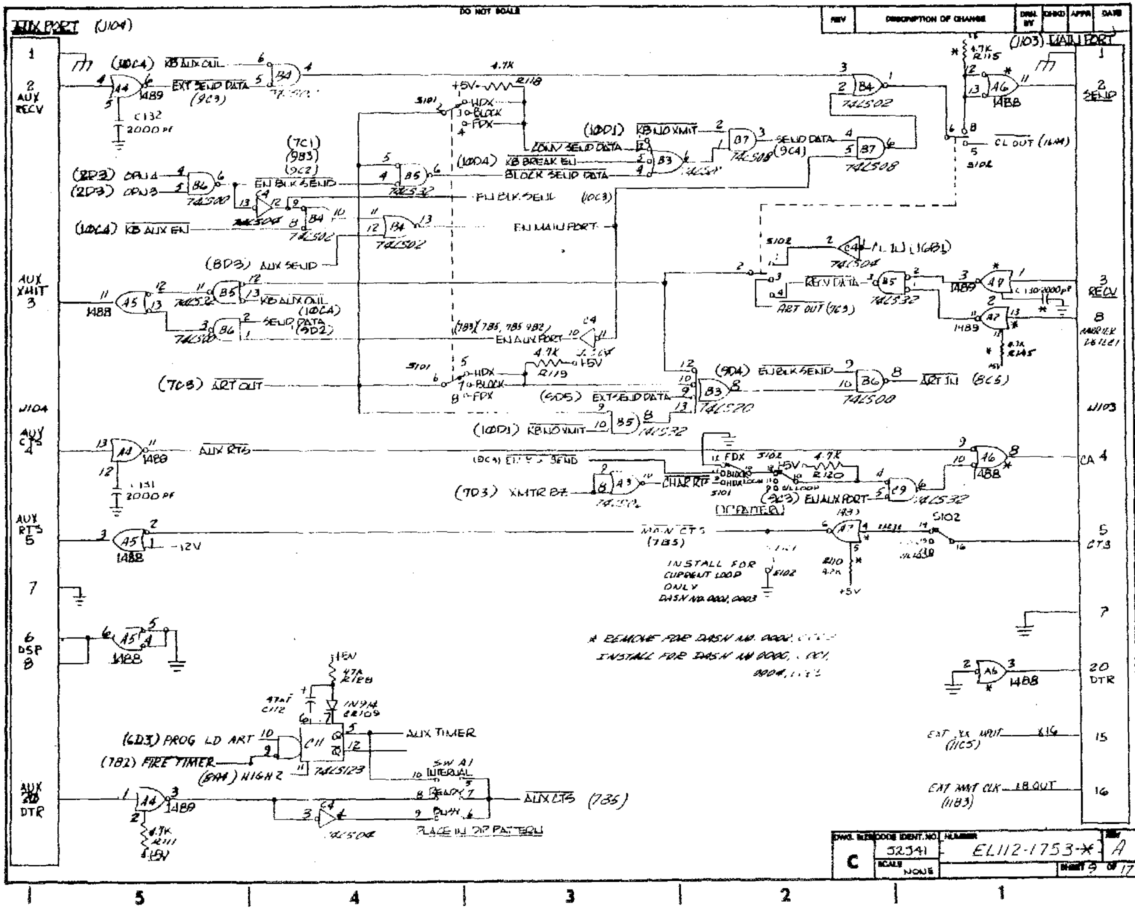

DO NOT SCALE
REV
DESCRIPTION OF CHANGE
DRN BY
CHKD
APPR
DATE
(BD) FORMAT
REG BLINK (2A5)
REG PROT (2A5)
MEMO7
MEMO6
MEMO5
MEMO4
MEMO3
MEMO2
MEMO1
MEMORY SHIFTER
LD REG
CLR REG
ELI REG OUT
K9
K8
L8
M8


DO NOT SCALE
REV
DESCRIPTION OF CHANGE
DRN BY
CHKD
APPR
DATE
74LS175
F2
CLR CURL (3C5)
CLR CURL (3C4)
CLR CURP (3A3, 3A4)
CLR INPUT BFR (8A3)(8B3)
LOAD (7D3)
PROG LD ART (9A5)
PROG LD ART (7D5)
74LS113
J10
DPC8
74LS08
74LS00
74LS04
74LS38
74LS123
74LS20
74LS32
74LS27
74LS10
74LS11
+5V
41K
R126
1N914
CR108
R121
150Ω
J102
HIGH 2
KBD LD ART
BEEP ENABLE
SET BEEP
WRITE EN
CURP 1
CURP 2
CURP 4
CURP 8
LD ART (10C1)
C
52541
EL112-1753-*
A

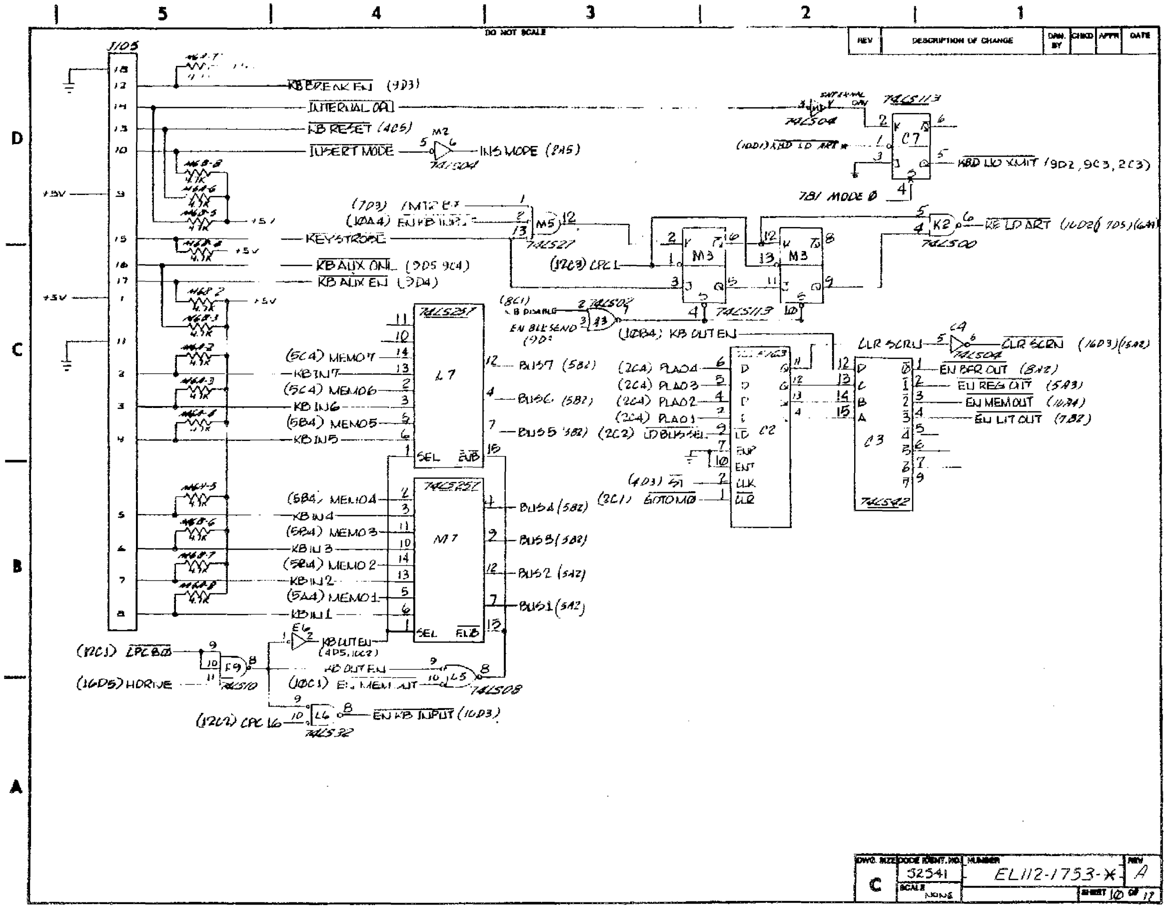

DO NOT SCALE
REV
DESCRIPTION OF CHANGE
NULL SUPPRESS
NULL ON BUS (8A2)
LOAD
HOLD REG BZ
XMTR BZ (15, C5)
PROG LD ART
KB LD ART
UART XMIT CLK
HIGH 2
CLEAR
LRT OUT
SELECTED CTS
ENB BLOCK SEND (9D4)
SELECTED CLK
UART XMIT CLK (7D4)
XD10 MAIN PORT
XD11 AUX PORT
STOP BIT
WORD LENGTH
PARITY INHIBIT
EVEN PARITY
EN AUX PORT
MAIN ART CLK
AUX ART CLK
MAIN CTS
AUX CTS
D8
UART WESTERN DIGITAL TR1602A TRANSMITTER SECTION
GOTO M0
ST
LD OPN
MODE 0
MODE 1
THIS BIT NORMALLY HIGH, PROG LOW FOR TIMER
EN LIT OUT
LD LIT ADR
FIRE TIMER (9A5)
32X8 PROM N.S. 8578
CONSTANTS
52541
EL112-1753-*
A
C

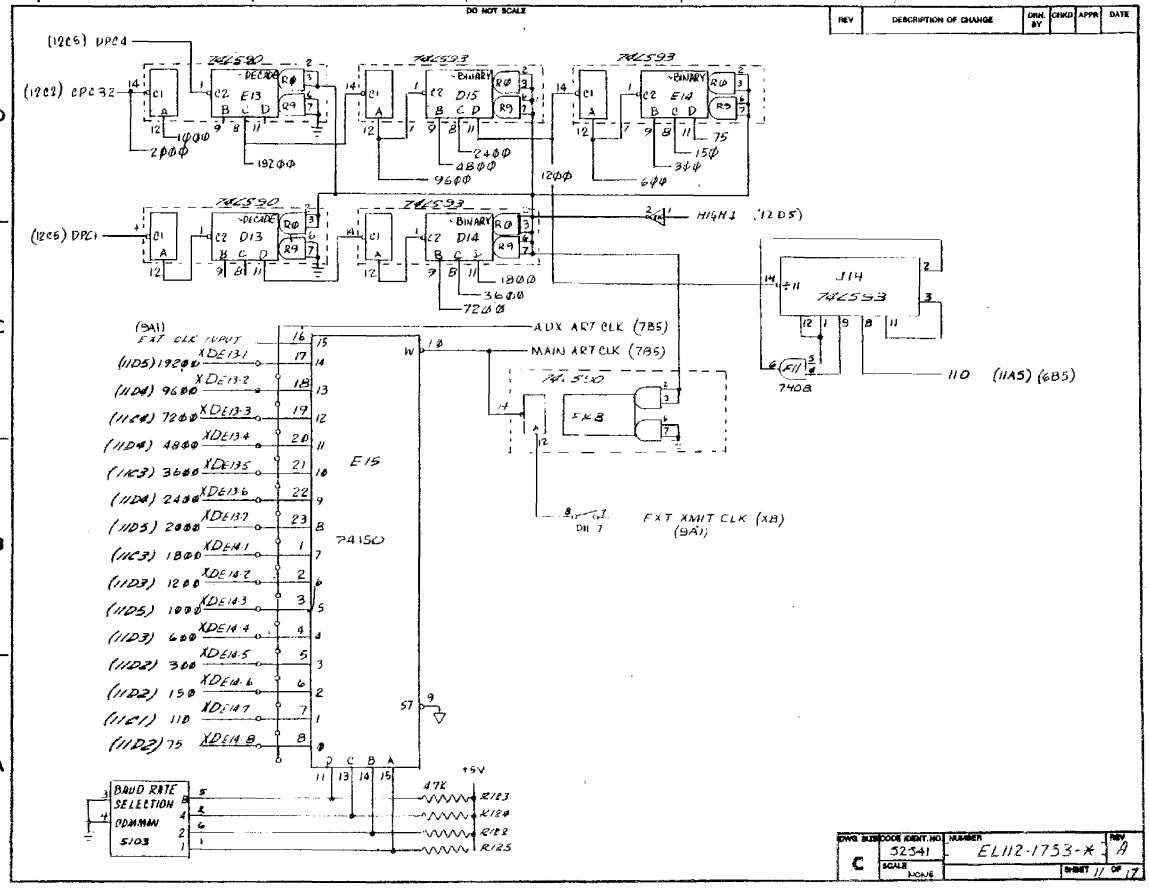


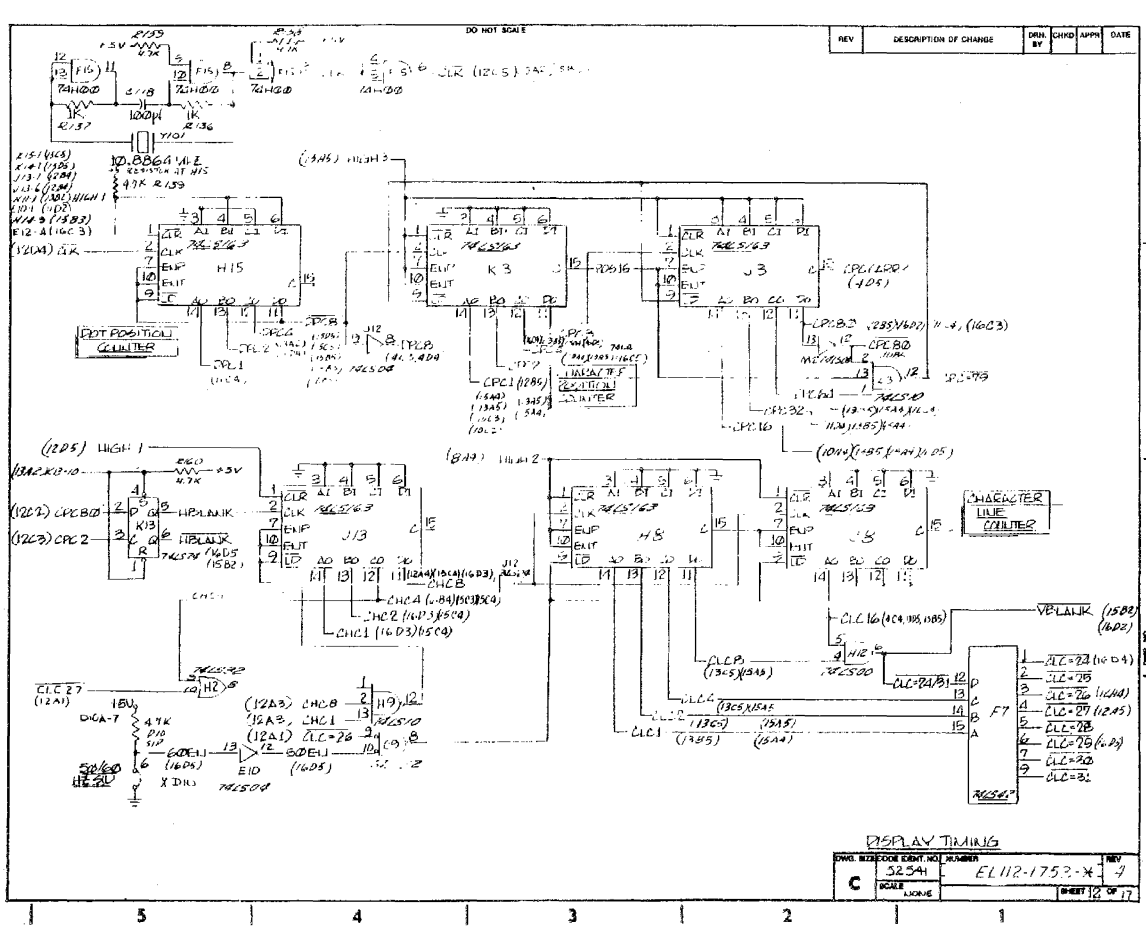
DO NOT SCALE
D
C
B
A
5
4
3
1
74LS74
FORMAT
(2C1) FLIT FLOP CLK
(2B1) PROT FLOP CLK
WRITE PROT (2A5)
KB DISABLE (10C3)
(2B1) KB CON CLK
(2B1) BLINK FLOP CLK
WRITE BLINK (2A5)
(4C2) CLEAR
(2D4) SEQ1
(4D3) ST
74LS74
74LS10
74LS04
R155 4.7K
R156 4.7K
(2A) EN AUX SEND
EN AUX SEND
AUX SEND (9D4)
(4D3) ST
(2C1) GUTO MD
(4C2) CLEAR
74LS04
74LS113
(9C1) ART IN
(7BA) SELECTED CLK
+5V
-12V
D8
UART
WESTERN DIGITAL
TR1602A
RECEIVER
SECTION
ART DATA 7
ART DATA 6
ART DATA 5
ART DATA 4
ART DATA 3
ART DATA 2
ART DATA 1
74LS173
D7
E7
BUS 7 (5B2)
BUS 6 (5B2)
BUS 5 (5B2)
BUS 4 (5B2)
BUS 3 (5B2)
BUS 2 (5A2)
BUS 1 (5A2)
BFR IN USE
NEXT CHAR (8A4)
74LS00
R134 4.7K
HIGH Z
(6C4) CLR INPUT BFR
DATA RDY
(8A1) NEXT CHAR
(4D3) ST
74LS74
LD INP BFR
(10C1) EN BFR OUT
(7D4) NULL ON BUS
74LS32
(4C2) CLEAR
5254I
EL112-1753-X
A
C
NONE
SHEET 8 OF 17

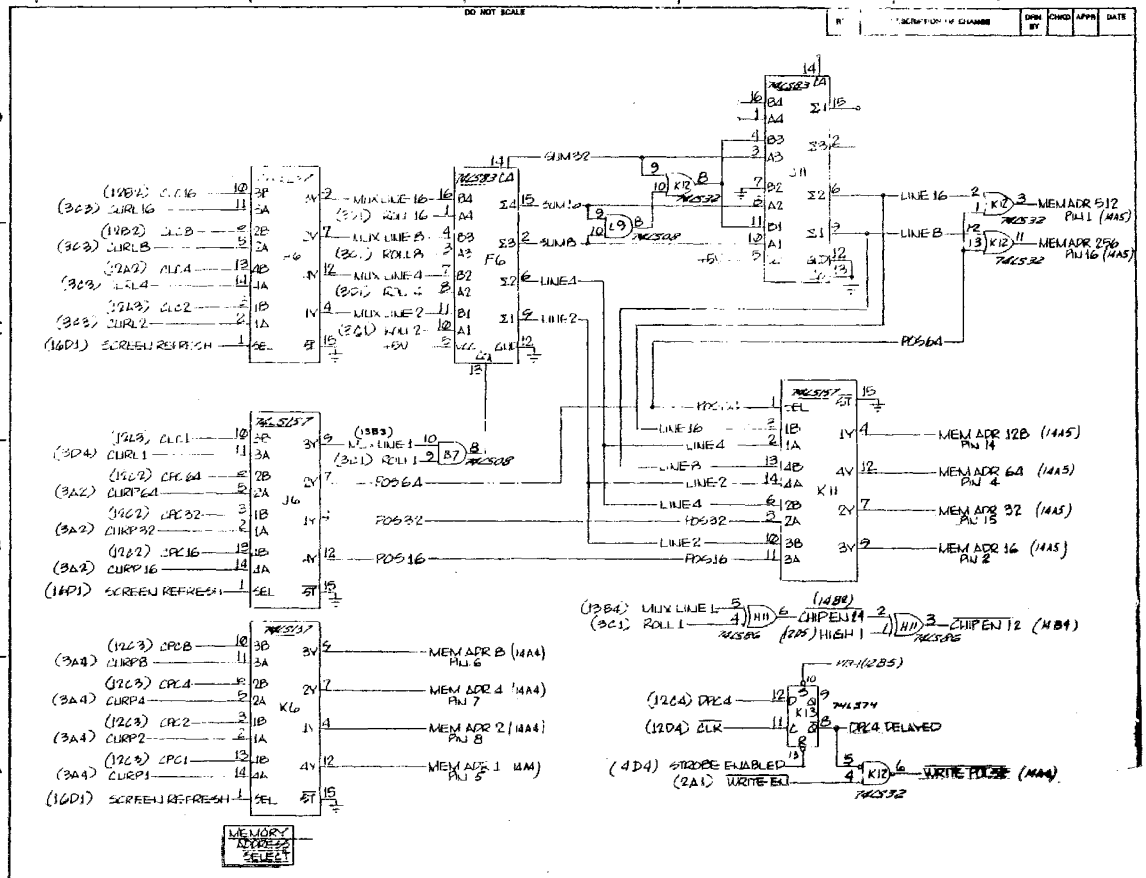


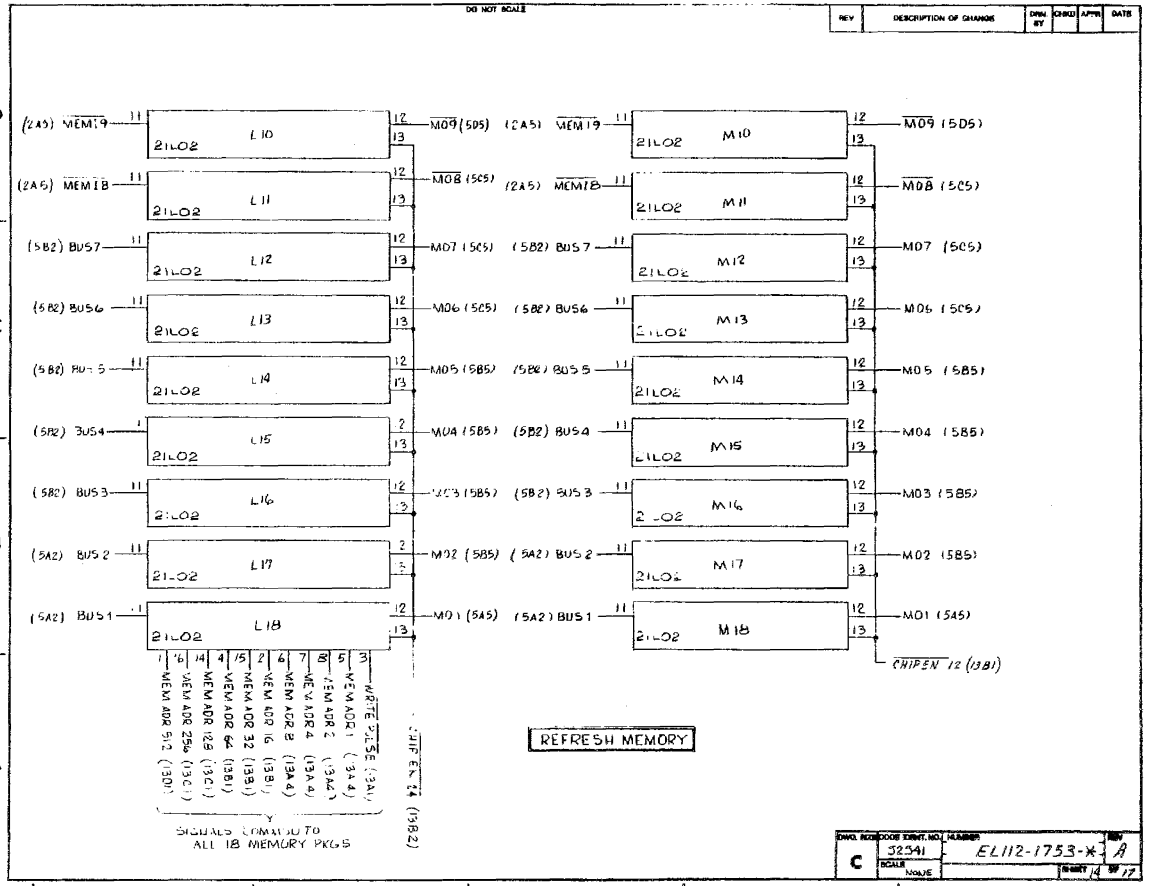
DO NOT SCALE
REV
DESCRIPTION OF CHANGE
DRN BY
CHKD
APPR
DATE
AUX PORT (J104)
(J103) MAIN PORT
AUX RECV
AUX XMIT
AUX CTS
AUX RTS
DSR
DTR
SEND
RECV
CARRIER DETECT
CTS
EXT SEND DATA
KB AUX OUT
SEND DATA
BLOCK SEND DATA
KB BREAK EN
EN BLK SEND
EN AUX PORT
EN MAIN PORT
AUX SEND
RECV DATA
ART OUT
ART IN
AUX RTS
CHAR RDY
XMTR BZ
MAIN CTS
INSTALL FOR CURRENT LOOP ONLY
AUX TIMER
PROG LD ART
FIRE TIMER
HIGH Z
AUX CTS
PLACE IN DIP PATTERN
CL OUT
EXT XX INPUT
EXT XMT CLK
DWG SIZE
CODE IDENT NO.
52341
NUMBER
EL112-1753-*
SCALE
NONE
SHEET 9 OF 17

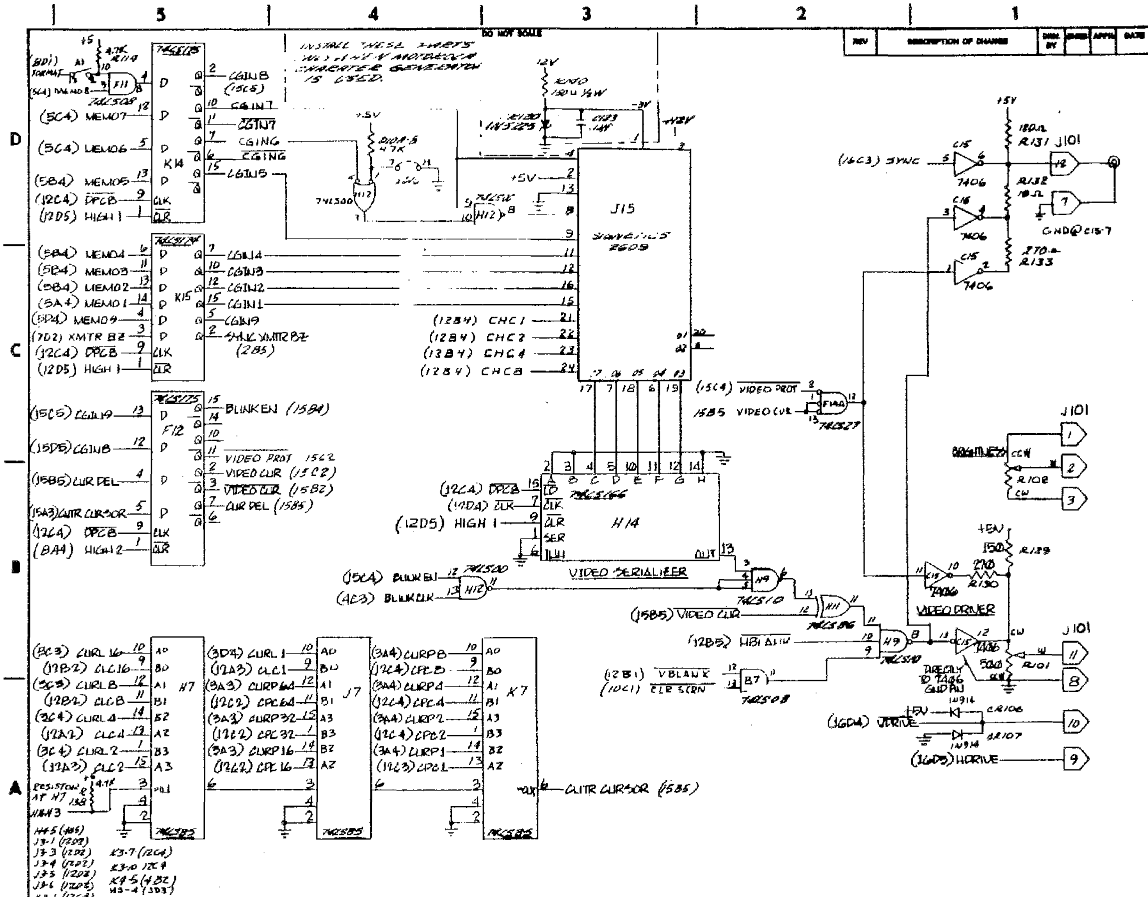

DO NOT SCALE
REV
DESCRIPTION OF CHANGE
DRN. BY
CHKD
APPR
DATE
J105
INTERNAL ON
KB RESET (4C5)
INSERT MODE
INS MODE (2A5)
KEYSTROBE
KB AUX ON (9D5 9C4)
KB AUX EN (9D4)
74LS04
74LS113
74LS27
74LS00
74LS257
74LS02
74LS163
74LS42
74LS10
74LS08
74LS32
(7D3) MODE Ø
KBD LD XMIT (9D2, 9C3, 2C3)
(1203) CPC L
(10B4) KB OUT EN
CLR SCRN
CLR SCRN (16D3)(15A2)
EN BFR OUT (8A2)
EN REG OUT (5A3)
EN MEM OUT (11B4)
EN LIT OUT (7B2)
(2C4) PLAD4
(2C4) PLAD3
(2C4) PLAD2
(2C4) PLAD1
(2C2) LD BUS SEL
(2C1) GOTO MØ
(5C4) MEMO7
KB IN7
(5C4) MEMO6
KB IN6
(5B4) MEMO5
KB IN5
(5B4) MEMO4
KB IN4
(5B4) MEMO3
KB IN3
(5B4) MEMO2
KB IN2
(5A4) MEMO1
KB IN1
BUS7 (5B2)
BUS6 (5B2)
BUS5 (5B2)
BUS4 (5B2)
BUS3 (5B2)
BUS2 (5A2)
BUS1 (5A2)
SEL
(12C1) CPC BØ
(16D5) HDRIVE
KB OUT EN (4D5, 10C2)
(10C1) EN MEM OUT
(12C2) CPC 16
EN KB INPUT (16D3)
+5V
4.7K
DWG. SIZE
C
CODE IDENT. NO.
32541
NUMBER
EL112-1753-X
REV
A
SCALE
NONE
SHEET 10 OF 17

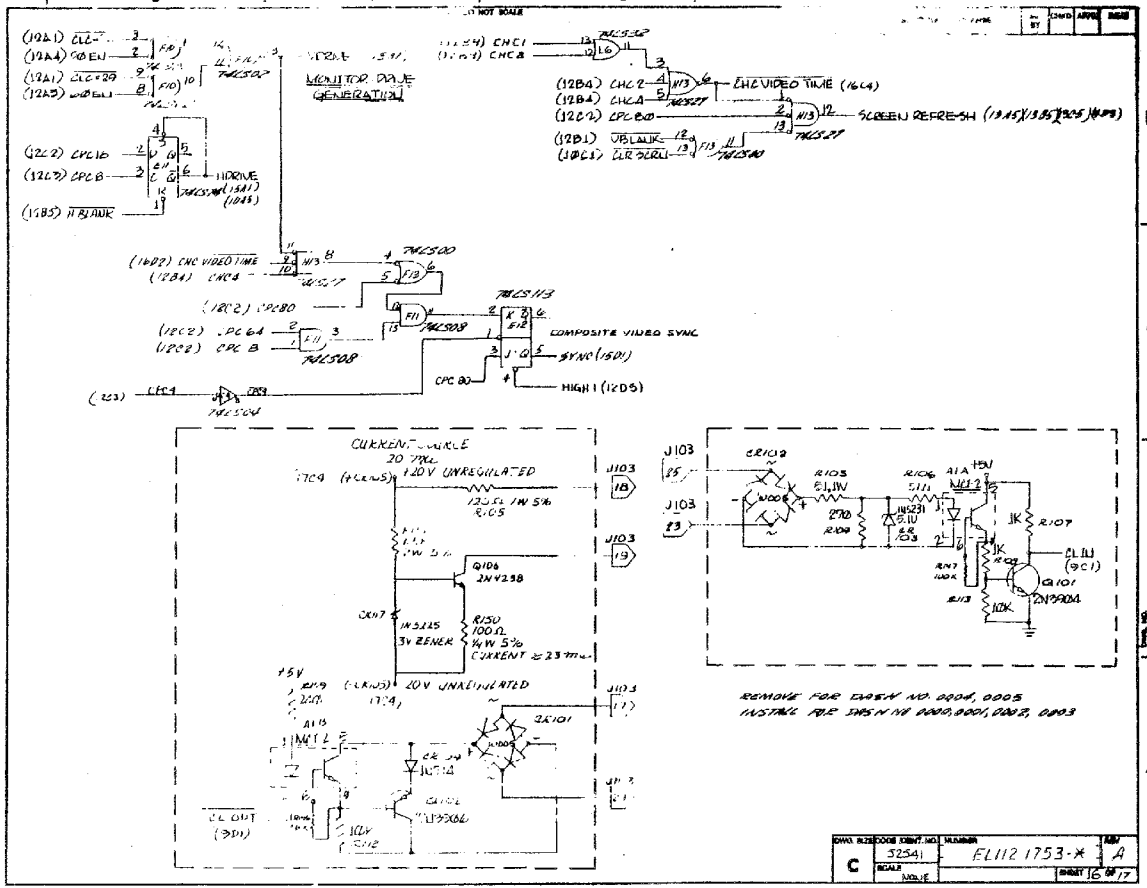

DO NOT SCALE
REV
DESCRIPTION OF CHANGE
DRN. BY
CHKD
APPR
DATE
74LS90
DECADE
74LS93
BINARY
(12C6) DPC4
(12C2) DPC32
(12C6) DPC1
1φφφ
2φφφ
192φφ
96φφ
48φφ
24φφ
12φφ
6φφ
3φφ
1φφ
75
HIGH1 (12D5)
J14
74LS93
740B
110 (11A5) (6B5)
(9A1)
EXT CLK INPUT
AUX ART CLK (7B5)
MAIN ART CLK (7B5)
74LS30
FXB
EXT XMIT CLK (X8)
(9A1)
E15
74150
(11D5) 19200
(11D4) 9600
(11C4) 7200
(11D4) 4800
(11C3) 3600
(11D4) 2400
(11D5) 2000
(11C3) 1800
(11D3) 1200
(11D5) 1000
(11D3) 600
(11D2) 300
(11D2) 150
(11C1) 110
(11D2) 75
BAUD RATE SELECTION
ODAMAN 5103
+5V
47K
R123
R124
R122
R125
DWG SIZE
CODE IDENT. NO
52541
NUMBER
EL112-1753-X
REV
A
C
SCALE
NONE
SHEET 11 OF 17


DO NOT SCALE
REV
DESCRIPTION OF CHANGE
DRN. BY
CHKD
APPR
DATE
DISPLAY TIMING
DWG. SIZE
CODE IDENT. NO.
52541
DWG. NUMBER
EL112-1753-X
REV
4
SCALE
NONE
SHEET 12 OF 17
DWG. NO. EL112-1753-X
12 of 17 B150 Schematic
6 12

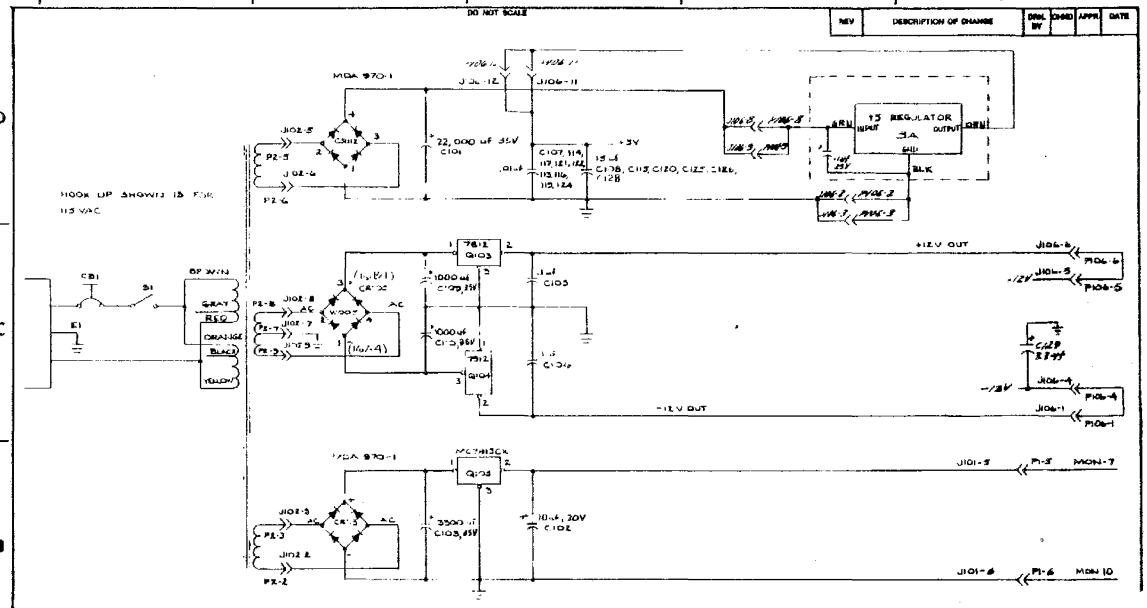

DO NOT SCALE
5
4
3
2
1
D
C
B
A
F6
J6
K6
K11
SCREEN REFRESH
MEMORY ADDRESS SELECT
LINE 16
LINE 8
LINE 4
LINE 2
POS64
POS32
POS16
MEM ADR 512 PIN 1 (4A5)
MEM ADR 256 PIN 16 (4A5)
MEM ADR 128 PIN 14
MEM ADR 64 PIN 4
MEM ADR 32 PIN 15
MEM ADR 16 PIN 2
MEM ADR 8 PIN 6
MEM ADR 4 PIN 7
MEM ADR 2 PIN 8
MEM ADR 1 PIN 5
CHIPEN 12 (4B4)
DRC4 DELAYED
WRITE PULSE (4A4)


DO NOT SCALE
REV
DESCRIPTION OF CHANGE
DRN BY
CHKD
APPR
DATE
L10
L11
L12
L13
L14
L15
L16
L17
L18
M10
M11
M12
M13
M14
M15
M16
M17
M18
21LO2
(2A5) MEM19
(2A6) MEM18
(5B2) BUS7
(5B2) BUS6
(5B2) BUS5
(5B2) BUS4
(5B2) BUS3
(5A2) BUS2
(5A2) BUS1
M09 (5D5)
M08 (5C5)
M07 (5C5)
M06 (5C5)
M05 (5B5)
M04 (5B5)
M03 (5B5)
M02 (5B5)
M01 (5A5)
CHIPEN 12 (13B1)
CHIP EN 24 (13B2)
MEM ADR 512 (13D1)
MEM ADR 256 (13C1)
MEM ADR 128 (13B1)
MEM ADR 64 (13B1)
MEM ADR 32 (13B1)
MEM ADR 16 (13B1)
MEM ADR 8 (13A4)
MEM ADR 4 (13A4)
MEM ADR 2 (13A4)
MEM ADR 1 (13A4)
WRITE PULSE (13A1)
SIGNALS COMMON TO ALL 18 MEMORY PKGS
REFRESH MEMORY
DWG. SIZE
C
DOOR PART NO.
32541
NUMBER
EL112-1753-X
REV
A
SCALE
NONE
SHEET 14 OF 17
D
C
B
A
5
4
3
2
1

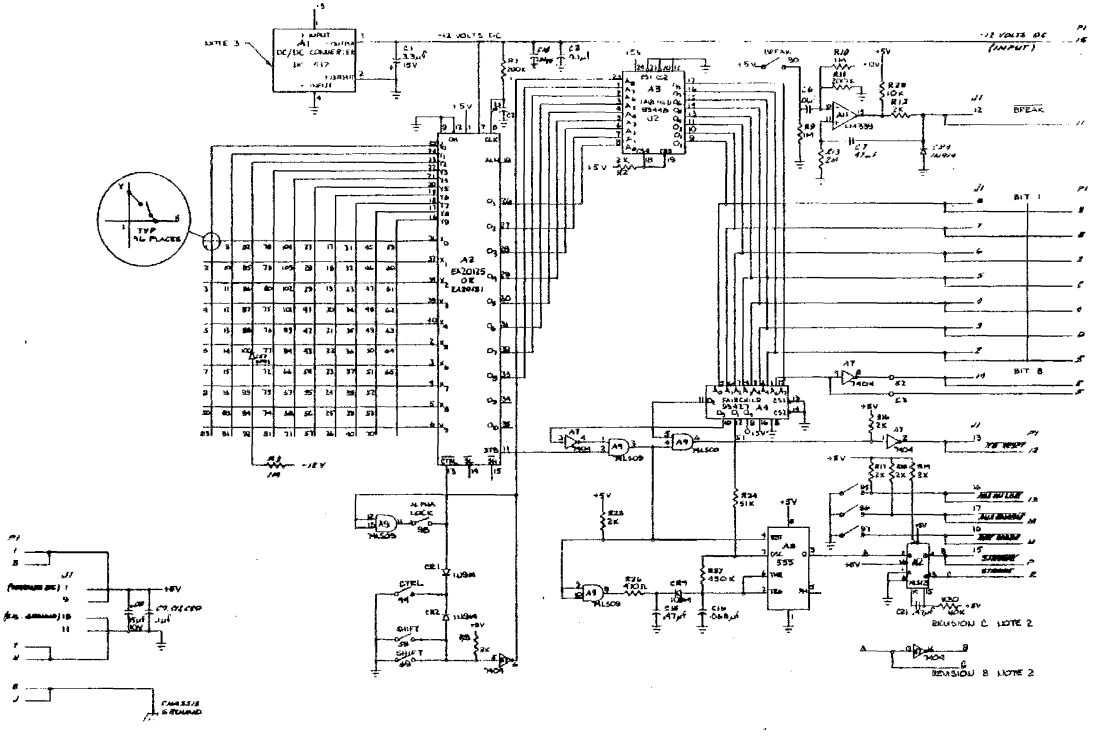

DO NOT SCALE
INSTALL THESE PARTS WHEN A MOTOROLA CHARACTER GENERATOR IS USED.
J15
SIGNETICS 2609
K14
K15
F12
H14
VIDEO SERIALIZER
VIDEO DRIVER
H7
J7
K7
J101
GND@C15-7
DIRECTLY TO 7406 GND PIN
CLTR CURSOR (15B5)
BLINKEN (15B4)
VIDEO PROT
VIDEO CUR
HBLANK
VBLANK
CLR SCRN
SYNC
VDRIVE
HDRIVE



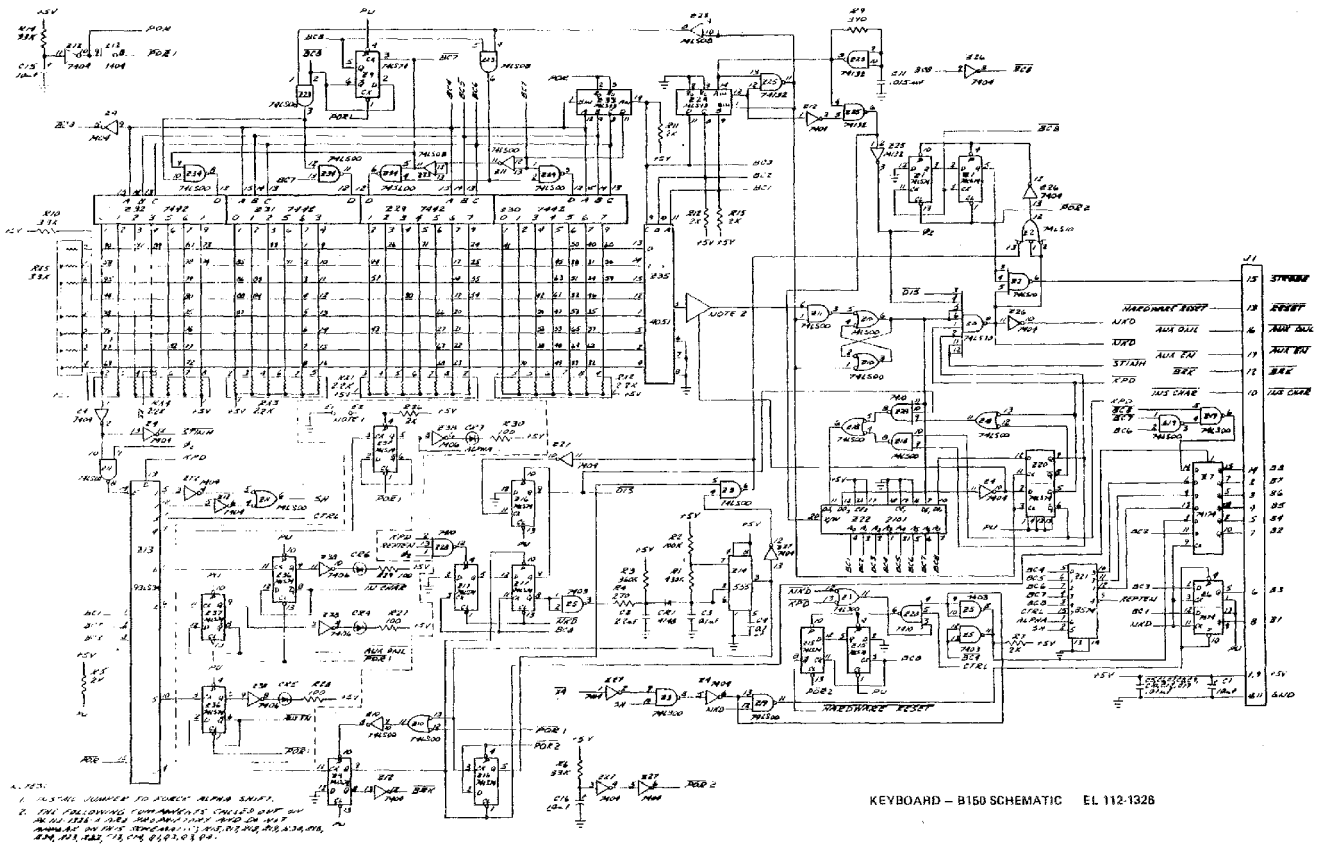
C	32541	FL112 1753-*	A		
SCALE	NONE	SHEET 16 OF 17			



17 of 17 B150 Schematic



KEYBOARD–B150 FOUR MODE
EL 112-1775
SCHEMATIC


KEYBOARD – B150 SCHEMATIC EL 112-1328

Appendix A

MONITOR

Section 1

GENERAL INFORMATION

1.1 MONITOR DESCRIPTION

The TV monitor is a solid-state unit for use in industrial and commercial installations where reliability and high quality video reproduction are desired.

The monitor features printed circuit board construction for reliability and uniformity. All circuits of the TV monitor are transistorized. The synchronization circuits have been custom designed to accept vertical and horizontal drive signals thus enabling the interfacing of this monitor with industrial or simple sync sources. This feature simplifies the user's sync processing and mixing and allows the unit to operate without requiring composite sync. The electronic packaging has been miniaturized for compatibility with small volume requirements.

Section 2

THEORY OF OPERATION

2.1 VIDEO AMPLIFIER

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101 and its components comprise the video output driver with a gain of about 17. Q104, operating as a class B amplifier, remains cutoff until a DC-coupled, positive-going signal arrives at its base and turns on the transistor.

R111 adds series feedback which makes the terminal-to-terminal voltage gain relatively independent of transistor variations as well as stabilizes the device against voltage and current changes caused by ambient termperature variations.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maxumum available contrast ratio.

The overall brightness at the screen of the CRT is determined by the negative potential at the grid and is varied by the brightness control.

2.2 VERTICAL DEFLECTION

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable resistor R116 and capacitors C105 and C106 form an RC network providing proper timing.

When power is applied, C105 and C106 charge exponentially through R115 and R116 until the voltage at the junction of R116 and C105 equals the anode "A" firing voltage. At this time, one of the unijunction's diodes that is connected between the anode and anode gate "G" becomes forward biased allowing the capacitors to discharge through another diode junction between the anode gate and the cathode "K" and on through R120.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter. Therefore, the changing of firing points from one device to another, together with the temperature dependency of this parameter, is no longer a problem as it can be with conventional unijunction transistors.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113. At the time of the vertical interval, an

external negative pulse is applied through R113, C104, and CR101 to the gate of Q102, causing the firing level of the unijunction to decrease.

The sawtooth voltage at the anode of Q102 is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and thereby maintains excellent impedance isolation between Q102 and Q104.

The output waveform from the unijunction oscillator is not suitable, as yet, to produce a satisfactory vertical sweep. Such a waveform would produce severe stretching at the top of the picture and compression at the bottom. C105 and C106 modify the output waveform to produce satisfactory linearity. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope. Slope change rate is determined by the position of the variable resistor R121.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power type transistor which operates as a class A amplifier. No output transformer is required since the output impedance of the transistor permits a proper impedance match with the yoke connected directly to the collector. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relative high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 whcih reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscillations by providing damping across the vertical deflection coils.

2.3 HORIZONTAL DEFLECTION

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. The circuitry associated with Q105 and Q106 has been designed to optimize the effeciency and reliability of the horizontal deflection circuits.

A positive going pulse is coupled through R127 to the base of Q105. The amplitude and duty cycle of this waveform must be as indicated in the electrical specifications (Section 1.2) for proper circuit operation.

The driver stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q105 into cut off, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

The horizontal output stage has five main functions: to supply the yoke with the correct horizontal scanning currents; develop a "C" VDC supply voltage for use with the CRT; develop a "B" VDC supply voltage for the video output stage; and develop a "D" VDC for the CRT bias.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltageplus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base which causes the output

circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

C113, in series with the yoke, also serves to block DC currents through the yoke and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not describe the same arc.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by C110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer-coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12 KV (9 and 12 inches) or 9 kV (5 inches), "C" VDC, and "B" VDC respectively. 12kV or 9 kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT The "B" VDC potentail is the supply voltage for the video output amplifier, Q101.

Section 3
PRELIMINARY ADJUSTMENTS

3.1 SYNCHRONIZATION AND DRIVE SIGNALS

Apply horizontal and vertical drive signals to the horizontal and vertical drive terminals as indicated on your schematic. Adjust their levels to a nominal +4 V peak-to-peak. The duty cycle of each signal must be adjusted as described in Section 1.2.

The horizontal drive signal is required to initiate horizontal scan and high voltage, and should be connected before applying power to the monitor.

3.2 BRIGHTNESS

Normally, the monitor will be used to display alphanumeric or other black and white information. Moreover, the video polarity is usually white characters on a black background.

The brightness control should be adjusted at a point where the white raster is just extinguished. The CRT will then be at its cutoff point, and a maximum contrast ratio can be obtained when a video signal is applied.

3.3 VIDEO CONTRAST

Q101 is designed to operate linearly when a +2.5 V signal is applied to its base. Some models incorporate a 500 ohm external contrast control to maintain this level of +2.5 V peak-to-peak when measured at the video input terminal of the printed circuit board edge connector. (Refer to the schematic.)

In all cases, the output DC impedance of the video signal source must be 500 ohms, or less.

3.4 VERTICAL ADJUSTMENTS

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

(1) Apply video and synchronization signals to the monitor.

(2) Set the vertical frequency control, R116, near the mechanical center for its rotation.

(3) Adjust the vertical height control, R124, for desired height.

(4) Adjust the vertical linearity control, R121, for best vertical linearity.

(5) Remove the vertical drive signal from the unit. Or, alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.

(6) Readjust the vertical frequency control, R116, until the picture rolls up slowly.

(7) Restore vertical drive to the monitor.

(8) Recheck height and linearity.

3.5 HORIZONTAL ADJUSTMENTS

Raster width is affected by a combination of the low voltage supply, width coil L101, and the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

(1) Apply video and synchronization signals to the monitor. insert the horizontal linearity sleeve about 2/3 of its length under the yoke. (If you received a monitor from the factory in which the placement of the linearity sleeve has been determined, make a mark on the sleeve and reinsert the sleeve to this mark when removal of the yoke and linearity sleeve are required.) If the linearity sleeve is inserted farther than necessary, excessive power will be consumed, and the horizontal output circuitry could be overstressed.

(2) Adjust the horizontal width coil, L101, for the desired width

(3) Insert the linearity sleeve farther under the yoke to obtain the best linearity. Although this adjustment will affect

the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.

(4) Readjust L101 for proper width.

(5) Observe final horizontal linearity and width, and touch up either adjustment if needed.

No horizontal hold control is used in this monitor. The raster should be properly locked and centered when the horizontal drive signals as described in Section 1.2 are used.

3.6 FOCUS ADJUSTMENT

The focus control, R107, provides an adjustment for maintaining best overall display focus. However, because of the construction of the gun assembly in the CRT, this control does not have a large effect on focus.

3.7 CENTERING

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

The ring magnets should not be used to offset the raster from its nominal center position because it would degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

Section 4

TROUBLESHOOTING AND MAINTENANCE

4.1 TROUBLESHOOTING GUIDE

SYMPTOM	POSSIBLE REMEDY
1. Screen is dark	Check "A" bus Q106, Q105, CR2
2. Loss of video	CR105, Q101
3. Power consumption is to high	Check horizontal drive waveform; Check proper placement of horizontal linearity sleeve; Q105, Q106

The voltage waveforms are shown in Fig. 1, and Fig. 2 is the interconnecting cabling diagram. Figure 3 shows the circuit board component locations.

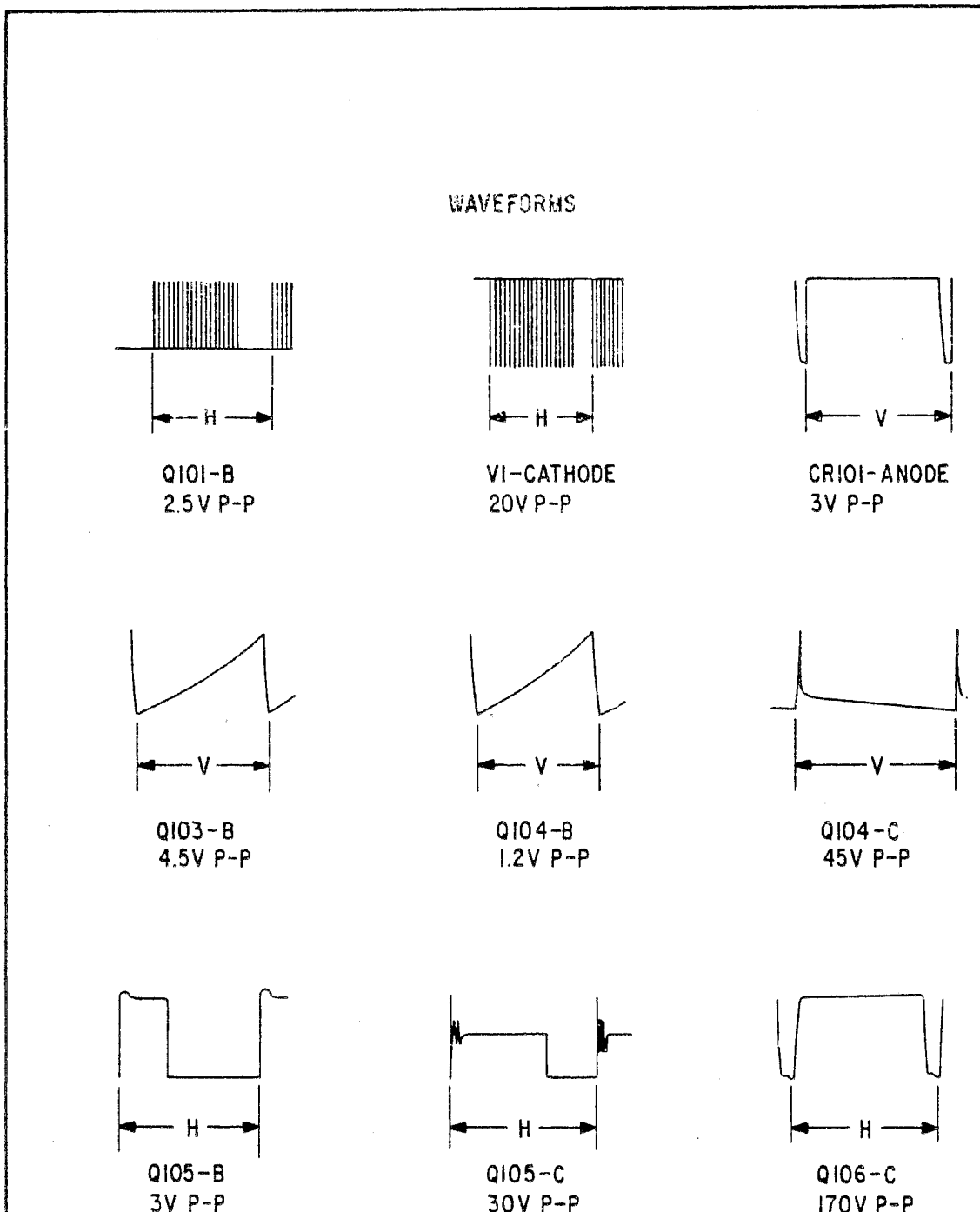


Fig. 1 Voltage Waveform

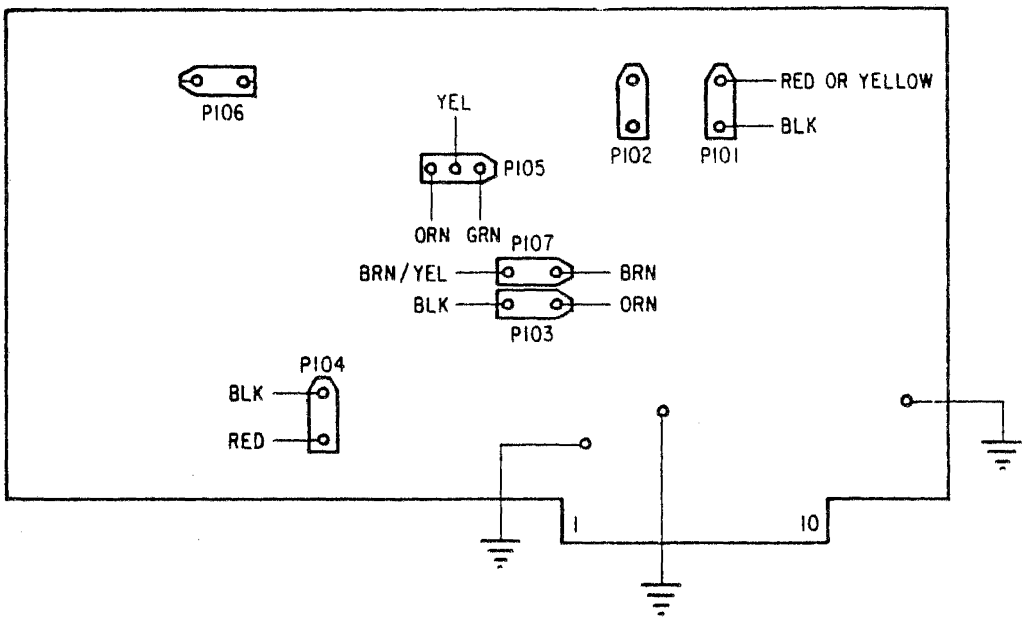
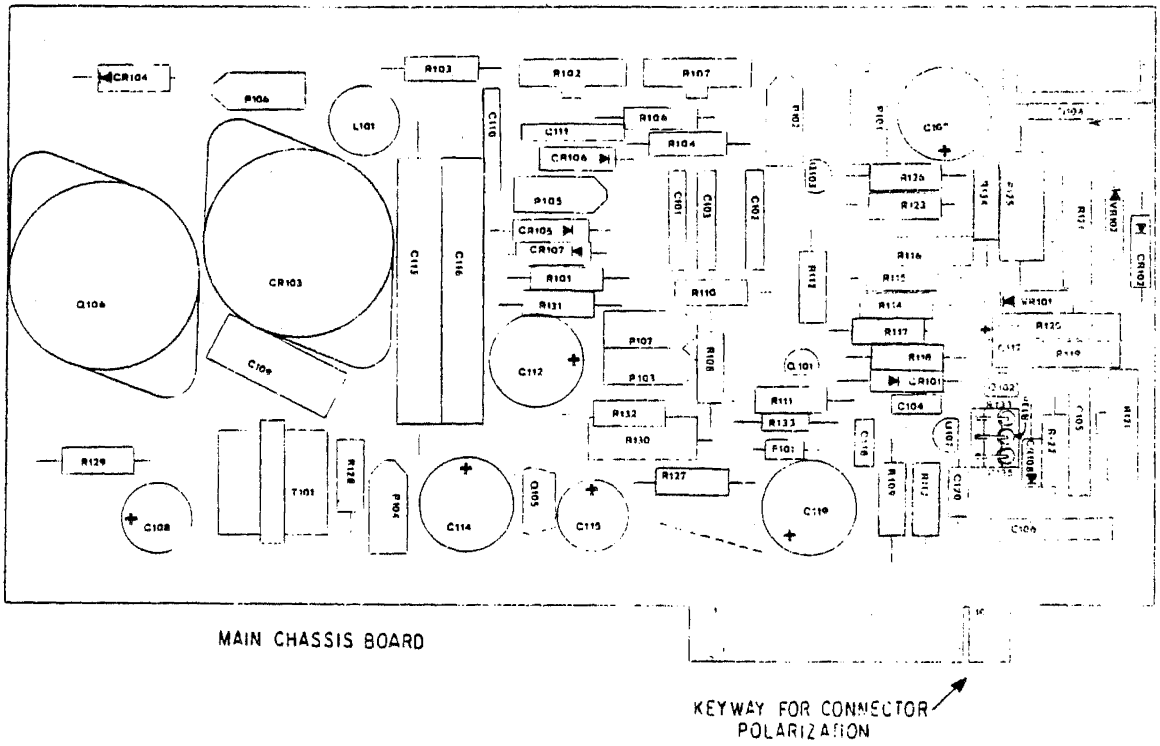
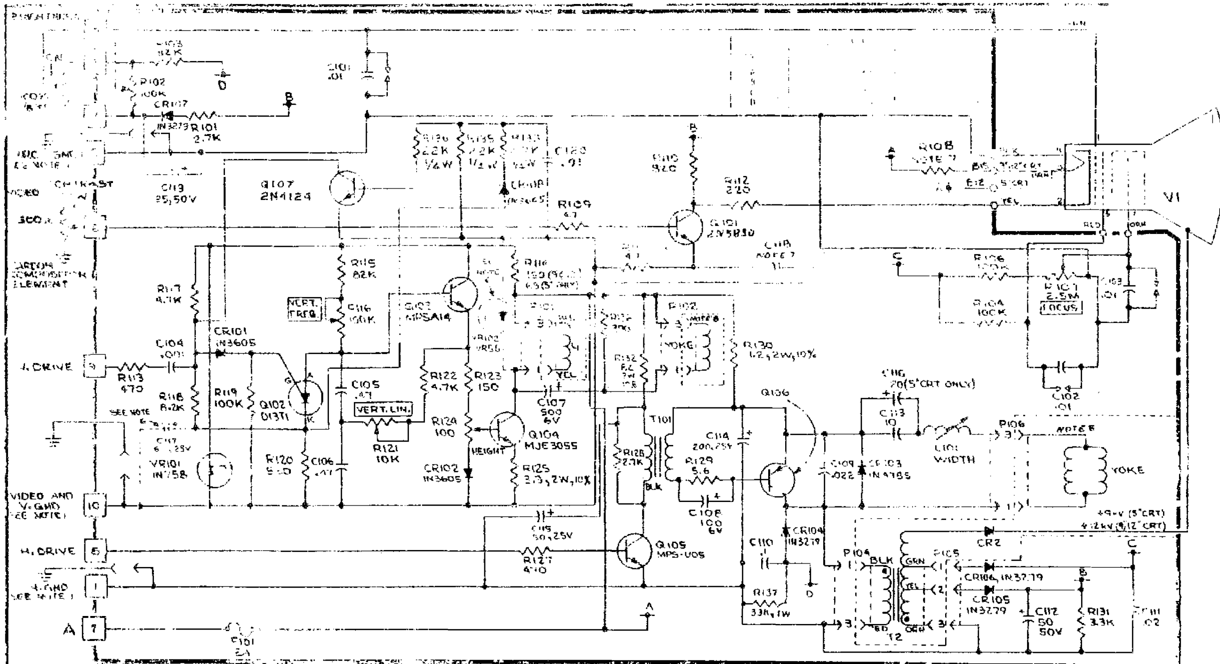


Fig. 2 Interconnecting Cabling Diagram



F101 AND R108 ARE USED ONLY WHEN LOW VOLTAGE POWER SUPPLY IS NOT SUPPLIED

Fig. 3 Circuit Board Components Location



8. Yoke Lead Identification:
P106-Blue and Red Leads.
P102 Green and Yellow Leads

NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE SECTION 2.2 OF MANUAL.
2. < ← DENOTES MOLEX PIN CONNECTOR.
3. ALL RESISTORS ARE 1/2 W ± 5%.
4. ALL CAPACITORS ARE IN uF.
5. ☐ DENOTES PRINTED CIRCUIT CARD EDGE CONNECTOR.

MOLEX CONNECTOR

A-12

Fig. 4 TV5, 9 and 12 Without Power Supply

Appendix B
GLOSSARY

ART DATA 1, 2, 3, 4, 5, 6, 7 – Asynchronous Receiver parallel output data lines bits 1 to 7.

$\overline{\text{ART IN}}$ – UART Receiver Serial Input Line - inputs come from I/O port, AUX port, and unit's own transmitter.

$\overline{\text{ART OUT}}$ – UART Serial Transmit Data line - transmits to I/O, AUX, and unit's own Receiver

ART XMIT CLK – X16 Clock used to clock data out of the transmitter

AUX ART CLK – X16 Clock used to clock data out of the transmitter when in an AUX mode

AUX CTS – AUX Clear to Send

AUX RTS – AUX port Request to Send

AUX SEND – Signal used to Enable AUX Port XMIT DATA Line

AUX TIMER – Timer used to Delay AUX Port CTS for Printer interface. This is a unit controlled delay

$\overline{\text{B CURL ILLEGAL}}$ – Buffered Cursor Line Illegal - Used to denote EOM line in Block Xmit.

$\overline{\text{B CURP ILLEGAL}}$ – Buffered Cursor Position Illegal - Used to denote EOM Position in Block Xmit.

BEEP ENABLE – Decode of Control "G" (007_8)

BFR IN USE – Denotes Receiver Buffer is in use and cannot receive another character for transfer to the bus

BLINK CLK – Clock of Binary Counter that clocks the blink memory

BLINK EN – Output of Blink Memory bit - enables Blink Clock to input to video

$\overline{\text{BLINK FLOP CLK}}$ – Clock used to Enable Blink Flop – Clock to Start Blink – Clock to Stop Blink – D type Flop

CLR BCURL EN – Clear Buffered Cursor Line Enable--- signals clears the registers storing the cursor line count in a block transmission

CLR BFR EN – Clear Buffer Enable - signal clears input buffer of receiver to a null

$\overline{\text{CLR CURL}}$ – Clear cursor line; resets cursor line registers to zero

$\overline{\text{CLR CURP}}$ – Clear cursor position; resets cursor position registers to zero

CLR REG – Clear register - signal which clears insert/delete character registers at output of memory.

$\overline{\text{CLR SCRN}}$ – Clear screen – command used to initiate screen blanking or video blanking for special operations

CLR SEQ – Clear Sequence - command used to clear sequence counter inputting PLA

CNTR CARRY – Counter Carry

CNTR CURSOR – Counter Cursor - final cursor compar output signal

CPC CARRY – Character position count carry– Counter Carry - Signal denoting 30ms time out has been completed.

CPC 1- – Character position Count = 1

$\overline{\text{CURL ILLEGAL}}$ – Cursor line illegal - signal which flags cursor line position as off displayable screen

$\overline{\text{CURP ILLEGAL}}$ – Cursor position illegal - signal which flags cursor position as off displayable screen

CURSOR LINE BUFFER – Buffer that is loaded to store cursor character position for block send operations.

CURSOR LINE REGISTER – Register containing current line position. Counts 0 to 23 up or down to depict cursor line count on display

CURSOR POSITION BUFFER – Buffer that is loaded to store cursor character position for block send operations.

CURSOR POSITION REGISTER – Register containing current cursor position Counts 0 to 79 up or down to depict cursor position within any one line on display

$\overline{\text{DECR BCURL}}$ – Decrement Block Cursor Line - Downcounts cursor line buffer containing stored line count in Block Send. When buffer is counted to zero, starting line count has been reached.

DECR BCURP - Decrement Buffer Cursor Position Register – This signal decrements the first of 2 Position Registers.

$\overline{\text{DECR CURL}}$ – Decrement Cursor Line - This signal will downcount cursor line register one count at a time

$\overline{\text{DECR CURP}}$ – Decrement Cursor Position. This signal downcounts cursor position register one count at a time.

$\overline{\text{DECR CURP 2}}$ - Decrement Cursor Position Register 2 - This signal decrements second of the 2 position registers, which will decrement cursor position 16 counts at a time.

DOT POSITION COUNTER – This counter is a divide-by-7 counter counting each of the 7-dot positions in one character scan

DR – Data Ready - This signal signifies a character has been loaded in the Receiver Buffer and is ready to be put in the bus.

DRR – Data Ready Reset – After character has been read on the bus, this signal will reset the receiver buffer and ready it for the next character to be received

EN AUX PORT – Enable Auxiliary Port - Signal will turn on Input/Output gates on Auxiliary port .

$\overline{\text{EN AUX SEND}}$ – Enable Auxiliary Send - Command signal which starts a block send out Auxiliary port.

$\overline{\text{EN BFR OUT}}$ – Enable Buffer Out - Command signal used to put receiver buffer on the bus for character receipt to display

$\overline{\text{EN BLK SEND}}$ – Enable Block Send - Command signal which starts block send out main port

$\overline{\text{EN LIT OUT}}$ – Enable Literal PRom Output - Signal used to put block send delimiter Rom on the bus

EN MAIN PORT – Enable Main Port - Signal will turn on Input/Output gates on main port.

$\overline{\text{EN MEM OUT}}$ – Enable Memory Out - Signal used to output contents of memory onto bus for block send output

$\overline{\text{EN REG OUT}}$ – Enable Register Out - Signal used to put stored contents of insert/delete registers onto the bus for restoration to new location in memory.

EXT CLK INPUT– External Clock Input - Input line on I/O port; a TTL times 16 clock on this input can externally clock the terminal (switch selectable to input)

EXT XMIT CLK (X8) – External Transmit Clock (times 8)- This is a TTL output clock at 8 times the baud rate which can be used to clock an external device (switch selectable to output)

FE – Framing Error - One of the unused outputs of the UART Receiver

FIRE TIMER - Signal used to start AUX port internal delay timer

$\overline{\text{FMT FLOP CLK}}$ - Format Flip Flop Clock - Clocking signal used to set or reset Format–Format On–Format Off

FORMAT – Term used to define an established protected-unprotected screen of data

H BLANK – Horizontal Blanking – Part of signal necessary for monitor display

H DRIVE – Horizontal Drive - Signal to monitor for horizontal deflection on CRT.

HOLD REG BZ – Holding Register Busy - Signal indicates the UART transmitter is holding a character to be transmitted

$\overline{\text{INCR CURL}}$ – Increment Cursor Line - Signal used to upcount cursor line register

$\overline{\text{INCR CURP}}$ – Increment Cursor Position - Signal used to upcount cursor position register

$\overline{\text{INCR ROLL}}$ – Increment Roll Register - This signal increments the roll counter for scroll feature; an upcount of this counter will add of this counter will add 80 positions to display.

$\overline{\text{INS MODE}}$ – Insert Mode - Signal indicates to PLA program that the input at this time is to be inserted into memory instead of overwritten in memory.

$\overline{\text{INTERNAL OPN}}$ – Internal Operation - This signal indicates the function under operation is internally controlled and not necessarily transmitted to the I/O ports

KB AUX EN – Keyboard Auxiliary Enable - Signal off keyboard which will enable the Auxiliary port on the terminal from the keyboard

$\overline{\text{KB AUX ONL}}$ – Keyboard Auxiliary On Line - Signal off keyboard which will enable the AUX port on line with with the main I/O port and the terminal

$\overline{\text{KB BREAK EN}}$ – Keyboard Break Enable - Signal off keyboard which fires break function in terminal

KB DISABLE – Keyboard Disable - Locks out keyboard entry

$\overline{\text{KB LD ART}}$ – Keyboard Load UART - Signal loads UART with character input from keyboard; similar to Keyboard Strobe

$\overline{\text{KB NO XMIT}}$ – Keyboard No Transmit - Signal flags an internal operation being done from keyboard and is not to be transmitted over the I/O ports.

KB OUT EN – Keyboard Output Enable - Timing signal used to enable keybaord input to display

$\overline{\text{KB RESET}}$ – Keyboard Reset - Signal is an output actuated by Control Home/Clear Command from keyboard; signal will reset all functions of terminal

KEY STROBE – Keyboard Strobe - Signal which tells unit a key is depressed on keyboard

$\overline{\text{LD ART EN}}$ – Load Asynchronous Receiver Transmitter Enable - Signal used to load UART buffers with characters from bus to be transmitted

$\overline{\text{LD BCUR}}$ – Load Buffered Cursor - Signals loads value of cursor location to cursor line and positon buffers for block send operation

LD BUS SEL – Load Bus Select - Signal will load which bus input device will be on the bus at a given time interval (Input Buffer, Memory, Literal PROM, Insert/Delete Register, Keyboard, etc.)

LD INP BFR – Load Input Buffer - Signal used to load the receiver bus input buffer with character to be placed on the bus

LD OPN – Load Operation - Command used to load the operation counter to specific operation; done by PLA. There are 15 that can be loaded.

LD SEQ – Load Sequence - Command used to load the sequence counter to a specific sequence within any operation or Mode 0. There are 15 sequences that can be loaded in Mode 0 or any of 15 operations.

$\overline{\text{LOAD CURL}}$ – Load Cursor Line - Signal will load cursor line register with bus value at time of command.

$\overline{\text{LD CURP}}$ – Load Cursor Position - Signal will load cursor position registers with bus value at time of command.

LD LIT ADR – Load Literal Address - Command used to instruct the load of the address of the literal PROM (Block Send Delimiter ROM)

$\overline{\text{MAIN ART CLK}}$ – Main UART Clock - Clock at 16 times the baud rate; main timing clock for transmit and receive

$\overline{\text{MAX ROLL}}$ – Maximum Roll - Register count equals 23; will automatically reset roll register

$\overline{\text{MEMORY SHIFTER}}$ – Name given to set of registers which do memory shift in insert/delete operations

MODE 0, 1 –Mode Zero, Mode One - State for PLAS; 15 sequences exist in Mode 0 and 15 operations of 15 sequences each exist in Mode 1

MR – Master Reset - Input to UART to do a reset of the UART device

NULL SUPPRESS – Name of circuit which decodes a Null on the bus and suppresses transmission of same

OPN 1-4 – Operation inputs 1, 2, 3, 4 - Binary value of each input: Input 1=1, Input 2=2, Input 3=4, Input 4=8. If operation 1–4 all equal a high operation 15 is decoded

PE – Parity Error - Unused output of UART which flags wrong parity receipt to the terminal

$\overline{\text{PROG LD ART}}$ – Program Load UART - Signal which loads the UART with characters from screen for block transmission

PROT BIT – Protect Bit - Signifies bit in memory which stores protected data fields for formated display

ROLL REGISTER – This is the register which is incremented in a Roll function (scroll)

SELECTED CLK – Selected Clock - Signifies 1 of 2 clock (baud) rates to be input to UART, either main port or auxiliary port rate.

SEND DATA – Transmit data line on main port

$\overline{\text{SET BEEP}}$ – Command which will fire bell one shot to give an audible alarm

ST – Strobe - This is the main timing strobe of the unit; all decodes and memory inputs are timed to strobe.

THRE – Transmitter Holding Register Empty

THRL – Transmitter Holding Register Load

TR 1-8 – Transmitter Receiver Input/Output bits 1 through 8

TRC – Transmitter Register Clock

TRE – Transmitter Register Empty

TRO – Transmitter Register Output

UART – Universal Asynchronous Receiver Transmitter (Transmit/Receive)

$\overline{\text{V BLANK}}$ – Vertical Blanking – Monitor drive signal.

VIDEO CURSOR – Name given to cursor signal when input to video drive circuit for display on CRT

VIDEO DRIVER – Name of circuit which drives final video output to CRT for display

$\overline{\text{VIDEO PROT}}$ – Video Protect - Name given to signal defining protected display area's output from memory bit

VIDEO SERIALIZER – 74166 serial shift register

WLS 1, 2 – Word Length Select 1 and 2

$\overline{\text{WRITE BLINK}}$ – Command given to start memory input as a blinking video display

$\overline{\text{WRITE EN}}$ – Write Enable - Command given to write a character to memory

$\overline{\text{WRITE PROT}}$ – Write Protect - Command given to start memory input of protected data fields for Format Display

Appendix C

PROGRAMMABLE LOGIC ARRAY INPUTS

PROGRAMMABLE LOGIC ARRAY INPUTS

MODE 0

PLA INPUT DESIGNATION	INPUT TERM	DESCRIPTION
I 13 I 12 I 11 I 10	SEQ4 SEQ3 SEQ2 SEQ1	This set of four inputs comes from the SEQUENCE counter and functions as the program counter. These four inputs do not change between Mode 0 and Mode 1.
I 9	SEQ5	This bit indicates to the program that an ASCII ESCAPE code has been received as a lead-in code and the next byte received is the second byte of an ESC sequence. This bit goes active upon receipt of an actual ESC code or is set directly from the keyboard if an ESC-type operation is desired.
I 8	MODE	This input indicates to the PROGRAMMABLE LOGIC ARRAY whether to interpret the inputs as Mode 0 or Mode 1 terms.
I 7	INSERT MODE	This is a function line from the keyboard which indicates to the program whether an alphanumeric input byte should be inserted into the text or overwrite the character under the cursor.
I 6 - I 0	BUS7 - BUS1	This set of seven inputs brings the bus information into the PLA. In Mode 0, the bus holds the contents of the data input buffer. This set is used to decode the incoming byte, regardless of source.

MODE 1

I 13 I 12 I 11 I 10	SEQ4 SEQ3 SEQ2 SEQ1	This set of four inputs comes from the SEQUENCE counter and functions as the program counter. These four inputs do not change between Mode 0 and Mode 1.
I 9	FORMAT	This active high signal indicates to the program whether the terminal is in the FORMAT mode, where protected data is recognized.
I 8	MODE	This input indicates to the PROGRAMMABLE LOGIC ARRAY whether to interpret the inputs as Mode 0 or Mode 1 terms.
I 7	ILLEGAL	This term is high when the cursor is taken off the displayable portion of the screen. It also goes high for one cycle when the stored cursor location (BCURP and BCURL) is decremented and underflows. This indicates that the cursor has been returned to its original location on the screen.
I 6 - I 3	OPN4 - OPN1	These four bits are outputs from the OPERATION REGISTER which indicates the function being accomplished in Mode 1.
I 2	CARRY	This input is used when the 30 millisecond timer is being used. The timer is fired, which drops this bit low. It goes high at the end of the timeout. When not being used, this bit pulses.
I 1	PROTECT BIT	This input goes high when the FORMAT MODE is "on" and the byte under the cursor is protected.
I 0	XMTR BUSY	This bit is high when the transmitter is sending a byte.

PROGRAMMABLE LOGIC ARRAY OUTPUTS

INSTRUCTION	OUTPUT 87654321	DESCRIPTION
GROUP 1		
load REG	–A...AAA	loads REG1 with byte from memory, REG1 byte shifted to REG2
decr BCURL	–A...AA–	decrements the stored cursor count, underflows when on proper line.
decr BCURP	–A...A–A	decrements the stored position count, underflows when on proper character position. No action unless BCURL has underflowed, indicating that the cursor is on the proper line.
set BEEP	–A...A––	activates the one-shot controlling the beeper.
clear REG	–A...–AA	clears REG2 to a null code and REG1 to a space code.
decr CURP 2	–A...–A–	used to move the cursor to the last position of a line (CPC=79).
incr ROLL	–A...––A	increments the ROLL counter which causes the data on the screen to shift up one character line. The top line goes to the bottom.
GROUP 2		
FORMAT clock	–AAAA...	issues a clock pulse to the FORMAT flip-flop. Whether the flop will "set" or "clear" is controlled by the LSB of the SEQ counter.
PROTECT clock	–AAA–...	issues a clock pulse to the PROTECT flip-flop. Whether the flop will "set" or "clear" is controlled by the LSB of the SEQ counter.
KB CONTROL clock	–AA–A...	issues a clock pulse to the KEYBOARD DISABLE flip-flop. Setting or clearing is controlled by the LSB of the SEQ counter.
BLINK clock	–AA––...	issues a clock pulse to the BLINK flip-flop. Setting or clearing is controlled by the LSB of the SEQ counter.
start TIME	–A–AA...	this command is issued when the 30 millisecond timeout is desired. The CARRY input to the PLA is used to sense the timeout.

NOTE: GROUP 1 and GROUP 2 instructions can be combined to accomplish two operations in the same instruction time. If only one instruction is desired, the undesignated bits should be programmed to "–'s". (e.g., clear REG alone is –A––––AA; clear REG and start TIME is –A–AA–AA.)

GROUP 3		
clear BCURL	––...AAA	clears the character line portion of the stored cursor location. This indicates that the cursor is on the same line as the originally stored cursor line.
EN AUX SEND	––...AA–	this command enables transmission out the AUXILIARY PORT and disables transmission of data out the MAIN I/O PORT.
load UART	––...A–A	loads the UART transmitter holding reg with the contents of the bus. The loading actually takes place on the next instruction cycle.
clear BUFFER	––...A––	clears the input buffer to a null code.
clear CURL	––...–AA	clears the cursor line reg (sends the cursor to the top line).
clear CURP	––...–A–	clears the cursor position reg (sends the cursor to the beginning of the line).
WRITE	––...––A	writes the bus data into the refresh memory.
GROUP 4		
incr CURL	––AAA...	moves the cursor down one line (increments the CURL reg).
decr CURL	––AA–...	moves the cursor up one line (decrements the CURL reg).
load CURL	––A–A...	subtracts octal 40 from the contents of the bus and loads the CURL reg.
incr CURP	––A––...	advances the cursor once (increments the CURP reg).
decr CURP	–––AA...	backspaces the cursor once (decrements the CURP reg).
load CURP	–––A–...	subtracts octal 40 from the contents of the bus and loads the CURP reg.
load BCUR	––––A...	saves the current cursor line count and cursor position count in BCURL and BCURP, respectively.

NOTE:
1. The execution of GROUP 3 instructions LOAD UART, CLEAR BUFFER, CLEAR CURL, and CLEAR CURP actually takes place during the cycle following the issuing of the instruction.
2. GROUP 3 and GROUP 4 instructions can be combined to accomplish two operations in the same instruction time. If only one instruction is desired, the undesignated bits should be programmed with –'s.

PROGRAMMABLE LOGIC ARRAY OUTPUTS
(concluded)

INSTRUCTION	OUTPUT 87654321	DESCRIPTION
GROUP 5		
load SEQ	AAAAxxxx	used to preset the SEQ counter and accomplish a program "jump". The xxxx portion identifies the desired SEQ count.
load OPN	AAA–xxxx	used to preset the OPN register which designates Mode 1 operations. All operations in Mode 1 are identified by a different OPN count (ADVANCE is OPN=A–AA). This OPN register is a PLA input in Mode 1 only. Issuing this instruction in Mode 0 causes a move to Mode 1. The xxx portion identifies which operation will be loaded.
load LIT ADDR	AA–Axxxx	used to load the addressing register of the LITERAL PROM, which governs what delimiters will be transmitted in the block-type transmissions. The xxxx portion identifies the address to be loaded.
BUS BUFFER	A–AAxAAA	data input buffer is gated to the bus.
BUS REG	A–AAxAA–	REG2 is gated to the bus.
BUS MEM	A–AAxA–A	output of the refresh memory is gated to the bus
BUS LIT	A–AAxA––	LITERAL PROM is gated to the bus. (**NOTE:** If x=0, the screen refresh is maintained for the course of the operation. If x=1, the refresh will be terminated until the completion of the current operation.)
GOTO MO	A–––xxxx	this instruction terminates any Mode 1 operation and returns the program to its "idle" state. The x's have no significance in this instruction and are usually programmed to -'s.

OPERATION CODE ASSIGNMENT

OPN #	FUNCTION	DESCRIPTION
0	CLEAR TO END OF SCREEN	This routine clears the screen to nulls starting at the cursor location and terminating at the end of the screen. This does not include any bytes which can be recognized as protected.
1	CLEAR TO END OF LINE	Same as described above, except that the operation terminates at the end of the line containing the cursor.
2	FORWARD PROTECT TEST	Tests to see if the byte under the cursor is protected. If so, the cursor will advance to the right and down if necessary.
3	BACKWARD PROTECT TEST	Tests to see if the byte under the cursor is protected. If so, the cursor will move to the left and up, if necessary.
4	ADVANCE	Moves the cursor one position to the right and tests to see if the cursor moved off the displayable portion of the line. If so, the cursor is sent to the first position of the current line and the program goes to the LINE FEED routine.
5	BACKSPACE	Moves the cursor one position to the left and tests to see if the cursor moved off the beginning of the line. Given this condition, the cursor is sent to the last position of the current line and the program moves to the UP routine.
6	LINE FEED	Moves the cursor down one line and tests to see if the cursor left the bottom of the page.
7	UP	Moves the cursor up one line and tests to see if the cursor left the top of the page, in which case the cursor is sent to the bottom line.
8	INSERT CHARACTER	Starts at the cursor position and moves all data to the end of the line or the first protected field one position to the right.
9	DELETE CHARACTER	Starts at the cursor position and moves all data to the end of the line or the first protected field one position to the left.
10	FORMAT TAB	Searches for the next protected field. Places the cursor in the first unprotected location following this field. If no protected field is found before the end of the page, the cursor is sent home.
11	RETURN CURSOR	Moves the cursor forward and simultaneously decrements the stored cursor count until the cursor count underflows. The cursor is now positioned in its original location.
12	FUNCTION KEY SEND	Sends the constants surrounding the lower-case code generated by the depression of a Function key.

OPERATION CODE ASSIGNMENT
(concluded)

OPN #	FUNCTION	DESCRIPTION
13	SEND TEXT	Sends the data from the refresh memory during a block-send operation. Also recognizes the points at which delimiters should be sent.
14	START SEND	Sends the two start-of-message codes from the LITERAL PROM and positions the cursor for the transmission of text.
15	SEND DELIMITERS	Sends the proper delimiters at the end of an unprotected field, end of line, and the end of the message.

```
                EMI  BUS        OUTPUT          MODE 0
           SEQ SQN  BITS         BITS
           4321CQS7654321      87654321
                           *A LLLLLLLL
                                          **  CONTROL CODES INSTRUCTIONS **

*P 05 *I LLLL-L-LLLLLLL *F  AAAAAAAA ;LOAD SEQ 0 (IDLE,WAIT ON NULL)          100
*P 42 *I LLLHLL-HHHHHHH *F  AAA-AA-A ;LOAD OPN 2 (FORWARD PROT TEST)DEL CODE  101

*P 21 *I LLHLLL-LLLHHLH *F  ------A- ;CLEAR CURP  (CARRIAGE RETURN) CTL M     102

*P 06 *I LLHLLL-LLLHLHL *F  AAA-A--A ;LOAD OPN 6 (DOWN, LF CODE)              103

*P 61 *I LLHLLL-LLLHLLL *F  AAA-A-A- ;LOAD OPN 5  (BACKSPACE) CNT H           200

*P 57 *I LLHLLL-LLLLHHH *F  -A---A-- ;SET"BEEP" (BELL) CNT G                 201

*P 89 *I LLHLLL-LLLHLLH *F  AAA--A-A ;LOAD OPN 10 (FORMAT TAB) CNTL I        247

*P 76 *I LLHLLL-LLHHLHH *F  AAAA---- ;LOAD SEQ 15 (ESC CODE 033)             202
*P 00 *I HHHHLL-------- *F  ----AA-- ;LOAD BCUR,CLEAR INPUT BUFFER           107
                                     OVERFLOW OF SEQUENCE COUNTERS SETS
                                     ESCAPE BIT (SEQ 5)

*P 43 *I HLHLLL-LL----- *F  AAA-AA-A ;LOAD OPN 2 (FORWARD PROT TEST)         104
                                     STOP UNUSED CONTOL CODES HERE

*P 76 *I HLHHLLH------- *F  -A---AAA ;LOAD REG (INSERT ON SAVE BYTE REG1)    400
*P 67 *I HHLHLLH------- *F  AAA--AAA ;LOAD OPN 8 (INSERT CHARACTER)          401

*P 14 *I HHLLLL-------- *F  -------A ;WRITE ALL CODES EXCEPT CTRL AND DEL     105
*P 04 *I HHHLLL-------- *F  AAA-A-AA ;LOAD OPN 4 (ADVANCE AFTER WRITE)       106

                                     ** ESCAPE CODES INSTRUCTIONS **
*P 64 *I LLLHHL-------- *F  ----A--- ;LOAD BCUR (SAVE CURSOR LOCATION)       245
                                     ON ANY ESCAPE CODE

*P 84 *I LLHLHL-HLLLLLH *F  AAA-A--- ;LOAD OPN 7 (UP) ESC A                  208

*P 66 *I LLHLHL-HLLLLHL *F  AAA-A--A ;LOAL OPN 6 (DOWN) ESC B                209

*P 86 *I LLHLHL-HLLLLHH *F  AAA-A-AA ;LOAD OPN 4(ADVANCE) ESC C              210

*P 62 *I LLHLHL-HLLLHLL *F  AAA-A-A- ;LOAD OPN 5  (BACKSPACE) ESC D          211

*P 52 *I LLHLHL-HLLLHLH *F  ------AA ;CLEAR CURL (ESC E)                     205
*P 69 *I LLHHHL-HLLLHLH *F  ------A- ;CLEAR CURP (ESC E)                     206
*P 79 *I LHLLHL-HLLLHLH *F  AAA-AAAA ;LOAD OPN 0  (CLEAR-END OF SCREEN)ESC E 207

*P 71 *I LLHHHL-HLLHLLL *F  ------A- ;CLEAR CURP (HOME) ESC H                 224
*P 54 *I LLHLHL-HLLHLLL *F  ------AA ;CLEAR CURL (HOME) ESC H                 223

*P 78 *I LLHLHL-HLLHLHL *F  AAA-AAAA ;LOAD OPN 0  (CLEAR-END OF SCREEN)ESC J 203
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```
*P 51 *I LLHLHL=HLLHLHH *F AAA=AAA= ;LOAD OPN 1 (CLEAR=END OF LINE) ESC K     204

*P 75 *I LLHHHL=HLHHHLH *F -AAA---- ;PROTECT CLOCK (SET WRITE PROTECT          218

*P 74 *I LHLLHL=HLHHLHH *F -AAA---- ;PROTECT CLOCK (CLEAR WRITE PROTECT)      217

*P 44 *I LLHHHL=HLHLHHH *F -AAAA--- ;FORMAT CLOCK (FORMAT ON) ESC W

*P 95 *I LHLLHL=HLHHLLL *F -AAAA--- ;FORMAT CLOCK (CLEAR FORMAT) ESC X        216

*P 83 *I LHLLHL=HHLLLHL *F -AA-A--- ;KBD CONTROL CLOCK (ENABLE KBD)          220

*P 82 *I LLHHHL=HHLLLHH *F -AA-A--- ;KBD CONTROL CLOCK (DISABLE KBD)         219

*P 90 *I LLHHHL=HHLHHLL *F -AA----- ;BLINK CLOCK (SET WRITE BLINK)           221

*P 91 *I LHLLHL=HHLHHLH *F -AA----- ;BLINK CLOCK (CLEAR WRITE BLINK)         222

                                    ** LOAD CURSOR OPERATION **  ESC F
*P 59 *I LLHLHL=HLLLHHL *F AAAA-A-A ;LOAD SEQ 10 (LOAD CURSOR OPN) ESC F     212
*P 48 *I HLHLHL=HLLLHHL *F -----A-- ;CLEAR BUFFER (RECEIVER BUFFER) ESC F    226
*P 58 *I HLLHHL=LLLLLLL *F AAAA-A-- ;LOAD SEQ 11 (WAIT-CURSOR ADD BITE)      227
*P 4A *I HHLLHL-------- *F --A-AA-- ;LOAD CURL;CLEAR BUFFER                  228
*P 50 *I HHLHHL=LLLLLLL *F AAAA--A- ;LOAD SEQ 15 (WAIT-CURSOR ADD BITE)      229
*P 65 *I HHHLHL-------- *F ---A-A-- ;LOAD CURP CLEAR BUFFER                  230

                                    ** AUXILARY SEND ** ESC ZERO
*P 28 *I LLHLHL=LHHLLLL *F -----AA- ;ENABLE AUX SEND PORT                    302
*P 14 *I LLHHHL=LHHLLLL *F ----A-AA ;LOAD BCUR;CLEAR CURL                    303
*P 45 *I LHLLHL=LHHLLLL *F AAA----A ;LOAD OPN 14 (START SEND)                304

                                    ** PAGE SEND ** ESC I
**P 15 *I LLHLHL=HLLHLLH *F ----A-AA ;LOAD BCUR;CLEAR CURL                    305
*P 46 *I LLHHHL=HLLHLLH *F AAA----A ;LOAD OPN 14 (START SEND)                306

                                    ** LINE SEND ** ESC SMALL I
*P 17 *I LLHLHL=HHLHLLH *F ----AAAA ;LOAD BCUR;CLEAR BCURL                   307
*P 47 *I LLHHHL=HHLHLLH *F AAA----A ;LOAD OPN 14 (START SEND)                308

                                    ** DELETE CHARACTER **  ESC P
*P 54 *I LLHLHL=HLHLLLL *F -A----AA ;CLEAR REAG (REG2 TO NULL REG1 TO SPACE   402
*P 73 *I LLHHHL=HLHLLLL *F AAA--AA- ;LOAD OPN 9 (DELETE CHARACTER)            403

                                    ** FUNCTION KEY SEND ** ESC SMALL P TO DEL
*P 79 *I LLHLHL=HHH---- *F -A---AAA ;LOAD REG (LOAD FKEY CODE TO REG1)       420
*P 56 *I LLHHHL=HHH---- *F -------A ;WRITE (LC CODE UNDER CURSOR)            421
*P 59 *I LHLLHL=HHH---- *F AAAAA--A ;LOAD SEQ 0 (JUMP PASS SEQ 5)            422
*P 52 *I LHHLHL=HHH---- *F -A-AAAA4 ;START TIME;LOAD REG (LCCODE TO REG1)    423
*P 58 *I LHHHHL=HHH---- *F AA-A-AAA ;LOAD LIT ADDR 8 (1ST CODE FKEY)         424
*P 90 *I HLLLHL=HHH---- *F A-AAAAA- ;BUSS REG2                               425
*P 89 *I HLLHHL-------- *F AAA---AA ;LOAD OPN 12 (FUNCTION SEND)             426

*P 77 *I LHLHHL-------- *F AAAA---- ;LOAD SEQ 15 (END ESC DECODE)            225
                                    ESCAPE CODE NOT FOUND ABORT ESC BIT

                                    ** TERMINATE MODE 0 **
*P 44 *I HHHHHL-------- *F AAA-AA-A ;LOAD OPN 2 (FORWARD PROT TEST) GOTO M01 109
```

```
                        X
                       FM
              FMI     CRT       OUTPUT          MODE 1
          SEQ MOLOPN ROW         BITS
          43211DL4321YT2       87654321
                                          ** OPERATION 0 **
                                          ** CLEAR TO END OF SCREEN **
*P 12 *I LLLL-H-LLL---- *F -A----AA ;CLEAR REG, REG2-SPACE                111
*P 34 *I LLLH-H-LLL---- *F A-AA-AA- ;BUSS REG2,DISABLE REFRESH            112
*P 40 *I LLHL-H-LLL---- *F ----A--- ;LOAD BCUR (SAVE CURSOR LOCATION)     113
*P 15 *I LHLL-H-LLL--L- *F -------A ;WRITE (NULL TO MEM-EOS,EOL)          116
*P 29 *I LHLH-H-LLL---- *F --A----- ;INCR CURP                            117
*P 37 *I LHHL-HLLLL---- *F AAAAA-AA ;LOAD SEQ 4                           118
*P 19 *I LHHH-HHLLLL--- *F --AAA-A- ;INCR CURL,CLEAR CURP                 119
*P 38 *I HLLL-HLLLLL--- *F AAAAA-AA ;LOAD SEQ 4                           120
*P 27 *I HLLL-HHLLLL--- *F ------AA ;CLEAR CURL                           121
*P 22 *I HLLH-H-LLL---- *F ------A- ;CLEAR CURP                           122
*P 35 *I HLHL-H-LLL---- *F AAA--A-- ;LOAD OPN 11 (RETURN CURSOR)          123

                                          ** OPERATION 1 **
                                          ** CLEAR TO END OF LINE **
*P 12 *I LLLL-H-LLL---- *F -A----AA ;CLEAR REG, REG2-SPACE                111
*P 34 *I LLLH-H-LLL---- *F A-AA-AA- ;BUSS REG2,DISABLE REFRESH            112
*P 40 *I LLHL-H-LLL---- *F ----A--- ;LOAD BCUR (SAVE CURSOR LOCATION)     113
*P 17 *I LLHH-H-LLLH--- *F -----AAA ;CLEAR BCURL                          114
*P 10 *I LHLL-H-LLLH-H- *F AAAA-AA- ;LOAD SEQ 9 (STOP EOL AT PROT FIELD)  115
*P 15 *I LHLL-H-LLL--L- *F -------A ;WRITE (NULL TO MEM-EOS,EOL)          116
*P 29 *I LHLH-H-LLL---- *F --A----- ;INCR CURP                            117
*P 37 *I LHHL-HLLLL---- *F AAAAA-AA ;LOAD SEQ 4                           118
*P 22 *I HLLH-H-LLL---- *F ------A- ;CLEAR CURP                           122
*P 35 *I HLHL-H-LLL---- *F AAA--A-- ;LOAD OPN 11 (RETURN CURSOR)          123

                                          ** OPERATION 2 **
                                          ** FORWARD PROTECT TEST
*P 05 *I LLLL-H-LLHL-H- *F AAA-A-AA ;LOAD OPN 4 (ADVANCE IF PROTECTED)    124

                                          ** OPERATION 3 **
                                          ** BACKWARD PROTECT TEST **
*P 63 *I LLLL-H-LLHH-H- *F AAA-A-A- ;LOAD OPN 5  (BACKSPACE) BACKWARD PROT  238

                                          ** OPERATION 4 **
                                          ** ADVANCE **
*P 30 *I LLLL-H-LHLL--- *F --A----- ;INCR CURP                            125
*P 45 *I LLLH-HLLHLL--- *F AAA-AA-A ;LOAD OPN 2 (FORWARD PROT TEST)NOT EOL  126
*P 23 *I HLLH-HHLH-L--- *F ------A- ;CLEAR CURP                           127
*P 07 *I HLHL-H-LHLL--- *F AAA-A--A ;LOAD OPN 6 (DOWN, END OPN 4)         128

                                          ** OPERATION 5 **
                                          ** BACKSPACE **
*P 72 *I LLLL-H-LHLH--- *F ---AA--- ;DECR CURP                            231
*P 73 *I LLLH-HLLH-H--- *F AAA-AA-- ;LOAD OPN 3 (BACKWARD PROT TEST       233
*P 88 *I LLHH-HHLHLH--- *F -A----A- ;DECR CURP2 (MOVE TO CPC79-END OF LINE)  235
*P 94 *I LHLL-HHLHLH--- *F AAAAAA-- ;LOAD SEQ 3                           236
*P 85 *I LHHL-H-LHLH--- *F AAA-A--- ;LOAD OPN 7 (UP) BKSP WRAP            237
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                                        ** OPERATION 6 **
                                        ** LINE FEED **
*P 25 *I LLLL-M-LMML---- *F  --AAA---- ;INCR CURL                                  129
*P 28 *I LLMLMMLMML---- *F  -------AA ;CLEAR CURL                                  130
*P 00 *I LLMLLMMLMML---- *F  ----A-A- ;LOAD BCUR,CLEAR CURP (0 CURP=READY ROLL)131
*P 46 *I LMLL-MLLMML---- *F  AAA-AA-A ;LOAD OPN 2 (FORWARD PROT TEST)           132
*P 01 *I LMLL-MMLMML---- *F  --AA-AAA ;DECR CURL,CLEAR,BCURL (SAVE ONLY CURP)  133
*P 10 *I LMLM-M-LMML---- *F  -A------A ;INCREMENT ROLL COUNTER                  134
*P 15 *I LMML-M-LMML---- *F  -A----AA ;CLEAR REG, REG2=NULL,LF SCROLL          135
*P 18 *I LMMM-M-LMML---- *F  A-AAAAA- ;REG2 TO BUSS (NULL IN REG2 TO BUSS)     136
*P 24 *I MLLL-M-LMML---- *F  --A----A ;WRITE INCR CURP                          137
*P 11 *I MLLM-MLLMML---- *F  AAAA-AAA ;LOAD SEN 8 (WRITE AGAIN,NOT ILLEGAL     138
*P 25 *I MLLM-MMLM-L---- *F  ------A- ;CLEAR CURP                               127
*P 50 *I MLML-M-LMML---- *F  AAA--A-- ;LOAD OPN 11 (RETURN CURSOR)             140

                                        ** OPERATION 7 **
                                        ** UP **
*P 60 *I LLLL-M-LMMM---- *F  --AA---- ;DECR CURL                                  232
*P 73 *I LLLM-MLLM-M---- *F  AAA-AA-- ;LOAD OPN 5 (BACKWARD PROT TEST            233
*P 4F *I LLMM-MMLMMM---- *F  AAAAAAAA ;LOAD SEN 0 (MOVE CURSOR TO LINE 24)      234

                                        ** OPERATION 8 **
                                        ** INSERT CHARACTER **
*P 41 *I LLLL-M-MLL---- *F  A-AA-AA- ;BUSS REG2;DISABLE REFRESH                 404
*P 48 *I LLLM-M-MLL---- *F  ----AAAA ;LOAD BCUR;CLEAR BCURL                     405
*P 09 *I LLMM-M-MLL---- *F  --A----- ;INCR CURP (INS-DEL CHAR)                  407
*P 77 *I LMLL-MLMLL--L- *F  -A---AAA ;LOAD REG (LOAD REG1 FROM MEMORY)          408
*P 85 *I LMML-MLMLL--L- *F  -------A ;WRITE (BYTE IN REG2 TO MEMORY)            411
*P 02 *I MLLL-MLMLLL-L- *F  AAAAAA-- ;LOAD SEN 3                                412
*P 5C *I MLMM-M-MLL---- *F  ---,---A- ;CLEAR CURP                               416
*P 71 *I MMLL-M-MLLL---- *F  --A----- ;INCR CURP                                417
*P 72 *I MMML-M-MLL---- *F  AAA--A-- ;LOAD OPN 11 (RETURN CURSOR)              418

                                        ** OPERATION 9 **
                                        ** DELETE CHARACTER **
*P 41 *I LLLL-M-MLL---- *F  A-AA-AA- ;BUSS REG2;DISABLE REFRESH                 404
*P 48 *I LLLM-M-MLL---- *F  ----AAAA ;LOAD BCUR;CLEAR BCURL                     405
*P 58 *I LLML-M-MLLM---- *F  -------A ;WRITE (NULL CODE TO MEMORY)              406
*P 09 *I LLMM-M-MLL---- *F  --A----- ;INCR CURP (INS-DEL CHAR)                  407
*P 77 *I LMLL-MLMLL--L- *F  -A---AAA ;LOAD REG (LOAD REG1 FROM MEMORY)          408
*P 78 *I LMLM-MLMLLM-L- *F  -A---AAA ;LOAD REG (MOVE REG1 TO REG2)              409
*P 80 *I LMML-MLMLLL-L- *F  ---AA--- ;DECR CURP (DEL MOVE BACK ONE)             410
*P 85 *I LMML-MLMLL--L- *F  -------A ;WRITE (BYTE IN REG2 TO MEMORY)            411
*P 70 *I MLLL-MLMLLM-L- *F  --A----- ;INCR CURP (DEL CHAR)                      413
*P 55 *I MLLM-MLMLLL-L- *F  -A----AA ;CLEAR REG (REG2 TO NULL REG1 TO SPACE)    414
*P 7A *I MLML-MLMLLM-L- *F  AAAAAA-A ;LOAD SEN 2 (RETURN DEL AGAIN)             415
*P 52 *I MLMM-M-MLL---- *F  ------A- ;CLEAR CURP                                416
*P 72 *I MMML-M-MLL---- *F  AAA--A-- ;LOAD OPN 11 (RETURN CURSOR)              418

                                        ** OPERATION 10 **
                                        ** FORMAT TAB **
*P 70 *I LLLLLM-M-MLL--- *F  AAA-AA-A ;LOAD OPN 2 (FORMAT NOT ON NO TAB)        213
*P 81 *I LLLM-M-M-LM---- *F  A-AA-A-A ;BUSS MEMORY,DISABLE REFRESH             242
*P 50 *I LLMM-M-M-LM---- *F  --A----- ;INCR CURP                                239
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*P 60 *I LLHH-HLHLHL-L- *F AAAAAA-A ;LOAD SEQ 2  (LOOK FOR PROT FIELD)          240
*P 87 *I LHLL-HLHLHL-H- *F AAA-A-AA ;LOAD OPN 4 (ADVANCE) PROT FIELD FOUND     241
   20 *I LHHH-HHHLH---- *F --AAA-A- ;INCR CURL,CLEAR CURP                      147
 P 95 *I HLLL-HLHLHL--- *F AAAAAA-- ;LOAD SEQ 3  (TAB NOT EOP, KEEP LOOKING)  243
*P 55 *I HLLH-H-HLHL--- *F ------AA ;CLEAR CURL (EOP,MOVE TO TOP LINE)        244
*P 67 *I HLHL-H-HLHL--- *F AAA-AA-A ;LOAD OPN 2 (FORWARD PROT TEST) END FTAB  246

                                    ** OPERATION 11 **
                                    ** RETURN CURSOR **
*P 33 *I L-LL-H-HLHH--- *F -A---AA- ;DECR CURL                                141
*P 41 *I L-LH-H-HLHH--- *F -A---A-A ;DECR BCURP                               142
*P 47 *I LLHL-HHHLHH--- *F AAA-AA-A ;LOAD OPN 2 (FORWARD PROT TEST)CUR HOME   143
*P 20 *I LLHL-HLHLHH--- *F AAAAA---A ;LOAD SEQ6                               144
*P 33 *I L-LL-H-HLHH--- *F -A---AA- ;DECR CURL                                141
*P 41 *I L-LH-H-HLHH--- *F -A---A-A ;DECR BCURP                               142
*P 09 *I LHHL-HHHLHH--- *F AAA-AA-- ;LOAD OPN 3 (BACKWARD PROT TEST)          145
*P 31 *I LHHL-HLHLHH--- *F --A------ ;INCR CURP                               146
*P 20 *I LHHH-HHHLH---- *F --AAA-A- ;INCR CURL,CLEAR CURP                     147
*P 02 *I LHHH-HLHLHH--- *F AAAAA-A- ;LOAD SEQ 5                               108
*P 85 *I HLLL-HHHLHH--- *F ------AA ;CLEAR CURL                               444
*P 39 *I HLLH-H-HLHH--- *F AAAAA-AA ;LOAD SEQ 4                               139

                                    ** OPERATION 12 **
                                    ** FUNCTION KEY SEND **
*P 67 *I LLLL-H-HHLL--- *F -------A ;WRITE (SEND SAVED CODE BACK TO MEMORY)   427
*P 59 *I LLLH-H-HHLL--- *F A-AAAA-- ;BUSS LIT (BUSS 1ST FKEY CODE)           428
*P 75 *I LLHL-H-HHLLL-- *F AAAAAA-A ;LOAD SEQ 2 (WAIT FOR TIMEOUT)           429
*P 63 *I LLHH-H-HHLL--H *F AAAAAA-- ;LOAD SEQ 3 (WAIT FOR XMIT BZY)          430
*P 92 *I LLHH-H-HHLL--L *F -----A-A ;LOAD UART (SEND 1ST CODE FKEY)          431
   66 *I LHLH-H-HHLL--H *F AAAAA-A- ;LOAD SEQ 5  (WAIT FOR XMIT BZY)         432
   49 *I LHLH-H-HHLL--L *F AA-A-AA- ;LOAD LIT ADDR 9 (2ND CODE FKEY)         433
*P 93 *I LHHL-H-HHLL--- *F -----A-A ;LOAD UART (SEND 2ND CODE-FKEY)          434
*P 83 *I LHHH-H-HHLL--- *F -A-AAAAA ;START TIME LOAD REG (FCODE REG2)         435
*P 91 *I HLLL-H-HHLL--- *F A-AAAAA- ;BUSS REG2 (LC CODE TO BUSS              436
*P 57 *I HLLH-H-HHLL--H *F AAAA-AA- ;LOAD SEQ 9 (WAIT FOR XMIT BUZY)         437
*P 94 *I HLLH-H-HHLL--L *F -----A-A ;LOAD UART (SEND LC CODE-FKEY)           438
*P 48 *I HLHL-H-HHLL--- *F AA-A-A-A ;LOAD LIT ADDR 10 (LAST CODE FKEY)       439
*P 60 *I HLHH-H-HHLL--- *F A-AAAA-- ;BUS  LIT (BUSS LAST FKEY CODE)          440
*P 65 *I HHLL-H-HHLL--H *F AAAA--AA ;LOAD SEQ 12 (WAIT FOR XMIT BZY)         441
*P 95 *I HHLL-H-HHLL--L *F -----A-A ;LOAD UART (SEND LAST CODE-FKEY)         442
*P 56 *I HHLH-H-HHLLL-- *F AAAA--A- ;LOAD SEQ 13 (WAIT FOR TIMER)            443

                                    ** OPERATION 13 **
                                    ** SEND ROUTINE **
*P 10 *I LLLL-H-HHLH--- *F A-AAAA-A ;BUSS MEMORY                             332
*P 29 *I LLLH-H-HHLH-L- *F AAAAA-A- ;LOAD SEQ 5 (JUMP BYTE NOT PROTECTED)    333
*P 35 *I LLHL-HLHHLH-H- *F -A---A-A ;DECR BCURP (MOVE PAST PROTECT)          334
*P 42 *I LLHH-HLHHLH-H- *F --A------ ;INCR CURP                              335
*P 37 *I LHLL-HHHHLH--- *F AAA------ ;LOAD OPN 15 (SEND DELIMITERS)          336
*P 04 *I LHLL-HLHHLH-H- *F AAAAAA-A ;LOAD SEQ 2 (STILL PROTECTED)            337
*P 30 *I LHLH-HLHHLH-LH *F AAAAA-A- ;LOAD SEQ 5 (WAIT FOR XMIT BZY)          338
*P 23 *I LHHL-H-HHLH--- *F -----A-A ;LOAD UART (WITH TEXT CHARACTERS)        339
*P 36 *I LHHH-H-HHLH--- *F -A---A-A ;DECR BCURP (COUNT CHAR FOR STOP POS)    340
*P 58 *I HLLL-HHHHLH--- *F AAA------ ;LOAD OPN 15 (SEND DELIMITERS)          341
*P 43 *I HLLH-H-HHLH--- *F --A------ ;INCR CURP                              342
*P 31 *I HLHL-HLHHLH-L- *F AAAAA-A- ;LOAD SEQ 5 (CHARACTER OK-SEND)          343
   39 *I HLHH-H-HHLH--- *F AAA------ ;LOAD OPN 15 (SEND DELIMITERS)          344
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                                        ** OPERATION 14 **
                                        ** START SEND ROUTINE  **
*P 18 *I LLLL-H-HHH---- *F. A-AAAA-- ;BUSS LIT (LITTERAL FROM TO BUSS)          309
*P 06 *I LLLH-H-HHHL--- *F -A-AA--- ;START TIME (BEGIN 240MS DELAY)            310
*P 03 *I LLHL-H-HHHLL-- *F AAAAAA-A ;LOAD SEQ 2 (WAIT ON TIMEOUT)              311
*P 11 *I LLHH-H-HHHL--- *F AA-AAAAA ;LOAD LIT ADDR 0 (HEADER STX)              312
*P 19 *I LHLL-H-HHH---H *F AAAAA-AA ;LOAD SEQ 4 (WAIT FOR XMIT BZY)            316
*P 21 *I LHLL-H-HHH---L *F -----A-A ;LOAD UART (WITH BYTE1 HEADER-STX)         317
*P 41 *I LHHL-H-HHHL--- *F AA-AAAA- ;LOAD LIT ADDR 1 (HEADER NULL)            318
*P 09 *I LHHH-H-HHH---H *F AAAAA--- ;LOAD SEQ 7                               322
*P 22 *I LHHH-H-HHH---L *F -----A-A ;LOAD UART (WITH BYTE2 HEADER-NUL)         323
*P 40 *I HLLL-H-HHHL--- *F -------A- ;CLEAR CURP                              329
*P 26 *I HLLH-H-HHHL--- *F -A---AA- ;DECR BCURL                               330
*P 10 *I HHHL-H-HHH---- *F AAA---A- ;LOAD OPN 13                              331

                                        ** OPERATION 15 **
                                        ** SEND DELIMITERS **
*P 18 *I LLLL-H-HHH---- *F A-AAAA-- ;BUSS LIT (LITTERAL FROM TO BUSS)          309
*P 20 *I LLHH-HLHHHH-H- *F AA-AAA-A ;LOAD LIT ADDR 2 (BYTE1 EOF UNPROTECT)    313
*P 34 *I LLHH-HHHHHH--- *F AA-AA-AA ;LOAD LIT ADDR 4 (BYTE1 EOL               314
*P 25 *I LLHH-HLHHHH-L- *F AA-AA--A ;LOAD LIT ADDR 6 (BYTE1 EOM)              315
*P 19 *I LHLL-H-HHH---H *F AAAAA-AA ;LOAD SEQ 4 (WAIT FOR XMIT BZY)           316
*P 21 *I LHLL-H-HHH---L *F -----A-A ;LOAD UART (WITH BYTE1 HEADER-STX)        317
*P 33 *I LHHL-HLHHHH-H- *F AA-AAA-- ;LOAD LIT ADDR 3 (BYTE2 EOF UNPROTECTED) 319
*P 01 *I LHHL-HHHHH---- *F AA-AA-A- ;LOAD LIT ADDR 5 (BYTE2 EOL)              320
*P 00 *I LHHL-HLHHHH-L- *F AA-AA--- ;LOAD LIT ADDR 7 (BYTE2 EOM)              321
*P 09 *I LHHH-H-HHH---H *F AAAAA--- ;LOAD SEQ 7                               322
*P 22 *I LHHH-H-HHH---L *F -----A-A ;LOAD UART (WITH BYTE2 HEADER-NUL)        323
*P 07 *I HLLL-HLHHHH-L- *F -A-AA--- ;START TIME (BEGIN 240MS DELAY)           324
*P 02 *I HLLH-HLHHHHLL- *F AAAA-AA- ;LOAD SEQ 9 (WAIT ON TIMEOUT)            325
*P 32 *I HLHL-HLHHHHHL- *F A------- ;GOTO 0 (RTN TO IDLE AFTER TIMEOUT)      326
*P 27 *I HLHL-HHHHHH--- *F -A---AA- ;DECR BCURL                               327
*P 08 *I HLHH-HHHHHH---- *F --AAA-A- ;INCR CURL:CLEAR CURP                    328
*P 10 *I HHHL-H-HHH---- *F AAA---A- ;LOAD OPN 13                              331

                                        ** TERMINATE MODE 1 **
*P 52 *I HHHH-H-------- *F A------- ;GO TO MODE 0                              110
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