CONTROL DATA®
DISK STORAGE UNIT

BR2A5

DIAGRAMS
MAINTENANCE AIDS
WIRE LISTS

CONTROL DATA
CORPORATION

CUSTOMER ENGINEERING MANUAL

REVISION RECORD (CONT'D)

REVISION	DESCRIPTION
J	Incorporates Engineering Change Orders PE29573, PE29907, PE29967, and Field Change Order PE29573
(4-4-72)	affecting pages ii.i, iii, iv, viii, ix, x, 5-26, 5-36, 5-42.1, 5-86, 5-94, 7-78, 7-79, 7-80, 7-81,
	7-82, 7-83, 7-84, 7-85, 7-86, 7-88, 7-89, 9-7, 9-16, 9-23.
K	Incorporates Field Change Order PE29923 affecting pages ii.i, iii, iv, 9-42.
(4-12-72)	
L	Incorporates Engineering Change Orders PE29921, PE29922, PE31007, and Field Change Order PE29922
(6-2-72)	affecting pages ii.i, iii, iv, viii, 5-23, 5-28.1, 5-34, 5-35, 5-36, 5-101, 5-102, 9-6, 9-36, 9-37,
	9-38, 9-39, 9-40, 9-41, 9-42, 9-43.
M	Incorporates Engineering Change Orders PE31014, PE31047, PE31081 affecting pages ii.i, iii, iv, ix,
(6-30-72)	5-29, 5-42.3, 9-48, 9-49, 9-50, 9-51, 9-52, 9-53, 9-54, 9-55, 9-56.
N	Incorporates Engineering Change Orders PE31133, PE31138, PE31160, PE31164, PE31272, PE31317, and
(2-10-73)	Technical Corrections affecting pages ii.i, iii, iv, ix, 5-34, 5-35, 9-23, 9-24, 9-27, 9-31,
	9-56, 9-57.
P	Incorporates Engineering Change Orders PE31344, PE31389, PE31421 affecting pages ii.i, iii, iv,
(7-17-73)	vii, 5-21, 5-26, 5-42.1, 5-42.3, 5-42.4, 5-42.5, 5-42.6, 9-11, 9-27, 9-51, 9-52, 9-53, 9-54.
R	Incorporates Engineering Change Orders PE31344C, PE31472 and Field Change Order PE31472 affecting
(8-17-73)	pages ii.i, iii, iv, vii, 5-28.1, 5-36, 5-42.5, 5-52, 5-53, 5-54, 9-52.
S	Incorporates Engineering Change Order PE31401 affecting pages ii.i, iii, iv, iv.i, viii, 5-35, 5-36,
(10-19-73)	5-103, 5-104, 5-105.
T	Incorporates Engineering Change Orders PE31497, PE31499A, PE31512, PE31561, and Field Change Order
(12-10-73)	PE31519 affecting pages ii.i, iii, iv, iv.i, 5-16, 5-21, 5-23, 5-27, 5-28.1, 5-29, 5-30.1, 5-37,
	5-38, 5-38.1, 5-42.1, 5-42.4, 5-42.5, 7-86.
U	Incorporates Engineering Change Order/Field Change Order PE31494 and Technical Corrections affecting
(2-28-74)	pages ii.i, iii, iv, iv.i, vii, ix, 5-40, 5-42, 5-42.1, 5-42.4, 5-106, 5-107, 9-58.
V	Incorporates Engineering Change Orders PE31656, PE31691 affecting pages ii.i, iii, iv, iv.i, vii,
(5-17-74)	ix, 5-36, 5-52, 5-53, 5-54, 9-54, 9-58.
W	Incorporates Engineering Change Order PE31739 affecting pages: ii.i, iii, 5-29, 5-30, 5-30.1,
(8-16-74)	5-35, 5-37, 5-42.3. iv.i
Publication No. 70614700	

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5-85	A
5-86	J
5-87	A
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PREFACE

Customer engineering material for the CONTROL DATA® BR2A5 Disk Storage Unit is contained in three separate manuals, which provide all information needed to install, operate, and maintain the unit:

Publication No. 70614600	General Description, Operation, Installation and Checkout, Theory of Operation, Maintenance
Publication No. 70614700	Diagrams, Maintenance Aids, Wire Lists
Publication No. 70614800	Illustrated Parts List

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Information for these sections is included in BR2A5 Disk Storage Unit, Pub. No. 70614600.

SECTION 1

GENERAL DESCRIPTION

SECTION 2

OPERATION

SECTION 3

INSTALLATION AND CHECKOUT

SECTION 4

THEORY OF OPERATION

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DIAGRAMS

DIAGRAMS

INTRODUCTION

This section contains diagrams that logically describe the DSU in terms of the functions which the unit performs. Figures 5-1 through 5-12 are flow charts, simplified circuits, and timing diagrams that describe the First Seek function, the Power Off sequence, the Direct Seek (forward and reverse) function, the Return to Zero function, the Read/Write operations, and Head Advance timing. The logic diagrams for the unit are provided on pages 5-14 through 5-36. The DSU signal distribution drawing is located on page 5-37. Panel (operator and maintenance) schematics are on pages 5-38 and 5-39. The unit power supply schematic for mods 01 through 06 is located on pages 5-41 and 5-42, and for mods 07 and above is located on pages 5-42.1 and 5-42.2. Schematic diagrams for the logic cards are found at the end of the section.

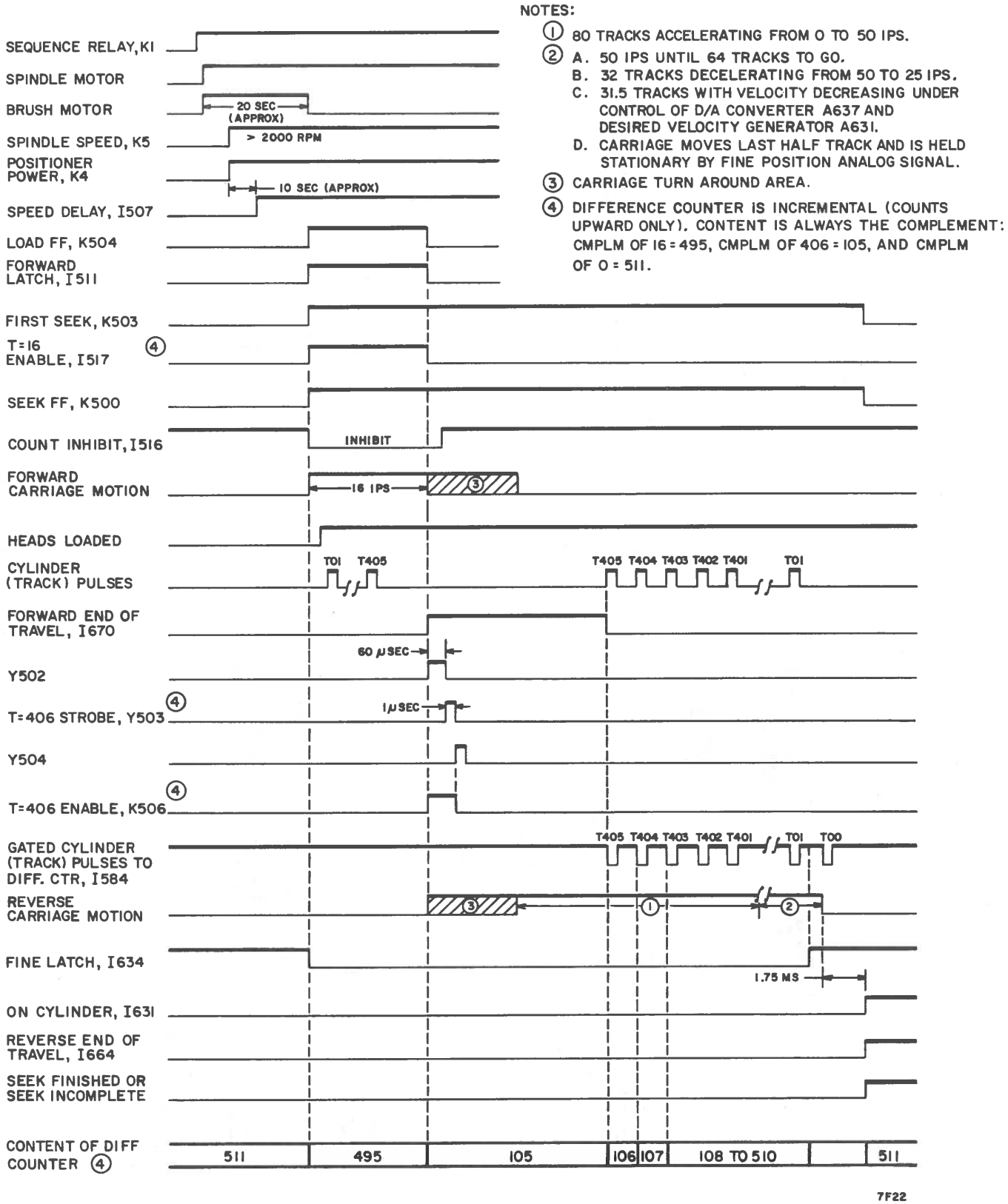


Figure 5-2. Power On/First Seek Timing

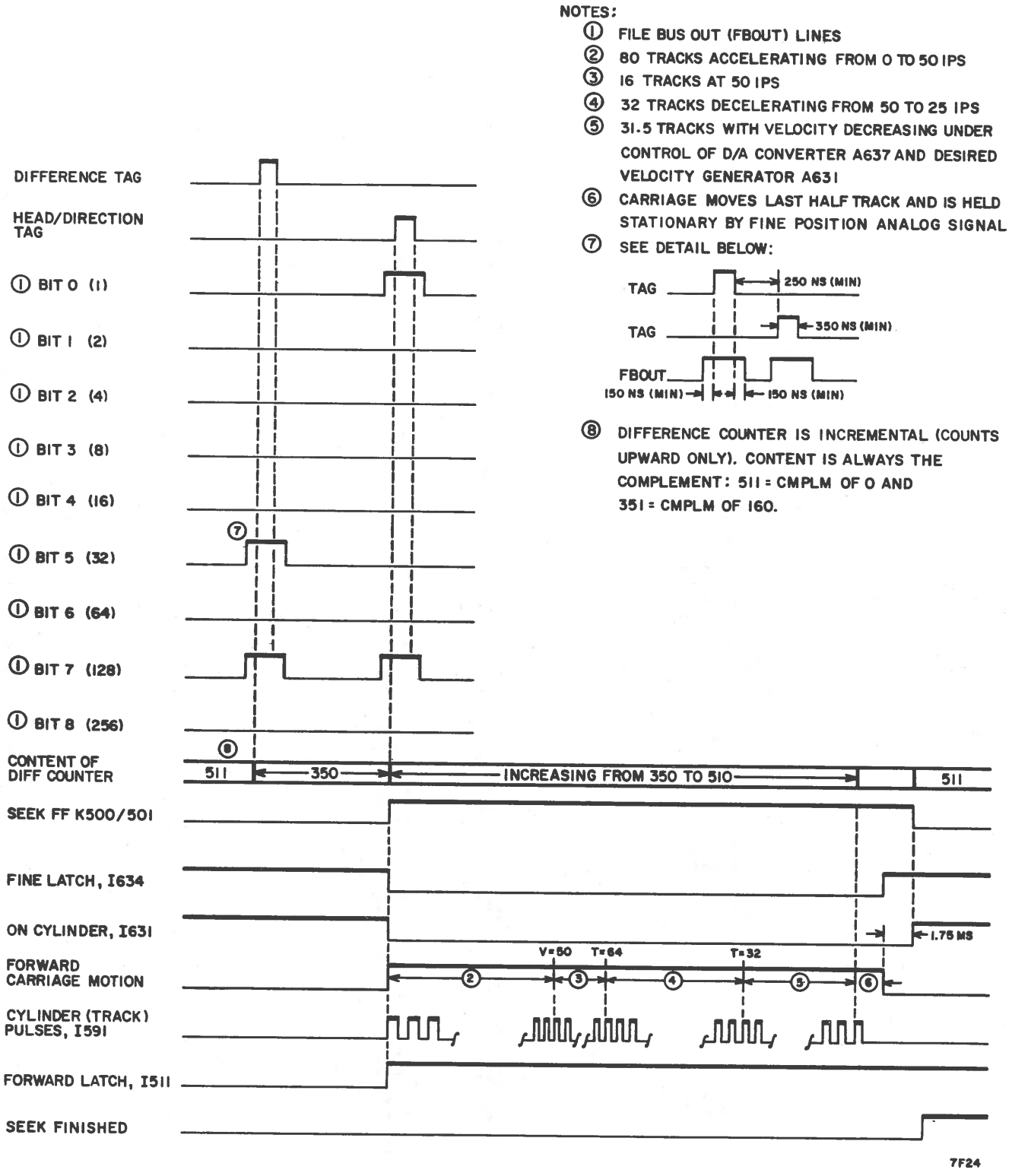
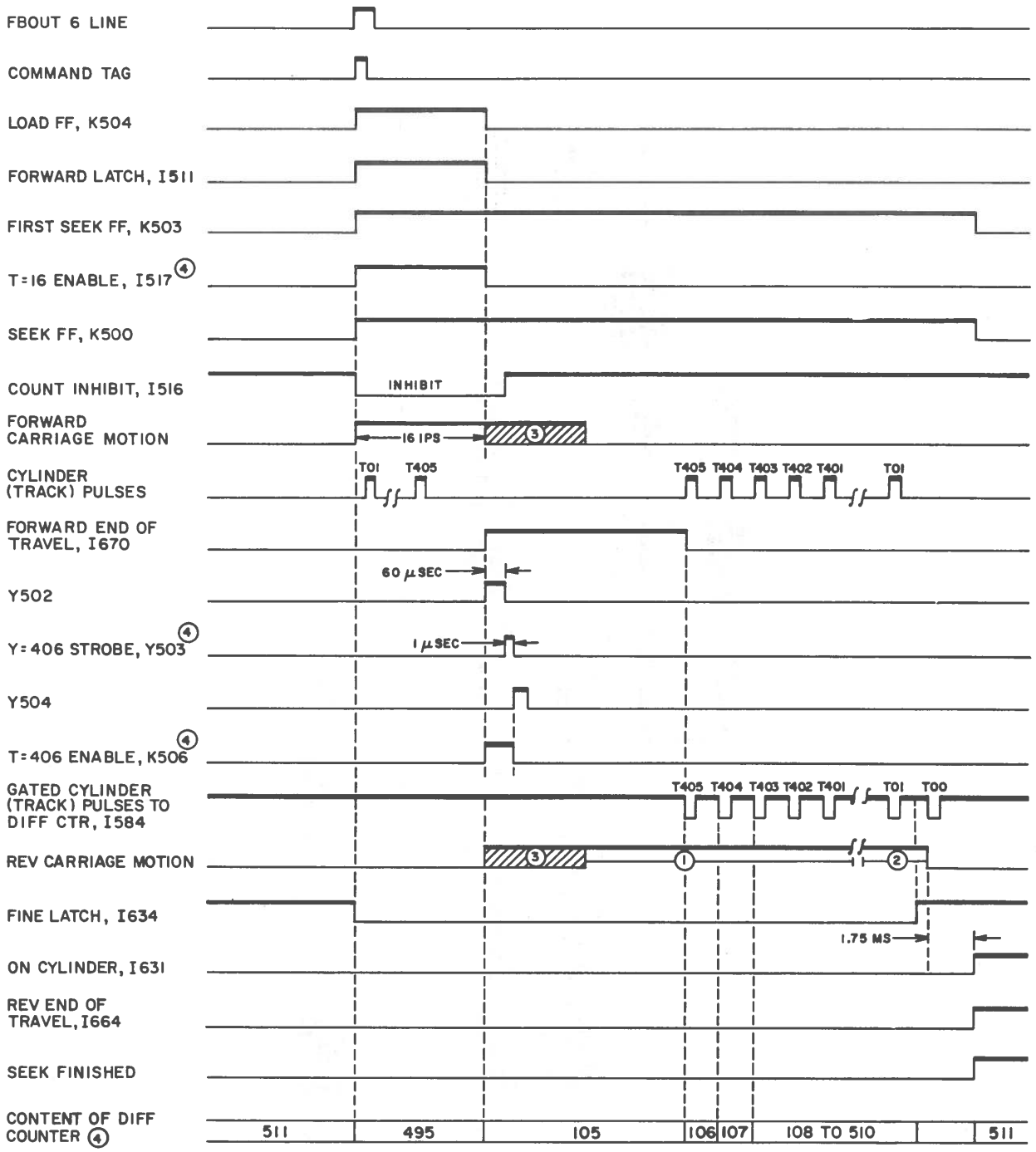


Figure 5-4. Direct Seek Timing



NOTES:

① 80 TRACKS ACCELERATING FROM 0 TO 50 IPS.

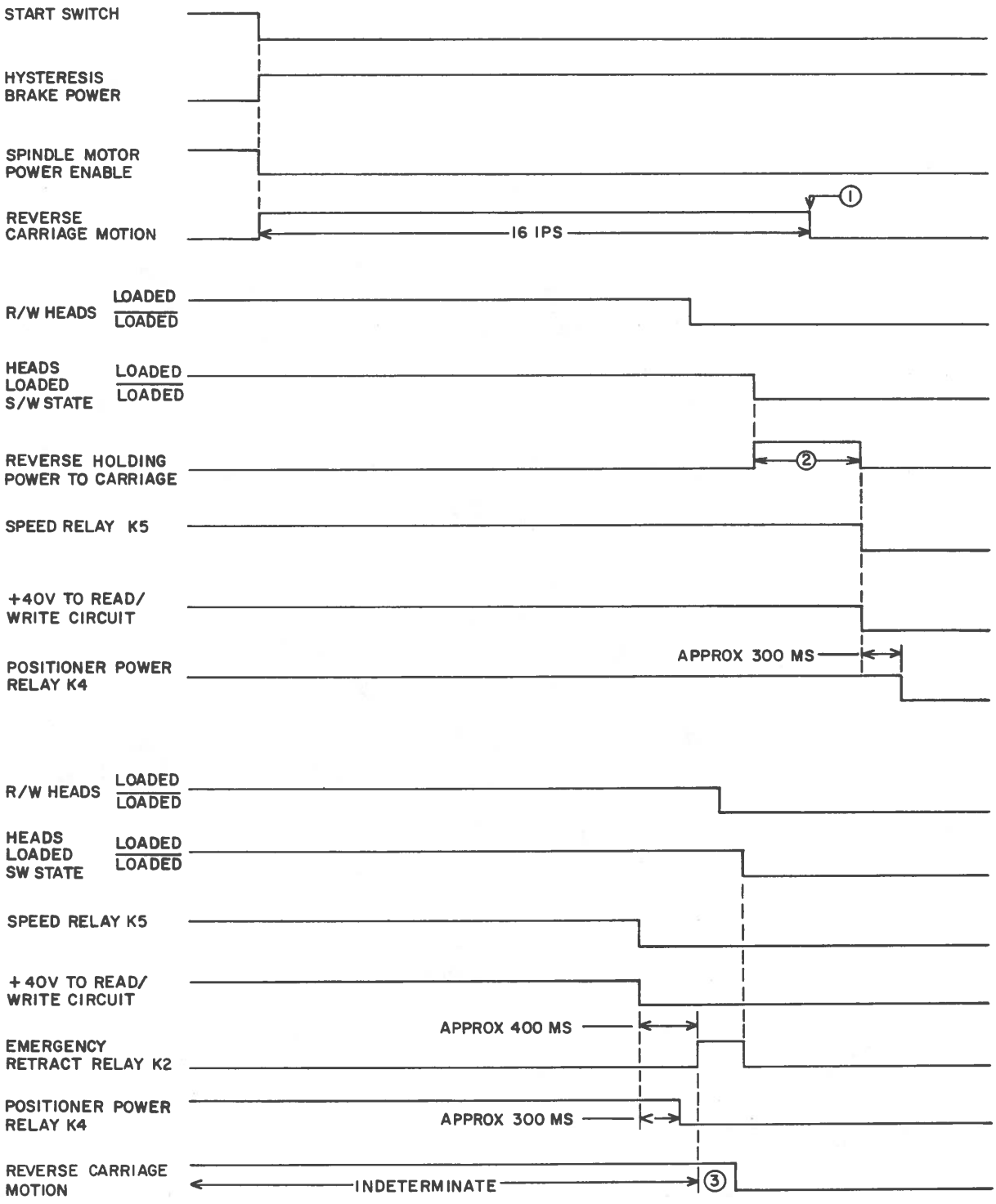
② A. 50 IPS UNTIL 64 TRACKS TO GO.
B. 32 TRACKS DECELERATING FROM 50 TO 25 IPS.
C. 31.5 TRACKS WITH VELOCITY DECREASING UNDER CONTROL OF D/A CONVERTER A637 AND DESIRED VELOCITY GENERATOR A631.
D. CARRIAGE MOVES LAST HALF TRACK AND IS HELD STATIONARY BY FINE POSITION ANALOG SIGNAL.

③ CARRIAGE TURN AROUND AREA.

④ DIFFERENCE COUNTER IS INCREMENTAL (COUNTS UPWARD ONLY). CONTENT IS ALWAYS THE COMPLEMENT:
COMPLEMENT OF 16 = 495
COMPLEMENT OF 406 = 105
COMPLEMENT OF 0 = 511

7F26

Figure 5-6. Return to Zero Seek Timing



NOTES:

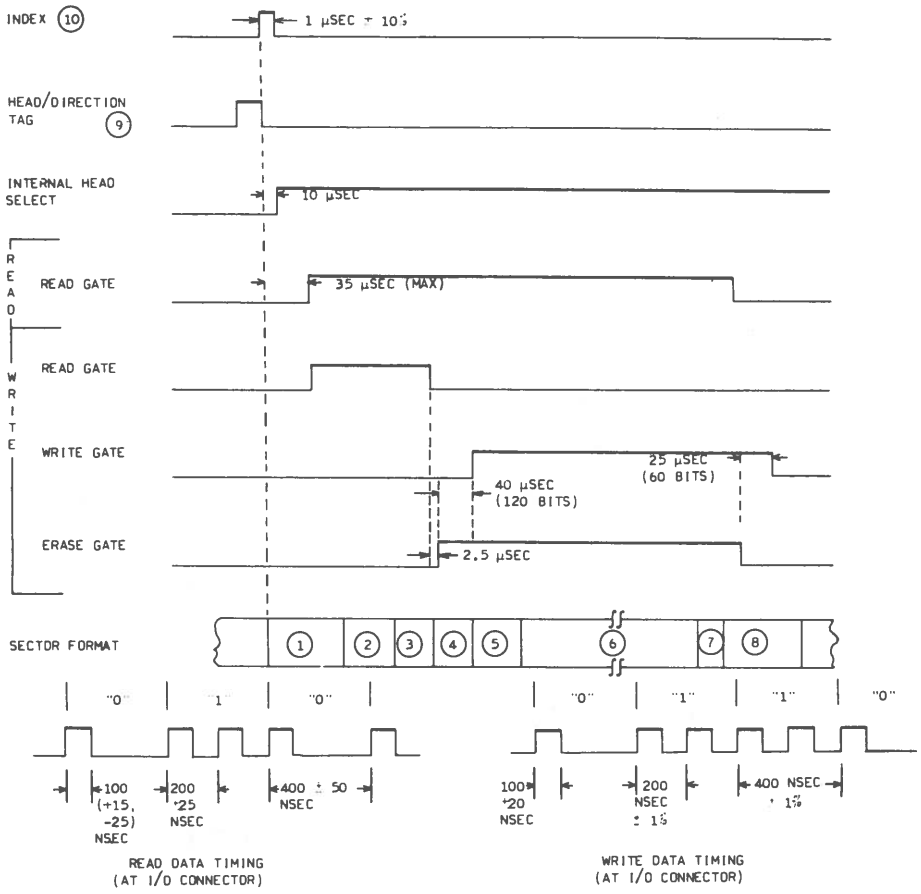
① CARRIAGE ENCOUNTERS RETRACTED STOP.

② ONE AMP (APPROX) OF HOLDING CURRENT APPLIED TO POSITIONER UNTIL K5 DROPS.

③ CARRIAGE MOVES TO RETRACTED STOP AT 60 IPS.

6T50

Figure 5-8. Power Off Timing



NOTES:

(1) TOLERANCE GAP 1 - 120 BITS - ACCOMODATES PHYSICAL READ/WRITE TO ERASE GAP DISTANCE AND ALLOWS HEAD SWITCHING AND READ AMPLIFIER STABILIZATION TIME.

(2) SYNC PATTERN 1 - 112 BITS - INDICATES BEGINNING OF ADDRESS AREA. CONTROLLER MUST INITIATE SYNC BYTE (OR BIT) SEARCH MIDWAY THROUGH THIS PATTERN (REQUIRED TO INSURE THAT HEAD IS READING A KNOWN PATTERN EVEN UNDER WORST-CASE CONDITIONS OF HEAD SKEW, RPM, AND INDEX TOLERANCES DUE TO DISK PACK INTERCHANGE).

(3) ADDRESS - 36 BITS (TYPICAL) - TWELVE-BIT UPPER ADDRESS, 12-BIT LOWER ADDRESS, AND 12-BIT CHECKWORD.

(4) HEAD GAP - 100 BITS (MIN) - ACCOMODATES PHYSICAL READ/WRITE TO ERASE GAP DISTANCE.

(5) SYNC PATTERN 2 - 112 BITS (MINIMUM) - INDICATES BEGINNING OF DATA FIELD.

(6) DATA FIELD - LENGTH DEPENDS UPON DATA RECORD FORMAT.

(7) POST AMBLE - 1 BIT - A PAD TO ENSURE THAT LAST BIT OF DATA IS NOT DESTROYED OR DISTORTED.

(8) TOLERANCE GAP 2 - LENGTH DEPENDS UPON FORMAT (SHOULD EQUAL APPROXIMATELY 2.5% OF SECTOR BIT CAPACITY). COMPENSATES FOR WORST-CASE CONDITIONS OF SPINDLE SPEED AND OSCILLATOR TOLERANCES.

(9) HEAD/DIRECTION TAG LINE SHOWN OCCURRING AT LATEST ACCEPTABLE TIME RELATIVE TO INDEX: NOT TO BE CONSIDERED A TYPICAL RELATIONSHIP.

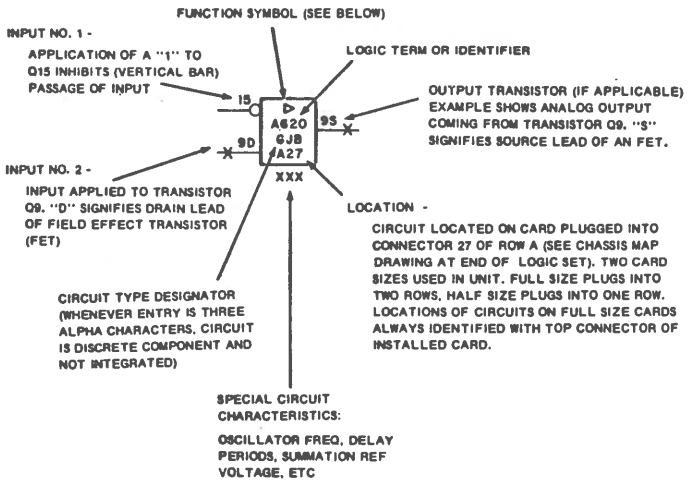
(10) INDEX PULSE AVAILABLE TO CONTROLLER TO INDICATE BEGINNING OF TRACK OR CYLINDER.

7F14

Figure 5-10. Read/Write Timing and Format

DISCRETE COMPONENT

DISCRETE COMPONENT CIRCUIT INFORMATION EXAMPLE:

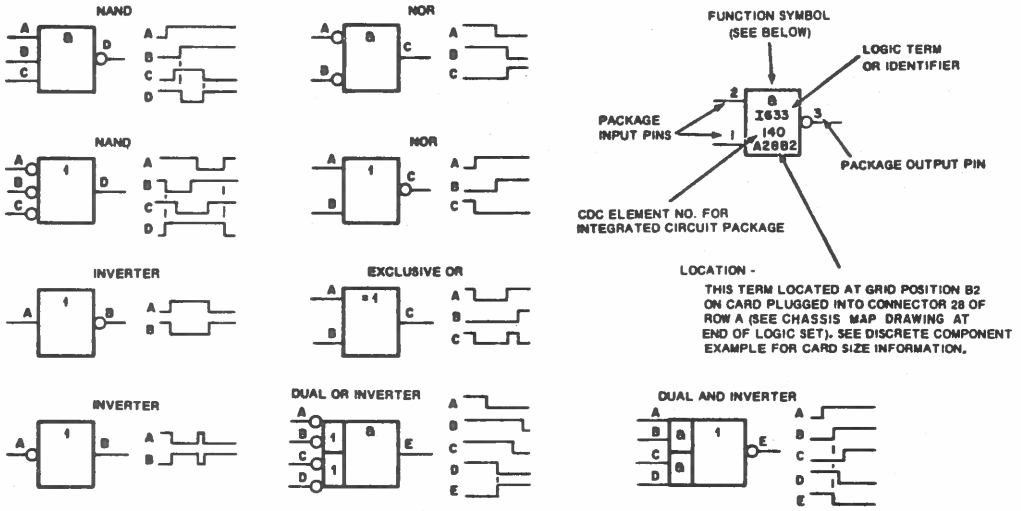


FUNCTION SYMBOLS:

▷	AMPLIFIER	Σx/▷	ANALOG SUMMATION OF DIGITAL INPUTS (REF VOLTAGE OUTSIDE OF BOX INDICATES OUTPUT SIGNAL LEVEL RESULTING WHEN SPECIFIED INPUT(S) ARE NEGATED)
x/▷	DIGITAL TO ANALOG CONVERSION	x/y	LEVEL CONVERSION - TRANSMISSION LINE TO LOGIC LEVEL, SWITCH STATE (GROUND OR OPEN) TO LOGIC LEVEL, LOGIC LEVEL TO POWER OUTPUT (TO DRIVE LAMP, RELAY, SOLENOID, ETC)
x/▷	DIGITAL TO ANALOG CONVERSION WITH ADJUSTABLE (ELECTRICALLY) GAIN	200NS ↑2	DELAY - WHEN INPUT CHANGES TO A "1", A 200 NSEC DELAY OCCURS BEFORE THE "1" IS PASSED ON.
G	OSCILLATOR (FREQ NOTED OUTSIDE OF BOX)	&	AND GATE OR INVERTER
∫▷•▷	DEMODULATOR	1	OR GATE OR INVERTER
F▷	FUNCTION GENERATOR	▷/Y	ANALOG TO DIGITAL CONVERTER
>28.5 HZ	FREQUENCY SENSOR	▷/Y	ADJUSTABLE ANALOG TO DIGITAL CONVERTER
∫▷-▷/Y	ABSOLUTE DIFFERENCE SENSOR (VOLTAGE VALUE OF DIFFERENCE INDICATED OUTSIDE OF BOX) WITH DIGITAL CONVERSION	1 ⎍	SINGLE SHOT
		1 ⎍	ADJUSTABLE SINGLE SHOT
> 1	SINGLE LINE MULTIPLE SELECT DETECTOR (EXCESSIVE VOLTAGE DROP OCCURS AT INPUT IF MORE THAN ONE SELECTION IS MADE)	x/▷/▷/Y	ADJUSTABLE RINGING AMPLIFIER (DESIRED RESONANT FREQ SPECIFIED ADJACENT TO BOX)
		∫x⊐Y	SWITCH RECEIVER

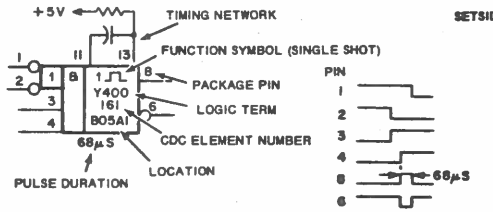
INTEGRATED

INTEGRATED CIRCUIT (GATES) INFORMATION EXAMPLE:

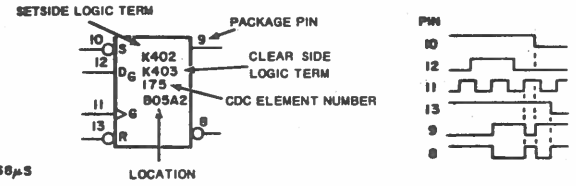


INTEGRATED CIRCUIT (FF, COUNTER, TRANSMITTER, SINGLE SHOT) INFORMATION EXAMPLE:

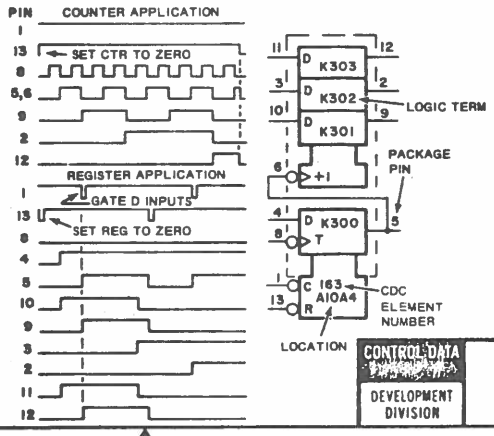
RETRIGGERABLE MULTIVIBRATOR (SINGLE SHOT)



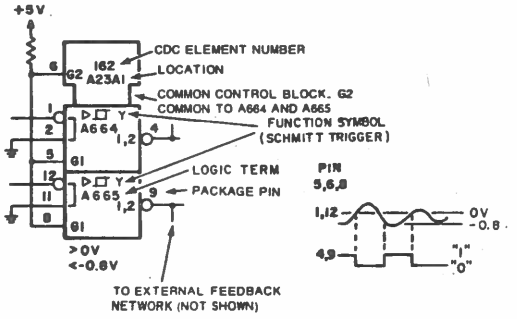
FLIP-FLOP (TYPE D)



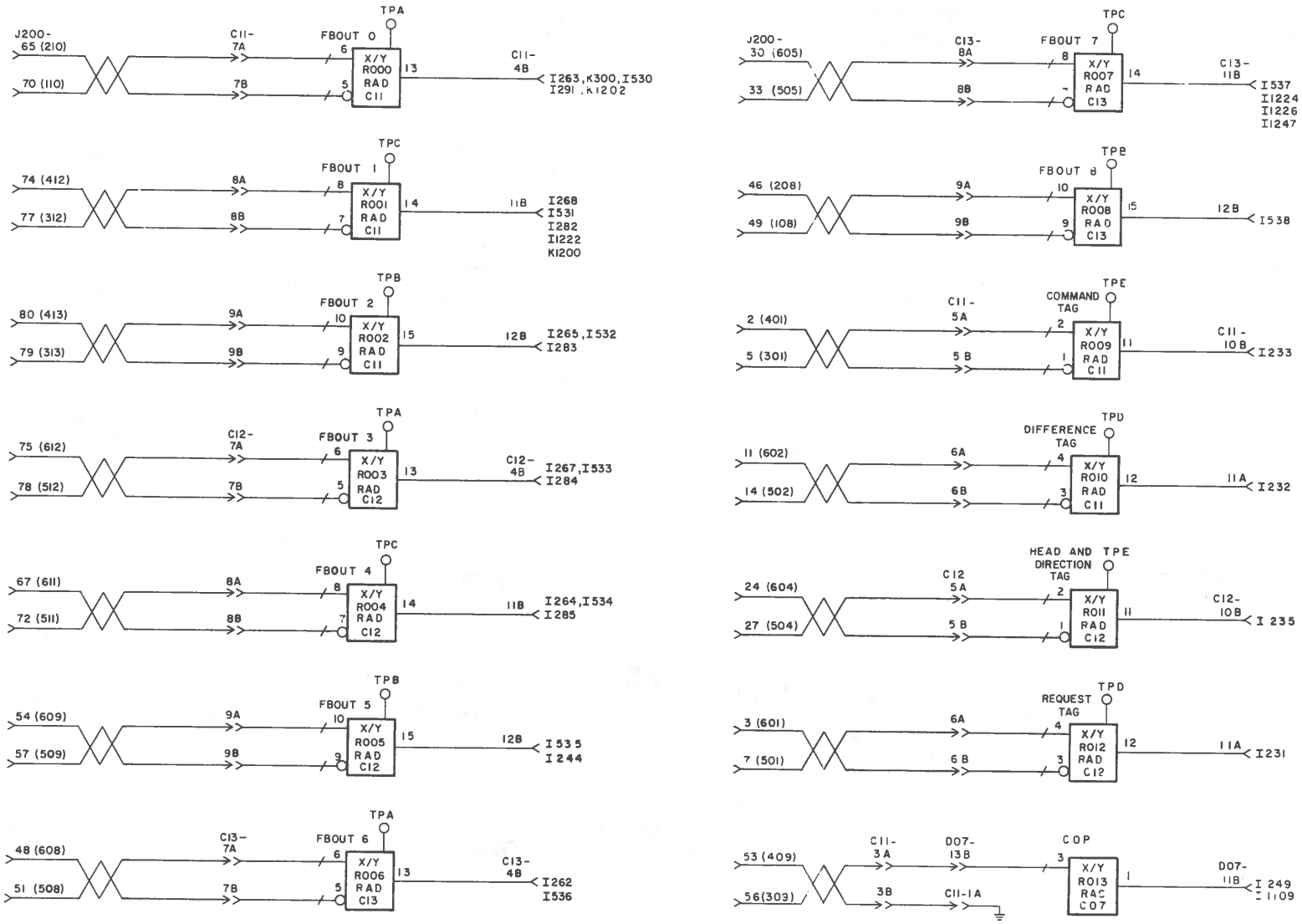
4-BIT COUNTER/STORAGE ELEMENT



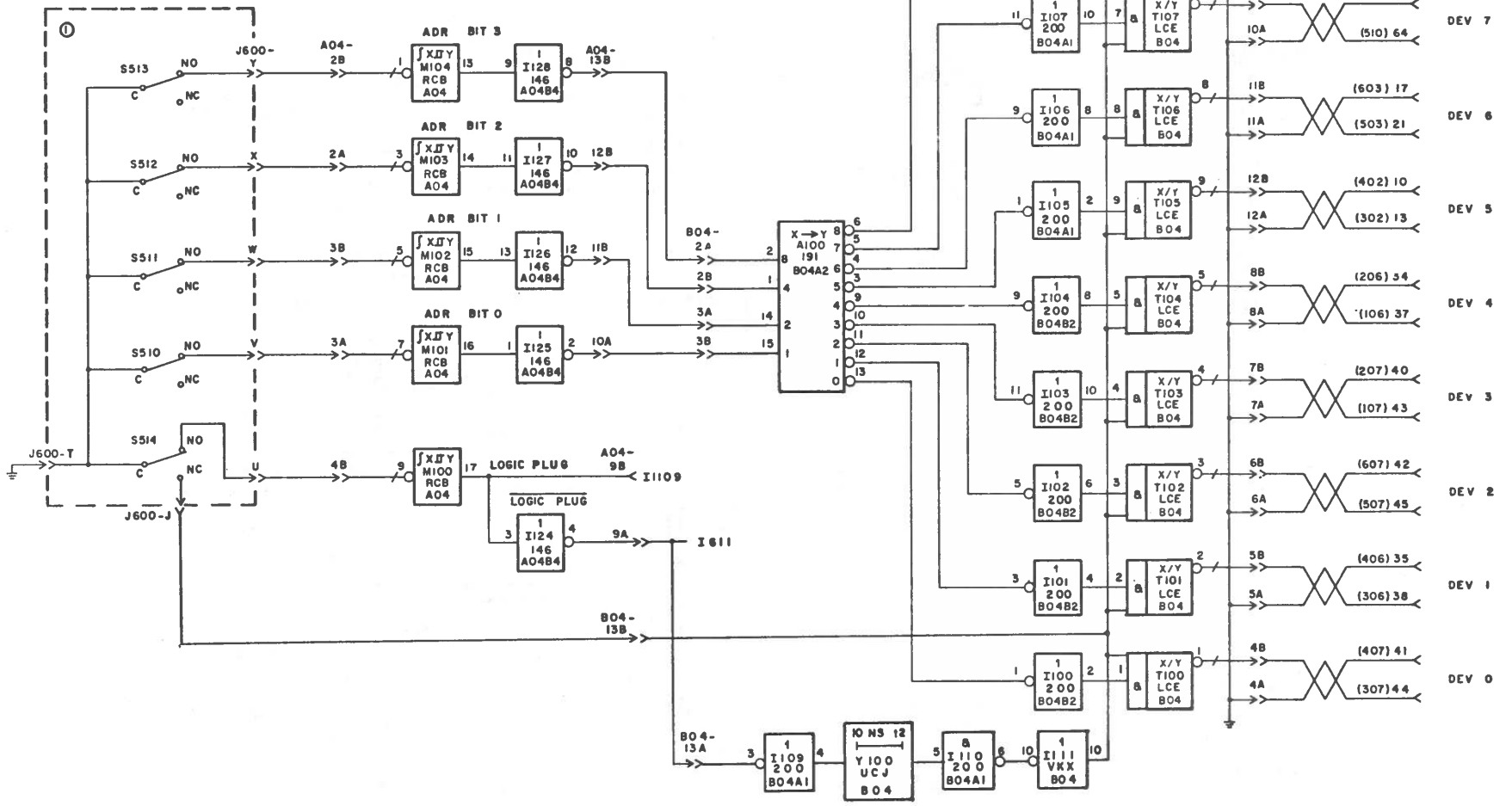
DUAL DIFFERENTIAL RCVR USED AS SCHMITT TRIGGER



CONTROL DATA DEVELOPMENT DIVISION	KEY TO LOGIC SYMBOLS PART I	CODE IDENT 19333	DWG NO VCD-7367	REV A
		C	SHEET 1	PAGE



CONTROL DATA	RECEIVERS	CODE IDENT	DWG NO	DIV
DEVELOPMENT DIVISION		19333	VCD-7367	E
		C	SHEET 3	PAGE

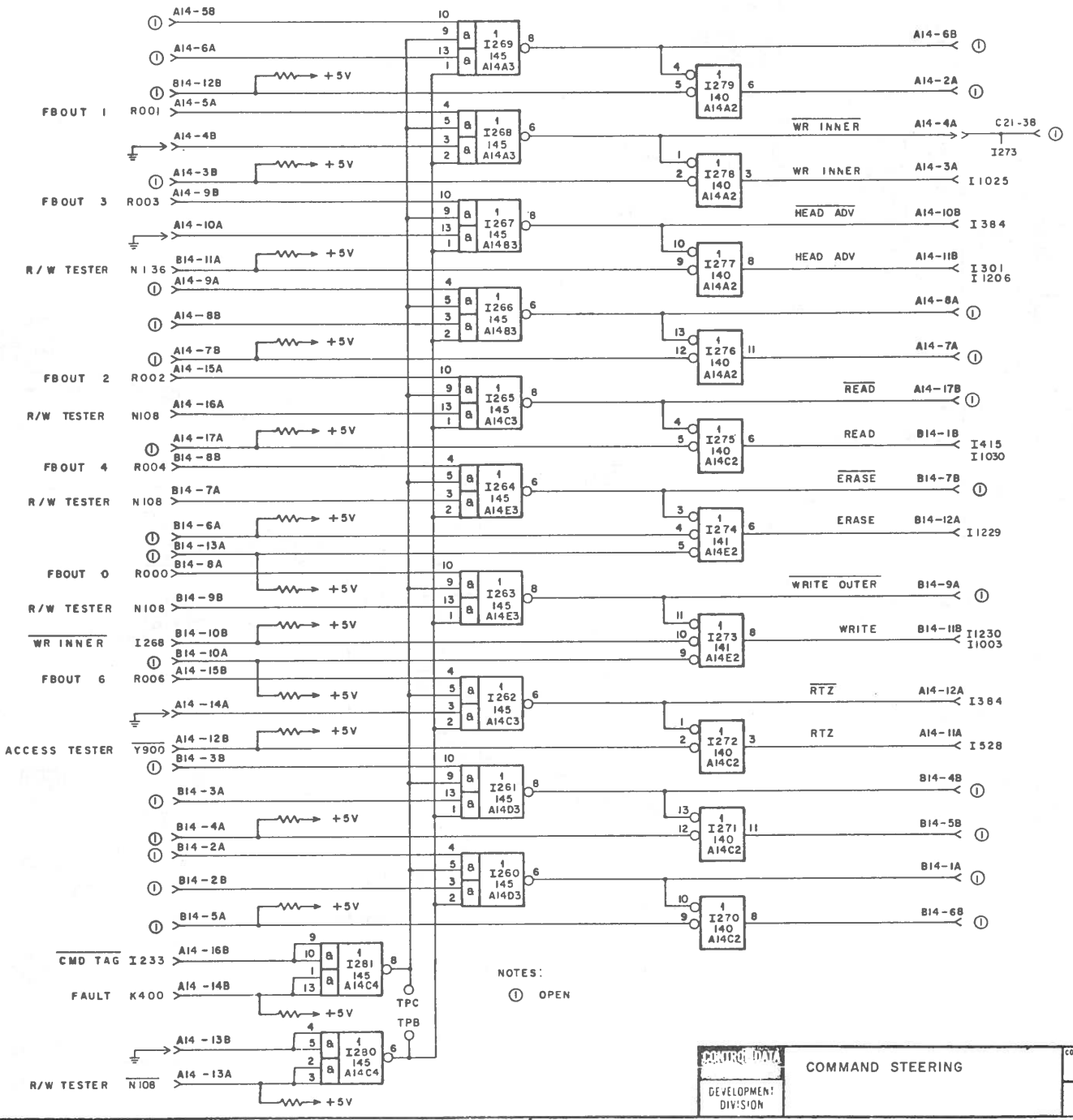


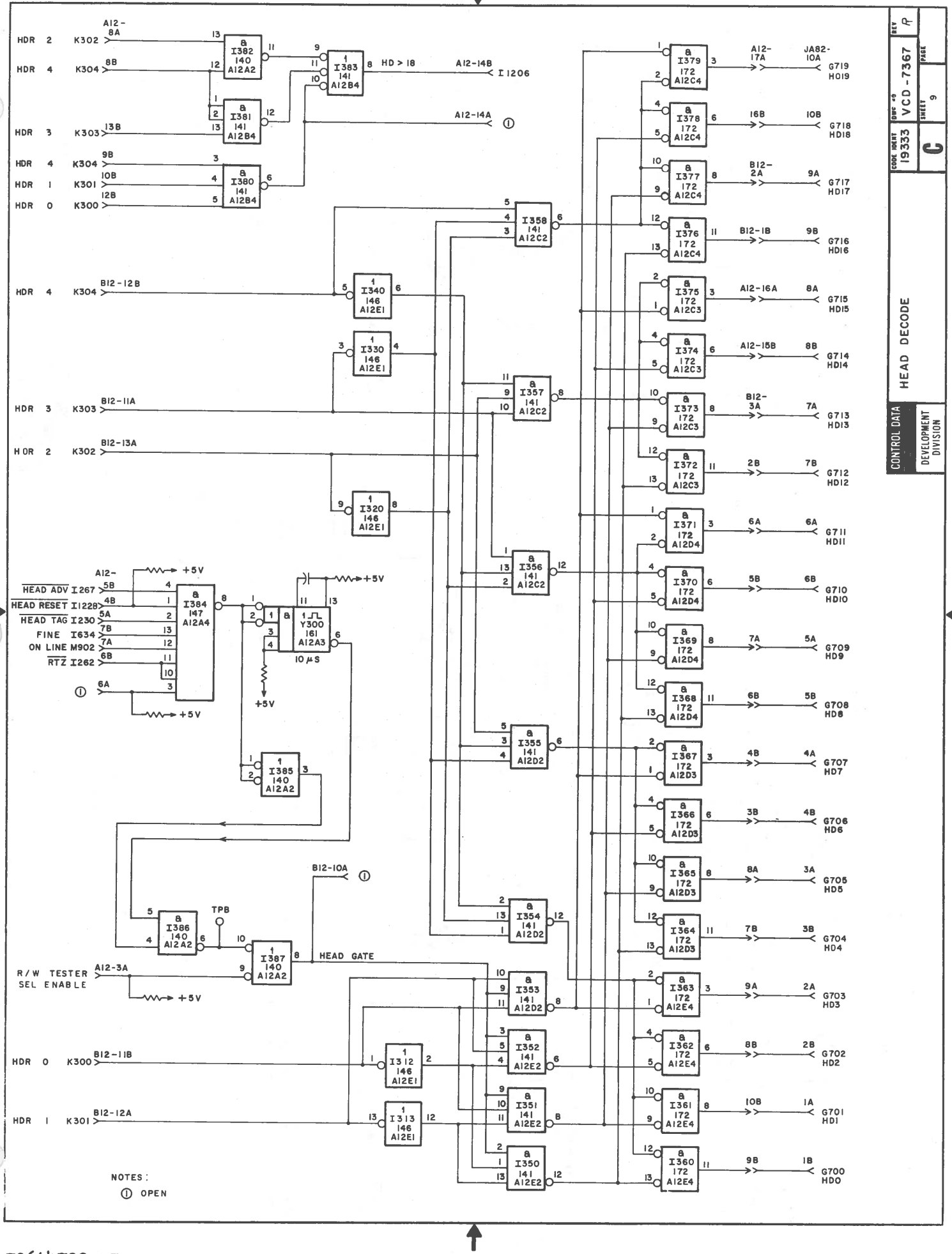
LOGIC NO.	OPEN = 1 CLOSED = 0				
	S514	S513	S512	S511	S510
0	C	C	C	C	C
1	C	C	C	C	O
2	C	C	C	O	C
3	C	C	C	O	O
4	C	C	O	C	C
5	C	C	O	C	O
6	C	C	O	O	C
7	C	C	O	O	O
S	C	O	C	C	C

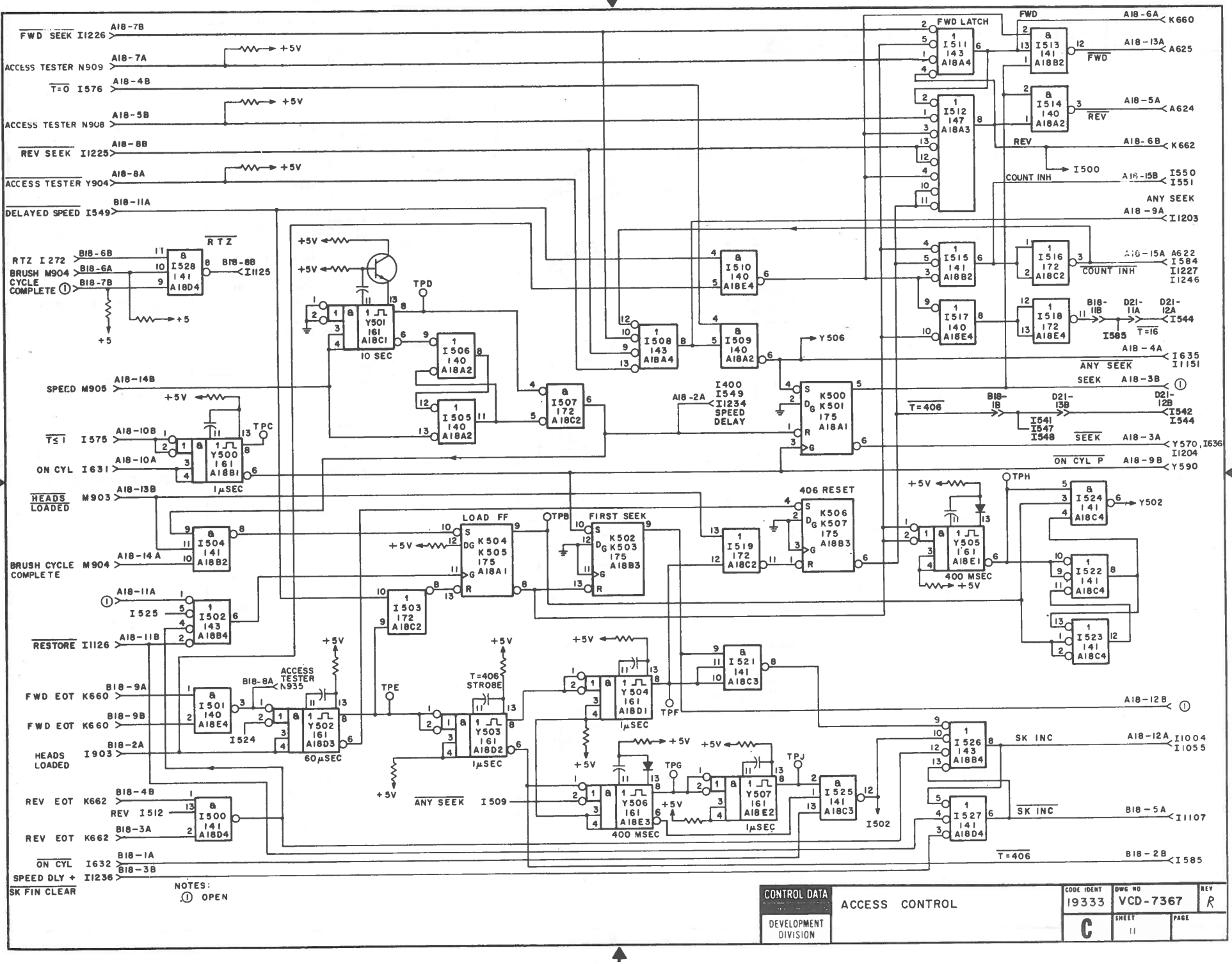
NOTE:

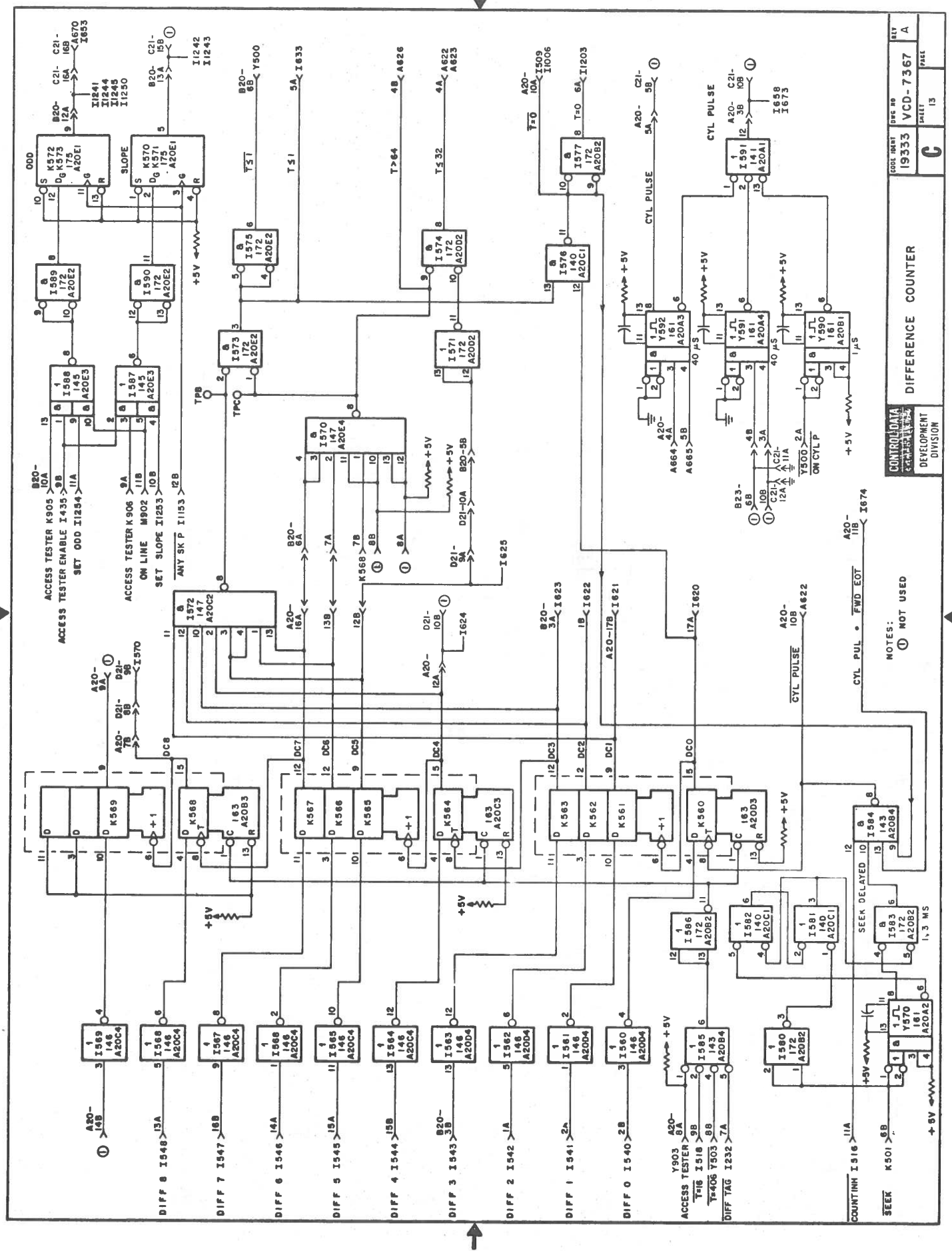
① THIS UNIT SHOWN WITH LOGIC PLUG "0" INSERTED IN OPERATOR CONTROL PANEL

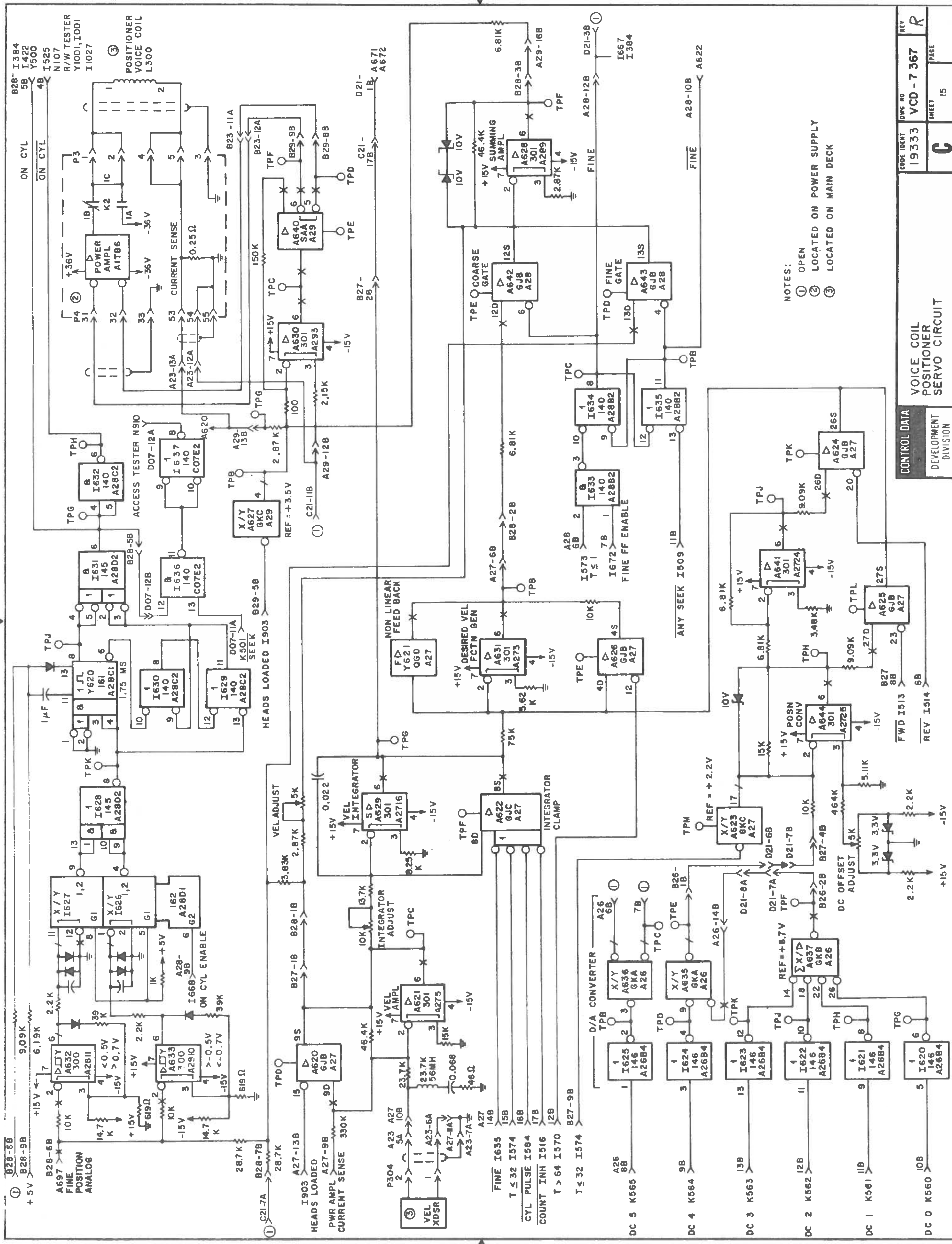
RELEASED	DEVICE ADDRESSING	CODE IDENT 19333	DWG NO VCD-7367	REV G
DEVELOPMENT DIVISION		C	SHEET 5	PAGE

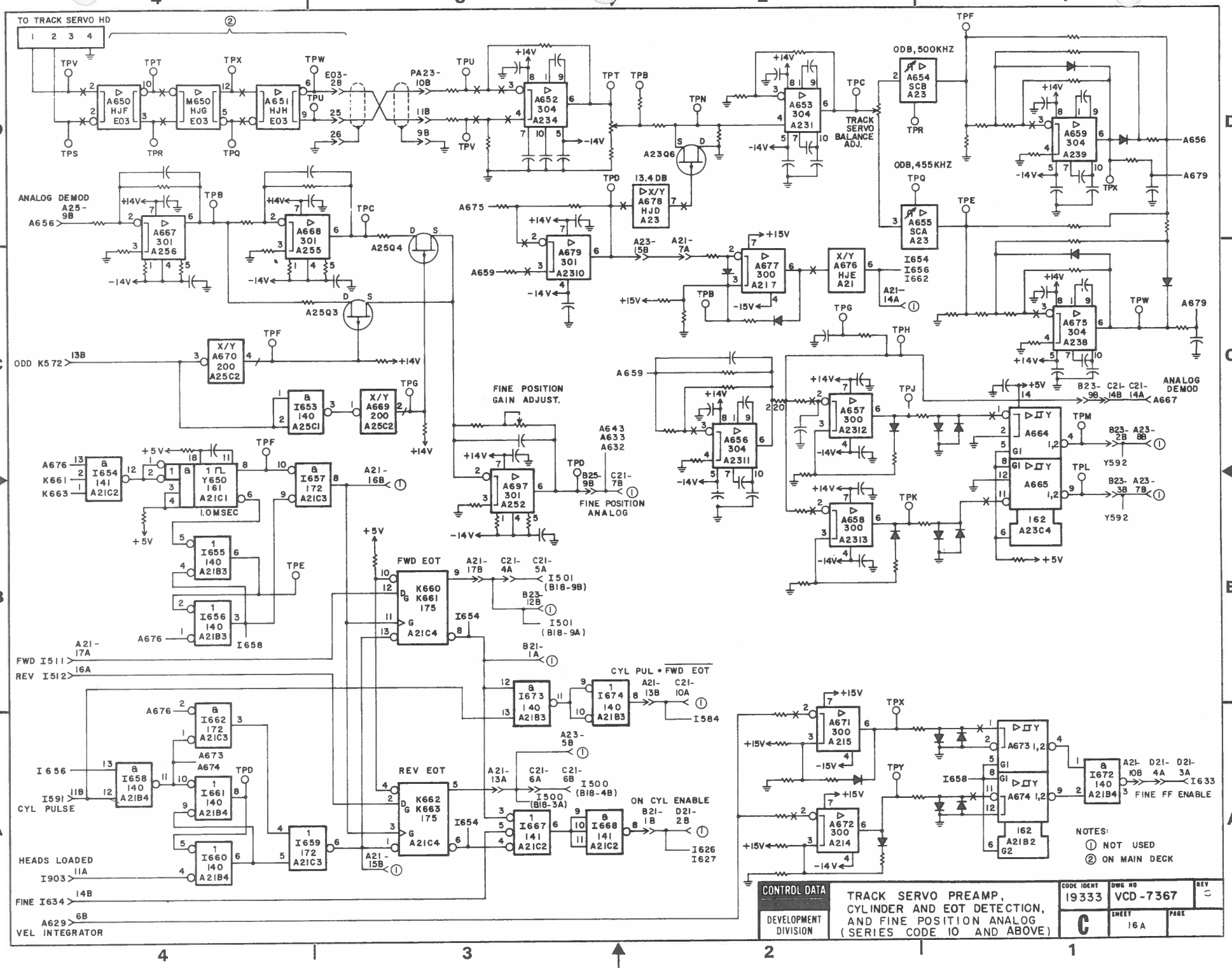

A14-5B
A14-6A
B14-12B
FBOUT 1 R001
A14-5A
A14-4B
A14-3B
FBOUT 3 R003
A14-9B
A14-10A
R/W TESTER N136
B14-11A
A14-9A
A14-8B
A14-7B
FBOUT 2 R002
A14-15A
R/W TESTER N108
A14-16A
A14-17A
FBOUT 4 R004
B14-8B
R/W TESTER N108
B14-7A
B14-6A
B14-13A
FBOUT 0 R000
B14-8A
R/W TESTER N108
B14-9B
WR INNER I268
B14-10B
B14-10A
FBOUT 6 R006
A14-15B
A14-14A
ACCESS TESTER Y900
A14-12B
B14-3B
B14-3A
B14-4A
B14-2A
B14-2B
B14-5A
CMD TAG I233
A14-16B
FAULT K400
A14-14B
A14-13B
R/W TESTER N108
A14-13A
+5V
I269 145 A14A3
I268 145 A14A3
I267 145 A14B3
I266 145 A14B3
I265 145 A14C3
I264 145 A14E3
I263 145 A14E3
I262 145 A14C3
I261 145 A14D3
I260 145 A14D3
I281 145 A14C4
I280 145 A14C4
TPC
TPB
I279 140 A14A2
I278 140 A14A2
I277 140 A14A2
I276 140 A14A2
I275 140 A14C2
I274 141 A14E2
I273 141 A14E2
I272 140 A14C2
I271 140 A14C2
I270 140 A14C2
A14-6B
A14-2A
WR INNER A14-4A C21-38 I273
WR INNER A14-3A I1025
HEAD ADV A14-10B I384
HEAD ADV A14-11B I301 I1206
A14-8A
A14-7A
READ A14-17B
READ B14-1B I415 I1030
ERASE B14-7B
ERASE B14-12A I1229
WRITE OUTER B14-9A
WRITE B14-11B I1230 I1003
RTZ A14-12A I384
RTZ A14-11A I528
B14-4B
B14-5B
B14-1A
B14-6B
NOTES:
① OPEN
CONTROL DATA
DEVELOPMENT DIVISION
COMMAND STEERING
CODE IDENT 19333
DWG # VCD-7367
REV C
C
SHEET 7
PAGE

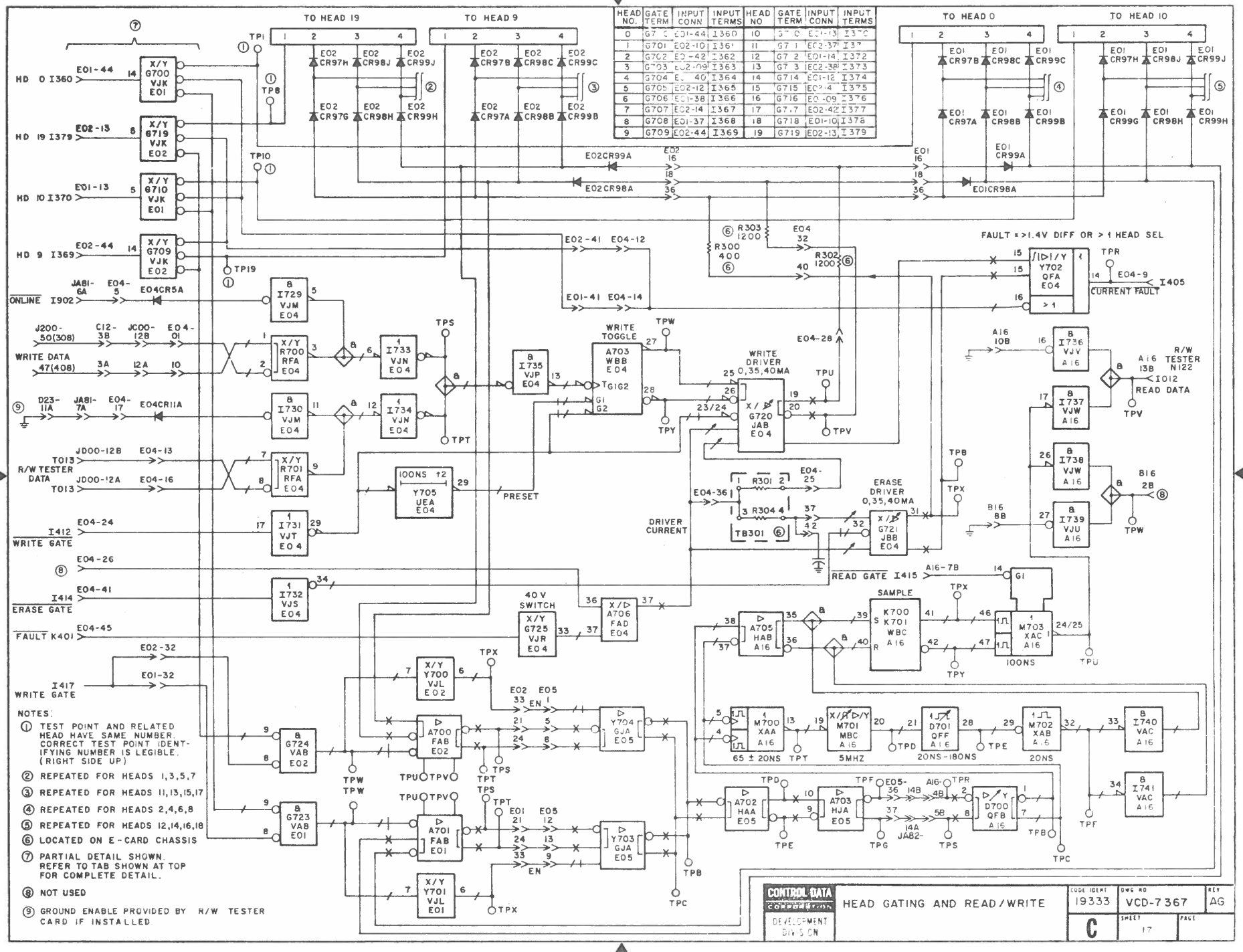

HEAD DECODE
CONTROL DATA
DEVELOPMENT DIVISION
CODE IDENT 19333
DWG # VCD-7367
REV P
SHEET 9
PAGE
HDR 2 K302 A12-8A
HDR 4 K304 8B
HDR 3 K303 13B
HDR 4 K304 9B
HDR 1 K301 10B
HDR 0 K300 12B
I382 140 A12A2
I381 141 A12B4
I383 141 A12B4
I380 141 A12B4
HD > 18
A12-14B
I 1206
A12-14A
HDR 4 K304 B12-12B
HDR 3 K303 B12-11A
HOR 2 K302 B12-13A
I340 146 A12E1
I330 146 A12E1
I320 146 A12E1
I358 141 A12C2
I357 141 A12C2
I356 141 A12C2
I355 141 A12D2
I354 141 A12D2
I353 141 A12D2
I352 141 A12E2
I351 141 A12E2
I350 141 A12E2
HEAD ADV I267
HEAD RESET I1228
HEAD TAG I230
FINE I634
ON LINE M902
RTZ I262
I384 147 A12A4
+5V
Y300 161 A12A3
10 µS
I385 140 A12A2
I386 140 A12A2
I387 140 A12A2
TPB
B12-10A
HEAD GATE
R/W TESTER SEL ENABLE A12-3A
HDR 0 K300 B12-11B
HDR 1 K301 B12-12A
I312 146 A12E1
I313 146 A12E1
I379 172 A12C4
I378 172 A12C4
I377 172 A12C4
I376 172 A12C4
I375 172 A12C3
I374 172 A12C3
I373 172 A12C3
I372 172 A12C3
I371 172 A12D4
I370 172 A12D4
I369 172 A12D4
I368 172 A12D4
I367 172 A12D3
I366 172 A12D3
I365 172 A12D3
I364 172 A12D3
I363 172 A12E4
I362 172 A12E4
I361 172 A12E4
I360 172 A12E4
A12-17A
JA82-10A
G719 HDI9
16B
10B
G718 HDI8
B12-2A
9A
G717 HDI7
B12-1B
9B
G716 HDI6
A12-16A
8A
G715 HDI5
A12-15B
8B
G714 HDI4
B12-3A
7A
G713 HDI3
2B
7B
G712 HDI2
6A
6A
G711 HDII
5B
6B
G710 HDI0
7A
5A
G709 HD9
6B
5B
G708 HD8
4B
4A
G707 HD7
3B
4B
G706 HD6
8A
3A
G705 HD5
7B
3B
G704 HD4
9A
2A
G703 HD3
8B
2B
G702 HD2
10B
1A
G701 HD1
9B
1B
G700 HD0
NOTES:
① OPEN

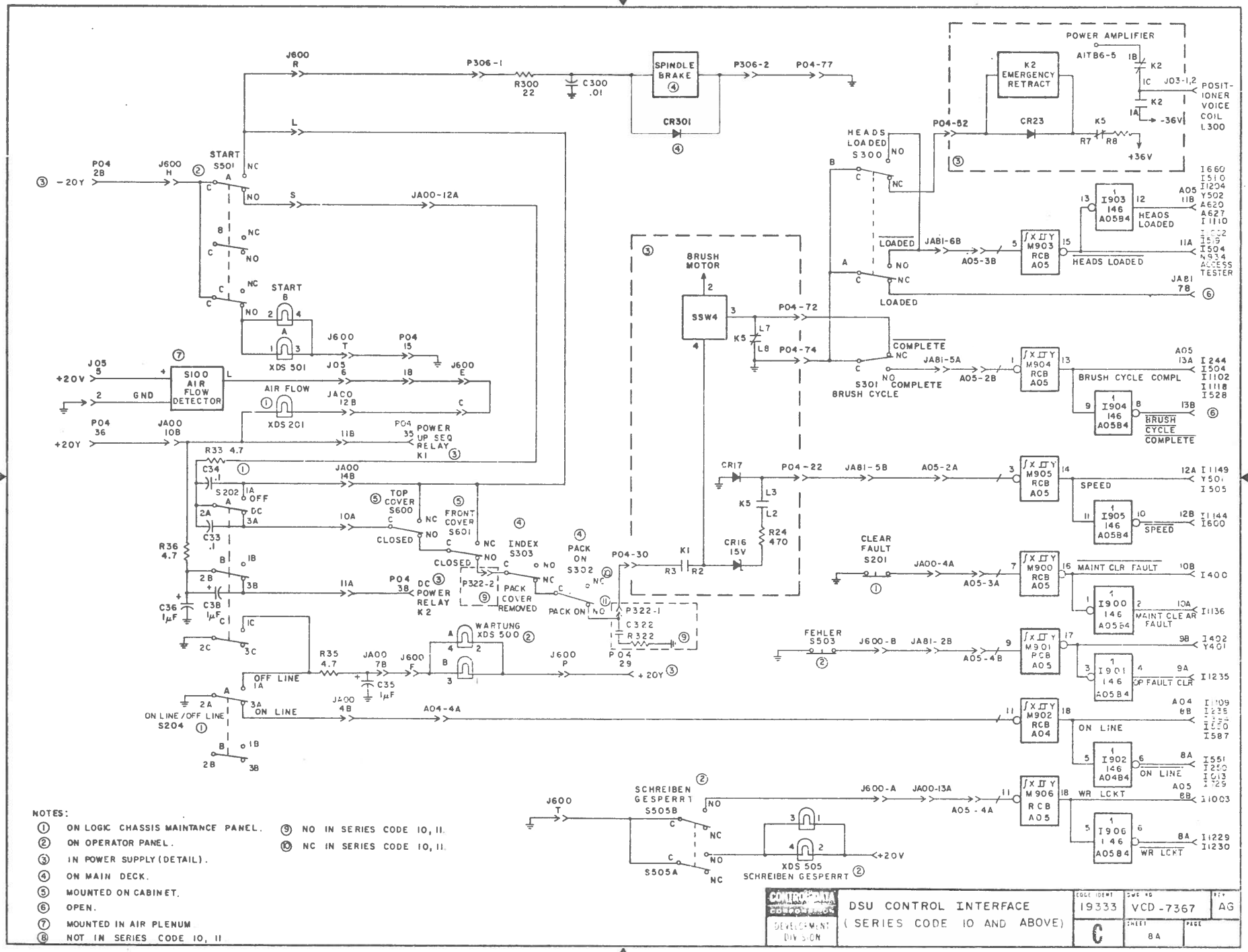

FWD SEEK I1226
ACCESS TESTER N909
T=0 I576
ACCESS TESTER N908
REV SEEK I1225
ACCESS TESTER Y904
DELAYED SPEED I549
RTZ I 272
BRUSH M904 CYCLE COMPLETE ①
SPEED M905
T≤1 I575
ON CYL I631
HEADS LOADED M903
BRUSH CYCLE COMPLETE M904
①
I525
RESTORE I1126
FWD EOT K660
FWD EOT K660
HEADS LOADED I903
REV EOT K662
REV I512
REV EOT K662
ON CYL I632
SPEED DLY + I1236
SK FIN CLEAR
+5V
+5
10 SEC
1μSEC
60μSEC
400 MSEC
TPD
TPC
TPE
TPF
TPG
TPH
TPJ
TPB
LOAD FF
FIRST SEEK
406 RESET
T=406 STROBE
ACCESS TESTER N935
I524
I502
I509
ANY SEEK
I1234 SPEED DELAY
I400 I549
A18-2A
Y506
FWD LATCH
FWD
REV
COUNT INH
ANY SEEK
SEEK
ON CYL P
SK INC
I500
I550 I551
I1203
A622 I584 I1227 I1246
I544
I635 I1151
I542 I544
Y570, I636 I1204
Y590
Y502
I585
I541 I547 I548
I1004 I1055
I1107
I1585
NOTES:
① OPEN
CONTROL DATA
DEVELOPMENT DIVISION
ACCESS CONTROL
CODE IDENT 19333
DWG NO VCD-7367
REV R
SHEET 11
PAGE
C

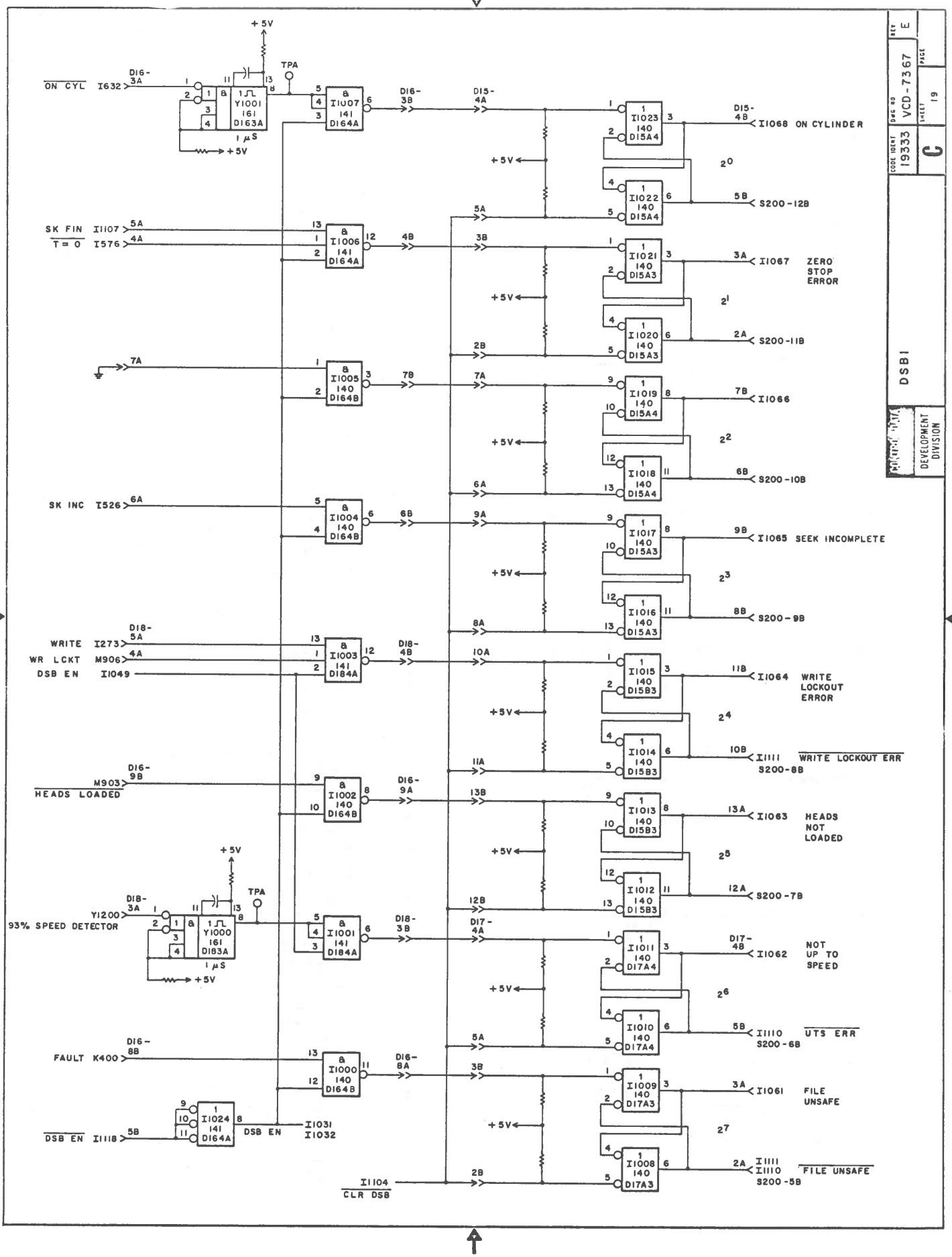

DIFFERENCE COUNTER
CONTROLDATA
DEVELOPMENT DIVISION
CODE IDENT 19333
DWG NO VCD-7367
REV A
SHEET 13
C
NOTES:
① NOT USED
ODD
SLOPE
CYL PULSE
SEEK DELAYED
1.3 MS
ACCESS TESTER K905
ACCESS TESTER ENABLE I435
SET ODD I1234
ACCESS TESTER K906
ON LINE M902
SET SLOPE I1253
ANY SK P I1153
DIFF 8 I548
DIFF 7 I547
DIFF 6 I546
DIFF 5 I545
DIFF 4 I544
DIFF 3 I543
DIFF 2 I542
DIFF 1 I541
DIFF 0 I540
ACCESS TESTER
DIFF TAG
COUNTINH I316
SEEK K501
CYL PUL • FWD EOT
+5V
40 µS
1 µS

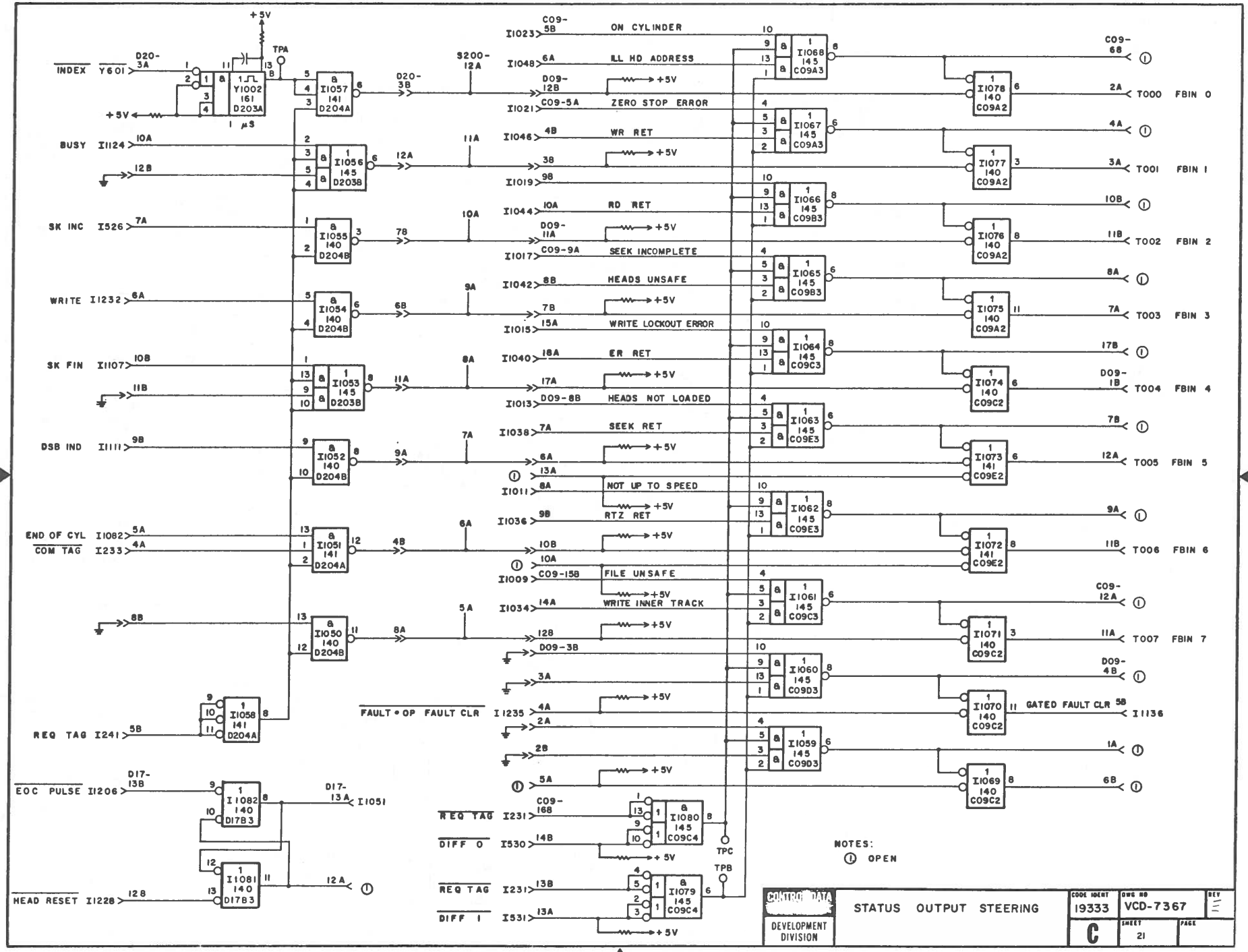

VOICE COIL
POSITIONER
SERVO CIRCUIT
CONTROL DATA
DEVELOPMENT DIVISION
CODE IDENT 19333
DWG NO VCD-7367
REV R
SHEET 15
C
NOTES:
① OPEN
② LOCATED ON POWER SUPPLY
③ LOCATED ON MAIN DECK
D/A CONVERTER
INTEGRATOR CLAMP
VEL INTEGRATOR
VEL AMPL
INTEGRATOR ADJUST
VEL ADJUST
DESIRED VEL FCTN GEN
NON LINEAR FEED BACK
COARSE GATE
FINE GATE
SUMMING AMPL
POSN CONV
DC OFFSET ADJUST
POWER AMPL
CURRENT SENSE
POSITIONER VOICE COIL L300
ACCESS TESTER N910
HEADS LOADED I903
PWR AMPL CURRENT SENSE
VEL XDSR
FINE POSITION ANALOG
ON CYL ENABLE
FINE FF ENABLE
ANY SEEK I509
FWD I513
REV I514
DC 5 K565
DC 4 K564
DC 3 K563
DC 2 K562
DC 1 K561
DC 0 K560

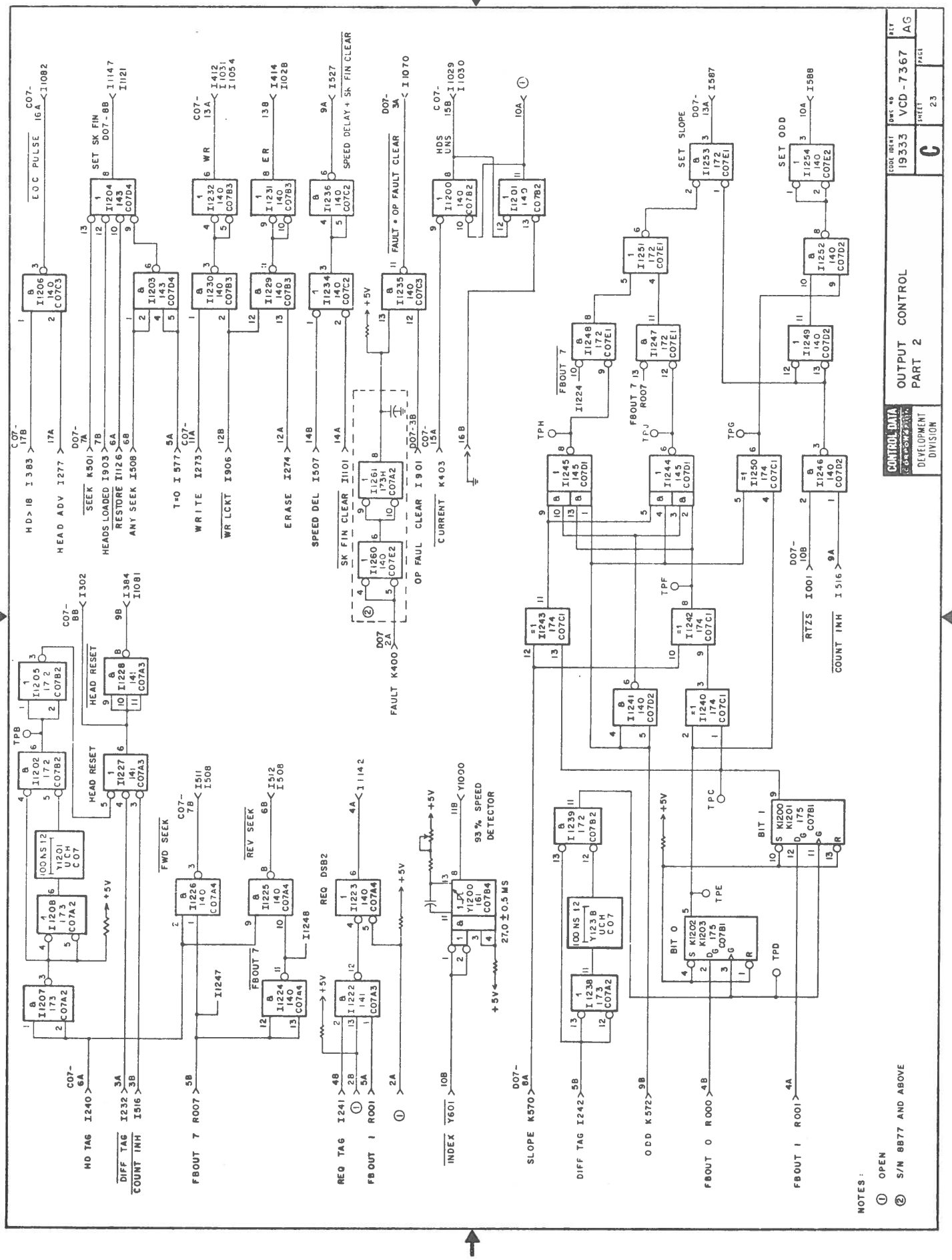

TO TRACK SERVO HD
1 2 3 4
TPV
TPT
TPX
TPW
TPS
TPR
TPQ
TPU
TPN
TPB
TPC
TPD
TPE
TPF
TPG
TPH
TPJ
TPK
TPL
TPM
TPY
A650 HJF E03
M650 HJG E03
A651 HJH E03
E03-28
PA23-10B
11B
9B
25
26
A652 304 A234
A653 304 A231
A654 SCB A23
A655 SCA A23
A659 304 A239
A656
A679
ODB,500KHZ
ODB,455KHZ
TRACK SERVO BALANCE ADJ.
A23Q6
ANALOG DEMOD A25-9B
A656
A667 301 A256
A668 301 A255
A25Q4
A25Q3
A675
A679 301 A2310
13.4 DB
X/Y A678 HJD A23
A23-15B
A21-7A
A677 300 A217
X/Y A676 HJE A21
I654
I656
I662
A21-14A
A675 304 A238
ODD K572 13B
X/Y A670 200 A25C2
X/Y A669 200 A25C2
I653 140 A25C1
FINE POSITION GAIN ADJUST.
A697 301 A252
A643
A633
A632
FINE POSITION ANALOG
A659
A656 304 A2311
A657 300 A2312
A658 300 A2313
A664
A665
162 A23C4
B23-9B
C21-7B
C21-14B
C21-14A
ANALOG DEMOD A667
B23-28 88
Y592
A676 K661 K663
I654 141 A21C2
Y650 161 A21C1
1.0MSEC
I657 172 A21C3
A21-16B
I655 140 A21B3
I656 140 A21B3
I658
FWD EOT
K660 K661 175
A21C4
A21-17B
C21-4A
C21-5A
I501 (B18-9B)
B23-12B
I501 (B18-9A)
FWD I511
REV I512
A21-17A
16A
B21-1A
CYL PUL • FWD EOT
I673 140 A21B3
I674 140 A21B3
A21-13B
C21-10A
I584
A23-5B
A676
I662 172 A21C3
A673
A674
I656
I658 140 A21B4
I591
CYL PULSE
I661 140 A21B4
TPD
REV EOT
K662 K663 175
A21-13A
C21-6A
C21-6B
I500 (B18-4B)
I500 (B18-3A)
I654
I659 172 A21C3
I667 141 A21C2
I668 141 A21C2
ON CYL ENABLE
B21-1B
D21-2B
I626
I627
HEADS LOADED
I903
11A
I660 140 A21B4
A21-15B
FINE I634
14B
A629
6B
VEL INTEGRATOR
A671 300 A215
A672 300 A214
A673 1,2
A674 1,2
I672 140 A21B4
A21-10B
D21-4A
D21-3A
I633
FINE FF ENABLE
162 A21B2 G2
NOTES:
① NOT USED
② ON MAIN DECK
CONTROL DATA
DEVELOPMENT DIVISION
TRACK SERVO PREAMP, CYLINDER AND EOT DETECTION, AND FINE POSITION ANALOG (SERIES CODE 10 AND ABOVE)
CODE IDENT 19333
DWG NO VCD-7367
REV C
SIZE C
SHEET 16A
PAGE

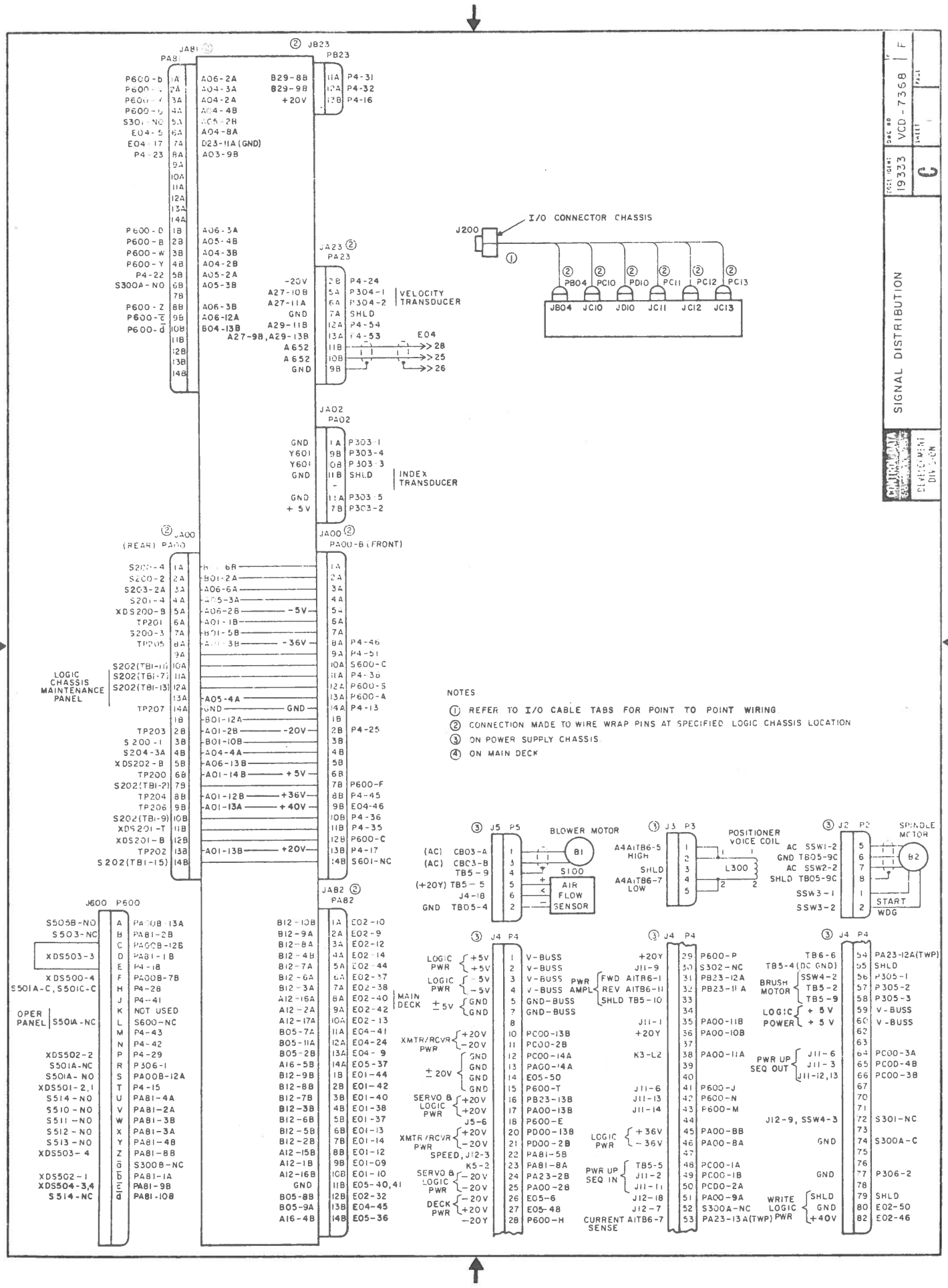

TO HEAD 19
TO HEAD 9
TO HEAD 0
TO HEAD 10
HEAD NO. | GATE TERM | INPUT CONN | INPUT TERMS | HEAD NO | GATE TERM | INPUT CONN | INPUT TERMS
0 | G7 0 | E01-44 | I360 | 10 | G7 0 | E01-13 | I370
1 | G701 | E02-10 | I361 | 11 | G7 1 | E02-37 | I371
2 | G702 | E01-42 | I362 | 12 | G7 2 | E01-14 | I372
3 | G703 | E02-09 | I363 | 13 | G7 3 | E02-38 | I373
4 | G704 | E01-40 | I364 | 14 | G714 | E01-12 | I374
5 | G705 | E02-12 | I365 | 15 | G715 | E02-4 | I375
6 | G706 | E01-38 | I366 | 16 | G716 | E01-09 | I376
7 | G707 | E02-14 | I367 | 17 | G7.7 | E02-42 | I377
8 | G708 | E01-37 | I368 | 18 | G718 | E01-10 | I378
9 | G709 | E02-44 | I369 | 19 | G719 | E02-13 | I379
HD 0 I360
HD 19 I379
HD 10 I370
HD 9 I369
ONLINE I902
WRITE DATA
R/W TESTER DATA
WRITE GATE I412
ERASE GATE I414
FAULT K401
WRITE GATE I417
FAULT = >1.4V DIFF OR > 1 HEAD SEL
CURRENT FAULT I405
WRITE TOGGLE
WRITE DRIVER 0,35,40MA
ERASE DRIVER 0,35,40MA
DRIVER CURRENT
PRESET
READ GATE I415
SAMPLE
READ DATA I012
R/W TESTER N122
40V SWITCH
65 ± 20NS
5MHZ
20NS-180NS
20NS
100NS
NOTES:
① TEST POINT AND RELATED HEAD HAVE SAME NUMBER. CORRECT TEST POINT IDENTIFYING NUMBER IS LEGIBLE. (RIGHT SIDE UP)
② REPEATED FOR HEADS 1,3,5,7
③ REPEATED FOR HEADS 11,13,15,17
④ REPEATED FOR HEADS 2,4,6,8
⑤ REPEATED ON E-CARD CHASSIS
⑥ LOCATED ON E-CARD CHASSIS
⑦ PARTIAL DETAIL SHOWN. REFER TO TAB SHOWN AT TOP FOR COMPLETE DETAIL.
⑧ NOT USED
⑨ GROUND ENABLE PROVIDED BY R/W TESTER CARD IF INSTALLED
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
HEAD GATING AND READ/WRITE
CODE IDENT 19333
DWG NO VCD-7367
REV AG
C
SHEET 17
PAGE

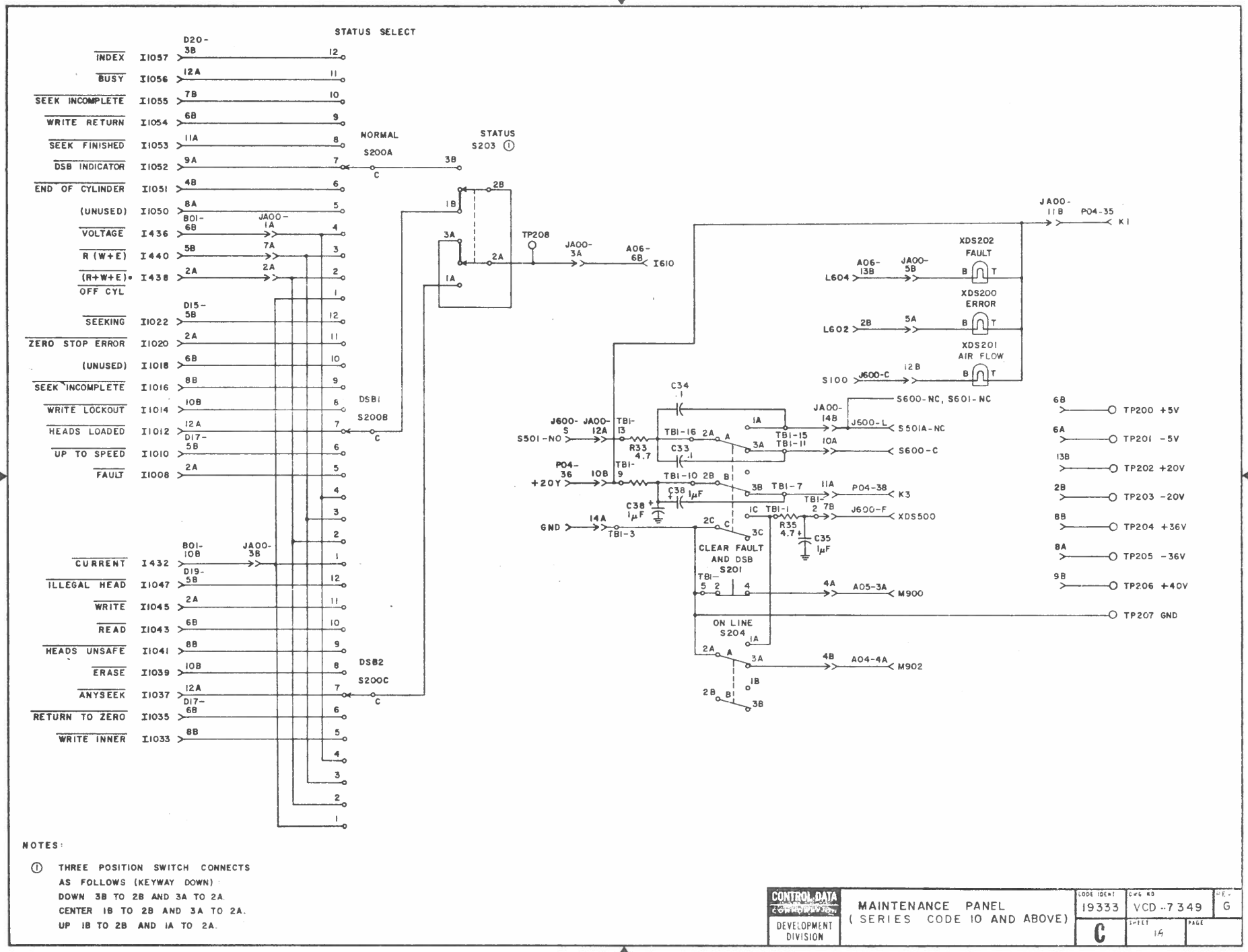

POWER AMPLIFIER
K2 EMERGENCY RETRACT
SPINDLE BRAKE
CR301
HEADS LOADED S300
BRUSH MOTOR
SSW4
START S501
START B
XDS 501
S100 AIR FLOW DETECTOR
AIR FLOW
XDS 201
POWER UP SEQ RELAY K1
S202 ON LINE/OFF LINE
TOP COVER S600
FRONT COVER S601
INDEX S303
PACK ON S302
P322-1
P322-2
PACK COVER REMOVED
DC POWER RELAY K2
WARTUNG XDS 500
OFF LINE
ON LINE
CLEAR FAULT S201
FEHLER S503
SCHREIBEN GESPERRT S505B
S505A
XDS 505 SCHREIBEN GESPERRT
HEADS LOADED
BRUSH CYCLE COMPL
SPEED
MAINT CLR FAULT
ON LINE
WR LCKT
BRUSH CYCLE COMPLETE
POSITIONER VOICE COIL L300
ACCESS TESTER
-20V
+20V
+36V
GND
NOTES:
① ON LOGIC CHASSIS MAINTANCE PANEL.
② ON OPERATOR PANEL.
③ IN POWER SUPPLY (DETAIL).
④ ON MAIN DECK.
⑤ MOUNTED ON CABINET.
⑥ OPEN.
⑦ MOUNTED IN AIR PLENUM.
⑧ NOT IN SERIES CODE 10, 11
⑨ NO IN SERIES CODE 10, 11.
⑩ NC IN SERIES CODE 10, 11.
DSU CONTROL INTERFACE
(SERIES CODE 10 AND ABOVE)
CONTROL DATA BOTTINEAU DEVELOPMENT DIVISION
CODE IDENT 19333
DWG NO VCD-7367
REV AG
SHEET C
SHEET 8A
PAGE


DSBI
DEVELOPMENT DIVISION
DWG NO VCD-7367
REV E
CODE IDENT 19333
C
SHEET 19
PAGE
ON CYL I632
SK FIN I1107
T=0 I576
SK INC I526
WRITE I273
WR LCKT M906
DSB EN I1049
M903 HEADS LOADED
Y1200 93% SPEED DETECTOR
FAULT K400
DSB EN I1118
CLR DSB I1104
TPA
+5V
1 μS
I1068 ON CYLINDER
I1067 ZERO STOP ERROR
I1066
I1065 SEEK INCOMPLETE
I1064 WRITE LOCKOUT ERROR
I1063 HEADS NOT LOADED
I1062 NOT UP TO SPEED
I1061 FILE UNSAFE
I1111 WRITE LOCKOUT ERR S200-8B
I1110 UTS ERR S200-6B
I1111 I1110 FILE UNSAFE S200-5B
S200-12B
S200-11B
S200-10B
S200-9B
S200-7B
I1031 I1032 DSB EN


+5V
TPA
INDEX
Y601
D20-3A
Y1002 161 D203A
1 μs
I1057 141 D204A
D20-3B
S200-12A
BUSY I1124
10A
12B
I1056 145 D203B
12A
11A
SK INC I526
7A
I1055 140 D204B
7B
10A
WRITE I1232
6A
I1054 140 D204B
6B
9A
SK FIN I1107
10B
11B
I1053 145 D203B
11A
8A
DSB IND I1111
9B
I1052 140 D204B
9A
7A
END OF CYL I1082
5A
COM TAG I1233
4A
I1051 141 D204A
4B
6A
8B
I1050 140 D204B
8A
5A
REQ TAG I241
5B
I1058 141 D204A
EOC PULSE I1206
D17-13B
I1082 140 D17B3
D17-13A
I1051
HEAD RESET I1228
12B
I1081 140 D17B3
12A
C09-5B
I1023
ON CYLINDER
I1048
6A
ILL HD ADDRESS
D09-12B
+5V
I1021
C09-5A
ZERO STOP ERROR
I1046
4B
WR RET
3B
I1019
9B
I1044
10A
RD RET
D09-11A
I1017
C09-9A
SEEK INCOMPLETE
I1042
8B
HEADS UNSAFE
7B
I1015
15A
WRITE LOCKOUT ERROR
I1040
16A
ER RET
17A
I1013
D09-8B
HEADS NOT LOADED
I1038
7A
SEEK RET
6A
13A
I1011
8A
NOT UP TO SPEED
I1036
9B
RTZ RET
10B
I1009
10A
C09-15B
FILE UNSAFE
WRITE INNER TRACK
I1034
14A
12B
D09-3B
3A
FAULT • OP FAULT CLR
I1235
4A
2A
2B
5A
REQ TAG
I1231
C09-16B
DIFF 0
I530
14B
I1080 145 C09C4
TPC
REQ TAG
I1231
13B
DIFF 1
I531
13A
I1079 145 C09C4
TPB
I1068 145 C09A3
I1067 145 C09A3
I1066 145 C09B3
I1065 145 C09B3
I1064 145 C09C3
I1063 145 C09E3
I1062 145 C09E3
I1061 145 C09C3
I1060 145 C09D3
I1059 145 C09D3
I1078 140 C09A2
I1077 140 C09A2
I1076 140 C09A2
I1075 140 C09A2
I1074 140 C09C2
I1073 141 C09E2
I1072 141 C09E2
I1071 140 C09C2
I1070 140 C09C2
I1069 140 C09C2
C09-6B
2A
T000 FBIN 0
4A
T001 FBIN 1
3A
10B
T002 FBIN 2
11B
8A
T003 FBIN 3
7A
17B
D09-1B
T004 FBIN 4
7B
T005 FBIN 5
12A
9A
T006 FBIN 6
11B
C09-12A
T007 FBIN 7
11A
D09-4B
GATED FAULT CLR 5B
I1136
1A
6B
NOTES:
① OPEN
CONTROL DATA
DEVELOPMENT DIVISION
STATUS OUTPUT STEERING
CODE IDENT 19333
DWG NO VCD-7367
REV
C
SHEET 21
PAGE


OUTPUT CONTROL
PART 2
CONTROL DATA
DEVELOPMENT DIVISION
CODE IDENT 19333
DWG NO VCD-7367
REV AG
SIZE C
SHEET 23
HD TAG I240
DIFF TAG I232
COUNT INH I516
FBOUT 7 R007
REQ TAG I241
FBOUT 1 R001
INDEX Y601
SLOPE K570
DIFF TAG I242
ODD K572
FBOUT 0 R000
FBOUT 1 R001
HD>18 I383
HEAD ADV I277
SEEK K501
HEADS LOADED I903
RESTORE I126
ANY SEEK I508
T=0 I 577
WRITE I273
WR LCKT I906
ERASE I274
SPEED DEL I507
SK FIN CLEAR I1101
OP FAUL CLEAR I901
CURRENT K403
FAULT K400
EOC PULSE
SET SK FIN
WR
ER
SPEED DELAY + SK FIN CLEAR
FAULT + OP FAULT CLEAR
HDS UNS
HEAD RESET
FWD SEEK
REV SEEK
REQ DSB2
93 % SPEED DETECTOR
27.0 ± 0.5 MS
SET SLOPE
SET ODD
RTZS I001
COUNT INH I 516
BIT O
BIT I
NOTES:
① OPEN
② S/N 8877 AND ABOVE

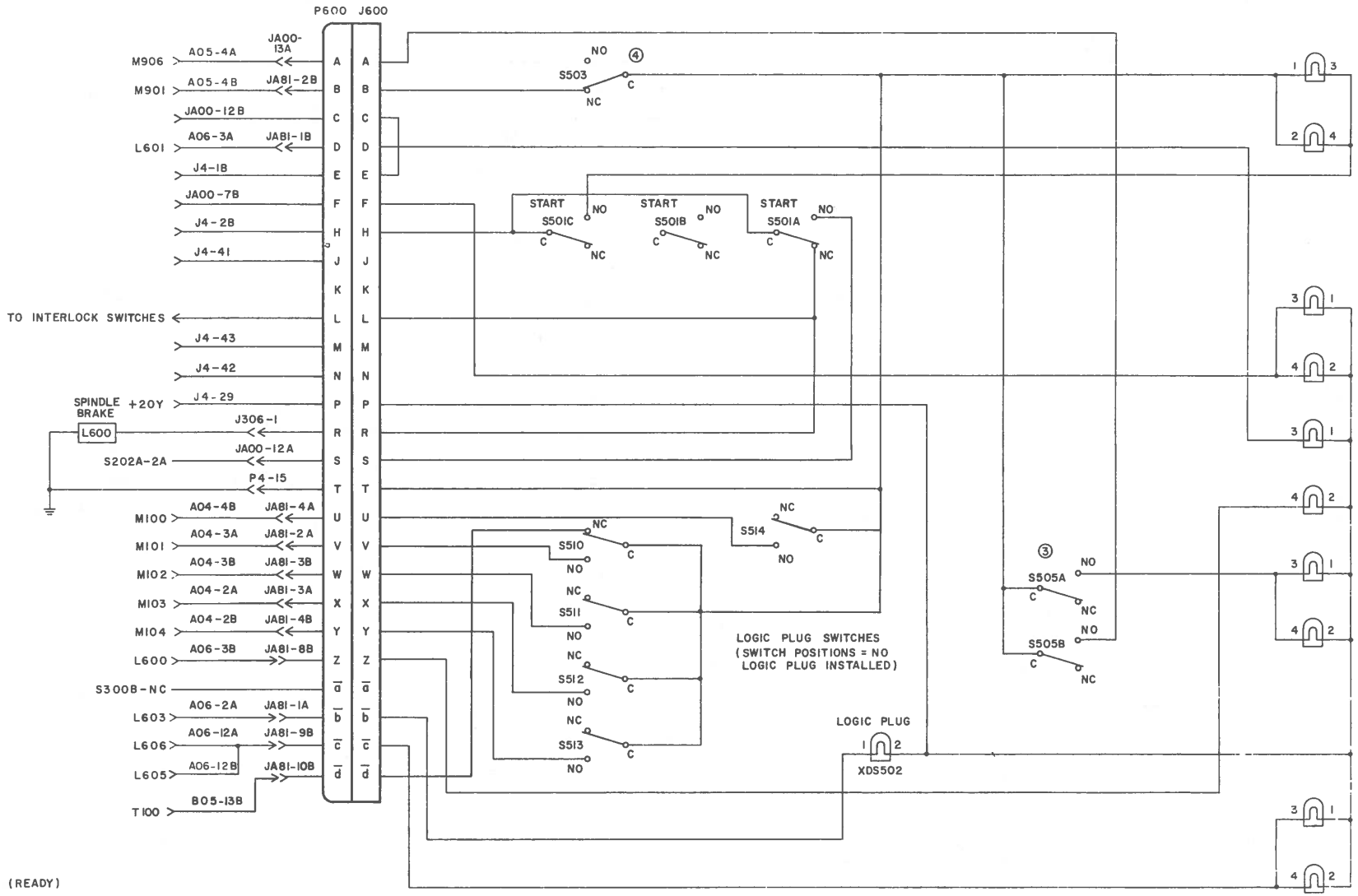

SIGNAL DISTRIBUTION
DWG NO VCD-7368
FSCM IDENT 19333
SIZE C
SHEET
REV F
CONTROL DATA CORPORATION
CLASSIFICATION DIVISION
I/O CONNECTOR CHASSIS
J200
JB04 JC10 JD10 JC11 JC12 JC13
PB04 PC10 PD10 PC11 PC12 PC13
JA81 PA81
JB23 PB23
JA23 PA23
JA02 PA02
JA00 (REAR) PA00
JA00 PA00-B (FRONT)
JA82 PA82
J600 P600
VELOCITY TRANSDUCER
INDEX TRANSDUCER
LOGIC CHASSIS MAINTENANCE PANEL
OPER PANEL
BLOWER MOTOR
POSITIONER VOICE COIL
SPINDLE MOTOR
AIR FLOW SENSOR
L300
START WDG
MAIN DECK
NOTES
1 REFER TO I/O CABLE TABS FOR POINT TO POINT WIRING
2 CONNECTION MADE TO WIRE WRAP PINS AT SPECIFIED LOGIC CHASSIS LOCATION
3 ON POWER SUPPLY CHASSIS
4 ON MAIN DECK



NOTES:

① THREE POSITION SWITCH CONNECTS AS FOLLOWS (KEYWAY DOWN):
DOWN 3B TO 2B AND 3A TO 2A.
CENTER 1B TO 2B AND 3A TO 2A.
UP 1B TO 2B AND 1A TO 2A.

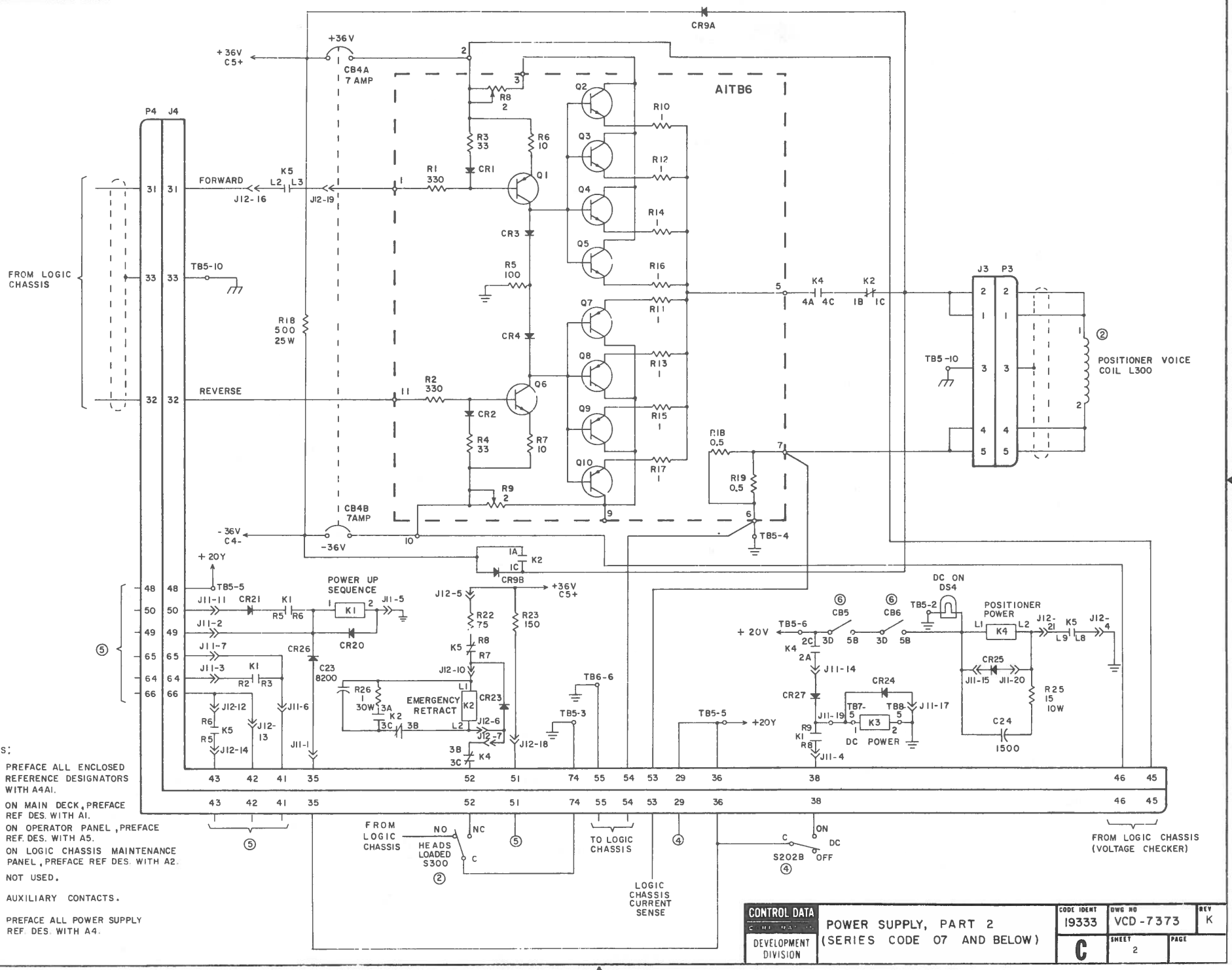
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	MAINTENANCE PANEL (SERIES CODE 10 AND ABOVE)	CODE IDENT 19333	DWG NO VCD-7349	REV G
		SIZE C	SHEET 14	PAGE



NOTES:

① BEREIT (READY)
② WARTUNG (TEST)
③ SCHREIBEN (WRITE GESPERRT LOCKOUT)
④ FEHLER (FAULT)

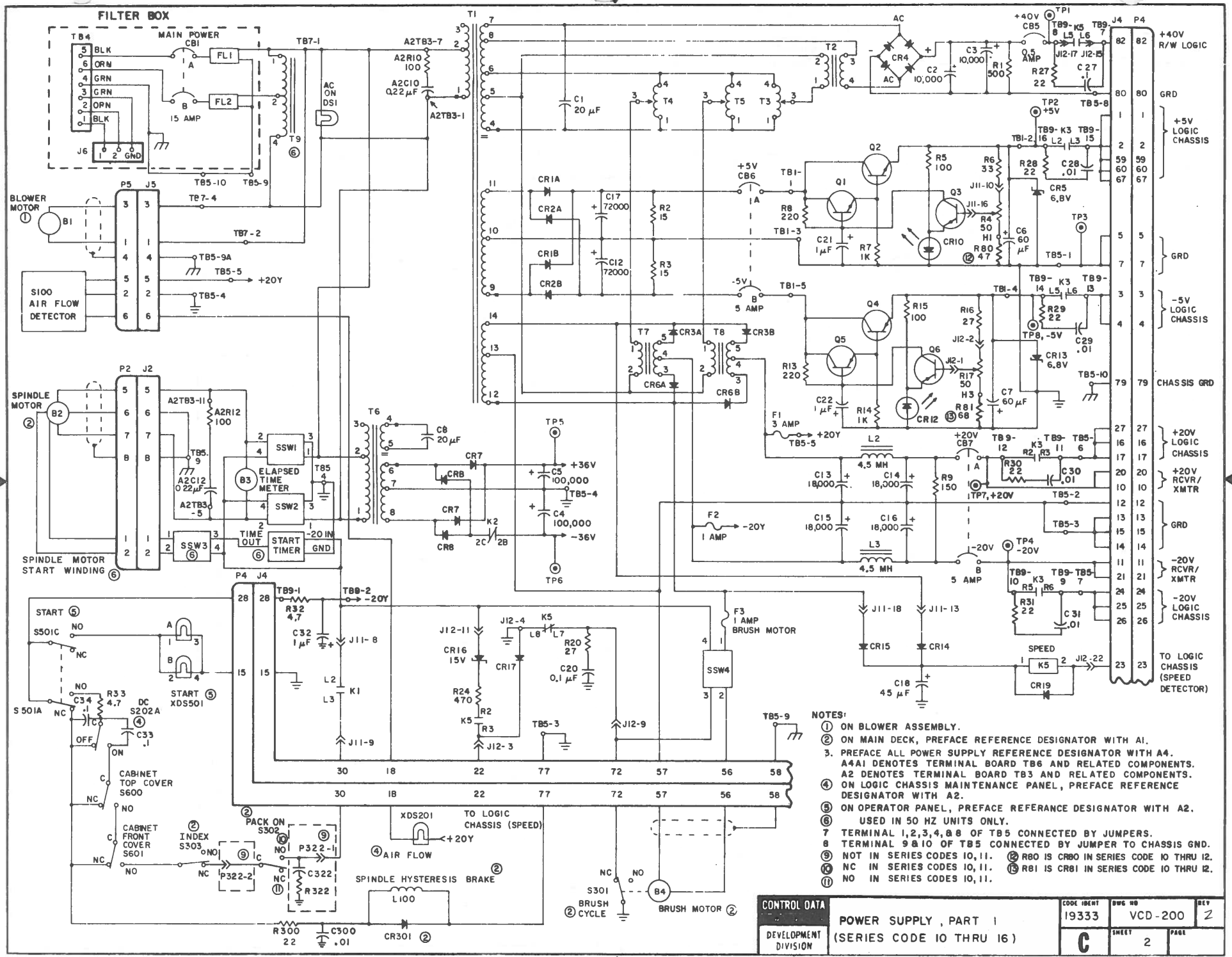
CONTROL DATA	CONTROL PANEL	CODE IDENT 19333	DWG NO VCD-7349	E
DEVELOPMENT DIVISION		C	SHEET 2	PAGE



NOTES:

1. PREFACE ALL ENCLOSED REFERENCE DESIGNATORS WITH A4AI.
2. ON MAIN DECK, PREFACE REF DES. WITH AI.
3. ON OPERATOR PANEL, PREFACE REF. DES. WITH A5.
4. ON LOGIC CHASSIS MAINTENANCE PANEL, PREFACE REF DES. WITH A2.
5. NOT USED.
6. AUXILIARY CONTACTS.
7. PREFACE ALL POWER SUPPLY REF. DES. WITH A4.

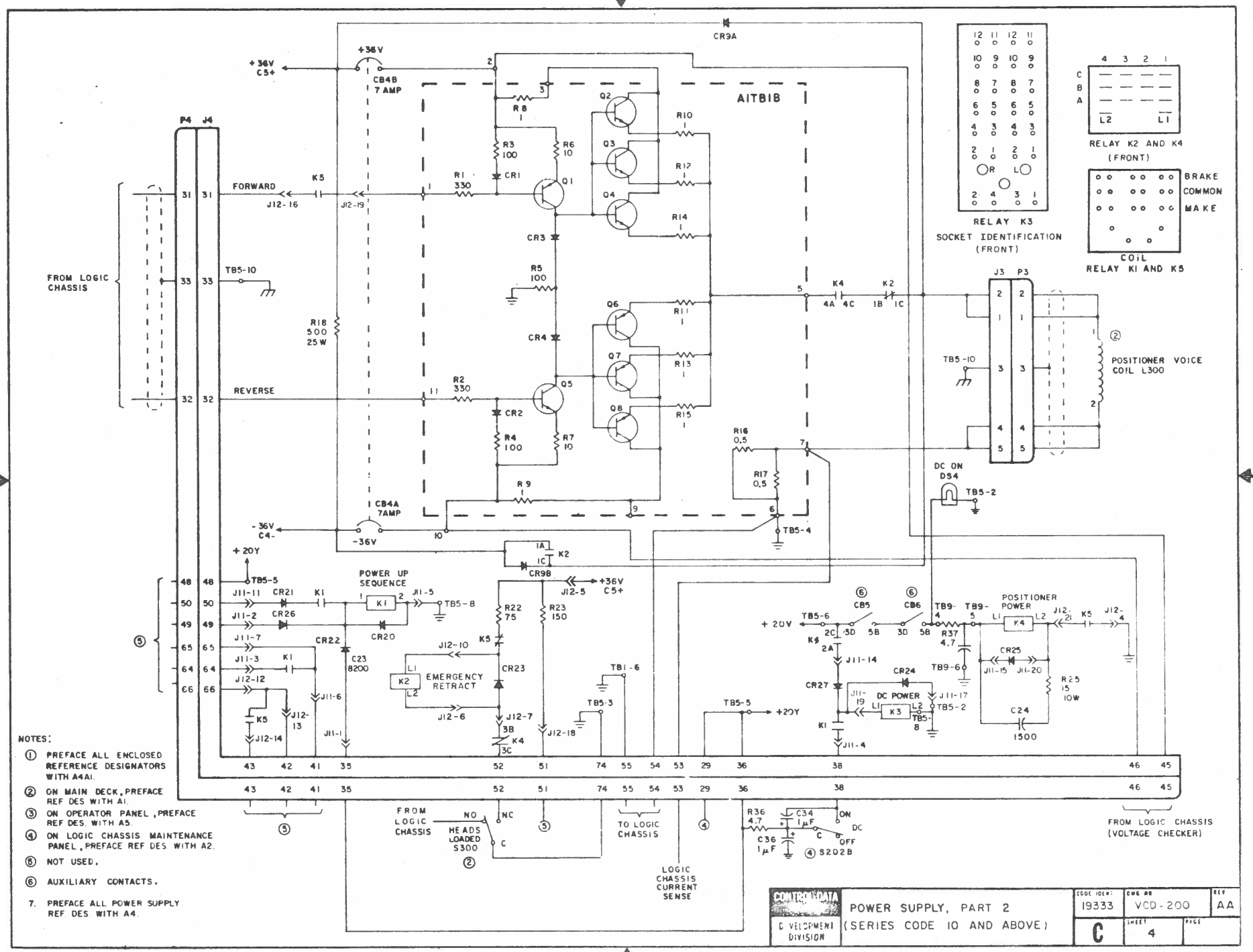
CONTROL DATA	POWER SUPPLY, PART 2 (SERIES CODE 07 AND BELOW)	CODE IDENT 19333	DWG NO VCD-7373	REV K
DEVELOPMENT DIVISION		C	SHEET 2	PAGE



NOTES:

1. ON BLOWER ASSEMBLY.
2. ON MAIN DECK, PREFACE REFERENCE DESIGNATOR WITH A1.
3. PREFACE ALL POWER SUPPLY REFERENCE DESIGNATOR WITH A4. A4A1 DENOTES TERMINAL BOARD TB6 AND RELATED COMPONENTS. A2 DENOTES TERMINAL BOARD TB3 AND RELATED COMPONENTS.
4. ON LOGIC CHASSIS MAINTENANCE PANEL, PREFACE REFERENCE DESIGNATOR WITH A2.
5. ON OPERATOR PANEL, PREFACE REFERANCE DESIGNATOR WITH A2.
6. USED IN 50 HZ UNITS ONLY.
7. TERMINAL 1,2,3,4,&8 OF TB5 CONNECTED BY JUMPERS.
8. TERMINAL 9&10 OF TB5 CONNECTED BY JUMPER TO CHASSIS GND.
9. NOT IN SERIES CODES 10, 11.
10. NC IN SERIES CODES 10, 11.
11. NO IN SERIES CODES 10, 11.
12. R80 IS CR80 IN SERIES CODE 10 THRU 12.
13. R81 IS CR81 IN SERIES CODE 10 THRU 12.

CONTROL DATA	POWER SUPPLY, PART 1 (SERIES CODE 10 THRU 16)	CODE IDENT 19333	DWG NO VCD-200	REV 2
DEVELOPMENT DIVISION		C	SHEET 2	PAGE



NOTES:

① PREFACE ALL ENCLOSED REFERENCE DESIGNATORS WITH A4A1.

② ON MAIN DECK, PREFACE REF DES WITH A1.

③ ON OPERATOR PANEL, PREFACE REF DES WITH A5.

④ ON LOGIC CHASSIS MAINTENANCE PANEL, PREFACE REF DES WITH A2.

⑤ NOT USED.

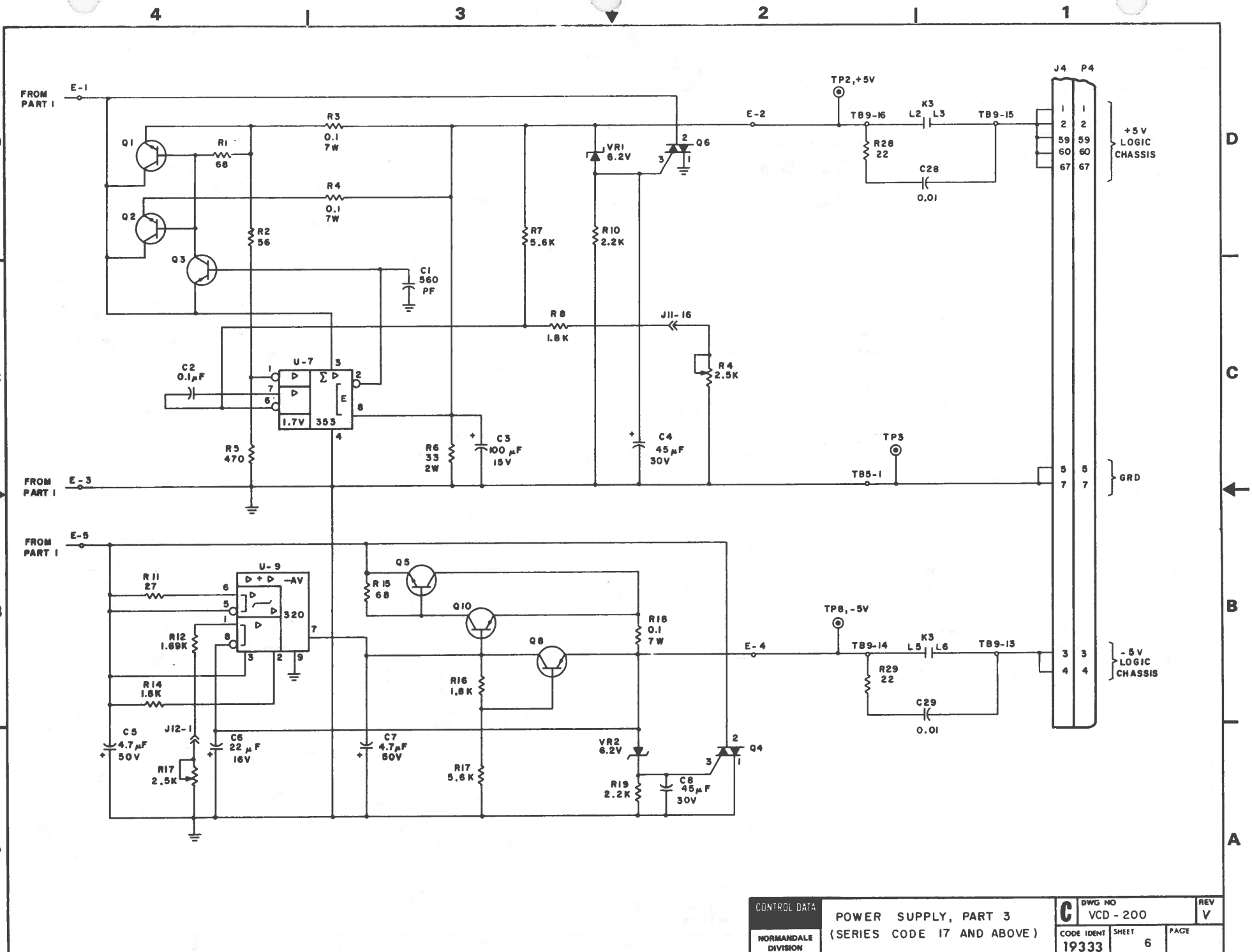
⑥ AUXILIARY CONTACTS.

7. PREFACE ALL POWER SUPPLY REF DES WITH A4.

CONTROL DATA DEVELOPMENT DIVISION

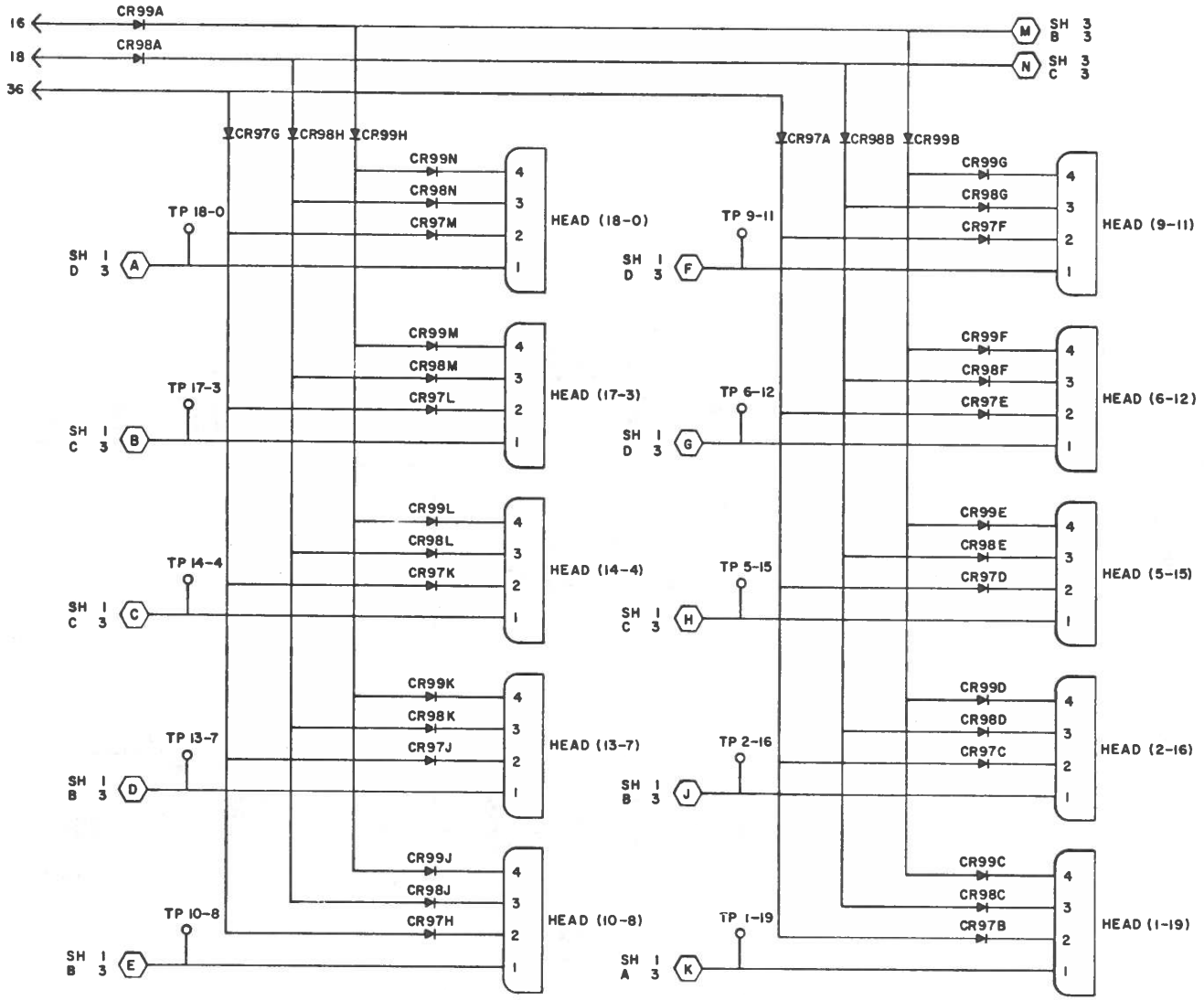
POWER SUPPLY, PART 2 (SERIES CODE 10 AND ABOVE)

CODE IDENT	DWG NO	REV
19333	VCD-200	AA
C	SHEET 4	PAGE



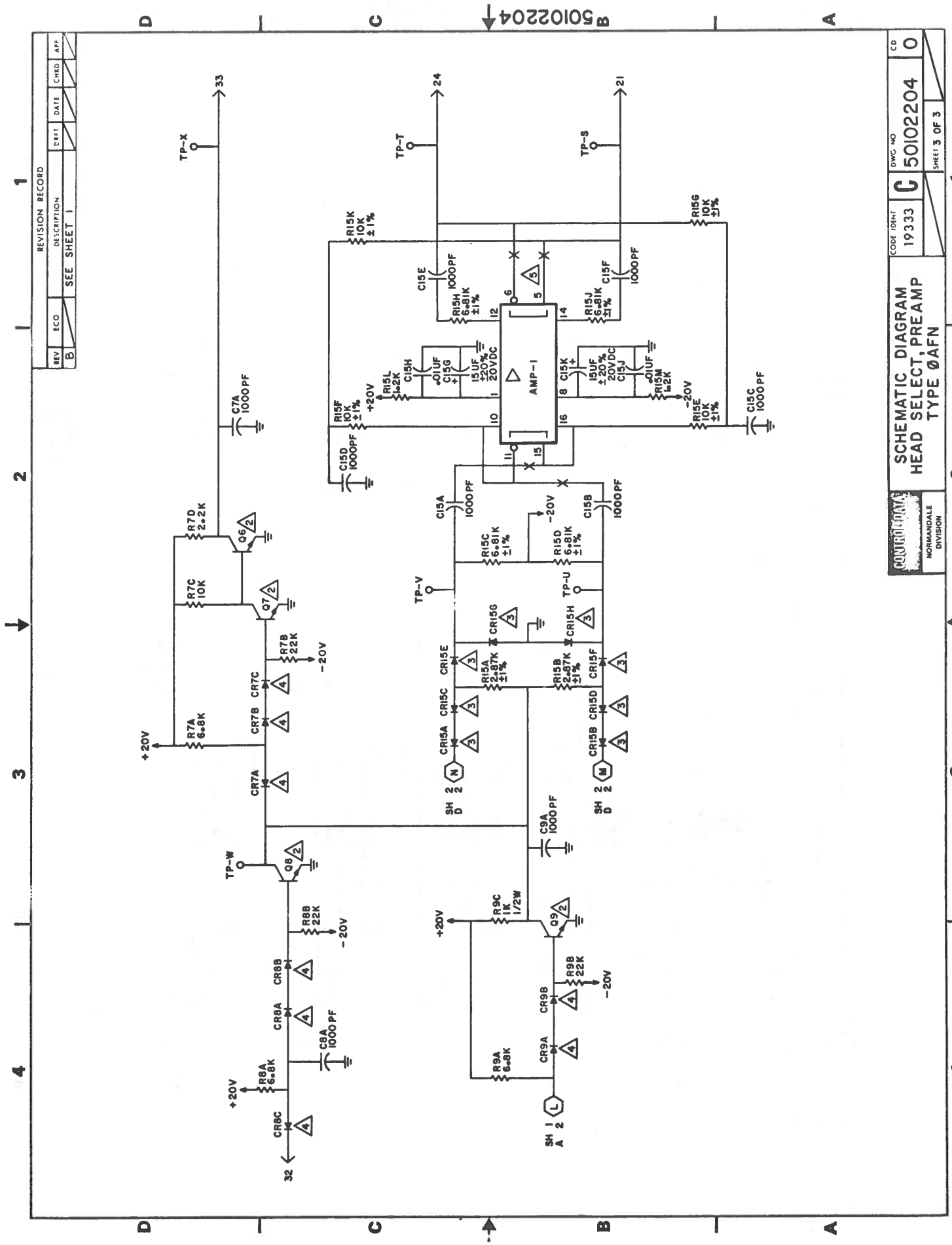
CONTROL DATA	POWER SUPPLY, PART 3 (SERIES CODE 17 AND ABOVE)	C DWG NO VCD-200	REV V
NORMANDALE DIVISION		CODE IDENT 19333	SHEET 6
			PAGE

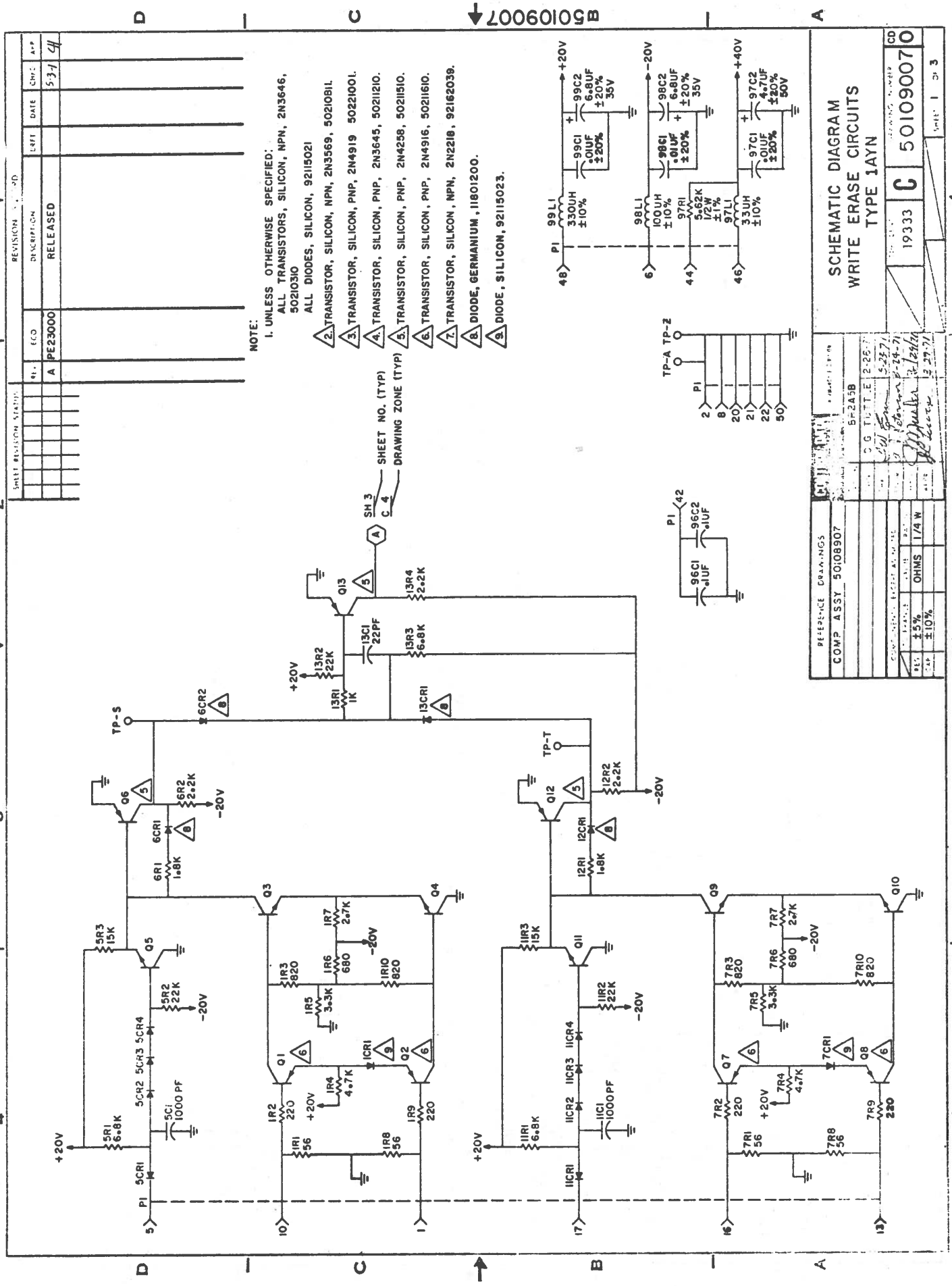
REVISION RECORD						
REV	ECO	DESCRIPTION	DRAFT	DATE	APP	APP
B		SEE SHEET 1				

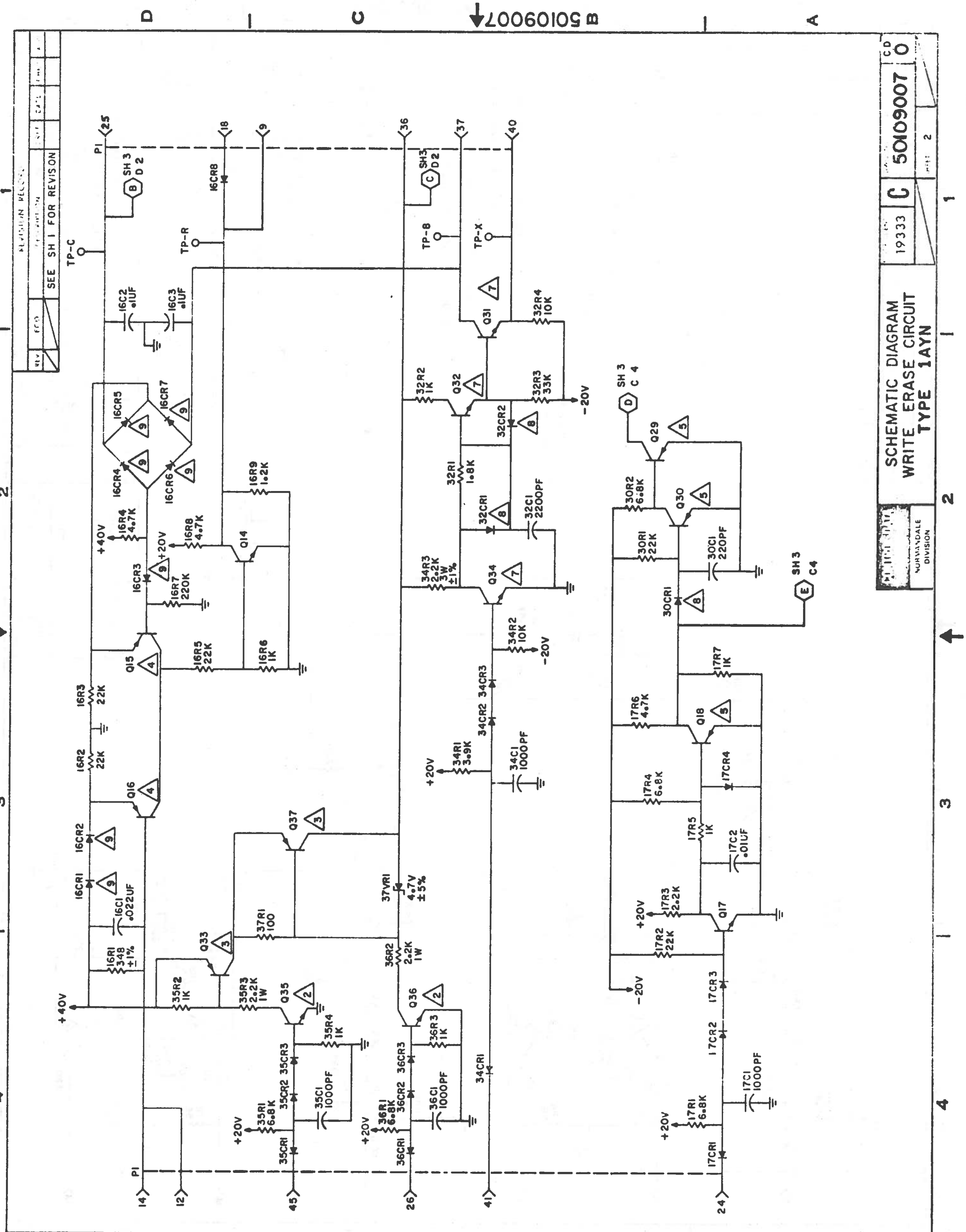


SCHEMATIC DIAGRAM HEAD SELECT, PREAMP TYPE ØAFN	19333	C	50102204	C.D. 0
			2 OF 3	

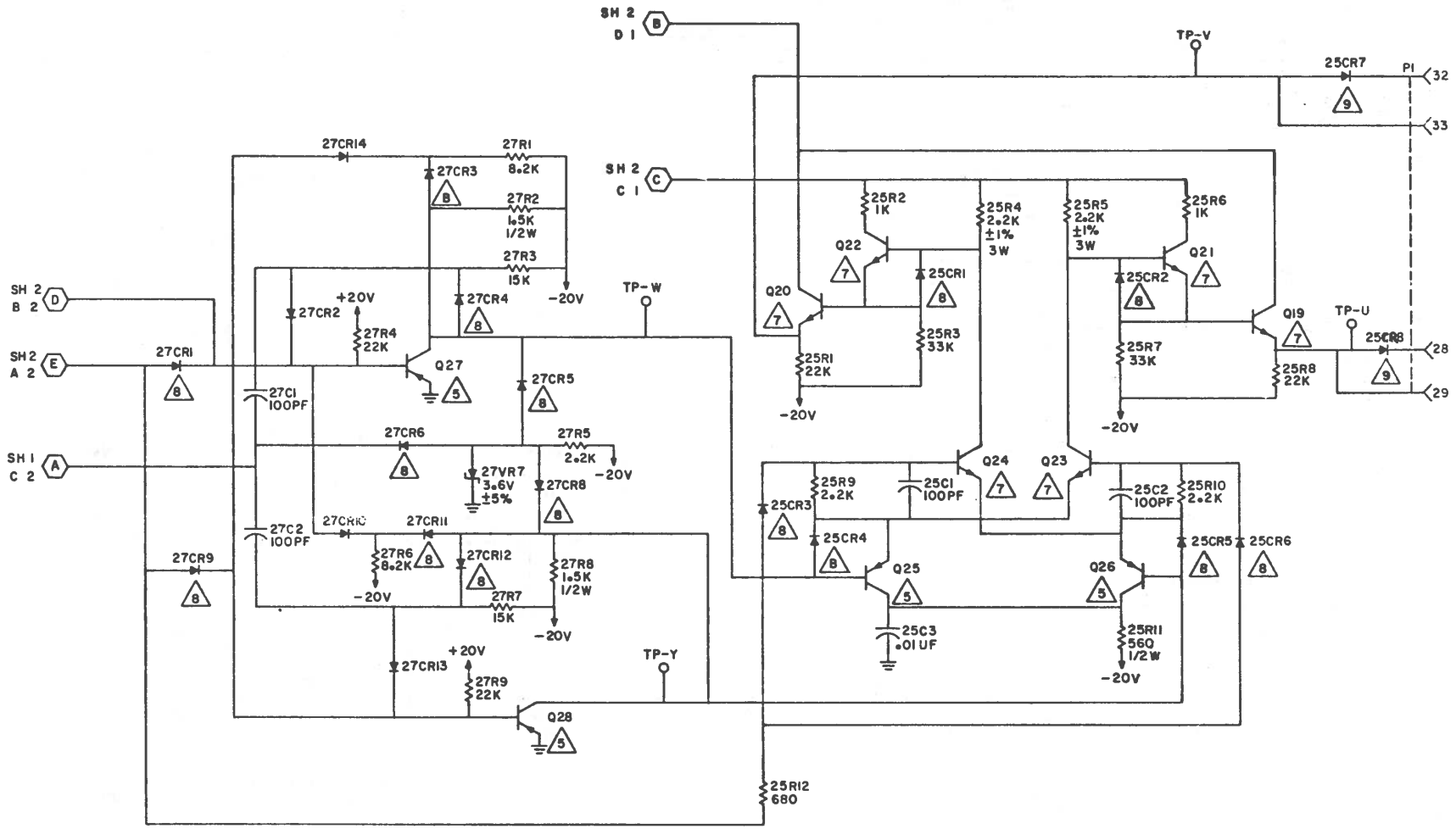
B 50102204


5010220 4
REVISION RECORD
REV
ECO
DESCRIPTION
DEFT
DATE
CHKD
APP
B
SEE SHEET 1
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
HEAD SELECT, PREAMP
TYPE ØAFN
CODE IDENT
19333
C
DWG NO
50102204
SHEET 3 OF 3
REV
0
AMP-1
TP-X
TP-T
TP-S
TP-V
TP-U
TP-W
+20V
-20V
R15K 10K ±1%
R15G 10K ±1%
R15H 6.81K ±1%
R15J 6.81K ±1%
R15L 1.2K
R15M 1.2K
R15F 10K ±1%
R15E 10K ±1%
C15E 1000PF
C15F 1000PF
C15H .01UF
C15G .15UF ±20% 20VDC
C15K .15UF ±20% 20VDC
C15J .01UF
C15D 1000PF
C15C 1000PF
C15A 1000 PF
C15B 1000PF
R15C 6.81K ±1%
R15D 6.81K ±1%
CR15G
CR15H
CR15E
CR15F
CR15C
CR15D
CR15A
CR15B
R15A 2.87K ±1%
R15B 2.87K ±1%
C7A 1000PF
R7D 2.2K
Q6
R7C 10K
Q7
R7B 22K
R7A 6.8K
CR7C
CR7B
CR7A
C9A 1000PF
Q8
R8B 22K
CR8B
CR8A
C8A 1000 PF
R8A 6.8K
CR8C
R9C 1K 1/2W
Q9
R9B 22K
CR9B
CR9A
R9A 6.8K
32
33
24
21
SH 2 D 2
SH 1 A 2


SCHEMATIC DIAGRAM
WRITE ERASE CIRCUITS
TYPE 1AYN
50109007
REVISION RECORD
DESCRIPTION
RELEASED
ECO
PE23000
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, SILICON, NPN, 2N3646, 50210310
ALL DIODES, SILICON, 92115021
2. TRANSISTOR, SILICON, NPN, 2N3569, 50210811
3. TRANSISTOR, SILICON, PNP, 2N4919 50221001.
4. TRANSISTOR, SILICON, PNP, 2N3645, 50211210.
5. TRANSISTOR, SILICON, PNP, 2N4258, 50211510.
6. TRANSISTOR, SILICON, PNP, 2N4916, 50211610.
7. TRANSISTOR, SILICON, NPN, 2N2218, 92162039.
8. DIODE, GERMANIUM, 11801200.
9. DIODE, SILICON, 92115023.
SHEET NO. (TYP)
DRAWING ZONE (TYP)
+20V
-20V
+40V
TP-S
TP-T
TP-A
COMP ASSY 50108907
19333
C
50109007
0


SCHEMATIC DIAGRAM
WRITE ERASE CIRCUIT
TYPE 1AYN
50109007
19333
C
SEE SH 1 FOR REVISON
NORMANDALE DIVISION

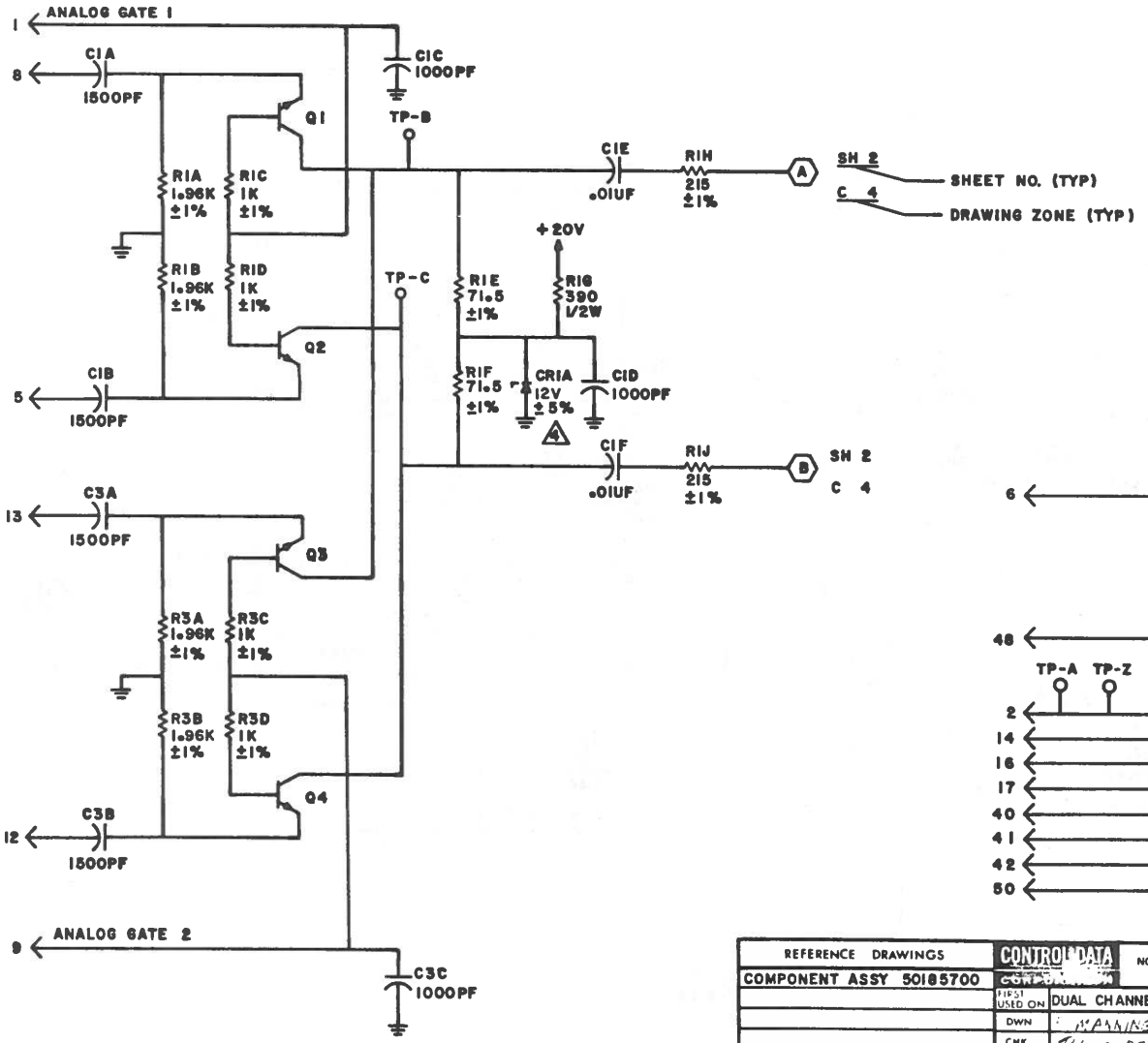
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHK	APP
		SEE SH 1 FOR REVISION				



SCHEMATIC DIAGRAM WRITE ERASE CIRCUIT TYPE 1AYN	19333	C	50109007	0
			SHT 3	

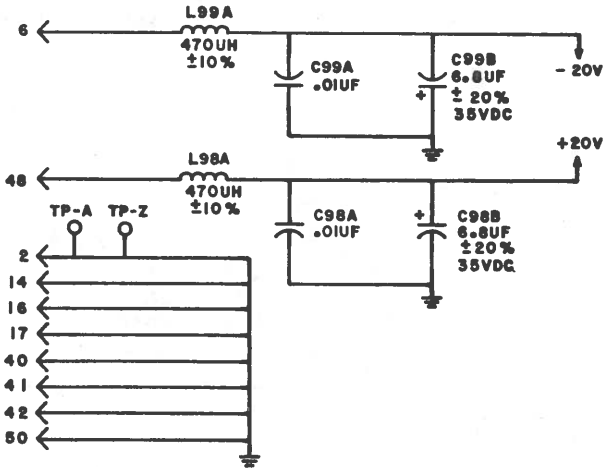
SHEET REVISION STATUS

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED		8/11/69		PH
B	PE29310 PE23000	DOC SIZE & SYM CHANGE	LB	6-4-71		



NOTE:

1. TRANSISTOR, SILICON, PNP, 2N4258, 50211500.
2. READ PREAMPLIFIER, TYPE AMP-1 EF 7400, 11644900
3. ALL OTHER TRANSISTORS, SILICON, NPN, 2N3646, 50210300.
4. DIODE, SILICON ZENER, 50240118
5. ALL OTHER DIODES, SILICON, 50241100



REFERENCE DRAWINGS
COMPONENT ASSY 50185700

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4W
CAP	± 10%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

	FIRST USED ON	DUAL CHANNEL RESOB	
DWN		MANNING	
CHK		[illegible] ECDS	4-21-69
ENGR		P Priest	8/4/69
MFG		J B Lewis	8-7-69
APPR		H E Amburg	6-11-69

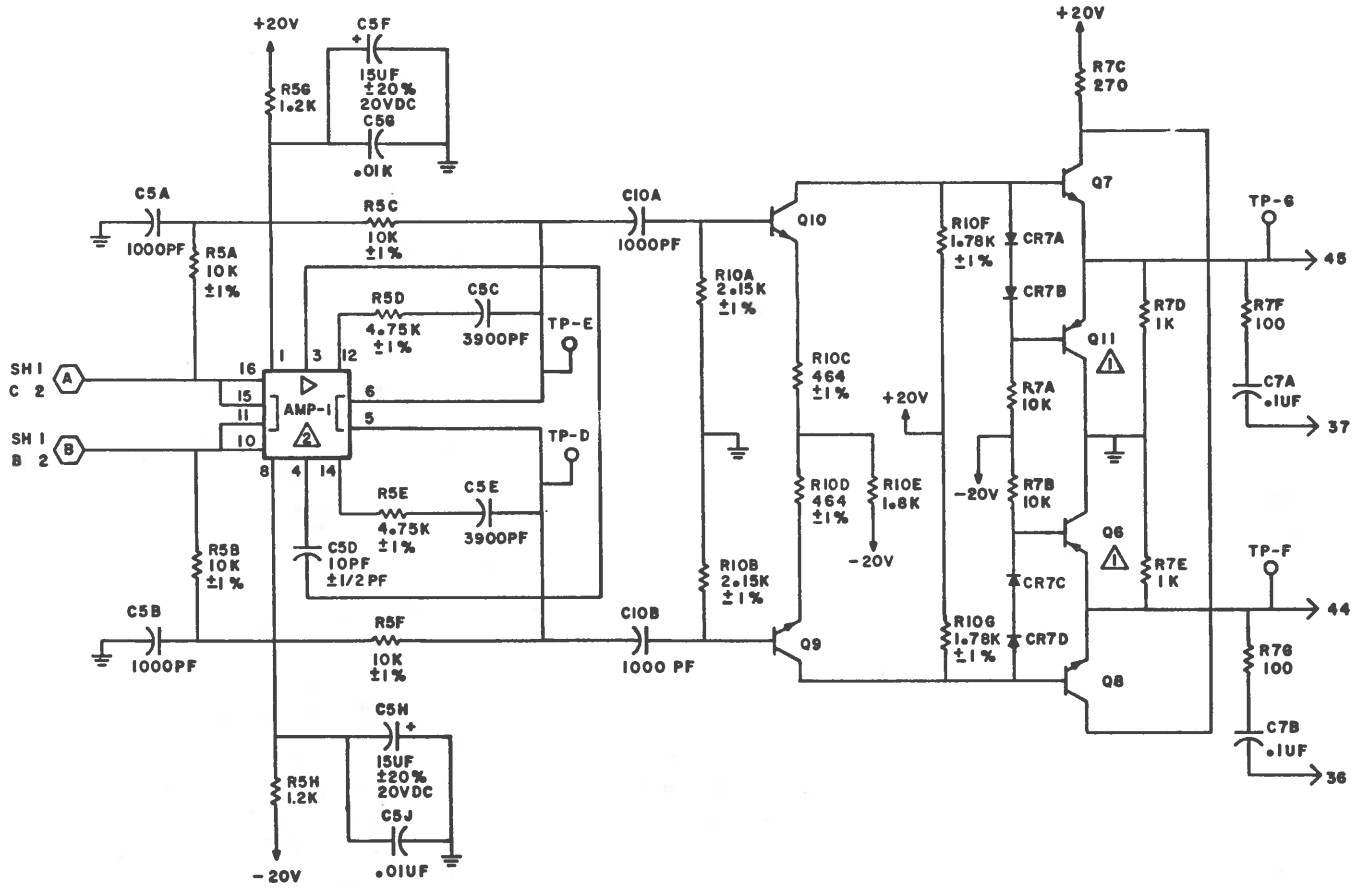
TITLE: SCHEMATIC DIAGRAM
ANALOG GATE AND AMPLIFIER
(IBM COMPATIBLE)
TYPE 9FQN

CODE IDENT		DRAWING NUMBER	
19333	C	50185800	5

SHEET 1 OF 2

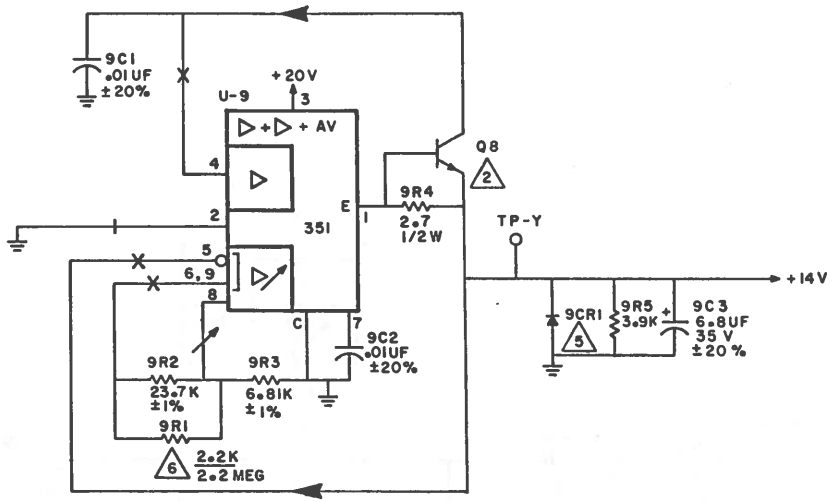
50185800 B

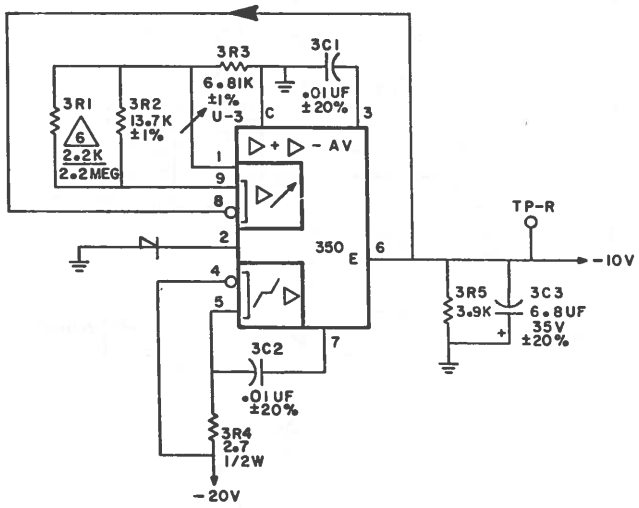
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHK	APP
B		SEE SH 1 FOR REVISIONS				

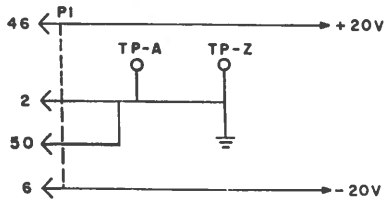


SCHEMATIC DIAGRAM ANALOG GATE AND AMPLIFIER (ISM COMPATIBLE) TYPE 9FQN		50185800	CD 5
		2	

SHEET REVISION STATUS	REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED			4-26-1	4H







NOTE:

1 UNLESS OTHERWISE SFECIFIED
ALL TRANSISTOR SPNP, 2N3645, 50211210.
ALL DIODES SILICON, 92115023.

△2 TRANSISTOR SNPN, 2N3646, 50210310.

△3 TRANSISTOR SNPN, 2N3569, 50210811

4 IC U2, TRANSISTOR ARRAY, HAS PIN 10 CONNECTED TO -10 V.

△5 DIODE GERMANIUM, 11801200.

△6 SEE 46325900 FOR SELECTION OF 9R1 AND 3R1.

REFERENCE DRAWINGS			
COMP ASSY 50189300			
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	5%	OHMS	1/4 W
CAP	±10%		

FIRST USED ON	BR2A1	
DWN	Streeter	4-5-71
CHK	W Fatum	4/14/71
ENGR	C Nelson	4/15/71
MFG	W Foster	4/22/71
APPR	W Fatum	4-26-71

NORMANDALE DIVISION

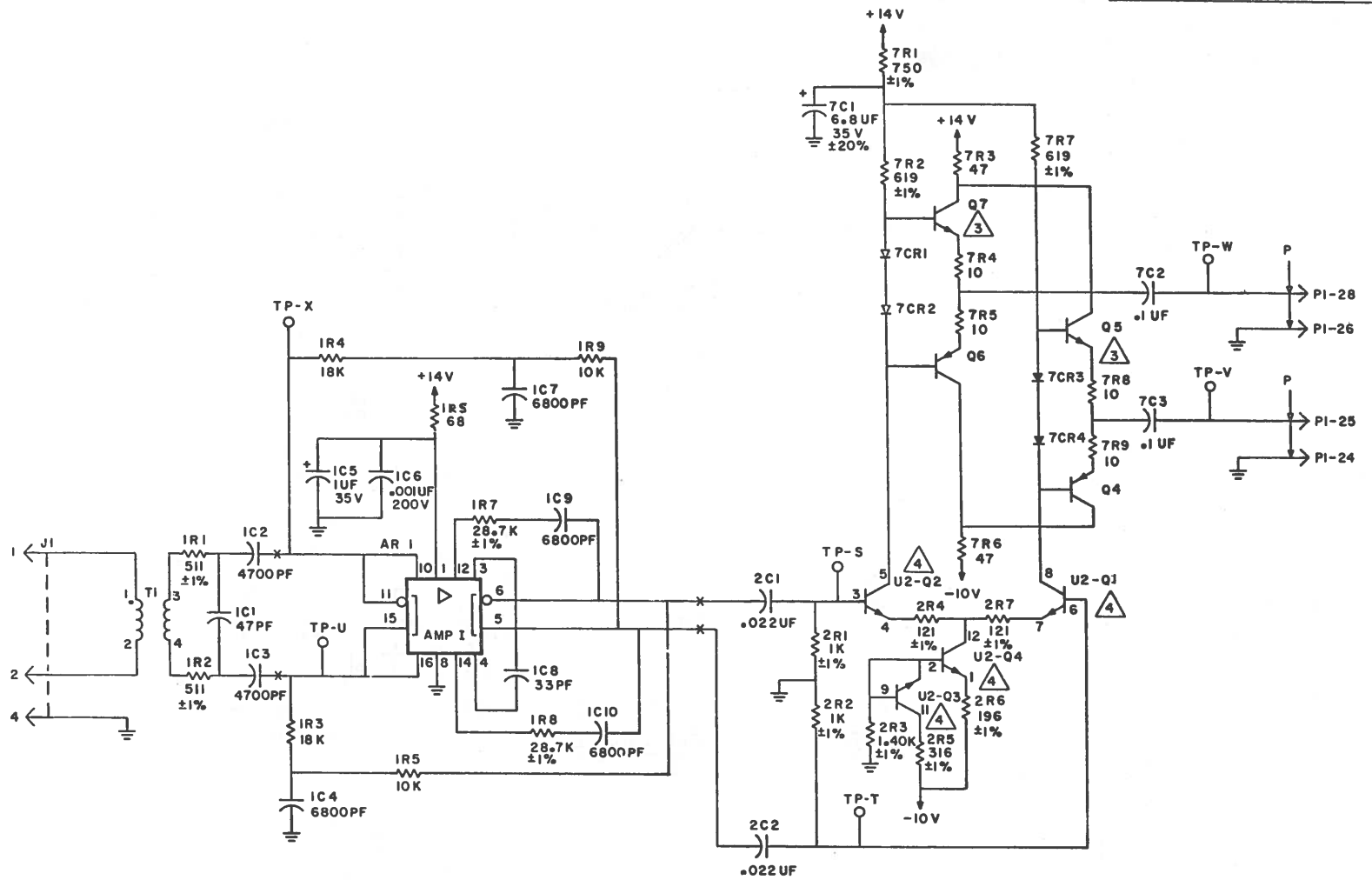
TITLE
SCHEMATIC DIAGRAM
PRE AMP
TRACK SERVO
TYPE ØFZN

CODE IDENT		DRAWING NUMBER	CD
19333	C	50189400	0

SHEET 1 OF 2

50189400 B

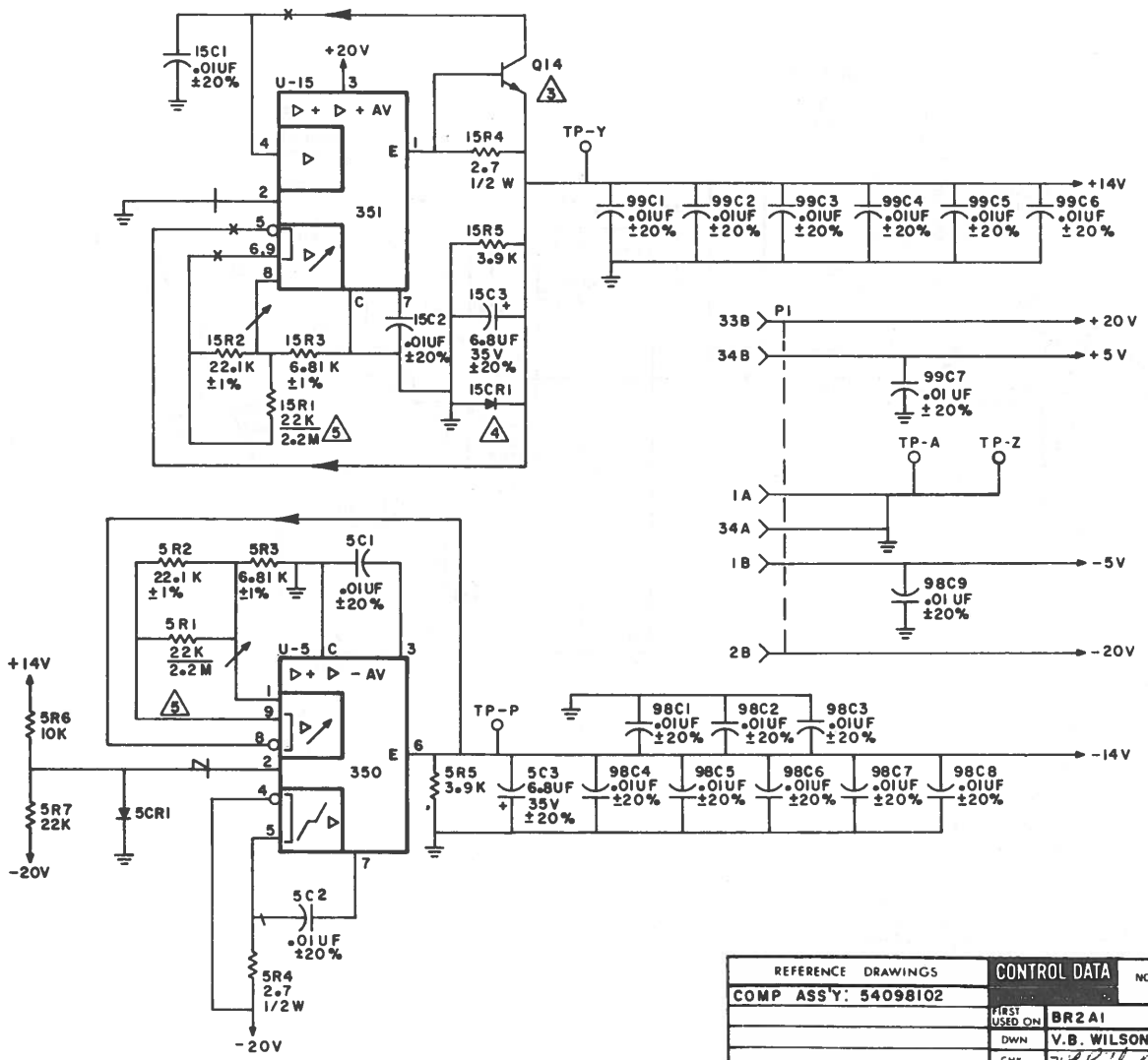
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHT 1 FOR REV				



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM PRE AMP TRACK SERVO TYPE ØFZN	CODE IDENT 19333	C	DWG NO 50189400	CD 0
				SHEET 2 OF 2	

50189400

SHEET REVISION STATUS	REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	-E-3300	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3569, 50210811.
   ALL FET'S, N CHANNEL JUNCTION, 2N4861, 50218100.
   ALL DIODES, SI, 92115023.
2. TRANSISTOR, SPNP, 2N4619, 50211610.
3. TRANSISTOR, SNPN, 2N3646, 50210310.
4. DIODE, GERMANIUM, 11801200
5. RESISTORS 5R1 AND 15R1 ARE SELECTED FROM 46325900.
6. ALL IC ELEMENT TYPE NO. 304 HAVE PINS 5 CONNECTED TO −14V AND PINS 8 CONNECTED TO +14V.
7. ALL IC ELEMENT TYPE NO. 300 AND 301 HAVE PINS 4 CONNECTED TO −14V AND PINS 7 CONNECTED TO +14V
8. IC 162 HAS PIN 7 CONNECTED TO GND, PIN 13 CONNECTED TO −5V AND PIN 14 CONNECTED TO +5V

REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION
COMP ASS'Y: 54098102	FIRST USED ON	BR2A1
	DWN	V.B. WILSON 1-28-74
	CHK	[illegible] 2-7-74
	ENGR	[illegible] 2-7-74
	MFG	[illegible] [illegible]
	APPR	[illegible] [illegible]

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

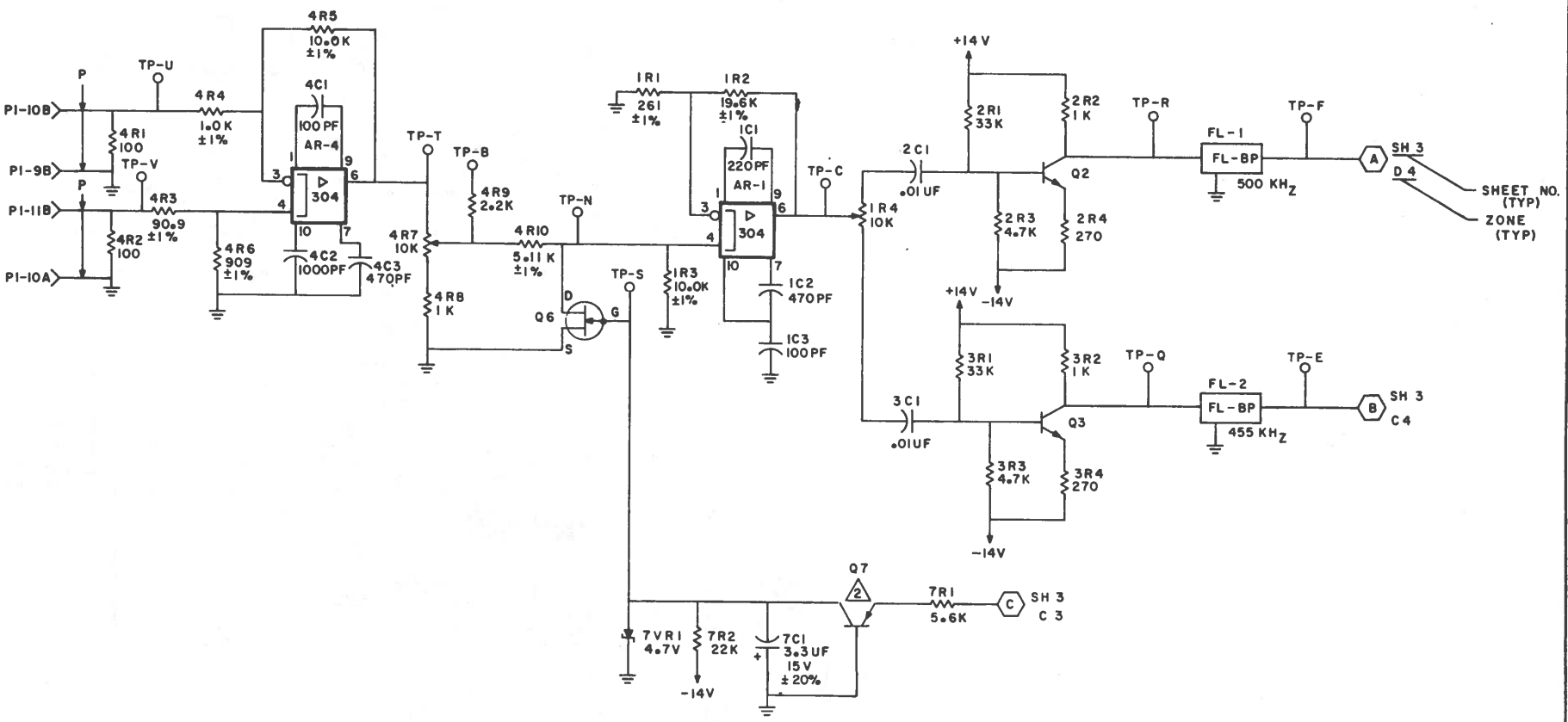
TITLE: SCHEMATIC DIAGRAM
TRACK SERVO FINE POSITION
TYPE 4AWV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54098202	2

SHEET 1 OF 3

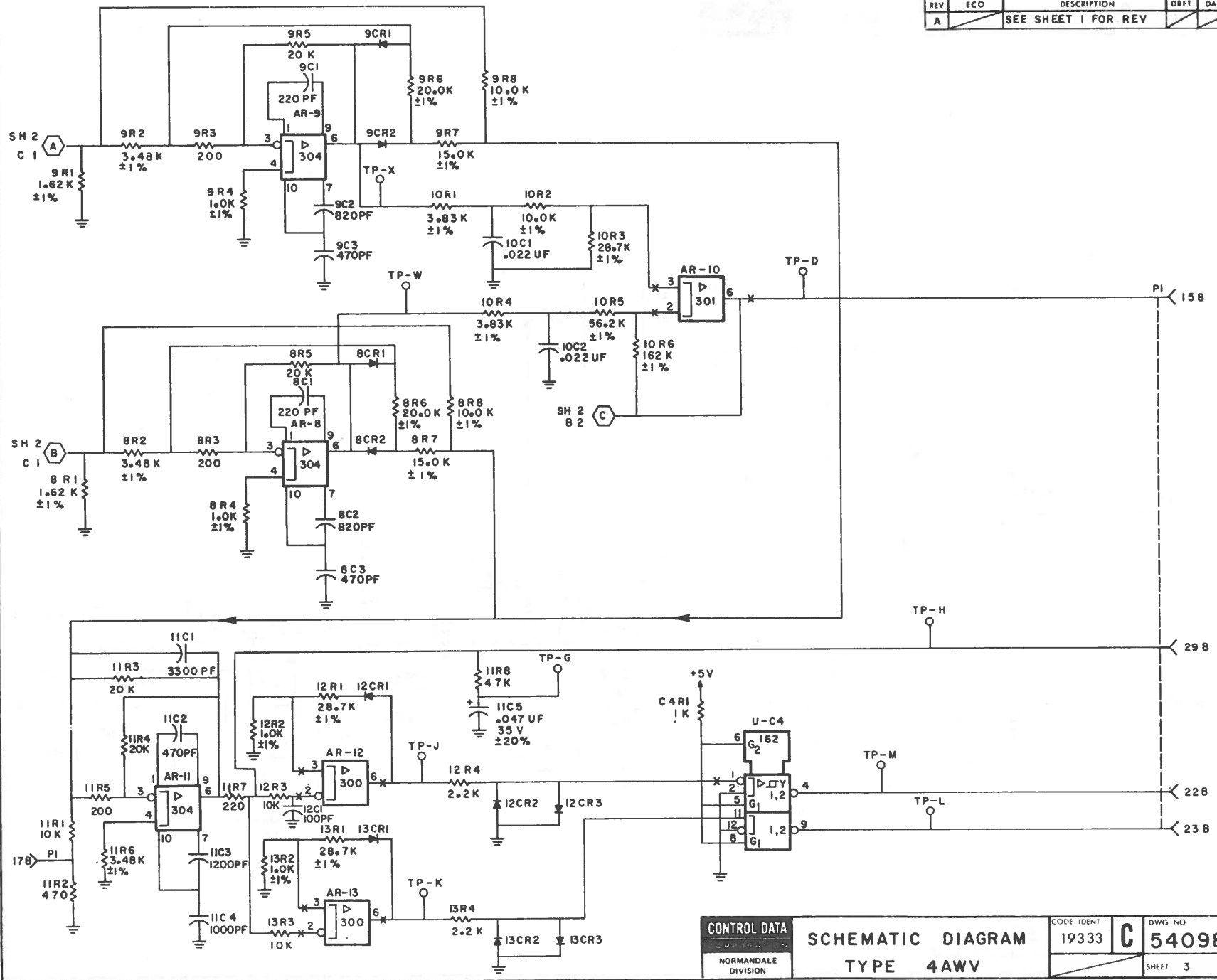
54098202 B

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



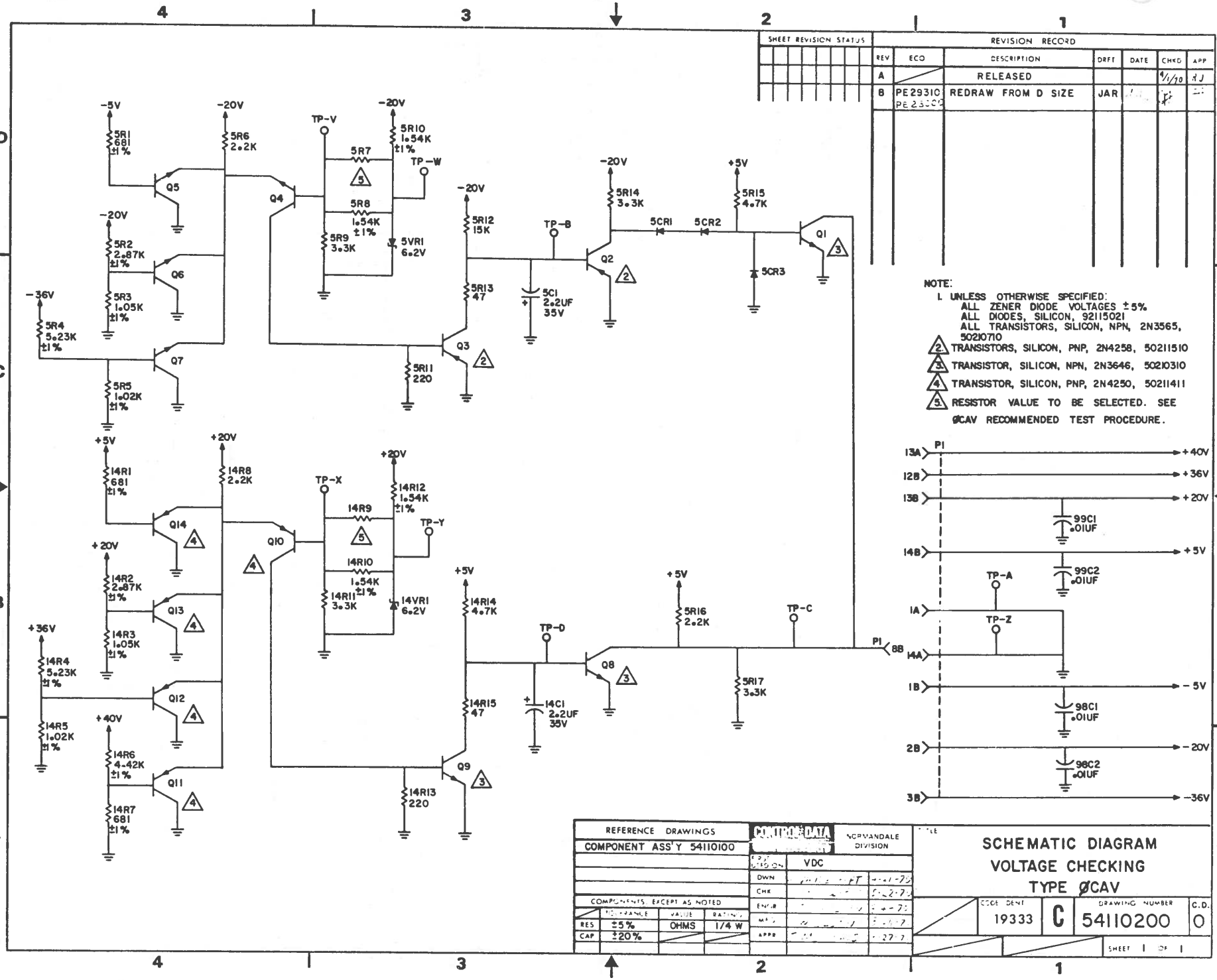
CONTROL DATA CORPORATION NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 4AWV	CODE IDENT 19333	C	DWG NO 54098202	CD 2
				SHEET 2	

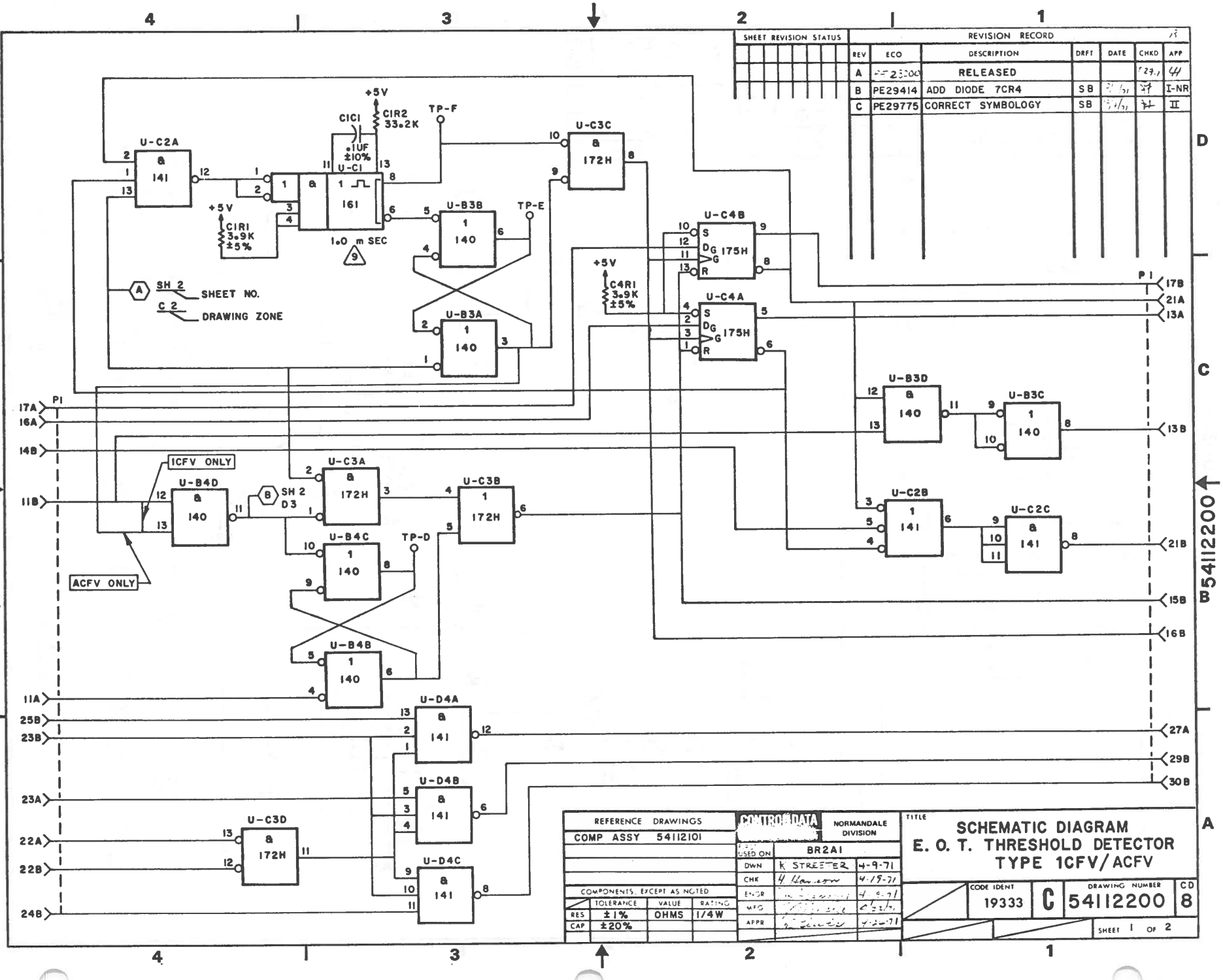
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



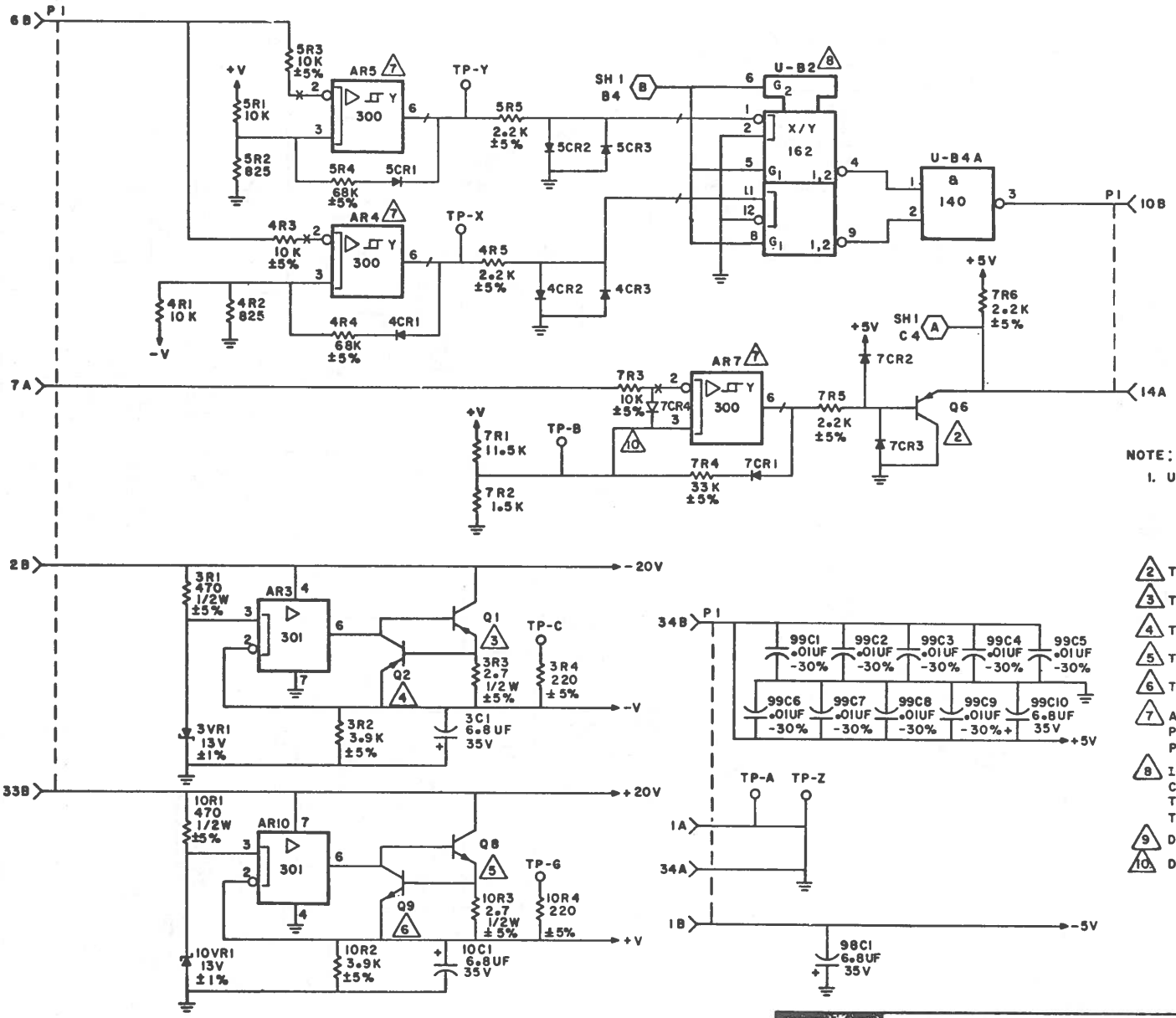
CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 4AWV	CODE IDENT 19333	C	DWG NO 54098202	CD 2
				SHEET 3	

B54098202


SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | | RELEASED | | | 4/1/70 | RJ
B | PE29310 PE23000 | REDRAW FROM D SIZE | JAR | | |
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL ZENER DIODE VOLTAGES ±5%
ALL DIODES, SILICON, 92115021
ALL TRANSISTORS, SILICON, NPN, 2N3565, 50210710
2. TRANSISTORS, SILICON, PNP, 2N4258, 50211510
3. TRANSISTOR, SILICON, NPN, 2N3646, 50210310
4. TRANSISTOR, SILICON, PNP, 2N4250, 50211411
5. RESISTOR VALUE TO BE SELECTED. SEE ØCAV RECOMMENDED TEST PROCEDURE.
-5V
-20V
-36V
+5V
+20V
+36V
+40V
TP-V
TP-W
TP-X
TP-Y
TP-A
TP-Z
TP-B
TP-C
TP-D
5R1 681 ±1%
5R2 2.87K ±1%
5R3 1.05K ±1%
5R4 5.23K ±1%
5R5 1.02K ±1%
5R6 2.2K
5R7
5R8 1.54K ±1%
5R9 3.3K
5R10 1.54K ±1%
5VR1 6.2V
5R11 220
5R12 15K
5R13 47
5C1 2.2UF 35V
5R14 3.3K
5R15 4.7K
5R16 2.2K
5R17 3.3K
5CR1
5CR2
5CR3
Q1
Q2
Q3
Q4
Q5
Q6
Q7
14R1 681 ±1%
14R2 2.87K ±1%
14R3 1.05K ±1%
14R4 5.23K ±1%
14R5 1.02K ±1%
14R6 4.42K ±1%
14R7 681 ±1%
14R8 2.2K
14R9
14R10 1.54K ±1%
14R11 3.3K
14VR1 6.2V
14R12 1.54K ±1%
14R13 220
14C1 2.2UF 35V
14R14 4.7K
14R15 47
Q8
Q9
Q10
Q11
Q12
Q13
Q14
P1
13A
12B
13B
14B
1A
14A
1B
2B
3B
99C1 .01UF
99C2 .01UF
98C1 .01UF
98C2 .01UF
REFERENCE DRAWINGS
COMPONENT ASS'Y 54110100
CONTROL DATA
NORWANDALE DIVISION
VDC
DWN
CHK
ENGR
MFG
APPR
COMPONENTS EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ±5% | OHMS | 1/4 W
CAP ±20%
SCHEMATIC DIAGRAM
VOLTAGE CHECKING
TYPE ØCAV
CODE IDENT 19333
C
54110200
DRAWING NUMBER
C.D. 0
SHEET 1 OF 1


SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | PE23000 | RELEASED | | | 7-29-71 | 4H
B | PE29414 | ADD DIODE 7CR4 | SB | 9-1-71 | 9-1 | I-NR
C | PE29775 | CORRECT SYMBOLOGY | SB | 9-7-71 | 9-7 | II
+5V
C1C1
.1UF ±10%
C1R2 33.2K
TP-F
U-C2A
U-C1
U-C3C
U-B3B
TP-E
U-C4B
C1R1 3.9K ±5%
1.0 m SEC
U-B3A
U-C4A
C4R1 3.9K ±5%
A SH 2 SHEET NO.
C 2 DRAWING ZONE
P1
17B
21A
13A
U-B3D
U-B3C
13B
17A
16A
14B
1CFV ONLY
U-B4D
B SH 2 D3
U-C3A
U-C3B
U-C2B
U-C2C
11B
U-B4C
TP-D
ACFV ONLY
21B
15B
16B
U-B4B
11A
25B
23B
U-D4A
27A
29B
30B
23A
U-D4B
22A
22B
U-C3D
U-D4C
24B
REFERENCE DRAWINGS
COMP ASSY 54112101
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ±1% | OHMS | 1/4W
CAP ±20%
CONTROL DATA NORMANDALE DIVISION
USED ON BR2A1
DWN K STREETER 4-9-71
CHK H Hanson 4-19-71
ENGR 4-9-71
MFG 4-22-71
APPR 4-22-71
TITLE
SCHEMATIC DIAGRAM
E. O. T. THRESHOLD DETECTOR
TYPE 1CFV/ACFV
CODE IDENT 19333
C
DRAWING NUMBER 54112200
CD 8
SHEET 1 OF 2
54112200 B

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHK	APP
C		SEE SHT 1 FOR REV				



NOTE:

1. UNLESS OTHERWISE SPECIFIED
   ALL DIODES, SILICON, 92115021
   ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5 VOLTS.

(2) TRANSISTOR, SPNP, 2N4258, 50211510

(3) TRANSISTOR, SPNP, 2N3645, 50211210

(4) TRANSISTOR, SPNP, 2N4916, 50211610

(5) TRANSISTOR, SNPN, 2N3569, 50210811

(6) TRANSISTOR, SNPN, 2N3646, 50210310

(7) ALL I-C ELEMENT TYPE NO. 300 HAVE PIN 4 CONNECTED TO −VOLTAGE AND PIN 7 CONNECTED TO + VOLTAGE

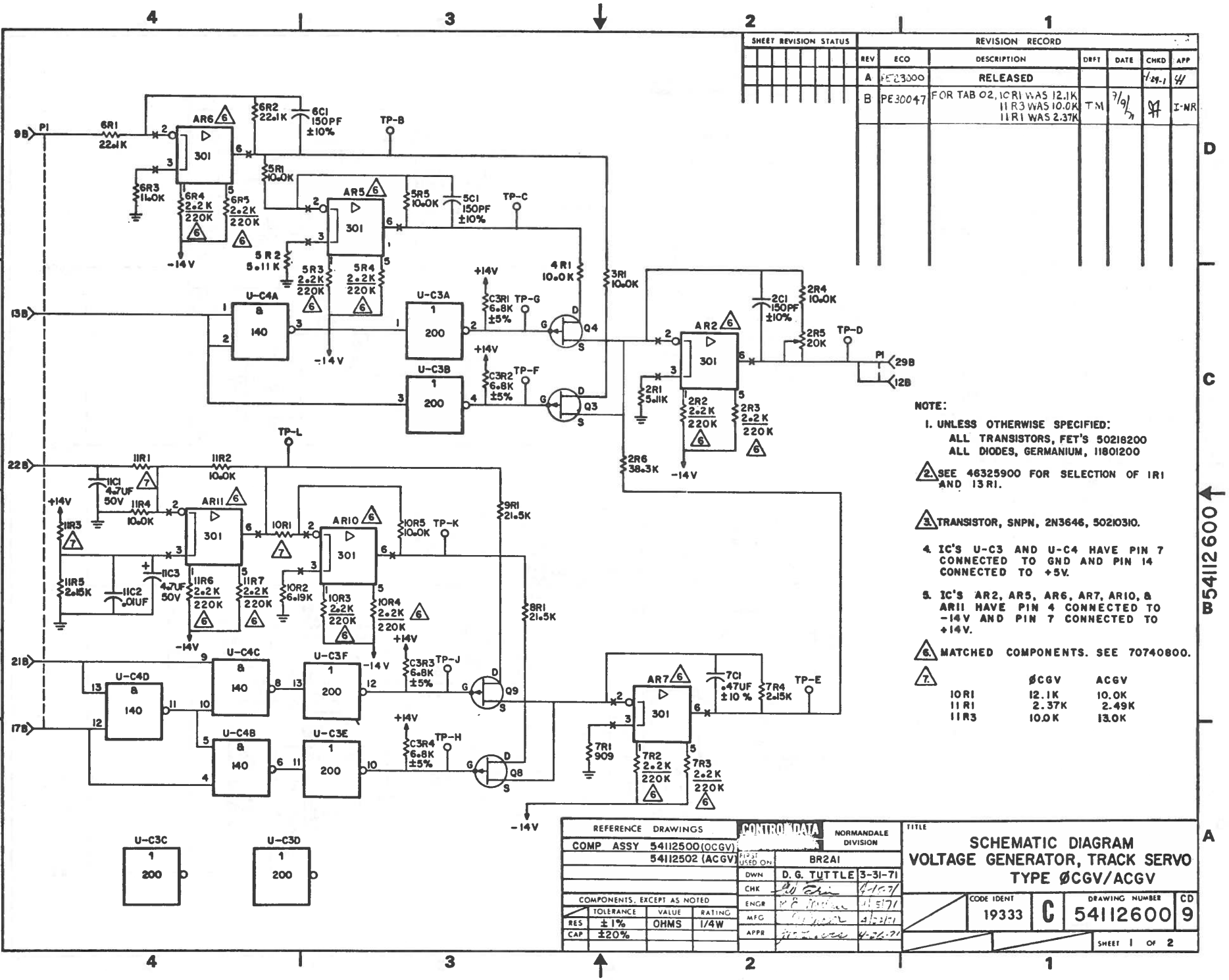
(8) I-C ELEMENT NO. 162 HAS PIN 7 CONNECTED TO GND, PIN 13 CONNECTED TO −5 VOLTS AND PIN 14 CONNECTED TO +5 VOLTS

(9) DELAY TIME FOR REFERENCE ONLY

(10) DIODE REMOVED ON ICFV.

CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM E. O. T. THRESHOLD DET TYPE 1CFV/ACFV	CODE IDENT 19333	C	DWG NO 54112200	CD 8
				SHEET 2	

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED			4/29-1	
	B	PE30047	FOR TAB 02, 10R1 WAS 12.1K 11R3 WAS 10.0K 11R1 WAS 2.37K	TM	7/9/71		I-NR



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, FET'S 50218200
   ALL DIODES, GERMANIUM, 11801200
2. SEE 46325900 FOR SELECTION OF 1R1 AND 13R1.
3. TRANSISTOR, SNPN, 2N3646, 50210310.
4. IC'S U-C3 AND U-C4 HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
5. IC'S AR2, AR5, AR6, AR7, AR10, & AR11 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
6. MATCHED COMPONENTS. SEE 70740800.
7.

	ØCGV	ACGV
10R1	12.1K	10.0K
11R1	2.37K	2.49K
11R3	10.0K	13.0K

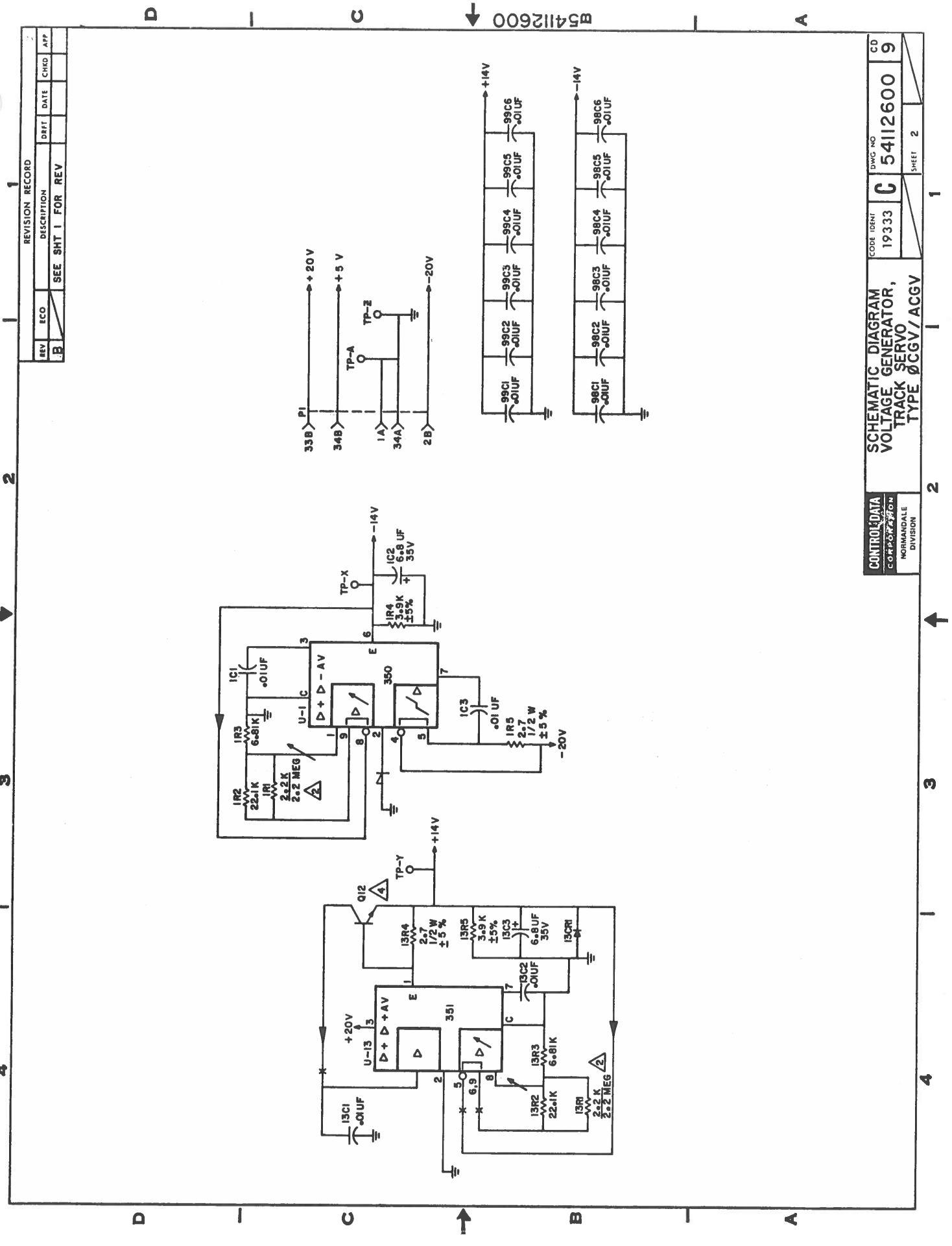
REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION
COMP ASSY 54112500 (ØCGV)	FIRST USED ON	BR2AI
54112502 (ACGV)	DWN	D. G. TUTTLE 3-31-71
	CHK	4-1-71
COMPONENTS, EXCEPT AS NOTED	ENGR	4-5-71
TOLERANCE / VALUE / RATING	MFG	4-21-71
RES ±1% OHMS 1/4W	APPR	4-26-71
CAP ±20%		

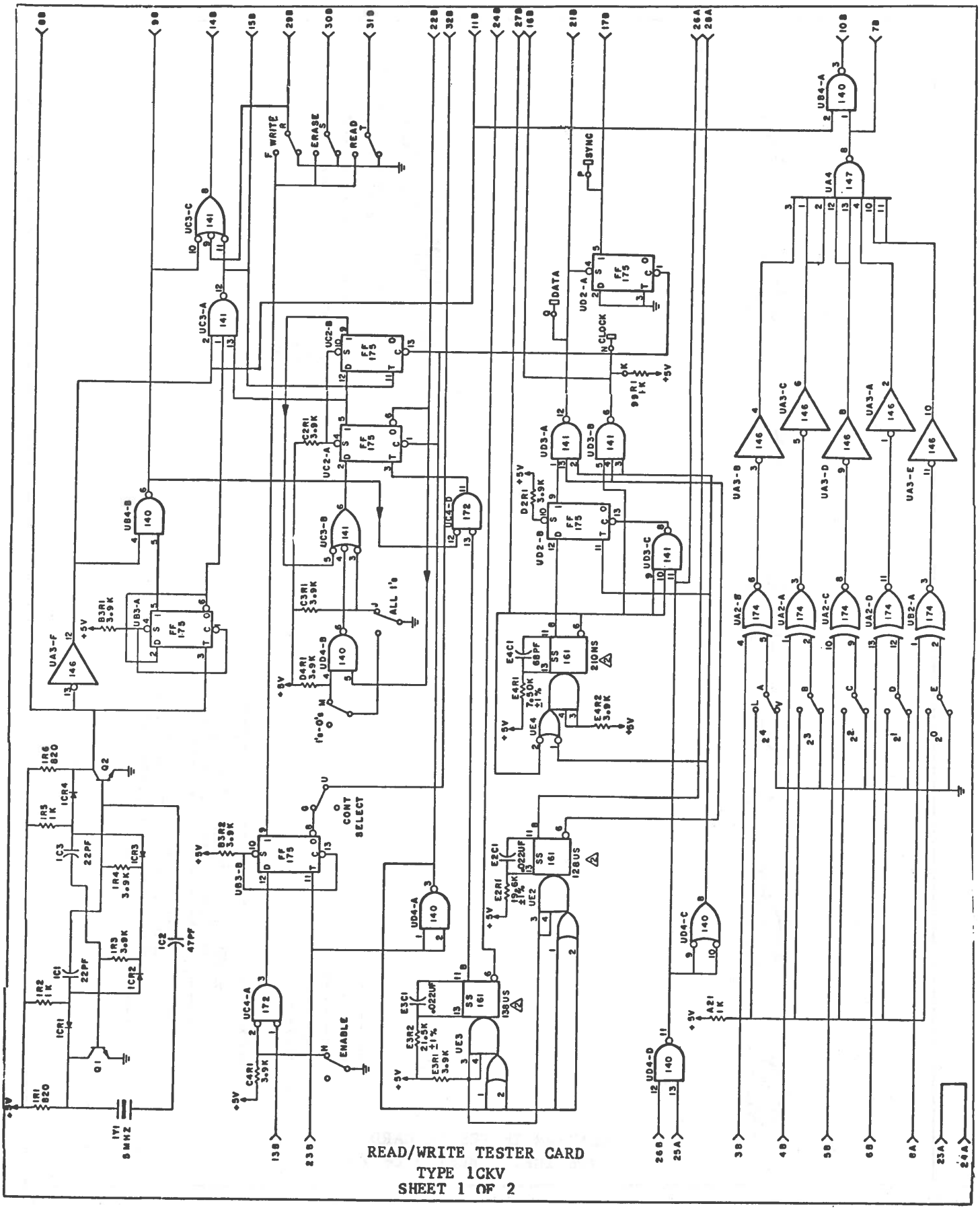
TITLE
SCHEMATIC DIAGRAM
VOLTAGE GENERATOR, TRACK SERVO
TYPE ØCGV/ACGV

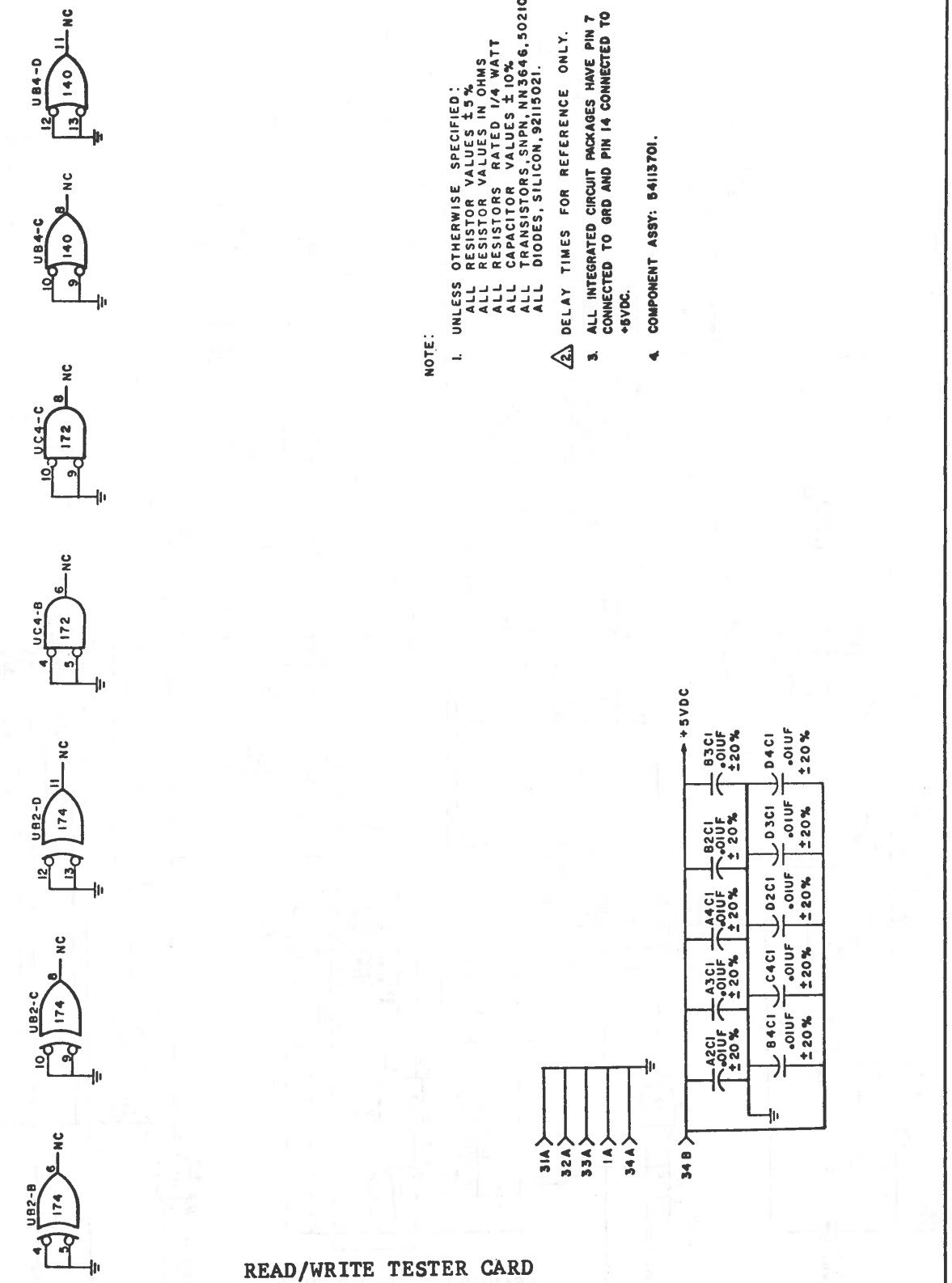
CODE IDENT		DRAWING NUMBER	CD
19333	C	54112600	9

SHEET 1 OF 2

B 54112600


REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
B
SEE SHT 1 FOR REV
SCHEMATIC DIAGRAM
VOLTAGE GENERATOR,
TRACK SERVO
TYPE ØCGV/ACGV
CONTROL DATA CORPORATION
NORMANDALE DIVISION
CODE IDENT
19333
C
DWG NO
54112600
SHEET 2
CD
9
54112600 B
+20 V
+5 V
-20V
+14V
-14V
TP-A
TP-B
TP-X
TP-Y
P1
33B
34B
1A
34A
2B
99C1 .01UF
99C2 .01UF
99C3 .01UF
99C4 .01UF
99C5 .01UF
99C6 .01UF
98C1 .01UF
98C2 .01UF
98C3 .01UF
98C4 .01UF
98C5 .01UF
98C6 .01UF
IC1 .01UF
IC2 6.8 UF 35V
IC3 .01 UF
IR1 2.2K 2.2 MEG
IR2 22.1K
IR3 6.81K
IR4 3.9K ±5%
IR5 2.7 1/2 W ±5%
U-1
350
13C1 .01UF
13C2 .01UF
13C3 6.8UF 35V
13CR1
13R1 2.2 K 2.2 MEG
13R2 22.1K
13R3 6.81K
13R4 2.7 1/2 W ±5%
13R5 3.9 K ±5%
U-13
351
Q12


WRITE
ERASE
READ
SYNC
DATA
CLOCK
ALL 1's
ALL 0's
CONT SELECT
ENABLE
1V1 8 MHZ
128US
138US
210NS
READ/WRITE TESTER CARD
TYPE 1CKV
SHEET 1 OF 2



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTOR VALUES ±5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT
   ALL CAPACITOR VALUES ±10%
   ALL TRANSISTORS, SNPN, NN3646, 50210310.
   ALL DIODES, SILICON, 92115021.
2. DELAY TIMES FOR REFERENCE ONLY.
3. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5VDC.
4. COMPONENT ASSY: 54113701.

READ/WRITE TESTER CARD
TYPE 1CKV (SHEET 2 OF 2)

REVISION RECORD						
REV	E.C.	DESCRIPTION	SHT	DATE	CHK	APP
A		RELEASED			9/4/70	RJ
B	PE29310 PE23000	REDRAW FROM D SIZE	JR	11/11	H	H

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTOR, SILICON NPN 2N3646, 50210310
   ALL DIODES, SILICON 24553500

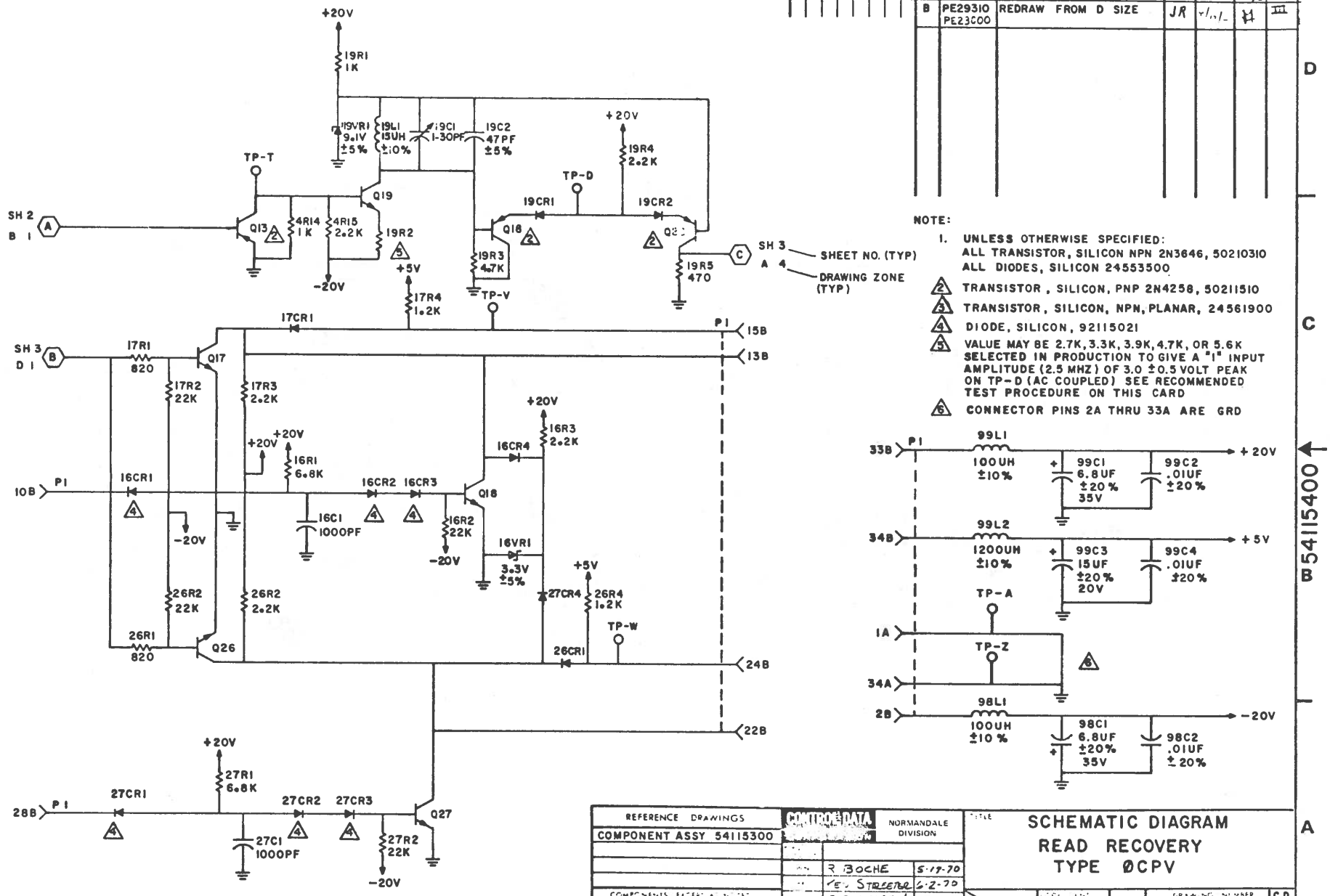
(2) TRANSISTOR, SILICON, PNP 2N4258, 50211510

(3) TRANSISTOR, SILICON, NPN, PLANAR, 24561900

(4) DIODE, SILICON, 9211502I

(5) VALUE MAY BE 2.7K, 3.3K, 3.9K, 4.7K, OR 5.6K SELECTED IN PRODUCTION TO GIVE A "1" INPUT AMPLITUDE (2.5 MHZ) OF 3.0 ±0.5 VOLT PEAK ON TP-D (AC COUPLED). SEE RECOMMENDED TEST PROCEDURE ON THIS CARD

(6) CONNECTOR PINS 2A THRU 33A ARE GRD



REFERENCE DRAWINGS	
COMPONENT ASSY 54115300	

COMPONENTS EXCEPT AS NOTED			
	TOLERANCE		RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA — NORMANDALE DIVISION

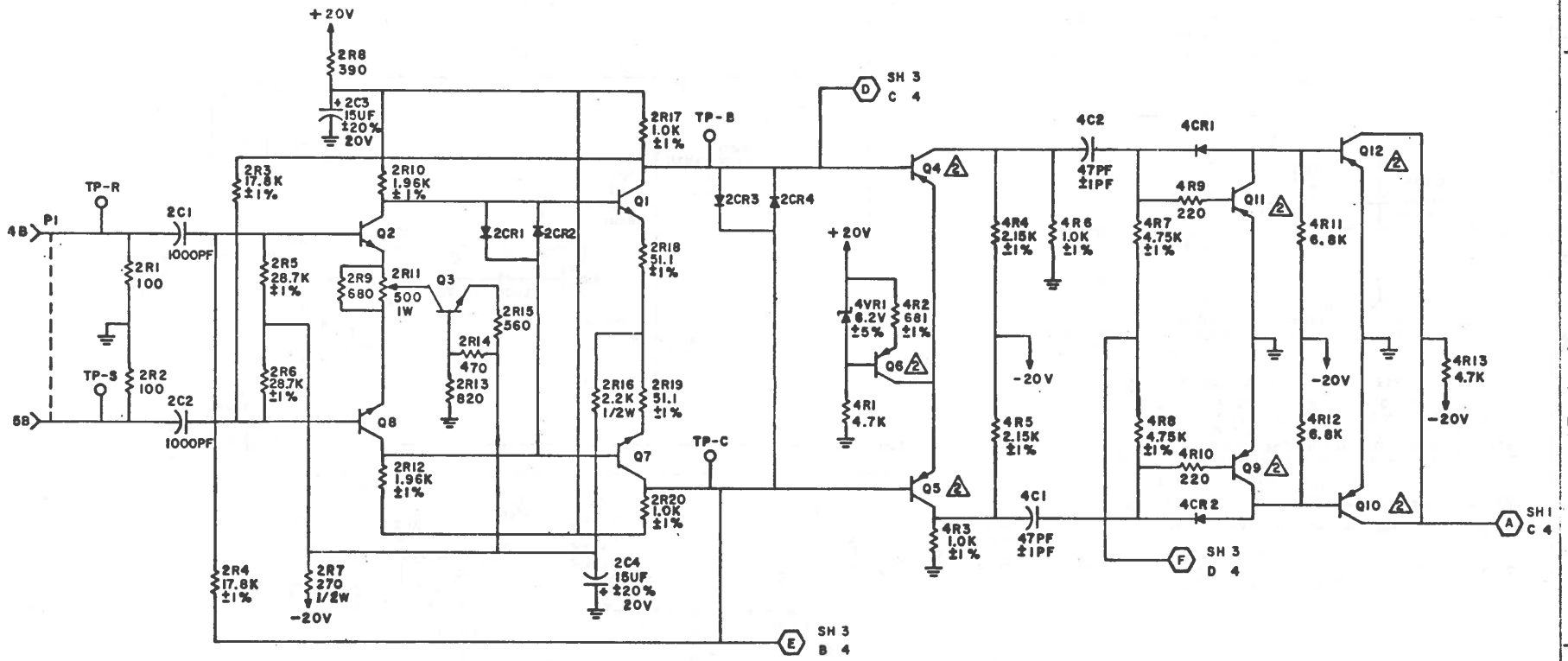
DRN	R BOCHE	5-19-70
CHK	E. STREETER	6-2-70
ENGR	RJ NIELSEN	7-27-70
MFG	SW OLSON	8-13-70
APPD	T McDONALD	9-3-70

TITLE: SCHEMATIC DIAGRAM
READ RECOVERY
TYPE ØCPV

CONT. NUMBER	DRAWING NUMBER	C.D.
19333	C 54115400	1

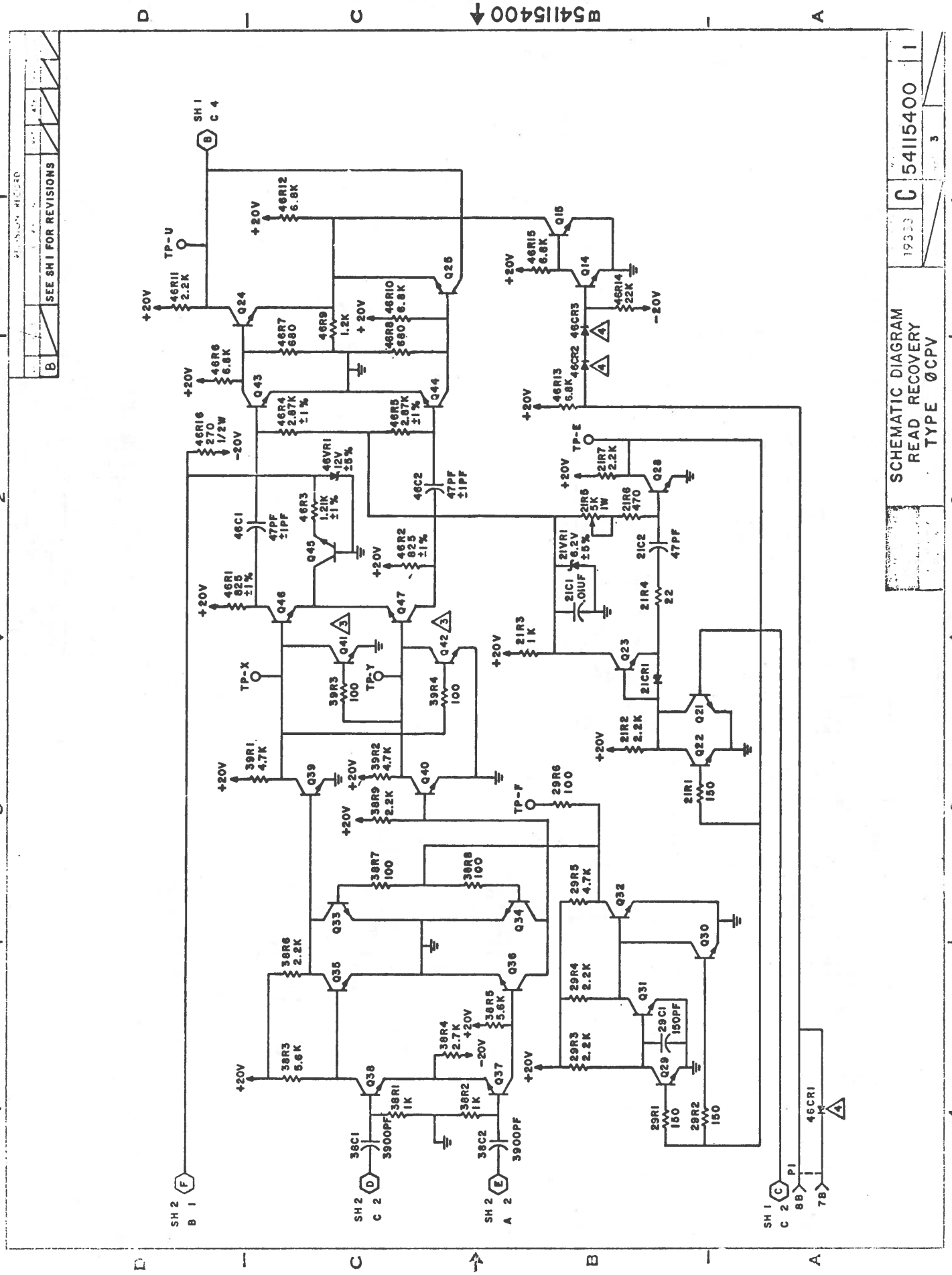
SHEET 1 OF 3

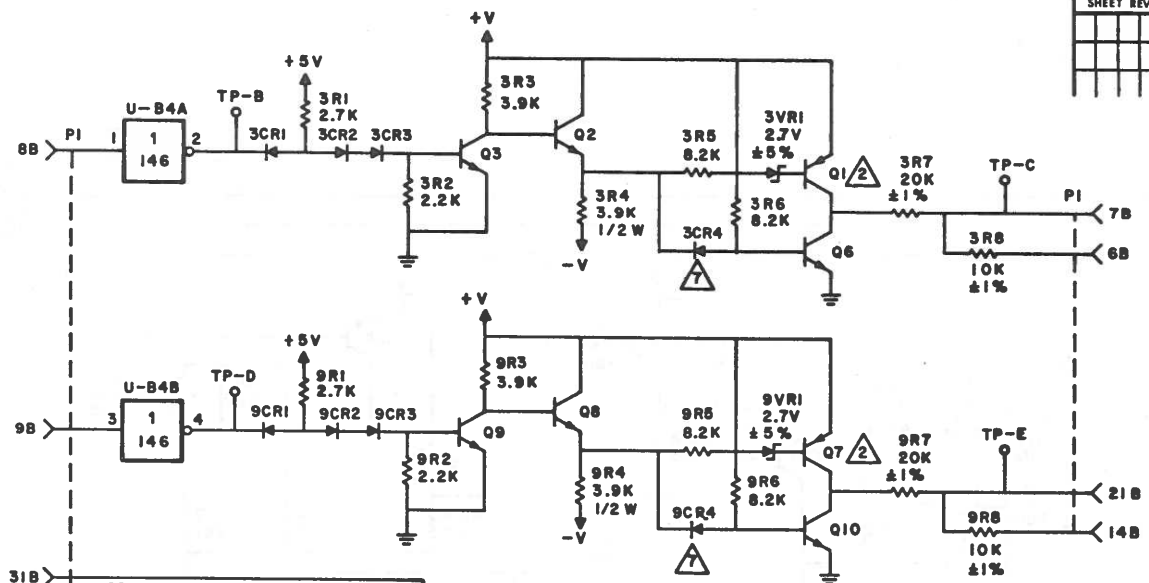
B SEE SH1 FOR REVISION



SCHEMATIC DIAGRAM
READ RECOVERY
TYPE ØCPV

19333 C 54115400 CD 1
2


SCHEMATIC DIAGRAM
READ RECOVERY
TYPE ØCPV
C 54115400
SEE SH 1 FOR REVISIONS
54115400



SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED			8/31/70	RA
B	PE21812	28VRI AND 5VRI WERE 5% ASSY NO. WAS 54116500.	DM	12/4/70	CAC	INR
C	PE29310 PE23000	DOC SIZE & SYM CHANGE	KB	6/14/71		III

NOTE:

1. UNLESS OTHERWISE SPECIFIED
   ALL TRANSISTORS SNPN, 2N3642, 50210510.
   ALL DIODES SILICON, 92115023
2. TRANSISTOR SILICON, PNP, 2N3638, 50210610.
3. TRANSISTOR SILICON, PNP, 2N4406, 50221500.
4. TRANSISTOR SILICON, NPN, 2N4922, 50220901.
5. TRANSISTOR SILICON, NPN, 2N3020, 50211900.
6. TRANSISTOR SILICON, PNP, 2N4919, 50221001.
7. DIODE GERMANIUM, 11801200.
8. ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GRD AND PIN 14 TO +5V
9. +V = +14.3V
   -V = -14.3V

REFERENCE DRAWINGS	
COMPONENT ASSY 54116501	

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	±10%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	VCD	
DWN	A. MARTIN	5-20-70
CHK	D. RADCLIFF	6-17-70
ENGR	R.E. McCANN	6-5-70
MFG	S.W. OLSON	6-26-70
APPR	T.M. DONALD	8-27-70

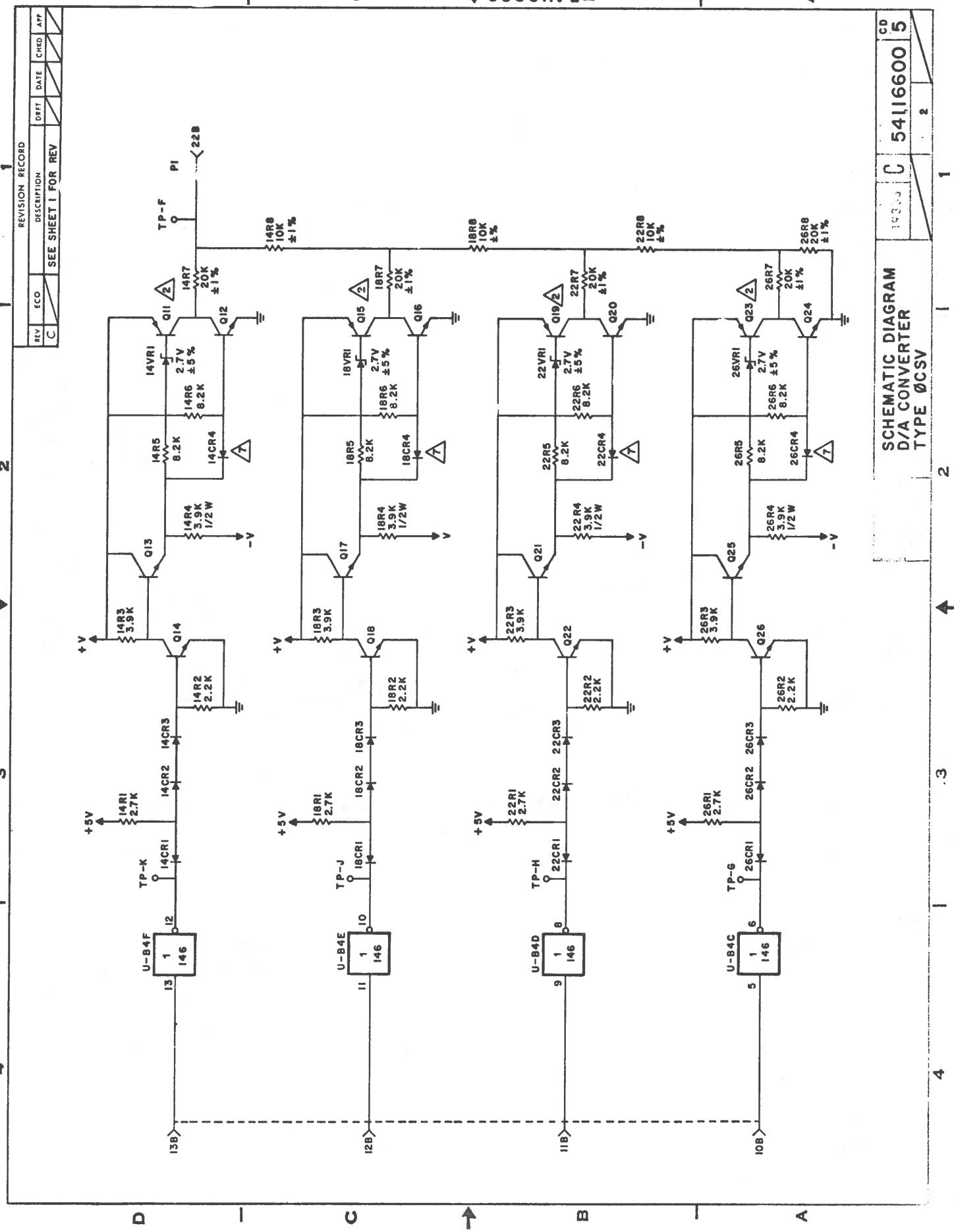
TITLE

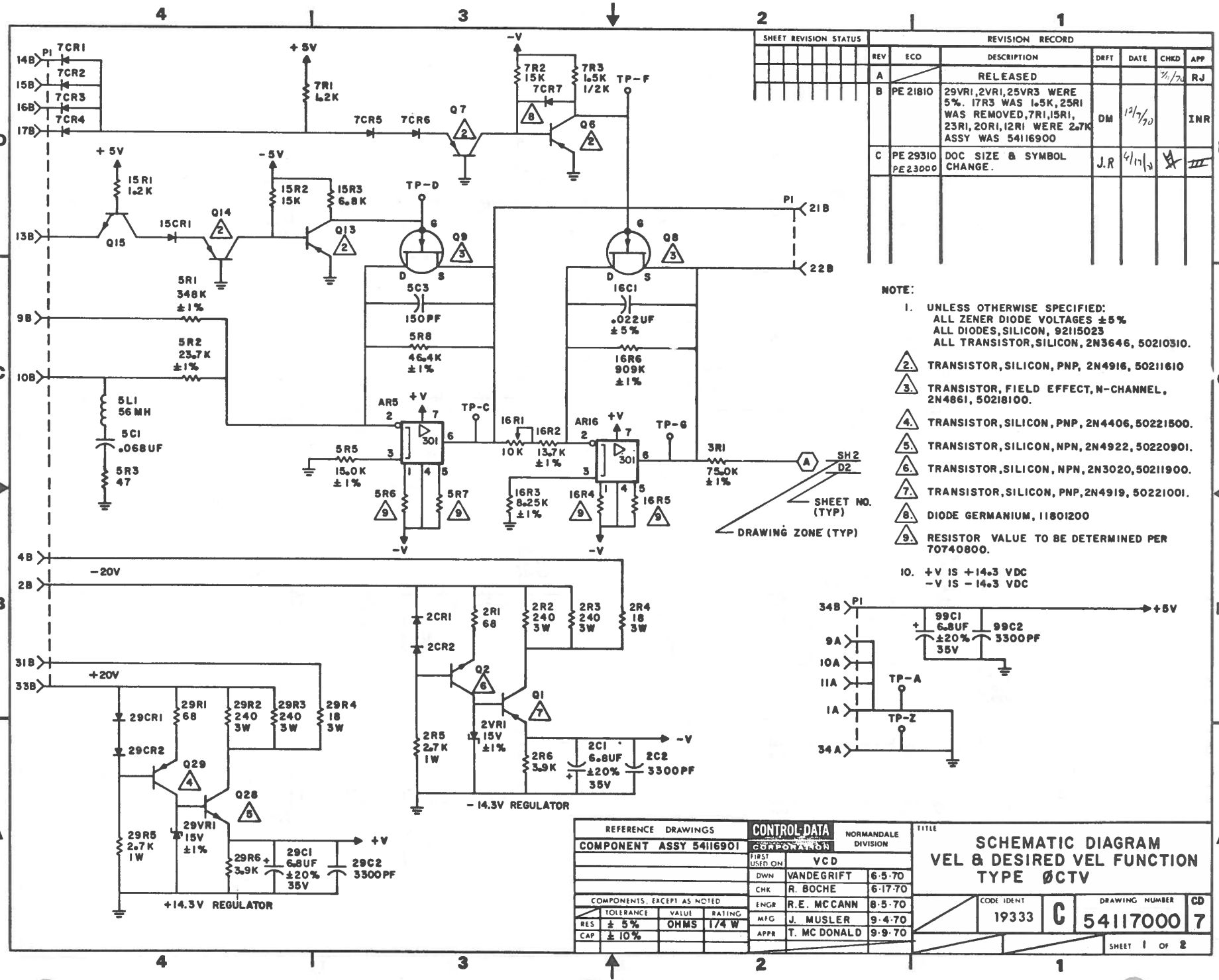
SCHEMATIC DIAGRAM D/A CONVERTER TYPE ØCSV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54116600	5

SHEET 1 OF 2

B 54116600


SCHEMATIC DIAGRAM
D/A CONVERTER
TYPE ØCSV
54116600
REVISION RECORD
SEE SHEET 1 FOR REV
TP-F
TP-K
TP-J
TP-H
TP-G
+V
-V
+5V
U-B4F
U-B4E
U-B4D
U-B4C



SHEET REVISION STATUS

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED			7/1/70	RJ
B	PE 21810	29VR1, 2VR1, 25VR3 WERE 5%. 17R3 WAS 1.5K, 25R1 WAS REMOVED, 7R1, 15R1, 23R1, 20R1, 12R1 WERE 2.7K ASSY WAS 54116900	DM	12/7/70		INR
C	PE 29310 PE 23000	DOC SIZE & SYMBOL CHANGE.	J.R	4/17/71		

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL ZENER DIODE VOLTAGES ±5%
   ALL DIODES, SILICON, 92115023
   ALL TRANSISTOR, SILICON, 2N3646, 50210310.
2. TRANSISTOR, SILICON, PNP, 2N4916, 50211610
3. TRANSISTOR, FIELD EFFECT, N-CHANNEL, 2N4861, 50218100.
4. TRANSISTOR, SILICON, PNP, 2N4406, 50221500.
5. TRANSISTOR, SILICON, NPN, 2N4922, 50220901.
6. TRANSISTOR, SILICON, NPN, 2N3020, 50211900.
7. TRANSISTOR, SILICON, PNP, 2N4919, 50221001.
8. DIODE GERMANIUM, 11801200
9. RESISTOR VALUE TO BE DETERMINED PER 70740800.
10. +V IS +14.3 VDC
    -V IS -14.3 VDC

REFERENCE DRAWINGS
COMPONENT ASSY 54116901

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4 W
CAP	± 10%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	VCD	
DWN	VANDEGRIFT	6-5-70
CHK	R. BOCHE	6-17-70
ENGR	R.E. MCCANN	8-5-70
MFG	J. MUSLER	9-4-70
APPR	T. MC DONALD	9-9-70

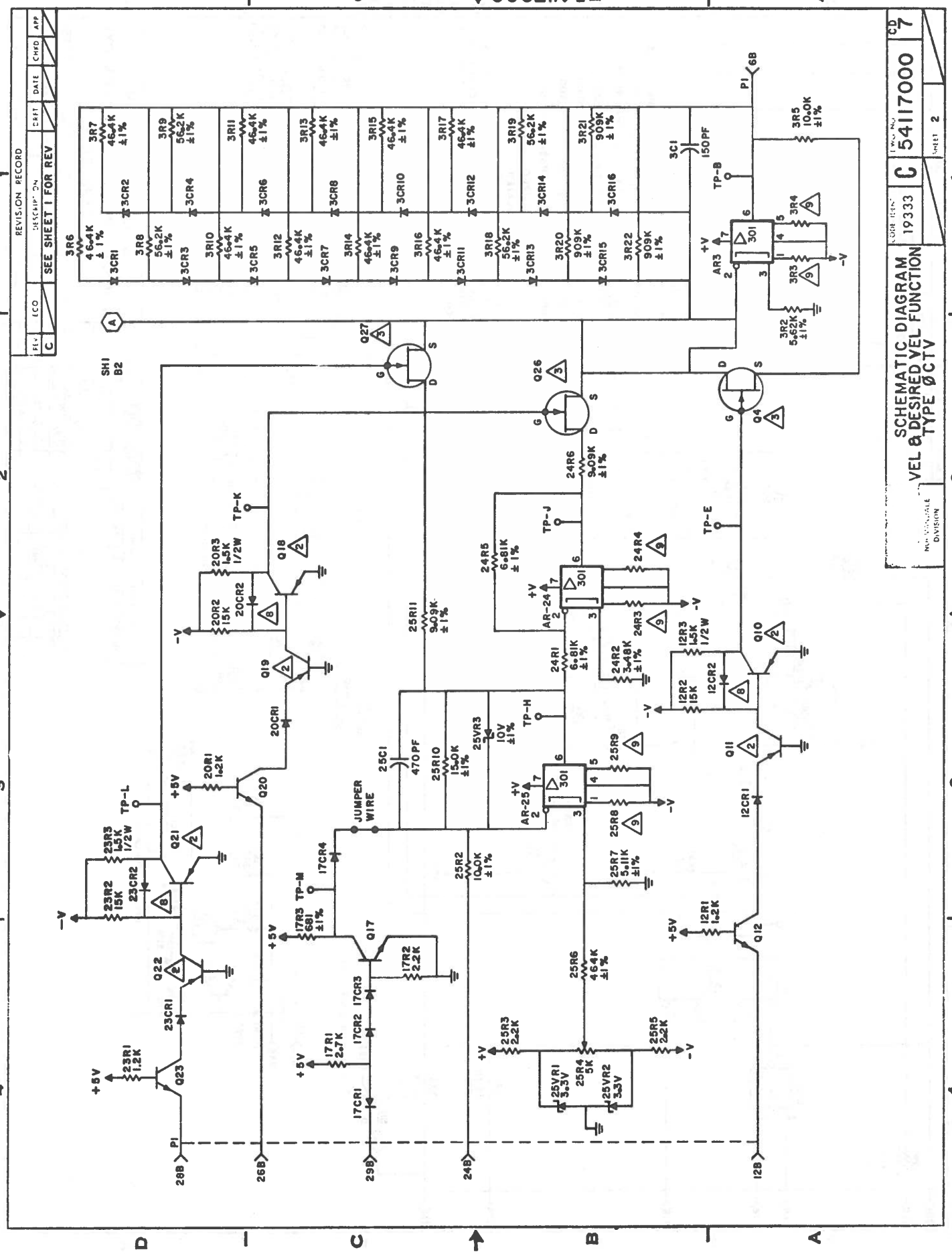
TITLE

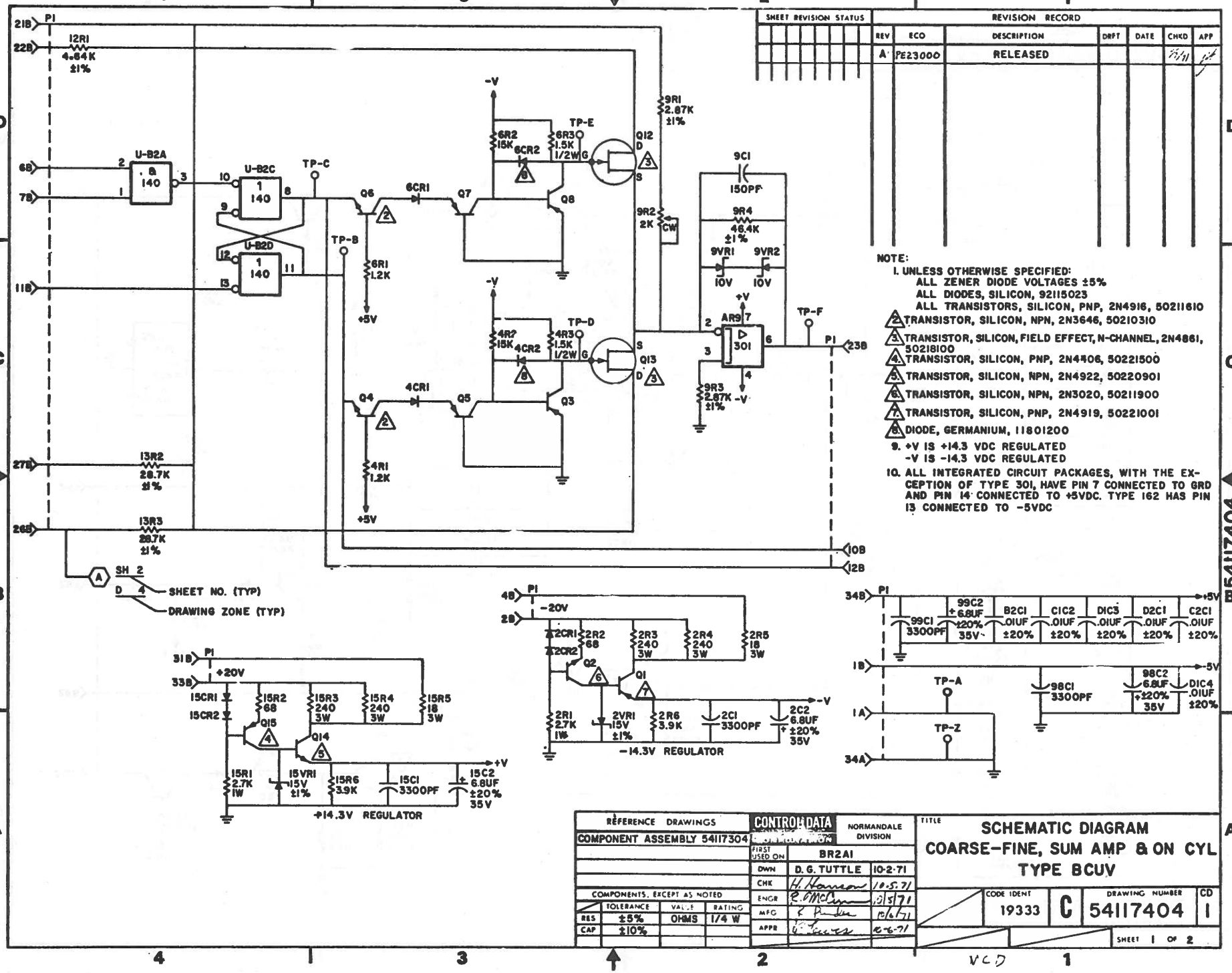
SCHEMATIC DIAGRAM VEL & DESIRED VEL FUNCTION TYPE ØCTV

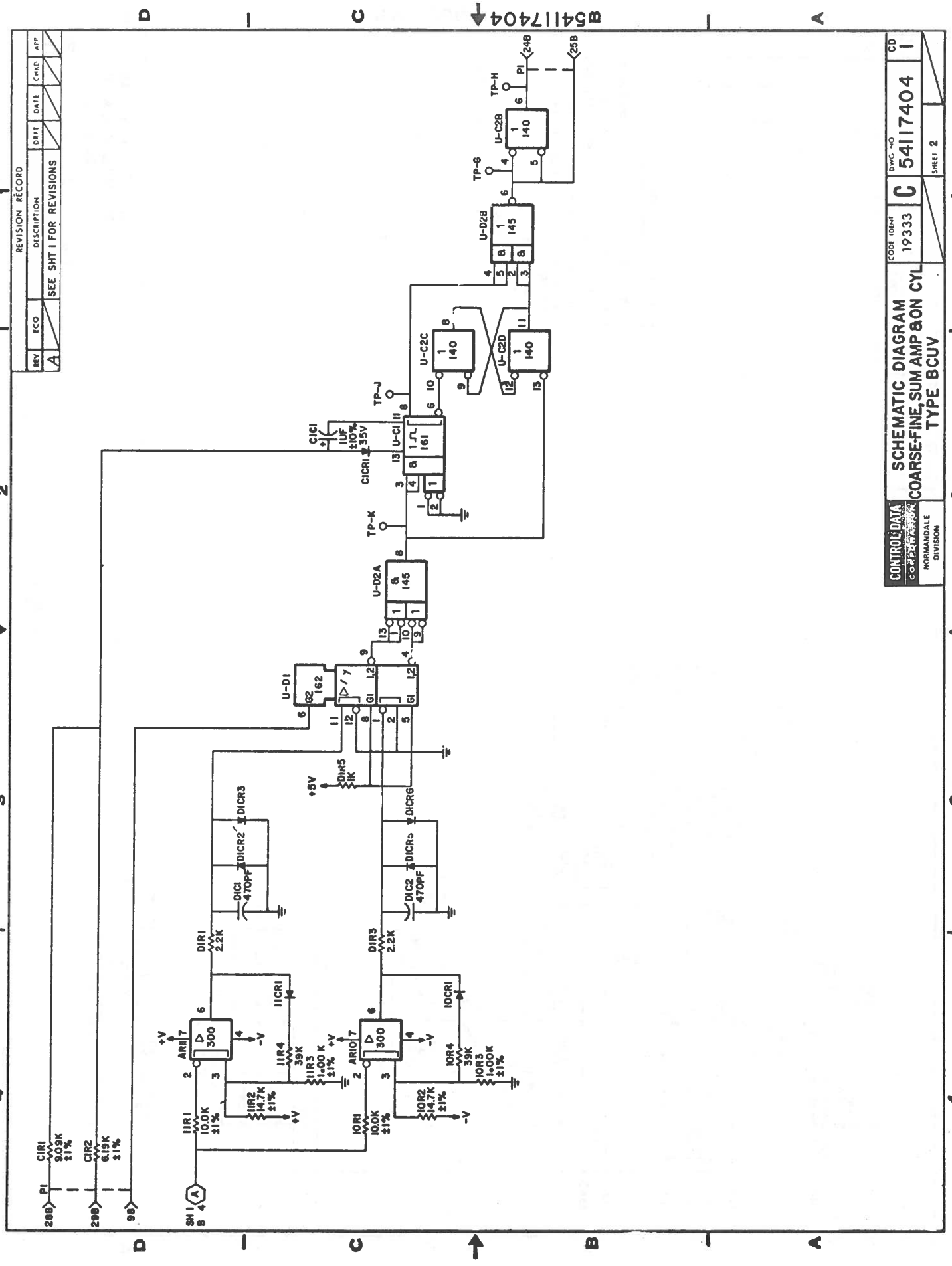
CODE IDENT		DRAWING NUMBER	CD
19333	C	54117000	7

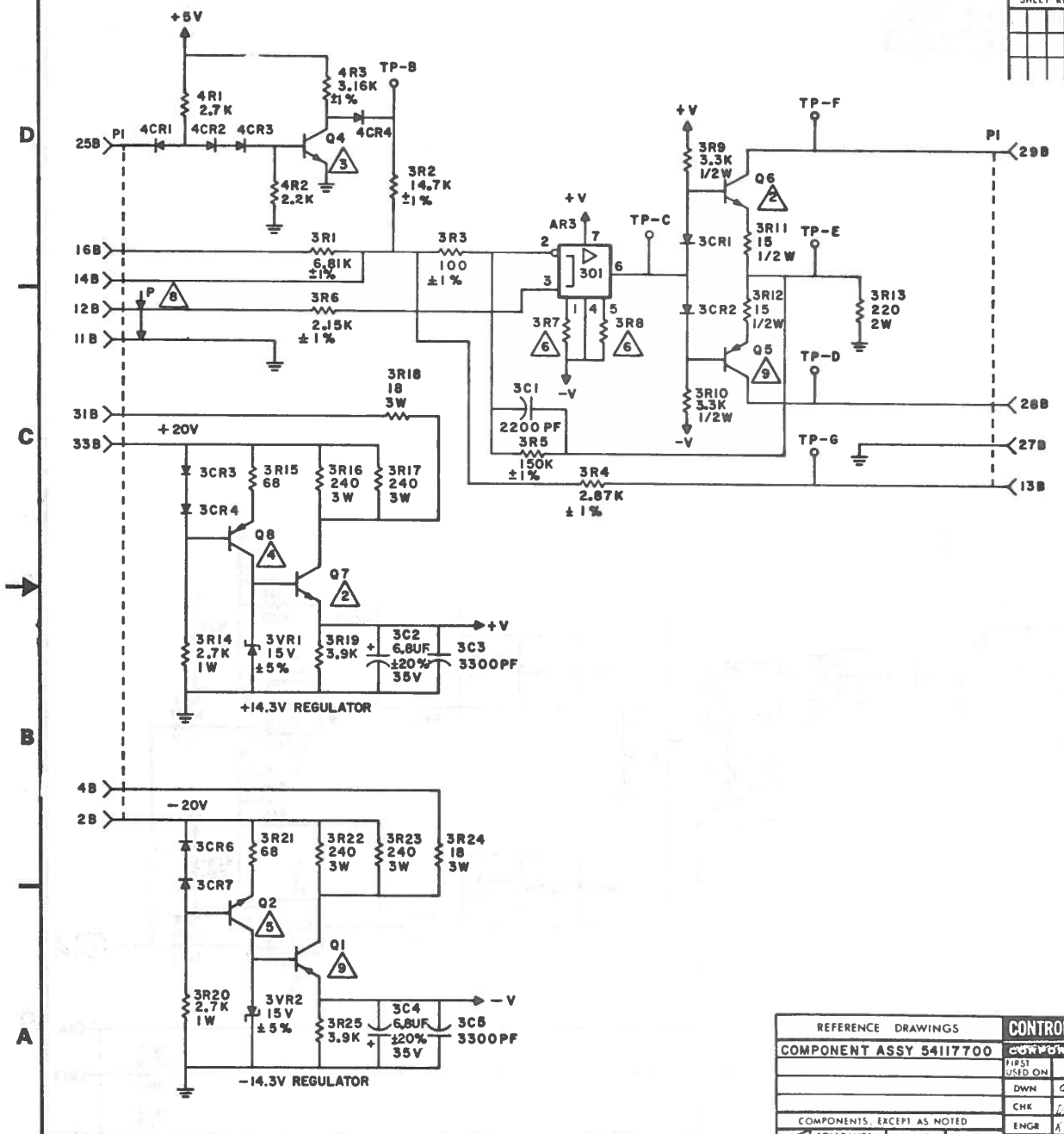
SHEET 1 OF 2

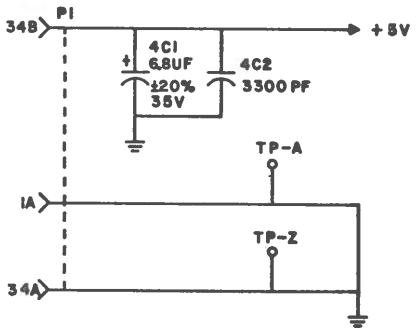
54117000


54117000
REVISION RECORD
SEE SHEET 1 FOR REV
SCHEMATIC DIAGRAM
VEL & DESIRED VEL FUNCTION
TYPE ØCTV
54117000
C
19333
SHEET 2
7


SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | PE23000 | RELEASED
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL ZENER DIODE VOLTAGES ±5%
ALL DIODES, SILICON, 92115023
ALL TRANSISTORS, SILICON, PNP, 2N4916, 50211610
2. TRANSISTOR, SILICON, NPN, 2N3646, 50210310
3. TRANSISTOR, SILICON, FIELD EFFECT, N-CHANNEL, 2N4861, 50218100
4. TRANSISTOR, SILICON, PNP, 2N4406, 50221500
5. TRANSISTOR, SILICON, NPN, 2N4922, 50220901
6. TRANSISTOR, SILICON, NPN, 2N3020, 50211900
7. TRANSISTOR, SILICON, PNP, 2N4919, 50221001
8. DIODE, GERMANIUM, 11801200
9. +V IS +14.3 VDC REGULATED
-V IS -14.3 VDC REGULATED
10. ALL INTEGRATED CIRCUIT PACKAGES, WITH THE EXCEPTION OF TYPE 301, HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5VDC. TYPE 162 HAS PIN 13 CONNECTED TO -5VDC
SHEET NO. (TYP)
DRAWING ZONE (TYP)
+14.3V REGULATOR
-14.3V REGULATOR
REFERENCE DRAWINGS
COMPONENT ASSEMBLY 54117304
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ±5% | OHMS | 1/4 W
CAP ±10%
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON BR2AI
DWN D. G. TUTTLE 10-2-71
CHK H. Hanson 10-5-71
ENGR R. McClure 10/5/71
MFG K. Pinder 10/6/71
APPR V. Power 10-6-71
TITLE
SCHEMATIC DIAGRAM
COARSE-FINE, SUM AMP & ON CYL
TYPE BCUV
CODE IDENT 19333
C
DRAWING NUMBER 54117404
CD 1
SHEET 1 OF 2
54117404 B


54117404
REVISION RECORD
REV
ECO
DESCRIPTION
SEE SHT 1 FOR REVISIONS
DRFT
DATE
CHKD
APP
CONTROL DATA CORPORATION
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
COARSE-FINE, SUM AMP & ON CYL
TYPE BCUV
CODE IDENT 19333
C
DWG NO 54117404
SHEET 2
CD 1
U-C2B
U-D2B
U-C2C
U-C2D
U-C1
U-D2A
U-D1
TP-H
TP-G
TP-J
TP-K
C1C1
C1CR1
D1C1 470PF
D1C2 470PF
D1R1 2.2K
D1R3 2.2K
D1R5 1K
D1CR2
D1CR3
D1CR5
D1CR6
11CR1
10CR1
11R1 10.0K ±1%
11R2 14.7K ±1%
11R3 1.00K ±1%
11R4 39K
10R1 10.0K ±1%
10R2 14.7K ±1%
10R3 1.00K ±1%
10R4 39K
C1R1 9.09K ±1%
C1R2 6.19K ±1%
+5V
+V
-V
SH 1 B 4





SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED				RJ
B	PE 29310 PE 23000	DOC SIZE & SYM CHANGE	JAR	6/11		

NOTE:

1. UNLESS OTHERWISE SPECIFIED: ALL DIODES SILICON, 92115023
2. TRANSISTOR SILICON, NPN, 2N4922, 50220901.
3. TRANSISTOR SILICON, NPN, 2N3646, 50210310.
4. TRANSISTOR SILICON, PNP, 2N4406, 50221500.
5. TRANSISTOR SILICON, NPN, 2N3020, 50211900.
6. RESISTOR VALUE TO BE SELECTED PER 70740800.
7. +V IS +14.3 VDC
   -V IS -14.3 VDC
8. PAIRED CONDUCTORS ARE NOT TWISTED.
9. TRANSISTOR SILICON PNP, 2N4919, 50221001.

REFERENCE DRAWINGS
COMPONENT ASSY 54117700

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4 W
CAP	± 10%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	VCD	
DWN	C. DAUGHTON	2-26-70
CHK	J. RADCLIFFE	3-[illegible]-70
ENGR	K. E. McCANN	3-5-70
MFG	K. N. OLSON	3-17-70
APPR	T. M. DONALD	3-[illegible]-70

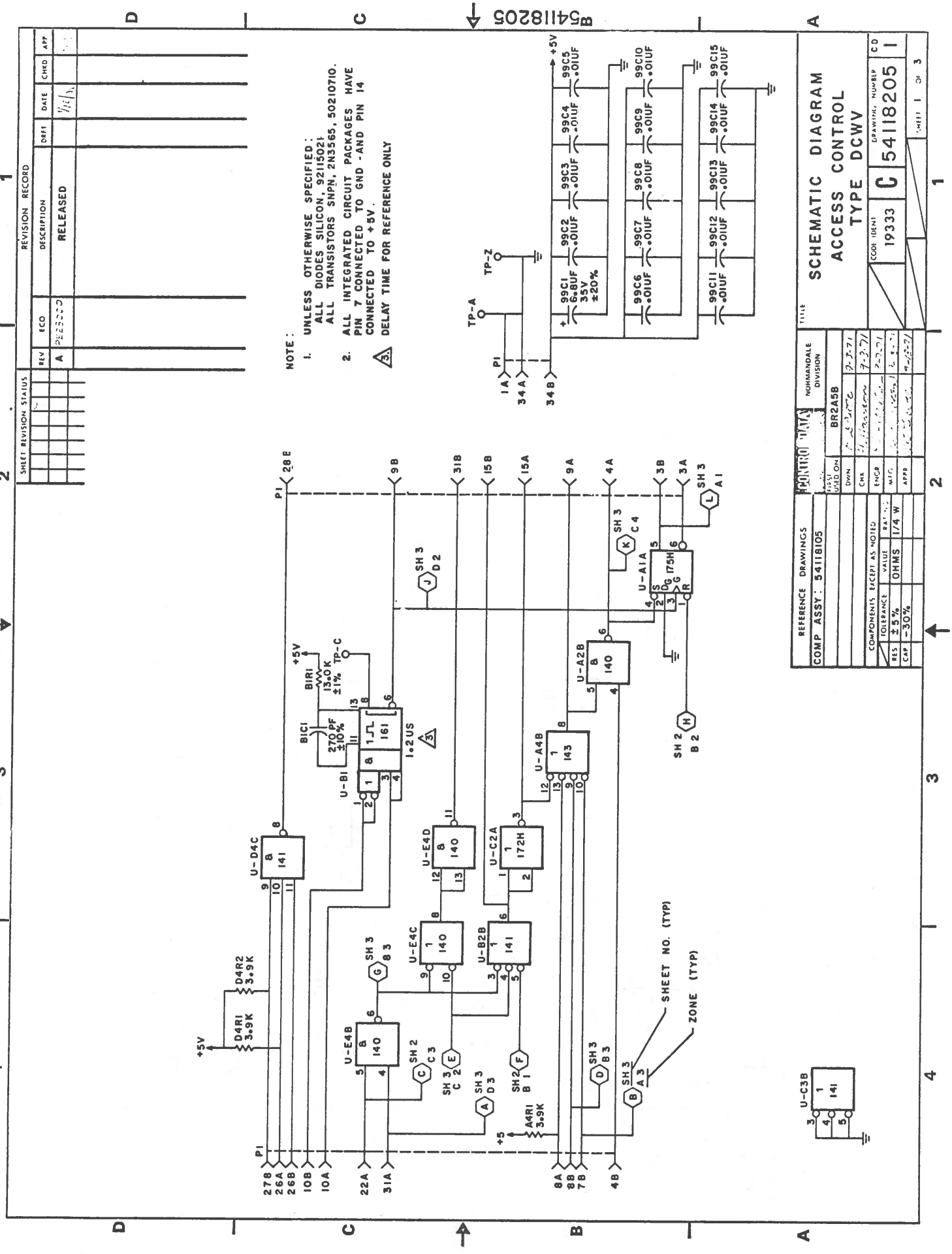
TITLE

SCHEMATIC DIAGRAM POWER AMPL PREAMP TYPE ØCVV

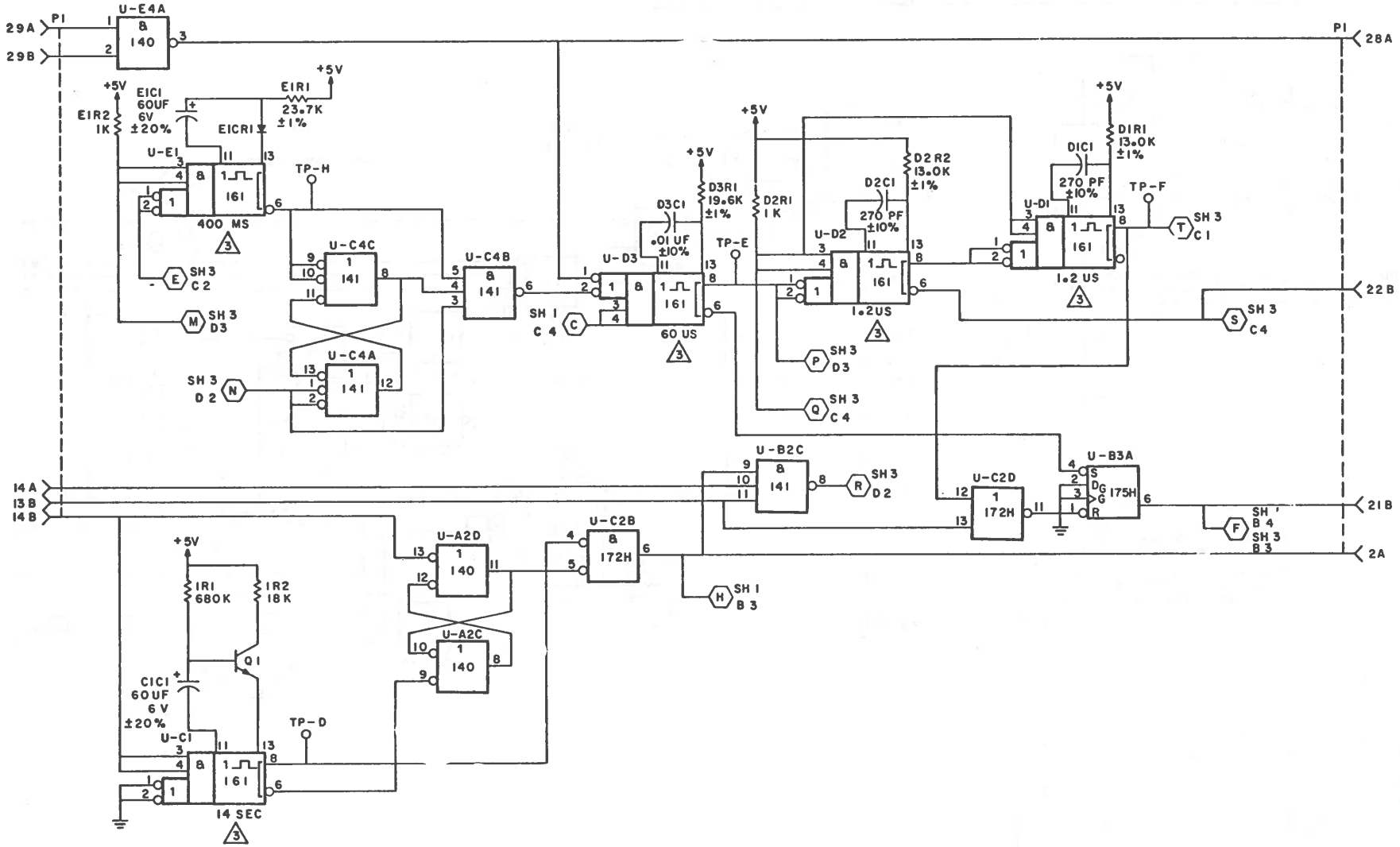
CODE IDENT		DRAWING NUMBER	CD
19333	C	54117800	0

SHEET 1 OF 1

54117800 B

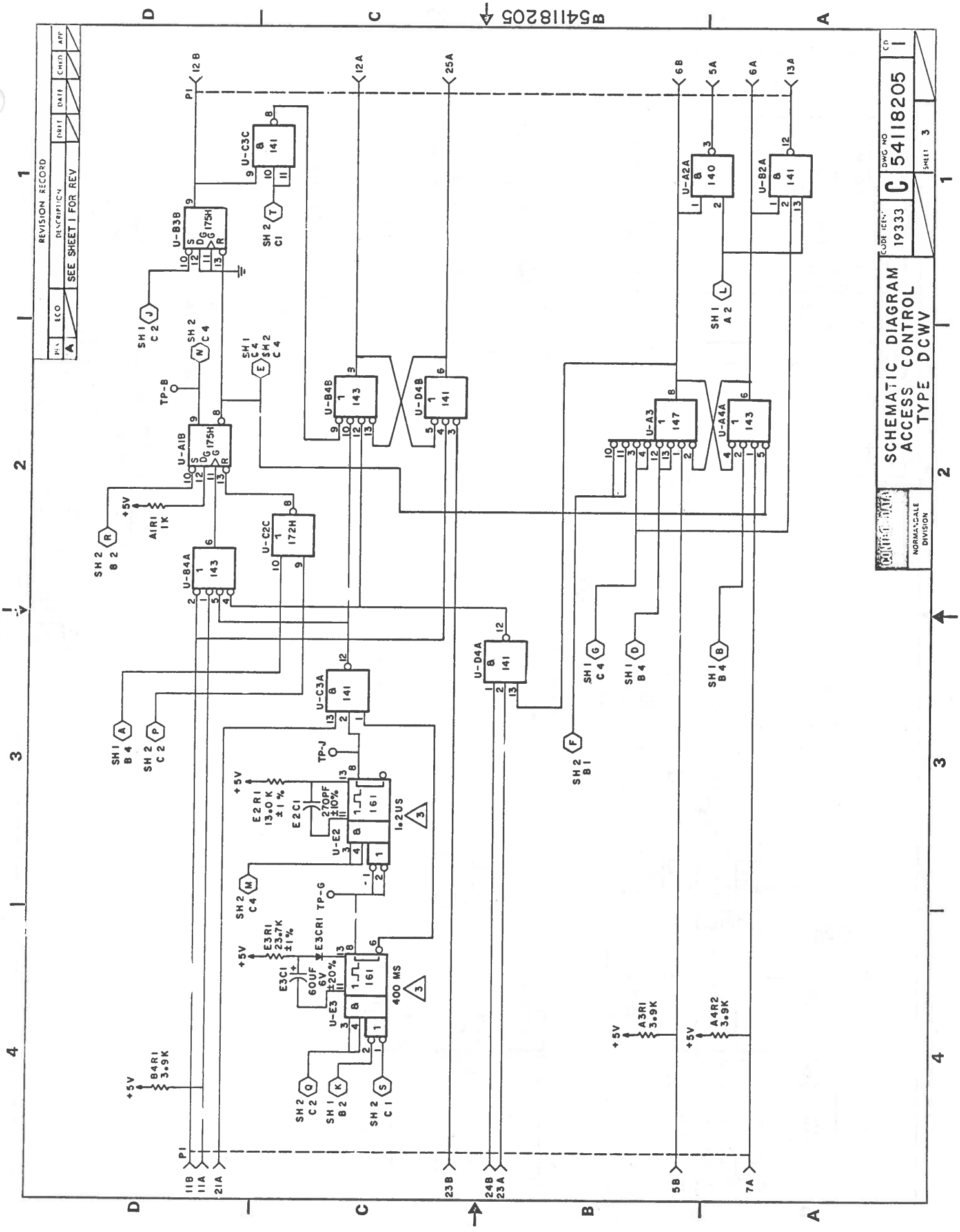

54118205
SCHEMATIC DIAGRAM
ACCESS CONTROL
TYPE DCWV
NORMANDALE DIVISION
BR2A5B
REVISION RECORD
SHEET REVISION STATUS
REFERENCE DRAWINGS
COMP ASSY: 54118105
COMPONENTS EXCEPT AS NOTED
TOLERANCE
RES ±5%
CAP -30%
VALUE
OHMS
1/4 W
CODE IDENT 19333
DRAWING NUMBER C 54118205
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL DIODES SILICON, 9211502
ALL TRANSISTORS SNPN, 2N3565, 50210710.
2. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND - AND PIN 14 CONNECTED TO +5V.
3. DELAY TIME FOR REFERENCE ONLY
+5V
TP-A
TP-Z
99C1 6.8UF 35V ±20%
99C2 .01UF
99C3 .01UF
99C4 .01UF
99C5 .01UF
99C6 .01UF
99C7 .01UF
99C8 .01UF
99C9 .01UF
99C10 .01UF
99C11 .01UF
99C12 .01UF
99C13 .01UF
99C14 .01UF
99C15 .01UF
U-D4C
U-E4D
U-C2A
U-A4B
U-A2B
U-A1A
U-B1
U-E4C
U-B2B
U-E4B
U-C3B
D4R2 3.9K
D4R1 3.9K
A4R1 3.9K
B1R1 13.0K ±1%
B1C1 270 PF ±10%
1.2US
SHEET NO. (TYP)
ZONE (TYP)

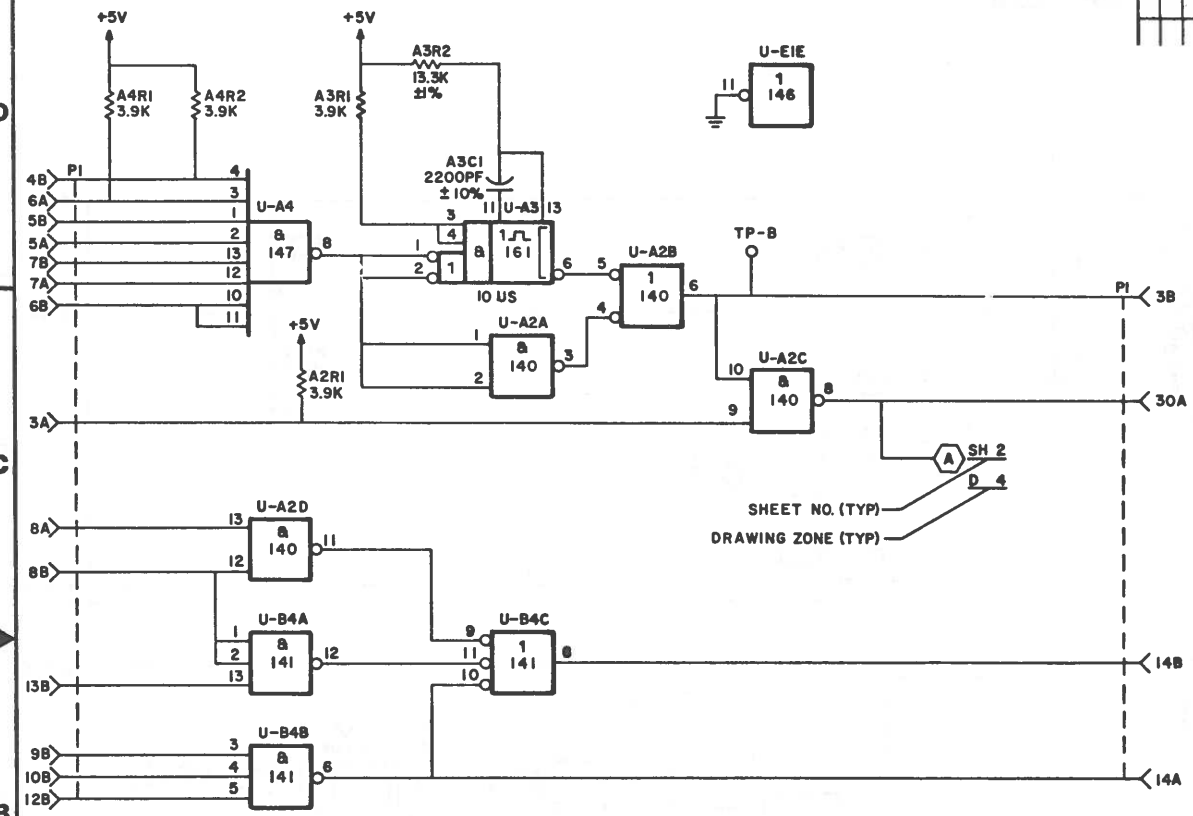
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
4		SEE SHEET 1 FOR REV				

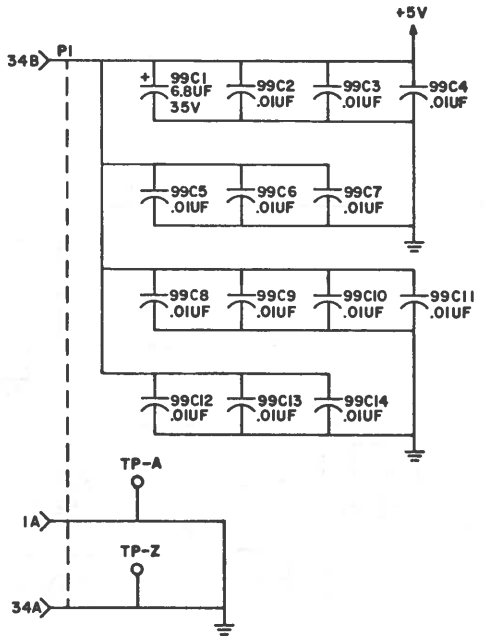


NORMANDALE DIVISION	SCHEMATIC DIAGRAM ACCESS CONTROL TYPE DCWV	CODE IDENT 19333	C	DWG NO 54118205	CD 1
				SHEET 2	

54118205


54118205
REVISION RECORD
SEE SHEET 1 FOR REV
SCHEMATIC DIAGRAM
ACCESS CONTROL
TYPE DCWV
NORMANDALE DIVISION
CODE IDENT 19333
DWG NO 54118205
SHEET 3
U-C3C
U-B3B
U-A1B
U-B4B
U-D4B
U-A2A
U-B2A
U-A3
U-A4A
U-C2C
U-B4A
U-D4A
U-C3A
U-E2
U-E3
E2R1 13.0K ±1%
E2C1 270PF ±10%
E3R1 23.7K ±1%
E3C1 60UF 6V ±20%
A1R1 1K
B4R1 3.9K
A3R1 3.9K
A4R2 3.9K
1.2US
400 MS
TP-B
TP-J
TP-G
+5V





SHEET REVISION STATUS

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED			5/31/70	RJ
B	PE 21807	A3R2 WAS 14.7K, A3C1 WAS 470 PF, 10US WAS 2US, ASSY NO WAS 54118900.	BR	7/17/70		INR
C	PE 29310 PE 23000	DOC SIZE & SYMBOL CHANGE.	JAR	9/17/71		III

NOTE:

1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5V

REFERENCE DRAWINGS
COMPONENT ASSEMBLY 54118901

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±20%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

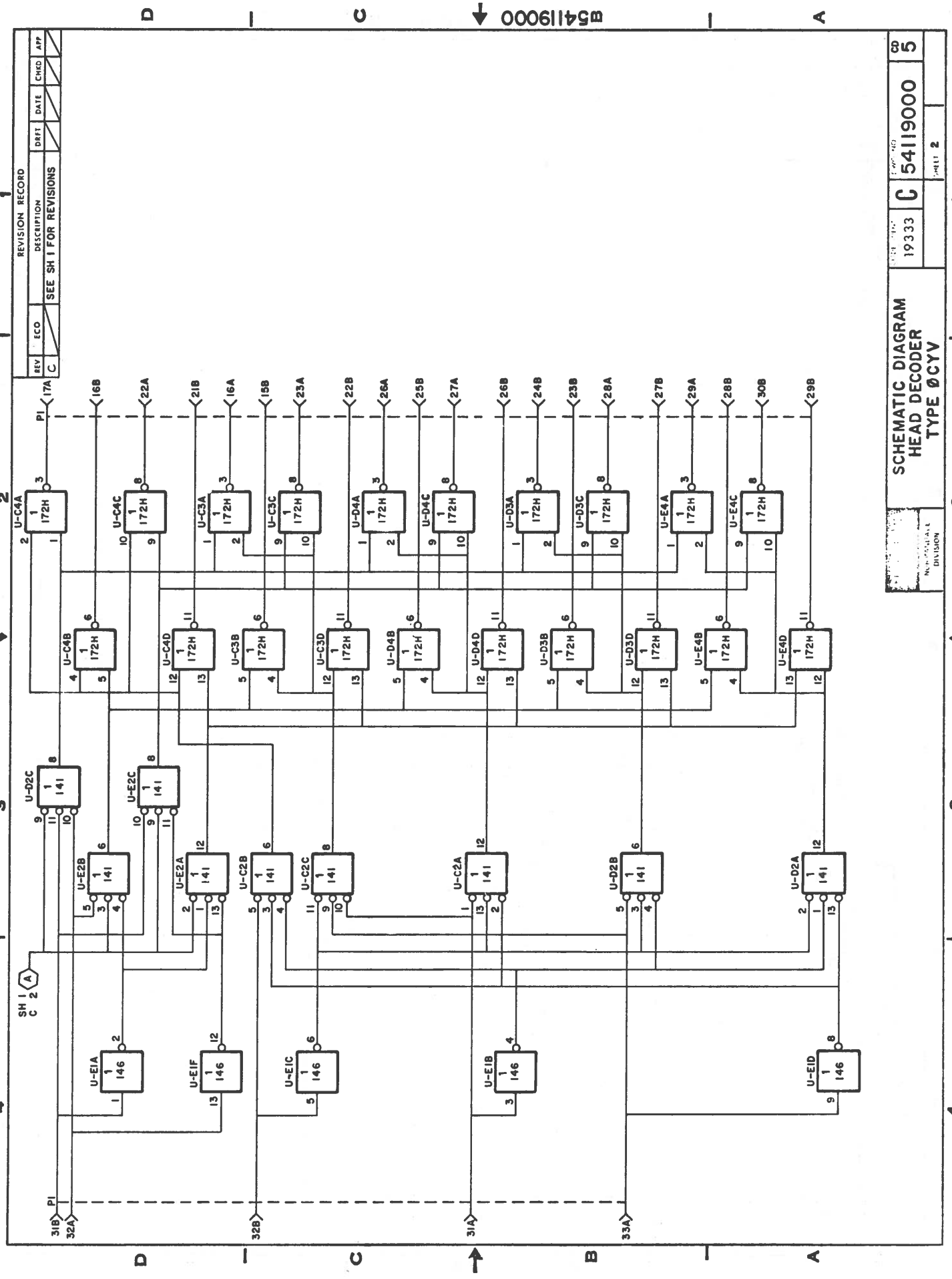
FIRST USED ON	VCD	
DWN	J.E. MATTSON	4-18-70
CHK	D. RADCLIFFE	5-26-70
ENGR	R.J. NIELSEN	7-27-70
MFG	S.W. OLSON	8-13-70
APPR	T. MC DONALD	8-27-70

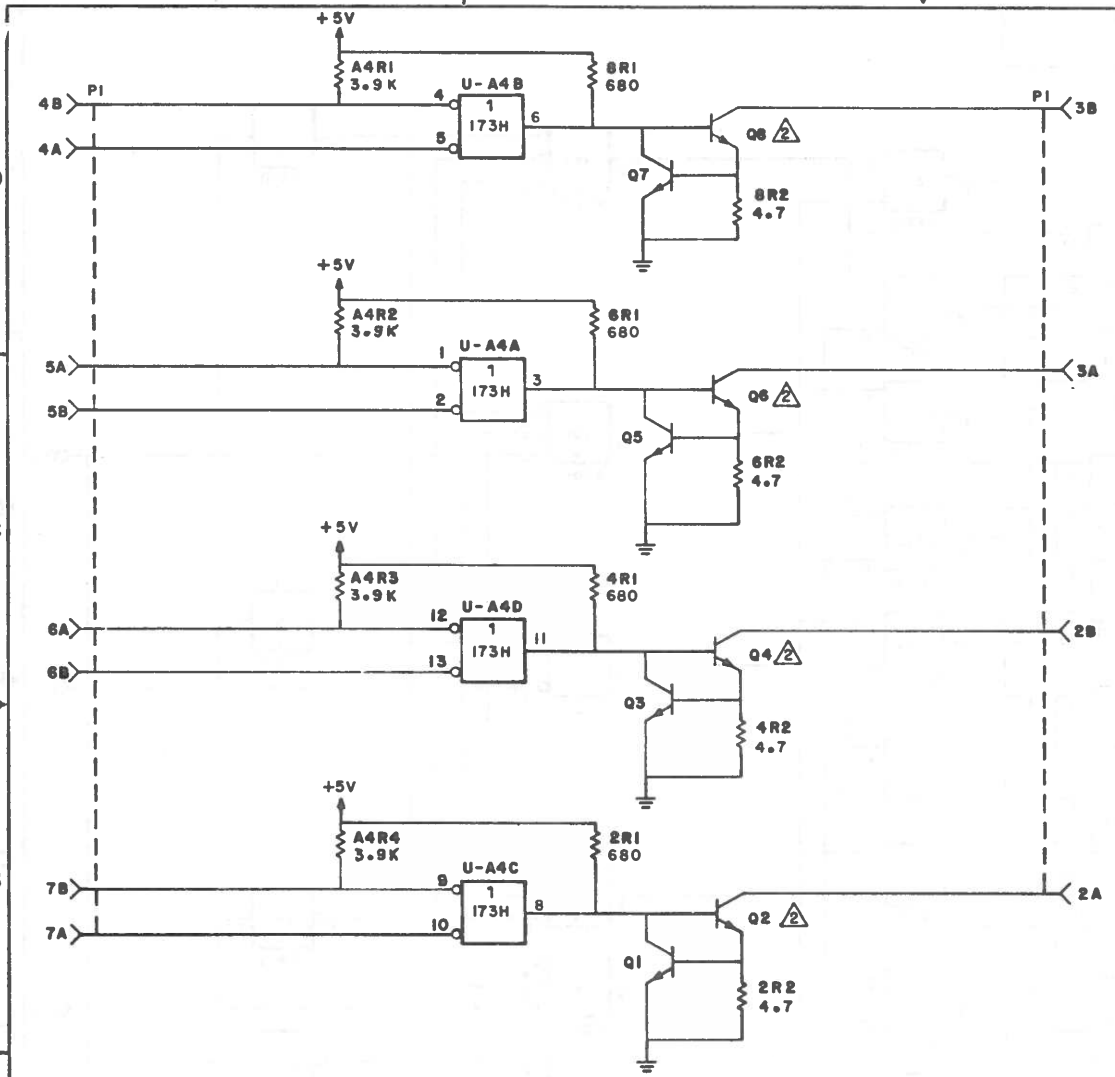
TITLE

SCHEMATIC DIAGRAM HEAD DECODER TYPE ØCYV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54119000	5

SHEET 1 OF 2


REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
C
SEE SH 1 FOR REVISIONS
SCHEMATIC DIAGRAM
HEAD DECODER
TYPE ØCYV
19333
C 54119000
SH 2
5
54119000 B
U-C4A 1 172H
U-C4C 1 172H
U-C3A 1 172H
U-C3C 1 172H
U-D4A 1 172H
U-D4C 1 172H
U-D3A 1 172H
U-D3C 1 172H
U-E4A 1 172H
U-E4C 1 172H
U-C4B 1 172H
U-C4D 1 172H
U-C3B 1 172H
U-C3D 1 172H
U-D4B 1 172H
U-D4D 1 172H
U-D3B 1 172H
U-D3D 1 172H
U-E4B 1 172H
U-E4D 1 172H
U-D2C 1 141
U-E2C 1 141
U-E2B 1 141
U-E2A 1 141
U-C2B 1 141
U-C2C 1 141
U-C2A 1 141
U-D2B 1 141
U-D2A 1 141
U-E1A 1 146
U-E1F 1 146
U-E1C 1 146
U-E1B 1 146
U-E1D 1 146
SH 1 C 2
P1
17A
16B
22A
21B
16A
15B
23A
22B
26A
25B
27A
26B
24B
23B
28A
27B
29A
28B
30B
29B
31B
32A
32B
31A
33A



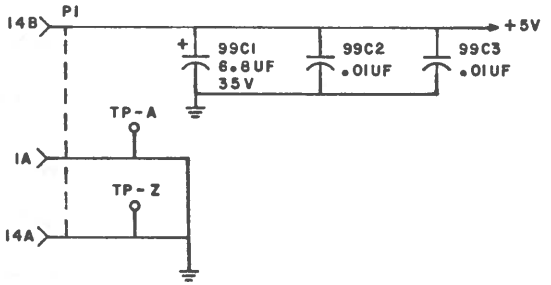
SHEET REVISION STATUS			REVISION RECORD					
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A		RELEASED		8-31-70		RJ
	B	PE29310 PE23000	DOC SIZE & SYM CHANGE	J.R.	9/1/70		III

NOTE:

1 UNLESS OTHERWISE SPECIFIED
ALL TRANSISTOR, SILICON NPN 2N3646
50210310

2 TRANSISTORS SILICON NPN 2N3569 50210811

3 ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5V



REFERENCE DRAWINGS			
COMP ASSY	54120100		
	± 5 %	OHMS	1/4 W
	± 20%		

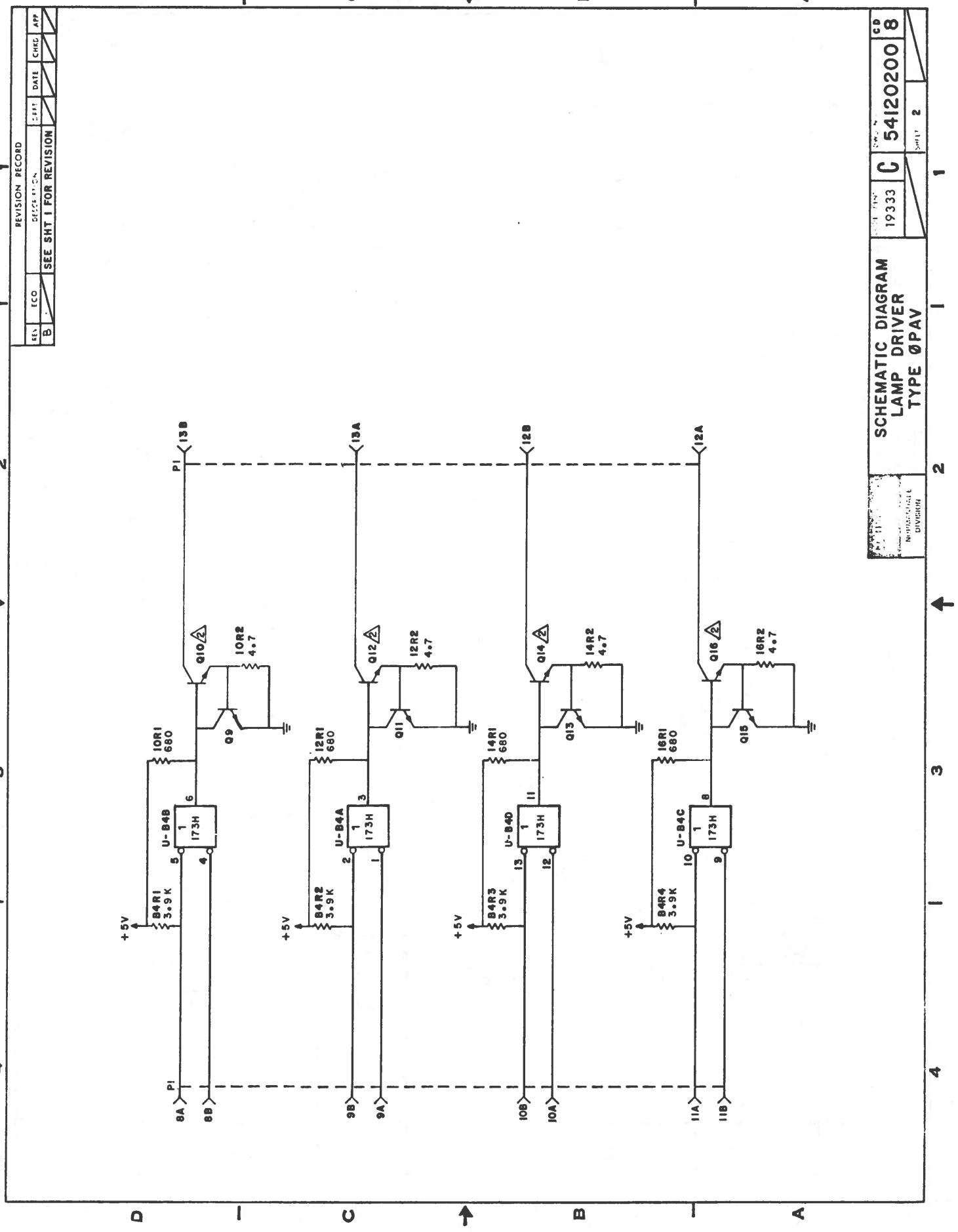
GORSUCH DIVISION
VCD
K. Fisher 5-19-70

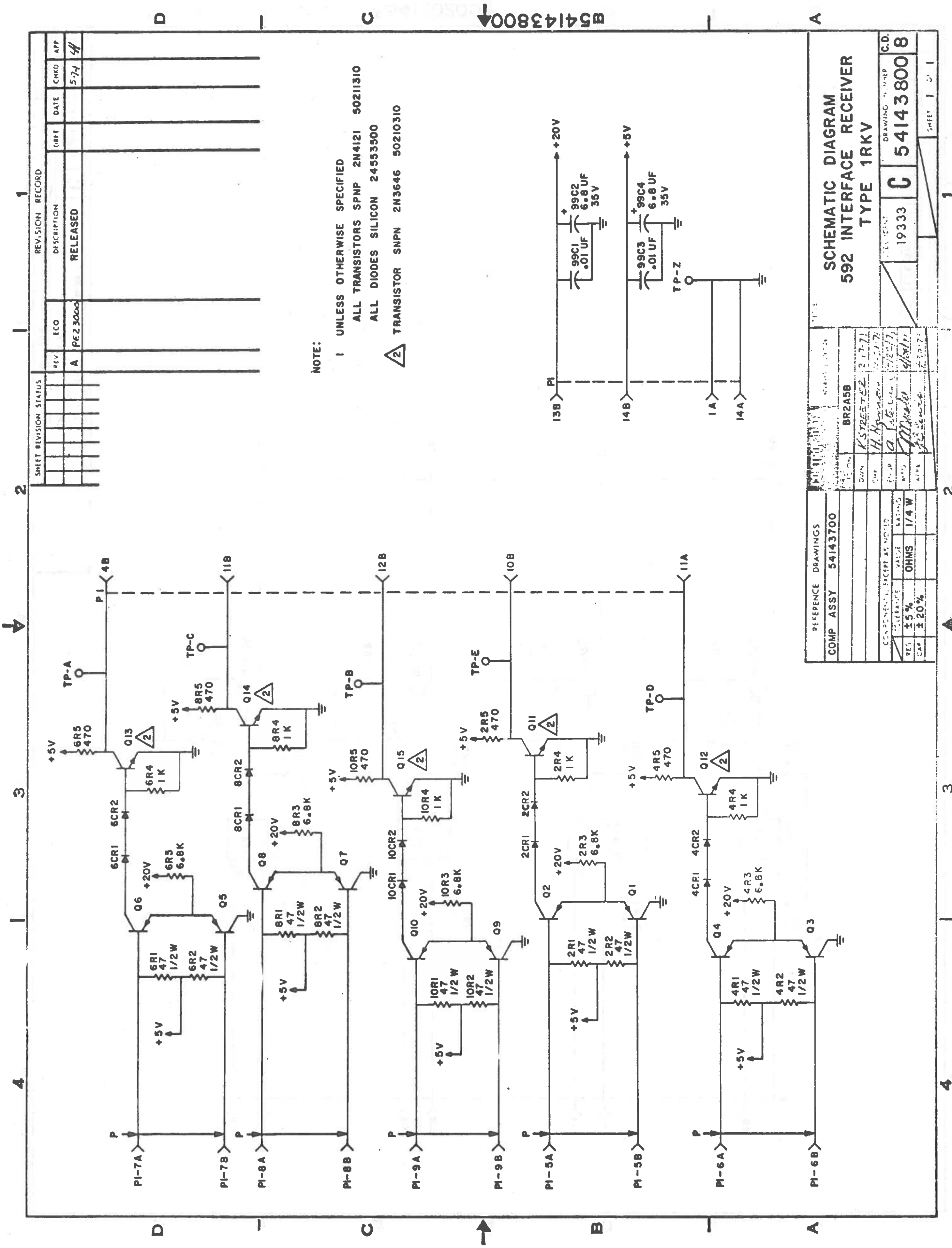
SCHEMATIC DIAGRAM
LAMP DRIVER
TYPE ØPAV

CAGE		DRAWING NUMBER	CD
19333	C	54120200	8

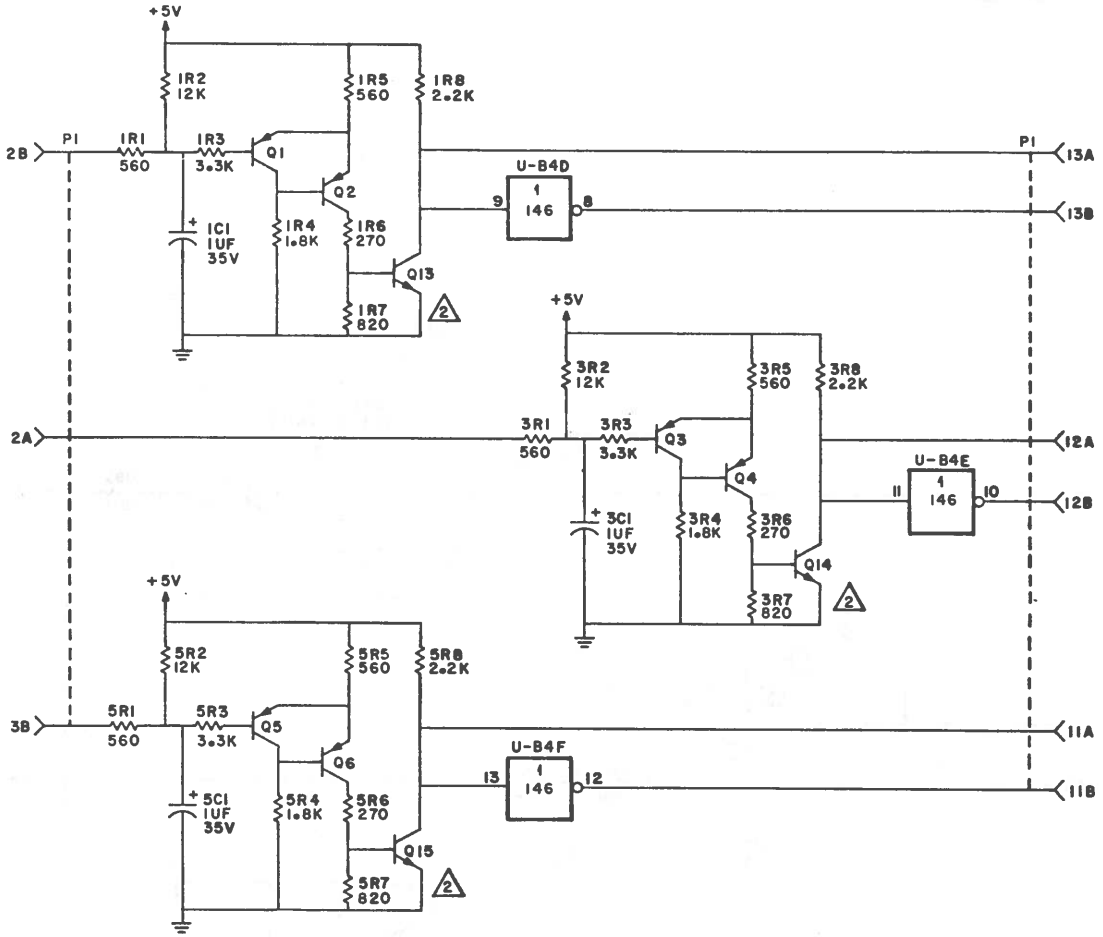
SHEET 1 OF 2

54120200


REVISION RECORD
REV
ECO
DESCRIPTION
DATE
CHKD
APP
B
SEE SHT 1 FOR REVISION
SCHEMATIC DIAGRAM
LAMP DRIVER
TYPE ØPAV
19333
C
54120200
SHT 2
8
P1
13B
13A
12B
12A
Q10
Q12
Q14
Q16
Q9
Q11
Q13
Q15
10R2 4.7
12R2 4.7
14R2 4.7
16R2 4.7
10R1 680
12R1 680
14R1 680
16R1 680
U-84B
U-84A
U-84D
U-84C
1
173H
B4R1 3.9K
B4R2 3.9K
B4R3 3.9K
B4R4 3.9K
+5V
8A
8B
9B
9A
10B
10A
11A
11B

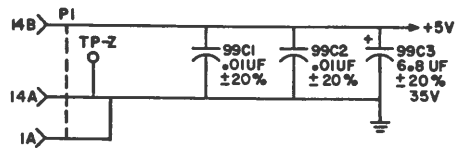

SCHEMATIC DIAGRAM
592 INTERFACE RECEIVER
TYPE 1RKV
54143800
C
19333
B54143800
NOTE:
1 UNLESS OTHERWISE SPECIFIED
ALL TRANSISTORS SPNP 2N4121 50211310
ALL DIODES SILICON 24553500
2 TRANSISTOR SNPN 2N3646 50210310
REVISION RECORD
RELEASED
PE 23000
REFERENCE DRAWINGS
COMP ASSY 54143700
BR2A5B
±5%
±20%
OHMS
1/4 W
+20V
+5V
99C1 .01 UF
99C2 6.8 UF 35V
99C3 .01 UF
99C4 6.8 UF 35V
TP-Z
TP-A
TP-B
TP-C
TP-D
TP-E
P1-7A
P1-7B
P1-8A
P1-8B
P1-9A
P1-9B
P1-5A
P1-5B
P1-6A
P1-6B

SHEET REVISION STATUS							
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED			4-3-70	RL
B	PE29310 PE23000	DOC SIZE & SYM CHANGE	J.R	6/11/71		



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS SILICON, PNP, 2N4258, 50211510.
2. TRANSISTOR SILICON, NPN, 2N3646, 50210310.
3. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5VDC.



REFERENCE DRAWINGS			
COMPONENT ASSY. 54150100.			
	±5%	OHMS	1/4 W.
	±10%	—	—

CONTROL DATA — NORMANDALE DIVISION

VCD

DSN	Stuber	3-30-70
CHK	[illegible]	5-13-70
ENGR	[illegible]	7-30-70
MFG	[illegible]	5-13-70
QUAL	[illegible]	5-27-70

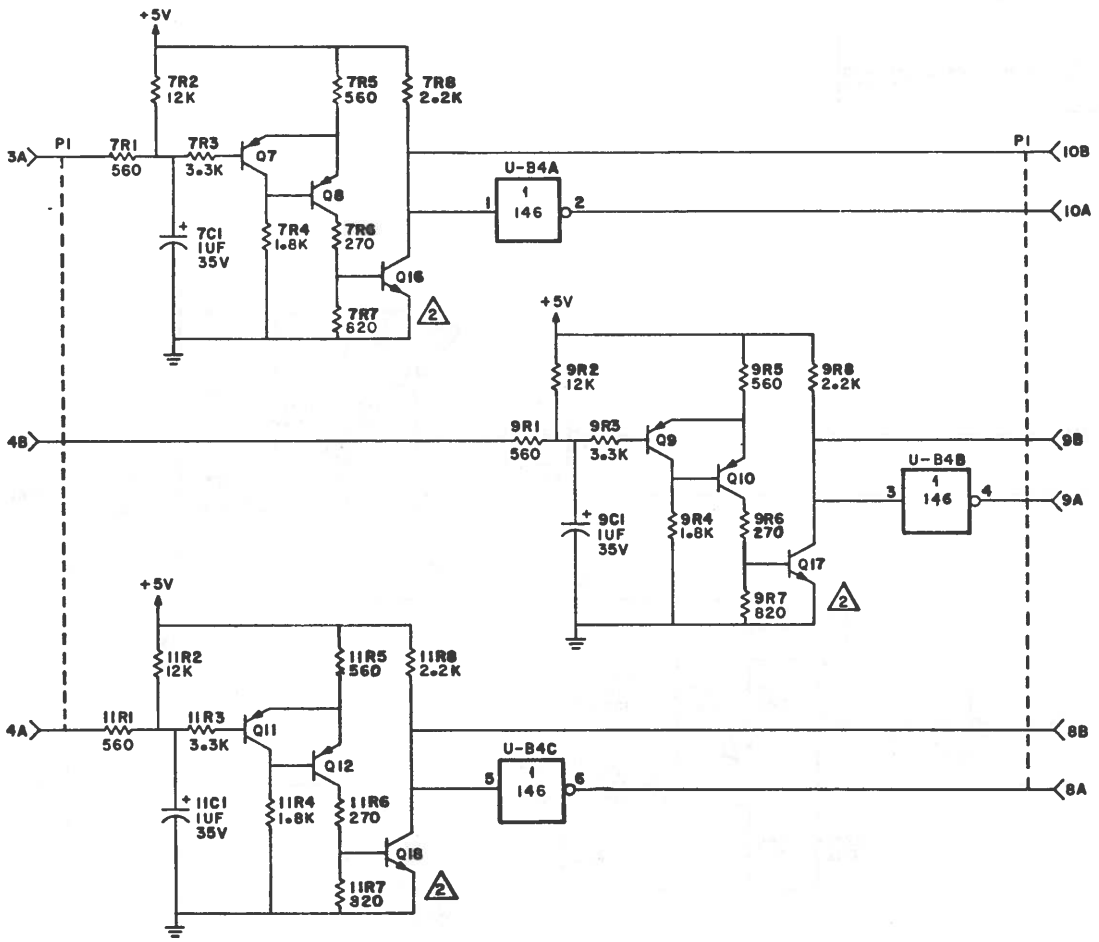
TITLE

SCHEMATIC DIAGRAM SWITCH RECEIVER TYPE ØSAV

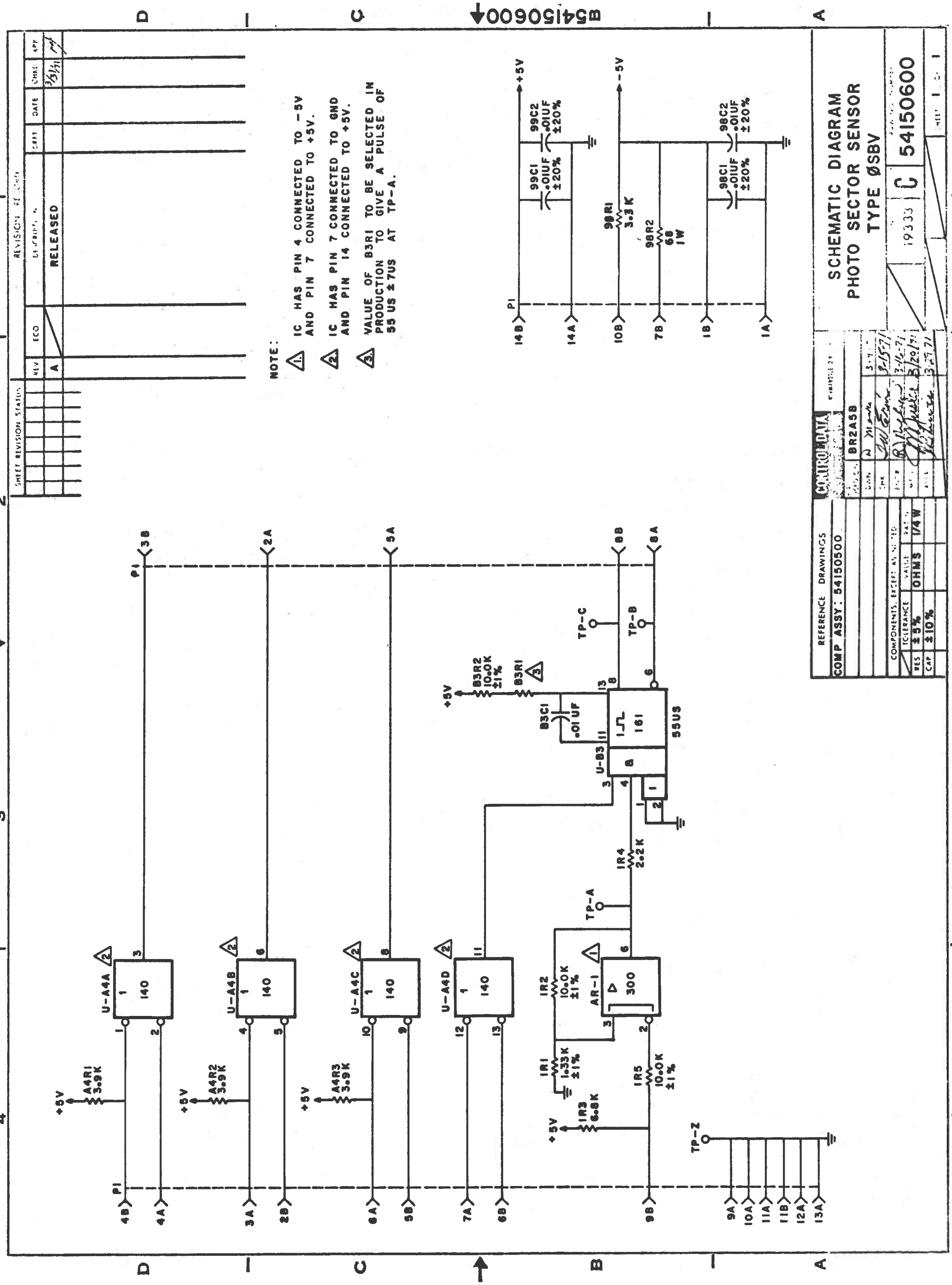
CONTRACT	DRAWING NUMBER	C.D.
19333	C 54150200	1

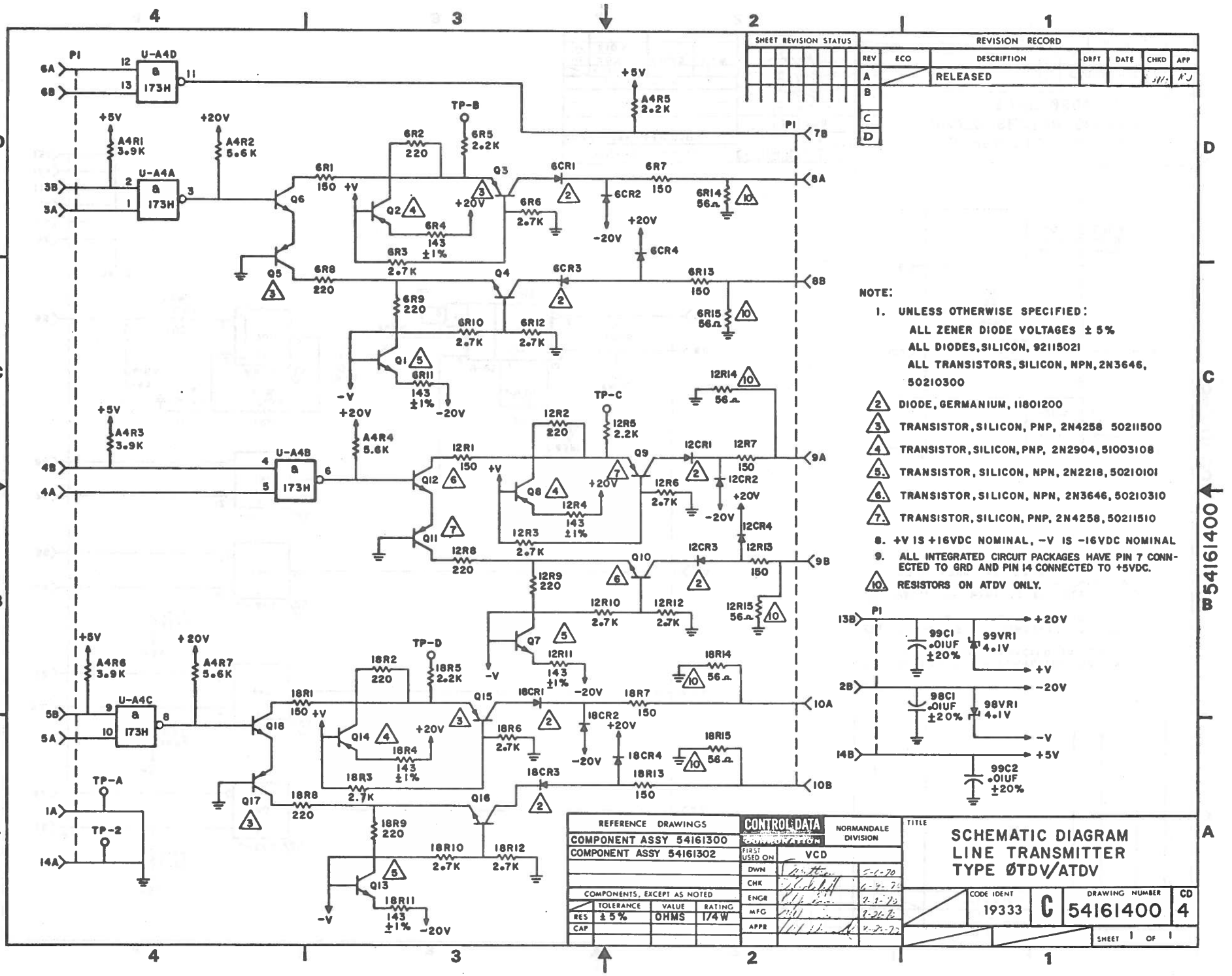
SHEET 1 OF 2

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHEET 1				



NORMANDALE DIVISION	SCHEMATIC DIAGRAM SWITCH RECEIVER TYPE ØSAV	CUSTOMER 19333 / C	DRAWING NO. 54150200 / C.D. 1
			SHEET 2

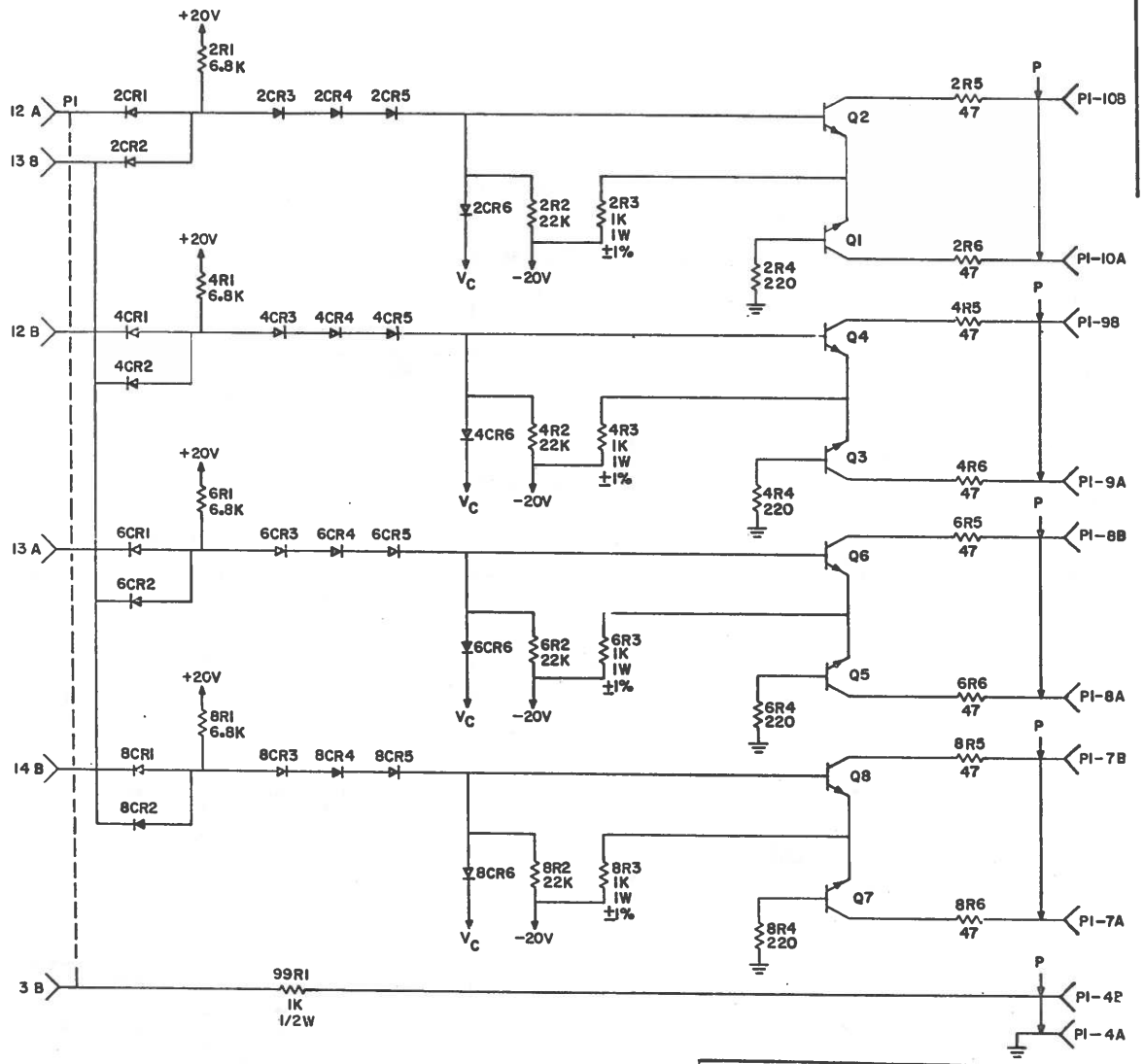

SCHEMATIC DIAGRAM
PHOTO SECTOR SENSOR
TYPE ØSBV
54150600
B54150600
NOTE:
1. IC HAS PIN 4 CONNECTED TO -5V AND PIN 7 CONNECTED TO +5V.
2. IC HAS PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
3. VALUE OF B3R1 TO BE SELECTED IN PRODUCTION TO GIVE A PULSE OF 55 US ±7US AT TP-A.
REFERENCE DRAWINGS
COMP ASSY: 54150500
RELEASED
BR2A5B
19333
U-A4A
U-A4B
U-A4C
U-A4D
AR-1
U-B3
TP-A
TP-B
TP-C
TP-Z
55US


SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | | RELEASED
B
C
D
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL ZENER DIODE VOLTAGES ± 5%
ALL DIODES, SILICON, 92115021
ALL TRANSISTORS, SILICON, NPN, 2N3646, 50210300
2 DIODE, GERMANIUM, 11801200
3 TRANSISTOR, SILICON, PNP, 2N4258 50211500
4 TRANSISTOR, SILICON, PNP, 2N2904, 51003108
5 TRANSISTOR, SILICON, NPN, 2N2218, 50210101
6 TRANSISTOR, SILICON, NPN, 2N3646, 50210310
7 TRANSISTOR, SILICON, PNP, 2N4258, 50211510
8. +V IS +16VDC NOMINAL, −V IS −16VDC NOMINAL
9. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5VDC.
10 RESISTORS ON ATDV ONLY.
U-A4D
U-A4A
U-A4B
U-A4C
173H
A4R1 3.9K
A4R2 5.6K
A4R3 3.9K
A4R4 5.6K
A4R5 2.2K
A4R6 3.9K
A4R7 5.6K
TP-A
TP-2
TP-B
TP-C
TP-D
99C1 .01UF ±20%
99VR1 4.1V
98C1 .01UF ±20%
98VR1 4.1V
99C2 .01UF ±20%
REFERENCE DRAWINGS
COMPONENT ASSY 54161300
COMPONENT ASSY 54161302
COMPONENTS, EXCEPT AS NOTED
RES ±5% OHMS 1/4W
CAP
CONTROL DATA CORPORATION
NORMANDALE DIVISION
FIRST USED ON VCD
DWN
CHK
ENGR
MFG
APPR
TITLE
SCHEMATIC DIAGRAM
LINE TRANSMITTER
TYPE ØTDV/ATDV
CODE IDENT 19333
C
DRAWING NUMBER 54161400
CD 4
SHEET 1 OF 1

54161400 B

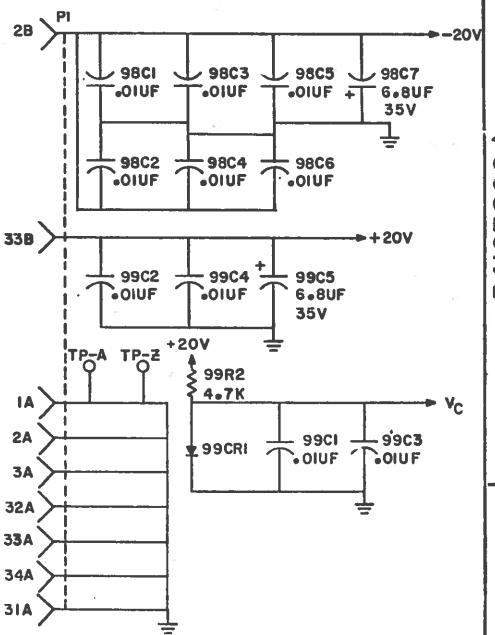
SHEET REVISION STATUS										

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	[illegible]	RELEASED			2-7-1	[illegible]



NOTE:

1. ALL TRANSISTORS, SILICON, NPN, 2N2221, 50210102.
2. ALL DIODE, SILICON, 24553500.



REFERENCE DRAWINGS
COMP ASSY 54163700

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5 %	OHMS	1/4W
CAP	±20%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	BR2A5B	
DWN	D. G. TUTTLE	2-8-71
CHK	H. Ha[illegible]	4-26-71
ENGR	A Peterson	4/26/71
MFG	[illegible]	11/30/71
APPR	[illegible]	4-30-71

TITLE

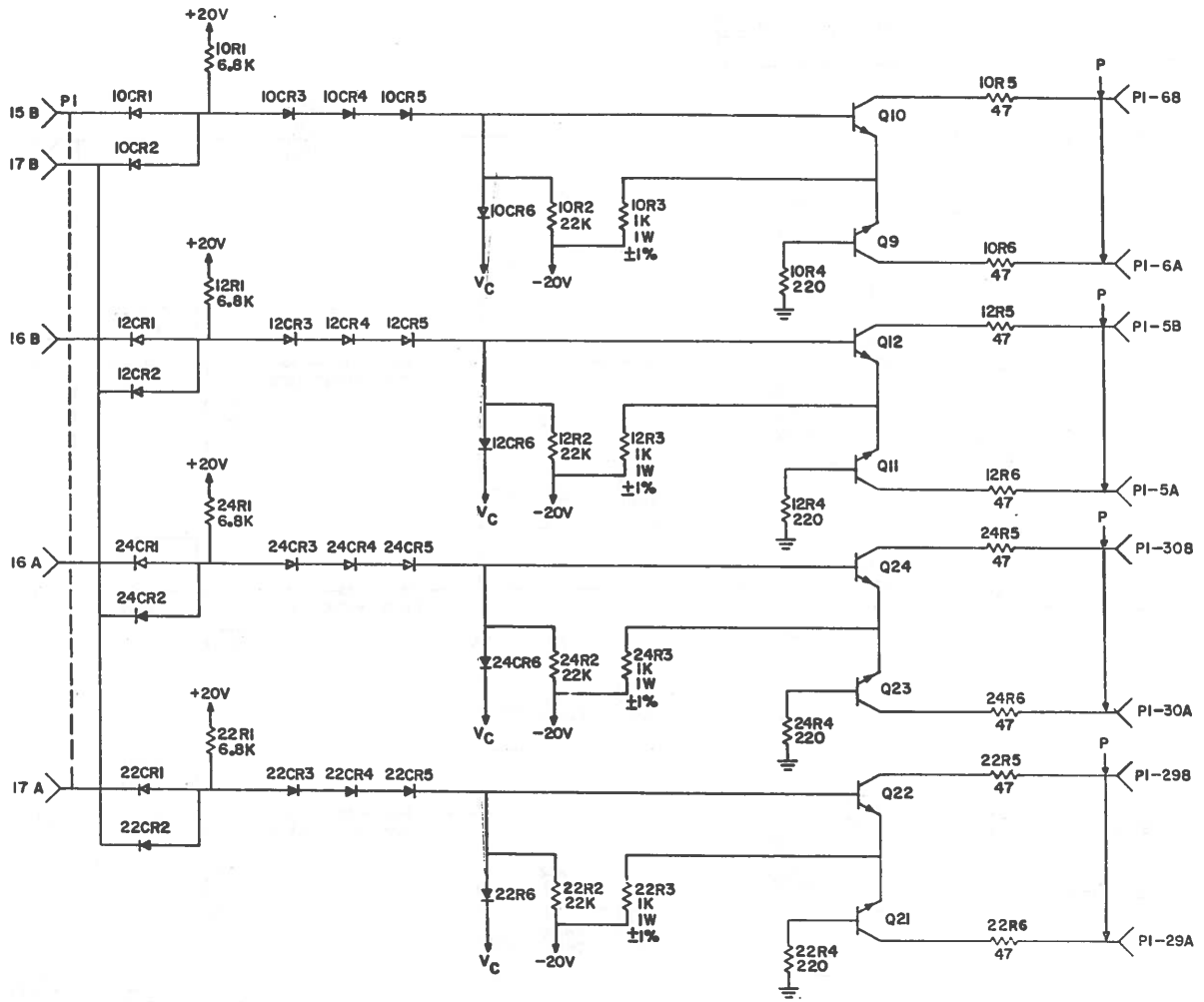
SCHEMATIC DIAGRAM 592 INTERFACE TRANSMITTER TYPE ØTKV

CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54163800	3

SHEET 1 OF 3

54163800 B

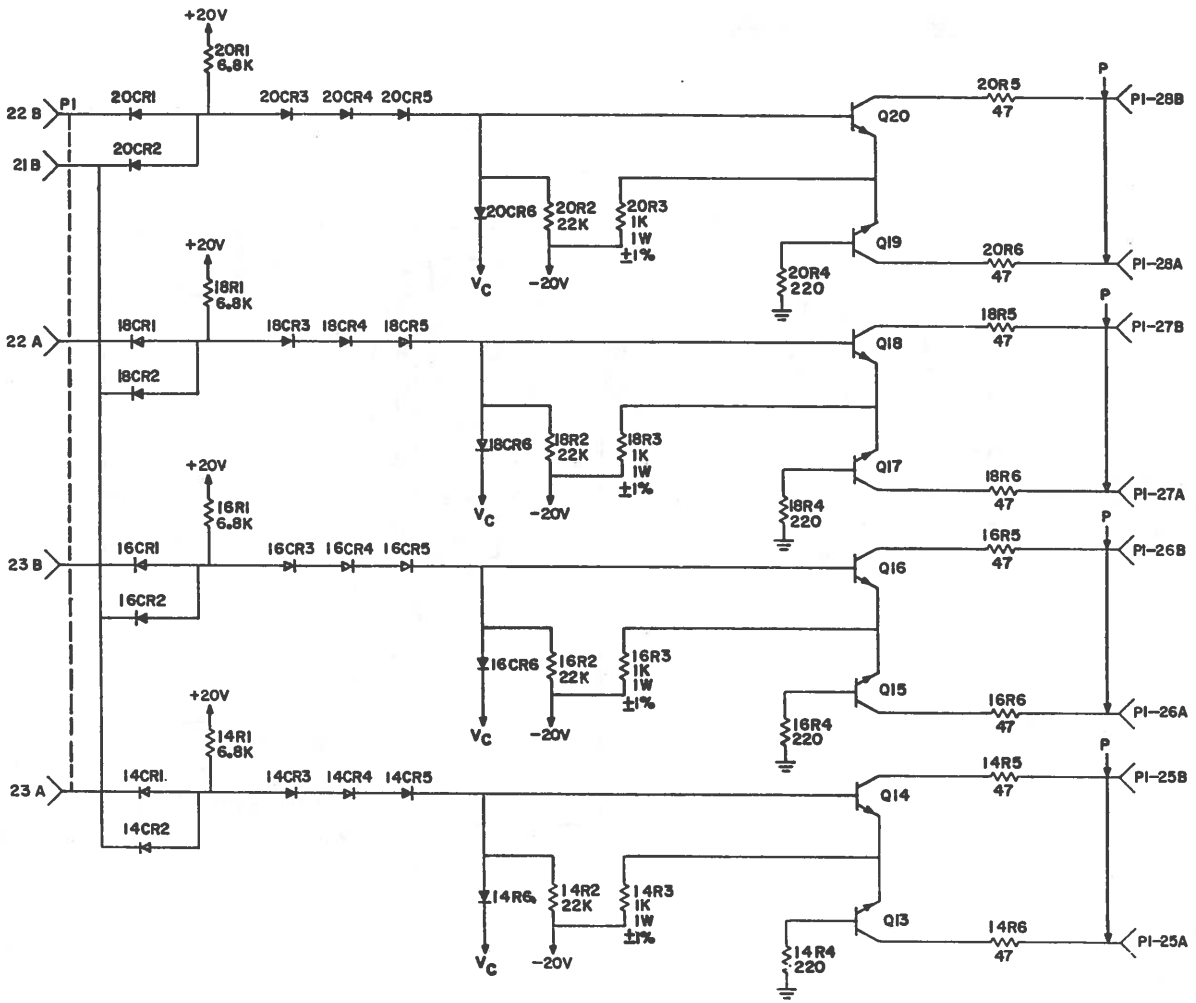
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SH 1 FOR REVISION				



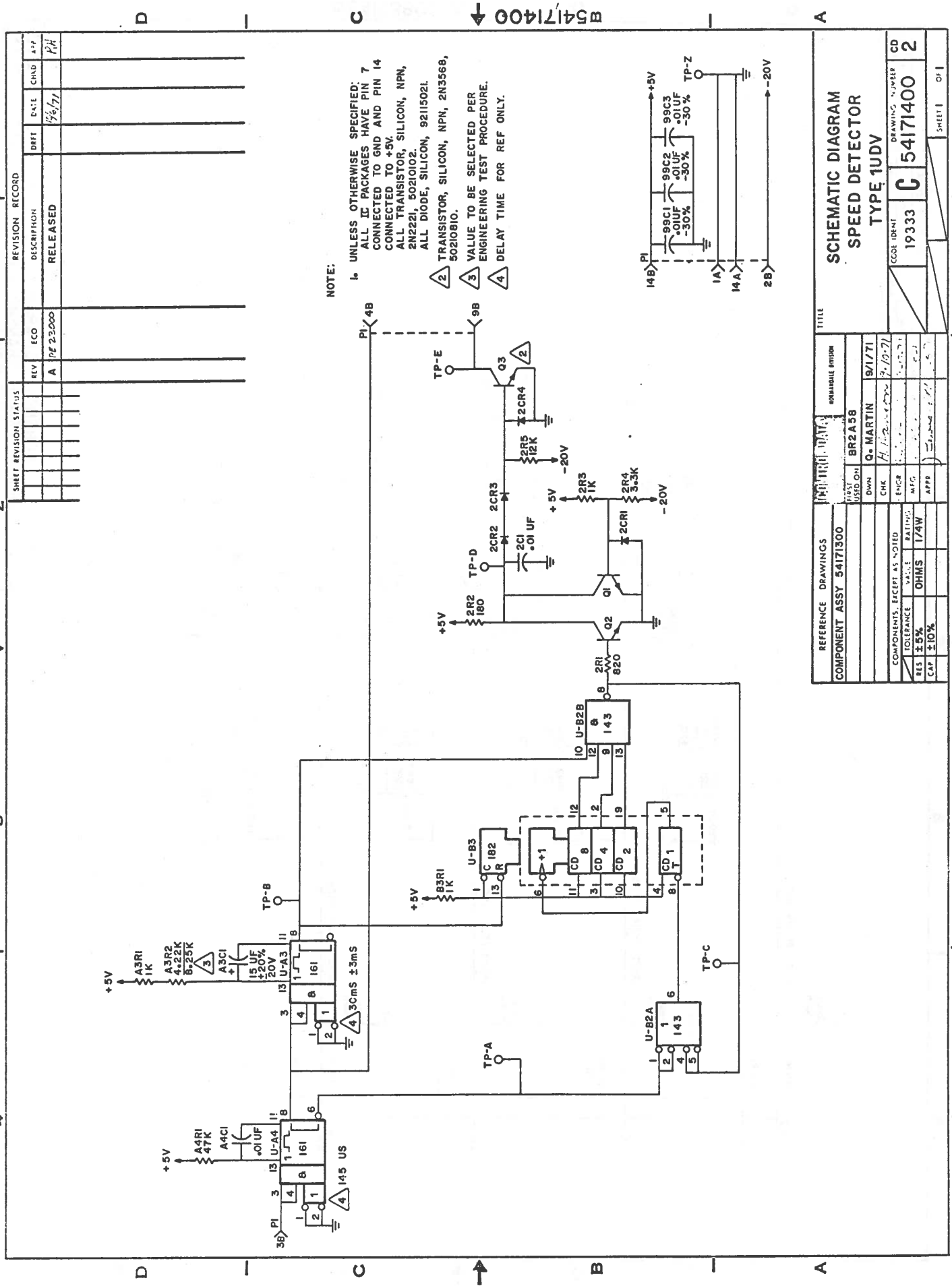
CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM 502 INTERFACE TRANSMITTER TYPE ØTKV	CODE IDENT 19333	C	DWG NO 54163800	C.D. 3
				SHEET 2	

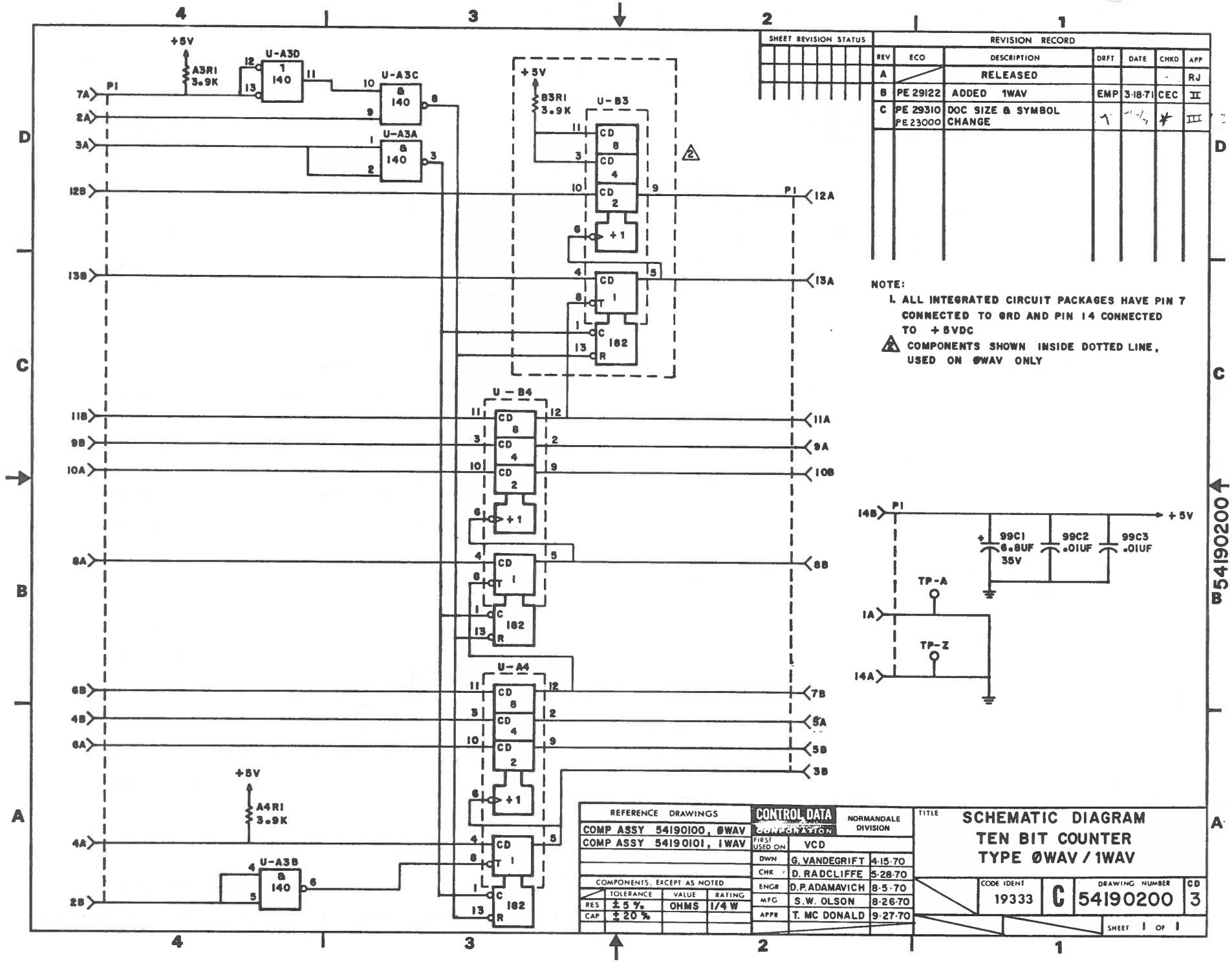
B 54163800

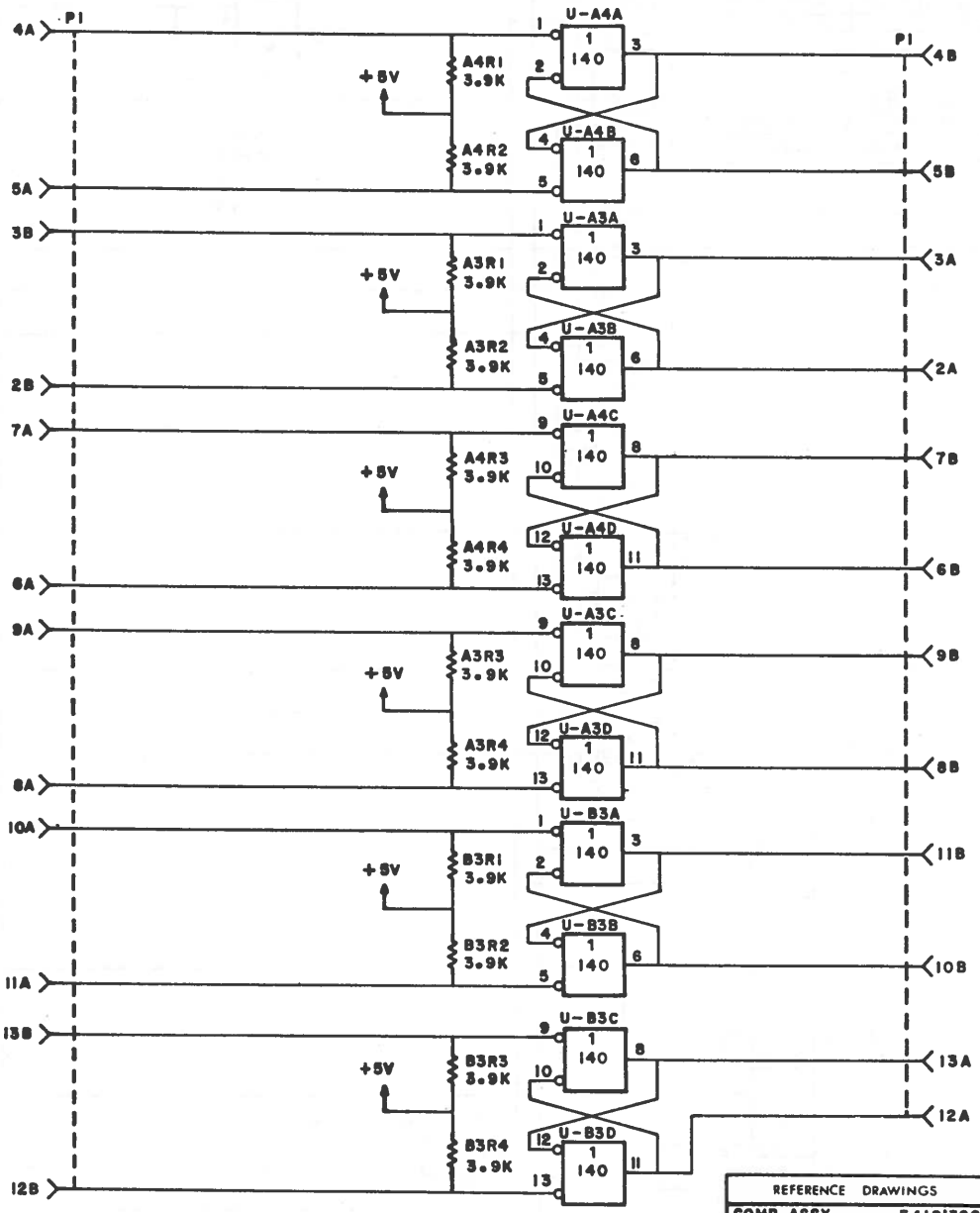
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SH 1 FOR REVISION				



CONTROL DATA	SCHEMATIC DIAGRAM 592 INTERFACE TRANSMITTER TYPE ØTKV	19333	C	54163800	C.D. 3
				3	


REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP'D
A
IDE 23000
RELEASED
9/6/71
SHEET REVISION STATUS
NOTE:
1. UNLESS OTHERWISE SPECIFIED: ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V. ALL TRANSISTOR, SILICON, NPN, 2N2222I, 50210102. ALL DIODE, SILICON, 9211502I.
2 TRANSISTOR, SILICON, NPN, 2N3568, 50210810.
3 VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
4 DELAY TIME FOR REF ONLY.
REFERENCE DRAWINGS
COMPONENT ASSY 54171300
FIRST USED ON
BR2A58
DWN
Q. MARTIN
9/1/71
CHK
9/13/71
ENGR
MFG
APPD
COMPONENTS, EXCEPT AS NOTED
TOLERANCE
VALUE
RATING
RES ±5%
OHMS
1/4W
CAP ±10%
TITLE
SCHEMATIC DIAGRAM
SPEED DETECTOR
TYPE 1UDV
CODE IDENT
19333
C
DRAWING NUMBER
54171400
CD
2
SHEET 1 OF 1
P1
TP-A
TP-B
TP-C
TP-D
TP-E
TP-Z
+5V
-20V
A3R1 1K
A3R2 4.22K 8.25K
A3C1 15 UF ±20% 20V
A4R1 47K
A4C1 .01 UF
2R1 220 820
2R2 180
2R3 1K
2R4 3.3K
2R5 12K
2C1 .01 UF
99C1 .01UF -30%
99C2 .01UF -30%
99C3 .01UF -30%
2CR1
2CR2
2CR3
2CR4
Q1
Q2
Q3
U-A3
U-A4
U-B2A
U-B2B
U-B3
161
143
182
CD 8
CD 4
CD 2
CD 1
+1
30mS ±3mS
145 US


+5V
A3R1
3.9K
U-A3D
U-A3C
U-A3A
U-A3B
A4R1
3.9K
B3R1
3.9K
U-B3
U-B4
U-A4
CD 8
CD 4
CD 2
CD 1
+1
T
C
R
162
140
P1
7A
2A
3A
12B
13B
11B
9B
10A
8A
6B
4B
6A
4A
2B
12A
13A
11A
9A
10B
8B
7B
5A
5B
3B
SHEET REVISION STATUS
REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
A
RELEASED
RJ
B
PE 29122
ADDED 1WAV
EMP
3-18-71
CEC
C
PE 29310
PE 23000
DOC SIZE & SYMBOL CHANGE
NOTE:
1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5VDC
2 COMPONENTS SHOWN INSIDE DOTTED LINE, USED ON ØWAV ONLY
14B
14A
1A
TP-A
TP-Z
99C1
6.8UF
35V
99C2
.01UF
99C3
.01UF
REFERENCE DRAWINGS
COMP ASSY 54190100, ØWAV
COMP ASSY 54190101, 1WAV
COMPONENTS, EXCEPT AS NOTED
TOLERANCE
VALUE
RATING
RES
±5%
OHMS
1/4 W
CAP
±20%
CONTROL DATA CORPORATION
NORMANDALE DIVISION
FIRST USED ON
VCD
DWN
G. VANDEGRIFT
4-15-70
CHK
D. RADCLIFFE
5-28-70
ENGR
D.P.ADAMAVICH
8-5-70
MFG
S.W. OLSON
8-26-70
APPR
T. MC DONALD
9-27-70
TITLE
SCHEMATIC DIAGRAM
TEN BIT COUNTER
TYPE ØWAV / 1WAV
CODE IDENT
19333
C
DRAWING NUMBER
54190200
CD
3
SHEET 1 OF 1
B 54190200 A

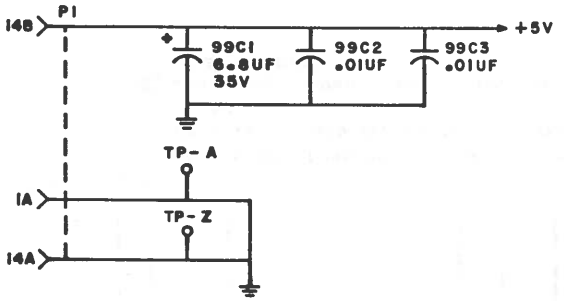


SHEET REVISION STATUS								

REVISION RECORD							
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED				RJ
B	PE29310 PE23000	DOC SIZE & SYMBOL CHANGE	J.R.	4/17/71		III

NOTE:

1. ALL INTEGRATED PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5V



REFERENCE DRAWINGS	
COMP ASSY	54191300

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	± 5 %	OHMS	1/4 W
CAP	± 20 %		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	VCD	
DWN	J. E. MATTSON	4-8-70
CHK	R. BOCHE	6-5-70
ENGR	D.P. ADAMAVICH	8-5-70
MFG	S.W. OLSON	8-26-70
APPR	T. MC DONALD	8-27-70

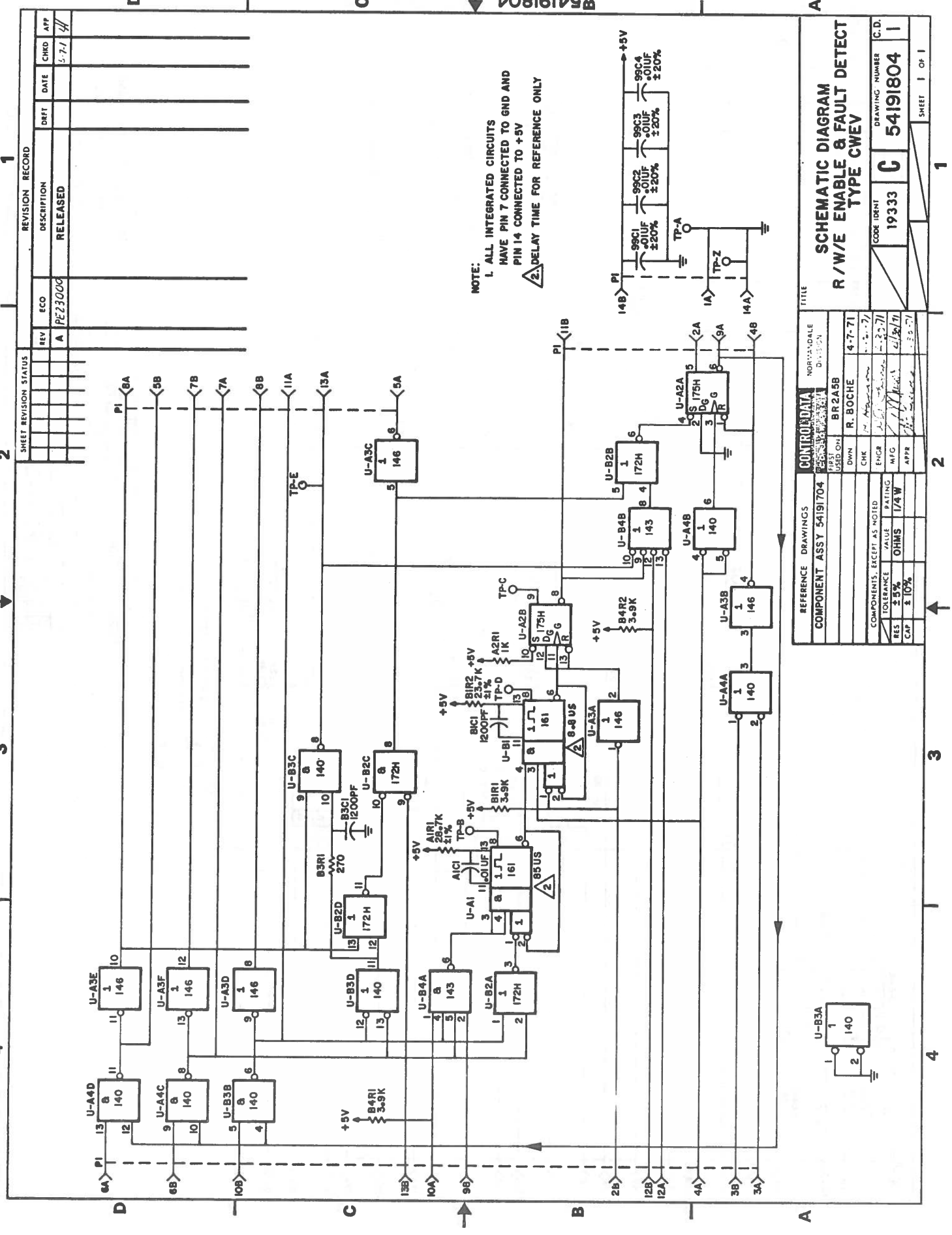
TITLE

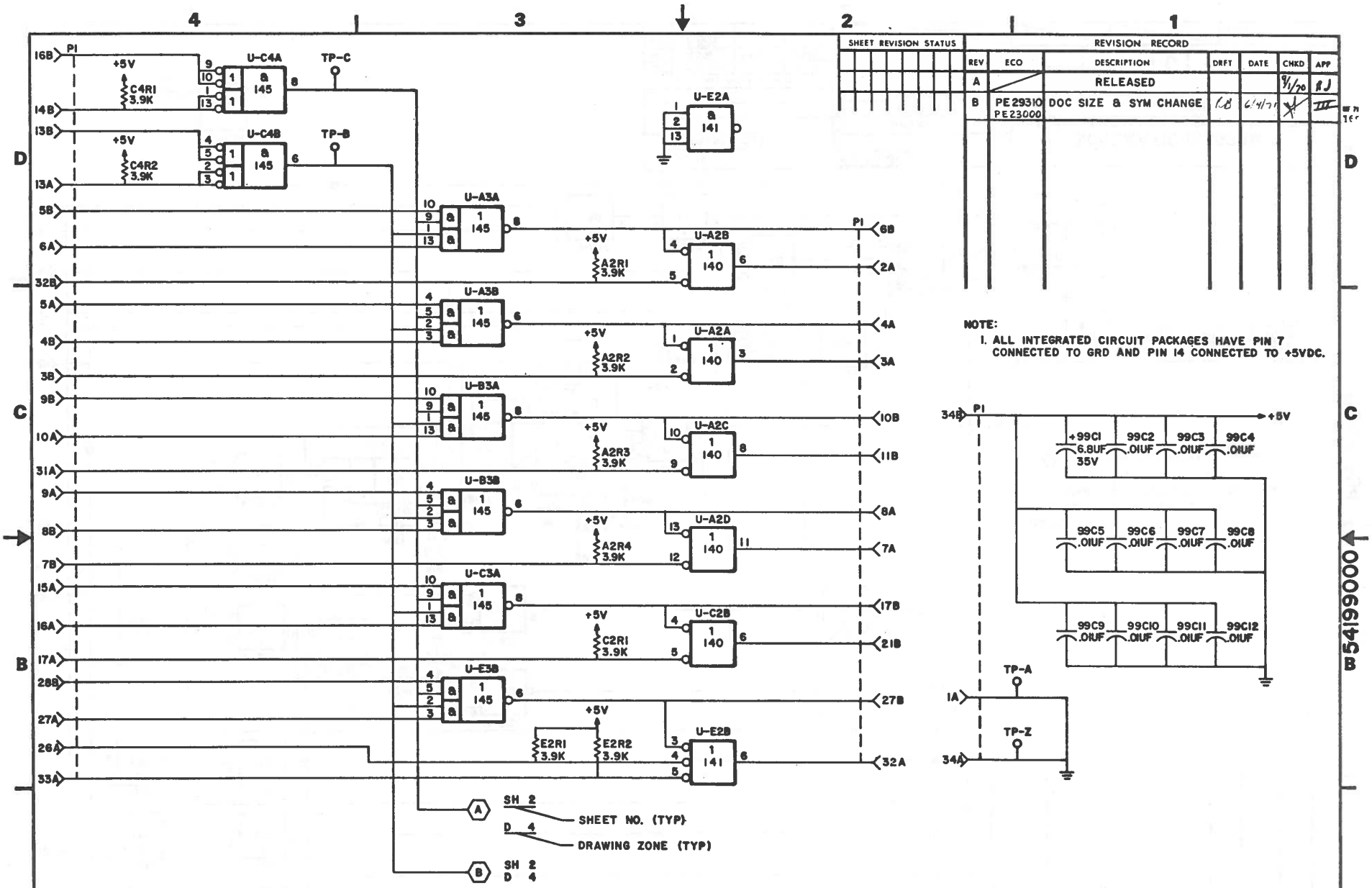
SCHEMATIC DIAGRAM
FAULT REGISTER
TYPE ØWDV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54191400	8

SHEET 1 OF 1

B 54191400


54191804
REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
A
PE23000
RELEASED
SHEET REVISION STATUS
NOTE:
1. ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
2. DELAY TIME FOR REFERENCE ONLY
SCHEMATIC DIAGRAM
R/W/E ENABLE & FAULT DETECT
TYPE CWEV
CONTROL DATA
NORTHDALE
REFERENCE DRAWINGS
COMPONENT ASSY 54191704
BR 2A5B
R. BOCHE
4-7-71
CODE IDENT
19333
DRAWING NUMBER
54191804
C.D.
SHEET 1 OF 1
COMPONENTS, EXCEPT AS NOTED
TOLERANCE
RES ±5%
CAP ±10%
VALUE
OHMS
RATING
1/4 W
+5V
99C1 .01UF ±20%
99C2 .01UF ±20%
99C3 .01UF ±20%
99C4 .01UF ±20%
TP-A
TP-Z
TP-E
TP-C
TP-D
TP-B
B4R2 3.9K
B2R2 23.7K ±1%
A2R1 1K
B1R2 3.9K
A1R1 28.7K ±1%
B4R1 3.9K
B3R1 270
B1C1 .01UF
B2C1 120PF
B3C1 120PF
A1C1 .01UF
B1C1 1200PF
U-A3C 1 146
U-B2B 1 172H
U-A2A S 175H
U-B4B 1 143
U-A4B 1 140
U-A3B 1 146
U-A4A 1 140
U-A2B S 175H
U-B2C 8 172H
U-B3C 8 140
U-A3A 1 146
U-B1 8 161
U-A1 8 161
U-B2D 1 172H
U-B3D 1 140
U-B4A 8 143
U-B2A 1 172H
U-A3E 1 146
U-A3F 1 146
U-A3D 1 146
U-A4D 8 140
U-A4C 8 140
U-B3B 8 140
U-B3A 1 140
8-8 US
85 US
P1
8A
5B
7B
7A
8B
11A
13A
5A
11B
2A
9A
4B
14B
1A
14A
6A
6B
10B
13B
10A
9B
2B
12B
12A
4A
3B
3A



SHEET REVISION STATUS

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED			9/1/70	RJ
B	PE 29310 PE 23000	DOC SIZE & SYM CHANGE	LB	6/4/71		

NOTE:
1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5VDC.

REFERENCE DRAWINGS
COMPONENT ASSEMBLY 54198900

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±20%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

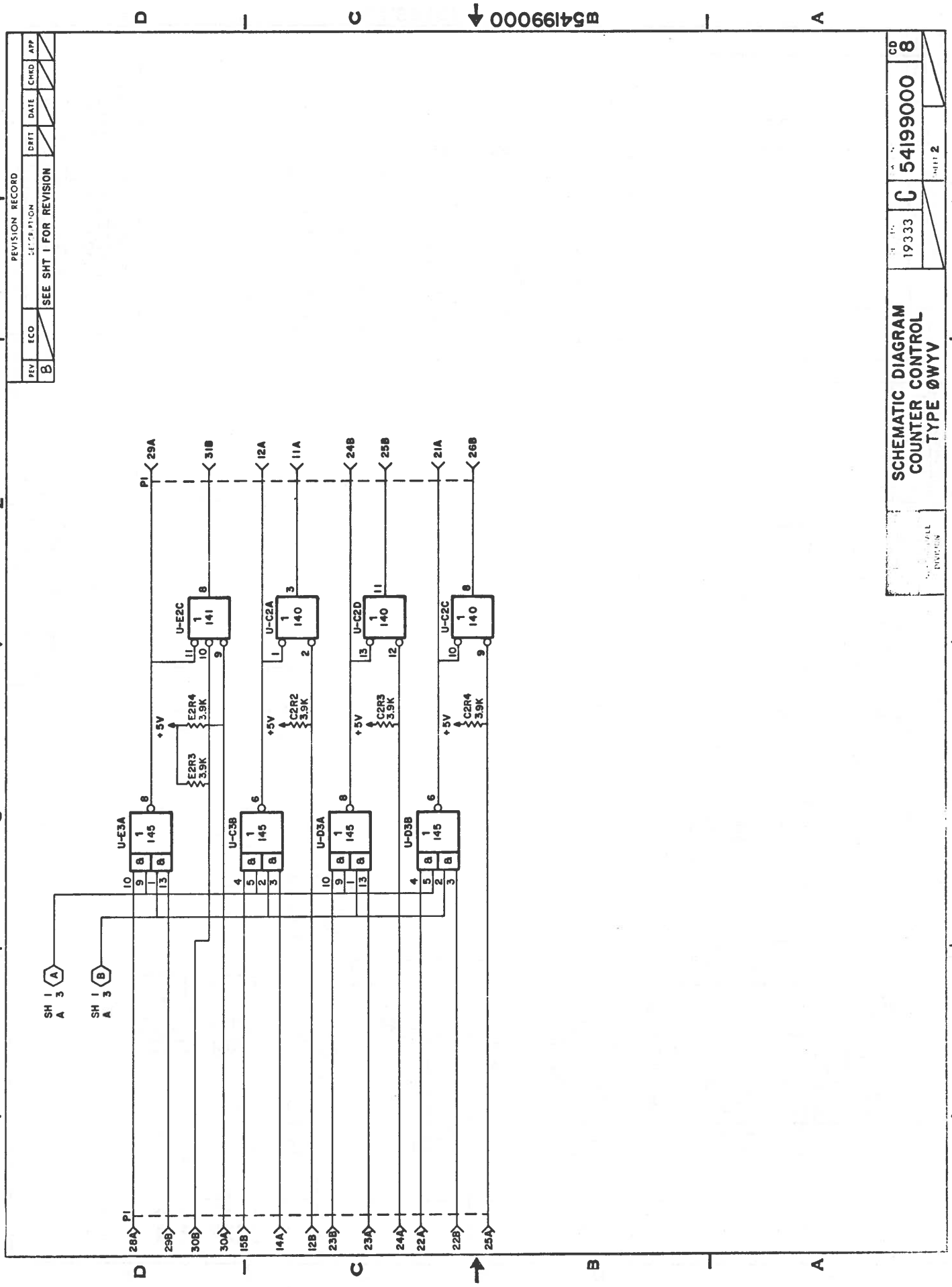
FIRST USEE PIN	VCD	
DWN	Vandergrift	4-15-70
CHK	Ratcliffe	5-27-70
ENGR	Nielsen	7-27-70
MFG	Wilson	8/12/70
APPR	T McDonald	9/27/70

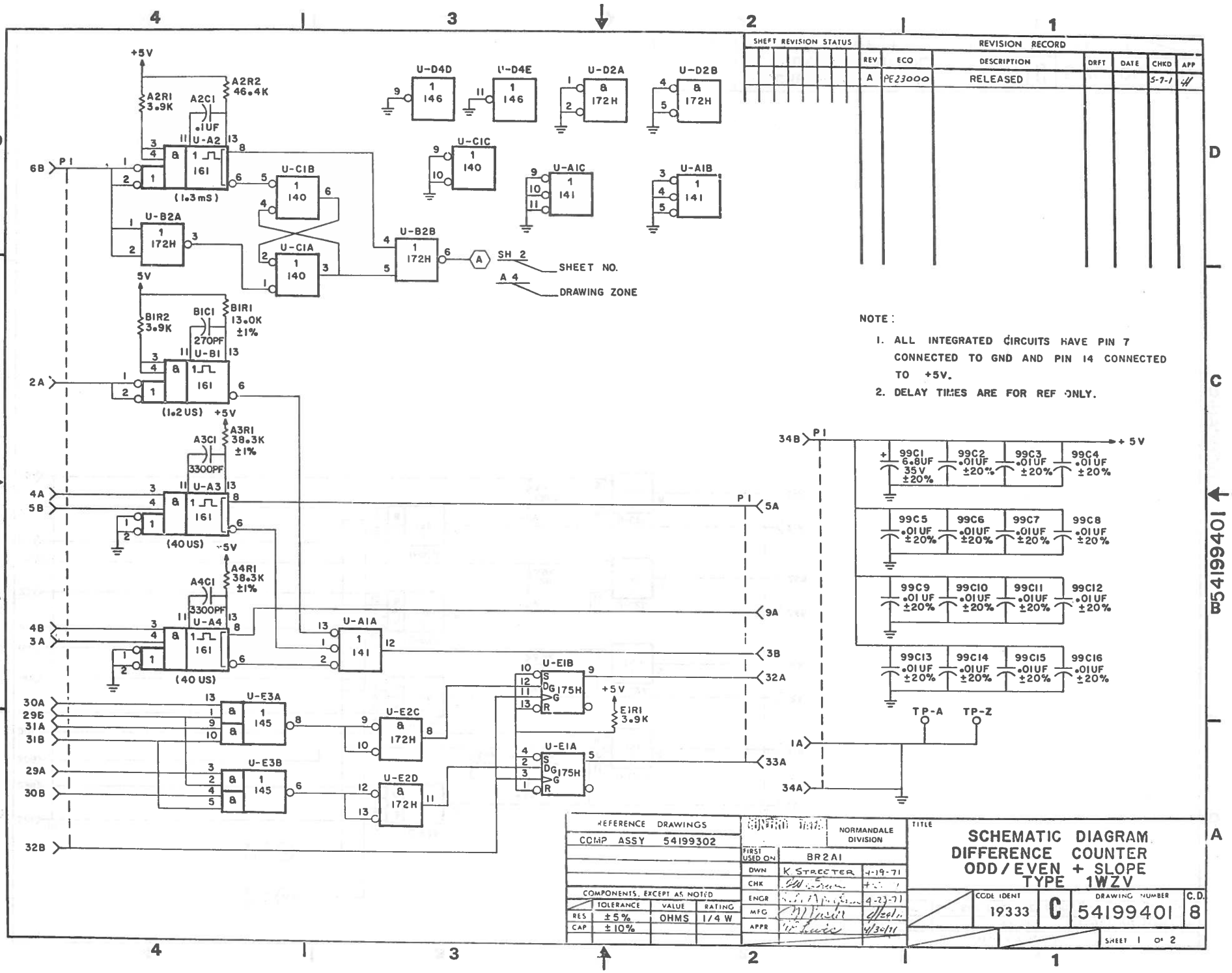
TITLE
SCHEMATIC DIAGRAM COUNTER CONTROL TYPE ØWYV

CODE IDENT 19333 | C | DRAWING NUMBER 54199000 | CD 8

SHEET 1 OF 2

54199000 B


REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
B
SEE SHT 1 FOR REVISION
SCHEMATIC DIAGRAM
COUNTER CONTROL
TYPE ØWYV
54199000
19333
C
CD 8
SHT 2
U-E3A
U-C3B
U-D3A
U-D3B
U-E2C
U-C2A
U-C2D
U-C2C
+5V
E2R4 3.9K
E2R3 3.9K
C2R2 3.9K
C2R3 3.9K
C2R4 3.9K
SH 1 A 3
SH 1 A 3
P1
29A
31B
12A
11A
24B
25B
21A
26B
28A
29B
30B
30A
15B
14A
12B
23B
23A
24A
22A
22B
25A



SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED			5-7-71	

NOTE:

1. ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. DELAY TIMES ARE FOR REF ONLY.

REFERENCE DRAWINGS
COMP ASSY 54199302

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA NORMANDALE DIVISION

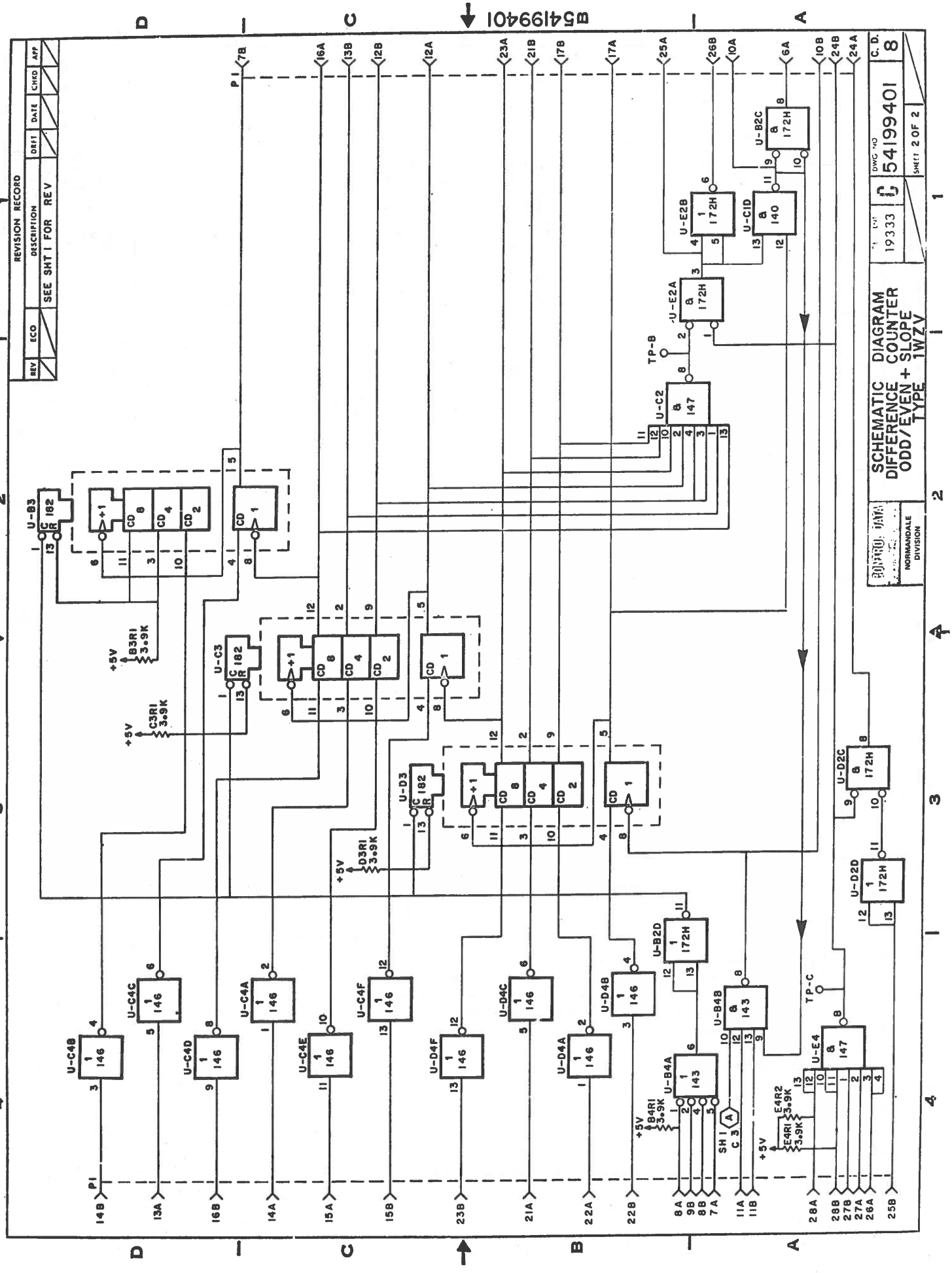
FIRST USED ON	BR2A1	
DWN	K STREETER	4-19-71
CHK		
ENGR		4-23-71
MFG		
APPR		4/30/71

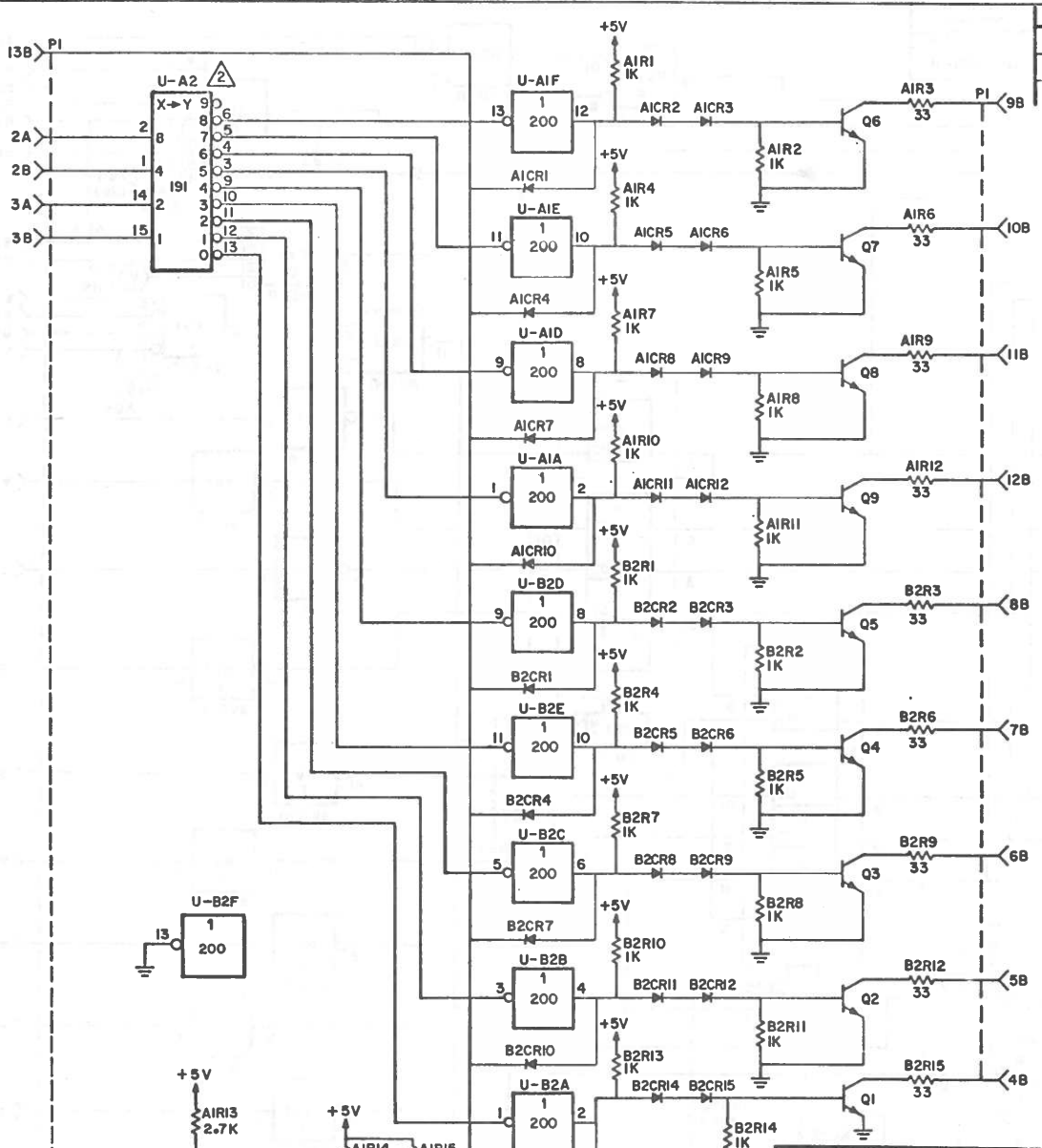
TITLE

SCHEMATIC DIAGRAM DIFFERENCE COUNTER ODD / EVEN + SLOPE TYPE 1WZV

CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54199401	8

SHEET 1 OF 2


SCHEMATIC DIAGRAM
DIFFERENCE COUNTER
ODD/EVEN + SLOPE
TYPE 1WZV
NORMANDALE DIVISION
DWG NO 54199401
SHEET 2 OF 2
C.D. 8
REVISION RECORD
REV
ECO
DESCRIPTION
SEE SHT 1 FOR REV
DRFT
DATE
CHKD
APP
54199401

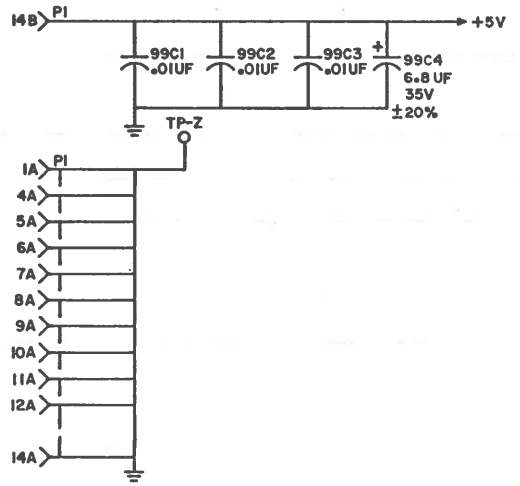


SHEET REVISION STATUS							

REVISION RECORD							
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	[illegible]	RELEASED		9-/-71		RH	

NOTE:

1. UNLESS OTHERWISE SPECIFIED
   ALL TRANSISTORS, SNPN, 2N2221, 50210102.
   ALL DIODES, SILICON, 92115021.
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. IC TYPE 191, HAS PIN 8 CONNECTED TO GND AND PIN 16 TO +5V.
3. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS
COMP ASS'Y 54210101

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR2A5B	
DWN	R. BOCHE	9-23-71
CHK	H. Hanson	9-27-71
ENGR	W.S.B.	9.27.71
MFG	[illegible]	9/29/71
APPR	[illegible]	9-29-71

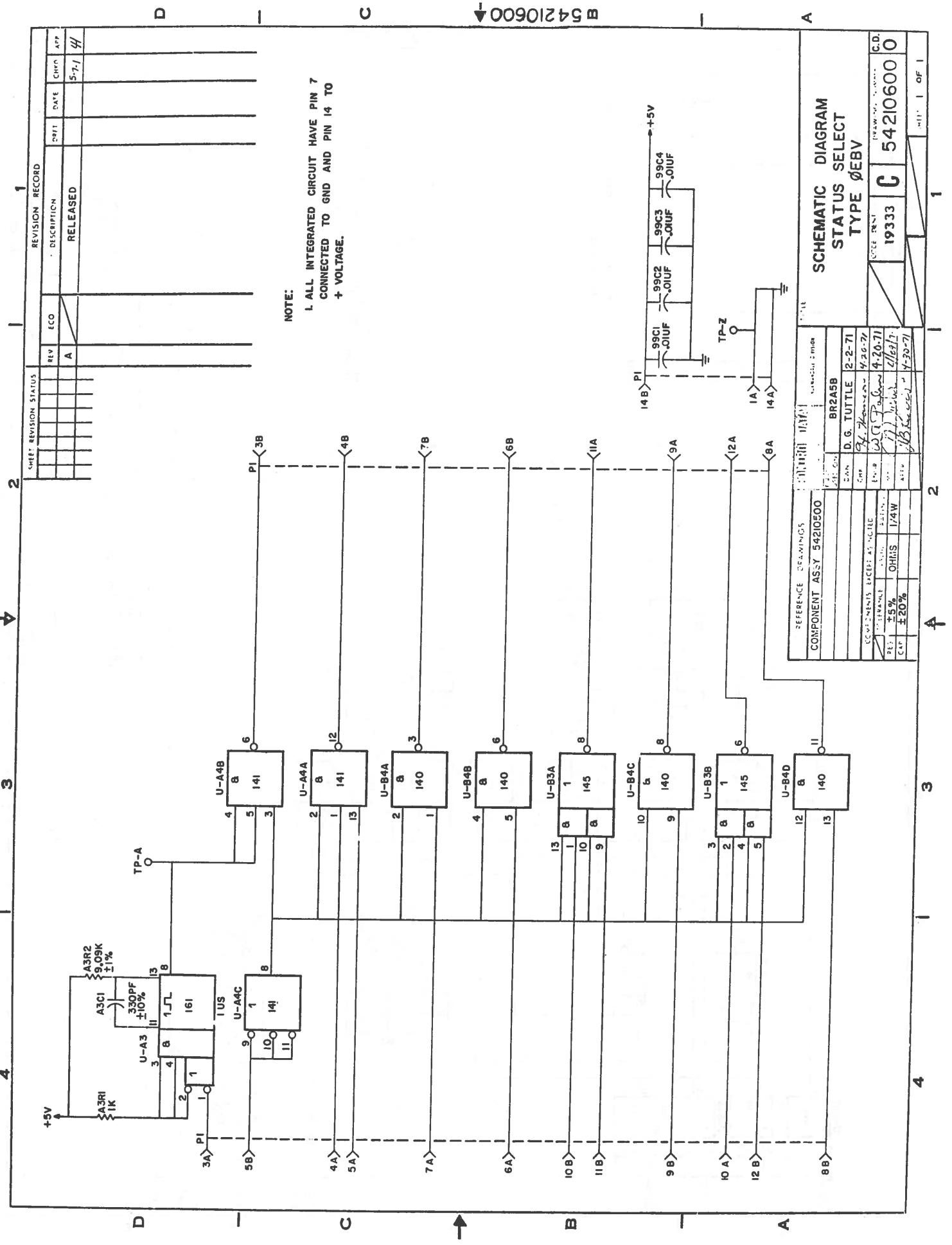
TITLE

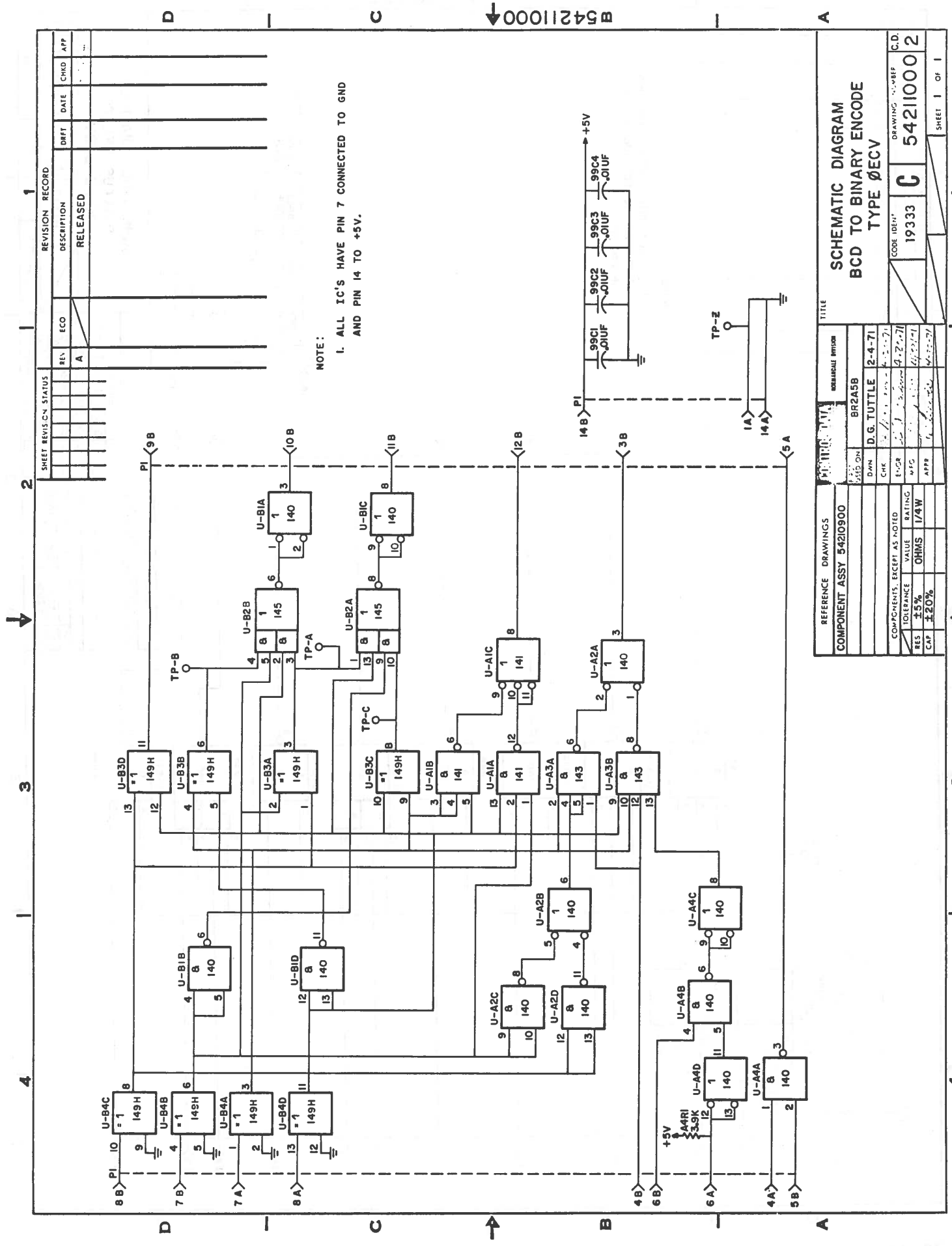
SCHMATIC DIAGRAM DEVICE ADDRESS TYPE 1EAV

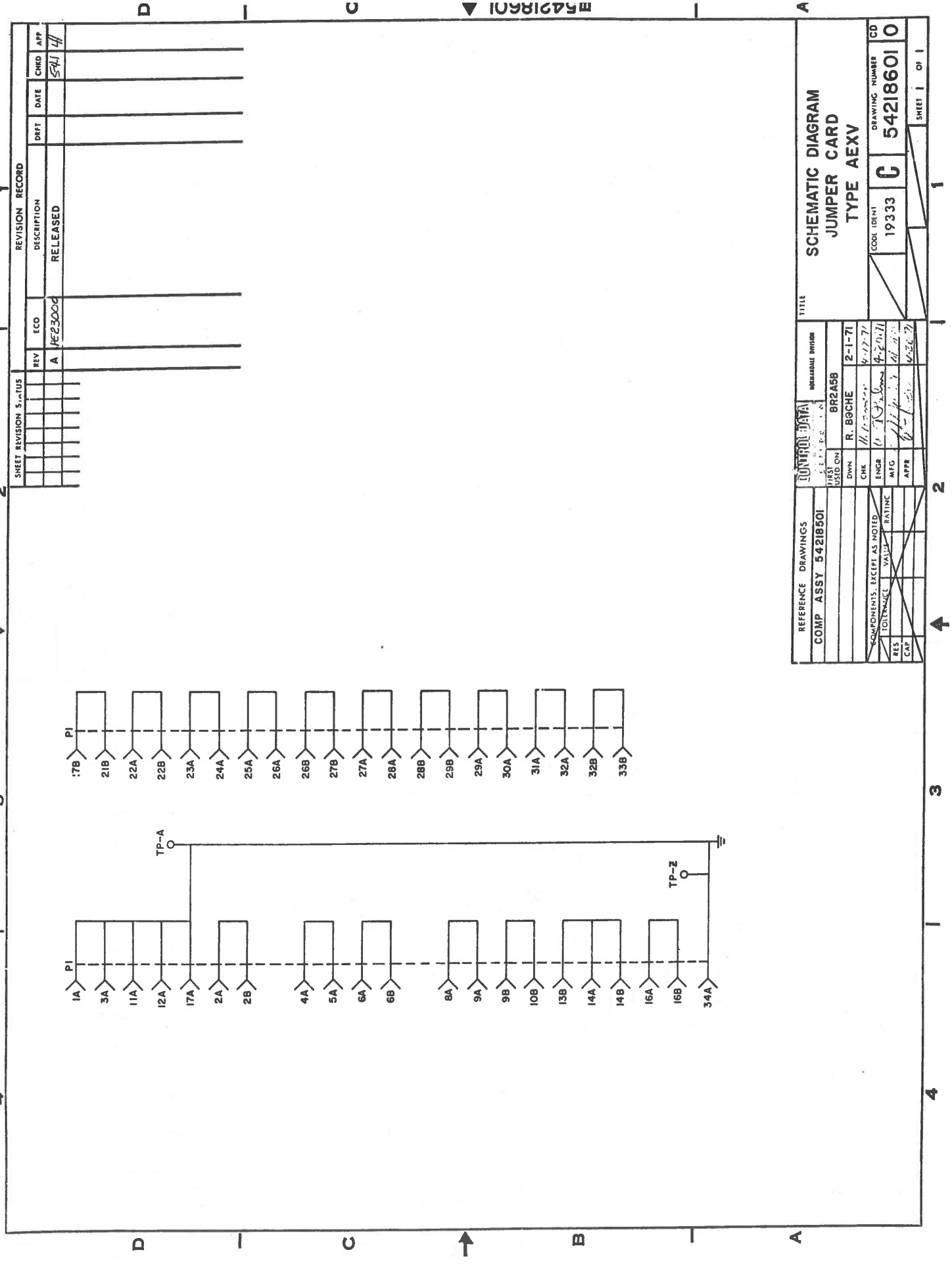
CODE IDENT		DRAWING NUMBER	CD
19333	C	54210201	7

SHEET 1 OF 1

VCD


SCHEMATIC DIAGRAM
STATUS SELECT
TYPE ØEBV
54210600
REVISION RECORD
RELEASED
NOTE:
1. ALL INTEGRATED CIRCUIT HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO + VOLTAGE.
COMPONENT ASSY 54210500
BR2A5B
D.G. TUTTLE
+5V
TP-A
TP-Z
U-A4B
U-A4A
U-B4A
U-B4B
U-B3A
U-B4C
U-B3B
U-B4D
U-A3
U-A4C
A3R2 9.09K ±1%
A3C1 330PF ±10%
A3R1 1K


SCHEMATIC DIAGRAM
BCD TO BINARY ENCODE
TYPE ØECV
54211000
NOTE:
1. ALL IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.
REVISION RECORD
SHEET REVISION STATUS
REFERENCE DRAWINGS
COMPONENT ASSY 54210900
BR2A5B
D.G. TUTTLE
2-4-71
TP-A
TP-B
TP-C
TP-Z
+5V
99C1 .01UF
99C2 .01UF
99C3 .01UF
99C4 .01UF
U-B1A
U-B1B
U-B1C
U-B1D
U-B2A
U-B2B
U-B3A
U-B3B
U-B3C
U-B3D
U-A1A
U-A1B
U-A1C
U-A2A
U-A2B
U-A2C
U-A2D
U-A3A
U-A3B
U-A4A
U-A4B
U-A4C
U-A4D
U-B4A
U-B4B
U-B4C
U-B4D
A4R1 3.9K


REVISION RECORD
SHEET REVISION STATUS
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
A
ME23000
RELEASED
SAJ
4/
REFERENCE DRAWINGS
COMP ASSY 54218501
FIRST USED ON
BR2A5B
DWN
R. B9CHE
2-1-71
CHK
ENGR
MFG
APPR
COMPONENTS EXCEPT AS NOTED
TOLERANCE
VALUE
RATING
RES
CAP
TITLE
SCHEMATIC DIAGRAM
JUMPER CARD
TYPE AEXV
CODE IDENT
19333
SIZE
C
DRAWING NUMBER
54218601
CD
0
SHEET 1 OF 1
P1
17B
21B
22A
22B
23A
24A
25A
26A
26B
27B
27A
28A
28B
29B
29A
30A
31A
32A
32B
33B
TP-A
TP-Z
P1
1A
3A
11A
12A
17A
2A
2B
4A
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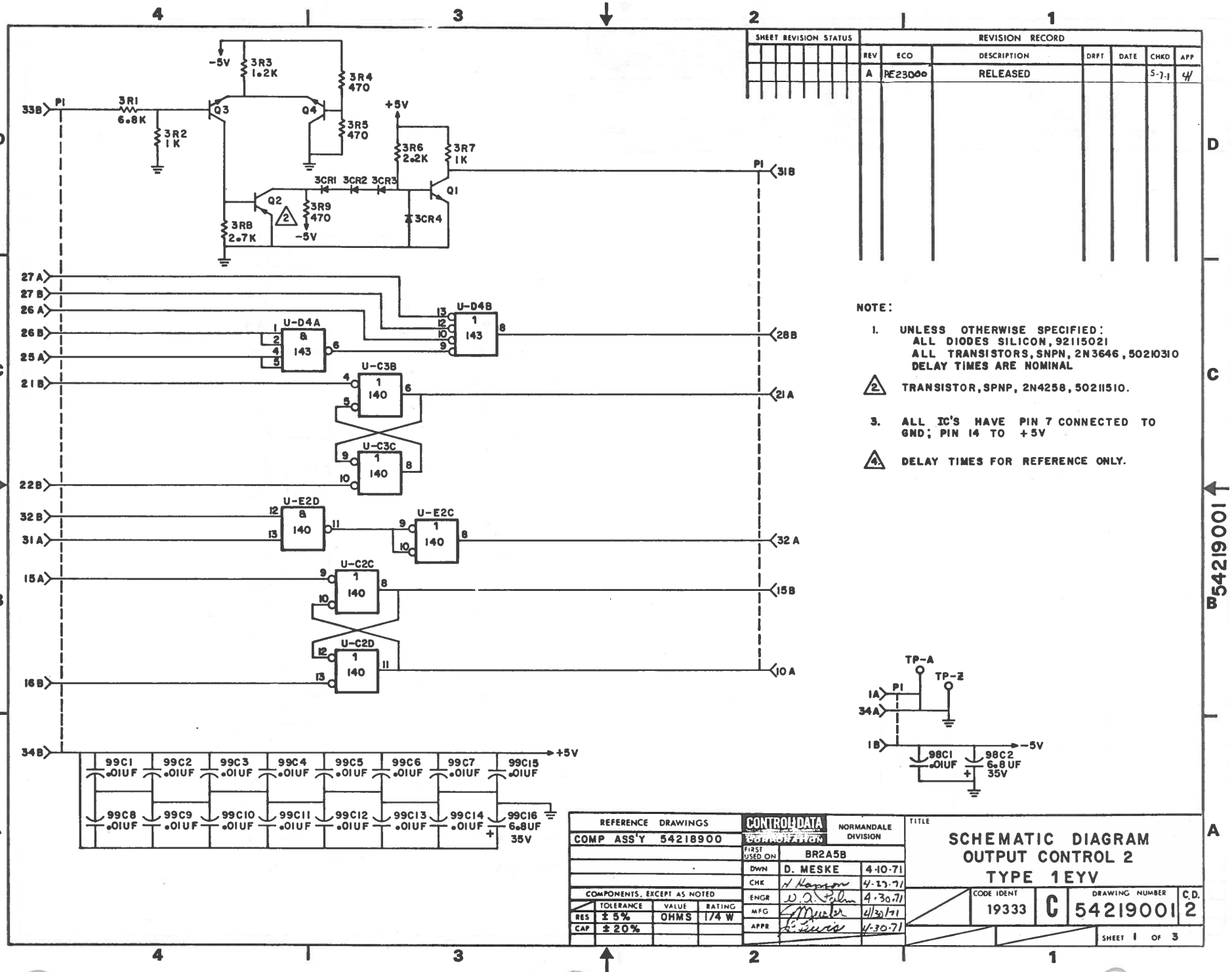
6A
6B
8A
9A
9B
10B
13B
14A
14B
16A
16B
34A



SHEET REVISION STATUS

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	RE23000	RELEASED			5-7-1	4/

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL DIODES SILICON, 92115021
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   DELAY TIMES ARE NOMINAL
2. TRANSISTOR, SPNP, 2N4258, 50211510.
3. ALL IC'S HAVE PIN 7 CONNECTED TO GND; PIN 14 TO +5V
4. DELAY TIMES FOR REFERENCE ONLY.

REFERENCE DRAWINGS
COMP ASS'Y 54218900

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4 W
CAP	± 20%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

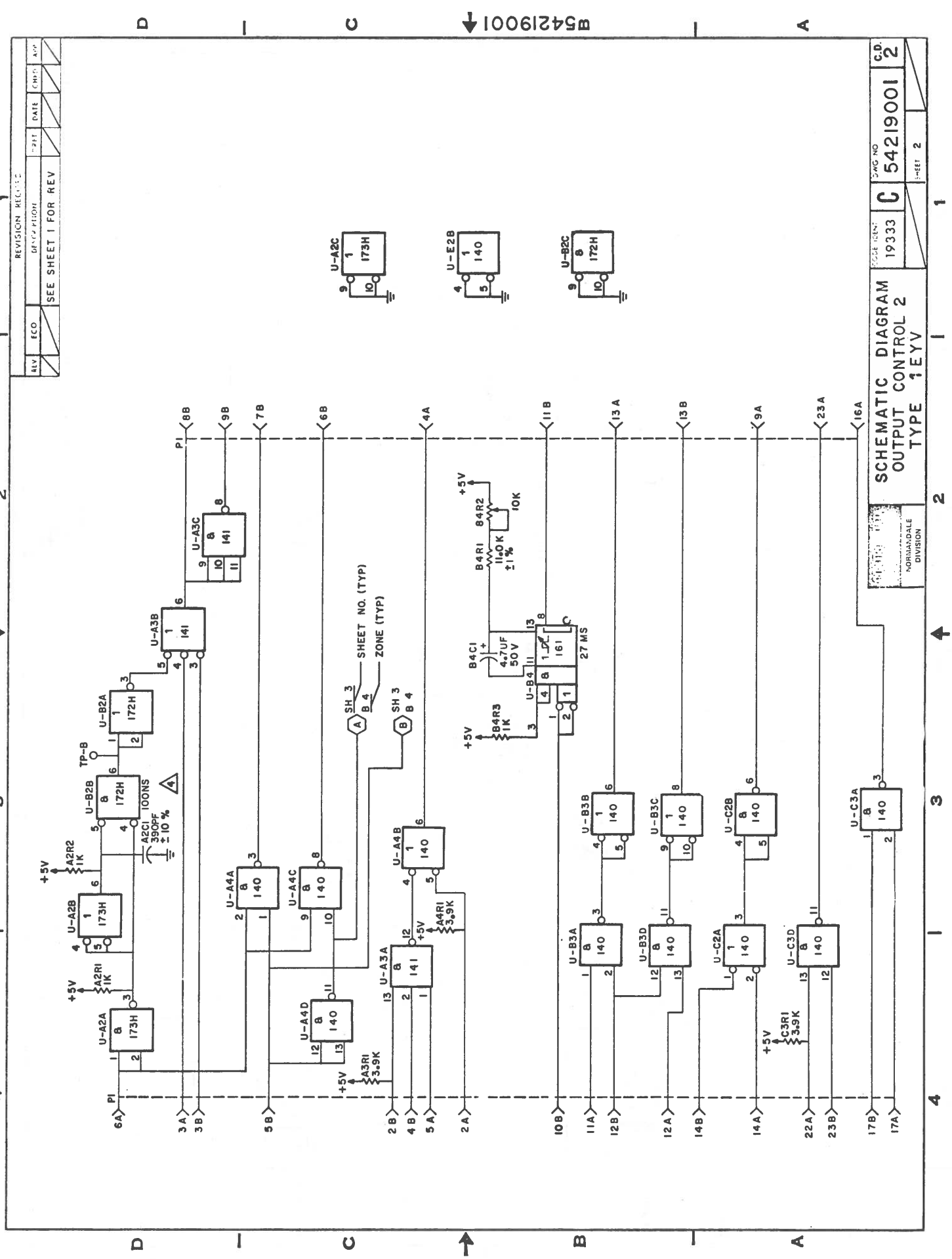
FIRST USED ON	BR2A5B	
DWN	D. MESKE	4-10-71
CHK	N Hanson	4-27-71
ENGR	W D Palm	4-30-71
MFG	F Mueller	4/30/71
APPR	L Lewis	4-30-71

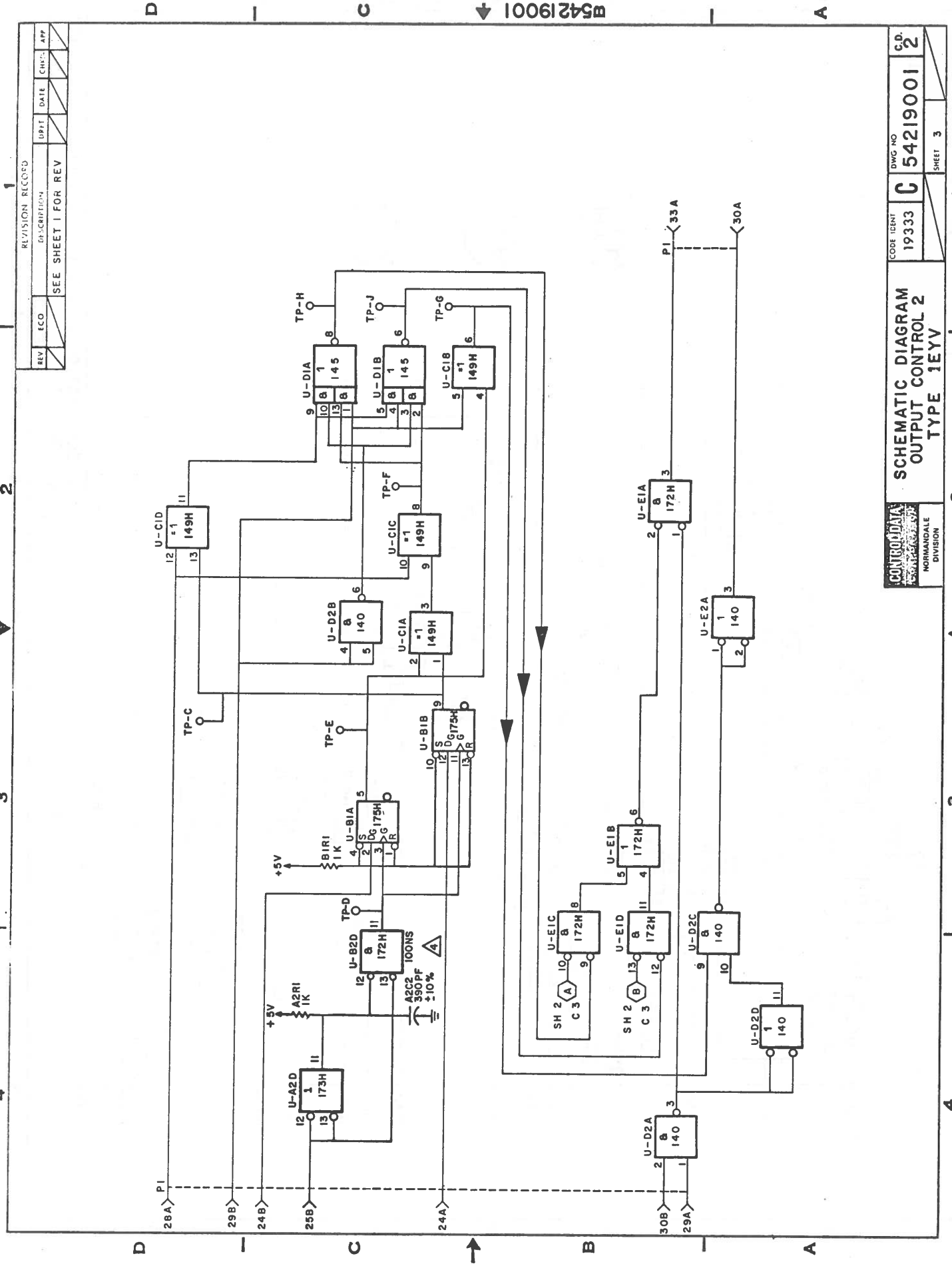
TITLE

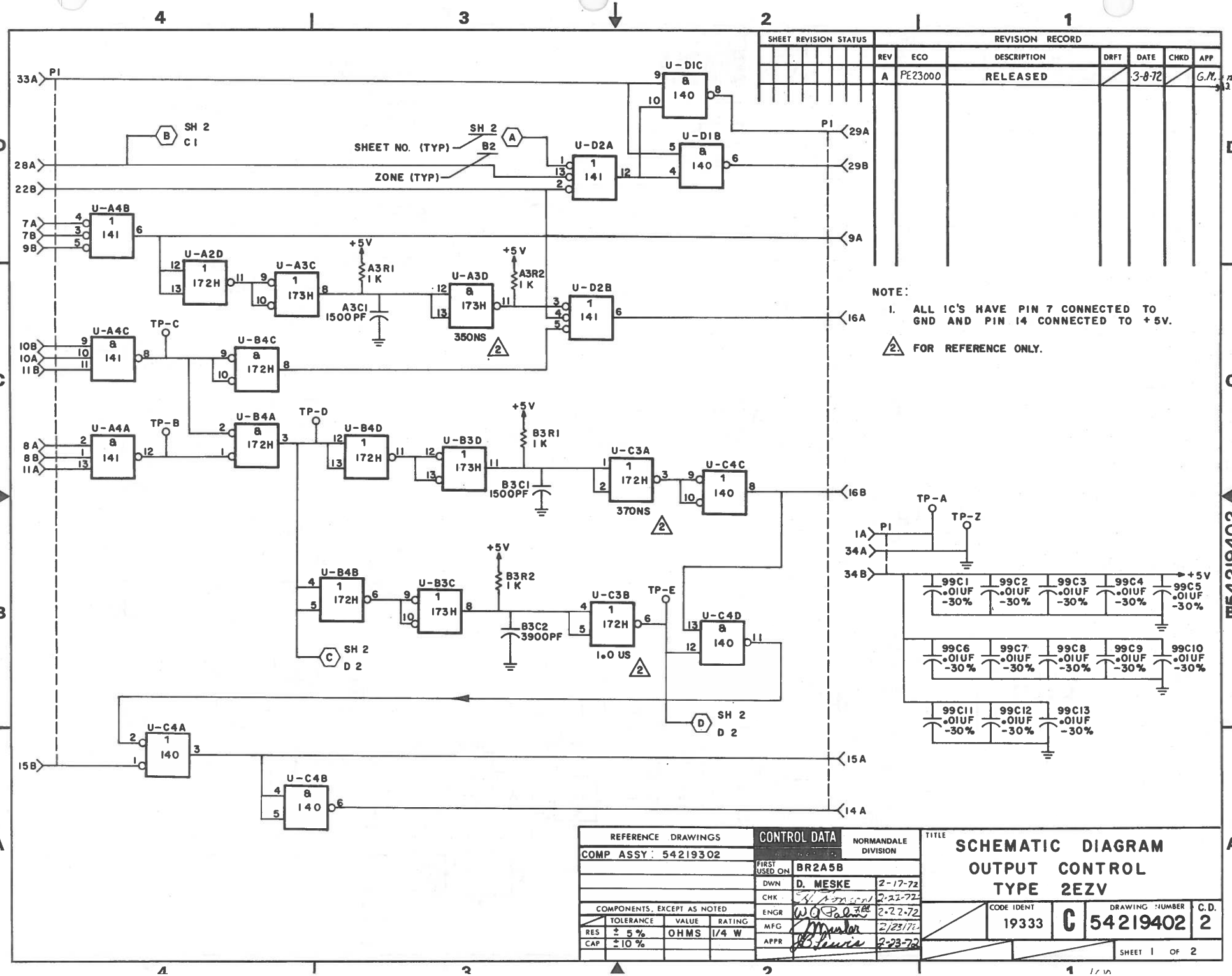
SCHEMATIC DIAGRAM OUTPUT CONTROL 2 TYPE 1EYV

CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54219001	2

SHEET 1 OF 3


SCHEMATIC DIAGRAM
OUTPUT CONTROL 2
TYPE 1EYV
NORMANDALE DIVISION
C 54219001 2
SEE SHEET 1 FOR REV
REVISION RECORD
REV
ECO
DESCRIPTION
DATE
CHKD
APP'D
SHEET NO. (TYP)
ZONE (TYP)
+5V
TP-B
27 MS
10K
1K
3.9K
390PF ± 10 %
100NS


SCHEMATIC DIAGRAM
OUTPUT CONTROL 2
TYPE 1EYV
CONTROL DATA
NORMANDALE DIVISION
CODE IDENT 19333
DWG NO 54219001
SHEET 3
S.D. 2
REVISION RECORD
REV
ECO
DESCRIPTION
SEE SHEET 1 FOR REV
DATE
APP
U-DIA
U-DIB
U-C1B
U-C1D
U-C1C
U-C1A
U-D2B
U-B1B
U-B1A
U-B2D
U-A2D
U-E1A
U-E2A
U-E1B
U-E1C
U-E1D
U-D2C
U-D2D
U-D2A
TP-H
TP-J
TP-G
TP-F
TP-C
TP-E
TP-D
+5V
B1R1 1K
A2R1 1K
A2C2 390PF ±10%
100NS
SH 2 C 3
P1
33A
30A
28A
29B
24B
25B
24A
30B
29A

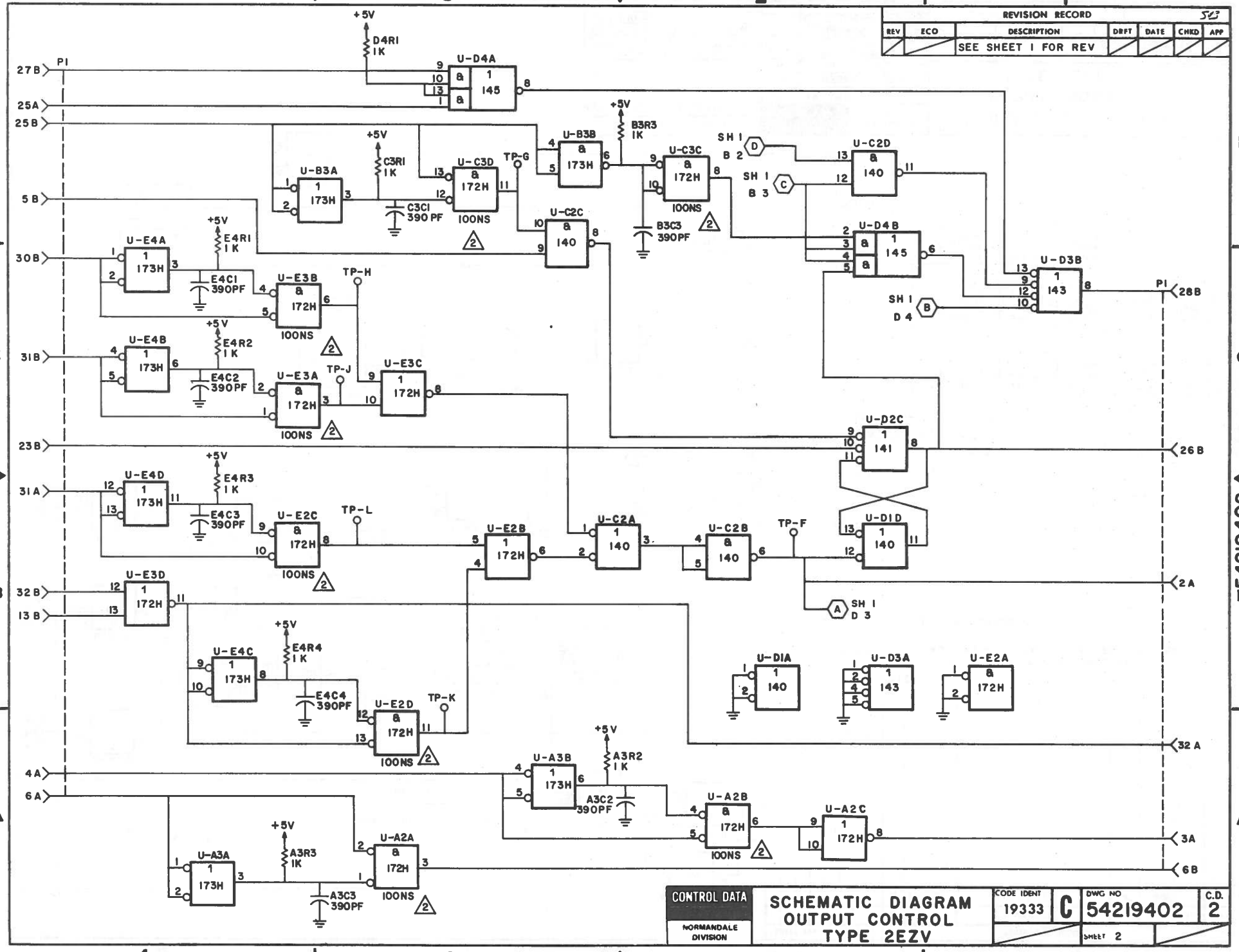


70614700 L

5-101

B 54219402

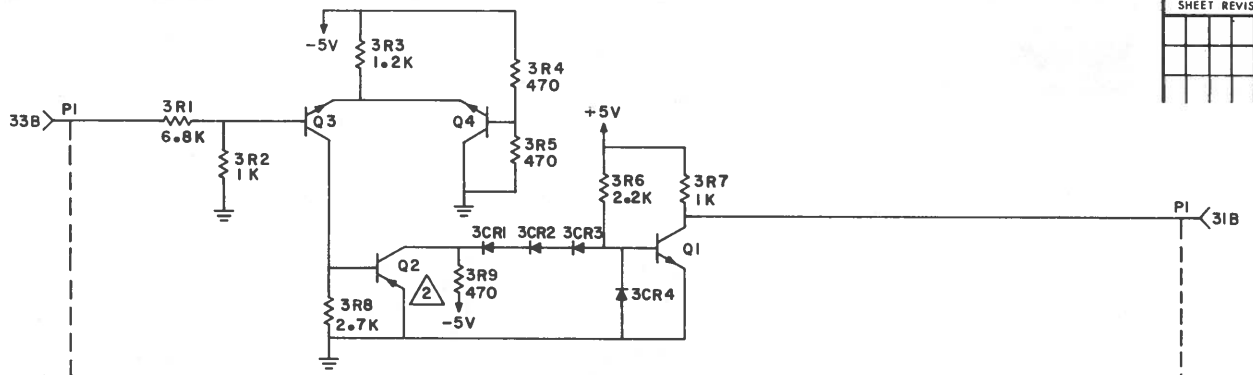
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				

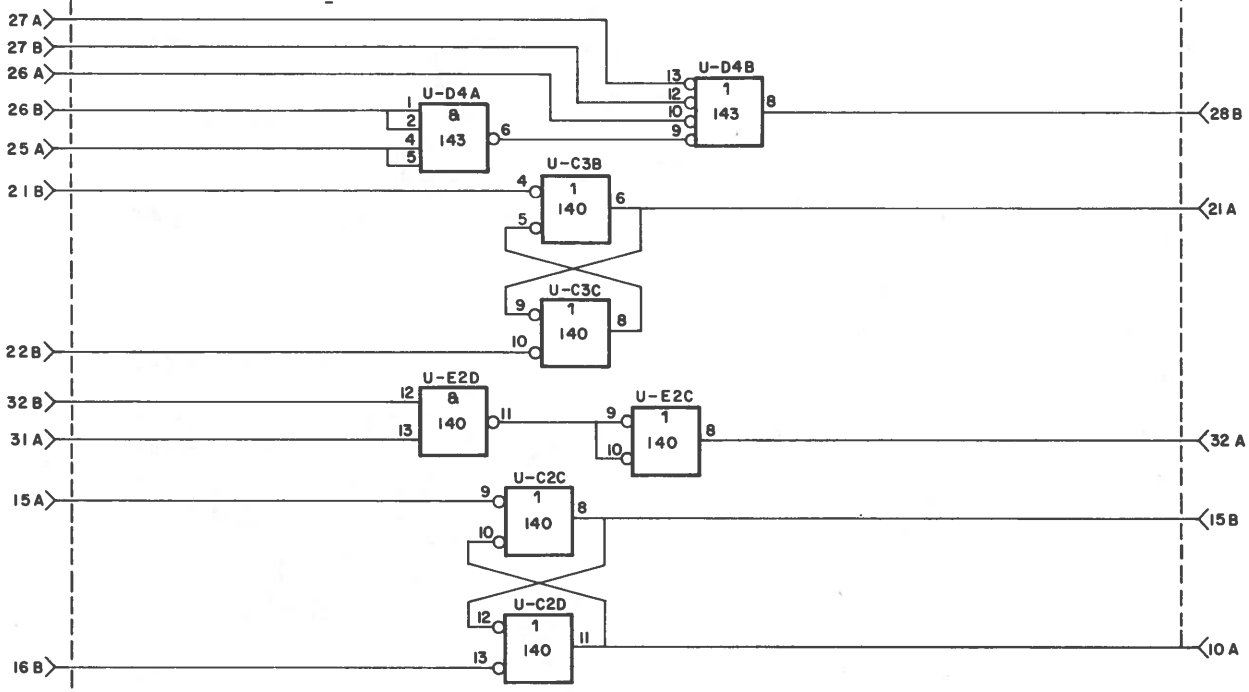


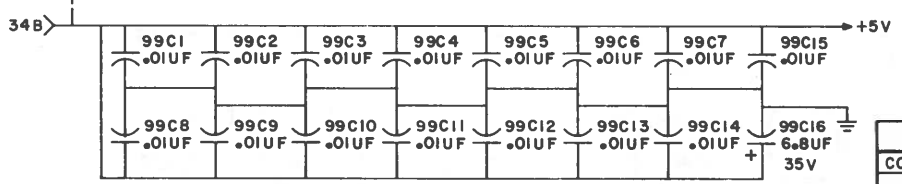
CONTROL DATA	SCHEMATIC DIAGRAM OUTPUT CONTROL TYPE 2EZV	CODE IDENT		DWG NO	C.D.
NORMANDALE DIVISION		19333	C	54219402	2
				SHEET 2	

54219402

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE 23000	RELEASED		4-28-73		

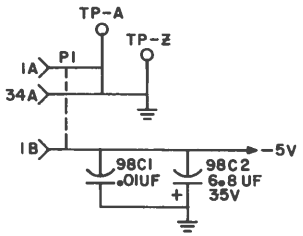






NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL DIODES SILICON, 92115021
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   DELAY TIMES ARE NOMINAL
2. TRANSISTOR, SPNP, 2N4258, 50211510.
3. ALL IC'S HAVE PIN 7 CONNECTED TO GND; PIN 14 TO +5V
4. DELAY TIMES FOR REFERENCE ONLY.



REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION
COMP ASS'Y 54218903	FIRST USED ON	BR2A5
	DWN	3-19-73
	CHK	4-13-73
	ENGR	4-3-73
	MFG	4-16-73
	APPR	4-16-73

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±20%		

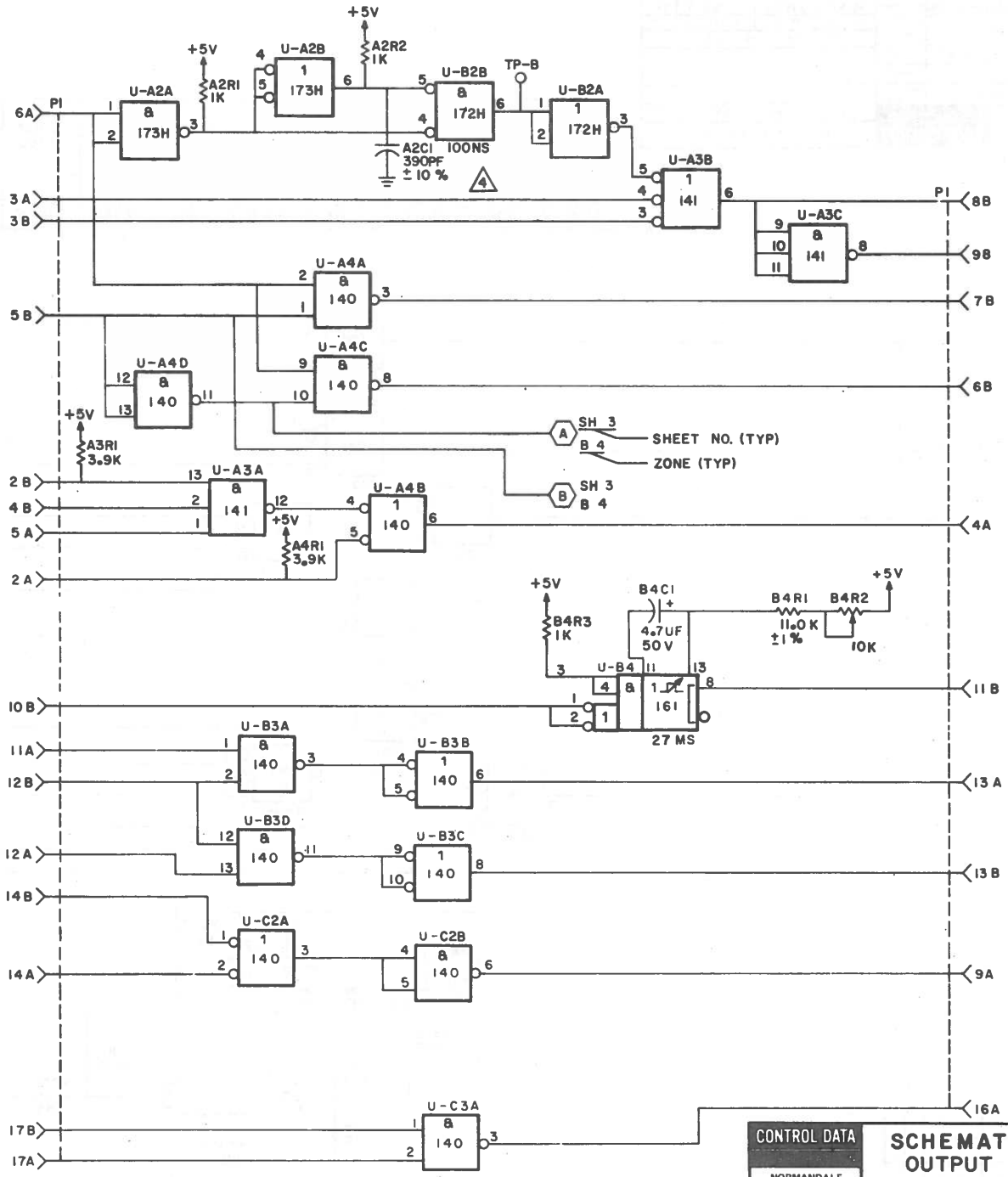
TITLE

SCHEMATIC DIAGRAM OUTPUT CONTROL 2 TYPE 3EYV

CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54219003	8

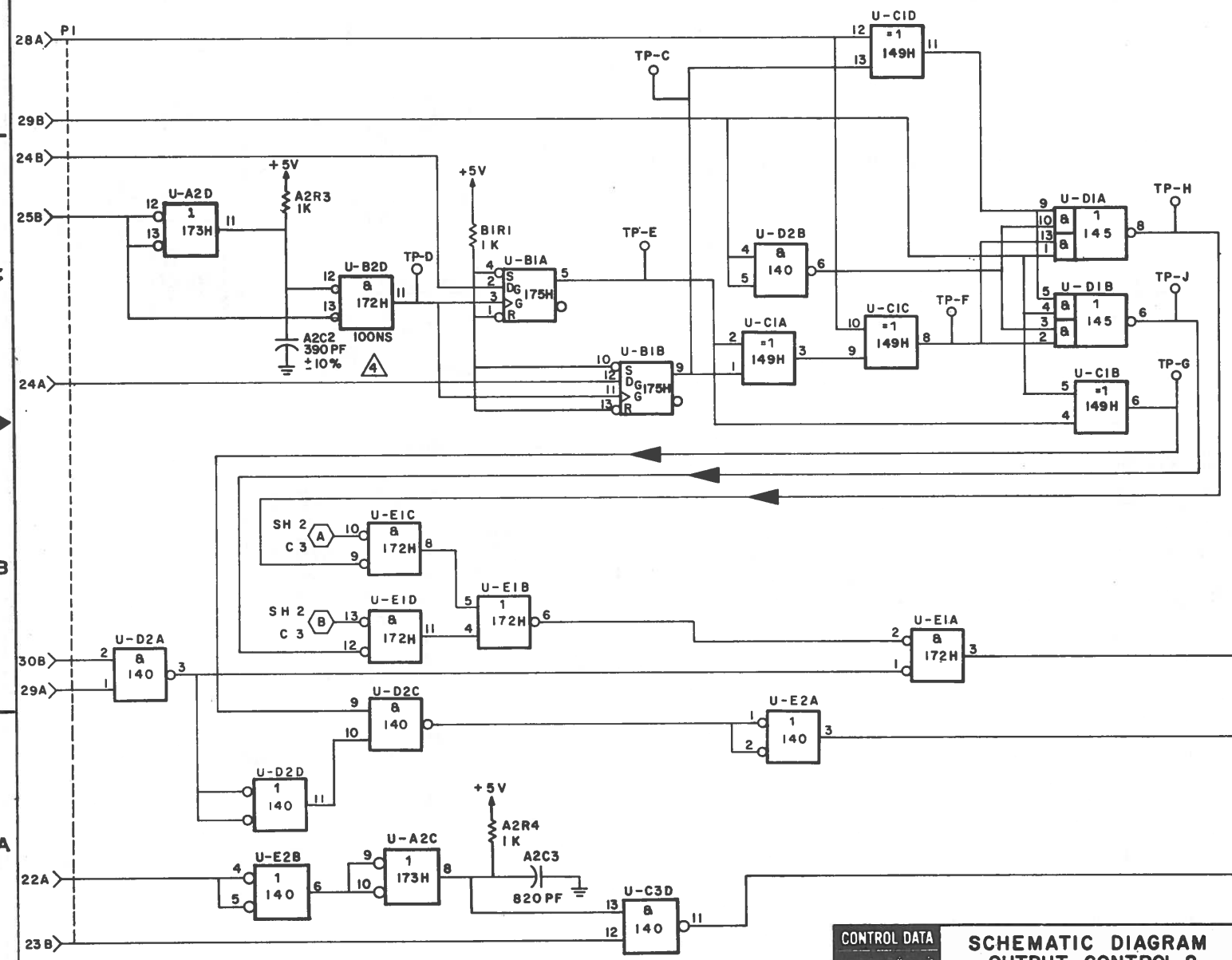
SHEET 1 OF 3

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				



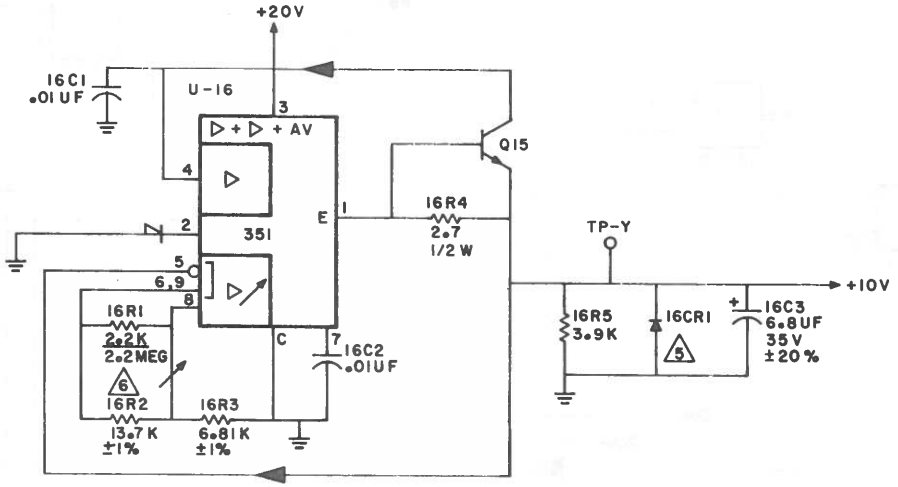
CONTROL DATA	SCHEMATIC DIAGRAM OUTPUT CONTROL 2 TYPE 3EYV	CODE IDENT		DWG NO	C.D.
NORMANDALE DIVISION		19333	C	54219003	8
				SHEET 2	

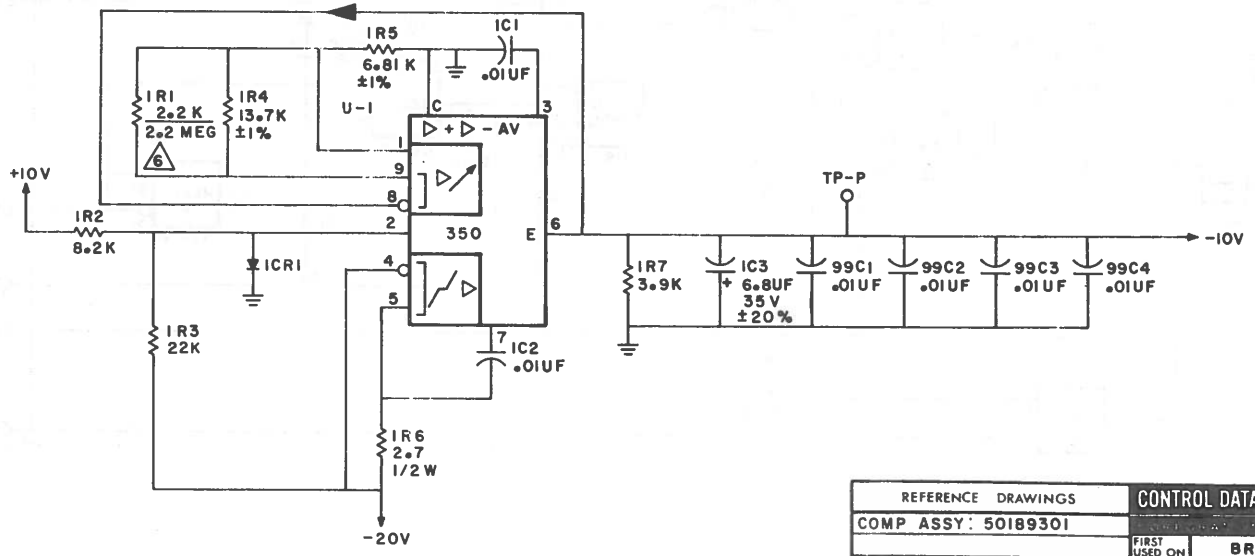
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				



CONTROL DATA	SCHEMATIC DIAGRAM OUTPUT CONTROL 2 TYPE 3EYV	CODE IDENT		DWG NO	C.D.
NORMANDALE DIVISION		19333	C	54219003	8
				SHEET 3	

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED				

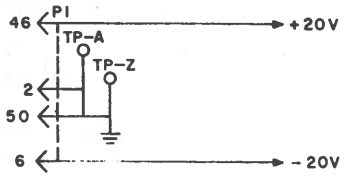




NOTE:

1. UNLESS OTHERWISE SPECIFIED
   ALL TRANSISTORS SNPN, 2N3646, 50210310
   ALL DIODES, SILICON, 92115023
   ALL ZENER DIODE TOLERANCES ±5%

2. TRANSISTOR, SNPN, 2N3569.
3. TRANSISTOR, QUAD SNPN, 50251100.
4. TRANSISTOR, DUAL SNPN, 2N3423, 50212000.
5. DIODE, GERMANIUM, 11801200.
6. RESISTOR VALUE SELECTED PER ENGINEERING TEST PROCEDURE.
7. TRANSISTOR, SPNP, 2N3645, 50211210.



REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION
COMP ASSY: 50189301	FIRST USED ON	BR2A1
	DWN	D Mosher 7-23-71
	CHK	9-7-71
	ENGR	R.E. MacCrone 9-7-71
	MFG	9-13-71
	APPR	9-13-71

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

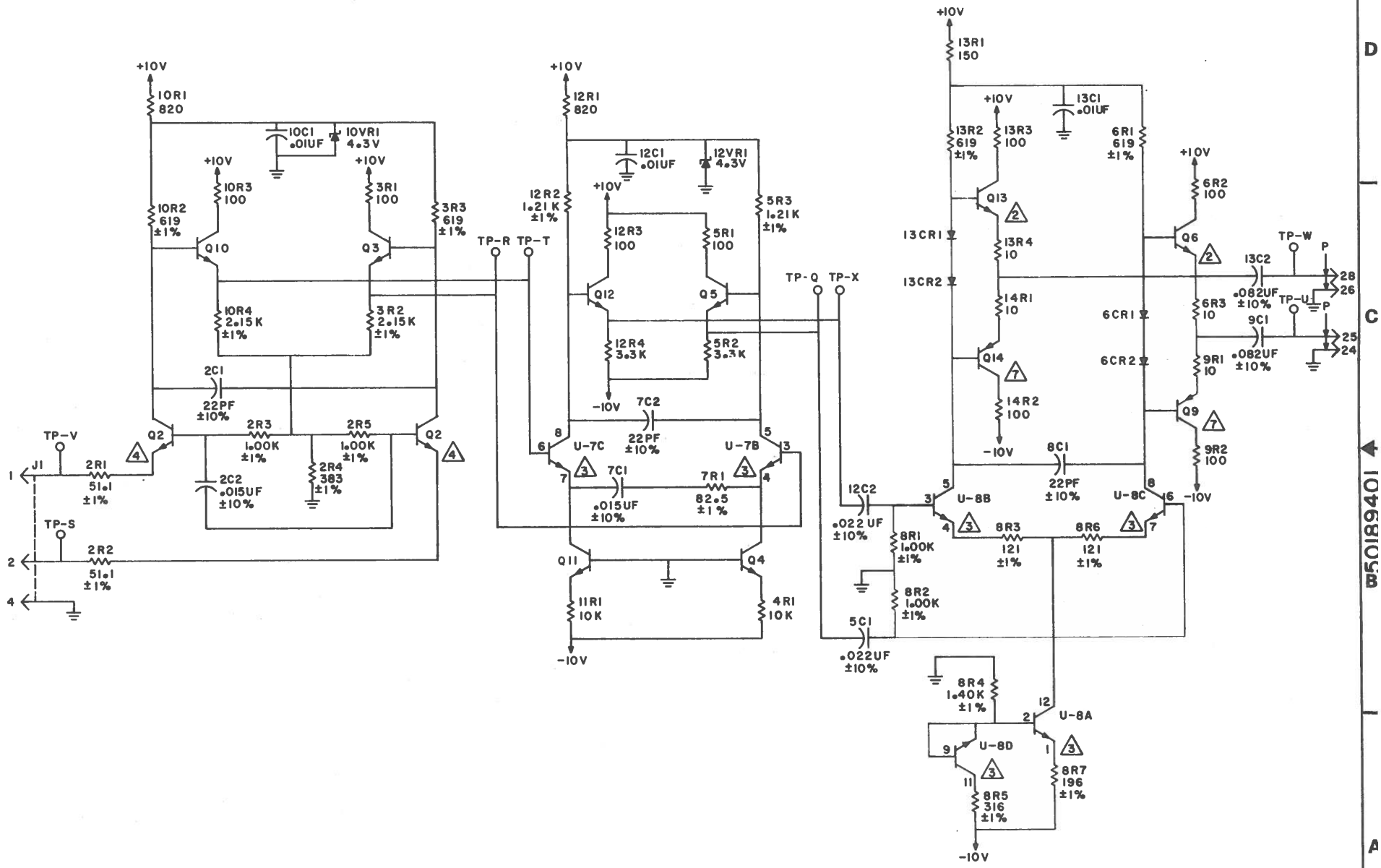
TITLE
SCHEMATIC DIAGRAM
TRACK SERVO PREAMP
TYPE 1FZN

CODE IDENT		DRAWING NUMBER	CD
19333	C	50189401	8

SHEET 1 OF 2

50189401 B

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA	SCHEMATIC DIAGRAM TRACK SERVO PREAMP TYPE 1FZN	CODE IDENT		DWG NO	CD
NORMANDALE DIVISION		19333	C	50189401	8
			SHEET 2		

Information for this section is included in BR2A5 Disk Storage Unit, Pub. No. 70614600.

SECTION 6

MAINTENANCE

SECTION 7

MAINTENANCE AIDS

MAINTENANCE AIDS

GENERAL

Section 7 contains information on logic circuits, the criteria used in determining the further usability of read/write heads and disk packs, and the tester card used in the Maintenance section.

LOGIC

The logic used in this device consists of two styles of circuits: discrete component and integrated circuits. Discrete component circuits contain individually identifiable resistors, capacitors, transistors, etc.

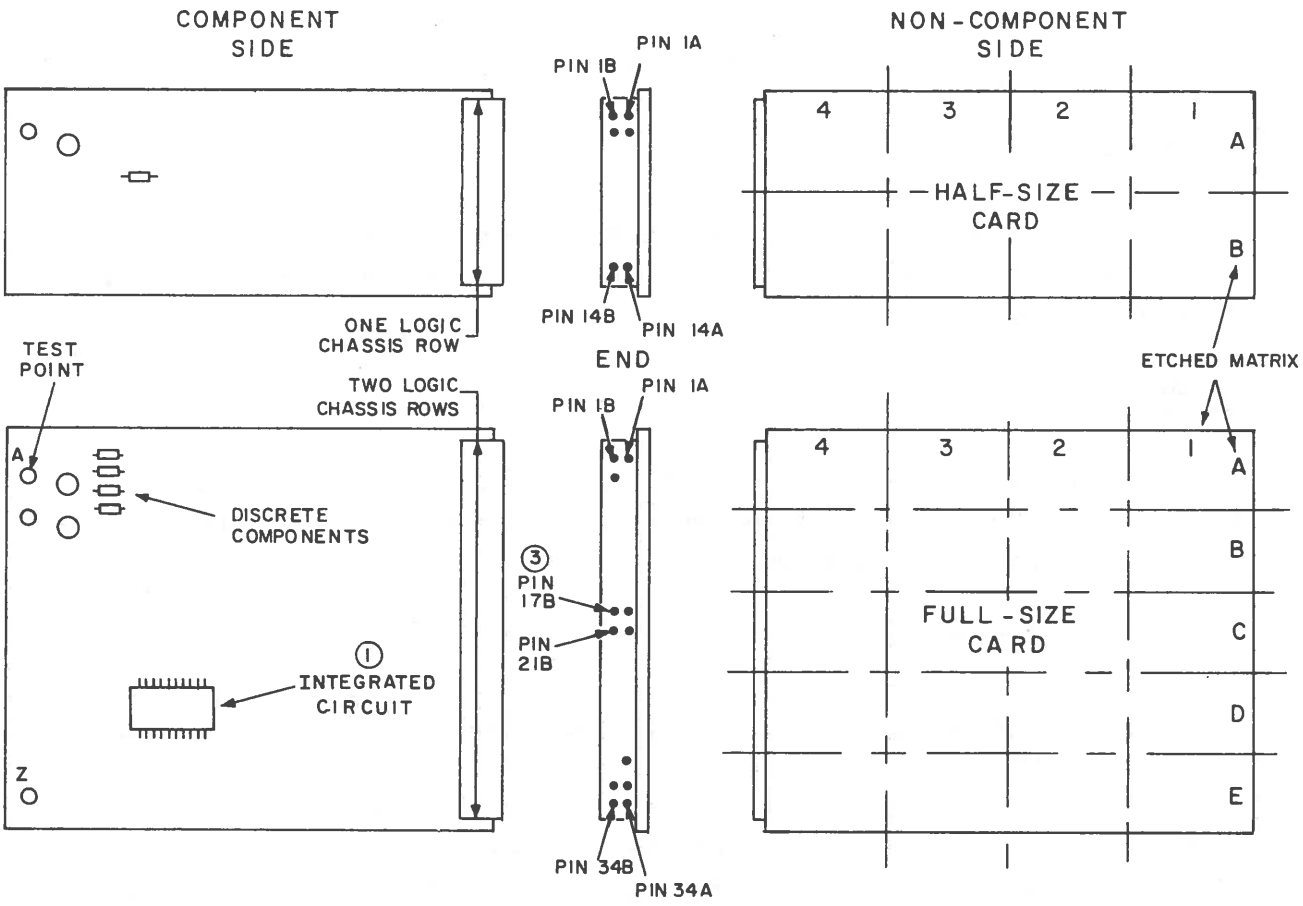
PHYSICAL DESCRIPTION

All components of the logic cards (Figure 7-1) are mounted on one side of a printed circuit board (PCB). Two sizes of PCB are used. The 6.075 x 2.3-inch PCB is the basis for the half-size card (plugs into one logic row). The 6.075 x 4.85-inch PCB is used on the full-size card. The latter card spans two rows of the logic chassis. The female connector of the cards mates with wire wrap pins extending through the chassis wire wrap board. The logic card functions are dispersed from the reverse ends of these pins through wiring installed using the wire wrap technique. Cards installed in the logic chassis are restricted from vertical and horizontal movement by card guide spacers.

Numerical designators (1 through 99) etched on the non-component side of the board identify each transistor. A 4-character alpha-numeric designator is etched on the non-component side of the board to identify the card type. A matrix code (alpha-numeric) also appears on this side. Non-amplifying components such as integrated circuits, resistors, capacitors, diodes, etc., are not marked.

Pin Assignments

Half-size cards are equipped with a 28-pin (sockets) connector, while the full-size card contains a 62-pin connector. Connectors are mounted along the shorter dimension on the component side of the board.



NOTES:

① INTEGRATED CIRCUIT LOCATED AT BOARD MATRIX D2.

2. ON LOGIC DRAWINGS, CARD PINS AND MATRIX LOCATIONS, ARE PRECEDED BY 3 DIGITS THAT IDENTIFY LOCATION OF CARD IN LOGIC CHASSIS (A23, POSITION 23 IN CHASSIS ROW A).

③ PINS 18, 19, 20, (A AND B) NOT PRESENT.

6T6

Figure 7-1. Logic Card Detail

The pins of each card connector are arranged in two columns (A and B) and are numbered from the top starting with pin 1 and continuing through pin 14 on the half-size card. The pins of the full-size card are numbered 1 through 34; however, pins 18A, 18B, 19A, 19B, 20A, and 20B are omitted.

The logic chassis wire wrap surface (side opposite surface where cards are installed) contains wire wrap pin identification information adjacent to each chassis row. Wire wrap pins are numbered 1 through 17 in each chassis row. When a full-size card (spans two logic rows) is installed in the logic chassis, card connector pins (sockets) 1A and 1B mate with wire wrap pins 1A and 1B of the upper row, while card connector pins 21A and 21B mate with wire wrap pins 1A and 1B of the row immediately below. The logic diagrams for this unit show connections in terms of wire wrap pins.

Test Points

Test points are located near the edge of the card opposite the connector and in other strategic places on the component side of the board. Test points are identified alpha-numerically starting with A on the top, outer edge. In most cases, test points A and Z are available for ground reference.

USE OF RELATIVE LEVEL INDICATORS

The relative level indicator is a small circle located at the origin or termination of a signal line, and tangent to a logic symbol. The presence or absence of this indicator tells the conditions that are necessary to satisfy the function of the logic symbol. The presence of the circle indicates a 0 logic level on that line is needed to satisfy the function. The absence of the circle represents a logical 1 as needed to satisfy the function.

The relative level indicator depicts the occurence of inversion. Figure 7-2 shows some representative examples of the relative level indicator being used in this manner.

INFORMATION CONTAINED WITHIN LOGIC SYMBOLS

Discrete Component Circuits

Figure 7-3 shows a schematic (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same theoretical discrete component circuit. Four lines of information are contained within the logic symbol. The top line is the function symbol and designates the broad logic function of that particular symbol. In this case, $\triangleright$ represents an amplifier, the logic function performed by the circuit. The third line, also an alphabetic code, designates the circuit type being used (HAB). The circuit type is a subdivision of the function identifier (specifically a high level amplifier). By using the circuit type designator,

detailed information on that particular circuit can be derived in the following paragraphs (see Discrete Component Circuit Descriptions).

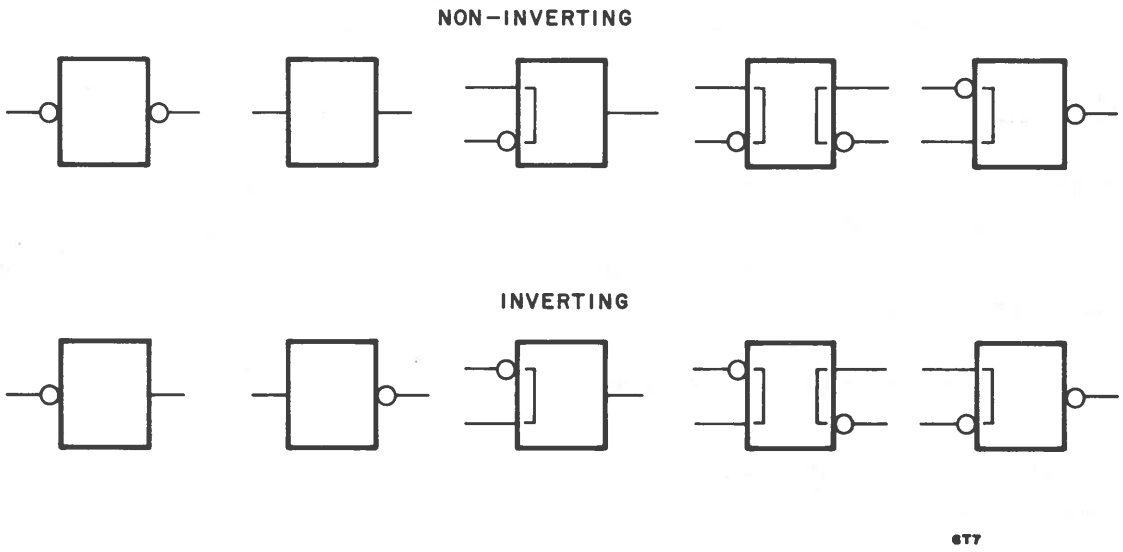


Figure 7-2. Inversion Conventions

The second line within the symbol is used to differentiate that particular symbol from similar symbols that appear on the logic diagram. It is called the logic term and consists of a one-letter prefix and an assigned identification number (in this case, A705).

The numbers on the input lines to the symbol indicate which transistor is driven by that input line. For example, the upper input has a number 22 on its line, showing that it drives transistor number 22 (ie., Q22 on the card schematic diagram).

The output lines also have numbers associated with them. These numbers indicate which transistor directly feeds the output line. For example, the lower output line has a number 40 above it, indicating that the output from transistor number 40 (Q40 on the card schematic diagram) drives the lower output line.

The lines on the interior of the logic block that bracket both inputs and both outputs show that the input lines and the output lines are differentials. The relative level indicators show that the amplifier does not invert the signal. Slashes on the inputs and outputs show that the signal levels are non-standard.

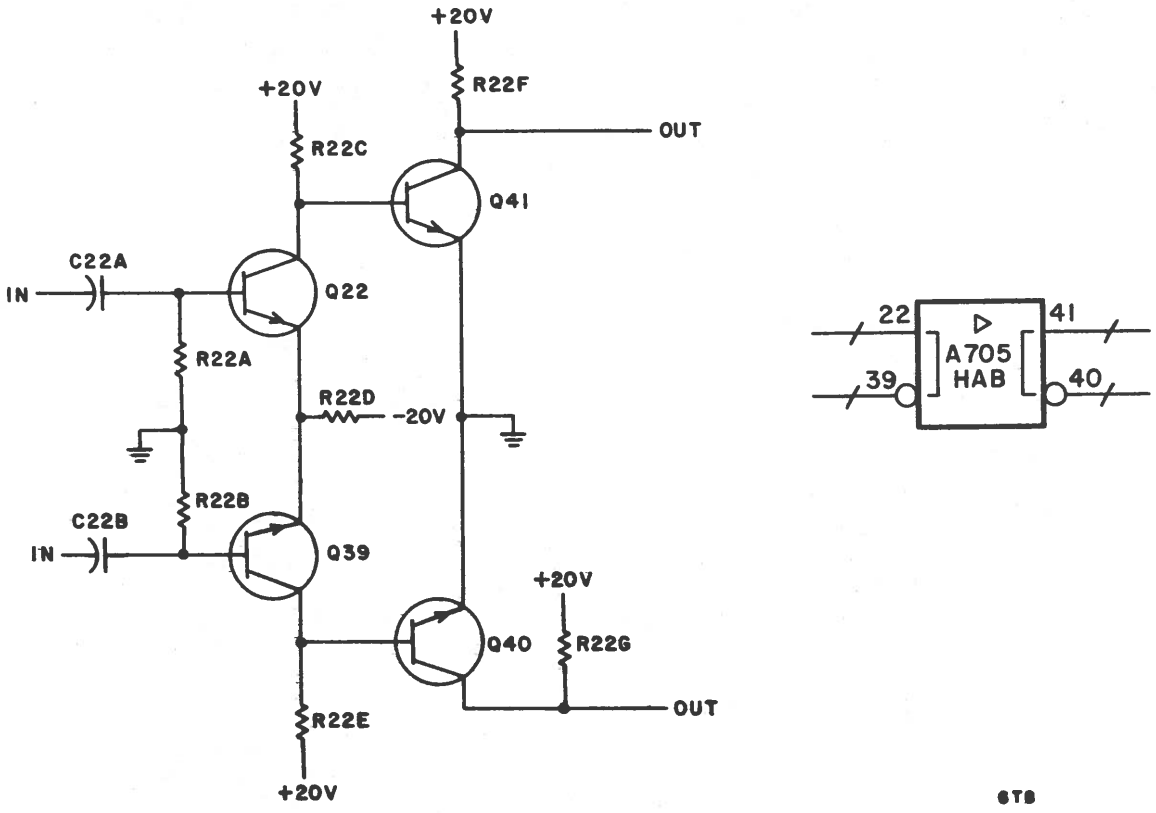


Figure 7-3. Discrete Component Circuit

Integrated Circuits

Figure 7-4 shows the schematic version (as shown on card schematic diagrams) and the logical representation (as shown on logic diagrams) for the same representative integrated circuit.

Referring to Figure 7-4, it is apparent that the two versions are essentially the same. Both views identify pin numbers, the function symbol, and the CDC element number for the circuit. Refer to Table 7-1 for manufacturer's information on the various element numbers. One line of information appears on the logic version that does not appear

on the schematic block. This is the logic term which provides specific identification for the circuit.

The last item of information regarding these two representations involves the location code which borrows part of the schematic symbol's reference designator. In the reference designator (U-A4B), the U specifies a non-amplifying integrated circuit, the A4 is the circuits board matrix location for the package, and the B indicates the section of the package. (A 140 package is a four-section package. Each section is a separate circuit. Sections are identified A through D.) The location code (on logic drawings) borrows the matrix location and additionally specifies the location of the card in the logic chassis: position 5 of row B.

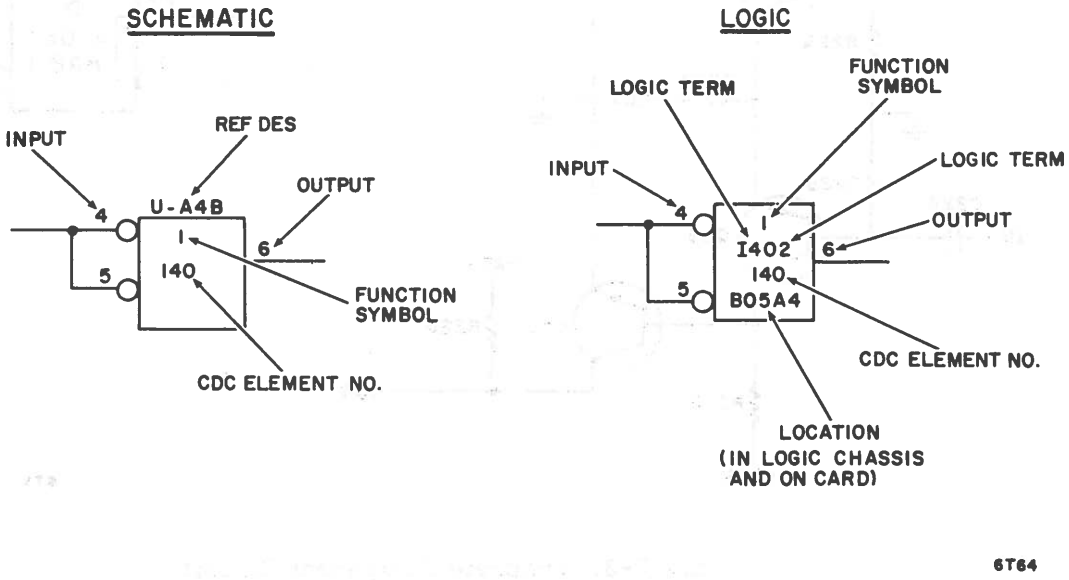


Figure 7-4. Integrated Circuit

TABLE 7-1. CDC ELEMENT NUMBER CROSS REFERENCE

CDC Element No.	Manufacturer, Type	Description
140	Fairchild, 9002	Quad, 2-input NAND
141	Fairchild, 9003	Triple, 3-input NAND
143	Fairchild, 9009	Dual, 4-input buffer
145	Fairchild, 9005	Dual, AND/OR inverter
146	Fairchild, 9016	Hex, inverter
147	Fairchild, 9007	8-input NAND
149H	Motorola, 3021	2-input exclusive OR
161	Fairchild, 9601	Retriggerable multivibrator
162	Texas Instrument, 75107	Dual differential receiver
163	Signetics, 8281	4-bit presettable counter
172H	Motorola, 3002	Quad, 2-input NOR
173H	Motorola, 3004	Quad, 2-input NAND
175	Motorola, 3060	Dual type-D flip-flop
182	Signetics, 8291 or Texas Instrument, 74197	4-bit presettable counter
191	Fairchild, 9301	1 of 10 Decoder
200	Texas Instrument, 7406	Hex, inverter
300	Fairchild, 709	Operational amplifier
301	Fairchild, 741	Operational amplifier
304	Fairchild, 715	Operational amplifier

WIRED FUNCTIONS

The logical representation for wired functions is shown in Figure 7-5. These functions are used where circuits have the capability of being combined as an AND or an OR function by having the outputs connected. This is simply a physical connection and no electrical or electronic components are involved. The logical interpretation of a wired OR function requires simply that one of the inputs be a "0" before the output can be a "0". The wired AND output will be a "1" only when both inputs are "1's".

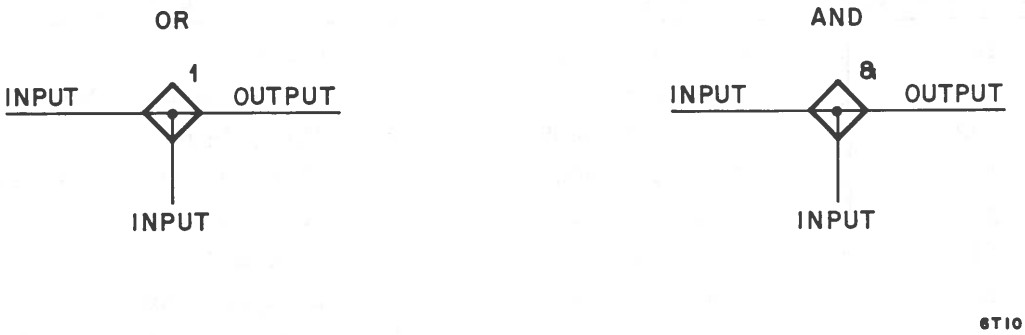


Figure 7-5. Wired Functions

STANDARD/NON-STANDARD LOGIC LEVEL INDICATOR

The input to a logic function at voltage other than the standard logic level is represented by a slash across the non-standard level line. Absence of the slash (or absence of an X, see below) indicates a standard logic level on that line.

When the input signal to a logic function is an analog signal, the input line will have an X across it. The analog designator is used on lines that normally operate at more than two voltage levels.

INTEGRATED CIRCUIT DESCRIPTIONS

Basic functional information for integrated circuits is provided on the Key to Logic Symbols sheet of the logic diagrams.

Detailed functional descriptions and schematic diagrams for integrated circuits is available in the circuit manufacturer's handbook, Table 7-1.

DISCRETE COMPONENT CIRCUIT DESCRIPTIONS

Figures 7-6 through 7-56 are the schematic diagrams for the discrete component circuits used in this device. A verbal description supports each circuit diagram. The order of presentation is in accordance with the 3-letter alphabetical circuit type designator.

Gated Amplifier - FAB

The FAB circuit (Figure 7-6) is a low level amplifier that amplifies the analog read signal from the head. Input B is a gate input.

When input B is +20v, diodes CRNA, CRNB, CRNC, CRND, CRNE, and CRNF are forward biased. The voltage between CRNC and CRNE and between CRND and CRNF is clamped at approximately +2.0v. With all diodes forward biases, the read signal can pass to the amplifier.

When input B is ground, diodes DRNG and DRNH clamp the voltage at +0.6v. This reverse biases the input diodes. No read signal can enter.

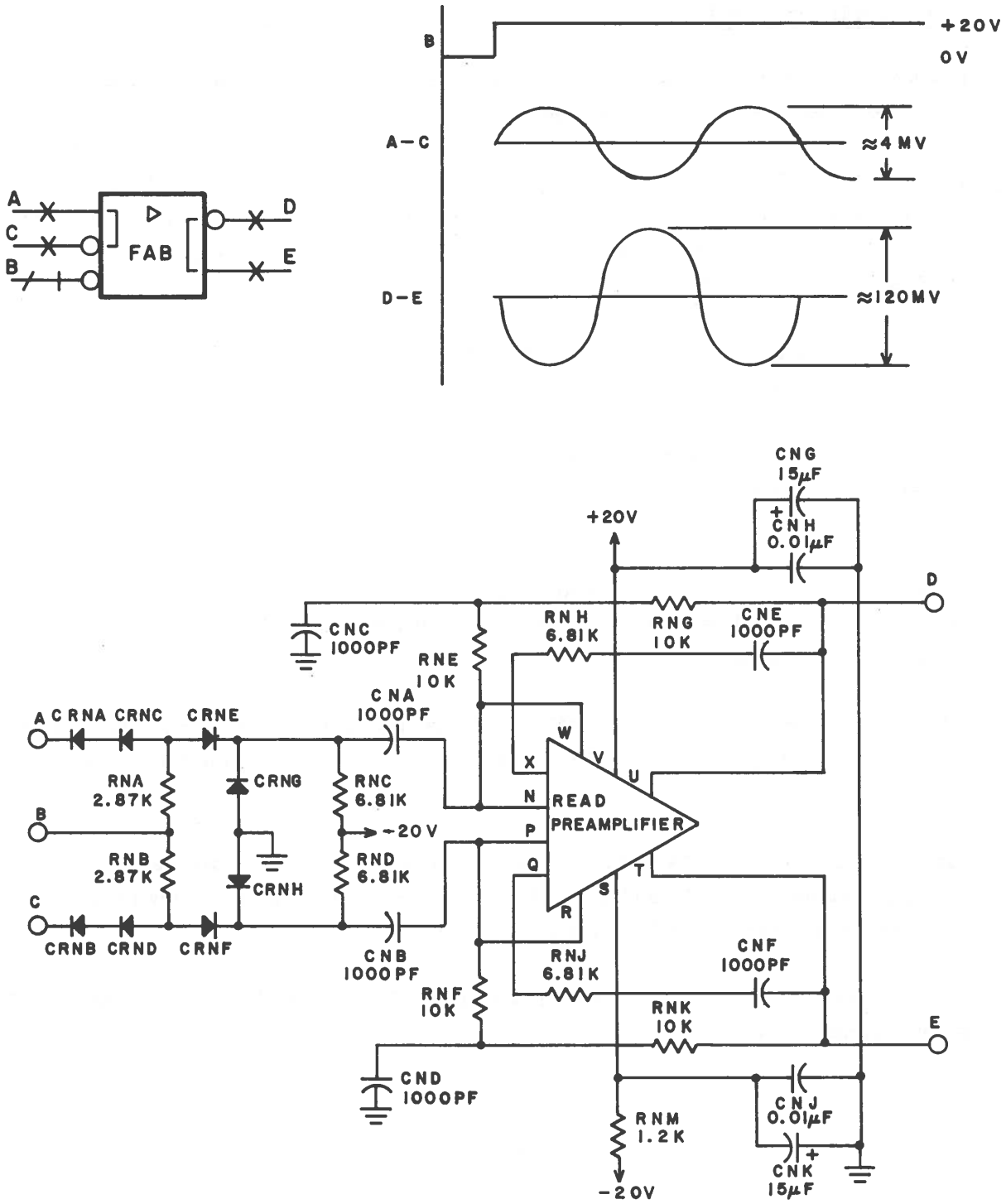
The preamplifier is a three-stage amplifier using an emitter follower output stage for low output impedance. The integrated preamplifier has discrete component ac and dc feedback.

AC feedback is provided by CNE and RNH in the top half and CNF and RNJ in the lower half of the circuit. The signal is brought back to the emitters of the input stage to increase input impedance.

DC feedback is provided by RNG, RNE, and CNC (to ground) in the upper half and RNK, RNF, and CND (to ground) in the lower half of the circuit. This feedback helps to stabilize the output.

Capacitors CNG, CNH, CNJ, and CNK filter noise from the +20v and -20v power supplies, respectively. The electrolytic capacitors filter low frequency noise. The paper capacitors filter high frequency noise.

Open loop gain in the amplifier is approximately 180. Closed loop gain in the amplifier is approximately 30.



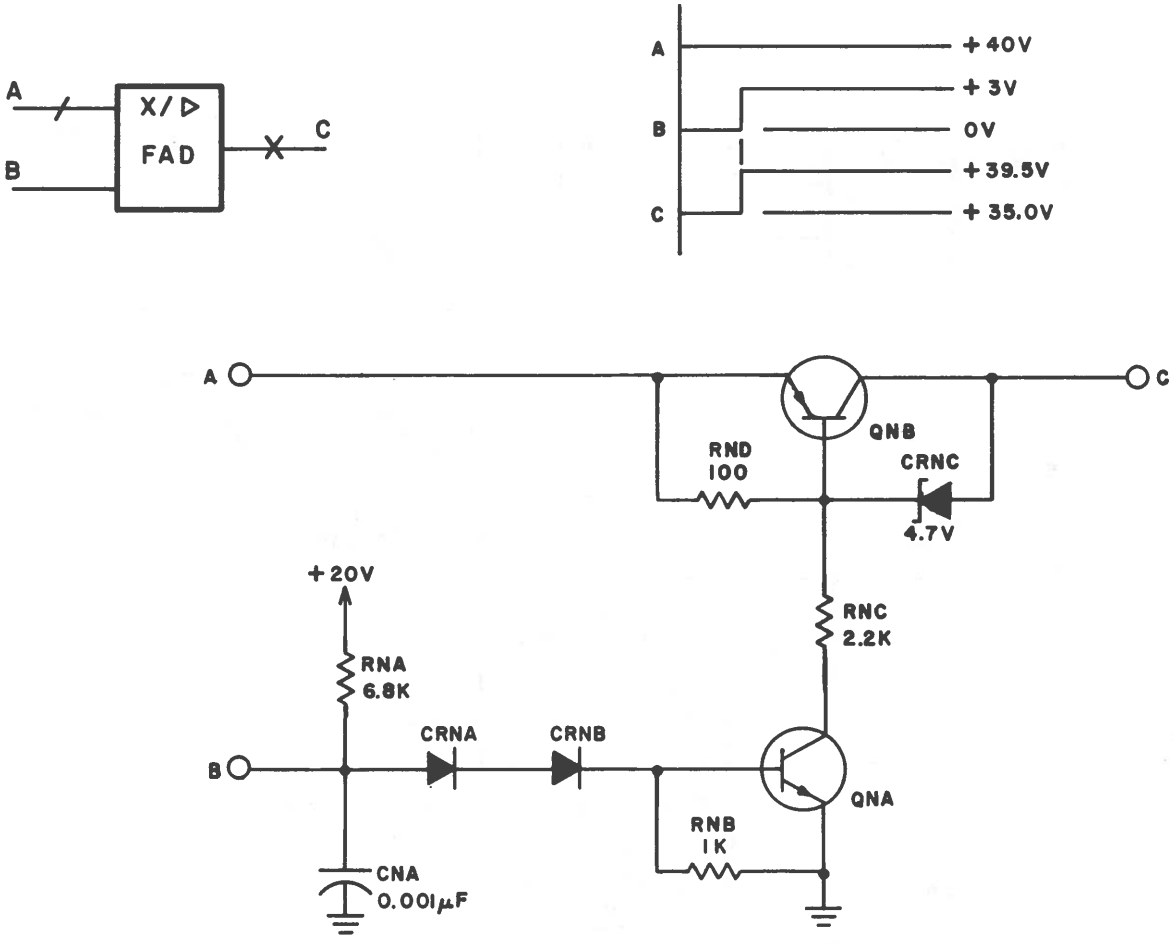
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T100

Figure 7-6. Gated Amplifier - FAB

Current Amplifier - FAD

The FAD circuit (Figure 7-7) provides a voltage drop from A to C of either 0.5v or 5.0v which is selected with a "1" or a "0", respectively, at B. A "1" at B turns transistor QNA on. This provides base drive through RNC to QNB which turns on. The output at C is now the same as the input at A except for the emitter-collector drop (0.5v) across QNB. With input B at ground, "0", QNA is off and base drive to QNB is provided through the 4.7-volt Zener diode, CRNC. The voltage drop from A to C is V_{be} plus V_z. Resistor RND improves circuit operation by increasing the Zener current.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T101

Figure 7-7. Current Amplifier - FAD

Gated Intermediate Level Amplifier - GJA

The GJA circuit (Figure 7-8) is an analog gate that is controlled by input B. When input B is +20v, both transistors are on. All analog signals pass through the circuit. Capacitors CNA and CNB ensure that only analog signals are passed. CNC filters noise spikes from the gating signal. Dc power for the transistors is supplied by the circuit in the next stage.

When input B is +0.2v, both transistors are off. No signals pass through the circuit.

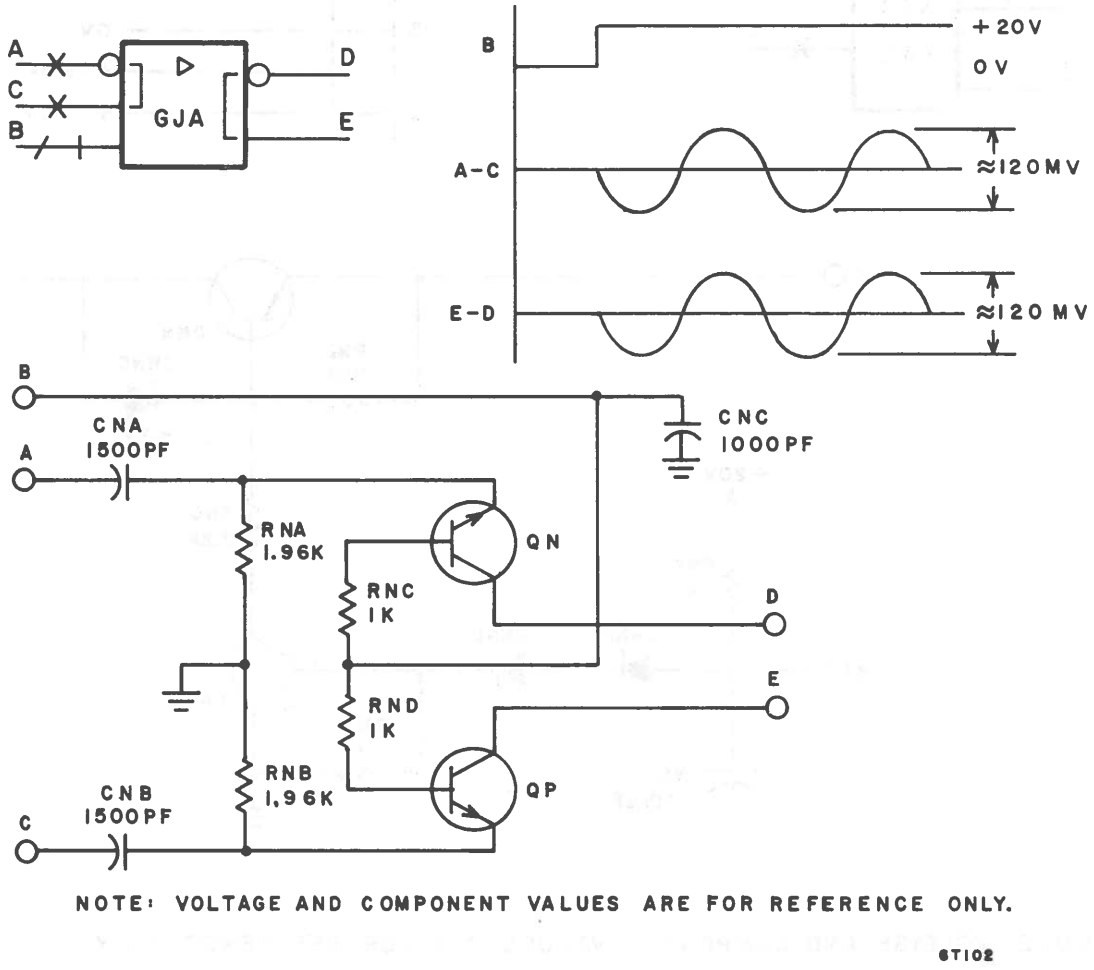


Figure 7-8. Gated Intermediate Level Amplifier - GJA

Gated Analog Clamp - GJB

The GJB circuit (Figure 7-9) functions to turn QR (an N channel junction field effect transistor) on when a logical 0 is applied at input B and to turn QR off when a logical 1 is applied at input B.

In actual application output C is connected to the summing point of an operational amplifier and therefore is always at ground potential. Terminal A is connected to the output of the operational amplifier. When QR turns on, it presents a very low resistance feedback path to the operational amplifier, thus forcing the gain of the amplifier toward zero. As a result the operational amplifier is essentially clamped to an output voltage of zero.

The on-off resistances of QR are 40 ohms and 50 megohms, respectively.

Multiple Gate Analog Clamp - GJC

The GJC circuit (Figure 7-10) functions to turn QQ (an N channel junction field effect transistor) on when a logical 0 is applied at any of the B inputs and to turn QQ off when all of the B inputs are at a logical 1.

In actual application output C is connected to the summing point of an operational amplifier and therefore is always at ground potential. Terminal A is connected to the output of the operation amplifier. When QQ turns on, it presents a very low resistance feedback path to the operational amplifier, thus forcing the gain of the amplifier toward zero. As a result, the operational amplifier is essentially clamped to an output voltage of zero.

The on-off resistance of QQ are 40 ohms and 50 megohms, respectively.

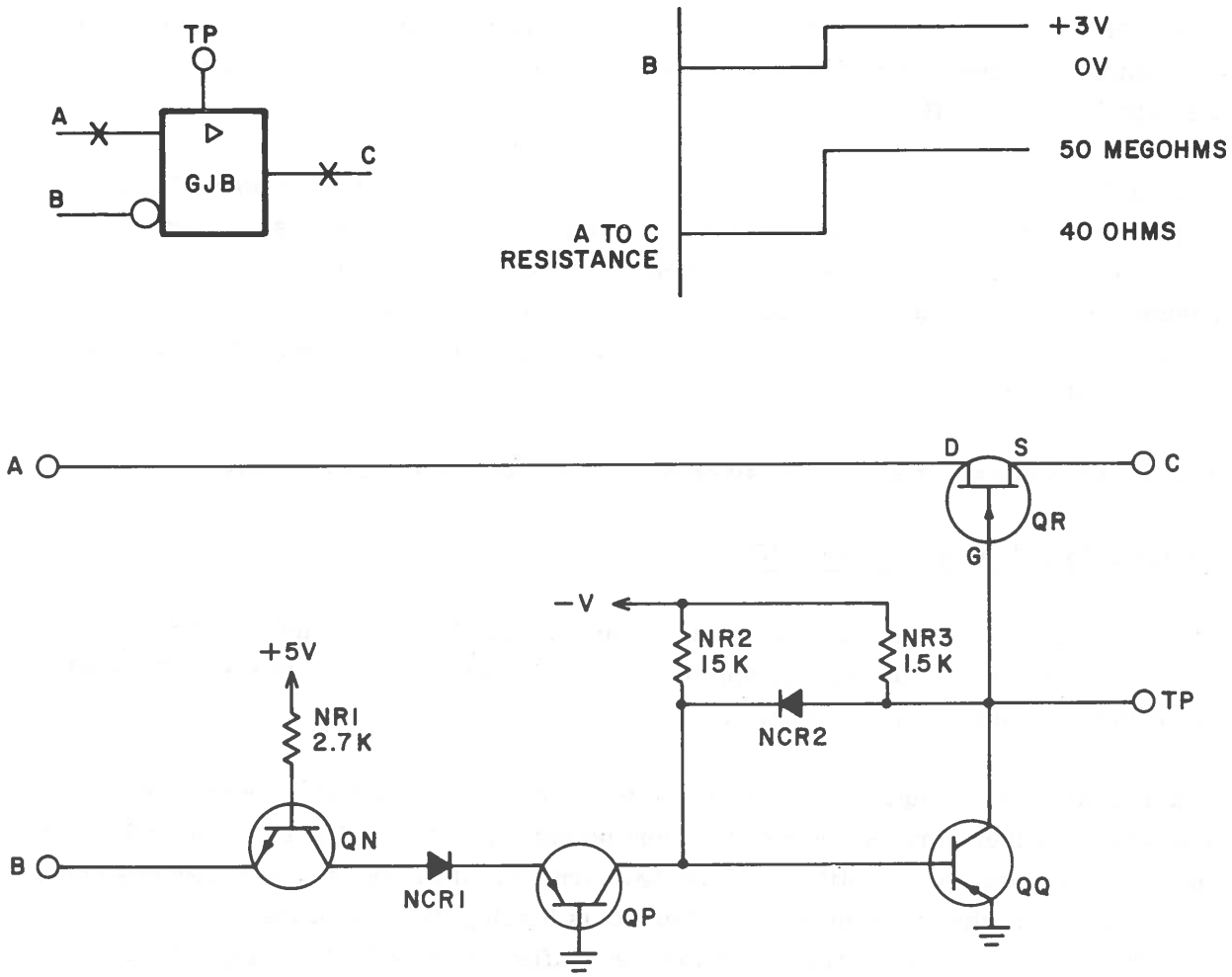
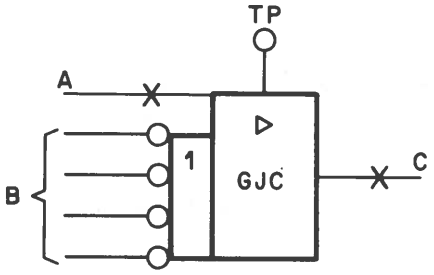
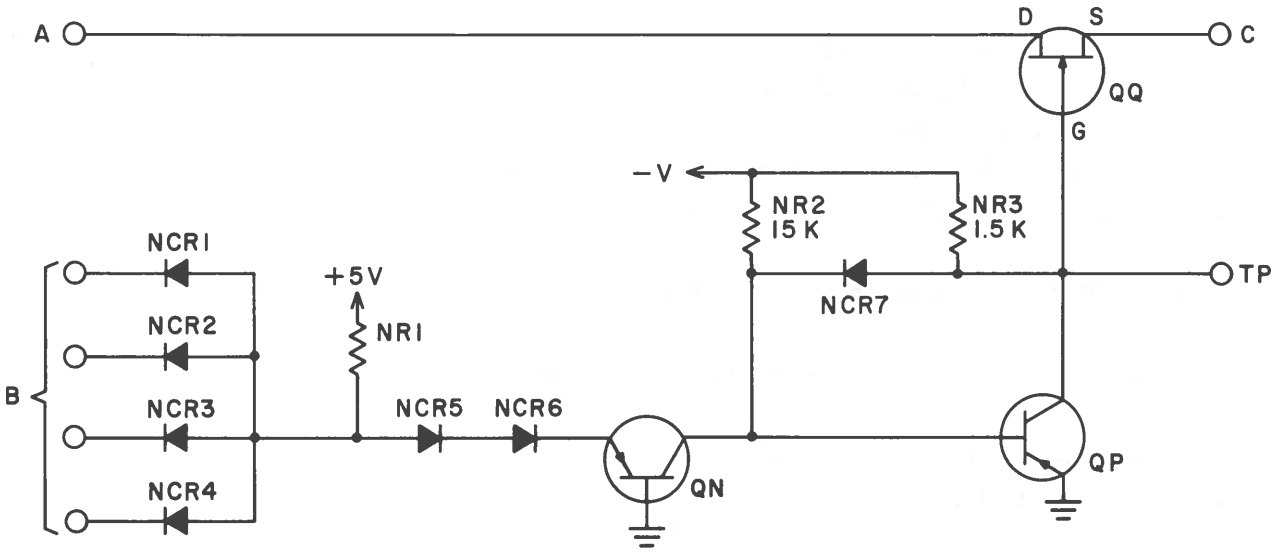


Figure 7-9. Gated Analog Clamp - GJB



IF ANY INPUT B EQUALS 0 VOLTS,
THE A TO C RESISTANCE EQUALS 40 OHMS.

IF ALL INPUT B'S EQUAL +3 VOLTS,
THE A TO C RESISTANCE EQUALS 50 MEGOHMS.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T133

Figure 7-10. Multiple Gate Analog Clamp - GJC

Level Translator - GKA and Digital to Analog Converter - GKB

The GKA and GKB circuits (Figure 7-11) when used together comprise a 5-bit D/A converter. The GKB circuit used singly is a 4-bit converter.

The GKB consists of four voltage switches and a 4-bit R-2R D/A ladder network. Each voltage switch circuit applies positive voltage to the related ladder input when its input is a logical 1. A voltage switch applies ground to the related ladder network input when its input is a logical 0.

In the GKB circuit, the digital inputs G, F, E, and D are ordered from least to most significant. When all digital inputs are "1's", the voltage at H is +6.7v (assuming a 10k ohm load is provided by the following circuit). When all digital inputs are "0's", the analog output is 0v (except for a +6 mv, max., dc offset). The analog output for an increase of one in the digital input code is +446 mv, nominal.

Transistors QN and QP operate as a saturated switch and an emitter follows, respectively, in the voltage switch circuit. Transistors QQ and QR operate as low offset saturated switches, only one of which is on at a time.

The R-2R D/A ladder has a resistance of 10k ohms from any node to ground and divides by two the voltage at the next lower, in significance, node.

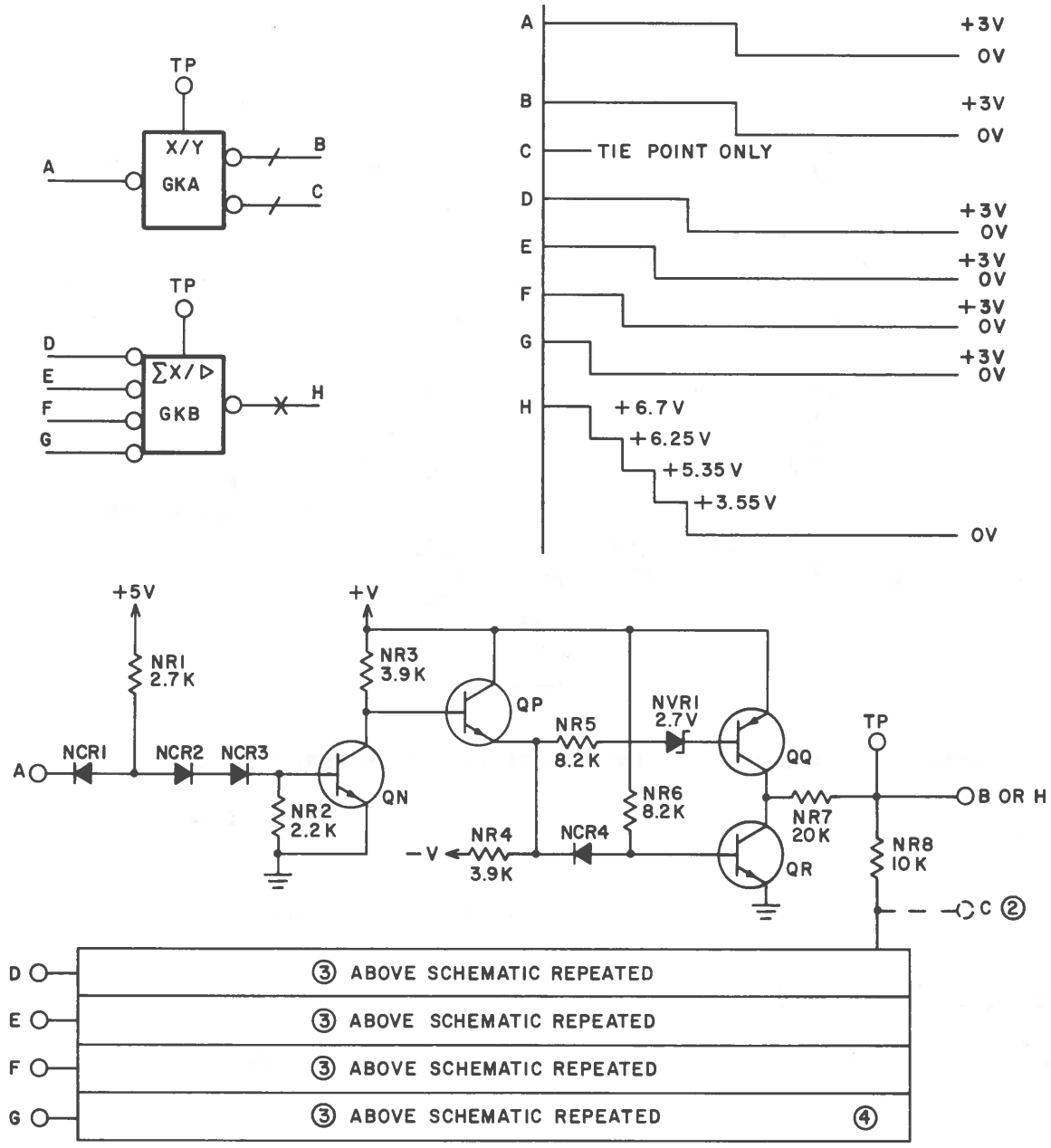
The GKA circuit is identical to one stage of the GKB.

Level Translator - GKC

The GKC circuit (Figure 7-12) converts a logical 0 to a +2.15 (nominal) level used to inject a current signal into the summing point of an operational amplifier.

Typically a resistor is connected between point B and the operational amplifier summing point to establish the magnitude of this current.

When a logical 1 is present at input A, transistor QN saturates, the output diode NCR4 shuts off, and output B drops to 0v, removing the current to the operational amplifier summing point.



NOTES: 1. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY.

② APPLICABLE TO GKA ONLY.

③ APPLICABLE TO GKB ONLY.

④ NR8 IN THIS SECTION IS 20K WITH LOWER END TO GROUND.

6T138

Figure 7-11. Level Translator and D/A Converter - GKA, GKB

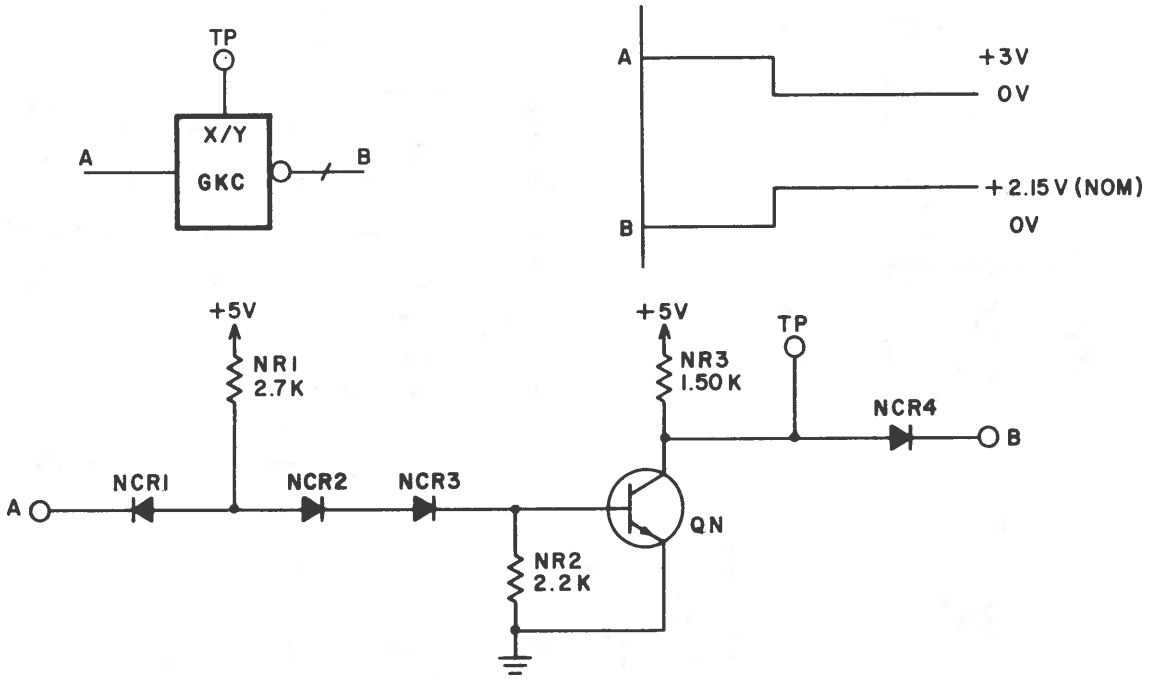


Figure 7-12. Level Translator - GKC

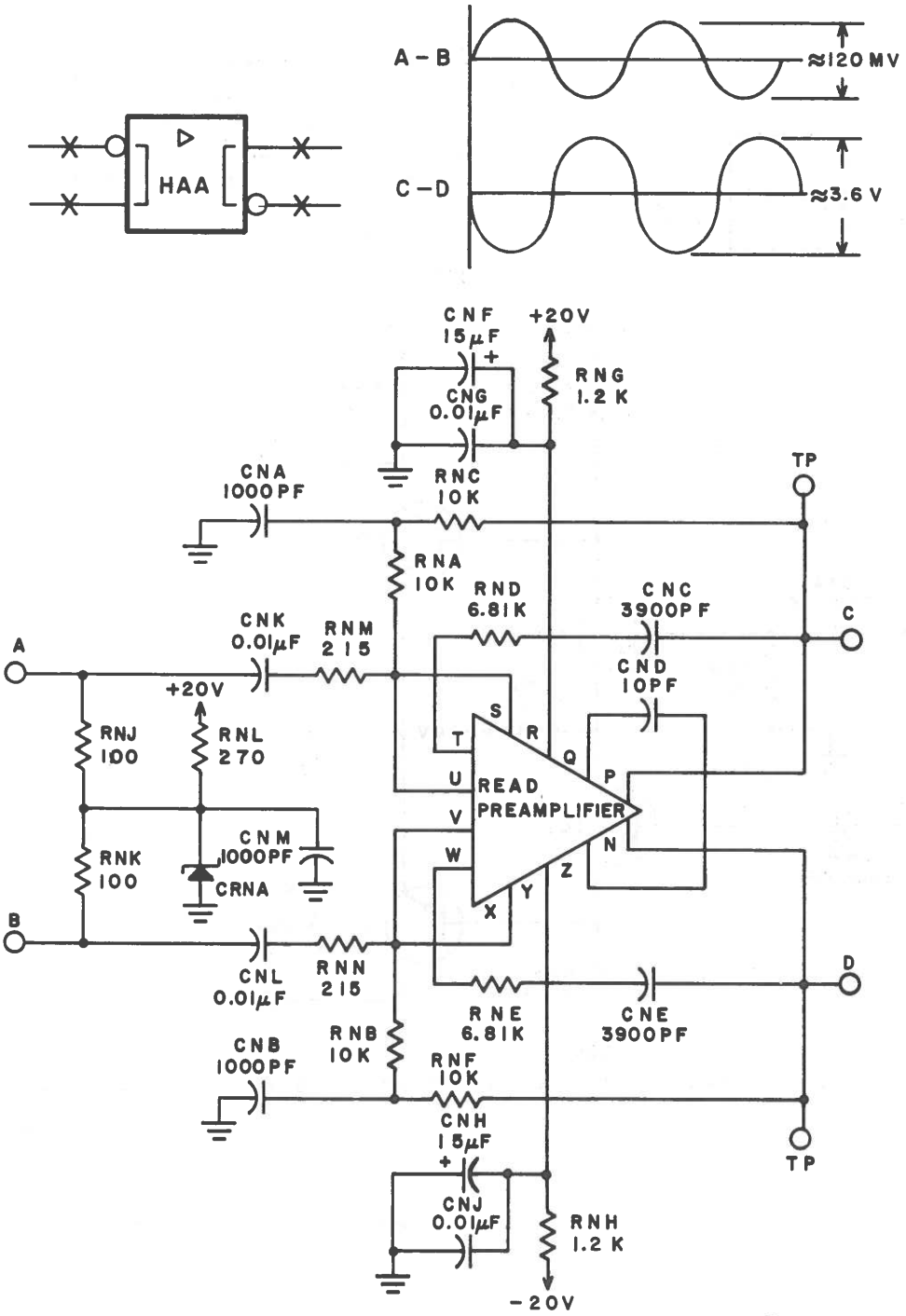
High Level Amplifier - HAA

The HAA circuit (Figure 7-13) is gated by an analog gate circuit (GJA) and provides the load and biasing for that circuit.

The preamplifier, ac feedback, and dc feedback are identical to the FAB circuit. Capacitor DND is added to the output of the second stage to decouple high frequency noise.

High Level Amplifier - HAB

Input to the HAB circuit (Figure 7-14) is a balanced square wave. Output is also a balanced square wave that follows the input.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

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Figure 7-13. High Level Amplifier - HAA

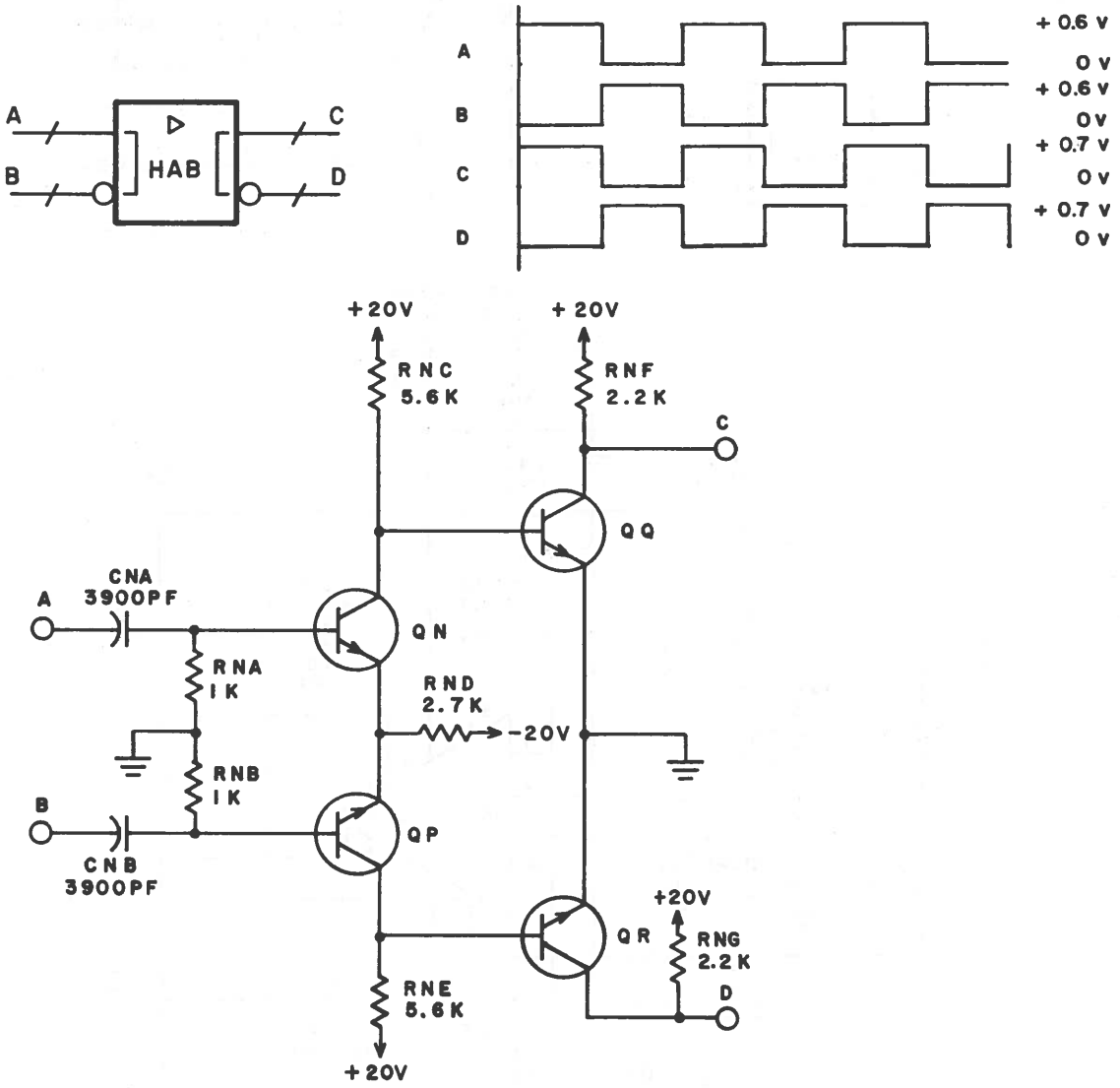


Figure 7-14. High Level Amplifier - HAB

When input A is positive, B is at 0v. Transistor QN is on and QP is off. The base of QQ falls to near ground. Transistor QQ is off. Output C rises to approximately +0.7v. With QP off, QR turns on. Output D falls to ground.

When input B is positive, A is at ground. Transistor QN is off, QP is on, QQ is on, and QR is off. Output C is at ground. Output B rises to +0.7v.

High Level Amplifier - HJA

The HJA circuit (Figure 7-15) increases the input signal power to transmit over a coaxial cable. The input is a differential signal of approximately 3.6v peak to peak.

The input signal across A and B is divided between resistors RNA and RNB. Transistors QN and QP are forward biases with a gain of 3. The -20v through resistor RNH and diodes CRNA and CRNB and through resistor RNJ and diodes CRNC and CRND forward biases QQ and QT, respectively. Transistors QQ and QT are in a common collector configuration to provide a current gain.

Transistors QR and QS are emitter followers that draw very little current from QQ and QT. They provide low impedance for discharging CNC and CND, thus reducing delay time when crossing the zero volt point.

Output voltage is approximately the same as input voltage. Output current is 20 ma maximum.

Differential Amplifier - HJC

The HJC circuit (Figure 7-16) is a differential amplifier with a voltage gain of 5 (14 db). The input/output waveforms shown on the figure are drawn for a situation where the track servo head is positioned between two tracks (of 406 tracks prerecorded alternately at 455 and 500 kHz) of the track servo disk pack surface. The beating together of the two frequencies causes the signal amplitude changes. The signal at maximum amplitude is an equal mixture of the 455 and 500 kHz frequencies. Transistors QP and QQ constitute a current source for the differential amplifier. Signal amplification occurs at transistors QN and QR. Transistors QS, QT, QU, and QV are the current buffers for the outputs.

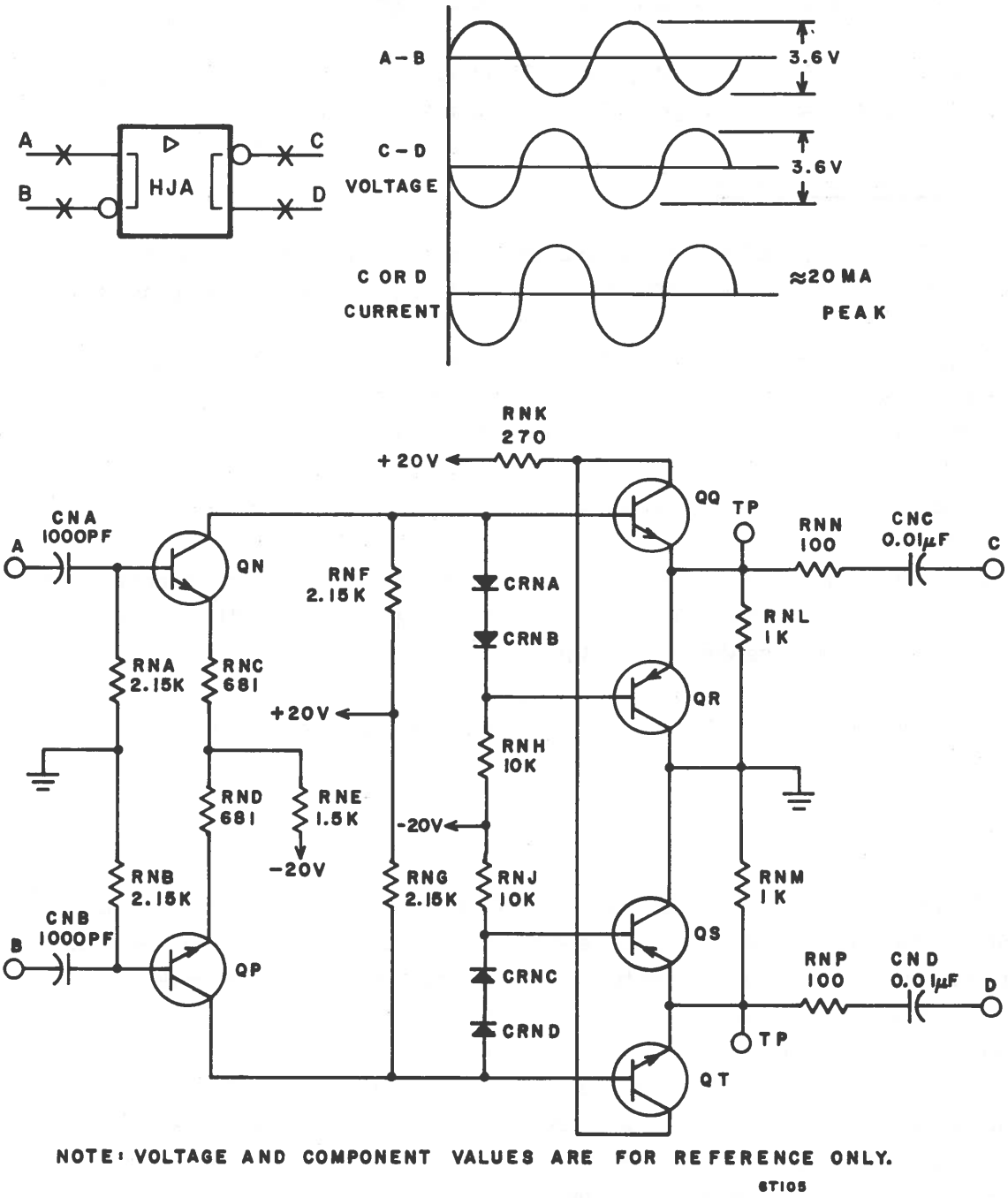


Figure 7-15. High Level Amplifier - HJA

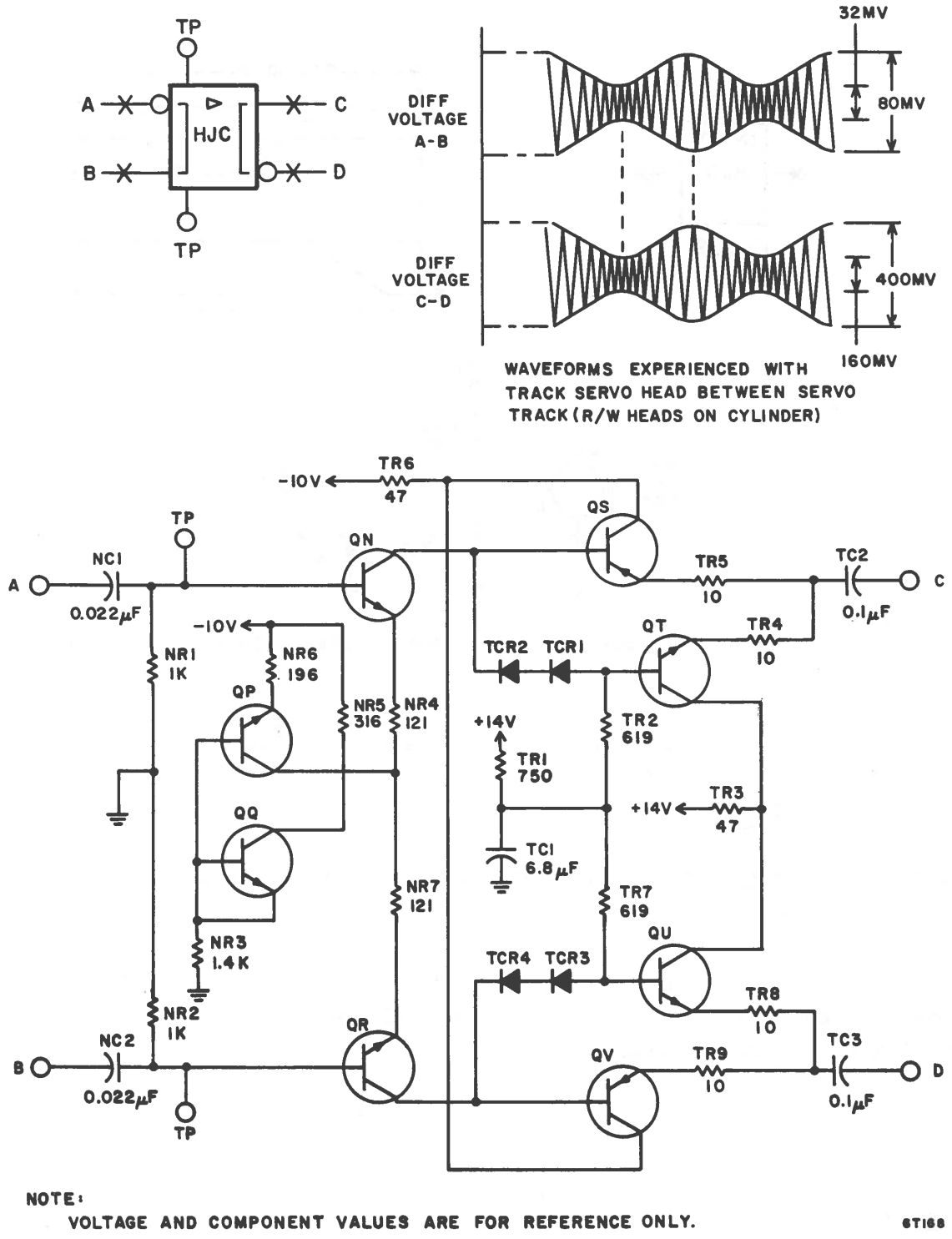


Figure 7-16. Differential Amplifier - HJC

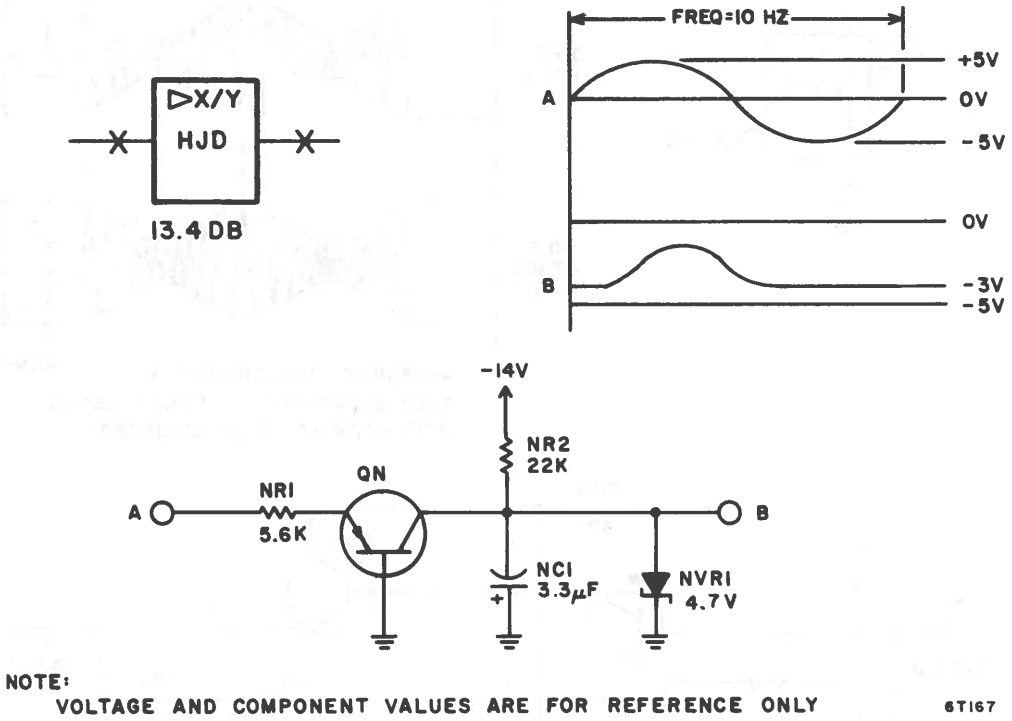


Figure 7-17. Amplifier/Level Translator - HJD

Amplifier/Level Translator - HJD

The HJD circuit (Figure 7-17) is an amplifier that provides a half-wave rectified, shifted output signal.

The output signal at B increases in a positive direction from a -3 vdc level. The output signal controls an N-channel JFET in an AGC loop that regulates the amplitude of the fine position servo signal.

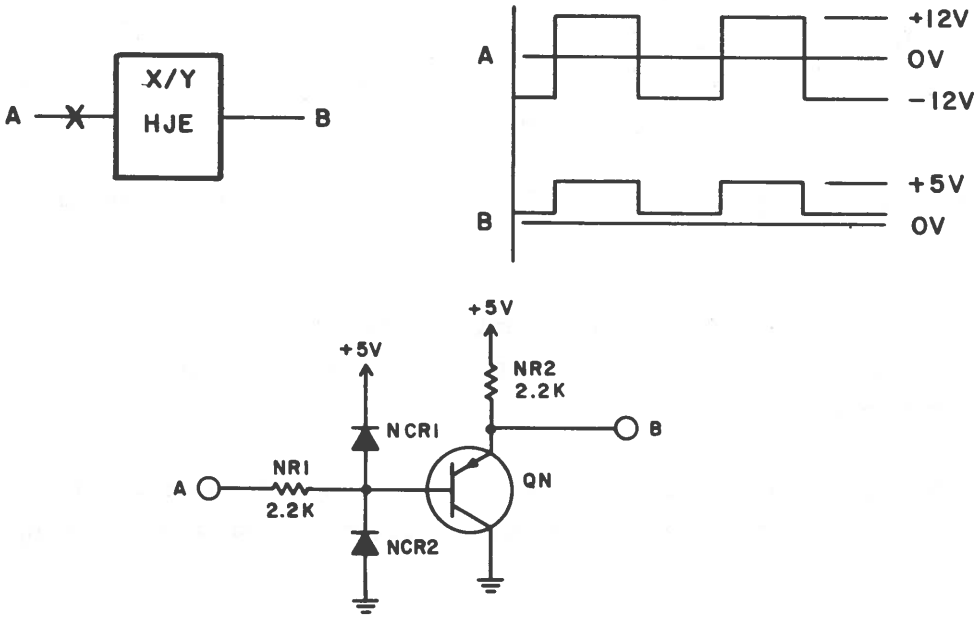


Figure 7-18. Level Translator - HJE

Level Translator - HJE

The HJE circuit (Figure 7-18) converts the output of an operational amplifier to a standard logic level.

When input A is at -12 volts, transistor QN is on. Diode NCR2 limits the input voltage at the base of QN to approximately -0.7 volt. Since the base to emitter voltage of QN is +0.8 volt, output B is at a level of approximately +0.1 volt.

When input A switches to +12 volts, QN becomes reverse biased and output B approaches +5 volts. The base voltage of QN is limited to approximately +5.7 volts by diode NCR1.

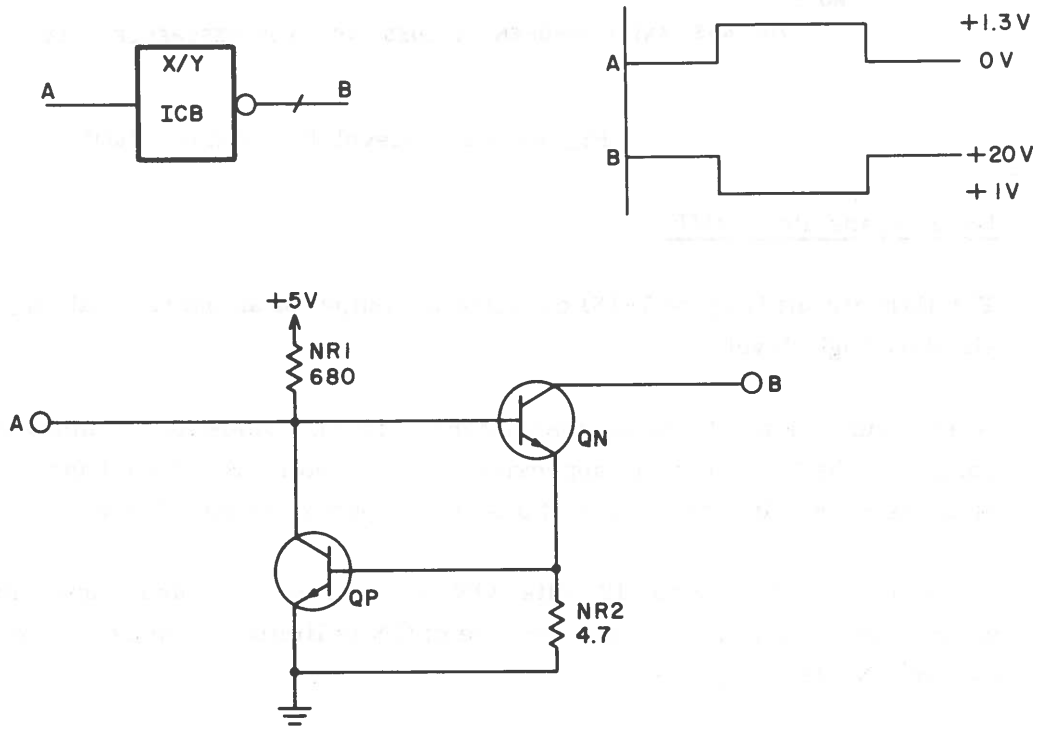
Lamp Driver - ICB

The ICB circuit (Figure 7-19) drives a lamp which terminates at +20v. The circuit is (and must be) driven by an open collector integrated circuit. The nominal current of the lamp must not exceed 100 ma.

When a high logical 1 is provided to the circuit input, transistor QN (and the lamp) turns on.

QP and NR2 serve as a current limiter. When approximately 140 ma flows through NR2, QP turns on and diverts base current from QN to ground. This prevents surge currents of greater than 140 ma.

A low (logical 0) at the input turns QN off, causing the circuit output to rise to the lamp termination voltage. With no path to ground available, the lamp turns off.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

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Figure 7-19. Lamp Driver - ICB

Write Driver - JAB

The JAB circuit (Figure 7-20) provides current to the write heads so that data may be recorded. Outputs E and F are connected to opposite ends of the write head, which is center tapped to ground. When input A is positive, current flows through output E to its half of the write head. When A is positive and the unit is writing, B is negative. When A is negative and the unit is writing, B is positive. Therefore, only one half of the write head may be activated at any one instant while the unit is writing.

With a positive charge on input A, transistor QN is off. The base of QR is positive and the emitter of QS is positive. The negative voltage at B turns transistor QT on. This drives the emitter of QR negative. Transistor QR conducts, driving the base of QQ to about -2v. Transistor QQ is an emitter follower, so the emitter QQ is also near -2v. The -2v on the base of QP turns QP off. No current flows through output F (-20v through resistor RNA only reverse biases an external diode). With QT on, the base of QS goes slightly negative. Transistor QS is off, allowing the base of QU to go to +40v. Transistor QU is an emitter follower, so the emitter of QU also goes to about +40v. The +40v on the base of QV turns QV on. Current now flows from a +40v supply connected to output G through transistor QV and its half of the write head to ground. A resistor lies between output E and the write head to limit the current flow in the write head.

When input A goes negative and B goes positive, QN and QS are on and QR and QT are off. On the bases of QQ and QU are currents of +40v and -2v, respectively. The emitter of QQ goes to about +40v. The emitter of QU goes to about -2v. Transistor QV is off. No current flows through output E. Transistor QP is on. Current flows from the +40v source connected to output G through QP and its half of the write head to ground.

Input D supplies a negative voltage when the unit is writing to reverse bias diodes CRNA and CRNF. If the unit is not writing, D is grounded and both inputs A and B go negative. This turns on QR and QS. Transistors QP and QV are, therefore, off and no current flows through the write head.

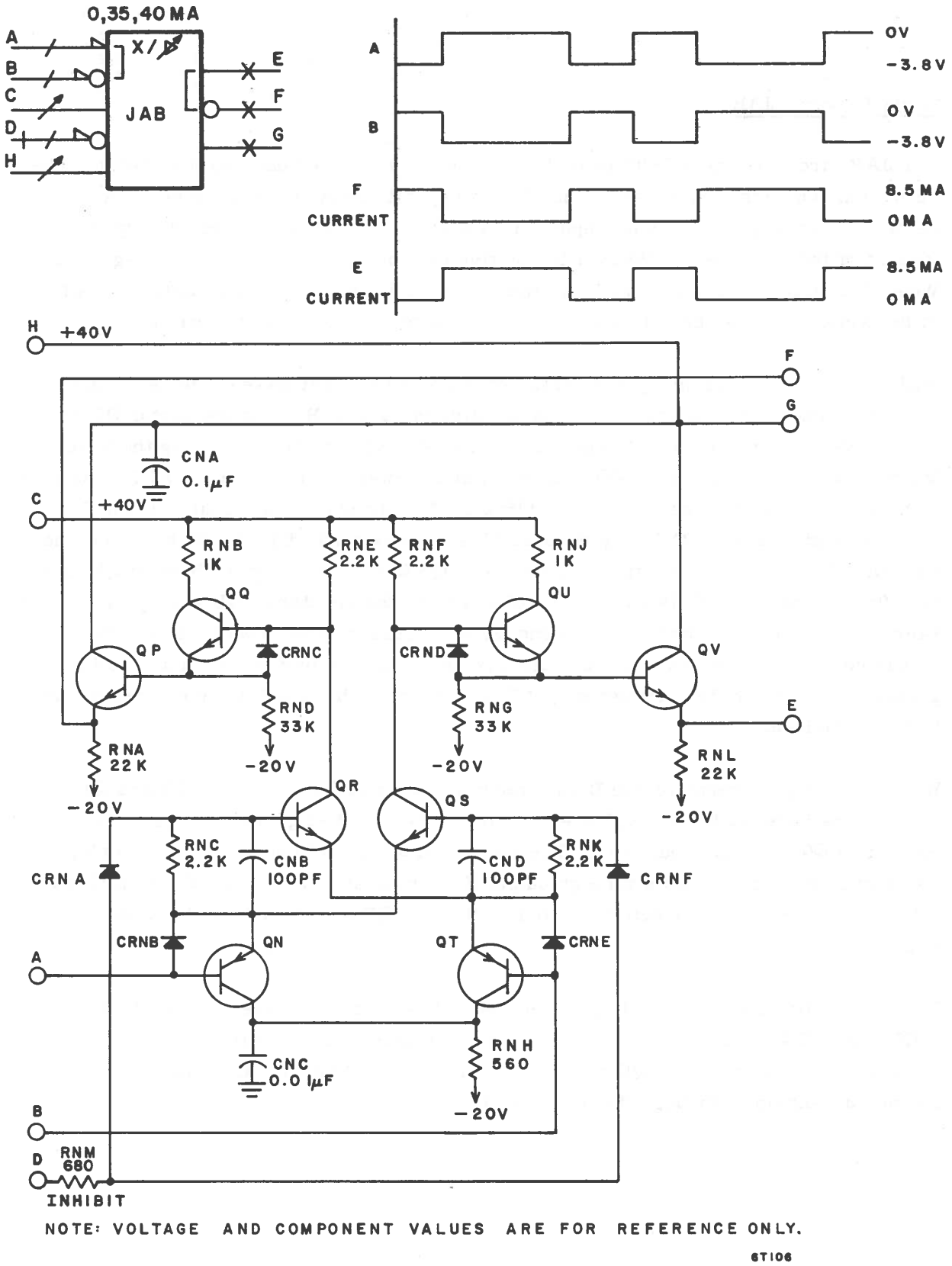


Figure 7-20. Write Driver - JAB

Erase Driver - JBB

The JBB circuit controls the current driving the erase heads. When input E (Figure 7-21) is a high voltage, output H provides current to erase heads.

When input E goes to a high voltage, capacitor CPA charges, causing a 10-μsec delay before transistors QR and QP turn on completely. Output G is connected to a +40v supply in a fault detect circuit. When QR is on, current flows from G through QR to the erase head connected to output H. The ramp output protects the information on neighboring tracks from being destroyed.

When E drops to 0v, CPA discharges through RPA. After 10 μsec, QP and QR are off. Output H is at 0v.

Line transmitter - LCA

The LCA circuit (Figure 7-22) provides a positive output at B and a negative output at C when input A is low. When the input is high, outputs B and C are at ground.

The circuit is (and must be) driven with an open collector integrated circuit. The LCA circuit input is a differential stage (QN and QP) which sinks the current from the minus and plus constant current sources (QQ and QR) whenever input A is high. When A is high, QN and QP are off and the 25 ma of current from the constant current sources is routed through the emitters of the differential output stages (QS and QT) to the outputs B and C. External Zener diodes on the plus and minus voltage supply lines serve as a common voltage divider for all circuits on one card and provide bias voltage to the constant current sources and the output transistors.

The complementary current sink (QN and QP) monitor a close phase relationship during turn-on and turn-off by having the emitter of QN (NPN) drive the emitter of QP (PNP). Returning the external resistor on the circuit input to +20 volts, instead of +5 volts, ensures that QN and QP will sink the drive current if the +5-volt power is lost.

NCR2, NCR4, NR7, and NR13 protect the transmitter if large externally produced transients should appear on the output lines.

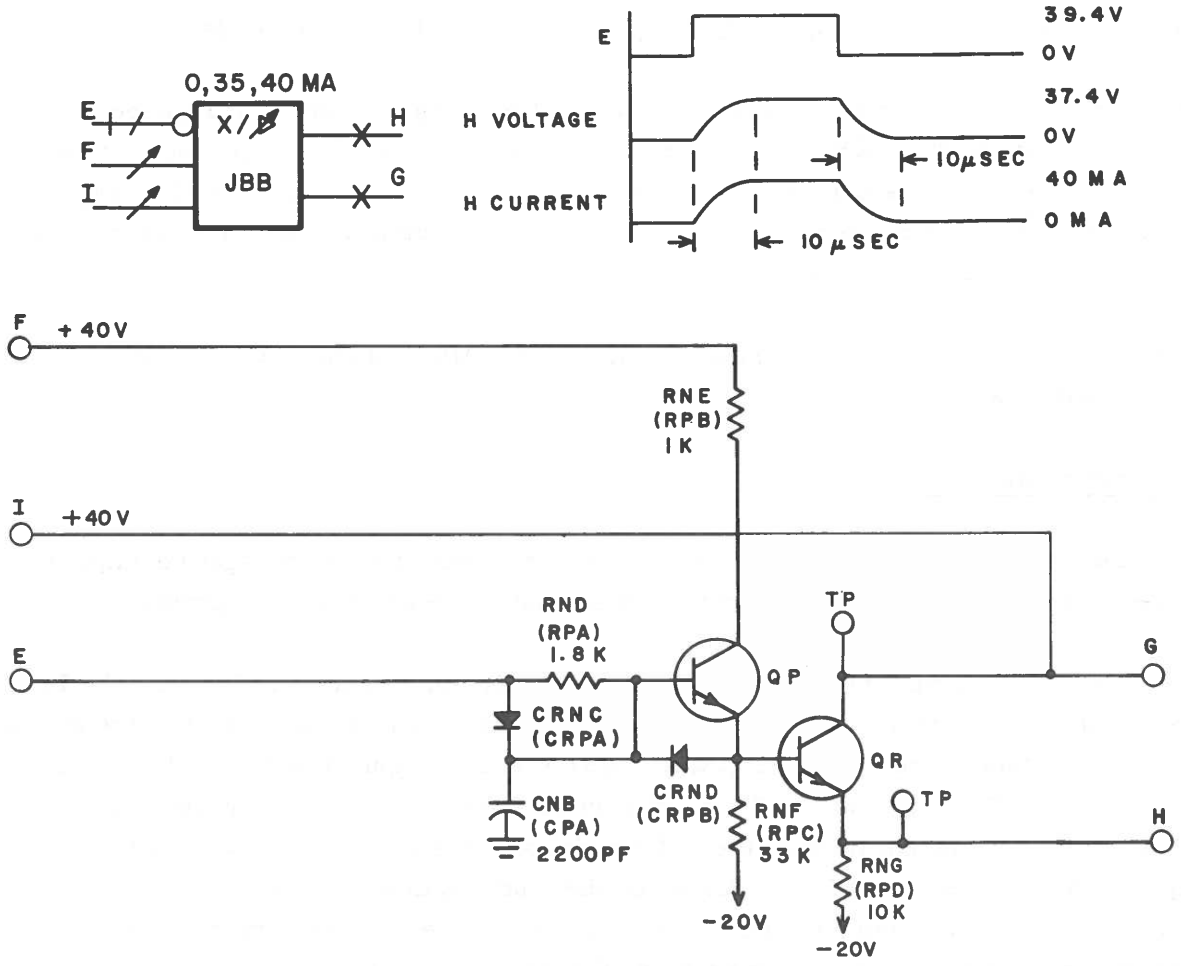


Figure 7-21. Erase Driver - JBB

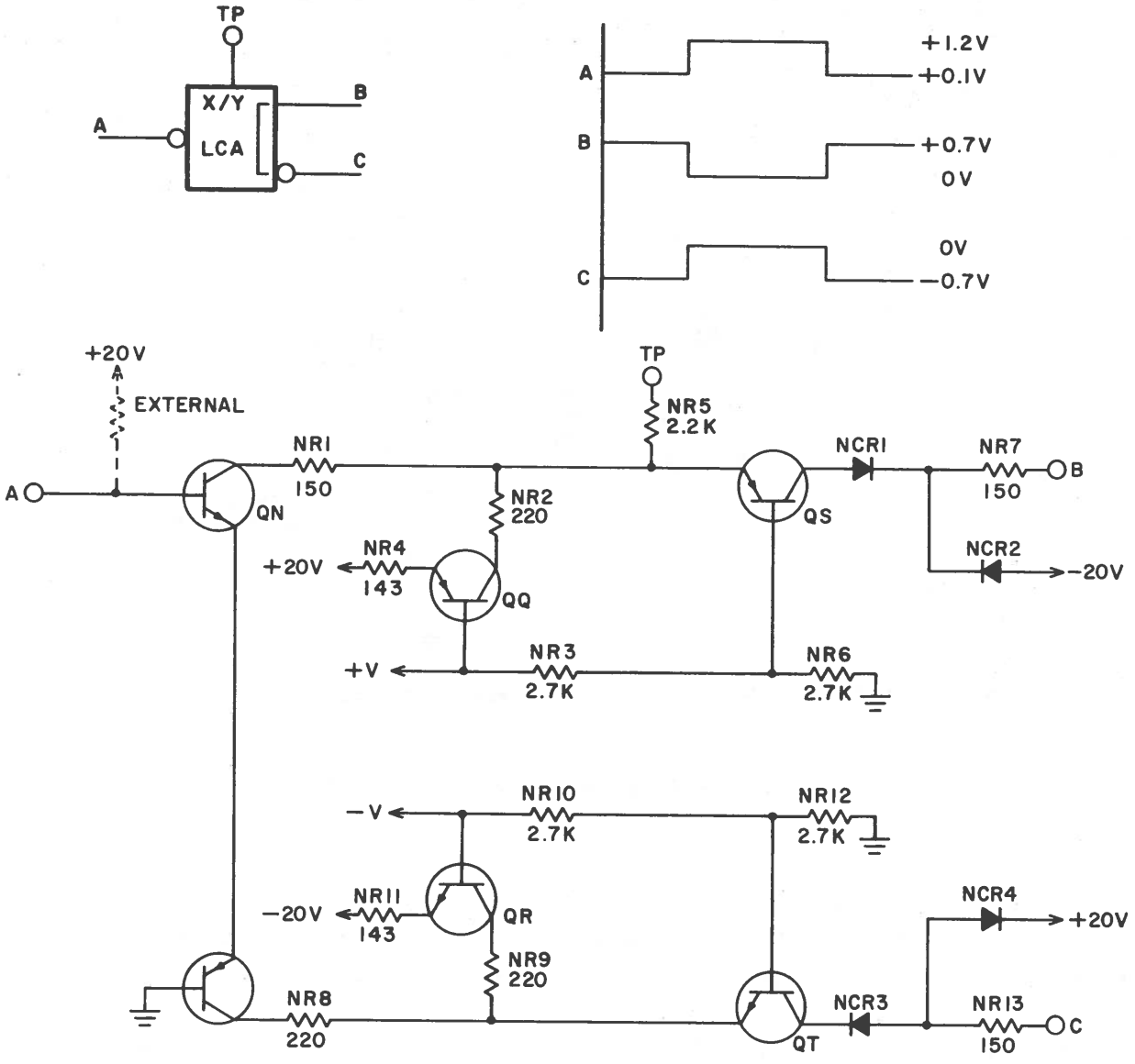


Figure 7-22. Line Transmitter - LCA

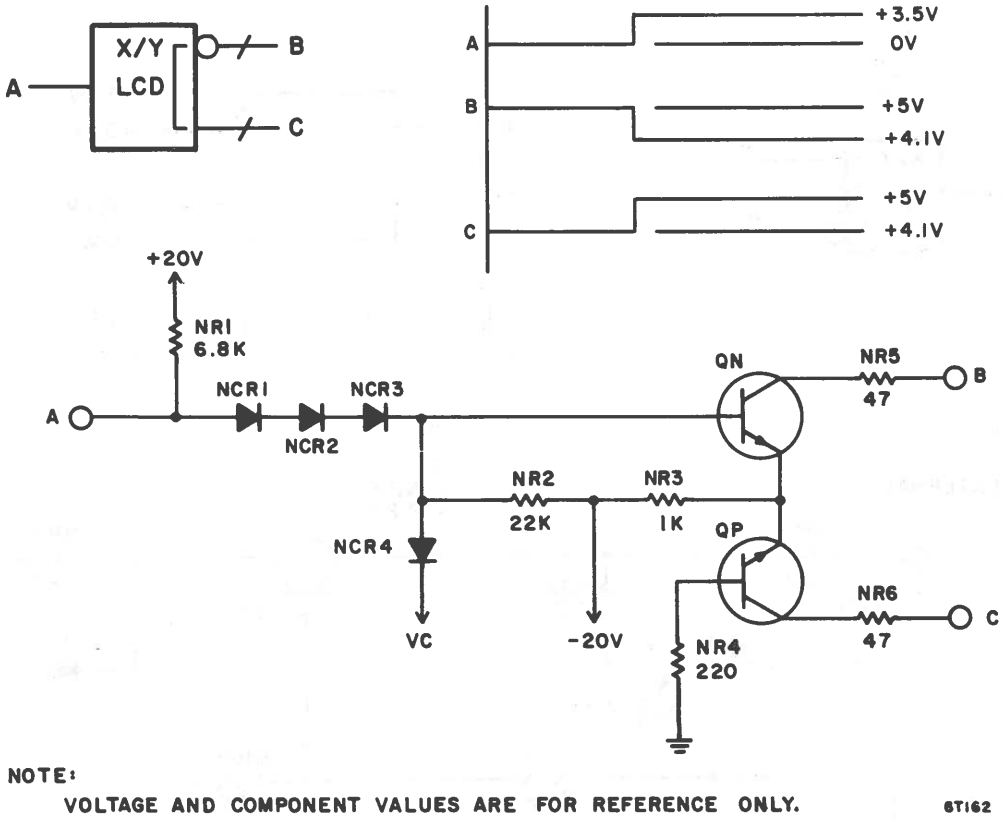


Figure 7-23. Line Transmitter - LCD

Line Transmitter - LCD

The LCD circuit (Figure 7-23) is a medium-speed, balanced-line, current transmitter. When input A goes high, transistor QN turns on and QP turns off. A 19-ma transmission line current across the 47-ohm external terminating resistor causes a 0.9-volt drop at B of the external +5-volt terminating voltage. Since QP is not conducting, the full +5-volt terminating voltage exists at output C.

When input A is a logic "0", transistor QP is on and QN is off. This situation causes a reversal of the previously stated voltage levels at outputs B and C.

Resistor NR3 and transistors QN and QP act as a constant current source. Diode NCR4 functions to limit the positive swing of QN's base.

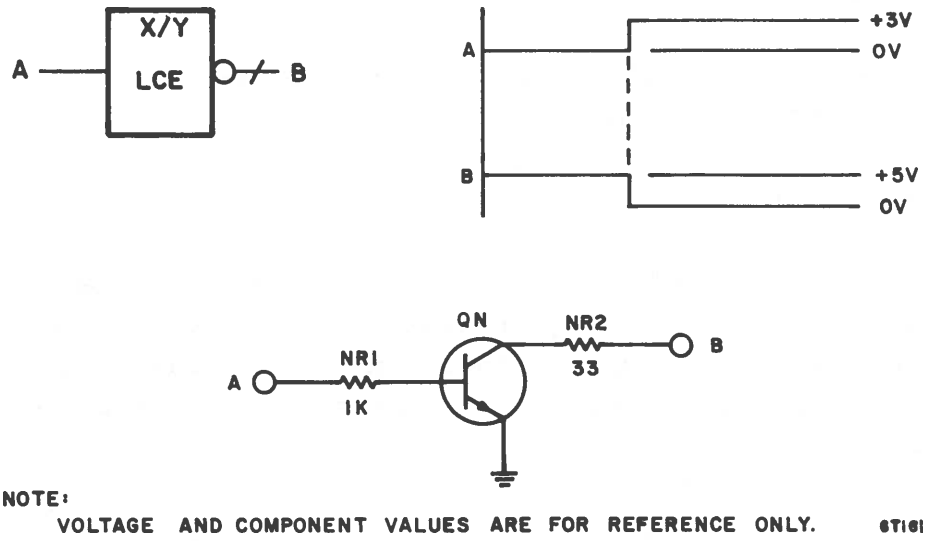


Figure 7-24. Line Transmitter - LCE

Line Transmitter - LCE

The LCE circuit (Figure 7-24) is a simple inverter used as a transmitter in a low speed transmission system. The pull-up voltage and resistor along with an integrating capacitor are located at the receiving end of the line connected to output B.

Ringing Amplifier - MBC

The MBC circuit (Figure 7-25) is a tuned amplifier which is rung by the negative clock and data pulses present at input A.

The tank circuit connected to the collector of QN is tuned (and is adjustable) to twice the frequency of the input data pulses (each data pulse falls between two clock pulses; absence of a data pulse is interpreted as a zero). The high Q of the circuit affords a flywheel effect and yields a sinusoidal signal that is almost totally free of peak shift.

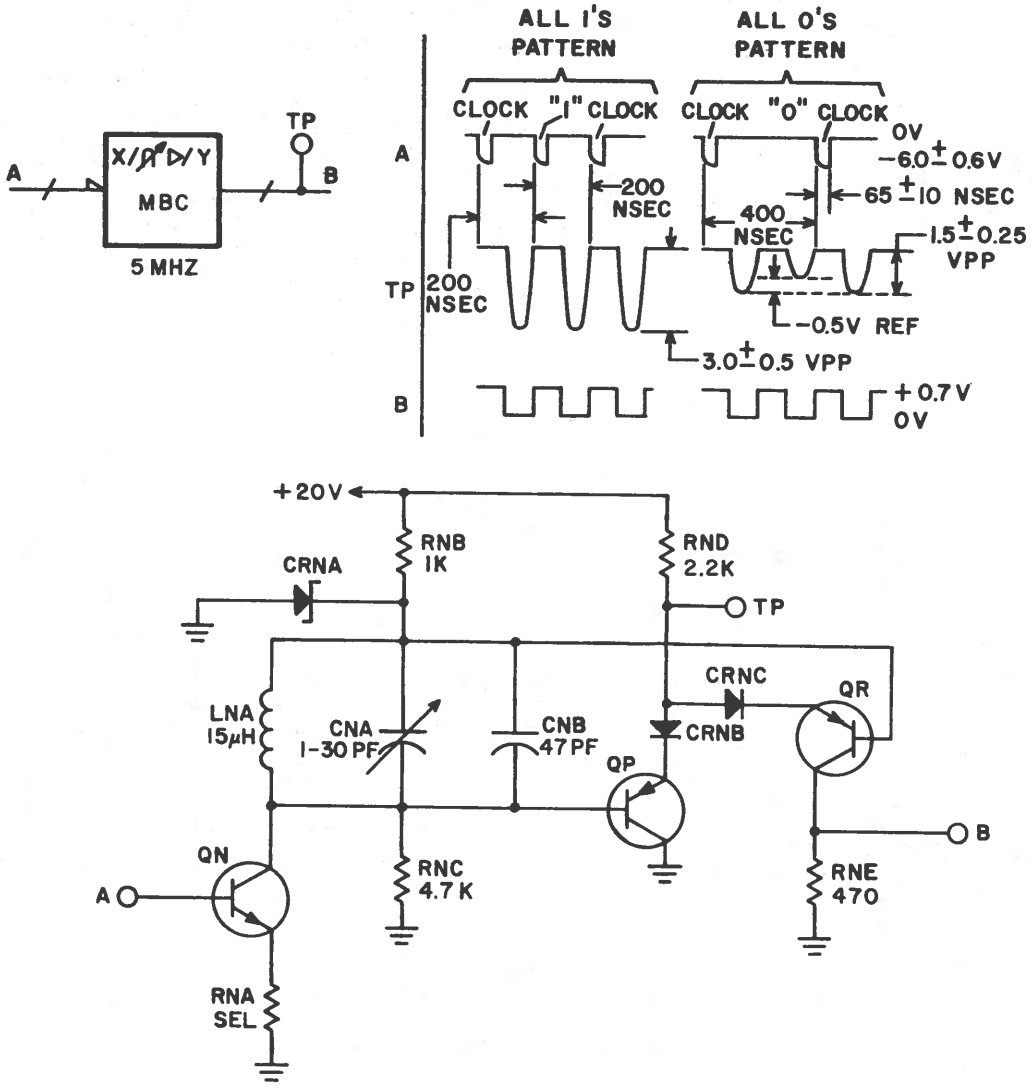
Transistors QP and QR form a zero-crossing detector, emitter follower circuit that provides high impedance so as not to distort the sine wave. The circuit clips the positive half of each sinusoidal excursion so that the signal at the TP is a half-wave rectified sine wave.

The transistor in the output lead (next circuit) functions to clamp this rectified signal and to provide what is nearly a square wave output at B.

Speed Detector - QDB

The QDB circuit (Figure 7-26) monitors sector pulses to determine whether the spindle is at a predetermined speed. If the spindle is below speed, no output is present. When the spindle reaches the desired speed (pulse rate of more than about 33 Hz), an output current activates the speed relay which signals the controller that the unit is up to speed.

Each time a sector is sensed, a short "1" pulse is applied at input A. Transistor QN conducts and completely discharges capacitor CNA through RND to ground. When the pulse is removed, CNA charges through RNC. When the base of QP reaches the voltage at the base of QR, AP and QQ turn off. Transistor QR conducts current to silicon controlled rectifier CRM, turning it on. Rectifier CRM draws current from the base of QS driving it to ground, and from the base of QR through RNK. The base of QR falls to about 9.03 volts. Transistor QR then turns on firmly and prevents "runt spikes" on the signal to CRM. Once CRM is turned on, CNB begins discharging through RNM and CRM. Rectifier CRM remains on until the discharge current from CNB falls below the holding current of CRM (typically 1ma). With the base of QS near ground, QS conducts. Transistor QT turns off, QU is on, and QV is off. No output signal is felt at B.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

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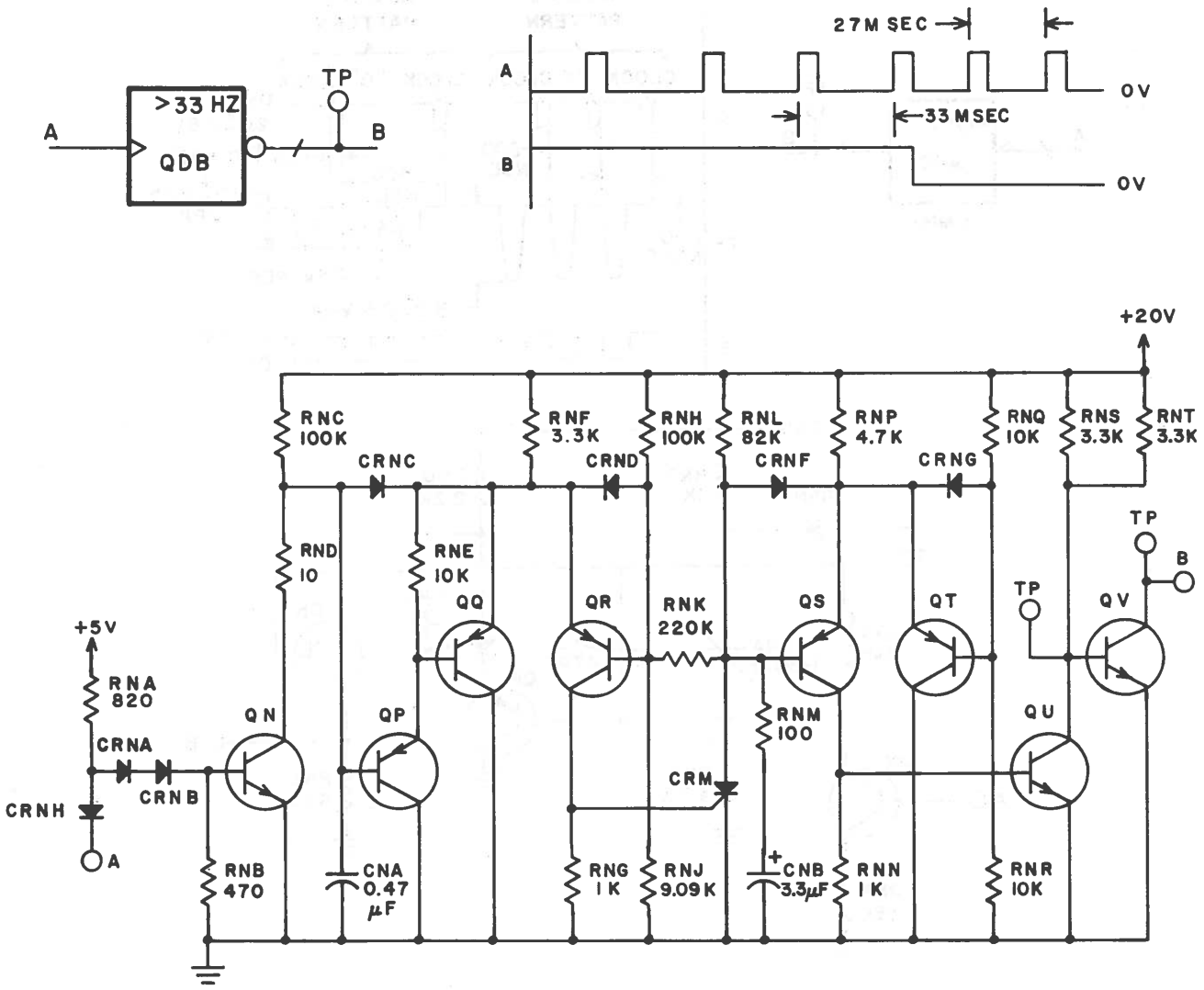
Figure 7-25. Ringing Amplifier - MBC



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

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Figure 7-26. Speed Detector - QDB

If the spindle is below speed, pulses arrive at the input at a low repetition rate. CNA repeatedly discharges and recharges to the point where QP and QQ are turned off. The output of QR is a series of positive pulses with a pulse width determined by $T = T_I - T_C$ where T_I is the time between input pulses and T_C is the time for CNA to change to the point where QP is turned off. The pulses repeatedly trigger CRM. CRM holds the voltage at the base of QS below the point where QS can turn off. Since QS is constantly on, QV is constantly off. No output is felt at B.

When the spindle reaches the required speed, the pulses at input A have the same period as T_C. The pulse width out of QR becomes $T_I - T_C = 0$. Transistor QR never emits a pulse. With no pulses out of QR, CRM never turns on. This permits CNB to charge to the point where QS is constantly off. The higher voltage at the base of QS is fed back to the base of QR through RNK to raise the voltage required across CNA to turn off QP. This feedback prevents rapid fluctuation of the output when the spindle is near the required speed. With QS constantly off, QU is off and QV is on. Current flowing through QV activates the speed relay connected to B, and signals the controller that the unit is up to speed.

Voltage Checker - QEB

The QEB circuit (Figure 7-27) detects any decrease in voltage supply greater than a specified percentage. A fault condition will occur if:

1. -20 supply decreases below -18v
2. +20 supply decreases below +18v
3. +40v supply decreases below +36v
4. -36v supply decreases below -28.8v
5. +36v supply decreases below +28.8v
6. -5v supply decreases below -4.75v
7. +5v supply decreases below +4.75v

If all positive supplies are normal, QR, QS, QT, and QU are off. Their emitters are held at +6.2v by Zener diode RVR1 and the value of RR9 (determined by testing to give a precise collector voltage). Current is pulled through QZ, causing a voltage drop across resistor RR13. This voltage drop turns QL on. Transistor QM turns off. If any of the voltage supplies drop below the specified percentage of their operating values, the respective transistor turns on. Transistor QZ will then be off. Transistor QL turns off. Transistor QM turns on, driving the output to ground.

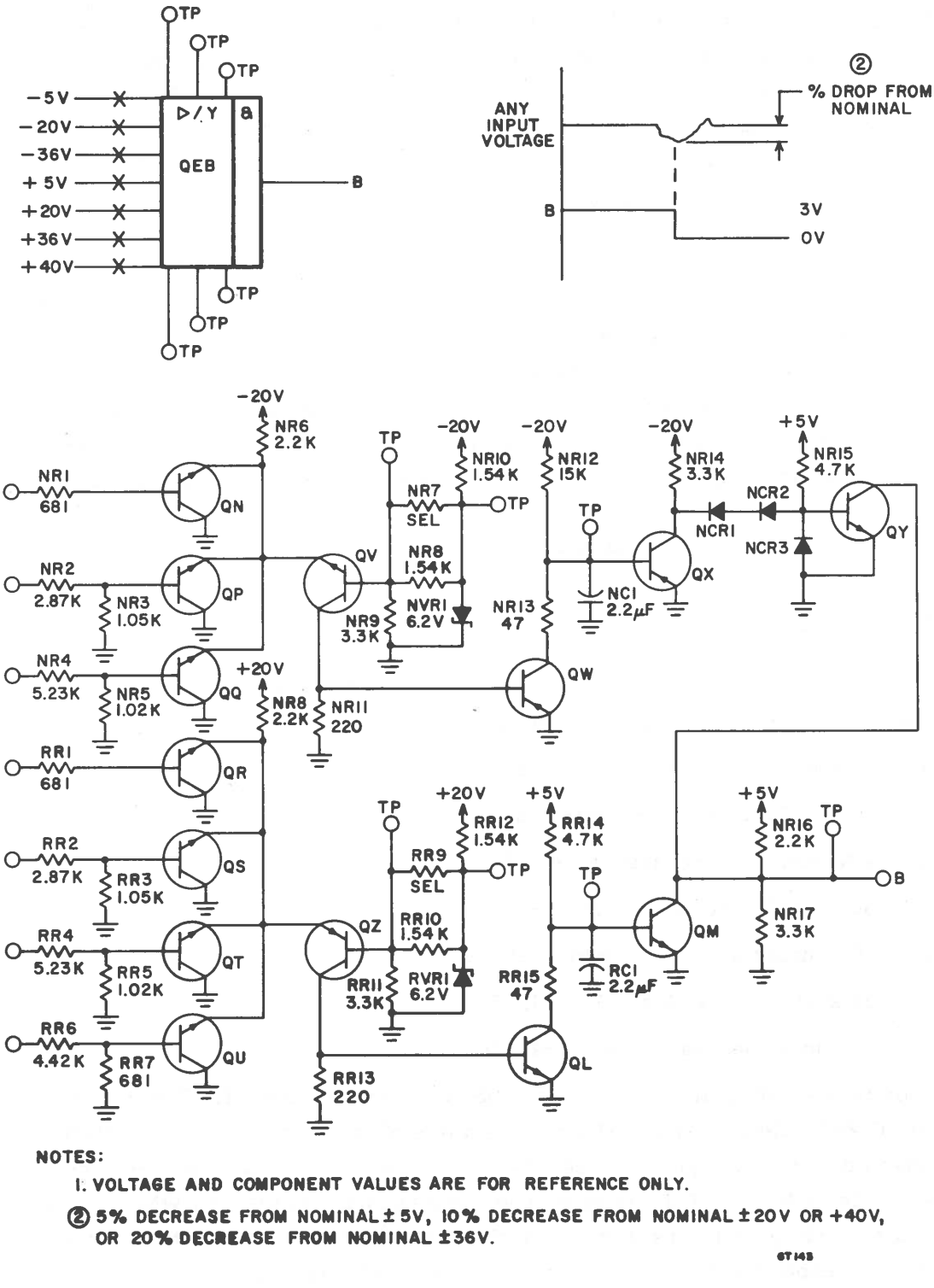


Figure 7-27. Voltage Checker - QEB

The negative voltage segment of the circuit is similar to the positive section. A decrease in the -20v supply below -18v will turn QP on. Transistor QV turns off, causing QW to turn off. Transistor QX turns on, causing a voltage drop across NR14 which turns QY on. The output drops to ground.

Quantizing Detector - QFA

The QFA circuit (Figure 7-28) detects a fault in the write and erase drivers or in the head select circuit. If there is an open in the head, either of the drivers is non-functional, or more than one head is selected, a fault signal occurs.

Inputs A and B are connected to the write and erase driver circuits and enter across a voltage bridge to the base of QP. Normally, both inputs are approximately 32v. All diodes are forward biased. Voltage on the base of QP is 32v and the emitter is at 31.4v due to a reverse bias 0.6v base-emitter voltage across QP. Transistor QP is off. All input current goes to ground through RND.

If input A is higher than input B by 1.4v, CRNB and CRNC are forward biased. CRNA and CRND are reverse biased. The voltage on the base of QP becomes that of input B. The emitter of QP is 0.7v higher than the base due to a 0.7v drop across CRNB. Transistor QP is on.

If input B is higher than input A by 1.4v, CRNA and CRND are forward biased. CRNB and CRNC are reverse biased. The base of QP is at the voltage of input A. The emitter of QP is 0.7v higher than the base. Transistor QP is on.

Input C is connected to the head select circuits. If more than one head is selected, the drop in effective resistance (due to external resistors in parallel) results in an increase in current through RNA. This increases the voltage drop across RNA, turning QN on.

If either QN or QP is on, QR turns on. Output D goes to ground to signify a fault condition.

Quantizing Detector - QFB

The QFB circuit (Figure 7-29) is used to amplify and shape an incoming wave. The input at A and B is a differential sine wave. The output at C and D is an amplified and clipped version of the input wave.

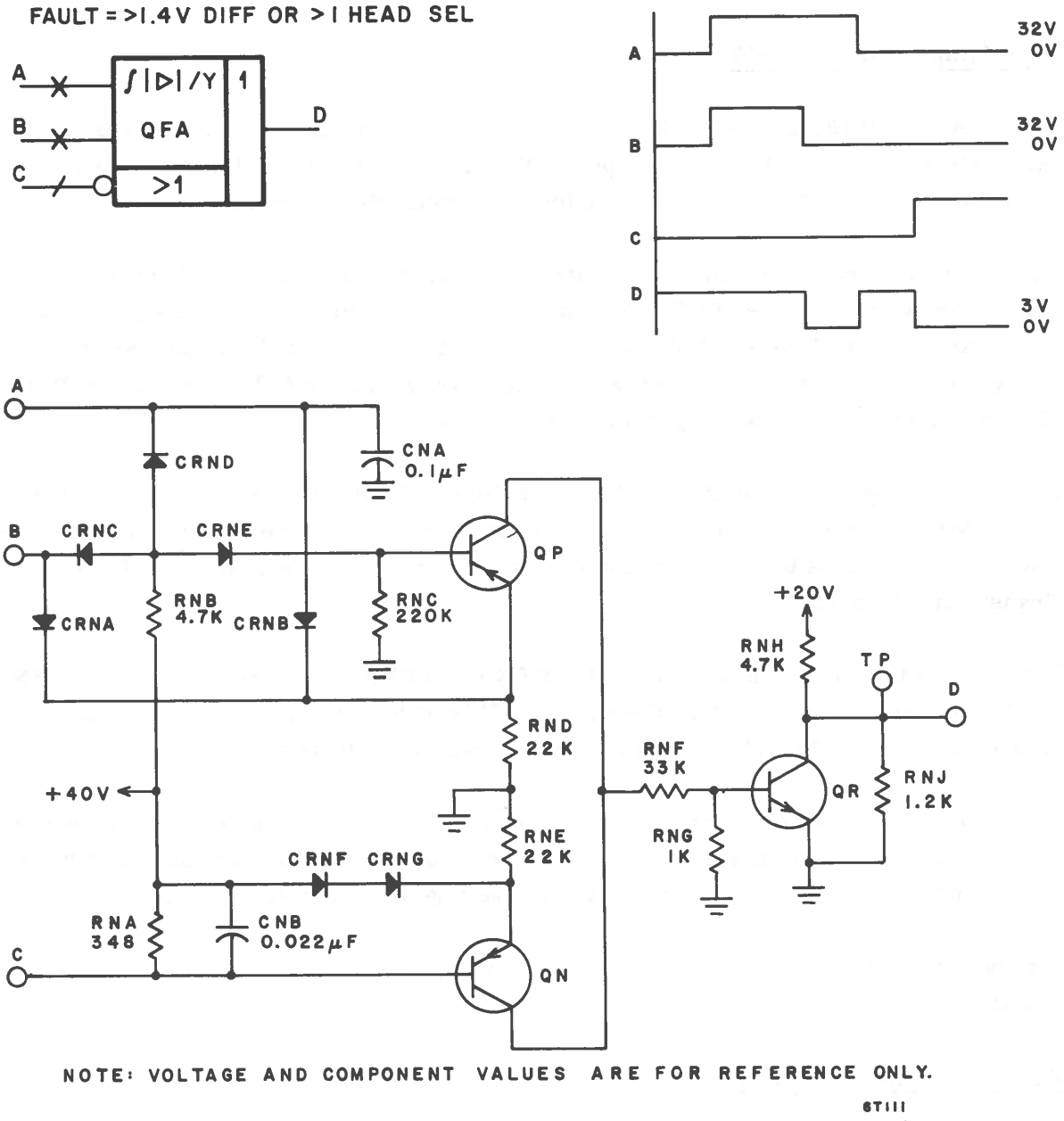


Figure 7-28. Quantizing Detector - QFA

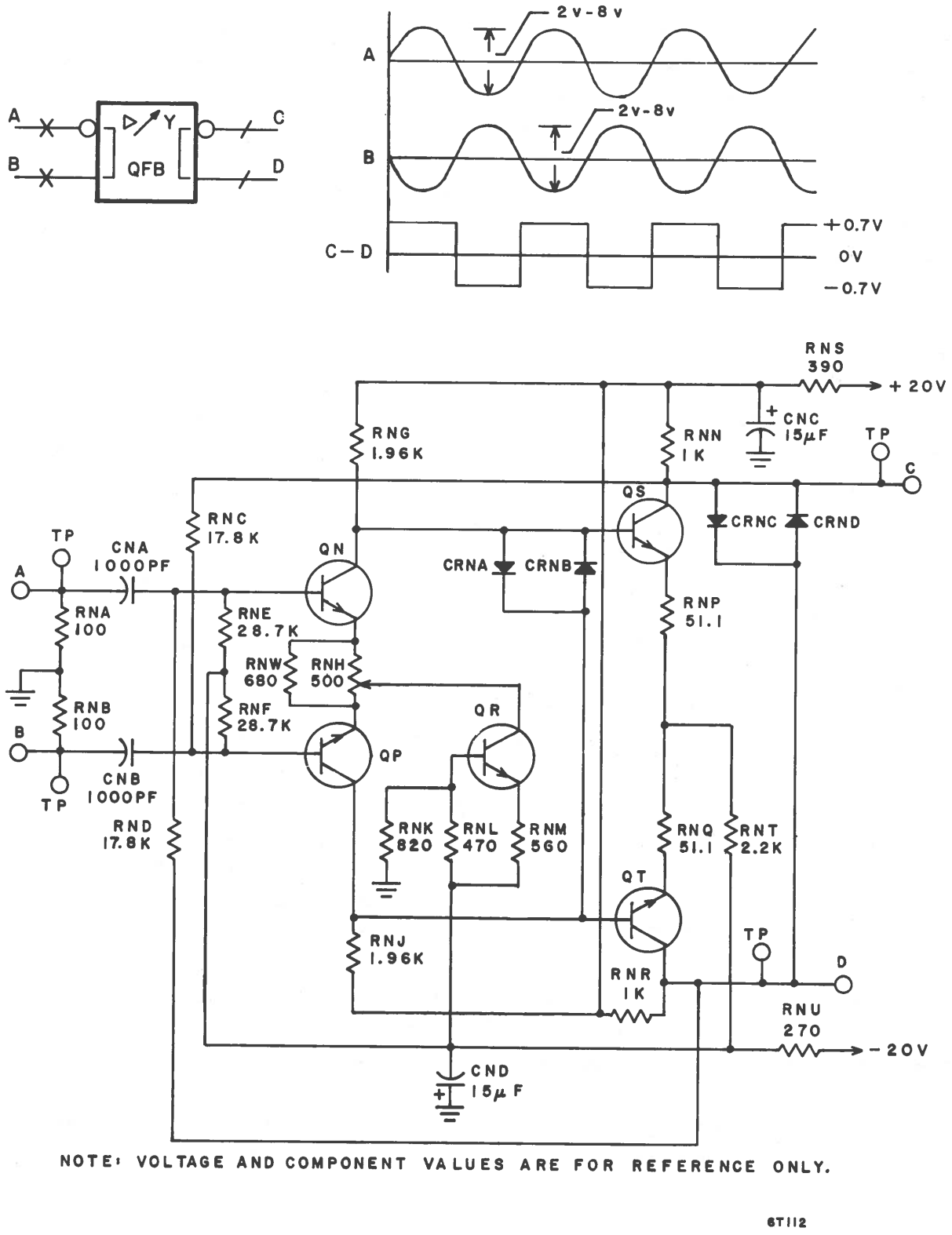


Figure 7-29. Quantizing Detector - QFB

Transistor QR is the current source for the differential amplifier stage consisting of QN and QP. Capacitors CNA and CNB filter out dc and low frequency noise and pass the input wave which alternately turns on QN and QP. The output at the collectors of QN and QP are clipped by diodes CRNA and CRNB to approximate a square wave. This square wave is fed to the bases of QS and QT for another stage of differential amplification. The square wave output at the collectors of QS and QT is again clipped by diodes CRNC and CRND. The output at C and D is a clipped, square wave between 0v and +0.6v corresponding to the rise and fall of the sine wave at inputs A and B, respectively.

Single Shot - QFF

The QFF circuit (Figure 7-30) produces a positive pulse output in response to a positive input pulse. The width of the output pulse is independent of the input and is adjustable.

Assume a condition where QN is on. With the collector of QN at ground, AP turns off and CNC begins charging (through RNL to ground via QN and QS) toward Vcc volts. The duration of the charging period is controlled by the time constant RNL X CNC. When the base of QQ reaches 0.7v, QQ turns on, QS truns off, and the output goes to ground.

With the circuit in the condition of the preceding paragraph, a no-signal state will have the following effect: Ground level at base of QN turns it off. Since QS is also off, current is drawn through the base of QP and turns it on. Current now flows through QP charging CNC in the opposite direction (from preceding paragraph) to about -5.3v (Zener diode CRNC voltage minus the 0.7 base-emitter voltage of QQ). As the current increases and decreases (during charging period) through QP, the remaining current still flows through RNL, thereby keeping QQ on.

Transistor QN turns on when a clock or data pulse is applied to its base. With the QN collector at ground, QP turns off and a -5.3 base-emitter voltage appears across QQ. Capacitor CNC again charges through the variable resistor RNL until QQ turns on.

When the circuit has been adjusted so that the width of the output pulse exceeds that of the input pulse, QS stays on (after the input drops) to hold the base of QP at ground.

Whenever CNC is charging through RNL with current flowing through RNN, QN and QS are on to conduct the increase current.

Capacitor CND is a filter capacitor to provide a constant voltage across CRNC.

Function Generator - QGD

The QGD circuit (Figure 7-31) is a non-linear feedback network used as the gain determining element for an operational amplifier.

With a 10K input resistor, an amplifier with the QGD circuit will exhibit high gain characteristics for amplifier output voltages of less than ±2v. A gain of unity is achieved at output voltages of ±5v with this gain persisting at higher voltages.

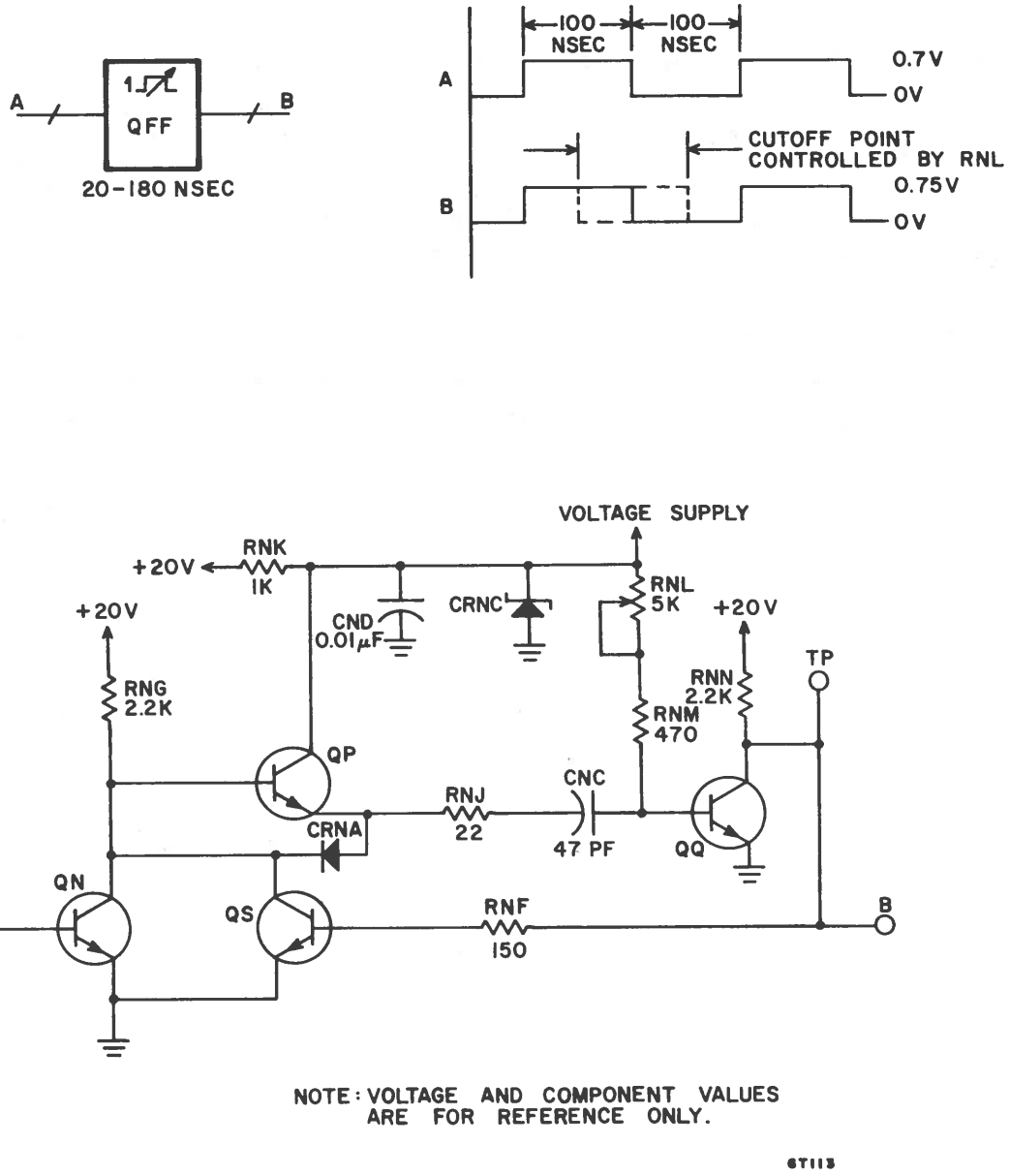
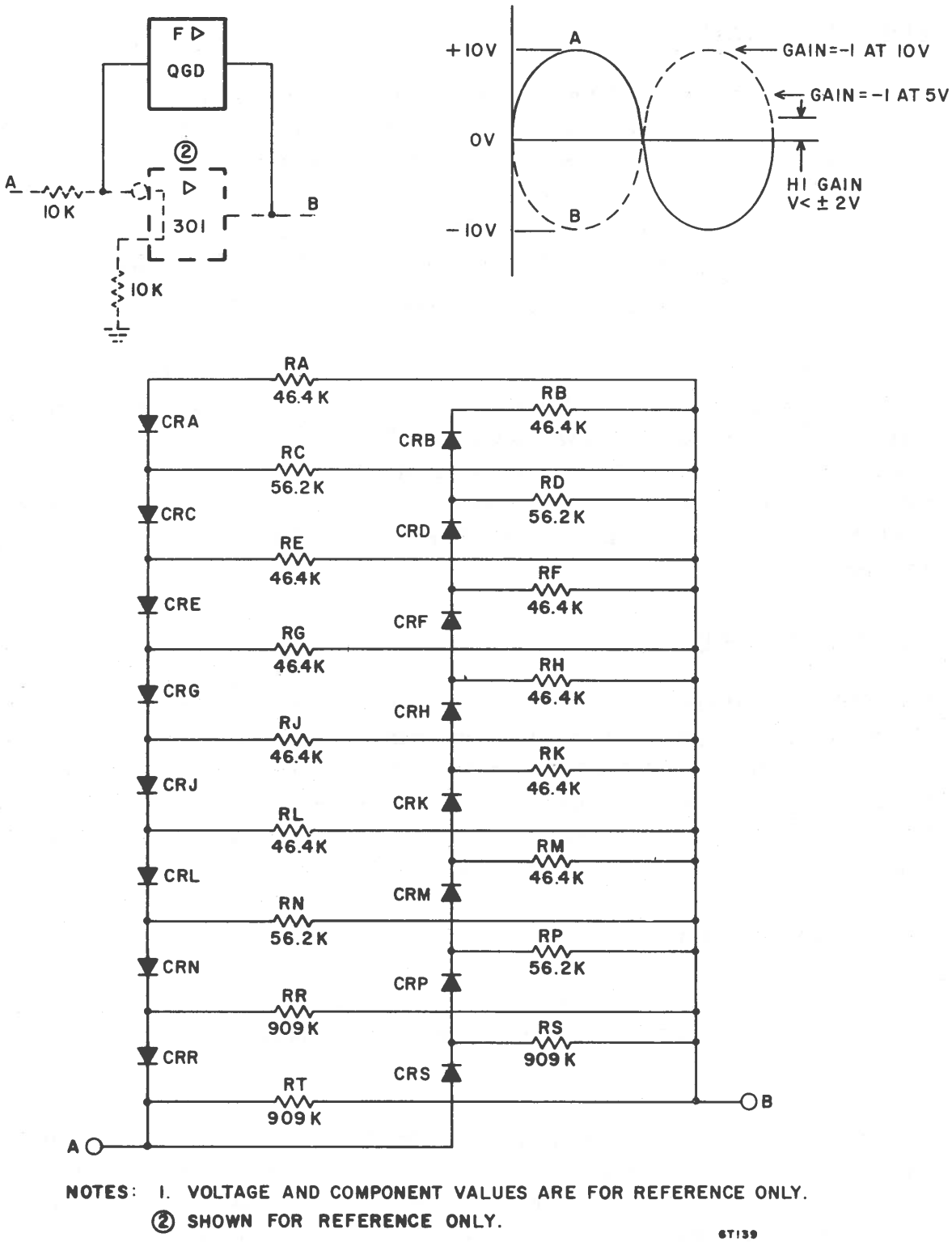


Figure 7-30. Single Shot - QFF



NOTES: 1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
② SHOWN FOR REFERENCE ONLY.

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Figure 7-31. Function Generator - QGD

Line Receiver - RAC

The RAC circuit (Figure 7-32) has an input threshold of -19.5 vdc nominal. A voltage more negative than -19.5 volts at A results in an output of +5 vdc at B. An input that is less negative than -19.5 vdc causes a circuit output of 0 volts.

NOTE

In actual application the signal to input A is -30 vdc through a 1.6K-ohm resistor (located in interfacing controller) so that the circuit input threshold is actually -23.5 vdc.

Transistors QN and QP form a voltage comparison circuit with a reference voltage on the base of QP of -2.5 volts. When the voltage at input A is more positive than the threshold, QN turns on causing QQ to turn on. With QQ conducting, diodes NCR1, 2, and 3 are forward biased. This causes transistor QR to turn on and pull output B to 0 volts. A situation where input A is more negative than the input threshold, turns QN and QQ off. The reverse bias on NCR1, 2, and 3 holds QR off, and output B becomes +5 volts.

Line Receiver - RAD

The RAD circuit (Figure 7-33) is a medium-speed, differential line receiver. The circuit provides a logic "1" at output C whenever input A is +5 volts and input B is less than +5 volts (normally +4.1 volts). Reversing the voltage levels at the differential inputs will cause a logic "0" output from the circuit. Resistors NR1 and NR2 are the line terminations. Resistor NR3 limits the base drive to transistor QQ when QN is on (input A low). Diodes NCR1 and NCR2 are used to optimize the switching level of QQ.

Switch Receiver - RCB

Switch receiver RCB (Figure 7-34) produces a "1" (+3v) output at B when the grounded switch connected to input A is closed. When the switch is open, a "0" (0v) is felt at output B.

A switch to ground is connected to input A. When this switch is open, capacitor NC1 approaches +5v and QN is shut off. Transistor QP is, therefore, on and conducts current to the base of QQ through resistor NR6. Transistor QQ turns on, conducting current away from output B, and drops the output to near ground or a "0".

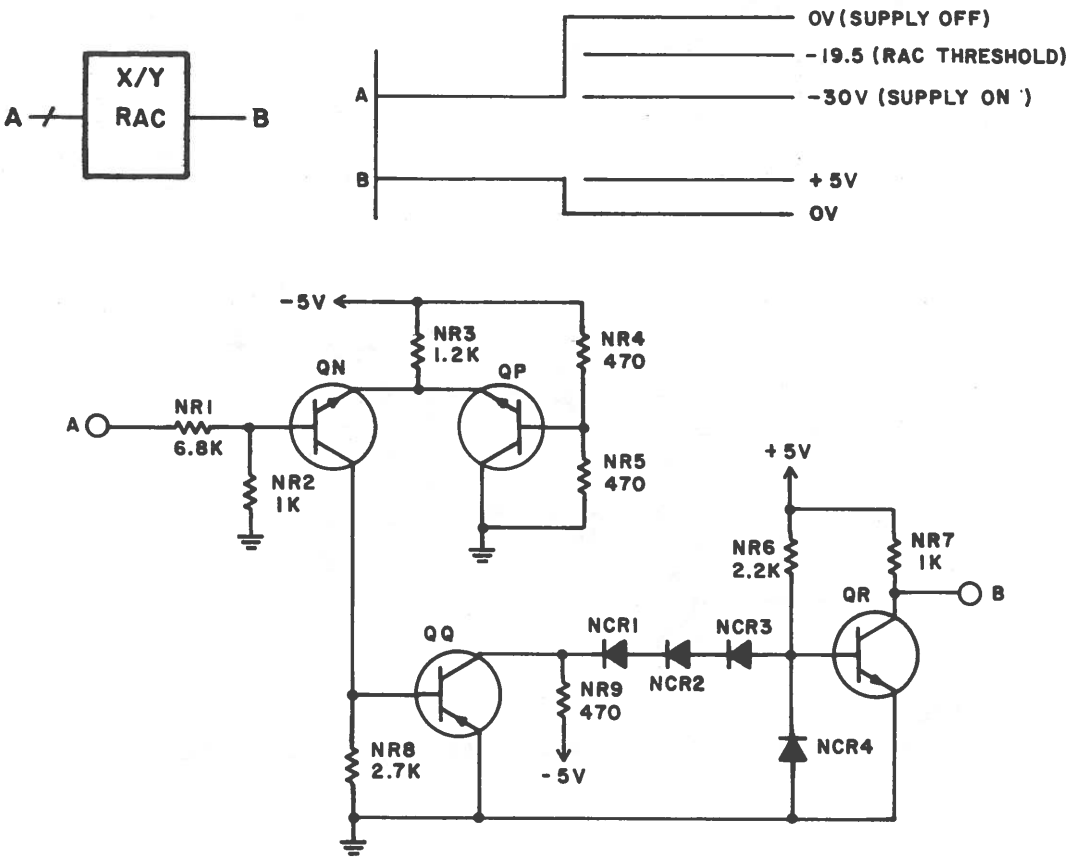


Figure 7-32. Line Receiver - RAC

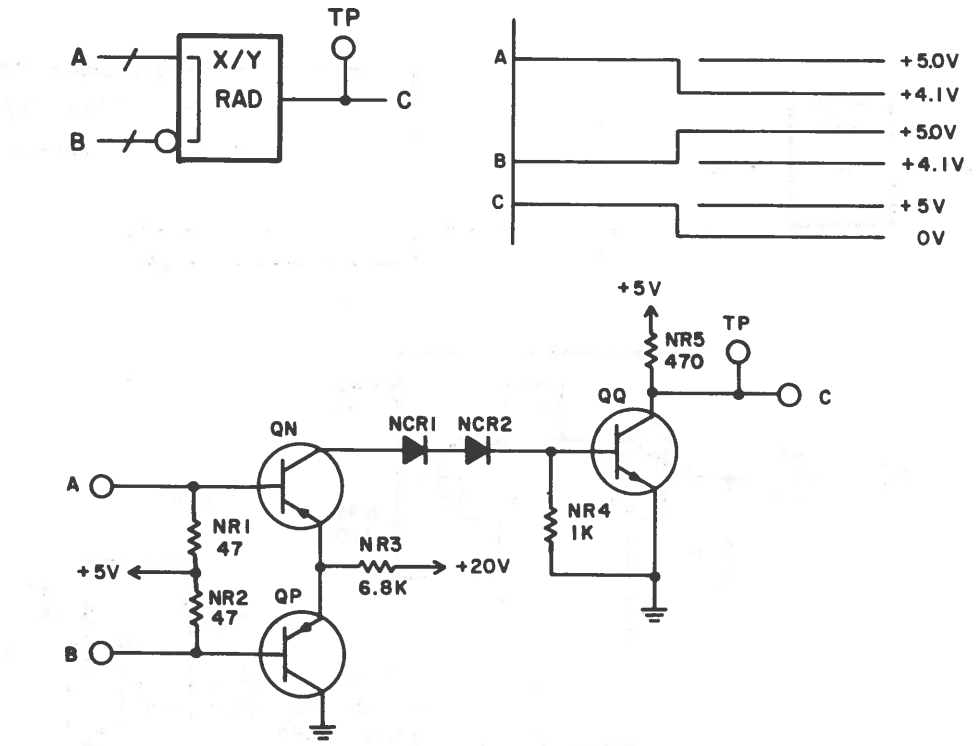


Figure 7-33. Line Receiver - RAD

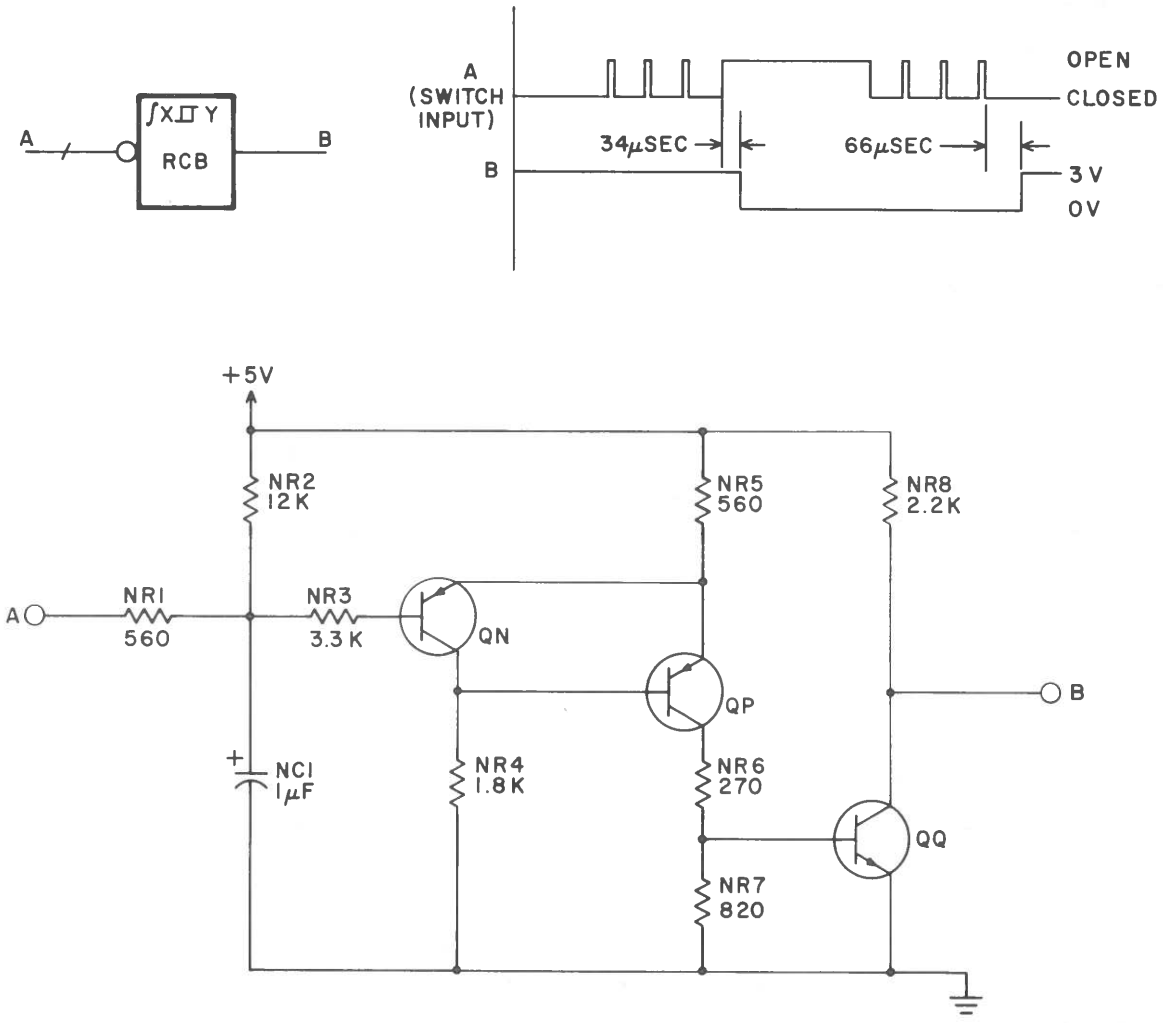


Figure 7-34. Switch Receiver - RCB

When the switch is closed, the voltage across NC1 rapidly increases through NR1 and the switch to ground because of the short time constant of NR1 and NC1. Any contact bounce on the switch will increase the discharge time. As the voltage across NC1 decreases, QN begins to turn on. As QN conducts current to the base of QP, the forward bias on QP is decreased and QP begins to turn off. As QP turns off, the current through NR5 decreases due to the higher lead resistance (NR4) of QN compared with QP (NR6). The current drop through NR5 causes a decrease in the voltage drop across NR5. The bias on QN is, therefore, increased. The cycle goes rapidly to completion. Transistor QP is shut off. With QP off, the base of QQ is near ground, causing QQ to shut off. This allows the +5v supply to flow through NR8 to output B, raising the output to +3v, "1".

When the switch is opened again, NC1 charges slowly to +5v due to the long time constant of NR2 and NC1. Any contact bounce on the switch will hold NC1 well below the switching level of QN until the bouncing ceases. As the voltage across NC1 increases, QN begins to turn off. Transistor QP begins to conduct current away from the emitter of QN. Transistor QP turns on rapidly because of this positive feedback. The output then returns to "0".

Line Receiver - RFA

The RFA circuit (Figure 7-35) provides a non-standard "0" output at C when input A is at least 0.6v more negative than input B. Diode CRNA holds the threshold at 0.6v. Under all other input conditions, the output will be a non-standard "1".

If the differential input (A-B) is greater than 0.6v, transistor QP turns on and QN turns off. This drives the base of transistor QR more positive than the base of QQ. Transistor QR conducts current from the -20v supply, through RNK to ground. The output at C is near 0v.

If the differential input (A-B) is less than 0.6v, QN turns on and QP turns off. The base of QQ goes more positive than the base of QR. Transistor QQ conducts and a negative voltage is felt at output C.

Since a "1" is defined in MDD logic as the most positive voltage, the 0v output in the first case is interpreted as a non-standard level "1". The negative voltage output in the second case is, therefore, a non-standard level "0".

The receiver is self-terminated with 56 ohms to ground on each line.

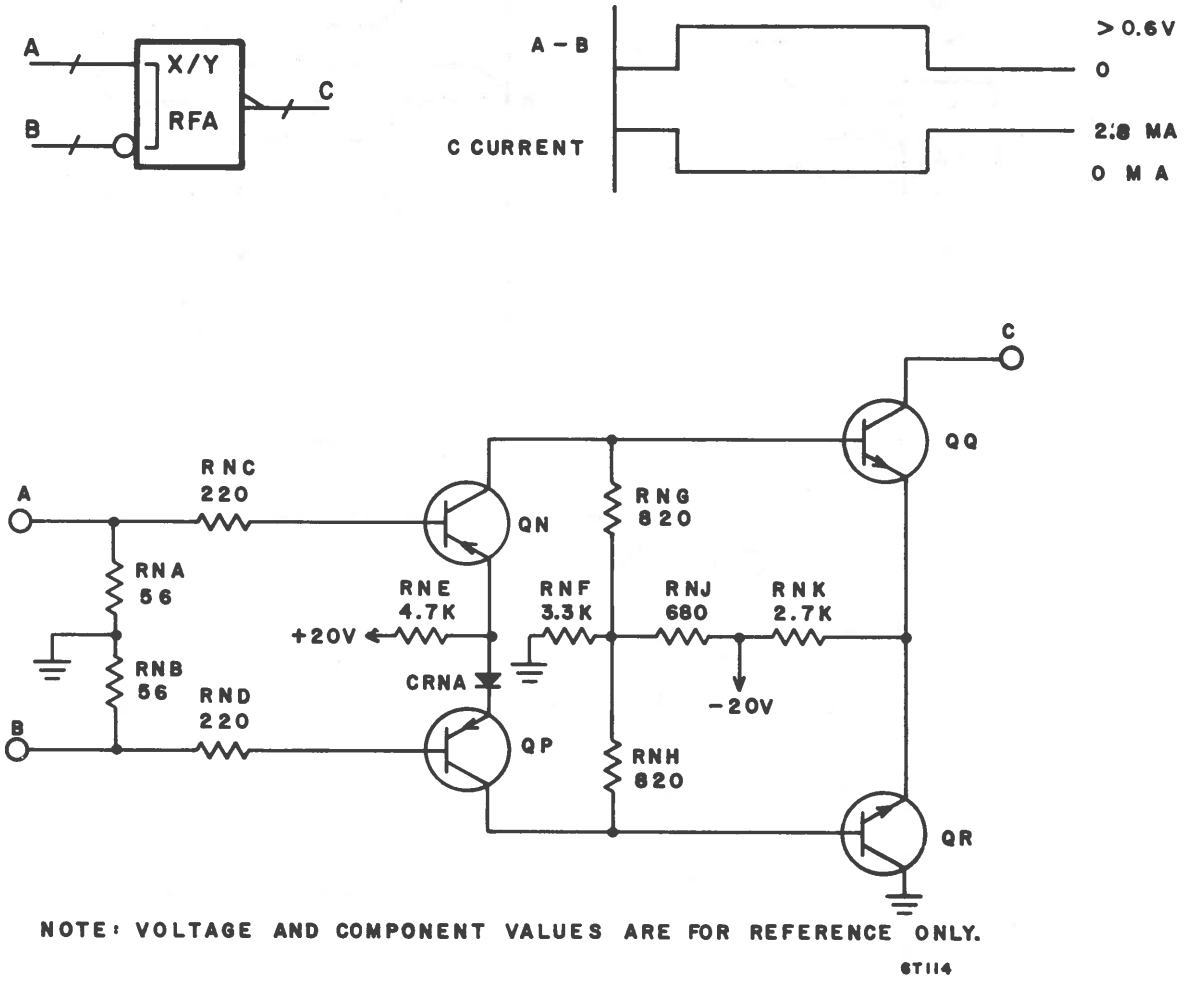
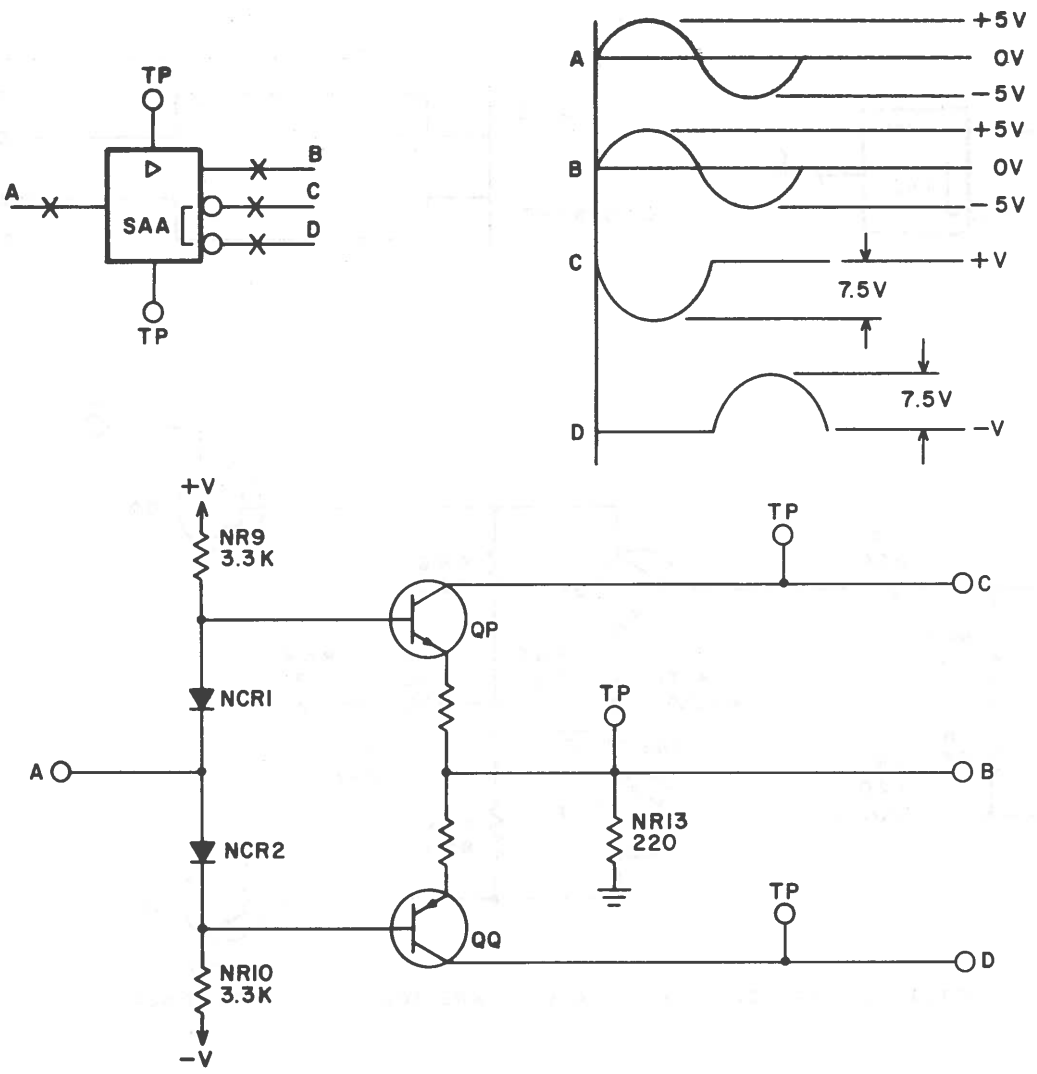


Figure 7-35. Line Receiver - RFA

Bipolar Current Buffer - SAA

The SAA circuit (Figure 7-36) is a power output stage for an operational amplifier. Transistors QP and QQ comprise a complementary output driver and are always biased slightly on by diodes NCR1 and NCR2.

The quiescent current in the output driver is nominally 6.5 ma and the maximum signal amplitude for the circuit is ±5v.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

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Figure 7-36. Bipolar Current Buffer - SAA

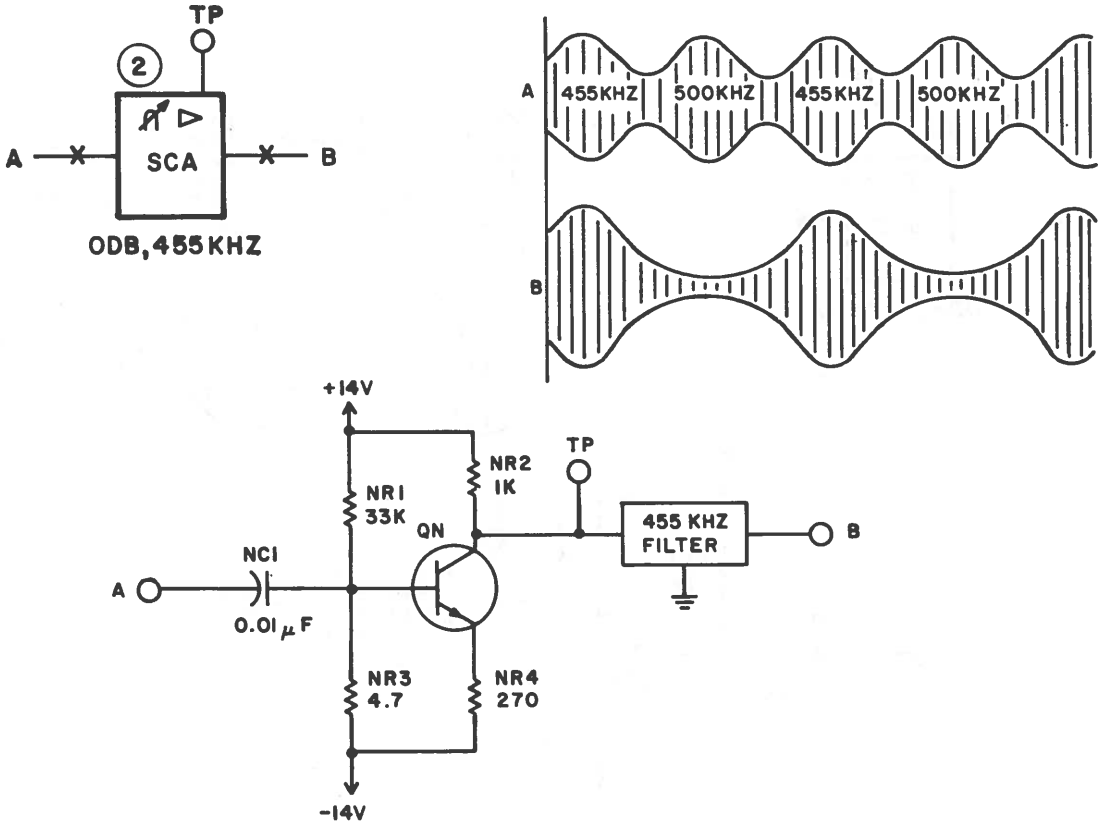


Figure 7-37. Filter - SCA

Filter - SCA

The SCA circuit (Figure 7-37) amplifies and passes the 455 kHz component of the track servo signal, and blocks passage of the other signal component (500 kHz). The circuit consists of a transistor voltage amplifier with a gain of 4.4 db and a ceramic, ladder-bandpass filter with an insertion loss of 4 db (max). As a result the signal incurs no voltage loss in the circuit.

The bandwidth at the -1 db point (relative to the center frequency attenuation) is 20kHz minimum, at -2 db it is 30 kHz minimum, at -6 db it is 40 kHz minimum, and at -60 db it is 72 kHz maximum.

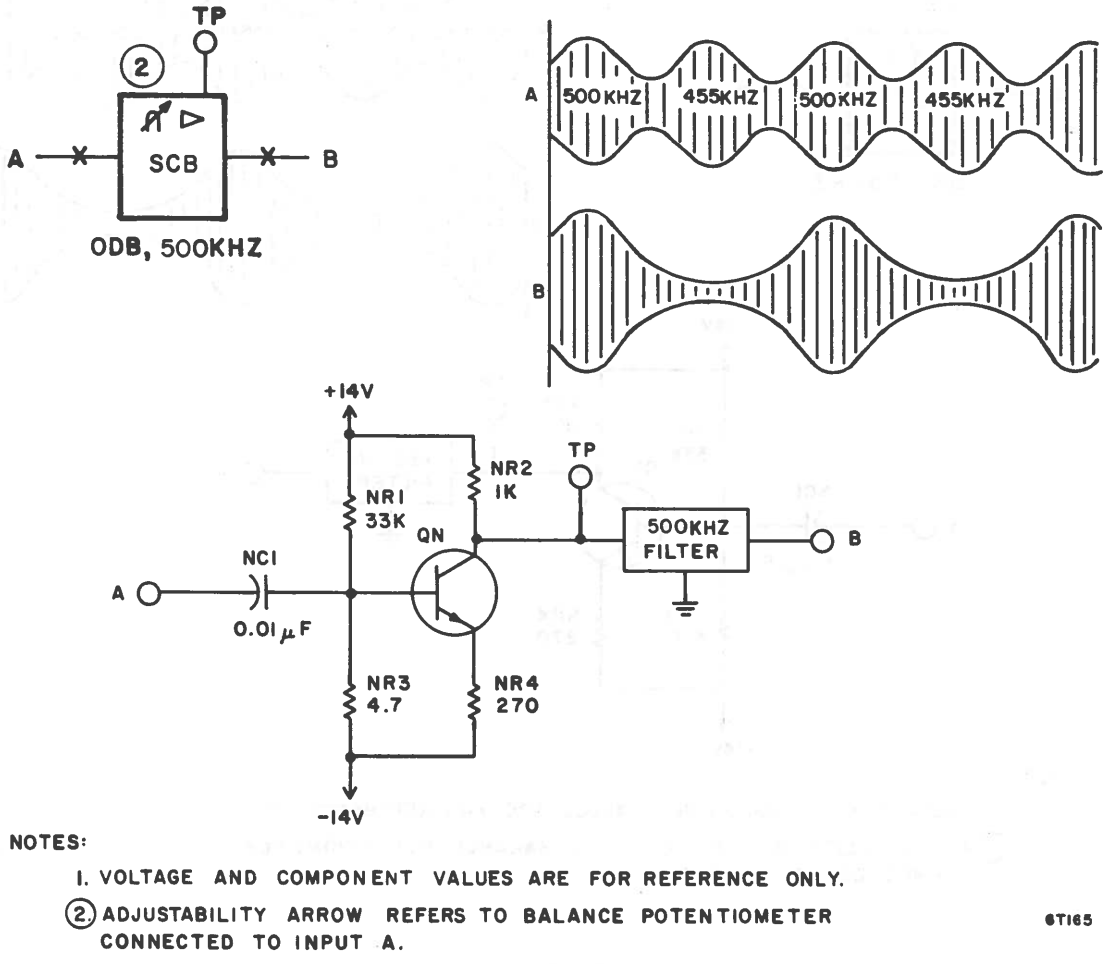


Figure 7-38. Filter - SCB

Filter - SCB

The SCB circuit (Figure 7-38) is identical to the SCA circuit except that it passes the 500 kHz component of the track servo signal and blocks the 455 kHz component.

Delay - UBD

The UBD capacitive delay circuit (Figure 7-39) delays a "1" input at A for 200 nsec before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor and a capacitor connected to ground.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If a "1" (+3.0v) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

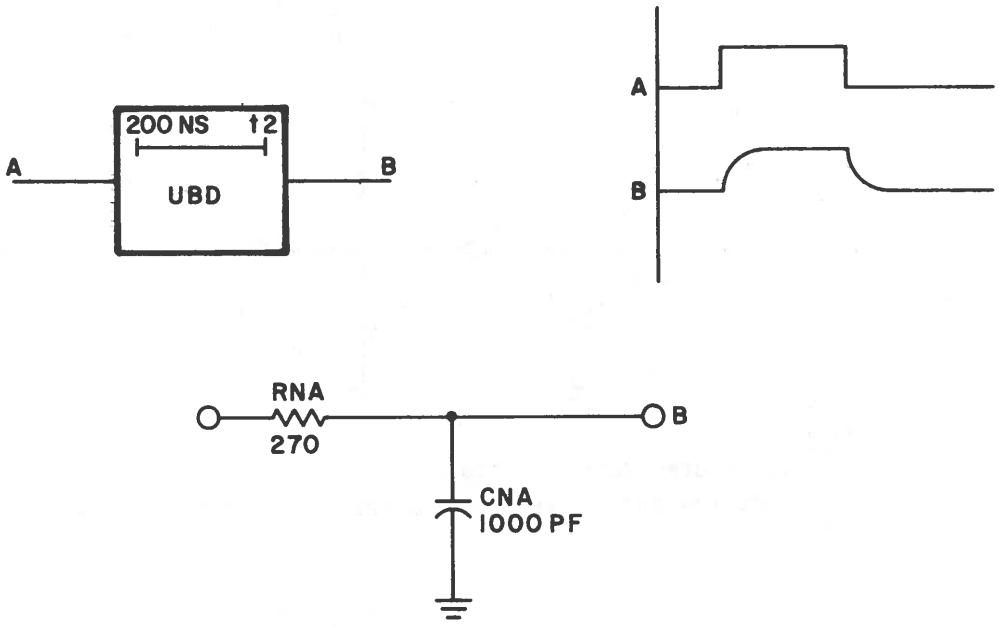


Figure 7-39. Delay - UBD

Delay - UC-

The UC- delay circuit (Figure 7-40) is used to delay open-collector integrated circuits. The circuit operates in the sam manner as the UBD delay circuit. Characteristics of the UC- circuits are as follows:

Circuit type	Capacitance	Delay
UCF	1500 pf	350 ns
UCG	3900 pf	1.0 μsec
UCH	390 pf	100 ns

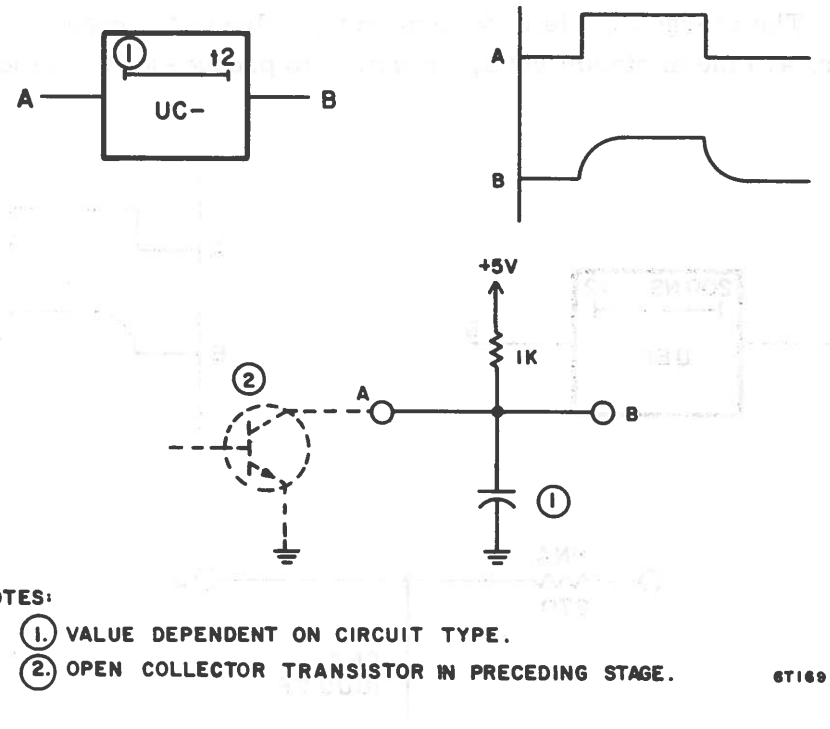


Figure 7-40. Delay - UC-

Unidirectional Time Delay - UEA

The UEA circuit (Figure 7-40.1) provides a 0.1-μsec delay between the time that a -3.5v signal appears at A and the time that transistor QP turns off. Output at B is either ground or an open circuit.

When input A is near ground, QN is off. Transistor QP is on. The output is ground.

When input A goes to -3.5v, capacitor CNA begins charging. After 0.1 μsec the base of QN is sufficiently negative to turn QN on. Transistor QP turns off. The output is an open circuit.

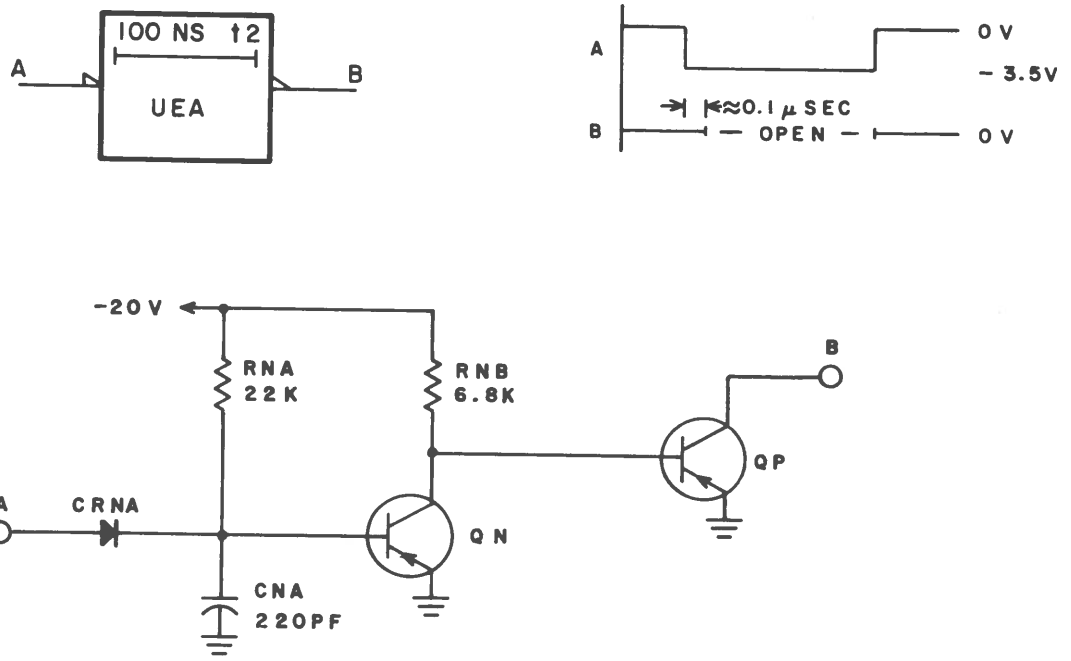


Figure 7-40.1. Unidirectional Time Delay - UEA

And - VAB

The VAB circuit (Figure 7-41) consists of two silicon peripheral logic inverters whose outputs share a common load resistor, RNE. When both inputs A and B are "0" (ground), the output at C will be a "1" (+3v). If either or both of the inputs are a "1", the output at C will be a "0". This is an AND gate for zeroes, or a NAND function.

When both A and B are at ground, QN and QP are off. The output at C is supplied from the +20v source through RNE. The output is a positive voltage, representing a non-logical 1. If input A experiences a positive voltage while B is at ground, QP turns on and conducts current from the +20v supply through RNE to ground. The "0" on B has no effect, as all the supply voltage is tapped to ground. The output at C is ground, or a "0". The situation is similar if A is "0" and B is "1". The output is "0". If both A and B have positive voltage applied to them, QN and QP both conduct. The output is "0".

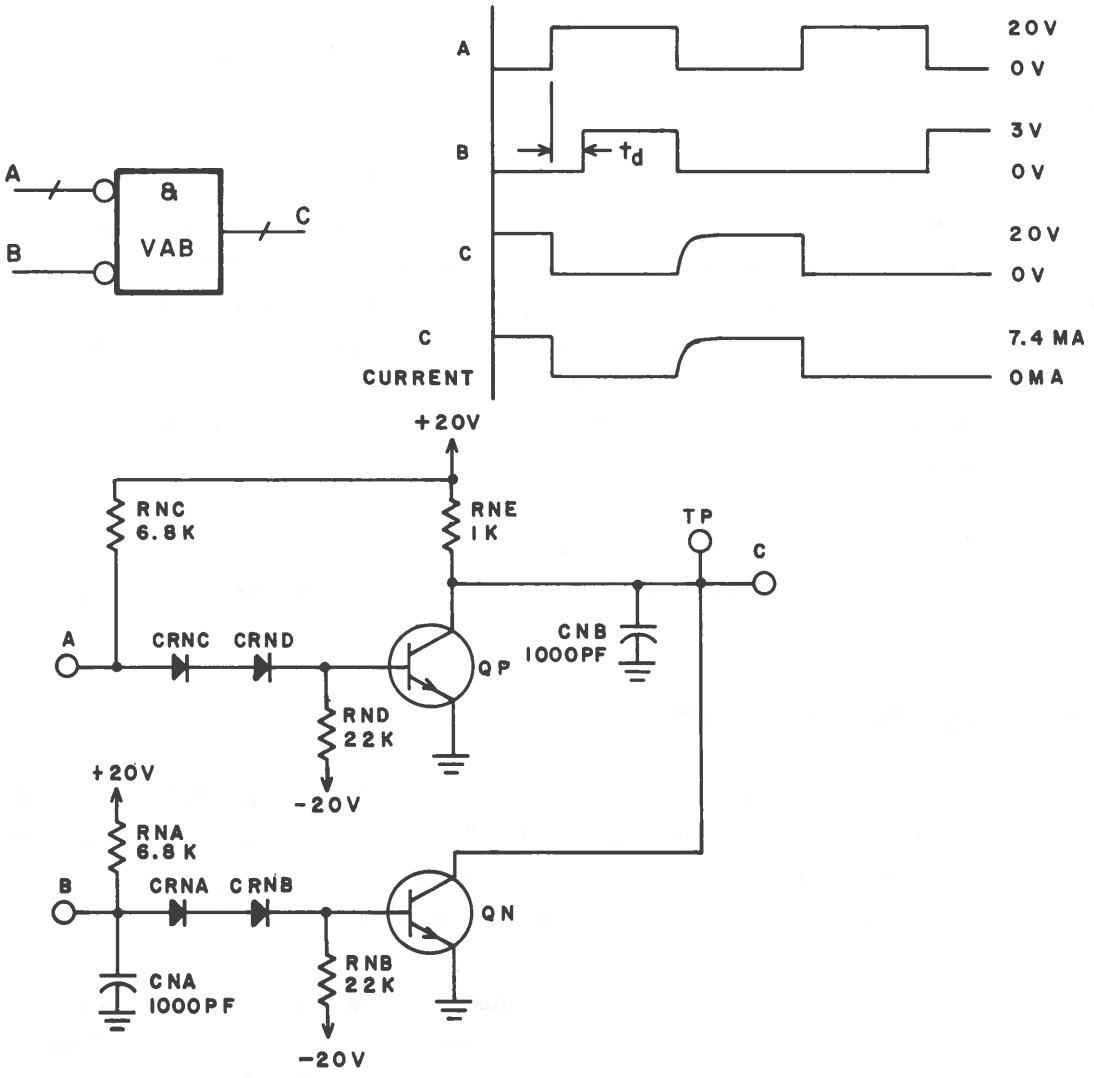
Capacitors CNA and CNB provide a one's delay on input B and output C, respectively. They also maintain a noise barrier to isolate the circuit from stray pulses on the lines.

And/Or (Single Input) - VAC, VJW

The single input AND/OR or silicon peripheral logic (SPL) inverter (Figure 7-42) provides an inversion from input A to output B: "1" on A produces a "0" on B, or a "0" on A produces a "1" on B. The inverter's output may be connected to the output of other inverters to form NAND functions or NOR functions.

The SPL inverter is a single NPN silicon transistor connected as a common emitter amplifier. When A is a "0" (between 0v and +0.3v), the transistor is off. This allows current to flow from the +20v supply, through RNB to output B. The output is a "1". When input A is a "1" (between +0.7v and +3.0v), the transistor turns on. The transistor conducts current from the +20v source, through RNB to ground. This leaves output B near ground, or a "0".

Since the base-emitter threshold for a silicon transistor is approximately +0.7v, the circuit ignores up to 0.5v of transient noise.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

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Figure 7-41. And - VAB

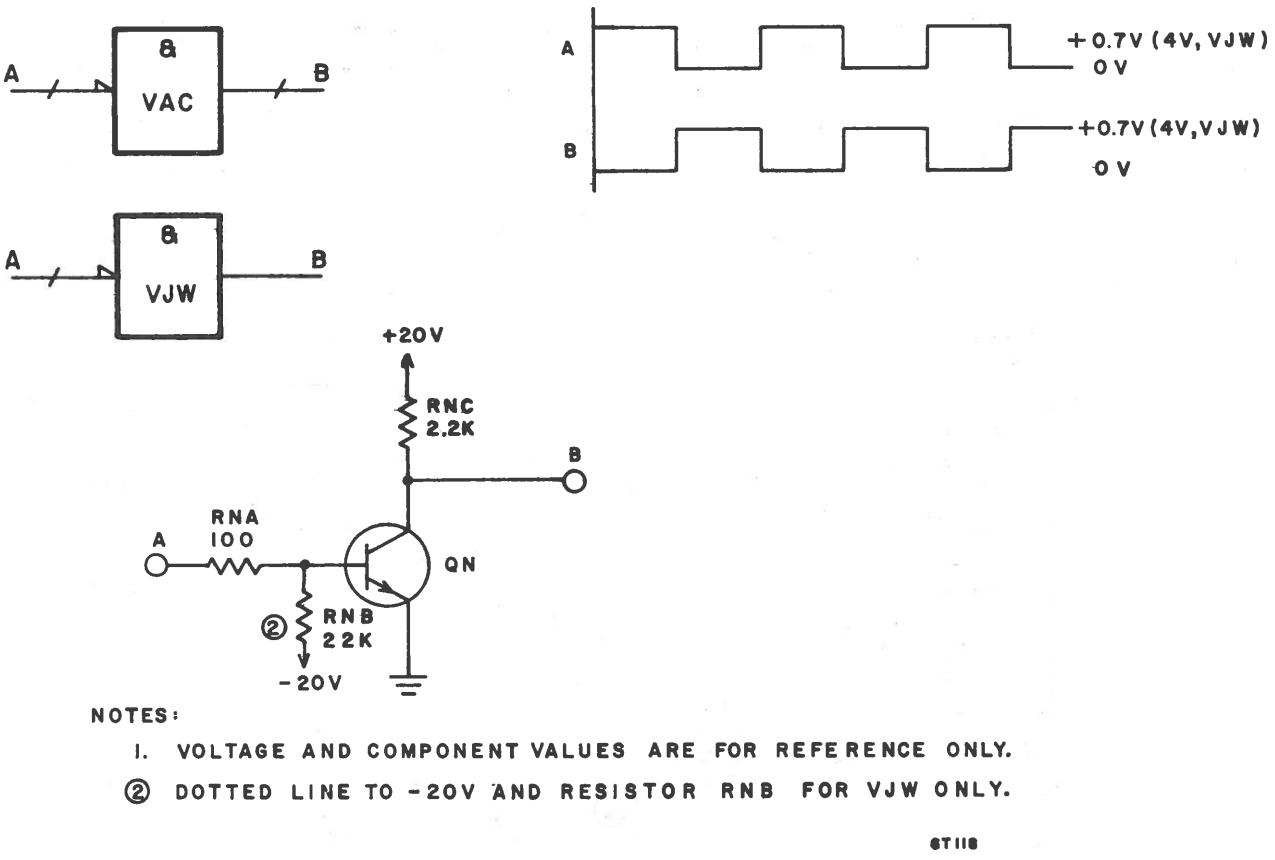


Figure 7-42. And/Or (Single Input) - VAC, VJW

If the circuit drives just one other transistor, the output may be connected directly to the base of the driven transistor. For a fin-out of 2 or more, a base isolation resistor is required for each driven transistor. This resistor ensures that the base drive provided to each of the driven transistors will be nearly independent of differences in base-emitter voltages. For a fan-out of 2, the collector load resistor must be reduced by one-half its value for driving one transistor to provide for the additional voltage drop across the isolation resistors.

Switching time for an inverter with a fan-out of 1 is typically 15 nsec.

Power Driver - VJK

The VJK circuit (Figure 7-43) is similar to the VJS circuit with the addition of capacitor CNB and two outputs. CNB slows the switching time of QN and provides a ramp output. Output B connects to the center tap of the head. Output C contains a 10K resistor and is connected to a voltage supply in a fault detect circuit. If two heads are selected the effective resistance falls to 5K (two 10K resistors in parallel). The increase in current causes a Fault signal. Output D contains a diode that isolates each Write Gate.

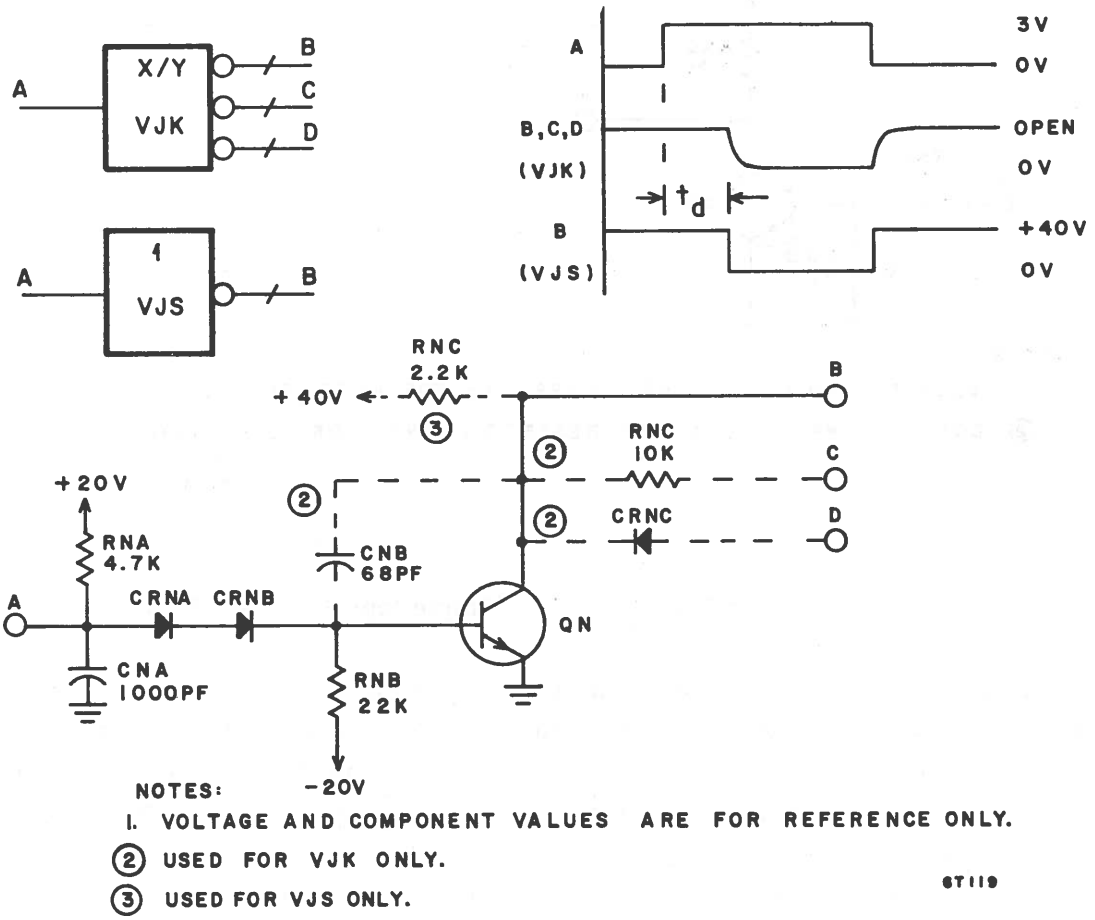


Figure 7-43. Power Driver - VJK, VJS

Power Driver - VJL

The VJL circuit (Figure 7-44) is a gate used to bias an analog gate.

If +20v appears at A, QN turns on. The base of QP goes to ground. Transistor QP is off. Capacitor CNA charges through RND to +20v. Output at B is a ramp to +20v.

A +0.2v signal at A turns QN off. When QP turns on, the collector voltage of QN clamps at +0.7v. CNA discharges rapidly through QP. Output B drops to ground.

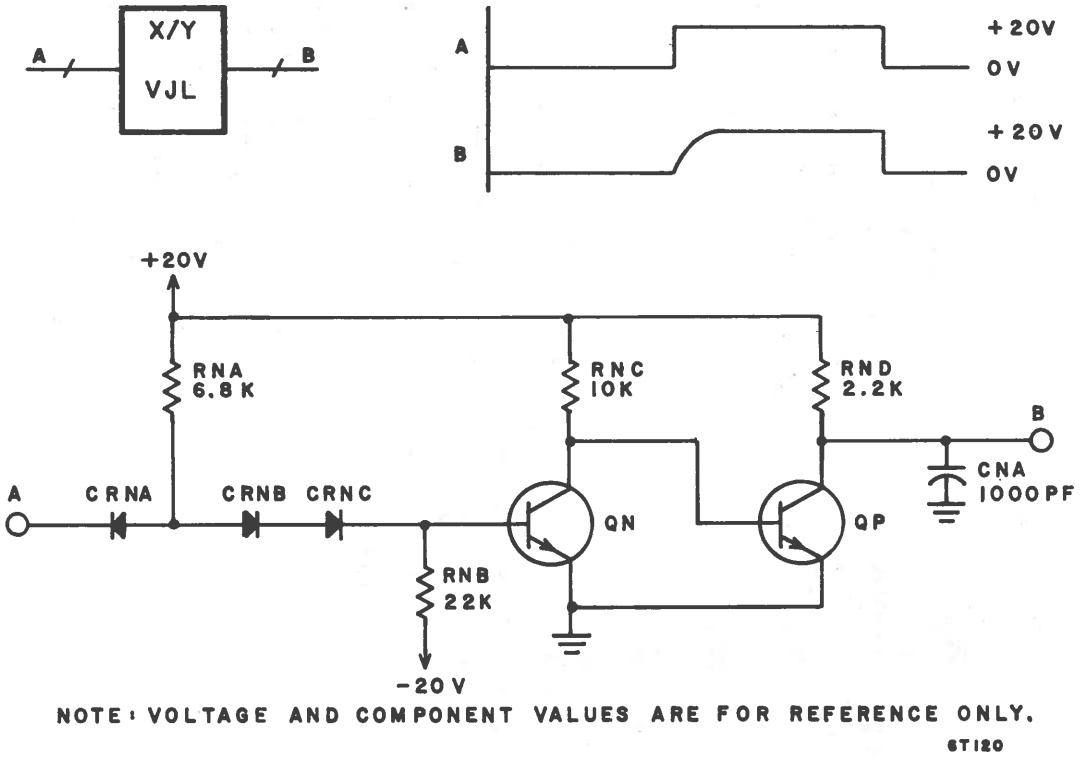


Figure 7-44. Power Driver - VJL

And - VJM

The VJM circuit (Figure 7-45) gates a particular receiver into operation. A "0" input at A results in an "open" enable signal to the receiver. A "1" input at A disables the receiver.

A "0" (0v) input forward biases diode CRNA. The +20v supply current is drawn through RNA and CRNA, leaving the base of QN reverse biases. Transistor QN if off. Output is held at -0.7v by the next stage.

A "1" input turns QN on. The output goes to ground. No receiver signal can pass into the receiver.

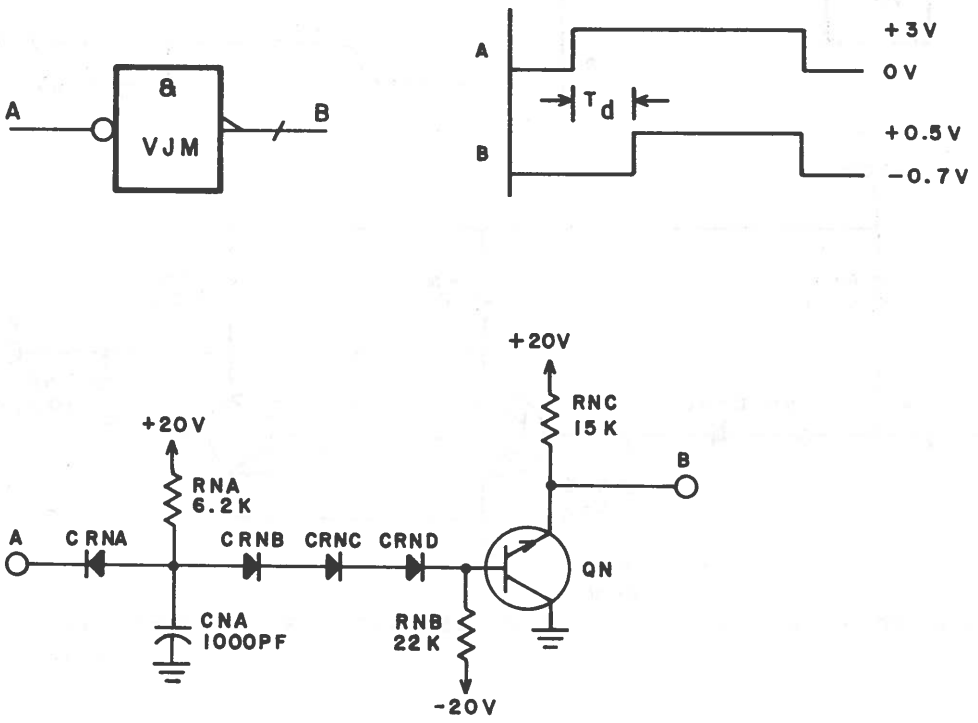


Figure 7-45. And - VJM

Or - VJN

The VJN circuit (Figure 7-46) is a NAND circuit that inverts the input signal. Input A is connected to the output of a receiver and to a gating circuit. If the Write gate is off, the base of QN is grounded. The circuit is disabled.

When the write gate is on, QN turns on and the receiver inputs a "0". Transistor QN turns on further and goes into saturation. Output voltage at B is approximately -0.2v.

When the receiver inputs a "1", QN comes out of saturation. Output at B is approximately -3.5v.

Whenever the write gate is on, QN is on to some degree. Only when the write gate is off is the base of QN at ground and QN off.

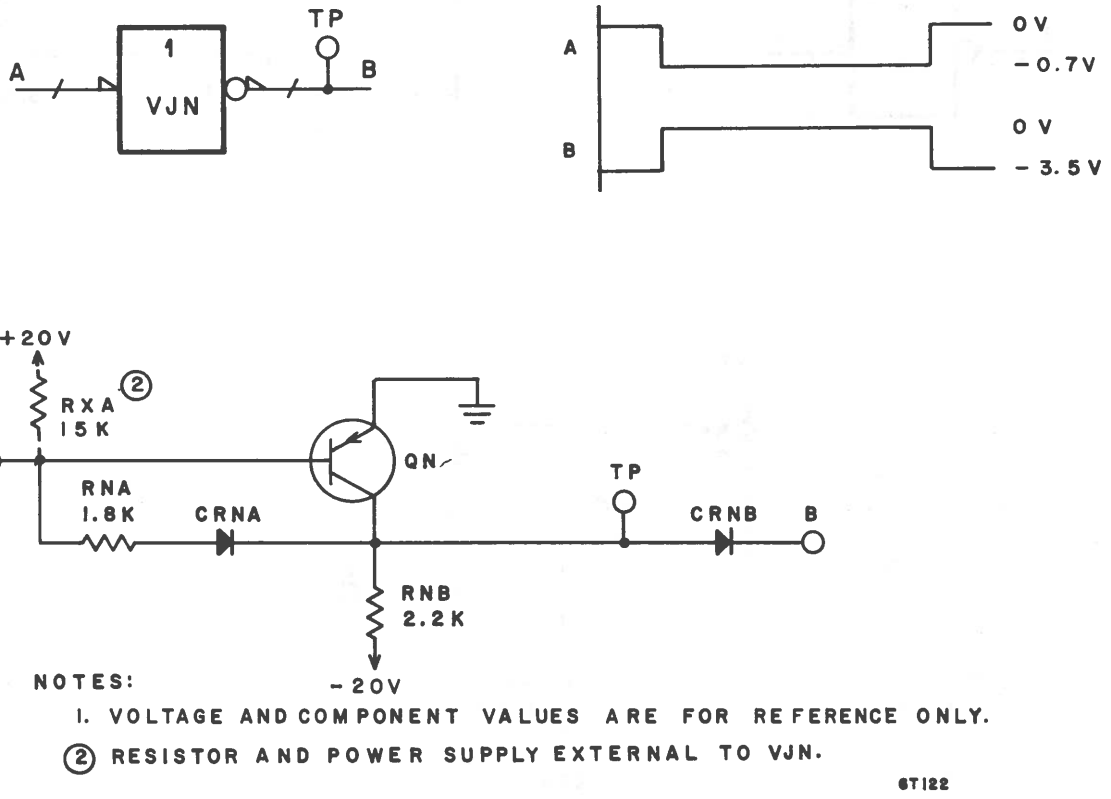


Figure 7-46. Or- VJN

And - VJP

The VJP circuit (Figure 7-47) is normally used as the input circuit to a toggle flip-flop. It ties two receiver outputs to a single-ended output. Capacitor CNA is used to reduce the input impedance for faster switching.

When input A is near ground, the base of QN is at approximately +0.9v. Transistor QN is off. Output at B approaches -20v, but is clamped at -3.8v by a Zener diode in the following circuit.

When input A is -3.5v, QN turns on. Output drops to approximately -0.2v.

Input to A is short (100 nsec), negative, data pulses. Output B is also short pulses.

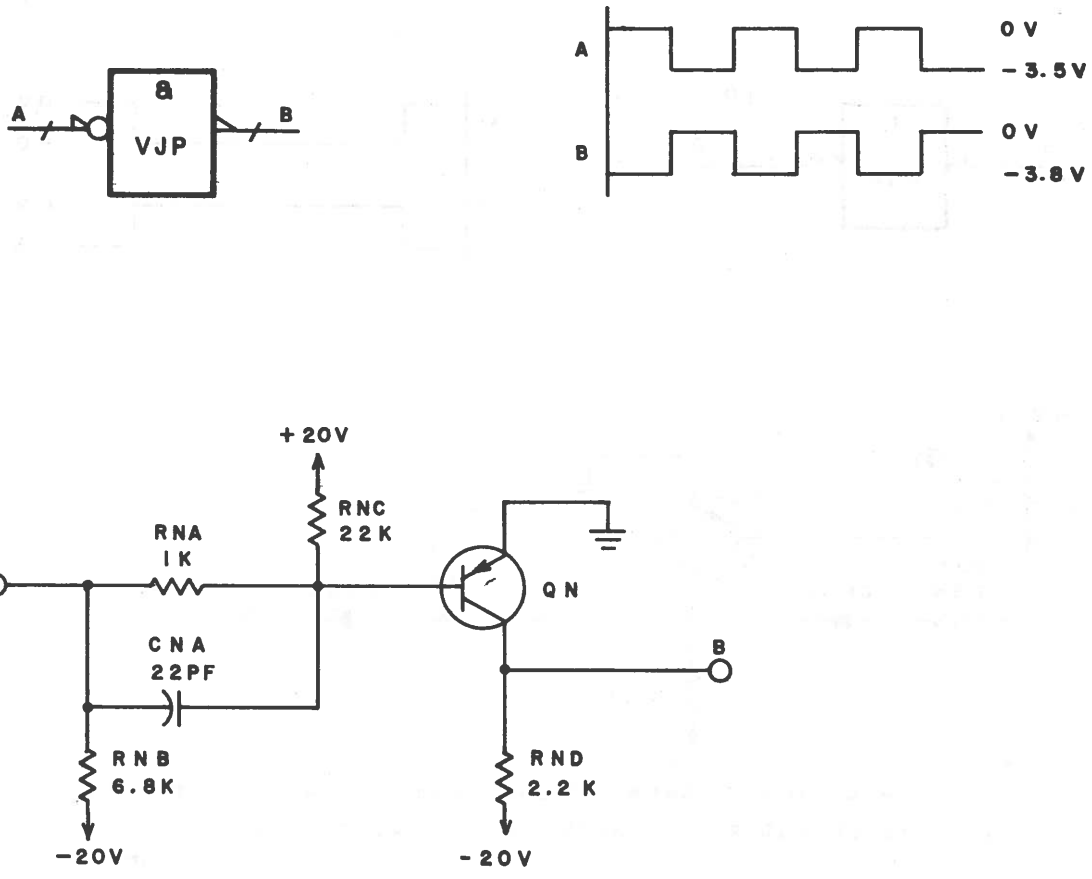


Figure 7-47. And - VJP

Power Driver - VJR

The VJR circuit (Figure 7-48) is a +40v switch. A "1" on input A produces +40v at output B. A "0" on input A stops current flow.

A "1" input turns QN on. Transistor QN conducts current from the +40v supply, causing a voltage drop across resistor RNB. This voltage drop turns on QP. Output B is at +40v.

A "0" input turns QN off. Since current no longer flows, the emitter and base of QP are at equal voltage. Transistor QP is off. Output B goes to ground.

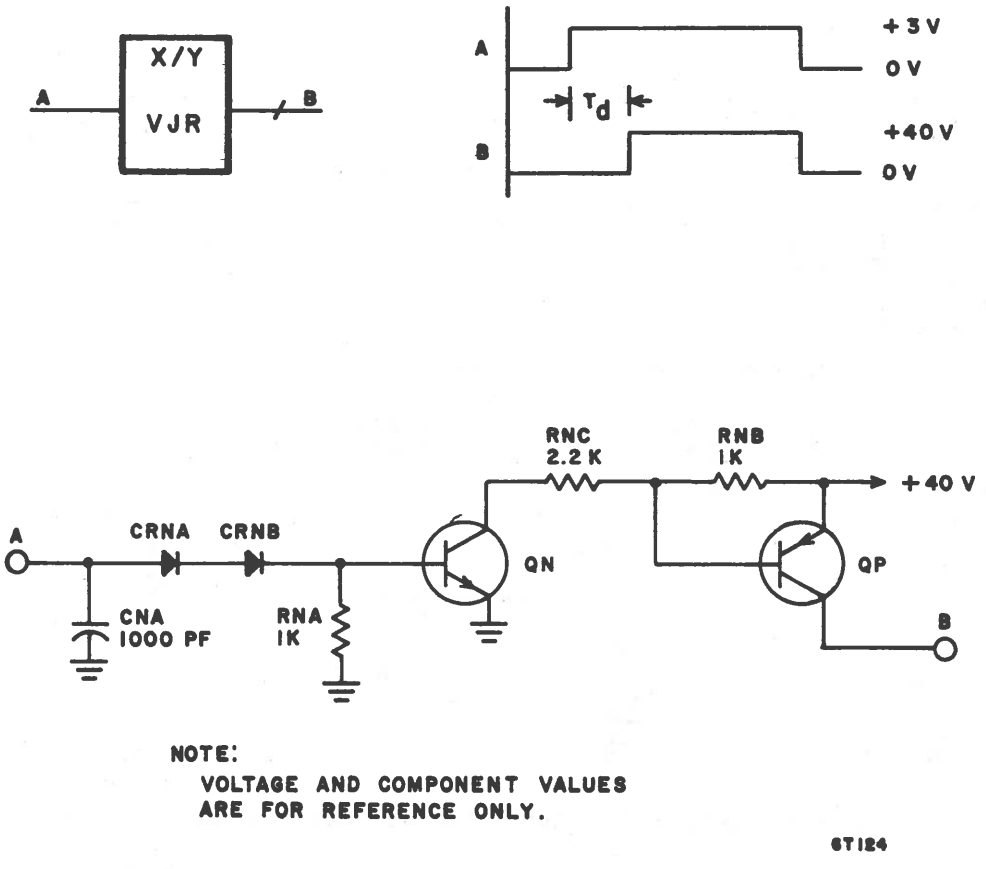


Figure 7-48. Power Driver - VJR

Or - VJS

The VJS circuit (Figure 7-43) is a standard inverter with a capacitor delay at the input. A "1" at input A pulls the output at B to ground. A "0" produces a +40v output.

Or - VJT

The VJT Circuit (Figure 7-49) is a gate to the WBB toggle flip-flop. A "1" input at A produces a ground at B, which keeps the flip-flop off. A "0" input at A produces a -3.5v output at B, which releases the flip-flop and presets it in a given state.

When a "0" is applied to input A, the base of QN goes to ground. Transistor QN is off. The base of QP is clamped at +0.6v by diode CRNC. Transistor QP is off. Output B is -3.5v derived from the voltage dividing network of RNF and RNG.

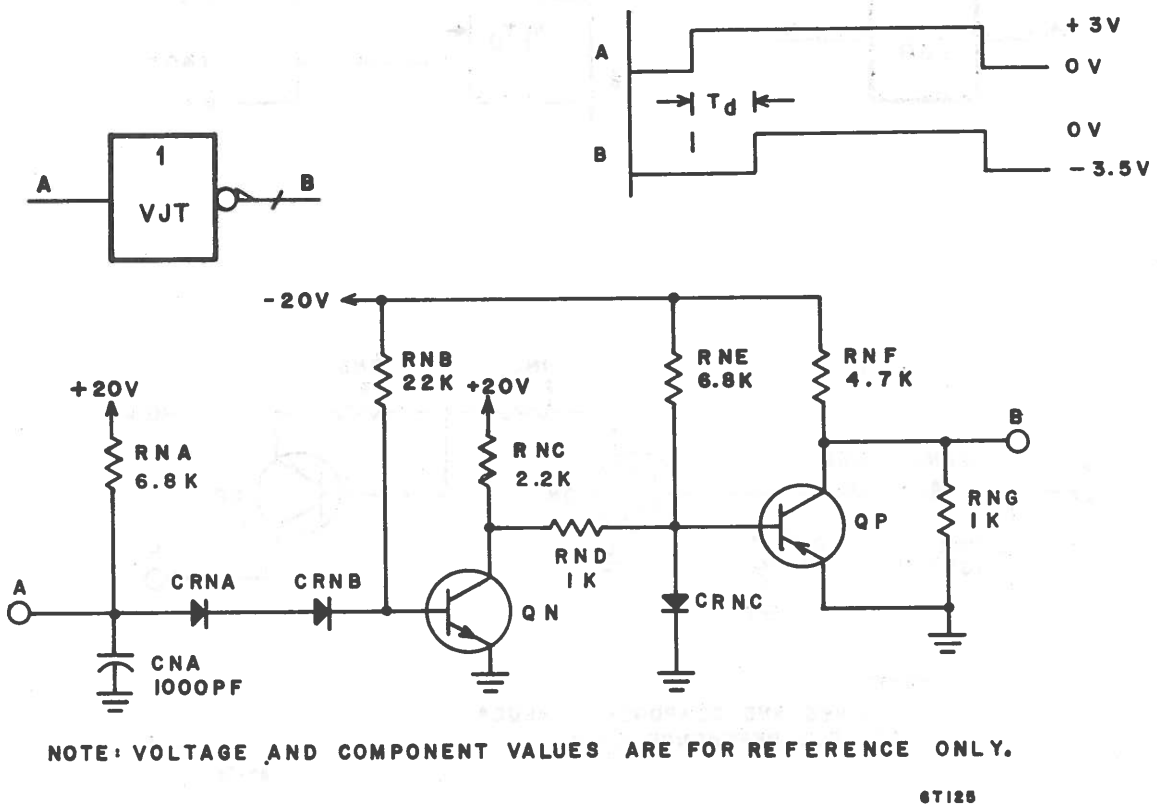


Figure 7-49. Or - VJT

When A goes to a "1", capacitor CNA charges. After a delay, the base of QN is positive enough to turn QN on. The base of QP goes negative through resistor RNE. Transistor QP turns on. The output at B drops to ground.

And - VJU, VJV

The VJU and VJV circuits (Figure 7-50) are functionally identical. They consist of a standard inverter circuit with a capacitive filter input. The capacitor also presents a delay.

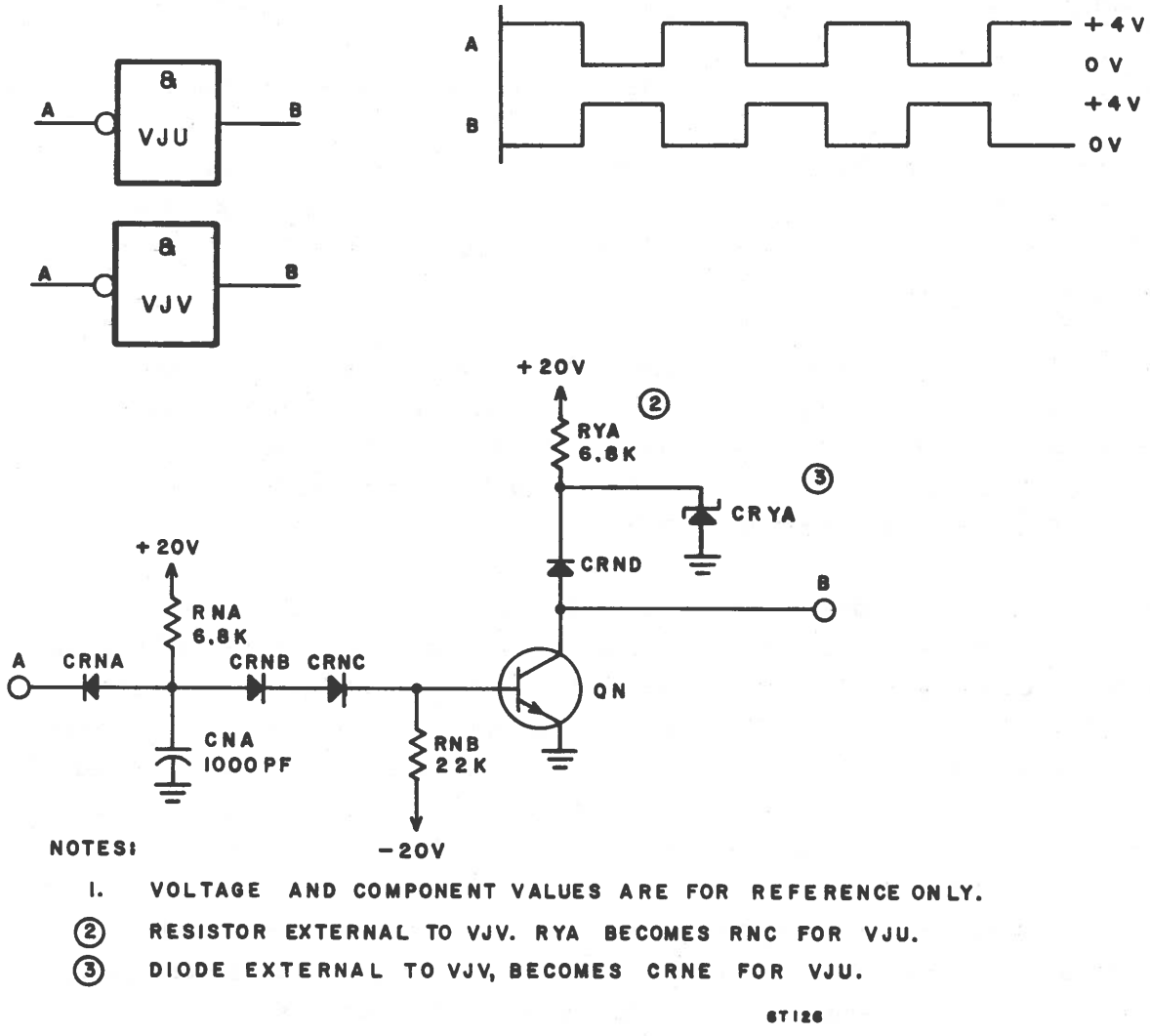


Figure 7-50. And - VJU, VJV

A "1" on input A reverse biases diode CRNA. Capacitor CNA charges through RNA until it is clamped at about 3 diode voltages (approximately 2.1v). QN turns on. Output B falls to ground.

If input A is a "0", CNA discharges through CRNA. Transistor QN turns off. Output B rises to a "1" level due to the clamping by a Zener diode.

And/Or - VJW

Refer to circuit description for circuit type VAC.

Flip-Flop WBB

The WBB circuit (Figure 7-51) is a toggle flip-flop with gate and data inputs.

Input B holds both transistors off by grounding the bases when the circuit is off. When a write operation is to be performed, the base of QP is released while QN is still grounded by input C. This sets an initial condition for the flip-flop: QP is on, QN is off.

After the flip-flop is pre-set, it is toggled through input A by a series of negative data pulses. The leading edge of the negative data pulse begins charging capacitor CNB. Diode CRND becomes forward biased. QP is on. Output E is at ground. A voltage of -3.6v across Zener diode CRNK keeps CRNN reverse biased. CRNK and CRNM clamp the output of QN at -3.8v.

The trailing edge of the data pulse results in a positive pulse to the base of QP. Transistor QP turns off. Output E goes toward -4v. Both sides of CNA are at ground. Therefore, CRNC anc CRNF are forward biased by the -20v source through RNC. The base of QN goes negative. Transistor QN turns on and output D drops to ground. Diodes CRNM and CRNJ are now reverse biased. Since the collector of QP is more negative than the voltage across Zener diode CRNK (-3.6v), CRNN is forward biased. This clamps the voltage at output E at approximately -3.8v.

The leading edge of the next negative pulse charges CNA and discharges CNB since both sides of CNB are at about -3.8v. The flip-flop will toggle on the ground-going edge of the pulse in the same manner as described for the first pulse.

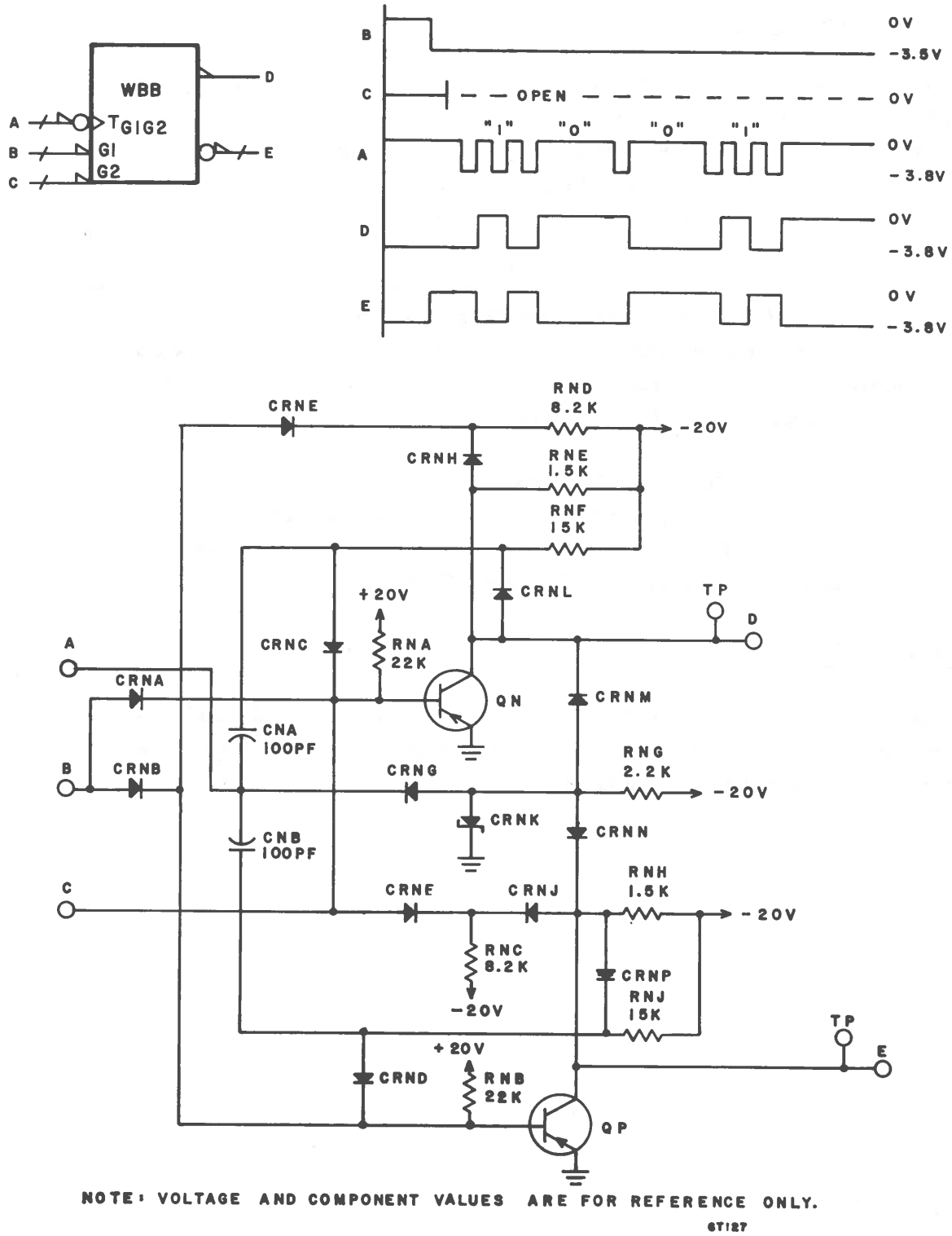


Figure 7-51. Flip-Flop - WBB

Toggle Flip-Flop - WBC

Inputs to A and B of the WBC flip-flop (Figure 7-52) are either a positive pulse or ground. If A has positive pulse, then B is at ground. If A is at ground, then B has a positive pulse. If input A receives a positive pulse, output C will be at ground and output D will be a constant positive voltage. A positive pulse at B will toggle the flip-flop. C will then be a positive voltage and D will be at ground.

A positive pulse to input A turns on transistor QN, which drives the base of QR to ground. Transistor QR is turned off. Input B is at ground and QP is off. The base of QQ is, therefore, positive and QQ turns on. This latches the base of QR at ground and puts a ground on output C. With QP off and QR latched off, current flows from the +20v source through RNB to output D.

When a positive pulse is felt at B, QP turns on. This drives the base of QQ to ground, turning QQ off. Input A is at ground and QN if off. The base of QR is, therefore, positive. Transistor QR conducts, latching the base of QQ at ground and driving output D to ground. With QN and QQ off, output C is positive.

Single Shot - XAA

The input to A and B (Figure 7-53) of the XAA circuit is a 0.7v balanced square wave centered around a positive voltage. Each time the inputs change polarity a short negative pulse is formed at output C.

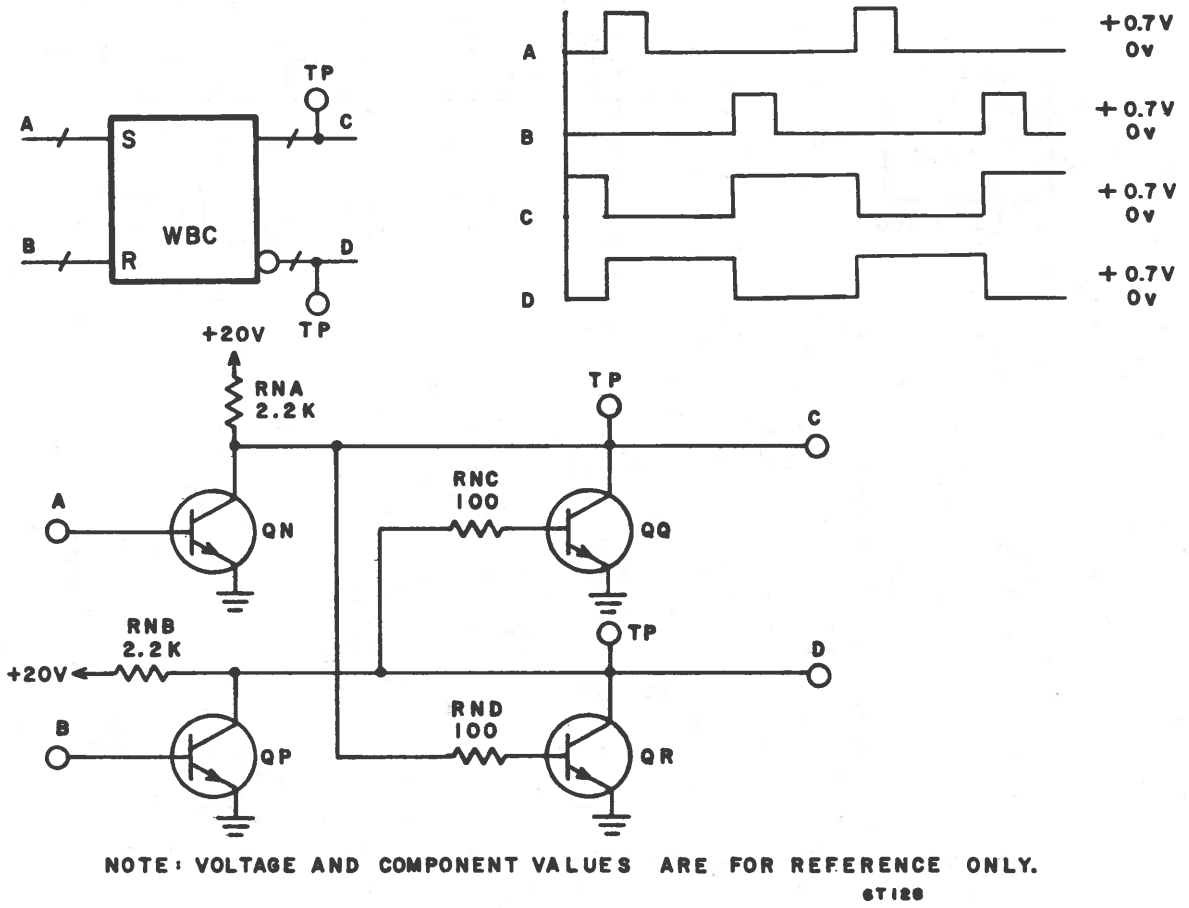
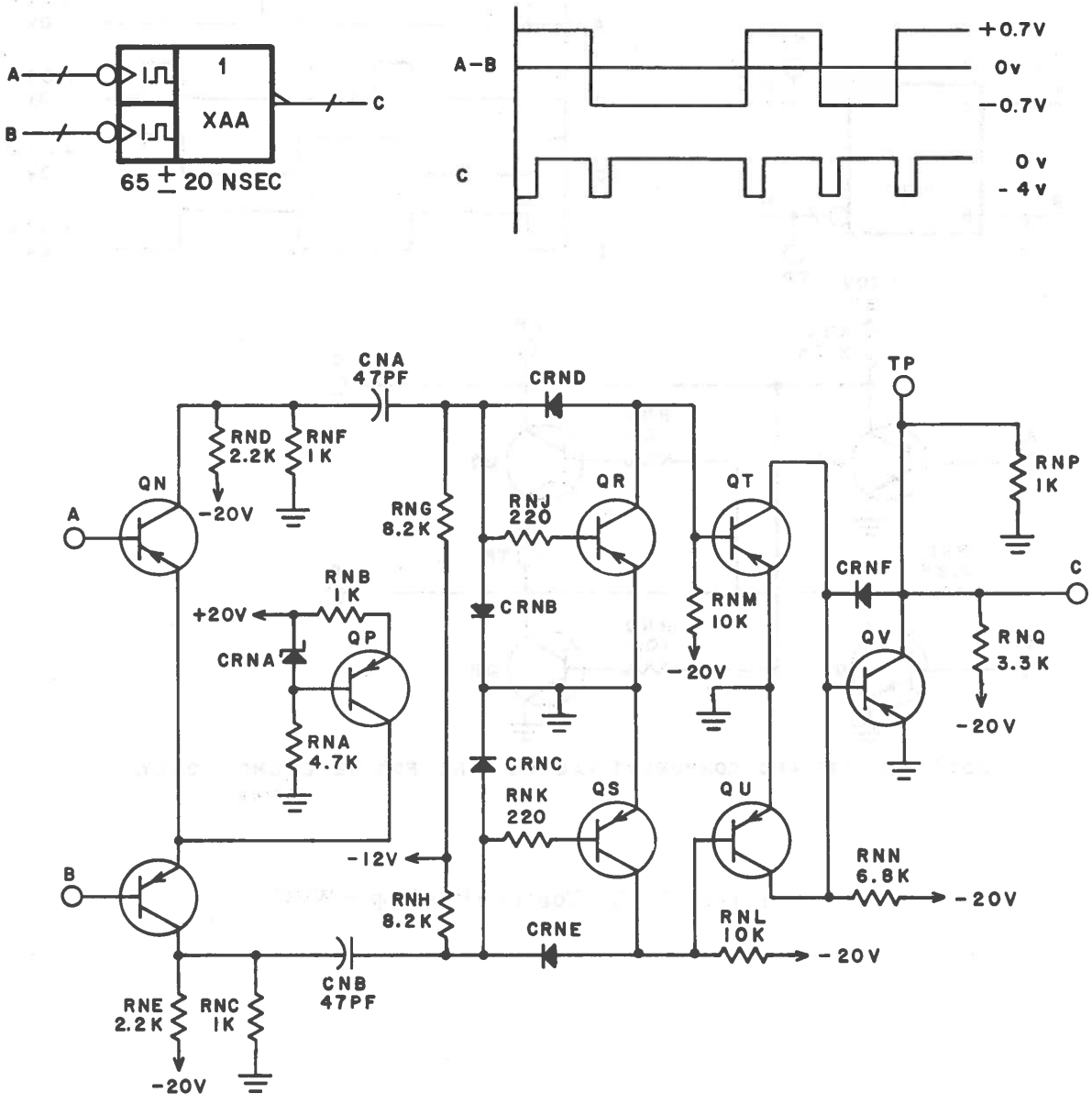


Figure 7-52. Toggle Flip-Flop - WBC



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

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Figure 7-53. Single Shot - XAA

The square wave input is sufficient to alternately turn QN and QQ on and off. A current of about 5.6 ma is alternately switched between QN and QQ. When input A is more positive than input B, QN turns off. The voltage at the collector of QN is about -20v. The voltage at the junction of RNG and RNJ is -1.6v. When the inputs switch, QN turns on. The collector of QN rises to about -8.7v. CNA forms a positive pulse to the base of QR. The positive pulse turns QR off, QT on, and QV off for the duration of the pulse. The amplitude of the pulse is limited by CRNB. Charging time for CNA is about 100 nsec. When the inputs switch again, QQ turns on and QN turns off. CNB forms a positive pulse which turns QV off again for the duration of the pulse. The output C is ground until QV is turned off. During the short time that QV is off, a negative pulse appears at output C.

Diodes CRND and CRNE prevent saturation of QR and QS. As the collectors of QR and QS approach ground, the negative voltage at the left ends of RNJ and RNK is limited to the sum of the voltage drops across QR and CRND or QS and CRNE, respectively. Diode CRNF prevents QV from saturating.

Single Shot - XAB

The input at A of the XAB circuit (Figure 7-54) is a balanced square wave between 0v and +0.75v. The output at B is normally positive, but drops to ground for a short time at the leading edge of the ground portion of the input wave.

During the positive portion of the input wave, transistors QN and QP are on. This leaves the bases of QQ and QR near ground. Transistors QQ and QR are off. The output at B is a positive voltage supplied through resistor RNE.

When the input wave goes to ground, transistors QN and QP turn off. With QP off, the base-emitter junction of QR is forward biased. Transistor QR conducts and the output at B drops to near ground. With QN off, capacitor CNA charges toward +20v. When the charge on CNA reaches a level sufficient to turn on QQ, the base of QR again drops to ground. Transistor QR turns off. The output at B returns to the positive level.

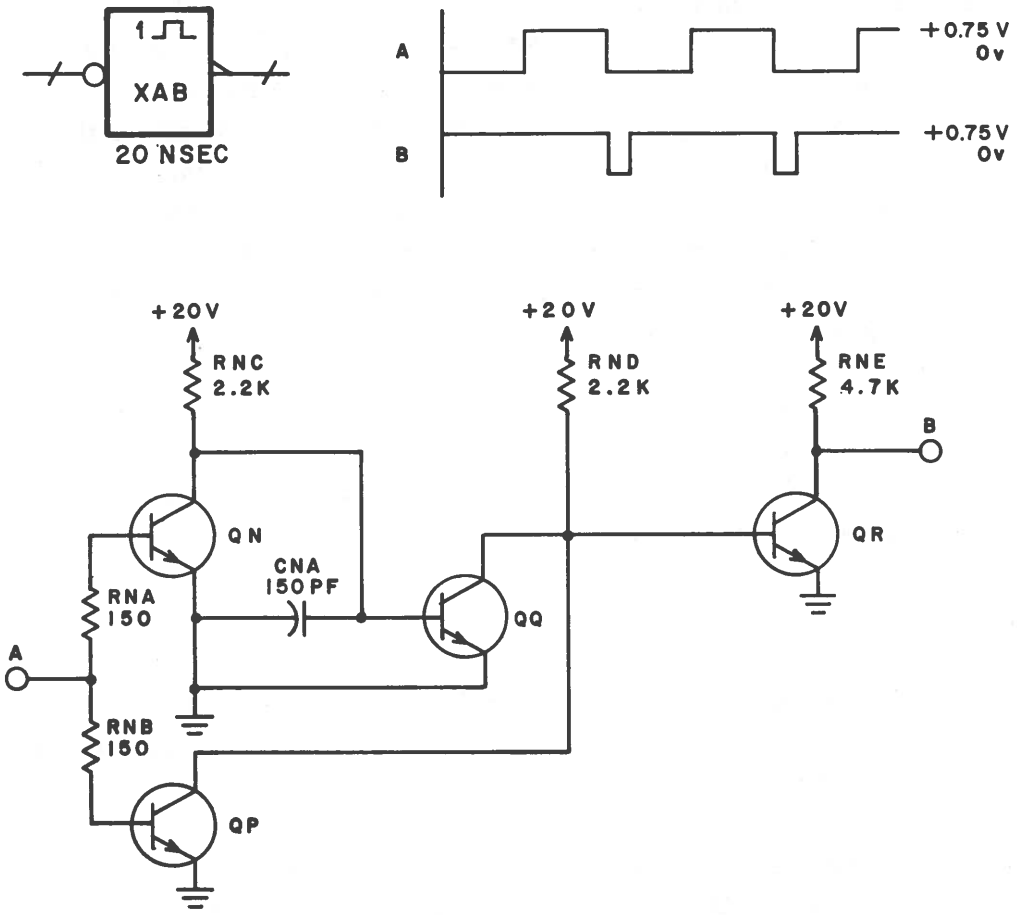


Figure 7-54. Single Shot XAB

Gated Single Shot - XAC

The XAC circuit (Figure 7-55) produces a 100-nsec ground pulse at output C when the inputs at A and B charge state. The output is normally positive. Input A is connected to the set side of a flip-flop and input B is connected to the clear side.

When the flip-flop is clear, the base of QR is positive. Transistor QR conducts 10ma of current from the -20v supply through RND, RNC, QS, QR, and RNB. The collector of QN is at -20v and the collector of QR is near +13v. Transistors QT and QU are on and QV and QW are off.

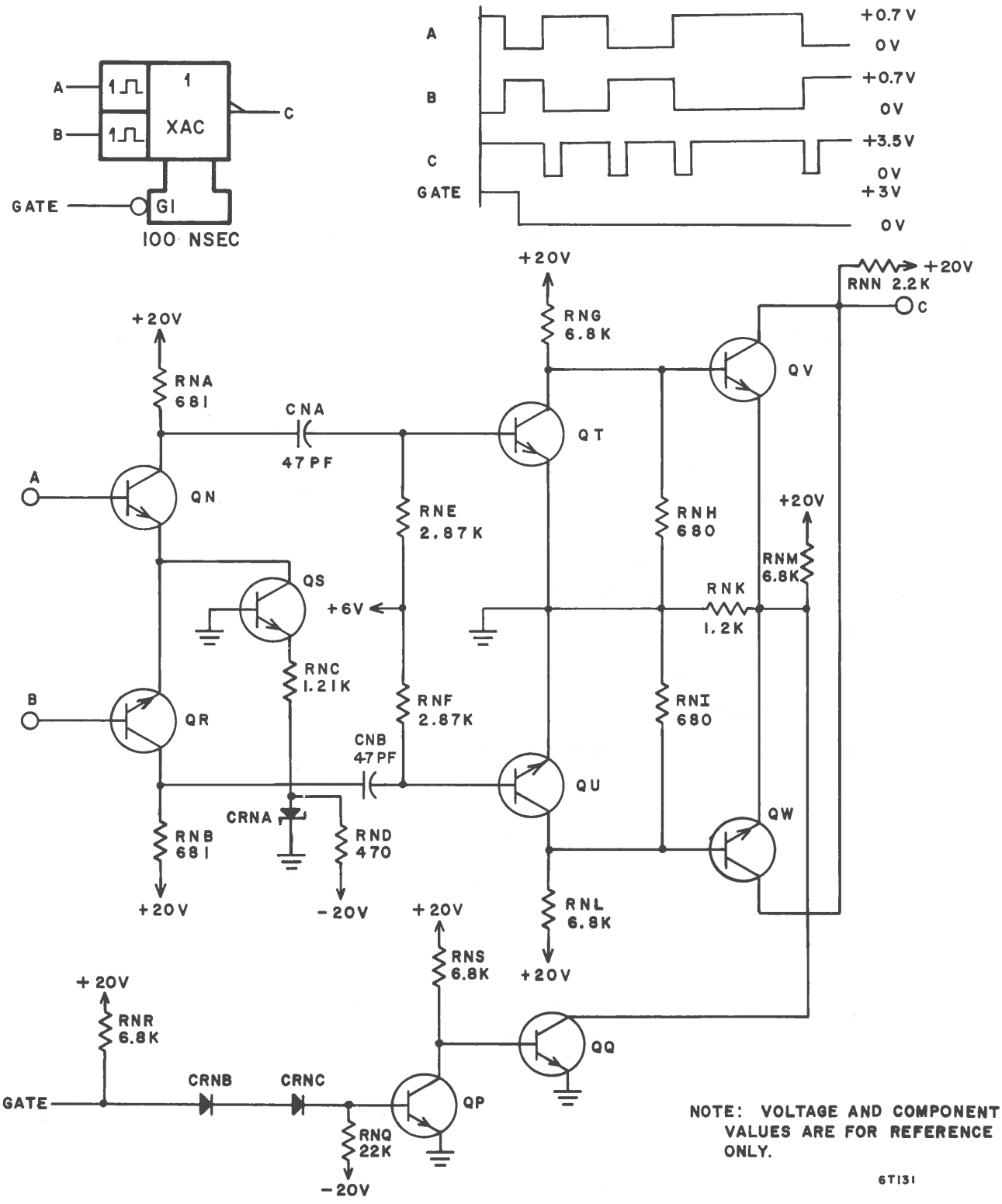


Figure 7-55. Gated Single Shot - XAC

When the flip-flop sets, QR turns off and QN turns on. The collector of QN goes to +13v, which drives the base of QT to about -6v. This turns QT off, driving the base of QV positive. QV turns on and the output at C goes to ground. Capacitor CNA charges through RNE with a time constant of 135 nsec. After 100 nsec the voltage at the base of QT has risen to +0..7v and QT turns on. This drives the base of QV to ground. QV turns off and the output at C returns to a positive level.

When the flip-flop clears again, a 100-nsec ground pulse is formed at C by QR, CNB, QU, and QW.

HEAD AND DISK PACK REPLACEMENT CRITERIA

HEAD REPLACEMENT CRITERIA

DSU heads have been designed so that they should not need replacement if given proper preventive maintenance and care. If a head requires replacement, refer to the Preface of this manual for the publication containing the Maintenance section. Refer to that section for Head/Arm Replacement procedure. A head is defective and needs replacing if any of the following conditions exist:

1. Consistent oxide buildup on head, indicating repeated head/disk impact.
2. Appreciable oxide buildup located primarily on the edge of the ferrite insert, indicating a warped head.
3. Oxide or wear over 1/2 of the head face surface.
4. A head which is scratched over 1/2 of the head face surface.
5. Concentric scratches on disk surface. Inspect the head for imbedded particles.
6. Audible ping indicating that the head is hitting the disk surface.

DISK PACK REPLACEMENT CRITERIA

The disk pack is designed to last the lifetime of the equipment: Replacement of the disk pack is required only if excessive runout (see Disk Pack Runout Check) is encountered or physical damage to the pack results in the loss of recording ability.

A disk pack is defective and needs replacement if any of the following conditions exist:

1. Damage to the disk pack resulting in a bent or broken disk. If a disk is bent, perform Disk Pack Runout Check procedure.
2. Gouged or scored disk surface causing the loss of stored data.
3. Imbedded particles in a disk surface that cannot be removed by cleaning and are causing damage to the heads.

Disk Pack Runout Check

This procedure determines whether a bent disk pack may remain in use. If the disk pack fails to meet the requirements of the porcedure, it should be returned to the manufacturer for reconditioning.

1. Open cabinet top cover.
2. Install the disk pack to be checked on a DSU spindle.
3. Grasp the pack cleaning brushes, override the shaft detent mechanism, and rotate the brushes into the disk pack.
4. Place the disk pack runout gage (Part No. 84357600) base on the DSU deck base plate (Figure 7-56) adjacent to disk cleaner cutout in shroud.
5. Turn the bezel of the dial indicator to indicate zero. Orient the dial indicator so that the plastic tip is not only contacting a disk surface but is deflected for an indication of approximately 0.020 inch. Tighten dial indicator in this position. Turn the bezel to set the dial indicator to zero.

NOTE

A mirror is required to observe dial indicator when some disk surfaces are checked.

6. Manually and slowly rotate the disk pack one full revolution while carefully observing the dial indicator. The sum of the deviations (to either side of zero should not exceed 0.012 inch.
7. If a total deflection of 0.012 inch is encountered in step 6, recheck the indication. The total deflection must occur in a disk circumference of 4 inches or more.
8. Repeat steps 5 through 7 for the 19 remaining disk surfaces.
9. Rotate the pack cleaning brushes clear of the disk surfaces.
10. Remove the disk pack and the disk pack runout gage.

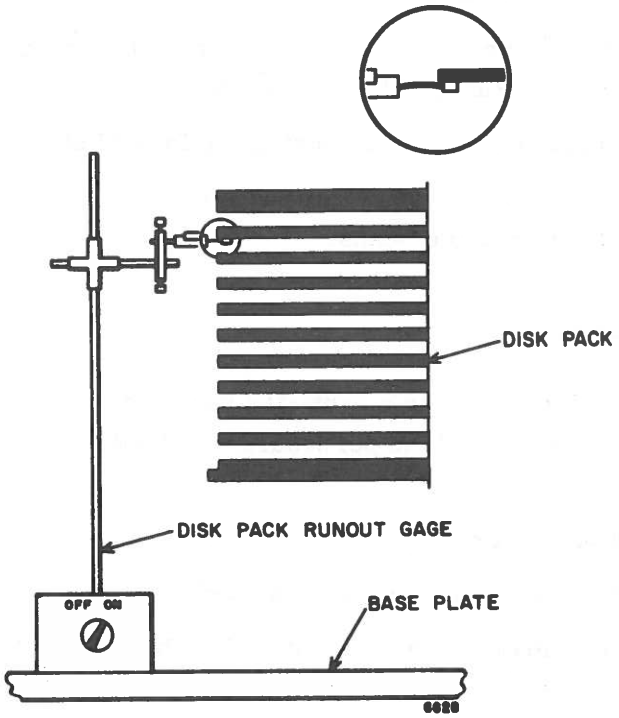


Figure 7-56. Disk Pack Runout Check

ACCESS TESTER CARD

The access tester card (P/N 54116100) is a special tool used optionally with some DSU's to perform off line maintenance procedures of Section 6. Figure 7-57 is the logic drawing for the card and is provided as an aid in using the tester. Erroneous and/or misleading positioning of the actuator will occur if the tester is not used as specified in the Operation paragraph.

OPERATION

The access tester card allows DSU positioning to be performed in one of two basic modes: repeat (continuous, alternate forward and reverse seeks between a specified pair of tracks) and incremental (sequential seeks of a specified length to the forward limit, returning to zero, and repeating). The desired mode is selected in accordance with the setting of the IN/RP (incremental/repeat) switch, S4. Operation in either mode is controlled by the R/W (run/stop) switch, S3, and the ST (start) switch, S1. A single step modification of the two basic modes may also be performed.

Repeat Mode (Figure 7-58)

To exercise a DSU in the repeat mode, perform the following procedures:

1. Set DSU logic chassis maintenance panel ON LINE/OFF LINE switch to OFF LINE and set DC switch to OFF.
2. Install access tester card in DSU logic chassis location C30.
3. Set DC switch to ON.
4. Install disk pack on DSU spindle.
5. Start spindle motor and allow brush cycle to end.
6. Press tester RT (return to zero) switch, S2. DSU should load heads and return to track 0.
7. Set tester IN/RP switch to RP position (repeat).
8. Set tester R/W switch to R position (run).

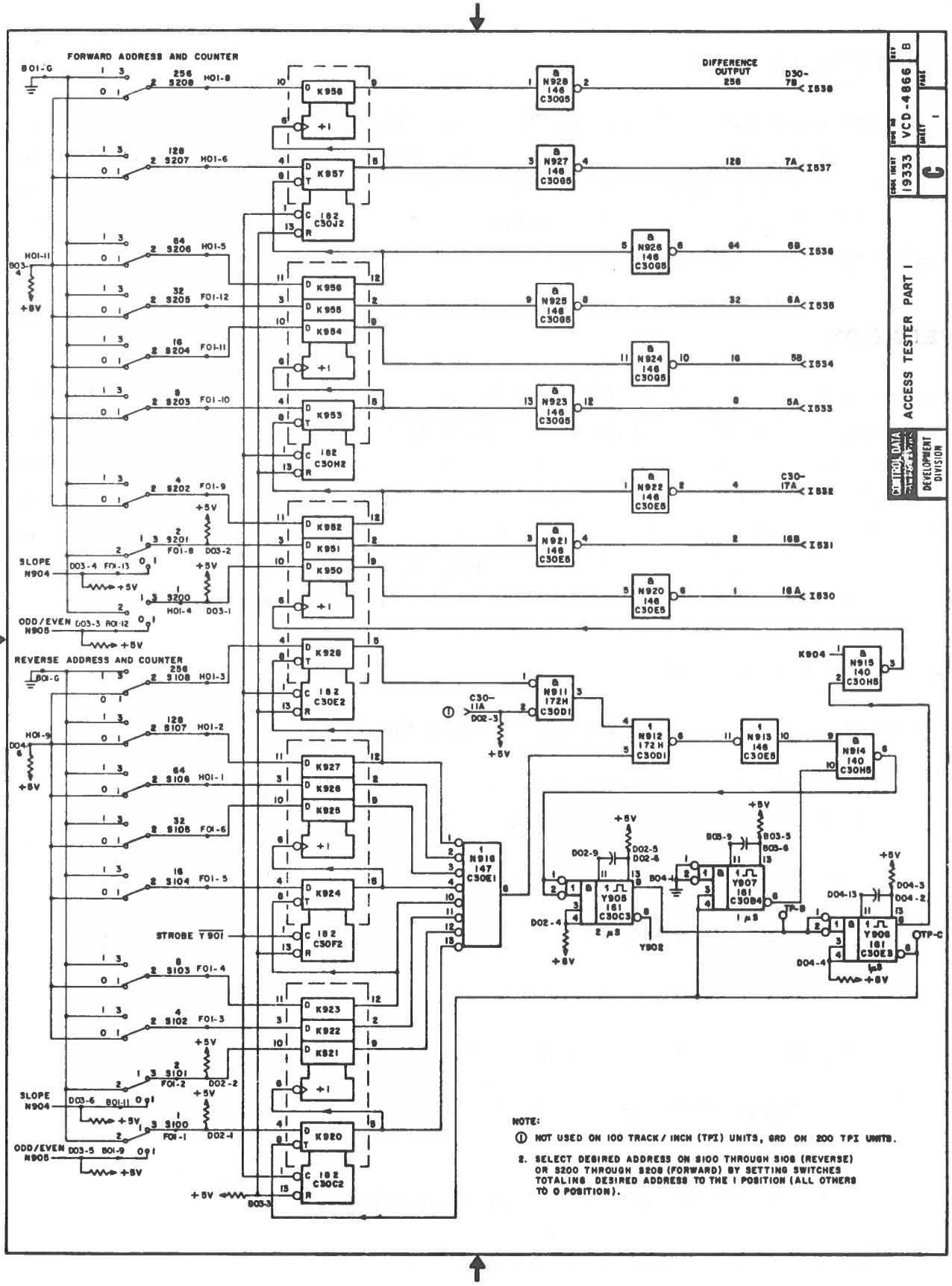


Figure 7-57. Access Tester Card Logic - Sheet 1 of 2

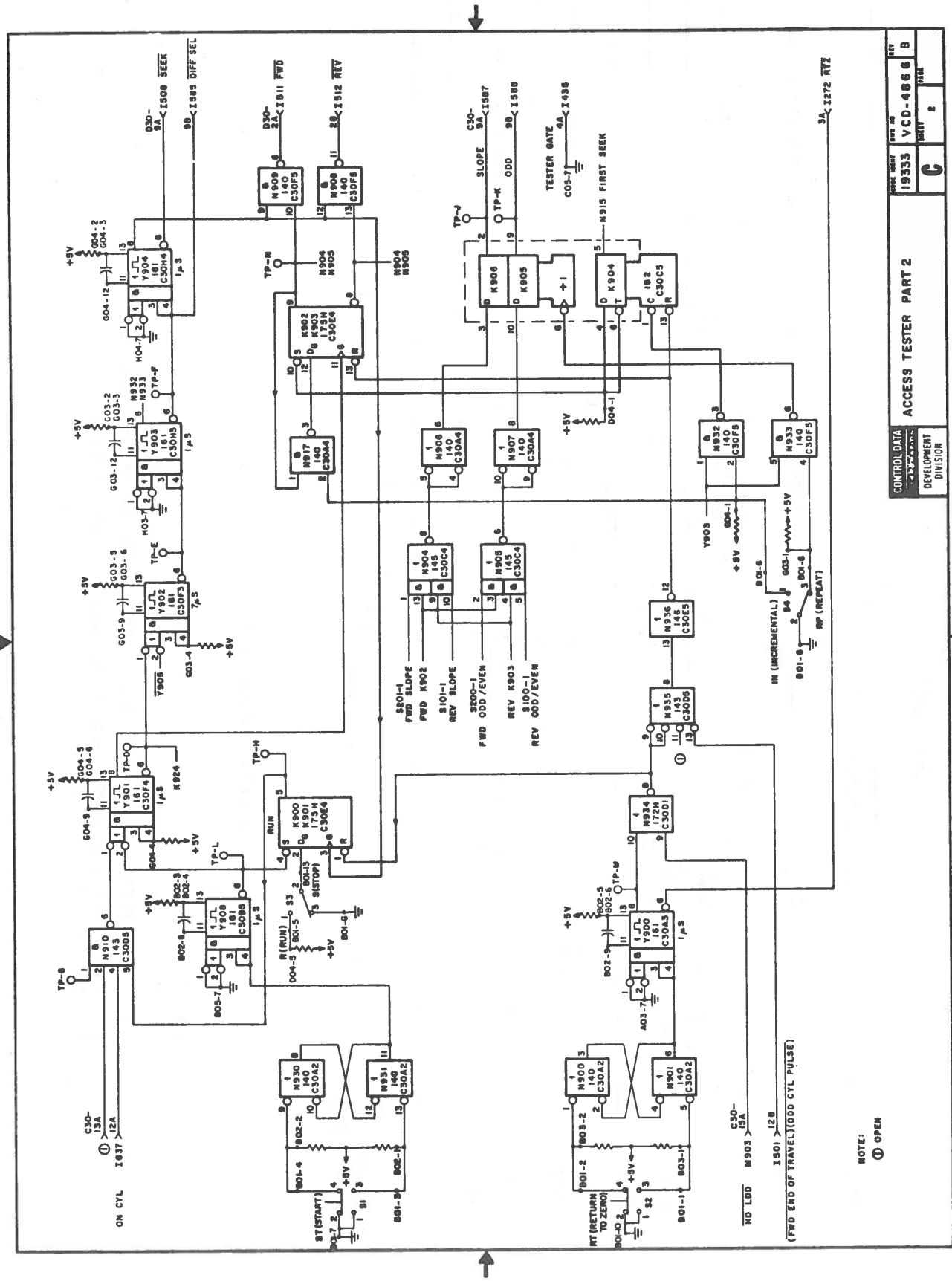
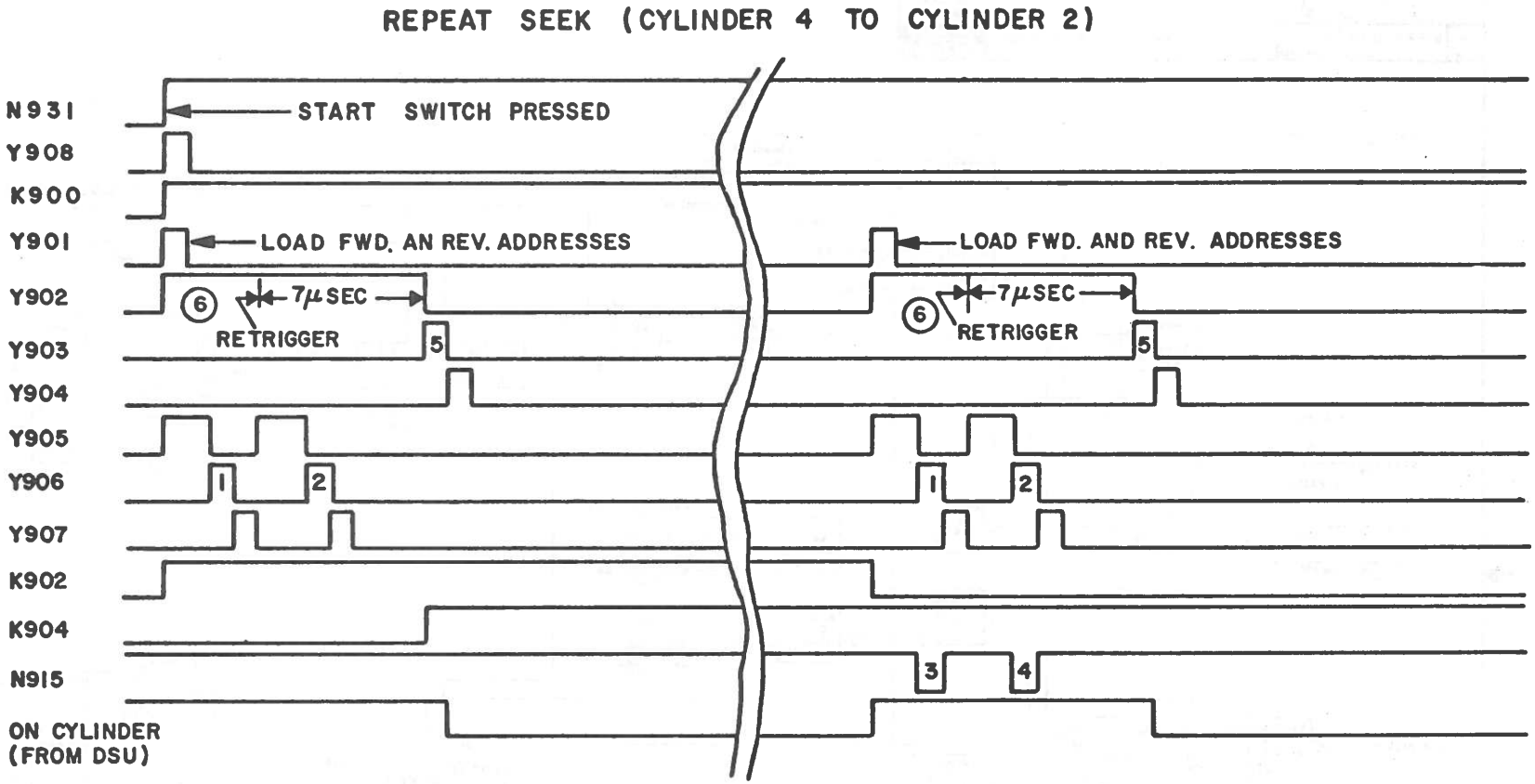


Figure 7-57. Access Tester Card Logic - Sheet 2 of 2



1. INCREMENT REVERSE COUNTER CONTENT 11111101 → 11111110
2. " " " " 11111110 → 11111111
3. INCREMENT FORWARD " " 11111011 → 11111100
4. " " " " 11111100 → 11111101
5. DELIVER DIFFERENCE FROM FORWARD COUNTER TO DSU DIFFERENCE COUNTER.
6. Y902 RETRIGGERED BY Y905 EVERY 4μSEC UNTIL REVERSE COUNTER IS INCREMENTED TO ALL ONES.

6T175

Figure 7-58. Repeat Mode Timing

9. Set tester FWD switches to binary equivalent of the higher valid track desired during the seek. (Example: To select track 100, set FWD switches 64, 32, and 4 to 1. Set other switches to 0.)

10. Set tester REV switches to binary equivalent of the lower valid track desired during the seek. (Example: To select track 10, set REV switches 8 and 2 to 1. Set other switches to 0.)

11. Press tester ST switch.

12. The DSU should now seek forward to the track specified by the FWD switches, generate an On Cylinder signal, seek in reverse to the track specified by the REV switches, and generate an On Cylinder signal.

13. The activities of step 12 will continue until either the tester RT switch is pressed or the R/S switch is set to the S position (stop).

14. Set DSU DC switch to OFF before removing tester card from logic chassis.

Incremental Mode

To exercise a DSU in the incremental mode, perform the following procedure:

1. Set DSU logic chassis maintenance panel ON LINE/OFF LINE switch to OFF LINE and set DC switch to OFF.

2. Install access tester card in DSU logic chassis location C30.

3. Set DC switch to ON.

4. Install disk pack on DSU spindle.

5. Start spindle motor and allow brush cycle to end.

6. Press tester RT (return to zero) switch, S2. DSU should load heads and return to track 0.

NOTE

This procedure is written for a one-track incremental seek. Other, but not all, increments may be selected. Valid selected increments are restricted to those where the FWD switch 1 is set to 1 and the FWD switch 2 is set to 0.

Remaining FWD switches (4 through 256) may be set as desired. Settings other than the aforementioned will result in unpredictable seek activity.

7. Set tester FWD switch 1 to 1.

8. Set all other FWD and REV switches to 0.

9. Set tester IN/RP switch to IN position (incremental).

10. Set tester R/S switch to R position (run).

11. Press tester ST switch.

12. The DSU should now seek forward, one track at a time, until the forward limit is reached, at which time the logic chassis maintenance panel FAULT indicator lights (indicates seek error). To recover from the seek error, the DSU will automatically return to track 0 and again seek forward, one track at a time.

13. The activities of step 12 will continue until either the tester RT switch is pressed or the R/S switch is set to the S position (stop).

14. Set DSU DC switch to OFF before removing tester card from logic chassis.

Single Step

To exercise a DSU in either a repeat single step mode or an incremental single step mode, perform the following procedure:

1. Perform either the procedure for repeat mode operation or the procedure for incremental mode operation, except when the applicable procedure directs positioning of R/S switch, set it to S (instead of R).

2. Now, when the tester ST switch is pressed (step 12 of both procedures), the DSU will perform one seek operation and stop.

3. Press tester ST switch each time a seek operation is desired.

READ/WRITE TESTER CARD

The R/W tester card (P/N 54113701) is a special tool used optionally with some DSU's to perform off line maintenance procedures of Section 6. Figure 7-59 is the logic drawing for the card and is provided as an aid in using the tester.

OPERATION

The R/W tester card allows checkout and diagnosis of the read/write circuits in a DSU.

Write Operation (Figure 7-60)

To write on a DSU disk pack, perform the following procedure:

1. Set DSU logic chassis maintenance panel ON LINE/OFF LINE switch to OFF LINE and set DC switch to OFF.

2. Install R/W tester card in DSU logic chassis location C23.

3. Set DC switch to ON.

   CAUTION

   A CE disk pack contains specially recorded tracks of data. Extreme care must be taken so that this data is not modified. Read or write circuit diagnosis or testing should be done using an unrecorded disk pack or one containing expendable data (scratch pack).

4. Install a scratch pack on DSU spindle.

5. Start spindle motor and allow brush cycle to end.

6. Select desired data pattern to be written by setting tester switches as follows:

Desired pattern	1-0 switch (S1)	ONE switch (S2)
All "1's"	OFF	OFF
All "1's"	ON	OFF
All "0's"	ON	ON
Alternate "1's" and "0's"	OFF	ON

7. Set tester W (write), E (erase), and C-S (control select) switches to ON.

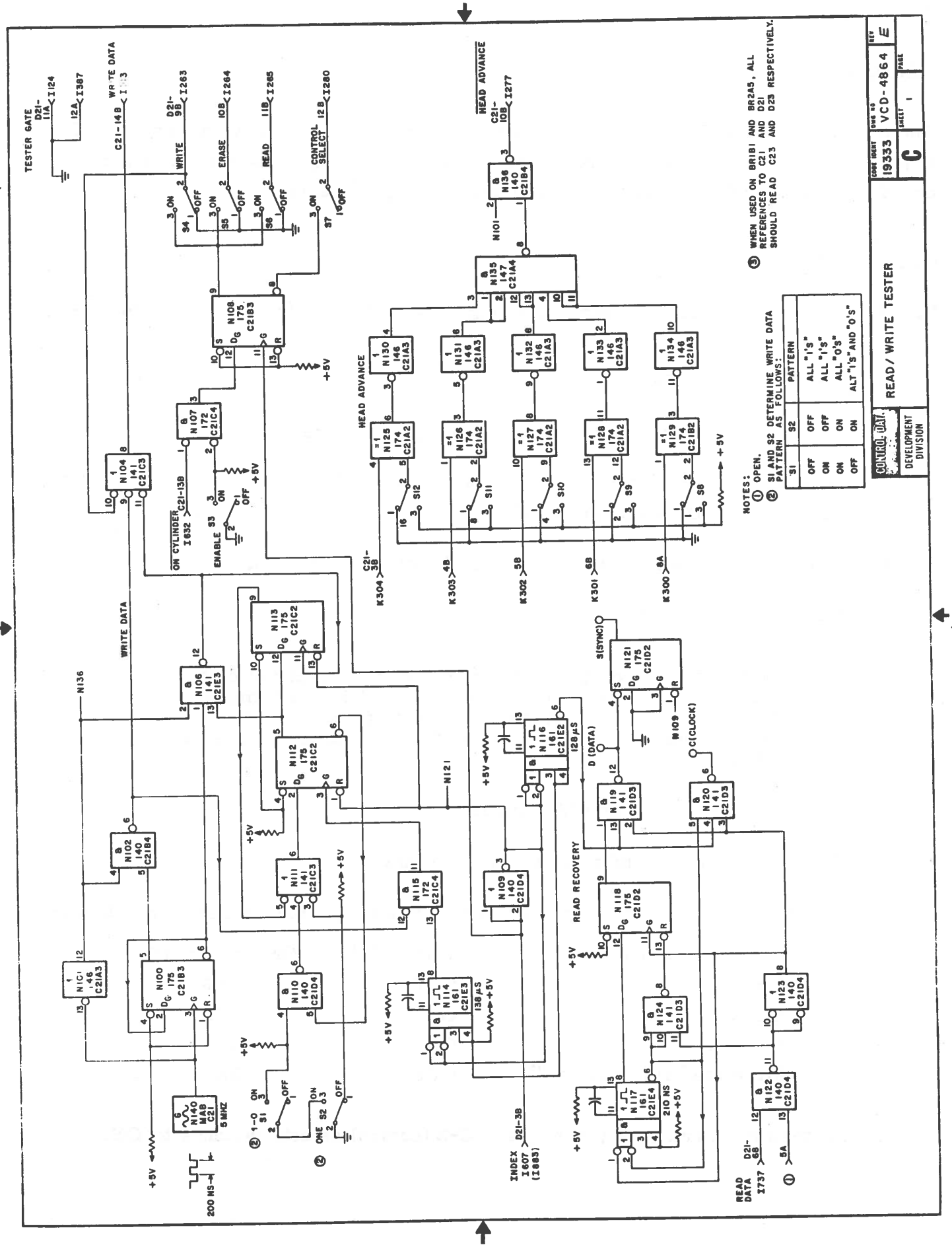


Figure 7-59. Read/Write Tester Card Logic

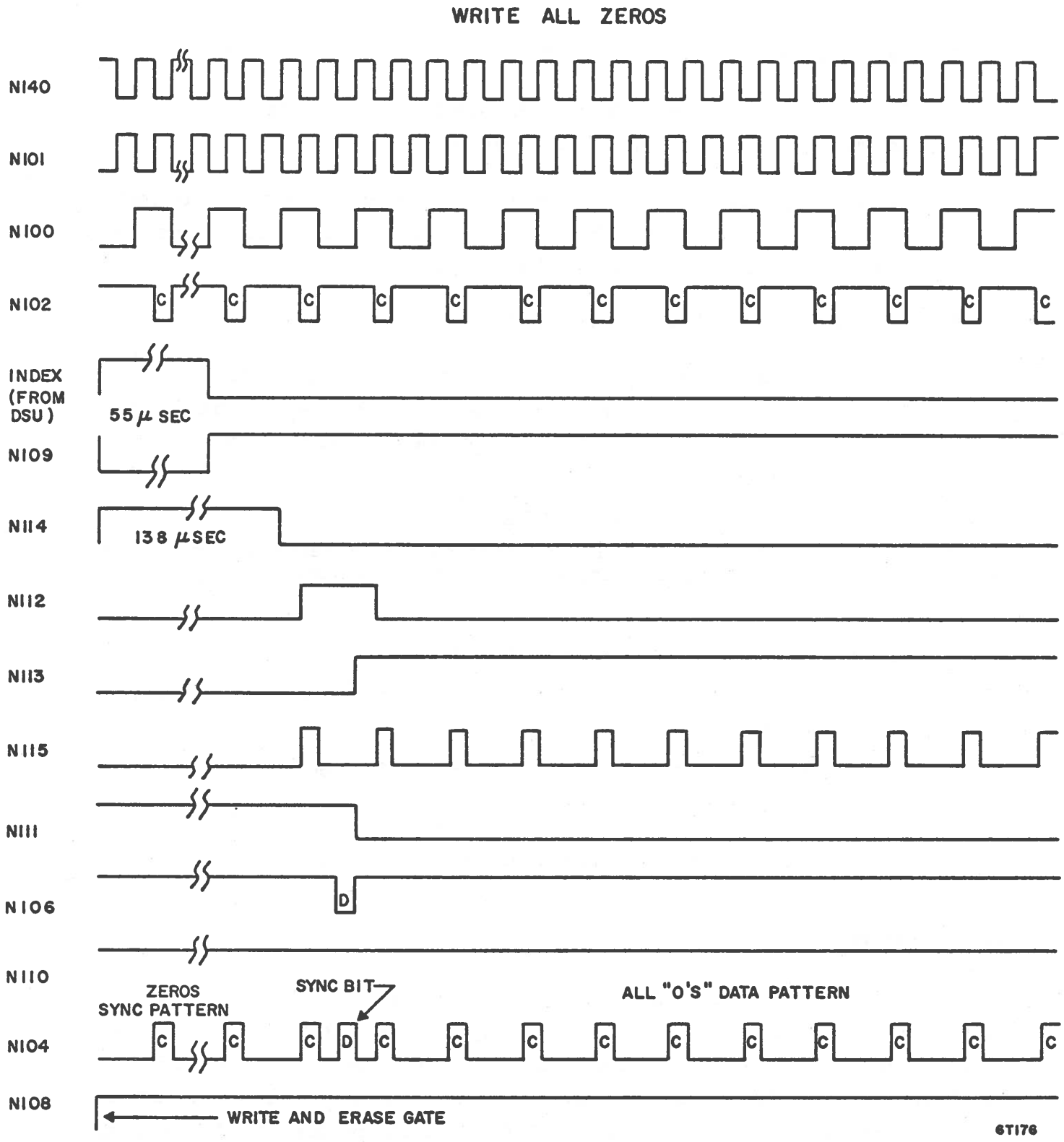


Figure 7-60. Write Operation Timing - All Zeros

8. Set tester R (read) switch to OFF.

9. Position DSU heads to desired track. (Positioning may be manually, using access tester card, or central processor.)

10. Set tester binary switches (1 through 16) representing binary equivalent of desired head to the right. (Example: To select head 11, set switches 8, 2, and 1 to the right. Set switches 4 and 16 to the left.)

11. Set tester EN (enable) switch to ON.

12. When the leading edge of Index (Figure 7-60) is sensed, a 138 μsec sync pattern of all "0's" is written. This is followed by a single data "1" sync bit and finally the pattern selected by switches S1 and S2 is written until the next leading edge of Index.

NOTE

The positions of the binary switches used to select a head may be changed during a write operation without affecting a read recovery.

13. The activity of step 12 will repeat until one of the following occurs:

- If W, E, or C-S switch is set to OFF, the write operation will stop immediately.
- If EN switch is set to OFF or a DSU not On Cylinder occurs, the write operation will stop with the next Index pulse.

14. Refer to Read Operation paragraph to recover written pattern.

Read Operation

The tester read recovery circuit is a simple discriminator designed to recover a pattern written during the above described Write Operation. The tester incorporates no checking logic, and pattern verification can be made only by monitoring the D (data) and C (clock) test jacks with an oscilloscope. Use the tester S (sync) test jack to trigger the oscilloscope. To read from a DSU disk pack, perform the following procedure:

NOTE

Following procedure assumes that tester was installed in DSU logic chassis to write a pattern, and now a read recovery of the pattern is to be performed.

1. Set tester W and E switches to OFF.

2. Set R and C-S switches to ON.

3. Set tester binary switches representing binary equivalent of desired head to the right. (Example: To select head 15, set switches 8, 4, 2, and 1 to the right. Set switch 16 to the left.)

4. Set Tester EN switch to ON.

5. When the leading edge of Index is sensed, tester generates Read Gate. Tester discriminator circuit then uses the 138-μsec all "0's" pattern to get in sync. When single-shot N116 times out (noise blanking), the recovered data "1" sync bit sets the Sync FF, N121. Then follows recovered data and clock pulses which the tester separates for monitoring (inverted) at the D and C test jacks.

6. The activity of step 5 will continue until the R, C-S, or EN switch is set to OFF.

7. Set DSU DC switch to OFF before removing tester card from logic chassis.

Information for this section is included in BR 2A5 Disk Storage Unit, Pub. No. 70614800.

SECTION 8

PARTS DATA

SECTION 9

WIRE LISTS

WIRE LISTS

DESCRIPTION OF WIRE LISTS

LOGIC WIRE LIST

The following is an example of the logic wire list with an explanation of the columns.

TITLE: LOGIC WIRE LIST				WL	SHEET NO.	DOCUMENT NO.	REV
WIRE IDENTIFICATION	COMMENT	ORIGIN	DESTINATION	Z LEVEL	REMARKS		
Y1201		C0711B	D1803A	1			
Y500		A1809B	A2002A	1			
Y503		A2008B	B1802B	1			
10026	GND	A1601A	A1610B	1			
10027	GND	A1610B	B1608B	2			
10028	P5V	B2809B	B2814B	1			
10029	RWT	D2311A	JA8107A	1			

General

Back panels are machine wired according to the following paragraphs. The wiring operation prepares the unit for a number of operational options. A wire is installed for each entry in the list even if the unit does not contain the logic card types or complement to make full use of these options.

Wire Identification/Comment

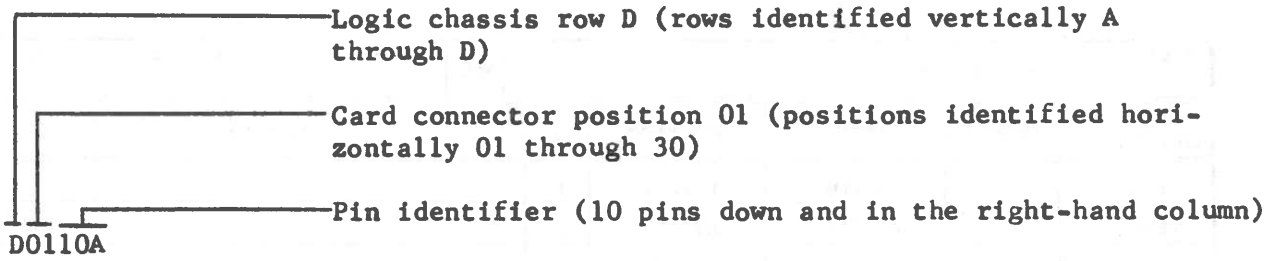
If the identifier begins with a letter, the signal on the wire originates at the listed logic term. A multiple output is indicated when a term is repeated on successive line entries. An additional digit at the end of the identifier denotes a second and different (generally a differential of the first) signal being originated by the term.

T023 - signal source is term T023
T0231 - last digit identifies a second and different signal being originated

If the identifier begins with a numeral, the signal on the wire generally originates at some point other than a logic term (switch, bus, test point, etc.). In this case, the adjacent Comment column provides a clarifying entry. A multiple output is indicated when the identifier is repeated on successive line entries.

Origin

This column locates the logic chassis wire wrap pin from which the identified wire originates.



If this column is preceded by the letter J, the origin is from one of the connectors above, below, or to either side of the area where the cards are installed. The locator (same as first four digits in this column) is etched alongside each connector.

Destination

This column locates the logic chassis wire wrap pin to which the identified wire is terminated. The location information provided for the Origin column is also applicable for this column.

Z Level

The Z level denotes the vertical separation which an installed wire has relative to the surface of the wire wrap pin board. This vertical separation is maintained at both ends of the installed wire when it is wrapped on the pins. Three vertical separation distances are possible. A numeral 1 in this column indicates the smallest separation. A 3 in the column indicates the largest separation. A level of 2 is the intermediate separation level.

NON-LOGIC WIRE LISTS

The following is an example of a non-logic wire list with an explanation of the columns.

CONTROL DATA	TITLE							WL	SHEET NO.	DOCUMENT NO.	REV
IDENTIFIER	WIRE SIZE	COLOR CODE	WIRE LENGTH	ORIGIN LOCATION	ORIGIN PIN NO.	DESTINATION LOCATION	DESTINATION PIN NO.	REMARKS			
1	12	0		FL1	1	CB2A	LINE				
2											
3	20	0		CB24	LINE	DS1	L				
4	12	3		FL1	2	CB2B	LINE				
5	12	5		FILTER CHASSIS	GND	TB5	10				
6	20	3		CB2B	LINE	DS1	R				
7	20	5		SHIELD		FILTER CHASSIS	GND				

Conductor Ident. - Not applicable to field usage

Wire Size - Size of conductor (AWG)

Color Code - Color information

Wire Length - Length of conductor in inches

Origin - Origin point of conductor

Destination - Destination point of conductor

Remarks - Useful comments

Color Code

Solid colored wires are identified by a one digit number in this column. Multicolored wires are identified by a number having two or three digits. Each digit of the number identifies one of the colors. The code numbers are identified as follows:

0 - Black	2 - Red	4 - Yellow	6 - Blue	8 - Gray	S - Shield
1 - Brown	3 - Orange	5 - Green	7 - Violet	9 - White	

In multi-digit color codes, the first digit denotes base color and the remaining digits denote tracer colors.

TITLE	WL	SHEET NO.	DOCUMENT NO.	REV
LOGIC WIRE LIST		1	VCD-7359	E

WIRE IDENTIFICATION	COMMENT	ORIGIN	DESTINATION	Z LEVEL	REMARKS
A620		B2701B	B2801B	1	
A627		A2313A	A2913B	2	
A627		A2313A	A2709B	1	
A628		A2916B	B2803B	1	
A629		B2702B	C2117B	1	
A631		A2706B	B2802B	1	
A635		B2601B	D2106B	1	
A637		B2602B	D2107A	1	
A640		B2311A	B2908B	1	
A640		B2312A	B2909B	1	
A651		A2107B	A2314B	1	
A661		A2309B	C2115A	1	
A664		A2004A	A2308B	1	
A664		A2308B	B2302B	2	
A665		A2005B	A2307B	1	
A665		A2307B	B2303B	2	
A671		B2307B	C2113B	2	
A671		A2508B	B2307B	1	
A674		A2003A	B2310B	1	
A674		B2310B	C2112A	2	
A675		A2004B	B2306B	1	
A675		B2306B	C2111A	2	
A679		A2107A	A2315B	1	
A683		A2305B	B1803A	1	
A693		B1809A	B2312B	1	
A697		B2509B	B2806B	1	
A697		B2806B	C2107B	2	
I000		C1016A	D1711B	2	
I001		D0710B	D1710B	1	
I1000		D1608A	D1703B	1	
I1001		D1704A	D1803B	1	
I1002		D1513B	D1609A	1	
I1004		D1509A	D1606B	1	
I1005		D1507A	D1607B	1	
I1006		D1503B	D1604B	1	
I1007		D1504A	D1603B	1	
I1008 I1008		C0810A C0807B	D1702A C0810A	1 2	
I1009		C0915B	D1703A	1	
I1010		C0811B	D1705B	1	
I1011		D0908A	D1704B	1	
I1013		D0908B	D1513A	1	

TITLE		WL	SHEET NO.	DOCUMENT NO.	REV
LOGIC WIRE LISTS			2	VCD-7359	E

WIRE IDENTIFICATION	COMMENT	ORIGIN	DESTINATION	Z LEVEL	REMARKS
I1014		C0807A	D1510B	1	
I1015		C0915A	D1511B	1	
I1017		C0909A	D1509B	1	
I1019		C0909B	D1507B	1	
I1021		C0905A	D1503A	1	
I1023		C0905B	D1504B	1	
I1025		D1709A	D1808A	1	
I1026		D1707A	D1812A	1	
I1027		D1811A	D1913B	1	
I1028		D1809A	D1910A	1	
I1029		D1806B	D1909A	1	
I1030		D1807B	D1907A	1	
I1031		D1612A	D1903B	1	
I1032		D1611A	D1904A	1	
I1034		C0914A	D1709B	1	
I1036		D0909B	D1707B	1	
I1038		D0907A	D1913A	1	
I1040		C0916A	D1911B	1	
				1	
I1042		C0908B	D1909B	1	
I1044		C0910A	D1907B	1	
I1046		C0904B	D1903A	1	
I1047		C0809B	D1905B	1	
I1048		C0906A	D1904B	1	
I1050		C0912B	D2008A	1	
I1051		D0910B	D2004B	1	
I1052		D0906A	D2009A	1	
I1053		C0917A	D2011A	1	
I1054		C0907B	D2006B	1	
I1055		D0911A	D2007B	1	
I1056		C0903B	D2012A	1	
I1057		D0912B	D2003B	1	
I1070		C0813B	D0905B	1	
I1071		C0911A	D1003A	1	
I1072		D0911B	D1003B	1	
I1073		C1012B	D0912A	1	
I1074		C1012A	D0901B	1	
I1075		C0907A	C1014B	1	
I1076		C0911B	C1013A	1	

TITLE				WL	SHEET NO.	DOCUMENT NO.	REV
LOGIC WIRE LISTS					3	VCD-7359	H

WIRE IDENTIFICATION	COMMENT	ORIGIN	DESTINATION	Z LEVEL	REMARKS
I1077		C0903A	C1016B	1	
I1078		C0902A	C1015B	1	
I1082		D1713A	D2005A	1	
I1101		C0714A	C0802A	1	
I1104		D1512B	D1705A	1	
I1104		D1506A	D1508A	2	
I1104		D1508A	D1511A	1	
I1104		D1511A	D1512B	2	
I1104		D0809B	D1702B	1	
I1104		D1702B	D1705A	2	
I1104		D1502B	D1506A	1	
I1104		D1502B	D1505A	2	
I1105		D0809A	D1708A	1	
I1105		D1902B	D1906A	1	
I1105		D1906A	D1908A	2	
I1105		D1908A	D1911A	1	
I1105		D1706A	D1912B	1	
I1105		D1706A	D1708A	2	
I1105		D1911A	D1912B	2	
I1105		D1902B	D1905A	2	
I1107		D1605A	D2010B	2	
I1107		D0806B	D1605A	1	
I1111		C0809A	D2009B	1	
I1112		B1004A	C0817A	1	
I1118		D1605B	D1805B	2	
I1118		C0816A	D1605B	1	
I1124		D0808B	D2010A	2	
I1125		C0815A	D1810A	1	
I1125		D1810A	D1811B	2	
I1126		A1811B	D0706A	1	
I1126		A1811B	D1710A	2	
I1126		C0814A	D1710A	1	
I1129		B1004A	C1017A	2	
I1129		C0816B	C1017A	1	
I1153		B2012B	C0803A	1	
I1155		C0806B	D1610B	1	
I1200		C0715B	D1611B	1	
I1200		D1611B	D1806A	2	
I1204		D0708B	D0805B	1	