



77711044


CONTROL DATA®

LARKTM 50 MICRO UNIT

MODEL 9457

**GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE (Non-Sealed Area)
PARTS DATA (Non-Sealed Area)**

MAGNETIC PERIPHERALS INC.

 a subsidiary of
CONTROL DATA CORPORATION

MODULE II

HARDWARE MAINTENANCE MANUAL

PREFACE

Module II of this manual provides the information needed to install, operate, maintain, and troubleshoot the Lark Micro Unit (LMU).

This module is a compilation of Control Data Corporation's Lark Micro Unit Installation/Operation Manual (# 77711044) and Lark Micro Unit Hardware Maintenance Manual (# 77711050).

The total content of this module is comprised of seven sections:

| <u>SECTION</u> | <u>TITLE</u> |
|----------------|---------------------------|
| 1 | GENERAL DESCRIPTION |
| 2 | OPERATION |
| 3 | INSTALLATION AND CHECKOUT |
| 4 | THEORY OF OPERATION |
| 5 | DIAGRAMS |
| 6 | MAINTENANCE |
| 7 | PARTS DATA |

NOTE

The Lark Micro Unit (LMU) and the Power Supply & I/O Adapter (PIO) are separate and distinct devices, with their own unique documentation. The LMU is identified as Model 9454 (the 16MB unit) or 9457 (the 50MB unit). The 16MB unit is used with the No Problem Shared System™ and requires Lanier Service Manual Z-200-299 for the PI/O and Z-200-300 for the Model 9454 Micro Unit. This manual on the 50MB unit consists of three modules--Module I covers the PI/O, Module II covers the Model 9457 Micro Unit, and Module III contains a listing of the Lark Status Codes.

EMI NOTICE: This equipment has been designed as a component to high standards of design and construction. The product, however, must depend on receiving adequate power and environment from its host equipment in order to obtain optimum operation and to comply with applicable industry and governmental regulations. Special attention must be given by the installers and CSRs in the areas of safety, input power, grounding, shielding, and environment temperature of the device to insure specified performance and compliance with all applicable regulations.

OPERATOR SAFETY INSTRUCTIONS

1. All operator controls can be found on the front panel.
 - 1.1 Start/Stop Switch
This switch energizes the spindle motor. The indicator light flashes until motor is up to speed.
 - 1.2 Requirements
The following conditions must be met to initiate operation of the On/Off switch:
 - a. The external power source must be on.
 - b. The disk cartridge must be properly inserted and the access door tightly closed.
 - 1.3 Fixed Prot Switch
This switch has an error interrupt indicator lamp. An error is present in the drive when the lamp is flashing.
2. OPERATING TEMPERATURE
The operating temperature of the drive is 10° to 40° C with a maximum temperature change of 10° C per hour.
3. Additional information on the drive can be found in Hardware Maintenance Manual 77711050.
4. The corresponding VDE regulations must be observed during installation.
5. Note: The spindle drive motor may reach a temperature of 70° C.
6. In case of a malfunction the unit is to be serviced only by trained personnel. The access door can be opened only by trained personnel after the power has been switched off.

BEDIENUNGSANLEITUNG

1. Alle Benienungseinrichtungen befinden sich an der Frontseite.
 - 1.1 Ein-und Ausschalter:
Dieser Schalter hat die Funktion den Motor und die Logik mit Strom zu versorgen. Die eingebaute Kontrolllampe blinkt so lange bis der Antriebsmotor seine Drehzahl erreicht hat.
 - 1.2 VORAUSSETZUNG
Voraussetzung zur Funktion des Aus-Einschalters ist:
 - a) Die aussere Stromversorgung muss einschaltet sein.
 - b) Die Kasette ist eingeschoben und die Bedienungsklappe ist geschlossen.
 - 1.3 Der zweite Drunkschalter (FIXED PROT) ist ebenfalls mit einer Fehleranzeigelampe ausgestattet. Ein Fehler im Gerat ist vorhanden wenn diese Anzeige blinkt.

2. BETRIEBSTEMPERATUR
10° C bis 40° C bei einer Änderung von 10° C innerhalb einer Stunde.
3. Zusätzliche Informationen sind zu ersehen im Hardware Maintenance Manual - 77711050.
4. Beim Einbau des Gerätes sind die einschlagigen VDE-Vorschriften einzuhalten.
5. Zu beachten ist, dass der Antriebsmotor eine Betriebstemperatur von ca. 70° C erreichen kann.
6. In Falle eines Defektes darf das Gerät nur von Fachpersonal nach Abschalten der Stromzufuhr geöffnet werden.

MODULE II

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1.1 INTRODUCTION

The Lark 50 Micro Unit (9457) is a small, low cost, medium performance, random access, rotating disk mass memory device featuring both removable and fixed storage. The Lark 50 Micro Unit (LMU) employs the latest 8 inch rigid disk technology using low mass flying read/write heads attached to a precisely controlled linear head positioner. The unformatted storage capacity of the LMU is 50 Mbytes. 25 Mbytes of storage is provided by the removable disk (cartridge) and 25 Mbytes of storage is provided by the non-removable disk.

1.2 GENERAL DESCRIPTION

1.2.1 STANDARD FEATURES

The following are standard features of the LMU:

- 25 MB front-loading cartridge receiver (cartridge not included)
- 32 or 64 hard sector configurations
- Early/late data strobing
- Independent manual write protect on fixed and/or cartridge media (switch for fixed; special tab on cartridge)
- Internal fault monitoring
- LSI and Microcomputer control
- No electrical adjustments required
- No head alignment required
- Low power consumption
- Low acoustic noise
- Small physical size
- Embedded servo
- Self circulating air filtration system
- Vertical or Horizontal Operation

1.2.2 MAJOR COMPONENTS

The LMU consists of major assemblies as illustrated in Figure 1-1.

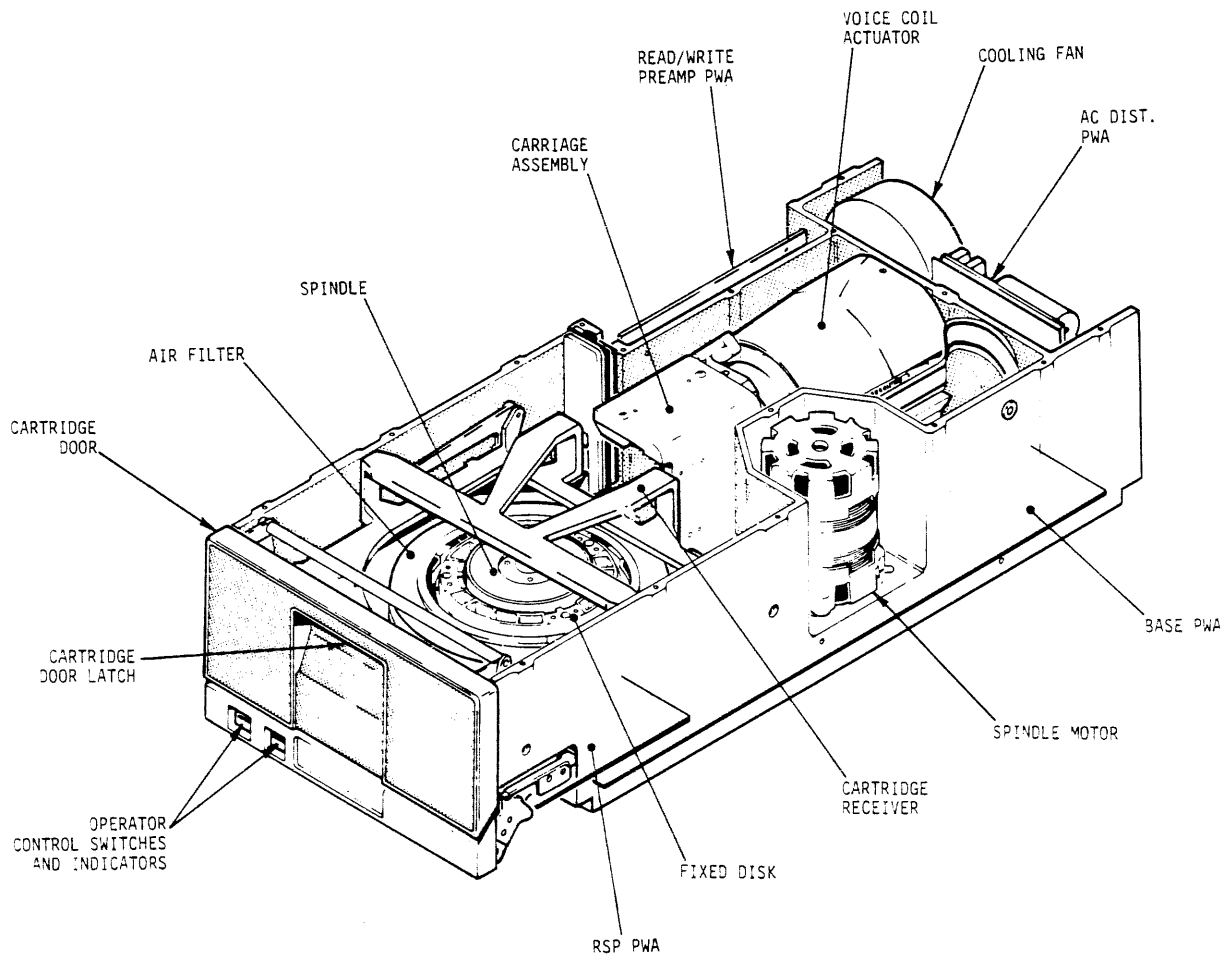
The following major components make up the LMU:

- Electronics

The logic is implemented using low power Schottky for commands and control logic and standard Schottky and ECL for the read/write and servo logic. The microprocessor is designed with standard microcomputer building blocks. The logic is mounted on three PWA's: Base PWA, Read/Write Preamp PWA and Read Signal Processor PWA.

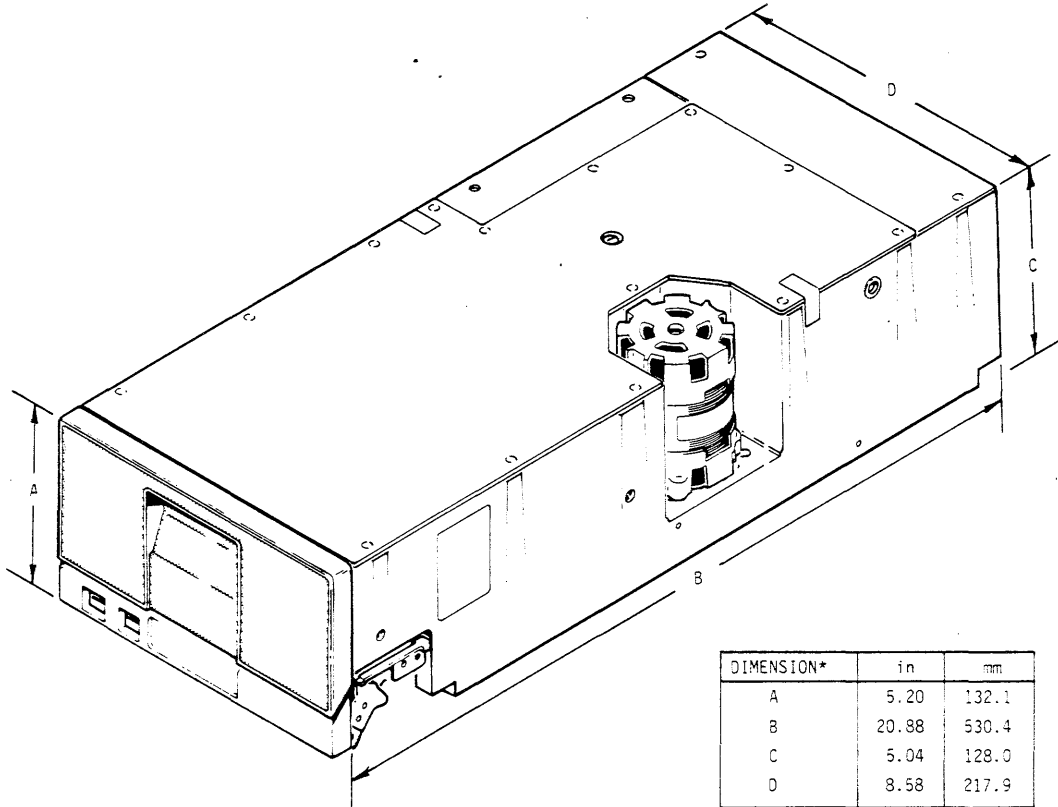
- Voice-Coil Head Positioner

Head positioning is performed using a closed-loop proportional servo system with acceleration, velocity and position feedbacks. The carriage is driven by a voice-coil linear actuator utilizing positioning information from embedded servo information.



FF018a

FIGURE 1-1. LMU MAJOR COMPONENTS



| DIMENSION* | in | mm |
|------------|-------|-------|
| A | 5.20 | 132.1 |
| B | 20.88 | 530.4 |
| C | 5.04 | 128.0 |
| D | 8.58 | 217.9 |

WEIGHT - 40 LBS (18 kg)

* MAX DIMENSIONS

EF018b

FIGURE 1-2. LMU PHYSICAL CHARACTERISTICS

- Deck and Spindle

A rigid cast-aluminum deck and precision spindle insures positive registration and seating of cartridge. An AC induction motor provides spindle rotation through a belt and pulley.

- Air Supply and Filtering

A direct drive blower provides external cooling air for the electronics located outside sealed area. Internal air in the sealed area of the unit is continually recirculated through a filter that separates the fixed disk area from the cartridge receiver area, provided the disk cartridge is installed.

- Cartridge Receiver

A front-load cartridge-receiving mechanism integral to the deck assembly facilitates the insertion and removal of cartridge media.

- Operator Control Panel

Controls and indicators for use by the operator are located in the LMU front panel. These are START/STOP switch, READY indicator (part of START/STOP switch), FIXED PROT switch, and FAULT indicator (part of FIXED PROT switch).

NOTE

The LMU is a component and therefore does not require a FCC label.

1.2.3 OPERATIONAL CHARACTERISTICS

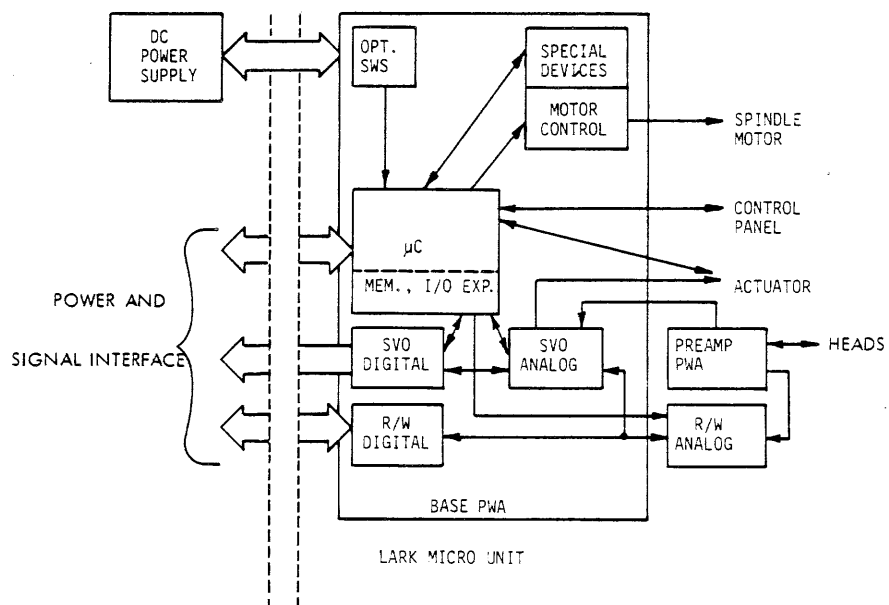
Operational characteristics of the LMU are summarized in Table 1-1.

1.3 FUNCTIONAL BLOCK DIAGRAM

A functional block diagram of the LMU is shown in Figure 1-3. The majority of the electronics is located on one large printed circuit board called the Base PWA which is mounted in the base of the LMU (shown enclosed by dotted lines in Figure 1-1). The Preamp PWA and the RSP PWA amplify and process the signals read from the disk. The AC Distribution PWA controls the AC power distribution to the fan motor and the spindle drive motor.

TABLE 1-1. OPERATIONAL CHARACTERISTICS SUMMARY

| TOTAL CAPACITY (UNFORMATTED) | LARK 50 |
|------------------------------|-----------------------------------|
| Removable Disk Cartridge | 25 MB |
| Fixed Disk | 25 MB |
| Total | 50 MB |
| Number Cylinders (Total) | 624 |
| Number Heads: | |
| Removable | 2 |
| Fixed | 2 |
| Total | 4 |
| Unformatted Track Capacity | 20,672 Bytes |
| Recording Mode | (2,9) |
| BPI | 10,166 |
| TPI | 715 |
| Spindle Speed | 3510 $\pm 3.0\%$ / -4.8% r/min |
| Data Transfer Rate (Nominal) | 9.677 MHz |
| Maximum Latency | 17.94 ms |
| Average Latency | 8.55 ms |



GG300

FIGURE 1-3. LMU FUNCTIONAL BLOCK DIAGRAM

2.1 INTRODUCTION

This section provides the instructions and information required to operate the Lark 50 Micro Unit.

2.2 OPERATOR CONTROLS AND INDICATORS

Figure 2-1 shows the location of the operator controls and indications. All operator controls and indicators are on the front panel. A functional description of these controls and indicators is given in Table 2-1.

2.3 OPERATING PRECAUTIONS

The following precautions and practices are to be observed while operating the LMU to obtain best performance and reliability of the equipment:

1. Keep a cartridge in the unit at all times and keep the access door closed to prevent unnecessary entry of atmospheric contaminants.
2. To prevent damage and/or data loss, follow the Disk Cartridge Installation procedure of this section.
3. The operator should not attempt to override any interlocks in the system.

WARNING

Removing seal or top cover on sealed area voids warranty.

NOTE

If a pinging or scratching sound (caused by head-to-disk contact) is heard and persists, stop the unit by using the Stop and Power down procedure of this section.

NOTE

If while the drive is operating the Cartridge Receiver Door Latch Release (Figure 2-1) is inadvertently operated sufficiently to cause the spindle to begin slowing (READY indicator blinks), place the START/STOP switch in the STOP position and allow the spindle to come to a complete stop. Remove the cartridge and inspect the door mechanism for any damage. In the absence of damage, re-insert the cartridge and restart the drive in a normal manner.

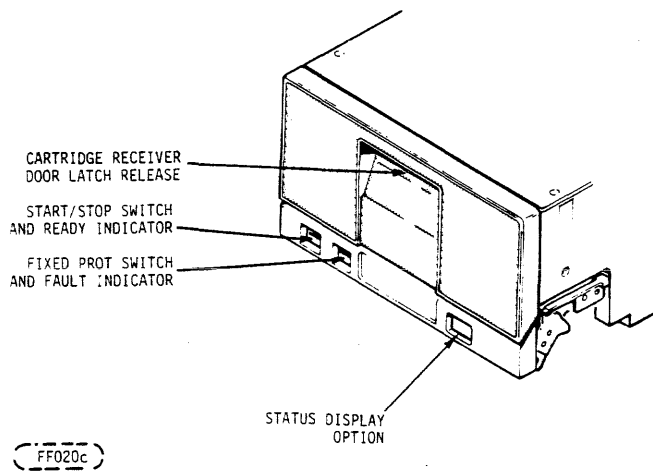


FIGURE 2-1. OPERATOR CONTROLS AND INDICATORS

TABLE 2-1. CONTROLS AND INDICATORS (SHEET 1 OF 2)

| CONTROL OR INDICATOR | FUNCTION |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| START/STOP switch/indicator | <p>Start switch energizes spindle motor and initiates the first seek mode provided the following conditions are met:</p> <ol style="list-style-type: none"> 1. AC Power is present (ON) at the LMU. 2. Disk cartridge loading door closed and latched with cartridge in place. 3. WRITE PROT indicator is not blinking, indicating a no fault condition. |
| READY indicator | <p>Located within the START/STOP switch. READY indicates unit ready status. READY indicator is illuminated whenever unit has completed purge cycle and heads are loaded.</p> <p>The READY light will blink throughout the spindle start and stop procedure.</p> <p>As long as the heads are on cylinder, the READY indicator will be illuminated even though the WRITE/PROT indicator may blink to show a fault.</p> |

TABLE 2-1. CONTROLS AND INDICATORS (SHEET 2 OF 2)

| CONTROL OR INDICATOR | FUNCTION |
|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| READY indicator (contd.) | The Lark 50 indicator will rapid blink during drive activity to indicate that the drive is either seeking, reading, writing or doing self test. |
| FIXED PROT switch/FAULT indicator | When operated to the inward position, this alternate action switch disables the write driver to the fixed media. The indicator, when illuminated steadily, indicates that the fixed disk is write protected. When the indicator blinks, it indicates a fault condition occurred or exists. Rapid blinking (with READY inactive) indicates a cartridge "Protect Data Quality" fault (see Section 2.5). |
| Disk Cartridge Access Door Latch | The Disk Cartridge Access Door is unlatched by lifting with the fingers on the latch that is under the lip of the recess in the access door. The latch will not release the door catch until the spindle motor has stopped rotating and the interlock solenoid releases the catch. The START/STOP switch must also be released (OUT) before the solenoid will release the catch. In the event of the loss of AC power, the interlock solenoid does not release the catch in order to prevent damage to the cartridge. |
| Status Display Option | Detailed status of the operation of the drive can be obtained for faults which the controller is unable to clear. The FIXED PROTECT switch may be depressed twice which will attempt to clear the fault and display up to sixteen status codes that occurred since the last fault clear command was sent (either thru the interface or the same front panel switch). These alphanumeric codes should be recorded and given to qualified maintenance personnel for interpretation. |

2.3.1 POWER UP FOR ON-LINE OPERATION

The following procedure is to be performed after the installation procedure has been completed including initial checkout and for normal day-to-day on-line operation.

1. Install disk cartridge in accordance with "Disk Cartridge Installation Procedure". Insure correct cartridge is selected (correct number of sectors, etc.)
2. Position START/STOP switch to START (inner) position. The front panel door will lock, READY will blink, and the spindle will start if the door is fully closed with a cartridge installed. If the spindle reaches the proper speed, the heads should load, servo adjustments will be made, and READY will rapid blink during cartridge "Protect Data Quality" tests (see Automatic Self Test section). READY should then stop blinking and remain illuminated (indicating the drive is READY for commands from the controller). Any seek, read, or write activity requested over the interface will then cause the READY Indicator to rapid blink again.

If the FAULT indicator starts blinking after a START sequence, attention should be given to the type of FAULT indicated. If FAULT blinks at a normal rate, the problem is probably drive related and attempts should be made to clear the fault using the FIXED PROT switch (see Section 2.4). READY should be active after the fault is cleared.

If the FAULT indicator rapid blinks after a START sequence, a cartridge "Protect Data Quality" fault has occurred indicating that the cartridge should be replaced after the fault is cleared (see Section 2.5 for details). READY will be active after the fault is cleared.

2.3.2 WRITE PROTECT OPERATION

1. Prepare disk cartridge by sliding write protect tab to the "up" position in slot (see Figure 2-3).
2. Perform "Power up for on-line operation" procedure.
3. Place drive in "Write Protect Mode" by pushing in FIXED PROT switch. FIXED PROT indicator will illuminate.

2.3.3 STOP OPERATION

1. Depress the START/STOP switch to STOP (extended) position. The READY indicator will blink until spindle has stopped rotating and then extinguish when spindle has stopped. Note that a "Protect Data Quality" test will occur during rapid blinking.
2. Remove the disk cartridge (if desired) in accordance with the "Normal Disk Cartridge Removal" procedure. The LMU front door panel does not unlock until READY indicator stops blinking and then extinguishes.

2.3.4 POWER DOWN

Position the AC power source switch to OFF (ON/OFF switch is not on the LMU). Preferably, this is to be done only after the LMU has been stopped in accordance with the normal "Stop Operation" procedures.

NOTE

Operating the AC power ON/OFF switch is normally performed by maintenance personnel.

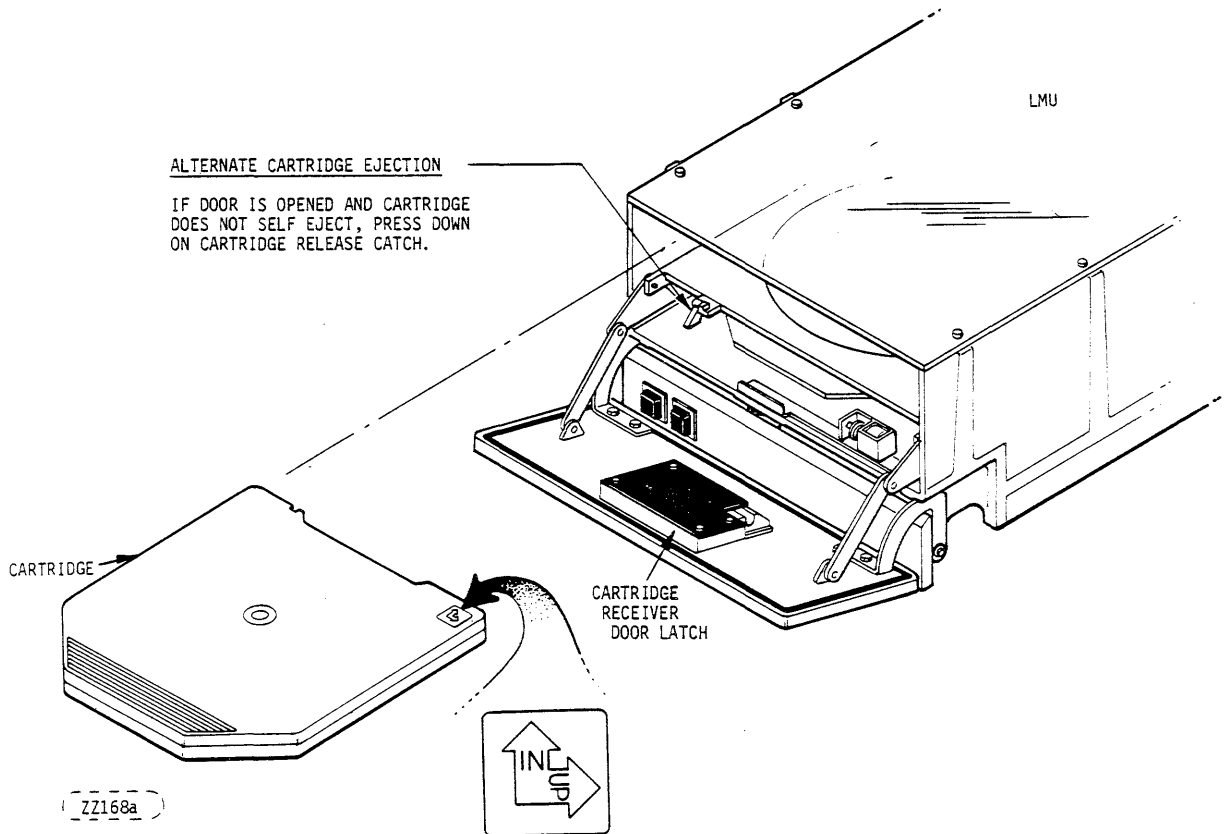


FIGURE 2-2. DISK CARTRIDGE; CARTRIDGE INSTALLATION AND REMOVAL

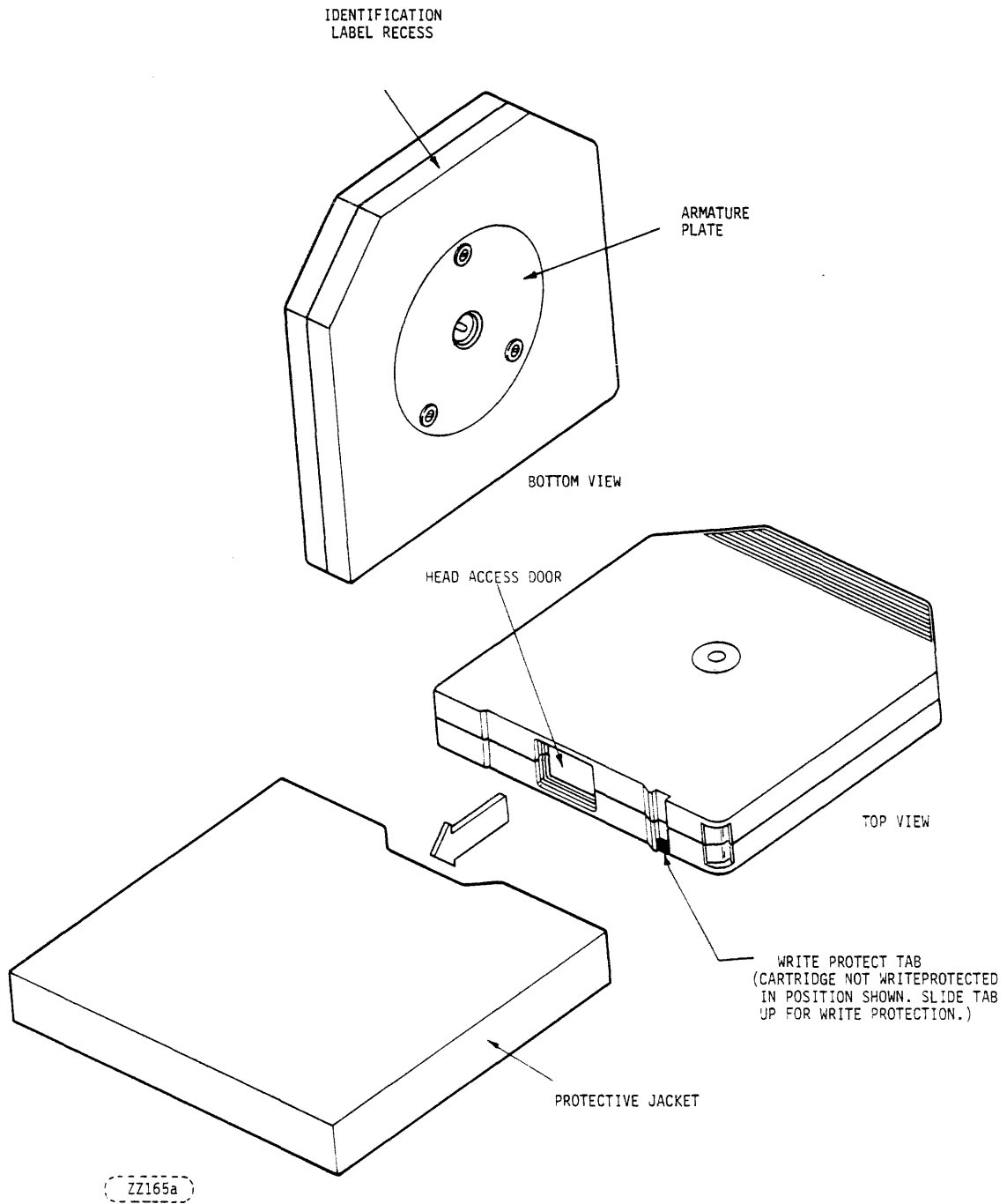


FIGURE 2-3. DISK CARTRIDGE SHOWING PROTECTIVE JACKET AND WRITE PROTECT TAB

2.4 FAULT OPERATING INSTRUCTIONS

A blinking FIXED PROT indicator indicates a fault exists in the drive. If this condition occurs, proceed as follows:

1. Actuate FIXED PROT switch twice to initiate a Fault Reset and return switch to original position. If FIXED PROT has ceased blinking, normal operation can be resumed. If the indicator still blinks, proceed to step 2.
2. Perform the "Stop Operation" and "Power Down" procedures then power up and start the unit again. If the FIXED PROT indicator still blinks, contact qualified maintenance personnel.

NOTE

See next section if FAULT is rapid blinking.

2.5 AUTOMATIC SELF TEST CAPABILITY

Upon initial power application, a Micro Processor within the LMU performs a self test function. This test is limited to the Micro Processor, its memory and I/O ports. A fault during this test sequence will be indicated by the Fixed Write Protect/Fault LED's failure to be reset within six seconds.

The next level of testing will occur after initial head loading. The Micro Processor will issue a series of seek commands while automatically adjusting velocity feed back to optimize access time. If the LMU should retract its heads during normal operation due to a fault condition, this test will be re-initiated via a Fault Clear command that results in a successful head load attempt.

The final phase of automatic testing is performed on the removable media and heads after each head load and prior to each head unload. Because of its industry uniqueness, based on a "Lark Technology" enhancement, it is named the Lark "PDQ" (Protect Data Quality) feature. It consists of a head/media performance test that will allow early detection of impending head/media failure before serious damage can occur. Three significant benefits are available to the user from this technology advancement: First, data is almost always recoverable, second, drive damage requiring depot level refurbishment is significantly reduced if not eliminated, and third, the undesirable effects of propagation to other components are eliminated.

When the velocity calibration test is complete, the Lark will automatically perform a sequential forward/reverse seek on each removable media surface while monitoring relative embedded servo amplitudes. If the amplitude delta exceeds a defined limit, the user is notified of a potential problem via the interface Fault line (SMD interface) or Fault bit (LDI interface) and a rapid blinking Fault indicator on the front operator panel with Ready indicator off.

If the "PDQ" fault is indicated, the user may, if desired, reinitiate the test by issuing a Fault Clear command either over the interface or by manual intervention using operator panel Fixed Write Protect/Fault Clear switch. The retest may be commanded a maximum of five times at which time the fault will be unclearable. It is recommended if the drive passes any subsequent retest to

copy data from the removable media immediately and remove the failing cartridge from use. Due to the characteristics of "Lark Technology" and early detection of failure, the drive will usually remain serviceable by installing a new cartridge.

In those cases where subsequent retries are unsuccessful, the user has still another option. However, it will require the assistance of a Field Engineer. The Engineer can disable the "PDQ" protective feature which effectively lowers the read threshold circuit. This allows another opportunity to recover the data and still keep the drive serviceable.

Customers may further identify a "PDQ" fault by recording the status codes. Any series of codes that include 88, 8A, 8C, 8D indicate a cartridge with a PDQ fault which should be replaced. 8A and 88 indicate a fault (on head 0 or head 1 respectively) which may be retried. 8D indicates that no further retries are available. The two status codes following one of these codes indicate the first defective cylinder address (in a modified form).

2.6 REMOVABLE DISK CARTRIDGE HANDLING AND STORAGE

The following practices should be observed when handling or storing disk cartridges.

NOTE

The cartridge is not to be shipped in the disk drive.

1. The cartridge should be stored in its protective jacket when not in the disk receiver, see Figure 2-3.
2. Cartridges can be stored flat or on edge. Avoid stacking Disk Cartridges on one another.

2.7 REMOVABLE DISK CARTRIDGE INSTALLATION

The removable disk cartridge must be stored in the same environment as the LMU for 60 minutes immediately preceding its use. In the event that it becomes necessary to use a Cartridge which has not been allowed to stabilize at the ambient LMD environment temperature for at least one hour or; a cartridge which was exposed to temperatures below 60° F (16° C) immediately prior to the stabilization period then the following procedures must be employed:

- a. The cartridge must be visually inspected or examined to insure that condensation is not present on any part of cartridge and;
- b. The cartridge must be allowed to spin on the LMU for a period of not less than five minutes prior to attempting to read or write on that cartridge.

Install the disk cartridge using the following procedure and refer to Figure 2-2.

1. Release latch under lip of front panel door recess and pull down cartridge area access door.

NOTE

Power must be applied to LMU, START/STOP in STOP (OUT) Position. READY indicator must be off and FIXED PROT indicator not blinking to release latch on front door panel.

2. Remove cartridge from protective jacket. Store jacket in such a way as to prevent dust from collecting inside the jacket.
3. Slide disk cartridge into receiver track, ensuring that the head opening is towards rear of drive and top surface* of cartridge is up.
4. Push disk cartridge in until it stops.
5. Close disk cartridge access door and press the door closed until it is latched. The disk cartridge seats into place on the spindle automatically as the access door is closed.
6. Operate the START/STOP switch to apply power to the spindle motor.
7. If the spindle motor will not rotate, the disk cartridge access door may not be completely closed or the disk cartridge may not be properly seated on the spindle chuck or the cartridge receiver/base may not be positioned properly on the lower chassis. If this occurs remove the cartridge and reinstall as outlined in the previous steps.

2.8 DISK CARTRIDGE REMOVAL

2.8.1 NORMAL REMOVAL

Refer to Figure 2-2 for the following procedure.

1. Operate START/STOP switch to STOP (out).
2. Pull down the Cartridge access door after the READY indicator ceases blinking and extinguishes entirely. When the access door is completely open the disk cartridge will partially eject out of the receiver.
3. Pull the cartridge out of the receiver.
4. Close the access door if another disk cartridge is not to be installed at this time. However, a disk cartridge should be in the drive at all times to prevent unnecessary entry of atmospheric contaminants into the sealed area of the drive. The drive will not operate without the disk cartridge installed.

NOTE

It is important that the door on the LMU remain closed when the drive is not in use. Good housekeeping accentuates high reliability.

*Top is marked "TOP".

2.8.2 POWER FAILURE OR EMERGENCY STOP REMOVAL

In case of an emergency need to remove the cartridge, perform the following procedure. (Refer to Figure 2-4):

NOTE

The procedures below should be performed only by qualified maintenance personnel.

1. If possible, check to see if the heads are unloaded. A small area of clear plastic over the carriage area is provided for that purpose.
2. If the heads are loaded (they are still flying over the disks), they must be carefully retracted manually before stopping the spinning of the disks (if they are still spinning). To manually retract the heads, carefully lift the front of the unit until the heads slide back into unloaded position. When the carriage is fully retracted, screw the lock pin into place to prevent the heads from rolling out of the fully unloaded position. There is a carriage locking solenoid, but it does not lock the carriage back until AC power is removed. However, the cartridge door cannot be opened in the normal manner if power is removed from the LMU.
3. Stop the unit and wait approximately 3 minutes for the disk cartridge to stop spinning.

CAUTION

Verify spindle rotation does not exist prior to defeating the door interlock. Refer to Disk Cartridge Removal Procedure. The cartridge removal procedure must be performed only by qualified maintenance personnel and should be only for drive failure. The cartridge access door should always be closed after the cartridge is replaced with a dummy cartridge.

4. Open the disk cartridge access door. This automatically removes disk cartridge from spindle chuck. Door will not open if a fault exists. Power must be ON and START/STOP switch out to retract door latch solenoid. Pull disk cartridge out and store in protective jacket. Close door if another disk cartridge is not to be installed. However, it is best to install a scratch disk cartridge having no valuable data.

In an emergency (emergency only) if the disk cartridge access door will not open proceed as follows:

1. Make sure the spindle motor has completely stopped. Either observe the motor or wait a full 3 minutes after initiating a stop. Make sure heads are retracted.

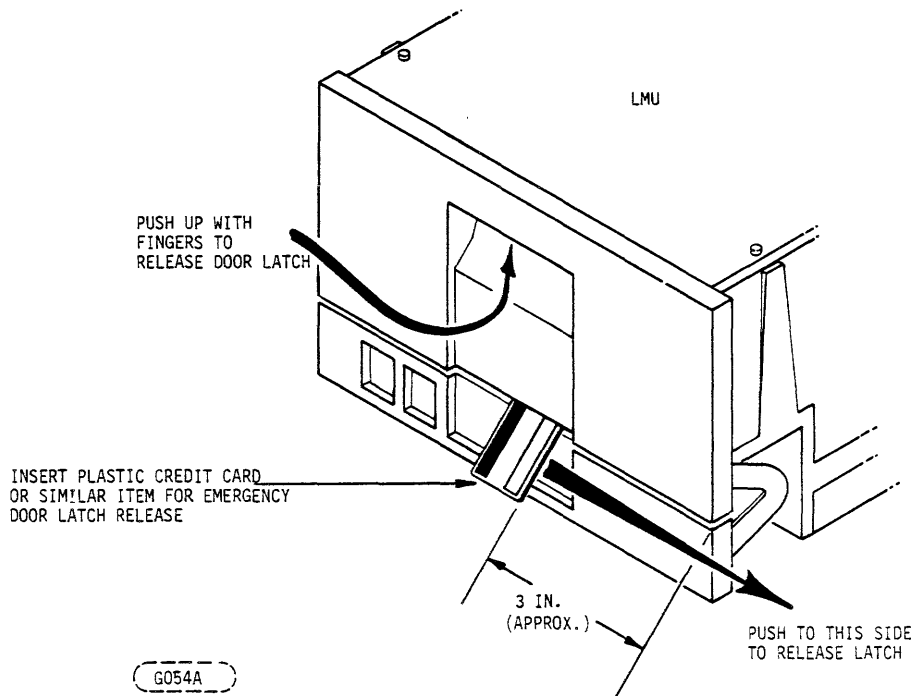


FIGURE 2-4. EMERGENCY/DRIVE FAILURE CARTRIDGE
DOOR OPENING PROCEDURE

2. See Figure 2-4. Insert a plastic credit card or similar object into the space between the access door and the lower front panel. Push the small release tab behind the panel (about 3 inches from the right edge) toward the right with the card and hold while pushing up with the fingers on the door latch release. Pull the door open and remove cartridge. Close front door.

2.9 MAINTENANCE FEATURES

The FAULT indicator blinks when a fault is detected in the drive.

The AC ON/OFF power switch (not on the LMU) when operated applies AC power to the LMU. The LMU fan motor energizes and the front door panel will unlock. This control is not available to the operator.

The LMU requires no electrical/mechanical adjustments or preventive maintenance procedures.

3.1 INTRODUCTION

This section provides the information and procedures necessary to install the LMU.

3.2 UNPACKING

During the unpacking, exercise take care so that tools being used do not cause damage to the unit. As the unit is unpacked, inspect it for possible shipping damage. All claims for this type of damage should be filed promptly with the transporter involved.

Retain the shipping container and packing material if a claim is to be filed for damage, unit is to be reshipped, or shipped to service center.

Unpack the unit as follows:

- a. Remove the tape from the shipping container.
- b. Open the container and remove the LMU assemblies and cables.

CAUTION

Do not release the carriage lock until the LMU is installed in its designated location. Damage may occur as a result of accidental loading of the heads. The carriage is to be locked in the retracted position any time the LMU is to be moved.

- c. Do not connect the input power cable until all other installation steps have been completed and the LMU is ready for initial checkout.
- d. Remove the isolation mounts from the accessory pack in the shipping container. Shown in Figure 3-1 is the location of isolation mounts for a horizontally mounted LMU. Figure 3-2 shows the location of isolation mounts for the vertically mounted LMU. Screw the four isolation mounts into the four 8-32 tapped holes in the base deck.

CAUTION

In handling the LMU care should be taken to not damage the exposed Base PWA in the bottom of the LMU.

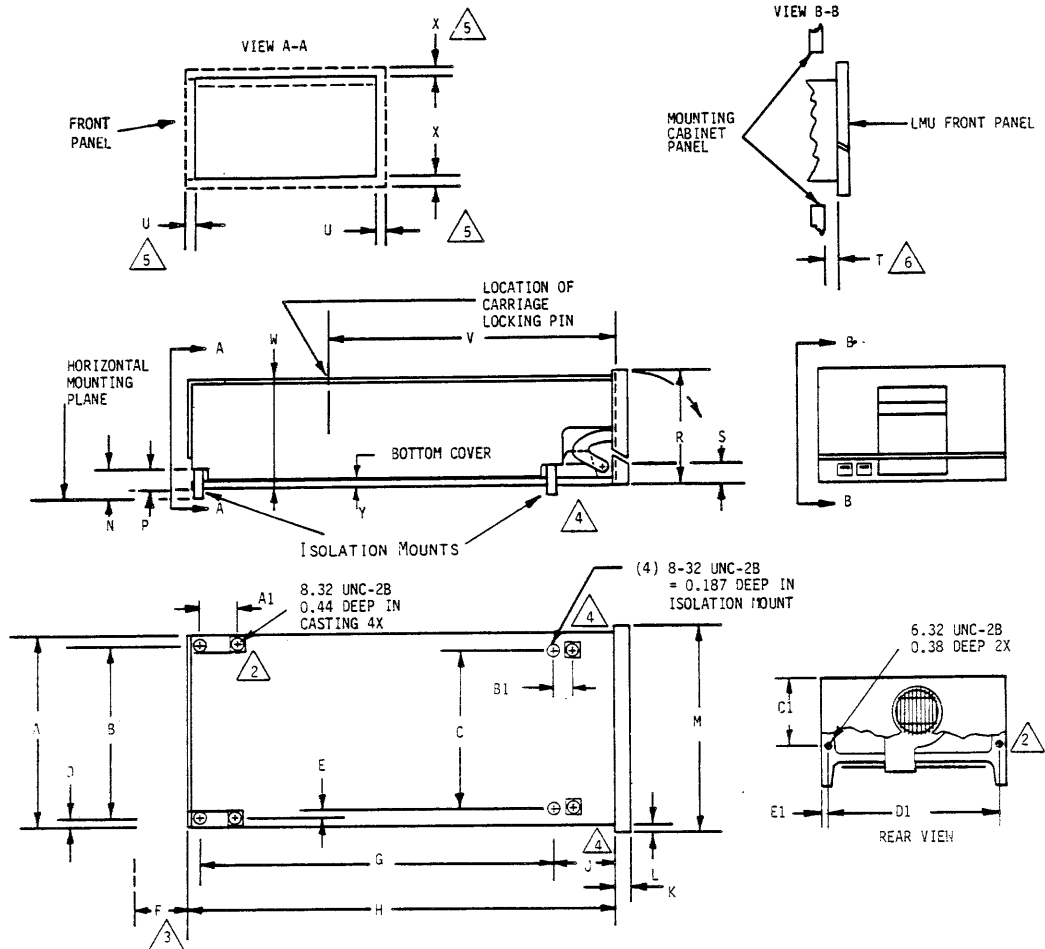
3.3 SPACE ALLOCATION

Figure 1-2 shows the LMU overall dimensions for determining space allocation. Detailed mounting hole data is provided in Figures 3-1 and 3-2. Example configurations are shown in Figure 3-3.

3.4 COOLING REQUIREMENTS

3.4.1 LMU COOLING

A fan draws air in at the rear of the LMU that is used to cool the electronics and PWA's. The air is exhausted on each side of the unit near the front. A minimum of 0.75 inch (19.05 mm) clearance must be provided at the air exits from both vertical and horizontal mountings. The maximum ambient air temperature at the blower inlet is not to exceed 104° F (40° C). The maximum ambient air temperature when measured 1/4 inch (8.4 mm) from the LMU surface shall not exceed 120° F (49° C) excluding hot spots. Positive pressure near the exhaust holes should not exceed 0.06 inches of water (14.9 Pascal).



| DIMENSION | INCHES | MILLIMETERS | REMARKS |
|-----------|--------|-------------|---------|
| * A | 8.58 | 217.9 | |
| B | 8.00 | 203.2 | |
| C | 7.75 | 196.9 | |
| D | 0.28 | 7.1 | |
| E | 0.13 | 3.3 | |
| F | 2.00 | 50.8 | 3 |
| G | 17.55 | 445.8 | |
| * H | 20.36 | 530.4 | REF |
| J | 2.94 | 74.7 | REF |
| K | 0.63 | 15.9 | |
| L | 0.10 | 2.5 | |

| DIMENSION | INCHES | MILLIMETERS | REMARKS |
|-----------|--------|-------------|------------|
| M | 8.78 | 223.0 | |
| N | 0.63 | 15.9 | FREE STATE |
| N | 0.58 | 14.6 | LOADED |
| P | 0.45 | 11.4 | |
| * R | 5.20 | 132.1 | |
| S | 0.53 | 13.5 | |
| T | 0.03 | 0.8 | |
| U | 0.03 | 0.8 | 5 6 |
| V | 12.55 | 318.8 | |
| * W | 5.04 | 128.0 | MAXIMUM |
| X | 0.13 | 3.2 | |
| Y | 0.06 | 1.5 | |

| DIMENSION | INCHES | MILLIMETERS | REMARKS |
|-----------|--------|-------------|---------|
| A1 | 0.95 | 24.1 | |
| B1 | 0.35 | 8.9 | |
| C1 | 3.84 | 97.5 | |
| D1 | 8.0 | 203.2 | |
| E1 | 0.28 | 7.1 | |

NOTES:

1. ALL DIMENSIONS SHOWN ARE NOMINAL UNLESS * THEN MAX.
2. PROVISIONS FOR SHIPPING TIE DOWN.
3. AIR ENTRY AND CABLE CLEARANCE.
4. CLEARANCE OF 0.75 INCHES (19.1 mm) MUST BE PROVIDED AT AIR EXITS.
5. MAINTAIN CLEARANCE BETWEEN LMU AND SURROUNDING STRUCTURE FOR RELATIVE MOTION.
6. MAINTAIN CLEARANCE BETWEEN LMU FRONT PANEL AND FRONT SURFACE OF MOUNTING CABINET PANEL FOR RELATIVE MOTION.

GG039a

FIGURE 3-1. LARK MODULE UNIT MOUNTING HOLE DATA

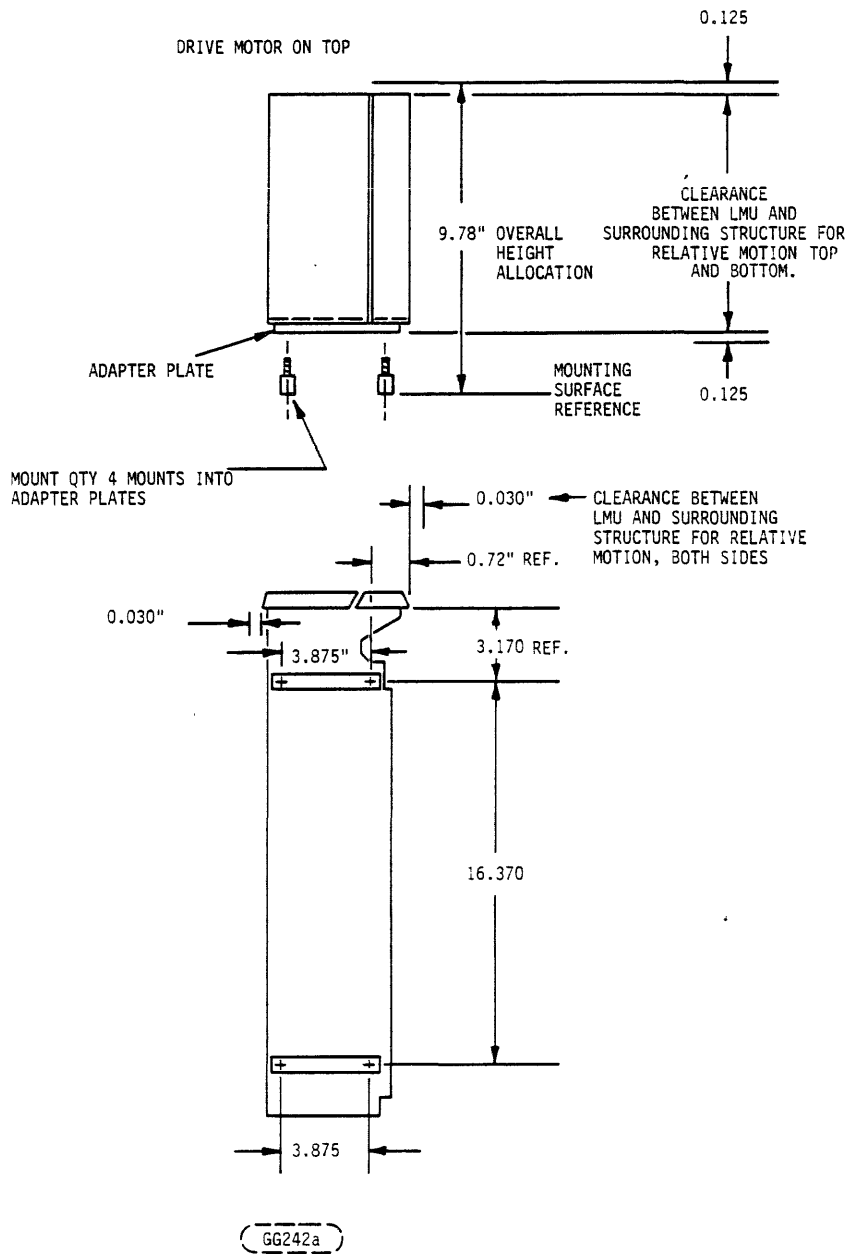
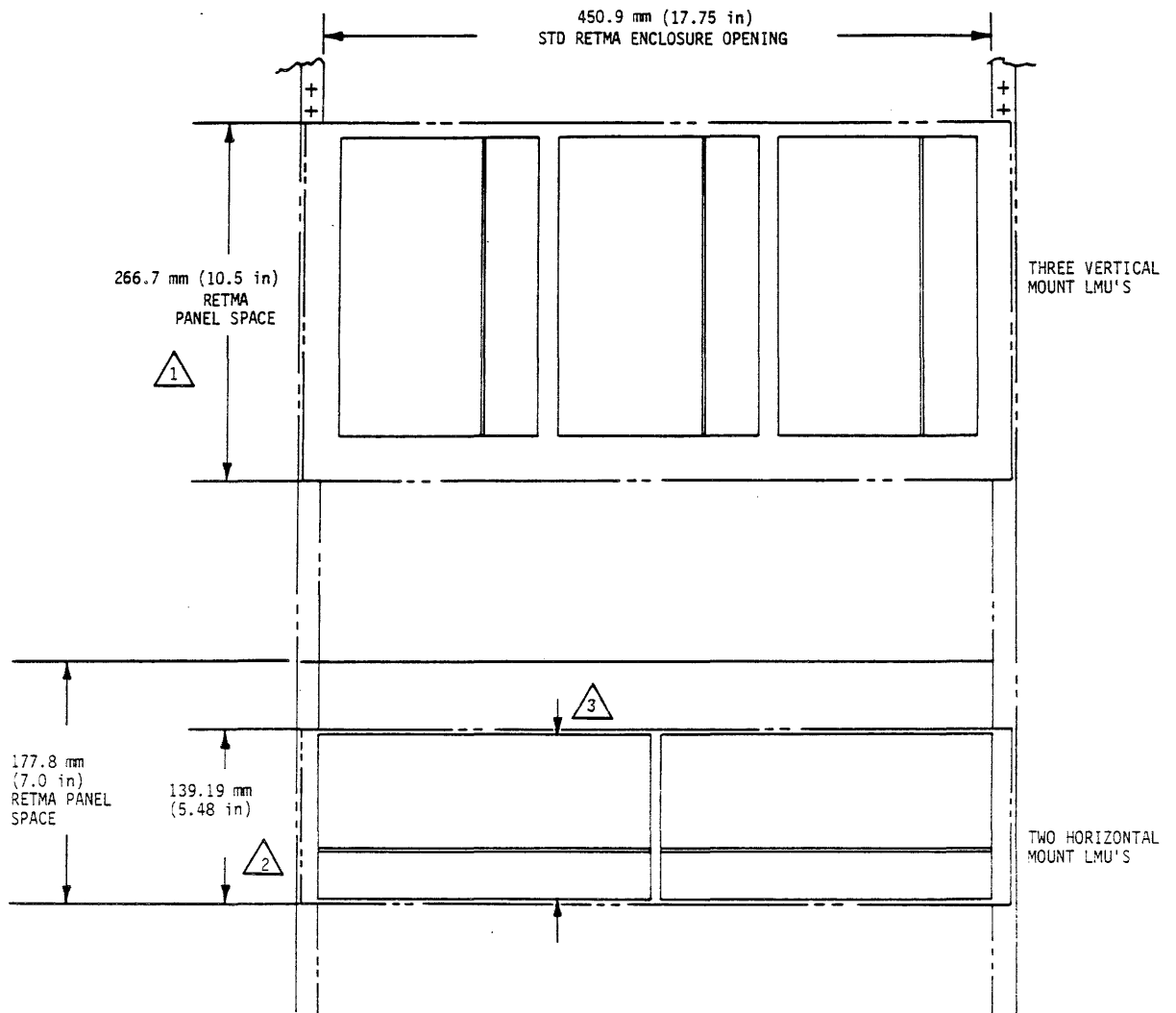


FIGURE 3-2. LMU VERTICAL MOUNTING DIMENSIONS



- 1 DIMENSION INCLUDES SPACE FOR SUPPORT STRUCTURE AND SLIDES.
- 2 DIMENSION INCLUDES SPACE FOR SUPPORT STRUCTURE.
STANDARD RACK REQUIRES MODIFICATION TO UTILIZE SLIDES.
- 3 LMU VERTICAL ENVELOPE 5.48" INCLUDING SHOCK ABSORBERS.

GG180a

FIGURE 3-3. EXAMPLE LMU CONFIGURATIONS

3.5 POWER REQUIREMENTS

3.5.1 PRIMARY POWER REQUIREMENTS

The primary voltage and current requirements are shown in Tables 3-1 and 3-2. The operational line currents are described in Figure 3-4.

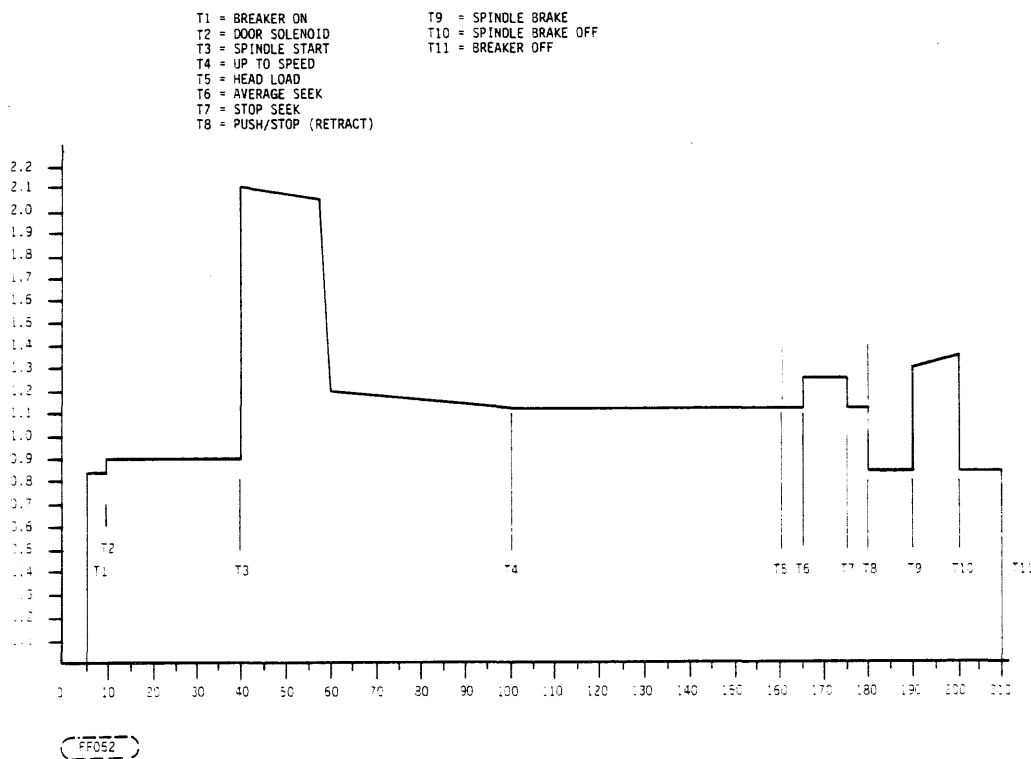


FIGURE 3-4. OPERATIONAL NOMINAL LINE CURRENTS TO POWER SUPPLY VS TIME (120 V INPUT)(WITH CDC POWER SUPPLY)

TABLE 3-1. PRIMARY VOLTAGE REQUIREMENTS

| VOLTAGE (VAC) | TOLERANCE (VAC) | FREQUENCY (Hz) | TOLERANCE (Hz) |
|---------------|-----------------|----------------|----------------|
| 120 | +8, -16 | 60 | +0.6, -1.0 |
| 220* | +15, -29 | 50 | +0.5, -1.0 |
| 230* | +16, -32 | 50 | +0.5, -1.0 |
| 240* | +16, -32 | 50 | +0.5, -1.0 |

*Voltage can be anything in 220-240 volt range, though this table only shows tolerances at three points in the range.

TABLE 3-2. CURRENT/POWER REQUIREMENTS

| DRIVE INPUTS | CURRENTS AND (WATTAGE) | | | | | |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|---------------------|--------------------|---------------------|-------------------|---------|
| | ON TRACK | | SEEKING | | STARTING | |
| | NOMINAL | MAXIMUM | NOMINAL | MAXIMUM | NOMINAL | MAXIMUM |
| 120 VAC | 0.5 A (60 W) | | 0.5 A (60 W) | | 0.85 A (102 W) | |
| 220-240 VAC | 0.35 A (60 W) | | 0.35 A (60 W) | | 0.8 A (190 W) | |
| +16.5 V | 0.4 A (6.6 W) | | 0.72 A (11.9 W) | | - | - |
| -16.5 V | 0.35 A (5.8 W) | | 0.67 A (11.1 W) | | - | - |
| +5 * V | 1.4 A (7.0 W) | 1.8 A (9.0 W) | 1.4 A (7.0 W) | 1.8 A (9.0 W) | - | - |
| -5 V | 2.88 A (14.4 W) | 3.25 A (16.25 W) | 2.88 A (14.4 W) | 3.25 A (16.25 W) | - | - |
| TOTAL WATTAGE | (93.8 W) | | (104.4 W) | | - | - |
| VOLTAGE (V dc) | REGULATION | MAX RIPPLE P/P | CURRENT DRAIN | | | |
| | | | MIN | MAX | | |
| +5* | ±2% | 50 mV | 0.05 A | 1.8 A | | |
| -5.2 | ±2% | 50 mV | 0.07 A | 3.25 A | | |
| +16.5 | ±10% | 500 mV | 0.1 A | 1.3 A | | |
| -16.5 | ±10% | 500 mV | 0.04 A | 1.3 A | | |
| NOTE 1: PEAK CURRENT FOR THE ±16.5 VOLT SUPPLIES MAY REACH 3.0 AMPERES FOR 24 MILLISECONDS DURATION FROM EITHER SUPPLY (NOT BOTH) WITH A 80 MILLISECOND MINIMUM INTERVAL BETWEEN CURRENT PULSES. | | | | | | |
| NOTE 2: THE ±5 VOLTS SHALL SHARE A DC COMMON. THE ±16.5 VOLTS SHALL SHARE A SEPARATE DC COMMON. | | | | | | |
| NOTE 3: IN REGARD TO DC POWER SEQUENCING, THE ±5 V DC SUPPLY MUST NOT PRECEDE THE REMAINING DC VOLTAGES IN EXCESS OF 50 MILLISECONDS. | | | | | | |
| * Includes optional status display requirement of 300 mA nominal and excludes PIO adapter board power requirements. | | | | | | |

3.6 CABLING AND MATING CONNECTORS

3.6.1 GENERAL

The connectors for interfacing LMU command/data signals to the Host Adapter and the DC power are located on the Base PWA at the rear of the unit. (See Figure 3-5). The connector for the AC power is located on the AC Distribution PWA (See Figure 3-6).

3.6.2 COMMAND/DATA INTERFACE CABLING AND CONNECTORS

The Command/Data physical interface consists of a 40-pin command ("C") cable and a 26-pin data ("D") cable. The command cable can be daisy-chained. However, since there is only one command I/O connector provided on the LMU Base PWA, the user must provide the daisy-chain facilities. A maximum of four LMU's can be daisy-chained. The data cable must be radially connected. The maximum cumulative daisy-chained cable length is 10 feet. The maximum radial cable length is 10 feet. Refer to Figure 3-7.

Figure 3-8 illustrates the type of connector used on the Base PWA and the cable connector required to mate with it. Section 3-10 lists the recommended components that can be used to interconnect the drive(s) to the user adapter. The connector pin and signal name assignments are shown in Figures 3-9 and 3-10. Timing and electronic information about the interface command/data signals is given in more detail in Volume II of the LMU Manual (P/N 77711050), Section 5.6.

3.6.3 AC AND DC POWER CABLING AND CONNECTORS

The AC power input connector is mounted on the AC Distribution PWA. It is a three circuit position Mate 'N' Lock Type female housing with male contacts. The DC power connector is an 8 circuit position male header mounted on the Base PWA. Locations of the above connectors are shown in Figure 3-6. Recommended mating connectors for the AC and DC power input cables are given in Section 3-10 "ACCESSORIES".

3.6.4 I/O AND POWER CABLE ROUTING

For sliding rack mounted drives, it is recommended that a cable retract mechanism be incorporated in the rack design. Retract mechanisms can be purchased from a number of available manufacturers.

3.7 GROUNDING

In order to ensure reliable interface operation and prevent damage to drivers or receivers, a DC ground should exist between the drive and the adapter. This ground should be carefully incorporated into the overall grounding system to prevent circulating ground currents. The ground connection, while necessary, is not within the scope of this manual. Figure 3-6 shows the location of the LMU system ground tie point.

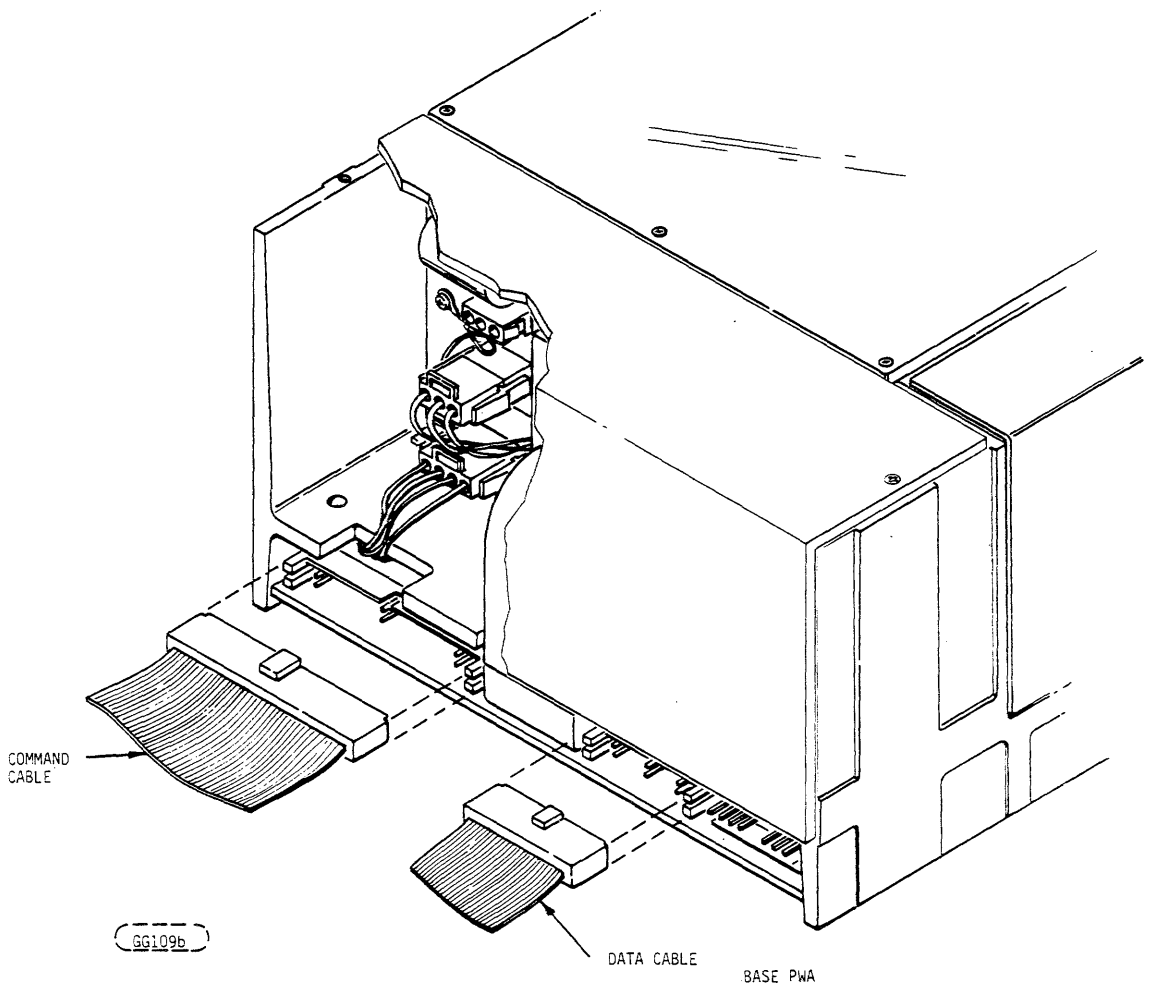


FIGURE 3-5. COMMAND/DATA CABLE CONNECTIONS

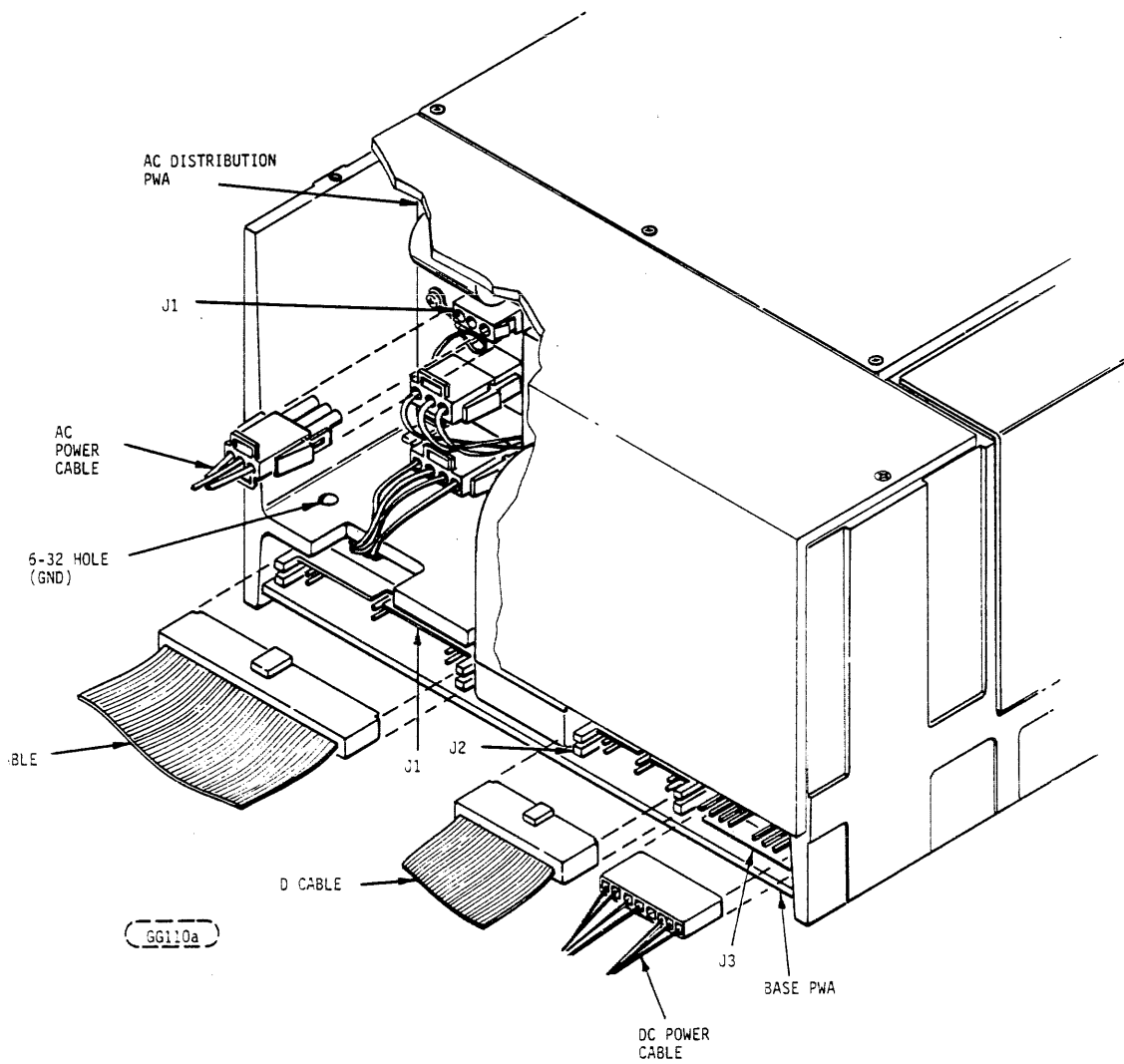
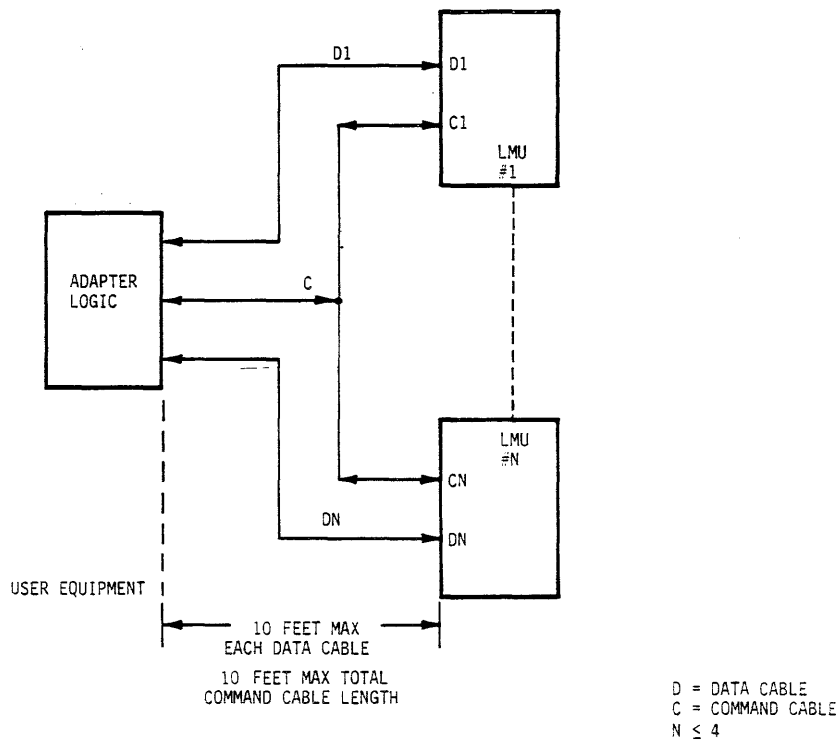
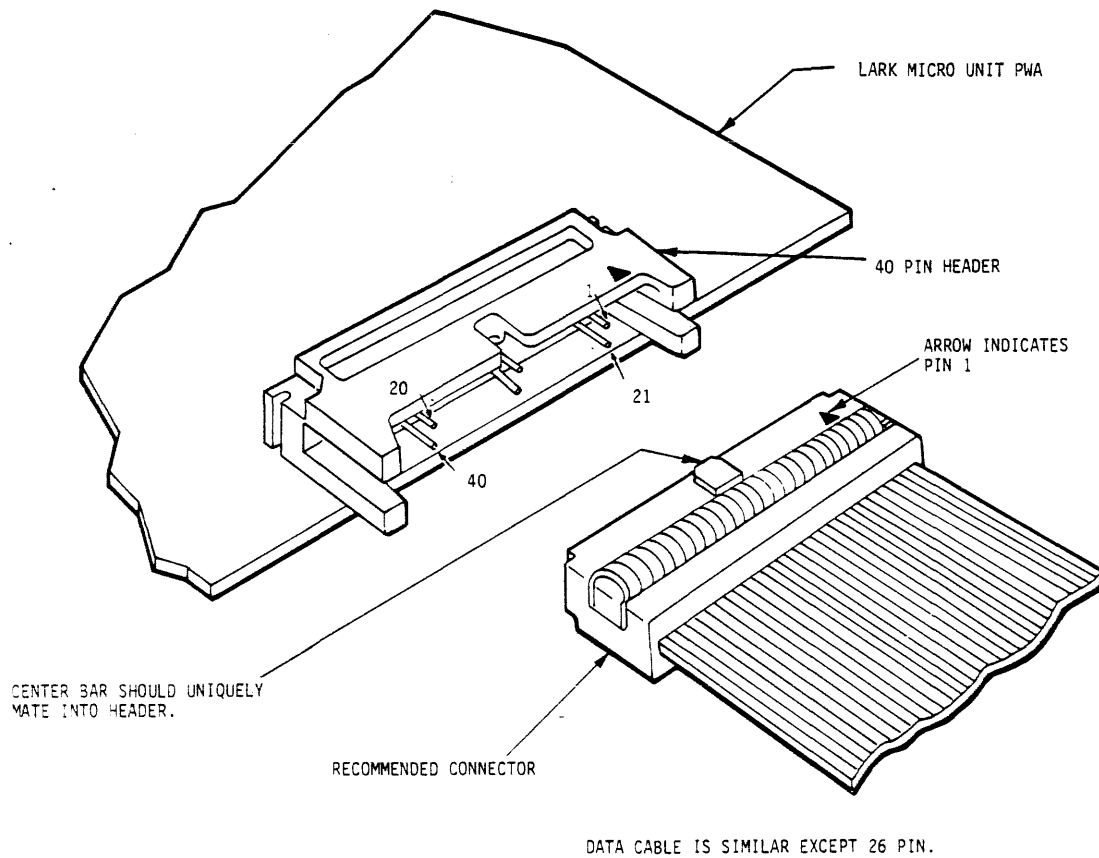


FIGURE 3-6. AC AND DC CABLING



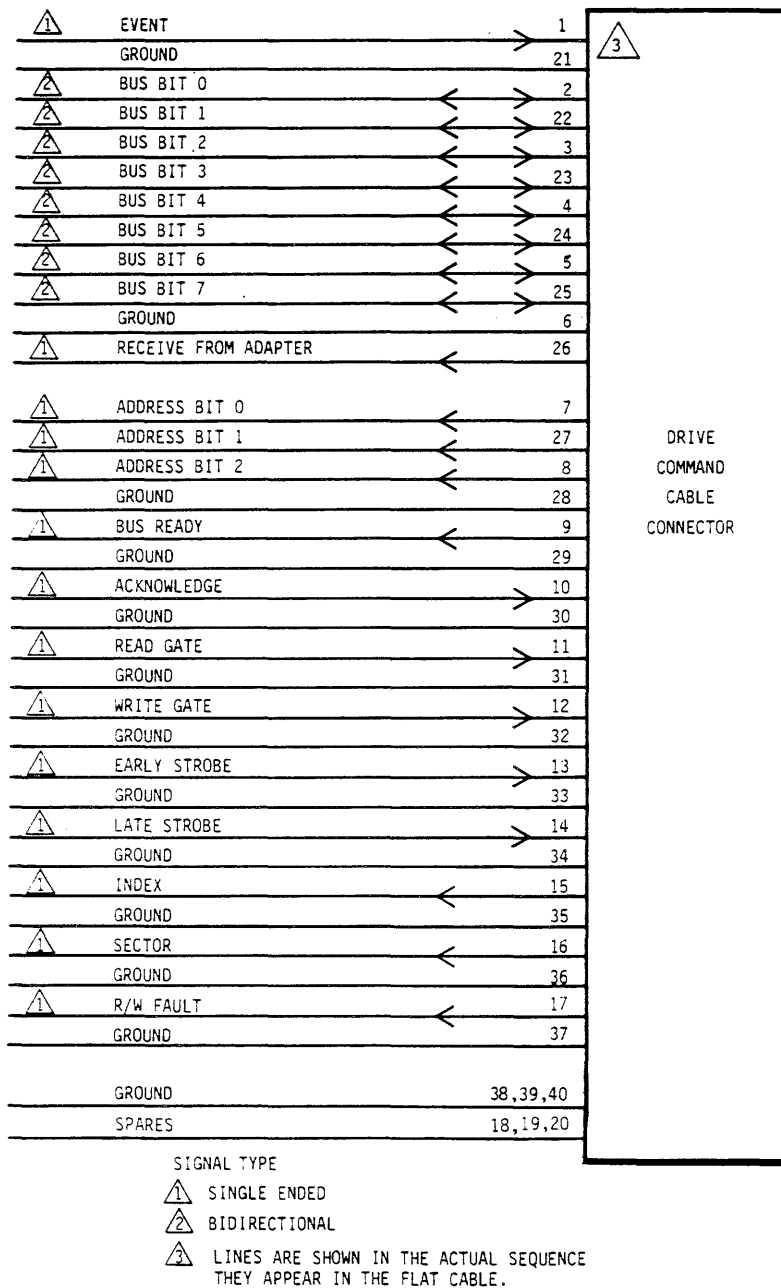
(Z172a)

FIGURE 3-7. LARK MICRO INTERFACE CABLING



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FIGURE 3-8. PICTORIAL REPRESENTATION OF COMMAND CABLE AND CONNECTOR



G260a

FIGURE 3-9. COMMAND CABLE PIN ASSIGNMENTS

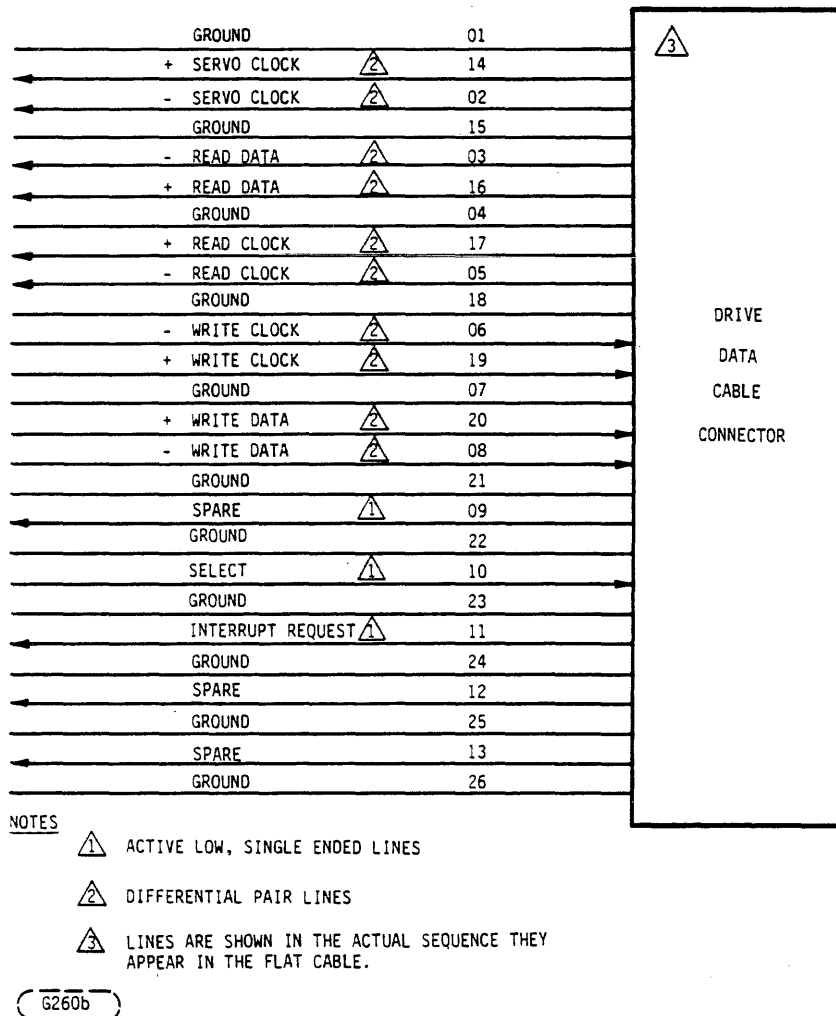


FIGURE 3-10. DATA CABLE CONNECTOR ASSIGNMENTS

3.8 ENVIRONMENT

Temperature

a. Operating

50° F (10.0 ° C) to 104° F (40° C) with a maximum gradient of 18° F (10° C) per hour. Maximum operating temperature should be reduced as a function of altitude by 1.95° F/1000 ft. (-15.5° C/304.8 m).

b. Transit Temperatures

-40° F (-40.4° C) to 140° F (60.0° C) with a maximum gradient of 36° F (20° C) per hour. This specification assumes that the LMU is packaged in the shipping container designed by manufacturer for use with the LMU.

c. Storage Temperature

14° F (-10° C) to 122° F (50.0° C) with a maximum gradient of 27° F (15° C) per hour.

If it becomes necessary to use an LMU cartridge which has not been allowed to stabilize at the ambient drive operating room temperature for at least one hour or if the cartridge was exposed to temperatures below 61° F (16° C) immediately prior to the stabilization period, then the following procedures must be employed:

1. The cartridge must be visually inspected or examined to ensure that condensation is not present on any part of the cartridge.
2. The cartridge must be allowed to spin on the LMU for a period of not less than five minutes prior to attempting to read or write on the cartridge.

Relative Humidity

a. Operating

20% to 80% RH (providing there is no condensation) with a maximum gradient of 10% per hour.

Transit (as packed for shipment)

5% to 95% (providing there is no condensation).

b. Storage

10% to 90% (providing there is no condensation).

c. Altitude (actual or effective)

1. Operating

983 ft. (300 m) below sea level to 6560 ft. (2000 m) above sea level.

2. Transit (as packed for shipment)

983 ft. (300 m) below sea level to 8200 ft. (2500 m) above sea level.

3.9 INITIAL CHECKOUT AND STARTUP PROCEDURE

This procedure should be used to make the first power application to the unit. The procedure assumes that the preceding procedures and requirements of this section have been performed.

1. Insure system AC power circuit breaker is OFF.
2. Insure Subsystem Power Supply power switch is positioned to OFF.
3. Verify START/STOP switch is in STOP (out) position.

4. Unscrew carriage locking pin (CCW direction) until head of screw is flush with top of cover (see Figure 3-11). Resistance to turning will be felt as locking pin nears the correct position.

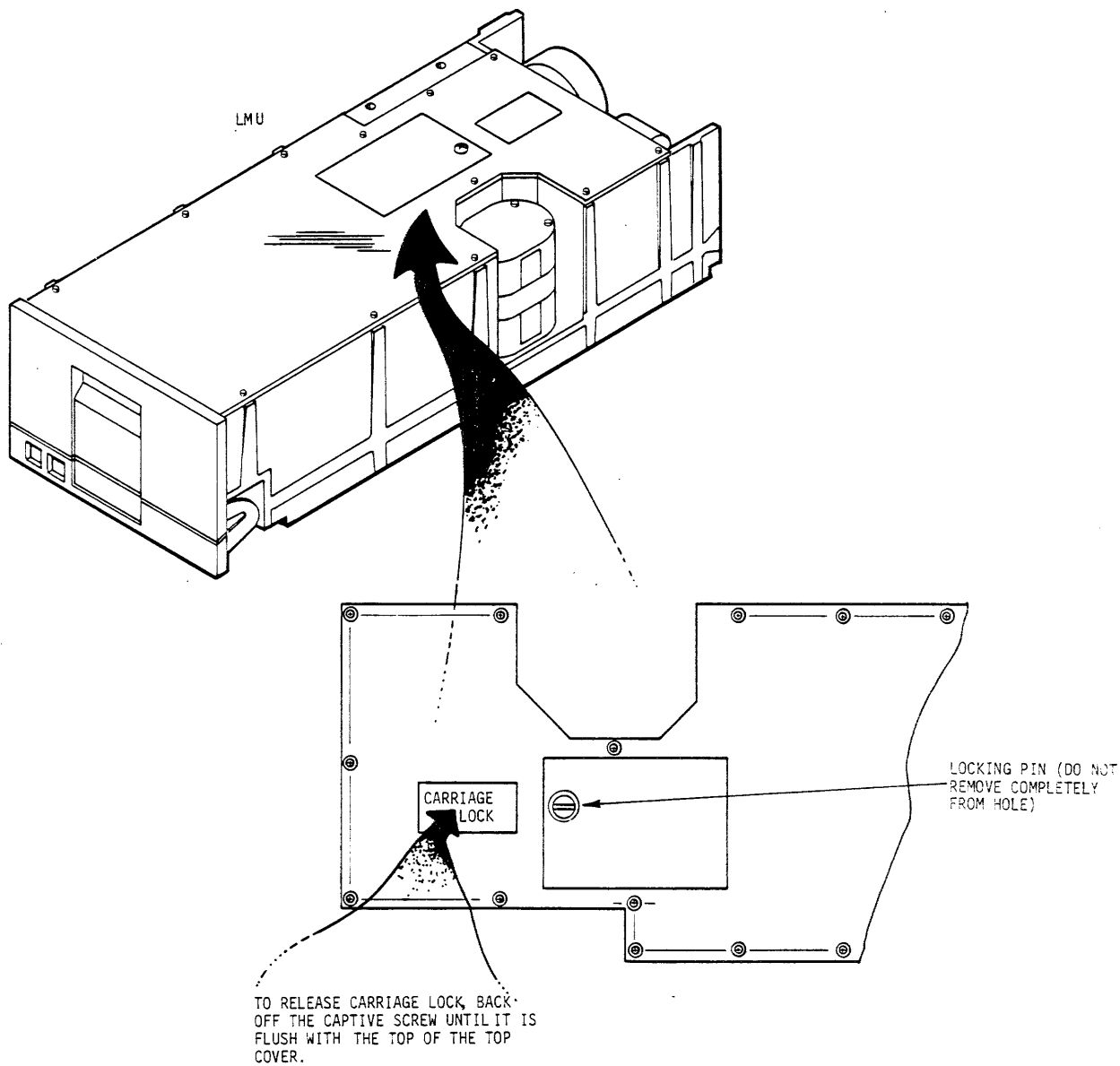
CAUTION

Do not remove the carriage locking pin at any time. The air system seal integrity requires that this screw remain in the top cover at all times.

CAUTION

The carriage is to be locked during shipping using the carriage locking pin (Figure 3-11). This prevents damage to the drive as a result of the heads loading.

5. Install the AC power cable between power source and drive.
6. Turn on Subsystem AC power circuit breaker.
7. Turn Subsystem power switch to ON. (If applicable to subsystem.) The LMU cooling fan should operate and front panel door should unlock when START/STOP switch is in STOP position (out).
8. Verify proper disk cartridge is available and insert into LMU.
9. Operate START/STOP switch to START (in). Spindle motor should rotate. Head loading sequence is initiated, START/STOP indicator blinks until heads are loaded then, remains illuminated. Also, front panel door locks when spindle rotation begins.
10. Perform on-line diagnostics, as applicable.



G054b

FIGURE 3-11. CARRIAGE LOCKING PIN

3.10 ACCESSORIES

Accessory items required, but not furnished with the drive, are the cables described in this section.

3.10.1 I/O CABLE CHARACTERISTICS AND CONNECTOR PART NUMBERS

All critical read/write signals are implemented using balanced, terminated differential pair lines across a flat cable. All other signals are implemented using single-ended, LS TTL compatible lines. Signal lines are separated by ground lines

to reduce crosstalk. (Refer to Figures 3-9 and 3-10 for pin assignments). These ground lines must be grounded both at the adapter and the drive(s). Polarized connectors should be used on all cables to prevent reversal of ground and signal lines. (Refer to Figure 3-8.) Further component details are given in Table 3-3. Grounding is discussed in Section 3-7.

3.10.1.1 I/O CABLE AND CONNECTOR PART NUMBERS

TABLE 3-3. I/O CABLE AND CONNECTOR PART NUMBERS

| ITEM NO. | DESCRIPTION | CDC PART NUMBER | VENDOR PART NUMBER |
|----------|--------------------------------------|-----------------|-----------------------|
| 1 | Connector (40 conductor) | 92014152-0/54-6 | Berg 65948-440/640 |
| 2 | Connector (40 conductor daisy chain) | 92014153-8/55-3 | Berg 65948-540/740 |
| 3 | Connector (26 conductor) | 92014136-3/38-9 | Berg 65948-426/626 |
| 4 | Right angle header (40 conductor) | 51847515 | Berg 65496-025 |
| 5 | Right angle header (26 conductor) | 51847513 | Berg 65496-013 |
| 6 | Vertical header (40 conductor) | 95433303 | AMP 102154-9 |
| 7 | Vertical header (26 conductor) | 95433301 | AMP 102154-6 |
| 8 | Cable (40 conductor) | 65832230 | 3M 3365-40 |
| 9 | Cable (26 conductor) | 75884912-9 | 3M 3476-26 |
| 10 | Shielded cable (40 conductor) | TBS | TBS |
| 11 | Shielded cable (26 conductor) | TBS | TBS |

Items 1 and 3 are closed-end cover connectors to be used at the end of cables to prevent the cable from shorting with drive board runs. Item 2 is an open-end cover connector which can be used for daisy chaining. Items 8 through 11 are part numbers for the cables described.

3.10.1.2 I/O CABLE CHARACTERISTICS

The cables described in this section may be used when cables are carefully routed and remain inside an RFI shielded enclosure. The shielded cables described in this section must be used to prevent RFI leakage where cables are used outside a shielded enclosure. The shield should be terminated to the outside skin of the enclosure.

Command Cable Characteristics

| | |
|---------------|-----------------------------------------------|
| Type: | 40 wire flat cable (not twisted) |
| Wire Size: | 28 AWG, 7 strand |
| Voltage: | 300 V (maximum) |
| Length: | 10 feet (maximum) [including all daisy chain] |
| Impedance: | 100 Ohms |
| Wire Spacing: | 0.050 inch |

Data Cable Characteristics

| | |
|---------------|-----------------------------------------------------|
| Type: | 26 wire flat cable with ground plane and drain wire |
| Wire Size: | 28 AWG, 7 strand |
| Voltage: | 300 V (maximum) |
| Length: | 10 feet (maximum) |
| Impedance: | 65 Ohms |
| Wire Spacing: | 0.050 inch |

Shielded Command and Data Cable Characteristics

| | |
|---------------|-----------------------------------------------|
| Type: | 40/26 wire flat cables with shield and jacket |
| Wire Size : | 28 AWG, 7 strand |
| Voltage: | 300 V (maximum) |
| Length: | 10 feet (maximum) |
| Impedance: | TBD |
| Wire Spacing: | 0.050 inch |

3.10.2 AC AND DC POWER CONNECTOR PART NUMBERS

Connectors required to supply power to the LMU are described in this section. These or equivalents are to be supplied by the user. Table 3-4 lists the part numbers of acceptable connectors and Table 3-5 lists the pin assignments for the AC and DC power connectors.

TABLE 3-4. AC AND DC POWER CONNECTORS

| ITEM NO. | DESCRIPTION | CDC PART NO. | VENDOR PART NO. |
|---------------------------------------|---------------------------------------------------------------------------------|--------------|-----------------------------------|
| <u>AC POWER CONNECTOR</u> | | | |
| 1 | 3 CIRCUIT POSITION MAT 'N' LOCK TYPE MALE HOUSING WITH FEMALE CONTACTS | 83435302-1 | AMP 1-480700-0 |
| 2 | CONTACT (3 REQ) | 83435507-5 | AMP 350536-1 or 350550-1 |
| <u>DC POWER CONNECTOR</u> | | | |
| 1* | 8 CIRCUIT POSITION FEMALE CONNECTOR WITH HIGH PRESSURE CONTACTS | 10128944 | AMP 640431-8 |
| 2 | KEYING PLUG FOR ABOVE | 10128937-9 | AMP 640629-1 |
| * KEYING PLUG IN #5 CIRCUIT POSITION. | | | |

TABLE 3-5. AC/DC PIN ASSIGNMENTS

| AC CONNECTOR | |
|--------------|---------------|
| PIN | SIGNAL |
| 1 | AC RETURN |
| 2 | SAFETY GROUND |
| 3 | AC LINE |

| DC CONNECTOR | |
|--------------|---------|
| PIN | SIGNAL |
| 1 | +16.5 V |
| 2 | +5 V |
| 3 | GROUND |
| 4 | GROUND |
| 5 | KEY |
| 6 | -5 V |
| 7 | -5 V |
| 8 | -16.5 V |

4.1 INTRODUCTION

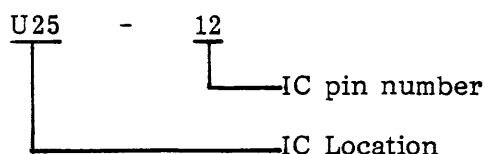
The theory of operation for the Lark Micro Unit (LMU) (BJ7D3-A) is divided into two parts: the mechanical and electrical descriptions. The theory of operation contained herein contains only that information deemed necessary for a general understanding of the LMU and to aid in the repair of the LMU assemblies outside the sealed area.

General Electronics Information:

Logic signal names are followed by the symbol +L or -L indicating that the active (logic "1") level of the signal is high (+4 Volts for TTL and -0.8 Volts for ECL) or low (nominal 0 Volts for TTL and -1.7 Volts for ECL) respectively. For example, the signal SEQ-END-INT/+L indicates the signal is at a nominal +4 Volt level when active (logic "1"). ECL signals are usually indicated as active high by a -P and an active low by a -N suffix.

Figure 4-1 shows a general block diagram of the LMU. As the theory of operation proceeds the block diagram will be repeated with the area to be described being outlined with thicker than normal lines.

Integrated circuit components are designated as follows:



Functional descriptions are frequently accomplished by simplified diagrams for instructional purposes and as an aid in troubleshooting. The diagrams have been simplified to illustrate the principles of operation: Therefore, some elements are omitted. The logic diagrams in Section 5 of this manual should take precedence over the diagrams in this section whenever there is a conflict between the two types of diagrams.

The theory describes typical operations and does not list variations or unusual conditions resulting from unique system hardware or software environments. Personnel using this manual should already be familiar with principles of operation of the computer system, the controller, programming considerations (including the correct sequencing of I/O commands and signals), and track format (i.e., data records and field operation). I/O theory of operation is described in Section 5.6.

All references to "MC" refer to the microcomputer used in the drive to control seeks, spindle power, front panel operations, data protection and information transfers on the interface.

4.2 ASSEMBLIES

Figure 4-2 illustrates the physical placement of the various major assemblies of the LMU. Figure 4-1 illustrates the functional relationships of these assemblies. The following paragraphs describe the operation of these assemblies.

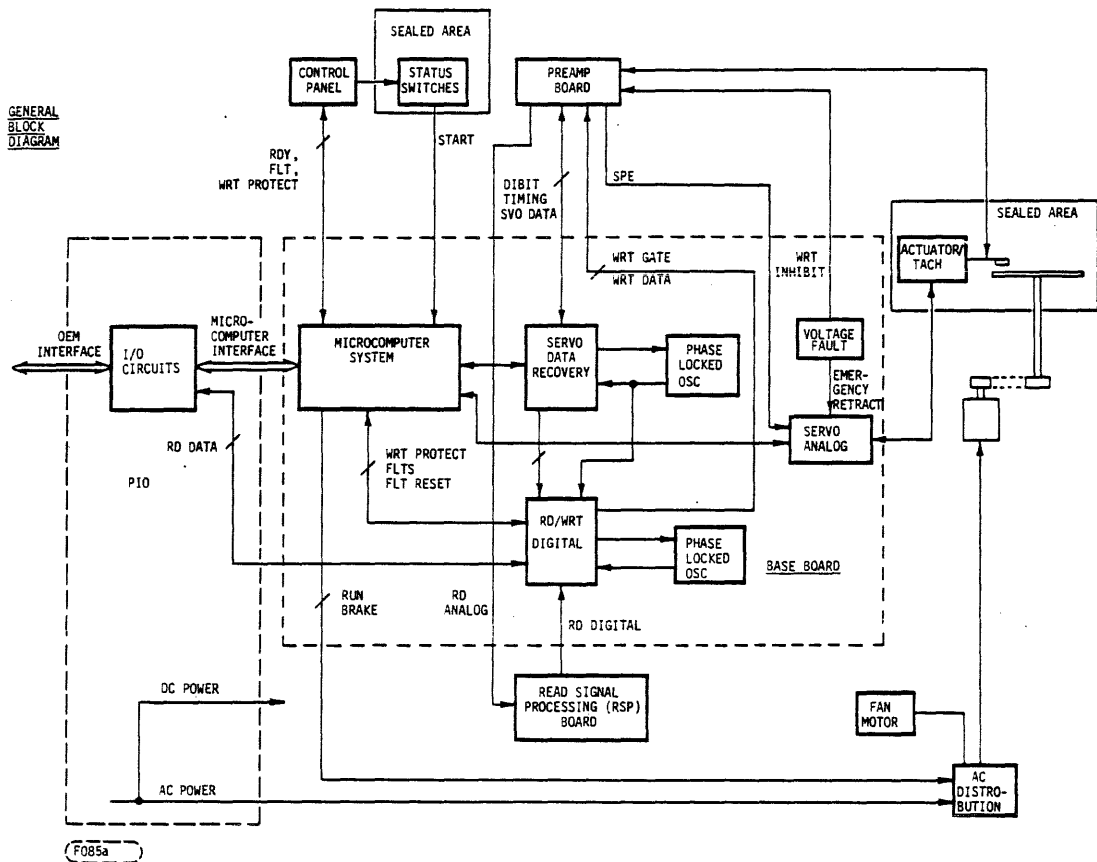


FIGURE 4-1. GENERAL BLOCK DIAGRAM OF LMU
MECHANICAL/ELECTROMECHANICAL ASSEMBLIES

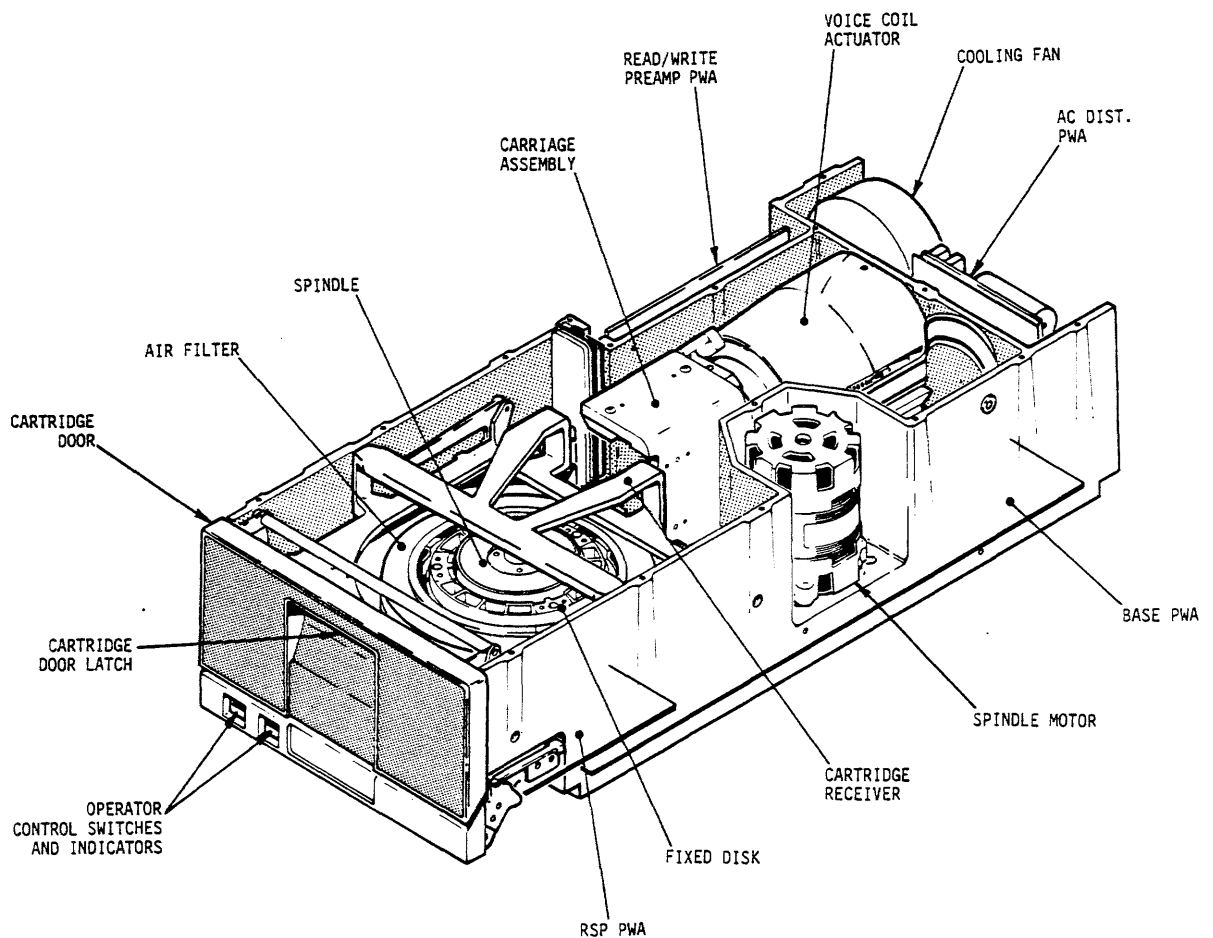
4.2.1

Some of the assemblies described in the following paragraphs cannot be repaired except at factory level depots. These assemblies will be pointed out. Theory of operation is provided on these assemblies in order that a more complete theory of operation of the LMU can be available.

4.2.1.1 SPINDLE DRIVE MOTOR ASSEMBLY

The drive motor drives the spindle assembly. The motor is a 1/50 hp unit of the induction type. The motor is secured directly to the base casting using insulating hardware so that AC current from the motor does not circulate in the base deck. Power is transferred to the spindle via a smooth-surfaced "vee" belt that threads over the pulleys of the spindle and drive motor. Proper belt tension is maintained by use of motor positioning. The motor is connected to chassis ground at the AC Distribution PWA via a wire in the motor power harness.

The temperature of the drive motor is monitored by an internal thermal overload switch. If the switch opens, power is removed from the motor. The loss of spindle speed causes the MC to retract the heads and initiate the STOP routine. The drive motor thermal overload switch closes again when the temperature drops to a safe level. If the fault has been manually reset, the MC initiates the START routine which operates relay K1 and connects power to the motor again.



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FIGURE 4-2. LMU MAJOR ASSEMBLIES

4.2.1.2 SPINDLE ASSEMBLY

The spindle assembly is the physical interface between drive motor and disks. The surface of the spindle magnetic mounting plate mates directly with the steel plate on the bottom of the disk cartridge, and spindle hub is counter-sunk in the center to accept a steel alignment ball in the center of the bottom of the disk cartridge (used for cartridge centering).

The spindle is driven by a "vee" belt linking the spindle drive pulley to the drive motor pulley. Spindle speed is 3510 +3.0%, -4.8% r/min. See Section 6.4.2.5 for belt tensioning requirements.

A ground spring is mounted at the lower end of the spindle assembly. The ground spring is mounted so that it is always in contact with the shaft to bleed off any accumulation of static electricity on the spindle through a ground strap. Mounted on the bottom of the spindle is a disk with 16 slots in its periphery. The disk periphery passes through a slot in the Spin Speed Sensor which puts out a pulse every time one of the 16 slots passes through the Spin Speed Sensor slot. See Paragraph 4.2.1.5 for additional Spin Speed Sensor details.

Removal and replacement of the spindle assembly is a depot level procedure ONLY.

4.2.1.3 COOLING/PURGING AIR CIRCULATION SYSTEMS

A blower at the rear of the Micro-Unit provides cooling air for the printed circuit boards. The blower does not provide air into the sealed area of the drive, but rather, the motion of the disks circulates the air in the sealed area through a filter that is mounted between the disk cartridge and the fixed disk area. When the cartridge is in place, the bottom of the cartridge is pushed up to allow air from the filter to pass into the area around the disk in the cartridge. The air passes out through the head entry hole and around through the filter again. Air passing through the filter also purges the fixed disk area. See Figure 4-2 and Figure 4-3.

Removal and replacement of the filter between the fixed disk and the cartridge area is a depot level procedure ONLY.

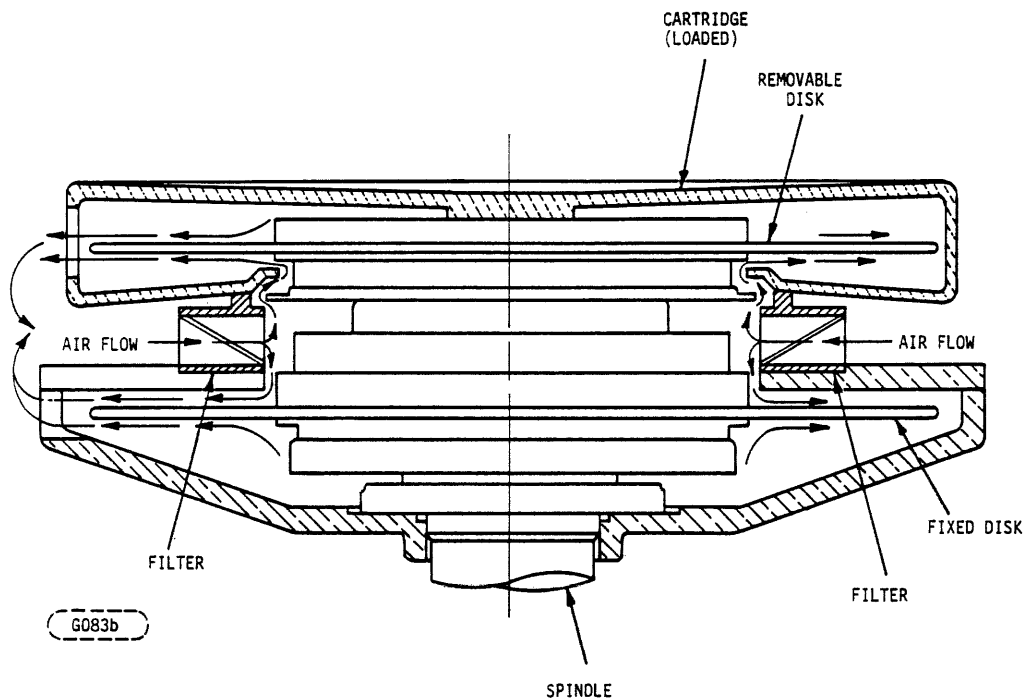


FIGURE 4-3. CROSS SECTION OF AIR CIRCULATION

4.2.1.4 ACTUATOR

The actuator consists of the coil and carriage, rail bracket assembly, and magnet assembly (Figure 4-4). The actuator is the device that supports and moves the read/write and track servo heads (Figure 4-5). The forward and reverse motions of the carriage on the carriage track are controlled by a servo signal. The velocity signal is generated by the microcomputer on the Base PWA and processed by a power amplifying stage.

The power amplifier output is applied to the voice coil positioner (part of carriage) creating a magnetic field about the voice coil positioner. This magnetic field reacts with the permanent magnetic field existing in the air gap of the magnet assembly. The reaction either draws the voice coil into the permanent magnet field or forces it out. Signal polarity determines the direction of motion, and signal amplitude controls the acceleration of the motion.

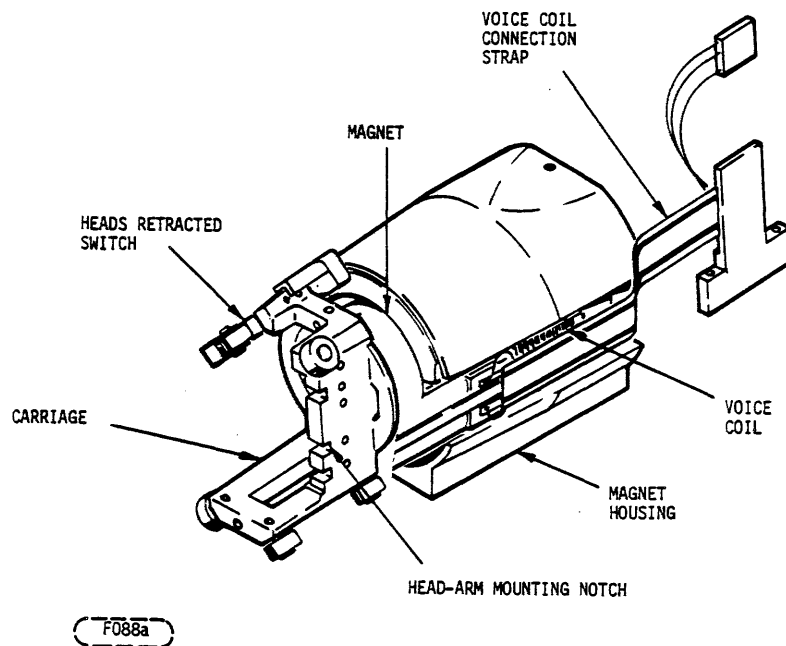


FIGURE 4-4. ACTUATOR ASSEMBLY

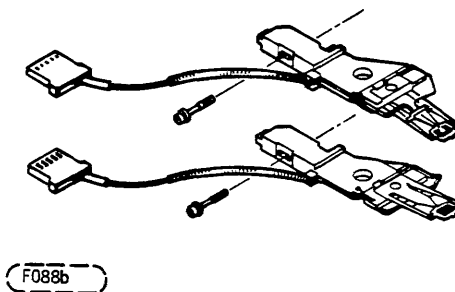


FIGURE 4-5. HEAD-ARM ASSEMBLIES (UPPER AND LOWER)

The voice coil positioner is a mandril-wound coil that is free to slide in and out of the gap section forward face of the magnet assembly. Fastened to the positioner is a head/arm receiver which holds the read/write heads. The head/arm receiver mounts on the coil and carriage assembly that moves along the carriage rail on antifriction bearings. Movement of the positioner in or out of the magnet causes the same motion to be imparted to the entire carriage assembly. This linear motion is the basis for positioning the read/write heads to a particular track of data on a disk. (Refer to Head Loading paragraph for detailed information on read/write head loading and unloading.)

The positioning signal is applied to the voice coil positioner via two flexible, insulated, metal straps, the ends of which are secured to the carriage and bearing assembly. There is a third metal strap which grounds the carriage to the base deck assembly.

During any seek operation, an I/O command gives the microcomputer the cylinder address to be accessed. The microcomputer compares this cylinder address with the current cylinder address which is stored within the MC memory and then issues a command to the positioner to move toward the new cylinder location with an acceleration and velocity that is proportional to the difference in position. The positioner moves in the direction of the new cylinder address under control of a velocity feedback loop, with the velocity signal being supplied by a velocity transducer.

The velocity transducer (Figure 4-7) is a two-piece device, (one piece stationary and the other movable.) Refer to the Transducer paragraph for a complete description.

The actuator contains stop mechanisms to limit extremes in forward and reverse movement. The forward stop assembly consists of a rubber bumper located at the front of the rail bracket. If the carriage moves too far toward the disks, the forward bumper contacts the front of the carriage. If the carriage is retracted far enough away from the disks the rear of the head/arm receiver contacts two rear bumpers which protrude out of the front face of the magnet assembly.

Removal and replacement of the actuator assembly is a depot level maintenance procedure ONLY.

HEAD LOADING

The read/write heads must be loaded on the disk surfaces before exchanging data with the controller. The heads must be removed (unloaded) from this position and driven clear of the disks either when power is removed from the unit or when the disk velocity falls below speed tolerance range.

Heads are loaded by moving the aerodynamically shaped head face toward the related disk surface. When the cushion of air that exists on the surface of the spinning disk is encountered, it resists any further approach by the head. Head load spring pressure is designed to just equal the opposing cushion pressure (function of disk r/min) at the required height. As a result, the head flies.

To prevent damage to the heads and/or the disks during operation, loading occurs at controlled velocity only after the disks are up to speed and the heads are over the disk surfaces. For the same reason, the heads unload automatically and are retracted at a controlled velocity if the disk r/min drops out of tolerance. Heads should never be loaded on a disk that is not rotating. Head loading is a part of the Start Load function. Pressing the START switch initiates disk rotation and purge.

After the purge, the spindle speed must be within tolerance. If so, the micro-computer specifies a load command and the carriage moves forward toward track 0. Heading loading occurs during this forward motion. The carriage continues to move toward the spindle until the servo detects track 0.

The actuator velocity is calibrated after heads are loaded. A long seek at approximately 8 inches per second is commanded from track 0 to an inner track. The elapsed time at constant velocity is measured between the detection of tracks 46 and 589, and then compared to a predetermined duration.

The velocity amplifier (U58) gain is decreased, if required, by an approximate 3 per cent increment after each seek. The resulting velocity increases until the proper time duration is compared and the gain setting is stored in memory. Sixteen amplifier gain values can be set. A status code is stored when a valid seek time cannot be determined.

PROTECT DATA QUALITY TEST FOR THE CARTRIDGE (Refer to Figures 4-6 and 4-7)

When the velocity calibration is complete, the Lark will automatically perform sequential forward seeks to all even tracks then sequential reverse seeks to all odd tracks. This is performed on both surfaces of the cartridge. The automatic gain control for the servo system is disabled just before each seek so that the servo data detector is unable to follow changes in servo data amplitudes during seeking and settling. Thus, the drive will be unable to recover valid servo data for tracks with abnormally low amplitude that are encountered before the AGC system is re-enabled. In order to make this test more stringent, servo data detection is shifted from a 50% to a higher level of its peak value. This is done only while settling on the new track. Most of this is done in the preamp AGC, preamp servo data detection circuits and the microprocessor. See Section 2.5 for definitions of faults, fault recovery, PDQ status codes, etc.

HEAD UNLOADING

Head unloading occurs whenever power to the unit is removed, the STOP switch is placed in STOP position, a voltage fault occurs, or disk r/min drops below tolerance. Signals from the microcomputer cause the voice coil to drive the carriage in reverse from its current location toward the retracted stop. (Either normal or emergency methods can be used. Refer to Stop Sequence paragraph for additional information.) As the carriage retracts, the cam surface encounters the head load springs and each head rides vertically away from the related disk surface. The carriage continues back to the retracted position and stops.



HEAD/ARM ASSEMBLIES

Four head/arm assemblies are mounted on the carriage (Figure 4-5). A read/write head assembly is mounted at the end of a supporting arm structure.

The head assembly, which includes a cable and plug, is mounted on a gimbal spring which, in turn, is mounted on a head load spring. This method of mounting allows the head assembly to pivot (independent of the arm) tangentially and radially relative to a data track on the disk surface. Such motion is required to compensate for possible irregularities in the disk surface.

The arm structure consists of a floating arm secured to a heavier fixed arm. The end of the fixed arm opposite the head mounts in the carriage receiver. The floating arm is mounting point for the head and is necessarily flexible so that it can flex during load and unload motions, onto and off of the cam surfaces.

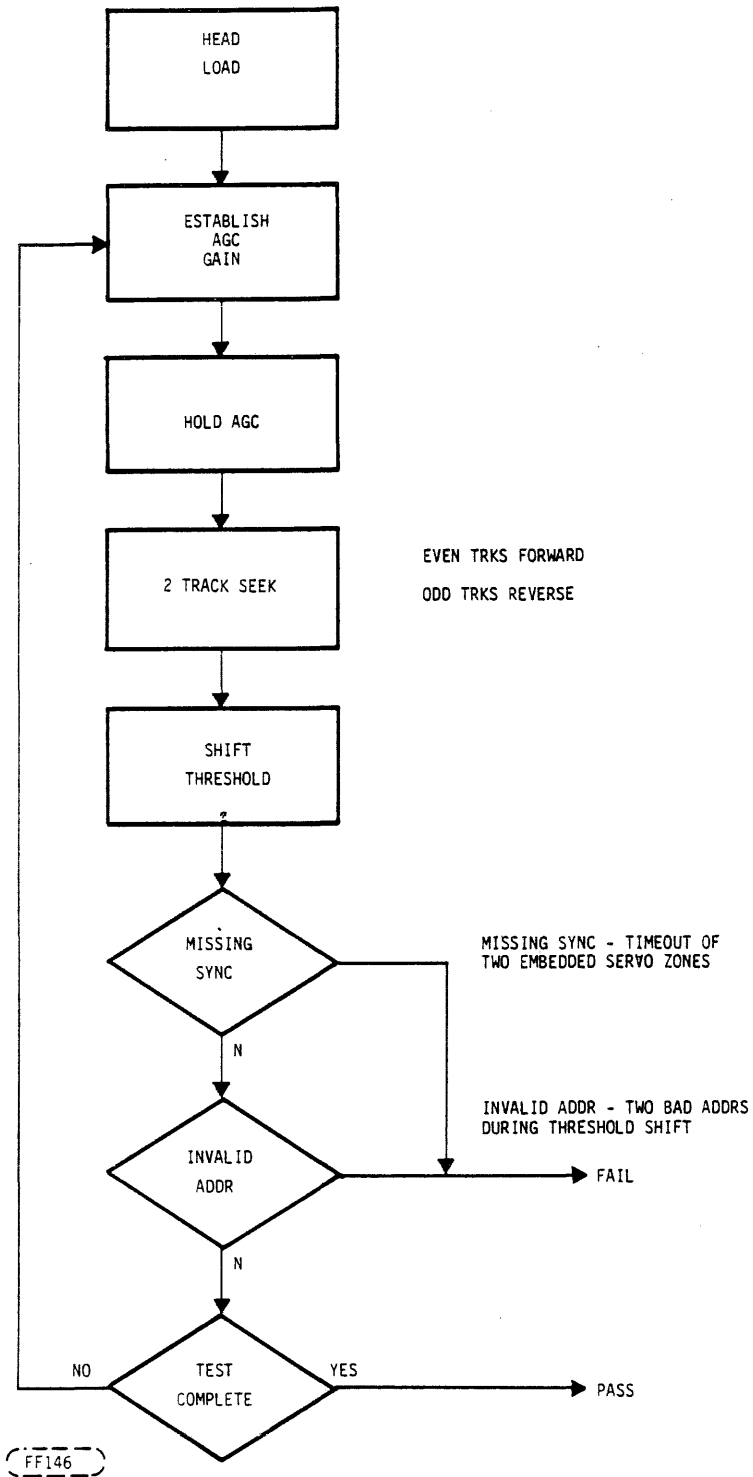


FIGURE 4-6. PROTECT DATA QUALITY FLOW DIAGRAM

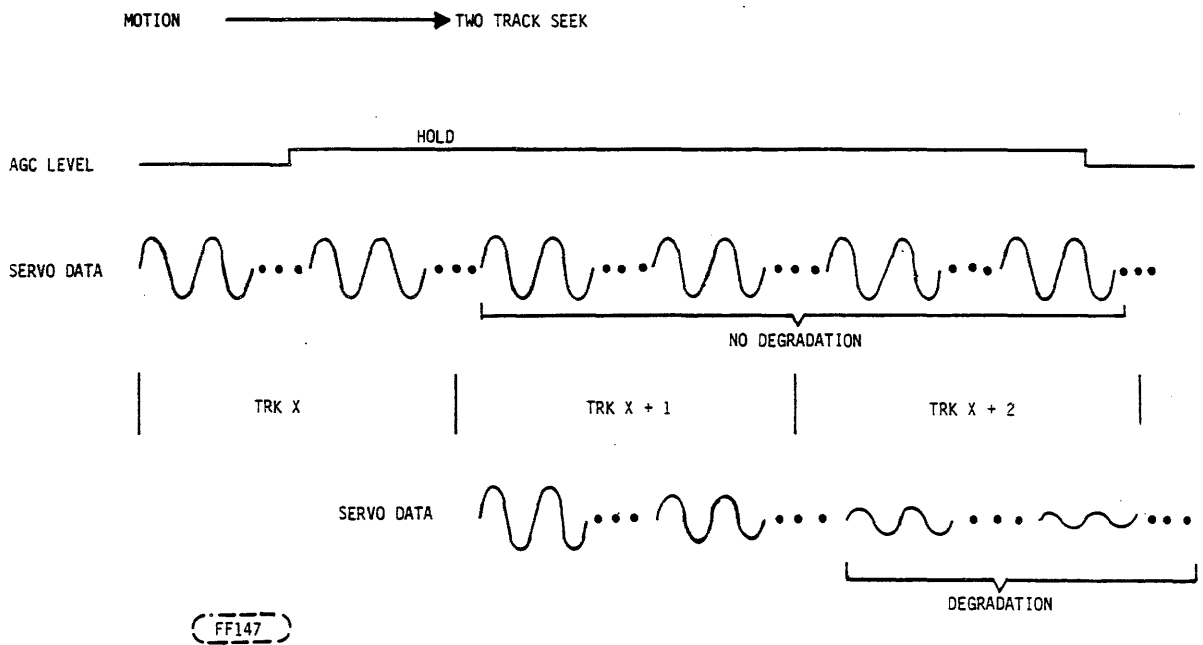


FIGURE 4-7. SERVO DATA DEGRADATION DURING PROTECT DATA QUALITY TESTS

During head loading, each floating arm is driven off the related cam and unflexes to force a head toward the air cushion on the spinning disk surface. The force applied by the floating arm causes the heads to fly or float on the air cushion. Vertical motion by a disk surface (due to warpage or imperfection) is countered by a move in the opposite direction by the gimballed head and/or floating arm. As a result, flying height remains nearly constant.

Head/Arm assemblies do not require alignment. Removal and replacement of Head/Arm assemblies is a depot level procedure ONLY.

4.2.1.5 TRANSDUCERS

The deck assembly contains two transducers: spin speed sensing transducer and velocity transducer. These transducers provide signals that are used by the microcomputer to generally control the progression of most machine operations.

SPIN SPEED SENSOR

The Spin Speed Sensor (Figure 4-8) generates a voltage pulse whenever a slot in a disk on the bottom of the spindle passes through the Spin Speed Sensor. The slot in the disk allows light from an infrared light emitting semiconductor to strike a light sensing semiconductor whose output current increases during the time the light through the disk slot strikes it. The resulting output is a train of pulses, each period of approximately 320 μ s in duration with a pulse occurring once each millisecond (approximately), see Figure 4-39. The period between Spin Speed Sensor pulses is checked by the microcomputer firmware (heads loaded, positioner in fine mode) and if the spin speed is within tolerance, an enable is provided for relay K1*. If the spin speed (r/min) is insufficient, this detected by the microcomputer which has one of two effects:

1. If the heads are not loaded, K1 will not be energized and the microcomputer will not initiate the load sequence.
2. If the heads are already loaded, K1 is opened, and thus the voice coil is disconnected from the power amplifier and connected to the emergency retract circuit. The heads are immediately unloaded at a controlled velocity to the retracted stop.

In addition, the "Spindle r/min Lost" fault will be stored in the microcomputer memory and the unit becomes "not ready."

VELOCITY TRANSDUCER

The Velocity Transducer (Figure 4-9) is a two-piece device consisting of a stationary tubular coil/housing and a movable magnetic core.

*K1 is on Base PWA, location shown in Figure 5-4.

The magnetic core is connected via the extension rod to the rear surface of the carriage assembly. All motion of the carriage is therefore duplicated by the magnetic core. As the core moves, an emf is induced in the coil. The amplitude of the emf is directly related to the velocity of the core (and carriage). The polarity of the emf is an indication of the direction of motion by the core (and carriage). The transducer output drives a summing operational amplifier located on the Base PWA. This signal is used by the servo system to control acceleration / deceleration and velocity of the carriage during seek operations.

Removal and Replacement of the Velocity Transducer is a depot level procedure ONLY.

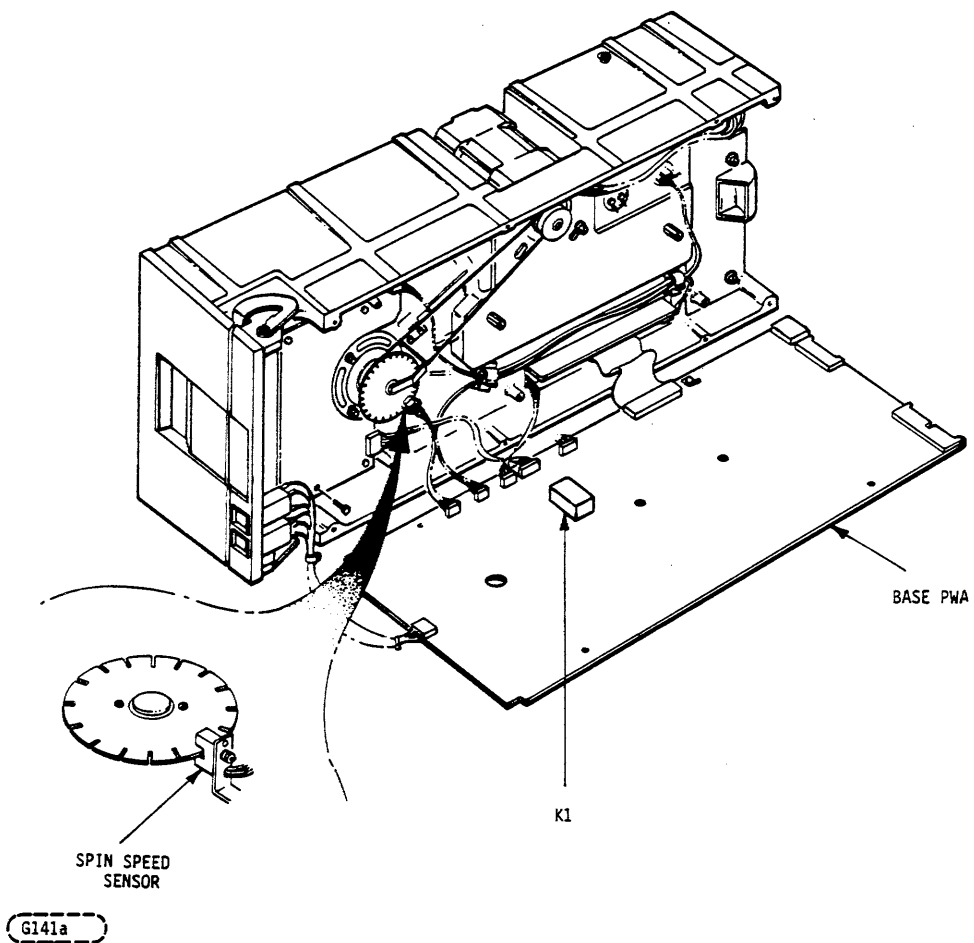
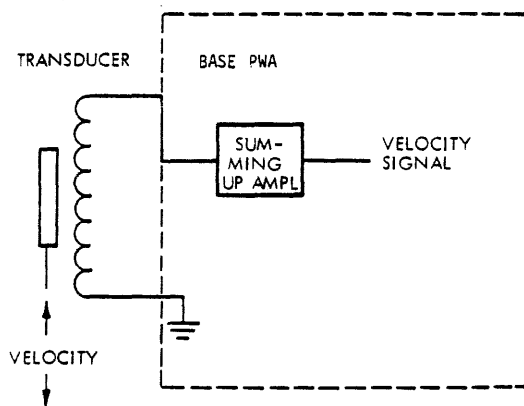
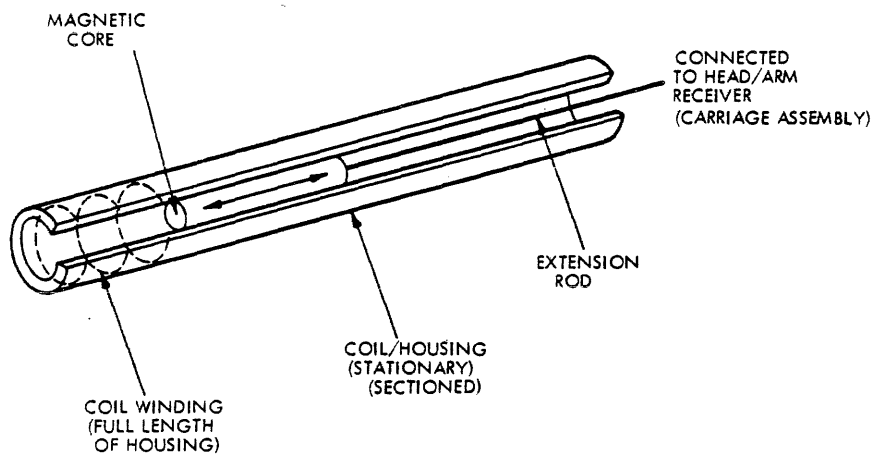


FIGURE 4-8. SPIN SPEED SENSOR



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FIGURE 4-9. VELOCITY DETECTION

4.2.1.6 DISKS

The disks are the recording media for the drive. The disks are 8 inches outer diameter. One disk is mounted on the spindle (non-removable by the operator) and one center-mounted on a hub in an operator removable cartridge. The recording surface of each disk is coated with a layer of magnetic iron oxide and related binders and adhesives.

Data is recorded on both surfaces of the fixed disk and of the cartridge disk. Servo information is embedded in each data track so that a separate surface for servo information is not required. Details on track formatting are given in the section on read/write theory of operation (Section 4.3.5).

Each disk surface has 624 tracks. The tracks are grouped in a 0.87 inch (22mm, approximately) band near the outer edge of the disk. The tracks are spaced about .0014 inch (0.36 mm, approximately) apart.

The disk cartridge has a one piece container that is sealed when not in the unit. When installed in the Micro Unit a door is opened to admit the read/write heads, and the bottom is bent up to allow purging air to flow around the disk. This design protects the disk cartridge from physical damage and greatly reduces the possibility of contamination of the disk recording surfaces.

Removal and replacement of the fixed disk is a depot level procedure ONLY.

4.2.1.7 SWITCHES

There are two types of switches used in the Micro Unit, front panel control switches and hardware interlock switches. Front panel control switches are described in Section 2, Operation. The various interlock switches are described in the following paragraphs.

HEADS LOADED SWITCH

The heads loaded switch status reflects the state of the read/write heads (loaded or unloaded). This status is used in the microcomputer. The switch is mounted on a bracket that is mounted on the side of the actuator magnet at about the 10 o'clock position (as viewed from the front of the unit). The switch is actuated by the carriage when it nears the fully retracted position, thus reflecting the unloaded status of the heads. When the carriage moves toward the disks during a power-on/load, the switch actuator is released transferring the switch contacts. This indicates the heads are not in the unloaded position; it does not indicate that the heads are loaded. This switch status remains unchanged until the carriage is retracted to the "unloaded" position and, therefore, does not precisely indicate the loaded/unloaded status of the heads. Precise loaded/unloaded status is determined by the logic when the servo circuits detect track 0. This switch is interlocked to the drive motor via the microcomputer which will not allow the spindle power to be removed until the heads are fully unloaded.

Removal and replacement of the Heads Loaded switch is a depot level procedure ONLY.

CARTRIDGE-IN-PLACE SWITCH

The Cartridge-in-Place switch is mounted on a bracket at the back of the cartridge receiver area. A spring actuator arm actuates this switch when the cartridge is fully in place. This switch is interlocked (wired in series) with the START/STOP switch and the Door Locked switch so that the drive cannot be started unless the door is locked and the cartridge fully in place.

Removal and replacement of the Cartridge-in-Place switch is a depot level procedure ONLY.

DOOR-CLOSED SWITCH

The Door-Closed switch is mounted on the top side of the base deck behind the door solenoid bracket. The switch is in the cartridge receiver area such that the plunger is actuated downward by the front door latch cover when the

front door is closed. This switch must be actuated together with the Cartridge-in-Place and the START switch before the drive will function.

Removal and replacement of the Door-Locked switch is a factory depot level procedure ONLY since, removing and replacing this switch requires the top cover to be removed and the solenoid bracket to be re-adjusted. The probability of damage to the disk surfaces is drastically increased if this is not done properly.

DOOR-LOCKED SENSE

An LED sensor detects the outer position of the door locking solenoid plunger. The MP requires a door-locked condition before the spindle motor is activated.

REMOVABLE DISK WRITE PROTECT SWITCH

The removable disk write protect switch is mounted on the same bracket as the Cartridge-in-Place switch. The spring actuator arm of the protect switch senses a plastic tab in a groove in the end of the cartridge where the heads go in. See Figure 8-10. When the tab is in the lowest position in the groove, the spring arm is in the "in" or actuated position, indicating that the cartridge disk is NOT write protected. When the tab is halfway up the groove the spring arm is in the out or unactuated position, signaling to the Microcomputer that the cartridge disk is to be write protected.

4.2.2 ELECTRONIC ASSEMBLIES

The electronic assemblies are the Base PWA, the Read/Write Preamp PWA and the Read Signal Processor PWA. These circuit boards are mounted as shown in Figure 4-2. Component location on the circuit boards is given in Section 5. PWA part numbers and Figure numbers for the schematics applicable to each in addition to other schematics are listed in Table 5-1. Theory of Operation for the electronics is described partly by functional categories and partly on an assembly PWA basis. See Section 4.3, Functional Description. The POWER SUPPLY and I/O ADAPTER are described in Manuals 77711033 and 77711038.

A summary of the functions performed by the LMU PWA are as follows: Refer to Figure 4-1.

- Preamp
 - Amplifies read signal from heads
 - Selects head
 - Detects certain write faults
 - Provides write current to head
 - Recovers servo position error and servo data
- RSP
 - Converts analog read signal to digital pulses for decode
- Base Board
 - Microcomputer System provides overall drive control
 - Servo data recovery (LSI)

- Read decoder and write encoder logic (LSI)
- Read and Servo PLOs
- Servo analog
- Voltage fault logic
- AC Distribution
 - Distribution point of AC to spindle and blower motors
 - Contains motor control solid state relays
- I/O Adapter (optional)
 - Converts Microcomputer interface to OEM interface.

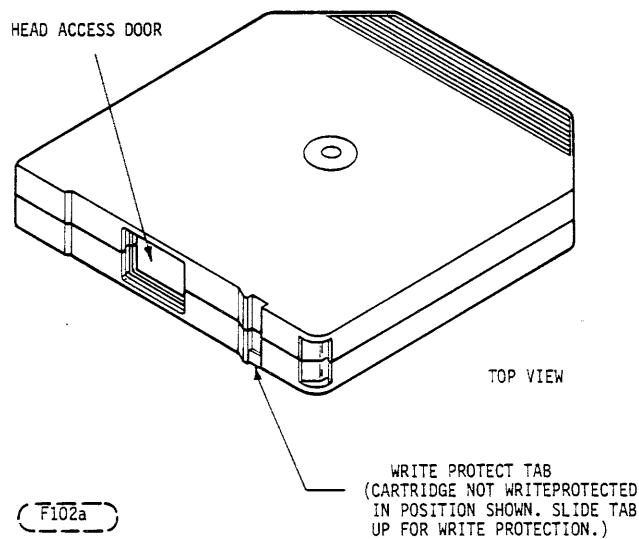


FIGURE 4-10. DISK CARTRIDGE SHOWING WRITE PROTECT TAB

4.3 FUNCTIONAL DESCRIPTION

4.3.1 GENERAL

The functional theory of operation is organized under the following major headings:

- Drive Overall Control System
- Power On/Off and Spindle Start/Stop Functions
- Read/Write Head Positioning System
- Read/Write System
- Fault Detection System
- Power and Input/Output Module
- I/O Interface, I/O Adapter to Controller

4.3.2 DRIVE OVERALL CONTROL SYSTEM

The LMU is under the overall control (excluding any control exerted by the controller via the interface lines) of the Microcomputer on the Base circuit board. The microcomputer system is described in the following paragraphs. Any further details of the microcomputer theory must be taken from vendor published descriptions of the various chips in the Microcomputer system. Figure 4-12 is a block diagram emphasizing the Microcomputer. Figure 4-13 is a block diagram of the Microcomputer system only.

The firmware is organized in 19 major modules as depicted in Figure 4-11.

The 'Action' module is the main control module and calls a function module according to the instructions it has received. Each of the function modules (center column of Figure 4-11) will in turn call upon the subroutines required to perform its function and determine the progress of execution of that function. When each function module finds that its function is completed (or has failed) it determines the next action to be performed and returns control to the Action module so that the next function may be executed.

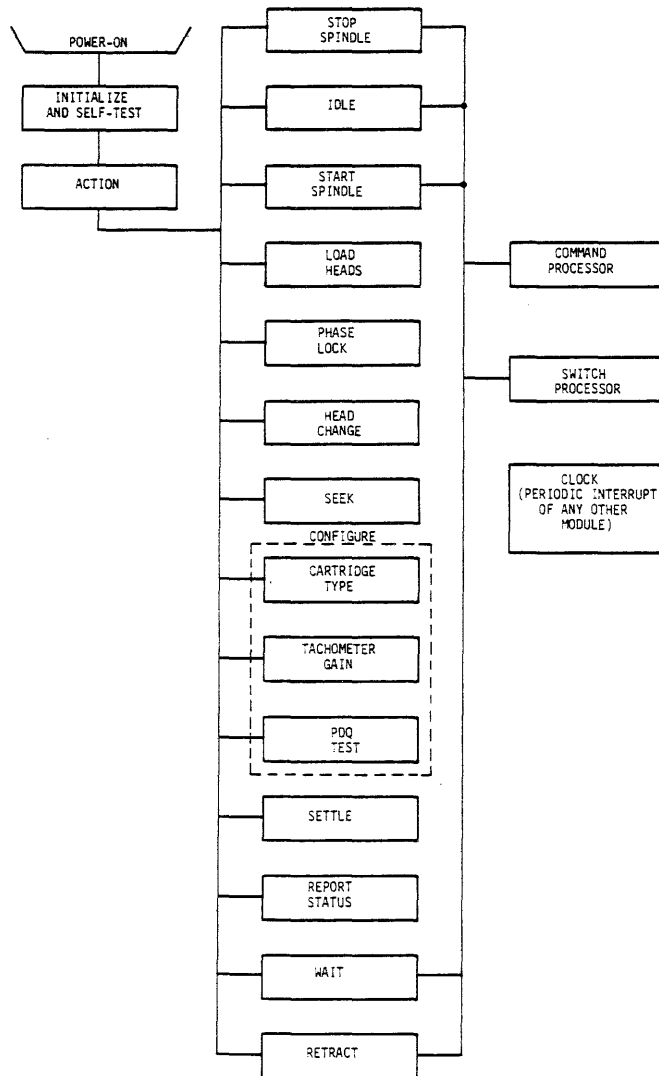
The clock module will interrupt the execution of any of the other modules in order to perform housekeeping services needed by all modules. These services include reading the switches, control of the LED's, determination of spindle RPM once the heads are loaded, and maintenance of a timer used by the function modules.

4.3.2.1 MICROCOMPUTER OVERVIEW

Refer to the Base PWA schematic in Section 5. The microcomputer is an 8039/8049 with 6 k byte of Program memory (in ROM) as shown on schematic sheet 2. I/O for the microcomputer is shown on sheet 3 and explained below. The microcomputer interface outputs are implemented with 74LS374 tristate latches. Interface inputs use 74LS244 input buffers. Several of the interface and internal hardware inputs are multiplexed into the microcomputer bus with 74LS257 circuits. The servo track address (from the embedded servo on the disk) is converted from serial to parallel with a 74LS164 shift register. Table 4-1 shows the I/O memory map for the above signals.

TABLE 4-1. MICROCOMPUTER I/O MEMORY MAP

| ADDR A2 | ADDR A1 | ADDR A0 | READ | WRITE |
|------------|------------|------------|--------------------------|-------------------------------------------|
| X | 0 | 0 | DATA-DET-RS/SVO-VALID-RS | TRK ADDR Register reset one shot clock |
| 0 | 0 | 1 | Status Byte 1 | Flt Reset |
| 1 | 0 | 1 | Status Byte 2 | Flt Reset |
| X | 1 | 0 | Track Addr Reg | Interface Address bus |
| X | 1 | 1 | Interface Data bus | Interface Data bus |



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FIGURE 4-11. FIRMWARE FUNCTION CHART

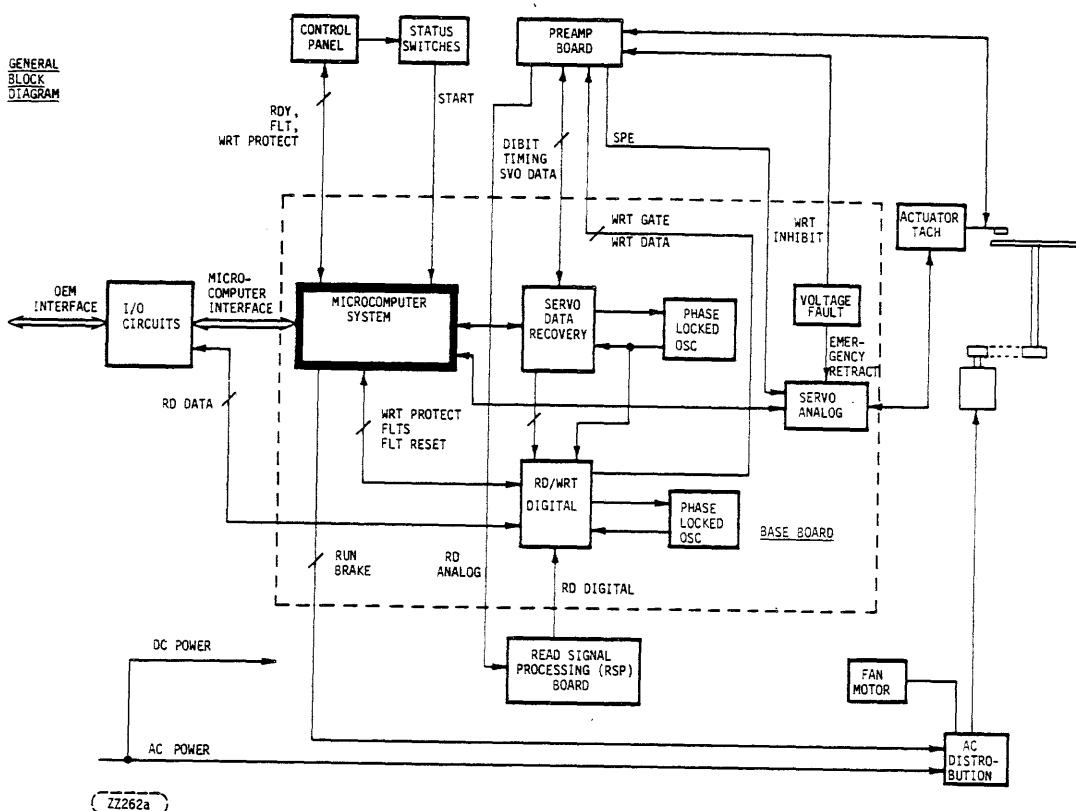


FIGURE 4-12. LMU GENERAL BLOCK DIAGRAM EMPHASIZING MICROCOMPUTER

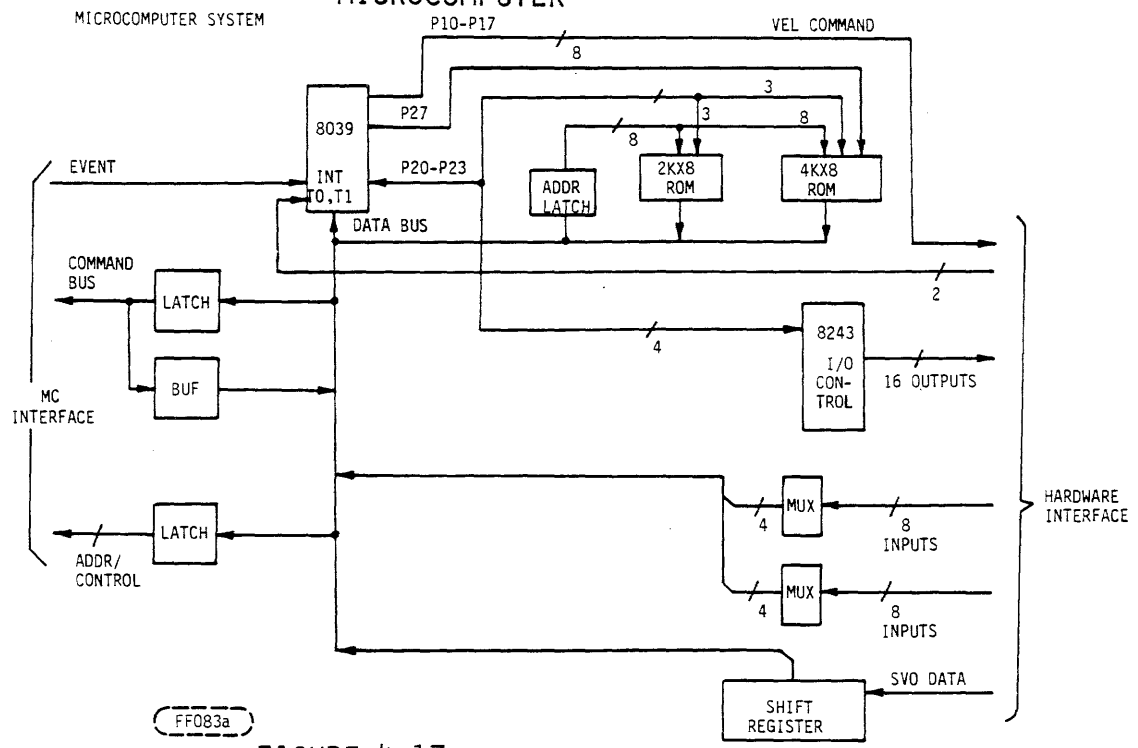


FIGURE 4-13. MICROCOMPUTER SYSTEM

Most of the internal hardware outputs are implemented with an 8243 (accessed with special I/O instructions) which is shown on schematic sheet 2.

The Microcomputer (8039/8049) has four basic functions:

1. Controls command data transfers from the PIO.
2. Monitors the front panel switches and interlock switches and controls the front panel LEDs. Thus the MC starts-stops the spindle, WRT protects fixed disk or clears fault indicators according to front panel switches.
3. Controls the actuator during coarse seek and head load or head change.
4. Monitors various status conditions and updates status to HOST.

The I/O of the Microcomputer system can be broken into functions groups as follows:

1. Micro-Unit to Host Interface.
2. Front Panel and Interlock Switch Monitor and Spindle START/STOP.

Outputs:

RDY-LED/-L active when drive is Ready (heads loaded and no faults). Also blinks during Spindle Start/Stop. Also rapid blinks during servo or Read/Write activity.

PROT-LED/-L active when fixed media is write protected due to action of front panel switch. Also blinks during faults.

RUN/-L active when spindle motor is running or braking and high when off.

BRK-SSR/-L active low when motor is braking.

It allows half wave rectified AC to go through motor to brake it.

UNLOCK DOOR/-L active when spindle stopped to activate door solenoid.

Inputs:

FIXED PROT/-L - From control panel, active when the fixed disk is write protected.

START/-L - Active low indicates to microcomputer that the START/STOP switch, Door Closed, and Cartridge-in-Place switches have been operated inward to the start position.

REM-PROT/+L - From switch at the back of cartridge receiver area. Active high indicates to the Microcomputer that the cartridge disk is to be protected from being written on. When the switch is pushed in (actuated) by the tab on the cartridge, REM-PROT/+L line is grounded indicating the removable disk is not to be write protected.

DOOR-NOT-LOCKED/+L - Active high when door solenoid plunger does not prevent door opening.

CARRIAGE-LD/+L - From the carriage load switch on the actuator. See Section 4.2.1.7. Active high when the heads are loaded or on the head load ramps.

3. Actuator Control and Head Load/Head Change.

These inputs/outputs to the microcomputer are discussed in detail in the sections on Actuator Positioning and Read/Write circuits (Section 4.3.4 and 4.3.5).

4. Status Monitoring.

Inputs:

UNSAFE/+L - From UNSAFE LATCH on R/W Preamp board. When active high, indicates to the microcomputer that an unsafe condition has been detected by the hardware. For details see Section 4.3.6.



R/W FLT/-L - From READ/WRITE CONTROL LSI circuit. Active low indicates the Read/Write digital circuits have detected a fault. See Section 4.3.6 for more details.

4.3.2.2 MICROCOMPUTER FLOW CHARTS

Details of the manner in which the microcomputer controls the various operations of the LMU are illustrated in the flow charts that follow.

| <u>FIGURE NUMBER</u> | <u>PURPOSE</u> |
|----------------------|-----------------------|
| 4-14 | Power on State |
| 4-15 | Idle State |
| 4-16 | Wait State |
| 4-17 | Retract State |
| 4-18 | Timer Interrupt State |

In the state diagrams, the following symbols are used.

-  = Steady State
-  = Transient State
- * = Adapter commands and switch changes are detected and processed within these modules.

COMMAND PROCESSOR

- Get Command from Host
- Accept or Reject Command
- Execute Command unless positioner motion is required (Seek, Head Select, RTZ, or Fault Reset) or unless spindle motor Start/Stop is required.

SWITCH PROCESSOR

- Set Up Switch State
- Set Up Write Protect State
- Cause Fault Reset

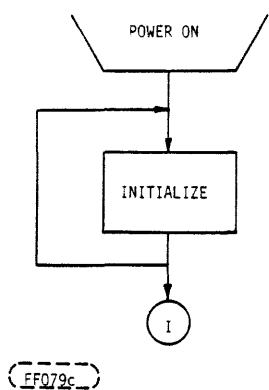


FIGURE 4-14. POWER ON STATE

Function of Power On State and Actions in the Function:

INITIALIZE

- Processor Self-Test
- Servo-Digital Test
- ROM Check
- Initialize RAM
- Initialize Output Ports

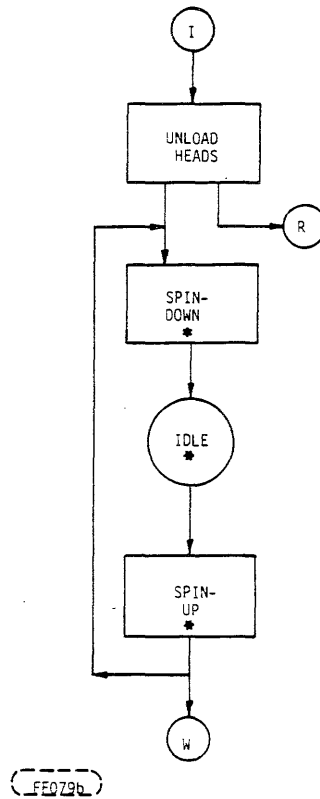


FIGURE 4-15. IDLE STATE

Functions of Idle State and actions in the functions.

UNLOAD HEADS

- Retract Heads

SPIN-DOWN

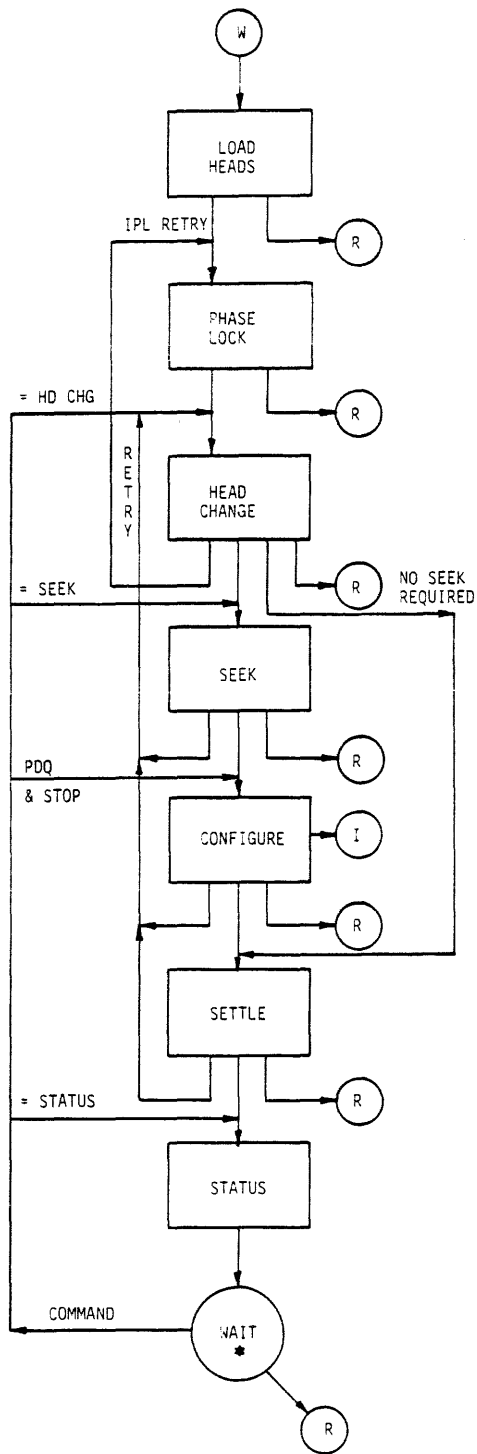
- Stop Spindle
- Send Status
- Process Commands
- Process Switches

IDLE

- Control Cartridge Access
- Wait for Spindle Start Conditions
- Process Commands
- Process Switches

SPIN-UP

- Start Spindle
- Wait for Chamber Purge
- Process Commands
- Process Switches



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FIGURE 4-16. WAIT STATE

LOAD HEADS

PHASE LOCK

- Frequency Lock
- Phase Lock

HEAD CHANGE

- Determine Positioner Location
- Move Positioner to Destination (Less than 2 tracks)
- Verify Phase Lock

SEEK

- Command Positioner Velocity According to Distance from Destination

CONFIGURE

- Determine Cartridge Type
- Adjust Tachometer Gain
- PDQ Test
- Null

SETTLE

- Verify Arrival at Destination
- Wait for Track Center Settling

STATUS

- Adjust Write Current Magnitude
- Report Status

WAIT

- Monitor Track Center
- Monitor Track Address
- Monitor Faults (R/W, RPM, Phase-Lock)
- Process Commands
- Process Switches

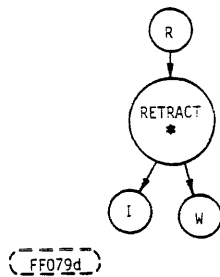


FIGURE 4-17, RETRACT STATE

Function of Retract State and actions in the function.

RETRACT

- Retract Heads
- Process Commands
- Process Switches

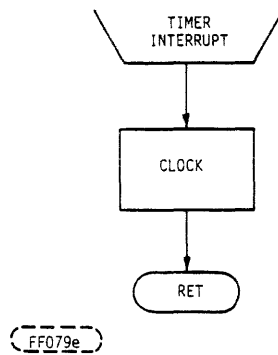


FIGURE 4-18, TIMER INTERRUPT STATE

Function of Timer Interrupt State and actions in the function.

CLOCK

- Maintain LED's
- Read Switches
- Determine RPM when Loaded
- Maintain Operation Timer
- Operate Condition Code Display

4.3.3 POWER ON/OFF SEQUENCING AND SPINDLE START/STOP FUNCTIONS

4.3.3.1 POWER SEQUENCING

Power up/down sequencing is done by some part of the system external to the LMU, as the LMU has no switch that controls either its AC or DC power inputs. Once AC power is on, the blower operates to cool the LMU. When the DC power is fully on, the electronics operate. The electronics performs an initialization and self test procedure (see Figure 4-14) and then controls the spindle start up sequence.

4.3.3.2 SPINDLE START SEQUENCE

The start of the LMU spindle motor is sequenced by microcomputer firmware and relays on the AC Distribution PWA. Figure 4-15 illustrates the sequences involved.

The spindle start sequence proceeds as follows:

- Operation of the START switch applies ground to the START/-L line through two interlock switches--cartridge in place and cartridge access door closed switches. This goes to the microcomputer I/O port U28 on the Base PWA.
- The microcomputer continually loops through a routine and as part of the routine, it interrogates the I/O port, detects that the START switch is in the START position and that the bit in LMU memory storing the Spindle Power On command indicates power can be applied to spindle (bit is logic 1).

This bit is initialized to logic 1 when power comes on. It can be changed by the interface Event Byte spindle power on (Bit 3) or spindle power off (Bit 0). Table 4-3 defines the interface Event Byte commands.

- The MP then turns the door lock solenoid off and checks for a Door-Locked condition.
- After making the above checks, the microcomputer sends out the command to the I/O port U28 to activate RUN/-L which causes relays K1 and K2 on the AC Distribution PWA to connect the AC power lines to the spindle motor.
- The start up is monitored by the microcomputer and if the start up is too slow or does not occur, a fault is generated. AC power will be removed from the motor and the start will be aborted.
- If the spindle speed is correct by the end of a two minute timeout head load is attempted. If head load is successful, the READY indicator ceases blinking and remains illuminated. Refer to Figure 4-16 for Head Load Sequence.

4.3.3.3 SPINDLE STOP SEQUENCE

The spindle stop sequence is under the control of the microcomputer. The command to stop could originate with the I/O Adapter which could send a Spindle Power off bit in the Event Byte or the microcomputer could detect that the START switch contacts are open. The operator should always wait for the green Ready LED to stop rapid blinking (which indicates drive activity has stopped) before deactivating the START switch. The microcomputer enters the carriage retract subroutine (Figure 4-17) and then the Stop Spindle subroutine (Figure 4-15). To turn off the spindle motor the microcomputer deactivates RUN/-L to de-energize relays K1 and K2, and activates BRK-SSR/-L to energize relay K3, K1, K2 and K3 are on the AC Distribution PWA. K3 remains energized connecting DC braking voltage to the motor for 6 seconds. When the spindle speed drops below 4 r/min, the microcomputer turns off K3, removing DC braking voltage from the motor.

The microcomputer continues to check spindle speed for a speed less than 4 r/min for 48 seconds. If the speed doesn't get below 4 r/min in that time, a fault is indicated.

4.3.3.4 POWER OFF

To power off the LMU after the spindle has stopped, open the system circuit breaker or power switch that routes power to the LMU. There is no power control switch on the LMU.

NOTE

Power must not be removed from the LMU if a fault occurs during Spindle Power Off sequence. If the fault cannot be cleared from the front panel and the READY Indicator remains ON or continues blinking, it indicates that the LMU was unable to retract heads. Power should not be removed if the heads cannot be retracted. Maintenance personnel should be summoned.

This should not be confused with rapid FAULT blinking which indicates a cartridge PDQ fault (see Section 2.5 of Manual 77711044).

4.3.4 READ/WRITE HEAD POSITIONING SYSTEM

4.3.4.1 GENERAL

The positioning servo system is a closed loop servo system containing a position loop, a velocity loop, and a current loop. Figure 4-18 is a very simplified block diagram of the servo system. The velocity and current loops are analog while the position loop is a combination of digital and analog circuitry.

The positioning system differs from previous systems in that it has absolute coarse position information (track number) so that the drive can verify its own position. This same coarse position information also allows head switching (selecting a new surface) to a totally arbitrary radial and concentric position and re-establishing the original track position. This means no head alignment is required for removable media or during head replacement.

This system has added complexity to give the capability to position across bad tracks (no valid servo data) and servo on partially valid tracks. Complexity is also required to accomplish the head switching to arbitrary radial and concentric positioned head in a random data zone.

4.3.4.2 SIMPLIFIED POSITIONING OPERATION

This section gives a simplified, overall description of the operation of the positioning servo system.

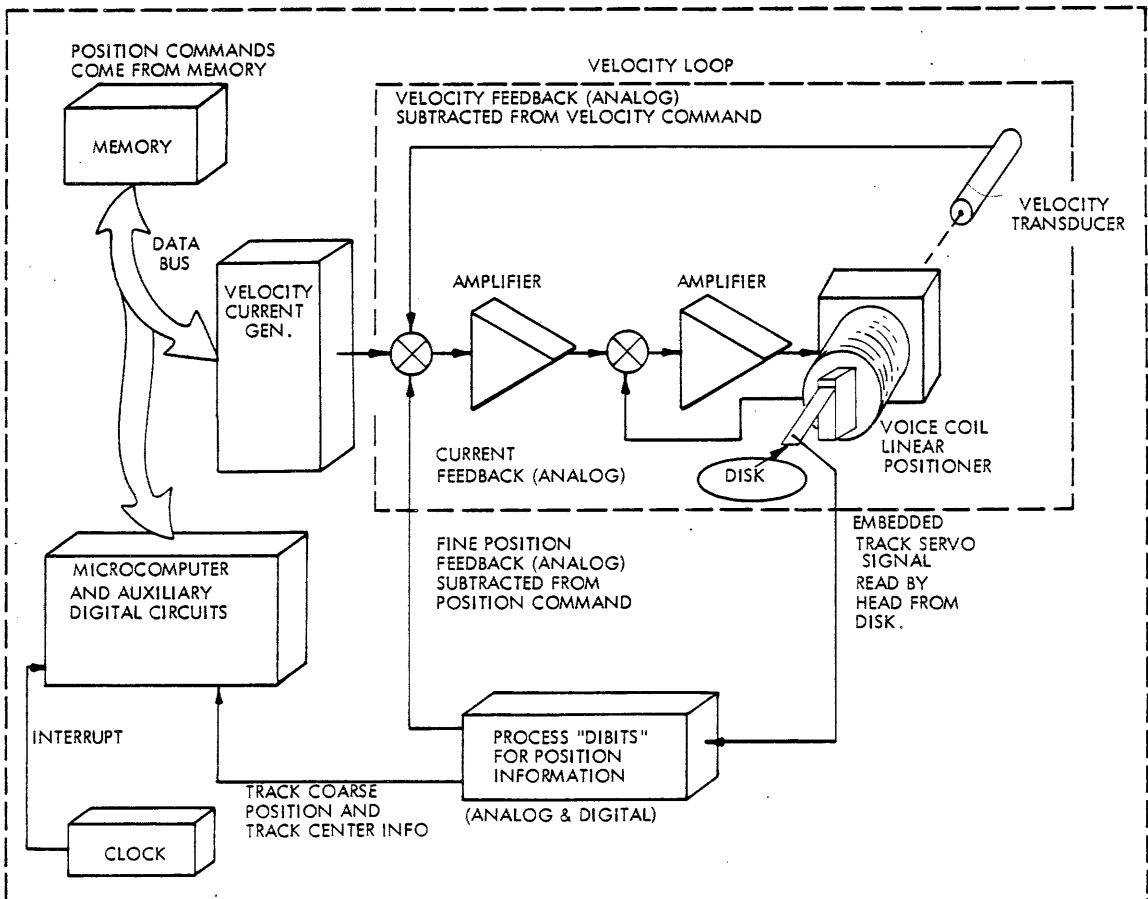
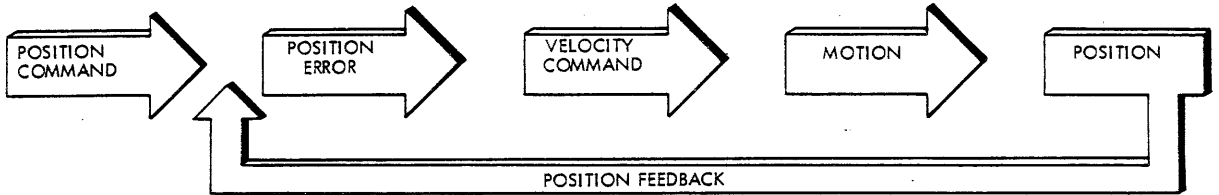
1. The positioning operation begins when the system controller communicates a SEEK command to the LMU. The microcomputer receives the SEEK command and initiates and controls the positioning operation. There are also times when the microcomputer initiates a positioning operation without being commanded to do so by the system controller. This is the initial seek to track 0, an RTZ (return to zero) and the retract operation.
2. The microcomputer calculates the number of tracks to be traversed during the positioning action by comparing the present track number (stored in microcomputer memory) with the destination track number.
3. The microcomputer searches a table of velocity profiles for the correct velocity profile required for the commanded repositioning, and for the correct entry point into the table.
4. The digital (binary) number representing the initial velocity is taken from the velocity profile table and converted to an analog voltage in a digital-to-analog (D/A) converter.
5. The digital to analog converter output voltage is amplified and applied to the voice coil linear positioner.
6. The positioner begins moving toward the location of the destination track.
7. An analog voltage proportional to positioner current is fed back to provide the proper acceleration profile to the positioner.
8. A velocity transducer (see Section 4.2.1.5) senses the positioner velocity and feeds back a voltage proportional to velocity. This velocity feedback is subtracted from the command voltage applied from the D/A converter (item 4 above) creating a "following error" signal which continues to provide drive to the voice coil.

9. The positioner ceases accelerating when the desired "initial" velocity is reached and continues at the "initial" velocity until the microcomputer commands a change in velocity. .
10. The position loop provides head positioning information to the positioning servo system. The positioning information includes the following:
 - a. A signal that indicates the displacement of the heads from their nominal track centerline (SPE).
 - b. Signals read from track embedded servo information during seeks to indicate each track address.

Information for the position loop is derived from the embedded track servo signals (Figure 4-21) written at the beginning of 32 sectors. A DC erased gap in the information written on the disk surface alerts the electronics that the sector AGC field, track address code and SPE dibits are coming up next on the track. During a seek, the Read/Write head reads the track addresses on the tracks it passes as the head moves radially toward or away from the center. This provides the coarse position information for the position system. Figure 4-23 shows track/sector information encountered by head and signal from head as it moves radially across disk toward center. Refer to Sections 4.3.4.3 and 4.3.4.4 for details.

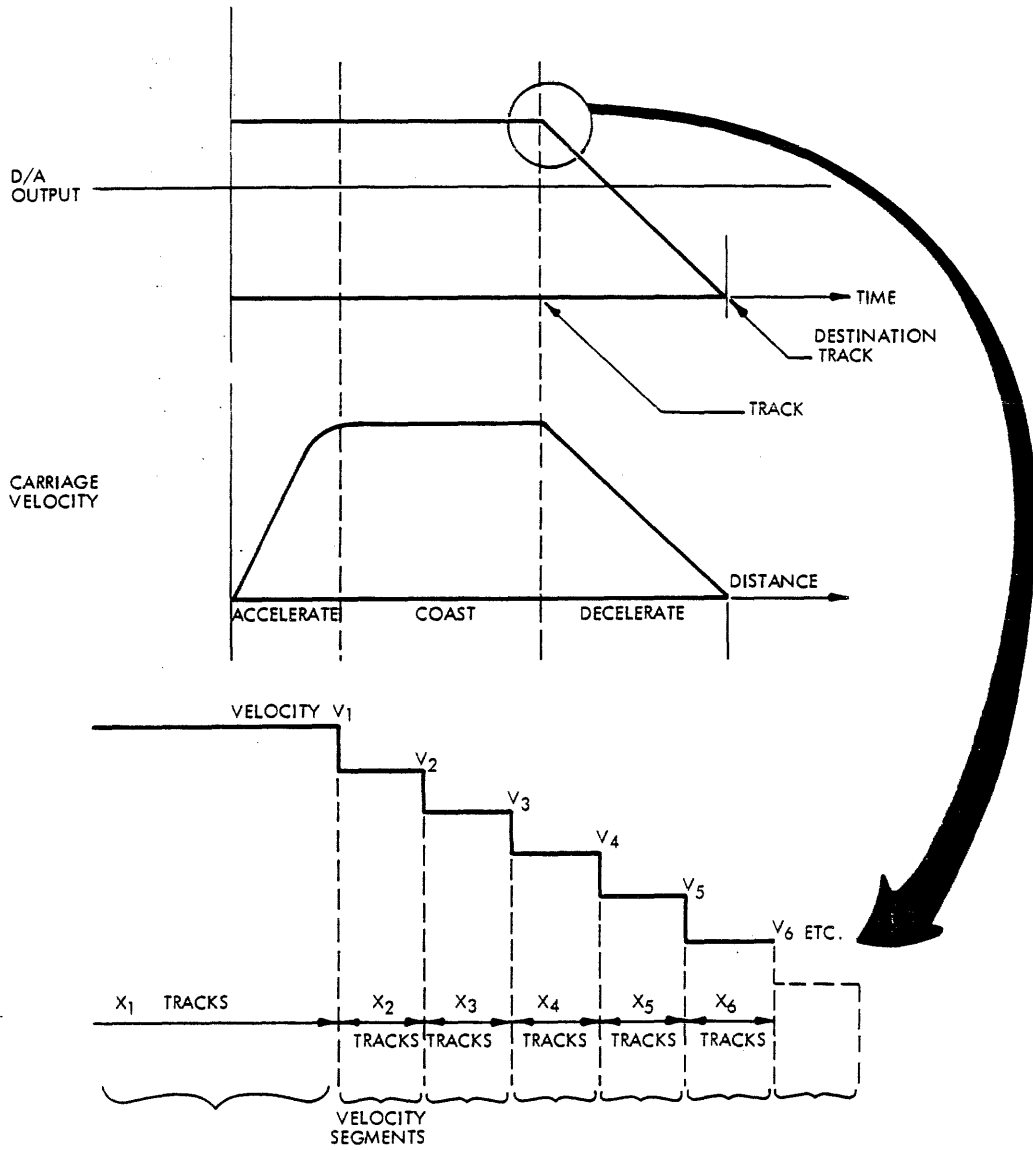
11. The microcomputer and associated digital circuits monitor position and number of tracks traversed using embedded track address information and change the velocity number in the D/A converter as required to provide the proper velocity profile for the positioning action in process. Figure 4-19 shows a velocity profile for a long seek. Every operation is made up of one or more of the distance/velocity segments like those shown in the expanded section.
12. When the positioning operation is completed to less than one track away from the destination track, operation enters what is called the servo fine mode. In the servo fine mode, fine position feedback derived from the track even/odd dibit signal is switched in to bring the head on track. The microcomputer monitors the time required to complete the seek and signals a seek error if the seek is not completed in time or if the heads do not stay on track when the track is reached.
13. The fine mode positioning circuit remains active following completion of a seek. If the head drifts off its centered position, the track servo position error signal (SPE) will no longer be at a null. The signal, functioning as the fine position analog signal acts as a position error signal to drive the positioner back into position.
14. As an aid to data recovery, the track servo position may be offset from a true null by a predetermined amount in either a forward or reverse direction in response to microprocessor commands.

SERVO FUNCTIONAL ELEMENTS



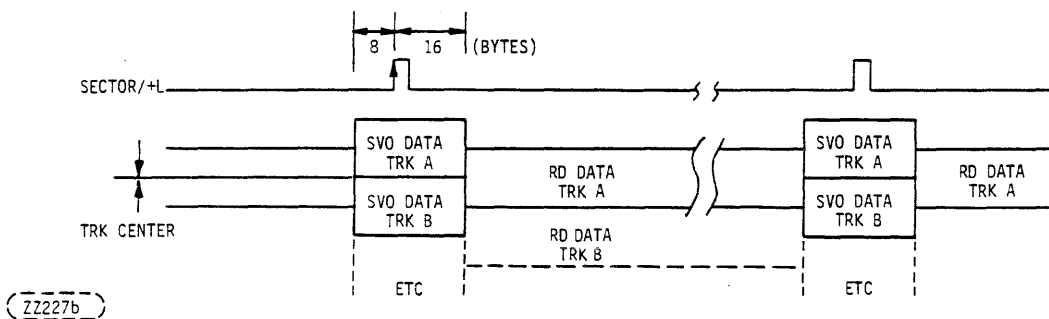
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FIGURE 4-19. POSITIONING SYSTEM GENERAL BLOCK DIAGRAM



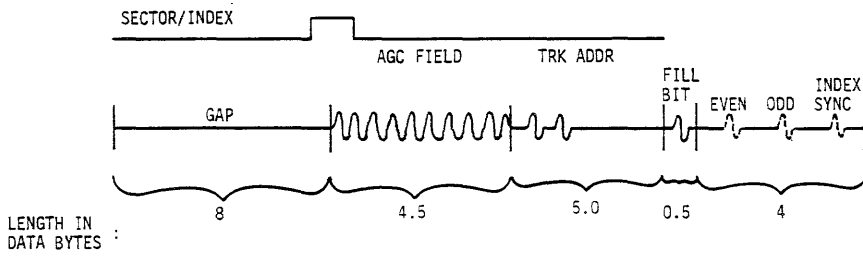
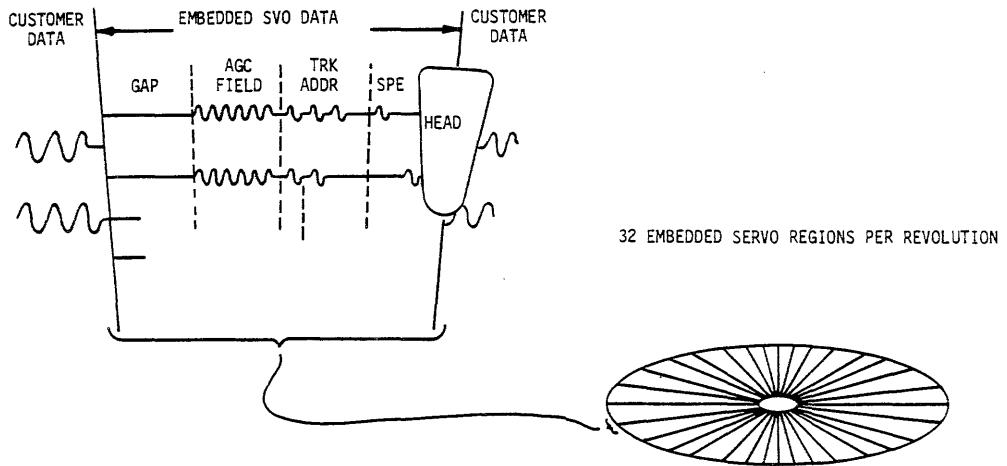
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FIGURE 4-20. SEEK VELOCITY PROFILE



Z2227b

FIGURE 4-21. ORIENTATION OF SVO DATA FIELD



TOTAL LENGTH = 22 DATA BYTES 24 BYTE HEAD SKEW REGION

GAP: DC ERASED REGION FOR PLO SYNC
 AGC FIELD: SET PREAMP GAIN FOR SVO AND DATA RECOVERY
 TRK ADDR: GRAY CODED TRACK ADDRESS READ BY MICROCOMPUTER
 FILL BIT
 ODD/EVEN DIBITS: USED TO DERIVE SERVO POSITION ERROR (SPE)
 INDEX SYNC: SYNCs SECTOR COUNTER TO PRODUCT INTERFACE INDEX

72271a

FIGURE 4-22. FORMAT OF SERVO DATA FIELD

4.3.4.3 EMBEDDED SVO CONCEPT/FORMAT

The coarse servo information (track address) and fine servo information (dibits) are prewritten 32 times per revolution. This servo field is written in the region normally reserved for head scatter on other SMD family drives. HD scatter requires 24 bytes or 8 bytes before sector and 16 bytes after. Thus the SVO data is written in a normally unused data region. Orientation of the SVO data field is shown in Figure 4-20.

The format of each SVO Data field is shown in Figure 4-21 and 4-22. Each SVO bit is a doublet written with 2 interface data bit time periods between doublet transitions. Each SVO field is written at equally spaced intervals maintaining phase coherence from track to track. This field provides the PLO reference CLK, AGC field, TRK address and fine servo information.

The servo information contained within each zone is summarized in Table 4-2. Also included in Table 4-2 is the system tolerance to format errors.

TABLE 4-2. ZONE SERVO INFORMATION

| EMBEDDED SVO INFORMATION | TOLERANCE TO FORMAT ERRORS |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1. Coarse Track Position | Microcomputer requires two consecutive correct cylinder address reads before accepting information. Single or multiple bad tracks can be tolerated because of seek recovery firmware. |
| 2. Fine Track Position | System tolerant to dibit errors due to filtering effect of SVO. |
| 3. Disk Speed Reference | Maximum ϕ -error injected into loop limited to 0.28% (800 ns) per sample allowing several missing sectors before excessive ϕ -error builds up. |
| 4. Rotational Position | The Index pulse included in the SVO field only serves as a sync to a hardware sector counter so that extra or missing index pulses can be tolerated without effecting the interface Index. |

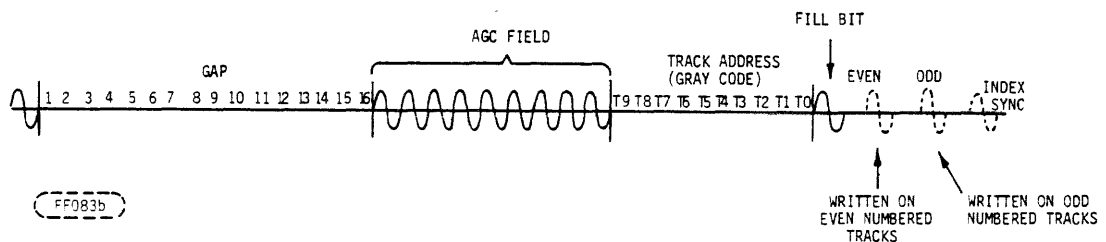


FIGURE 4-23. EMBEDDED SERVO DATA FIELD

SERVO DATA ERROR TOLERANCE

Concentric position tolerance to servo data zone flaws: (Phase locked OSC System)

If a gap is not detected due to a flaw in the gap area, no phase error will be injected into the PLO. The maximum phase error is set to +16 SVO clks so that if a flaw in the sync bit area exists the PLO will remain locked for several flawed servo data zones.

Radial position tolerance to servo data zone flaws in the coarse track address field are allowed for non-consecutive servo zones because the MC reacts only when two consecutive track addresses are either correct or incorrect. the fine position error is also monitored by the MC and digitally filtered allowing some flaws in the dibit field.

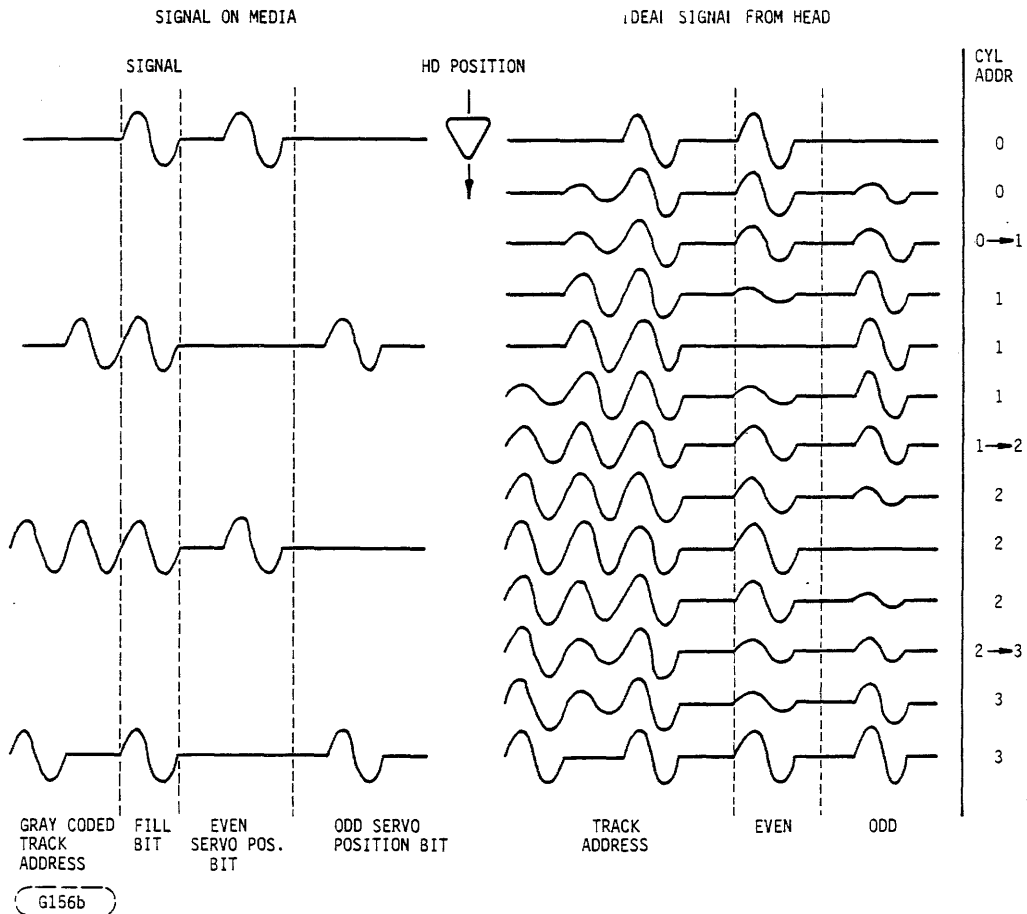


FIGURE 4-24. TRACK/SECTOR SERVO INFORMATION SHOWN AS HEAD MOVES TOWARDS CENTER OF DISK

HEAD SWITCHING

Head switching is complicated because the radial and concentric position is lost and the re-establishment of position is done in a random data zone. The establishment of the concentric position relies on the detection of a gap-absence of read data of amplitude less than approximately 20% of normal AGCed level. Although there are no other written gaps on track center, the data from adjacent tracks can sum to zero due to arbitrary phase of the written data when the head is positioned between tracks. The approximate 20% threshold is set by noise margins to guarantee normal gap detection and low enough not to detect excessive gaps between tracks.

To re-establish concentric position, hardware first looks for a gap of a certain length followed by a sync bit. The PLO counter then starts and a window opens when the next servo field should be found. If a gap is detected during this window and the sync bit following the gap falls within 800 ns (16 SVO clks) of where the correct sync bit should be, the PLO is considered re-phased. If a gap is not found during this window or the sync bit has excessive phase error, the PLO counter will be stopped and the process restarted - looking for a gap. Thus to rephase the PLO (re-establish concentric position) falsely would require correct minimum sized gaps written at the same spacing as the servo fields with sync bits within 16 servo clocks of the servo field timing. (This is +16 clks out of 5,168 total). Even if this happens, the microcomputer checks the track address to be within ± 8 tracks (includes maximum mechanical head misalignment) of the previous (before head change) position for two consecutive samples, it will re-start the rephasing process. If the track address is correct, it will begin radial repositioning to the correct track. Once the system has re-established its concentric position, a window generated from the PLO counter prevents false gap detection by allowing the gap detector to function only during the established window.

The hardware will rephase Index and Sector at the same time the MC is correcting the track position. Index is generated from a Sector counter which is phased by an Index sync pulse located in one servo zone around the disk. The first Index sync encountered will cause an Index output and Sector counter start. If the next Index sync pulse occurs when the sector counter final count is reached, the sector counter is considered locked and further Index pulses are ignored unless two Index pulses occur in the same radial position other than the Sector counters established position. The sector counter will then be rephased. Thus, the Index logic has the following characteristics.

1. Outputs Index on first and second detected Index pulses during initialization.
2. Initialization requires two consecutive good Index synchs to synch sector counter.
3. Can handle infinite dropouts after sync.
4. Can handle 1 extra Index/Revolution. (False sync)
5. Uses 50% threshold on pulse detection to guarantee no extra Index sync pulse detections.

4.3.4.4 DETAILED POSITIONING SYSTEM THEORY OF OPERATION DIGITAL

The servo system is shown in block diagram form in Figure 4-25. Each major block's function is summarized below and discussed in detail in following paragraphs.

Servo Data Recovery (Digital) - This block includes the SVO data recovery, PLO phase detector, PLO counter, SVO data write protect and Index, sector generation. It interfaces to the MC providing the track address and the MC provides PLO sync control during initialization and head change. It also interfaces to the Servo Sample Demodulator (SPE/AGC system) providing gating signals to control AGC timing and SPE generation. Finally it interfaces to the PLO providing phase error information and the PLO divider/counter.

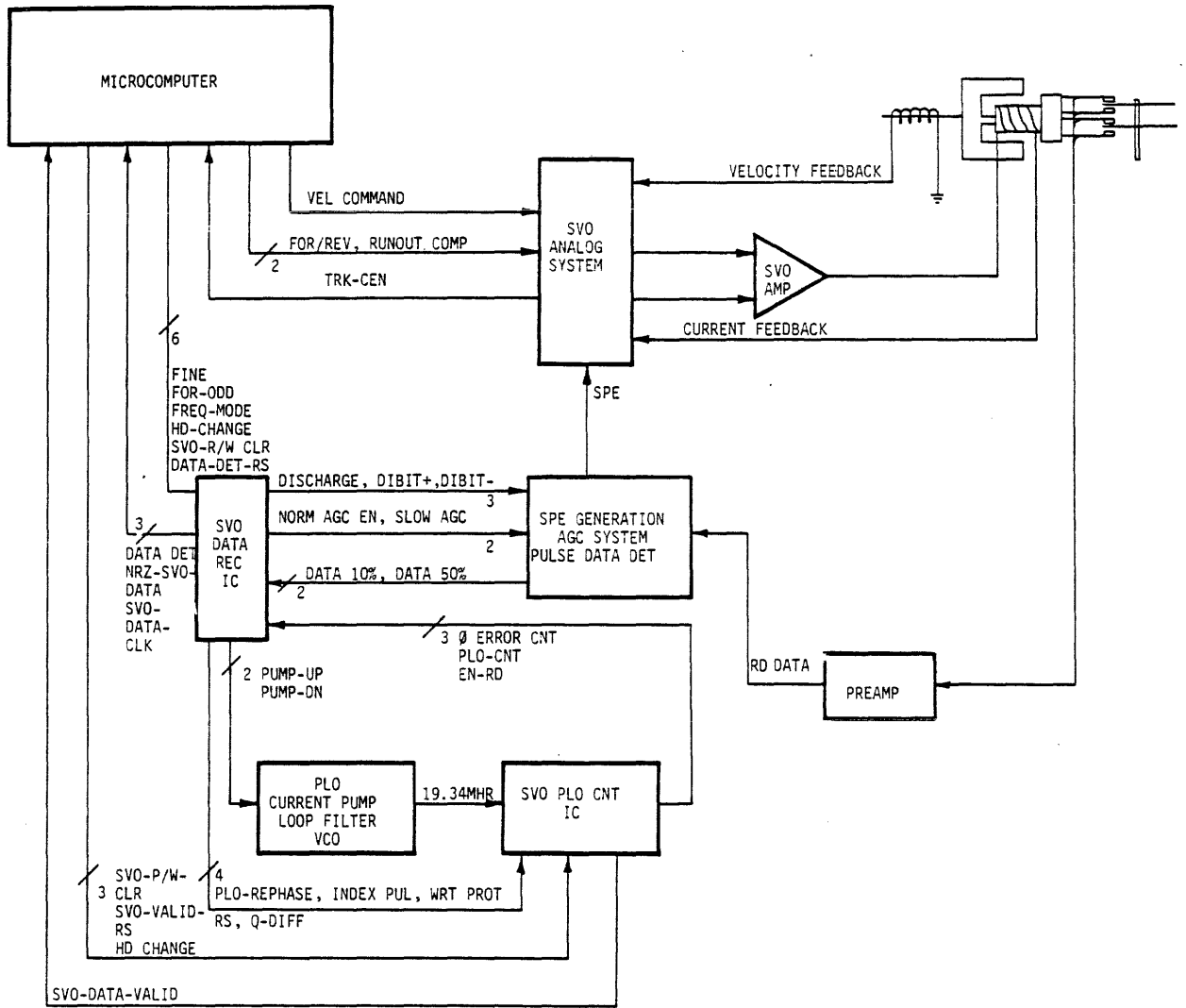
Phase Locked Loop (PLL) - This includes the PLO (current pumps, loop filters and VCO), the phase detector in the SVO DATA REC IC, PLO counter in the SVO PLO CNT IC, and the phase detector in RD/WRT Digital IC. Emphasis is placed on the PLO discussion including loop dynamics where as the digital blocks are discussed in detail under Servo Digital and RD/WRT Digital.

Servo Sample Demodulator - This is the sample and hold circuit which produces SPE using the timing signals provided by the Servo Data Recovery IC. The AGC system is also discussed.

Positioning Firmware (Microcomputer) - The MC provides coarse seek control by producing the velocity command as a function of the distance to go. Also, it provides initialization of the PLL and serves as status monitor during seek.

Positioning Hardware - This includes the servo loop analysis/velocity command D/A converter, summing AMP, loop compensation and the actuator power AMP.

For details of the contributions made to the positioning system by the Read/Write Preamp and Read Signal Processing PWAs, refer to Section 4.3.6.8 and 4.3.6.9.



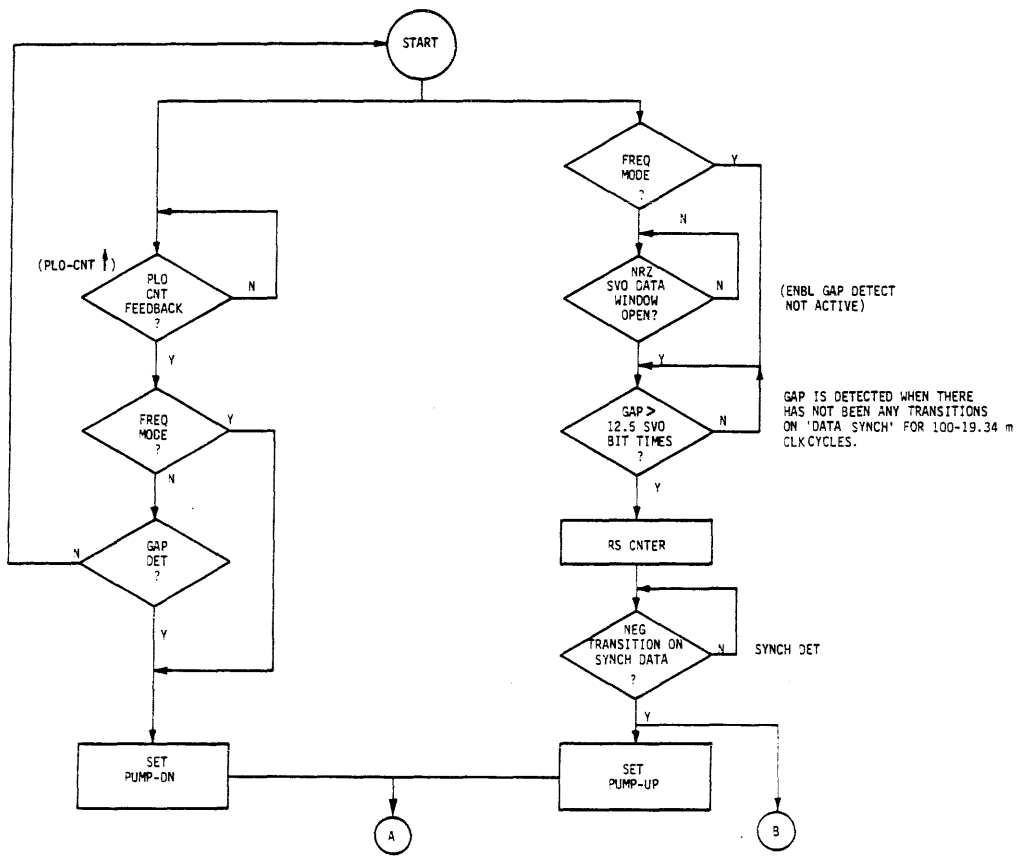
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FIGURE 4-25. POSITIONING SYSTEM OVERVIEW

SERVO DATA RECOVERY LSI CIRCUIT

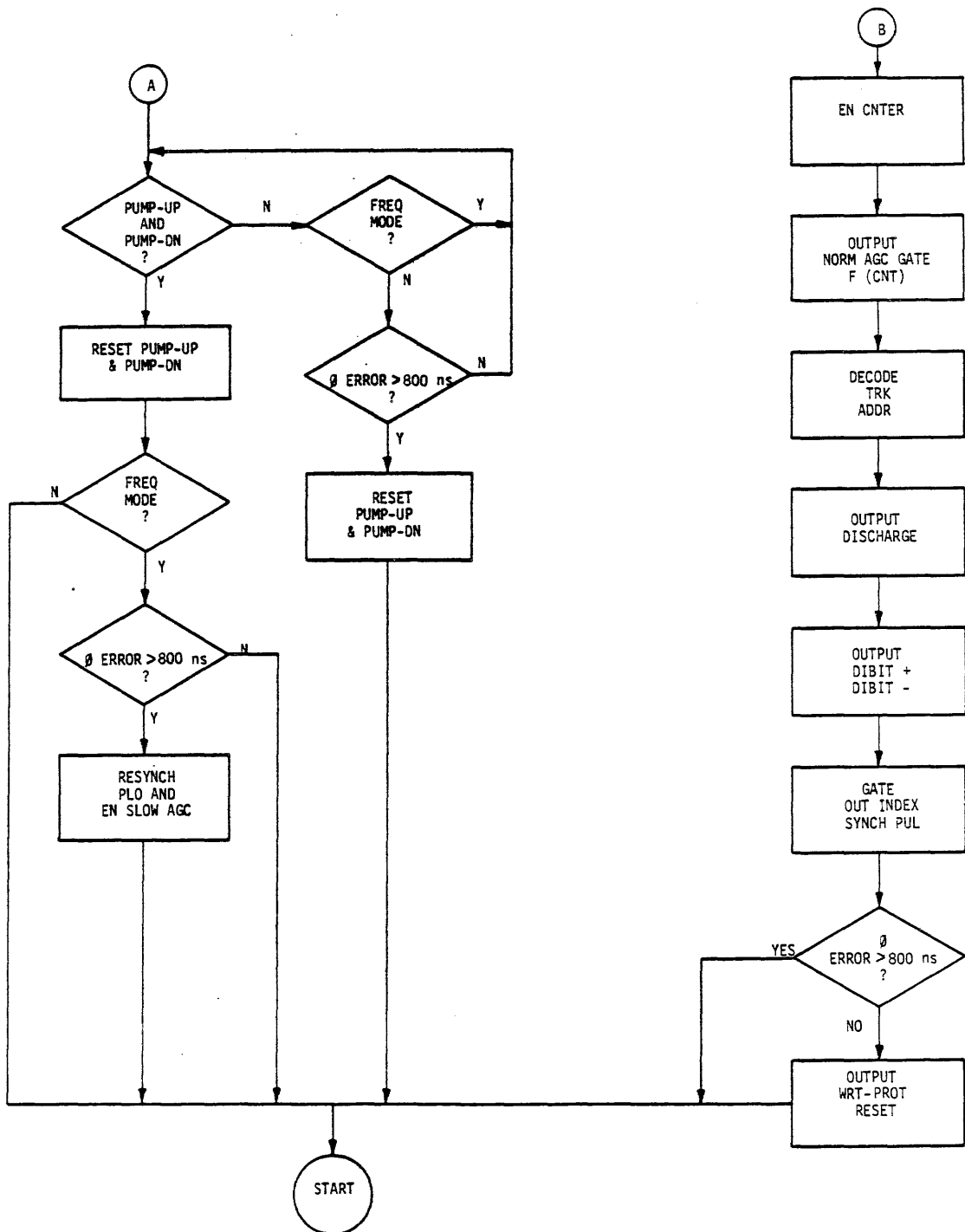
The servo data is recovered primarily in the 40 pin ECL I.C. U46 under control of the microcomputer. Refer to diagram, Figure 5-1. Also, see Appendix of this Section for a description of each I/O pin function.

Basically this IC provides two functions--recovery of SVO data and PLO phase detection. See flowchart, Figure 4-26. After the GAP and sync bit are detected, a counter produces timing signals which provide a gate for the AGC field, track address decode, a discharge pulse and gates to recover a discharge pulse and gates to recover the SVO fine information, an Index gate and a WRT PROT RS pulse. This timing is shown in Figures 4-30 and 4-31. At the same time a phase comparison is made between the PLO feedback counter and the embedded SVO data which serves as the media timing reference. This phase comparison is fed into the PLO loop via the PUMP-UP and PUMP-DN outputs. A special mode is required for initial PLO lock called "FREQ MODE". In the normal mode the \emptyset error (maximum length of either pump-up or pump-dn) is limited to 800 ns and a PUMP-DN output must be preceded by a gap detection. These requirements minimize the effect of missing SVO zones or incorrect sync detection on the PLO loop. In the frequency mode the \emptyset error is not limited but if over 800 ns, a PLO counter re-sync is initiated and the slow AGC is enabled. In either mode if the \emptyset error is greater than 800 ns, the WRT-PROT-RS is inhibited causing the following data sector to be WRT protected.



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FIGURE 4-26. SERVO DATA RECOVERY FLOWCHART (SHEET 1 OF 2)



77228

FIGURE 4-27. SERVO DATA RECOVERY FLOWCHART (SHEET 2 OF 2)

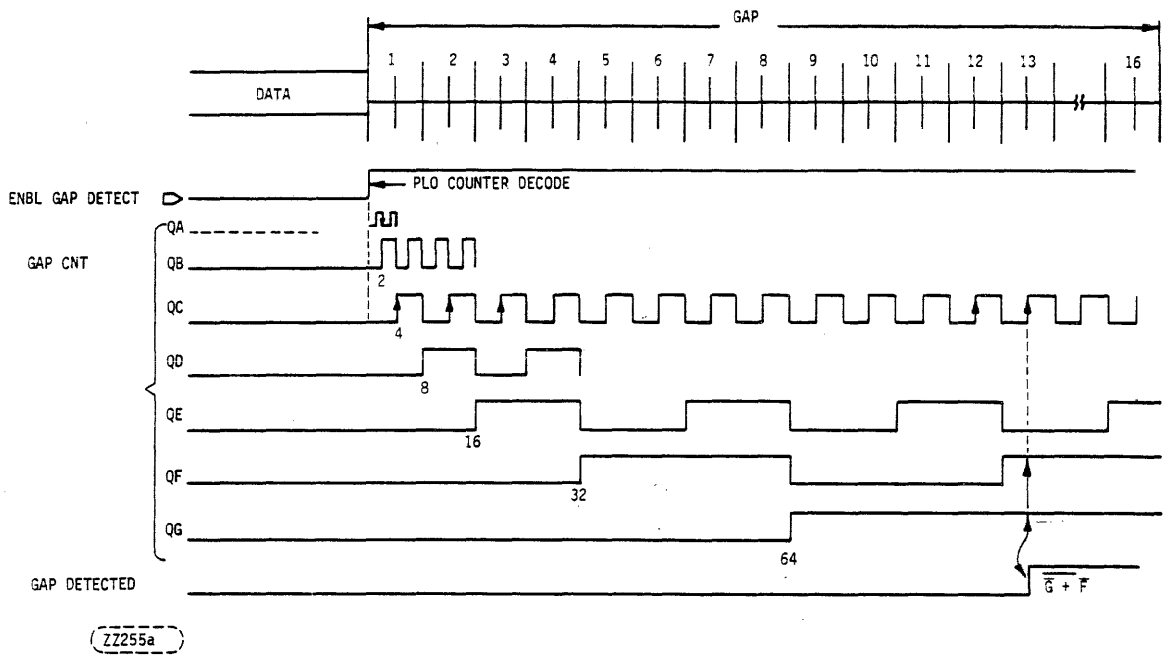


FIGURE 4-28. GAP DETECTION

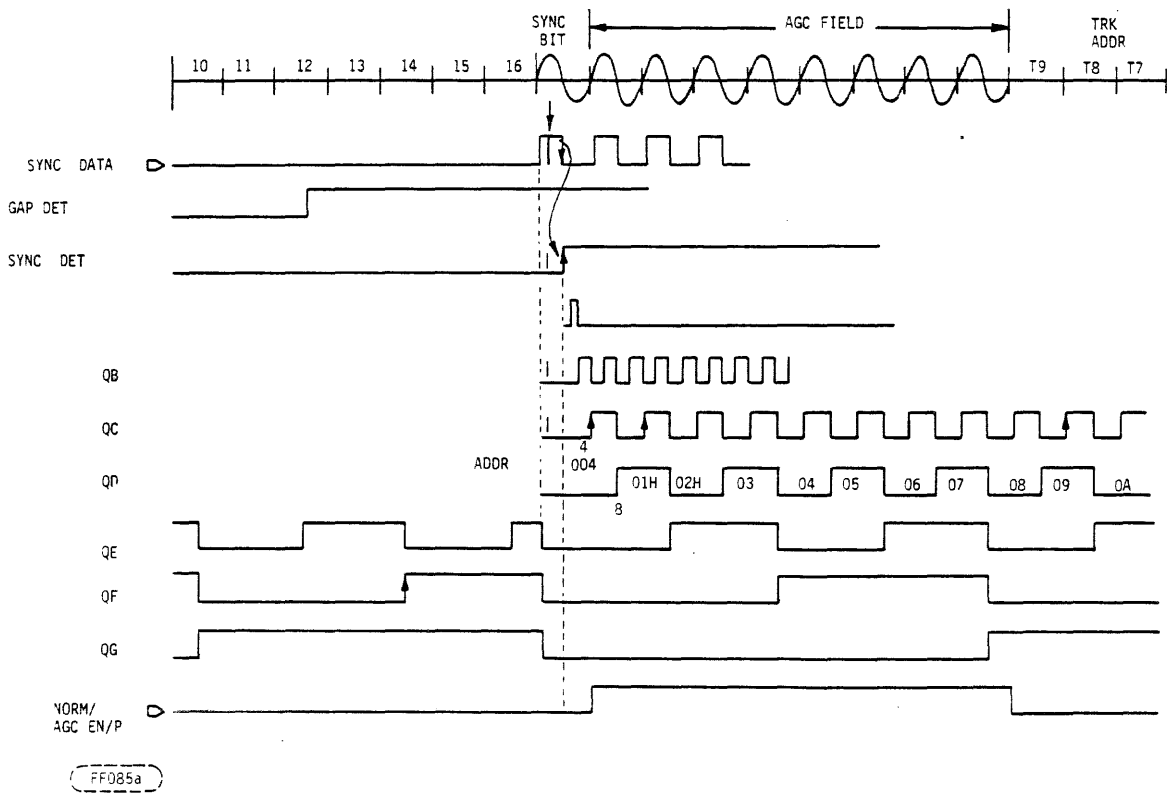


FIGURE 4-29. SYNC DETECTION

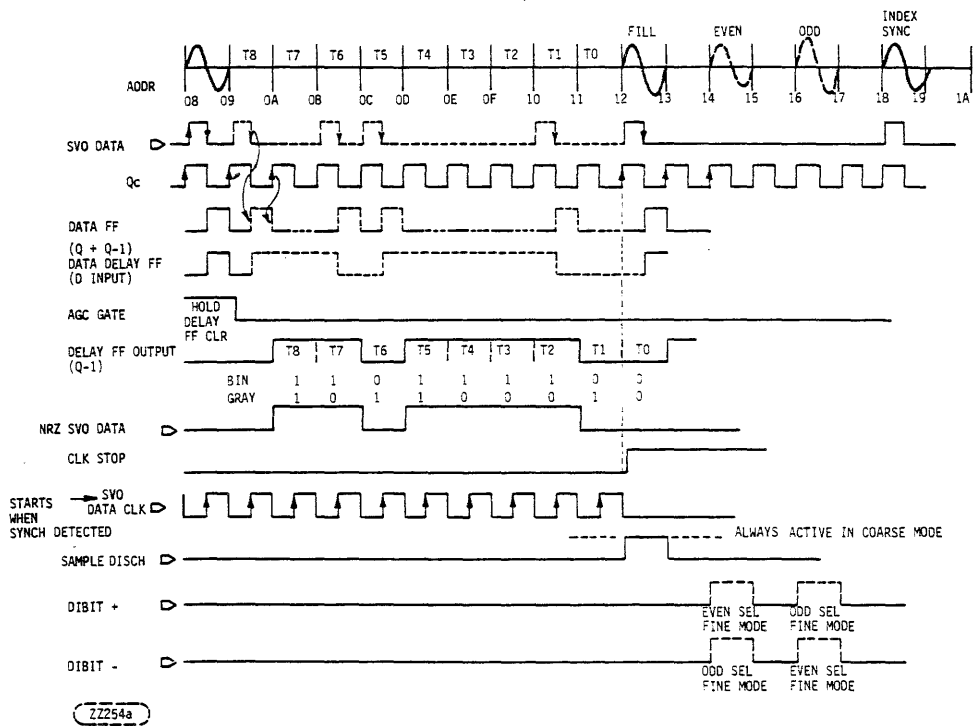


FIGURE 4-30. SVO DATA RECOVERY

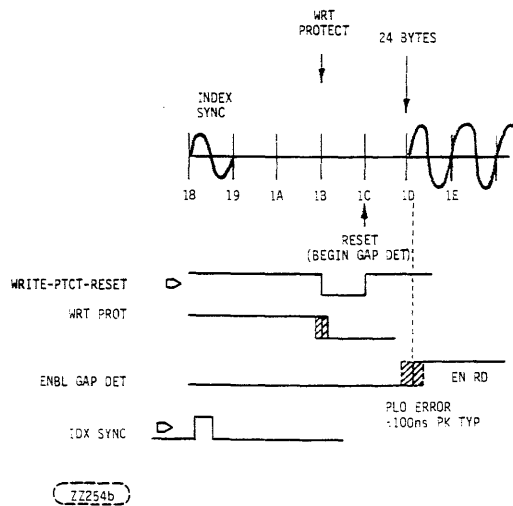


FIGURE 4-31. INDEX SYNC AND WRT PROT RS

SERVO-PLO-CNT LSI CIRCUIT

The SVO PH LOCK OSC CNTR (U39) contains the Servo PLO counter, Servo write protect window, read enable window, the Ph Error Counter and Sector/Index generation.

The PLO counter counts to -10336. Several decodes are taken from this counter to produce timing for RD/WRT control. See Figures 4-32 and 4-33.

Also, the Sector/Index timing is taken from the PLO counter which is locked to the disk SVO data zones. This guarantees Sector/Index without recovering every SVO data zone. The Index Sync logic synchronizes the embedded SVO data Index pulse to the sector counter. See Figures 4-34 and 4-35.

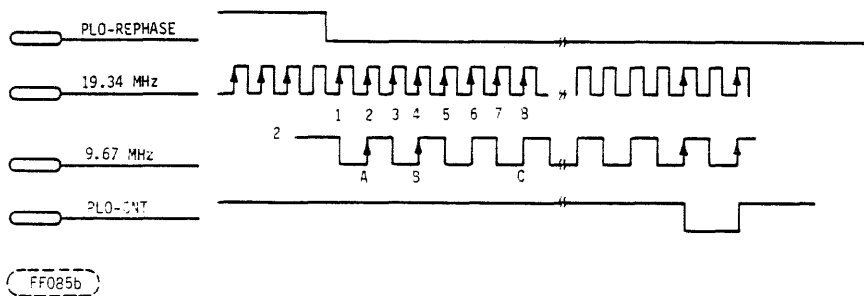


FIGURE 4-32. PLO INITIAL CNT

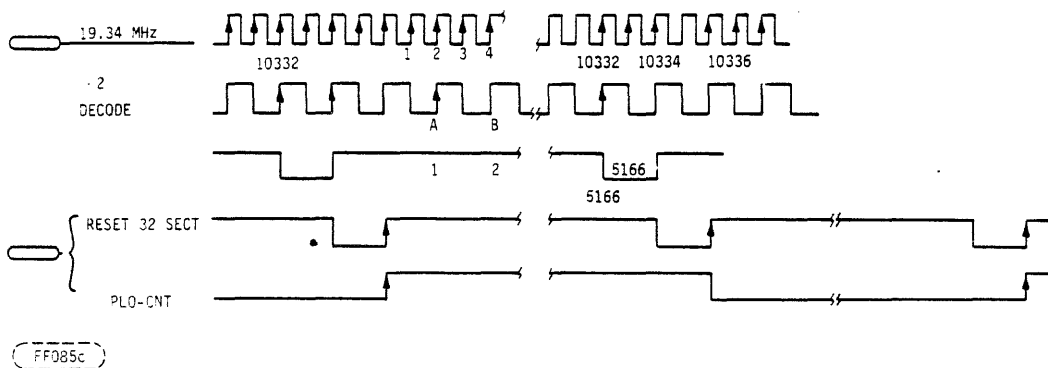


FIGURE 4-33. PLO COUNT FOR 32 SECTORS

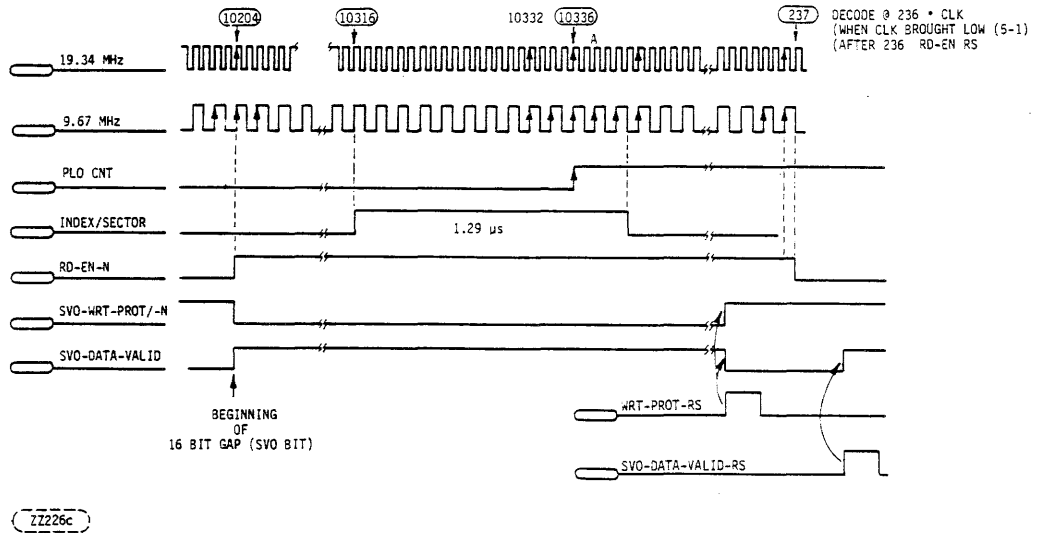


FIGURE 4-34. PLO SECTOR TIMING

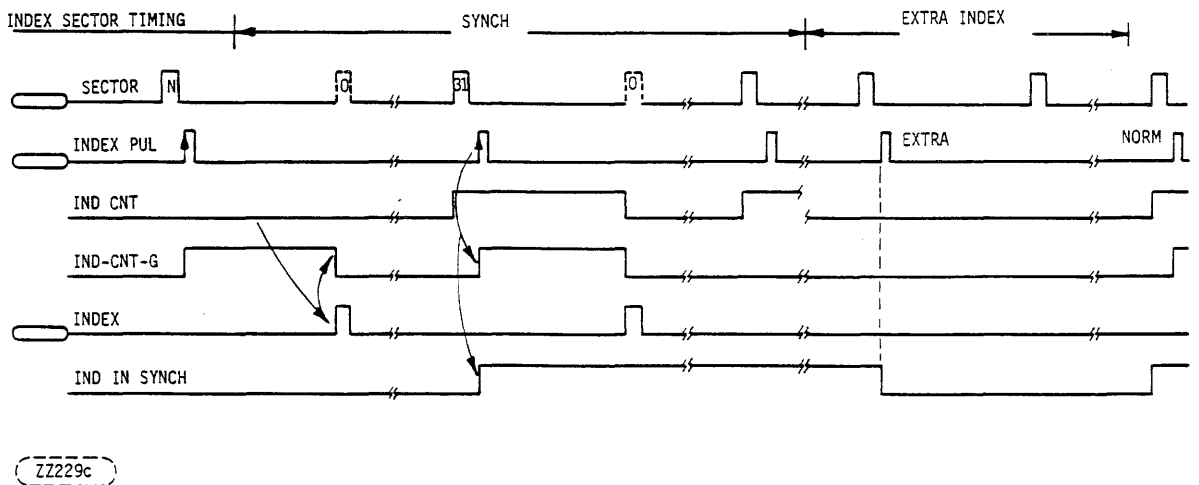


FIGURE 4-35. INDEX SYNC

4.3.4.5 POSITION SYSTEM THEORY - ANALOG CIRCUITRY

GENERAL

Seek operations are performed by the positioning servo system of the LMU which is made up of both digital and analog circuitry. The details of most of the digital portion are covered in Sections 4.3.2 and 4.3.4.4 which describe the Microcomputer and auxiliary digital circuits. This section discusses mostly the operation of the analog portions with occasional references to microcomputer and other digital circuitry where applicable. See Figure 4-35. Certain functions related to but not directly involved in positioning will also be described in this section.

The positioning servo system of the LMU is a closed loop servo system containing a position loop, a velocity loop, and a current feed back loop representing acceleration. Figure 4-37 is a simplified block diagram of the LMU servo system. Figure 4-38 is a detailed block diagram of the servo system. The velocity, compensation and acceleration loops are analog while the position loop is a combination of digital and analog circuitry.

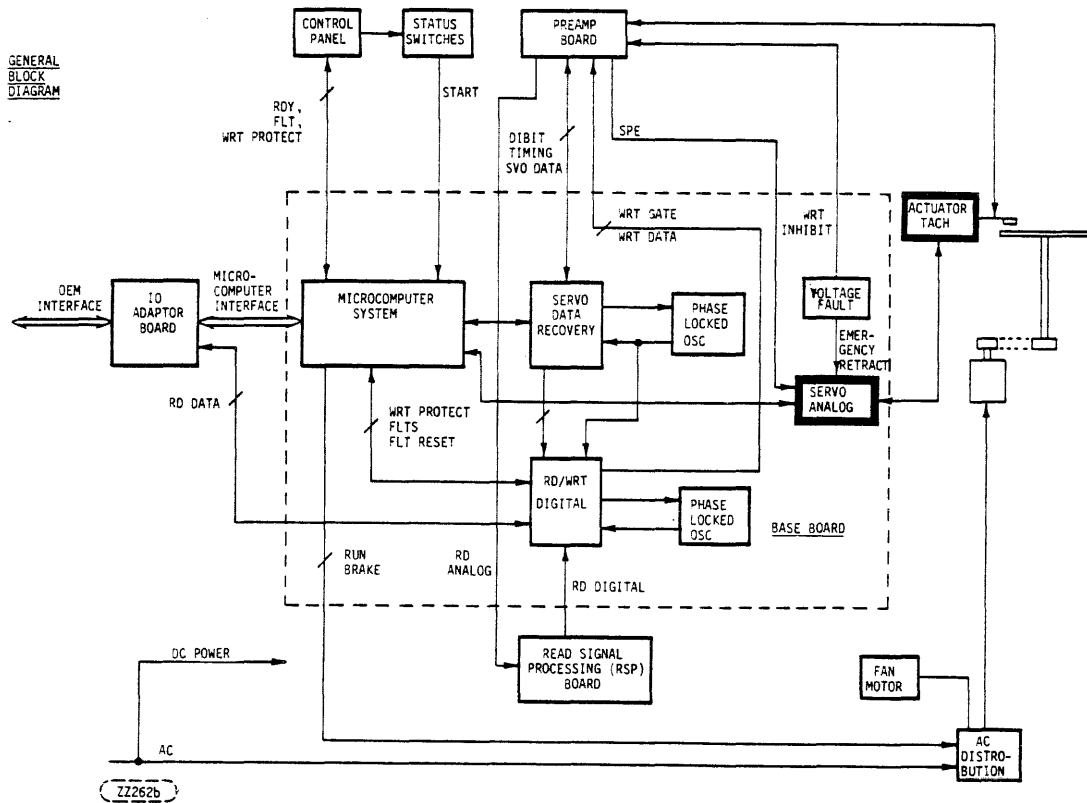


FIGURE 4-36. GENERAL BLOCK DIAGRAM EMPHASIZING SERVO ANALOG CIRCUITS

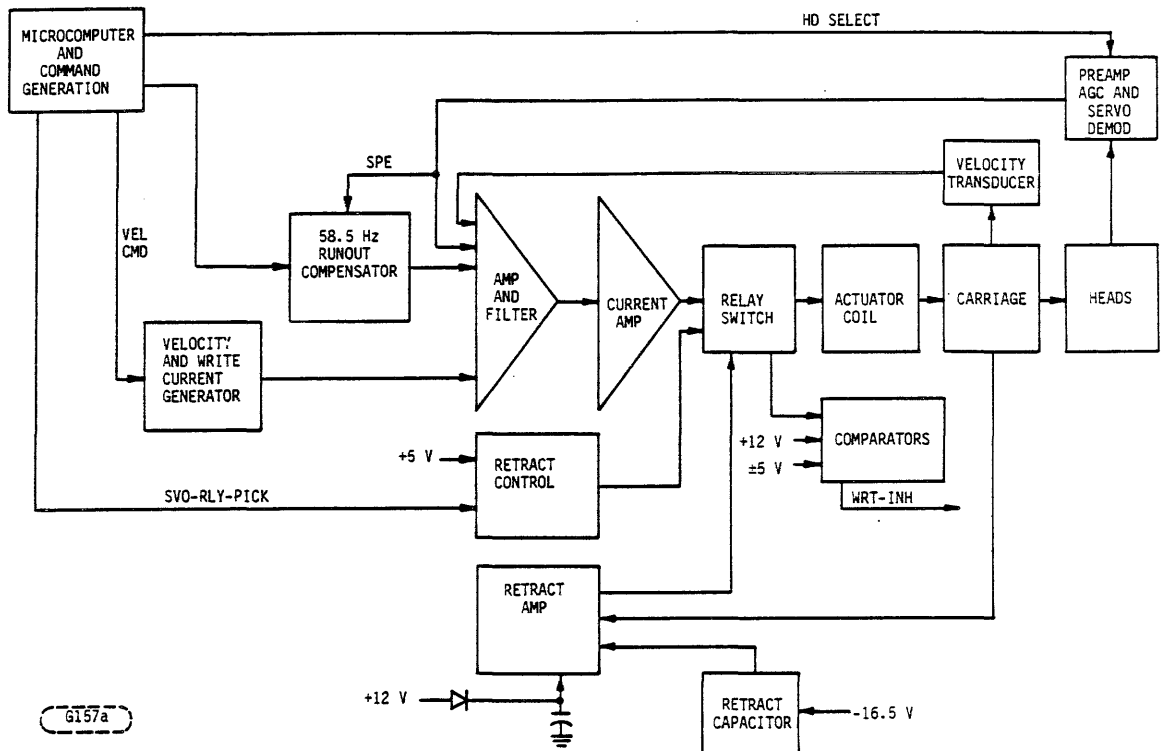


FIGURE 4-37. SIMPLIFIED SERVO SYSTEM ANALOG BLOCK DIAGRAM

SERVO ANALOG OPERATION DETAILS

The Servo-Analog circuits provide the following circuit functional groups (refer to Figures 4-37 and 4-38):

- Position velocity and offset command generation
- Actuator drive circuitry
- Servo system velocity feedback circuitry
- Servo system current feedback circuitry
- Actuator retract (unload heads) circuitry
- Compensation circuitry
- Track center detection circuitry
- Spin speed pulse generation circuitry

The details of the first item above are described in detail in Section 4.3.2. Details of the other nine items are described in paragraphs which follow. Unless specifically noted, all schematic references in Section 4.3.4.5 are to sheets in the Base PWA schematic found in Section 5.

ACTUATOR DRIVE CIRCUITRY

For purposes of this description the actuator drive circuitry is considered to consist of the velocity and write current generator, the summation amplifier, the 5.1 kHz notch filter, the pre-driver op amp, the driver amp, and the power amp. All of the above items are located on the Base circuit board.

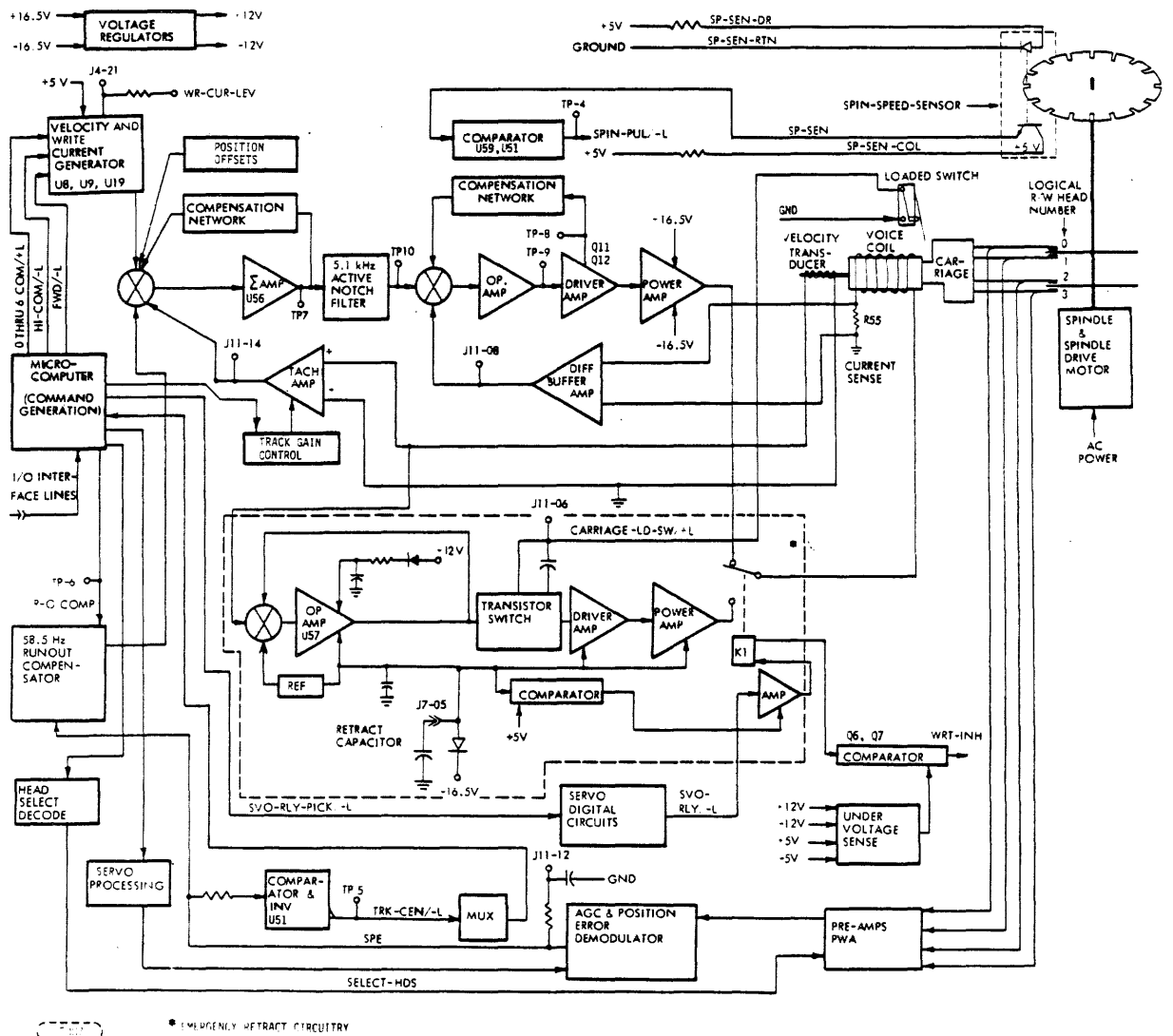


FIGURE 4-38. DETAILED POSITIONING SYSTEM BLOCK DIAGRAM

The velocity/write current generator is located on the Base PWA, Sheet 9. It is made up of the D/A converter U54, two op amps U56 and analog switch IC U55. The velocity/write current generator provides approximately sixteen different levels of velocity that can be commanded from the microcomputer by proper activation of the COM-0/+L through COM-6/+L lines to the D/A converter and by choosing between two different resistances on the second U56 amplifier output. The least significant bit of the D/A converter is not used to provide greater stability in the low end of the two velocity ranges. In operation, precision resistor R114 is connected in parallel with R113 by analog switch U55-6, 7, 8 to provide the higher velocities of the 16 velocities that the velocity/write current generator commands. COM-HI/-L when active low closes the analog switch U55-6, 7, 8 to allow a higher range of currents to be input to the summing amplifier U61. The velocity/write current generator can be commanded (COM-0/+L thru COM-6/+L and COM-HI/-L) to control R/W current as a function of track address. Direction is determined by FWD-SK/+L and REV-SK/+L which control switch U55. The D/A output is inverted through inverting amplifier U56-7 when REV-SK/+L is logic 1 (high). When FWD-SK/+L is logic 1, the signal is non inverting. When both REV-SK/+L and FWD-SK/+L are "Low" U56-7 output is zero allowing write current levels to be set at J4-21 without servo interference. A positive signal (FWD-SK/+L high) places the heads closer to the spindle center.

ACTUATOR RETRACT (UNLOAD HEADS) CIRCUITRY

The actuator retract circuitry is located on the Base PWA, Sheet 11. It operates in a way that provides a controlled retract velocity current to the actuator voice coil. Proper control of the retracting of the heads prevents head-arm vibration that would cause head to disk contact when the head cam surfaces contact the head unload ramps during retract. Proper control is also needed to prevent the carriage from banging into the stops at the actuator magnet. Low power op amp U66 controls the retract velocity of the carriage in the following manner. Resistor R219 (on U66 pin 8) programs the quiescent currents within the op amp U66 so that capacitors C138 and C149 can hold enough charge after power is lost to allow retraction to be completed at the proper rate. CR13 operates as a velocity voltage reference and U66 compares the velocity signal directly from the velocity transducer with the reference voltage at U66-2 and thereby limits the drive current provided to transistor Q16. The amplifier chain Q9 and Q14 and Q16 will not drive the actuator beyond the proper velocity, but due to the small amount of current C138 and C149 must furnish, the retract velocity is uniform. The emergency retract power is supplied to Q9 by the energy stored in a large retract capacitor.

The signal CARRIAGE-LD/+L switches off the drive to Q14 and Q16 when the carriage actuates the heads loaded switch. The large retract capacitor can then charge to a nominal 16 volts. Zener diode VR8 and transistor Q15 detect that the retract capacitor is charged and turns on Q13 which pulls in relay K1. WRT-INH/+L from Q5 resets the UNSAFE latch. The microcomputer does not allow the heads to be loaded again until UNSAFE has been reset, indicating that the capacitor is adequately recharged. The comparators in U52 (Base PWA, Sheet 12) also sense incorrect voltages and set the UNSAFE latch when they are out of tolerance. A low voltage zener diode VR6 and transistor Q15 deactivate K1 if the +5 V logic voltage drops. This will cause an emergency retract before the logic voltage drops completely.

COMPENSATION CIRCUITRY

The Power AMP compensation feedback network around U63, Q11 and Q12 (C144, R203 sheet 11) is essentially a rolloff filter, to control the gain and bandwidth of the current loop and to reduce the deadband non-linearity of Q11 and Q12.

The U61 feedback network (on sheet 10) controls the gain and rolls off the velocity loop response a limited amount to aid in attenuating the loop gain at the mechanical resonant frequencies in the carriage and velocity transducer.

Following U61 is an active notch filter at U63, centered near 5.1 kHz. The notch filter provides additional attenuation of signals in the vicinity of the notch center frequency which otherwise would be greatly accentuated due to the mechanical resonances of the carriage and velocity transducer.

The 58.5 Hz runout compensation circuit (on sheet 10) consisting of U56 essentially produces an increase in gain for the SPE signal (switched by U55) in the band around 58.5 Hz. The increase in gain takes effect after the last 1/2 track of a seek operation after track center is first made active. This allows the servo system to remain on track when using a servo signal modulated by an eccentric track caused by mechanical imperfections in disk and spindle. On the LMU with a spindle rotation of 3510 r/min eccentricity in the track will pass under the heads 58.5 times a second, thus causing an amplitude variation in the servo signal that is centered around 58.5 Hz.

The signal RUNOUT-COMP/-L operates the analog switch U55-9, 10, 11 thereby adding or removing the 58.5 Hz runout compensation circuit in series with the SPE signal. When RUNOUT-COMP/-L is active low, the 58.5 Hz runout compensation is connected in the circuit.

A basic block diagram for the servo position loop is shown in Figure 4-38. The position servo system utilizes the velocity transducer that is used in the track seeking mode. A low frequency lead/lag compensator in the feedback of the velocity loop appears as a lag/lead compensator in the forward position loop. A reciprocal lag/lead compensator in the forward velocity loop stabilizes the wide band velocity loop.

The velocity loop gain in Figure 4-39 shall be equal to $(K)(W_X) = (A_V)(A_G)(1/M)$ radians per second and $A_{P1} = A_V (W_X) (W_2) / W_1$ volts per inch.

The capacitors located in the W_1 and W_2 compensation networks are automatically precharged during the seek mode by the velocity command loop prior to closing the position loop. Care has been taken to insure that these capacitors are not improperly charged by saturated or non linear signals.

TRACK CENTER DETECTION CIRCUITRY (SHEET 10)

TRK-CEN/-L is a logic signal that is active low when the heads are positioned within prescribed offset limits. TRK-CEN/-L goes active low when the SPE signal does not exceed the positive or negative threshold voltage required to generate a digital output from the D/A comparators U64-13 and U64-2. SPE is generated only when the microcomputer activates the FINE/+L signal, indicating that the heads are very close to being on track.

SPIN SPEED PULSE GENERATION CIRCUITRY (SHEET 10)

The spin speed pulse generation circuitry consists of an optical sensor which senses the presence of 16 slots in a disk on the bottom of the disk drive spindle, and a comparator circuit. The optical sensor consists of a light emitting diode and a light sensing transistor which senses the infrared light from the diode as the light passes through one of the 16 slots in the slotted disk. Comparator U64-1 squares up the edges of the pulse from the light sensing transistor and sends the pulse to the microcomputer input "TO" where it can be tested periodically by the firmware. The waveform expected is shown in Figure 4-40. The times shown are approximate and are not critical. Speed tolerance of $\pm 5\%$, slot mechanical tolerances, and electronic component tolerances will cause the actual signal to vary somewhat from the figure shown. The waveform is shown here for general information only, since no adjustment can be made to alter it.

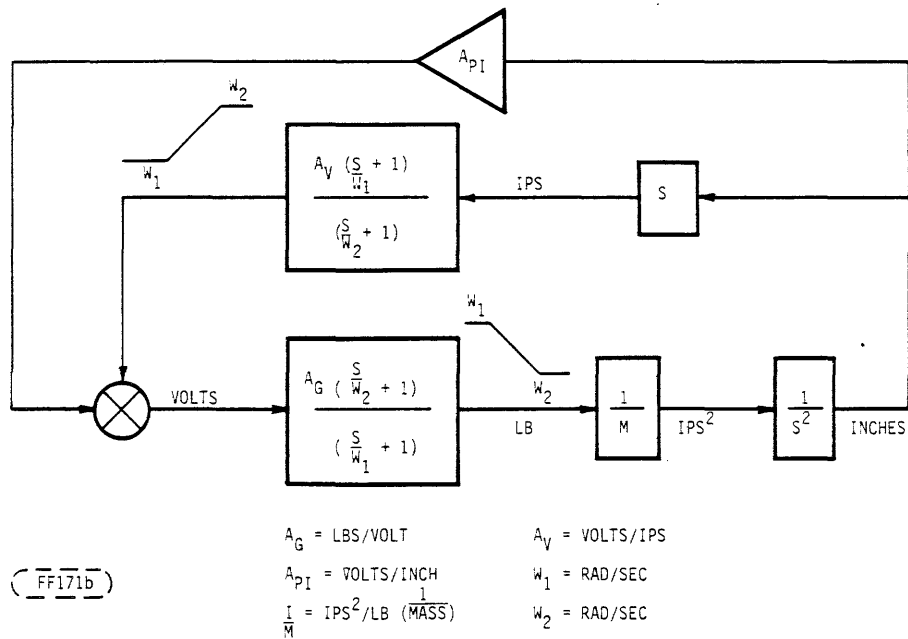


FIGURE 4-39. SERVO POSITION LOOP BLOCK DIAGRAM

SERVO POSITION OFFSETS (Figure 5-4 Sheet 10):

The track position may be offset slightly from track center to aid in recovering marginal data. When "Off +" is active high, U63-7 will drive the actuator off track toward the spindle. "Off -" will provide a slight offset away from the spindle when active high.

TACH GAIN ADJUSTMENT (Figure 5-4 Sheet 9):

The gain of the velocity feedback from the velocity transducer (or tach) may be adjusted by switching resistors into the U58 non-inverting gain path. The analog switches at U60 are controlled by U62 binary counter. The gain is increased slightly each time the microprocessor toggles "0.5-CLK/-L". See the last paragraphs under HEAD LOADING in Section 4.2.1.4 for further details.

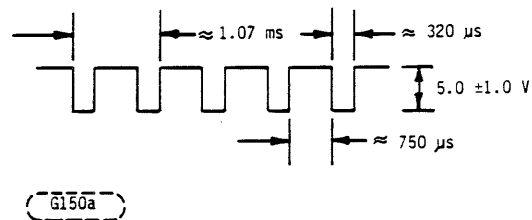


FIGURE 4-40. SPIN SPEED PULSE

4.3.5 READ/WRITE SYSTEM

4.3.5.1 READ/WRITE LSI OVERVIEW

The overall block diagram of Figure 4-41 shows the relation of the Read/Write circuitry to the remainder of the LMU circuitry. Figures in Section 5-6 show the Read/Write and format timing of the data read on or written from a typical disk sector. Figure 4-42 shows the Read/Write digital circuits. The two R/W LSI chips; the R/W-Contr and the R/W-Enc/Dec, contain all the necessary logic to implement the 2,9 code in two 40 pin packages. The R/W-Contr contains the R/W fault logic and the logic needed to generate the proper timing signals used by the R/W-Enc/Dec and the read PLO. The R/W-Enc/Dec contains the flux and NRZ shift registers along with the encode and decode combinational logic. The following diagrams show the major logic blocks for the R/W-Contr and R/W-Enc/Dec. The input/output lines are labeled with their appropriate names and pin numbers.

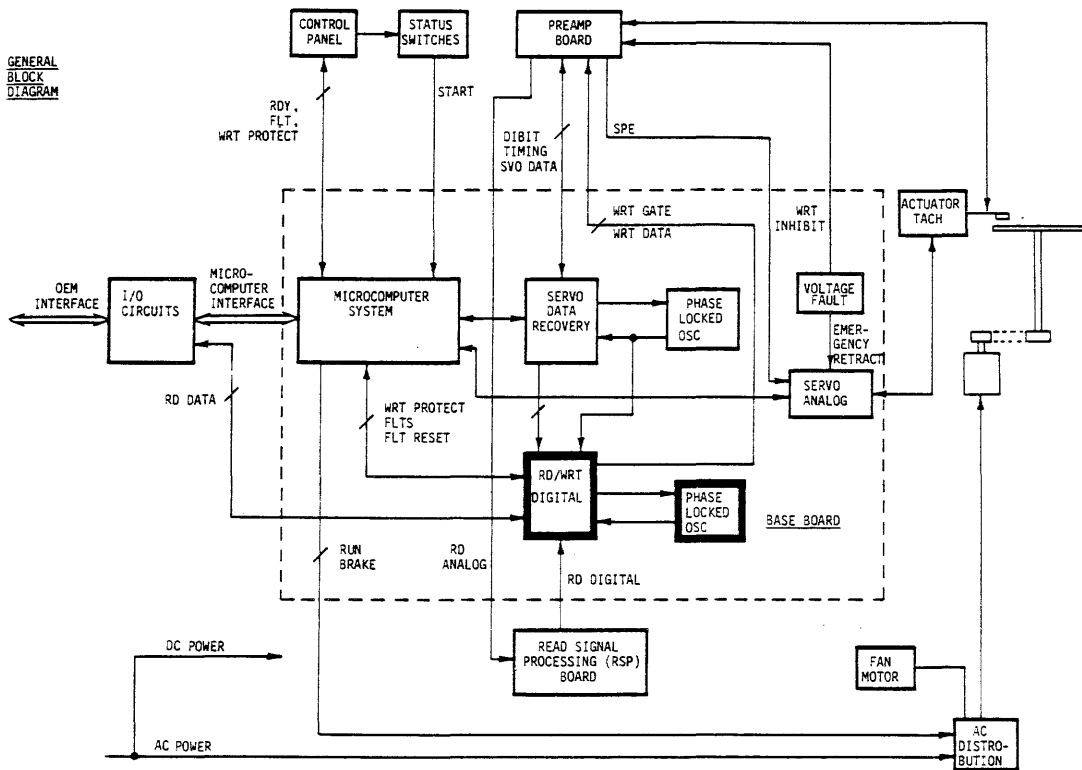
During a write, the R/W LSI takes three interface data bits and encodes them into one of seven combinations of flux reversals that are loaded into the flux register. The flux register is shifted out to the write driver. The write driver writes a flux reversal for each positive going edge received from the flux register.

A read operation takes the pulse data from the read signal processing board and shifts it into the flux register. The flux reversals are then decoded, three data bits at a time, and loaded into the NRZ shift register to be transferred out as RD DATA. Because of these shift registers, the R/W LSI have delays that must be accounted for during a write or read operation. The pads at the end of the address and data fields are used for this purpose.

4.3.5.2 LMU DATA CODE (2,9)

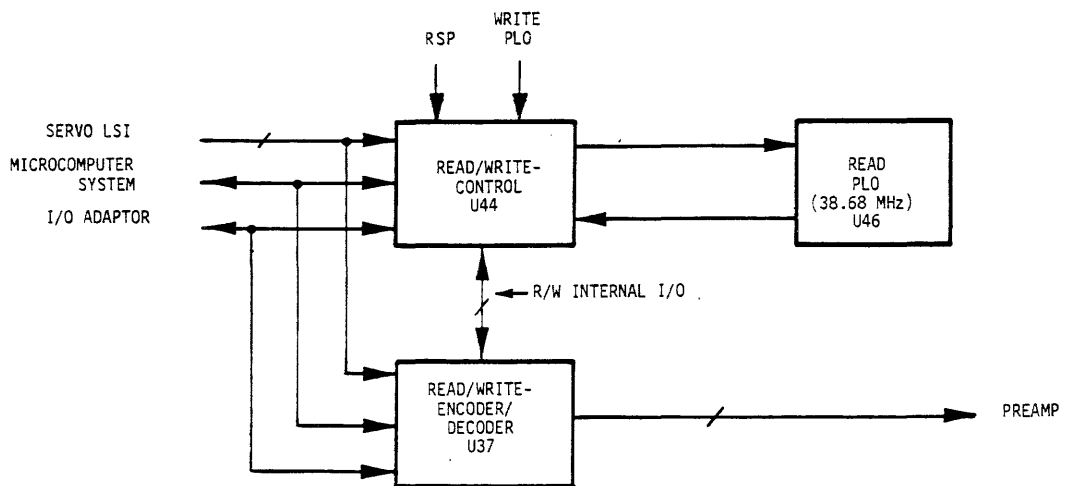
The code chosen for the eight-inch LMU rigid disk drive is the 2,9. This code is included in the family of modulation codes that are used in digital recording the same as MFM. These codes are in general categorized into run length limited codes (RLL codes). RLL codes take "M" data bits and convert them into "N" code bits. The value for "M" for MFM is one and for the 2,9 code is three, the value of "N" is equal to two and six respectively. These codes are such that any two consecutive ones are separated by at least "D" zeroes and no more than "K" zeroes. The value of "D" for MFM is one for the 2,9 code is two and the value of "K" is three and nine respectively. The detection window as related to the data cell is the ratio of "M" to "N". This ratio is the same for MFM and the 2,9 code (0.5). There is no loss in the detection window between the two codes, but the 2,9 code has increased the number of code bits from two to three per flux position.

This makes the efficiency of the 2,9 code 1.5 times that of MFM. That is, we can record fifty percent more data in a given area with the 2,9 code than with MFM.



Z2250a

FIGURE 4-41. OVERALL BLOCK DIAGRAM - RD/WRT DIGITAL AND PLO EMPHASIZED



Z2258a

FIGURE 4-42. READ/WRITE DIGITAL

4.3.5.3 READ/WRITE LSI I/O DESCRIPTION

Figures 4-45 and 4-46 show block diagrams of the two Read/Write LSI chips. All inputs and outputs of the two R/W LSI are 10K ECL compatible. The outputs are loaded with 500 ohm or 1 K ohms to -5 V depending on the speed required. The three test points on the R/W Control LSI are not capable of driving any load. They are to be used as scoping test points only. Eleven I/O signals are generated and used exclusively by the R/W LSI. These signals will be grouped together and described as internal I/O. These signals are very useful to "see" what is taking place between the R/W LSI pair.

Internal I/O

- WRITE/RD - Generated by R/W ENC/DEC and is the OR-ed function of WRITE GATE ENBL and RD CMD. It controls a ÷ 6 counter and the nine bit flux register.
- FORCED RESET 5 - Bit 5 of the nine bit flux register.
- SYNC - It is a decode off the nine bit flux register. SYNC along with FORCED RESET 5 is used to generate DXFER and the rephasing of the ÷ 6 counter.
- RD T - A delayed function of RD CMD or RD ENBL by 48 bit times.
- DCD T - A 51 ns pulse decoded off the ÷ 6 counter occurring every 310 ns during a write or a read. It is used by the R/W-END/DEC for read decoding.
- DATA XFER - Enables valid data in the NRZ shift register to be shifted out of RD DATA. The rising edge of DATA XFER is in sync with the analog read signal.
- RETIMED PLS DATA - RD PLS DATA retimed to the read PLO during a read. It is input to the flux register.
- INTL CLK - 19.34 MHz clock used internally in both R/W chips.
- SHF CLK - 9.67 MHz clock decoded off of the ÷ 6 counter. It is used by the R/W-ENC/DEC to clock the NRZ shift register.
- ENCD T - A 51 ns pulse decoded off the ÷ 6 counter occurring every 310 ns during a write operation. It is used by the R/W-ENC/DEC for write encoding.
- ONES ENBL - Forces the R/W-ENC/DEC to write an all 1's pattern for 66 bit times at the beginning of the PLO sync field.

4.3.5.4 READ/WRITE-CONTROL I/O DESCRIPTION

Inputs

- RD CMD - Read command from the interface, active low.
- WRITE CMD - Write command from the interface, active low.
- SGL - Always LOW. Used for test purpose.
- RD PLS DATA - Flux reversals in the form of pulse data received from the read signal processing board.

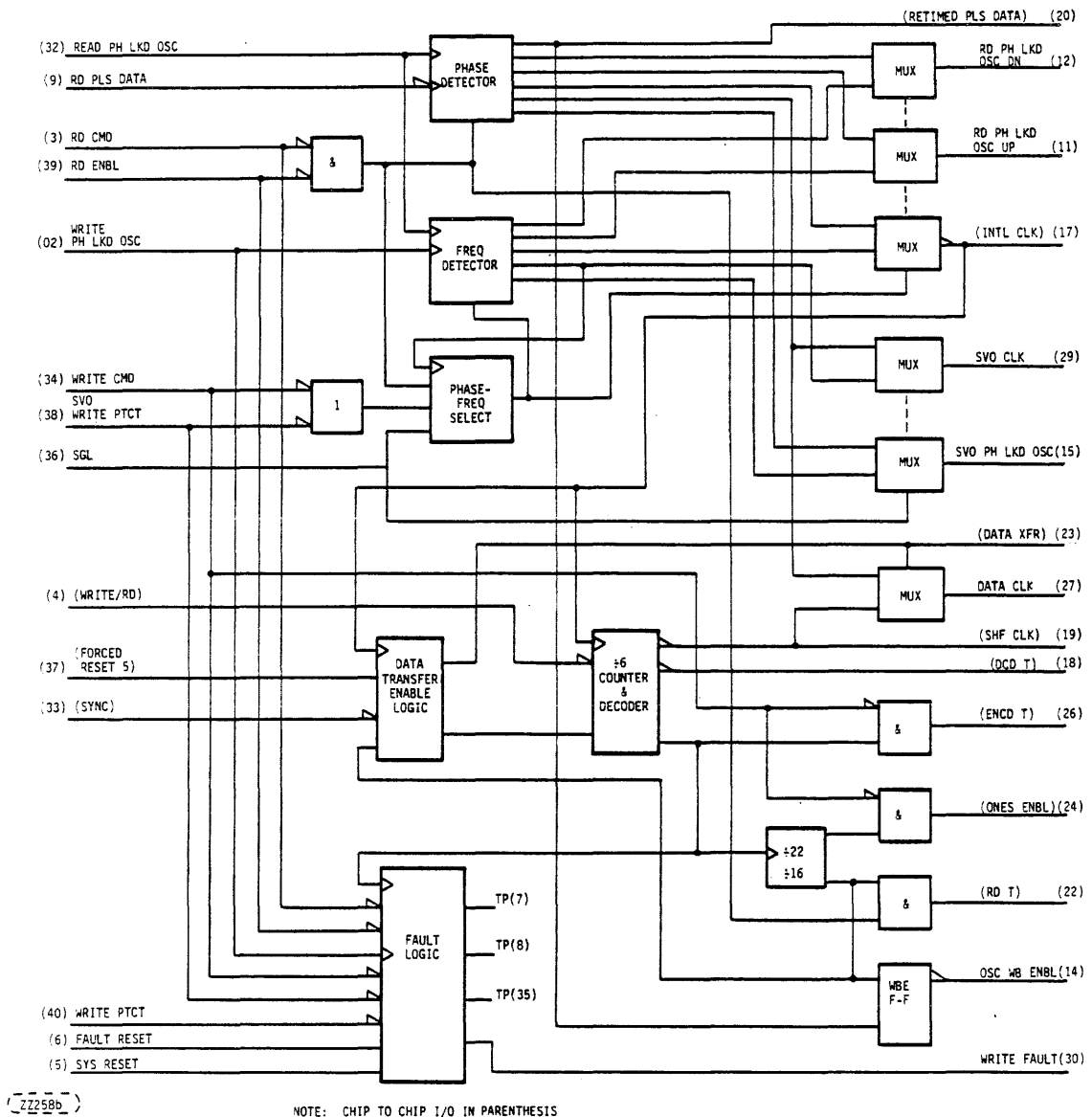


FIGURE 4-45. READ/WRITE CONTROL-50

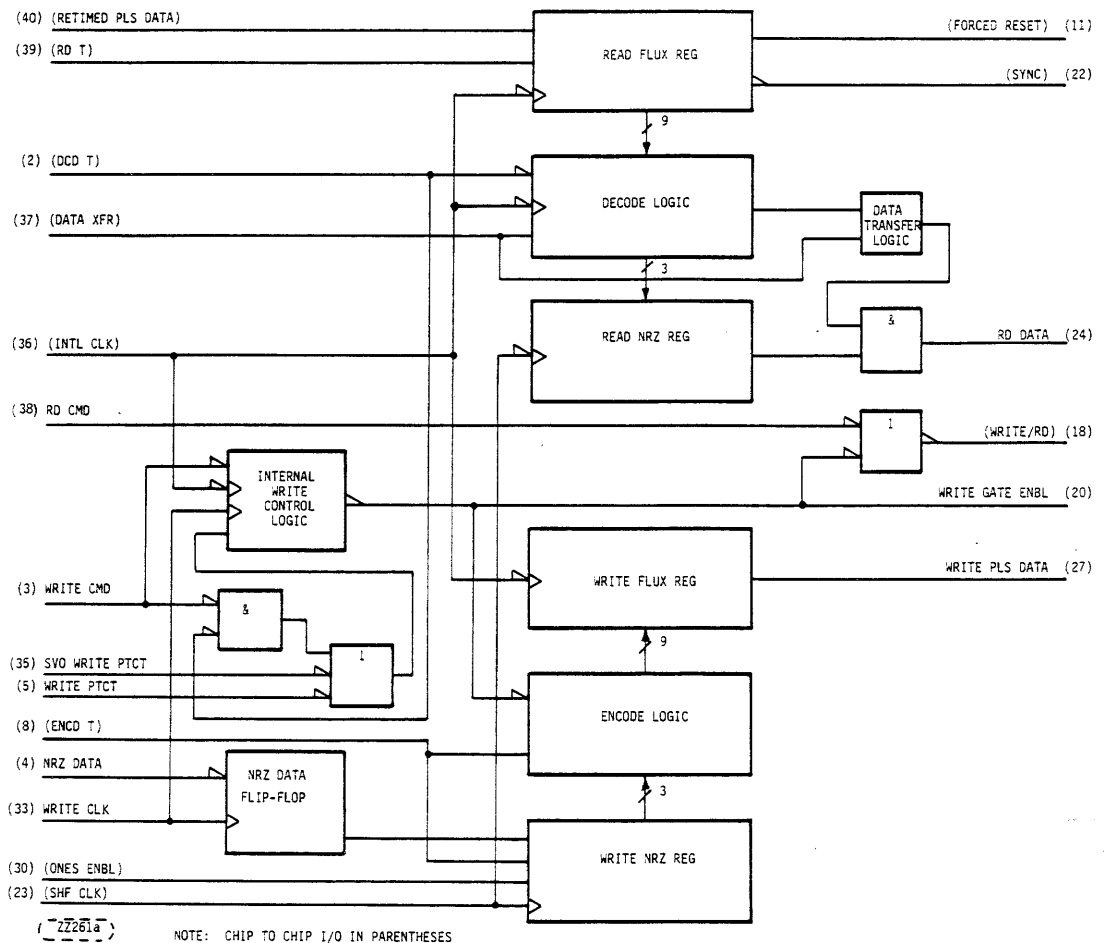


FIGURE 4-46. READ/WRITE ENCODER/DECODER

- RD ENBL - Active low signal from the SVO LSI enabling a read after the header write splice.
- SVO WRITE PTCT - Active low signal protecting the embedded servo field.
- WRITE PTCT - Active low signal created by the microcomputer to disable the write function.
- FAULT RESET - Resets write fault output if fault conditions are no longer present.
- SYS RESET - Always LOW. Used for test purpose.
- WRITE PH LKD OSC - 19.34 MHz oscillator locked to the servo information.
- RD PH LKD OSC - 38.68 MHz oscillator locked to the RD PLS DATA during a read operation or locked to the WRITE PLO when not reading.

Outputs

- RD PH LKD OSC UP - READ PLO up control.
- RD PH LKD OSC DN - READ PLO down control.
- OSC WB ENBL - Wideband enable control for the READ PLO.
- SVO PH LKD OSC - 19.34 MHz clock.
- SVO CLK - 9.67 MHz clock output to the interface.
- DATA CLK - 9.67 MHz clock output to the interface with the RD DATA. The rising edge of DATA CLK is in the center of the data cell.
- WRITE FAULT - Active high signal signifying a write fault condition exists.

4.3.5.5 READ/WRITE-ENCODER/DECODER I/O DESCRIPTION

Inputs

- RD CMD - Read command from the interface, active low.
- WRITE CMD - Write command from the interface, active low.
- NRZ DATA - Inverted interface data to be written.
- WRITE CLK - Interface data write clock.
- SVO WRITE PTCT - Active low signal protecting the embedded servo field.
- WRITE PTCT - Active low input used by microcomputer to disable write function.

Outputs

- RD DATA - NRZ data decoded from the flux reversals on the recorded surface.
- WRITE PLS DATA - Flux reversal information sent to the write driver during a write operation.
- WRITE GATE ENBL - Active low signal enabling the write operation of the write driver.

4.3.5.6 READ PLO OPERATION

READ PLO-READ OPERATION

Figure 4-47 shows a block diagram of the Read PLO Read/Write Operation. During a read operation, the Read PLO is locked to the pulse data by selecting the phase detector to control the 38.68 MHz VCO's charge pump. Wideband enable comes true at the start of the PLO Sync Field to Speed Locking of the Read PLO to the pulse data early and the late strobe enable the read PLO to be phased either early or late with respect to the pulse data to recover marginal data.

The timing diagram in Figure 4-48 shows the Read PLO's inputs for three different relationships of the RD PH LKD OSC (38.68 MHz) and the RD PLS DATA. The down control is a constant width while the UP control is varying. The rising edge of RETIMED PLS DATA, the falling edge of RD PH LKD OSC UP, and the rising edge of RD PH LKD OSC DN occur simultaneously.

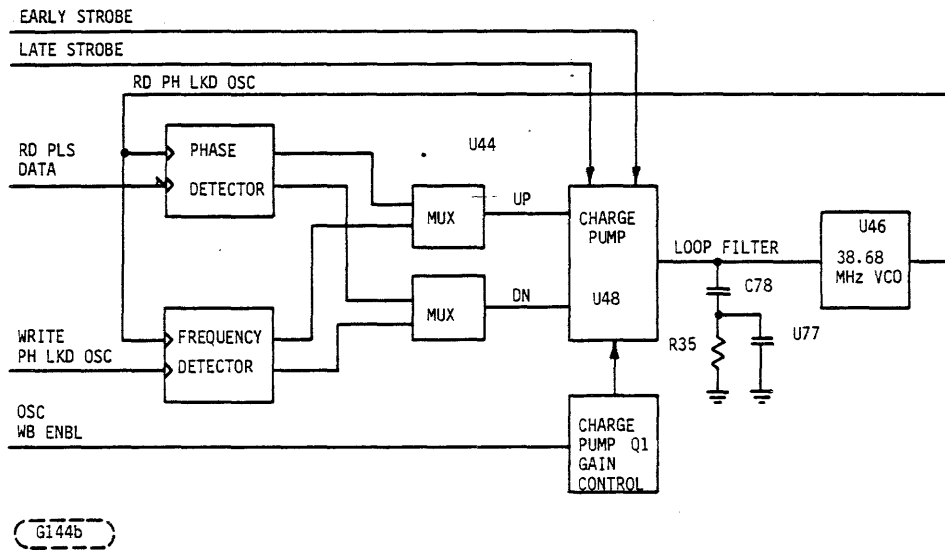


FIGURE 4-47. READ PLO READ/WRITE OPERATION BLOCK DIAGRAM

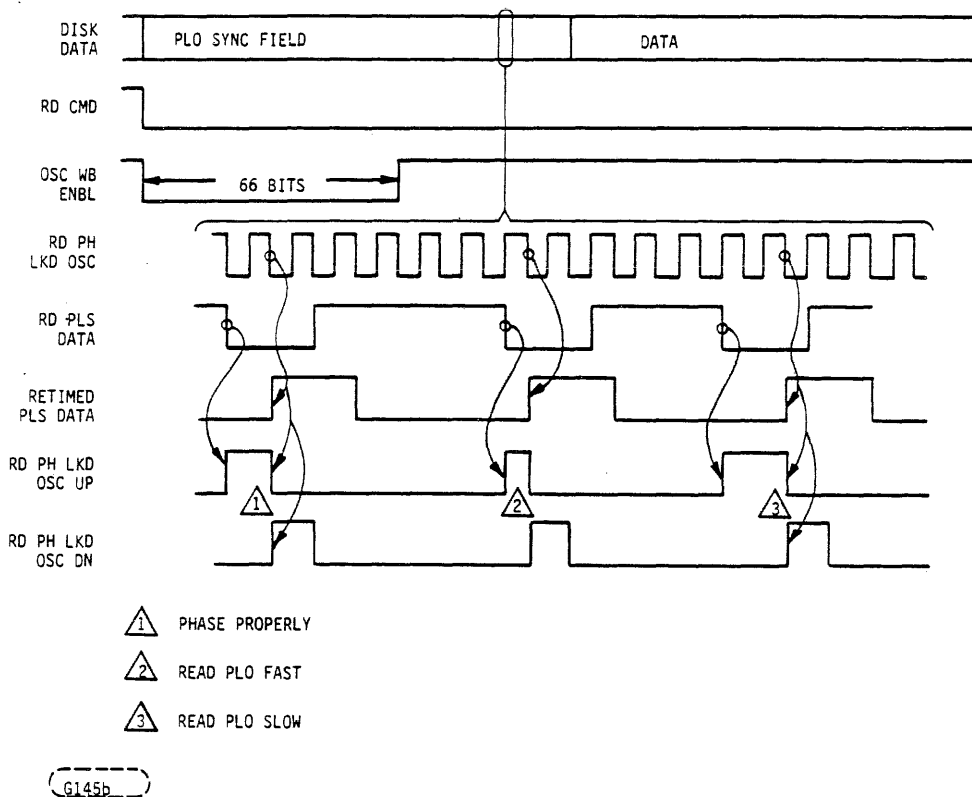


FIGURE 4-48. PHASE DETECTOR TIMING

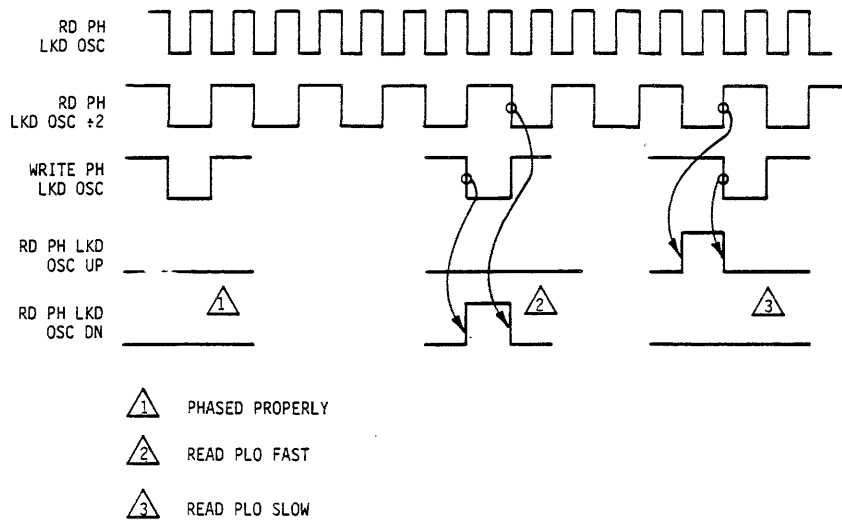
READ PLO - WRITE OPERATION

While the device is not in a read operation, the Read PLO is locked to the Write PLO by selecting the frequency detector. The Write PLO is locked to the embedded servo information. Typical timing for the frequency detector is shown in Figure 4-49. The up and down latches are reset when both latches are set. This will cause both up and down to be of varying widths.

WRITE OPERATION - INTERNAL WRITE PHASING

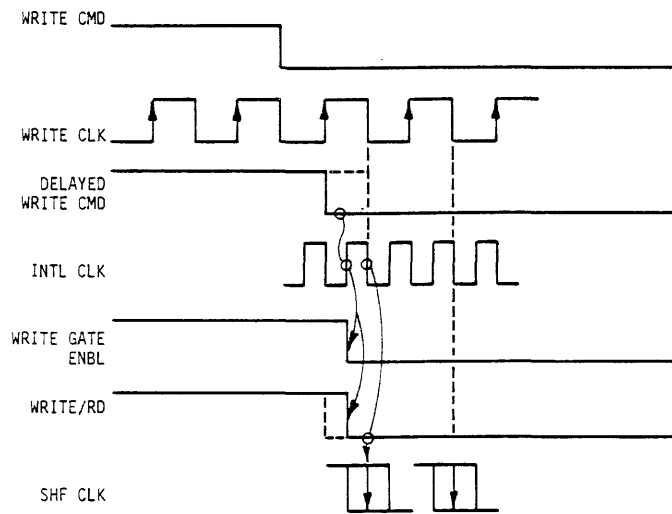
Because of the various cable and controller delays, the WRITE CLK will be out of phase with the internal clocks. To phase the clocks properly, the R/W-ENC/DEC delays the internal write command until the proper clock edges are present. This insures that the rising edge of WRITE CLK and the falling edge of SHF CLK never occur simultaneously.

Figure 4-50 shows how this phasing is done and the possible positions of SHF CLK to WRITE CLK.



G145a

FIGURE 4-49. FREQUENCY DETECTOR TIMING



G147c

FIGURE 4-50. WRITE PHASING

WRITE OPERATION - PLO SYNC FORMAT

At the beginning of a write, either to a header or data field update, a PLO sync field 88 bits long is required. this field is specified to be all zeroes. For the 2,9 code, all zeroes is a constant low frequency pattern. Since the PLO when reading can lock faster to a high frequency pattern, 66 bits of all ones are forced at the beginning of the sync field.

The output ones enabled out of the R/W-CONTR forces the R/W-ENC/DEC encoding logic to encode all ones. This will then cause WRITE PUL DATA to be its highest frequency, with a flux reversal every 155 ns. For a count of 22 ENCD T pulses (ones), ENBL will be true. This accounts for the 66 bits of forced ones since an encode pulse comes every 3 bit times.

The format timing is shown in Figure 4-51 and in the interface section.

WRITE OPERATION - WRITE DISABLE

At the end of a write operation the internal write commands are not disabled at the termination of Write CMD. They are held active until DCD T comes true. This makes sure that the three bits being encoded have been written. Immediate termination of a write operation is possible only by having SERVO WRITE PTCT or WRITE PTCT GO ACTIVE. This resets the Write Gate ENBL Flip-Flop in the R/W-ENC/DEC.

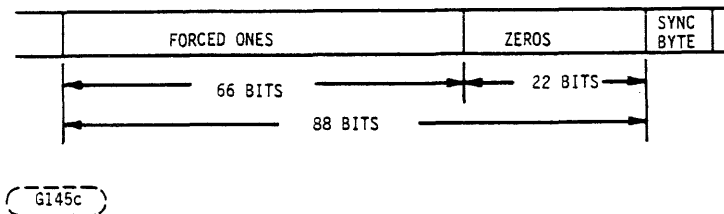
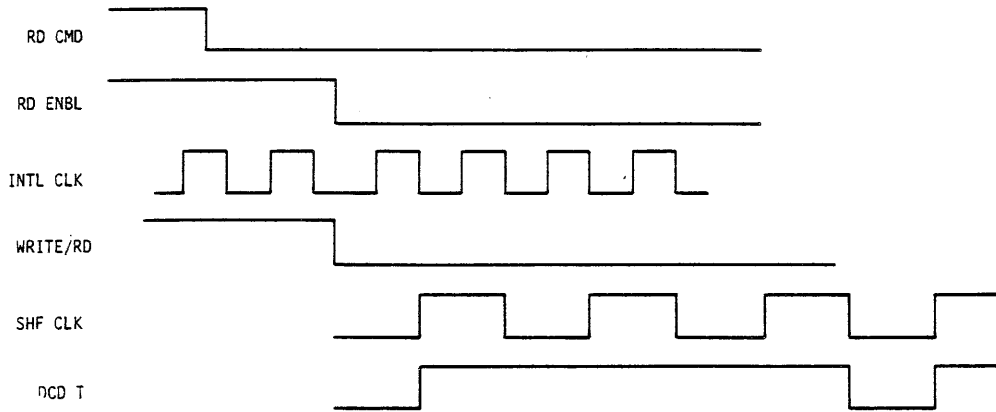


FIGURE 4-51. PLO SYNC FIELD

4.3.5.7 READ OPERATION

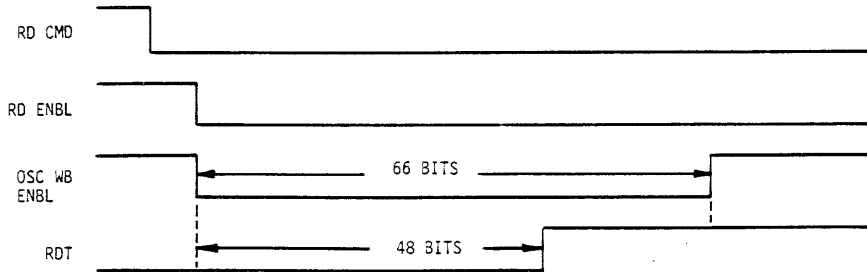
READ OPERATION - INITIATION AT READ COMMAND

Refer to timing in Figure 4-52 and 4-53 the R/W LSI will not begin a read operation until RD ENBL (from Servo LSI) comes true. This protects the phase detector from the write splice at the beginning of the header PLO sync field. Once the read is started, the Read PLO is enabled to lock to the PLO sync field. Also at this time the internal clock is switched from the Write PLO to the Read PLO. A divide-by-6 counter and decoder and a divide-by-16 circuit in the R/W-Control LSI are enabled. The divide-by-6 counter and decoder produce timing clocks for the 2,9 decode logic in the R/W ENC/DEC. The divide-by-16 counter produces OSC WB ENBL and RD T. The R/W-ENC/DEC is enabled by RD T.



G146a

FIGURE 4-52. READ INITIATION TIMING



FF088b

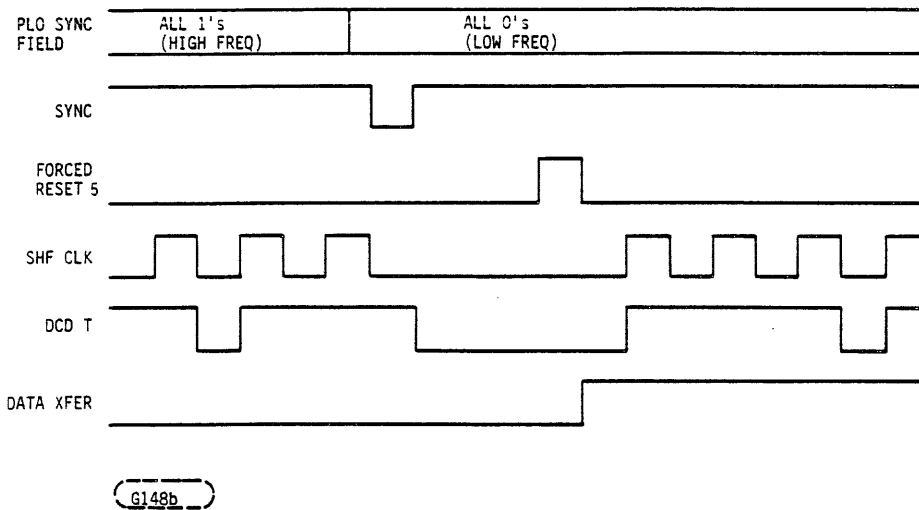
FIGURE 4-53. DIVIDE-BY-16 DECODE TIMING

READ OPERATION - INTERNAL PHASING

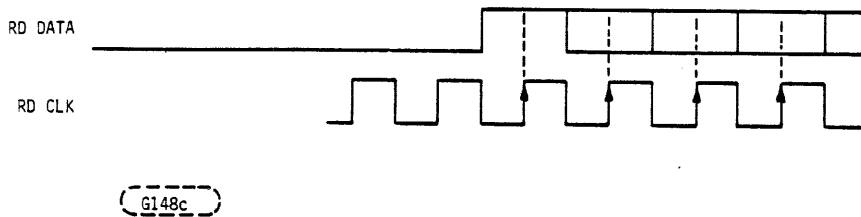
Internal read phasing takes place at the transition of the all ones to the all zeroes in the PLO sync field. This phasing reinitializes the divide-by-6 counter and decoder to be in sync with the pulse data. Figure 4-54 shows the internal read phasing. A decode from the pulse data causes SYNC to come true. This resets the divide-by-6 counter. The counter is held in this state until FORCED RESET 5 comes true approximately 200 ns later. At this time the counter is enabled to operate and DAT XFER becomes active: RD DATA has been held at an all zero state by DATA XFER being inactive.

READ OPERATION - VALID DATA

At the end of the PLO sync field occurs the customer sync byte. At this time the RD DATA is considered to be valid. The sync byte indicates the beginning of the data and it established byte synchronization. Figure 4-54 shows the sync byte along with DAT CLK. DAT CLK is the clock sent with RD DATA over the interface. The rising edge of RD CLK indicates the center of the individual RD DATA cells.



G148b
 FIGURE 4-54. INTERNAL PHASING TIMING



G148c
 FIGURE 4-55. READ CLOCK TIMING

The read operation will continue until RD CMD is dropped or until RD ENBL goes inactive. Because of the internal delays in the R/W-ENC/DEC, RD CMD must be held active nine bit times after the end of the disk data. Refer to Figure 4-55 for a diagram illustrating disk data format and its relationship to other Read/Write Signals.

4.3.5.8 LMU R/W PREAMP BOARD

INTRODUCTION

The LMU Preamp Board provides four major functions:

1. Basis amplification of the signal from the disk. The amplified signal is sent to the read signal processing board for further processing.
2. Writing data on the disk and fault indication. The write data comes from the Read/Write LSI chips.

3. Demodulation of the position bits that are written in the embedded servo zone. The output of the demodulator is the servo position error (SPE) signal. Control signals for the demodulation come from the servo LSI chips.
4. Detection of servo data for decoding of the gap, reading the cylinder address and locking the servo PLO.

READ AMP CIRCUIT DESCRIPTION

Refer to Block Diagram (Figure 4-47). Timing Diagram (Figures 4-52, 4-54 and 4-55), and Schematic (Section 5).

The M104 Read/Write LSI circuit contains a two stage preamp for each head. The two head select inputs are internally decoded and enable the proper preamp circuit. The signal is output on PINS 6 and 8. R76, 77, 78 provide termination for the M104 output stage. The nominal gain of the M104 is 35.

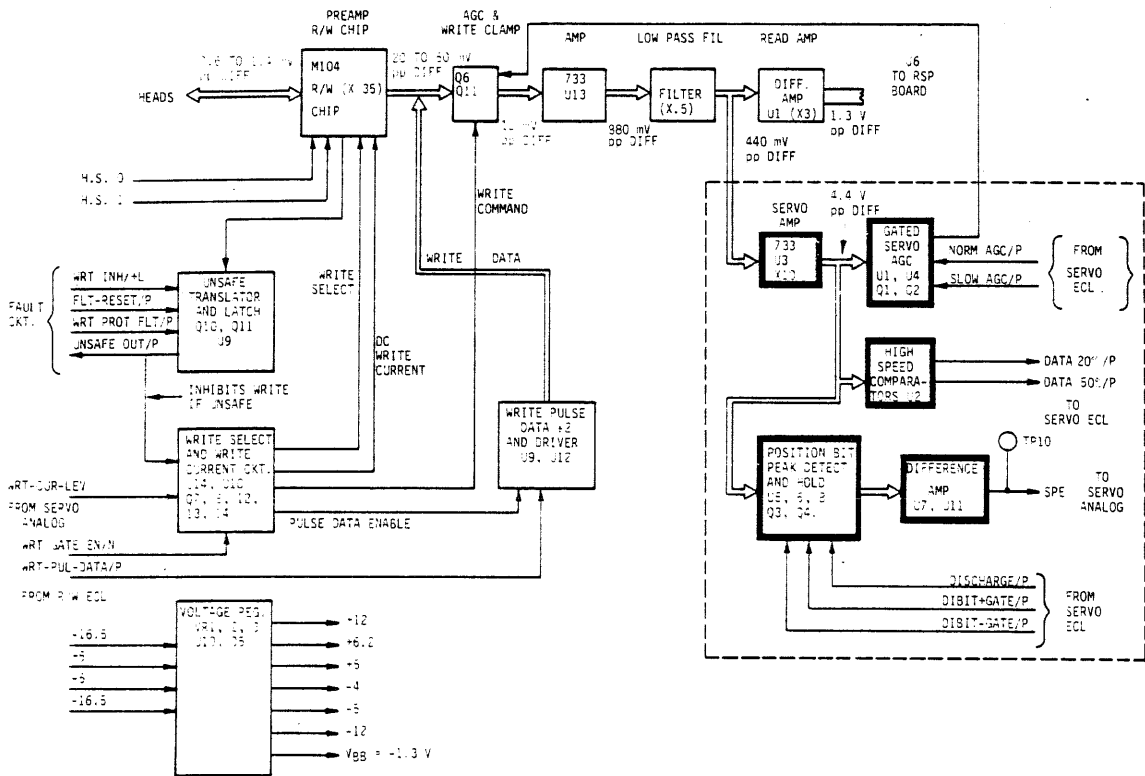
The signal is then AC coupled to R73, 75 and Q6. Q6 is the AGC FET. The signal is then amplified by U13 (GAIN 50). The output of U13 is filtered by L1, L2, L3, L4, C39 C33, C26 and fed to R30, 31, 32, 33. R31 and R32 input to a differential pair in U1. The output of the two transistors is applied to J6 which feeds the RSP PWA. R30 and R33 Feed U3 which amplifies the signal by 10. The output of U3 feeds the AGC detector comprised of U4, U1, Q1, Q2. Q6 is a FET whose small signal resistance varies with its gate to source voltage. The gate voltage of the FET is the voltage across C44. U4-2 has a DC reference voltage (approximately 0.7 V). If the voltages at U4-4 and U4-6 are below the reference, then U4-1 conducts current out of capacitor C51. When the signal at U4-6 or U4-8 goes above the reference then U4-5 or U4-8 conducts. Transistor Q1 "mirrors" this current and charges C51. For the voltage of C51 to stay constant, equal amounts of charge and discharge currents are needed. This will be the case if the AC signals at U4-6 and U4-4 go above the reference level 50% of the time this requires that the peak signal at U4-4 and U4-6 be 1 V peak. U1-1 supplies the current that is switched and U1-1 will conduct only if NORM AGC EN is high. Thus the AGC circuit is gated only during the embedded servo AGC zone. U12-11 provides a lower current (the smaller current gives a slower AGC response) that is enabled by SLOW-AGC-EN-P. This signal is used during head load and head switching to provide some AGC action until the PLO is locked and normal AGC can be activated.

POSITION BIT DEMODULATION FOR SPE POSITION ERROR (Bottom of Last Sheet)

Figure 4-58 shows the Servo Position Bit Demodulation timing described below. The AGC'd level at U3-8 is buffered and level shifted by U4-10 and applied to U5-3 which is the input to the demodulator. U5-3, 4, 5 and U5-3, 2, 1 are connected as diode gates. When U8-12 and U8-7 are low these diodes are reversed biased and no signal appears at U5-6 or U5-9. U5-6, 7, 8 and U5-9, 10, 11 function as peak detectors. When U8-7 or U8-12 go high, signal current is allowed to flow thru the diodes and is peak detected by the peak detecting transistors. The peak is held on capacitors C27 and C28 and applied to difference circuit U7 and U11. FETs Q3 and Q4 are driven by U6 and discharge the holding capacitors just before the position bits are sampled. The three control signals DIBIT+GATE-P and DISCHARGE-P are generated in the ECL SERVO LSI. SPE polarity is determined by gating the odd or even bit into the + or - dibit circuit.

SERVO DATA DETECT COMPARATORS (Top of Last Sheet)

Figure 4-59 shows timing for the Data Detect Comparators. U2 is dual ECL comparator (MC1650) that is used to detect the presence or absence of data. U3-8 output is high pass filtered by C8 and R19 and applied to U2-5. U2-6 has a small threshold voltage and U2-2 goes high when the signal at U2-5 is above that of U2-6. U2-12 is biased at 50% of the peak signal. When U2-11 goes above U2-12, then U2-14 goes low.



(ECL) FIGURE 4-56. LARK R/W PREAMP BLOCK DIAGRAM
SERVO READ CIRCUITRY EMPHASIZED

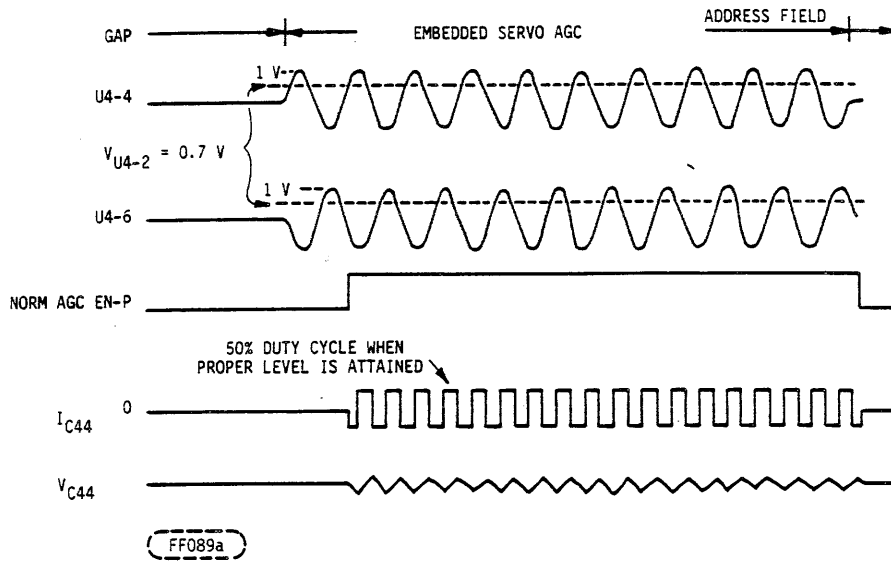


FIGURE 4-57. AGC CIRCUIT

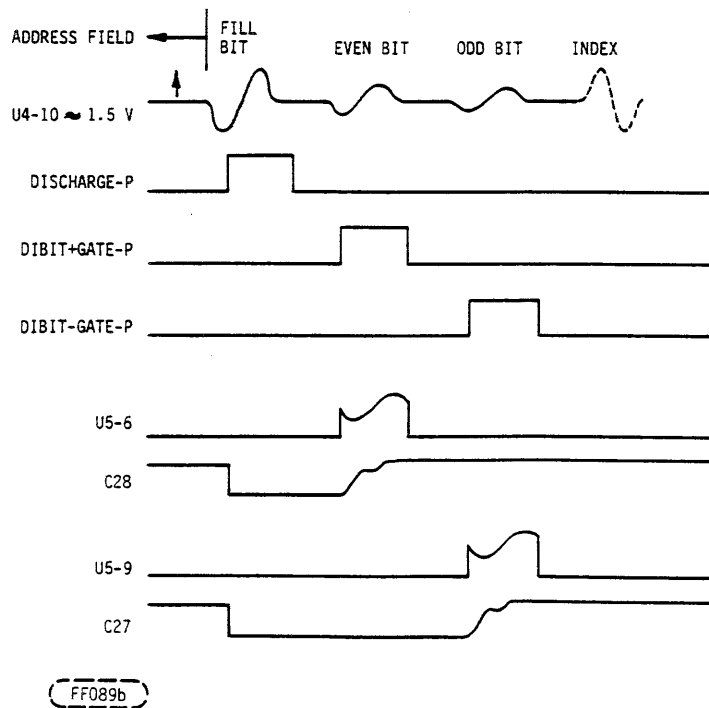
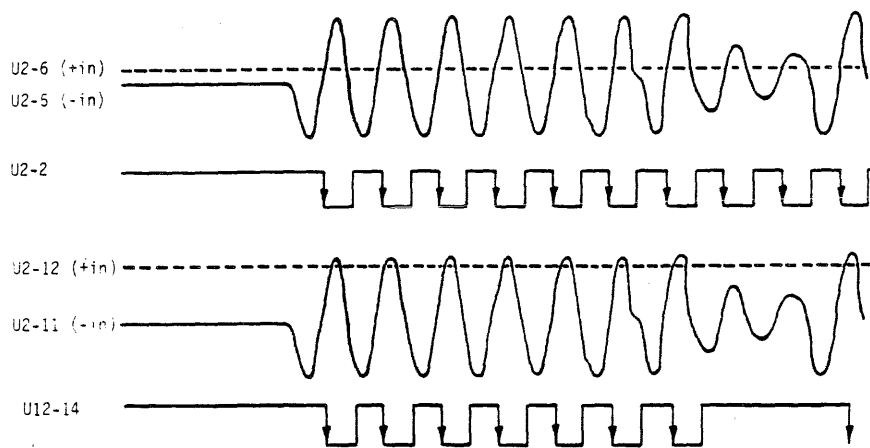


FIGURE 4-58. SERVO POSITION BIT DEMODULATION
(FOR SPE = EVEN - ODD)



FF089c

FIGURE 4-59. DATA DETECT COMPARATOR TIMING

READ SIGNAL PROCESSING PWA

The Read Signal Processing PWA receives the read signal from the preamp and processes this signal to generate a pulse data signal that is then sent to the R/W LSI for decoding and PLO synchronization. Figure 4-60 shows a block diagram of the RSP board. Refer to 77666450 for a schematic of the RSP board.

The signal from the preamp is first applied to an automatic gain control circuit (Q2) and then buffered by an amplifier (U16). The AGC'ed and amplified signal is then split into two separate channels.

One is the high resolution channel which contains a pulse slimmer circuit (U15, U14, U13, U17), filter, active differentiator (U9) and zero cross detector (U8). The pulse slimmer used is a modification of a cosine equalizer which uses a delay line that is open circuited at one end (U14). At the terminated driver end, the signal present is the input signal, plus the signal that has been reflected back from the open end. A portion of this signal is subtracted from the signal at the open end of the delay line by U13. This, produces, a slimmer pulse and reduces the effect of peak shift. The amount of signal that is subtracted is controlled by a variable gain amp (U15, U17) and this change depending upon the portion of the head. (More slimming at inner radius and less slimming at the outer radius.) The output of the slimmer is filtered and differentiated by U9 and the output of U9 is applied to a zero cross detector U8. The output of the zero cross detector contains the accurate timing signal which represent the flux reversals written on the disk, but it also has some false crossing due to the action of the pulse slimmer.

These false crossings must be removed by the qualifier channel. The qualifier channel also receives the output of the AGC circuit and amplifier. It is first low pass filtered, amplified (U12) and buffered (U11). The output of the buffer is peak detected by U10. A percentage of this peak is used to generate a qualifying gate based on the amplitude of the signal by U7 comparator/latch circuit. The output of the buffer is also differentiated and applied to a zero cross detector with hysteresis (U8). This "low resolution" signal is also used as a qualifier. The two qualifying signals and the high resolution (pulse slimmed) signal are applied to the data latch circuit (U1, U3, U5). The output of the data latch is pulse data which has the accurate timing of the high resolution channel, but with the false signals removed. Figure 4-61 shows the timing diagram for the data latch circuit.

The output of the peak detector also feeds an AGC amplifier and filter (Q1, U2) which closes the feedback for the AGC system.

4.3.6 FAULT DETECTION

Figure 4-62 is a block diagram illustrating the fault detection system of the LMU.

4.3.6.1 HARDWARE FAULTS

FAULT (INTERFACE FAULT LINE)

This fault is activated by the fault logic associated with the RD/WRT digital CKT.

The following conditions set the fault line:

1. WRT Gate AND Servo Write Protect

This detects the condition of a missed embedded servo field detection, which causes a WRT protect condition for the following data field, AND an attempt to write.

2. WRT Gate AND Microcomputer WRT Protect

This detects an attempt to write when WRT protected by the MP. The MP may write protect when Off-cylinder during seek, during command dialog, if a fault condition exists, if fixed or removable WRT protect is active and the associated volume is selected, or when not ready (RDY not active).

3. Read Gate AND Write Gate

4. Read Gate AND OFF-CYL doesn't inhibit writing.

UNSAFE (DETECTED BY HARDWARE BUT REPORTED BY MC)

Any unsafe condition detected by hardware forces a WRT protect condition, and does it independent of the usual WRT GATE. The unsafe condition causes an emergency retract of the heads. Both the write protect and retract actions are taken independent of the microcomputer.

Preamp faults:

1. Write gate and no write data.
2. Head shorted across both or one side or open.
3. Read mode and DC write current (preamp chip shunts current internally).

Any of the above fault conditions set the unsafe latch which turns off the write gate and write current and places circuit in read mode.

Servo Detected faults:

1. -5, +5, +16, or -16 voltage fault.
2. Retract cap charge low.

(Circuit which detects above faults also detects when the Retract Relay is active, thus even when normal relay disable is done the unsafe latch is set.)

SERVO DIGITAL FAULT LOGIC

The servo data recovery circuit samples the normal WRT gate at sector or Index time and produces a circuit to set the unsafe latch if WRT Gate is active. This is a check of the write circuitry and the write protect logic.

ONESHOT SYSTEM PROTECT LOGIC

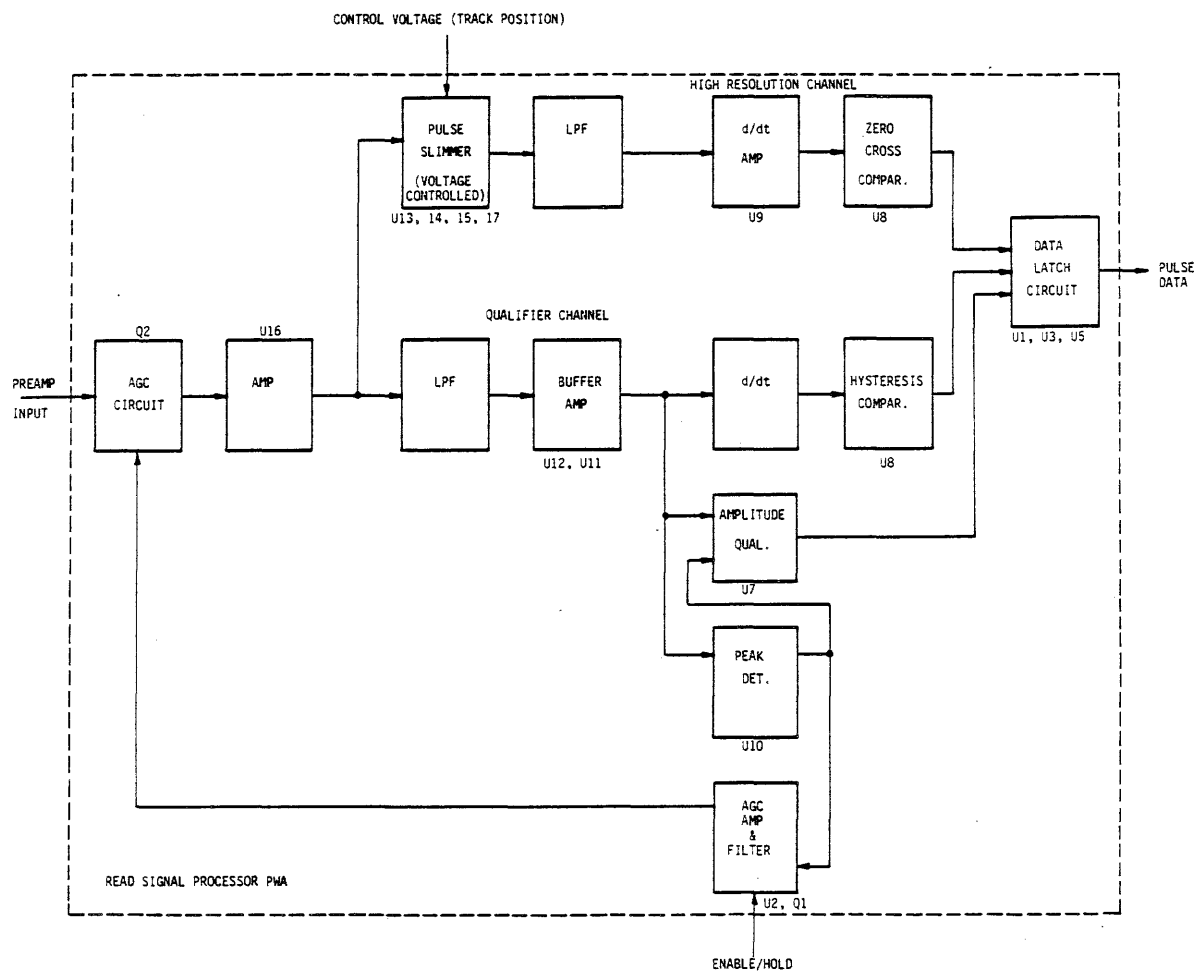
One Oneshot is clocked by the speed sensor set at 50% speed threshold. This will protect against loading the head with spindle motor off in case of MC failure.

A second oneshot is used to monitor the embedded SVO data recovery logic. The signal CLK, which is produced when a valid SVO field is found, will stop if a continuous read problem exists, if the actuator is outside data zone or if the PLO loses lock and is not relocked by the MC. The PLO will unlock if the disk speed drops out of the VCO range. All of these functions are provided by the micro-processor and thus the oneshot is a redundant safeguard to MC failure.

Both oneshots are used to protect against the consequences of a MC failure. They protect against loading when disk is not moving or not unloading when disk is stopping.

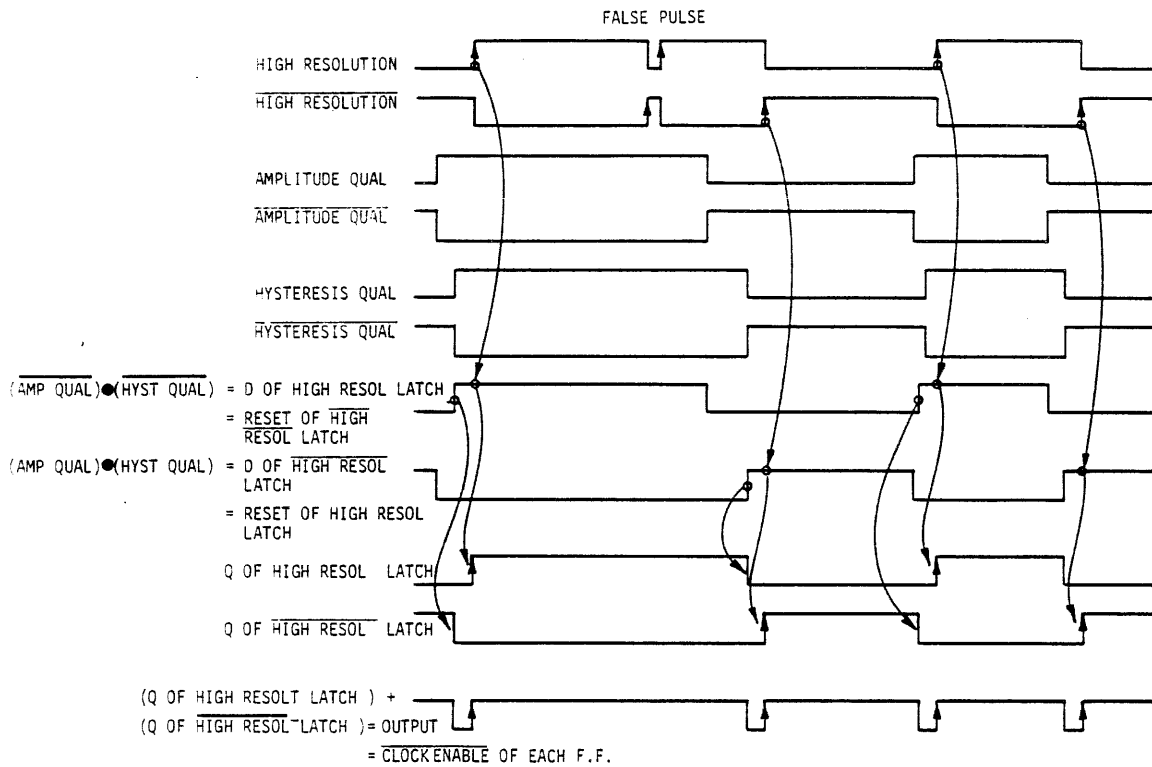
4.3.6.2 FAULT RECOVERY

The Fixed Write Protect indicator on the operator control panel blinks when there is a fault. Actuating the Fixed Write Protect switch twice in succession attempts to clock the Write Fault Latch inactive and the fault test point latches inactive. If the fault persists, the unit should be stopped and started again to see if the fault will remain cleared. If not, stop the unit and have it repaired by the proper maintenance facility. The Write Fault latch will not clock inactive if one of the fault conditions remains.



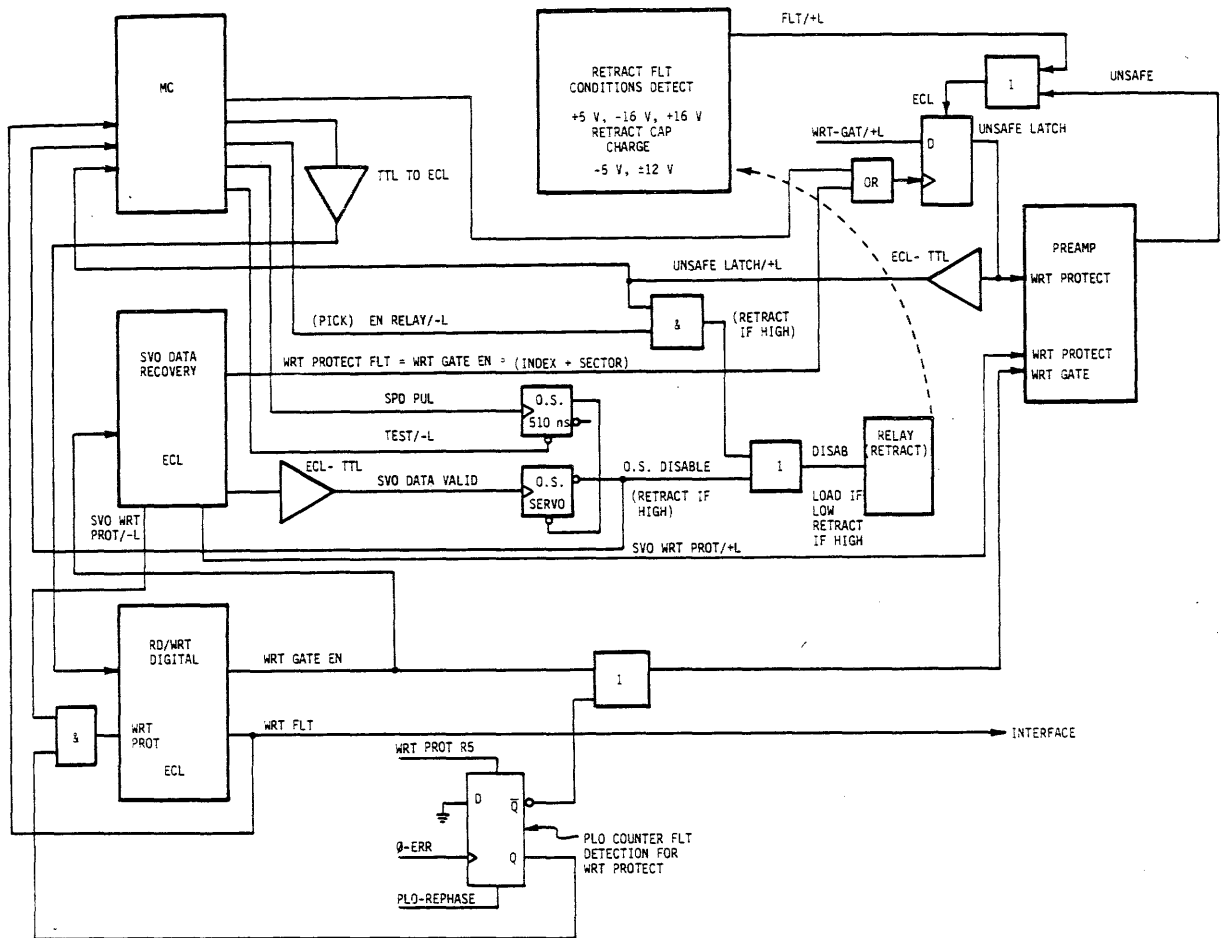
FF172

FIGURE 4-60. LARK 50 RSP PWA



FF171a

FIGURE 4-61. DATA LATCH TIMING



(FF080)

FIGURE 4-62. FAULT LOGIC BLOCK DIAGRAM

4.3.6.3 ACCESSING FAULT INFORMATION ON MICRO-UNIT INTERFACE

Using a Logic Analyser, fault information can be accessed by observing the LMU interface lines. The meaning of the interface line command, status and fault codes are described in Section 5.6. The Status Display option below also aids fault diagnosis.

4.3.6.4 LARK 50 STATUS DISPLAY OPTION

The front panel with the Status Display option is shown in Figure 4-64. The Status Display Board provides the following functions:

1. Buffers PROT-LED/-L and RDY-LED/-L signals.
2. Displays the drive status codes.
3. Blanks the display and activates the sound generator when a 00H status code is received.

The buffering of the two LED signals is achieved through a 74LS132 Schmitt-trigger NAND gate and a 7437 NAND buffer for each signal. These two buffered signals are then outputted from the board to the two switch LED's. The +5 that goes to the switch LED's is also outputted from the board.

To display the machine status, the logic (74LS123, 74LS132) decodes a positive going pulse of less than 20 μ s on the RDY-LED/-L input. If this decode is true, the inverse of the PROT-LED/-L input is clocked as data into a 74LS164 8-bit shift register on the falling edge of RDY-LED/L. This procedure of clocking data should happen as rapidly as possible with the most significant bit first as shown below. The display uses two 4-bit hexadecimal latch/decoder/drive displays. The data is latched into the displays at the end of the 100 ms one-shot timeout.

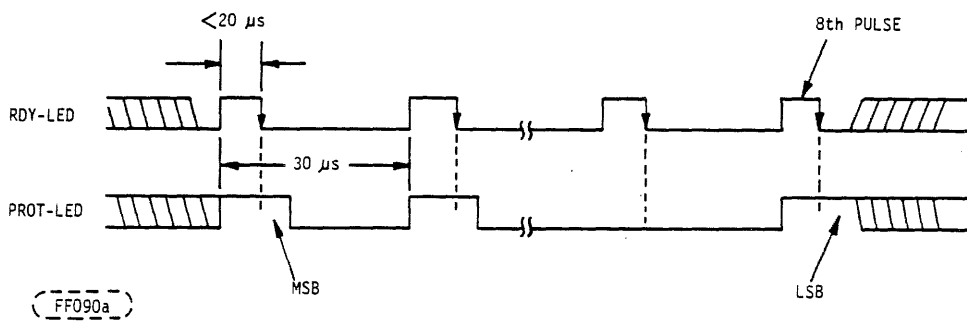


FIGURE 4-63. LED SIGNALS

The sound generator consists of a 555 oscillator, 7437 buffer and a transducer sound generator. A 100 ms one-shot (74LS123) is triggered on each clock pulse to the shift register. The 7437 gates the oscillator output with the outputs of the 7433 open-collector NOR gates (all outputs wire-anded). The 7433 output is high when all zeroes are present at the shift-register's output, which causes the transducer to be activated.

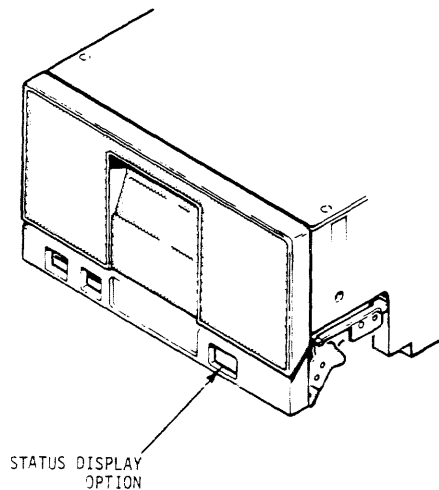


FIGURE 4-64. FRONT PANEL WITH STATUS DISPLAY OPTION

The paragraphs of this section describe in more detail the inputs and outputs of the two Servo LSI circuits.

4A.1 SVO DATA RCVY (SERVO DATA RECOVERY) IC PIN DEFINITIONS

4A.1.1 INPUTS

1. CLK-19.34 MHz CLK

A clock from the VCO* used for timing such as gap detection and Track address decode. The CLK frequency is locked to the disks rotational speed so that each CLK cycle is 1/8 of a SVO data bit. The timing and data recovery logic uses this frequency relationship but is independent of the phase of the CLK relative to the data.

2. SYNC DATA (Data 10%)

Pulse read data derived by thresholding the analog read data as shown below in Figure 4A-1. Data 10% is used for gap and synch detection when phase/frequency locking the servo PLO only.

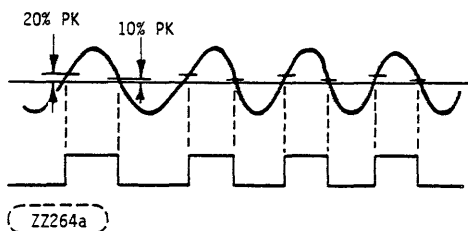


FIGURE 4A-1. SYNC DATA

3. SVO DATA (Data 50%)

Pulse read data derived by thresholding the analog read data as shown in Figure 4A-2. Data 50% is used for track address decode, Data-Det-F/F*, and Index Sync recovery.

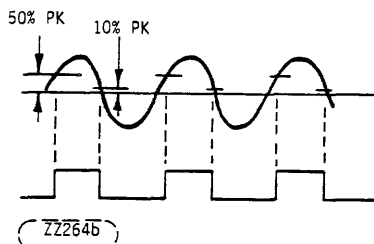
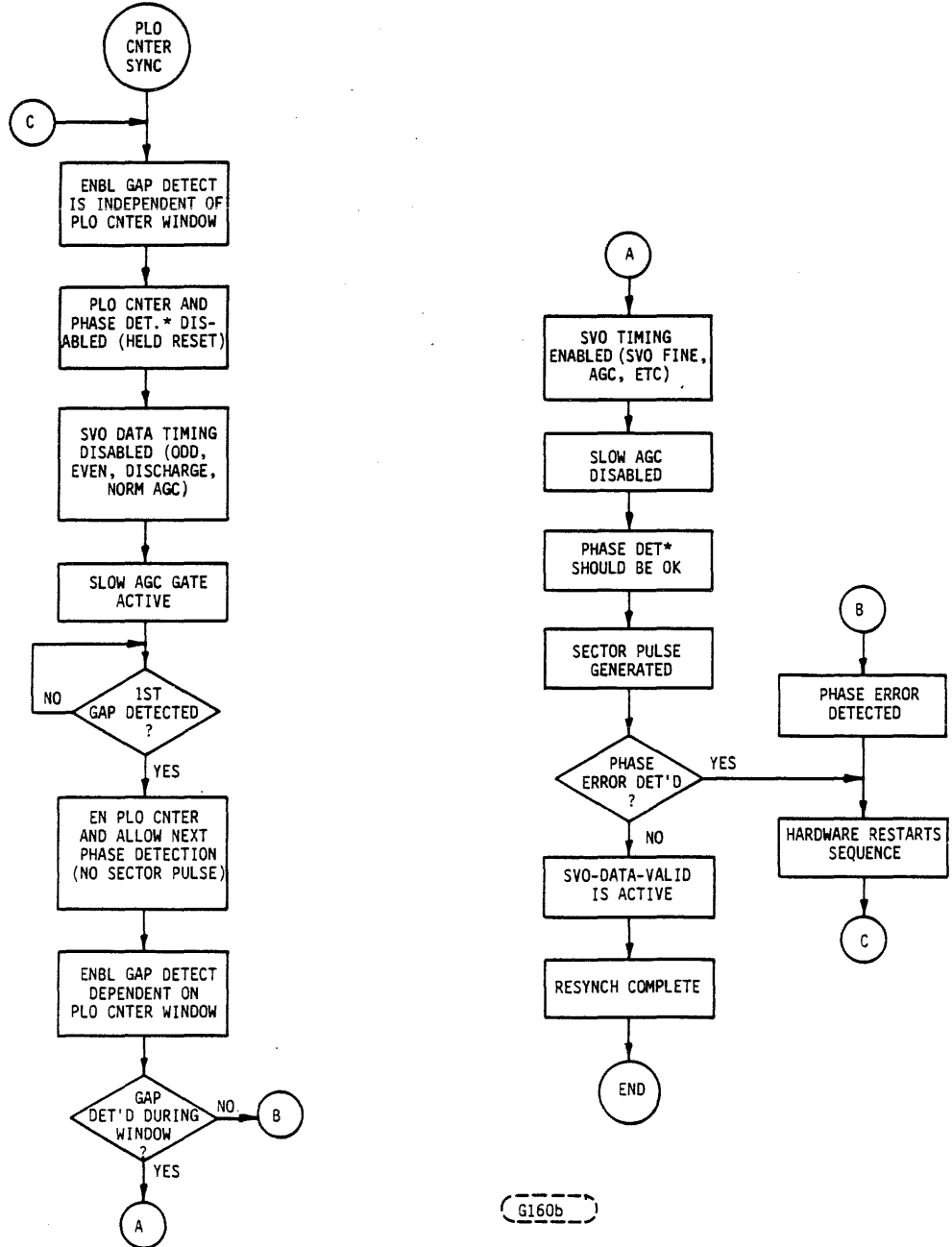


FIGURE 4A-2. SVO DATA

*Inside LSI chip.

4. REPHASE (after head change)

When held active SVO data recovery is disabled, the PLO-Rephase F/F* is set and the SVO DATA TIMING EN F/F* is reset. When switched to the inactive level the sequence shown in Figure 4A-3 begins which leads to the PLO counter being rephased to new Servo data zones without losing PLO lock.



*CIRCUITRY WITHIN LSI

G160a

G160b

FIGURE 4A-3. RESYNCH OF PLO COUNTER

*Inside LSI chip.

5. **FREQ-DETECT M**

When active allows auto PLO resync and when Phase error is greater than 800 ns, it opens SVO data window, disables maximum Phase-error limit of 800 ns, and disables requirements of gap detection between Phase difference output. Finally when both FREQ-DETECT M and REPHASE are active PUMP-UP goes active pumping the PLO frequency up. A Pump-up time of time 200 μ s to 400 μ s is required to hit the high frequency rate.

6. **SAMPLE GATE ENBL**

When set for coarse mode, the dibit gates are disabled and SAMPLE DISH is held active. When in the fine mode the NRZ SVO DATA (TRK ADDR) is always inverted and not a function of DIBIT GATE CONT.

7. **DIBIT GATE CONT**

Selects which dibit gate comes first (odd or even) and inverts the NRZ SVO DATA (TRK ADDR) output when in the coarse mode and REV direction selected. The selection of dibit gate output timing determines the SPE polarity.

8. **TEST**

When active resets the SVO-DATA F/F* and provides a wrap-around feature of the MP controlled inputs into the MP monitored outputs. Thus certain inputs are multiplexed into certain outputs: DATA-DET-RS \rightarrow SVO DATA CLK; FREQ MODE \rightarrow NRZ SVO DATA; FINE \rightarrow SVO DATA DETECT.

9. **ENBL GAP DETECT**

The timing signal from SVO PH LOCK OSC CNTR which provides a window relative to the PLO CNTR where the SVO field gap and synch should be found.

This output from the SVO PH LOCK OSC CNTR serves a second purpose of enabling a Read after the WRT splice if Read Gate is active. See SVO PH LOCK OCS CNTR outputs paragraph--for timing.

10. **PH LOCK OSC COUNT (Phase Locked Oscillator Counter)**

The output of the PLO counter from the SVO PH LOCK OSC CNTR. It is one input of the \emptyset detector*, the other being SVO synch detection.

11. **PH ERROR (Phase Error Count)**

An output of SVO PH LOCK OSC CNTR which goes active if there is more than 800 ns of \emptyset -error between PH LOCK OSC COUNT and the synch detection of the servo field.

*Inside LSI chip.

12. DATA DETECT RESET

The reset to the Data Detect F/F*.

13. SYNC SEL

Select input for sync data or SVO DATA to the SVO DATA DET F-F.

4A.1.2 SVO DATA RCYV OUTPUTS

1. SVO DATA DETECT (Data Detect)

Set the trailing edge of 50% threshold pulse data - reset by DATA DET RS. Basic function is to tell MC when heads have loaded and are in data zone or have gone out of data zone.

2. NRZ-SVO-DATA

Serial output of CYL ADDR. See SVO-DATA-CLK and SVO-DATA-VALID for timing.

3. SVO-DATA-CLK

CLK which defines when SVO DATA is valid. The clock is internally controlled. It starts when sync is detected and stops on T1. See Figure 4A-4.

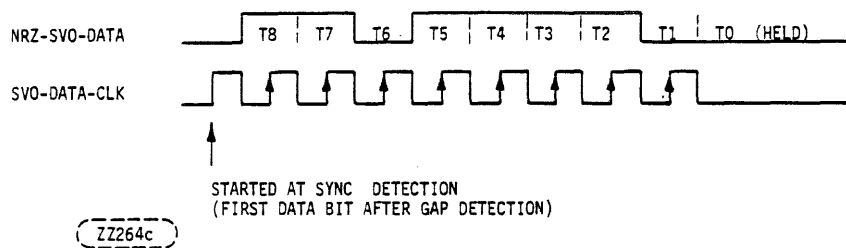
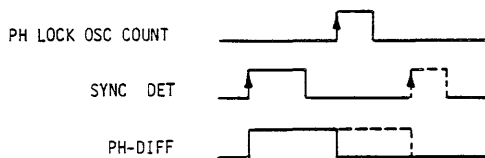


FIGURE 4A-4. SERVO-DATA-CLK TIMING

4. PH-DIFF

Active on leading edge of either PH LOCK OSC COUNT or SVO field sync detection and reset on the leading edge of the one (PLO-CNT or SVO field sync detection) which didn't activate it (see Figure 4A-5).

*Inside LSI chip.

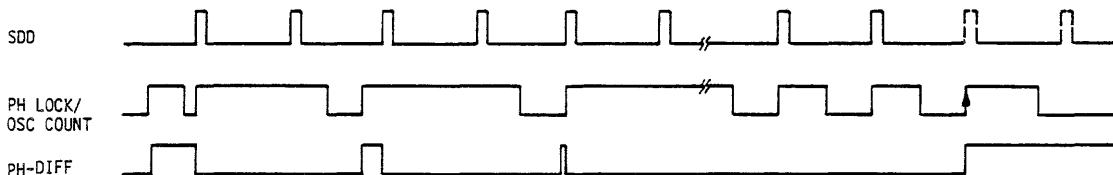


ZZ264d

FIGURE 4A-5. PH-DIFF TIMING

PH-DIFF is used by the microcomputer to detect when a PLO lock retry is necessary. The retry is needed when the PLO CLK has dropped below the point where the gaps can be detected. The retry is needed when PH-DIFF remains active for two sector times as shown in Figure 4A-6.

Retry Detection-Lack of SDV Detection (Timeout) or PH-DIFF Struck High.

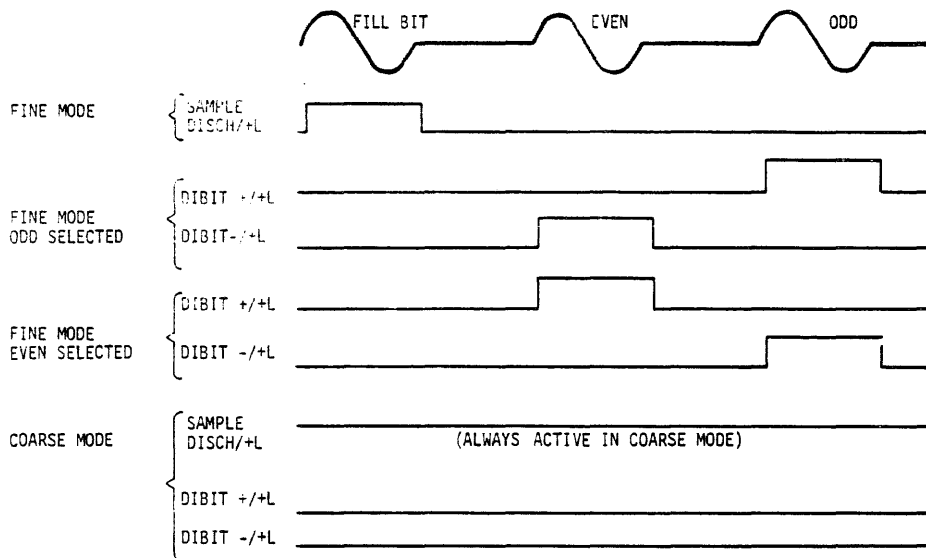


ZZ264e

FIGURE 4A-6. PH-DIFF HIGH FOR SDV TIMEOUT

5. DISCHARGE, DIBIT+, DIBIT-

Figure 4A-7 defines these three signals.

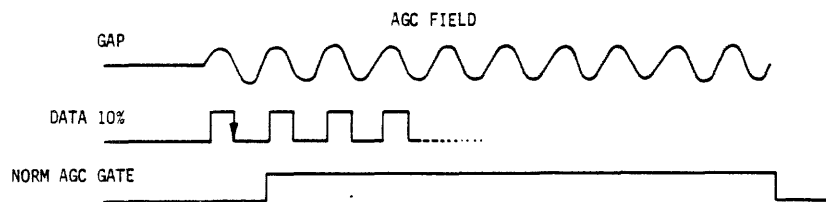


ZZ264f

FIGURE 4A-7. DISCHARGE, DIBIT+, DIBIT- TIMING

6. AGC/+1

Figure 4A-8 defines the AGC Logic.



ZZ266a

FIGURE 4A-8. AGC/+1 TIMING

7. REPHASE-ENBL

Holds PLO Counter reset and enables SLOW AGC. It is set by REPHASE or PH-ERROR-CONT in FREQ DETECT M and is reset by first SVO data sync detection. While REPHASE ENBL is active no timing gates are active. (SAMPLE DISCH, DIBIT+, DIBIT-, AGC.) See flowchart in Figure 4A-3.

8. PUMP-UP, PUMP-DN

Figure 4A-9 illustrates Logic for PUMP-UP, PUMP-DN.

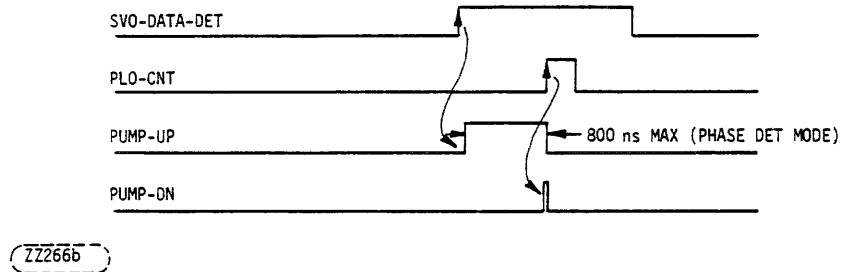


FIGURE 4A-9. PUMP-UP, PUMP-DN TIMING

PUMP-UP is set by detection of SVO DATA, PUMP-DN is set by the PH LOCK OSC COUNT feedback. Both are synchronously (with 19.34 MHz) reset when both have been set or if max time has been reached (800 ns). If put in the frequency detector mode (EN-FREQ-DET active) the maximum (800 ns) restriction is disabled allowing each to stay active until the other has passed a GAP detection. This allows missing SVO DATA Regions. Also during a RE-PHASE if the first detected GAP was false the window will find no SVO region and thus an erroneous PH-error will not be induced.

9. IDX PLS (INDEX PULSE)

This is the output of a gate enabled at Index time (SVO field Index sync time) with SVO DATA (Data 50%) as the other input.

10. SVO Z END (Write Protect Reset)

A reset pulse produced relative to the SVO field sync detection which resets the write window in the PH LOCK OSC COUNT, Figure 4A-12.

4A.2 SVO-PH LOCK OSC CNTR-CNT-IC PIN DEFINITIONS

4A.2.1 INPUTS

1. CLK (19.34 MHz-CLK)

Input to SVO PH LOCK OSC CNTR and θ -error counter.

2. CNTR RESET

When Active holds SVO PH LOCK OSC CNTR cleared.

3. 32/64-SELECT

Selects between 32 sector format or 64-42 sector format by selecting correct decode on SVO PH LOCK OSC CNTR and the Sector Counter.

4. SECTOR SELECT

Select between 32-64 Sector format and 42 Sector format.

5. WRITE PTCT FAULT ENBL

Gated with sector to product WRT PTCT FLT.

6. WRT PTCT RESET

Resets Wrt Protect F/F* enabling a write.

7. DATA VALID RESET

Resets Data Valid F/F* which will be set again after the next SVO Data field diode.

8. IDX SYNC - Later

9. PH-DIFF - Later

10. IDX REPHASE

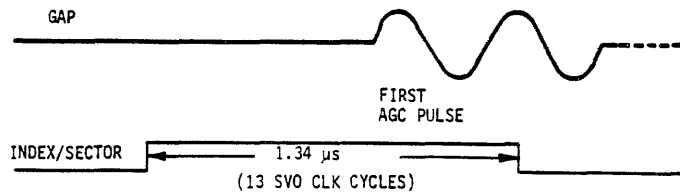
Reset sector counter and Index sync F/F* to allow rephase of sector counter to new Index.

The first detected Index will create an Index pulse on the interface and sync the sector counter. The second detected Index will also create an Index pulse and if in sync with Sector counter the following Index pulses will be created by the Sector counter only.

NOTE

- a. Outputs on first and second detected Indexes during sync.
- b. Sync requires two consecutive good Indexes.
- c. Can handle 2 dropouts after sync.
- d. Can handle 1 extra Index/rev.
- e. Uses 50% Data threshold to minimize extra Indexes.

*Inside LSI chip.



ZZ266d

FIGURE 4A-11. INDEX AND SECTOR TIMING

INDEX/SECTOR is a decode from the PLO CNTR which is locked to the detection of the first AGC pulse. Maximum \emptyset Error ± 16 SVO CLKS.

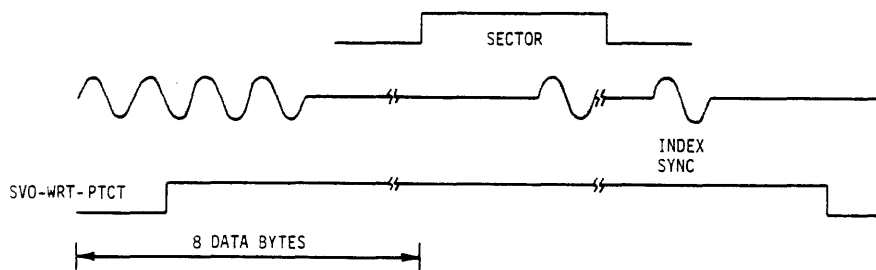
6. SVO-WRT-PTCT

Figures 4A-12 and 4A13 define this signal.

SECTOR, RD ENBL, and rising edge of SVO-WRT-PTCT are decodes of the PLO counter and thus have maximum position error relative to DISK of ± 800 ns. Falling edge of SVO-WRT-PTCT is a decode from SVO-DATA-RCVY logic and thus has ± 1 SVO CLK (50 ns) error relative to DISK position.

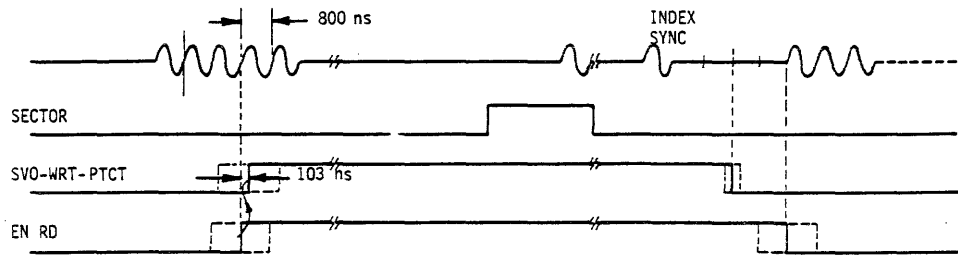
7. SVO RD ENBL

Decode of the PLO counter. Active only for the 32 servo sectors.



ZZ266e

FIGURE 4A-12. SVO-WRT-PTCT TIMING



ZZ266f

FIGURE 4A-13. RD ENBL TIMING

5.1 INTRODUCTION

This section contains the intracabling diagram, a key to logic diagram symbology, printed circuit board documentation subassembly schematics and Interface Theory of Operation.

5.2 INTRACABLING DIAGRAM

The intracabling diagram (Figure 5-1) shows the cabling between the circuit boards, switches and electro-mechanical assemblies. Since the Base PWA contains the majority of the control circuitry, the box representing that PWA has within it a block diagram showing the functions performed on that PWA and their connections to other PWAs and assemblies. The numbers in the functional blocks of sheet 2 are cross reference numbers whose use is explained in paragraph 5.3.1.

5.3 CIRCUIT BOARD DIAGRAMS

Table 5.1 lists printed circuit board assembly part numbers and the figure numbers of the schematic set. Each schematic set also has a cross reference number used to facilitate point-to-point signal tracing among the diagrams (Paragraph 5.3.1 gives details). Refer to Operation/Installation Manual Figure 1-1 for diagram which shows location of circuit boards within the LMU.

TABLE 5-1. LMU CIRCUIT BOARDS

| CKT PWA IDENT | FIGURE NUMBER | CROSS REF. NO. | TITLE |
|------------------|------------------|-------------------|------------------------------------------|
| 77685900 | 5-4 | 04XX | Base PWA |
| 77659600 | 5-5 | 05XX | Read/Write Pre-Amp PWA* |
| 77666450 | 5-6 | 06XX | Read Signal Processor (RSP) PWA |
| 77666500 | 5-7 | 07XX | AC Distribution PWA |
| 77662151 | 5-8 | N/A | Feed Through PWA (do not remove/replace) |
| | 5-9 | 0901 | AC Power Control for Spindle/Blower |

5.3.1 POINT-TO-POINT LOGIC INTERCONNECTIONS BETWEEN CIRCUIT BOARDS

Interconnections between circuit boards are traced with the aid of Figure 5-1. Trace from signal source to Figure 5-1 to destination, or destination to Figure 5-1 to source, whichever is applicable. Cross Reference numbers in Figure 5-1 and on each schematic page provide the figure number and page number of the schematic where the signal being traced is next found.

*Piggy Back PWA-77682990

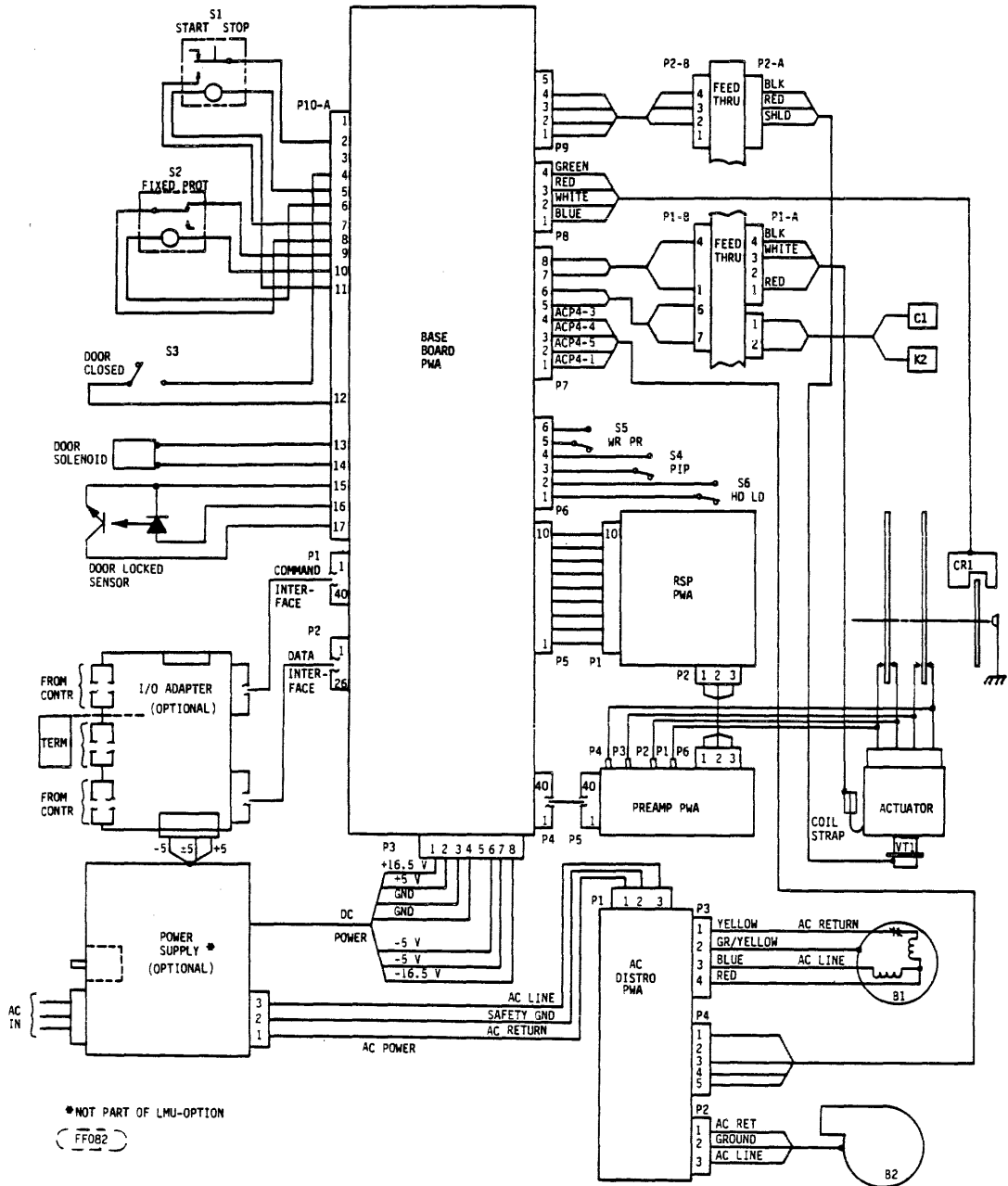
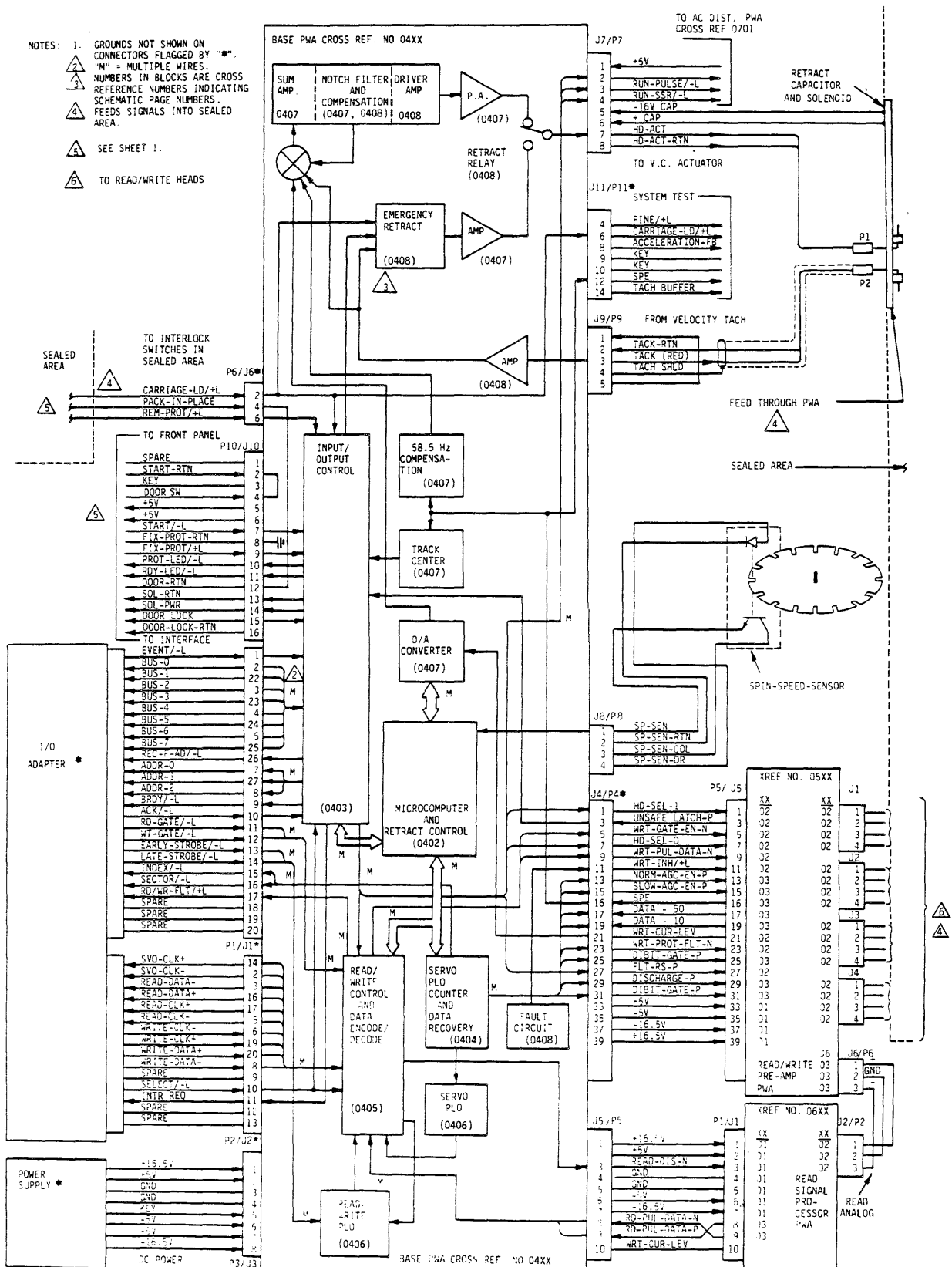


FIGURE 5-1. INTRACABLING DIAGRAM (SHEET 1 OF 2)



*NOT PART OF LMU-OPTIONAL

FF081 FIGURE 5-1. INTRACABLING DIAGRAM (SHEET 2 OF 2)

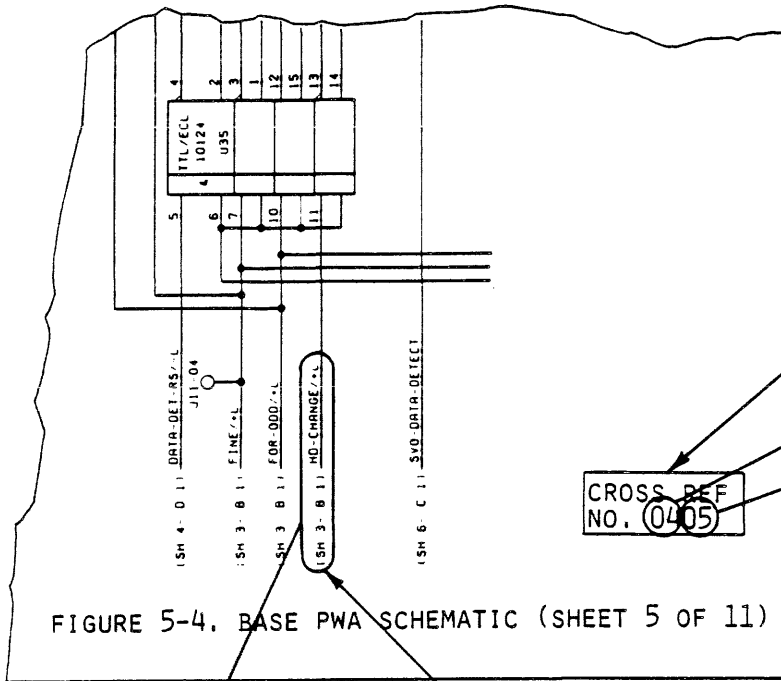


FIGURE 5-4. BASE PWA SCHEMATIC (SHEET 5 OF 11)

CROSS REFERENCE NUMBER IN LOWER RIGHT HAND CORNER OF EACH SCHEMATIC PAGE

SCHEMATIC FIGURE NUMBER

SCHEMATIC SHEET NUMBER

CROSS REF
NO. 0405

INDICATES SEE HD-CHANGE/+L ON SHEET 3

SAME SIGNAL

INDICATES SEE HD-CHANGE/+L ON SHEET 5

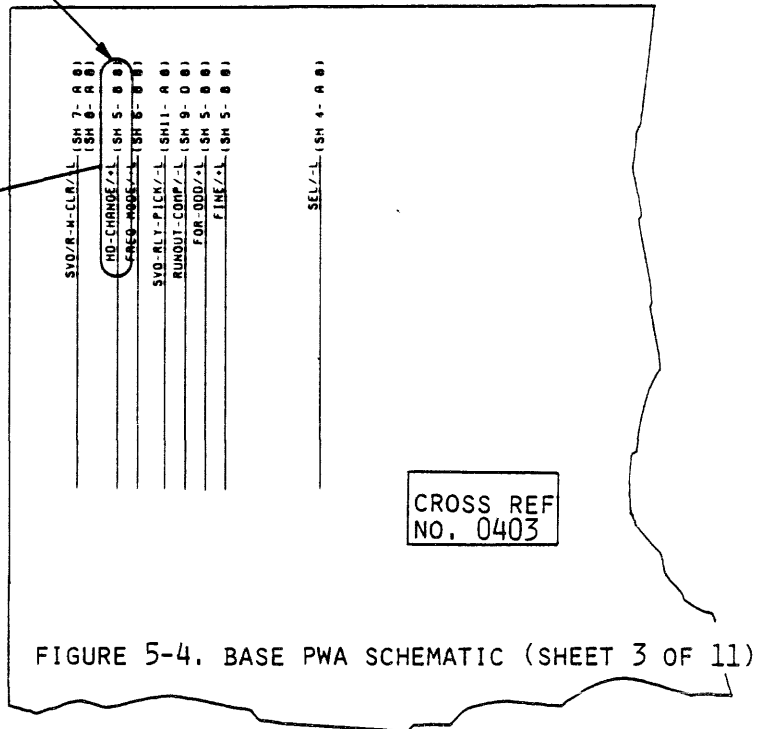


FIGURE 5-4. BASE PWA SCHEMATIC (SHEET 3 OF 11)

FIGURE 5-2A. ILLUSTRATION OF SCHEMATIC DIAGRAM INTERCONNECTION SYMBOLOGY

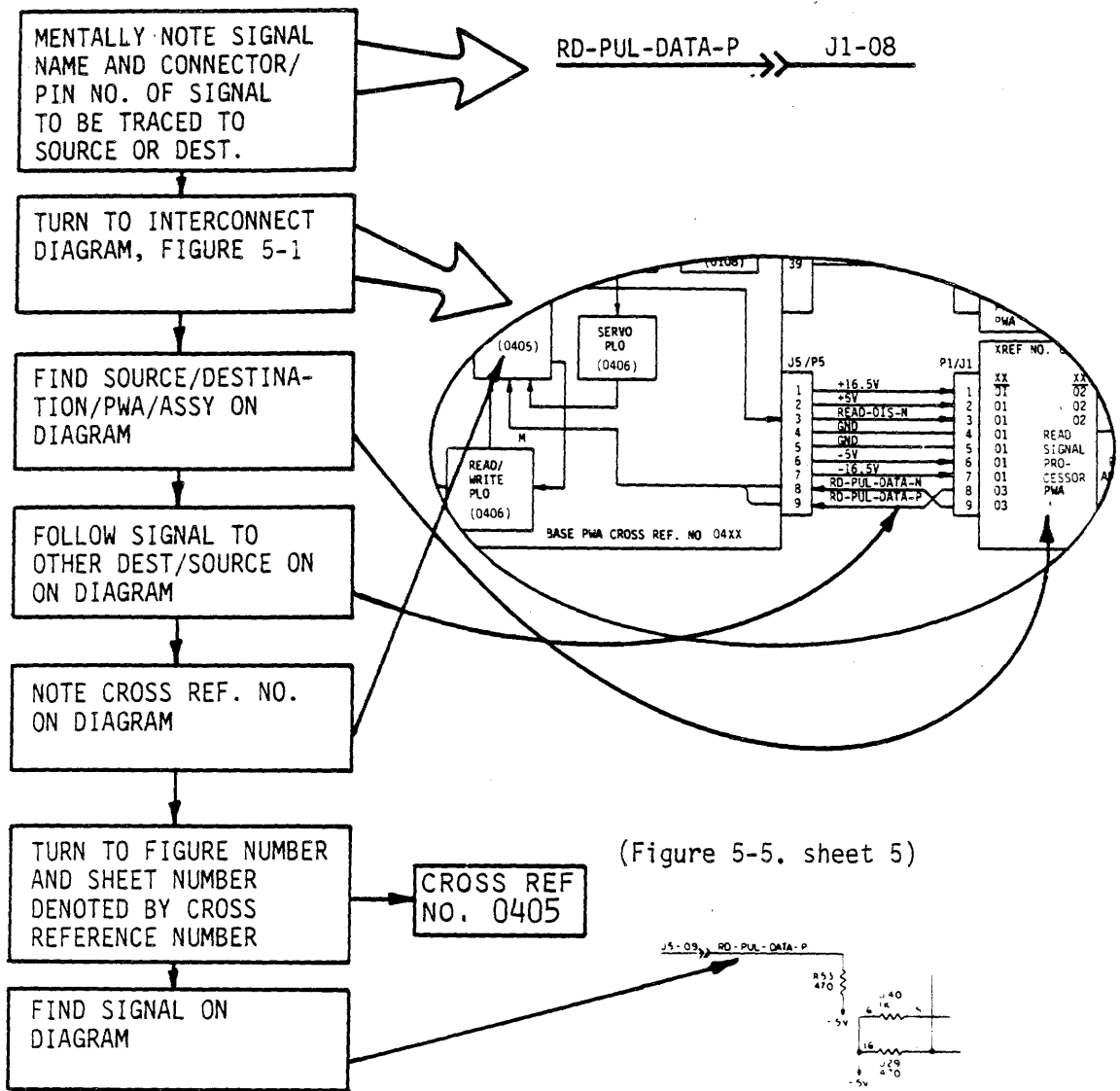


FIGURE 5-2B. SUMMARY OF SIGNAL TRACING PROCEDURE

5.3.2 CROSS REFERENCE NUMBERS

The cross reference number is located in the lower right hand corner of each schematic sheet. The first two digits (left-most) indicate the figure number of the schematic and the right-most digits indicate the sheet number of the schematic set. The documentation set for each board consists of a circuit board assembly and the schematic sheets. The schematic set is numbered using the Cross Reference numbers. Figure 5-2a shows an example for the Figure 5-4 schematic set.

The "-4" part of the 5-4 figure number is used in the cross reference number.

5.3.3 SUMMARY: POINT-TO-POINT INTERCONNECTION SIGNAL TRACING

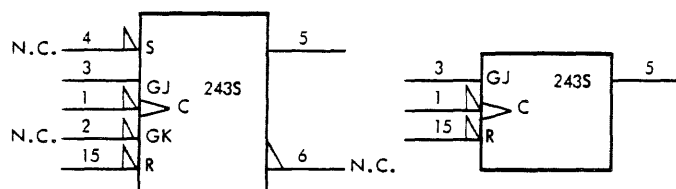
Figure 5-2b summarizes the procedure for tracing signals board-to-board (or "other assembly"-to-board and vice-versa).

5.4 LOGIC DIAGRAM SYMBOLOGY

5.4.1 GENERAL INFORMATION

Logic symbols are drawn with inputs on the left and outputs on the right whenever space and layout permit.

Power supply connections, discrete timing components, etc, may be shown connected to the top or bottom of the symbol. Unused pins and unused elements need not be shown. Figure 5-3 illustrates functionally equivalent symbols.



BOTH SYMBOLS REPRESENT A BI-STABLE JK F/F CIRCUIT WITH SOME OF THE PINS UNUSED. (N.C. INDICATES "NOT CONNECTED")

(X370b)

FIGURE 5-3. FUNCTIONALLY EQUIVALENT SYMBOLS

5.4.2 GENERAL SIGNAL ANNOTATION

- S = Set input to bistable device
- R = Reset (Clear) input to bistable device
- G = Gate input has no direct action on circuit, but must be present before inputs (and/or outputs) are able to function. If more than one gate is used, a numeric suffix is added (G1, G2, etc.).
- D = Identifies a signal which requires the presence of another signal to perform its function.
- C = Strobe pulse. Usually used to gate "D" inputs into a bistable device.

F = Enable output on tristate chips.
243S= Example CDC element identifier.

Non-standard binary level (—) indicators are generally shown where there was even a small expectation that one of the levels might be outside the standard defined tolerance of the logic family section. The logic levels may depend on such things as terminations or loads. The standard binary levels were assumed to be:

TABLE 5-2. LOGIC LEVEL DEFINITIONS

| <u>LOGIC FAMILY</u> | <u>LO LEVEL</u> | <u>HI LEVEL</u> |
|---------------------|------------------|------------------|
| TTL | 0.0 to +0.8 V | +2.4 to +5 V |
| ECL | -2.0 V to -1.4 V | -1.0 V to -0.6 V |

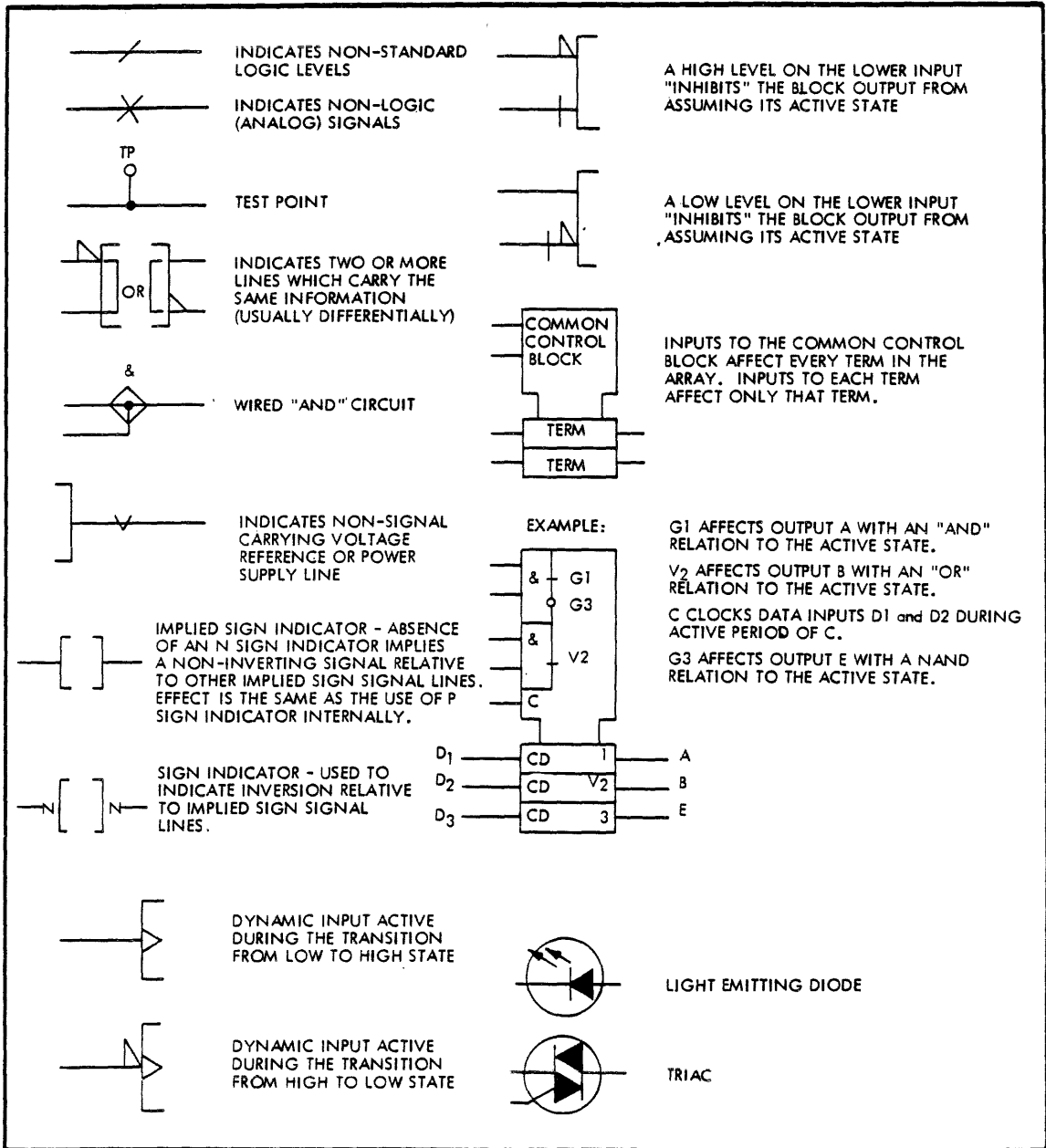
Logic signals that are "Active-Hi" have the appendage /+L attached to their names, and Logic signals that are "Active-Lo" have the appendage /-L attached. For example, the signal FLT-RESET /+L will be "Low" (logic 0) most of the time except when the fault circuitry is to be reset (Fault indication cleared). FLT-RESET /+L will go "Active-Hi" (Logic 1) for a brief instant when the fault circuitry is to be cleared. Active-Hi/Low will be shown by "-P" and "-N" for ECL signals.

Table above defines voltage levels for "Hi" and "Lo".

5.4.3 SYMBOLOGY

Logic Symbols are as described in Table 5-3.

TABLE 5-3. LOGIC SYMBOLY



(X370a)

5.4.4 FUNCTION SYMBOLOGY

Function symbols are described in Table 5-4.

TABLE 5-4. FUNCTION SYMBOLS

| CONTROL GATE INPUT - AFFECTS INPUTS OR OUTPUTS WITH "AND" RELATION TO ACTIVE STATE | |
|------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | OSCILLATOR |
| | AMPLIFIER |
| | "AND" GATE |
| | "OR" GATE |
| | "EXCLUSIVE OR" |
| | FUNCTION GENERATOR |
| | LEVEL CONVERSION |
| | SCHMITT TRIGGER |
| | SINGLE SHOT |
| | SUMMING CIRCUIT |
| | THRESHOLD (ANALOG OUTPUT) OR COMPARATOR (BINARY OUTPUT) PRODUCES A CHANGE IN THE OUTPUT SIGNAL WHEN INPUT EXCEEDS A PREDETERMINED LEVEL "m". |
| D | DATA INPUT |
| C | CONTROL or CLOCK INPUT |
| G | CONTROL GATE INPUT - AFFECTS INPUTS OR OUTPUTS WITH "AND" RELATION TO ACTIVE STATE. |
| V | CONTROL GATE INPUT - AFFECTS INPUTS OR OUTPUTS WITH AN "OR" RELATION TO THE ACTIVE STATE. |
| | DECODER |
| | DIGITAL TO ANALOG CONVERTER |
| mVR | VOLTAGE REGULATOR OUTPUT VALUE "m" |
| MUX | MULTIPLEXER |
| SR | SHIFT REGISTER |
| CNTR | COUNTER |
| ALU | ARITHMETIC LOGIC UNIT |
| RCVR | RECEIVER |
| (M) | ANNOTATION RESTRICTING THE NUMBER OF COINCIDENT INPUTS OR OUTPUTS GROUPED BELOW IT ACCORDING TO M. EXAMPLE: (≤ 1) MEANS ONLY ONE OR LESS COINCIDENT INPUT OR OUTPUT BELOW ALLOWED. |
| | WIRED "OR" OR WIRED "AND", OR OPEN COLLECTOR OR EMITTER CIRCUIT CAPABLE OF BEING USED AS WIRED "OR" OR "AND", SUCH AS ON BUS DRIVER CIRCUITS. |
| | NEGATING INDICATOR |
| | BILATERAL SWITCH. BINARY CONTROLLED, PASSES OR BLOCKS ANALOG OR BINARY SIGNALS IN EITHER DIRECTION. |

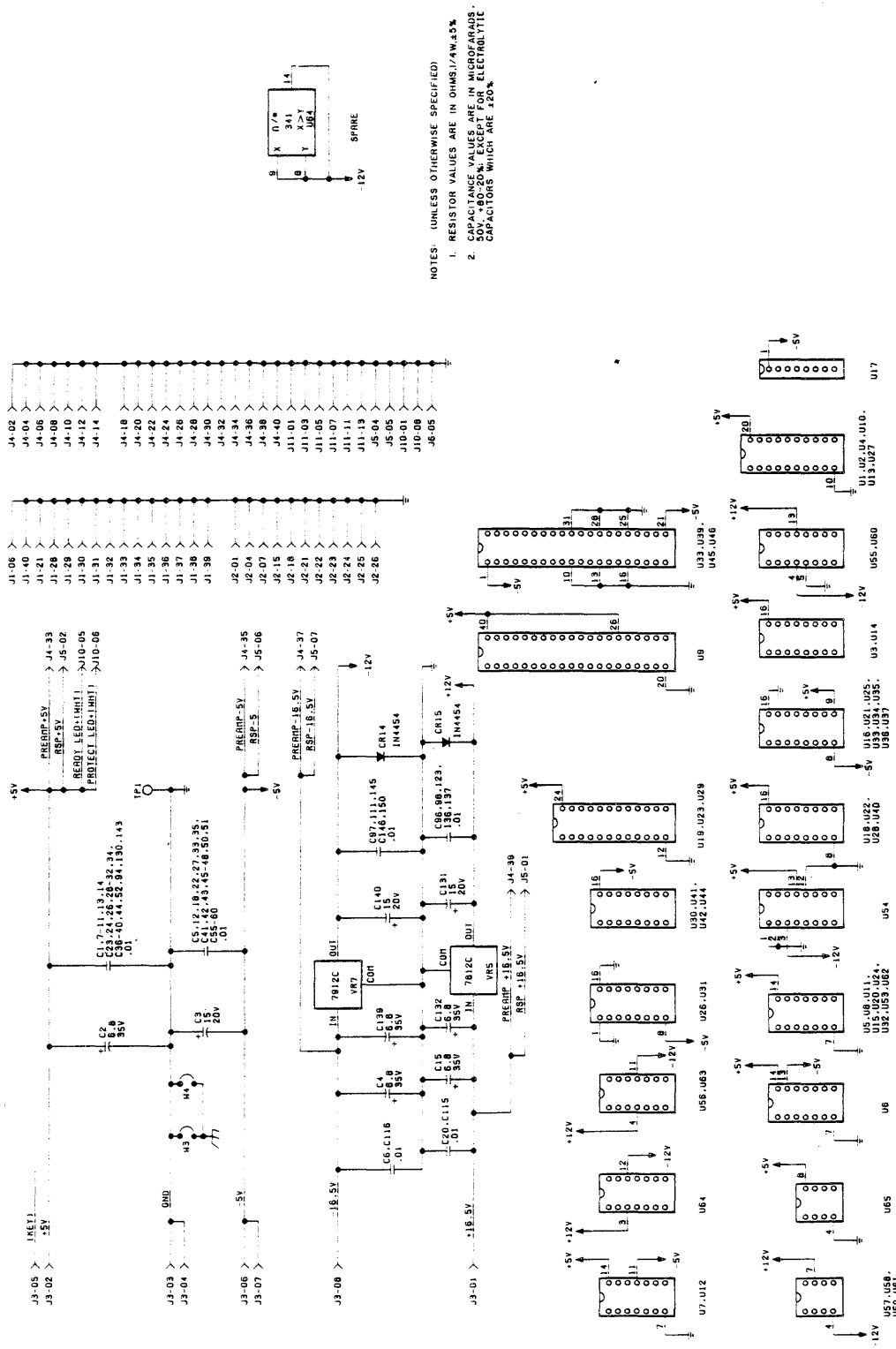
(X368a)

5.5 LOGIC DIAGRAMS AND SCHEMATICS

The diagram sets other than the printed circuit board diagram sets are the logic diagrams and schematics for the circuits of the LMU, the interface adapter and the power supply. Transistor types and Integrated circuit types are given on each device on the diagrams so that the vendor catalogs may be consulted for information about internal circuitry, characteristics of input and output signals, typical timing and so forth.

5.5.1 BASE PWA MATRIX

64 Sector operation is obtained by shorting the pins of Base PWA J12 together with a pluggable jumper (at back of LMU). 32 Sector operation is obtained by removing the jumper.



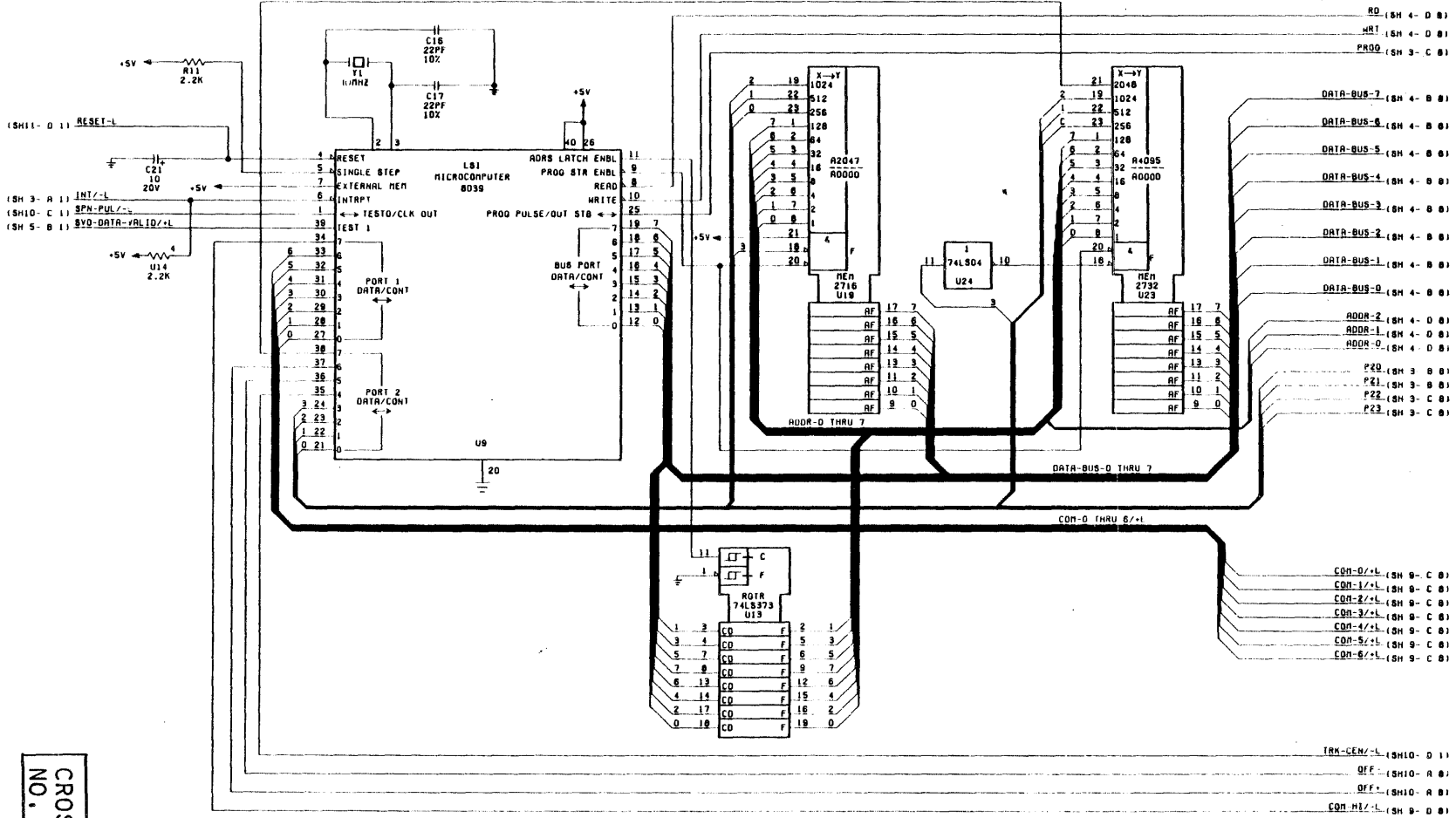
- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. RESISTOR VALUES ARE IN OHMS/4W.45%
 2. CAPACITANCE VALUES ARE IN MICROFARADS. 50V, 100-20M, EXCEPT FOR ELECTROLYTIC CAPACITORS WHICH ARE 120V.

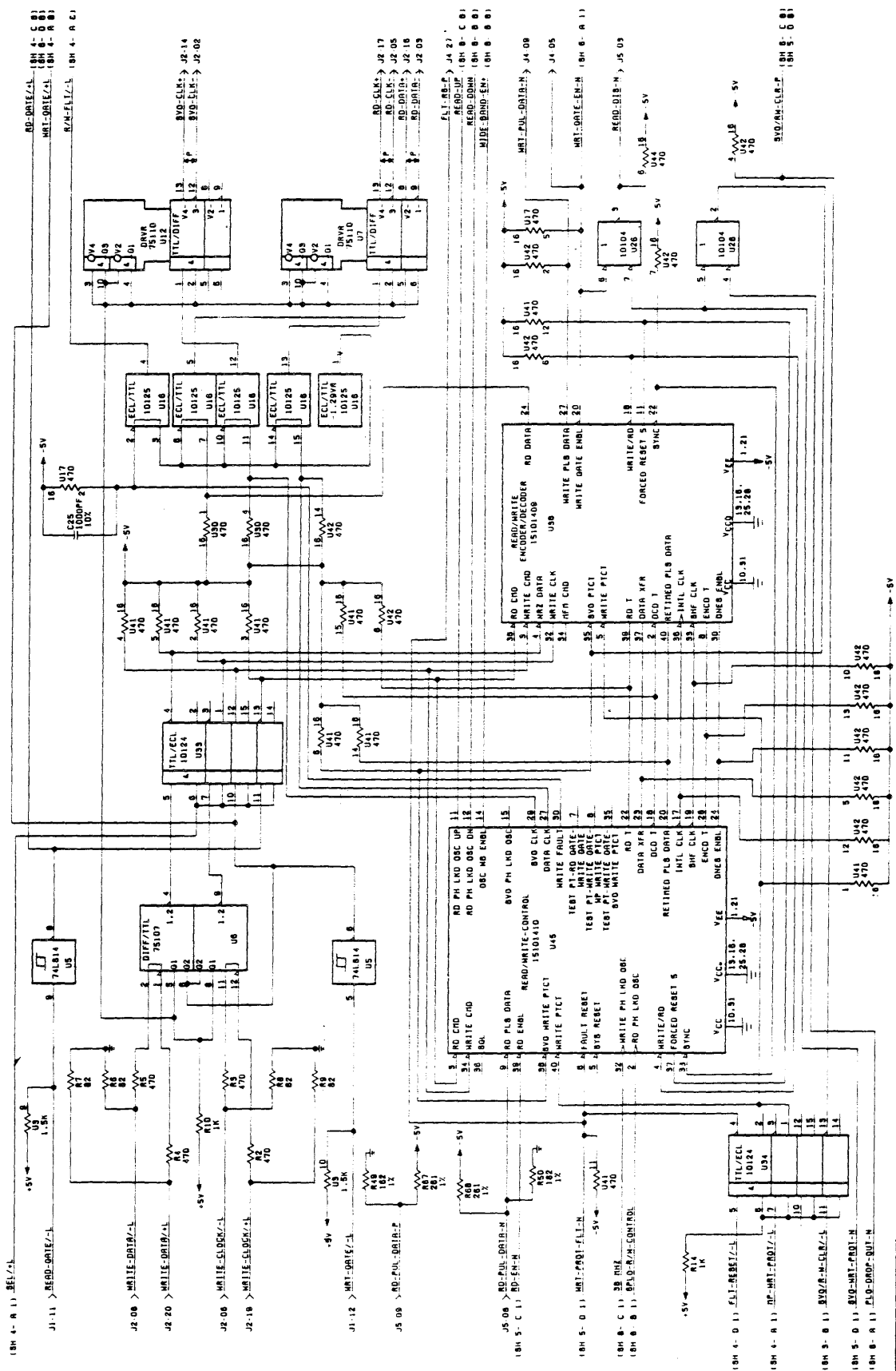
CROSS REF
NO. 0401

FIGURE 5-4. BASE SCHEMATIC (SHEET 1 OF 12)

FIGURE 5-4, BASE SCHEMATIC (SHEET 2 OF 12)

CROSS REF
NO. 0402





CROSS REF
NO. 0407

77711052-A **FIGURE 5-4. BASE SCHEMATIC (SHEET 7 OF 12)** 5-17

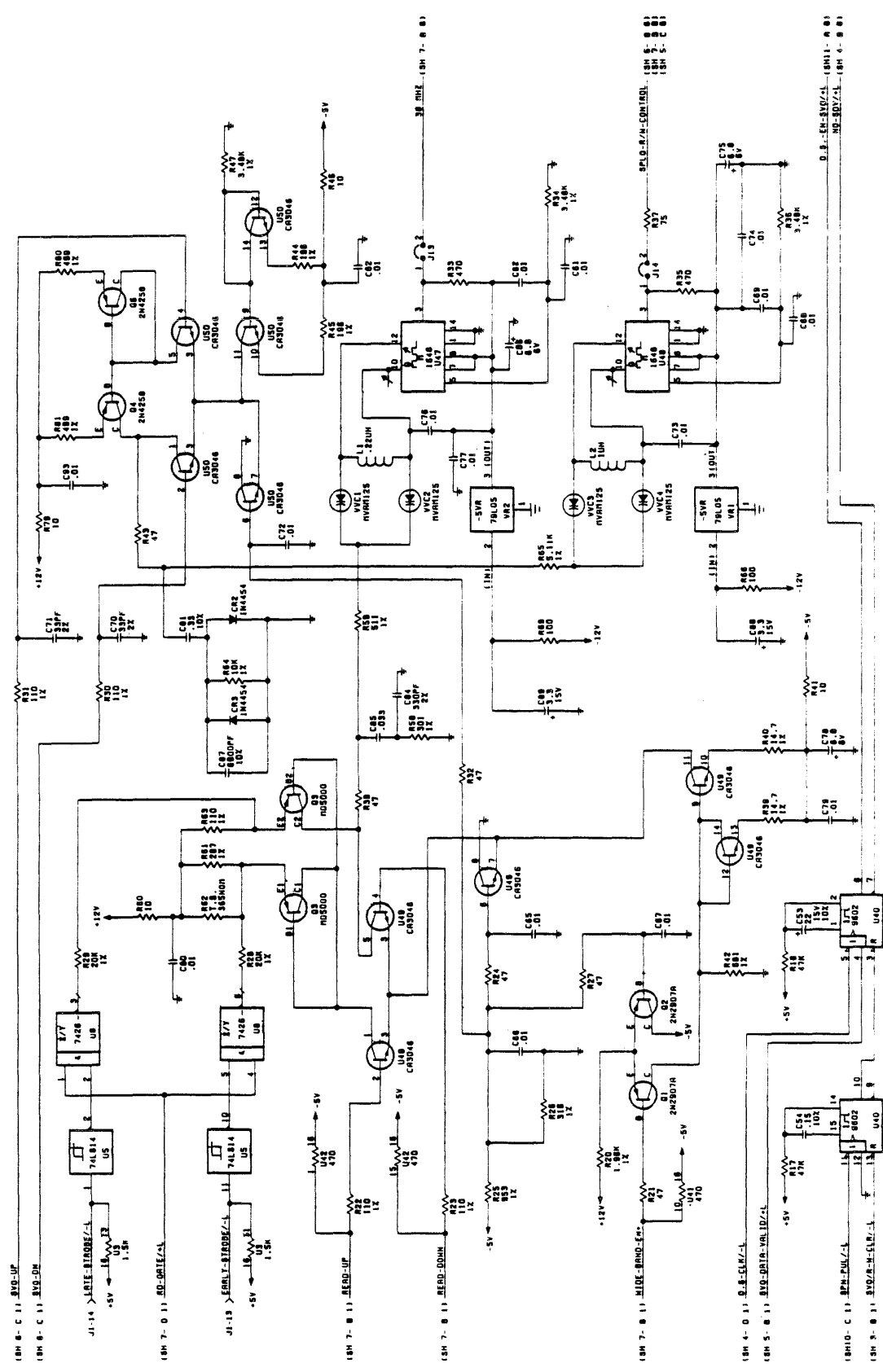
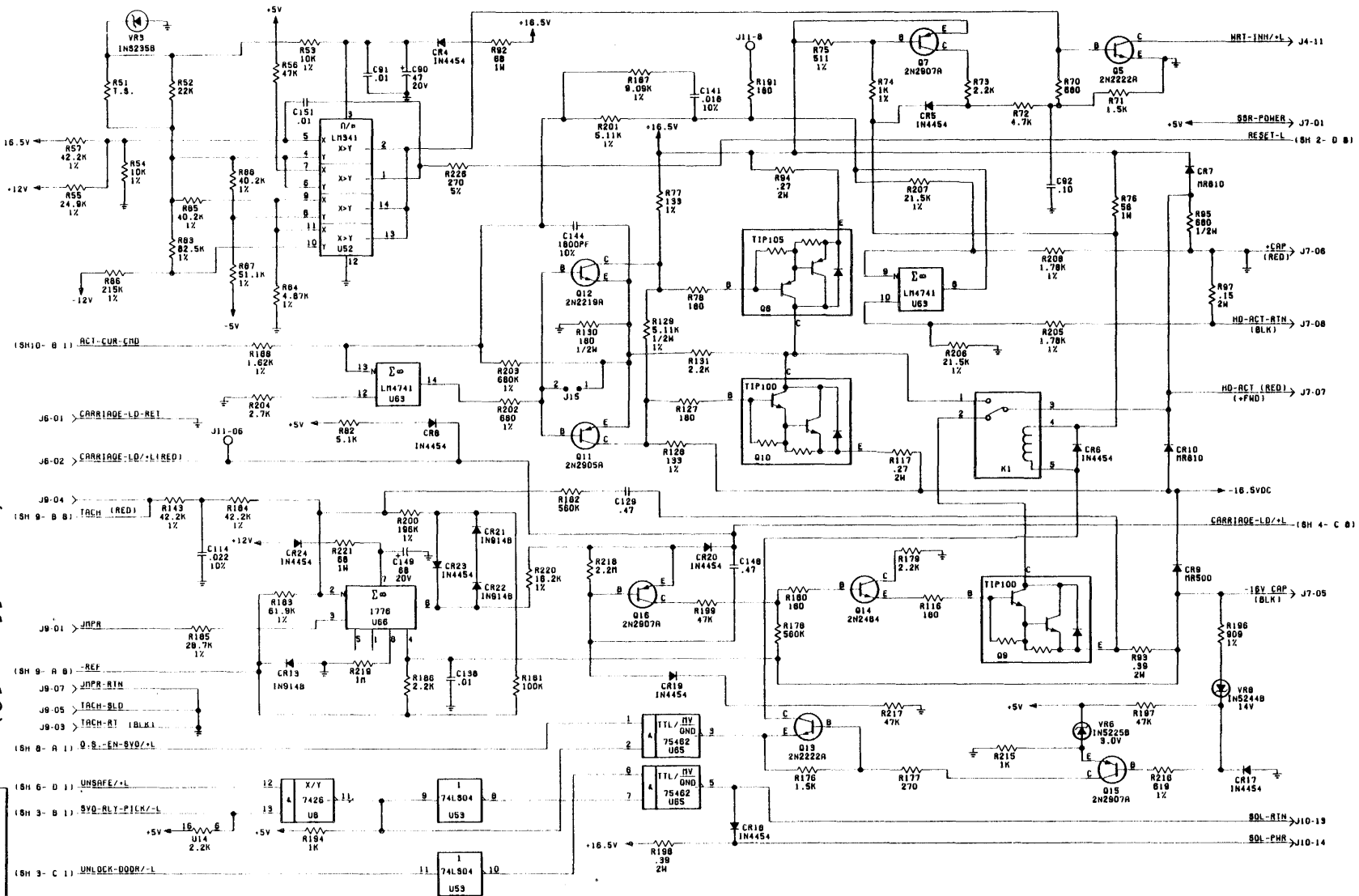


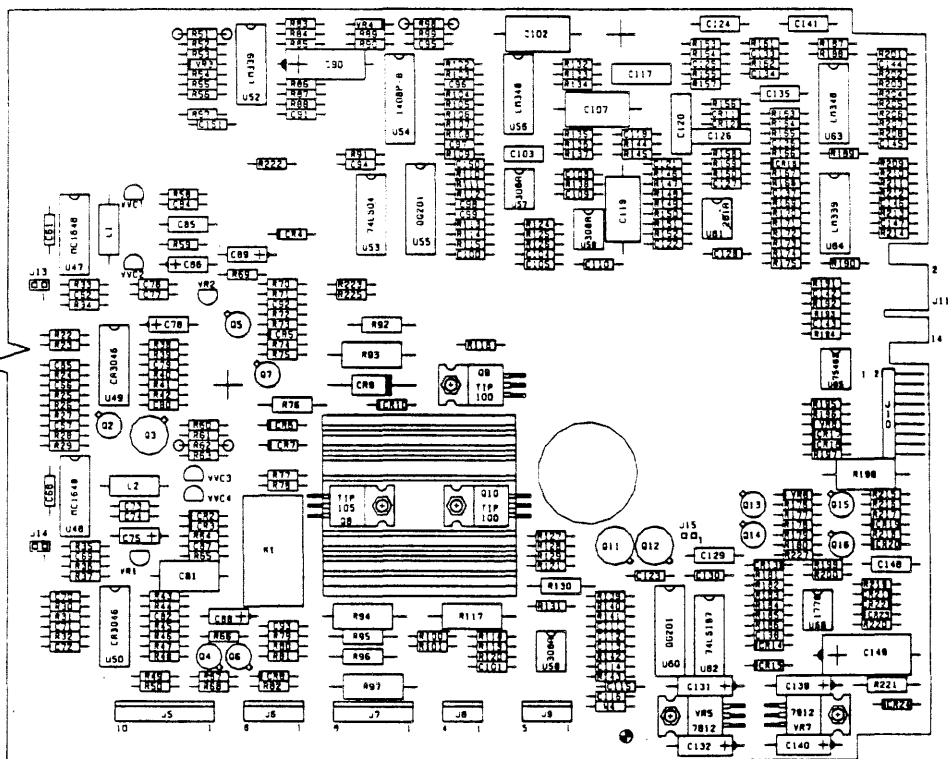
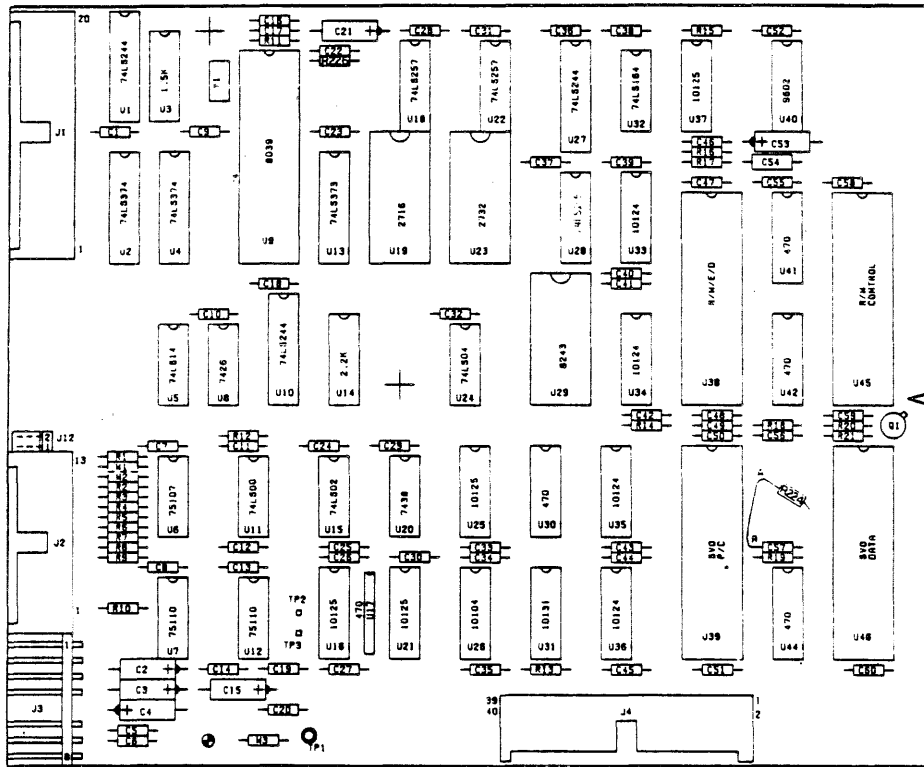
FIGURE 5-4. BASE SCHEMATIC (SHEET 8 OF 12)

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NO. 0408

FIGURE 5-4. BASE SCHEMATIC (SHEET 11 OF 12)

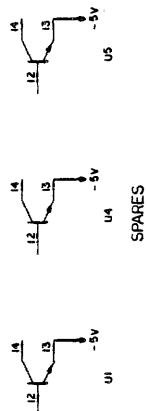
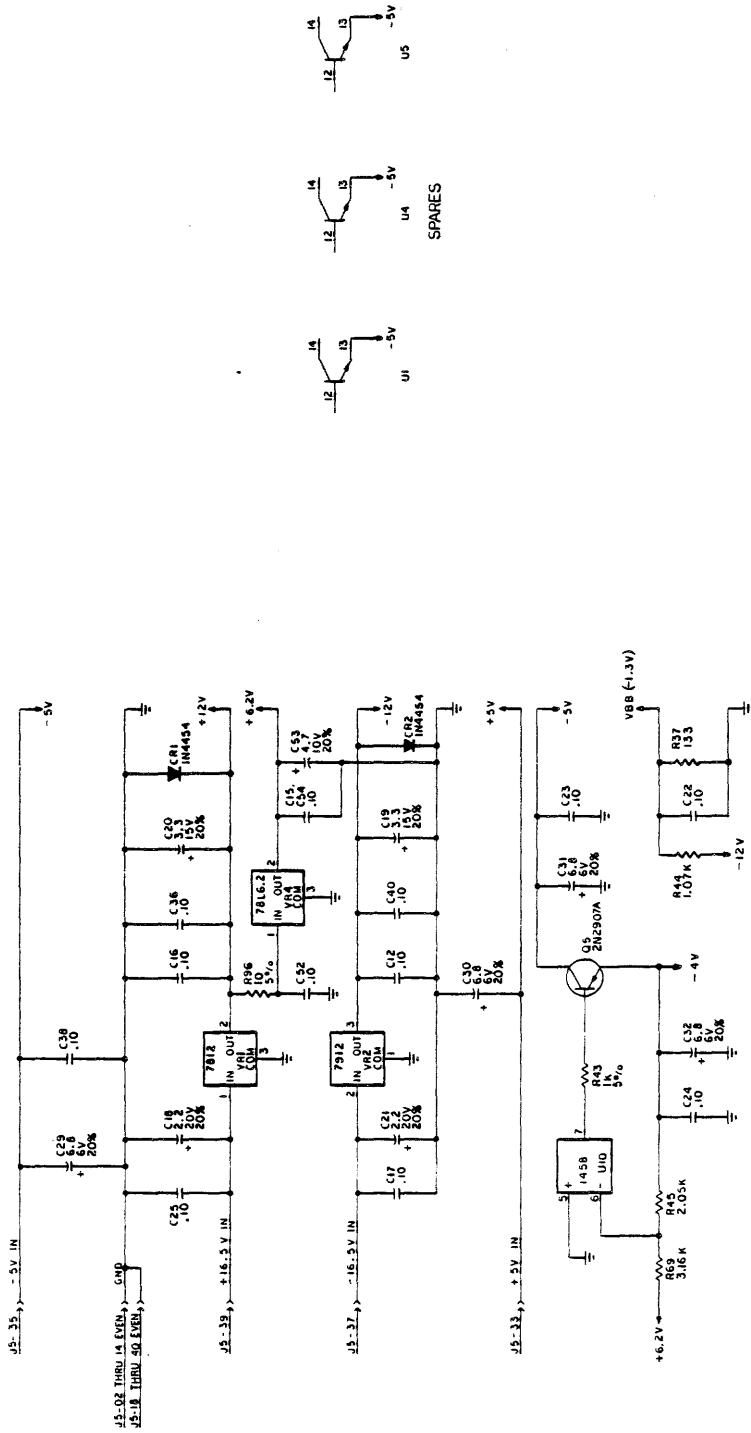


CROSS REF NO. 0411

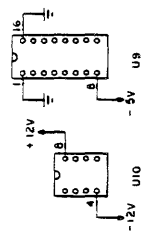


(FF182a)

FIGURE 5-4. BASE PWA (SHEET 12 OF 12)



NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTOR VALUES ARE IN OHMS, 1/4W, ±1%
 2. CAPACITANCE VALUES ARE IN MICROFARADS, 50V, ±20%
 3. TRANSISTOR PACKAGES ARE CA3046-(U1,U4,U5,
 U12,U14)



CROSS REF
 NO. 0501

FIGURE 5-5. R/W PREAMP SCHEMATIC (SHEET 1 OF 4)

FIGURE 5-5. R/W PREAMP SCHEMATIC (SHEET 2 OF 4)

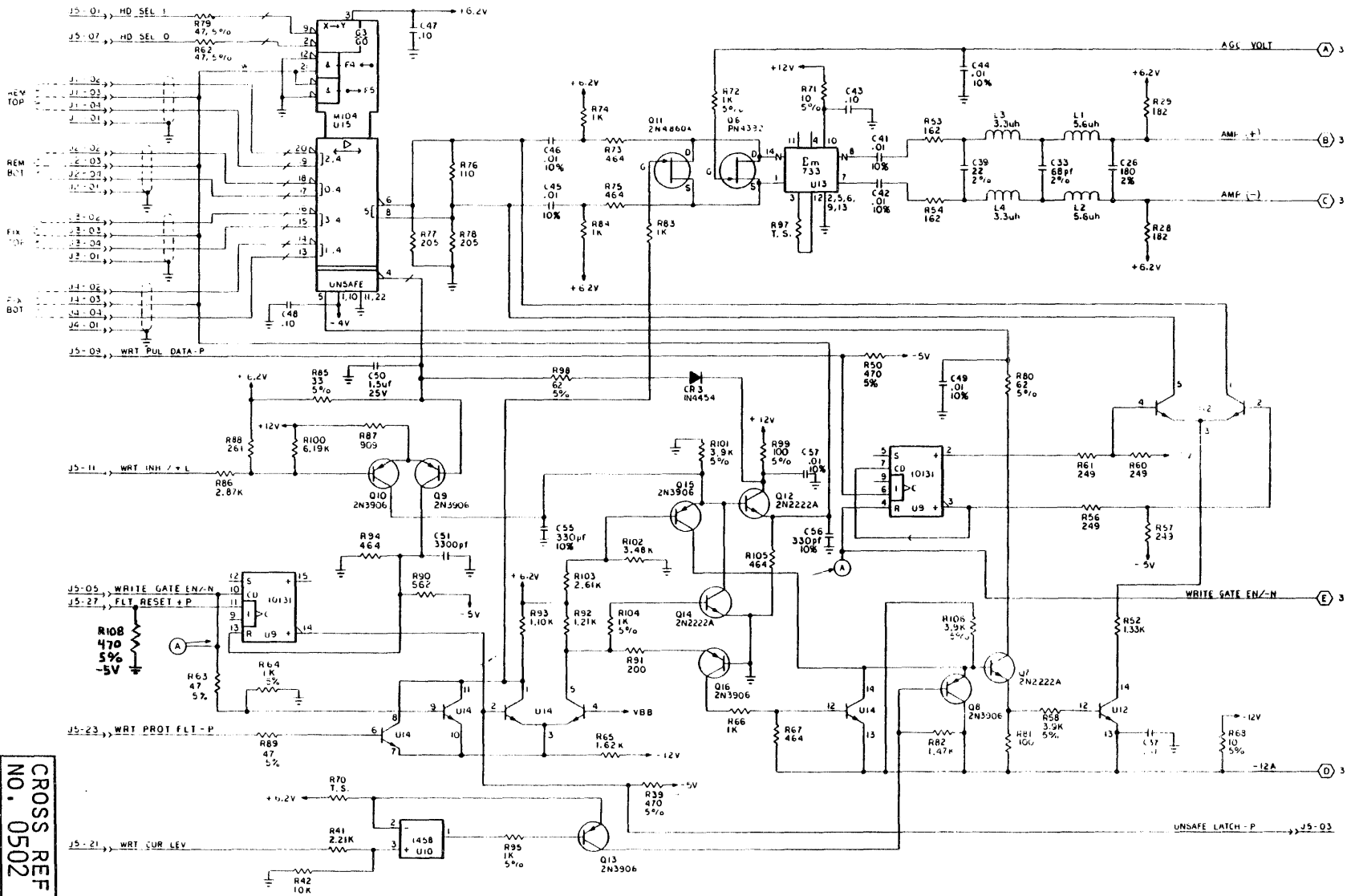
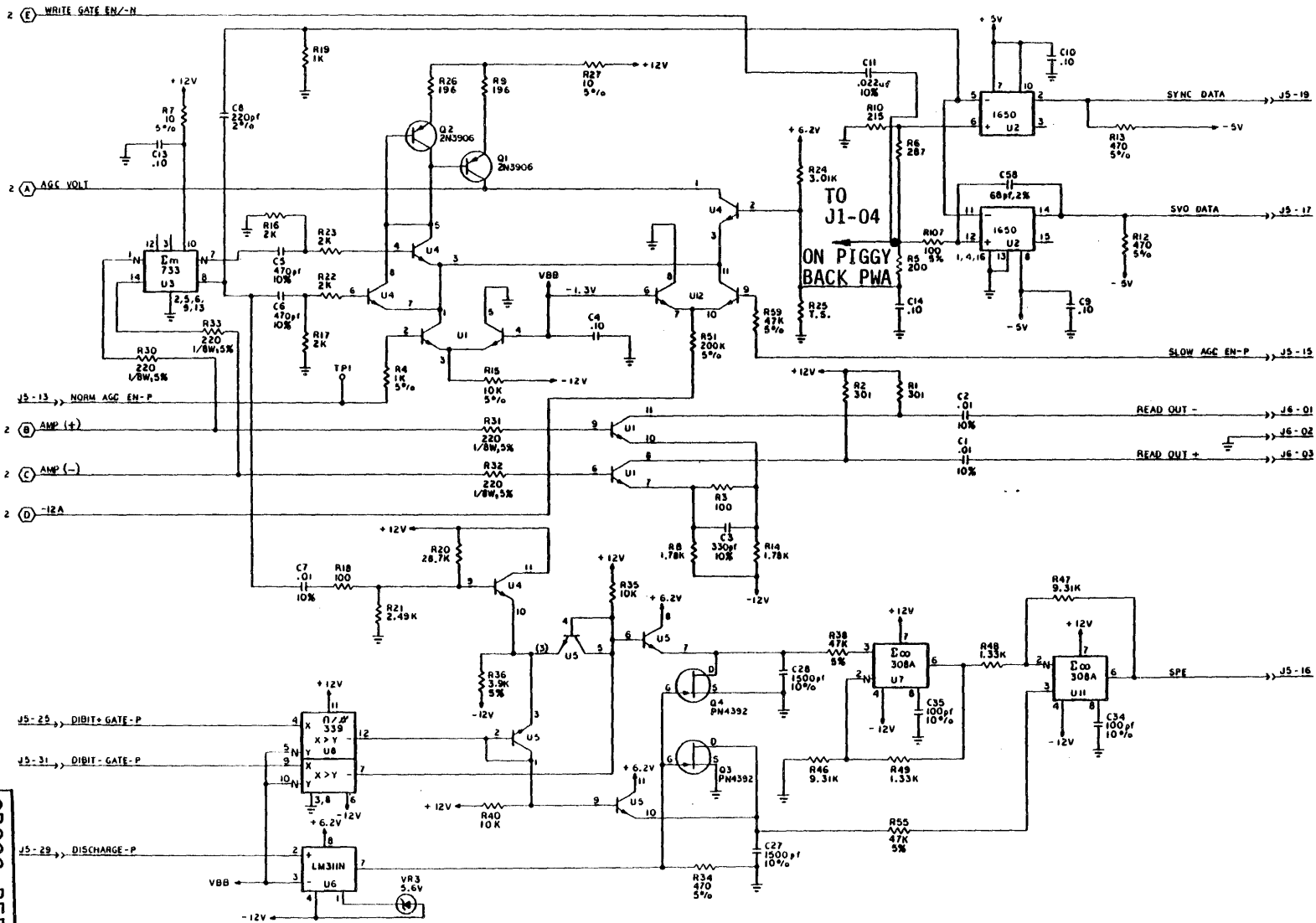


FIGURE 5-5. R/W PREAMP SCHEMATIC (SHEET 3 OF 4)



CROSS REF
NO. 0503

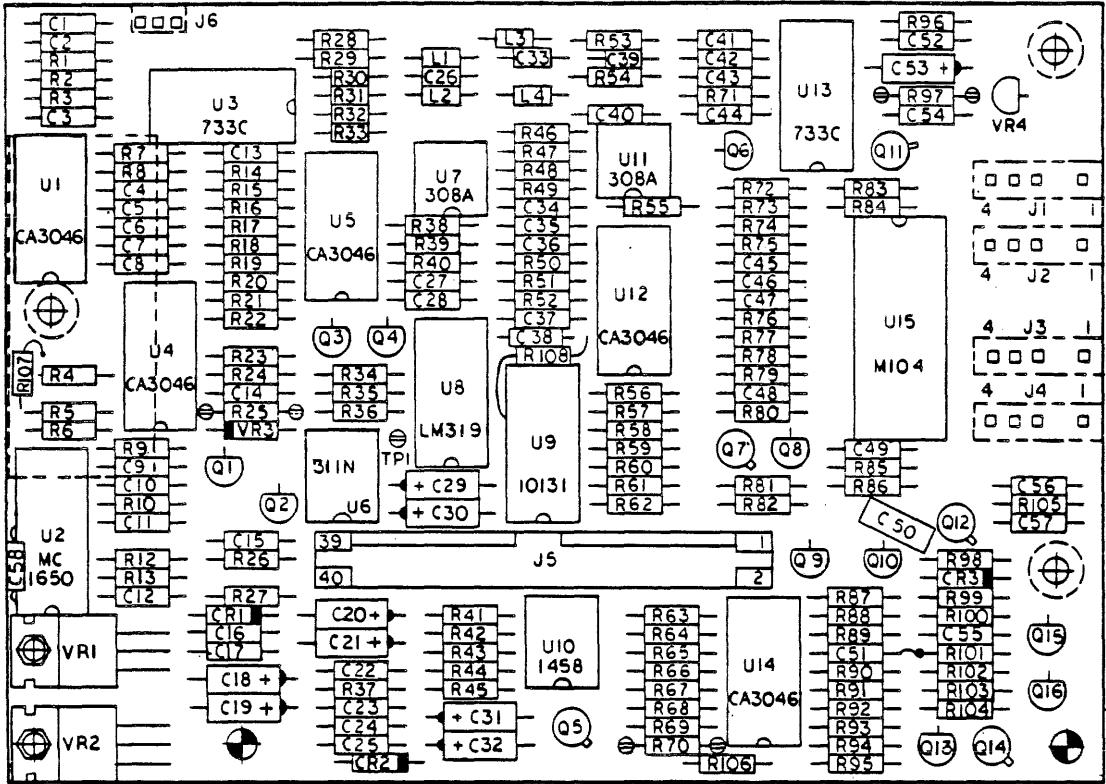
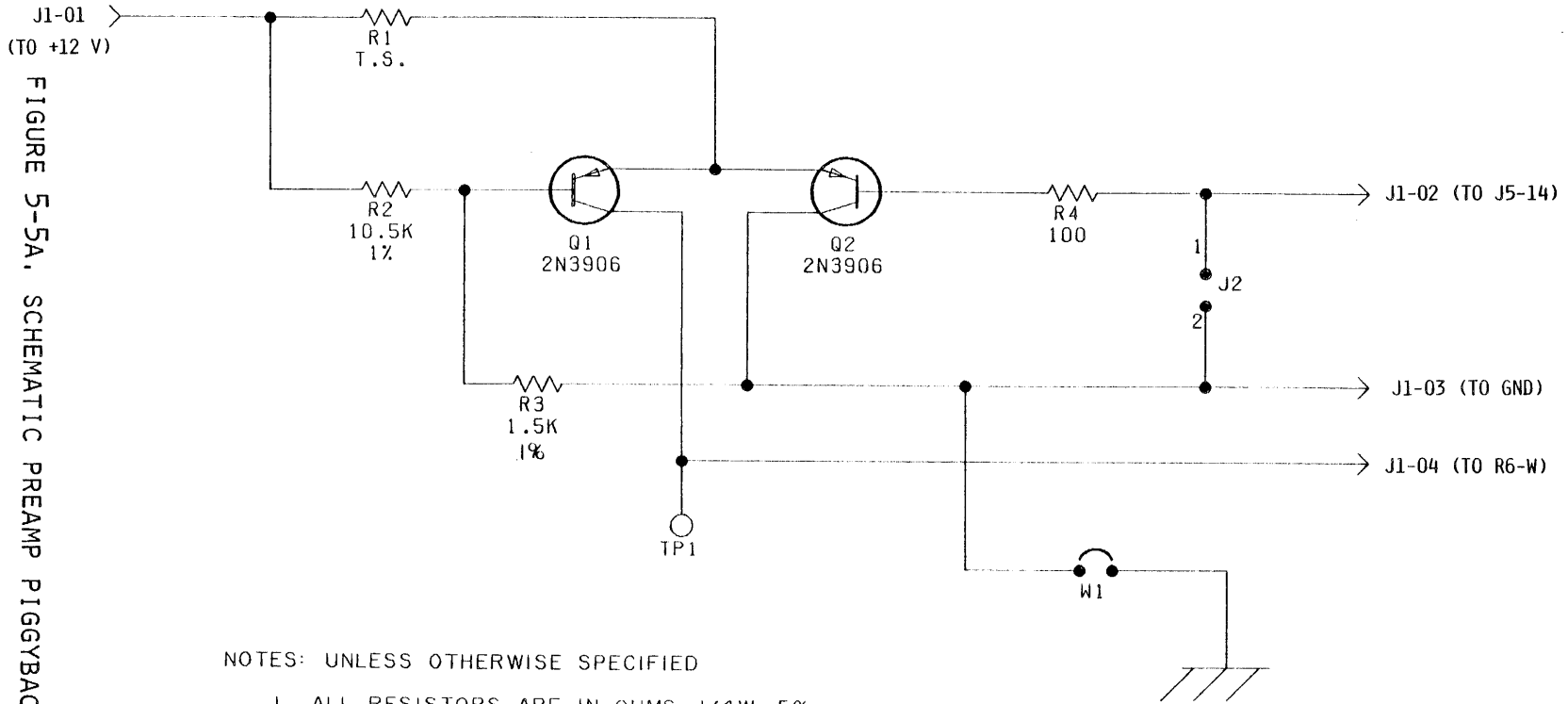


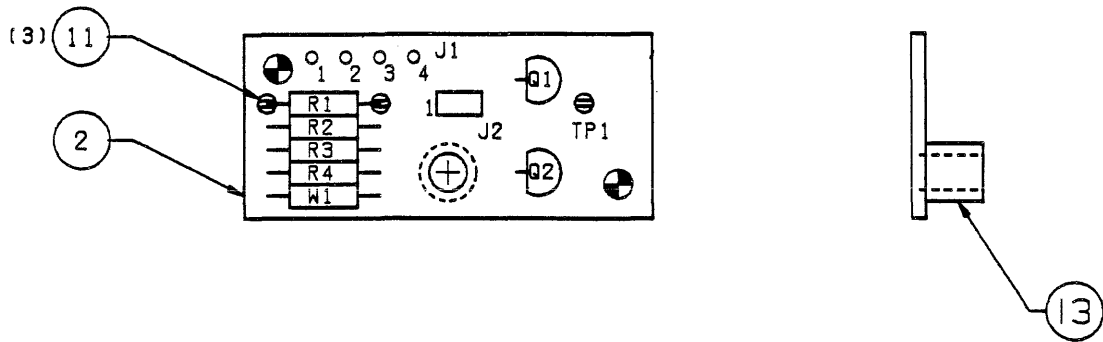
FIGURE 5-5. R/W PREAMP PWA (SHEET 4 OF 4)

FIGURE 5-5A. SCHEMATIC PREAMP PIGGYBACK



NOTES: UNLESS OTHERWISE SPECIFIED

I. ALL RESISTORS ARE IN OHMS, 1/4W, 5%



| RES | PL ITEM |
|-----|---------|
| R1 | 8 |
| R2 | 9 |
| R3 | 7 |
| R4 | 6 |

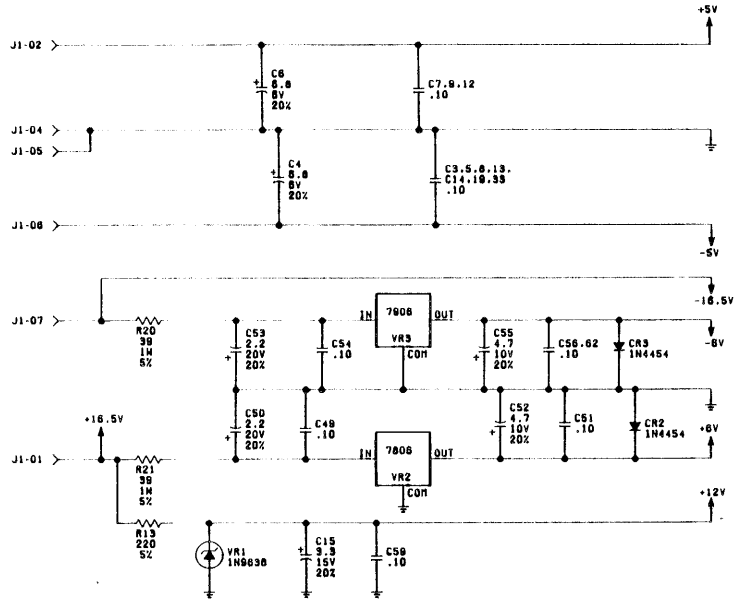
| TRAN | PL ITEM |
|------|---------|
| Q1 | 5 |
| Q2 | 5 |

| JMPR | PL ITEM |
|------|---------|
| W1 | 10 |

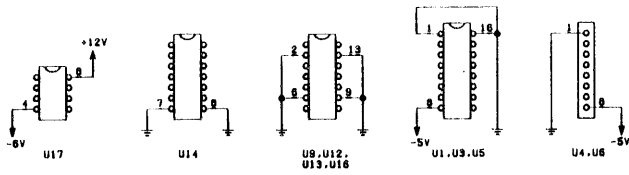
| CONN | PL ITEM |
|------|---------|
| J1 | - |
| J2 | 12 |

FIGURE 5-5A. PWA PREAMP PIGGYBACK

FIGURE 5-6. RSP SCHEMATIC (SHEET 1 OF 4)



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4WATT, 1%
 2. ALL CAPACITOR VALUES ARE IN MICROFARADS, +80-20%, 50V
 3. U2, U10, U11 & U15 ARE CA3046



CROSS REF
NO. 0601

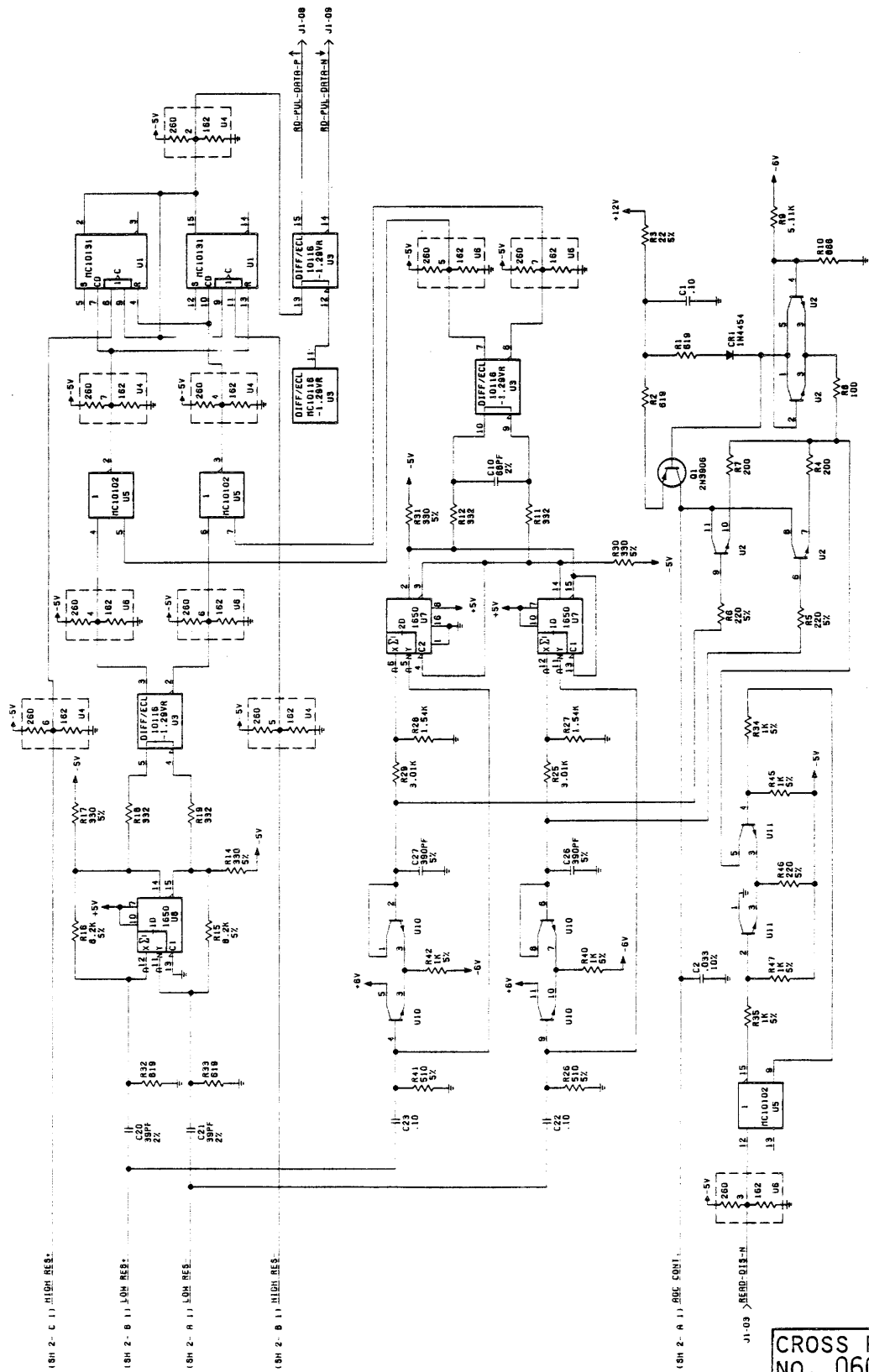


FIGURE 5-6. RSP SCHEMATIC (SHEET 3 OF 4)

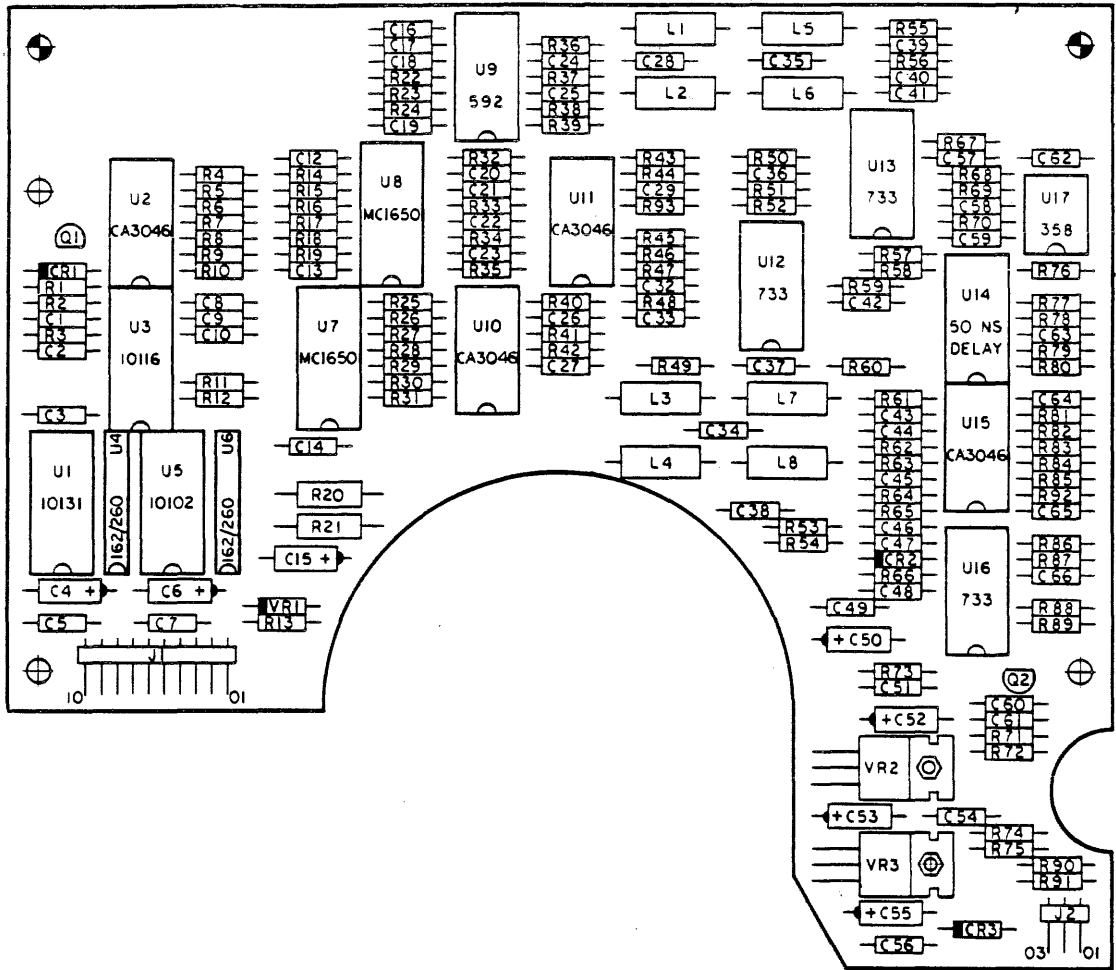


FIGURE 5-6. RSP PWA (SHEET 4 OF 4)

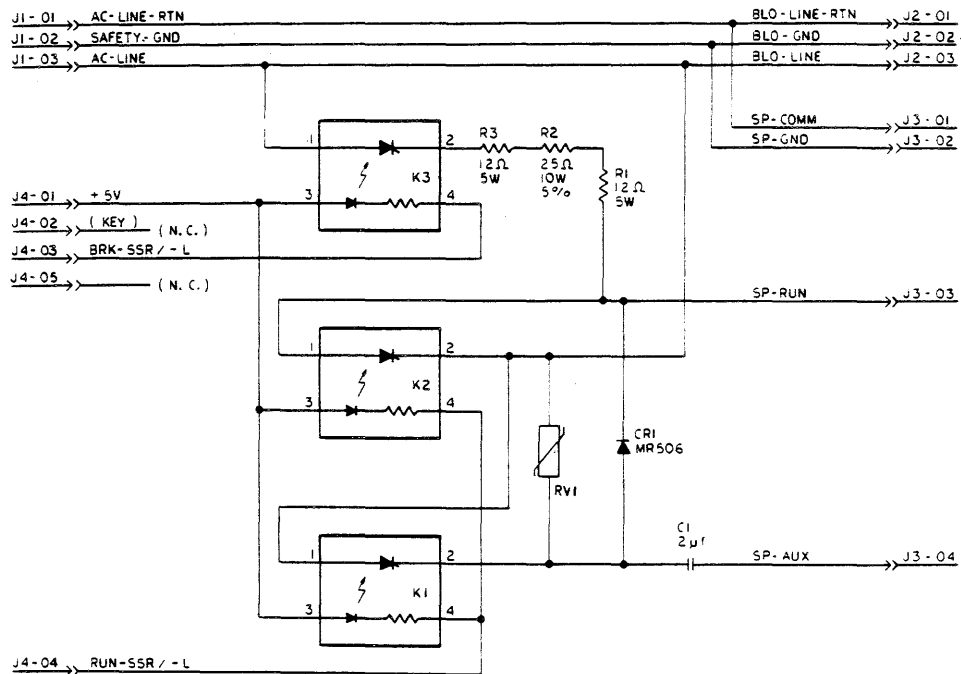


FIGURE 5-7. AC DISTRIBUTION SCHEMATIC
(SHEET 1 OF 2)

CROSS REF
NO. 0701

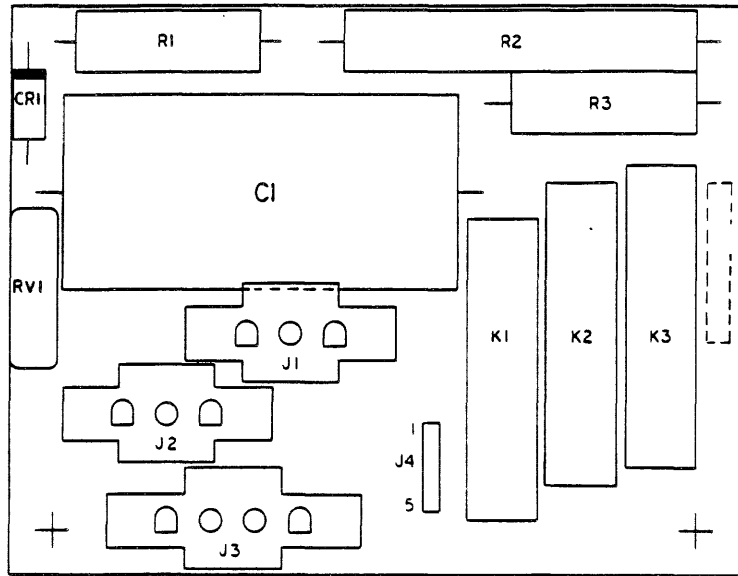
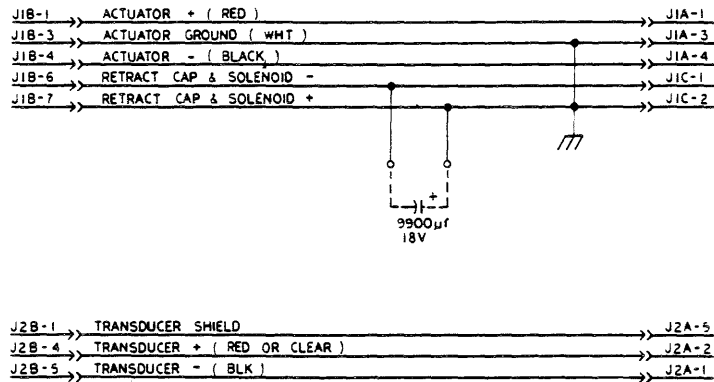


FIGURE 5-7. AC DISTRIBUTION PWA
(SHEET 2 OF 2)



NOTE:

1. J1A-2, J1B-2 & 5, J2A-3 & 4, AND J2B-2 & 3 ARE BLANK POSITIONS FOR POLARIZATION

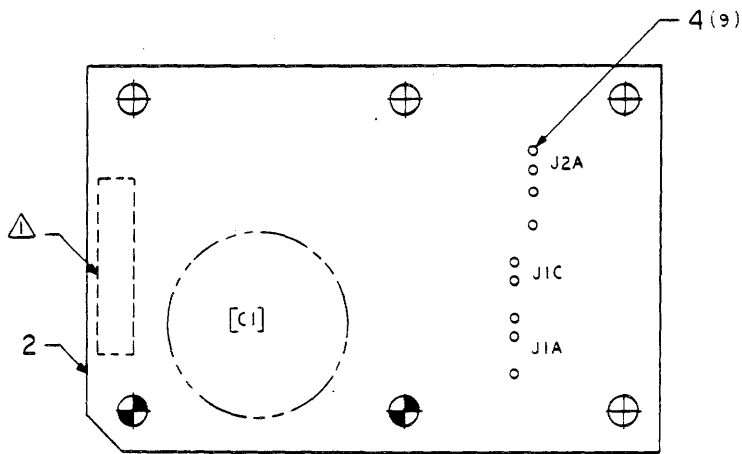
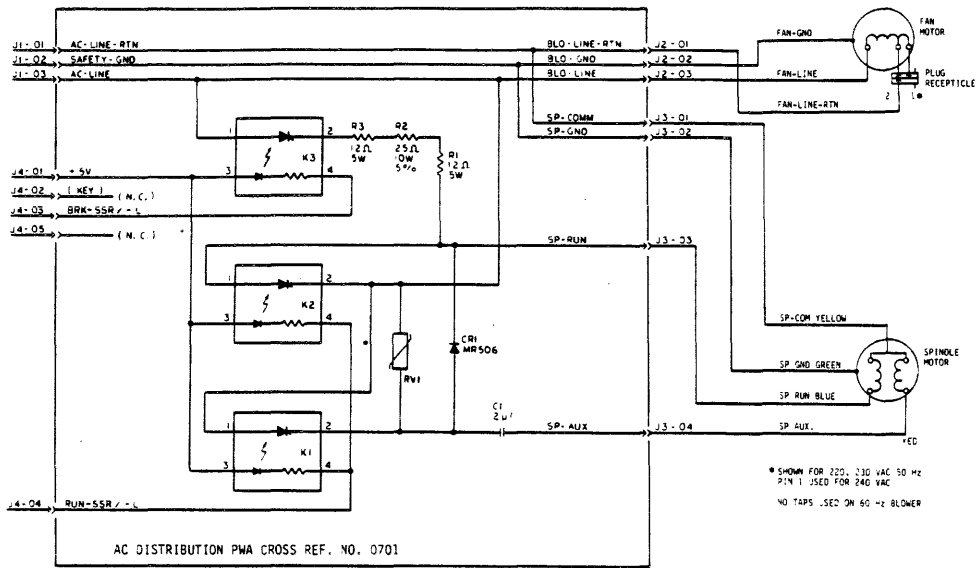


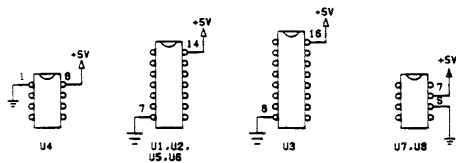
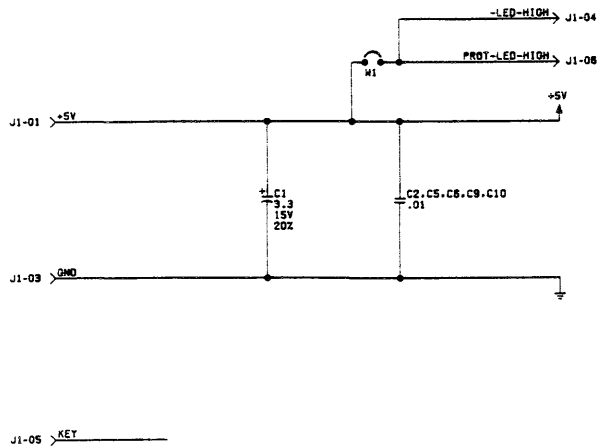
FIGURE 5-8, FEED THROUGH PWA



F133

CROSS REF
NO. 0901

FIGURE 5-9. AC POWER CONTROL FOR SPINDLE MOTOR AND BLOWER



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTOR VALUES IN OHMS, 1/4W, 5%
 2. ALL CAPACITOR VALUES IN MICROFARADS, 50V, +80%,-20%

CROSS REF
NO. 1001

FIGURE 5-10. STATUS DISPLAY SCHEMATIC (SHEET 1 OF 3)

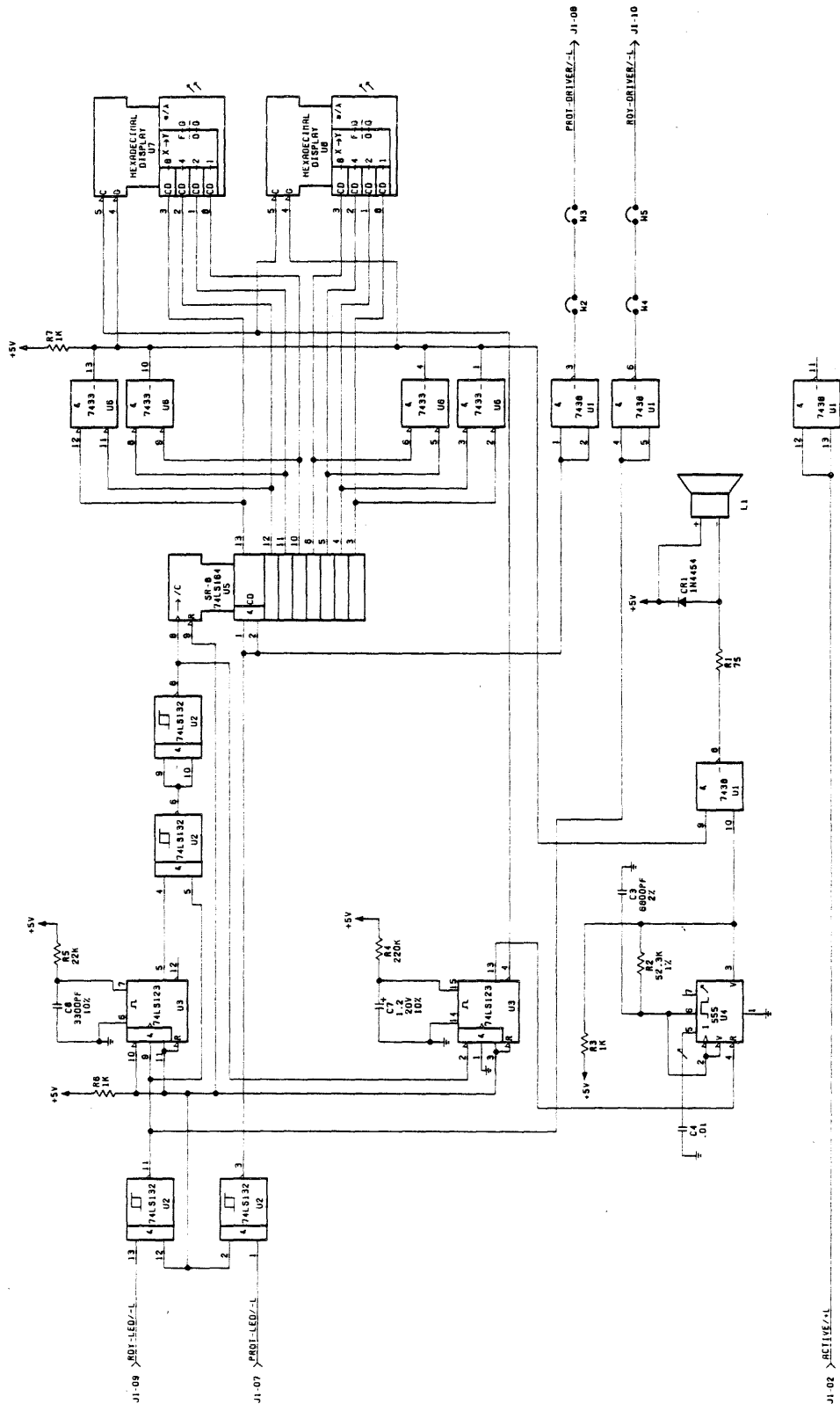


FIGURE 5-10. STATUS DISPLAY SCHEMATIC (SHEET 2 OF 3)

CROSS REF
NO. 1002

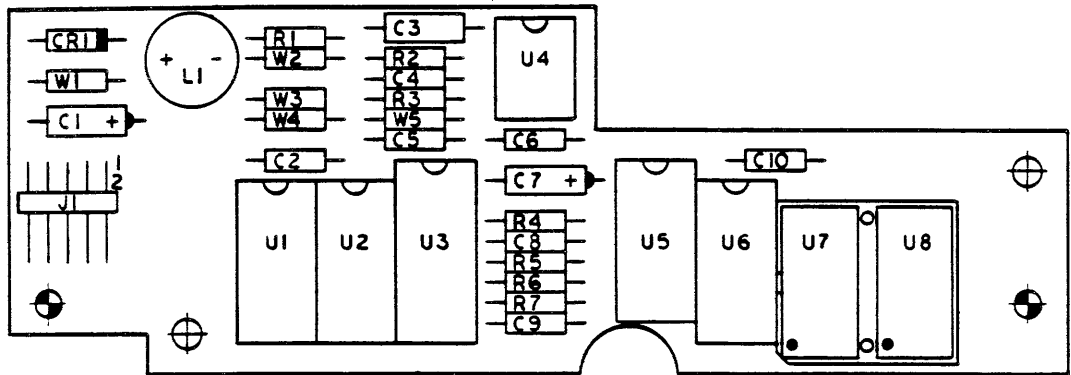


FIGURE 5-10. STATUS DISPLAY PWA (SHEET 3 OF 3)

5.6

I/O INTERFACE-LMU TO I/O ADAPTER

This section describes the characteristics of the interface between the LMU and the I/O adapter. Figure 5-11 shows a simple block diagram of the interface. One of the I/O cables is called the Command "C" cable and the other is called the Data "D" cable. Figure 5-12 and 5-13 show pin assignments for the two I/O cables. The I/O adapter mentioned in this section can be a controller or an adapter to another interface (i.e., SMD or other standard interface).

BUS TRANSFER LINES

The asynchronous portion of the interface uses a bidirectional bus for information transfer. The LMU drive directs the flow of information across the bus using the address and Bus Ready lines (see Figure 5-14). This situation allows a large amount of information to be transferred over the Bus without a great deal of logic in the I/O adapter board. The I/O adapter maintains control over the bus by initiating transfers of commands over the bus using the event line and controlling the rate of transfer using the acknowledge line. The specified timing is shown in Figures 5-17, 5-18, 5-19 and 5-20. Figure 5-21 shows a sequence of a transfer of a seek command and cylinder address to the drive. Figure 5-22 shows the resulting status information that is transferred back to the I/O adapter. Table 5-4 shows the definition of the information transferred across the command bus. Any status change in the drive is transferred back to the I/O Adapter in accordance with interrupt operation.

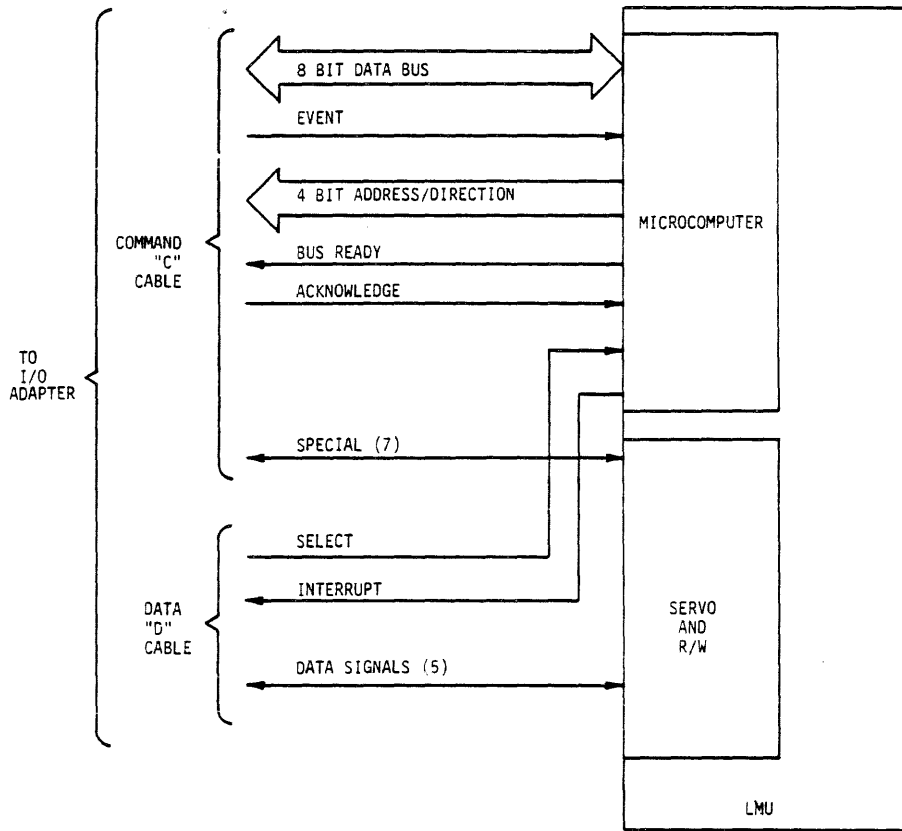
HIGH SPEED LINES

Certain signals must be transferred "instantaneously" across the interface to maintain critical timing. These signals are shown in Figures 5-15 and 5-16. All differential pair signals are transmitted and received according to the requirements for the SMD "B" cable. All single ended signals use tristate 74LS drivers and 74LS receivers. The receiver requires input hysteresis and input clamping diodes to provide low noise termination of incoming signals.

INTERFACE DIALOGUE

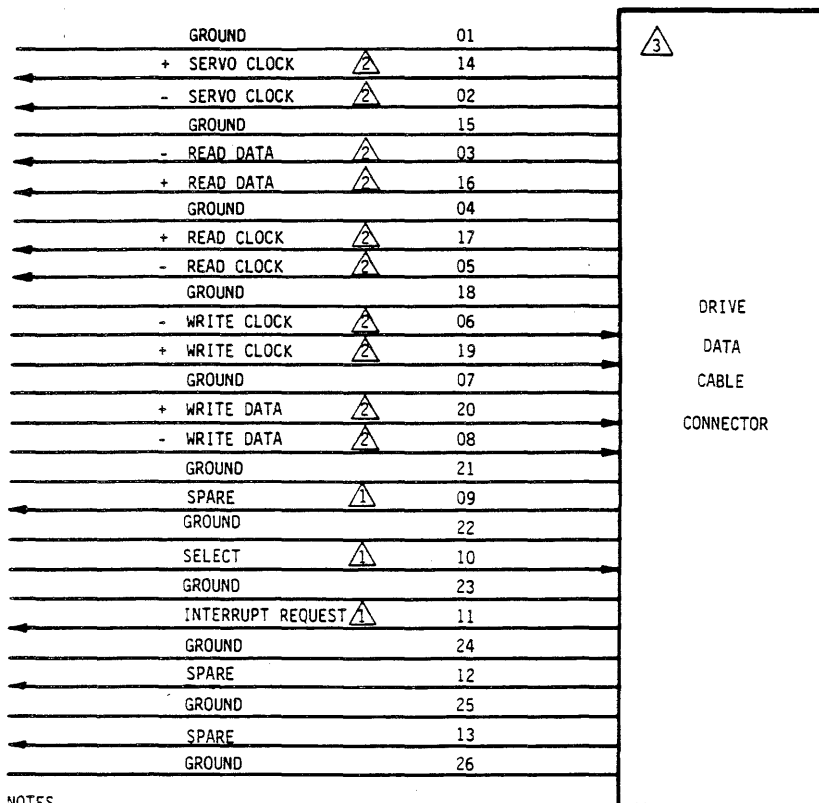
Interface dialogue is initiated by the adapter via a dedicated signal line called the "Event" line. The LMU then responds by requesting the adapter to transmit the Event Byte which contains information relative to the desired activity. Subsequent requests for additional bytes of information from the adapter may occur as a function of the Event Byte transfer.

For example, if the Event Byte requested a head change, the LMU would respond by asking for the desired head address. Multiple operations may be requested within a single Event Byte transfer to minimize interface dialogue. Table 5-5 details combinations of valid multiple events and the complementary information, the LMU will begin execution of the Event in a prescribed manner. At the completion of the Event(s), the LMU will request the adapter to receive current status of the LMU in one of two modes. In one of these modes an automatic status transfer will be requested. The adapter should be prepared to respond to this request.



G148a

FIGURE 5-11. LMU INTERFACE BLOCK DIAGRAM

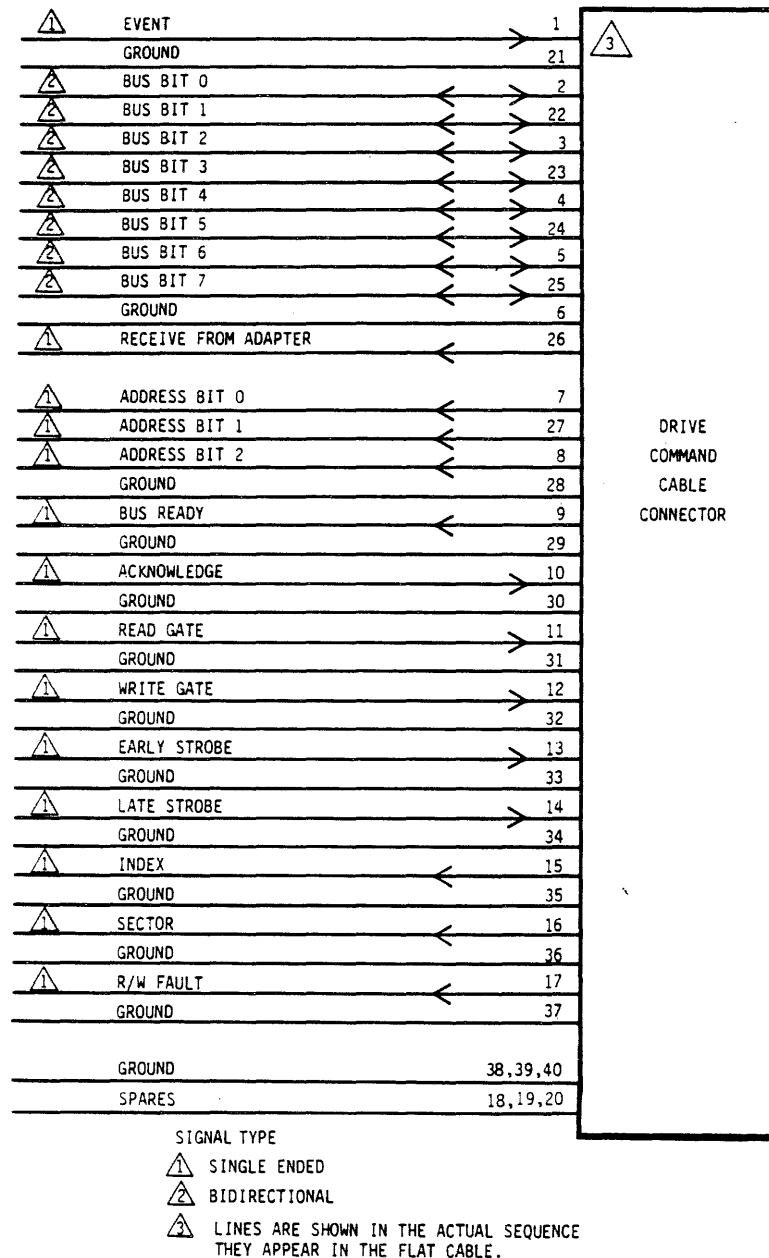


NOTES

- ⚠ ACTIVE LOW, SINGLE ENDED LINES
- ⚠ DIFFERENTIAL PAIR LINES
- ⚠ LINES ARE SHOWN IN THE ACTUAL SEQUENCE THEY APPEAR IN THE FLAT CABLE.

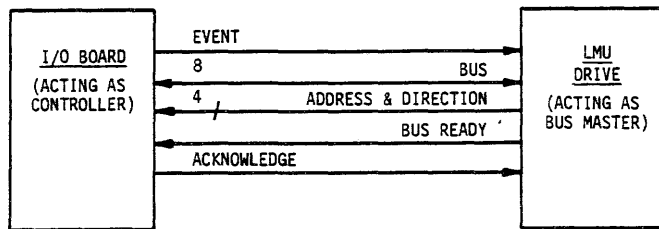
G260b

FIGURE 5-12. DATA CABLE CONNECTOR ASSIGNMENTS



G260a

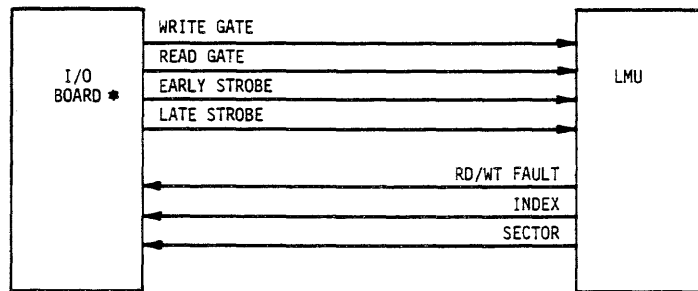
FIGURE 5-13. COMMAND CABLE PIN ASSIGNMENTS



EVENT - REQUESTS TRANSFER OF COMMANDS (OPERATIONS)
 BUS - EIGHT LINES TO TRANSFER INFORMATION (BOTH WAYS).
 ADDRESS - INDICATES WHAT IS TO BE TRANSFERRED.
 BUS READY - USED BY DRIVE TO INITIATE EACH TRANSFER.
 ACKNOWLEDGE - USED BY I/O ADAPTER BOARD TO ACKNOWLEDGE EACH TRANSFER.

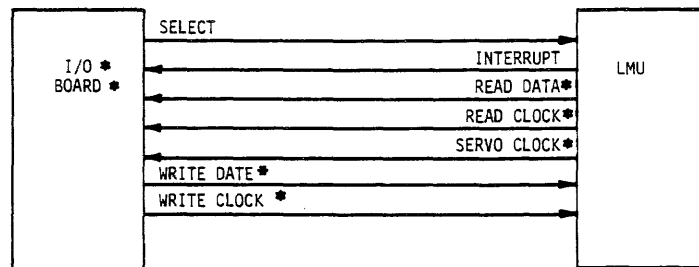
G147a

FIGURE 5-14. LMU INTERFACE BUS TRANSFER LINES (SINGLE-ENDED)



G146c

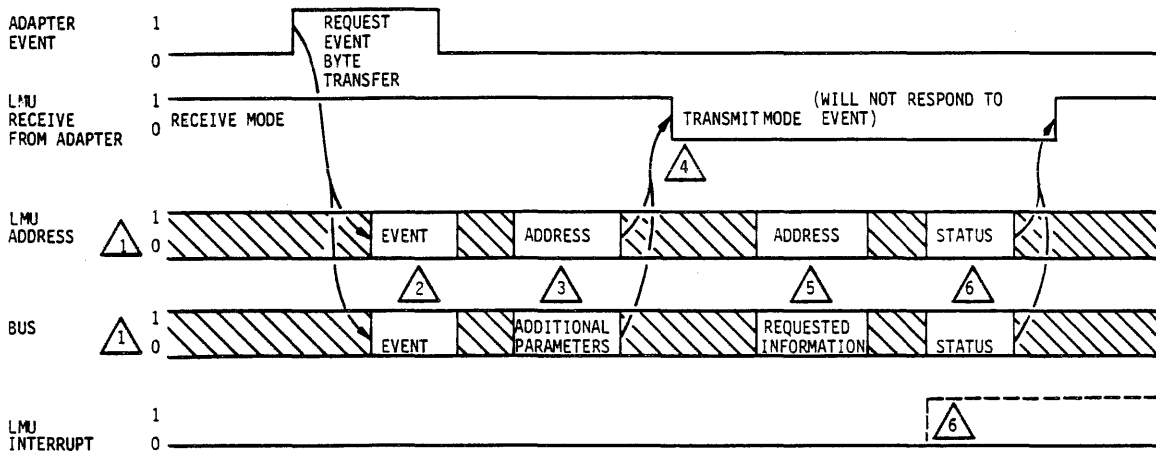
FIGURE 5-15. OTHER COMMAND CABLES LINES



G146d

* DENOTES BALANCED DIFFERENTIAL PAIR.
 (RESERVED AND SPARE LINES NOT SHOWN)

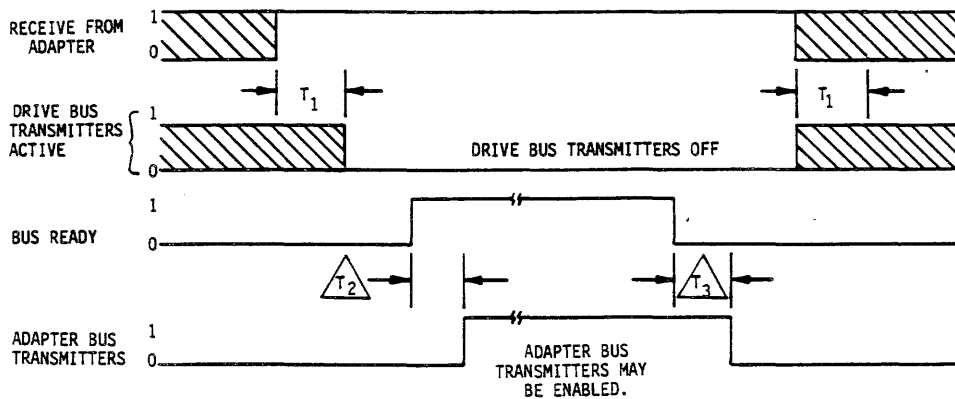
FIGURE 5-16. DATA ("D") CABLE LINES



- △1 ADDRESS AND BUS VALIDITY ARE DEFINED BY THE INTERLOCKED LMU BUS READY AND ADAPTER ACKNOWLEDGE SIGNALS.
- △2 LMU RESPONDS TO THE ADAPTER EVENT LINE BY READING THE EVENT BYTE TO DETERMINE THE FUNCTION(S) TO BE PERFORMED.
- △3 IF REQUIRED, THE LMU READS ADDITIONAL PARAMETERS FROM THE ADAPTER TO COMPLETE THE FUNCTION(S) DEFINED IN THE EVENT BYTE.
- △4 LMU DEACTIVATES RECEIVE FROM ADAPTER SIGNIFYING THAT ALL REQUIRED PARAMETERS HAVE BEEN REQUESTED. ADAPTER MAY DESELECT.
- △5 IF APPLICABLE (DEPENDENT ON COMMAND BITS ACTIVATED) LMU RESPONDS WITH REQUESTED INFORMATION (FOR EXAMPLE DEVICE ID).
- △6 IF APPLICABLE, AND NOT IN THE INTERRUPT MODE, LMU RESPONDS WITH COMPLETION STATUS OF THE COMMAND. IF APPLICABLE AND IN INTERRUPT MODE, NO STATUS TRANSFER WILL BE REQUESTED AND THE INTERRUPT LINE WILL BE ACTIVATED.

G263b

FIGURE 5-17. GENERALIZED MICRO UNIT INTERFACE OPERATION



$$T_1 \leq 200 \text{ ns}$$

$$\Delta T_2 \geq 0$$

$$\Delta T_3 \leq 1 \mu\text{s}$$

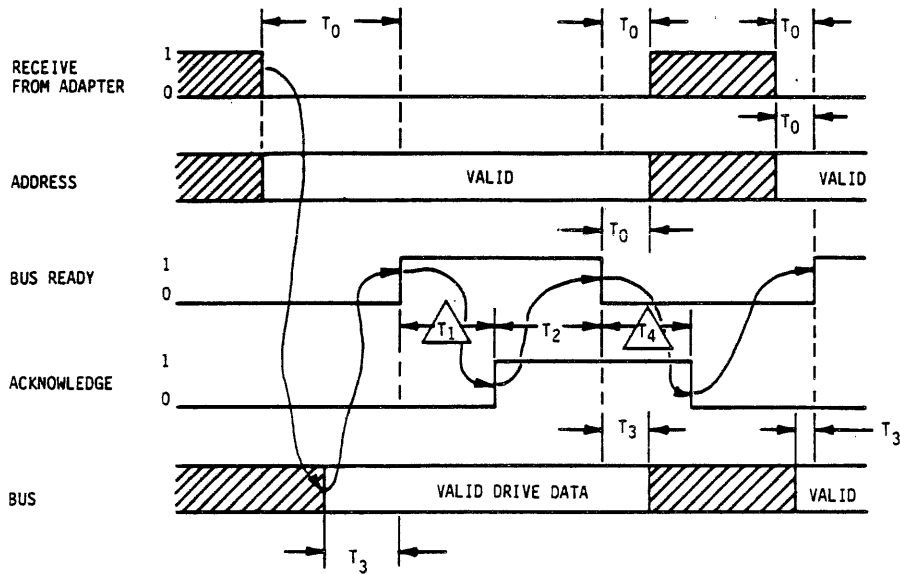
T_x - DRIVE CONTROLLED TIME

T_y - ADAPTER CONTROLLED TIME

"1" \Rightarrow 0.4 VOLTS MAX. AT INTERFACE WHICH IS ACTIVE STATE (TTL LOW).

G259a

FIGURE 5-18. BUS TRANSCEIVER CONTROL



- $T_0 \geq 400 \text{ ns}$ - THE ADDRESS IS VALID 400 ns BEFORE BUS READY BECOMES ACTIVE.
- $0 \leq \triangle T_1 \leq 500 \mu\text{s MAX}$ - THE ADAPTER MUST RESPOND TO BUS READY ACTIVATION WITHIN 500 ns.
- $0 \leq T_2 \leq 100 \mu\text{s}$
- $T_3 \geq 400 \text{ ns}$ - DRIVE DATA TO BUS READY SET UP AND HOLD TIME.
- $0 \leq \triangle T_4 \leq 100 \mu\text{s MAX}$

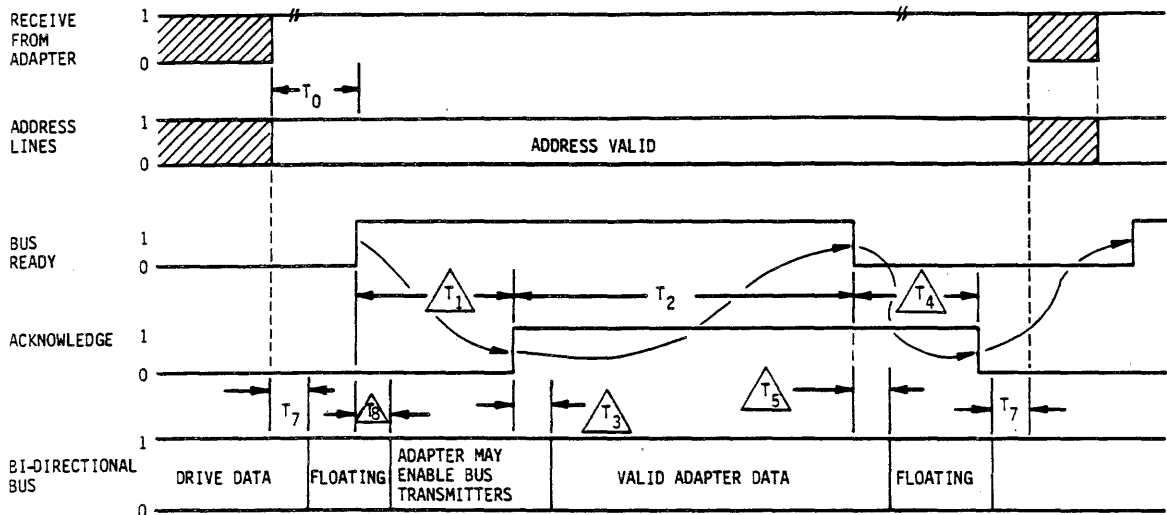
NOTE: "1" \Rightarrow 0.4 VOLTS MAX AT INTERFACE (TTL LOW)

$T_i \Rightarrow$ DRIVE CONTROLLED TIME WHERE $i = 0, 2$ and 3

$\triangle T_i \Rightarrow$ ADAPTER CONTROLLED TIME WHERE $i = 1$ and 4

G050a

FIGURE 5-19. SEND A BYTE TO THE ADAPTER TIMING



* $T_0 \geq 400 \text{ ns}$ ADDRESS SETUP TIME

$0 \leq T_1 \leq 500 \mu\text{s MAX}$

$0 \leq T_2 \leq 100 \mu\text{s MAX}$

$T_3 \leq 1 \mu\text{s MAX}$ ADAPTER DATA MUST BE VALID AT THE DRIVE CONNECTOR AFTER ACKNOWLEDGE

$0 \leq T_4 \leq 100 \mu\text{s MAX}$

$T_5 \leq 1 \mu\text{s MAX}$ THE ADAPTER MUST CEASE DRIVING THE BUS WITHIN $1 \mu\text{s}$ AFTER BUS-READY BECOMES INACTIVE

$T_7 \leq 200 \text{ ns MAX}$ THE DRIVE WILL CEASE DRIVING THE BUS A MAXIMUM OF 200 ns AFTER RECEIVE-FROM-ADAPTER BECOMES ACTIVE

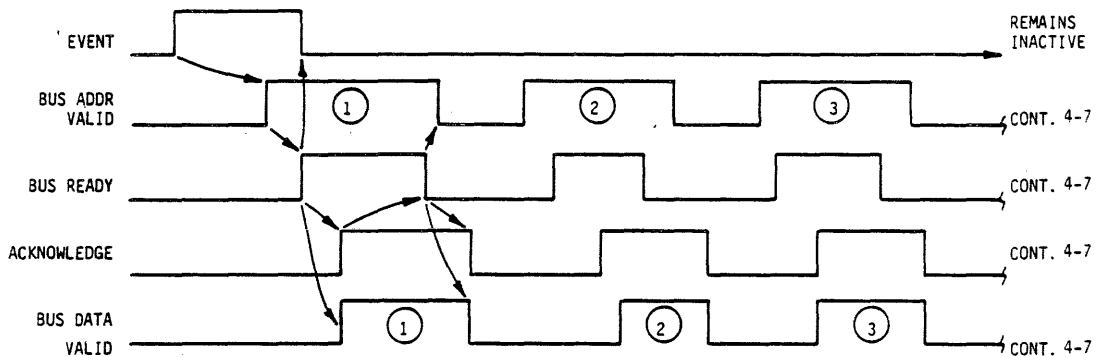
$T_8 \geq 0 \text{ MIN}$ THE ADAPTER MAY DRIVE THE BUS AFTER BUS-READY BECOMES ACTIVE

* ALL T_x TIMING CONTROLLED BY DRIVE.

* ALL T_y TIMING CONTROLLED BY ADAPTER.

G259b

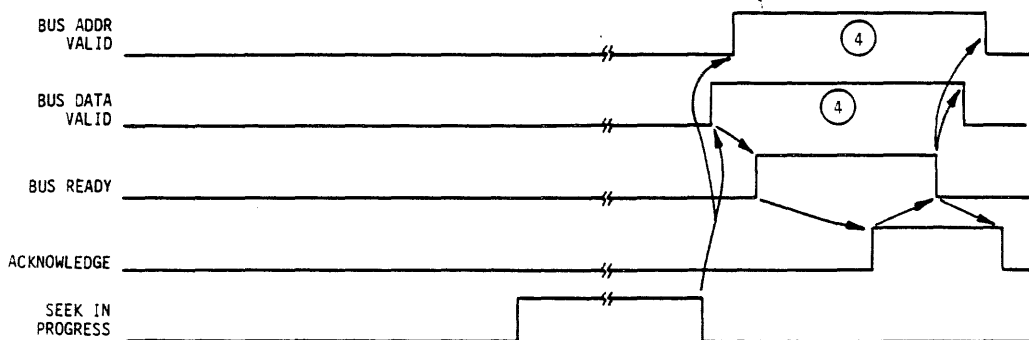
FIGURE 5-20. READ AN ADAPTER BYTE TIMING



- ① - DRIVE REQUESTS A LIST OF OPERATIONS TO BE PERFORMED USING BUS READY AND ADDRESS LINES. I/O ADAPTER BOARD ACKNOWLEDGES REQUEST AND SENDS DATA ACROSS THE BUS. THE DRIVE TAKES DATA THEN DROPS BUS READY.
- ② - DRIVE REQUESTS HIGH ORDER BITS OF CYLINDER ADDRESS. TIMING IDENTICAL TO ①. (IF USED)
- ③ - DRIVE REQUESTS LOW ORDER BITS OF CYLINDER ADDRESS. TIMING IDENTICAL TO ①. SEEK THEN STARTS.

G149a

FIGURE 5-21. TYPICAL BUS TRANSFERS FOR A SEEK (I/O ADAPTER BOARD-TO-DRIVE TRANSFERS)



- ④ - THE LMU SENDS STATUS WITH "ON CYLINDER" ACTIVE. STATUS IS PLACED ON THE BUS AND TRANSFERRED TO I/O BOARD USING ADDRESS AND BUS READY LINES. THE I/O BOARD TAKES THE DATA AND ACKNOWLEDGES THE TRANSFER.

FF010

FIGURE 5-22. TYPICAL BUS TRANSFERS FOR A SEEK (DRIVE-TO-I/O ADAPTER BOARD TRANSFERS)

The LMU also provides an alternate method of handling status returns via a dedicated bit within the Event Byte called the Interrupt Bit. If this bit is true, the drive will inform the adapter of a Status change by means of the Interrupt Request line in the data cable. This line will function independently of Unit Select and will allow the user a capability to perform overlapping operations in a multiple-LMU or interrupt-driven system.

A microcomputer within the LMU monitors all critical drive activity and will store conditions relative to this activity in its memory. As an aid to fault diagnosis, this information can be requested by the adapter and subsequently transferred across the interface. The interface also incorporates early and late data strobing capabilities to aid in read data recovery.

The following section contains a detailed description of the Event signal and a brief description of the other signal lines together with command/status information tables. For comprehensive details on all of the signal lines refer to "Product Specification - 9454 Lark Micro Unit".*

COMMAND CABLE SIGNAL DEFINITION

Interface signals for the command and data cables depicted in block diagram Figures 5-12 and 5-13 are described in the following paragraphs and in Table 5-6.

Event

The Event signal indicates the drive must execute a command. The drive will request the adapter's Event Byte to determine the operation to be performed. Response to the Event signal will be delayed if the LMU is currently performing the operation(s) specified by a previous Event (that is, the drive will honor a new Event after completion of a previous Event) or if the drive is responding to a status change. The drive will inhibit writing of the media when Event is active. Writing is inhibited by drive electronics as soon as the leading edge of the Event signal is detected. The adapter must not activate Event while a data read or write operation is in progress. Writing will be inhibited until Event is deactivated. Depending upon the operation, writing may also be inhibited until the operation specified by Event is completed. Attempting to write during these times will generate a fault condition.

The Micro Unit Interface has been designed to require a minimal utilization of the Event signal. Anytime the drive is selected and the status of the drive changes, the drive automatically requests to send the updated Status Byte to the adapter. Thus, the adapter need only use the Event function to specify operations to be performed and need not utilize Event to Request status. The LMU can, therefore, dedicate time to performing internal tests (such as RPM tests, etc.) without being continuously interrupted by status transfer commands from the adapter.

*Consult local CDC Sales Office for applicable part number.

If the Interrupt bit is active when the Event Byte is transferred or if the drive is deselected, the LMU will respond to a status change by raising the Interrupt Request line. The adapter may then respond by selecting the drive (if deselected), initiating an Event request, and sending an Event Byte requesting the updated status.

To ensure the drive has detected that a command is to be executed, Event should remain activated until the Bus Ready signal requesting the Event Byte (Address 111 with Receive From Adapter active) is received from the LMU. The Event line must be deactivated after the adapter acknowledges the Event Byte transfer to the LMU to ensure that the drive will not execute a redundant command.

TABLE 5-4. BUS DEFINITION

| RECEIVE FROM ADAPTER | | ADDRESS (2 ² , 2 ¹ , 2 ⁰) | BUS BIT | | | | | | | | |
|---------------------------------|---|-------------------------------------------------------------|---------|--------------------------------------------------------------------------------|-------------------|--------------------|-------------------|-------------------|-------------------|----------------------|--------------------------|
| | | | (MSB) ← | 7 | 6 | 5 | 4 | 3 | 2 | 1 | (LSB) |
| BYTES RECEIVED FROM THE ADAPTER | 1 | EVENT (111) | 7 | READ ESCAPE REG | SEEK | HEAD SELECT | RTZ | SPINDLE POWER ON | FAULT RESET | INTERRUPT MODE | SPINDLE POWER OFF |
| | 1 | ESCAPE (000) | 0 | ⓐ | PDQ | SERVO OFFSET MINUS | SERVO OFFSET PLUS | LOOP LOW CYL REG | SEND DEV ID | SEND MC STATUS CODE | SEND DETAILED STATUS |
| | 1 | LOW CYL (110) | 6 | 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ |
| | 1 | HIGH CYL (100) ⓐ | 4 | 2 ¹⁵ | 2 ¹⁴ | 2 ¹³ | 2 ¹² | 2 ¹¹ | 2 ¹⁰ | 2 ⁹ | 2 ⁸ |
| | 1 | HEAD (101) | 5 | ⓑ RESERVED FOR HEAD EXPANSION | | | | | | 2 ¹ | 2 ⁰ |
| BYTES SENT TO THE ADAPTER | 0 | STATUS (111) | 7 | READY TO LOAD | WRITE PROTECTED | ON CYLINDER | UNIT READY | ATTN ⓑ | SEEK ERROR | ⓑ | FAULT |
| | 0 | MC STATUS CODE (001) | 1 | 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ |
| | 0 | DEV ID (000) | 0 | ID ₃ ⓐ | ID ₂ ⓐ | ID ₁ ⓐ | ID ₀ ⓐ | CB ₃ ⓑ | CB ₂ ⓑ | CB ₁ ⓑ | CB ₀ ⓑ |
| | 0 | DETAILED STATUS (010) | 2 | STOP SWITCH | SPINDLE STOPPED | RPM OK | ⓑ | ⓑ | ⓑ | FIXED PROTECT SWITCH | REMOVABLE PROTECT SWITCH |
| | 0 | AUXILIARY (011) WHEN USED: | 3 | CONTENTS OF ADAPTER'S LOW CYLINDER ADDRESS (SENT BY LOOP LOW CYLINDER ADDRESS) | | | | | | | |

| ⓐ | ⓑ | DEVICE ID | CONFIGURATION CODE | EXPLANATION |
|---|---|-----------|--------------------|-------------------------------------------|
| | | 0001 | 0000 | LARK 16 MICRO UNIT |
| | | 0010 | 0000 | LARK 50 MICRO UNIT WITH LARK 50 CARTRIDGE |
| | | 0010 | 0010 | LARK 50 MICRO UNIT WITH LARK 16 CARTRIDGE |

ⓑ RESERVED - MUST BE ZERO

ⓐ ONLY REQUIRED FOR LARK 50 MICRO UNIT, THE LARK 16 MICRO UNIT WILL NOT REQUEST THIS BYTE

ⓑ ONLY DEFINED FOR LARK 50 MICRO UNIT, WILL ALWAYS BE ZERO FOR THE LARK 16 MICRO UNIT.



TABLE 5-6. INTERFACE SIGNAL DEFINITIONS (COMMAND CABLE)

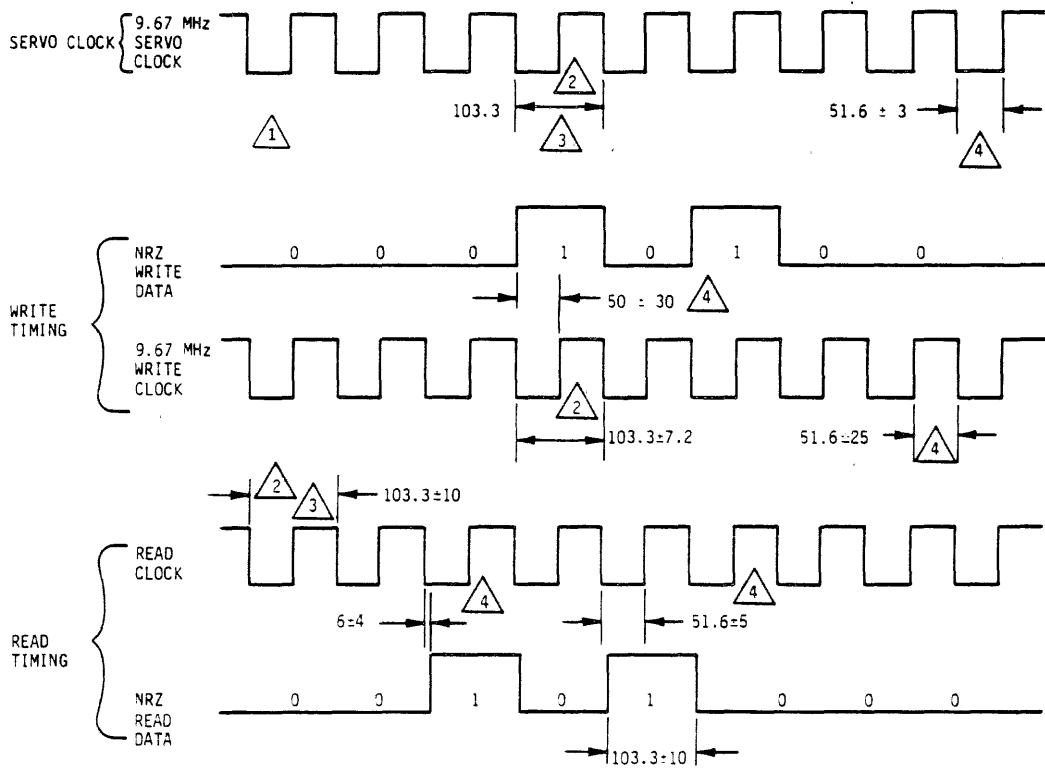
| <u>PIN NO.</u> | <u>SIGNAL NAME</u> | <u>I/O*</u> | <u>SIGNAL FUNCTION</u> |
|----------------|----------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | EVENT | IN | Signal indicating to drive it must execute a command (details given in text). |
| 2 | BUS BIT 0 | | |
| 22 | BUS BIT 1 | | |
| 3 | BUS BIT 2 | | |
| 23 | BUS BIT 3 | | |
| 4 | BUS BIT 4 | | |
| 24 | BUS BIT 5 | | |
| 5 | BUS BIT 6 | | |
| 25 | BUS BIT 7 | | |
| 26 | RECEIVE FROM ADAPTER | OUT | Signifies direction of data transfer on BUS lines. 1 = IN; 0 = OUT. Also 1 = drive can be deselected. |
| 7 | ADDRESS BIT 0 | | |
| 27 | ADDRESS BIT 1 | OUT | Specifies up to eight different interpretations of information on the BUS lines. See Table 5-4. |
| 8 | ADDRESS BIT 2 | | |
| 9 | BUS READY | OUT | Handshaking line that initiates all BUS transfer requests from drive. |
| 10 | ACKNOWLEDGE | IN | Handshaking line from adapter indicating acceptance of a BUS byte, or presence of valid BUS byte to drive. |
| 11 | READ GATE | IN | Enables serial NRZ Read Data on radial Read Data lines. |
| 12 | WRITE GATE | IN | Enables drive to write serial NRZ write data defined by data cable WRITE DATA and WRITE CLOCK signals. |
| 13 | EARLY STROBE | IN | TRUE = strobe data earlier than usual; FALSE = strobe data at normal time. |
| 14 | LATE STROBE | IN | TRUE = strobe data later than usual; FALSE = strobe data at normal time. |
| 15 | INDEX | OUT | Pulse that occurs once per revolution of disk. Indicates beginning of sector 0. Valid only when ON CYLINDER is TRUE. |
| 16 | SECTOR | OUT | Pulse derived from embedded servo. Divides tracks into N equal length sectors when combined with INDEX in adapter (N=32 or 64 depending on LMU assy. no.). |
| 17 | R/W FAULT | OUT | Real time indicator of a read or write fault. The only active high line in the interface. |

*Input to or output from LMU.

TABLE 5-6. INTERFACE SIGNAL DEFINITIONS (DATA CABLE)

| PIN NO. | SIGNAL NAME | I/O | SIGNAL FUNCTION |
|----------|--------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 02 14 | SERVO CLOCK - SERVO CLOCK + | OUT | Continuously transmitted, phase-locked 9.677 MHz (nominal) clock used by adapter to generate WRITE CLOCK (below). |
| 03 16 | READ DATA - READ DATA + | OUT | Transmits recovered NRZ data to adapter. 9-bit delay from detection by head to appearance at interface connector. |
| 05 17 | READ CLOCK - READ CLOCK + | OUT | Clock defining beginning of a data cell. Synchronous with detected data, transmitted continuously, but not in phase with data unless reading. |
| 06 19 | WRITE CLOCK - WRITE CLOCK + | IN | Clock from adapter must be synchronous with NRZ data. Adapter should create WRITE CLOCK from SERVO CLOCK above. |
| 08 20 | WRITE DATA - WRITE DATA + | IN | NRZ data from adapter to be recorded on the LMU disks. 8-bit delay from I/O connector to write head due to conversion of NRZ to coded data. |
| 10 | SELECT | IN | Enables or disables command cable interface for daisy chained operation. |
| 11 | INTERRUPT REQUEST | IN | Signifies to the adapter that a status change has occurred within the drive when the drive is deselected. When selected, adapter may respond to this line and request updated status at any time. |

| | |
|-------------------------------------------------------------------------------------|------------------------------------------------------|
|  | Differential pair lines. See Figure 5-22 for timing. |
|  | Active low, single ended lines. |



NOTES

- 1 ALL TIMES IN ns MEASURED AT I/O CONNECTOR OF THE DRIVE.
- 2 SIMILAR PERIOD SYMMETRY SHALL BE ± 2 ns BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.
- 3 EXCEPT DURING A HEAD CHANGE OR PLO SYNCHRONIZATION THE CLOCK VARIANCES FOR SPINDLE SPEED AND CIRCUIT TOLERANCES SHALL NOT VARY MORE THAN -5.5% TO +4%.
- 4 PHASE RELATIONSHIP BETWEEN SERVO CLOCK AND NRZ WRITE DATA OR WRITE CLOCK IS NOT DEFINED. TIMING APPLICABLE DURING READING OR WRITING.

2187a

FIGURE 5-23. NRZ DATA AND CLOCK TIMING

6.1 INTRODUCTION

This section contains the instructions required to maintain the LARK Micro Unit (LMU). The information presented is provided in the form of corrective maintenance. There is no preventive maintenance to be performed. All maintenance should be performed by qualified and trained service personnel.

Before performing any drive maintenance, install a scratch cartridge or equivalent in the drive and secure the carriage to prevent damage. The drive must be disconnected from the subsystem and moved to a bench test area for trouble shooting. The maintenance procedures provided in this section assume that the proper test equipment is available to troubleshoot and replace selected malfunctioning parts. In reference to the LMU, parts replacement is accomplished **OUTSIDE THE SEALED AREA OF THE DRIVE, ONLY. ENCROACHMENT OF THE SEALED AREA VOIDS THE UNIT WARRANTY.**

6.2 SAFETY AND SPECIAL MAINTENANCE PRECAUTIONS

Before proceeding with any maintenance, maintenance personnel should become familiar with the precautions given in paragraphs 6.2.1 and 6.2.2.

6.2.1 SAFETY PRECAUTIONS

- Use care when power is applied to the LMU. AC voltages are present on the AC distribution PWA at the back of the LMU; the cover should not be removed unless absolutely necessary.

6.2.2 SPECIAL MAINTENANCE PRECAUTIONS

CAUTION

The LMU shall contain a cartridge at all times whether operating or not. This is necessary to insure proper sealing of the fixed disk area from environmental contaminants. **UNDER NO CONDITIONS SHALL THE COVER TO THE SEALED AREA BE REMOVED FOR ANY MAINTENANCE PROCEDURE.** Maintenance in the sealed area can be accomplished only at facilities especially set up for that purpose. **ENCROACHMENT OF THE SEALED AREA OF THE UNIT VOIDS THE WARRANTY.**

In addition to the above special cautions, the following precautions should be taken:

- Keep disk cartridge access door closed unless it must be open for insertion or removal of cartridge. Maintenance attempts should not be made through the disk cartridge access door.
- Keep all watches, disk cartridges, meters and other test equipment at least two feet away from the voice coil magnet.
- Use a scratch cartridge to perform maintenance procedures rather than a data cartridge; otherwise customer data may be destroyed.

WARNING

The circuit assemblies contained in this equipment can be degraded or destroyed by ELECTRO-STATIC DISCHARGE (ESD).

Static electrical charges can accumulate quickly on personnel, clothing, and synthetic materials. When brought in close proximity to, or in contact with delicate components, ELECTRO-STATIC DISCHARGE OR FIELDS can cause damage to these parts. This damage may result in degraded reliability or immediate failure of the affected component or assembly.

- Avoid overtightening hardware (screws, nuts, etc.) when replacing assemblies and components. All screws and nuts are of the low carbon variety.
- Do not connect or disconnect cables without first removing all power from the drive.

6.3 MAINTENANCE TOOLS

Table 6-1 lists special tools required to maintain that part of the LMU external to the sealed area.

TABLE 6-1. SPECIAL TOOLS REQUIRED

| <u>PART NUMBER</u> | <u>DESCRIPTION</u> |
|--------------------|---------------------------------------------------------------------------|
| 77653781 | Belt Tensioning Tool Torque Wrench, UTICA Model DA-130, or equivalent. |
| LATER | Test or Scratch Cartridge |

6.4 MAINTENANCE PROCEDURES

6.4.1 INDEX AND SCHEDULE

The LMU is designed to require no preventative maintenance at the user site. Unless requested by the user of the drive it is expected that only corrective maintenance will be performed. No special testing is required to confirm repairs other than the test that is used to isolate the fault.

6.4.2 REMOVAL AND REPLACEMENT PROCEDURE LIST

Table 6-2 lists the Removal and Replacement procedures provided in this section. The procedures are for the removal and replacement of recommended spare assemblies and components for the LMU.

TABLE 6-2. LIST OF REMOVAL AND REPLACEMENT PROCEDURES

| <u>PARAGRAPH NUMBER</u> | <u>REMOVAL AND REPLACEMENT PROCEDURE</u> |
|-------------------------|-----------------------------------------------------|
| 6.4.2.1 | LMU Printed Circuit Boards |
| 6.4.2.2 | Static Eliminator Brush |
| 6.4.2.3 | Spin Motor Sensor |
| 6.4.2.4 | Spin Speed Pulley Flange |
| 6.4.2.5 | Spindle Drive Belt |
| 6.4.2.6 | Spindle Motor Pulley |
| 6.4.2.7 | Spindle Drive Motor |
| 6.4.2.8 | Belt Guard |
| 6.4.2.9 | Blower |
| 6.4.2.10 | Front Panel Switch and Lens Removal and Replacement |

6.4.2.1 LMU PRINTED CIRCUIT BOARD REMOVAL AND REPLACEMENT

Removal power from drive before performing any of the following procedures.

a. Base PWA (Refer to Figure 6-1)

1. Position Drive on its left side (as viewed from front). Use spacers between drive and bench so bottom plate and covers can be removed.
2. Remove eight (8) screws that secure bottom plate to casting and remove bottom plate.
3. Remove six (6) mounting screws that secure Base PWA to casting.
4. Pivot PWA 90° clockwise to lay flat along side drive.
5. Disconnect all cables and remove PWA.

Replacement of Base PWA is reverse of removal.

b. Read Signal Processor (RSP) PWA (Refer to Figure 6-1).

1. Remove Base PWA in accordance with procedure a. except do not disconnect cables from PWA.
2. Disconnect all cables from RSP PWA.
3. Remove four (4) screws that secure RSP PWA to casting and remove PWA.

Replacement of RSP PWA is reverse of removal.

c. R/W Preamp PWA (Refer to Figure 6-2).

1. Position drive on its bottom.
2. Remove two (2) screws that secure cover to casting (two holes are provided to accommodate a screwdriver).
3. Disconnect all cables.
4. Remove three (3) screws that secure R/W Preamp PWA to casting and remove PWA.

Replacement of R/W Preamp PWA is reverse of removal.

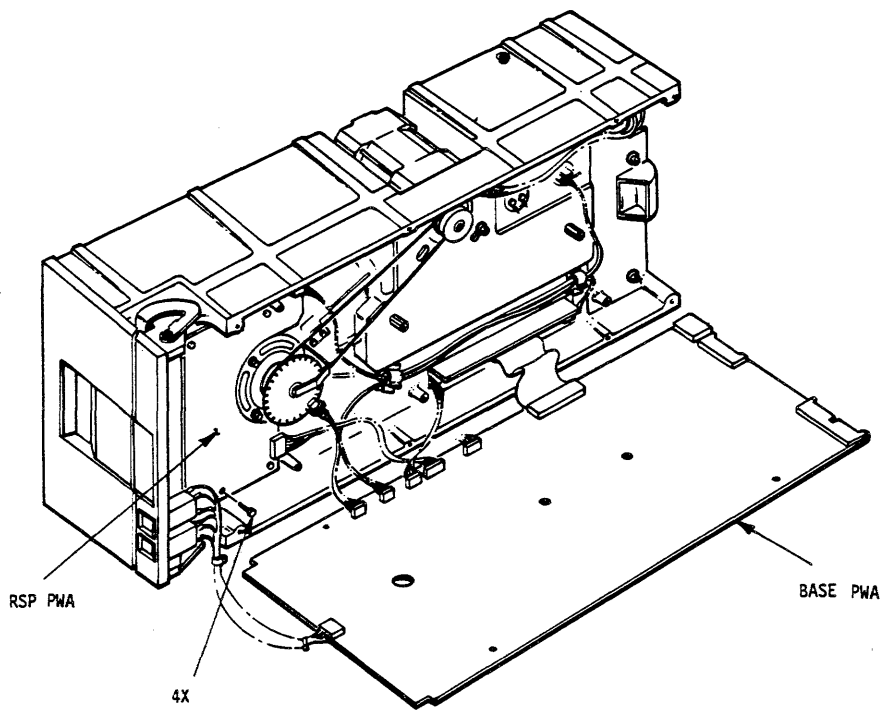
d. AC Distribution PWA (Refer to Figure 6-2).

1. Position drive on its bottom.
2. Remove two screws that secure rear cover to casting and remove rear cover.
3. Disconnect all cables.
4. Remove two (2) screws that secure AC Distribution PWA to casting and remove PWA.
5. Retain insulating material and mounting brackets for installation with new PWA.

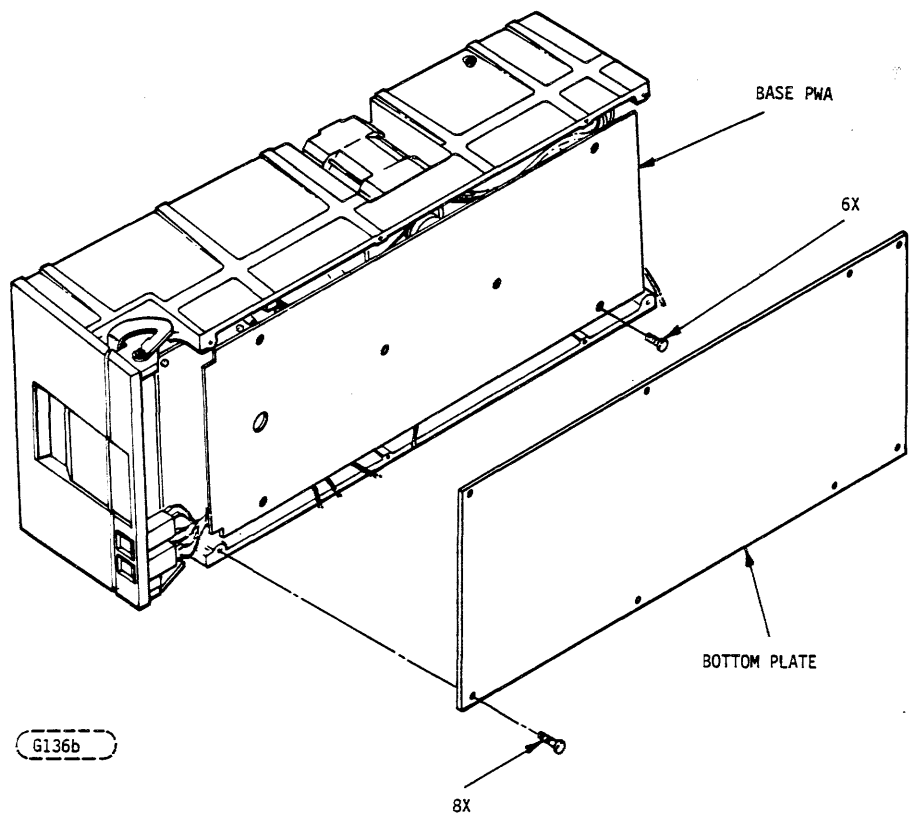
Replacement of AC Distribution PWA is reverse of removal.

e. Status Display Option (Refer to Figure 6-3).

1. The Lark Micro Unit may have the Status Display option or the customer may wish to install the option into a LMU that does not have it. These installation instructions are for installing the option into a LMU that does not have the option, however, they can be used for removal and replacement of parts.
2. Remove panel and return to stock or discard.
3. Remove panel mount.
4. Remove jumper connector and return to stock or discard.
5. Connect plug DPI to PWA.
6. Mount PWA to panel mount as shown.
7. Remount panel mount.
8. Mount panel.



G136a



G136b

FIGURE 6-1. BASE PWA AND RSP PWA REMOVAL

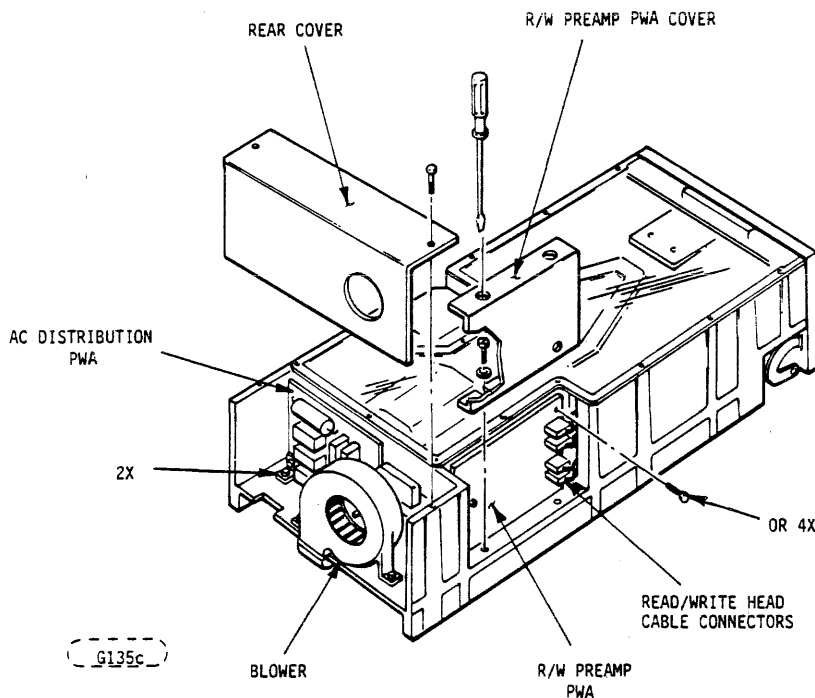


FIGURE 6-2. R/W PREAMP PWA AND AC DISTRIBUTION PWA REMOVAL

6.4.2.2 STATIC ELIMINATOR BRUSH REMOVAL AND REPLACEMENT

1. Remove Base PWA in accordance with procedure a, paragraph 6.4.2.1 except do not disconnect cables.
2. Remove two (2) screws that secure Static Eliminator Brush to casting (refer to Figure 6-4).

Replacement of Static Eliminator Brush is reverse of removal.

6.4.2.3 SPIN SPEED SENSOR REMOVAL AND REPLACEMENT

1. Remove Base PWA in accordance with procedure a, paragraph 6.4.2.1 except do not disconnect cables.
2. Remove one of two screws securing spin speed sensor bracket to casting (refer to Figure 6-4).
3. Loosen the other mounting screw and pivot bracket until screw that secures Spin Speed Sensor to bracket is accessible.
4. Remove screw securing Spin Speed Sensor to bracket and remove sensor.
5. Disconnect cable from Base PWA.

Replacement of Spin Speed Sensor is reverse of removal.

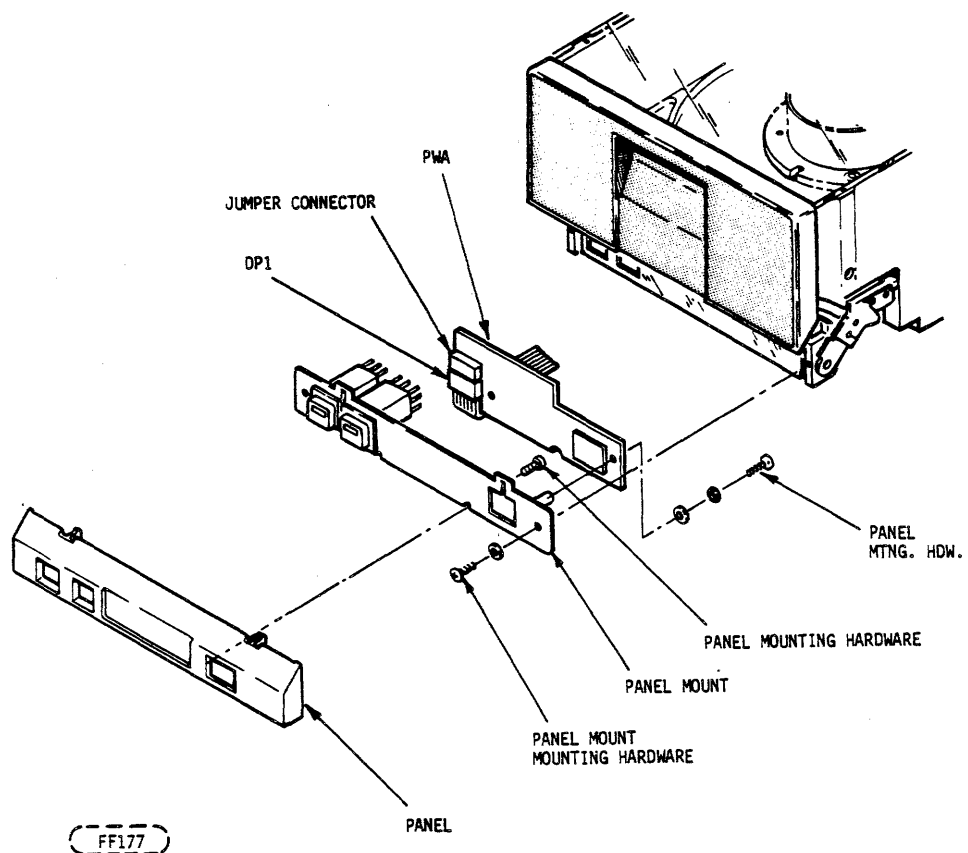


FIGURE 6-3. STATUS DISPLAY OPTION



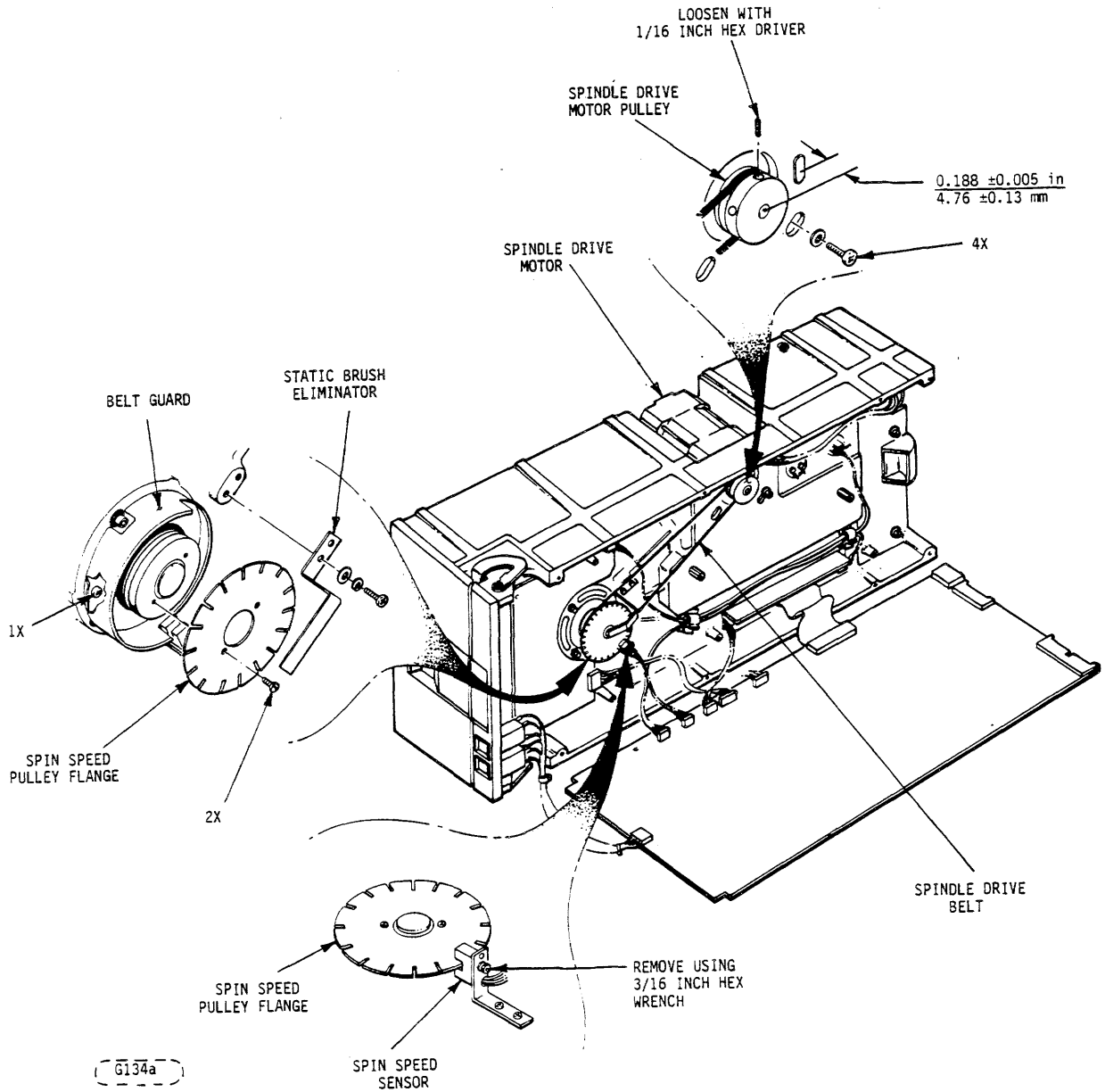


FIGURE 6-4. SUBASSEMBLY REMOVAL AND ADJUSTMENT

6.4.2.4 SPIN SPEED PULLEY FLANGE REMOVAL AND REPLACEMENT

1. Remove Base PWA in accordance with procedure a, paragraph 6.4.2.1 except do not disconnect cables.
2. Remove Static Eliminator Brush in accordance with paragraph 6.4.2.2.
3. Pivot Spin Speed Sensor in accordance with paragraph 6.4.2.3.
4. Remove two (2) screws that secure Spin Speed Pulley Flange to spindle pulley (refer to Figure 6-4).

Replacement of Spin Speed Pulley Flange is reverse of removal.

6.4.2.5 SPINDLE DRIVE BELT REMOVAL AND REPLACEMENT

1. Remove Spin Speed Pulley Flange in accordance with paragraph 6.4.2.4.
2. Loosen four (4) screws that hold Spindle Drive Motor in position (refer to Figure 6-4).
3. Slide motor until belt is loose and remove belt.

Replacement of Spindle Drive Belt.

1. Place the belt around the spindle and motor pulleys.
2. Make sure four motor mounting screws are loose enough for motor to slide easily.
3. Slide motor away from spindle to take up slack in the belt, and at the same time, guide belt into the V-grooves of the pulleys.
4. Place belt tensioning tool between the two pulleys such that the stepped end of the tool engages the groove of the spindle pulley, and the opposite end engages the groove of the motor pulley (see Figure 6-5).
5. Place a torque wrench (see paragraph 6.3) on the 3/8" drive of the tool and apply torque as specified below. Move the motor about its mounting screws to help overcome the friction, then, while holding the torque steady, tighten the motor mounting screws to 5 in. lb. Remove the tool.

60 Hz: Apply 5.5 inch - pounds

50 Hz: New Belts - Apply 10.5 inch-pounds.

Used Belts (200 or more hours) - Apply
7.5 inch-pounds.

NOTE

If any residue is noted, the parts and area around the spindle pulley and drive pulley should be cleaned with alcohol on cue tip.

6. Install Spin Speed Pulley Flange in accordance with paragraph 6.4.2.4.

6.4.2.6 SPINDLE MOTOR PULLEY REMOVAL AND REPLACEMENT

1. Remove Base PWA in accordance with procedure a, paragraph 6.4.2.1 except do not disconnect cables.
2. Loosen four (4) screws that hold Spindle Drive Motor in position (refer to Figure 6-4).
3. Slide motor until belt is loose and remove belt.
4. Using 1/16 inch hex driver (or Allen wrench) loosen set screw in pulley and remove pulley.

Replacement of Spindle Motor Pulley

1. Install new pulley on motor shaft and adjust position of pulley in accordance with Figure 6-4.
2. Install belt and adjust motor position to obtain belt tension as described in 6.4.2.5 and completely tighten four (4) Spindle Drive Motor mounting screws.
3. Install Base PWA in accordance with procedure a, paragraph 6.4.2.1.

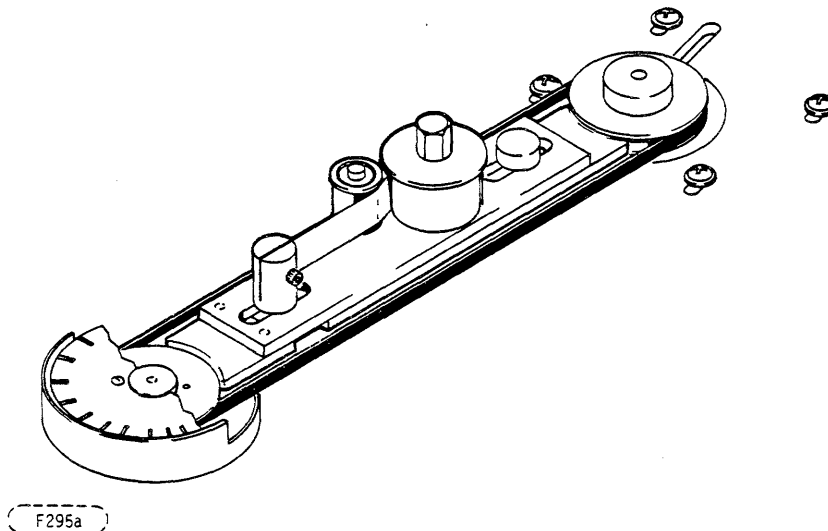


FIGURE 6-5. BELT TENSION GAGE

6.4.2.7 SPINDLE DRIVE MOTOR REMOVAL AND REPLACEMENT

1. Position drive on its bottom.
2. Remove two (2) screws that secure rear cover to casting and remove rear cover (refer to Figure 6-4).
3. Disconnect Spindle Drive Motor cable from J3.

4. Remove Base PWA in accordance with procedure a, paragraph 6.4.2.1 except do not disconnect cables.
5. Remove cable clamps securing cable to casting.
6. Remove four (4) screws that hold Spindle Drive Motor in position (refer to Figure 6-4).
7. Remove belt from motor pulley and remove motor.
8. Using 1/16 inch hex driver (or Allen wrench) loosen set screw in pulley and remove pulley.

Replacement of Spindle Drive Motor

1. Install new Spindle Drive Motor with previously used four (4) mounting screws. Leave screws slightly loose until belt tension adjustment is complete.
2. Install pulley and belt in accordance with replacement procedure, paragraph 6.4.2.5 and 6.4.2.6.
3. To complete replacement of Spindle Drive Motor, reverse removal procedure starting with Step 5, above.

6.4.2.8 BELT GUARD REMOVAL AND REPLACEMENT

1. Remove Base PWA in accordance with procedure a, paragraph 6.4.2.1.
2. Remove Spin Speed Pulley Flange in accordance with paragraph 6.4.2.4.
3. Loosen four (4) screws that hold Spindle Drive Motor in position and remove belt (refer to Figure 6-4).
4. Remove one (1) screw that secures plastic belt guard.

Replacement of Belt Guard is reverse of removal except for belt installation (Step 3): Install belt and adjust motor position to obtain tension as described in 6.4.2.5 and completely tighten four (4) Spindle Drive Motor mounting screws to 5 in. lb.

6.4.2.9 BLOWER ASSEMBLY REMOVAL AND REPLACEMENT

1. Position drive on its bottom.
2. Remove two (2) screws that secure rear cover to casting and remove rear cover (refer to Figure 6-2).
3. Disconnect motor cable from connector J2 on AC Distribution PWA.
4. Remove two (2) screws (with nuts) securing blower assembly to casting and remove blower.

Replacement of Blower Assembly is reverse of removal.

6.4.2.10 FRONT PANEL SWITCH AND LENS REMOVAL AND REPLACEMENT

1. Position drive on its left side (as viewed from front). Use spacers between drive and bench so lower part of front panel can be removed.
2. Using 3/16 in. nut driver, remove two (2) screws that secure lower part of front panel to sub-panel (refer to Figure 6-6) and remove lower part of front panel.
3. If lens is to be replaced, pull lens off pushbutton switch. Indentations are provided at top and bottom of lens to accommodate finger nail or suitable instrument during removal.
4. Disconnect wire fast-ons on rear of both switches.
5. Remove two (2) screws that secure sub-panel to casting and remove sub-panel (switches will pass through holes in deflector plate).
6. To remove switch, simultaneously compress springs (on each side of switch) and push switch out through front of sub-panel.

Replacement of Front Panel Switch is reverse of removal.

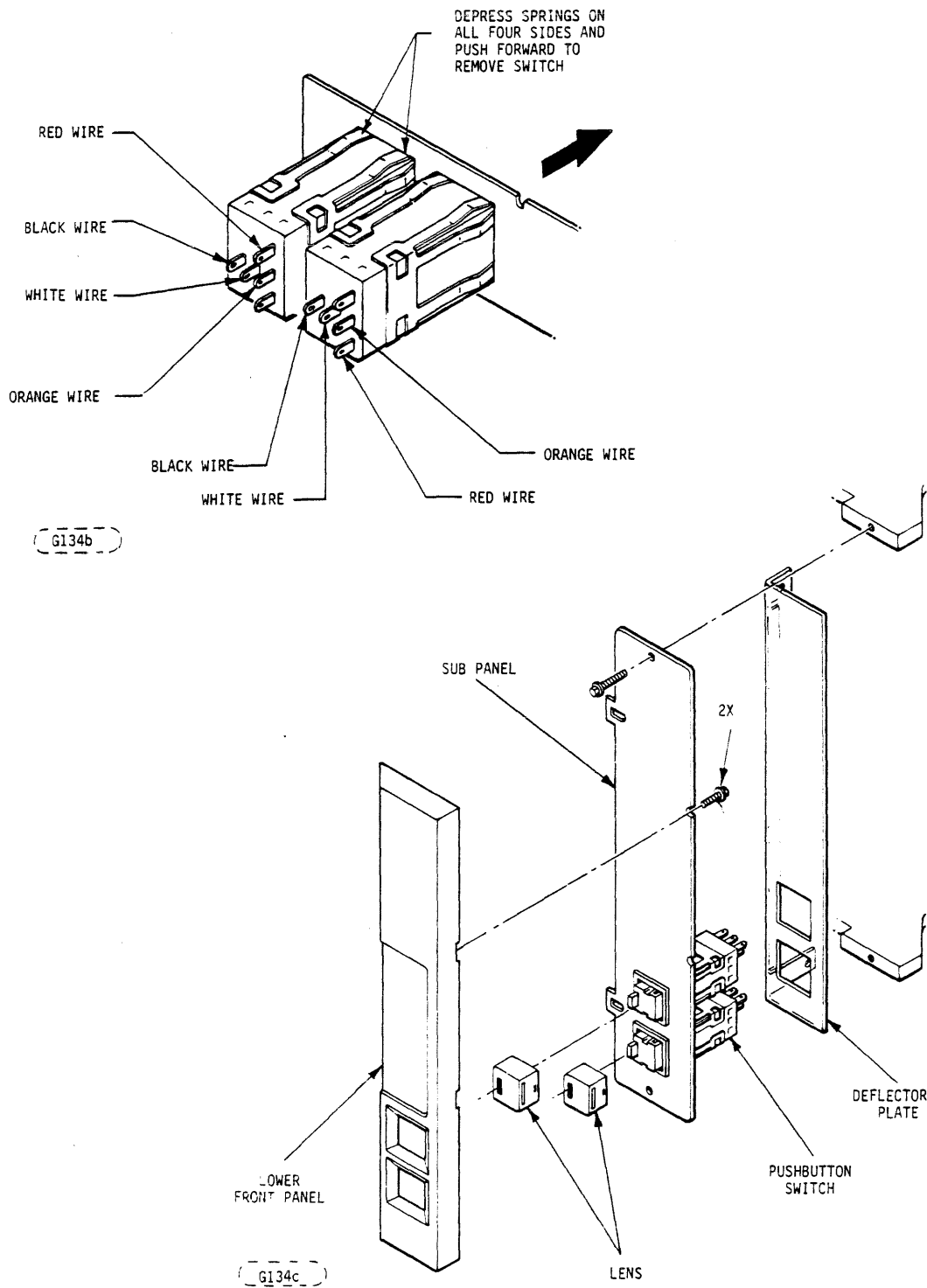


FIGURE 6-6. FRONT PANEL SWITCH REMOVAL

7.1 INTRODUCTION

This section provides the information necessary to order the recommended replaceable parts for the Lark Micro Unit (LMU).

7.2 ORDERING PARTS

When ordering replacement parts for the LMU, include the equipment identification number to insure positive identification of parts.

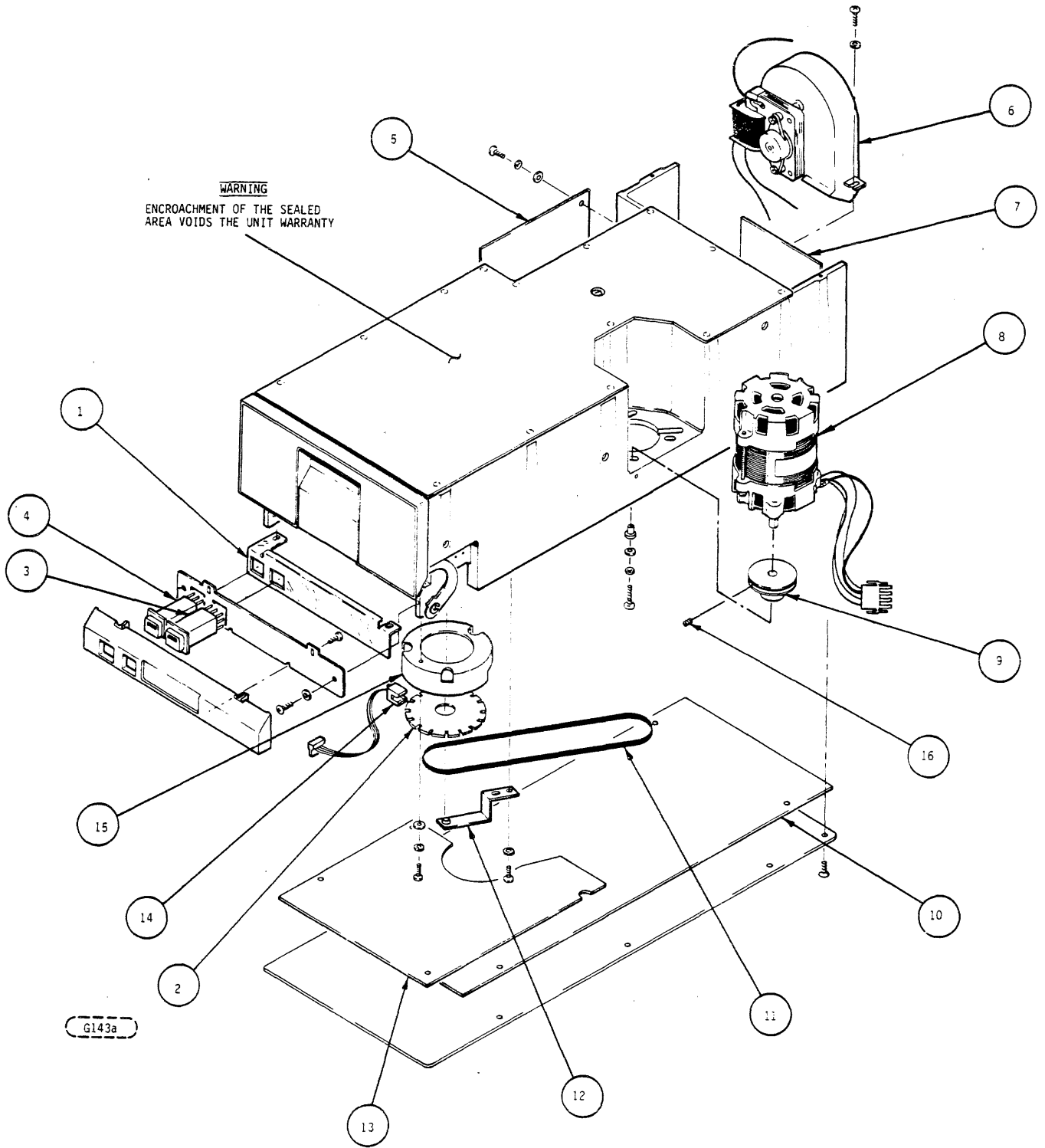


FIGURE 7-1. LARK MICRO UNIT ASSEMBLY (SHEET 1 OF 2)

| <u>ITEM</u> | <u>IDENT. NO.</u> | <u>DESCRIPTION</u> |
|-------------|-------------------|--------------------------------------|
| 1 | 77624886 | Deflector |
| 2 | 77633991 | Flange Pulley |
| 3 | 94394024 | Pushbutton Switch |
| 4 | 94394025 | Pushbutton Switch |
| 5 | * | R/W Preamp PWA |
| 6 | 77622885 | Blower and Connector ASM, 60 Hz |
| 6 | 77622886 | Blower and Connector ASM, 50 Hz |
| 7 | * | AC Distribution PWA |
| 8 | 77638950 | Drive Motor and Connector ASM, 60 Hz |
| 8 | 77638951 | Drive Motor and Connector ASM, 50 Hz |
| 9 | 77633987 | Motor Pulley, 60 Hz |
| 9 | 77633988 | Motor Pulley, 50 Hz |
| 10 | * | Base PWA |
| 11 | 77619094 | Vee Belt, 60 Hz |
| 11 | 77619097 | Vee Belt, 50 Hz |
| 12 | 77700260 | Ground Spring |
| 13 | * | RSP PWA |
| 14 | 77622862 | Speed Sensor and Connector |
| 15 | 77638990 | Belt Guard |
| 16 | 77670243 | Set Screw |

| <u>LANIER</u> | | <u>CDC</u> |
|--------------------|----------------------------------|--------------------|
| <u>PART NUMBER</u> | <u>DESCRIPTION</u> | <u>PART NUMBER</u> |
| E-009-019 | Belt, Vee, 60 Hz | 77619094 |
| E-009-019A | Belt, Vee, 50 Hz | 77619097 |
| E-040-073 | Motor and Connector Assy, 60 Hz | 77638950 |
| E-040-073A | Motor and Connector Assy, 50 Hz | 77638951 |
| E-040-074 | Blower and Connector Assy, 60 Hz | 77622885 |
| E-040-074A | Blower and Connector Assy, 50 Hz | 77622886 |
| E-066-370 | AC Distribution PWA | 77666500 |
| E-066-422 | Read/Write Pre-Amp PWA | 77659600 |
| E-066-423 | Read Signal Processor (RSP) PWA | 77666450 |
| E-066-424 | Base Board PWA | 77685900 |
| E-066-372 | Speed Sensor and Connector Assy | 77622862 |

*Refer to Table 5-1 for printed circuit board identification no.

FIGURE 7-1. LARK MICRO UNIT ASSEMBLY (SHEET 2 OF 2)



LARK DRIVE

STATUS CODES

MODULE III

LARK II 50MB STATUS CODES

The Status Codes described in this module were extracted from CDC Application Note No. 77715907, MC Status Code. Copyright 1983 by Magnetic Peripherals, Inc.

The LARK 50 status codes not only define specific faults, but provide a history of firmware and hardware activity leading up to the fault condition. Up to 16 codes may be stored in a cumulative fashion and can be cleared by the user only by reading them via the front panel display. The front panel display will only become active whenever a drive condition occurs that results in a fault.

The codes will be displayed, oldest to latest, at one-second intervals after the operator panel fault reset is activated. You should have some method of recording the faults as they appear. The codes will give a history of drive activity from the last time the codes were cleared, or the drive powered down, up to the code giving the cause for the present fault condition. The code for the current fault is always the last one displayed.

All disk drives will experience some recoverable errors (soft errors) in normal operation and typically have a method for recovery from these errors. Only when these errors become frequent is a potential problem indicated. The Lark drive will store the code for a soft error, even though it is recovered as part of the normal operation of the drive. It may be necessary to separate soft error codes and event (none error) codes from the codes pertinent to the fault condition.

All notes referenced under Interface Fault may be located on the last page of this document. There are three acronyms used in the table that need definition:

1. PLO - Phase Lock Oscillator
2. LDI - Lark Drive Interface
3. PDQ - Protect Data Quality (Head Output Test - see note 3)

The Status Codes are divided into these basic groupings:

| <u>PAGE</u> | <u>TABLE</u> | <u>DRIVE OPERATION OR ACTIVITY</u> |
|-------------|-----------------------|----------------------------------------|
| 1 | 1 | General |
| 2 | 2 | Head Load Operation |
| 3 | 3 | Seek Operation |
| 4 | 4 | Phase Lock Operation |
| 5 | 5 | Head Retract Operation |
| 6 | 6 | Head Select Operation |
| 8 | 7 | Settle Operation |
| 9 | 8 | PDQ Test |
| 10 | 9 | Spindle Motor Start/Stop Operation |
| 11 | 10 | Self Test Operation |
| 12 | 11 | Velocity Transducer Feedback Operation |
| 13 | 12 | Cartridge Type Determination |
| 14 | 13 | Event Module |
| 15 | 14 | Idle State Operation |
| 16 | Notes for Tables 1-14 | |

TABLE 1 - GENERAL

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|
| 11 | Microprocessor time log overflow. Microprocessor is unable to satisfy all timing requirements expected from different firmware modules. | Inability to maintain phase lock of PLO or synchronization of servo data recovery circuits with embedded servo data zones, due to circuit failure or noise. Possible media defect. | Drive | Note 1 |
| 12 | Heads retracted - micro-processor malfunction--invalid data in RAM. | Component failures affecting data bus or disruption of bus due to short circuit, open circuit, noise, etc. | Drive | Yes |
| 13 | Affects front panel display only. Status code in memory was overwritten after display was initiated. | An additional status code was recorded when the status code memory was full. | Drive or User | Note 1 |

TABLE 2 - HEAD LOAD OPERATION

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|------------------------|------------------------|
| 18 | Microprocessor malfunction during RPM check. | Reference Code 12. | Drive | Yes |
| 19 | Spindle RPM too fast. | Spin speed pulse sensor/circuit fault. Spindle motor, pulleys, belt, etc. | Drive | Yes |
| 1A | Spindle RPM too slow. | Reference Code 19. | Drive | Yes |
| 1B | Fault before load attempted. | Unexpected velocity transducer output. Also Reference Code 1C. | Drive | Yes |
| 1C | Fault after load. | Activation of Read/Write gate before interface ready or a circuit failure. | Drive or User | Yes |
| 1D | Invalid cylinder address. Seek error reported on interface. | Default load address (Cyl 0) changed by user system. Only possible with LDI. | User | Note 1 |
| 1E | No positioner velocity detected or Read/Write fault. | Velocity transducer failure due to cables improperly installed or component failure. Reference Code 1C also. | Drive | Yes |
| 51 thru 57 | Pre-load logic state error. Microprocessor status inputs not equal to expected values. Lower three bits of code are coded to identify specific failure. | Failure of carriage retract switch, unsafe circuitry, or retriggerable one shot for servo data valid one shot. | Drive | Yes Note 2 |
| 59 thru 5F | Post-load logic state error. Microprocessor status inputs not equal to expected values. Lower three bits coded to identify specific failure. | Failure of retriggerable RPM detect one shot. Also reference Codes 51-57. | Drive | Yes Note 2 |

TABLE 3 - SEEK OPERATION

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-----------------|------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|
| 21 | Heads retracted because no flux reversals detected through read chain (50% data) during a 1.1 ms interval. | Heads not positioned between inner and outer guard bands due to servo system failure. May be read chain or servo recovery circuit failure. Possible media defect. | Drive | Yes |
| 22 | No embedded servo data (servo data valid) detected during a 1.1 ms interval. Recovery is attempted. | False embedded servo detection during head change operation. Possible media defect, although occasional appearance of this code is to be expected. Reference Code 11. | Drive | Note 1 |
| 23 | Heads retracted because operation time limit expired. | Actuator/servo circuit failure. May also occur during recovery-- especially if Code 63 is stored. | Drive | Yes |
| 25 | Apparent overshoot of destination track. Recovery is attempted. | Actuator velocity error due to circuit or microprocessor command fault. Also may indicate failure to read the embedded servo data correctly. | Drive | Note 1 |
| 26 | Heads retracted-- microprocessor malfunction --invalid data in RAM. | Reference Code 12. | Drive | Yes |
| 27 | Improper velocity command at end of seek. | Microprocessor port 1 circuit failure. May be internal or external to microprocessor. Reference Code 12 also. | Drive | Note 1 |
| 29 thru 2F | Heads retracted. Unsafe condition detected. | Unexpected Read/Write fault. May be caused by read or write gate circuit failure. Loss of RPM or servo data valid pulses. | Drive | Yes |

TABLE 4 - PHASE LOCK OPERATION

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|----------------------------|----------------------------|
| 30 | Heads retracted because phase lock was not achieved within time limit. Head #1 was selected. | Phase lock oscillator circuit failure to lock to embedded servo zones. Possible media defect. | Drive | Yes |
| 31 | Same as Code 30 except head #3. | Reference Code 30. | Drive | Yes |
| 32 | Same as Code 30 except head #0. | Reference Code 30. | Drive | Yes |
| 33 | Same as Code 30 except head #2. | Reference Code 30. | Drive | Yes. |
| 34 | Heads retracted because phase lock oscillator failed to lock before head reached inner guard band. | Reference Code 21. | Drive | Yes |
| 35 | Same as Code 34 except head #3. | Reference Code 21. | Drive | Yes |
| 36 | Same as Code 34 except head #0. | Reference Code 21. | Drive | Yes |
| 37 | Same as Code 34 except head #2. | Reference Code 21. | Drive | Yes |
| 38 | Heads retracted because of too many phase lock attempts during one activity, i.e., seek, head select, RTZ. Phase lock was indicated, but either the indication was false or phase lock was not maintained. | Erroneous phase lock due to media defects, servo or read circuit failure, unstable PLO, etc. | Drive | Yes |

TABLE 5 - HEAD RETRACT OPERATION

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|
| 40 | Head retract completed using hardware emergency retract circuits. This code will not appear, unless following codes 41, 43, 44, 45, or 47. | Backup required due to failure of normal head retract. Loss of DC voltages, servo data valid, or RPM watchdog timer. Reference Code 41. | Drive | Yes |
| 41 | Normal retract not completed successfully because servo data is still detected (50% data). PLO is not locked and switch indicates heads are retracted. | Failure of Servo/Read chain to detect embedded servo fields. RPM out of limits. Heads are positioned outside the normal servo zones. | Drive | Yes |
| 43 | Same as Code 41 except PLO is locked. Servo data is still detected, yet switch indicates carriage retracted. | Reference Code 41. | Drive | Yes |
| 44 | Carriage retract switch indicates heads are still loaded. PLO is unlocked and no servo data is detected. | Failure of carriage retract switch or associated circuit. Reference Code 41. | Drive | Yes |
| 45 | Same as Code 41 except switch indicates heads are loaded. PLO is unlocked and no servo data is detected (50%). | Reference Code 41. | Drive | Yes |
| 47 | Same as Code 41 except PLO is locked and switch indicates heads are loaded. Servo data is detected (50%). | Absence of normal servo reverse drive signal due to failure in servo analog reverse circuit. | Drive | Yes |

TABLE 6 - HEAD SELECT OPERATION

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|---------------------------------|
| 61 | Heads retracted because no flux reversals detected through read chain (50% data) during a 1.1 ms interval. | Heads not positioned between inner and outer guardbands due to servo system failure. May be read chain or servo recovery circuit failure. Possible media defect. | Drive | Yes |
| 62 | No embedded servo data (servo data valid) detected during a 1.1 ms interval. Recovery is attempted. | False embedded servo detection during head change operation. Possible media defect or summation of user data fields. Occasional appearance of this code is to be expected. Reference Code 11. | Drive | Note 1, or Yes if seek recovery |
| 63 | Repeated attempts to synchronize digital circuits to embedded servo have failed. Indicates need to enter phase lock mode (frequency mode) because of excessive phase error. | Servo data circuits failed to detect correct embedded servo field gap. May be caused by false gap detection or failure of PLO and associated servo data recovery circuit. | Drive | Yes |
| 65 | Time limit expired while reading current location. Heads are retracted. | This code is not expected, unless a preceding operation required excessive time. If recovery was in process, preceding code(s) will indicate cause. If no codes are preceding, the previous operation was probably phase lock; otherwise, actuator servo circuit has failed. | Drive User | Note 2 |
| 66 | Time limit expired while moving to destination tracks. Heads are retracted. | Reference Code 65. | Drive | Yes |

TABLE 6 - HEAD SELECT OPERATION (continued)

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|---------------------|--------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|----------------------------|
| 69 thru 6F | Unsafe condition detected. Heads are retracted. | Unexpected Read/Write fault may be caused by read or write gate. Loss of RPM or servo data valid pulses. | Drive | Note 2 |
| 71 | Too much offset between current head and previous head. Recovery is attempted. | Mechanical head toler- ances are excessive. May be servo or servo data recovery circuit failure. | Drive | Note 1 |
| 72 | Invalid track address detected. Address found is outside the range of 0 to 623. Recovery is attempted. | PLO may be locked falsely, i.e., to false gaps or servo data recovery circuit failure. Possible media defect. | Drive | Note 1 |
| 73 | Overshoot of destination track. Recovery is attempted. | Actuator velocity error due to circuit or microprocessor command fault. Also, may indi- cate failure to read the embedded servo field correctly. Possible media defect. | Drive | Note 1 |

TABLE 7 - SETTLE OPERATION

| <u>CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-------------|-----------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|
| 81 | Heads retracted because no flux reversals were detected through read chain (50% data) during a 1.1 ms interval. | Heads not positioned between inner and outer guard bands due to servo system failure. May be read chain or servo recovery circuit failure. Possible media defect. | Drive | Yes |
| 82 | No embedded servo data (servo data valid) detected during a 1.1 ms interval. Recovery is attempted. | Inability to maintain phase lock of PLO or synchronization of servo data recovery circuits with embedded servo data zones, due to recovery circuit failure. Possible media defect. | Drive | Note 1 |
| 83 | Time limit has expired during settle. Heads are retracted. | Reference Code 65. | Drive | Yes |
| 84 | Track address from embedded servo data not as expected. Recovery is attempted. | Positioner servo circuit failure causing over velocity during final approach. Servo data recovery circuit failure. Possible media defect. | Drive | Note 1 |

TABLE 8 - PDQ TEST

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-----------------|------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|
| 88 | PDQ failure while using head #1. Heads are retracted. Rapid blinking of fault LED. | Head/media integrity problem. Head output is not adequate to assure proper servoing, writing, or reading of drive/media. | Drive | Yes Note 3 |
| 89 | Same as Code 88 except head #3. | Reference Code 88. | Drive | Yes Note 3 |
| 8A | Same as Code 88 except head #0. | Reference Code 88. | Drive | Yes Note 3 |
| 8B | Same as Code 88 except head #2. | Reference Code 88. | Drive | Yes Note 3 |
| 8C | Reference Code 12. | Reference Code 12. | Drive | Yes Note 3 |
| 8D | Maximum number of PDQ retries has been exhausted. | Too many fault clear commands have been issued. | User | Yes Note 3 |
| 8E | An attempt has been made to disable PDQ feature. May also be ROM check failure. | Improper PDQ disable procedure followed. For qualified use only. | User | Yes Note 3 |

TABLE 9 - SPINDLE MOTOR START/STOP OPERATION

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|---------------------|------------------------------------------------------------------------|----------------------------------------------------------------------------------|----------------------------|----------------------------|
| 90 | Reference Code 12. | Reference Code 12. | Drive | Yes |
| 91 | Spindle RPM too slow before head load. | Failure of motor, pulleys, belt, motor control circuit. AC line voltage problem. | Drive | Yes |
| 92 | Spindle RPM too fast before head load. | Reference Code 91. | Drive | Yes |
| 93 | Spindle will not stop. | Motor control circuit failure. Possible spin pulse sensor failure. | Drive | Yes |
| 94 | Spindle RPM not as expected (measured 60 seconds after start command). | Reference codes 91 and 93. | Drive | Yes |

TABLE 10 - SELF TEST OPERATION

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-----------------|------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|------------------------|------------------------|
| 95 | ROM check failure. | Failure of microprocessor address bus, data bus, EPROM or ROM. | Drive | |
| 96 | Data read from microprocessor Port 2 does not equal data written. | Microprocessor Port 2 failure. | Drive | |
| 97 | Same as Code 96 except Port 1. | Reference Code 96 except Port 1. | Drive | |
| 98 | Microprocessor internal timer failure. | Microprocessor | Drive | |
| 99 | Microprocessor input status error. | Failure of U22, carriage loaded switch, servo data valid one shot, or unsafe circuit. | Drive | |
| 9A | Failure of servo data test. Microprocessor simulates normal track address output of servo LSI. | Servo data recovery circuit. Microprocessor or wrap-around path failure. | Drive | |
| 9B | Microprocessor input status error. | Failure of U22, read or write fault circuit, or velocity transducer output detected. | Drive | |
| 9C | Microprocessor bus expander chip (8243) test failure. | Failure of 8243, 8243 output pins grounded, or microprocessor Port 2, bits 0-3 shorted or open. | Drive | |
| 9D | Failed servo data valid test. Microprocessor simulates servo data valid output of servo LSI. | Reference Code 9A. | Drive | |
| 9E | No spin pulse detected. | Spin speed pulse sensor. Base Board spin pulse circuits. | Drive | |

TABLE 11 - VELOCITY TRANSDUCER FEEDBACK OPERATION

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|---------------------|------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|----------------------------|
| A0 | Gain adjust time limit has expired. Heads are retracted. | Failure of actuator servo circuit or servo data recovery. | Drive | Yes |
| A1 | Heads retracted because no flux reversals detected through read chain (50% data) during a 1.1 ms interval. | Heads not positioned between inner and outer guard bands due to servo system failure. | Drive | Yes |
| A2 | No embedded servo data (servo data valid) detected during a 1.1 ms interval. Recovery is attempted. | False embedded servo detection during head change operation. Possible media defect, although occasional appearance of this code is to be expected. | Drive | Note 1 |
| A3 | Start point for velocity timing measurement has been passed, but not recognized. Recovery is attempted. | Failure in servo data recovery circuits or excessive velocity applied to actuator. | Drive | Note 1 |
| A4 | Finish point for velocity timing measurement has been passed, but not recognized. Recovery is attempted. | Reference Code A3. | Drive | Note 1 |
| A5 | Velocity at this gain step is too fast. Operation is terminated. Minimum velocity selected. | Failure of transducer gain adjust circuitry or actuator servo circuit. | Drive | Note 1 |
| A6 | Velocity cannot be calibrated to proper value. Operation is terminated. Minimum velocity selected. | Reference Code A5. | Drive | Note 1 |
| A7 | Microprocessor failure. Invalid data in RAM. Operation terminated. Minimum velocity selected. | Component failures affecting data bus or disruption of data bus due to open or short circuit, noise, etc. | Drive | Note 1 |

TABLE 12 - CARTRIDGE TYPE DETERMINATION

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|
| A8 | Heads retracted because operation time limit expired. | Actuator/servo circuit failure. May also occur during recovery especially if code 63 is stored. | Drive | Yes |
| A9 | Cannot determine the cartridge type. Heads are retracted. | Defective cartridge or head failure. | Drive Cartridge | Yes |
| AA | Attempt to use a Lark 16 cartridge with obsolete 64 embedded servo field format. | Invalid cartridge. | Cartridge | Yes |
| AC | Failure occurred when cartridge was initially selected. No embedded servo data (servo data valid) detected during a 1.1 ms interval. Recovery is attempted. | False embedded servo detection during head change operation. Possible media defect although occasional appearance of this code is to be expected. Reference Code 11. | Drive Cartridge | Note 1 |

TABLE 13 - EVENT MODULE

| <u>HEX CODE</u> | <u>CODE DEFINITION</u> | <u>PROBABLE CAUSE</u> | <u>PROBABLE SOURCE</u> | <u>INTERFACE FAULT</u> |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|------------------------|------------------------|
| B0 | Drive deselected during interface dialog sequence. Normally only possible using LDI interfaces. | Protocol error, defective drive cables or failure of select circuitry in host or drive. | Host Drive | Yes |
| B1 | Invalid event byte. Spindle off together with seek, RTZ, or Head Select. | Protocol error. Possible cable or termination problem. | Host | Yes |
| B2 | Invalid event byte. Normally only possible using LDI interface. | Spindle off together with spindle on. | Host | Yes |
| B3 | Invalid event byte. Head Select, or RTZ while heads retracted, but without fault reset. | Protocol error. | Host | Yes |
| B4 | Interface dialogue error. Acknowledge not activated within 500 us after bus ready is activated. Normally only possible using LDI interface. | Protocol error or failure of SMD adapter using SMD interface. | Host | Yes |
| B5 | Interface dialogue error. Acknowledge not deactivated within 500 us after bus ready deactivated. Normally only possible using LDI interface. | Reference Code B4. | Host Drive | Yes |
| B6 | Track addressed is greater than drive maximum limit. Seek error will be set. | Protocol error. | Host | Note 1 |
| B7 | Head addressed is greater than drive maximum limit. Seek error will be set. Normally only possible using LDI. | Protocol error. | Host Drive | Note 1 |
| B8 | Interface dialogue error. Seek, Head Select, or RTZ with spindle stopped and without spindle on command. | Protocol error. | Host | Yes |
| BD | Indicates that all bytes regarding firmware revision level have been read. LDI only. | Normal | Drive | Note 1 |

TABLE 14 - IDLE STATE OPERATION

| HEX CODE | CODE DEFINITION | PROBABLE CAUSE | PROBABLE SOURCE | INTERFACE FAULT | |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----------------|----|
| C1 | Heads retracted because no flux reversals were detected through read chain (50% data) during a 1.1 ms interval. | Heads not positioned between inner and outer guard bands due to servo system failure. May be recovery circuit failure. Possible media defect. | Drive | Yes | 08 |
| C2 | Heads retracted. No embedded servo data (servo data valid) detected during a 1.1 ms interval. Recovery is attempted. | False embedded servo detection during head change operation. Possible media defect although occasional appearance of this code is to be expected. Reference Code 11. | Drive | Yes | 08 |
| C9 CF | Heads retracted because thru unsafe condition was detected. | Unexpected Read/Write fault. May be caused by read or write gate Loss of RPM or servo data valid pulses. | Drive | Yes | 48 |
| D1 | Reference Code 22 | Reference Code 22. | Drive | Yes | |
| D2 | Heads retracted. RPM is too slow. | Reference Code 91. | Drive | Yes | |
| D4 | Heads retracted. RPM is too fast. | Reference Code 91. | Drive | Yes | |
| D9 | Drive was positioned on track and subsequently lock track center. Seek error is reported. | Failure of servo circuit or position error circuit. Possible media defect or excessive runout. | Drive | Note 1 | 18 |
| DA | Embedded servo data was as expected and subsequently became erroneous. | Failure of servo positioning circuit or servo data recovery. Possible media defect. | Drive | Note 1 | |
| DB | Read/Write fault. Read gate while off cylinder. Read and write gate on together. Write protect with write gate. Write gate and servo write protect. | Usually protocol error although may be a problem in read circuits. | Drive | Yes | 08 |

NOTES FOR TABLES 1 - 14

NOTE 1: The fault bit in the status byte will not be changed from its previous status.

NOTE 2: One or more of the three low order bits will be set for Codes 29-2F, 69-6F, or C9-CF. The interpretation of the three low order bits is given in the following table:

| <u>Bit</u> | <u>Interpretation</u> |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | Unsafe latch is set in Read/Write preamplifier. |
| 1 | The retriggerable one-shot which is set by the servo-data-valid pulse is reset. This one-shot will be held reset if another one-shot which is set by "spindle pulses" is reset. |
| 2 | Always ZERO. |

NOTE 3: PDQ is test performed at head load or unload to verify sufficient head output for subsequent write/read operations. Heads will retract on failure and the fault lamp will blink at double the normal rate. The first code is the surface on which the fault occurred. The second and third codes provide the absolute cylinder address in hex. To obtain the decimal equivalent, subtract one from each of the two codes, then convert the code to decimal. Twelve is then subtracted from the result, providing the failing track. If the track is 243 or 499, the second code is zero and not displayed.

For a description of the PDQ test, refer to Module II, section 2.5.

To disable the PDQ temporarily, place a jumper across J2 on the Preamp Piggyback board. Install this jumper only for backup or recovery of cartridges that fail the PDQ test. Refer to Module II, Figure 5-5A.

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