ANALOG INTEGRATED CIRCUITS

FUNDAMENTALS

and

APPLICATIONS

VIDEO COURSE
STUDY GUIDE

Return for use by other employees

MAGNETIC PERIPHERALS INC.
a subsidiary of
CONTROL DATA CORPORATION

P.O. Box 12313
Oklahoma City, Oklahoma 73157

RIGID DISK ENGINEERING

1984

THIS COURSE IS INTENDED FOR

1. Electrical engineers who have graduated some time ago and feel the need to refresh and update their knowledge on transistor circuits.
2. Electrical engineers who have graduated recently but feel the need to have a quick review and then go much more in depth and coverage than normally encountered in undergraduate study of transistor circuits.
3. Other engineers and scientists who like to acquire the necessary knowledge on transistor circuits in a very short time.

THE GOALS OF THE COURSE ARE

1. Starting with the fundamentals, present a thorough and extensive understanding of the low-frequency behavior of the bipolar transistor.
2. Present and discuss in detail commonly used discrete and integrated analog circuits.
3. Provide design oriented practical information that can be used readily.
4. Provide the necessary tools, skills, and confidence for analyzing as well as designing analog transistor circuits.

HOW THE GOALS ARE ACHIEVED

1. By solving one practical circuit problem after another.
2. By demonstrating the actual performance characteristics of some of the widely used circuits that are discussed.
3. By putting together circuits that are commonly used as building blocks to design more complex circuits.

SUGGESTED STUDY FORMAT

1. View the videotape.
2. Then try to reproduce all derivations on your own. Since the lectures are entirely on analysis and discussion of practical and useful circuits, being able to derive all the results by oneself demonstrates intimate knowledge and understanding of the circuits involved.

PREFACE

The course deals with bipolar transistor analog circuits that are essential in the design of a large variety of amplifiers. The entire series consists of 19 videotapes, averaging about 43 minutes in length, devoted to a thorough understanding of widely used amplifier circuits. For convenience, the series is divided into four modules.

Module A: Bipolar Transistor Fundamentals and Basic Amplifier Circuits.

The characteristics of diodes and bipolar transistors are presented and discussed. Then the small-signal equivalent circuits are derived. Large and small-signal characteristics of common-emitter, common-base, common-collector, and composite transistor amplifiers are derived and discussed. (Seven lectures with five demonstrations.)

Module B: Current Sources and Applications.

Widely used dc current sources are presented and discussed in detail. (Four lectures with one demonstration.)

Module C: The Differental Amplifier.

The differential amplifier is discussed in detail. (Four lectures with three demonstrations.)

Module D: Class A, B, and AB Output Stages and μA741 Operational Amplifier.

Class A, class B, and class AB output stages are discussed in detail. Finally, the versatility of the circuits discussed in various modules is demonstrated by showing how they are put together in the design of the μA741 operational amplifier. (Four lectures with two demonstrations.)

PREREQUISITES

1. Working knowledge of circuit theory. Knowledge of Laplace transformation is not necessary.
2. Understanding of basic transistor circuits. Determined individuals can acquire this knowledge while taking this videotaped course since it covers the basics as well as more advanced material.

REFERENCES

1. Analysis and Design of Analog Integrated Circuits, P.R. Gray and R.G. Meyer, Wiley 1977. This is a basic reference and can be used as textbook to supplement the videotaped lectures.
2. Basic Integrated Circuit Engineering, D.J. Hamilton and W.G. Howard, McGraw Hill, 1975.
3. Introduction to Integrated Circuits, V.H. Grinich and H.G. Jackson, McGraw Hill, 1975.
4. Applied Electronics, J.F. Pierce and T.J. Paulus, Bell and Howell, 1972.

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MODULE A

LECTURE SUMMARIES

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1. Characteristics of diodes and transistors.

   The pn junction diode equation is presented and discussed. The input and output characteristics of the bipolar transistor are derived from the Ebers-Moll model. Circuit models are obtained with V_{be} or I_b as a dependent parameter. Departures from the Ebers-Moll model are discussed.

   Demonstration: The output voltage of a discrete transistor is compared with an integrated circuit.

2. The small-signal equivalent circuit of transistors.

   Using the forward-active-region large-signal characteristics of the transistor, the small-signal input- and output- equivalent circuits are obtained. r_π, g_m, β, and r_o are defined graphically as well as mathematically.

3. The common-emitter amplifier.

   The large-signal characteristics of the common-emitter amplifier with resistive load are presented. The small-signal characteristics are derived, and the expression of gain as a function of the operating point is obtained and plotted. The common-emitter amplifier with current-source load is discussed.

   Demonstration: The transfer characteristics of common-emitter amplifiers with resistive and current-source loads are compared.

4. The common-base and the common-emitter amplifier.

General analysis of transistor circuits. The large-signal characteristics of the common-base and common-emitter amplifers are derived. The operating point of a transistor circuit having a resistance and a voltage source connected in series with each terminal lead and ground is obtained. The small-signal equivalent circuits facing each source are derived.

Demonstration: Distortions caused by voltage and current excitations are compared for small and not so small sinusoidal output-signal amplitudes.

5. Input and output-equivalent circuits. Input- and output-equivalent circuits for the common-emitter, common-base, and common-collector amplifiers are obtained with and without the r_o of the transistor.

6. CC-CC, CC-CE, and CE-CB amplfiers. Equivalent circuits of composite CC-CC, CC-CE, and CE-CB transistors are obtained. The large- and small-signal characteristics of the cascode amplifier are derived.

Demonstration: The collector characteristics of the transistor are compared with the cascode-connected transistor.

7. Biasing. The power-supply sensitivities of base-current and base-voltage controlled-bias circuits are compared. Fixed collector-current bias circuits using one and two power supplies are given. The need for using dc current sources for biasing is shown.

Demonstration: Power supply sensitivities of fixed base-current and fixed base-voltage bias circuits are compared.

MODULE B

LECTURE SUMMARIES

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8. <u>Dc current sources</u>. The ideal and actual dc current source characteristics are presented. Methods are given for measuring the output characteristic curve. Equivalent circuits of current sources using a single transistor with one or two power supplies are derived. The basic integrated circuit used for current source generation is introduced and discussed.

9. <u>Dc current sources</u>. Current sources based on a common reference are given. Causes for mismatches in current sources are discussed. The Widlar current source is introduced and its reduced dependence on power supply voltages is shown.

10. <u>Widlar and cascode current sources</u>. The output equivalent circuits of the Widlar and cascode current sources are derived. Different value current source circuits based on a common reference are given. A stabilized bias circuit for an amplifier is discussed.

    <u>Demonstration</u>: The characteristics of a simple, a Widlar, and a cascode current source are compared.

11. <u>The common-emitter amplifier with resistive and active loads</u>. The large- and small-signal characteristics of the common-emitter amplifier are discussed graphically and analytically for three kinds of loads: resistive, ideal current source, and actual current source. The expression showing the dependence of the gain on the output operating point is derived.

MODULE C

LECTURE SUMMARIES
12 → 15

12. The differental amplfier. The large- and small-signal characteristics of the differential amplifier are derived. Input- and output-equivalent circuits are given.

    Demonstration The transfer characteristics and the variations of the base-to-emitter voltages of the differential amplifier are displayed.

13. The differential amplifier.(Cont'd). The input is decomposed into the common-and difference-mode components, and the corresponding half circuits are obtained. The expressions for the common- and difference-mode gains are derived. The common-mode-rejection ratio is defined and a method for improving it is given. Mismatches in resistor and saturation current values are shown to result in the offset voltage.

14. The differential amplifier.(Cont'd). Offset current is defined and calculated. A method for measuring offset voltage and current is given. The input resistance and the gain of two differential amplifiers are compared. A differential amplifier with an active load is presented and the effect of mismatches in saturation currents on the output voltage is calculated.

    Demonstration: A method for measuring ratios of saturation currents is given.

15. The differential amplifier.(Cont'd). The common- and difference-mode gains of the differential amplifier with active load are calculated. The expression for the offset voltage is obtained. A current difference amplifier using a single power supply is presented and discussed.

    Demonstration: The transfer characteristics of the differential amplifier with active load is displayed. The effect of mismatches in saturation currents is demonstrated.

MODULE D

LECTURE SUMMARIES

16 → 19

16. The class-A emitter-follower output stage. The transfer characteristic of the class-A emitter-follower output stage is derived and plotted. The small-signal gain is calculated and is shown to be practically constant regardless of the value of the collector current. Expressions for instantaneous and average output power and power conversion effciency are obtained.

    Demonstration: The transfer characteristic and input and output waveforms of the class-A output stage are demonstrated.

17. The class-A and class-B output stages. Instantaneous and average power dissipation expressions for the class-A output stage are obtained and plotted. The points for maximum collector power and standby collector power dissipation are shown on the load line. The transfer curve of the class-B emitter-follower output stage showing crossover distortion is presented. Various waveforms needed for power calculations are given, and the power conversion efficiency is obtained.

18. The class-AB output stage. The transfer characteristic of the class-AB output stage is derived as a function of the base-to-base voltage, and it is plotted to show how crossover distortion can be eliminated. Means for generating the base-to-base voltage are presented and discussed.

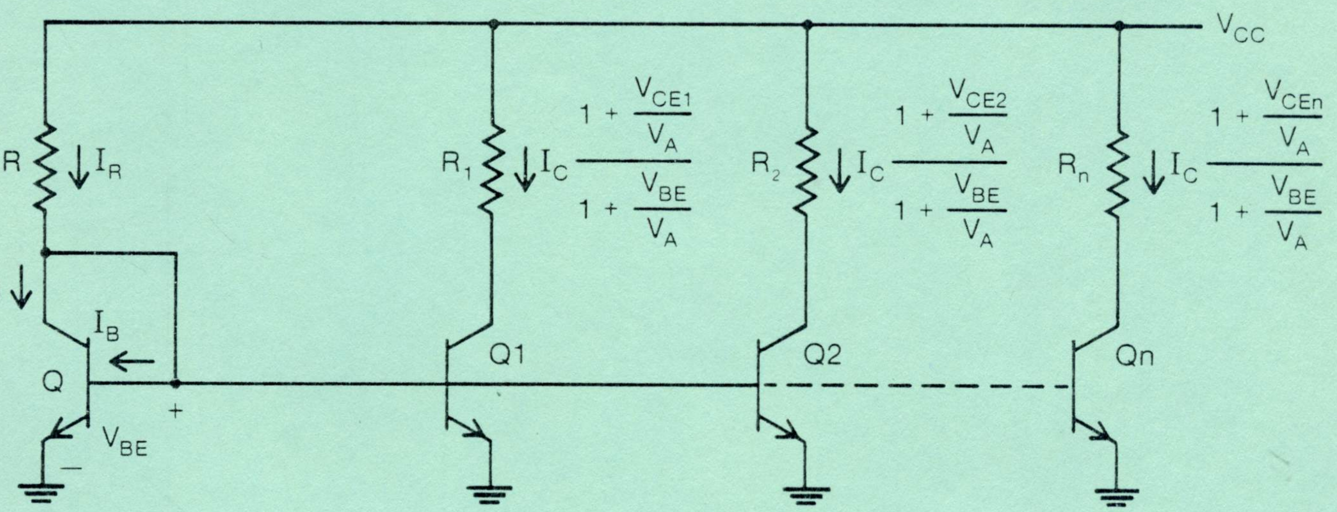
    Demonstration: The transfer characteristics and waveforms associated with the class-AB amplifier are demonstrated.

19. The μA741 operational amplifier. The μA741 operational amplfier is used as an example to show how the various circuits presented and discussed in previous lectures are put together to design an integrated circuit operational amplifier. With the two inputs grounded and the output at zero, all quiescent currents are calculated. Then, the amplifier is partitioned into the input differential stage, the intermediate gain stage, and the output stage. The small-signal input- and output- equivalent circuits are calculated for each stage and then put together to determine the overall gain. Feedback is used to stabilize the gain.

A Self Study Subject

FUNDAMENTALS & APPLICATIONS OF ANALOG INTEGRATED CIRCUITS

PART I
LOW FREQUENCY ANALYSIS & DESIGN



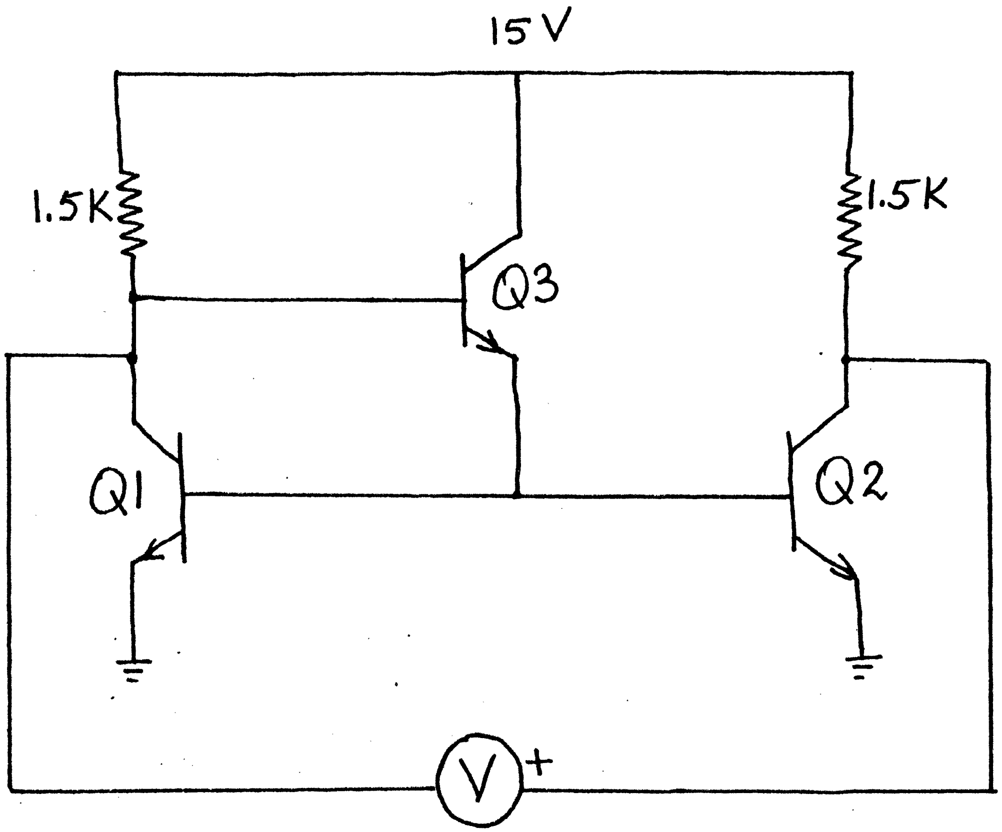
Study Guide
for

MODULE A
Bipolar Transistor Fundamentals & Basic Amplifier Circuits

Colorado State University
Engineering Renewal
& Growth Program

Aram Budak

L1: Comparison of a Discrete Transistor Circuit with an Integrated Circuit



Voltmeter Reading

Discrete: 380 mV

Integrated Circuit: 12 mV

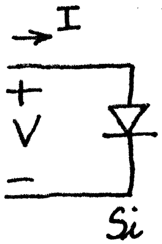
Demostration

Integrated Circuits

Advantages:
1. Circuits containing a large number of elements can be fabricated as a unit on a chip.
2. Size, weight, and cost are reduced.
3. Devices of the same kind have well-matched characteristics. (Ratios of identical resistor values or identical transistor saturation currents are close to unity.)
4. Device characteristics are quite uniform and track well with temperature. (Base-to-emitter voltages of transistors located on isothermal lines change by the same amount and almost at the same time with changes in temperature.)

Disadvantages:
1. Inflexibility. Once manufactured, component values cannot be changed.
2. Absolute values cannot be attained precisely. (Resistor values may be 25% off the desired values.)
3. Choice of component values is restricted. (1 MΩ resistor values and 0.1 μF capacitor values are impractical.)
4. Inductors are unavailable.
5. Compatible active devices are difficult to obtain. (Complementary NPN and PNP bipolar transistors of equal quality are difficult to fabricate on the same chip.)

The Idealized pn Junction Diode

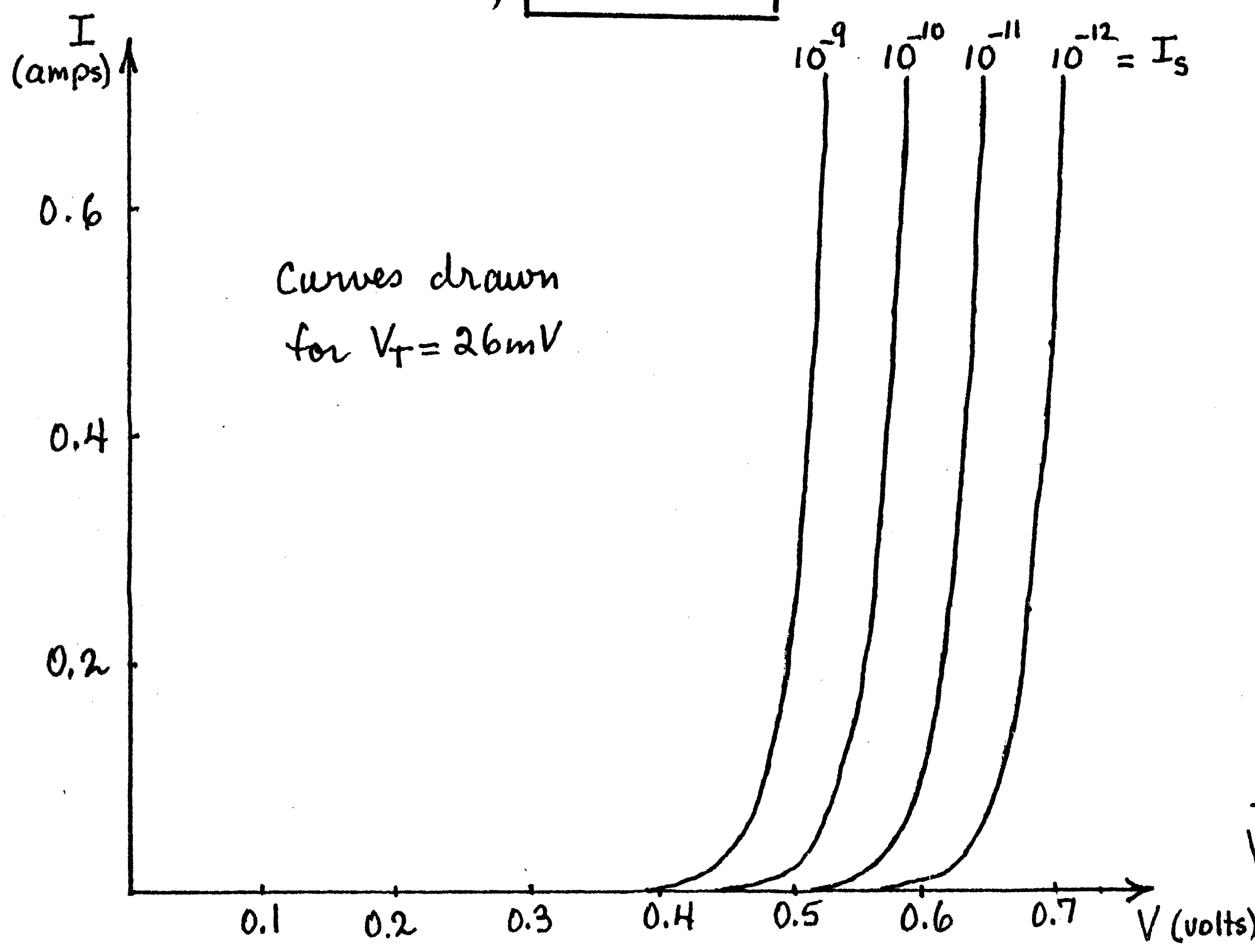


From semiconductor theory $\boxed{I = I_s\left(e^{\frac{V}{V_T}} - 1\right)}$

For $T = 27°C$, $\boxed{V_T = 26\,mV}$

I_s = saturation current
V_T = thermal voltage $= \frac{kT}{q}$
k = Boltzmann's constant
T = absolute temperature
q = electronic charge

[More generally $I = I_s\left(e^{\frac{V}{\eta V_T}} - 1\right)$ where $\eta = 1 \sim 2$.]



Only one constant, I_s, is needed to characterize the diode.

I_s is a strong function of temperature (for Si at room temp., I_s doubles every 10°C)

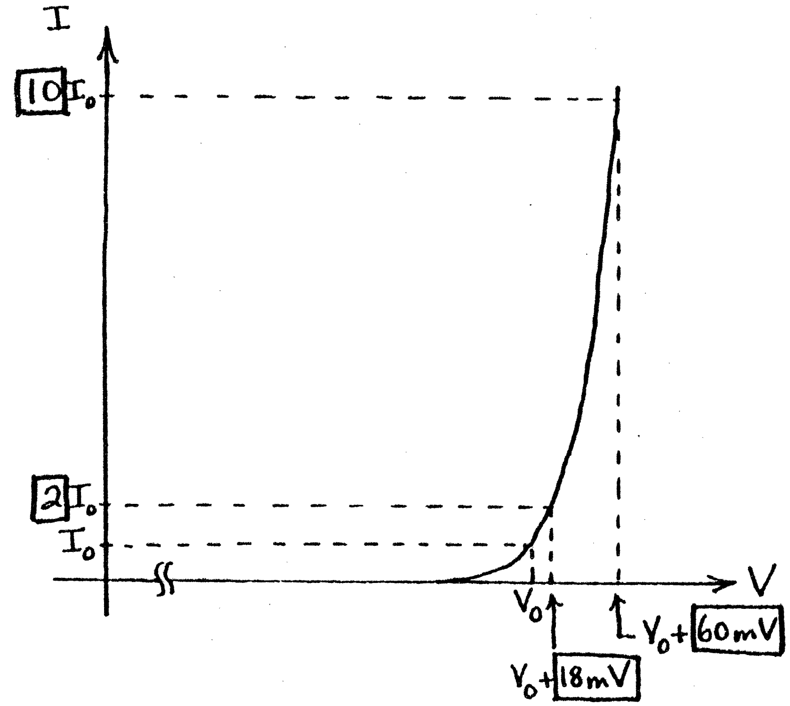
At fixed I, V decreases approx. 2mV/°C.

$\frac{I}{I_s}$	10^7	10^8	10^9	10^{10}	10^{11}	10^{12}
V (mV)	419	479	539	599	659	718

For $\frac{V}{V_T} \leq -5$ (corresponding to $V \leq -130\,mV$ at room temp.), $e^{\frac{V}{V_T}} \leq 0.0067$. $I \cong -I_s$

For $\frac{V}{V_T} \geq 5$ (corresponding to $V \geq 130\,mV$ at room temp.) $e^{\frac{V}{V_T}} \geq 148.41$. $\boxed{I \cong I_s e^{\frac{V}{V_T}}}$

From now on, when the diode is conducting $I = I_s e^{\frac{V}{V_T}}$. (We shall keep in mind that this equation is inaccurate for very small currents; in particular, it predicts $V = -\infty$ to make $I = 0$, which of course is wrong since it takes $V = 0$ to make $I = 0$.)



Let I_o represent the diode current when the voltage across is V_o, i.e.,

$$I_o = I_s e^{\frac{V_o}{V_T}}$$

If the voltage is changed from V_o to $V_o + \Delta V$, the current becomes

$$I = I_s e^{\frac{V_o + \Delta V}{V_T}} = \left(I_s e^{\frac{V_o}{V_T}}\right) e^{\frac{\Delta V}{V_T}} = I_o e^{\frac{\Delta V}{V_T}}$$

For $\Delta V = 18\,mV$,

$$I = I_o e^{18/26} = 1.998\, I_o \cong 2 I_o$$

For $\Delta V = 60\,mV$,

$$I = I_o e^{60/26} = 10.051\, I_o \cong 10\, I_o$$

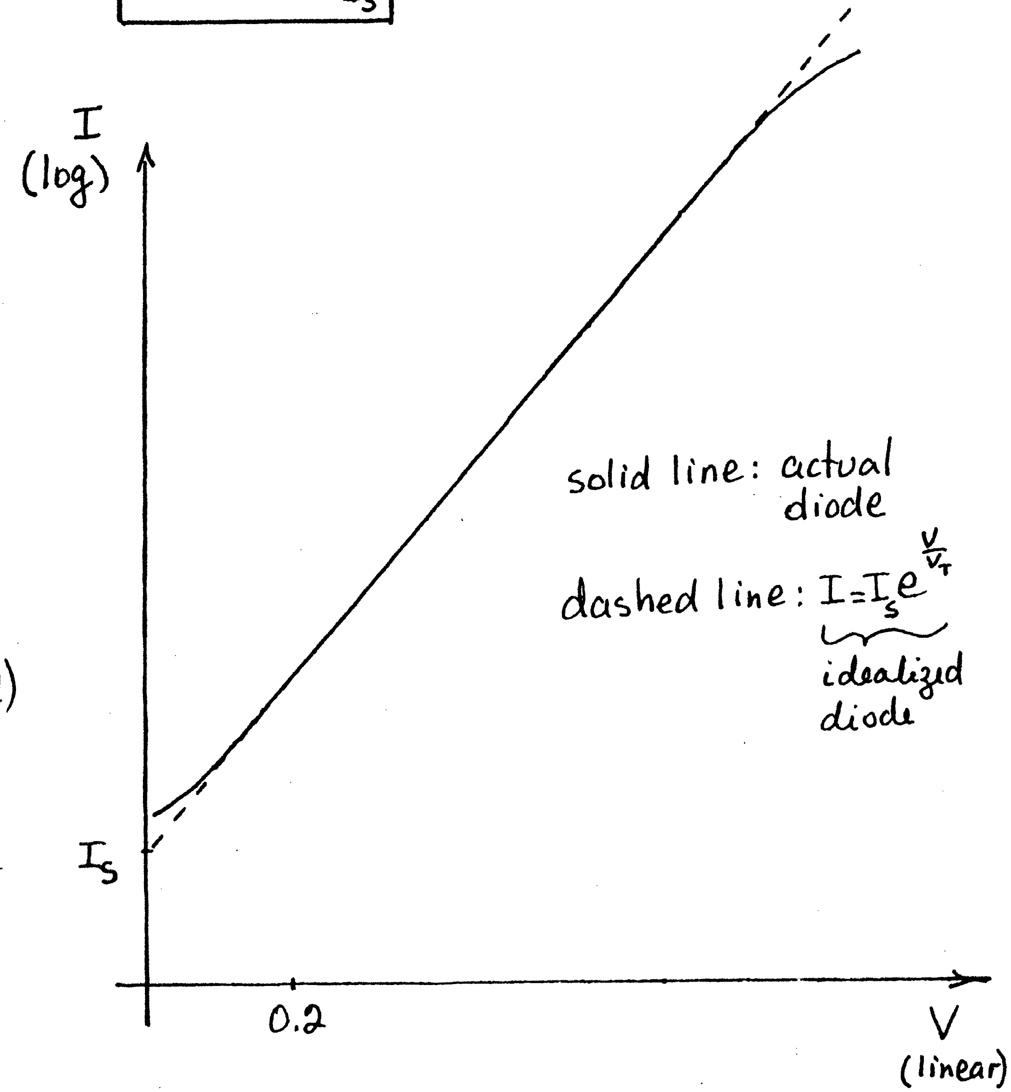
1. It takes a change of 18 mV to double the diode current.
2. It takes a change of 60 mV to change the diode current by a factor of 10.

$$\boxed{I = I_s e^{\frac{V}{V_T}}} \qquad \frac{I}{I_s} = e^{\frac{V}{V_T}} \qquad \ln \frac{I}{I_s} = \frac{V}{V_T} \qquad \boxed{V = V_T \ln \frac{I}{I_s}}$$

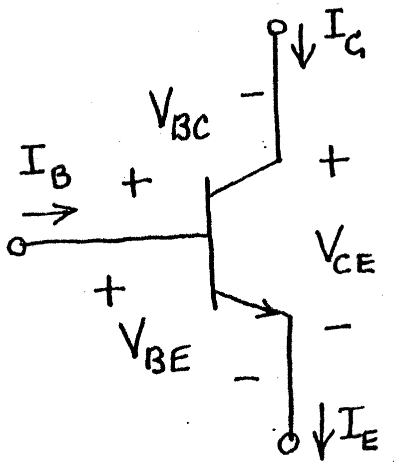
Also, $\ln I = \ln I_s + \frac{V}{V_T}$.

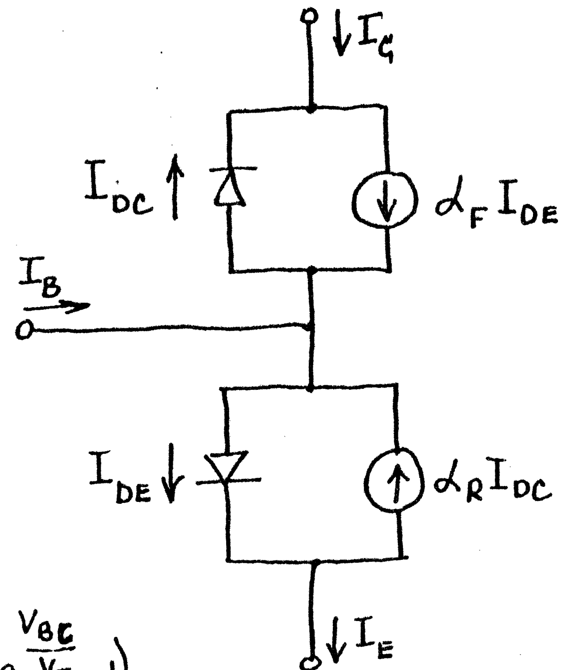
Hence, when I is plotted vs. V on semi-log paper, a straight line with a slope of $\frac{1}{V_T}$ results. The I-axis intercept is I_s, the saturation current.

A best straight line fit (dashed) can be drawn to characterize the actual (solid) diode curve. The two curves match very well over at least three to four decades of current.



The Idealized Transistor





Ebers-Moll model of the transistor

α_F = forward alpha $\cong 0.99$

α_R = inverse alpha $\cong 0.5 - 0.8$

I_{CS} = collector diode sat. current

I_{ES} = emitter diode sat. current

$$I_{DE} = I_{ES}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) \qquad I_{DC} = I_{CS}\left(e^{\frac{V_{BC}}{V_T}} - 1\right)$$

$$\left\{\begin{aligned} I_C &= \alpha_F I_{DE} - I_{DC} = \alpha_F I_{ES}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - I_{CS}\left(e^{\frac{V_{BC}}{V_T}} - 1\right) \\ I_E &= I_{DE} - \alpha_R I_{DC} = I_{ES}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - \alpha_R I_{CS}\left(e^{\frac{V_{BC}}{V_T}} - 1\right) \end{aligned}\right\} \text{ Ebers-Moll eqs.}$$

$$I_B = I_E - I_C = (1-\alpha_F) I_{ES}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) + (1-\alpha_R) I_{CS}\left(e^{\frac{V_{BC}}{V_T}} - 1\right) \quad ; \quad V_{BC} = V_{BE} - V_{CE}$$

$\alpha_F I_{ES} = \alpha_R I_{CS} = I_S$ typical values of $I_S = 10^{-15} - 10^{-14}$ A

β_F = forward beta $= \dfrac{\alpha_F}{1-\alpha_F}$ $\qquad$ β_R = inverse beta $= \dfrac{\alpha_R}{1-\alpha_R}$

$$\beta_F = \begin{cases} 50-500 \text{ NPN} \\ 10-100 \text{ PNP} \end{cases} \qquad \beta_R = 1-5$$

$$\left.\begin{cases} I_B = \dfrac{I_S e^{\frac{V_{BE}}{V_T}}}{\beta_F}\left(1+\dfrac{\beta_F}{\beta_R} e^{-\frac{V_{CE}}{V_T}}\right) - I_S\left(\dfrac{1}{\beta_F}+\dfrac{1}{\beta_R}\right) \\[2ex] I_C = I_S e^{\frac{V_{BE}}{V_T}}\left(1 - \dfrac{1+\beta_R}{\beta_R} e^{-\frac{V_{CE}}{V_T}}\right) + \dfrac{I_S}{\beta_R} \end{cases}\right\} \text{ exact eqs.}$$

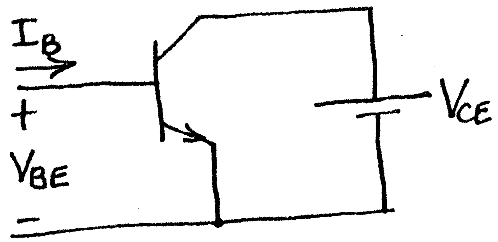
Assume $V_{CE} \geq 10 V_T$ (260mV) ; then $\dfrac{\beta_F}{\beta_R} e^{-\frac{V_{CE}}{V_T}} \ll 1$, $\dfrac{1+\beta_R}{\beta_R} e^{-\frac{V_{CE}}{V_T}} \ll 1$

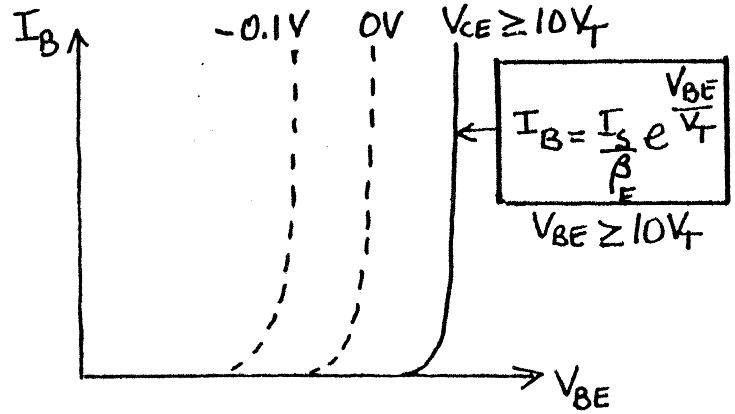
$$\left.\begin{cases} I_B \cong \dfrac{I_S e^{\frac{V_{BE}}{V_T}}}{\beta_F} - I_S\left(\dfrac{1}{\beta_F}+\dfrac{1}{\beta_R}\right) \\[2ex] I_C \cong I_S e^{\frac{V_{BE}}{V_T}} + \dfrac{I_S}{\beta_R} \end{cases}\right\}$$

Assume further $e^{\frac{V_{BE}}{V_T}} \gg 1 + \dfrac{\beta_F}{\beta_R}$ (thus excluding very small currents)

$$\boxed{\begin{array}{l} \left.\begin{cases} I_B \cong \dfrac{I_S e^{\frac{V_{BE}}{V_T}}}{\beta_F} \\[2ex] I_C \cong I_S e^{\frac{V_{BE}}{V_T}} \end{cases}\right\} \text{ approx. eqs that will be used henceforth in the } \underline{\text{forward active region}} \\[3ex] I_C = \beta_F I_B \end{array}}$$

The Input Characteristics

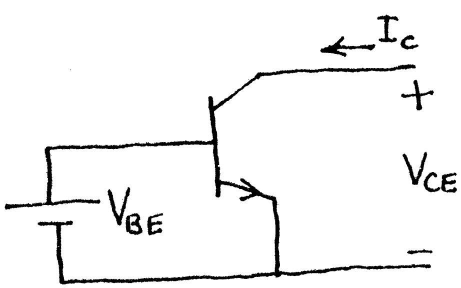




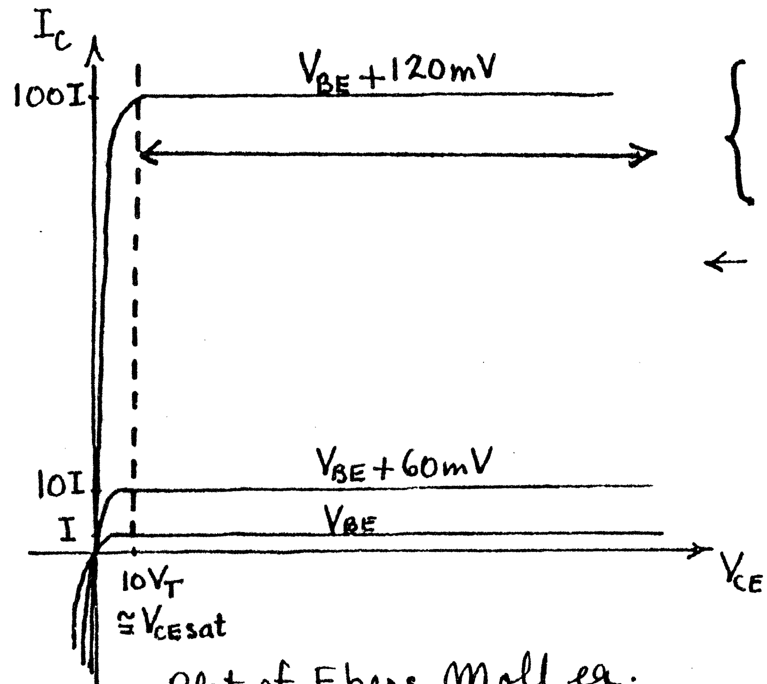
These characteristics are also temperature dependent: approx. −2mV/°C at constant I_B.

The Output Characteristics

V_{BE} held constant



$$I_c = I_s e^{\frac{V_{BE}}{V_T}} \text{ (forward active region)}$$



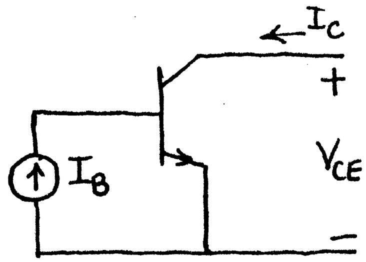
Plot of Ebers-Moll eq.

Forward active region
$$I_c = I_s e^{\frac{V_{BE}}{V_T}}$$

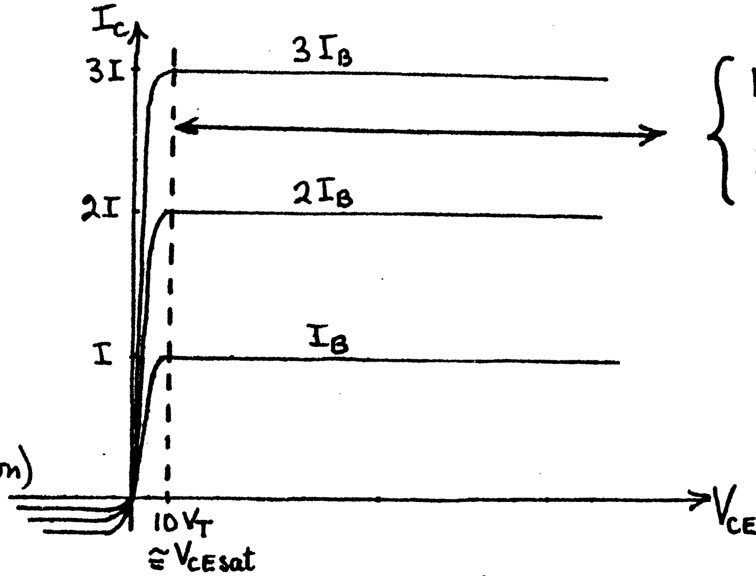
← Note uneven spacing on linear I_c scale

I_c	V_{BE}: $I_s=10^{-15}$	V_{BE}: $I_s=10^{-14}$
1μA	539mV	479mV
100μA	659mV	599mV
10mA	778mV	718mV

I_B held constant



$I_C = \beta_F I_B$ (forward active region)



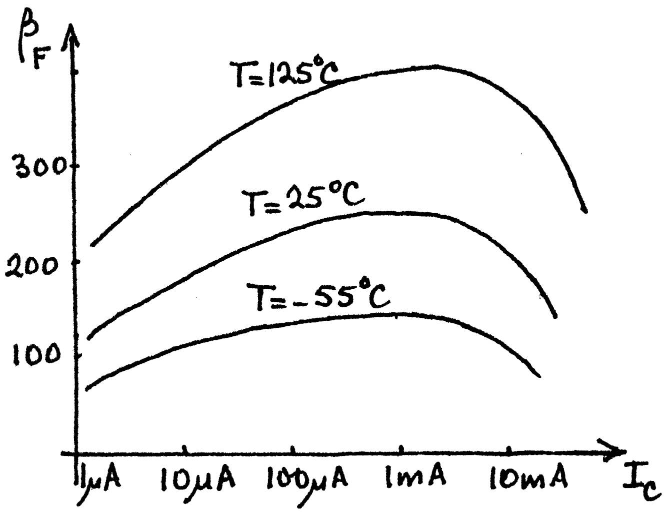
Plot of Ebers-Moll eq.

Forward active region
$I_C = \beta_F I_B$

β_F is the most important parameter

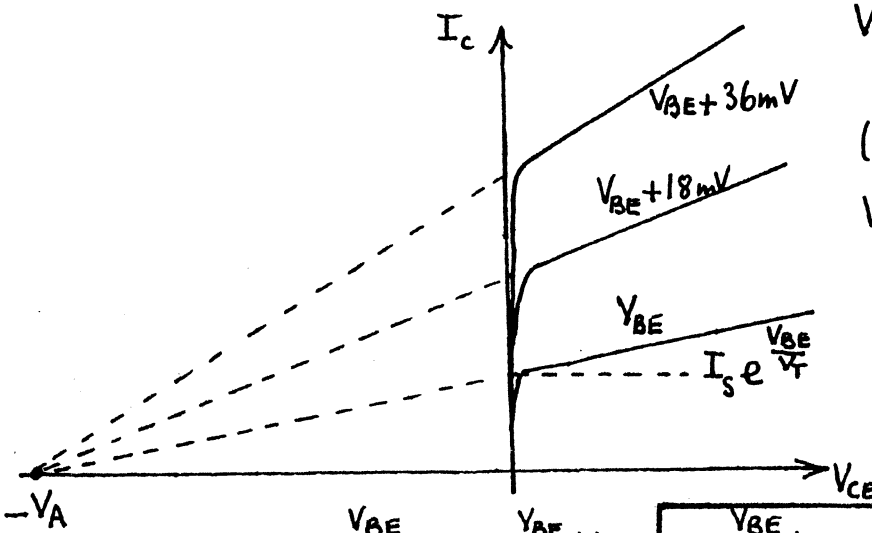
Note even spacing

The actual transistor



β_F depends on I_C and temp. (7000 ppm/°C)

Nonetheless, β_F will be assumed constant.



V_A = Early Voltage (indep. of temp.)

V_A = 50–130V

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} + I_S e^{\frac{V_{BE}}{V_T}} \frac{V_{CE}}{V_A} = \boxed{I_S e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE}}{V_A}\right)}$$

$$\boxed{I_C = \beta_F I_B\left(1+\frac{V_{CE}}{V_A}\right)}$$

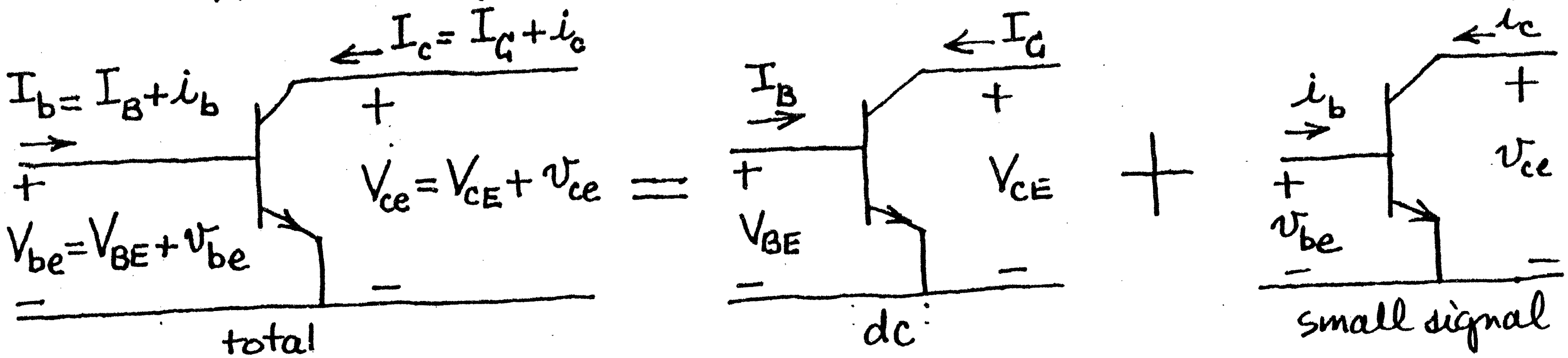
L2: Small-Signal Equivalent Circuit

Signal Notation

dc : upper-case symbol with upper-case subscript – I_B, V_{CE}

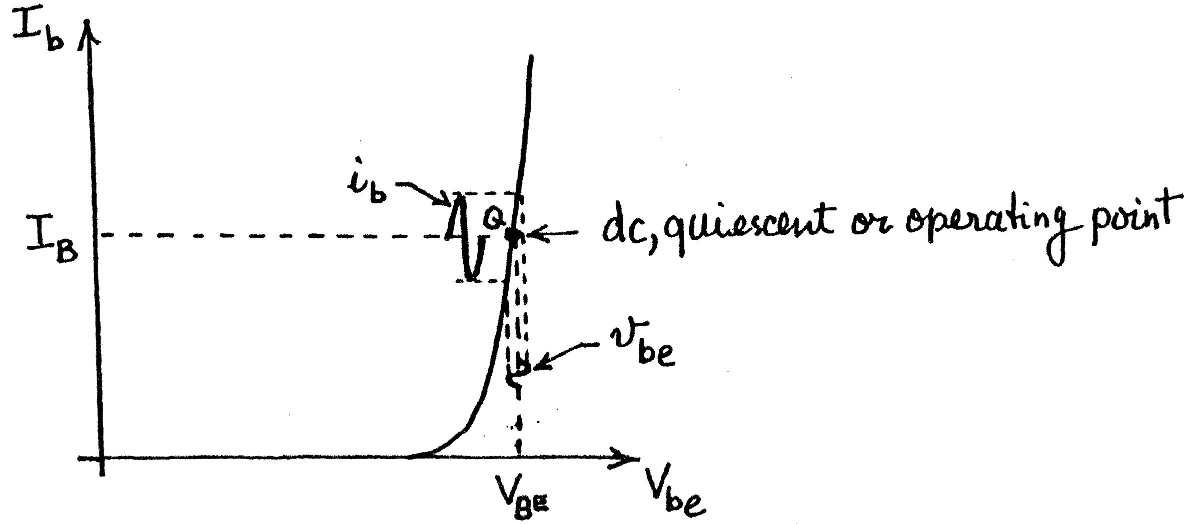
small signal: lower-case symbol with lower-case subscript – i_b, v_{ce}

total : upper-case symbol with lower-case subscript – I_b, V_{ce}



Input Model

1. Graphical



2. Mathematical Model

In the forward active region $I_b = \frac{I_s}{\beta_F} e^{\frac{V_{be}}{V_T}}$. We also know that $I_b = I_B + i_b$.

Since $V_{be} = V_{BE} + v_{be}$ and $e^x \cong 1 + x$ for $|x| \ll 1$, we can write

$$I_b = \frac{I_s}{\beta_F} e^{\frac{V_{BE}+v_{be}}{V_T}} = \frac{I_s}{\beta_F} e^{\frac{V_{BE}}{V_T}} e^{\frac{v_{be}}{V_T}} \cong \frac{I_s e^{\frac{V_{BE}}{V_T}}}{\beta_F}\left(1 + \frac{v_{be}}{V_T}\right) \quad \text{for } \left|\frac{v_{be}}{V_T}\right| \ll 1.$$

Even for $v_{be} = 10\text{mV}$, the approx. value given by $\left(1 + \frac{v_{be}}{V_T}\right) = 1 + \frac{10}{26} = 1.38$ is within 6% of the exact value given by $e^{\frac{v_{be}}{V_T}} = e^{\frac{10}{26}} = 1.47$. So for small signals, $|v_{be}| \leq 10\text{mV}$,

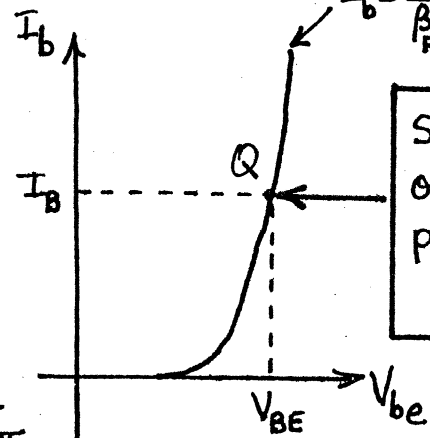
$$I_b = \frac{I_s e^{\frac{V_{BE}}{V_T}}}{\beta_F} + \frac{v_{be}}{\frac{\beta_F V_T}{I_s e^{\frac{V_{BE}}{V_T}}}} = I_B + \underbrace{\frac{v_{be}}{r_\pi}}_{i_b} \quad \text{where } \boxed{I_B = \frac{I_s e^{\frac{V_{BE}}{V_T}}}{\beta_F}} \text{ and } \boxed{r_\pi = \frac{\beta_F V_T}{I_s e^{\frac{V_{BE}}{V_T}}} = \frac{V_T}{I_B}}$$

What is r_π?

$$I_b = \frac{I_s}{\beta_F} e^{\frac{V_{be}}{V_T}}$$

$$\frac{dI_b}{dV_{be}} = \left.\frac{I_s e^{\frac{V_{be}}{V_T}}}{\beta_F V_T}\right|_{V_{be}=V_{BE}}$$

$$\frac{dI_b}{dV_{be}} = \frac{I_s e^{\frac{V_{BE}}{V_T}}}{\beta_F V_T} = \frac{I_B}{V_T} = \frac{1}{r_\pi}$$



$I_b = \frac{I_s}{\beta_F} e^{\frac{V_{be}}{V_T}}$

Slope at operating point is $\frac{1}{r_\pi}$

$$r_\pi = \frac{\beta_F V_T}{I_s e^{\frac{V_{BE}}{V_T}}} = \frac{V_T}{I_B}$$

r_π Varies with operating point

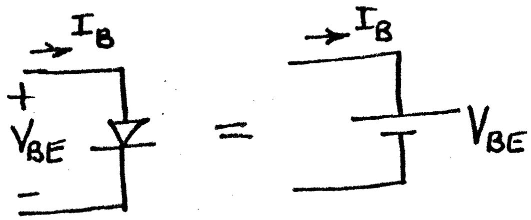
At room temp.

$$r_\pi = \frac{V_T}{I_B} = \frac{26 \times 10^{-3}}{I_B}\,\Omega = \frac{26 \times 10^{-3}}{I_{B\mu A} \times 10^{-6}}\,\Omega$$

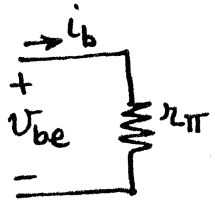
$$r_\pi = \frac{26 \times 10^{3}}{I_{B\mu A}}\,\Omega = \boxed{\frac{26}{I_{B\mu A}}\,\text{K}\Omega}$$

3. Circuit Model

dc model
$$\begin{cases} I_B = \dfrac{I_S}{\beta_F} e^{\frac{V_{BE}}{V_T}} \\ V_{BE} = V_T \ln \dfrac{\beta_F I_B}{I_S} \end{cases}$$



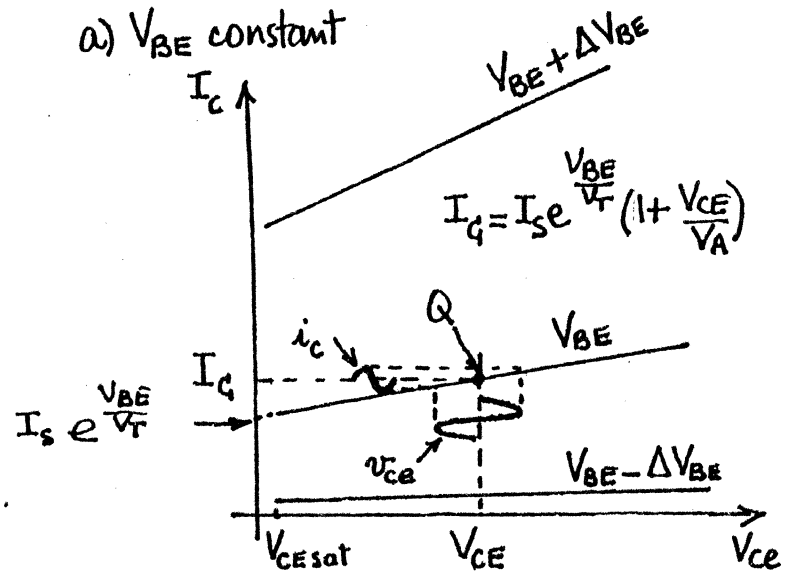
small-signal model
$$\begin{cases} i_b = \dfrac{v_{be}}{r_\pi} \\ v_{be} = i_b r_\pi \end{cases}$$



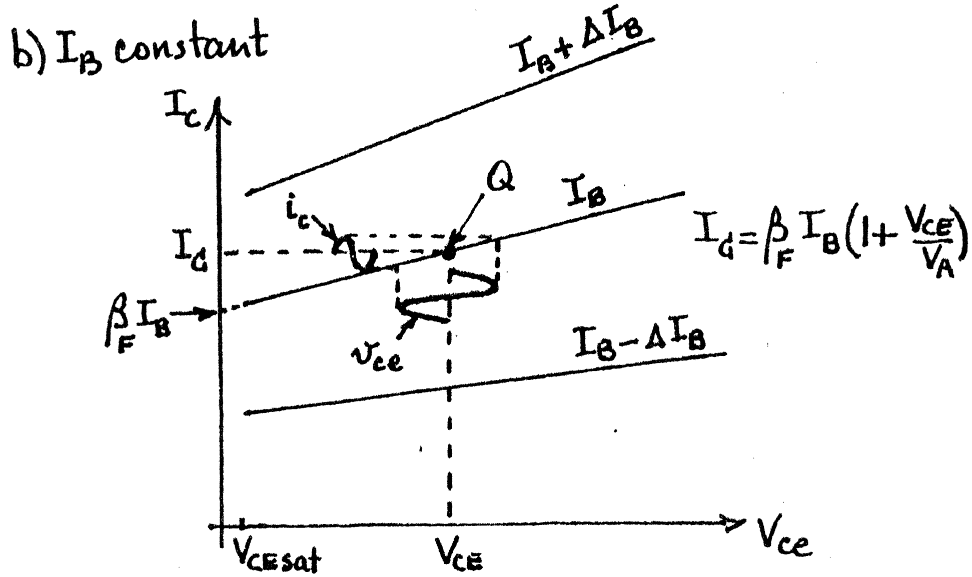
Output Model

1. Graphical

a) V_{BE} constant



b) I_B constant



2. Mathematical Model

a) In terms of changes in V_{be} and V_{ce}

In the forward active region $I_c = I_s e^{\frac{V_{be}}{V_T}}\left(1+\frac{V_{ce}}{V_A}\right) = I_Q + i_c$

$$I_c = I_s e^{\frac{V_{BE}+v_{be}}{V_T}}\left(1+\frac{V_{CE}+v_{ce}}{V_A}\right) = I_s e^{\frac{V_{BE}}{V_T}} e^{\frac{v_{be}}{V_T}}\left(1+\frac{V_{CE}}{V_A}+\frac{v_{ce}}{V_A}\right)$$

$$\cong I_s e^{\frac{V_{BE}}{V_T}}\left(1+\frac{v_{be}}{V_T}\right)\left(1+\frac{V_{CE}}{V_A}+\frac{v_{ce}}{V_A}\right)$$

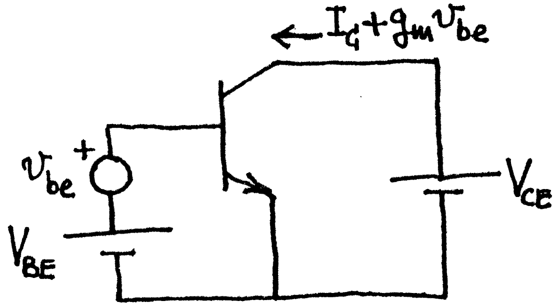
$$= I_s e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE}}{V_A}\right) + I_s e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE}}{V_A}\right)\frac{v_{be}}{V_T} + I_s e^{\frac{V_{BE}}{V_T}}\frac{v_{ce}}{V_A} + \overbrace{I_s e^{\frac{V_{BE}}{V_T}}\frac{v_{be}}{V_T}\frac{v_{ce}}{V_A}}^{\text{second-order effect; neglect this term}}$$

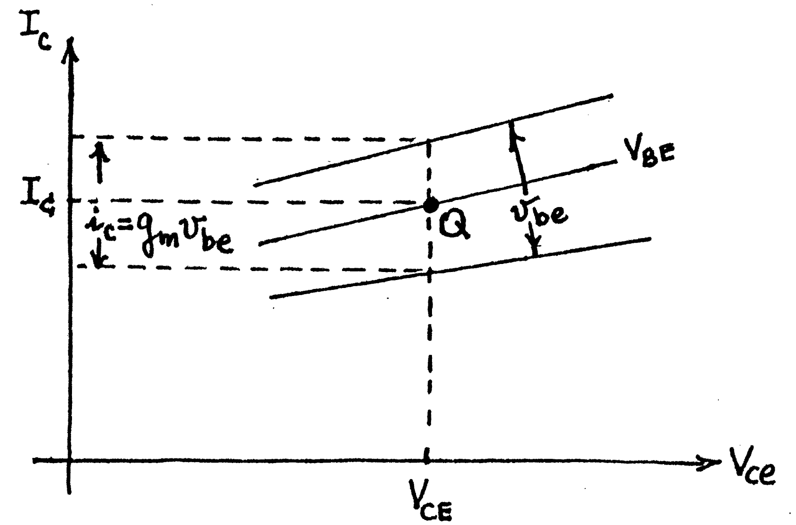
$$\cong I_Q + \underbrace{g_m v_{be} + \frac{v_{ce}}{r_o}}_{i_c} \quad \text{where} \quad \boxed{I_Q = I_s e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE}}{V_A}\right), \quad g_m = \frac{I_Q}{V_T}, \quad r_o = \frac{V_A}{I_s e^{\frac{V_{BE}}{V_T}}}}$$

What is g_m?

If $v_{ce}=0$,

$$I_c = I_Q + \underbrace{g_m v_{be}}_{i_c}$$





$$\boxed{g_m = \frac{I_C}{V_T}}$$

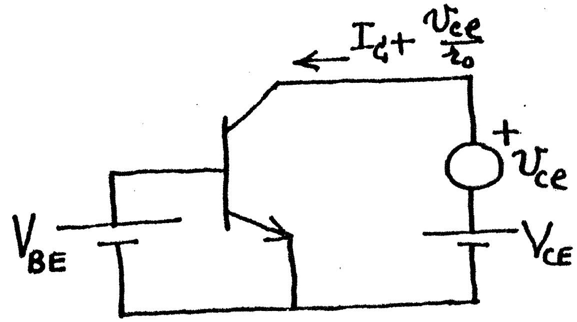
g_m varies with operating point

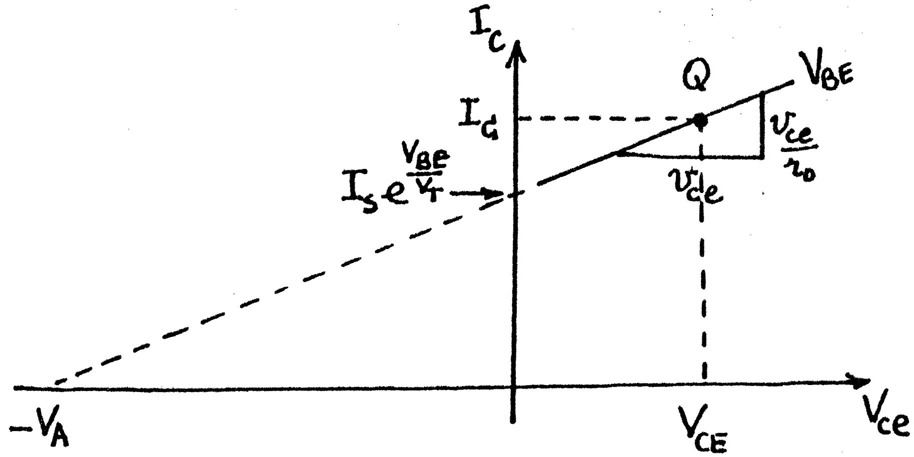
g_m is the short-circuit ($v_{ce}=0$) transconductance

What is r_o?

If $v_{be}=0$,

$$I_c = I_Q + \underbrace{\frac{v_{ce}}{r_o}}_{i_c}$$





r_o is $\frac{1}{\text{slope}}$ of output characteristic curve

$$\boxed{r_o = \frac{V_A}{I_s e^{\frac{V_{BE}}{V_T}}}} = \frac{V_A}{I_Q \text{ with } V_{CE}=0} = \boxed{\frac{V_A + V_{CE}}{I_Q}}$$

r_o varies with operating point. The higher I_Q the lower r_o.

b) In terms of changes in I_b and V_{ce}

In the forward active region $I_c = \beta_F I_b\left(1+\frac{V_{ce}}{V_A}\right) = I_Q + i_c$

$$I_c = \beta_F (I_B + i_b)\left(1+\frac{V_{CE}+v_{ce}}{V_A}\right) = \beta_F I_B\left(1+\frac{V_{CE}}{V_A}\right) + \beta_F I_B \frac{v_{ce}}{V_A} + \beta_F i_b\left(1+\frac{V_{CE}}{V_A}\right) + \overbrace{\beta_F i_b \frac{v_{ce}}{V_A}}^{\text{second-order effect neglect}}$$

$$\cong I_Q + \underbrace{\frac{v_{ce}}{r_o} + \beta_F' i_b}_{i_c} \quad \text{where} \quad \boxed{I_Q = \beta_F I_B\left(1+\frac{V_{CE}}{V_A}\right), \quad r_o = \frac{V_A}{\beta_F I_B}, \quad \beta_F' = \beta_F\left(1+\frac{V_{CE}}{V_A}\right)}$$

Comparing the a and b results we see that $I_c = \underbrace{I_Q + g_m v_{be} + \frac{v_{ce}}{r_o}}_{\text{from a}} = \underbrace{I_Q + \frac{v_{ce}}{r_o} + \beta_F' i_b}_{\text{from b}}$.

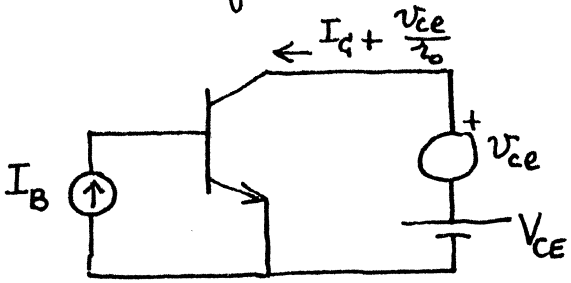
Hence $\beta_F' i_b = g_m v_{be}$

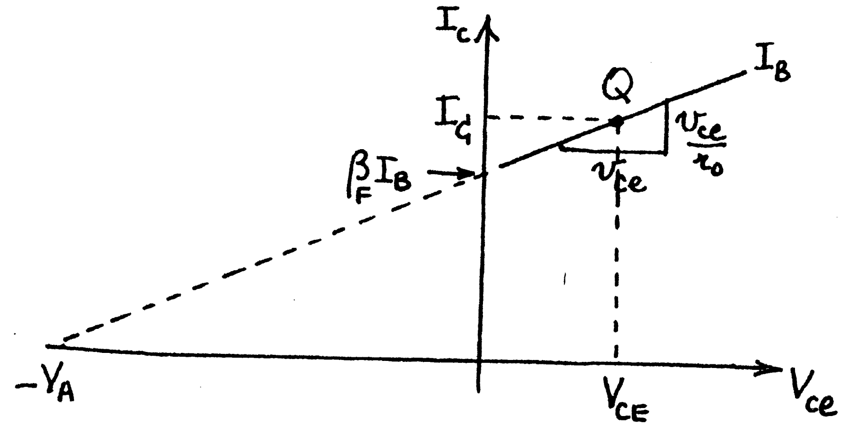
Since $v_{be} = i_b r_\pi$, $\boxed{\beta_F' = g_m r_\pi}$

What is r_o? (alternative definition)

If $i_b = 0$,

$$I_c = \underbrace{I_Q + \frac{v_{ce}}{r_o}}_{i_c}$$





$$\boxed{r_o = \frac{V_A}{\beta_F I_B} = \frac{V_A + V_{CE}}{I_Q}}$$

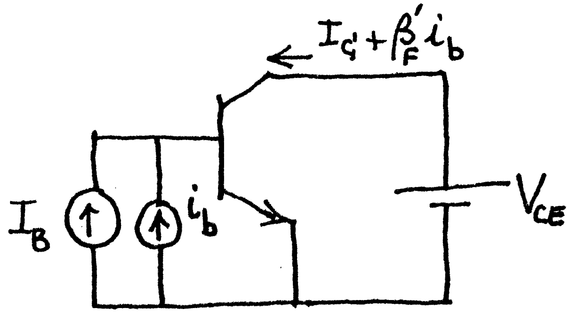
r_o is $\frac{1}{\text{slope}}$ of output characteristic curve

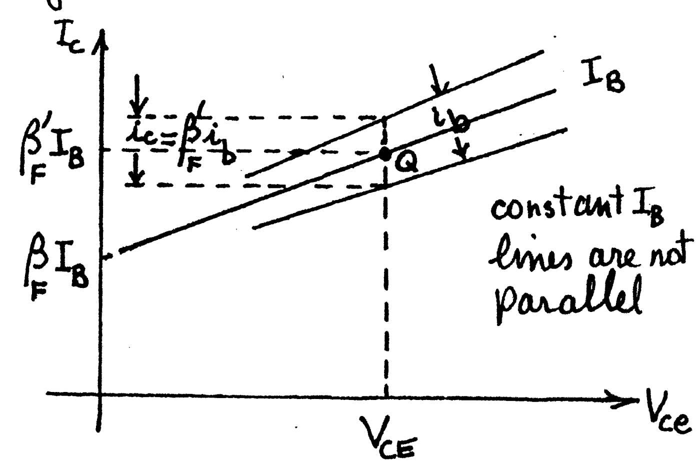
It is worth repeating: r_o varies with operating point.

What is β'_F?

If $v_{ce} = 0$,

$$I_c = \underbrace{I_Q + \beta'_F i_b}_{i_c}$$





$$\boxed{\beta'_F = \beta_F \left(1 + \frac{V_{CE}}{V_A}\right)}$$

$\beta'_F = \beta_F$ if $V_{CE} = 0$.

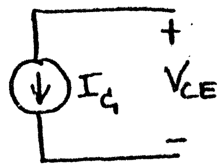
β'_F is the short-circuit ($v_{ce} = 0$) current gain

Henceforth the symbol β will be used to designate β'_F.

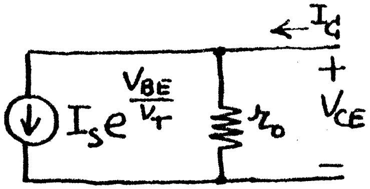
β_F "does not" depend on operating point. β'_F does because constant I_B lines are not parallel.

3. Circuit Model

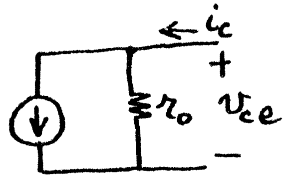
dc model : $I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_A}\right)$



or $I_C = I_S e^{\frac{V_{BE}}{V_T}} + \frac{V_{CE}}{r_o}$

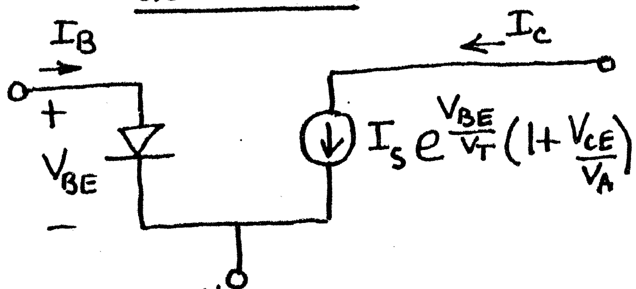


small-signal model: $i_c = g_m v_{be} + \frac{v_{ce}}{r_o} = \beta i_b + \frac{v_{ce}}{r_o}$



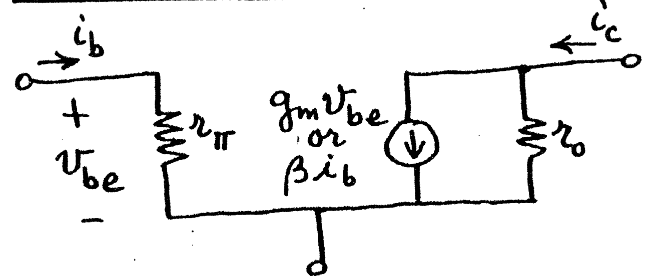
The complete model

dc model



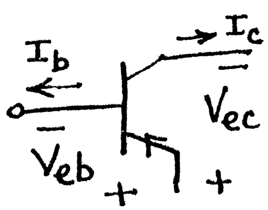
$I_B = \frac{I_S}{\beta_F} e^{\frac{V_{BE}}{V_T}}$

small-signal model

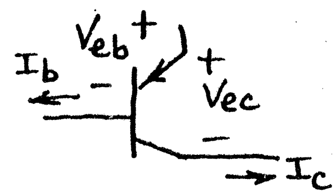


Low frequency hybrid-π model

Convention to be used for PNP transistor

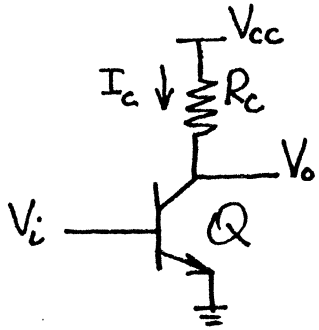


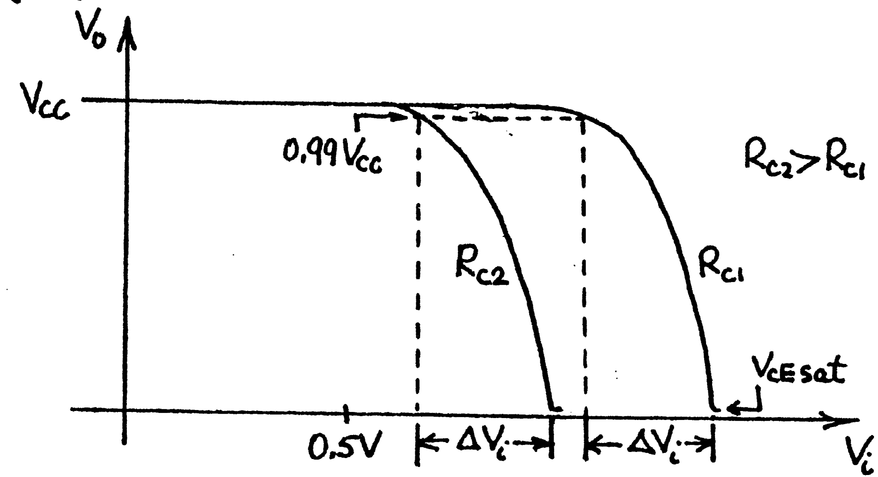
or



L3: The Common-Emitter Amplifier with Resistive Load

Simplified Analysis (Ignoring Early effect, i.e., $r_o = \infty$)





$$V_o = V_{CC} - R_C I_C$$

$$I_c = I_S e^{\frac{V_i}{V_T}}$$

$$\boxed{V_o = V_{CC} - R_C I_S e^{\frac{V_i}{V_T}}} \qquad V_{CEsat} \le V_o \le V_{CC}$$

This equation is not valid for very small currents because $(e^{\frac{V_i}{V_T}} - 1)$ has been replaced by $e^{\frac{V_i}{V_T}}$.

How much ΔV_i does it take to drive the output from $0.99V_{CC}$ to $0.01V_{CC}$?

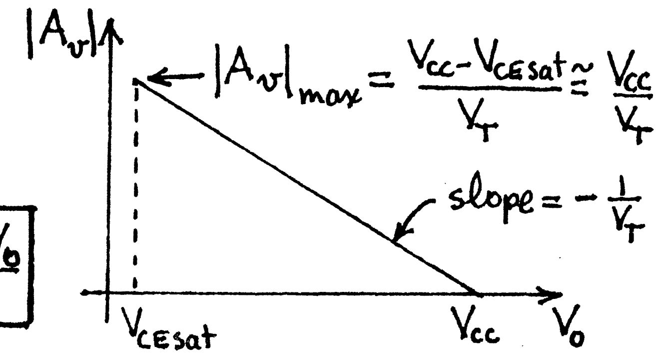
$$\left\{\begin{array}{l} 0.99V_{CC} = V_{CC} - R_C I_S e^{\frac{V_i}{V_T}} \\ 0.01V_{CC} = V_{CC} - R_C I_S e^{\frac{V_i + \Delta V_i}{V_T}} \end{array}\right\} \quad \begin{array}{l} \Delta V_i = V_T \ln 99 \\ \cong 120\text{mV} \end{array}$$

Independent of V_{CC} and R_C, it takes 120mV.

What is the small-signal gain?

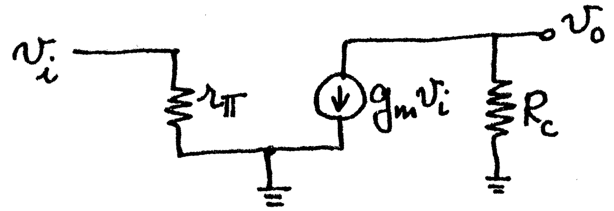
Find the slope of the V_o vs V_i curve.

$$\text{Small-signal gain} = \frac{dV_o}{dV_i} = A_v = -\frac{R_C I_S e^{\frac{V_i}{V_T}}}{V_T} = \boxed{-\frac{V_{CC} - V_o}{V_T}}$$



Alternative Derivation of small-signal gain

Use the small-signal model



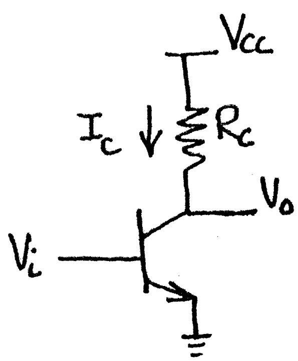
$$v_o = -g_m v_i R_c$$

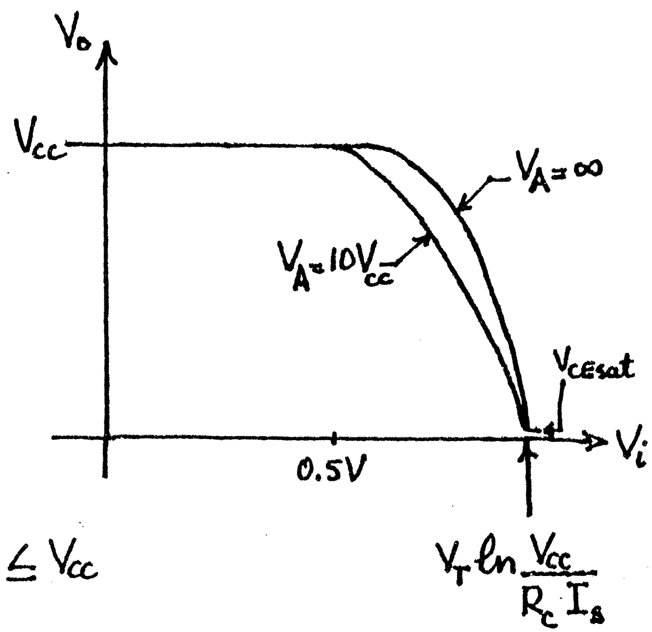
$$A_v = \frac{v_o}{v_i} = \boxed{-g_m R_c = -\frac{I_C}{V_T} R_c}$$

$|A_v|_{max}$ occurs when $I_C = I_{C\,max}$ which occurs when the transistor is sat.

$$|A_v|_{max} = \frac{I_{C\,max}}{V_T} R_c = \frac{V_{CC} - V_{CEsat}}{V_T} \cong \boxed{\frac{V_{CC}}{V_T}}$$

More exact analysis (Including the Early effect)





ΔV_i to drive V_o from $0.99V_{CC}$ to $0.01V_{CC}$:

$$\Delta V_i = V_T \ln\left[99\left(\frac{0.99V_{CC} + V_A}{0.01V_{CC} + V_A}\right)\right]$$

For $V_{CC} = 15V$, $V_A = 120V$

$$\Delta V_i = 123\,mV$$

$$V_o = V_{CC} - R_c I_c = V_{CC} - R_c I_S e^{\frac{V_i}{V_T}}\left(1 + \frac{V_o}{V_A}\right)$$

$$\boxed{V_o = V_{CC}\,\frac{1 - \frac{R_c I_s}{V_{CC}} e^{\frac{V_i}{V_T}}}{1 + \frac{R_c I_s}{V_A} e^{\frac{V_i}{V_T}}}}$$

$V_{CEsat} \leq V_o \leq V_{CC}$

Small-signal gain as a function of operating point

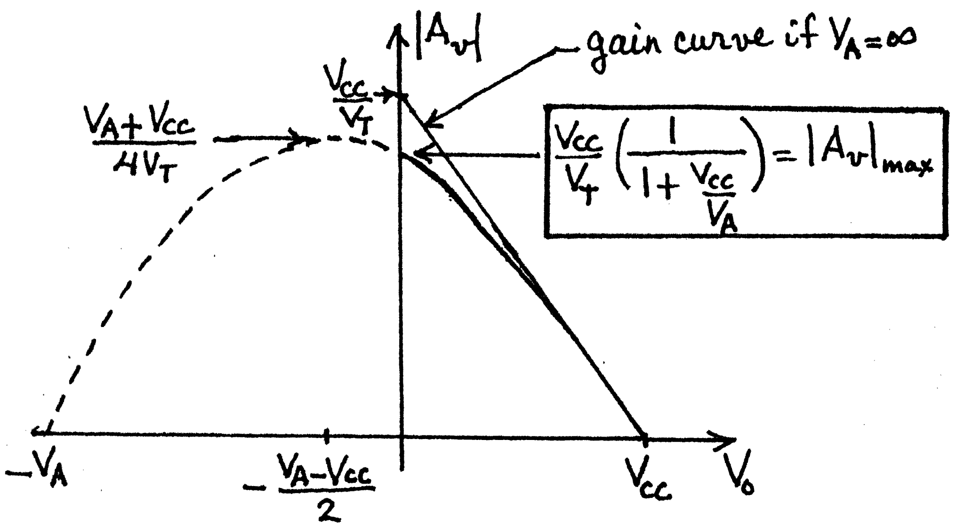
$$A_v = \frac{dV_o}{dV_i} = -\frac{R_c I_s e^{\frac{V_i}{V_T}}}{V_T}\left[\frac{1+\frac{V_{cc}}{V_A}}{\left(1+\frac{R_c I_s}{V_A}e^{\frac{V_i}{V_T}}\right)^2}\right]$$

Since $R_c I_s e^{\frac{V_i}{V_T}}\left(1+\frac{V_o}{V_A}\right) = V_{cc}-V_o$, we obtain

$$\boxed{A_v = -\frac{(V_{cc}-V_o)(V_A+V_o)}{V_T(V_A+V_{cc})}}$$

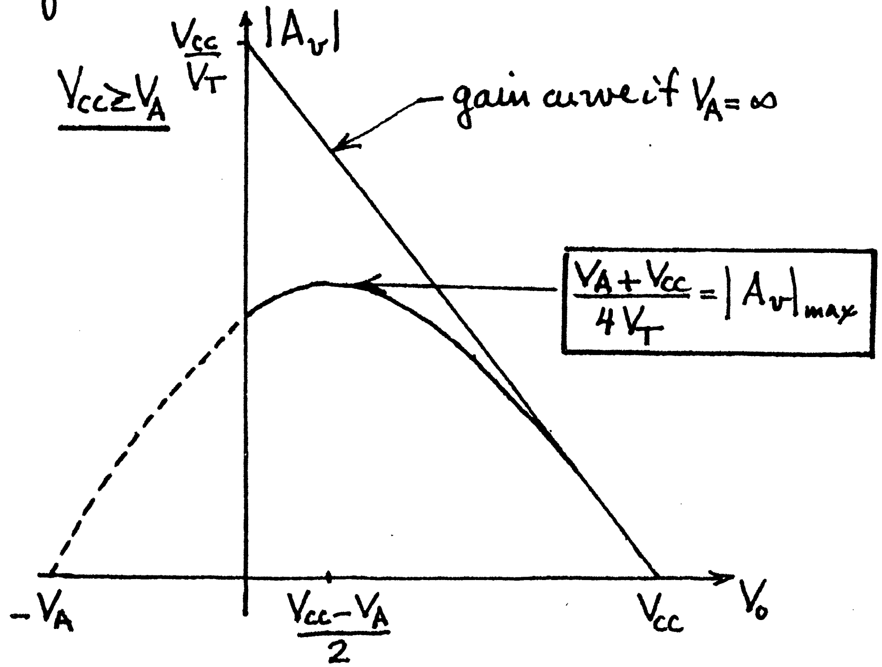
The A_v vs. V_o curve is a parabola with center at $V_o = \frac{V_{cc}-V_A}{2}$. Therefore two cases are of interest: $V_{cc} \le V_A$ and $V_{cc} \ge V_A$.

$V_{cc} \le V_A$ (the usual case)



$|A_v|_{max}$ occurs at sat.

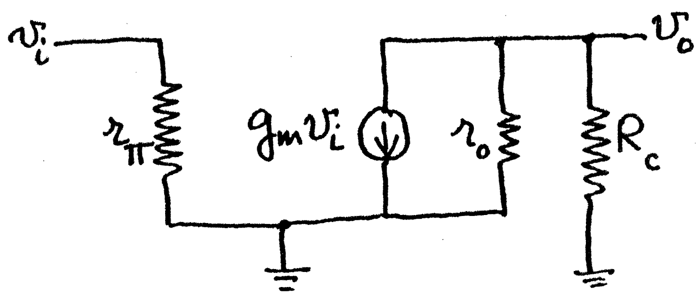
$V_{cc} \ge V_A$



$|A_v|_{max}$ occurs at $\frac{V_{cc}-V_A}{2}$

In either case $|A_v|$ is less than predicted by the tangent drawn to the parabola at $V_o=V_{cc}$. This tangent represents the $|A_v|$ vs. V_o curve for $V_A=\infty$. More gain is obtainable if $V_{cc} \ge V_A$.

Alternative derivation of gain using the small-signal model



$$v_o = -g_m v_i \frac{r_o R_C}{r_o + R_C} \qquad A_v = \frac{v_o}{v_i} = \boxed{-g_m \frac{r_o R_C}{r_o + R_C}}$$

To see how the gain varies with the operating point, use $g_m = \frac{I_C}{V_T}$ and $r_o = \frac{V_A + V_{CE}}{I_C} = \frac{V_A + V_{CC} - R_C I_C}{I_C}$ and obtain

$$A_v = -\frac{I_C R_C (V_A + V_{CC} - I_C R_C)}{V_T (V_A + V_{CC})} = \boxed{-\frac{(V_{CC} - V_o)(V_A + V_o)}{V_T (V_A + V_{CC})}}$$

which agrees with previous result.

<u>Example</u>: What is the gain if $V_{CC} = 15V$ and $V_A = 120V$? Choose operating point to maximize the gain. Assume small-signal operation.

$$A_v = -\frac{(V_{CC} - V_o)(V_A + V_o)}{V_T (V_A + V_{CC})} = -\frac{(15 - V_o)(120 + V_o)}{0.026\,(120 + 15)} = \boxed{-\frac{(15 - V_o)(120 + V_o)}{3.51}}$$

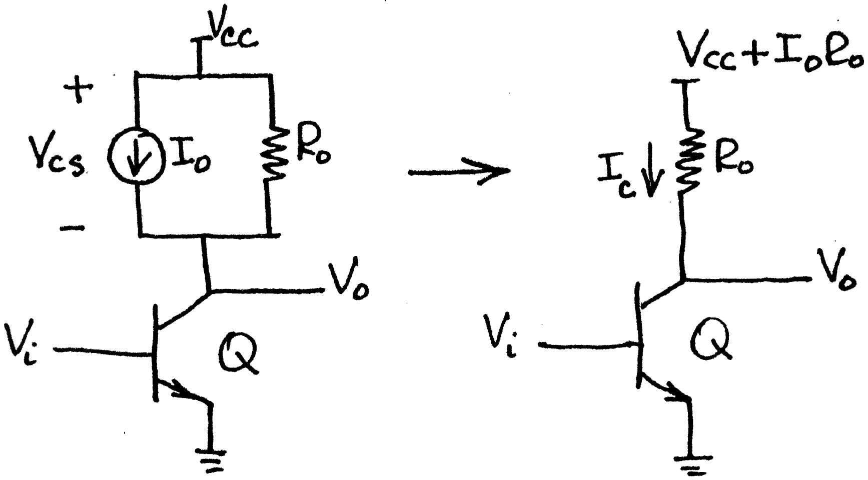
Since $V_{CC} < V_A$, maximum gain occurs at sat. So, $V_o = V_{CEsat} \cong 0$

$$A_v \cong -\frac{15 \times 120}{3.51} = \boxed{-512.8}$$

To achieve this gain, make $I_C R_C \cong 15V$.

Note that the <u>$I_C R_C$ product</u> (not the individual values of R_C and I_C) determines the gain, maximum or otherwise.

The Common-Emitter Amplifier with Current-Source Load



If $V_{CC} = 15V$, $I_o = 100\mu A$, and $R_o = 1M\Omega$, $V_{CC} + I_o R_o = 115V$.

An <u>effective</u> power supply voltage of 115V is obtained using an actual power supply voltage of only 15V.

21

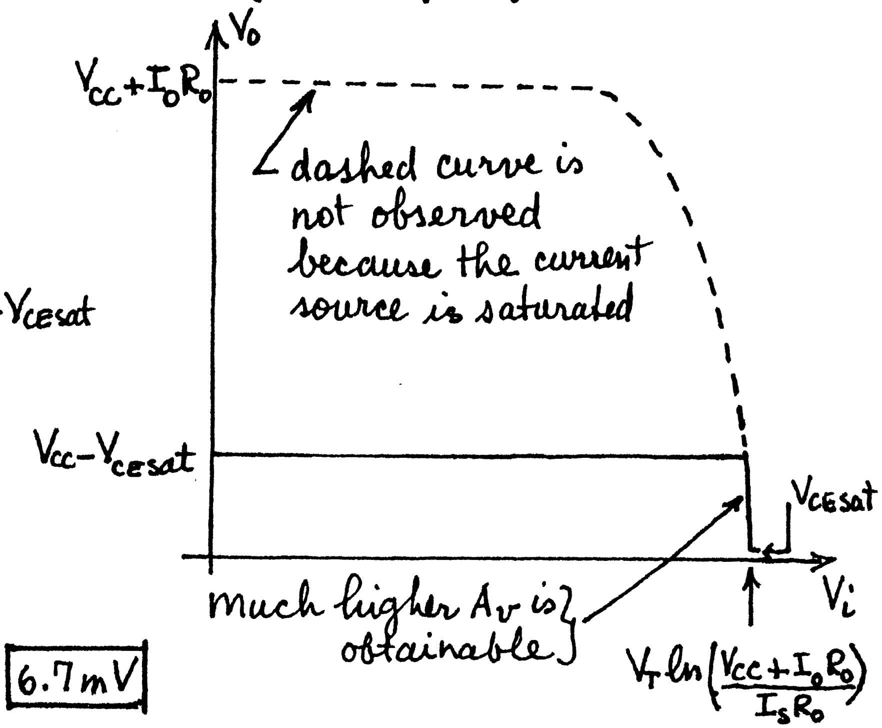
For proper operation

$V_{CS} \geq V_{CEsat}$

$$V_o = (V_{CC} + I_o R_o) - R_o I_C = (V_{CC} + I_o R_o) - R_o I_S e^{\frac{V_i}{V_T}}\left(1 + \frac{V_o}{V_A}\right)$$

$$\boxed{V_o = V_{CC}\,\frac{\left(1 + \frac{I_o R_o}{V_{CC}}\right) - \frac{I_S R_o}{V_{CC}} e^{\frac{V_i}{V_T}}}{1 + \frac{I_S R_o}{V_A} e^{\frac{V_i}{V_T}}}}$$

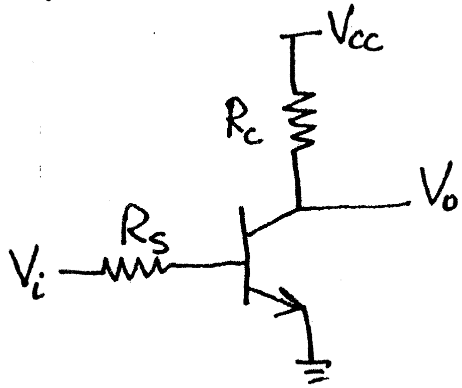
for $V_{CEsat} \leq V_o \leq V_{CC} - V_{CEsat}$

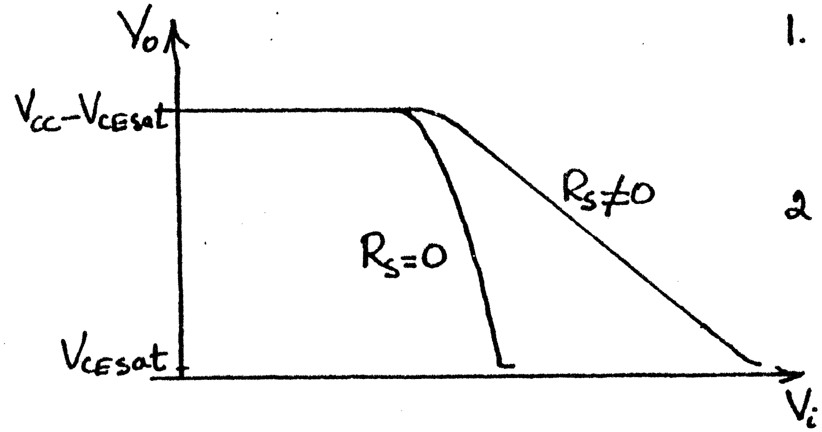


To drive V_o from $V_{CC} - V_{CEsat} \cong V_{CC}$ to $V_{CEsat} \cong 0$ requires a ΔV_i of $\boxed{\Delta V_i = V_T \ln\left[\left(1 + \frac{V_{CC}}{V_A}\right)\left(1 + \frac{V_{CC}}{I_o R_o}\right)\right]}$

For $V_{CC} = 15V$, $V_A = 120V$, $I_o = 100\mu A$, $R_o = 1M\Omega$, $\Delta V_i = \boxed{6.7mV}$

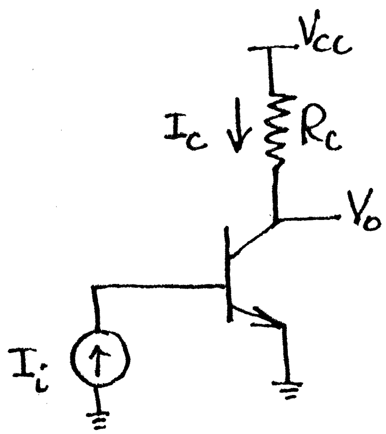
Effect of Source Resistance





1. Onset of conduction is pretty much independent of R_S.
2. The larger R_S, the more linear the V_o vs V_i curve and the smaller the incremental gain

Current Source Drive



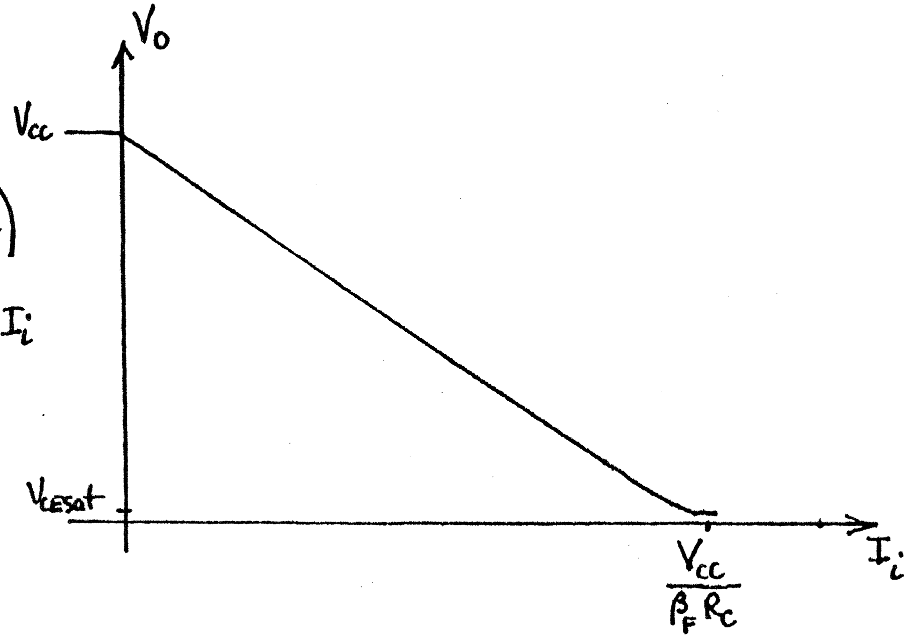
$$V_o = V_{CC} - R_C I_C$$
$$= V_{CC} - R_C I_S e^{\frac{V_i}{V_T}}\left(1+\frac{V_o}{V_A}\right)$$

But $I_S e^{\frac{V_i}{V_T}} = \beta_F I_B = \beta_F I_i$

$$V_o = V_{CC} - R_C \beta_F I_i \left(1+\frac{V_o}{V_A}\right)$$

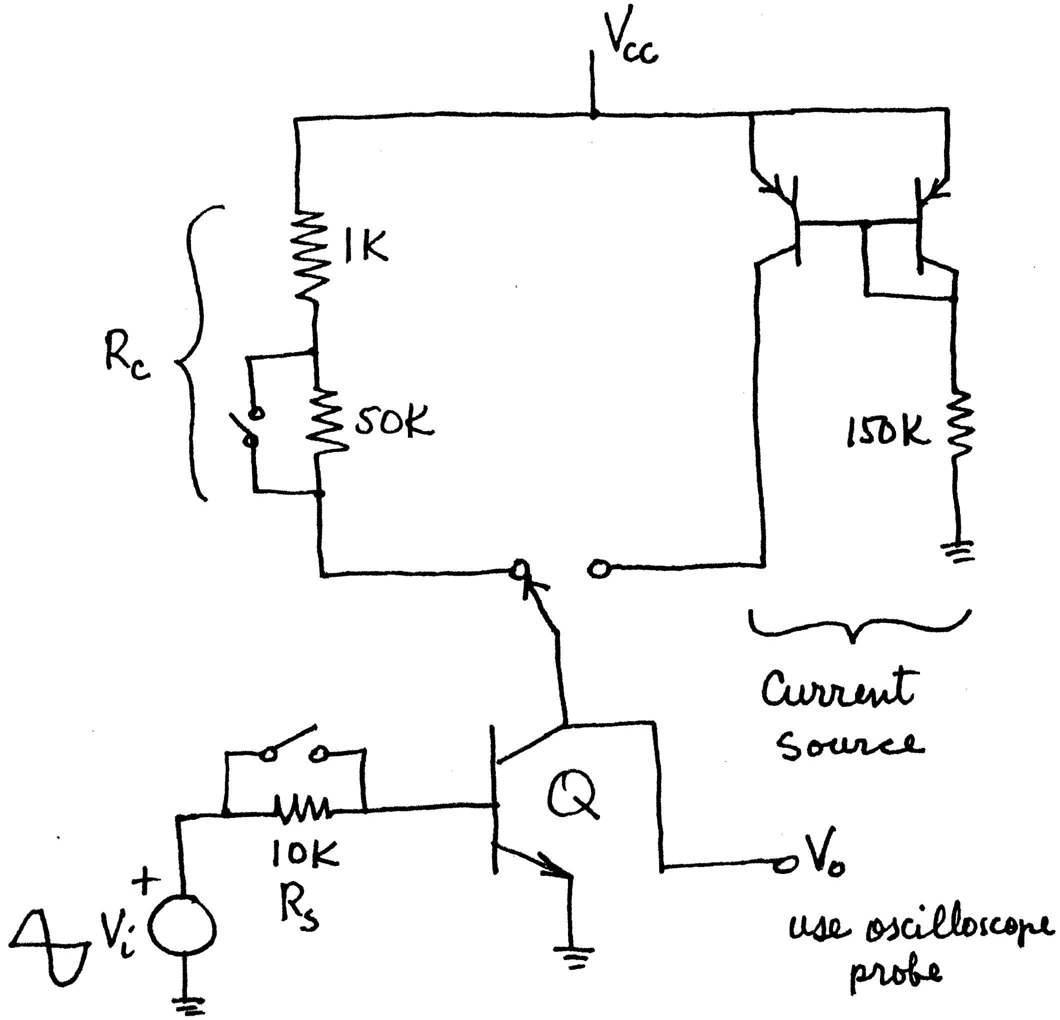
$$\boxed{V_o = V_{CC}\,\frac{1-\frac{\beta_F R_C I_i}{V_{CC}}}{1+\beta_F\frac{R_C I_i}{V_A}}}$$

$V_{CEsat} \le V_o \le V_{CC}$



For $V_A = \infty$ V_o vs I_i curve is linear with slope $-\beta_F R_C$.

Demonstration: Common-emitter Amplifier

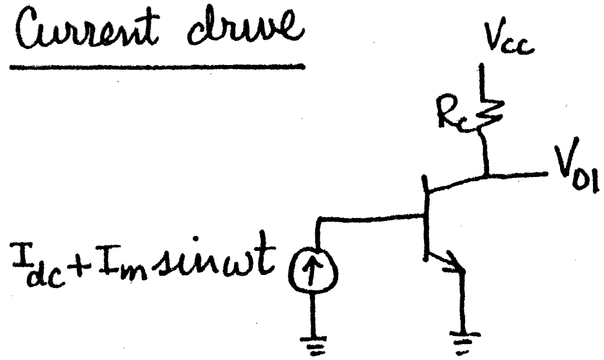


V_o vs V_i

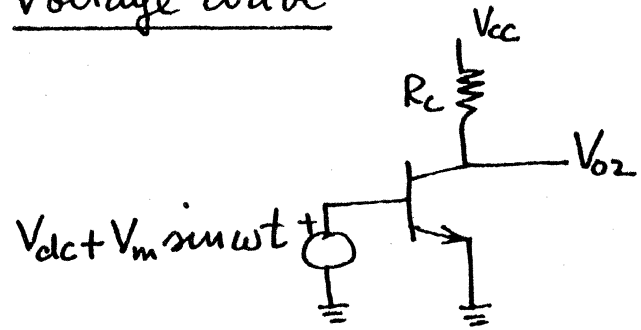
1. $R_s = 0$, $R_c = 1K$
   Vary V_{cc}
2. $R_s = 0$, $V_{cc} = 15V$
   Change R_c from 1K to 51K
3. $R_c = 1K$, $V_{cc} = 15V$
   Change R_s from 0 to 10K
4. $R_s = 0$, $V_{cc} = 15V$
   Current-source load

L4: Comparison of distortion caused by current and voltage excitations

Current drive



Voltage drive



Assume

1. $V_{O1dc} = V_{O2dc} = V_{Odc}$ (adjust I_{dc} and V_{dc} to obtain this result)
2. $V_{O1acm} = V_{O2acm} = V_{Om}$ (adjust I_m and V_m to obtain this result when output amplitude is small)
3. $V_A \gg V_{cc}$

$$V_{O1} = V_{cc} - \beta_F R_c (I_{dc} + I_m \sin\omega t)$$

$$= \underbrace{V_{cc} - \beta_F R_c I_{dc}}_{V_{Odc}} - \underbrace{\beta_F R_c I_m}_{V_{Om}} \sin\omega t$$

$$= \boxed{V_{Odc} - V_{Om} \sin\omega t}$$

$$V_{O2} = V_{cc} - R_c I_s e^{\frac{V_{dc}+V_m \sin\omega t}{V_T}}$$

$$= V_{cc} - R_c I_s e^{\frac{V_{dc}}{V_T}} e^{\frac{V_m \sin\omega t}{V_T}}$$

$$\cong V_{cc} - R_c I_s e^{\frac{V_{dc}}{V_T}} \left[1 + \frac{V_m}{V_T}\sin\omega t + \frac{1}{2}\left(\frac{V_m}{V_T}\right)^2 \sin^2\omega t\right]$$

$$= \underbrace{V_{cc} - R_c I_s e^{\frac{V_{dc}}{V_T}}}_{V_{Odc}} - \underbrace{R_c I_s e^{\frac{V_{dc}}{V_T}} \frac{V_m}{V_T}}_{V_{Om}} \sin\omega t \left(1 + \frac{1}{2}\frac{V_m}{V_T}\sin\omega t\right)$$

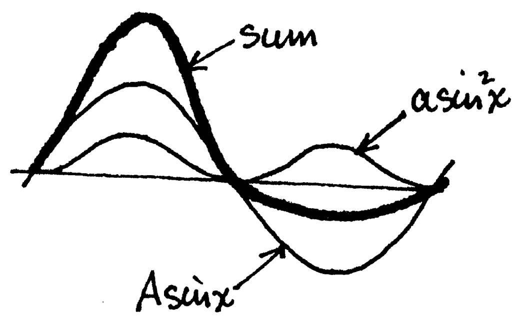
$$= \boxed{V_{Odc} - V_{Om}\sin\omega t - \frac{V_{Om}}{2}\frac{V_m}{V_T}\sin^2\omega t}$$

Assumption 1 is satisfied if $\underline{\beta_F I_{dc} = I_S e^{\frac{V_{dc}}{V_T}}} = I_C$

Assumption 2 is satisfied if $\beta_F I_m = I_S e^{\frac{V_{dc}}{V_T}} \frac{V_m}{V_T} = \frac{I_C}{V_T} V_m = g_m V_m$ which simplifies to $\underline{V_m = I_m r_\pi}$

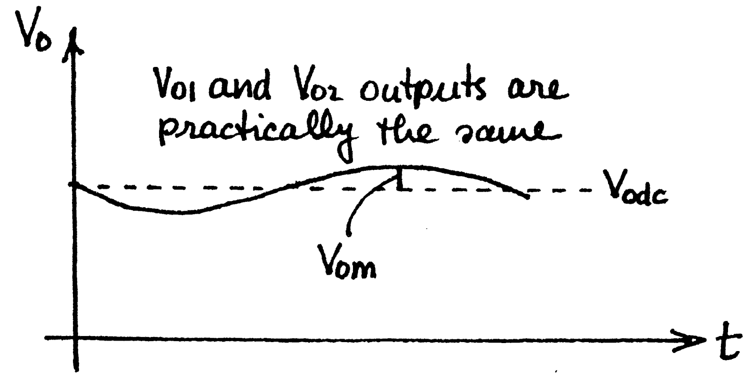
Note that $A\sin x + a\sin^2 x$

gives →

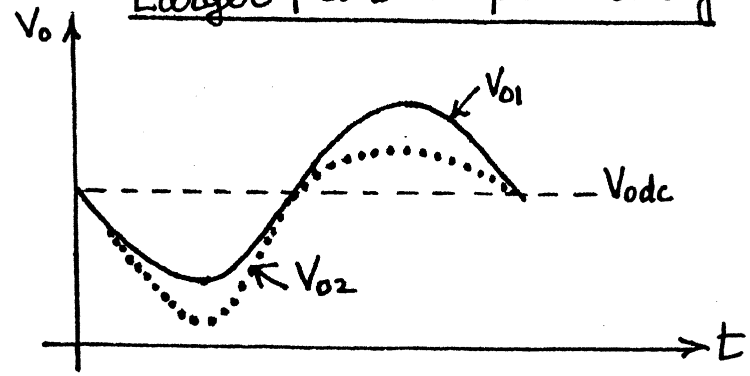


With this drawing in mind, we can now draw the V_{o1} (current-source drive) and V_{o2} (voltage-source drive) outputs for small and not so small peak-to-peak swings

Small peak-to-peak swing

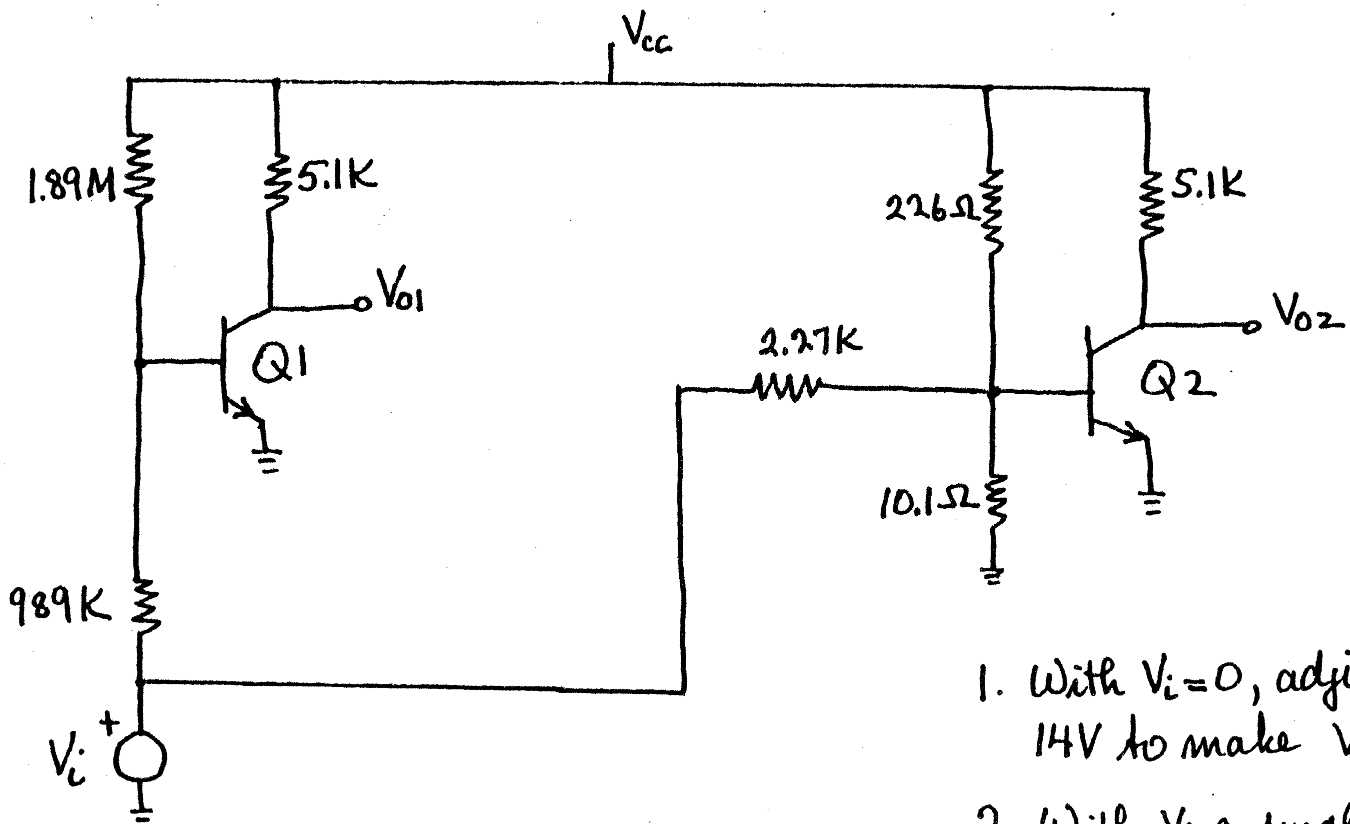


Larger peak-to-peak swing



For the same peak-to-peak output swing, the current source drive produces less distortion.

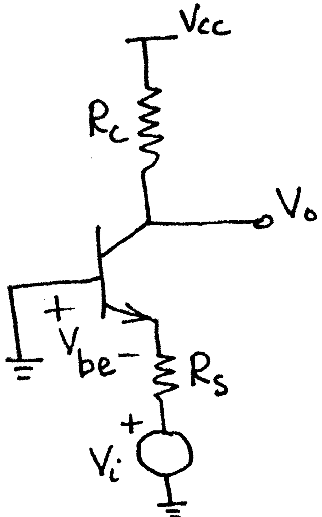
Demostration: Distortion comparison



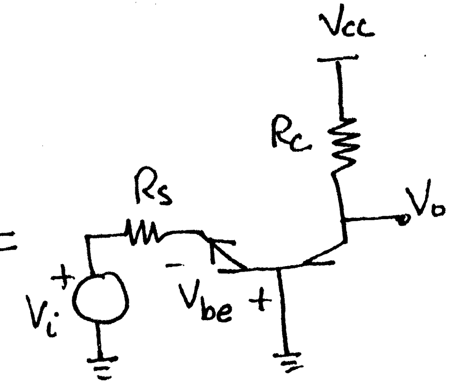
Q1 base is fed from a high resistance source (989K || 1.89M); therefore drive approximates a current source.
Q2 base is fed from a low resistance source (10.1Ω || 226Ω || 2.27K); therefore drive approximates a voltage source.

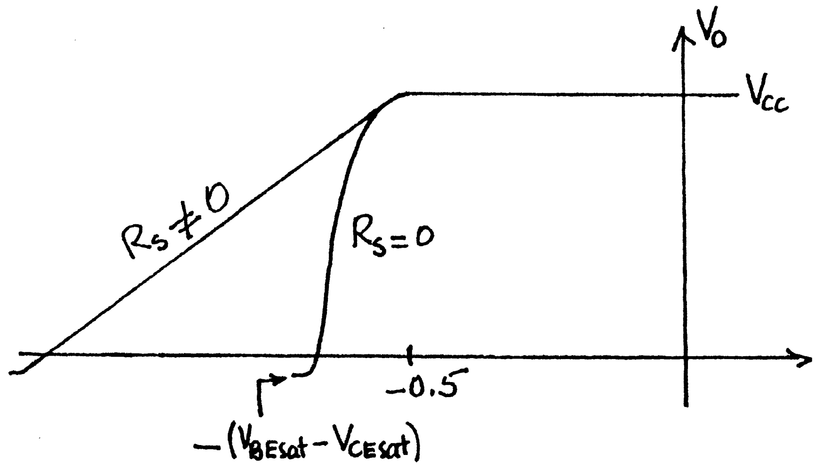
1. With $V_i = 0$, adjust V_{cc} around 14V to make $V_{O1} = V_{O2} \cong 7.5V$.
2. With V_i a small sine wave, V_{O1} and V_{O2} outputs show no noticeable distortion.
3. As V_i is increased in amplitude, the V_{O2} output starts showing noticeable distortion.

The Common-Base Amplifier



$=$



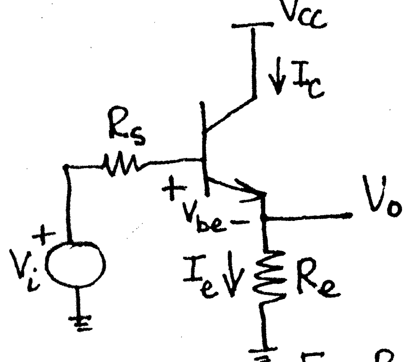


For $R_s=0$, $V_o = V_{cc} - R_c I_s e^{\frac{V_{be}}{V_T}}\left(1+\frac{V_{ce}}{V_A}\right) = V_{cc} - R_c I_s e^{-\frac{V_i}{V_T}}\left(1+\frac{V_o-V_i}{V_A}\right)$

$$\boxed{V_o = \left[\frac{1 - \frac{R_c I_s e^{-\frac{V_i}{V_T}}}{V_A}\frac{(V_A - V_i)}{V_{cc}}}{1+\frac{R_c I_s e^{-\frac{V_i}{V_T}}}{V_A}}\right] V_{cc}}$$

for $V_{CEsat} - V_{B_{sat}} \le V_o \le V_{cc}$

The Common-Collector Amplifier

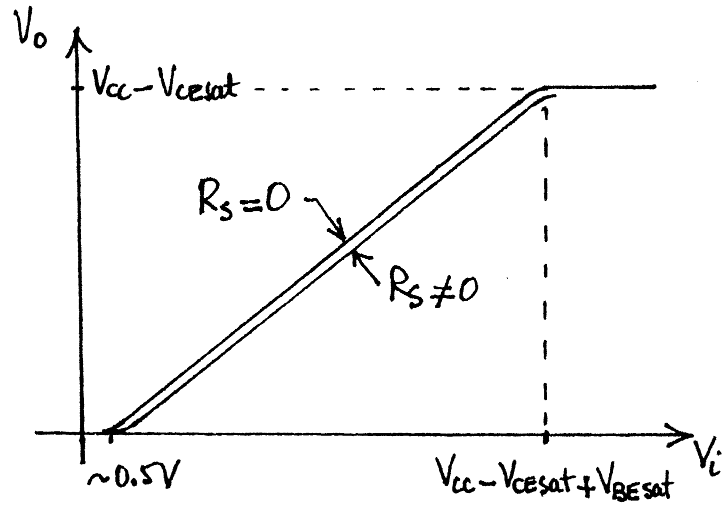


$$V_o = R_e I_e = R_e \frac{\beta_F+1}{\beta_F} I_c$$

$$= \frac{\beta_F+1}{\beta_F} R_e I_s e^{\frac{V_{be}}{V_T}}\left(1+\frac{V_{ce}}{V_A}\right)$$

For $R_s=0$, $\boxed{V_o = \frac{\beta_F+1}{\beta_F} R_e I_s e^{\frac{V_i-V_o}{V_T}}\left(1+\frac{V_{cc}-V_o}{V_A}\right)}$

for $0 \le V_o \le V_{cc} - V_{CEsat}$

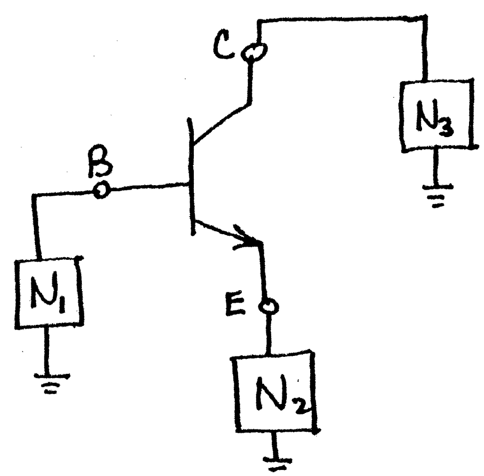


General Analysis of Resistive Transistor Circuits

Transistor circuits are analyzed with two specific objectives in mind:

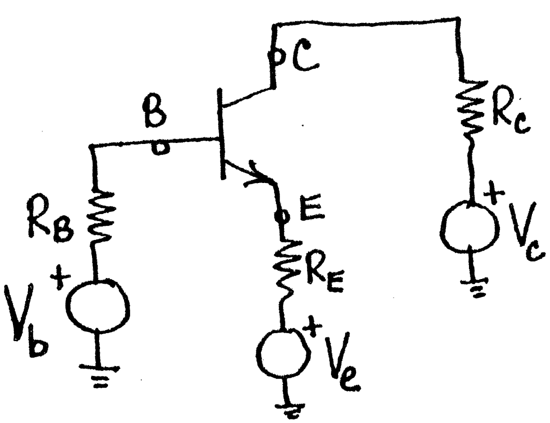
1. To determine bias values that establish the Q point
2. To calculate the small-signal gain about the Q point

A typical transistor circuit can be represented by

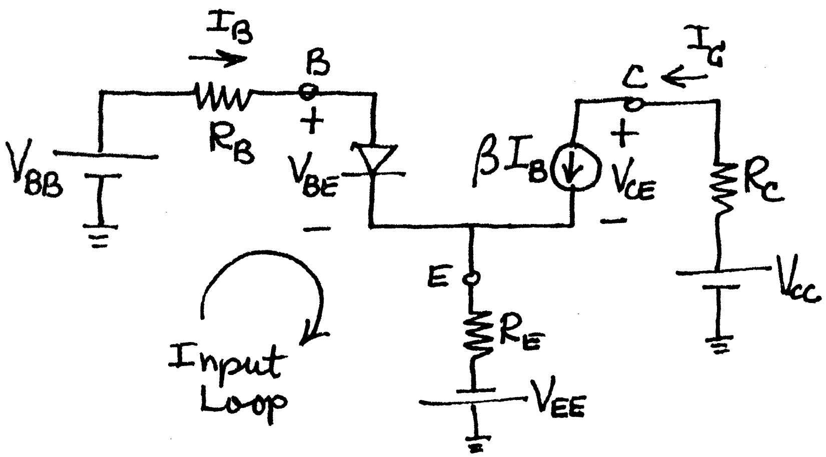


N_1, N_2, and N_3 contain resistors and independent voltage and current sources. Note that feedback between the base, collector, and emitter leads are not considered here.

The first step in the analysis is to simplify the given circuit by obtaining the Thévenin (or Norton) equivalent circuits facing the transistor between 1. base and ground 2. emitter and ground and 3. collector and ground. The result is:



<u>Operating Point Calculation</u>: Represent the transistor by the large signal model and use only the dc components of the three voltage sources.



From the sum of voltages around the input loop obtain

$$V_{BB} - I_B R_B - V_{BE} - I_B(1+\beta) R_E + V_{EE} = 0$$

$$\boxed{I_B = \frac{V_{BB} + V_{EE} - V_{BE}}{R_B + (1+\beta) R_E} \quad , \quad I_C = \beta I_B}$$

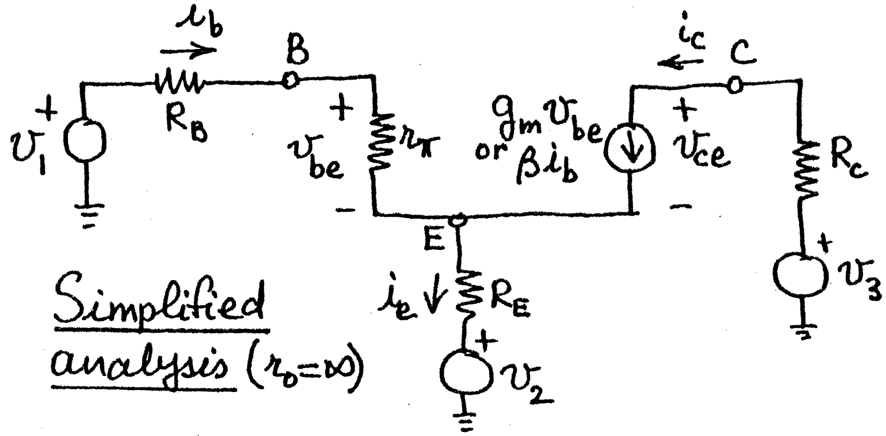
Note that in the expression for I_B and hence I_C everything is known except V_{BE}. However, we know that for Si transistors operating in the forward active region $V_{BE} = 0.6 - 0.7V$. This small uncertainity does not have any significant effect in the determination of I_B particularly when $V_{BB} + V_{EE} \gg V_{BE}$, which is the usual situation.

<u>The aim of biasing is to fix I_C such that it is practically independent of</u> β of the transistor which may vary a lot from one transistor to another. This aim can be achieved if $\beta+1 \cong \beta$ and $(1+\beta)R_E \gg R_B$, in which case I_C becomes

$$\boxed{I_C \cong \frac{V_{BB} + V_{EE} - V_{BE}}{R_E}}$$

Stated differently, if the voltage across R_B can be made negligible relative to the voltage across R_E, then I_C is fixed by V_{BB}, V_{EE}, and R_E.

Small-signal Response: Represent the transistor by the small-signal model and use only the variational components of the three input voltage sources.



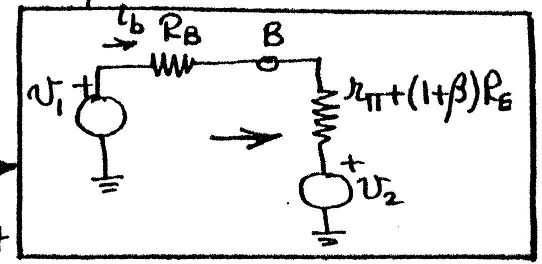
Simplified analysis ($r_o = \infty$)

Equivalent circuit facing source v_1

From the input loop we obtain

$$v_1 = i_b(R_B + r_\pi) + i_b(1+\beta)R_E + v_2$$

$$i_b = \frac{v_1 - v_2}{R_B + r_\pi + (1+\beta)R_E}$$



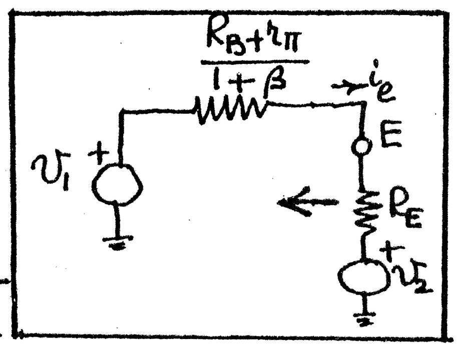
Note that v_3 has no influence on the base circuit

Equivalent circuit facing source v_2

Since $i_e = i_b(1+\beta)$, we obtain

$$i_e = \frac{(1+\beta)(v_1 - v_2)}{R_B + r_\pi + (1+\beta)R_E}$$

$$i_e = \frac{v_1 - v_2}{R_E + \dfrac{R_B + r_\pi}{1+\beta}}$$

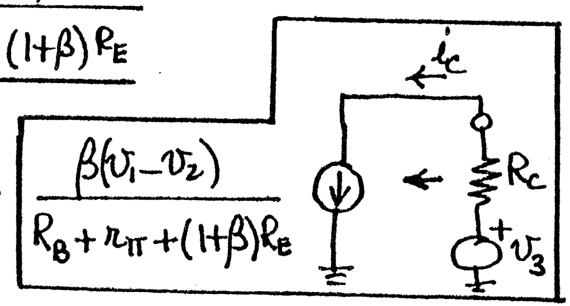


Note that v_3 has no influence on the emitter circuit

Equivalent circuit facing source v_3

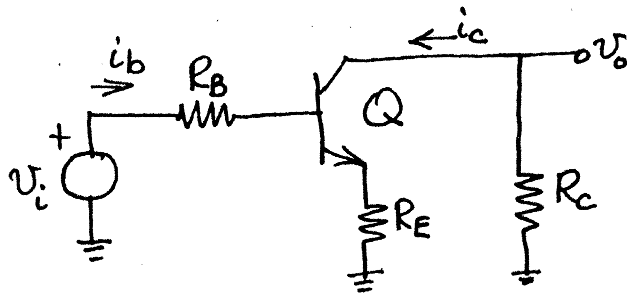
Since $i_c = \beta i_b$, we obtain

$$i_c = \frac{\beta(v_1 - v_2)}{R_B + r_\pi + (1+\beta)R_E}$$



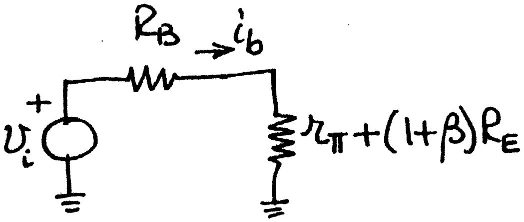
Even with R_E present, source v_3 in the collector has no influence on any of the currents.

L5: Analysis of CE Amplifier with R_B and R_E included (small signal)



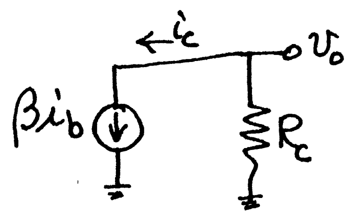
r_o assumed to be infinite

The input equivalent circuit is : v_i



Source v_i sees a high input resistance: $R_B+r_\pi+(1+\beta)R_E$

The output equivalent circuit is:



Load R_C sees an infinite output resistance

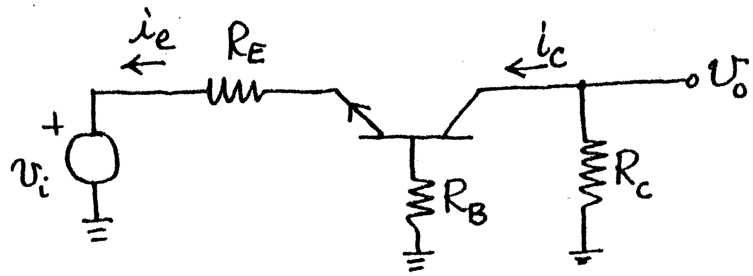
The voltage gain is: $A_v=\dfrac{v_o}{v_i}=\dfrac{-\beta i_b R_C}{v_i}=\boxed{-\dfrac{\beta R_C}{R_B+r_\pi+(1+\beta)R_E}}$

The presence of R_E reduces the gain (this is called emitter degeneration).

$|A_v|_{max}=|A_v|_{R_B=R_E=0}=+\dfrac{\beta R_C}{r_\pi}=+g_{m_{max}}R_C=\dfrac{I_{C_{max}}}{V_T}R_C\cong\dfrac{V_{CC}}{V_T}$ which occurs when Q is at sat.

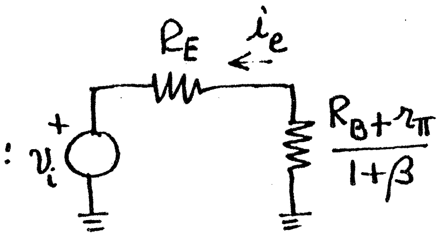
The current gain is $=\dfrac{i_c}{i_b}=\boxed{\beta}$

Analysis of CB Amplifier with R_B and R_E included (small signal)



r_o assumed to be infinite

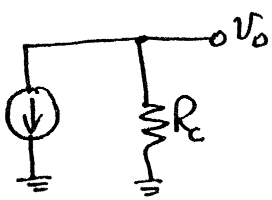
The input equivalent circuit is:



Source v_i sees a low input resistance:

$$R_E + \frac{R_B+r_\pi}{1+\beta}$$

The output equivalent circuit is:



Load R_c sees an infinite output resistance

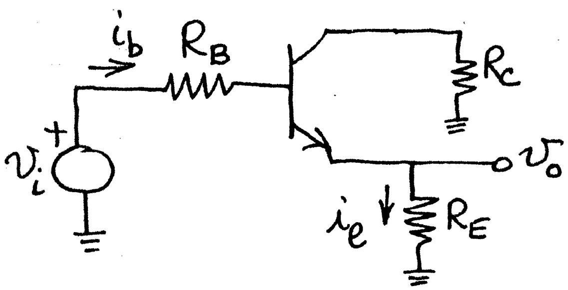
The voltage gain is: $A_v = \frac{v_o}{v_i} = \frac{-\frac{\beta}{1+\beta} i_e R_c}{-i_e\left(R_E + \frac{R_B+r_\pi}{1+\beta}\right)} = \boxed{\frac{\beta R_c}{r_\pi + R_B + (1+\beta)R_E}}$

The source and base resistances reduce the gain.

$|A_v|_{max} = |A_v|_{R_B=R_E=0} = \frac{\beta R_c}{r_\pi} = g_{m_{max}} R_c = \frac{I_{C\,max}}{V_T} R_c \cong \frac{V_{CC}}{V_T}$ which occurs when Q is at sat.

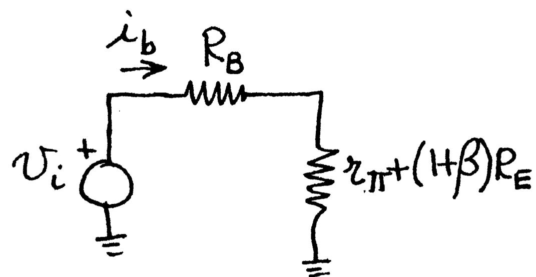
The current gain is $= \frac{i_c}{i_e} = \boxed{\frac{\beta}{1+\beta}}$

Analysis of CC Amplifier with R_B and R_E included (small signal)



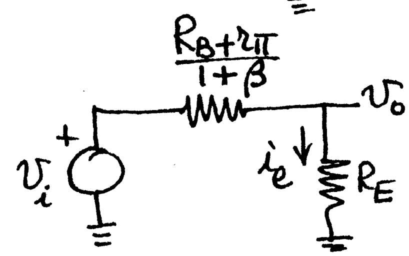
r_o assumed to be infinite

The input equivalent circuit is:



Source v_i sees a high input resistance: $r_\pi+(1+\beta)R_E$

The output equivalent circuit is:



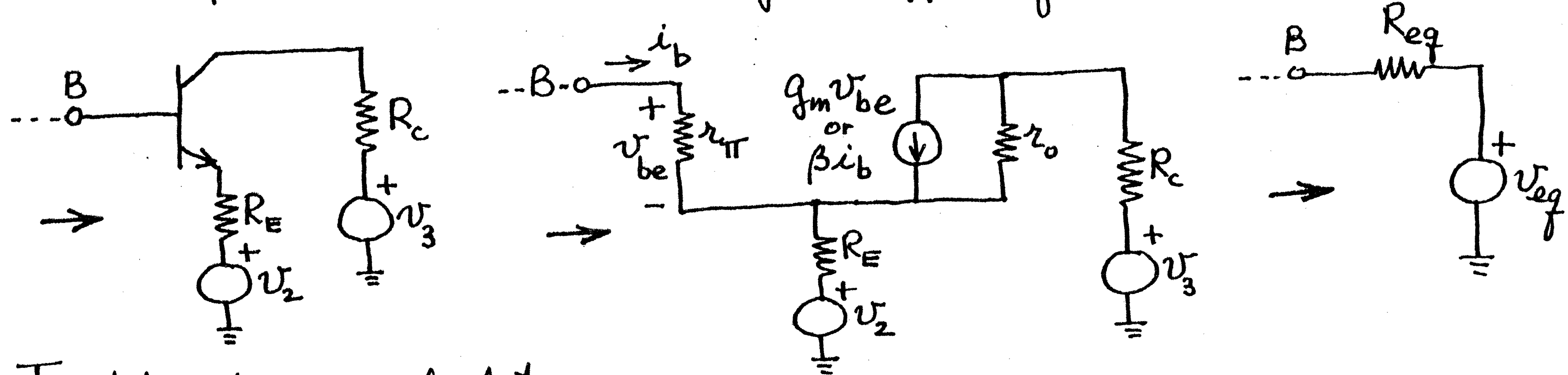
Load R_E sees a low output resistance: $\dfrac{R_B+r_\pi}{1+\beta}$

The voltage gain is $A_v=\dfrac{v_o}{v_i}=\boxed{\dfrac{R_E}{R_E+\dfrac{R_B+r_\pi}{1+\beta}}}$

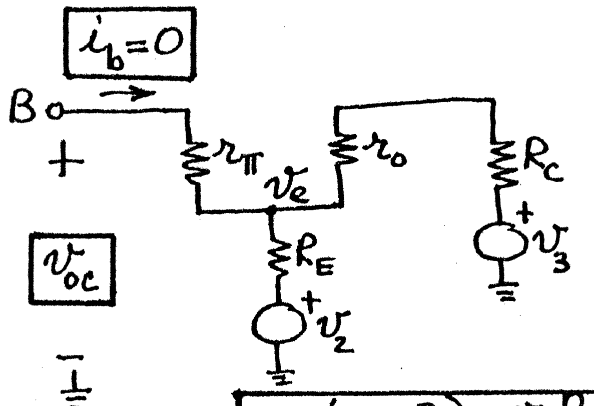
The voltage gain is less than 1. If $R_E \gg \dfrac{R_B+r_\pi}{1+\beta}$ (the usual situation), then $A_v \cong 1$.

The current gain is $\dfrac{i_e}{i_b}=\boxed{1+\beta}$

Input equivalent circuit including the effect of r_o (small signal)

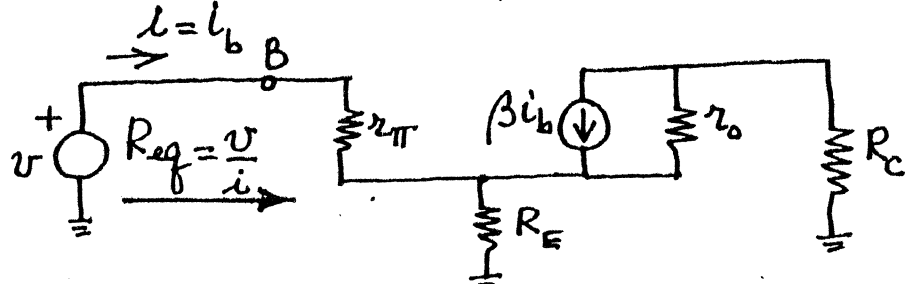


To determine v_{eq}, calculate the open-circuit voltage v_{oc} at the input.



$$v_{oc} = v_e = \boxed{\frac{v_2(r_o+R_C)+v_3 R_E}{R_E+R_C+r_o} = v_{eq}}$$

To determine R_{eq}, let $v_2 = v_3 = 0$ and calculate resistance seen at input.

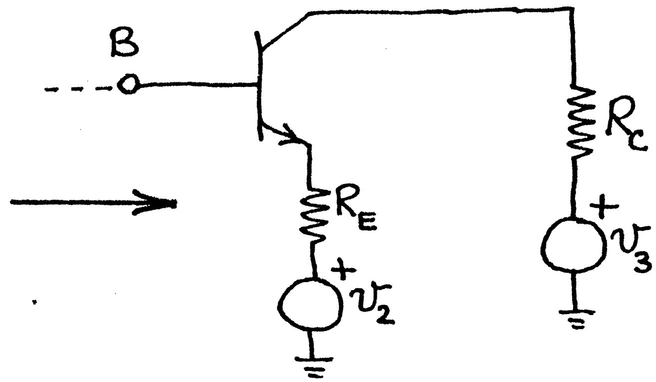


Use superposition to obtain

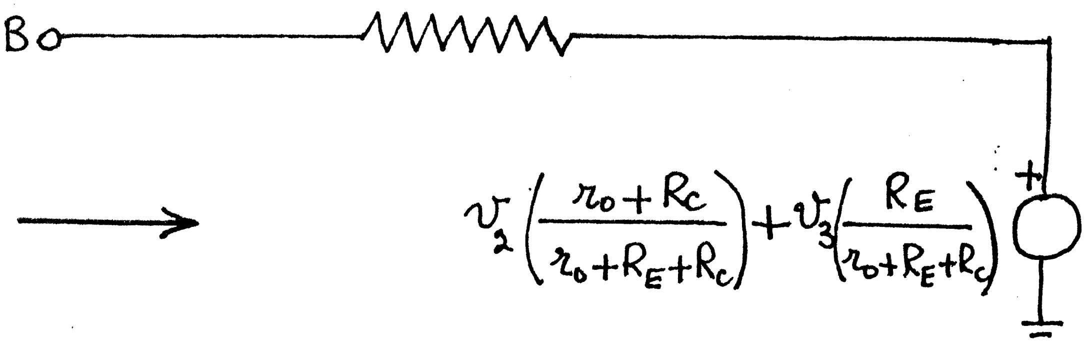
$$i_b = \frac{v}{r_\pi + \frac{R_E(r_o+R_C)}{R_E+r_o+R_C}} - \beta i_b \frac{r_o \frac{R_E}{R_E+r_\pi}}{r_o + R_C + \frac{r_\pi R_E}{r_\pi + R_E}}$$

$$R_{eq} = \frac{v}{i} = \frac{v}{i_b} = \boxed{\frac{r_o[r_\pi + R_E(1+\beta)] + r_\pi R_E + r_\pi R_C + R_C R_E}{R_E+R_C+r_o}}$$

Thévenin Input Equivalent Circuit (small signal)



$$\left[r_\pi + (1+\beta)R_E\right]\left(\frac{r_o}{r_o + R_E + R_C}\right) + \frac{r_\pi R_E + r_\pi R_C + R_E R_C}{r_o + R_E + R_C}$$

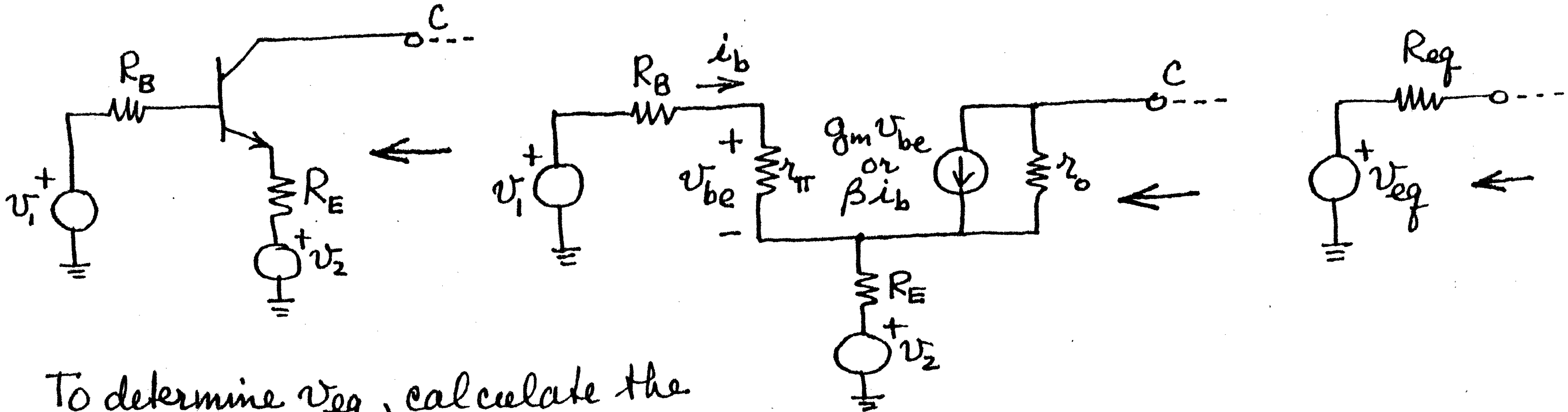


$$v_2\left(\frac{r_o + R_C}{r_o + R_E + R_C}\right) + v_3\left(\frac{R_E}{r_o + R_E + R_C}\right)$$

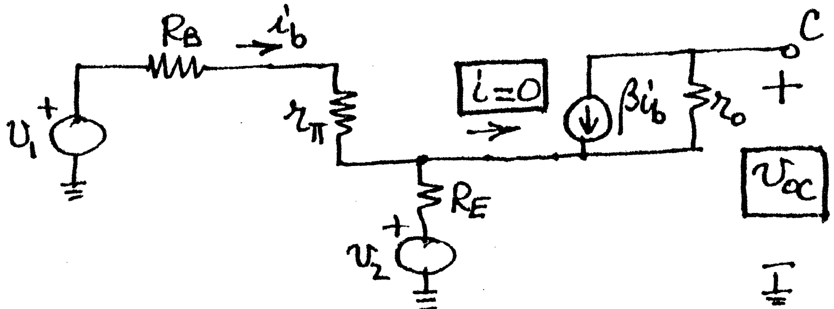
Discussion:

The most significant effect of r_o is that it provides coupling between output and input circuits. As a result changes in the collector circuit influence the base circuit. A voltage proportional to v_3 is fed back as long as $R_E \neq 0$.

Output equivalent circuit including the effect of r_o (small signal)



To determine v_{eq}, calculate the open-circuit output voltage v_{oc}.

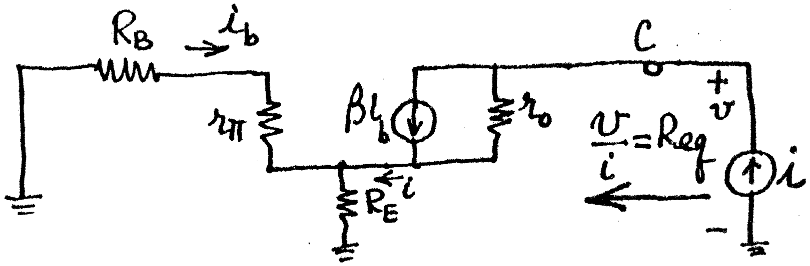


$$i_b = \frac{v_1 - v_2}{R_B + r_\pi + R_E}$$

$$v_{oc} = v_2 + i_b R_E - \beta i_b r_o = v_2 + \frac{(v_1 - v_2)(R_E - \beta r_o)}{R_B + r_\pi + R_E}$$

$$\boxed{v_{oc} = \frac{v_2 (R_B + r_\pi + \beta r_o) - v_1 (\beta r_o - R_E)}{R_B + r_\pi + R_E} = v_{eq}}$$

To determine R_{eq}, let $v_1 = v_2 = 0$, and calculate resistance seen at output.

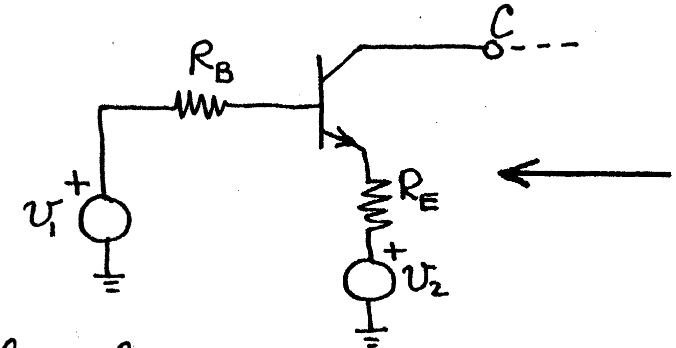


$$i_b = -i \frac{R_E}{R_B + r_\pi + R_E}$$

$$v = (i - \beta i_b) r_o + i \frac{R_E (R_B + r_\pi)}{R_E + R_B + r_\pi} = i \left[r_o \left(1 + \frac{\beta R_E}{R_B + r_\pi + R_E} \right) + \frac{R_E (R_B + r_\pi)}{R_E + R_B + r_\pi} \right]$$

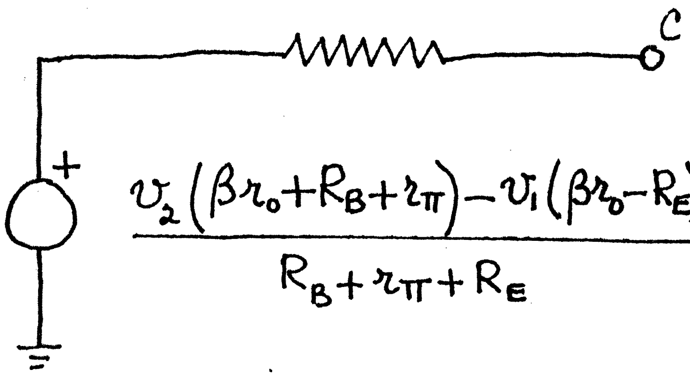
$$\boxed{R_{eq} = r_o \left[1 + \frac{R_E \left(\beta + \frac{R_B + r_\pi}{r_o} \right)}{R_B + r_\pi + R_E} \right]}$$

Thévenin and Norton Output Equivalent Circuits (small signal)



Thévenin Equivalent Circuit

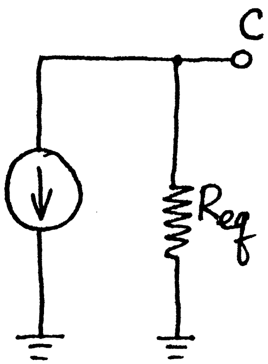
$$r_o\left[1+\frac{R_E\left(\beta+\frac{R_B+r_\pi}{r_o}\right)}{R_B+r_\pi+R_E}\right]=R_{eq}$$



$$\frac{v_2\left(\beta r_o+R_B+r_\pi\right)-v_1\left(\beta r_o-R_E\right)}{R_B+r_\pi+R_E}$$

Norton Equivalent Circuit

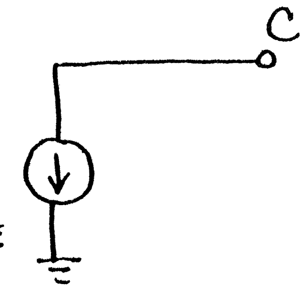
$$\frac{v_1\beta\left(1-\frac{R_E}{\beta r_o}\right)-v_2\beta\left(1+\frac{R_B+r_\pi}{\beta r_o}\right)}{\left[R_B+r_\pi+(1+\beta)R_E\right]\left\{1+\frac{R_E\left(R_B+r_\pi\right)}{r_o\left[R_B+r_\pi+(1+\beta)R_E\right]}\right\}}$$



Discussion of output equivalent circuit (small signal)

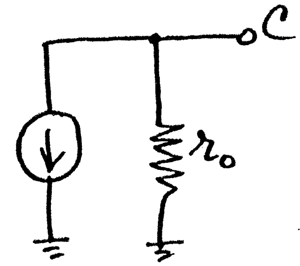
1. The output behaves like an ideal current source only when $r_o = \infty$. Can be used as a difference amplifier.

$$\frac{\beta(v_1 - v_2)}{R_B + r_\pi + (1+\beta)R_E}$$



2. The output behavest least like a current source when $R_E = 0$. Cannot be used as a difference amplifier.

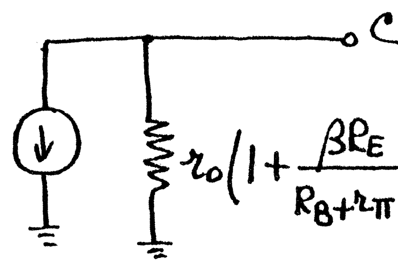
$$\frac{\beta\left[v_1 - v_2\left(1 + \frac{R_B + r_\pi}{\beta r_o}\right)\right]}{R_B + r_\pi}$$



r_o

3. If $R_E \ll \beta r_o$ and $R_B + r_\pi \ll \beta r_o$, the output equivalent circuit to an excellent approximation is:

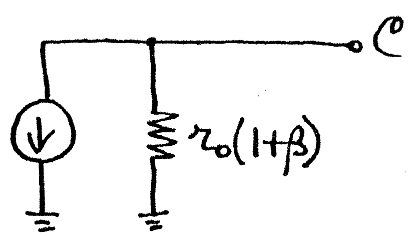
$$\frac{\beta(v_1 - v_2)}{R_B + r_\pi + (1+\beta)R_E}$$



$$r_o\left(1 + \frac{\beta R_E}{R_B + r_\pi + R_E}\right)$$

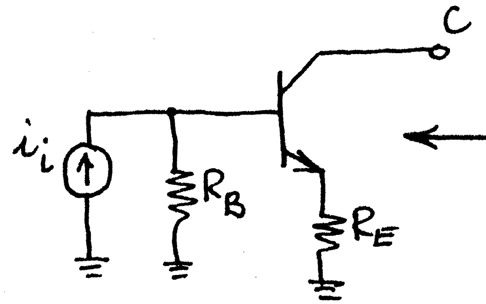
Further increase in output resistance results if R_B is kept low. In particular, for $R_B + r_\pi \ll R_E$, the circuit simplifies to:

$$\frac{\beta}{1+\beta}\frac{(v_1 - v_2)}{R_E}$$

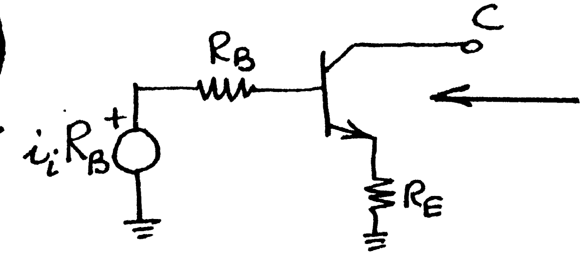


$r_o(1+\beta)$

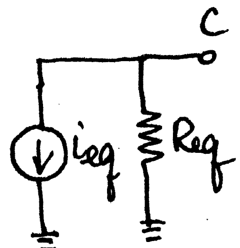
L6: Output equivalent circuit for current-source excitation (small signal)



Convert the nonideal current source to a nonideal voltage source and obtain



Use the Norton equivalent circuit given on p37 with $v_1 = i_i R_B$ and $v_2 = 0$ and obtain



where

$$i_{eq} = \frac{i_i R_B \beta \left(1 - \frac{R_E}{\beta r_o}\right)}{\left[R_B + r_\pi + (1+\beta) R_E\right] \left\{1 + \frac{R_E (R_B + r_\pi)}{r_o \left[R_B + r_\pi + (1+\beta) R_E\right]}\right\}}$$

$$R_{eq} = r_o \left[1 + \frac{R_E \left(\beta + \frac{R_B + r_\pi}{r_o}\right)}{R_B + r_\pi + R_E}\right]$$

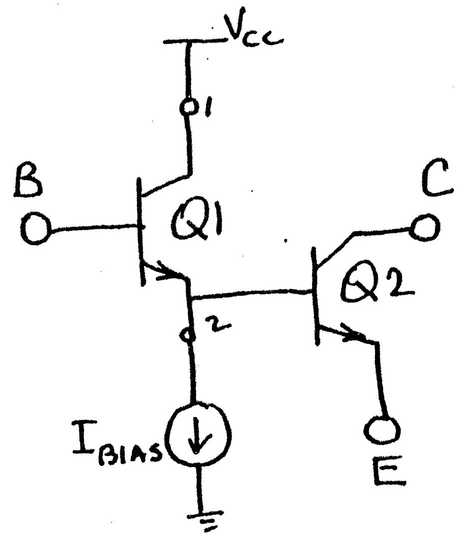
If the current-source excitation is ideal, i.e. $\underline{R_B = \infty}$, i_{eq} and R_{eq} can be simplified to

$$i_{eq} = \frac{i_i \beta \left(1 - \frac{R_E}{\beta r_o}\right)}{1 + \frac{R_E}{r_o}}$$

$$R_{eq} = r_o \left(1 + \frac{R_E}{r_o}\right)$$

Composite Transistors: CC–CC and CC–CE pairs

Consider the five-terminal composite transistor circuit shown. Two of the terminals, 1 and 2, are committed; 1 is connected to V_{cc} and 2 to I_{BIAS}. The remaining three terminals, B, C, and E are free.

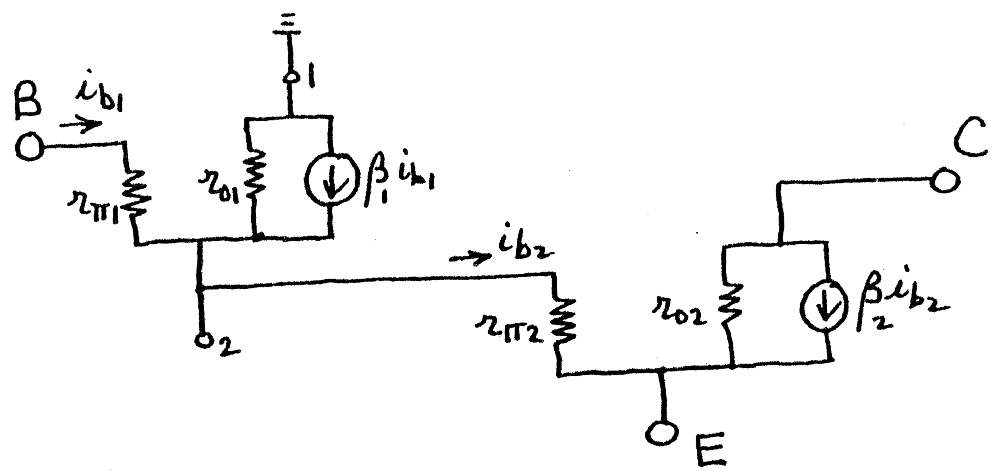


Assume the input is between the base B and ground.
If the output is taken between collector C and ground, a CC-CE composite pair results.
If the output is taken between emitter E and ground, a CC-CC composite pair results.

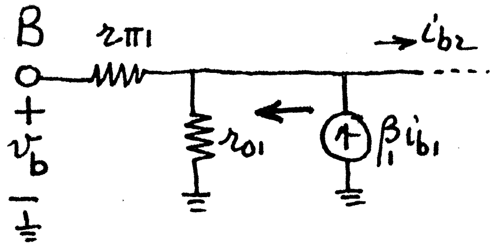
Problem: Determine the small-signal equivalent circuit of the composite pair.

Solution:

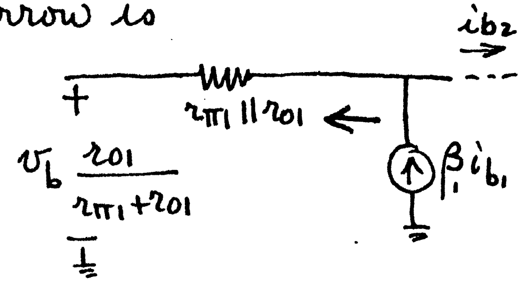
Represent the transistors with their small-signal equivalent circuits and obtain →



Part of the circuit is redrawn here for simplification.



The Thévenin equivalent circuit to the left of the arrow is



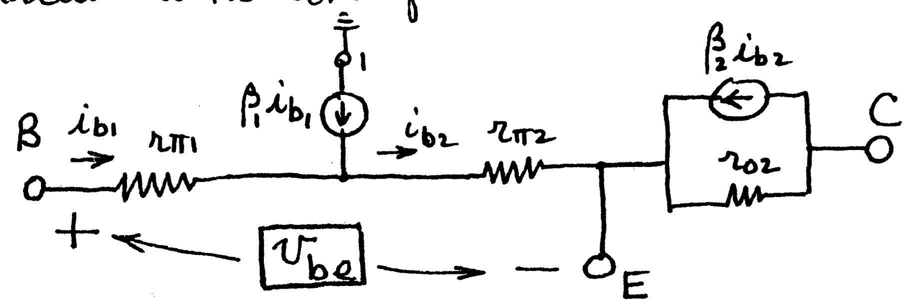
$r_{\pi 1}$ and r_{01} are fixed by operating point (quiescent) values:

$$r_{\pi 1} = \frac{V_T}{I_{B1}} = \frac{V_T}{I_{C1}/\beta_1} = \beta_1 \frac{V_T}{I_{C1}}$$

$$r_{01} = \frac{V_A + V_{CE1}}{I_{C1}}$$

Comparing $r_{\pi 1}$ with r_{01}, we see that $r_{\pi 1} \ll r_{01}$

Consequently, the Thévenin equivalent-circuit representation simplifies to the original input circuit with r_{01} left out.

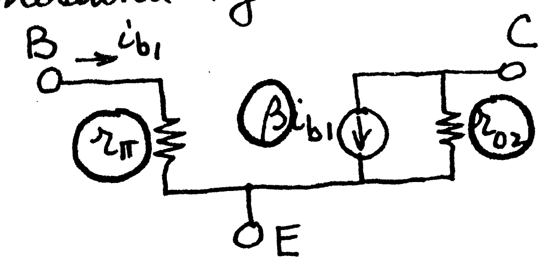


$$v_{be} = i_{b1} r_{\pi 1} + i_{b2} r_{\pi 2}$$

But $(1+\beta_1) i_{b1} = i_{b2}$

Therefore, $\boxed{v_{be} = i_{b1}\left[r_{\pi 1} + (1+\beta_1) r_{\pi 2}\right]}$

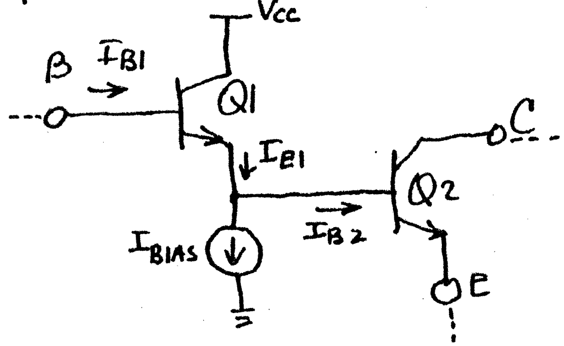
This result suggests that as far as the B, E, C terminals are concerned, the composite transistor circuit can be replaced with a single transistor represented by



where

$$\boxed{\begin{aligned} r_\pi &= r_{\pi 1} + (1+\beta_1) r_{\pi 2} \\ \beta &= (1+\beta_1)\beta_2 \end{aligned}}$$

Because $r_{\pi 2}$ is related to $r_{\pi 1}$, r_π can be simplified further. For this, we must first establish the relationship between the quiescent base currents.



$$I_{B2} = I_{E1} - I_{BIAS} = (1+\beta_1)I_{B1} - I_{BIAS}$$

$$\boxed{\frac{I_{B2}}{I_{B1}} = (1+\beta_1) - \frac{I_{BIAS}}{I_{B1}}}$$

$$r_{\pi 1} = \frac{V_T}{I_{B1}} \qquad r_{\pi 2} = \frac{V_T}{I_{B2}} \qquad \boxed{\frac{r_{\pi 2}}{r_{\pi 1}} = \frac{I_{B1}}{I_{B2}}}$$

$$r_\pi = r_{\pi 1} + (1+\beta_1)r_{\pi 2} = r_{\pi 1}\left[1 + (1+\beta_1)\frac{r_{\pi 2}}{r_{\pi 1}}\right]$$

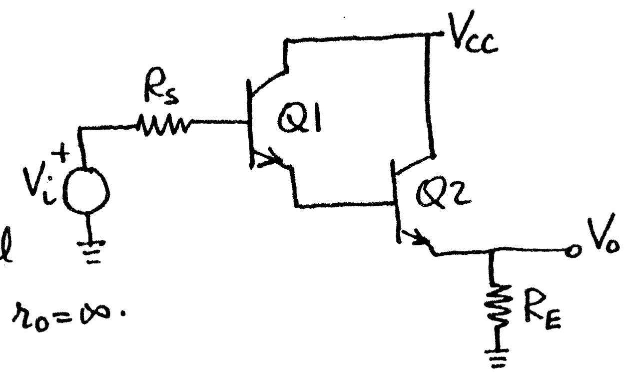
$$= r_{\pi 1}\left[1 + (1+\beta_1)\frac{I_{B1}}{I_{B2}}\right]$$

$$= r_{\pi 1}\left[1 + (1+\beta_1)\frac{1}{(1+\beta_1) - \frac{I_{BIAS}}{I_{B1}}}\right]$$

$$\boxed{r_\pi = r_{\pi 1}\left[1 + \frac{1}{1 - \frac{1}{1+\beta_1}\frac{I_{BIAS}}{I_{B1}}}\right]}$$

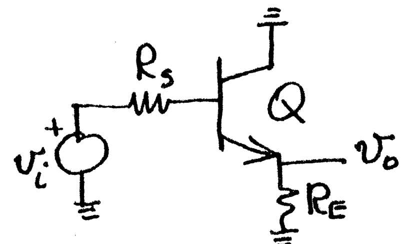
Example:

Find the impedance seen by the voltage source and the overall voltage gain. Assume $r_o = \infty$.



Solution:

Replace the composite transistor with its equivalent and obtain



The r_π and β of Q are given by

$$r_\pi = r_{\pi 1} + (1+\beta_1)r_{\pi 2} \qquad \beta = (1+\beta_1)\beta_2$$

Since $I_{BIAS} = 0$, $I_{B2} = (1+\beta_1)I_{B1}$ and hence $r_{\pi 2} = \frac{r_{\pi 1}}{1+\beta_1}$

the resulting $\boxed{r_\pi = 2r_{\pi 1}}$.

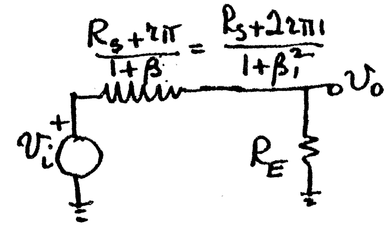
Since $V_{CE2} = V_{CE1} + V_{BE2} \cong V_{CE1}$, the two β's are the same resulting in $\boxed{\beta = (1+\beta_1)\beta_1 \cong \beta_1^2}$

Source v_i sees

$$R_S + r_\pi + (1+\beta)R_E$$

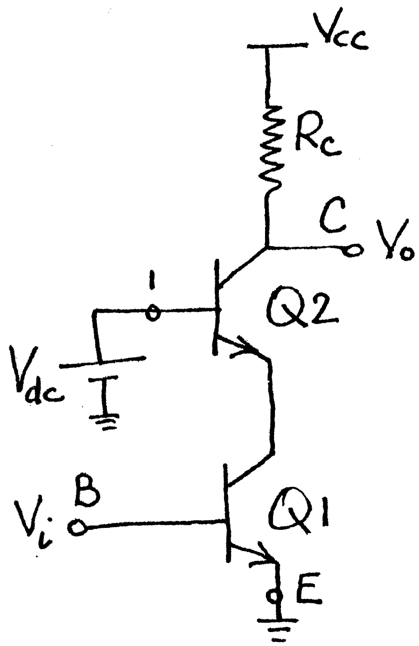
$$= \boxed{R_S + 2r_{\pi 1} + (1+\beta_1^2)R_E}$$

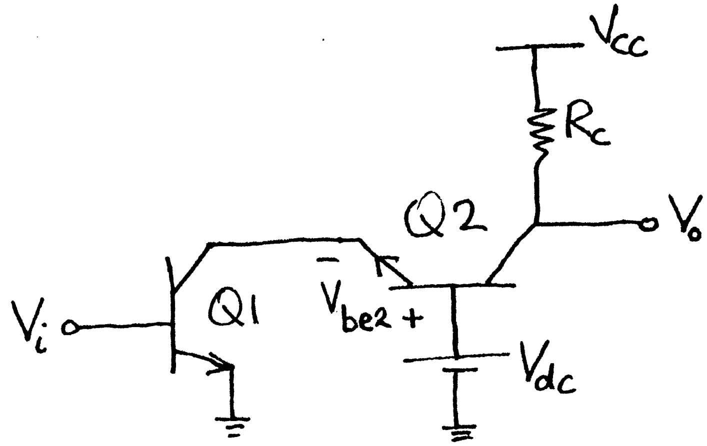
The equivalent circuit facing R_E is



The gain is $\boxed{A_v = \frac{R_E}{R_E + \frac{R_S + 2r_{\pi 1}}{1+\beta_1^2}}}$

The Cascode (CE–CB) Amplifier





$$V_{dc} - V_{be2} + V_{CE2sat} \leq V_o \leq V_{cc}$$

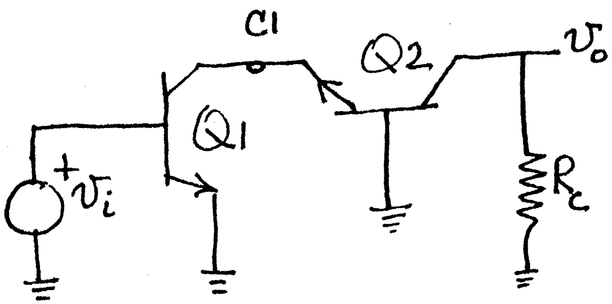
To prevent Q1 from sat.

$$V_{dc} > V_{be2} + V_{CE1sat}$$

To prevent Q2 from sat.

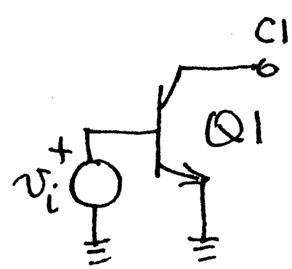
$$V_o > \underbrace{V_{dc} - V_{be2}}_{V_{ce1}} + V_{CE2sat}$$

Small-signal analysis

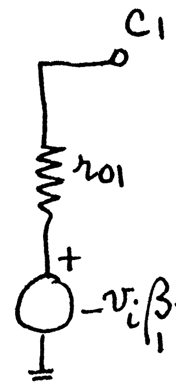


CE Amplifier CB Amplifier

The CE Amplifier portion of the circuit

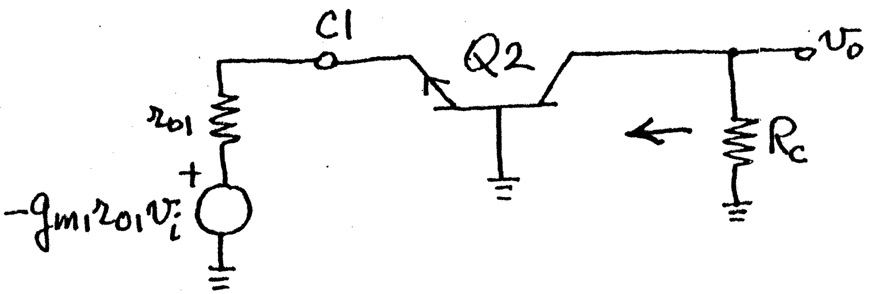


using the results given on p37

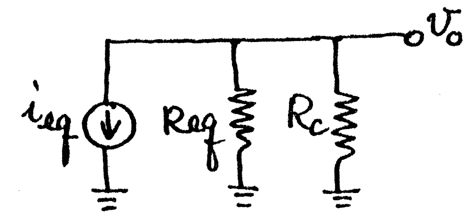


$$-v_i \beta_1 \frac{r_{o1}}{r_{\pi 1}} = -g_{m1} r_{o1} v_i$$

The CB Amplifier portion of the circuit



Using the results given on p37

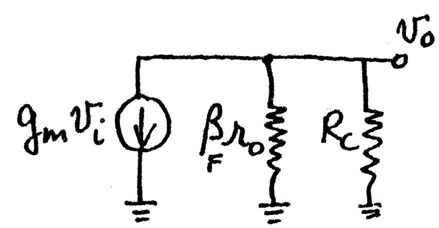


$$i_{eq} = g_{m1} r_{o1}\left[\frac{v_i \beta_2}{r_{\pi 2} + (1+\beta_2) r_{o1}}\right]\left\{\frac{1 + \frac{r_{\pi 2}}{\beta_2 r_{o2}}}{1 + \frac{r_{o1} r_{\pi 2}}{r_{o2}\left[r_{\pi 2} + (1+\beta_2) r_{o1}\right]}}\right\}, \quad R_{eq} = r_{o2}\left[1 + \frac{r_{o1}\left(\beta_2 + \frac{r_{\pi 2}}{r_{o2}}\right)}{r_{\pi 2} + r_{o1}}\right]$$

Now assume $V_A \gg V_{CE1}$ and V_{CE2}. This means that $\beta = \beta_F\left(1 + \frac{V_{CE}}{V_A}\right) \cong \beta_F$. Also we see that $I_{C1} \cong I_{C2}$. It follows that $r_{\pi 1} = r_{\pi 2} = r_\pi$, $g_{m1} = g_{m2} = g_m$, $r_{o1} = r_{o2} = r_o$, $\beta_1 = \beta_2 = \beta_F$.

$$\boxed{i_{eq} = v_i\left[\frac{g_m r_o \beta_F}{r_\pi + (1+\beta_F) r_o}\right]\left[\frac{1 + \frac{r_\pi}{\beta_F r_o}}{1 + \frac{r_\pi}{r_\pi + (1+\beta_F) r_o}}\right]}, \quad \boxed{R_{eq} = r_o\left[1 + \frac{r_o\left(\beta_F + \frac{r_\pi}{r_o}\right)}{r_\pi + r_o}\right]}$$

We can simplify these results further by assuming $\beta_F + 1 \cong \beta_F$ and $r_\pi \ll r_o$. (The latter approx. implies $\frac{\beta_F V_T}{I_C} \ll \frac{V_A}{I_C}$.) $\rightarrow$

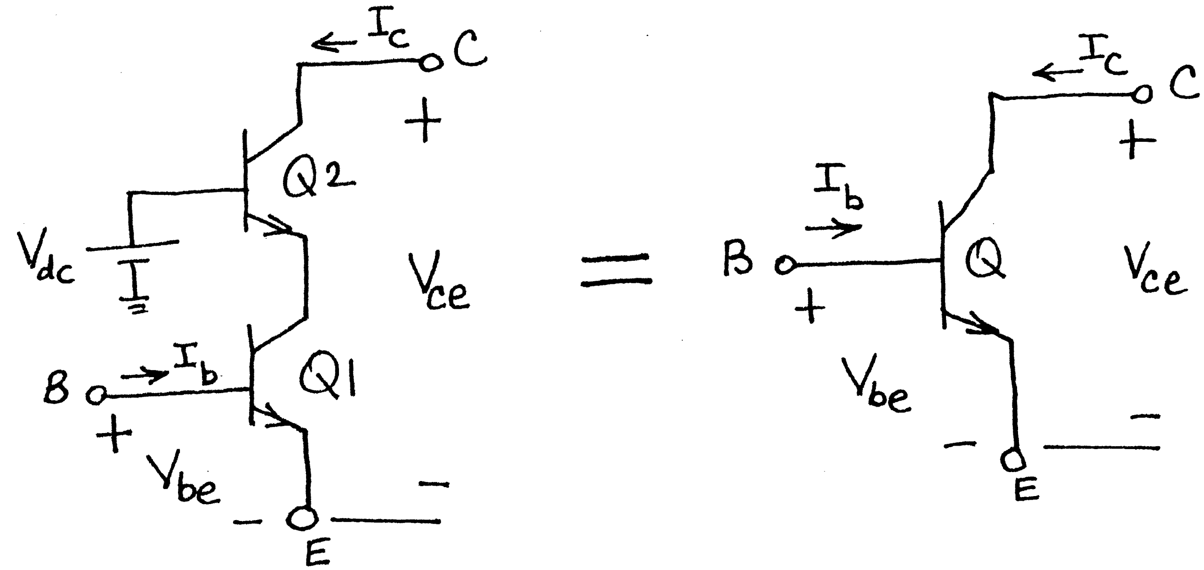


$$v_o = -g_m v_i \frac{\beta_F r_o R_C}{\beta_F r_o + R_C}$$

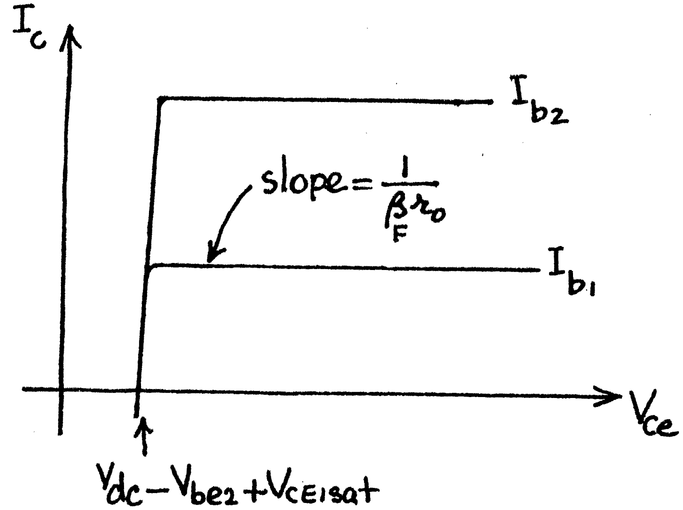
$$\boxed{A_v = -g_m \frac{\beta_F r_o R_C}{\beta_F r_o + R_C}}$$

$$A_v\Big|_{\beta_F r_o \gg R_C} \cong \boxed{-g_m R_C}$$

Summary of the results of the Cascode Amplifier

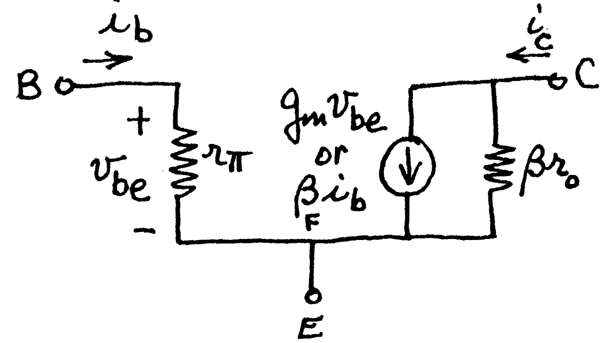


Large-signal characteristics



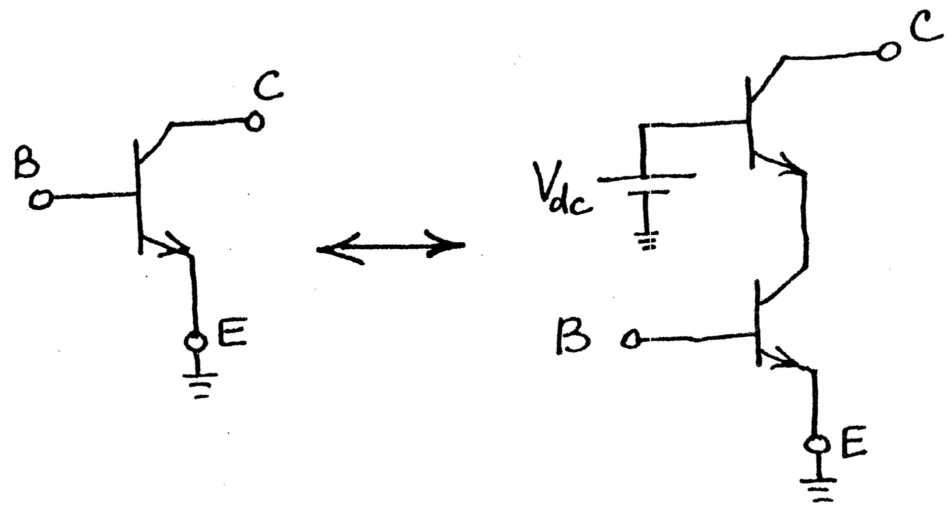
I_c becomes negative when the base-to-collector junction of Q_2 becomes forward biased

Small-signal characteristics



Demonstration

Comparison of single transistor output characteristics with the cascode circuit using the curve tracer.

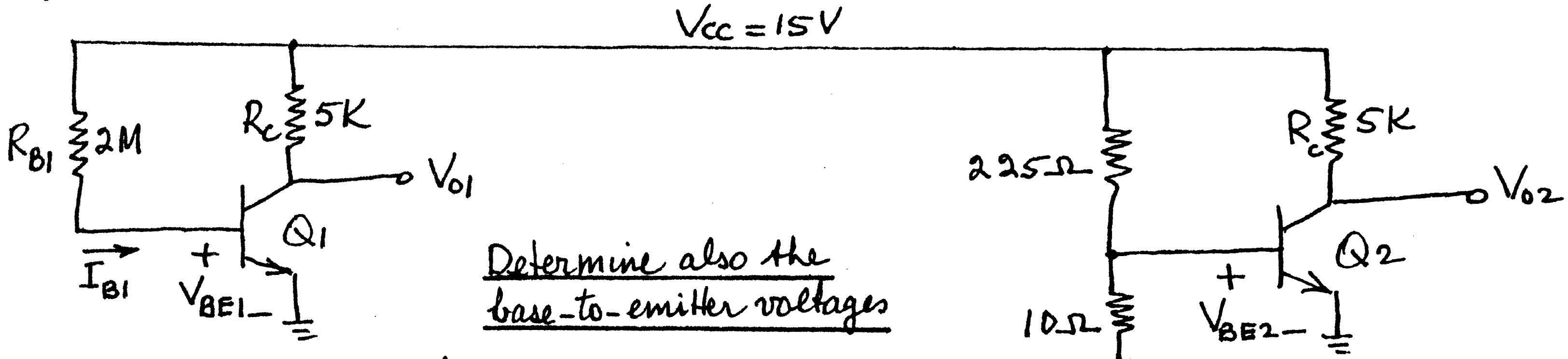


Use I_b as a parameter and display the I_c vs V_{ce} curves.

Vary V_{dc} to show its effect.

L7: Power supply sensitivity of bias circuits

Given $I_s = 3.305\times10^{-14}$ A and $\beta = 210$. Calculate V_{o1} and V_{o2}. Assume $V_A = \infty$.



Determine also the base-to-emitter voltages

Base-current controlled bias

$$I_{B1} = \frac{I_s e^{\frac{V_{BE1}}{V_T}}}{\beta} = \frac{V_{CC} - V_{BE1}}{R_{B1}}$$

$$\frac{15 - V_{BE1}}{2\times10^6} = \frac{3.305\times10^{-14}\, e^{\frac{V_{BE1}}{26\times10^{-3}}}}{210}$$

Solve by trial and error for V_{BE1}.

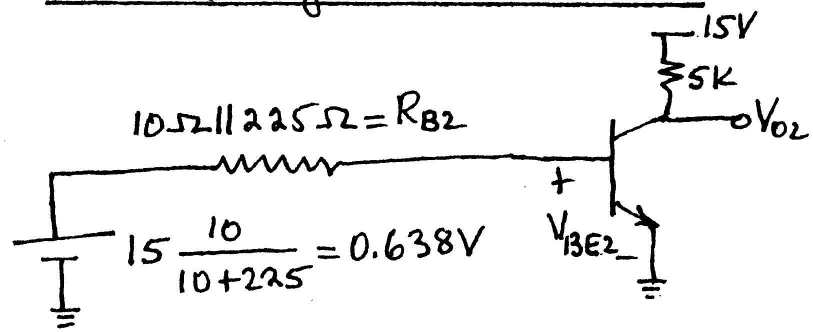
$\boxed{V_{BE1} = 0.638V}$

$$I_{C1} = \beta I_{B1} = \beta\frac{(V_{CC} - V_{BE1})}{R_{B1}} = 210\left(\frac{15-0.638}{2\times10^6}\right)$$

$\boxed{I_{C1} = 1.5mA}$

$V_{o1} = V_{CC} - R_C I_{C1} = 15 - 5\times1.5 = \boxed{7.5V}$

Base-voltage controlled bias



$$15\frac{10}{10+225} = 0.638V$$

Since $R_{B2} < 10\Omega$, the voltage across it is negligible. Consequently

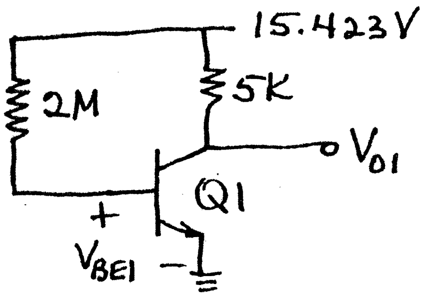
$\boxed{V_{BE2} = 0.638V}$

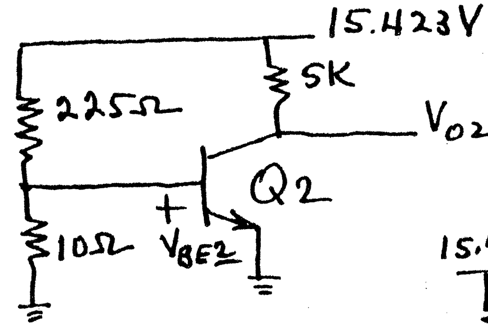
$\boxed{I_{C2} = 1.5mA}$ $\boxed{V_{o2} = 7.5V}$

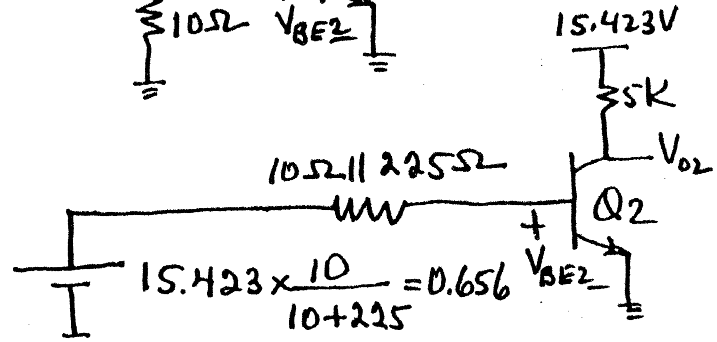
Both circuits have the same operating point.

Now suppose V_{cc} changes from 15V to 15.423V

Calculate the new operating points:







$$15.423 \times \frac{10}{10+225} = 0.656$$

$$\frac{15.423 - V_{BE1}}{2\times10^{6}} = \frac{3.305\times10^{-14}}{210}\, e^{\frac{V_{BE1}}{26\times10^{-3}}}$$

Solve for V_{BE1} by trial and error.

$\boxed{V_{BE1} = 0.639\,V}$

There is only 1mV change in V_{BE1}.

$$I_{C1} = \beta I_{B1} = 210\,\frac{15.423-0.639}{2\times10^{6}} = \boxed{1.55\,mA}$$

$$V_{01} = 15.423 - 5\times1.55 = \boxed{7.67\,V}$$

There is very little change in operating point voltage and current.

$\boxed{V_{BE2} = 0.656\,V}$

There is $656 - 638 = 18mV$ change in base-to-emitter voltage.

Therefore, the new I_{C2} will be

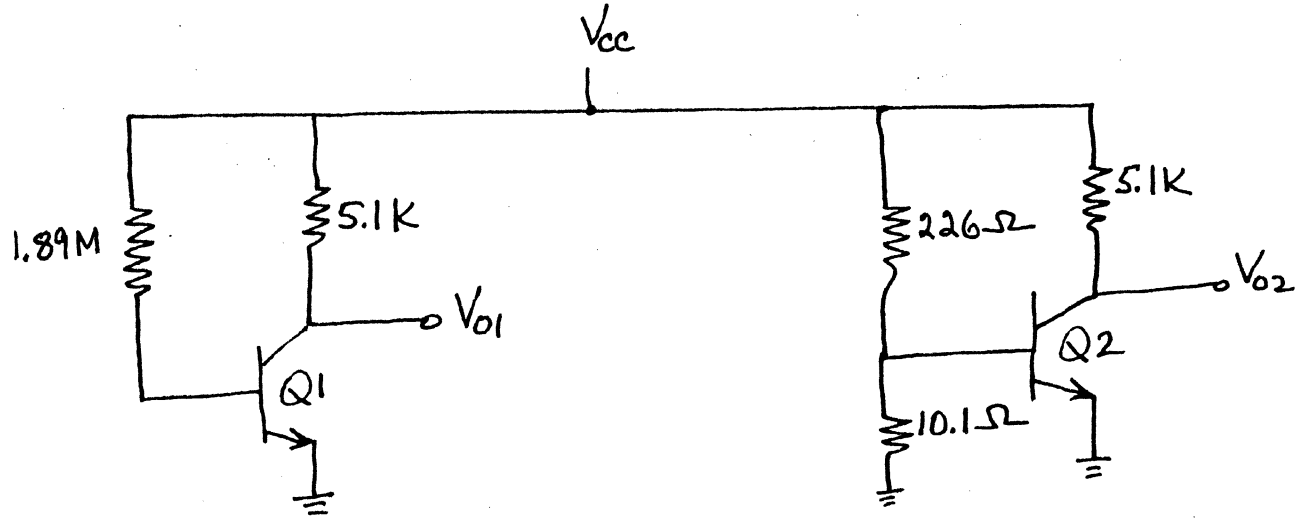
$$I_{C2} = 2\times1.5 = \boxed{3\,mA}$$

$$V_{02} = 15.423 - 3\times5 = \boxed{0.423\,V}$$

The transistor Q_2 is near sat.

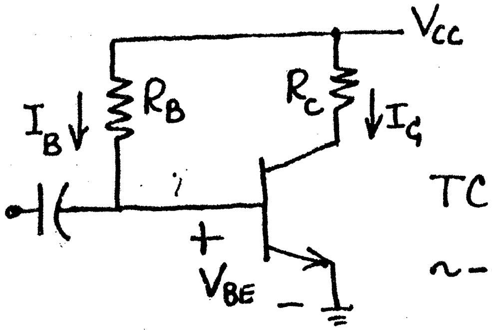
Make V_{BE} as independent of supply voltage as possible.

Demonstration: Power Supply Sensitivity



1. Adjust V_{cc} around 15V until $V_{o1} = V_{o2} \cong 7.5V$.
2. Change V_{cc} slightly (about 0.5V) to drive V_{o2} to saturation while V_{o1} changes only slightly.

Fixed-base-current bias



TC of V_{BE}
$\sim -2\text{mV}/°\text{C}$

$$I_B = \left.\frac{V_{CC}-V_{BE}}{R_B}\right|_{V_{CC}\gg V_{BE}} \cong \frac{V_{CC}}{R_B}$$

The base current is fixed.

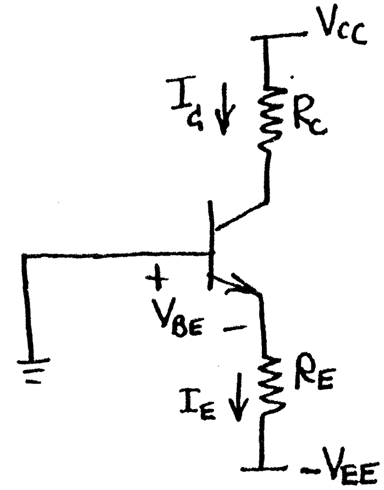
However, $I_C = \beta I_B \cong \boxed{\beta \frac{V_{CC}}{R_B}}$

<u>The collector current depends on the β of the transistor.</u>

β varies
- from wafer to wafer (50–500)
- with temp. (25% for $\Delta T = 25°\text{C}$)
- with V_{CE} (Early effect)

<u>Collector operating point</u> <u>cannot</u> <u>be fixed</u>.

Fixed-collector-current bias using two power supplies

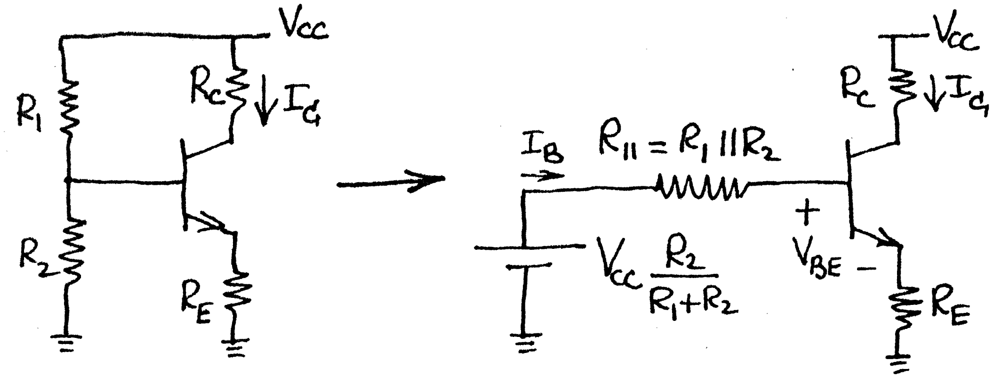


R_E provides coupling (feedback) between the base and collector circuits.

$$I_C \cong I_E = \left.\frac{V_{EE}-V_{BE}}{R_E}\right|_{V_{EE}\gg V_{BE}} \cong \boxed{\frac{V_{EE}}{R_E}}$$

The collector current and hence <u>the output operating point is fixed</u>. If the input signal (not shown) has no dc component, it can be inserted in series with the base. (Otherwise, use RC input coupling.)

Fixed-collector-current bias using one power supply



$$V_{cc}\frac{R_2}{R_1+R_2} = I_B R_{\parallel} + V_{BE} + R_E(I_B+I_C)$$

Since $I_C=\beta I_B$, this equation can be written as

$$V_{CC}\frac{R_2}{R_1+R_2} = I_B\left[R_{\parallel}+R_E(1+\beta)\right]+V_{BE}$$

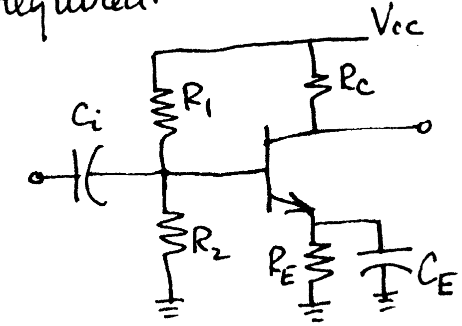
$$I_B=\frac{V_{CC}\frac{R_2}{R_1+R_2}-V_{BE}}{R_{\parallel}+(1+\beta)R_E}$$ which for $\boxed{\underbrace{R_{\parallel} \ll (1+\beta)R_E}_{\text{make } R_{\parallel}\le 10R_E}}$

becomes $$I_B \cong \frac{V_{CC}\frac{R_2}{R_1+R_2}-V_{BE}}{(1+\beta)R_E}$$

$$I_C=\beta I_B \cong \frac{\beta}{1+\beta}\,\frac{V_{CC}\frac{R_2}{R_1+R_2}-V_{BE}}{R_E} \cong \frac{V_{CC}\frac{R_2}{R_1+R_2}-V_{BE}}{R_E}$$ which

for $V_{CC}\frac{R_2}{R_1+R_2} \gg V_{BE}$ becomes $\boxed{I_C \cong \frac{V_{CC}\,R_2}{R_E(R_1+R_2)}}$

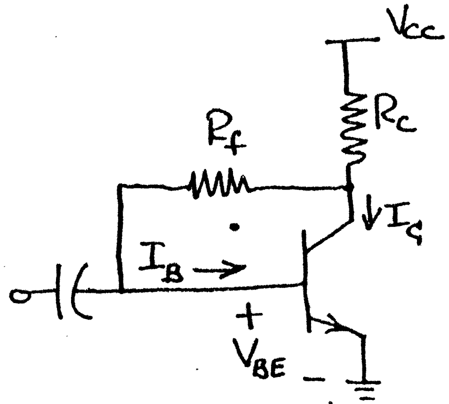
Thus the collector current is fixed, i.e., made independent of the transistor. The presence of R_E, however, reduces the signal gain unless it is bypassed with a capacitor. Also an input coupling capacitor is required.



For biasing IC's, this biasing scheme is undesireable because

1. It uses 3 resistors, two of which (R_1 and R_2) are large
2. Requires capacitors, one of which (C_E) is large.

Fixing the collector current by other methods



Bias stabilization through feedback

$$V_{CC} = (I_C + I_B)R_C + I_B R_f + V_{BE}$$

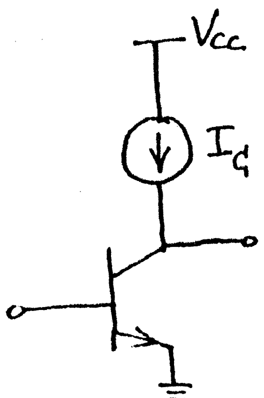
$$= \left(I_C + \frac{I_C}{\beta}\right)R_C + \frac{I_C}{\beta}R_f + V_{BE}$$

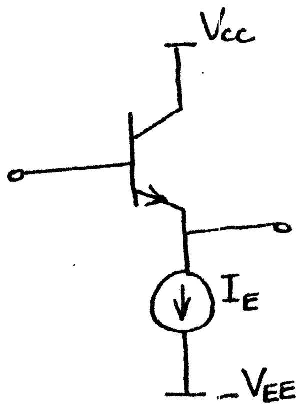
$$\boxed{I_C = \frac{V_{CC} - V_{BE}}{\left(1+\frac{1}{\beta}\right)R_C + \frac{R_f}{\beta}}}$$

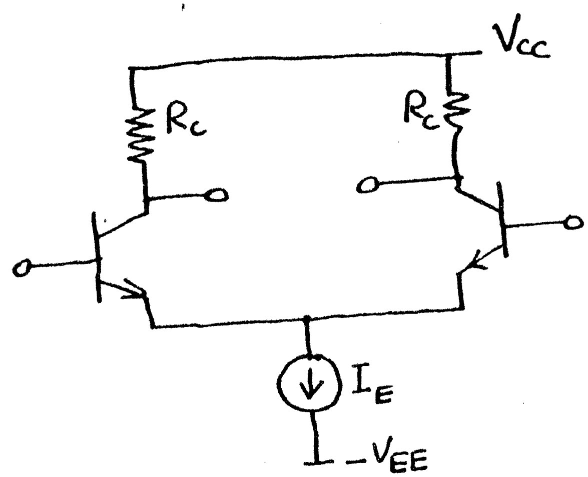
The β dependence of I_C can be minimized by making $\frac{R_f}{\beta} \ll R_C$. Too small of an R_f, however, reduces the signal gain.

Biasing schemes using current sources

Circuits that fix the collector or emitter current.

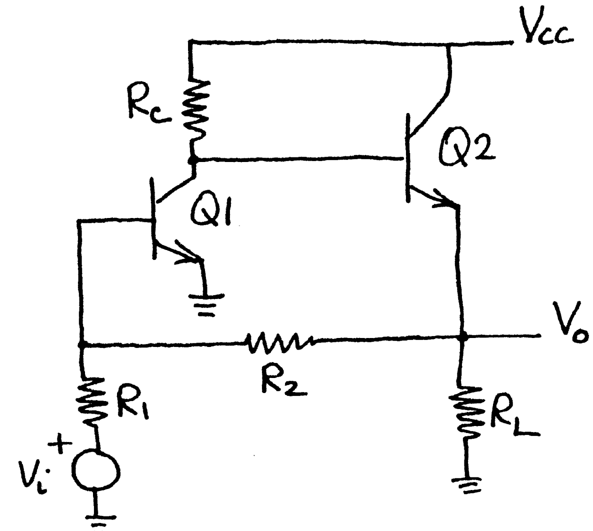




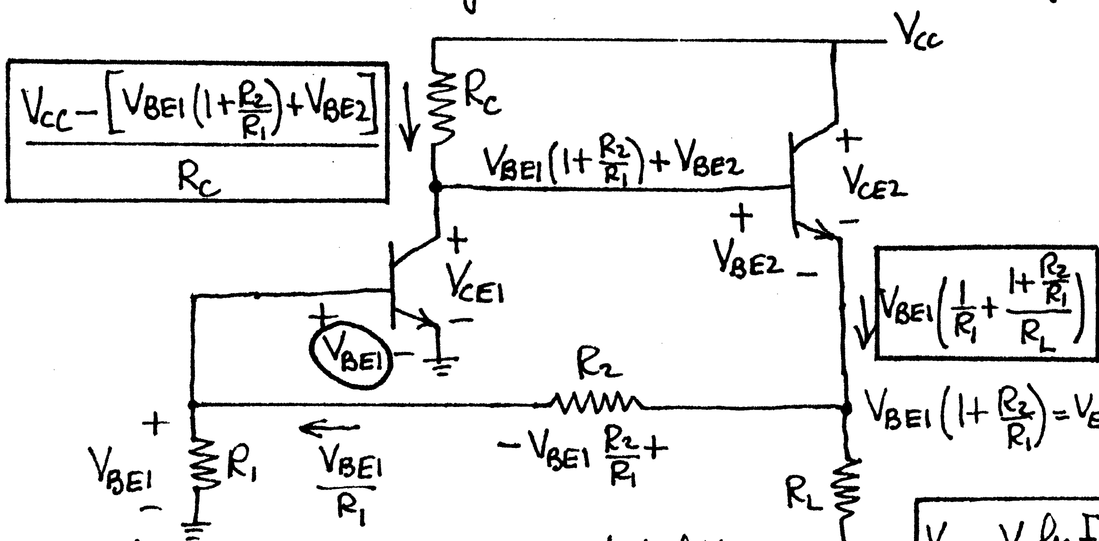


Fixing the collector-to-emitter voltages

Calculate the collector-to-emitter voltages and the collector currents for the circuit shown. Assume the transistor β's are sufficiently high, and therefore the base currents can be neglected relative to the other currents. The input V_i does not affect the operating points.



Solution: Redraw the circuit with $V_i = 0$. Starting out with V_{BE1}, calculate all the significant currents and voltages with respect to ground.



Note that V_{CE1} and V_{E2} are independent of V_{CC}.

$$\boxed{\begin{aligned} V_{CE1} &= V_{BE1}\left(1+\frac{R_2}{R_1}\right)+V_{BE2} \\ V_{CE2} &= V_{CC} - V_{BE1}\left(1+\frac{R_2}{R_1}\right) \end{aligned}}$$

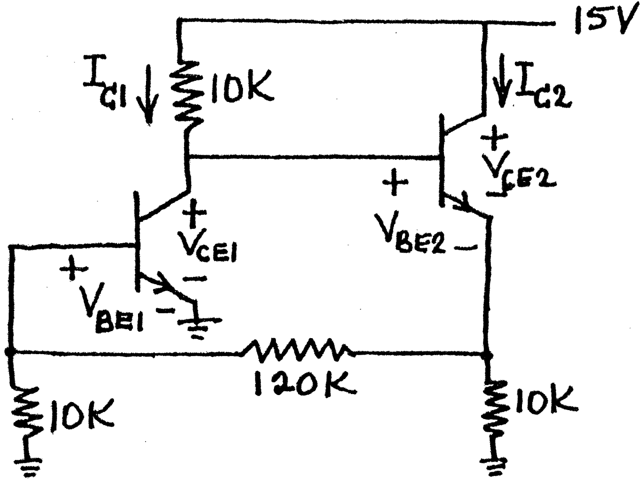
No current or voltage shown is β dependent.

Knowing that V_{BE}'s will be around 0.6–0.7V, we can make a rough estimate of all the currents and voltages. Then, using the I_C's thus found, we can make a more accurate determination of V_{BE}'s.

$$\boxed{V_{BE} = V_T \ln \frac{I_C}{I_S}}$$

Example:

For the circuit shown determine I_{C1}, I_{C2}, V_{CE1}, and V_{CE2}. $I_S = 10^{-15}$A.



From the results of the previous page,

$$I_{C1} \cong \frac{V_{CC} - \left[V_{BE1}\left(1 + \frac{R_2}{R_1}\right) + V_{BE2}\right]}{R_C} = \boxed{\frac{15 - 13V_{BE1} - V_{BE2}}{10}}$$

$$I_{C2} \cong V_{BE1}\left(\frac{1}{R_1} + \frac{1 + \frac{R_2}{R_1}}{R_L}\right) = \boxed{1.4\,V_{BE1}}$$

To start the trial and error solution of the problem, assume $V_{BE1} = V_{BE2} = 0.6$V. Then,

$I_{C1} = 0.660$ mA , $I_{C2} = 0.840$ mA

Using these first trial values of I_C's, calculate more accurate estimates of V_{BE}'s using

$$\boxed{V_{BE1} = V_T \ln \frac{I_{C1}}{I_S} = 26 \ln 10^{15} I_{C1},\ V_{BE2} = V_T \ln \frac{I_{C2}}{I_S} = 26 \ln 10^{15} I_{C2}}$$

The results are $V_{BE1} = 707.6$mV, $V_{BE2} = 713.9$mV. With these better estimates of V_{BE}'s, calculate the new I_C's.

$I_{C1} = 0.509$ mA , $I_{C2} = 0.991$ mA

Using these more accurate values of I_C's, calculate the new V_{BE}'s.

$V_{BE1} = 700.9$mV , $V_{BE2} = 718.2$mV

One more iteration gives

$$\boxed{I_{C1} = 0.517\text{ mA},\ I_{C2} = 0.981\text{ mA}}$$

$V_{BE1} = 701.3$ mV , $V_{BE2} = 718.0$ mV

Note that the last set of V_{BE} values are hardly different from the previous set; hence no further iteration is necessary. The resulting V_{CE}'s are

$$V_{CE1} = V_{CC} - I_{C1}R_C = \boxed{9.83\text{V}}$$

$$V_{CE2} = V_{CC} - V_{BE1}\left(1 + \frac{R_2}{R_1}\right) = \boxed{5.88\text{V}}$$

Now suppose V_{CC} is changed from 15 to 20V. What are the new I_C's, V_{CE}'s, and V_{BE}'s?

Starting with $V_{BE1} = V_{BE2} = 0.7$V, after three iterations, we obtain

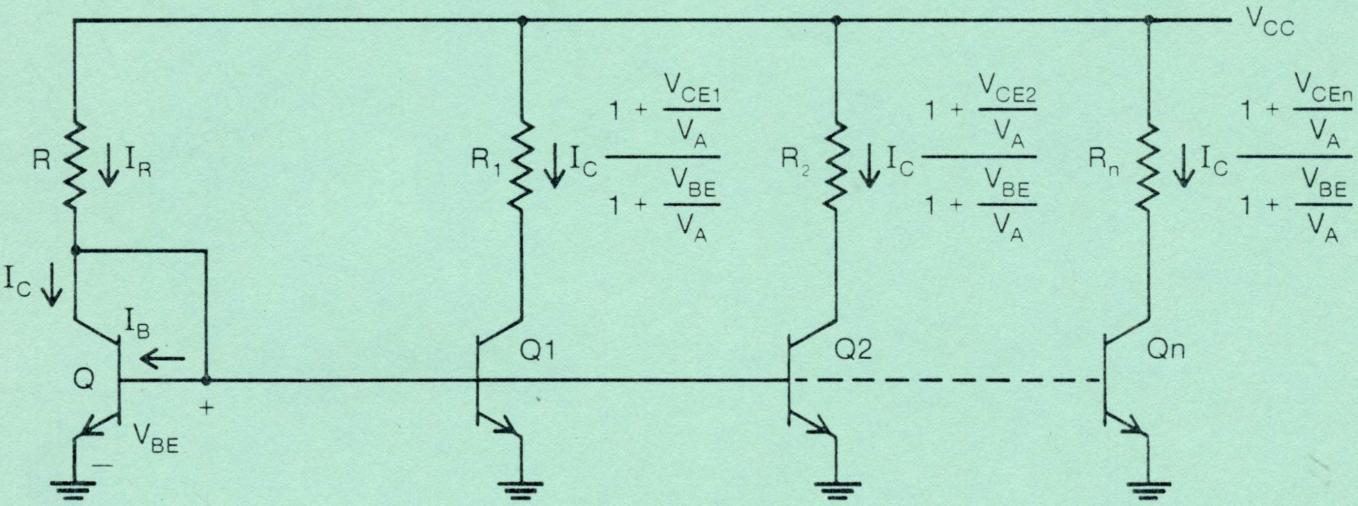
$V_{BE1} = 718.3$mV	$V_{BE2} = 718.6$mV
$I_{C1} = 0.994$mA	$I_{C2} = 1.007$mA
$V_{CE1} = 10.06$V	$V_{CE2} = 10.66$V

As V_{CC} changes from 15 to 20V, V_{CE1} changes from 9.83 to 10.06V.

A Self Study Subject

FUNDAMENTALS & APPLICATIONS OF ANALOG INTEGRATED CIRCUITS

PART I
LOW FREQUENCY ANALYSIS & DESIGN



Study Guide
for

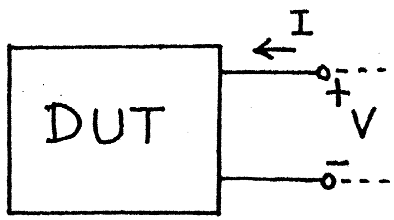
MODULE B
Current Sources & Applications

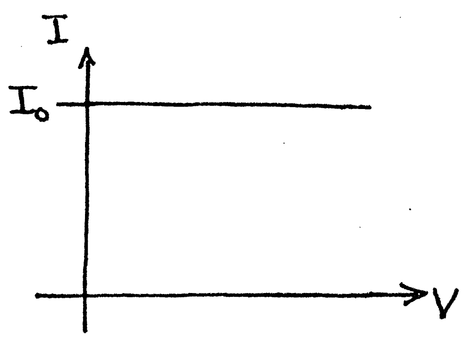
Colorado State University
Engineering Renewal
& Renewal & Growth Program

Aram Budak

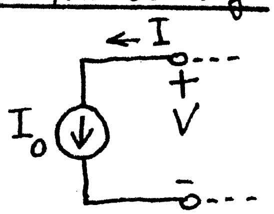
L8: DC CURRENT SOURCES

The ideal current source

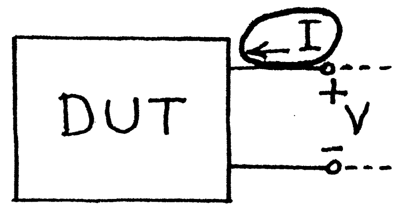


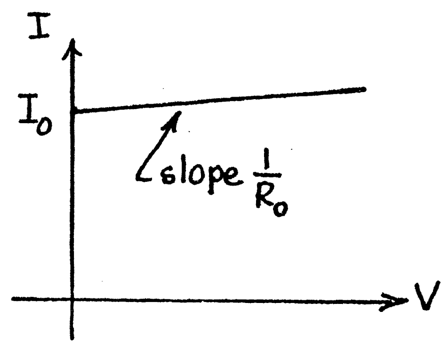


In an ideal current source, the current is independent of the voltage across the source.

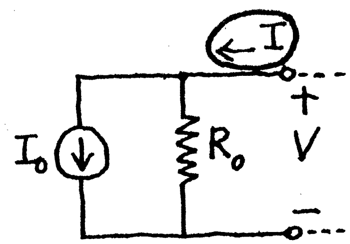


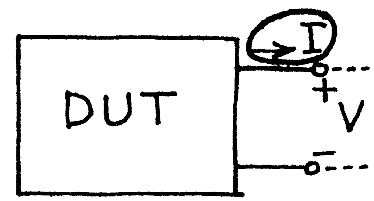
The actual current source

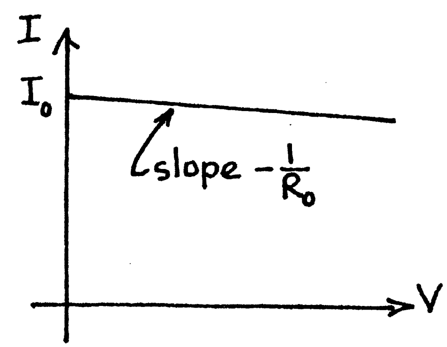




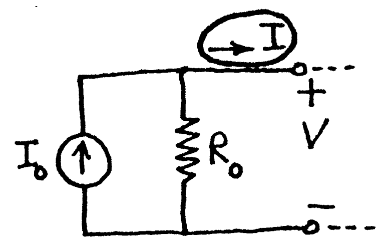
$$\boxed{I = I_0 + \frac{1}{R_0} V}$$







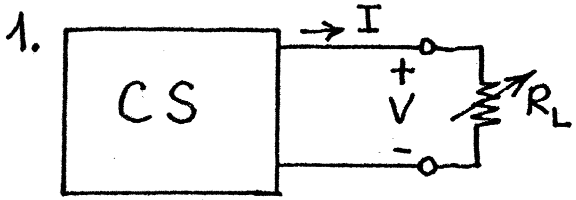
$$\boxed{I = I_0 - \frac{1}{R_0} V}$$



The larger R_0, the better the current source.

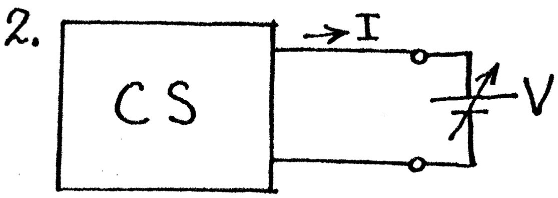
Measurement of output characteristics

1.



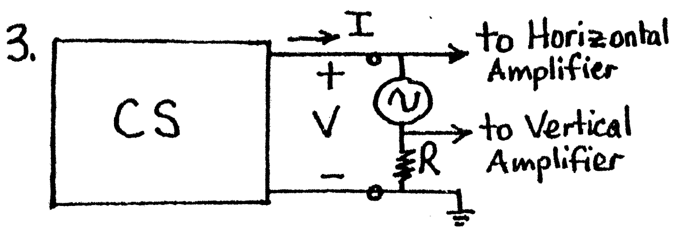
For each setting of R_L measure (I,V) and plot.

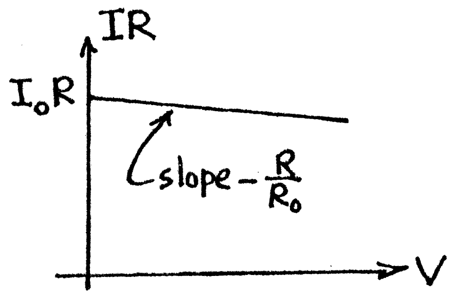
2.



For each setting of V measure (I,V) and plot.

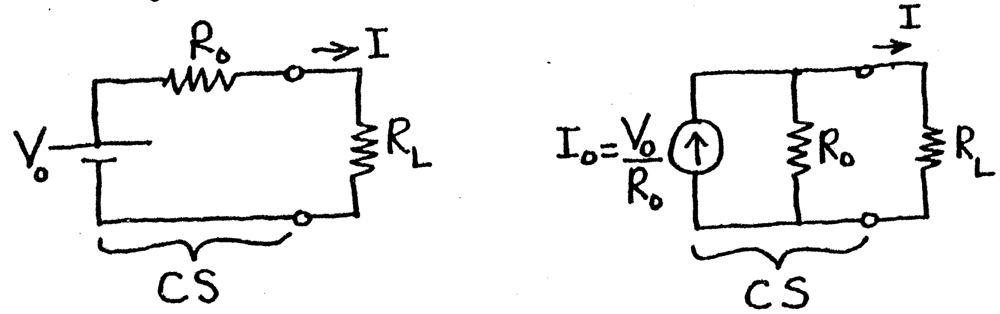
3.





Note: Signal source must be floating.

An elementary current source using a voltage source and a resistor

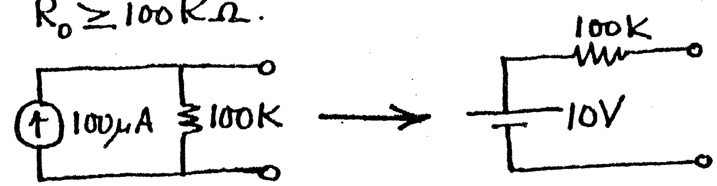


$$I = \frac{V_0}{R_0+R_L} = \frac{V_0}{R_0}\left(\frac{1}{1+\frac{R_L}{R_0}}\right) \qquad I = \frac{V_0}{R_0}\,\frac{R_0}{R_0+R_L} = \frac{V_0}{R_0}\left(\frac{1}{1+\frac{R_L}{R_0}}\right)$$

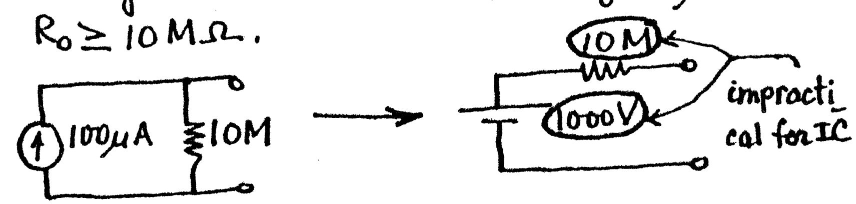
$$I\Big|_{R_L \ll R_0} \cong \boxed{\frac{V_0}{R_0}} \qquad I\Big|_{R_L \ll R_0} \cong \boxed{\frac{V_0}{R_0}}$$

Current through load, I, "does not depend" on R_L.

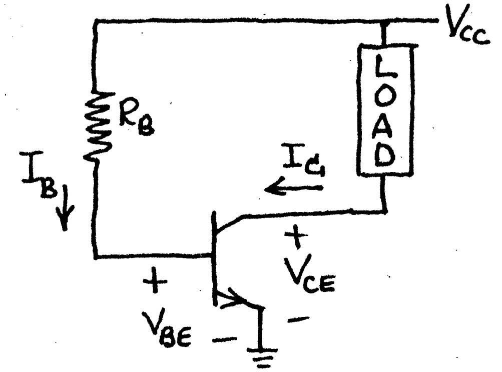
Example 1: Design a current source with $I_0 = 100\mu A$ and $R_0 \geq 100K\Omega$.



Example 2: Design a current source with $I_0 = 100\mu A$ and $R_0 \geq 10M\Omega$.

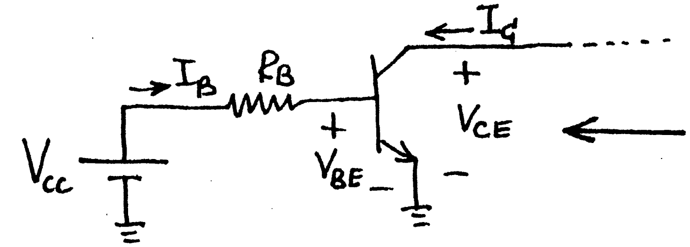


A current source using a transistor

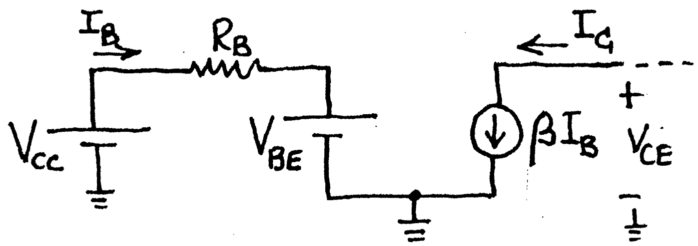


Load must have a dc path

$V_{CE} > V_{CEsat}$



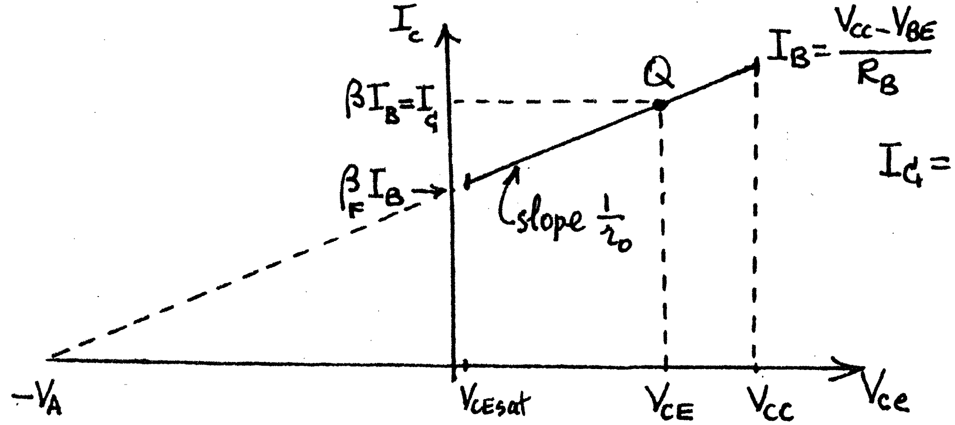
The output characteristic is that of a current source.



Note that the base-to-emitter voltage is assumed to be constant at V_{BE}. (Even under widely varying load conditions V_{BE} does not change.) V_{BE} can be assumed to be ~ 0.6V.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

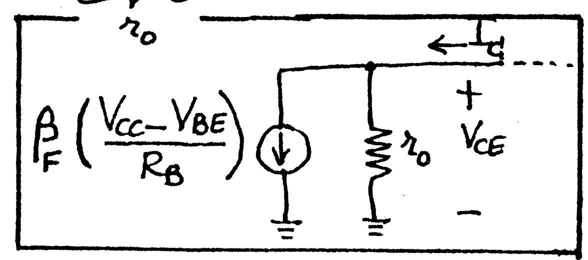
[Of course V_{BE} can be solved by trial and error using $\frac{(V_{CC} - V_{BE})}{R_B} = \frac{I_S e^{\frac{V_{BE}}{V_T}}}{\beta_F}$]



The Q point varies along the constant I_B line with changes in the load.

$$I_C = \beta I_B = \beta_F \left(1 + \frac{V_{CE}}{V_A}\right) I_B$$

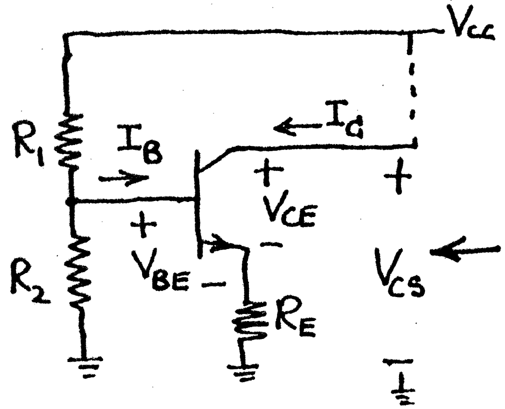
$$I_C = \beta_F I_B + \frac{V_{CE}}{\underbrace{V_A/\beta_F I_B}_{r_o}} = \boxed{\beta_F \left(\frac{V_{CC} - V_{BE}}{R_B}\right) + \frac{V_{CE}}{r_o}}$$

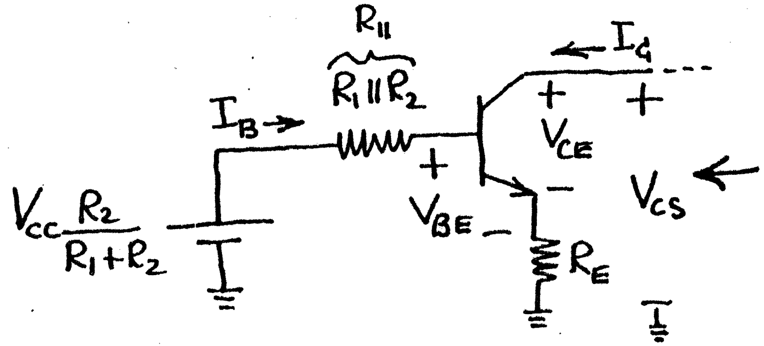


$V_{CEsat} \leq V_{CE}$

$V_{CE} \leq V_{CC}$

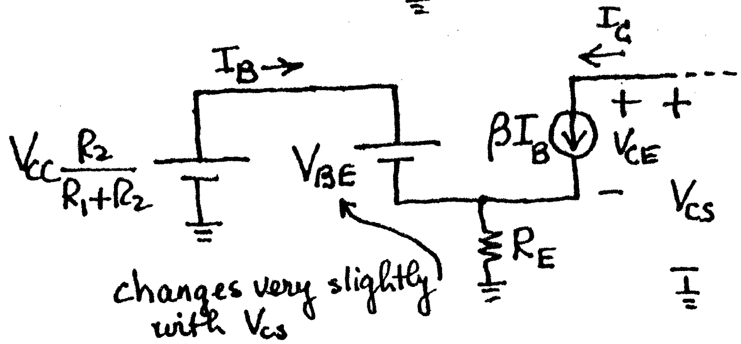
A better current source (uses three resistors two of which are not small)



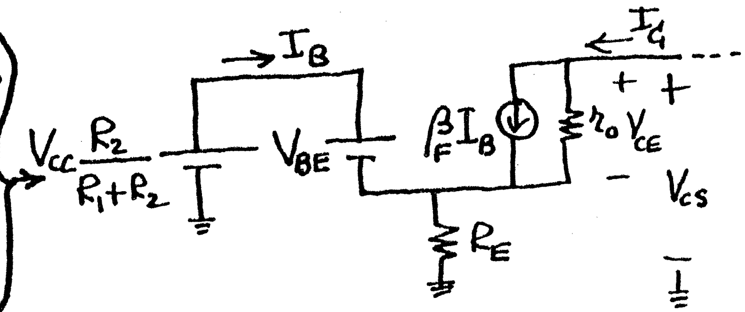


Load must be returned to V_{CC} or some other positive voltage supply. Load must have dc path.

Assume $I_B R_{11} \ll V_{CC}\frac{R_2}{R_1+R_2}$



$$\beta I_B = \beta_F\left(1+\frac{V_{CE}}{V_A}\right)I_B = \beta_F I_B + \frac{V_{CE}}{V_A/\beta_F I_B} = \beta_F I_B + \frac{V_{CE}}{r_o}$$



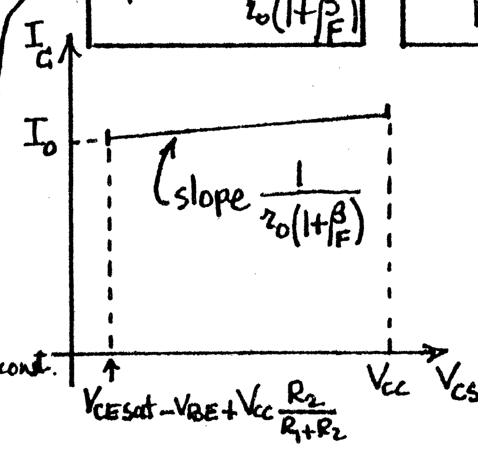
$$V_{CC}\frac{R_2}{R_1+R_2} - V_{BE} = (I_B + I_C)R_E \qquad I_B = \frac{V_{CC}\frac{R_2}{R_1+R_2} - V_{BE}}{R_E} - I_C$$

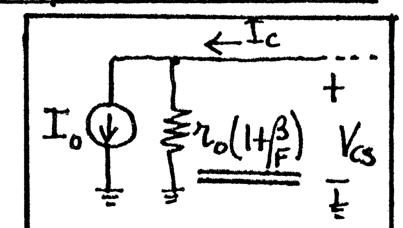
$V_{CS} = (I_C - \beta_F I_B)r_o - V_{BE} + V_{CC}\frac{R_2}{R_1+R_2}$; substitute I_B

and solve for I_C.

$$\boxed{I_C = \left(\frac{\beta_F}{1+\beta_F}\right)\frac{\left(V_{CC}\frac{R_2}{R_1+R_2} - V_{BE}\right)}{R_E}\left(1-\frac{R_E}{r_o\beta_F}\right) + \frac{V_{CS}}{r_o(1+\beta_F)}}$$

$$\boxed{I_C = I_O + \frac{V_{CS}}{r_o(1+\beta_F)}} \rightarrow \boxed{I_O = \frac{\beta_F}{1+\beta_F}\left(1-\frac{R_E}{r_o\beta_F}\right)\left(\frac{V_{CC}\frac{R_2}{R_1+R_2} - V_{BE}}{R_E}\right)}$$

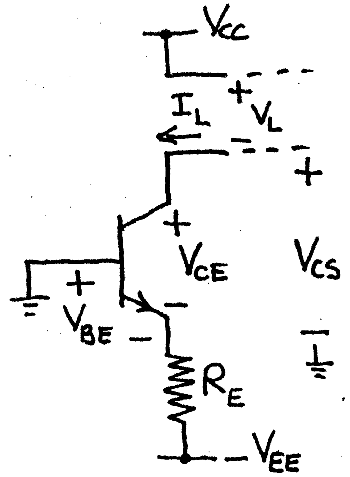


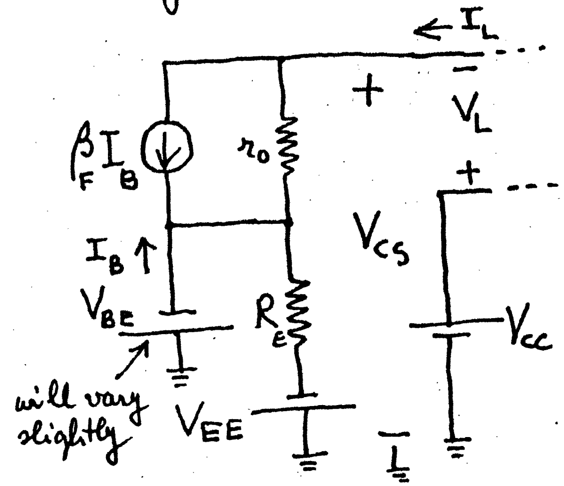


$V_{CE}sat - V_{BE} + V_{CC}\frac{R_2}{R_1+R_2} \leq V_{CS} \leq V_{CC}$

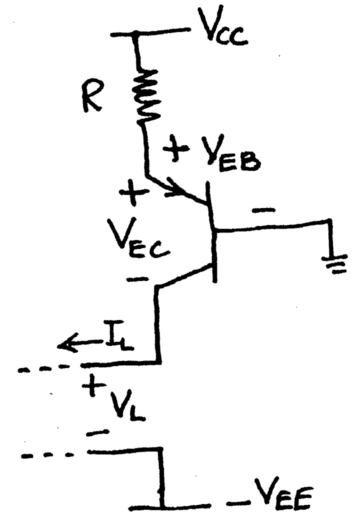
Note: Output resistance will actually be lower because $\begin{cases} V_{BE} \text{ is not const.} \\ R_{11} \neq 0 \end{cases}$

Current Sources using two power supplies





Similarly



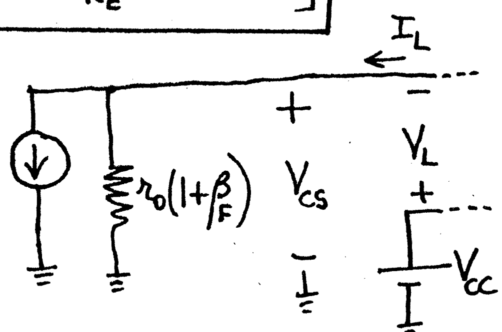
$$-V_{BE} = (I_B + I_L)R_E - V_{EE} \qquad I_B = \frac{V_{EE} - V_{BE}}{R_E} - I_L$$

$$V_{CS} = (I_L - \beta_F I_B) r_o - V_{BE} = I_L r_o - \beta_F r_o\left(\frac{V_{EE} - V_{BE}}{R_E} - I_L\right) - V_{BE}$$

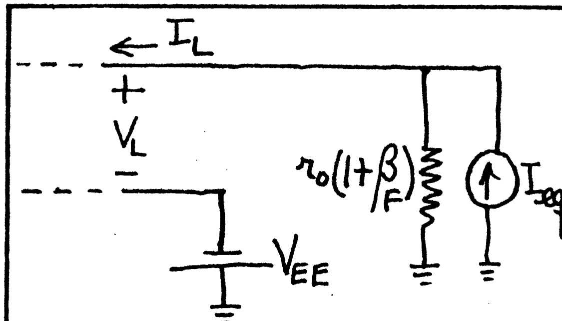
$$\boxed{I_L = \frac{V_{CS}}{r_o(1+\beta_F)} + \left[\frac{\beta_F}{1+\beta_F}\left(\frac{V_{EE} - V_{BE}\left(1 - \frac{R_E}{\beta_F r_o}\right)}{R_E}\right)\right]}$$

$$\frac{\beta_F}{1+\beta_F}\left[\frac{V_{EE} - V_{BE}\left(1 - \frac{R_E}{\beta_F r_o}\right)}{R_E}\right]$$

$$\cong \frac{V_{EE} - V_{BE}}{R_E}$$



$$0 \le V_L \le V_{cc} - V_{CEsat} + V_{BE}$$



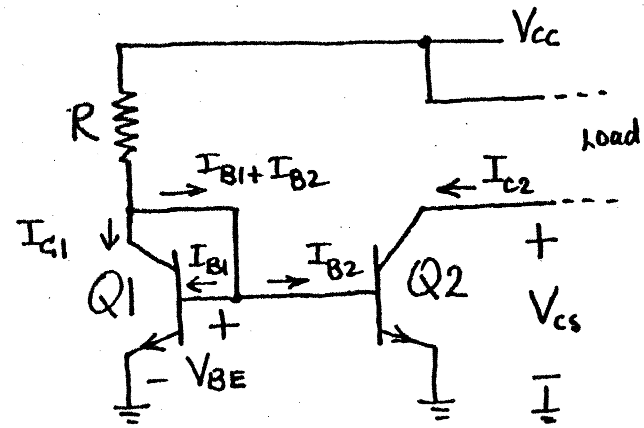
$$0 = V_L \le V_{EE} - V_{ECsat} + V_{EB}$$

$$I_{eq} = \frac{\beta_F}{1+\beta_F}\left[\frac{V_{CC} - V_{EB}\left(1 - \frac{R_E}{\beta_F r_o}\right)}{R_E}\right]$$

$$\cong \frac{V_{CC} - V_{EB}}{R_E}$$

Note: Actual output resistance will be lower because V_{BE} is not quite constant.

A simple current source for IC's using one power supply



In an IC, Q1 and Q2 are closely matched, i.e., their saturation currents are practically the same: $I_{S1} \cong I_{S2} = I_S$. Furthermore Q1 and Q2 are practically at the same temperature.

[In discrete transistors I's differ quite a lot, and it is difficult to put Q1 and Q2 in exactly the same temperature environment.]

Quick but approx. analysis

If we neglect $I_{B1}+I_{B2}$ relative to I_{C1}, we see that

$$I_{C1} = \frac{V_{CC} - V_{BE}}{R}$$

So, I_{C1} is fixed. Because of the strong negative feedback on Q1 (collector tied to base), I_{C1} is highly stabilized.

The collector current in a transistor is given by

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_A}\right)$$

If now we assume 1) identical transistors ($I_{S1} = I_{S2} = I_S$), ($V_{A1} = V_{A2} = V_A$) 2) $V_A = \infty$ and note that $V_{BE1} = V_{BE2} = V_{BE}$, we can at once write

$$\boxed{I_{C2} = I_{C1} = \frac{V_{CC} - V_{BE}}{R}} \qquad V_{CE2sat} \leq V_{CS} \leq V_{CC}$$

So the output current of the CS (current source) is solely determined by V_{CC}, V_{BE}, and R.

But <u>what is V_{BE}?</u> Roughly speaking V_{BE} is some number between 0.6 and 0.7 V. If desired, an accurate determination of V_{BE} can be made by solving the equation

$$\frac{V_{CC}-V_{BE}}{R} = I_S e^{\frac{V_{BE}}{V_T}}$$

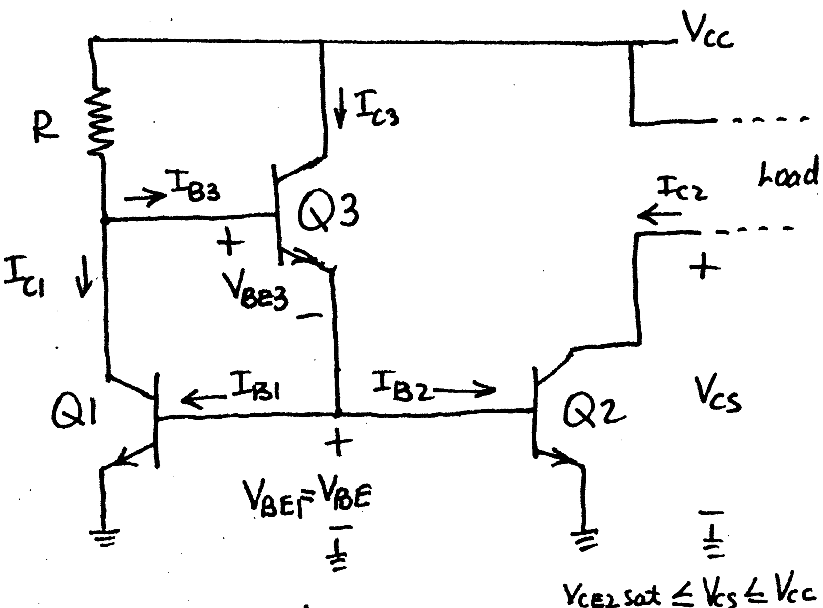
What if the two base currents are not negligible? (this situation arises particularly when PNP transistors with low β are used and the temperature may vary a lot.) In that case the current through R would be $I_{C1} + (I_{B1}+I_{B2}) =$

$$I_{C1} + 2I_{B1} = I_{C1}\left(1 + 2\frac{I_{B1}}{I_{C1}}\right) = I_{C1}\left(1+\frac{2}{\beta_F}\right).$$

Hence, $\dfrac{V_{CC}-V_{BE}}{R} = I_{C1}\left(1+\dfrac{2}{\beta_F}\right)$.

$$\boxed{I_{C2} = I_{C1} = \left(\frac{V_{CC}-V_{BE}}{R}\right)\left(\frac{1}{1+\frac{2}{\beta_F}}\right)}$$

If this β_F dependence of the output current is objectionable, another transistor, Q3, can be used to supply the two base currents as shown in the following circuit.



First, we determine V_{BE3}.

$$I_{C3} \cong I_{E3} = I_{B1}+I_{B2} = 2I_{B1} = \left.\frac{2I_{C1}}{\beta_F}\right|_{\beta_F=100} = \frac{2I_{C1}}{100}$$

Since it takes 18 mV in V_{BE} to double the collector current and −120 mV to reduce it by two orders of magnitude, we can write

$$V_{BE3} = V_{BE1} + 18\,\text{mV} - 120\,\text{mV} = V_{BE1} - 102\,\text{mV} \cong V_{BE1}$$

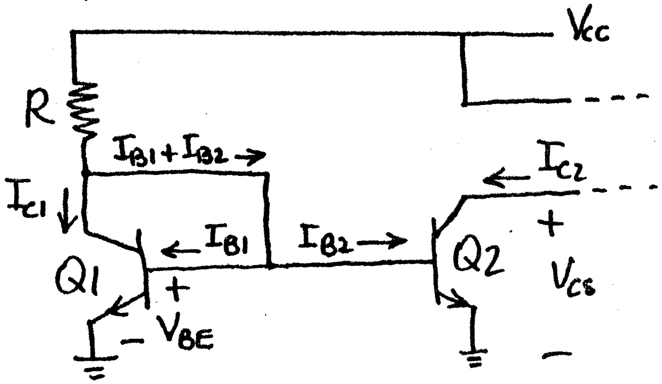
Hence $\dfrac{V_{CC}-2V_{BE}}{R} = I_{C1} + I_{B3} = I_{C1} + \dfrac{2I_{B1}}{1+\beta_F} = I_{C1}\left(1+\dfrac{2/\beta_F}{1+\beta_F}\right)$

$$\boxed{I_{C2} = I_{C1} = \left(\frac{V_{CC}-2V_{BE}}{R}\right)\left(\frac{1}{1+\frac{2}{\beta_F+\beta_F^2}}\right)}$$

← Note the much-reduced β_F-dependence of I_{C2}.

Output equivalent circuit

More accurate analysis that includes V_A.



$$\frac{V_{CC}-V_{BE}}{R} = I_{C1}+I_{B1}+I_{B2} = I_{C1} + \frac{2 I_S e^{\frac{V_{BE}}{V_T}}}{\beta_F}$$

But $I_{C1} = I_S e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{BE}}{V_A}\right)$

So, $\dfrac{V_{CC}-V_{BE}}{R} = I_S e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{BE}}{V_A}\right) + \dfrac{2 I_S e^{\frac{V_{BE}}{V_T}}}{\beta_F}$

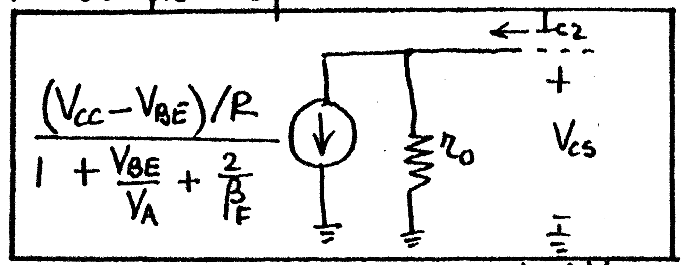
which gives $I_S e^{\frac{V_{BE}}{V_T}} = \dfrac{(V_{CC}-V_{BE})/R}{1+\frac{V_{BE}}{V_A}+\frac{2}{\beta_F}}$

But $I_{C2} = I_S e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE2}}{V_A}\right) = I_S e^{\frac{V_{BE}}{V_T}} + \dfrac{V_{CE2}}{r_o}$

where $r_o = V_A / I_S e^{\frac{V_{BE}}{V_T}}$

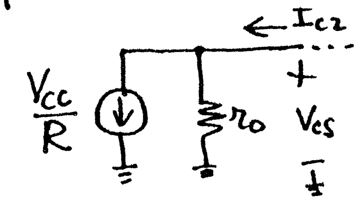
Hence, $\boxed{I_{C2} = \dfrac{(V_{CC}-V_{BE})/R}{1+\frac{V_{BE}}{V_A}+\frac{2}{\beta_F}} + \dfrac{V_{CE2}}{r_o}}$

The output equivalent circuit is:



$V_{CE2sat} \le V_{CS} \le V_{CC}$

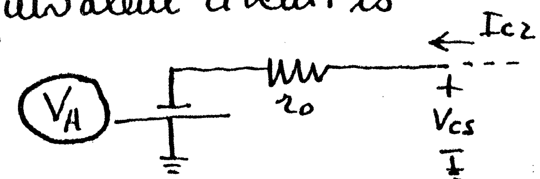
For $V_{CC} \gg V_{BE}$, $V_A \gg V_{BE}$, and $\beta_F \gg 2$, this equivalent circuit can be approx. by



The resulting open-circuit voltage is

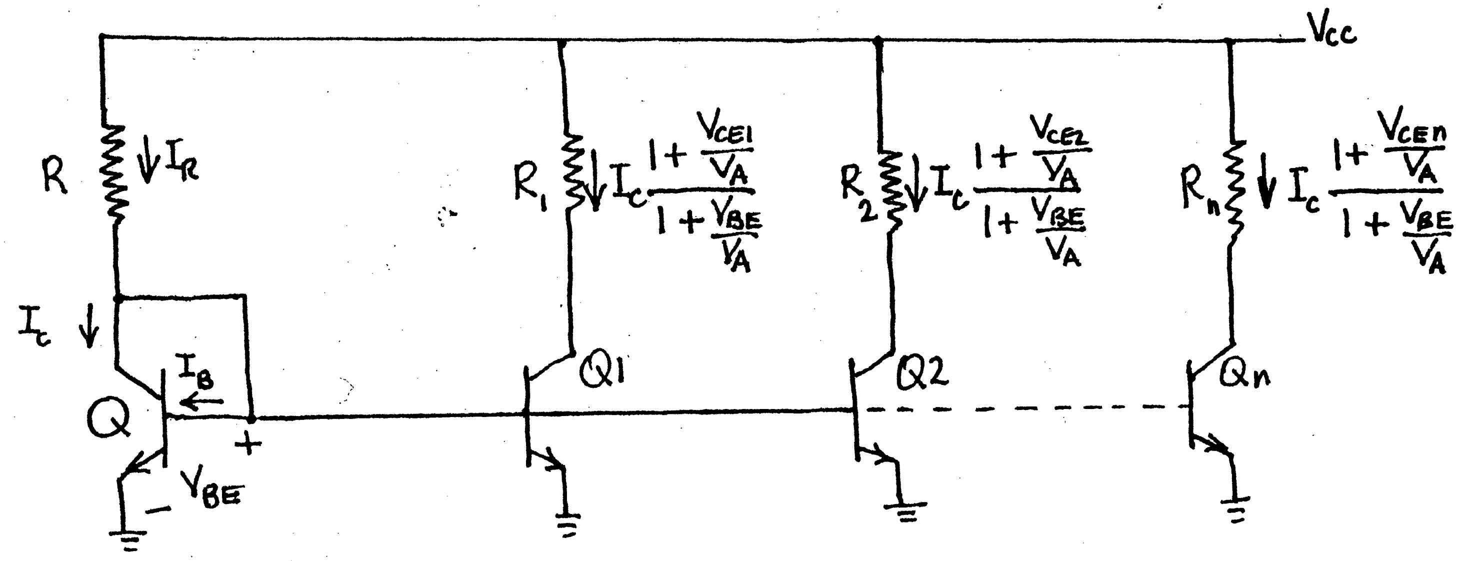
$$V_{OC} = -\frac{V_{CC}}{R} r_o \cong - I_{C1} r_o \cong - I_{C1}\frac{V_A}{I_{C1}} = -V_A$$

Hence, the approx. Thévenin output equivalent circuit is



Thus, this CS can be realized equivalently if a voltage source of value V_A were available. The CS uses only V_{CC}.

L9: Obtaining two or more equal current sources

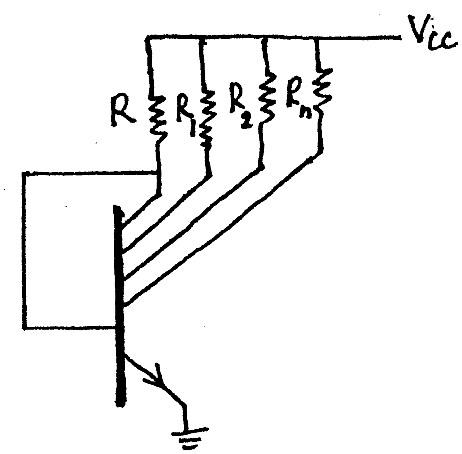


$$I_R = \frac{V_{CC} - V_{BE}}{R} = I_C + (n+1) I_B = I_C + (n+1)\frac{I_C}{\beta_F}$$

$$\boxed{I_C = \frac{(V_{CC} - V_{BE})/R}{1 + \frac{n+1}{\beta_F}}}$$

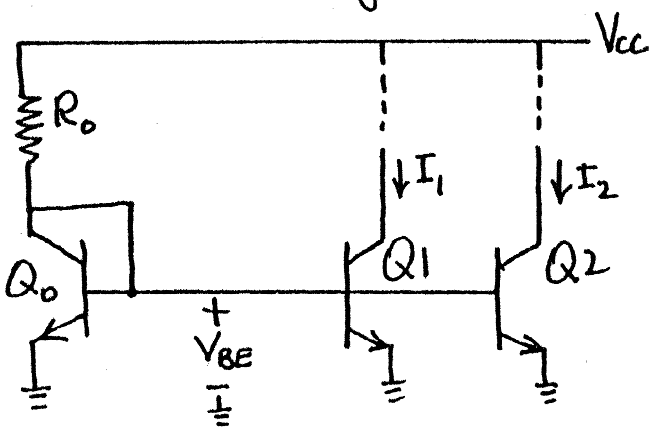
$$\left.\begin{aligned} I_C &= I_S e^{\frac{V_{BE}}{V_T}}\left(1 + \frac{V_{BE}}{V_A}\right) \\ I_{Ci} &= I_S e^{\frac{V_{BE}}{V_T}}\left(1 + \frac{V_{CEi}}{V_A}\right) \end{aligned}\right\} \quad \boxed{\frac{I_{Ci}}{I_C} = \frac{1 + \frac{V_{CEi}}{V_A}}{1 + \frac{V_{BE}}{V_A}}}$$

Since all bases are connected together and all emitters are grounded, the circuit can be redrawn as



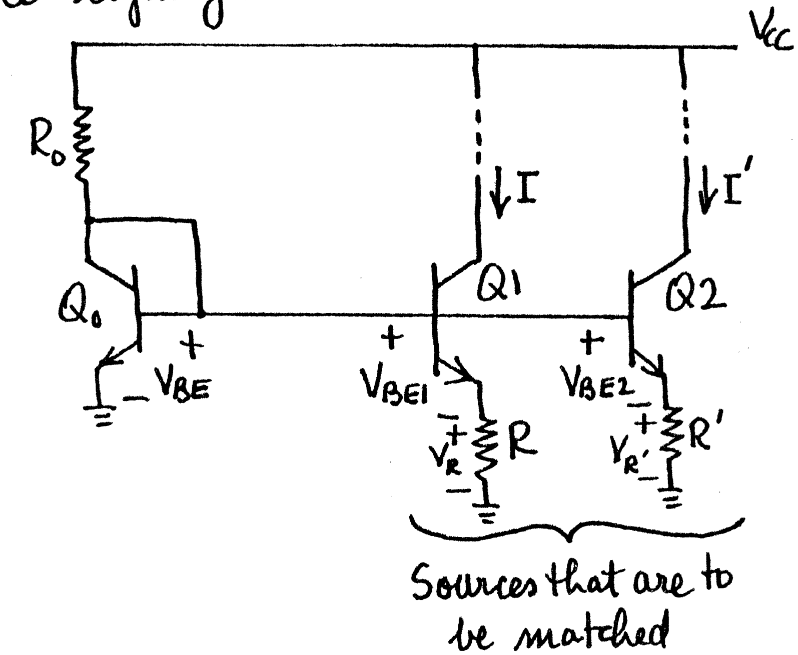
Mismatches in current sources

A circuit for obtaining two identical current sources is given below.



If Q1 is perfectly matched to Q_2 and $V_{CE1} = V_{CE2}$, then $I_1 = I_2$. However, even under the best of circumstances, Q1 and Q2 are not identical. Their saturation currents (I_S) will be slightly different. [Their α_F's will differ slightly too. (Recall that $I_C = \alpha_F I_E = \frac{\beta_F}{1+\beta_F} I_E$.)] Consequently I_2 will not exactly equal to I_1.

A better current match is obtained if resistors are inserted in the emitter leads. The slightly modified circuit is



I' will differ from I, i.e., $I' = I + \Delta I$, because

$$\begin{Bmatrix} I_S' = I_S + \Delta I_S \\ \alpha_F' = \alpha_F + \Delta \alpha_F \\ R' = R + \Delta R \end{Bmatrix}$$

To calculate ΔI, we proceed as follows:

$$V_{BE} = V_{BE1} + V_R = V_{BE2} + V_{R'}$$

But $V_{BE1} = V_T \ln\left(\frac{I}{I_S}\right)$, $V_{BE2} = V_T \ln\left(\frac{I'}{I_S'}\right)$

and $V_R = \frac{I}{\alpha_F} R$, $V_{R'} = \frac{I'}{\alpha_F'} R'$. Hence

$$V_T \ln\left(\frac{I}{I_S}\right) + \frac{I}{\alpha_F} R = V_T \ln\left(\frac{I'}{I_S'}\right) + \frac{I'}{\alpha_F'} R'.$$

$$= V_T \ln\left(\frac{I+\Delta I}{I_S + \Delta I_S}\right) + \left(\frac{I+\Delta I}{\alpha_F + \Delta\alpha_F}\right)(R+\Delta R)$$

Rearranging, we obtain

$$V_T \ln\left[\left(\frac{I}{I_S}\right)\left(\frac{I_S+\Delta I_S}{I+\Delta I}\right)\right] = \left(\frac{I+\Delta I}{\alpha_F+\Delta\alpha_F}\right)(R+\Delta R) - \frac{I}{\alpha_F} R$$

$$V_T \ln\left[\frac{1+\frac{\Delta I_S}{I_S}}{1+\frac{\Delta I}{I}}\right] = \frac{IR}{\alpha_F}\left[\left(\frac{1+\frac{\Delta I}{I}}{1+\frac{\Delta\alpha_F}{\alpha_F}}\right)\left(1+\frac{\Delta R}{R}\right) - 1\right]$$

$$V_T \ln\left(1+\frac{\Delta I_S}{I_S}\right) - V_T \ln\left(1+\frac{\Delta I}{I}\right) = \frac{IR}{\alpha_F}\left[\frac{\left(\frac{\Delta R}{R} + \frac{\Delta I}{I} - \frac{\Delta\alpha_F}{\alpha_F} + \frac{\Delta I}{I}\frac{\Delta R}{R}\right)}{1+\frac{\Delta\alpha_F}{\alpha_F}}\right]$$

Using the approximations $\ln(1+x) \cong x$ and $\frac{1}{1+x} \cong 1-x$ for $|x|$ small and neglecting second-order effects, we obtain

$$V_T\left(\frac{\Delta I_S}{I_S} - \frac{\Delta I}{I}\right) \cong \frac{IR}{\alpha_F}\left(\frac{\Delta R}{R} + \frac{\Delta I}{I} - \frac{\Delta\alpha_F}{\alpha_F}\right)$$

Since $\frac{I}{V_T} = g_m$, this result can be written as

$$\boxed{\frac{\Delta I}{I} = \left(\frac{1}{1+\frac{g_m R}{\alpha_F}}\right)\frac{\Delta I_S}{I_S} + \left(\frac{\frac{g_m R}{\alpha_F}}{1+\frac{g_m R}{\alpha_F}}\right)\frac{\Delta R}{R} - \left(\frac{\frac{g_m R}{\alpha_F}}{1+\frac{g_m R}{\alpha_F}}\right)\frac{\Delta\alpha_F}{\alpha_F}}$$

Typical mismatches are $\begin{cases} \pm 10\% \text{ to } \pm 1\% \text{ for } \frac{\Delta I_S}{I_S} \\ \pm 2\% \text{ to } \pm 0.1\% \text{ for } \frac{\Delta R}{R} \\ \pm 0.1\% \text{ NPN}, \pm 1\% \text{ PNP for } \frac{\Delta\alpha_F}{\alpha_F} \end{cases}$

<u>Case 1</u>: $\frac{g_m R}{\alpha_F} \ll 1$ (special case: $R=0$)

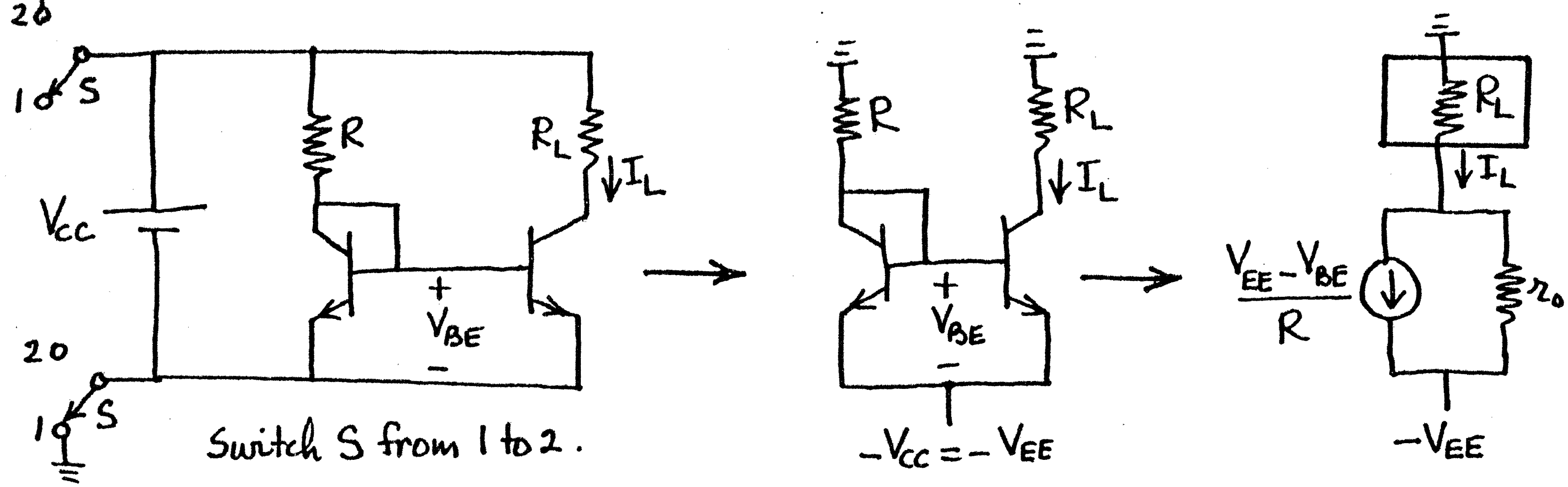
$\boxed{\frac{\Delta I}{I} \simeq \frac{\Delta I_S}{I_S}}$ — mismatches in sat. currents determine primarily mismatches in the CS's.

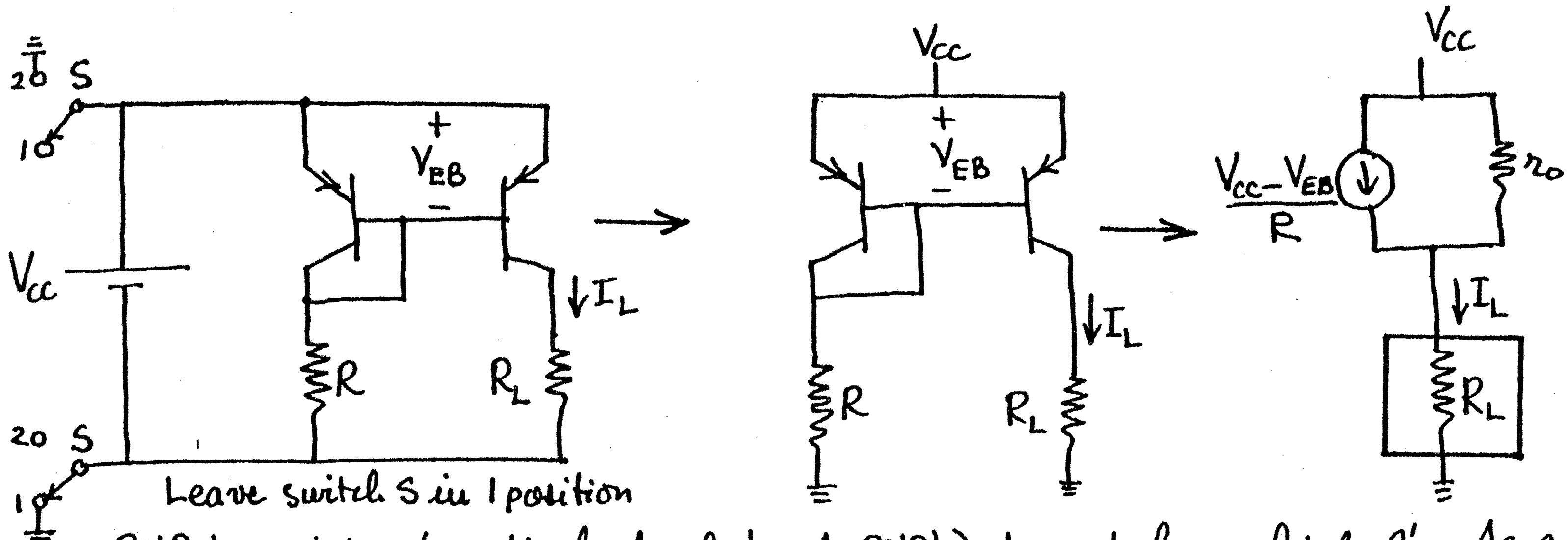
<u>Case 2</u>: $\frac{g_m R}{\alpha_F} \gg 1$

$\boxed{\frac{\Delta I}{I} \simeq \frac{\Delta R}{R} - \frac{\Delta\alpha_F}{\alpha_F}}$ — mismatches in R and α_F determine primarily mismatches in the CS's.

Since $\frac{\Delta R}{R} - \frac{\Delta\alpha_F}{\alpha_F}$ is generally less than $\frac{\Delta I_S}{I_S}$, <u>adding emitter resistors and making $g_m R \gg \alpha_F$ result in better current equalization.</u>

Current sources driving grounded loads

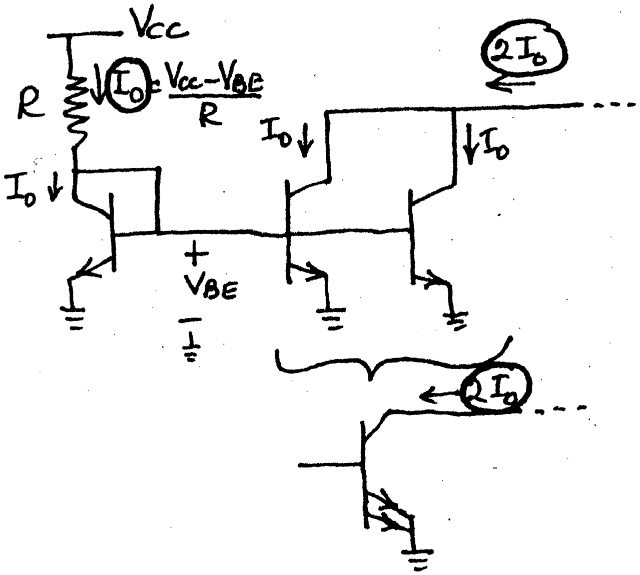


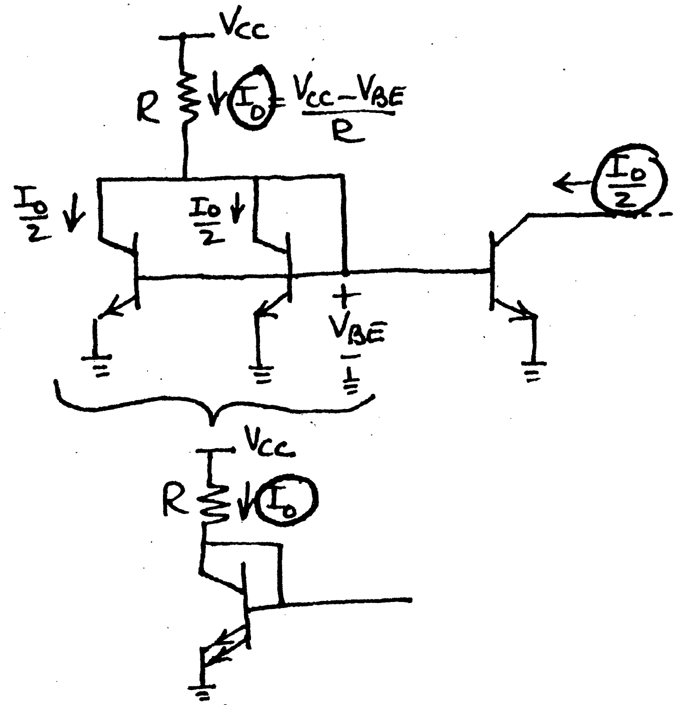


PNP transistors (particularly lateral PNP's) do not have high β_F's. As a result, the base currents may not be negligible. If so, use the more accurate values given on p62.

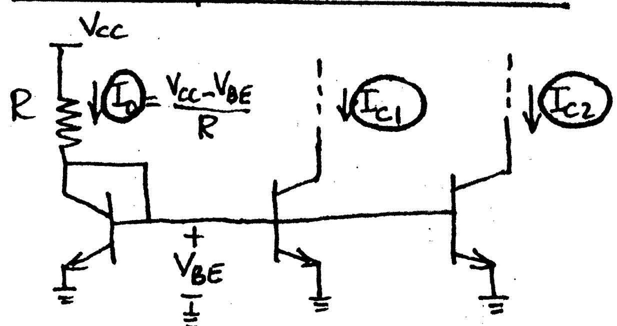
Obtaining unequal currents

1. Use parallel connections



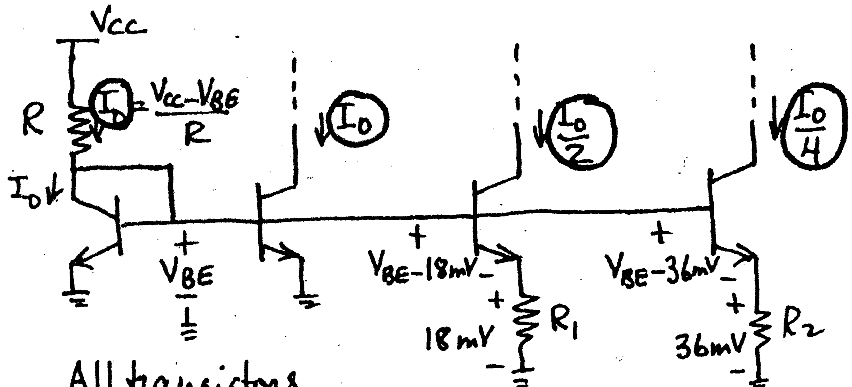


2. Use unequal emitter areas



$$\left.\begin{aligned} I_{C1} &= I_{S1}\, e^{\frac{V_{BE}}{V_T}} \\ I_{C2} &= I_{S2}\, e^{\frac{V_{BE}}{V_T}} \end{aligned}\right\} \qquad \boxed{I_{C2} = I_{C1}\,\frac{I_{S2}}{I_{S1}}}$$

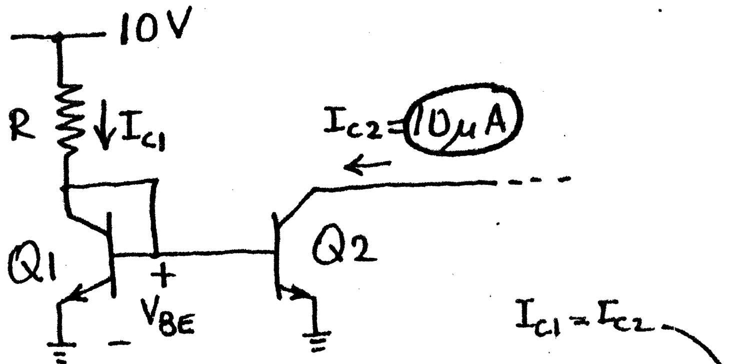
3. Use emitter resistors



All transistors have the same I_S: $\boxed{\frac{I_0}{2}R_1 \cong 18mV}$ $\boxed{\frac{I_0}{4}R_2 \cong 36mV}$

Designing a 10µA current source

1. Use basic circuit



Assume $I_{S1}=I_{S2}=I_S$ and $V_A=\infty$. Further assume that the base currents are negligible!

$$V_{BE}=V_T \ln \frac{I_{C1}}{I_S} = 26 \ln \frac{10\times10^{-6}}{I_S}$$

Assume I_S is such that $V_{BE}=600\ mV$. Then

$$R=\frac{10-0.6}{10\mu A}=\boxed{940K}$$

This is too costly a solution because of the large die area required for 940K.

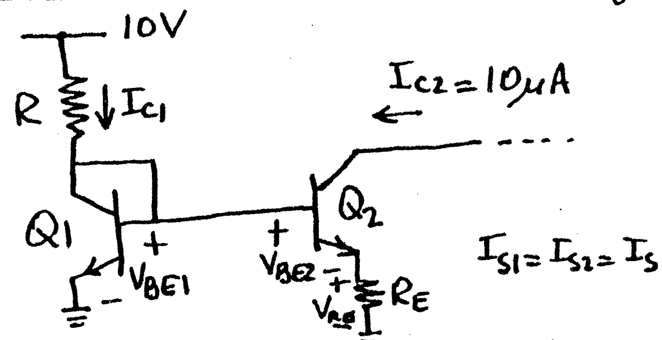
2. Make emitter areas of Q1 and Q2 in the ratio of 10:1. This will require $I_{S1}=10I_{S2}=10I_S$. Since $I_{C1}=I_{S1}e^{\frac{V_{BE}}{V_T}}$ and $I_{C2}=I_{S2}e^{\frac{V_{BE}}{V_T}}$, we have

$$I_{C1}=I_{C2}\left(\frac{I_{S1}}{I_{S2}}\right)=10\mu A(10)=100\mu A$$

Since both I_{C1} and I_{S1} have gone up by a factor of 10, V_{BE} stays the same, i.e., 0.6V.

$$R=\frac{10-0.6}{100\mu A}=\boxed{94K}$$

3. Add a resistor in the emitter of Q_2



To keep to size of R down, make I_{C1} large, say 1mA. Since I_{C1} is 100x larger than previously, V_{BE1} will be 120mV higher, i.e., $V_{BE1}=720mV$.

$$R=\frac{10-0.72}{1mA}=\boxed{9.28K}$$

Since I_{C2} is still the same, $V_{BE2}=600mV$.

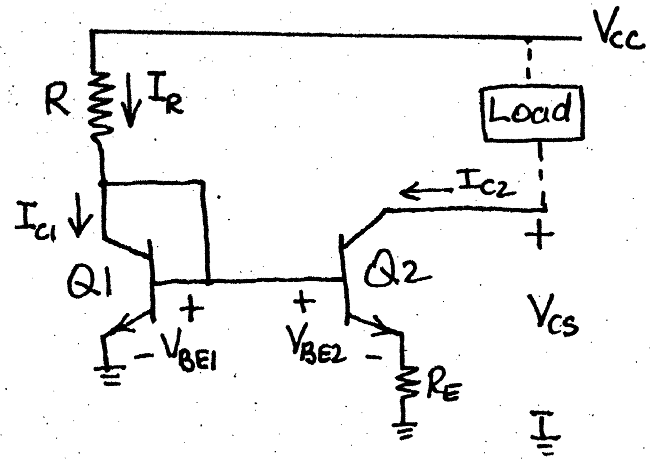
Hence $V_{RE}=V_{BE1}-V_{BE2}=720-600=120mV$.

But $V_{RE}\cong 10\mu A\ R_E$. Hence $R_E=120mV/10\mu A=\boxed{12K}$

Total resistance of circuit $=9.28K+12K=21.28K$.

Total die area required is quite reasonable.

The Widlar current source



$$V_{CE2sat} - V_{BE2} + V_{BE1} \leq V_{CS} \leq V_{CC}$$

Assume $V_A \gg V_{BE}$ and neglect the base currents. By inspection we see that

$$\boxed{I_{C1} = I_R = \frac{V_{CC} - V_{BE1}}{R}}$$

We can assume a V_{BE1}, say 0.6V, and use the above equation to determine I_{C1}. Using this I_{C1}, a more accurate determination of V_{BE1} can be made as follows:

$$\boxed{V_{BE1} = V_T \ln \frac{I_{C1}}{I_{S1}}}$$

Note that Q2 has no effect on the V_{BE1} determination because I_{B2} has been neglected.

Assuming $I_{E2} \cong I_{C2}$, we see that

$$V_{BE1} \cong V_{BE2} + I_{C2} R_E$$

Since V_{BE1} is fixed by I_{C1}, which is fixed by I_R, an increase of R_E from zero will result in a decrease of V_{BE2} which will cause a reduction of I_{C2} relative to I_{C1}. Thus current sources of small current can be generated.

Solving for R_E, we obtain $R_E = \dfrac{V_{BE1} - V_{BE2}}{I_{C2}}$.

$$R_E = \frac{V_T\left(\ln \frac{I_{C1}}{I_{S1}} - \ln \frac{I_{C2}}{I_{S2}}\right)}{I_{C2}} = \boxed{\frac{V_T \ln\left(\frac{I_{C1}}{I_{C2}} \frac{I_{S2}}{I_{S1}}\right)}{I_{C2}}}$$

This equation gives the value of R_E for obtaining the desired I_{C2} for a given $\frac{I_{C1}}{I_{C2}}$ ratio.

Advantages of the Widlar CS

1. CS's of small value can be generated without the use of large resistances.
2. Because of R_E, the output current is less dependent on V_{CC}.
3. Because of R_E, the output resistance of the CS is higher.

Power supply dependence of the Widlar CS

For $I_{S1}=I_{S2}$, the output current I_{C2} is given by

$$I_{C2}=\frac{V_T}{R_E}\ln\left(\frac{I_{C1}}{I_{C2}}\right)=\frac{V_T}{R_E}\ln\left[\frac{(V_{CC}-V_{BE1})/R}{I_{C2}}\right]$$

$$=\frac{V_T}{R_E}\left[\ln(V_{CC}-V_{BE1})-\ln(I_{C2}R)\right]$$

Note that I_{C2} appears on both sides of the above equation. To see how it varies with V_{CC}, we differentiate I_{C2} with respect to V_{CC}. In so doing, we will ignore the slight dependence of V_{BE1} on V_{CC} and assume V_{BE1} to be constant.

$$\frac{\partial I_{C2}}{\partial V_{CC}}=\frac{V_T}{R_E}\left[\frac{1}{V_{CC}-V_{BE1}}-\frac{R\frac{\partial I_{C2}}{\partial V_{CC}}}{I_{C2}R}\right]$$

Solving for the derivative we obtain

$$\frac{\partial I_{C2}}{\partial V_{CC}}=\frac{\frac{V_T}{R_E}\left(\frac{1}{V_{CC}-V_{BE1}}\right)}{1+\frac{V_T}{I_{C2}R_E}}=\frac{I_{C2}\left(\frac{1}{V_{CC}-V_{BE1}}\right)}{1+\frac{I_{C2}R_E}{V_T}}$$

It is more meaningful to look at changes on a per unit basis rather than absolute. Therefore, we multiply both sides by $\frac{V_{CC}}{I_{C2}}$ and obtain

$$\frac{\frac{\partial I_{C2}}{I_{C2}}}{\frac{\partial V_{CC}}{V_{CC}}}=\left(\frac{V_{CC}}{V_{CC}-V_{BE1}}\right)\left(\frac{1}{1+\frac{I_{C2}R_E}{V_T}}\right)\Bigg|_{V_{CC}\gg V_{BE1}}$$

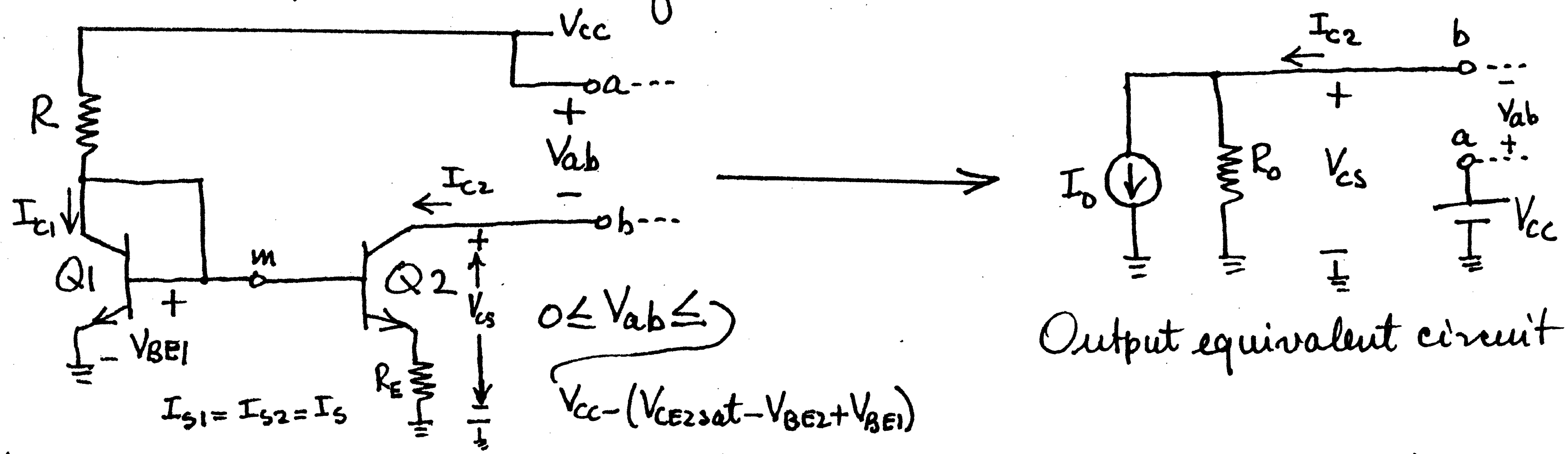
$$\cong\frac{1}{1+\frac{I_{C2}R_E}{V_T}}=\frac{1}{1+g_mR_E}$$

This result in incremental form is

$$\boxed{\frac{\Delta I_{C2}}{I_{C2}}\cong\frac{1}{1+g_mR_E}\,\frac{\Delta V_{CC}}{V_{CC}}}$$

If $R_E=0$, a 10% change in V_{CC} will cause a 10% change in I_{C2}. On the other hand, if $g_mR_E=3$, a 10% change in V_{CC} will cause only a 2.5% change in I_{C2}. <u>The larger g_mR_E, the less is the power supply dependence.</u>

L10: Output equivalent circuit of Widlar current source



Output equivalent circuit

<u>In design</u>, I_o is the desired output current and is therefore known. $I_o = I_{C2}\big|_{V_{CS}=0} \cong I_{C2}$. This desired I_o is obtained by determining the R and R_E values for a <u>preselected I_{C1}</u> using the equations

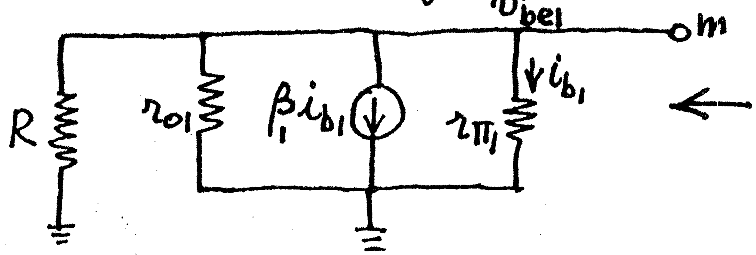
$$\left\{\begin{aligned} R &= \frac{V_{CC} - \overbrace{V_T \ln(I_{C1}/I_S)}^{V_{BE1}}}{I_{C1}} \\ R_E &= \frac{V_T \ln(I_{C1}/I_o)}{I_o} \end{aligned}\right\}$$

These equations are based on the assumptions that 1) base currents are negligible 2) $V_{CE} \ll V_A$. This latter assumption is quite valid since $V_{CE1} = V_{BE1}$ and $V_{CE2} \cong 0$. (Note from the output equivalent circuit that $I_o = I_{C2}$ when $V_{CS} = 0$.)

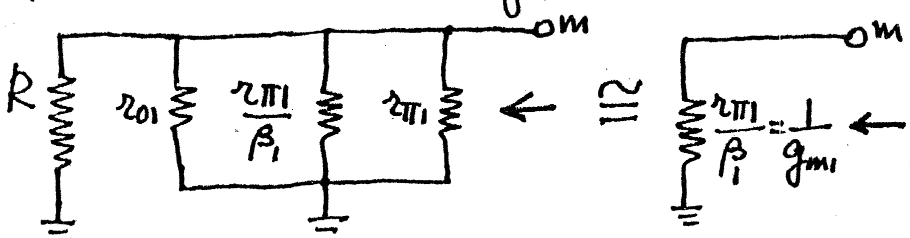
Determination of R_o

As the load on the CS varies, I_{C2} would vary. However, we know that this variation is going to be very small. Consequently, the four transistor parameters r_π, g_m, r_o and β would change very little as the entire dynamic range of the CS ($V_{CE2sat} - V_{BE2} + V_{BE1} \le V_{CS} \le V_{CC}$) is covered. Hence, the R_o determination based on the small-signal model of the transistors can be expected to hold over a wide operating range as the load on the current source varies.

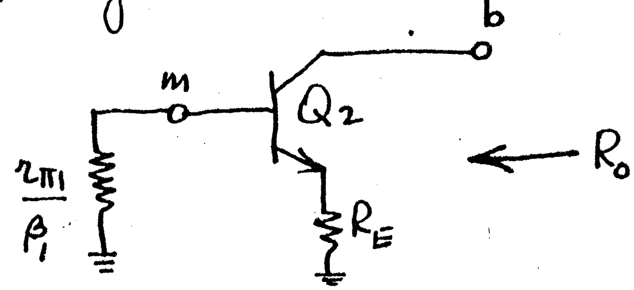
The resistance seen to the left of the midpoint m is calculated using the small-signal model of Q1.



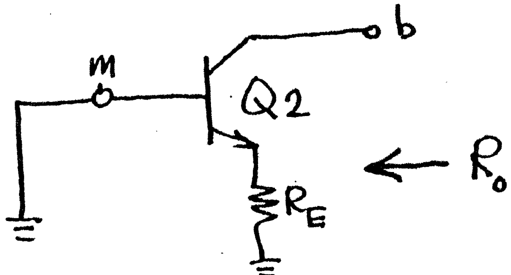
Since $\beta_1 i_{b_1} = \beta_1 \dfrac{v_{be1}}{r_{\pi 1}} = \dfrac{v_{be1}}{r_{\pi 1}/\beta_1}$, the dependent current source $\beta_1 i_{b_1}$ can be replaced by an equivalent resistance of $r_{\pi 1}/\beta_1$.



Using this <u>small</u> resistance as the base-to-ground resistance of Q_2, we can draw the remaining circuit as



$\frac{r_{\pi 1}}{\beta_1}$ is in series with $r_{\pi 2}$. Because $I_{C2} < I_{C1}$, $r_{\pi 2}$ is greater than $r_{\pi 1}$. Hence, $\frac{r_{\pi 1}}{\beta_1}$ can be altogether neglected and the circuit associated with Q_2 redrawn as



This says that the base-to-ground voltage is established as V_{BE1} by Q1 and is not affected to any significant extend by the output current.

R_o can be calculated using the general equation given on p37.

$$R_o = r_{o2}\left[1 + \frac{\beta_2 R_E\left(1+\frac{r_{\pi 2}}{\beta_2 r_{o2}}\right)}{r_{\pi 2}+R_E}\right]$$

Since $\dfrac{r_{\pi 2}}{\beta_2 r_{o2}} = \dfrac{V_T/I_{B2}}{\beta_2 (V_A+V_{CE2})/I_{C2}} = \dfrac{V_T}{V_A+V_{CE2}} \ll 1$,

the expression for R_o can be simplified to

$$R_o = r_{o2}\left(1+\frac{\beta_2 R_E}{r_{\pi 2}+R_E}\right) = r_{o2}\left(1+\frac{g_{m2}R_E}{1+\frac{R_E}{r_{\pi 2}}}\right)$$

But $\dfrac{R_E}{r_{\pi 2}} \simeq \dfrac{I_{C2}R_E}{I_{C2}r_{\pi 2}} = \dfrac{I_{C2}R_E}{\beta_2 I_{B2} r_{\pi 2}} = \dfrac{V_{R_E}}{\beta_2 V_T} \ll 1$,

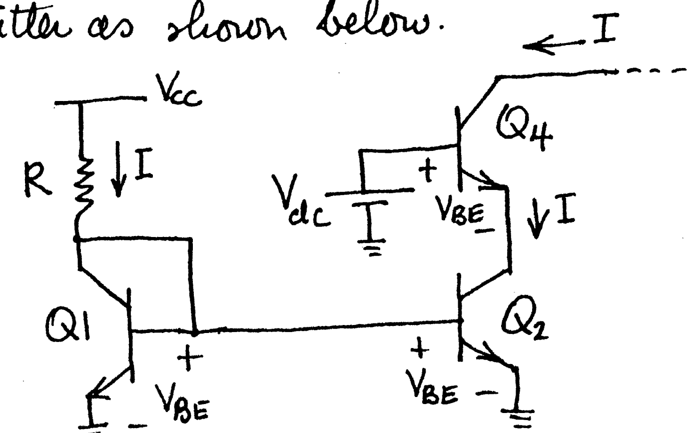
because V_{R_E} is of the order of 120 mV (for $I_{C2} = \frac{1}{100} I_{C1}$) or less and $\beta_2 V_T$ is of the order of 2600 mV (for $\beta_2 = 100$). Hence, R_o can be further simplified to

$$\boxed{R_o = r_{o2}(1+g_{m2}R_E) = r_{o2}\left(1+\frac{I_{C2}R_E}{V_T}\right)}$$

For $g_{m2}R_E = 3$, R_o of the CS is 4x higher than the R_o of a CS of the same value with $R_E = 0$.

The cascode current source

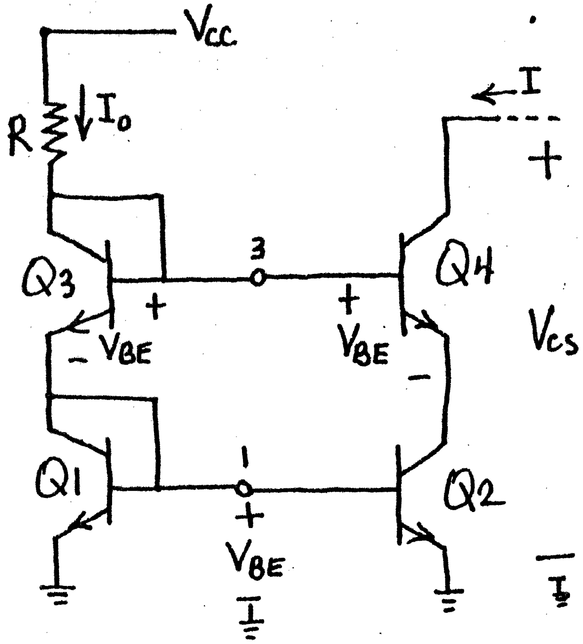
The larger the resistance that is inserted in the emitter of the output transistor, the larger becomes the output resistance of the current source. Instead of using an actual resistance, a large effective (equivalent) resistance can be created using a current source in the emitter as shown below.

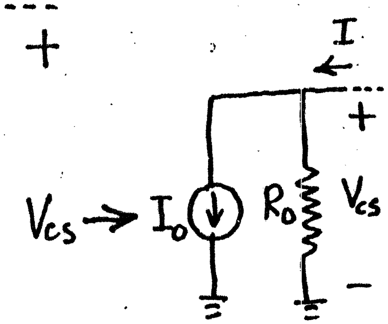


I_B's are assumed negligible; $V_A = \infty$.

Q1 sets the current I. Q2 acts as effective resistance in the emitter of Q4 which acts as the current source. $V_{dc} > V_{BE} + V_{CEsat}$.

To generate V_{dc}, add another transistor Q_3.

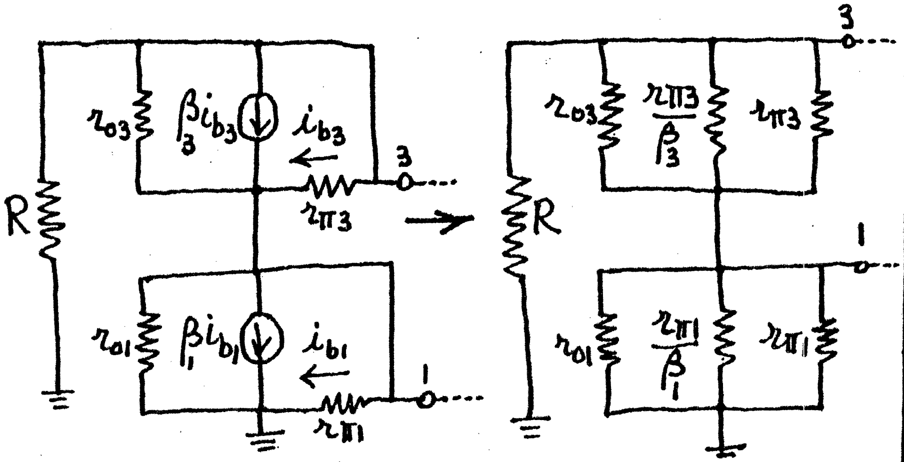




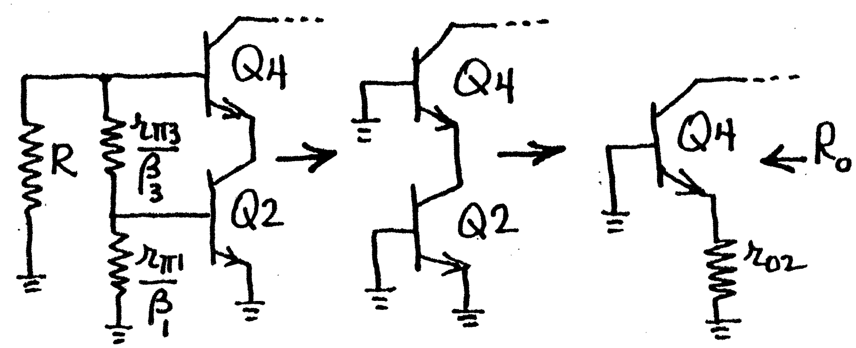
$V_{CE4sat} + V_{BE} < V_{CS} \le V_{CC}$

$$\boxed{I_o \cong \frac{V_{CC}-2V_{BE}}{R}}$$

Again, the small-signal models can be used since the currents remain practically constant as the load on the CS changes.



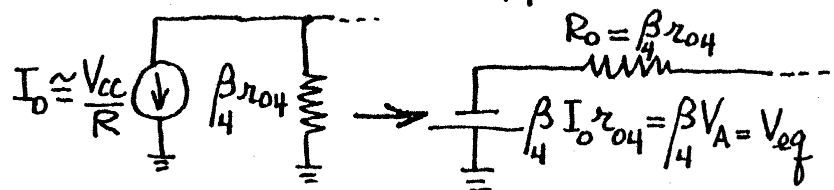
$r_o \gg r_\pi \gg \frac{r_\pi}{\beta} \quad \left(\frac{V_A+V_{CE}}{I_C} \gg \frac{\beta V_T}{I_C} \gg \frac{V_T}{I_C}\right)$



Using the results on p37, we obtain

$$\boxed{R_o = r_{o4}\left[1 + \frac{r_{o2}\left(\beta_4 + \frac{r_{\pi4}}{r_{o4}}\right)}{r_{\pi4} + r_{o2}}\right] \cong r_{o4}(1+\beta_4)}$$

If we assume $V_{CC} \gg 2V_{BE}$, $\beta_4 \gg 1$, then



For $I_o = 100\mu A$, $V_A = 100V$, and $\beta_4 = 100$

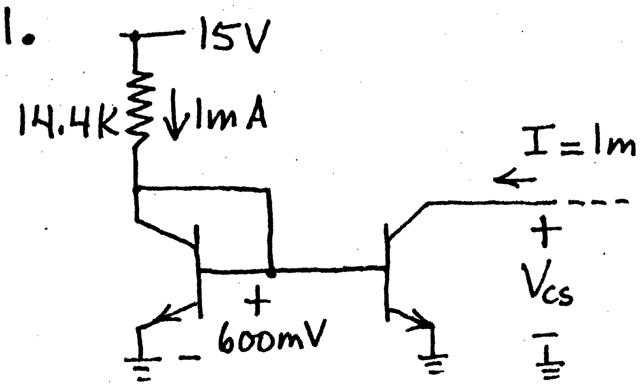
$V_{eq} = \beta_4 V_A = 100 \times 100 = \underline{10KV}$

$R_o = \beta_4 r_{o4} = \beta_4 \frac{V_A}{I_o} = 100 \times \frac{100}{100\mu A} = \underline{100 M\Omega}$

When the resulting R_o is so high, parasitic effects, not considered here, must be included.

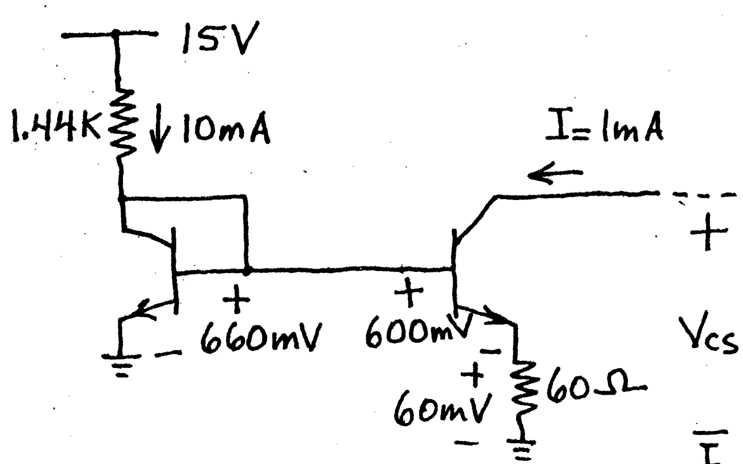
Three 1 mA current sources – Demonstration

1.



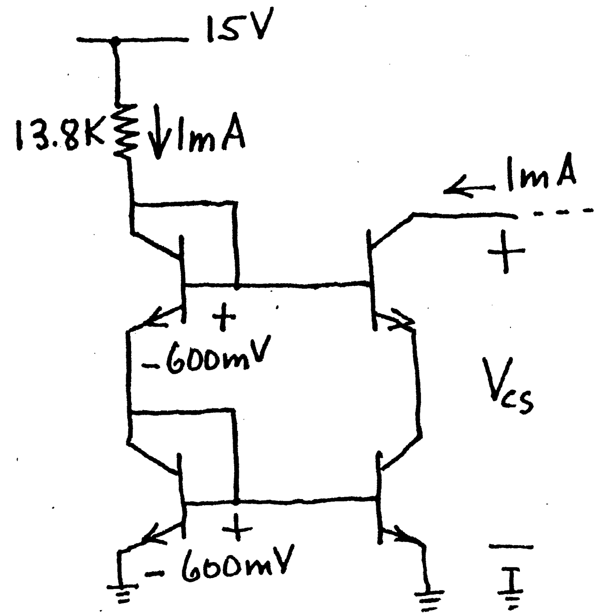
$$R_o = r_o = \frac{V_A}{I} = \frac{100\,V}{1mA} = 100K$$

2.

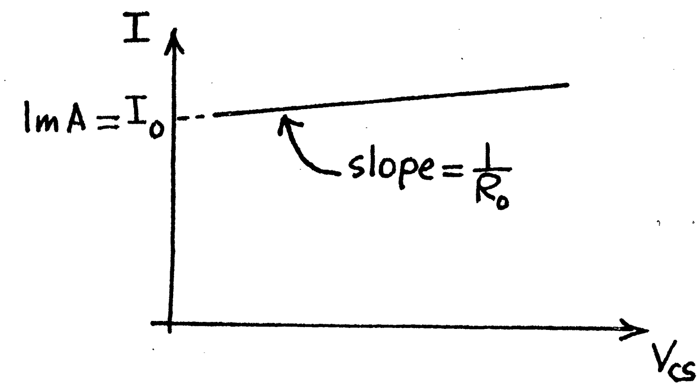


$$R_o = r_o\left(1 + g_m R_E\right) = 100\left(1 + \frac{1mA}{26mV} \times 60\right) = 330K$$

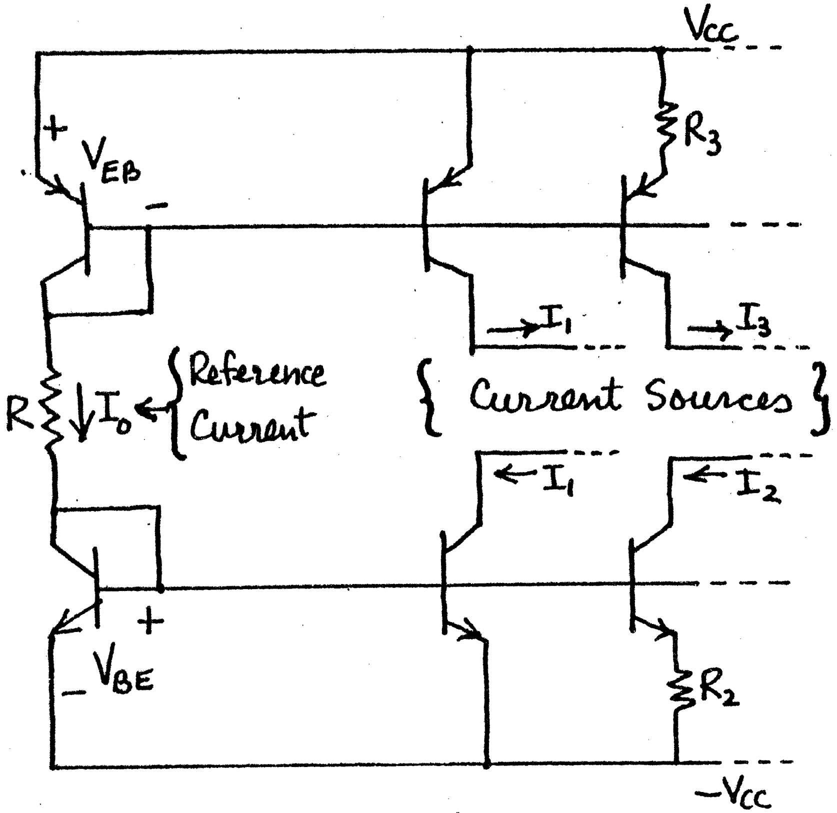
3.



$$R_o = \beta r_o \cong 100 \times 100K = 10M$$



Current sources using a common reference



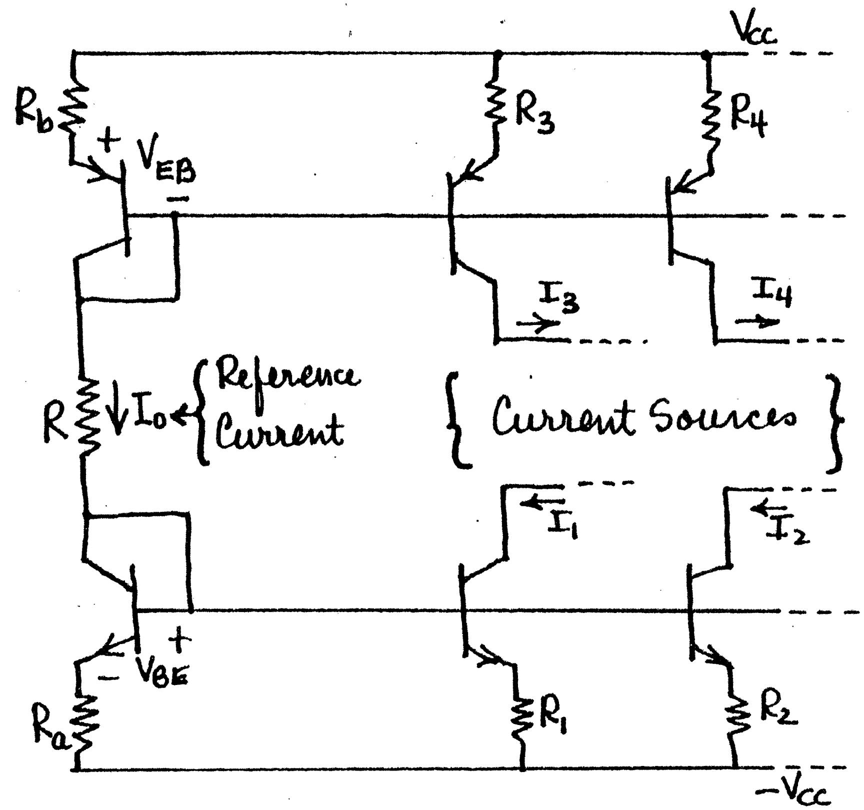
Assume identical I_S's and neglect I_B's.

$$\boxed{I_o = \frac{2V_{CC} - 2V_{BE}}{R}}$$

$$I_1 = I_o$$

$$I_2 = \frac{V_T}{R_2} \ln \frac{I_o}{I_2} \longleftarrow I_2 < I_o$$

$$I_3 = \frac{V_T}{R_3} \ln \frac{I_o}{I_3} \longleftarrow I_3 < I_o$$

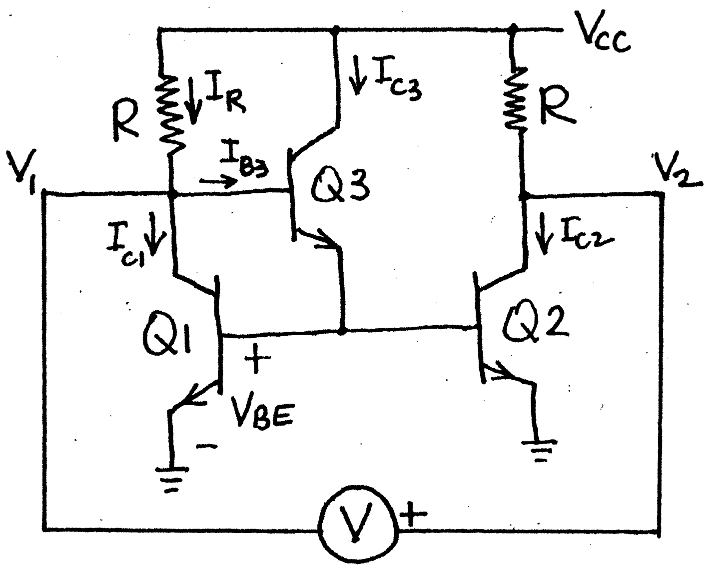


Assume identical I_S's and neglect I_B's.

$$\boxed{I_o = \frac{2V_{CC} - 2V_{BE}}{R_a + R + R_b}}$$

$I_1 > I_o$	if	$R_1 < R_a$
$I_2 < I_o$	if	$R_2 > R_a$
$I_3 > I_o$	if	$R_3 < R_b$
$I_4 < I_o$	if	$R_4 > R_b$

A check for matched transistors



This circuit can be used to see whether Q1 and Q2 are matched.

The purpose of Q3 is to supply the base currents of Q1 and Q2 via I_{C3} by taking a negligibly small base current $\left(I_{B3} = \dfrac{I_{C1}+I_{C2}}{\beta(1+\beta)} \ll I_{C1}\right)$.

The resistors are matched.

With I_{B3} neglected, $I_{C1} = I_R$.

Assume the current drawn by the voltmeter is negligible. The voltmeter reading is

$$V_2 - V_1 = (V_{CC} - I_{C2}R) - (V_{CC} - I_{C1}R)$$

$$= R(I_{C1} - I_{C2})$$

$$= \left[I_{S1} e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_1}{V_A}\right) - I_{S2} e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_2}{V_A}\right)\right] R$$

When $V_1 = V_2 = V$

$$0 = R\left(1+\frac{V}{V_A}\right) e^{\frac{V_{BE}}{V_T}} (I_{S1} - I_{S2})$$

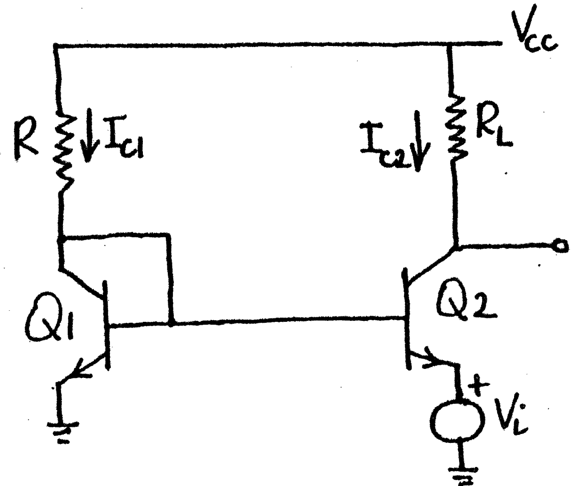
which implies $I_{S1} = I_{S2}$.

<u>Q1 and Q2 are matched if the voltmeter reads zero.</u>

<u>Note</u>: Since I_S is temperature dependent, Q1 and Q2 must be at the same temperature.

[To obtain $\frac{I_{S2}}{I_{S1}}$, measure I_{C2} and I_{C1} and form $\dfrac{I_{C2}}{I_{C1}} = \dfrac{I_{S2} e^{V_{BE}/V_T}(1+V_1/V_A)}{I_{S1} e^{V_{BE}/V_T}(1+V_2/V_A)} \cong \dfrac{I_{S2}}{I_{S1}}$]

An amplifier with stabilized bias



Quiescent value of V_o ($V_i = 0$)

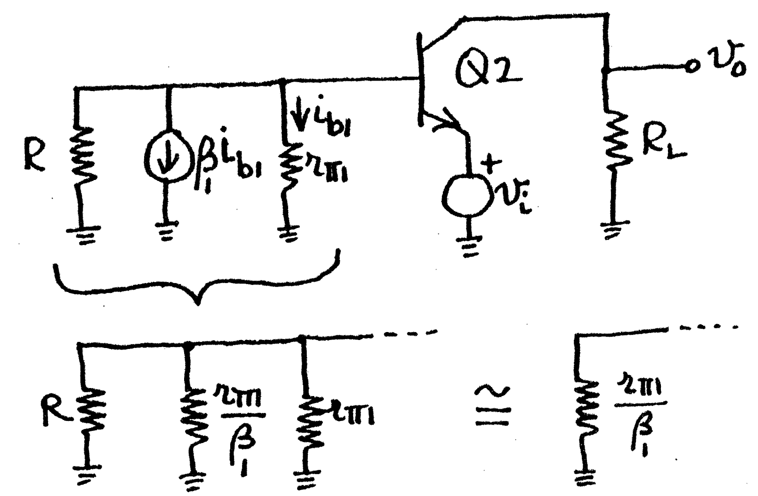
$$V_o = V_{CC} - I_{C2}R_L \cong V_{CC} - I_{C1}R_L$$

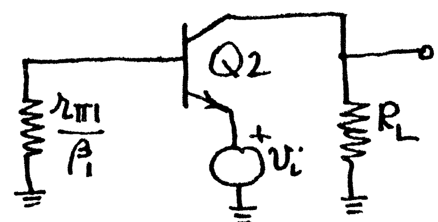
$$\boxed{V_o = V_{CC} - \left(\frac{V_{CC} - V_{BE}}{R}\right)R_L}$$

Except for V_{BE}, the operating point at the output is independent of the transistor.

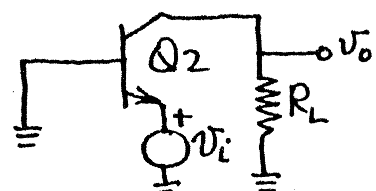
Note that any resistance associated with source V_i will change I_{C2} (reduce it) relative to I_{C1} unless an equal resistance is placed in the emitter of Q1.

Calculation of gain (assume $r_o = \infty$)

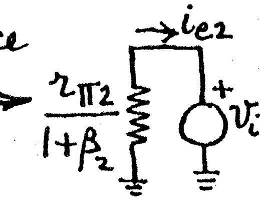




Because $I_{C1} = I_{C2}$, $r_{\pi 1} = r_{\pi 2}$. The base of Q_2 is effectively at ground because $\frac{r_{\pi 1}}{\beta_1}$, which is in series with $r_{\pi 2}$, is much less than $r_{\pi 2}$.



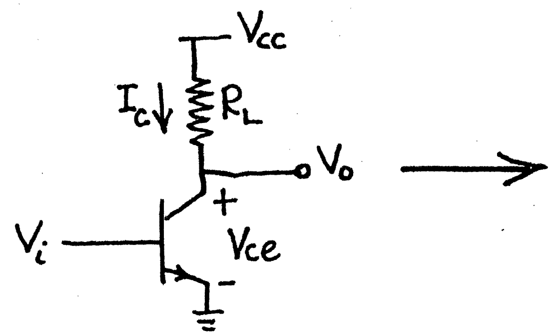
The source v_i sees $\rightarrow$



$$v_o \cong -i_{e2}R_L \cong R_L \frac{v_i}{r_{\pi 2}/\beta_2} \qquad A_v = \frac{v_o}{v_i} = \boxed{g_{m2}R_L}$$

L11: Common-Emitter Amplifier with resistive and active loads

I Resistive Load

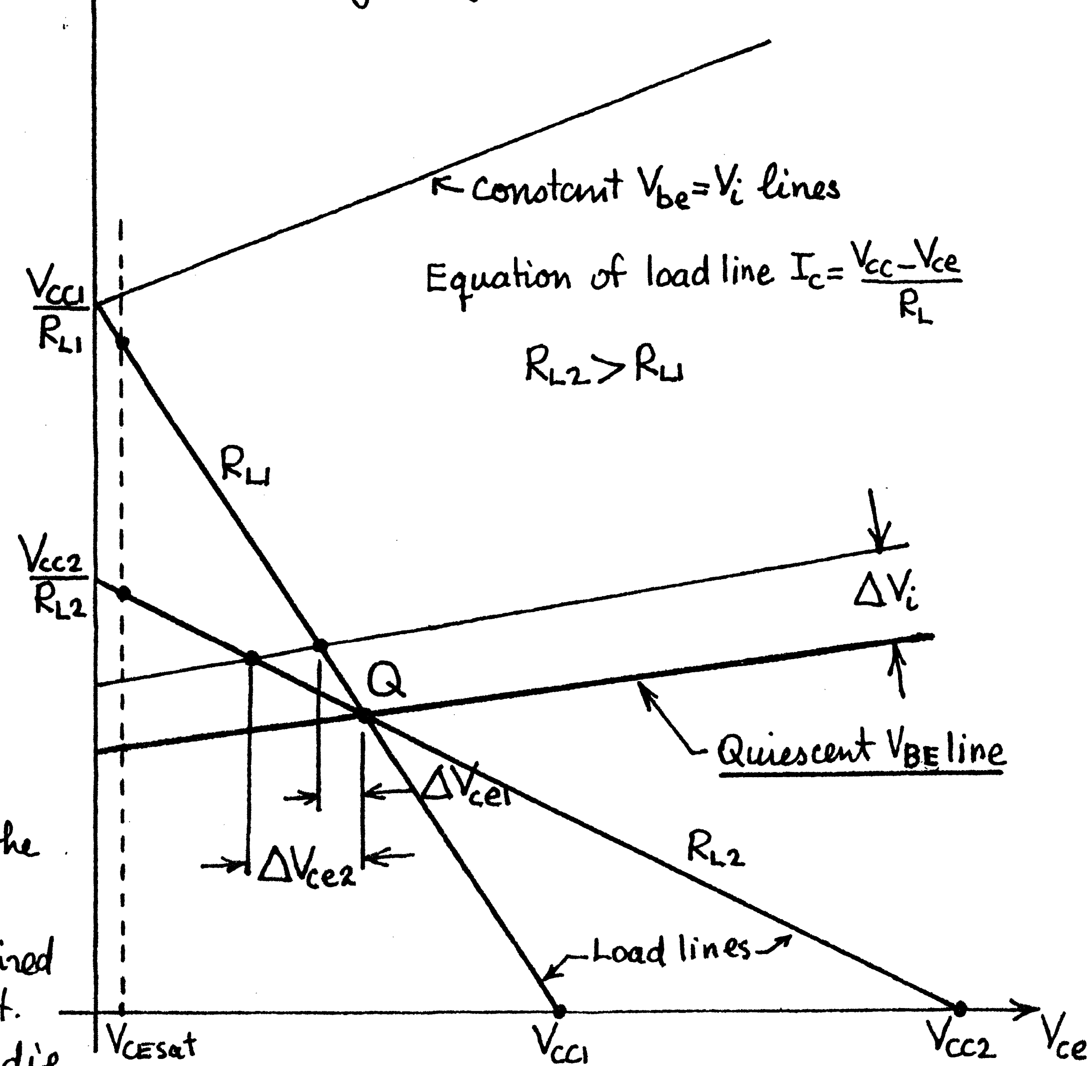


$V_{CEsat} \le V_o \le V_{CC}$

Important observations

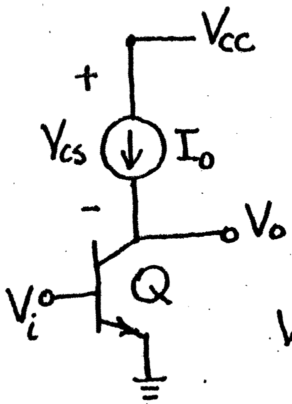
1. Regardless of V_{CC} and R_L, it takes $\Delta V_i = 120mV$ to go from $0.99V_{CC}$ to $0.01V_{CC}$ (practically from cutoff to saturation). See p17.
2. At a given Q-point, the larger R_L, the more ΔV_{ce} for a given ΔV_i (the larger the small-signal gain).
3. The larger R_L, the larger the required V_{CC} to establish the same Q-point. Consequently <u>it takes too large a die area (large R_L) and too large a supply voltage to achieve large gains.</u>

Operating range



Equation of load lines $I_c = \frac{V_{cc} - V_{ce}}{R_L}$

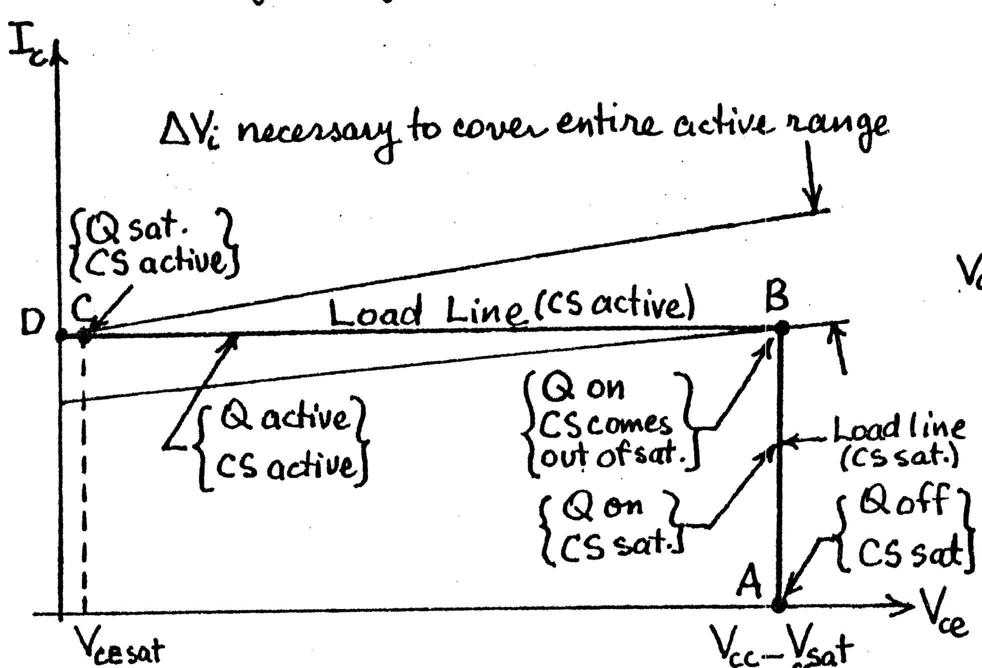
II Ideal current-source load



The collector current cannot change as long as the CS is active.

$$V_{CEsat} \le V_o \le V_{CC} - V_{CSsat}$$

Operating range



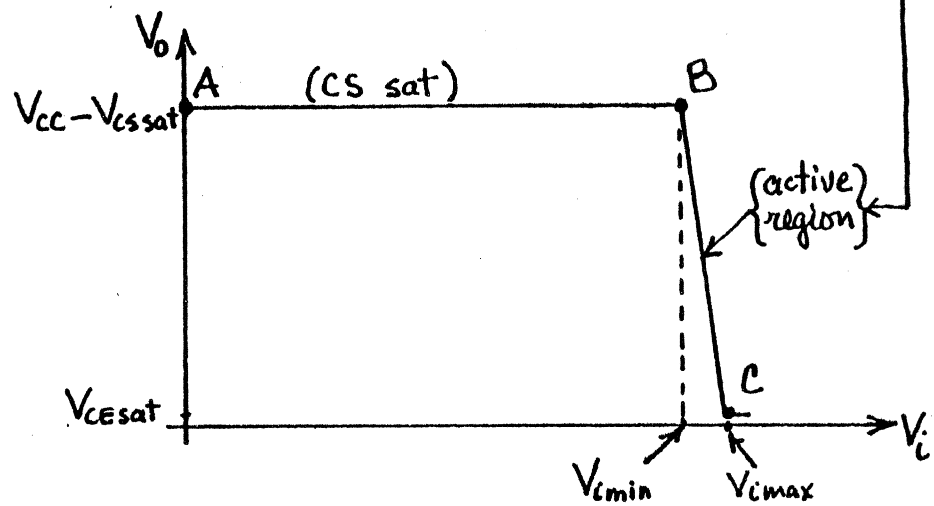
As V_i increases from 0, the op. pt goes from A to B to C to D.

The transfer characteristics

When the transistor and the current-source are both active,

$$I_c = I_s e^{\frac{V_i}{V_T}}\left(1+\frac{V_o}{V_A}\right) = I_o$$

$$\boxed{V_o = V_A\left(\frac{I_o}{I_s} e^{-\frac{V_i}{V_T}} - 1\right) \qquad V_{CEsat} \le V_o \le V_{CC} - V_{CSsat}}$$



To find V_{imin}, let $V_o = V_{CC} - V_{CSsat}$ and solve for V_i.

$$V_{CC} - V_{CSsat} = V_A\left(\frac{I_o}{I_s} e^{-\frac{V_{imin}}{V_T}} - 1\right)$$

$$\boxed{V_{imin} = V_T \ln\left(\frac{I_o/I_s}{1+\frac{V_{CC}-V_{CSsat}}{V_A}}\right)}$$

To find V_{imax}, let $V_o = V_{CEsat}$ and solve for V_i.

$$V_{CEsat} = V_A\left(\frac{I_o}{I_S} e^{-\frac{V_{imax}}{V_T}} - 1\right)$$

$$\boxed{V_{imax} = V_T \ln\left(\frac{I_o/I_S}{1 + \frac{V_{CEsat}}{V_A}}\right)}$$

ΔV_i necessary to cover entire active range can be found from

$$\Delta V_i = V_{imax} - V_{imin} = V_T \ln\left[\frac{1 + \frac{V_{CC} - V_{CSsat}}{V_A}}{1 + \frac{V_{CEsat}}{V_A}}\right]$$

Since $\frac{V_{CC} - V_{CSsat}}{V_A} \ll 1$ and $\frac{V_{CEsat}}{V_A} \ll 1$, we can use the approx. $\ln(1+x) \cong x$ and obtain

$$\Delta V_i = V_T\left[\left(\frac{V_{CC} - V_{CSsat}}{V_A}\right) - \left(\frac{V_{CEsat}}{V_A}\right)\right] \cong \boxed{V_T \frac{V_{CC}}{V_A}}$$

For $V_T = 26\,mV$, $V_{CC} = 15\,V$, and $V_A = 130\,V$, we obtain

$$\Delta V_i = 26 \times \frac{15}{130} = \boxed{3\,mV}$$

Calculation of voltage gain

The small-signal voltage-gain A_v can be found by differentiating the expression for V_o with respect to V_i.

$$V_o = V_A\left(\frac{I_o}{I_S} e^{-\frac{V_i}{V_T}} - 1\right)$$

$$A_v = \frac{dV_o}{dV_i} = \boxed{-\frac{V_A}{V_T}\frac{I_o}{I_S} e^{-\frac{V_i}{V_T}}}$$

The gain is max, when $V_i = V_{imin}$.

$$A_{vmax} = -\frac{V_A}{V_T}\frac{I_o}{I_S} e^{-\frac{V_{imin}}{V_T}}$$

But from the previous page,

$$\frac{I_o}{I_S} e^{-\frac{V_{imin}}{V_T}} = 1 + \frac{V_{CC} - V_{CSsat}}{V_A} \cong 1 + \frac{V_{CC}}{V_A}$$

So, $\boxed{A_{vmax} = -\frac{V_A}{V_T}\left(1 + \frac{V_{CC}}{V_A}\right)}$

The gain is min, when $V_i = V_{imax}$.

$$A_{vmin} = -\frac{V_A}{V_T}\frac{I_o}{I_S} e^{-\frac{V_{imax}}{V_T}}$$

But $\frac{I_o}{I_S} e^{-\frac{V_{imax}}{V_T}} = 1 + \frac{V_{CEsat}}{V_A} \cong 1$

So, $\boxed{A_{v\,min} = -\frac{V_A}{V_T}}$

Note that $A_{v\,max} = A_{v\,min}\left(1+\frac{V_{CC}}{V_A}\right)$.

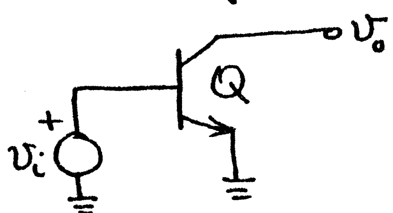
Hence, as long as $V_{CC}/V_A \ll 1$, the gain (the slope) is constant for all practical purposes and is given by

$$\boxed{A_v \cong -\frac{V_A}{V_T}} \quad V_{CEsat} \le V_O \le V_{CC} - V_{CSsat}$$

Stated differently, the transfer characteristic in the active region is practically a straight line.

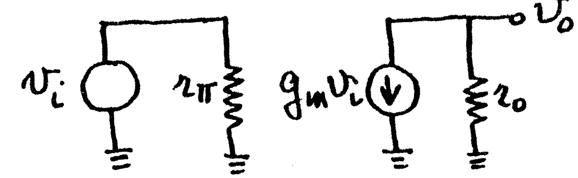
Alternative derivation of A_v

The small signal circuit is



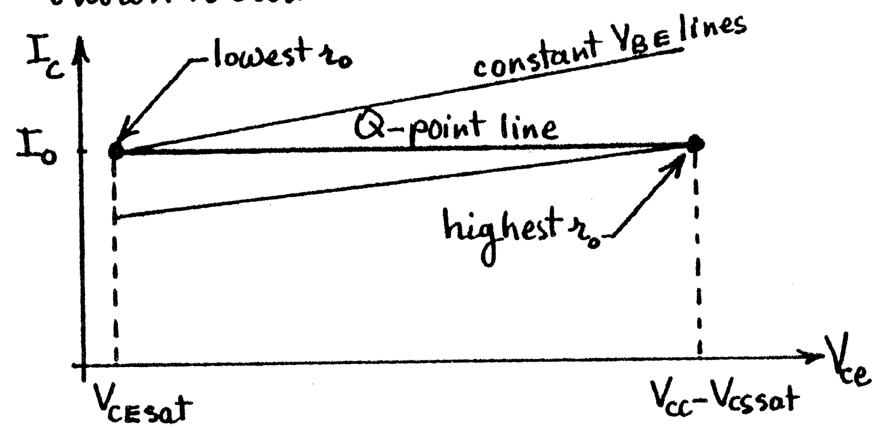
Note that signalwise, the collector is open-circuited since the load is an ideal CS.

The small-signal equivalent circuit is



$$\boxed{A_v = \frac{v_o}{v_i} = -g_m r_o} \qquad g_m = \frac{I_C}{V_T} = \frac{I_o}{V_T}$$

As the operating point is varied in the active region, g_m stays constant because $I_C = I_o$. However, r_o changes as shown below.

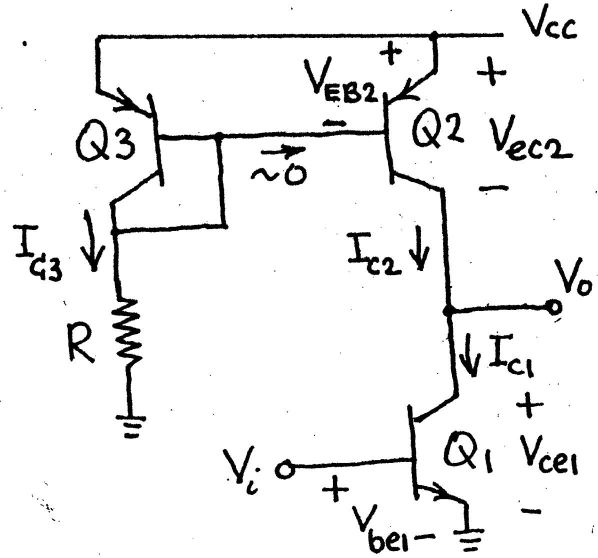


$$A_v = -g_m r_o = -\frac{I_o}{V_T}\left(\frac{V_A+V_{CE}}{I_o}\right) = \boxed{-\frac{V_A+V_{CE}}{V_T}}$$

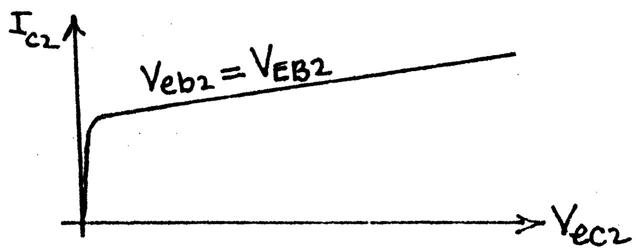
$$A_{v\,min} = A_v\Big|_{V_{CE}=V_{CEsat}\cong 0} \cong \boxed{-\frac{V_A}{V_T}}$$

$$A_{v\,max} = A_v\Big|_{V_{CE}=V_{CC}-V_{CSsat}\cong V_{CC}} \cong \boxed{-\frac{V_A+V_{CC}}{V_T}}$$

III Actual current source load



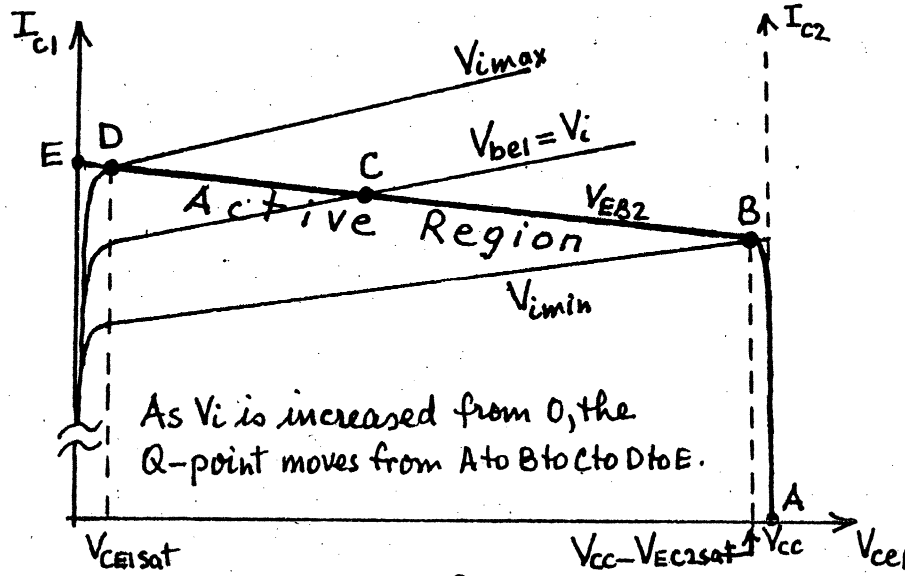
$I_{c3} \cong \frac{V_{cc}-V_{EB3}}{R}$. Hence $V_{EB2}=V_{EB3}$ is fixed and is given by $V_{EB2}=V_T \ln \frac{I_{c3}}{I_s}$. As long as I_{b2} can be neglected, V_{eb2} cannot change and the op. pt. of Q2 is somewhere on the curve shown below.



Since Q2 serves as load on Q1, the output variables of Q2 must be expressed in terms of the output variables of Q1:

$I_{c2}=I_{c1}$ $\quad V_{ec2}=V_{cc}-V_{ce1} \rightarrow V_{ce1}=V_{cc}-V_{ec2}$

Hence, by reflecting the I_{c2} vs V_{ec2} curve shown below, left about the I_{c2} axis and then shifting it to the right by V_{cc}, we obtain the "load curve" on Q1 as shown below.



A–B Q1 on, Q2 sat

B–C–D Q1 and Q2 on

D–E Q1 sat, Q2 on

Since curves are nearly horizontal, it takes very little ΔV_i to go from B to D.

The transfer characteristic

V_o vs. V_i curve when both Q1 and Q2 are active. Since an NPN and a PNP transistor are involved, the transistor parameters will be designated by either N (for NPN) or P (for PNP) subscripts.

$$I_{C2} = I_{SP}\, e^{\frac{V_{EB2}}{V_T}}\left(1+\frac{V_{EC2}}{V_{AP}}\right)$$

$$= I_{SP}\, e^{\frac{V_{EB2}}{V_T}}\left(1+\frac{V_{CC}-V_o}{V_{AP}}\right)$$

$$I_{C1} = I_{SN}\, e^{\frac{V_i}{V_T}}\left(1+\frac{V_{CE1}}{V_{AN}}\right)$$

$$= I_{SN}\, e^{\frac{V_i}{V_T}}\left(1+\frac{V_o}{V_{AN}}\right)$$

Using $I_{C1}=I_{C2}$, and solving for V_o, we obtain

$$\boxed{V_o = \frac{I_{SP}\, e^{\frac{V_{EB2}}{V_T}}\left(1+\frac{V_{CC}}{V_{AP}}\right) - I_{SN}\, e^{\frac{V_i}{V_T}}}{I_{SP}\, e^{\frac{V_{EB2}}{V_T}}\frac{1}{V_{AP}} + I_{SN}\, e^{\frac{V_i}{V_T}}\frac{1}{V_{AN}}}}$$

$V_{CE1sat} \leq V_o \leq V_{CC}-V_{EC2sat}$

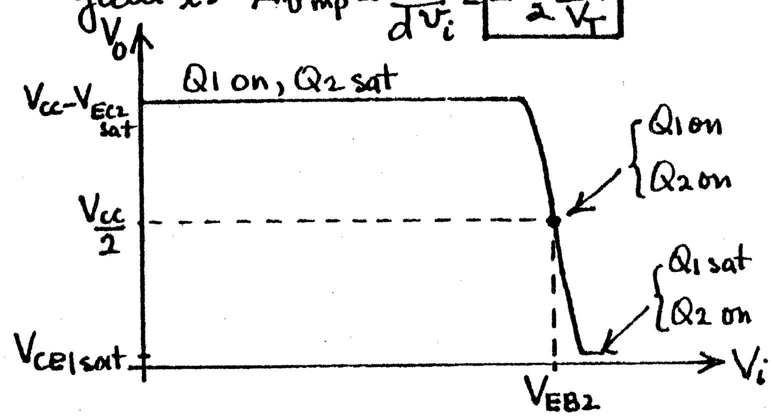
For $I_{SP}=I_{SN}$, $V_{AP}=V_{AN}=V_A$, and $V_i = V_{EB2}$, this equation gives $\underline{V_o = \frac{V_{CC}}{2}}$ (as it must since the bottom and top half of the circuit become then mirror images of each other). With $\underline{V_i = V_{EB2}+v_i}$, the expression for V_o simplifies to

$$V_o = V_A\left(\frac{1+\frac{V_{CC}}{V_A} - e^{v_i/V_T}}{1+e^{v_i/V_T}}\right)$$

For $v_i/V_T \ll 1$, we can approximate e^{v_i/V_T} by $(1+v_i/V_T)$ and obtain

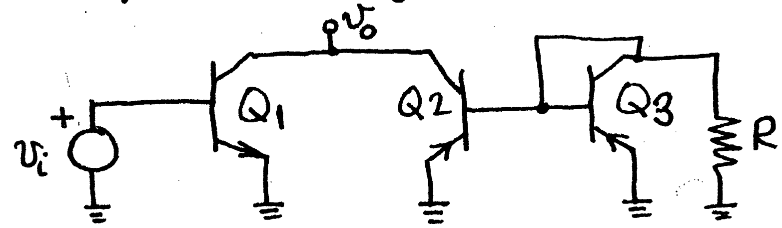
$$\boxed{V_o = \frac{V_{CC}}{2} - \frac{1}{2}\frac{V_A}{V_T}v_i}$$

which represents the output only about the midpoint of the operating range. The midpoint gain is $A_{vmp} = \frac{dV_o}{dv_i} = \boxed{-\frac{1}{2}\frac{V_A}{V_T}}$

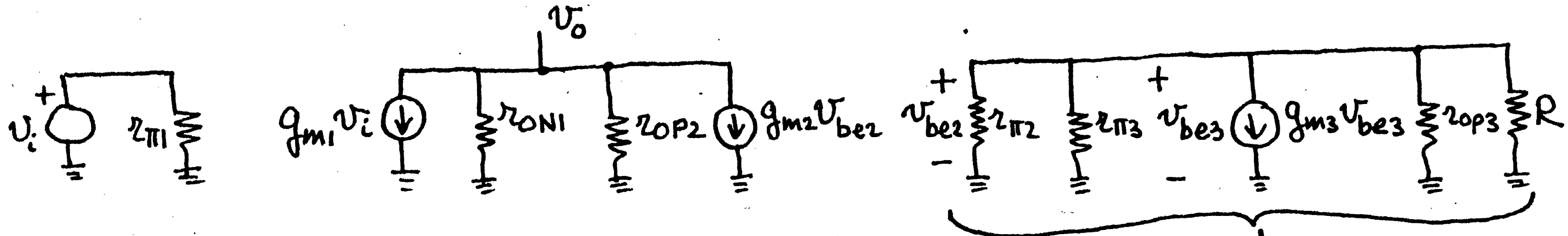


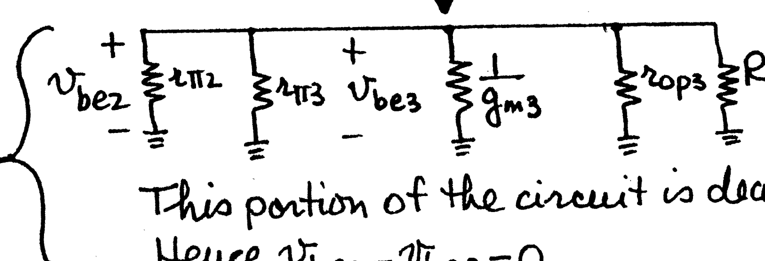
Small-signal gain as a function of the operating point

The small-signal circuit is:



The small-signal equivalent circuit is:





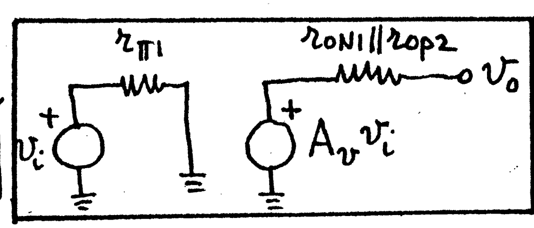
This portion of the circuit is dead. Hence $v_{be2} = v_{be3} = 0$

With $v_{be2} = 0$, v_o becomes

$$v_o = -g_{m1}(r_{oN1} \| r_{oP2}) v_i$$

$$\boxed{A_v = -g_{m1} \frac{r_{oN1} r_{oP2}}{r_{oN1} + r_{oP2}}}$$

The input and output equivalent circuits are given by



where

$$g_{m1} = \frac{I_{C1}}{V_T}$$

$$r_{oN1} = \frac{V_{AN1} + V_{CE1}}{I_{C1}} = \frac{V_{AN} + V_o}{I_{C1}}$$

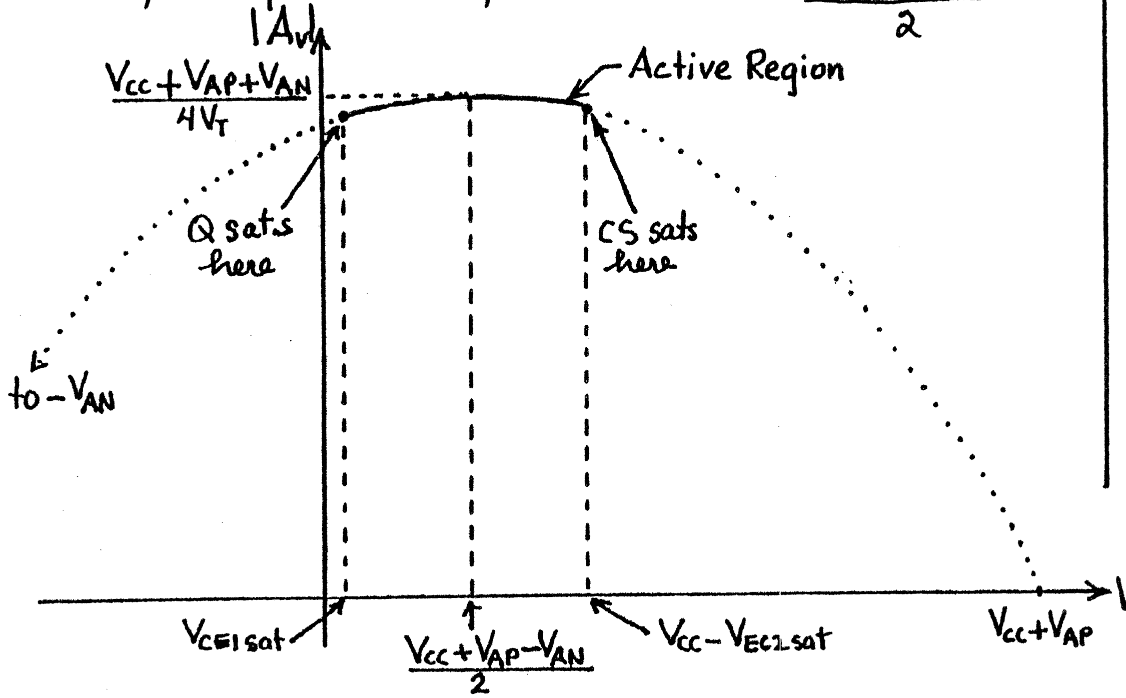
$$r_{oP2} = \frac{V_{AP2} + V_{EC2}}{I_{C2}} = \frac{V_{AP} + V_{CC} - V_o}{I_{C2}}$$

How does the gain vary with the operating point?

$$A_v = -g_{m1}\frac{r_{oN1}r_{oP2}}{r_{oN1}+r_{oP2}} = -\frac{I_{C1}}{V_T}\,\frac{\left(\frac{V_{AN}+V_o}{I_{C1}}\right)\left(\frac{V_{AP}+V_{CC}-V_o}{I_{C1}}\right)}{\left(\frac{V_{AN}+V_o}{I_{C1}}\right)+\left(\frac{V_{AP}+V_{CC}-V_o}{I_{C1}}\right)}$$

$$\boxed{A_v = -\frac{1}{V_T}\,\frac{(V_{AN}+V_o)(V_{AP}+V_{CC}-V_o)}{V_{AN}+V_{AP}+V_{CC}}}$$

The A_v vs. V_o curve is a parabola with V_o-axis intercepts at $-V_{AN}$ and $(V_{AP}+V_{CC})$. Hence, the apex of the parabola is at $\frac{(V_{CC}+V_{AP}-V_{AN})}{2}$.



The maximum gain occurs when $V_o = \frac{V_{CC}+V_{AP}-V_{AN}}{2}$ and is equal to

$$\boxed{|A_v|_{max} = \frac{V_{CC}+V_{AP}+V_{AN}}{4V_T}}$$

which for $V_{AP}=V_{AN}=V_A$ and $V_{CC} \ll V_A$ reduces to $\boxed{V_A/2V_T}$. Furthermore, as the plot shows, the apex of the parabola would then be at $V_o = \frac{V_{CC}}{2}$, and the gain would vary very little over the entire active region from $V_o \cong 0$ to $V_o \cong V_{CC}$.

With $V_{CC}=15V$, $V_A=130V$, and $V_T=26mV$, the max. and min. gains are

$$|A_v|_{max} = \frac{V_{CC}+2V_A}{4V_T} = 2644$$

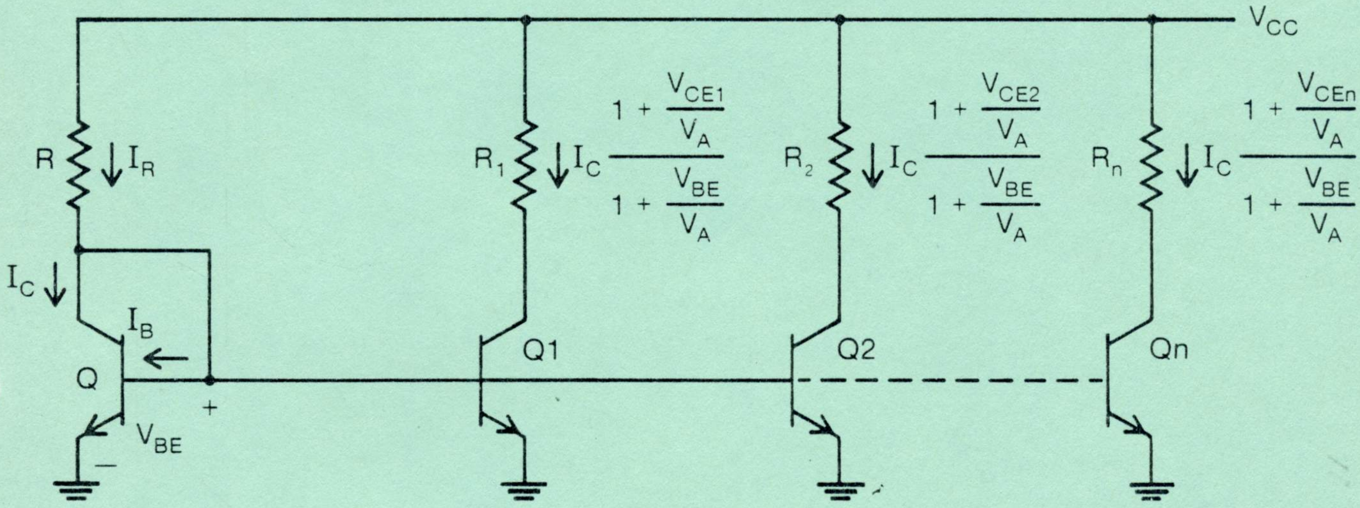
$$|A_v|_{min} = \frac{V_A}{V_T}\left(\frac{V_{CC}+V_A}{V_{CC}+2V_A}\right) = 2636$$

Hence, the gain varies $\frac{1}{3}\%$ as the op. pt. is moved from $V_o \cong 0$ to $V_o \cong 15V$. Correspondingly $\Delta V_i \cong \frac{15\times10^3}{2640} = 5.7mV$ for $\Delta V_o = 15V$.

A Self Study Subject

FUNDAMENTALS & APPLICATIONS OF ANALOG INTEGRATED CIRCUITS

PART I
LOW FREQUENCY ANALYSIS & DESIGN



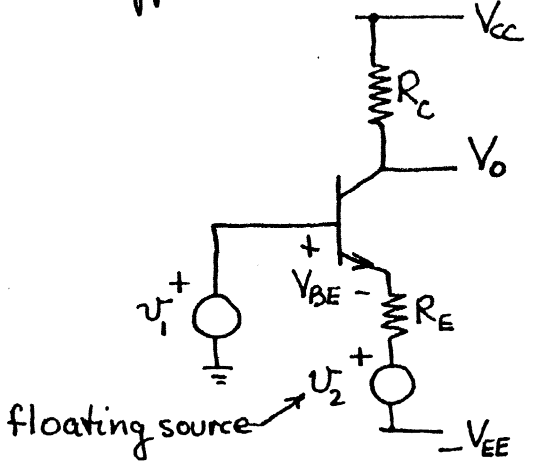
Study Guide
for

MODULE C
The Differential Amplifier

Colorado State University
Engineering Renewal
& Renewal & Growth Program

Aram Budak

L12: A simple but not so accurate difference amplifier



Operating point $v_1 = v_2 = 0$

$$V_o = V_{CC} - I_{C_Q} R_C \cong V_{CC} - R_C \frac{(V_{EE} - V_{BE})}{R_E}$$

$$V_{CE\,sat} - V_{BE} \le V_o \le V_{CC}$$

Gain

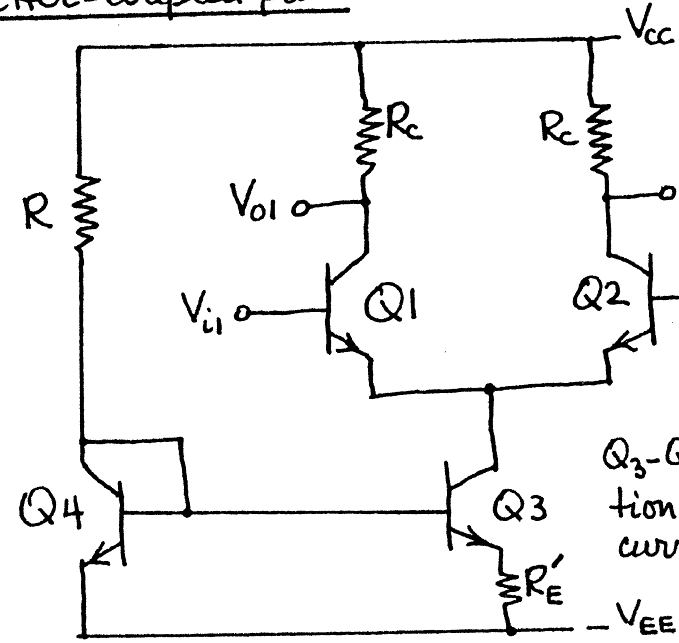
If $r_o = \infty$, $v_o = \dfrac{(v_2 - v_1)\beta R_C}{r_\pi + (1+\beta)R_E}$

$v_o = (v_2 - v_1)A_v$ $\quad A_v = \dfrac{\beta R_C}{r_\pi + (1+\beta)R_E}$

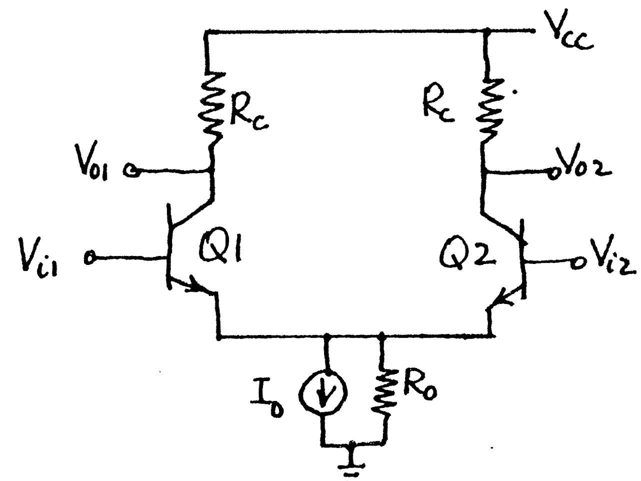
However, for $r_o \neq \infty$, $v_o = A_2 v_2 - A_1 v_1$ (see p37) where $A_1 \neq A_2$. Hence not a diff. amplifier.

The differential amplifier

Also known as difference amplifier or emitter-coupled pair.

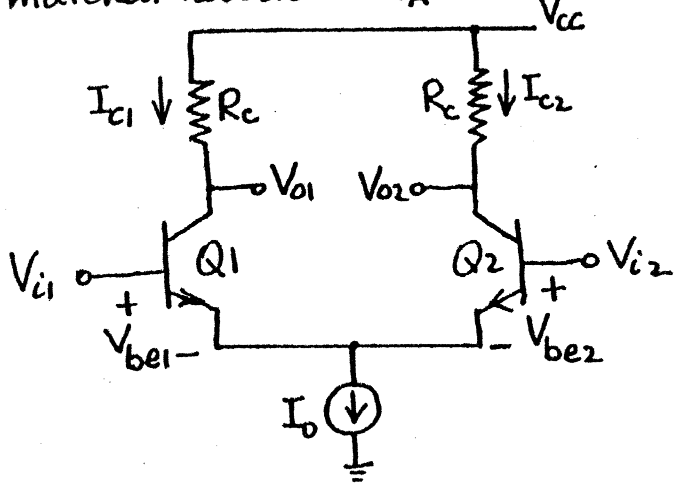


Q_3-Q_4 combination forms a current source



Large-signal characteristics

Assume matched transistors and matched resistors. $V_A = \infty$.



$$V_{i1} - V_{be1} = V_{i2} - V_{be2} \qquad V_{i1} - V_{i2} = V_{id} = V_{be1} - V_{be2}$$

When $V_{i1} = V_{i2} = 0$

$$V_{be1} = V_{be2} = V_{BE} \qquad I_{c1} = I_{c2} = I_s e^{\frac{V_{BE}}{V_T}} = \alpha \frac{I_o}{2}$$

$$V_{BE} = V_T \ln\left(\frac{\alpha I_o}{2 I_s}\right)$$

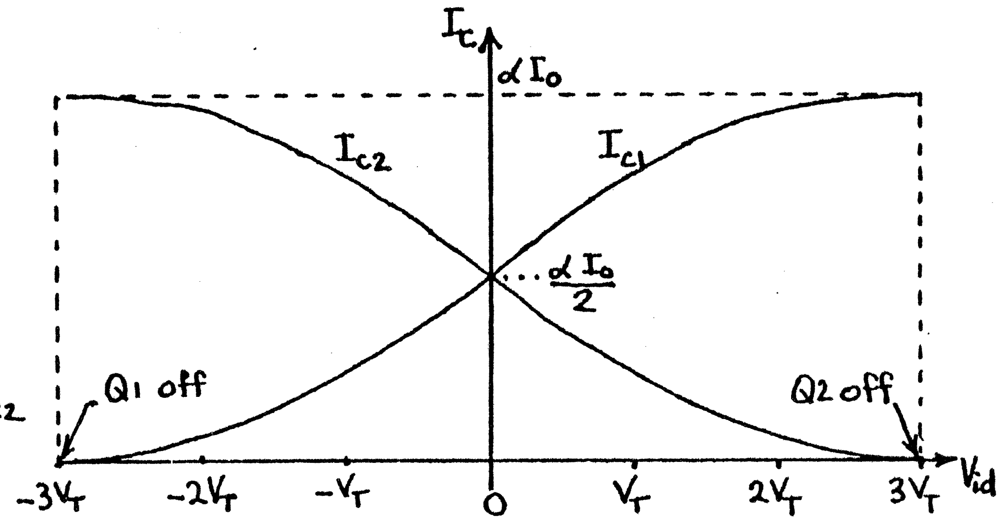
How do I_c's, V_{be}'s, and V_o vary with V_{id}?

$$\left\{\begin{array}{l} V_{id} = V_{i1} - V_{i2} = V_{be1} - V_{be2} \\ I_{c1}/\alpha + I_{c2}/\alpha = I_o \\ I_{c1} = I_s e^{V_{be1}/V_T}, \quad I_{c2} = I_s e^{V_{be2}/V_T} \end{array}\right\}$$

$$\frac{I_{c1}}{I_{c2}} = e^{(V_{be1} - V_{be2})/V_T} = e^{V_{id}/V_T}$$

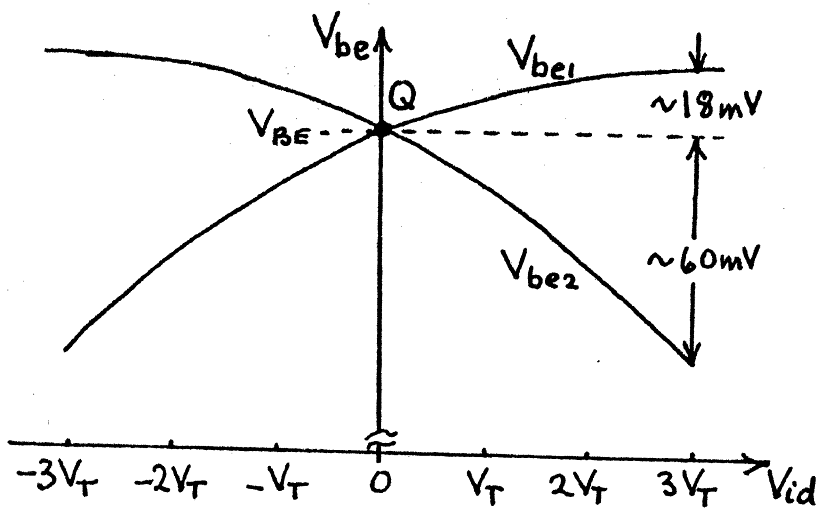
$$I_{c2} e^{V_{id}/V_T} + I_{c2} = \alpha I_o$$

$$\boxed{I_{c2} = \frac{\alpha I_o}{1 + e^{V_{id}/V_T}}} \qquad \boxed{I_{c1} = \frac{\alpha I_o}{1 + e^{-V_{id}/V_T}}}$$

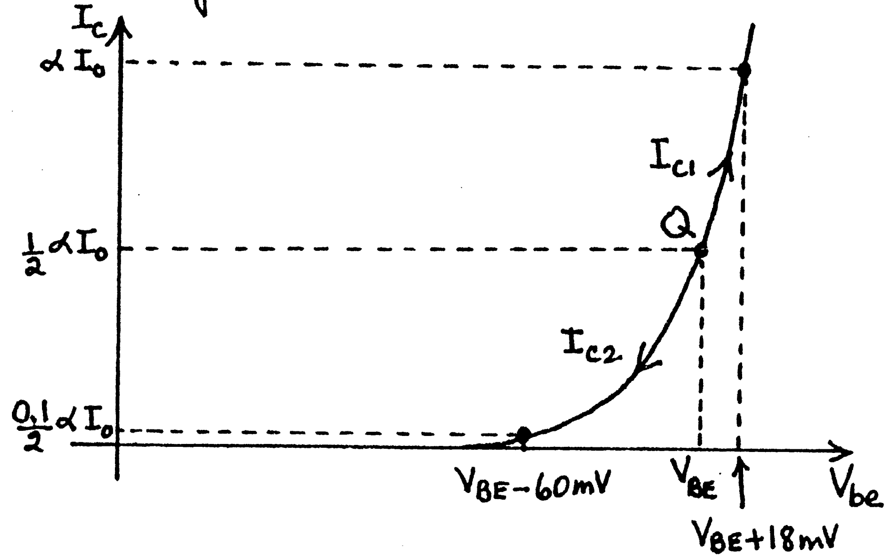


$\frac{V_i}{V_T}$	1	2	3	4	5
$\frac{I_{c1}}{I_{c2}}$	2.72	7.39	20.09	54.60	148.41

$$\boxed{\begin{array}{l} V_{be1} = V_T \ln \frac{I_{c1}}{I_s} = V_T \ln\left(\frac{\alpha I_o / I_s}{1 + e^{-V_{id}/V_T}}\right) \\ V_{be2} = V_T \ln \frac{I_{c2}}{I_s} = V_T \ln\left(\frac{\alpha I_o / I_s}{1 + e^{V_{id}/V_T}}\right) \end{array}}$$



As V_{id} increases from 0, V_{be1} increases and V_{be2} decreases from V_{BE}. <u>The increase in V_{be1} is less than the decrease in V_{be2}.</u> Particularly when V_{id} gets large, say $3V_T$, most of the V_{id} appears across the base-to-emitter of Q2 for turning it off. This is because it takes an increase of only 18mV in V_{be1} in order for I_{c1} to go from its quiescent value of $\frac{\alpha I_o}{2}$ to its maximum possible value of αI_o whereas it takes a decrease of 60mV in V_{be2} in order for I_{c2} to go from its quiescent value of $\frac{\alpha I_o}{2}$ to $0.1\frac{\alpha I_o}{2}$. This can be clearly seen by looking at the I_c vs. V_{be} curves. $I_c = I_s e^{\frac{V_{be}}{V_T}}$.



It takes about <u>78mV in V_{id}</u> (18mV increase in V_{be1} and 60mV decrease in V_{be2}) to cause practically all the current supplied by the common emitter current source to go through Q1 and thereby cut Q2 almost off, i.e., reduce its current to 10% of its quiescent value. This is shown below.

$$V_{be1} = V_{BE} - V_T \ln \tfrac{1}{2}\left(1+e^{-V_{id}/V_T}\right)\Big|_{V_{id}/V_T=3} = \boxed{V_{BE}+16.8mV}$$

$$V_{be2} = V_{BE} - V_T \ln \tfrac{1}{2}\left(1+e^{V_{id}/V_T}\right)\Big|_{V_{id}/V_T=3} = \boxed{V_{BE}-61.0mV}$$

Calculation of differential output voltage

$V_{od} = V_{o1} - V_{o2}$.

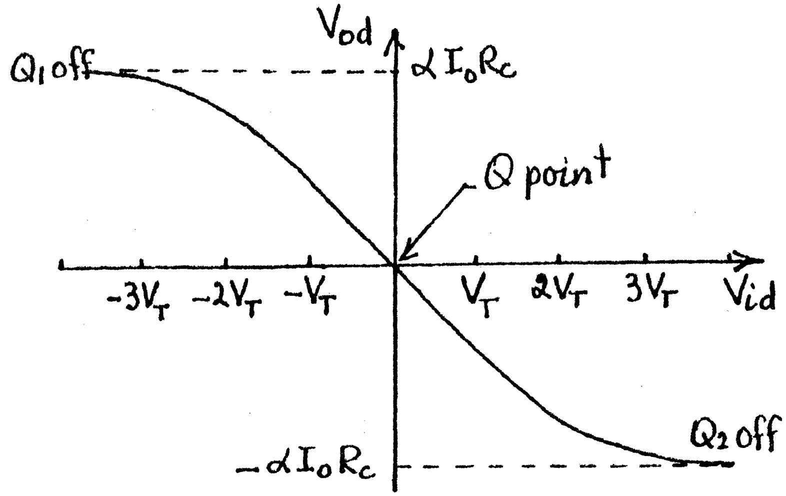
$$V_{od} = (V_{CC} - I_{C1}R_C) - (V_{CC} - I_{C2}R_C) = (I_{C2} - I_{C1})R_C$$

$$= \alpha I_o R_C \left(\frac{1}{1+e^{V_{id}/V_T}} - \frac{1}{1+e^{-V_{id}/V_T}} \right)$$

$$= -\frac{\alpha I_o R_C \left(e^{V_{id}/V_T} - e^{-V_{id}/V_T}\right)}{e^{V_{id}/V_T} + 2 + e^{-V_{id}/V_T}}$$

$$= -\alpha I_o R_C \frac{\left(e^{V_{id}/2V_T} + e^{-V_{id}/2V_T}\right)\left(e^{V_{id}/2V_T} - e^{-V_{id}/2V_T}\right)}{\left(e^{V_{id}/2V_T} + e^{-V_{id}/2V_T}\right)^2}$$

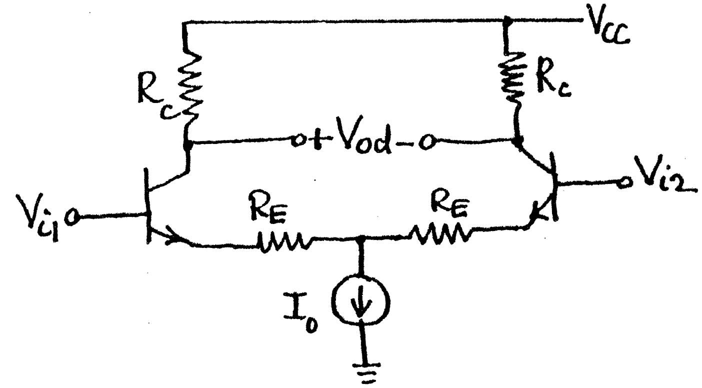
$$= -\alpha I_o R_C \frac{\left(e^{V_{id}/2V_T} - e^{-V_{id}/2V_T}\right)}{\left(e^{V_{id}/2V_T} + e^{-V_{id}/2V_T}\right)} = \boxed{-\alpha I_o R_C \tanh \frac{1}{2}\frac{V_{id}}{V_T}}$$

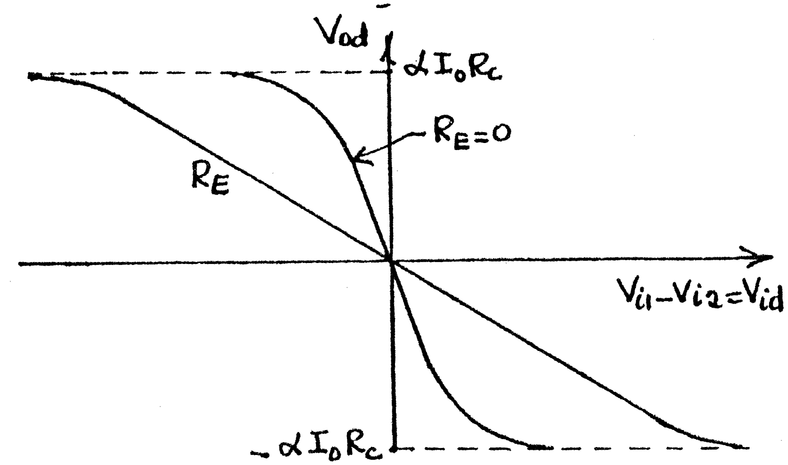


$\frac{V_{id}}{V_T}$	$\frac{\lvert V_{od}\rvert}{\alpha I_o R_c}$
1	.462
2	.762
3	.905
4	.964

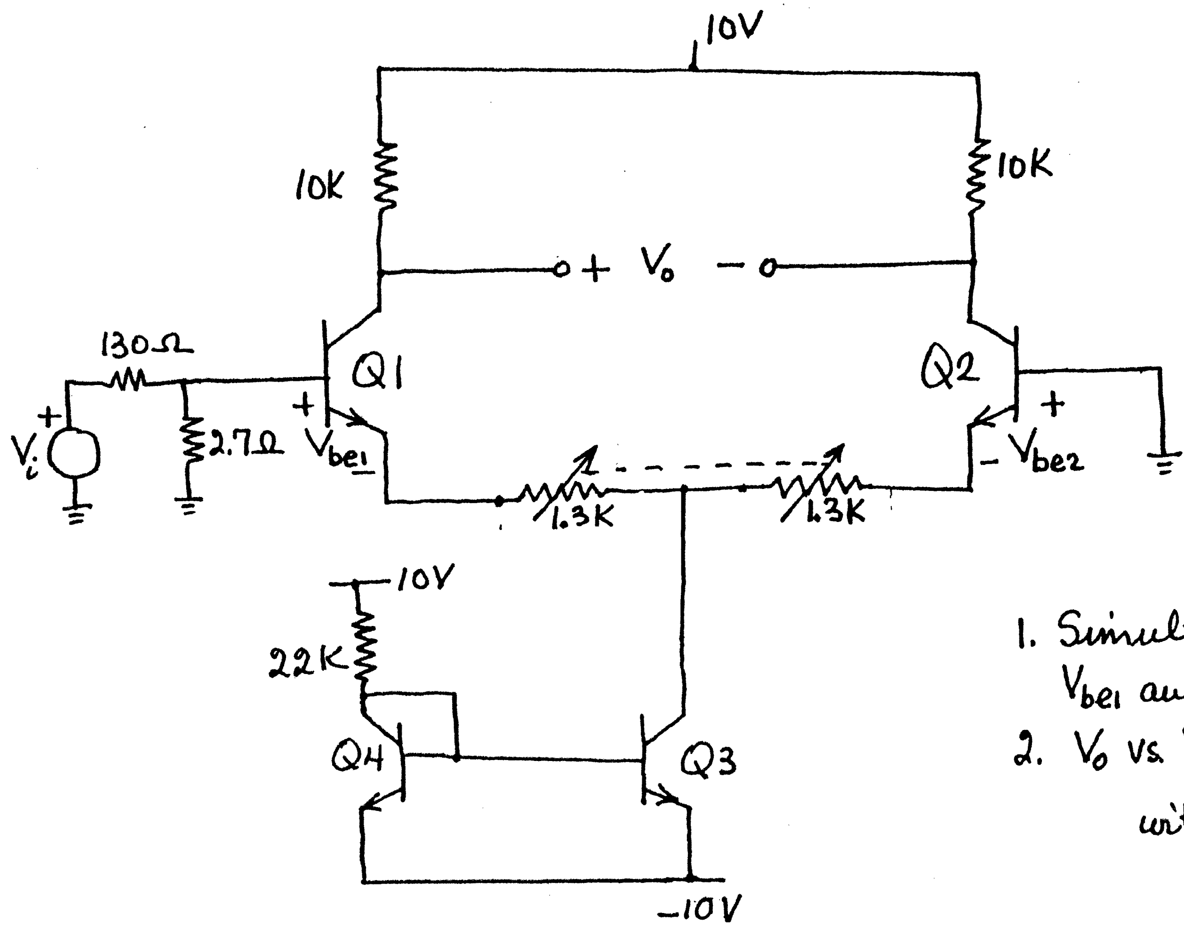
Provided $V_{cc} - \alpha I_o R_c > V_{CEsat} - V_{be} + V_i$, neither Q1 nor Q2 can saturate. Unless V_{EE} is made very small, Q3 cannot saturate either. It should be noted that if $|V_{i1}|$ or $|V_{i2}|$ is made too large, the collector-to-base junctions become forward biased.

Effect of emitter degeneration



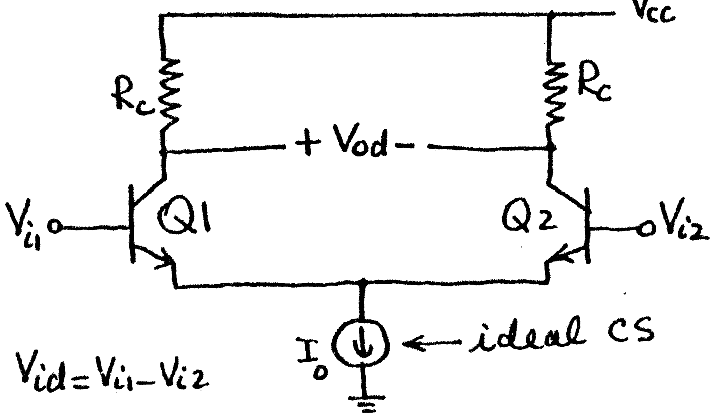


Differential Amplifier Demonstration



1. Simultaneous display of V_{be1} and V_{be2} curves vs. V_i ($R_E=0$)
2. V_o vs. V_i curve with $\begin{cases} R_E = 0 \\ R_E = 1.3K \end{cases}$

Calculation of differential gain



$V_{id} = V_{i1} - V_{i2}$

From large-signal analysis we have

$$V_{od} = -\alpha I_o R_c \tanh \frac{1}{2}\frac{V_{id}}{V_T}$$

For $|x| \ll 1$, $\tanh x \cong x - \frac{x^3}{3}$

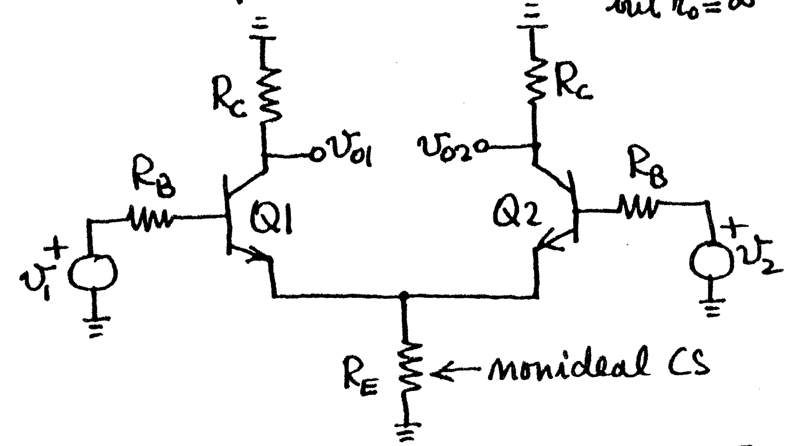
$$V_{od} \cong -\alpha I_o R_c \frac{1}{2}\frac{V_{id}}{V_T}\left[1 - \frac{1}{12}\left(\frac{V_{id}}{V_T}\right)^2\right]$$

For $\left|\frac{V_{id}}{V_T}\right| \leq 1$ $\boxed{V_{od} \cong -\frac{\alpha I_o R_c}{2}\frac{V_{id}}{V_T}}$

As long as $|V_{id}| \leq V_T$, V_{od} is linearly dependent on V_{id}. Hence, over this range, the gain is independent of the signal amplitude and is given by

$$A_v = \frac{d(V_{od})}{d(V_{id})} = \frac{V_{od}}{V_{id}} = -\frac{\alpha I_o R_c}{2V_T} = -\frac{I_C R_c}{V_T} = \boxed{-g_m R_c}$$

Small-signal analysis (with R_B and R_E present but $r_o = \infty$)



Quiescent collector currents are $I_{C1} = I_{C2} = \frac{\alpha I_o}{2}$.

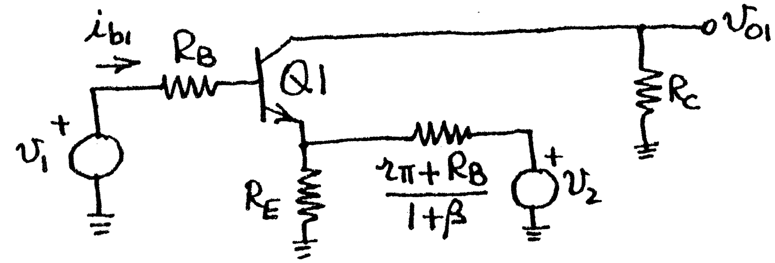
Hence, for small-signal analysis

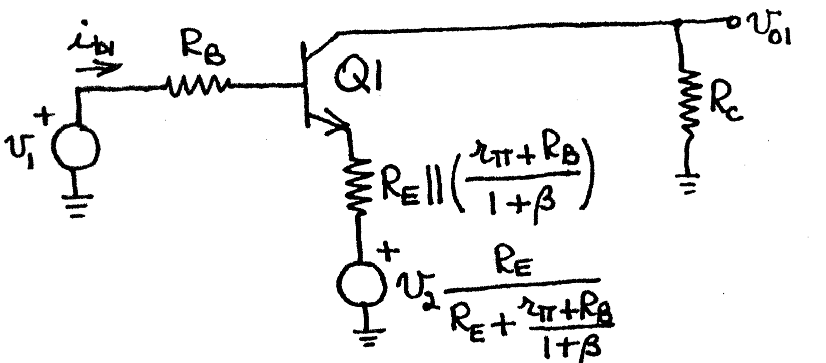
$$r_{\pi 1} = r_{\pi 2} = r_\pi = \frac{V_T}{I_B} = \frac{V_T}{\frac{\alpha I_o}{2}/\beta} = \boxed{\frac{2V_T(1+\beta)}{I_o}}$$

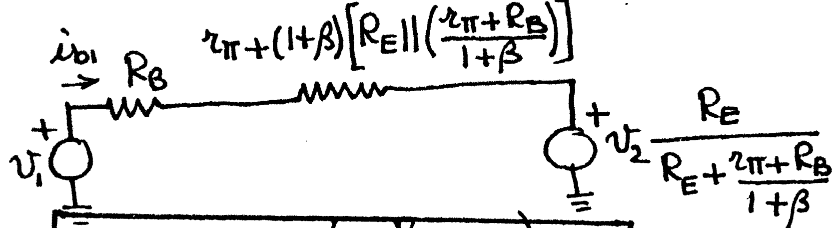
$$g_{m1} = g_{m2} = g_m = \frac{I_C}{V_T} = \boxed{\frac{\alpha I_o}{2V_T}}$$

Assume $r_o = \infty$

<u>Method 1</u> Start with eq. circuit facing v_1.







$$\boxed{i_{b1} = \frac{v_1 - v_2\left(\dfrac{R_E}{R_E + \frac{r_\pi + R_B}{1+\beta}}\right)}{R_B + r_\pi + \dfrac{(1+\beta)R_E(r_\pi + R_B)}{(1+\beta)R_E + r_\pi + R_B}}}$$

What resistance does source v_i see?

The answer depends on what v_2 is.

1. If v_2 is independent, make it 0. Then source v_1 sees

$$\boxed{R_B + r_\pi + \frac{(r_\pi + R_B)(1+\beta)R_E}{r_\pi + R_B + (1+\beta)R_E} \Bigg|_{R_E \to \infty} \rightarrow 2(r_\pi + R_B)}$$

2. If $v_2 = v_1$, common-mode excitation, source v_1 sees

$$\frac{R_B + r_\pi + \dfrac{(r_\pi + R_B)(1+\beta)R_E}{r_\pi + R_B + (1+\beta)R_E}}{1 - \dfrac{R_E}{R_E + \frac{r_\pi + R_B}{1+\beta}}} = \boxed{r_\pi + R_B + (1+\beta)2R_E \Big|_{R_E \to \infty} \rightarrow \infty}$$

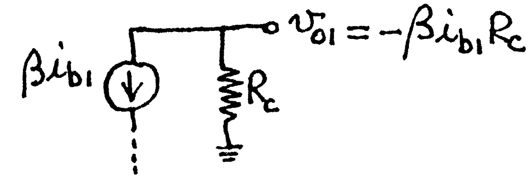
Source v_1 sees a very high resistance.

3. If $v_2 = -v_1$, difference-mode excitation, source v_1 sees

$$\frac{R_B + r_\pi + \dfrac{(r_\pi + R_B)(1+\beta)R_E}{r_\pi + R_B + (1+\beta)R_E}}{1 + \dfrac{R_E}{R_E + \frac{r_\pi + R_B}{1+\beta}}} = \boxed{r_\pi + R_B}$$

What is the v_{01} output?

This is the output with respect to ground.



$$v_{O1} = -\frac{\beta R_C\left(v_1 - v_2\dfrac{R_E}{R_E + \frac{r_\pi + R_B}{1+\beta}}\right)}{R_B + r_\pi + \dfrac{(r_\pi + R_B)(1+\beta)R_E}{r_\pi + R_B + (1+\beta)R_E}}$$

$$\boxed{v_{O1} = -\frac{\beta R_C}{R_B + r_\pi}\left[\frac{v_1 - v_2\left(\dfrac{R_E}{R_E + \frac{r_\pi + R_B}{1+\beta}}\right)}{1 + \dfrac{R_E}{R_E + \frac{r_\pi + R_B}{1+\beta}}}\right]}$$

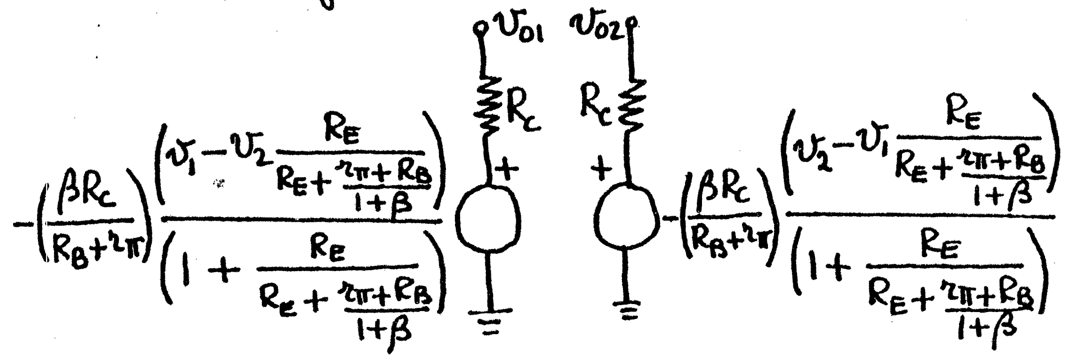
The v_{O1} output is <u>not</u> proportional to the difference of the two input signals. Stated differently, if the output is <u>single ended</u>, the circuit does <u>not</u> act like <u>a difference amplifier</u> even when the r_o of the transistors are assumed ∞.

However, if $R_E = \infty$ (ideal CS in the emitter), then

$$v_{O1} = -\frac{\beta R_C}{2(R_B + r_\pi)}(v_1 - v_2)$$

which is proportional to the difference signal.

<u>Putting the two halves of the circuit together</u>

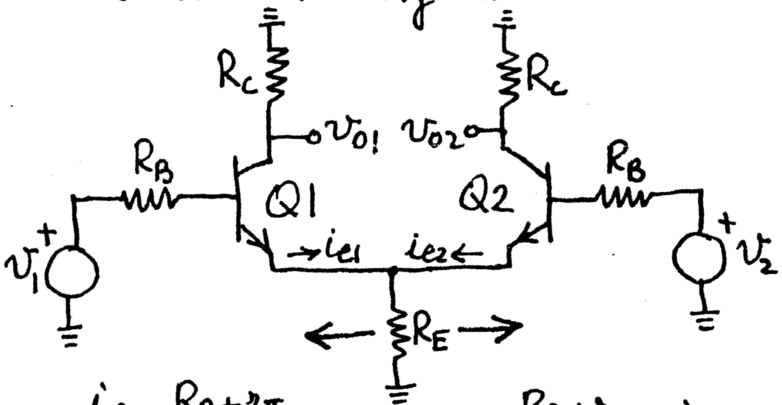


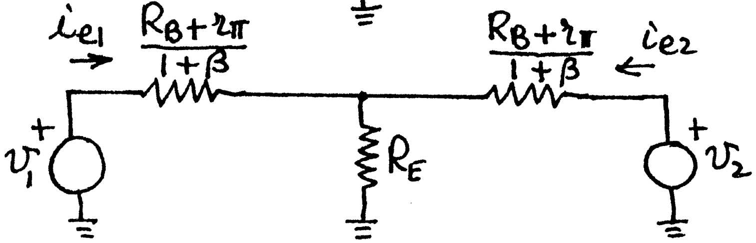
$$\boxed{v_{od} = v_{O1} - v_{O2} = -\left(\frac{\beta R_C}{R_B + r_\pi}\right)(v_1 - v_2)}$$

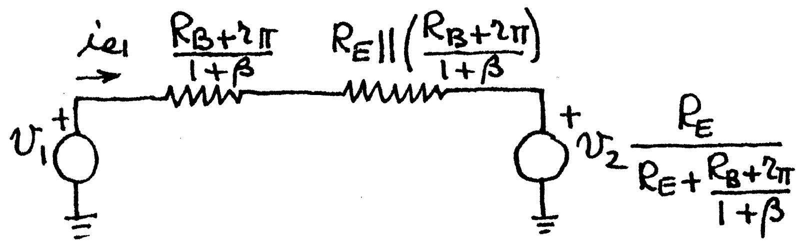
The collector-to-collector output, v_{od}, is proportional to the difference signal regardless of the value of R_E. The circuit then is a <u>difference or differential amplifier</u>. Although not considered here, this is true even when the r_o's of the transistors are taken into account. Of course <u>all these results are based on the assumption that the two halves of the circuit are perfectly matched.</u>

For $R_B = 0$, $v_{od} = -g_m R_c (v_1 - v_2)$ which agrees with the result obtained from the large-signal analysis.

L13: Method 2 Start with equivalent circuits facing R_E.







$$v_{o1} = -i_{e1}\alpha R_c = -\frac{\beta}{1+\beta}R_c\,\frac{v_1 - v_2\left(\dfrac{R_E}{R_E+\frac{R_B+r_\pi}{1+\beta}}\right)}{\dfrac{R_B+r_\pi}{1+\beta} + \dfrac{R_E\left(\frac{R_B+r_\pi}{1+\beta}\right)}{R_E+\frac{R_B+r_\pi}{1+\beta}}}$$

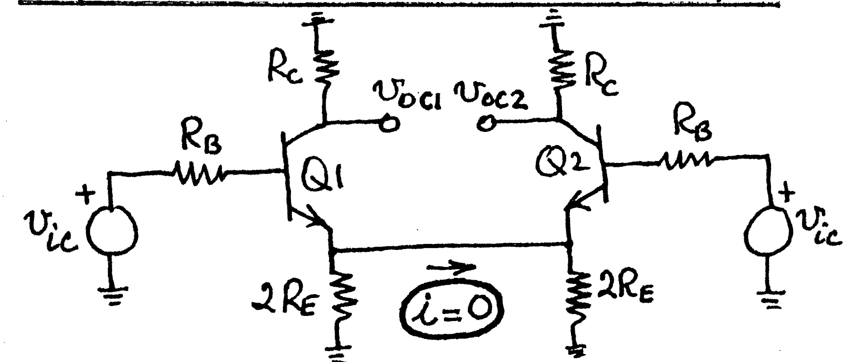
$$\boxed{v_{o1} = -\left(\frac{\beta R_c}{R_B+r_\pi}\right)\frac{\left(v_1 - v_2\dfrac{R_E}{R_E+\frac{R_B+r_\pi}{1+\beta}}\right)}{\left(1 + \dfrac{R_E}{R_E+\frac{R_B+r_\pi}{1+\beta}}\right)}}$$

Method 3 Split the v_1 and v_2 inputs into their common-mode and difference-mode components.

$$v_1 = \frac{v_1+v_2}{2} + \frac{v_1-v_2}{2} = v_{ic} + \frac{v_{id}}{2} \qquad v_{ic} = \frac{v_1+v_2}{2}$$

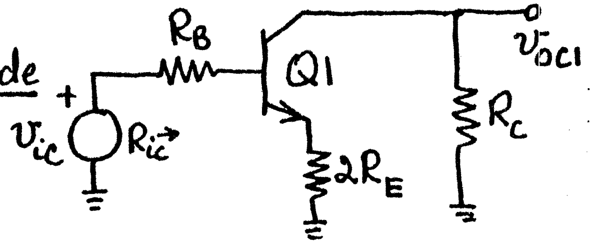
$$v_2 = \frac{v_1+v_2}{2} - \frac{v_1-v_2}{2} = v_{ic} - \frac{v_{id}}{2} \qquad v_{id} = v_1 - v_2$$

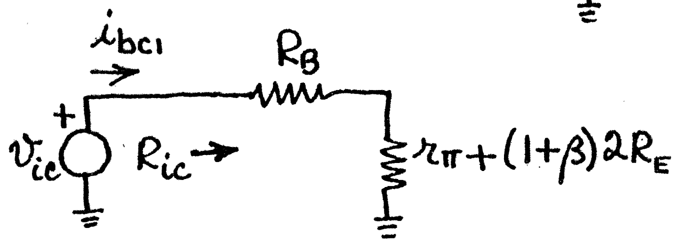
Response due to the common-mode input



Because of the symmetry, the current in the wire connecting the emitters is zero.

Common-mode Half Circuit



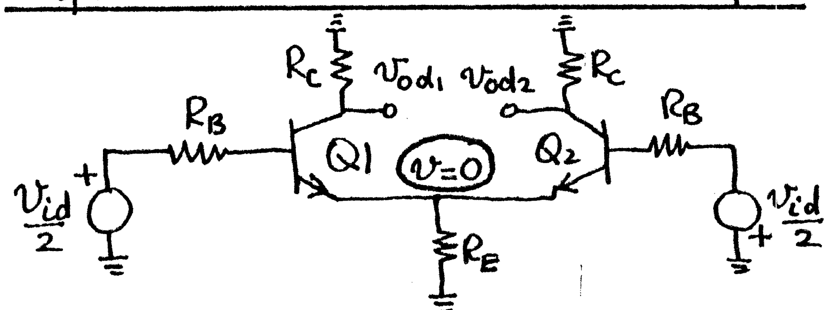


$$\boxed{R_{ic} = R_B + r_\pi + (1+\beta)2R_E}$$ common-mode input resistance

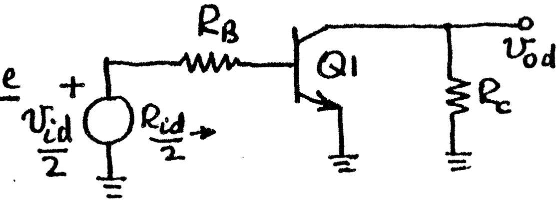
$$v_{oc1} = -\beta i_{bc1} R_C = -\frac{\beta R_C v_{ic}}{R_B + r_\pi + (1+\beta)2R_E} = v_{oc2}$$

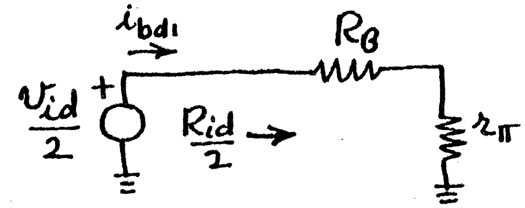
$$\boxed{A_c = -\frac{\beta R_C}{R_B + r_\pi + (1+\beta)2R_E}}$$ common-mode gain

Response due to the difference-mode input



Difference-mode Half Circuit





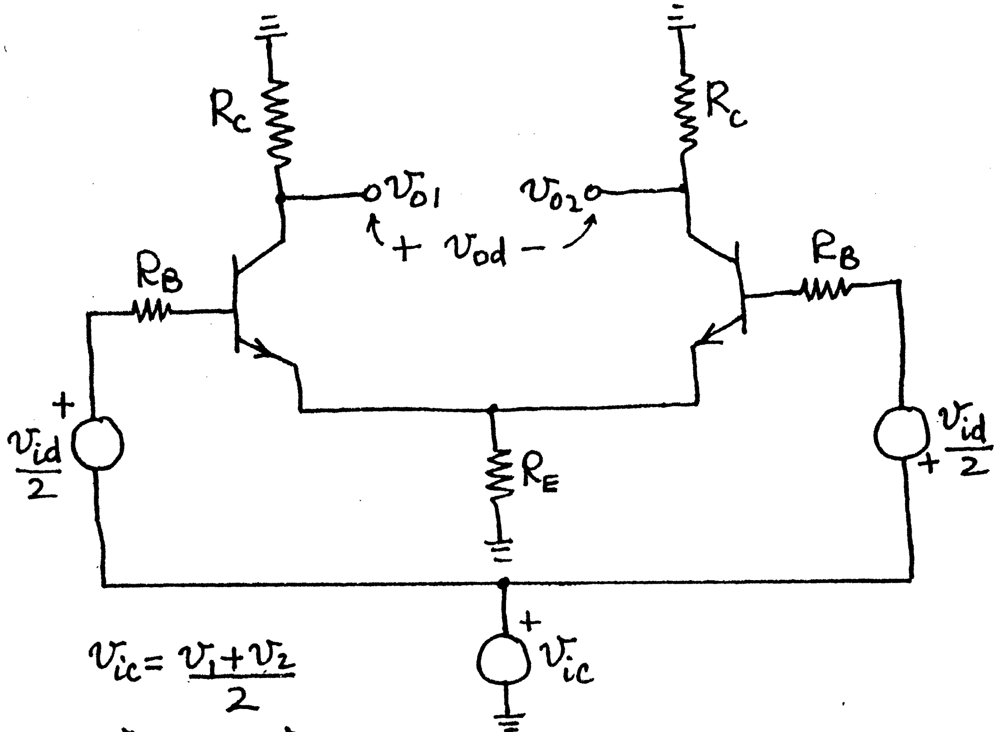
$$\boxed{R_{id} = 2(R_B + r_\pi)}$$ differential-mode input resistance

$$v_{od1} = -\beta i_{bd1} R_C = -\frac{\beta R_C \frac{v_{id}}{2}}{R_B + r_\pi} = -v_{od2}$$

$$\boxed{A_d = -\frac{\beta R_C}{R_B + r_\pi}}$$ difference-mode gain

Since R_E is very large (being the output resistance of a current source), $R_{ic} \gg R_{id}$, $|A_c| \ll |A_d|$. Ideally ($R_E = \infty$), $R_{ic} = \infty$, $A_c = 0$. R_{id} and A_d are not dependent on R_E.

Putting common- and difference-mode responses together



$$v_{ic} = \frac{v_1 + v_2}{2}$$

$$v_{id} = v_1 - v_2$$

$$v_{o1} = v_{oc1} + v_{od1} = \underbrace{\left[\frac{-\beta R_C}{R_B + r_\pi + (1+\beta)2R_E}\right]}_{A_c} v_{ic} + \underbrace{\left[\frac{-\beta R_C}{R_B + r_\pi}\right]}_{A_d} \frac{v_{id}}{2}$$

$$\left\{\begin{aligned} v_{o1} &= A_c v_{ic} + A_d v_{id}/2 \\ v_{o2} &= A_c v_{ic} - A_d v_{id}/2 \end{aligned}\right\}$$

The single-ended outputs v_{o1} and v_{o2} are not proportional to the difference signal.

$$\boxed{v_{od} = v_{o1} - v_{o2} = A_d v_{id}}$$

Common-mode rejection ratio = CMRR

$$CMRR = \left|\frac{A_d}{A_c}\right| = \frac{R_B + r_\pi + (1+\beta)2R_E}{R_B + r_\pi}$$

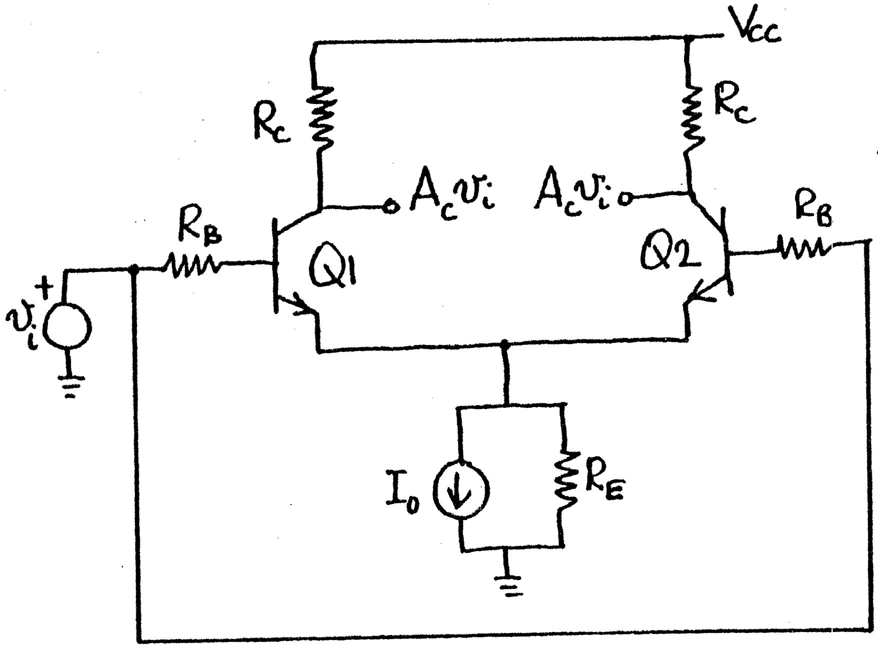
$$\boxed{CMRR = 1 + \frac{(1+\beta)2R_E}{R_B + r_\pi}}$$

$$CMRR\Big|_{R_B=0} \cong 2g_m R_E = 2\frac{I_C}{V_T}R_E \cong \frac{I_o R_E}{V_T}$$

To increase CMRR, make R_E as large as possible. This is why a current source is used in the emitter. In cases where the attainment of a high CMRR is not such an important consideration, instead of the current source, a resistor R_E returned to a negative supply voltage, $-V_{EE}$, can be used. Then, $I_o R_E \cong V_{EE}$ and hence

$$CMRR\Big|_{R_B=0} \cong \frac{V_{EE}}{V_T}\Big|_{V_{EE}=15V} = \frac{15\times10^3}{26} = 577$$

Measurement of A_c

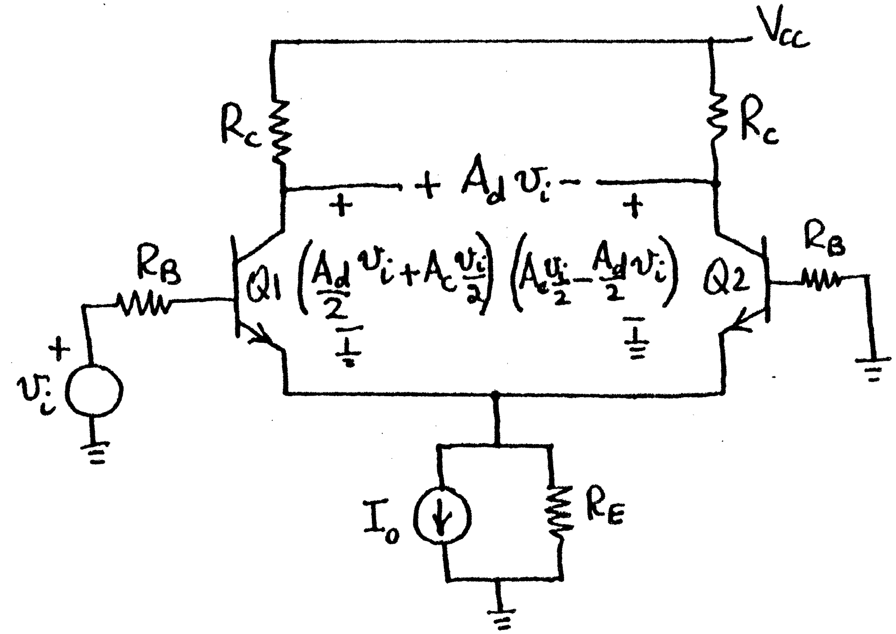


Source v_i sees $\frac{R_{ic}}{2}$ where

$$R_{ic} = R_B + r_\pi + (1+\beta)2R_E$$

$$A_c = \frac{-\beta R_c}{R_B + r_\pi + (1+\beta)2R_E}$$

Measurement of A_d

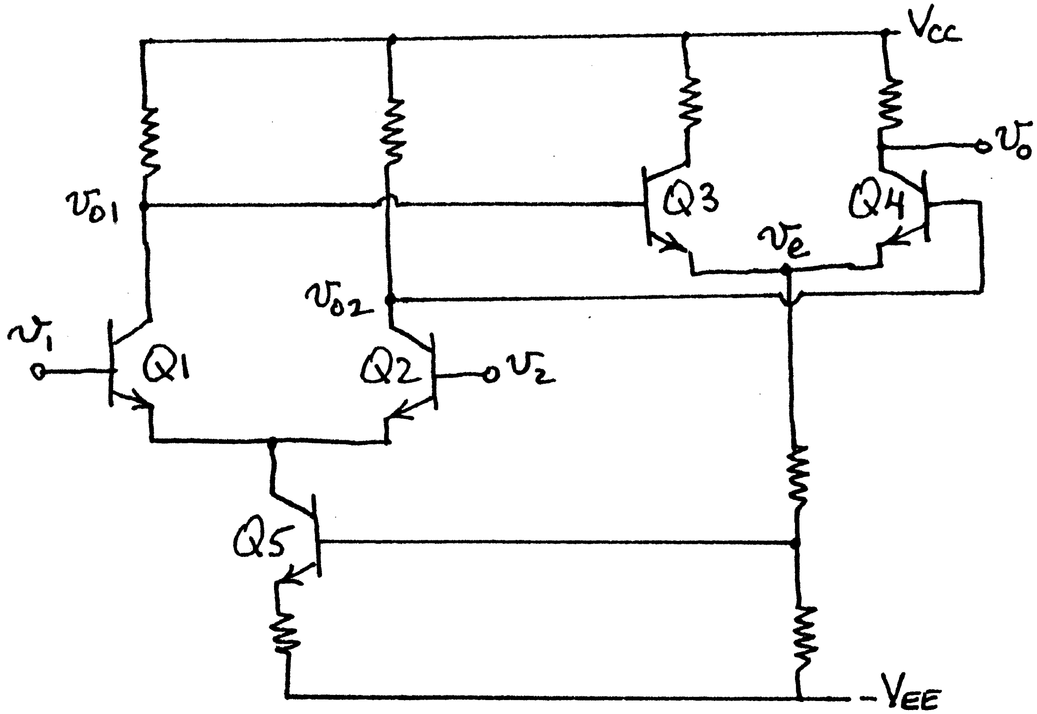


Source v_i sees R_{id} where

$$R_{id} = 2(R_B + r_\pi)$$

$$A_d = \frac{-\beta R_c}{R_B + r_\pi}$$

Common-mode feedback to improve CMRR



The feedback signal is derived from the common emitters of Q_3 and Q_4. At this node, the voltage is proportional only to the common-mode component of the v_1 and v_2 input signals, and therefore feedback affects only the common-mode voltage. No difference-mode signal is fed back because $v_e = 0$ for the difference-mode component of the input signals.

Let A_{c1}, A_{d1} and A_{c2}, A_{d2} represent the common- and difference-mode gains of the input (Q_1, Q_2) and output (Q_3, Q_4) differential amplifiers respectively. Let K_1 represent the attenuation from the v_{o1} output to node e with $v_{o2} = 0$ (or from the v_{o2} output to node e with $v_{o1} = 0$). Let K_2 represent the gain from node e to v_{o1} or v_{o2} outputs. (We see, by inspection, that $K_2 < 0$ and $K_1 > 0$.) The K_1K_2 product would than represent the loop gain.

The input stage is driven by three signals: v_1, v_2, and the feedback signal derived from v_e. Using the principle of superposition, the v_{o1} and v_{o2} outputs can be found.

$$\begin{cases} v_{o1} = A_{c1}\left(\dfrac{v_1+v_2}{2}\right) + A_{d1}\left(\dfrac{v_1-v_2}{2}\right) + K_2 v_e \\ v_{o2} = A_{c1}\left(\dfrac{v_1+v_2}{2}\right) - A_{d1}\left(\dfrac{v_1-v_2}{2}\right) + K_2 v_e \end{cases}$$

Since $v_e = K_1(v_{o1}+v_{o2})$, we obtain

$$v_e = K_1\left[A_{c1}(v_1+v_2) + 2K_2 v_e\right]$$

$$\boxed{v_e = \frac{K_1 A_{c1}(v_1+v_2)}{1-2K_1K_2}}$$

Note that v_e is proportional to the common-mode signal only. Eliminating v_e in the expressions for v_{o1} and v_{o2}, we get

$$\begin{cases} v_{o1} = A_{c1}\left(\dfrac{v_1+v_2}{2}\right) + A_{d1}\left(\dfrac{v_1-v_2}{2}\right) + \dfrac{K_1K_2A_{c1}(v_1+v_2)}{1-2K_1K_2} \\ v_{o2} = A_{c1}\left(\dfrac{v_1+v_2}{2}\right) - A_{d1}\left(\dfrac{v_1-v_2}{2}\right) + \dfrac{K_1K_2A_{c1}(v_1+v_2)}{1-2K_1K_2} \end{cases}$$

$$\begin{cases} v_{o1} = \dfrac{A_{c1}(v_1+v_2)}{2(1-2K_1K_2)} + A_{d1}\left(\dfrac{v_1-v_2}{2}\right) \\ v_{o2} = \dfrac{A_{c1}(v_1+v_2)}{2(1-2K_1K_2)} - A_{d1}\left(\dfrac{v_1-v_2}{2}\right) \end{cases}$$

The output v_o can now be expressed in terms of v_{o1}, v_{o2}, A_{c2}, and A_{d2}.

$$v_o = A_{c2}\left(\frac{v_{o1}+v_{o2}}{2}\right) - A_{d2}\left(\frac{v_{o1}-v_{o2}}{2}\right)$$

$$\boxed{v_o = \underbrace{\frac{A_{c1}A_{c2}}{1-2K_1K_2}}_{A_c}\left(\frac{v_1+v_2}{2}\right) - \underbrace{A_{d1}A_{d2}}_{-A_d}\left(\frac{v_1-v_2}{2}\right)}$$

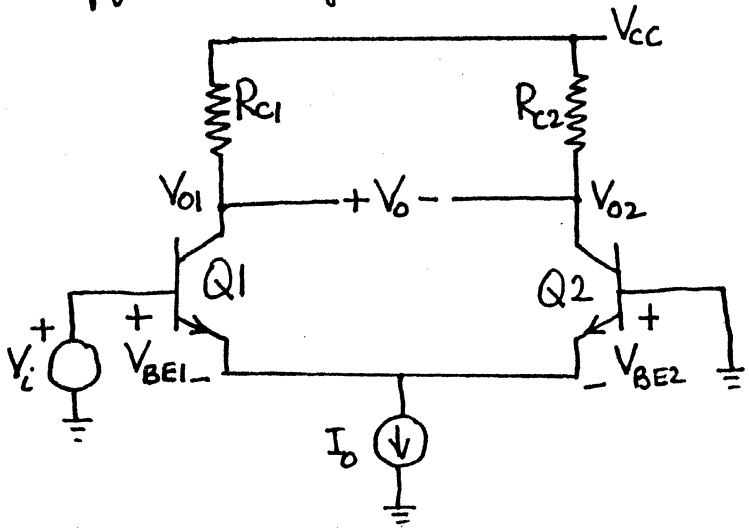
where A_c and A_d are the overall common- and difference-mode gains.

$$\text{CMRR} = \left|\frac{A_d}{A_c}\right| = \boxed{\left(\frac{A_{d1}A_{d2}}{A_{c1}A_{c2}}\right)\underbrace{(1-2K_1K_2)}_{\substack{\text{common-mode}\\ \text{improvement factor}}}}$$

For $K_1K_2 = -4.5$, CMRR is improved by 20dB (10:1).

Mismatch effects in difference amplifiers

1. Offset voltage



Assume the CS to be ideal (as shown) and $V_A = \infty$. Let $V_i = 0$. Then, it follows that

$$V_{BE1} = V_{BE2} = V_{BE}$$

If Q1 and Q2 are matched perfectly, then the CS I_O will divide equally between Q1 and Q2 and V_{BE} and V_O will be given by $V_{BE} \cong V_T \ln \frac{I_O/2}{I_S}$, $V_O = 0$.

However, it is impossible to have a perfect match. So, even though the two base-to-emitter voltages are the same, $I_{C1} \neq I_{C2}$ because $I_{S1} \neq I_{S2}$. Mismatches in I_S's are caused by mismatches in base widths, base and collector doping levels, and emitter areas. Furthermore $R_{C1} \neq R_{C2}$ because it is impossible to construct two identical resistors. Mismatches in R_C's are caused by differences in edge definitions when windows are cut. As a result of these imperfections, there will be an output voltage even though the two inputs are grounded ($V_i = 0$).

$$V_O = V_{O1} - V_{O2} = (V_{CC} - I_{C1}R_{C1}) - (V_{CC} - I_{C2}R_{C2})$$
$$= I_{C2}R_{C2} - I_{C1}R_{C1}$$
$$= I_{S2}e^{V_{BE}/V_T}R_{C2} - I_{S1}e^{V_{BE}/V_T}R_{C1}$$
$$= \boxed{e^{V_{BE}/V_T}(I_{S2}R_{C2} - I_{S1}R_{C1})}$$

To make matters worse, this voltage is temperature dependent. V_o is also affected by the common-mode level of the two inputs which changes the base-to-collector voltages which in turn change the base widths and hence I_s's.

Since this V_o caused by mismatches cannot be distinguished from the difference of the input signals that are being amplified, it sets a limit on the accuracy of the difference signal that can be detected.

The output caused by mismatches in I_s's and R_c's can be counteracted by introducing at the input a V_i that will drive the output to zero. This V_i is called the input offset voltage V_{OS}.

$$V_i = V_{OS} = V_{BE1} - V_{BE2} = V_T\left(\ln\frac{I_{C1}}{I_{S1}} - \ln\frac{I_{C2}}{I_{S2}}\right)$$
$$= V_T \ln\left(\frac{I_{C1}}{I_{C2}}\,\frac{I_{S2}}{I_{S1}}\right)$$

Since $V_o = I_{C2}R_{C2} - I_{C1}R_{C1}$, to make it zero requires that $I_{C2}R_{C2} = I_{C1}R_{C1}$. Hence, V_{OS} can be expressed as

$$\boxed{V_{OS} = V_T \ln\left(\frac{I_{S2}}{I_{S1}}\,\frac{R_{C2}}{R_{C1}}\right)}$$

Stated differently, the input must be offset by V_{OS}, which causes the necessary difference in the two base-to-emitter voltages, to drive the output to zero.

Let $I_{S1} = I_S$ and $I_{S2} = I_S + \Delta I_S$, $R_{C1} = R_C$ and $R_{C2} = R_C + \Delta R_C$. Then, V_{OS} can be written as

$$V_{OS} = V_T \ln\left(1 + \frac{\Delta I_S}{I_S}\right)\left(1 + \frac{\Delta R_C}{R_C}\right)$$
$$= V_T\left[\ln\left(1 + \frac{\Delta I_S}{I_S}\right) + \ln\left(1 + \frac{\Delta R_C}{R_C}\right)\right]$$

Since $\frac{\Delta I_S}{I_S} \ll 1$ and $\frac{\Delta R_C}{R_C} \ll 1$, the approx. $\ln(1+x) \cong x$ can be used to obtain

$$\boxed{V_{OS} \cong V_T\left(\frac{\Delta I_S}{I_S} + \frac{\Delta R_C}{R_C}\right)}$$

The offset voltage is proportional to the individual mismatches. $\frac{\Delta I_S}{I_S}$ and $\frac{\Delta R_C}{R_C}$ are random parameters that take on different values for each circuit that is fabricated. The worst situation arises when all changes are in the same sense:

$$V_{OS} = V_T\left(\frac{|\Delta I_S|}{I_S} + \frac{|\Delta R_C|}{R_C}\right)$$

If we assume $\frac{|\Delta I_S|}{I_S} = 0.05$ and $\frac{\Delta R_C}{R_C} = 0.01$, then, at room temperature

$$V_{OS} = 26\,(0.05 + 0.01) \cong \underline{1.5\,mV}$$

<u>Drift</u>

To see how the offset voltage varies with temperature, we substitude $V_T = \frac{kT}{q}$ in the expression for V_{OS}.

$$V_{OS} = V_T \ln\left(\frac{I_{S2}}{I_{S1}}\frac{R_{C2}}{R_{C1}}\right)$$

$$V_{OS} = \frac{kT}{q} \ln\left(\frac{I_{S2}}{I_{S1}}\frac{R_{C2}}{R_{C1}}\right)$$

I_S, as well as R_C, are temperature dependent too. However, ratios of I_S's and R_C's should be quite independent of temperature. Consequently,

$$\frac{dV_{OS}}{dT} = \frac{k}{q} \ln\left(\frac{I_{S2}}{I_{S1}}\frac{R_{C2}}{R_{C1}}\right)$$

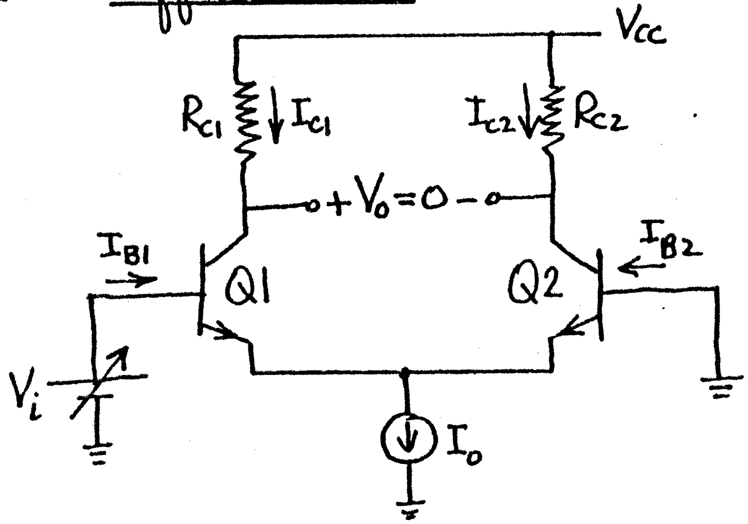
$$\boxed{\frac{dV_{OS}}{dT} = \frac{V_{OS}}{T}}$$

Note that the smaller V_{OS}, the smaller the drift. For $V_{OS} = 1.5\,mV$ and $T = 300°K$,

$$\frac{dV_{OS}}{dT} = \frac{1.5 \times 10^{-3}}{300} = 5\mu V/°K = 5\mu V/°C.$$

With careful designs, it is possible to achieve $1\mu V/°C$. This drift is to be compared against $\frac{dV_{BE}}{dT} \cong -2\,mV/°C$. However, the two V_{BE} drifts in the differential amplifier cancel each other out in well-matched pairs.

L14: 2. Offset current



Adjust V_i to make $V_o = 0$. By definition, the magnitude of this voltage is the offset voltage, i.e., $|V_i| = V_{OS}$.

The magnitude of the difference of the two base currents, $|I_{B1} - I_{B2}|$, when $V_o = 0$ is by definition called the offset current I_{OS}. The reason there is an offset current is because 1) $I_{C1} \neq I_{C2}$ 2) $\beta_1 \neq \beta_2$.

The reason $I_{C1} \neq I_{C2}$ when $V_o = 0$ is because $R_{C1} \neq R_{C2}$.

I_{OS} can be calculated as follows.

$$I_{OS} = |I_{B1} - I_{B2}| = |I_{C1}/\beta_1 - I_{C2}/\beta_2|$$

Let $I_{C1} = I_C$ and $I_{C2} = I_C + \Delta I_C$, $\beta_1 = \beta$ and $\beta_2 = \beta + \Delta\beta$. Then

$$I_{OS} = \left| \frac{I_C}{\beta} - \frac{I_C + \Delta I_C}{\beta + \Delta\beta} \right| = \frac{I_C}{\beta} \left| 1 - \frac{1 + \Delta I_C/I_C}{1 + \Delta\beta/\beta} \right|$$

$$= \frac{I_C}{\beta} \left| \frac{\Delta\beta/\beta - \Delta I_C/I_C}{1 + \Delta\beta/\beta} \right| \underset{\left|\frac{\Delta\beta}{\beta}\right| \ll 1}{\cong} \frac{I_C}{\beta} \left| \frac{\Delta\beta}{\beta} - \frac{\Delta I_C}{I_C} \right|$$

Since $V_o = 0$, $I_{C1}R_{C1} = I_{C2}R_{C2}$. Let $R_{C1} = R_C$ and $R_{C2} = R_C + \Delta R_C$.

$$I_C R_C = (I_C + \Delta I_C)(R_C + \Delta R_C)$$

$$1 = \left(1 + \frac{\Delta I_C}{I_C}\right)\left(1 + \frac{\Delta R_C}{R_C}\right)$$

$$0 = \frac{\Delta I_C}{I_C} + \frac{\Delta R_C}{R_C} + \underbrace{\frac{\Delta I_C}{I_C}\frac{\Delta R_C}{R_C}}_{\text{second-order effect, neglect}}$$

$$0 \cong \frac{\Delta I_C}{I_C} + \frac{\Delta R_C}{R_C}$$

$$I_{OS} = \frac{I_C}{\beta} \left| \frac{\Delta\beta}{\beta} + \frac{\Delta R_C}{R_C} \right| = \boxed{I_B \left| \frac{\Delta\beta}{\beta} + \frac{\Delta R_C}{R_C} \right|}$$

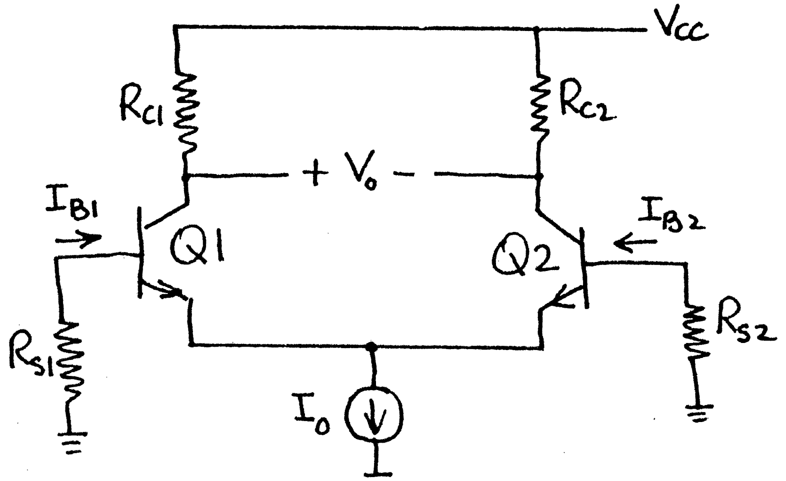
$$I_{OS\,\text{worst case}} = I_B \left(\frac{|\Delta\beta|}{\beta} + \frac{|\Delta R_C|}{R_C} \right)$$

The smaller I_B, the smaller I_{OS}.

Typically $\frac{|\Delta\beta|}{\beta} = 0.1$ and $\frac{|\Delta R_C|}{R_C} = 0.01$.

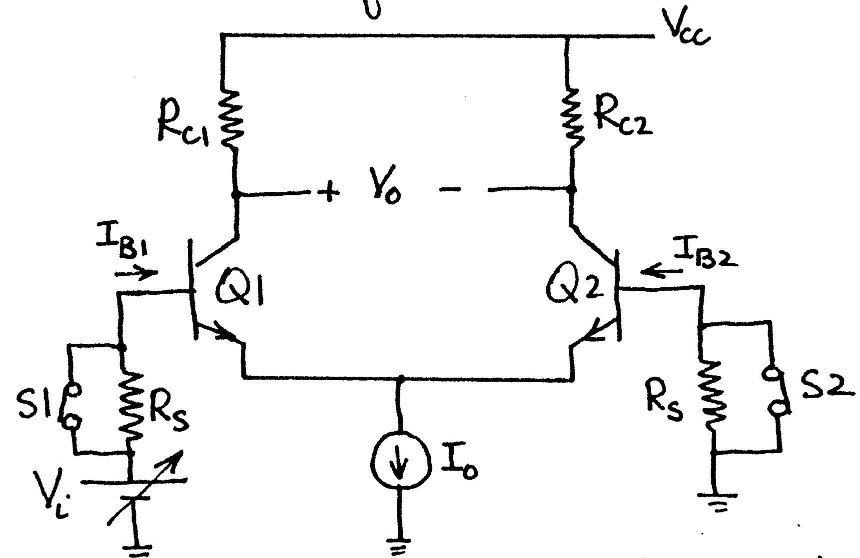
$$I_{OS\ \text{worst case}} = I_B(0.1+0.01) = 0.11\, I_B$$

If the two sources are driven from sources of zero resistance, I_{OS} has no effect on the output. However, the situation changes if there is a resistance in either base lead.



The unequal base currents flowing through unequal source resistances produce a differential voltage at the input which results in an error voltage. This is true even when the two source resistances are equal.

Measurement of V_{OS} and I_{OS}



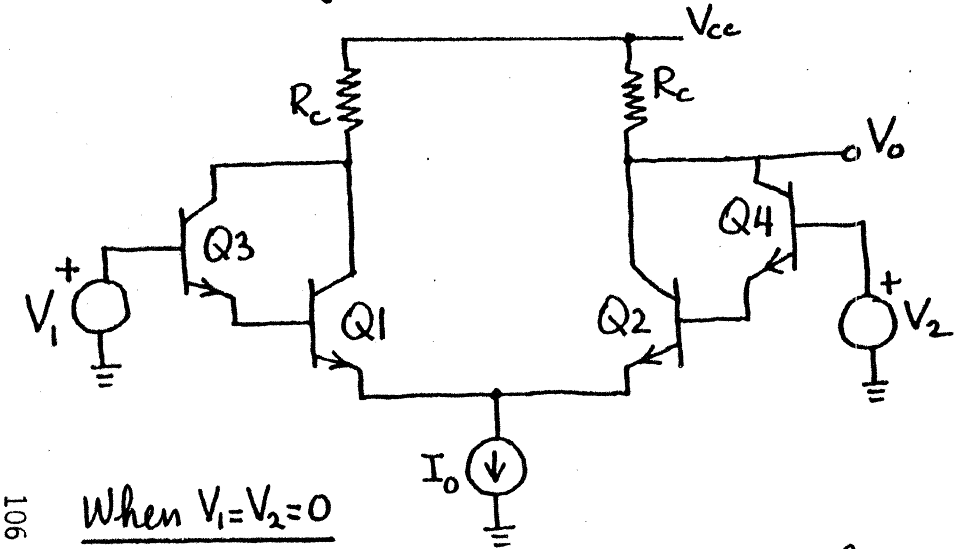
With S1 and S2 closed, adjust V_i to make $V_o=0$. The resulting $|V_i| = V_{OS}$.

If now S1 and S2 are opened V_o will change from 0 because of differential input voltage produced by the base currents. Readjust V_i to V_i' to make V_o zero again. The magnitude of the change in V_i is equal to the magnitude of $(I_{B2}-I_{B1})R_S$, i.e.,

$$|V_i' - V_i| = |V_i' - V_{OS}| = |I_{B1} - I_{B2}|R_S = I_{OS} R_S$$

$$\boxed{I_{OS} = \left|\frac{V_i' - V_{OS}}{R_S}\right|}$$

Increasing the input resistance



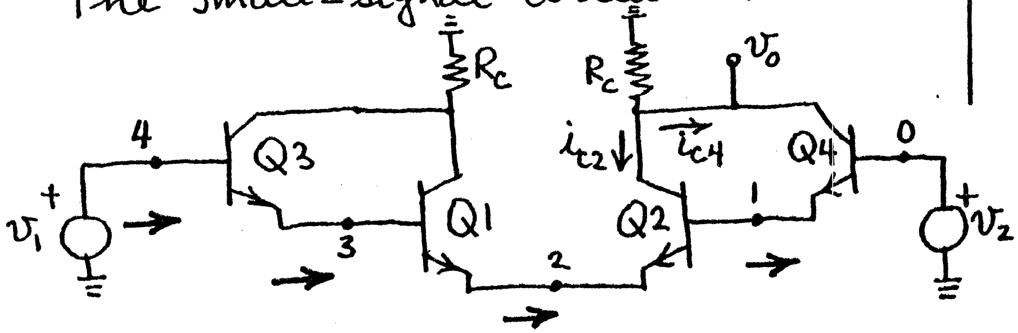
When $V_1 = V_2 = 0$

$$I_{C1} = I_{C2} = \frac{I_o}{2}\,\frac{\beta}{1+\beta} \qquad I_{C3} = I_{C4} = \frac{I_o}{2}\,\frac{\beta}{(1+\beta)^2}$$

$$r_{\pi 1} = r_{\pi 2} = \frac{V_T}{I_{B1}} = \frac{\beta V_T}{I_{C1}} = \frac{2(1+\beta)\,V_T}{I_o}$$

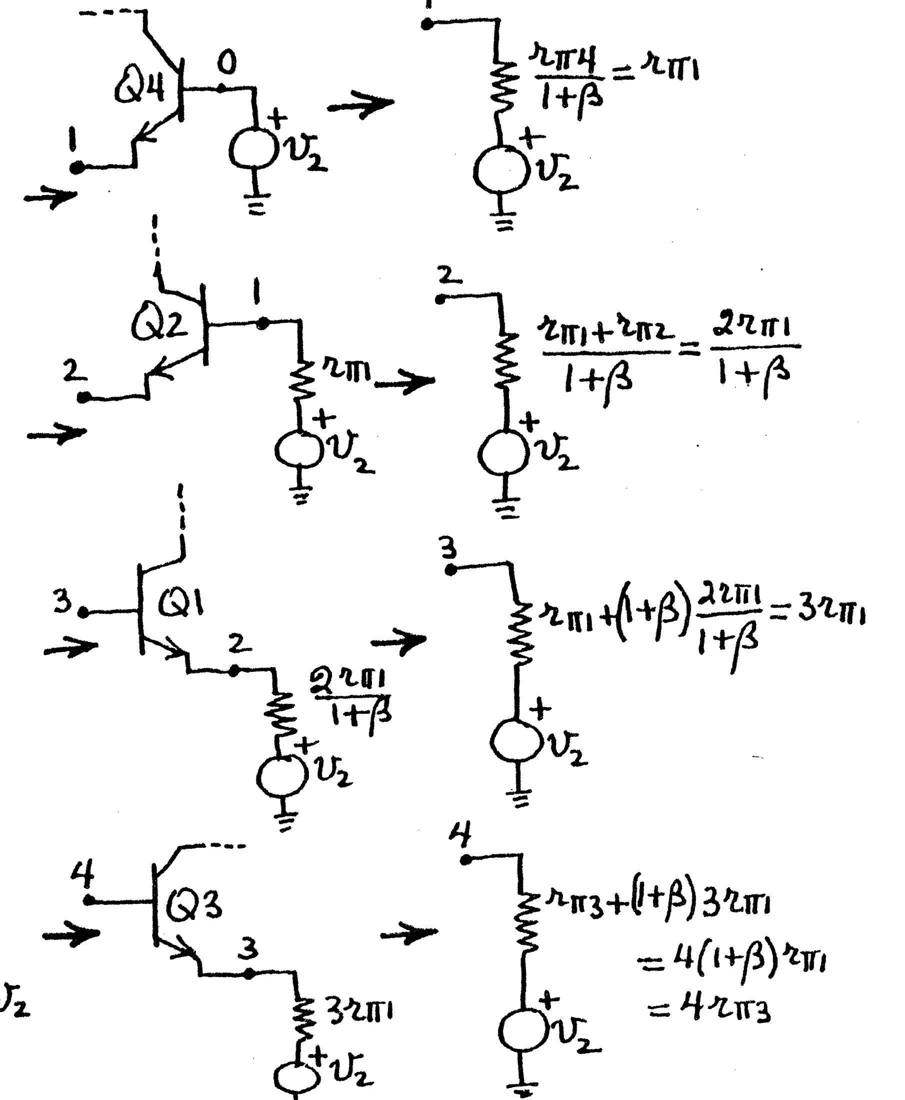
$$r_{\pi 3} = r_{\pi 4} = \frac{V_T}{I_{B3}} = \frac{\beta V_T}{I_{C3}} = \frac{2(1+\beta)^2\,V_T}{I_o} = (1+\beta)\,r_{\pi 1}$$

The small-signal circuit is:

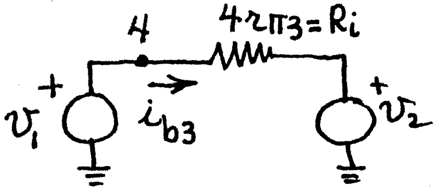


What does source v_1 see?

Moving from right to left, we obtain the successive equivalent circuits. Assume $r_o = \infty$.



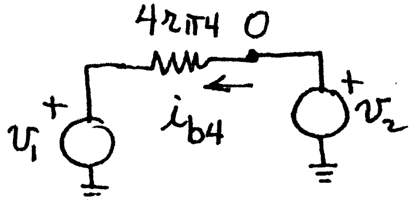
The input equivalent circuit for v_1 is:



where

$$4r_{\pi 3} = \boxed{\frac{8(1+\beta)^2 V_T}{I_o} = R_i}$$

The input equivalent circuit for v_2 is



where

$$4r_{\pi 4} = \boxed{\frac{8(1+\beta)^2 V_T}{I_o}}$$

What is the output equivalent circuit?

By inspection of the small-signal circuit we see that

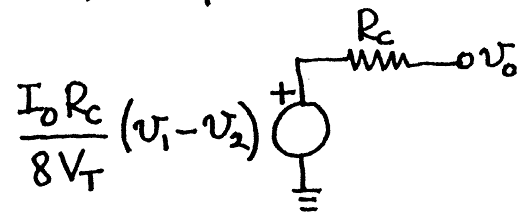
$$v_0 = -(i_{c4} + i_{c2}) R_c = -\beta R_c (i_{b4} + i_{b2})$$

$$= -\beta R_c \left[i_{b4} + (1+\beta) i_{b4} \right] = -\beta R_c (2+\beta) i_{b4}$$

$$= -\beta(2+\beta) R_c \frac{(v_2 - v_1)}{4r_{\pi 4}}$$

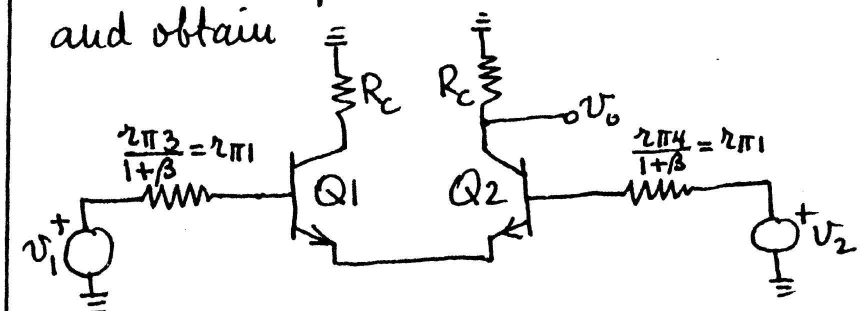
$$= \frac{\beta(2+\beta)}{(1+\beta)^2} \frac{I_o R_c}{8V_T} (v_1 - v_2) \cong \boxed{\frac{I_o R_c}{8V_T}(v_1 - v_2)}$$

The output equivalent circuit is:



Alternative derivation

Since $i_{c1} = (1+\beta) i_{c3}$ and $i_{c2} = (1+\beta) i_{c4}$, neglect i_{c3} relative to i_{c1} and i_{c4} relative to i_{c2}. Use the emitter equivalent circuits of Q_3 and Q_4 and obtain



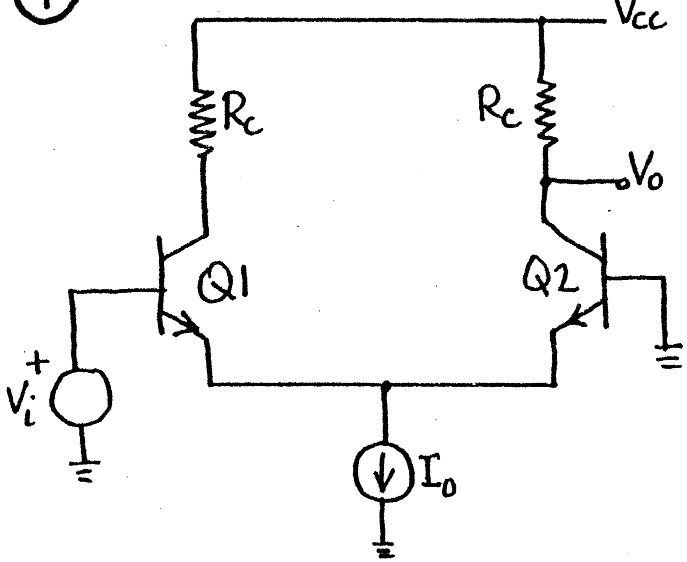
Use the results presented on p94 with $R_E = \infty$, $R_B = r_{\pi 1}$, $r_\pi = r_{\pi 1}$ and obtain

$$v_0 = \frac{\beta R_c}{R_B + r_\pi} \frac{(v_1 - v_2)}{2} = \frac{\beta R_c}{4r_{\pi 1}} (v_1 - v_2) \Big|_{r_{\pi 1} = \frac{2(1+\beta)V_T}{I_o}}$$

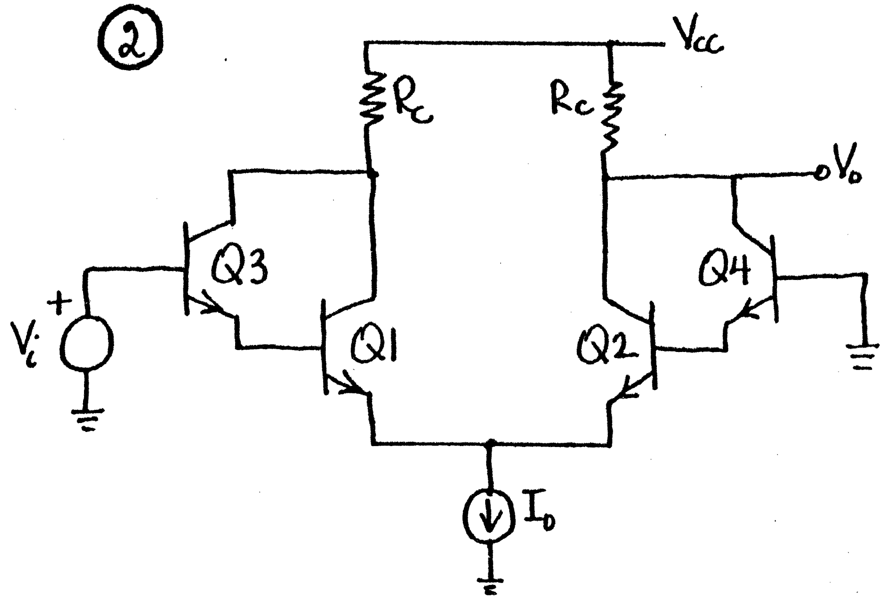
$$= \frac{\beta}{1+\beta} \frac{I_o R_c}{8V_T} (v_1 - v_2) \cong \boxed{\frac{I_o R_c}{8 V_T} (v_1 - v_2)}$$

Comparing input resistance and gain

(1)



(2)



v_i sees a resistance of

$$R_{i1} = 2r_{\pi 1} = \boxed{\frac{4(1+\beta)V_T}{I_o}}$$

The gain is

$$A_{v1} = \frac{1}{2} g_m R_c = \boxed{\frac{I_o R_c}{4V_T}}$$

v_i sees a resistance of

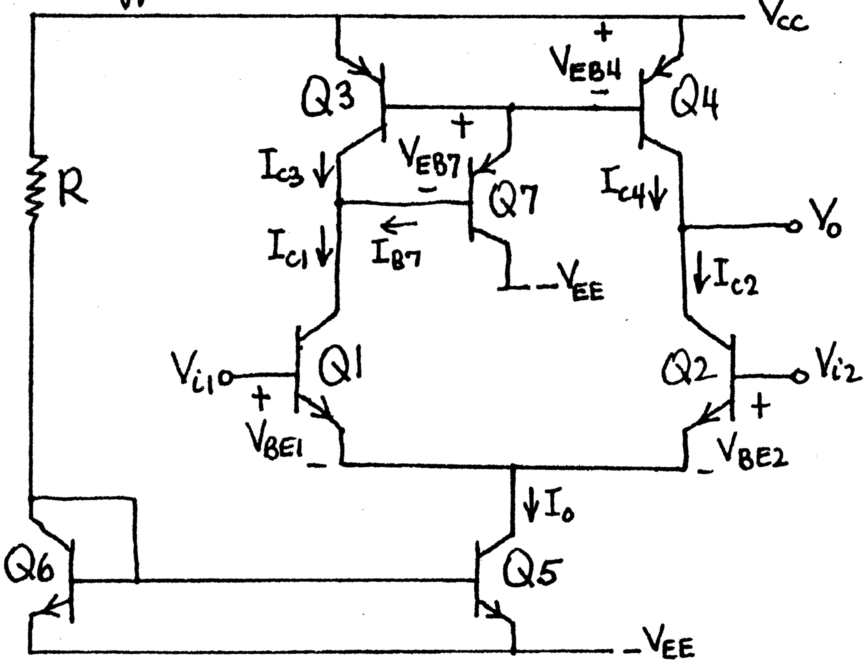
$$R_{i2} = 4r_{\pi 4} = \boxed{\frac{8(1+\beta)^2 V_T}{I_o}} = \underline{2(1+\beta)R_{i1}}$$

The gain is

$$A_{v2} = \boxed{\frac{I_o R_c}{8V_T}} = \underline{\frac{1}{2}A_{v1}}$$

To prevent the transistors from saturating, $\frac{I_o}{2}R_c < V_{CC} - V_{CEsat} + V_{BE}$ where $V_{BE} \cong V_T \ln \frac{I_o/2}{I_s}$.
Note that $(I_o R_c)_{max} \cong 2V_{CC}$ (For $V_{cc} = 15V$, $A_{v1} \cong 300$)

A difference amplifier with active load



Q1 and Q2 form the input of the differential amplifier. The emitter currents are supplied by the current source Q5 which is controlled by Q6. The load on the output transistor Q2 is the current source Q4 which is controlled by Q3. Q7 supplies the base currents for Q3 and Q4 through $-V_{EE}$ while taking a <u>negligibly small current I_{B7}</u> away from the collector junction of Q1 and Q3.

If $V_{i1}=V_{i2}=0$, Q1 matched to Q2, Q3 matched to Q4, and $I_{B7}=0$, then we see by inspection that

$$\boxed{V_o = V_{CC} - V_{EB4} - V_{EB7}}$$

Because $I_{C7} \cong 2I_{B4} = \left.\dfrac{2I_{C4}}{\beta}\right|_{\beta=100} = \dfrac{I_{C4}}{50}$, we would expect $V_{EB7} = V_{EB4} - 0.102$.

Because <u>mismatches in the saturation currents</u> have such an important effect on the output level, we calculate <u>V_o with $V_{i1}=V_{i2}=0$</u>. Then $V_{BE1}=V_{BE2}$

$$\left\{\begin{aligned}
I_{C1} &= I_{S1} e^{\frac{V_{BE2}}{V_T}}\left(1+\frac{V_{CC}-V_{EB4}-V_{EB7}+V_{BE2}}{V_{AN}}\right)\\
I_{C2} &= I_{S2} e^{\frac{V_{BE2}}{V_T}}\left(1+\frac{V_o+V_{BE2}}{V_{AN}}\right)\\
I_{C3} &= I_{S3} e^{\frac{V_{EB4}}{V_T}}\left(1+\frac{V_{EB4}+V_{EB7}}{V_{AP}}\right)\\
I_{C4} &= I_{S4} e^{\frac{V_{EB4}}{V_T}}\left(1+\frac{V_{CC}-V_o}{V_{AP}}\right)
\end{aligned}\right\}$$

Note that it was assumed $V_{A1}=V_{A2}=V_{AN}$ and $V_{A3}=V_{A4}=V_{AP}$. Also I_{B7} was assumed 0. Since <u>$I_{C1}=I_{C3}$</u> and <u>$I_{C2}=I_{C4}$</u>, we obtain

$$\left\{\begin{aligned}
I_{S1} e^{\frac{V_{BE2}}{V_T}}\left(1+\frac{V_{CC}-V_{EB4}-V_{EB7}+V_{BE2}}{V_{AN}}\right) &= I_{S3} e^{\frac{V_{EB4}}{V_T}}\left(1+\frac{V_{EB4}+V_{EB7}}{V_{AP}}\right)\\
I_{S2} e^{\frac{V_{BE2}}{V_T}}\left(1+\frac{V_o+V_{BE2}}{V_{AN}}\right) &= I_{S4} e^{\frac{V_{EB4}}{V_T}}\left(1+\frac{V_{CC}-V_o}{V_{AP}}\right)
\end{aligned}\right\}$$

$$\frac{I_{S1}\left(1+\frac{V_{CC}-V_{EB4}-V_{EB7}+V_{BE2}}{V_{AN}}\right)}{I_{S2}\left(1+\frac{V_o+V_{BE2}}{V_{AN}}\right)} = \frac{I_{S3}\left(1+\frac{V_{EB4}+V_{EB7}}{V_{AP}}\right)}{I_{S4}\left(1+\frac{V_{CC}-V_o}{V_{AP}}\right)}$$

Solving for V_o, we obtain

$$V_0 \cong \frac{\left(\frac{I_{S1}}{I_{S2}}\frac{I_{S4}}{I_{S3}}-1\right)V_{AN}+\frac{I_{S1}}{I_{S2}}\frac{I_{S4}}{I_{S3}}\left[V_{cc}\left(1+\frac{V_{AN}}{V_{AP}}\right)+V_{BE2}-V_{EB4}-V_{EB7}\right]-\left[V_{BE2}+(V_{EB4}+V_{EB7})\frac{V_{AN}}{V_{AP}}\right]}{1+\frac{I_{S1}}{I_{S2}}\frac{I_{S4}}{I_{S3}}\frac{V_{AN}}{V_{AP}}}$$

where terms divided by $V_{AN}V_{AP}$ have been neglected. If mismatches in I_s are small, V_o can be approx. as

$$V_0 \cong \frac{\left(\frac{I_{S1}}{I_{S2}}\frac{I_{S4}}{I_{S3}}-1\right)V_{AN}+\left[V_{cc}\left(1+\frac{V_{AN}}{V_{AP}}\right)+V_{BE2}-V_{EB4}-V_{EB7}\right]-\left[V_{BE2}+(V_{EB4}+V_{EB7})\frac{V_{AN}}{V_{AP}}\right]}{1+\frac{V_{AN}}{V_{AP}}}$$

After dividing through, this expression simplifies to

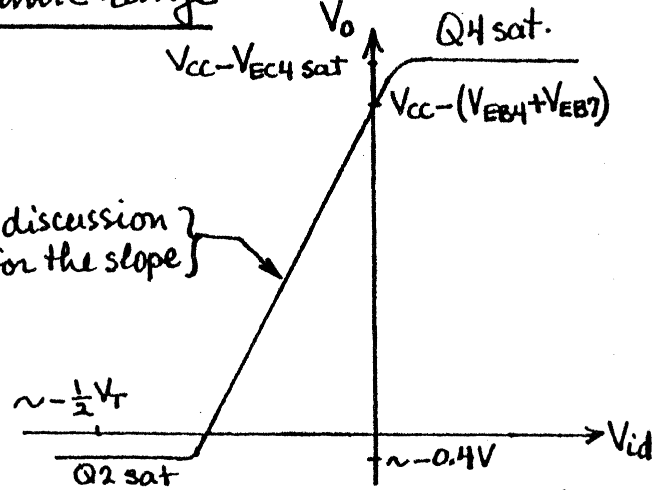
$$\boxed{V_0 = \left(\frac{I_{S1}}{I_{S2}}\frac{I_{S4}}{I_{S3}}-1\right)\frac{V_{AN}}{1+\frac{V_{AN}}{V_{AP}}}+\left[V_{CC}-(V_{EB4}+V_{EB7})\right]}$$

If there were no mismatch, i.e., $I_{S1}=I_{S2}$ and $I_{S3}=I_{S4}$, the first term in the above expression would be 0. However, even a small mismatch in I_s's would cause a considerable change in the quiescent value of V_o because the mismatch term is multiplied by a large number, namely $\frac{V_{AN}}{1+V_{AN}/V_{AP}}$. For example, for $V_{AN}=120V$, $V_{AP}=60V$ and $\frac{I_{S1}}{I_{S2}}=1.01$ and $\frac{I_{S4}}{I_{S3}}=1.01$, V_o becomes $\underline{V_o = 0.8+V_{cc}-(V_{EB4}+V_{EB7})}$.

It is interesting to note that the emitter current source I_o has negligible effect on the quiescent value of the output voltage. It influences only V_{EB4} and V_{EB7}. If the two halves of the differential amplifier were perfectly matched, then the current produced by Q5 will divide evenly resulting in $I_{C4}=\frac{I_o}{2}$. Correspondingly

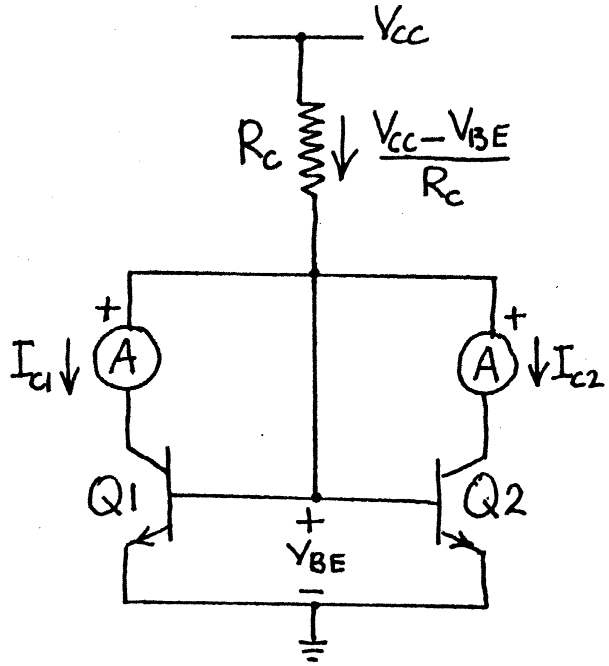
$$V_{EB4} \cong V_T \ln\frac{I_o/2}{I_{SP}}, \quad V_{BE7} \cong V_T \ln\frac{I_o/\beta}{I_{SP}} = V_{EB4}-0.102$$

Dynamic range



Since the collector currents remain essentially constant, the transistor parameters do not change appreciably. The result is a transfer curve that is quite straight

Measurement of mismatch



$$\begin{cases} I_{C1} = I_{S1}\, e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{BE}}{V_{A1}}\right) \\ I_{C2} = I_{S2}\, e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{BE}}{V_{A2}}\right) \end{cases}$$

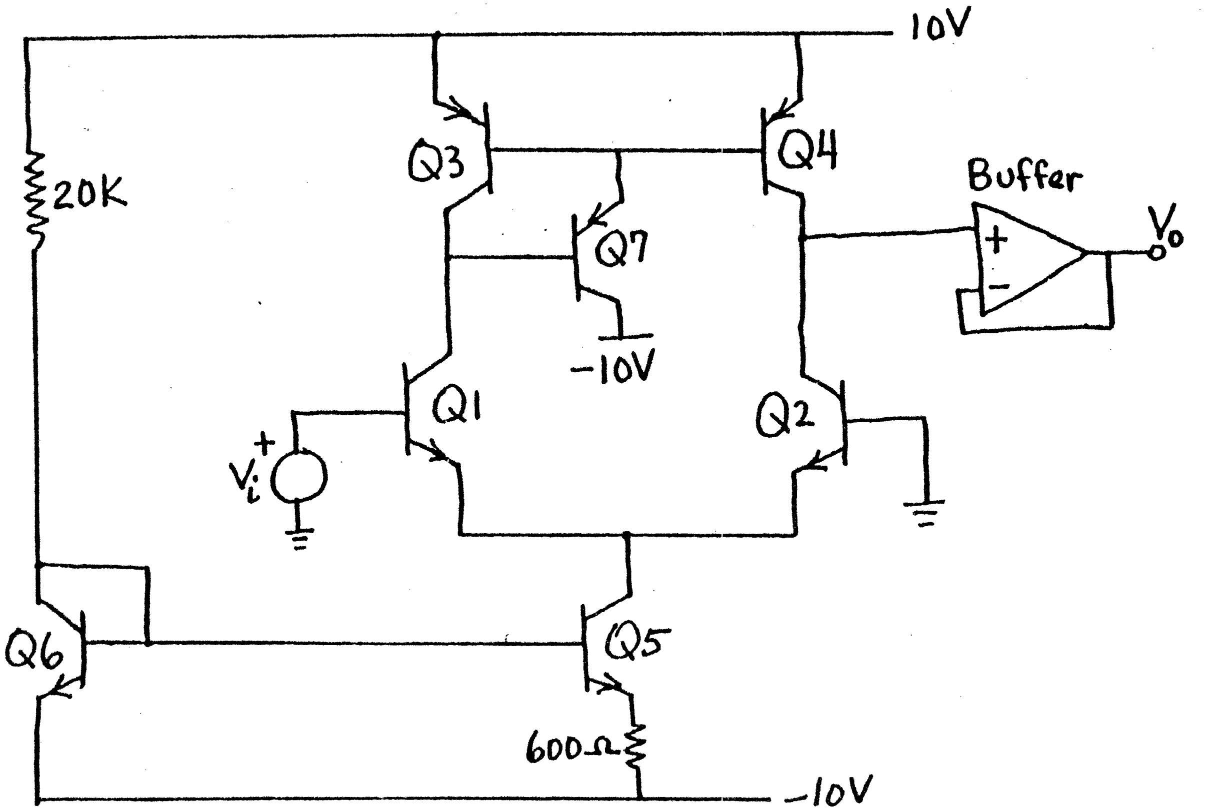
Even a 10% mismatch in V_A's will hardly have an effect on I_C's.

$$\boxed{\frac{I_{C1}}{I_{C2}} = \frac{I_{S1}}{I_{S2}}}$$

Demonstration

1. Use ammeter readings to obtain the $\frac{I_{S1}}{I_{S2}}$ ratio for an IC.
2. Show that the $\frac{I_{S1}}{I_{S2}}$ ratio is independent of temperature and value of the collector current.
3. Repeat 1 and 2 for a discrete pair of transistors.

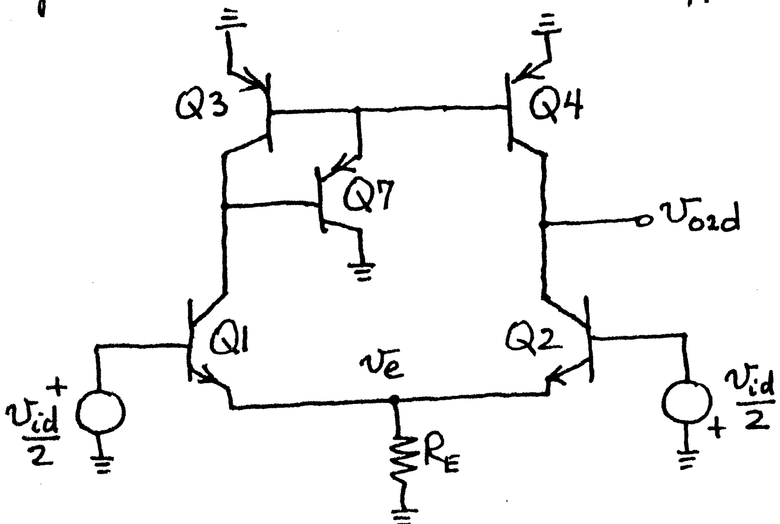
L15: Demonstration of differential amplifier with active load



1. Display V_o vs V_i curve
2. With matched (Q_1, Q_2) and $(Q_3, Q4)$, $V_o = V_{CC} - V_{EB4} - V_{EB7} \cong 10 - 0.6 - 0.5 = 8.9\,V$
3. A ±2% mismatch in the I_{S1}/I_{S2} ratio will result in $V_o \cong 8.9 \pm 0.8 = \begin{cases} 9.7V \\ 8.1V \end{cases}$

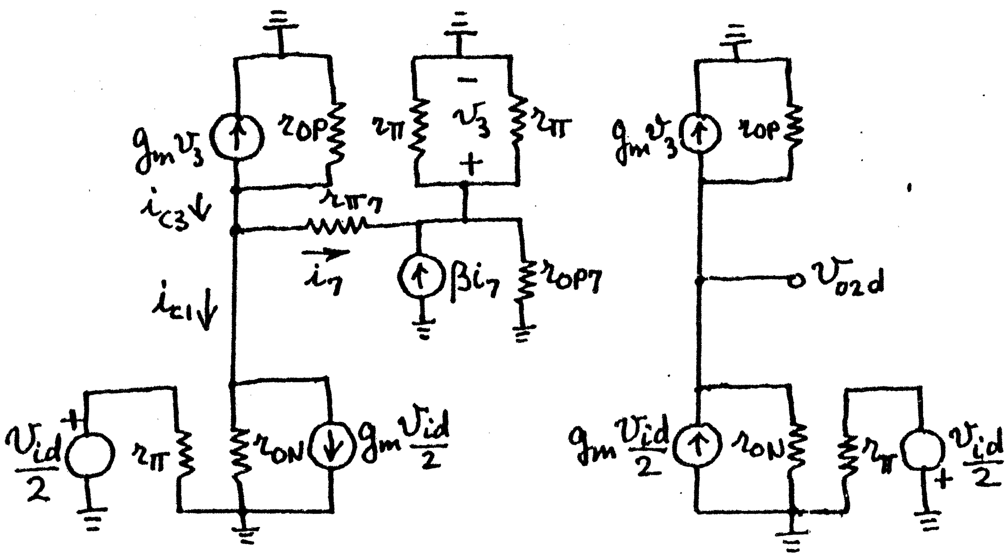
Determination of the differential gain

In amplifiers having CS's as collector loads g_m, r_π, β, and r_o do not vary much with the operating point resulting in practically constant gain over the entire dynamic range. This gain can be calculated using the small signal model. (See also discussion on pp 83-86.)

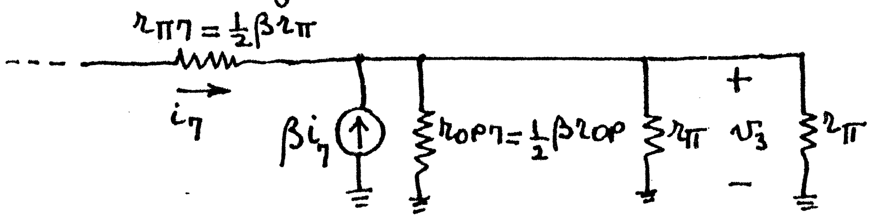


R_E represents the output resistance of Q5 current source. Because $I_{C1} \cong I_{C2} \cong I_{C3} \cong I_{C4}$, no distinction will be made on the r_π's and g_m's of these transistors. They will be designated by r_π and g_m. The r_o's of the NPN transistors will be designated by r_{oN}; similarly r_o's of PNP transistors will be designated by r_{oP}. Although the r_o's of the transistors rise slightly in value as the collector-to-emitter voltage varies from ~ 0 to $\sim V_{CC}$, this second-order effect will be neglected. Since $I_{C7} \cong \frac{2 I_{C3}}{\beta}$, $r_{\pi 7} \cong \frac{\beta}{2} r_\pi$, $r_{oP7} \cong \frac{1}{2}\beta r_{oP}$. If the circuit were symmetric about a vertical line through its middle, the emitter voltage v_E would have been zero because of the difference-mode excitation. While the bottom half is symmetric, the top half is not. Nonetheless, if the r_o's of the NPN transistors were infinite, the lack of symmetry in the collector circuits of Q1 and Q2 wouldn't have mattered because changes in the collector circuits would not then have any effect on the base and emitter circuits, and v_E would still have been 0.

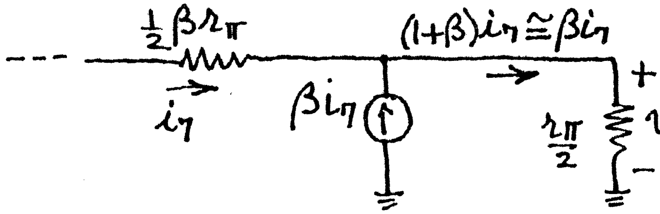
For $r_{oN} \neq \infty$, v_E will be slightly different from 0. Still, as long as r_{oN} is large, to a first-order approx. v_E can be taken as 0, thus decoupling Q1 and Q2 at their emitters and in so doing removing altogher any effect of R_E on the differential gain.

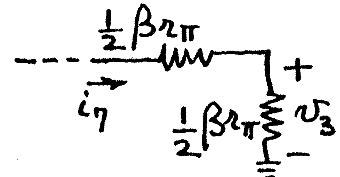


The portion of the circuit consisting of Q7 and the bases of Q3 and Q4 can be simplified.

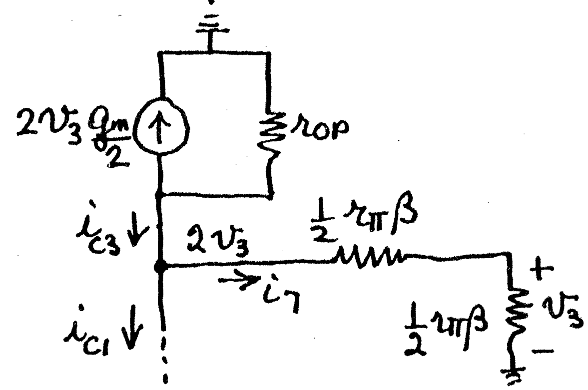


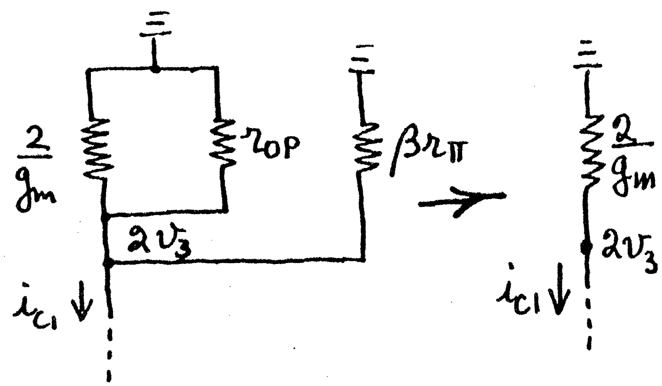
$\frac{1}{2}\beta r_{oP} \gg \frac{r_\pi}{2}$ $\left(\frac{1}{2}\beta\frac{V_{AP}}{I_C} \gg \frac{\beta}{2}\frac{V_T}{I_C}\right)$





We now combine this result with the collector equivalent circuit of Q3.

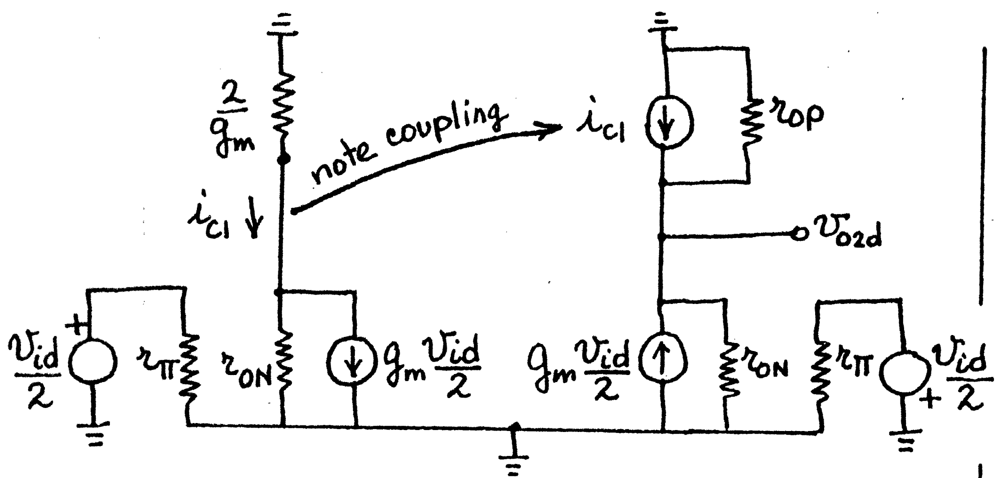




$\frac{2}{g_m} \ll r_{oP}$ $\left(2\frac{V_T}{I_C} \ll \frac{V_{AP}}{I_C} \rightarrow 2V_T \ll V_{AP}\right)$

$\frac{2}{g_m} \ll \beta r_\pi$ $\left(2\frac{V_T}{I_C} \ll \beta^2\frac{V_T}{I_C} \rightarrow 2 \ll \beta^2\right)$

So $2v_3 \cong -i_{c1}\frac{2}{g_m}$ and $g_m v_3 \cong -i_{c1}$



Since $\frac{2}{g_m} \ll r_{ON}$, $\quad i_{c1} = g_m \frac{v_{id}}{2}$

$$v_{O2d} = \left(g_m \frac{v_{id}}{2} + i_{c1}\right) \frac{r_{ON}\, r_{OP}}{r_{ON}+r_{OP}} = g_m v_{id} \frac{r_{ON}\, r_{OP}}{r_{ON}+r_{OP}}$$

$$\boxed{A_d = \frac{v_{O2d}}{v_{id}} = g_m \frac{r_{ON}\, r_{OP}}{r_{ON}+r_{OP}}}$$

Using the approx. $r_o = \frac{V_A + V_{CE}}{I_c} \cong \frac{V_A}{I_c}$, we obtain

$$A_d \cong \frac{I_c}{V_T} \frac{\frac{V_{AN}}{I_c} \frac{V_{AP}}{I_c}}{\frac{V_{AN}}{I_c} + \frac{V_{AP}}{I_c}} = \boxed{\frac{1}{V_T}\left(\frac{V_{AN} V_{AP}}{V_{AN}+V_{AP}}\right)}$$

{ See also pp 85–86

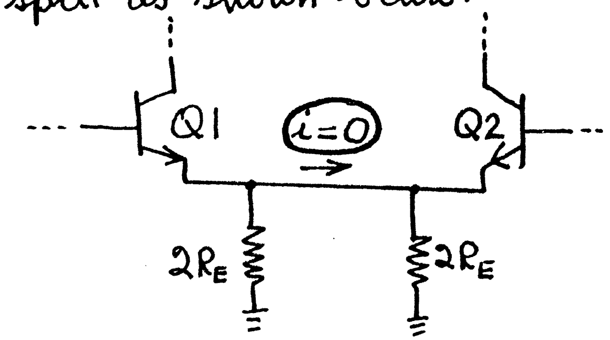
For $V_{AN} = 120V$, $V_{AP} = 60V$, and $V_T = 26mV$, we get

$$A_d = \frac{1}{26 \times 10^{-3}} \frac{120 \times 60}{180} = \boxed{1538}$$

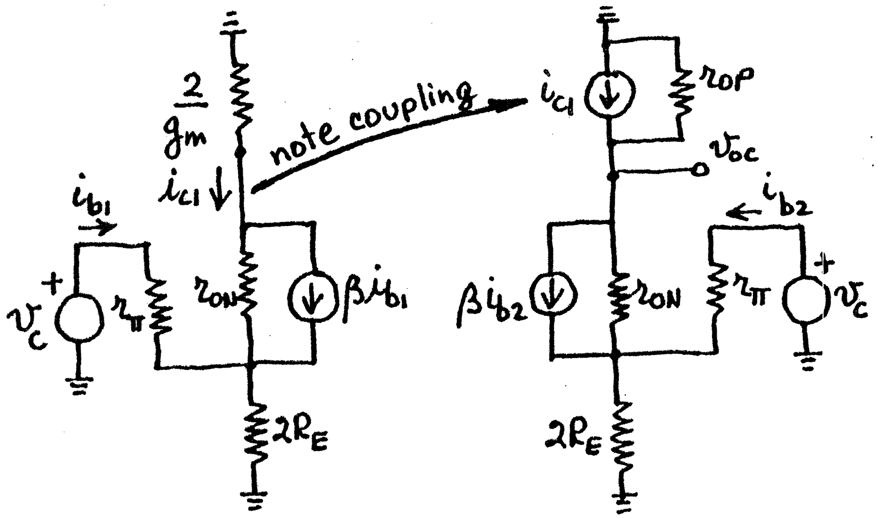
If we assume the V_{O2} vs. V_{id} curve to be a straight line (see p110) having a slope of 1538, then for $V_{CC} = 15V$ it takes a V_{id} of $\frac{15}{1538} V \cong \underline{10\,mV}$ to drive the output from 0 to 15V.

Determination of the common-mode gain

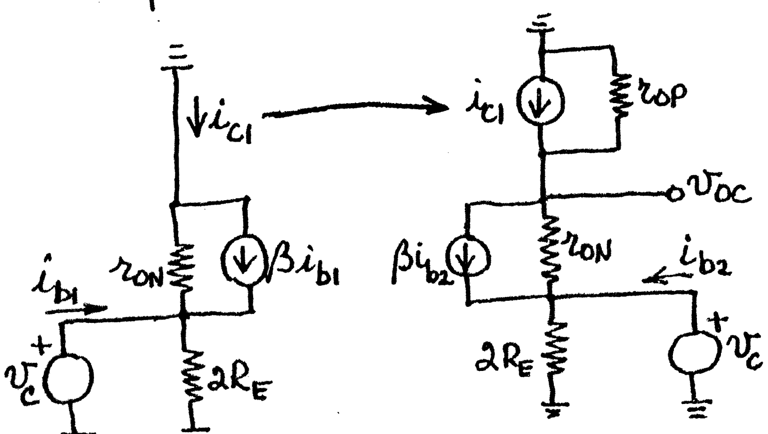
Again, even though the circuit is not symmetric, we can argue that the current between the emitters is 0 if the output resistance R_E of the Q5 current source is split as shown below.



The upper portion of the circuit consisting of Q_3, Q_4, and Q_7 can again be simplified to the equivalent circuits shown for the differential mode excitation in upper left column on this page. The resulting circuit is shown on next page.



Because r_π is so much smaller than the resistance following it, practically all of v_c appears at the emitters. Stated differently, letting r_π to equal zero does not adversely affect the responses of the circuit. Similarly the $2/g_m$ resistor can be replaced with a short circuit. The result is



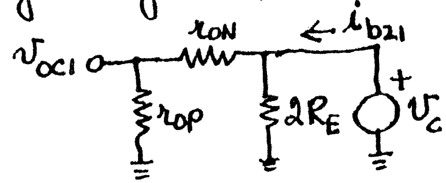
By inspection of the left half of the circuit we see that

$$\begin{cases} v_c = (1+\beta)\, i_{b1} \dfrac{r_{oN}\, 2R_E}{r_{oN}+2R_E} \\[2ex] i_{c1} = \beta i_{b1} - \dfrac{v_c}{r_{oN}} \end{cases}$$

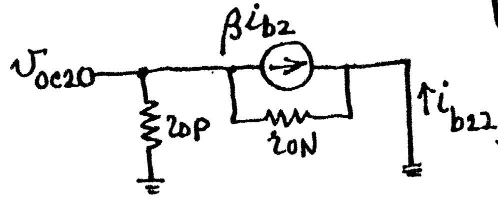
Solving for i_{c1} we obtain

$$\boxed{i_{c1} = -v_c\left(\frac{1}{r_{oN}} - \frac{\beta}{1+\beta}\,\frac{r_{oN}+2R_E}{r_{oN}\,2R_E}\right)}$$

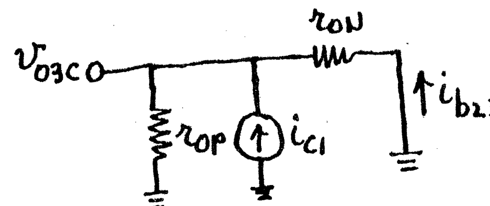
The right half of the circuit will be solved by using the principle of superposition.



$$\begin{cases} i_{b21} = \dfrac{v_c}{\dfrac{2R_E(r_{oN}+r_{oP})}{2R_E+r_{oN}+r_{oP}}} \\[2ex] v_{oc1} = v_c \dfrac{r_{oP}}{r_{oN}+r_{oP}} \end{cases}$$



$$\begin{cases} i_{b22} = -\beta i_{b2} \dfrac{r_{oN}}{r_{oN}+r_{oP}} \\[2ex] v_{oc2} = -\beta i_{b2} \dfrac{r_{oN}\, r_{oP}}{r_{oN}+r_{oP}} \end{cases}$$



$$\begin{cases} i_{b23} = -i_{c1} \dfrac{r_{oP}}{r_{oP}+r_{oN}} \\[2ex] v_{oc3} = i_{c1} \dfrac{r_{oP}\, r_{oN}}{r_{oP}+r_{oN}} \end{cases}$$

$$i_{b2} = i_{b21} + i_{b22} + i_{b23}$$

$$= \frac{v_c(2R_E + r_{oN} + r_{oP})}{2R_E(r_{oN} + r_{oP})} - \frac{\beta i_{b2} r_{oN}}{r_{oN} + r_{oP}} - \frac{i_{c1} r_{oP}}{r_{oN} + r_{oP}} \quad (1)$$

$$v_{oc} = v_{oc1} + v_{oc2} + v_{oc3}$$

$$= \frac{v_c r_{oP}}{r_{oN} + r_{oP}} - \frac{\beta i_{b2} r_{oN} r_{oP}}{r_{oN} + r_{oP}} + \frac{i_{c1} r_{oP} r_{oN}}{r_{oP} + r_{oN}} \quad (2)$$

Substitude for i_{c1} in the first equation and solve for i_{b2}. Using this i_{b2} and i_{c1}, solve the second equation for v_{oc}. The result is

$$\boxed{v_{oc} = 0}$$

It should be emphasized that <u>no algebraic approximations were made in arriving at this remarkable result</u>. Note that the zero output is independent of the output resistance of the current source transistor Q5. Consequently the common-mode-rejection-ratio of this amplifier would be infinite.

<u>Offset voltage calculation</u>

The expression for the quiescent value of the output with both input bases grounded was derived on p110. It is reproduced here for convenience.

$$V_o = \underbrace{\left(\frac{I_{S1}}{I_{S2}}\frac{I_{S4}}{I_{S3}} - 1\right)\frac{V_{AN}}{1 + \frac{V_{AN}}{V_{AP}}}}_{\substack{\text{Offset output voltage} \\ \text{caused by saturation} \\ \text{current mismatches}}} + \left[V_{CC} - (V_{EB4} + V_{EB7})\right]$$

The expression for the differential-mode gain was derived on p 115 and is reproduced here for convenience.

$$A_d = \frac{1}{V_T}\frac{V_{AN}V_{AP}}{V_{AN} + V_{AP}}$$

To drive the output to its quiescent value (under perfectly matched conditions) of $V_{CC} - (V_{EB4} + V_{EB7})$ requires that <u>an offset voltage be introduced</u> at the input of the differential amplifier. This voltage can be obtained by dividing the output offset voltage with the differential gain.

$$V_{os} = \frac{\left(\frac{I_{S1}}{I_{S2}}\frac{I_{S4}}{I_{S3}} - 1\right)\left(\frac{V_{AN}V_{AP}}{V_{AN}+V_{AP}}\right)}{\frac{1}{V_T}\left(\frac{V_{AN}V_{AP}}{V_{AN}+V_{AP}}\right)}$$

$$V_{os} = V_T\left[\left(\frac{I_{S1}}{I_{S2}}\right)\left(\frac{I_{S4}}{I_{S3}}\right) - 1\right]$$

To simplify, let $I_{S2} = I_{SN}$, $I_{S1} = I_{SN} + \Delta I_{SN}$, $I_{S3} = I_{SP}$, $I_{S4} = I_{SP} + \Delta I_{SP}$. Then

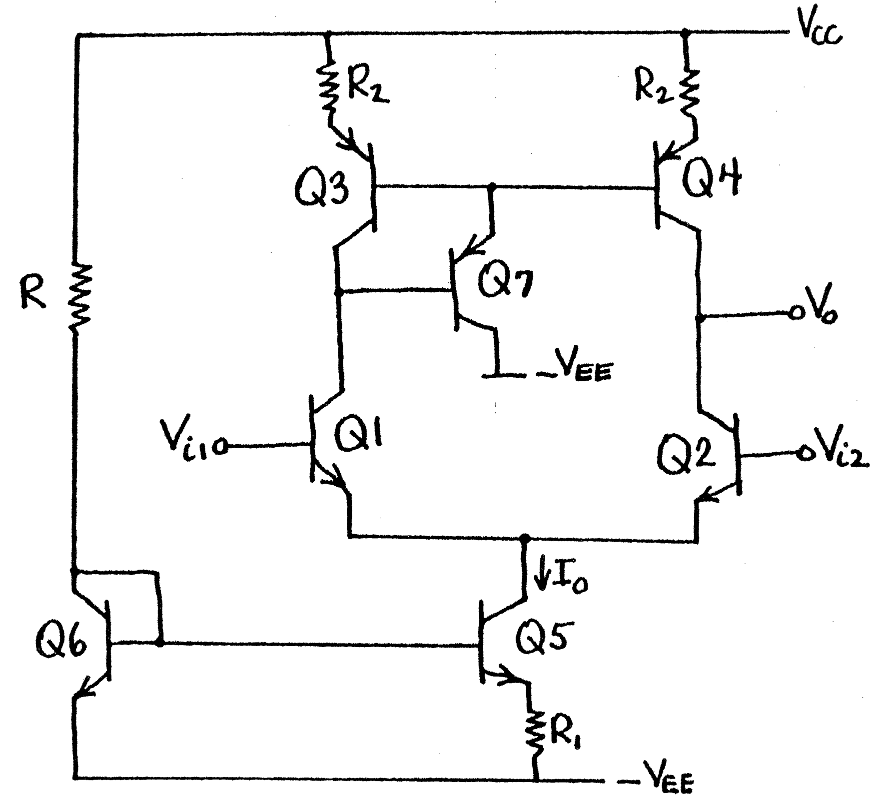
$$V_{os} = V_T\left[\left(1 + \frac{\Delta I_{SN}}{I_{SN}}\right)\left(1 + \frac{\Delta I_{SP}}{I_{SP}}\right) - 1\right]$$

$$V_{os} \cong V_T\left(\frac{\Delta I_{SN}}{I_{SN}} + \frac{\Delta I_{SP}}{I_{SP}}\right)$$

$$\boxed{V_{os\ \text{worst case}} = V_T\left(\frac{|\Delta I_{SN}|}{I_{SN}} + \frac{|\Delta I_{SP}|}{I_{SP}}\right)}$$

If saturation current mismatches can be held within 1%, then $V_{os\ \text{worst case}} \leq 0.52\text{mV}$. It would take an input voltage of ± 0.52mV to drive the output to 0.

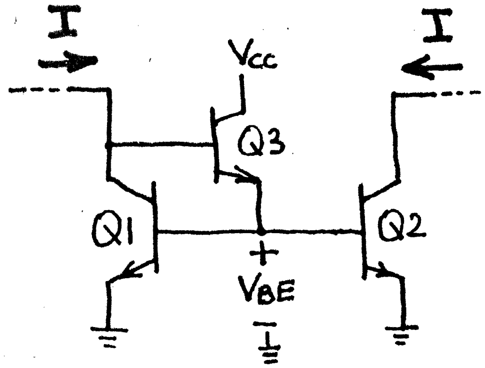
Improving the circuit further



R_1 allows us to use a smaller R to establish I_0. Also it makes the output resistance of Q5 higher (see also discussion presented on pp 71–72).

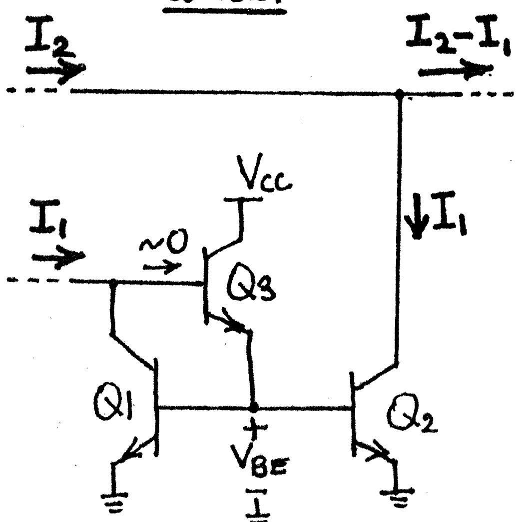
R_2 forces a better match of the collector currents of Q3 and Q4 (see also pp 64–65). It also makes the output resistance of Q4 (active load) higher thereby increasing the differential gain.

A current mirror

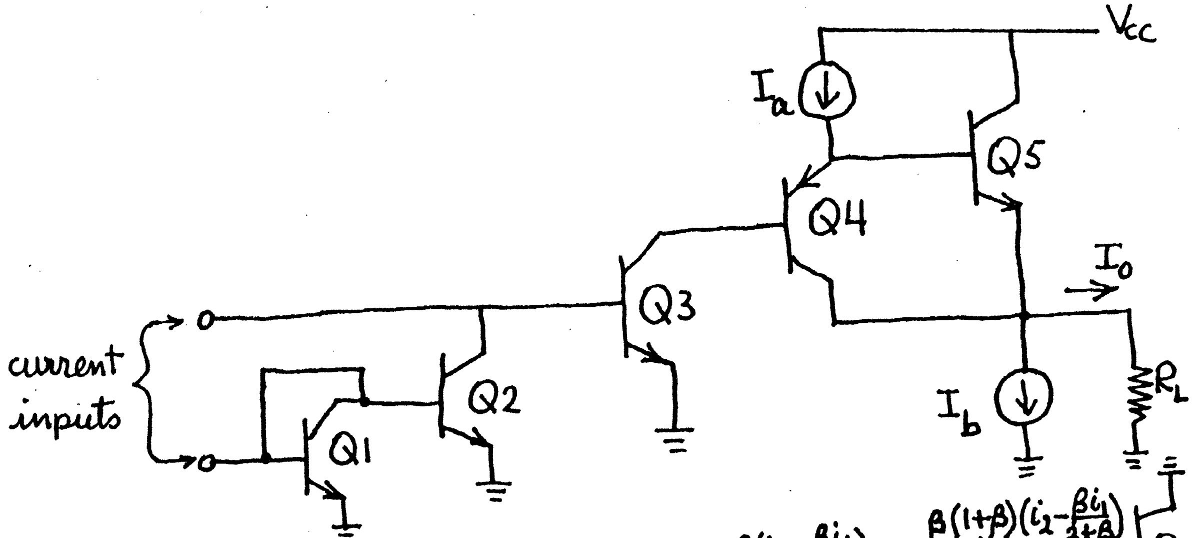


If I_{B3} is neglected, $I_{C1} = I_{C2}$ as shown

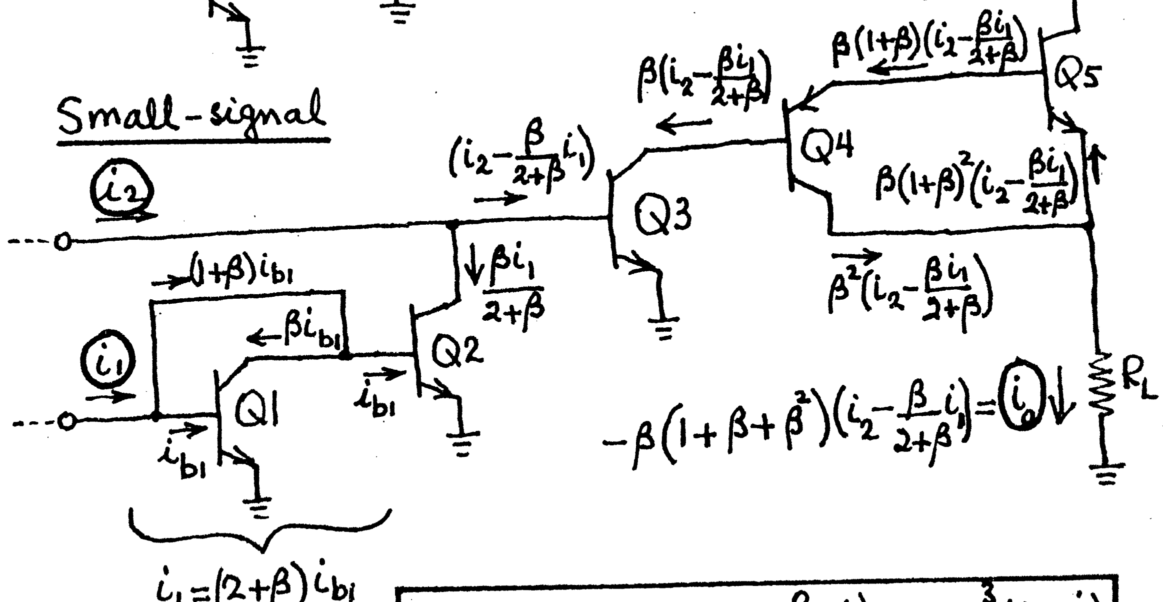
A current differencing circuit



A current difference amplifier using a single supply



Small-signal

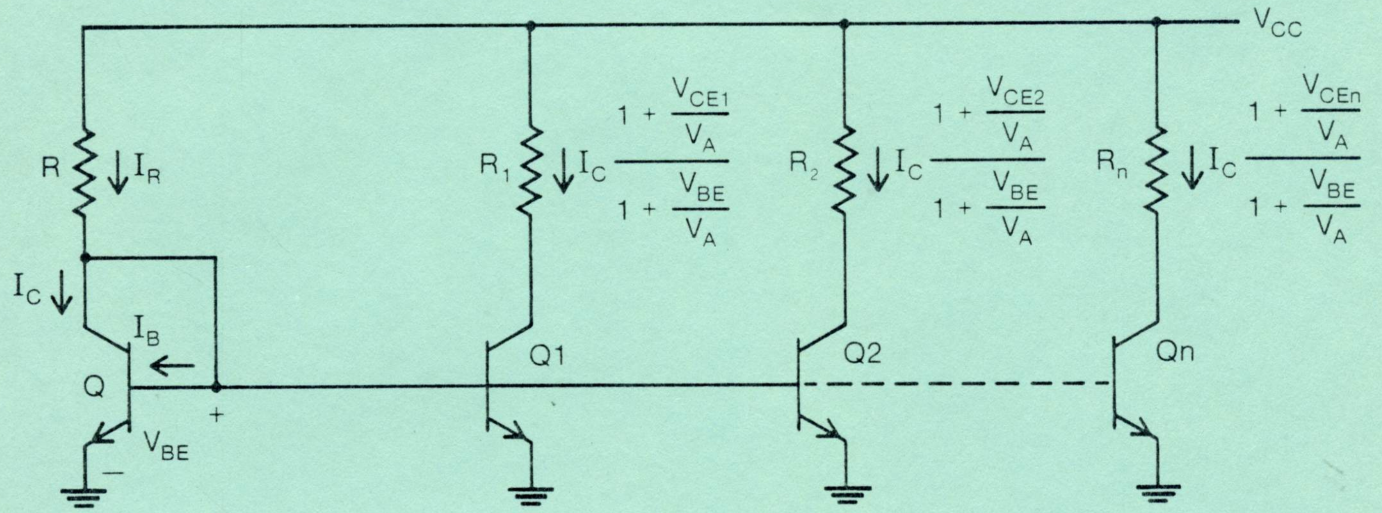


$$\boxed{i_o = -\beta(1+\beta+\beta^2)\left(i_2 - \frac{\beta}{2+\beta} i_1\right) \cong -\beta^3 (i_2 - i_1)}$$

A Self Study Subject

FUNDAMENTALS & APPLICATIONS OF ANALOG INTEGRATED CIRCUITS

PART I
LOW FREQUENCY ANALYSIS & DESIGN



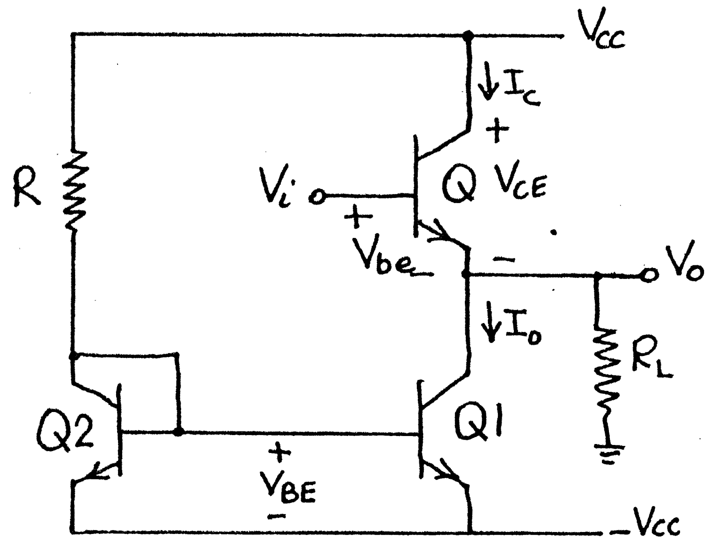
Study Guide
for

MODULE D
Class A, B, & AB Output Stages & the μA741 Operational Amplifier

Colorado State University
Engineering Renewal
& Renewal & Growth Program

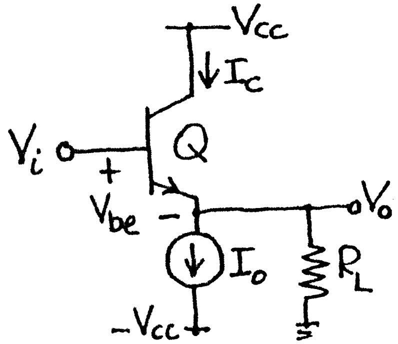
Aram Budak

16: Class-A emitter-follower output stage



$$\boxed{I_o = \frac{2V_{CC}-V_{BE}}{R}}$$

V_A assumed ∞.
Q1 and Q2 matched.



$$V_o = V_i - V_{be}$$
$$= V_i - V_T \ln \frac{I_c}{I_s}$$

$$I_c \cong I_e = I_o + \frac{V_o}{R_L}$$

$$V_o = V_i - V_T \ln\left(\frac{I_o + \frac{V_o}{R_L}}{I_s}\right)$$

$$V_o = V_i - V_T \ln \frac{I_o}{I_s}\left(1 + \frac{V_o}{I_o R_L}\right) = V_i - \underbrace{V_T \ln \frac{I_o}{I_s}}_{V_{BE}} - \boxed{V_T \ln\left(1 + \frac{V_o}{I_o R_L}\right)}$$

where $V_{BE} = V_{be}$ when $V_o = 0$

$$\boxed{\begin{aligned} V_o &= V_i - V_{BE} - V_T \ln\left(1 + \frac{V_o}{I_o R_L}\right) \\ I_c &= I_o + \frac{V_o}{R_L} \end{aligned}}$$

As V_i increases V_o and I_c increase until either Q gets sat. (at which time $V_o = V_{CC} - V_{CEsat}$) or maximum allowable current I_{cmax} for Q is reached (at which time $V_o = (I_{cmax} - I_o)R_L$).

As V_i decreases V_o and I_c decrease until either Q gets cut off (at which time $V_o = -I_o R_L$) or the current source transistor Q1 gets sat (at which time $V_o = -V_{CC} + V_{CEsat}$).

V_o vs. V_i, I_c vs. V_i, and I_c vs. V_{CE} curves

There are 3 cases (excluding the I_{cmax} limitation).

1. Q gets cut off and Q1 gets sat. for the same negative value of V_i. This requires that $V_o = -I_o R_L = -V_{CC} + V_{CEsat}$

$$\boxed{I_o R_L = V_{CC} - V_{CEsat}}$$

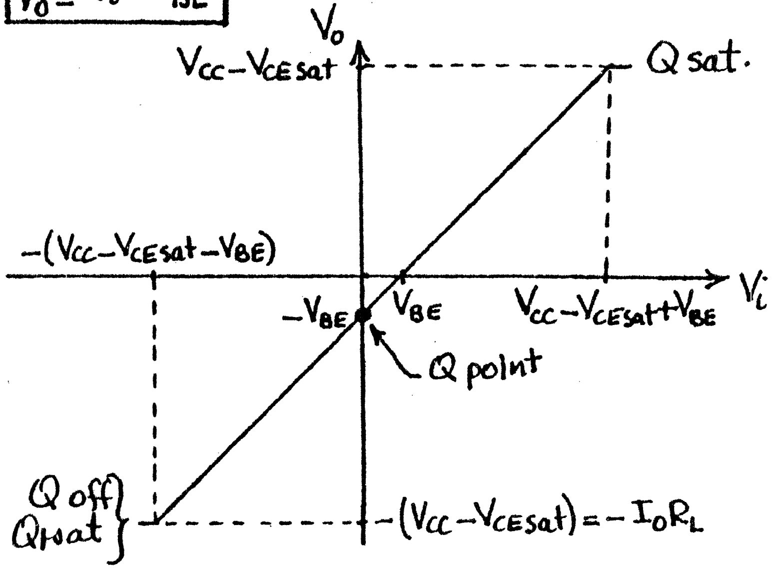
a) <u>The V_o vs. V_i curve</u>

$$V_o = V_i - V_{BE} - V_T \ln\left(1 + \frac{V_o}{I_o R_L}\right)$$

$$= V_i - V_{BE} - V_T \ln\left(1 + \frac{V_o}{V_{CC} - V_{CEsat}}\right)$$

The logarithmic term is negligible.

$$\boxed{V_o \cong V_i - V_{BE}}$$



Error caused by neglected log. term.

$$-V_T \ln\left(1 + \frac{V_o}{V_{CC} - V_{CEsat}}\right) = \begin{cases} \underline{V_o = V_{CC} - V_{CEsat}} = -V_T \ln 2 = -18\,\text{mV} \\ \underline{V_o = -.99(V_{CC} - V_{CEsat})} = -V_T \ln 0.01 = 120\,\text{mV} \end{cases}$$

Since $I_C = I_S e^{V_{BE}/V_T}$ [instead of the more accurate expression of $I_C = I_S(e^{V_{BE}/V_T} - 1)$] cutoff is achieved only when $V_{BE} = -\infty$ which requires $V_i = -\infty$. This is why we consider it adequate for V_o to be at 99% of its cutoff value.

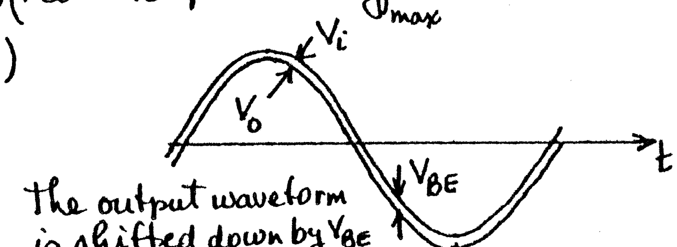
Note that the error is negligible even when it assumes its greatest magnitude at the extreme ends of the linear curve.

<u>Remarks</u> 1) If $V_i = V_m \sin \omega t$, it takes a slightly smaller V_m to sat Q1 than to sat Q or stated differently the upper limit on V_m is set by the saturation of the current source Q1.

2) To get $V_{o\,max} = V_{CC} - V_{CEsat}$ (to sat Q.), V_i needs to swing to $V_{CC} - V_{CEsat} + V_{BE}$ which is larger than V_{CC}. This will be impossible to achieve if the driver stage producing V_i is itself supplied by the same V_{CC}.

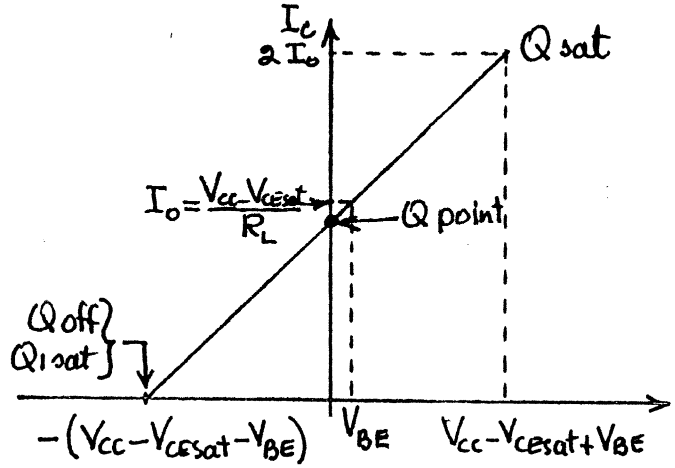
3) $(\text{Peak-to-peak swing})_{max} = 2(V_{CC} - V_{CEsat}) \cong \boxed{2V_{CC}}$.

4)



b) The I_c vs. V_i curve

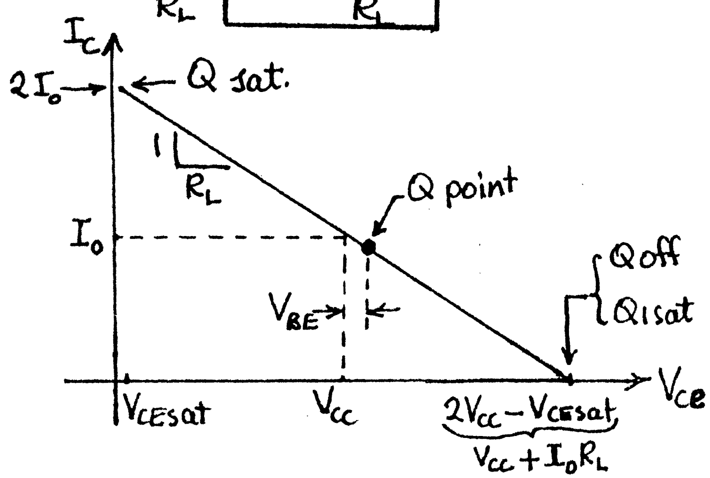
$$I_c = I_o + \frac{V_o}{R_L} \cong \boxed{I_o + \frac{V_i - V_{BE}}{R_L}}$$



$$(\text{Peak-to-peak swing of } I_c)_{max} = \boxed{2I_o}$$

c) The I_c vs V_{CE} curve – the load line

$$I_c = I_o + \frac{V_o}{R_L} = \boxed{I_o + \frac{V_{cc}-V_{CE}}{R_L}}$$



If we assume $\left\{\begin{matrix} V_{BE} \cong 0 \\ V_{CEsat} \cong 0 \end{matrix}\right\}$ a maximum peak-to-peak sinusoidal $\left\{\begin{matrix} \text{current swing of } 2I_o \\ \text{voltage swing of } 2V_{cc} \end{matrix}\right\}$ can be obtained about the Q-point.

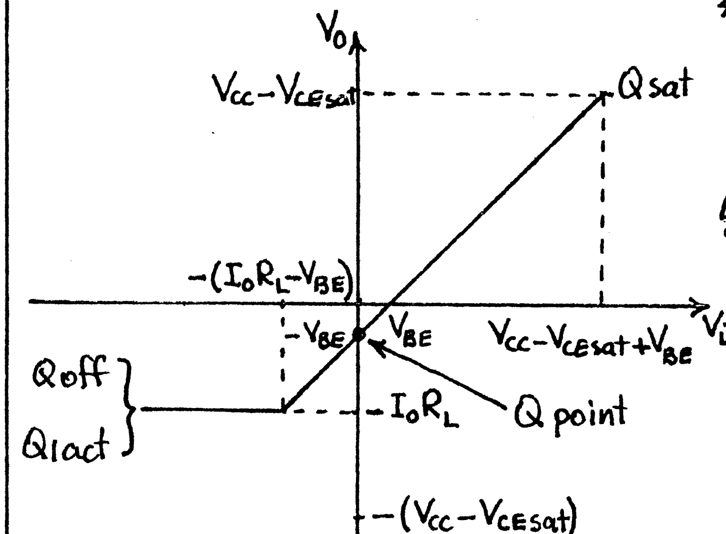
(2) Q gets cutoff for some negative value of V_i while Q1 remains active. This requires that

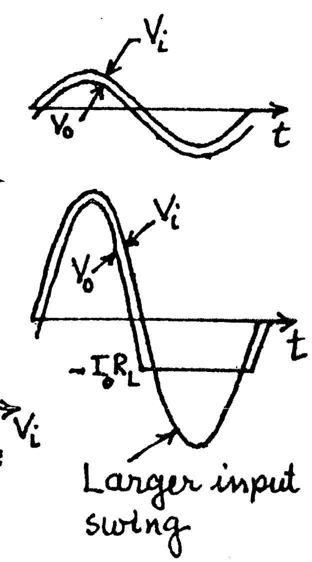
$$\boxed{I_oR_L < V_{cc} - V_{CEsat}}$$

occurs when I_o or R_L or both are small

a) The V_o vs. V_i curve

$$\boxed{V_o \cong V_i - V_{BE}}$$

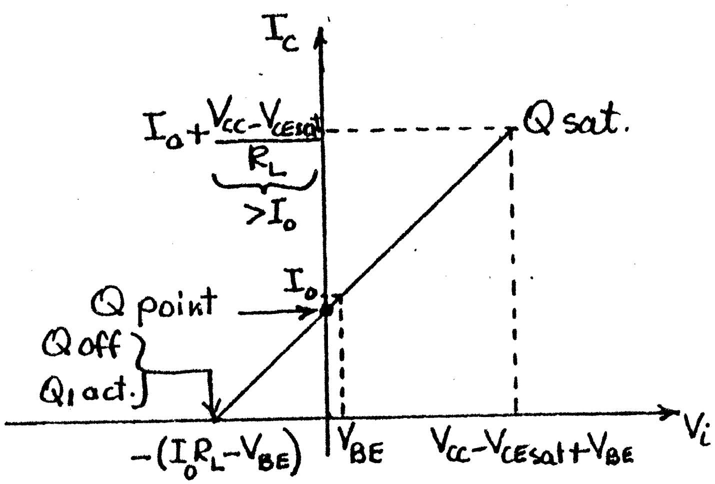




When V_i is positive, the load current is supplied by Q.

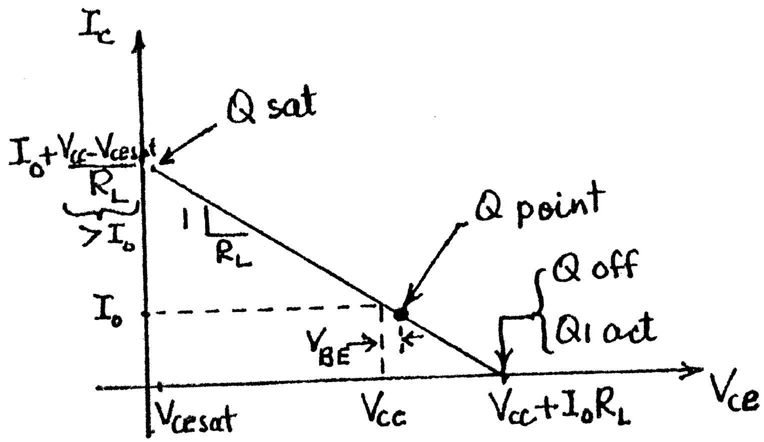
b) The I_c vs. V_i curve

$$\boxed{I_c = I_o + \frac{V_i - V_{BE}}{R_L}}$$



c) The I_c vs. V_{CE} curve – the load line

$$\boxed{I_c = I_o + \frac{V_{CC} - V_{CE}}{R_L}}$$



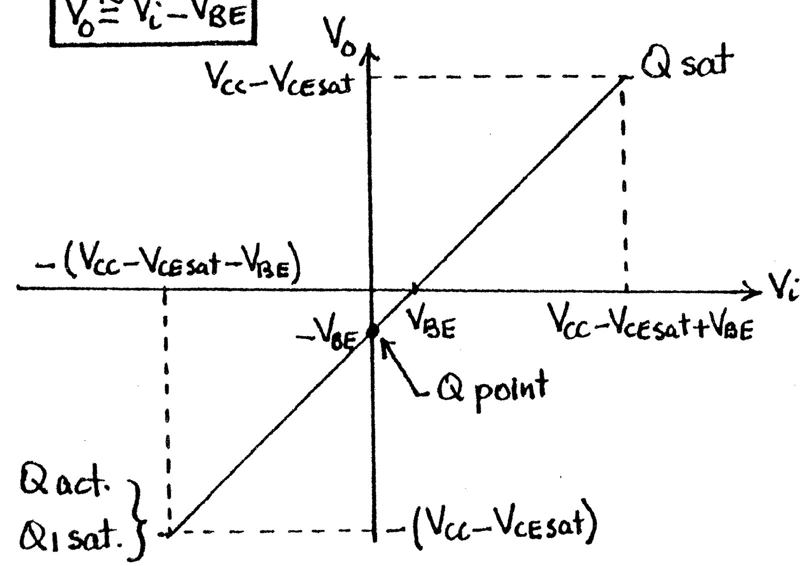
If we assume $\left\{\begin{matrix} V_{BE} \cong 0 \\ V_{CEsat} \cong 0 \end{matrix}\right\}$, maximum peak-to-peak sinusoidal $\left\{\begin{matrix} \text{current swing of } 2I_o \\ \text{voltage swing of } 2I_oR_L \end{matrix}\right\}$ can be obtained about the Q point. Note that the voltage swing is less than $2V_{CC}$ because $I_oR_L < V_{CC}$.

(3) Q1 gets saturated for some negative value of V_i while Q remains active. This requires that

$$\boxed{I_oR_L > V_{CC} - V_{CEsat}}$$

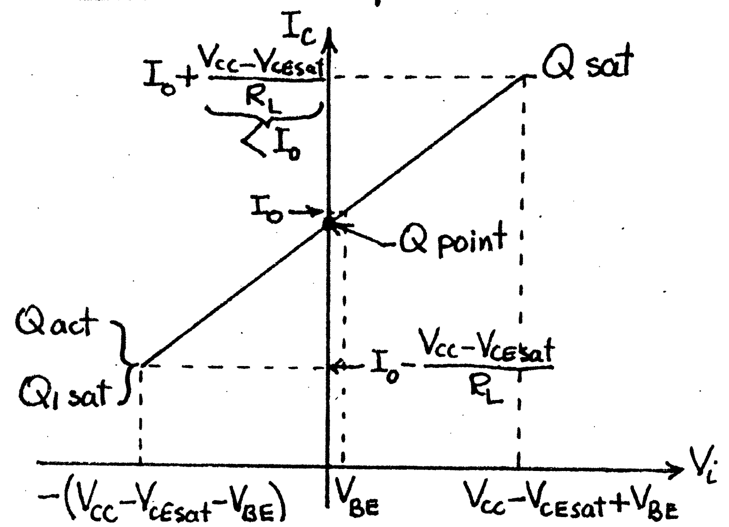
a) The V_o vs. V_i curve

$$\boxed{V_o \cong V_i - V_{BE}}$$



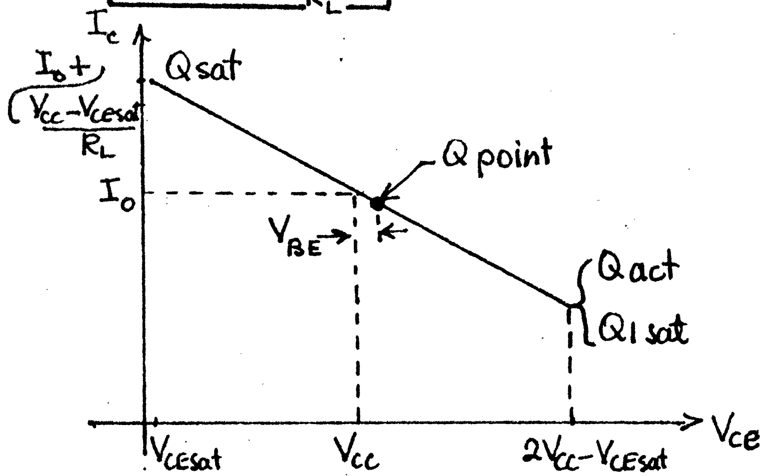
b) The I_c vs. V_i curve

$$\boxed{I_C = I_o + \frac{V_i - V_{BE}}{R_L}}$$



c) The I_c vs. V_{CE} curve – the load line

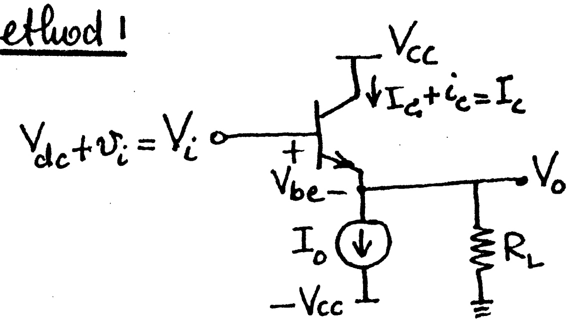
$$\boxed{I_c = I_o + \frac{V_{CC} - V_{CE}}{R_L}}$$



If we assume $\begin{Bmatrix} V_{BE} \cong 0 \\ V_{CEsat} \cong 0 \end{Bmatrix}$, a maximum peak-to-peak sinusoidal $\begin{Bmatrix} \text{current swing of } \frac{2V_{CC}}{R_L} \\ \text{voltage swing of } 2V_{CC} \end{Bmatrix}$ can be obtained about the Q-point. Note that the current swing is less than $2I_o$ because $I_o > \frac{V_{CC}}{R_L}$.

Small-signal gain calculation

Method 1



dc level of V_i adjusted to secure the operating point I_q

$$V_o = V_i - V_{be} = V_i - V_T \ln \frac{I_C}{I_S} \cong V_i - V_T \ln \frac{I_e}{I_S}$$

$$= V_i - V_T \ln\left(\frac{I_o + V_o/R_L}{I_S}\right) \leftarrow \text{equation for transfer characteristic}$$

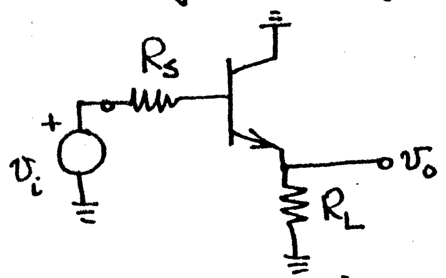
$$A_v = \frac{dV_o}{dV_i} = 1 - V_T \left.\frac{\frac{dV_o}{dV_i}/I_S R_L}{(I_o + V_o/R_L)/I_S}\right|_{I_c = I_q} = 1 - \frac{V_T}{I_q R_L}\frac{dV_o}{dV_i}$$

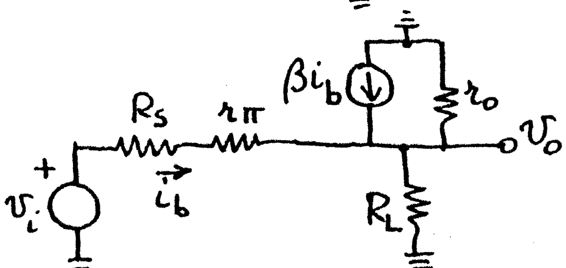
Solving for $\frac{dV_o}{dV_i}$ we obtain

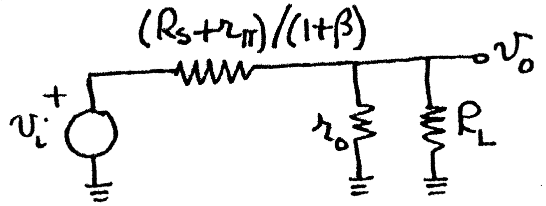
$$\frac{dV_o}{dV_i} = \frac{1}{1 + V_T/I_q R_L} = \frac{1}{1 + 1/g_m R_L} = \boxed{\frac{g_m R_L}{1 + g_m R_L}}$$

Method 2

Small-signal analysis circuit is







$$A_v = \frac{v_o}{v_i} = \frac{r_o \| R_L}{r_o \| R_L + (R_S + r_\pi)/(1+\beta)} \Bigg|_{r_o \gg R_L} \cong \frac{R_L}{R_L + \frac{R_S + r_\pi}{1+\beta}}$$

which for $\underline{R_S = 0}$ and $1+\beta \cong \beta$ reduces to

$$A_v = \frac{R_L}{R_L + \frac{r_\pi}{\beta}} = \frac{R_L}{R_L + \frac{1}{g_m}} = \boxed{\frac{g_m R_L}{1 + g_m R_L}}$$

Resistance facing $R_L \cong \frac{1}{g_m} = \boxed{\frac{V_T}{I_C}}$ ← varies with op. point but is small throughout

The gain depends on g_m which depends on the operating point I_C. Let us now calculate the gain at three different operating points for the case when $I_o R_L = V_{CC} - V_{CEsat} \cong V_{CC} = 15\ V$.

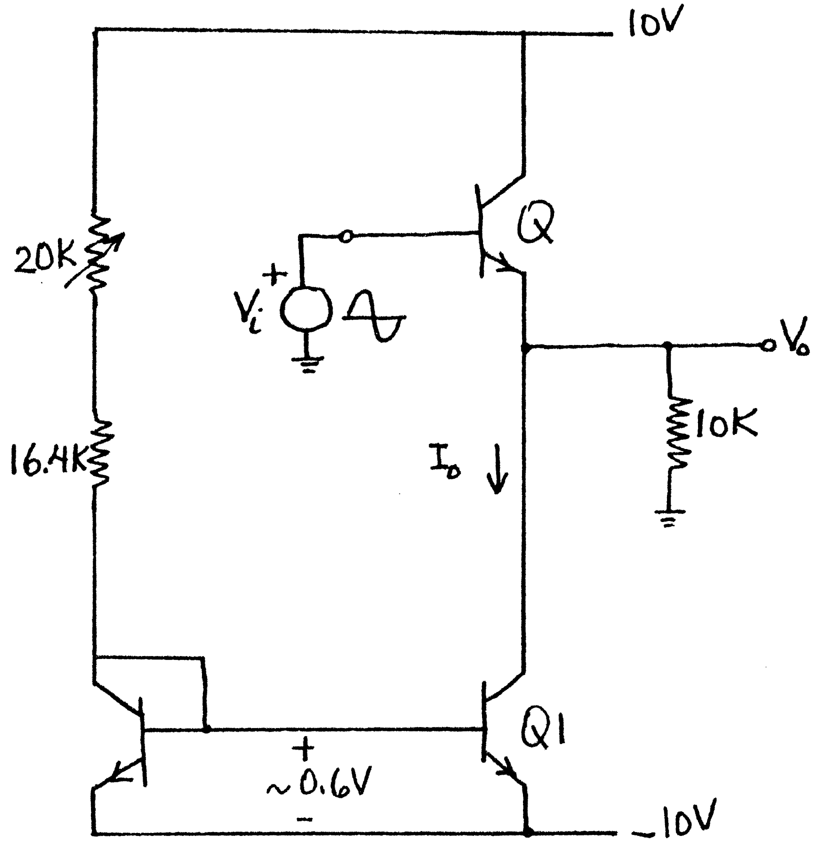
$$A_v = \frac{1}{1 + \frac{V_T}{I_C R_L}} = \frac{1}{1 + \frac{I_o}{I_C}\frac{V_T}{V_{CC}}} \qquad I_C = I_o + \frac{V_{CC} - V_{CE}}{R_L} \cong 2I_o - \frac{V_{CE}}{R_L}$$

$A_v =$

- $v_i \cong V_{CC}\ (I_C = 2I_o) \rightarrow = \dfrac{1}{1 + \frac{1}{2}\frac{V_T}{V_{CC}}} = \underline{0.999}$
- $v_i \cong 0\ (I_C = I_o) \rightarrow = \dfrac{1}{1 + \frac{V_T}{V_{CC}}} = \underline{0.998}$
- $v_i \cong -V_{CC}\ (I_C = 0.1 I_o) \rightarrow = \dfrac{1}{1 + 10\frac{V_T}{V_{CC}}} = \underline{0.983}$
- $v_i \cong -V_{CC}\ (I_C = 0.01 I_o) \rightarrow = \dfrac{1}{1 + 100\frac{V_T}{V_{CC}}} = \underline{0.853}$

As long as operation near cutoff is excluded, the small-signal gain varies about 1% throughout the entire dynamic range of the amplifier. Hence, even for large signals covering the entire dynamic range, distortion will be small.

Class-A output stage demonstration



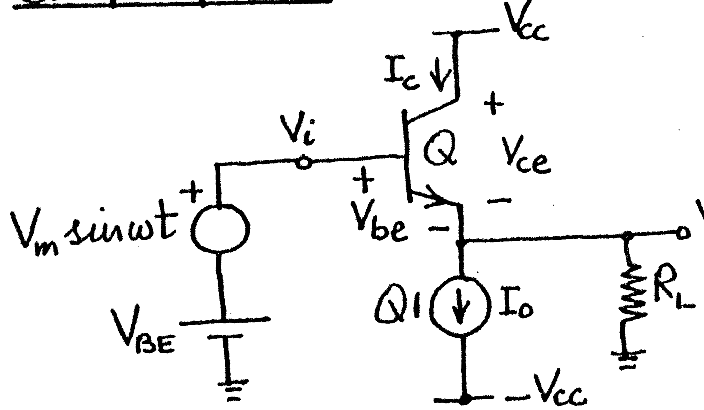
$$I_{o\,max} \cong \frac{20-0.6}{16.4} = 1.18\,mA$$

$$I_{o\,min} \cong \frac{20-0.6}{36.4} = 0.53\,mA$$

Show

1. Linearity
2. Dynamic range
3. Unity gain
4. Output offset
5. Effect of I_o
6. Neg. output limit being reached before positive limit
7. Input and output waveforms

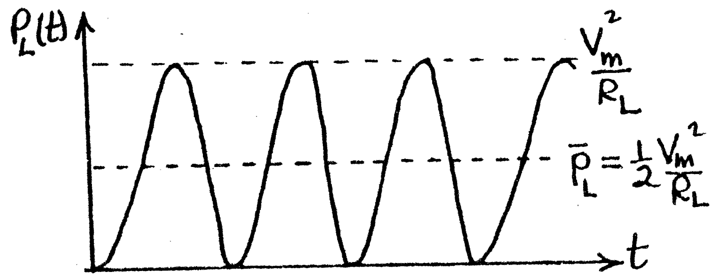
Output power



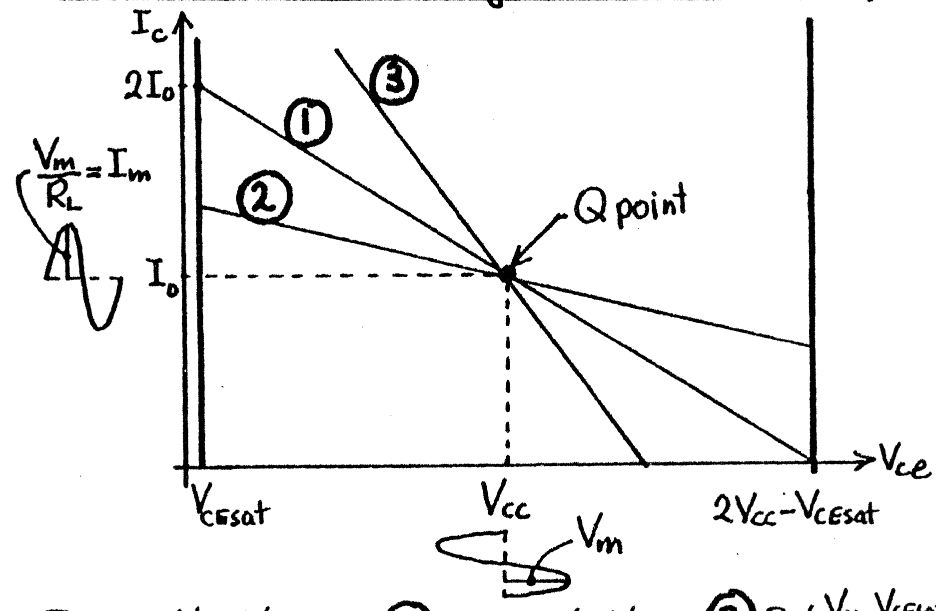
As V_i varies, V_{be} will change slightly. Neglect this variation and assume $V_{be} = V_{BE}$.

$$\left\{ \begin{array}{l} V_o = V_m \sin\omega t \\ I_c \cong I_o + \dfrac{V_o}{R_L} = I_o + \dfrac{V_m}{R_L} \sin\omega t \\ V_{ce} = V_{cc} - V_o = V_{cc} - V_m \sin\omega t \end{array} \right\}$$

$$P_L(t) = \frac{V_o^2}{R_L} = \frac{V_m^2}{R_L} \sin^2\omega t \qquad \bar{P}_L = \text{average power}$$



How much can voltage and current swing?



① $R_L = \dfrac{V_{cc} - V_{CEsat}}{I_o}$ ② $R_L > \dfrac{V_{cc} - V_{CEsat}}{I_o}$ ③ $R_L < \dfrac{V_{cc} - V_{CEsat}}{I_o}$

$$\bar{P}_L = \frac{1}{2}\frac{V_m^2}{R_L} = \frac{1}{2} V_m \left(\frac{V_m}{R_L}\right) = \boxed{\frac{1}{2} V_m I_m}$$

The larger V_m, the larger the average power delivered to the load. For load lines ① and ② $(V_m)_{max} = V_{cc} - V_{CEsat}$. Further increase in $\bar{P}_L$ can be obtained by making I_m as large as possible. $(I_m)_{max} = I_o$ for load line ①. So for <u>maximum possible power delivery to the load, operation must be along load line ①</u> with $V_m = V_{cc} - V_{CEsat}$ and $I_m = I_o$. The resulting power is $\boxed{(\bar{P}_L)_{max} = \frac{1}{2}(V_{cc} - V_{CEsat}) I_o}$

For $R_L > \frac{V_{CC}-V_{CEsat}}{I_o}$ (load line ②)

$$(I_m)_{max} < I_o$$

For $R_L < \frac{V_{CC}-V_{CEsat}}{I_o}$ (load line ③)

$$(V_m)_{max} < V_{CC} - V_{CEsat}$$

Thus, the maximum swing is limited either for current or for voltage resulting in $(\bar{P}_L)_{max} < \frac{1}{2}(V_{CC}-V_{CEsat})I_o$ for these two cases.

Power conversion efficiency

$$\eta = 100 \frac{\text{Average power delivered to load}}{\text{Average power supplied to circuit}} \%$$

$$= 100 \frac{\bar{P}_L}{\bar{P}_s}$$

$$P_L(t) = \frac{V_m^2}{R_L} \sin^2 \omega t \qquad \bar{P}_L = \frac{1}{2}\frac{V_m^2}{R_L}$$

$$P_s(t) = P_{V_{CC}}(t) + P_{-V_{CC}}(t) + \underbrace{\text{power supplied by } V_i}_{\text{negligible}}$$

where $\begin{cases} P_{V_{CC}}(t) = \text{power delivered by the } V_{CC} \text{ source.} \\ P_{-V_{CC}}(t) = \text{power delivered by the } -V_{CC} \text{ source.} \end{cases}$

$$P_{V_{CC}}(t) = V_{CC} I_c \cong V_{CC}\left(I_o + \frac{V_o}{R_L}\right) = V_{CC}\left(I_o + \frac{V_m}{R_L}\sin\omega t\right)$$

$$\bar{P}_{V_{CC}} = V_{CC} I_o$$

$$P_{-V_{CC}}(t) = (-V_{CC})(-I_o) = V_{CC} I_o$$

$$\bar{P}_{-V_{CC}} = V_{CC} I_o$$

$$\eta = 100 \frac{\bar{P}_L}{\bar{P}_{V_{CC}} + \bar{P}_{-V_{CC}}} = 100 \frac{\frac{1}{2}V_m^2/R_L}{V_{CC}I_o + V_{CC}I_o} = \boxed{25 \frac{V_m^2}{V_{CC} I_o R_L} \%}$$

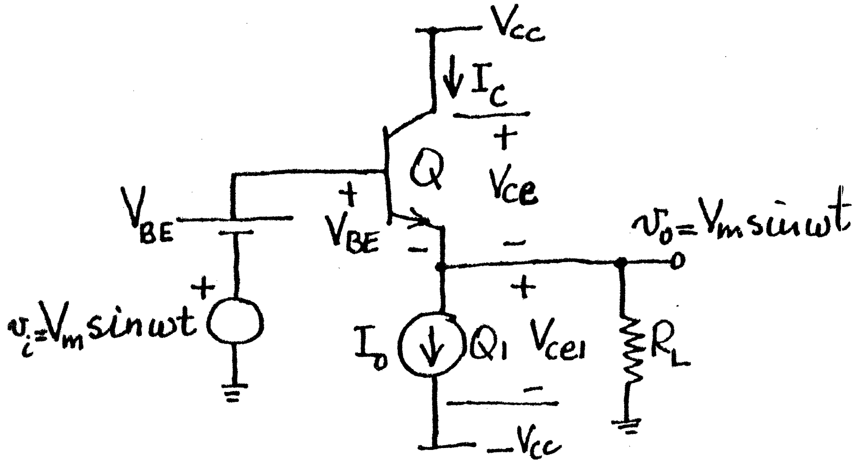
The maximum possible value of V_m is $(V_{CC}-V_{CEsat})$ provided that $R_L \geq \frac{V_{CC}-V_{CEsat}}{I_o}$.

The maximum power conversion efficiency occurs when V_m is at its maximum possible value while R_L assumes its lowest value which is $(V_{CC}-V_{CEsat})/I_o$. Hence,

$$\eta_{max} = 25 \frac{(V_{CC}-V_{CEsat})^2}{V_{CC} I_o (V_{CC}-V_{CEsat})/I_o} = 25\left(1 - \frac{V_{CEsat}}{V_{CC}}\right) \cong \boxed{25\%}$$

Stated differently, at least 75% of the power supplied to the circuit is wasted as heat in Q and Q1.

L17: Power dissipation in Q and Q1



$$\begin{cases} I_c = I_o + \dfrac{V_m}{R_L}\sin\omega t \\ V_{ce} = V_{cc} - V_m \sin\omega t \\ V_{ce1} = V_{cc} + V_m \sin\omega t \end{cases}$$

$$P_{Q1} = I_o V_{ce1} = I_o\left(V_{cc} + V_m \sin\omega t\right)$$

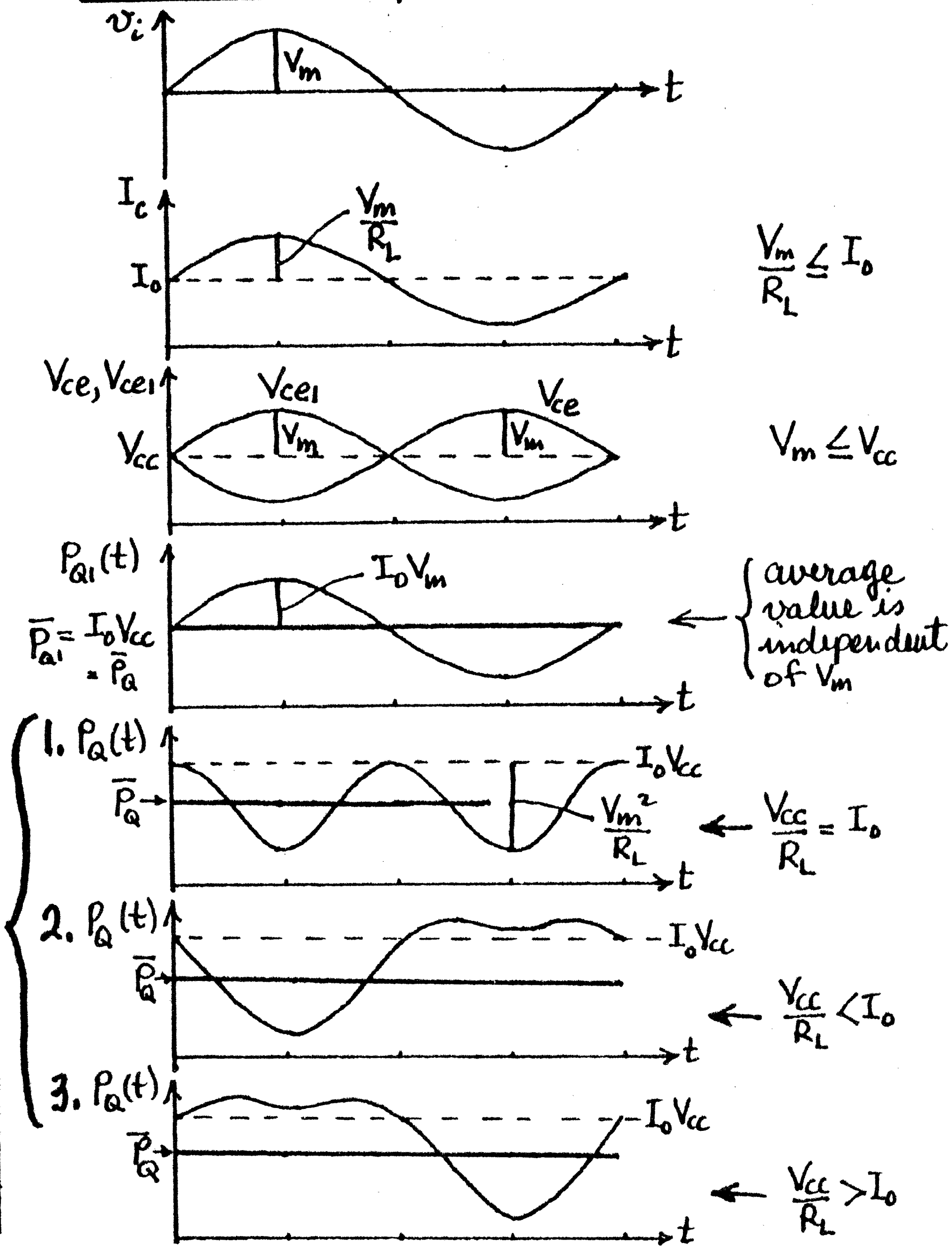
$$P_Q = I_c V_{ce} = \left(I_o + \frac{V_m}{R_L}\sin\omega t\right)\left(V_{cc} - V_m \sin\omega t\right)$$

$$= I_o V_{cc} - \frac{V_m^2}{R_L}\sin^2\omega t + V_m \underbrace{\left(\frac{V_{cc}}{R_L} - I_o\right)}_{+,\,0,\,-}\sin\omega t$$

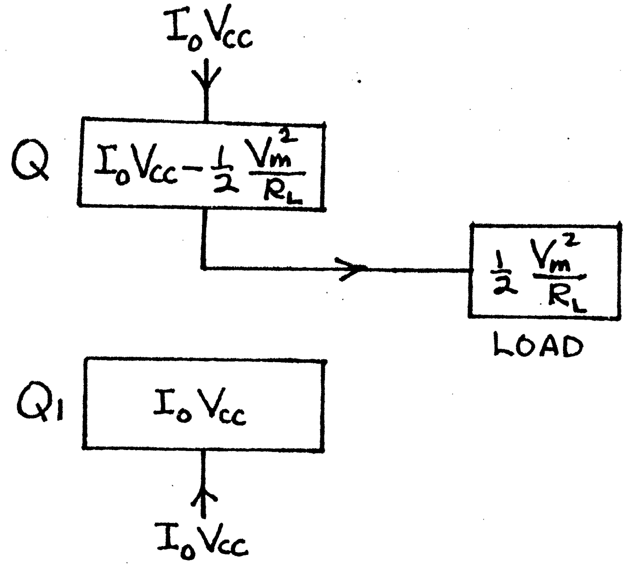
$\left\{\overline{P}_{Q1} = I_o V_{cc}\right\}$ independent of signal

$\left\{\overline{P}_Q = I_o V_{cc} - \frac{1}{2}\frac{V_m^2}{R_L}\right\}$ <u>the larger the signal, the less is the power dissipated in Q.</u>

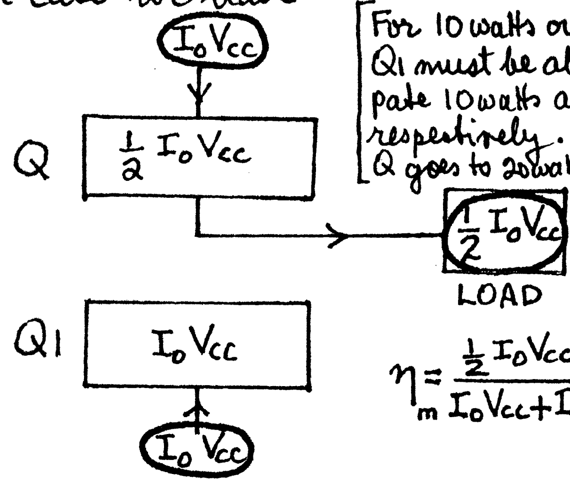
Instantaneous power waveforms



Average power-flow diagram



Q dissipates the least power when V_m is largest while R_L is the smallest. This occurs when $I_oR_L = V_{cc}$ and $V_m = V_{cc}$ in which case we have



[For 10 watts output, Q and Q1 must be able to dissipate 10 watts and 20 watts respectively. Dissipation in Q goes to 20 watts when $v_i = 0$.]

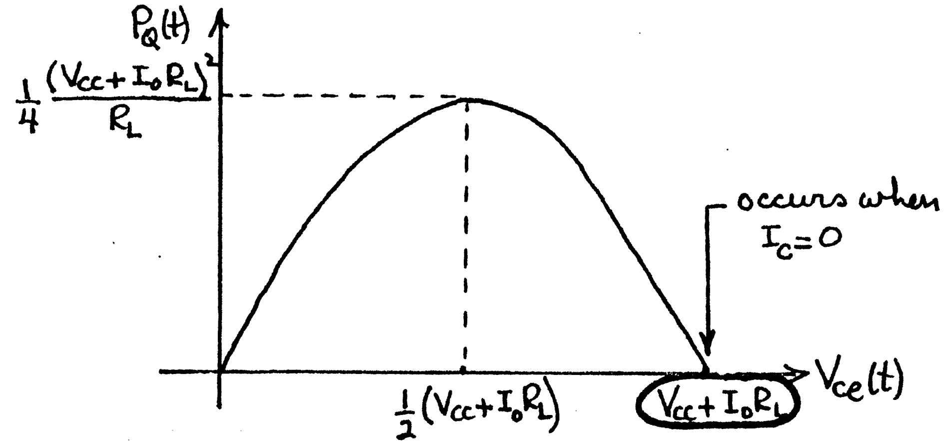
$$\eta_m = \frac{\frac{1}{2} I_oV_{cc}}{I_oV_{cc} + I_oV_{cc}} \times 100 = \boxed{25\%}$$

At what point does Q dissipate the most power?

The instantaneous power dissipated in Q for any signal waveform is

$$P_Q(t) = I_cV_{ce} = \left(I_o + \frac{V_{cc} - V_{ce}}{R_L}\right)V_{ce}$$

The $P_Q(t)$ vs. V_{ce} curve is a parabola with V_{ce} axis intercepts at $V_{ce} = 0$ and $V_{ce} = V_{cc} + I_oR_L$ as shown below.

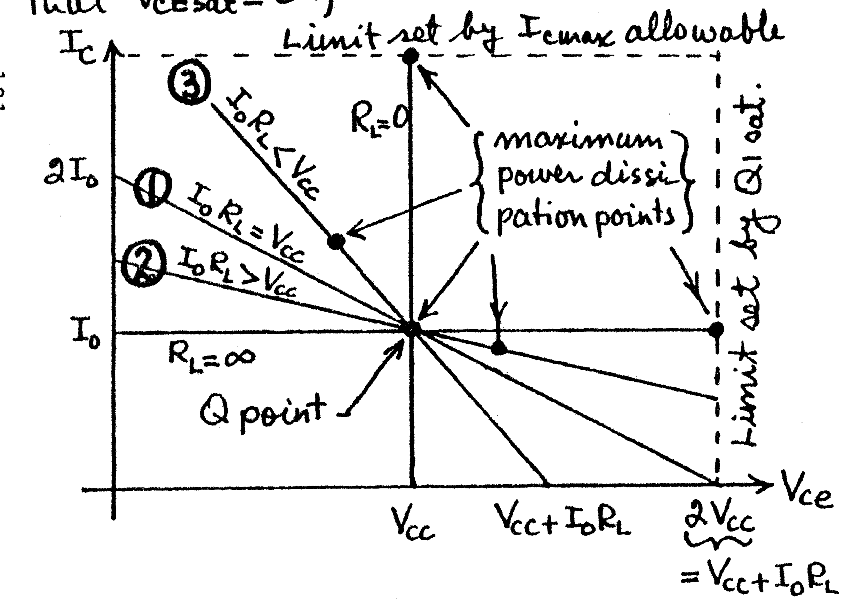


Maximum instantaneous power is dissipated in Q every time $V_{ce}(t)$ assumes the value of $\frac{1}{2}(V_{cc} + I_oR_L)$ which results in

$$\boxed{P_Q(t)\Big|_{max} = \frac{1}{4}\frac{(V_{cc} + I_oR_L)^2}{R_L}}$$

Designating the maximum power dissipation points on the load line:

When $v_i(t)=0$, $v_o(t)=0$. At these times $I_c(t)=I_o$ and $V_{ce}(t)=V_{cc}$. These values do not depend on R_L. As before, we consider 3 cases: 1. $I_oR_L=V_{cc}$, 2. $I_oR_L>V_{cc}$, and 3. $I_oR_L<V_{cc}$. (These results are based on the assumption that $V_{ce\,sat}\cong 0$.)

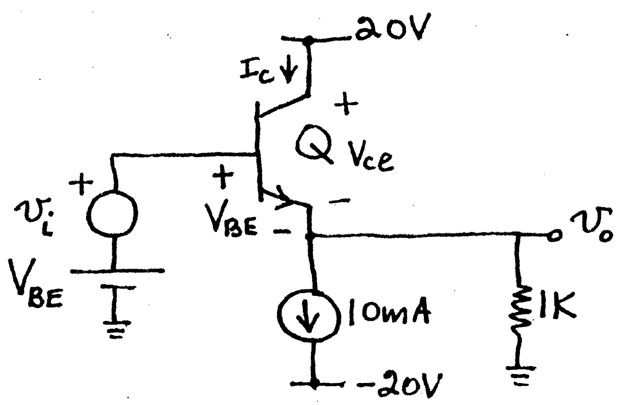


The point of maximum power dissipation occurs when $v_i(t)$ drives the transistor to the midpoint on its load line provided the midpoint is within the boundaries set by $V_{ce\,max}=2V_{cc}$ and $I_c=I_{cmax}$ which represents the maximum permissible collector current. For $\infty \geq R_L \geq \frac{V_{cc}}{I_o}$, $p(t)_{max}$ occurs for $2V_{cc}\geq V_{ce}\geq V_{cc}$ and $I_o \geq I_c \geq 0$. For $\frac{V_{cc}}{I_o}\geq R_L \geq 0$, $p(t)_{max}$ occurs for $V_{cc}\geq V_{ce}\geq 0$ and $I_o \leq I_c \leq I_{cmax}$.

It should also be clear that for

1. $R_L=\frac{V_{cc}}{I_o}$, the maximum inst. power dissipation occurs at the quiescent point, i.e., when $v_i(t)=0$.
2. $R_L>\frac{V_{cc}}{I_o}$, the max. inst. power dissipation occurs for $v_i(t)<0$.
3. $R_L<\frac{V_{cc}}{I_o}$, the max. inst. power dissipation occurs for $v_i(t)>0$.
4. Regardless of the value of R_L, power dissipation in Q falls of on either side of the max. inst. power dissipation point. Moreover, the reduction is symmetric about the midpoint of the load line as the parabola shown on the previous page clearly demostrates.

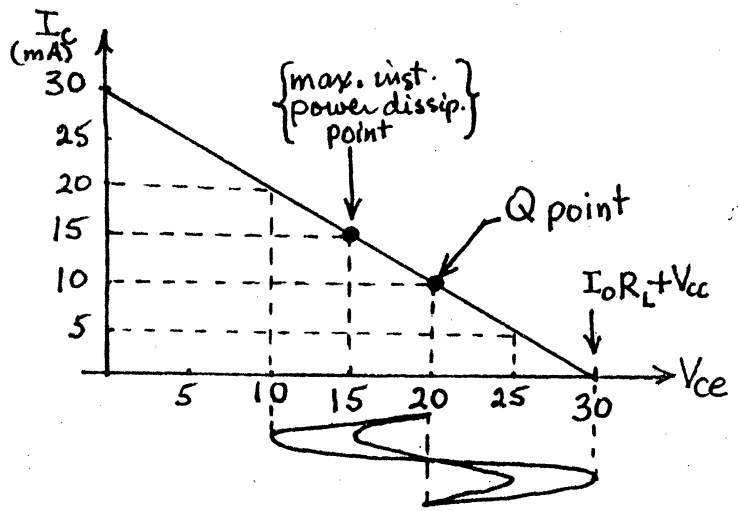
Example:

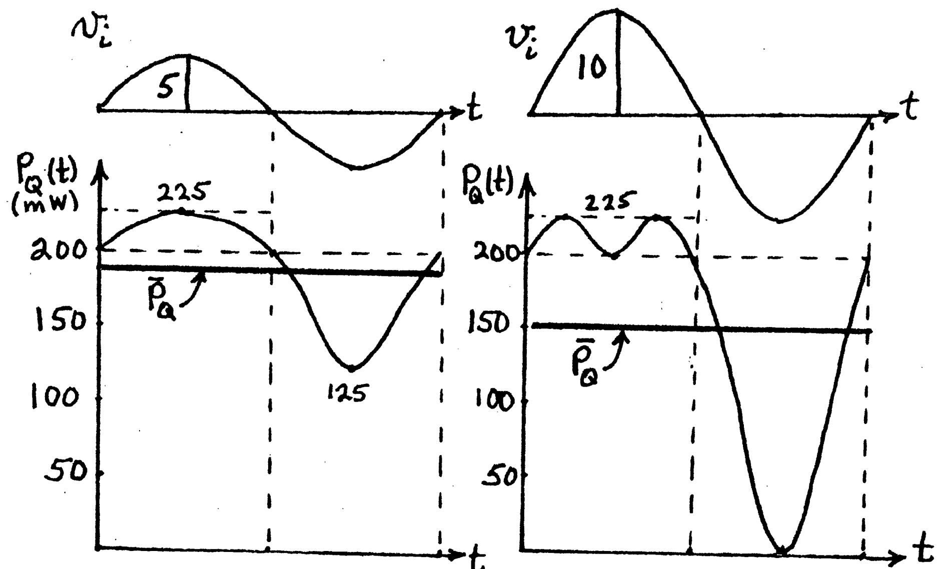


$v_i = V_m \sin \omega t$

Sketch the instantaneous power dissipation in Q as a function of time for $V_m = 5V$ and $V_m = 10V$.

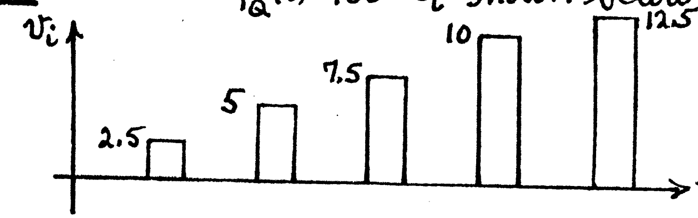
Solution: Draw the load line.



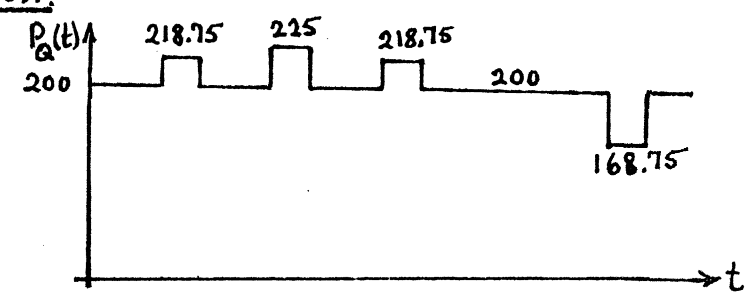


$\bar{P}_Q = I_o V_{cc} - \frac{1}{2}\frac{V_m^2}{R_L} = 187.5$ $\qquad$ $\bar{P}_Q = 150$

Example: Obtain $P_Q(t)$ for v_i shown below



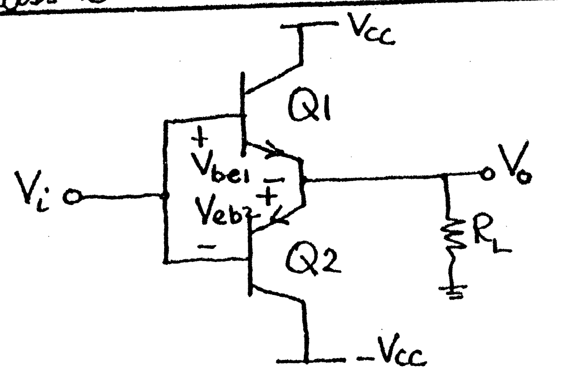
Solution:



In a class-A amplifier, the transistors conduct all the time. As a result
1. 25% efficiency is achieved at best
2. Power is wasted at standby
3. The transistors must operate at higher temperatures than necessary to deliver a prescribed power to the load.

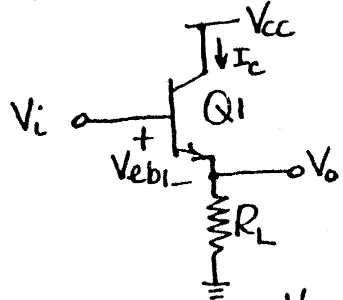
In a class-B amplifier, the transistors conduct half the time. As a result
1. Efficiencies as high 78.6% can be achieved
2. No power is wasted at standby
3. The transistors operate at a lower temperatures thereby lowering failure rate.

Class-B emitter follower output stage

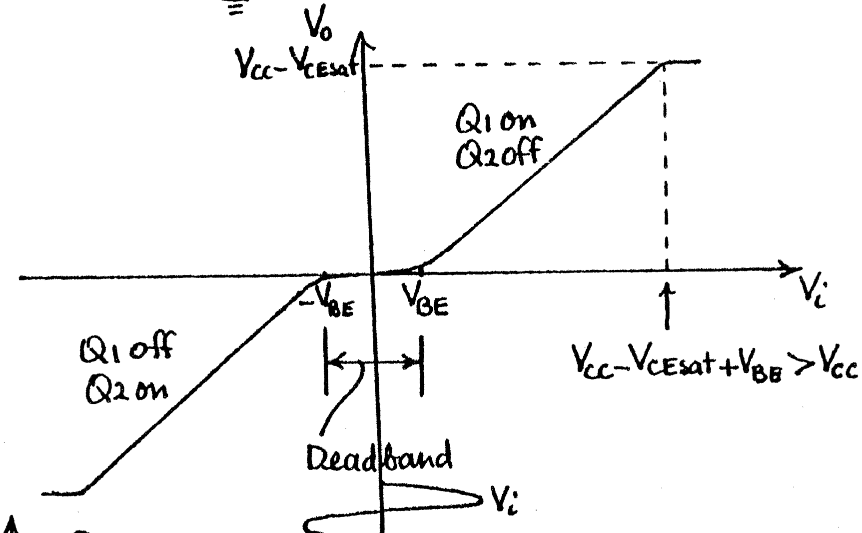


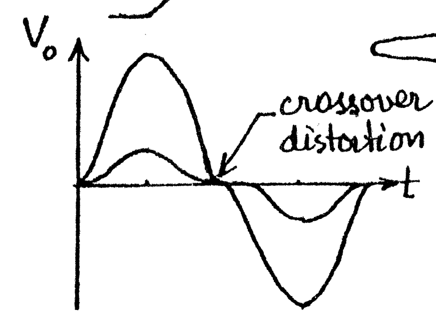
also known as push-pull amplifier; complementary NPN−PNP output stage

Since $V_{be1}+V_{eb2}=0$, when one voltage is positive, the other must be negative. Hence, only one of the transistors is on at a given time; the other one is off. Assume $V_i>0$, which assures that Q1 is on and Q_2 off.



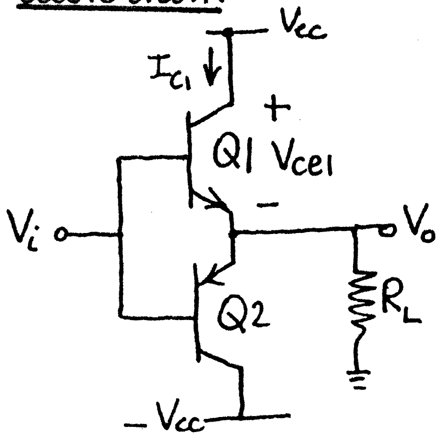
$$V_o = V_i - V_{eb1}$$
$$= V_i - V_T \ln \frac{I_C}{I_S}$$
$$\cong V_i - V_T \ln \frac{V_o}{I_S R_L} \qquad V_o>0$$

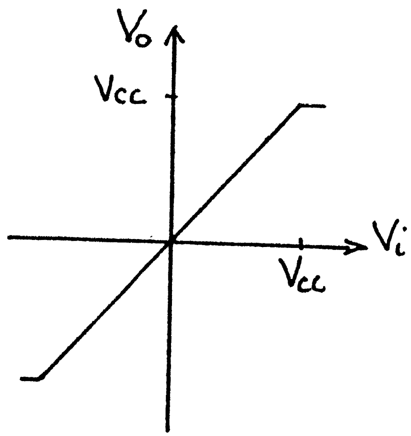




the smaller V_i, the more pronounced is the cross-over distortion. If $I_{SN} \neq I_{SP}$, the two halves of the waveform are not the same.

Power calculations neglecting crossover distortion.

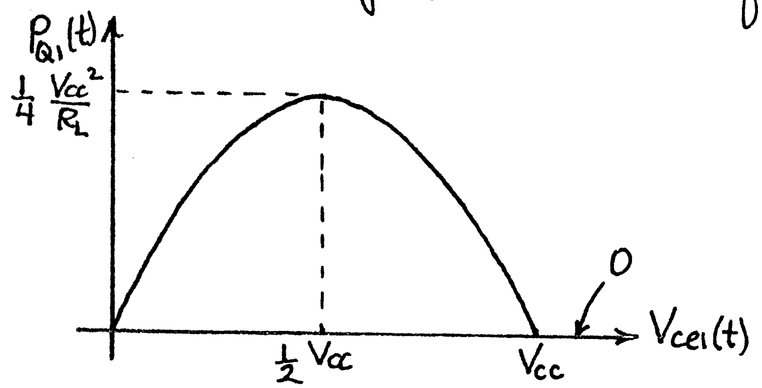




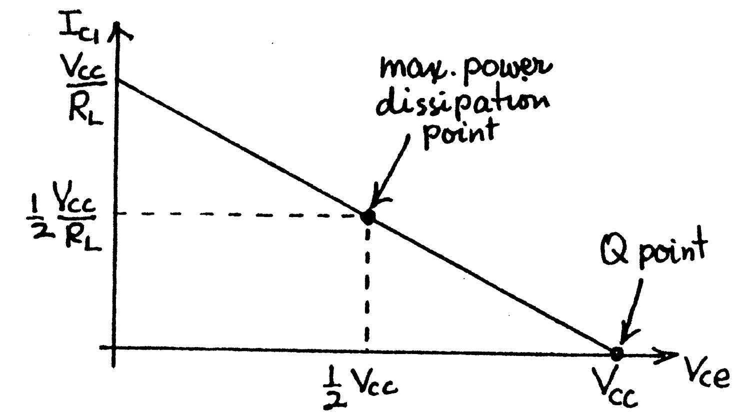
Regardless of V_i waveform

$$P_{Q1}(t) = I_{C1}V_{ce1} \cong \frac{V_o}{R_L}V_{ce1} = \left(\frac{V_{cc}-V_{ce1}}{R_L}\right)V_{ce1} \qquad V_o>0$$

where V_{ce1} is in general a function of t.



Maximum dissipation in Q1 (as well in Q_2) occurs when V_{ce}'s are $\frac{1}{2}V_{cc}$.



When $V_i=0$, $V_{ce1}=V_{cc}$, $I_{C1}=0$.

Maximum power dissipation point for Q1 is at the mid point of the load line regardless of the waveform of V_i.

For $V_i = V_m \sin\omega t$, $V_o = V_m \sin\omega t$, $V_{ce1} = V_{cc} - V_m \sin\omega t$

$$I_{C1} = \begin{cases} \frac{V_m}{R_L}\sin\omega t & V_i>0 \\ 0 & V_i<0 \end{cases}$$

$$P_{R_L}(t) = \frac{V_o^2}{R_L} = \frac{V_m^2}{R_L}\sin^2\omega t \qquad \overline{P_{R_L}(t)} = \frac{1}{2}\frac{V_m^2}{R_L}$$

$$P_{V_{cc}}(t) = V_{cc}I_{C1} = \begin{cases} V_{cc}\frac{V_m}{R_L}\sin\omega t & V_i>0 \\ 0 & V_i<0 \end{cases}$$

$$\overline{P_{V_{cc}}(t)} = \frac{1}{\pi}V_{cc}\frac{V_m}{R_L} = \overline{P_{-V_{cc}}(t)}$$

$$\eta = 100\frac{\overline{P_{R_L}}}{\overline{P_{V_{cc}}}+\overline{P_{-V_{cc}}}} = 100\frac{\frac{1}{2}\frac{V_m^2}{R_L}}{\frac{2}{\pi}V_{cc}\frac{V_m}{R_L}} = \boxed{25\pi\frac{V_m}{V_{cc}}\,\%}$$

$$\eta_{max} = \eta\Big|_{V_m=V_{cc}} = 25\pi = \boxed{78.6\%}$$

Average power-flow diagram

$$\overline{P}_{V_{cc}} = \overline{P}_{-V_{cc}} = \frac{1}{\pi} V_{cc} \frac{V_m}{R_L}$$

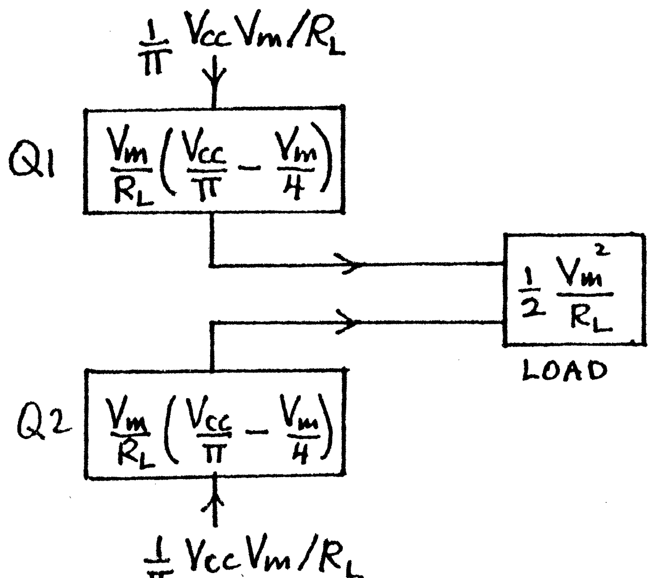
$$\overline{P}_{R_L} = \frac{1}{2} \frac{V_m^2}{R_L}$$

$$P_{Q1}(t) = I_{c1}(t) V_{ce1}(t) = \frac{V_o(t)}{R_L}\left[V_{cc} - V_o(t)\right] \quad V_o(t) > 0$$

$$= \frac{V_m}{R_L} \sin\omega t \left[V_{cc} - V_m \sin\omega t\right] \quad \text{for } \sin\omega t > 0$$

$$P_{Q1}(t) = 0 \quad \text{for } \sin\omega t < 0$$

$$\overline{P}_{Q1} = \frac{1}{\pi}\frac{V_m}{R_L} V_{cc} - \frac{1}{4}\frac{V_m^2}{R_L} = \frac{V_m}{R_L}\left(\frac{V_{cc}}{\pi} - \frac{V_m}{4}\right)$$



Power dissipated in Q1 and Q2 is zero when $V_m = 0$. As V_m is increased from zero, power dissipation increases and reaches a maximum value. Further increase in V_m decreases the average power dissipation. The maximum occurs when $V_m = \frac{2}{\pi} V_{cc}$ resulting in

$$\overline{P}_{Q1\,max} = \frac{2}{\pi}\frac{V_{cc}}{R_L}\left(\frac{V_{cc}}{\pi} - \frac{1}{4}\frac{2}{\pi}V_{cc}\right) = \boxed{\frac{V_{cc}^2}{\pi^2 R_L}}$$

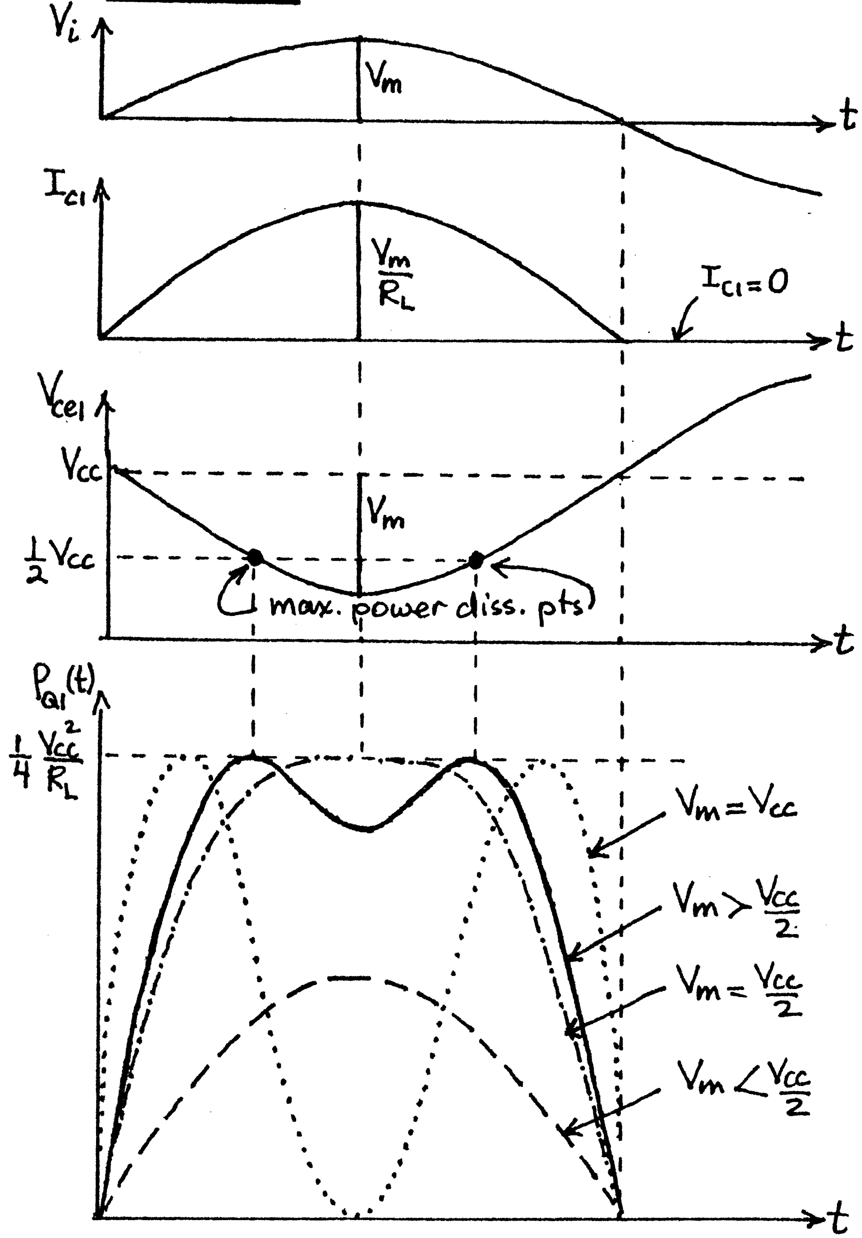
On the other hand, maximum power delivered to the load occurs for $V_m = V_{cc}$ resulting in

$$\boxed{\overline{P}_{L\,max} = \frac{1}{2}\frac{V_{cc}^2}{R_L}}$$

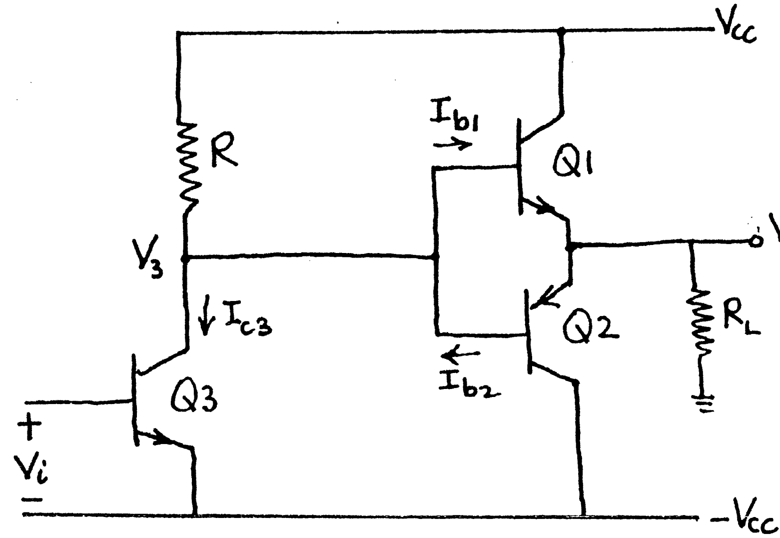
Hence $\boxed{\overline{P}_{Q1max} = \frac{2}{\pi^2}\overline{P}_{L\,max}}$

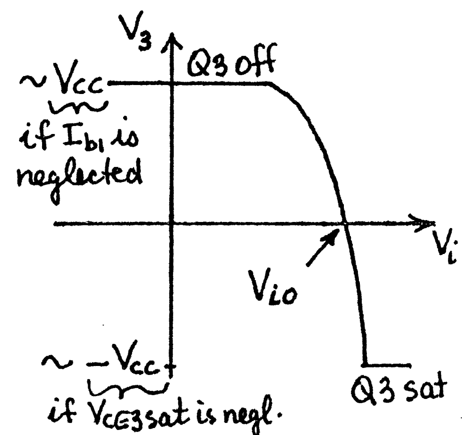
Thus, for a maximum average power output of 10W, Q1 and Q2 must be able to dissipate $\frac{2}{\pi^2} \times 10 \cong 2W$ of average power.

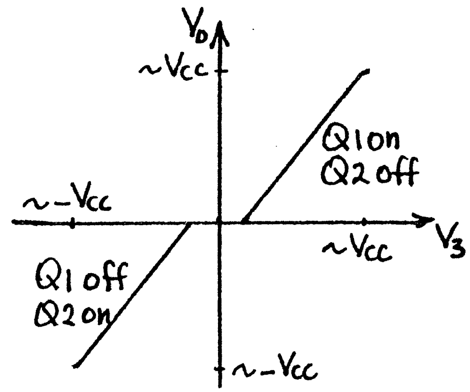
Waveforms



Class-B output stage and driver



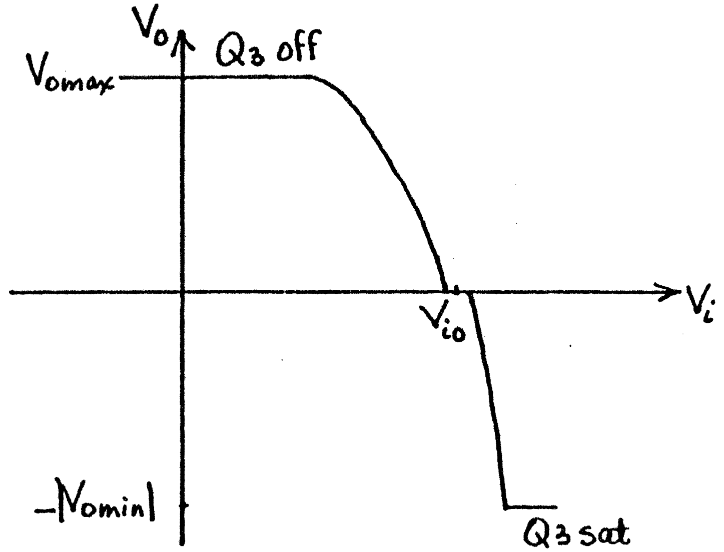




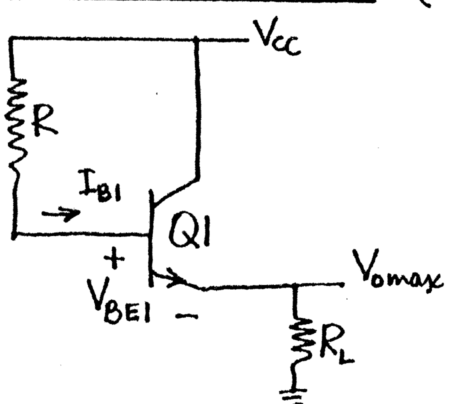
The output V_o is zero when $V_3 = 0$ which implies $I_{b1} = I_{b2} = 0$. Hence

$$V_3 = V_{cc} - I_{c3}R = 0 \qquad I_{c3} = \frac{V_{cc}}{R} = I_{S3}\, e^{\frac{V_{io}}{V_T}}$$

$$V_{io} = V_T \ln I_{c3}/I_{S3} \approx 600\,\mathrm{mV}$$



<u>To determine V_{omax}</u> (Q_3 off)

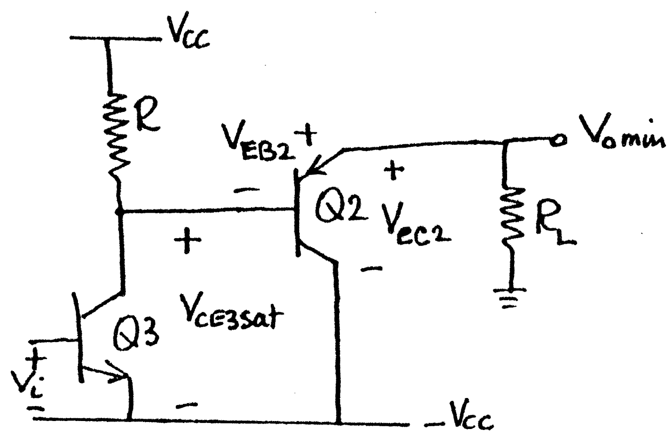


$$V_{omax} = (1+\beta_1) I_{B1} R_L = (1+\beta_1)\left[\frac{V_{CC}-V_{BE1}}{R+(1+\beta_1)R_L}\right] R_L$$

$$= \left.\frac{V_{CC}-V_{BE1}}{R_L + \frac{R}{1+\beta_1}} \times R_L \right|_{\substack{R=20K \\ \beta_1=100}} = \begin{cases} R_L = 10K: & = \underline{0.98\,(V_{CC}-V_{BE1})} \\ R_L = 1K: & = \underline{0.83\,(V_{CC}-V_{BE1})} \end{cases}$$

Note that it is impossible to sat. Q1. Even for R_L very large $V_{CE1} = V_{CC} - V_{omax} \cong V_{BE1}$.

<u>To determine V_{omin}</u> (Q_3 sat)



$$V_{omin} = -V_{CC} + V_{CE3sat} + V_{EB2}$$

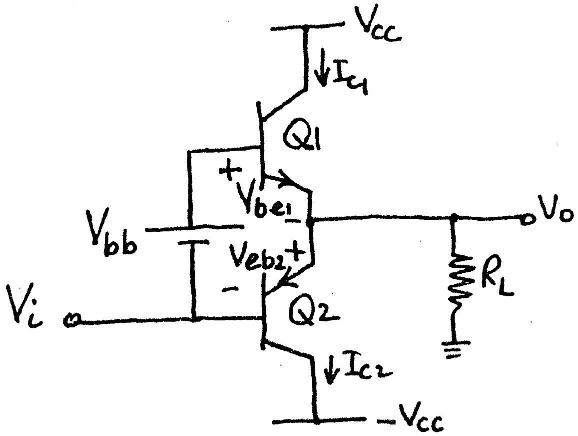
It is impossible to sat Q_2 either because

$$V_{EC2} = V_{omin} + V_{CC} = V_{CE3sat} + V_{EB2} > V_{CE2sat}$$

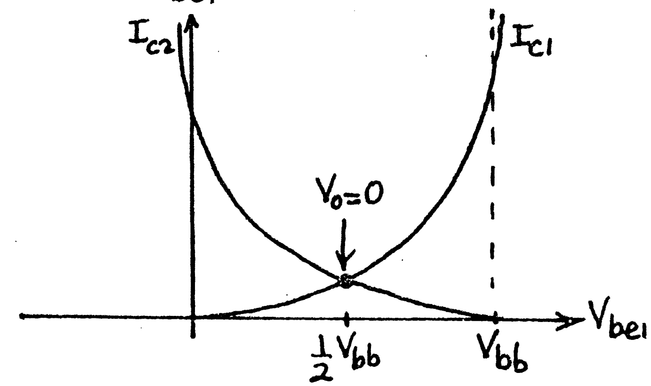
When $V_o > 0$ ($V_o < 0$), the base of Q1 (Q2) loads the collector of Q3. Since $\beta_{NPN} > \beta_{PNP}$, the loading is unequal. This plus the exponential dependence of the transfer characteristics of the driver stage result in an overall transfer characteristic that is quite nonlinear (in addition to the crossover distortion). This is particularly noticeable for low values of R_L. Feedback from the output stage to the driver stage linearizes the overall characteristic.

L18: Class-AB output stage

In the class-A amplifier, the transistors conduct all the time. In the class-B amplifier, the transistors conduct half the time. In the class-AB amplifier the transistors are biased such that they conduct more than half the time but not necessarily all the time. The circuit given below shows how this is achieved.



The input is applied between base of Q_2 and ground. The voltage V_{bb}, which is produced across diode-connected transistors driven by a current source (to be shown shortly), assures that both transistors are on when $|V_i|$ is small. In particular when $V_o=0$, $I_{c1}=I_{c2}$, and hence $V_{be1}=V_{eb2}$ (assuming complementary transistors so that $I_{SNPN}=I_{SPNP}=I_S$). Since the relationship $V_{bb}=V_{be1}+V_{eb2}$ is always valid, $V_{be1}=V_{eb2}=\frac{1}{2}V_{bb}$ and therefore $V_i=-\frac{V_{bb}}{2}$. Thus, a small negative voltage must be put in to drive the output to zero. For $V_i=0$, the output is slightly positive: $V_o=V_{eb2}$. As V_i is increased from 0, V_{be1} goes up while V_{eb2} goes down but their sum remains constant at V_{bb}. Since, $I_{c1}=I_S e^{\frac{V_{be1}}{V_T}}$ and $I_{c2}=I_S e^{\frac{V_{eb2}}{V_T}}=I_S e^{\frac{V_{bb}-V_{be1}}{V_T}}$, we can plot both I_{c1} and I_{c2} as a function of V_{be1} as shown below.



By controlling V_{bb}, the quiescent values of I_{c1} and I_{c2} (corresponding to $V_o=0$) can be controlled. The larger V_{bb}, the more the I_{c2} curve is shifted to the right and therefore the more the

the quiescent values of the collector currents, thus approaching class-A type of operation. On the other hand, if $V_{bb}=0$, class-B operation results.

Effect of V_{bb} on transfer characteristic

$$V_o \cong R_L(I_{c1}-I_{c2}) = R_L I_s\left(e^{\frac{V_{be1}}{V_T}} - e^{\frac{V_{eb2}}{V_T}}\right)$$
$$= R_L I_s\left(e^{\frac{V_{bb}-V_{eb2}}{V_T}} - e^{\frac{V_{eb2}}{V_T}}\right)$$

Since $V_o = V_{eb2}+V_i$, we can write

$$V_o = R_L I_s\left(e^{\frac{V_{bb}-V_o+V_i}{V_T}} - e^{\frac{V_o-V_i}{V_T}}\right)$$
$$= R_L I_s\, e^{\frac{1}{2}\frac{V_{bb}}{V_T}}\left(e^{\frac{V_i-V_o+\frac{1}{2}V_{bb}}{V_T}} - e^{-\frac{V_i-V_o+\frac{1}{2}V_{bb}}{V_T}}\right)$$

$$\boxed{V_o = 2R_L\, e^{\frac{1}{2}V_{bb}/V_T}\sinh\left(\frac{V_i-V_o+\frac{1}{2}V_{bb}}{V_T}\right)}$$

This equation cannot be solved explicitely for V_o. However, it can be solved explicitely for V_i.

$$\boxed{V_i = -\frac{1}{2}V_{bb} + V_o + V_T\sinh^{-1}\left(\frac{V_o\, e^{-\frac{V_{bb}}{2V_T}}}{2I_sR_L}\right)}$$

This equation results in a transfer characteristic (V_o vs V_i curve) that behaves like an odd function about $V_i = -\frac{1}{2}V_{bb}$.

The $V_T\sinh^{-1}\left(\frac{V_o e^{-\frac{1}{2}\frac{V_{bb}}{V_T}}}{2I_sR_L}\right)$ term is responsible for the crossover distortion. It has the most pronounced effect when $V_{bb}=0$, which of course results in class-B operation. As V_{bb} is increased from 0, this term becomes less and less significant because $e^{-\frac{1}{2}\frac{V_{bb}}{V_T}}$ becomes smaller. As a result, crossover distortion is reduced. For V_{bb} large enough, the distortion is practically eliminated. The transfer characteristic then becomes

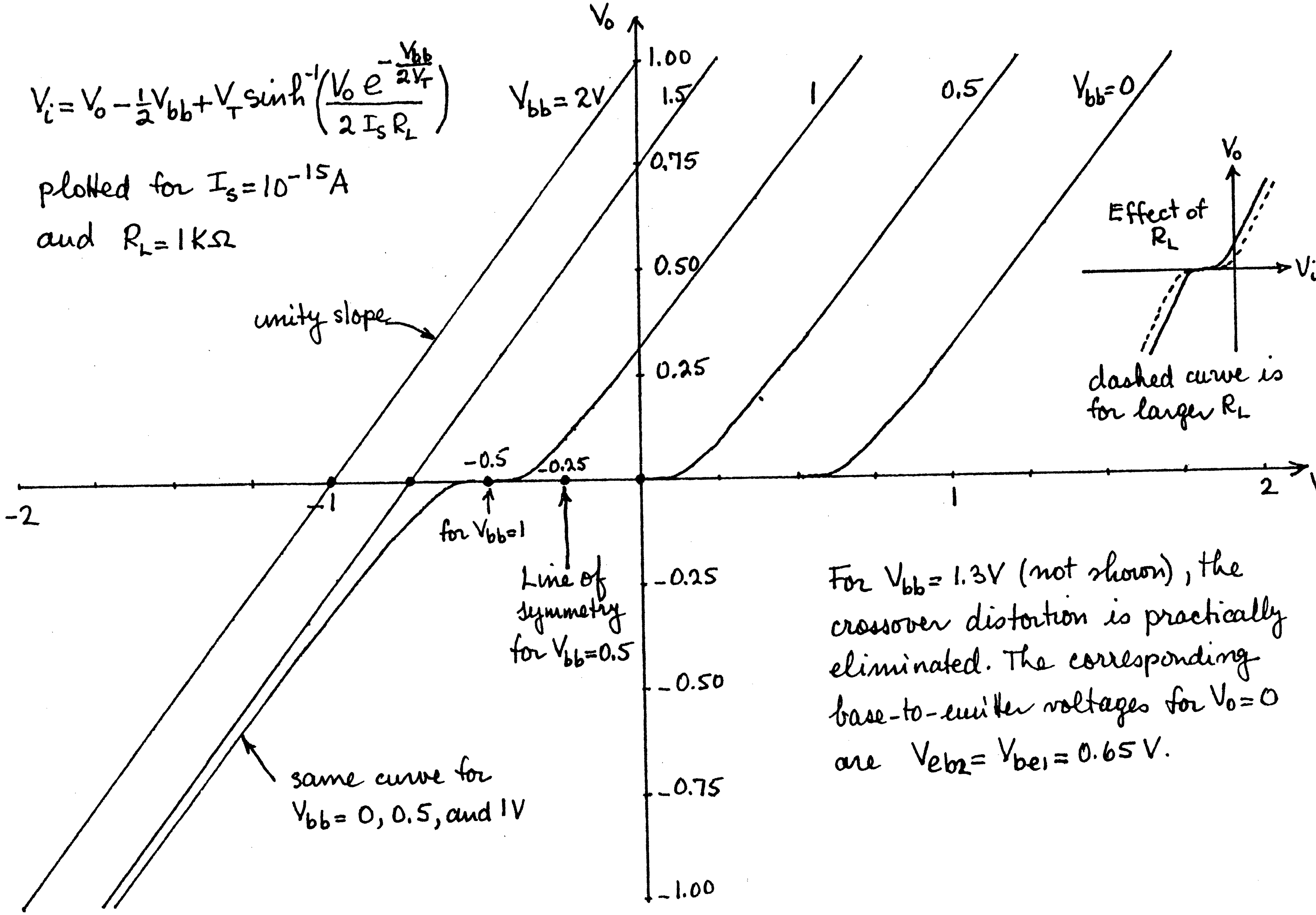
$$V_o \cong V_i + \frac{1}{2}V_{bb}$$

which represents a straight line of unity slope shifted up by $\frac{1}{2}V_{bb}$.

The exact equation that includes the sinh term is plotted accurately on the next page. Note the straight line behavior for V_{bb} large.

$$V_i = V_o - \tfrac{1}{2}V_{bb} + V_T \sinh^{-1}\left(\frac{V_o\, e^{-\frac{V_{bb}}{2V_T}}}{2 I_S R_L}\right)$$

plotted for $I_s = 10^{-15}$A and $R_L = 1K\Omega$



For V_{bb}= 1.3V (not shown), the crossover distortion is practically eliminated. The corresponding base-to-emitter voltages for $V_o=0$ are $V_{eb2} = V_{be1} = 0.65$ V.

Requirement for reduction of crossover distortion

A measure of the amount of crossover distortion can be obtained by evaluating the slope of the transfer characteristic at $V_o=0$ and $V_i=\frac{1}{2}V_{bb}$ which represents the line of symmetry.

$$V_o = 2R_L I_s e^{\frac{1}{2}\frac{V_{bb}}{V_T}} \sinh\left(\frac{V_i - V_o + \frac{1}{2}V_{bb}}{V_T}\right)$$

$$\frac{dV_o}{dV_i} = 2R_L I_s e^{\frac{1}{2}\frac{V_{bb}}{V_T}} \left(\frac{1-\frac{dV_o}{dV_i}}{V_T}\right)\cosh\left(\frac{V_i - V_o + \frac{1}{2}V_{bb}}{V_T}\right)$$

$$\frac{dV_o}{dV_i} = \frac{\left(2R_L I_s e^{\frac{1}{2}\frac{V_{bb}}{V_T}}/V_T\right)\cosh\left[\left(V_i - V_o + \frac{1}{2}V_{bb}\right)/V_T\right]}{1 + \frac{2R_L I_s e^{\frac{1}{2}\frac{V_{bb}}{V_T}}}{V_T}\cosh\left(\frac{V_i - V_o + \frac{1}{2}V_{bb}}{V_b}\right)}$$

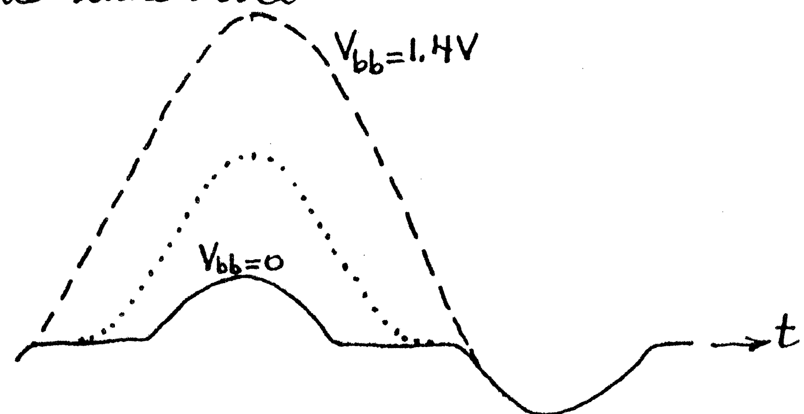
$$\left.\frac{dV_o}{dV_i}\right|_{\substack{V_o=0\\ V_i=-\frac{1}{2}\frac{V_{bb}}{V_T}}} = \frac{2R_L I_s e^{\frac{1}{2}\frac{V_{bb}}{V_T}}/V_T}{1 + 2R_L I_s e^{\frac{1}{2}\frac{V_{bb}}{V_T}}/V_T} = \boxed{\frac{1}{1 + \frac{V_T}{2R_L I_s e^{\frac{1}{2}\frac{V_{bb}}{V_T}}}}}$$

The closer the value of the slope to unity at the midpoint of crossover, the less the distortion.

For various values of V_{bb}, the slope at crossover is given below for $I_s = 10^{-15}$ A and $R_L = 1K$.

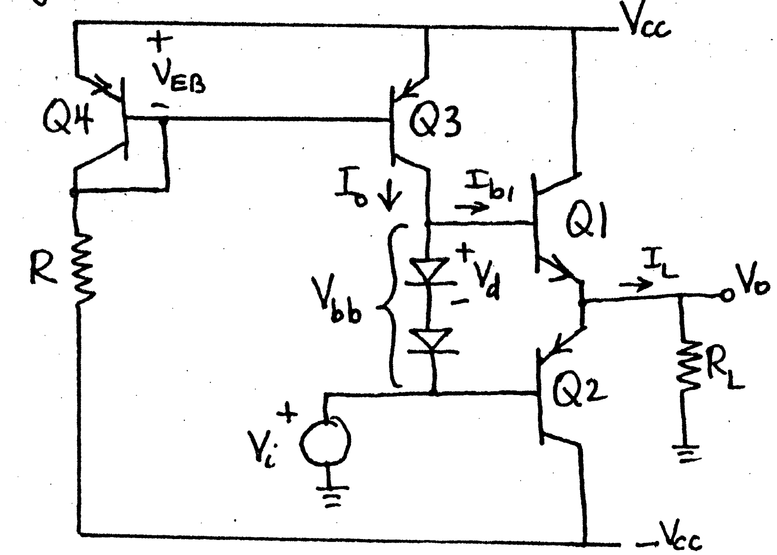
$\frac{1}{2}V_{bb}$	0.60	0.65	0.70
$\left.\frac{dV_o}{dV_i}\right\|_{\text{at crossover}}$	0.447	0.847	0.974

Except for $V_{bb}=0$, the transfer curve is not symmetric about $V_i=0$. As a result, as V_{bb} is increased from 0, an input sine wave of fixed amplitude will produce an output sine wave the positive portion of which progressively moves up while the lower portion remains at the same level.



As a result, for $V_{bb}>0$, the average value of the output is not 0. When the crossover distortion is negligible, the dc shift is $\frac{1}{2}V_{bb}$.

Generation of V_{bb}



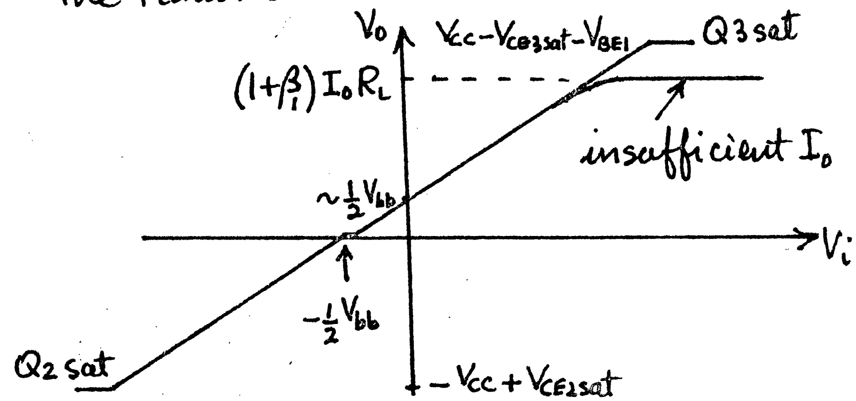
Q3 is a current source the value of which is fixed by Q4. $I_o = (2V_{cc} - V_{EB})/R$. If we neglect the base current taken by Q1, then

$$V_{bb} = 2V_d = 2V_T \ln \frac{I_o}{I_s}$$

Thus by changing the value of I_o, V_{bb} can be contolled. However, if I_o is made too low, the current taken by the base of Q1 when V_i goes to a large positive value cannot be neglected (relative to I_o) particularly for heavy loads (low values of R_L). Thus as V_i goes more and more positive, a progressively larger portion of I_o is shunted to the base of Q1 thereby reducing the current through the diodes. This results in lower V_{bb} for $V_i > 0$. (For $V_i < 0$, the base current of Q_2 is supplied by the signal source V_i.) Indeed, I_L can become current limited if all of I_o is used to supply I_{b1} in which case

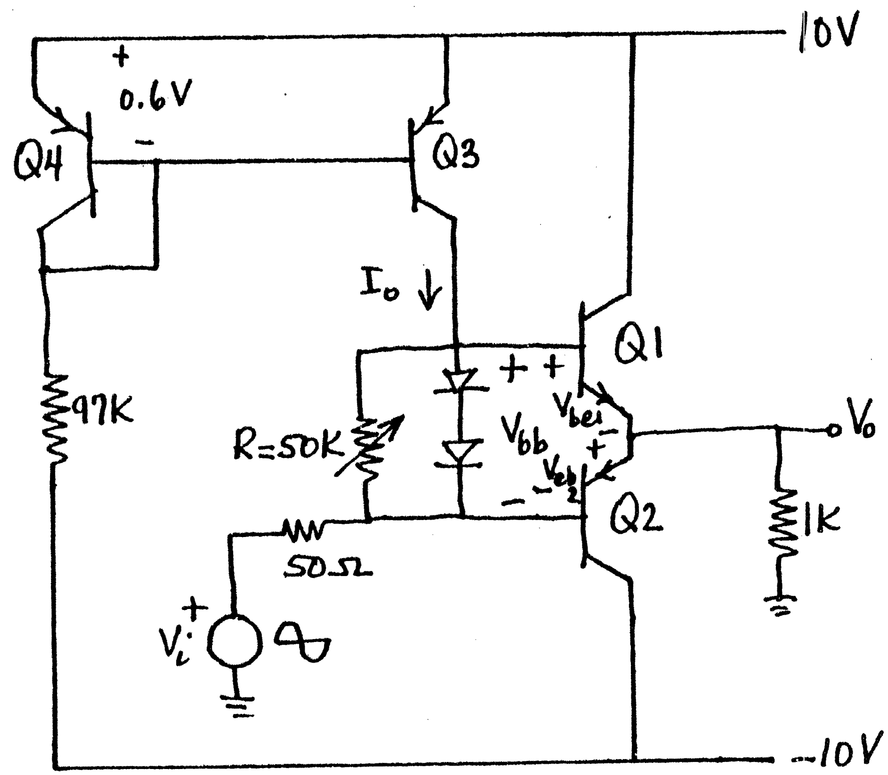
$$V_o = (1+\beta_1) I_o R_L$$

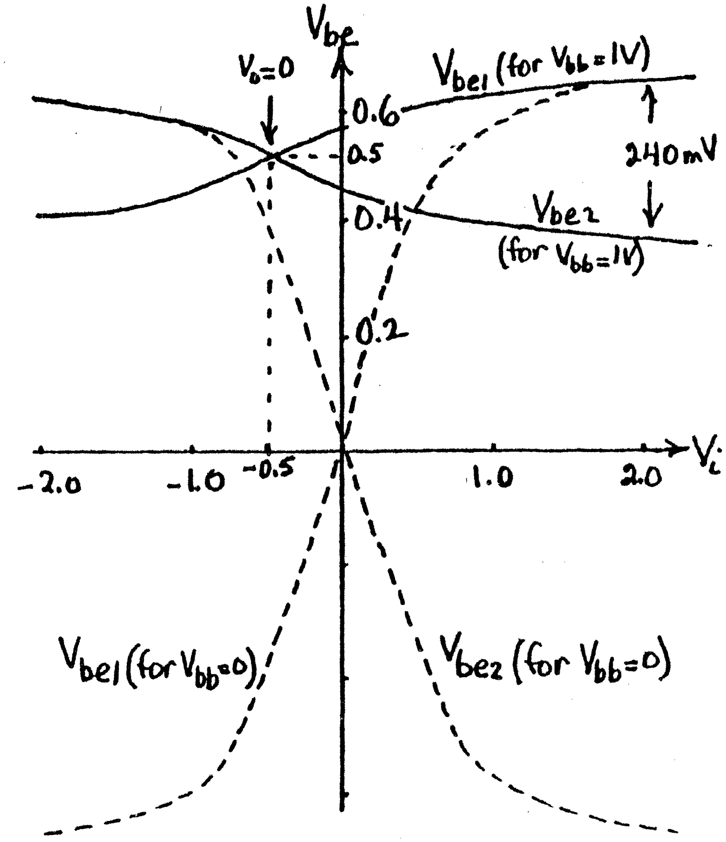
Any further increase in V_i produces no change in V_o. The result is a flattening of the transfer curve as shown below.



An increase of I_o or decrease in the load (larger R_L) reduces this unwanted distortion for V_i large.

Class-AB amplifier demonstration



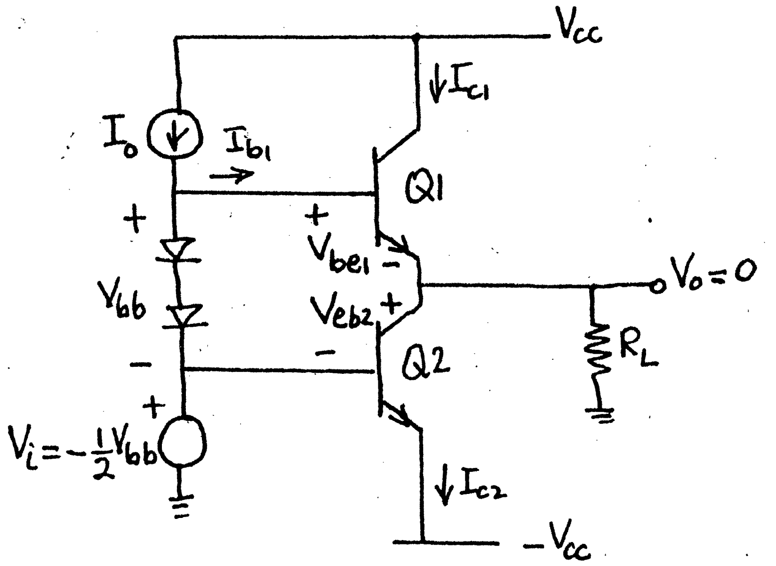


$$I_o = \frac{20-0.6}{97} = 0.2\,mA$$

As a function of R show
- V_o vs V_i
- V_o and V_i waveforms
- V_{be1} and V_{eb2} vs V_i

at $V_i = 2V$, $V_{be1} - V_{be2} = 240$ mV.
This means $I_{c1} = 10^4 I_{c2}$ if $I_{SNPN} = I_{SPNP}$.

More flexible control of V_{bb}



When $V_o=0$, $I_{c1}=I_{c2}$ and therefore $V_{be1}=V_{eb2}=\frac{1}{2}V_{bb}$ which occurs for $V_i=-\frac{1}{2}V_{bb}$. Assuming I_{b1} negligible relative to I_o, we can evaluate V_{bb}.

$$V_{bb}=2V_T \ln\frac{I_o}{I_{SD}} = \text{Two diode voltages}$$

The resulting collector currents are

$$I_{c1}=I_{c2}=I_s e^{\frac{1}{2}\frac{V_{bb}}{V_T}}=I_s e^{\ln\frac{I_o}{I_{SD}}}=I_o\left(\frac{I_s}{I_{SD}}\right)$$

As is generally the case, the saturation currents I_s of the output transistors are larger than the saturation currents I_{SD} of the diodes or diode connected transistors. For $I_s=5I_{SD}$,

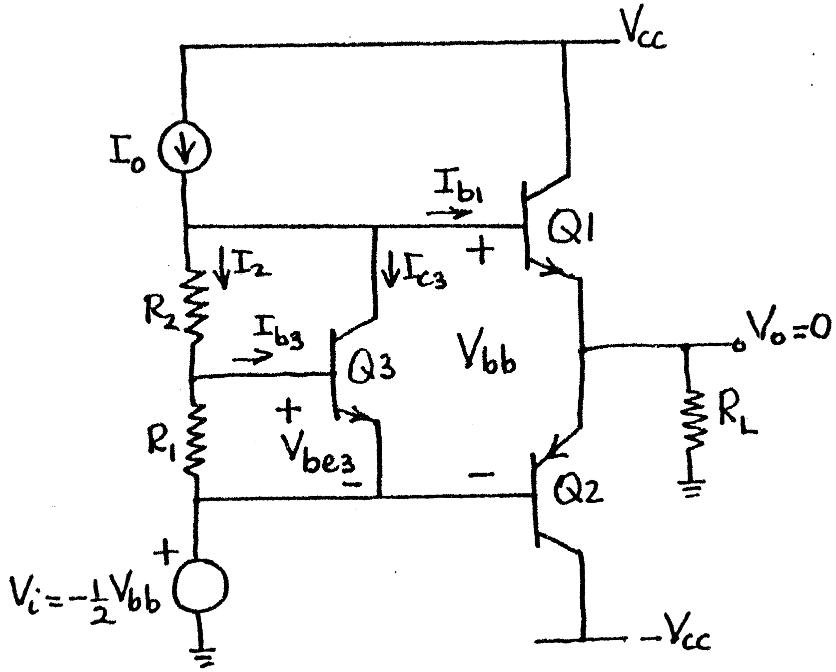
$$I_{c1}=I_{c2}=5I_o$$

To make these stanby collector currents small, I_o must be small. However, making I_o small causes premature clipping of the output waveform as V_i swings to large positive values (see discussion on p142).

To make the standby collector currents small, we could use one diode instead of two to generate V_{bb}. This, however, will result in too small standby currents and therefore will produce too much crossover distortion.

What is needed is the generation of a <u>V_{bb} that can be adjusted to fall between one and two diode voltages</u>. Two circuits for obtaining a wide range of control over V_{bb} are presented and discussed on the following pages.

Circuit 1

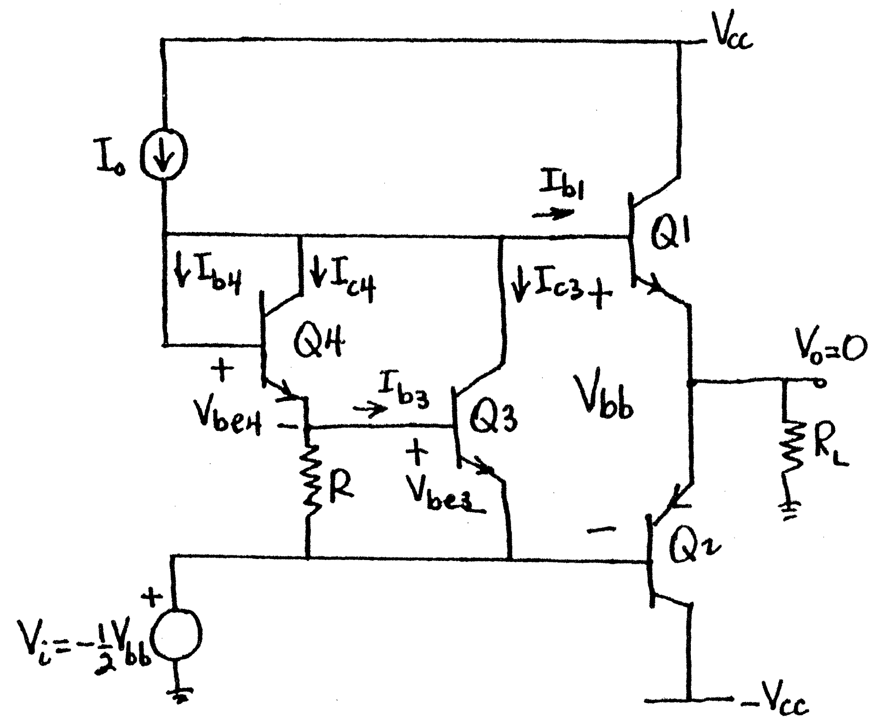


Assume that I_2 and I_{b1} are negligible in comparison to I_o. This implies that $I_{c3} = I_o$. Further assume that I_{b3} is negligible relative to I_2. Then

$$V_{bb}\,\frac{R_1}{R_1+R_2} = V_{be3} = V_T \ln \frac{I_{c3}}{I_S} \cong V_T \ln \frac{I_o}{I_S}$$

$$\boxed{V_{bb} = \underbrace{\left(1+\frac{R_2}{R_1}\right)}_{\text{multiplier}} \underbrace{V_T \ln \frac{I_o}{I_S}}_{\text{one diode voltage}}}$$

Circuit 2



<u>If $R = 0$</u>, $V_{be3} = 0$, $I_{c3} = 0$. Neglecting I_{b1} and I_{b4} relative to I_o, we obtain

$$I_{c4} \cong I_o$$

$$V_{bb} = V_{be4} = V_T \ln \frac{I_{c4}}{I_S} = \underbrace{\boxed{V_T \ln \frac{I_o}{I_S}}}_{\text{one diode voltage}}$$

Now suppose that R is adjusted to <u>split I_o evenly between I_{c3} and I_{c4}.</u>

$I_{c3} = I_{c4} = \frac{I_o}{2}$ (I_{b4} neglected)

$V_{bb} = V_{be3} + V_{be4} = 2V_{be3}$ since I_c's are same.

$$V_{bb} = 2V_T \ln \frac{I_{c3}}{I_s} = 2V_T \ln \frac{I_o/2}{I_s} = 2V_T\left(\ln\frac{I_o}{I_s} - \ln 2\right)$$

$$\boxed{V_{bb} = \underbrace{2V_T \ln \frac{I_o}{I_s}}_{\text{two diode voltages}} - 36\,mV}$$

The resistance R required to obtain this V_{bb} can be determined from

$I_{c4} R \cong V_{be3}$ (I_{b3} and I_{b4} neglected)

$$\frac{I_o}{2} R = \frac{1}{2} V_{bb}$$

$$\boxed{R = \frac{V_{bb}}{I_o}}$$

It can be shown that this value of R results in the largest possible V_{bb}. Any increase of R beyond this value results in a slight decrease of V_{bb}.

Thus, by adjusting R <u>any V_{bb} from one diode voltage to practically two diode voltages can be generated</u>.

To obtain V_{bb} for any R, proceed as follows.

$I_o = I_{c3} + I_{c4}$ (I_{b4} and I_{b1} neglected)

$= I_{c3} + \left(\frac{I_{c3}}{\beta_3} + \frac{V_{be3}}{R}\right)$ (I_{b4} neglected)

$$\boxed{I_o = I_{c3}\left(1 + \frac{1}{\beta_3}\right) + \frac{V_T}{R} \ln \frac{I_{c3}}{I_s}}$$

Solve this equation by trial and error for I_{c3}. Then obtain I_{c4} from

$$I_{c4} = I_o - I_{c3}$$

Using these values of I_{c3} and I_{c4}, obtain V_{bb} from

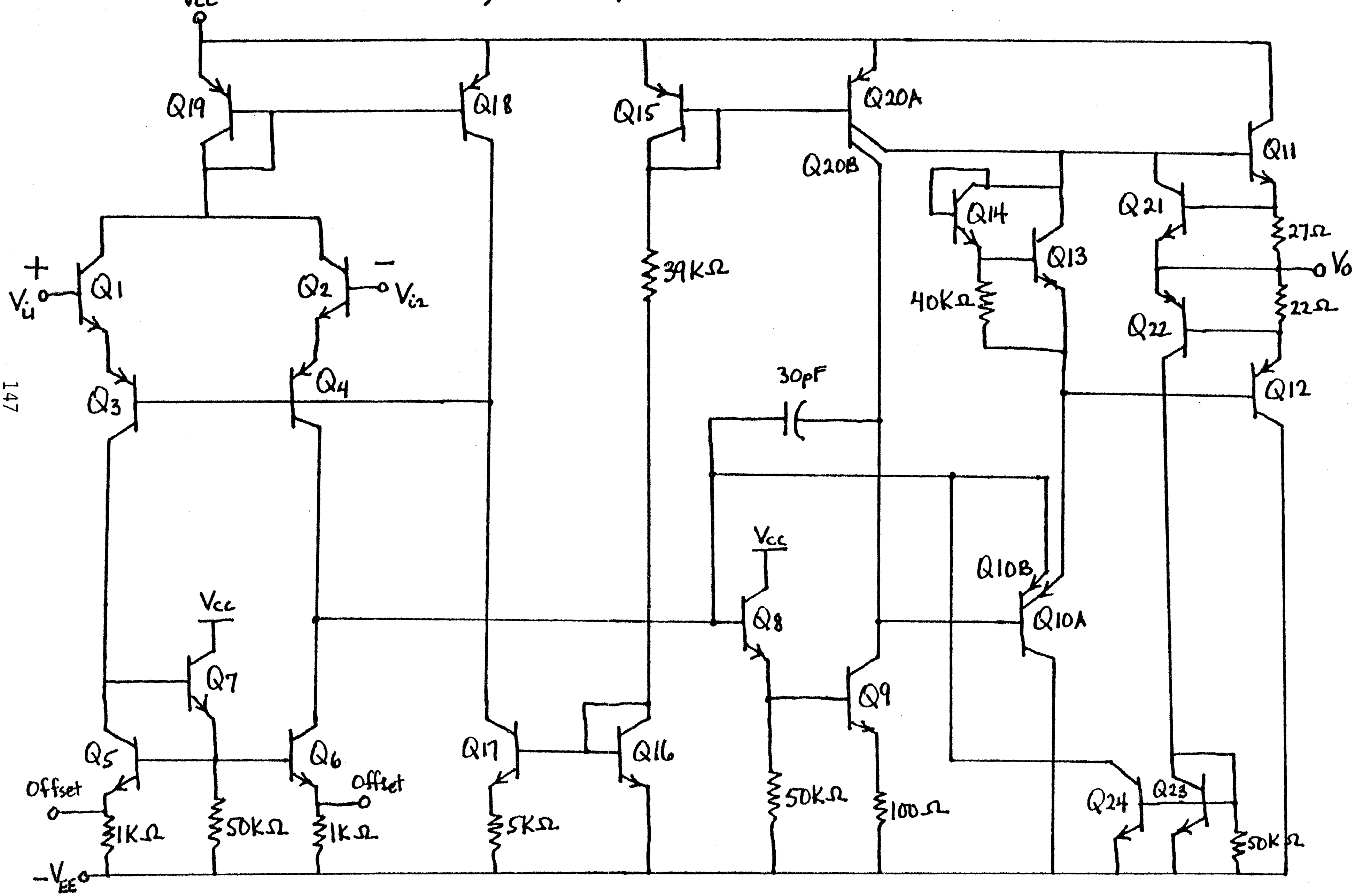
$$V_{bb} = V_{be3} + V_{be4}$$

$$= V_T \ln \frac{I_{c3}}{I_s} + V_T \ln \frac{I_{c4}}{I_s}$$

$$\boxed{V_{bb} = V_T \ln\left(\frac{I_{c3} I_{c4}}{I_s^2}\right)}$$

L19:

The μA741 Operational Amplifier



Current sources used for biasing

Assume $I_{S17} = I_{S16} = I_S$

$I_{17}\, 50K + V_{BE17} = V_{BE16}$

$I_{17}\, 50 + V_T \ln \frac{I_{17}}{I_S} = V_T \ln \frac{I_{15}}{I_S}$

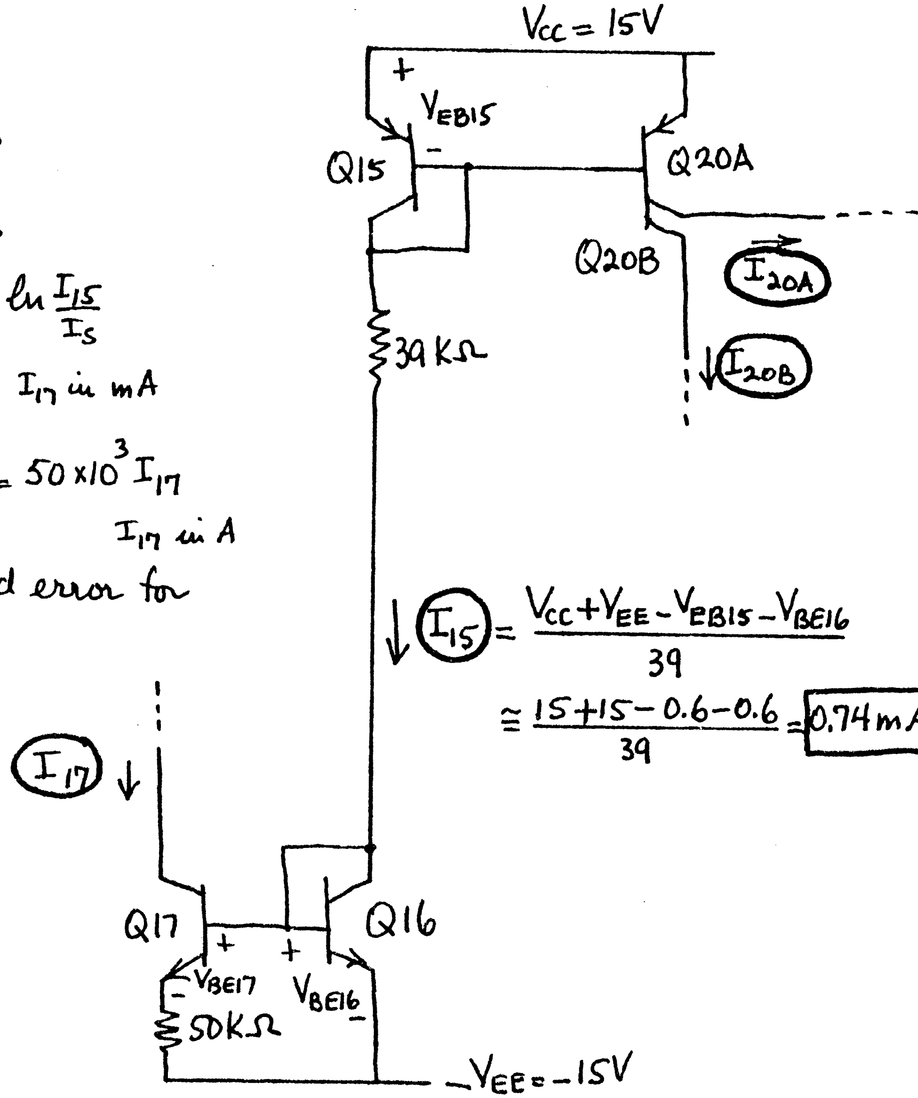
$V_T \ln \frac{I_{15}}{I_{17}} = 50\, I_{17}$ $\quad I_{17}$ in mA

$26\times10^{-3} \ln \frac{0.74\times10^{-3}}{I_{17}} = 50\times10^{3}\, I_{17}$

I_{17} in A

Solve by trial and error for

$\boxed{I_{17} = 19\mu A}$



$I_{15} = \frac{V_{CC} + V_{EE} - V_{EB15} - V_{BE16}}{39}$

$\cong \frac{15+15-0.6-0.6}{39} = \boxed{0.74 mA}$

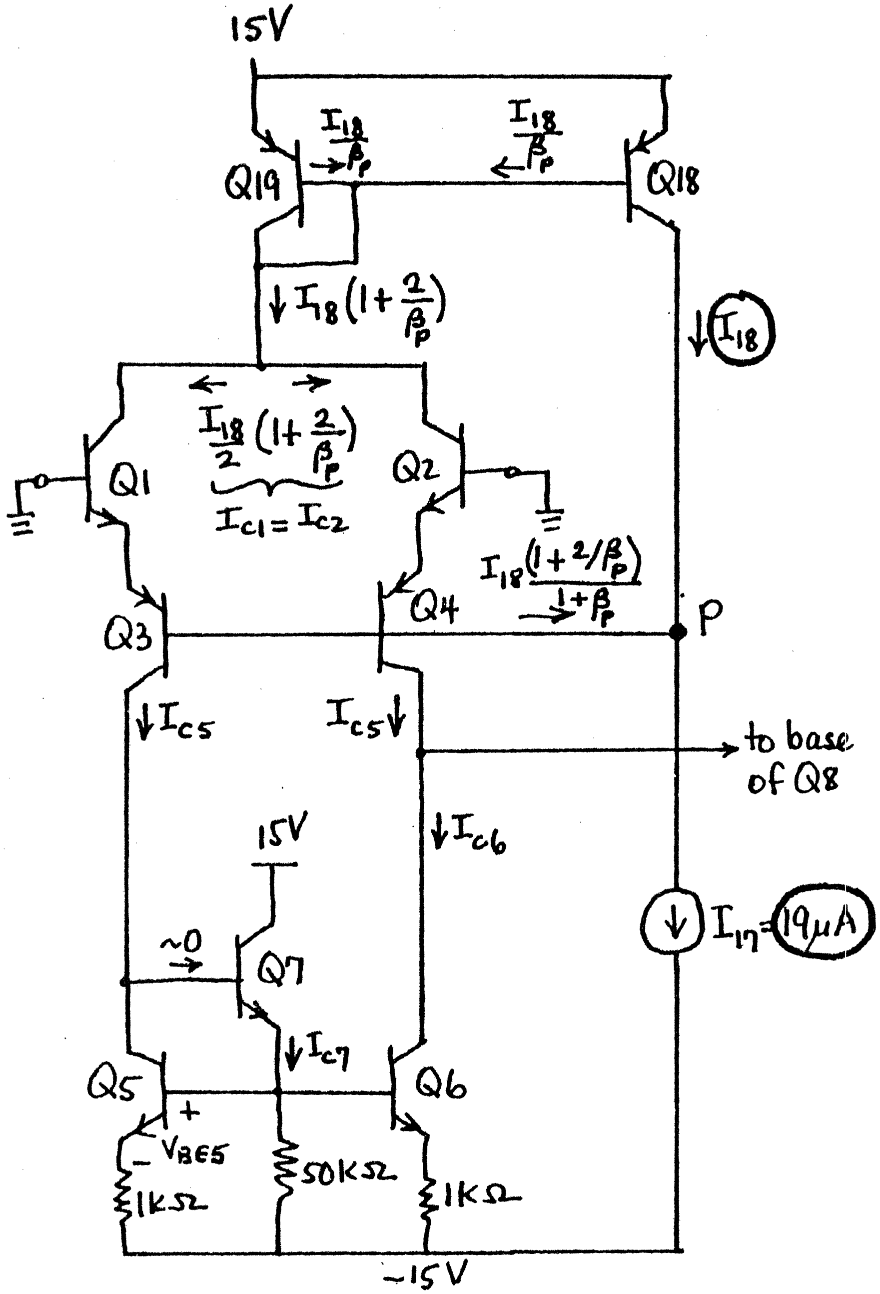
$I_{S15} = I_S$

$I_{S20A} = \frac{1}{4} I_S \quad I_{S20B} = \frac{3}{4} I_S$

$I_{20A} = \frac{1}{4} I_{15} = \frac{0.74}{4} = \boxed{0.19 mA}$

$I_{20B} = \frac{3}{4} I_{15} = \frac{3}{4} \times 0.74 = \boxed{0.56mA}$

Bias Currents of the input stage



With $I_{17}=19\mu A$ obtained from the previous page, we now calculate I_{18} by assuming matched pairs Q18 and Q19, Q1 and Q2, Q3 and Q4, Q5 and Q6. Since the β of the NPN transistors is high, the NPN base currents will be neglected. On the other hand, the PNP base currents will be included in the calculations because their β's are not so high.

Summing currents at node P, we obtain

$$I_{18}\left[1+\left(1+\frac{2}{\beta_p}\right)/\left(1+\beta_p\right)\right] = I_{17}$$

$$I_{18} = I_{17}\,\frac{\beta_p^2+\beta_p}{\beta_p^2+2\beta_p+\beta_p} \cong I_{17} = \boxed{19\mu A}$$

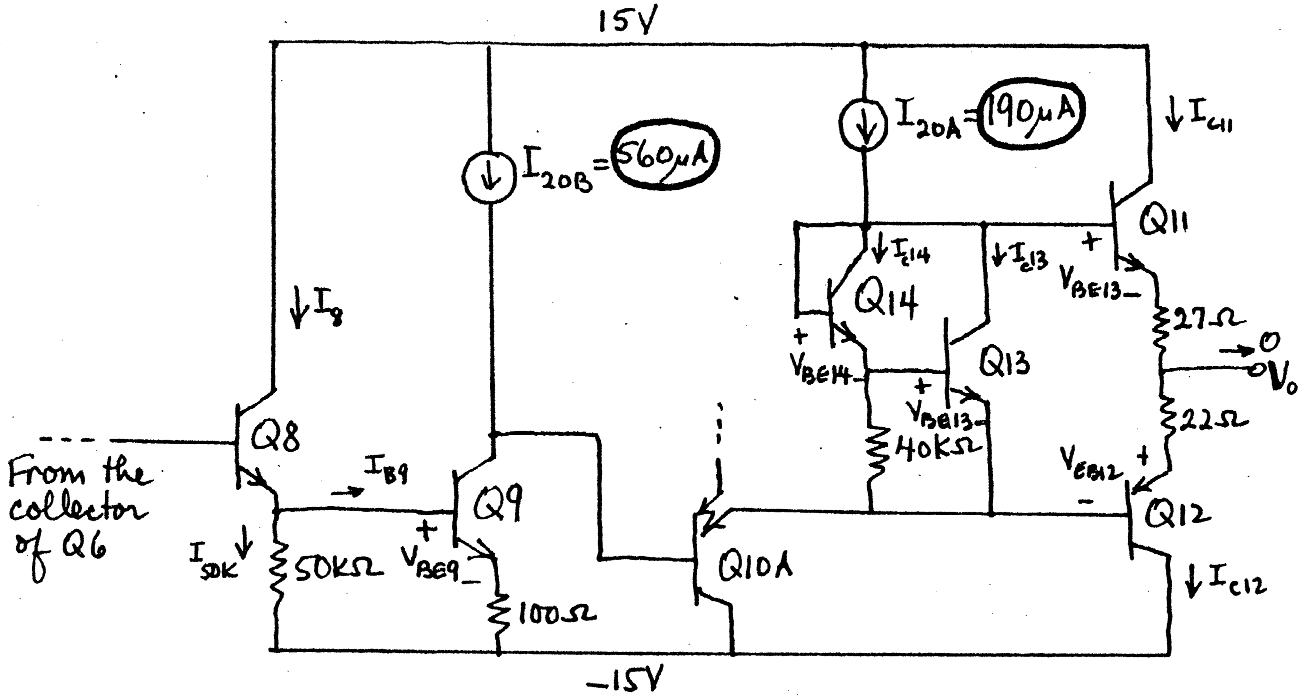
$$I_{C1}=I_{C2}=\frac{I_{17}}{2}\left(\frac{\beta_p^2+3\beta_p+2}{\beta_p^2+2\beta_p+2}\right) = \begin{cases} \beta_p=5: & \simeq 10.8\mu A \\ \beta_p=\infty: & = \boxed{9.5\mu A} \end{cases}$$

Thus the operating currents of Q1, Q2, Q3 and Q4 are well stabilized against variations in β_p.

$$I_{C5} \cong I_{C1} = I_{C6} \cong \boxed{9.5\mu A}$$

$$I_{C7}\,50K = V_{BE5} + I_{C5}\times 1K \qquad I_{C7} = \left.\frac{V_T \ln\frac{I_{CS}}{I_S} + I_{CS}}{50}\right|_{I_S=10^{-14}} = \boxed{11\mu A}$$

Bias currents in the intermediate and output stages



Note that the base of Q8 is about two V_{BE} above –15V.

The 560μA current source fixes V_{BE9} (neglect I_{B10A}).

$$V_{BE9} = V_T \ln \frac{I_{20B}}{I_s}\Big|_{I_s = 10^{-14}} = 644\,mV$$

$$I_8 = I_{50K} + I_{B9} = \frac{V_{BE9} + I_{20B}\,100\Omega}{50K} + \frac{I_{20B}}{\beta_9}\Big|_{\beta_9 = 250} = \boxed{16\mu A}$$

To determine I_{c13} and I_{c14}, assume $V_{BE13} = 612\,mV$ and check to see whether the resulting $I_{c13} + I_{c14} = I_{20A} = 190\mu A$. $I_{c13} = I_s e^{\frac{V_{BE13}}{V_T}} = 10^{-14} e^{\frac{612}{26}} = \boxed{167\mu A}$

$$I_{c14} = \frac{I_{c13}}{\beta_{13}} + \frac{V_{BE13}}{40K}\Big|_{\beta_{13} = 100} = \boxed{17\mu A}$$

$I_{c13} + I_{c14} = 167 + 17 = 184\mu A$ (which is close enough to 190μA)

To determine $I_{C11} = I_{C12}$, use the relationship between the base-to-emitter voltages.

$$V_{BE11} + V_{EB12} = V_{BE13} + V_{BE14}$$

$$V_T \ln \frac{I_{C11}}{I_{S11}} + V_T \ln \frac{I_{C12}}{I_{S12}} = V_T \ln \frac{I_{C13}}{I_{S13}} + V_T \ln \frac{I_{C14}}{I_{S14}}$$

$$\frac{I_{C11}\, I_{C12}}{I_{S11}\, I_{S12}} = \frac{I_{C13}\, I_{C14}}{I_{S13}\, I_{S14}}$$

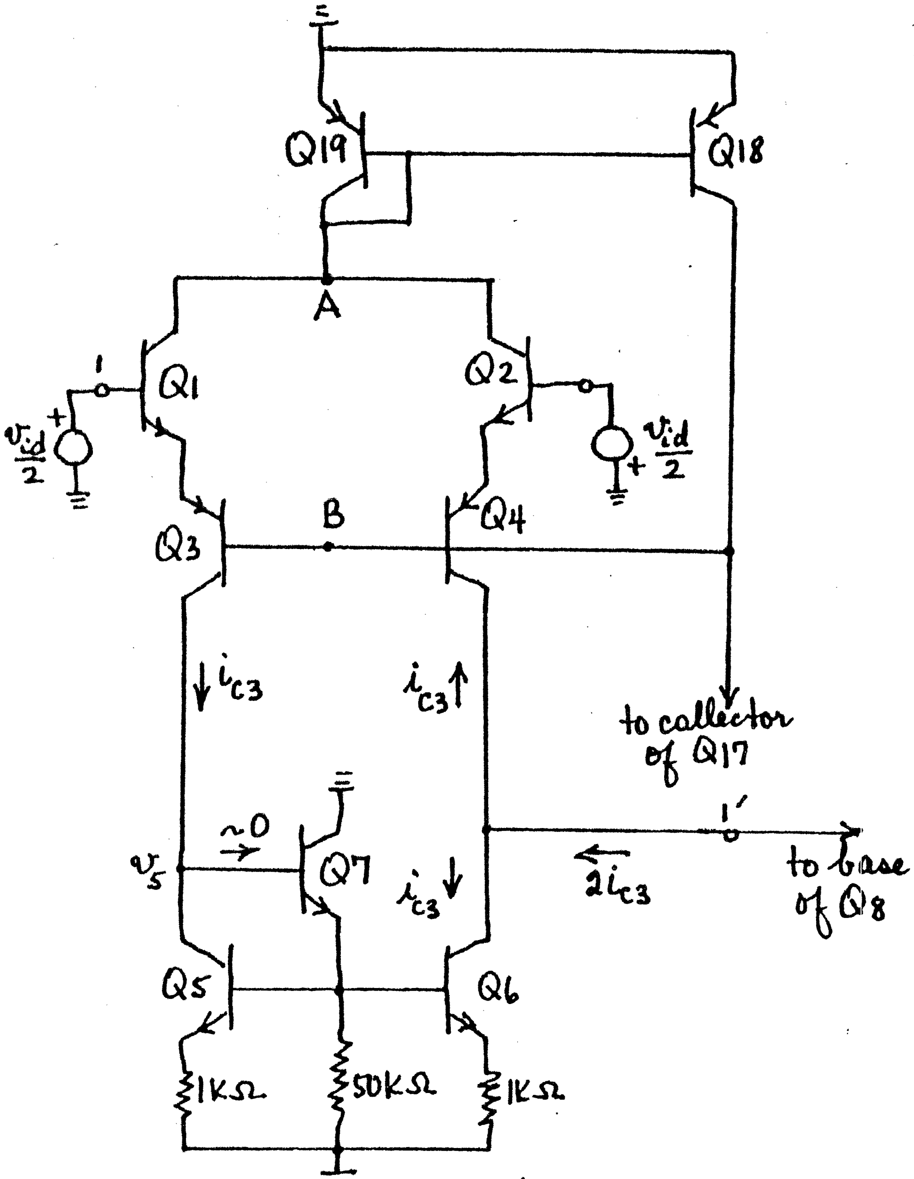
$$I_{C11} = I_{C12} = \sqrt{I_{C13} I_{C14}} \sqrt{\frac{I_{S11} I_{S12}}{I_{S13} I_{S14}}}$$

With $I_{C13} = 167\mu A$, $I_{C14} = 17\mu A$ and $I_{S13} = I_{S14} = \frac{1}{3} I_{S11} = \frac{1}{3} I_{S12}$ we obtain

$$I_{C11} = I_{C12} = 3\sqrt{I_{C13} I_{C14}} = 3\sqrt{167 \times 17} = \boxed{160\mu A}$$

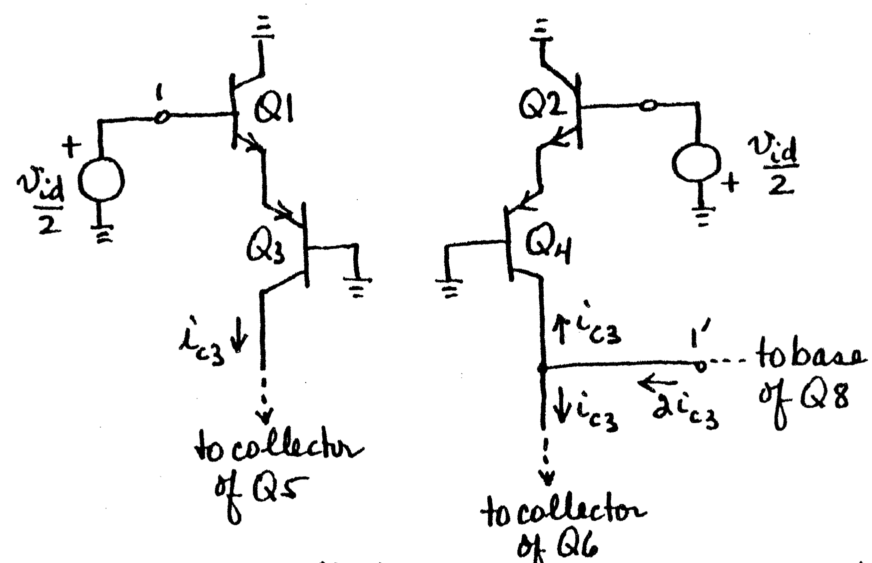
Note: With both inputs grounded V_o will fluctuate over wide limits. Feedback to the – input terminal stabilizes V_o.

Small-signal analysis : input stage



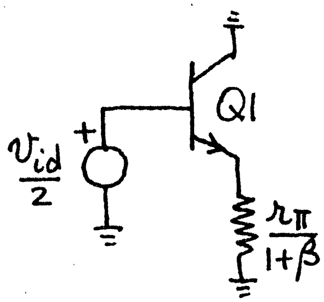
See also discussion given on pp109–117.

Except for the base connection of Q7, the circuit is symmetrical about the mid line. Since signals in the collectors of Q3 and Q4 have negligible effect on their bases and emitters, nodes A and B can be grounded inspite of the lack of symmetry of the lower half of the circuit. Furthermore, because Q6 mirrors the current of Q5 (i_{b7} can be neglected), $i_{c6} = i_{c5} = i_{c3}$ as shown. Consequently the circuit can be drawn as shown below.



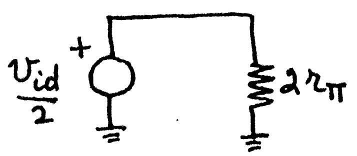
Since all collector currents (with the exception of Q7) have the same dc value, <u>all r_π's and g_m's are the same</u>.

Input equivalent faced by source $\frac{v_{id}}{2}$



$$r_\pi = \frac{26}{I_{B1}} = \frac{26}{I_{C1}/\beta}\ \mathrm{K}$$

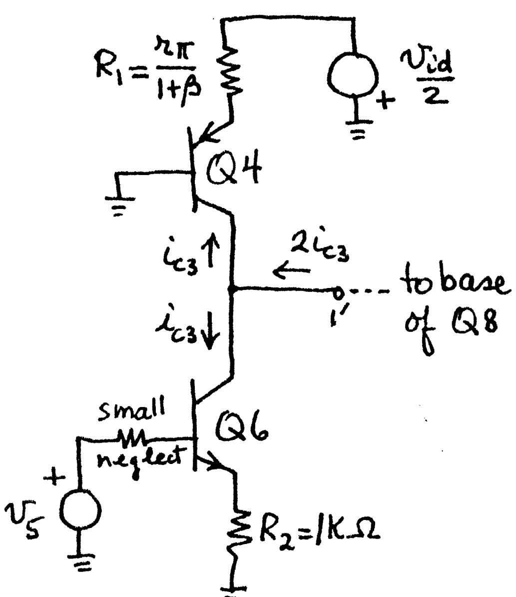
$$= \frac{26}{9.5/250} = \boxed{684\mathrm{K}}$$



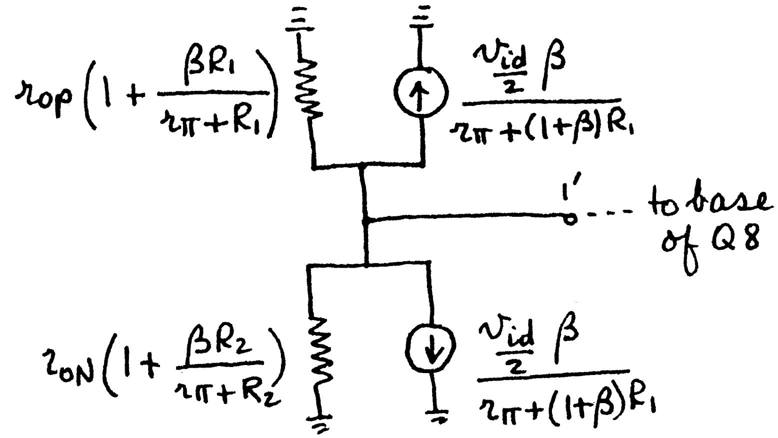
Source v_i faces

$\boxed{4r_\pi}$

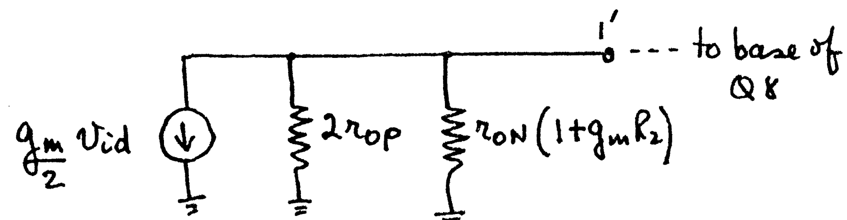
Output equivalent of the input stage



Making use of the results presented on p37, we obtain



Since $r_\pi \gg R_2$ and $R_1 = \frac{r_\pi}{1+\beta}$, we obtain



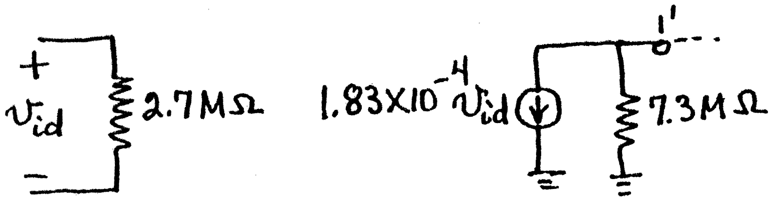
$$g_m = \frac{I_{C1}}{V_T} = \frac{9.5\times10^{-6}}{26\times10^{-3}} = 3.65\times10^{-4}$$

$$r_{op} = \frac{V_{AP}}{I_{C1}} = \frac{60}{9.5\times10^{-6}} = 6.3\ \mathrm{M\Omega}$$

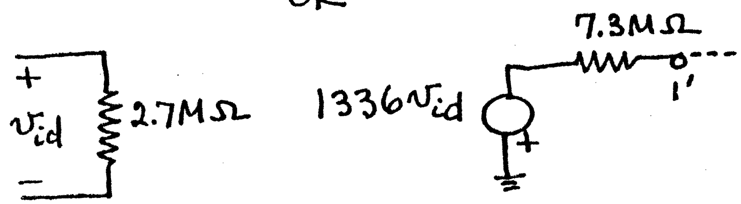
$$r_{oN} = \frac{V_{AN}}{I_{C1}} = \frac{120}{9.5\times10^{-6}} = 12.6\mathrm{M\Omega}$$

$$r_{oN}(1+g_m R_2) = 12.6\left(1+\frac{9.5}{26}\right) = 17.2\mathrm{M\Omega}$$

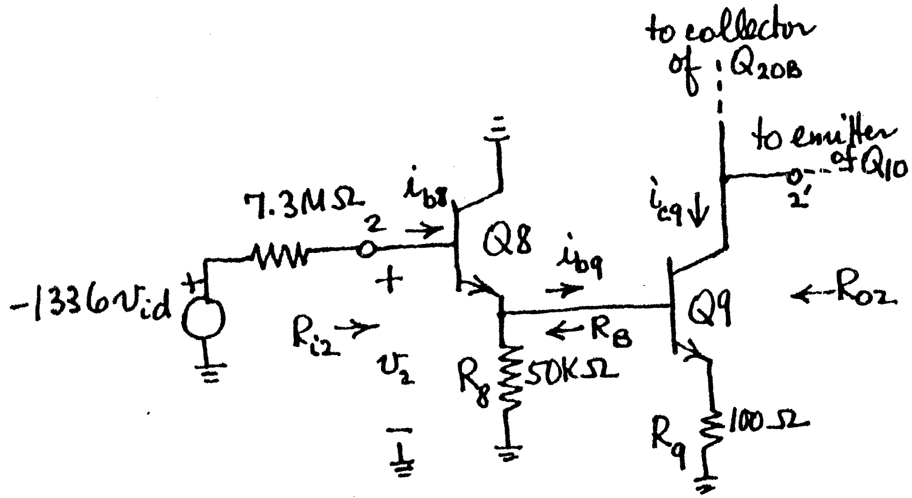
Equivalent circuit of input stage



OR



The intermediate stage



In calculating voltages and currents, assume r_o's are infinite and $\beta_8 = \beta_9 = 250$.

$$R_{i2} = r_{\pi 8} + (1+\beta_8)\left\{R_8 \,\|\, [r_{\pi 9} + (1+\beta_9)R_9]\right\}$$

$$r_{\pi 8} = \frac{26}{I_{B8}} = \frac{26}{I_{C8}/\beta_8} = \frac{26\times 250}{16} = 406.3\,K\Omega$$

$$r_{\pi 9} = \frac{26}{I_{B9}} = \frac{26}{I_{C9}/\beta_9} = \frac{26\times 250}{560} = 11.6\,K\Omega$$

$$R_{i2} = 406.3 + 251\left\{50 \,\|\, [11.6 + 251\times 0.1]\right\} = \boxed{5.7M\Omega}$$

$$i_{b8} = \frac{v_2}{R_{i2}} = \frac{v_2}{5.7}\,\mu A$$

$$i_{b9} = i_{b8}(1+\beta_8)\frac{R_8}{R_8 + r_{\pi 9} + (1+\beta_9)R_9}$$

$$= \frac{v_2}{5.7}\times 251 \times \frac{50}{50 + 11.6 + 251\times 0.1}$$

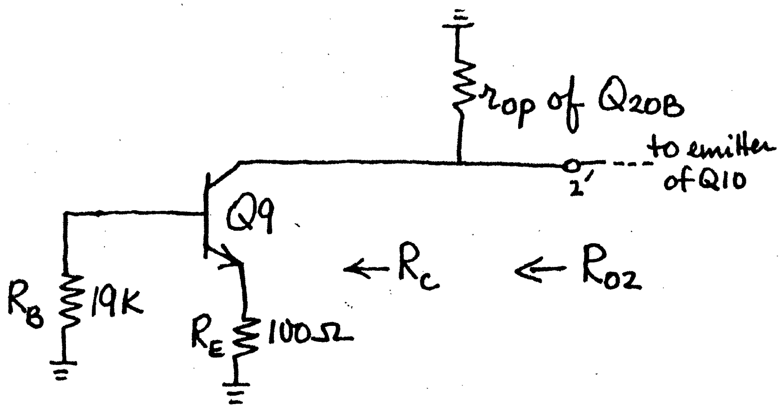
$$= 25.4 v_2\,\mu A = 0.0254 v_2\ mA$$

$$i_{c9} = \beta_9 i_{b9} = 250\times 0.0254 v_2 = 6.35 v_2$$

In the calculation of the output resistance R_{o2}, we must include the output resistance 7.3 MΩ of the previous stage. First, we calculate R_B.

$$R_B = \frac{(7.3M + r_{\pi 8})}{1+\beta_8} \,\|\, R_8 = \left(\frac{7300+406.3}{251}\right)\|50 = 19K\Omega$$

So far r_o's have been assumed infinite. For the calculation of R_{o2}, however, we have to use $r_{o9} = r_{oN}$ and $r_{o20B} = r_{oP}$.



Using the results of p37, we obtain

$$R_C = r_{oN}\left[1 + \frac{R_E\left(\beta_9 + \frac{R_B + r_{\pi 9}}{r_{oN}}\right)}{R_B + r_{\pi 9} + R_E}\right]$$

where $r_{oN} = \dfrac{V_{AN}}{I_{C9}} = \dfrac{120}{0.56} = 214.3\,K\Omega$

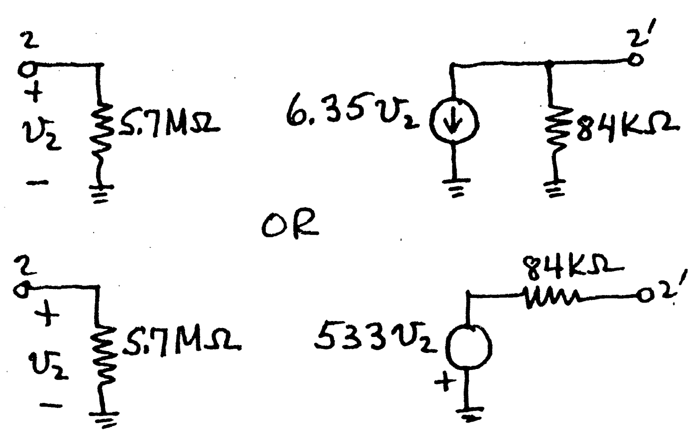
$$r_{op} = \frac{V_{AP}}{I_{C20B}} = \frac{60}{0.56} = 107.1\,K\Omega$$

$$R_C = 214.3\left[1 + \frac{0.1\left(250 + \frac{19 + 11.6}{214.3}\right)}{19 + 11.6 + 0.1}\right] = 388.9K$$

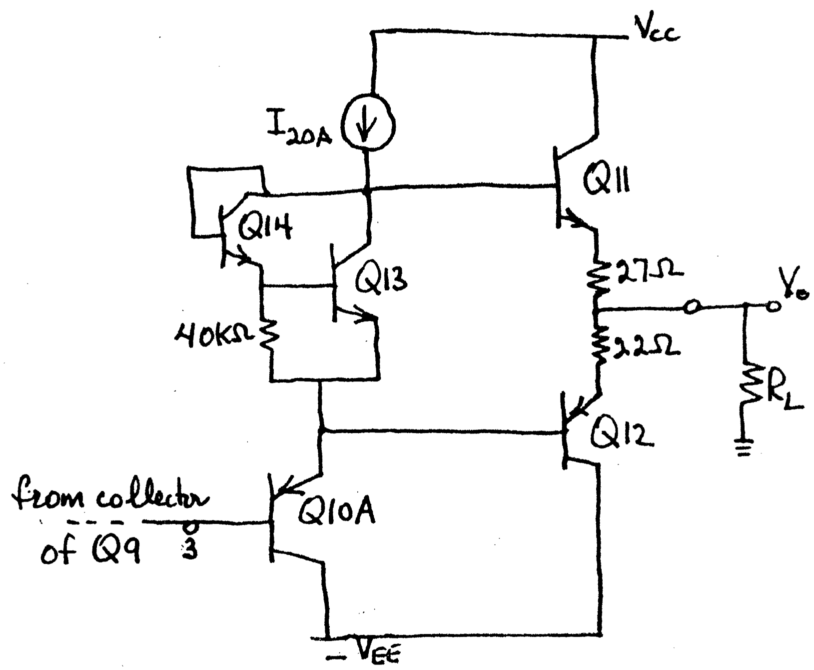
$$R_{o2} = R_C \,\|\, r_{op} = 388.9 \,\|\, 107.1 = \boxed{84\,K\Omega}$$

If we had taken r_o's as infinite, the output resistance R_{o2} would have come out infinite which is not a realistic result in comparison to the actual 84KΩ.

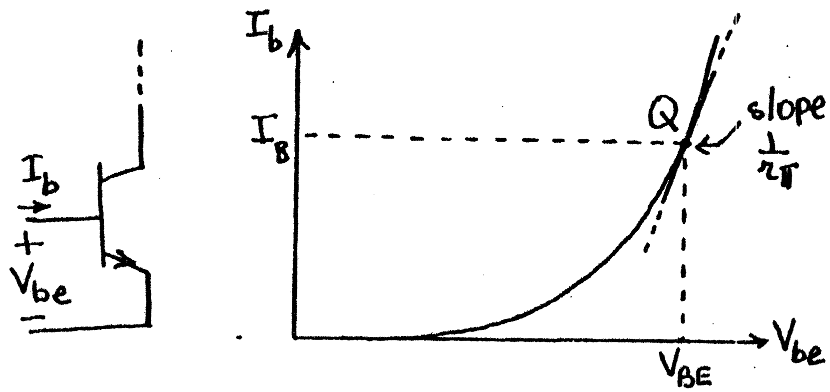
Equivalent circuit of intermediate stage



The output stage with driver



Meaninglessness of $r_{\pi 11}$ and $r_{\pi 12}$



When the transistor is biased such that operation is about the quiescent point Q and does not depart too far from it, then any change along the exponential can be approximated by following the straight line tangent to the exponential at the point Q.

$$I_b = \frac{I_s}{\beta} e^{\frac{V_{be}}{V_T}}$$

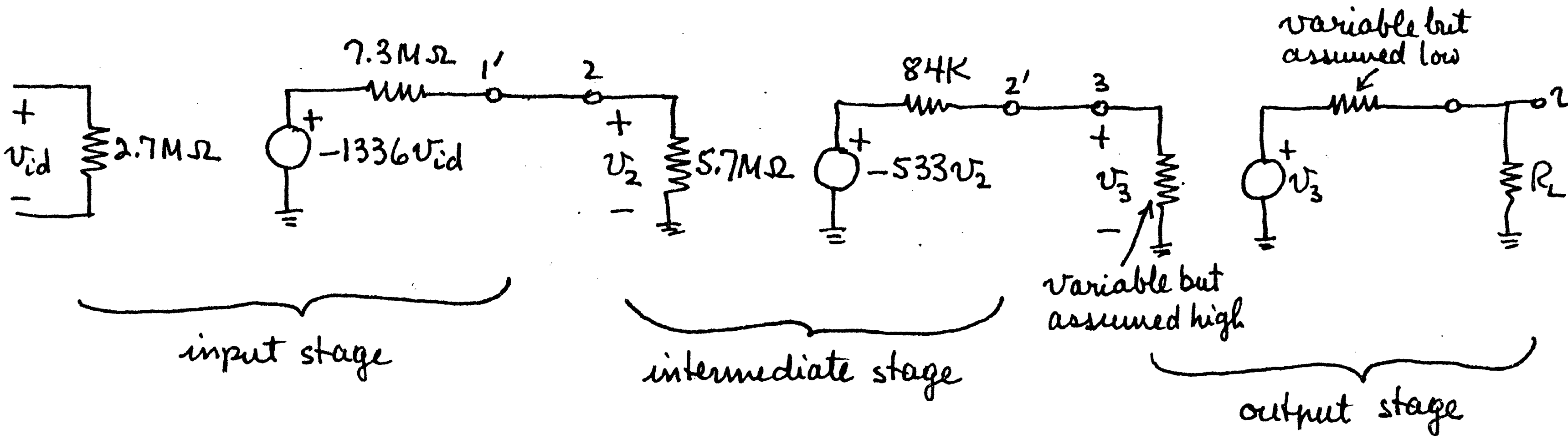
$$\frac{dI_b}{dV_{be}} = \frac{I_s}{\beta V_T} e^{\frac{V_{be}}{V_T}}\Bigg|_{V_{be}=V_{BE}} = \frac{I_s e^{\frac{V_{BE}}{V_T}}}{\beta V_T} = \frac{I_B}{V_T} = \frac{1}{r_\pi}$$

Thus $\Delta I_b = \frac{1}{r_\pi}\Delta V_{be}$ or $i_b = \frac{v_{be}}{r_\pi}$

(Also see discussion presented on p 11.)

As long as operation is confined to the vicinity of the quiescent point, r_π has meaning and can be used in the calculation of small signal voltages and currents. In the class-AB output stage however, transistors Q11 and Q12 are operated not at or about a point but rather along a wide span of the exponential and therefore the slope changes from very high values to very low values as the sinusoidal signal goes through a cycle of operation. Therefore, to speak of a single value for r_π is totally meaningless and results in highly erroneous values for voltages and currents.

However, in our discussion of the class-AB output stage (see pp138–143), we saw that the transfer curve, the V_o vs V_i characteristic, is quite linear if the crossover distortion is eliminated. Furthermore, the slope is practically unity. Hence, without introducing any significant error, the output stage including the emitter-follower-driver Q10A can be assumed to have unity gain. Also the variable loading presented by the base of Q10A on the output of the intermediate stage can be considered negligible. Similarly, the loading of R_L on the output stage can be assumed to have negligible effect on the gain. Hence, the complete equivalent circuit can be put together as shown below.

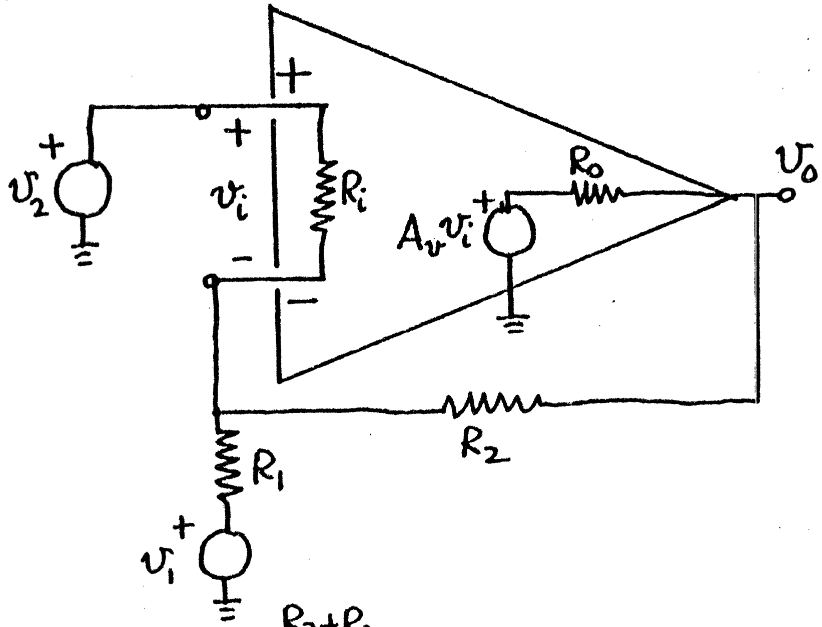


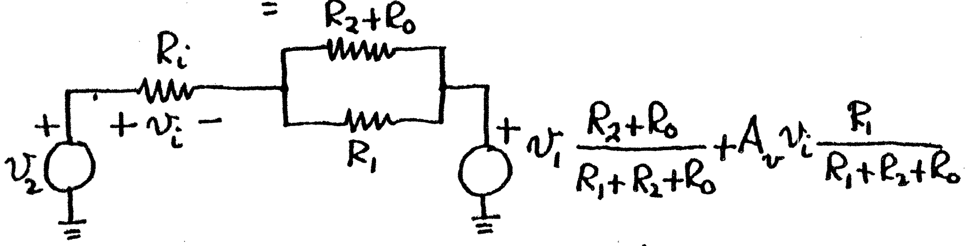
$$v_o \cong v_3 \cong -533v_2 = (-533)\left[(-1336v_{id})\underbrace{\left(\frac{5.7}{7.3+5.7}\right)}_{\substack{\text{reduction of}\\ \text{gain caused}\\ \text{by loading of}\\ \text{int. stage}}}\right] \cong \boxed{312000\, v_{id}} = A_v v_{id}$$

$$A_v = 312000$$

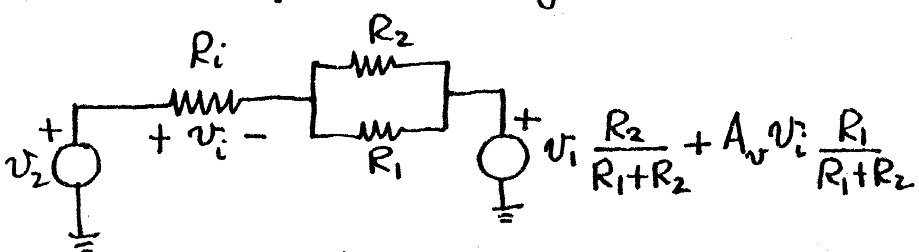
It should be realized that this gain of 312000 will not stay constant since it depends on temperature, power supply voltages, common-mode level at the input and other factors. However, vary as it may, it will always be a large number, and this is what is wanted in an operational amplifier.

To stabilize the gain, use feedback





Even though not clearly defined, assume $R_o \ll R_2$.



$$v_o = A_v v_i$$

$$v_i = \frac{\left[v_2 - \left(v_1 \frac{R_2}{R_1+R_2} + A_v v_i \frac{R_1}{R_1+R_2}\right)\right] R_i}{R_i + R_1R_2/(R_1+R_2)}$$

$$v_i = \frac{\left(v_2 - v_1 \frac{R_2}{R_1+R_2}\right) \frac{R_i}{R_i + R_1R_2/(R_1+R_2)}}{1 + A_v \frac{R_1}{R_1+R_2}\left(\frac{R_i}{R_i + R_1R_2/(R_1+R_2)}\right)}$$

$$v_o = A_v v_i$$

$$\boxed{v_o = \frac{v_2\left(1+\frac{R_2}{R_1}\right) - v_1 \frac{R_2}{R_1}}{1 + \frac{\left(1+\frac{R_2}{R_1}\right)}{A_v}\left(1 + \frac{R_1R_2}{R_1+R_2}/R_i\right)}}$$

As is almost invariably the case,

$$\frac{1+\frac{R_2}{R_1}}{A_v} \ll 1 \quad \text{and} \quad \frac{R_1R_2}{R_1+R_2}/R_i \ll 1,$$

in which case the expression of v_o simplifies to

$$\boxed{v_o = v_2\left(1+\frac{R_2}{R_1}\right) - v_1 \frac{R_2}{R_1}}$$

which is independent of A_v and R_i. For $R_1 = 1\,K\Omega$, $R_2 = 100\,K\Omega$, $A_v = 312000$, and $R_i = 2.7\,M\Omega$, we have

$$v_o = \frac{101\,v_2 - 100\,v_1}{1 + \frac{101}{312000}\left(1 + \frac{100}{101}/2700\right)} = \frac{101 v_2 - 100 v_1}{1.00032}$$

INDEX

Useful formulas

$$r_\pi = \frac{V_T}{I_B} = \frac{26}{I_{B\mu A}}\ K\Omega$$

$$g_m = \frac{I_C}{V_T}$$

$$\beta = g_m r_\pi$$

$$r_o = \frac{V_A}{I_C}$$